Swept Neutral Pressure Instrument (SNeuPI): Investigating Gravity Waves In The Ionosphere

Vidur Garg

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Gregory D. Earle, Chair
Dennis G. Sweeney
Scott M. Bailey

7 August 2015
Blacksburg, Virginia

Keywords: Space, Vacuum, Ions, Electrons, Analog and Digital Design
Swept Neutral Pressure Instrument (SNeuPI): Investigating Gravity Waves In The Ionosphere

Vidur Garg

Abstract

A swept neutral pressure instrument (SNeuPI) is used to study the effect of gravity waves on the composition of the ionosphere. When mounted on a nanosatellite in the low earth orbit, changes in atmospheric pressure due to gravity waves are measured as the changes in neutral gas density. This measurement is achieved by use of micro-tip emitters as an electron source and micro channel plates (MCPs) as ion collectors. Ionization of the neutral gas produces a current at the output of the MCPs to quantify the pressure of the ionosphere. Traditionally, such measurements are made on larger satellites which enable the use of higher power equipment. This thesis describes the design and use of a low power instrument, to be used on a limited-resource satellite. The background and theoretical analysis is presented first, followed by descriptions of the mechanical and electrical designs. The laboratory tests are limited to a vacuum chamber setup that simulates the conditions of the ionosphere.
Acknowledgements

I would like to thank my adviser Dr. Gregory Earle for his guidance and patience through the entire project. I would also like to thank members of the Space@VT team - Stephen Noel, Robbie Robertson, Cameron Orr, Peter Marquis, Lee Kordella, Grant Roth, Saurav Dhar, and Debbie Collins.

The author is indebted to the NSF for funding the CubeSat development effort through grant AGS-1242898.

Unless otherwise noted, all photographs by author, 2015.
# Table of contents

List of figures vi

List of tables ix

1 Introduction and Hypothesis 1
   1.1 Pressure measurements in space . . . . . . . . . . . . . . . . . . . . . . . . 1
   1.2 Need for a new swept neutral pressure instrument . . . . . . . . . . . . . . . 2
   1.3 Theoretical background . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2

2 Design Expectations and Simulation 4
   2.1 Mechanical limitations, emitter and ion collector selection . . . . . . . . . . . 4
   2.2 Simulation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9

3 Electronic Design 11
   3.1 Electronics requirements . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11
   3.2 Electronics overview . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12
   3.3 Electronics details . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13
      3.3.1 Power system . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15
      3.3.2 Communication . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15
      3.3.3 High voltage generation . . . . . . . . . . . . . . . . . . . . . . . . . 16
      3.3.4 Digital to analog conversion . . . . . . . . . . . . . . . . . . . . . . . . 16
      3.3.5 Trans-impedance amplifier . . . . . . . . . . . . . . . . . . . . . . . . 17
      3.3.6 Emitter control circuit . . . . . . . . . . . . . . . . . . . . . . . . . . . 21
      3.3.7 Analog to digital conversion . . . . . . . . . . . . . . . . . . . . . . . . 21
      3.3.8 MCP and emitter configuration in accommodation chamber . . . . . . 23

4 Digital Design 24

5 Laboratory Setup 33

6 Validation 37
   6.1 Upper board test results . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 37
      6.1.1 Digital to analog conversion . . . . . . . . . . . . . . . . . . . . . . . . 38
Table of contents

6.1.2 High voltage DC-DC conversion 40
6.1.3 Analog to digital conversion 43
6.2 Lower board test results 46
6.3 Validation of MCP-Emitter performance 49
6.3.1 Characteristics with emitters heated to 80°C 49
6.3.2 Characteristics with emitters heated to 185°C 53
6.3.3 Discussion of MCP-Emitter performance 56

7 Conclusion and Future Work 58
7.1 Conclusion 58
7.2 Future work 59

References 60

Appendix A Upper Board: Schematics and Bill of Materials 61
Appendix B Lower Board: Schematics and Bill of Materials 70
Appendix C Daughter Board: Schematics and Bill of Materials 73
Appendix D Digital Design Simulation Waveforms 76
Appendix E MATLAB Instrument Control 77
List of figures

1.1 Principle of operation of neutral density measurement .......................... 3
2.1 LAICE CubeSat accommodation chamber ........................................ 4
2.2 Spindt type field emitter ............................................................... 5
2.3 Front view of the emitter ............................................................... 5
2.4 APD 2 MiniTOF MCP assembly ...................................................... 6
2.5 Particle trajectory simulation of the SNeuPI instrument concept .......... 10
3.1 Block diagram of electronics ......................................................... 12
3.2 3D model of the upper board ....................................................... 13
3.3 3D model of the lower board ....................................................... 14
3.4 3D model of the lower board fitting into the upper board ................. 14
3.5 3D model of the daughter board .................................................. 15
3.6 Connections of power supplies to the MCP assembly ....................... 16
3.7 Negative to positive current inversion schematic .............................. 17
3.8 Laboratory test results for negative to positive current inversion .......... 18
3.9 Simulation circuit for end-to-end daughter board test ....................... 19
3.10 Simulation results of input current and output voltage on daughter board 20
3.11 Block diagram of charge pump circuit on lower board for emitter current control 21
3.12 CAD model of accommodation chamber with components mounted ...... 23
4.1 Flowchart depicting the process flow of the digital logic in the FPGA .... 25
4.2 Timing diagram of the FPGA with emphasis on communication and analog to digital conversion .............................................................. 29
5.1 First iteration test box mounted on the stands of a vacuum chamber .... 33
5.2 Second iteration test box ............................................................... 34
5.3 Setup for temperature sensing on the test box .................................. 34
5.4 Emitter held in place with a ceramic tube ....................................... 35
5.5 Halogen lamp used to heat the emitter array .................................... 35
6.1 Top view of the upper board ......................................................... 37
6.2 Bottom view of the upper board .................................................... 38
List of figures

6.3 Block diagram of DAC connections and high voltage generation on the upper board .................................................. 38
6.4 A short (11.5 s) example of the output voltage from Ch 1 on DAC ................................................................. 39
6.5 Voltage output from UMHV0505 at point B in Figure 6.3, controlled by DAC channel 2 ............................................. 40
6.6 A short example (14 s) of the output of the high voltage DC-DC converter ...................................................... 41
6.7 Gain of the HV DC-DC converter (UMHV0530N) when a control voltage is applied to its program pin using the DAC ................................................................. 42
6.8 Timing relationship between the two HV converters ......................................................................................... 42
6.9 Block diagram of the ADC flow chain .............................................................................................................. 43
6.10 Amplification and level shift of signal from the daughter board before conversion by ADC ............................................. 43
6.11 Calculated MCP current reading based on ADC output data .............................................................................. 44
6.12 Clamping action of Schottky diodes .............................................................................................................. 45
6.13 Picture of the 2.9"x 3.4" lower board with a slot cut out for converters on the upper board ............................................. 46
6.14 Block diagram depicting connections between the DAC and lower board ............................................................... 46
6.15 Voltage across a load resistor (between tips and gate connectors) when a control voltage is applied to the lower board ............................................................................. 47
6.16 Voltage proportional to emission current ...................................................................................................... 48
6.17 Measurement of tips to gate voltage on lower board when a control voltage is applied to the lower board using channel 4 of the DAC ..................................................... 48
6.18 Emission current measured on the walls of the test box that serves as a proxy for the accommodation chamber ................................................................. 49
6.19 Output current from the MCP .................................................................................................................... 50
6.20 Ratio of MCP current to electron emission current at a constant pressure of $10^{-5}$ Torr .............................................................................................................. 51
6.21 Emission current measured on the walls of the test box at low pressure .............................................................. 51
6.22 Current output from the MCP at low pressure, for various emission current settings .................................................. 52
6.23 Ratio of MCP current to emitter current at a constant pressure of $4 \times 10^{-5}$ Torr .......................................................... 52
6.24 Temperature in the ceramic tube behind the emitters during bake-out .............................................................. 53
6.25 Electron emission after bake out at 185 °C with a background pressure of $2.3 \times 10^{-7}$ Torr .......................................................... 54
6.26 Fowler-Nordheim plot of emitters after bake out at 185 °C with a background pressure of $2.3 \times 10^{-7}$ Torr .......................................................... 54
6.27 Background pressure inside vacuum chamber vs. MCP output current .............................................................. 55
6.28 The density of gas inside vacuum chamber vs. current out of the MCP .............................................................. 55

A.1 Upper board schematic: RS-422 communication .......................................................... 62
A.2 Upper board schematic: FPGA section .......................................................... 63
A.3 Upper board schematic: Digital to analog and high voltage converters . . . . . . 64
A.4 Upper board schematic: Voltage monitors . . . . . . . . . . . . . . . . . . . . 65
A.5 Upper board schematic: Power system 1 . . . . . . . . . . . . . . . . . . . . . 66
A.6 Upper board schematic: Power system 2 . . . . . . . . . . . . . . . . . . . . . 66
A.7 Upper board schematic: Analog to digital converter and multiplexer . . . . . . 67
A.8 Upper board schematic: Lower and daughter board connectors . . . . . . . . . 68

B.1 Schematic of lower board . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 71

C.1 Schematic of daughter board . . . . . . . . . . . . . . . . . . . . . . . . . . . 74

D.1 ModelSim simulation of the DAC control using FPGA . . . . . . . . . . . . 76
D.2 ModelSim simulation of the ADC control using FPGA . . . . . . . . . . . . 76
List of tables

1.1 Types of gauge measuring total pressure ........................................ 1
2.1 Expected output current at different altitudes .................................. 8
2.2 Device potentials used to simulate the SNeuPI concept using SIMION®. .... 9
2.3 SIMION® simulation parameters for the SNeuPI concept. ....................... 9
3.1 Electrical requirements of the SNeuPI systems .................................. 11
4.1 Communication uplink commands. .................................................... 26
4.2 Downlink data and conversion factors. .............................................. 30
4.3 FPGA implementation summary. ...................................................... 31
A.1 Bill of materials: SNeuPI upper board ............................................. 69
B.1 Bill of materials: SNeuPI lower board ............................................. 72
C.1 Bill of materials: SNeuPI daughter board ........................................ 75
Chapter 1

Introduction and Hypothesis

1.1 Pressure measurements in space

According to [3], when we talk about pressure measurement either in the lower atmosphere or in vacuum chambers, what we are usually concerned about is the number density ‘n’ (\(\text{particles/m}^3\)) of the gas present in a given region. The pressure of the lower atmosphere and ionosphere corresponds to the high and ultra high vacuum range. In this region, the atmospheric pressure varies from \(10^{-5}\) to \(10^{-7}\) Torr when the ram effect is taken into consideration.

Over the past few decades, there have been many instruments developed to measure the density of gas in a low-pressure environment. Some of these measure partial atmospheric pressure while others are used for total pressure calculations. Some are mechanical while others are ionization or current based instruments. Table 1.1 summarizes different types of gauges that are used to measure total pressure[3].

<table>
<thead>
<tr>
<th>Type</th>
<th>Principle</th>
<th>Min. Pressure (Torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barometric</td>
<td>Generally use mercury or oil. Limited to 0.75 torr pressure, 10% accuracy</td>
<td>0.75</td>
</tr>
<tr>
<td>Mechanical</td>
<td>Usually involving mechanical movement of a septum forming a wall of an evacuated enclosure</td>
<td>0.75</td>
</tr>
<tr>
<td>McLeod</td>
<td>Manometric principle, where the volume of a gas sample is lowered and resultant pressure is measured</td>
<td>(1 \times 10^{-6})</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>Decrease in thermal conductivity at low pressure results in increased thermal insulation</td>
<td>(1 \times 10^{-4})</td>
</tr>
<tr>
<td>Hot cathode ionization</td>
<td>Works by measuring the number of ions produced by collision of electrons with a gas beam</td>
<td>(1 \times 10^{-10})</td>
</tr>
<tr>
<td>Cold cathode ionization</td>
<td>Works by measuring current in a cold cathode discharge tube</td>
<td>(1 \times 10^{-12})</td>
</tr>
</tbody>
</table>
1.2 Need for a new swept neutral pressure instrument

While a large satellite normally has enough resources to support most low-pressure gauges discussed in section 1.1, a CubeSat or a nanosatellite doesn’t have similar resources. There are restrictions in terms of size, weight, and power. Magnetic interference also plays a role in the selection of some gauges. The hot-cathode ionization gauge has a proven track record of being able to accurately measure gas density in the micro Torr range. However, this type of device requires large currents at moderately high voltages for operation. This leads to significant power consumption and hence limits activity to short bursts on a CubeSat. The other current based gauge that could be used on a nanosatellite is the cold cathode or the Penning gauge [1]. However, this instrument has a powerful permanent magnet. The presence of a large DC magnet can lead to a malfunction of the spacecraft’s direction sensors when there is an interaction with the earth’s magnetic field. Hence, there exists a need to develop a new pressure measurement system.

Over the past several years, there has been a thrust by agencies such as NASA and NSF for the development of CubeSats for educational and scientific purposes. Budget limitations have contributed to this move towards smaller satellites, especially those with a mass under 10 kg. Our research group has spent the last year in developing a new robust method to measure neutral gas density in high vacuum conditions. This thesis describes the mechanical design, the electrical (analog and digital) design and the test process for the design of this instrument. We call it SNeuPI, which stands for Swept Neutral Pressure Instrument. It will fly aboard the LAICE (Lower Atmosphere/Ionosphere Coupling Experiment) satellite mission.

1.3 Theoretical background

The principle of pressure measurement by ionization is described in detail in [6]. When a stream of electrons passes through a neutral gas, the number of positive ions that are produced is directly proportional to the molecular concentration of the neutral gas. This is a linear relation, and it holds good from zero pressure to the point when the ion formation can sufficiently alter the energy of the electron stream. Since the ion concentration depends on the density of the gas, it may be used as a direct indication of the pressure. Thus, the idea is to develop an instrument that generates an energetic electron beam (e\(^{-}\)) and ionizes molecules (A) according to equation 1.1.

\[
A + e^{-} = A^{+} + 2e^{-} \quad (1.1)
\]

It is shown in [2] that the resulting ion current \(I^{+}\) is related to the electron current, \(I^{-}\) by equation 1.2

\[
I^{+} = nl\sigma I^{-} \quad (1.2)
\]

where ‘l’ is the average electron path length, ‘n’ is the molecular density, and ‘\(\sigma\)’ is the ionization probability. It has been shown that ionization probability reaches a maximum when the electron
1.3 Theoretical background

energy is between 80 to 120 eV. The sensitivity ‘K’ of the instrument at a pressure ‘p’ is thus expected to be

$$K = \frac{I^+}{I^-} \frac{mbar}{p}$$

(1.3)

Thus, the principle idea is to develop a system that has an electron emitter and an ion collector at its heart.

![Figure 1.1 Principle of operation of neutral density measurement. A stream of electrons ionizes neutral gas in a chamber. The resulting ion current is measured by an electrometer and is proportional to the density of the neutral gas.](image)

This idea is depicted in Figure 1.1. An electron source generates ions on the left, the neutral particle stream arrives from the top, and the ionized molecules are collected and read by a measuring device.
Chapter 2

Design Expectations and Simulation

2.1 Mechanical limitations, emitter and ion collector selection

The selection of the components required as mentioned in section 1.3 is restricted by the space available in an existing accommodation chamber of the LAICE CubeSat. A redesign of the chamber was not possible owing to existing mission requirements. A CAD model of the accommodation chamber is shown in Figure 2.1. The SNeuPI components are expected to sit in the right half.

![Figure 2.1 LAICE CubeSat accommodation chamber. SNeuPI components will be in the right half of the chamber, where the 32 pin golden connector is present.](image)

It was decided to use Spindt type field emitters developed by SRI International owing to prior experience on earlier missions. The principle of operation for these devices is explained in [4, Chapter 4]. These emitters work on the basis of electron emission from metal surfaces. A Spindt type field emitter consists of small, sharp, conductive cones to form a large-area field electron source. The emitter tips act as the cathode and a counter-electrode (called the “gate”) serves as a grid to shape the electron emission. The emitter tips are driven to a negative potential
2.1 Mechanical limitations, emitter and ion collector selection

with respect to the gate. Owing to its sharp apex, the emitter tips create a high electric field at a relatively low voltage. The electron emission from metals under intense electric fields is characterized by the well-known Fowler-Nordheim (F-N) equation [5]. The F-N equation predicts emission current \( I \) for an applied voltage \( V \) as follows

\[
I = aV^2 e^{-b/V}
\]

(2.1)

where

\[
a \approx 1.5 \times 10^{-6} \frac{A}{\phi^{1.4}} e^{10.4/\phi^{0.5}} \beta^2
\]

\[
b \approx 6.44 \times 10^7 \phi^{3/2}/\beta
\]

given,

- \( A \) is the emitting area in \( cm^2 \)
- \( \phi \) the cathode work function in eV and,
- \( \beta \) the geometric factor in \( cm^{-1} \) that determines the electric field \( E \) at the cathode such that

\[
E = \beta V
\]

Figure 2.2 shows a lateral view of an emitter array. Figure 2.3 shows a close up of the front face of an emitter mounted in a holding plate.

Figure 2.2 Spindt type field emitter. The emitter arrays are part of a T0-5 can.

Figure 2.3 Front view of the emitter.

Since the number of ions produced is expected to be very low owing to the low molecular concentration of gases, it is necessary to choose an ion collector that can multiply the ion current to values above the noise level, so that the external electronics can measure the resulting current.
Since commercially available channel electron multipliers (CEMs) from Photonis are made from a relatively thin glass and are brittle, they are not recommended for use on rocket flights [8]. A device called a micro channel plate (MCP) can provide a significant electron or ion gain. The gain of this device depends on the voltage difference between its plate and a collector. The typical configuration of such a plate is that the current gain is in the range of a few thousand. It is seen from [7], when either two or three MCP’s are used in a back to back configuration, their combined gain can be in the range of a few million.

A micro channel intensifies single particles by multiplication of electrons via secondary emission. In principle, the functionality is similar to an electron multiplier. A plate consists of ultra-small capillaries (tiny tubes) that are parallel to each other while being at a small angle to the surface. The MCP plate is biased to create a strong electric field. An ion that enters one of the micro channels hits the wall of the channel. The impact starts a cascade of electrons. Relative to the electric field strength, the original signal is amplified by several orders of magnitude. At the other end, a single anode is used to collect the electrons and measure the current.

The MCP setup selected here is of the chevron type, which consists of two micro-channel plates. The two plates are at 180° to each other, such that the capillaries on the two plates form a ‘V’ like shape. The electrons that exit one plate enter the second plate and continue to cascade. The advantage of this design is that the gain is much higher. The two plates and an anode are encompassed in a single package by Photonis, as shown in Figure 2.4, to form a device called the Advanced Performance Detector (APD2).

![Figure 2.4 APD 2 MiniTOF MCP assembly. Two micro channel plates are arranged in a chevron configuration. The output current is measured through the SMA connector at the back. The body of the SMA connector is connected to the body of the assembly and can be used to ground the assembly.](image)

The APD2 has the following specifications:

- Center-to-Center Spacing: 6\(\mu\)m nominal
- Pore Size: 5\(\mu\)m Nominal
2.1 Mechanical limitations, emitter and ion collector selection

- Bias Angle: 12° ± 1°
- High Voltage (MCP in and out): Feed through pin
- Output Signal: SMA
- Operating Pressure (Maximum): 1.0 × 10^{-5} Torr
- Maximum Specified Operating Voltage: 2400 Volts
- Bias Current Range @ 2000 Volts: 6-30 µA
- Gain (Minimum): 1.0 × 10^6 @ 2000 Volts
- Dark Count (Maximum): 2.5 cts/second
- Pulse Width (Minimum): 750 psec @ Half Height (Typical)

For the purpose of designing the measurement electronics, it is first necessary to estimate the output from the MCP assembly. This estimation can be realized by first estimating the amount of gas and its ionization. Using the MSIS-E-90 Atmosphere Model[9] we can find the number density of the neutral gas \( n_0 \). For Blacksburg, VA - 1 January 2015 at 12 pm, at an altitude of 350 km:

\[
 n_0 = 2.26 \times 10^{14} \text{ particles/m}^{-3}
\]

Considering a ram effect increase of 15 times, it is seen that the number density \( n_1 \) within the accommodation chamber is:

\[
 n_1 = 3.40 \times 10^{15} \text{ particles/m}^{-3}
\]

At a state of equilibrium the flux into the accomodation chamber is equal to the flux out of the accommodation chamber. The flux out the accommodation chamber is given by,

\[
 Flux = n_1 \times v_{th} \times A
\]

(2.2)

Where,

- \( n_1 \) is the number density seen above.
- \( v_{th} \) is the mean of the magnitude of the velocity of oxygen (O) molecules.
  - \( v_{th} = \sqrt{\frac{8k_B T}{m \pi}} \), where
  - Temperature of the gas \( T = 300 \text{ K} \)
  - \( k_B \) is the Blotzmann constant in J/K.
  - \( m \) is the mass of an atomic oxygen particle. Atomic oxygen is chosen for calculation as it is the dominant gas at these altitudes.
  \( \Rightarrow v_{th} = 630.06 \text{ m/s} \)
2.1 Mechanical limitations, emitter and ion collector selection

- A is the area of the aperture of the accommodation chamber
  - Aperture diameter \( d = 0.127 \) cm
  - Aperture radius \( r = d/2 = 0.0635 \) cm
  - Aperture area \( , A = \pi r^2 \)
    \[ \Rightarrow A = 1.267 \times 10^{-6} \text{ m}^2 \]

Substituting these values in equation 2.2, we get

\[
Flux = 2.71 \times 10^{12} \text{ particles/s.}
\]

Based on past experience, the ionization efficiency of the gas due the micro-tip electron emission is \( 10^{-6} \). Then the number of ions generated in the chamber is expected to be

\[
N_{ions} = 2.71 \times 10^{12} \times 10^{-6} \text{ ions/s}
\]

\[
N_{ions} = 2.71 \times 10^6 \text{ ions/s}
\]

The ion current will then be,

\[
I_{ion} = -e \times N_{ion}
\]

\[
I_{ion} = 1.602 \times 10^{-19} \times 2.71 \times 10^6
\]

\[
I_{ion} = 4.34 \times 10^{-13} \text{A} \approx 430 \text{ fA}
\]

As per the specification provided by Photonis, the APD2-MiniTOF is a 2-stack chevron-type MCP assembly. The combined gain of this device is 1 million at a control voltage of -1800 V. Therefore, the expected current out of the MCP is \( I_{out} = 430 \text{ nA} \). Table 2.1 shows the expected variation of the output current against the variation of altitude and background neutral gas density.

<table>
<thead>
<tr>
<th>Altitude (km)</th>
<th>Density ( n_0 ) at 12pm ( \text{ (particles/m}^3 )</th>
<th>Density ( n_0 ) at 1am ( \text{ (particles/m}^3 )</th>
<th>Output current ( I_{out} ) at 12pm ( \text{A} )</th>
<th>Output current ( I_{out} ) at 1am ( \text{A} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>( 7.91 \times 10^{15} )</td>
<td>( 6.96 \times 10^{15} )</td>
<td>( 1.52 \times 10^{-05} )</td>
<td>( 1.33 \times 10^{-05} )</td>
</tr>
<tr>
<td>250</td>
<td>( 2.07 \times 10^{15} )</td>
<td>( 1.88 \times 10^{15} )</td>
<td>( 3.97 \times 10^{-06} )</td>
<td>( 3.61 \times 10^{-06} )</td>
</tr>
<tr>
<td>300</td>
<td>( 6.51 \times 10^{14} )</td>
<td>( 6.27 \times 10^{14} )</td>
<td>( 1.25 \times 10^{-06} )</td>
<td>( 1.20 \times 10^{-06} )</td>
</tr>
<tr>
<td>350</td>
<td>( 2.26 \times 10^{14} )</td>
<td>( 2.32 \times 10^{14} )</td>
<td>( 4.34 \times 10^{-07} )</td>
<td>( 4.44 \times 10^{-07} )</td>
</tr>
</tbody>
</table>
2.2 Simulation

SIMION®, an ion optics simulation program is used to validate the SNeuPI instrument concept. The simulation objective is to estimate electric fields and particle trajectories in the instrument. The mechanical model drawn is an approximation of the actual accommodation chamber. For the purpose of simulation, the potentials on the various surfaces of the micro channel plate assembly and emitters are listed in Table 2.2.

Table 2.2 Device potentials used to simulate the SNeuPI concept using SIMION®.

<table>
<thead>
<tr>
<th>Surface</th>
<th>Value (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chamber wall</td>
<td>0</td>
</tr>
<tr>
<td>MCP front plate</td>
<td>-2000</td>
</tr>
<tr>
<td>MCP body</td>
<td>0</td>
</tr>
<tr>
<td>Emitter tips</td>
<td>-150</td>
</tr>
<tr>
<td>Emitter gate</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 2.5 depicts the position of the emitters with respect to the MCP assembly. The emitter tip voltage is chosen to be 150 V, such that with the gate at 0 V, the electrons coming out of the device will have a kinetic energy of 150 eV. The electrons are expected to slow down due to the large negative potential on the MCP, and the maximum ionization is expected to happen at the center of the chamber.

For the purpose of simulating the electrons and ions, their simulation parameters are listed in Table 2.3. Since the lower levels of the thermosphere (of which the ionosphere is a part), contains a large amount of atomic oxygen, this is chosen as the neutral gas for simulation.

Table 2.3 SIMION® simulation parameters for the SNeuPI concept.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unitsa</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron mass</td>
<td>0.000548579903</td>
<td>u (atomic mass unit)</td>
</tr>
<tr>
<td>Electron charge</td>
<td>-1</td>
<td>e (elementary charge)</td>
</tr>
<tr>
<td>Electron distribution</td>
<td>circle</td>
<td></td>
</tr>
<tr>
<td>Electron direction (x,y,z)</td>
<td>1,0,0</td>
<td></td>
</tr>
<tr>
<td>Electron KE at gate</td>
<td>150</td>
<td>eV</td>
</tr>
<tr>
<td>Ion mass</td>
<td>16</td>
<td>u (atomic mass unit)</td>
</tr>
</tbody>
</table>

*a* correspond to units used in SIMION®
2.2 Simulation

Figure 2.5 Particle trajectory simulation of the SNeuPI instrument concept. The contour potentials from the left of the MCP up to the emitters are -1024 V to -1 V in factors of 0.5x. So the contour closest to the MCP is -1024 V, the next is at -512 V, etc.

Figure 2.5 shows the simulation results. The two-dimensional figure portrays a stream of energetic electrons emanating from a micro-tip emitter array (left side). The electrons that have sufficient energy to ionize the atmospheric neutrals in the chamber are depicted by the blue and green segments of the trajectory plots. The potential distribution in the chamber effectively deflects these electrons back toward the grounded walls, where they are collected. The ionized neutrals within the chamber (black traces) are attracted to the large negative potential on the micro-channel plate, which is shown on the right side of the figure. The MCP is expected to have a cascade of secondary electrons and produce a significant current on its output.

Thus, using particle trajectory simulation software, it has been shown that the SNeuPI concept can work with the use of field emitters and micro-channel plates. Chapter 3 describes the electronics needed to run these devices.
Chapter 3

Electronic Design

3.1 Electronics requirements

The fundamental requirement for the SNeuPI electronics is to generate the various potentials required by the components inside the accommodation chamber and to sample correctly the current collected. The main components are the Spindt type field emitter and the micro channel plates in an APD2 assembly (see Figure 2.4). The electronics must also be capable of measuring the extremely low current output from the MCP assembly. There must be provisions to measure the potentials and current on the emitter tips such that there can be an estimation of the electron emission. These measurements can also serve as an aliveness check. For commanding and communication with the ground station, there must be components that allow communication with the rest of the CubeSat system. Apart from this, the system must check the various incoming power lines for reliability considerations, and to provide state-of-health information.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>1 W or less</td>
</tr>
<tr>
<td>Operation temperature</td>
<td>20° C to 75° C</td>
</tr>
<tr>
<td>Measurement cycle time</td>
<td>1 second or less</td>
</tr>
<tr>
<td>Current readings per cycle</td>
<td>3</td>
</tr>
<tr>
<td>Measured amplified ionization current</td>
<td>200 pA to 1 µA</td>
</tr>
<tr>
<td>Micro channel plate voltages</td>
<td>0 to -2000 V</td>
</tr>
<tr>
<td>Field emission current</td>
<td>150 µA</td>
</tr>
</tbody>
</table>

It is not required to convert the raw data generated by the SNeuPI instrument to direct density or pressure readings. Software does this conversion as part of the data analysis process. The specific requirements of the electrical system are formed from a knowledge of the composition of the F-region, the specifications of the rest of the CubeSat and a historical understanding of other density measurement techniques. The potentials and current measurement requirements
are based on the analysis performed in section 2.1. A summary of the requirements is tabulated in Table 3.1.

The main purpose of building the instrument is to achieve high-fidelity measurements with low power consumption. When compared to existing sources it was decided to place a requirement of less than one-third the power consumed by a hot filament ionization gauge. This gauge, which is a Bayard-Alpert type, will be used to validate the SNeuPI concept on the CubeSat. The one second or lower timing requirement arises from the specification of the spacecraft control system, which commands the instrument every second and expects a response before the next command is sent. This is done to maintain data flow among the various instruments and due to bandwidth considerations. Space and power constraints lead to a very limited pool of available components that can be used to achieve the desired characteristics.

### 3.2 Electronics overview

![Block diagram of electronics](image)

Figure 3.1 Block diagram of electronics. The FPGA controller is at the heart of operation. The FPGA controls the ADC and DAC which enable the control and measurement sections of the circuit boards.

A block diagram overview of the electronics used for the SNeuPI instrument is shown in Figure 3.1. At the heart of the system is a low power field programmable gate array (FPGA) which controls the operation of the rest of the system. The FPGA is operated in a synchronous manner and receives its clock from a 10 MHz crystal oscillator. The programming connection to the FPGA is a JTAG interface. Most power lines arrive from an external circuit board. They are then further filtered and used on the SNeuPI boards. The various controllable potentials required are generated via a digital to analog converter (DAC), and the science and housekeeping measurements are performed through an analog to digital converter (ADC). The DAC controls the MCP voltage. The field emitters are controlled using a subsystem that aims to stabilize the emission current from the field emitters by adjusting the voltage of the emitter tips. This FPGA
control this subsystem through the DAC. The current output from the MCP is converted to a proportional voltage by a logarithmic amplifier. More detailed descriptions of the design are provided in the remainder of this chapter.

## 3.3 Electronics details

Physically, the circuit is distributed over three boards. The main functions of each of these are detailed as follows:

**Board 1 - The Upper Board**  This is the main control board. The schematic is depicted in Appendix A and comprises:

- FPGA controller
- Digital to analog converter
- Analog to digital converter
- Housekeeping multiplexer
- Power filtering lines
- Battery voltage to 5 V conversion
- High voltage DC converters
- Debug port
- Programming JTAG port
- High voltage safety lanyard connection
- Serial communication system
- Power on reset circuit
- Temperature and voltage monitors

Figure 3.2 portrays a 3D model of the upper board.

![3D model of the upper board](image)

**Board 2 - The Lower Board**  This board forms the intermediate control board for stabilizing the electron emission. The board also contains components to measure related emission

Figure 3.2 3D model of the upper board. This is the main control board and houses the FPGA, ADC, DAC, and communication system.
parameters like the emitter tip-to-gate voltage and the emission current. The schematic is shown in Appendix B. This schematic is a slightly modified version of a schematic obtained from SRI International. Figure 3.3 depicts a 3D model of this board. The physical relationship between the upper and lower boards is shown in Figure 3.4. There is a cut out on the lower board to accommodate the large profile DC-DC converters on the upper board.

![Figure 3.3 3D model of the lower board. Contains a circuit to enable stable electron emission from the emitter array.](image)

![Figure 3.4 3D model of the lower board fitting into the upper board. The available space between two boards on the LAICE CubeSat electronics box necessitates the cut out on the lower board to make space for the two high voltage DC-DC converters.](image)

**Board 3 - The Daughter Board** This board houses the trans-impedance logarithmic amplifier which reads the output from the SMA connector on the MCP. The schematic is displayed in Appendix C and a 3D model is shown in Figure 3.5.
3.3 Electronics details

![3D model of the daughter Board](image)

Figure 3.5 3D model of the daughter Board. This board has current inversion circuit for converting electron current from the MCP to a positive current. It then converts this current to a voltage reading with the use of a logarithmic transimpedance amplifier.

3.3.1 Power system

The power required by the electronics is drawn from the +3.3 V digital, +5 V digital, +5 V analog, -5 V analog, +15 V analog and -15 V lines. These lines are generated externally and fed into the main (upper) board via a 37 pin connector. Other voltages required (such as 2.5 V and 1.25 V references for the converters) are generated on the upper board. Since the power available on the input power lines to the upper board was predefined for a different version of the SNeuPI concept, it was also necessary to generate a separate 5 V line to be used by high voltage DC-DC converters described in subsection 3.3.3. The 7.4 V battery line of the CubeSat is down converted to 5 V using a micro-module switch mode power supply (LTM8020). A high conversion efficiency and a small footprint make the LTM8020 an ideal choice for this system. The LTM8020 can supply up to 200 mA. The expected current drawn from this line is 70 mA which lies right at the peak of its specified performance.

3.3.2 Communication

Communication with the spacecraft computer is designed to occur via an RS-422 link. The serial RS-422 transceiver was chosen over the RS-232 link as its differential and balanced line properties make it better suited for eliminating noise induced from external sources. This allows for higher transmission rates. SNeuPI communicates with the rest of the CubeSat at a rate of 115,200 baud. By choosing to communicate via a UART (universal asynchronous receive and transmit), we effectively make the clock within SNeuPI independent of the other instruments on the CubeSat.
3.3.3 High voltage generation

One of the quirks of choosing an MCP for ion current magnification is the generation of the bias potentials for its plates. The chevron type MCP assembly has two plates and an anode collector. The electrical schematic of the MCP connection is portrayed in Figure 3.6.

![Figure 3.6 Connections of power supplies to the MCP assembly. The front plate (plate 1) of the MCP assembly requires a potential of -2 kV in order to attract ions and the second plate (plate 2) requires a potential of -100 V in order to attract the secondary electrons produced on plate 1.](image)

Two high voltages (-2 KV and -100 V) are generated by using the UMHV converters from HVM Tech. These converters have a specified operation range of $-55^\circ$ to $70^\circ$C which covers our desired operating range. They are low power devices with a small form factor. The output voltages of these DC-DC converters are configurable and are programmed via the digital to analog converter.

3.3.4 Digital to analog conversion

The digital to analog converter (DAC) has 4 outputs with a 0 to 5 V range. The first two outputs control the two HV-DC-DC converters. The last two control the operation of the lower board. The LTC2604 DAC is a 16 bit chip that communicates with the FPGA over an SPI (serial peripheral interface) bus. The outputs of the DAC are cleared on a power on reset. When the chip select goes low, the device reads the serial data on the SDI line at the rising edge of the clock (SCK). The DAC can run on a wide range of clock rates. To prevent any additional clocks and circuits being generated on the FPGA, the 10 MHz input from the oscillator is fed through directly to the DAC via the FPGA.
3.3 Electronics details

3.3.5 Trans-impedance amplifier

The output current of the MCP assembly is converted to a proportional voltage by using the high-speed logarithmic LOG114. The output voltage is a logarithmic ratio of the reference current to the input current. The reference resistance for the LOG114 $R_{REF}$ is chosen to be 79.1 M$\Omega$ such that at the reference voltage ($V_{REF}$) of 2.5 V, the reference current $I_2$ is 31.6 nA. This gives a $V_{LOGOUT}$ range of 0.937 V for $I_{in} = 1 \mu A$ to -0.937 V for $I_{in} = 100 \ pA$. The output of this stage is fed to a non-inverting op-amp with a gain of 2.66 to give an output voltage range of 2.5 V to -2.5 V.

The output of the MCP, however, is a negative current; that is, electrons flow out of the MCP. In the conventional sense this means that the current is flowing into the MCP. However, since the LOG114 works with only positive input currents, it was necessary to add a current inversion stage. As seen in figure 3.7, this is achieved by using a combination of an ultra low-noise matched transistor pair such as the SSM2212 and an OPA703NA op-amp that has a bias current of 1 pA. Laboratory results for this part of the circuit tested separately are shown in figure 3.8.

![Figure 3.7 Negative to positive current inversion schematic. Electron current (negative current) out of the MCP needs to be converted to a positive current for input into the logarithmic trans-impedance amplifier.](image-url)
3.3 Electronics details

Figure 3.8 Laboratory test results for negative to positive current inversion. Based on circuit shown in Figure 3.7. The conversion is linear over the desired operation range.

Figure 3.9 shows a circuit used for SPICE simulation of the daughter board. The voltmeters and ammeters depict results when the input current is $-1\mu A$. 
Figure 3.9 Simulation circuit for end-to-end daughter board test. The current inversion circuit is connected to an equivalent schematic of the LOG114.
A DC-sweep of the current source (I1 in Figure 3.9) results in the plot seen in Figure 3.10. The logarithmic amplifier follows its expected linear characteristic between -2.5 V to 2.5 V for input ranges of 100 pA to 10 µA. Higher or lower current inputs lead to output voltage saturation, which plateaus at the rail potentials.
3.3.6  Emitter control circuit

A block diagram of the emitter control circuit on the lower board is shown in Figure 3.11.

The electron emission from the tips is a function of the voltage difference between the emitter tips and the gate electrode. The emission level is controlled by a charge pump circuit where the output emission is stabilized by providing a stable control voltage to the input of an opto-isolator. The high voltages needed for operation are generated using zener diodes and are isolated from the main board using transformers. The circuit also consists of a high voltage measurement section and an emitter current sensor for feedback to the upper board. The emission output from the tips is expected to follow Fowler-Nordheim characteristics.

3.3.7  Analog to digital conversion

A 16 bit, four channel analog-to-digital converter is used to convert various analog voltages into digital signals for further processing on the FPGA. The ADC inputs are referenced to
a 2.5 V reference and a COM line. The conversion range is then 2.5 V ± (REF-COM).

With the COM line at ground this gives a 0 to 5 V range on the ADC. The accuracy of
the ADC depends on the impedance matching between the signal and COM lines, and
on the clock rate. The ADC clock is set at 1.25 MHz through the FPGA for the highest
conversion accuracy. The connection to the four channels are as follows:

1. The output from the logarithmic amplifier is called "Data_In" on the upper board.
   This signal is amplified and buffered using op-amps before being fed into the ADC on
   channel 1. The signal into the ADC has a transfer function of $V_{CH1} = 2.5 - V_{DATA_IN}$.
   Since the ADC is rated to convert from 0 to 5 V with a maximum rating of 6 V, it
   is necessary to limit the input voltage to below 6 V. This is done using Schottky
   diodes to limit the voltage signal at -0.320 V and 5.480 V. Without diode protection,
   voltages greater than 5 V on the line occur when the input signal to the logarithmic
   amplifier is lower than 100 pA, and voltages less than 0 V occur when the input
current is greater than 10 µA.

2. The second channel is connected to the lower board in order to measure the voltage
   between the emitter tips and gate. The voltage range on this input line is 0 to 4 V.
   The transfer function of this channel is $V_{CH2} = -\frac{3}{150} V_{emitter-gate}$.

3. The third channel is also connected to the lower board in order to read the emission
   current as measured on the lower board. The transfer function for this is $I_{emission} =
   V_{CH3} \times 37.5 \mu A/V$.

4. The fourth channel is connected to the housekeeping/management line from a
   multiplexer in order to obtain state of health information from the power lines,
temperature sensors and control voltages on the DC-DC converters.

**Housekeeping**

The housekeeping line on the ADC is the output of a 16:1 multiplexer that runs from a
±15 V supply. The inputs to the multiplexer are limited to 0 to 5 V as the ADC has a 0 to
5 V limit. The first ten channels of the multiplexer are connected to power supply lines,
temperature sensors, and DAC outputs. The FPGA controls the channel selection.
3.3.8 MCP and emitter configuration in accommodation chamber

Figure 3.12 shows a CAD model of the accommodation chamber that will be mounted in the CubeSat. The configuration of the emitters and MCP-APD2 assembly is seen. The APD2 has fairly long connection leads which will be trimmed prior to assembly. The longer of the two leads (prior to trimming) connects to the UMHV0530N for the -2 kV signal.

Figure 3.12 CAD model of accommodation chamber with components mounted. The emitter on the right is surrounded by PCTFE (polychlorotrifluoroethylene) for insulation. The APD2 MCP assembly is mounted on the left, next to the high voltage feedthrough connector.

Summary This chapter described the electronics that are necessary to adequately provide the required potentials for the emitters and APD2-MCP assembly. A brief overview of housekeeping and current measurement was also provided. Chapter 4 describes the digital design of the FPGA that is used to control the rest of the electronics.
Chapter 4

Digital Design

An FPGA is a configurable integrated circuit that can be configured using a hardware description language (HDL). Such an FPGA is present on the upper board and serves as the overall controller for the SNeuPI instrument, including serial communications, analog to digital conversions, and digital to analog conversion. The VHSIC Hardware Description Language (VHDL) has been used to design the digital logic for the control operation. This digital design controls the operation of the various components that are part of the analog and schematic design. The FPGA design is synchronous in nature. That is, the design is clock based. Most internal signals and flip flop conditions change at the rising clock edge. The timing of the various transitions in the design are derived from a knowledge of the functionality of individual components such as the ADC, DAC, multiplexer, etc. The FPGA works by receiving commands from an external computer or ground station and interpreting them to control voltages on the MCP and the emitters. It also measures the current out of the MCP and the voltage present on the emitter tip. The measurement intervals are derived from an expectation of the rate of density change in the F-region. Apart from these signals the FPGA also monitors housekeeping and management lines for the various potentials and temperature sensors in order to provide vital health information. The flow diagram of the FPGA operation from power on reset is seen in Figure 4.1.

Initialization The start of the FPGA operation after power on begins with the asynchronous reset of the system. This ensures that all the internal signals in the digital design are initialized in known states. The reset occurs at power-on by the use of a low pass filter (LPF) along with a Schmitt trigger. The time difference between power on of the board and output of the Schmitt trigger is 100 ms. This is the also the time constant of the LPF. Owing to its hysteresis, the Schmitt trigger enables a glitch free reset signal to be provided to the FPGA.

Communication After power on and asynchronous reset the FPGA waits for commands over the serial line (universal asynchronous receiver/transmitter (UART) interface) for further operation. The UART transceiver features galvanic isolation and allows bidirectional data transfer between the FPGA and external devices. The byte to be transmitted is sent to a 128 bit FIFO on the FPGA. This FIFO is derived from one of the eight 4,608-bit blocks on the
Figure 4.1 Flowchart depicting the process flow of the digital logic in the FPGA. When a command byte is received for the first time after power on, the process can flow in one of two directions. After power on the HV converters are always off. When the HV start bit of the mode command is 0, the HV converters stay off and only the housekeeping data are converted and sent out. When the HV start bit is set for the first time, DAC channel 1 output ramps up over a period of 14 minutes. This ramps up the output of the HV converter to -2 kV. When channel 1 conversion is finished, the other DAC outputs get enabled consecutively. Since command bytes are sent every second to SNuPI, the I-V data out of the ADC are only valid when the HV status bit in downlink data is set. This bit is set after HV ramp to indicate the readiness of the device.
Similarly, a 128 bit FIFO on a second block is used for the receive operation. A counter tracks the number of bytes that are present in the FIFO at any given time. The use of a 10 MHz oscillator for the FPGA along with 8-bit data words allows for the use of 115,200 baud rate over the RS-422 interface. Since the FPGA generates 280 bits of data in a one-second measurement cycle, the selected rate provides ample communication speed. The number of bits is small owing to the slow expected variation of the neutral density in the lower atmosphere. This slow change leads to a requirement of fewer data points in a second, or a spatial sampling interval of ∼ 8 km for an orbital spacecraft.

**Uplink commands and sequence of operations** The uplink communication with SNeuPI always starts with an 8-bit start word and an 8-bit mode command. An understanding of the uplink communication commands in Table 4.1 and the modes of operation of SNeuPI requires an understanding of the MCP and field emitters.

Table 4.1 Communication uplink commands.

<table>
<thead>
<tr>
<th>Byte number</th>
<th>Action</th>
<th>Binary value&lt;sup&gt;a&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Start byte: signifies a communication start byte at 1 second intervals</td>
<td>00110101</td>
</tr>
<tr>
<td>2</td>
<td>HV start, sweep emission: start HV ramp to MCP and sweep between 112 µA, 131 µA and 150 µA emission levels after MCP is ready</td>
<td>xxxxx100&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>HV start, standby emission mode: start HV ramp to MCP; keep emitters off</td>
<td>xxxxx101&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>HV start, emission level A: start HV ramp to MCP; initial emission equals 112 µA after MCP is ready</td>
<td>xxxxx110&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>HV start, emission level C: start HV ramp to MCP; initial emission equals 150 µA after MCP is ready</td>
<td>xxxxx111&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>Sweep Emission: Sent after MCP is ready - sweep between 112 µA, 131 µA and 150 µA emission</td>
<td>xxxxx000&lt;sup&gt;c&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>Standby emission mode: Sent after MCP is ready; used to deactivate emitters</td>
<td>xxxxx001&lt;sup&gt;c&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>Emission level A: Sent after MCP is ready; used to change emission level to 112 µA</td>
<td>xxxxx010&lt;sup&gt;c&lt;/sup&gt;</td>
</tr>
<tr>
<td>2</td>
<td>Emission level C: Sent after MCP is ready; used to change emission level to 150 µA</td>
<td>xxxxx011&lt;sup&gt;c&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

<sup>a</sup>x indicates don’t care bits

<sup>b</sup>this byte sent to SNeuPI only once after power on

<sup>c</sup>can be sent to SNeuPI anytime after MCP is ready

**MCP and emitter control requirements for digital design** The MCP is a high voltage device that requires a gradual turn-on. Its voltage ramp occurs in -50 V to -200 V steps over a few minutes. After the plates on the MCP have the required potentials, the signal from the
APD2-MCP assembly output becomes relevant. To save time and power, it is necessary to perform this voltage ramp only once after powering on the boards, and then perform multiple measurements for a fixed electron emission level from the emitters. However, before the FPGA issues a command to start the high voltage DC-DC conversion, it is necessary to monitor the housekeeping lines at least once to ensure the health of the device.

**Uplink commands** The second byte of the uplink command is designed to meet these requirements. One bit controls the start of high voltage generation through the DAC and the HV DC-DC converters. When this bit (called HV-start) is zero, the FPGA only controls analog to digital conversions. The status of the high voltage is a part of the echo byte in the downlink data stream. The second part consists of two bits that control the emission level. The two bits allow for four electron emission modes as seen in Table 4.1. For example, consider that the system has been powered on, and a start byte is received for the first time. Next the command byte 00000001 is received. Since the HV-start bit is zero, the voltage ramp up to the MCP is inactive. There will also be no electron emission. However, the ADC conversions are active, and housekeeping data is going to be sent on the downlink. The downlink data indicates that the MCP is inactive, and only housekeeping data is valid. Next consider that a command byte 00000110 is sent. In this case, the HV-Start bit (bit 3 from LSB) is set and the voltage step-up will begin. Subsequent HV-Start commands are ignored in order to prevent a restart of the voltage ramp. After the voltage has been stepped up to the maximum level, and the MCP is ready, the electron emission will be held at a fixed level. A downlink bit (HV-Status) changes to indicate that the system is ready. Any of the subsequent uplink commands in Table 4.1 will not alter the state of the MCP, but can change the emission level. One of the emission modes has been defined as a standby mode. There can be a scenario where we need to turn the emission off, but we do not want to go through the MCP ramp-up cycle. This mode can be used in such a scenario. Also, one of the emission modes is defined as a sweep mode, where the emission level is going to change thrice in a one second period.

**Control of the DAC** The DAC converter has four channels. As seen in Figure 4.1, the first channel controls the -2000 V ramp on the front plate of the MCP over a 14 minute period. One second after the high voltage on the first plate is ready, the second channel causes the second plate to have a potential of -100 V. Once the MCP is ready, channels 3 and 4 enable and control the electron emission from the emitters by controlling the operation of the lower board. The voltage on the emission control pin on DAC 4 depends on the uplink command and is valid only after the other DACs have enabled the MCP and the emitter control circuit on the lower board. The 16 bit DAC operates over a simple 3-wire serial interface. The inputs to the DAC are the chip select, serial clock, serial data in and asynchronous clear lines. The DAC clock is the same as the FPGA clock, i.e, 10 MHz. The reference low pin of the DAC is connected to ground and
the conversion reference pins are connected to 5 V. This causes the ideal output of the DAC to be

\[ V_{\text{out}} = \frac{k}{2^{16}} \times 5 \]

where \( k \) is the 16 bit serial word from the FPGA. When the chip select pin is pulled low, the next 24 clock cycles shift a 24-bit word from the FPGA into the DAC. The first 8 bits define the command and address, and the next 16 bits signify the expected output of the DAC.

**Safety lanyard**  Owing to the presence of high voltages on the MCP and emitters, it is necessary to have a safety lanyard in the system. The status of the safety lanyard is read by the FPGA and determines the operation of the DAC. The safety lanyard works by externally shorting four connector pins, two for the MCP voltages and two for the emitter voltages. When the pins are short-circuited there will be no high voltage conversion, and when the short is removed the voltage conversion can occur based on the uplink command word. There are two possible scenarios when the safety lanyard may be taken off. The first one is when the device is powered off. In this case the pins will be disconnected even before power is applied, so the high voltage generation can occur as soon as the power is applied and the uplink command is sent. In the second case the power supply to the system may be on before the safety is removed. This is an accidental case. Here, the voltage ramp doesn’t occur even if HV-Start byte has been previously received. The HV ramp will only occur after a new start and command bytes have been received. The recommended manner is to remove the safety lanyard before supplying power to SNeuPI.
Downlink sequence of operations  The system timing diagram from the point of analog to
digital conversion is shown in Figure 4.2. Current data from the MCP and the voltage data
for the emitter tips are transmitted three times in a one second period. The diagram shows the
sequence of operations from receiving a start byte to the output of the end byte.

![Figure 4.2 Timing diagram of the FPGA with emphasis on communication
and analog to digital conversion. When the start and mode commands
are received, they are immediately transmitted back. This is followed by
housekeeping data and current and voltage data. The current data from the
output of the MCP is averaged over 1024 conversions and then transmitted.
An end byte indicates the end of a transmission. The ADC is in an idle state
until the next set of commands are received and the process repeats.]

Table 4.2 lists the details of downlink data bytes along with conversion factors for data
interpretation. The start byte and the next eight status bits are immediately sent on the downlink
channel after an uplink command. This is a precaution that echoes the command so that there
is no ambiguity in the flight data interpretation. This echo byte is followed by housekeeping
(management) data, the current equivalent voltage reading from the logarithmic trans-impedance
amplifier, and the voltage between emitter tips and gate (also analog ground). The end word
signals the last byte that is transmitted in response to an uplink command.

Control of the ADC  The four channel ADC uses three of its channels to convert housekeeping,
current and tips voltage data. The 16-bit, 4-channel serial ADC has four control lines that are
controlled by the FPGA. These are the chip select, shutdown, clock and data lines. The ADC
needs 24 clock cycles to complete one conversion. The first eight clock cycles correspond to the
8-bit serial word that is transmitted to the ADC from the FPGA. These 8 bits control the channel
selection and power state of the ADC. After the first eight clock cycles, the busy line goes high
for one clock cycle. The output of the ADC appears on the digital out line over the next sixteen
<table>
<thead>
<tr>
<th>Byte #</th>
<th>Bit sequence</th>
<th>Meaning</th>
<th>Expected value</th>
<th>Data conversion factors (based on circuit components)</th>
<th>Expected Reading</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td>Start</td>
<td>1010011</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>blank/nothing</td>
<td>00000</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>HV status</td>
<td>0/1</td>
<td>discard I-V data if 0</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Emission mode</td>
<td>00/01/10/11</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>3+4</td>
<td>16</td>
<td>3.3 V monitor</td>
<td>data</td>
<td>$data \times (5/65535)/(100/124)$</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>5+6</td>
<td>16</td>
<td>5 V Digital</td>
<td>data</td>
<td>$data \times (5/65535)/(100/124)$</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>7+8</td>
<td>16</td>
<td>5 V Analog</td>
<td>data</td>
<td>$data \times (5/65535)/(100/124)$</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>9+10</td>
<td>16</td>
<td>15 V Analog</td>
<td>data</td>
<td>$data \times (5/65535)/(10/34)$</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>11+12</td>
<td>16</td>
<td>Plate 1</td>
<td>data</td>
<td>$data \times (5/65535)$</td>
<td>0 to 4</td>
<td>V</td>
</tr>
<tr>
<td>13+14</td>
<td>16</td>
<td>Plate 2</td>
<td>data</td>
<td>$data \times (5/65535)$</td>
<td>0 to 1</td>
<td>V</td>
</tr>
<tr>
<td>15+16</td>
<td>16</td>
<td>Main board temp</td>
<td>data</td>
<td>$data \times (5/65535)/(0.004 - 273)$</td>
<td>25</td>
<td>°C</td>
</tr>
<tr>
<td>17+18</td>
<td>16</td>
<td>Daughter temp</td>
<td>data</td>
<td>$data \times (5/65535)/(0.004 - 273)$</td>
<td>25</td>
<td>°C</td>
</tr>
<tr>
<td>19+20</td>
<td>16</td>
<td>5 V converter</td>
<td>data</td>
<td>$data \times (5/65535)/(100/124)$</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>21+22</td>
<td>16</td>
<td>Extra/ignore</td>
<td>data</td>
<td>$data \times (5/65535)$</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>23+24</td>
<td>16</td>
<td>MCP current sample # 1$^a$</td>
<td>data</td>
<td>$10^4 \times 2.5/(79.1 \times 10^6)^b$</td>
<td>100 p to 10 u</td>
<td>A</td>
</tr>
<tr>
<td>25+26</td>
<td>16</td>
<td>Tip V # 1</td>
<td>data</td>
<td>$data \times (5/65535) \times (-150/3)$</td>
<td>0-4</td>
<td>V</td>
</tr>
<tr>
<td>26+27</td>
<td>16</td>
<td>MCP current sample # 2</td>
<td>data</td>
<td>$10^4 \times 2.5/(79.1 \times 10^6)$</td>
<td>100 p to 10 u</td>
<td>A</td>
</tr>
<tr>
<td>28+29</td>
<td>16</td>
<td>Tip V # 2</td>
<td>data</td>
<td>$data \times (5/65535) \times (-150/3)$</td>
<td>0-4</td>
<td>V</td>
</tr>
<tr>
<td>30+31</td>
<td>16</td>
<td>MCP current sample # 3</td>
<td>data</td>
<td>$10^4 \times 2.5/(79.1 \times 10^6)$</td>
<td>100 p to 10 u</td>
<td>A</td>
</tr>
<tr>
<td>32+33</td>
<td>16</td>
<td>Tip V # 3</td>
<td>data</td>
<td>$data \times (5/65535) \times (-150/3)$</td>
<td>0-4</td>
<td>V</td>
</tr>
<tr>
<td>34</td>
<td>8</td>
<td>End Word</td>
<td>1000111</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

$^a$MCP current sample is an average of 1024 samples

$^b$x = (2.5 − data × (5/65535)) × (16/(16 + 26.7))/0.375
clock cycles, the first of which corresponds to the most significant bit. These 16 bits are read in by the FPGA. For the housekeeping data on channel 4 and emitter voltage on channel 2, these 16 bits are buffered and directly sent out to the serial port FIFO for transmission. However, the current data coming into channel 1 is accumulated and averaged in the FPGA before it is sent to the transmit FIFO. The accumulation and average is done over 1024 samples of the current for higher accuracy. There is a 200 ms wait time between successive current readings in order to cover the one second communication interval, and also to give the MCP and field emitters sufficient time for a new operation.

**Control of the multiplexer** The housekeeping signals from various potentials on the board are routed through to the ADC via a 16:1 multiplexer running from the ±15 V supply lines. The multiplexer is switched in order of the downlink housekeeping words displayed in Table 4.2. The multiplexer has a four signal parallel addressing scheme. These four signals enable the relevant input of the multiplexer and feed the output to channel 4 of the ADC via a buffer op-amp. These four address signals are generated in the FPGA. The FPGA digital logic is written such that inputs 0 to 9 on the MUX appear in sequence at its output. To account for the 20 µs settling time of the buffer and internal switch transition time of the multiplexer, the FPGA waits for 34 µs to command the ADC for a conversion after switching the multiplexer channel.

**FPGA statistics** Table 4.3 summaries some of the main digital design characteristics on the FPGA. The core cell usage is at 32.71%. The core cells consists of system gates formed using 3-input look up tables, latches and D-flip-flops. The IO cells correspond the the IO lines being used. The IO lines are either input or output but not configured as bi-directional. The maximum time delay for state transition is well below the clock frequency and the total power consumption is 4.565 mW.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core cells used</td>
<td>2010 of 6144 (32.71%)</td>
</tr>
<tr>
<td>IO cells used</td>
<td>23 of 68 (33.82%)</td>
</tr>
<tr>
<td>IO Technology</td>
<td>LVCMOS33 (3.30 V)</td>
</tr>
<tr>
<td>Block RAMs used</td>
<td>2 of 8 (25%)</td>
</tr>
<tr>
<td>Timing delay - input to output(min)</td>
<td>2.825 ns</td>
</tr>
<tr>
<td>Timing delay - input to output(max)</td>
<td>10.474 ns</td>
</tr>
<tr>
<td>Timing violations</td>
<td>none</td>
</tr>
<tr>
<td>Power consumption (static)</td>
<td>0.099 mW</td>
</tr>
<tr>
<td>Power consumption (dynamic)</td>
<td>4.466 mW</td>
</tr>
</tbody>
</table>

**Summary** The synchronous digital design of the FPGA controls the timing and function of various components that are a part of the analog and schematic design. The digital design
interprets the uplink commands, controls the ADC and DAC timing, generates slow turn-on ramp for the MCP, averages current data, and sends housekeeping and I-V data out for downlink by the flight computer. That is, the digital design enables the three circuit boards to be validated with the vacuum chamber setup, as described in Chapter 5.
Chapter 5

Laboratory Setup

This chapter describes the sequence of events undertaken to set up a satisfactory test box as a proxy for the LAICE accommodation chamber. The Spindt type emitters require thorough outgassing before operation in vacuum. Ideally this requires temperatures in excess of 450° C. However, such temperatures cannot be achieved in the available vacuum chamber due to the presence of materials with much lower melting points. Halogen bulbs, flexible kapton heater tapes and filament wires were used at various stages of testing to heat the emitters. Halogen bulbs and filament wires have been found reliable for our application. There have also been various combinations used for housing the emitters. Aluminum on a Kel-F (PCTFE) mount was first used to hold the emitters, but this was changed to a ceramic housing as it was found that Kel-F melts at 150° C at low pressures. Figure 5.1 shows the first version of the test box, which is a proxy for the SNeuPI accommodation chamber on the CubeSat. This box is made out of sheet aluminum and mounted on the stands of a vacuum chamber.

Figure 5.1 First iteration test box mounted on the stands of a vacuum chamber.
At this stage the DC converters were controlled externally through bench top sources and were placed inside the vacuum chamber. A high voltage feed through was later installed on the vacuum chamber to enable the use of DC converters mounted on the SNeuPI upper board. Figure 5.2 shows the second iteration of the test box. The APD2 MCP is on the left. The longer lead connects to the -3 kV DC-DC converter. The emitter array is mounted on the right along with a thermistor and heater tape.

![Second iteration test box](image)

**Figure 5.2** Second iteration test box. The MCP is on the left side and emitter array on the right.

The output of the thermistor is connected to an analog to digital converter. The ADC is connected to a Raspberry Pi computer over SPI and controlled via a Python program. This provides effective monitoring of the temperature inside the test box. The block diagram of the measurement setup is shown in Figure 5.3.

![Block diagram](image)

**Figure 5.3** Setup for temperature sensing on the test box. Voltage across the thermistor is a function of its resistance. This voltage is measured and converted to a temperature reading.

The temperature calculation is based on the resistance of the thermistor and is derived from the empirical Steinhart-Hart equation:

\[
\frac{1}{T} = A + B \ln(R) + C [\ln(R)]^3
\]

(5.1)
where $A, B$ and $C$ are Steinhart–Hart coefficients, $T$ is the Kelvin temperature and $R$ is the resistance at $T$ express in ohms. From Honeywell’s resistance-temperature conversion table [10] and a simultaneous solution of equation 5.1 it is found that $A = 0.00112463$, $B = 0.00023492$ and $C = 8.32029 \times 10^{-8}$. This enables conversion of the resistance reading of the thermistor into temperature readings.

Figures 5.4 and 5.5 display the final version of the test box with ceramic used to hold the emitters and the lamp in place of the heater tape.

Figure 5.4 Emitter held in place with a ceramic tube. The tube has slots on the sides to allow for radiant heating. The slots also provide a place for a tab on the TO-5 emitter header. This ensures that the emitter does not slide back out of the box.

Figure 5.5 Halogen lamp used to heat the emitter array. The lamp is mounted next to the ceramic tube that holds the emitter array.

As part of pre-circuit board component level testing, various Keithley™ electrometers, voltage sources and current sources were used. These were connected to a desktop computer using GPIB and RS-232 interfaces. These devices were monitored and controlled using MATLAB software on the computer. An example of MATLAB control of these devices is shown in Appendix E. The final test set-up shown in Figures 5.4 and 5.5 was found to be adequate for
validating the measurement concept and electronics. The test results of electronics and science related data are presented in Chapter 6.
Chapter 6

Validation

The SNeuPI instrument comprises three boards - the upper board, lower board, and daughter board. The upper board houses the FPGA, converters and communication systems. The lower board controls the electron emission level from the emitter array. The daughter board serves as the electrometer that converts the MCP output current to a proportional voltage that is digitized by the ADC on the upper board. This chapter presents validation results of electronics, emitters and the MCP-APD2 assembly. Both bench top and vacuum tests are described.

6.1 Upper board test results

The top and bottom views of the upper board which houses the FPGA are seen in Figures 6.1 and 6.2. The high voltage pin of the UMHV0530N DC-DC converter is isolated from the rest of the board to provide insulation from the rest of the components. This pin and the gap around it can be seen in the top right corner in Figure 6.1.
Figure 6.2 displays the bottom side of the upper board where the large profile DC-DC converters are mounted.

![Figure 6.2 Bottom view of the upper board.](image)

### 6.1.1 Digital to analog conversion

Figure 6.3 shows the connections of the digital to analog converter (DAC) to the high voltage DC-DC converters and to the lower board. Connections between the HV DC-DC converters and the MCP assembly are also shown.

![Figure 6.3 Block diagram of DAC connections and high voltage generation on the upper board. The dotted box contains the elements that are location on the upper board.](image)
As seen in Figure 6.3, channel 1 (Ch 1) output of the DAC is connected to the programming pin of UMHV0530N for 0 to -2 kV generation. It is a requirement of the MCP to have at least a gap of 1 minute between voltage steps during initial turn on and ramp-up of the plate potentials. Figure 6.4 depicts a short (11.5 s) example of the control of this ramp in 1-second steps for the purpose of testing the output channel 1 of the DAC. After this test, the number of steps was changed to 14 and the step length changed to 60 seconds so that the total time to step up the HV supply to -2 kV is 14 minutes.

![Image of oscilloscope trace]

Figure 6.4 A short (11.5 s) example of the output voltage from Ch 1 (see Figure 6.3) on DAC. This voltage is used to control the high voltage DC-DC converter. $\Delta T/division = 2.5 \text{ s}$, $\Delta V/division = 1 \text{ V}$ on the oscilloscope.

Similarly, DAC output channels 2 to 4 were tested. Further results from channel 1 and 2 testing are presented in the next section on high voltage conversion. Section 6.2 displays validation results on the lower board, which is controlled by DAC channels 3 and 4.
6.1 Upper board test results

6.1.2 High voltage DC-DC conversion

-100 V conversion from the UMHV0505

The second plate of the MCP-APD2 assembly requires a potential of -100 V. This voltage is generated using the UMHV0505 DC-DC converter. The output of this converter is seen in Figure 6.5. The programming pin of this controller is connected to channel 2 of the DAC. Initially a 47 kΩ resistor along with a 0.1 µF capacitor formed a low pass filter on this line. This resistor was later changed to a 0 Ω resistor as it was found that the input impedance of the UMHV0505 is fairly low (<14 kΩ).

In order to obtain a -100 V output of the UMHV0505 (point B in Figure 6.3), output channel 2 of the DAC is set at 0.73 V. At this control voltage, the UMHV0505 has a gain of 137.

-2 kV conversion from the UMHV0505

The UMHV0530N is a proportional converter that converts a control input (channel 1 of DAC) into a negative high voltage output on the scale of 0 to -3000 kV (point C in Figure 6.3). The front plate of the MCP-APD2 assembly (also called plate 1) connects to the output of this converter. An example of the UMHV0530N output is seen in Figure 6.6.

Figure 6.5 Voltage output from UMHV0505 at point B in Figure 6.3, controlled by DAC channel 2. ΔT/division = 50 µs, ΔV/division = 100 V on the oscilloscope
6.1 Upper board test results

Figure 6.6 A short example (14 s) of the output of the high voltage DC-DC converter. This output is applied to front plate of MCP.

The measurements are taken on an oscilloscope using a 2.5 kV peak, 40 MΩ / 1.5 pF probe. The first step is a drop of 500 V followed by several 200 V steps and 100 V steps. As the potentials increase, in accordance with MCP specifications, the step size drops to 50 V until the voltage reaches -1950 V. While the step time is set at 1 s for the purpose of testing, the final time delay between steps has been set at 1 min in the FPGA in accordance with the MCP specifications.

Since it is impractical to feed the high voltage output of the HV DC-DC converters back into the DAC for safety and isolation, two of the downlink communication parameters are the output voltages of DAC channels 1 and 2. To convert this downlink data value to a potential reading for the MCP, it is important to know the gain of the HV DC-DC converters. The conversion gain for the UMHV0530N is plotted in Figure 6.7. The device has an average gain of 565.
Figure 6.7 Gain of the HV DC-DC converter (UMHV0530N) when a control voltage is applied to its program pin using the DAC. The average gain is 565. This average gain value can be used to convert the programming voltage, which is a part of housekeeping data, into a reading corresponding to potential on plate 1.

Figure 6.8 shows the timing relationship between the two HV DC-DC converters. The high voltage from the UMHV0530N is applied to plate 1 of the MCP, and then the UMHV0505 puts out a -100 V potential on plate 2.

Figure 6.8 Timing relationship between the two HV converters. The -100 V output from the UMHV0505 is enabled by the FPGA after the voltage steps up from the UMHV0530N to -1950 V.
6.1 Upper board test results

6.1.3 Analog to digital conversion

Figure 6.9 depicts the flow chain of the ADC operation. The current out of the MCP is converted to a scale of -2.5 V to 2.5 V on the daughter board, which houses the electrometer. This is converted to a 0 to 5 V scale on the upper board before it is fed into channel 1 of the ADC. Shottky diodes protect the inputs of the ADC by keeping voltages within specified levels.

![Figure 6.9 Block diagram of the ADC flow chain.](image)

To test the ADC section of the upper board, a -2.5 V to 2.5 V supply voltage was applied to point B in Figure 6.9. The scaling and amplification of this signal is seen in Figure 6.10.

![Figure 6.10 Amplification and level shift of signal from the daughter board before conversion by ADC. Blue curve depicts output from the daughter board (point B in Figure 6.9). Purple curve depicts the input to the ADC on channel 1 (point D in Figure 6.9). \(V_D = 2.5 \text{ V} - V_B\). On the oscilloscope - \(\Delta T/\text{division} = 5 \text{ s}, \Delta V/\text{division} = 2 \text{ V}\).](image)

Data from the ADC, when the conversion is based on its channel 1 input, corresponds to the current out of the MCP. During testing, 1024 samples of this 16-bit data are averaged on the FPGA and read out through the serial port to an external computer and mathematically back-converted to a current reading. The back-conversion is based on the conversion factor for MCP current samples as shown in Table 4.2. Figure 6.11 represents this conversion from the...
input to the ADC channel (point D in Figure 6.9) to the calculated current reading based on the data output of the ADC. This plot also validates the linear conversion of the ADC on a full scale input.

Figure 6.11 Calculated MCP current reading based on ADC output data. ADC data (from point E in Figure 6.9) is used to mathematically back-calculate the MCP output current (point A in Figure 6.9). The conversion factor used for this ADC output data to MCP current calculation is listed in Table 4.2. Horizontal axis corresponds to input channel 1 of the ADC (point D in Figure 6.9). Vertical axis corresponds to the calculated MCP output current.
The voltage clamping action of the Schottky protection diode on the ADC input line is seen in Figure 6.12. When the input signal (point C in Figure 6.9) falls below -0.32 V the output voltage at point D in the figure is clamped to -0.32 V. On the higher end it is clamped to 5.48 V. The clamping action was tested with a sinusoidal input. The Shottky diodes ensure that the ADC is safe from out of scale voltages that may be generated on the daughter board, and from fluctuations on other input lines to the ADC.

Figure 6.12 Clamping action of Schottky diodes. The yellow curve corresponds to the signal at point C in Figure 6.9 before it reaches the Shottky diode. The blue horizontal bars correspond to cursors on the oscilloscope that are used to measure voltage levels. The lower bar is at ground and the upper bar is at the high clamping potential of the diode. The signal after the diode is also in blue and follows the input signal when its within the -0.32 to 5.48 V range.
6.2 Lower board test results

The lower board as seen in Figure 6.13 is used to control the electron emission level from the emitter array. A 21 pin nano connector is used to connect to the upper board. The nine pin connector is used to connect to the emitter array and the -100 V line on the MCP-APD2 assembly.

![Figure 6.13 Picture of the 2.9"x 3.4" lower board with a slot cut out for converters on the upper board.](image)

Figure 6.13 shows some of the connections to the lower board. A detailed block diagram of the lower board can be seen in Figure 3.11.

![Figure 6.14 Block diagram depicting connections between the DAC and lower board. The lower board controls the voltage levels on the ‘tips’ line to control emission from the emitter array. The gate is at ground.](image)

Figure 6.14 shows some of the connections to the lower board. A detailed block diagram of the lower board can be seen in Figure 3.11.

To test the performance of the lower board on a bench-top, a 470 kΩ resistor was substituted in place of the emitter array (between tips and gate connector cables). Emitters can’t be used on the bench-top for testing since they require pressures under $10^{-5}$ Torr. Since there are three emission levels (112, 131, 150 µA) set by the FPGA, the following plots depict the various characteristics at control voltages (3, 3.5, 4 V) corresponding to these three emission levels. The control voltage for the three emission levels is generated on output 4 of the DAC. The power supply to the board is controlled by an enable line which is generated on channel 3 of the DAC. Linear curve fits were performed to characterize the behavior of the lower board.
6.2 Lower board test results

Figure 6.15 depicts the voltage across the load resistor when the DAC applies a control voltage to the lower board. The voltage across the load is measured using a bench-top Keithley voltmeter as this voltmeter has a high input impedance of approximately 180 MΩ. A regular multimeter cannot be used owing to its low impedance value.

![Graph showing relationship between voltage and current](image)

Figure 6.15 Voltage across a load resistor (between tips and gate connectors) when a control voltage is applied to the lower board. This control voltage is called out as the emitter current control on the lower board. The three points correspond to the voltage on channel 4 of the DAC on the upper board, and correspond to emission currents of 112, 131, 150 µA. The voltage across the resistor (which is connected between tips and gate connectors) is measured using a Keithley voltmeter.

The lower board has circuitry that converts the emission current drawn from the lower board to a proportional voltage on a 0 to 4 V scale. Figure 6.16 depicts this proportional voltage when a control voltage is applied by the DAC. A 1 V reading corresponds to a current draw of 37.5 µA by the emitter tips from the lower board. Thus, a 4 V reading will correspond to a 150 µA emission.
6.2 Lower board test results

Figure 6.16 Voltage proportional to emission current. The control voltage on the horizontal axis corresponds to channel 4 of the DAC. This voltage controls the emission level. The vertical axis shows a voltage that is proportional to the current drawn across the tips and the gate. The three points shown correspond to the control voltages that produce emissions of 112, 131, 150 μA respectively.

Figure 6.17 depicts measurement of tips to gate voltage on the lower board using a negative feedback op-amp. The op-amp is used in this configuration to inverter and lower the high voltages to a 0 to 4 V scale, such that the ADC can read them.

Figure 6.17 Measurement of tips to gate voltage on lower board when a control voltage is applied to the lower board using channel 4 of the DAC. The measurement is a fraction of the actual tips to gate value as it is generated using a negative feedback op-amp with the op-amp input connected to the emitter tips. The three points correspond to the same emission control levels as seen in Figures 6.15 and 6.16.
6.3 Validation of MCP-Emitter performance

The following section shows the results of testing the MCP output current vs emitter current in two cases:

1. With minimal preconditioning of emitter array.
2. With heating the emitter array to 180 °C.

The current measurements were made on the bench-top using Keithley electrometers. The manufacturer of the emitter array recommends hard bake out prior to using emitters in order to stabilize their performance. Section 6.3.1 shows the erratic nature of the emitters when they haven’t been sufficiently heated. Section 6.3.2 then displays results after bake-out at 180 °C. MCP output current vs. density variations are shown along with stable emission currents.

6.3.1 Characteristics with emitters heated to 80° C

Emission and MCP characteristics are presented here for the case when the emitter arrays have not been sufficiently baked. The erratic behavior of the plots in this section is attributed to gas adsorption and the presence of impurities on the emitter tips.

**Characteristics at higher pressure (≈ 10^{-5} Torr)**

Figure 6.18 displays the emission current measured on the test box, which serves as a proxy for the accommodation chamber.

![Electron emission as measured on walls of test box](image)

Figure 6.18 Emission current measured on the walls of the test box that serves as a proxy for the accommodation chamber. It is seen that the emission levels are erratic, which is attributed to insufficient bake-out of the emitter array. The step discontinuity in the case of a 3 V control is also due to erratic behavior of the tips.
Since electron emission is measured, according to standard conventions the sign of the current is negative. The lower values on the graph thus indicate a higher emission from the emitter tips. The control voltages shown in the following plots correspond to voltages on channel 4 of the DAC (see Figure 6.3). This channel is connected to the lower board which controls the emission level. A current limiting resistor (R37) on the lower board was set to 198 Ω at the time of this test. This resistance value limits the emission level to a maximum level of -120 µA.

Figure 6.19 displays the corresponding current readout of the MCP. When an ion hits the front plate of the MCP, it causes a cascade of electrons which show up at the output. Thus the sign of the current out of the MCP is negative. Figures 6.18 and 6.19 show that the ionization/gain curve is proportional to the electron emission curve. This is clearly seen in the case of the 3 V control input where the emission level abruptly decreased from -40 µA to -100 µA, causing a change in the MCP output from approximately -1 nA to -3.5 nA.

Figure 6.19 Output current from the MCP. Output current from the MCP corresponds to the ions created by collision of neutral gas with energetic electrons from the emitters. There are three curves, each corresponding to a different emission level (see Figure 6.18), as set by the FPGA program. On comparing with Figure 6.18 it is seen that the MCP current follows the emission current, despite the erratic emission vs time.
Figure 6.20 shows the average emission current plotted against average output current of MCP. This shows a linear relation between emission current and ionization current at a constant pressure of $10^{-5}$ Torr.

**Characteristics at lower pressure ($\approx 4 \times 10^{-7}$ Torr)**

Figures 6.21 - 6.23 show the same behavior as seen in Figures 6.18 - 6.20, but at a much lower background pressure. As expected, the MCP output level lowers as the pressure is decreased. The erratic behavior of the emission current corresponds to insufficient bakeout.
6.3 Validation of MCP-Emitter performance

Figure 6.22 Current output from the MCP at low pressure, for various emission current settings.

Figure 6.23 Ratio of MCP current to emitter current at a constant pressure of $4 \times 10^{-5}$ Torr.

Similar to Figure 6.20, Figure 6.23 shows a linear relation between emission and MCP output at a lower pressure.
6.3 Validation of MCP-Emitter performance

6.3.2 Characteristics with emitters heated to 185 °C

From the plots in section 6.3.1 it is seen that electron emission behaves erratically when the microtip emitters are preconditioned by baking at 80 °C. This is attributed to adsorption of gas molecules on the tips and filamentary shorts between tips. This behavior is also attributed to insufficient bake-out of the emitter tips prior to the first emission tests. In these initial tests, the emitters were mounted on Kel-F and were heated to around 80 °C using Kapton® heater tapes. Heating the tapes any higher causes their glue to break down, and heating Kel-F® (PCTFE) higher than 150 °C causes it to melt. Hence, for subsequent tests the Kel-F insulators in the test box were replaced by ceramic tubing, and the heater tape was replaced with a tungsten filament and eventually a halogen lamp. Since the maximum bake-out of the MCP is 150 °C and we wish to bake the emitters at a higher temperature, the MCP assembly was taken out of the test box and placed in a dry box. To calibrate the temperature of the test box as a function of the filament and lamp current the emitters were also taken out, and a thermistor was positioned in their place. The halogen bulb was then controlled such that the temperature reading based on the thermistor was at an average of 185 °C. After inspection of the test box, a Spindt type emitter was placed in the ceramic tube and the thermistor was held in place behind the emitters. The heating and cooling curve in this configuration is seen in Figure 6.24. The heating conditions are similar to the case when there were no emitters in the test box. That is, while the temperature measured by using the thermistor is at 162 °C, the actual temperature on the case of the emitter array is going to be closer to 185 °C. Figure 5.4 shows the position of the emitter array. The thermistor is placed behind it in the ceramic tube.

![Figure 6.24 Temperature in the ceramic tube behind the emitters during bake-out. The curve shows a peak temperature of 162 °C. This is the temperature measured by using a thermistor which is placed behind the emitters. The position of emitters in the ceramic is seen in Figure 5.4.](image-url)
6.3 Validation of MCP-Emitter performance

The emitters were then controlled using the emitter current control circuit, and the emission current on the box can be seen in Figure 6.25. In contrast with Figures 6.18 and 6.21, where the emitters were pre-conditioned at a lower temperature, it can be seen that the emission current is steady when the emitters have been baked at a high temperature for a sufficient amount of time.

![Figure 6.25](image)

Figure 6.25 Electron emission after bake out at 185 °C with a background pressure of $2.3 \times 10^{-7}$ Torr.

Figure 6.26 shows a Fowler-Nordheim scatter plot of the average emission current, with error bars corresponding to the standard deviation of the emission. The plot also shows a linear trend that resembles the expected Fowler-Nordheim characteristic.

![Figure 6.26](image)

Figure 6.26 Fowler-Nordheim plot of emitters after bake out at 185 °C with a background pressure of $2.3 \times 10^{-7}$ Torr.
Next, the MCP assembly was replaced inside the test box, and the emitters heated to 95 °C after pumping down the vacuum chamber to $6 \times 10^{-7}$ Torr. Figure 6.27 shows the MCP output vs. pressure when $N_2$ gas is subsequently leaked into the vacuum chamber while the emission current is held approximately constant at an average level of 126 µA. In the background pressure range of $6 \times 10^{-7}$ to $4 \times 10^{-6}$ Torr, the mean current out of the MCP follows a linear characteristic with changing pressure.

![Figure 6.27 Background pressure inside vacuum chamber vs. MCP output current. Blue crosses indicate the mean current out of the MCP and error bars correspond to the standard deviation of the MCP output.](image)

Figure 6.28 The density of gas inside vacuum chamber vs. current out of the MCP. Blue crosses indicate the mean current out of the MCP and error bars correspond to the standard deviation of the MCP output.
6.3 Validation of MCP-Emitter performance

Figure 6.28 is a graph of the number density of the gas in the vacuum chamber plotted against the MCP output current in nano amperes. The density calculations are based on pressure readings from a Bayard-Alpert gauge mounted in the vacuum chamber. Pressure is converted to density using \( P = NkT \), where \( N \) is number density in \( \frac{\text{particles}}{\text{m}^3} \), \( P \) is pressure in Pascal, \( k \) is Boltzmann’s constant in J/K and \( T \) is temperature in Kelvin.

6.3.3 Discussion of MCP-Emitter performance

The Fowler-Nordheim characteristic curve for the emitter tips is seen in Figure 6.26. The linear curve fit follows the following equation:

\[
\ln \frac{I_{\text{emission}}}{V_{\text{tips}}^2} = -\frac{905.21}{V_{\text{tips}}} - 6.0211
\]  

(6.1)

This curve can be used to interpret tips voltage data since it relates the emitted current to the gate-to-tip voltage. The voltage data going into the ADC is obtained by lowering and inverting the tips-to-gate voltage by the use of a negative feedback amplifier. This input to the ADC is converted to a digital value and sent to the FPGA, from which it is sent out as part of the downlink communication. This digital value sent can be converted back to a tips voltage using Table 4.2. The conversion factor is based on circuit components on the lower board. The slope and intercept of the Fowler-Nordheim curve shown are expected to change as the emitters age with exposure to oxygen gas in the thermosphere. For this reason the SNeuPI instrument will be useful for measuring relative neutral density fluctuations, but not absolute values of pressure or density.

Background pressure inside vacuum chamber vs. MCP output current is seen in Figure 6.27. The linear curve fit for this plot follows the following equation:

\[
I_{\text{MCP out}} = 0.030461 \times P + 0.063882
\]  

(6.2)

where \( P \) is the Pressure in the vacuum chamber in micro Torr, and \( I_{\text{MCP out}} \) is the absolute value of the current out of the MCP in nano-amps. This linear curve is obtained at a fixed emission level, \( I_{\text{emission}} = 126 \mu A \). Similarly linear curve fit for Figure 6.28 follows the following equation:

\[
I_{\text{MCP out}} = 9.5294 \times 10^{-19} \times n + 0.064456
\]  

(6.3)

where \( n \) is the number density of gas in the vacuum chamber in \( \frac{\text{particles}}{\text{m}^3} \), and \( I_{\text{MCP out}} \) is the absolute value of the current out of the MCP in nano-amps.

When compared to the MCP output current levels seen in section 6.3.1, it is seen that the MCP output values are lower in section 6.3.2. The lower values can be accounted for by the fact that the MCP degrades as it is used, especially when stored outside a vacuum. Also, the MCP assembly used was exposed to gas generated when the heater tapes broke down at high temperates in earlier tests. It is expected that a new MCP assembly will provide higher output.
levels. Some of the fluctuations of error bars can also be accounted for by the fact that the amount of gas leaked into the vacuum chamber can have fluctuations that are not well controlled.

In all the test cases it is seen that the MCP output current is lower than the estimation in Chapter 2. The expected current out of the MCP is a function of the state of the MCP, gain and voltage of the MCP, ionization efficiency, ionization cross section, the density of the gas and the emission current. While values of some parameters like the charge of an electron and temperature of the gas are known, some of the parameters mentioned above are an estimate at best. Also, the SIMION® study performed at the simulation stage considered the electron energy to be at 150 eV. As these electrons approach the MCP, their energy reduces. The maximum ionization is expected to happen in the middle of the chamber. However, based on the type of emitters used and test results obtained, the initial electron energy is much lower. This lower electron energy is going to lower the estimate of the number of neutrals that get ionized and change the ionization cross-section.

This chapter presented validation results of the electronics that serve as an effective control and monitoring system for the SNeuPI sensors. The performance of the MCP and emitter system is evaluated, and results are presented. Overall conclusions from the tests described here are given in the next chapter.
Chapter 7

Conclusion and Future Work

7.1 Conclusion

This thesis details the need, principle and design of a low powered instrument that can be used to measure neutral density variations in the lower atmosphere. Results are presented that validate the SNeuPI concept in a test box that mimics the actual flight instrument. Despite the issues noted concerning testing, the data presented in Chapter 6 leads to several conclusions:

1. The emitters perform better when they are pre-conditioned by heating them to \( \sim 185 \, ^\circ\text{C} \) in vacuum. The electron emission was found to be significantly more stable after such preconditioning (compare Figures 6.18 and 6.21 with Figure 6.25).

2. The positive ion current to the MCP scales linearly versus the emitter current at a fixed pressure, even when the emission is not constant. This behavior is shown in Figures 6.20 and 6.23, at different pressures.

3. After appropriate preconditioning, the ion current measured by the MCP scales linearly versus the background pressure when the emission current is constant. Therefore, the SNeuPI detector can detect fluctuations in the ambient pressure, as long as the emitter current is well controlled.

4. The chamber pressure range over which the system was tested corresponds to altitudes in the low-earth orbit of \( \sim 127 \) to \( 155 \) km (based on MSIS-E-90 Atmosphere Model for Blacksburg, VA - 1/1/2014, 9 am). The background pressure outside the accommodation chamber is going to be 12-15 times lower than the chamber pressure. This is due to ram-effect on the satellite which is going to increase the pressure inside the chamber. Therefore, the operational altitude that these pressure ranges correspond to is going to be much higher (170 to 240 km).

Thus, it has been demonstrated that the instrument concept is valid for the LAICE CubeSat mission.
7.2 Future work

Further work needs to be performed where tests are done in the actual flight accommodation chamber. End-to-end calibration needs to be performed using new MCP assemblies and flight emitters. The end-to-end calibration should be performed using the three circuit boards to provide current and voltage curves for the flight emitters. An external electro-meter was used for the measurements. This will be substituted by a daughter board which converts the negative MCP current to a positive current for the log-amp.

The emitters used in the tests mentioned in this thesis were meant to work in nitrogen. However, the ones that are going be flown aboard the CubeSat will be fabricated from different materials (carbide based), to enable them to function in oxygen-dominated space conditions. These are expected to have a slightly higher turn-on voltage and there will be variations in the calibration curves relating MCP output current to pressure. The test results also demonstrate the importance of pre-conditioning the microtip emitters. This requirement is also expected to apply to the carbide based emitters. Despite the difference in the microtips, the circuit designs have been shown capable of driving the emitter array. Variation of the emitter turn on voltage vs. pressure for the new emitters can also be characterized. There isn’t expected to be a large variation of the turn-on voltage with respect to pressure changes.

As discussed in section 6.3.3, to provide a better estimate of the current out of the MCP, it is necessary to characterize its behavior independently. This characterization can be performed in two ways. Placing an ion source with a known flux in front of the MCP, and biasing the MCP in its present configuration can help characterize the MCP better. On the other hand, having an electron source in front of the MCP and biasing the MCP plates to attract these electrons can also help determine the gain of the MCP.

The swept neutral pressure instrument (SNeuPI) presented in this thesis forms an effective system to measure the density changes in the lower atmosphere. With further tests and calibration with the new emitters, SNeuPI can be flown aboard a CubeSat.
References


Appendix A

Upper Board: Schematics and Bill of Materials

Appendix A contains schematics and bill of materials for the SNeuPI upper board.
Figure A.1 Upper board schematic: RS-422 communication
Figure A.2 Upper board schematic: FPGA section
Figure A.3 Upper board schematic: Digital to analog and high voltage converters
Figure A.4 Upper board schematic: Voltage monitors
Figure A.5 Upper board schematic: Power system 1

Figure A.6 Upper board schematic: Power system 2
Figure A.7 Upper board schematic: Analog to digital converter and multiplexer
Figure A.8 Upper board schematic: Lower and daughter board connectors
<table>
<thead>
<tr>
<th>Qty</th>
<th>Value</th>
<th>Part</th>
<th>Device</th>
<th>Package</th>
<th>MF</th>
<th>MPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>29</td>
<td>0</td>
<td>R2, R9, R10, R15, R17, R21, R33, R34, R35, R37, R38, R39, R40, R45, R46, R50, R53, R57, R62, R65, R69, R73, R81, R85, R97, R99, R93, R95, R96, R98, R99, R100</td>
<td>RESISTOR, THICK, OR, 0.1W, 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-3EGY080V0</td>
</tr>
<tr>
<td>33</td>
<td>0.1uF</td>
<td>C5, C6, C7, C15, C16, C17, C22, C26, C27, C28, C29, C32, C33, C37, C43, C46, C51, C54, C56, C59, C62, C63, C64, C68, C69, C70, C72, C81, C83, C86, C90, C92, C95</td>
<td>CAP CER 0.1UF 25V 20% X7R 0.06T0</td>
<td>C1608</td>
<td>[EIA] TDK Corporation</td>
<td>C1608X7R10104M</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>R100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>1.0uF</td>
<td>C1, C4, C13, C14, C31, C39, C40, C41, C42, C50, C53, C65, C71, C73, C82, C84</td>
<td>RES SMD 1.0mF 5% 1/2W 0.06T0</td>
<td>C1608</td>
<td>[EIA] TDK Corporation</td>
<td>C1608X7R10105M080AB</td>
</tr>
<tr>
<td>3</td>
<td>1.5k</td>
<td>R48, R52, R56</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-PF1510V</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1.8u</td>
<td>R16</td>
<td>RES SMD 1.8uF 5% 1/2W 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-PF1510V</td>
</tr>
<tr>
<td>21</td>
<td>100</td>
<td>R5, R6, R7, R8, R12, R13, R14, R22, R23, R24, R25, R26, R28, R39, R36, R41, R60, R61, R97, R99, R3, R49, R64, R75, R83, R87, R91</td>
<td>RES 100K OHM 1/2W 5% 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-3EGY010V</td>
</tr>
<tr>
<td>10K</td>
<td>R67</td>
<td></td>
<td>RES 10K OHM 1/2W 5% 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-3EGY010V</td>
</tr>
<tr>
<td>10pF</td>
<td>C88,C89,C90,C92</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0.1uF</td>
<td>C1, C34, C70, C79, C91</td>
<td>RES SMD 0.1uF 10% 1/2W 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-PF1510V</td>
</tr>
<tr>
<td>1</td>
<td>10K</td>
<td>R100</td>
<td>RES SMD 10K OHM 5% 1/2W 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-3EGY010V</td>
</tr>
<tr>
<td>100K</td>
<td>R23, R25</td>
<td></td>
<td>RES SMD 100K OHM 5% 1/2W 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-3EGY010V</td>
</tr>
<tr>
<td>100K</td>
<td>R100</td>
<td></td>
<td>RES SMD 100K OHM 5% 1/2W 0.06T0</td>
<td>R0603</td>
<td>Panasonic</td>
<td>ERJ-3EGY010V</td>
</tr>
<tr>
<td>10pF</td>
<td>C88,C89,C90,C92</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10pF</td>
<td>C88,C89,C90,C92</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10pF</td>
<td>C88,C89,C90,C92</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10pF</td>
<td>C88,C89,C90,C92</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.25</td>
<td>VQG100</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table A.1 Bill of materials: SNeuPI upper board
Appendix B

Lower Board: Schematics and Bill of Materials

Appendix B contains schematics and bill of materials for the SNeuPI lower board.
Figure B.1 Schematic of lower board
# Table B.1 Bill of materials: SNeuPI lower board

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Reference</th>
<th>Part</th>
<th>PCB Footprint</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Mfrptno</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>C1, C2, C5, C6, C40</td>
<td>0.1u</td>
<td>CC1210</td>
<td>CER, 50V, XTR</td>
<td>Kemet</td>
<td>C1210C040KRCTRUT</td>
</tr>
<tr>
<td>2</td>
<td>C9, C12</td>
<td>0.33u</td>
<td>CC1210</td>
<td>CER, 100V, XTR</td>
<td>AVX Corporation</td>
<td>AVX5355X5R</td>
</tr>
<tr>
<td>2</td>
<td>C10, C17</td>
<td>3.3u</td>
<td>CC1210</td>
<td>CER, 25V, XTR</td>
<td>AVX Corporation</td>
<td>AVX5355X5R</td>
</tr>
<tr>
<td>3</td>
<td>C11, C13, C16</td>
<td>10u 5V</td>
<td>6032</td>
<td>POLAR, TANT, 15V, LOW ESR</td>
<td>AVX Corporation</td>
<td>TRJC10K0505F0600</td>
</tr>
<tr>
<td>5</td>
<td>C13, C14, C27, C34, C35</td>
<td>10u 5V</td>
<td>cap1210</td>
<td>CER, 55V, X5R</td>
<td>Taiyo Yuden</td>
<td>UM3K2SB1106K6M-T</td>
</tr>
<tr>
<td>2</td>
<td>C23, C31</td>
<td>1p</td>
<td>CC0805</td>
<td>CER, 50V, NP0</td>
<td>Yageo</td>
<td>CC1005RN509BN120</td>
</tr>
<tr>
<td>2</td>
<td>C2, C32</td>
<td>0.33u</td>
<td>CC0805</td>
<td>CER, 100V, X7R</td>
<td>A VX Corporation</td>
<td>12101C334KAZ2A</td>
</tr>
<tr>
<td>2</td>
<td>C24, C33</td>
<td>0.33u</td>
<td>CC0805</td>
<td>CER, 100V, X7R</td>
<td>A VX Corporation</td>
<td>12101C334KAZ2A</td>
</tr>
<tr>
<td>1</td>
<td>C41</td>
<td>0.1u</td>
<td>CC0805</td>
<td>CER, 25V, X5R</td>
<td>Kemet</td>
<td>C0805C04X5R3ACTU</td>
</tr>
<tr>
<td>1</td>
<td>C41</td>
<td>0.1u</td>
<td>CC0805</td>
<td>CER, 25V, X5R</td>
<td>Kemet</td>
<td>C0805C04X5R3ACTU</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>MMBD4148-7-F</td>
<td>so23</td>
<td>Diodes - 75V 350mA</td>
<td>Diodes Incorporated</td>
<td>MMBD4148-7-F</td>
</tr>
<tr>
<td>2</td>
<td>D2, D3</td>
<td>MBAT70-7-F</td>
<td>so23</td>
<td>Diodes - 70V 200mA</td>
<td>Diodes Incorporated</td>
<td>MBAT70-7-F</td>
</tr>
<tr>
<td>1</td>
<td>J21</td>
<td>OMN21-A29400</td>
<td>21 Pin Connector Omnetics</td>
<td>Omnetics</td>
<td>A29400-021</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J22</td>
<td>OMN9-A29400</td>
<td>9 Pin Connector Omnetics</td>
<td>Omnetics</td>
<td>A29400-009</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Q2</td>
<td>MMBT3904</td>
<td>so23</td>
<td>NPN, 40V, 200mA</td>
<td>Fairchild Semiconductor</td>
<td>MMBT3904</td>
</tr>
<tr>
<td>1</td>
<td>Q5</td>
<td>BSS127</td>
<td>so23</td>
<td>MOSFET, NCH, 250V</td>
<td>Fairchild Semiconductor</td>
<td>BSS127-7</td>
</tr>
<tr>
<td>1</td>
<td>Q6</td>
<td>MMBS7006/5OT</td>
<td>so23</td>
<td>NPN, 40V, 200mA</td>
<td>Fairchild Semiconductor</td>
<td>MMBT3906</td>
</tr>
<tr>
<td>1</td>
<td>R3</td>
<td>47k</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF4702V</td>
</tr>
<tr>
<td>1</td>
<td>R3</td>
<td>200k</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF2003V</td>
</tr>
<tr>
<td>1</td>
<td>R10</td>
<td>0</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-46GE0080V</td>
</tr>
<tr>
<td>5</td>
<td>R11, R15, R22, R29, R39, R47</td>
<td>100k</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF1003V</td>
</tr>
<tr>
<td>1</td>
<td>R12</td>
<td>499</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF4990V</td>
</tr>
<tr>
<td>2</td>
<td>R27, R33</td>
<td>301</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF3010V</td>
</tr>
<tr>
<td>1</td>
<td>R6, R30, R41</td>
<td>1k</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF1001V</td>
</tr>
<tr>
<td>2</td>
<td>R36, R48</td>
<td>26.7k</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF2672V</td>
</tr>
<tr>
<td>1</td>
<td>R37</td>
<td>137</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF1370V</td>
</tr>
<tr>
<td>1</td>
<td>R38</td>
<td>33.2k</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF3322V</td>
</tr>
<tr>
<td>1</td>
<td>R40</td>
<td>100</td>
<td>0805</td>
<td>1/8W</td>
<td>PANASONIC</td>
<td>ERI2-48NF1000V</td>
</tr>
<tr>
<td>3</td>
<td>R42, R43, R44</td>
<td>50M</td>
<td>1206</td>
<td>0.3W</td>
<td>Vishay</td>
<td>CR1V1206F5000M0F5ES</td>
</tr>
<tr>
<td>1</td>
<td>R45</td>
<td>2M</td>
<td>1206</td>
<td>1/4W</td>
<td>Vishay</td>
<td>CRCW12062M00FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R46</td>
<td>1M</td>
<td>1206</td>
<td>1/2W</td>
<td>Vishay</td>
<td>CRCW12061M00FKEAHP</td>
</tr>
<tr>
<td>7</td>
<td>TP1, TP2, TP3, TP4, TP5, TP6, TP7</td>
<td>TESTPOINT 0.040” (1.02mm) Hole Diameter</td>
<td>TESTPOINT</td>
<td>Keystone Electronics</td>
<td>5001</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>T1</td>
<td>T6650-D</td>
<td>coilcraft_d_size</td>
<td>Transformer, Miniature, SMT, 1:5</td>
<td>Colorcraft</td>
<td>T6650-D</td>
</tr>
<tr>
<td>1</td>
<td>T2</td>
<td>T6843-D</td>
<td>coilcraft_d_size</td>
<td>Transformer, 1CT, 1:5, SMT, 1:1</td>
<td>Colorcraft</td>
<td>T6843-D</td>
</tr>
<tr>
<td>3</td>
<td>U1, U12, U3</td>
<td>MMBD30045-7-F</td>
<td>so23</td>
<td>Dual Schottky, 300V, 70mA, SOT-23</td>
<td>Diodes Incorporated</td>
<td>MMBD30045-7-F</td>
</tr>
<tr>
<td>1</td>
<td>U6</td>
<td>LM2937IMP-10</td>
<td>so223</td>
<td>10V REGULATOR</td>
<td>Texas Instrument</td>
<td>LM2937IMP-10N0PB</td>
</tr>
<tr>
<td>1</td>
<td>U7</td>
<td>MAX845</td>
<td>soic8</td>
<td>IC, 5V TRANSFORMER DRIVER</td>
<td>Maxim</td>
<td>MAX6403ESA+T</td>
</tr>
<tr>
<td>2</td>
<td>U11, U17</td>
<td>TLC2720BDR</td>
<td>soic8</td>
<td>LcMOS Precision Amp</td>
<td>Texas Instrument</td>
<td>TLC2720BDR</td>
</tr>
<tr>
<td>1</td>
<td>U16</td>
<td>HCNR201</td>
<td>8_smd_gl (8 DIP Gull wing)</td>
<td>Asic Technologies</td>
<td>HCNR201-300E</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U18</td>
<td>MAX603/5O SO</td>
<td>soic8</td>
<td>3.35/AdV LDO</td>
<td>Maxim</td>
<td>MAX603/5ES3A+</td>
</tr>
<tr>
<td>1</td>
<td>U19</td>
<td>LMC6082</td>
<td>soic8</td>
<td>Precision Dual Opamp</td>
<td>Texas Instrument</td>
<td>LMC6082AAMXN0PB</td>
</tr>
</tbody>
</table>
Appendix C

Daughter Board: Schematics and Bill of Materials

Appendix C contains schematics and bill of materials for the SNeuPI daughter board.
Figure C.1 Schematic of daughter board

Current to Voltage conversion - Logarithmic amplifier

R: Y of COP2011/Measured negative current from

JQ2: Connection to the signal wire in the daughter connector as a support mechanism.

Input current wire connector

VINCERHE

Connects to pin 4 (terminal) of COP203 in the air
### Table C.1 Bill of materials: SNeuPI daughter board

<table>
<thead>
<tr>
<th>Reference</th>
<th>qty</th>
<th>Value</th>
<th>Package</th>
<th>Manufacturer PN</th>
<th>Manufacturer Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C3, C6, C61</td>
<td>4</td>
<td>0.1uF</td>
<td>C-USC0805</td>
<td>CG402XTE1E04K120AA TDK Corporation</td>
<td>CAP CER 0.1UF 25V 10% X7R 00805</td>
</tr>
<tr>
<td>C2, C5</td>
<td>2</td>
<td>10uF</td>
<td>C-USC0805</td>
<td>CG402XTE1E04K085AC TDK Corporation</td>
<td>CAP CER 10UF 25V 10% X5R 00805</td>
</tr>
<tr>
<td>C4, C7</td>
<td>2</td>
<td>100pF</td>
<td>C-USC0805</td>
<td>CG402XTE1E04K120AA TDK Corporation</td>
<td>CAP CER 100PF 100V 5% COG 00805</td>
</tr>
<tr>
<td>D1</td>
<td>1</td>
<td>0.0805</td>
<td>BAV70</td>
<td>BAV70-7-F</td>
<td>Diodes Incorporated DIODE ARRAY GP 75V 100MA SOT23-3</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>10M</td>
<td>R-US_R1206</td>
<td>CHV1206AF1000MFE5</td>
<td>Vishay Dale RES SMD 100 OHM 1% 0.3W 1206</td>
</tr>
<tr>
<td>R2, R3, R4</td>
<td>3</td>
<td>20M</td>
<td>R-US_R1206</td>
<td>CHV1206AF2000MFE5</td>
<td>Vishay Dale RES SMD 20M OHM 1% 0.3W 1206</td>
</tr>
<tr>
<td>R5</td>
<td>1</td>
<td>16K</td>
<td>R-US_R0805</td>
<td>ERA-6AEB163V</td>
<td>Panasonic Electronic Components RES SMD 16K OHM 0.1% 1/8W 00805</td>
</tr>
<tr>
<td>R6</td>
<td>1</td>
<td>26.7K</td>
<td>R-US_R0805</td>
<td>ERA-6AEB2672V</td>
<td>Panasonic Electronic Components RES SMD 26K OHM 0.1% 1/8W 00805</td>
</tr>
<tr>
<td>R7</td>
<td>1</td>
<td>1.5K</td>
<td>R-US_R0805</td>
<td>ERA-6AEB152V</td>
<td>Panasonic Electronic Components RES SMD 1.5K OHM 0.1% 1/8W 00805</td>
</tr>
<tr>
<td>R8</td>
<td>1</td>
<td>9.1M</td>
<td>R-US_R1206</td>
<td>RC1206FR079M1L</td>
<td>Yageo RES SMD 9.1M OHM 1% 1/4W 1206</td>
</tr>
<tr>
<td>TP1, TP2, TP3</td>
<td>3</td>
<td>TESTPOINT</td>
<td>0.040&quot; (1.02mm) Hole Diameter</td>
<td>5001</td>
<td>Keystone Electronics TESTPOINT</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>LOG114</td>
<td>SSM2212</td>
<td>LOG144A1RGVT</td>
<td>Texas Instruments IC OPAMP LOG 15MHZ 16VQFN Audio, Dual-Matched NPN Transistor IC OPAMP LOG 15MHZ 16VQFN Audio, Dual-Matched NPN Transistor</td>
</tr>
<tr>
<td>U2</td>
<td>1</td>
<td>SSM2212</td>
<td>8-SOIC</td>
<td>SSM2212RZ-R7</td>
<td>Texas Instruments Analog Devices IC OPAMP LOG 15MHZ 16VQFN Audio, Dual-Matched NPN Transistor IC OPAMP LOG 15MHZ 16VQFN Audio, Dual-Matched NPN Transistor</td>
</tr>
<tr>
<td>U3</td>
<td>1</td>
<td>OPA703</td>
<td>SOT23-5</td>
<td>OPA703NA250</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>U4</td>
<td>1</td>
<td>LTC2997HDCB</td>
<td>6-WFDFN Exposed Pad</td>
<td>LTC2997HDCB#TRMPBF</td>
<td>Linear Technology SENSOR TEMP RATIO/METRIC 6DFN</td>
</tr>
<tr>
<td>J24</td>
<td>1</td>
<td>JF1P1510B4597</td>
<td>JF1P1510B4597</td>
<td>Winchester</td>
<td>JF series connector</td>
</tr>
</tbody>
</table>
Appendix D

Digital Design Simulation Waveforms

Appendix D contains FPGA waveforms from simulation of the digital design in Libero SOC and Modelsim. The most elegant way of simulating the digital design is to open the design project in Libero SOC and then simulating it interactively in ModelSim.

Figure D.1 ModelSim simulation of the DAC control using FPGA. Test waveform to show the output of DAC on channel 1. MCP control values correspond to the output which is shifted out on the SDI line when chip select goes low.

Figure D.2 ModelSim simulation of the ADC control using FPGA. The oscillator clock signal has a 100 ns period corresponding to a 10 MHz clock rate. The FPGA divides this by eight times to produce a 1.25 MHz clock which is fed through to the ADC. 24 ADC clock cycles represent a conversion period. The first 8 clocks correspond to the command word sent to the ADC and the next 16 clocks represent the data shifted out of the ADC.
Appendix E

MATLAB Instrument Control

Below is a MATLAB code listing to control Keithley electrometers over the GPIB interface.

% Find a GPIB object.
obj6517B = instrfind ('Type', 'gpib', 'BoardIndex', 0,
... 'PrimaryAddress', 12, 'Tag', '');

% Create the GPIB object if it does not exist
% otherwise use the object that was found.
if isempty(obj6517B)
    obj6517B = gpib ('NI', 0, 12);
else
    fclose (obj6517B);
    obj6517B = obj6517B (1)
end

% Connect to instrument object, obj1.
 fopen (obj6517B);

% Configure instrument object, obj1.
 set (obj6517B, 'EOSCharCode', 'LF');

% Communicating with instrument object, obj1.
 name6517 = query (obj6517B, '*IDN?'); % get instrument ID
 fprintf (obj6517B, 'CONF:CURR'); % Configure instrument to read current
data6517 = query (obj6517B, 'READ?'); % Get a current reading

% Use as a voltage source
 fprintf (obj6517B, ':SOUR:VOLT 0'); % Set voltage level
 fprintf (obj6517B, ':OUTP 1'); % Enable output voltage
data5 = query(obj6517B, ':OUTP:STAT?'); %read status of voltage source

% Disconnect all objects.
%fclose(obj6517B);

% Clean up all objects.
%delete(obj6517B);