High Power High Frequency 3-level Neutral Point Clamped Power Conversion System

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ABSTRACT

The high penetration of renewable energy and the emerging concept of micro-grid system raises challenges to the high power conversion techniques. Multilevel converter plays the key role in such applications and is studied in detail in the dissertation.

The topologies and modulation techniques for multilevel converter are categorized at first by a thorough literature survey. The pros and cons for various multilevel topologies and modulation techniques are discussed. The 3-level neutral point clamped (NPC) topology is selected to build a 200kVA, 20 kHz power conversion system.

The modularized phase leg building block of the converter is carefully designed to achieve low loss and stress for high frequency and high power operation. The switching characteristics for all the commutation loops of 3-level phase leg are evaluated by double pulse tests. The switching performance is optimized for loss and stress tradeoff. A detailed loss model is built for system loss distribution and loss breakdown calculation. Loss and stress for the phase leg and 3-phase system are quantified at all power factors.

The space vector modulation (SVM) for 3-level NPC converter is investigated to achieve loss reduction, neutral voltage balance and noise reduction. The loss model and simulation model provides a quantitative analysis for loss and neutral voltage ripple tradeoff. An improved SVM method is proposed to reduce NP imbalance and switching

loss simultaneously. This method also ensures an evenly distributed device loss in each phase leg and gives a constant system efficiency under different power factors.

Based on the improved modulation strategy, a new modulation scheme is then proposed with largely reduced conduction loss and switching stress. Moreover, the device loss and stress distribution on a phase leg is more even. This scheme also features on the simplified implementation. The improved switching characteristics for the proposed method are verified by double pulse tests. Also the system loss breakdown and the phase leg loss distribution analysis shows the loss reduction and redistribution result.

The harmonic filter for the grid interface converter is designed with LCL topology. A detailed inductor current ripple analysis derives the maximum inductor current ripple and the ripple distribution in a line cycle. The inverter side inductor is designed with the optimum loss and size trade-off. The grid side inductor is designed based on grid code attenuation requirement. Different damping circuits for LCL filter are evaluated in detail. The filter design is verified by both simulation and hardware experiment.

The average model for the 3-level NPC converter and its equivalent circuit is derived with the consideration of damping circuit in both ABC and d-q frame. The modeling and control loop design is verified by transfer function measurement on real hardware. The control loops design is also tested and verified on real hardware.

The interleaved DC/DC chopper is introduced at last. The different interleaving methods and their current ripple are analyzed in detail with the coupled and non-coupled inductor. An integrated coupled inductor based on 3-dimentional core structure is proposed to achieve high power density and provide both CM and DM impedance for the inductor current and output current.

To My Grandfather:

X.S. Cai

For his enlightenment and encouragement

Also to My Family:

My parents: Xiuqi Jiao
Rong Cai
My wife: Bowen Zhu

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CHAPTER.1 INTRODUCTION

This chapter presents the motivations and objectives of my research work. A literature review of the multilevel converter topologies, modulation techniques and representative applications are given. The advantages and design challenges are identified for the neutral point clamped (NPC) converter for a wide range of application in renewable energy and energy storage system. The structure and specifications for the research target are provided, followed by the dissertation outline and the scope of research.

1.1 Research Background

The demand for sustainable energy sources has never been more exigent as the energy and environmental crisis becomes critical. The renewable energy generation systems like photovoltaic (PV) and wind farms are therefore emerging in the power grid with a dramatically fast rate. The energy storage systems are also widely spread in power grid as conditioner and compensator for the renewable energy sources with intermittent and stochastic property. Such changes occur not only at power generation side, but also at power consumption side with the rooftop PV panels, plug-in electrical vehicles and super-charge stations are connected to the residential and commercial communities. The high penetration of the renewable energy and energy storage system dramatically changes the infrastructures of power grid. The renewable energy smart grid in the future is reformed as in Fig.1.1, where the power converters not only serve as renewable energy grid interface, but also replace the traditional power transformer and switch gears for power transmission and distribution. With the decreased volume and weight, higher efficiency, more intelligent control and better performance, the power converters play the key role as energy router and energy control center (ECC) in future smart grid [1]-[3]. Such an

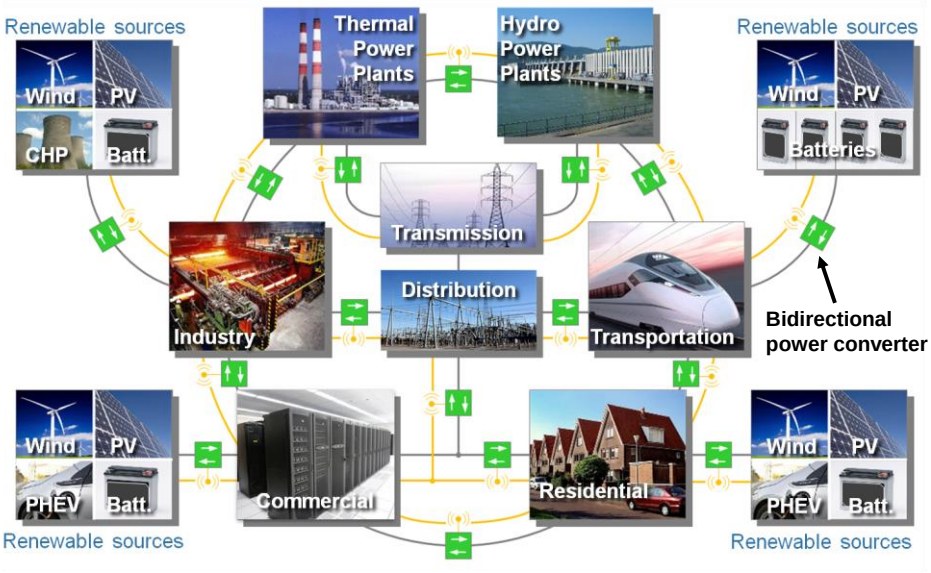


Fig. 1.1. Infrastructure of future renewable energy smart grid

ambitious goal can only be achieved by the high voltage high power converter. At power generation side, it serves as renewable energy and energy storage grid interface. For power transmission and distribution, high power converter is the key part for high voltage DC (HVDC) transmission and flexible AC transmission system (FACTS). In the power consumption areas, it serves as motor drive for pump, fan compressor, conveyor, grinder or propulsion system in various industrial and transportation applications. It also works as uninterrupted power supply (UPS) for critical loads like data center or telecom base station in commercial applications.

To implement the high power high voltage converter, one solution relies on the high power semiconductor devices. Fig.1.2. shows the device ratings for the state of the art high power switches, which have power capability up to megawatt level. By connecting them in serial or parallel, the conventional 2-level power converter can reach high voltage and high current rating. However, the current and voltage sharing of the serial and paralleled switches are serious issue that easily fails the converter and jeopardizes the reliability and safety of the whole system. This problem is yet to be solved. In addition, the high power device can only be switched at very low frequency, which is undesirable for power density and power quality. Last but not least, the high

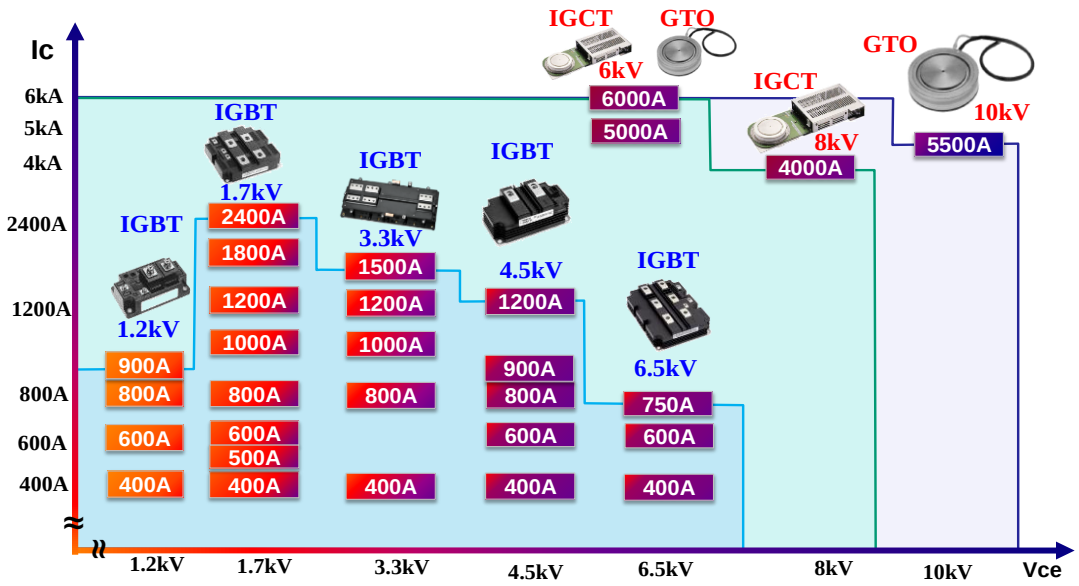
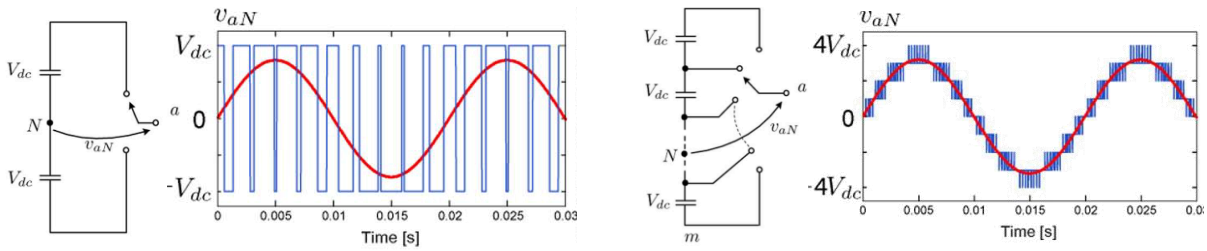


Fig. 1.2 State of the art high power semiconductor switches

power device is really expensive and requires sophisticated driving circuit, snubber circuit and protection circuit, all of which increases the cost and complexity of the converter.

Besides the device level solution for high power converter, there is also topological level solution known as the multilevel converter topology. Fig.1.3 compares the circuit structure and output waveform for 2-level and multilevel converter. The 2-level converter in Fig.1.3(a) equals to a 1 pole 2-throw switch that can only be connected to positive and negative rail. These two levels are modulated to generate the sinusoidal output voltage. On the contrary, the multilevel converter in Fig.1.3(b) is a 1 pole multi-throw switch that can generate multiple output voltage levels. There are extra control freedoms to synthesize the output voltage. As an advanced power conversion technique, the multilevel converter has several obvious advantages [4]-[8]. Firstly, each switch blocks less voltage and hence has smaller voltage stress. Since the switches are not connected in serial, there is no voltage sharing problem. Several low rating devices with low cost can be used to replace one high rating device. Secondly, each device is switched at lower voltage and has smaller dv/dt. Consequently, the switching noise is reduced and the EMI emission is ameliorated. Finally, the multilevel output voltage synthesize the sinusoidal waveform in a better

way compared to the 2-level converter. As a result, the multilevel converter has better output power quality. Also because the reduced EMI noise and improved power quality, the harmonic and EMI filter size can be significantly reduced.



(a) 2-level converter (b) Multilevel converter

Fig. 1.3. Comparison of 2-level and multilevel converter

1.2 Review of Multilevel Converter Topologies

Because of all the benefits and advantages for multilevel converter, this topology has been evolving for decades and numerous variations have been invented [9]-[13]. In general, there are four major categories for multilevel converter family as shown in Fig.1.4. The first and second categories of the flying capacitor (FC) and the neutral point clamped (NPC) converter are invented in early 1980's. The cascaded topology as the third category is first reported in 1980's as well. Then, within the last three decades, it has been widely used in high power applications. This topology is evolved in 2000's when the modular multilevel converter (MMC) topology is

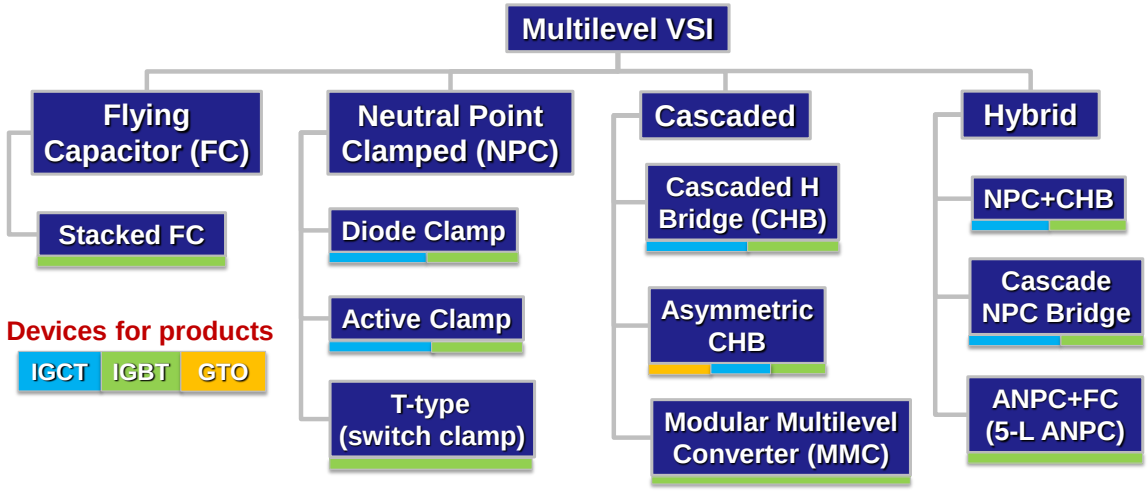


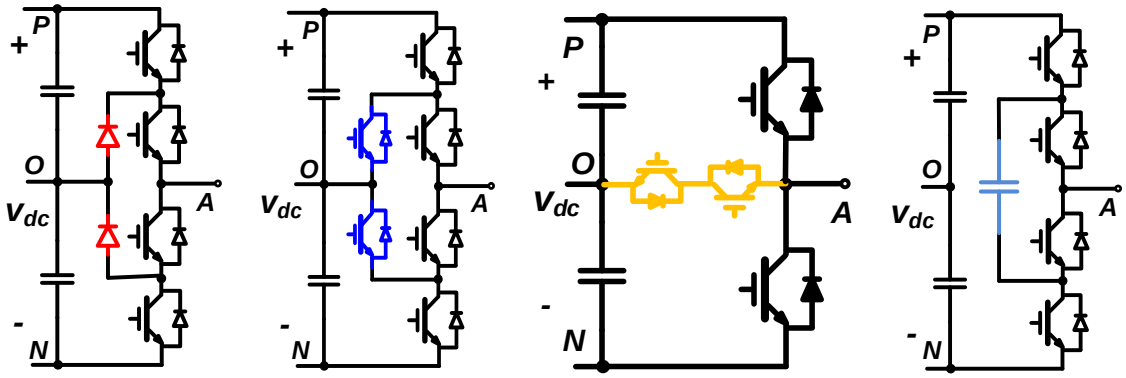
Fig. 1.4. Classification of multilevel converter topologies

proposed for even higher voltage and power rating. The fourth category of hybrid topology is a combination and mixture of the other three categories. For each of the category, it can be further divided into several subdivisions.

1.2.1 Neutral Point Clamped and Flying Capacitor Topology

The neutral point clamped topology and the flying capacitor topology share some common features in the structure. They are hence introduced together in this part. The NPC topology has three subdivisions. Fig.1.5 uses 3-level topologies as an illustration. The diode neutral point clamped (DNPC) [14] phase leg in Fig.1.5(a) is the original NPC topology, which contains two traditional 2-level half bridge cells stacked together and two clamping diodes connected to the neutral point. By replacing the clamping diodes with active switches in Fig.1.5(b), the active neutral point clamped (ANPC) topology [15] can be derived. Also the neutral point can be directly connected to the output through a bi-directional switch as shown in Fig.1.5(c). This is the T-type 3-level topology. The 3-level output voltage can also be generated by a floating capacitor as shown in Fig.1.5(d), which is the flying capacitor (FC) topology [16],[17]. Although the FC topology is classified as a separate category, it shares many similarities as the NPC topology like circuit structure, device rating and modulation strategy. Hence it is introduced together with the NPC topology here. The DNPC topology has intrinsically uneven loss and stress distribution for each device on the phase leg. The ANPC topology can solve this problem by proper control. For the T-type 3-level topology, the device number for each phase leg is reduced from 6 to 4. The conduction loss is hence reduced with less switches in the circuit. But the device rating for the two main switches that connect the positive and negative bus to the output is increased. They need to block the whole DC link voltage while the two switches for the neutral rail just block half DC link voltage. There are various configurations for the bidirectional

switches to connect the neutral point. Some configurations can be found in [18]. In addition to these issues, the NPC and T-type topologies require extra control to balance the neutral point voltage. In other word, the voltage difference between the two DC link capacitors should be considered. Although the FC circuit doesn't have the neutral point voltage balance issue, it still requires extra control to maintain the flying capacitor voltage at half DC link voltage. The voltage balance for the NPC and FC topology may bring complexity in the control scheme.



(a) DNPC (b) ANPC (c) T-type 3-level (d) Flying capacitor

Fig. 1.5. Subdivisions of NPC and FC topologies

The 3-L NPC circuit can be extended to higher level. Fig.1.6 shows the example of how the 2-level phase leg is extended to a 5-level ANPC phase leg. In general, the NPC circuit can be upscale to higher level. For an m-level DNPC phase leg, 2(m-1) switches and (m-1)×(m-2) diodes are needed. For the m-level ANPC phase leg, m×(m-1) switches are needed. Obviously, this upscale structure has very complex system configuration with large number of devices. Moreover, the unbalanced device loss issue gets worse as the level increases. So does the unbalanced capacitor voltage issue, which is almost unattainable with higher level. Due to these issues, the level number for NPC topology in common industrial practice never exceeds five. The typical industrial applications for the NPC topology include medium voltage drive and grid interface for large scale PV and wind farm.

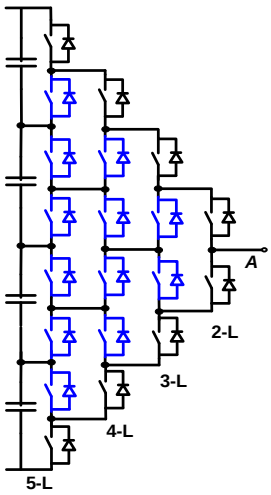
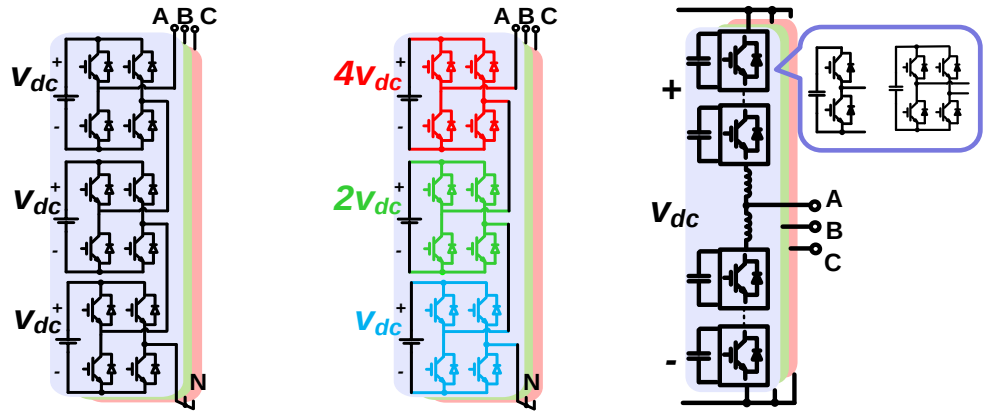


Fig. 1.6. Generalized 5-level ANPC phase leg

1.2.2 Cascaded Multilevel Topology

The cascaded topology is another widely used multilevel structure. The phase leg contains several basic 2-level converter cells that are cascaded together [19]. The output voltage reaches higher level as the cell number increases. As a result, this topology is suitable for high voltage applications. It also features on the highly scalable and modularized structure. There are several cascading configurations as shown in Fig.1.7. The symmetrical cascaded H bridge (CHB) [20] in Fig.1.7(a) is the basic structure. The phase leg with cell number equals to N in serial can produce voltage level of 2N+1. The asymmetrical CHB [21] has similar structure. The only difference is that each H bridge cell has different DC link voltage. With the proportional DC link voltage configuration, the same amount of cell can generate more voltage levels that is exponential to the cell numbers. An asymmetrical CHB with cells by N produces $2^{(N+1)}$-1 output levels. Nonetheless, each cell has different voltage stress and loss. The device rating for each cell is different and the system lost some modularity as a result. For the modular multilevel converter (MMC) [22] in Fig.1.7(c), each phase leg has two arms and each arm has several identical cells which can be either full bridge or half bridge. These cells equally share the DC link voltage. The

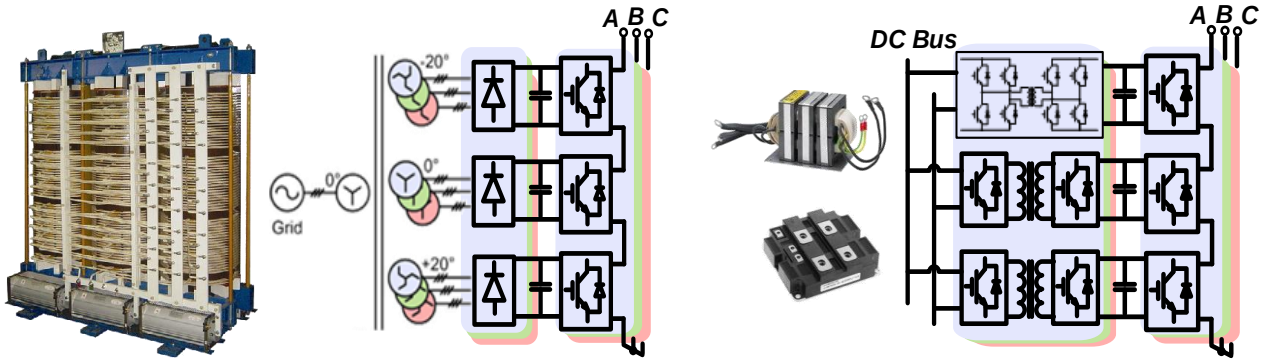
MMC with half bridge cell by N in each arm can provide level of 2N-1 which is basically the same as CHB.



(a) Symmetrical CHB (b) Asymmetrical CHB (c) MMC

Fig. 1.7. Subdivisions of cascaded topology

Though a highly modularized structure it is, the CHB circuit needs multiple isolated DC sources to generate the multilevel output. This is the major challenge for cascaded configuration. One solution uses multi-winding multi-pulse transformer plus multiple rectifier units to provide the isolated DC sources as shown in Fig.1.8(a). Here the isolation and energy transfer is achieved by the line frequency transformer. The multi-pulse structure provides good input power quality at grid side, which is the advantage for this method. But the drawback is obvious since the line frequency transformer has bulky size, heavy weight and complex structure. It takes lot of space and increases the complexity as shown in Fig.1.8(a). Moreover, the diode rectifier prevents the bidirectional operation for the whole system. This configuration is majorly used for high power high voltage motor drive system with unidirectional power flow.



(a) Line frequency isolation (b) High frequency isolation

Fig. 1.8. Two isolated DC voltage solutions for CHB

Another solution for DC source relies on high frequency isolation as shown in Fig.1.8(b). This method uses several isolated DC/DC converters with the same input DC bus to provide the isolated DC voltage. The phase shift full bridge topology is the most suitable one for the isolated DC/DC stage. The energy transfer component here is the high frequency transformer, which has size and weight benefits compared to the line frequency transformer. The DC/DC converter enables the bidirectional operation for the whole system as well. The phase shift full bridge shares the same cell structure with the cascaded H-bridge, which means a highly modularized structure for the whole system. On the other hand, this method has large number of switching devices and auxiliary circuits which may increase the total cost. Also the high switching frequency for the switch and transformer may compromise the total system efficiency.

Compared with the CHB structure, the MMC circuit does not require isolated DC sources. Only one high voltage DC source is needed for three phases, which largely simplifies the system structure. However, the operating principle of the MMC circuit results in the capacitor for each cell to be charged and discharged at line frequency. The outcome is the increased size for the line frequency capacitor with reliability issue. Fig.1.9 uses one module structure in a commercialized MMC system to illustrate the size of the capacitor. It clearly shows that the capacitor bank occupies a large portion of space while the converter itself is a small cubic. As a conclusion, the

cascaded topology has modularized structure and is suitable for high voltage application. But the DC structure is the tricky part, which requires either isolated DC sources or large capacitors.

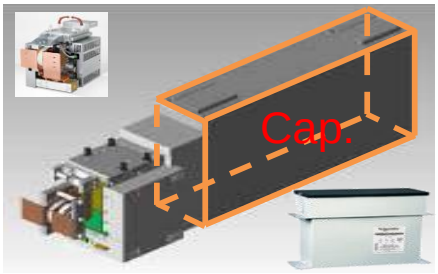
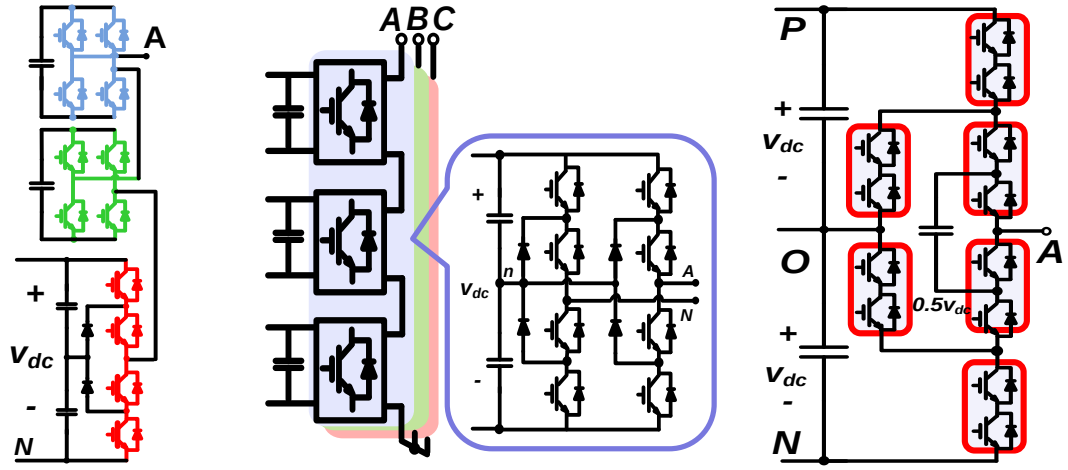


Fig. 1.9. Module structure for MMC

1.2.3 Hybrid Multilevel Topology

The hybrid topology as the name indicates, is the combination of the basic multilevel topologies. This category covers a wide range of topological combinations. To have a concise and simple paragraph, only a few typical hybrid topologies are discussed. The circuit in Fig.1.10(a) stacks the NPC topology and CHB topology together [23]. The DC link of the NPC circuit is provided by DC source while the DC side for the CHB circuit is floating. The energy is generated by the NPC part and the CHB circuit only provides extra voltage levels. The more cells in the CHB, the more output voltage level it can generate. But the combination also inherits the downside of both NPC and CHB circuit. For NPC part, the voltage balance for neutral point should be considered. As for the CHB part, the floating DC side voltage control is also an issue. For this reason, this structure has complicated voltage control for both two parts.



(a) NPC+CHB (b) Cascaded NPC H bridge (c) ANPC+FC

Fig. 1.10. Subdivisions of hybrid topology

Another topology in Fig.1.10(b) uses the 3-level NPC phase leg to form a H bridge and then cascades the NPC H bridge [24]. Each 3-level NPC bridge cell in the circuit generates 5-level output instead of 3 for the 2-level cell. For this reason, the cascaded H-NPC can generate more voltage level with less number of cells and DC voltage sources. But the number of switching device is not reduced. This topology still needs multiple isolated DC sources as the classic CHB does. The neutral point voltage balance for each H-NPC cell is also required. Since this structure still has some modularity, it is adopted by some commercial product for high power motor drive.

The hybrid topology in Fig.1.10(c) is the combination of ANPC and FC circuit [25]. The circuit structure looks like a typical NPC phase with split DC link and neutral point. But there are both clamping switches to the neutral point and a flying capacitor near the output terminal. The circuit in the figure generate 5-level output with 8 switches and 3 capacitors. On the contrary, the classic 5-level ANPC phase leg in Fig.1.6 has 20 switches and 4 capacitors. By combining the ANPC and FC topology, the circuit structure is simplified and device number is reduced. Nonetheless, this structure has complicated commutation loop during switching, which causes extra loss and stress for the switching device. Also the loss and stress distribution on each switch is uneven. In addition, both the neutral point voltage and the flying capacitor voltage need to be

controlled as for the NPC and FC circuit. As a result, this topology is simpler than the classic NPC topology with the same output voltage level. But it still have some issues to be considered.

Finally, the aforementioned multilevel topology categories are compared for a conclusion. The NPC and cascaded topologies are the two major groups for multilevel converter. The hybrid structure is a combination of these two. The NPC topology has simple structure with three or five output levels. When the level number rises up, the system becomes complicated. To reach high voltage and high power for NPC topology, high rating device should be used. The modularity for this structure stay at the phase leg level. The switching devices in the phase leg have different stress and loss. Also the neutral point voltage should be balanced by extra control. The NPC topology is suitable for medium voltage bidirectional back to back operation like motor drive since it has a single DC link. The cascaded topology can easily reach high voltage by stacking multiple cells with low rating device. This structure also features on high modularity, scalability and redundancy. But the multiple isolated DC source requirement of CHB complicates the front end configuration and prevents the bidirectional back to back operation. Nevertheless, the CHB structure is suitable for reactive power compensation in high voltage power grid. This application does not need active power transfer, hence the isolated DC sources can be saved. The only thing needs to be worried about is the balance of multiple floating DC side capacitors. The MMC topology has single high voltage DC link with modularized low voltage cell. It is suitable for high voltage bidirectional back to back operation like HVDC application. Also it can be used as reactive power compensation and motor drive. The only issue for MMC topology is the large capacitors with line frequency charging and discharging.

1.3 Review of Multilevel Converter Modulation Strategies

The modulation strategy is tightly connected with the topology for multilevel converter and it largely determines the system performance. For this reason, the modulation strategies are also reviewed in this chapter. The categories of the modulation strategies are shown in Fig.1.11 in a similar way for the topology categories. There are two major groups for modulations. One is the

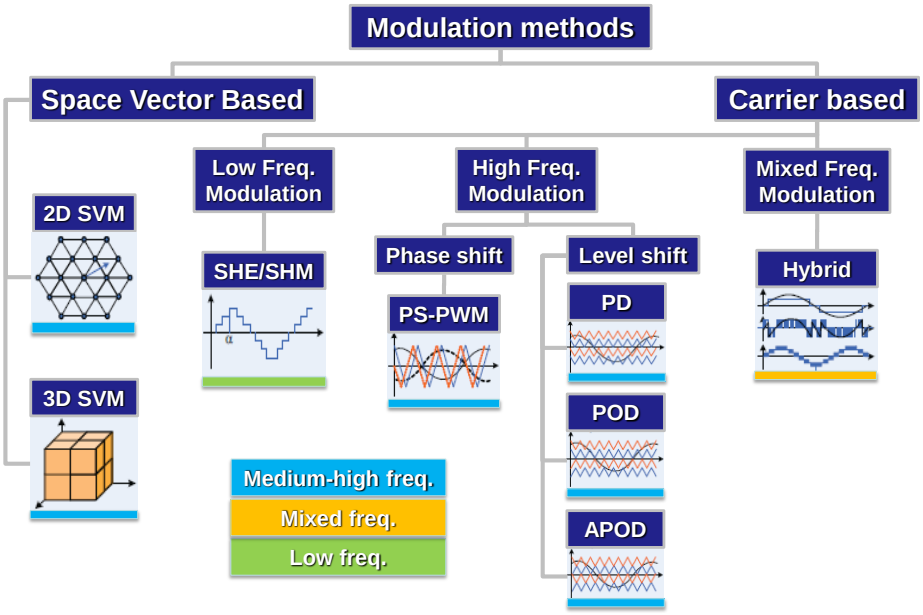


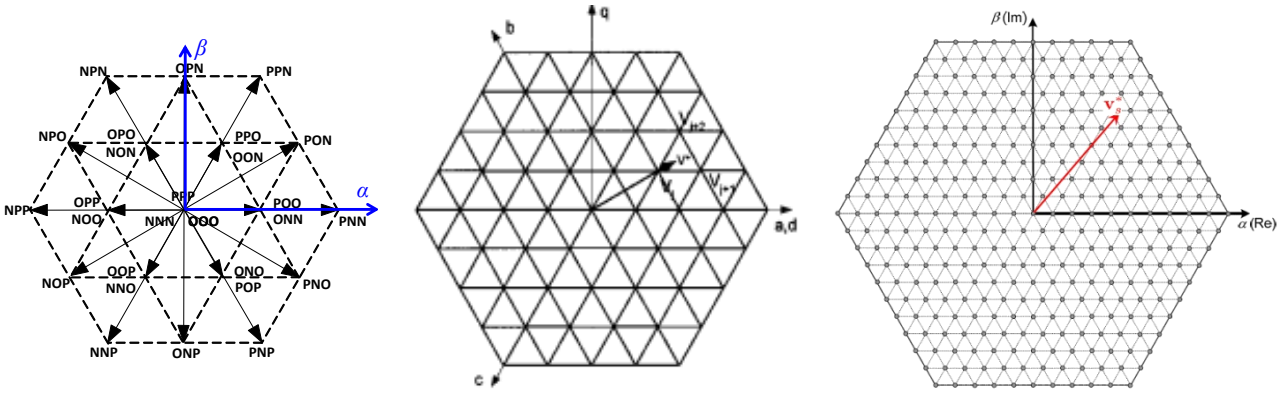
Fig. 1.11. Classification of modulation strategies for multilevel converter

space vector based and the other one is carrier based. The space vector based method has 2D and 3D SVM. For carrier based methods, there are low frequency, high frequency and mixed frequency modulations. The high frequency modulation can be further divided into several subdivisions. Different modulation methods fit to different topologies with various performance.

1.3.1 Space Vector Based Modulation

The space vector modulation is based on the 3-phase system [26], [27]. The different switching states for the 3-phase multilevel converter can be mapped to the line to line voltage space and they form a space vector hexagon. The voltage reference can also be mapped to the hexagon and it can be synthesized in various manners by the space vectors, or the switching

status. For a three-level converter, each phase leg has 3 switching states and the 3-phase system has 27 switching states, which corresponds to 19 space vectors in the hexagon as shown in Fig.1.12(a). There are redundant switching states for some vectors, which can be used as freedom to achieve certain control objectives. For a converter with higher level, there will be large number of space vectors. Fig.1.12(b) and (c) show the space vector hexagons for a 5-level and 11-level converter. It can be concluded that the number of switching states is the cubic of the level numbers for multilevel converter. The higher level gives more redundant switching states for control freedom. But it also causes higher computation cost for the reference voltage locating



(a) 3-level (b) 5-level (c) 11-level

Fig. 1.12. Space vector hexagon for multilevel converter

and the vector selection from a large number of candidates. For this reason, the SVM is not realistic for implementation when the level goes high. But it is extremely suitable for 3-level NPC topology since the calculation is not complex and there is control freedom to achieve neutral point voltage balance. The 3-D SVM is the extension of 2-D SVM when there is a fourth phase leg for the system. Then the space vectors are mapped on the 3-D column or cube. This is a special case with particular application. The implementation is even more complicated. For this reason, it will not be covered in this part.

1.3.2 Carrier Based Low Frequency Modulation

Different from vector based modulation, the carrier based modulation can be applied to both 3-phase system and single phase leg. Its implementation is also simpler than SVM. For the carrier based modulation, it can be further divided into 3 categories according to the switching frequency of the device. The low frequency modulation [28] [29] is based on the staircase synthesis. The sinusoidal voltage waveform can be represented by stacking multiple 2-level square wave. The multilevel converter with very high level number can generate perfect sinusoidal waveform. As a result, this modulation is usually applied to cascaded topology with high level number. The typical low frequency modulation waveform for CHB is shown in Fig.1.13 with three modules. Each module has only four commutations per line cycle and the switching loss is ignorable. This is the major benefit for this modulation. Also by properly set the trigger angle for each module, certain order harmonics can be reduced or even eliminated at the output voltage. This is the selective harmonic elimination (SHE) method used in low frequency modulation. This method is based on the pre-calculated trigger angle for each cell. The transient response may be compromised with the fixed trigger angle. Another obvious issue for the modulation in Fig.1.13 is the unevenly distributed conduction loss for each cell. To solve this problem, the pulse alteration low frequency modulation is used as shown in Fig.1.14. This method alternatively applies pulses with different length on each module to balance the conduction loss. The total system loss is balanced within several line cycles

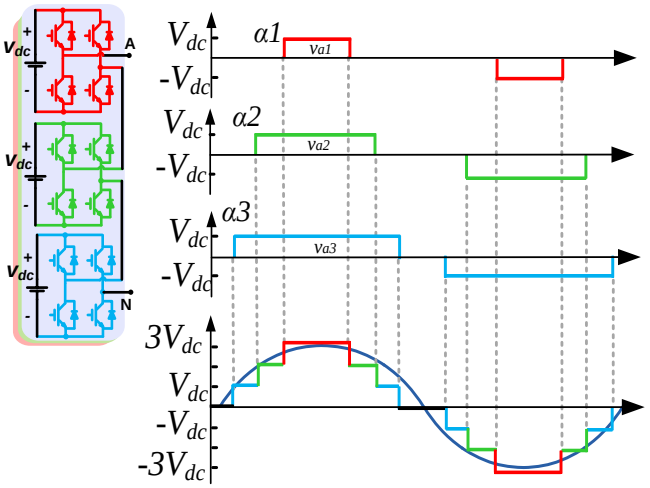


Fig. 1.13. Low frequency modulation

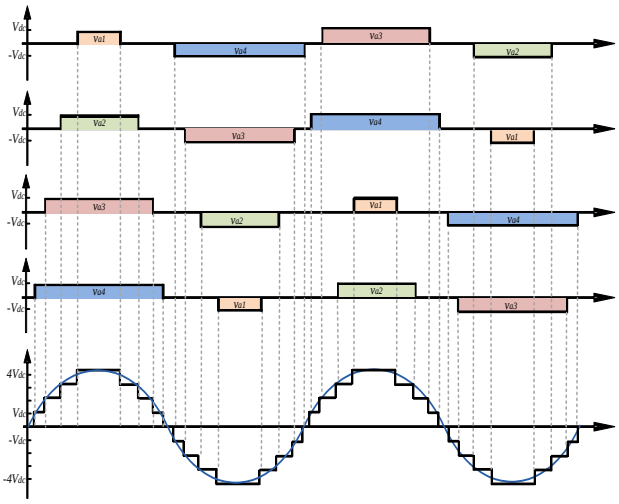


Fig. 1.14. Pulse alteration modulation

1.3.3 Carrier Based High Frequency Modulation

If the converter does not have many levels, the low frequency modulation may not have good power quality and the high frequency modulation should be used. The carrier based high frequency modulation also has two categories. One is the phase shifted modulation and the other one is level shifted modulation [28], [30].

For the phase shifted (PS) modulation, the carrier for each cell has a phase shift with the other carriers. The specific phase shift angle is 180° divided by the module numbers. Fig.1.15 gives the illustration of the phase shift method. For the CHB circuit with 3 modules in this

example, the phase shift angle is 60°. It can also be observed from the figure that all the modules in a phase leg have the same switching pattern. The switching frequency and switching loss for each module is therefore naturally balanced. The thermal design for each cell can be modularized due to this reason. Another benefit for this modulation is the high equivalent switching frequency at the output, which equals to the switching frequency for each carrier times the cell numbers. The more cells in the phase leg, the higher switching frequency and lower THD at its output. Consequently, the phase shift method is especially suitable for CHB and MMC topology.

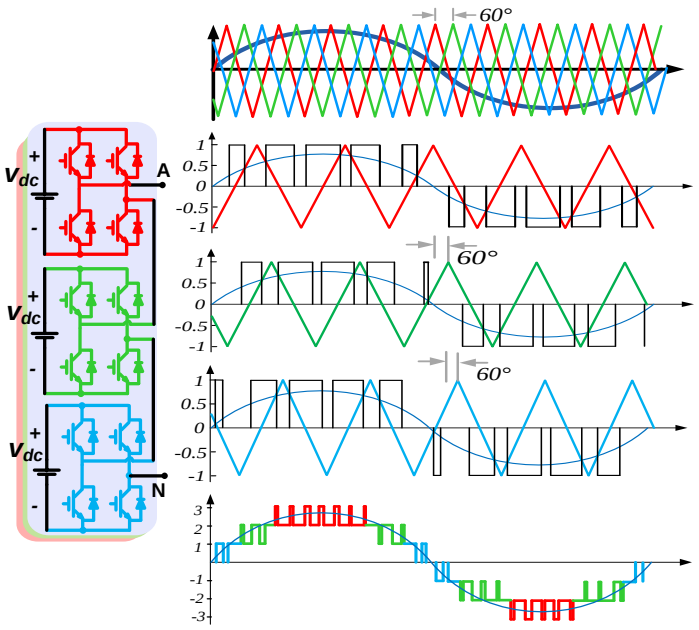
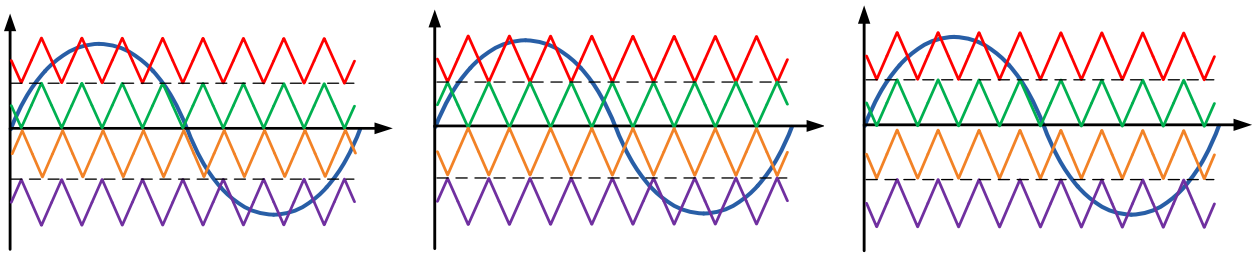


Fig. 1.15. High frequency phase shift modulation

Another carrier based method is the level shifted modulation. The carrier waves shift their level with respect to the reference wave. There are three types of level shifting schemes as shown in Fig.1.16. For the phase opposite disposition (POD) method in Fig.1.16(a), all the positive carriers are in phase with each other, so does the negative carriers. But the positive and negative



(a) Phase Opposite Disposition (POD)

(b) Alternative Phase Opposite Disposition (APOD)

(c) Phase Disposition (PD)

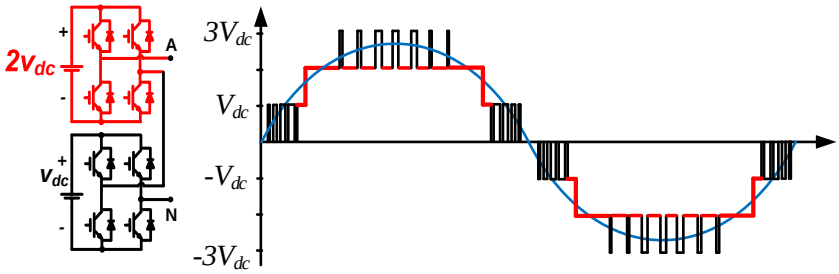
Fig. 1.16. Three high frequency level shift modulation methods

carriers are in phase opposite with each other. For the alternative phase opposite disposition (APOD) method in Fig.1.16(b), all the carriers are in phase opposite with each other. And for the phase disposition (PD) method in Fig.1.16(c), all the carriers are in the same phase. The issues for the level shift modulation can be clearly found from the figure. This method generates different switching frequency and switching pattern for each cell. The inner cells have lower switching frequency and switching loss than the outer cells. Also the switching pattern and loss distribution is influenced by the modulation index. This issue makes the level shift modulation undesirable for the modularized design. Also from THD point of view, the level shift modulation has higher THD than the phase shift (PS) modulation. And the THD for the three level shift methods are different. The THD comparison for all the carrier based high frequency modulation gives the following sequence for THD from low to high: PS<PD<APOD<POD. From the above analysis, it can be concluded that the level shift method is not as advantageous as the phase shift method for the cascaded topology. But it is often used on the NPC topology since it has intrinsic unbalanced loss and switching pattern for each device. Each carrier modulates one switch in the phase leg. It is a simple way to modulate one NPC phase leg compared with SVM method.

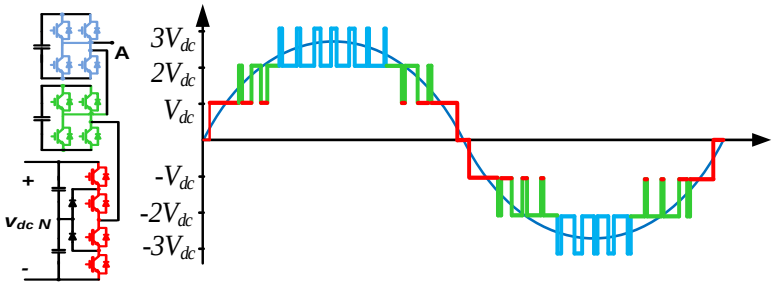
1.3.4 Carrier Based Mixed Frequency Modulation

The mixed frequency modulation, as its name indicates, is the mixture of low frequency and high frequency modulation [31]. The concept is to use different switching frequencies for

different cells in the system according to their voltage ratings. Therefore, it is suitable for the asymmetrical and hybrid multilevel topologies. Fig.1.17 gives the illustration of mixed frequency modulation for asymmetrical CHB and hybrid NPC+CHB circuit. For the asymmetrical CHB with 2 cells in Fig.1.17(a), the top cell with higher DC link voltage is switched at low frequency to reduce the switching loss. The bottom module with lower DC voltage is doing high frequency switching to reduce the THD. With the mixed switching frequency, both the switching loss and the THD is considered. For the hybrid topology in Fig.1.17(b) with NPC plus CHB structure, the mixed frequency modulation can also be applied. The NPC phase leg can be modulated with low frequency, also to reduce loss. And the CHB part with floating DC voltage can be switched at high frequency to provide extra levels and to reduce the THD. Though the mixed frequency modulation is suitable for the asymmetrical topology as indicated by the two examples, it can be applied to symmetrical cascaded structure as well. Some cells can switch at low frequency for loss reduction. However, the mixed frequency modulation results in different loss distribution patterns for each cell and the system structure lost modularity.



(a) Mixed frequency modulation for asymmetrical CHB



(b) Mixed frequency modulation for NPC+CHB

Fig. 1.17. Mixed frequency modulation for cascaded and hybrid topology

1.4 Research Motivations, Objectives and Challenges

In this part, the potential applications and research motivation is introduced at first. Then the research objectives and goals are identified with possible challenges discussed.

1.4.1 Research Application

To encourage the high penetration of renewable energy and to reform the power grid infrastructure, the concept of renewable energy micro grid is proposed. There are several motivations for this concept. The first one is to reduce the energy consumption from traditional grid powered by fossil fuels. The second one is to fully utilize the renewable energy with the help of energy storage. The third one is to achieve the high efficiency and high performance power conversion with minimized size and weight for various electric loads. The last one is to simplify the power system structure and to increase the system stability and reliability. Fig.1.18 shows a demonstration of the future renewable energy micro grid structure. A residential house with renewable energy, energy storage, plug in electrical vehicle and home electronic appliance

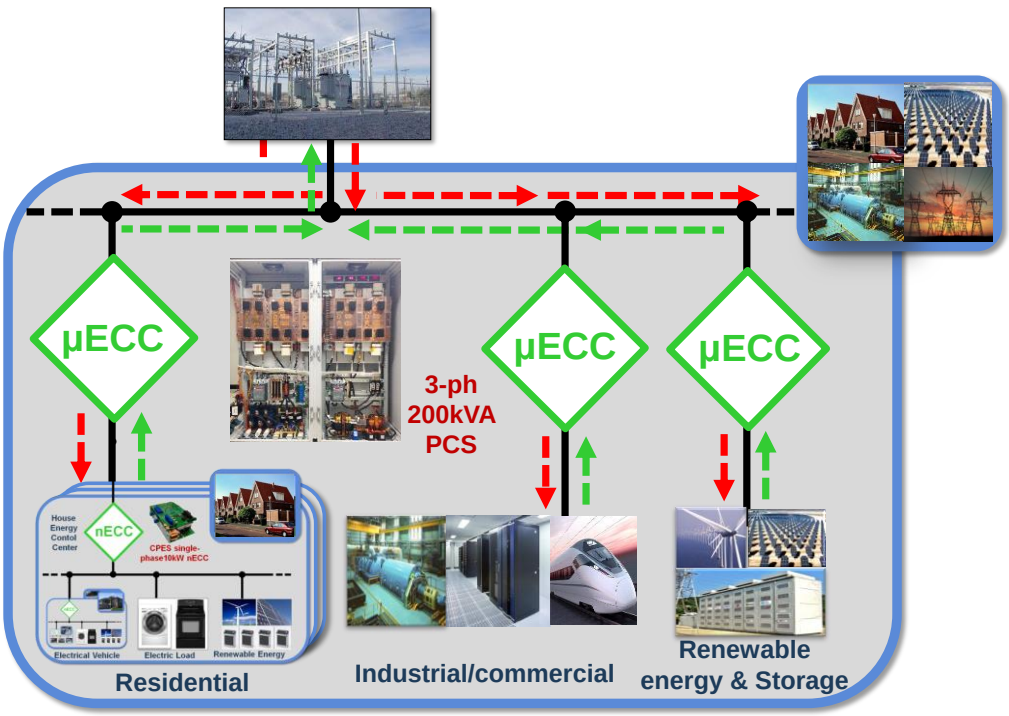


Fig. 1.18. Concept of renewable energy micro grid system

forms the basic frame of nano-grid as shown in the bottom left corner of Fig.1.18. The power conversion system (PCS) plays the key role in such a system. It serves as the energy control center that dispatches the power flow and balance the power consumption. It also provides a bidirectional interface between the conventional utility grid and the house nano-grid. The concept of renewable energy DC nano-grid is well established in [32]. And the hardware prototype of 10kW single phase nECC is developed.

The nano-grid structure can be further extended to a higher power and voltage level with large scale of renewable energy, numerous industrial and commercial loads and high power utility grid. For such a system, a bidirectional power conversion system is still needed as grid interface. The PCS for a micro energy control center (μECC) is the research objective. It can be used in many applications like grid interface for renewable energy or energy storage, power supply for industrial or commercial loads. Also it can work as conditioner or compensator for power system control. For most of the applications listed, a bidirectional power flow with four-quadrant operation is required. Fig.1.18 provides an illustration of how the μECC work in the future grid at both power generation side and power consumption side. The ultimate goal for the future grid is to replace the bulky line frequency transformer in the substation with the power conversion system with smaller size, higher efficiency and better performance.

1.4.2 Research Motivations

The research target is the 3-level NPC topology. Although this topology has been studied for decades, there are several reasons for choosing it as target. First of all, the 3-level NPC is the basic multilevel building block that can be extended to higher power and voltage level. As shown in Fig.1.10(b), the 3-level phase leg can be used as the basic cell for cascaded configuration. Also for the circuit in Fig.1.10(c) the 5-level topology is based on the basic 3-level NPC

topology. In addition, the 3-level phase leg has many topological variations such as DNPC, ANPC, FC, and T-type as shown in Fig.1.5. The research on 3-level topology has some generality and broad applications. At last, the 3-level NPC topology is not as complex as the 5-level or higher level NPC circuit, which has significantly large number of device and high cost. More importantly, some intrinsic issues for NPC like neutral point balance and uneven loss and stress becomes serious problem for 5 level. While for the 3-level topology, they are still achievable and are potential research points. All these reasons justify the research motivation.

The 3-level NPC topology is widely used by numerous industrial products in various applications like renewable energy, power quality control, industrial drive and power supply. Basically all the major high power converter providers like GE, ABB and Siemens have 3-level NPC products. The power rating ranges from hundreds kilowatt to megawatt. But the switching frequency for the state of the art products stays at around several kilo hertz and the efficiency is below 98%. The research motivation is to take advantage of new generation IGBT device, ANPC topology and new modulation scheme to push the switching frequency to IGBT limits as well as to achieve high efficiency and reduced stress.

1.4.3 Research Objectives

This dissertation focuses on a 3-level NPC power conversion system with 200kVA power rating and bidirectional power flow. The AC side of the PCS is connected to 480V/600V three-phase utility grid. The DC side can accept a wide range of voltage input from 400V to 800V. With the given AC side voltage, the DC link voltage for the converter is set to 1200V with enough operation margin. To block the high voltage DC link, 1200V insulated gate bipolar transistor (IGBT) device is used. The IGBT device in this rating is the most ordinary device with low price. To accommodate sources and loads with a wide range of voltage at DC side, and also

to have better control flexibility, the power conversion system adopts a 2-stage system architecture. A 3-level DC/DC chopper is also included as the DC stage besides the 3-level 3-phase DC/AC converter. With this setup, the whole system can follow a modularized design approach. The 3-level NPC phase leg is the basic building block for the whole system, which standardize the structure and also ensures the scalability and modularity for the whole system. With those constrains and specifications, the system structure for the 3-level NPC power conversion system for renewable energy and micro-grid is shown in Fig.1.19. The system contains 2 stages, both of which are constructed by the modularized 3-level phase leg building block. The 2 stages share the same DC bus for positive, negative and neutral rail. The AC side is tied to the utility grid by the LCL filter. The DC/DC chopper is connected to the DC bus by a specially designed coupled inductor. The detail of the power stage design and parameters will be covered in detail in the later chapters. The objective is to design a general purpose bidirectional PCS. Its applications include grid interface converter for renewable energy, charger/discharger for energy storage system, power supply for DC load like data center and power supply for AC load like motor drive. It can also support the utility grid as a reactive power compensator or dynamic voltage regulator. Besides all the topological and structural requirement, there are also

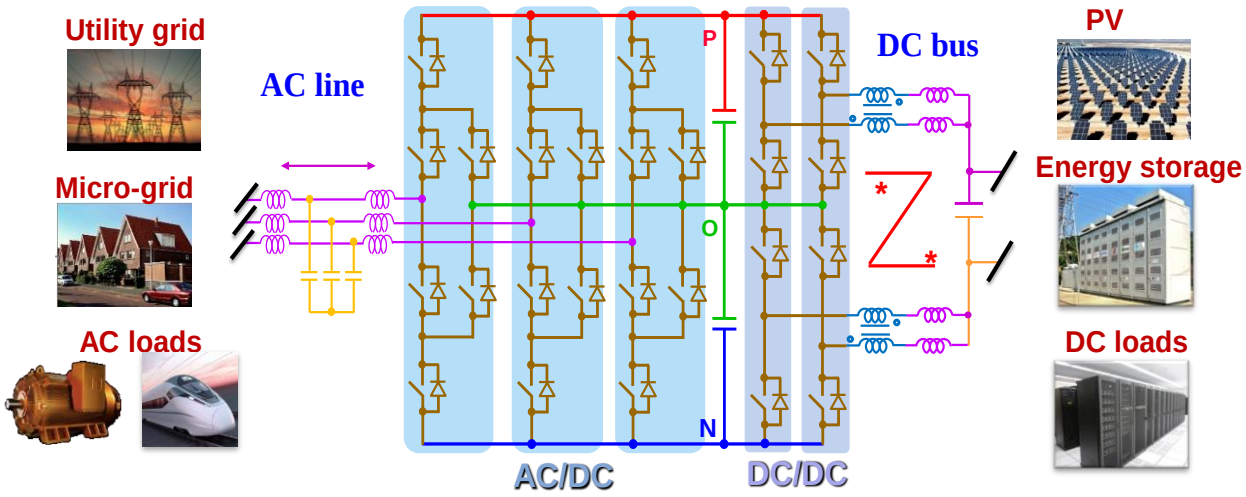


Fig. 1.19. System structure for 3-level NPC power conversion system

some other criterions to judge the performance of the PCS. In order to compete with the state of the art benchmark, this PCS should have several key features like high efficiency, high power density, high reliability and good power quality. The efficiency for such a system is targeting at 98.5% at different operating points with the bidirectional power flow at 200kVA and 20 kHz.

1.4.4 Research Challenges

The design and implementation for such a versatile PCS with general purpose and high performance may face several theoretical and practical challenges. Some challenges are universal for all power converter design, some are exclusively for the specific topology of 3-level NPC. It is just these challenges that provide some research opportunities. For this reason, the potential challenges and possible research opportunities are briefly discussed in the following.

One major common challenge for the high power high frequency converter is the contradictory design objectives. To achieve high power density, the switching frequency should be pushed high enough to shrink the passive component size. However the high switching frequency causes excessive switching loss which compromise the efficiency. To reduce the switching loss, the devices are usually driven at fast speed, which causes high voltage stress due to the dv/dt and di/dt. The stress influence the system reliability while the large dv/dt generates EMI issue and influences the power quality. As a result, there are many trade-off to be considered between various objectives. Also the intrinsic problems of the 3-level NPC converter should be dealt with. The major design challenges for the high power high frequency 3-level NPC power conversion system is listed below. It is also the major research opportunities and research points for this dissertation:

1. Commutation loops for the 3-level NPC phase leg varies with operating conditions.

2. Special switching transient with higher stress and loss exclusively for 3-level NPC commutation loop at high switching speed case.
3. Unevenly distributed device loss and stress on the 3-level phase leg over a line cycle.
4. The device loss and stress distribution pattern varies with the operating conditions and the patterns need to be quantified.
5. The neutral point voltage for the 3-level NPC converter has intrinsic line cycle ripple and the voltage needs to be balanced.
6. The neutral point balancing result is largely influenced by the power factor of the converter. Low power factor cases has intrinsically large voltage ripple.
7. The system total loss is influenced by the neutral point voltage balance control and results in different system efficiency at different power factors. The quantitative analysis for the loss and NP voltage ripple trade-off is not clear.
8. There are numerous modulation strategies for the 3-level NPC converter. The trade-off between the different modulation methods needs to be quantified in terms of system loss, neutral point voltage ripple and EMI spectrum.
9. The grid interface filter design should consider the trade-off between the grid attenuation requirement, the converter current ripple and loss, and also the inductor size and volume.
10. The inductor for the interleaved DC/DC chopper stage should consider both power density and the ability to suppress the circulating current within phase legs.

1.5 Dissertation Outlines

In chapter 1, a thorough survey and literature review of the multilevel converter topology and modulation techniques is given. The advantages and disadvantages for different topologies and modulation strategies are compared. The typical applications are also introduced. The

applications and motivations for the research are discussed then. The last part of this chapter identifies the research objective and challenges.

In chapter 2, the design of the high power high frequency 3-level NPC phase leg building block is carried out. Operating modes and switching loops for the phase leg are identified. Switching characteristics at different load current cases for each loop is evaluated. Various parameters are taken into consideration as the influential factors to the switching loss and stress. An in-depth analysis of some special switching transients is also given. A detailed loss model is built based on the tests to calculate the system loss distribution and the loss breakdown under different operating conditions. The phase leg loss and stress distribution for different modulation schemes under different operating points are evaluated and compared based on the loss model and the test result. The total system loss at different power factor cases are also calculated. The phase leg is tested at full power rating to verify the design objective.

Chapter 3 investigates the SVM modulation for the 3-level NPC converter. Various control objectives with SVM like loss reduction, neutral point (NP) balance and noise reduction are evaluated. A quantitative analysis for loss and NP voltage ripple is given for the various SVM and discontinuous PWM (DPWM) methods. An improved SVM modulation is proposed to reduce the NP imbalance and the switching loss simultaneously. The proposed method considers both the NP charge and the pulse sequence so that the minimized NP ripple and switching events is guaranteed in each switching cycle. In addition, the switching events between switching cycles are also considered to reduce the total switching loss. This method ensures an evenly distributed device loss and also a constant system efficiency under different power factors. Finally, the dead-time compensation method for the 3-level NPC converter with SVM modulation is introduced. The principle is analyzed and the result is verified by both simulation and experimental result.

In chapter 4, a new modulation scheme with new switching states and new commutation loops is proposes for the 3-level ANPC phase leg. With this new switching states, the conduction loss is largely reduced. Moreover, the new commutation loops have smaller switching stress and a better loss/stress distribution for each switch on the phase leg. In addition, the proposed modulation needs less PWM comparators per phase compared with the conventional modulation. The simple gate signal logic can be applied to any SPWM or SVM modulation strategy. Switching waveforms by double pulse tests show the improved switching characteristics under different load current cases. Also the system loss breakdown and the phase leg loss distribution analysis shows the loss reduction and redistribution result.

In chapter 5, the harmonic filter for the 3-level NPC grid interface converter is designed to achieve good filtering performance and small component size. Several different filter topologies are compared and the LCL structure is selected. The design of the inverter side inductor L1 is elaborated in great detail. The inductor current ripple analysis is given based on the SVM method in chapter 3. The analysis derives the inductor volt-second and the maximum current ripple equation in line cycle. It also reveals the switching cycle current ripple distribution over a line cycle, with the consideration of power factor. The total system loss is calculated with different ripple current. Inductance for L1 is determined by the loss and size tradeoff. Also the capacitor and grid side inductor L2 is designed based on the attenuation requirement imposed by grid code. Different damping circuits for LCL filter are compared and investigated in detail. The damping circuit with minimum loss and best damping performance is selected to help the filter and control loop design.

In chapter 6, the modeling and control for the 3-level 3-phase DC/AC converter is discussed. First, different control algorithms for the grid interface converter in a micro-grid system are

introduced and compared. The system level control algorithm for the whole power conversion system is identified. The switching model and average model for the DC/AC converter in both ABC and d-q coordinates are established. The modeling result is verified by transfer function measurement on the real converter hardware. The AC current control loop and DC link voltage control loop is designed based on the modeling and measurement result. The controller design is verified by both simulation and hardware experiment. The time domain transient response and frequency domain loop gain is measured to verify the design. Finally in this chapter, the input and output impedance for the 3-level NPC converter is discussed. The impedance with open loop and closed-loop control is compared for rectifier mode and inverter mode. The system stability and sub-system interaction for the 2-stage power conversion system is also investigated.

In chapter 7, the interleaved 3-level DC/DC chopper stage is introduced with the focus on the inductor current ripple analysis and coupled inductor design. The different interleaving methods are first presented with the related inductor current ripple and output current ripple analyzed. Then the coupled inductor is adopted on the interleaved chopper stage to suppress the circulating current within phase legs. The analytical expression of the inductor and output current ripple for different interleaving methods are derived. Finally, an integrated coupled inductor design is proposed with 3-dimensional flux path. It can reduce both the inductor and output current ripple as well as shrink the volume of the magnetic component. Detailed design and analysis is given in this chapter and the interleaved DC/DC chopper with integrated coupled inductor is verified by both simulation and experiment result. It worth mentioning that some part of the work in this chapter is done in collaboration with Mr. Sizhao Lu from Tsinghua University, who was a visiting scholar at CPES, and with Dr. Mingkai Mu, who is the research scientist at CPES.

In chapter 8, the hardware structure and the implementation for the 3-level NPC power conversion system is given. The system structure and the components for the DC/AC and DC/DC part are thoroughly introduced. The architecture of the digital control system is introduced in this part as well. The whole system is tested at different operating modes to verify its functionality.

Finally in chapter 9, the future work is introduced and the conclusions of the research in this dissertation are given.

CHAPTER.2 SWITCHING PERFORMANCE CHARACTERIZATION FOR 3-LEVEL NPC PHASE LEG

In most high power industrial applications where NPC topology is used, the switching frequency stays at several kHz or even lower. But for the 200kVA PCS, the high power density, high efficiency and good power quality is required as key design objectives. So the switching frequency needs to be pushed high enough to reduce the filter size, lower the THD and increase the control bandwidth. The target switching frequency is 20 kHz and the target efficiency is above 98%. For such a high efficiency phase leg with high power rating and high switching frequency, the power stage and driving circuit need to be carefully designed. Switching characteristics should be thoroughly investigated and switching performance should be optimized. Previous literatures discuss the influence of parasitic on the switching performance. But they only focus on low power DC/DC converter [1], [2], 2-level converter [3]-[5] and for converter with MOSFET device [6]-[8]. The switching performance and loop parasitic for a 3-level NPC phase leg has never been discussed in detail. Also very few literatures mentioned the different switching modes for NPC circuit [9]-[11] and no one investigates the influence of switching mode on the switching performance like stress and loss.

In this chapter, the aforementioned issues are discussed in detail in order to characterize and optimize the switching performance for the high power phase leg building block. A detailed design for the phase leg power stage and driving circuit is given. The IGBT device is selected based on system simulation. Different switching modes and switching loops for the 3-level NPC phase leg under various operating conditions are categorized with their features introduced. Based on the phase leg double pulse tests, the turn on and turn off performance for all switching modes is evaluated and optimized considering the loss and stress. Many factors like loop

inductance, gate resistance and load current are taken into consideration and their impact on switching characteristics is analyzed. Some special switching performance exclusively for the 3-level NPC topology are observed and discussed in detail. Based on the experimental results, guidance for the gate resistor selection is given. A system loss model is also built for accurate loss calculation. The system loss breakdown reveals different efficiency for different NPC switching modes under different system operating modes. The result shows new benefits brought by the ANPC topology, which helps the loss and stress reduction under certain operating modes.

2.1 Phase Leg Building Block Design Considerations

The 3-level NPC phase leg building block is the key component for the power conversion system. Its power stage, cooling system and driving circuit are carefully designed by the modularized approach to fit the special case of high power and high frequency application.

2.1.1 Switching Device Selection

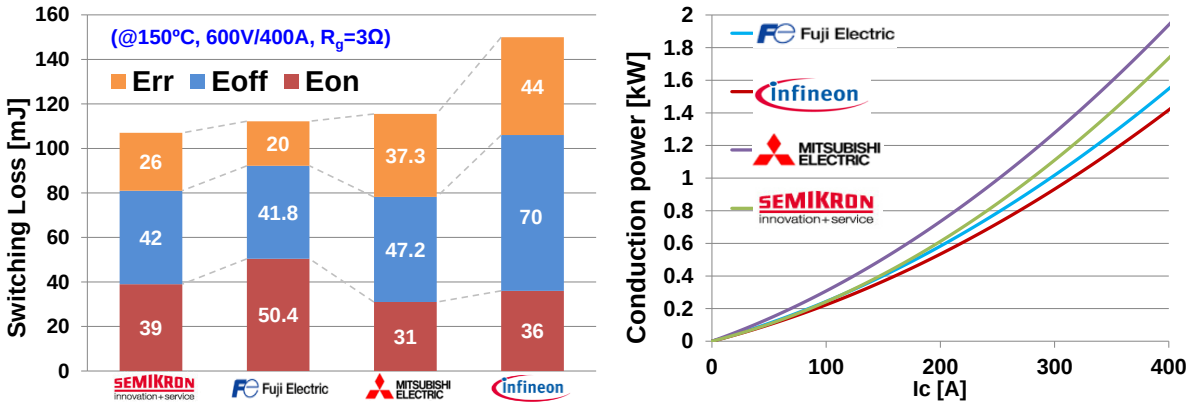
For the 200kVA power converter, each phase leg takes 67kVA power. To connect it to 480V AC grid, the phase leg current rating is 240A. Considering such current rating and also the 1200V DC link voltage, the 1200V/400A single IGBT module is used as switching device. Four commercial products at this rating with the same package and footprint are selected as candidates. The manufacturer and device model is listed in Table.2.1. It also gives the key parameters comparison like switching energy and conduction loss at 600V/400A switching condition.

Table 2.1. IGBT device candidate comparison

Manufacturer	Semikron	Mitsubishi	Fuji	Infineon
Device model	SKM400GA12V	CM400HA-24H	1MBI400V-120	FZ400R12KP4
E_{on}/mJ	26	31	50.4	36
E_{off}/mJ	42	47.2	41.8	70
E_{rr}/mJ	39	37.3	20	44

V_{on}/V	0.7	0.91	/	0.795
R_{on}/Ω	0.0038	0.0029	/	0.0028

In order to select a device with the lowest total loss for high efficiency, the switching energy and conduction loss are also compared based on the data sheet. The result in Fig.2.1 shows that the device with the smallest switching energy at rated voltage and current has larger conduction loss under all current condition. The system loss is influenced by both load current and switching



(a) Switching energy comparison (b) Conduction loss comparison

Fig. 2.1. Loss comparison for candidate devices based on datasheet

frequency. So the datasheet comparison itself doesn't help the device selection. As a result, the simulation model of the power conversion system is built for system loss calculation. Based on the switching energy and conduction loss information provided by device datasheets, the total loss over a whole line cycle can be calculated. The calculation also needs the information of the converter phase current and gate signals from simulation. The switching cycle energy under different current conditions is integrated over a line cycle to have the total loss. The 3-phase inverter is simulated with rated power and frequency (200kVA/20kHz). The result in Fig.2.2 gives the system total loss breakdown comparison for all the candidate devices. For the high power high frequency application, the IGBT with the smallest switching energy is preferable because of the switching loss takes a large percentage in the total loss. But for other scenarios like low frequency and high current condition, low conduction loss device may give the smallest total loss. Different operating conditions like temperature and power factor are considered and

the system total loss is not influenced much. For the high frequency phase leg design, the IGBT from Semikron is selected based on the loss breakdown information. This device can ensure an estimated 98% power stage efficiency.

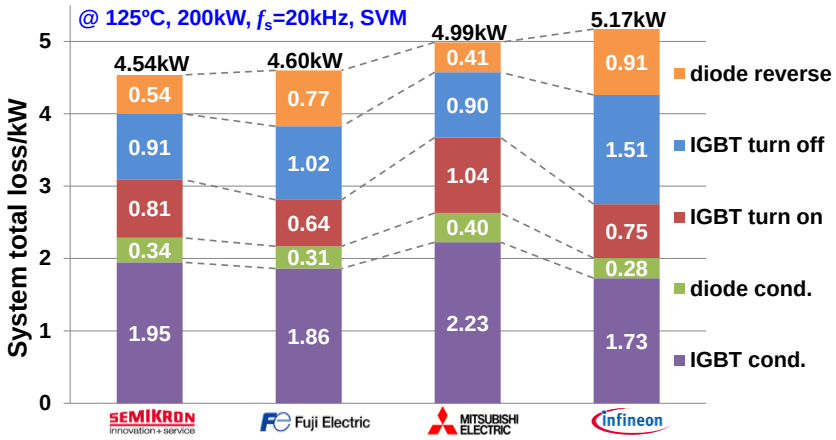
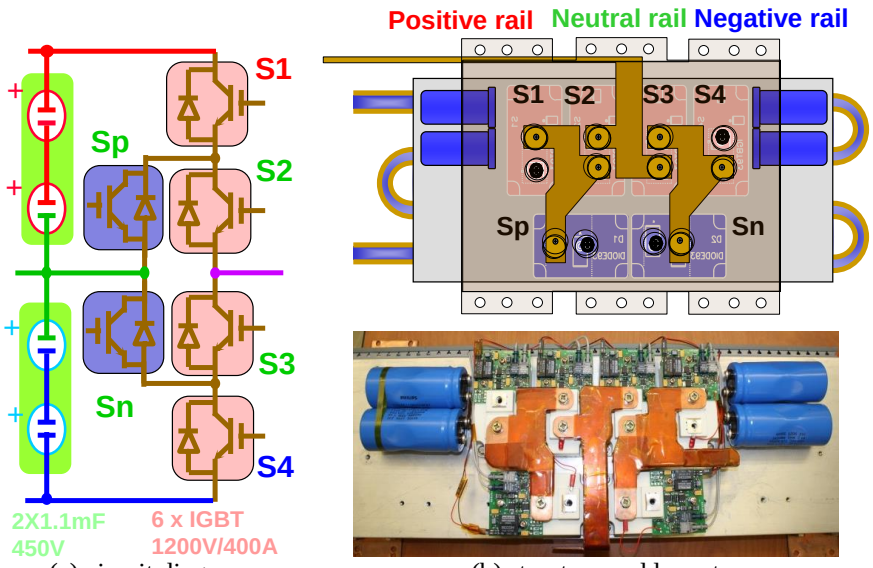


Fig. 2.2. System total loss breakdown comparison for candidate IGBT devices

2.1.2 Phase Leg Structure and Layout

Base on the selected device footprint, the structure and physical layout of the NPC phase leg building block is carefully designed as shown in Fig.2.3. This is the modularized building block for the whole system. To better support the DC link voltage and to mitigate the influence of loop parasitic, the DC link capacitors are evenly distributed on each phase leg between positive-neutral rail and also neutral-negative rail. Certain measures are taken to minimize the total loop parasitic inductance due to the high switching frequency. The main switches and clamping switches are connected with specifically designed copper bar to reduce the parasitics. Laminated bus bars are also adopted as positive, negative and neutral rail to provide low impedance and low parasitic current path. There are three layers of bus bar. The positive bus is connected to the collector of S1 as well as to the positive bus of other phase legs. So does the negative bus which is connected to the emitter of S4. The neutral bus is connected to the two clamping switches. The decoupling capacitors are mounted very close to the IGBT modules for parasitic inductance

cancellation. The position of each device and the layout of the whole phase leg are designed to be compact in order to shrink the power stage size.



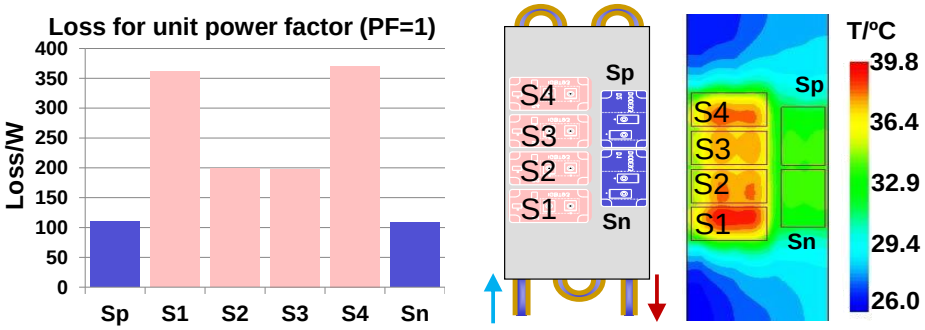
(a) circuit diagram (b) structure and layout

Fig. 2.3. Structure and physical layout of 3-level NPC phase leg building block

2.1.3 Cooling System Structure and Layout

For this high power high frequency phase leg, the total loss as low as 2% means several kW power. So the water cooling system is used to dissipate the large amount of heat. The devices are mounted on the cold plate with water pipe connected to a heat exchanger. The structure and layout of the heat sink can be found in Fig.2.3(b). The loss distribution on the phase leg under rated power and unit power factor is simulated using the aforementioned simulation model and the result is shown in Fig.2.4(a). The loss distribution for each device in this figure verifies the unevenly distributed loss for NPC phase leg mentioned in previous chapter. Based on the loss distribution, a thermal simulation for the temperature distribution on the phase leg is done by the finite element analysis (FEA) software. The cold plate dimension and device placement are pre-determined. The thermal resistance between device junction and case can also be obtained from device datasheet. By adjusting the liquid temperature, pressure and flow speed, the case and

junction temperature can be controlled. At an ambient temperature of 25ºC, the highest case and junction temperature are 39.8ºC and 60ºC respectively. The phase leg thermal distribution is shown in Fig.2.4(b) It is verified by the full power phase leg test introduced later in this chapter.



(a) Phase leg loss distribution (b) Phase leg thermal distribution

Fig. 2.4. Phase leg loss and thermal distribution at rated power

2.1.4 Gate Drive Circuit Design for IGBT

With the given operating condition, the device should be able to switch high current at high frequency, which requires meticulous design of the gate driver. Many aspects of the driving conditions should also be considered because it is one of the dominant factors that determine the switching performance like loss and stress. There are many driving solutions for IGBT. The device providers have recommended driver board associated with the devices. The hybrid gate driver IC has strong driving capability and complete protection functions. But in order to accommodate the bus bars covered on top of the phase leg building block, the gate driver should keep low profile and small size. As a result, the customized design is needed and only small gate drive IC meets the size requirement. So the MC-33153 driver IC for single IGBT module is used. It has small size and full protection functions for device over current and under voltage fault.

The gate voltage threshold of the selected IGBT module is ±20V. To ensure the fully turn-on and to leave some margin for possible gate voltage ringing and overshoot, the turn on voltage is set to +15V. This is also the recommended turn on voltage by the datasheet. The turn off gate

voltage is set to -5V to guarantee fully turn-off for the device and also to consider the total gate voltage applied on the driver IC. The +15V and -5V gate voltage is provided by two separate DC power supplies with 12V input and isolated power stage to avoid noise interference. Because the driver IC itself can't provide sufficient gate charge current to turn on and turn off the device, a current boost circuit is therefore required. Here a push-pull current booster with PNP and NPN transistor is used. The peak gate current can be calculated as:

$$I_{peak} \approx \frac{\Delta V}{R_g + R_{g\_in}} = \frac{V_{g\_on} + \left|V_{g\_off}\right|}{R_g + R_{g\_in}} = \frac{15 + \left|-5\right|}{2 + 0.5} = 8A \tag{2-1}$$

where V_{g_on} and V_{g_off} are the turn on and turn off voltage. The R_g and R_{g_int} represents external and internal gate resistance. The internal gate resistance for the device is 2Ω and minimum external gate resistance is 0.5Ω for loss reduction. Therefore, the peak gate current is 8A. The MJD44/45H11 transistor is used as current boost transistor for the gate driver.

The switching frequency also influences the driver design because it is related to the power loss of the driver. The datasheet gives the turn on gate charge Q_{g_on} of 4417nC at 15V turn on voltage. And turn off gate charge Q_{g_off} is -780nC at -5V turn off voltage. The average current for the gate driver can be then calculated as

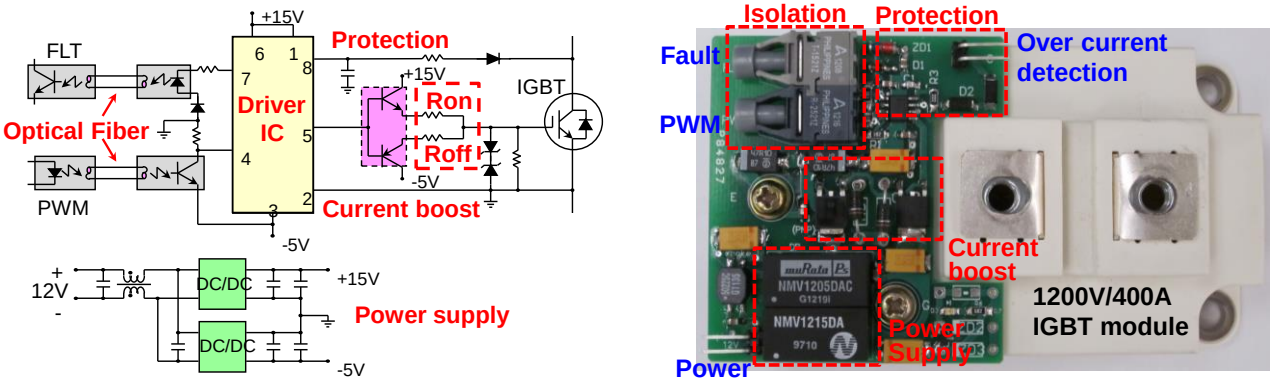
$$I_{avg} \approx \left(Q_{g\_on} - \left|Q_{g\_off}\right|\right) f_{sw} = 0.07A \tag{2-2}$$

Based on the 0.07A average current and 20 kHz switching frequency, the power dissipation of the gate driver can be calculated as

$$P_{drv} \approx I_{avg} \Delta V = Q_f \, f_{sw} \Delta V = 1.4W \tag{2-3}$$

The total power loss for the gate driver is 1.4W. The higher switching frequency is, the larger power required by the driver. In this design, two isolated power supplies with 2W power rating are used to support up to 30 kHz frequency and to provide +15V and -5V gate voltage. The power supply can provide up to 3kV isolation for the driving circuit.

The circuit diagram and physical layout of gate drive board is shown in Fig.2.5. The driver board is mounted on the IGBT module to minimize the driving loop and to avoid noise interference. It can be observed from Fig.2.5(b) that the gate drive board is quite compact and does not occupy extra space. The optical fiber is used to transmit the PWM signals. This practice provides highly isolated interface for the gate and fault signals, thereby enhance the noise immunity for the system. The most important feature is the separate configuration of the turn on and off gate resistor which enables the separate optimization for the turn on and turn off performance. The gate drive board design considers most of the research objectives. For high power density, it has small and compact size. For reliability requirement, it has good isolation for noise immunity and complete protection function. For high efficiency, the gate resistor for turn on and turn off can be separately configured to have the minimized loss.



(a) Gate drive circuit diagram (b) Gate drive board layout

Fig. 2.5. Structure and function block of gate drive board

2.2 Four-Quadrant Operation Modes for NPC Phase Leg

The power conversion system is designed to have bidirectional power flow with both active and reactive power. Therefore, the converter should be able to work as both inverter and rectifier. Fig.2.6 shows the phase leg output voltage and current waveforms under a four-quadrant operation mode with only inductive load. In the 1st quadrant, the phase leg has a positive output voltage and current while the 3rd quadrant is just the opposite. The PCS works at inverter mode

in these two quadrants. In 2nd and 4th quadrants, it works in the rectifier mode. In each quadrant, one of the six switches in the phase leg is triggered for high frequency switching. This switch and a freewheeling diode form a commutation pole in the specific quadrant. Depending on the different modulation schemes, there are three different switching modes for an NPC phase leg.

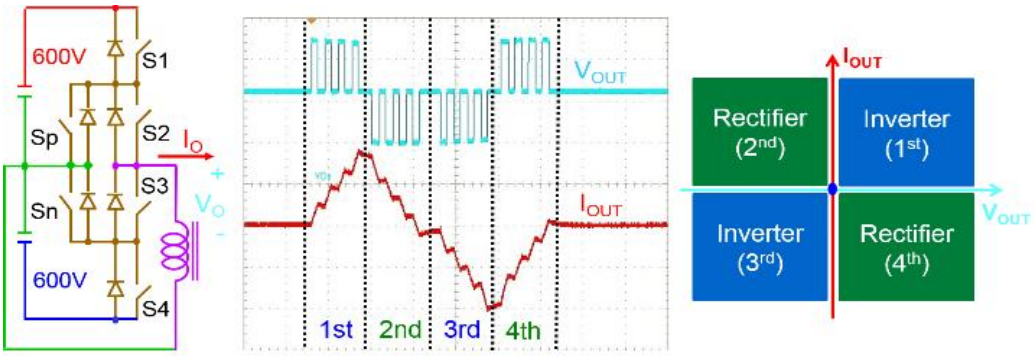


Fig. 2.6. Four-quadrant operation modes and waveform for NPC phase leg

2.2.1 Switching States and Modulation schemes for 3-level NPC Phase Leg

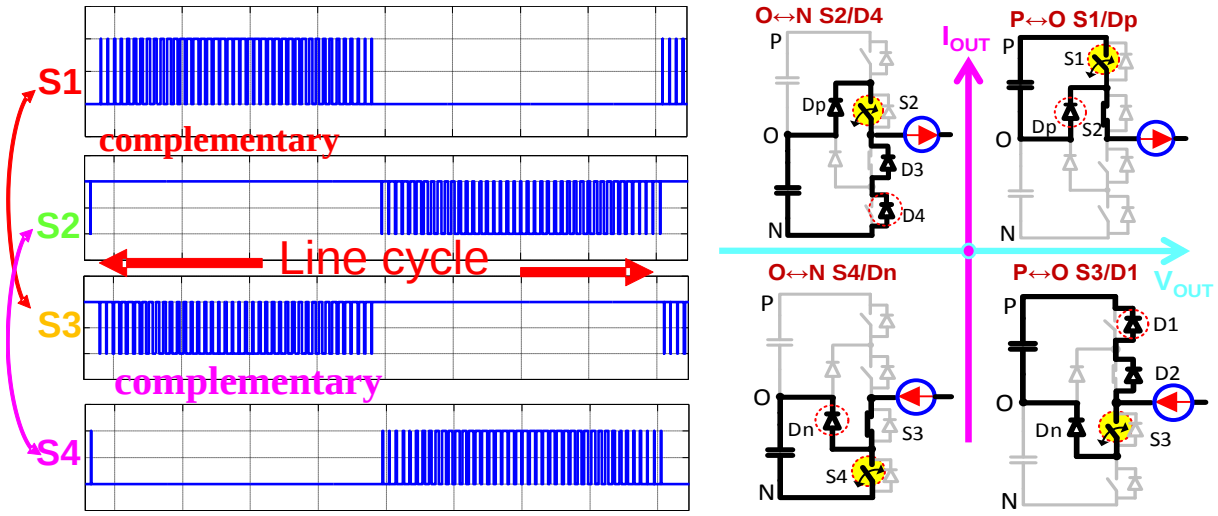
Even if the clamping devices for the NPC phase leg are active switches, it can be modulated to work as the DNPC phase leg when the two clamping switches are turn off constantly. For the DNPC phase leg, when the output is connected to positive rail, the top 2 switches S1 and S2 are on. For the negative state, the bottom 2 switches S3 and S4 are on. For the neutral state, since the load current direction determines the neutral current path, two inner switches S2 and S3 are on. Then the gate signal sequence is concluded in Table 2.2. The gate signals for all the switches in a

Table 2.2. Gate sequence for DNPC phase leg

	S1	S2	S3	S4
P	on	on	off	off
O	off	on	on	off
N	off	off	on	on

line cycle is shown in Fig.2.7(a). It clearly shows that the top outer switch S1 is switched in complementary with the bottom inner switch S3. The switches S2 and S4 follow the same manner. Each complementary switch pole has half line cycle in high frequency switching. With

this operating mode, the four quadrant switching loops are derived in Fig.2.7(b). For inverter mode (power factor=1) in 1st and 3rd quadrants, the outer switch commutates with the clamping diode. For rectifier mode (power factor= -1) in 2nd and 4th quadrants, the inner switch commutates with the outer diode. For the non-unity power factor cases, all the switches are involved in high frequency commutation.



(a) Gate signals (b) Switching loops

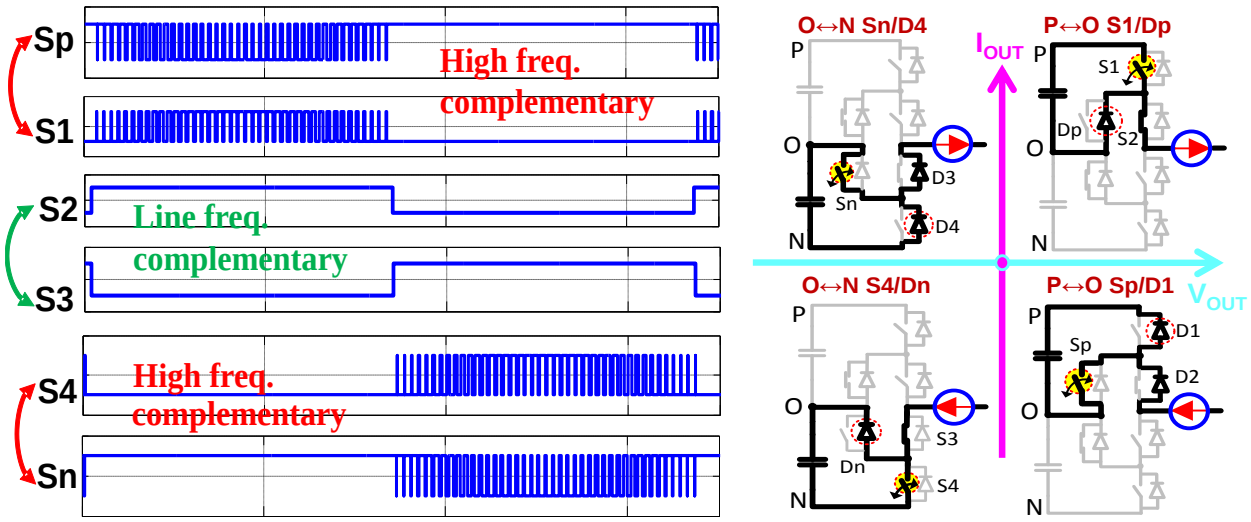
Fig. 2.7. Gate signals and switching loops for DNPC phase leg

For the ANPC phase leg, the neutral current path can be flexibly configured, which enables more variety in the modulation schemes. The neutral current can flow through either the upper path of Sp and S2, or the lower path of Sn and S3. One modulation scheme for ANPC uses only the outer and clamping switches for commutation. In the positive half line cycle when the output is switched between P and O with the top cell, the upper path is used. In the negative half cycle for the bottom cell, the lower path is used. The gate signal sequence in Table.2.3 shows the two

Table 2.3. Gate sequence for ANPC outer switch mode modulation

	Sp	S1	S2	S3	S4	Sn
P	off	on	on	off	off	on
O^+	on	off	on	off	off	on
O^-	on	off	off	on	off	on
N	on	off	off	on	on	off

neutral states O+ and O- are used for the positive and negative half line cycle separately. The line cycle gate signals in Fig.2.8(a) shows the complementary switch pair for this modulation scheme. The outer and clamping devices in the top cell have high switching frequency in complementary manner in the positive half line cycle. The bottom cell devices do the same for the negative half line cycle. The inner two switches are also complementary but with only line switching frequency. The switching loops in the four quadrants are concluded in Fig.2.8(b). In all the four



(a) Gate signals (b) Switching loops

Fig. 2.8. Gate signals and switching loops for ANPC outer switch mode modulation

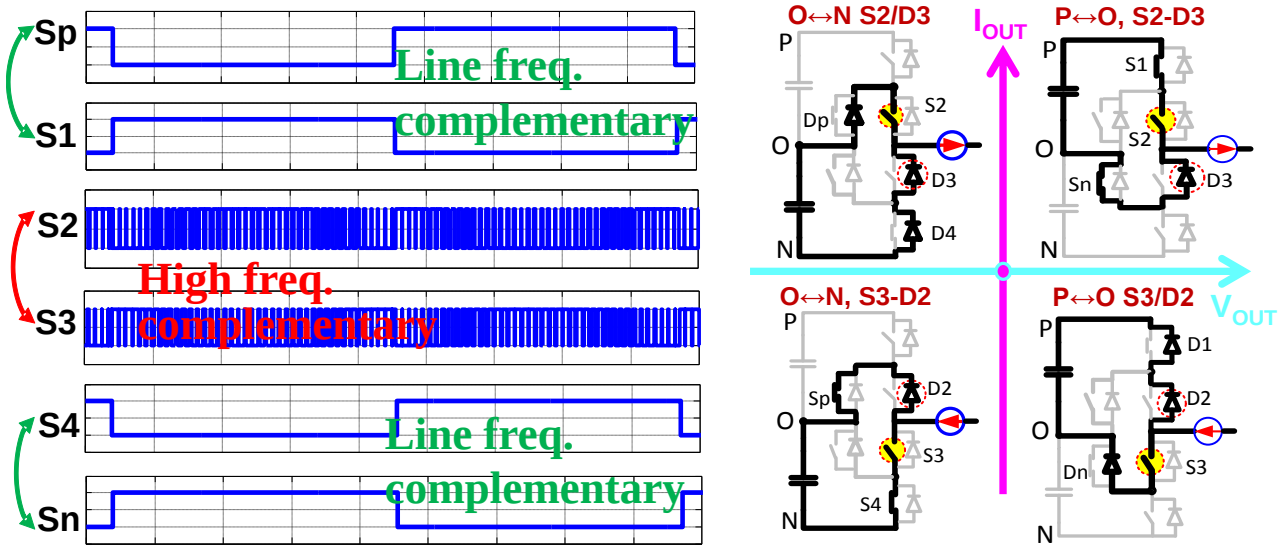
quadrants, the commutation happens between the outer and the clamping devices. As a result, the inner switches only bear conduction loss. The major switching loss is either on the outer switches or the clamping switches, depending on the power factor and operating modes.

Another modulation for ANPC phase leg uses the lower neutral path for the top cell commutation and the upper path for the bottom cell commutation. The gate sequence is given in Table.2.4. There are also two neutral states O- and O+, each one correspondents to half line cycle.

Table 2.4. Gate sequence for ANPC inner switch mode modulation

	Sp	S1	S2	S3	S4	Sn
P	off	on	on	off	off	on
O^-	off	on	off	on	off	on
O^+	on	off	on	off	on	off
N	on	off	off	on	on	off

From the gate signals waveform in Fig.2.9(a), three pairs of complementary switches can be found. The outer and clamping switches are complementary, but only at line switching frequency. On the contrary, the 2 complementary inner switches have high switching frequency over the whole line cycle. The switching loops in Fig.2.9(b) also shows this pattern. It should be noticed that all the outer and clamping switches are switched at line frequency. The switching loss only occurs on the inner switches regardless of the power factor and operating modes.



(a) Gate signals (b) Switching loops

Fig. 2.9. Gate signals and switching loops for ANPC inner switch mode modulation

2.2.2 Switching Loops for 3-level NPC Phase Leg

Comparing the three modulation schemes for the NPC phase leg, the symmetry and duality in the power loop can be noticed. From the switching device point of view, there are two types of switching loops, the long loop and the short loop. The short loop contains an outer switch and a neighboring clamping switch, for instance, S1 and Sp. One IGBT commutates with the anti-parallel diode of the other IGBT. For the long loop, one inner switch, say S2, is involved for high

frequency switching with the anti-parallel diode of either inner switch S3 or outer switch S4, depending on the modulation scheme used.

For DNPC operating mode, the phase leg is modulated with two pairs of complementary PWM signals. One pair includes S1 and S3, the other includes S2 and S4. The switching loop is not determined by the modulation, but by the phase current direction, in other word the power factor. For this reason, the DNPC switching loop is predetermined by the operating modes. On the contrary, the switching loops for ANPC phase leg can be selected by the modulation scheme regardless of the power factor. The ANPC has controllable neutral current path. If upper path is used for top cell and lower path is used for bottom cell, there will be only short loop engaged. Similarly, if upper path is used for bottom cell and lower path for top cell, only long loop is used. The different modulation schemes result in different commutation poles. The complementary gate signals and dead-time configurations also varies with the modulation schemes.

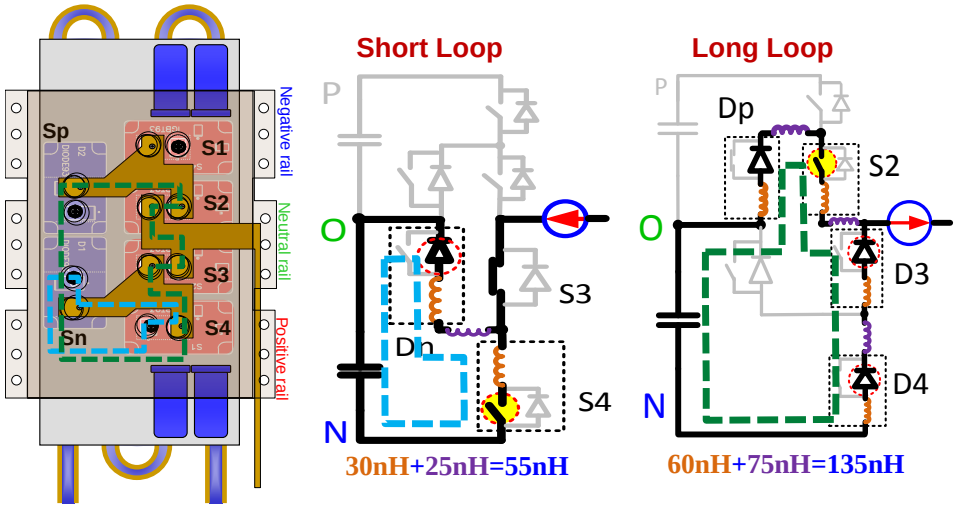


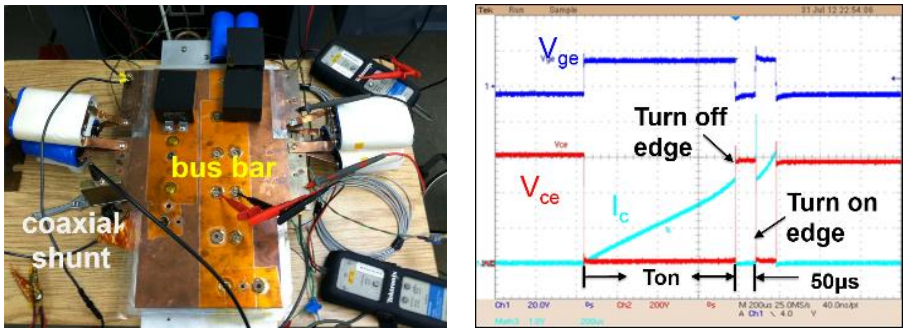
Fig. 2.10. Two different commutation loops for 3-level NPC phase leg

Considering the real phase leg layout shown in Fig.2.10, the difference for these two switching loops can be easily identified. The short switching loop includes 2 IGBT modules and 1 connection while the long loop has 4 modules and 3 connections. The parasitic inductance for

the IGBT module is about 15nH according to the datasheet and the copper bar connection has an estimated 25nH inductance by measurement. The total loop parasitic inductance for the long loop and the short loop can be calculated. The result shows that parasitic inductance for the long loop is two times larger than that of the short loop. This difference causes distinctive difference on switching characteristic. The switching performance like loss and stress should be optimized separately for these two switching loops. To investigate the different switching characteristics and to optimize the switching performance for the inner and outer switching loop, double pulse tests for both loops are conducted based on the rated phase leg parameters as shown in Table.2.5. The tests cover four different load current cases from very low current to the peak current. With such a wide range of load current, the switching performance over a line cycle can be evaluated.

Table 2.5. Double pulse test conditions

DC voltage	DC link cap.	Load inductance	Load current/A
1200V	2.5mF	0.3mH	40/120/230/340



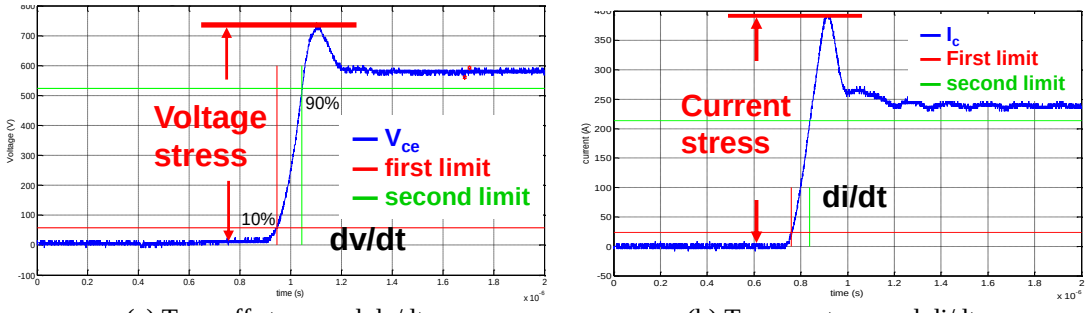
(a) Test circuit setup (b) Test waveform

Fig. 2.11. Double pulse test setup and testing waveform

The testing circuit shown in Fig.2.11(a) is built on the real phase leg hardware to keep the same layout and parasitic for the switching loop. A coaxial shunt is connected in serial in the loop to measure the IGBT current. This shunt has a very high bandwidth and low inductance, which ensures accuracy and avoids influence on the power loop structure. With such a tester, the tested waveform and characteristics represent the switching performance of the real 3-level NPC

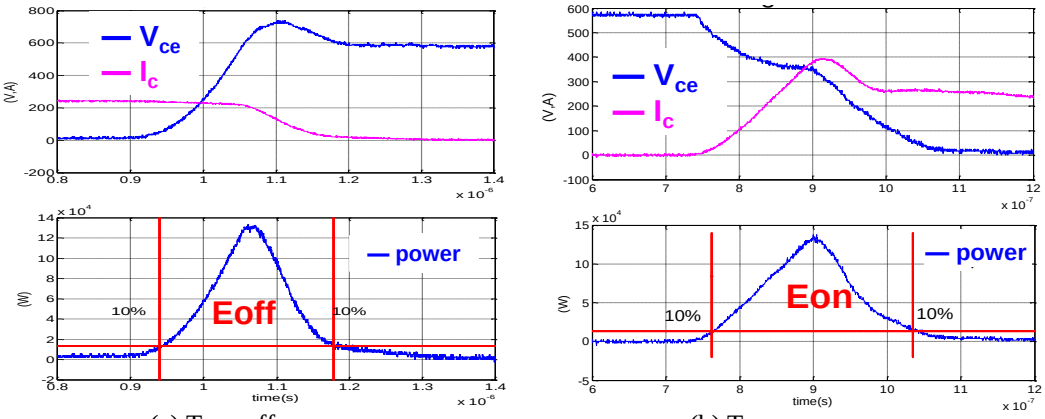
phase leg building block. Fig.2.11(b) shows the complete double pulse test waveform. The IGBT switch is first turned on to charge the inductor current to the rated value. Then it is turned off and on within a short time interval. The turn off and turn on edge is observed and evaluated. The device stress is measured and the switching energy, dv/dt and di/dt are calculated.

A typical turn on and turn off waveform in Fig.2.12 demonstrates the measurement of the switching stress. For the turn off transient in Fig.2.12(a), the turn off voltage peak is measured as the voltage stress. For the dv/dt calculation, the boundary is set from 10% of the steady state voltage to 90% of it. During this time interval, the voltage has a linear increase trend. The turn off loss is measured by multiplying the device voltage and current during the switching transient as shown in Fig.2.13(a). For the turn on stress and di/dt, the measurement and calculation follows the same rule as shown in Fig.2.12(b) and 2.13(b). The switching loss is integrated over the switching transient time to get the switching energy. The integration starts from 10% of the peak power and also ends at the same value. By doing so, some oscillation and reactive power transfer can be avoided at the beginning and ending of the switching transients.



(a) Turn off stress and dv/dt (b) Turn on stress and di/dt

Fig. 2.12. Switching stress measurement



(a) Turn off energy (b) Turn on energy

Fig. 2.13. Switching energy measurement

These key indices reflect the switching characteristics and are influenced by many factors like gate resistor and switching loops. The turn on and off performance is optimized based on the loss and stress tradeoff.

2.3 Switching Performance Evaluation and Characterization

2.3.1 Turn off Performance Evaluation

The turn off transients for long and short switching loops are first compared. The influence of gate resistance on the turn off performance is evaluated at first. Fig.2.14 shows the voltage stress, turn off loss, di/dt and dv/dt comparison for the two switching loops with different gate resistor

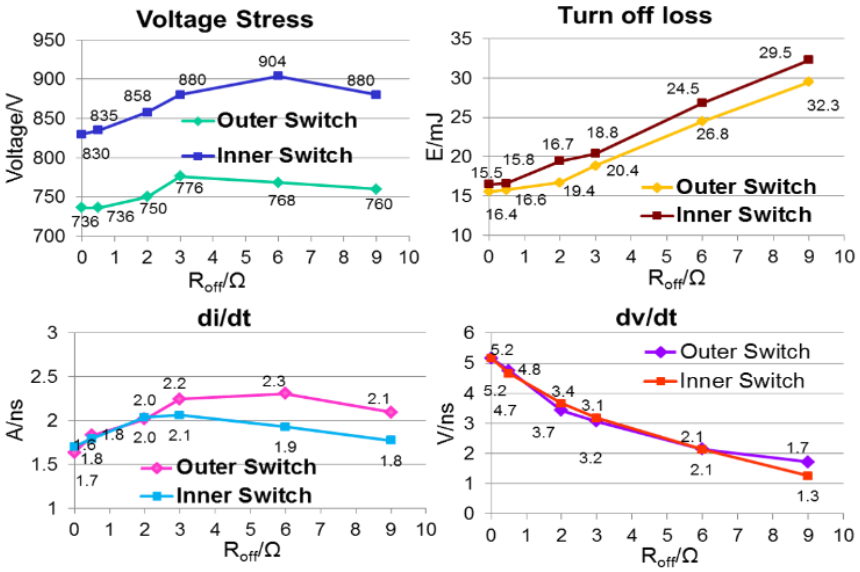
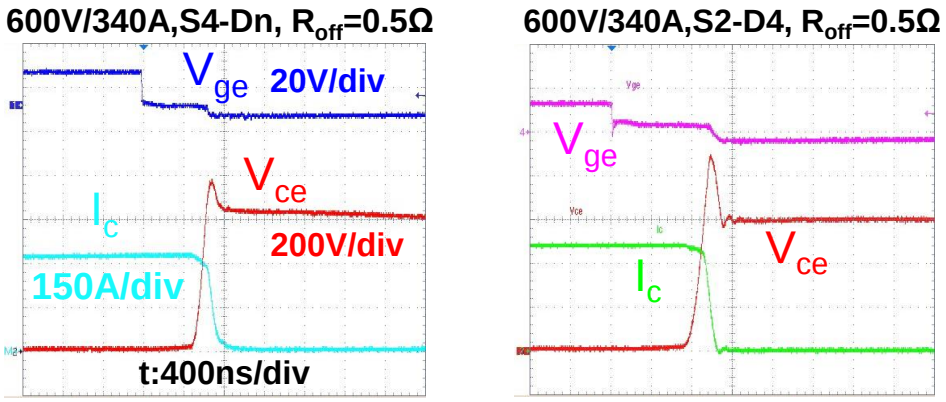


Fig. 2.14. Turn off characteristics with different turn off gate resistor

values. During turn off transient, di/dt of the falling current induces voltage on loop inductance and causes the voltage overshoot on the IGBT. For most IGBT modules, a small turn off resistor increases turns off speed and reduces turn off loss. But it inevitably causes a higher voltage spike because of the larger di/dt. However, the new generation of IGBT module used in this design has a nonlinear relationship between gate resistance and voltage spike. That is because of the carrier streaming effect [12] of the semiconductor device. The di/dt in the small gate resistor case can be reduced and voltage spike consequently decreases. This statement is verified by the nonlinear trend between turn off di/dt and gate resistor measured and shown in Fig.2.14. This special property is helpful for choosing the turn off gate resistor. No tradeoff between E_{off} and stress needs to be considered. The turn off resistor can be small for both loss and stress reduction.

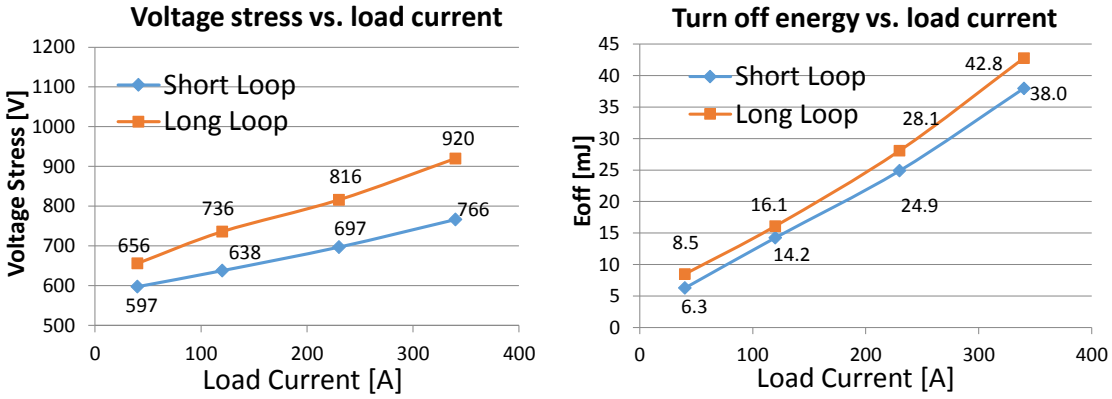
Comparing the turn off loss and stress for the inner and outer switch loop, it can be easily determined that the inner switch has higher stress and loss. This is because of the larger loop parasitic inductance and higher voltage drop on it. The larger loop parasitic inductance also helps to suppress the current falling rate and thus resulting in a smaller di/dt for the inner switch. The turn off dv/dt is not influenced much by the loop parasitic. So the slower current falling speed of the inner switch eventually increases turn off loss. The turn off waveform comparison for the short loop and long loop is given in Fig.2.15 with the 0.5Ω gate resistor and 340A turn off current. The waveform shows that the short loop has obviously smaller voltage stress compared with the long loop. Also the turn off characteristic is better. The same turn off resistor for inner and outer switch results in different loss and voltage stress. To provide enough margins, different turn off resistors should be applied to the inner and outer switch. The above waveform comparison clearly shows the significant difference of switching performance for the long and

short loop. The turn off characteristics like turn off energy and voltage stress for the two loops at different load current cases are also compared in Fig.2.16. It shows that the voltage stress and turn off energy for the long loop is larger than the short loop in all current conditions.



(a) Short loop (b) Long loop

Fig. 2.15. Turn off waveform comparison for two loops



(a) Turn off voltage stress (b) Turn off energy

Fig. 2.16. Turn off characteristics comparison for two loops

2.3.2 Turn on Performance Evaluation

For turn on transient, the same evaluation and characterization is also made. First, the impact of gate resistance on current stress, loss, dv/dt and di/dt is evaluated and the result is shown in Fig.2.17. A small gate resistor increases the changing speed of IGBT voltage and current. Thus, the turn on loss is reduced by smaller R_{on}. However, the fast turn on of IGBT also helps the diode sweep out the minority carrier and fasten the reverse recovery speed. The reverse recovery current flows through IGBT and causes a larger current spike under the small gate resistor case.

Compared with turn off performance, turn on gate resistor selection is not so straightforward because the tradeoff for loss and current stress should be considered. The same comparison for

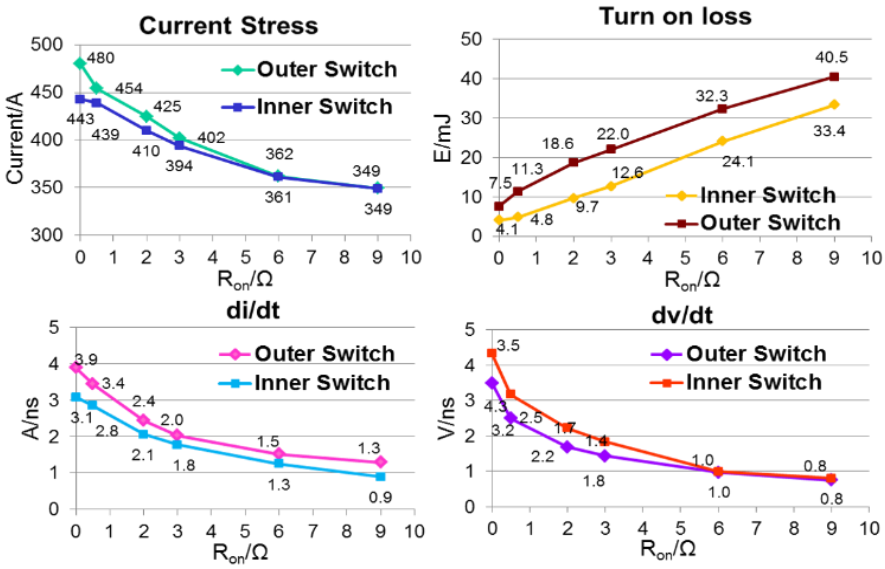
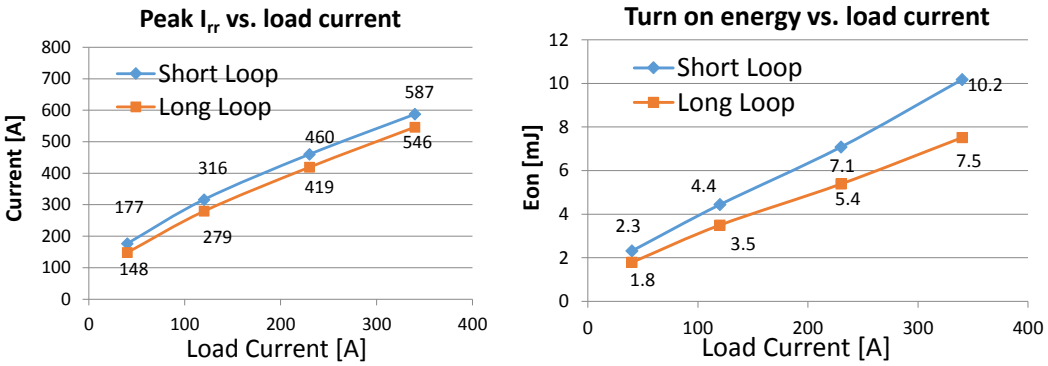


Fig. 2.17. Turn on characteristics with different turn on gate resistor

turn on characteristic under different load current conditions is given in Fig.2.18. For turn on transient, the reverse recovery current brings the major stress on the IGBT. Also it influence the turn on energy. The long loop with large parasitic inductance help the suppression of the current overshoot. In addition, the voltage drop induced on the loop parasitic also makes the IGBT voltage drop faster, resulting in a small intersection area of device voltage and current. The outcome is a smaller turn on energy. The turn on characteristics comparison in Fig.2.18 verifies that the long loop with larger parasitic has smaller turn on current stress and switching energy. From this point of view, the loop parasitic during turn on transient seems to play a positive role. Nevertheless, the double pulse tests reveal several problems for the long loop turn on with large parasitics, under both DNPC and ANPC mode. The following discussion gives reasons and influential factors for the observed problems.

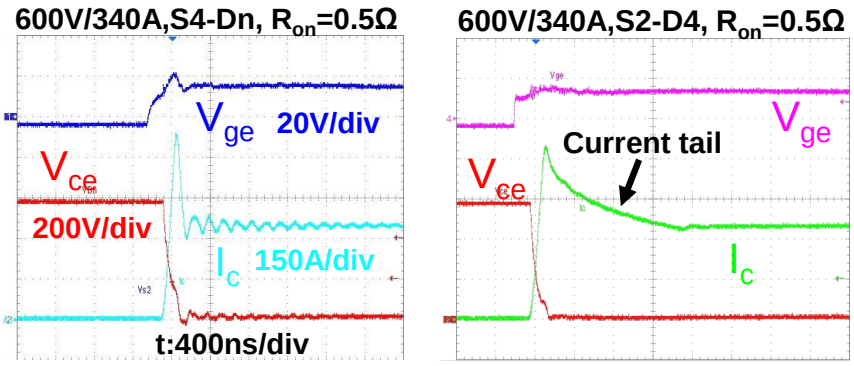


(a) Turn on current stress (b) Turn on energy

Fig. 2.18. Turn on characteristics comparison for two loops

2.3.3 Long Current Tail for Inner Switch Turn on

The turn on waveform for the short and long loop at DNPC mode is compared at first in Fig.2.19 The short loop has a typical IGBT turn on waveform in Fig.2.19(a) with current spike and oscillation caused by the diode reverser recovery. But for the long loop in Fig.2.19(b), when the inner switch S2 commutates with diode D4 under small gate resistor case, a long current tail is observed after diode reverser recovery. This is unique case for the 3-level DNPC long loop.



(a) Short loop (b) Long loop

Fig. 2.19. Turn on waveform comparison for two loops at DNPC mode

A detailed analysis of the turn on transient for the inner switch in DNPC phase leg explains the reason for the long current tail. Fig.2.20 gives the turn on voltage and current waveforms for all the switches and diodes in the commutation loop. There are five pieces of time interval in the whole turn on transient. The corresponding power loop for each time interval is displayed in Fig2.21. Reference directions for voltage and current are also labeled in the circuit diagram.

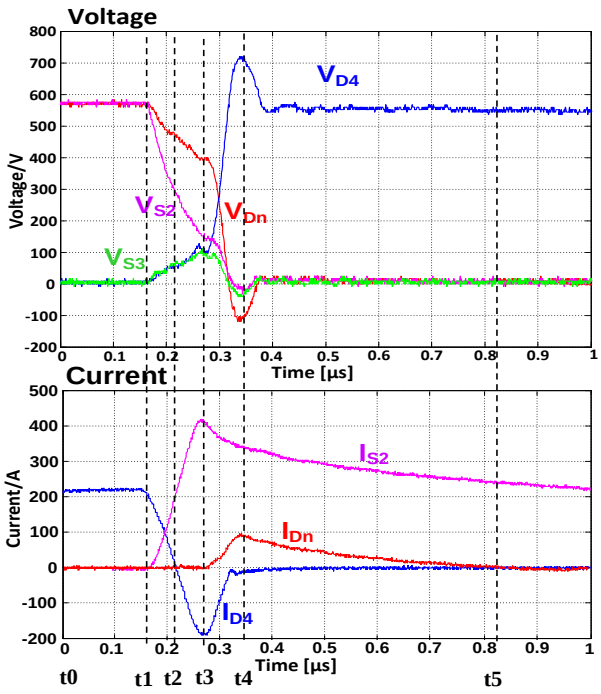


Fig. 2.20. Turn on transient voltage and current waveform for long loop

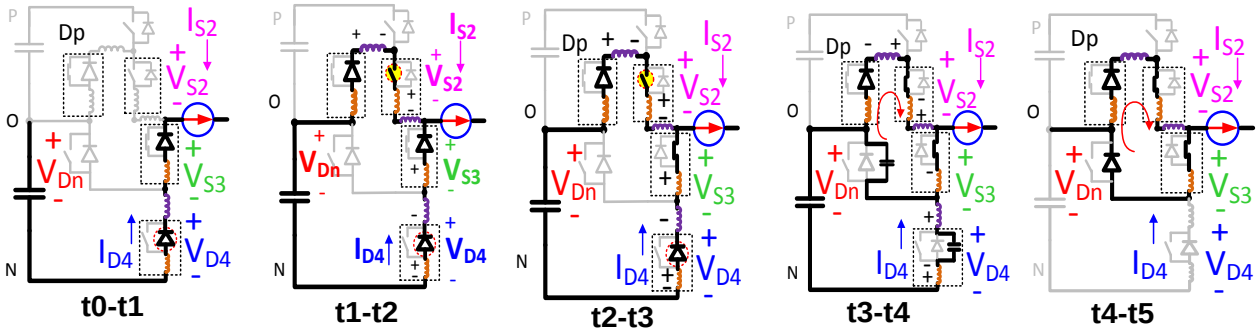


Fig. 2.21. Commutation loops for turn on transient intervals

From t0 to t1, the load current is freewheeling through diode D3 and D4. IGBT S2 is turned on at t1 and load current commutates from D4 and D3 to S2. At t2, diode current drops to zero. Since the gate signal for S3 is constantly on during the whole commutation period for DNPC modulation, the reverse recovery only occurs on D4. After t2, the current direction in D4 is reversed and S3 starts to conduct the reverse recovery current instead of D3. Before t3, D4 is under reverse recovery and should not block voltage. But the di/dt of commutation current is imposed on the switch modules of S2, S3 and S4, hence induces voltage on the module and loop parasitic. The induced voltage causes a small voltage drop on Dn and a voltage rise on both D3

and D4. This voltage is clearly shown in Fig.2.20 from t1-t3. At t3, reverse recovery current reaches its peak. The junction capacitor of D4 is fully charged and it starts to block voltage. The fast voltage buildup on D4 can also be observed from the waveform after t3. Since the diode Dn blocks the bottom DC link voltage together with D4, its voltage is clamped by D4. The fast voltage rise on D4 consequently causes a fast voltage drop on Dn. The junction capacitor of Dn is discharged quickly with a large discharging current. This discharging current I_{Dn} flows through Dp, S2 and S3 in t3-t4. During this time interval, di/dt of reverse recovery current inverses its polarity and causes voltage overshoot on D4. At t4, the voltage overshoot on D4 exceeds the half DC link voltage and Dn is therefore forward biased. At this time, S2 is fully turned on. Current I_{Dn} freewheels through a low impedance path formed by Dp, S2, S3 and Dn. The large loop parasitic also helps the freewheeling and causes the long current tail after IGBT is turned on. The analysis reveals that the cause for the current tail is very complex and many devices are involved.

The impact of different parameters on the current tail is then investigated to further verify the above analysis. The current tail waveforms under different load current conditions are observed in Fig.2.22. The tail length and peak are also measured and summarized in Table.2.6. The long tail still exists under a small load current. The current tail peak is proportional to the load current. It can reach up to 175A under full load conditions. On the contrary, the current tail length is not influenced much by load current.

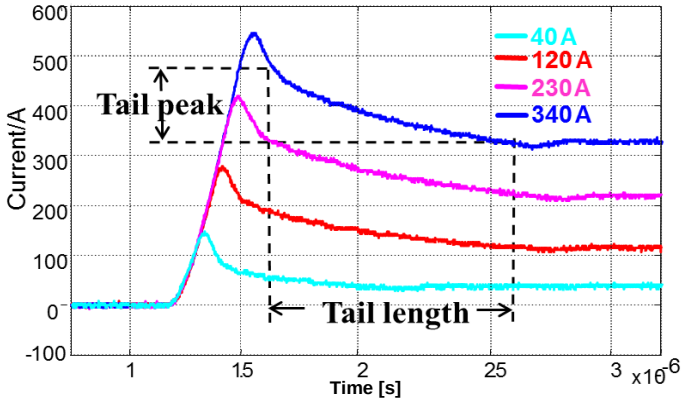


Fig. 2.22. Current tail waveform with different load current

Table 2.6. Current tail parameters with load current

Load current	40A	120A	230A	340A
Tail peak	42A	128A	145A	175A
Tail length	0.94μs	1.02μs	0.98μs	1.04μs

Different connections are used to connect Dp and S2, resulting in different loop parasitic. For the original phase leg design, the parasitic inductance for Dp module and its connection is around 40nH. Then longer and shorter copper bars are applied to the power stage in order to observe the influence of parasitic on the current tail. The modified copper bars give an approximated parasitic inductance of 25 and 80nH. The current waveforms with different loops are shown in Fig.2.23. The measured current tail peak and tail length are concluded in Table.2.7. The result shows that with large loop parasitic, the current tail peak can be suppressed. However, the parasitic inductance helps the freewheeling of the tail current and causes longer tail length. This result is easy to be comprehended with the above explanations of the current tail.

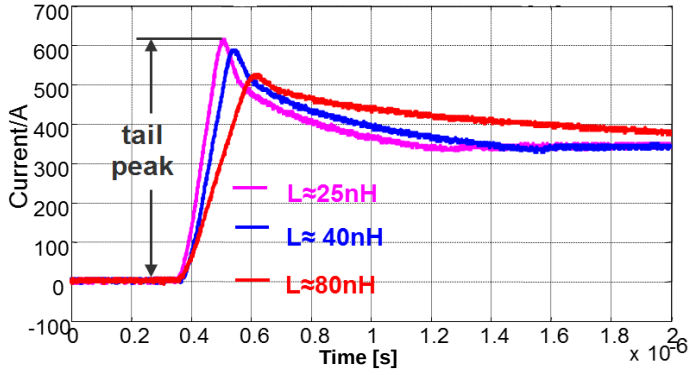


Fig. 2.23. Current tail waveform with different loop parasitic

Table 2.7. Current tail parameters with loop parasitics

Loop parasitic	25nH	40nH	80nH
Tail peak	610A	586A	522A
Tail length	0.62μs	0.86μs	1.52μs

The same analysis for the influence of the gate resistor on the current tail is shown in Fig2.24 and Table.2.8. The figure shows that current tail can be eliminated with a large gate resistor. This is because the large gate resistor reduces the turn on di/dt and overshoot voltage on diode D4. The above analysis explains that it is the D4 voltage overshoot that forward biases Dn and results in the freewheeling path. With turn on speed slowed down, the current tail disappears. However, Table.2.8 also shows that the large gate resistor increases turn on loss dramatically. This places a tradeoff between current tail and turn on loss.

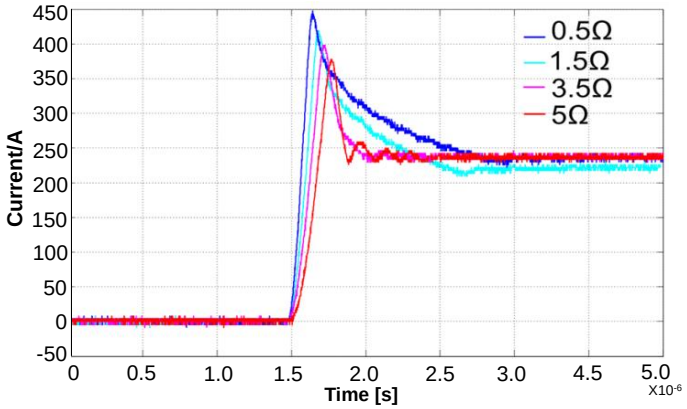
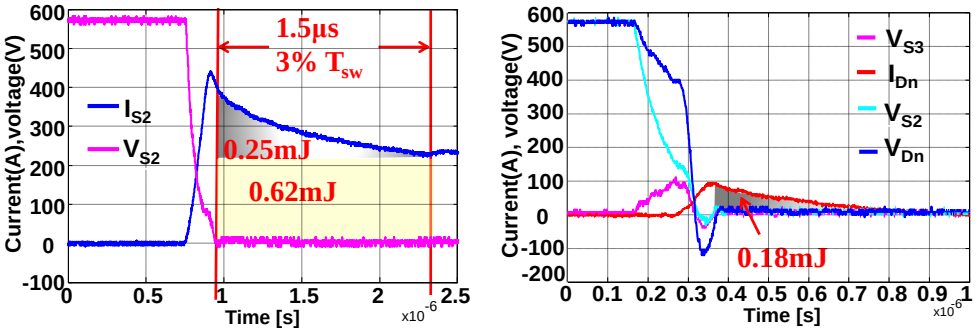


Fig. 2.24. Current tail waveform with different gate resistor

Table 2.8. Current tail parameters with gate resistor

R_{on}	0.5Ω	1.5Ω	3.5Ω	5Ω
current peak	447.7A	419.1A	385.9A	357.4A
di/dt(A/ns)	2.84	2.06	1.67	1.25
Turn on loss	6.73mJ	7.02mJ	20.1mJ	28.9mJ

Knowing the cause and influential factors to the long current tail, the problems brought by it are then discussed. Fig.2.25 shows the current and voltage waveform on each device in the freewheeling path under 230A turn on current and 0.5Ω gate resistor. It is noticed that the freewheeling current can reach 100A at peak and is proportional to the load current. The slow damping of this current causes extra conduction loss on diode and IGBT. The extra loss for Dp



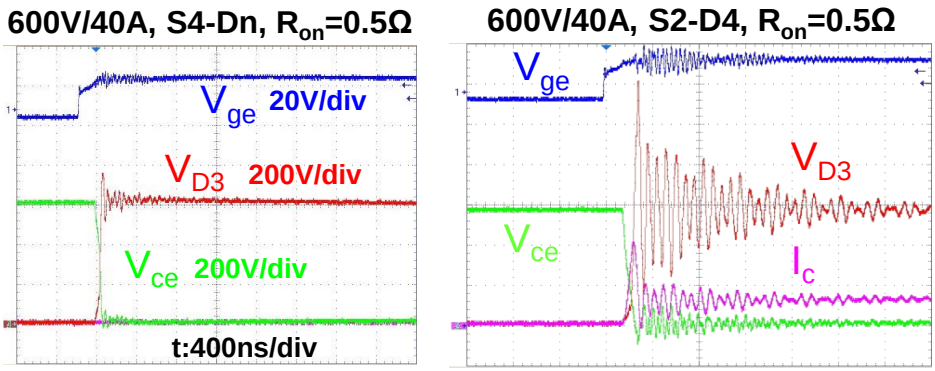
(a) Loss on S2 (b) Loss on S3, Sp and Sn

Fig. 2.25. Voltage and current waveform on freewheeling path

and S2 is around 0.25mJ. For Dn and S3, it is 0.18mJ. The overall 0.43mJ extra conduction loss is comparable with the 0.62mJ conduction loss without current tail. This extra loss occurs every switching cycle and is not trivial if switching frequency is high. Besides the extra conduction loss, the long current tail also extends the turn on transient. The freewheeling current lasts for 1.5μs and takes about 3% of the switching cycle under 20 kHz switching frequency. In the case of a small duty cycle and high frequency, the device may be turned off during the switching transient and cause a higher voltage spike. Therefore, the current tail is not desirable. Minimizing loop parasitic is one way to eliminate the tail, the other way is to increase the gate resistor. However, tradeoff is needed considering the switching loss of the large gate resistor.

2.3.4 Voltage Spike for Inner Switch Turn on

Besides the long turn on current tail for DNPC inner switch loop, another problem for inner switch turn on is observed under the ANPC mode where the inner switch commutates with the anti-parallel diode of the other inner switch. A high voltage spike and large voltage ringing is observed on that anti-parallel diode under small current turn on for the inner switch. Fig.2.26 gives the reverse recovery diode voltage comparison for the short loop and the long loop of the ANPC mode. Under 40A turn on current with 0.5Ω gate resistor, the voltage spike can be even higher than the device voltage rating. This is a more serious problem which may lead to disastrous consequences compared with the current tail of the long loop for DNPC mode.



(a) Short loop (b) Long loop

Fig. 2.26. Turn on waveform comparison for diode voltage

The impact of different parameters on the voltage spike is investigated in order to find out the cause and solution for the voltage spike. The diode voltage waveforms under different load current conditions are first compared and shown in Fig.2.27. It shows that the large diode voltage spike and ringing after reverse recovery only occurs under small load current conditions. Under a 340A peak load current, the voltage spike and ringing is not so obvious. Fig.2.28 shows the relationship between the load current and the diode voltage spike. It shows that 40A is the worst case with 1300V voltage spike. The spike reduces as the load current increases.

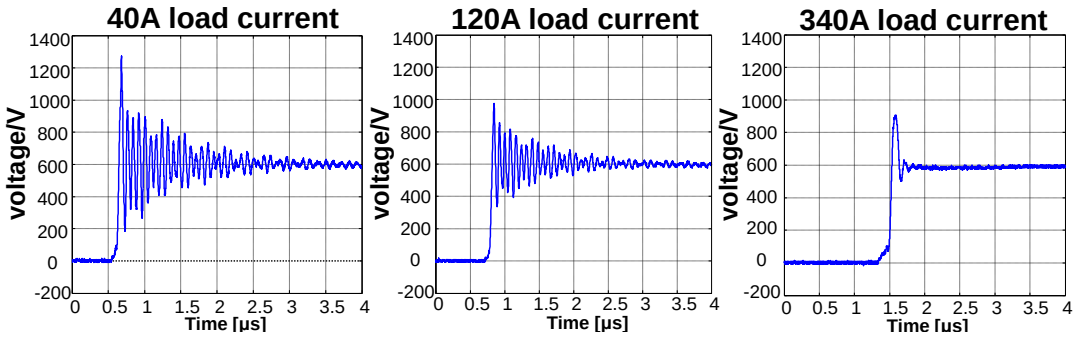


Fig. 2.27. Reverse recovery diode voltage under different load current

The cause of the voltage spike on the reverse recovery diode can be explained from Fig.2.29. After reverse recovery, the diode current I_{D3} quickly drops to zero. This current also appears in IGBT current I_{S2}, and make it drop fast to the load current. The high di/dt of this current induces voltage drop on parasitic inductance in the switching loop as shown in Fig.2.29. Voltage on D3 is the summation of DC link voltage and the induced voltage on parasitic. Since the long loop

contains many devices and copper bar connections, the commutating diode is subject to higher voltage stress caused by the high di/dt and fast transient.

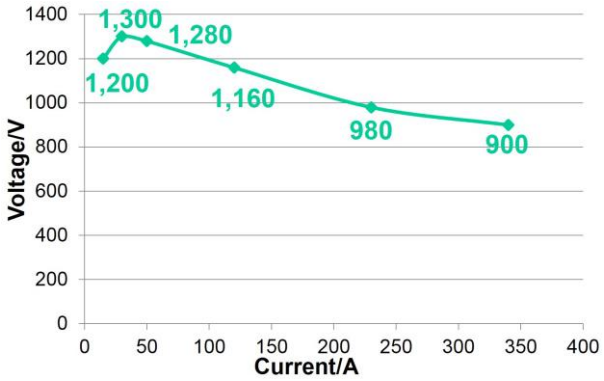


Fig. 2.28. Diode voltage spike with different load current

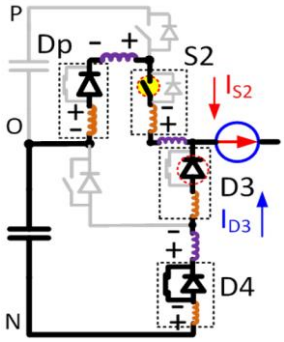
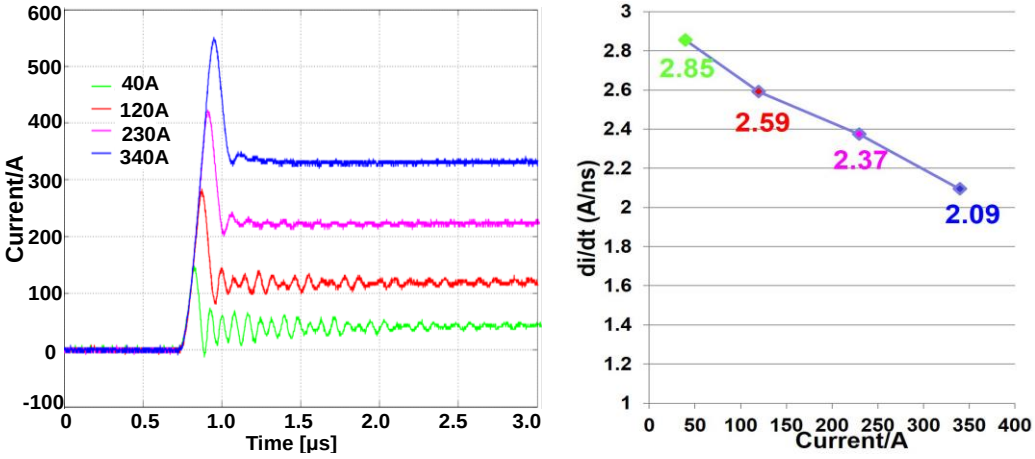


Fig. 2.29. Commutation loop for inner switch and diode after reverse recovery

To explain why the highest voltage stress happens under small load current conditions, the turn on current waveforms under different load current are compared in Fig.2.30. The di/dt after reverse recovery is also compared and shown in the same figure. The waveform shows that small current reverse recovery has a larger current oscillation. The reverse recovery current di/dt also shows an increasing trend with the decrease of load current. From the waveform in Fig.2.30(a) and the di/dt measurement in Fig.2.30(b), it can be concluded that the diode has a snappier reverse recovery performance under small current conditions. This property under small current condition is reported in [13]. The distribution of the minority carrier is influenced by the reverse recovery current and causes this phenomenon. It is said that the Controlled Axial Lifetime (CAL)

diode has the snappiest reverser recovery performance under 10% nominal current. In this design,



(a) Short loop (b) Long loop

Fig. 2.30. Turn on current waveform with different load current

the anti-parallel diode in the IGBT module is just the CAL diode. The highest voltage spike happens at 40A, which is 1/10 of the current rating. The special property of the CAL diode together with the large loop parasitic causes the ringing and higher spike on diode voltage.

Finally, different gate resistors are applied to evaluate the diode voltage spike under small current turn on. Fig.2.13 and Table.2.9 shows the diode voltage spike and turn on loss with different gate resistance under a 40A turn on current. The result shows that a large turn on gate resistor reduces the reverser recovery speed and related di/dt, thereby alleviating the voltage stress on the diode. This method is the only way to solve the voltage spike problem under the given phase leg design. However, the turn on loss is inevitably increased. Tradeoff between loss and voltage margin should be considered when selecting the R_{on} value for the inner switch.

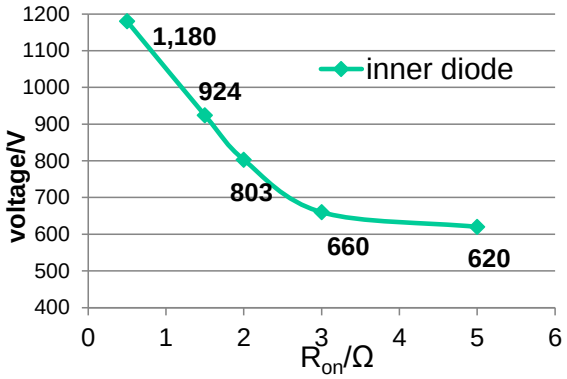


Fig. 2.31. Diode voltage stress at small current for long loop

Table 2.9. Diode voltage spike with turn on gate resistance

R_{on}	0.5Ω	1.5Ω	2 Ω	3Ω	5Ω
Vspike/V	1180	924	803	660	620
Eon/mJ	4.76	8.32	9.65	12.64	18.8

The turn on performance test reveals several special transients like a long current tail and a large voltage spike for the inner switch. These cases are exclusive for the 3-level NPC phase leg and have not been reported before. The causes for the phenomenon are complicated with the involvement of numerous factors like gate resistor, loop parasitic, load current and device property. But the dominant factors are the large parasitic for the inner switch loop and the high speed turn on with the small gate resistor. As a result of all the special turn on transients, the gate resistor for inner switch turn on can not be easily determined. All the problems should be taken care of by gate resistor selection. Tradeoff between loss and stress should also be considered.

2.4 System Loss/Stress Distribution and Loss Breakdown Analysis

The double pulse tests for the two switching loops show significant difference on their switching characteristics. To achieve the optimal switching performance for both loss and stress, the two switching loops should be treated differently. This is also true for the turn on and turn off performance. Turn off performance can be easily optimized as mentioned earlier. On the other hand, the optimization for turn on performance should consider the tradeoff between loss and stress. The current tail and voltage spike for the inner switch in the long loop also needs to be

dealt with. As a result, the turn on gate resistor for the inner switch in the long loop is larger than that of the outer switch in the short loop. In the real experiment, a 0.5Ω gate resistor is used for the inner and outer switch turn off. For the turn on resistor, 0.5Ω is applied to the outer switch in the short loop. The inner switch in the long loop uses 1.7Ω for the current tail and voltage spike elimination. The selection for inner switch R_{on} considers the loss and stress trade off.

2.4.1 Phase Leg Loss and Stress Distribution Analysis

A curve fitting for the switching energy of the two loops is conducted and shown in Fig2.32. The curve fitting result is used for switching loss calculation in one line cycle. The detailed loss model can also be built based on the simulation model for the system and the double pulse test result. The switching energy in each switching cycle can be integrated over a line cycle based on the modulation scheme and the operating mode. According to the gate signals and the current directions, the switching loop used for the specific switching cycle can be derived and the switching energy for that loop is added to the summation. Then combined with the conduction loss, the total system loss breakdown and system efficiency can be calculated. Also the phase leg loss distribution on each device can be calculated. This method provides a very powerful tool to conduct quantitative analysis for total system loss of different NPC modulation schemes with different power factors. The calculation is based on 200kVA, 20 kHz operating condition. A loss and stress distribution is analyzed for all the three modulation schemes.

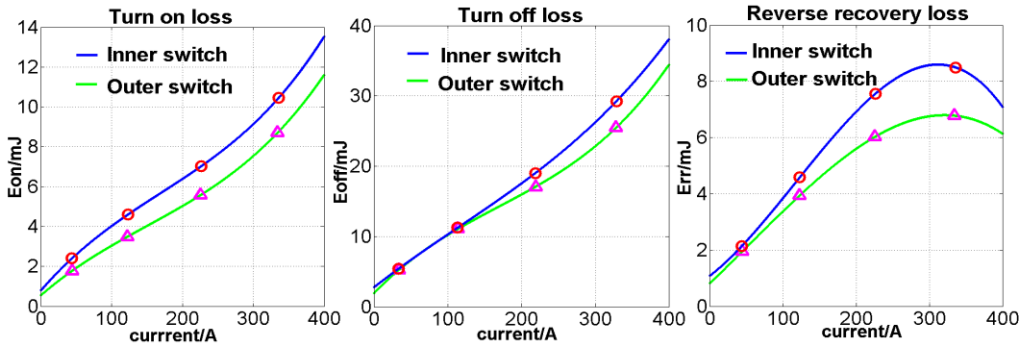


Fig. 2.32. Switching loss curve fitting for the two switching loops

For the DNPC operation mode, since the switching loop varies with the power factor, the device stress and loss distribution also changes with the operating conditions. Fig2.33 gives the maximum voltage stress for all the switches in the phase leg with power factors. Fig.2.34 shows a detailed analysis for phase leg loss distribution on all switches with power factors. When the power factor is 1, the system works at the inverter mode in 1st and 3rd quadrants. Only the outer

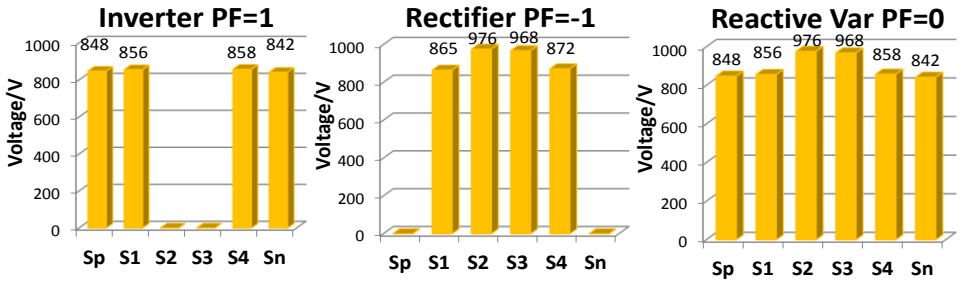


Fig. 2.33. Maximum voltage stress for DNPC with power factor

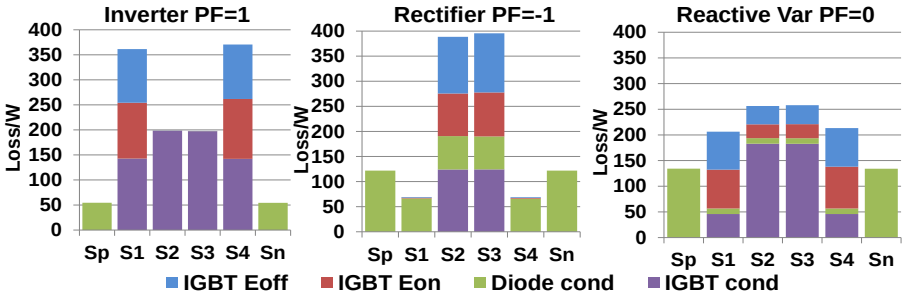


Fig. 2.34. Phase leg loss distribution for DNPC with power factor

switches and clamping diodes in the short loops are engaged for high frequency switching. Major loss occurs at the two outer switches S1 and S4. The two inner switches S2 and S3 only have conduction loss. The stress also only occurs on the outer switch since they are doing high frequency switching. In the case of power factor equals to -1, the system works at rectifier mode and only two inner switches in the long loop are involved in the switching. Most part of the switching loss concentrates on the inner switches. The major stress is also endured by the inner switches. Outer switches only have diode loss. For PF=0 case, the system works at all 4 quadrants and both the long loop and short loop are involved. All the four switches and the

clamping diodes take stress and loss. The loss and stress analysis shows that the switches in DNPC phase leg have different stress and loss. The loss/stress distribution pattern also varies with power factor. In addition, since the loss/stress for long loop and short are not the same, the DNPC has different total loss and maximum stress under different power factors.

For the ANPC modulation with outer switch mode, the commutation happens between the outer and the clamping devices in all quadrants. As a result, only the short loop is involved. The maximum voltage stress for the ANPC outer switch mode and the DNPC phase leg are compared under different power factors in Fig.2.35. The stress for ANPC concentrates on the outer and clamping devices. Compared with the DNPC phase leg with uneven stress distribution, the ANPC outer switch mode keeps the same stress under different operating conditions. Also the maximum stress is smaller for ANPC since only short loop is used. The phase leg loss distribution for ANPC phase leg is also analyzed in Fig2.36. Because of the unified switching loops under different power factors, the outer and clamping switches bear the major loss. The inner switches only have conduction loss. Besides the same loss and stress distribution pattern with power factor, this modulation for ANPC has the unified total system loss with power factor.

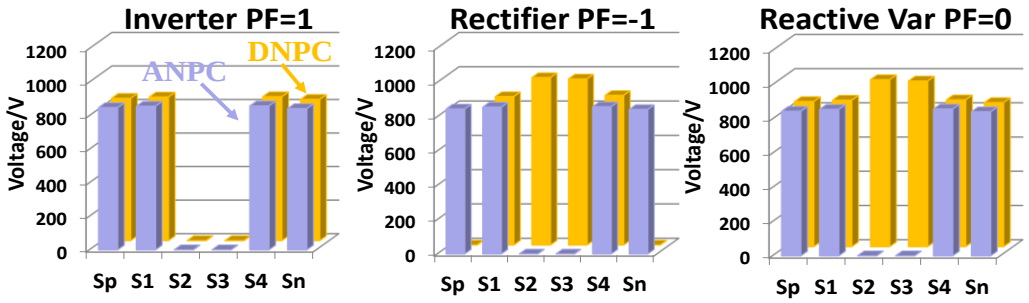


Fig. 2.35. Maximum voltage stress for DNPC and ANPC outer switch mode

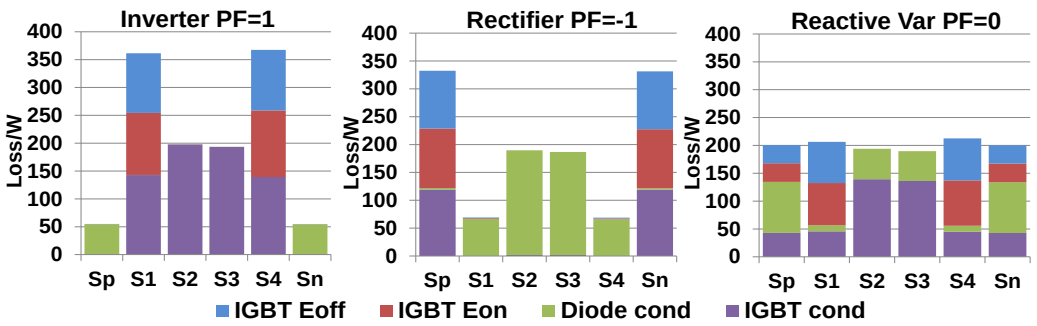


Fig. 2.36. Phase leg loss distribution for ANPC outer switch mode

The ANPC modulation with inner switch mode only uses long loop in all the four quadrants. Moreover, only the inner switches are used for commutation at different operating conditions. As a result, the voltage stress is only imposed on the inner switches as shown in Fig.2.37. The phase leg loss distribution for this modulation in Fig2.38 shows that the major loss also concentrates on the inner switches. This modulation only uses long switching loop, which results in higher switching stress and loss. But it contains only 1 commutation pole in all quadrants. For ANPC phase leg with soft switching [10], it can save 1 resonant tank and 2 auxiliary switches.

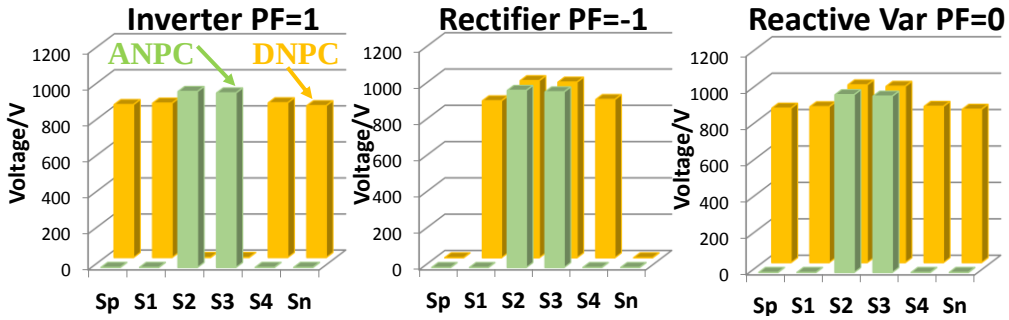


Fig. 2.37. Maximum voltage stress for DNPC and ANPC inner switch mode

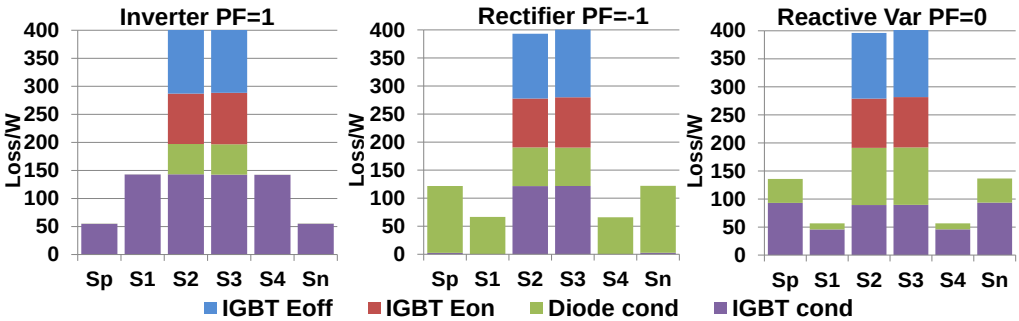


Fig. 2.38. Phase leg loss distribution for ANPC inner switch mode

The above analysis shows that loss distribution for DNPC phase leg varies with power factors because different switching loops are used under different cases. The ANPC phase leg has two modulation schemes with two switching modes associated with them. The outer switch mode with short loop has switching loss and stress concentrated on the outer and clamping switches under all power factors while the inner switch mode with long loop has higher loss and stress on inner switches. By alternatively choosing different ANPC modes, loss can be distributed on each device more evenly. This is a well-known benefit for ANPC topology.

From the switching loop point of view, new benefit of ANPC topology is revealed. The switching performance evaluation shows that the inner switches in the long loop have a larger parasitic which causes some undesirable switching transients like current tail and high voltage spike. For DNPC phase leg, the turn on gate resistor for the inner switch should be large enough to slow down the switching speed and to avoid the undesired switching transients. The turn on loss for the inner switches in the long loop is inevitably increased. Also the turn off loss for the inner switches in the long loop is larger than that of the outer switches in the short loop due to the large parasitic. As a result, the total system loss for rectifier mode with only long loop is larger than that of the inverter mode with only short loop. The total system loss breakdown for the 3-phase DNPC converter at rated power and rated current is shown in Fig.2.39. The loss for DNPC converter with different power factors are calculated from the loss model and compared together. It clearly shows that the total conduction loss for different operating modes does not change too much. It only transfers from IGBT to diode when the power factor shifts from 1 to -1. But the total switching loss for different operating modes has significant difference. For the DNPC converter, the total system loss and efficiency varies with the operating modes and power factors of the converter.

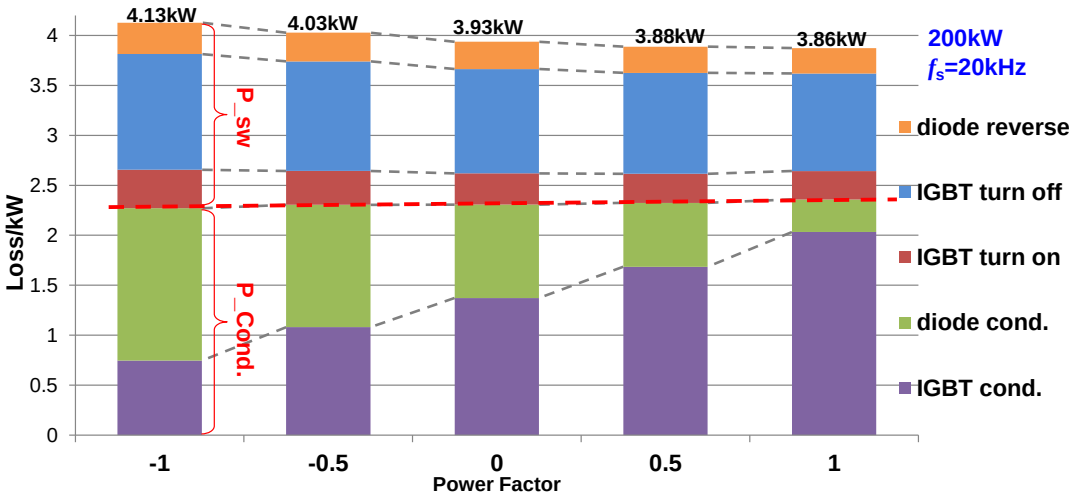


Fig. 2.39. Total system loss breakdown for DNPC converter

By using ANPC topology, the switching loops can be flexibly chosen to avoid the large loop parasitic of the long loop. By doing so, loss can be reduced and stress can be alleviated. System loss breakdown for ANPC with two modulation schemes can also be calculated as the DNPC system does. The total system loss and efficiency of the 3 different modulation schemes for 3-level NPC converter under different power factor cases are compared in Fig.2.40. For DNPC operation, the system has the highest efficiency of 98.08% under PF=1 at inverter mode when the short loop is used only. Under rectifier mode when PF= -1, the system has the lowest efficiency below 98% because only the long loop is used. For ANPC outer switch mode, the system efficiency stays constant at around 98.08% under all power factors, which correspondent to the highest efficiency for DNPC at inverter mode. And for ANPC inner switch mode, the efficiency keeps constant at 97.9% which is the lowest efficiency for DNPC at rectifier mode. This result demonstrates the advantage of the ANPC phase leg for loss and stress reduction.

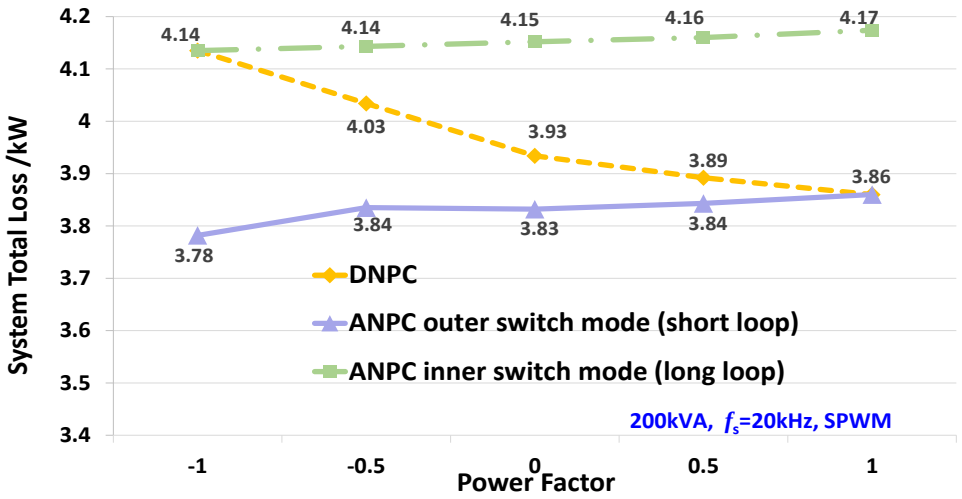
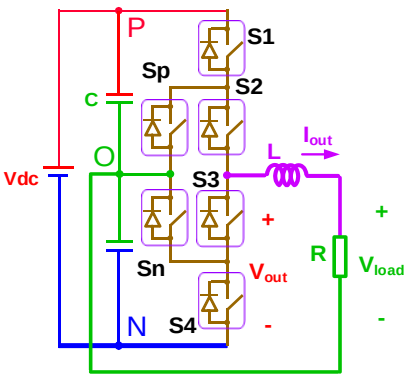


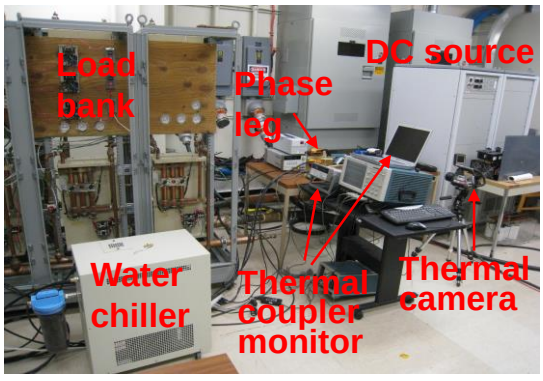
Fig. 2.40. Total system loss for 3 operating modes for 3-level NPC converter

2.4.2 Experimental Verification for Phase leg Loss and Efficiency

Finally, to verify the switching performance optimization result, the phase leg is tested under different power ratings from full load (67kVA) to one quarter load (15kVA). The test circuit and test bed setup are shown in Fig.2.41. The circuit parameters are given in Table.2.10. The DC link of the phase leg is powered up by a 100kW DC power source. A 100kW water cooled adjustable load bank is used as resistive load for the phase leg. A recycling water chiller is used as the cooling system for the phase leg. The case temperature on each switching device is recorded by the thermal couplers and thermal camera. The phase leg efficiency is measured by a power meter with up to 1MHz bandwidth. The 3-level output voltage and sinusoidal phase current proves that the phase leg works as expected. Fig.2.42 gives the power test waveform at full power rating.



(a) Test circuit diagram



(b) Test setup

Fig. 2.41. Power test circuit diagram and test setup

Table 2.10. Phase leg power test circuit parameters

Power	DC voltage	Load current	Inductor L	Capacitor C
15-67kW	1200V	240A RMS	0.3mH	2.5mF

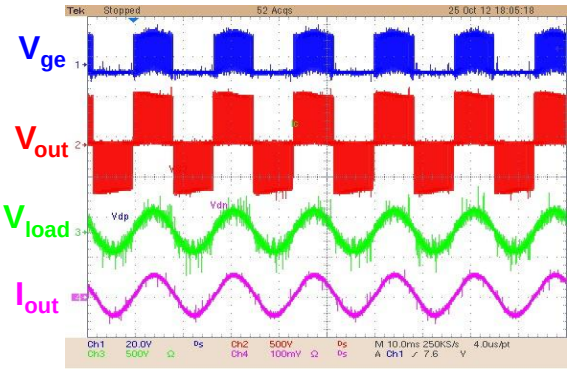
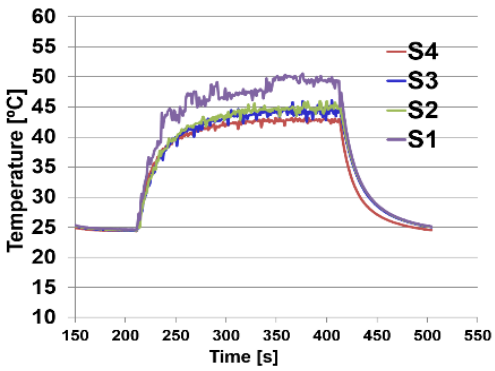
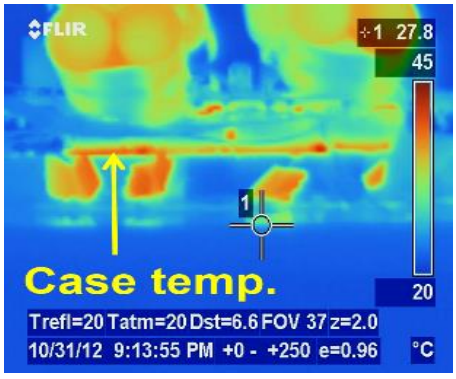


Fig. 2.42. Phase leg full power test waveform

The thermal performance of the phase leg is evaluated by thermal coupler and also by a thermal camera that records the temperature distribution on phase leg. The phase leg is running at full power until it reaches the thermal steady state. Temperature curves in Fig.2.43(a) is measured by thermal couplers attached on the case of each device and thermal image in Fig2.43.(b)shows the heat distribution on phase leg. The experimental result is compared with the simulation result mentioned in 2,1,3. The comparison in Table.2.11 shows that the simulation result and experimental result does not have too much variation. The highest case temperature is only 50ºC, the junction temperature will not exceed 80ºC and there is large enough thermal margin to run the phase leg at high power and high frequency.





(a) Recorded device case temperature (b) Thermal camera image of phase leg

Fig. 2.43. Phase leg temperature curves and thermal image

Table 2.11. Case and junction temperature by simulation and experiment

Switch	Case temp. by experiment	Case temp. by simulation	Junction temp. by simulation
S1	50ºC	39.8ºC	60.7ºC
S2	45ºC	38.7ºC	52.9ºC
S3	44ºC	38.4ºC	52.6ºC
S4	42ºC	38.1ºC	58.6ºC

Finally the phase leg efficiency is measured with different load conditions from a quarter of full load to full load to verify the calculated efficiency by the loss model. The measured result from the power meter at full load condition is shown in Fig.2.44. The voltage and current at both AC and DC side are displayed. The total power, power factor and system efficiency result can also be found in the measurement. The phase leg efficiency curve at different load conditions is shown in Fig.2.45. It can be seen that the phase leg efficiency at rated power is 98.33% and the highest efficiency is 98.43% under 50kW power. This result shows the design objective of a high power high efficiency phase leg under high switching frequency condition is accomplished. But more importantly, it verifies the loss model built by simulation and double pulse test. The measured real phase leg efficiency at full power condition matches the calculated efficiency. The loss model can be used as a powerful tool for quantitative loss analysis. It can provide an accurate loss estimation for the power conversion system design.

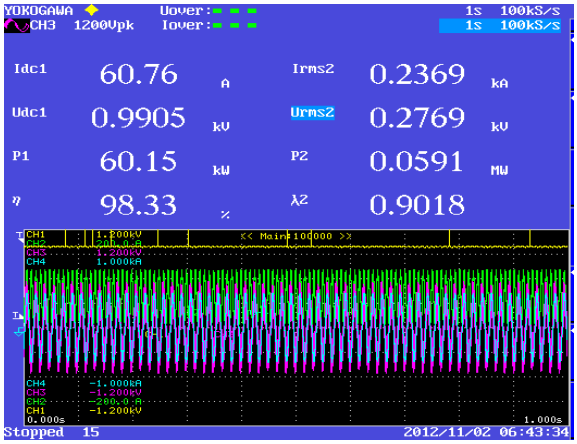


Fig. 2.44. Efficiency measurement result by power meter

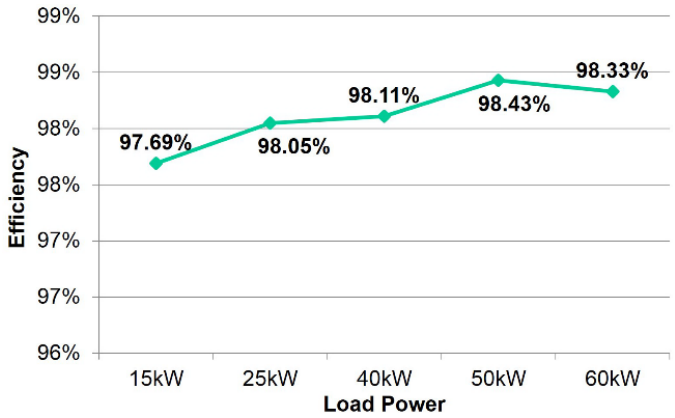


Fig. 2.45. Phase leg efficiency curve by measurement result

2.5 Summary and Conclusion

This chapter discusses the design and implementation of the high power high frequency 3-level NPC phase leg building block for the power conversion system. The major research work in this chapter is the thorough switching performance evaluation and characterization of the 3-level NPC phase leg. The switching frequency for the 200kVA rated converter is 20kHz and the efficiency target is over 98%. A step by step design procedure is given for the modularized phase leg building block. The issues under high switching frequency and high power operation are identified and analyzed. The device is first selected to enable the minimum total loss and highest efficiency. Then the phase leg layout is designed with minimum loop parasitic. The gate driver is designed to support high switching frequency. The four-quadrant operating modes and switching

loops for DNPC and ANPC phase leg are identified. The different loop parasitic for inner and outer switch results in distinctive switching performance variation. Turn on and turn off characteristics for the inner and outer switch in the long and short switching loop is evaluated with the consideration of various factors like gate resistor and parasitic inductance. Special switching transients like long current tail and large voltage spike on the diode, which have never been reported before are observed. These transients are exclusively for a 3-level NPC phase leg. The causes of these transients are thoroughly explained and analyzed. The analysis considers many factors like load current, loop parasitic and gate resistance. The double pulse test results show that switching performance for the inner and outer switch should be optimized separately due to the different loop parasitic. It is also true for the turn on and turn off performance optimization.

The overall switching performance is optimized for loss and stress tradeoff. A detailed loss model is built based on the optimization result. The total system loss breakdown for DNPC and ANPC modulations under different power factors are calculated. The phase leg loss and stress distributions for DNPC and ANPC with different power factors are revealed. The ANPC phase leg can be modulated to have a more evenly distributed loss and stress among all the switches in one phase leg. Also the total system loss and efficiency is constant at different power factor cases. Moreover, the ANPC topology can also be used to reduce the switching loss under different operating conditions because of the flexibility in the switching loops. Finally, the phase leg is tested under rated power and 20 kHz switching frequency. The efficiency measurement is above 98% under rated power and the phase leg design objective is achieved.

The research contributions in this chapter is concluded as the following:

1. Provides a detailed design procedure for the modularized 3-level NPC phase leg.

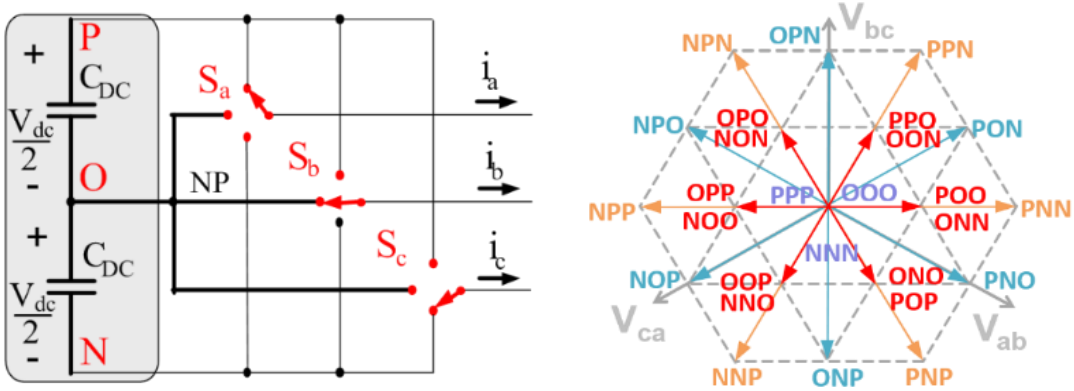
2. Identifies the two switching loops in 3-level NPC phase leg and gives an in thorough evaluation of the switching characteristics for the two loops.
3. Investigates some special switching transients for the 3-level NPC phase leg. Gives an in-depth explanation and analysis for these switching transients.
4. Build an accurate loss model for the 3-level NPC converter based on simulation and experiment. The loss model provides a quantitative analysis for loss breakdown and loss distribution for each switching devices in the circuit. It can provide the total system loss over a line cycle for different power factor cases or operating modes. This methodology is universal and can be adopted for loss analysis for other topologies.
5. Gives a detailed analysis for the phase leg loss and stress distribution, as well as the system total loss breakdown for DNPC and ANPC with different power factors.

CHAPTER.3 SVM STRATEGIES FOR NP BALANCE AND LOSS REDUCTION

Different modulation strategies for multilevel converter like the carrier based SPWM, the space vector based modulation (SVM or SVPWM) and the hybrid modulation are investigated in Chapter.1.3. The SPWM method is easy to implement by simply comparing the reference with the carrier. On the contrary, the SVM method is complex in its calculation and implementation. But it has more control freedom because the vector selection and pulse sequence alignment can be flexibly configured. Considering the extra control flexibility and freedom, the SVM is used for the high frequency converter to enable a better performance. Also it is the common practice for most of the industrial products of 3-level NPC converter to use SVM as modulation strategy.

In this chapter, the principle of the SVM for the 3-level NPC converter is introduced at first. The conventional 3-step implementation for the SVM is elaborated. The different duty cycle calculation method is first introduced and compared in 3.1. Then the different small vector selection criteria for control objectives like neutral point balance, loss reduction and noise reduction is analyzed and evaluated in 3.2. The control result like total system loss, NP voltage ripple and CM noise spectrum for these control objectives is also quantified and compared together in this part. Then the different pulse sequence alignment methods are also introduced and compared in 3.3. The issue for the conventional SVM for NP balance is raised in 3.4. Then the proposed SVM for NP balance and loss reduction is introduced in detail and the result is quantified by simulation and experimental result. Finally in 3.5, the dead-time compensation method for the 3-level NPC converter using SVM is discussed. The compensation principle is introduced first, followed by the dead-time compensation result, which is verified by both simulation and experimental result.

For the 3-level NPC converter, each phase leg can be equaled to a 1 pole triple-throw switch that connects to the positive, negative or neutral rail as shown in Fig.3.1(a). For the 3-phase 3-level converter, there are total 27 switching status, corresponding to 19 space vectors in the line to line voltage space as shown in Fig.3.1(b). Among them, there are 6 long vectors, 6 medium vectors, 6 small vectors and 1 zero vectors. The small and zero vectors have redundant switching states to choose. For the SVM method, the selection of the redundant switching states is the key step that enables the modulation to achieve different control objectives like neutral point (NP) voltage balance [1]-[5], switching loss reduction [6] or common-mode (CM) noise reduction [7]-[9]. The NP voltage balance isessential to maintain a good output voltage and current waveform. It also guaranties the proper function of the converter. Therefore, it is treated as the control priority by most of the conventional SVM schemes for 3-level NPC converter.



(a) Circuit diagram (b) Space vector diagram

Fig. 3.1. Circuit and space vector diagram for 3-level NPC converter

Although different NP balance algorithms are proposed [10]-[14], none of them deals with the switching loss reduction because the redundant switching states selection is based on single objective. However, for the high power high frequency NPC power conversion system, loss and noise reduction is another important goal besides the NP balance. This chapter gives a thorough survey on the different control objectives of SVM for 3-level NPC converter. The control result for NP voltage ripple, switching loss and CM noise spectrum are compared and analyzed. The

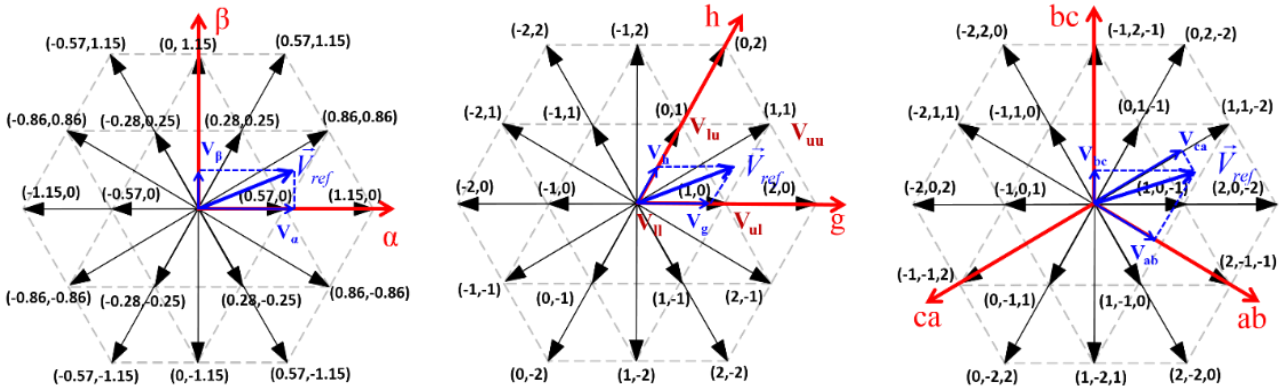
detailed loss model from chapter 2 is used to provide a quantitative analysis of the system loss with different SVM and DPWM strategies. Based on the existing control algorithms, a new SVM strategy is proposed in this chapter to achieve multiple control objectives at the same time. The NP voltage is balanced together with the switching loss/noise reduced. The switching states for small vector are selected based on both the NP charge and the pulse sequence. Moreover, the switching loss between switching cycles is also reduced by proper pulse sequence alignment. It further reduces the total loss and most importantly makes the phase leg loss distribution symmetrical. The proposed SVM strategy maintains the similar total loss and NP balance result under different power factors. The control result is verified on both simulation model and hardware of the 3-level NPC converter. In this chapter, the dead-time compensation method for the 3-level NPC converter is also discussed and implemented on the converter hardware.

3.1 SVM Duty Cycle Calculation Methods

The trajectory of the rotating voltage reference mapped on the space vector diagram is a circle. In steady state, the voltage reference vector V_{ref} rotates inside the inscribed circle of the space vector hexagon. The radius of this circle is the longest voltage reference vector the converter can generate. The first step for SVM is to determine the location of the V_{ref} and find three vectors to synthesis it. The duty cycle of these three vectors is also calculated in this step.

There are three different coordinate systems for the vector space as shown in Fig.3.2 The calculation for the V_{ref} location and duty cycle can be done in any of the coordinate systems. The commonly used one is the orthogonal α-β coordinate in Fig.3.2(a) [15]. In this coordinate, the location for V_{ref} and the duty cycle for the vectors is calculated with trigonometric functions. A non-orthogonal g-h coordinate system shown in Fig.3.2(b) is mentioned in [16]. The benefit of this coordinate system is that all the vectors have an integer coordinate in this system. Therefore,

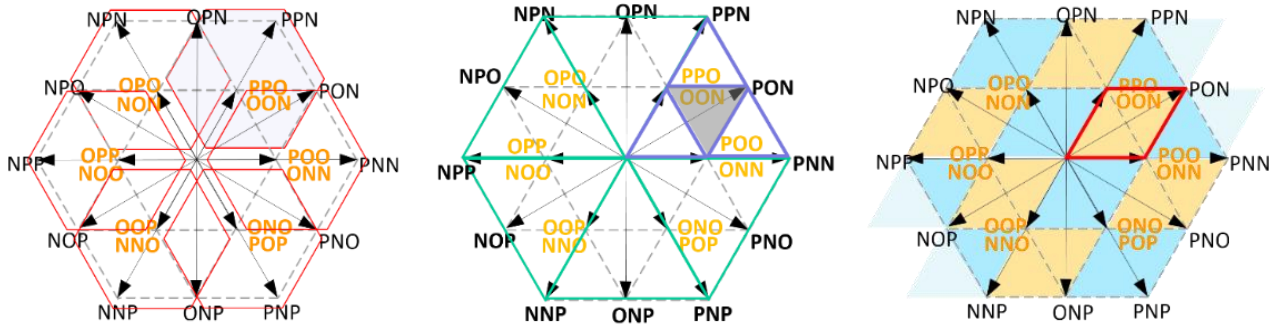
trigonometric functions are replaced by algebraic operation. Thus the calculation process is largely simplified. Another coordinate system in Fig.3.2(c) is proposed by [17]. This system has three axes and shares the same benefit of the g-h coordinate.



(a) α-β coordinate (b) g-h coordinate (c) a-b-c coordinate

Fig. 3.2. Three types of coordinate systems for 3-level NPC space vector diagram

For the 3-level space vector hexagon, there are several sector division methods to locate the V_{ref} and to calculate the duty cycle. The hexagon division method shown in Fig.3.3(a) divides the 3-level vector hexagon into six of the 2-level hexagons [18]. With this sector division method, the calculation rules for the 3-level SVM follows the rules of 2-level SVM. However, this division method results in overlapped areas. Also the origins for the 2-level hexagons are different. These problems need to be dealt with by an extra process. The triangular division method in Fig.3.3(b) is commonly used [15]. The 3-level vector hexagon is divided into 6 large triangles. Each of them can be further divided into 4 small triangles. The vertexes of the small



(a) Hexagon division (b) Triangular division (c) Parallelogram division

Fig. 3.3. Three sector division methods for 3-level NPC vector space diagram

triangle are the nearest three vectors (NTV) to synthesis the V_{ref}. Taking the shaded area in Fig.3.3(b) as an example and considering the orthogonal α-β coordinates in Fig.3.2(a), the large triangle area can be drawn in Fig.3.4. This triangle area is determined by the rotating angle θ of the vector reference V_{ref} in the α-β coordinates as follow:

$$\theta = \arctan \frac{V_{ref}(\beta)}{V_{ref}(\alpha)} \tag{3-1}$$

The triangle area in Fig.3.4 is the first 60° for θ where $0<\theta<60^{o}$. Besides the rotating angle, the amplitude for the voltage reference vector should be calculated to locate its position. The amplitude M for V_{ref} can be calculated by

$$M = \frac{\sqrt{V_{ref}^2(\alpha)+V_{ref}^2(\beta)}}{V_{dc}} \tag{3-2}$$

With M and θ calculated, the sector that contains the nearest three vectors to synthesis V_{ref} can be determined by the following inequality. It should be noticed that the inequality only applied to the shaded area in Fig.3.4. The other small triangle areas have totally different inequalities.

$$\begin{aligned} \sqrt{3}M\cos\theta - M\sin\theta < 1 \\ \sqrt{3}M\cos\theta + M\sin\theta > 1 \end{aligned} \tag{3-3}$$

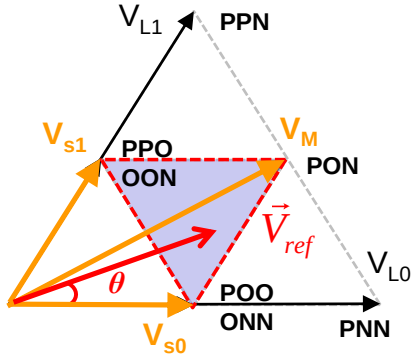


Fig. 3.4. First 60° of the triangle in space vector hexagon

Finally, the duty cycle for the nearest three vectors V_{S0}, V_{S1} and V_M can be calculated as

$$\begin{aligned} d_{S0} &= 1-2M\sin\theta \\ d_{S1} &= 1+M(\sin\theta-\sqrt{3}\cos\theta) \\ d_{M} &= -1+M(\sin\theta+\sqrt{3}\cos\theta) \end{aligned} \tag{3-4}$$

This method is the common practice for 2-level and 3-level SVM calculation. From the above equations, it is noticed that the calculation involves complex trigonometric functions which increase the computation cost. Also, there are 24 small triangles in total. The boundary conditions for each triangle are different and also the duty cycle calculation for each vectors are not the same. A case by case analysis is needed in the calculation.

The parallelogram sector division [16] in Fig.3.3(c) comes with the g-h coordinate. The space vector diagram is divided into 14 parallelogram instead of 24 triangles. The coordinate for V_{ref} in the g-h system is easily transformed from α-β system by the following transformation:

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & -1 \\ 0 & 2 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3-5}$$

Because all the vectors in the g-h system have an integer coordinate, the vertexes of the parallelogram can be easily identified by rounding the numbers of V_g and V_h. There is one example in Fig.3.2(b) to define the variables V_{ul}, V_{lu}, V_{ll} and V_{uu} in red letters. The position for these variables in the g-h coordinate can be calculated in the follow, where ceil is the rounded up operation and floor means the rounded down operation.

$$V_{ul} = \begin{bmatrix} ceil(V_g) \\ floor(V_h) \end{bmatrix}, V_{lu} = \begin{bmatrix} floor(V_g) \\ ceil(V_h) \end{bmatrix}, V_{ll} = \begin{bmatrix} floor(V_g) \\ fllor(V_h) \end{bmatrix}, V_{uu} = \begin{bmatrix} ceil(V_g) \\ ceil(V_h) \end{bmatrix} \tag{3-6}$$

The NTVs can then be located with the vector's location determined. Duty cycle calculation for NTVs is also simple with algebraic operation instead of trigonometric functions as follow:

$$\begin{aligned} d_{lu} &= V_{uu}(g) - V_{ref}(g) \\ d_{ul} &= V_{uu}(h) - V_{ref}(h) \\ d_{uu} &= 1 - d_{ul} - d_{lu}, \end{aligned} \tag{3-7}$$

The above calculation only involves algebraic operation. Also the whole calculation process can be applied to all the sectors. The case by case analysis is no longer needed. For these reasons, the calculation process is largely simplified. This simplification is important to save

computation costs for the neutral point balance and loss reduction control of the SVM at high switching frequency. The computation cost for the above two calculation methods are compared in Table.3.1. The comparison is based on the implementation of the two methods with C code in a 32-bit floating-point DSP. The DSP is TMS320C28343 with 200MHz clock frequency.

Table 3.1. Comparison of the two calculation methods for 3-level NPC SVM

	Operation	Numbers of instructions	Execution time
α-β coordinates	trigonomitric	1140	18μs
g-h coordinates	algebraic	202	4μs

3.2 Criteria for Small Vector Selection

With the reference vector's location determined and the duty cycle for the vectors calculated, the next step is the selection of redundant switching states for small vector to achieve different control objectives. Still taking the first 60º sector in the space vector hexagon as example, it can be noticed that each small vector has two switching states, which is the redundancy that provides extra control freedom. Depending on the applications, the redundant switching states can be used to balance the neutral point voltage, reduce EMI noise or reduce the switching loss. Based on the 200 kVA 3-level NPC power conversion system, the principle to achieve the three control objectives are analyzed and the control results for the NP voltage, the CM noise and the switching loss are compared in the following parts.

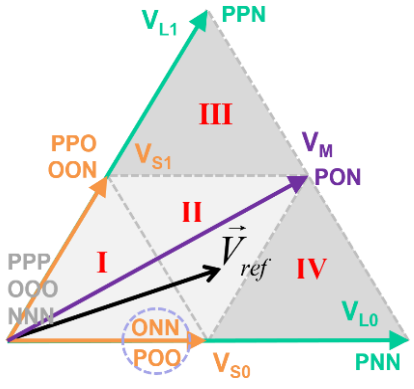
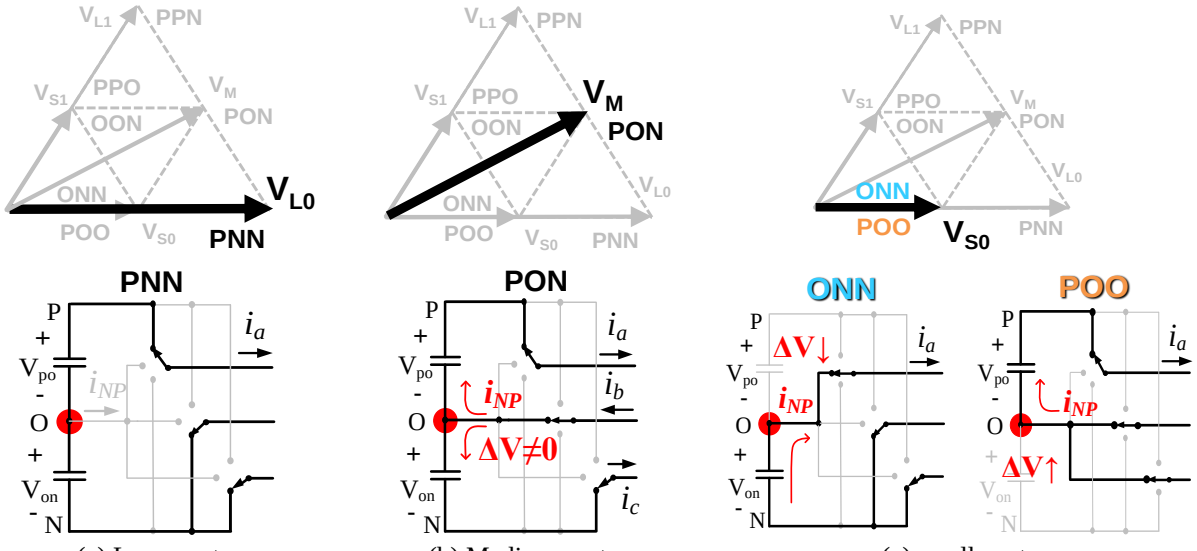


Fig. 3.5. First 60° sector of the space vector diagram

3.2.1 Method 1: Neutral Point Voltage Balance

For the NPC converter, the DC link is separated by several capacitors, each of which provides one output voltage level. For the 3-level NPC converter, the positive and negative level keep the same voltage only if the voltage across the two DC link capacitors are the same. In other word, the neutral point voltage potential must be a fixed value. If not, the output voltage waveform is distorted and the output harmonic is increased. So the neutral point voltage balance is necessary to reduce the harmonic and to maintain proper function of the converter. The NP balance is usually achieve by the modulation scheme and SVM is capable for such task. The four types of vectors for 3-level NPC converter that is introduced in 3.1 have different influence on neutral point voltage. By defining the neutral point voltage imbalance as the difference between the bottom and top cell capacitor voltage $\Delta V=V_{ON}-V_{PO}$, the influence of different vectors can be analyzed as shown in Fig.3.6. The analysis still takes the first 60° triangle sector in Fig.3.5 as example. The circuit diagram for the long, medium and small vectors are also shown. For the long vector in Fig.3.6(a), both of the top and bottom cell capacitors are connected in the circuit. There is no neutral current in the circuit so the two capacitors are charged or discharged by the



(a) Long vector (b) Medium vector (c) small vector

Fig. 3.6. Circuit diagram for vectors and the influence on NP voltage

same current. Consequently, the long vector does not create any neutral point voltage imbalance. For the medium vector in Fig.3.6(b), the top and bottom cell capacitors are connected in the circuit as well. However, there is neutral current in the circuit and the two DC capacitors are charged or discharged by different current. The medium vector create imbalance and is the source for the neutral point voltage variation. For the small vector in Fig.3.6(c), the two switching states for the small vector V_{S0} is shown. These two switching states connect different DC link capacitors in the circuit but with the same charging or discharging current from phase A. If phase current $i_A>0$, vector ONN reduces V_{ON} and increases ΔV while POO reduces V_{PO} and decreases ΔV. Under $i_A<0$ case, the result is just the opposite. The conclusion is that the two switching states for one small vector have an opposite influence on the neutral point voltage and this is the basis to balance the neutral point voltage.

From the above analysis, it is clear that the medium and small vectors have influence on the neutral point voltage. A quantitative analysis for their influence on NP charge is then carried out. For the medium vector, the NP current is the influential factor that determines the NP charge. And the NP charge reflects the NP voltage imbalance. The six medium vectors and their corresponding neutral current are shown in Fig.3.7. Each 60º sector has its own medium vector with different neutral current. Still taking the first 60º sector as example, the NP charge by the medium vector PON can be calculated by the neutral current and the duty cycle for PON as:

$$Q_{NP\_MV} = i_b d_{PON} T_{sw} \tag{3-8}$$

The NP charge in the other sectors can also be calculated in the same way. With the information of the phase current, the line cycle NP charge by the medium vector can be calculated. It is obvious that the phase current direction, in other word, the power factor has large impact on the NP charge. The line cycle NP charge by the medium vector is shown in Fig.3.8 under different

power factor cases [19]. The NP charge is normalized into the per unit value with the rated operating condition. A low frequency NP charge ripple can be observed which essentially generates low frequency NP voltage ripple. There is a large ripple at zero power factor case and small ripple at unity power factor case. So the NP imbalance is more serious at low power factor.

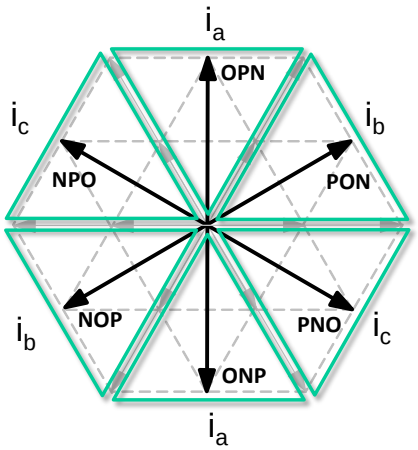
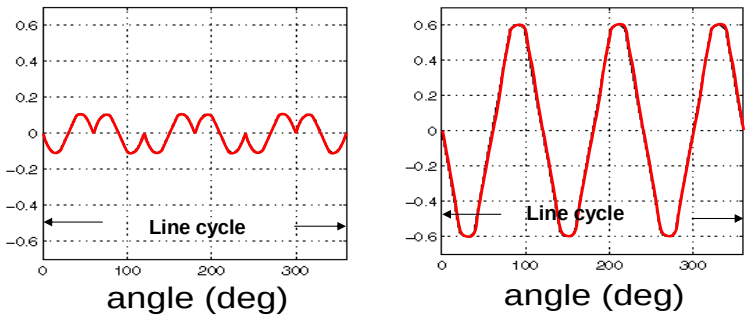


Fig. 3.7. Medium vectors in space vector hexagon and their NP current



(a) PF=1 (b) PF-0

Fig. 3.8. Line cycle NP charge by medium vector at different power factors

The influence of small vectors on the NP charge can be analyzed in the same way. The 6 small vectors with the 12 switching states is shown in Fig.3.9. The neutral current associated with the specific small vector is also identified. It is noticed that in 60° sector, there are two small vectors and each one has two switching states. So the NP charge calculation contains two parts, one from the influence of V_{S0} and one from the influence of V_{S1}. For each small vector, there are two switching states to select with either positive or negative neutral current. So the NP charge for each sector is:

$$Q_{NP\_SV} = (m_{s0} d_{s0} i_a + m_{s1} d_{s1} i_c) T_{sw}, \quad m_{S0}, m_{S1} = \pm 1 \tag{3-9}$$

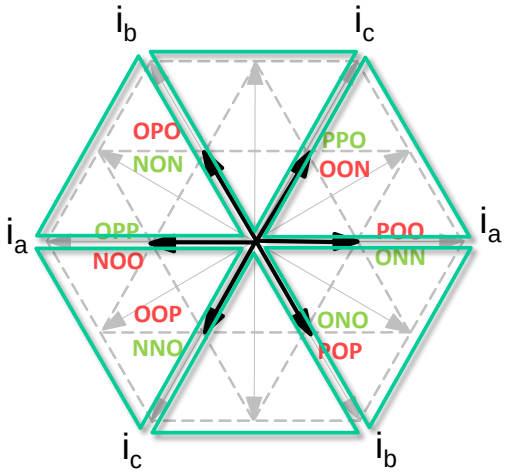
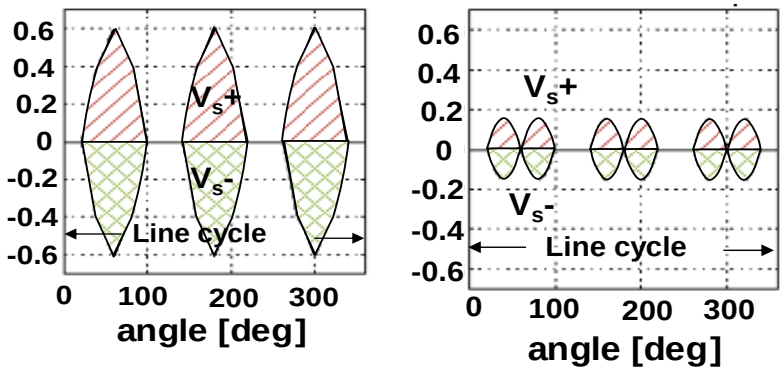


Fig. 3.9. Small vectors in space vector hexagon and their NP current

The NP charge expression for the small vector contains the coefficient m, which can be either positive or negative. This is the control freedom for NP balance. The NP charge for small vector in a line cycle is shown in the same way in Fig.3.10 [19]. If the positive switching status V_{S+} is used, then the NP charge is positive. If negative status V_{S-} is used, then the NP charge is negative. By selecting the two types of switching states, the NP balance can be achieved. Fig.3.10 shows that the small vectors have large NP charge and strong influence on NP balance at unity power factor. But for zero power factor, it has small charge and weak influence on NP balance. However, the imbalance brings by the medium vector is just the opposite. The NP charge imbalance by the medium vector is strong at low power factor while the control freedom by the



(a) PF=1 (b) PF-0

Fig. 3.10. Line cycle NP charge by small vector at different power factors

small vector is weak. This means an intrinsically large NP voltage ripple at low power factor case. The lower the power factor is, the higher the NP voltage ripple is.

The two switching states for one small vector have an opposite influence on the NP voltage and this is the basis to achieve the NP balance. There are three approaches to select the small vectors for NP balance. The passive balancing method alternately uses the two switching states in a pair in each switching cycle. Since the influence of the two states are opposite, the neutral point voltage can be balanced naturally. This method does not need to sense the neutral point voltage and phase current. Also it does not cause extra switching events and related loss in the switching cycle. But the balancing result largely relies on the power factor. Also it can only work under a balanced 3-phase system and the balancing result is poor under system dynamics.

The active balance scheme uses both two switching states for the small vector in each switching cycle. Fig.3.11 uses the region II in Fig.3.5 to illustrate the concept. The gist of this control scheme is to achieve a net zero neutral point charge in one switching cycle so that ΔV returns to the initial value after the switching cycle. For each small vector, the two switching states are used with different duty cycle to achieve net zero NP charge. The charge is calculated by sensing the phase current and knowing the duty cycle of each vectors. The duty cycle ratio for the two switching states in the pair is solved by the following equations:

$$\Delta Q = [i_a d_{POO} + i_c d_{OON} - i_a d_{ONN} - i_c d_{PPO} - i_b d_{PON}]T_{sw} = 0 \quad (3\text{-}10)$$

$$d_{POO} + d_{ONN} = d(V_{s0}), d_{PPO} + d_{OON} = d(V_{s1}) \quad (3\text{-}11)$$

The active scheme has a perfect balancing result within one switching cycle. However, it uses both two switching states for each small vector in the switching cycle. The transition between the two switching states inevitably introduces extra switching events as in Fgi.3.11. The result is an increased switching loss for the power stage. Also the implementation for this control scheme is complex with large computation cost for zero NP charge in each switching cycle.

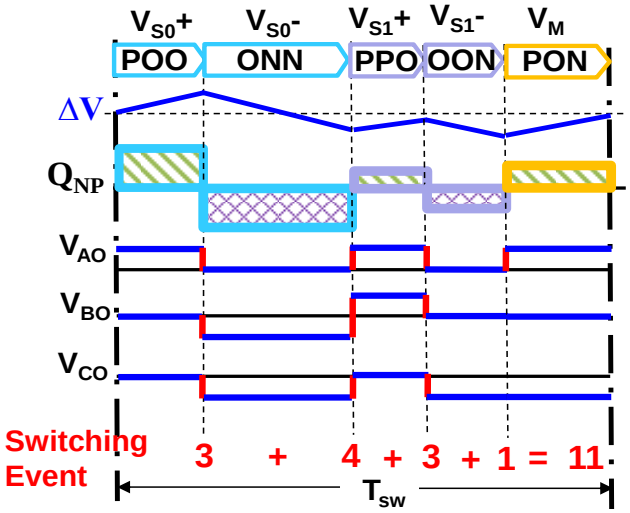


Fig. 3.11. NP voltage & current for active balance scheme

Compared with the active balance scheme which uses both switching states and tries to balance NP voltage in every switching cycle, the hysteresis balance scheme balances the NP voltage in two or more switching cycles by using only one switching state for the small vector in each switching cycle. Fig.3.12 also uses the same triangle region II to show the concept for hysteresis balance. The selected small vector moves the neutral point voltage to the opposite direction of the imbalance. In each switching cycle, the neutral point voltage ΔV is sensed together with the 3-phase current. The switching state for small vector is selected based on the ΔV and the phase current direction. If ΔV is positive at the beginning of the switching cycle as Fig.3.12 shows, than the switching state is selected to bring down the NP voltage. In the next switching cycle, if ΔV is reduced to negative value, then the other switching state for the same small vector is used to increase NP voltage. If one cycle is not enough to control the NP voltage, this method will use the same switching state continuously for several cycles to control the NP voltage. This method is robust to the system dynamics because it has neutral voltage feedback. The NP balancing result is not as good as that of the active scheme since the neutral point voltage is controlled back and forth around zero. The NP voltage also has a strong harmonic component at half of the switching frequency. But this method can still achieve NP balance

within several switching cycles. It has the benefit of having the least switching events because it only uses one switching state in each switching cycle.

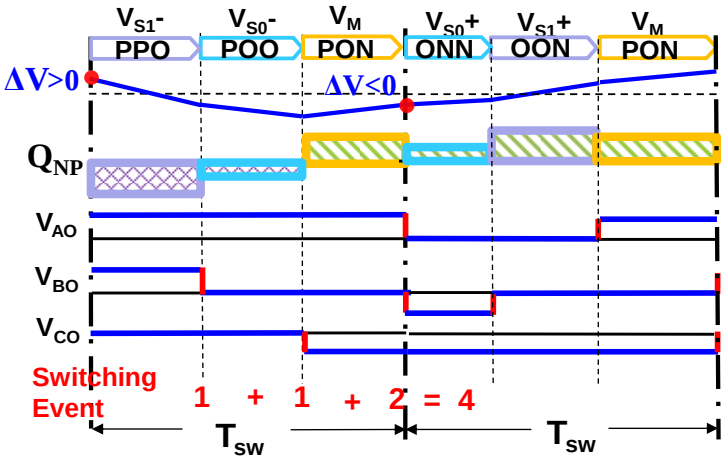
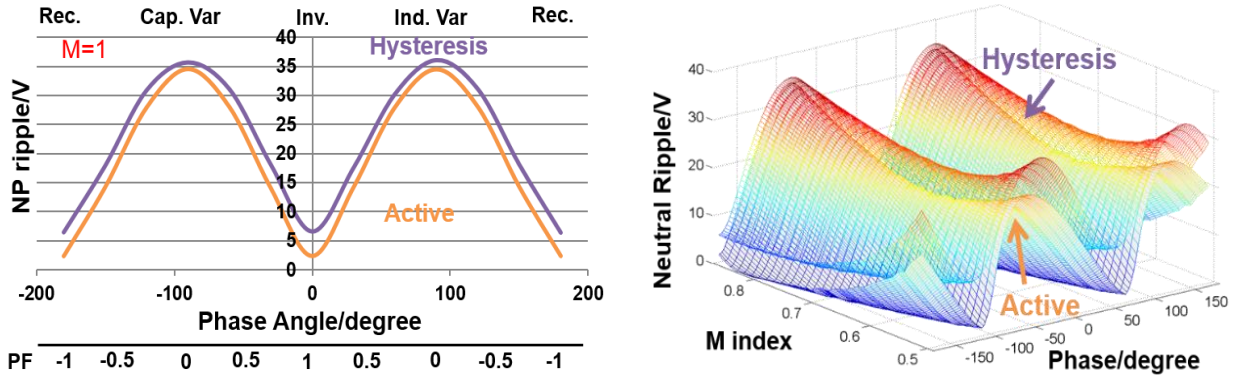


Fig. 3.12. NP voltage & current for hysteresis balance scheme

Finally, different NP balance schemes are compared together. The comparison is based on the simulation of the power conversion system and also the loss model. The DC link voltage is 1200V and DC link capacitor is 2.5mF, which is the rated value for the PCS. Fig.3.13 shows the maximum NP voltage ripple comparison for the two schemes under different power factors and modulation index. The power factor is defined at the output of converter phase leg in this case.



(a) NP voltage with power factor

(b) NP voltage with power factor and modulation index

Fig. 3.13. NP voltage ripple comparison with power factor and modulation index

The figures show the intrinsically large NP voltage ripple at low power factor case. The in-depth explanation for this pheromone is described earlier. The comparison shows the active NP balance scheme has a slightly small voltage ripple at all power factor and modulation index cases. On the

other hand, the total system loss for the two scheme is also quantified by the loss model and displayed in Fig.3.14. It clearly shows the two schemes have basically the same conduction loss. But active balance scheme has excessive switching loss due to the transition between several switching states. The hysteresis balance scheme on the other hand has far smaller switching loss.

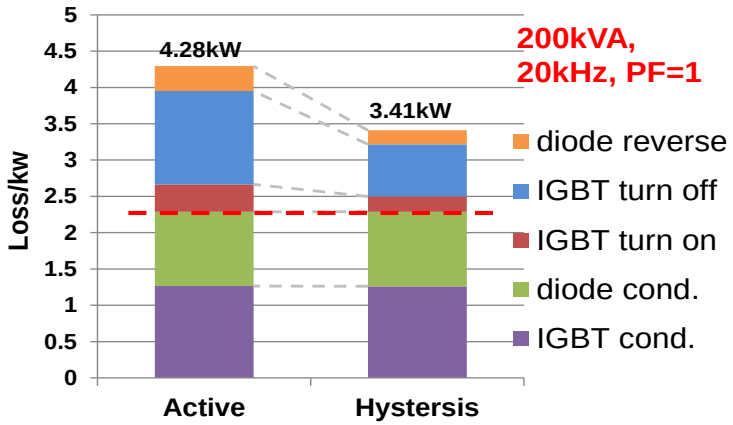


Fig. 3.14. Total system loss comparison for two NP balance schemes

The above comparison shows a distinctive trade-off between the NP voltage ripple and switching loss for the active and hysteresis balance scheme. Other features for all the three balance schemes are also compared in Table.3.2. The active and hysteresis scheme with feedback has a better balance result under dynamics and unbalanced system. But they are consequently more complicated in the control algorithm. The hysteresis scheme has a good balance result and the least switching loss. Therefore it is chosen as the basis for the NP balance scheme proposed later in this chapter.

Table 3.2. Comparison for three NP balance schemes

Scheme	Sensors	NP ripple	Complexity	Loss
Passive	No	large	low	low
Hysteresis	i_{abc}/V_{dc}	small	medium	low
Active	i_{abc}	smallest	high	high

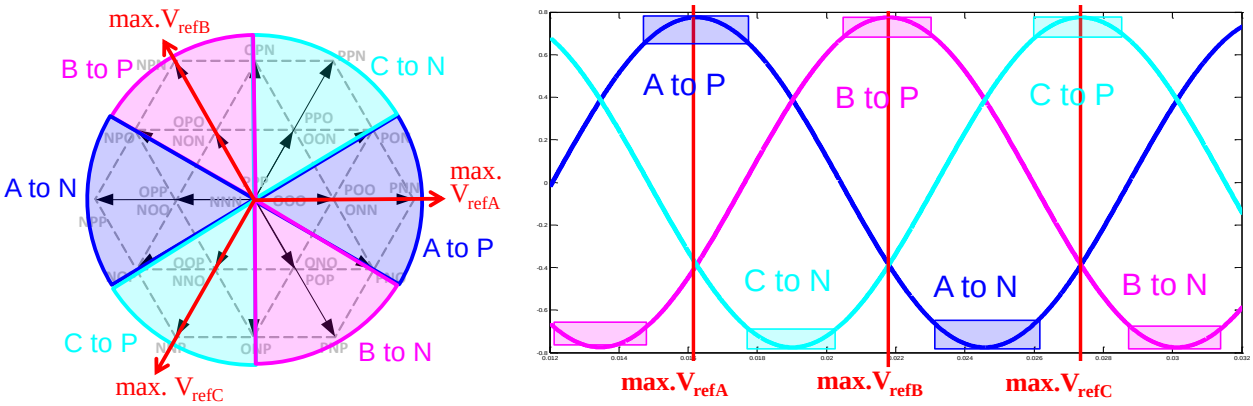
3.2.2 Method 2: Switching Loss Reduction

The redundant switching states can also be used for the switching loss reduction. The basic principle for this control objective is to clamp the phase leg for a certain period of time, so that

the phase leg with the largest current can avoid switching. Each phase leg can save some switching loss during the clamped period. This method is actually a discontinuous PWM (DPWM) method. With this method, the three phases take turns to be clamped for certain period of time in the line cycle. There are some variations on the clamping methods and they are similar to the DPWM for the 2-level voltage source converter. The phase leg can be clamped for 60° or 30° in a line cycle. Each leg can be clamped to positive, negative or neutral rail. Among all these combinations, the meaningful one should give sinusoidal line to line output without distortion. To achieve the DPWM with space vector based method, the redundant switching states of the small vectors are the key to be played with. Several different space vector based DPWM methods are introduced and compared in the following.

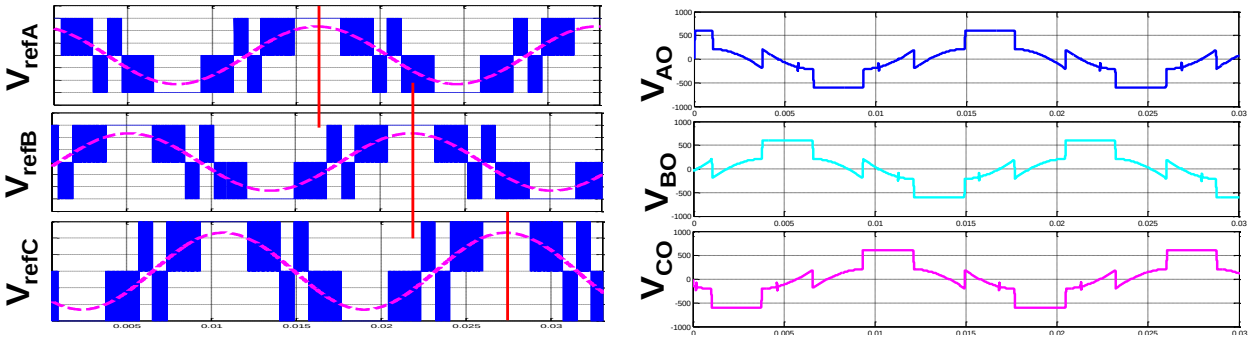
The most commonly used DPWM method for both 2-level and 3-level converter is the 60° DPWM that clamps each phase leg for 60° near its voltage reference peak. This method can avoid the phase leg switching in the vicinity of its maximum voltage reference. The space vector hexagon division for this method is given in Fig.3.15(a). The hexagon is equally divided into six sectors. Each sector is center aligned to the peak or valley of the phase leg reference voltage as shows in Fig.3.15(b). The shaded areas on the voltage reference waveform is the clamped period. By properly select the switching states for the small vector, each phase leg is clamped to P or N in consecutive 60° area. The 3-phase output voltage and reference voltage waveforms are displayed in Fig.3.16(a). Each phase is clamped to the peak and valley of its reference voltage.

For the positive half line cycle, the phase leg is clamped to the positive rail. And for the negative half line cycle, it is clamped to the negative rail. Fig.3.16(b) gives the switching cycle moving average of the phase leg output voltage over a line cycle. The results are actually the equivalent reference voltage for each phase leg. This equivalent reference voltage can be derived



(a) Space vector hexagon division (b) Clamped voltage reference area

Fig. 3.15. Space vector hexagon and voltage reference for 60° DPWM method 1



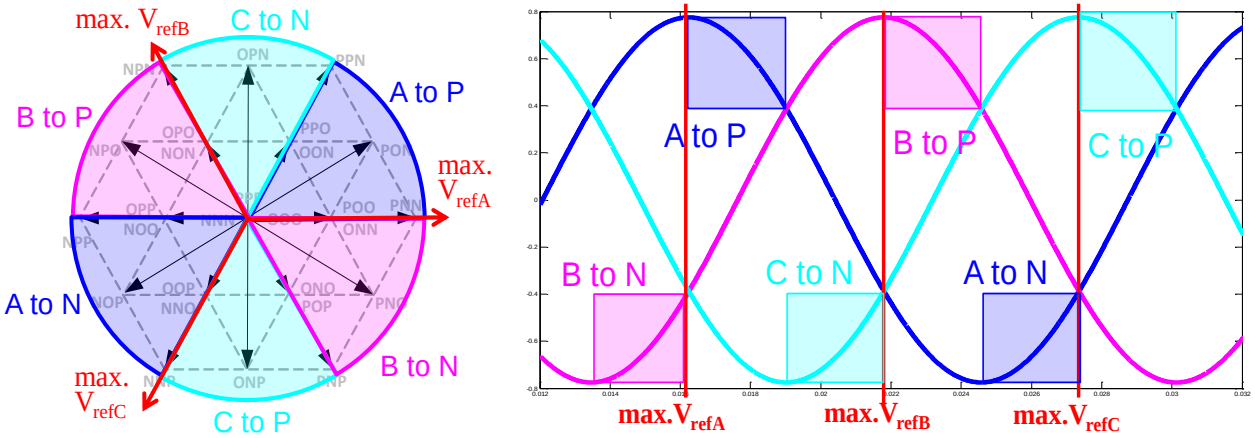
(a) Phase leg output voltage and reference voltage (b) Moving average of phase leg output voltage

Fig. 3.16. Phase leg voltage and its reference for 60° DPWM 1

by injecting a zero sequence component into the sinusoidal reference voltage. This is the carrier based approach to achieve this DPWM strategy. Under the unity power factor case, when the current is in phase with the reference voltage, this method gives the minimum total loss by clamping the phase leg with the maximum current. But at non-unity power factor case, the loss reduction result is not as prominent as the unity power factor case. Also it can be noticed from Fig.3.15(a), the sector division method for this DPWM splits the inner triangles of the NTV by two. In the real implementation, there are different switching states with the same NTV in the inner triangles. It cuts the naturally divided space vector triangle by half and therefore increases the implementation complexity.

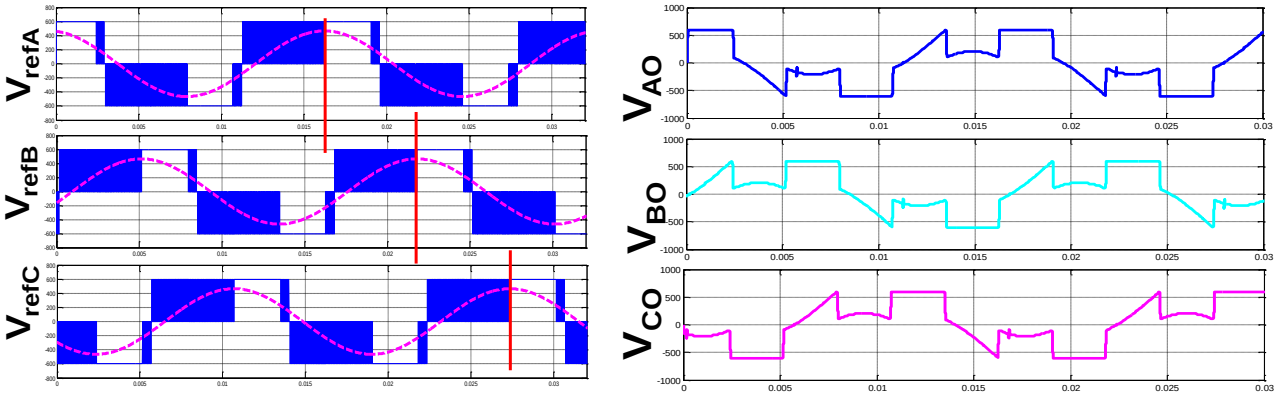
There are some other 60° DPWM methods to simplify the implementation. One method clamps the phase leg output for 60° after its reference voltage peak and valley. The space vector

hexagon for this method is given in Fig.3.17(a) and the 3-phase voltage reference waveforms are shown in Fig.3.17(b). The space vector hexagon shows that this method keeps the integrity of the naturally divided triangles for the NTV. The phase leg output voltage waveform is shown in Fig.3.18(a). Each phase leg is clamped right after its reference voltage peak or valley. The moving average of the phase leg output is given in Fig.3.18(b). It can still be derived as the summation of the zero sequence voltage and the 3-phase sinusoidal reference voltage. But the equivalent reference voltage is not symmetrical to its peak anymore. Also there is another variation of this method by clamping the phase leg for 60° right before the reference voltage peak or valley. The result is similar and is not reported here.



(a) Space vector hexagon division (b) Clamped voltage reference area

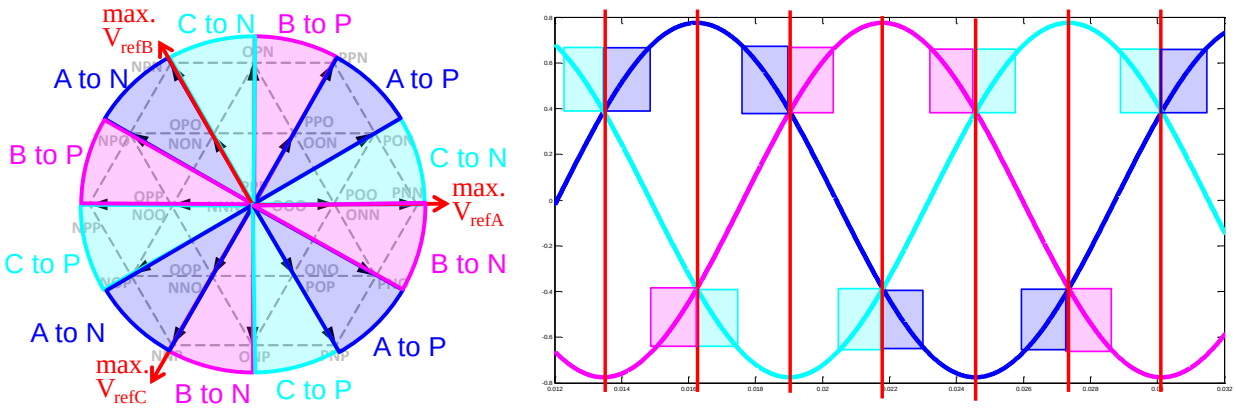
Fig. 3.17. Space vector hexagon and voltage reference for 60° DPWM method 2



(a) Phase leg output voltage and reference voltage (b) Moving average of phase leg output voltage

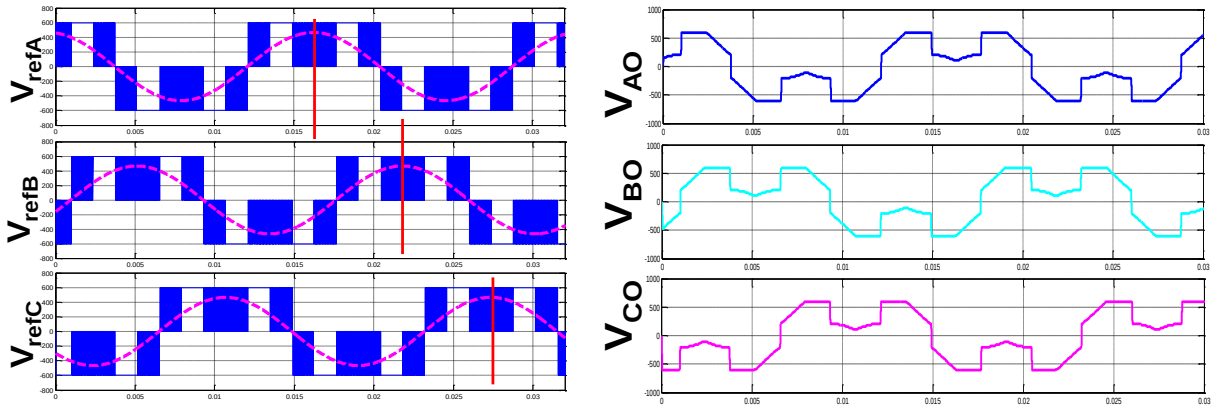
Fig. 3.18. Phase leg voltage and its reference for 60° DPWM 2

The 30° DPWM method is also explored and introduced here. The space vector hexagon and the 3-phase voltage reference is given in Fig.3.19(a) and (b). This method divides the space vector hexagon into 12 sectors. Each phase leg is clamped four times in the line cycle, two times to the positive and two times to the negative. The 3-phase output voltage waveforms and their moving average are given in Fig.3.20(a) and (b). It shows that the clamped region for each phase leg is symmetrical to the reference voltage peak and valley. As a result, the equivalent reference voltage for this modulation is symmetrical.



(a) Space vector hexagon division (b) Clamped voltage reference area

Fig. 3.19. Space vector hexagon and voltage reference for 30° DPWM

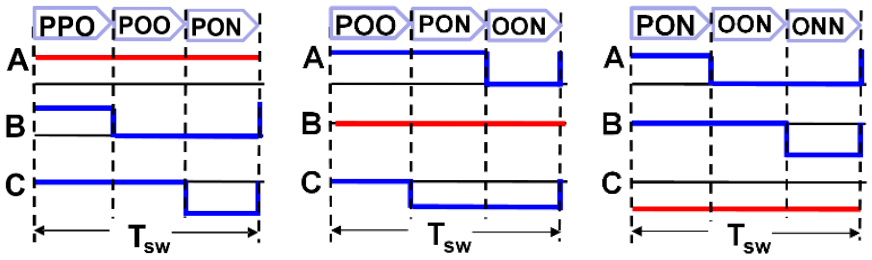


(a) Phase leg output voltage and reference voltage (b) Moving average of phase leg output voltage

Fig. 3.20. Phase leg voltage and its reference for 30° DPWM

All the aforementioned methods clamp the phase leg output according to its reference voltage. The switching states selection for the small vector is predetermined in each sector. These methods has relatively simple implementation with fixed switching states for small

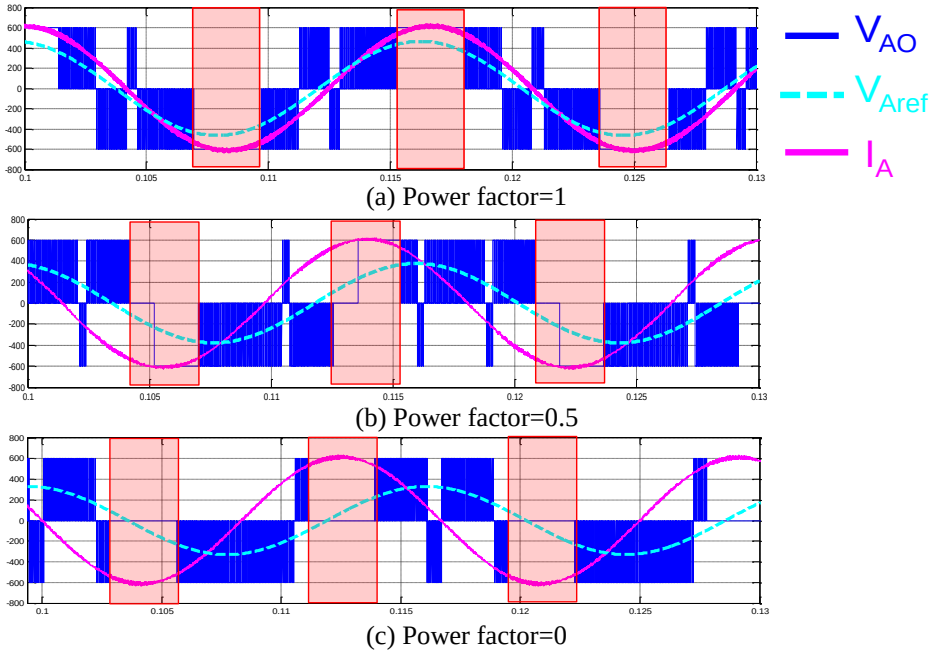
vectors. But the loss reduction result may vary with the power factor, which is determined by the phase angle between the current and the voltage reference. Therefore, a space vector modulation for minimum loss is proposed based on the DPWM concept. The phase legs are still clamped for 60° twice in a line cycle. But they are clamped to their current peak, not reference voltage peak. This method guarantees that the phase leg with the maximum current is clamped and therefore it reduces the switching loss to the minimum. The switching states for small vectors are no longer fixed, but are selected based on the phase current information. Still taking the first 60º sector in the space vector hexagon in Fig.3.5 as example. For the triangle regions I and II, which contain two small vectors in its vertexes, each of the three phases can avoid switching in one cycle. Considering region II, if the current in phase A is the largest among the three phases, then the small vectors POO, PPO are selected together with the medium vector PON to keep phase A stay at positive as shown in Fig.3.21(a). If phase B has the largest current, then OON and POO are selected with PON so that Phase B can stay at the neutral as shown in Fig.3.21(b). It is the same case if phase C carries the largest current. The pulse sequence is shown in Fig.3.21(c). For region III and IV, which contain only one small vector, the redundant switching state can only avoid the switching for one phase current out of two phases instead of three phases. In these regions, the control law only switches the relatively smaller current, not necessarily the smallest among the three phases. Considering region III as example, the small vector can only keep phase A or phase C unchanged in the switching cycle. If phase A has a larger current, then the small vector PPO is



(a) Phase A not switched (b) Phase B not switched (c) Phase C not switched

Fig. 3.21. Switching sequences for loss reduction method

selected together with the long vector PPN and medium vector PON. Fig. 3.22 gives the phase leg output voltage and phase current waveform at different power factor cases. It shows that each phase leg is clamped for 60° degree around its current peak, regardless of the voltage reference waveform. By selecting the switching states for small vectors based on the current feedback, this method avoids the switching of the larger phase current and hence gives the minimum total loss.



(a) Power factor=1

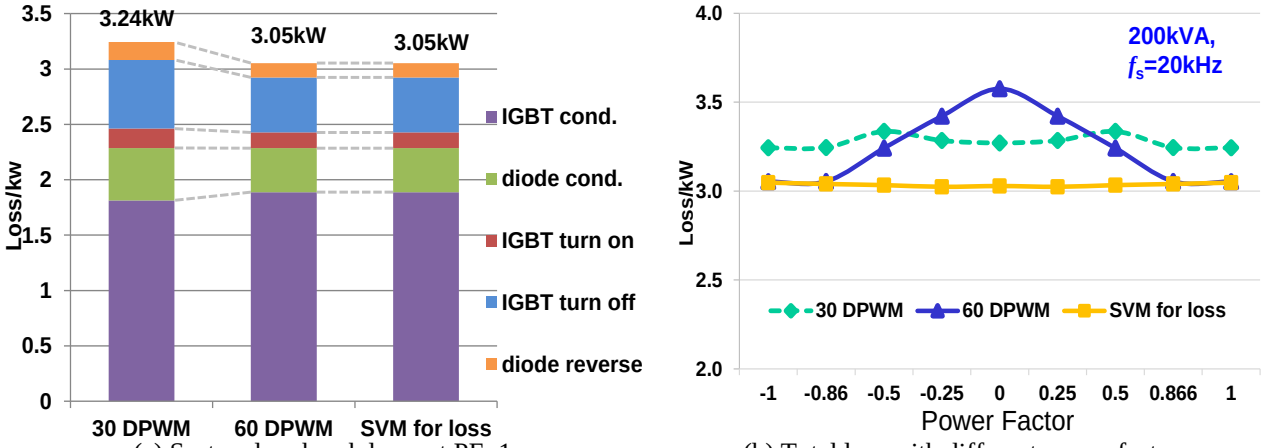
(b) Power factor=0.5

(c) Power factor=0

Fig. 3.22. Phase leg output voltage and current for SVM with min. loss

Since the DPWM methods feature on the loss reduction, the total system loss for the different DPWM methods are compared. The 60° DPWM method 1, the 30° DPWM and the SVM for minimum loss are compared in Fig.3.23 in terms of system total loss. Fig.3.23(a) gives the total system loss break down comparison at unity power factor. Under this case, the SVM for loss equals to the 60° DPWM method 1 because the voltage reference is in phase with the current. The 60° DPWM method 1 has the minimum loss at this time. Fig.3.23(b) gives the total system loss at all power factor cases for the three methods. The 60° DPWM method 1 has different total loss that varies with the power factor. The proposed SVM for loss has constant minimum loss over all power factor ranges since it clamps the maximum phase current. The 30° DPWM also

has nearly constant system total loss. But the total loss is higher than the SVM with minimum loss. Although the DPWM has excellent loss reduction result, it causes too much NP voltage ripple since only one switching state for the small vector is used in 60° sector. The loss and neutral point voltage ripple comparison with other SVM methods is given later in chapter 3.2.4.



(a) System loss breakdown at PF=1 (b) Total loss with different power factors

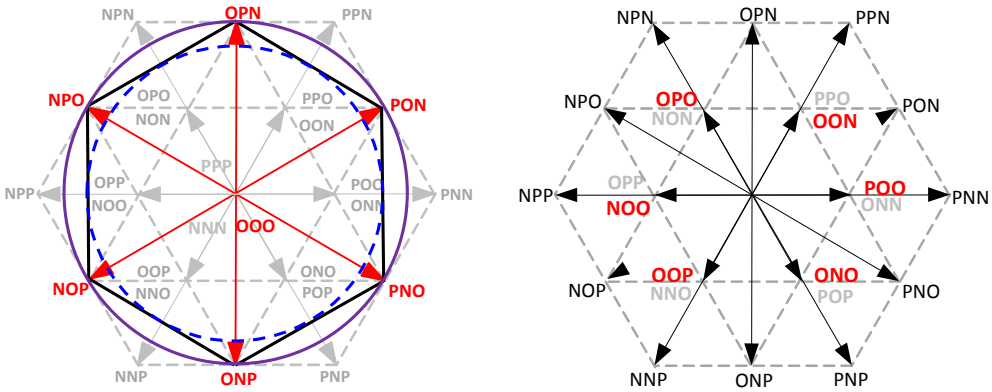
Fig. 3.23. System loss comparison for different DPWM methods for loss

3.2.3 Method 3: Common Mode Voltage Control

Besides the NP voltage ripple and switching loss, the common mode voltage can also be reduced or even eliminated by the redundant small vector selection. The switching behavior of the 3-level NPC phase leg creates common mode noise, which can generate large common mode current on the output if there is not enough common mode impedance presents in the circuit. The common mode noise issues can deteriorate the output current waveform and also cause extra loss on the power stage. To deal with the CM noise issue, the noise propagation path and the noise source should be considered. The solutions for CM noise include increase the common mode impedance in the path or suppress the noise source. The switching behavior of the modulation is the noise source. For the 3-phase system, the CM voltage is defined as one third of the summation of the three phase output voltage:

$$V_{CM} = \frac{1}{3}(V_{AO} + V_{BO} + V_{CO}) \tag{3-12}$$

The CM voltage generated by the different types of vectors can be calculated by this equation. The long vectors generate $\pm 1/3V_{dc}$ CM voltage, where V_{dc} is half of the DC link voltage. For the medium vectors, they generate no CM voltage. For the small vectors, the two switching states generates different CM voltage. They give either $\pm 1/6V_{dc}$ or $\pm 1/3V_{dc}$ CM voltage. For the zero vectors, they generate either $\pm V_{dc}$ or 0 CM voltage. There are two methods to deal with the CM noise. The CM elimination method can totally avoid CM noise generated by the modulation. It only uses the medium vectors and the zero vector OOO since they don't generate any CM voltage. The vector diagram for this method is shown in Fig.3.24(a). The vectors in red color is the usable vectors for this method. By using only the medium and zero vectors, this method can totally eliminate the CM voltage noise. But it reduces the DC link voltage utilization rate from the original circle with solid line in Fig.3.24(a) to the circle with dashed line in the same figure. The implementable V_{ref} trajectory for conventional SVM is the inscribed circle of the large space vector hexagon, whereas the V_{ref} trajectory for CM elimination method is the inscribed circle of the hexagon with the medium vector as its vertex. The radius for the V_{ref} vector is reduced from 1 to $\sqrt{3}/2$. By using only the medium vector to synthesis the V_{ref}, this method lose the benefit of the nearest three vectors. Each phase leg has more switching events and higher switching loss associated with the switching. Additionally, due to the influence of the dead-time, the CM noise



(a) Common mode elimination method (b) Common mode reduction method

Fig. 3.24. Two methods for common mode noise control

can not be totally eliminated. Another method to deal with the noise is the CM reduction method. It uses the nearest three vectors for V_{ref}. This method is also bases on the redundancy of the small vector switching states. Since the two switching states have different CM voltage, the one with smaller CM voltage of $\pm 1/6V_{dc}$ is selected as shown in Fig.3.24(b). The output CM noise is reduced but not totally eliminated. This method has limited reduction of CM noise but has small loss and dv/dt. The CM noise control result is also measured and is shown in the following part.

3.2.4 Comparison and Summary between Small Vector Selection Criteria

Finally the different control objectives are compared together. The aforementioned SVM strategies for NP balance, loss reduction and CM noise reduction are compared with the SPWM as a benchmark. The comparisons are based on the NP voltage ripple, total system loss and the common-mode noise spectrum. For neutral point balance control, the hysteresis balance scheme with best loss and balance trade-off is used. For the loss reduction control, the SVM with minimum loss is used with phase legs clamped for 60° based on current feedback. For the CM noise control, the CM noise reduction method is used. These three modulation strategies are evaluated and compared on their NP ripple and loss.

The neutral point voltage is first compared since it is the foundation to ensure the proper function of the converter. Fig.3.25 compares the inverter output voltage and the neutral point voltage waveform for different modulation methods. The comparison is based on a 1200V DC link voltage and a 2.5mF DC link capacitor with unity power factor. This is the rated value for the power conversion system. The SVM for NP balance has the smallest NP voltage ripple which is below 3V. The NP balance is achieved within switching cycle. On the contrary, the SVM for loss reduction and CM noise reduction have a very large NP voltage ripple and the output voltage waveform is even distorted. This is because these modulation methods select the small

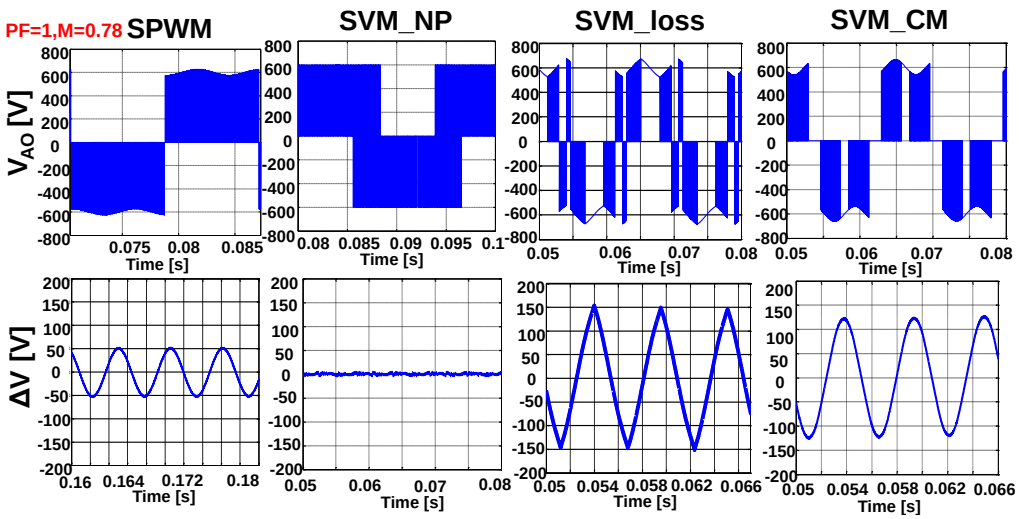


Fig. 3.25. NP voltage waveform comparison for different modulation methods

vector only for the loss or noise reduction. The selected small vectors are the same for 60° sector. They charge or discharge one DC link capacitor for a consecutive 1/6 line cycle. The result is a large low frequency NP voltage ripple as shown in the figure. It shows that the voltage ripple for these two modulations is even larger than the naturally balanced SPWM. Because the NP balance is critical to the converter performance, the small vector selection for loss or noise reduction is not practical unless the DC link capacitor is large enough or the two DC link cells are supported with two separate DC sources so that the ripple can be avoided. The SVM for NP balance method has 3V NP voltage ripple with 2.5mF DC link capacitor. For the SVM for loss reduction method, to achieve the same small NP voltage ripple, the DC link capacitor should be increased to 100mF. Yet the SVM for NP balance has high frequency ripple while the SVM for loss reduction has low frequency ripple. So the size and cost for such a large capacitor with low frequency voltage ripple is an issue. The maximum peak to peak NP voltage ripple at different power factor cases are also compared in Fig.3.26. It clearly indicates that the SVM for NP balance has the lowest ripple amplitude at all power factor range. The SVM for loss and SVM for CM noise have large NP voltage ripple that is even larger than the SPWM method. Also these two methods give low frequency ripple which increases the capacitor size. In conclusion, the

SVM for loss method and SVM for CM reduction has unacceptable large NP voltage ripple at low frequency if the DC link capacitor is not large enough.

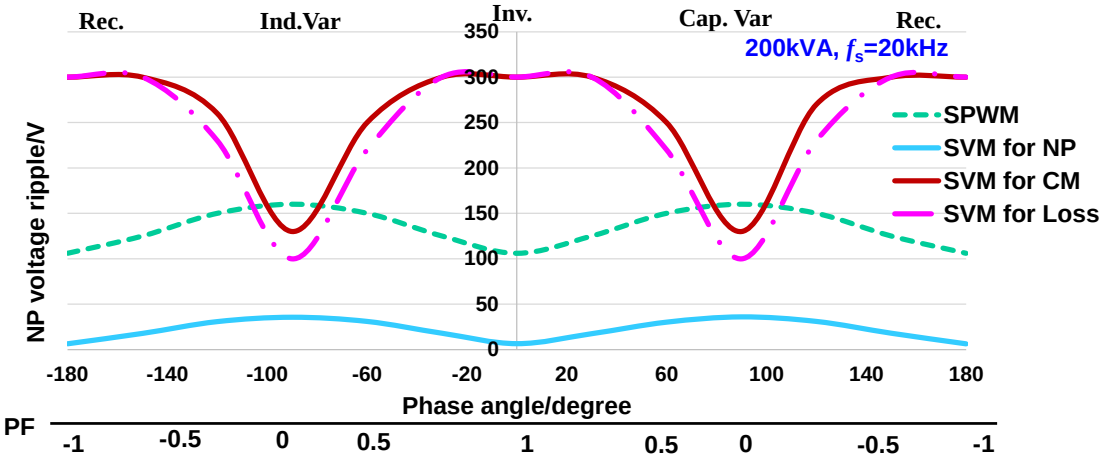


Fig. 3.26. NP voltage ripple comparison at all power factors

The system total loss under unity power factor and unit modulation index in line cycle is compared in Fig.3.27 for different modulation methods. The conduction loss below the red dotted line in the figure for all the methods are the same. However, the switching loss is largely reduced if the small vectors are used for the purpose of loss reduction. For SVM with CM loss reduction, the small vectors are predetermined. But for SVM with NP balance, the small vectors are selected based on the balance scheme and NP voltage feedback. Therefore, the SVM with NP balance has a larger switching loss due to the extra switching events for switching state change.

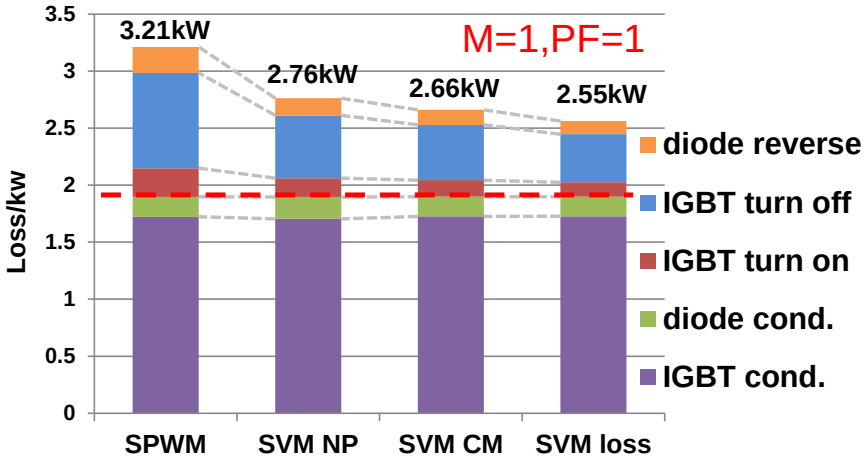
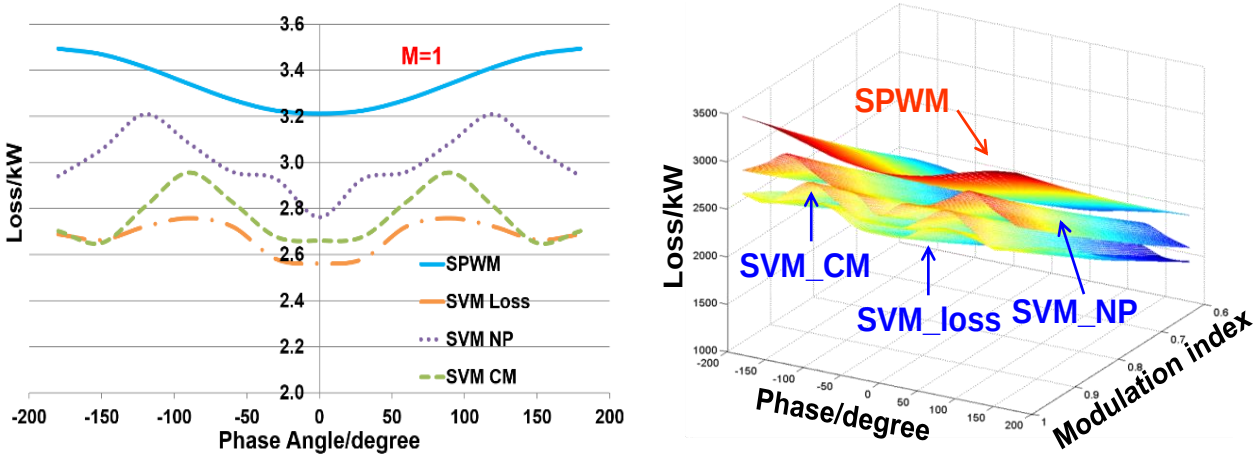


Fig. 3.27. System loss breakdown for all modulation methods

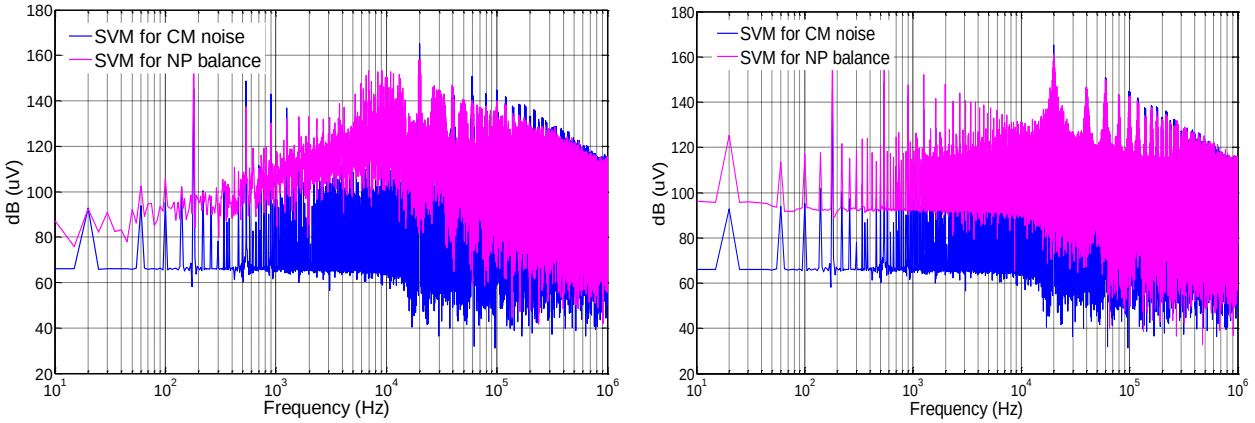
Fig.3.28 shows the same loss comparison under all power factors and modulation index. Fig.3.28(a) gives the loss curve for all modulation methods at all power factor with unity modulation index. Fig.3.28(b) shows the 3-D loss surface under all power factors and modulation index. The SVM with loss reduction still has the lowest loss under all power factors. Unity power factor is the best case for loss reduction result.



(a) Total loss with power factors (b) Total loss with power factor and modulation index

Fig. 3.28. Total loss comparison with power factor and modulation index

The CM noise reduction result for all these methods are finally compared. The CM voltage spectrum for the NP balance SVM and the CM noise reduction SVM is compared up to 1MHz under the unity and zero power factor case. The spectrum is shown in Fig.3.29. The SVM with CM noise reduction has less noise in the whole frequency range when compared to the SVM for



(a) CM voltage spectrum at PF=1 (b) CM voltage spectrum at PF=0

Fig. 3.29. CM voltage spectrum comparison under different power factors

NP balance. The CM reduction method works for both unit and zero power factor cases but the unbalanced NP voltage is an issue for this method. The voltage ripple is extremely large because the small vectors are used for noise reduction. Therefore, this method is not practical unless large capacitor is used to support the DC link voltage.

Finally, the conclusions are given for the redundant switching state selection of the small vector. The major control objectives like NP voltage balance, loss reduction and CM noise reduction are provided by the small vector redundancy. The variation in the small vector selection methods generate different SVM strategies. Since the NP voltage balance is critical to maintain a good output voltage and current waveform and it largely determines the output THD, it is considered as the control priority. Also from the quantitative analysis for the NP balance and loss trade-off, it can be clearly demonstrated that the NP voltage ripple for the loss reduction and CM noise reduction method is too large to be accepted. For this reason, the small vector is selected based on the NP voltage balance. The hysteresis balance scheme in 3.2.1 is used.

3.3 Pulse Sequence Alignment Patterns

The above analysis shows different control objectives for the SVM. The key to achieve these objectives is the switching states selection for the small vectors. Because the control freedom can only achieve single objective and the neutral point voltage balance is essential for the converter, most of SVM use the freedom to achieve NP balance. However, the loss and efficiency is also critical for the high frequency converter. This gives the motivation to improve the SVM to achieve both NP voltage balance and loss reduction at the same time. A number system is first introduced for simplification and expression convenience. The switching states P-O-N are coded with number 2-1-0 respectively. Then the vectors can be labeled with the number code and can also be expressed by the summation of the switching state code for the three phases. For the first

60º sector in the space vector hexagon, the number expression of each vector is shown in Fig.3.30. Taking small vector OON as an example, the number code for it is 110 and the vector can be labeled as V2 (1+1+0).

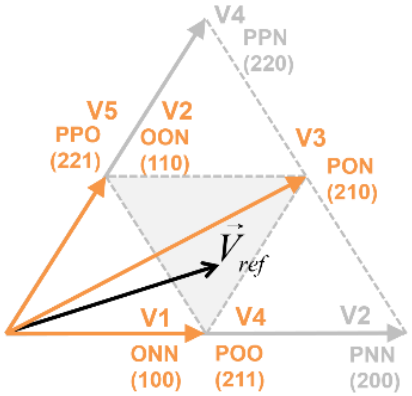
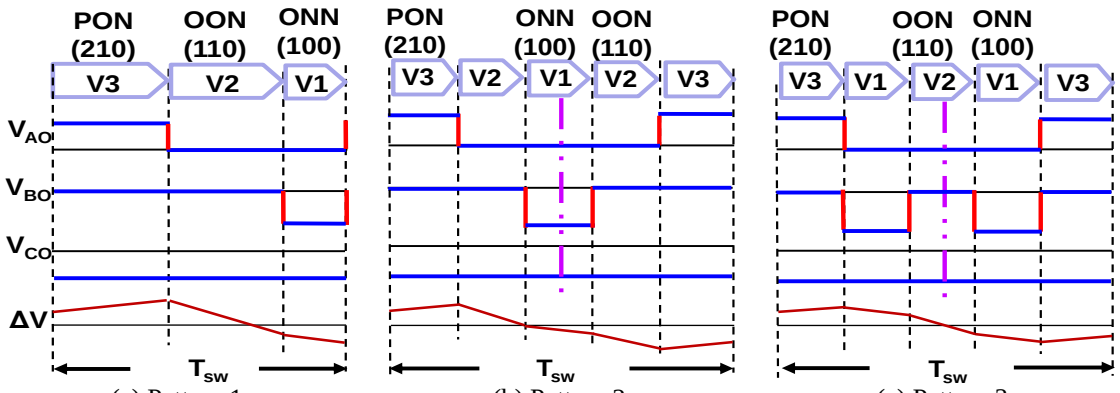


Fig. 3.30. Number code system for 60° sector

To achieve the NP voltage balance, the hysteresis balance scheme is used for switching state selection as this method uses only one switching state in each switching cycle and thus has less switching events. Although the freedom for the small vector is used for the NP balance, the switching loss can still be reduced by proper pulse sequence alignment, which is another control freedom for SVM. With the nearest three vectors determined by the NP balance scheme, the pulse sequence can be aligned in different manners. It can be symmetrical or asymmetrical in one switching cycle. The pulse can also be arranged with certain order. The different pulse sequence results in different THD and switching events in one cycle. Taking the shaded area in Fig.3.30 as an example, and assuming ONN and OON are selected as small vectors by the NP balance control, different switching patterns and their NP voltage are shown in Fig.3.31. For pattern 1 in Fig.3.31(a), there are three segments of switching states in the switching cycle. The nearest three vectors are applied one by one. For pattern 2 and 3 in Fig.3.31(b) and (c), they are symmetric in one switching cycle. Two of the NTVs are divided into two parts and are aligned symmetrically to the center. These alignments have five segments in one cycle. The difference between pattern

2 and pattern 3 is the sequence order for the five pieces. Pattern 2 in Fig.3.31(b) has only 4 switching events per cycle while pattern 3 in Fig.3.31(c) has 6 events.



(a) Pattern 1 (b) Pattern 2 (c) Pattern 3

Fig. 3.31. Pulse sequence alignment patterns for hysteresis NP balance

The grid current THD for these alignments are compared under different power levels together with the SPWM as a benchmark. The converter is connected to the LCL filter. The THD is calculated up to 50 kHz. The result in Fig.3.32 shows that the symmetric sequence of pattern 2 has a smaller THD compared with the asymmetric sequence of pattern 1 at all power level. The SPWM method is also a symmetric sequence but has more switching events in each cycle, therefore it has a THD in between the symmetric and asymmetric sequence.

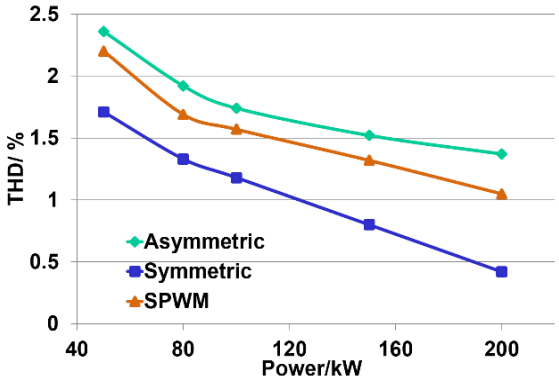


Fig. 3.32. Grid current THD for different pulse sequence patterns

Different pulse sequences also cause different switching events in the cycle. In the number system for vectors, it is easily noticed that the transition between vectors with an adjacent number has only one switching event. For example, the transition from V3 (PON) to V2 (OON)

only causes switching from P to O in phase A. To minimize the switching events for loss and dv/dt reduction in each cycle, the vectors is sequenced in an order of consecutive vector number and only the vectors with adjacent number are involved. The pulse sequence patterns in Fig.3.31(a) and (b) are arranged with the above order and the sequence in Fig.3.31(c) does not follow the above order. It is clearly shown that the sequence with order only has 4 switching events in one cycle, which is the least that can ever be achieved for the 3-level NPC modulation. In contrast, the sequence without order has 2 more switching events every cycle. This introduces an enormous switching loss and dv/dt for the high frequency high power NPC converter. The system total loss can be minimized by arranging the pulse sequence in the manner with the least switching events. A system loss breakdown for the converter at rated power is shown in Fig.3.33 to compare the loss reduction result for the different pulse sequence patterns. The loss reduction result is also summarized in Table.3.3. The result shows a 53% switching loss reduction and 0.5% efficiency improvement for the pulse sequence pattern 2 compared to the SPWM method.

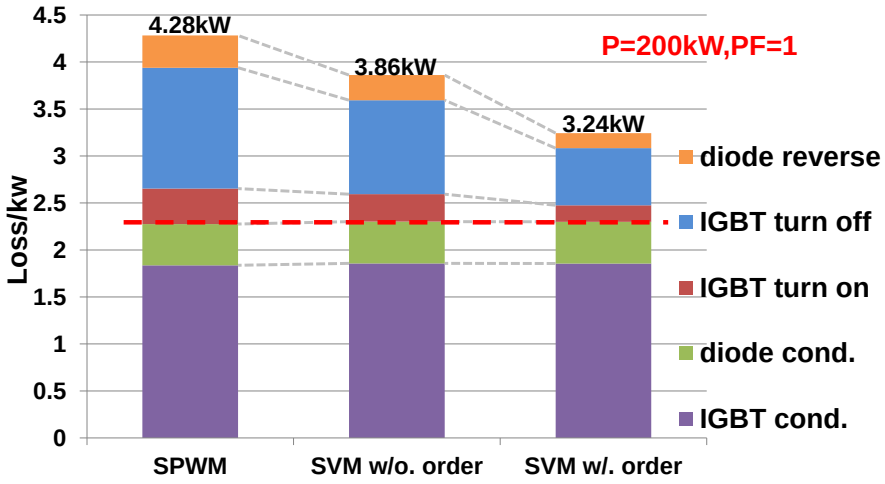


Fig. 3.33. System loss breakdown for 3 pulse sequence patterns

Table 3.3. Loss reduction result comparison for pulse sequence patterns

	P_{sw}/kW	P_{cond}/kW	P_{total}/kW	η
SPWM	2.01	2.27	4.28	97.8%
Pattern2	1.56	2.30	3.76	98.0%
Pattern3	0.94	2.30	3.24	98.3%

3.4 Proposed SVM for NP Balance and Loss Reduction

3.4.1 Issues with Conventional SVM for NP Balance

The above pulse sequence example is based on an arbitrary small vector selection given by the hysteresis NP balance. As mentioned before, this NP balance scheme relies on the phase current and NP voltage information for small vector selection. For the bidirectional power conversion system, various small vector combinations are possible in different power factor cases. In the shaded triangle area in Fig.3.30, if the small vector PPO (V5) and ONN (V1) are selected together with the medium vector PON (V3), the pulse sequence can only be aligned in a new pattern in Fig.3.34. Even if the pulse sequence alignment considers the vector number order, the order is not consecutive and therefore, the switching events in one cycle are doubled. With this new pattern, the minimum switching events are 8 instead of 4. This is because the small vectors are selected only based on the NP voltage balance without considering the pulse sequence order. To explore the operating condition under which the undesired scenario can happen, switching states combinations for the small vectors are considered under different phase

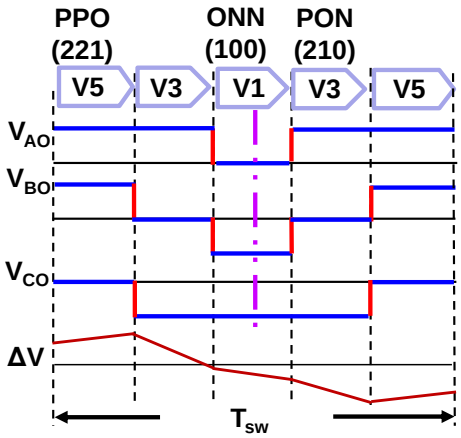


Fig. 3.34. Pulse sequence pattern 4

current as noted in the shaded area in Fig.3.30. In this region, phase A and phase C are connected to the neutral point. Therefore i_a and i_c together with the NP voltage difference ΔV influence the switching states selection. All the possible switching states selections are listed in Table.3.4. The

undesired pattern 4 with more switching events happens when V1 and V5 are selected. Considering the switching states for the nearest three vectors, it can be determined that phase A switches between P and O while phase C switches between O and N. For the 3-level NPC converter, this means the reference voltage for phase A is in the positive half line cycle and the phase C reference voltage is in the negative half line cycle. In the meantime, the phase current for these two phases are in opposite polarity. This is to say the phase output voltage and phase

Table 3.4. Small vectors combination for hysteresis NP balance scheme

	$i_a>0,i_c>0$	$i_a<0,i_c<0$	$i_a>0,i_c<0$	$i_a<0,i_c>0$
$\Delta V>0$	V4(211) V2(110)	V5(221) V1(100)	V5(221) V4(211)	V2(110) V1(100)
$\Delta V<0$	V5(221) V1(100)	V4(211) V2(110)	V2(110) V1(100)	V5(221) V4(211)

current are not in phase with each other. With the above analysis, it is concluded that the undesired pattern 4 only happens under a non-unity power factor case. It can also be concluded that the pattern 4 happens when the nearest three vectors contain two small vectors. The simulation result reveals that the smaller the power factor is, the more frequently the pattern 4 case happens. When the power factor is 1, there is no pattern 4 in the whole line cycle. The whole space vector hexagon only contains desired pattern 1 with green color. In the space vector diagram in Fig.3.35, the star shaped area has possibility of having pattern 4 at non-unity power

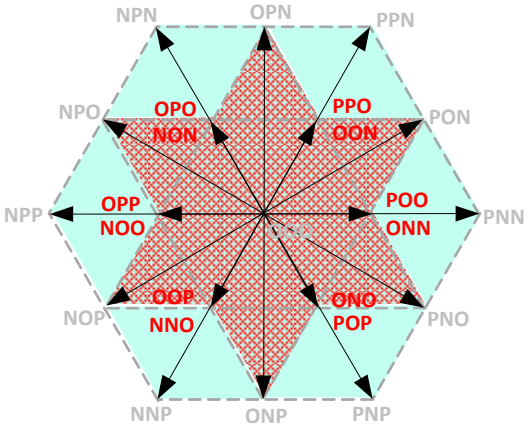
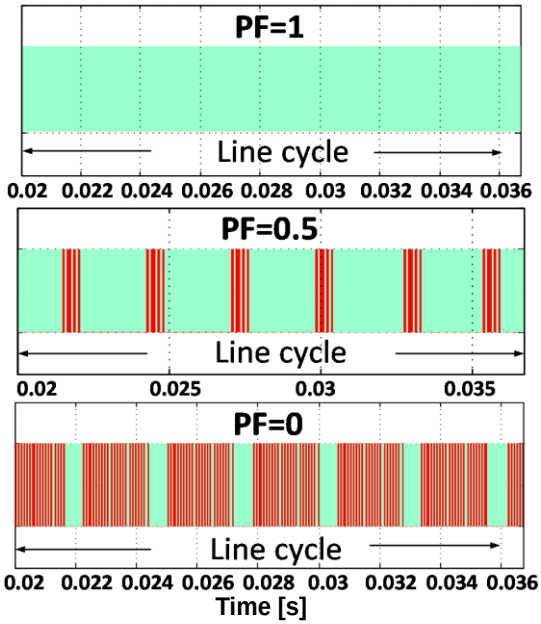
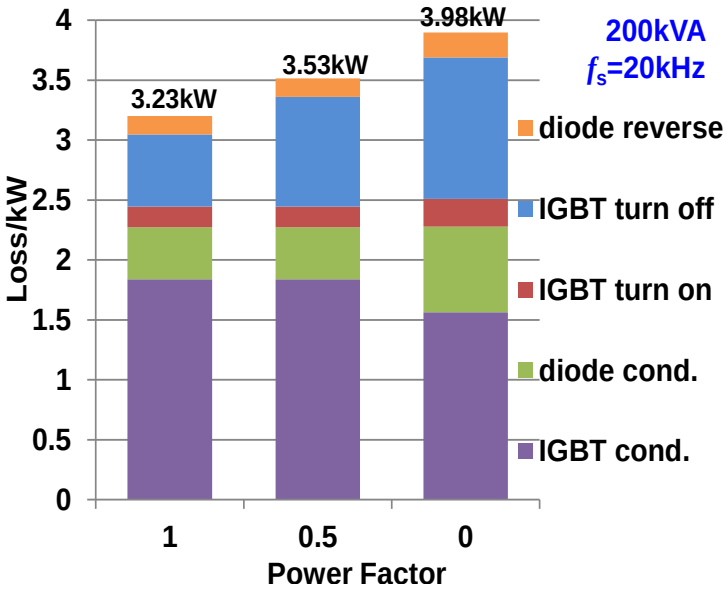


Fig. 3.35. Area division of space vector diagram for pattern 2 and pattern 4

factor case. The rest of the green areas are free for extra switching events. The figure also shows that the modulation index is irrelevant to the undesired case. The only influential factor is the power factor. Fig.3.36(a) shows the frequency of the undesired case happened in one line cycle under different power factors. The green area illustrates the switching cycles with only desired switching pattern 2 and the least switching events. The red area has the undesired pattern 4 with doubled switching events. The figure clearly shows that the lower the power factor is, the more frequently the undesired pattern 4 happens. To demonstrate the different loss generated by the undesired pattern 4 at different power factors, the total system loss is quantified over a line cycle as shown in Fig.3.36(b). It can be noticed that the lower the power factor is, the higher the switching loss will be. The quantitative analysis shows that at low power factor case, system loss is increased due to the undesired pattern 4 with extra switching events.



(a) Frequency for pattern 4 in a line cycle



(b) Total system loss with power factors

Fig. 3.36. Frequency and total system loss for undesired pattern 4 in one line cycle

3.4.2 Principle of the Proposed SVM for NP Balance and Loss Reduction

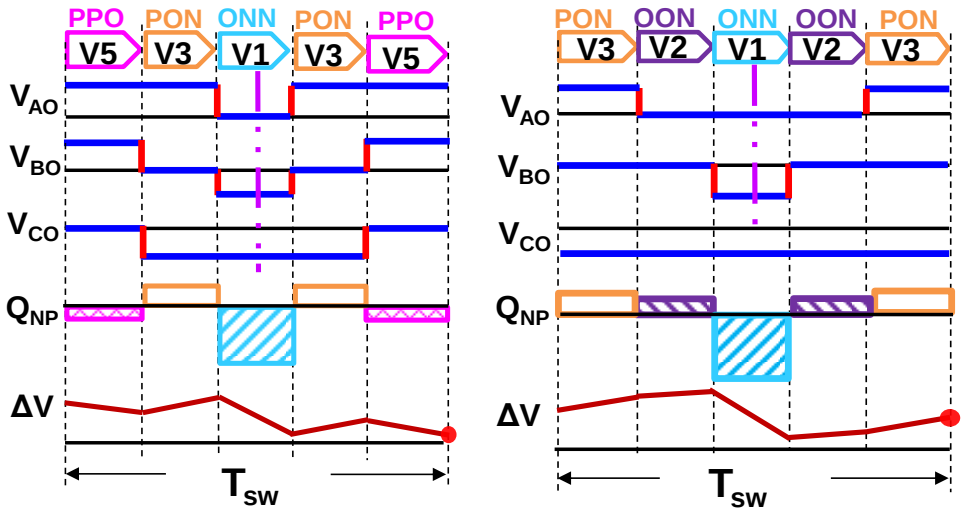
To avoid the undesired pattern 4, an improved SVM for NP balance and loss reduction is proposed to minimize the switching events in each switching cycle while maintaining the NP

voltage balance. This method is based on the hysteresis control for NP voltage balance. But it coordinately selects the switching states for the small vector so that the NP voltage can be balanced and the pulse sequence can be properly aligned. Compared with the hysteresis control which selects the switching state solely for NP voltage balance, the improved method can achieve multiple objectives simultaneously. The details of this method is then introduced.

For the star-shaped region in Fig.3.35, there is only one small vector and the consecutive vector number can always be guaranteed. The small vector selection only focuses on the NP balance. For the star shaped area, under the non-unity power factor case when the conventional hysteresis NP balance does not guarantee the consecutive vector number, one of the small vectors in the NTVs are selected for NP balance and the other one is selected for loss reduction. With the phase current and duty cycle information, the NP charge caused by the small vector V1 and V5 can be calculated as:

$$\begin{aligned} Q_{V5} &= i_c d(V_5) T_{sw} \\ Q_{V1} &= i_a d(V_1) T_{sw} \end{aligned} \tag{3-13}$$

The small vector with the larger NP charge is kept for NP balance and the other small vector is replaced by its counterpart in the small vector pair to ensure the consecutive vector number. Fig.3.37 gives an example for the conventional and proposed modulation in one switching cycle. For the conventional method in Fig.3.37(a), V1 and V5 are selected by the hysteresis control and V1 has larger NP charge than V5. As a result, the proposed method keeps V1 with larger influence on the NP balance and replace V5 by V2 for the pulse sequence alignment as in Fig.3.37(b). With the proposed method the vector number order is V3-V2-V1 instead of V5-V3-V1. By coordinately selecting the small vector, the consecutive vector number and the minimum switching events in one cycle can always be guaranteed. In principle, this method sacrifices a little NP voltage balancing result to gain loss reduction under a low power factor case.



(a) Conventional scheme 2 (b) Proposed method

Fig. 3.37. Switching cycle comparison for scheme 2 and proposed method

The NP balancing results for the SVM with hysteresis NP balance and the proposed SVM with NP balance and loss reduction are first compared. Fig.3.38 gives the NP voltage ripple comparison at different power factor cases. It show that the proposed balance scheme has the same NP voltage ripple at high power factor. The ripple for the proposed scheme is larger at very low PF than that of the hysteresis balance. Fig.3.39 shows the NP ripple comparison under all power factor and modulation index cases for the two balance scheme together with SPWM as benchmark. The proposed scheme has smaller ripple than SPWM and basically the same ripple as hysteresis control. The result shows the proposed method sacrifices very little NP voltage ripple to gain loss reduction.

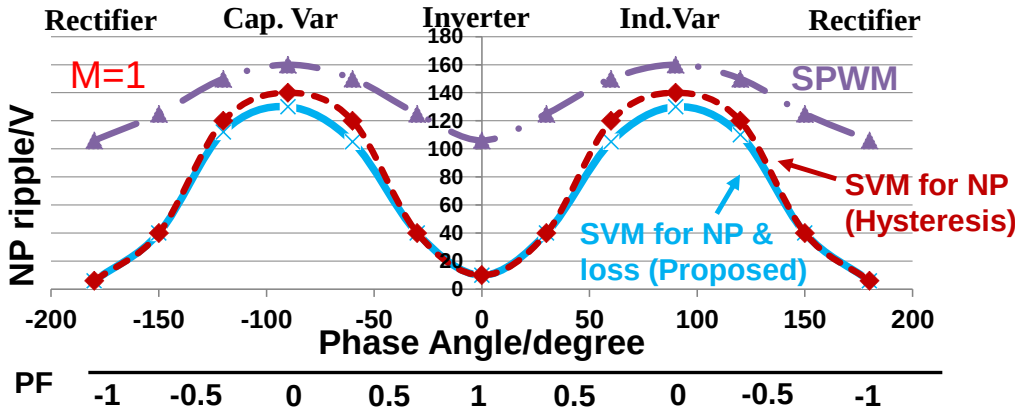


Fig. 3.38. NP voltage ripple comparison under different power factors

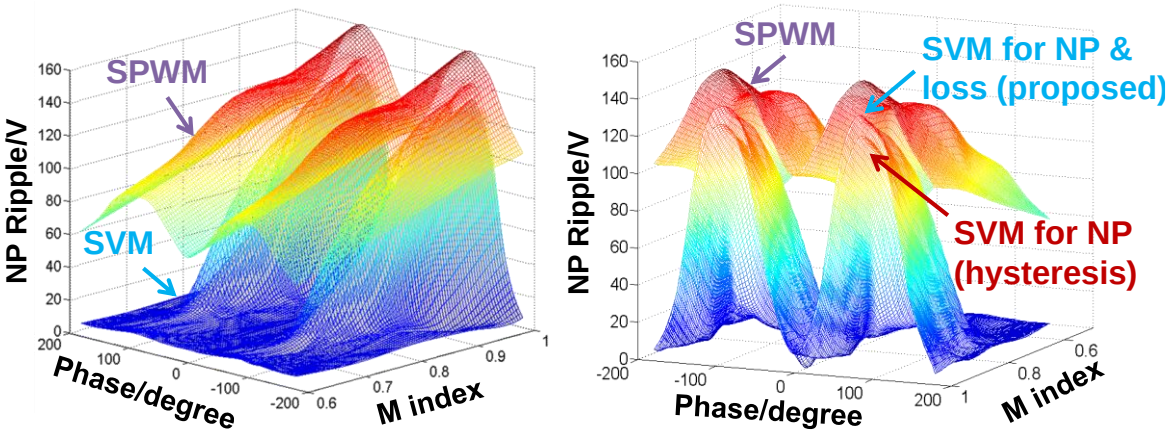


Fig. 3.39. NP voltage ripple comparison under different PF and M

The loss reduction result is also quantified by the loss model. Since the lower power factor causes more undesired pattern 4 in the line cycle, the total system loss breakdown is compared in Fig.3.40 for the two schemes under zero power factor. The conduction loss for the proposed method stays the same while the switching loss is largely reduced since the switching events in certain switching cycles are reduced from 8 to 4. For other power factors smaller than 1, the switching loss is also reduced by the proposed method. Fig.3.41 gives the system total loss comparison under different power factors to illustrate the loss reduction result. The SPWM is also shown in the figure as benchmark. The SPWM with 6 switching events per switching cycle has higher loss than both the two SVM methods at unity power factor with 4 switching events. But at zero power factor case, the conventional SVM with hysteresis NP balance has 8 switching events in each switching cycle and it generates even higher loss than SPWM. But the proposed SVM has the same pulse sequence pattern with 4 switching events regardless of the power factor. As a result, it has constant system loss and efficiency under all power factor cases. The quantitative analysis also reveals that the proposed SVM method sacrifices only 1.3% NP voltage ripple at zero power factor, but gains 14% loss reduction. At high power factor case, the ripple for the two SVM methods basically keeps the same. This feature is important for the high power high frequency PCS with bidirectional power flow.

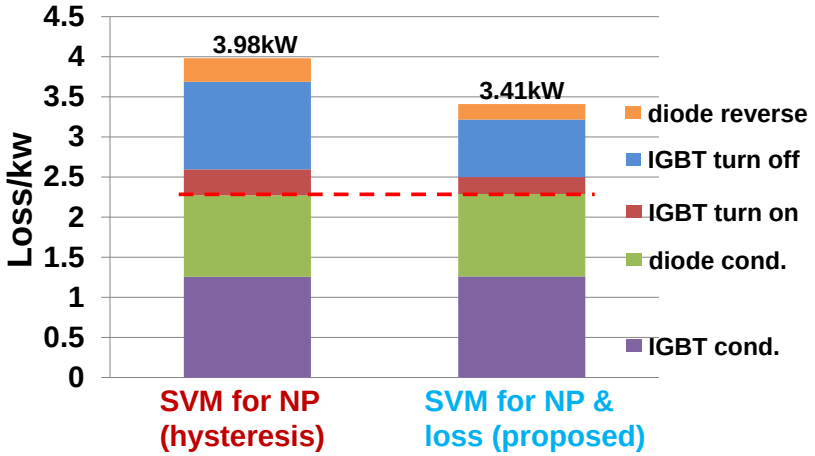


Fig. 3.40. System loss breakdown comparison at PF=0

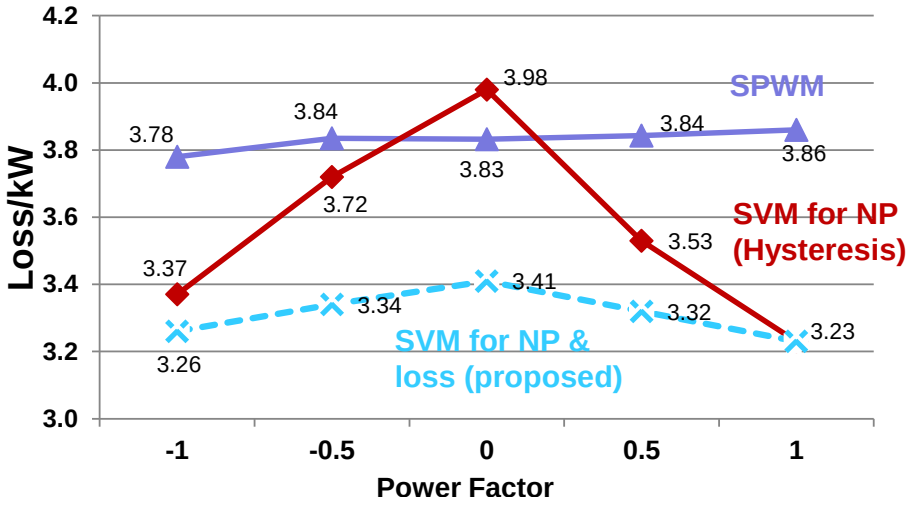
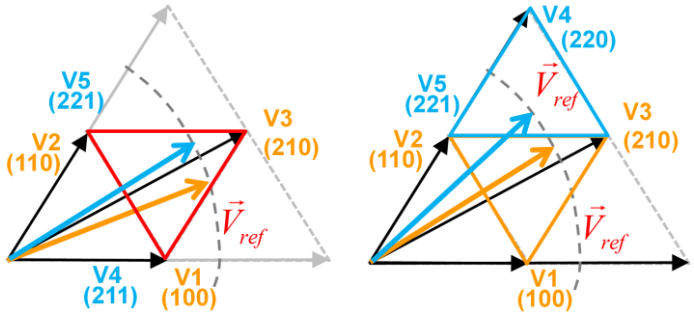


Fig. 3.41. System total loss comparison at all power factor cases

3.4.3 Switching Events Reduction between Switching Cycles

Besides minimizing the switching events in one switching cycle, the switching events between two switching cycles are also considered and eliminated for loss reduction. If the nearest three vectors for two switching cycles are the same, the pulse sequence starts and ends with the same vector and no switching event occurs between the two cycles. But the NTVs for two switching cycles are not always the same. There are two scenarios that cause different NTV in two cycles. One scenario, shown in Fig.3.42(a), happens when the switching states are changed by the SVM control like NP balance. Another scenario in Fig.3.42(b) happens when the voltage reference rotates from one triangle sector to another. The different NTVs may result in



(a) Switching status change (b) NTV sector change

Fig. 3.42. Two scenarios for NTV change

extra switching events if the last vector of one cycle is different from the first vector of the next cycle as shown in Fig.3.43. Although the switching events in these two cycles are minimized, there are extra switching events on each phase between the two cycles. Phase B even switched between P and N, which is not the nearest level and should be forbidden because of the possibility of phase leg shoot through. The aforementioned pulse sequence alignment rule only requests the consecutive vector number, it doesn't decide which vector starts first. If the pulse sequence ends and starts with the same vector within two cycles, the extra switching events between two cycles can be eliminated as shown in Fig.3.44. This pulse sequence can be achieved by coordinately considering the two sets of NTVs of the adjacent two switching cycles.

The loss reduction result by eliminating the extra switching events between two switching cycles is given in Fig.3.45. By eliminating the switching events between the two cycles, a 300W switching loss is reduced. Besides the loss reduction benefit, further investigation on the phase leg loss distribution also reveals that by eliminating the extra switching events between cycles, the loss distribution on the phase leg can be evenly distrusted on each device. For the NPC phase leg, the operation of the top cell and the bottom cell are symmetric in one line cycle. For SPWM modulation, the loss distribution pattern for the top cell devices is the same as the bottom cell devices. But for the SVM method, if extra switching events exists between two cycles, the loss distribution pattern is uneven for the two cells because the extra switching events are not

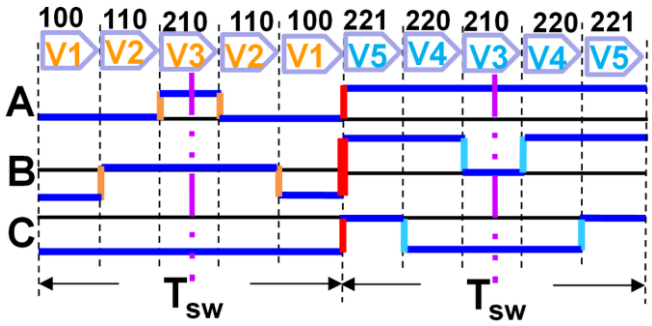


Fig. 3.43. Pulse sequence with extra switching events between cycles

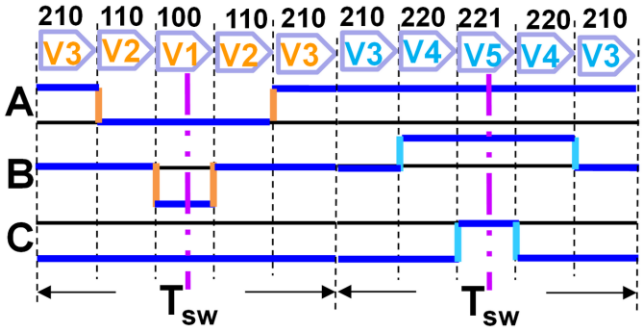


Fig. 3.44. Pulse sequence without extra switching events between cycles

symmetrically applied to the top and bottom cells. Fig.3.46 shows the phase leg loss distribution for a DNPC phase leg under different power factors case. With different PF, different devices undertake the extra switching loss. By eliminating the extra switching events between switching cycles, the phase leg loss distribution is symmetric for top and bottom cell devices as shown in Fig.3.47. The symmetric loss distribution patterns facilitate the thermal design and gives the devices even loss and thermal stress.

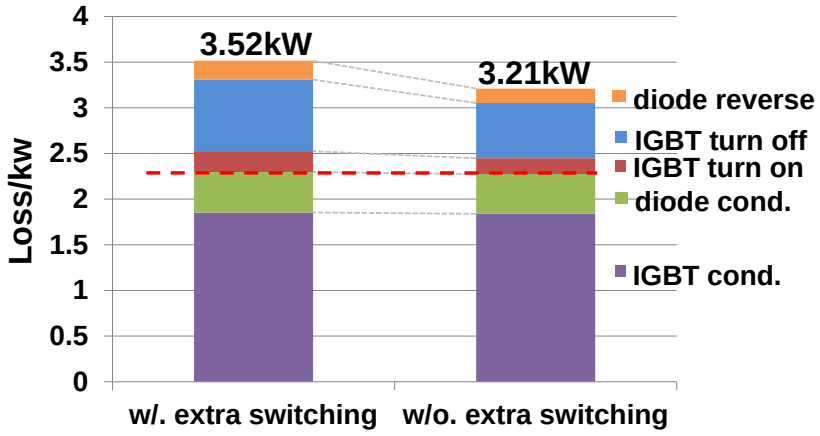


Fig. 3.45. Loss reduction result by eliminating switching between cycles

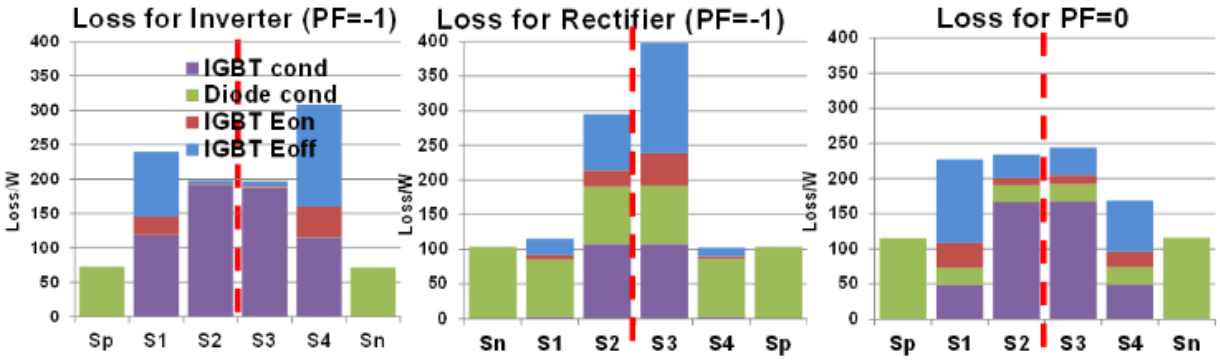


Fig. 3.46. Phase leg loss distribution with extra switching between cycles

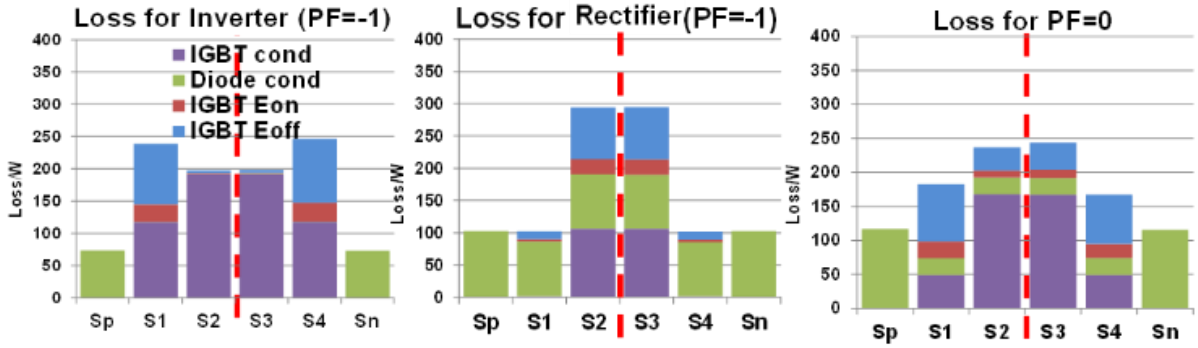


Fig. 3.47. Phase leg loss distribution without extra switching between cycles

3.4.4 Experiment Verification for the Proposed SVM

The proposed SVM method with NP balance and loss reduction is verified by both simulation model built in Matlab/Simulink and an experimental prototype of the 200kVA 3-level NPC power conversion system. The converter system contains several parts. The power stage is composed by the modularized 3-level NPC phase leg building block introduced in chapter 2. The grid interface part includes the contactor, fuses, LCL filter and a sensor board, which is also connected to the control board as feedback for the SVM control. The detail of the hardware will be introduced later in this dissertation. Here only shows the experimental result. The converter is connected to 480V AC grid via the LCL filter. With the given DC link voltage and the AC side voltage, the modulation index is around 0.8.

The NP balance result for the proposed SVM method is tested under unit power factor. Limited by the test environment, the whole system is run at 65 kW power. But the phase leg

building block is tested under full power. The loss model in simulation matches the experimental result well. Therefore, all the loss breakdown results are verified by experiment. For the NP balance result, the line to line output voltage and 3-phase grid current for the proposed SVM is shown in Fig.3.48. The voltage scale is 500V/div, the current scale is 50A/div and the time scale is 10ms/div in the figure. The NP balancing result for the proposed SVM is shown in Fig.3.49(a) with the voltage for top and bottom DC link capacitors displayed together with the output voltage and NP voltage ripple. Fig.3.49(b) shows the same result for the SPWM method. The experimental result shows that SPWM has a large NP voltage ripple. The proposed SVM method on the contrary has very little NP voltage variation, which verifies the NP balancing result.

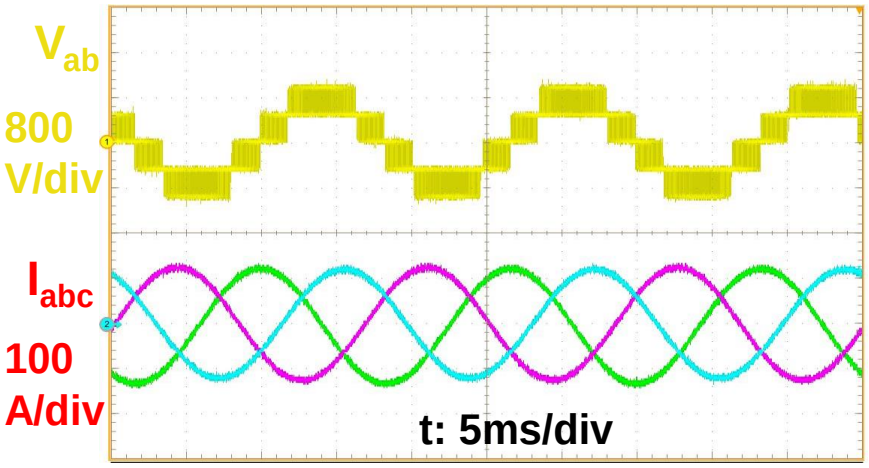
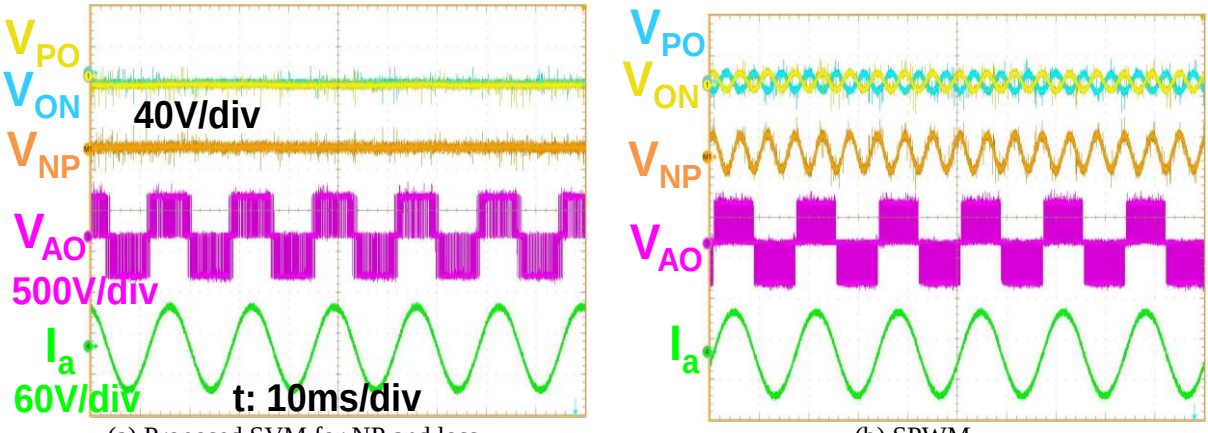


Fig. 3.48. Line-line voltage and 3-phase current for SVM



(a) Proposed SVM for NP and loss (b) SPWM

Fig. 3.49. NP voltage ripple and DC link voltage for two modulation methods

To verify the proposed pulse sequence alignment, the 3-phase output voltage is displayed in Fig.3.50. The phase to neutral voltage is then zoomed in to observe the switching states of the three phases within the time interval of several switching cycles as shown in Fig.3.51. The time

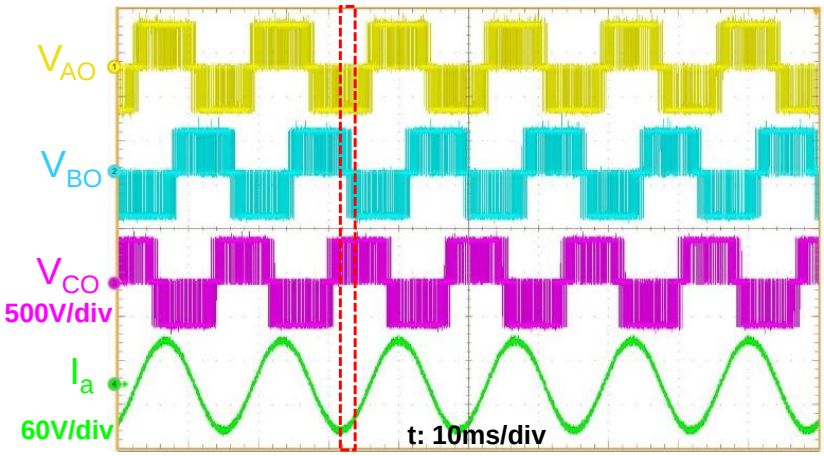


Fig. 3.50. Three-phase output voltage for the proposed SVM

scale shown in Fig.3.51 is 20μs/div. The result in the figure shows that the pulse sequence in each switching cycle only has four switching events. One phase stays constant in the cycle. Fig.3.51 also shows the scenario for vectors change. The two switching cycles have different NTVs. But with the proper sequence order, there are no extra switching events between the two cycles. The result verifies the proposed pulse sequence alignment for switching loss reduction.

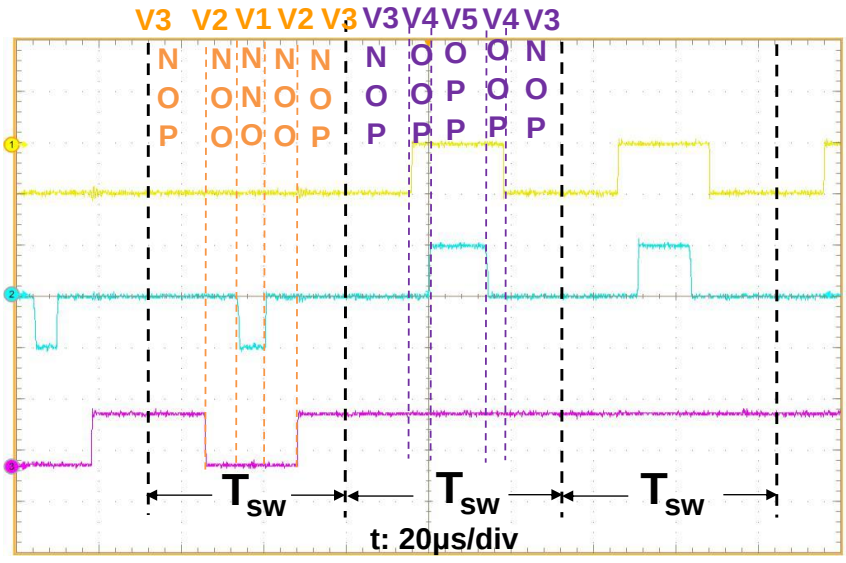


Fig. 3.51. Switching combinations within switching cycles

3.5 Dead-time Compensation for 3-level NPC Converter

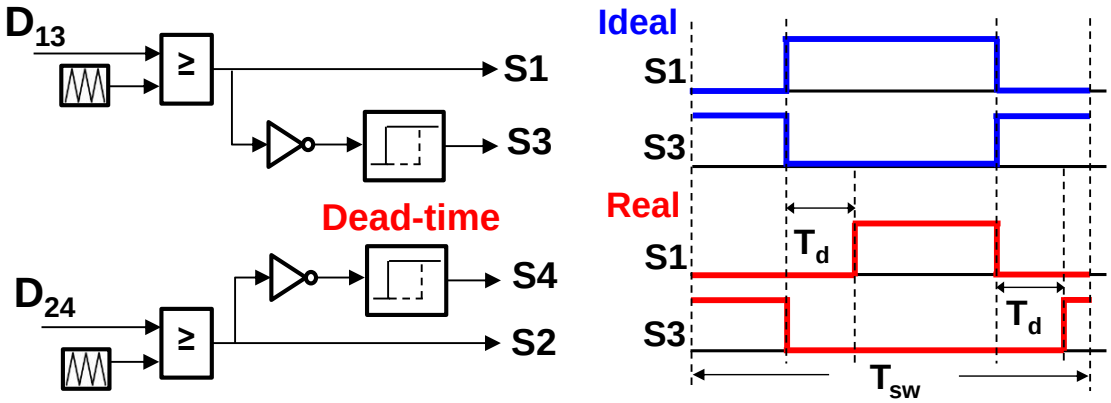
In the real implementation of the 3-level NPC converter hardware, the dead-time is essential to prevent the possible shoot through of the phase leg and provide safety operation margin. The dead-time is applied to every complementary switches in the commutation pole. The dead-time causes inevitable output current waveform distortion and increases THD. To avoid the side-effect from the dead-time, a dead-time compensation is necessary to be added into the modulation function into the converter. The dead-time compensation method for 3-level NPC converter with space vector modulation is discussed in this part.

For the 3-level NPC phase leg, there are several different modulation schemes introduced in Chapter2.2.1. The commutation pole for these methods contain different complementary switches. For the DNPC modulation, S1 and S3 are complementary while S2 and S4 are complementary. The dead-time is applied to the two complementary switches. For the other modulation schemes, the dead-time configuration is different. The phase leg gate signals implementation for DNPC phase leg is shown in Fig.3.52(a). The duty cycle reference for S1 and S3 is compared with the high frequency carrier and generates S1 gate signal. This gate signal is inverted and delayed with a dead-time to have the gate signal for S3. It is the same case for S2 and S4 gate signals. The ideal case gate signals without dead-time and the real gate signals with dead-time is shown in Fig.3.52(b). The rising edge for the two complementary gate signals are delayed with the dead-time to avoid shoot through. The dead-time T_d is typically determined by the turn off delay T_{off} and turn on delay T_{on} by the following expression.

$$T_d = 2(T_{off} - T_{on}) \tag{3-14}$$

Here the turn on and off delay is determined by the gate driver and also the switching device. The dead-time is designed to have enough safety margin. From the switching characteristics

evaluation in chapter 2, the on and off delay can be measured as T_{off}=764ns, T_{on}=330ns. By following equation 3-14, the dead-time for the 3-level NPC phase leg is set to 1μs.



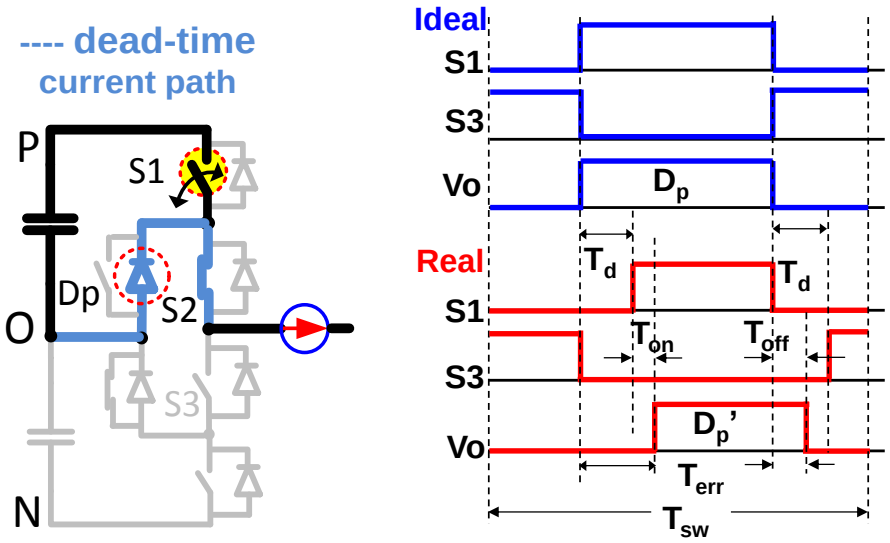
(a) Dead-time configuration (b) Gate signals with and without dead-time

Fig. 3.52. Dead-time configuration and gate signals for DNPC

3.5.1 Influence of Dead-time on Output Voltage and Current

The dead-time influences the duty cycle of the positive, negative and neutral switching states in each switching cycle and hence deteriorates the output waveform. In real implementation, there is a turn on and turn off time for the device to reach steady state. This time also influences the output voltage duty cycle. For the 3-level converter, phase leg current direction determines how the switching states are influence by the dead-time. The switching transient for the top cell between P and O for DNPC phase leg is taken as an example. The circuit diagram and gate signals with and without dead-time for the positive phase leg current is shown in Fig.3.53. Assuming the switching cycle begins with neutral state where S2 and S3 is on and neutral current flows through Dp and S2. For ideal case without dead-time, the switch S3 is turned off and S1 is turned on simultaneously, so that the output voltage switches from neural to positive at the same time. This is shown with the blue line in Fig.3.53(b). If dead-time and turn on delay is considered, the real gate signals and output voltage is shown with the red line in Fig.3.53(b). After S3 is turned off without delay, S1 is not turned on until the dead-time T_d. During this time,

since the output current is positive, it still flows through the freewheeling path of Dp and S2 as shown in



(a) Circuit diagram for freewheeling path (b) Gate signals with and without dead-time

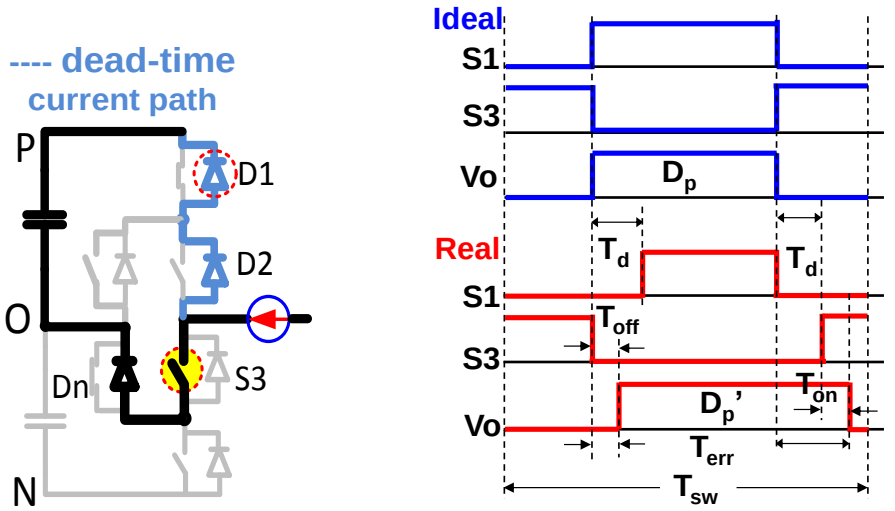
Fig. 3.53. Dead-time for P and O switching with positive phase current

Fig.3.53(a). The commutation between S1 and diode Dp happens after the dead-time when S1 is turned on. After S1 is on, there is a turn on time T_{on} for the device to be fully turned on and conduct current. So the real output voltage switches to positive after the dead-time T_d and the turn on time T_{on}. For the switching transition from O to P with positive phase current, the neutral state O is extended by T_d+T_{on} as shown in the figure. For the switching transition from P to O in the same switching cycle, S1 is turned off without delay and S3 is turned on after the dead-time. The commutation happens after S1 is turned off and the phase current freewheels through the neutral path during the dead-time. Considering the turn off time, the output switches from P to O after T_{off}. For P to O transient, the positive state is just extended by T_{off}. So the duty cycle for the positive state D_p is influenced by an error time T_{err}, which is determined by the dead-time, turn on time and turn off time. So the real duty cycle for positive state D_p' with the consideration of dead-time is given in 3-15. Here D_P is the original duty cycle without dead-time and T_{err} is the error time for dead-time and turn on/off time. For the transient between P and O with positive

phase current, the duty cycle for positive state is diminished by T_{err} and the duty cycle for neutral state is extended by T_{err}.

$$D_P' = D_P - \frac{T_{err}}{T_{sw}} = D_P - \frac{T_d + T_{on} - T_{off}}{T_{sw}} \tag{3-15}$$

For the same transient between P and O with negative phase current, the same analysis can be carried out. The circuit diagram and gate signals are shown in Fig.3.54. With the negative current, similar analysis also applies, but the freewheeling path during the dead-time is changed from neutral current path to positive current path as shown in Fig.3.54(a). So during the transient from O to P, commutation happens at S3 turn off and output is connected to P after the turn off time. For the transient from P to O, commutation happens at S3 turn on after the dead-time. The



(a) Circuit diagram for freewheeling path (b) Gate signals with and without dead-time

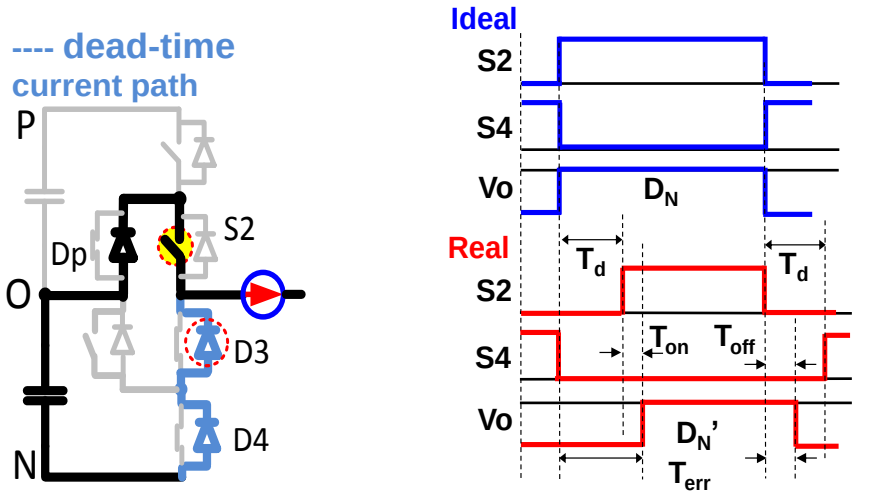
Fig. 3.54. Dead-time for P and O switching with negative phase current

output is connected to P after the dead-time and the turn on time. As a conclusion, for negative phase current, the duty cycle for positive state is extended by T_{err}.

$$D_P' = D_P + \frac{T_{err}}{T_{sw}} = D_P + \frac{T_d + T_{on} - T_{off}}{T_{sw}} \tag{3-15}$$

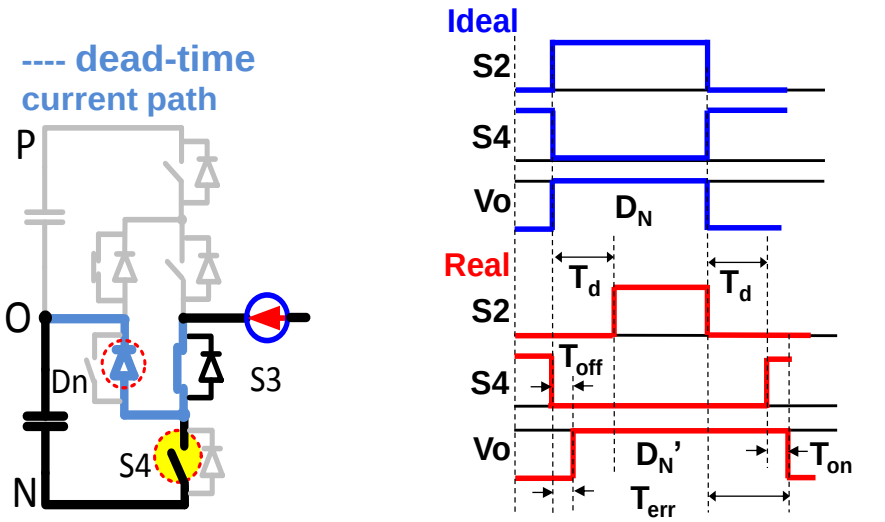
For the transient between neutral and negative state, the conclusion can be drawn by the similar analysis. The circuit diagram and gate signals for the transient between N and O with

positive phase current is shown in Fig.3.55. The same circuit diagram and waveform for the N and O transient with negative phase current is shown in Fig.3.56. For the N and O transient with positive current, the freewheeling path during the dead-time is connected to the negative state. Consequently the duty cycle for negative state D_N is extended by T_{err} and duty cycle for neutral state is diminished by T_{err}. For the same transient with negative phase current, the freewheeling path at dead-time is connected to the neutral state. So the duty cycle for neutral state is extended and the duty cycle for negative state D_N is reduced by T_{err}. The above analysis for the dead-time provides the basis for dead-time compensation. For the real 3-level NPC phase leg, the error time brings by the dead-time and on/off time is around 566ns.



(a) Circuit diagram for freewheeling path (b) Gate signals with and without dead-time

Fig. 3.55. N and O transient with positive current



(a) Circuit diagram for freewheeling path (b) Gate signals with and without dead-time

Fig. 3.56. N and O transient with negative current

Then the impact of dead-time on the SVM modulation is considered. The 3-phase output voltage waveform in a switching cycle with certain phase current direction is given in Fig.3.57.

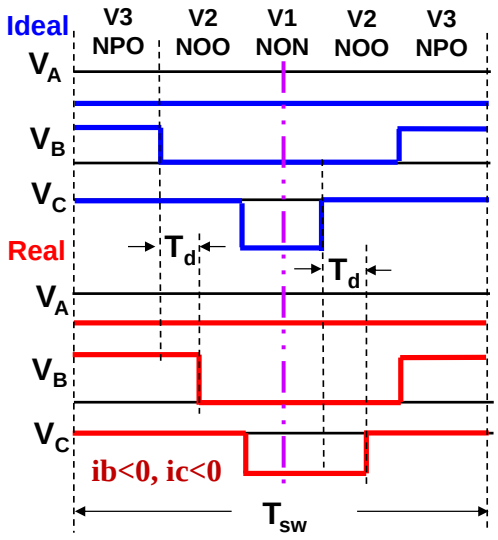
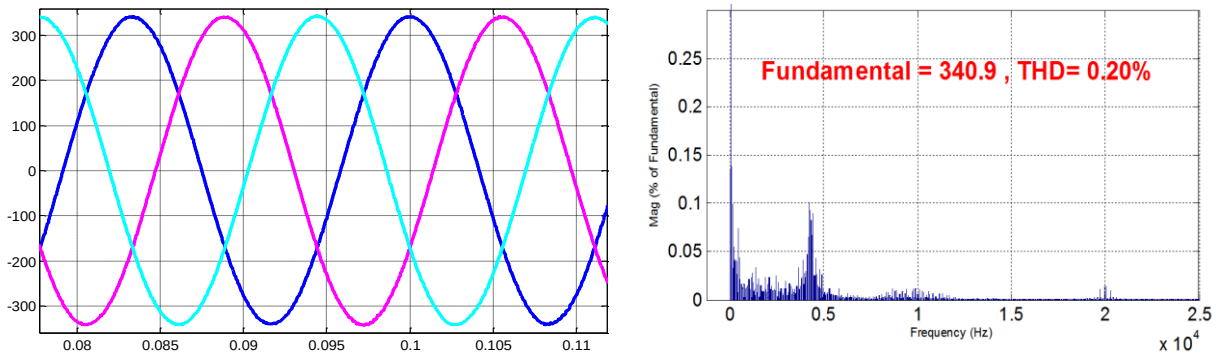


Fig. 3.57. Impact of dead-time on 3-phase output voltage with SVM

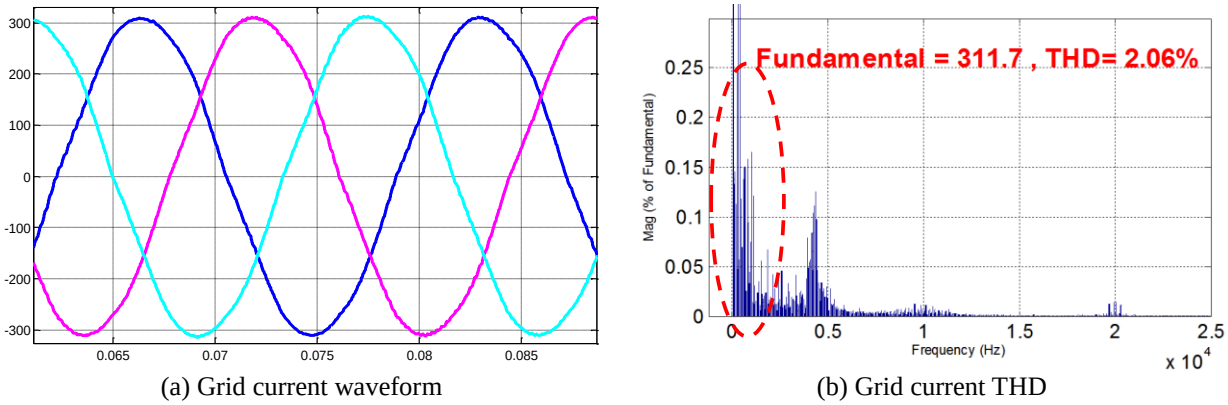
For the ideal case with the blue curve, the pulse sequence alignment is center aligned and symmetrical. But for the real case with dead-time in the red curve, the pulse sequence is not center-aligned and it is asymmetrical. The duty cycle for each vector is also distorted. For this reason, the grid current waveform is deteriorated and the THD will be increased. The grid

current waveform and current THD is simulated for the 3-phase converter at rated power. Fig.3.58 gives the grid current waveform and current spectrum at ideal case. Fig.3.59 on the other hand gives the same waveform at real case. The current waveform at the ideal case is pure



(a) Grid current waveform (b) Grid current THD

Fig. 3.58. Grid current waveform and THD without dead-time



(a) Grid current waveform (b) Grid current THD

Fig. 3.59. Grid current waveform and THD with dead-time

sinusoidal and the THD is only 0.2%. However, for the real case with dead-time, an obvious distortion can be observed in the grid current waveform and there are large low order harmonic component in the current spectrum. The grid current THD also rises up to 2.06%.

3.5.2 Dead-time Compensation Method and Result

The dead-time compensation method for 3-level NPC converter is introduced in this part. With the influence of the dead-time on the duty cycle for each switching state analyzed in detail, the principle to compensate the duty cycle is clear. For each phase leg, the original duty cycle is

modified to compensate the influence of dead-time according to the phase leg current. This compensation method is based on the phase leg. But the SVM modulation is based on the vector, which is the switching states for all the 3 phases. So the compensation method should be adjusted to fit the vector based modulation. Taking the pulse sequence in Fig.3.57 for instance, during each vector transition, there is only one switched phase leg. Therefore, the vector based modulation can be transformed into the phase leg based modulation. For the transition from V3 to V2 in that figure, phase B is switched from P to O. Since phase B has negative current in this switching cycle, the duty cycle for P state is extended. In other word, the duty cycle for V3 is extended and the duty cycle for V2 is reduced. Likewise, the transition between V2 and V1 switches phase C from O to N. With negative phase current, this transition extends the neutral state and also the duty cycle for V2. To compensate the influence of dead-time, the duty cycle for each phase should be increased or decreased according to the phase current. Taking phase B in Fig.3.57 as example, the gate signal waveform for S1 and S3 in this phase at ideal case, real case and compensated case are shown in Fig.3.60. Since the positive state is extended by T_{err} with dead-time, the compensation method deducts T_{err}/T_{sw} from the duty cycle of P state as the magenta colored curve shows. With the compensated gate signal, the phase output voltage returns to the original case and the output voltage is symmetrical in a switching cycle. For the other phases, the same principle can be applied with the sensed current direction information. This compensation method is first implemented in the simulation model. The grid current waveform has less distortion and the current THD reduced to 0.78% from 2.06%.

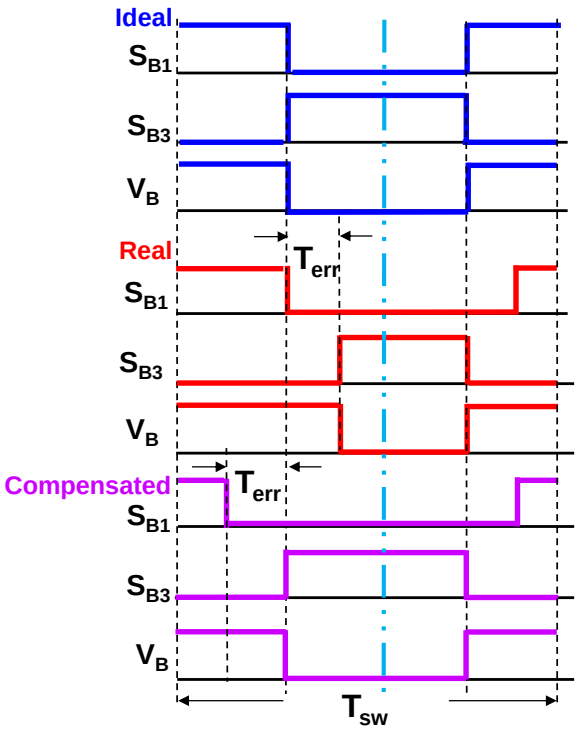
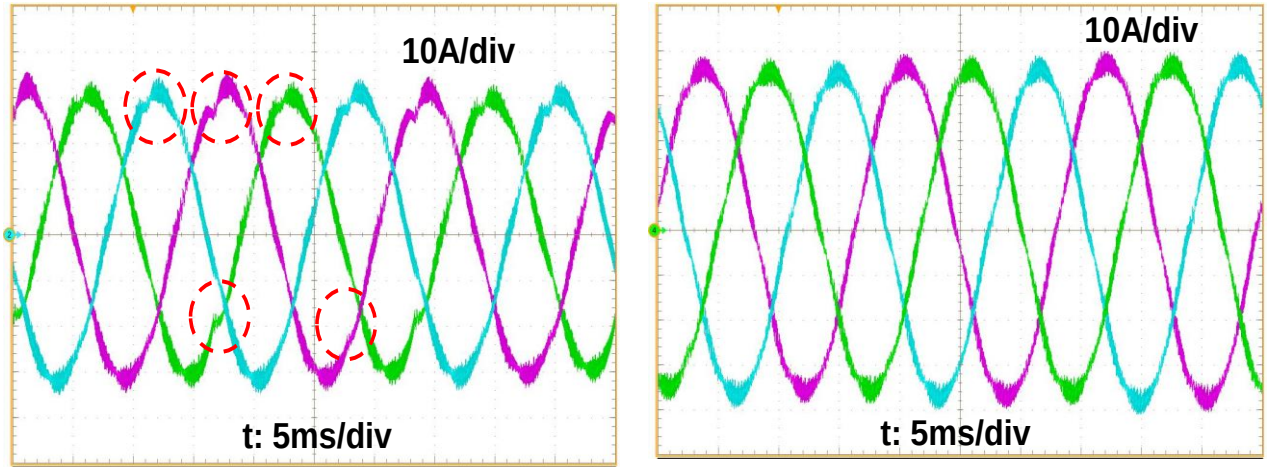


Fig. 3.60. Gate signals for one phase with dead-time compensation

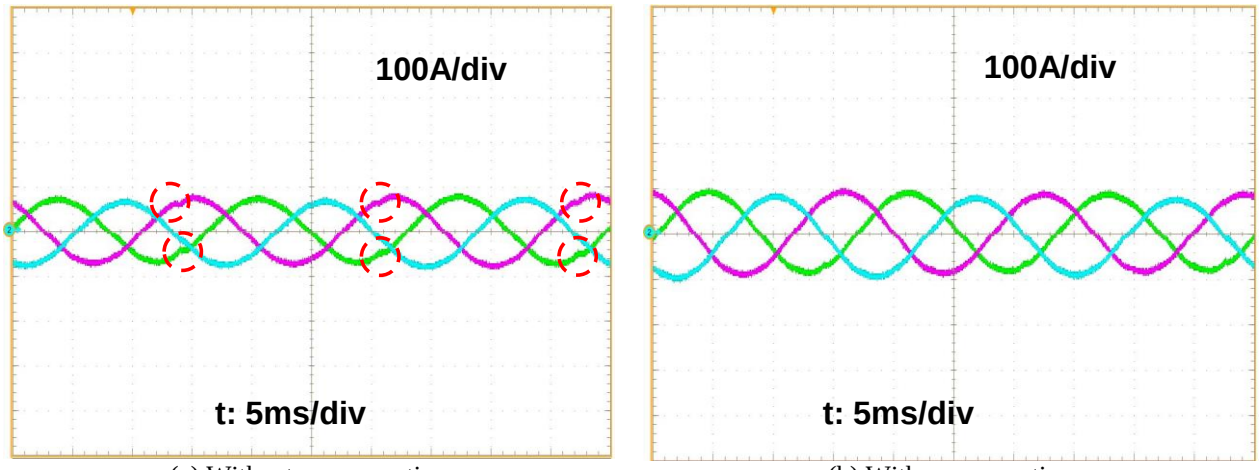
The dead-time compensation method is also implemented in the 3-level NPC converter for verification. The inverter output current and grid current waveform with and without compensation is compared side by side. The 3-phase current without compensation in Fig.3.61(a) has an obvious glitch near its peak, where is the zero-crossing for another phase. The current glitch caused by the dead-time generates distortion and also increases the THD. The compensated current in Fig.3.61(b) is free of the current glitch and the waveform is sinusoidal. The grid current waveform is also compared in Fig.3.62. The current glitch is also reflected in the grid current. The dead-time compensation reduces the glitch and distortion in the grid current as well. The spectrum of the grid current is analyzed and compared for the compensated and uncompensated case in Fig.3.63. For the uncompensated case in Fig.3.63(a), the spectrum contains some low order harmonics. The amplitude of the 5^{th} and 7^{th} order harmonic is especially prominent, which is caused by the dead-time effect. The THD for the uncompensated grid current is around 3.05%. But for the compensated current in Fig.3.63(b), the low order harmonic

components have been largely reduced. The odd order harmonic like 5^{th} and 7^{th} order harmonic is basically eliminated by the dead-time compensation. Also the THD for the grid current is reduced from 3.05% to 1.32%. In reality, the dead-time and on/off time is influenced by various factors like propagation delay or device non-linearity. So the compensation can not totally eliminate the dead-time effect. However, it can largely reduce the THD and compensate the current distortion. The experiment provides solid support to this statement.



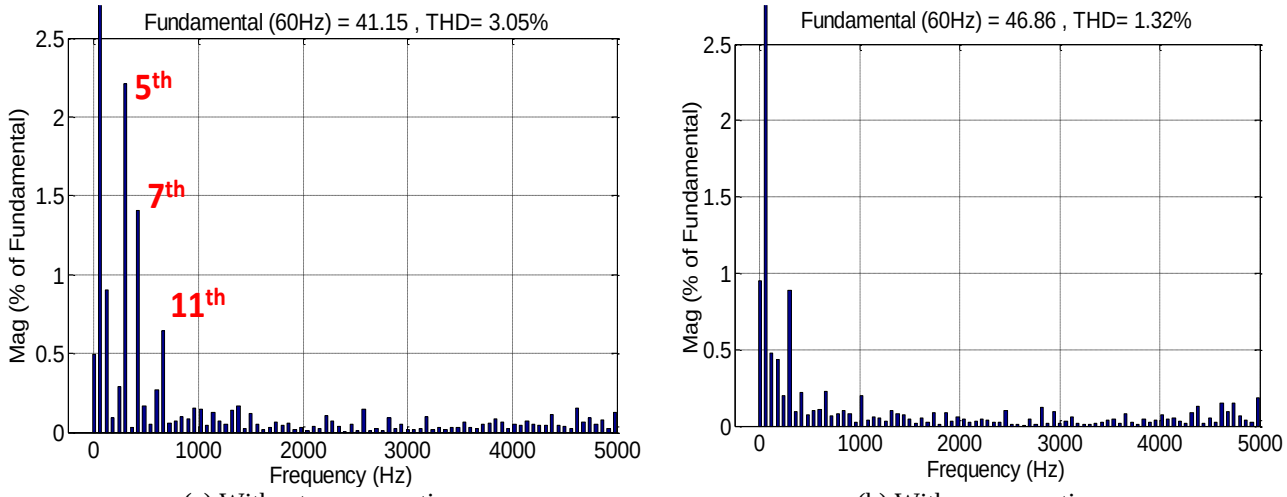
(a) Without compensation (b) With compensation

Fig. 3.61. Inverter output current waveform with and without compensation



(a) Without compensation (b) With compensation

Fig. 3.62. Grid current waveform with and without compensation



(a) Without compensation (b) With compensation

Fig. 3.63. Grid current spectrum with and without compensation

3.6 Summary and Conclusion

This chapter discuss the modulation scheme for 3-level NPC converter with bidirectional power flow and high switching frequency. Different control objectives with SVM is evaluated and a new SVM scheme for NP balance and loss reduction is proposed. The different calculation methods for the duty cycle and vector location are first introduced and compared. A simplified calculation method is adopted to save the computation cost for the control scheme. Different control objectives using the redundant switching states for small vectors are discussed. The principles for the neutral point voltage balance, switching loss reduction and common mode noise reduction by SVM are introduced in detail. Different control schemes are compared by simulation result and loss model. The NP voltage ripple, total system loss and CM noise spectrum are compared for all the SVM strategies. Based on the conventional SVM for NP balance, an improved SVM method is proposed. This method balances the NP voltage while maintains the minimum switching events in every switching cycle. The multiple control objectives are achieved simultaneously by properly selecting the switching states for small vectors that considers both the NP charge and pulse sequence. Also the pulse sequence order is

carefully treated so that the extra switching events between two switching cycles are eliminated. By doing so, the switching loss is further reduced and the phase leg loss is distributed more evenly on each device. With this modulation method, the NP voltage can be perfectly balanced and the switching loss is largely reduced. The system efficiency stays the same under all power factor cases. The control result is verified by both simulation model and experimental prototype on a 200 kVA, 20kHz 3-level NPC converter. The impact of the dead-time on the 3-level NPC converter is considered and analyzed at the end of this chapter. The dead-time compensation method is also introduced. It is implemented in the hardware and the experiment waveform verifies the compensation result.

The research contributions in this chapter is concluded in the following:

1. Detailed survey and comparison of different calculation methods for duty cycle for SVM
2. In-depth investigation and analysis of the switching states selection criteria for neutral point balance, loss reduction and common mode noise reduction
3. Quantitative analysis and trade-off between the NP voltage ripple and total loss for different modulation strategies considering different operating conditions
4. Proposed a new modulation strategy to balance the neutral point voltage and reduce the switching loss simultaneously.
5. Explored and implemented the dead-time compensation for 3-level NPC converter with SVM modulation strategy.

CHAPTER.4 FURTHER IMPROVEMENT OF 3-LEVEL ANPC FOR LOSS/STRESS REDUCTION

As mentioned in chapter 2, the DNPC phase leg has unevenly distributed loss and switching stress for each devices. The loss and stress distribution pattern varies with the converter operating condition since the neutral current path is passively determined by the load current direction [1], [2]. The ANPC topology on the other hand can actively choose the neutral current path therefore provides possible solution for the unbalanced loss issue. There are several modulation schemes for 3-level ANPC phase leg [3]-[5], with different phase leg loss distribution patterns. But these methods still have unbalanced device loss and stress. Then a modulation strategy is proposed [6] to balance the phase leg loss by actively using different modulation schemes. This method generates the gate signals according to device temperature feedback and also online temperature calculation by thermal model. This process is really complicated with high computation cost. In addition, this method is a mixture of different modulation schemes, so the gate signals don't have a fixed complementary manner as the conventional modulation schemes do. There is no unified dead-time configuration for the complementary switches since the commutation pole for this modulation scheme is uncertain. The aforementioned issues make this method very hard for real implementation.

In this chapter, a new modulation scheme is proposed for the 3-level ANPC phase leg. This method takes the advantage of the flexibly configured neutral current path. Both two neutral paths are used to conduct the neutral current and therefore largely reduce the conduction loss. Also this method results in new type of commutation loops for 3-level NPC phase leg, which helps the balance of phase leg loss distribution and most importantly, reduces the switching stress during commutation. Besides the loss/stress reduction and balance, this method also

features on its simplified implementation. Compared with the conventional modulation for 3-level ANPC phase leg, which requires 3 pairs of comparators for 6 PWM channels, the proposed method only needs 2 pairs of comparators. For a 3-phase system, it can save 6 PWM channels in total. Double pulse tests on the new switching loop are conducted for the 3-level ANPC phase leg hardware at different load current cases to investigate the switching characteristics. Detailed loss and stress analysis is also given. The proposed method is finally verified on the 3-level ANPC power conversion system.

4.1 Proposed Modulation Scheme for 3-level ANPC Phase Leg

There are three different modulation schemes for the 3-level NPC phase leg, one for DNPC and another two for ANPC [7]-[9]. They are introduced in detail in chapter 2.2.1. The switching states and gate signals for these methods are given. With the double pulse tests and the detailed loss model, the phase leg loss and stress distribution for different methods are also analyzed in Chapter 2.4. In addition, the total system loss and efficiency with the three modulation schemes are also quantified in the same part. Since the ANPC phase leg has configurable neutral current path, the aforementioned two modulation schemes for ANPC have two neutral states O+ and O- as shown in Table.2.3 and 2.4. If the conventional SPWM or SVM modulation strategy is applied to the converter, the phase to neutral voltage for one phase leg switches between P and O for the positive half line cycle. In the negative half line cycle, the phase leg output switches between N and O as in Fig.4.1. With the ANPC outer switch mode introduced in Table.2.3, the neutral state O+ is used in positive half cycle for top cell switching and O- is used in the negative half cycle for bottom cell switching. By doing so, only short switching loop is involved. Similarly, if O- is used for positive half cycle and O+ is used for negative half cycle, then only long loop is used. But for the SVM modulation strategy with the neutral point voltage balanced

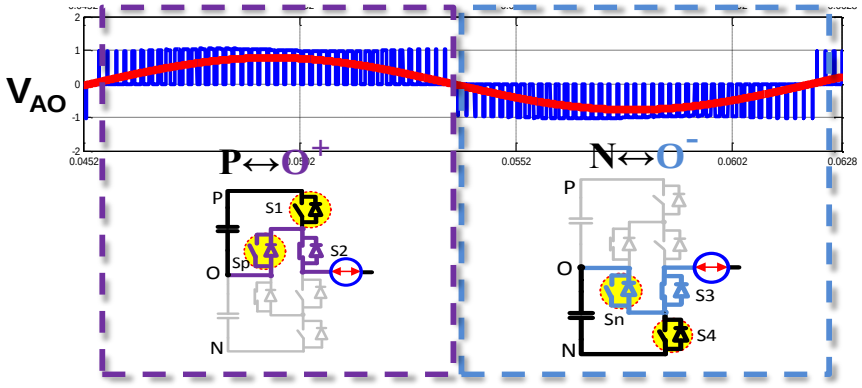


Fig. 4.1. 3-level NPC phase to neutral voltage with SPWM or conventional SVM

in each switching cycle as introduced in chapter 3 and other literatures [10]-[12], the phase leg output voltage looks like the one shown in Fig.4.2. In each line cycle, there exists a period when the output voltage alternatively switches between all the 3 states in consecutive switching cycles, like the bottom part of Fig.4.2. Under this circumstances, neither of the two neutral states is suitable in the period with mixed 3-level output. If the O+ is used for P-O switching with short loop, then in the next cycle, the switching between N and O have to use the long loop since the neutral state stays at O+ as shown in the left bottom part of Fig.4.2. It is the same case if O- is

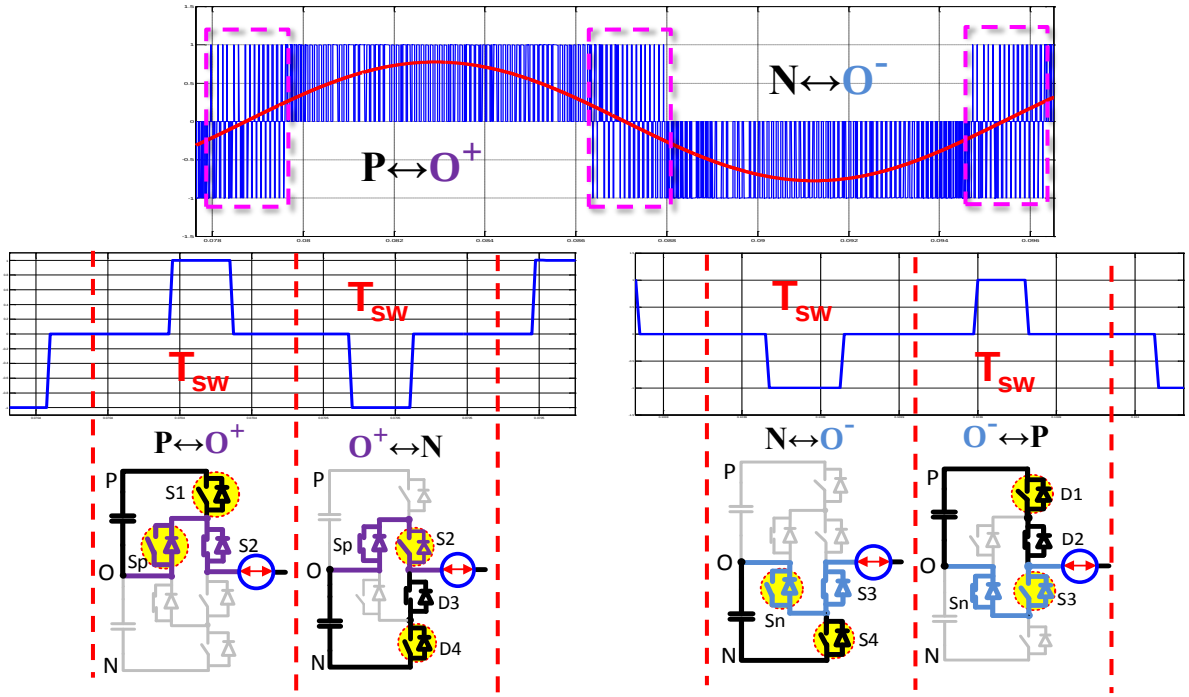


Fig. 4.2. 3-level NPC phase to neutral voltage with SVM for NP balance

used for N-O switching with short loop. The neutral state is uncertain and the long loop with larger stress and loss is inevitable for a large portion in line cycle. Although the modulation can be modified by adding an intermediate step to transfer the neutral states from O+ to O-, the modification increases the complexity of the scheme and also causes extra switching events and related loss. Also the dead-time configuration for the complementary switches is changed.

To solve this problem and also to further reduce the system loss and stress, a new modulation scheme for 3-level ANPC phase leg is proposed. The gate signal sequence is shown in Table.4.1. For positive state, switch S1 and S2 are turned on to connect the output to positive rail. Switch Sn is also on so that the switches S3 and S4 in off state can equally share the DC link voltage. The negative state follows the similar rule. But for the neutral state, both the upper path and lower path for the neutral current are used simultaneously. So there is only 1 neutral state for the proposed method instead of 2 for the conventional ANPC modulation. As a result, no matter the output voltage is switching between P and O or N and O, the only neutral state is used. More importantly, by using both two neutral current paths to conduct current, the conduction loss can be significantly reduced. A quantitative analysis for the loss reduction is given later. The circuit diagrams for the three switching states together with the phase leg output voltage waveform are given in Fig.4.3. The positive and negative states are the same for the conventional modulation for 3-level NPC. But the clamping device Sn is on for positive state and Sp is on for negative state. For positive state, switch Sn connects the neutral point to the emitter of S3, so that the top DC link voltage is blocked by S3 and bottom DC link voltage is blocked by S4. It is the similar

Table 4.1. Gate sequence for the proposed modulation scheme

	Sp	S1	S2	S3	S4	Sn
P	off	on	on	off	off	on
O	on	off	on	on	off	on
N	on	off	off	on	on	off

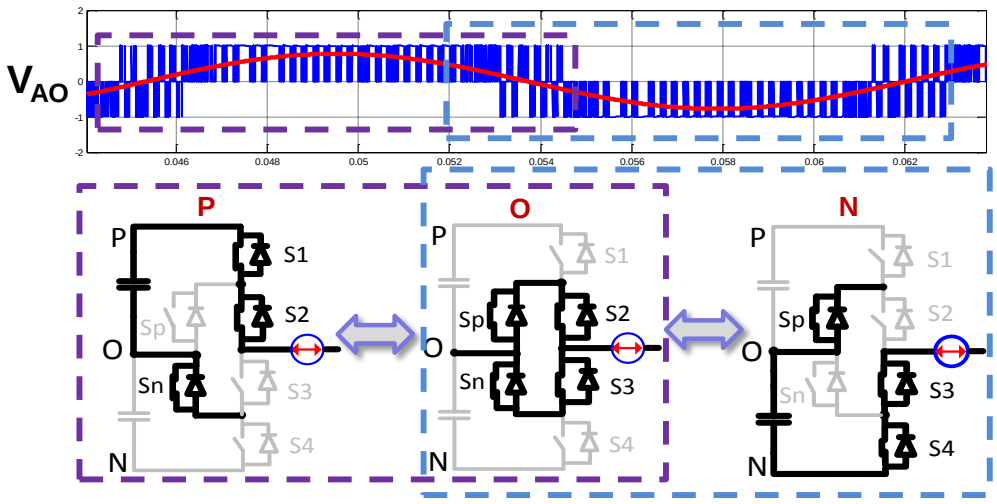
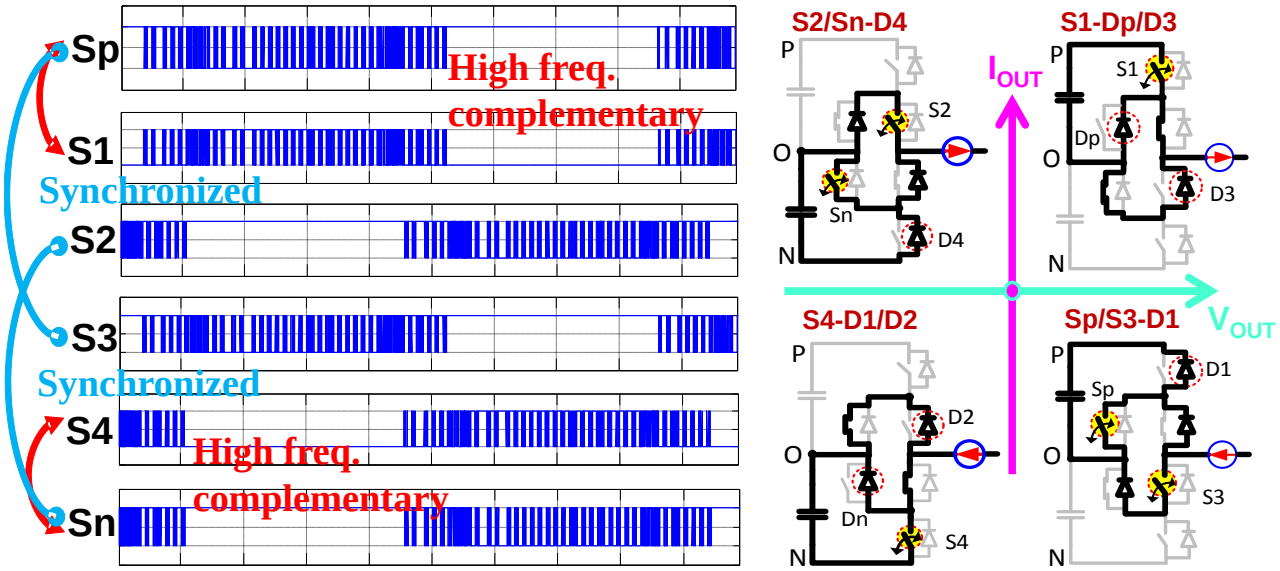


Fig. 4.3. Circuit diagram for three switching states

case for the negative state. This measure ensures an evenly split DC link voltage on the two switches in off state. Typical solution for this problem puts resistors in parallel with all the switches to ensure they block the same voltage. Obviously that measure causes extra loss. For the neutral state, the two paralleled neutral current path can be observed. This is the key to reduce the conduction loss for neutral state. Fig.4.3 also shows that over the line cycle, there is only one neutral state that commutates with both the positive and negative states. This neutral state works with the P and O in consecutive switching cycles in the area where the output voltage switches between all the three levels.

The line cycle gate signals for the proposed modulation is shown in Fig.4.4(a). The outer and clamping switches for top and bottom cells are still in a complementary manner with high switching frequency. The inner switch S2 is switched synchronously with its diagonal clamping switch Sn. So does the other inner switch S3. As a result, all the 6 switches have high switching frequency for half a line cycle. With this modulation scheme, the commutation loops in the 4-quadrant are derived in Fig.4.4(b). In the 1st and 3rd quadrant for inverter mode, the outer switch commutates with two synchronized inner and clamping diodes. In the 2nd and 4th quadrant for rectifier mode, the outer diode commutates with two synchronized inner and clamping switches.



(a) Gate Signals in line cycle (b) Four quadrants switching loops

Fig. 4.4. Gate signals and switching loops for proposed modulation scheme

Compared with the conventional commutation loop that contains single switch and diode, the proposed modulation scheme generates new switching loops that contain 1 switch (diode) and 2 paralleled diodes (switches). Although the new switching loops seem to be complex, it can be simplified. The switching loop in 2nd quadrant (S2/Sn-D4) equals to the combination of a short switching loop (Sn-D4) plus a long switching loop (S2-D4) as shown in Fig.4.5. Both of these two loops just switch at half load current. The switching loop in 3rd quadrant (S4/Dn-D2) also equals to the combination of a short loop (S4-Dn) plus a long loop (S4-D2) as in Fig.4.6. The two loops also switch at half load current. The new switching loops in other quadrants can be simplified as combination of a short loop and a long loop in the same manner. As a conclusion,

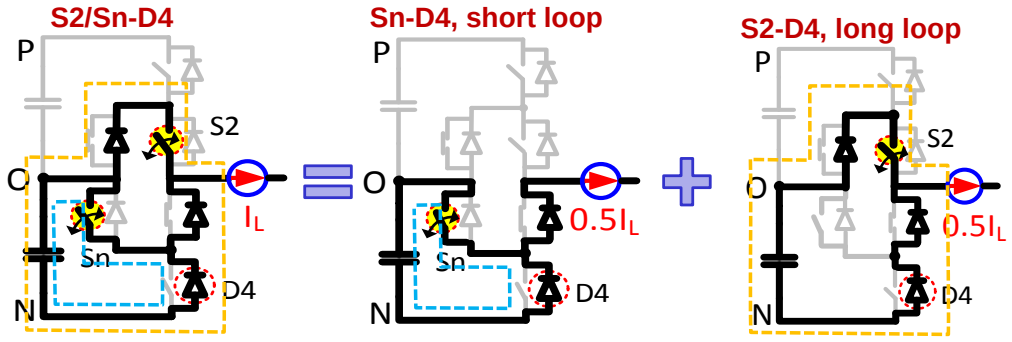


Fig. 4.5. Equivalent switching loops of the new switching loop in 2nd quadrant

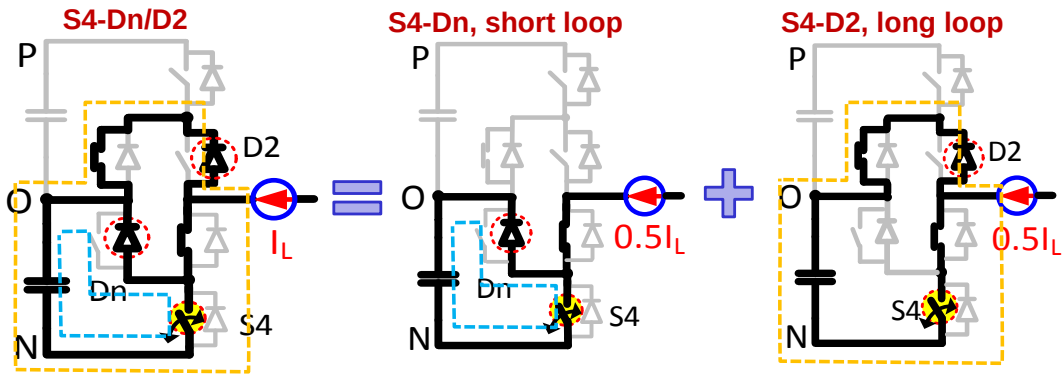


Fig. 4.6. Equivalent switching loops of the new switching loop in 3rd quadrant

the new switching loop in 1st and 3rd quadrant for inverter mode contains one switch commutates with 2 paralleled diode. The new switching loop in 2nd and 4th quadrant for rectifier mode contains 2 paralleled switch commutate with 1 diode.

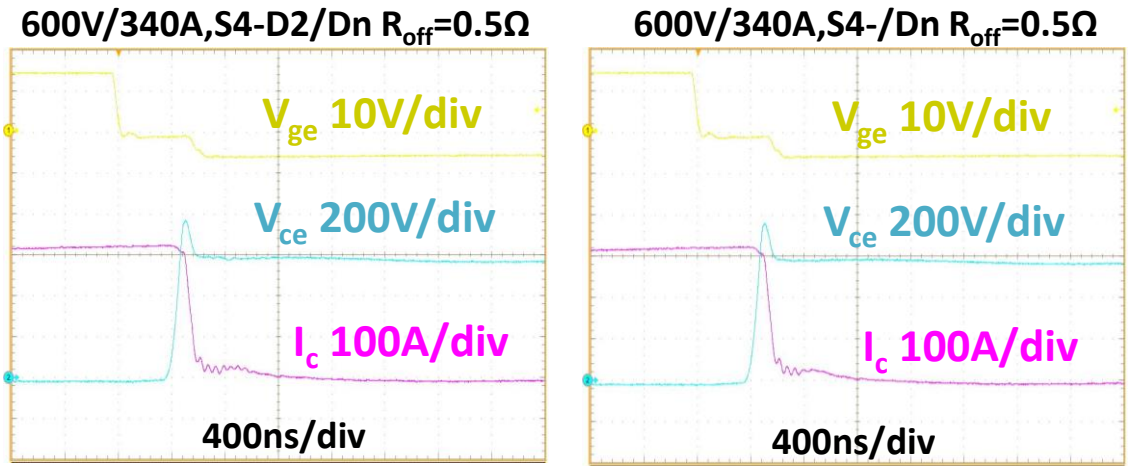
4.2 Switching Characteristic Evaluation for the New Switching Loops

To verify the switching performance of the new switching loops, double pulse tests are conducted. The tests are also based on real phase leg layout. The switching waveforms and characteristics for the new loop in 2nd and 3rd quadrants are explored. Because of the symmetry in this circuit, the switching performance in 1st and 4th quadrants is the same. Since the short switching loop has small loss and stress, it is used as the benchmark for the new switching loop in the same quadrants with the same load current.

It is worth mentioning here about the implementation of the synchronized gate signals for the inner and clamping switches. The test is based on the phase leg module introduced in chapter 2. All the switches have the same gate driver board. The gate signals are transmitted by optic fibers. The complementary gate signals are generated from the ePWM modules in DSP and passed through FPGA for protection. For the synchronized clamping and inner switches, the original signal is also generated in DSP and is duplicated in FPGA to drive the two switches. There is no special gate driver design or extra synchronization mechanism to synchronize the two switches.

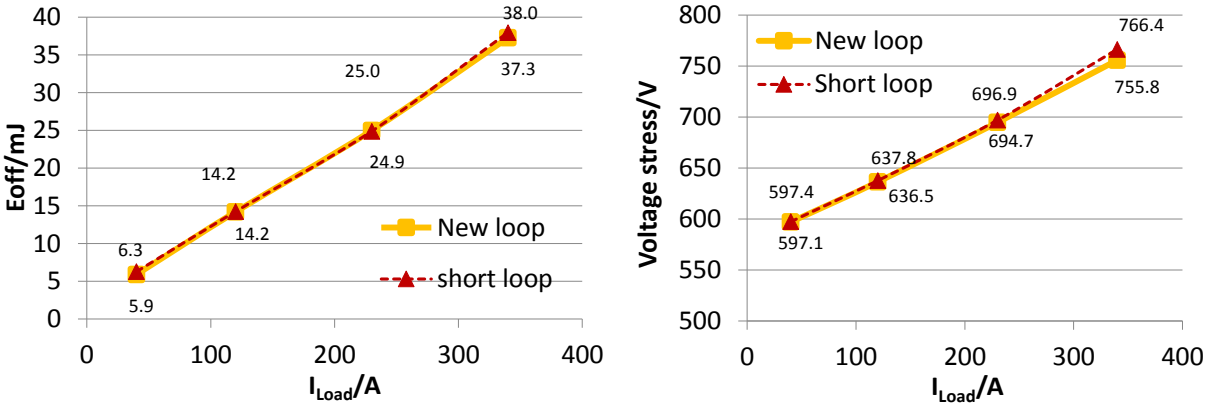
4.2.1 Switching Characteristic in 3rd Quadrant

For the new switching loop in 3rd quadrant, the outer switch S4 commutates with 2 paralleled diodes D2 and Dn. The turn off performance is evaluated first in comparison with the short loop. The turn off waveforms for the two loops are compared in Fig.4.7 at full load current and rated DC link voltage with 0.5Ω turn off resistor. The two waveforms look the same. The turn off characteristics for the two loops at different load current cases are also compared in Fig.4.8. The comparison shows that the new switching loop and the short loop has the same turn off transient with same turn off loss and stress. It is quiet understandable since in both the two loops, the switch S4 turns off a full load current.



(a) New switching loop (b) Short switching loop

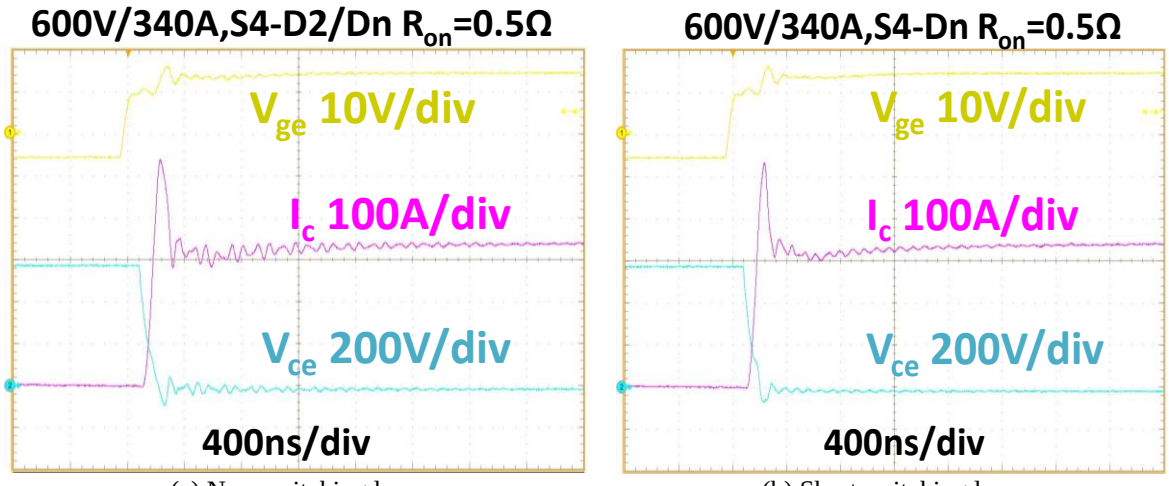
Fig. 4.7. Turn off waveform comparison in 3rd quadrant



(a) Turn off energy (b) Voltage stress

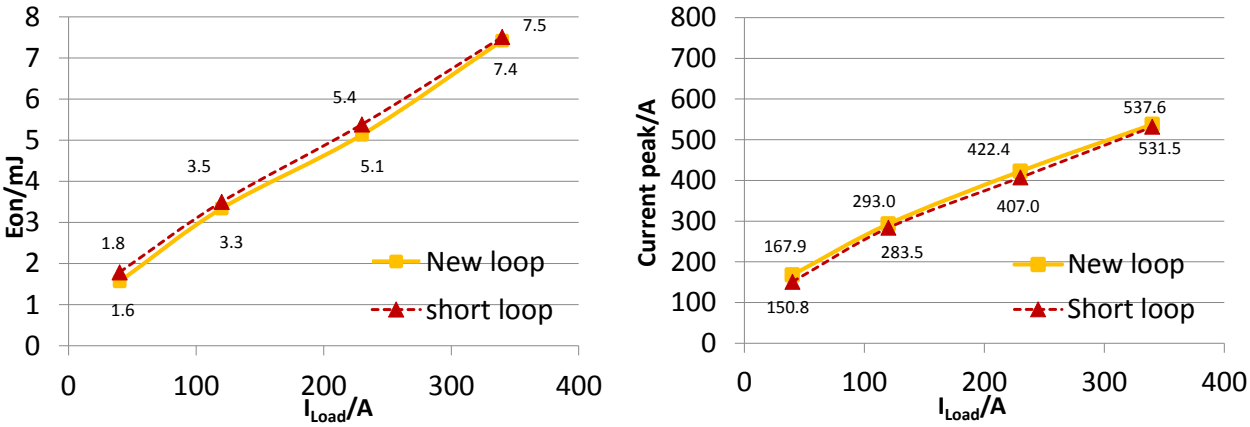
Fig. 4.8. Turn off characteristics in 3rd quadrant

The turn on performance for the new loop is then investigated, also in comparison with the short loop. Fig.4.9 shows the turn on waveform comparison at full load current. The new switching loop and the short loop have similar turn on waveforms. For the new switching loop, the small oscillation performance after reverse recovery is slightly different from that of the short loop. This oscillation is caused by the resonance between junction capacitor of the device and loop parasitic inductance after diode reverse recovery. For the short switching loop, the resonance frequency is solely determined by the loop parasitics. But for the new switching loop, there are two equivalent switching loop, both of which has reverse recovery diode. The parasitic inductance for the two loops are totally different, causing the different resonant frequency of the reverse recovery diode. This is the reason for the slightly different turn on current waveform. The turn on characteristic comparison is shown in Fig.4.10. Similar as the turn off performance, the new switching loop has the same turn on transient, as well as the same turn on energy and reverse recover current peak at all current conditions. As a conclusion, the new switching loop in 3rd quadrant keeps the same switching characteristics as that for the short loop.



(a) New switching loop (b) Short switching loop

Fig. 4.9. Turn on waveform comparison in 3rd quadrant



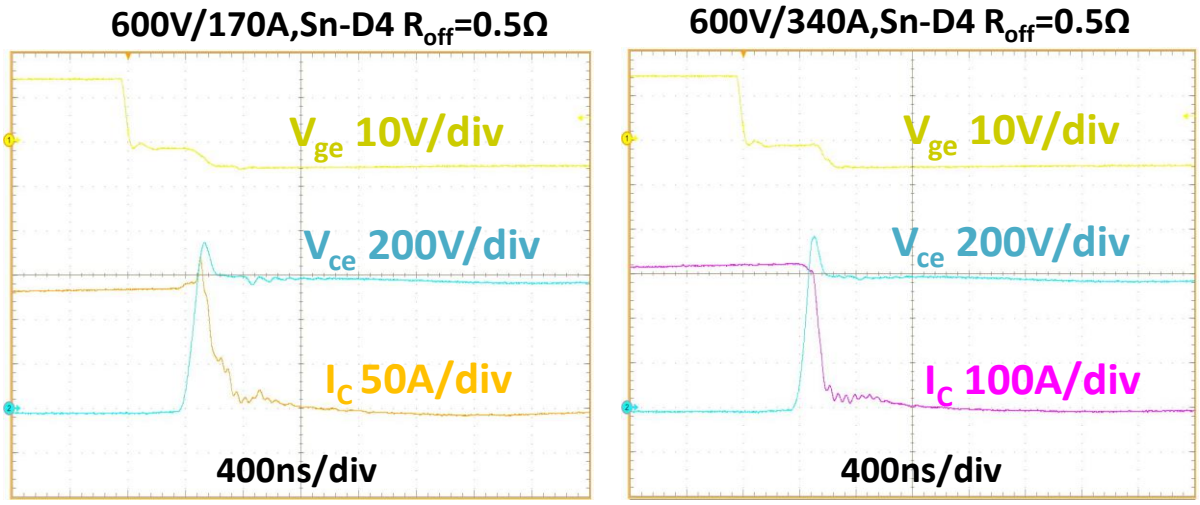
(a) Turn on energy (b) Current peak

Fig. 4.10. Turn on characteristics in 3rd quadrant

4.2.2 Switching Characteristic in 2nd Quadrant

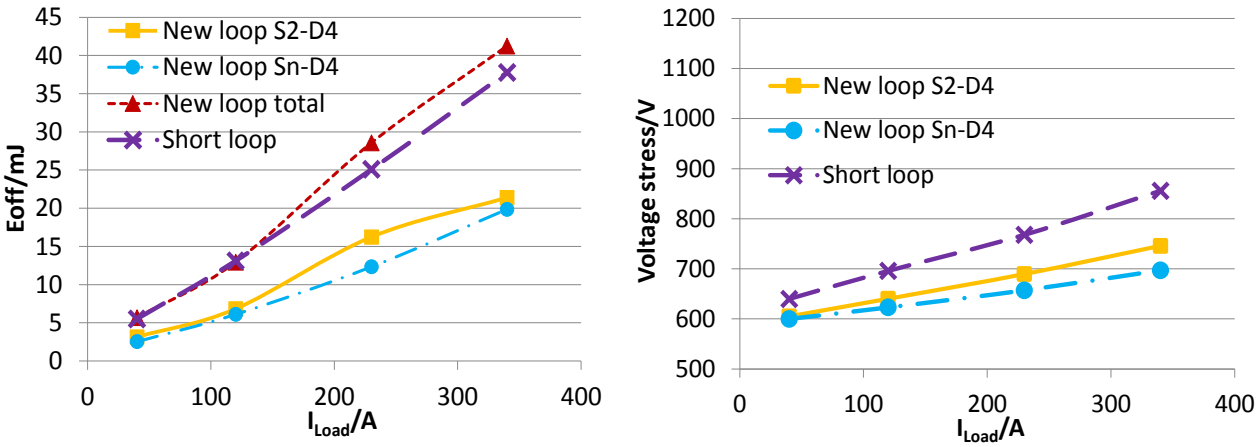
For the new switching loop in the 2nd quadrant, two paralleled switches Sn and S2 commutate with single diode D4. The switching performance for the two switches is evaluated and compared with the switching performance for the short loop. The turn off performance is compared first. Fig.4.11 shows the comparison of turn off waveform for new loop and short loop at peak load current. In the new switching loop, switches Sn and S2 are switched simultaneously and share the load current. Therefore, each of the two switches in the new loop commutates half load current. Fig.4.11(a) shows the turn off waveform for switch Sn. The turn off waveform for the other switch S2 is not shown since it looks the same as that in Fig.4.11(a). As mentioned previously, the new switching loop equals to the combination of a short loop plus a long loop with half load current. As a result, each switch in the new loop has almost half the switching stress and loss compared with original short loop at full load current. Although the two switches equally share the load current, the switch in the short loop (Sn) with smaller parasitics should have lower stress and loss than the one in the long loop (S2). This is verified by the turn off characteristics comparison between the new loop and short loop in Fig.4.12. For the turn off energy in Fig.4.12(a), each switch in new loop has almost half loss of the short loop. The total

loss for the new switching loop is similar as the original short loop. For the turn off stress in Fig.4.12(b), each switch in the new loop have smaller stress than the original short loop.



(a) Sn in New switching loop (b) Short switching loop

Fig. 4.11. Turn off waveform comparison in 2nd quadrant

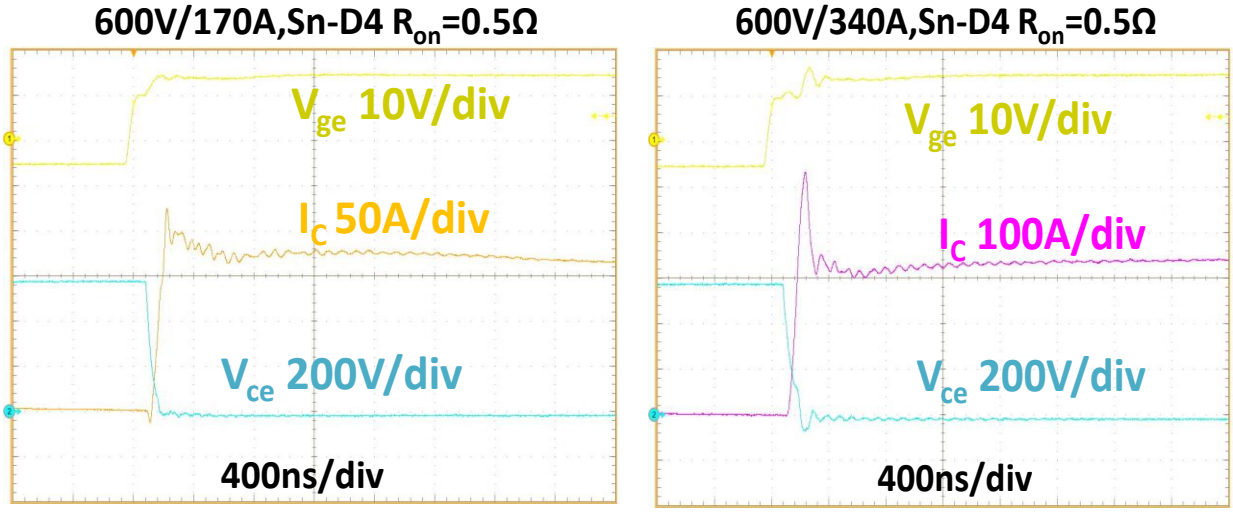


(a) Turn off energy (b) Voltage stress

Fig. 4.12. Turn off characteristics in 2nd quadrant

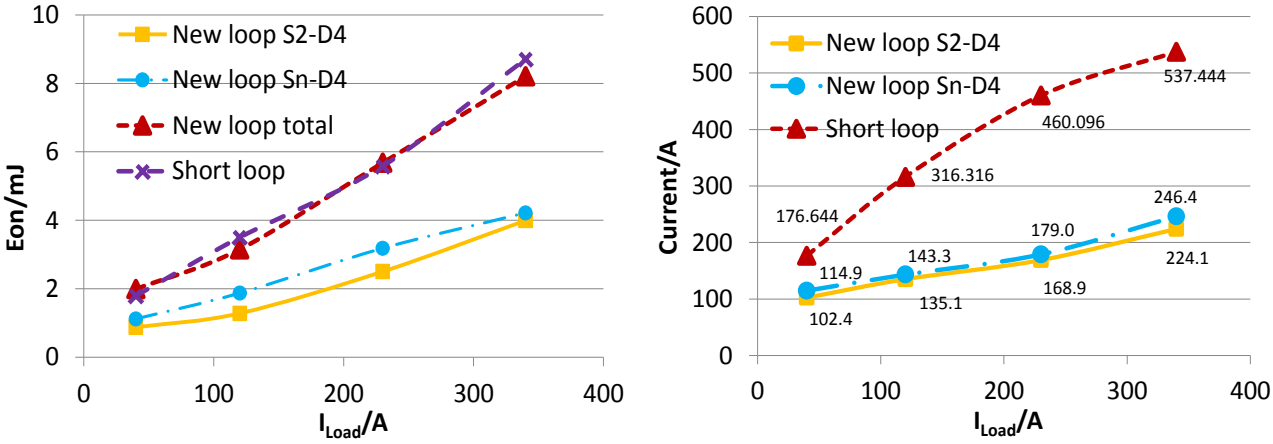
The turn on performance for the new switching loop in the 2nd quadrant is studied in the same way. For turn on transient, the new switching loop also contains 2 paralleled switches that commutate simultaneously with the diode. Both the two switches commutate at half load current, but one is in the short loop while the other one is in the long loop. The turn on waveform comparison for new loop and original short loop at full load current is shown in Fig.4.13. As the switch in new loop takes only half load current, the reverser recovery current peak is obviously

reduced. Fig.4.13 (a) shows the turn on waveform for switch Sn. The waveform for switch S2 is not shown since it is the same as the one for Sn. The turn on characteristic for the new switching loop and the short loop is compared in Fig.4.14. Similar conclusion as for the turn off transient can be drawn for the turn on energy and turn on current peak. The two switches have different turn on energy and reverse recovery current peak due to the difference in their commutation paths. However, the stress and loss for each switch in the new loop is almost half of the loss and stress for the short loop. The total loss for the new switching loop with different load current case are the same as the short loop, but the current peak for switches in the new loop is reduced.



(a) Sn in New switching loop (b) Short switching loop

Fig. 4.13. Turn on waveform comparison in 2nd quadrant



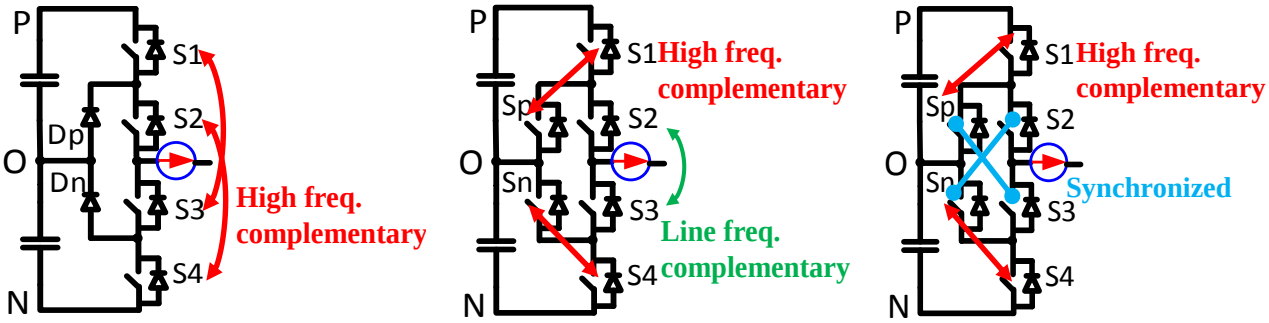
(a) Turn on energy (b) Current peak

Fig. 4.14. Turn on characteristics in 2nd quadrant

4.3 Loss and Stress Quantification for the Proposed Scheme

4.3.1 Phase Leg Loss and Stress Distribution

The switching performance evaluation shows that the proposed modulation scheme with new switching loop has a similar switching loss as for the original short loop, but a largely reduced switching stress in all quadrants and all current conditions. For the 3-level NPC phase leg, there are various modulation schemes introduced in chapter 2.2. The basic operating principles for these modulation schemes are briefly reviewed here in Fig.4.15. The modulation for DNPC in Fig.4.15(a) has two pairs of complementary switches. Each pair contains an outer switch and an inner switch. Also each pair of complementary switches have high frequency switching for half a line cycle. For the conventional ANPC modulation in Fig.4.15(b). There are still two pairs of complementary switches. The top cell outer and clamping switches are in high frequency complementary manner for the positive half line cycle. The bottom cell switch pair is involved in

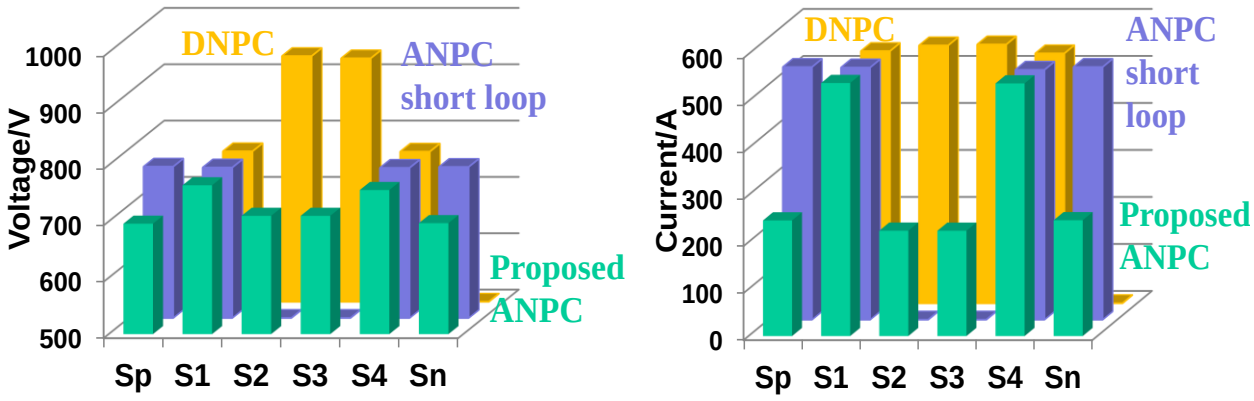


(a) DNPC (b) Conventional ANPC outer mode (c) Proposed ANPC

Fig. 4.15. Switching stress comparison for NPC phase leg with modulation schemes

the negative half line cycle. For the two inner switches, they are also switched in complementary manner, but only switch once in a line cycle. For the proposed ANPC modulation scheme in Fig.4.15(c). The outer and clamping switches for the top and bottom cells still follow the same manner as the conventional ANPC. But the inner switches are synchronized with their diagonal clamping switches instead of doing nothing in a line cycle. As a result, they are also involved in high frequency switching. The variation in modulation schemes results in different stress

distribution patterns for all switches. The maximum voltage and current stress distribution for the phase leg is compared in Fig.4.16 (a) and (b). For DNPC phase leg, the inner switches are more stressed. For ANPC phase leg with outer switch mode, since only short loop is used, the outer and clamping switches are stressed. The inner switches have neither switching stress nor loss since they are switched once per line cycle. For the proposed modulation scheme for ANPC, the inner and clamping switches are switched simultaneously and the load current is shared by these two synchronized switches. Because the commutating current is reduced to half for the two switches, the voltage and current stress is consequently reduced for them. With the proposed modulation scheme, the inner switches share some burden with the clamping switches instead of doing nothing with the conventional outer switch mode. So the proposed modulation has a more evenly distributed stress. The above comparison are made with unity power factor. But for any other power factor cases, since the proposed modulation scheme has same switching loop in all quadrants, the result is the same.



(a) Voltage stress (b) Current stress

Fig. 4.16. Switching stress comparison for NPC phase leg with modulation schemes

The phase leg loss distribution for the proposed modulation scheme under different power factors is investigated in Fig.4.17. Compared with the phase leg loss distribution for conventional modulation schemes in Fig.2.34, Fig.2.36 and Fig.2.38, the proposed method has more evenly distributed loss. It can also be verified from Fig.4.17 that the two inner switches S2 and S3 share

some switching loss for the clamping switches Sp and Sn. For the ANPC outer switch mode in Fig.2.36, the two inner switches only bear conduction loss.

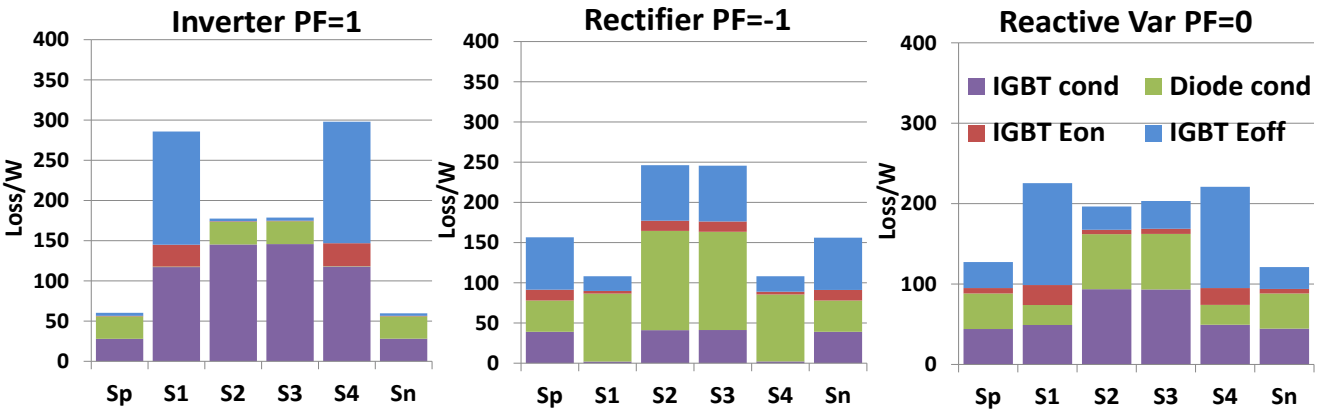


Fig. 4.17. Phase leg loss distribution for proposed modulation scheme

4.3.2 System Total Loss Comparison

Although the new switching loop with the proposed modulation scheme does not reduce the switching loss as shown in the turn on and turn off energy curves, the switching state for the proposed modulation scheme can reduce conduction loss as mentioned previously. Because both neutral current paths are used for neutral state, the equivalent on state resistor for neutral current is reduced to half. The neutral state occurs in both the positive and negative half line cycle and it takes 44% percent of the duty cycle in the whole line cycle for SVM strategy. Consequently, the conduction loss can be dramatically reduced for the proposed modulation scheme. A detailed loss breakdown in Fig.4.18 for different modulation strategies and schemes shows the loss reduction result at different power factor cases. Comparing with the SPWM strategy, the SVM strategy proposed in chapter.3.4 has reduced switching loss but the same conduction loss. This is because this SVM strategy has only 4 switching events in each switching cycle while the SPWM strategy has 6 switching events per cycle. But the SVM strategy for neutral point voltage balance has some issue when using the conventional ANPC modulation schemes as introduced in the beginning of chapter 4.1. With the proposed modulation scheme, the SVM strategy can be used

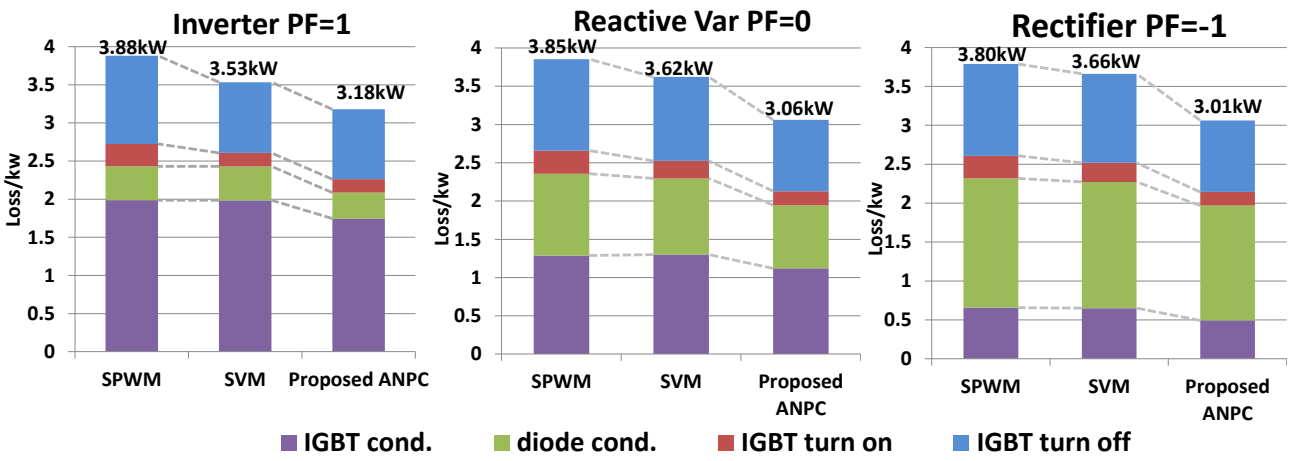


Fig. 4.18. Total system loss breakdown for different modulations with power factor

for ANPC to have the minimum switching loss and switching cycle NP balance. Besides that, the conduction loss for proposed modulation scheme is also reduced compared with the conventional modulation scheme at all power factor cases. The quantitative analysis of loss breakdown reveals that the proposed modulation scheme can reduce 15% conduction loss compared with the conventional one. Finally the total system loss for different modulation schemes and modulation strategies is compared at all power factors in Fig. 4.19. For the DNPC and ANPC with SPWM modulation, the loss curve is already analyzed in Fig.2.40. For the SVM modulation strategy, the

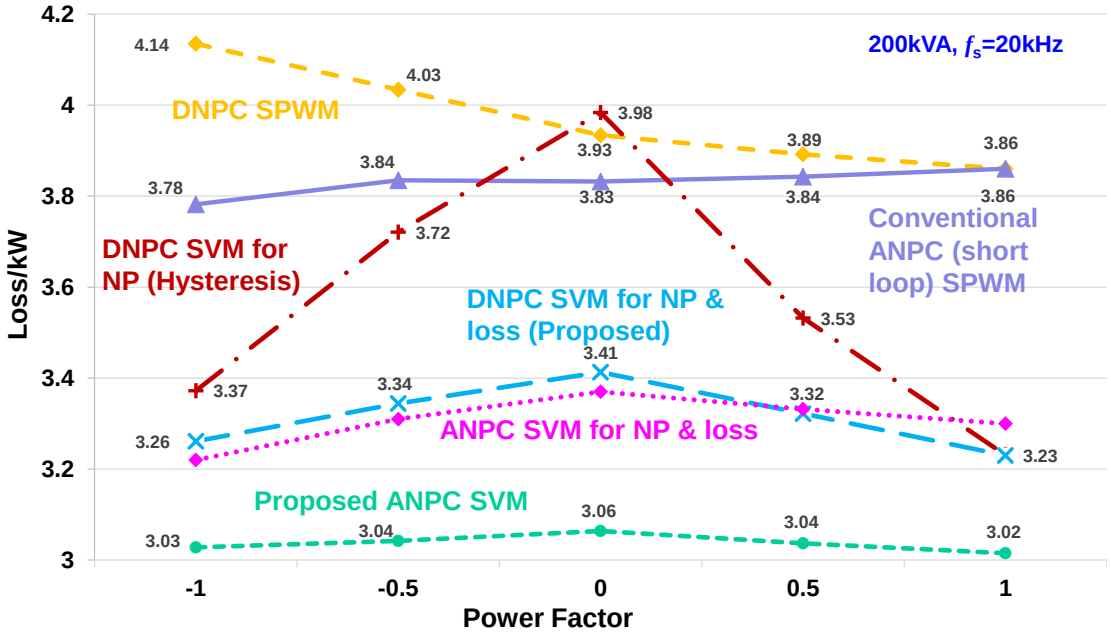


Fig. 4.19. System total loss comparison for all modulation schemes

switching loss is reduced so the loss curve is shifted downward. For the proposed modulation scheme with SVM modulation strategy, the conduction loss is further reduced so that the loss curve is even lower. Finally, a 3-lelvel ANPC converter with the proposed modulation scheme can reach 98.5% power stage efficiency with 200kVA power rating and 20kHz switching frequency at all power factors.

4.3.3 System Experimental Result

Finally, the propose modulation scheme is verified on the 200kVA, 20kHz 3-level ANPC power converter hardware. The system structure for the DC/AC converter is shown in Fig.4.20. The system rating for the converter is shown in Table.4.2. The power stage is constructed by the modularized phase leg building block introduced in chapter.2. The LCL filter is used as the grid interface harmonic filter. The control system contains a DSP and a FPGA as IO extension. For the proposed method, only 2 ePWM channels of the MCU is used per phase to generate the 2 pairs of complementary gate signals. Then the two synchronized gate signals are duplicated in the FPGA. Compared with the conventional ANPC modulation which requires 3 ePWM channels to generate 6 gate signals, the implementation for the proposed modulation is simplified.

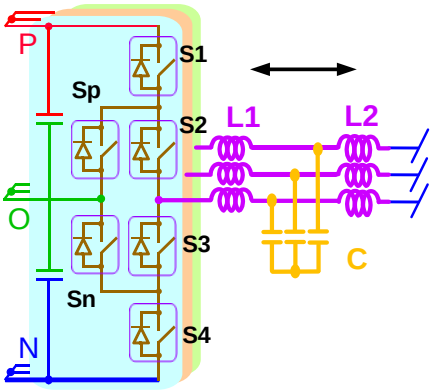
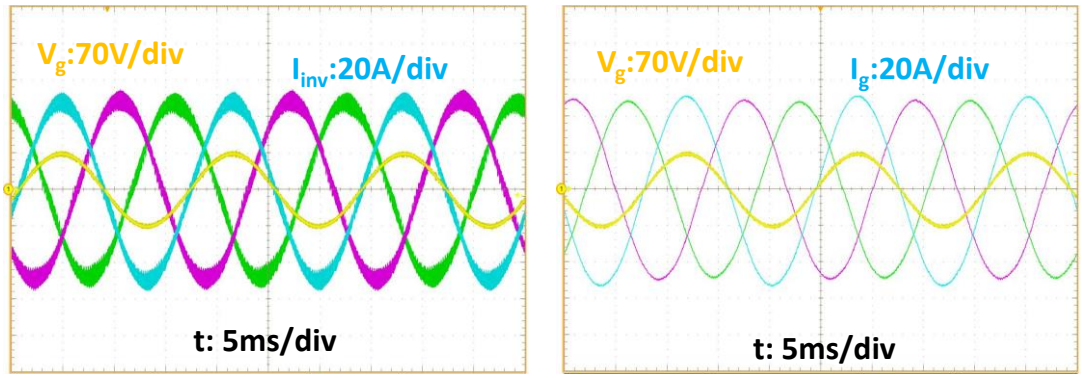


Fig. 4.20. System structure for the 3-level ANPC converter

Table 4.2. System rating for the 3-level ANPC converter

S_N	f_{sw}	V_{grid}	V_{dc}	L1	L2	C
200kVA	20kHz	480V	1.2kV	0.1mH	0.27mH	10μF

The converter output voltage and current waveforms are shown in Fig.4.21. Different operating conditions are tested and the unity power factor case with inverter mode is shown. Fig.4.21(a) and (b) gives the 3-phase inverter output current and grid current waveform with grid voltage. The waveforms verify that the proposed modulation scheme works at all power factor cases with reduced stress and loss.



(a) Inverter output current (b) Grid current

Fig. 4.21. Converter output voltage and current waveforms

4.4 Summary and Conclusion

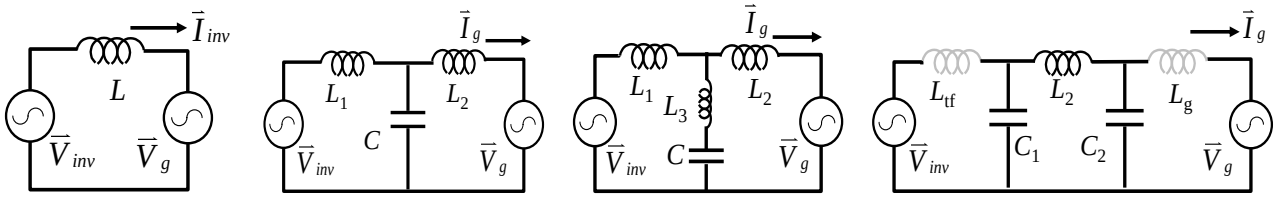
In this chapter, a new modulation scheme for 3-level ANPC phase leg is proposed. The conventional modulation schemes have some issues when using a SVM modulation strategy with NP voltage balance. The proposed modulation scheme solves this problem. Taking advantage of the flexibly configured neutral current path for ANPC phase leg, this modulation scheme uses both neutral paths to conduct neutral current. Thus the conduction loss is significantly reduced. Compared with the conventional modulation schemes for ANPC, which have different neutral state for positive and negative half line cycle, the proposed modulation scheme has a unified neutral state for both the positive and negative half line cycle. With the new modulation scheme, new switching loops for the 3-level ANPC phase leg is generated in the four quadrants operation.

The new switching loops have two pairs of complementary switches and two pairs of synchronized switches. The two inner switches share the loss and stress for the two clamping switches instead of doing only line frequency switching for the conventional method. In the new switching loops, two paralleled switching devices commutate simultaneously with another switching device. So the load current is shared by the two switches and the switching stress is reduced. The double pulse tests measures the switching characteristics for the new loops. It shows a largely reduced switching stress and basically unchanged switching loss for the new loop. The phase leg loss distribution shows the more evenly distributed phase leg loss and stress. Also the system loss breakdown shows a 15% conduction loss reduction. With this modulation scheme, the 200kVA 3-level ANPC power converter operating at 20kHz can reach up to 98.5% efficiency at all power factors. Another benefit for the proposed method is that only 2 pairs of PWM channels are needed for each phase leg. So the 3-phase system can save 6 PWM channels. The proposed method is verified on the 200kVA 3-level ANPC converter hardware. The research contributions in this chapter is concluded in the following:

1. Investigated the issue of conventional ANPC modulation scheme used for the SVM with switching cycle NP balance.
2. Proposed a new modulation scheme for 3-level ANPC phase leg with reduced conduction loss and switching stress.
3. More evenly distributed switching stress and loss for all the devices on the phase leg.
4. Simplified implementation for the modulation scheme and saved PWM channels
5. Detailed loss and stress distribution comparison for the proposed schemes with other modulation schemes for 3-level NPC.

CHAPTER.5 LCL FILTER DESIGN FOR 3-LEVEL NPC GRID INTERFACE CONVERTER

With the modularized phase leg building block designed and the modulation strategy determined, the next step for the power conversion system design is to develop the harmonic filter for the grid interface converter. This filter is essential to attenuate the current harmonics and to meet the grid code requirement for the grid-tied application. This chapter investigates the harmonic filter design for the bidirectional 3-level NPC gird interface converter. To find a suitable topology for the harmonic filter, different filter structures are evaluated and several typical topologies are shown in Fig.5.1. The simplest structure in Fig.5.1(a) uses an inductor to connect the VSI to the grid. It has the least number of components but with only 20dB/dec attenuation. A large inductance value is needed to meet the grid standard. The LCL filter structure in Fig.5.1(b) is the most widely used structure. It has 60dB/dec attenuation at high frequency and relatively small size [1]-[2]. The leakage inductance at grid side sometimes can play the role of L2, therefore only 2 components are required. The LLCL filter in Fig.5.1(c) is proposed in [3]. This structure is based on LCL structure with an extra inductor. This extra inductor resonates with capacitor and provides a resonant notch on the filter transfer function. The resonant notch can be placed at the switching frequency to eliminate this major harmonic component. This filter has good attenuation at notch frequency but sacrifices some high frequency attenuation. Also it requires extra component. There are even more topological variations for the harmonic filter with more components and complex structures [4]. Some filter has two stages and utilizes the grid leakage inductance as part of its structure. The filter in Fig.5.1(d) is a 2-stage LCL filter which utilizes the leakage of the isolation transformer and the grid leakage inductance. This filter structure has even better attenuations at high frequency and



(a) L filter (b) LCL filter (c) LLCL filter (d) 2-stage LCL filter

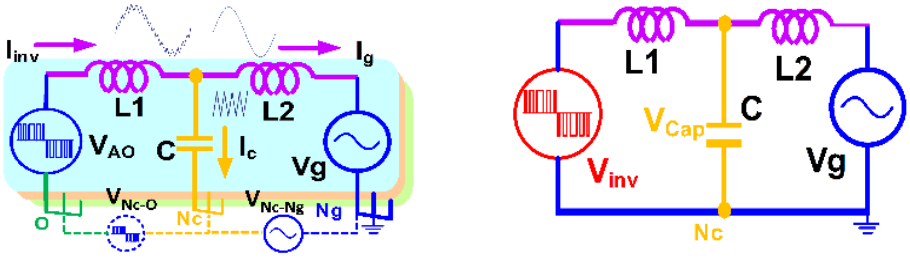
Fig. 5.1. Typical harmonic filter topologies

functions as both harmonic filter and EMI filter. But the added components increase the size, weight and cost for the whole system. Also the leakage inductance variation influences the filter performance. The high order transfer function with multiple resonant peak is another issue for the damping circuit design. Based on the evaluation, LCL filter is the basis for other topologies and has the best trade-off between the attenuation and the component size.

Although there are vast majorities of literatures that introduce the LCL filter design for grid interface converter [1]-[9]. The discussed issues include basic design guidelines [5], magnetic design and integration for filter [6], control issue with LCL filter [7] or damping circuit [8]. Only a few focus on the 3-level NPC topology [9], [10]. And even few have detailed analysis on the inductor current ripple with certain modulation scheme and pulse sequence [11]. In this chapter, the basic design procedure and guideline for the LCL filter is introduced. Then the current ripple for the inverter side inductor L1 is thoroughly analyzed. An analytical expression for the maximum inductor current ripple is established. The ripple distribution in a line cycle is studied under different power factor cases. The L1 inductance is determined by loss and inductor size trade-off. The grid side inductor is designed according to the grid code attenuation requirement. Different damping circuit are also explored and compared in detail. The best topology is chosen from several damping circuit candidates. The filter parameters are finally verified by the simulation and experimental result on the 3-level NPC converter.

5.1 Equivalent Circuit and Design Guideline for LCL Filter

It is essential to derive the equivalent circuit of the 3-phase inverter for the filter design and inductor current ripple analysis. Fig.5.2(a) shows the 3-phase equivalent circuit for the inverter with LCL filter. The voltage source V_{AO} represents the inverter output voltage of phase A and the voltage source V_g is the grid voltage. In a balanced and symmetrical 3-phase system, there is



(a) 3-phase equivalent circuit (b) Single phase equivalent circuit

Fig. 5.2. Equivalent circuit for LCL filter

a common mode voltage between the neutral point O and the capacitor common point Nc. This CM voltage is $V_{CM}=1/3(V_{AO}+V_{BO}+V_{CO})$, which is the same expression as in equation 3-12. The voltage across Nc and the grid ground Ng can also be derived as

$$V_{Nc-Ng}=\frac{1}{3}(V_{CA}+V_{CB}+V_{CC}) \tag{5-1}$$

where V_{CA} is the voltage across the filter capacitor of phase A. Then the single phase equivalent circuit for LCL filter can be derived in Fig.5.2(b). At inverter side, a voltage source V_{inv_A} represents the combined phase A output and the CM voltage.

$$V_{inv\_A}=V_{AO}-V_{CM} \tag{5-2}$$

At grid side, considering only line frequency component and the balanced 3-phase system, the summation of the 3-phase capacitor voltage has the following relationship

$$V_{CA}+V_{CB}+V_{CC}=0 \tag{5-3}$$

Thus the grid ground can be directly connected to Nc. The equivalent circuit shows that the inverter output voltage V_{inv} together with the capacitor voltage determines the current ripple on the inverter side inductor L1. This inductor deals with high frequency ripple current and thus

faces the excessive core loss. The capacitor sinks the majority of high frequency ripple current of I_{inv} and mainly leaves line frequency component in grid current. The grid side inductor L2 provides the major attenuation for the grid side current to meet the grid code.

For the LCL filter, there are certain design constraints that set up the boundary for the component parameters. For L1, a larger inductance is desirable to give small current ripple, but it also raises the cost with the high price for the high frequency core material. The capacitor also influences the current ripple. Larger capacitance value provides a better high frequency ripple current sink, but it also consumes more reactive power at line frequency and shifts the power factor at grid side. The tolerable reactive power consumption by C is typically set to 2%-5% of the total system power rating. Then the maximum capacitance can be calculated in 5-4 and 5-5 where V_{ph} is the RMS value of the phase to neutral output voltage. Considering the system rating for the 3-level NPC converter, the maximum capacitance is calculated as 46μF.

$$Q_c \approx V_{ph}^2 \cdot \omega_{line} C \le 2\% \cdot \left(\frac{S_N}{3} \right) \tag{5-4}$$

$$C \le \frac{2\% \cdot S_N}{3V_{ph}^2 \omega_{line}} = 46\mu F \tag{5-5}$$

The grid side inductor L2 achieves the harmonic attenuation. Larger inductance provides higher attenuation at high frequency. But the total inductance for L1 & L2 should not be too large to cause significant line frequency voltage drop on them. The phasor diagram for a grid interface converter is shown in Fig.5.3, in which the inverter output voltage V_{inv}, grid voltage V_g and inductor voltage V_L are represented by vectors. For the 4-quadrant power conversion system with bidirectional power flow, all the operating conditions like inverter mode, rectifier mode and 0 power factor case should be considered. Fig.5.4 gives the vectors' relationship under 4 specific modes. The DC link voltage determines the maximum V_{inv} and thus imposes the voltage drop boundary on the inductor. Then the maximum total inductance can be calculated as:

$$L_1 + L_2 \le \frac{V_{inv} - V_g}{\omega_{line} \cdot I_g} = 3.9mH \tag{5-6}$$

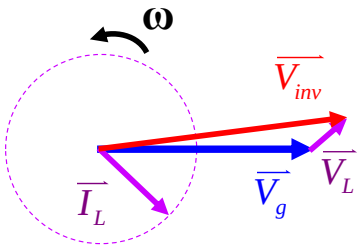


Fig. 5.3. Line frequency phasor diagram of LCL filter

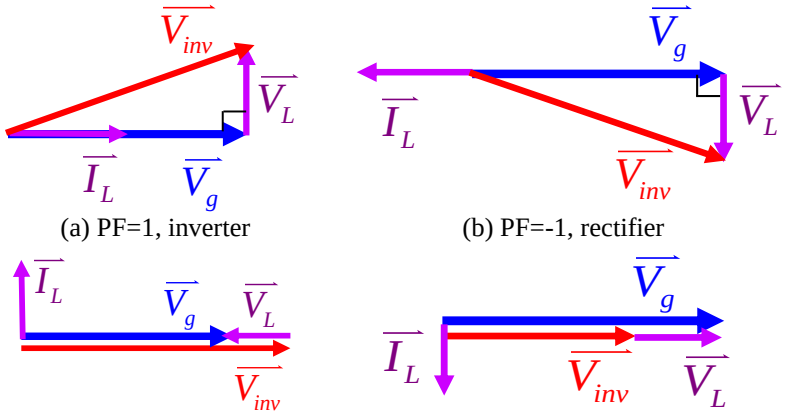


Fig. 5.4. Phasor diagram at different power factors

Besides this individual limitations for each component value, the three components together determine the LCL resonant frequency. This frequency also has boundary. The lower boundary is typically set to be larger than 10 times of the line frequency to avoid the major low frequency harmonics. These harmonics are dealt with by the control loop. The upper boundary is usually below half switching frequency to avoid resonance with these major frequency components.

5.2 Inductor Current Ripple Analysis

The inductor current ripple on inverter side inductor L1 is critical to the filter design since L1 is the key part that connects the inverter power stage and the grid. For this reason, it influences both the power stage loss and the grid current harmonics. Moreover, its high frequency core material takes a large percentage of the filter total cost.

5.2.1 Maximum Inductor Current Ripple Derivation

The equivalent circuit in Fig.5.2(b) indicates that the inductor voltage is determined by V_{inv} and V_{cap}. The capacitor voltage in a switching cycle is nearly constant. Then the inductor current ripple is dominated by V_{inv}, which is further influenced by the modulation scheme and pulse sequence of the 3-phase vectors. The SVM with NP balance and loss reduction in Chapter.3 is still used here. As introduced in Chapter.3, this modulation uses the nearest three vectors to synthesis the reference voltage. The pulse sequence is symmetrical with 5 pieces of segments in each switching cycle as shown in Fig.3.31(b). Taking phase C for instance, the inverter output voltage V_{inv}, capacitor voltage V_{cap} and the inductor voltage V_{L1} of this phase can be simulated in the line cycle as shown in the left part of Fig.5.5. If zoomed in to one switching cycle, the current ripple can be analyzed in detail in the right part of Fig.5.5. There are two assumptions made for

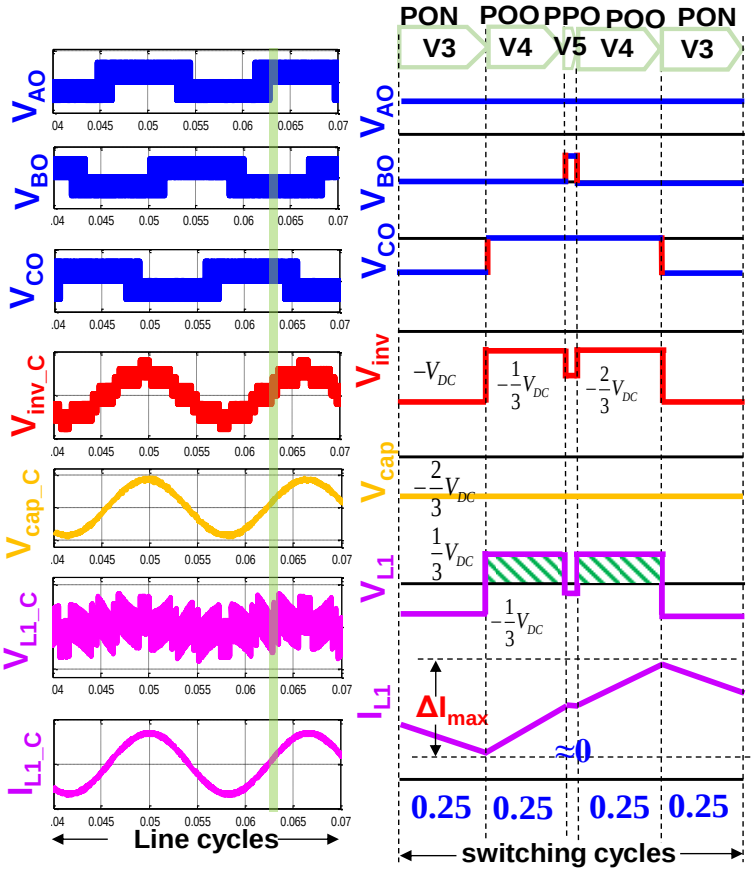


Fig. 5.5. Inductor voltage & current waveform

derivation simplicity. The first assumption is that within each 50μs switching cycle, the capacitor voltage is assumed to be constant. The other one is that in each switching cycle, the volt-second on inductor L1 is assumed to be roughly balanced so that the inductor current does not change dramatically from cycle to cycle. With these two assumption, V_{cap} can be approximated to be the average value of V_{inv} in switching cycle. Then the analytical expression for V_{inv}, V_{cap} and V_{L1} can be derived in 5-7 to 5-9 with the vector duty cycle known from the modulation scheme.

$$V_{inv\_C} = V_{CO} - V_{CM} = \frac{2}{3}V_{CO} - \frac{1}{3}V_{AO} - \frac{1}{3}V_{BO} \tag{5-7}$$

$$V_{cap} \approx V_{avg} = V_{inv(V3)}d_{V3} + V_{inv(V4)}d_{V4} + V_{inv(V5)}d_{V5} \tag{5-8}$$

$$V_{L1} = V_{inv} - V_{cap} = V_{inv} - V_{avg} \tag{5-9}$$

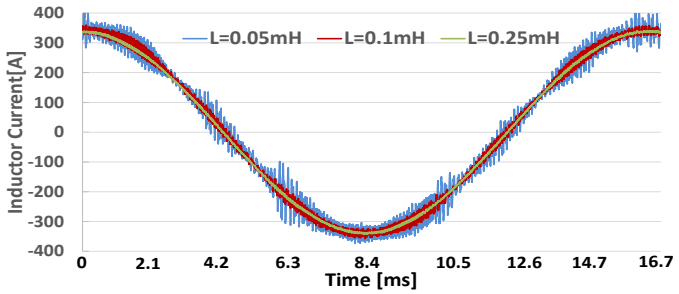
The right part of Fig.5.5 shows that in a switching cycle, the waveform of V_{L1} and I_{L1} have 5 segments and the volt-second is roughly balanced. The current ripple ΔI is defined as the peak to peak value of inductor current in the switching cycle. With the given SVM scheme, the worst case for current ripple in the line cycle can also be identified. It occurs when the duty cycle for one vector is nearly zero and the other 2 vectors equally divide the switching period as shown in the switching cycle waveform in Fig.5.5. Under this circumstances, the inductor current keeps rising or falling for almost half switching cycle. The duty cycle for the three vectors are known as $d_{V5} \approx 0$, $d_{V3} = d_{V4} \approx 0.5$. Then the volt-second on L1 is certain and the maximum current ripple ΔI_{max} in a line cycle can be calculated as follow, where V_{DC} is half DC link voltage

$$\Delta I_{\max} \approx \frac{V_{DC}T_{sw}}{6L_1} \tag{5-10}$$

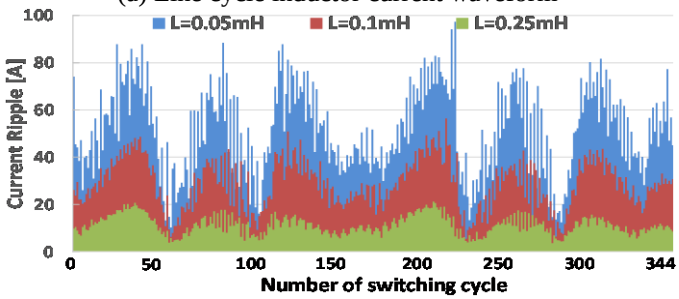
This analytical expression estimates the relationship between L1 inductance and its maximum current ripple in a line cycle. Actually it applies to all the 2-phase SVM modulation or DPWM modulation for 3-level NPC converter, not only the particular SVM method in this dissertation. No matter the pulse sequence is symmetrically or asymmetrically aligned, the volt-second on

inductor keeps the same and gives the same current ripple. The only determinant factor is the vectors used in the switching cycle.

Since the derivation involves some assumptions, it is necessary to verify this estimation with real case simulation. The inductor current is simulated at unity power factor with several L1 inductance value. The current waveforms in Fig.5.6(a) are recorded and analyzed in every switching cycle. The peak to peak value of inductor current is calculated cycle by cycle and a current ripple bar chart is drawn in Fig.5.6(b). The height of each bar indicates the current ripple amplitude in one switching cycle. The whole chart depicts the current ripple distribution in a line cycle. With this bar chart, the real maximum current ripple in line cycle can be easily identified. Also the estimated value can be verified by simulation. The comparison of the estimated and simulated maximum ripple in Fig.5.7 shows a good match between the real ripple and the estimated ripple, which verifies the accuracy of equation 5-10. In addition, a direct relationship between L1 inductance and the maximum current ripple in line cycle ΔI_{max} is found. It is clearly observed from 5-10 and Fig.5.7 that L1 and ΔI_{max} has an inverse-proportional relationship.



(a) Line cycle inductor current waveform



(b) Line cycle inductor current ripple bar chart

Fig. 5.6. Line cycle inductor current waveform & its ripple bar chart

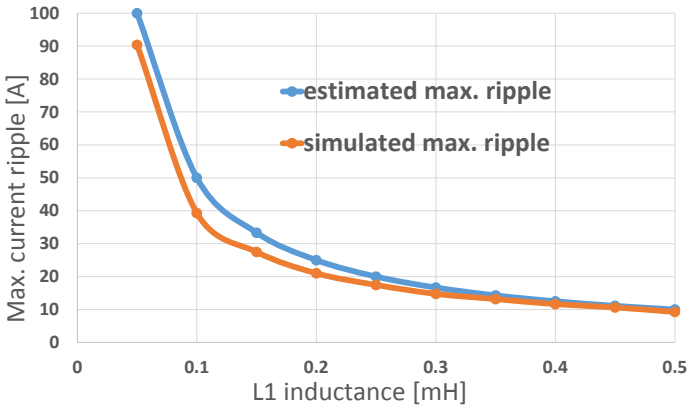


Fig. 5.7. Max. current ripple w/. L1 inductance

5.2.2 Inductor Current Ripple Distribution with Power Factor

The above simulation results are all based on unity power factor case. However, the non-unity power factor cases are inevitable for the grid interface converter. The power factor is an influential factor that determines not only the current ripple distribution in the line cycle, but also the absolute maximum current on the inductor. For this reason, the inductor current ripple distribution with different power factor is investigated and the same bar charts are displayed in Fig.5.8. It shows that the current ripple distribution patterns indeed varies with the power factor. Fig.5.9 also provides a quantitative analysis of the maximum current ripple and current stress with different power factor. Fig.5.9(a) indicates that the maximum current ripple for different

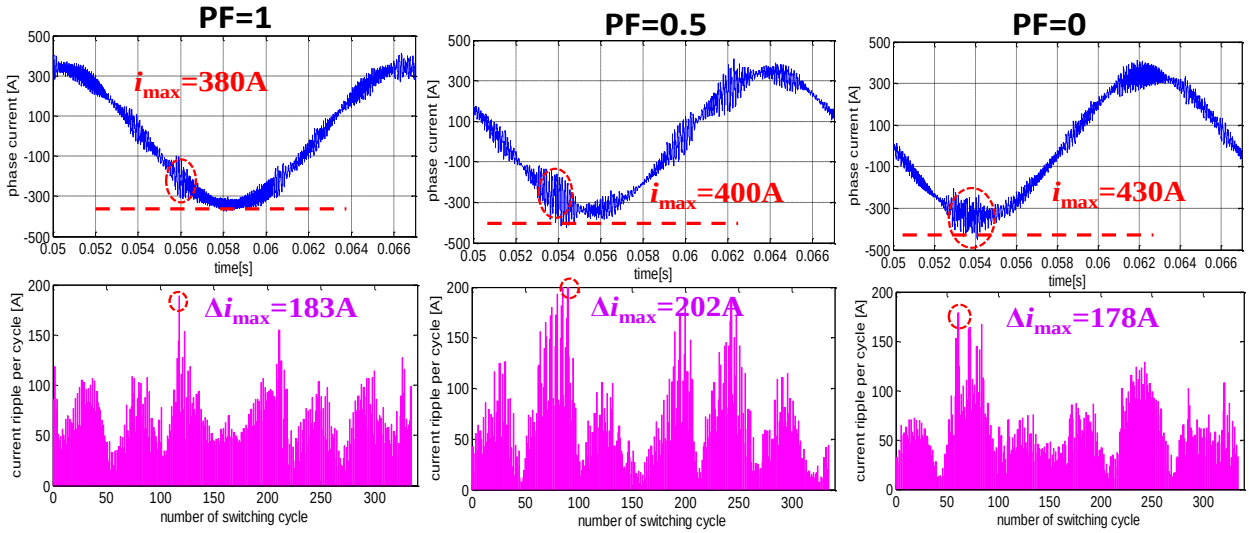
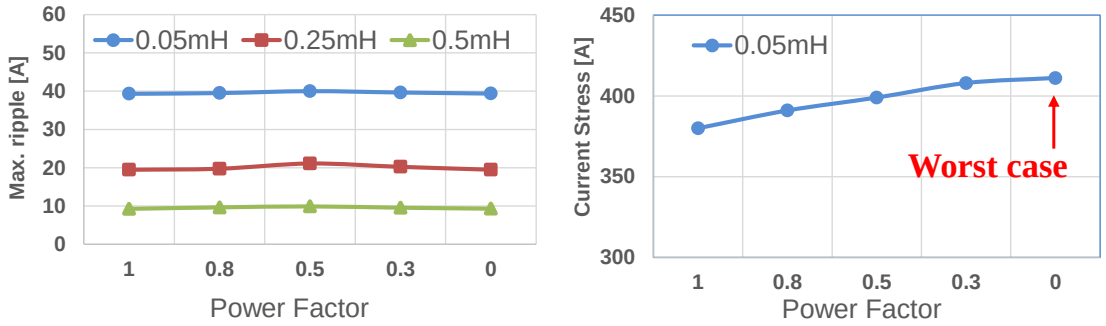


Fig. 5.8. Current ripple distribution with power factor

power factor cases are basically the same at a certain L1 inductance. Although the peak value for the current ripple is the same, the maximum ripple happened at different position under different power factor cases. The position where the maximum current ripple occurs determines the absolute current stress on the inductor and the semiconductor devices. At low power factor, the maximum current ripple occurs around the peak current point in line cycle, which means larger absolute current value. Fig.5.9(b) further reveals that the lower the power factor is, the higher current stress for the inductor and power stage. The worst case occurs at zero power factor when the inductor undertakes the highest current stress. This high current may easily saturate the core of inductor L1 and causes disastrous consequence. The saturation current should be determined by the worst case current stress. As a result, it is meaningful to identify the worst case to design the core for inductor L1 saturation.



(a) Max. current ripple on L1 (b) Max. current stress on L1

Fig. 5.9. Max. current ripple and stress for L1 with power factors

5.2.3 Inductor Current Ripple's Influence on System Loss

Besides the influence of current ripple on the inductor saturation value, the ripple current also influences the power stage loss since the ripple current also appears in the semiconductor devices. The total system loss is thus analyzed with different inductance and their corresponding maximum current ripple. The total loss in line cycle is also quantified by the loss model in Chapter.2. The total system loss with different L1 inductance and the maximum current ripple percentage ($\Delta I_{max}/I_{max}$) is shown in Fig.5.10. Also the grid side inductance L2 is taken into

consideration in the analysis. As discussed previously, the grid side inductor L2 does not have too much influence on the current ripple at inverter side. An important information in the loss analysis is that when the L1 inductance is large enough, the system loss does not change too much, which means a basically constant system efficiency. Therefore, the system loss can be quantified by L1 inductance and also the maximum current ripple percentage. There is a knee point on the loss/inductance curve. Any larger inductance beyond this point does not reduce the current ripple and system loss so much, but increases the inductor size and cost. For any inductance smaller than the knee point, it gives extremely large current ripple and system loss. From the inductor size/cost and system loss/ripple point of view, the knee point is the optimum point for loss and size trade-off. Based on that criteria, the L1 inductance can be selected. Meanwhile, the L1 and ΔI_{max} relationship in equation 5-10 also shows an optimum point around 15% inductor current ripple. This optimum ΔI_{max} can be easily calculated with the inverse proportional relationship in equation 5-10. The 15% current ripple value matches most of the industrial filter design guidelines which also selects the inductance to give 15%-20% ripple. With the chosen L1 inductance around 0.1mH, the total system loss is around 3.25kW at 20kHz switching frequency and 200kW power rating from Fig.5.10. So the system efficiency is 98.5%, which is relatively high for such a high frequency high power converter.

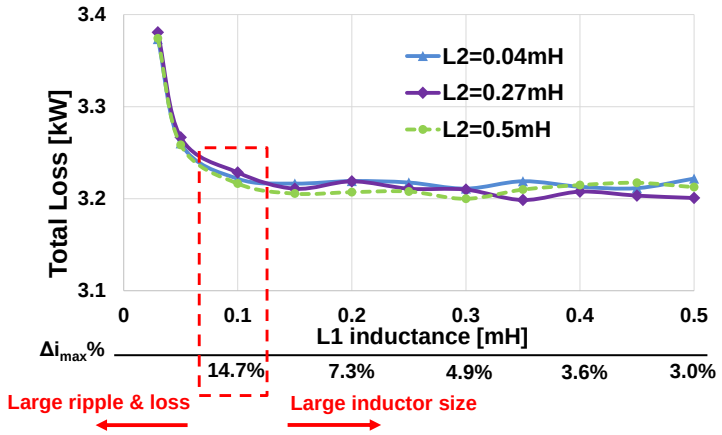
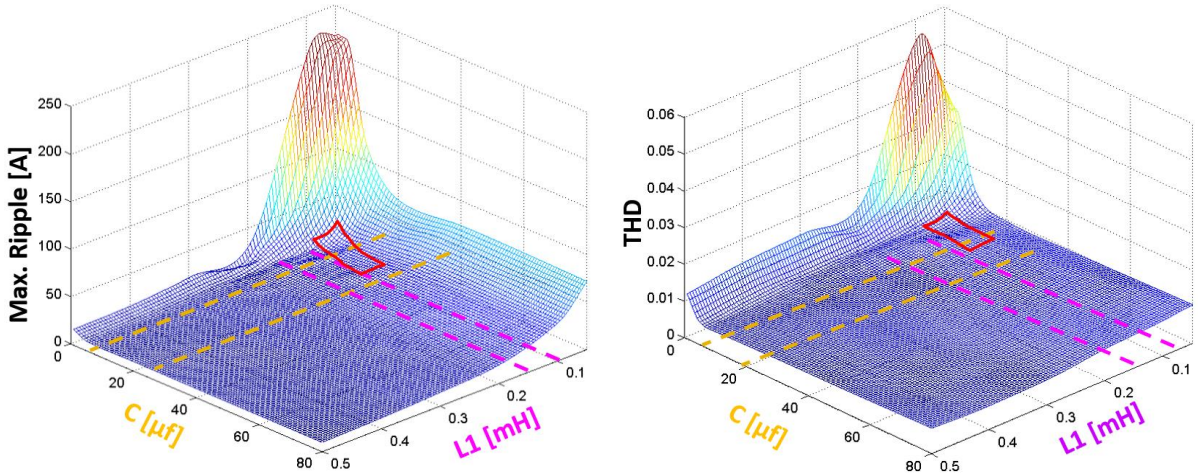


Fig. 5.10. Total system loss with L1 inductance & current ripple

5.3 Capacitor and Grid Side Inductor Design

5.3.1 Inverter Side Inductance and Capacitance Design

The selection for L1 inductance is determined by the current ripple and also the related current stress and loss. The filter capacitor C absorbs the ripple current and impacts both the inverter side and grid side current. Since the capacitor works together with L1, their influence on the inverter side current ripple and grid side current THD is analyzed together. The 3-D surface in Fig.5.11(a) shows the inverter current ripple with different L1 and C values. The capacitance of C impacts the current ripple in a similar way as the L1 inductance, whereas the current is more sensitive to L1 inductance than the capacitance. In terms of the THD for grid current, the same 3-D surface is shown in Fig.5.11(b). The influence of C & L1 on THD follows the same pattern as they influence the current ripple. The only difference is that the THD and C/L1 relationship is non-monotonous. This is because C and L1 decide the resonant frequency in a non-monotonous way and so does the resonant frequency's influence on THD. In both the 2 surfaces in Fig.5.11, an optimum region for inverter current ripple and grid current THD can be found. This region gives the best inductor/capacitor size and ripple/THD trade-off. This region is marked by the solid line on both 2 surfaces. It also provides a boundary for the capacitance and L1 inductance



(a) Inverter max. current ripple with L1 and C (b) Grid current THD with L1 and C

Fig. 5.11. Current ripple & THD vs. L1 & C

selection. For the specific converter in this dissertation, the boundary for capacitance is 10-20μF and the L1 inductance is around 0.08-0.15mH. Another boundary to be considered is the reactive power consumption on C and the voltage drop on L, which is limited by equation 5-5 and 5-6 introduced in previous session. The selected parameters are cross checked by these boundaries and the chosen L1 inductance and capacitance are 0.1mH and 10μF respectively.

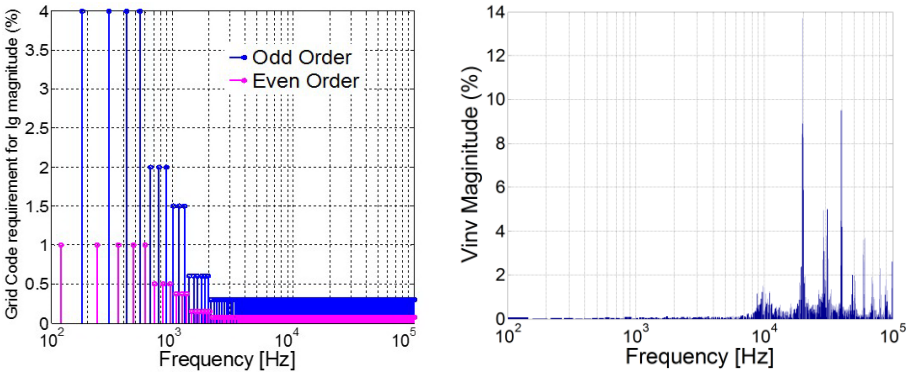
5.3.2 Grid Side Inductance Design

In this design, the grid is assumed to be ideal with negligible leakage inductance. Therefore, the grid side inductor L2 is responsible for the harmonic attenuation so that the grid code can be met. The commonly followed grid code are IEEE 519 and IEEE 1547 standard for the grid interface converter in distributed generation and renewable energy system, which limit the amplitude of each harmonic component and the THD of the grid current. The harmonic current restriction on the odd order harmonics of these 2 standards is shown in Table.5.1. The even order harmonic requirement is half of the odd order harmonics. The restriction for each individual harmonic component can be drawn in the frequency domain as shown in Fig.5.12(a). At the grid side, the spectrum of the injected current must have its harmonic magnitude lower than the corresponding harmonic bar in Fig.5.12(a). At the inverter side, the converter output voltage V_{inv} is a PWM waveform and its spectrum is shown in Fig.5.12(b). The filter must attenuate this input side voltage spectrum in Fig.5.12(b) to have the output side current spectrum lower than the grid standard spectrum in Fig.5.12(a). The converter output voltage spectrum has strong harmonic components around the switching frequency and its sideband, while the grid code requires low harmonic at high frequency. This poses a stringent demand for the filter's high frequency attenuation. In the frequency domain, this requirement can be visualized as a bode plot by 5-11

$$G_{grid}(s) = \frac{I_{g\_spec}(s)}{V_{inv\_SVM}(s)} = 20\lg\frac{I_{g\_spec}(\omega)}{V_{inv\_SVM}(\omega)} \tag{5-11}$$

Table 5.1. IEEE 519 & 1547 standard for harmonic current of grid-tied converter

harmonic order	<11th	11-17th	17-23rd	23-35th	>35th	THD
Limit (%)	<4%	<2%	<1.5%	<0.6%	<0.3%	<5%



(a) Spectrum of grid standard (b) Spectrum of V_{inv} with SVM

Fig. 5.12. Spectrum of inverter output voltage & grid current standard

The red curve in Fig.5.13 shows the visualized grid code requirement on the filter output current to input voltage transfer function. It ranges from the control bandwidth below 1kHz to 5 times of the switching frequency. In this range, the filter transfer function $G_{LCL}(s)$ must be smaller than the grid code specification $G_{grid}(s)$ at each individual frequency as in 5-12 to meet the current harmonic requirement.

$$G_{LCL}(s)=\frac{I_g(s)}{V_{inv}(s)}=\frac{1}{L_1\cdot L_2\cdot C\cdot s^3+(L_1+L_2)s}<G_{grid}(s) \tag{5-12}$$

In the visualized bode plot in Fig.5.13, inequality 5-12 means that the bode plot of the filter transfer function must be lower than that of the grid code requirement. For the LCL filter transfer function, inverter side inductor L1 provides 20dB/dec attenuation at low frequency. After the resonant frequency, the inductor L1, capacitor C and grid side inductor L2 together provide a total 60dB/dec attenuation on high frequency. With L1 and C value determined, the influence of L2 inductance on high frequency attenuation can be analyzed. Fig.5.13 also gives the filter output current to input voltage transfer function with different L2 inductance. With small L2 inductance, the attenuation is insufficient at the switching frequency and its sideband. The L2 inductance should be selected to ensure enough attenuation margin at these frequencies. It can be

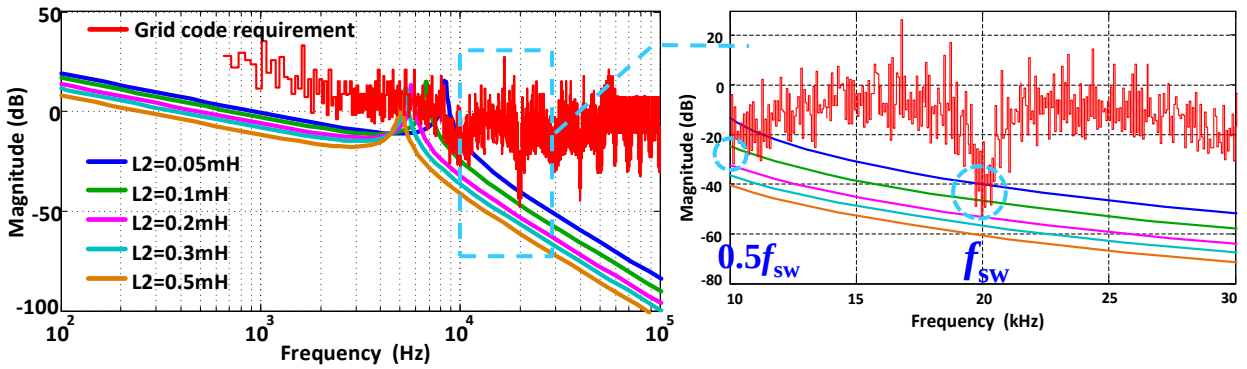


Fig. 5.13. Gird code attenuation and filter bode plot

observed in the zoomed in area at the right side of Fig.5.13, that any L2 inductance smaller than 0.2mH can not meet grid code at switching frequency or its sideband. An inductance around 0.3mH is proper. Based on this criterion, L2 is finally set to 0.27mH.

With the LCL filter parameters determined, it is necessary to check whether its resonant frequency meets the constraint introduced at the end of first part of this chapter. The resonant frequency is calculated by equation 5-13 as 5.7 kHz.

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 \cdot L_2 \cdot C}} \tag{5-13}$$

This resonant frequency is far away from the low order harmonics. Also it avoids the switching frequency and its sideband. If ω_r does not fall into this range, L2 & C can be fine-tuned to meet the constraint.

The design procedure for the LCL filter parameters is briefly restated here as a summary. First the maximum inductance and capacitance value can be calculated by equation 5-4 and 5-5 as the parameter boundary. Then the maximum inductor current ripple can be calculated by 5-6. An optimum L1 inductance value can be found to give the best ripple/loss and size/weight trade-off. Then the capacitance is determined by the maximum reactive power consumption. Finally, the L2 inductance is chosen by the grid side current attenuation requirement. With all the parameters determined, the resonant frequency can be calculated and double checked with the

design guideline. Following this procedure, the LCL filter parameters are chosen as: L1=0.1mH, C=10μF, L2=0.27mH. It is noticed that L2 is larger than L1. Generally speaking, the value for the two inductors is selected separately by the design procedures which decouples the function of the two inductors so that their value are independent. But if the core material cost is considered in real practice, L1 endures high current ripple and needs more expensive cores material like amorphous or nano-crystalline. On the contrary, L2 as a line reactor can use cheap silicon steel core. As a result, from cost point of view, although it is possible to have larger L1 and smaller L2 to achieve the same design objective, it is reasonable to make L1 smaller for cost reduction.

5.4 Damping Method for Resonant Peak

Although the filter transfer function in Fig.15 provides enough attenuation at the switching frequency, a high peak still presents in the transfer function at the LCL resonant frequency. The grid code requirement around this frequency can not be met due to the resonant peak. The LCL filter design also needs to consider the damping of this resonant peak. Typically, there are active damping and passive damping methods for the resonant peak.

5.4.1 Active Damping Method

The active damping method relies on the control loop to suppress the resonant peak. The basic principle is to emulate a damping resistor on the power stage by the control loop. For most of the grid interface converter with LCL filter, the inner control loop controls the inverter output current. The active damping control is usually added to the current loop. Fig.5.14 and Fig.5.15 show the two common active damping methods by the block diagram in frequency domain. The right part of the block diagram is the transfer function of the LCL filter power stage. It illustrates the inverter output voltage v_{inv} to grid current i_g transfer function. The left part of the diagram shows the current loop controller and modulator, which generates the v_{inv} from current reference

i_{ref} and inverter output current feedback i_{inv}. The gist of the active damping is to emulate a virtual resistor at the capacitor branch of the LCL power stage to serve as a damping resistor. The block and signal path in red color in the two figures shows the added active damping part in the control loop. The damping method 1 in Fig.5.14 senses the current i_c in capacitor branch. Then i_c is multiplied with the virtual resistance R_d to generate the voltage across the virtual resistor, which is used to compensates the voltage reference v_{ref} in the control loop. Also the voltage across the capacitor branch v_c can be sensed in active damping method 2 in Fig.5.15. The sensed v_c is divided by the virtual resistance R_d to generate current compensation term i_c. Then the calculated capacitor current i_c is subtracted from the current reference i_{ref} before it goes to the controller.

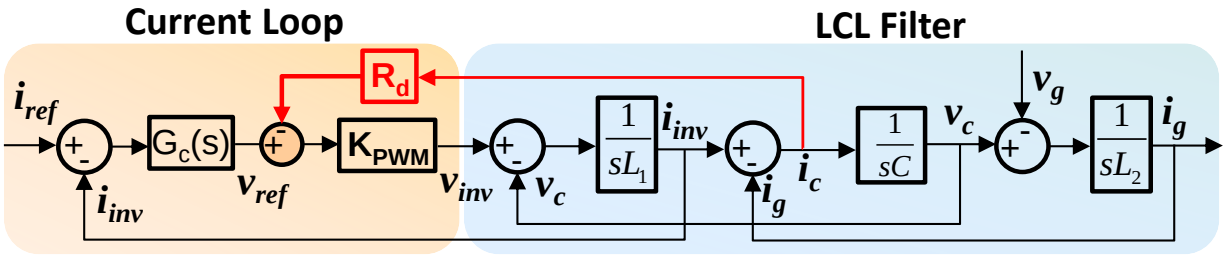


Fig. 5.14. Block diagram of active damping method 1

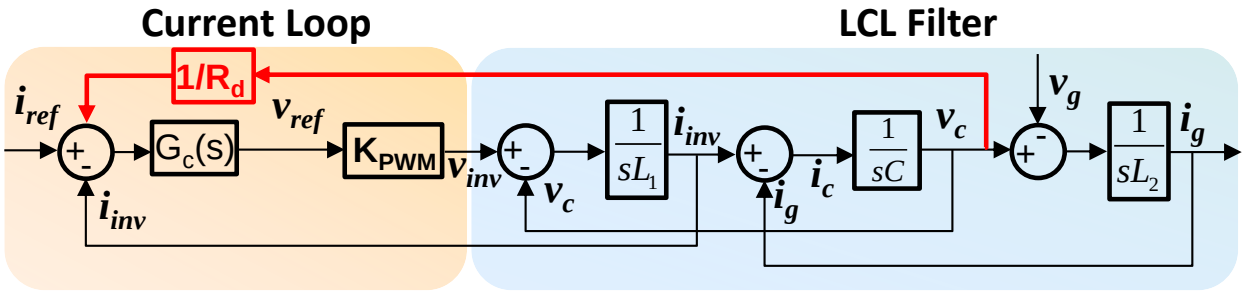
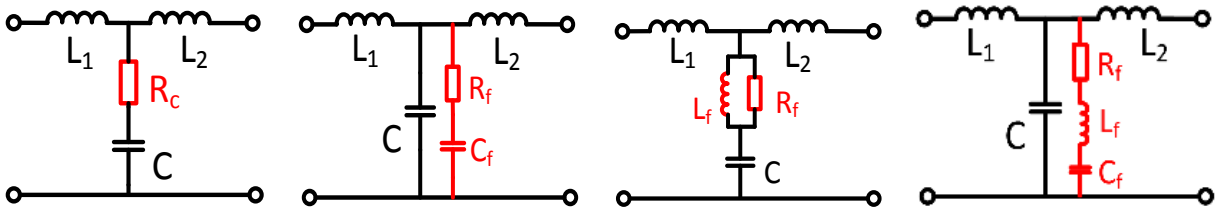


Fig. 5.15. Block diagram of active damping method 2

The active damping method does not modify the filter circuit structure and can be flexibly configured. But the damping result is largely dependent on the control loop bandwidth. It may not have desirable damping result if the resonant frequency of the LCL filter is higher than the control bandwidth. Also extra sensors are needed to get the capacitor current or voltage information for most of the active damping method.

5.4.2 Passive Damping Method

On the contrary, passive damping method adds extra damping circuit in the power stage. The resistor in the damping circuit can effectively damp the resonant peak. But it also causes extra loss on the power stage. There are several passive damping circuit topologies introduced in [11]. To avoid the high current and related loss on inductor branch, the damping circuits are typically added to the capacitor branch. Fig.5.16 gives some typical damping circuit topologies for LCL filter. The advantage and drawback of those damping circuits are discussed then.



(a) R damping (b) RC damping (c) RL damping (d) RLC damping

Fig. 5.16. Typical damping circuit topologies for LCL filter

The damping circuit in Fig.5.16(a) adds only one extra resistor on the capacitor branch and features on the simplicity of its structure. On the other hand, a large resistor is needed to damp the resonant peak which influences the high frequency attenuation. The bode plot for R damping circuit is given in Fig.5.17 compared with the same grid code requirement line in red color. It clearly shows that the small damping resistor like 0.2 or 0.5Ω can not suppress the resonant peak

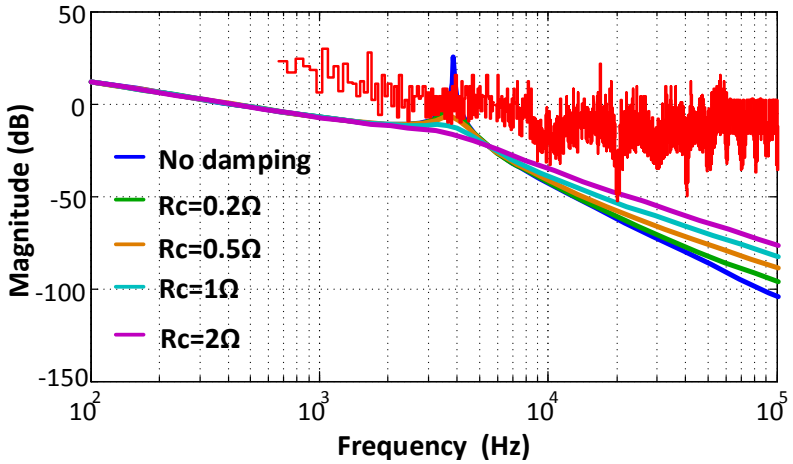


Fig. 5.17. Bode plot for R damping

below the grid code requirement. However, large damping resistor like 1 to 2Ω with damped resonant peak has poor high frequency attenuation. The bode plot at high frequency rises up as R increases. It easily touches the grid code requirement line at switching frequency. Moreover, larger resistor in C branch causes significant power loss, especially in the high power converter.

The RC damping circuit in Fig.5.16(b) adds another RC branch in parallel with the original capacitor. The bode plot for this damping circuit is shown in Fig.5.18. The major benefit for this damping circuit is that it does not sacrifice the high frequency attenuation at switching frequency. It only shifts the resonant peak to lower frequency where the grid attenuation requirement is less strict. A large resistor is still necessary with inevitable loss. But the major problem for this damping circuit lies on the added capacitor. Its capacitance is comparable with the original capacitor, which means extra reactive power consumption and drifted power factor at grid side. Also the high voltage across this capacitor results in a significantly large capacitor size.

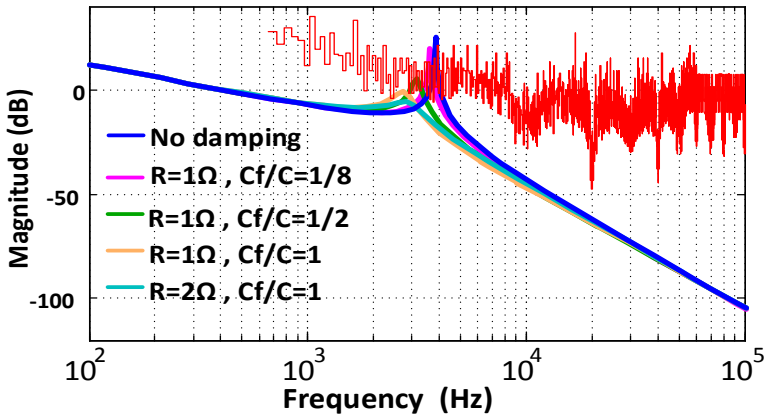


Fig. 5.18. Bode plot for RC damping

Another variation of the damping circuit is the RL damping in Fig.5.16(c). It adds a paralleled RL circuit in serial with the capacitor. The resistor still provides damping at the resonant frequency while the added inductor and capacitor provides low impedance path at other frequencies to lower the power loss on the resistor. The resistance can be small and the loss on resistor is also reduced compared with the R damping and RC damping. Nevertheless, the bode

plot in Fig.5.19 shows a damped resonant peak with sacrificed high frequency attenuation. This topology also loses some attenuation margin at the switching frequency.

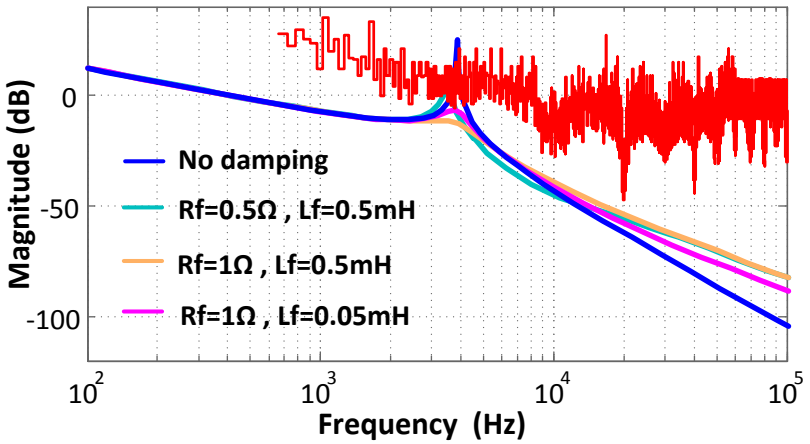


Fig. 5.19. Bode plot for RL damping

The damping circuit shown in Fig.5.16(d) contains an extra inductor L_d and capacitor C_d besides the damping resistor. The damping resistor provides enough damping at resonant frequency while the L_d and C_d provides a resonant notch to reduce the power loss on the damping circuit. Fig.5.20 shows that the damping circuit effectively suppress the resonant peak and the transfer function is below the grid code requirement at the whole frequency range. The high frequency attenuation keeps the same with the damping circuit added, which means no attenuation margin is sacrificed near the switching frequency. Additionally, this damping circuit

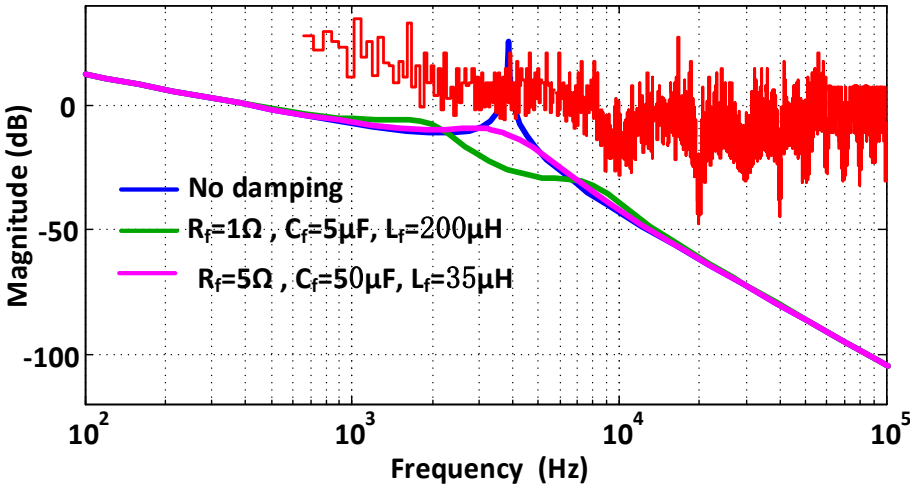


Fig. 5.20. Bode plot for RLC damping

provides a better open loop transfer function for the compensator design. Fig.5.21 shows the open loop bode plot from the d channel duty cycle D_d to the d channel output current i_{L1d} with and without the damping circuit. It clearly shows that the resonant notch of the damping circuit reshapes the open loop gain at around 5.7 kHz of the LCL resonant frequency. With the reduced resonant peak, the control loop design is easier and the bandwidth of the current control loop can be pushed higher. The detailed controller design will be covered in Chapter.6.

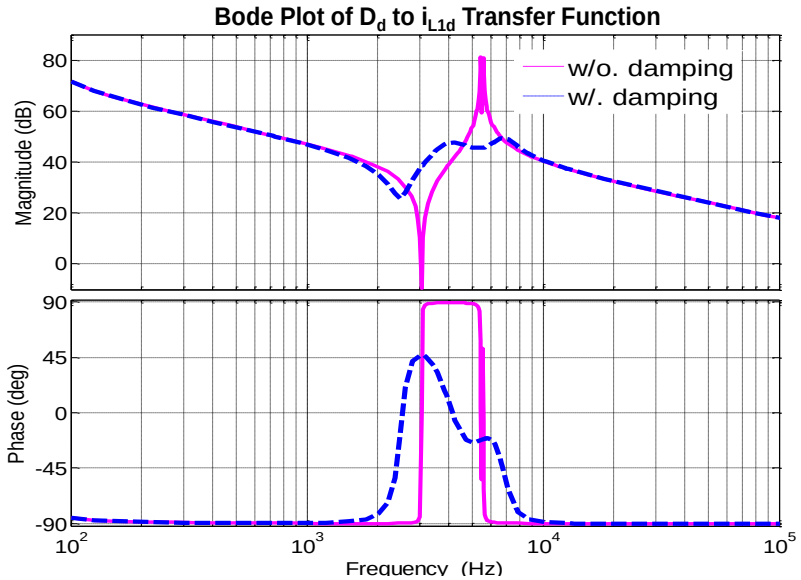
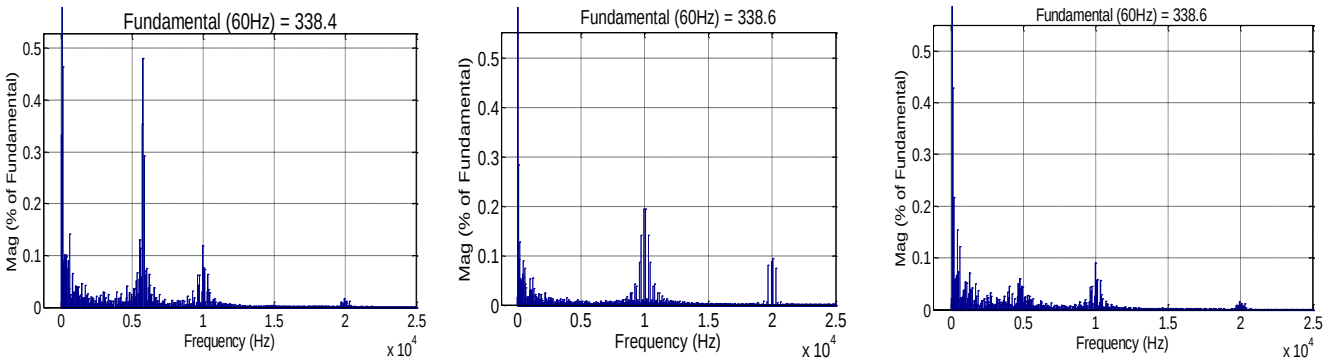


Fig. 5.21. Bode plot for the d-channel duty cycle to current transfer function

To compare these 4 damping circuit topologies, the power loss, high frequency attenuation and size are evaluated. From loss point of view, R damping and RC damping cause too much extra loss on the resistor. In terms of attenuation, the R damping and RL damping sacrifice some high frequency attenuation. For the circuit size consideration, extra capacitor in the damping circuit is disadvantageous for size. The damping capacitors are added in parallel with the original one. The voltage across them are almost grid voltage, which gives a large capacitor size. On the contrary, the added inductor has relatively small current rating and does not take too much space. For the 4 damping circuits, the RC damping and RLC damping have extra capacitors. The size for the added capacitor is comparable with the filter capacitor considering they have basically the

same capacitance. But for the overall performance, the RLC damping is used because of the good damping performance and low loss. The RLC damping circuit parameters is determined by the green line in Fig.5.20 as: R=5Ω, C=4μF, L=200μH. These parameters provide good damping result at resonant frequency as well as smallest loss and component size.

The damping result for the designed RLC damping circuit is then compared with the R damping by the simulated grid current spectrum in Fig.5.22. The non-damped grid current in Fig.5.22(a) has strong harmonic component around 5.7kHz which is the resonant frequency. For the R damping circuit, the resonant peak is eliminated as shown in Fig.5.21(b). But the switching frequency and its sideband rise up and exceed the grid code. For the RLC damping circuit, it effectively eliminates the resonant frequency component while keeps the switching frequency component low as shown in Fig.5.22(c). The result verifies the performance for RLC circuit. The power loss on the RLC circuit is also verified in Fig.5.23. The instantaneous and RSM power on the resistor is far less than the power stage device loss. The 20W loss for the damping circuit takes only 0.01% power of the 200kVA converter. Also the current in the damping circuit is trivial, which means small component size for the damping circuit. In summary, the designed RLC damping circuit has good damping result at resonant frequency while keeps the same high frequency attenuation. The damping resistor does not cause too much loss either.



(a) Without damping (b) R damping (c) RLC damping

Fig. 5.22. Grid current spectrum with different damping circuits

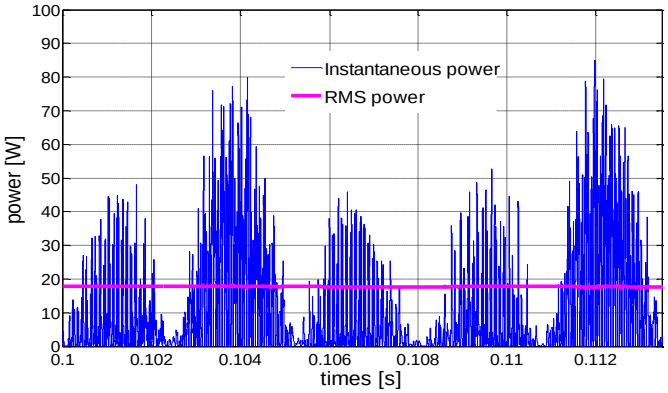


Fig. 5.23. Power loss on RLC damping circuit

5.5 Filter Components Design and Experiment Result

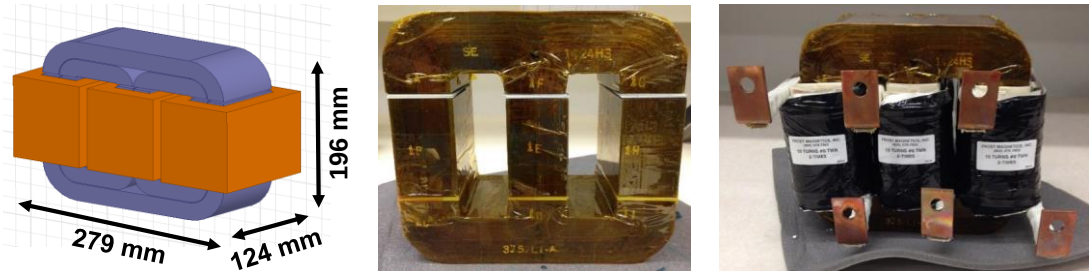
Finally, the components for the LCL filter and damping circuit are fabricated. Also the power conversion system is built based on the components and the phase leg building block. The filter design is verified by the 200kVA 3-level NPC grid interface converter hardware. The system rating is listed in Table.5.2 with the designed parameters for LCL and damping circuit.

Table 5.2. Parameters and ratings for 3-level NPC converter

S_N	f_{sw}	V_{grid}	V_{dc}	L1	L2	C	L_d	C_d	R_d
200kVA	20kHz	480V	1200V	0.1mH	0.27mH	10μF	0.2mH	4μF	5Ω

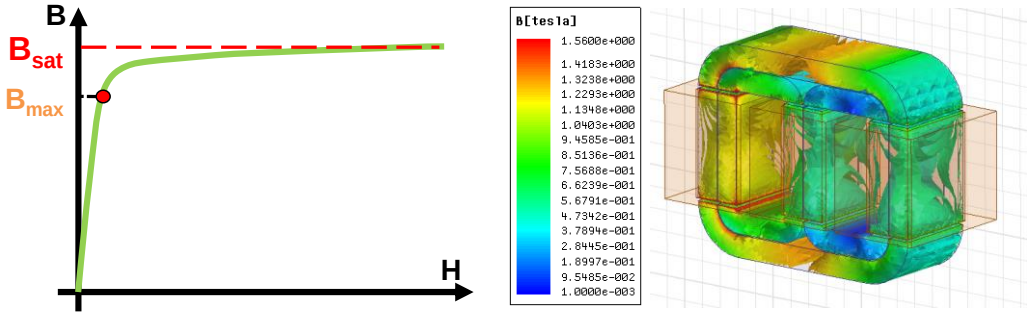
The inverter side inductor L1 is a 3-phase coupled inductor with amorphous core to reduce the core loss. The structure and physical layout of this 3-phase coupled inductor is shown in Fig.5.24. The specific amorphous material is Metglas 2605SA1. The core material selection considers both the core loss density and the flux density for the high current and high ripple in the inductor. The maximum flux in the core is also designed to avoid saturation at high current. The saturation flux for the core is 1.56T and the maximum flux in the core is designed to be 3/4 of the saturation flux as shown in Fig.5.25(a). The flux distribution in the core at full current (240A rms) is also simulated by FEA software as shown in Fig.5.25(b). It verifies the designed flux in the core. The grid side inductor L2 is also a 3-phase coupled inductor with silicon steel

core. The grid side inductor doesn't have high current ripple, therefor the core loss is not an issue.



(a) 3-D dimension (b) Core shape (c) fabricated inductor

Fig. 5.24. Dimension and physical layout for inductor L1



(a) Maximum flux design for saturation (b) FEA analysis for flux distribution

Fig. 5.25. Max. flux and flux distribution in the core

So the silicon steel core material with high flux density and low cost is selected. More detail information of the filter power stage and the DC/AC converter system will be covered in Chapter 8 when the system hardware structure is introduced.

The filter performance is verified by the experiment. The power converter system is connected to the 480V AC source that emulates the grid. The DC side is connected to either a resistive load bank for rectifier mode or a DC source for inverter mode. The AC source can generate and take power at full power rating so the converter can work at both inverter and rectifier mode with bidirectional power flow. The test setup for different mode is shown in Fig.5.26. The experimental waveform at unity power factor with rectifier mode is shown in Fig.5.27. The inverter side current in L1 and grid side current in L2 is shown in Fig.5.27(a) and

Fig.5.27(b) respectively. The grid voltage is also given in the waveform. The large current ripple in the inverter current is filtered by the LCL circuit and also the damping circuit. In the grid current waveform, neither the switching frequency nor the resonant frequency component can be observed. The inverter mode with non-unity power factor are also tested. Fig.5.28(a) and (b) shows the same current waveform with 0.6 power factor at inverter mode. The grid voltage is not in phase with the current anymore, but the current waveform keeps the same. This experimental result verifies the filter performance at different operating conditions and power factor cases.

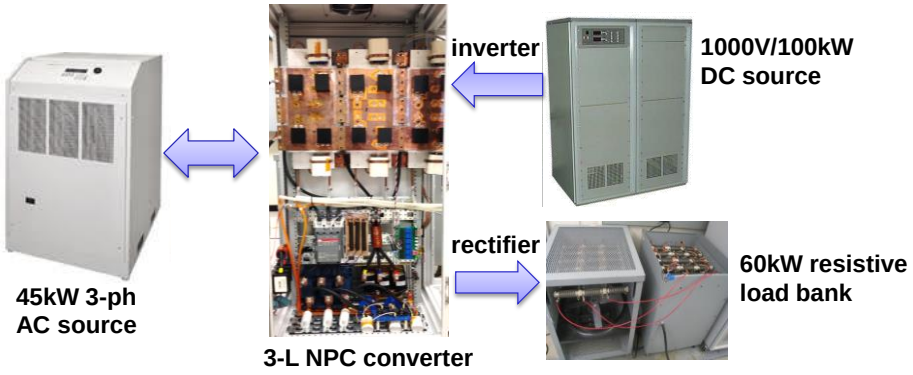
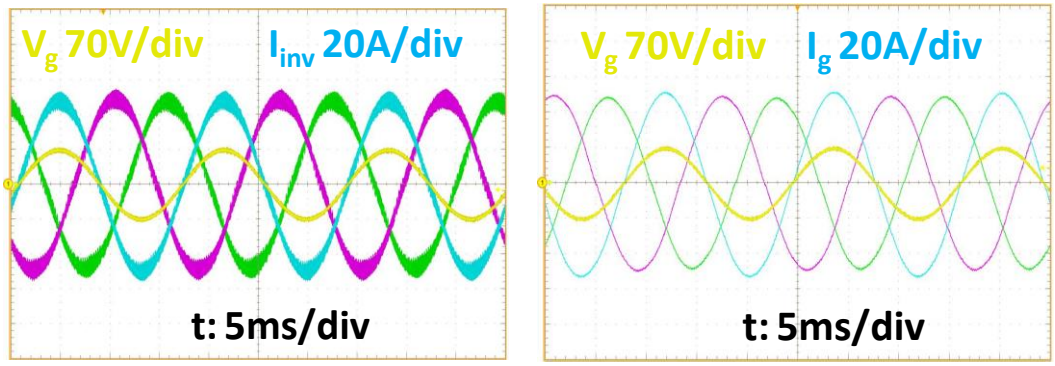
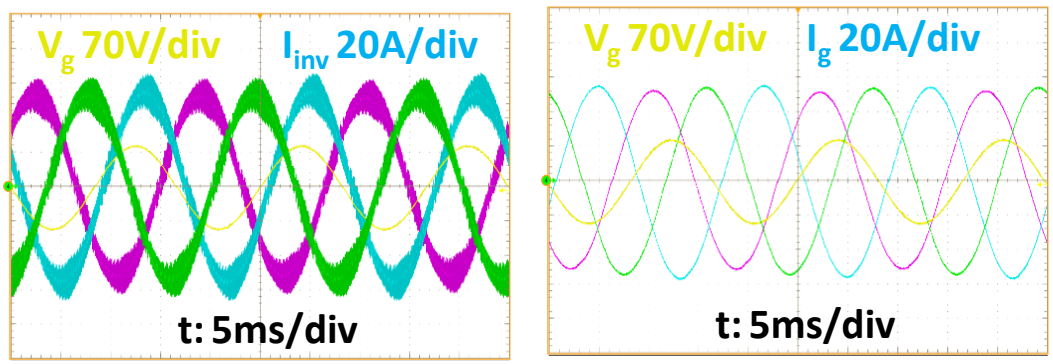


Fig. 5.26. Test setup for bidirectional operation of the 3-level NPC converter



(a) Inverter output current (b) Grid current

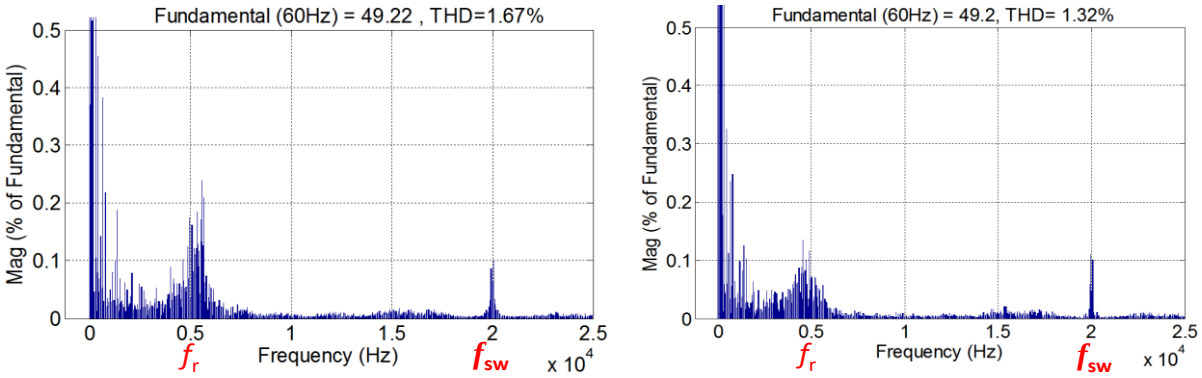
Fig. 5.27. Inverter and grid current at rectifier mode with unity power factor



(a) Inverter output current (b) Grid current

Fig. 5.28. Inverter and grid current at rectifier mode with 0.6 power factor

The grid current is also analyzed in frequency domain and its spectrum is shown in Fig.5.29. The damping result is also tested by adding and removing the damping circuit branch in the filter. Without the damping circuit, although the switching frequency component is attenuated as shown in Fig.5.29(a), the resonant frequency component still exist. If damping circuit is added, then the resonant frequency component is suppressed as in Fig.5.29(b). Fig.5.29 also shows the THD is reduced from 1.67% without damping to 1.32% with damping. The experimental result shows that the designed LCL filter and its damping circuit achieves the desired attenuation at resonant frequency and switching frequency. The current injected to the grid meets all the grid standard requirement and the total loss and size of the filter is minimized.



(a) Spectrum without damping (b) Spectrum with damping

Fig. 5.29. Grid current spectrum with and without damping

5.6 Summary and Conclusion

This chapter introduces the design procedures for the LCL filter of the 3-level NPC grid interface converter. The design emphasizes the inductor current ripple analysis and the high frequency attenuation. The equivalent circuit for the LCL filter is derived for detailed ripple analysis. The switching cycle volt-second on the inductor is quantified. The maximum current ripple case in the line cycle is identified by both the analytical expression and the simulation calculation. The maximum ripple estimation provides the switching cycle current ripple data in the whole line cycle. The influence of power factor on current ripple is considered. The result shows that power factor influences the current stress and furthermore influences the inductor saturation current. The system total loss is quantified with different ripple cases. The inverter side inductance L1 is determined by the loss/ripple and size/cost tradeoff. The grid side inductor L2 is designed to meet the grid code requirement. The L2 inductance is selected based on the high frequency attenuation. The damping circuit for LCL filter is investigated to solve the issue of resonant frequency peak. Several different damping circuits are compared with their advantage and drawback discussed. Finally the RLC damping with good damping result and low loss is chosen. The designed parameters for the filter is verified by both simulation and experimental result on the 200kVA 3-level NPC converter hardware. The grid and inverter current in time domain and frequency domain verifies the filter performance.

The research contributions in this chapter is concluded in the following:

1. Derived the analytical expression for the maximum inductor current ripple in line cycle
2. Analyzed the inductor current ripple and maximum current distribution in the line cycle with different power factor cases
3. Quantified the total system loss with inductor L1 and maximum current ripple ΔI_{max}.

4. Optimized the filter inductor value based on size and loss trade-off
5. Quantified the grid code attenuation based on the inverter output voltage and grid current harmonic requirement. Generalized the inductor L2 design method based on the grid code attenuation requirement.
6. Evaluated different passive damping circuit topologies and compared them in terms of loss, size and damping performance

CHAPTER.6 MODELING AND CONTROL FOR THE 3-LEVEL NPC DC/AC CONVERTER

With phase leg building block design introduced in Chapter.2 and the grid interface filter design finished in Chapter.5, the power stage of the DC/AC part of the power conversion system is completed. Also the modulation strategy and scheme for the 3-level NPC converter is explored in Chapter.3 and 4. With the power stage done and the modulation strategy determined, the next step is to connect the DC/AC part to the grid with closed-loop control. To design the control loop with good performance, a detailed model for the power stage for DC/AC part with LCL filter and damping circuit should be built. The control loop design is based on the modeling of the power stage. The design of the control bandwidth and phase margin is influenced by the accuracy of the converter model. In this chapter, different control algorithms for the grid-tie converter in micro-grid application is first explored. Then the state-space equations for the converter in ABC and d-q coordinates is derived with the consideration of filter and damping circuit. The equivalent circuit for the average model in ABC and d-q coordinates is also built. The grid side and DC side impedance of the converter is derived by the model. The accuracy of the converter modeling is verified by the small signal loop gain measurement on the real converter hardware. The AC current and DC voltage control are designed and verified by both simulation and experiment.

6.1 Control Strategies Survey of Grid Interface Converter in Micro-grid

The control strategies for a grid-tied converter has been well established by numerous literatures in the past. The application for the grid-tied converter basically focus on distributed generation (DG) system with renewable energy or energy storage. In most of the conventional scenarios, the distributed generation system has limited power capacity compared to the vast-

scale utility grid. Also there are limited number of DG system compared with the large number of synchronous generators in the power grid. The stochastic and unpredictable characteristic of the renewable energy makes it uncontrollable by grid dispatchers. Under this circumstances, the utility grid dominates the bus voltage at the point of common coupling (PCC) for the DG. The grid interface converter for DG just follows the voltage regulated by the grid and injects its maximum power to the grid. When the DG system has insufficient capacity and low penetration in the grid, it just works as a current source that delivers the maximum power to the grid. Under islanding mode, the DG system must be shut down and disconnected from the grid. This is mandatory for DG system enforced by old IEEE standard 519 and 1547.

Nowadays, with the higher penetration of DG system in the utility grid and the increased power rating for the renewable energy and storage system, the infrastructure of the utility grid is gradually shifting [1]-[3]. More and more micro-grid with DG systems and local loads appear in the conventional utility grid as Fig.6.1 shows. This figure demonstrates the DC and AC micro-grid system with renewable energy and energy storage. The DC micro-grid system in the center part distributes power in DC voltage and current. The DC distribution system interfaces with the AC grid with directional power flow via a micro energy control center (μECC). The right part in Fig.6.1 shows the AC micro-grid system that contains various DG systems, numerous local loads and some synchronous generators in the vicinity of the loads and sources. The left part is the conventional utility grid that is connected to the AC micro-grid system by transmission line. In such a micro-grid system, there are plenty of grid-tied converters with bidirectional power flow for DG system. The total power rating for the DG system is comparable to the installation capacity of the synchronous generator in the local area. Therefore, the DG systems in the micro-grid are able to regulate the local bus voltage when connected to the grid. Additionally, they are

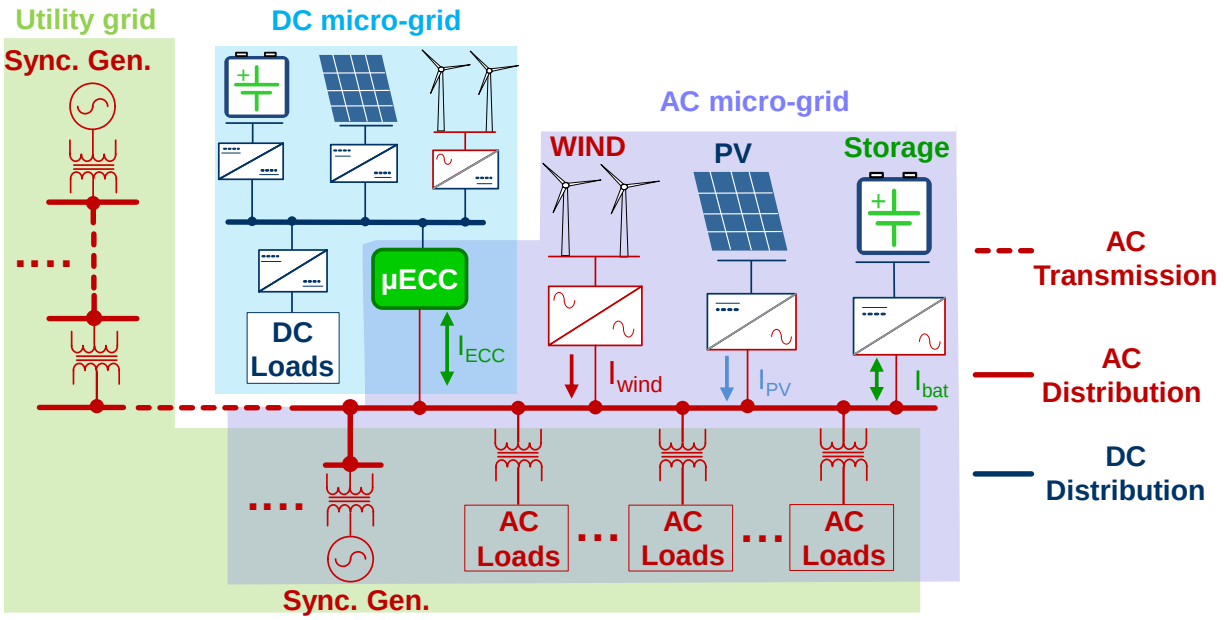


Fig. 6.1. Power grid infrastructure with renewable energy micro-grid.

also able to support the local loads when the grid is disconnected at islanding mode. Recently, the IEEE 1547 standard is modified to allow the islanding operation for the DG system, so that it can support the load. In addition, more and more research has been concentrated on the converter control in the micro-grid system or control the converter as a synchronous generator [4]-[12].

There are two major objectives to investigate the control design for grid interface converter. First one is to find a better control algorithm for grid interface converter in the micro-grid system. The grid interface converters in the micro-grid should be able to regulate the bus voltage and frequency together with the synchronous generator without fighting with each other [4], [5]. Moreover, several converters should share the local loads together at both grid-connected mode and islanding operation mode [6]. They should also be able to seamlessly synchronize with the local generator [7]. To achieve these control objective, the converter is controlled to emulate the function of a synchronous generator [8]-[10]. The converter with this control is called as virtual synchronous machine or synchronous converter in some literatures. The other objective of the converter control is to provide grid support capability like reactive power compensation,

dynamic voltage recovery or oscillation damping [11]-[13]. The converter has faster transient response than the synchronous generator. As a result, the converter with proper control can assist the power grid in a better way than the synchronous generator does under grid fault conditions.

The control strategies of the grid interface converter are generalized and classified into 4 major categories in [4]. The grid forming control in Fig.6.2 controls the converter as a voltage source by regulating the output voltage amplitude and frequency. The voltage and frequency reference is provided to the outer loop voltage controller in Fig.6.2 and it generates the current reference for the inner loop current controller. The controller can be implemented in either stationary ABC frame or synchronous rotating d-q frame. With this control scheme, the converter works as the AC source. It can be also used to supply the local loads at stand-alone mode without utility grid or work as major voltage source in a micro-grid system.

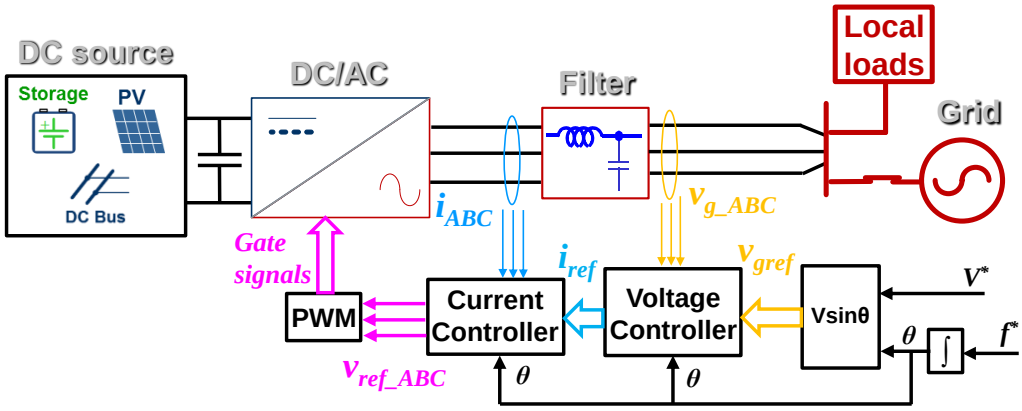


Fig. 6.2. Grid forming control for grid-tied converter

The grid feeding control in Fig.6.3 regulates the output active and reactive power by controlling the converter output current. This control method follows the grid voltage by a phase locked loop (PLL) and controls the converter as a current source that injects designated power to the grid. The current is usually controlled in d-q frame to regulate the output active and reactive power. This converter can only work in grid connected mode with the presence of large scale

utility grid or grid forming converters in micro-grid system. Usually the PV converter is controlled in this form with the maximum power injected to the grid.

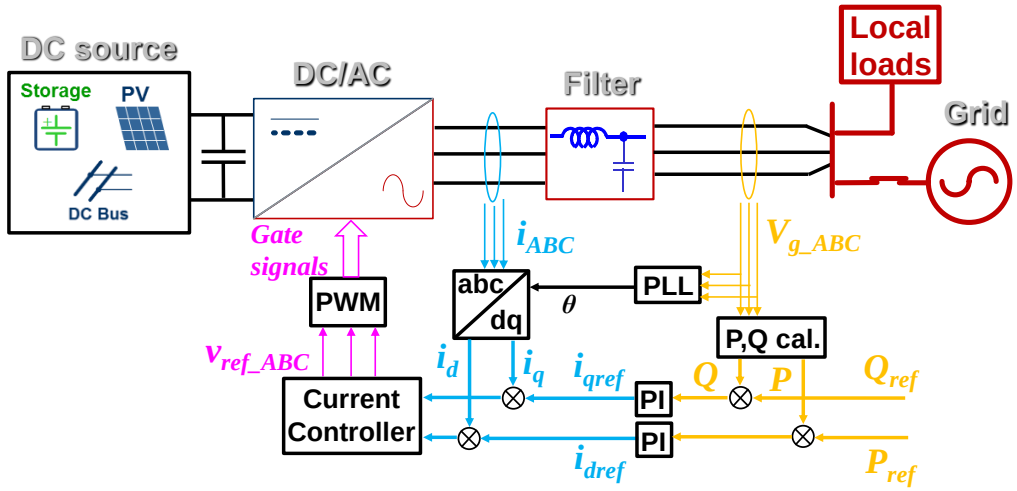


Fig. 6.3. Grid feeding control for grid-tied converter

The third and fourth categories of the converter control in micro-grid system are called grid supporting control. These two types of control regulates the output voltage amplitude and frequency, as well as controls the output active and reactive power. This control objective is achieved by the droop mode control. In most of the micro-grid system, the grid voltage amplitude is closely connected with the reactive power. The grid frequency is strongly coupled with the active power. The grid supporting control implements the voltage and frequency regulation by controlling the output active and reactive power from the outer control loop. With different inner loop control, there are current based grid supporting control in Fig.6.4 and voltage based grid supporting control in Fig.6.5. For the current based grid supporting control, the outer loop droop mode control provides the active and reactive power reference to the inner loop current controller. The converter is controlled as a current source that delivers designated active and reactive current to the grid so that the bus voltage amplitude and frequency can be regulated by the droop control. On the other hand, the outer control loop for the voltage based grid supporting control provides frequency and amplitude reference of the bus voltage to the inner

loop voltage controller. This voltage reference is generated by the droop control for active and reactive power regulation. The inner loop for the voltage based grid supporting control is the voltage controller. These two types of grid supporting control enables the converter to work in a micro-grid system without a large scale of utility grid. In other word, these two control schemes can work at stand-alone mode to independently support the local loads

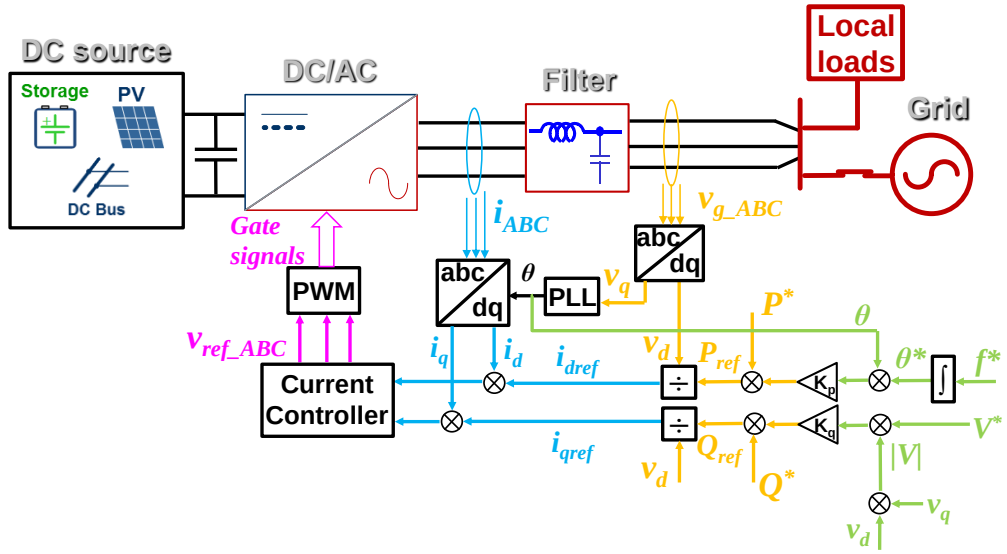


Fig. 6.4. Current source based grid supporting control for grid-tied converter

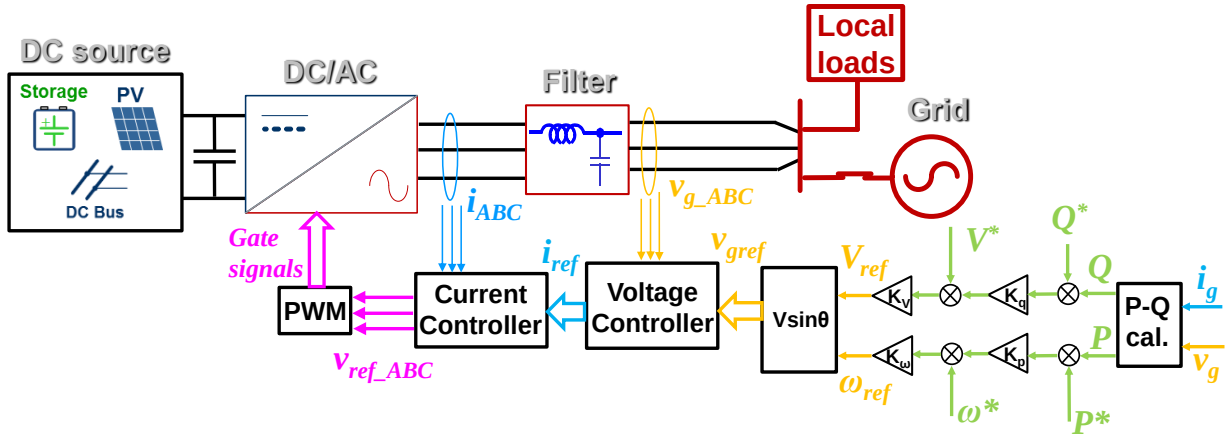


Fig. 6.5. Voltage source based grid supporting control for grid-tied converter

It can be observed from the above control strategy survey that the current control for the grid interface converter is an essential part in the system level control strategy. So the inner loop of the 3-level power conversion system is designed to be a current controller so that it can work

with all the aforementioned system level control strategies. It should also be mentioned that the grid forming control needs sufficient and constant power capacity from DC side to regulate the AC bus voltage. However, the 3-level PCS is designed as a general purpose grid interface converter for different applications like PV farm, energy storage system or DC bus. Since the DC side of the PCS can be flexibly configured, the DC/AC stage is controlled as the grid feeding converter at first. This control scheme can be easily upgraded to the current based grid supporting control by adding the outer loop with droop mode control. With this control scheme, the PCS can work in both conventional utility grid and micro-grid system.

The system level control strategy for the 3-level PCS is demonstrated in Fig.6.6. The control block diagram for both the DC/AC part and the DC/DC part is shown in this figure. For the DC/AC part, the inner loop is current controller in d-q frame with proportional integration (PI) controller. The output of the current loop is the duty cycle reference in d-q frame. The duty cycle is send to the SVM modulation block for NP balance and loss reduction that is introduced in chapter 3 and 4. The SVM needs DC link voltage and output current feedback to achieve switching cycle NP balance. The input of the current loop is the active and reactive current reference in d-q frame I_{dref} and I_{qref}. The d channel active current reference is provided by the outer loop, which is the DC link voltage controller. The outer loop controls the active power to achieve a power balance at AC and DC side. Therefore the DC link voltage can be regulated. As for the reactive current reference, it can be used for different purposes. For conventional grid interface converter control, the reactive power can be used to achieve islanding detection by injecting some reactive power perturbation. For the power converter in the micro-grid system, the reactive current reference can be provided by the outer loop droop control for bus voltage regulation. The DC/DC converter controls its current and voltage so that the operating point at

the DC bus side can be regulated. The inner loop is the current loop and the outer loop is the voltage loop. The DC/DC converter achieves different control objectives in various applications. For the PV system, the DC/DC converter controls the operating point for the maximum power point tracking (MPPT) control. For the energy storage system, the converter is used for charge/discharge control and battery management. If the DC side is connected to a DC bus or load, the converter is responsible for the DC bus voltage regulation.

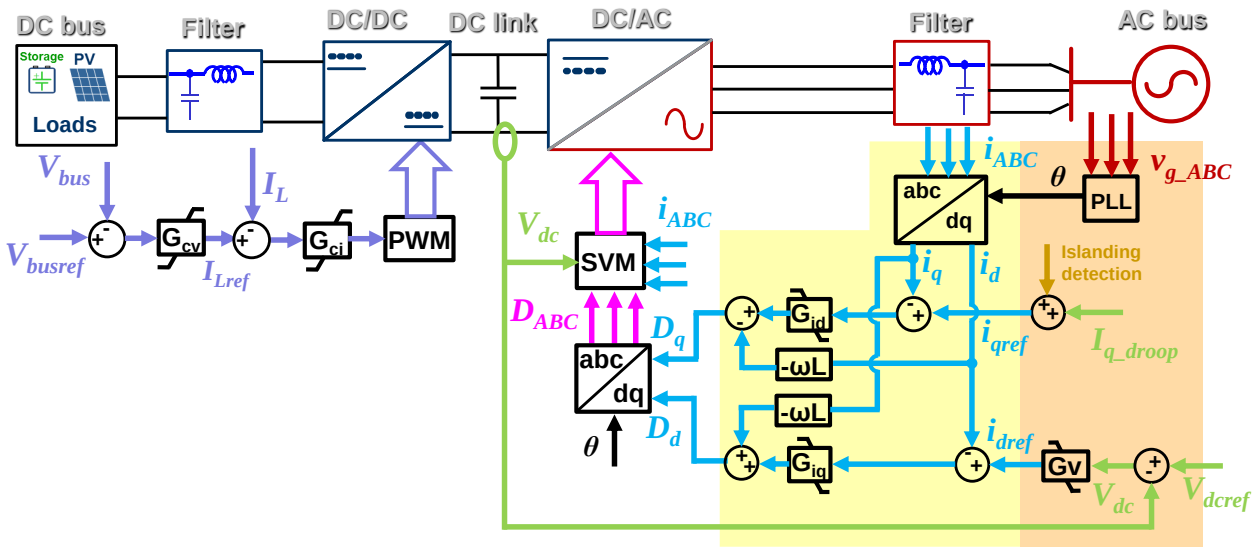


Fig. 6.6. System control strategy diagram for the power conversion system

6.2 Average Model for the 3-L NPC DC/AC Converter

In order to design the control loop for the 3-L NPC converter, the average model of the converter should be derived at first. The average model provides the converter control to output transfer function and bode plot, with which the control loop phase margin and bandwidth can be designed and determined. The converter can be controlled in either stationary ABC frame or synchronous rotating d-q frame. The derivation of the model in d-q frame relies on the model in ABC frame. As a result, the following sessions introduce the 3-L NPC converter average model in both ABC and d-q frame. The model is based on the specific LCL filter and damping circuit design that is introduced in Chapter 5.

6.2.1 Average Model in Stationary ABC Frame

The average model for the converter in ABC coordinates is first derived with the switching function for each phase leg defined. Each phase leg equals to a 1-pole 3-throw switch that can be connected to P, O and N as shown in Fig.6.7. The switching function for phase A can be then defined as follow:

$$\begin{cases} S_{AP}=1, \text{ A to P} \\ S_{AP}=0, \text{ else} \end{cases}, \quad \begin{cases} S_{AO}=1, \text{ A to O} \\ S_{AO}=0, \text{ else} \end{cases}, \quad \begin{cases} S_{AN}=1, \text{ A to N} \\ S_{AN}=0, \text{ else} \end{cases} \tag{6-1}$$

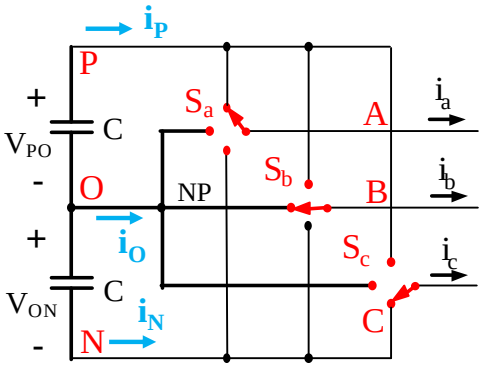


Fig. 6.7. Equivalent circuit for 3-phase 3-level NPC converter

For the 3-phase system, the switching function can be generalized as:

$$S_{ij}=\begin{cases} 1, \text{ (i connected to j)} \\ 0, else \end{cases}, \quad i\in\{A,B,C\}, j\in\{P,O,N\} \tag{6-2}$$

For each phase leg, the output can be connected to single DC rail, as the following rule defined

$$\sum_{\substack{i\in\{A,B,C\} \\ j=P,O,N}} S_{ij}=1 \tag{6-3}$$

Then the AC side voltage can be derived as the function of DC side voltage in 6-4. The DC side current can also be derived as a function of AC side current in 6-5.

$$\begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix}=\begin{bmatrix} S_{AP} & -S_{AN} \\ S_{BP} & -S_{BN} \\ S_{CP} & -S_{CN} \end{bmatrix}\cdot\begin{bmatrix} v_{PO} \\ v_{ON} \end{bmatrix} \tag{6-4}$$

$$\begin{bmatrix} i_P \\ i_O \\ i_N \end{bmatrix}=\begin{bmatrix} S_{AP} & S_{BP} & S_{CP} \\ S_{AO} & S_{BO} & S_{CO} \\ S_{AN} & S_{BN} & S_{CN} \end{bmatrix}\cdot\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{6-5}$$

By applying the switching cycle average in 6-6 to the switching function, the duty cycle for each phase leg and switching states can be derived in 6-7 and 6-8

$$D_{ij} = \frac{1}{T_{sw}} \int_0^{T_{sw}} S_{ij}(t)dt \tag{6-6}$$

$$\bar{v}_{ABC} = \begin{bmatrix} D_{AP} & -D_{AN} \\ D_{BP} & -D_{BN} \\ D_{CP} & -D_{CN} \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{PO} \\ \bar{v}_{ON} \end{bmatrix} \tag{6-7}$$

$$\bar{i}_{PON} = \begin{bmatrix} D_{AP} & D_{BP} & D_{CP} \\ D_{AO} & D_{BO} & D_{CO} \\ D_{AN} & D_{BN} & D_{CN} \end{bmatrix} \cdot \bar{i}_{abc} \tag{6-8}$$

The average voltage and current for the converter output is used to derive the full model with filter and damping circuit. The power stage circuit diagram for the DC/AC part of the power conversion system is drawn in Fig.6.8. The reference direction for the voltage and current is labeled in the figure. Also the ESR for the inductors and capacitors are considered for accurate model derivation. Then the circuit differential equations on the filter inductors and capacitors can be listed based on KVL and KCL. By defining the state variables as the current in all the inductors and voltage on all the capacitors, the state-space equations for the DC/AC converter can be listed in 6-9. There are 17 state variables in total. Each phase has 5 passive components so

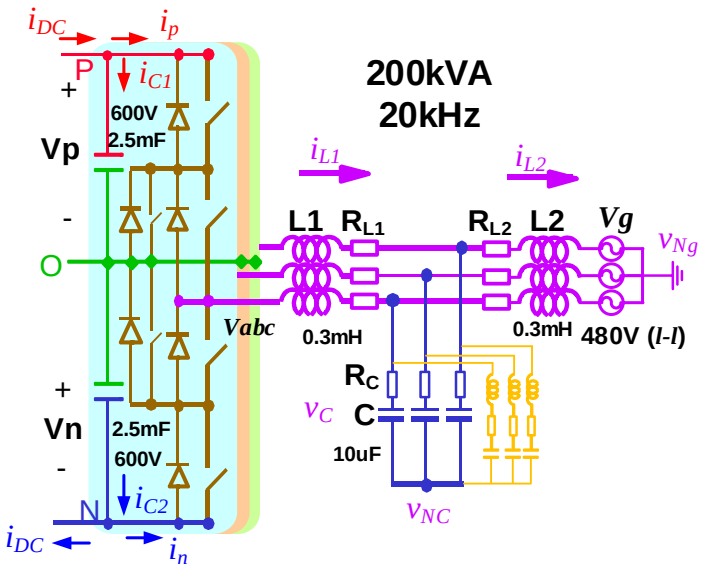


Fig. 6.8. Circuit diagram and reference direction of the DC/AC converter

$$
\begin{aligned}
\frac{d\bar{\bar{i}}_{L1abc}}{dt} &= -\frac{R_{L1}+R_c}{L_1}\bar{\bar{i}}_{L1abc} + \frac{R_c}{L_1}\bar{\bar{i}}_{L2abc} - \frac{1}{3L_1}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\bar{\bar{v}}_{Cabc} + \frac{R_c}{L_1}\bar{\bar{i}}_{Lrabc} + \frac{1}{3L_1}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} D_{ap} & D_{an} \\ D_{bp} & D_{bn} \\ D_{cp} & D_{cn} \end{bmatrix}\cdot\begin{bmatrix} \bar{v}_p \\ -\bar{v}_n \end{bmatrix} \\
\frac{d\bar{\bar{i}}_{L2abc}}{dt} &= \frac{R_c}{L_2}\bar{\bar{i}}_{L1abc} - \frac{R_{L2}+R_c}{L_2}\bar{\bar{i}}_{L2abc} + \frac{1}{3L_2}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\bar{\bar{v}}_{Cabc} - \frac{R_c}{L_2}\bar{\bar{i}}_{Lrabc} - \frac{1}{L_2}\bar{\bar{v}}_{gabc} \\
\frac{d\bar{\bar{v}}_{Cabc}}{dt} &= \frac{1}{C}\bar{\bar{i}}_{L1abc} - \frac{1}{C}\bar{\bar{i}}_{L2abc} - \frac{1}{C}\bar{\bar{i}}_{Lrabc} \\
\frac{d\bar{\bar{i}}_{Lrabc}}{dt} &= \frac{R_c}{L_r}\bar{\bar{i}}_{L1abc} - \frac{R_c}{L_r}\bar{\bar{i}}_{L2abc} + \frac{1}{L_r}\bar{\bar{v}}_{Cabc} - \frac{R_c+R_r}{L_r}\bar{\bar{i}}_{Lrabc} - \frac{1}{L_r}\bar{\bar{v}}_{Crabc} \\
\frac{d\bar{\bar{v}}_{Crabc}}{dt} &= \frac{1}{C_r}\bar{\bar{i}}_{Lrabc} \\
\frac{d}{dt}\begin{bmatrix} \bar{v}_{po} \\ \bar{v}_{on} \end{bmatrix} &= \frac{1}{C_{bus}}\begin{bmatrix} -D_{ap} & -D_{bp} & -D_{cp} \\ D_{an} & D_{bn} & D_{cn} \end{bmatrix}\begin{bmatrix} \bar{i}_{L1a} \\ \bar{i}_{L1b} \\ \bar{i}_{L1c} \end{bmatrix} + \frac{\bar{i}_{dc}}{C_{bus}}
\end{aligned}
\tag{6-9}
$$

the AC side has 15 variables. There are also two DC link capacitors with 2 variables at DC side. The 15 state-space equations are corresponding to 15 state variables. The average model in ABC coordinates for the 3-level converter can be built based on these equations. At AC side of the converter, the output voltage are replaced by a controlled voltage source that is controlled by the duty cycles of P, O and N for the three phases. At DC side, there are three controlled current sources that represent the three DC rails current. The current sources charge and discharge the DC link capacitors and influence the NP voltage. Limited by space, the equivalent circuit diagram for the average model in ABC frame is not given here.

6.2.2 Average Model in Synchronous Rotating d-q Frame

By applying the d-q to ABC transformation on 6-9, the average model in d-q coordinates can be derived in 6-10. It gives the state-space differential equations for the state variables in d-q coordinates. There are 10 state variables for AC side in d-q coordinates and still 2 variables at DC side. With a balanced 3-phase system, the zero sequence component is ignored in the state-space equation. The coupling terms between d channel and q channel should be noticed in the equation. Based on the state-space equations, the equivalent circuit for the average model in d-q

$$\frac{d}{dt}\begin{bmatrix}\bar{i}_{L1d}\\ \bar{i}_{L1q}\\ \bar{i}_{L2d}\\ \bar{i}_{L2q}\\ \bar{v}_{cd}\\ \bar{v}_{cq}\\ \bar{i}_{Lrd}\\ \bar{i}_{Lrq}\\ \bar{v}_{crd}\\ \bar{v}_{crq}\\ \bar{v}_{po}\\ \bar{v}_{on}\end{bmatrix}=\begin{bmatrix}
-\frac{R_{L1}+R_c}{L_1} & \omega & \frac{R_c}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{R_c}{L_1} & 0 & 0 & 0 & \frac{D_{dp}}{L_1} & -\frac{D_{dn}}{L_1}\\
-\omega & -\frac{R_{L1}+R_c}{L_1} & 0 & \frac{R_c}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{R_c}{L_1} & 0 & 0 & \frac{D_{qp}}{L_1} & -\frac{D_{qn}}{L_1}\\
\frac{R_c}{L_2} & 0 & -\frac{R_{L2}+R_c}{L_2} & \omega & \frac{1}{L_2} & 0 & -\frac{R_c}{L_2} & 0 & 0 & 0 & 0 & 0\\
0 & \frac{R_c}{L_2} & -\omega & -\frac{R_{L2}+R_c}{L_2} & 0 & \frac{1}{L_2} & 0 & -\frac{R_c}{L_2} & 0 & 0 & 0 & 0\\
\frac{1}{C} & 0 & -\frac{1}{C} & 0 & 0 & \omega & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0\\
0 & \frac{1}{C} & 0 & -\frac{1}{C} & -\omega & 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & 0\\
\frac{R_c}{L_r} & 0 & -\frac{R_c}{L_r} & 0 & \frac{1}{L_r} & 0 & -\frac{R_r+R_c}{L_r} & \omega & -\frac{1}{L_r} & 0 & 0 & 0\\
0 & \frac{R_c}{L_r} & 0 & -\frac{R_c}{L_r} & 0 & \frac{1}{L_r} & -\omega & -\frac{R_r+R_c}{L_r} & 0 & -\frac{1}{L_r} & 0 & 0\\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_r} & 0 & 0 & \omega & 0 & 0\\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_r} & -\omega & 0 & 0 & 0\\
-\frac{D_{dp}}{C_{bus}} & -\frac{D_{qp}}{C_{bus}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0\\
\frac{D_{dn}}{C_{bus}} & \frac{D_{qn}}{C_{bus}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}\begin{bmatrix}\bar{i}_{L1d}\\ \bar{i}_{L1q}\\ \bar{i}_{L2d}\\ \bar{i}_{L2q}\\ \bar{v}_{cd}\\ \bar{v}_{cq}\\ \bar{i}_{Lrd}\\ \bar{i}_{Lrq}\\ \bar{v}_{crd}\\ \bar{v}_{crq}\\ \bar{v}_{po}\\ \bar{v}_{on}\end{bmatrix}$$

$$+\begin{bmatrix}
0 & 0 & 0\\
0 & 0 & 0\\
-\frac{1}{L_2} & 0 & 0\\
0 & -\frac{1}{L_2} & 0\\
0 & 0 & 0\\
0 & 0 & 0\\
0 & 0 & 0\\
0 & 0 & 0\\
0 & 0 & 0\\
0 & 0 & 0\\
0 & 0 & \frac{1}{C_{bus}}\\
0 & 0 & \frac{1}{C_{bus}}
\end{bmatrix}\begin{bmatrix}v_{gd}\\ v_{gq}\\ i_{dc}\end{bmatrix} \tag{6-10}$$

coordinates can be drawn in Fig.6.8. The AC side equivalent circuit contains the d channel and q channel circuit in Fig.6.9 (a) and (b). The DC side equivalent circuit for the converter is given in Fig.6.9(c). Different from the average model of two-level converter, the 3-level converter has two duty cycle components in each equivalent circuit in d-q channel. One duty cycle Dp is for

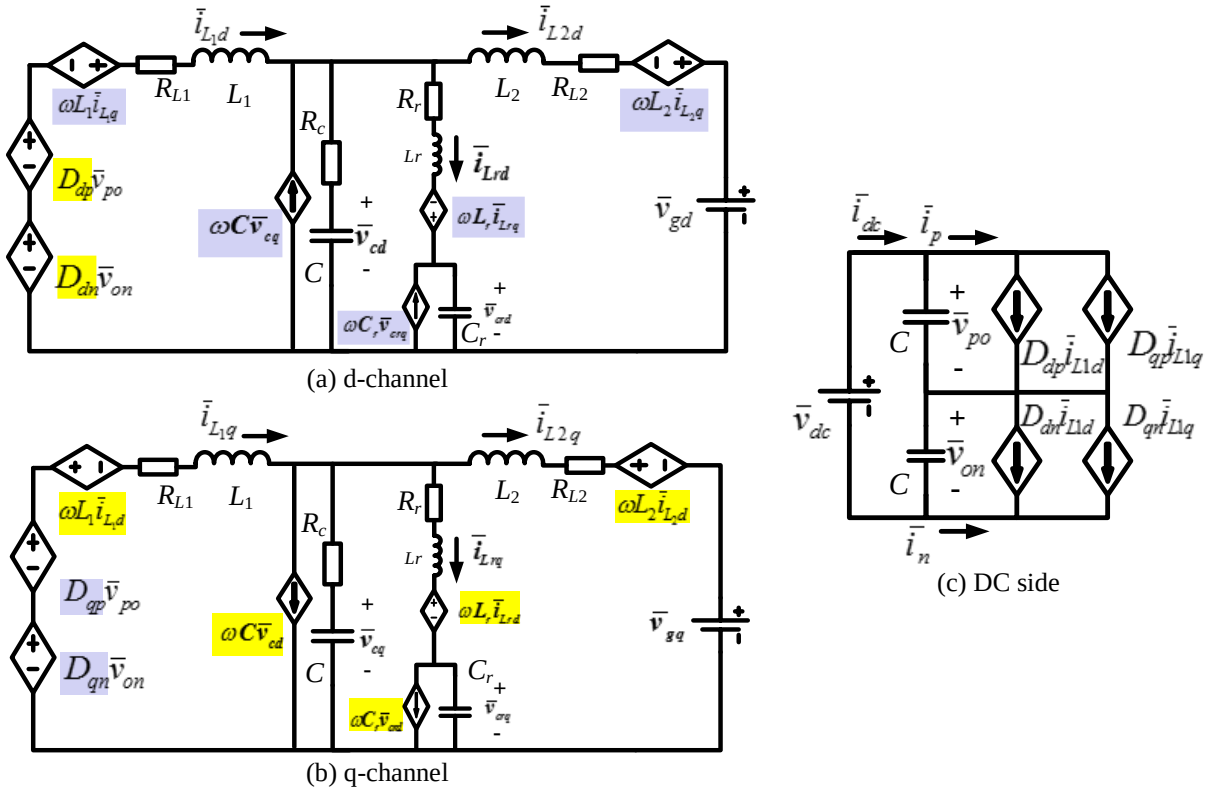


Fig. 6.9. Equivalent circuit for average model in d-q coordinates

the top DC link voltage V_{PO}, the other one Dn is for the bottom DC link voltage V_{ON}. Also the DC side equivalent circuit contains two controlled current for each channel due to the split DC link. In the AC side equivalent circuit, there are cross-coupling terms for the inductor current and capacitor voltage for both the LCL filter and the damping circuit. The cross-coupling terms are highlighted in the figure. Equation 6-10 gives the state-space differential equation for the power stage. Under steady state, all the differential items like di/dt and dv/dt are zero. Then, if the active and reactive power at grid side is a fixed value, the duty cycle for the d-q channel can be easily calculated by linear algebraic equations according to the average model in equation 6-10. With the given active/reactive power and grid voltage, the grid side current i_{L2d} and i_{L2q} in d-q frame can be calculated. Considering a symmetrical 3-level system with equal voltage for the top and bottom cell DC link. Also assuming the modulation for the positive and negative half line cycle is symmetrical, the following relationship in 6-11 can be derived for the duty cycle

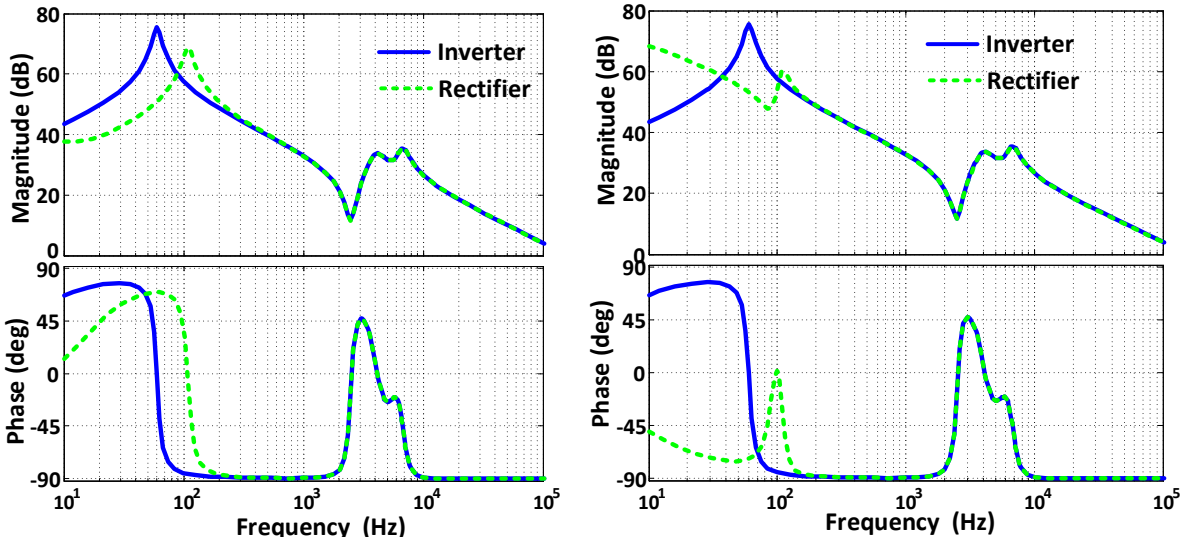
$$\begin{aligned} D_{dp} &= -D_{dn}, D_d = D_{dp} - D_{dn} = 2D_{dp} = -2D_{dn} \\ D_{qp} &= -D_{qn}, D_q = D_{qp} - D_{qn} = 2D_{qp} = -2D_{qn} \end{aligned} \tag{6-11}$$

Then the state variables like inductor current, capacitor voltage and duty cycle in d-q frame can be calculated by solving 6-12, which is the steady state equations for the system. This equation also provides the steady state duty cycle for the open loop test of the converter. The equivalent circuits in both ABC and d-q frame are simulated in Matlab/Simulink. The validity of the derived average model and equivalent circuit is verified by both simulation and experiment result.

$$\begin{bmatrix} -\frac{R_{L1}+R_c}{L_1} & \omega & -\frac{1}{L_1} & 0 & \frac{R_c}{L_1} & 0 & 0 & 0 & \frac{\bar{v}_{pn}}{2L_1} & 0 \\ -\omega & -\frac{R_{L1}+R_c}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{R_c}{L_1} & 0 & 0 & 0 & \frac{\bar{v}_{pn}}{2L_1} \\ \frac{R_c}{L_2} & 0 & \frac{1}{L_2} & 0 & -\frac{R_c}{L_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{R_c}{L_2} & 0 & \frac{1}{L_2} & 0 & -\frac{R_c}{L_2} & 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \omega & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C} & -\omega & 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 \\ \frac{R_c}{L_r} & 0 & \frac{1}{L_r} & 0 & -\frac{R_r+R_c}{L_r} & \omega & -\frac{1}{L_r} & 0 & 0 & 0 \\ 0 & \frac{R_c}{L_r} & 0 & \frac{1}{L_r} & -\omega & -\frac{R_r+R_c}{L_r} & 0 & -\frac{1}{L_r} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_r} & 0 & 0 & \omega & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_r} & -\omega & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \bar{i}_{L1d} \\ \bar{i}_{L1q} \\ \bar{v}_{cd} \\ \bar{v}_{cq} \\ \bar{i}_{Lrd} \\ \bar{i}_{Lrq} \\ \bar{v}_{crd} \\ \bar{v}_{crq} \\ D_d \\ D_q \end{bmatrix} = \begin{bmatrix} -\frac{R_c}{L_1}\bar{i}_{L2d} \\ -\frac{R_c}{L_1}\bar{i}_{L2q} \\ \frac{R_{L2}+R_c}{L_2}\bar{i}_{L2d} - \omega\bar{i}_{L2q} + \frac{\bar{v}_{gd}}{L_2} \\ \omega\bar{i}_{L2d} + \frac{R_{L2}+R_c}{L_2}\bar{i}_{L2q} + \frac{\bar{v}_{gq}}{L_2} \\ \frac{1}{C}\bar{i}_{L2d} \\ \frac{1}{C}\bar{i}_{L2q} \\ \frac{R_c}{L_r}\bar{i}_{L2d} \\ \frac{R_c}{L_r}\bar{i}_{L2q} \\ 0 \\ 0 \end{bmatrix} \tag{6-12}$$

With the average model in equation 6-10, the duty cycle to output current transfer function can be derived from this 12-order system with cross-coupling terms. With the equivalent circuit in Fig.6.9, the control to output transfer function can also be easily acquired by doing a linear analysis on the simulation model in Matlab/Simulink. The small signal perturbation is injected into the d and q channel duty cycle. The response in the d-q channel current is observed. The analytical expression of the 12-order transfer function for the control to output gain is not shown here for paragraph concise and simplicity.

With the control to output transfer function derived by linear analysis in simulation, the bode plot for the open loop transfer function can also be drawn. Since the control design is aiming for both inverter and rectifier mode, the transfer function for both the two modes are derived. For inverter mode, the DC voltage is dominated by the DC source. For rectifier mode, the DC side is connected to a resistive load at full power rating. The bode plot for the d and q channel in these two modes are displayed and compared in Fig.6.10(a) and (b) respectively. The d channel and q channel bode plot for inverter keeps the same at a wide frequency range from 10Hz to 100kHz. For the rectifier mode, the d and q channel bode plot are the same at the frequency above 300Hz. But there are discrepancy at low frequency. The bode plot for the inverter mode and rectifier mode matches with each other at high frequency for both the d channel and q channel. But the low frequency transfer functions are not the same. For the 2-stage power conversion system, the control loop design is based on the rectifier mode.

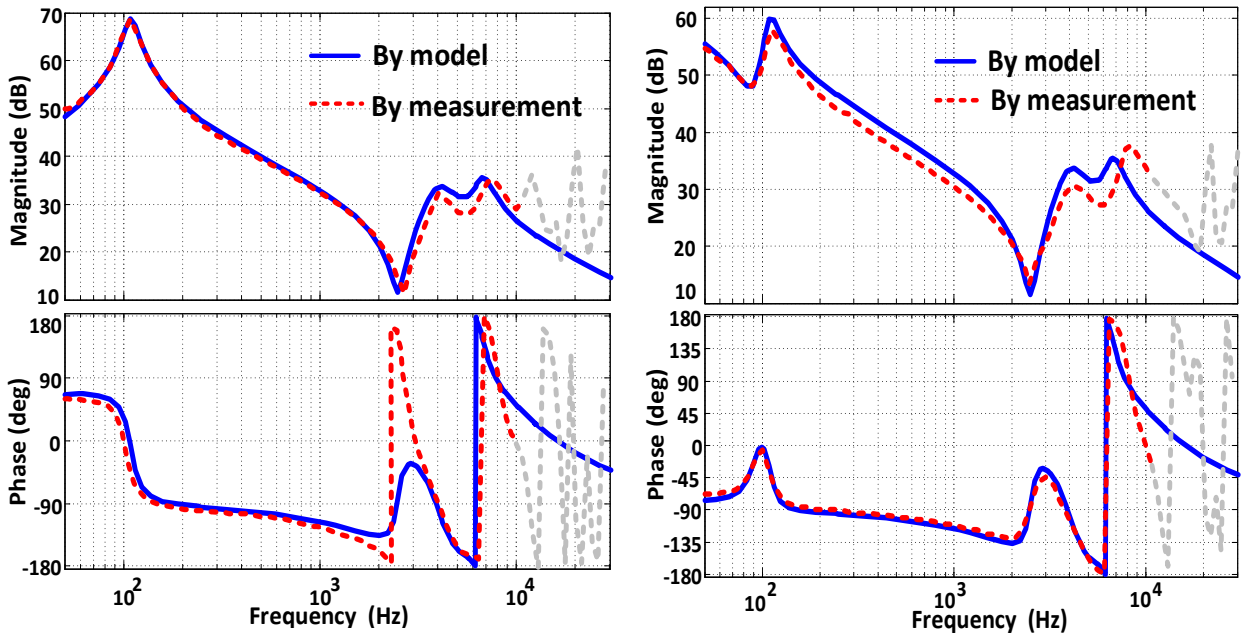


(a) d channel bode plot (b) q channel bode plot

Fig. 6.10. Control to output transfer function for inverter and rectifier modes

To verify the accuracy of the average model for the 3-level NPC converter, the open loop and closed-loop transfer function of the real converter hardware in d-q frame is measured by experiment. The transfer function is measured by injecting small signal perturbation to the duty

cycle in d-q channel and by observing the response in d-q channel current. The small signal injection and transfer function measurement is achieved by the Software Frequency Response Analyzer (SFRA) library provided by Texas Instrument. The SFRA function is incorporated into the control code of the converter. The SFRA configuration and measurement result is displayed by a graphic user interface (GUI). The 3-level NPC power converter is tested at rectifier mode with a proportionally scaled-down rating for perturbation injection. All the voltage and current is 1/5 of the full rating so that the power stage has the same loop gain. The injected perturbation frequency range is from 50Hz to 30kHz with 100 injection points. The injection amplitude is 10% of the rated value. The bode plot of the measured open loop transfer function is compared with the bode plot derived from the modeling. The result in Fig.6.11 gives the duty cycle to converter output current transfer function in both d and q channel with damping circuit. It shows a perfect match between the measurement result and the modeling result in a wide frequency range. The modeling of the 3-level converter is accurate up to half switching frequency.



(a) d channel bode plot (b) q channel bode plot

Fig. 6.11. Duty cycle to output current transfer function by measurement

6.3 Control Loop Design for 3-L NPC DC/AC Converter

With the validity of the modeling verified, the control loop design can be carried out based on the modeling of the 3-level converter. As shown in Fig.6.6, the inner loop controls the active and reactive current for the converter. The outer loop controls the DC link voltage.

6.3.1 Current Control Loop Design and Verification

The digital delay and sampling effect in real practice is considered when designing the current control loop. The delay effect is caused by many factors like the feedback sensing, the propagation delay by the gate driver, the calculation delay by the digital controller and also the delay from modulation. For the digital control used in the system, the control period is the switching cycle. The feedback signals are sampled at the beginning of each control cycle. The total delay time T_d in the loop is estimated to be one and half switching cycle with 1 cycle of sampling delay and 0.5 cycle of computation delay. The second order Pade approximation is used to estimate the delay effect as shown in 6-13. The delay transfer function H_d is multiplied to the open loop transfer function to reflect the delay effect. With the delay added, the phase margin and bandwidth for the control loop will be decreased.

$$H_d = \frac{1 - \frac{sT_d}{2} + \frac{(sT_d)^2}{12}}{1 + \frac{sT_d}{2} + \frac{(sT_d)^2}{12}} \tag{6-13}$$

The control block diagram for the d channel current loop is given in Fig.6.12. The power stage transfer function G_{id} is expressed as in 6-14 and the proportional-integral (PI) controller in 6-15 is used as the feedback controller for the current loop.

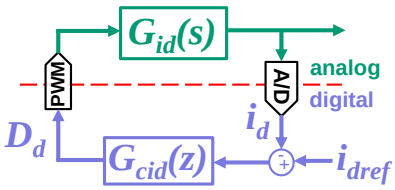
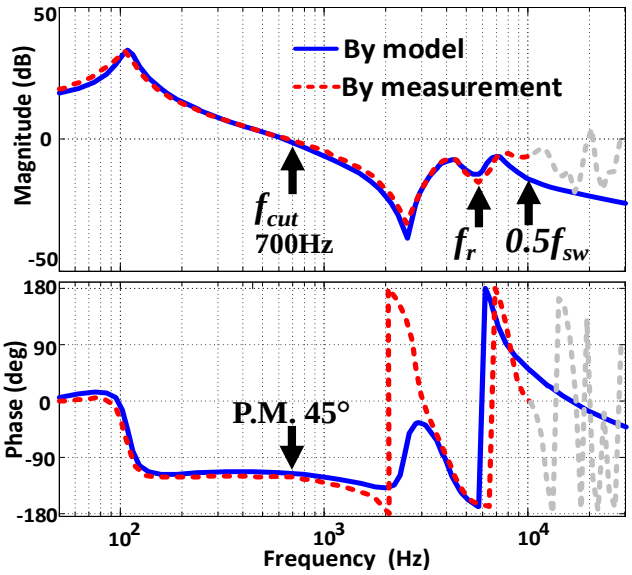


Fig. 6.12. Control block diagram for d-channel current loop

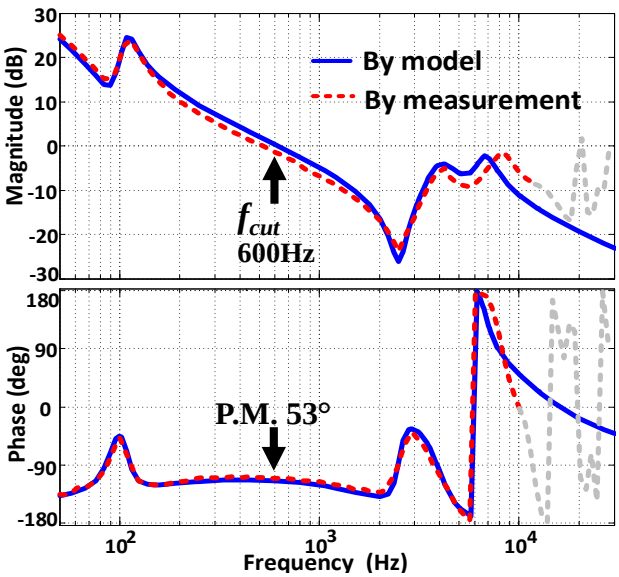
$$G_{id} = \frac{\hat{i}_{L1d}}{\hat{d}_d} \tag{6-14}$$

$$G_{c\_id} = K_p + \frac{K_i}{s} \tag{6-15}$$

The control loop design is done by the control toolbox in Matlab. The highest bandwidth for the d-channel current controller is pushed to 0.7kHz with 45° phase margin. This bandwidth is around 1/10 of the switching frequency and is high enough for the current loop. The q-channel current loop is designed to be similar as the d-channel current loop with 0.6kHz bandwidth and 53 degree phase margin. The bode plot for the closed-loop current loop gain in d and q channel is shown in Fig.6.13. Again the closed-loop transfer function by real hardware measurement is compared with the modeling result in the same figure. The solid blue curve in the figure is generated by modeling and simulation. The dashed red curve in this figure is the test result by the SFRA measurement. The measured result matches the modeling result below half of the switching frequency. The measured result shows a desired bandwidth and phase margin for the real hardware. This result verifies the control loop design in the frequency domain.



(a) d channel bode plot



(b) q channel bode plot

Fig. 6.13. Bode plot of current control loop gain

Then the current control loop design is verified by time domain simulation with average model in d-q coordinates and switching model in ABC coordinates. The d-channel current step response from half load current (100kW) to full load current (200kW) with average model in d-q coordinate is given in Fig.6.14. The overshoot and settling time for the controller is evaluated and marked in the figure. The current reaches the steady state in 4ms after the step change. The settling time is less than 1/4 of the line cycle. The same step response for d-channel current is also observed with the switching model in ABC coordinates. The 3-phase inverter output current is given in Fig.6.15(a) and the active and reactive power is shown in Fig.6.15(b). The converter output current has very small overshoot during the transient time and it reaches steady state in about 4ms. The active power at the grid side in Fig.6.15(b) also has small overshoot and smooth

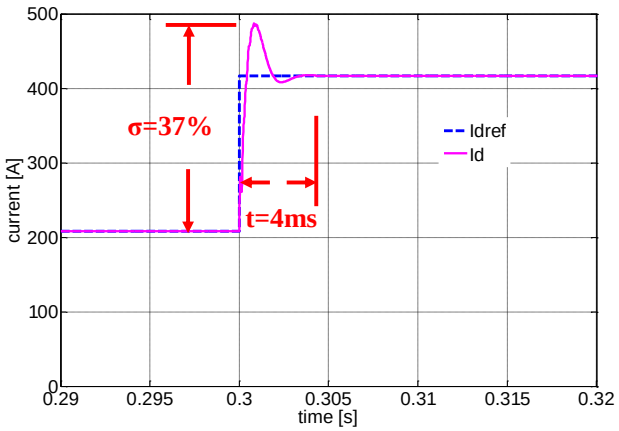
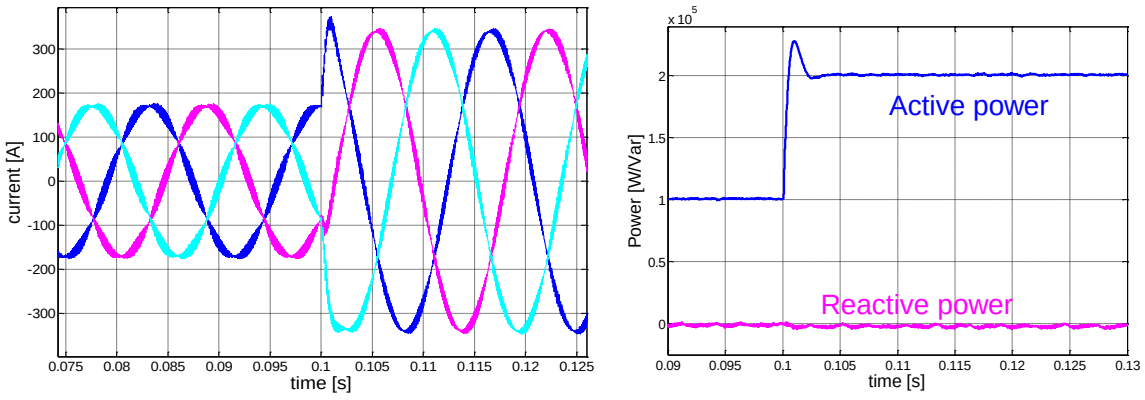


Fig. 6.14. d-channel current step response in average model

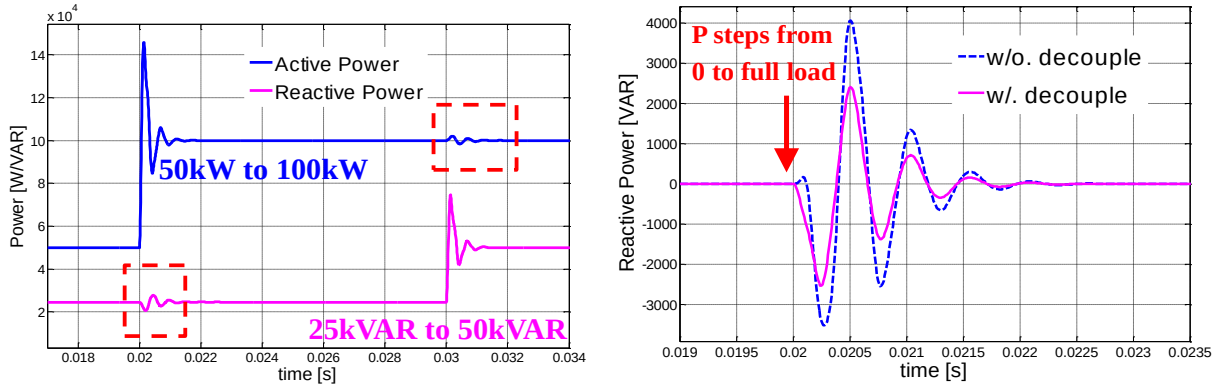


(a) Inverter current step response (b) Grid side power step response

Fig. 6.15. Step response for inverter current and grid power in switching model

transient. The result with the switching model in ABC frame matches the result with the average model in d-q frame, which validates the good performance of the current loop.

The cross-coupling effect in d-q channel transfer function is also considered and dealt with in the current control loop. The cross coupling terms is clearly highlighted in the equivalent circuit in Fig.6.9. The controlled current source for the inductor and the controlled voltage source for the capacitor in the circuit represents the cross-coupling effect between d and q channel. The d channel transient is reflected to the q channel and vice versa due to the presence of the cross coupling between d and q channel. Fig.6.16(a) shows the cross coupling effect on the active and reactive power at step transient. The active power step response incurs the reactive power oscillation during the transient and vice versa. The cross coupling effect can be partly cancelled by adding the decoupling terms to d and q channel duty cycle reference in the current loop. The control block diagram in Fig.6.6 shows the structure of the decoupling item in the current loop. The cross coupling effect caused by the two inductors L1 and L2 is considered and is subtracted from the output of the controller. This decoupling term can partly cancel the cross coupling effect at low frequency. The decoupling result is shown in Fig.6.16(b) by comparing the reactive power at the active power step with and without the decoupling control. With the decoupling control, the reactive power oscillation is largely reduced during the active power transient.



(a) Cross coupling effect on P and Q step transient (b) Decoupling result on reactive power

Fig. 6.16. Cross-coupling effect on P and Q and the decoupling result

The current loop design is also verified by the experiment result on the converter hardware. Due to the limitation of the testing facility, the experiment for the converter is tested at a proportionally scaled down ratings. Both of the DC and AC side voltage and current is reduced to 1/5 of their original value. With this proportionally scaled down rating, the inductor current ripple keeps the same. The controller design can be used with only a proportional gain of 1/5 added to the original parameters. The power test at the scaled-down rating can reflect the performance for the converter at full power rating. The step response from half load to full load of the grid current is observed and shown in Fig.6.17. The result shows that the step response for the grid current has a very smooth transient with neither obvious over shoot nor long settling time. The d-channel current feedback is also recorded from the digital controller and is given in Fig.6.18. The d-channel current step without damping is compared in the same figure. Without damping circuit, the current loop bandwidth can only be pushed to 200Hz with large oscillation and overshoot in transient. This experimental result verifies the benefit of the damping circuit. The decoupling result is also verified by experiment result in Fig.6.19 by monitoring the reactive current during the same active current step as Fig.6.18 shows. The reactive current waveform with and without decoupling control is compared. The one with control has significantly reduced

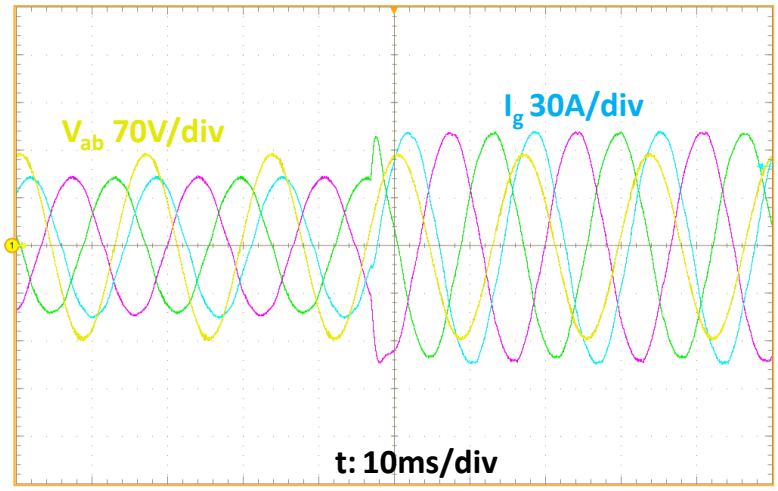


Fig. 6.17. Experimental result on step response of grid current

oscillation. The experimental result matches the simulation result very well, which verifies the implementation of the control loop on the real hardware.

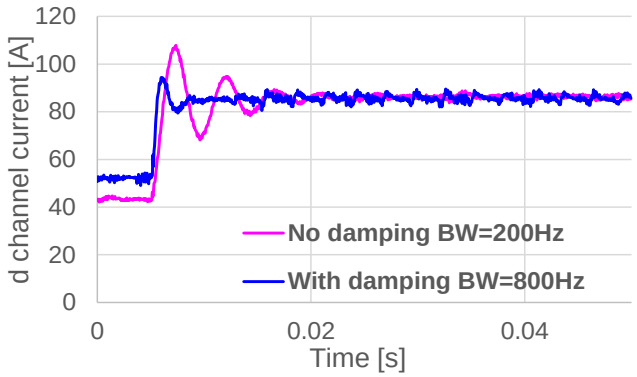


Fig. 6.18. Experimental result on step response of d-channel current

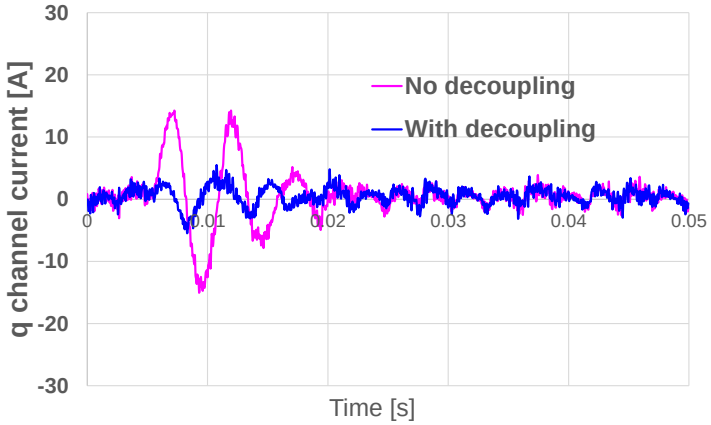


Fig. 6.19. Experimental result for the decoupling on reactive current

6.3.2 Voltage Control Loop Design and Verification

The current control loop is the inner loop for the converter that provides the active and reactive current controllability for the outer loop. For the 2-stage grid interface converter, the DC/AC stage controls its output current and also regulates its own DC link voltage. The DC voltage control is achieved by balancing the active power between AC side and DC link. The DC voltage control loop is the outer loop for the d-channel current loop. It provides the active power current reference to the inner loop. So the voltage loop is designed after the current loop is closed. The equivalent circuit with both voltage and current control is shown in Fig.6.20. The

loop to be designed is from d-channel current reference to DC link voltage. The perturbation is injected in

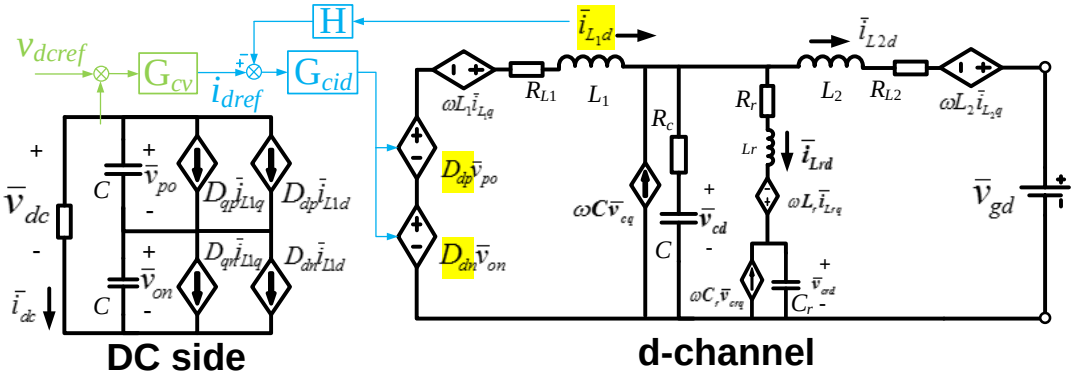


Fig. 6.20. Closed current loop d-channel and DC link equivalent circuit

I_{dref} and the response on V_{dc} is observed. The voltage loop regulates DC link voltage by controlling the d channel current reference. The bode plot of the V_{dc} to I_{dref} is given in Fig.6.21. Similar as the current loop design, the bode plot is generated by both the modeling result and the measurement result on the real hardware. The comparison shows that the model and equivalent circuit accurately reflects the power stage behavior in a wide frequency range. The voltage loop is designed for rectifier mode with resistive load. The voltage controller also uses PI compensator. The designed bandwidth for the DC link voltage loop is at 200Hz with 42° phase margin. The bode plot of the voltage loop gain is show in Fig.6.22. Similarly, it gives the comparison between modeling and measurement result, which verifies the voltage loop design.

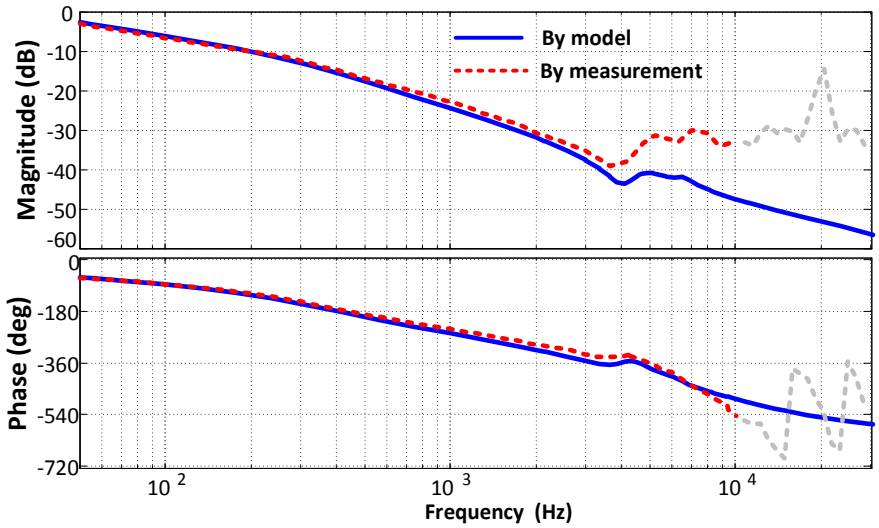


Fig. 6.21. DC link voltage to d-channel current reference transfer function

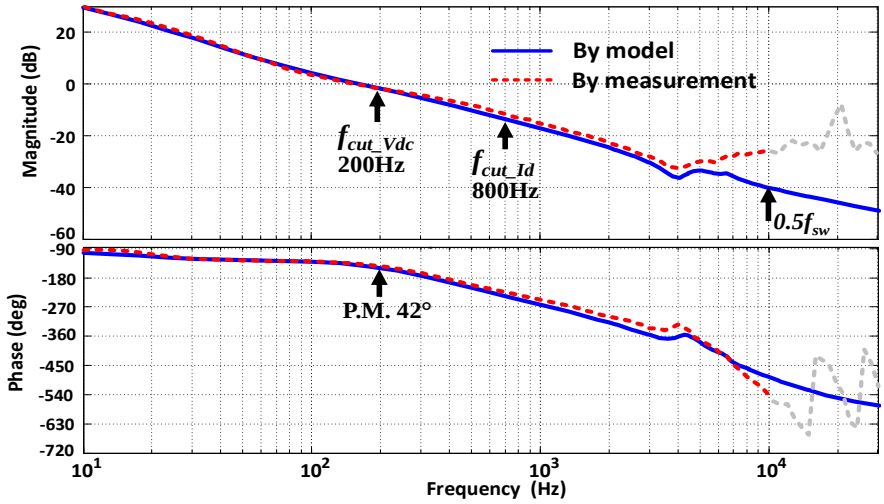
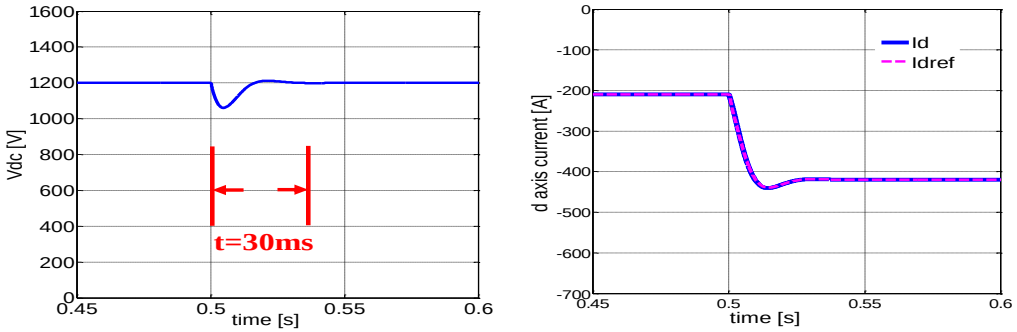


Fig. 6.22. Bode plot for the voltage loop gain

The performance for the voltage loop controller is also verified by the simulation and experiment result in time domain. A load transient at the DC link is applied to the simulation model to observe the step response of the voltage loop controller. The resistive load at the DC link is increased from half load (100kW) to full load (200kW). The DC link voltage and also the d-channel current is simulated first in the average model in d-q coordinates. The result is given in Fig.6.23. It can be seen that the DC link voltage has a sag during the load transient. The transient lasts for about 1-2 line cycles. The undershoot of the DC link voltage is less 6%. The d-channel

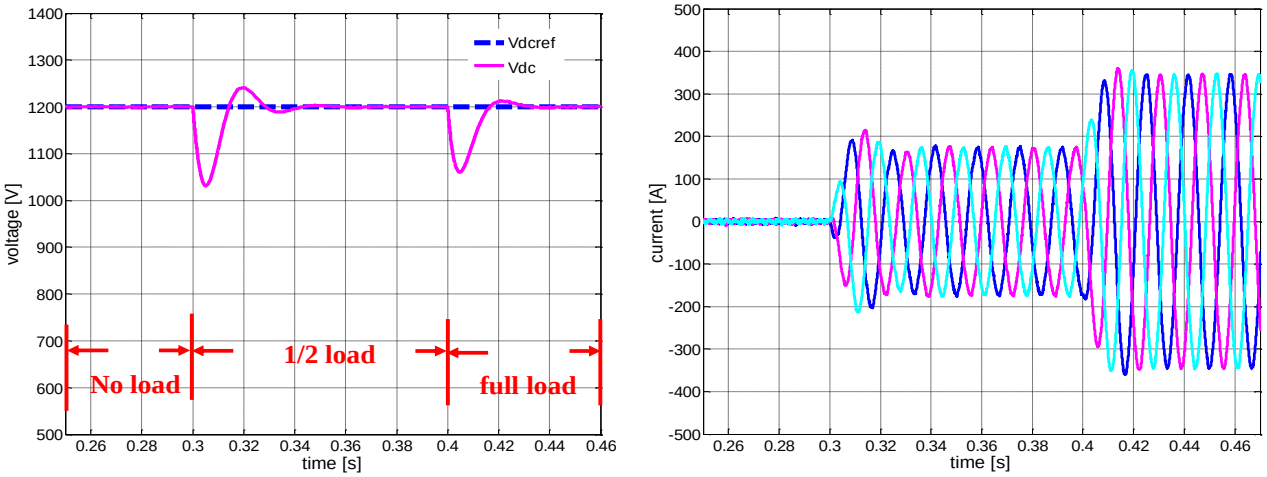
current response to the load transient in Fig.6.23(b) shows that the voltage loop has lower bandwidth than the current loop so the current controller is fast enough to follow the reference generated by the voltage loop and respond to the transient.



(a) DC link voltage (b) d-channel current and its reference

Fig. 6.23. DC link voltage and d-channel current step response in average model

The DC voltage and grid current waveform with switching model is also simulated in ABC coordinates. The converter starts running from no load condition to half load and then to full load. The voltage loop should be able to regulate the DC voltage with only DC link capacitors. The transfer function of the power stage is changing with the load conditions for the rectifier mode. At light load or even no load condition, the voltage have lower bandwidth because there is very little resistive damping for the power stage. The step response for the DC link voltage is given in Fig.6.24(a). The DC link voltage stays at the rate value all the time with smooth transient during the load change. The transient response for different load transients are not the same due to the different transfer function and bandwidth for the loop gain. The grid current response is given in Fig.6.24(b) with the same load change. It shows that the grid current is almost zero when there is no load. The grid current step response doesn't have too much overshoot or oscillation either, which verifies the good performance for the voltage control loop.



(a) DC link voltage (b) Grid current

Fig. 6.24. DC link voltage and grid current step response in switching model

Finally, the voltage loop is added in the converter hardware and the DC/AC converter is tested with both voltage and current loop closed. The converter is still tested at the scaled down power rating. The control result of the DC voltage loop is first verified by stead state waveform in Fig.6.25. The figure shows a pure sinusoidal current waveform and constant DC link voltage

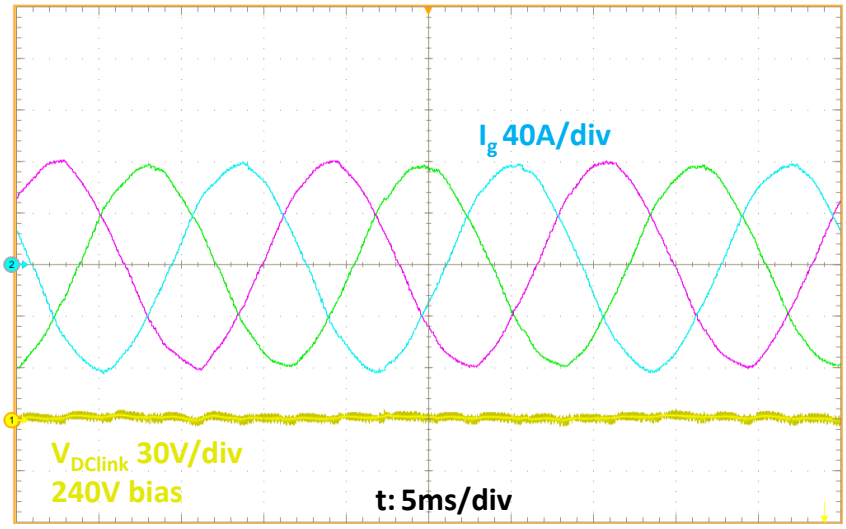


Fig. 6.25. Experimental result for I_g and V_{dc} at steady state

at rated value. Then the performance of voltage control loop is verified by the startup transient in Fig.6.26. The circuit starts with the diode rectifier mode when all the switches are off. Then the closed-loop controllers start working and the converter works at rectifier mode. The DC link

voltage is controlled at rated value. There is no obvious transient at the startup. Finally, the load step transient response is tested on the hardware. The experimental result for a load transient response is shown in Fig.6.27. The converter starts from no load condition and the DC link voltage is regulated by the voltage loop. The grid current is almost zero since no active power is

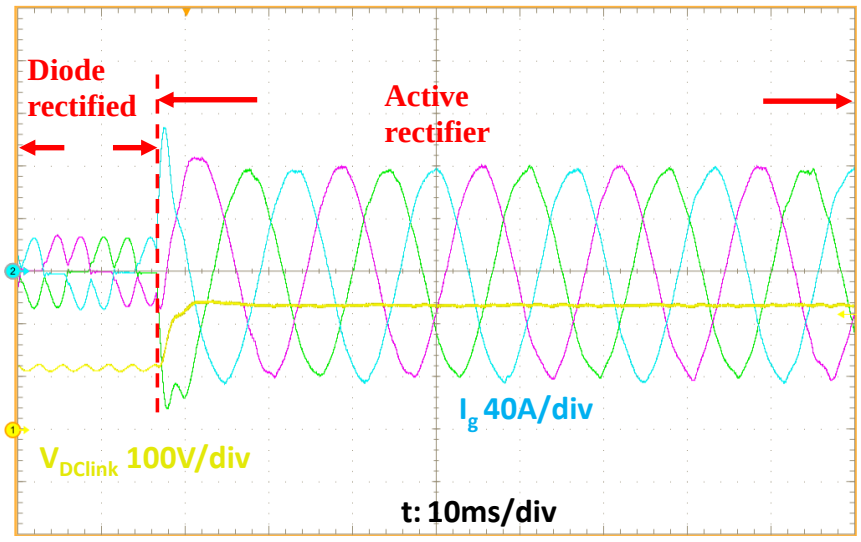


Fig. 6.26. Experimental result for I_g and V_{dc} at startup transient

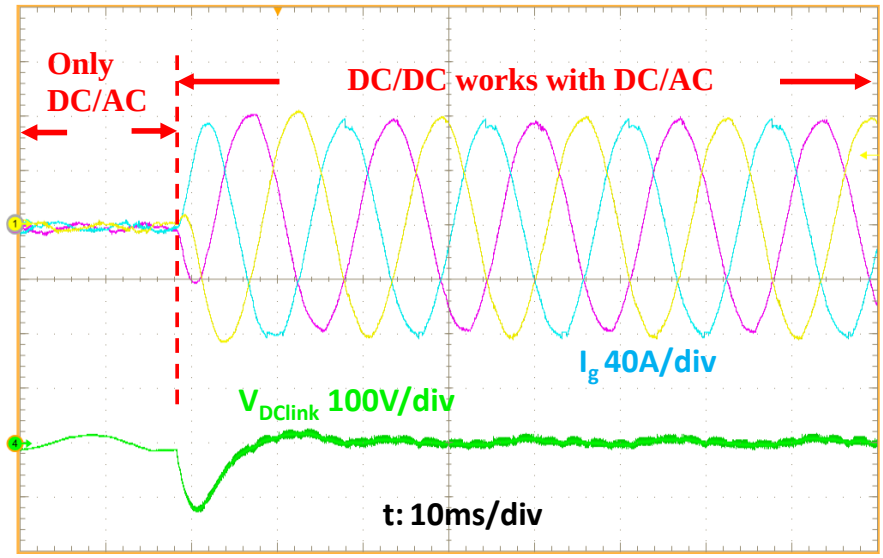


Fig. 6.27. Experimental result for I_g and V_{dc} at load transient

drawn from the grid. Then the full load is applied to the DC link and the grid current reaches rated value. The DC link voltage has very slight transient after the load step change. No obvious overshoot or oscillation can be observed from the grid current waveform. The experimental

result for voltage loop control also matches well with the simulation result. The result shows the full controllability of the DC/AC system at very light load or even no load condition. The system also has very smooth transient from zero to full load step. With the voltage loop closed, the DC/AC part of the power conversion system is finished with full control functions.

6.4 Input and Output Impedance for System Stability

With the average model and equivalent circuit for the 3-level DC/AC converter verified by real measurement result, the AC side and DC side impedance for the power stage can also be derived by the equivalent circuit for system stability analysis. The input and output impedance for both rectifier and inverter mode can be derived by the equivalent circuit as shown in Fig.6.28. For the converter working at rectifier mode, the grid side impedance is the input impedance and the DC side impedance is the output impedance. For the inverter mode operation, it is just the opposite. The d and q channel impedance at grid side for open loop inverter and rectifier mode is

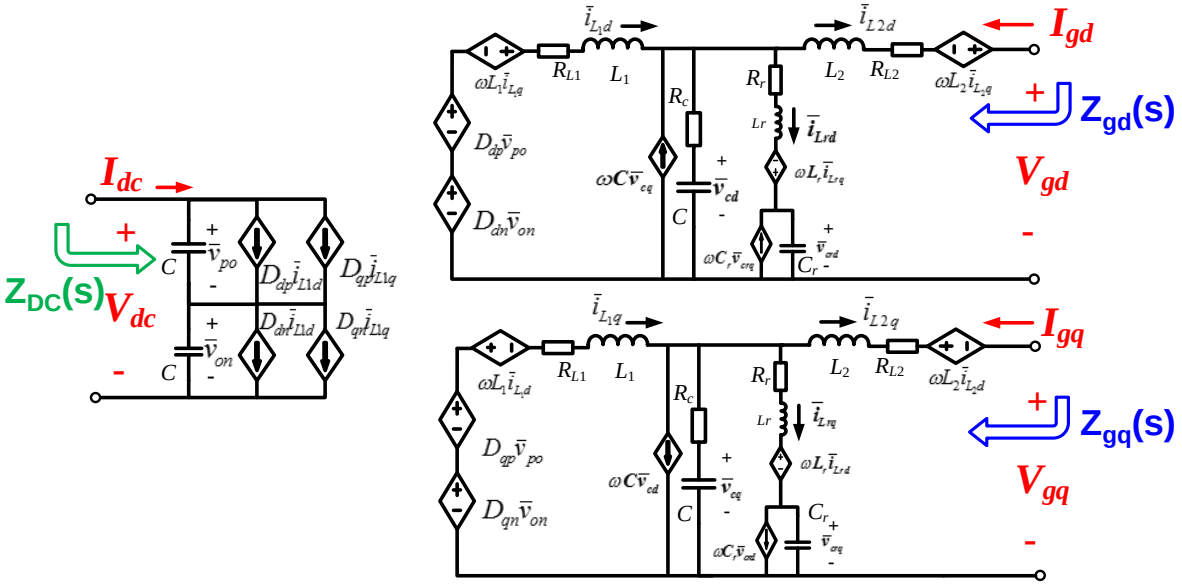
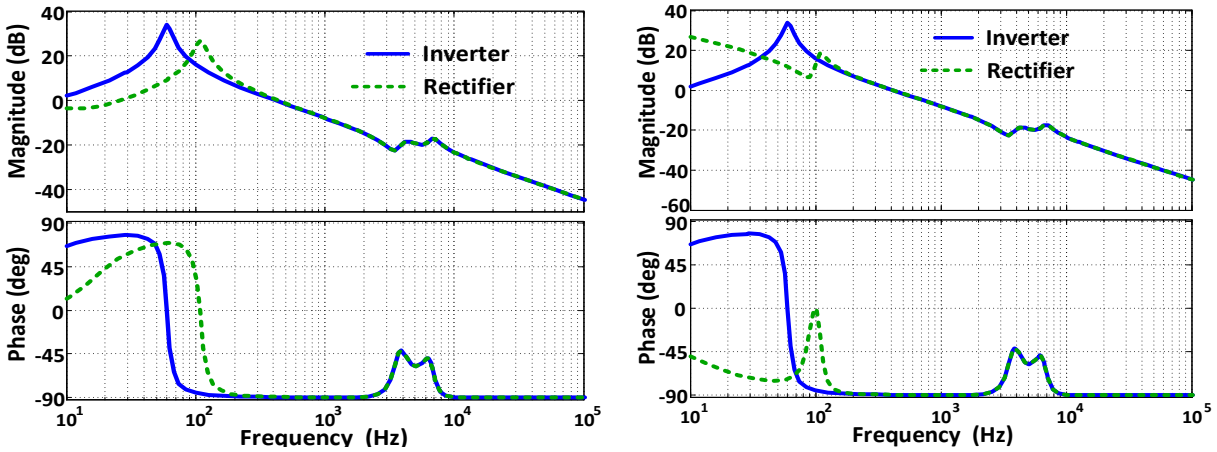


Fig. 6.28. Equivalent circuit for input and output impedance for DC/AC converter

analyzed at first. The bode plots for the impedance at inverter and rectifier mode are compared in Fig.6.29. It shows that the d-q channel impedance for inverter and rectifier follows the same

pattern of the d-q channel control (duty cycle) to output (current) transfer function. The impedance for inverter and rectifier keeps the same above 300Hz. Rectifier mode has different impedance for d and q channel while the inverter mode has same impedance for d and q channel. The bode plot for DC side impedance at rectifier and inverter mode is displayed in Fig.6.30. The DC side impedance for rectifier and inverter mode stays the same in the whole frequency range.



(a) d channel bode plot (b) q channel bode plot

Fig. 6.29. Bode plot of grid side d-q channel impedance for inverter and rectifier

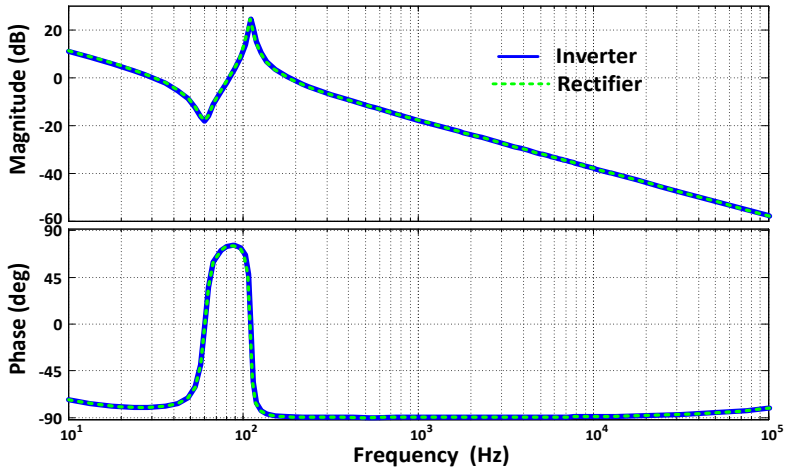
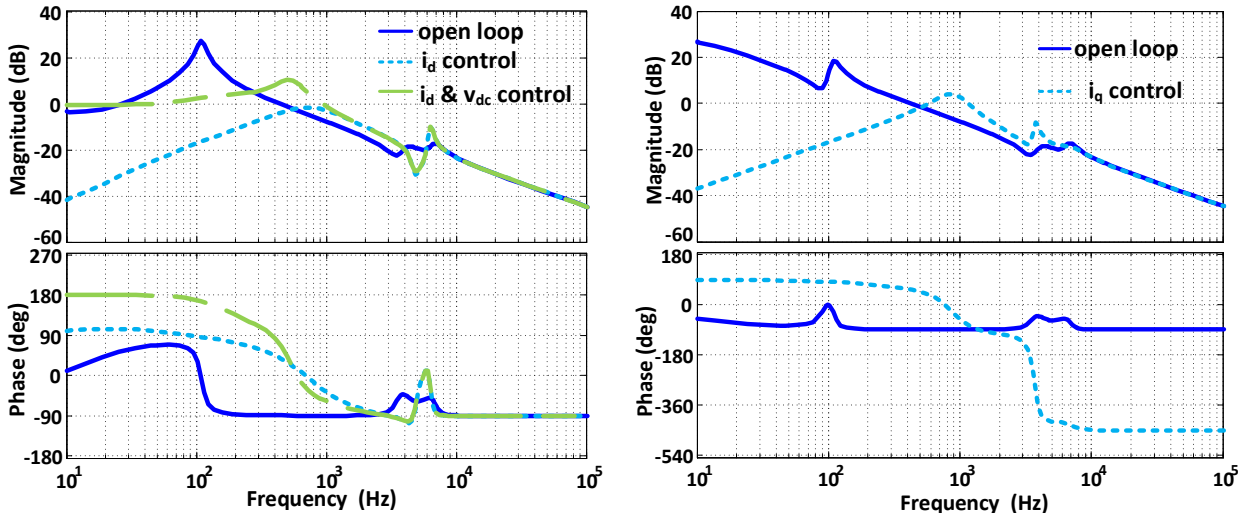


Fig. 6.30. Bode plot of DC side impedance for inverter and rectifier

After the grid side current and DC link voltage control loop is closed, the grid side and DC side impedance for the 3-level DC/AC converter is brought out for discussion with closed-loop control. The grid side impedance in d-q channel with and without control is compared in Fig6.31.

It shows the impedance with open loop, with current control and with both current and voltage control. The DC side impedance with the same comparison is shown in Fig.6.32. The impedance bode plot comparison shows that the impedance at high frequency keeps the same for different control loop. The control loop only shapes the low frequency impedance. The grid side impedance with closed-loop control is important data to analyze the interaction between the grid



(a) d channel bode plot (b) q channel bode plot

Fig. 6.31. Bode plot of grid side impedance with closed loop control

and the converter. This impedance largely influence the system stability when the converter is connected to a weak grid or a grid with large leakage inductance. The DC side impedance is also critical for the stability analysis of the 2-stage power conversion system. This impedance of the DC/AC converter interacts with the impedance of the DC/DC chopper stage. For rectifier mode, the DC side impedance is the output impedance of the source converter. For inverter mode, it is the input impedance of the load converter. With the DC side impedance derived, the stability and interaction for the 2-stage power conversion system can be analyzed.

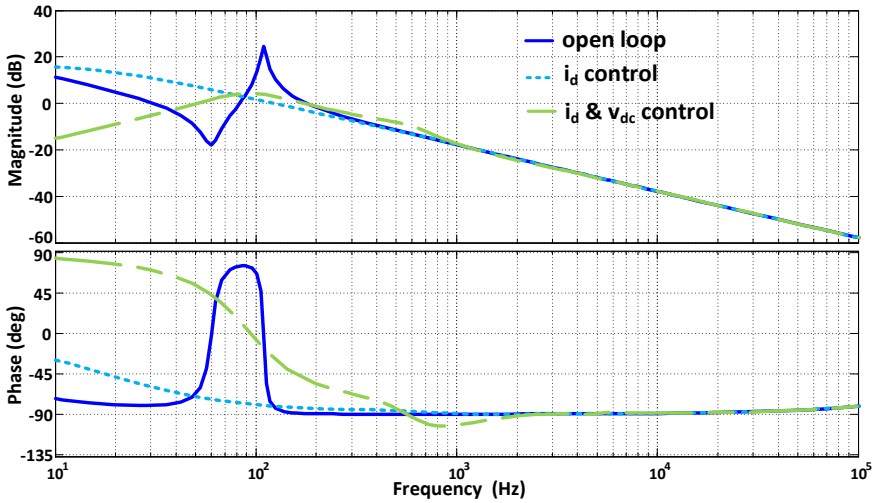


Fig. 6.32. Bode plot of grid side impedance with closed loop control

In order to investigate the subsystem interaction between the DC/AC converter and the DC/DC chopper, the equivalent circuit for both the load converter and source converter should be derived. Fig.6.33 shows the overall system structure for the 2-stage power conversion system. The control block diagram for the system is given in Fig.6.6. The DC/AC converter regulates DC link voltage while the DC/DC chopper controls the DC bus voltage and current. When the power flows from grid to the DC bus, the AC/DC rectifier is the source converter and the DC/DC buck converter is the load converter. It is just the opposite when the power is delivered from the DC bus to the grid. The subsystem interaction is largely influenced by the output and input impedance for the two converters. The equivalent circuit of DC/AC converter with full control is

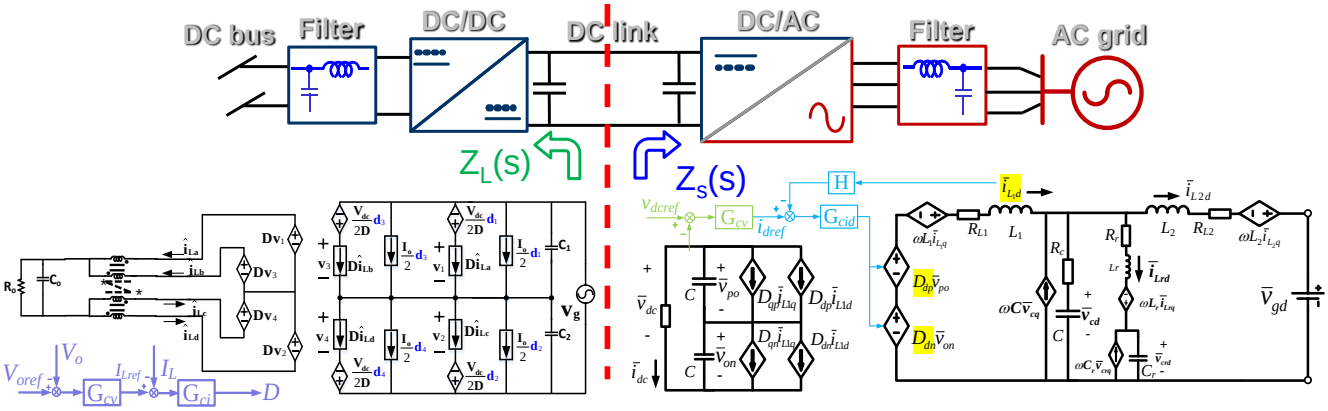


Fig. 6.33. Equivalent circuits of the 2-stage power converter for impedance analysis

shown in Fig.6.20 and in the bottom right part in Fig.6.33. For the DC/DC chopper stage, the equivalent circuit with full control function is also derived. The detailed power stage and control loop design for the DC/DC chopper is introduced in Chapter 7. Its equivalent circuit and control block diagram is given in the bottom left part in Fig.6.33 for impedance analysis in this chapter. With this equivalent circuit, the input impedance for the load converter $Z_L(s)$ can be derived and compared with the output impedance for the source converter $Z_S(s)$. Fig.6.34 shows the bode plot of the source output impedance and load input impedance. The gain diagram shows that $Z_S(s)$ is below $Z_L(s)$ for all the frequency, which means the return ratio $L(s)$ is smaller than 1. The 2-stage converter system is stable with minimal interaction between the two sub-systems. The Nyquist diagram for the return ratio $L(s)$ is also given in Fig.6.35. The return ratio stays away from -1, which verifies the system stability for all frequency.

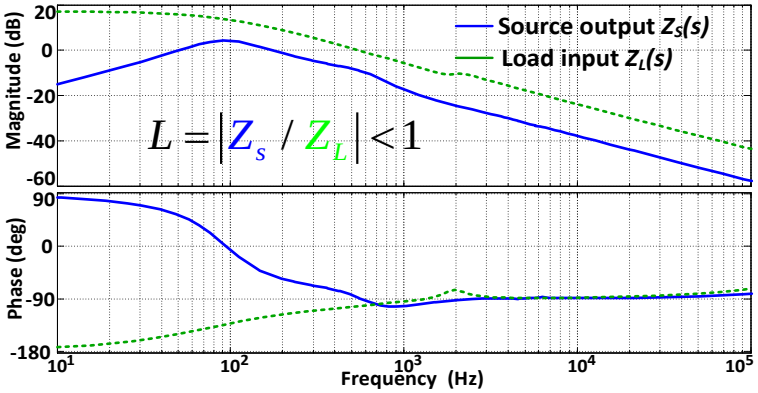


Fig. 6.34. Bode plot for source output and load input impedance

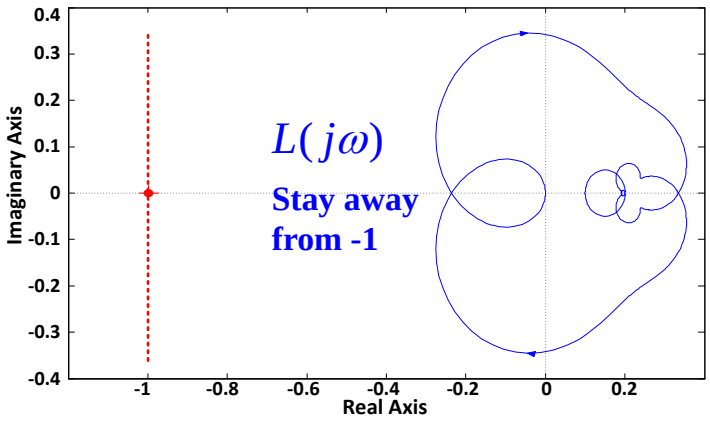


Fig. 6.35. Nyquist diagram for return ratio L

6.5 Summary and Conclusion

This chapter concentrates on the modeling and control loop design for the 3-level NPC grid interface converter with bidirectional power flow. Different control strategies for the grid interface converter are first investigated and compared. The control requirements and objectives for the grid interface converter in the micro-grid system are identified and pinpointed. The new challenges for the power converter that operates in the micro-grid system with renewable energy and energy storage are discussed. The grid interface converter for distributed generation system in the micro-grid should be able to regulate its own bus voltage and support the local loads at both grid connected mode and stand-alone mode. In addition to that, different converters for distributed generation system in the micro-grid system should share the local loads and smoothly synchronize with the grid without fighting with each other. To achieve these objectives and goals, various control strategies for the grid interface converter are proposed. These control strategies are classified into several categories. The features for different categories are introduced in this chapter and the pros and cons for them are compared. For the general purpose power conversion system with various possible applications, the control loop design should be universal and works for different applications like PV system, battery storage, DC loads or DC bus. For this reason, the inner control loop controls the converter output active and reactive current, which enables the outer loop to control the active and reactive power. It also provides flexibly configured control architecture with the P and Q interface for different high level control strategies. With the control strategy determined, the average model for the DC/AC stage of the power conversion system is derived. This model considers the converter power stage in detail, including not only the harmonic filter, but also the damping circuit. The average model and

equivalent circuits in both ABC frame and d-q frame are derived. This model and equivalent circuit can accurately depict the behavior of the converter. The accuracy of the model is verified by measuring the transfer function of the real hardware. The grid side and DC side impedance for the DC/AC converter is also derived based on the average model. The control loop is designed based on the loop gain by both modeling and measurement. The design is verified in both frequency domain and time domain by equivalent circuit simulation and experiment on the hardware. The experimental result verified the control loop design for the DC/AC stage of the power conversion system.

CHAPTER.7 INTERLEAVED 3-LEVEL DC/DC CHOPPER WITH COUPLED INDUCTOR

As mentioned in the previous chapters, the 3-level power conversion system uses a 2-stage system architecture to achieve high modularity and to decouple the DC side and AC side. It is a very important step to minimize the dynamic interactions between the two sub-systems for micro-grid application [1]. The design and optimization for the 3-level NPC DC/AC converter has been thoroughly investigated in terms of the power stage switching characteristics, modulation scheme and control strategy. The DC/DC chopper stage is then studied since it also faces several design challenges for high power density and high efficiency.

Similar to the 3-level NPC DC/AC converter, the DC/DC chopper uses 3-level topology not only because of the high modularity for the whole system, but also because of several other benefits that are shared by the DC/AC part [2]-[4]. By using the 3-level topology, the switching stress, dv/dt and device rating is reduced. Also the 3-level DC/DC converter has even lower inductor current ripple than the 2-phase interleaved 2-level DC/DC converter [4]. In the high power application for the micro grid system, paralleled or interleaved 3-level DC/DC phase leg configuration is adopted, which may further reduce the current ripple and shrink the passive component size due to the ripple cancellation by interleaving. In order to reduce the inductor current ripple, the interleaved DC/DC converter always works with the coupled inductor in various voltage and power ratings for several different applications [5]-[9]. The coupled inductor can further reduce the passive component size, as well as to improve the steady-state efficiency [10]. Most of the previous literatures focus on the interleaving of the 2-level converters. Only a few papers talk about the interleaved 3-level phase legs [11], even few discusses the interleaved 3-level phase leg with coupled inductors [12]. None of them give the detail analysis of the

interleaving methods for the 3-level phase legs and their related inductor current ripple waveform and expression.

In this chapter, the system structure for the interleaved 3-level DC/DC chopper stage is introduced at first. Then the different interleaving methods for the 3-level phase legs are discussed in detail. The inductor current ripple, output current ripple and common mode voltage is analyzed and the analytical expression for the current ripple is given. To further reduce the inductor current ripple and to suppress the circulating current within the interleaved phase legs, the coupled inductor is added to the power stage and the inductor current ripple with coupled inductor is also analyzed. Then a novel inductor structure is proposed with two tape-wound cores and two magnetic bridges. This integrated coupled inductor has inverse coupling to reduce the inductor current ripple and suppress the circulating energy. It also contains positive coupling between the two cores to increase the leakage inductance and to reduce the output current ripple. This concept is brought into implementation and tested on the 3-level DC/DC chopper.

7.1 Current Ripple Analysis for the Interleaved 3-level DC/DC Chopper

7.1.1 Interleaving Modes for 2-phase 3-level Chopper

The power stage of the DC/DC chopper shares a similar phase leg building block structure and layout for modularity concern. It also uses the same laminated bus bar as the DC/AC stage so that the two stages can be connected to the 1200V DC link in a back to back manner. To handle the 200kW power with the similar phase leg building block as the DC/AC part, two of the phase legs are connected in parallel. The structure and configuration of the whole power conversion system is given in Fig.1.19 and is not repeated here. But the structure of the 3-level DC/DC chopper stage is given in Fig.7.1. The bidirectional chopper can work at buck mode or boost mode. The two outer switches in each phase leg (S_{1a} and S_{4a} for phase leg A) are actively

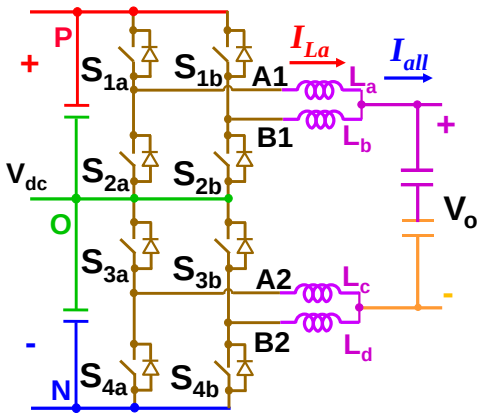


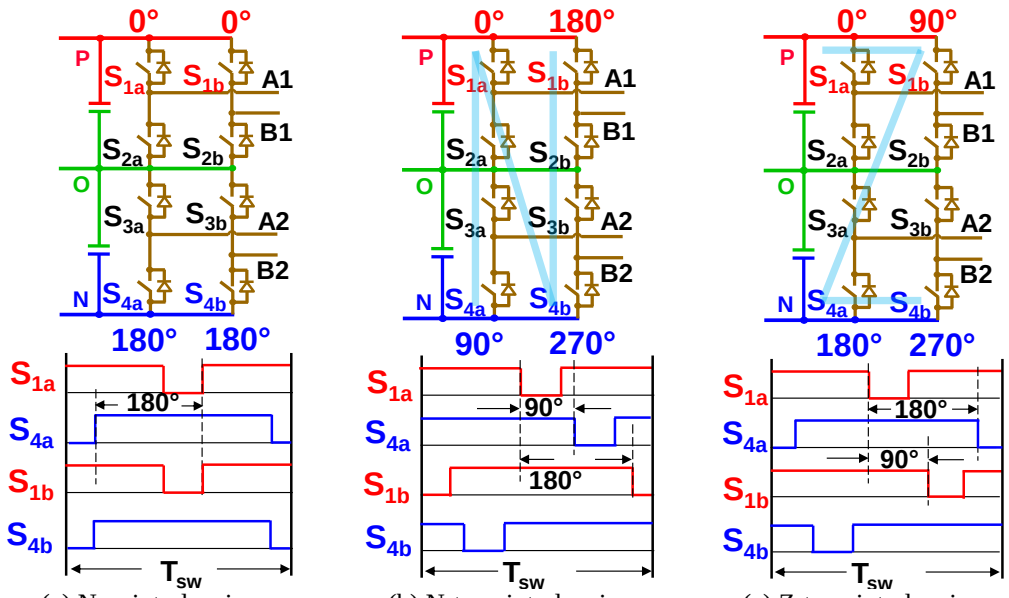
Fig. 7.1. Power stage structure of the 2-phase 3-level DC/DC chopper

controlled in buck mode. The two inner switches S_{2a} and S_{3a} are switched in complementary with the two outer switches. It is just the opposite for boost mode. The two inner switches (S_{2a} and S_{3a} for phase A) are controlled and the two outer switches (S_{1a} and S_{4a}) follows the two inner switches in complementary manner. This is the basic operating principles for each phase leg of the chopper with the bidirectional power flow. With the two phase legs, the DC/DC chopper can be operated in three different ways, which is the non-interleaving case, N-type interleaving case and Z-type interleaving case. These three different operating modes result in different inductor current ripple and common mode voltage. As a result, the operating principle and related inductor current ripple for the three operating modes are analyzed in detail. Since the interleaving type is not influenced by the power flow, the following analysis is based on buck mode and the current reference direction is labeled in Fig.7.1.

The switching sequences of controllable switches for the three cases are given in Table.7.1. For non-interleaving case, the controllable devices of the two phases are switched in phase and the switching pattern is shown in Fig.7.2(a). For the N-type interleaving case, the gate signal sequence of the 4 switches is $S_{1a}\rightarrow S_{4a}\rightarrow S_{1b}\rightarrow S_{4b}$, forming an N-shaped path as in Fig.7.2(b). For the Z-type interleaving case, the switching sequence of controllable switches is $S_{1a}\rightarrow S_{1b}\rightarrow S_{4a}\rightarrow S_{4b}$, forming a Z-shaped path as in Fig.7.2(c).

Table 7.1. Phase angle of the controllable switches for each phase leg

	Phase A		Phase B	
Non-interleaving	S_{1a}	0°	S_{1b}	0°
	S_{4a}	180° (π)	S_{4b}	180° (π)
N-type interleaving	S_{1a}	0°	S_{1b}	180° (π)
	S_{4a}	90° (π/2)	S_{4b}	270° (3π/2)
Z-type interleaving	S_{1a}	0°	S_{1b}	90° (π/2)
	S_{4a}	180° (π)	S_{4b}	270° (3π/2)



(a) Non-interleaving (b) N-type interleaving (c) Z-type interleaving

Fig. 7.2. Interleaving modes and their gate signals sequence

7.1.2 Inductor & Output Current Ripple Analysis

To analyze the inductor current ripple for different interleaving modes, the equivalent circuit for the 2-phase 3-level DC/DC chopper should be derived. The switching poles for the top and bottom cell for each phase leg is equaled to a controlled voltage sources (V_{ao}, V_{bo}, V_{co}, V_{do}). The DC output voltage are represented by constant voltage sources. Then the equivalent circuit is derived in Fig.7.4. Due to the circuit symmetry, the voltage between point G and O is given by

$$V_{GO} = \frac{V_{ao} + V_{bo} + V_{co} + V_{do}}{4} \tag{7-1}$$

Then the voltage across the inductor can be expressed as following:

$$V_{Li} = V_{iO} - \frac{V_{out}}{2} - V_{GO} \text{ (i=a,b,c)} \tag{7-2}$$

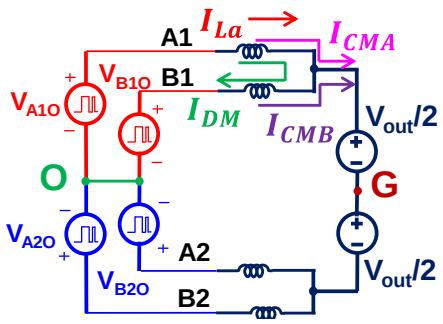


Fig. 7.3. Equivalent circuit for 2-phase 3-level DC/DC converter.

The equation 7-2 shows that the voltage across the inductor is related to the switching pole output voltage, load voltage and V_{GO}. The impacts of V_{GO} on inductor current ripple are given in [13] and [14] with inductor current ripple and V_{GO} waveforms shown. The different interleaving modes result in various phase-shift angles for the gate signals and consequently cause different V_{GO} waveform. This voltage is beneficial for the inductor voltage-second reduction and current ripple reduction. For the non-interleaving case, the V_{GO} gives the lowest inductor current ripple. For the other two interleaved cases, the inductor current ripple is larger than the non-interleaved case. This is because the non-interleaved case parallel the two phase legs together so that there is no circulating energy within the phase legs. But for the two interleaved cases, the interleaving causes circulating current through the two phase legs and therefore increases the inductor current ripple. For the non-interleaving case, the inductor current ripple ΔI_L is related to the duty cycle and the inductance by the following expression:

$$\Delta I_{L\_non} = \begin{cases} \dfrac{V_{dc} \cdot T_{sw}}{4L} \cdot D \cdot (1-2D) & 0<D<0.5 \\ \dfrac{V_{dc} \cdot T_{sw}}{4L} \cdot (1-D) \cdot (2D-1) & 0.5<D<1 \end{cases} \tag{7-3}$$

where V_{dc} is the whole DC link voltage and T_{sw} is the switching period. The output current ripple ΔI_{all} before the output capacitor is two times of the inductor current ripple for the non-interleaving case since the two phase legs are in phase with each other. The maximum inductor current ripple and output current ripple is given as follow:

$$\Delta I_{L\_\max\_non} = \frac{V_{dc} \cdot T_{sw}}{32L}$$
$$\Delta I_{all\_\max\_non} = \frac{V_{dc} \cdot T_{sw}}{16L} \quad (7\text{-}4)$$

The above analysis gives the inductor current ripple for the non-interleaving case. However, the current ripple analysis for the N-type and Z-type interleaving case is not so straightforward. The interleaving brings circulating current within the two phase legs and complicates the inductor current ripple analysis. The output current is split into common mode and differential mode for derivation simplicity. The common mode current in the two phase legs contributes to the output current and the differential mode current in the two legs represent the circulating current within the legs. For phase leg A, the common mode and differential mode voltage V_{CM} and V_{DM} which generated CM and DM current is defined as

$$V_{CM\_A} = \frac{V_{ao} + V_{bo}}{2}, \quad V_{DM\_A} = \frac{V_{ao} - V_{bo}}{2} \quad (7\text{-}5)$$

Then the equivalent circuit for inductor current ripple analysis at interleaving case is derived in Fig.7.4. The inductor current for phase A can be separated into two parts, the common mode current I_{CMa} and the differential mode current I_{DM}. The equivalent circuit indicates that the inductor current is related to both the output current I_{CMa} and the circulating current I_{DM}. It also shows that the CM current is generated by the V_{CM}-V_{GO} and the DM current is generated by the difference between the two phase legs, which is V_{ao}–V_{bo}. With the given pulse sequence, the CM

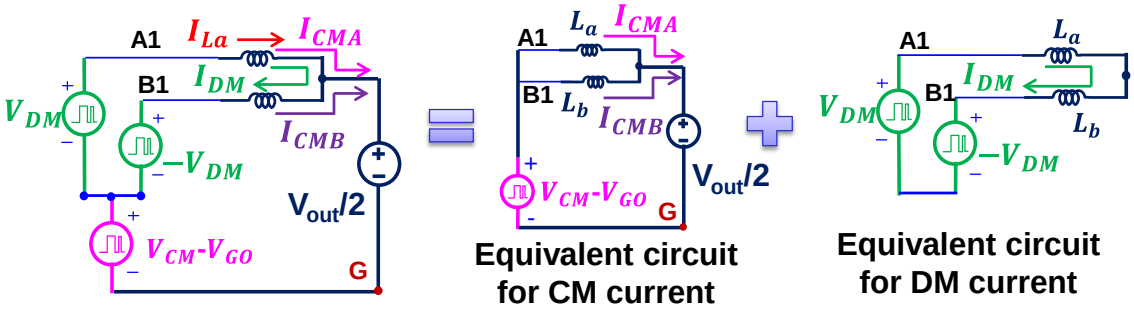
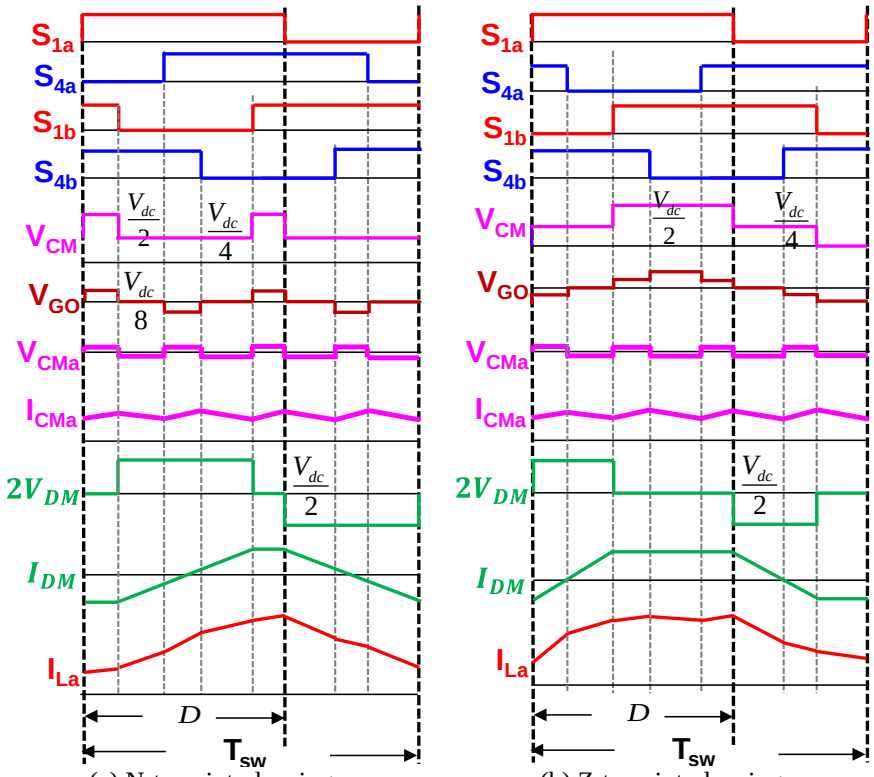


Fig. 7.4. Equivalent circuit for inductor current ripple analysis at interleaving case.

voltage, DM voltage and the inductor current waveform for the N-type and Z-type interleaving case is given in Fig.7.5. [13], [14]



(a) N-type interleaving (b) Z-type interleaving

Fig. 7.5. Gate sequence and inductor current waveform for two interleaving modes

According to the equivalent circuit in Fig.7.4 and the waveforms in Fig.7.5(a). The inductor current ripple of the N-type interleaving case is derived as:

$$\Delta I_{L\_N}=\begin{cases}\frac{V_{dc}T_{sw}}{8L}\cdot(D-4D^2)+\frac{V_{dc}T_{sw}}{4L}\cdot D & \text{D<0.25}\\ \frac{V_{dc}T_{sw}}{16L}\cdot(-1+6D-8D^2)+\frac{V_{dc}T_{sw}}{4L}\cdot D & \text{0.25<D<0.5}\\ \frac{V_{dc}T_{sw}}{16L}\cdot(-3+10D-8D^2)+\frac{V_{dc}T_{sw}}{4L}\cdot(1-D) & \text{0.5<D<0.75}\\ \frac{V_{dc}T_{sw}}{8L}\cdot(-3+7D-4D^2)+\frac{V_{dc}T_{sw}}{4L}\cdot(1-D) & \text{0.75<D<1}\end{cases} \tag{7-6}$$

The first item in the expression is the CM current ripple, which determines the output ripple. The second item is the DM current ripple. For two-phase N-type interleaving case, the total output current ripple is two times of the common mode current ripple, which can be expressed as:

$$\Delta I_{all\_N}=\begin{cases}\frac{V_{dc}T_{sw}}{4L}\cdot(D-4D^2) & \text{D<0.25}\\ \frac{V_{dc}T_{sw}}{8L}\cdot(-1+6D-8D^2) & \text{0.25<D<0.5}\\ \frac{V_{dc}T_{sw}}{8L}\cdot(-3+10D-8D^2) & \text{0.5<D<0.75}\\ \frac{V_{dc}T_{sw}}{4L}\cdot(-3+7D-4D^2) & \text{0.75<D<1}\end{cases} \tag{7-7}$$

The maximum inductor current ripple and output current ripple for the N-type interleaving is

$$\begin{aligned}\Delta I_{L\_\max\_N}&=\frac{V_{dc}T_{sw}}{8L}\\ \Delta I_{all\_\max\_N}&=\frac{V_{dc}T_{sw}}{64L}\end{aligned} \tag{7-8}$$

The analytical expression of the inductor current ripple and output current ripple for the Z-type interleaving case can also be derived based on the equivalent circuit in Fig.7.4 and the current waveform in Fig.7.5(b). The inductor current ripple expression is:

$$\Delta I_{L\_Z}=\begin{cases}\frac{V_{dc}T_{sw}}{8L}\cdot(D-4D^2)+\frac{V_{dc}T_{sw}}{4L}\cdot D & \text{D<0.25}\\ \frac{V_{dc}T_{sw}}{16L}\cdot(-1+6D-8D^2)+\frac{V_{dc}T_{sw}}{16L} & \text{0.25<D<0.5}\\ \frac{V_{dc}T_{sw}}{16L}\cdot(-3+10D-8D^2)+\frac{V_{dc}T_{sw}}{16L} & \text{0.5<D<0.75}\\ \frac{V_{dc}T_{sw}}{8L}\cdot(-3+7D-4D^2)+\frac{V_{dc}T_{sw}}{4L}\cdot(1-D) & \text{0.75<D<1}\end{cases} \tag{7-9}$$

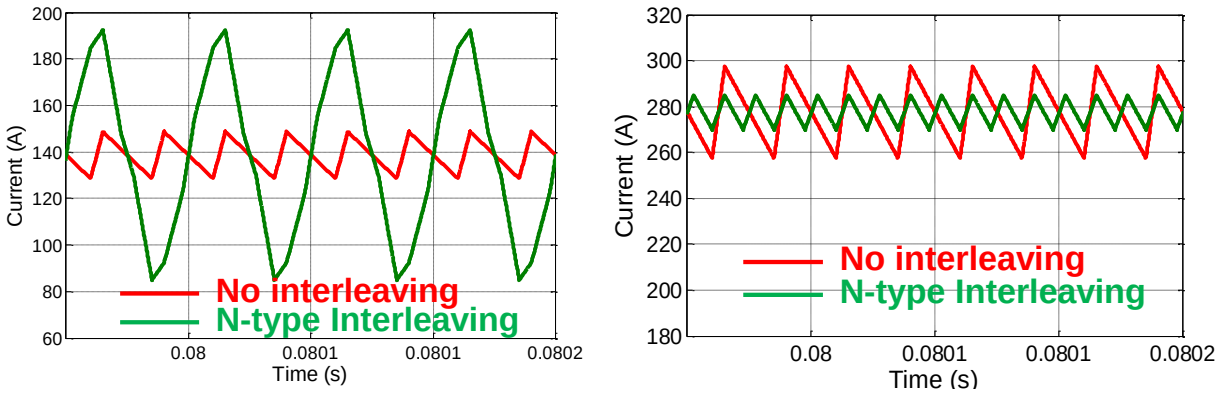
The total output current ripple for Z type interleaving is the same as the N-type interleaving case in 7-7. The maximal inductor current ripple is given by

$$\Delta I_{L\_\max\_Z}=\frac{9V_{dc}T_{sw}}{128L} \tag{7-10}$$

Comparing the inductor current ripple expression in 7-6 for N type interleaving and the same expression in 7-9 for Z type interleaving, it can be determined that the common mode current component for the two interleaving cases keep the same while the differential mode current component is slightly different for the two modes. This statement can also be verified by comparing the CM and DM current waveform in Fig.7.5. The analytical expression for the

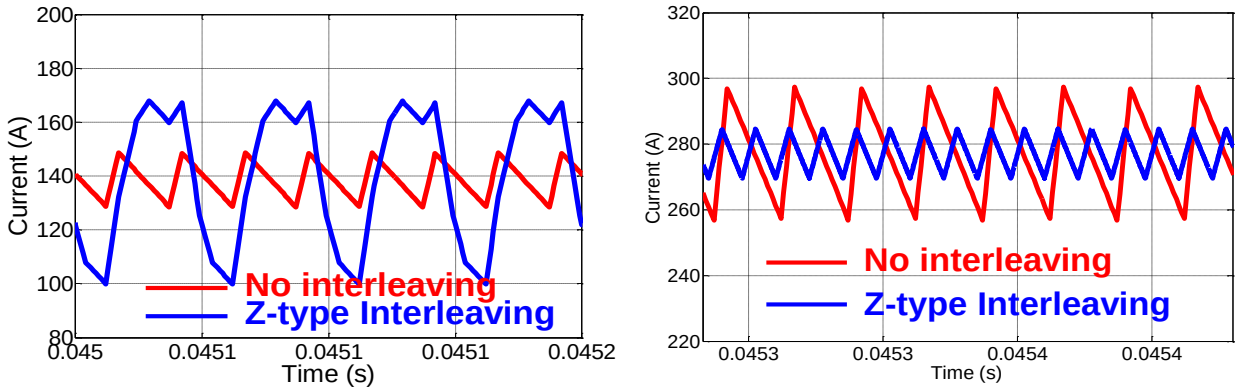
maximum inductor current ripple and the output current ripple in 7-4, 7-8 and 7-10 also shows that the two interleaving cases have larger inductor current ripple than the non-interleaving case due to the differential mode current that circulates within the two phase legs. But the output current ripple for the two interleaving cases is lower than the non-interleaving case due to the ripple cancellation effect by interleaving.

The inductor current ripple and output current ripple waveform is simulated for verification. The waveforms are compared for the interleaving and non-interleaving cases to investigate the influence of interleaving modes on the current ripple. The simulation is conducted based on the rated parameters of the 2-phase 3-lelvel converter as shown in Fig.7.1. The total power is 200kW and the DC link voltage is 1200V. The switching frequency is 20kHz and the duty cycle for all cases is 0.6. The inductance for each inductor is 60μH and the output capacitance is 180μF. The inductor current for the non-interleaving and N-type interleave case is compared in Fig.7.6(a). The output current waveform is compared in Fig.7.6(b). The same comparison between the non-interleaving and Z-type interleaving for the inductor and output current is given in Fig.7.7(a) and (b). The waveforms clearly verify that the interleaved phase leg has larger inductor current ripple due to the circulating current within the phase legs, regardless of the interleaving modes. But the interleaved phase leg has a reduced output current ripple due to the ripple cancellation effect.



(a) Inductor current waveform (b) Output current waveform

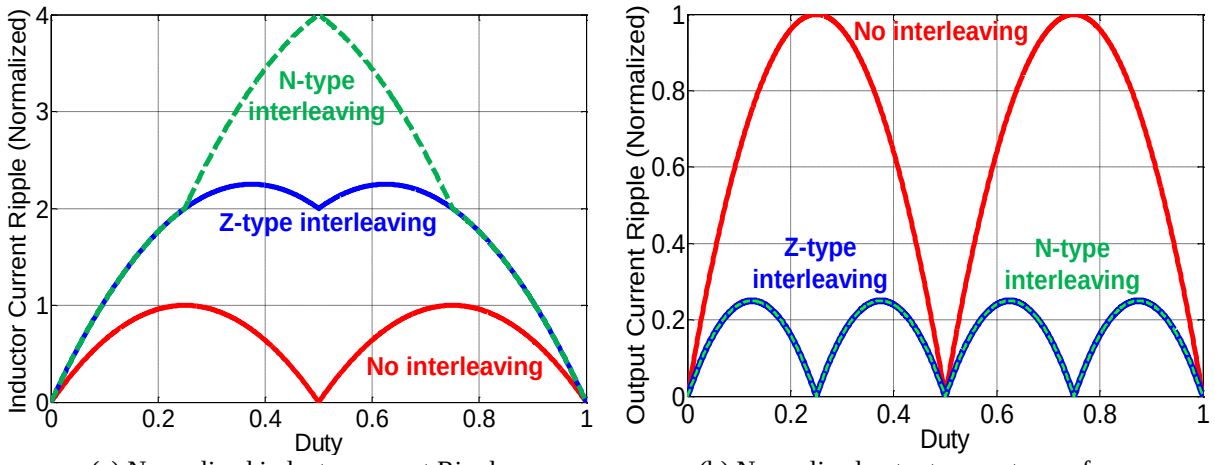
Fig. 7.6. Inductor and output current for N-type interleaving and non-interleaving



(a) Inductor current waveform (b) Output current waveform

Fig. 7.7. Inductor and output current for Z-type interleaving and non-interleaving

The analytical expression of the inductor and output current ripple [13], [14] can also be used to compare the current ripple with different operating modes in the whole duty cycle range. The result is given in Fig.7.8. The current ripple is normalized to the maximum current ripple for the non-interleaving case. The inductor current ripple in Fig.7.8(a) shows the non-interleaving case has the lowest ripple while the N-type interleaving has the highest current ripple when D=0.5. The Z-type interleaving case has the same ripple as the N-type interleaving when the duty cycle is smaller than 0.25 or larger then 0.75. For the output current ripple in Fig.7.8(b), the two interleaving modes have the same output ripple and it is much lower than the non-interleaved case. This result also verifies the conclusion for the current ripple at different interleaving modes.



(a) Normalized inductor current Ripple (b) Normalized output current waveform

Fig. 7.8. Current ripple with duty cycle for different operating modes

7.2 Interleaved 3-level DC/DC Chopper with Coupled Inductor

As mentioned earlier, the interleaving of the 3-level phase legs results in an increased inductor current ripple due to the circulating current. To reduce the circulating current, the inverse-coupled inductors which is commonly used for the 2-level interleaved converter can be adopted for the 3-lelvel interleaved DC/DC chopper stage. The inverse coupled inductor presents high impedance on the circulating current path and thus suppresses the circulating current. The circuit topology of an interleaved 3-level DC/DC chopper is shown in Fig.7.9. The phase leg structure keeps the same as the non-coupled case in Fig.7.1. But the coupled inductors are added to the upper two output terminals and the lower two output terminals. A1 and B1 in the figure has an inverse coupled inductor and it is the same case for A2 and B2. For analysis simplicity, the coupled inductor is separated into two parts. For phase leg A, it contains a non-coupled self-inductor La and an ideally coupled inductor M.

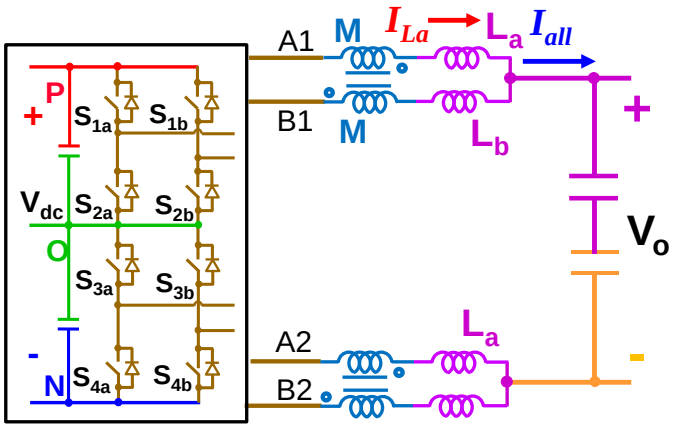


Fig. 7.9. Interleaved 3-level DC/DC chopper with coupled inductor

The same equivalent circuit as the one in Fig.7.4 for inductor current ripple derivation is shown in Fig.7.10. The circuit can still be divided into the common mode part and differential mode part. The inverse-coupled inductor doesn't influenced the CM part and only appears in the DM part to suppress the circulating current. With the equivalent circuit, the inductor and output current ripple for the N-type and Z-type interleaving with coupled inductor can also be derives as

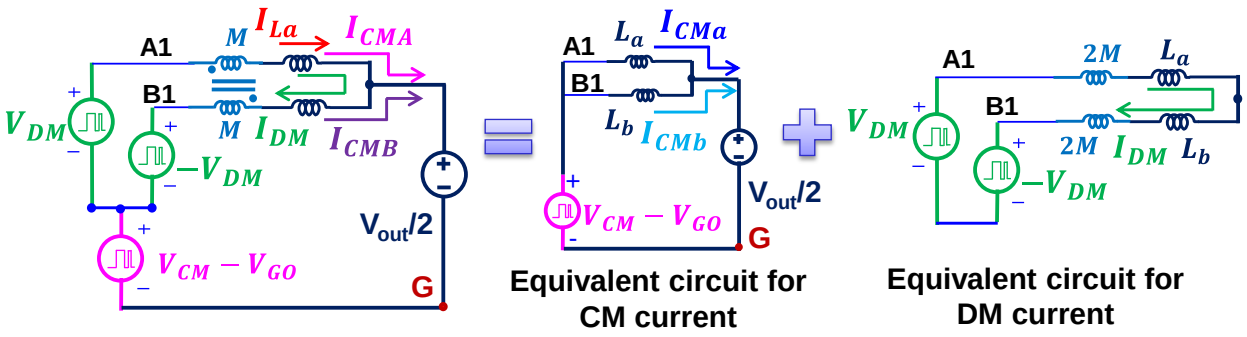
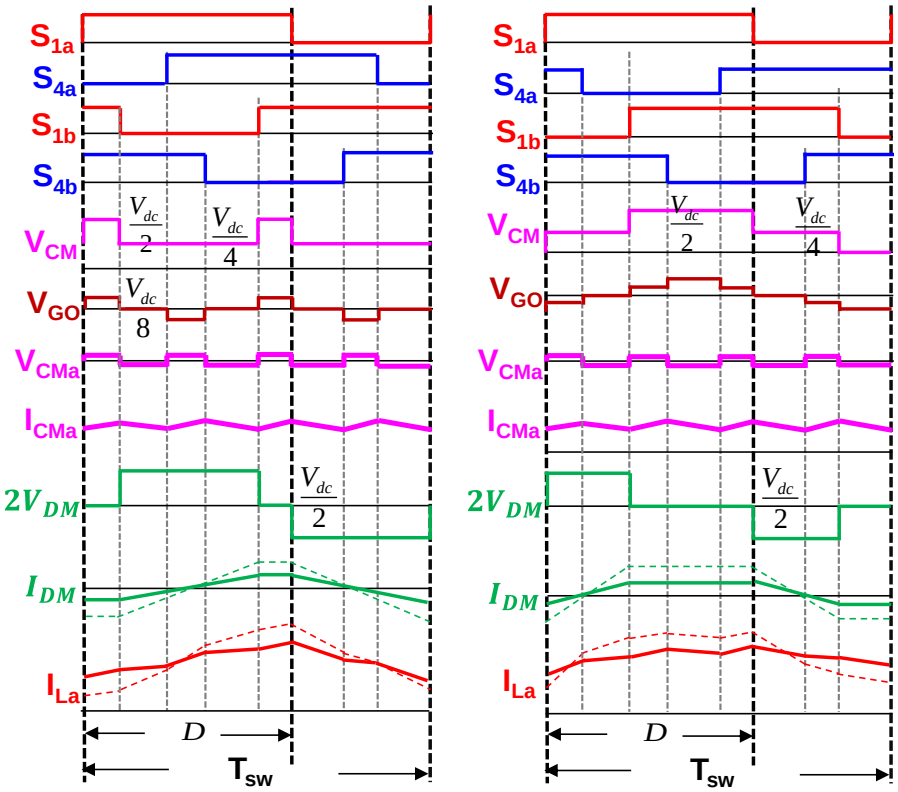


Fig. 7.10. Equivalent circuit for interleaved 3-level phase leg with coupled inductor

in Fig.7.5. The waveform of the coupled case is given in Fig.7.11 [13], [14]. The only difference between Fig.7.5 without coupled inductor and Fig.7.11 with coupled inductor is the DM current. The dashed lines in Fig.7.11 show the same waveforms without coupled inductor as comparison. The coupled inductor limits the circulating current and therefore reduces the inductor current ripple for both the N-type and Z-type interleaving. The common mode voltage and current for the 2 interleaving cases are not influenced by the coupled inductor.



(a) N-type interleaving (b) Z-type interleaving

Fig. 7.11. Inductor current for 2 interleaving modes with coupled inductor

7.2.1 N-type Interleaving with Coupled Inductor

Based on the equivalent circuit and the inductor current waveform, the analytical expression of the inductor current ripple for the two interleaving cases with coupled inductor can be derived. The inductor current ripple of N-type interleaving with coupled inductors is derived as [13], [14]:

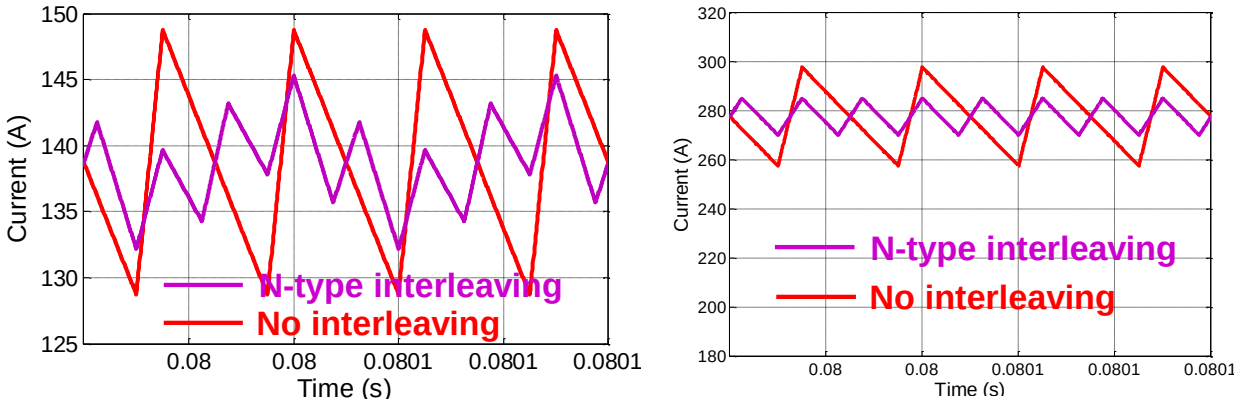
$$\Delta I_{L\_N\_cp}=\begin{cases}\dfrac{V_{dc}T_{sw}}{8L}\cdot(D-4D^2)+\dfrac{V_{dc}T_{sw}}{4(L+2M)}\cdot D & \text{D<0.25}\\ \dfrac{V_{dc}T_{sw}}{16L}\cdot(-1+6D-8D^2)+\dfrac{V_{dc}T_{sw}}{4(L+2M)}\cdot D & \text{0.25<D<0.5}\\ \dfrac{V_{dc}T_{sw}}{16L}\cdot(-3+10D-8D^2)+\dfrac{V_{dc}T_{sw}}{4(L+2M)}(1-D) & \text{0.5<D<0.75}\\ \dfrac{V_{dc}T_{sw}}{8L}\cdot(-3+7D-4D^2)+\dfrac{V_{dc}T_{sw}}{4(L+2M)}\cdot(1-D) & \text{0.75<D<1}\end{cases} \tag{7-11}$$

It can be observed from the equation that the second term in the current ripple expression, which is the differential mode component, is influenced by the mutual inductance. The larger the mutual inductance is, the lower the inductor current ripple will be. This is a very straightforward concept when the inductor current ripple is analyzed from CM and DM current point of view. On the other hand, the coupled inductor doesn't influence the CM current component, which determines the output current. As a result, the output current ripple is not in relation with the mutual inductance. The analytical expression of the output current ripple with coupled inductor is the same as the non-coupled case for the N-type interleaving. The expression is given in 7-7. Then the maximum inductor current ripple for the N-type interleaving with coupled inductor can be derived as the following. The maximum output current ripple in this case is the same as the non-coupled case given in 7-8.

$$\Delta I_{L\_\max\_N\_cp}=\frac{V_{dc}T_{sw}}{16L}\cdot\frac{(-3L^2+4LM+4M^2)}{8(L+2M)^2}+\frac{V_{dc}T_{sw}}{32}\frac{(5L+6M)}{(L+2M)^2} \tag{7-12}$$

The N-type interleaving operation with coupled inductor case is also simulated. The circuit parameters keep the same as the non-coupled case. The mutual inductance for the coupled

inductance is 300μH and the leakage inductance is 60μH. The coupling coefficient is -0.83 in this case. The inductor current and output current waveforms for the N-type interleaving case with coupled inductor are compared in Fig.7.12. The output current waveform keeps the same as the non-coupled case since the coupling doesn't influence the output current. But the inductor current ripple for the interleaved case is reduced with coupled inductor and it is lower than the non-coupled case. It verifies the effect of the coupled inductor for circulating current reduction. The inductor current ripple with different duty cycle is calculated and normalized by the analytical expression in 7-11. Several mutual inductance values are compared together. The result in Fig.7.13 [13], [14] shows that the current ripple is largely reduced with coupled inductor. The result in Fig.7.8 for non-coupled case shows the N-type interleaving has 4 time larger ripple



(a) Inductor current waveform (b) Output current waveform

Fig. 7.12. Inductor and output current for N-type interleaving with coupled inductor

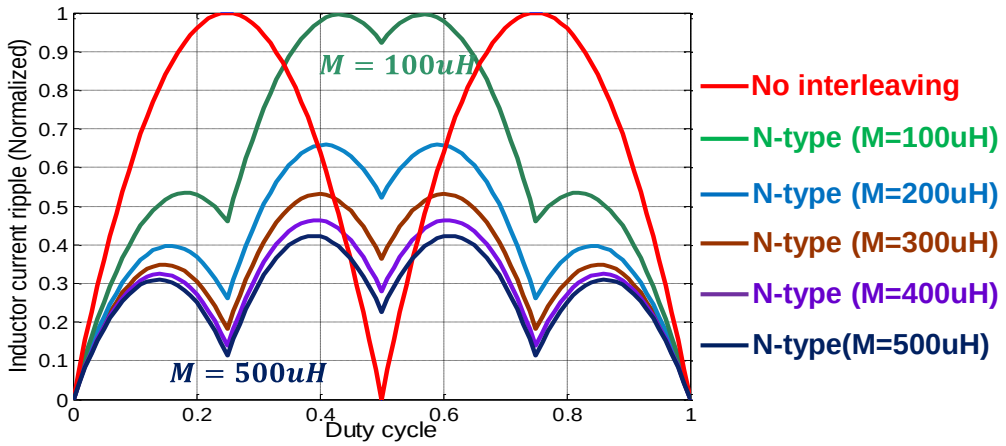
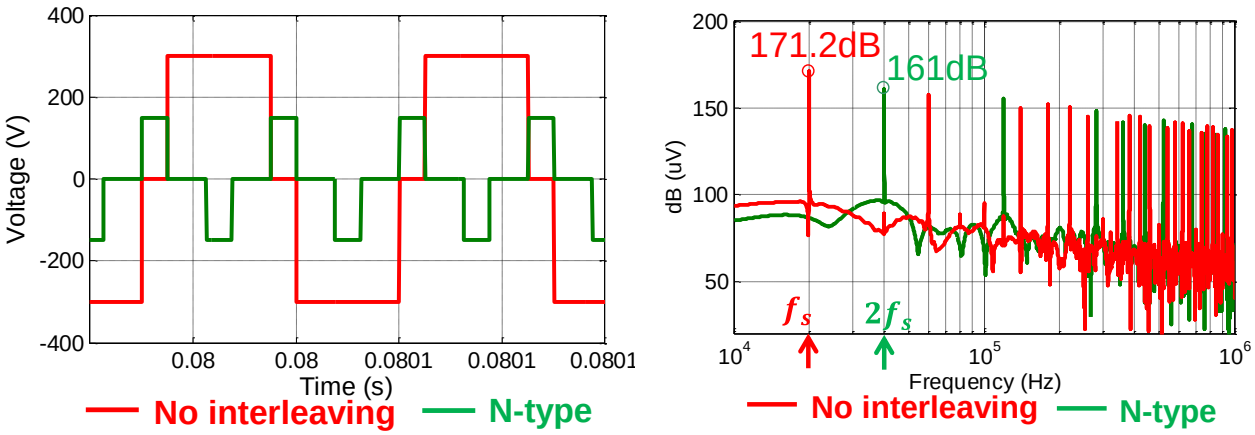


Fig. 7.13. Current ripple vs. duty cycle for N-type interleaving with coupled inductor

than the non-interleaving case. However, for the coupled case, the inductor current ripple for the N-type interleaving with 300μH mutual inductance is only half of the non-interleaving case. The result also verifies that larger mutual inductance gives lower inductor current ripple. The output current ripple for the coupled case follows the same pattern as in Fig.7.8(b).

Besides the inductor current ripple concern, the voltage between neutral point O and mid-point of the DC output cap G should be considered because this voltage V_{GO} is the common mode voltage which influences the EMI spectrum. The CM voltage waveform and spectrum for the N-type interleaving with coupled inductor and the non-interleaving case is compared in Fig.7.14. The voltage waveform in Fig.7.14(a) shows the N-interleaving case has lower CM voltage amplitude and higher voltage frequency than the non-interleaving case. The spectrum in Fig.7.14(b) clearly shows that the amplitude of the CM noise for N-type interleaving is reduced by 10dB compared with the non-interleaving case. The first peak of the CM noise of the N-type interleaving is also pushed to two times of the switching frequency. As a result, the corner frequency of the CM noise filter is increased and the size for the filter will be reduced. This result shows that the N-type interleaving is beneficial from the EMI point of view. This result is not influenced by the coupled inductor since the coupling does not influence the CM component.



(a) CM voltage waveform (b) CM voltage spectrum

Fig. 7.14. CM voltage waveform and spectrum for N-type interleaving

7.2.2 Z-type Interleaving with Coupled Inductor

The same in-depth analysis for the Z-type interleaving with coupled inductor is given in this part. The analytical expression for the inductor current ripple can be derived by the equivalent circuit and the current waveform in Fig.7.11(b). The inductor current ripple expression is [13]:

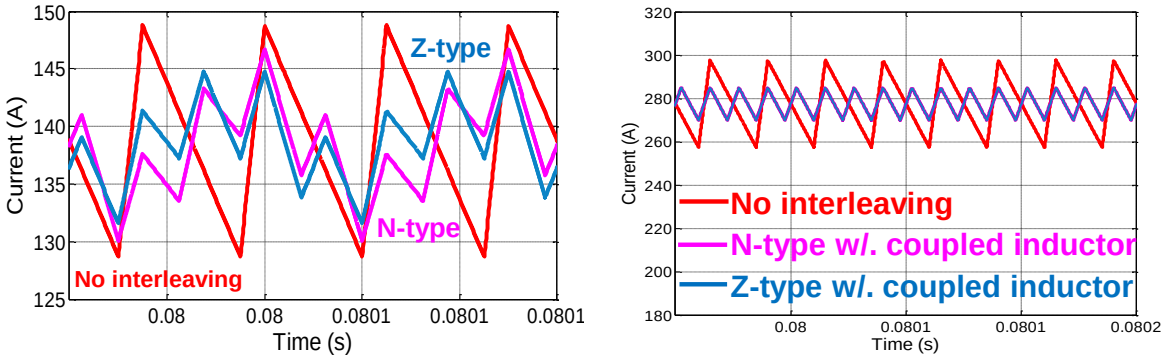
$$\Delta I_{L\_Z\_cp}=\begin{cases}\dfrac{V_{dc}T_{sw}}{8L}\cdot(D-4D^2)+\dfrac{V_{dc}T_{sw}}{4(L+2M)}\cdot D & \text{D<0.25}\\ \dfrac{V_{dc}T_{sw}}{16L}\cdot(-1+6D-8D^2)+\dfrac{V_{dc}T_{sw}}{16(L+2M)} & \text{0.25<D<0.5}\\ \dfrac{V_{dc}T_{sw}}{16L}\cdot(-3+10D-8D^2)+\dfrac{V_{dc}T_{sw}}{16(L+2M)} & \text{0.5<D<0.75}\\ \dfrac{V_{dc}T_{sw}}{8L}\cdot(-3+7D-4D^2)+\dfrac{V_{dc}T_{sw}}{4(L+2M)}\cdot(1-D) & \text{0.75<D<1}\end{cases} \tag{7-13}$$

The maximum inductor current ripple expression can then be derived as:

$$\Delta I_{L\_\max\_Z\_cp}=\frac{V_{dc}T_{sw}}{128L}\cdot+\frac{V_{dc}T_{sw}}{16(L+2M)} \tag{7-14}$$

The expression in 7-12 and 7-14 shows that the Z-type interleaving has smaller maximum inductor current ripple. The inductor current and output current waveform for the N-type, Z-type interleaving and non-interleaving case with coupled inductor is simulated in the same condition. The result is shown in Fig.7.15. It verifies that the two interleaving cases with coupled inductor has lower inductor current ripple than the non-interleaving case. The Z-type interleaving has

slightly lower inductor current ripple than the N-type. The output current ripple for N-type and Z-type with coupled inductor is the same and it is lower than the non-interleaving case.



(a) Inductor current waveform (b) Output current waveform

Fig. 7.15. Inductor and output current with coupled inductor

The inductor current ripple in different duty cycle is also compared for the three interleaving modes with coupled inductor. The mutual inductance is also taken into consideration and the current is normalized to the non-interleaving case. The result in Fig.7.16 [13], [14] also verifies that the Z-type interleaving has lower inductor current ripple than N-type with the same mutual inductance for the coupled inductor.

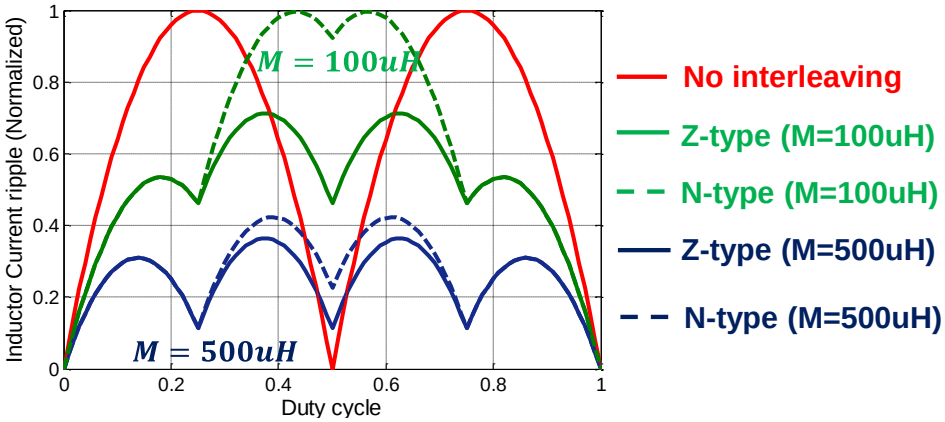
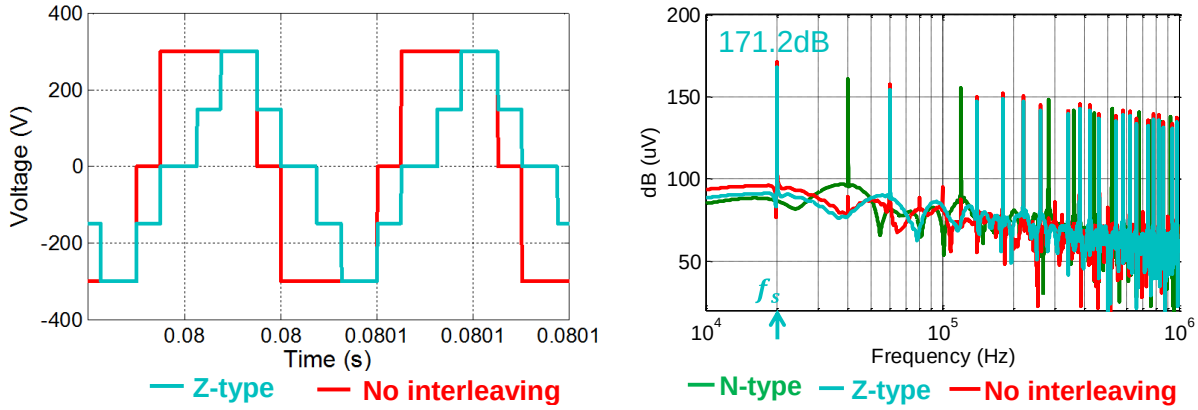


Fig. 7.16. Inductor current ripple vs. duty cycle with coupled inductor

The CM voltage waveform and spectrum for all three interleaving modes is also compared in Fig.7.17. The z-type interleaving has the same CM voltage amplitude as the non-interleaving case as shown in Fig.7.17(a). The first peak of the CM spectrum for Z-type interleaving locates

at the switching frequency. The magnitude for this peak is the same as the non-interleaving case, which is 10dB higher than the N-type. The result shows that the N-type is better for CM noise.



(a) CM voltage waveform (b) CM voltage spectrum

Fig. 7.17. CM voltage waveform and spectrum for all interleaving modes

7.2.3 Comparison and Conclusion

Finally, a brief comparison between the three interleaving modes is given. For the operation modes without coupled inductor, the two interleaved cases have the same output current ripple which is lower than the non-interleaving case due to the ripple cancellation effect. However, the interleaving results in circulating current in the phase legs and the inductor current ripple for the interleaving cases is higher than the non-interleaving case. The N-type interleaving has higher inductor current ripple than the Z-type when the duty cycle is between 0.25-0.75. To reduce the circulating current and inductor current ripple, coupled inductor is used for interleaving. With the coupled inductor, the inductor current ripple is reduced to be lower than the non-interleaving case. The Z-type interleaving still has lower inductor current ripple than the N-type interleaving with coupled inductor. The output current ripple is not influenced by adding the coupled inductor. The common mode voltage spectrum is also compared and the N-type interleaving is advantageous from the CM noise point of view. Its CM voltage peak is lower than the other two modes and the peak frequency is twice higher than the other two cases. A detailed comparison of

the current ripple and CM voltage for the three modes is given in Table 7.2. It shows that N-type interleaving has the best performance and it is thus used for the 2-phase 3-level DC/Dc chopper.

Table 7.2. Comparison between three interleaving modes

	Mutual Inductance	Inductor Current Ripple	Output Current Ripple	CM voltage amplitude & freq.
Non-interleaving	N/A	ΔI_L	ΔI_{all}	$0.25V_{dc}$ @f_{sw}
N-type	M	$<\Delta I_L$	$<0.25\Delta I_{all}$	$0.125V_{dc}$ @$2f_{sw}$
Z-type	M	< N-type	$<0.25\Delta I_{all}$	$0.25V_{dc}$ @f_{sw}

7.3 Integrated Coupled Inductor for the Interleaved DC/DC Chopper

7.3.1 Conventional Coupled Inductor Design

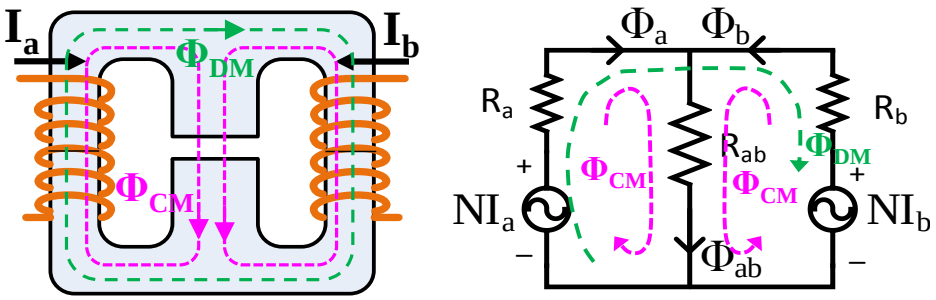
The design and implementation for the coupled inductor for the 3-level chopper is then discussed. The analysis for this coupled inductor is not quite the same as for the 2-level converter since the voltage and current waveform is complicated and the inductor current is influenced by both the common mode and differential mode voltage. The coupled inductor for the upper output A1 and B1 is introduced to illustrate the design procedure. The other one for the lower output is exactly the same. As analyzed previously, the inductor current has both CM and DM component. The equivalent circuit in Fig.7.10 reveals that the CM current for each phase leg I_{CM} is just half of the output current I_{all}. This current is only related to the leakage inductance L. The DM current within the two legs is influenced by the mutual inductance M and larger M gives lower DM current. The flux in the coupled inductor can be therefore analyzed in the same manner.

The structure of a conventional inverse coupled inductor is like the one in Fig.7.18(a). Its magnetic circuit model is in Fig.7.18(b). The flux direction is labeled in the figures. The CM flux flows from the outer leg to the center leg. Fig.7.11(a) shows that the CM current is a DC current with small ripple. So the CM flux is a DC flux with a small AC flux swing. The DM flux only appears in the outer legs. Fig.7.11(a) shows the DM voltage is in rectangular shape with dead

time. The width of the rectangular wave is *DT* (when $D \leqslant 0.5$) or *(1-D)T* (when $D>0.5$). So the DM flux can be calculated by the voltage-second product of the DM voltage. With this analysis, the CM and DM flux in the center leg and outer leg of the core can be calculated as [15]:

$$\Phi_a = \Phi_b = \Phi_{CM} \pm \Phi_{DM} = \frac{NI_{all}}{2(2R_{ab}+R_b)} \pm \frac{\int_0^{T_{sw}} v_{DM}\,dt}{2N}$$
$$\Phi_{ab} = 2\Phi_{CM} = \frac{NI_{all}}{(2R_{ab}+R_b)} \tag{7-15}$$

Here *N* is the turn number on each core. R_a is the reluctance in the outer leg and R_{ab} is the reluctance of the center leg, which should be large enough so that the core won't be saturated. The outer leg has two parts of flux. The CM flux is a DC term with a small AC ripple at four times of the switching frequency; the DM flux is a large AC term at the switching frequency.



(a) Coupled inductor structure (b) Equivalent magnetic circuit model

Fig. 7.18. Conventional coupled inductor and its magnetic circuit model

7.3.2 Integrated Coupled Inductor for High Power Density

The 3-level 2 phase interleaved DC/DC chopper in Fig.7.9 requires two of the inverse coupled inductors in Fig.7.18(a). In order to further reduce the component size and to increase the power density, a novel design is proposed to integrate the two coupled inductors into one. The equivalent circuit of the DC/DC chopper with the integrated coupled inductor is given in Fig.7.19 [15]. The chopper stage is represented by four voltage sources. In this circuit, the leakage inductance of the top and bottom part coupled inductors are coupled together. This is a positive coupling that increases the output inductance for the interleaves power stage. Previous

analysis shows the output current ripple is determined by the leakage inductance. As a result, the positive coupling reduces the output current ripple. The integrated coupled inductor suppresses the circulating current and increases the output inductance simultaneously. Only one inductor is needed for the four output terminals of the 2 phase legs and hence increases the power density.

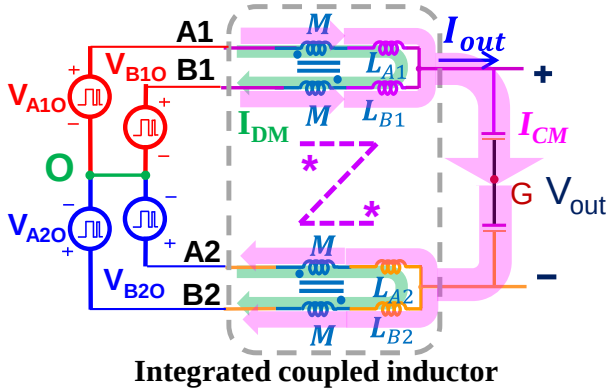


Fig. 7.19. Interleaved DC/DC chopper with integrated coupled inductor

The voltage and current waveforms of the interleaved phase leg with the integrated coupled inductor is analyzed in common mode and differential mode. The voltage and current waveforms are given in Fig.7.20. Here V_{A1} is the voltage between phase terminal A1 and positive output terminal of the power stage. Similarly, V_{A2} is the voltage between A2 and positive output. The common mode and differential mode voltage and current can be expressed as follow:

$$V_{CM\_AB} = \frac{V_{A1} + V_{A2}}{2}, \quad V_{DM\_AB} = \frac{V_{A1} - V_{A2}}{2} \tag{7-16}$$

$$I_{CM\_AB} = \frac{I_{LA1} + I_{LB1}}{2}, \quad I_{DM\_AB} = \frac{I_{LA1} - I_{LB1}}{2} \tag{7-17}$$

It is very straightforward that the CM current is the output current and the DM current is the circulating current. The inductor current waveform is the summation of the CM and DM current. The inductor current waveform in Fig.7.20 contains two components. One is the CM current with large DC bias and small ripple at four times of switching frequency. The other one is the DM current envelope with larger ripple amplitude at the switching frequency.

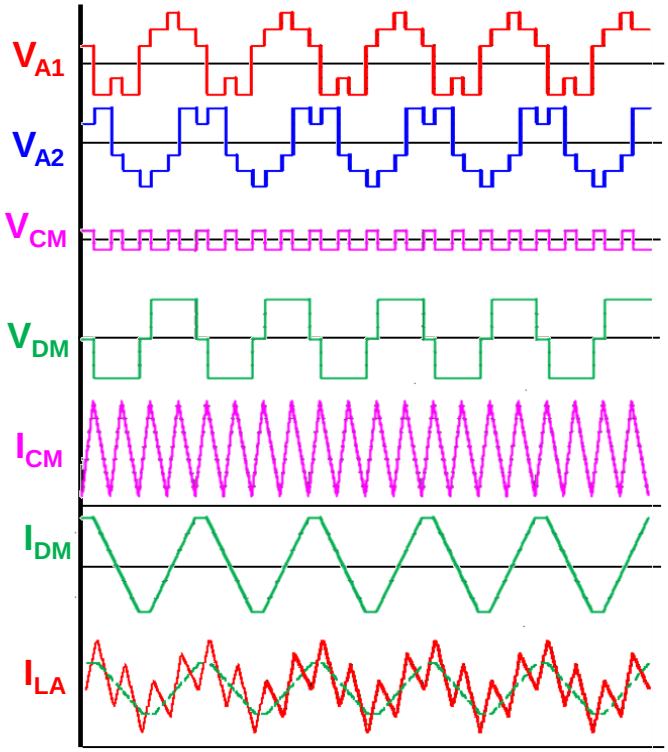


Fig. 7.20. CM and DM voltage and current waveform with coupled inductor

The conceptual structure for the integrated coupled inductor is shown in Fig.7.21. The two legs on the left are used for the upper terminals A1 and B1. The other two legs are connected to the lower terminals A2 and B2. The left two legs and right two legs can be magnetically linked together through an intermediate leg that provides extra flux path. This intermediate leg also contains air gap to produce leakage inductance for the output current. This inductor structure includes both negative coupling for the original two coupled inductors and also positive coupling for the output inductance. There are four windings in total and the winding polarities should be considered carefully to achieve the desired coupling effect. The winding structure and current direction is illustrated in Fig.7.21 as well. With the given current direction, the winding polarity between A1 and B1 should be opposite to achieve inverse coupling. It is the same case for A2 and B2. The winding polarity for A1 and A2 is the same to achieve a positive coupling. So does the winding polarities for B1 and B2.

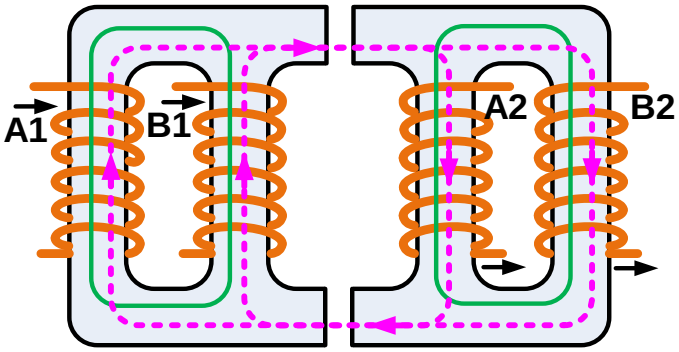


Fig. 7.21. Conceptual drawing of the integrated coupled inductor structure

With this configuration, the flux in the integrated coupled inductor contains two parts, one for the positive coupling and the other one for the negative coupling. The DM flux generated by circulating current is labeled by the solid line in Fig.7.21 and the CM flux generated by common mode current is labeled with dashed line in the same figure. The simplified magnetic equivalent circuit for the integrated coupled inductor is shown in Fig.7.22. The magnetic circuit is driven by four sources. The four magnetic voltage sources are excited by the current in each winding. The

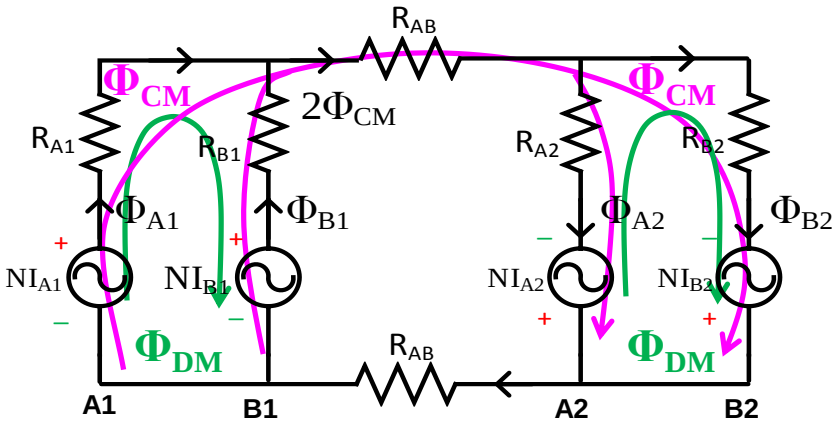


Fig. 7.22. Magnetic circuit model for the integrated coupled inductor

differential mode flux can be calculated by the DM current/voltage between winding A1 and B1 (or A2 and B2). The CM flux can be calculated in the same way as the conventional coupled inductor in 7.3.1. The differential-mode flux is [15]:

$$\Phi_{DM} = \frac{NI_{DM}}{R_a} = \begin{cases} \dfrac{V_{dc}T_{sw}D}{2N} & \text{D} \le 0.5 \\ \dfrac{V_{dc}T_{sw}(1-D)}{2N} & \text{D>0.5} \end{cases} \tag{7-18}$$

The CM current in each inductor leg is half of the output current, so the CM flux is calculated as

$$\Phi_{DM} = \frac{NI_{out}}{2(R_{AB}+R_{A1})} \approx \frac{NI_{out}}{4R_{AB}} \tag{7-19}$$

For the four legs of the converter, their flux contains both CM and DM part. So the total flux is

$$\Phi_i = \Phi_{CM} + \Phi_{DM} = \frac{NI_{out}}{2(R_{AB}+R_i)} \pm \frac{NI_{DM}}{R_i},\ i\text{=A1,A2,B1,B2} \tag{7-20}$$

The maximum flux density in each individual leg is given in 7-21, where N is the turn number and A_e is the core leg cross section area. M_{A1A2} is the mutual inductance between A1 and A2.

$$\left|B_{\max\_A}\right| = \frac{2M_{A1A2}I_{out}}{NA_e} + \frac{V_{dc}T_{sw}D}{4NA_e} = \left|B_{CM}\right| + \left|B_{DM}\right| \tag{7-21}$$

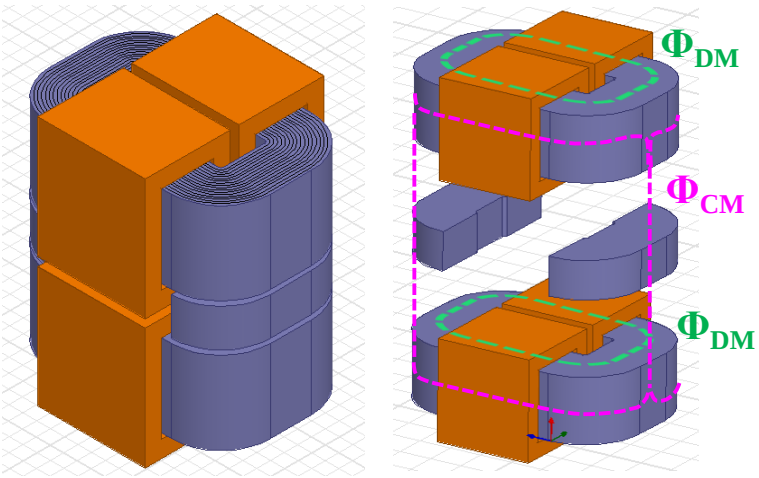
For the intermediate leg, its flux is twice of the CM flux. So the maximum flux density is

$$\left|B_{\max\_AB}\right| = \frac{NI_{out}}{(2R_{AB}+R_A)A_{\text{int}}} = \frac{4M_{A1A2}I_{out}}{NA_{\text{int}}} \tag{7-22}$$

After the flux analysis, the real implementation of the integrated coupled inductor is brought out for discussion. The most straightforward way to fabricate this inductor follows the structure given in Fig.7.21. The four legs of the core with their windings are arranged side by side. Each winding is connected to one output terminal of the converter phase leg. The two windings on the left are inversely coupled and so do the two windings on the right. The intermediate leg connects the left and right part together and creates the positive coupling. This leg has certain amount of air gap to prevent core saturation. This core structure is quite simple and can be implemented with ferrite core or laminated alloy core. But for some core materials which are produced in the form of tape-wound structure (e.g. amorphous magnetic alloy or nano-crystalline magnetic alloy), this paralleled core structure can't be used because the flux must flows in the direction of

the lamination layers. Although these materials can be built in the form of stacked blocks, they suffer from high manufacturing cost.

To use the tape-wound core and also to reduce the component size, another core structure for the integrated coupled inductor is introduced in Fig.7.23(a). Different from the planar structure in the above case, the new core has 3-dimension structure. Two legs and their windings are placed at the top while the other two are placed at the bottom. Each of them are constructed by a tape-wound C-C core. There are two magnetic blocks between the top and bottom part that serve as the intermediate legs and provide leakage flux path. The CM and DM flux path in the core is also illustrated in the exploded view of the inductor structure in Fig.7.23(b). On one hand, this is a very compact and highly integrated core structure for core size minimization. But on the other hand, the structure is really complicated and the flux has 3-dimensional distribution. There are several couplings between multiple windings, which influence both the mutual inductance and leakage inductance. The interleaved DC/DC chopper stage should have low inductor current ripple for switching loss reduction and also low output ripple for output capacitance reduction. The output current ripple is determined by the positive coupled inductance M_{AB}, which provides leakage inductance between the top and bottom part. The inductor current ripple is determined by the negative coupling between the two windings of the C-C core.



(a) Assembled structure (b) Exploded view

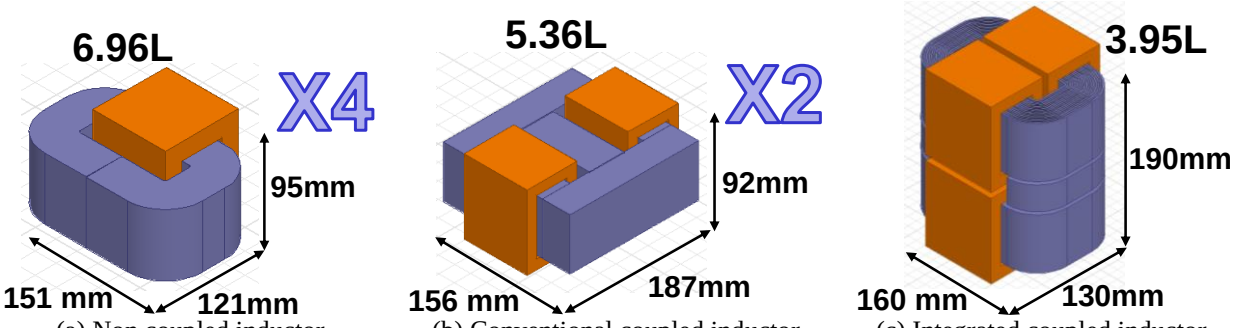
Fig. 7.23. Integrated coupled inductor structure with tape-wound core

There are several design considerations for the integrated coupled inductor. The maximum flux density in each individual leg and in the intermediate leg is given in 7-21 and 7-22 respectively. With the circuit parameters known, the saturation flux density can be determined with certain safety margin. The core loss density is also considered during the design process. The CM flux in this case is a biased flux with small ripple. This flux does not cause excessive core loss due to the small AC flux ripple. The DM flux on the contrary is an AC flux with switching frequency fluctuation. It induces considerable core loss and related heat. The core loss density design should take into account the DM flux loss and leave enough margin. To get enough inversely coupled mutual inductance between A1 and B1 (also A2 and B2), the turn number should meet certain criteria. Larger turn number shrinks the volume and weight of the core, as well as the core loss. But it increases the winding loss. The mutual inductance and power density should be considered together to have a reasonable trade-off.

Finally, the integrated coupled inductor is designed by following the above procedure and considerations. For the given parameters of the 200kW, 20kHz DC/DC chopper, the nano-crystalline material (e.g. FINEMET FT-3M) is used for the tape-wound C-core for the negative coupling. This core material has relatively good core loss density for the high ripple of DM flux.

Mega Flux material is chosen to build the intermediate leg because of the distributed air gap, high saturation and low cost for the high DC bias of the CM current. The mutual inductance for the positive coupled mutual inductance M_{A1B1} is 500μH and the leakage inductance L_{AB} is 60μH. The maximum flux density is designed at 75% of the saturation flux density with B_{CM}=0.608T and B_{DM}=0.292T.

The design for other operating modes and coupling structures is also carried out and they are compared together with the integrated coupled inductor. For the non-interleaved case with paralleled phase leg in Fig.7.1, four individual inductors are needed. Each inductor is 120μH to keep the inductor current ripple below 10A and output current ripple below 20A. The inductor is designed with amorphous core material (Metglas 2605SA1) and the dimensions are given in Fig.7.24(a). The total volume of the four inductors is 6.96L. With the conventional coupled inductor design using the same nano-crystalline core material as the integrated coupled inductor, two of them are needed. The dimensions for this design is shown in Fig.7.24(b). The total volume of the two coupled inductors is 5.36L. The dimensions of the integrated coupled inductor



(a) Non coupled inductor (b) Conventional coupled inductor (c) Integrated coupled inductor

Fig. 7.24. Comparison of size and volume of different inductor designs

is given in Fig.7.24(c) as comparison. The total volume of this design is 3.95L. The total volume of the conventional coupled inductor is 77% of the non-coupled design. As for the integrated coupled inductor, the volume is reduced to 57% of the non-coupled case [15]. This result verifies the size reduction brings by the integration of the coupled inductor.

7.4 Inductor Hardware and Experimental Verifications

7.4.1 Integrated Coupled Inductor Test

The integrated coupled inductor design is implemented in hardware and also tested on the 3-level interleaved DC/DC chopper. Fig7.25 shows the physical structure of the inductor hardware. The two C-C core uses nano-crystalline material and the intermediate legs use iron powder blocks. The windings of the inductor uses flat copper wire and leaves spaces for heat dissipation. There are totally eight terminals for the four windings and the terminals that connect to the phase leg output is labeled in the figure.

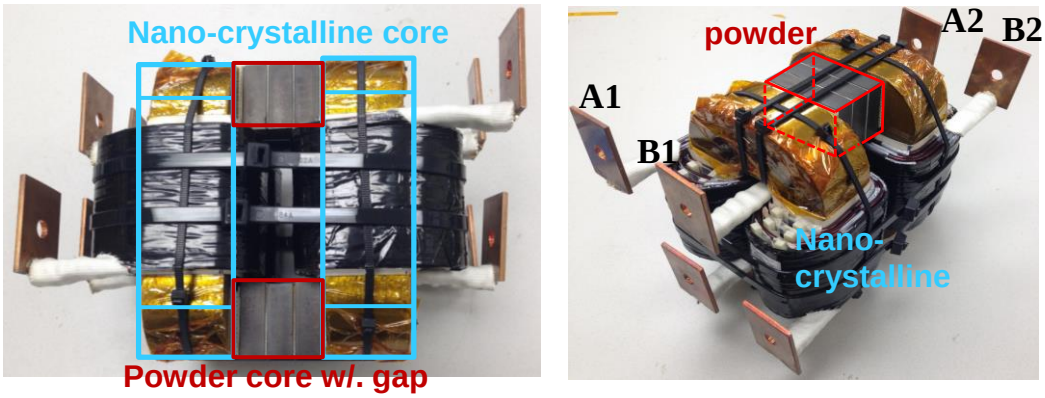
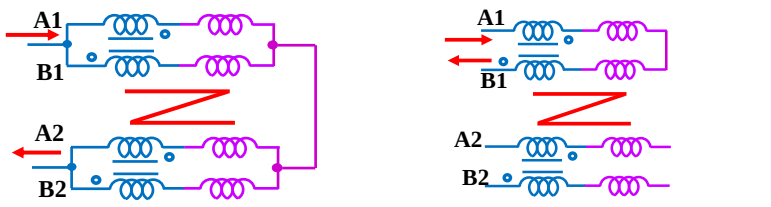


Fig. 7.25. Physical structure of the integrated coupled inductor

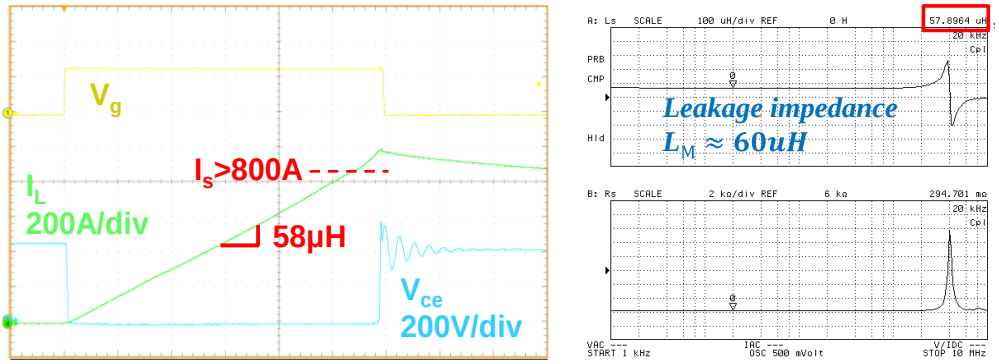
The different inductance of the coupled inductor is tested by both impedance analyzer and single pulse power test. The leakage inductance of the positive coupling is tested at first and the single pulse power test circuit is given in fig.7.26(a). The pulse width is set to charge the inductor current high enough for saturation test. The inductor current slope, the DC voltage and pulse width together can determine the large signal inductance. The single pulse test waveform is



(a) Leakage inductance test (b) Inverse coupled DM inductance test

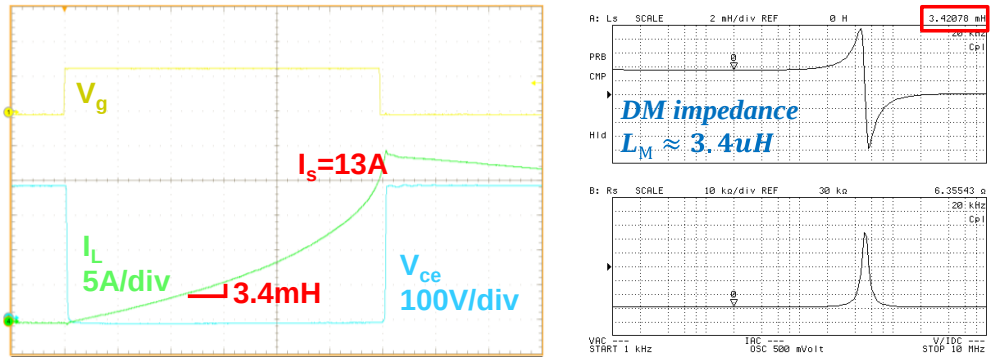
Fig. 7.26. Single pulse test configuration for inductance and saturation current

given in Fig.7.27(a). The result shows that the leakage inductance is around 60μH and the saturation current is about 800A. The small signal leakage inductance measured by the impedance analyzer is shown in Fig.7.27(b). The measured small signal inductance is also around 60μH. Then the inverse coupled inductance for the DM current is tested by the circuit in Fig.7.26(b), which ignores the self-inductance. The single pulse test result is given in Fig.7.28(a) and the small signal impedance measurement result is given in Fig.7.28(b). The result shows a 3.4mH inverse coupled inductance for DM current and 13A saturation current for DM ripple.



(a) Single pulse test (b) Impedance measurement result

Fig. 7.27. Leakage inductance test result



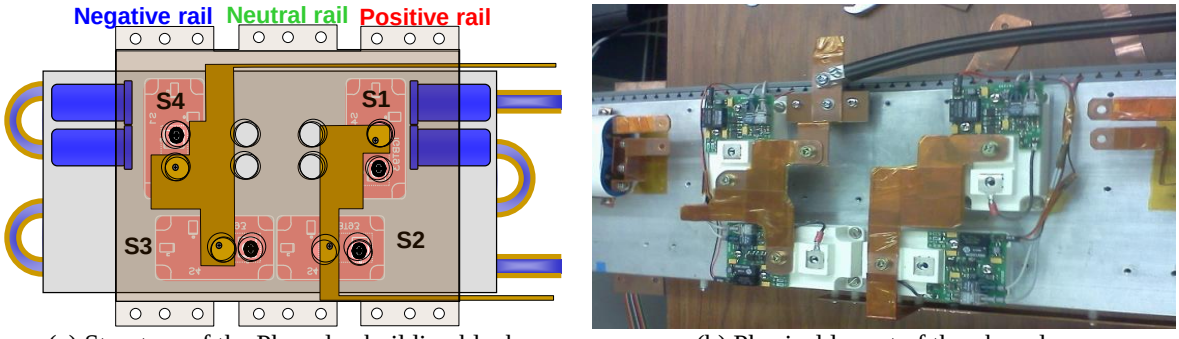
(a) Single pulse test (b) Impedance measurement result

Fig. 7.28. Inverse coupled DM inductance test result

7.4.2 DC/DC Chopper Power Stage and Control Loop Test

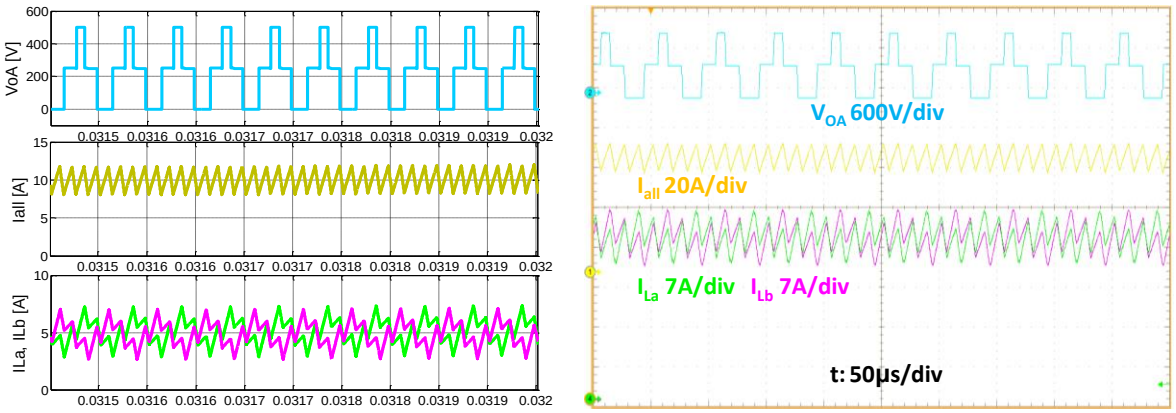
The phase leg building block for the DC/DC chopper stage is also fabricated based on the phase leg for the DC/AC part. The DC/DC part shares the similar layout and bus bar design as the DC/AC part. The structure and physical layout of the DC/DC phase leg is given in Fig.7.29.

Two of the phase leg building blocks are interleaved by the coupled inductor and other passive component and protection circuit to form the power stage of the DC/DC chopper. The system structure of the chopper hardware will be introduced later in chapter 8.2. The DC/DC chopper is tested at buck mode with a resistive load at the output and a 1000V DC source at the DC link. The two phase legs are modulated with N-type interleaving and the duty cycle for each phase leg is 0.42. The tested power for the whole system is around 20kW. The simulation result and experimental result for the N-type interleaving case with integrated coupled inductor is given in Fig.7.30(a) and (b) respectively. The result gives the output voltage for one phase leg V_{oA}, output current I_{all} and two inductor current I_{LA} and I_{LB}. For the N-type interleaving, the phase leg output voltage switches between zero and half V_{dc} when the D<0.25. When D>0.75, the output switches between half V_{dc} and V_{dc}. In these two cases, the output voltage is 2-level. When duty cycle is between 0.25 and 0.75, the phase output voltage switches between all the three levels as shown in the experimental result. The output current I_{all} has high DC component and small ripple at four times of switching frequency. The Inductor current I_{La} contains both CM and DM component.



(a) Structure of the Phase leg building block (b) Physical layout of the phase leg

Fig. 7.29. Chopper phase leg building block structure and layout

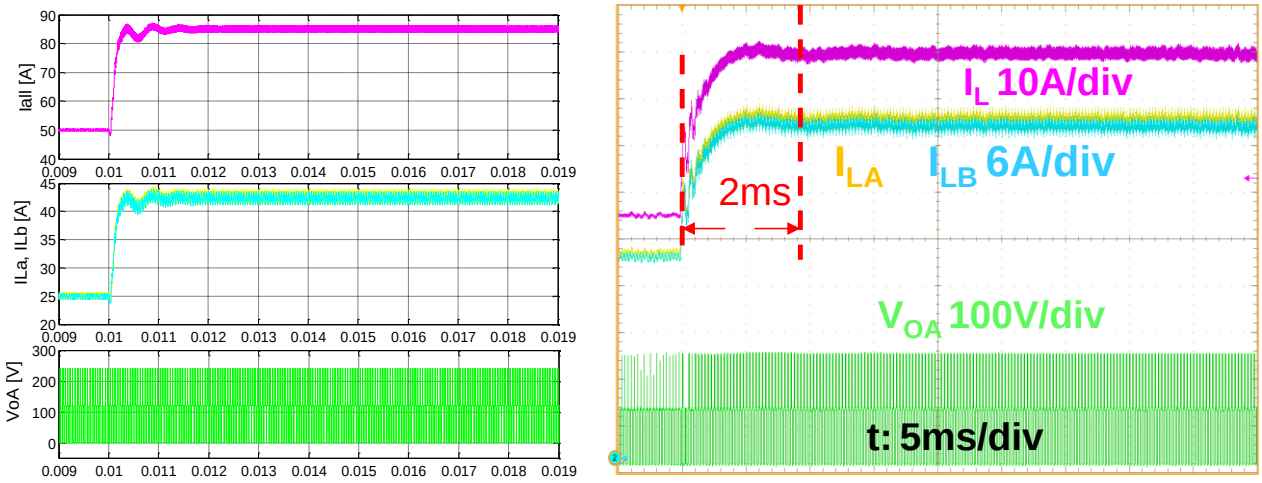


(a) Simulation result (b) Experimental result

Fig. 7.30. Simulation and experimental result for N-type interleaving

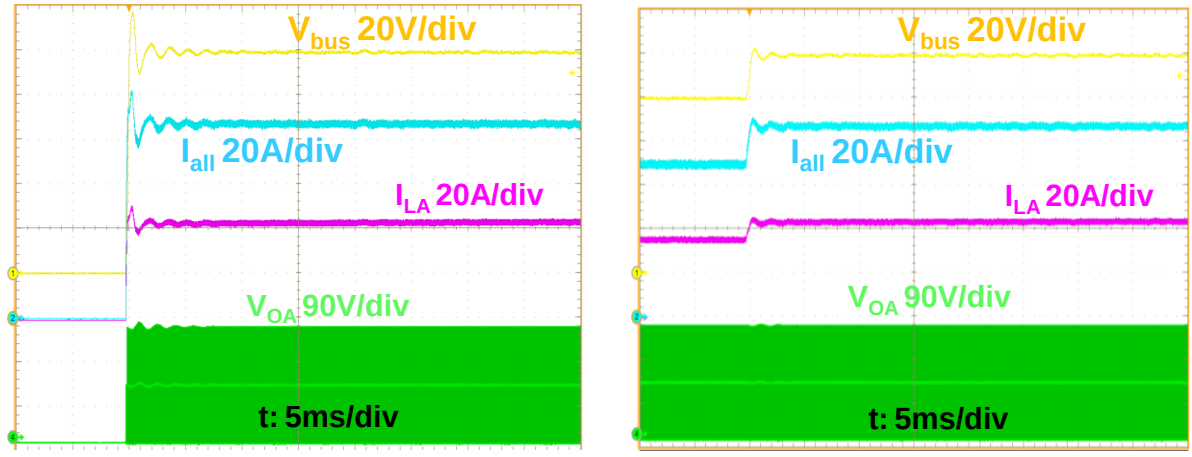
After the open loop power test for the DC/DC chopper, the closed loop compensators are designed for the current and voltage control. The DC/DC chopper controls the average value of its output current I_{all} as the inner loop for active power transfer between the AC bus and DC bus. It also regulates the DC bus voltage as outer loop which provides the current reference for the inner loop. The control block diagram for the DC/DC part is illustrated in Fig.6.6 when the system control algorithm is introduced. The control loop design for the DC/DC part follows the same procedure as the DC/AC part. The detailed average model and equivalent circuit for the DC/DC chopper is first derived considering the integrated coupled inductor. Then the current control loop is designed to compensate the open loop duty cycle to output current transfer function. After the current loop is closed, the voltage loop controller is designed based on the current loop transfer function. The compensated transfer function is from the current reference to the DC bus voltage. The compensator for the current loop uses a Type III controller with one integrator, one pole and two zeroes. The inner current loop has 50° phase margin at 1 kHz bandwidth. The voltage compensator uses traditional proportional integral (PI) controller with 500Hz bandwidth and 65° phase margin. The detailed design procedure is not covered in this part. The DC/DC chopper is also tested at a scaled-down rating with 1/5 of the rated value to keep the consistency for the controller parameters. The simulation and experimental result for the

current loop control is shown in Fig.7.31 to verify the design. A step change from half load to full load current is applied to the I_L reference at 0.01 second. The output current I_{all}, inductor current I_{La}, I_{Lb} and phase A output voltage V_{OA} is monitored in the simulation waveform in Fig.7.31(a) and experimental waveform in Fig.7.31(b). The output current has a fast and smooth step transient. The settling time is less than 2ms and no obvious overshoot or ringing is observed. The result verifies the performance of the current control loop. Then the performance of the voltage control loop is verified based on the closed-loop current control. The experimental result for the startup transient is shown in Fig.7.32(a) with DC bus voltage, output current, phase leg



(a) Simulation result (b) Experimental result

Fig. 7.31. Simulation and experimental result for current control loop



(a) Startup transient (b) Bus voltage reference change

Fig. 7.32. Experimental result for voltage control loop

current and voltage. The DC bus voltage has smooth transient and slight overshoot before it reaches steady state. The output current has a similar step transient response as the bus voltage. A step change of the DC bus voltage reference is also applied and the experimental result is given in Fig.7.32(b). The bus voltage rises from 0.8 of rated value to rated value. The overshoot is small and settling time is very short. The experimental result verifies the control loop design for the voltage and current control of the DC/DC chopper.

The loss and thermal performance for the coupled inductor and the power stage is also verified. The estimated core loss for the coupled inductor is around 41W and the winding loss is around 104W at full load condition. The power stage loss for the DC/DC chopper at different load conditions is also calculated by the loss model introduced in chapter 2. The system loss breakdown for the chopper stage is given in fig.7.33. The interleaved phase leg has over 98.8% efficiency at full load condition. The result shows that the turn off loss still dominates the total loss though the interleaved phase leg and coupled inductor is used to reduce the current ripple.

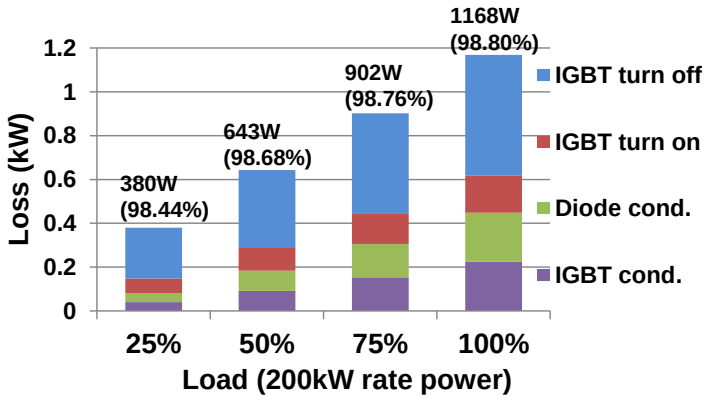


Fig. 7.33. Total system loss breakdown for the DC/DC chopper

7.5 Summary and Conclusion

In this chapter, the power stage of the 3-level bidirectional DC/DC chopper is studied in detail. The 3 different operating modes for the 2-phase 3-level chopper is presented at first. The equivalent circuit for current ripple analysis is divided into the common mode and differential

mode for derivation simplicity. The CM and DM voltage, current and the inductor current waveform is illustrated for ripple analysis. The analytical expressions for the inductor current and output current ripple is derived for the non-interleaving, N-type interleaving and Z-type interleaving cases. The maximum inductor and output current ripple is also identified based on the analytical expression. The inductor and output current for the different operating modes is simulated and compared together. Also the inductor and output current ripple at different duty cycle cases is compared for all the operating modes. The result shows that the two interleaved cases have the same output current ripple, which is lower than the non-interleaving case due to the ripple cancellation effect. But they have higher inductor current ripple because of the circulating current within phase legs. The N-type interleaving has slightly higher inductor current ripple than the Z-type interleaving. Then the current ripple for the interleaved phase leg with coupled inductor is analyzed. The equivalent circuit shows that the coupling effect only exists in the differential mode current path for the circulating current. It does not influence the output current, which is the common mode current. The analytical expression for inductor current ripple is then derived for both N-type and Z-type interleaving. The simulation waveform compares the non-interleave case and interleaved case with coupled inductor. Both the analytical expression for maximum inductor current ripple and the simulation waveform verifies that the coupled inductor can reduce the inductor current ripple compared with the non-interleaving case. For the non-coupled case, the interleaved operation has high inductor current ripple than the non-interleaved operation. But with coupled inductor, the interleaved case has lower inductor current ripple than the non-interleaved case. The output current ripple is not changed for the coupled and non-coupled case. Besides the inductor current ripple, the common mode voltage is also considered and compared for the three operating modes. The CM noise spectrum shows the N-

type interleaving has lower noise peak and higher CM noise frequency than both the Z-type interleaving and non-interleaving case. As a result, the N-type interleaving is used for the 3-level chopper. Then the implementation for the coupled inductor is discussed. The core structure and equivalent magnetic circuit model is presented at first. Then the flux in each core is calculated. Based on the conventional coupled inductor structure, an integrated coupled inductor with lower volume and higher output inductance is proposed. The proposed inductor is based on a 3-dimensional core structure. It contains both negative coupling for the circulating DM current and positive coupling for the output CM current. The core structure and equivalent magnetic circuit model is also introduced. The flux in each core leg is also given. The design consideration and core material selection is discussed. Finally, the integrated coupled inductor is fabricated and tested with the 3-level DC/DC chopper. The experimental result verifies the integrated coupled inductor design and the analysis of the inductor current ripple for the interleaved phase leg. Also the current and voltage control loop is tested by the experimental result to verify the control loop design.

CHAPTER.8 SYSTEM HARDWARE STRUCTURE AND EXPERIMENTAL VERIFICATION

The hardware for the power stage and control system of the power conversion system is thoroughly introduced in this chapter. The DC/AC and DC/DC power stage is introduced separately, followed by the control system architecture and system experimental result.

8.1 Power Stage and Component Structure for DC/AC Part

The system structure of the DC/AC part for the power conversion system is given Fig.8.1. The system is constructed by the modularized phase leg building block, the harmonic and EMI filter, as well as the protection and auxiliary circuit. The inverter side inductor L1 and the grid side inductor L2 are both 3-phase coupled inductor. L1 uses amorphous core and L2 uses silicon-steel core. The inverter side inductor is introduced in detail in chapter 5.5. The pictures for these two inductors are given in Fig.8.2(a) and (b). The damping circuit structure is given in Fig.8.3(a). Compared with the LCL filter, the damping circuit has small size. Besides the harmonic filter, the common mode choke is also added in the power stage. Because of the 3-phase coupled structure, L1 and L2 don't have any common mode impedance. The common mode choke is necessary to provide some common mode impedance in the power stage. As shown in Fig.8.1, the common mode choke is connected in serial with the differential mode filter inductor L1 and L2. The toroidal core with nano-crystalline material is used for the choke. Five of the one-turn core is used to provide a total 100μH common mode impedance at 100kHz frequency. The structure of the common mode choke is shown in Fig.8.3(b). Due to the size and current rating limitation, this common mode choke has only 10A saturation current. A larger common mode

choke with hundreds amps of saturation current is put at the DC side, which will be covered later.

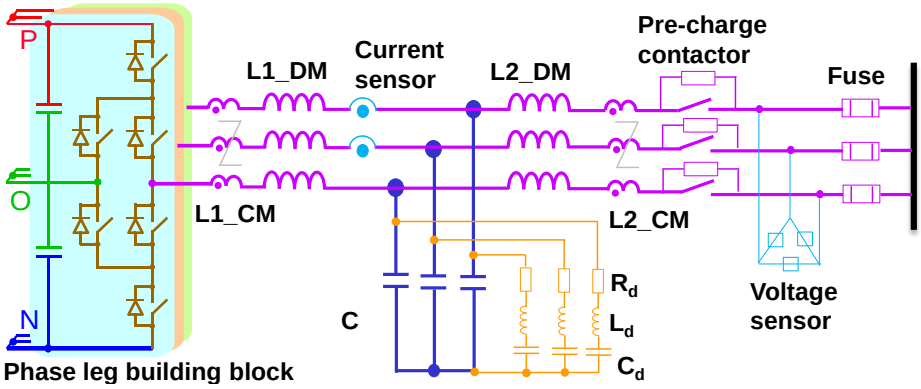


Fig. 8.1. System structure of the DC/AC part for the power conversion system

(a) Inverter side inductor L1 (b) Grid side inductor L2

Fig. 8.2. Inverter side and grid side inductor

(a) RLC damping circuit (b) Common mode choke

Fig. 8.3. Damping circuit and common mode choke

Besides the passive component in the power stage, there are also some auxiliary components for the system. To implement the feedback control, the current and voltage sensors [1], [2] are needed in the power stage. The position of the sensors in the system is demonstrated in Fig.8.1 as well. For the 3-phase 3-wire system, only two current sensors are needed to get the 3-phase

current. The SVM for NP balance and the dead-time compensation need inverter output current information. The current controller for the DC/AC converter also requires inverter current feedback. As a result, the converter output current is sensed. The 3-phase grid voltage is also sensed and it is send to the PLL for grid synchronization. Fig.8.4 shows the voltage and current sensor with the sensor board. This board provides interface between sensors and the control board. It contains all the sensor channels for both the DC/AC stage and the DC/DC stage. The board has its own power supply for the sensors. The power stage also contains pre-charge circuit and protection circuit. The pre-charge circuit consists of a 3-phase AC contactor with resistor in parallel with it. The power source of the contactor is provided by a solid state relay, which is controlled by the micro-controller I/O for automatic pre-charge from AC side. There are also AC fuses [3] at the output terminals for protection. The contactor and the fuses are shown in Fig.8.5.

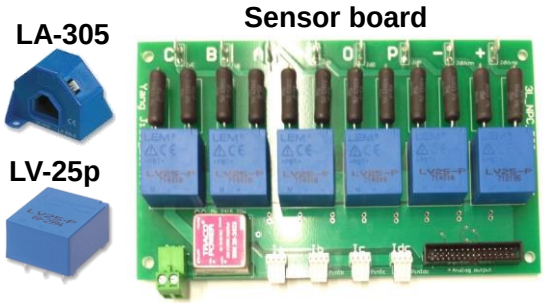


Fig. 8.4. Current and voltage sensor with sensor board

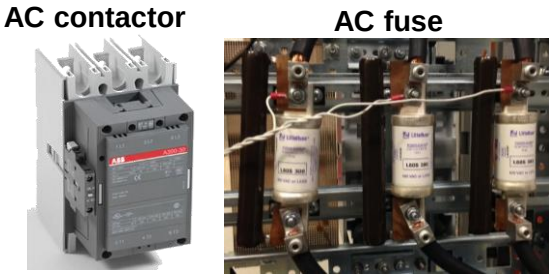


Fig. 8.5. Pre-charge and protection circuit

The system structure and power stage layout for the DC/AC part [4]-[6] is shown in Fig.8.6. The power stage is constructed by the modularized phase leg building block. Each phase leg is connected to a modularized gate driver interface board via optic fiber for gate and fault signals.

The DC/AC power stage takes the left half of the system rack as shown in the figure. The phase legs are connected by the laminated bus bars. The water pipe for the cooling system is beneath the phase leg. The bottom part of the rack is the grid interface filter and damping circuit. The auxiliary circuit like pre-charge contactor and sensor board are mounted on the grid-strap in between the phase legs and the filter. There is also a cabinet fan at the top of the rack to provide air cooling for all the components in the rack. The fan is also controlled by the micro-controller. The figure shows the DC/AC part has good space utilization and compact layout.

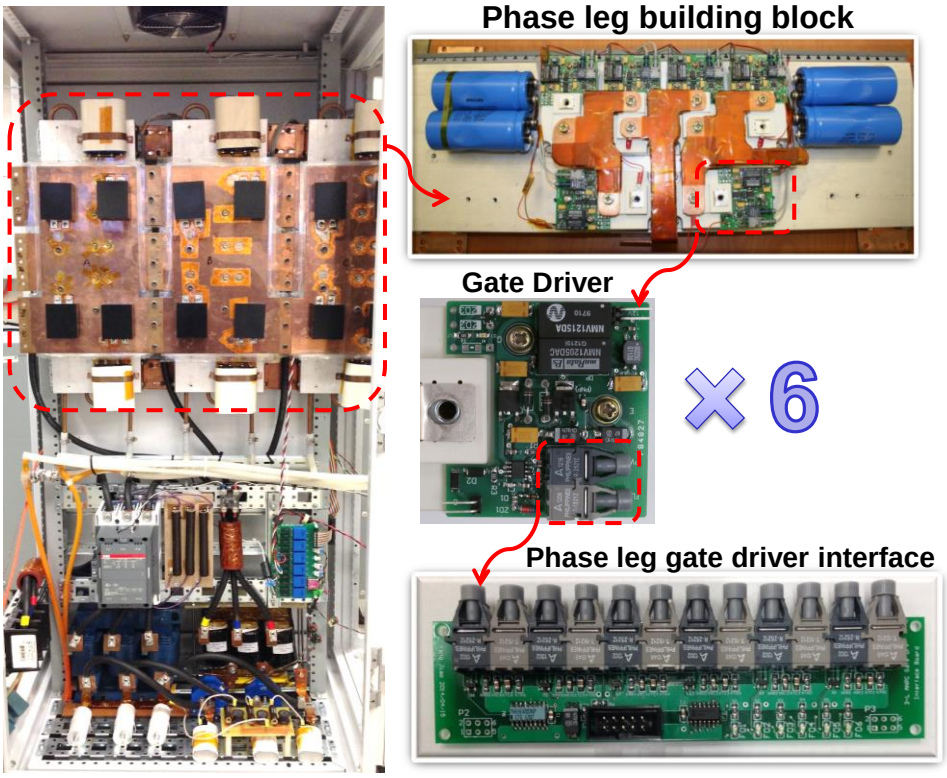


Fig. 8.6. Power stage structure and layout for DC/AC part

8.2 Power Stage and Component Structure for DC/DC Part

The DC/DC part for the power conversion system is introduced in this part. The system structure for the bidirectional DC/DC chopper is given in Fig.8.7. The power stage of the DC/DC chopper contains two phase leg building blocks. The two phase legs use N-type interleaving. To prevent the circulating current in the phase leg and also to increase the output impedance, a

unique coupled inductor for the 2-phase interleaved DC/DC chopper is designed. The coupled inductor has negative coupling to suppress the circulating DM current and positive coupling to reduce the CM output current ripple. With this design, only one inductor is need with integrated

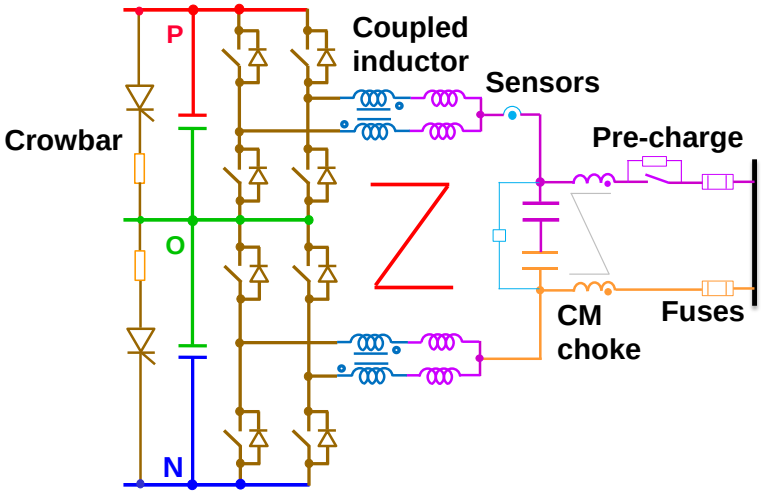
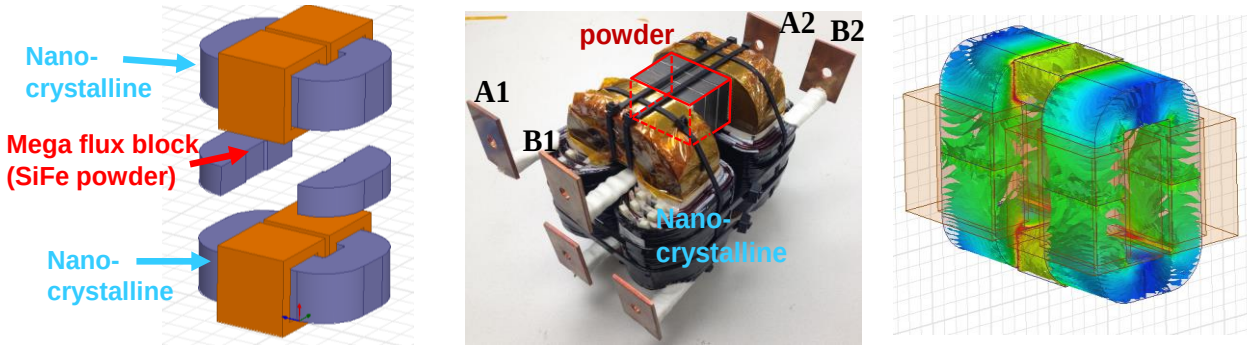


Fig. 8.7. System structure of the DC/DC part for the power conversion system

core structure instead of 2 coupled inductors or 4 individual inductors. The structure and physical layout of the coupled inductor is shown in Fig.8.8(a) and (b). For the coupling between the two legs, nano-crystalline material is used with tape-wound C core. For the coupling between the two phases, iron powder core block is used to provide the leakage. The FEA analysis for the flux distribution in the core is shown in Fig.8.8(c).



(a) Exploded view of structure (b) Physical layout (c) Flux distribution in the core

Fig. 8.8. Structure, layout and flux distribution for DC side coupled inductor

Besides the coupled inductor and capacitor for the filter, there is also a large common mode choke at the DC side. Although the DC/AC converter has its own common mode choke, the saturation current for this choke is small. Therefore, a large common mode choke is used at the DC side to provide enough common mode impedance with large saturation current. The structure for the choke is given in Fig.8.9. The common mode choke uses amorphous core. The core type is AMCC-1000 from Metglas. Copper foil is used as the winding to shrink the size. This choke has 350μH common mode inductance and saturates at over 800A current.

Fig. 8.9. DC side common mode choke

Two DC fuses are connected in serial with the DC bus terminal to provide over current protection just as the DC/AC side does. Also there is another protection circuit at the DC link to prevent it from over voltage fault. Since the DC link is shared by the DC/AC and DC/DC part, the protection circuit works for both the two parts. The crossbar circuit [6] that is used for the DC link overvoltage protection is shown in Fig.8.10(a). It contains a high current rating thyristor in serial with a high power resistor. The thyristor will be triggered and turned on when DC link voltage exceeds the threshold so that the surplus energy is dumped on the resistor. The threshold voltage to trigger the thyristor is adjusted by the gate configurations, which is the serial connected zenner diodes. The physical layout of the circuit is given in Fig.8.10(b). The crowbar circuit is connected in parallel with both the top and bottom cells of the DC link.

(a) circuit diagram (b) Physical structure and layout

Fig. 8.10. Structure and layout of the crowbar circuit

8.3 Control Architecture and System Structure for the System

Finally, the power conversion system is built by combining the DC/AC and DC/DC part. The system overall structure is given and the control system architecture is introduced. The auxiliary circuit structure is also reviewed in this part.

8.3.1 System Structure for the Power Conversion System

The overall structure for the power conversion system is given in Fig.8.11. The DC/AC and DC/DC part is connected together by the common DC link. Both the two parts has the same phase leg building blocks. Each part contains its own filter and common mode choke, as well as the sensors and protection circuit. The physical layout of the power conversion system is shown in Fig.8.12. The DC/AC part and the DC/DC part is located at the left side and right side separately, with the shared DC link. The phase legs are mounted at the middle and filters are located at the bottom. There are four digital panel meters at the top part of the DC/DC side to display the system key parameters. Each side of the cabinet has a cabinet fan for air cooling. The control system and auxiliary power supply are mounted at the back of the cabinet. The system control block diagram is given in Fig.6.6 and is not repeated here.

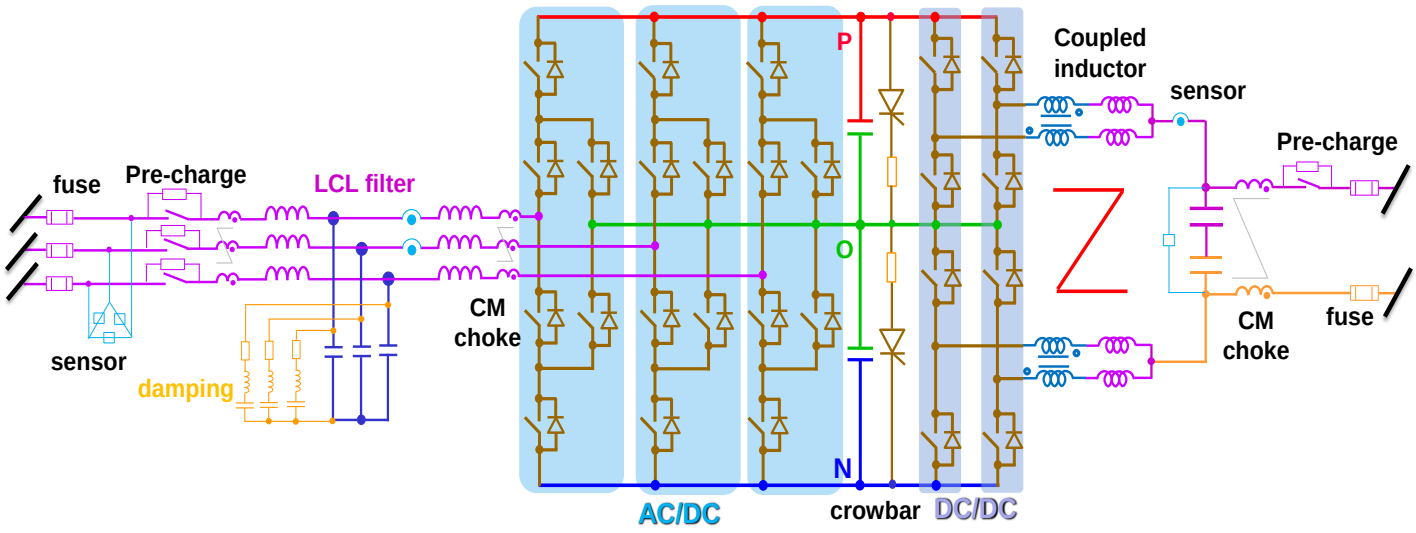


Fig. 8.11. Overall structure for the power conversion system

Fig. 8.12. Physical structure of the power conversion system

8.3.2 Control System Architecture

The power conversion system is controlled by a digital microcontroller that contains a digital signal processor (DSP) and a field programmable gate array (FPGA). The floating point DSP is TMS320C28343 from Texas Instrument [7], [8] with 200MHz frequency. The FPGA is MXO2-4000 from Lattice [9], [10]. The control system architecture is given in Fig.8.13. The DSP is

responsible for the major control function and the FPGA is the extension and interface for the input and output peripheral. The DSP uses external interface bus to communicate with two AD chips for sensor feedback. The DSP has communication with the FPGA through SPI port to exchange key variables and status. Also the PWM signals for all the switches are passed from the DSP to the FPGA for dead-time configuration and protection. The sensed voltage and current signal is compared in the hardware comparators for protection. The overcurrent and overvoltage fault together with the power module fault signals are processed by the FPGA and used to lock the PWM signals. The system fault status are also reported to the DSP via SPI communication. The FPGA also has interface with some digital input and output. It controls the contactor for DC

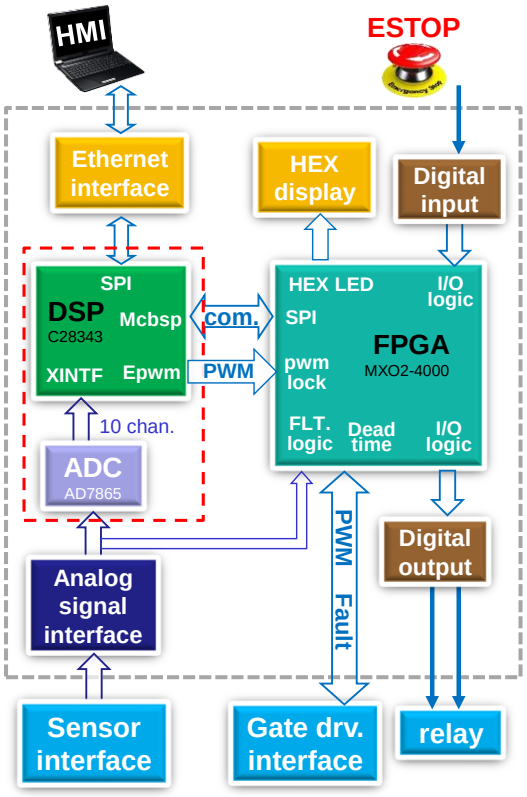


Fig. 8.13. Control system architecture

link pre-charging. The FPGA is connected to an emergency stop button for system shutdown. It is also connected to an LED display to indicate the control board internal status. The DSP is connected to the human machine interface (HMI) through optic fibers with Ethernet protocol.

The system status, operating conditions and sensed voltage and current information can be updated to the HMI. Also the operating command and system parameters can be send to DSP.

The physical layout and structure of the control board is shown in Fig.8.14. It also uses modularized design approach with several plug-in modules. The DSP control card [8] contains the DSP and the AD chips. There are 12 channel of modularized signal conditioning board for 12 channel AD signals. The digital input/output board and display board also have plug-in and play capability. This part can be flexibly configured with multiple functions The Ethernet board for HMI contains an ARM MCU to deal with the communication protocols. The whole control system is small and compact, but has full control functions. The whole control board and the gate drive interface board is mounted in the aluminum box with an auxiliary power supply and a box fan. The physical control system structure and layout is given in Fig.8.15. The aluminum box

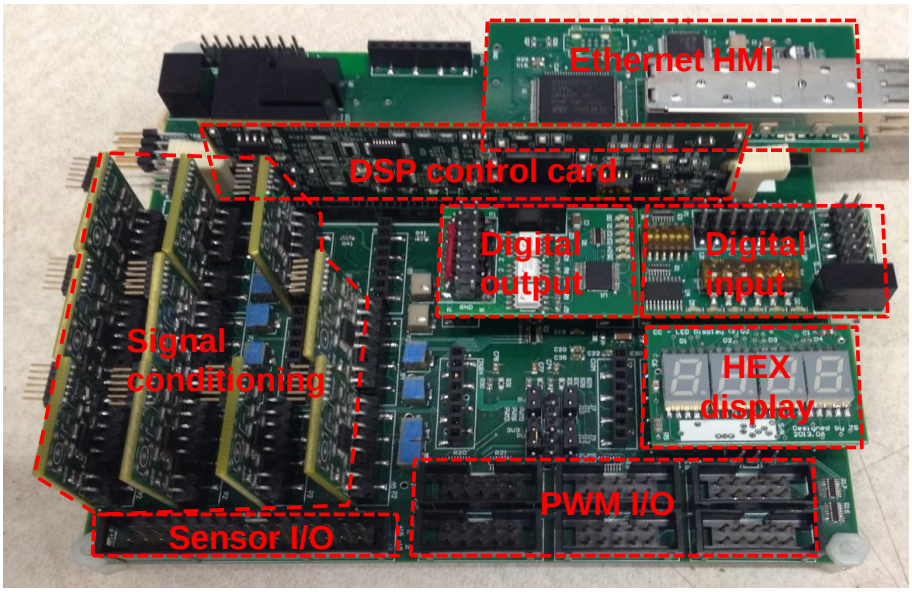


Fig. 8.14. Physical layout of the control board

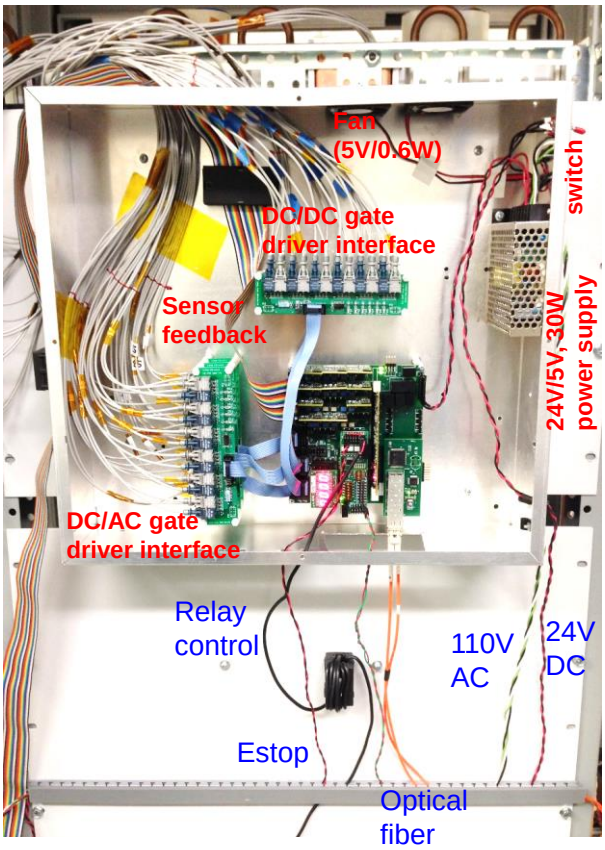


Fig. 8.15. Control system structure and layout

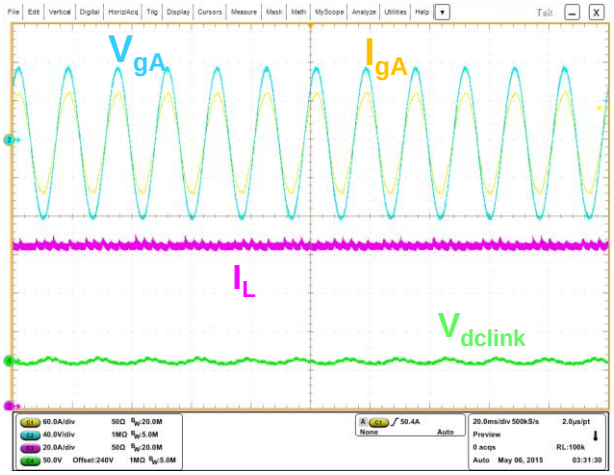
that contains the controller is mounted at the back of the system cabinet for better shielding and isolation. The gate signals are transmitted by the optic fiber. The sensor feedback from the sensor board is transmitted by the flat ribbon cable. There are also other wires to control the pre-charge contactor and provide interface to the HMI. The control system has small size and compact layout, as well as good isolation from the power stage.

8.4 Experimental Result for the Power Conversion System

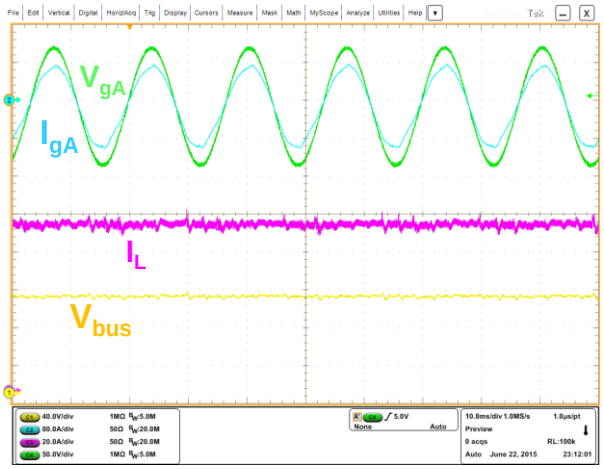
Finally, the whole power conversion system is tested with closed-loop control for both the DC/AC and DC/DC part. The system control algorithm is presented in Fig.6.6. The DC/AC part controls its active and reactive current in d-q frame as the inner current loop. The outer loop of the active current is used to regulate the DC link voltage. The DC/AC converter is synchronized

to the grid with a PLL in d-q frame. The DC/DC part controls its output current and voltage for different applications. The experimental waveforms of the steady state and step transient for the two parts has been introduced in chapter 6 and 7 respectively. Here the whole power conversion system is tested at a scaled-down power rating due to the test facility limitation. All the voltage and current rating for the system is reduced to 1/5 of their original value and the full power at the scaled-down condition is 8kW. With this proportionally scaled-down test, all the parameters for the controller just need to be scaled with a proportional gain and the transient response for the system keeps the same.

The steady state of both the unity power factor and non-unity power factor cases for the power conversion system is tested at first. The grid voltage, grid current, DC link voltage, DC bus voltage and DC inductor current waveforms are given in Fig.8.16 for the unity power factor case. The grid voltage and current waveform are in phase with each other. The DC link voltage is controlled at 240V. The average value of the DC output current is around 80A and the DC bus voltage is 100V with the scaled-down rating. For the non-unity power factor case, the same waveforms are given in Fig.8.17. The AC grid delivers 8kW active power to the DC load and 6kVAR reactive power to the DC link. The power factor is 0.8 at this case. The waveform shows the grid voltage and current has a phase shift, which indicates some reactive power from the grid. The DC voltage and current waveforms are the same as the unity power factor case.

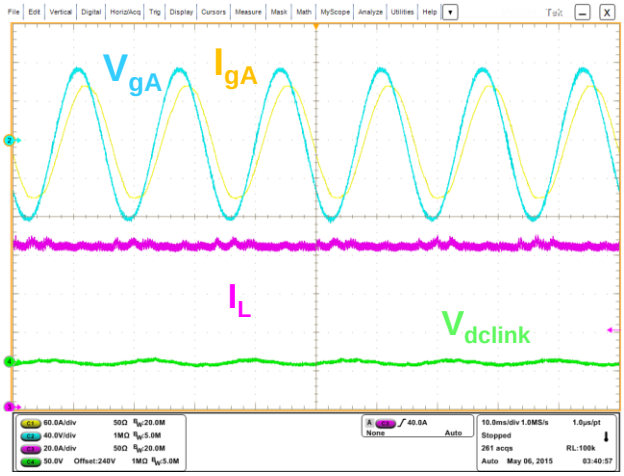


(a) Grid voltage/current, DC link voltage and DC current

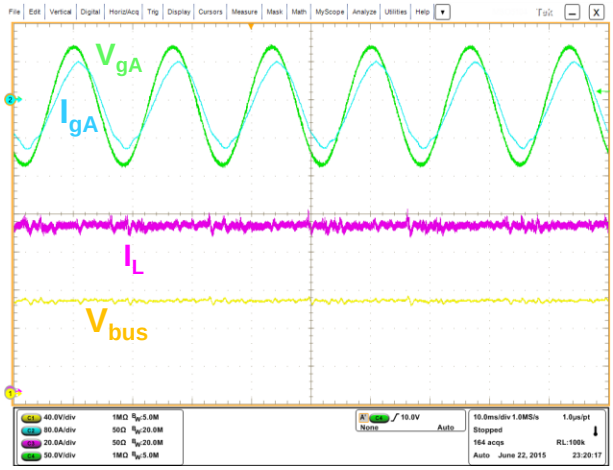


(b) Grid voltage/current, DC bus voltage and DC current

Fig. 8.16. Steady state experimental result at unity power factor



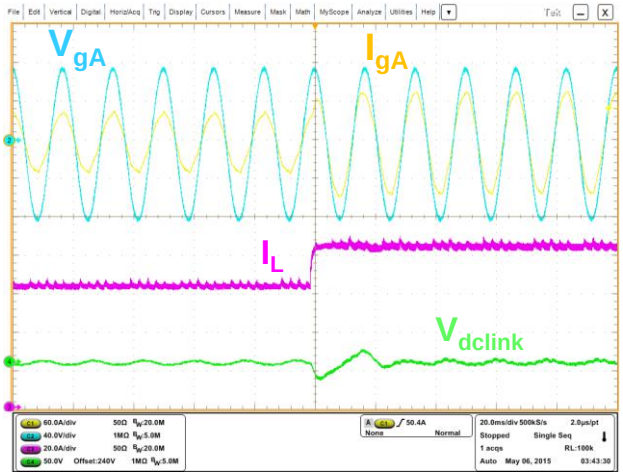
(a) Grid voltage/current, DC link voltage and DC current



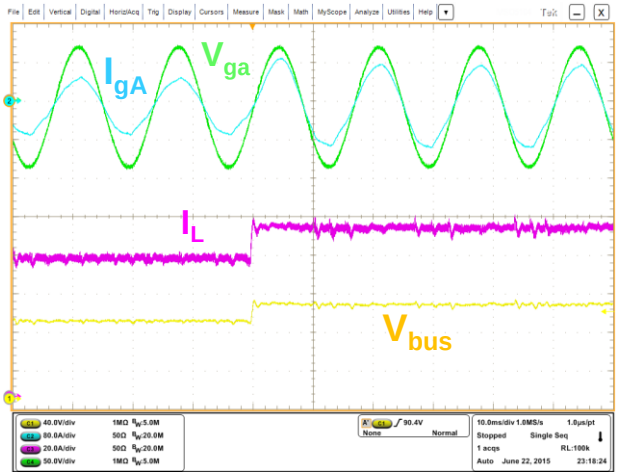
(b) Grid voltage, current/DC bus voltage and DC current

Fig. 8.17. Steady state experimental result at non-unity power factor

Then the active and reactive power step transient is tested and the same waveforms for AC and DC side voltage and current are presented. The active power step transient response is given in Fig.8.18. Step change is applied to the DC bus voltage reference. The increased power at DC



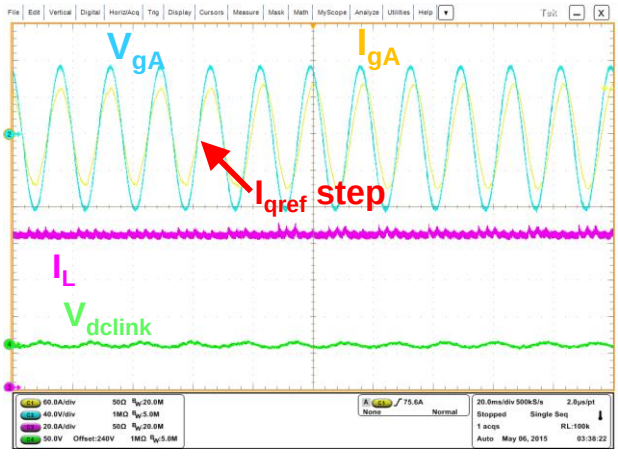
(a) Grid voltage/current, DC link voltage and DC current



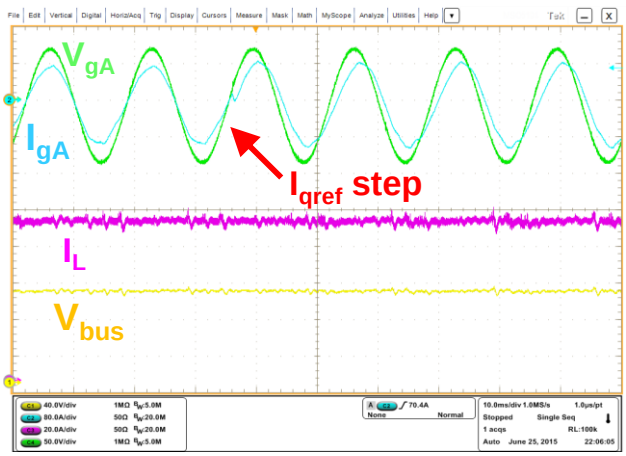
(b) Grid voltage/current, DC bus voltage and DC current

Fig. 8.18. Step transient experimental for active power

side draws more active power from the grid so that the DC link voltage can be controlled at constant value. The grid voltage and current is in phase with each other and the grid current amplitude increases after the step change. The DC link voltage goes through a small transient with the step change. The DC current and voltage also has smooth transient. This result verifies the performance of the multiple voltage and current control loops for the DC/DC chopper and DC/AC converter. Then the reactive power transient response is tested. The step change is applied to the reactive current reference for the DC/AC converter current loop. The same test result is given in Fig.8.19. The active power keeps at 8kW and the reactive power steps from 0 to



(a) Grid voltage/current, DC link voltage and DC current

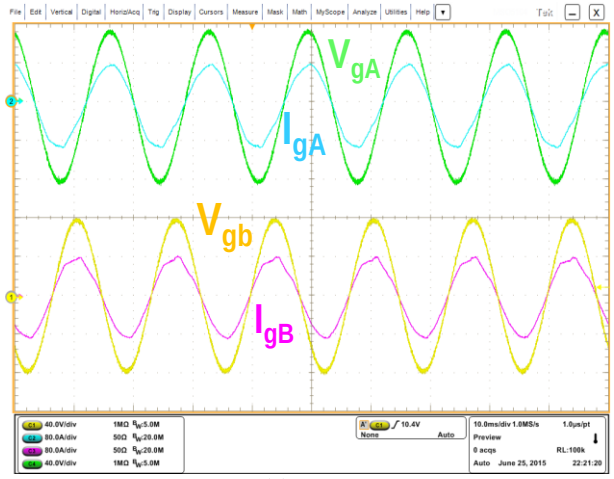


(b) Grid voltage/current, DC bus voltage and DC current

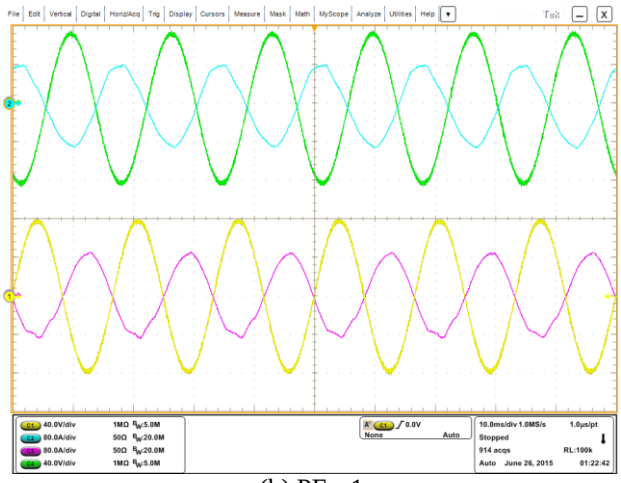
Fig. 8.19. Step transient experimental for reactive power

6kVar. A phase shift between the grid voltage and current is observed after the step change. The DC side output current and voltage does not change with the reactive power. The DC link voltage doesn't have large transient due to the d-q decoupling term added in the current control loop. The experimental result of the scaled-down power stage verifies the control loop design and the proper function of the whole power conversion system.

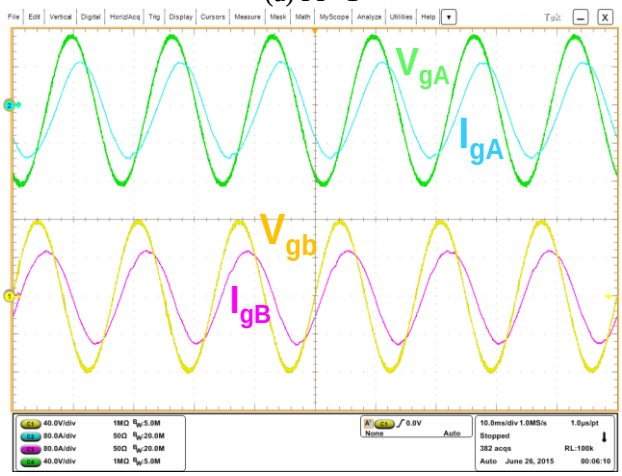
Finally, the power conversion system is tested at different power factors to verify the four quadrants operation mode. The grid voltage and current waveforms for phase A and B are shown in Fig.8.20 for the different operating points. The voltage and current waveforms for power factor at 1 and -1 are given in Fig.8.20(a) and (b) respectively. The grid voltage and current are



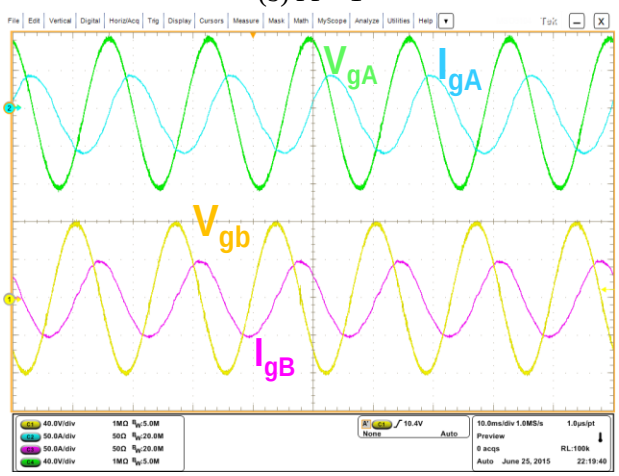
(a) PF=1



(b) PF=-1



(c) PF=0.7



(d) PF=0

Fig. 8.20. Grid voltage and current waveforms at different power factor cases

in phase or anti-phase with each other for these two cases. For the zero power factor case in Fig.8.20(d), the phase angle between grid voltage and current is 90°. This result verifies the performance of the power conversion system with bidirectional power flow at all power factors.

8.5 Summary and Conclusion

Finally, a brief summary for this chapter is given. The hardware structure of the power conversion system is introduce in this chapter. The DC/AC converter contains three of the modularized phase leg building blocks, grid interface filter and some auxiliary circuit. The grid interface filter contains the LCL harmonic filter, its damping circuit and two common mode chokes at both the grid side and converter side. The DC/AC converter has pre-charge circuit with a contactor controlled by solid state relay to establish the DC link voltage from the grid. Also the AC output terminals are connected in serial with fuses for over current protection. The DC/DC chopper stage is designed in a similar structure with phase leg building block, passive filter and some auxiliary circuit. The DC filter includes the integrated coupled inductor and a large common mode choke with high saturation current. The auxiliary circuit contains DC pre-charge circuit, DC fuses and a crow bar circuit for DC link overvoltage protection. The whole system is built with modularized structure, complete protection function and versatile control ability. The embedded digital micro controller system for the power stage is also introduced. The control system architecture and its interface with the peripheral boards is presented. The whole system has compact size and flexibly configured control functions. The performance of the power conversion system is verified by experimental result on the scaled-down hardware at different operating conditions and power factor cases.

CHAPTER.9 SUMMARY AND FUTURE WORK

In this chapter, the conclusion and summary for the whole dissertation is given. The design challenges for the high power high frequency power conversion system is discussed. The key research points and contributions are also listed. Finally, the ongoing work on the power conversion system is presented and the possible future research topics are discussed.

9.1 Summary and Conclusion

This dissertation investigates the design and optimization of the high power high frequency bidirectional 3-level power conversion system. It is a general purpose converter and the possible applications for the power conversion system includes renewable energy grid interface, energy storage system, motor drives and tractions, power supply for DC load and DC bus, energy control center for smart grid and micro-grid. The key design challenges for the power conversion system are identified as high power density, high efficiency in a wide range of operating conditions, high reliability and good power quality.

To achieve the design objectives, a survey on the high power multilevel converter topologies and modulation strategies is done in chapter 1. The survey gives a detail classifications for the multilevel topologies and modulation strategies. The pros and cons for various multilevel converters and modulation schemes are discussed. The 3-level neutral point clamped topology is selected for the 200kVA 20kHz power conversion system with bidirectional power flow.

Then the design for the high power high frequency 3-level NPC phase leg building block is carried out in chapter 2. The converter is built with a modularized approach. The phase leg building block is carefully design and optimized to achieve high frequency, high efficiency and small stress simultaneously. Different operating modes and modulation schemes for the 3-level

NPC phase leg is introduced. The four-quadrant switching loops for three modulation schemes are introduced. The two different switching loops for the 3-level NPC phase leg are identified with totally different loop parasitics. The switching performance and switching characteristics like switching energy and switching stress is evaluated for different loops. The evaluation is based on a double pulse tester with real phase leg layout. The switching performance is characterized with different influential factors like gate resistor and load current. The switching characteristic for the two switching loops are compared. Some unique switching transients are discovered and the reason for the specific switching performance is investigated and explained in detail. With the double pulse test, an accurate loss model is built based on the hardware test result and the simulation waveforms. The loss model can quantify the system total loss over a line cycle considering the difference in the switching loop. It also gives the phase leg loss distribution on each devices. This is a useful tool to quantify the system total loss at different operating points and modulation strategies for the design trade-off. The phase leg loss and stress distribution for the 3-level NPC phase leg with different modulation schemes are quantified by the loss model. Also the system total loss is calculated. The ANPC phase leg has a more evenly distributed loss and stress. The system total loss is also constant with different operating conditions. As a result, the ANPC phase leg is more advantageous than the DNPC.

In chapter 3, the space vector modulation for the 3-level NPC converter is explored due to its control freedom. The different duty cycle calculation methods are first reviewed and compared. The simplest method is adopted. Then the control flexibility with the small vectors are discussed. The implementation for different control objectives like neutral point voltage balance, loss reduction and CM noise reduction are introduced. The overall performance for different methods are compared. The neutral point voltage is selected as major control objective because it is

important to the converter's proper function. Different neutral point balance schemes are introduced and evaluated in terms of the neutral point voltage ripple and loss. The problem of high loss at low power factor cases for the conventional methods are presented and an improved SVM with NP balance and loss reduction is proposed. This method coordinately select the small vector to achieve both NP balance and loss reduction. It has the minimum switching events in each switching cycle and also has control on the NP voltage. This method has a good trade-off between the NP voltage ripple and system loss. It also keeps a constant system efficiency under different power factors. The control result for NP balance is verified on the 3-level NPC converter hardware experiment. The dead-time compensation for the 3-level NPC converter with space vector modulation is also discussed in this chapter. The influence of dead-time is presented and the compensation method is introduced. The result is verified by hardware experiment.

In chapter 4, a new modulation scheme for the 3-level ANPC phase leg is proposed to avoid the long switching loop when using the proposed SVM modulation strategy with switching cycle NP balance. The proposed modulation scheme uses paralleled neutral current paths for neutral state, therefore it reduces the conduction loss dramatically. Moreover, it results in new switching loops for the phase leg, which has reduced stress and more evenly distributed loss. The proposed method also features on its simple implementation. Each phase leg needs less PWM channels and PWM comparators. It can save 6 PWM channels in total for the 3-phase system. The switching performance for the new switching loops with the proposed modulation scheme is evaluated and characterized by the double pulse test. The test result shows a reduced switching stress for some devices. The loss distribution calculation also shows the more evenly distributed device loss on the phase leg. The total system loss analysis demonstrates the largely reduced total system loss. With the carefully designed phase leg, the proposed modulation strategy and

modulation scheme, the power stage efficiency for the 3-phase 3-level NPC converter can reach 98.5% at all power factors with 20kHz switching frequency and 200kVA power rating.

In chapter 5, the harmonic filter design for the 3-level NPC converter is discussed. The LCL filter topology is used as the harmonic filter structure. The equivalent circuit for inductor current ripple analysis is derived. The inductor current ripple is analyzed based on the proposed modulation strategy. The analytical expression for the maximum inductor current ripple over a line cycle is derived and this expression is verified by the simulation result. The inductor current ripple distribution in a line cycle is also analyzed with different power factors. The result shows that the power factor influences the position of the maximum ripple in line cycle and therefore determines the maximum current. The current stress and saturation current for the inductor should be designed accordingly. The total system loss is also quantified by the loss model with different inductor current ripple and inductance. The optimum trade-off between the power stage loss and inductor size is made by the analysis. The grid side inductor value is selected based on the grid code attenuation requirement. The damping circuit for the resonant peak of the LCL filter is also considered and discussed in this chapter. The damping result for different damping circuits are evaluated and compared. The RLC damping circuit is selected because of the good damping performance, low loss and benefit for control loop design. The designed filter and damping circuit is implemented in the hardware and tested by experiment.

With the power stage of the converter finished, the modeling and control for the DC/AC part is introduced in chapter 6. Several control strategies for the grid interface converter in the micro-grid system is first introduced and the control algorithm for the 3-level power conversion system is determined. The switching function for the 3-level NPC phase leg is defined and the state-space equation for the converter is derived with LCL filter and damping circuit. The equivalent

circuit for the average model in both ABC and d-q coordinates is given in this chapter for control loop design. One important aspects of this chapter is the verification of the derived average model by the transfer function measurement on the real hardware. The different loop gains of the power stage is measured by small signal perturbation injection. The measured result is compared with the modeling result to validate the accuracy of the modeling. With the transfer function measured in real hardware, the control loop design, especially the bandwidth and phase margin design can be more accurate and reliable. Based on the average model in d-q coordinates, the current control loop for the converter is first designed. The performance of the designed current loop is verified by the simulation and experiment result. Also the voltage loop is designed with the closed current loop. The design result is verified by the simulation and experimental result as well. Finally, the input and output impedance for the 3-level DC/AC converter is derived. The impedance for both inverter and rectifier mode operation is analyzed with and without closed-loop control. The system stability for the whole power conversion system is investigated with the load and source converter impedance analysis. The control loop design ensures a stable system and minimal sub-system interaction for the 2-stage power conversion system.

In chapter 7, the DC/DC power stage for the power conversion system is presented with the focus on the interleaving methods, current ripple analysis and also the integrated coupled inductor for high power density and ripple reduction. The three operating modes for the 3-level 2-phase DC/DC chopper is identified. Then the current ripple for the three operating modes are investigated in detail with analytical ripple expression derived. The interleaving operation reduces the output current ripple but increases the inductor current ripple. To solve this problem, the coupled inductor is added to the interleaved chopper phase legs. The same current ripple analysis is repeated. Both the analytical expression and current waveform shows the coupled

inductor reduces the circulating current and gives lower inductor current ripple. The common mode spectrum for the two interleaving methods is also compared. An integrated coupled inductor concept that combines the two coupled inductor into one is proposed. It contains the negative coupling for differential mode circulating current suppression and positive coupling to increase the output inductance. This coupled inductor is based on a 3-dimensional core structure. The flux distribution and design consideration for the core is also introduced. Finally in this chapter, the integrated coupled inductor is built and tested with the DC/DC chopper stage to verify the design and the performance of the interleaved DC/DC phase legs.

Finally in chapter 8, the system hardware structure and layout for the power conversion system is introduced in detail. The components for the DC/AC and DC/DC part are presented. The embedded micro-controller system architecture is also displayed in this part. The phase leg design, modulation scheme and control strategy is implemented in the 3-level NPC power conversion system hardware with high efficiency, high power density and full control functions. The experimental result for the whole system is also given in this part, which verifies the control loop design and the overall performance of the whole system.

At last, the key design challenges and research point for the challenges are listed in the table shown in Fig.9.1. Each research points in a row correspondents to a chapter in this dissertation. All of them considers the challenges for the high power high frequency design.

9.2 Future Work

Finally, the future work for this dissertation is discussed. The finished work on this power conversion system focus on the power stage design including the phase leg building block and the filter. The modulation strategy and scheme is also studied thoroughly. But in this dissertation, the system control algorithm just follows the conventional control strategy of the grid interface

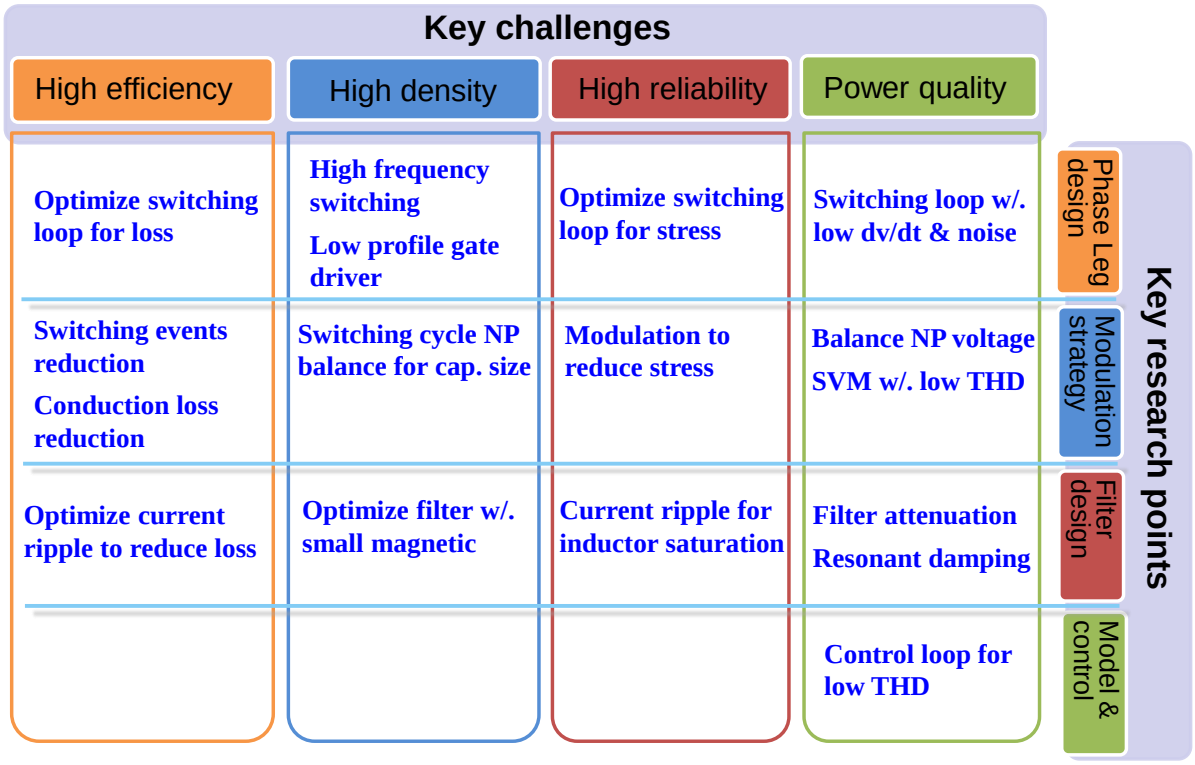


Fig. 9.1. Design challenges and corresponding research points

converter. The control design leaves interface for outer control loop to achieve high level control. There is potential to design better control loop, especially to make the power conversion system work as the energy control center. In the renewable energy micro-grid, the grid interface converter not only follows the grid voltage, but can also takes part in the grid regulation. The converter with renewable energy and energy storage system has the capability to control its own voltage in the micro-grid. It is no longer a pure current source that is tied to the grid, but an active part that forms the grid together with other converters. Also the revised IEEE standard for distributed generation system allows the converter to regulate the AC side voltage in its vicinity at the grid fault condition, which is forbidden previously. As the penetration of grid tied converter becomes higher, there are emerging concepts of designing the converter to behave like a synchronous generator. The converters can automatically synchronize with each other and share the load, as the synchronous generators do. It is possible for the 3-level power conversion

system to be controlled like this. The control method for synchronization should be investigated in the future. The control strategy for the converter to share load with others and to keep its output voltage and frequency should be studied as well. Besides the AC side control, the DC side control can also be studied. The power conversion system can also be connected to a DC bus with different renewable energy sources, energy storage systems and DC loads. The control strategy at DC side is another research point. Also the system level control for the power conversion system should be studied with the interaction between the two stages considered. With all the control strategies determined and implemented, the power conversion system will become a versatile energy control center that not only has high efficiency, high density and high reliability, but also has good control performance for the AC and DC side bus with different sources and loads.

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