Equivalent Circuit Model of High Frequency Pulse-Width-Modulation (PWM) and Resonant Converters

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Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

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Aug, 17th, 2015

Blacksburg, Virginia

Keywords: Equivalent Circuit, Design, PWM Converters,

Resonant Converters, SRC, LLC

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(Abstract)

Distributed power system (DPS) is widely adopted in Power supplies for the telecom, computer and network applications. Constant on-time current mode control and V^2 control are widely used as point-of-load (POL) converters and voltage regulators (VR) in DPS systems. Series resonant converters (SRC) are widely used in aerospace systems and LLC resonant converters are widely used as Front-end converters in DPS systems. The technological innovations bring increasing demand for optimizing the dynamic performance of the switching regulators in these applications. There has been a strong desire to develop simple and accurate equivalent circuit models to facilitate the design of these converters.

Constant on-time current-mode control has been widely used in POL and VRM converters. For multi-phase application, external ramp is required to improve jittering performance using pulse distribution method. Chapter II analyzes the effect of external ramp on small-signal model of constant on-time current mode control. It is found that external ramp brings additional dynamics by introducing a moving pole and a static zero. Next, a three-terminal switch model is proposed based on non-ideal current source concept, where the non-idealness of the current source is presented by a R_{e2}-L_{e2} branch. Based on the proposed model, design guidelines are proposed based on either worst case design strategy or auto-tuning strategy.

V^2 control has advantages of simple implementation and fast transient response and is widely used in industry for POL and VR applications. However, the capacitor voltage sideband effect, which casues the instability problem when ceramic capacitors are employed, also needs to be taken into consideration in modeling. Chapter III proposed a unified equivalent circuit model of V^2 control, the model is built based on non-ideal voltage source concept. The model represents capacitor voltage sideband effect with a R_{e2}-L_{e2} branch, which forms the double pole by resonating with power stage output capacitor. The equivalent circuit model is a complete model and can be used to examine all the transfer functions. Bsed on the unified equivalent circuit model, design guidelines for VR applications and general POL applications are provided in Chapter IV, for both constant on-time V^2 control and constant frequency V^2 control.

For resonant converters, the small-sginal modelling is very challenging as some of the state variables do not have dc components but contain strong switching frequency component and therefore the average concept breaks down. For SRC, the equivalent circuit model proposed by E. Yang in [E26] based on the results by the extended describing function concept is the most successful model. However, the order of the equivalent circuit model is too high and the transfer functions are still derived based on numerical solution instead of analytical solutions. Chapter V proposes a methodology to simplify the fifth-order equivalent circuit of SRC to a third-order equivalent circuit. The proposed equivalent circuit model can be used to explain the beat frequency dynamics: when switching frequency is far away from resonant frequency, beat frequency will occur; when the two frequencies are close, beat frequency will disappear and another double pole which is determined by equivalent inductor and output capacitor will be formed. For the first time, analytical solutions are provided for all the transfer functions which are very helpful for feedback design.

LLC resonant converters are widely adopted as front-end converter in distributed power system for the telecom, computer and network applications [F2]. Besides, LLC resonant converters are also very popular in other applications, such as LCD, LED and plasma display in TV and flat panels [F3]-[F6]; iron implanter arc power supply[F7]; solar array simulator in photovoltaic application[F8]; fuel cell applications[F9],and so on. For LLC, no simple equivalent circuit model is available and no analytical expressions of transfer functions are presented. Chapter VI proposes an equivalent circuit model for LLC resonant converter. When $F_s \geq F_o$, L_m is clamped by the output voltage and LLC behaves very similar as SRC. As a result, the dynamic behavior is similar as SRC: when switching frequency is larger than resonant frequency, the beat frequency double pole show up and the circuit is third-order; when switching frequency is close to resonant frequency, beat frequency double pole disappear and a new double pole formed by equivalent inductor L_e and equivalent output capacitor C_f show up. The circuit reduces to second order. When $F_s<F_o$, L_m participates in resonance during some time periods and the circuit is essentially a multi-resonant structure. An approximated model is proposed where the equivalent resonant inductor is modified to include the effect of L_m. As a result, the double pole will move to a little lower frequency. For the first time, analytical solutions are provided for all the transfer functions which are very helpful for feedback design.

In conclusion, the works shown in this dissertation focus on small-signal equivalent circuit modeling for Buck converters with advanced control schemes and also resonant converters. The models are simple and accurate up to very high frequency range (1/2 f_{sw}).

To My Family:

My parents: *Chunyong Tian*

Qiu'e Gu

My sister: *Lijun Tian*

Acknowledgments

First I would like to express my sincere gratitude to my advisor, Dr. Fred C. Lee. In my early research life, he shows me hand-by-hand how to climb the mountain of research in power electronics. His depth of knowledge, strict standards on research, and inspiring encouragement during the hard time provide me the power to break the rock blocking my research. The traning of the rigorous research attitude and logical thinking process have been a great value for me and will be a great asset during my future career and life.

I would like to thank Dr. Paolo Mattavelli for his valuable guidance during my research. I also want to acknowledge the other members of my advisory committee, Dr. Dushan Boroyevich, Dr. William T. Baumann and Dr. Steve C. Southward for their support, comments, and suggestions. Meanwhile, I would like to thank Dr. Qiang Li, for his guidance and discuss on my research.

I want to acknowledge my teammates in control group (POL group) in Power Management Consortium (PMC) of CPES: Dr. Yingyi Yan, Mr. Feng Yu, Dr. Pei-hsin Liu, Mr. Syed Bari, Ms. Virginia Li, Dr. Yipeng Su, Dr. Dongbin Hou, and Mr. Mohamed H. Ahmed.It has been a great pleasure to work with the talented, creative, helpful and dedicated colleagues.

I would like to thank my colleagues in Dr Lee and Dr Li's other groups. It has been an honor to work with these intelligent people: Dr. Dianbo Fu, Dr. Pengju Kong, Dr. David Reusch, Dr. Mingkai Mu, Dr. Weiyi Feng, Dr. Daocheng Huang, Mr. Pengjie Lai, Mr. Zijian Wang, Mr. Qian Li, Mr. Haoran Wu, Mr. Chanwit Prasantanakorn, Mr. Shu Ji, Mr. Li Jiang, Mr. Wei Zhang, Mr. Zhiqiang Wang, Mr. Xiucheng Huang, Mr. Zhengyang Liu, Mr. Yucheng Yang, Mr. Chao Fei, Mr. Xuebing Chen, Mr. Zhongsheng Cao, Mr. Bin Li, Mr. Tao Liu, Mr. Zhengrong Huang, Mr. Junjie Feng. Mr. Yang Jiao, Mr. Sizhao Lu, Mr. Yadong Lv, Mr. Ruiyang Qin, Mr, Chen Li, Mr. Shishuo Zhao.

I also appreciate all other colleagues and students at CPES: Dr. Fang Luo, Mr. Igor Cvetkovic, Dr. Dong Dong, Dr. Ruxi Wang, Dr. Zheng Chen, Dr. Sara Ahmed, Dr. Zhiyu Shen, Dr. Xuning Zhang, Dr. Bo Wen, Dr. Marko Jaksic, Dr. Milisav Danilovic, Mr. Lingxiao Xue, Mr. Bo Zhou, Dr. Hemant Bishnoi, Ms. Christina DiMarino, Mr. Jun Wang, Mr. Qiong Wang,Mr. Chi Li, Mr. Vahid Najmi, Mr. Bingyao Sun, Ms. Nidhi Haryani, Mr. Li Jiang, Mr. Yin Wang, Ms. Han Cui, Mr. Woochan Kim, Mr. Tao Tao, Mr. Di Xu, Mr. Kumar Gandharva, Mr. Zhemin Zhang, Mr. Hanguang Zheng, Dr. Yiying Yao, Ms. Yincan Mao,Mr. Ming Lu, Mr. Ting Ge, Mr. Lujie Zhang, Ms. Fan Ye, Mr. Chien-An Chen, Mr. Fang Chen. It is a great fortune to have the opportunity to learn from each other in the past six years, and widen the knowledge of different areas in the vast power electronics field.

I am thankful for the helpful discussion with many visiting scholars. They are: Dr. Brian Cheng, Dr. Xiaoyong Ren, Dr. Fanghua Zhang, Dr. Yuling Li, Dr. Qiaoliang Chen, Dr. Yue Chang, Dr. Xinke Wu, Dr. Feng Wang, Dr. Xin Ming, Dr. Feng Zheng. Dr. Weijun Lei, Mr. Zeng Li, Dr. Xiaofei Chen, Dr. Li Wang, Mr Chaofeng Cai. Dr. Weijing Du, Dr. Ruofeng Yang. Dr. Yan-Cun Li, Mr. Shuojie She, and Mr. Peiqing Hu.

I would also like to thank all the wonderful staffs in CPES: Ms. Linda Gallagher, Ms. Teresa Shaw, Ms. Marianne Hawthorne, Ms. Linda Long, Ms. Teresa Rose, Dr. Wenli Zhang, Mr. Doug Sterk and Mr. David Gilham for their support and help over the past six years.

With much love and gratitude, I want to thank my parents and my sister for their endless love, encouragement, and support throughout more than twenty years of school.

This work was supported by the power management consortium (3M Company, Altera - Enpirion Power, Chicony Power, CSR Zhuzhou Institute Co., Ltd., Delta Electronics, Eltek, Emerson Network Power, Huawei Technologies, International Rectifier, Linear Technology, Macroblock, Inc., Murata Manufacturing Co., Ltd., Panasonic Corporation, Richtek Technology, ON Semiconductor, Sonos, Texas Instruments).

This work was conducted with the use of SIMPLIS software, donated in kind by Simplis Technology of the CPES Industrial Consortium.

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Chapter 1. Introduction

1.1 Research Background

With the development of information technology, telecom, computer and network systems have become a large market for the power supply industry [A1]. Power supplies for the telecom, computer and network applications are required to provide more power with less size and cost [A2][A3]. To meet these requirements, the distributed power system (DPS) is widely adopted. As shown in Figure 1.1, the distributed power system is characterized by distribution of the power processing functions among many power processing units [A4]. DPS system has many advantages, such as less distribution loss, faster current slew rate to the loads, better standardization and ease of maintenance[A7][A8].

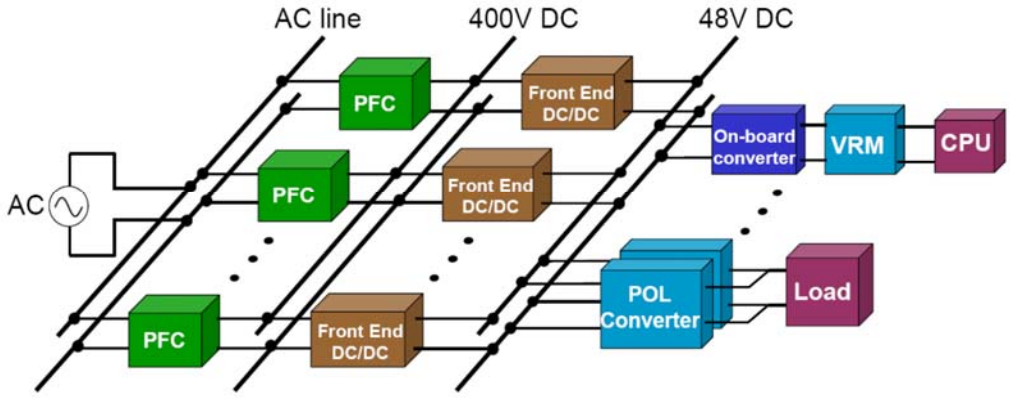


Figure 1.1 A typical distributed power system

Let us look at the trend for the distributed power system. Using data center as an example, recently the exponential rise in "Big Data" generation, processing and storage highlights the growing demand for datacenter and cloud computing power worldwide. The challenge is to maximize energy efficiency, thus saving money and natural energy resource, minimizing pollution

and meeting the US Department of Energy's "Exascale" challenge. To pursuit higher efficiency and power density, the existing solution within the AC-DC conversion-system topology is struggling to provide even a few percentage points of large-scale improvement despite localized improvements in performance.

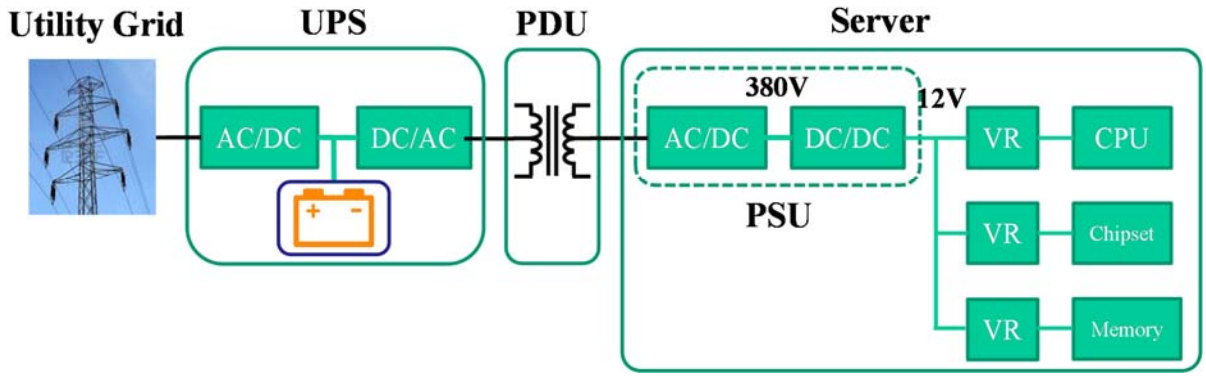


Figure 1.2 Traditional AC distribution system for data center

Recently, A DC data center structure is proposed to improve efficiency and power density. Using high-voltage DC for power transmission, in conjunction with new conversion approaches, offers tangible and significant benefits for both sourcing options and system end-to-end performance. By eliminating a transformer in the power distribution unit (PDU) and reducing the length of 12V bus, the overall efficiency can be improved. This structure is employed recently by IBM in their Power 775 supercomputer structure [A9]. As shown in Figure 1.4, the frond end DC-DC converter and the VRMs are put into the same drawer therefore the loss on 12V bus is minimized. However, to achieve this the power density needs to be improved by 5 to 10 times. The challenge lies in how to design high efficiency high desity front end DC-DC converer and high frequency high bandwidth VR module and POL converters.

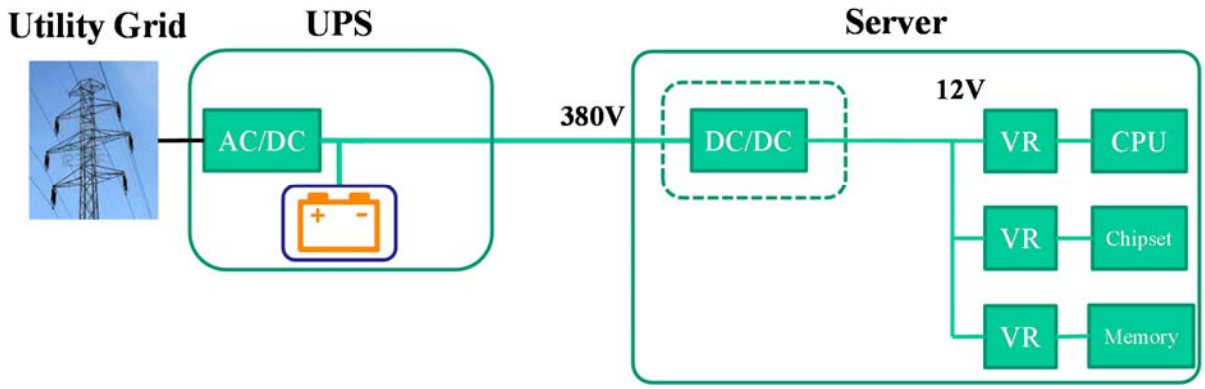


Figure 1.3 380V DC distribution system for data center

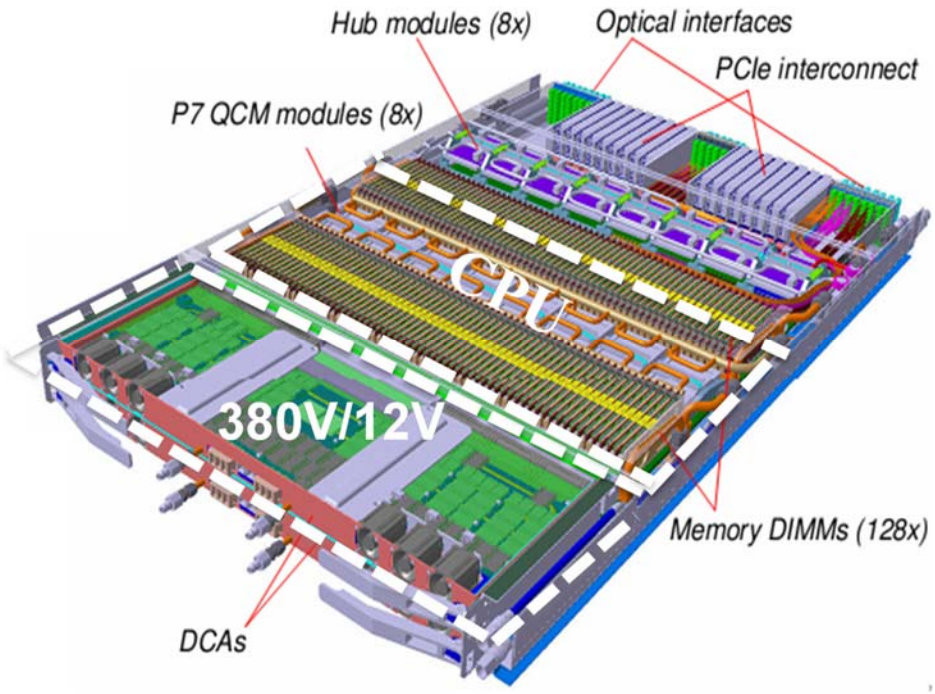


Figure 1.4 IBM power 775 supercomputer for data center.

Current-mode control has been widely used in POL and VRM converters for several decades [C1]-[C10]. In current-mode control, as shown in Figure 1.5, the inductor current, which is one of the state variables, is sensed through a current sensing network and used in the PWM modulator. Generally speaking, two-loop structure is used in current-mode control. Current mode control has

many advantages compared with traditional voltage mode control, such as simple compensation, inherent current limiting and current sharing abilities.

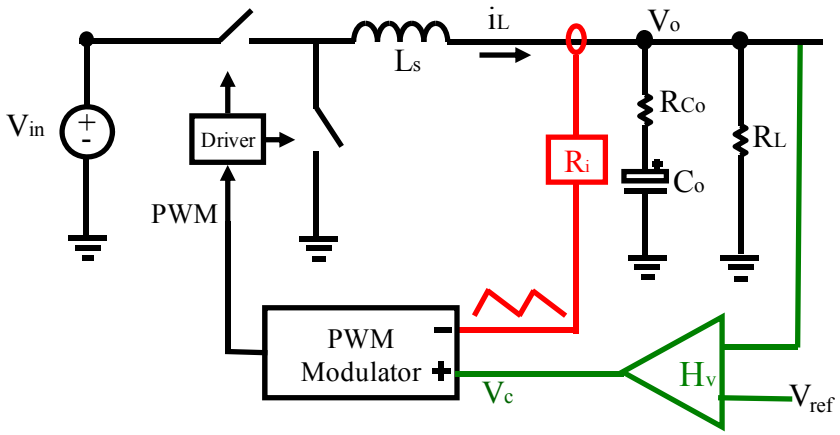


Figure 1.5. Control structure of current-mode control

Many different schemes of current mode control have been proposed and were summarized in [C7], including peak current-mode control, valley current-mode control, constant on-time control, constant off-time control, as shown in Figure 1.6. From switching frequency point of view, peak current and valley current mode control are constant frequency cases, while constant on-time and constant off-time current mode control are variable frequency cases.

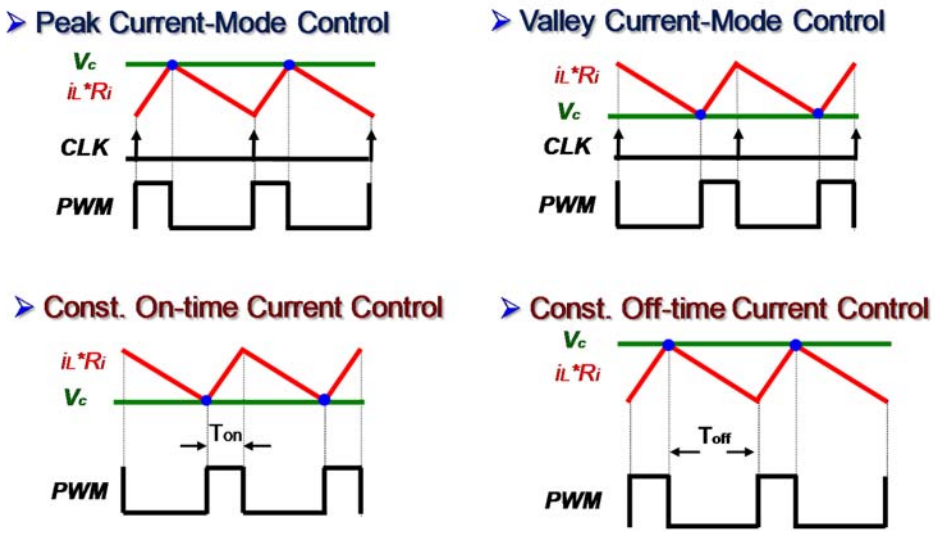


Figure 1.6 Four different modulation schemes of current mode control

Among the above four current mode schemes, peak current mode is widely used in industry from the moment current mode control is proposed. And recently, due to its unique feature of high light load efficiency, constant-on-time control is gaining more and more attraction both in industry [C11]- [C14] and in academy [C26] [C27]. Consider notebook as an example, the CPU goes into sleep states very frequently and spends 80% of the time at light load condition, therefore, light-load efficiency of the VR is very important for battery life extension. At the light load condition, switching-related loss dominates the total loss. Thus, constant-on-time control is widely used to improve light-load efficiency, since the switching frequency can be lowered to reduce switching-related loss. Many commercial products of constant-on-time current mode control are used in industry for POL [C11][C12] and VR applications [C13][C14][C15].

A typical implementation of current mode control, which tries to utilize the ESR of the output capacitor as current sensing resistor, is gaining more and more attention for POL and VR applications in industry [D1]-[D11]. This structure is called V^2 control as it directly feedbacks the output voltage and use it twice. Originally V^2 control is proposed to provide ultra-fast transient performance [D1][D2]. The structure of V^2 control is shown in Figure 1.7.

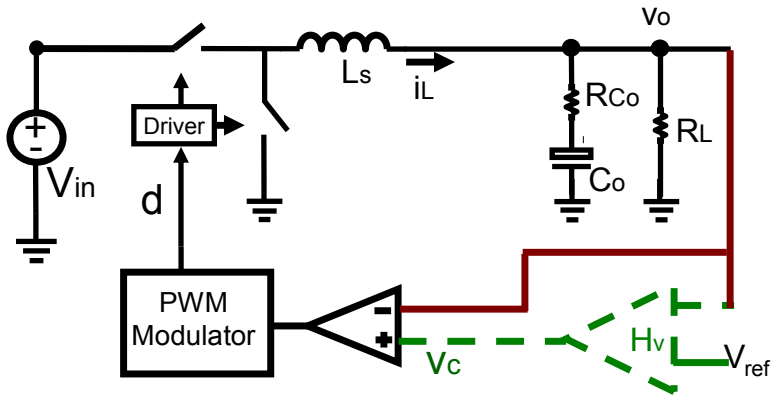


Figure 1.7 Structure of V^2 control (with outer loop compensator shown in dashed line) and ripple based control (without outer loop compensator).

There are two voltage feedback loops for V^2 control. The inner loop is a direct voltage feedback loop: the output voltage signal is directly fed into the modulator. Usually the outer loop is slower than inner loop: the voltage feedback will go through a compensation network to generate the control signal. When the output voltage varies due to disturbances either from the input voltage or the load variations, the duty cycle will change immediately since the modulator will directly see the output voltage change through the inner feedback loop. Therefore, one advantage for V^2 control is that it can provide faster transient response. Especially, it can provide faster load transient response compared with current mode control. As for current mode control, when load transient happens, the duty cycle response through the outer loop compensation which is intuitively slower compared with the direct feedback inner loop in V^2 control.

Another advantage of V^2 control compared with current mode is its simple implementation. There are two aspects to show its simplicity over current mode control. One aspect is that for V^2 control, no current sensing network is required; conceptually it uses the ESR of the output capacitor as a current sensing resistor. The other aspect is the outer loop compensation for V^2 control is simpler than current mode control. In current mode control, the outer loop bandwidth is responsible for the load transient performance and typically a one-zero two-pole compensation network (or type II compensation) is required to achieve the desired bandwidth and stability margin. In V^2 control, a low-bandwidth integrator network is enough since the purpose of the outer loop is to eliminate the steady state error which equals to half of the output voltage switching ripple instead of its responsibility for the transient performance. In some applications which does not care so much about the steady state error, the outer loop compensation, shown as green dashed line in Figure 1.7 can be saved, which is referred as ripple based control in some literatures [D12][D13].

V^2 control concept can be implemented as constant frequency modulation (including constant frequency V^2 peak control [D14]-[D23] or constant frequency V^2 valley control [D24][D35]) or variable frequency modulation (including constant on-time V^2 control[D25]-[D32] and constant off-time V^2 control [D1][D2]). Among the four, constant on-time V^2 control [D3]-[D8] and constant frequency V^2 peak control [D9]-[D11] are most popular in commercial products. In industry products, various names are used based on their own understanding on constant on-time V^2 control structure: for example, Texas Instruments' D-CAP, D-CAP+, and D-CAP2 control products; Maxim's Quick-PWM control products and National Semiconductor's constant on-time control products.

For front-end DC-DC converters, due to hold-up time requirement [E1], conventional PWM converters have to sacrifice normal operation efficiency to extend their operation range. As a result, resonant DC-DC converters have drawn a lot of attention and are widely adopted in front-end DC-DC converters.

Series resonant converter (SRC) is the simplest resonant converter. The schematic of full-bridge series resonant converter is shown in Figure 1.8. It has been used widely for power conditioning in the sophisticated aerospace industry [E2]-[E6] and in some industrial applications such as laser power supply applications [E7]. By using this topology, zero-current switching can be achieved when switching frequency is below than the resonant frequency. Therefore, the switching loss can be reduced. Furthermore, the cumbersome and costly apparatus needed for forced current commutation is avoided for transistor.

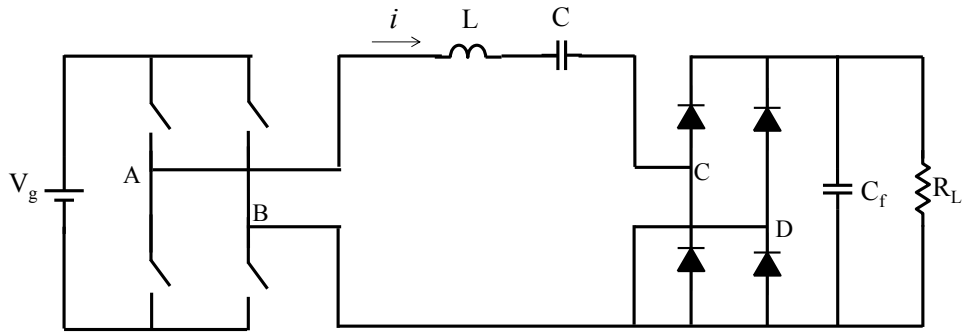


Figure 1.8 Schematic of full-bridge series resonant converter (SRC)

The most popular resonant converter for front-end DC-DC converters is LLC resonant converter [F1]. The half-bridge LLC topology is shown in Figure 1.9. With this topology, the holdup time extension capability is accomplished without sacrificing the efficiency under the nominal operating condition. As a result, in comparison with soft-switching PWM converters, LLC resonant converters can achieve a higher power density with better efficiency.

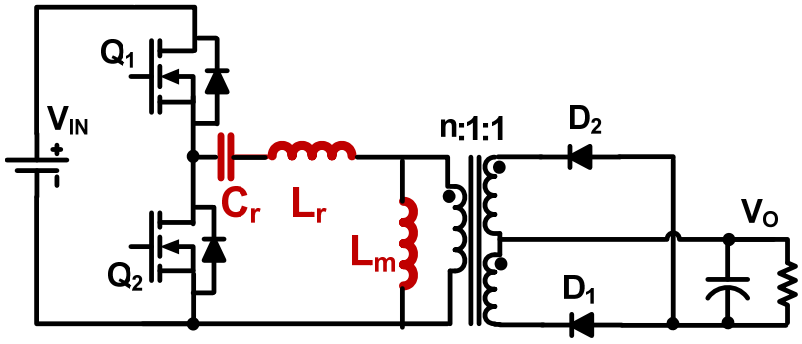


Figure 1.9 Schematic of half-bridge LLC resonant converter (LLC)

Besides of front-end converter in distributed power system for the telecom, computer and network applications [F2], LLC resonant converters are also widely adopted in other applications, such as LCD, LED and plasma display in TV and flat panels [F3]-[F6]; iron implanter arc power supply[F7]; solar array simulator in photovoltaic application[F8]; fuel cell applications[F9],and so on. A lot of commercial IC companies, such as Texas instruments, STMicroelectronics, and On Semiconductors are developing controllers to support the design of LLC converter [F10]-[F16].

1.2 Literature Review of Existing Models

As discussed in previous section, current mode control and V^2 control are very popular in POL and VR applications, while resonant converters are widely used in front-end DC-DC converters.

For stability concern and optimal design purpose, small-signal models are indispensable and numerous research efforts have already been spent in modeling area. Previous achievements and remaining challenges are summarized in this section.

1.2.1 Literature review on modeling of current mode control

Before current mode control is proposed, average technique is widely adopted in power electronics community to tackle the problem of power stage modeling. The average concept focus on low-frequency dynamic of the power stage by eliminating the switching frequency information through switching averaging operation. The original concept is proposed by G. Wester [B1]. Later, S. Cuk proposed state-space averaging method which combines the averaging technique with state-space representation [B2][B3]. State-space averaging technique is a general systematic method for any topology and a canonical circuit model is proposed. However, the model is obtained after a considerable amount of matrix manipulations. R. Tymerski [B4] and V. Vorperion [B5][B6] proposed three-terminal switch model and the basic concept is to do the average model of the non-linear switch pair instead of the whole converter. Compared with state-space averaging method, three-terminal switch model is much simpler and more circuit-oriented. Therefore, it is widely used for design of the compensator in voltage mode control.

For current mode control, modeling of peak current mode control is a main focus in early days due to its popularity. For peak (valley) current mode control, it is well-known that the current

loop may run into sub-harmonic oscillation if the duty cycle is larger (smaller) than 0.5. As early as 1980s, many papers are devoted to the modeling of peak (valley) current mode control [C16][C17][C18][C19]. However, these models are either based on the "current source" concept or "state space average" concept which can only predict the low-frequency response and can't be used to predict subharmonic oscillations in peak (valley) current-mode control. The first model that can predict subharmonic oscillation is by using discrete-time analysis which treat the current loop as a discrete-time system by D. J. Packard [C20] or a sample-data system by A. R. Brown [C21]. However, the discrete-time model or sampled-data model is hard to use and several modified average models are proposed based on the results of discrete-time analysis and sample-data analysis[C22][C23][C24][C25]. The most popular model for peak (valley) current mode control is proposed by Dr. R. Ridley[C24], which provides both the accuracy of the sample-data analysis and the simplicity of the three-terminal switch model in continuous time domain. The model is based on the so called sample and hold concept and the sample and hold term $H_e(s)$ is used to capture all the sideband related information and hence to predict the sub-harmonic oscillation. R. Ridley's model is shown as Figure 1.10.

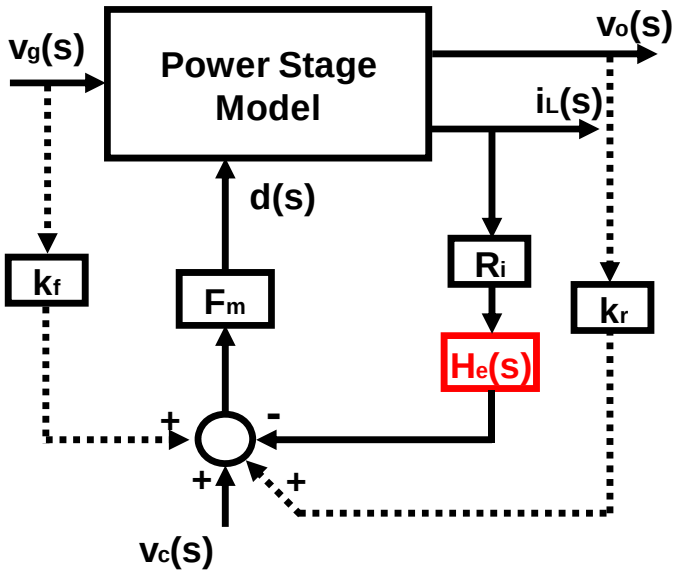


Figure 1.10 R. Ridley' model for peak current-mode control [C24]

R. Ridley's model can accurately predict sub-harmonic oscillations in peak current-mode control and valley current-mode control. However, for variable frequency modulation current mode control, the current-loop behavior is different from that in peak current-mode control. In peak current-mode control, the inductor current error varies at switch off instant and stays the same for one switching period. This is called the "sample and hold" effect, as shown in Figure 1.11 (a). While in constant on-time control, the inductor current goes into steady state in one switching period. No "sample and hold" effects exist in constant on-time control, as shown in Figure 1.11 (b). Therefore, R. Ridley's model can't be applied to variable frequency current mode control. Figure 1.12 shows that R. Ridley's extended model to constant on-time control is not accurate at predicting the small-signal behavior [C31].

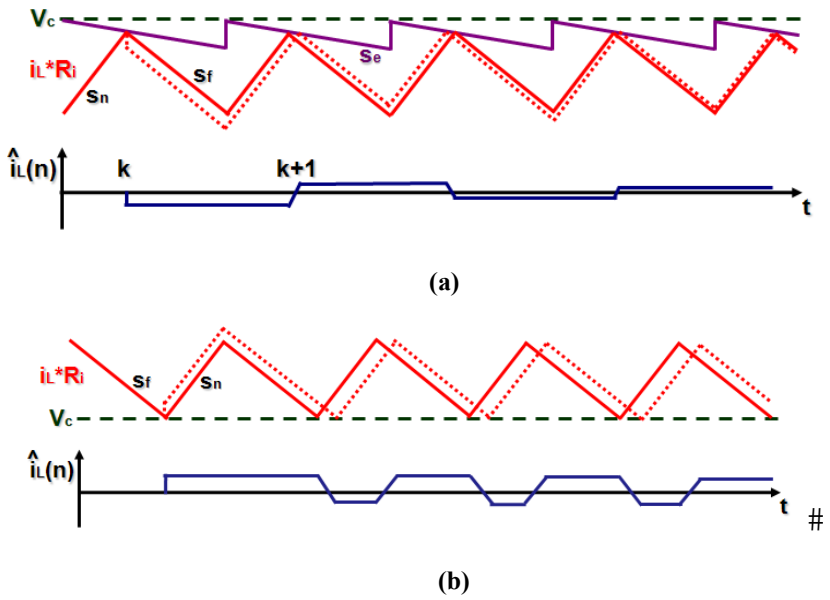


Figure 1.11 Perturbed inductor current waveform: (a) in peak current-mode control (b) in constant on-time current mode control

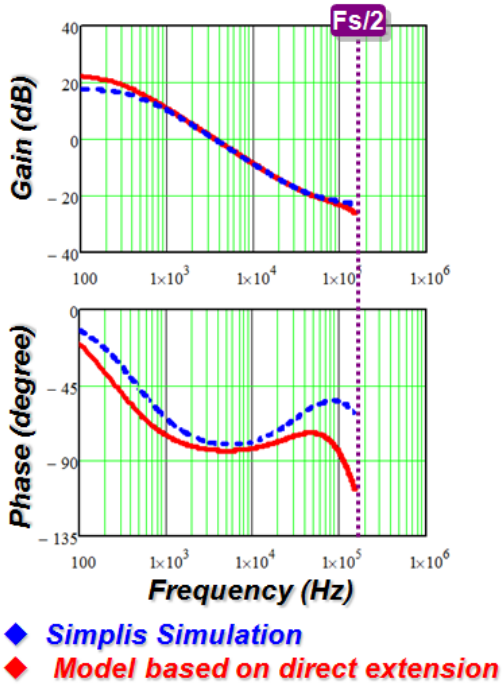


Figure 1.12. Discrepancy of the extended model for constant on-time current mode control [C31]

To propose an accurate small-signal model for constant-on-time current mode control, a continuous time model is derived and proposed in [C32] from a brand new angle: time domain

describing function method [C33]. The PWM modulator, the switches and the inductor are treated as a single entity instead of breaking into separate parts. As shown in Figure 1.13, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the control signal v_c; then, based on the perturbed inductor current waveform, the describing function from the control signal v_c to the inductor current i_L can be found by mathematical derivation. The same method is applied to derive two additional terms that represent the influence from input voltage v_{in} and output voltage v_o.

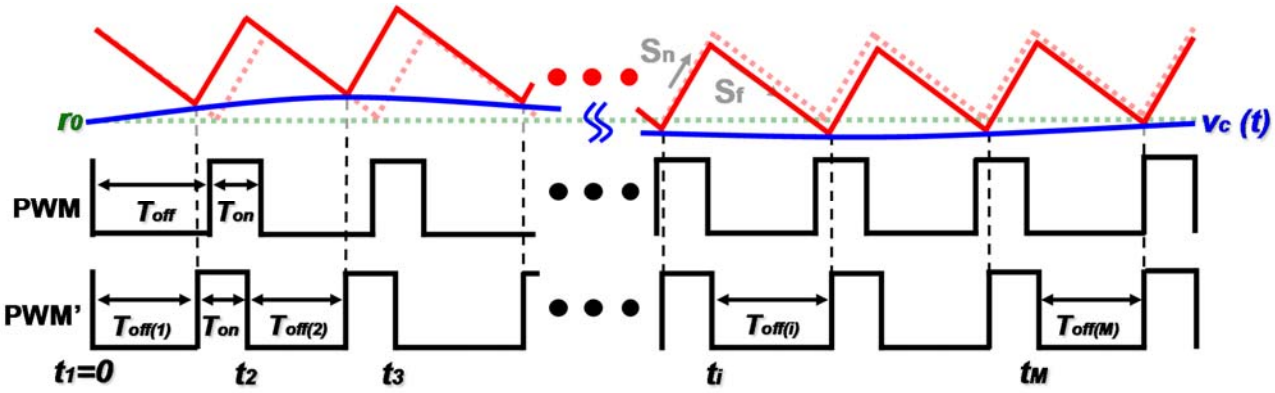


Figure 1.13. Perturbed waveform in constant on-time current mode control [C32]

Describing function method is not only applicable to constant on-time current mode control, but also to other current mode control such as peak current mode control, following the similar derivation process. Therefore, it is a systematic method for modeling of current mode control. The disadvantage of this method is its complicated mathematical derivation process without adequate physical meaning. To gain more physical insight, a unified equivalent circuit model for Buck converters with different modulation schemes is derived based on the results from describing function method [C32], as shown in Figure 1.14. This equivalent circuit model reveals the fact that physically current mode control turns inductor into a non-ideal current source, and the non-ideal ness is represented by R_e and C_e, which will resonate with power inductor L_s and form a double

pole at high frequency. This equivalent circuit model can be used to derive control to output, output impedance and input to output transfer functions, all of them are accurate up to half of switching frequency.

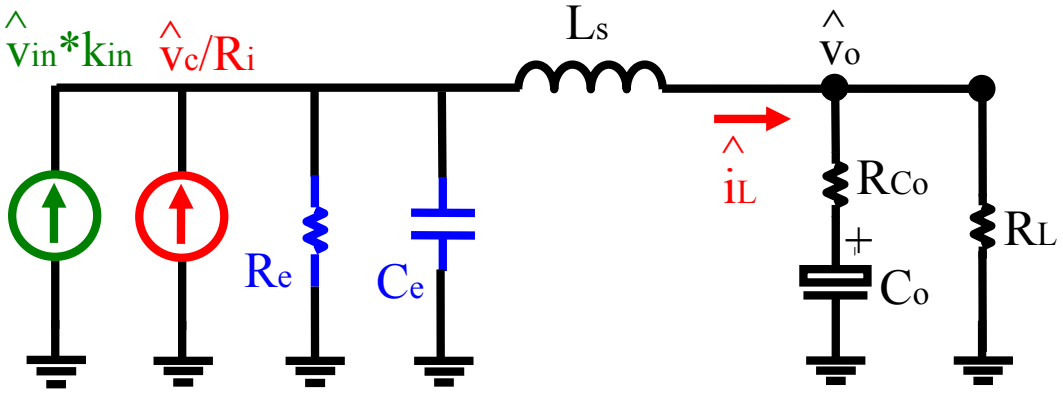


Figure 1.14 Jian Li's equivalent circuit model for Buck converter with current mode control [C32]

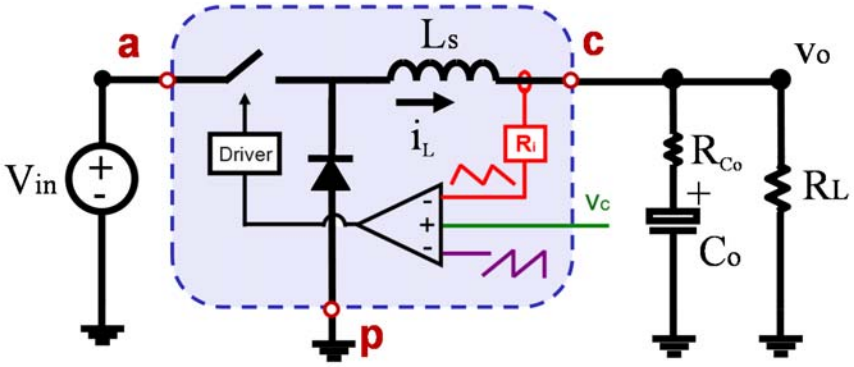
However, the equivalent circuit model shown in Figure 1.14 has the following two limitations:

(1) It is not a complete model for a Buck converter with current mode control since the input current property is lost. As a result, input impedance tansfer funciton, which is very important for cascading converters, is missing.

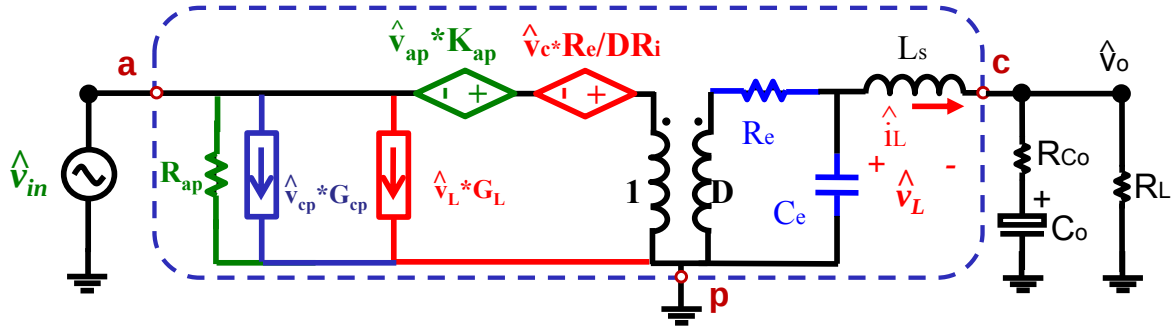
(2) The equivalent circuit is only for Buck converter, no equivalent circuits for Boost and Buck-boost converters with current mode control are available.

To solve the above two issues, a three-terminal switch concept with current feedback is proposed in [C34]. This equivalent circuit model takes the active switch, passive switch and the closed current loop as an invariant entity, which is a common sub-circuit for different topologies, as shown in Figure 1.15 (a). Then the three-terminal equivalent circuit is derived to represent the small signal behavior of this common sub-circuit in current mode control power converter, as shown in Figure 1.15 (b). Therefore, all transfer functions, including input impedance can be examined and small signal model for other commonly used topologies, such as boost and buck-

boost with current mode control can be also easily obtained.



(a)



(b)

Figure 1.15 Unified three-terminal switch model for current mode control (a) three-terminal switch block in Buck converter (b) small-signal model for three-terminal switch block [C34]

Three-terminal switch model can be used to predict small-signal characteristics of constant on-time current mode control. For constant on-time current mode control, R_e is always positive which means that there is no instability issue, C_e and L_s forms a double pole at high frequency. The simplified control-to-output transfer function for constant-on-time current mode control is shown as follows:

$$\frac{v_o(s)}{v_c(s)} \approx K_c \frac{R_{Co}C_o s+1}{s/\omega_a+1} \frac{1}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}} \tag{1.1}$$

Where $\omega_1=\pi/T_{on}$, $Q_1=2/\pi$. From (1.1), the location of double poles is determined by T_{on} and the quality factor is always positive which means that the double poles never move to the right

half plane. From the bode plots shown in Figure 1.16, for constant on-time current mode control, the current loop is always stable and no sub-harmonic oscillation occurs.

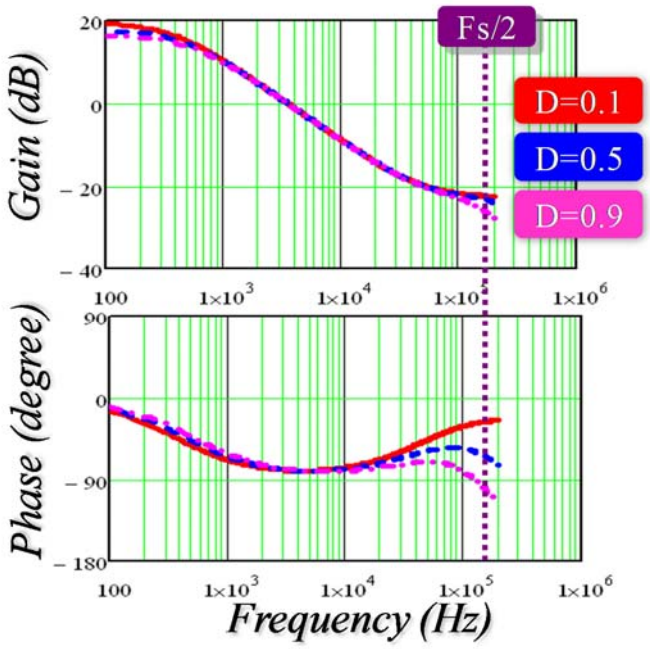


Figure 1.16 The bode plots of control-to-output transfer function for constant on-time current mode control with different duty cycles

From above analysis, for constant on-time current mode control, no external ramp compensation is required as peak current mode control. As a consequence, the equivalent circuit model shown in [C32][C34] does not include the case for constant on-time current mode control with external ramp compensation. However, for multi-phase constant on-time current mode control, the situation is different. For multi-phase application, pulse distribution method is widely used in industry [C13][C14][C28], for this method, external ramp is required to improve jittering performance in some applications but it also affects the dynamics of the system (the details will be presented in Chapter 2). For quantitative analysis and optimal design purpose, an accurate small-signal model is indispensable. For previous small-signal models for constant on-time current mode control, which includes Redl's analysis based on injected-absorbed current method [C29],

Ridley's modified average model [C31], Voperian's current-controlled PWM switch model [C30], Li's equivalent circuit model based on describing function [C32], Yan's three-terminal switch model [C34], none of them includes external ramp compensation as the external ramp is rarely used at that time. Up to now, there is no literature talking about the effect of external ramp on the dynamic behavior of constant on-time current mode control. As a result, no good equivalent circuit model is proposed for constant on-time current mode with external ramp compensation. Chapter II of the dissertation will try to solve this remaining challenge for constant on-time current mode control.

1.2.2 Literature survey on modeling of V^2 control

As discussed in section 1.1, V^2 control has advantages of simple implementation and fast transient response and is widely used in industry for POL and VR applications. However, it has potential issue which is related to the feedback of capacitor voltage ripple. As shown in Figure 1.17, the feedback output voltage contains two parts: The ESR voltage as shown is the red triangular waveform. It is formed by capacitor current flowing through the ESR of output capacitors. As the load resistor is usually much larger than ESR, almost all of the AC inductor switching current flows through the output capacitor. So the ESR ripple voltage has similar waveform as inductor current and it contains inductor current information. The other part in is the voltage over the pure capacitance. This voltage is formed by integration of the capacitor current over the output capacitance and it has 90 degree additional phase delay compared with the ESR ripple information. Therefore, in V^2 implementation, the nonlinear PWM modulator is much more complicated than current mode control, since not only is the inductor current information fed back to the modulator but also the capacitor voltage ripple information. For constant on-time current mode control, no sub-harmonic oscillation is shown in the current loop. However, for constant on-

time V^2 control, when the capacitor ripple is dominant, sub-harmonic oscillation can be observed in simulation due to the delay effect of the capacitor. For example, at 300kHz switching frequency and 0.1 duty cycle, if using OSCON caps (560uF/6mΩ), the circuit is stable; if using ceramic caps (100uF/1.4 mΩ), sub-harmonic oscillation occurs, as shown in Figure 1.18 .

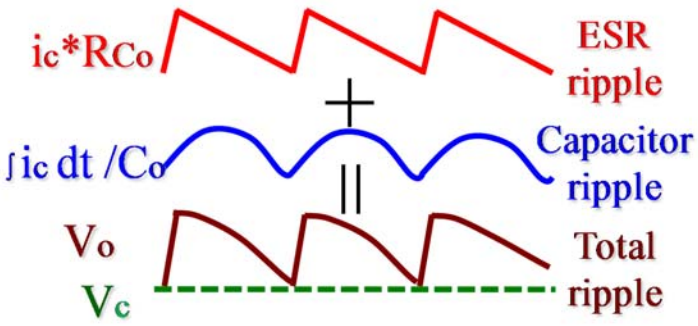
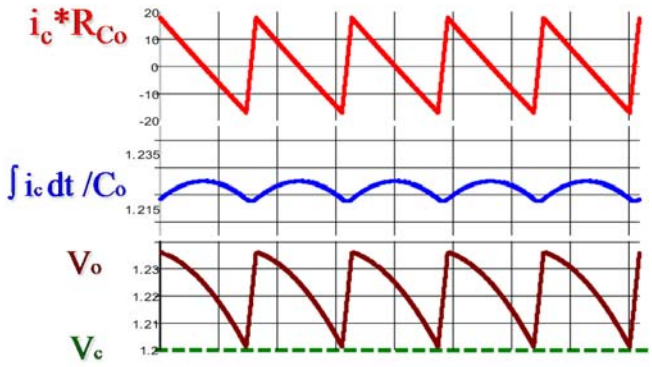
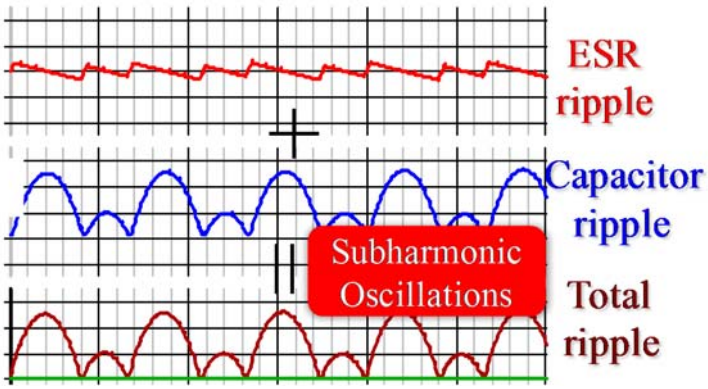


Figure 1.17. Feedback output voltage waveform of V^2 control.



(a)



(b)

Figure 1.18 Comparisons of waveforms for constant on-time V^2 control with different caps when F_{sw}=300kHz; D=0.1; (a) OSCON Cap (560uF/6mΩ) (b) Ceramic Cap (100uF/1.4 mΩ)

The modeling of V^2 control is even more complicated than current mode control due to the complexity of PWM modulator. A lot of literatures have been published to provide a simple and accurate small-signal model. The early models proposed in [D15][D16][D17][D33] directly use Ridley's extension model for constant frequency V^2 peak control, as shown in Figure 1.19. The same sample & hold block of peak current mode control is used without justification. Generally speaking, extension of R. Ridley's model is not applicable for V^2 implementation, since this model is based on constant-frequency discrete-time analysis, which just consider the sideband information of the current loop and does not consider the influence of the capacitor ripple. This is why the models used in [D15][D16] [D17][D33] cannot accurately predict the influence from the capacitor ripple in constant frequency V^2 peak control. For constant on-time V^2 control, Ridley's extension model fails to predict the small-signal behavior, as shown in Figure 1.20.

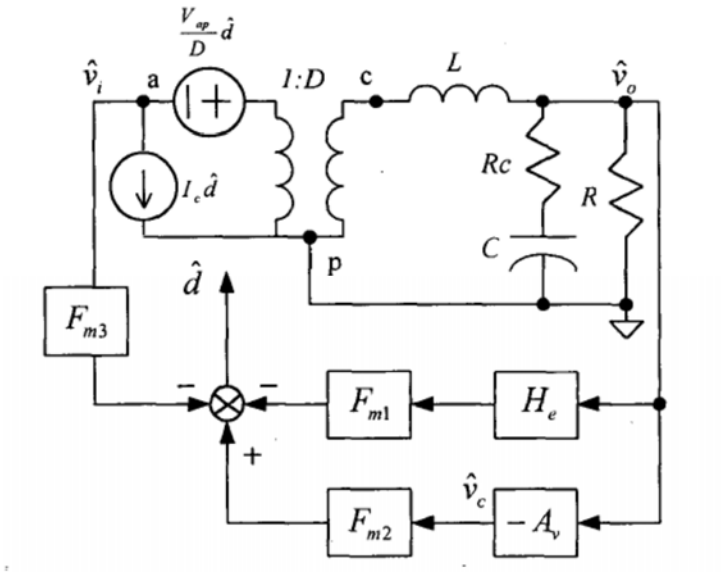


Figure 1.19 Extension of R. Ridley's model to V^2 control in [D33]

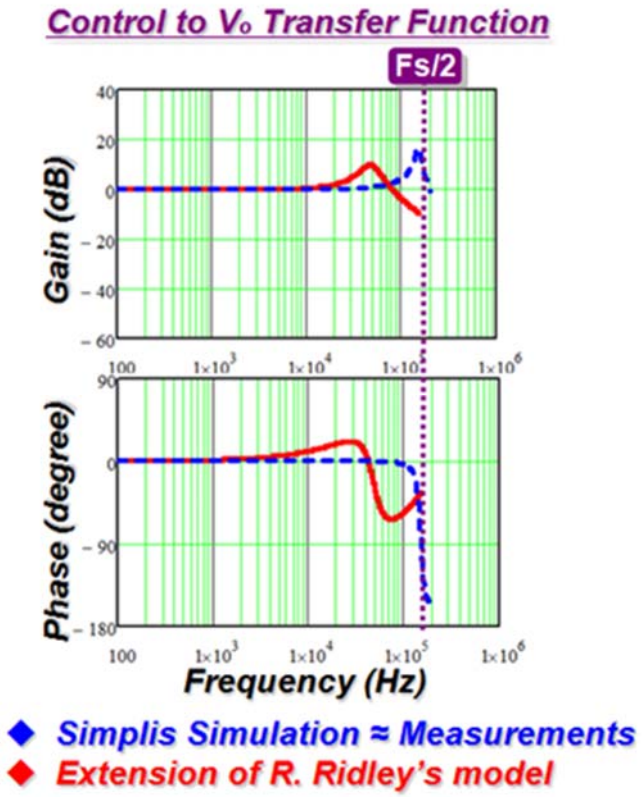


Figure 1.20 Extension of R. Ridley's model to constant on-time V^2 control

To accurately predict the influence from the capacitor voltage ripple in V^2 control, several methods are proposed: In [D12], Krylov–Bogoliubov–Mitropolsky algorithm is used to reconstruct the switching ripple from state-space averaged models and therefore to improve the accuracy of the model. However, it is too complex for practical use. Besides, the conclusion shown in [D12] is only applicable in constant frequency V^2 control and no small-signal model and design analysis is presented for constant-on-time V^2 control. In [D13][D38]-[D41], the sampled-data modeling techniques are employed to derive the stability criterion by judging whether the eigenvalues are less than unity in discrete-time domain. For sampled-data modeling method, it is conducted in discrete-time domain and it is difficult for practical engineers. In [D35]-[D37], the general discrete-time analysis is applied on to constant frequency V^2 valley control and constant on-time V^2 control. In [D42], accurate analysis based on discrete time modeling and Floquet theory is presented. However, these discrete-time analyses are based on numerical analysis and no symbolic expression can be extracted and very little physical insight is provided. In [D43]- [D45], the time domain analysis is used based on the calculation of the inductor current information, the compensation ramp and the charge variation of the output capacitor, as shown in Figure 1.21. The model based on this method can accurately predict the stability criterion of V^2 control and the magnitude of the ramp compensations to avoid instability. However, only the critical stability point can be predicted and no design guideline can be provided with a certain stability margin.

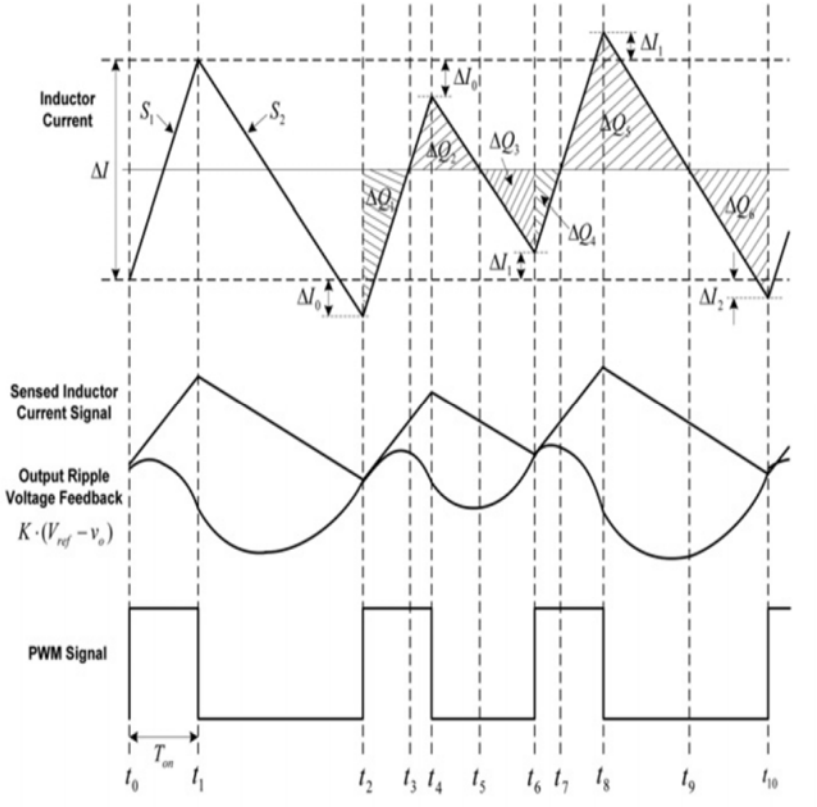


Figure 1.21 Modeling concept for V^2 control based on time domain analysis [D43]

For most of power electronics engineers, continuous domain small signal analysis is preferred, as in the voltage mode control [B2] and current mode control [C32]. The most successful continuous domain small signal model of V^2 control is derived based on describing function method by Dr. J. Li [D46], which is an extension of the modeling work for current mode control [C32]. In order to capture the nonlinearity of the circuit, the power stage as well as the inner voltage feedback is considered as a single entity. By doing this, the influence from capacitor voltage ripple is considered and included in the modeling process. The modeling concept is shown as in Figure 1.22. A small-signal sinusoidal perturbation is injected into the control signal, and the time domain output voltage variation is calculated. After the time domain relation between control signal perturbation and output voltage variation is obtained, the time domain relation is transferred into frequency domain using Fourier analysis.

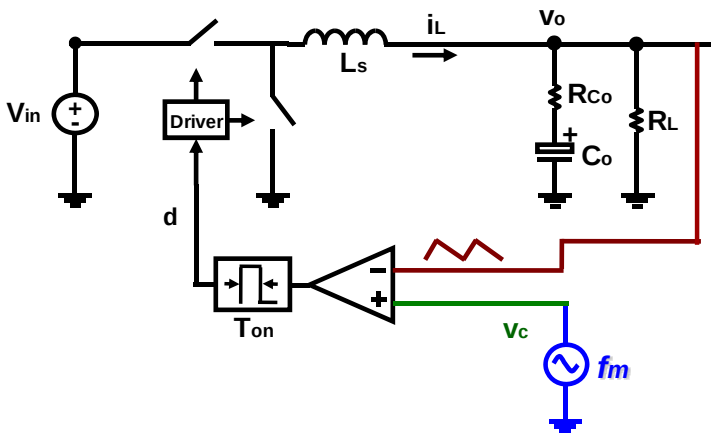


Figure 1.22 Modeling concept for constant on-time V^2 control based on describing function method [D42]

The control-to-output and output impedance transfer functions of V^2 control are derived and summarized in [D46]. The instability issue when using ceramic capacitors can be well predicted. External ramp compensation and current ramp compensation are proposed in [D46] as two solutions to eliminate sub-harmonic oscillations and the small-signal models are also derived based on time-domain describing function. In [D49], the describing method is extended to V^2 control with composite capacitor case. Although describing function methods have already been successfully applied to V^2 control to predict instability problem, however, the model is incomplete as audio susceptibility and input impedance are still lacking. Furthermore, as all the feedback information is lumped together with complicated mathematical derivation, little physical insight is provided. Besides, the mathematical derivation of this model is very complicated and time consuming. The tedious re-derivation process limits its application to the modified version of V^2 control. As an example, for Texas Instruments' D-CAP2 control products, a current sensing network with a high pass filter is added into the original V^2 control. Up to now, there is no small signal model published for this control structure based on describing function method.

Equivalent circuit model, on the other hand, can eliminate all the previous disadvantages and has already been a powerful tool for analysis of DC-DC converters with traditional voltage mode

control [C36] and current mode control [C34]. For equivalent circuit model of V^2 control, however, no satisfactory result has been proposed. A design-oriented equivalent circuit model for V^2 control is proposed in [D47] as shown in Figure 1.23. A significant issue of this equivalent circuit model is that it failed to explain the output impedance characteristic of V^2 control, as shown in Figure 1.24. Furthermore, transfer functions related to input property, such as input impedance, are not included in this incomplete model.

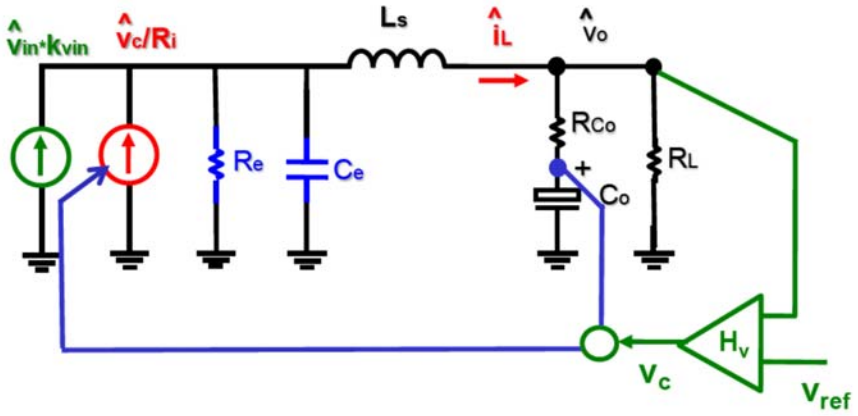


Figure 1.23 Design-oriented equivalent circuit model of V^2 control in [D47].

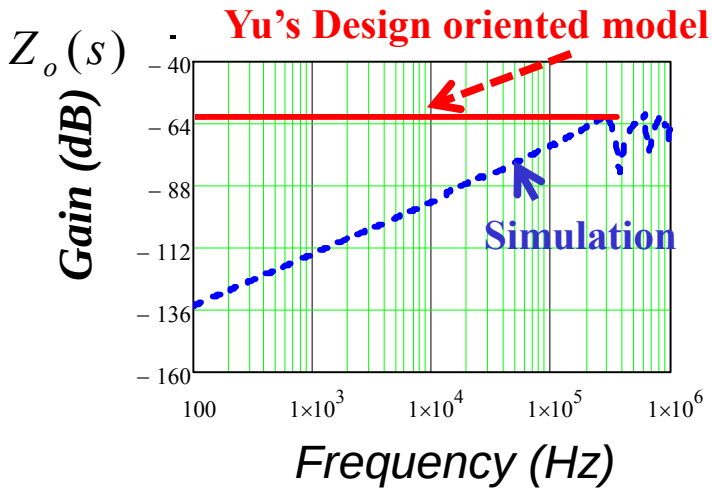


Figure 1.24 Inaccuracy of the output impedance in [D47].

In [D48], an equivalent circuit model based on current mode control is proposed for V^2 control, as shown in Figure 1.25. For capacitors with large RC time constant, such as Tantalum capacitor and OSCON Capacitor, this model is accurate and can predict the output impedance, as shown in Figure 1.26. However, the derivation of the model makes an assumption that the voltage ripple across the pure capacitance is negligible comparing with the voltage ripple across the ESR. Therefore, the model is not applicable to capacitors with small RC time constant, such as ceramic capacitors. As shown in Figure 1.27, Yan's equivalent circuit model fails to predict the double pole at high frequency and is not applicable in general for ceramic capacitors.

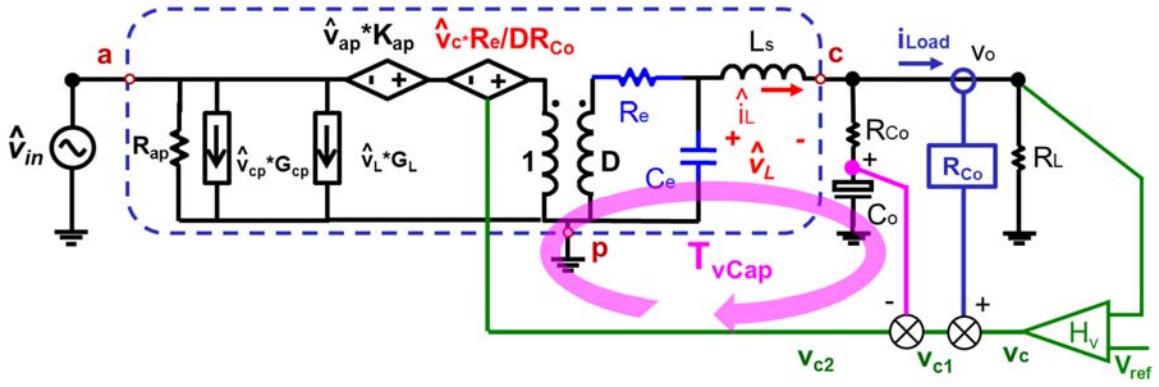


Figure 1.25 Equivalent circuit model of V^2 control based on current mode control model [D48]

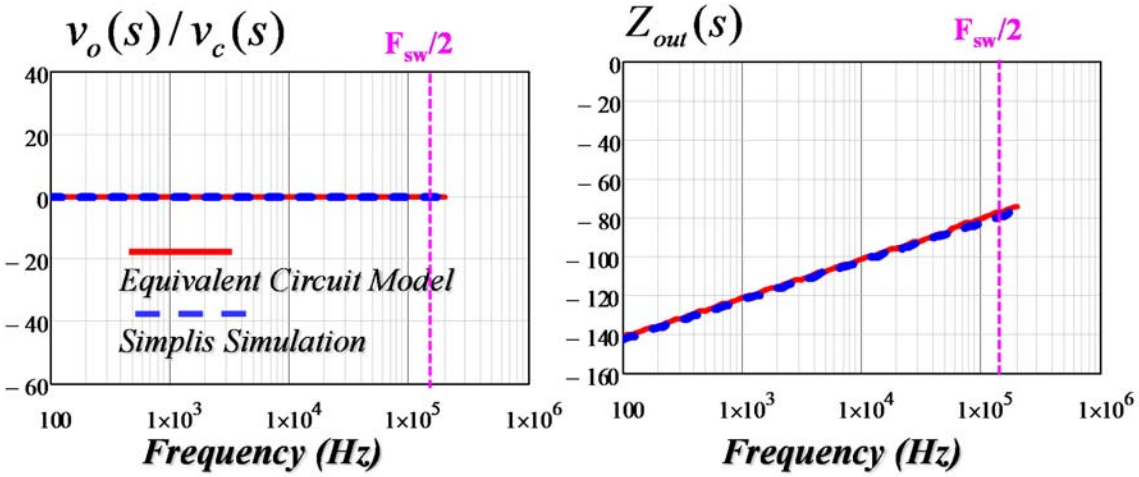


Figure 1.26 Verification of Yan's Equivalent circuit model of V^2 for Tantalum capacitor (1mF/20mΩ) [D48]

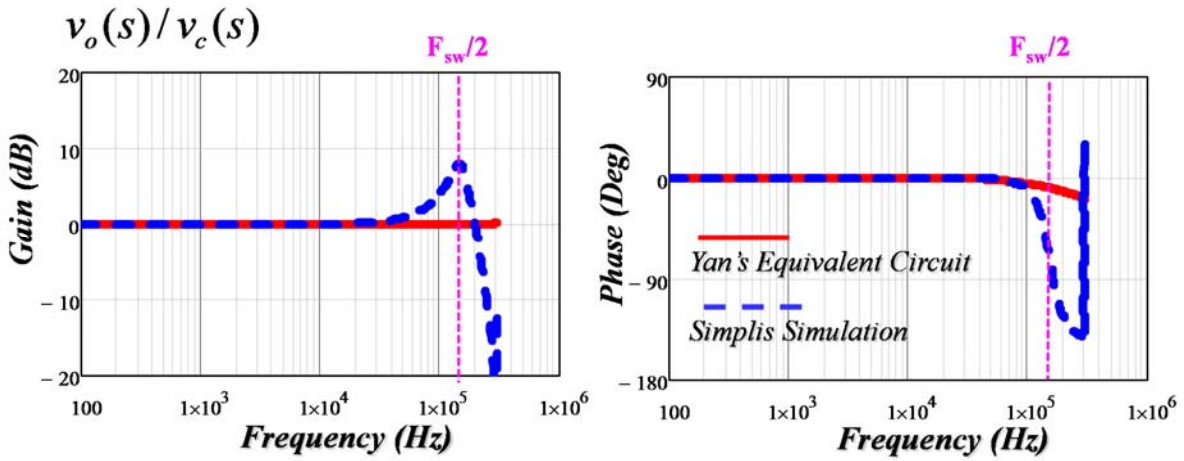


Figure 1.27 Inaccuracy of Yan's Equivalent circuit model of V^2 for Ceramic capacitor (220uF/3mΩ)

However, in many applications such as digital camera, netbook, cellular phone, ceramic caps are preferred due to its small size and small output voltage ripple requirement. Up to now, there is no good equivalent circuit model provided for V^2 control which is able to predict the instability problem and can be utilized to design ramp compensations for Ceramic capacitor application. Deriving an equivalent circuit model which is applicable to V^2 control with different kinds of capacitors is a remaining challenging task for researchers.

Chapter III of the dissertation tries to derive a unified equivalent circuit model for V^2 control. The model considers the influence of capacitor voltage ripple and is applicable for all kinds of capacitors and with different modulation schemes (including variable switching frequency V^2 and constant frequency V^2 control). Chapter IV discusses optimal design considerations and performance comparison of V^2 control with different modulation schemes, based on the proposed unified equivalent circuit model.

1.2.3 Literature survey on modeling of resonant converters

As discussed in section 1.1, series resonant converters are widely used for power conditioning in the aerospace industry and LLC resonant converters are widely used in front-end DC-DC

converters. Most of the DC power conditioning applications involve a regulated voltage output, therefore a feedback loop is incorporated into the control system to stabilize the output voltage. For optimal design purpose, small-signal models are indispensable.

However, State-space averaging method [B2][B3], which is a popular approach for power stage modeling of PWM converters, breaks down for resonant converters. The reason is that for resonant converters, some of the state variables do not have dc components but contain strong switching frequency harmonics, whereas the dc components are the dominant parts of the state variables for PWM converters.

Numerous research efforts are spent to investigate steady state and small signal AC model on series resonant converter: In [E8][E9], King presents a complete steady state analysis of the series resonant converter based on diode-conduction-angle control, or α control. Normalized curves for various currents and voltages are plotted as a function of the circuit parameters to help design. In [E5], switching frequency control or γ control is proposed and it is found that it has certain advantages over the older α control. Some of these include the relative simplicity, freedom from imbalance problems, and inherent current limiting characteristics [E10]. Verperian and Cuk derived the first complete solution for the DC conversion ratio of the series resonant converter with switching frequency control [E11]. In the analysis, voltage conversion ratio M is plotted versus the switching frequency for constant values of load resistance, based on numerical solution of implicit equations. The result is shown in Figure 1.28. This approach is similar to the analysis of pulse width modulated converters in which M is plotted as a function of the duty ratio. Later, Witulski[E12] presented an alternative steady state analysis of the series resonant converter with switching frequency control, in which the characteristics are plotted in the output plane, i.e., output current I_{out} is plotted versus output voltage V_{out}. The advantage is that the output characteristics

have a particular simple solution in closed form. As a result of these efforts, the steady-state behavior of series resonant converter is well understood to power electronics society.

For the small-signal AC analysis, the situation is more complicated. Due to the strongly oscillatory nature of resonant states, the switching frequency interacts with the natural resonant frequency. This results in an interesting phenomenon which is often referred to as the beat frequency dynamics [E13]. This interaction cannot be investigated using the averaging concept because it eliminates the switching frequency information.

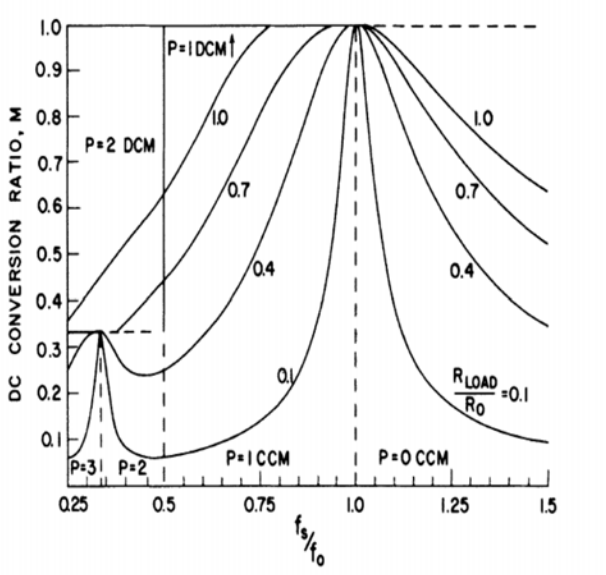


Figure 1.28 DC conversion ratio M versus switching frequency for series resonant converter [E11]

Several methods are presented to successfully capture beat-frequency dynamics: the first method is proposed by Vorperian from combination of state space analysis without linear ripple approximation in time-domain and discrete-time analysis [E13]. The modeling results of control-to-output voltage and input to output voltage transfer functions are shown to be very accurate experimentally with the capability of capturing beat-frequency dynamics, as shown in Figure 1.29. However, the results obtained are computed numerically because of the occurrence of functions of matrices which are difficult to determine in expression form. The second is sample-data method

or discrete-time analysis [E14] - [E17]. The discrete model captures the inherent sampling nature and can predict the small-signal behavior up to switching frequency. However, the sampled-data analysis and discrete analysis technique is very difficult to extract physical insight and is too complex for practical use. The third method is generalized averaging concept [E18][E19]. An effort was made by S. Sander [E18] to extend the state-space averaging technique to model the resonant converters. The derived model can correctly predict the beat frequency dynamic, however, it only propose the modeling concept and did not propose a method to implement the concept in the general case. Later, J. Sun proposed a similar averaged modeling concept based on the so-called slowly varying amplitude and phase transformation technique. The result is accurate but only numerical solution can be used to plot the transfer function. The fourth method is the extended describing function method by E. Yang [E20]. The describing function technique is extended to a more generalized multi-variable case, where state variables are represented by some limited number of harmonic terms. The modulation frequency is limited to one-half of the output ripple frequency from the harmonic balance point of view. Compared with experimental results, this method can predict beat frequency dynamics very accurately, as shown in Figure 1.30.

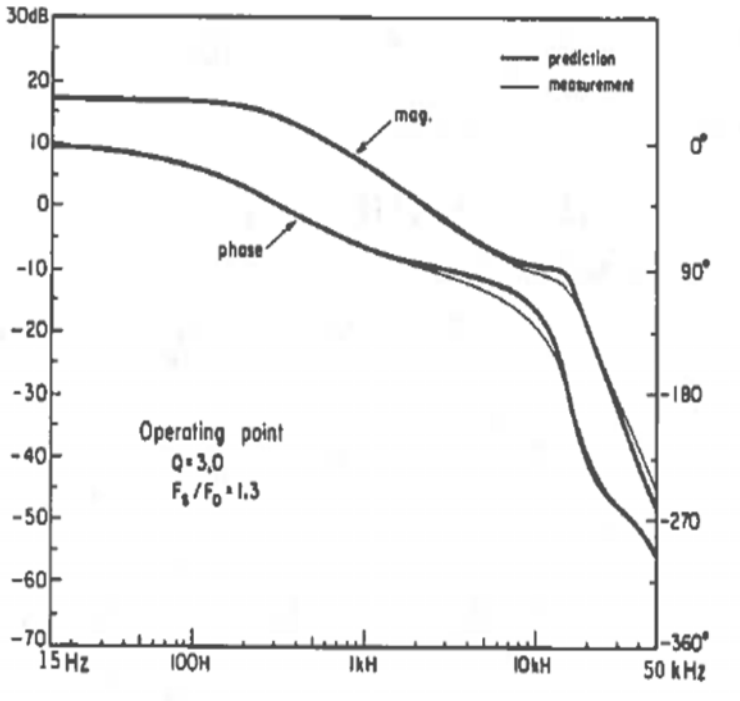


Figure 1.29 Control-to-output voltage verification using state-space analysis by Vorperian.[E13]

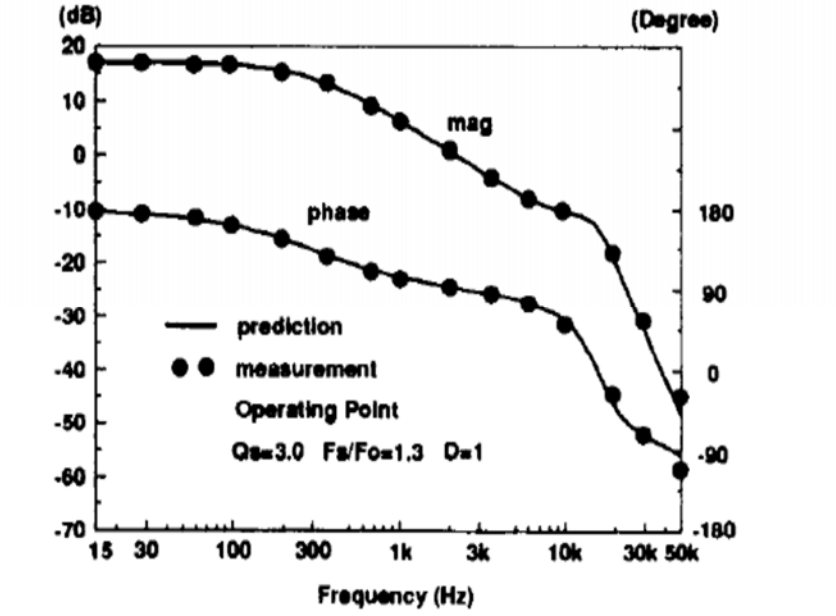


Figure 1.30 Control-to-output voltage verification using extended describing function by E. Yang [E20]

Although small signal models shown in [E13] - [E20] are accurate enough to capture beat frequency dynamics, none of the models is widely used as all of them have complicated

mathematics instead of using a circuit-oriented way. Therefore, little physical insight can be extracted from these models. Efforts have also been spent to modify or extend these methods to gain some physical insights and are summarized as follows: In [E21], an approximated model based on intuition was proposed by Vorperion and it provides good physical insight for low-frequency pole and is able to capture the beat frequency dynamics. As shown in Figure 1.31 (b), the low frequency behavior is determined by a single pole composed primarily by load and output capacitor. This approach is a good combination of simplicity and accuracy, but nonetheless is an approximation and relies on an intuitive rather than a formal derivation. Moreover, the model is not accurate when the switching frequency is close to the resonant frequency, as shown in Figure 1.32. In [E22][E23], a low frequency continuous time two-port y parameter equivalent circuit model is proposed by Witulski based on discrete time result, as shown in Figure 1.33. However, as show in Figure 1.34, this equivalent circuit model is only accurate when perturbation is at low frequency and it can not predict beat frequency dynamics. In [E24], a new modeling technique based on Phasor transformation is proposed by Rim. This approach gives explicit and simple equations with fruitful physical insight. The model captures low-frequency dynamics of SRC: In the case that switching frequency deviates from resonant frequency, the SRC is modeled as the first order, and in the case of resonance the SRC is modeled as the second order. As shown in Figure 1.36, the time domain simulation verifies the circuit order change when the steady state changes. However, the high frequency beat frequency dynamics can not be seen easily in time domain simulation and the information is lost in the equivalent circuit model. Therefore, it is not accurate enough for high-bandwidth design.

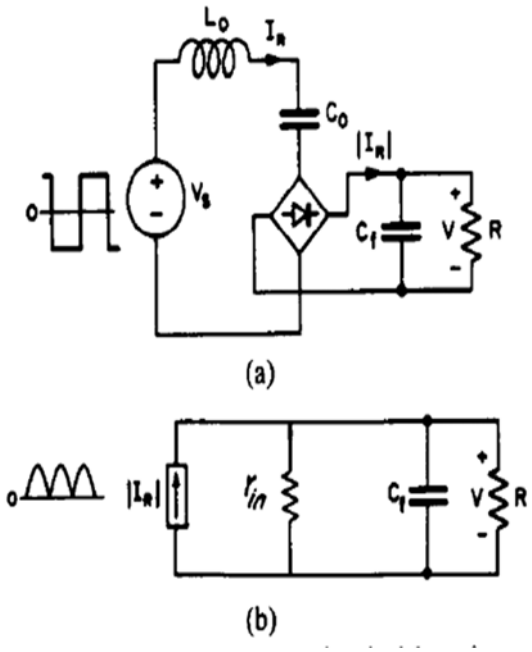


Figure 1.31 (a) Series resonant converter as circuit driven by square voltage source (b) equivalent circuit for determination of low-frequency pole proposed by Vorperian. [E21]

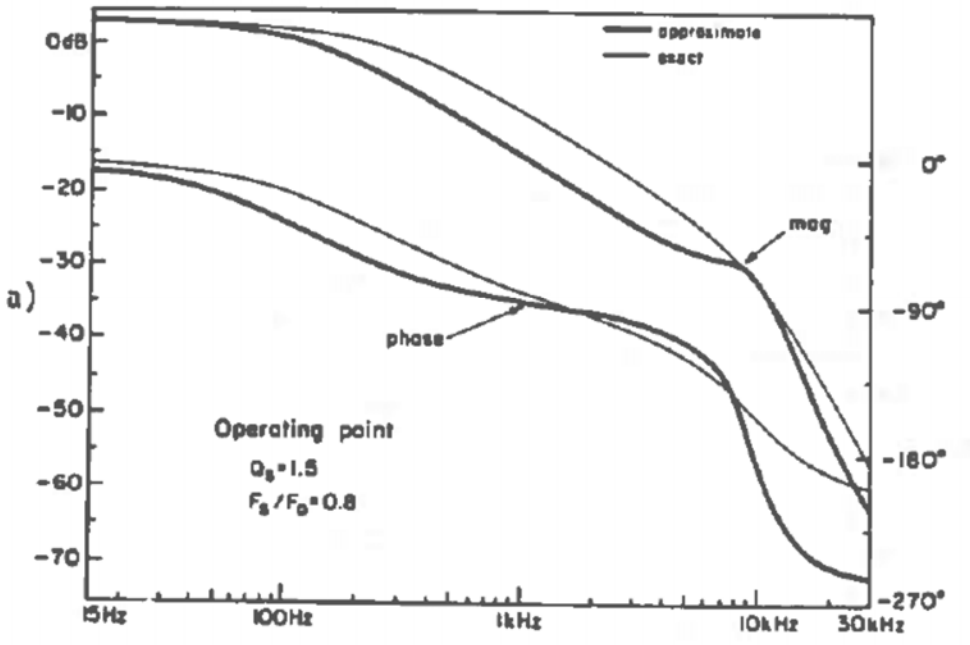


Figure 1.32 Breakdown of approximate control-to-output voltage for operating points close to resonant frequency

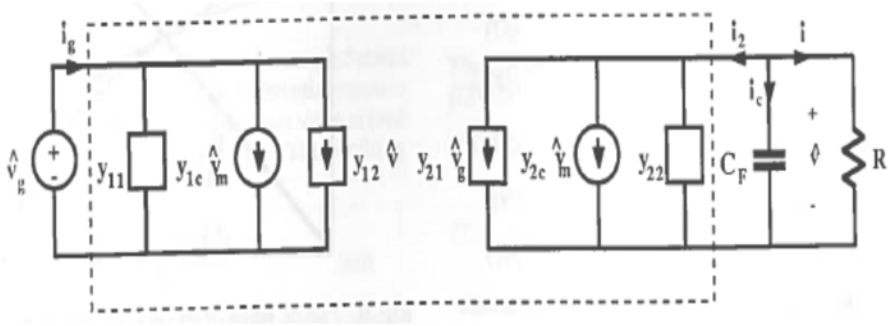


Figure 1.33 A low-frequency y parameter equivalent circuit model proposed by Wiltuski [E23]

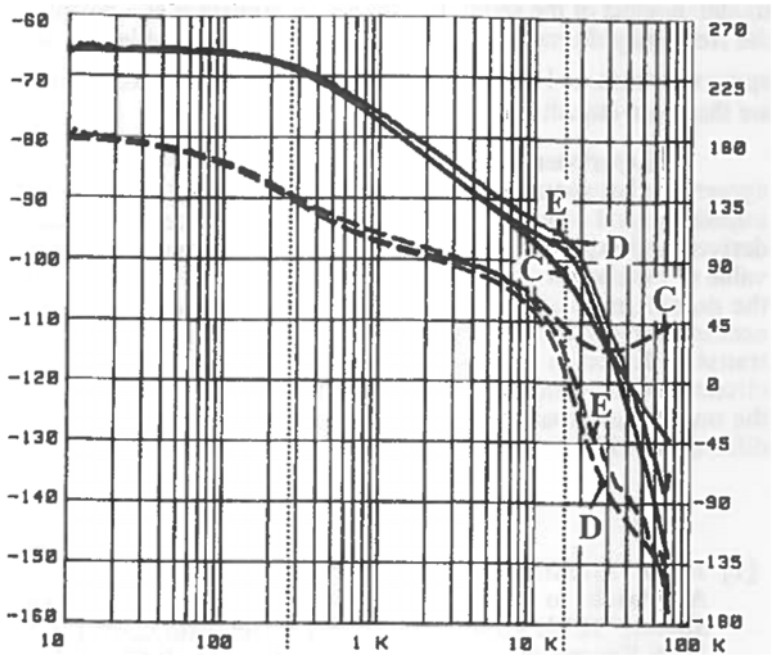


Figure 1.34 Accuracy of low-frequency y parameter equivalent circuit proposed by Wiltuski [E23] (C is model prediction while E is experimental data)

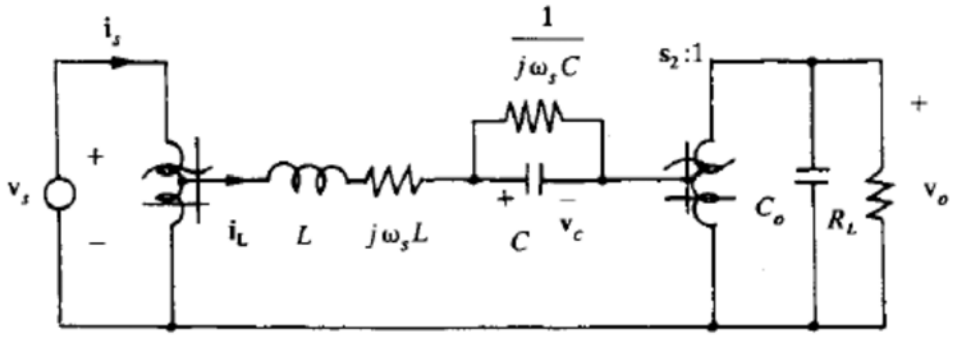
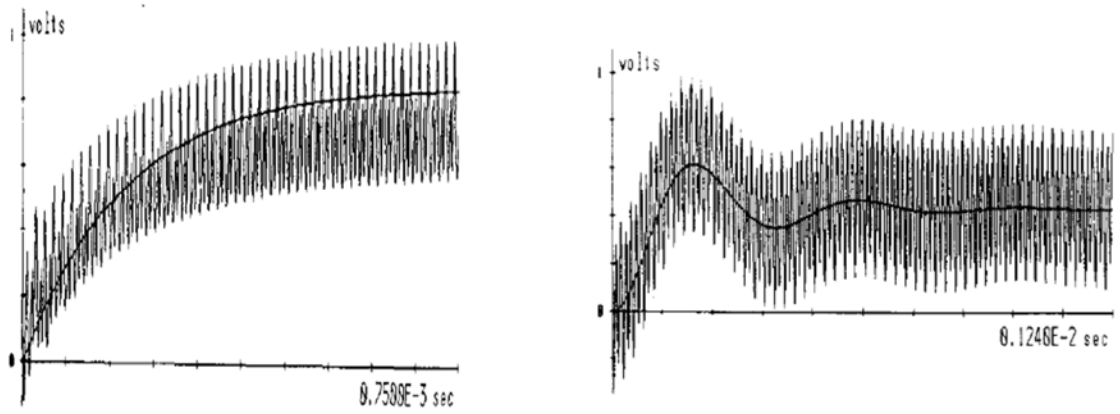


Figure 1.35 Phasor transformed SRC by Rim [E24]



(a) (b)

Figure 1.36 Step response simulation results (a) f_s/f_o=1.65, first order response (b) f_s/f_o=1.0, second order response [E24]

In [E26], the equivalent circuit model for SRC is proposed by E. Yang, based on the small-signal modeling results by the extended describing function concept as shown in Figure 1.37. The small-signal model equivalent circuit model can well capture the beat frequency dynamics and is as accurate as the describing function result. One example is shown in Figure 1. 38 under the following parameters: V_{in}=400V, L=197uH, C=51nF, C_f=32μF, R_C=0mΩ, R=15.5Ω, Ω_o=50.2kHz, Ω_s=1.2Ω_o. All four transfer functions, i.e. control-to-output, audio susceptibility, output impedance and input impedance are compared. The predictions can match with simplis simulation results very well up to switching frequency.

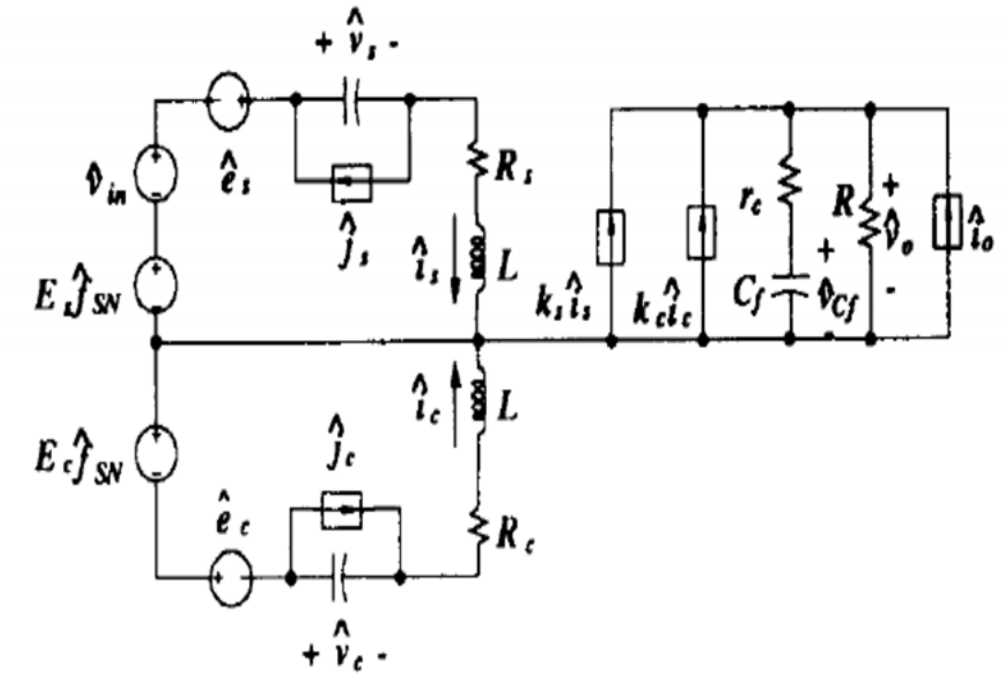


Figure 1.37 Small-signal equivalent circuit model proposed by E. Yang [E26]

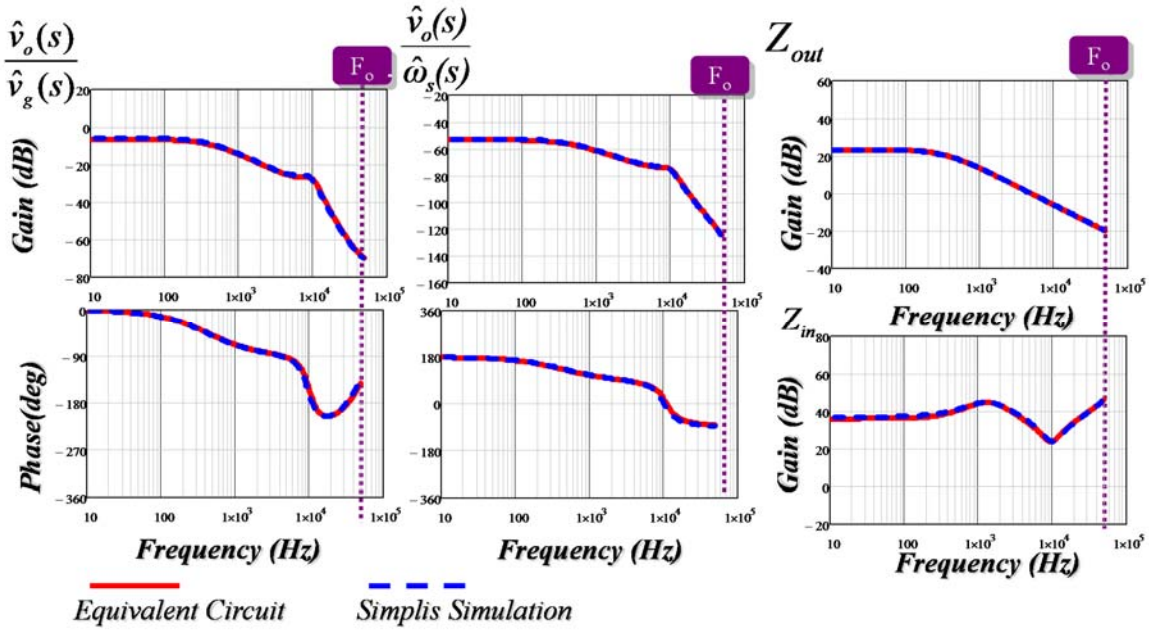


Figure 1. 38 Simplis simulation verification of equivalent circuit model proposed by E. Yang for Ωs=1.2Ωo [E26]

The major shortcoming of equivalent circuit model shown in [E26] is the higher than usual order of the model. From Figure 1.37, the equivalent circuit model is a fifth-order circuit as there

are five energy storage elements. However, from the results shown in [E26], the small-signal behavior is sufficient to be described as a third-order circuit, which is also proved in [E19], where numerical solution shows that third-order transfer function using higher order averaging method is almost as accurate as the results by extended describing function method. Therefore, the equivalent circuit model is still too complicated to extract fruitful physical insight. Furthermore, the transfer functions are still derived based on numerical solution and no explicit analytical solutions are provided for design purpose.

Chapter V of this dissertation tries to take the advantage of the accurate results of the equivalent circuit model shown in [E26] and overcome the shortcomings related with it. The following two major objectives will be achieved: (1) Simplify the small-signal equivalent circuit model of SRC to a third-order circuit which is simpler but accurate enough to predict beat frequency dynamics. (2) Provide analytical expressions for all transfer functions to help engineers to design the feedback loop.

For LLC resonant converters, as this topology is more and more popular, a lot of research efforts have been spent on control and design, such as the design of the power stage parameters [F17], design of the transformer [F18], synchronous rectifier driving scheme [F19], the burst mode [F20] and start up control [F21][F22]. For the small-signal analysis, although numerous research efforts have been spent recently on this topic, only a few papers are published to discuss about the equivalent circuit models and the small-signal behaviors. The reason is that the small-signal behavior of LLC resonant converter is even more complicated than series resonant converter due to the effect of magnetizing inductor. In [F23]-[F26] , extended describing function concepts are extended to LLC resonant converter, however, all the models proposed in these papers using numerical solution and no analytical transfer functions are derived for understanding and design

purpose. Besides, the equivalent circuit models presented are seven-order system which is way too far complicated for practical use. In [F27], a novel approach based on communication theory is presented to determine the small signal model of an LLC resonant converter, in this approach, the variable switching frequency control method is analogous to frequency modulation (FM) and the effects of the resonant tank filter are analogous to amplitude modulation (AM). The derivation of control-to-output transfer function is presented. However, the final expression is not closed-form which is too complex for practical use. Moreover, no other transfer functions, such as output impedance, input to output voltage are presented. In [F28], sampled-data modeling approach is employed for small-signal analysis of the LLC resonant converter. The discrete model captures the inherent sampling nature and can predict the small-signal behavior up to switching frequency. However, the sampled-data analysis and discrete analysis technique is very difficult to extract physical insight and is too complex for practical use. In [F29], analysis of small-signal behavior of LLC resonant converters working under different conditions (i.e. below, close to or above switching frequency) are conducted based on Simplis simulation results. The accuracy of this method is without any question as the results are directly from time-domain simulation software and the effect of the parameters on small-signal behavior can be qualitatively analyzed. The drawback of this method is lack of physical insights and lack of analytical tool for compensation design. To sum up, up to now, no simple and accurate small-signal equivalent circuit model is available for LLC resonant converters. No analytical expressions of transfer functions are available for LLC resonant converters to aid the control design. In industry, engineers have to use the real bench measurements of the control to output voltage transfer function for feedback compensator design [F30], which is very time-consuming due to the insufficient understanding and lack of good design tool.

Chapter VI of this dissertation tries to extend the simple equivalent circuit model shown in Chapter V to LLC resonant converters. The equivalent circuit model can serve as a useful design tool for feedback design. A third-order equivalent circuit model of LLC will be derived and analytical expressions for all transfer functions will be presented when switching frequencies are above, close to and below resonant frequency.

1.3 Dissertation Outline

As discussed in previous chapter, numerous research efforts have already been spent on modeling of constant on-time current mode control, V^2 control and resonant converters. For each area, there still remains some challenging issues and this dissertation try to take cracks on these challenges. This dissertation consists of seven chapters. They are organized as follows: First, the application background and history of the small-signal modeling of constant on-time current mode control, V^2 control and resonant converters are introduced in Chapter 1. Next, a three-terminal equivalent circuit model for constant on-time current mode control with external ramp compensation is proposed in Chapter 2. Then, unified three-terminal equivalent circuit model for V^2 control is proposed in Chapter 3. Based on the unified equivalent circuit model, design considerations and performance comparisons between different modulations of V^2 controls are presented in Chapter 4. After that, a simplified equivalent circuit model of series resonant converter is proposed in Chapter 5. In Chapter 6, the equivalent circuit model of LLC resonant converter is proposed. Chapter 7 summarizes the work of this dissertation.

The detailed outline is elaborated as follows:

Chapter 1 is the review of application background of constant on-time current mode control, V^2 control, resonant converters and their modeling technologies. Constant on-time current mode control and V^2 control are widely used as POL converters and VR regulators in DPS systems.

Series resonant converters are widely used in aerospace systems and LLC resonant converters are widely used as Front-end converters in DPS systems. Simple and accurate equivalent circuit models are indispensable to design these converters. However, available models can only solve partial issues. Up to now, no good equivalent circuit model for constant on-time current mode control with external ramp is proposed. No good equivalent circuit model for V^2 control is proposed. And the available Yang's equivalent circuit model for resonant converter needs significant simplification for practical use. The primary objective of this dissertation is to develop equivalent circuit models for high frequency PWM converters (including constant on-time current mode control and V^2 control) and resonant converters.

In Chapter 2, the original three-terminal switch model for current mode control is extended to constant on-time current mode control with external ramp compensation case. External ramp compensation is utilized as a simple solution to alleviate jittering problem in commercial products for multi-phase constant on-time current mode control based on pulse distribution structure. However, the external ramp also affects the dynamic performance of the circuit. The effect of the external ramp is first analyzed by the accurate small signal model based on describing function method. Then a simple and accurate three terminal switch model for constant on-time current mode control with external ramp compensation is proposed. The model adds a simple R-L branch on the original three-terminal switch model to represent the effect of external ramp. The equivalent circuit model can be reduced to previous unified three-terminal switch model when external ramp is zero and can be reduced to model of constant on-time voltage mode control when external ramp is much larger than inductor current ramp. It will serve as a useful tool for understanding the effect of external ramp and designing feedback control appropriately.

In Chapter 3, a unified equivalent circuit model for V^2 control is proposed. The equivalent circuit model is suitable to all kinds of capacitors as it considers the effect of both inductor current ripple and capacitor voltage ripple. The equivalent circuit model has clear physical meaning which shows that the inductor current feedback turns the power stage into a non-ideal current source, while the capacitor voltage feedback turns the non-ideal current source into a non-ideal voltage source. The equivalent circuit model is a simple yet accurate, complete model and can be used to investigate all transfer functions. The proposed equivalent circuit model is applicable to both variable frequency modulation and constant frequency modulation. Furthermore, the model can be extended to enhanced V^2 control and muti-phase V^2 converters. Besides, as ripple based control is just V^2 control without using the outer loop compensation, the model is also applicable for all kinds of ripple based control.

In Chapter 4, based on the proposed unified equivalent circuit model, design guidelines of ramp compensations for constant on-time V^2 control is proposed for ceramic capacitor applications. For constant frequency V^2 peak control, the physical causation of two pairs of double poles are identified and explicit stability criterion is presented. Optimal design strategies are proposed, both for Oscon capacitor and ceramic capacitor applications. For the first time, it is found that different design strategies should be used with different capacitors. For OSCON capacitors, designing external ramp appropriately is adequate, while for ceramic capacitors additional current ramp is required to control the stability margin. Moreover, the capacitor tolerance effects are analyzed for practical consideration. In addition, the small-signal characteristics are compared between constant on-time V^2 control and constant frequency V^2 peak control.

In Chapter 5, a simplified equivalent circuit model is proposed for Series Resonant Converter (SRC). The simplified equivalent circuit model is a third-order equivalent circuit and is accurate

enough to predict beat frequency dynamics. Analytical expressions are provided for all transfer functions to understand the effect of circuit parameters and design the feedback loops appropriately.

In Chapter 6, the simple equivalent circuit model is also extended to LLC resonant converter. When the switching frequency is at or above resonant frequency, the behavior of LLC resonant converter is very similar as SRC since only Lr and Cr participates in resonance. As a result, the equivalent circuit model is very similar and the only difference is that the existence of L_m will affect the low frequency gain of the transfer function. When the switching frequency is below resonant frequency, there will be a certain time period that L_m also participates in resonance and therefore it is a multi-resonant topology conceptually. A modified equivalent circuit model is proposed to accommodate the change of operation modes. The model shows that not only low frequency gain but also the poles of the transfer function will be affected by L_m. Analytical expressions are provided for all transfer functions to understand the effect of circuit parameters and design the feedback loops appropriately.

Chapter 7 is the summary of this dissertation.

Chapter 2. Three-Terminal Switch Model of Constant on-time Current Mode with External Ramp Compensation

2.1 Introduction

Multi-phase constant on-time current mode control based on pulse distribution structure is widely used in VR application for microprocessor [C13][C14][C28]. The structure is shown as Figure 2. 1 and the steady-state waveform for a two-phase constant on-time current mode control is shown in Figure 2. 2. The switch turn off instant is determined by the on time and the switch turn on instant is decided by the comparison of the total inductor current and the control signal from feedback. The pulse distribution scheme sends the first turn on instant to the first phase and the second turn-on instant to the second phase. By this way, the implementation is simple and it is capable of automatic interleaving between different phases.

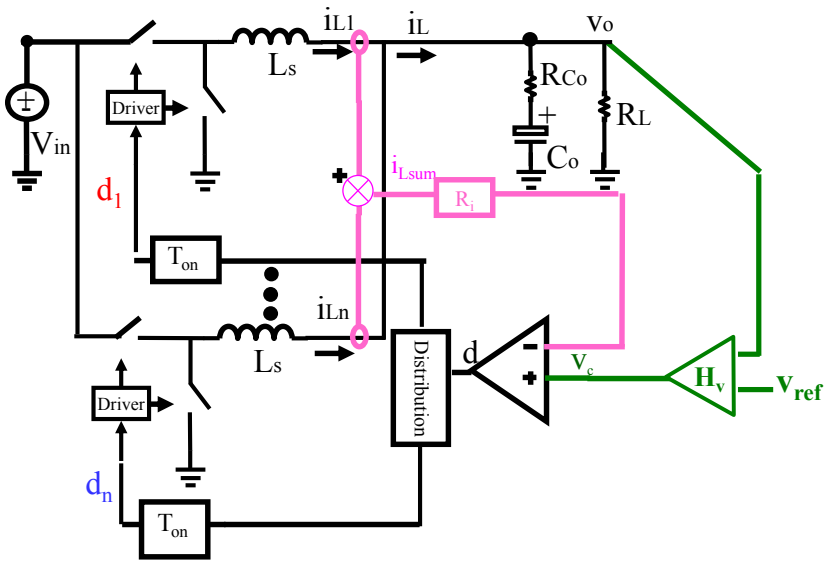


Figure 2. 1 Multi-phase constant on-time current mode structure based on pulse distribution [C28]

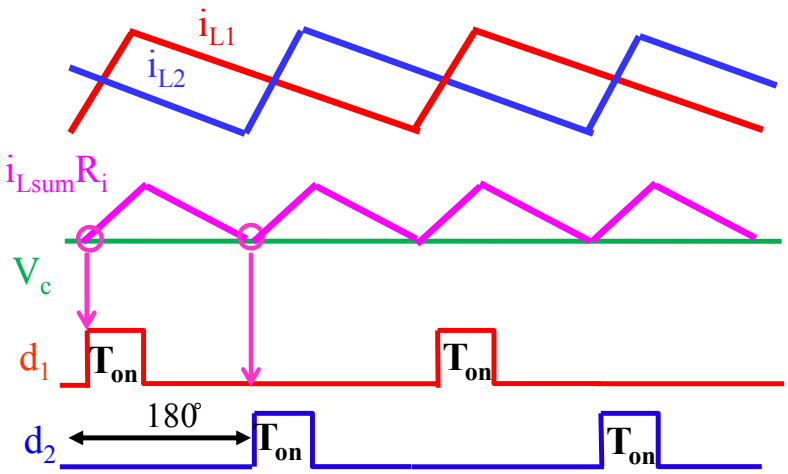


Figure 2. 2. Steady-state waveform for two-phase constant on-time current mode structure based on pulse distribution.[C28]

One concern of this simple structure is the ripple cancelation effect due to interleaving between different phases. Figure 2. 3 shows the ratio of summed inductor current and the phase current. When the operation range is close to ripple cancellation point, the total inductor current ripple is small and the small amount of current ripple is prone to be disturbed by noise. Figure 2. 4 shows the experimental results of jittering performance for a three-phase Buck converter, when duty cycle is around 0.3, which is very close to ripple cancellation point (D=33%), severe jittering is observed.

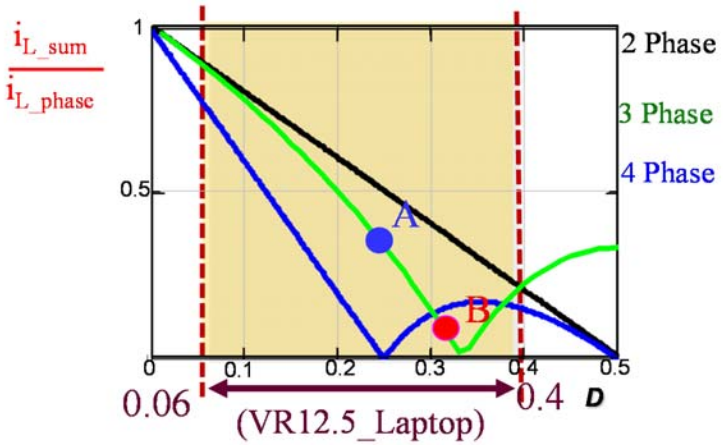


Figure 2. 3. Interleaving effect on summed inductor current ripple

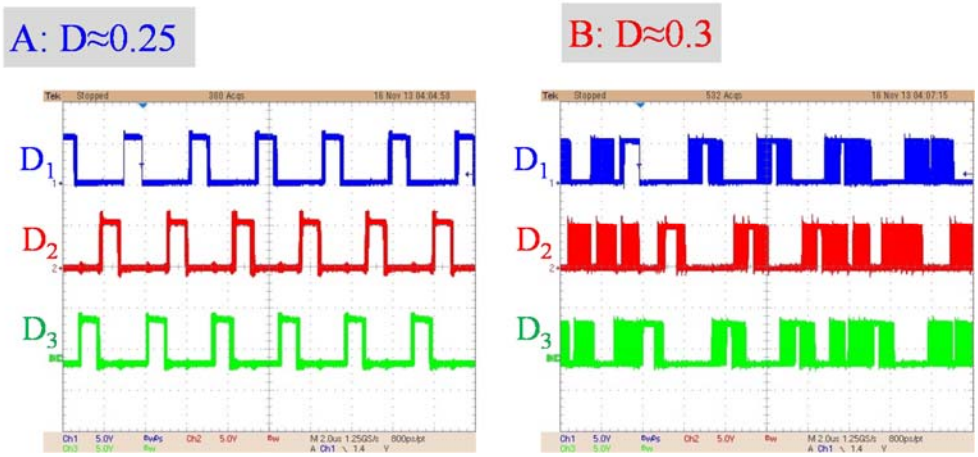


Figure 2. 4 Jittering performance comparison for a three-phase converter (a) D ≈ 0.25 (b) D ≈ 0.3, very close to cancellation point (0.33)

To alleviate the jittering problem caused by the ripple cancellation effect, external ramp compensation is utilized in commercial products [C13][C14]. As shown in Figure 2. 5 and Figure 2. 6, the external ramp increases the total ramp to compare with control signal and therefore the immunity of the circuit to the disturbing noise is improved. There are different implementations for the generation of external ramp: in [C14][C15], the ramp starts to build up at the beginning of the off-time, In [C13], the ramp starts to build up after a certain delay of the beginning of the on-time.

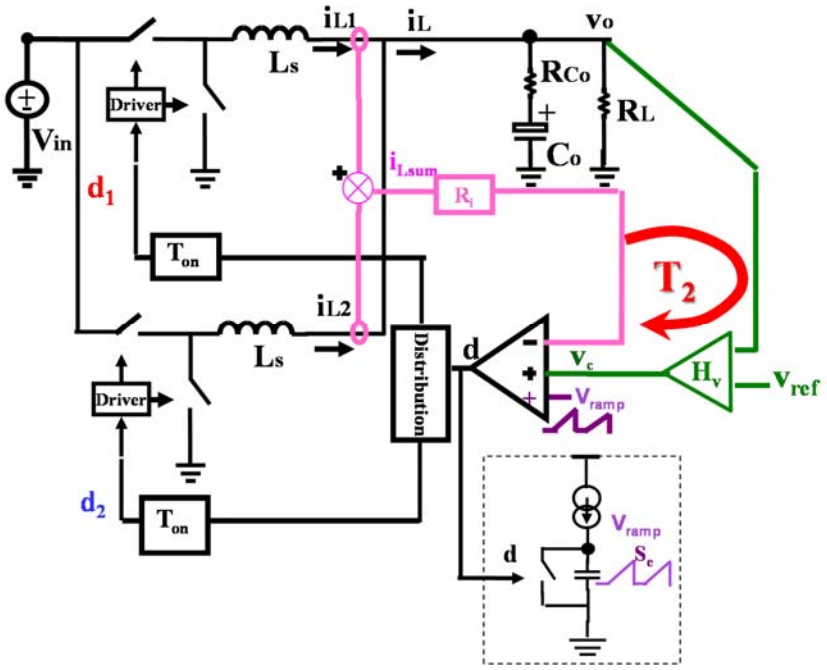


Figure 2. 5. Two-phase constant on-time current mode control with external ramp compensation [C14]

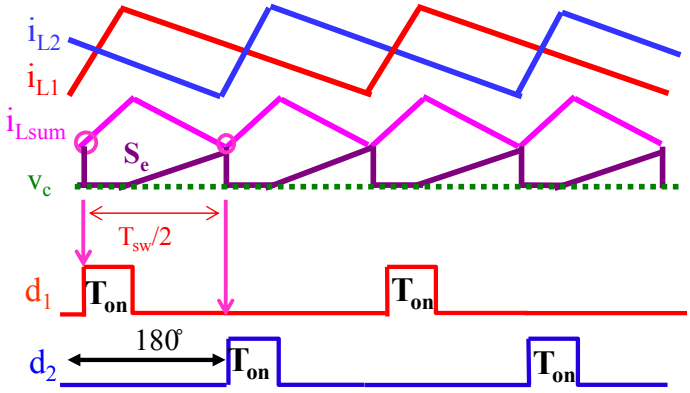


Figure 2. 6. Steady-state waveform for two-phase constant on-time current mode with external ramp compensation [C14]

External ramp compensation is a simple solution to alleviate jittering problem, however, the addition of external ramp affects the dynamic performance. Without changing the compensator parameters, it is observed that the introduction of the external ramp reduces the bandwidth and phase margin of the total loop gain transfer function. One example is shown as Figure 2. 5 with the following parameters: n_{ph}=2; F_{sw}=800kHz/phase, V_{in}=5.2V, V_o=2V, L_s=150nH/phase,

R_{LL}=1.5mΩ, Io=40A. As shown in Figure 2. 7, without external ramp, the converter is designed with 230kHz bandwidth and sufficient phase margin (70degrees). With the external ramp slope around the inductor current falling slope (magnitude of 38mV), the phase margin reduce to 50degrees while the bandwidth reduce from 230kHz to 150kHz. With external ramp slope around 2 times the inductor current falling slope, the phase margin further reduces to 38degrees, which is out of many engineer's comfort zone of at least 45 degree phase margin.

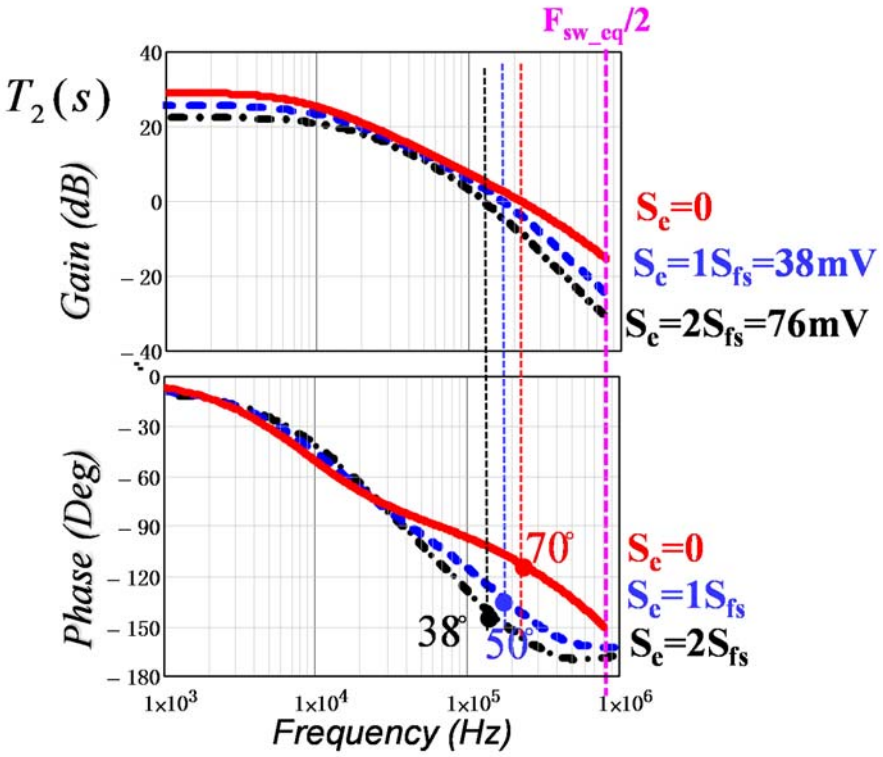


Figure 2. 7. Impact of external ramp on loop gain bandwidth and phase margin in 2-phase VR example

For quantitative analysis, an accurate small-signal model is indispensable. Several papers which are closely related to this subject are summarized as follows: In [C35], the describing function method is used to derive the transfer function of constant on-time modulator. However, the inductor current information is not included in voltage mode control structure. For previous small-signal models for constant on-time current mode control, which includes Redl's analysis

based on injected-absorbed current method [C29], Ridley's modified average model [C31], Voperian's current-controlled PWM switch model [C30], Li's equivalent circuit model based on describing function [C32], Yan's three-terminal switch model [C34], none of them includes external ramp compensation as the external ramp is rarely used at that time. Up to now, no good small signal model for constant on time current mode control with external ramp compensation is proposed in the literature.

This chapter tries to provide a simple and accurate three terminal switch model for constant on-time current mode control with external ramp compensation, which will serve as a useful tool for understanding the effect of external ramp and designing feedback control appropriately. This chapter is organized as follows: firstly, the accurate small-signal control-to-output voltage transfer function is derived using describing function method and the results are presented in section 2.2. The describing function result is infinite order and accurate up to infinite frequency. In section 2.3, the infinite order transfer function is simplified to polynomial form in order to derive a simple equivalent circuit model. A three-terminal switch model is proposed based on non-ideal current source concept. It is a complete model which can be used to examine all transfer functions and is accurate up to half of switching frequency. Section 2.4 discusses some important aspects about the proposed three-terminal switch model. Section 2.5 extends the three-terminal switch model to multi-phase converters. Section 2.6 provides the design consideration based on the proposed model. Section 2.7 provides Simplis simulation and experimental results to verify the proposed three-terminal switch model. Section 2.8 summarizes this chapter. The major content of this chapter is published in [C39] and [C40].

2.2 Proposed Small-signal Model Based on Describing Function

To get exact small-signal control-to-inductor current transfer function, the describing method which is first proposed in [C32] for current mode control is employed. The structure of constant on-time current mode control with external ramp compensation when v_c is under perturbation is shown in Figure 2. 8, the nonlinear constant on-time modulator, which consists of the switches, the inductor current, the comparator with external ramp and the on-time generator, is treated as a single entity. The steady-state waveform and perturbed waveform are shown in Figure 2. 9. The assumptions of the describing method and derivation steps are exactly same as [C32], therefore, only critical steps are listed in this chapter.

Step 1: perturbed off-time calculation

$$v_c(t_{i-1}+T_{off(i-1)})+s_eT_{off(i-1)}+s_nT_{on}=v_c(t_i+T_{off(i)})+(s_e+s_f)T_{off(i)} \quad (2.1)$$

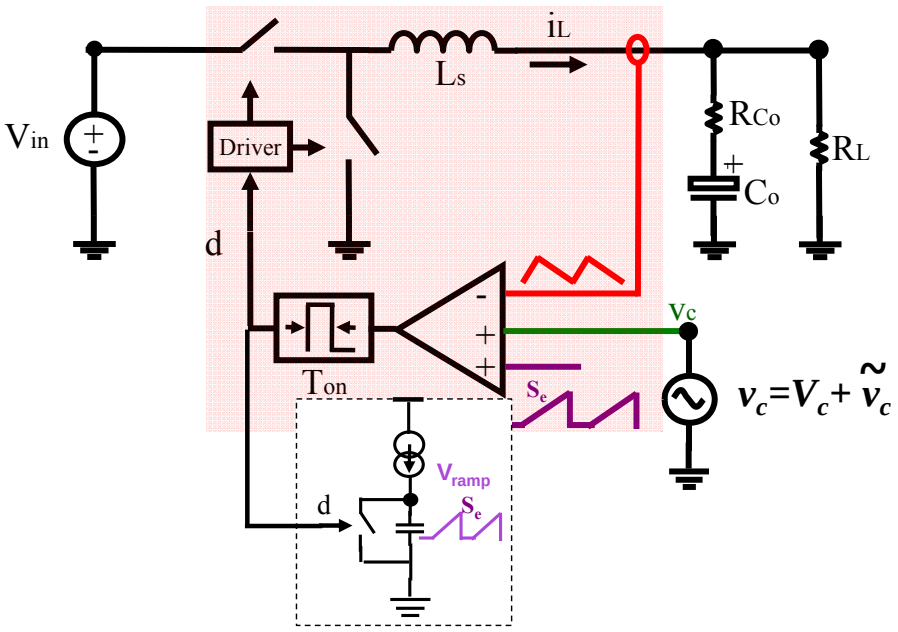


Figure 2. 8. Modelling method for constant on-time current mode with external ramp.

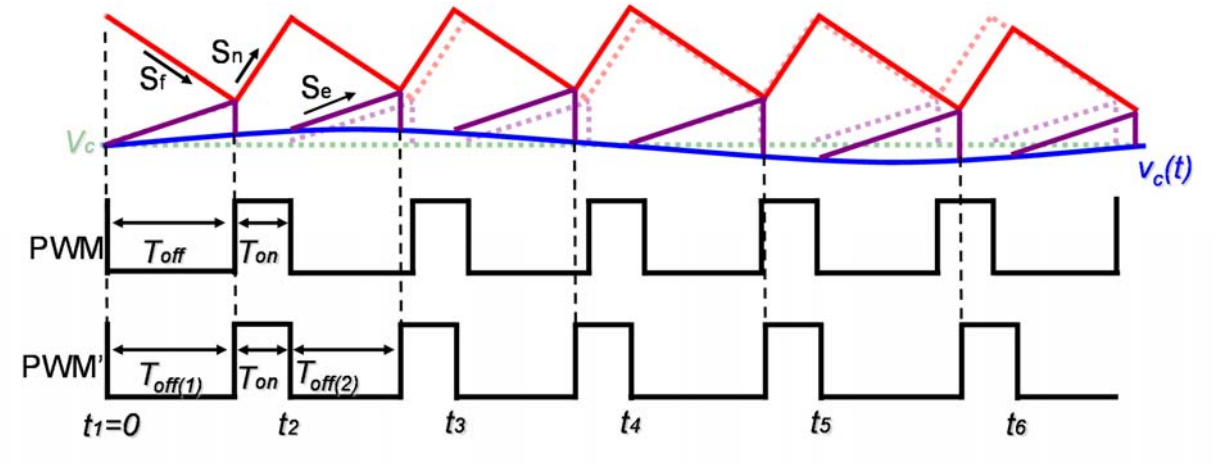


Figure 2. 9. Steady-state and perturbed waveform for constant on-time current mode with external ramp.

Step 2: perturbed duty cycle and perturbed inductor current calculation, as shown follows:

$$d(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \sum_{i=1}^{M}[u(t-t_i-T_{off(i)})-u(t-t_i-T_{off(i)}-T_{on}) \tag{2. 2}$$

$$i_L(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \int_0^t \left\{\frac{V_{in}-V_o}{L_s}d(t)-\frac{V_o}{L_s}[1-d(t)]\right\}\cdot dt + i_{L0} \tag{2. 3}$$

Step 3: Fourier analysis on inductor current and output voltage to obtain describing function result, as shown in following equations:

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\frac{V_{in}}{L_s s} \tag{2. 4}$$

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\frac{V_{in}}{L_s s}\frac{R_L(R_{Co}C_o s+1)}{R_L C_o s+1} \tag{2. 5}$$

Step 4: Consider the variation of inductor current slopes, the transfer functions from the input voltage to inductor current and output voltage to inductor current are derived in a similar method and the results are shown as follows:

$$\frac{i_L(s)}{v_{in}(s)} = \frac{-1}{L_s s}\left[\frac{f_s(1-e^{-sT_{on}})}{(1-e^{sT_{sw}})[(s_f+s_e)-s_e e^{-sT_{sw}}]}\frac{(1-e^{sT_{on}})}{s\cdot L_s/R_i}\cdot V_{in}+D\right] \tag{2. 6}$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s} \cdot [\frac{f_s(1-e^{-sT_{on}})}{(s_e + s_f) - s_e e^{-sT_{sw}}} \cdot \frac{1}{s \cdot L_s / R_i} \cdot V_{in} - 1] \quad (2.7)$$

2.3 Proposed Three-terminal Switch Model

For small duty cycle application, the effect of dynamic term related with on time in (2. 4) is small and can be neglected. Furthermore, with a first-order polynomial simplification, the infinite order control-to-inductor transfer function shown in (2. 4) is simplified as follows:

$$\frac{i_L(s)}{v_c(s)} \approx \frac{1}{R_i} \frac{1 + \frac{T_{sw}}{2} s}{1 + \left(\frac{s_e}{s_f} + \frac{1}{2}\right) T_{sw} s}, s_f = R_i \cdot \frac{V_o}{L_s} \quad (2.8)$$

The approximation is good up to half of switching frequency compared with simulation results, as shown in Figure 2. 10.

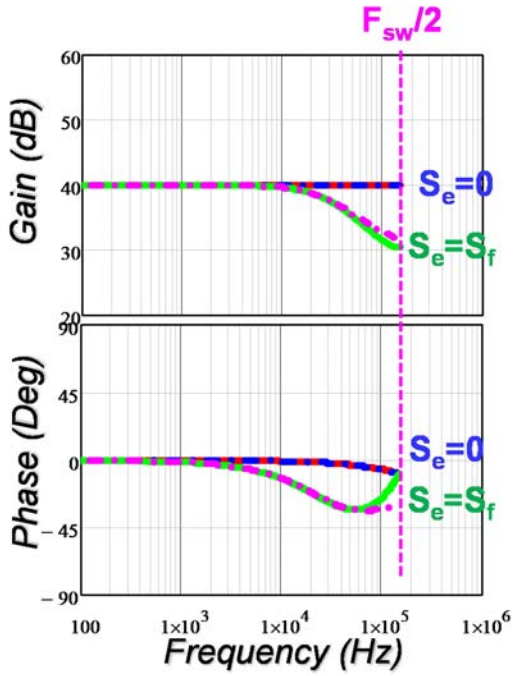


Figure 2. 10. Comparison of control to inductor current transfer function between approximation (2. 8) and simplis simulation: Blue dash: approximation with Se=0; Red solid: simulation with Se=0; Pink dash: approximation with S_e=S_f; Green Solid: simulation with S_e=S_f.

From Figure 2. 10, if there is no external ramp, the control to inductor current is constant gain, which reveals the fact that in this case the inductor current is well controlled by control signal, or equivalently, the circuit can be regarded as an ideal current source. By adding an external ramp, the gain of control to inductor current drops at high frequency, which reveals the fact that the external ramp reduces the ability of controlling the inductor current, or in other words, the circuit is a non-ideal current source due to the effect of external ramp. Based on the physical insight of non-ideal current source, an equivalent circuit is derived to represent (2. 8) as follows:

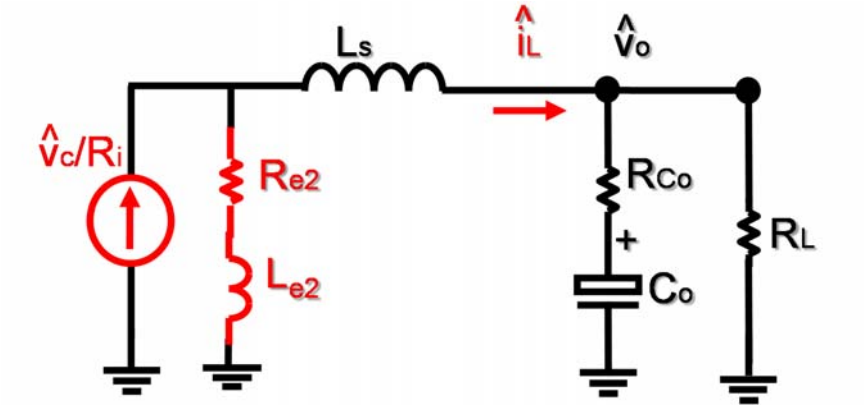


Figure 2. 11. Equivalent circuit representation of constant on time current mode control with external ramp compensation for small duty cycle.

The expressions of R_{e2} and L_{e2} is shown as follows:

$$R_{e2} = \frac{L_s}{\frac{s_e}{s_f} T_{sw}}, L_{e2} = \frac{L_s}{2\frac{s_e}{s_f}} \tag{2. 9}$$

For general case, the effect of dynamic term related with on-time in (2. 4) may need to be considered: as the duty cycle is large, additional phase delay is observed. As shown in Figure 2. 12, compared with D=0.1 case, there is additional 33 degree phase delay at half of the switching frequency for D=0.5 case. Previous equivalent circuit model of constant on time control uses an impedance comprised by R_e and C_e to represent the additional phase delay by forming a pair of double pole whose position is related with on-time [C32]. Apply the same concept, the polynomial

simplification of control-to-inductor current and its equivalent circuit representation is shown as (2. 10) and Figure 2. 13, respectively.

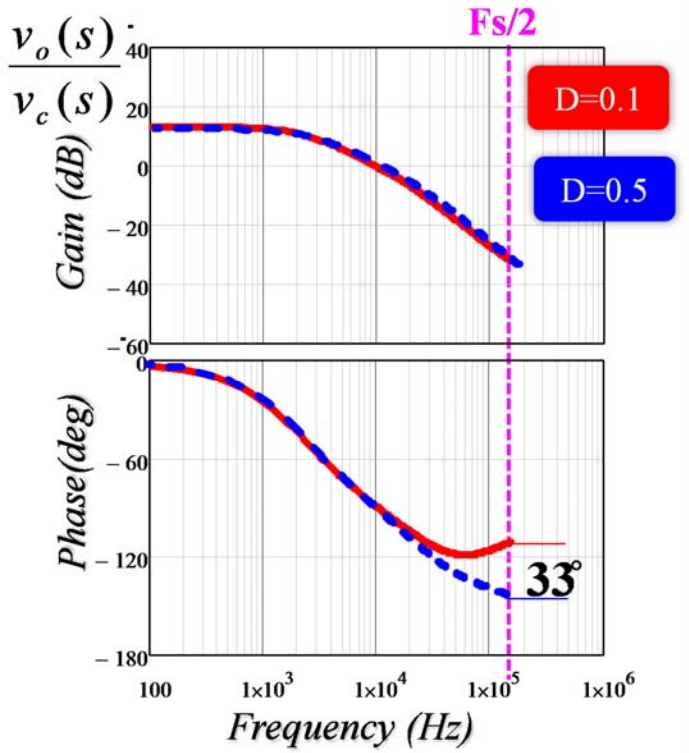


Figure 2. 12 Effect of duty cycle on high frequency phase response

$$\frac{i_L(s)}{v_c(s)} \approx \frac{1}{R_i} \frac{1+\frac{T_{sw}}{2}s}{1+\left(\frac{s_e}{s_f}+\frac{1}{2}\right)T_{sw}s} \frac{1}{1+\frac{s}{Q_1\omega_1}+\left(\frac{s}{\omega_1}\right)^2} \qquad Q_1=\frac{2}{\pi}, \omega_1=\frac{\pi}{T_{on}} \tag{2. 10}$$

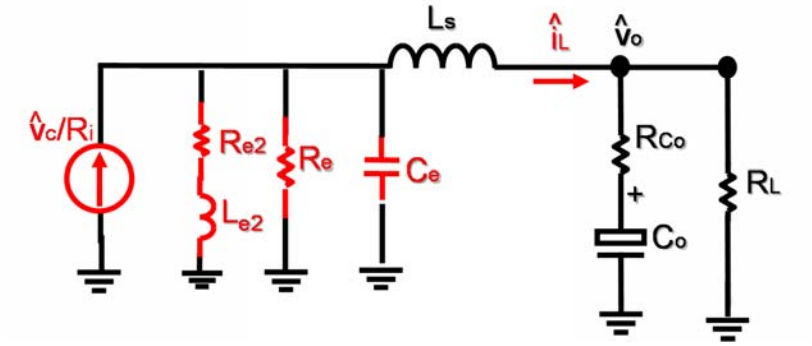


Figure 2. 13. Equivalent circuit representation of constant on time current mode control with external ramp compensation for general case.

The expressions of R_{e2}, L_{e2}, R_e and C_e are shown as follows:

$$R_e = \frac{2L_s}{\left(\frac{2s_e}{s_f}+1\right)T_{on}}, C_e = \frac{1}{L_s\omega_1^2}, R_{e2} = \frac{L_s}{\frac{s_e}{s_f}(1-D)T_{sw}}, L_{e2} = \frac{L_s}{2\frac{s_e}{s_f}(1-D)} \quad (2.\ 11)$$

Figure 2. 13 can be used to derive control-to-output voltage transfer function and output impedance, however, the input property is lost. To consider the input property and apply the three-terminal switch model concept, the same strategy as [C34] is adopted. The three-terminal switch model for single phase is shown as Figure 2. 14.

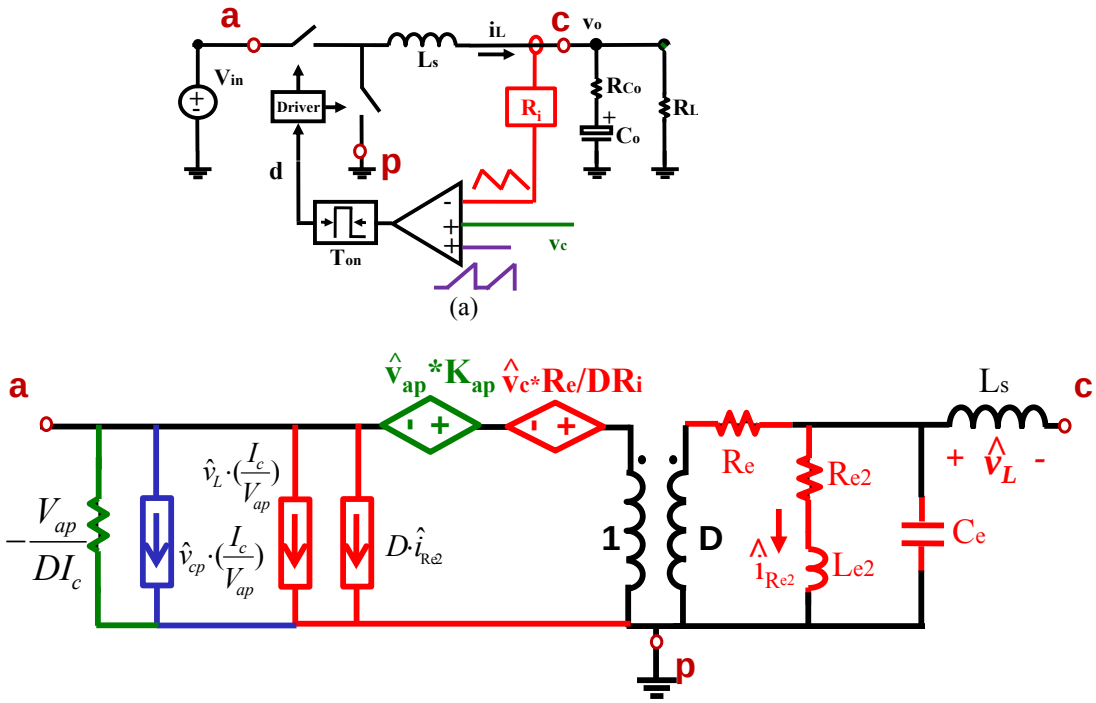


Figure 2. 14. Three-terminal switch model of single phase constant on time current mode control with external ramp compensation.

The expressions of K_{ap} for constant on-time current mode control is shown as follows:

$$K_{ap} = \frac{T_{off}}{T_{on}} \quad (2.\ 12)$$

2.4 Discussion on Proposed Three-terminal Switch Model

2.4.1 Comparison with previous three-terminal switch model [C34]

As seen from (2. 9), the impedance comprises by R_{e2} and L_{e2} is infinite when there is no external ramp, therefore, additional R_{e2}-L_{e2} branch disappears and the model in Figure 2. 14 reduces to previous model proposed in [C34] , as shown in Figure 2. 15. This means the model shown in Figure 2. 14 is more inclusive and general.

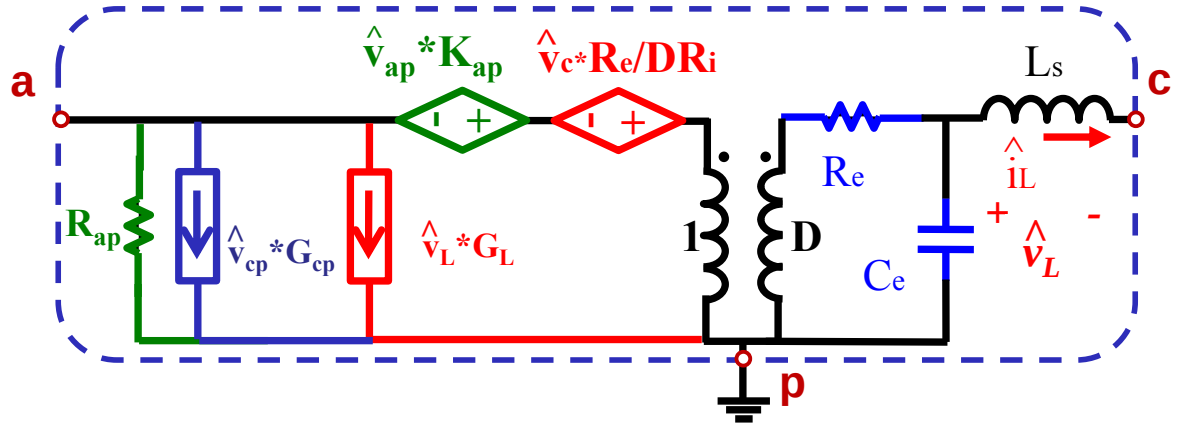


Figure 2. 15. Proposed three-terminal switch model reduced to original three-terminal switch model in [C34] when S_e=0.

2.4.2 Moving pole and static zero represented by R_{e2}-L_{e2} Impedance

When external ramp increases, the impedance R_{e2} and L_{e2} reduces. To illustrate this point, use S_e=S_f as an example. The values of R_{e2} and L_{e2} can be calculated from (2. 9), which is $L_s/(T_{sw})$ and $L_s/2$, respectively. The following analysis shows how R_{e2} and L_{e2} represent the pole and zero of the circuit shown in Figure 2. 11. When modulation frequency is low, the impedance of R_{e2} is much larger than L_{e2} and L_s, therefore, the R_{e2}-L_{e2} impedance does not shunt current, all the current from the current source flows into L_s branch, therefore, the gain is flat, as seen from Figure 2. 10. When modulation frequency increases, the impedance of inductor L_s branch increases, and the R_{e2}-L_{e2} branch starts to shunt current. According to current divider theory, the boundary modulation

frequency is the point at which the impedance of R_{e2} is the same as the sum impedance of L_{e2} and L_s. For this example, the values is $F_{sw}/(3\pi)$. After modulation frequency surpasses this frequency, R_{e2}-L_{e2} branch starts to shunt current as the impedance is smaller compares with L_s branch. The inductor current is determined by an ideal current source coming through a first order current divider. The larger the modulation frequency, the smaller the R_{e2}-L_{e2} impedance compared with L_s branch, the more current it shunts and the more phase delay. From Figure 2. 10, the gain and phase both continue to drop which is a pole effect. Now if the modulation frequency further increases to surpass the critical point where the impedance of R_{e2} is the same as impedance of L_{e2}, then impedance of L_{e2} will dominate R_{e2}-L_{e2} branch and the ratio between this branch and L_s branch is same afterwards. Therefore the gain starts to drop and the phase increases, which is a zero effect. The frequency of zero is at F_{sw}/π. In general, based on current division theory, due to the branch of R_{e2}-L_{e2}, there is a moving pole and a static zero: the pole is determined by R_{e2}, L_{e2} and L_s the zero is determined by R_{e2} and L_{e2}. The expression of the zero and the pole is shown as follows:

$$\begin{aligned} f_{pe} &= \frac{1}{2\pi}\frac{R_{e2}}{L_{e2}+L_s} = \frac{F_{sw}}{\pi(2s_e/s_f+1)}, \\ f_{ze} &= \frac{1}{2\pi}\frac{R_{e2}}{L_{e2}} = \frac{F_{sw}}{\pi} \end{aligned} \tag{2. 13}$$

2.4.3 Effect of external ramp on pole-zero movements and Bode plots

Previously the effect of R_{e2}-L_{e2} impedance with a given external ramp is discussed: a moving pole and a static zero. To understand the reason of increased circuit order by the external ramp physically, the natural response of the circuit is examined, as shown in Figure 2. 16. The solid line is steady state of the sensed inductor current waveform while the dashed line is the purebred waveform. At time t_0, there is a perturbation on the inductor current Δi_{L0}, after k switching cycles,

the deviation magnitude of inductor current changes to Δi_{Lk}. From geographical calculation, the relations between Δi_{Lk} and Δi_{L0} can be derived as follows:

$$\Delta i_{Lk} = \left(\frac{s_e}{s_e + s_f} \right)^k \Delta i_{L0} \tag{2. 14}$$

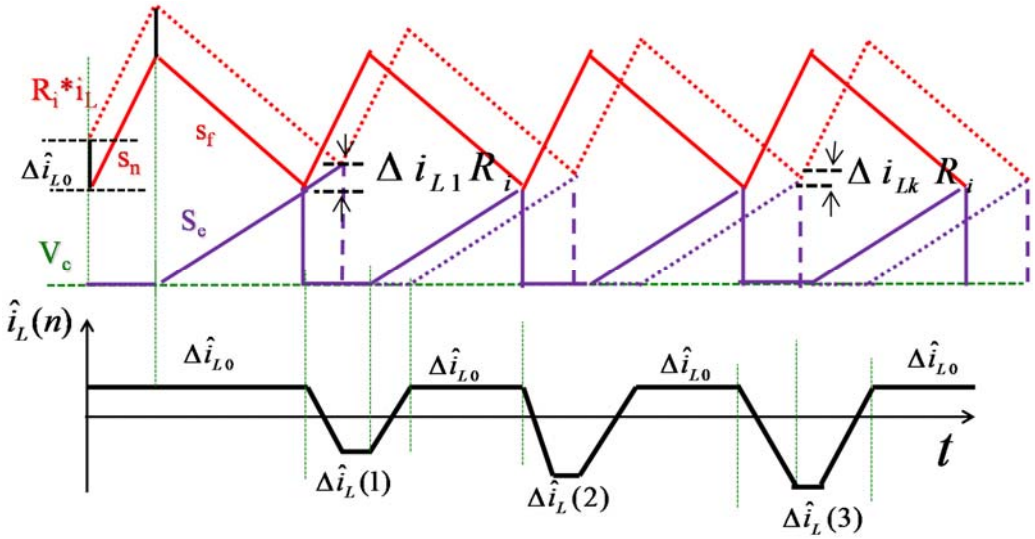


Figure 2. 16 Natural response of constant on-time current mode control with external ramp: Solid, Steady-state; Dashed, perturbed.

From (2. 14), without s_e, the perturbation is disappeared in just one cycle, this is shown in Figure 1.11 (b), where the natural response shows the error is settled in just one switching cycle without further dynamics. With external ramp, as shown in (2. 14), the dynamics is observed, the larger external ramp, the longer time it requires to damp out the perturbation, as the coefficient in (2. 14) is closer to 1. From (2. 14) a first order dynamic response is observed and the time constant is related with external ramp. Physically, without external ramp, the inductor current does not contribute to any dynamic for constant on-time structure, with addition of external ramp, the inductor current error information is transmitted into next switching cycle and it causes the dynamics. The larger the ramp magnitude, the longer time the error information lingers. That intuitively explains the dependence of the pole on the external ramp magnitude.

Figure 2. 17 shows the pole zero map with different external ramp and the following circuit parameters: F_{sw}=300kHz, V_{in}=12V, V_o=1.2V, L_s=300nH, R_L=100mΩ, 8 ceramic capacitors (1.4mΩ/100uF), R_i=10 mΩ. The ESR zero of the capacitor is far away from the switching frequency and can be ignored. From Figure 2. 11, when external ramp is zero, R_{e2}-L_{e2} impedance is infinite and only the pole caused by output capacitor and load exists. When external ramp increases, R_{e2}-L_{e2} branch impedance decreases and starts to shunt current in a certain frequency range. As analyzed in previous section, there is a stationery zero located at F_{sw}/π, which is determined by R_{e2} and L_{e2} and a moving pole which is determined by R_{e2}, L_{e2} and L_s, as shown in (2. 13). Further increase the external ramp, the impedance of R_{e2}-L_{e2} branch is so small that the current loop effects is killed by the large external ramp, turning the current mode control into voltage mode control. The moving pole combines with the single pole caused by output capacitor and load and forms a pair of double pole at power stage LC filter corner frequency.

Figure 2. 18 shows the Bode plots of control to output voltage transfer function with increasing external ramp. When s_e=0 (red), only one pole caused by output capacitor and load exists and it is first order circuit as the minimum phase is around -90 deg. When s_e=1s_f (blue), the pole starts to move and split with the zero. When S_e=20s_f (pink), the moving pole combines with the low frequency pole and forms a double pole at power stage corner frequency, in this case, the current loop effect is killed by the large external ramp, changing current mode to voltage mode control.

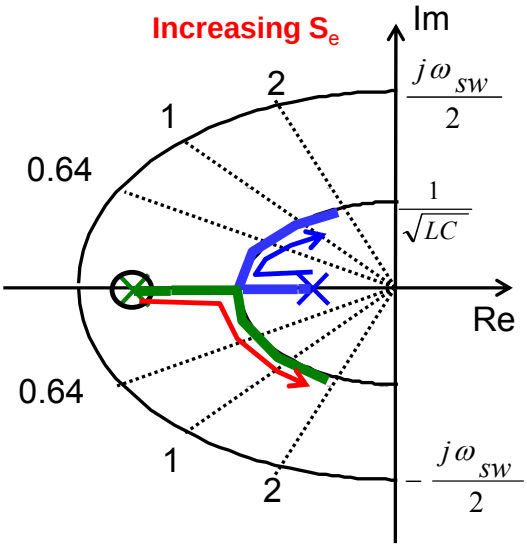


Figure 2. 17. Pole-zero map of control-to-output voltage with increasing external ramp.

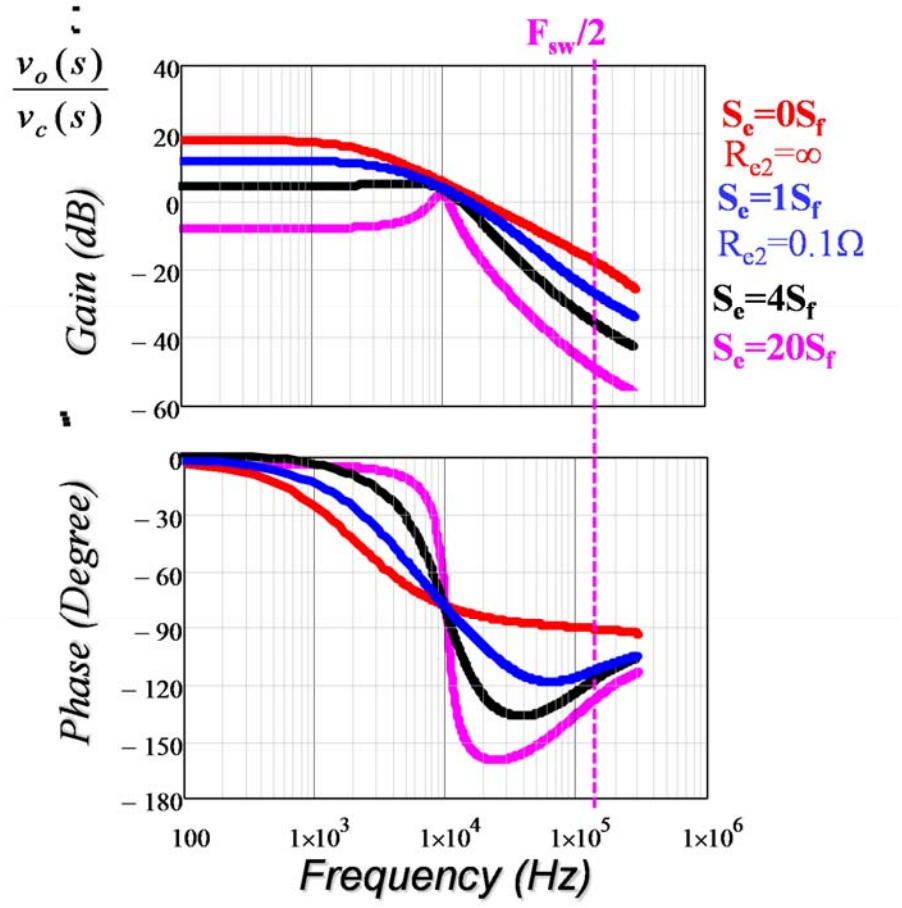


Figure 2. 18. Bode plots of control-to-output voltage transfer function with increasing external ramp.

2.4.4 Comparison with peak current mode control and constant on-time voltage mode control

From Figure 2. 17 and Figure 2. 18, the characteristics of control-to-output voltage transfer function with different external ramps are similar as in the case of constant frequency peak current mode control. The only difference is caused by the stationery zero, which shows a high frequency phase boost, shown as Figure 2. 19. The comparison indicates possible bandwidth improvement with constant on-time current mode control due to stationery zero.

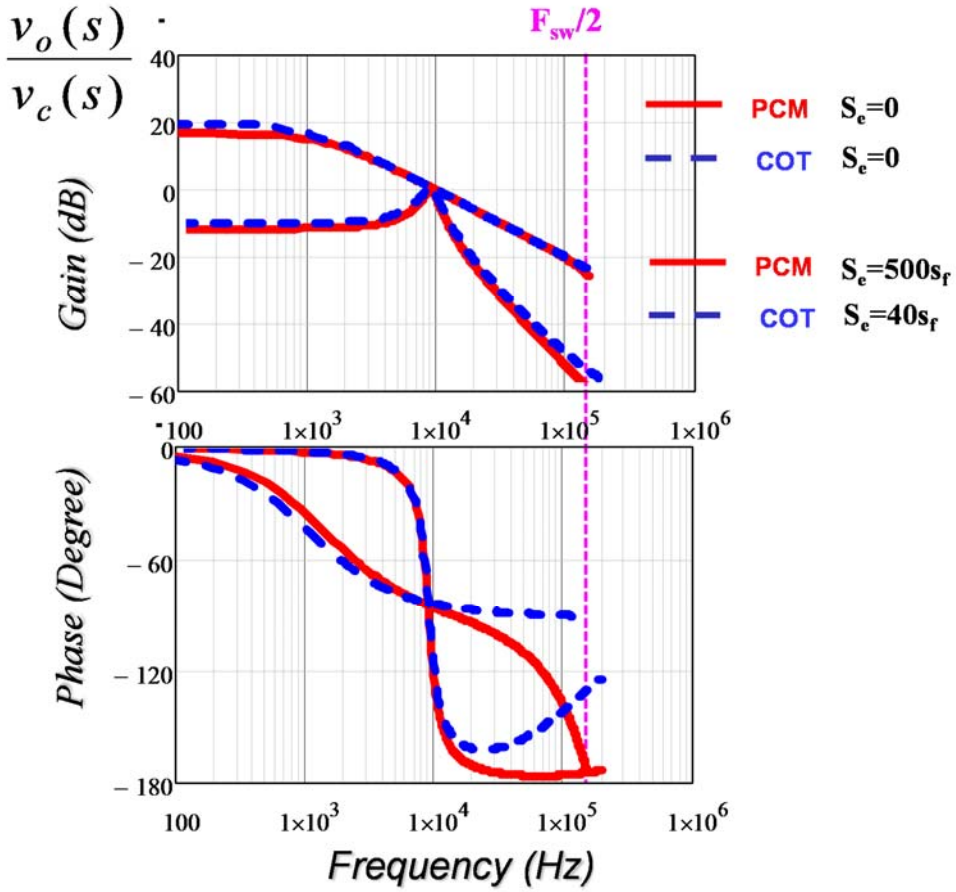


Figure 2. 19. Control-to-output voltage Bode plots comparison between constant on-time current mode and peak current mode: (1) $S_e=0$; (2) $S_e=500S_f$ (PCM) and $S_e=40S_f$ (COT).

With large external ramp, the current loop effect is killed and the circuit turns into voltage mode control. For constant on-time voltage mode control, the describing function method is utilized to derive the transfer function of variable frequency modulation scheme in [C35] and the control-to-output voltage transfer function is shown in the following equation:

$$G_{c2vo\_v} = \frac{DV_{in}}{s_e T_{sw}} \frac{1 + R_{Co} C_o s}{1 + s/(Q_o \omega_o) + \left(\frac{s}{\omega_o}\right)^2} e^{\frac{1-D}{2} T_{sw} s}, \quad \omega_o = \frac{1}{\sqrt{LC}}, Q_o \approx R_L \sqrt{\frac{C}{L}} \tag{2. 15}$$

As shown in Figure 2. 20, under S_e=1000s_f case, control-to-output voltage transfer function of constant on-time voltage mode agrees very well with constant on-time current mode. There is a slight difference in high frequency phase due to the first order polynomial approximation when deriving constant on-time current mode control while the model shown in (2. 15) use exponential term to represent the phase boosting phenomenon.

2.5 Extension to Multi-phase Converters and Constant-off-time Current Mode Control

To extend the proposed three-terminal switch model to multi-phase constant on-time current mode control case, the summed inductor current signal should be examined carefully as it is the feedback signal to determine the duty cycle. The strategy is to derive an equivalent single-phase converter and then use the equivalent circuit model of single-phase converter. For a two-phase converter shown in Figure 2. 5 and Figure 2. 6, the rising and falling slope of summed inductor current is shown as follows:

$$s_{n\_2} = R_i \frac{V_{in} - 2V_o}{L_s} = R_i \frac{V_{in}/2 - V_o}{L_s/2}, s_{f\_2} = R_i \frac{2V_o}{L_s} = R_i \frac{V_o}{L_s/2} \tag{2. 16}$$

Following the same reason, for n-phase converter under duty cycle no-overlap case, the rising slope and falling slope for summed inductor current is shown as follows:

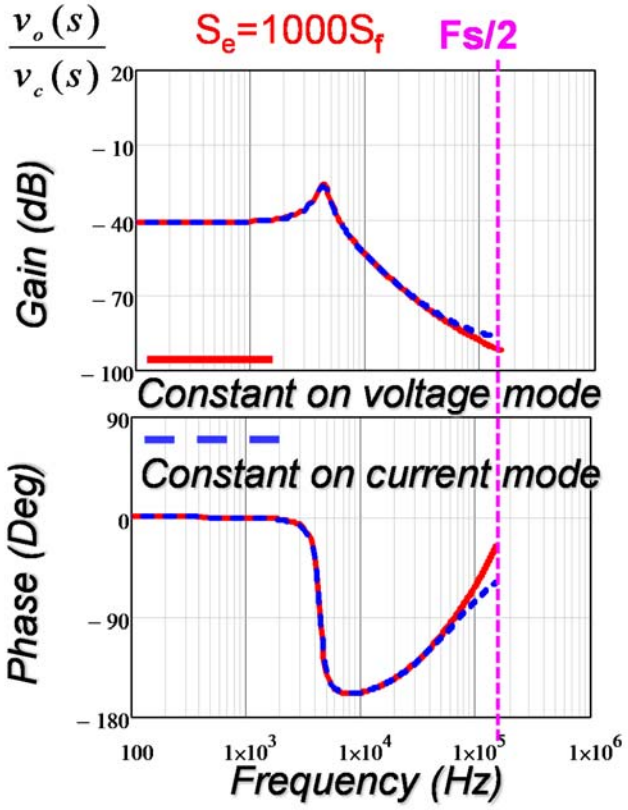


Figure 2. 20. Control to-output voltage Bode plots comparison between constant on-time voltage mode and current mode under s_e=1000s_f.

$$s_{n\_n} = R_i \frac{V_{in} - nV_o}{L_s} = R_i \frac{V_{in}/n - V_o}{L_s/n}, s_{f\_n} = R_i \frac{nV_o}{L_s} = R_i \frac{V_o}{L_s/n} \quad (2.\ 17)$$

From (2. 17), for n-phase constant on-time current mode control structure, from small-signal point of view, it is equivalent to the single-phase constant on-time control, as shown in Figure 2. 21. The equivalent switching frequency is n times that of single phase, the inductor is reduced to 1/n of the single phase inductor and the input voltage is also reduced to 1/n.

Therefore, the equivalent circuit model for multi-phase constant on-time current mode control with external ramp compensation can be derived, as shown in Figure 2. 22.

The expressions of R_{e_n}, C_{e_n}, R_{e2_n} and L_{e2_n} are shown in (2. 18) and the expressions of pole and zero caused by external ramp are shown in (2. 19):

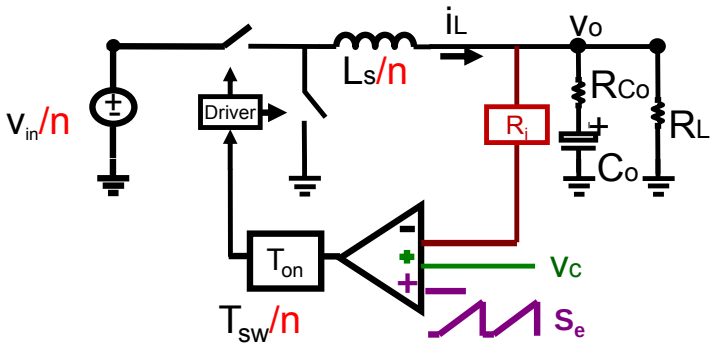


Figure 2. 21. Equivalent single phase constant on-time current mode control

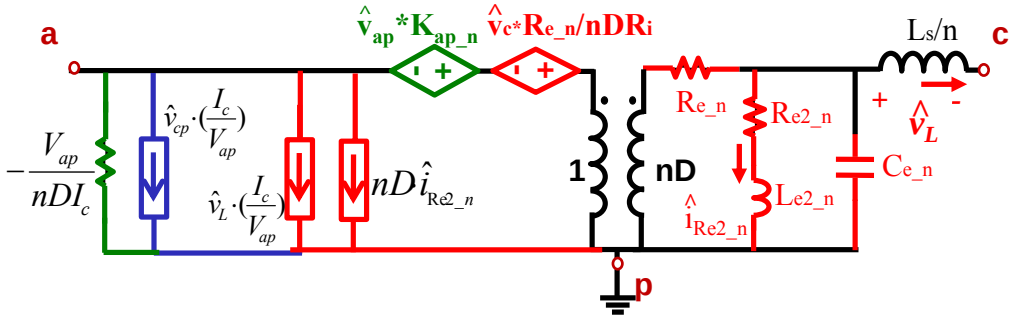


Figure 2. 22. Complete three-terminal switch model of n-phase constant on-time current mode control with external ramp compensation.

$$R_e = \frac{2L_s/n}{\left(\frac{2s_e}{s_{f\_n}}+1\right)T_{on}}, C_e = \frac{n}{L_s\omega_1^2}$$

$$R_{e2} = \frac{L_s}{\frac{s_e}{s_{f\_n}}(1-nD)T_{sw}}, L_{e2} = \frac{L_s/n}{2\frac{s_e}{s_{f\_n}}(1-nD)} \quad (2.\ 18)$$

$$f_{pe\_n} = \frac{1}{2\pi}\frac{R_{e2\_n}}{L_{e2\_n}+L_s/n} = \frac{nF_{sw}}{\pi(2s_e/s_{f\_n}+1)}, \quad (2.\ 19)$$

$$f_{ze} = \frac{1}{2\pi}\frac{R_{e2\_n}}{L_{e2\_n}} = \frac{nF_{sw}}{\pi}$$

Compare (2. 18), (2. 19) with single phase equations (2. 11) and (2. 13), the pole and zero position are higher as the equivalent switching frequency is n times the switching frequency of single phase.

The equivalent circuit model can be extended easily to constant off-time current mode control with external ramp compensation case, based on duality principle. The equivalent circuit model is shown in Figure 2. 22 with the expresiions of R_{e_n}, C_{e_n}, R_{e2_n} and L_{e2_n} are shown as follows:

$$R_e = \frac{2L_s / n}{\left(\frac{2s_e}{s_{n\_n}} + 1\right)T_{off}}, C_e = \frac{n}{L_s \omega_1^2}, \omega_1 = \frac{\pi}{T_{off}}$$
$$R_{e2} = \frac{L_s}{\frac{s_e}{s_{n\_n}} nDT_{sw}}, L_{e2} = \frac{L_s / n}{2\frac{s_e}{s_{n\_n}} nD} \quad (2.\ 20)$$

2.6 Design Consideration Based on Equivalent Circuit Model

Based on the equivalent circuit model in Figure 2. 22, the effect on the external ramp on the loop gain of the circuit can be analyzed. Using a 2 phase Buck-converter for laptop VR application as an example which has the following parameters: V_{in} =5.2V—8.1V, V_o=0.5V—2V, D=0.06 -- 0.4, f_{sw}=800kHz, L=150nH/ph, full load current Io=40A, load line requirement R_{LL}=1.5mΩ. The external ramp compensation is designed to be S_e=1S_{fs}@V_o=2V based on jittering performance. In this example, the external ramp starts to build up at the beginning of off-time and the above ramp magnitude is 40mV per switching cycle.

When V_o=2V, the pole caused by the external ramp is calculated as follows:

$$@V_o = 2V : f_{pe} = \frac{f_{sw}}{\pi(\frac{s_e}{s_{fs}} + \frac{1}{2})} = 170kHz \quad (2.\ 21)$$

However, when operating point changes to V_o=0.5V, the summed inductor current falling slope is changed therefore there ratio between the two is changed and the pole position in this case is shown as follows:

$$@V_o = 0.5V : f_{pe} = \frac{f_{sw}}{\pi(\frac{s_e}{s_{fs}(0.5)} + \frac{1}{2})} = 56kHz \quad (2.\ 22)$$

The Bode plots of the control-to-output transfer function is shown as Figure 2. 23. Due to wide operating range, there is a moving pole which reduces the gain and phase. Therefore, from design point of view, either the worst case needs to be considered for compensation or smart compensation such as auto tuning can be adopted.

2.6.1 Traditional worst case design strategy

Similar procedure to design the compensator as shown in [C37] can be followed, a simple compensator can be used with one pole and one zero. The compensator expression is shown as follows:

$$H_v(s) \approx K_p \frac{s/\omega_z + 1}{s/\omega_p + 1} \quad (2.\ 23)$$

The design steps are as follows:

(1) Design K_p to meet load line requirement; $K_p = R_i/R_{LL}$.

(2) Place Zero to cancel the pole caused by external ramp for enough phase margin: the pole position of the worst case needs to be considered. In this case, the lowest pole position is @ 56kHz when Vo=0.5V. Therefore, place the zero at 56kHz.

(3) Place pole at power stage ESR zero or half the switching frequency, whichever is lower. As ceramic capacitor is used in this example, the pole is placed at half of the switching frequency.

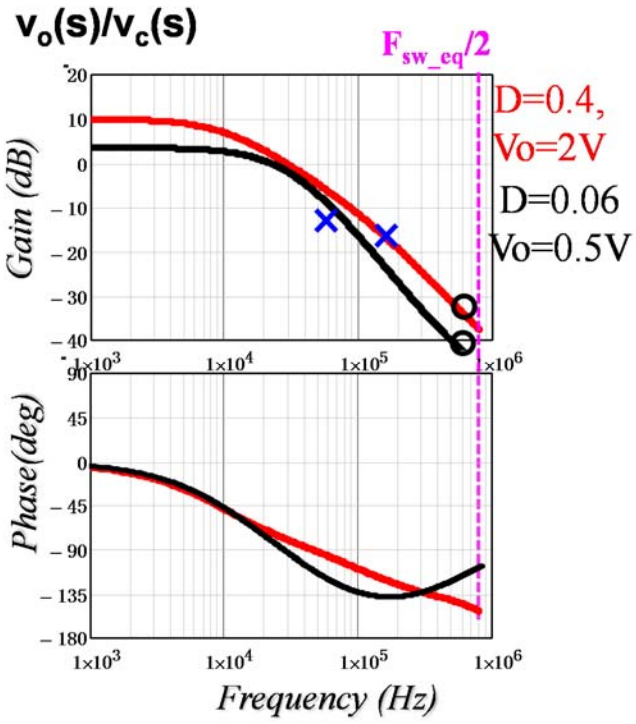


Figure 2. 23. Control-to-output voltage transfer function with different operating points for a 2-phase Buck converter

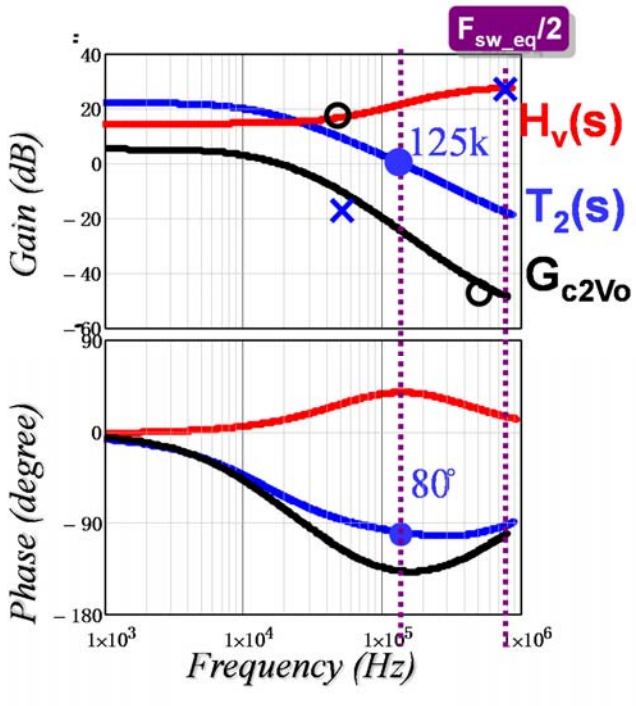


Figure 2. 24. Bode plots of control-to-output voltage, compensator H_v and loop gain T_2 @V_o=0.05V

As shown in Figure 2. 24, when output voltage is 0.05V, the loop gain bandwidth is 125kHz with 80 degree phase margin. Figure 2. 25 shows with this design, when output voltage is 2V, as the zero can not cancel the pole, the bandwidth is increased. In this case, the bandwidth is 300kHz with around 80 degree phase margin. By this worst-case design strategy, the system has very good phase margin over the wide duty cycle range, however, the bandwidth varies due to the moving pole and the lowest bandwidth limits the output capacitor design.

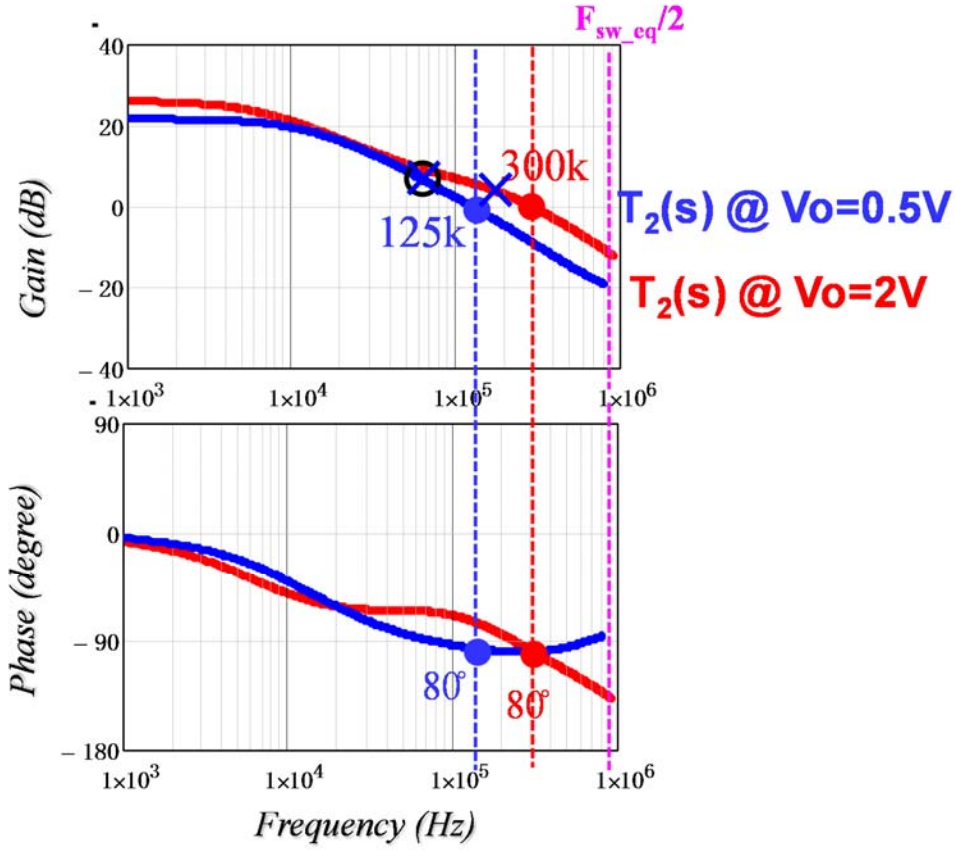


Figure 2. 25. Loop gain T_2 comparisons @V_o=0.05V and @V_o=2V by worst case design strategy.

2.6.2 Adaptive ramp design strategy

To solve the issue of bandwidth variation over wide duty cycle range, some smart control strategy such as auto-tuning concept can be employed. The auto-tuning of external ramp by sensing

the real inductor current slope is proposed in [C38] in constant-frequency peak current mode control to control the quality factor of the double pole. This method can also be extended to constant on-time current mode control to anchor the pole position caused by external ramp compensation, i.e. adaptive tune external ramp to fix the pole position. For multi-phase constant on-time current mode control, the pole position caused by external ramp is shown in (2. 19). The external ramp required to fix the low frequency pole position is shown as follows:

$$s_e = K \cdot s_{fs} = \left(\frac{n}{2\pi T_{sw} f_{pe}} - 0.5 \right) \cdot s_{fs} \tag{2. 24}$$

The basic concept is to directly sensing the summed inductor current slope using differentiation [C38]. By this way, all possible variations from the duty cycle, component tolerance are considered as they are included in the real inductor current slope. One possible implementation is shown in Figure 2. 26.

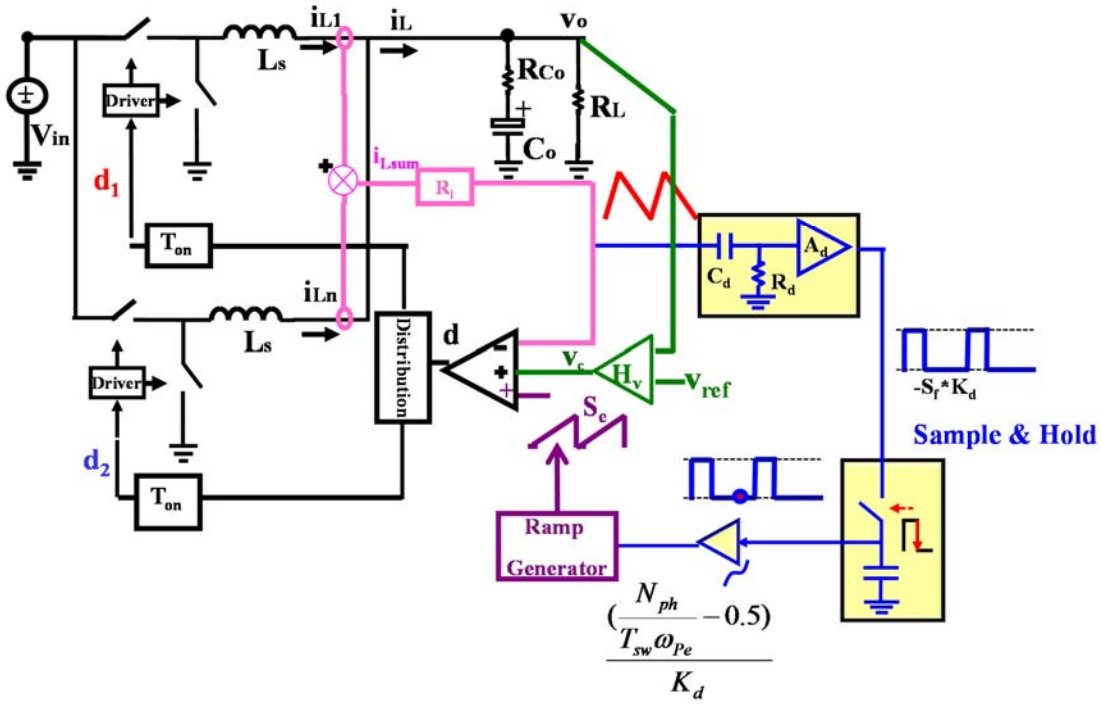


Figure 2. 26. One implementation of auto-tuning strategy based on analog differentiation block.

As shown in Figure 2. 27, with adaptive ramp design, the bandwidth of the loop gain in the example can be fixed at around 300kHz, therefore, the number of output capacitors can be saved compared with worst case design strategy.

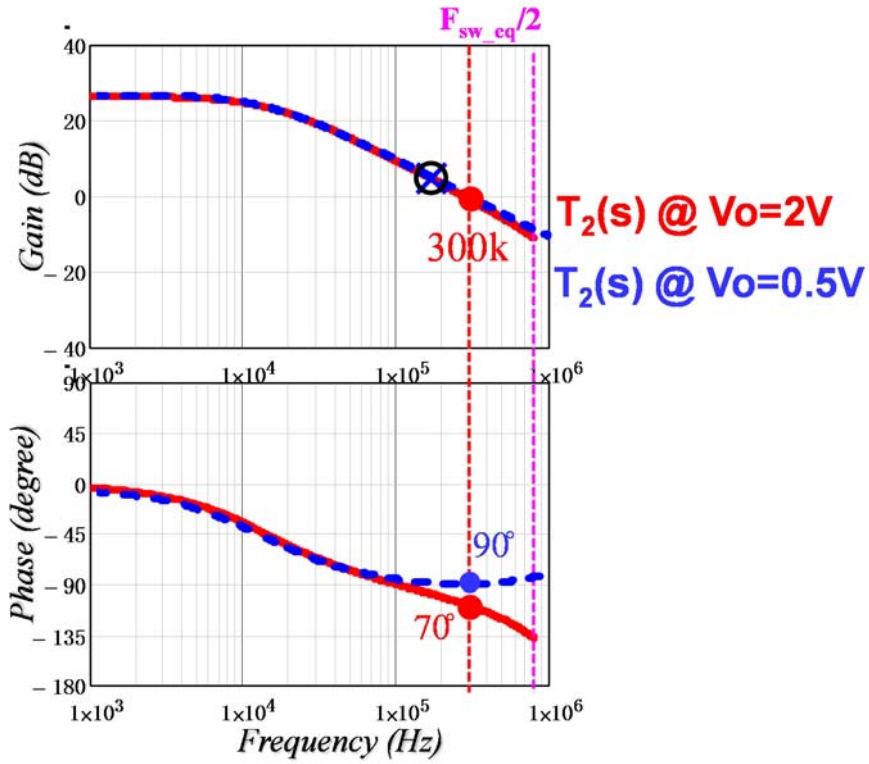


Figure 2. 27. Loop gain T_2 comparisons @V_o=0.05V and @V_o=2V by auto-tuning strategy.

2.7 Simulation and Experimental Verification

Figure 2. 28 shows simulation verification for single phase constant on time current mode control with the following parameters: F_{sw}=300kHz, V_{in}=12V, V_o=1.2V, L_s=300nH, R_L=100mΩ, 8 OSCON capacitors (6mΩ/560uF), R_i=10mΩ, s_e=1s_f. All four transfer functions including control-to-output voltage, audio susceptibility, output impedance and input impedance are compared. The results from proposed equivalent circuit model shown in Figure 2. 13 agrees with simulation results well up to 1/2 f_{sw} for all transfer functions.

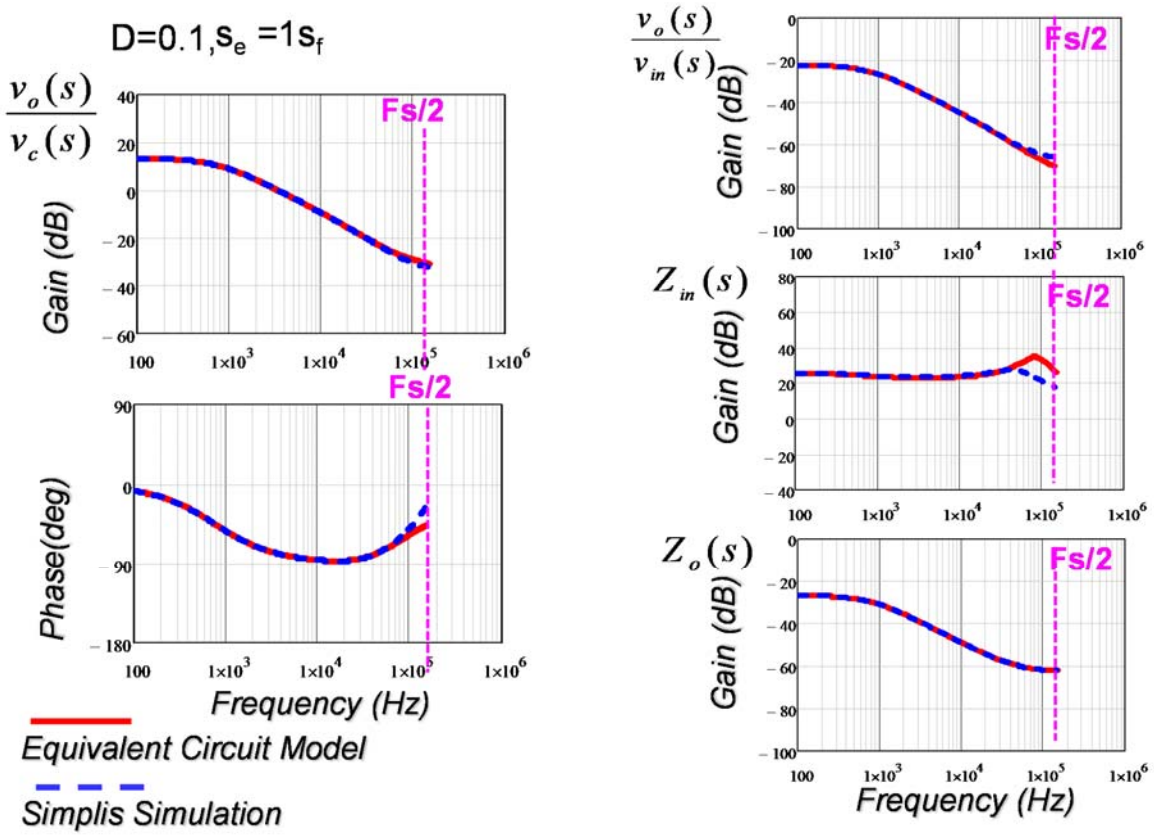


Figure 2. 28. Simplis verification for single-phase constant on-time current mode with D=0.1 and S_e=1S_f.

Figure 2. 29 shows verification of control-to-output transfer functions for different duty cycles with s_e=1s_f. For all cases, the proposed equivalent circuit model shown in Figure 2. 13 agrees very well with simulation results up to 1/2 f_{sw}. When duty cycle is larger, the phase boost is less: as shown in Figure 2. 29, at 1/3 f_{sw}, for D=0.1, the phase is -60deg, while for D=0.5 and D=0.9, the phases drop to -80 and -100, respectively. The phenomenon is consistent with the conclusion from [C35], where it is found that the phase leading property of the constant on-time modulator is related with off-time: Larger duty cycle means smaller off-time, which leads to smaller phase leading.

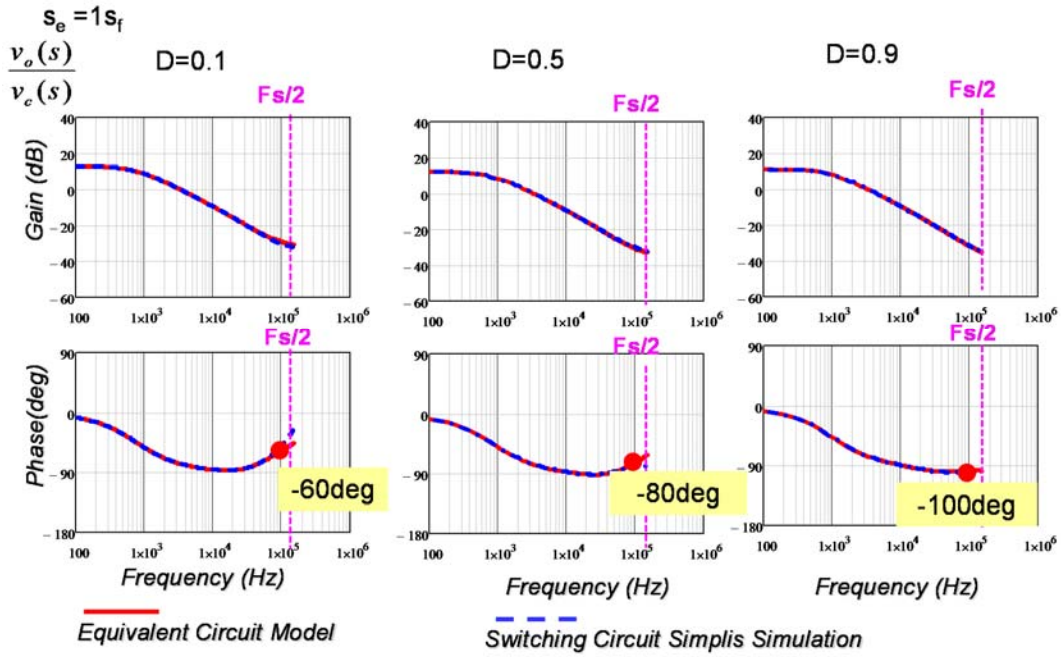


Figure 2. 29. Simplis verification of control to output voltage transfer function for single phase constant on-time current mode with various duty cycles and $s_e=1s_f$.

Figure 2. 30 shows verification of control to output voltage transfer function with different external ramps and 0.1 duty cycle. In all cases, the model agrees well with simulation result up to ½ f_{sw}. When external ramp is large, the circuit changes from first order current mode control to second order voltage mode control, with high frequency phase boost due to the stationery zero.

Figure 2. 31 shows simulation verification of two-phase constant on-time current mode control with the following parameters for each phase: F_{sw}=800kHz, D=0.4, V_{in}=5.2V, V_o=2V, L_s=150nH, R_i=10mΩ, Total output capacitors are 20 ceramic capacitors (22uF/5mΩ). The control to output voltage and audio susceptibility transfer functions predicted by equivalent circuit model shown in Figure 2. 22 agree very well with simplis simulation results up to ½ f_{sw}. Figure 2. 32 shows loop gain verification with the compensator shown as in Figure 2. 24 by worst-case design strategy. The agreements verify the proposed equivalent circuit model and proposed design strategy.

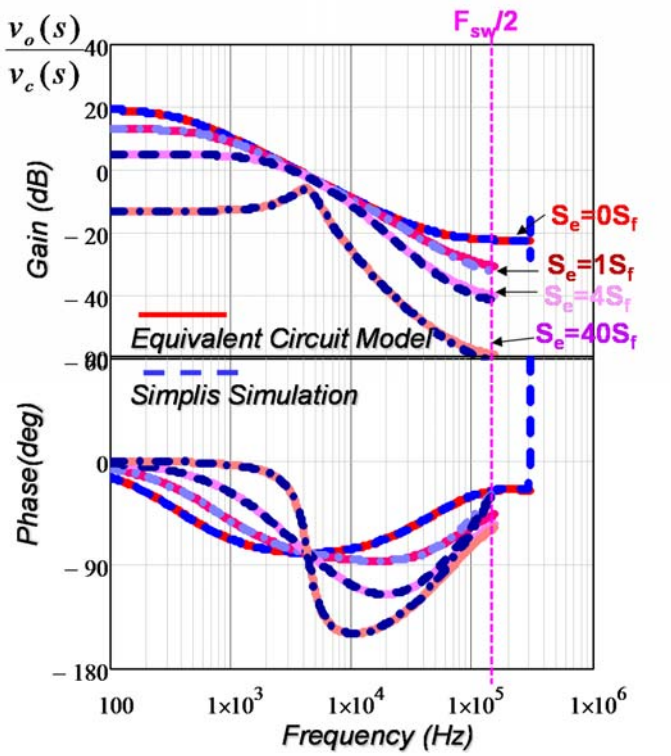


Figure 2. 30. Simplis verification of control-to-output voltage transfer function for single-phase constant on time current mode with different external ramps.

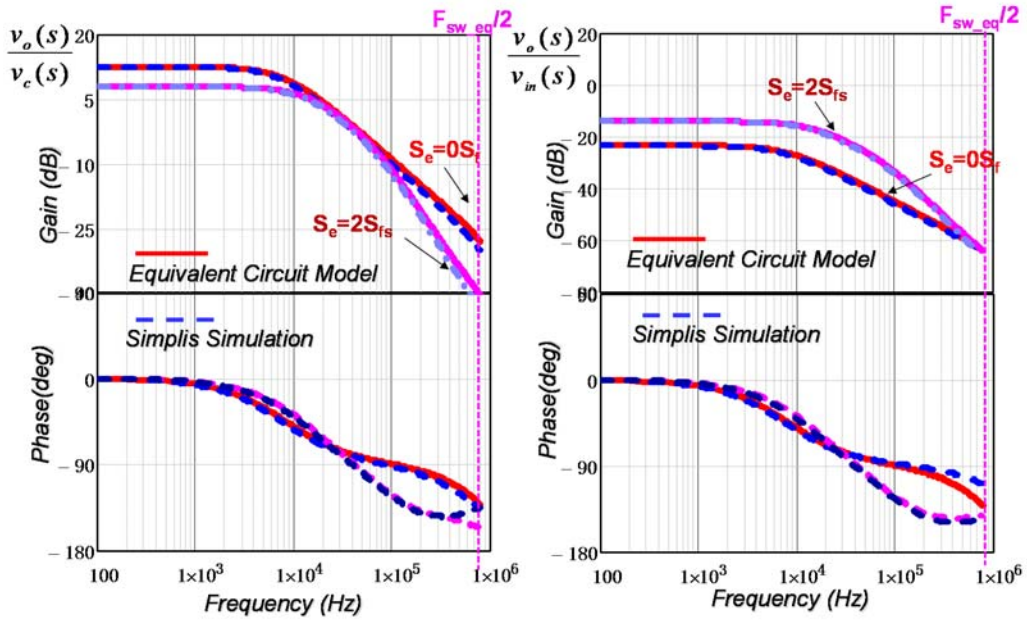


Figure 2. 31. Simplis verification of control to output voltage transfer function and audio susceptibility for 2-phase constant-on-time current mode.

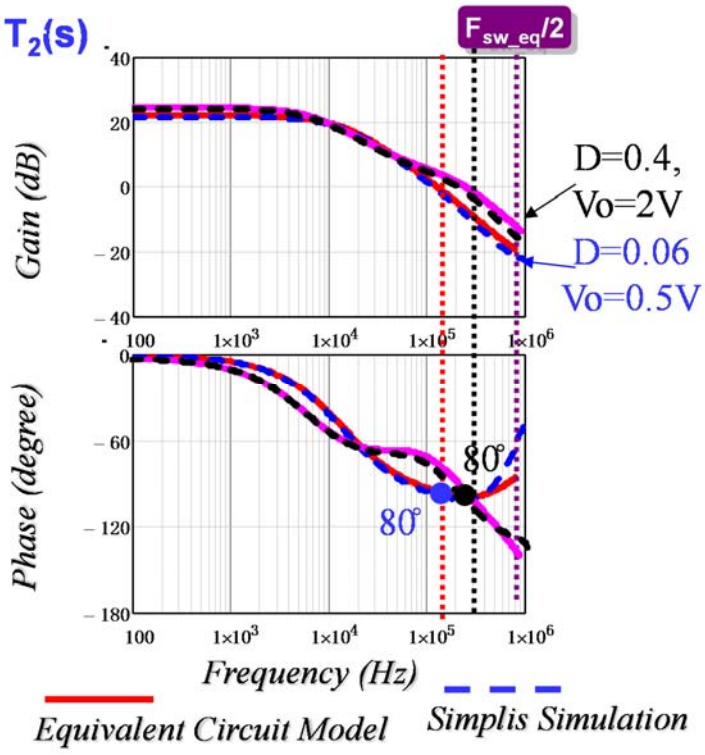


Figure 2. 32. Simplis verification of loop gain transfer function for 2-phase constant-on-time current mode by worst-case design strategy.

Figure 2. 33 and Figure 2. 34 shows the experimental verification based on Demoboard RT8859M from Richtek Inc. with the following circuit parameters: V_{in}=6V; V_o=1V; Io = 4A; phase number n=4; For each phase D ≈ 0.2; T_{sw} ≈ 315kHz; L_s=300nH; Effective current sensing gain R_i ≈ 10mΩ; Output capacitor: 7 OSCON Caps (560uF/6mΩ); The external ramp is implemented inside the controller RT8859M and the magnitude is 133kV/s, or around 40mV per switching cycle which corresponding to around 1.2S_f in experiment. From Figure 2. 33, although the operating point is around cancellation point, jittering performance is good due to the help of the external ramp. Figure 2. 34 shows verification of control-to-output transfer function. Compared with measurement data, the equivalent circuit model accurately predicts the small-signal behavior. As analyzed in previous sessions, the high frequency phase boost due to the stationary zero is also observed in measurement.

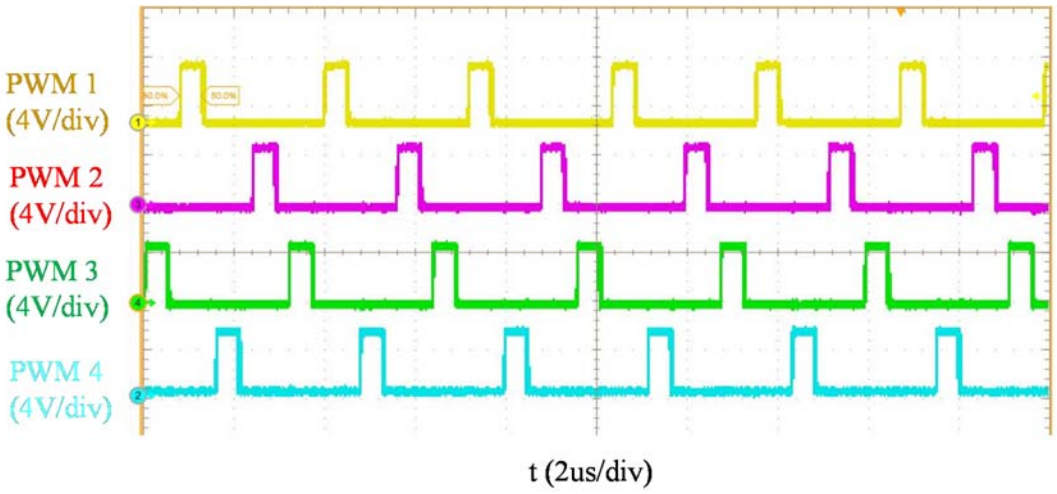


Figure 2. 33. Steady-state waveforms and jittering performance for 4-phase constant-on-time current mode control with external ramp.

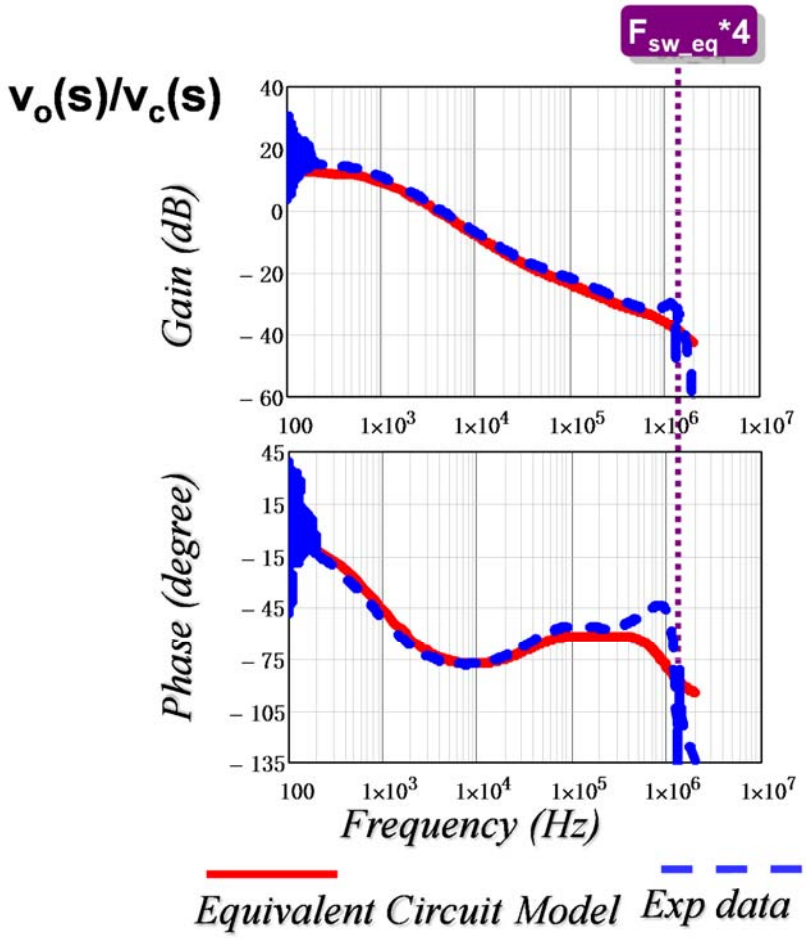


Figure 2. 34. Experimental verification of control-to-output transfer function.

2.8 Summary

This chapter first analyzes the effect of external ramp on small-signal model of constant on-time current mode control. It is found that external ramp brings additional dynamics by introducing a moving pole and a static zero. Next, a three-terminal switch model is proposed based on non-ideal current source concept, where the non-idealness of the current source is presented by a R_{e2}-L_{e2} branch. The equivalent circuit model is an extension of previous unified three-terminal switch model proposed in [C34] and can be reduced to constant on time voltage mode model [C35]when external ramp is extremely large. Furthermore, the model is extended to multi-phase current mode control and design guidelines are proposed based on either worst case design strategy or auto-tuning strategy.

Chapter 3. Unified Equivalent Circuit Model of V^2 Control

3.1 Introduction

V^2 control has advantages of simple implementation and fast transient response and is widely used in industry for POL and VR applications. This control scheme is elegant when output capacitors with large RC time constants are employed, such as OSCON capacitors. However, in most cases using capacitors with small RC time constant, such as ceramic capacitors, instability problem will occur. As discussed in section 1.2.2, although the sampled-data modeling [D13] [D38]-[D41], discrete-time analysis [D35]-[D37] [D42], the time domain analysis [D43]- [D45] have already been successfully employed to predict the critical instability condition for V^2 control. All these models can only predict the boundary between stable and unstable operation and no stability margin can be controlled for design purpose. Furthermore, these methods are very mathematical and are difficult for practically engineers. The describing function method is successfully employed in V^2 control to derive continuous time domain control-to-output and output impedance transfer functions [D46][D49]. However, the models in [D46][D49] are incomplete as other properties of V^2 controlled converter, such as audio susceptibility and input impedance, are still lacking. Furthermore, the mathematical derivation of this model is very complicated and time consuming. If some modification has been done to the original V^2 control, engineers need to redo the complicated derivation to derive the small-signal model, which is tedious and time consuming. In addition, as all the feedback information is lumped together as a black box to derive the model, little physical insight is provided. The above limitations trigger the motivation to derive an equivalent circuit model for V^2 control, previous equivalent circuit model [D48] tries to obtain an equivalent circuit model of V^2 control based on equivalent circuit model

of current mode control. The model is accurate when capacitor voltage ripple is much smaller than ripple voltage across ESR, or in another way, with capacitors having large RC time constants, such as OSCON capacitors. However, this model fails to predict the instability associated with ceramic capacitors, as shown in Figure 1.27. Up to now, no equivalent circuit model is proposed which is able to predict instability issue in V^2 control. This chapter proposes a unified equivalent circuit model which is suitable to all kinds of capacitors by considering the effect of both inductor current ripple and capacitor voltage ripple. The equivalent circuit model is a simple yet accurate, complete model and can be used to investigate all transfer functions. The proposed equivalent circuit model is applicable to both variable frequency modulation and constant frequency modulation. Furthermore, the model can be extended to enhanced V^2 control (which is utilized in VR application where there a certain load-line requirement) and multi-phase V^2 converters. The equivalent circuit model is verified with Simplis simulation and experimental results. The major content of this chapter is published in [D50] and [D51].

3.2 Equivalent Circuit Model Development of Constant On-time V^2

3.2.1 Sideband effect analysis in V^2 control

In switching mode power converter, the pulse width modulator is non-linear: When control signal has small-signal perturbation with frequency f_m, the modulator generates multiple frequency components: fundamental component (f_m), the switching frequency component (f_{sw}) and its harmonics ($n*f_{sw}$), and the sideband components ($f_{sw}\pm f_m$, $nf_{sw}\pm f_m$).

For traditional voltage mode control, state-space average concept has been well established [B2]. With averaging concept, switching frequency component is eliminated and therefore the sideband component is not considered. In [B7], the reason why the average model loses accuracy

when modulation frequency is close to half of switching frequency is explained by the sideband effect: with closed loop, additional f_m is generated when the sideband frequency f_{sw}-f_m goes through modulator. This part of f_m is ignored in average model which makes the average concept loses its accuracy in high frequency range. In the example shown in [B7], for a 1MHz switching converter, in the 400kHz bandwidth design, the average model is good only up to 100kHz, i.e. one-tenth of the switching frequency. Taking into consideration of the sideband effect, a multi-frequency small-signal model is proposed for buck converters with voltage mode control in [B7] and the model is applicable beyond half of the switching frequency.

For current mode control, the scenario is similar but more complex as the sideband of inductor current needs to be considered in inner current loop [C32]. It is very hard to consider the sideband effects directly in the frequency domain and time-domain analysis is utilized in the describing function (DF) modeling approach in [C32][C39]. The DF method is applied to the closed-loop time-domain waveform to model the non-linear current-mode modulator. By doing so, the sideband effect of the inductor current has been taken into consideration and the model is accurate up to switching frequency. An equivalent circuit model, which has clear physical insight, is proposed based on non-ideal current source concept in [C34][C39]. The non-idealness of the current source is caused by the sideband effect of inductor current: for peak current mode control, it causes a pair of double pole at half of switching frequency. For constant on-time current mode control, it causes a pair of double pole at $1/(2*D*f_{sw})$: When D is small, the double pole is at very high frequency and its effect is small. Therefore, for constant on-time current mode with small duty cycle, inductor current sideband effect can be neglected and the current source can be regarded as ideal.

For V^2 Control, the scenario is even more complicated than current mode control. The output voltage is the sum of the voltage across ESR and the voltage across the capacitance. The voltage across ESR contains information of the inductor current and load current. Therefore, from modeling point of view, the direct feedback of output voltage can be separated into three parts, shown as (3. 1). Usually, the outer loop of V^2 control is a low bandwidth compensator, which is straight forward in modeling. The small signal modeling effort is mainly focused on the complicated inner direct feedback loop of V^2 control.

$$v_o = i_{Co} \cdot R_{Co} + v_{cap} = i_L \cdot R_{Co} - i_{Load} \cdot R_{Co} + v_{cap} \quad (3.1)$$

Figure 3. 1 explicitly shows three feedback paths and shows frequency spectrum of each feedback path when control signal is under modulation. Similar as current mode control, inductor current feedback does not have a low pass filter, so all the sidebands (f_{sw}-f_m, f_{sw}+f_m, etc.) are fed back to the modulator and the sideband effect needs to be considered. The capacitor voltage loop is a direct feedback without any compensation. Therefore, the sidebands of capacitor voltage also need to be taken into consideration. As a result, the scenario in V^2 control is even more complicated than current mode control: not only does the inductor current sideband effect needs to be considered, but also the capacitor voltage sideband effect. The load current feedback is simpler and only modulation frequency component needs to be considered: for a practical voltage regulator, the impedance of capacitor branch is usually much smaller than that of load resistor at $f>f_{sw}/10$. Therefore, sideband of inductor current mainly flow through the capacitor and sideband in load current are negligible.

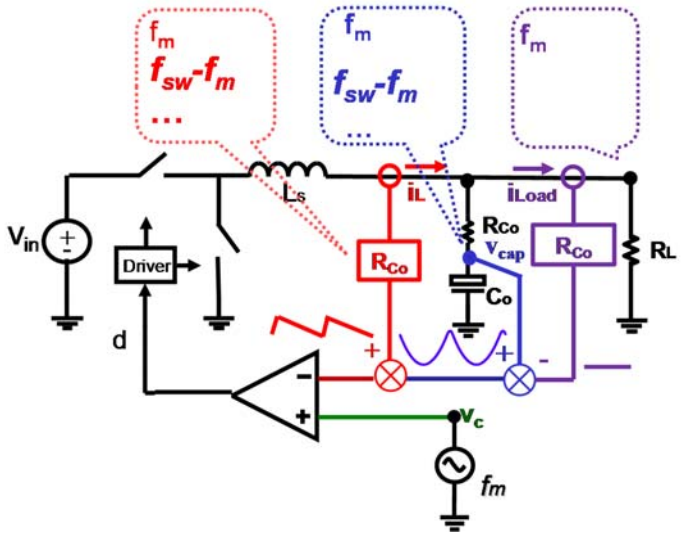


Figure 3. 1. Frequency spectrum for inner loop of V^2 control with three feedback paths.

The fact that both the sidebands of inductor current and capacitor voltage participate in modulation makes it extremely difficult for modeling in frequency domain. Similar as in current mode control, the most successful continuous small-signal model is derived in [D46] based on describing function method. Both sidebands of inductor current and capacitor voltage are included and the model is accurate up to switching frequency.

The control-to-output transfer function of constant on-time V^2 control for small D is shown in the following:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_3\omega_2}+\frac{s^2}{\omega_2^2})}, \qquad Q_3 = \frac{T_{sw}}{\pi(R_{Co}C_o - \frac{T_{on}}{2})}, \omega_2 = \frac{\pi}{T_{sw}} \tag{3. 2}$$

As shown in Figure 3. 2, the gain is unity (0dB) up to frequency close to ½ f_{sw}, where a pair of double pole occurs, the quality factor of this double pole is related with capacitor parameters. This double pole is caused by capacitor voltage sidebands, as the effect of inductor current sideband can be neglected for constant on-time modulation with small duty cycle [C32]. Basically, the capacitor voltage loop changes the converter into a non-ideal voltage source.

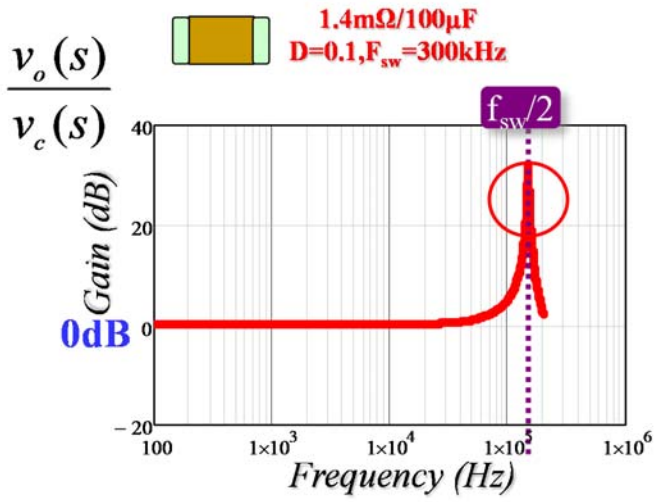


Figure 3. 2. Bode plot of control-to-output transfer function for ceramic capacitor (1.4mΩ/100uF) with D=0.1 and F_{sw}=300kHz.

In short, for current mode control, inductor current sideband effect is critical and the equivalent circuit model shown in [C32] [C34] [C39] clearly shows the inductor current loop turns the converter into a non-ideal current source and the sideband effect is responsible for the non-idealness of the current source. For V^2 control, the modeling result shown in [D46] reveals that capacitor voltage loop turns the converter into a non-ideal voltage source.

3.2.2 Equivalent circuit representation of constant on-time V^2 control

As shown in the previous analysis, the buck converter with V^2 control can be regarded as a non-ideal voltage source. To derive an equivalent circuit model to represent this non-ideal voltage source, the methodology is to establish the connection between V^2 control and current mode control, as the equivalent circuit model of current mode control is well established in [C32][C34]. The circuit shown in Figure 3. 1 is manipulated by combining the control signal, load current signal and capacitor voltage, as shown in Figure 3. 3(a). The combination signal, v_{c2} is used as a reference to control inductor current. Note v_{c2} contains the information as follows:

$$v_{c2}(f_m) = v_{c1}(f_m) - v_{cap}(f_m) - v_{cap}(f_s - f_m) \quad (3.3)$$

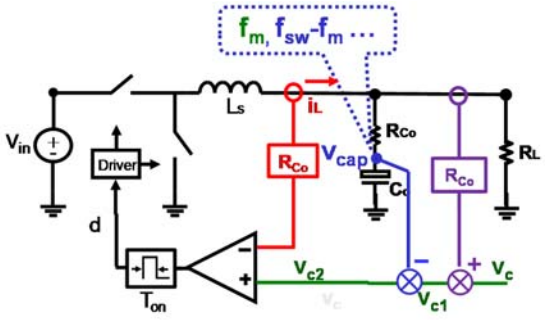
With this manipulation, equivalent circuit model of current mode control in [C32] can be employed, as shown in Figure 3. 3(b). Compared with current mode control, two more current sources appeared in V^2 control. To understand the contribution of the green current source which is controlled by the modulation frequency of capacitor voltage, the following assumption is made:

$$\hat{v}_{cap}(f_m) \approx \hat{v}_o(f_m) \quad (3.4)$$

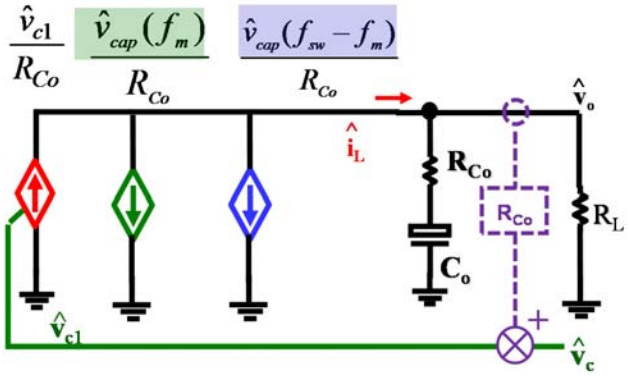
The magnitude of the green current is $\hat{v}_o / R_{Co}$, while the voltage across the current source is $\hat{v}_o$. Therefore, this current source essentially is a resistor with the magnitude of R_{Co}, as shown in Figure 3. 3(c). With Thevenin's theorem, now it is clear that modulation frequency of capacitor voltage feedback actually turns the current source into a voltage source, as shown in Figure 3. 3 (d).

In current mode control, the inductor current sideband effect is represented by an impedance comprised by R_e and C_e, which will resonate with power stage inductor to form a pair of double pole at high frequency [C34]. For V^2 control, capacitor voltage sideband also cause a pair of double poles, as shown in Figure 3. 2. Using similar concept, it is assumed that the effect of capacitor voltage sideband is equivalent to an impedance comprised by R_{e2} and L_{e2}, as shown in Figure 3. 3(e). This impedance resonates with output capacitor to represent the double pole at ½ f_{sw}. Based on the result shown in (3. 2), the expression of R_{e2} and L_{e2} can be derived as follows:

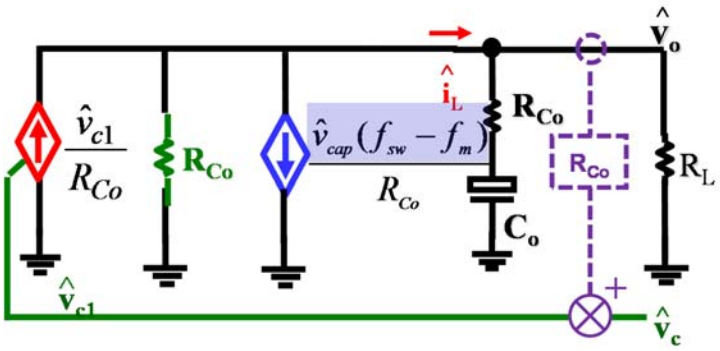
$$R_{e2} = -R_{Co} - \frac{T_{on}}{2C_o}, L_{e2} = \frac{T_{sw}^{\ 2}}{\pi^2 C_o} \quad (3.5)$$



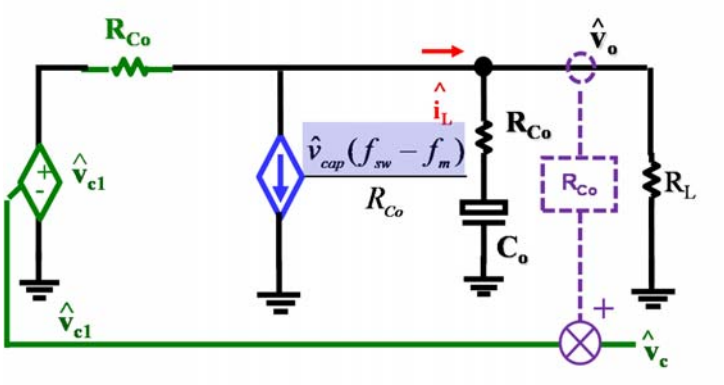
(a) Combine control signal, load current and capacitor voltage as reference for inductor current.



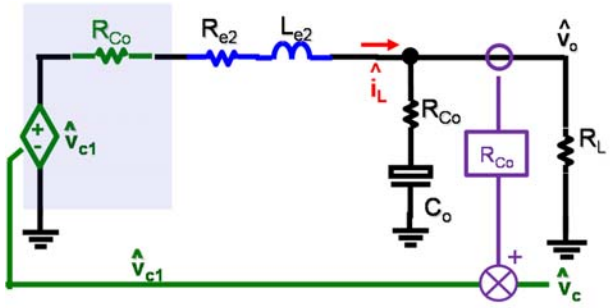
(b) Employ equivalent circuit model for current mode control in [C32].



(c) Use resistor to represent current source controlled by modulation frequency of capacitor voltage



(d) Transforming to a voltage source using Thevenin's theorem



(e) Use R_{e2}-L_{e2} branch to represent current source controlled by sideband frequency of capacitor voltage

Figure 3. 3. Derivation of equivalent circuit model of constant on-time V^2 control for small D

The transfer function shown in (3. 2) is an approximated transfer function which is only valid under small D case. When D is becoming larger, the effect of an additional double pole caused by inductor current sideband needs to be considered as it will cause additional phase delay at high frequency [D46]. The control-to-output voltage transfer function which is applicable for all duty cycle is shown as follows [D46]:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2})(1+\frac{s}{Q_3\omega_2}+\frac{s^2}{\omega_2^2})} \tag{3. 6}$$

$$Q_1=\frac{2}{\pi}, \omega_1=\frac{\pi}{T_{on}}, Q_3=\frac{T_{sw}}{\pi(R_{Co}C_o-T_{on}/2)}, \omega_2=\frac{\pi}{T_{sw}}$$

The scenario turns out to be very interesting as one pair of double pole is caused by capacitor voltage sidebands and another pair of double pole is caused by inductor current sidebands. From the knowledge of the current mode control [C32], the double pole caused by inductor current sidebands indicates that the inductor is a non-ideal current source. The expression of this double pole is the same as constant on-time current mode control shown in [C32]. Therefore, we can directly employ the equivalent circuit model for constant on-time current mode control to represent this double pole, as shown in Figure 3. 4, where the expression of R_e and C_e is shown as follows:

$$R_e = 2L_s / T_{on}, C_e = T_{on}^2 /(L_s \pi^2) \tag{3. 7}$$

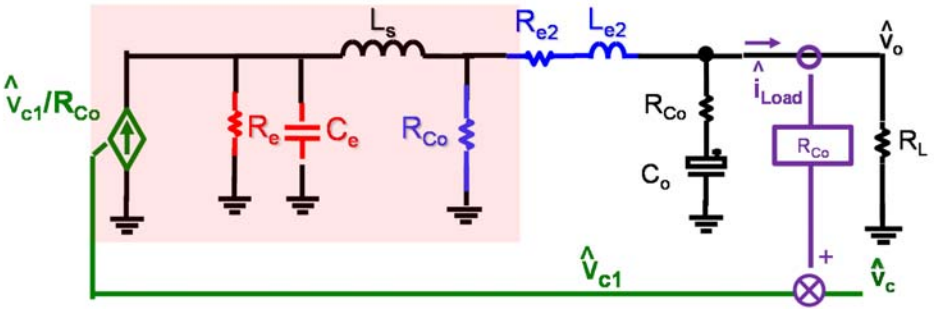


Figure 3. 4. Equivalent circuit model of constant on-time V^2 control considering double pole caused by inductor current sidebands.

Figure 3. 4 shows that the inductor current loop turns the power stage into a non-ideal current source, with the non-idealness shown by resonance between C_e and L_s; the capacitor voltage loop turns the non-ideal current source into a non-ideal voltage source, with the non-idealness shown by resonance between L_{e2} and C_o. Now use the same derivation strategy as unified three-terminal switch model for current mode control in [C34], the input property can also be considered and the complete model for constant on-time V^2 control is shown as Figure 3. 5, where the expressions of R_{in}, G_o, G_{Ls}, K_{in} are shown as follows:

$$R_{in} = -\frac{V_{in}}{DI_c}, G_{Ls} = \frac{I_c}{V_{in}}, G_o = (\frac{I_c}{V_{in}} - \frac{D}{R_{Co}}), K_{in} = \frac{D'}{D} \tag{3. 8}$$

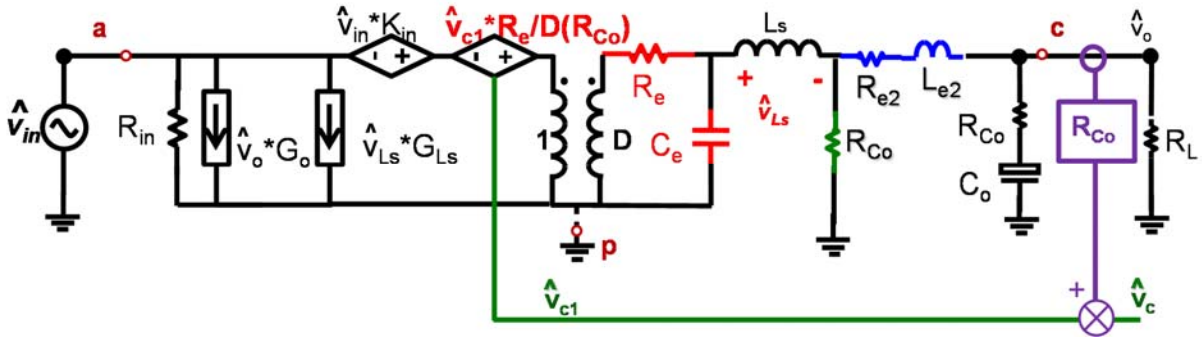


Figure 3. 5. Complete equivalent circuit model of constant on-time V^2 control

3.3 Discussion on Equivalent Circuit Model of Constant on-time V^2

3.3.1 Physical meaning of equivalent circuit

The equivalent circuit model reveals that the inductor current feedback turns the power stage into a non-ideal current source. The non-idealness of this current source is shown in equivalent circuit by resonance between virtual C_e and power stage inductor L_s, which forms a pair of double pole at $1/(2D)* f_{sw}$. The capacitor voltage feedback turns current source into a non-ideal voltage source. The non-idealness of this voltage source is shown in equivalent circuit by resonance between virtual L_{e2} and output capacitor C_o, which forms another pair of double pole at $1/2\ f_{sw}$. The strategy to represent double pole caused by inductor current sideband and capacitor voltage sideband is very similar: inductor current sideband effect is represented by resonance between a virtual capacitor C_e and power stage inductor L_s, while capacitor voltage sideband effect is represented by resonance between a virtual inductor L_{e2} and power stage capacitor C_o. For Constant on-time V^2 control, the capacitor voltage sidebands may cause the circuit unstable. The damping factor of the double pole caused by capacitor voltage sideband is decided by the damping resistance R_{damp} in the resonance loop. The expressions of the damping resistor R_{damp} and the quality factor of the double pole are shown as follows:

$$R_{damp} = R_{Co} - \frac{T_{on}}{2C_o}, Q_3 = \frac{1}{R_{damp}}\sqrt{\frac{L_{e2}}{C_o}} = \frac{T_{sw}}{\pi(R_{Co}C_o - \frac{T_{on}}{2})} \quad (3.9)$$

R_{damp} can be negative or positive, depending on the capacitor parameter, which means that the double pole may lie in right-half-plane and the circuit may run into instability problem.

3.3.2 Capacitor parameter effect on dynamic performance

Using OSCON capacitors (6mΩ/560uF), R_{damp} is 710u, which is large and Q_3 is around 0.3, R_{e2} and L_{e2} in Figure 3. 3(c) in this case can be neglected, and it is a well-controlled voltage source. For a comparison, for a special ceramic capacitor (3mΩ/220uF), R_{damp} is 280u and Q_3 is 2.5, although it is stable, there is a large peaking shown in Figure 3. 6 which means the dynamic performance is bad. For another type of traditional ceramic capacitor (1.4mΩ/100uF), R_{damp} is -33u, which means the circuit is unstable.

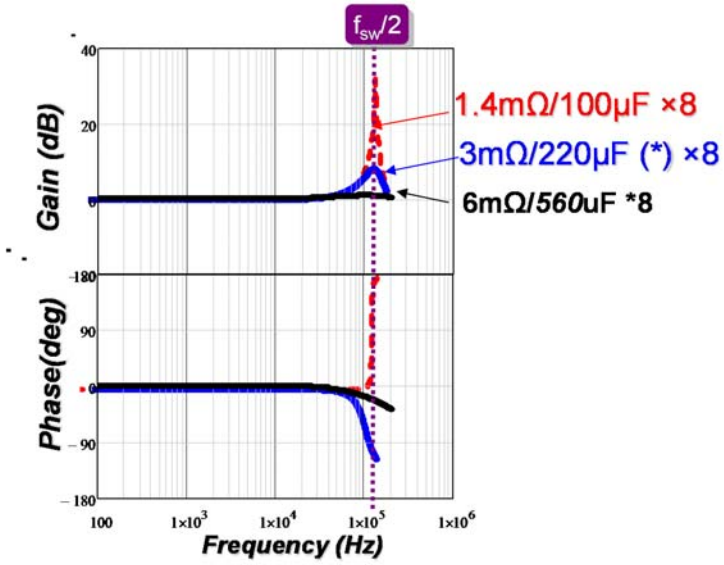


Figure 3. 6. Control-to-output transfer function comparisons with different output capacitors.

The methods to solve the instability problem and optimal design of the parameters will be discussed further in Chapter 4.

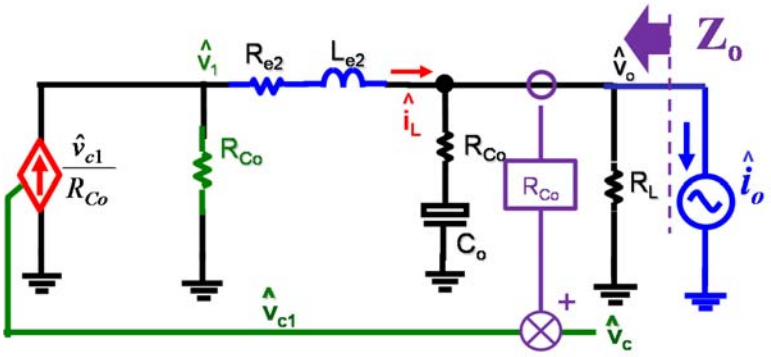
3.3.3 The effect of load current feedback

For V^2 control, there is inherent load current feedback as shown in (3. 1). The load current feedback is negligible from control to output transfer function point of view [D48]. However, it has dramatic effect on output impedance. Figure 3. 7(a) shows the output impedance with load current feedback loop. As it is a linear circuit, the output impedance without load current feedback loop can be solved as follows:

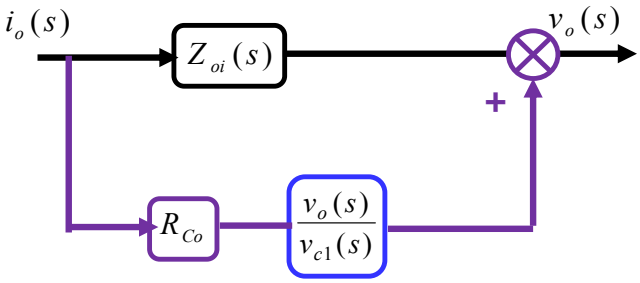
$$Z_{oi}(s) \approx -(R_{Co} + sL_{e2}) \tag{3. 10}$$

Figure 3. 7(b) shows that the output impedance with load current loop has two paths, one path is Z_{oi} and the second path is a constant gain R_{Co} multiplying control to output transfer function. The total output impedance can be solved as follows:

$$Z_o(s) \approx Z_{oi}(s) + R_{Co} \approx -sL_{e2} \tag{3. 11}$$



(a) Output impedance derivation with load current perturbation



(b) Block diagram for derivation of output impedance

Figure 3. 7. Output impedance derivation with load current feedback loop.

As shown in Figure 3. 8, the load current feedback makes the DC output impedance zero and reduces the output impedance at low frequency. Figure 3. 7 illustrates a physical scenario of low output impedance and fast transient response of V^2 control: through load current feedback, the control signal senses the load current information, therefore, inductor provides the incremental load current without capacitor voltage disturbance. This makes the output impedance of V^2 control extremely small, which means that with the help of the inherent load current feedback, the circuit is an excellent voltage source with very small internal impedance.

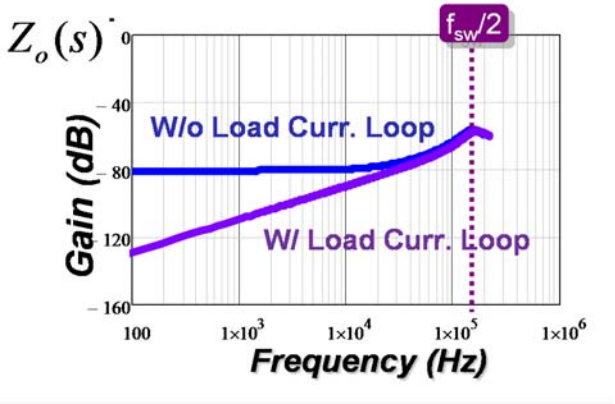


Figure 3. 8. Comparisons of output impedance between with and without load current loop.

3.4 Extension to Enhanced Constant on-time V^2 Control

For VR application, adaptive voltage position is recommended. As a result, additional inductor current information is sensed and injected into control, as shown in Figure 3. 9. This structure is called enhanced constant on-time V^2 control and is widely used in commercial VR products [D54][D55].

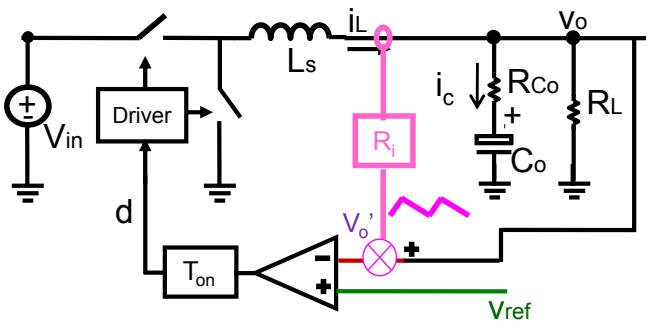
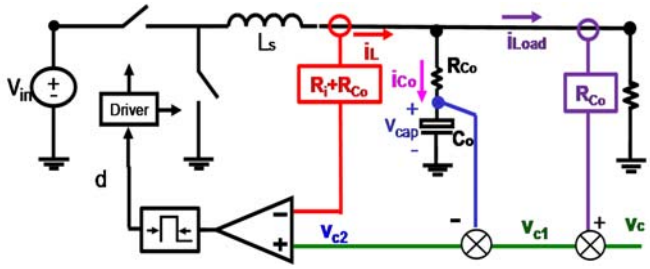
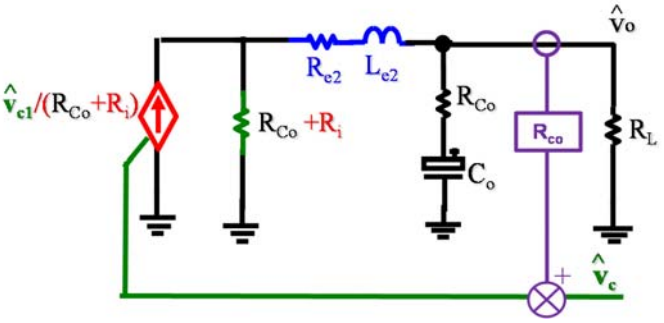


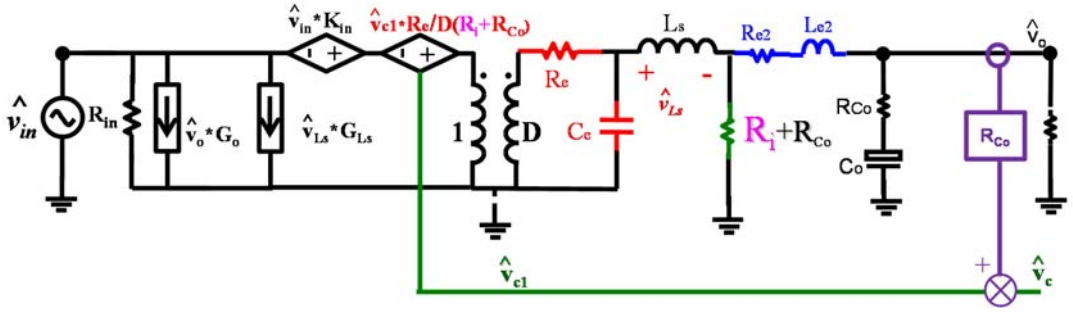
Figure 3. 9 Diagram of enhanced constant on-time V^2 control



(a) Combine control signal, load current and capacitor voltage as reference for inductor current.



(b) Equivalent circuit model to derive control-to-output voltage transfer function for small D



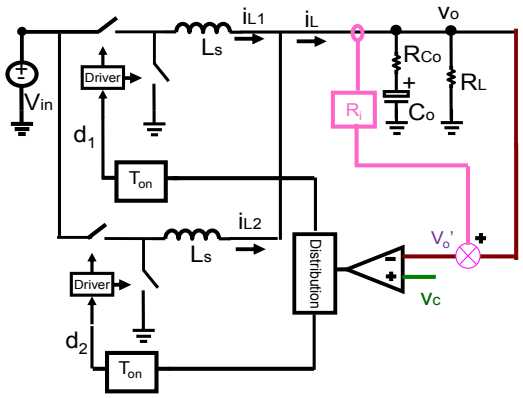
(c) Three-terminal switch model for enhanced constant on-time V^2 control

Figure 3. 10. Derivation of three-terminal switch model for enhanced constant on-time V^2 control

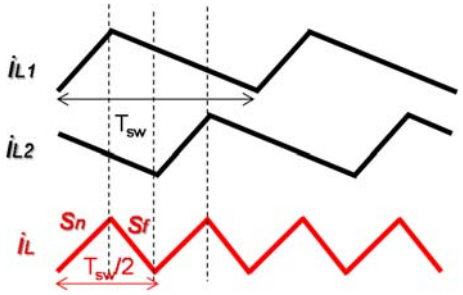
The prediction of control-to-output transfer function, output impedance and design guideline for VR application will be discussed in Chapter 4.

3.5 Extension to Multi-phase Constant on-time V^2 control

The equivalent circuit model is also extended to multi-phase constant on-time V^2 and enhanced V^2 converters. Several commercial products use multi-phase constant on-time enhanced V^2 control based on pulse distribution method for VR application [D54][D55]. As shown in Figure 3. 11(a), the summed inductor current is sensed and added on top of output voltage for modulation purpose. If R_i=0, then this control structure becomes multi-phase constant on-time V^2 control. The derivation strategy is to derive an equivalent single-phase converter and use the equivalent circuit model of single-phase converter.



(a)



(b)

Figure 3. 11. (a) Diagram of two-phase enhanced constant on-time V^2 control (b) Waveforms of phase inductor current and summed inductor current

Figure 3. 11 (b) shows the waveforms of phase inductor current and summed inductor current. For a two-phase converter, the summed inductor current rising and falling slope for duty cycle non-overlap case is shown as follows:

$$s_{n\_2} = R_i \frac{V_{in} - 2V_o}{L_s} = R_i \frac{V_{in}/2 - V_o}{L_s/2}, s_{f\_2} = R_i \frac{2V_o}{L_s} = R_i \frac{V_o}{L_s/2} \quad (3.12)$$

Following the same reason, for n-phase converter, the rising slope and falling slope for summed inductor current for duty cycle non-overlap case is shown as follows:

$$s_{n\_n} = R_i \frac{V_{in} - nV_o}{L_s} = R_i \frac{V_{in}/n - V_o}{L_s/n}, s_{f\_n} = R_i \frac{nV_o}{L_s} = R_i \frac{V_o}{L_s/n} \quad (3.13)$$

From (3. 13), for n-phase constant on-time enhanced V^2 control structure, from small-signal point of view, it is equivalent to the single-phase constant on-time enhanced V^2 control, as shown in Figure 3. 12. the equivalent switching frequency is n times that of single phase, the inductor is reduced to one-n_{th} of the single phase inductor and the input voltage is also reduced to one-n_{th}.

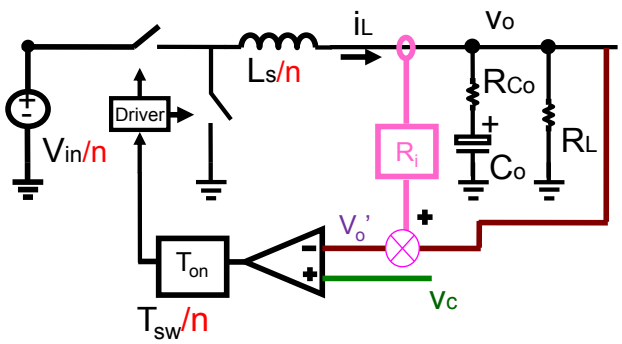


Figure 3. 12. Equivalent single phase constant on-time enhanced V^2 control

Therefore, the equivalent circuit model for multi-phase constant on-time enhanced V^2 control can be derived, as shown in Figure 3. 13.

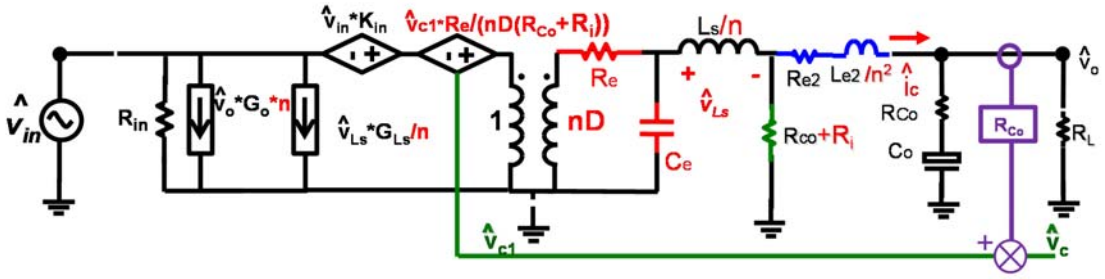


Figure 3. 13. Complete equivalent circuit model of n-phase constant on-time enhanced V² Control.

The damping factor of the double pole caused by capacitor voltage loop is shown as follows:

$$Q_{3\_n} = \frac{1}{R_{damp}}\sqrt{\frac{L_{e2}/n^2}{C_o}} = Q_3/n \tag{3. 14}$$

As shown in Figure 3. 14, compared with single phase, the double pole frequency for two-phase converter is twice and the quality factor is one-half. Generally speaking, for multi-phase converter, the damping is improved compared with single phase converter.

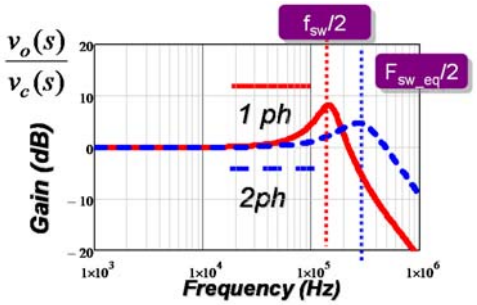


Figure 3. 14. Comparisons of control-to-output transfer function between one phase and two phase constant on-time V²

3.6 Extension to Other V² control Schemes

Following the same derivation strategy, equivalent circuit model for other V² control can also be derived. For constant frequency V² peak control, the small-signal control-to-output transfer function is shown as follows [D52]:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2})}, \omega_2 = \frac{\pi}{T_{sw}}$$

$$Q_{e1} = \frac{2}{\pi}\frac{1}{\alpha+\sqrt{\alpha^2+(4D-2)\alpha+(1-D)^2+D^2}} \quad (3.15)$$

$$Q_{e2} = \frac{2}{\pi}\frac{1}{\alpha-\sqrt{\alpha^2+(4D-2)\alpha+(1-D)^2+D^2}}, \alpha = \frac{R_{Co}C_o}{T_{sw}}$$

α is defined as current feedback strength and will be discussed in chapter 4.

Following similar derivation strategy as constant on-time V^2 control, the Expression of R_e C_e, R_{e2} and L_{e2} is shown as follows:

$$C_e = T_{sw}^2/(L_s\pi^2), R_e = \frac{L_s\pi}{T_{sw}}Q_{e1}, L_{e2} = T_{sw}^2/(C_o\pi^2), R_{e2} = -2R_{Co}+Q_{e2}\frac{T_{sw}}{\pi} \quad (3.16)$$

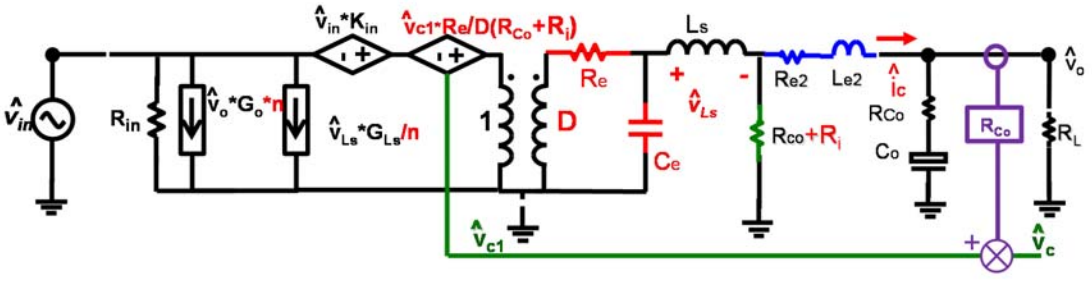


Figure 3. 15. Unified equivalent circuit model of V^2 control for different modulation schemes

Figure 3. 15 shows a unified equivalent circuit model for V^2 control, the model includes inductor current ramp R_i for all modulation schemes as it is needed to improve the dynamic performance when traditional low-ESR ceramic capacitors are employed. Besides, the model also includes external ramp compensation in constant frequency V^2 control, as it is required to solve instability problem in large duty cycle applications [D13][D46] [D52].

The difference between different V^2 control structures is that the damping and position of the double poles caused by inductor current loop and capacitor voltage loop are different. As a result,

expression of R_e, C_e, L_{e2} and R_{e2} are different. The expressions are summarized and listed in Table 3.1.

TABLE 3.1 Expressions of R_e, C_e, R_{e2} and L_{e2} in unified equivalent circuit model of V^2 control

Modulation Type	R_e	C_e	R_{e2}	L_{e2}
Constant on-time V^2	$2L_s / T_{on}$	$T_{on}^2 / (L_s \pi^2)$	$-R_{Co} - T_{on} / 2C_o$	$T_{sw}^2 / (C_o \pi^2)$
Constant off-time V^2	$2L_s / T_{off}$	$T_{off}^2 / (L_s \pi^2)$	$-R_{Co} - T_{off} / 2C_o$	$T_{sw}^2 / (C_o \pi^2)$
Constant Frequency V^2 Peak	$\frac{L_s \pi}{T_{sw}} Q_{e1}$	$T_{sw}^2 / (L_s \pi^2)$	$-2R_{Co} + Q_{e2} \cdot T_{sw} / \pi$	$T_{sw}^2 / (C_o \pi^2)$
Constant Frequency V^2 Valley	$\frac{L_s \pi}{T_{sw}} Q_{e1\_d}$	$T_{sw}^2 / (L_s \pi^2)$	$-2R_{Co} + Q_{e2\_d} \cdot T_{sw} / \pi$	$T_{sw}^2 / (C_o \pi^2)$

3.7 Simulation and Experimental Verification

Figure 3. 16 shows simulation verification for OSCON capacitors (6mΩ/560uF), with 0.1 duty cycle and 300kHz switching frequency. All four transfer functions, i.e. control-to-output, audio susceptibility, output impedance and input impedance are compared. The proposed model agrees with simulation results very well up to f_{sw} for all transfer functions.

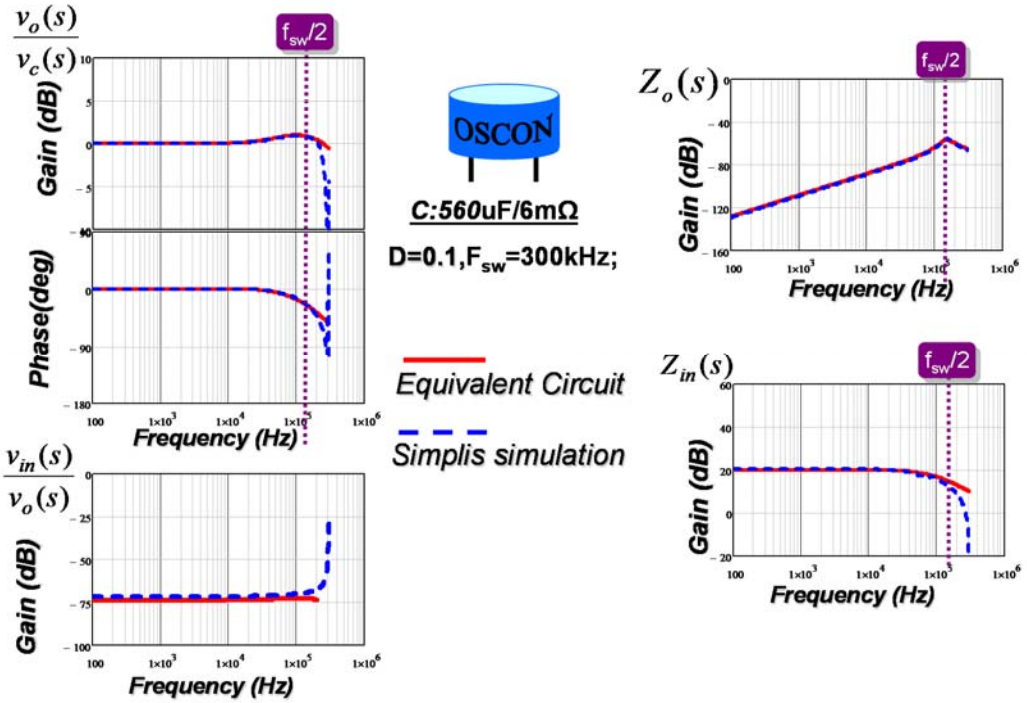


Figure 3. 16. Simplis verification for single-phase constant on-time V^2 control with OSCON capacitors (6mΩ/560uF).

Figure 3. 17 shows verification for two-phase constant on-time V^2 control with Ceramic capacitors (220uF/3mΩ). It is clear that for the control-to output transfer function, the proposed equivalent circuit model can predict the peaking of double pole at ½ f_{sw} very well, the output impedance, input impedance and audio susceptibility also agree with simulation results up to f_{sw}.

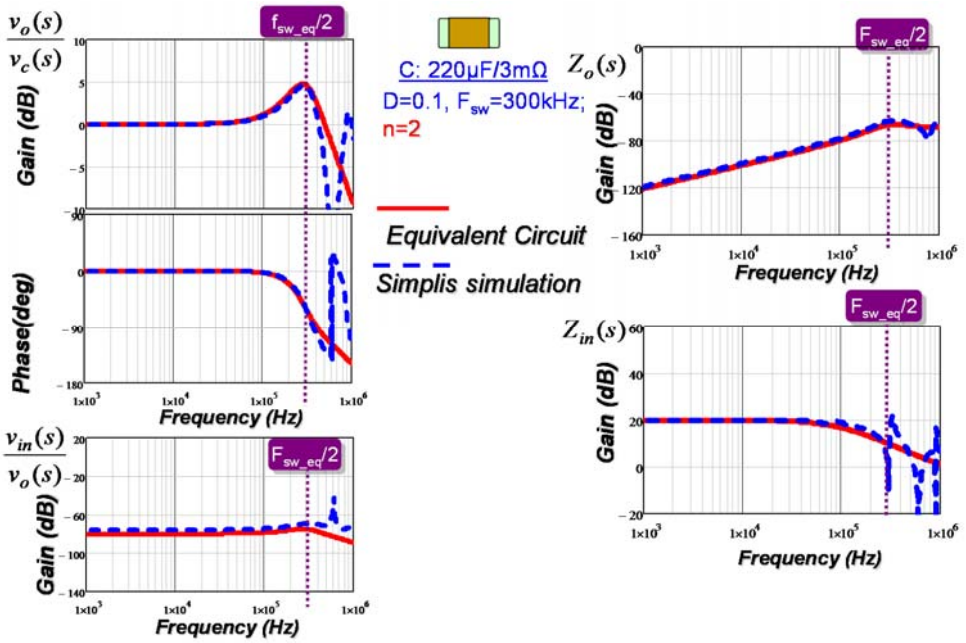
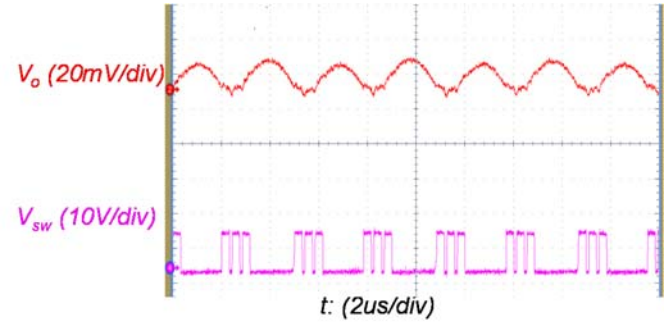
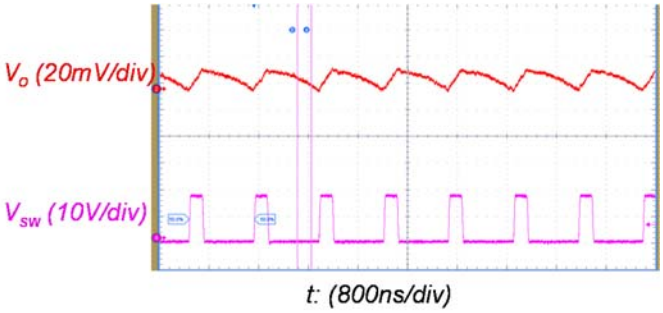


Figure 3. 17. Simplis verification for two-phase constant on-time V^2 control with ceramic capacitors (220uF/3mΩ).

Figure 3. 18 shows experimental waveform based on LM34919 demo-board with the following parameters: F_{sw}=900kHz; V_{in}=15V; D=0.22; V_o=3.3V; L_s=10uH; R_o=10Ω. According to the prediction from equivalent circuit model, for traditional ceramic capacitors (10uF/5mΩ), damping of the double pole caused by capacitor voltage loop is negative, instability is observed, as shown in Figure 3. 18(a). With controlled ESR ceramic capacitors CERD1JX5R0J106M (10uF/50mΩ), the double pole is well-damped and the circuit is stable in Figure 3. 18(b). From Figure 3. 19, the prediction from equivalent circuit model can match with experimental data up to ½ f_{sw}. Figure 3. 20 shows verification of audio susceptibility transfer function. Audio susceptibility performance for constant on-time V^2 control is very good as the gain is very low (around -60dB) in the whole frequency region up to ½ f_{sw}. Compared with measurement data, the prediction from the equivalent circuit model is good.



(a)



(b)

Figure 3. 18. Experimental waveform for constant on-time V^2 control (a) traditional ceramic capacitors (10uF/5mΩ) (b) controlled ESR ceramic capacitors (10uF/50mΩ)

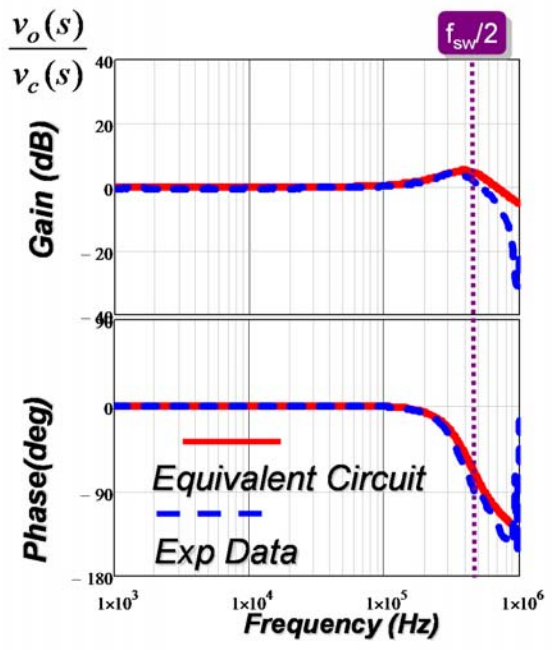


Figure 3. 19. Experimental verification of control-to-output transfer function with controlled ESR ceramic capacitors CERD1JX5R0J106M (10uF/50mΩ).

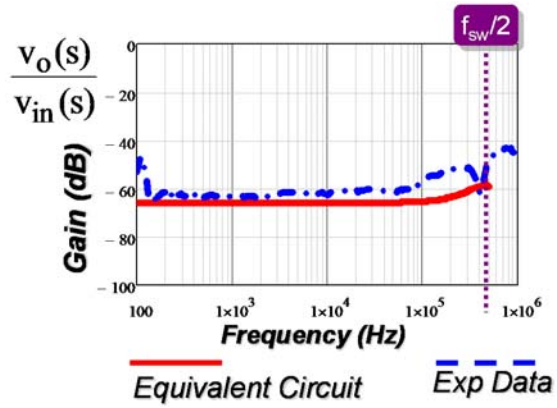


Figure 3. 20. Experimental verification of audio susceptibility transfer function with controlled ESR ceramic capacitors CERD1JX5R0J106M (10uF/50mΩ).

3.8 Summary

This chapter proposed a unified equivalent circuit model of V^2 control, the model represents capacitor voltage sideband effects with a R_{e2}-L_{e2} branch, which represents the double pole by resonating with output capacitor. The equivalent circuit model is a complete model and can be used to examine all the transfer functions. For the first time, an equivalent circuit model which can predict instability for V^2 control is proposed. The model is also extended to enhanced V^2 control, multi-phase V^2 control and V^2 control with different modulation schemes. Simulation and experimental results verify the accuracy of the equivalent circuit model for all transfer functions. Based on the unified equivalent circuit model, the design consideration and performance comparison of V^2 control will be discussed in chapter 4.

Chapter 4. Optimal Design and Performance Comparison of V^2 Control

4.1 Introduction

In previous chapter, a unified equivalent circuit model is proposed. This chapter investigates design considerations and performance comparison of V^2 control. For VR application, design guideline is proposed for enhanced constant on-time V^2 control. For traditional point-of-load application with ceramic capacitors, three methods to solve the instability issue are presented: controlled ESR ceramic capacitors, enhanced V^2 control with high pass filter and V^2 control with capacitor current. The limitation and advantage of each method is analyzed and design guidelines are proposed. For constant frequency V^2 peak control, explicit stability criterion is derived. The small-signal model with ramp compensations is presented and optimal design guidelines from dynamic performance point of view are provided. For the first time, it is found the external ramp is good enough to get a well-damped performance when current feedback strength is strong (for example, when employing OSCON capacitors). However, current ramp is necessary to achieve good dynamic performance when current feedback strength is weak (for example, when employing Ceramic capacitors). The small-signal models are compared between constant on-time V^2 control and constant frequency V^2 peak control, concluding that constant on-time modulation is much better from dynamic performance point of view. The analyses are verified by Simplis simulation and experimental results. The major content of this chapter is published in [D51][D52][D53].

4.2 Optimal Design for Constant On-time V^2 Control

4.2.1 Enhanced constant on-time V^2 control for VR application

Several commercial products use multi-phase constant on-time enhanced V^2 control for VR application [D54][D55]. This section discuss the design guideline based on equivalent circuit model. A two-phase enhanced constant on-time V^2 control diagram is shown in Figure 4. 1 while the equivalent circuit model to derive output impedance for small duty cycle application is shown in Figure 4. 2.

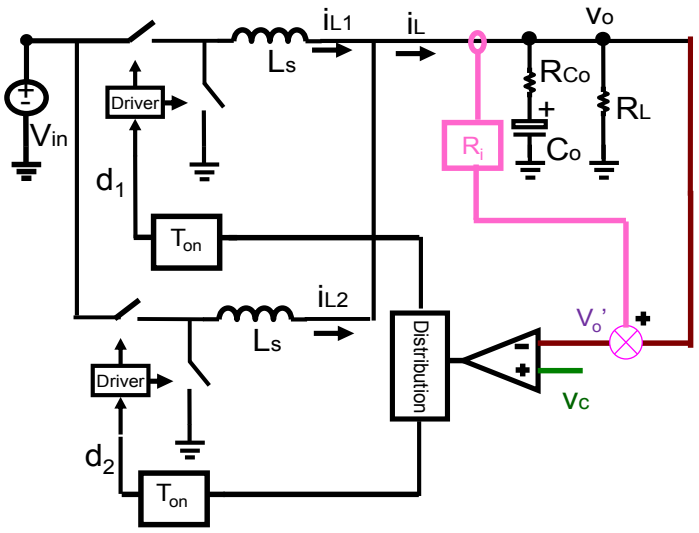


Figure 4. 1. Diagram of n-phase enhanced constant on-time V^2 control

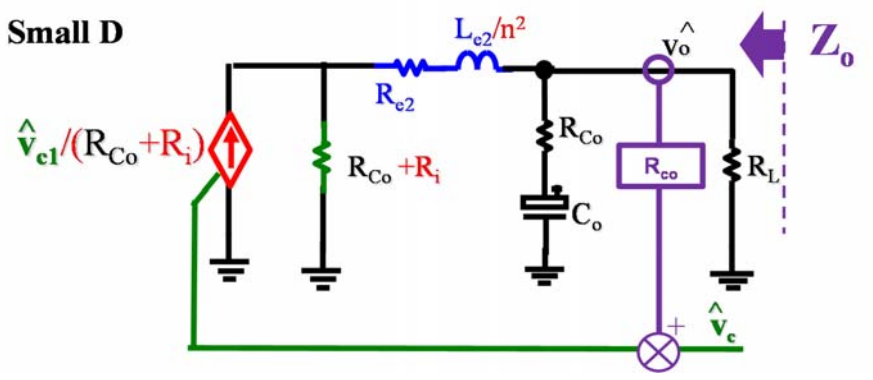


Figure 4. 2. Equivalent circuit model for output impedance with small D

The output impedance can be derived and is shown as follows:

$$Z_o(s) \approx R_i \frac{(R_{Co}C_o s + 1)}{(1 + \frac{s}{Q_{3\_n}\omega_{2\_n}} + \frac{s^2}{\omega_{2\_n}^2})}$$
$$\omega_{2\_n} = n\frac{\pi}{T_{sw}}, Q_3' = \frac{T_{sw}/n}{\pi \cdot \left((R_{Co} + R_i) \cdot C_o - \frac{T_{on}}{2} \right)} \quad (4.1)$$

The low-frequency output impedance is determined by the current sensing gain R_i, the design guideline of R_i and output capacitor is shown as follows:

Step 1: Design current sensing gain R_i according to load line requirement R_{LL}

$$R_i = R_{LL} \quad (4.2)$$

Step 2: Choose output capacitor number to control Q_3 (for example, control Q_3=1) of double pole to avoid peaking of the output impedance at high frequency.

Using a two-phase enhanced constant on-time V^2 control with the following parameters as an example: D=0.1, f_{sw}=300kHz, n=2; ceramic capacitors (100uF/1.4mΩ); load line requirement R_{LL}=1mΩ. According the step 1, R_i should be 1mΩ. The number of ceramic capacitors are selected from step 2. As shown in Figure 4. 3, 7 ceramic capacitors are required from output impedance.

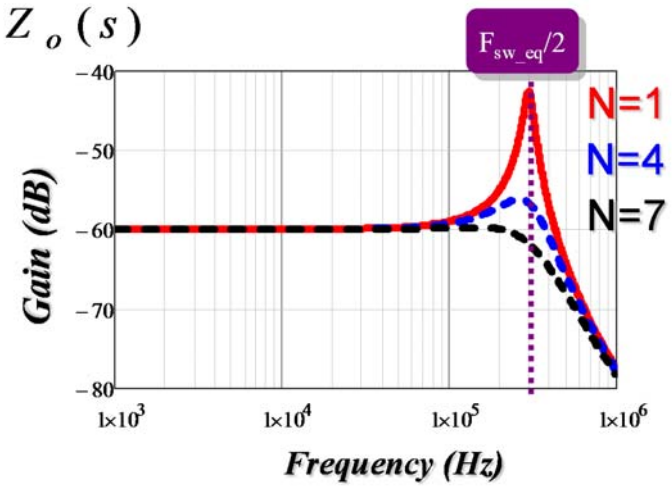


Figure 4. 3. Selection of number of capacitors to meet output impedance requirement

4.2.2 Controlled ESR ceramic capacitor solution for portable electronics applications

As shown in Figure 3. 6, for capacitors having large RC time constants, such as OSCON capacitors, the dynamic performance is good, however, the sub-harmonic oscillation occurs when traditional ceramic capacitors are used. On the other hand, ceramic capacitors are preferred in portable electronics applications due to the small size. To solve the instability problem, one simple solution is to employ controlled ESR ceramic capacitors [D56]: TDK Corporation recently provides options to customize ESR for ceramic capacitors. With this technology, the ESR of the ceramic capacitors can be customized without increasing the ESL value. For V^2 application, (3. 9) can be used for customization of ESR so that the double pole at ½ f_{sw} is well damped: for example, ESR can be customized such that Q_3=1. As shown in Figure 4. 4, with traditional ceramic capacitors for 10uF/3mΩ, the peaking at ½ f_{sw} is large. With the ESR customized to 200mΩ, the peaking is eliminated as Q_3 is around 1. With customized ESR products, conceptually the ripple voltage across ESR overwhelmed the ripple voltage across pure capacitance, which is similar as OSCON capacitor case. The disadvantage of this controlled ESR approach is that the output voltage ripple is increased due to increased ESR, therefore more capacitors need to be paralleled to meet the output voltage ripple requirement. Besides, only a few products are available with limited capacitance value, such as 1uF and 10uF. For large capacitance value such as 100uF, up to now, no customized ESR ceramic capacitors are available. This limitation prevents controlled ESR capacitors as a solution in applications where large capacitance is required.

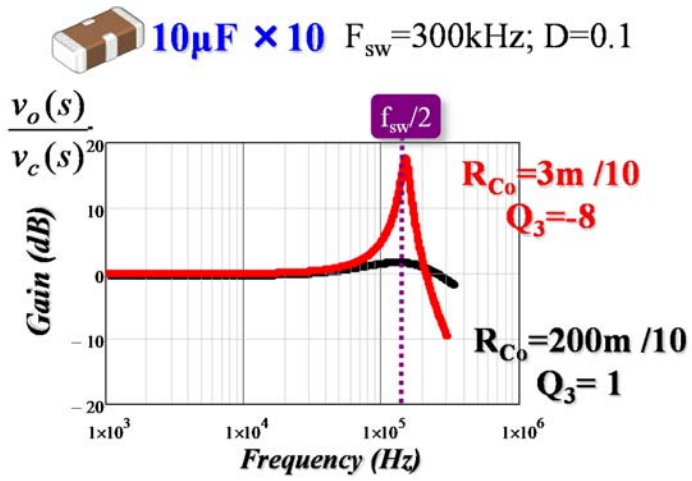


Figure 4. 4. Customization of ESR for ceramic capacitors to improve dynamic performance

4.2.3 Enhanced V^2 control with high pass filter for POL application

The second method is to enhance current feedback by adding inductor current ramp, as shown in Figure 3. 9. Traditional inductor current sensing methods can be used and this method is widely used in industry products [D3][D4]. The control to-output voltage transfer function for enhanced constant on-time V^2 control is shown as follows:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_3^{'}\omega_2}+\frac{s^2}{\omega_2^2})} \tag{4. 3}$$

$$Q_3^{'} = \frac{T_{sw}}{\pi\left((R_{Co}+R_i)C_o - T_{on}/2\right)}, \omega_2 = \frac{\pi}{T_{sw}}$$

The principle for design of R_i is similar as controlled ESR ceramic capacitor case: design R_i to control the quality factor of double at half of switching frequency. As an example shown in Figure 4. 6, for traditional ceramic capacitor (8*100uF/1.4mΩ), a flat gain can be achieved by adding R_i=1.4 mΩ.

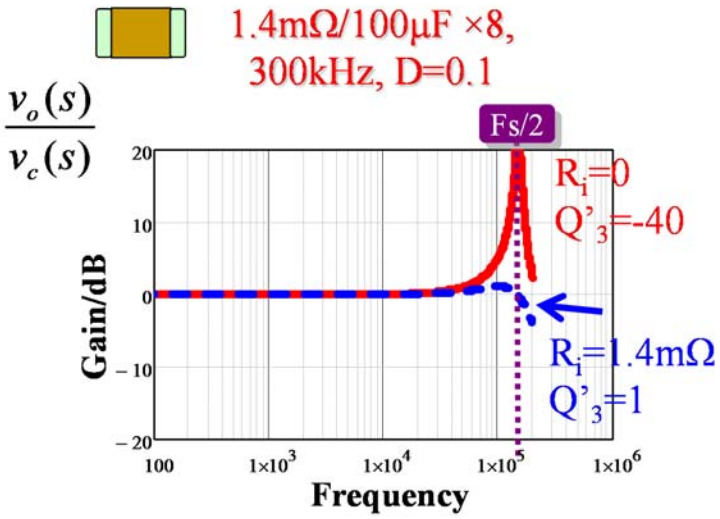


Figure 4. 5. Design of R_i to control quality factor of the double pole at ½ f_{sw}

However, by adding inductor current information, the output impedance is modified due to DC information of inductor current. In time-domain, adaptive voltage positioning is achieved, as shown in Figure 4. 7.

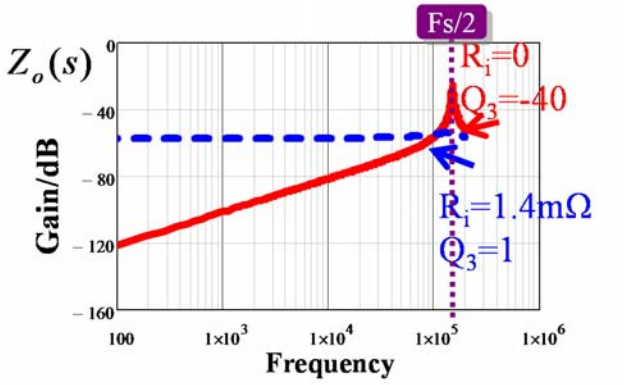


Figure 4. 6. Effect of R_i on output impedance

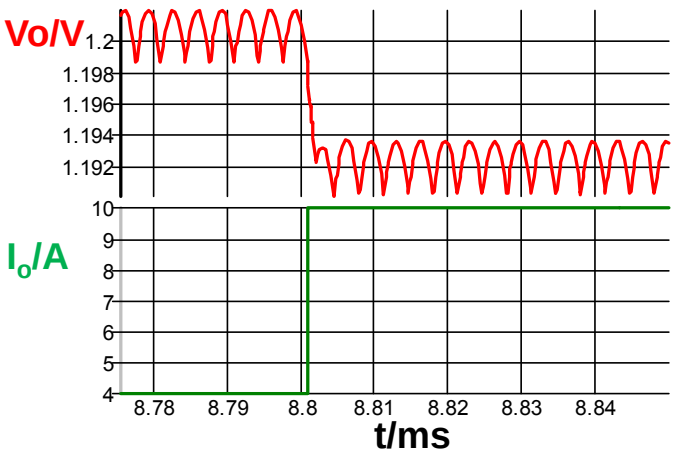


Figure 4. 7. Adaptive voltage positioning behavior due to injected DC inductor current

In many point-of-load applications, output voltage should be well regulated and adaptive voltage positioning is undesired. To eliminate steady-state droop voltage, a high pass filter is inserted after current sensing in commercial products [D3][D4], as shown in Figure 4. 8.

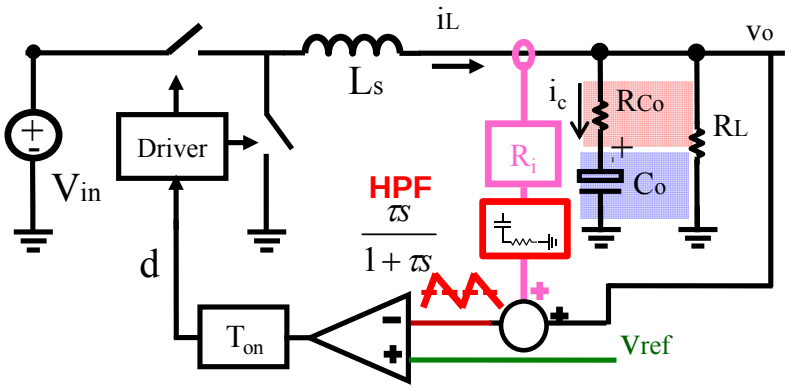


Figure 4. 8. Addition of high pass filter to eliminate DC current information

Up to now, there is no small-signal model provided for enhanced constant on-time V^2 control with high pass filter case. The proposed equivalent circuit model can be easily extended to this case with similar modeling strategy: the sensed current information after high pass filter is manipulated as the subtraction of two signals: one is direct current feedback and the other is the sensed current information flowing through a low-pass filter, as shown in Figure 4. 9.

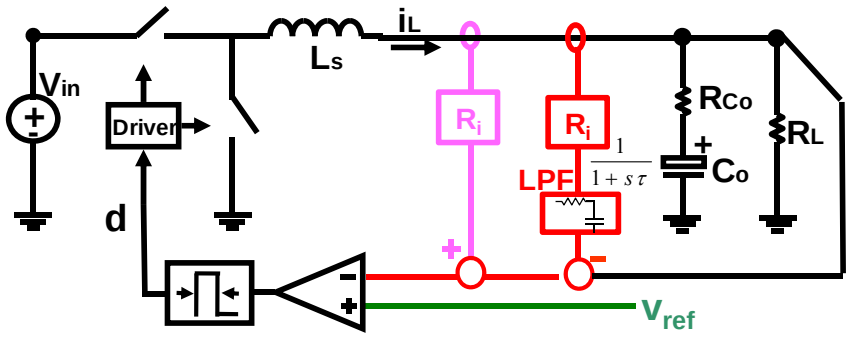


Figure 4. 9. Modeling strategy: separating high pass filter into two paths

As the purpose of high pass filter is to eliminate the DC information of inductor current while keeping its switching frequency information, the pole position of the filter is designed to be much lower than switching frequency, as shown in follows:

$$\tau >> \frac{T_{sw}}{2\pi} \tag{4. 4}$$

As a result, all the switching frequency and sideband component is in the pink path, while the red path only has modulation frequency component. Therefore, equivalent circuit model with high pass filter can be derived as follows:

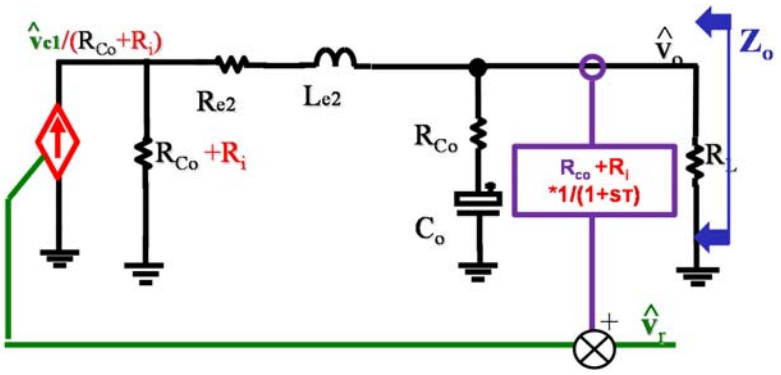


Figure 4. 10. Equivalent circuit model for output impedance with small D

The output impedance can be obtained solving the above equivalent circuit:

$$Z_o(s) \approx R_i(\frac{\varpi}{1+\varpi})\frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_3^{'}\omega_2}+\frac{s^2}{\omega_2^2})}$$
$$Q_3^{'} = \frac{T_{sw}}{\pi \cdot \left((R_{Co}+R_i)\cdot C_o - \frac{T_{on}}{2}\right)} \quad (4.5)$$

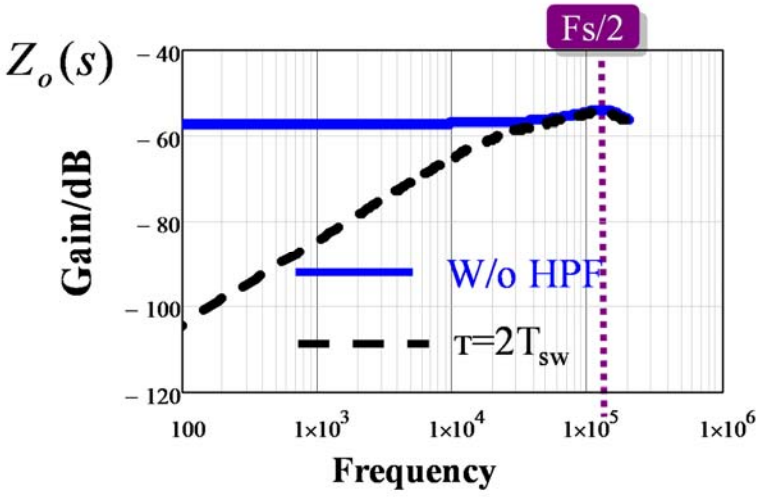


Figure 4. 11. Improvement of output impedance due to high pass filter

As shown in Figure 4. 11, the high pass filter reduces the low-frequency output impedance as expected. The simulation result will be provided in section 4.2.6 to prove the accuracy of the equivalent circuit model.

Another point worthwhile to be mentioned is that accurate current sensing is assumed in above model derivation. However, DCR mismatch effect may affect the accuracy of the current sensing in reality, Nonetheless, the mismatch effect can be also easily included to modify the equivalent circuit model, using similar strategy as high pass filter case.

4.2.4 V^2 control with capacitor current for POL application

The third method reported in literature is to enhance current feedback by adding capacitor current [D21][D29], as shown in . To sense capacitor current, a simple lossless capacitor current sensing method

has been proposed in [D21]. Alternatively, a non-invasive capacitor current sensing method which considers the ESL effect has been proposed in [D29].

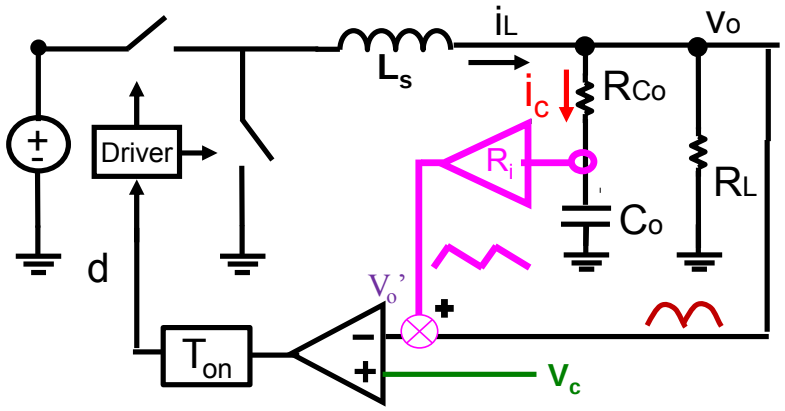


Figure 4. 12. Diagram of constant on-time V^2 control with capacitor current ramp compensation.

Following similar strategy, the equivalent circuit model with capacitor current ramp with small duty cycle application can be derived as follows:

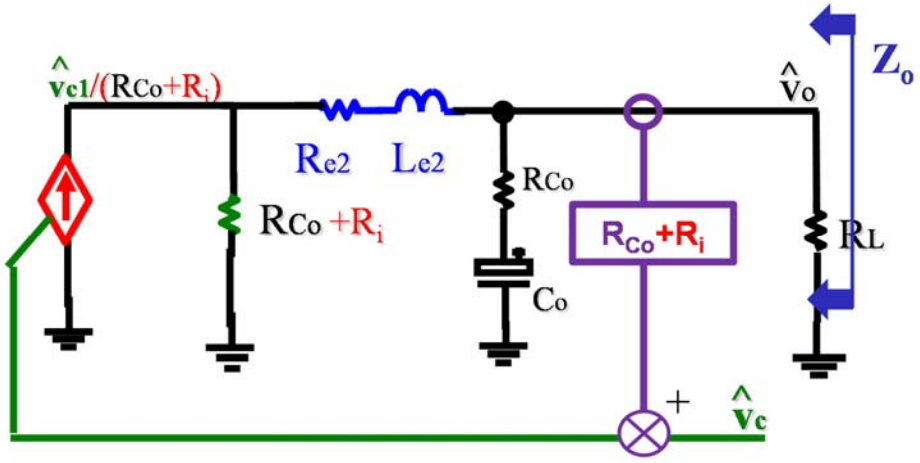


Figure 4. 13. Equivalent circuit model for output impedance with small D

Compared with Figure 3. 9, the only difference between inductor current ramp and capacitor current ramp is the different load current feedback gain: for inductor current ramp case, it is R_{Co} while for capacitor current ramp case, it is the sum of R_{Co} and R_i. The control-to-output transfer functions of the two cases are almost the same, as the role of load current feedback is negligible in both cases. Therefore, design of R_i is

the same as inductor current ramp case: design R_i to control the quality factor of double pole at ½ f_{sw} shown in (4. 3).

The difference between the two methods lie in the fact that the output impedances are different due to different load current feedback gains. The output impedance with capacitor current ramp can be derived as follows:

$$Z_o \approx \frac{T_{on}}{2}(R_{Co} + R_i) \cdot s \frac{1 + R_{Co} C_o s}{1 + \frac{s}{Q_3 \omega_2} + \frac{s^2}{\omega_2^2}} \tag{4. 6}$$

As shown in Figure 4. 14, while the output impedance is determined by R_i for inductor current ramp, by adding capacitor current ramp, the output impedance is still very low which means it can still achieve very fast transient response. For practical application, the influence on accuracy of sensed current due to the parasitic parameters (such as ESL effect of the capacitor, ESL due to trace) needs to be taken into consideration. That is one reason why it is not as popular as using inductor current ramp in commercial products.

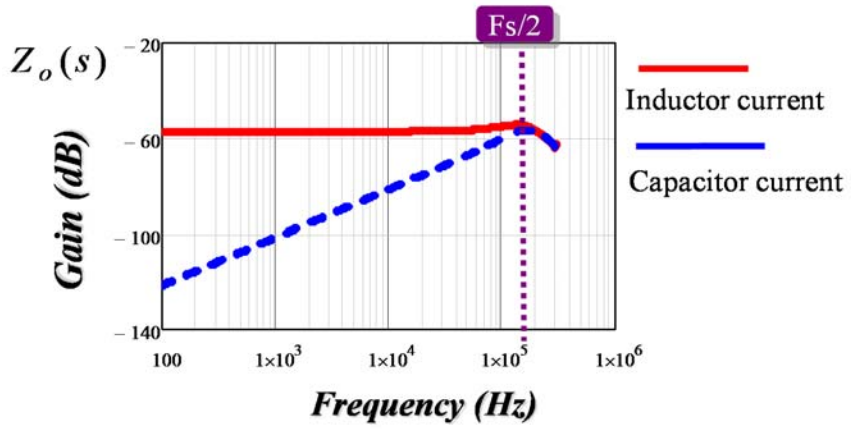


Figure 4. 14. Comparison of V^2 control using inductor current and capacitor current

4.2.5 Capacitor parameter tolerance consideration

In real application, the effect of capacitor parameter tolerance needs to be analyzed and considered. ormance sacrifice a little bit.

Table 4. 1 shows the capacitor parameter (ESR and capacitance) tolerance due to manufacture, DC bias, temperature and aging effect. In practical design, worst case analysis should be used to ensure the dynamic performance throughout the whole life cycle of output capacitors. As an example, for ceramic capacitor (1.4mΩ/100uF), the time constant tolerance range is (-35% to +50%), therefore, the design should control the quality factor of double pole for -35% case. Under this circumstance, the bode plots of control to output voltage transfer function for normal case and best case (+50%) is shown in Figure 4. 15. Due to worst case design strategy, the dynamic performance sacrifice a little bit.

Table 4. 1 Capacitor parameter tolerance for OSCN, SP and Ceramic capacitors

Parameter tolerance	OSCON:6mΩ/560uF (4SEPC560MW, SANYO)	SP: 6mΩ/330uF (EEFSX0E331X, Panasonic)	Ceramic:1.4mΩ/100uF (C3216X5R0G107M, TDK)
C: f(Temp)	-5% / +10%	-5%/+5%	-15% / +15%
C:f(Manufacture)	-20% / +20%	-20% / +20%	-20% / +20%
C: f(aging)	-20% / +20%	-10%/+10%	-5% / 0%
C: f(DC Bias)	No change	No change	-10%
ESR: f(Temp)	No change	No change	Not available
ESR: f(aging)	-0%/+50%	No change	Not available
C (total)	-45% / +50%	-35%/+35%	-50% / +35%
ESR (total)	-0%/+50%	-0%/+0%	-0%/+0%
ESR*C (total)	-45%/+125%	-35%/+35%	-50%/+35%

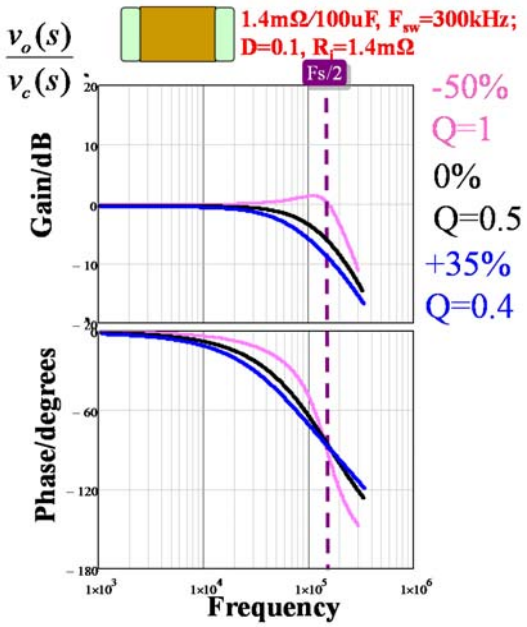


Figure 4. 15. Worst-case design example to include capacitor parameter tolerance effect

4.2.6 Simulation and experimental verification

Figure 4. 16 shows simulation verification for enhanced constant on-time V^2 control with the following parameters: 8 ceramic capacitors (1.4mΩ/100uF), with 0.1 duty cycle and 300kHz switching frequency; R_i=1.4mΩ, time constant of high pass filter $\tau=2T_{sw}$. All four transfer functions, including control to output voltage, input to output voltage, output impedance and input impedance are compared. The proposed model agrees with simulation results very well up to f_{sw} for all transfer functions.

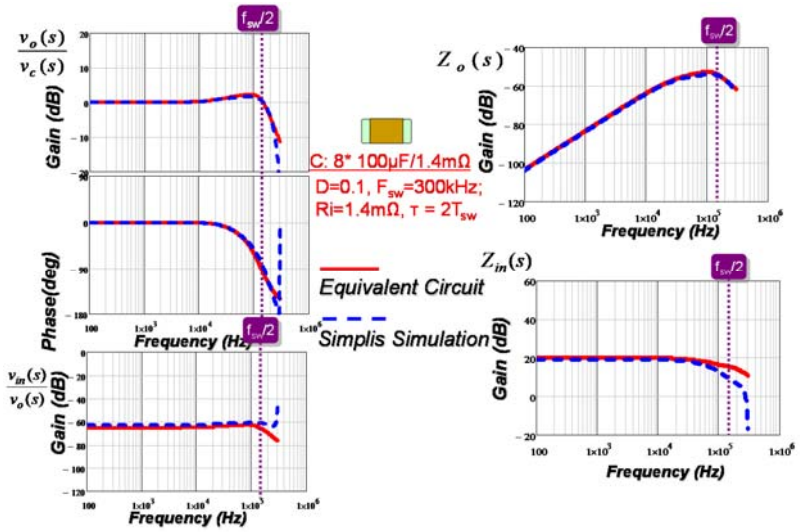


Figure 4. 16. Simulation verification of equivalent circuit model with inductor current ramp and high-pass filter

Figure 4. 17 shows the effects of R_i on load transient performance. Compared with other two arbitrary design, the proposed optimal design strategy provides better transient performance.

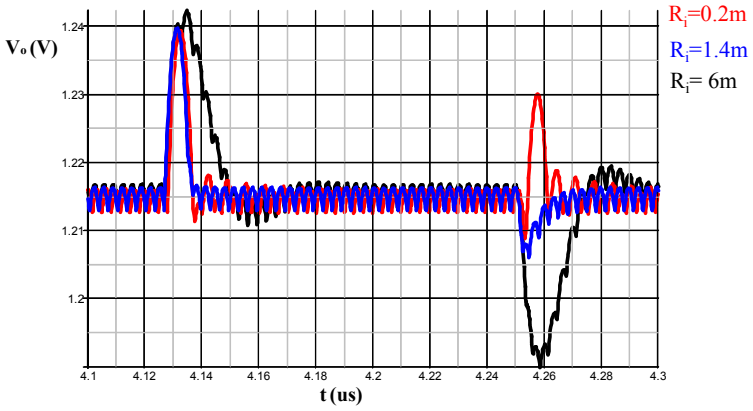
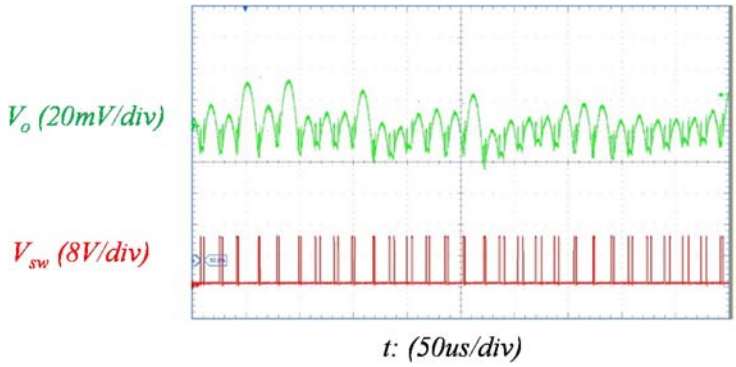


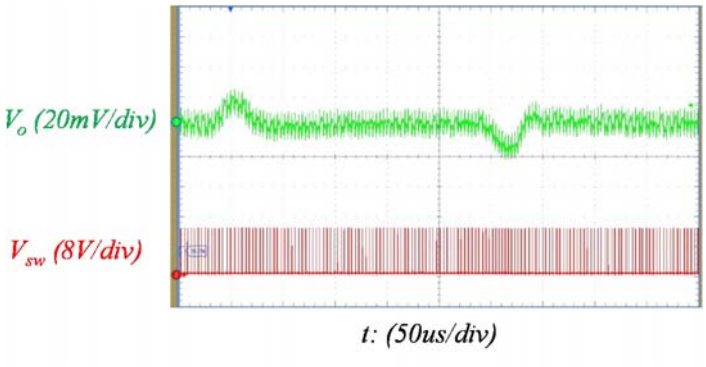
Figure 4. 17. Comparison of load transient performances: (1) with insufficient R_i, (2) with optimized R_i (3) with too large R_i

To verify proposed optimal design guideline, Figure 4. 18 shows load transient experimental waveforms for constant on-time enhanced V^2 control with high-pass filter, based on TPS51513 evaluation board with the following parameters: F_{sw}=300kHz; V_{in}=12V; V_o=1.1V; D=0.1; L_s=0.47uH; 6 Ceramic Caps (100uF/2m Ω); Load transient: 3A to 8A with 2kHz frequency and 50% duty cycle. In Figure 4. 18 (a), current sensing gain R_i is insufficient and Q_3' shown in (4. 3) is 4, the dynamic performance is very bad.

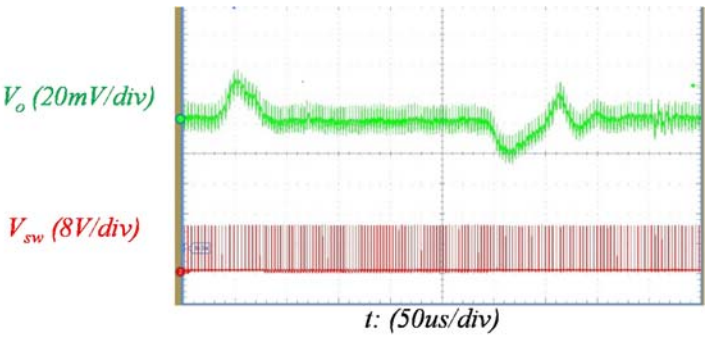
In Figure 4. 18 (b), current sensing gain R_i is optimized to control Q_3'around 1 and transient performance is good. In Figure 4. 18 (c), R_i is too large, the settling time, the overshoot and undershoot voltage all increase. The proposed optimal design to control quality factor around 1 provides best transient performance among the three.



(a)



(b)



(c)

Figure 4. 18. Comparison of load transient experimental waveforms: (a) with insufficient R_i (R_i=0.4m, Q_3'=4) (b) with optimized R_i (R_i=2m, Q_3'=1) (c) with too large R_i (R_i=10m, Q_3'=0.2)

4.3 Optimal Design for Constant Frequency V^2 Peak Control

For constant frequency V^2 peak control, based on equivalent circuit model shown in Figure 3. 15, the small-signal control-to-output transfer function is shown as follows:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2})} \tag{4. 7}$$

$$Q_{e1}=\frac{2}{\pi}\frac{1}{\alpha+\sqrt{\alpha^2+(4D-2)\alpha+(1-D)^2+D^2}}, Q_{e2}=\frac{2}{\pi}\frac{1}{\alpha-\sqrt{\alpha^2+(4D-2)\alpha+(1-D)^2+D^2}}$$

α is called feedback strength and is defined as follows:

$$\alpha = \frac{R_{Co}C_o}{T_{sw}} = \frac{1}{2\pi}\frac{f_{sw}}{f_{esr}} \tag{4. 8}$$

α is related with the ratio of the ESR ripple magnitude over the capacitor voltage ripple magnitude, as shown in follows:

$$\frac{\Delta v_{ESR}}{\Delta v_{Co}} = \frac{R_{Co}\Delta i_L}{\frac{1}{8C_o}\Delta i_L T_{sw}} = \frac{8R_{Co}C_o}{T_{sw}} = 8\alpha \tag{4. 9}$$

It can be seen that α represents the relative strength of the current feedback: The larger α value, the larger the ESR ripple when compared with the capacitor voltage ripple. From a design point of view, α is the ratio of switching frequency over ESR zero frequency.

For the typical capacitor, the values of α are listed and shown in Table 4. 2.

Table 4. 2 Values of current strength α with various capacitors

Cap Type	Cap Parameters	F_{sw}(Hz)	F_{esr}/F_{sw}	α	$\Delta V_{esr}/\Delta V_{co}$
OSCON	6mΩ/560uF	300k	≈ 1/6	≈ 1	≈ 8
SP	6mΩ/330uF	300k	≈ 1/4	≈0.6	≈ 5
Ceramic	1.4mΩ/100uF	300k	≈ 4	≈0.04	≈0.3
		4.2M	≈ 1/4	≈0.6	≈ 5

Table 4. 2 shows that the current feedback strength is relatively large when using the OSCON and SP capacitors with a typical 300 kHz switching frequency while it is very small for ceramic capacitors. It also shows that the switching frequency needs to be increased to 4.2 MHz for ceramic caps so that it has the same current feedback strength as the SP caps with a 300 kHz switching frequency. The importance of α is shown in the following analysis of the small-signal model.

4.3.1 Small-signal analysis of control to output voltage transfer function

For small duty cycle application, with simple mathematical manipulation, Q_{e1} and Q_{e2} in (4. 7) can be approximated and rewritten as follows:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2})} \qquad (4.\ 10)$$

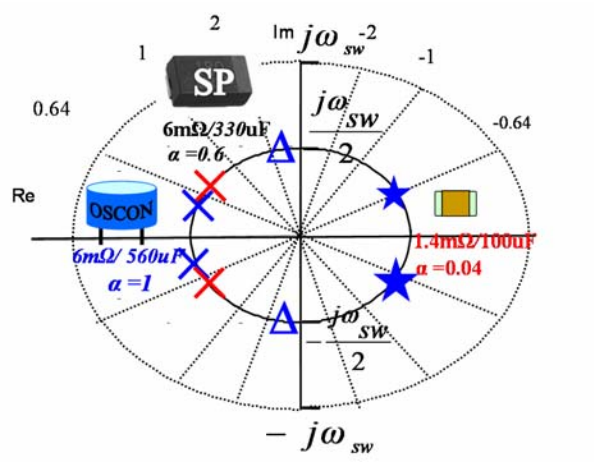
$$Q_{e1} \approx \frac{1}{\pi}\frac{1}{D'-0.5}, Q_{e2} \approx \frac{1}{\pi}\frac{1}{\alpha-0.5}$$

By closing the current loop, one pair of double pole, which is located at half of switching frequency shows up. The quality factor Q_{e1} is related to duty cycle, as in the peak current mode case. Note that the expression Q_{e1} shown in (4. 10) is the same as the expression of Q of the double pole in peak current mode control shown in [C31][C32].

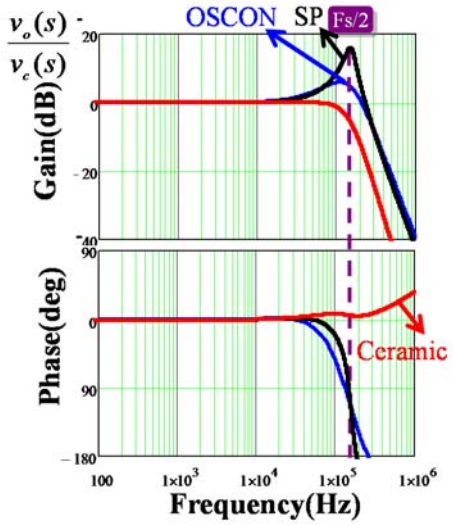
By closing the capacitor voltage feedback loop, another pair of double pole, which is also located at half of switching frequency shows up and the quality factor Q_{e2} is related to the current feedback strength *α,* as shown in (4. 10).

The effect of the current feedback strength *α* can be clearly seen in (4. 10), as the quality factor Q_{e2} is related with *α.* For illustration purpose, with different types of output capacitors, the comparisons of pole zero maps and bode plots for control-to-output voltage transfer function under D=0.1 and f_{sw}=300kHz are shown in Figure 4. 19. With smaller *α,* the capacitor voltage feedback is stronger which means the phase

delay effect is more severe, and the circuit is more unstable. Comparing SP capacitor with OSCON capacitor, the second pair of double poles has a larger quality factor and the peaking is larger. For ceramic capacitor, since α is 0.04 with a 300 kHz switching frequency which is smaller than 0.5, the double pole locates on right-half-plane, which means that the circuit is unstable.



(a)



(b)

Figure 4. 19. Comparisons between OSCON, SP and Ceramic capacitors with D=0.1 and f_{sw}=300kHz (a) Pole-zero maps (b) Control-to-output voltage transfer function.

Duty cycle is related with the sample-and-hold effect in peak current mode control [C31]. As peak current control loop still exists in constant frequency V^2 peak control, duty cycle also impacts the control-to-output voltage transfer function, as it affects Q_{e1} and Q_{e2} shown in (4. 7). To illustrate this point, the bode plots of control-to-output voltage transfer function for OSCON caps with f_{sw}=300 kHz and different duty cycles are shown in Figure 4. 20. When D is larger, the peaking at half of switching frequency is larger, which indicates a smaller stability margin. The phenomenon is the same with respect to peak current mode control: when D is larger, the sample-and-hold effect of the current loop is stronger and the stability is worse. However, the difference is that in constant frequency V^2 peak control, the additional capacitor voltage phase delay affects the stability and instability may happen before D=0.5. As shown in Figure 4. 20, when D=0.4, the phase plot goes up, which indicates that there is a right-half-plane double pole and the system is already unstable.

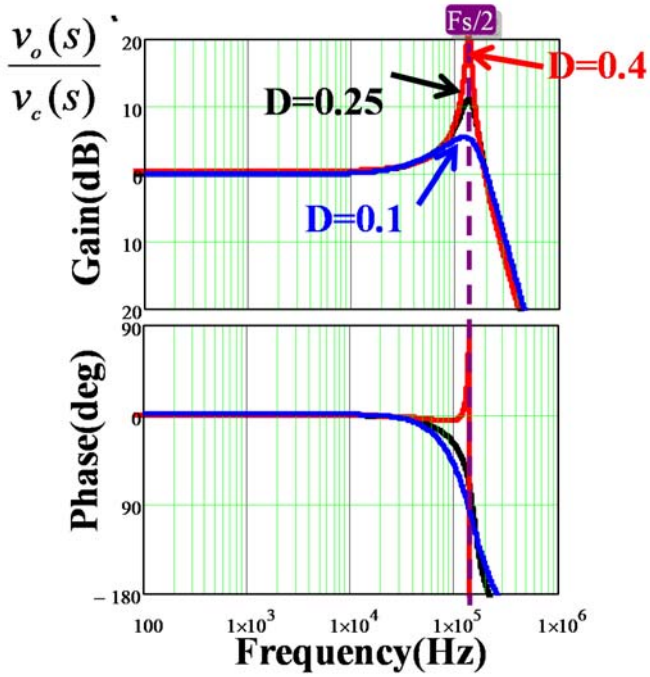


Figure 4. 20. Comparison of bode plots of control-to-output voltage transfer function for OSCON capacitors with 300kHz switching frequency and different duty cycles

4.3.2 Stability criterion and design consideration

As shown above, when D is small, the two kinds of sidebands can be decoupled, inductor current sidebands cause one pair of double pole and capacitor voltage sidebands cause another pair of double pole, as shown in (4. 10). When D is becoming larger, the two kinds of sidebands are coupled and interacting with each other, as shown in (4. 7). In general, the criterion for stable operation is that all the poles are located at the left-half-plane, or equivalently the quality factors related with the double poles are both positive. The stability criterion can then be solved from (4. 7) as shown in the following equation:

$$D \le \frac{1}{2} - \frac{1}{2}\frac{1}{2\alpha + \sqrt{4\alpha^2 - 1}}, \text{ where } \alpha = \frac{R_{Co}C_o}{T_{sw}} = \frac{1}{2\pi}\frac{f_{sw}}{f_{esr}} \qquad (4.\ 11)$$

The stability is not only related to duty cycle, as in the peak current mode control, but also to the current feedback strength α, which also reflects the phenomenon that the phase delay of capacitor voltage plays an important role in the constant frequency V^2 peak control.

Equation (4. 11) can be represented as Figure 4. 21, which shows the stability criterion with respect to duty cycle and current feedback strength α. As an example, at 300 kHz, for the OSCON cap, $\alpha \approx 1$, D should be smaller than 0.37 shown as the blue point, while for the SP cap, D should be smaller than 0.23, which is the black point. For the ceramic cap, it is unstable for any D since $\alpha < 0.5$. The stability criterion shown in (4. 11) is consistent with peak current mode control case: When α is infinite, the stability criterion reduces to $D \le 1/2$, which is well-known stability criterion for peak current mode control. When α is finite, the stability region of constant frequency V^2 peak control is smaller due to the effect of the capacitor voltage feedback.

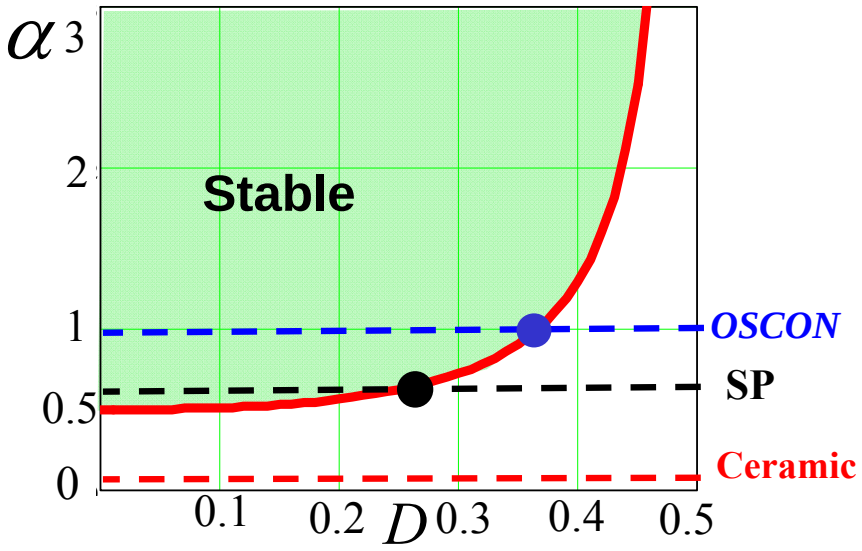


Figure 4. 21. Stability criterion of constant frequency V^2 peak control with F_{sw}=300kHz.

Given certain type of capacitor, α is only related to switching frequency. (4. 11) can be rewritten as follows:

$$F_{sw} \geq \frac{1}{R_{Co}C_o}\left(\frac{1}{2}+\frac{D^2}{1-2D}\right) \qquad (4.\ 12)$$

Table 4. 3 shows the switching frequency requirement for different types of capacitors and different duty cycles. For design purpose, design the converter to avoid the critical stability is not enough. A certain stability margin should be obtained. The same concept shown in peak current mode control can be adopted here in constant frequency V^2 peak control: control the quality factor of double poles. For example, choose Q_{e2} around 1 to gain enough margin. Figure 4. 22 shows the relations between different Q_{e2} values and parameters of duty cycle and current feedback strength α. To control Q_{e2} around 1, a larger α is required for a given duty cycle, for example, when D=0.1, for critical stability, α is around 0.5 while α needs to be increased to around 1.3 to design Q_{e2} around 1. As for OSCON capacitor, the switching frequency should be around 400kHz to control Q_{e2} around 1, compared with 150kHz for critical stability.

Table 4. 3: Switching frequency requirements with different types of caps and duty cycles

Switching Freq. Requirement			α Requirement	Duty cycle
Ceramic 1.4mΩ/100uF	SP 6mΩ/*330*uF	OSCON 6mΩ/*560*uF		
10.8M	*720k*	*430k*	α≥1.3	D=0.4
3.5M	*250k*	*150k*	α≥0.5	D=0.1

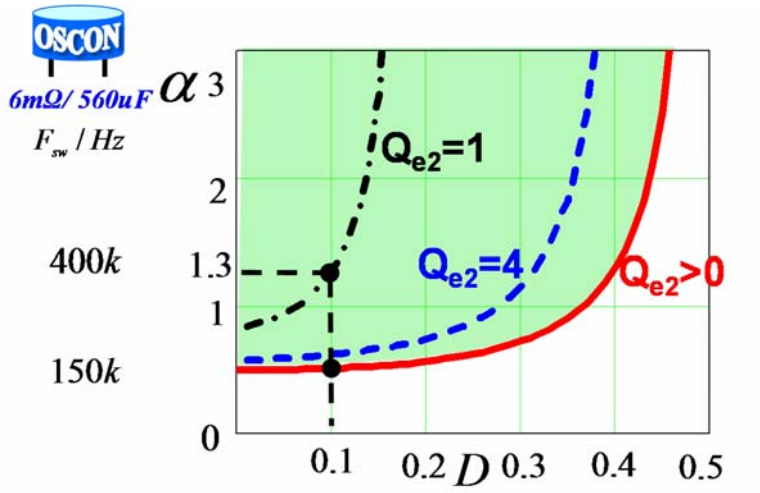


Figure 4. 22. Stability margin control by controlling Q_{e2}.

One of the benefits of V^2 control is fast transient response. Therefore, it is meaningful to investigate the output impedance. The transfer function of the output impedance can be also derived from the equivalent circuit model and shown in (4. 13), in which Q_{e1} and Q_{e2} are shown in (4. 7).

$$Z_o(s) \approx \frac{-R_{Co}T_{sw}\left(\frac{1}{2}-D\right)*s*(R_{Co}C_o s+1)}{(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2})} \quad (4.\ 13)$$

The output impedance for OSCON Cap and SP Cap with 0.1 duty cycle and 300kHz switching frequency is shown as Figure 4. 23. The important aspects of output impedance are listed as follows:

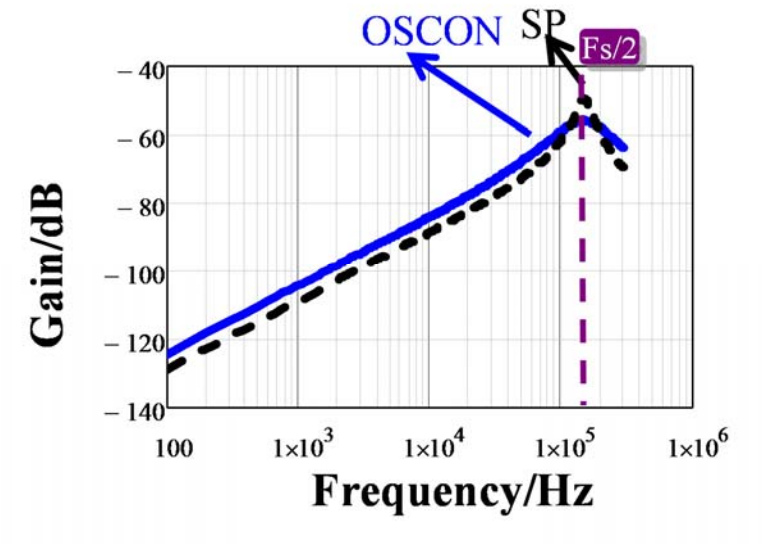


Figure 4. 23.Output impedance for OSCON capacitor and SP capcitor with D=0.1 and f_{sw}=300kHz.

(1) For constant frequency V^2 peak control, the output impedance is very low during the entire frequency region up to half of switching frequency, which indicates fast transient response and is also seen in other types of V^2 control such as constant on-time V^2 control. At steady state, the output impedance is zero and in low frequency range, the output impedance shows the characteristic of an equivalent inductor, the value of the equivalent inductor is related with the modulator and is different between different V^2 control structures. The zero steady state impedance is attributed to the existence of the load current feedback loop, as shown in Section 3.3.3. At half of switching frequency, the double poles caused by current loop sidebands and capacitor voltage sidebands still exist, as all the transfer functions have the same characteristic equations.

(2) Compare the OSCON capacitor with SP capacitor, in low frequency, OSCON Cap has a larger output impedance, as the equivalent inductance is related with R_{Co}. However, SP Cap has a larger peaking around half of switching frequency, as the current feedback strength is smaller and the quality factor of the double pole is larger. Nevertheless, the difference is minor as the output impedance is very low. As long as the circuit has enough stability margin, the output impedance characteristic is very good.

4.3.3 Optimal design of external ramp for OSCON capacitors

External ramp compensation is a well-known solution to eliminate sub-harmonic oscillation in peak current-mode control, and this strategy can be employed to eliminate sub-harmonic oscillation in constant frequency V^2 peak control as well. Figure 4. 24 shows the circuit diagram of constant frequency V^2 peak control with external ramp compensation.

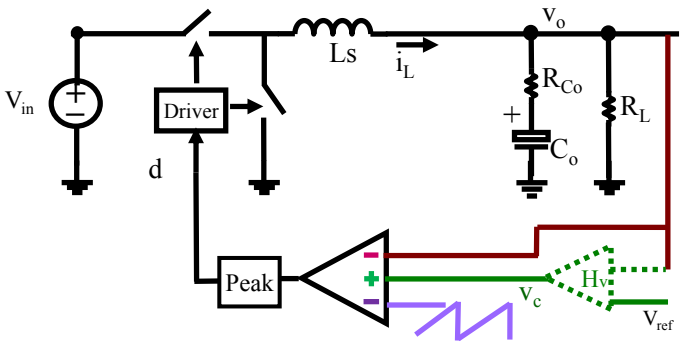


Figure 4. 24. Diagram of constant frequency V^2 peak control with external ramp compensation.

The small-signal control-to-output voltage transfer function is shown as follows [D52]:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{R_{Co}C_o s+1}{\left(1+\frac{s}{Q_{e1}\cdot\omega_2}+\frac{s^2}{\omega_2^{\,2}}\right)\left(1+\frac{s}{Q_{e2}\cdot\omega_2}+\frac{s^2}{\omega_2^{\,2}}\right)}$$

$$Q_{e1}=\frac{2}{\pi}\frac{1}{\alpha+\sqrt{\alpha^2+(4D-2-4D\cdot s_e/s_f)\alpha+(1-D)^2+D^2}} \qquad (4.\ 14)$$

$$Q_{e2}=\frac{2}{\pi}\frac{1}{\alpha-\sqrt{\alpha^2+(4D-2-4D\cdot s_e/s_f)\alpha+(1-D)^2+D^2}},\quad s_f=R_{Co}\frac{V_o}{L_s}$$

In (4. 14), s_e is the external ramp slope while s_f represents the falling slope of ESR ripple voltage. Compared with (4. 7), it can be seen that the external ramp affects quality factors of the double poles. The minimum external ramp for critical stability can be derived by solving (4. 14), which is shown as follows:

$$\frac{s_e}{s_f}>\left(\frac{(1-D)^2+D^2}{4D\alpha}\right)+1-\frac{1}{2D} \qquad (4.\ 15)$$

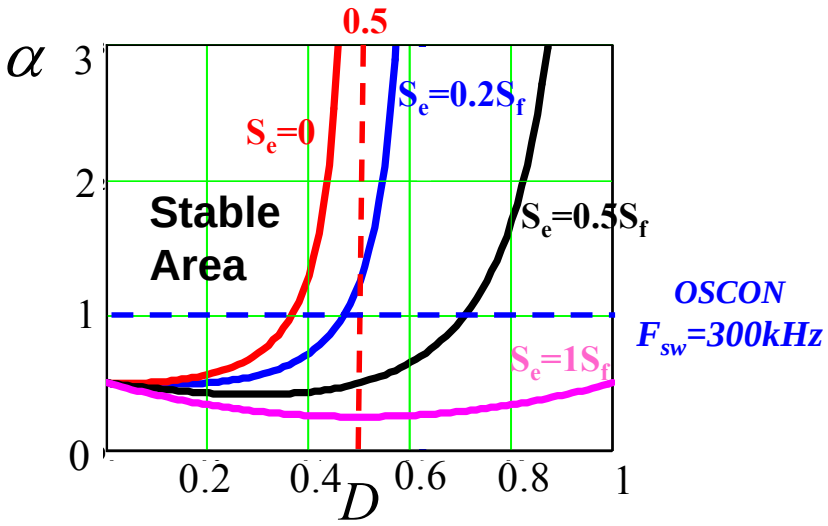


Figure 4. 25. Diagram of stability criterion with external ramp compensation.

Figure 4. 25 shows the stability criterion diagram with different external ramp compensations. Note that in Figure 4. 25 the horizontal axis is the whole duty cycle range. It is obvious that with an external ramp, the stability region can be expanded: using OSCON capacitor with 300kHz switching frequency ($\alpha \approx 1$) as an example, it is unstable when duty cycle is larger than 0.37 without an external ramp, when $S_e=S_f$, it is stable within all the duty cycle range.

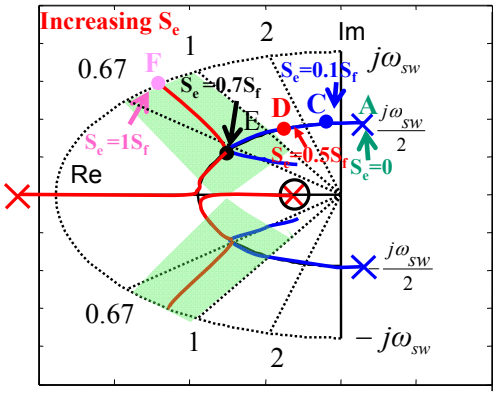
For optimal design purposes, external ramp should be selected appropriately to improve the dynamic performance. For illustration purpose, the pole-zero maps and bode plots of control-to-output voltage transfer function with a series of different external ramps for OSCON capacitor with F_{sw}=300kHz and D=0.4 are plotted in Figure 4. 26. Without an external ramp (shown as green point A), $Q_{e2}<0$ and the circuit is unstable. With the external ramp increasing, this double pole moves toward left half plane (shown as blue point C and red point D) and meets with another double pole at black point E, which is a key point since the quality factor for Q_{e2} is the smallest during the whole trajectory. The quality factor of the key point, Q_{e_k} can be derived from (4. 14) and is expressed in (4. 16):

$$Q_{e\_k} = \frac{2}{\pi}\frac{1}{\alpha} \tag{4. 16}$$

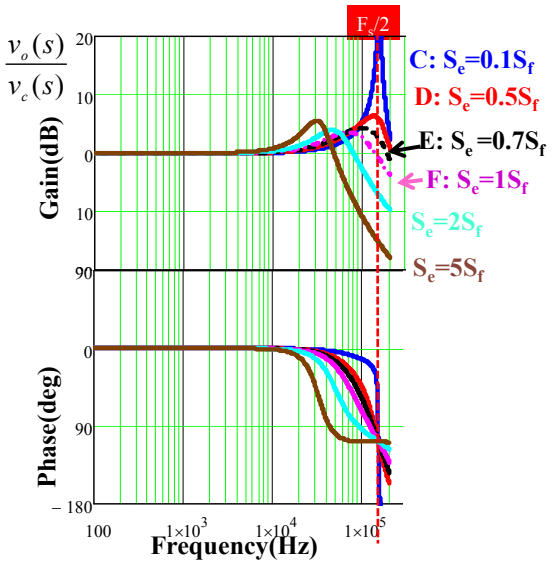
In this case, the value of Q_{e_k} is approximately $2/\pi$, which is smaller than 1. Further increasing S_e separates two pairs of double poles, one moves to a higher frequency, while the other one to a lower frequency. For design purposes, the external ramp should be designed appropriately: On one hand, it should be large enough to control quality factor for enough stability margin; On the other hand, it should not be too large, as it will slow down the transient performance by bringing a low frequency double pole with increased quality factor [D58][D59]. The suggested area is Q around 1, which is shown as the light green shaded area in Figure 4. 26(a). For example, the external ramp can be chosen to make $Q_{e2} = 2/\pi$, the required ramp magnitude can be solved from (4. 14), as shown in (4. 17):

$$\frac{s_e}{s_f} \approx 1 - \frac{1-D}{2\alpha} \tag{4. 17}$$

As shown in Figure 4. 26, when the external ramp is too small (Point C: $S_e=0.1S_f$), the peaking is large indicating bad dynamic performance. When the external ramp is too large ($S_e=5S_f$), there is a low frequency dominant double pole, which slows the transient performance . Therefore, the external ramp should be designed appropriately, e.g. around $Q_{e2}=2/\pi$, which is between point E and point F in Figure 4. 26 (a) and between the black dashed line ($S_e=0.7S_f$) and pink dashed line ($S_e=S_f$) in Figure 4. 26 (b). The preferred external ramp, in this case is between $0.7S_f$ to S_f.



(a)



(b)

Figure 4. 26. (a) Pole-zero mapping and (b) Bode plots of the control-to-output voltage transfer function with increasing external ramp for OSCON capacitor with F_{sw}=300kHz and D=0.4.

The output impedance transfer function with external ramp compensation is shown as (4. 18):

$$Z_o(s) \approx \frac{-R_{Co}T_{sw}\left(\frac{1}{2}-D+D\frac{s_e}{s_f}\right)*s*(R_{Co}C_o s+1)}{(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2})} \quad (4.\ 18)$$

Compare with (4. 13) , the external ramp not only influences the quality factor of double poles, but also increases the low frequency output impedance. As shown in Figure 4. 27, the low frequency impedance of S_e=5S_f is much larger than S_e=0.1S_f case while the high frequency impedance is much lower. This is because adding too much external ramp reduces the weight of output voltage in modulation process, which indicates reducing the ability to control the output voltage. Consider the total output impedance performance, S_e=0.7S_f is the best among the three, which is the same conclusion from control-to-output voltage transfer function.

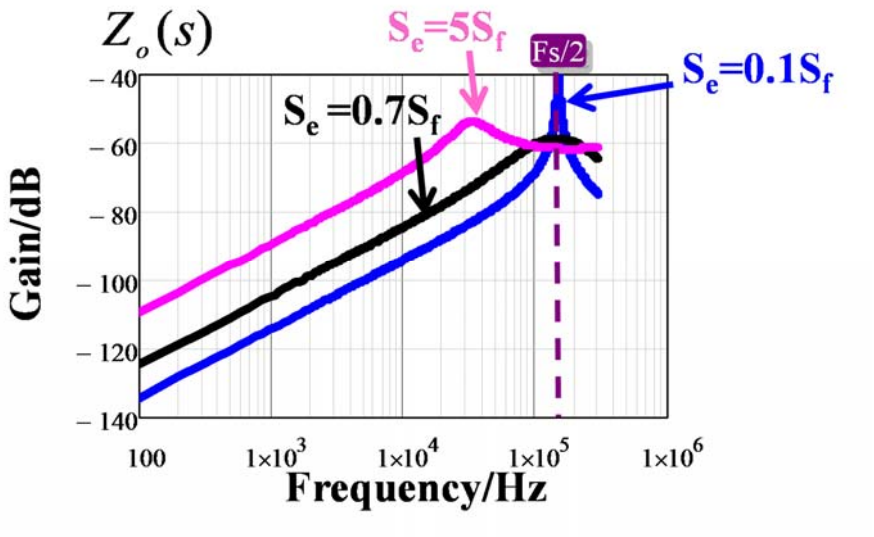
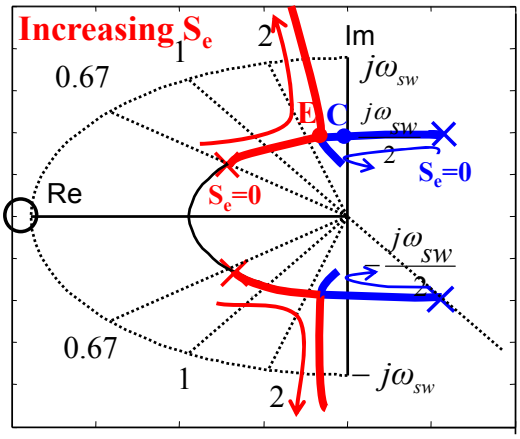


Figure 4. 27. Bode plots of output impedance with different external ramps for OSCON capacitor with F_{sw}=300kHz and D=0.4.

However, using external ramp to improve the dynamic performance has its limitation, which is dependent on current feedback strength α. As shown in (4. 16), when α is too small, the smallest quality factor is very large, which indicates that the peaking will be large for any case. To illustrate this point, consider the ceramic capacitor with f_{sw}= 600 kHz (α≈0.08) and D=0.1 case, the pole-zero trajectory and bode plots with different external ramps are shown in Figure 4. 28. For this case, the minimum value of Q_{e2} is about 7.6, no matter how much external ramp is used, the peaking is no less than 20dB, as shown in Figure 4. 28(b).Therefore, additional current ramp is needed to improve the dynamic performance.



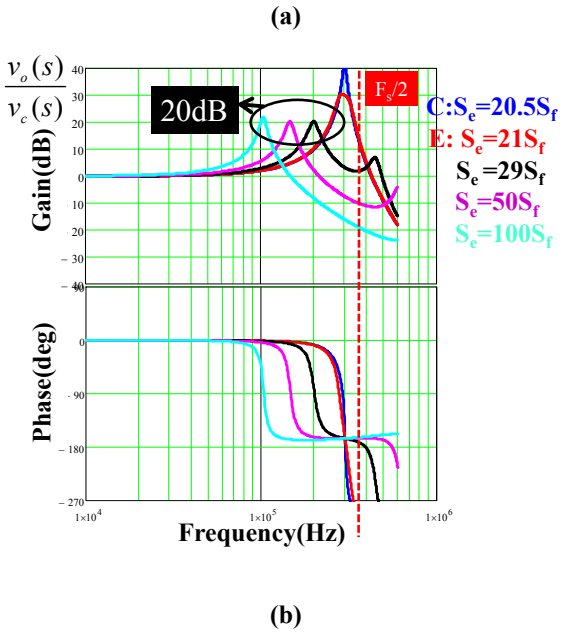


Figure 4. 28. (a) Pole-zero trajectory and (b) Bode plots of the control-to-output voltage transfer function with increasing external ramp for ceramic capacitor with F_{sw}=600kHz and D=0.1.

4.3.4 Optimal design of hybrid ramp for ceramic capacitors

As analyzed in section 4.3.3, to provide better damping for the ceramic cap case, it is necessary to enhance the current strength feedback by adding current information. Therefore, hybrid ramp strategy is proposed for optimum design purpose: current ramp is used to enhance current strength feedback to minimize the effect of capacitor voltage feedback loop, while external ramp is used to reduce the effect of sample and hold effect for the inductor current feedback loop. The hybrid ramp strategy is first proposed in [D57] in digital constant on-time VRM application. The hybrid ramp includes the external ramp and the estimated inductor current ramp, which is provided by a digital inductor current estimator, by only sampling the input voltage, output voltage and average inductor current with low oversampling rate ADCs. For analog constant frequency V^2 control, either inductor current or capacitor current can be used to enhance current feedback strength, as shown in Figure 4. 29(a) and Figure 4. 29(b).

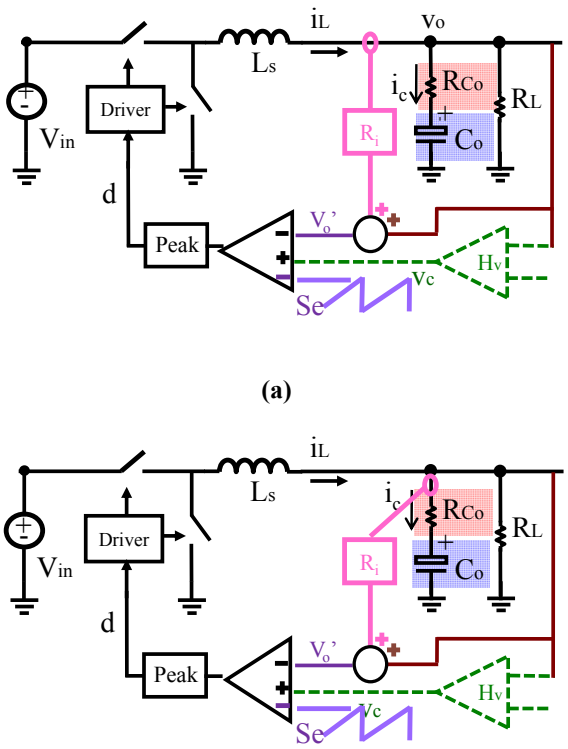


Figure 4. 29. Constant frequency V^2 peak control with hybrid ramp compensation: (a) with inductor current ramp (b) with capacitor current ramp

Additional current feedback changes the current feedback strength from α to α', which is defined as (4. 21):

$$\alpha' = \frac{(R_{Co} + R_i)C_o}{T_{sw}} \tag{4. 19}$$

Compared with (4. 8), it can be seen that R_i enhances current feedback strength as a virtual ESR. The small-signal model for constant frequency V^2 peak control with hybrid ramp is shown as (4. 14), with the modification that α is replaced with α' and s_f is replaced with s_f' shown in (4. 20), both of the parameters are modified by R_i. Therefore, the conclusions associated with (4. 14) are all applicable.

$$s_f' = (R_{Co} + R_i)\frac{V_o}{L_s} \tag{4. 20}$$

The suggested design guidelines are as follows:

Step 1: Design R_i to enhance current information so that the following equation is met:

$$\alpha' = \frac{(R_{Co} + R_i)C_o}{T_{sw}} = 1 \tag{4. 21}$$

Step 2: Design s_e to control Q_{e2}: for example, $Q_{e2}=2/\pi$, then S_e should be:

$$\frac{s_e}{s_f'} \approx 1 - \frac{1-D}{2\alpha'} = \frac{1+D}{2} \tag{4. 22}$$

For example, for ceramic capacitors with f_{sw}=600 kHz and D=0.1, according to the above design guideline, design R_i =2mΩ and S_e=0.55S_f'. As shown in Figure 4. 30, a flat gain up to a very high frequency can be achieved. Compared with the large peaking using only external ramp compensation, a well-damped system can be achieved with a hybrid ramp.

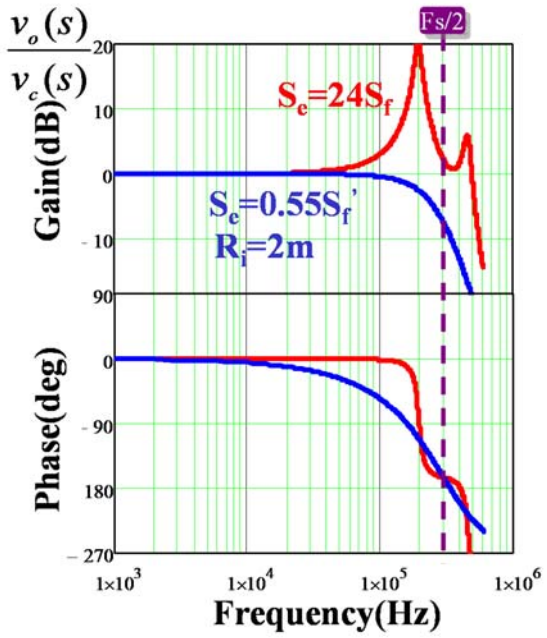


Figure 4. 30. Comparisons of bode plots of control-to-output voltage transfer function for ceramic capacitor with F_{sw}=600 kHz and D=0.1: external ramp (red) and hybrid ramp (blue).

The output impedance transfer function with hybrid ramp (inductor current) compensation is shown as follows:

$$Z_o(s) \approx \frac{-\left(R_i + R_{Co}T_{sw}\left(\frac{1}{2} - D + D\frac{s_e}{s_f}\right) * s\right) * (R_{Co}C_o s + 1)}{(1 + \frac{s}{Q_{e1}\omega_2} + \frac{s^2}{\omega_2^2})(1 + \frac{s}{Q_{e2}\omega_2} + \frac{s^2}{\omega_2^2})} \quad (4.\ 23)$$

Compare with (4. 18), the additional inductor current ramp has dramatic effect on low frequency output impedance. As shown in Figure 4. 31, low frequency output impedance is determined by R_i with hybrid ramp design. The reason for this is the inductor current ramp includes DC information, which introduces a droop function while the capacitor current information only has switching frequency information. This characteristic may be utilized in applications where adaptive voltage positioning is required. However, it is not required for typical point-of-load application, to reduce the low frequency output impedance, one method is to add a high pass filter after current sensing network to eliminate the DC inductor current. An alternative method, capacitor current sensing can be utilized as it does not have DC current information. For more discussion on this, please refer to section 4.2.3 and 4.2.4.

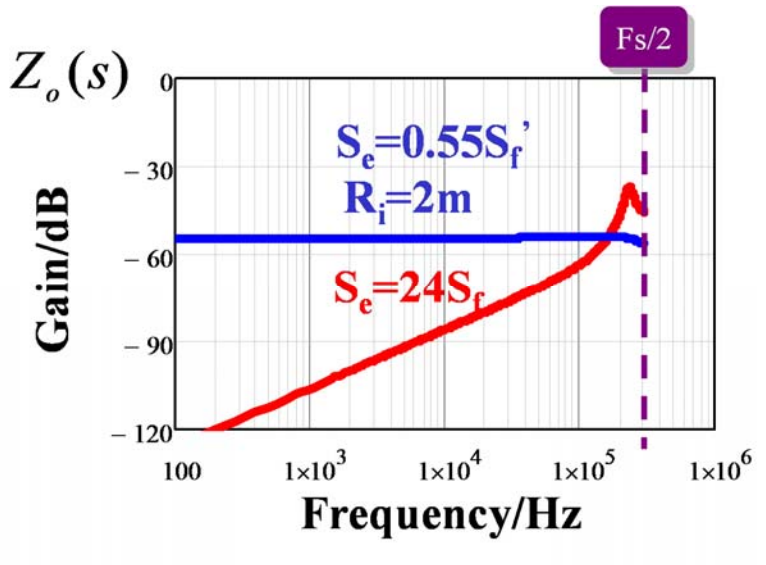


Figure 4. 31. Comparisons of bode plots of output impedance transfer function for ceramic capacitor with F_{sw}=600 kHz and D=0.1: external ramp (red) and hybrid ramp (blue).

4.3.5 Simulation and experimental verification

The SIMPLIS simulation tool is used to verify the small-signal analysis for constant frequency V^2 control. Circuit parameters are shown as follows: OSCON capacitor, C_o =560μF, R_C =6mΩ, V_o=1.8V, L_s=2.3uH, I_o=1.5A. From stability criterion in (4. 11), for F_{sw}=300kHz, α is around 1, the instability point occurs when D is 0.37. As shown in Figure 4. 32(a), when V_{in}=5V corresponding to D=0.36, the circuit is stable, while in Figure 4. 32 (b), when V_{in}=4.5V corresponding to D=0.4, the circuit is unstable as sub-harmonic oscillation is shown. This agrees with the prediction from (4. 11). Figure 4. 32 (c) shows the effect of current feedback strength α on stability, in this case, F_{sw}=600kHz, α is around 2, from (4. 11), with increasing α, the instability point is D=0.43 which means the circuit should be stable at 0.4 duty cycle, which is verified in Figure 4. 32 (c).

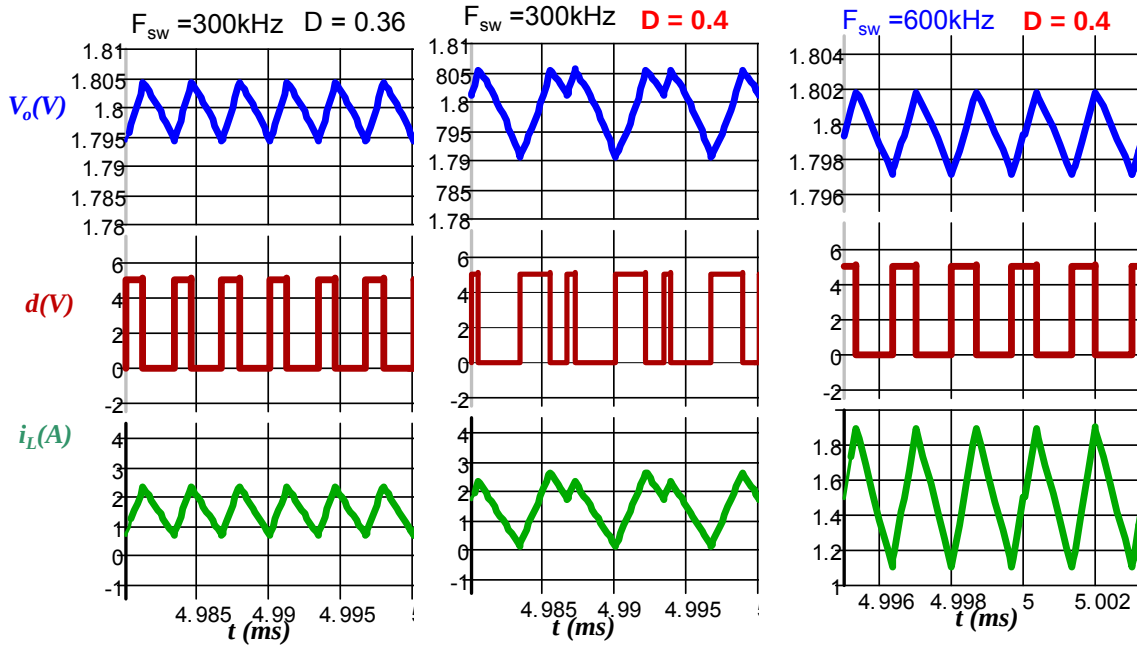
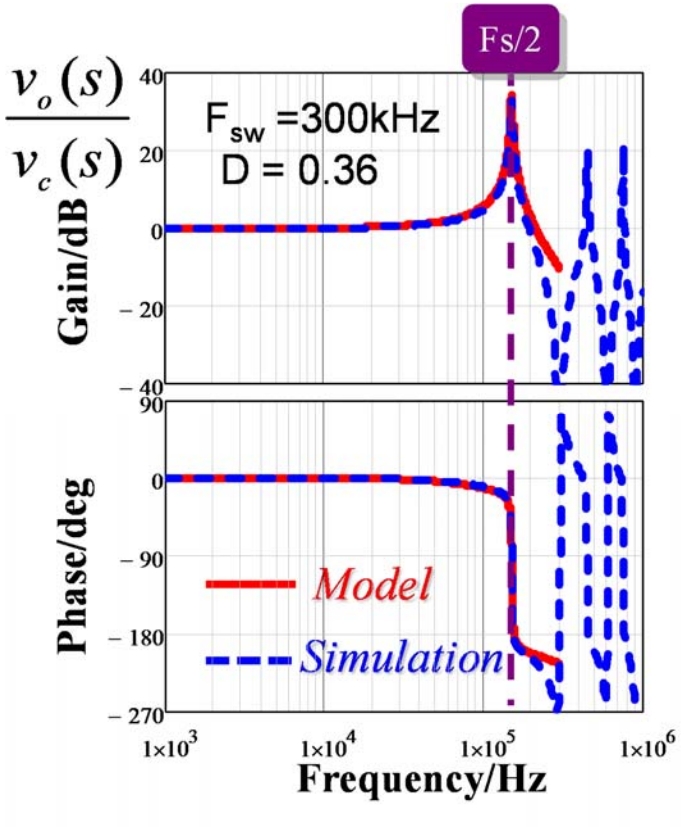
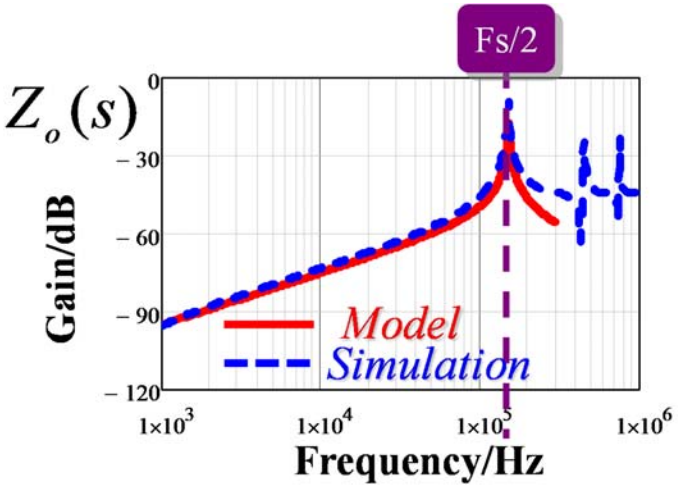


Figure 4. 32. Operating waveforms with different circuit parameters (a) F_{sw}=300kHz, V_{in}=5V,D=0.36, stable (b) F_{sw}=300kHz,V_{in}=4.5V,D=0.4, unstable (c) F_{sw}=600kHz,V_{in}=4.5V,D=0.4, stable

Figure 4. 33 shows the comparison between equivalent circuit model and simulation results. It can be seen that both the control-to-output and output impedance are accurate at half of switching frequency and useful up to switching frequency. The models are simple and can predict the peaking at half of switching frequency very accurately. It is very close to the instability point as the double pole at half of switching frequency has a very large quality factor, which can be seen from Figure 4. 33 (a) where the peaking on gain plot is very high and the phase drops very fast at half of switching frequency.



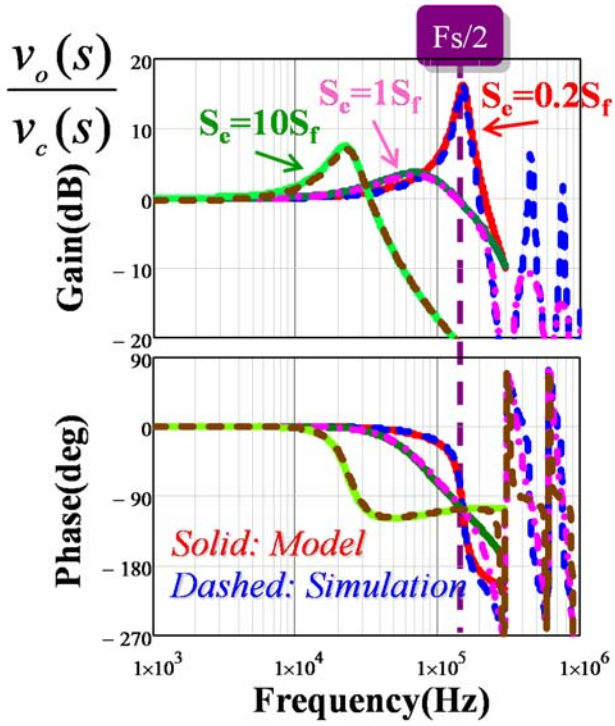
(a)



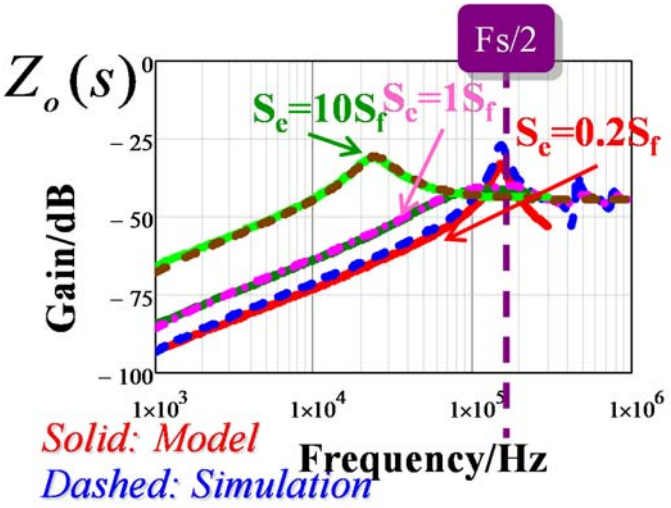
(b)

Figure 4. 33. Small-signal model verification with F_{sw}=300kHz, V_{in}=5V, D=0.36 (a) Control-to-output transfer function (b) Output impedance.

Figure 4. 34 shows the small-signal verification for constant frequency V^2 peak control with different external ramps and the following circuit parameters: OSCON capacitor, C_o =560μF, R_C=6mΩ, F_{sw}=300kHz, V_{in}=4.5V, D=0.4. The model agrees with simulation results very well.



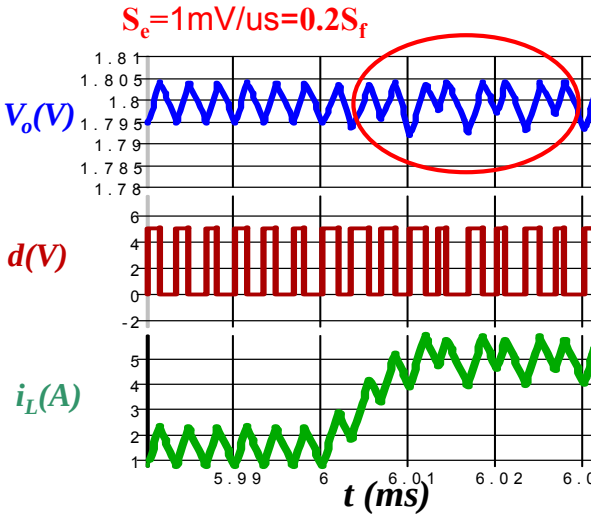
(a)



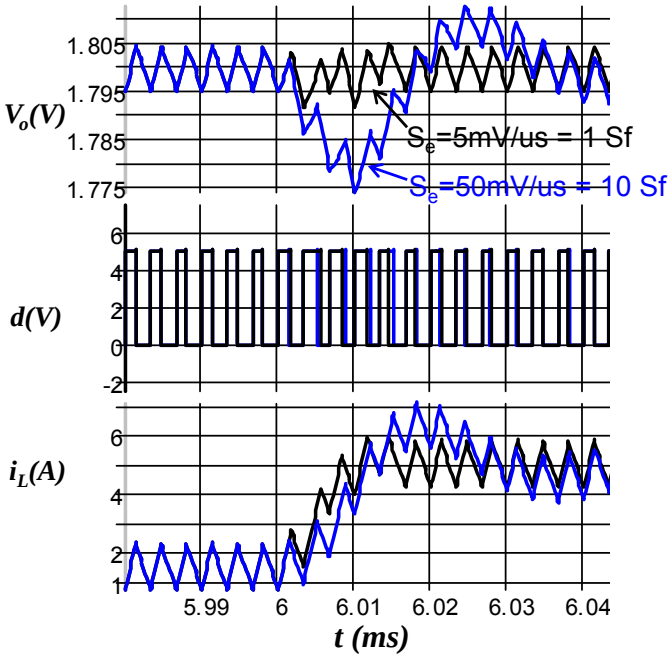
(b)

Figure 4. 34. Small-signal verification for constant frequency V^2 peak control with different external ramps and with parameters: OSCON capacitor, F_{sw}=300kHz, D=0.4 (a) Control-to-output transfer function (b) Output impedance.

To verify proposed design guideline, load transient performances are compared among three different external ramp designs, as shown in Figure 4. 35. The load step up is from 1.5A to 5A in all the cases. In Figure 4. 35(a), small external ramp s_e=0.2s_f is used, before load step, the circuit is stable. However, as Figure 4. 34 shows, the quality factor in this case is very large which indicates small stability margin. As shown in Figure 4. 35(a), after load step up, sub-harmonic oscillation occur. In Figure 4. 35(b), proposed external ramp s_e=s_f and a very large external ramp s_e=10s_f is used and load transient performances are compared. It is clearly shown that too large external ramp is detrimental to the transient performance: with s_e=10s_f, the transient performance is more oscillatory and a long settling time is required. With proposed s_e=1s_f, the transient performance is much better with just a few switching cycle to reach the new steady state. Among the three, the transient performance with s_e=s_f is the best which verifies proposed design guideline.



(a)

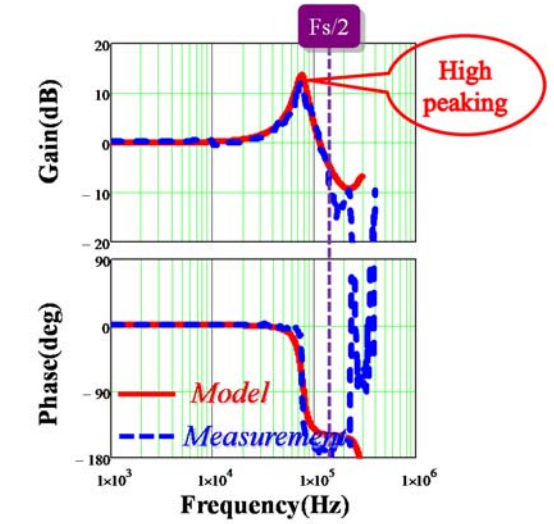


(b)

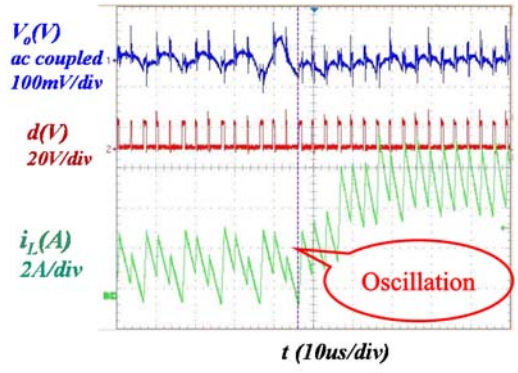
Figure 4. 35. Load step-up transient performance (1.5A-5A) comparisons for constant frequency V^2 peak control with different external ramps (a) $S_e=0.2S_f$ (b) $S_e=1S_f$ and $S_e=10S_f$.

To verify the ineffectiveness of external ramp compensation for ceramic capacitor applications where current feedback strength α is very small. Experiments on the control-to-output voltage transfer function and load transient measurements are conducted based on the demo-board NCP5422A from ON

semiconductor. The circuit parameters are shown as follows: F_{sw} =305kHz, D=0.15, V_{in}=12V V_o=1.8V, Ceramic capacitor: C_o =300μF, R_C =2mΩ, L_s=1.3uH and the measurement is based on the network analyzer Agilent 4395A. Figure 4. 36(a) shows the small-signal measurements using only external ramp S_e=21mV/us. The results show that the model agrees very well with the experiment. Since α is only around 0.2 in this case, although a relatively large external ramp is used, there is still high peaking from the gain plot. Figure 4. 36(b) shows step up load transient (1.5A to 5A) experimental result, the dynamic performance is very poor and there is oscillation during transient due to large quality factor.



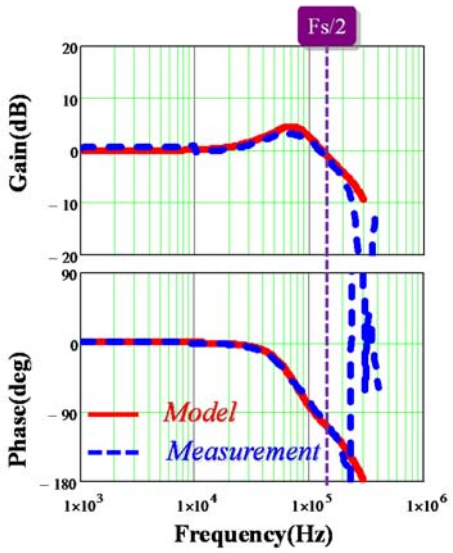
(a)



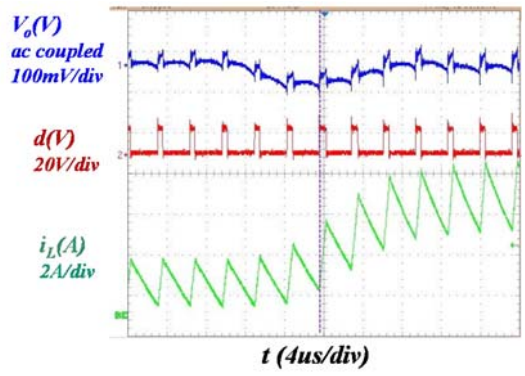
(b)

Figure 4. 36. Experimental results for ceramic caps with only external ramp compensation. (a) Control-to-output voltage transfer function (b) Load transient step-up (1.5A—5A) performance.

Figure 4. 37 shows the small-signal measurement and load transient result with additional current feedback strength. In this case R_i= 7m and α is around 0.8. As shown in Figure 4. 37(a), the small-signal model agrees with the measurement result and the peaking decreases significantly when compared with Figure 4. 36(a). Therefore, the dynamic load transient performance shown in Figure 4. 37(b) improves substantially. This verifies that for ceramic caps, current ramp is required in order to achieve a well-damped performance.



(a)



(b)

Figure 4. 37.Experimental results for ceramic caps with hybrid ramp compensation. (a) Control-to-output voltage transfer function (b) Load transient step-up (1.5A—5A) performance

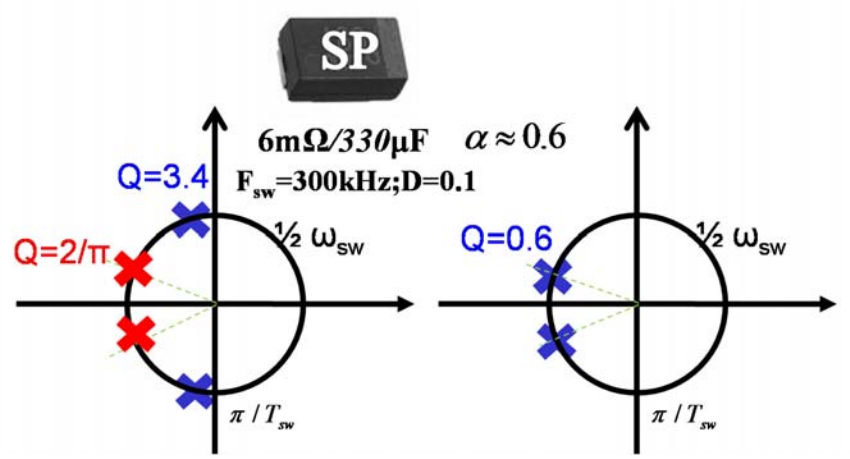
4.4 Performance Comparison between V^2 with Different Modulation Schemes

For comparison purpose, the control-to-output voltage transfer functions of constant frequency V^2 peak control and constant on-time V^2 control for small duty cycle application are rewritten as shown in (4. 24) and (4. 25), respectively:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2})}, \omega_2=\frac{\pi}{T_{sw}}, Q_{e1}=\frac{1}{\pi}\frac{1}{D'-0.5}, Q_{e2}=\frac{1}{\pi}\frac{1}{\alpha-0.5} \quad (4.\ 24)$$

$$\frac{v_o(s)}{v_c(s)} \approx \frac{R_{Co}C_o s+1}{1+\frac{s}{Q_3\omega_2}+\frac{s^2}{\omega_2^2}}, \omega_2=\frac{\pi}{T_{sw}}, Q_3=\frac{1}{\pi}\frac{1}{\alpha-\frac{D}{2}} \quad (4.\ 25)$$

For constant frequency V^2 peak control, the double pole caused by inductor current loop is located at ½ f_{sw}. As a comparison, for constant on-time V^2 control, the double pole caused by inductor current loop is located at 1/(2D)*f_{sw}, which is much higher than ½ f_{sw} for small duty cycle application. Besides, although the position of the double pole caused by capacitor voltage loop are all located at ½ f_{sw} for all modulation schemes, the damping of the double pole is also different. To illustrate the difference, Figure 4. 38 shows the comparisons of poles locations with SP capacitors. For constant on-time modulation, only one pair of double pole exist at ½ f_{sw} and the damping is larger than constant frequency V^2 case. Therefore, from dynamic performance point of view, constant on-time modulation is better.



(a) **(b)**

Figure 4. 38. Comparisons of pole locations between (a) constant frequency V^2 peak control and (b) constant on-time V^2 control with SP capacitors with D=0.1 and f_{sw}=300kHz

Figure 4. 39 shows comparison of minimum switching frequency for constant frequency V^2 peak control and constant on-time V^2 control. A much higher switching frequency is required for constant frequency V^2 peak control from stability point of view.

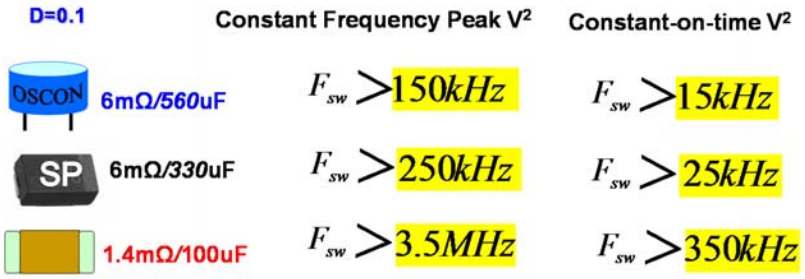


Figure 4. 39.Stability criterion comparison between constant frequency V^2 peak control and constant on-time V^2

4.5 Summary

In this chapter, design guidelines for VR applications and general point-of-load applications are provided. For VR application, current sensing gain R_i is determined by load line requirement and capacitors are selected to meet output impedance requirement. For general point-of-load applications, controlled ESR ceramic capacitors is a good option for portable electronics while V^2 control with additional current information is preferred when large capacitance is required or very small ripple is required. For constant frequency V^2 peak control, stability is not only related to the duty cycle, but also to current feedback strength. A sub-harmonic oscillation occurs either in a large duty cycle application or in application with small current feedback strength (e.g. with ceramic capacitors). With large current feedback strength (e.g. with OSCON capacitors), the external ramp is effective to solve the instability problems and achieve good dynamic performance as long as it is designed appropriately (e.g. shown in Figure 4. 16). However, using only an external ramp is not an effective solution when current feedback strength is small (e.g. with ceramic capacitors). In this case, hybrid ramp which includes both external ramp and current ramp is proposed to improve the dynamic performance. Generally speaking, constant on-time modulation is better than constant frequency modulation from dynamic performance point of view.

Chapter 5. Simplified Equivalent Circuit Model of Series Resonant Converter

5.1 Introduction

Series resonant converter has been used widely for power conditioning in the sophisticated aerospace industry [E2]-[E6] and in some industrial applications such as laser power supply applications [E7]. Most of the applications involve a regulated voltage output, therefore a feedback loop is incorporated into the control system to stabilize the output voltage. For optimal design purpose, small-signal models are indispensable. For resonant converters, an interesting phenomenon which is referred to as the beat frequency dynamics [E21] is well-known. As discussed in 1.2.3, all previous small-signal models shown in [E13]-[E26] can not achieve accuracy and simplicity at the same time. Up to now, the equivalent circuit model proposed by E. Yang in [E26] based on the results by the extended describing function concept is the most successful model. It is very accurate compared with simplis simulation and experimental results, as shown in Figure 1. 38. However, the order of the equivalent circuit model is too high and the transfer functions are still derived based on numerical solution instead of analytical solutions. This chapter tries to simplify the small-signal equivalent circuit model of SRC to a third-order circuit which is simpler but accurate enough to predict beat frequency dynamics. Besides, analytical expressions for all transfer functions will be provided to help engineers to design the feedback loop.

5.2 Review of Equivalent Circuit Model Proposed by E. Yang

As shown in Figure 5. 1, for series resonant converter, tank current does not have DC components but contain strong switching frequency harmonics. Therefore, the averaging concept breaks down.

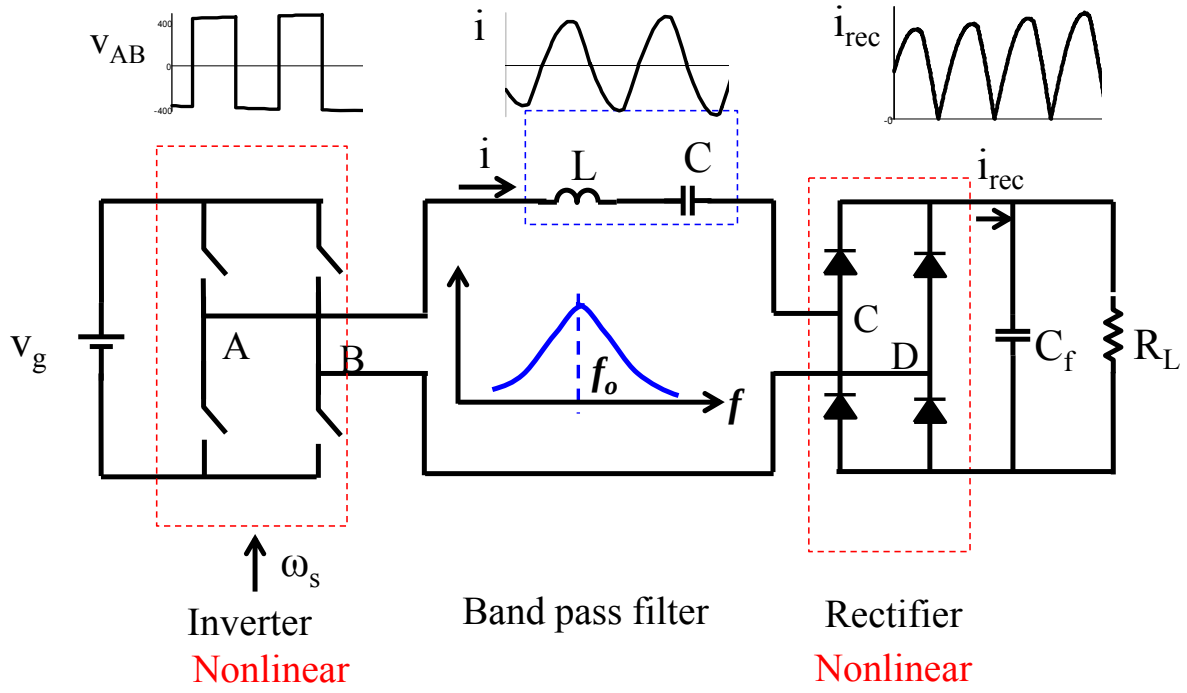


Figure 5. 1. Diagram of series resonant converter with waveforms of major signals

Up to now, the equivalent circuit model for proposed by E. Yang in [E26] based on the results by the extended describing function concept is the most successful model. During the derivation, Fundamental approximation is used, i.e. only fundamental components of resonant tank variable is considered. For the three working conditions shown in Figure 5. 2, the fundamental component is dominant and fundamental approximation is reasonable. When switching frequency is far away from resonant frequency, the THD can be very large. However, as shown in [E27], even in this

condition, the small-signal model using fundamental component is adequate accurate for series resonant converter.

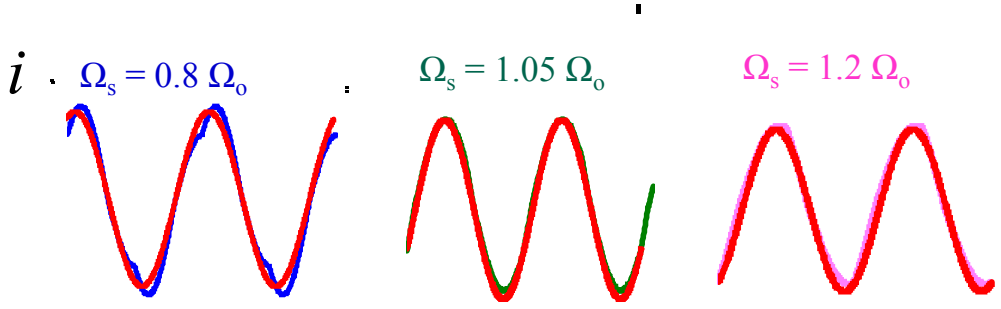


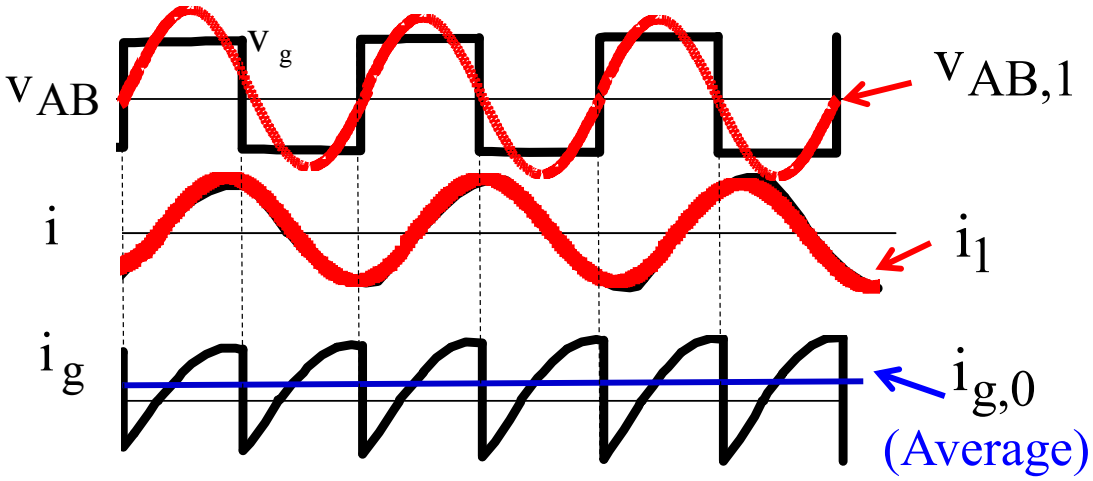
Figure 5. 2 Comparison of simulated resonant current waveforms and fundamental approximation.

The describing function methods are applied to the inverter, rectifier and resonant tank, respectively. For the inverter, the waveforms are shown as Figure 5. 3 (a). The input of the inverter uses average approximation while the output uses fundamental approximation. The small-signal model is shown in Figure 5. 3 (b): for the input side, it is a controlled current source as the average value of the input current is related with resonant current; for the output side, it is a controlled voltage source as the magnitude of fundamental component $v_{AB,1}$ is related with input voltage v_g. The expressions are shown as follows:

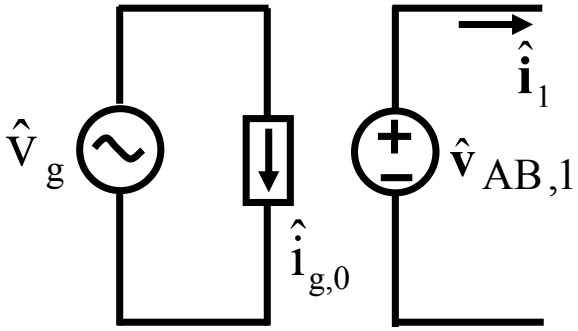
$$\hat{i}_{g,0} = \frac{2}{\pi}\mathrm{Re}\left(\hat{\mathbf{i}}_1(\omega_m)\right), \hat{\mathbf{v}}_{AB,1} = \frac{4}{\pi}\hat{v}_g \tag{5. 1}$$

For the rectifier, the scenario is similar. The waveforms are shown as Figure 5. 4(a). The input uses fundamental approximation while the output uses average approximation. The small-signal model is shown in Figure 5. 4(b): for the input side, it is a controlled voltage source as the magnitude of fundamental component $v_{R,1}$ is related with input voltage v_o; for the output side, it is a controlled current source as the average value of the output current is related with resonant current; The expressions are shown as follows:

$$\hat{v}_{R,1} = k_{vo}\hat{v}_o + k_{is}\,\mathrm{Re}(\hat{\mathbf{i}}_1) + k_{ic}\,\mathrm{Im}(\hat{\mathbf{i}}_1)\,,\ \hat{i}_{R,0} = k_s\,\mathrm{Re}(\hat{\mathbf{i}}_1) + k_c\,\mathrm{Im}(\hat{\mathbf{i}}_1) \tag{5. 2}$$

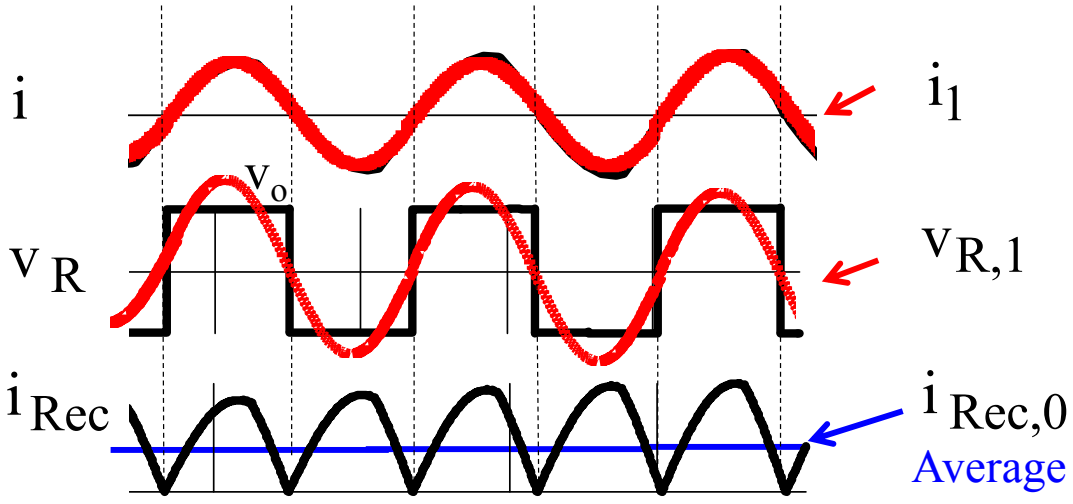


(a)



(b)

Figure 5. 3 (a) Waveforms of input and output of inverter. (b) small-signal model of the inverter



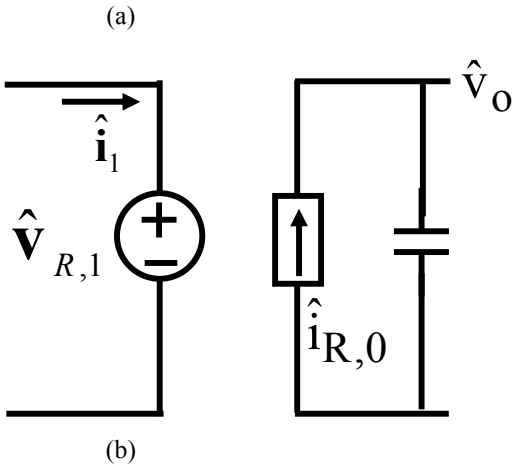


Figure 5. 4 (a) Waveforms of input and output of rectifier (b) small-signal model of the rectifier

For the resonant inductor and resonant capacitor, the small-signal models based on describing function are shown as Figure 5. 5 and Figure 5. 6, respectively. There is one complex impedance due to the effect of switching frequency which is shaded in green. Besides, there is one complex voltage source due to perturbation of switching frequency in Figure 5. 5 and complex current source in Figure 5. 6, both are shaded in blue.

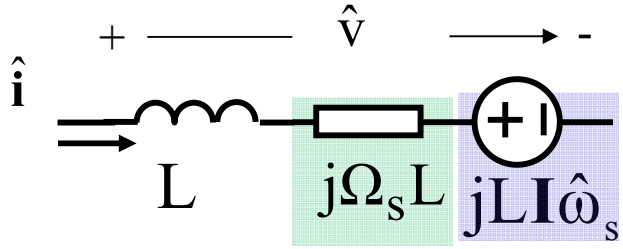


Figure 5. 5 small-signal model of the resonant inductor

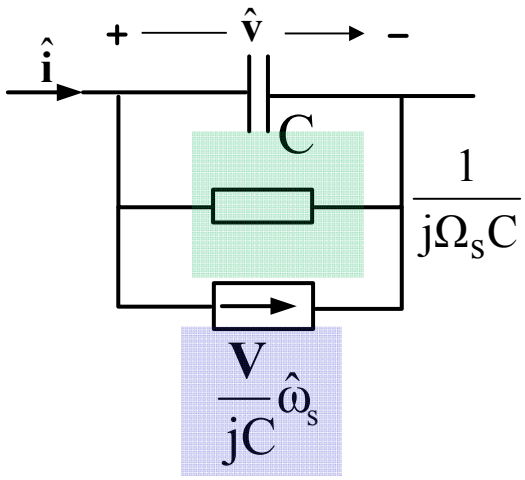


Figure 5. 6 small-signal model of the resonant capacitor

Combine the small signal models of inverter, resonant indicator and capacitor, rectifier and output filter, the small signal model of series resonant converter can be derived as shown in Figure 5. 7. However, due to the complex number of the impedance and controlled sources shaded in red and blue, this equivalent circuit model can not be simulated.

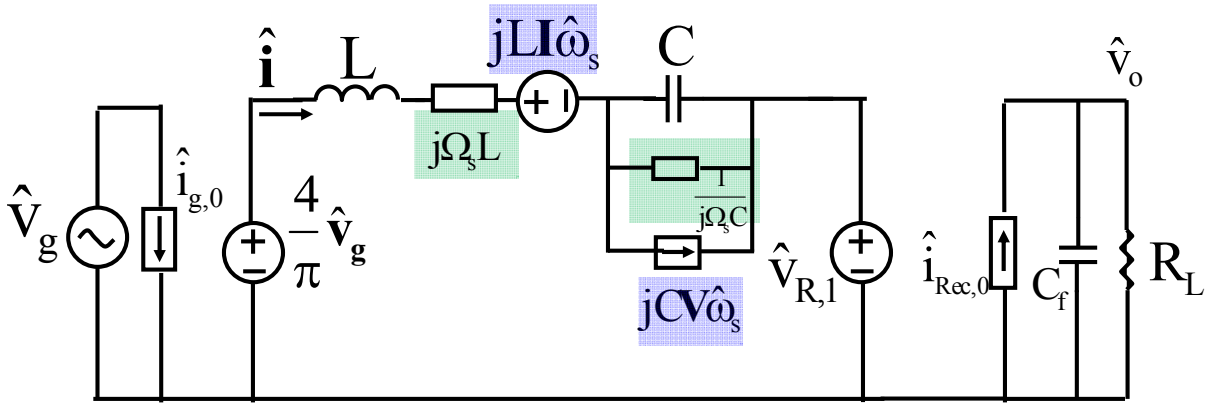


Figure 5. 7 small-signal model of series resonant converter

To derive an equivalent circuit model suitable for simulation, E. Yang separates the sine part and cosine part, which in concept are orthogonal, as shown in Figure 5. 8. By this way, the complex terms disappears but some coupling terms occurs. This is reasonable as the complex term in essence changes the sine part into cosine part and vice versa. Therefore, the j terms shown in Figure

5. 7 are replaced by the coupled terms in Figure 5. 8. The equivalent circuit model shown in Figure 5. 8 is suitable for simulation.

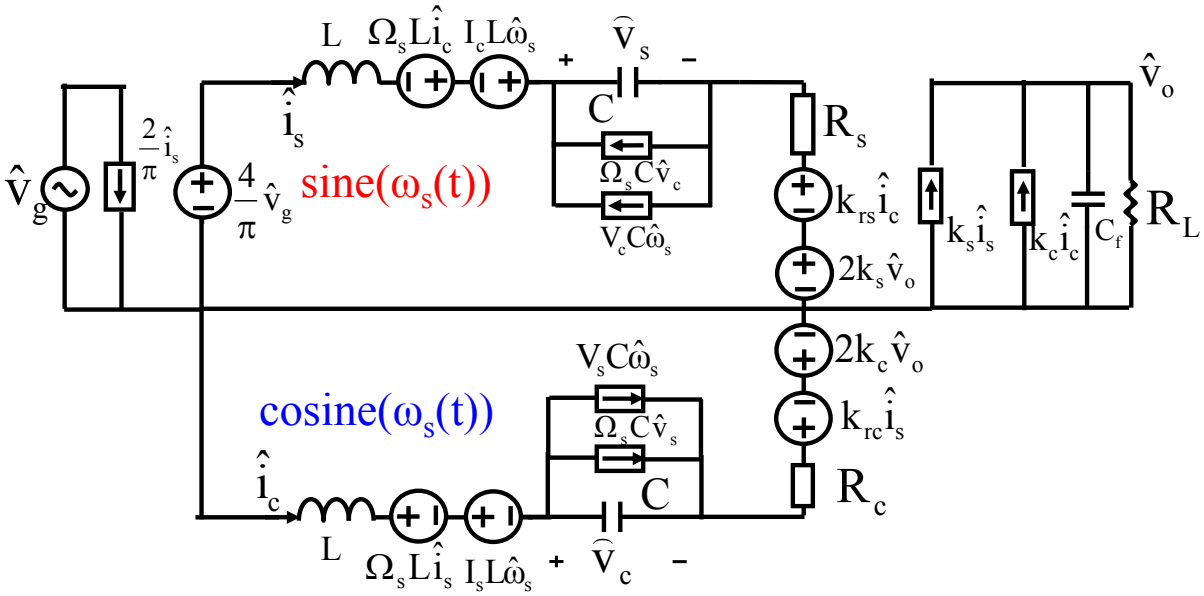


Figure 5. 8. small-signal model of series resonant converter suitable for simulation

V_s, V_c, I_s and I_c are derived from steady state solutions and the results are shown below:

$$\mathbf{I_s} = \frac{4V_g}{\pi}\frac{R_{eq}}{R_{eq}^{\ 2}+X_{eq}^{\ 2}}, \mathbf{I_c} = -\frac{4V_g}{\pi}\frac{X_{eq}}{R_{eq}^{\ 2}+X_{eq}^{\ 2}}$$
$$\mathbf{V_s} = -\frac{4V_g}{\pi\Omega_s C}\frac{X_{eq}}{R_{eq}^{\ 2}+X_{eq}^{\ 2}}, \mathbf{V_c} = -\frac{4V_g}{\pi\Omega_s C}\frac{R_{eq}}{R_{eq}^{\ 2}+X_{eq}^{\ 2}} \quad (5.\ 3)$$

X_{eq} represents the tank impedance at switching frequency, R_{eq} represents the equivalent load resistance. The expressions are shown as follows:

$$X_{eq} = \Omega_s L - \frac{1}{\Omega_s C}, R_{eq} = \frac{8}{\pi^2}R_L \quad (5.\ 4)$$

Expressions of k_{rs}, k_{rc}, R_s, R_c, k_s and k_c are shown as below:

$$
\begin{aligned}
k_{rs} &= k_{rc} = \frac{{R_{eq}}^2 X_{eq}}{{X_{eq}}^2 + {R_{eq}}^2} \\
k_s &= \frac{2}{\pi}\frac{R_{eq}}{\sqrt{R_{eq}^2 + X_{eq}^2}}, k_c = -\frac{2}{\pi}\frac{X_{eq}}{\sqrt{R_{eq}^2 + X_{eq}^2}} \\
R_s &= R_{eq}\frac{{X_{eq}}^2}{{X_{eq}}^2 + {R_{eq}}^2}, R_c = R_{eq}\frac{{R_{eq}}^2}{{X_{eq}}^2 + {R_{eq}}^2}
\end{aligned}
\tag{5. 5}
$$

As shown in Figure 1. 38, the small-signal model equivalent circuit model can well capture the beat frequency dynamics and is very accurate compared with simplis simulation result. From Figure 1. 38, the small-signal behavior is sufficient to be described as a third-order circuit. However, the order of the equivalent circuit model in Figure 5. 8 is five and obviously too high. More importantly, the transfer functions are still derived based on numerical solution instead of analytical solutions. This intrigues the continuing work to simplify the equivalent circuit model and derive the analytical solution for series resonant converter.

5.3 Proposed Simple Equivalent Circuit Model for SRC

5.3.1 Simplification of resonant capacitor branch

To simplify the equivalent circuit model, the focus is on the model of the resonant tank. As shown in Figure 5. 6, the small signal model of the resonant capacitor is a traditional capacitor with one complex impedance and one controlled current sources. It is of critical value to understand and analyze the effect of the complex impedance and the controlled current course. For simplicity, first we consider a particular case in which $\hat{\omega}_s = 0$. In this case the controlled current sources is disappeared, as shown in Figure 5. 9 (a).

To analyze the effect of complex impedance, we do the following mathematical analysis:

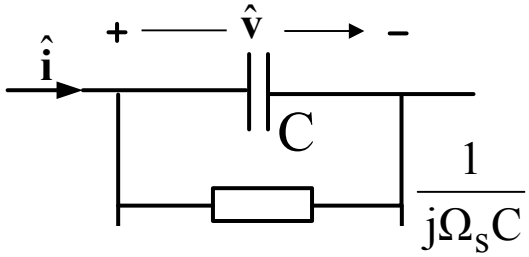
$$\frac{\hat{\mathbf{v}}}{\hat{\mathbf{i}}} = \frac{1}{sC + j\Omega_s C} = \frac{1}{j\Omega_s C(\frac{s}{j\Omega_s} + 1)} = \frac{-\frac{s}{j\Omega_s} + 1}{j\Omega_s C(\frac{s}{j\Omega_s} + 1)(-\frac{s}{j\Omega_s} + 1)} = \frac{-\frac{s}{j\Omega_s} + 1}{j\Omega_s C(1 + \frac{s^2}{\Omega_s^2})} \tag{5. 6}$$

Under the condition that $\omega_m << \Omega_s$, the second term in the denominator is much less than 1 and therefore can be neglected. The simplification leads to the following:

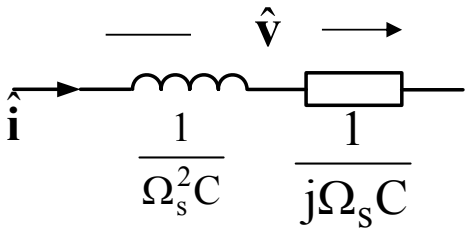
$$\frac{\hat{\mathbf{v}}}{\hat{\mathbf{i}}} \approx \frac{-\frac{s}{j\Omega_s} + 1}{j\Omega_s C} = \frac{s}{{\Omega_s}^2 C} + \frac{1}{j\Omega_s C} \tag{5. 7}$$

The above equation can be represented using an equivalent circuit, shown as in Figure 5. 9 (b). Very surprisingly, the capacitor in parallel with the complex impedance can be simplified as

an equivalent inductor in series with the same complex impedance, with the inductance value determined by switching frequency and capacitance value.



(a)



(b)

Figure 5. 9. (a) Original small-signal model of resonant capacitor @ $\hat{\omega}_s = 0$ (b) Equivalent model under $\omega_m << \Omega_s$

The above phenomenon is very interesting as it is somewhat against the common sense in PWM converter: a capacitor and an inductor are two basic energy storage elements with very different dynamic behavior. In other words, there is no such case in PWM converter that a capacitor can be turned into an inductor. However, the transformation in Figure 5. 9 shows that in resonant converter, for low frequency modulation $\omega_m << \Omega_s$, the capacitor behaves like an equivalent inductor with respect to modulation frequency ω_m. It should be noted that this conclusion is only valid in the case that the modulation signal is carried by carrier frequency (switching frequency). Therefore, this phenomenon only exist in resonant converters and can never be observed in PWM type converters.

The above phenomenon can also be interpreted from spectrum perspective with more physical insights. As shown in Figure 5. 10, the current in the resonant tank has both modulation frequency

(the envelope) and switching frequency. The spectrum of resonant current includes f_s, f_s-f_m and f_s+f_m components. The modulation signal is carried by the sideband components f_s-f_m and f_s+f_m. The impedance of the capacitor in frequency domain is decreasing monotonously. As a result, the voltage on f_s-f_m is dominating. When f_m of resonant current increases, f_s-f_m moves to lower frequency (see the green bar in frequency spectrum), the voltage on f_s-f_m also increases. In other words, with respect to modulation frequency, the voltage increases as the modulation frequency increases. From this perspective, the resonant capacitor behaves like an equivalent inductor: for a traditional inductor, when the modulation frequency of the current increases, the voltage across the inductor also increases as the impedance of the inductor is increasing. As stated previously, this scenario only happens when modulation frequency signal is carried by the sideband component, which is a special phenomenon in the resonant tank due to resonant behavior.

Although the above analysis is based on a simple case when $\hat{\omega}_s = 0$, similar conclusion can be drawn for general case. As shown in Figure 5. 11 (a) and (b), the original small-signal model can be represented as an equivalent inductor branch, using the previous result. By Thevenin's Theorem, final simplified equivalent circuit model can be derived as shown in Figure 5. 11 (c). Compared Figure 5. 11 (a) with Figure 5. 11 (c), the capacitor behaves like an equivalent inductor with respect to modulation frequency.

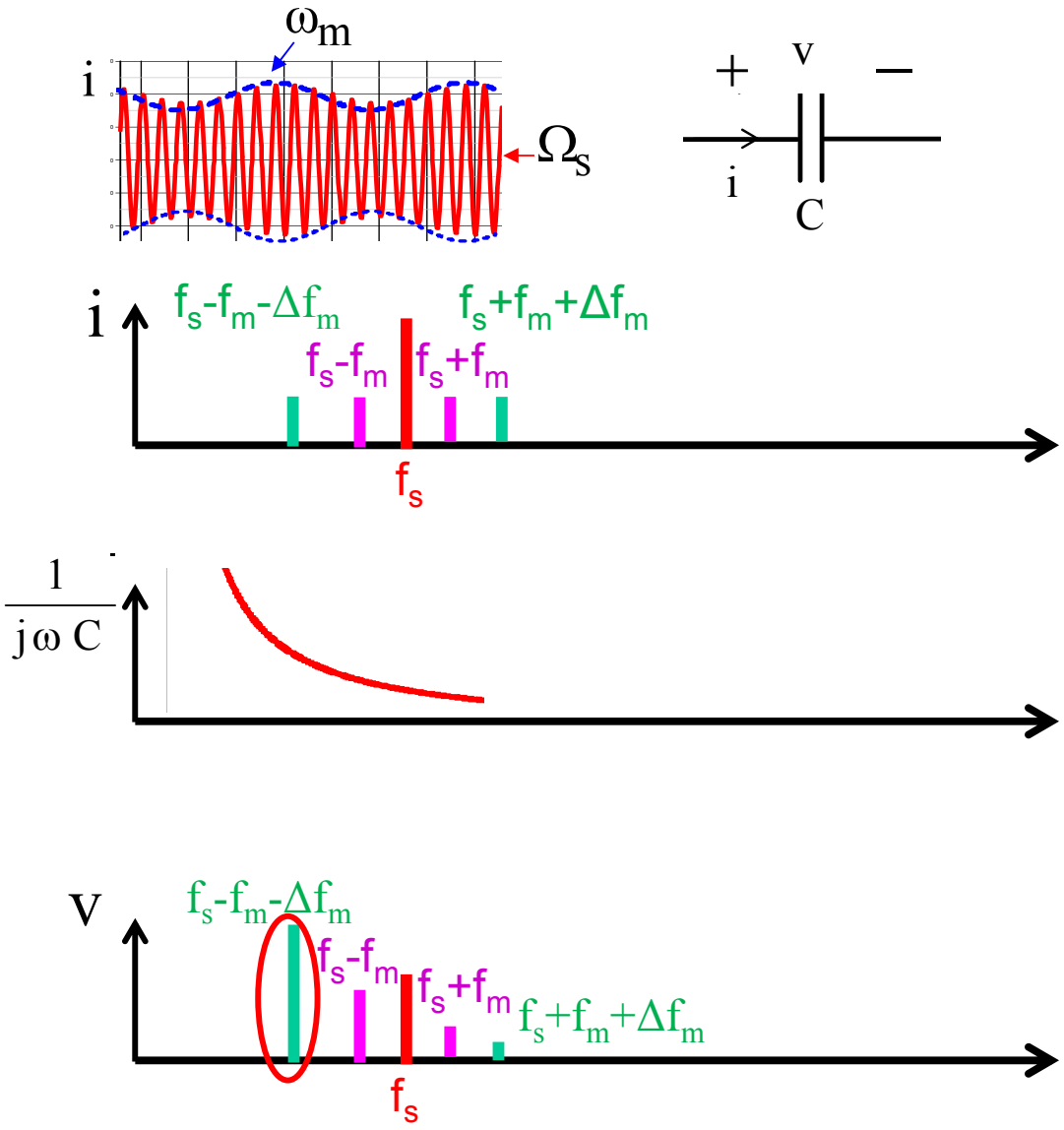
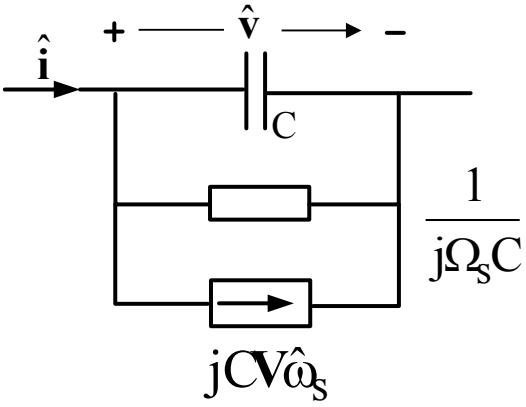
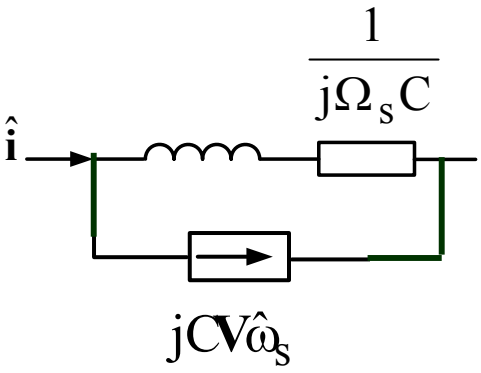


Figure 5. 10. Frequency spectrum interpretation of resonant capacitor branch.



(a)



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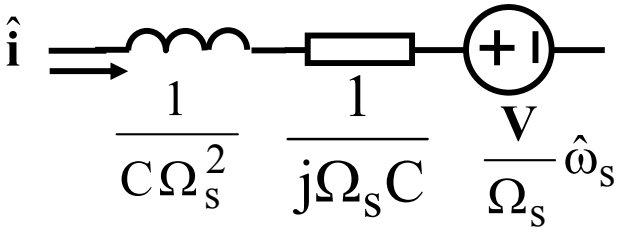
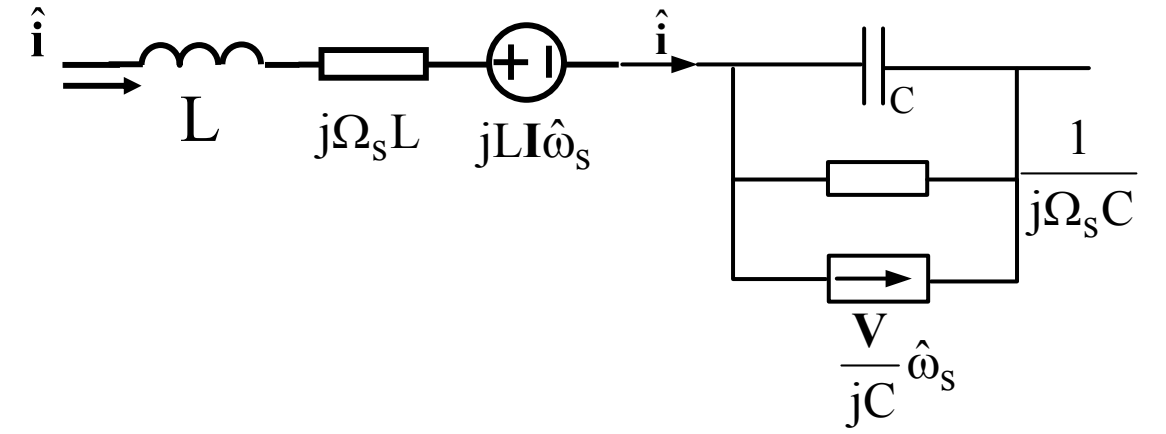


(c)

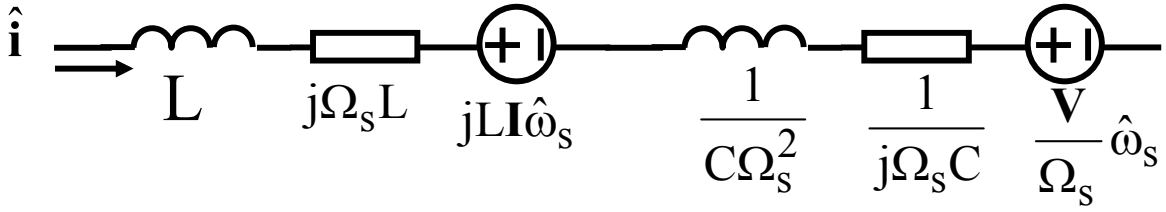
Figure 5. 11. (a) Original equivalent circuit model of resonant capacitor. (b) Equivalent circuit model under $\omega_m << \Omega_s$ using the result of Figure 5. 9. (c) Simplified equivalent circuit model using Thevenin's Theorem.

With the result shown in Figure 5. 11, the equivalent circuit model of resonant tank shown as Figure 5. 12 (a) can be simplified as shown in Figure 5. 12 (b) and (c). With respect to modulation frequency, the resonant tank always shows inductive behavior. The equivalent inductor of the resonant tank L_e, is determined by both L and C, as shown in the follows:

$$L_e = L + \frac{1}{C\Omega_s^2} = L(1 + \frac{\Omega_o^2}{\Omega_s^2}) \tag{5. 8}$$



(a)



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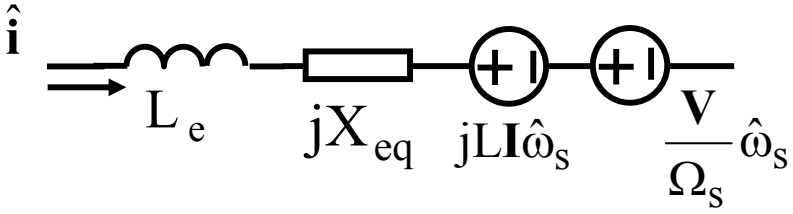


(c)

Figure 5. 12. (a) Original equivalent circuit model of resonant tank. (b) Equivalent circuit model under $\omega_m << \Omega_s$ using the result of Figure 5. 11. (c) Further simplified equivalent circuit model by combining inductor and complex impedance.

With simplified resonant tank, the original small signal model shown in Figure 5. 7 can be simplified, shown as Figure 5. 13. The resonant capacitor branch disappears as it behaves like an equivalent inductor with respect to modulation frequency. As there is still complex number which

is not suitable for simulation. Similar methodology can be adopted to separate the circuit into sine and cosine part, as shown in Figure 5. 14.

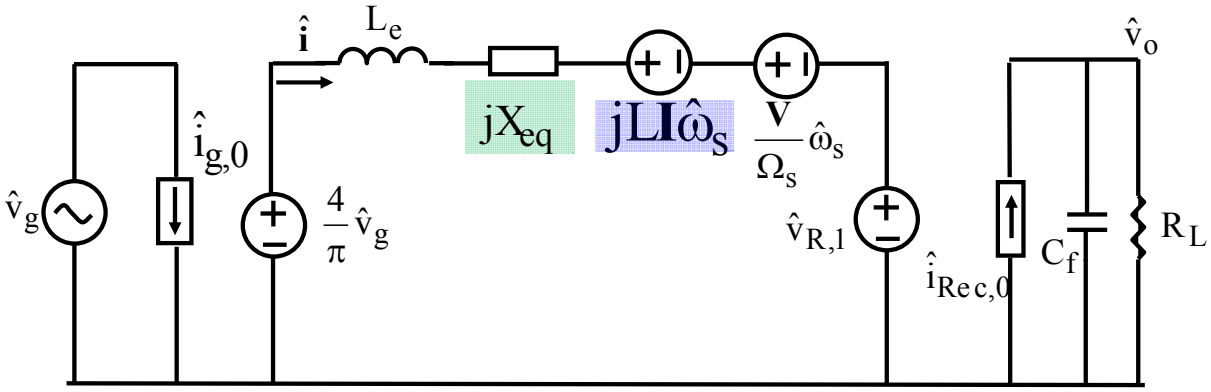


Figure 5. 13. Small-signal model of series resonant converter with simplified resonant tank.

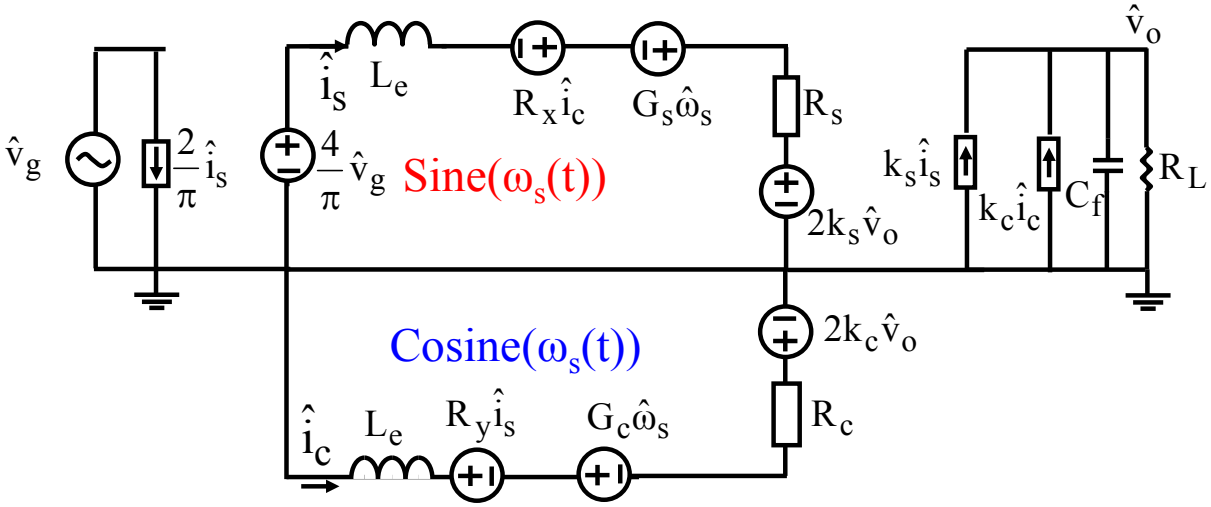


Figure 5. 14. Simplified third-order equivalent circuit model of series resonant converter.

Compare the original fifth order equivalent circuit model shown in Figure 5. 8 with the simplified third-order equivalent circuit model shown as Figure 5. 14, the input inverter model and output rectified model are same while the tank model is simplified to reduce the circuit order. The dynamic capacitors are transformed into equivalent inductor and therefore disappeared, which reduce the order of the model from 5th to 3rd order.

The expressions of R_s, R_c, k_s and k_c are shown in (5. 4) and the expressions of L_e, R_x, G_s, R_y and G_c are shown as follows:

$$L_e = L + \frac{1}{C\Omega_s^2}, R_x = \frac{X_{eq}^3}{X_{eq}^2 + R_{eq}^2}, R_y = X_{eq} \cdot \frac{X_{eq}^2 + 2R_{eq}^2}{X_{eq}^2 + R_{eq}^2}$$
$$G_s = LI_c + \frac{V_s}{\Omega_s}, G_c = LI_s - \frac{V_c}{\Omega_s} \quad (5.\ 9)$$

Where X_{eq} represents the tank impedance at switching frequency and R_{eq} represents the equivalent load resistance. The expressions of X_{eq} and R_{eq} are shown in (5. 4). I_c, V_s, I_s and V_c are steady state parameters and shown in (5. 3).

Figure 5. 15 shows the comparison of poles between the original fifth-order equivalent circuit model shown in Figure 5. 8 and simplified third-order equivalent circuit model shown in Figure 5. 14. The poles are derived numerically using matlab for control to output voltage transfer function with F_s=360kHz and F_o=300kHz. The blues poles are from the original model and red poles are from simplified model. Three blue poles are located within switching frequency while the other two are at frequency much higher than switching frequency. The two poles have very little influence in the region of interest which is below switching frequency and therefore can be neglected. The simplified model keeps the three low-frequency poles while neglecting two high frequency poles. As a result, the simplified model preserves accuracy of the original model and reduces the complexity of the original model.

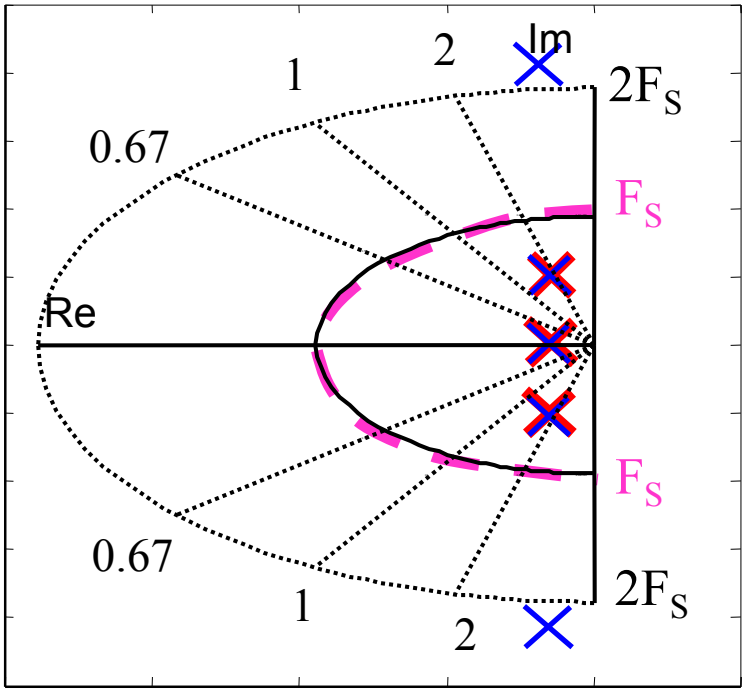


Figure 5. 15. Comparison of poles between original fifth order equivalent circuit model (blue) and simplified third-order equivalent circuit model (red) for control to output voltage transfer function with F_s=360kHz and F_o=300kHz.

5.3.2 Proposed non-coupled equivalent circuit model

Although the equivalent circuit model shown in Figure 5. 14 is third-order, there is still cross-coupling between the sine branch and cosine branch. It is worthwhile to pursue a non-coupled equivalent circuit model.

Case I: Special case @ $\Omega_s=\Omega_o$

When switching frequency is equal to resonant frequency, the steady-state tank impedance is zero. At this particular case, the expressions of L_e, R_x, G_s, R_y, R_s, k_s, and k_c are shown as follows:

$$L_e = 2L, R_x = 0, G_s = 0, R_y = 0$$
$$R_s = 0, k_s = \frac{2}{\pi}, k_c = 0 \quad (5.\ 10)$$

As R_x and k_c are zero, the effect of cosine branch to sine branch and output branch are zero which means the cosine branch is decoupled for this special case. Therefore, the equivalent circuit model shown in Figure 5. 14 can be simplified as follows:

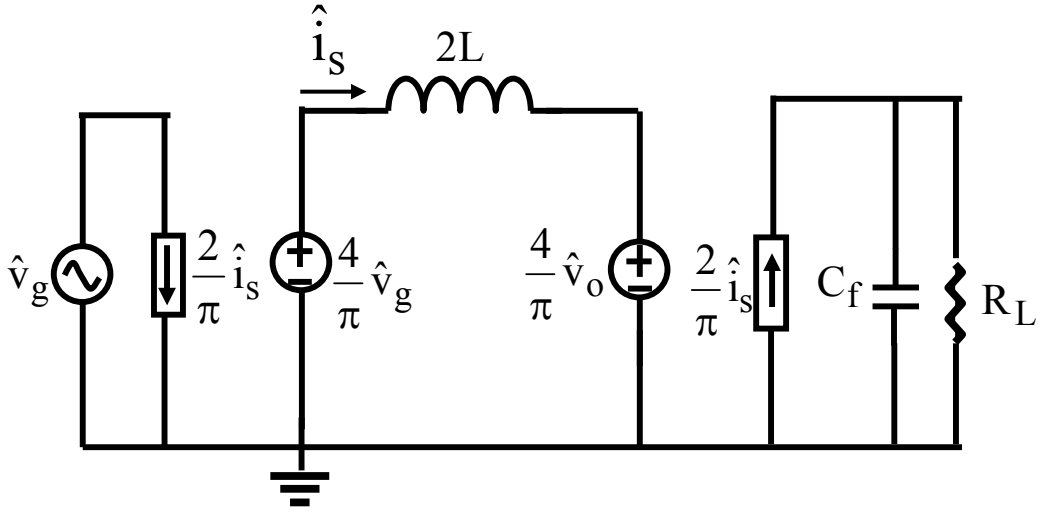


Figure 5. 16. Non-coupled equivalent circuit model @ $\Omega_s=\Omega_o$

Figure 5. 16 is a desired model as it is already de-coupled. It is clear that tank impedance in this case is 2L with respect to modulation frequency. One L is from resonant inductor, the other L is from resonant capacitor: as shown in Figure 5. 12 (c), the equivalent inductance value of the resonant capacitor is also L. As a result, the total inductance of the resonant tank is 2L.

For this special case, the circuit is only a second-order circuit. For example, the transfer function of input to output voltage can be solved as follows:

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)}=\frac{1}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}},\omega_1=\frac{2}{\pi}\frac{1}{\sqrt{LC_f}},Q_1=\frac{2}{\pi}\frac{R_L}{\sqrt{\frac{L}{C_f}}} \tag{5. 11}$$

The expression of the position and quality factor of the double pole are shown in (5. 11): the double pole is determined by resonance between 2L and the equivalent output capacitor while output load determines the quality factor. The double pole position is misunderstood in literature [E27] where it states that the double pole is located at the output filter corner frequency.

For control-to-output voltage transfer function, as G_s is very small (zero when switching frequency is right at resonant frequency), the gain is very small when switching frequency is very close to resonant frequency. This phenomenon will be discussed in section 5.4.

Case II: General case.

For general case, the superposition theorem is applied to derive a non-coupled equivalent circuit model. As shown in Figure 5. 14, the output current is affected by the input voltage perturbation, output voltage perturbation and switching frequency perturbation, as shown in the following:

$$\begin{aligned}&\hat{i}_{rec}(s) \approx G_{vg}(s)\hat{v}_g(s)+G_{vs}\hat{\omega}_s(s)+G_{vo}(s)\hat{v}_o(s)\\&G_{vg}=\frac{\hat{i}_{rec}(s)}{\hat{v}_g(s)}\Big|_{\hat{v}_o=0,\hat{\omega}_s=0}, G_{vs}=\frac{\hat{i}_{rec}(s)}{\hat{\omega}_s(s)}\Big|_{\hat{v}_g=0,\hat{v}_o=0}, G_{vo}=\frac{\hat{i}_{rec}(s)}{\hat{v}_o(s)}\Big|_{\hat{v}_g=0,\hat{\omega}_s=0}\end{aligned} \tag{5. 12}$$

G_{vg}, G_{vs} and G_{vo} are first derived separately using circuit techniques, then the total response of output current is obtained by adding the individual response. The detailed derivation process is shown in appendix. From output voltage point of view, the non-coupled equivalent circuit is shown as follows:

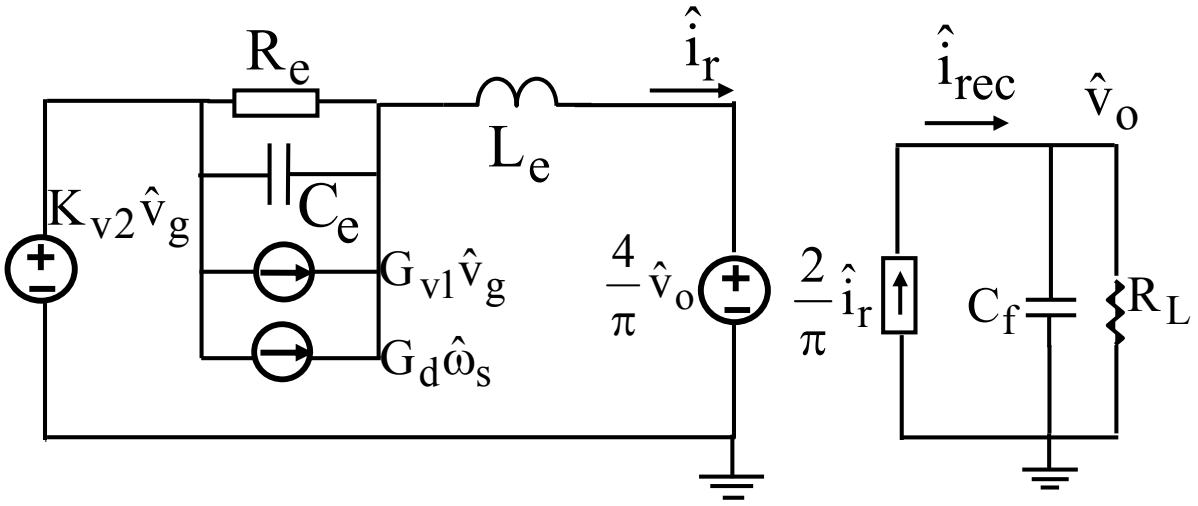


Figure 5. 17. Proposed non-coupled equivalent circuit model for general case.

The expressions of L_e, R_e, C_e, G_{v1}, K_{v2} and G_d are listed as follows:

$$\begin{aligned} &L_e = L(1+\frac{\Omega_o^2}{\Omega_s^2}), C_e = \frac{1}{L_e(\Omega_s-\Omega_o)^2}, R_e = \frac{L_e\left|X_{eq}\right|\left|\Omega_s-\Omega_o\right|}{R_{eq}} \\ &G_d = -\frac{4}{\pi}\frac{V_g}{\Omega_s\sqrt{R_{eq}{}^2+X_{eq}^2}}\frac{\Omega_s^2+\Omega_o^2}{\Omega_s^2-\Omega_o^2}, \\ &G_{v1} = \frac{2}{\pi}\frac{X_{eq}}{\sqrt{X_{eq}{}^2+R_{eq}^2}}, K_{v2} = \frac{4}{\pi}\frac{R_{eq}}{\sqrt{X_{eq}{}^2+R_{eq}^2}}, \\ &R_{eq} = \frac{8}{\pi^2}R_L, X_{eq} = \Omega_s L - \frac{1}{\Omega_s C} \end{aligned} \tag{5. 13}$$

For control-to-output voltage transfer function, Figure 5. 17 can be further simplified as Figure 5. 18:

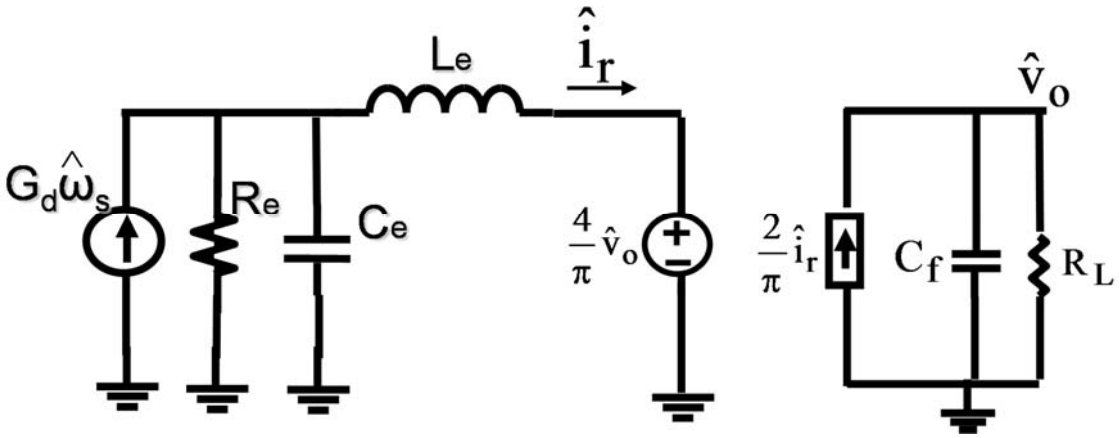
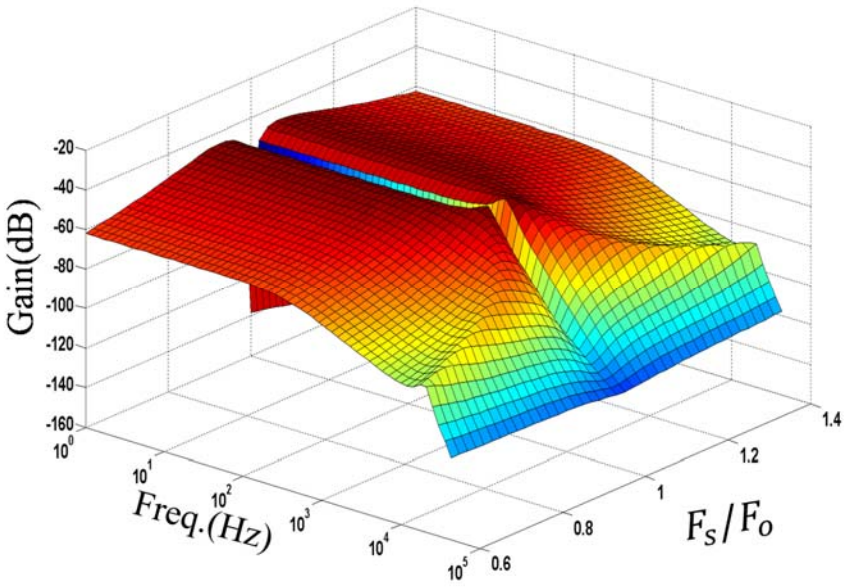


Figure 5. 18. Proposed non-coupled equivalent circuit model for control-to-output voltage transfer function.

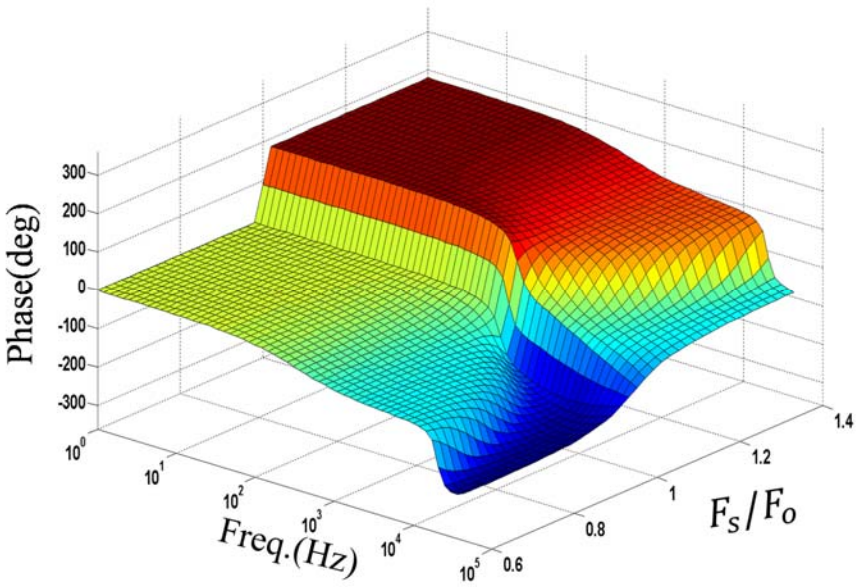
5.4 Discussion and Prediction of Proposed Equivalent Circuit Model

5.4.1 DC gain and beat frequency dynamics

With the help of Figure 5. 18, the 3D-plot of control to output voltage transfer function can be plotted, as shown in Figure 5. 19:



(a)



(b)

Figure 5. 19. 3D Bode plot of control-to-output voltage transfer function (a) Gain plot. (b) Phase plot.

The DC gain and poles can be explained clearly using the proposed non-coupled equivalent circuit model shown in Figure 5. 18.

From Figure 5. 18, the DC gain of the control-to-output voltage transfer function can be derived easily as shown in the follows:

$$G_{DC} = G_d \cdot R_e \| R_{eq} = \frac{V_g X_{eq} R_{eq} \left(X_{eq} \Omega_s + 2L\Omega_s^{\,2} \right)}{\Omega_s^{\,2} \sqrt{X_{eq}^{\,2} + R_{eq}^{\,2}} \left(X_{eq}^{\,2} + R_{eq}^{\,2} \right)} \tag{5. 14}$$

The DC gain can be related with the slope of the voltage conversion ratio curve by the following relations:

$$G_{DC} = \frac{\partial V_o}{\partial \Omega_s} = \frac{V_g}{\Omega_o} \frac{\partial M}{\partial \Omega_s} \tag{5. 15}$$

As shown in Figure 5. 20, When $\Omega_s=\Omega_o$ shown as the black point, the slope is zero as the curve is at maximum point, therefore, DC gain is zero which explains the canyon region in 3D graph in Figure 5. 19. When $\Omega_s<\Omega_o$ shown as the blue point, the slope is positive. When $\Omega_s>\Omega_o$ shown as the green point, the slope is negative. This explains the phenomenon observed in 3D plots in Figure 5. 19, where 180deg phase difference is shown for $\Omega_s<\Omega_o$ and $\Omega_s>\Omega_o$ cases.

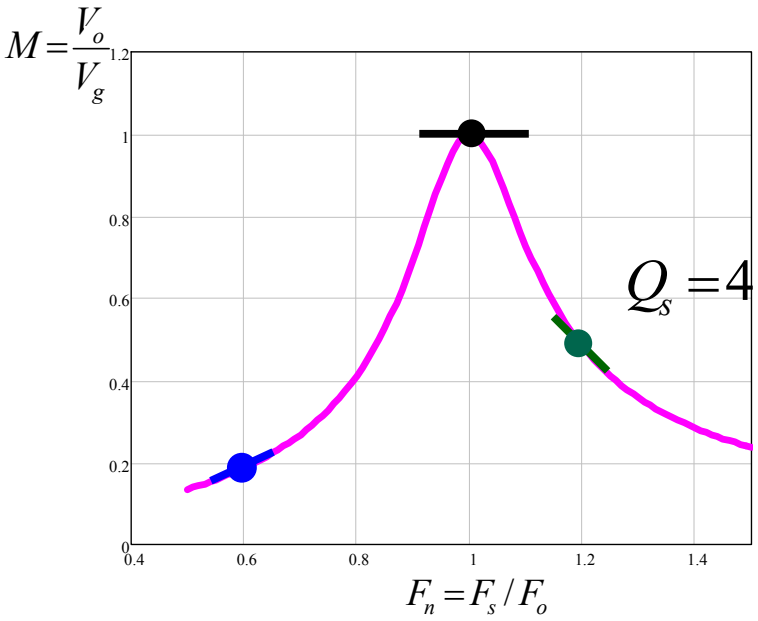


Figure 5. 20. Slope of voltage conversion ratio Vs. normalized switching frequency.

The beat frequency dynamic performance of the circuit can also be well explained by the equivalent circuit. The components R_e, C_e and L_e represent beat frequency dynamics. The equivalent inductor L_e is probably resonant with the equivalent output capacitor or the equivalent capacitor C_e, depending on the value of R_e.

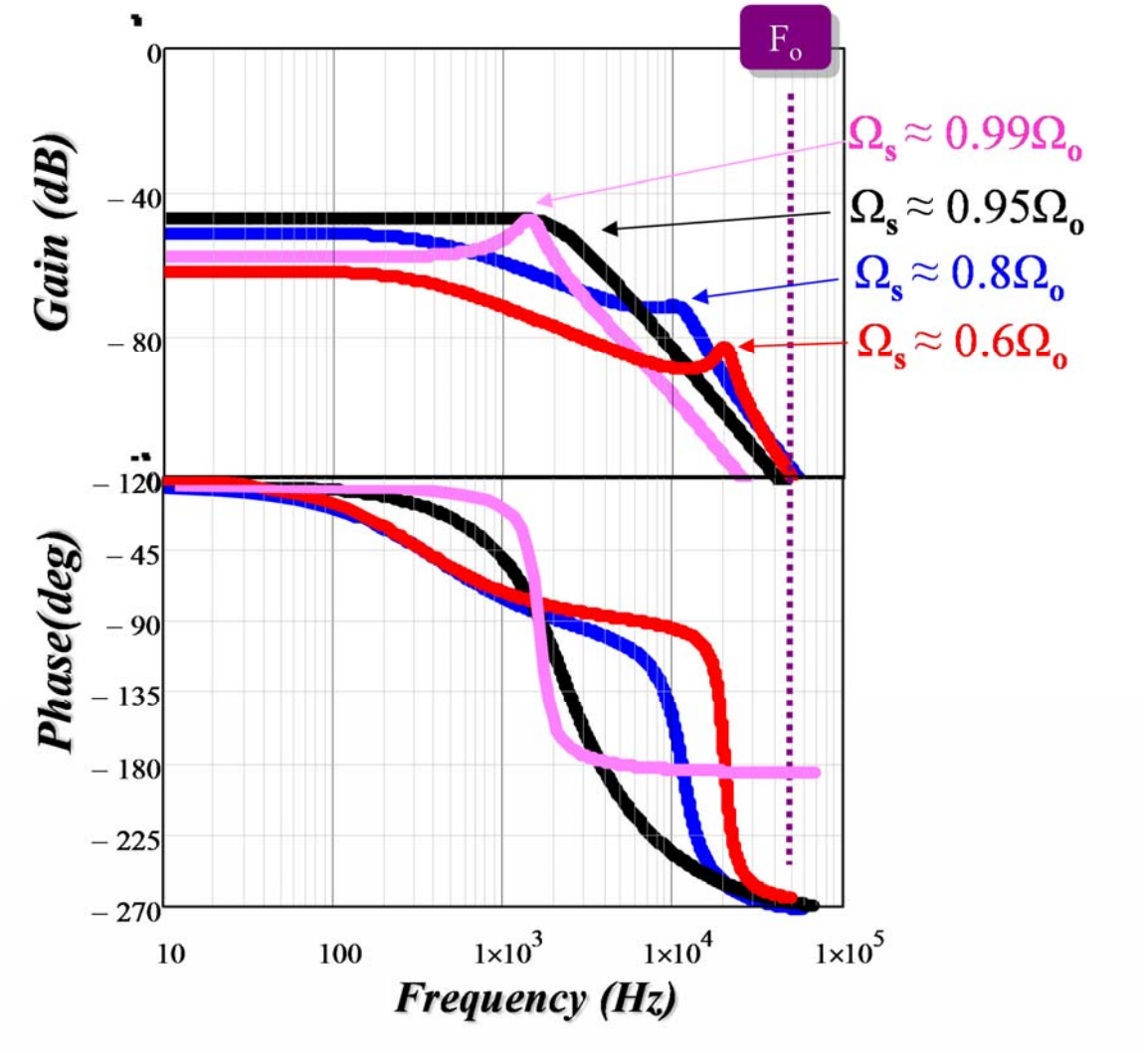
When switching frequency F_s is far away from resonant frequency F_o, R_e is large. L_e is resonant with C_e, which forms the beat frequency double pole. The output capacitor and load resistor forms a single pole on the load side. In this case, the double pole position its quality factor can be easily derived from Figure 5. 18 as follows:

$$\omega_p = \left|\Omega_s - \Omega_o\right|, Q_p = \frac{\left|\Omega_s L - \frac{1}{\Omega_s C}\right|}{R_{eq}} \tag{5. 16}$$

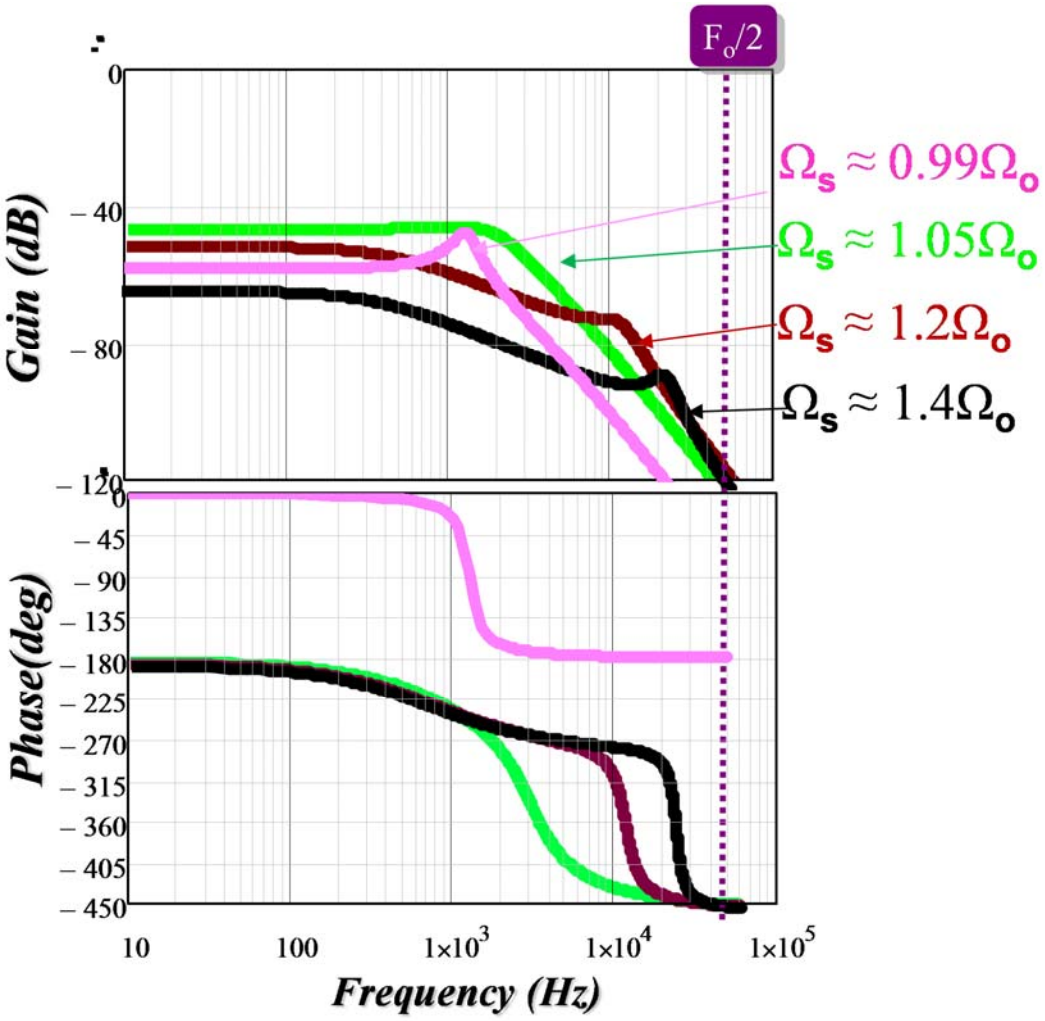
When switching frequency F_s is very close to resonant frequency F_o, R_e is small. The double pole caused by L_e and C_e will be damped out and split, one moves to high frequency and the other one moves to low frequency. This low frequency pole will combine with low pass filter pole and forms a double pole. In other words, L_e is resonant with output capacitor C_f and load resistance determines the damping factor of this double pole. In this case, the double pole position its quality factor are shown as (5. 11).

The following illustration example is provided to explain the beat frequency dynamics. When $\Omega_s=0.6\Omega_o$, $R_e=360\Omega$ is very large, L_e resonates with C_e. F_{beat}=20kHz, Q_{beat}=5.5. The 2D Bode plot is shown as the red curve in Figure 5. 21 (a), there is a beat frequency double pole at 20kHz and a single pole at low frequency caused by the output filter. When $\Omega_s=0.8\Omega_o$, $R_e=64\Omega$ is still very large, L_e is resonate with C_e. F_{beat}=10kHz, Q_{beat}=2.3. Shown as the blue curve in Figure 5. 21 (a), the beat frequency moves to 10kHz while the peaking reduces. When $\Omega_s=0.95\Omega_o$, $R_e=3\Omega$ is smaller, F_{beat}=2.5kHz, Q_{beat}=0.5. The beat frequency double pole is about to split. This means that L_e is not

only resonate with C_e, but also with output capacitor C_f. Shown as the black curve in Figure 5. 21 (a), the beat frequency double pole is about to split and no peaking is observed. When $\Omega_s=0.99\Omega_o$, $R_e=0.1\Omega$ is very small. The beat frequency double pole is split. L_e is resonant resonate with output capacitor C_f. Shown as the pink curve in Figure 5. 21 (a), the double pole formed by L_e and equivalent output capacitor, instead of beat frequency double pole, is observed. The similar scenario is observed for region $\Omega_s \geq \Omega_o$ shown in Figure 5. 21 (b): For the green curve, $\Omega_s=1.05\Omega_o$, $R_e=3\Omega$, $F_{beat}=2.5kHz$, $Q_{beat}=0.5$. L_e is resonant with both C_e and C_f. For red curve, $\Omega_s=1.2\Omega_o$, $R_e=43\Omega$, $F_{beat}=10kHz$, $Q_{beat}=1.8$. Beat frequency double pole is shown again. L_e is resonant only with C_e. For black curve, $\Omega_s=1.4\Omega_o$, $R_e=149\Omega$, $F_{beat}=20kHz$, $Q_{beat}=3.5$. As switching frequency is farther away, beat frequency double pole is more obvious.


F_o
Ω_s ≈ 0.99Ω_o
Ω_s ≈ 0.95Ω_o
Ω_s ≈ 0.8Ω_o
Ω_s ≈ 0.6Ω_o
Gain (dB)
0
– 40
– 80
– 120
Phase(deg)
– 45
– 90
– 135
– 180
– 225
– 270
10
100
1×10^3
1×10^4
1×10^5
Frequency (Hz)

(a)



(b)

Figure 5. 21. Illustration example of beat frequency dynamics. (a) For region $\Omega_s \leq \Omega_o$. (b). For region $\Omega_s \geq \Omega_o$.

In sum, the proposed equivalent circuit model can successfully explain the beat frequency dynamics: When switching frequency is far away from resonant frequency, beat frequency double pole is obvious, and the circuit is third-order; When switching frequency is close to resonant frequency, beat frequency will split and the circuit will become second-order. The quality factor of beat frequency is related with quality factor of series resonant converter as follows:

$$Q_{beat} = \frac{\pi^2}{8} \frac{\left|\Omega_s^2 - \Omega_o^2\right|}{\Omega_s \Omega_o} Q_s \tag{5. 17}$$

The boundary of beat frequency double pole can be plotted as shown in the following graph. Within the shaded area, the beat frequency double pole splits. Outside of the shaded area, the beat frequency double pole exists. For example, For Q_s=1, when $0.82F_o \leq F_s \leq 1.22\Omega_o$, the beat frequency double pole does not exist. When $F_s \leq 0.82F_o$ or $F_s \geq 1.22F_o$, beat frequency double pole is observable. From Figure 5. 22, for larger Q_s, the region where beat frequency double pole dose not exist is narrower. This is reasonable as physically larger Q_s means the band pass filter is more ideal, which means that the interaction between resonant frequency and switching frequency is stronger. As a result, beat frequency double pole is more likely to occur.

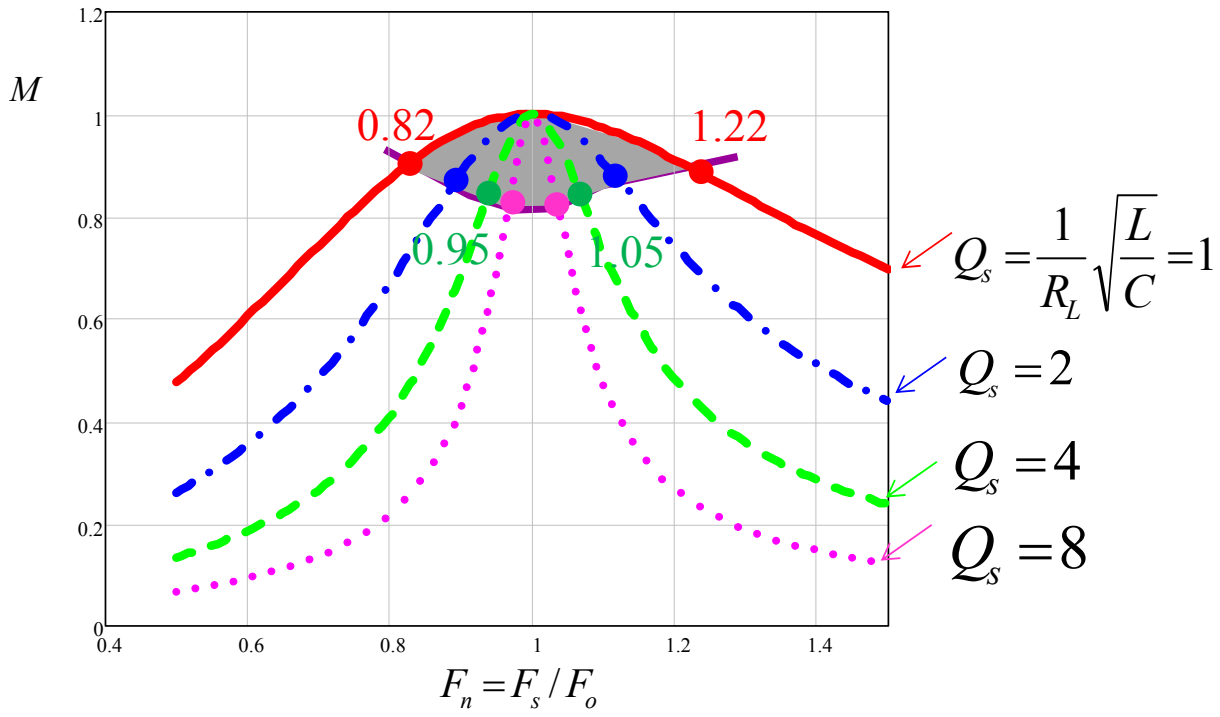


Figure 5. 22. Boundary for existence of beat frequency double poles.

5.4.2 Analytical expression of transfer functions

All the analytical transfer functions can be derived from Figure 5. 17 and Figure 5. 14. The analytical transfer functions are provided in Table 5. 1 for easy reference. These transfer functions are very helpful in designing the outer feedback compensator. The transfer functions are generally third-order and can be reduced to second order when switching frequency is very close to resonant frequency.

Table 5. 1 Analytical transfer functions of series resonant converter

$\frac{\hat{v}_o(s)}{\hat{\omega}_s(s)} = K_d \frac{1}{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}$ $K_d = -\frac{V_g}{\Omega_s} \frac{R_{eq}}{\sqrt{R_{eq}^{\ 2} + X_{eq}^2}} \frac{\Omega_s^2 + \Omega_o^2}{\Omega_s^2 - \Omega_o^2} X_{eq}^2, L_e = L(1 + \frac{\Omega_o^2}{\Omega_s^2})$ $R_{eq} = \frac{8}{\pi^2} R_L, X_{eq} = \Omega_s L - \frac{1}{\Omega_s C}$	(5. 18)
$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{R_{eq}}{\sqrt{R_{eq}^{\ 2} + X_{eq}^2}} \frac{R_{eq}^{\ 2} + X_{eq}^2 + L_e R_{eq} s}{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}$	(5. 19)
$Z_o(s) = R_L \frac{s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2}{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}$	(5. 20)
$Z_{in}(s) = \frac{\pi^2}{8} \frac{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}{s^2 L_e C_f R_L + sL_e + sC_f R_L \frac{R_{eq}^{\ 3}}{R_{eq}^{\ 2} + X_{eq}^2} + R_{eq}}$	(5. 21)

5.5 Simulation and Experimental Verifications

The SIMPLIS simulation tool is used to verify the small-signal analysis. Circuit parameters are shown as follows: V_g=400V, L=197uH, C=51nF, F_o=50.2kHz, C_f =32μF, R_L=15.5Ω, the corresponding Q_s=4. The comparison results of the equivalent circuit model and simulation results for F_s=0.9F_o, F_s=1.01F_o and F_s=1.2F_o are shown in Figure 5. 23, Figure 5. 24, and Figure 5. 25 respectively. All the transfer functions match very well.

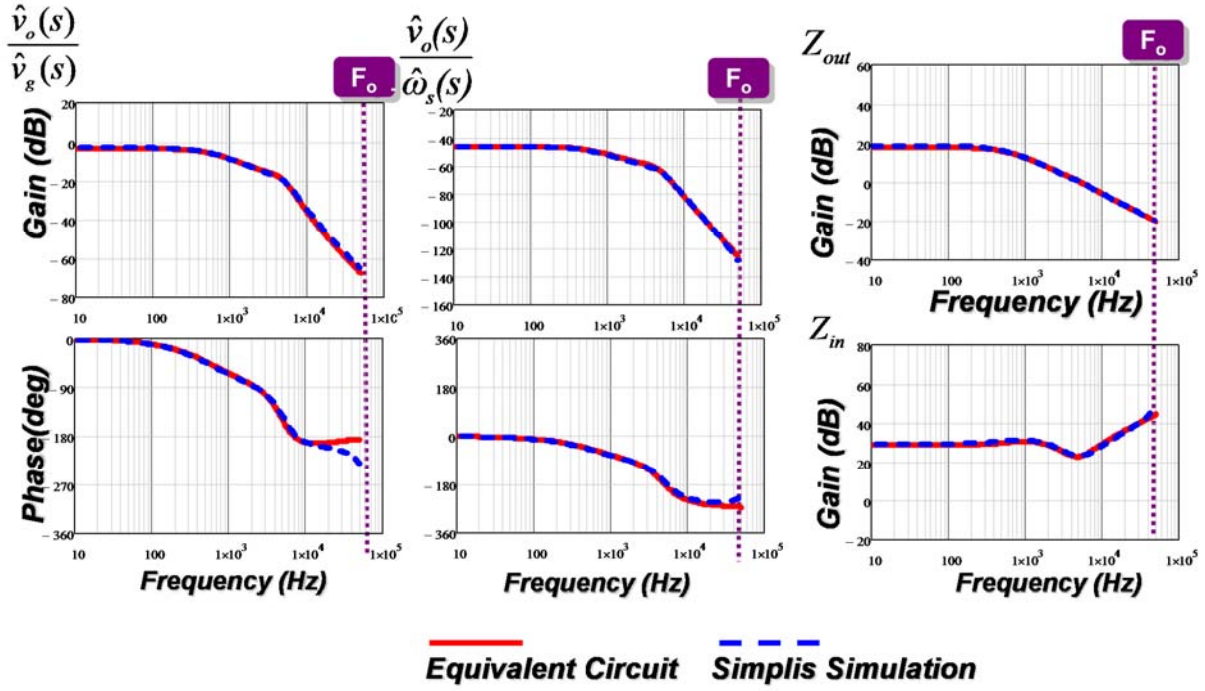


Figure 5. 23. Simplis verification of small-signal equivalent circuit model for F_s=0.9F_o.

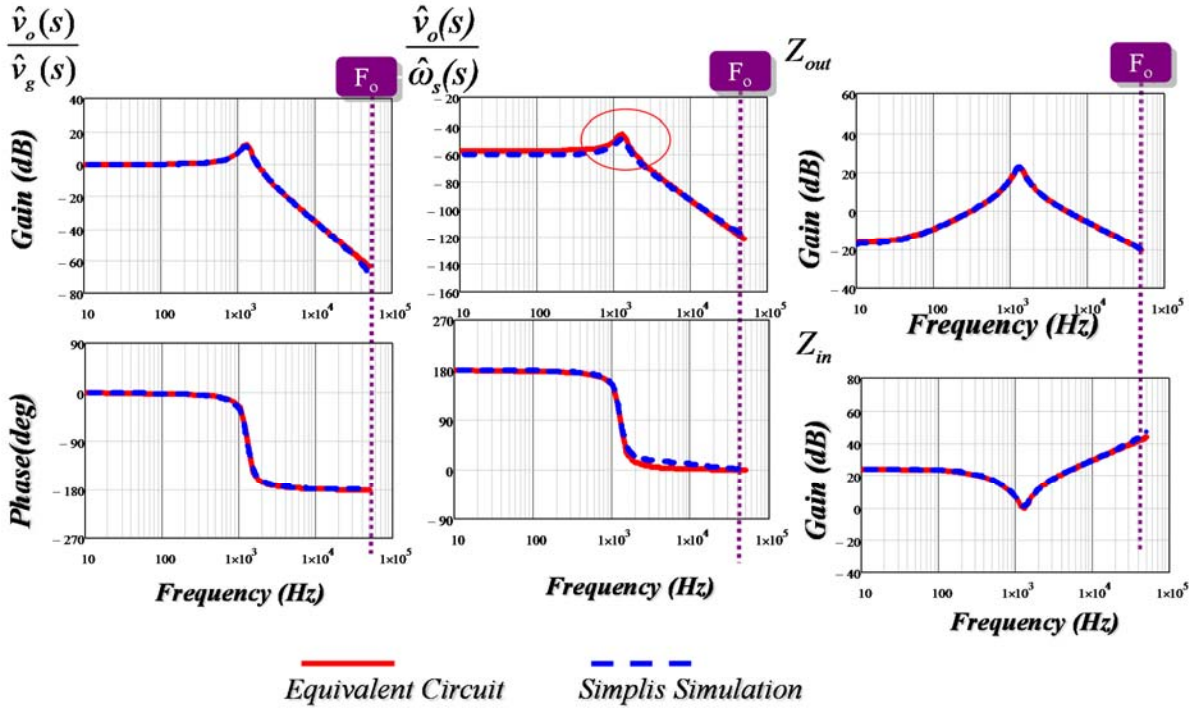


Figure 5. 24. Simplis verification of small-signal equivalent circuit model for $F_s=1.01F_o$.

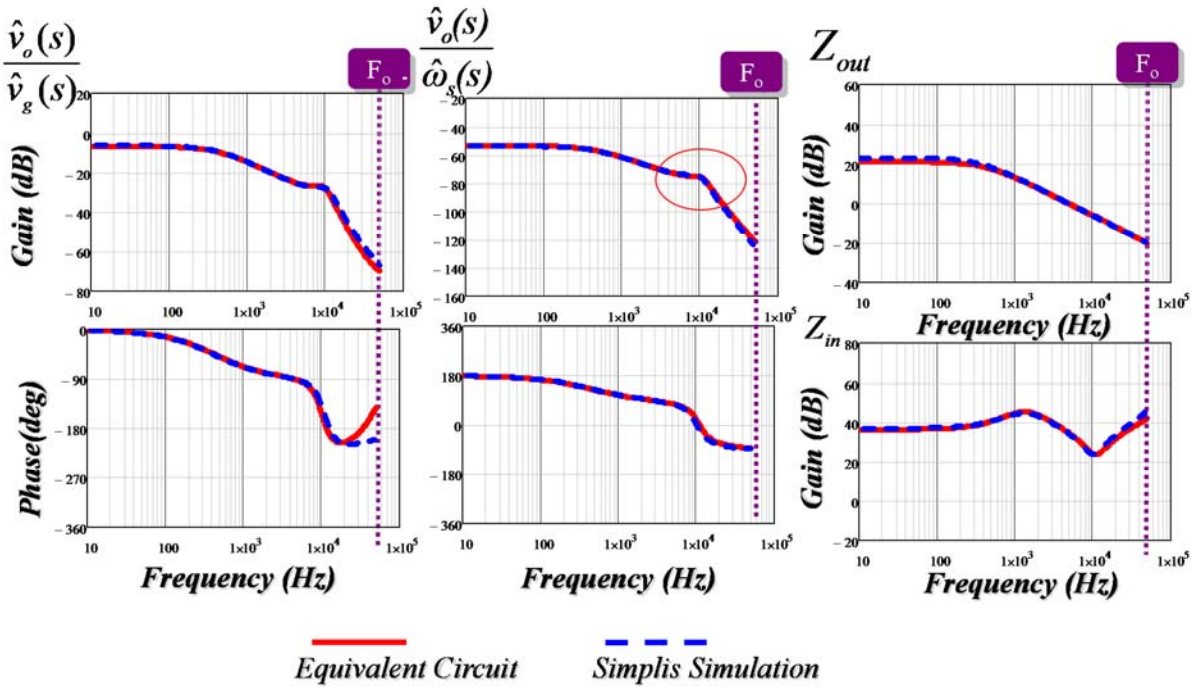


Figure 5. 25. Simplis verification of small-signal equivalent circuit model for $F_s=1.2F_o$.

The experimental verification are shown as Figure 5. 26--Figure 5. 29. The experimental data for Figure 5. 26 and Figure 5. 27 are taken from [E27] and the circuit parameters are: L=22.5uH, C=6.56nF, F_o=414kHz, C_f =16.75μF, r_c=212mΩ. Compared with E.Yang's model and also experimental data, the control-to-output voltage predictions from equivalent circuit are very good, although a little worse than E.Yang's model. This is reasonable as some accuracy especially at high frequency is lost due to the approximation of the simplified equivalent circuit model. Nonetheless, the model still gains adequate accuracy from practical design point of view. The beat frequency double pole is shown in Figure 5. 26, where switching frequency is far away from resonant frequency, while it disappear in Figure 5. 27, where the two frequencies are close. This agrees with the analysis from our equivalent circuit model. The experimental data for Figure 5. 28 and Figure 5. 29 are taken from [E28] and the circuit parameters: L=197uH, C=51nF, F_o=50.2kHz, C_f =32μF. The input to output voltage transfer function and input impedance are also shown very accurate.

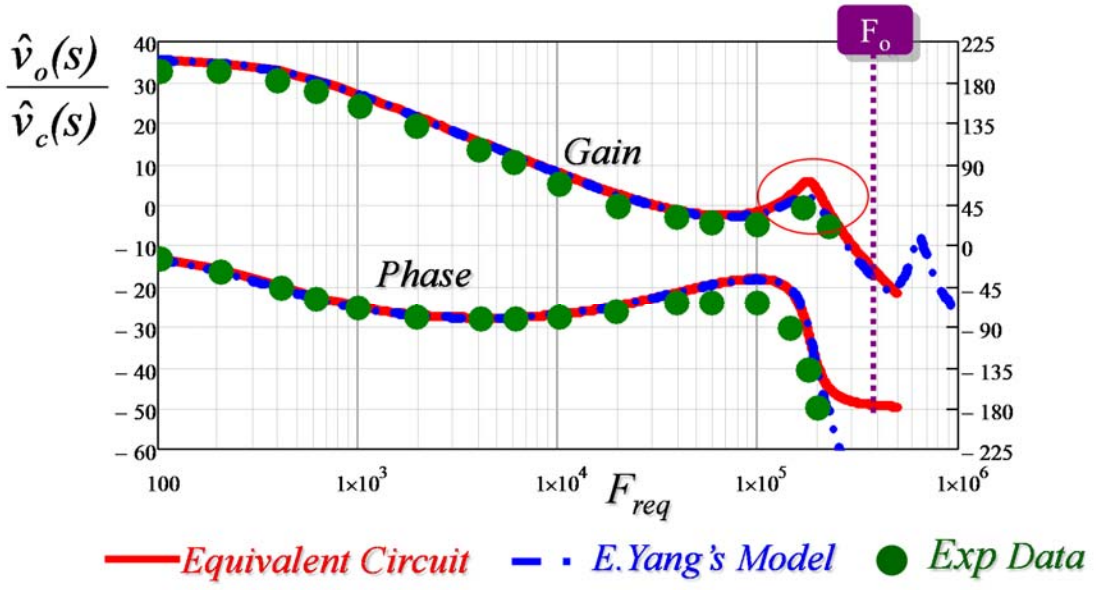


Figure 5. 26. Experimental verification of control-to-output transfer function for F_s=0.56F_o and Q_s=2.2. The experimental data are taken from [E27].

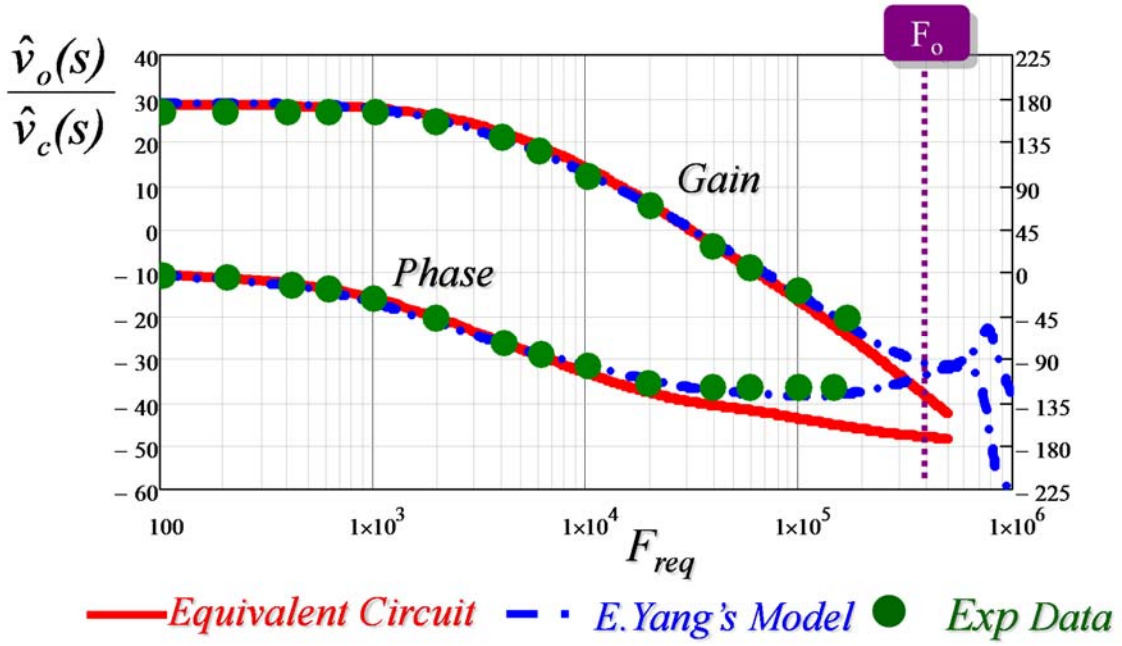


Figure 5. 27. Experimental verification of control-to-output transfer function for F_s=0.905F_o and Q_s=1.5. The experimental data are taken from [E27].

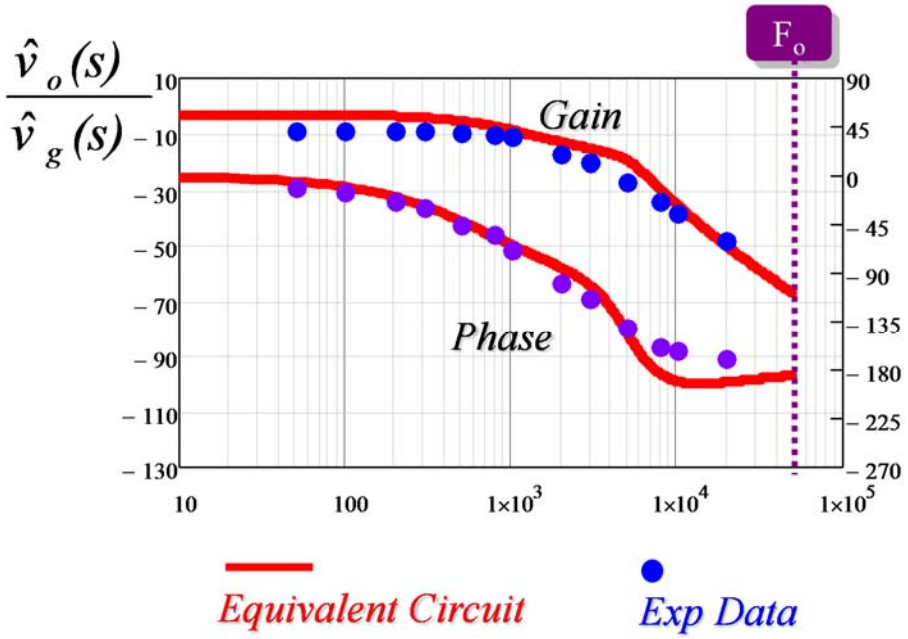


Figure 5. 28. Experimental verification of input-to-output transfer function for F_s=0.9F_o and Q_s=4. The experimental data are taken from [E28].

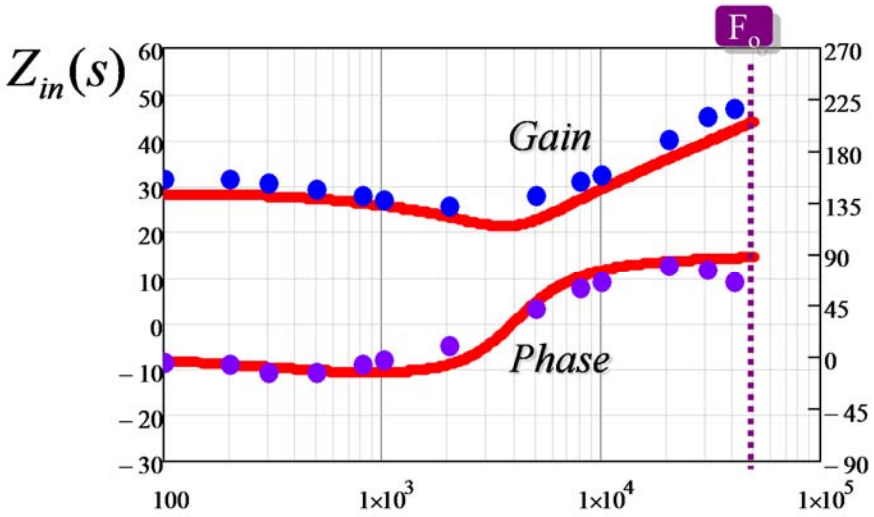


Figure 5. 29. Experimental verification of input impedance transfer function for $F_s=0.92F_o$ and $Q_s=4$. The experimental data are taken from [E28][E13] .

5.6 Summary

This chapter proposes a methodology to simplify the fifth-order equivalent circuit of series resonant converter to a third-order equivalent circuit. The result shows that with the coupling effect, the behavior of the resonant capacitor is equivalent to an inductor, with the inductance value determined by the capacitance. A simple non-coupled equivalent circuit model is proposed which considers the coupling effect by adding an equivalent R_e-C_e branch. Proposed equivalent circuit model can be used to explain the beat frequency dynamics: when switching frequency is far away from resonant frequency, beat frequency will occur; when the two frequencies are close, beat frequency will disappear and another double pole which is determined by equivalent inductor and output capacitor will be formed. For the first time, analytical solutions are provided for all the transfer functions which are very helpful for feedback design. Simulation and experimental results verify that the equivalent circuit model can well predict the dynamic behavior when switching frequency is below, close to or above resonant frequency.

Chapter 6. Small-signal Equivalent Circuit Model of LLC Resonant Converter

6.1 Introduction

LLC resonant converter is the most popular resonant converter for front-end DC-DC converters used in distributed power systems in telecom, computer and network applications [F1]-[F2]. Besides, they are also widely adopted in other applications, such as LCD, LED and plasma display in TV and flat panels [F3]-[F6]; iron implanter arc power supply[F7]; solar array simulator in photovoltaic application [F8]; fuel cell applications [F9],and so on. A lot of commercial IC controllers are available to support the design of LLC converter [F10]-[F16]. As discussed in 1.2.3, available small-signal models published in literatures include extended describing function method [F23]-[F26], approach based on communication theory [F27], sampled-data modeling approach [F28], analysis based on Simplis simulation [F29] or bench measurement results [F30]. All of the above models use numerical solutions instead of analytical solutions. As a result, no simple equivalent circuit model is available and no analytical expressions of transfer functions are presented. This chapter tries to extend the simple equivalent circuit model shown in Chapter V to LLC resonant converters. The equivalent circuit model can serve as a useful design tool for feedback design. A third-order equivalent circuit model of LLC will be derived and analytical expressions for all transfer functions will be presented when switching frequencies are above, close to and below resonant frequency.

6.2 Equivalent Circuit Model of LLC Resonant Converter

For LLC resonant converter, one major advantage is its ZVS capability for zero to full load range. Generally speaking, ZVS is preferred for applications using MOSFET. For SRC, ZVS can only be achieved when switching frequency is above the resonant frequency. However, for LLC, due to the effect of L_m, ZVS can also be achieved when switching frequency is below the series resonant frequency F_o [F1]. From resonance point of view, the resonant tank is different when comparing $F_s \geq F_o$ with $F_s \leq F_o$: For $F_s \geq F_o$, only Lr resonates with Cr and Lm is clamped by the output voltage. For $F_s < F_o$, there is some time period that L_m also participates in resonance. Due to different resonant behavior, the small-signal models are developed for each case, as follows:

6.2.1 Equivalent circuit model of LLC for $F_s \geq F_o$

Figure 6. 1 shows steady-state waveforms when $F_s=1.4F_o$ and Figure 6. 2 shows the operating modes at different time periods. Obviously, in this case, LLC behaves like SRC. The magnetizing inductor, L_m, is either clamped by V_o or $-V_o$ and never participates in resonance. From resonant tank point of view, the equivalent circuit is shown in Figure 6. 3.

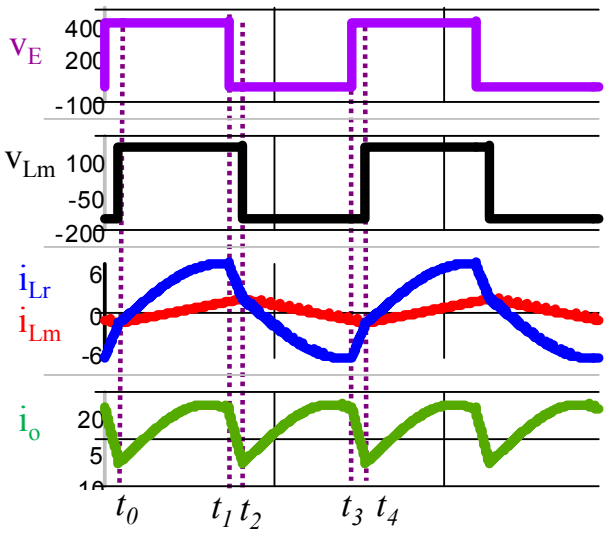


Figure 6. 1 Steady-state waveforms for Fs=1.4F_o.

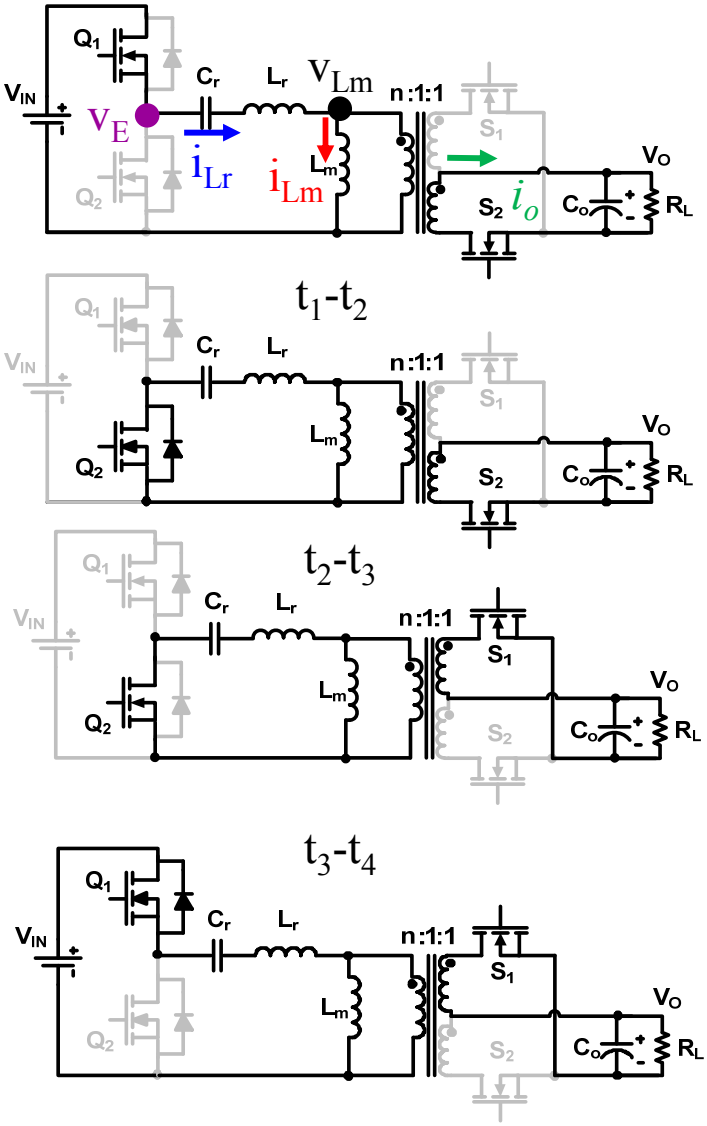
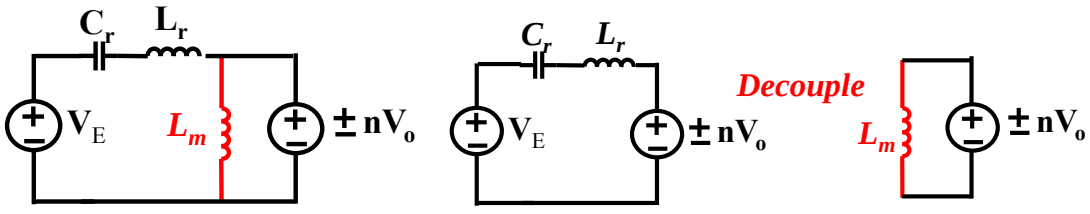


Figure 6. 2. Operating modes of LLC resonant converter for Fs ≥ Fo.



(a) (b)

Figure 6. 3 Equivalent circuit of resonant tank for Fs ≥ Fo. (a) coupled form (b) decoupled form.

Although L_m does not participates in resonance in this case, L_m has some effect on the modulation model as it is in parallel with the equivalent output load and shunts a certain amount of current, as shown in Figure 6. 4. Due to frequency modulation and the band pass filter characteristic of resonant tank, the waveform of magnetizing inductor current also contains modulation frequency as well as switching frequency, as shown in Figure 6. 5. The switching frequency component is shown as the red triangular carrier frequency while the modulation frequency is shown in the blue envelop.

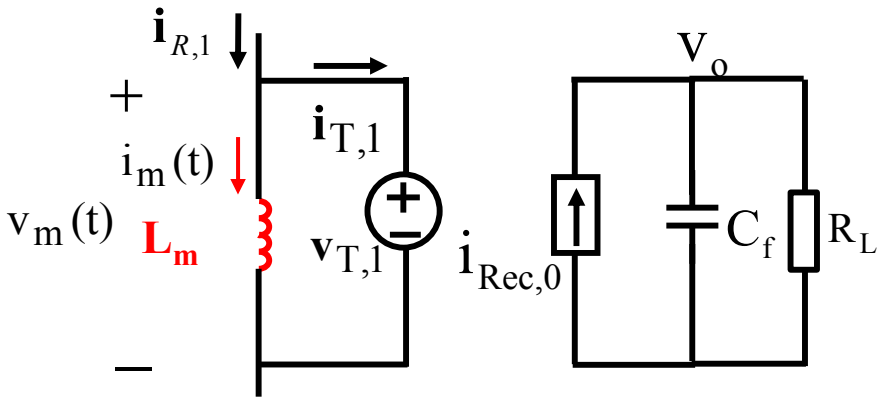


Figure 6. 4 The relation of L_m, rectifier and output load for Fs ≥ Fo.

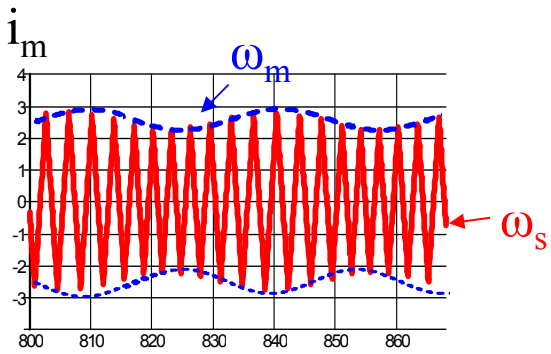
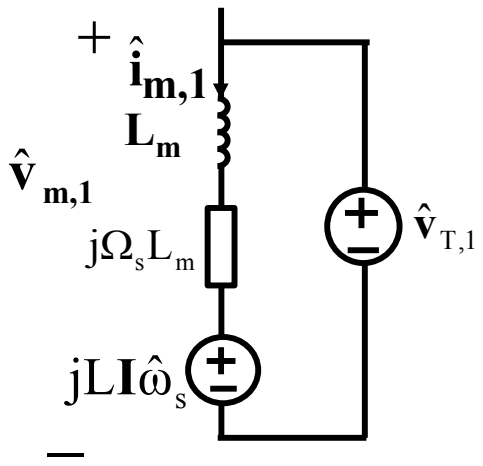


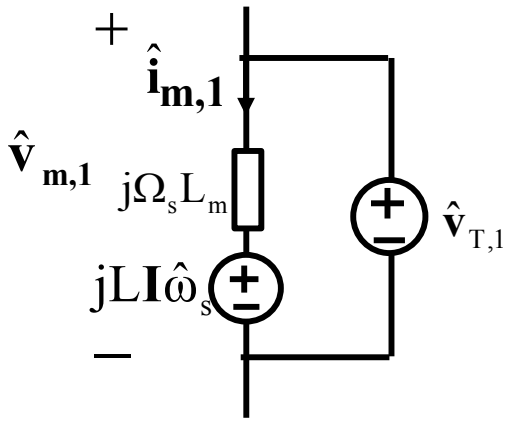
Figure 6. 5. Typical waveform of magnetizing inductor current under modulation for Fs ≥ Fo.

To model the magnetizing inductor, similar as the model of resonant inductor, fundamental approximation is used, i.e. only the fundamental of the triangular waveform of switching frequency is considered and the harmonics are neglected. Following the similar methodology as resonant

inductor, the small-singal model of magnetizing inductor is derived as shown in Figure 6. 6 (a). For low frequency modulation $\omega_m << \Omega_s$, the voltage across the inductor L_m is much smaller than the voltage across the complex impedance $j\Omega_s L_m$, therefore, it can be neglected and leads to the simplified small-signal model, shown in Figure 6. 6 (b). There is one complex impedance due to the effect of switching frequency and one complex voltage source due to perturbation of switching frequency. Note that, the dynamic element L_m does not show in the small signal model, this is reasonable as in this case, L_m is clamped by output voltage and its current is not a state variable anymore.



(a)



(b)

Figure 6. 6. Small-signal model of magnetizing inductor L_m for $F_s \geq F_o$. (a) Original small-signal model (b) Simplified small-signal model.

The model of inverter, rectifier, resonant inductor and resonant capacitor can be derived following the same methodology as SRC shown in Section 5.2. The small-signal model of LLC resonant converter for $F_s \geq F_o$ is shown as Figure 6. 7. Note that since half-bridge inverter is used in LLC resonant converter, compared with the full-bridge inverter model shown in Figure 5. 3, the magnitude of the input current source and output voltage source is reduced to half.

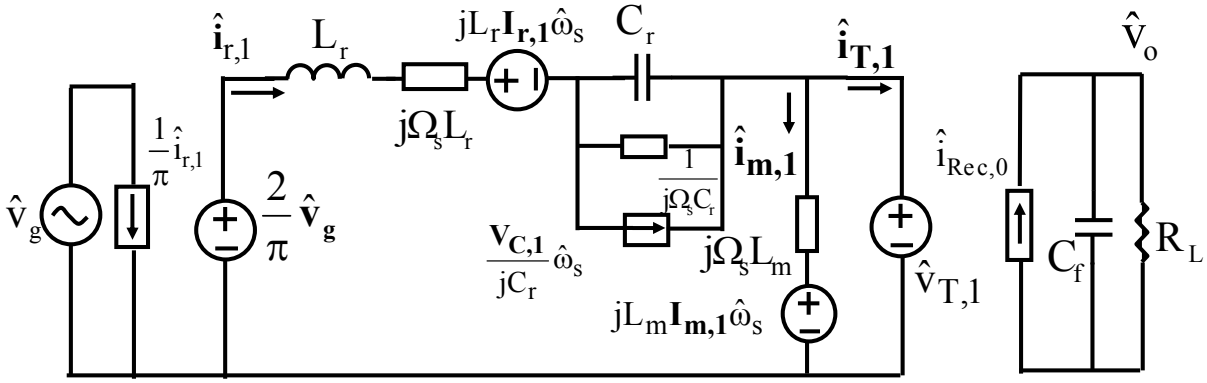


Figure 6. 7. Small-signal model of LLC for $F_s \geq F_o$.

The steady-state model can be derived from Figure 6. 7 when there is no perturbation signal, as shown in Figure 6. 8.

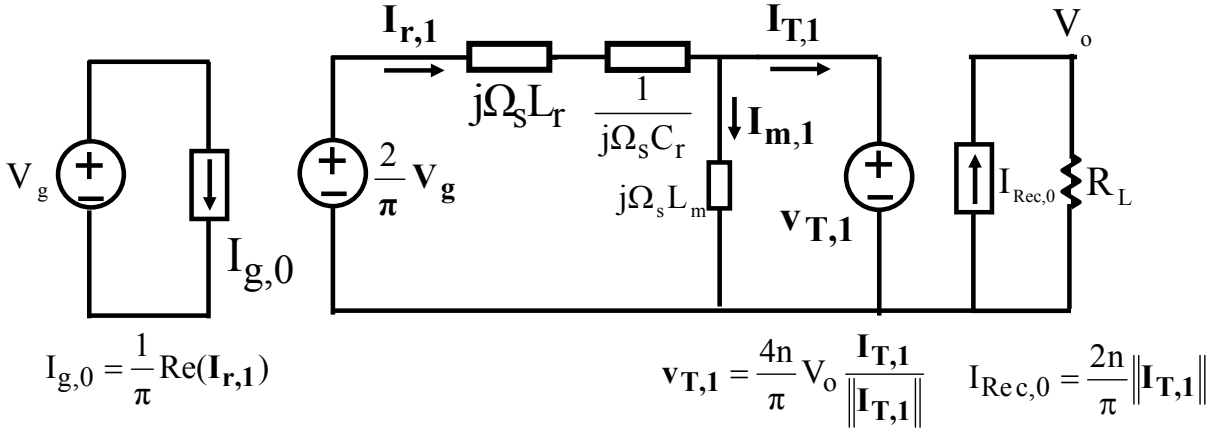


Figure 6. 8. Steady-state model of LLC for $F_s \geq F_o$.

The voltage conversion ratio can be derived from Figure 6. 8, shown as (6. 1):

$$M = \frac{2nV_o}{V_g} = \left\| \frac{j\omega_n L_n}{j\omega_n\left(L_n + 1 - \frac{1}{\omega_n^2}\right) + \frac{\pi^2}{8}Q(1-\omega_n^2)L_n} \right\| \quad (6.1)$$

$$\omega_n = \frac{\Omega_s}{\Omega_o} = \frac{F_s}{F_o}, L_n = \frac{L_m}{L_r}, Q = \frac{\sqrt{L_r / C_r}}{n^2 \cdot R_L}$$

Compared with SRC, the voltage conversion ratio of LLC is not only related with normalized switching frequency ω_n, quality factor Q, but also with normalized inductance ratio L_n, which is related with magnetizing inductance L_m. Given a certain L_n, the relations between M, ω_n and Q is very similar as SRC as L_m is clamped by output voltage and is essentially another branch in parallel with equivalent output load. As an example, For L_n=4.3, the voltage conversion ratio M is plotted versus ω_n and Q as shown in Figure 6. 9. In this case, the scenario is similar as SRC: Given the same frequency, when load is heavier, i.e. Q is larger, the output voltage is smaller as the load impedance is smaller compared with tank impedance. Given the same load or same Q, whe switching frequency is higher, the tank impedance is larger. As a result, the output voltage is smaller.

The magnetizing inductor L_m affects the output voltage as it can be regarded as another branch in parallel with equivalent output load. As shown in Figure 6. 10, for a given Q=0.6 and given switching frequency, when L_n is smaller, the impedance of magnetizing inductor is smaller, therefore, the equivalent output load impedance is smaller, which causes a smaller output voltage. From control point of view, the most important effect of L_m is that it affects the slope of voltage conversion ratio gain curve. For example, at point F_s=F_o shown in Figure 6. 10, the slope of gain curve is related with L_n shown as (6. 2). This means that there is a certain DC gain of control to output voltage due to L_m at point F_s=F_o. As a comparison, for SRC, at this point, the slope of gain-

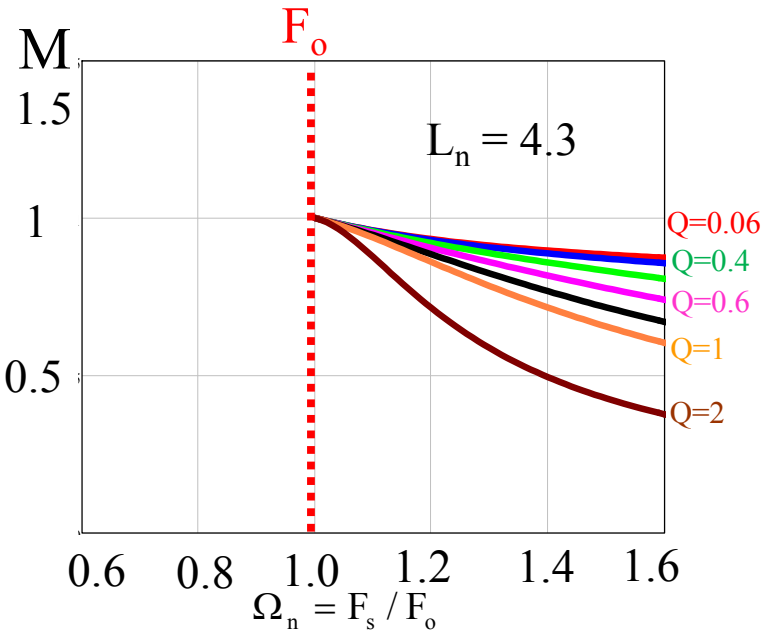


Figure 6. 9. Plot of M versus Ω_n and Q of LLC for Fs ≥ Fo with L_n=4.3.

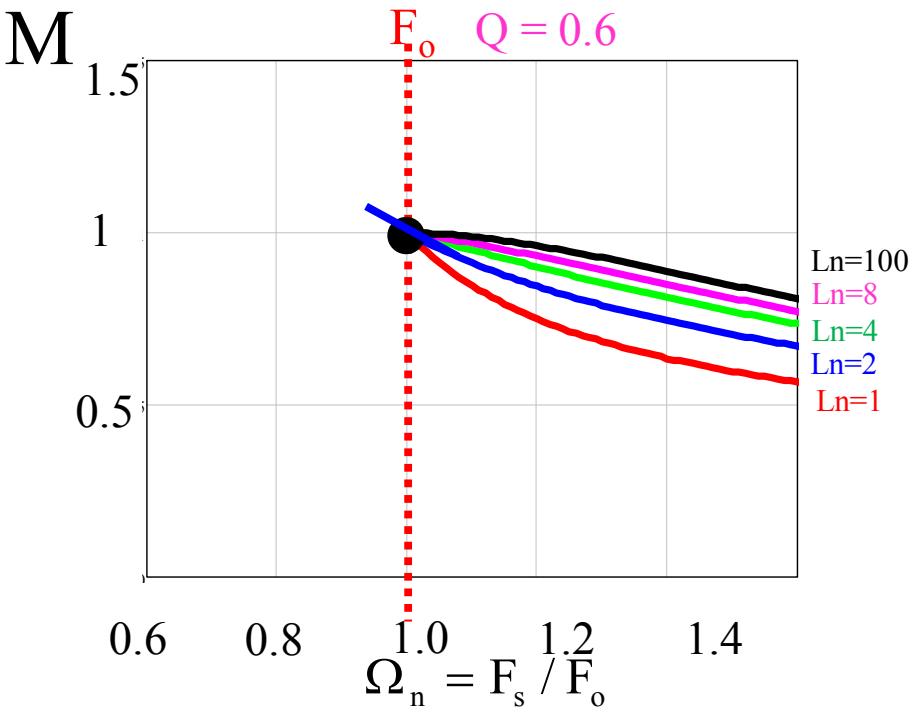


Figure 6. 10. Plot of M versus Ω_n and L_n of LLC for Fs ≥ Fo with Q=0.6.

-curve is zero, which is responsible for the canyon region in 3D control to output voltage transfer function plot shown in Figure 5. 19. From another perspective, SRC can be treated as a special case of LLC with infinite value of magnetizing inductance: When $L_m = \infty$, (6. 2) reduces to zero.

$$\frac{\partial M}{\partial \omega_n} = -\frac{2}{L_n} \tag{6. 2}$$

Similar as SRC, the resonant capacitor behaves like an equivalent inductor with respect to modulation frequency. Therefore, the resonant tank can be simplified as shown in Figure 6. 11.

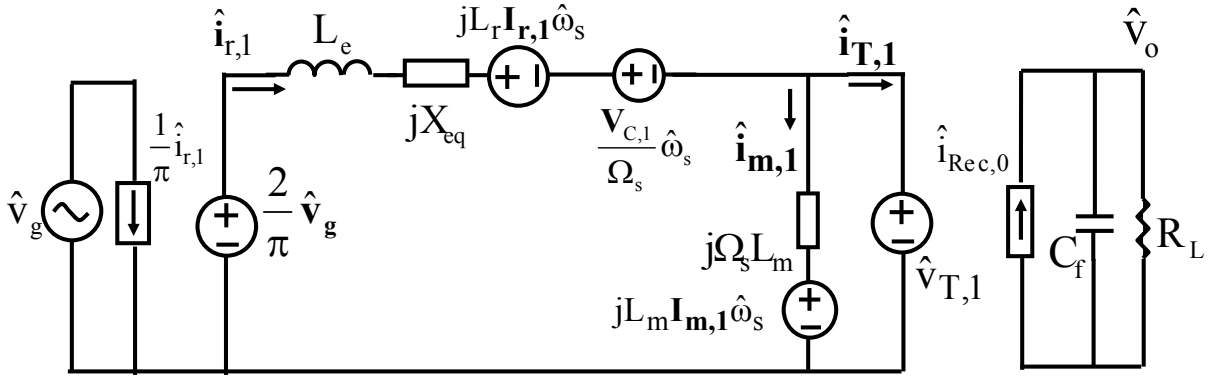


Figure 6. 11. Small-signal model of LLC for Fs ≥ Fo with simplified resonant capacitor branch.

The expression of equivalent inductor L_e and impedance X_{eq} is shown as (6. 3):

$$\begin{aligned} L_e &= L_r + \frac{1}{C_r\Omega_s^2} = L_r\left(1+\frac{\Omega_o^2}{\Omega_s^2}\right) \\ X_{eq} &= \Omega_s L_r - \frac{1}{\Omega_s C_r} \end{aligned} \tag{6. 3}$$

The small-signal model shown in Figure 6. 11 has complex terms and can not be used for simulation. Following the similar methodology as SRC, the complex terms can be eliminated by separating the resonant tank into sine part and cosine part, shown as Figure 6. 12.

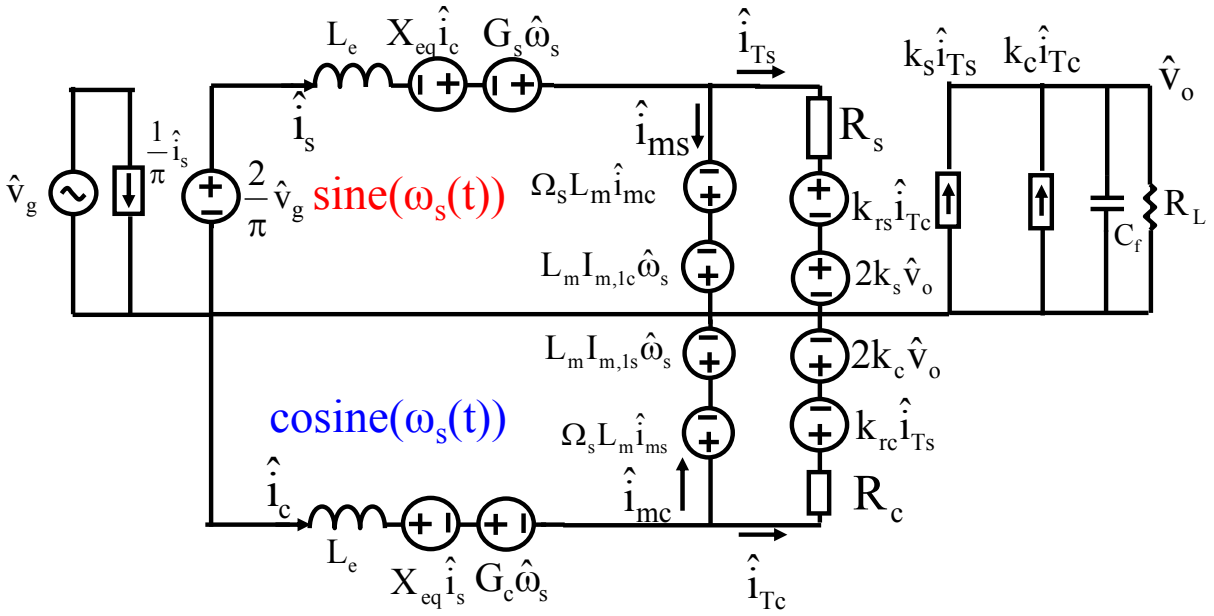


Figure 6. 12. Separated third-order equivalent circuit model of LLC for $F_s \geq F_o$.

The expressions of G_s, R_s, k_{rs}, k_s, G_c, k_{rc}, k_c are shown in (6. 4):

$$
\begin{aligned}
&G_s = L_r I_{r,1c} + \frac{V_{C,1s}}{\Omega_s}, G_c = L_r I_{r,1s} - \frac{V_{C,1c}}{\Omega_s} \\
&k_s = \frac{2}{\pi} n \frac{I_{T,1s}}{\sqrt{I_{T,1s}{}^2 + I_{T,1c}{}^2}}, k_c = \frac{2}{\pi} n \frac{I_{T,1c}}{\sqrt{I_{T,1s}{}^2 + I_{T,1c}{}^2}} \\
&R_s = \frac{4n}{\pi} \frac{V_o}{\sqrt{I_{T,1s}^2 + I_{T,1c}^2}} \frac{I_{T,1c}^2}{I_{T,1s}^2 + I_{T,1c}^2}, \\
&R_c = \frac{4n}{\pi} \frac{V_o}{\sqrt{I_{T,1s}^2 + I_{T,1c}^2}} \frac{I_{T,1s}^2}{I_{T,1s}^2 + I_{T,1c}^2}, \\
&k_{rs} = k_{rc} = -\frac{4n}{\pi} \frac{V_o}{\sqrt{I_{T,1s}^2 + I_{T,1c}^2}} \frac{I_{T,1s} I_{T,1c}}{I_{T,1s}^2 + I_{T,1c}^2}
\end{aligned}
\tag{6. 4}
$$

The expressions of $I_{r,1c}$, $I_{r,1s}$, $V_{C,1s}$, $V_{C,1c}$, $I_{T,1s}$, $I_{T,1,c}$ in (6. 4), $I_{m,1s}$ and $I_{m,1c}$ in Figure 6. 12 are derived from steady-state model shown in Figure 6. 8 and are listed in (6. 5):

$$
\begin{aligned}
I_{T,ls} &= \frac{2V_g}{\pi R_{eq}} \frac{\omega_n^2 L_n (L_n + 1 - \frac{1}{\omega_n^2})}{\omega_n^2 \left(L_n + 1 - \frac{1}{\omega_n^2} \right)^2 + \left(\frac{\pi^2}{8} Q\left(1 - \omega_n^2\right) L_n \right)^2}, \\
I_{T,lc} &= \frac{2V_g}{\pi R_{eq}} \frac{\omega_n L_n^2 \frac{\pi^2}{8} Q\left(1 - \omega_n^2\right)}{\omega_n^2 \left(L_n + 1 - \frac{1}{\omega_n^2} \right)^2 + \left(\frac{\pi^2}{8} Q\left(1 - \omega_n^2\right) L_n \right)^2}, \\
I_{m,ls} &= \frac{I_{T,lc} R_{eq}}{\Omega_s L_m}, I_{m,lc} = -\frac{I_{T,ls} R_{eq}}{\Omega_s L_m}, \\
I_{r,ls} &= I_{T,ls} + I_{m,ls}, I_{r,lc} = I_{T,lc} + I_{m,lc}, \\
V_{C,ls} &= \frac{I_{r,lc}}{\Omega_s C_r}, V_{C,lc} = -\frac{I_{r,ls}}{\Omega_s C_r}, R_{eq} = \frac{8}{\pi^2} n^2 R_L
\end{aligned}
\tag{6. 5}
$$

Similar as SRC, the superposition theorem is applied to derive a non-coupled equivalent circuit model. The non-coupled equivalent circuit is shown as Figure 6. 13.

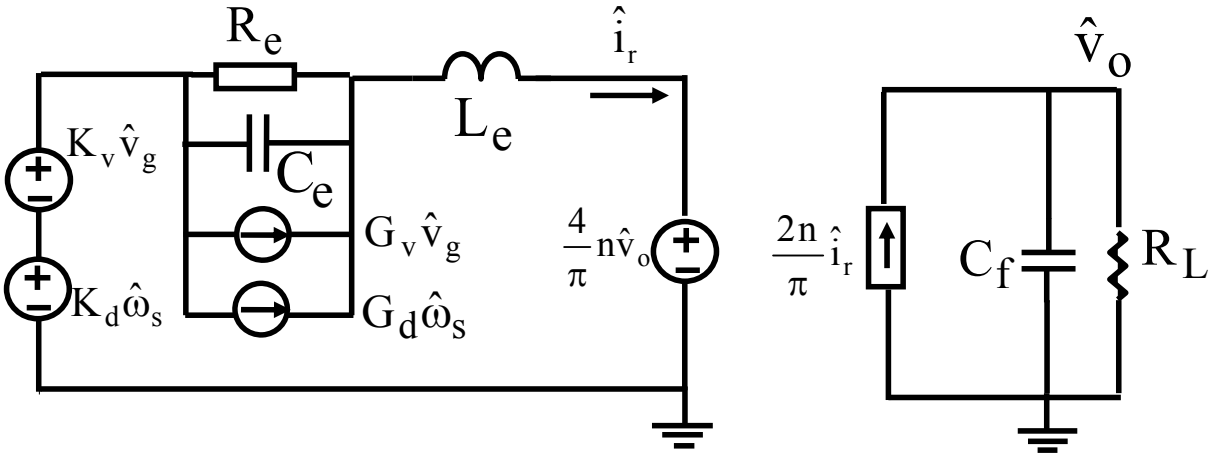


Figure 6. 13. Non-coupled third-order equivalent circuit model of LLC for $F_s \geq F_o$.

L_e, R_e, C_e are used to represent beat frequency dynamics and their expressions are same as SRC. The expressions of K_v, G_v, K_d and G_d are different from SRC and will be affected by the design of L_m. All the expressions are shown as (6. 6).

$$L_e = L_r(1+\frac{\Omega_o^2}{\Omega_s^2}), C_e = \frac{1}{L_e(\Omega_s-\Omega_o)^2}, R_e = \frac{L_e|X_{eq}||\Omega_s-\Omega_o|}{R_{eq}}$$

$$G_d = \frac{2V_g}{\pi}\frac{L_n}{\omega_o}\frac{1}{R_e}\left(\frac{\frac{1}{\omega_n}(\frac{1}{\omega_n^2}-\omega_n^2)\left(\frac{\pi^2}{8}QL_n\right)^2-\left(L_n+1-\frac{1}{\omega_n^2}\right)\left(\frac{2}{\omega_n^3}\right)}{\left[\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left((\frac{1}{\omega_n}-\omega_n)\frac{\pi^2}{8}QL_n\right)^2}\right]^3}+\frac{2}{{L_n}^2}\right), \quad (6.6)$$

$$K_d = -\frac{4V_g}{\pi}\frac{1}{\omega_o L_n}, G_v = \frac{1}{\pi}\frac{X_{eq}}{\sqrt{{X_{eq}}^2+R_{eq}^2}},$$

$$K_v = \frac{4}{\pi^2}\frac{V_g L_n \omega_n}{R_{eq}}\frac{L_n+1-\frac{1}{\omega_n^2}}{\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left((\frac{1}{\omega_n}-\omega_n)\frac{\pi^2}{8}QL_n\right)^2}},$$

$$R_{eq} = \frac{8}{\pi^2}n^2R_L, X_{eq} = \Omega_s L_r - \frac{1}{\Omega_s C_r}, L_n = \frac{L_m}{L_r}$$

6.2.2 Equivalent circuit model of LLC for $F_s < F_o$

Figure 6. 14 shows steady-state waveforms when $F_s=0.8F_o$ and Figure 6. 15 shows the operating modes at different time periods. Obviously, in this case, the resonant tank changes at different time periods: in time periods $[t_0, t_1]$ and $[t_2, t_3]$, the magnetizing inductor, L_m, is either clamped by V_o or $-V_o$ and never participates in resonance. This is exactly the same condition as previous case when $F_s \geq F_o$; in time periods $[t_1,t_2]$ and $[t_3,t_4]$, the magnetizing inductor L_m participates in resonance and the resonant tank is comprised of C_r and L_r in series with L_m. In the meanwhile, the output load is decoupled from the resonant tank. As the resonant tank is changing within one switching period, the LLC essentially belongs to multi-resonant structure when operating in the region $Fs< Fo$.

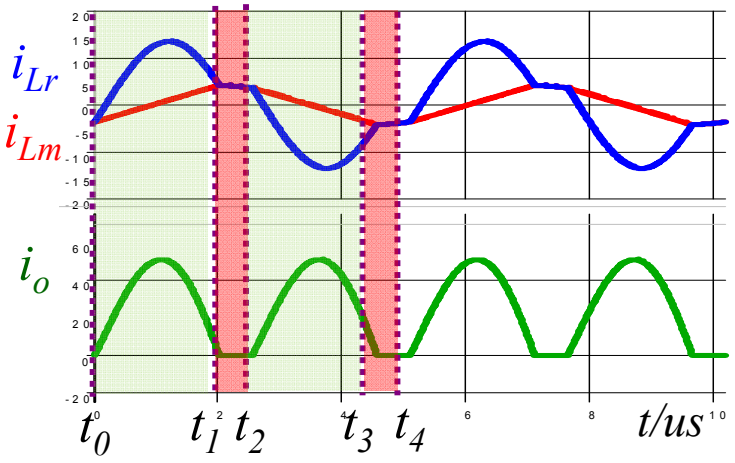


Figure 6. 14. Steady-state waveforms for Fs=0.8F_o.

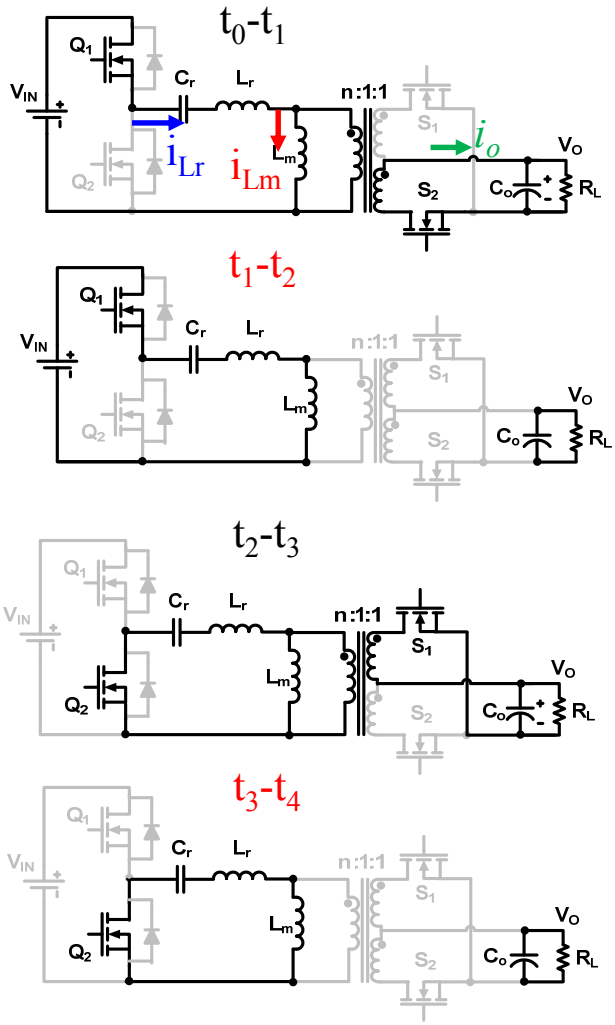
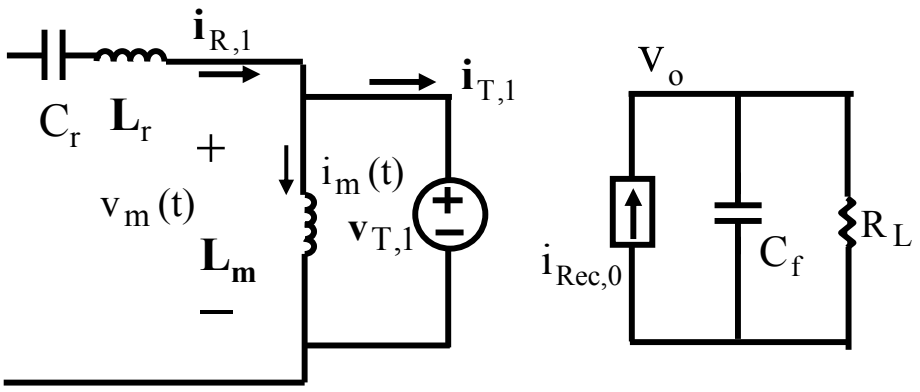
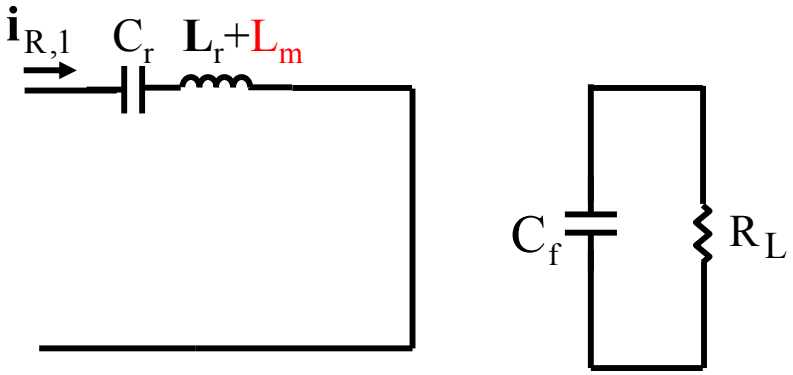


Figure 6. 15. Operating modes of LLC for Fs < F_o.

In time periods [t_0, t_1] and [t_2, t_3], tank and load are coupled and the relation of L_m, rectifier and output load are same as $F_s \geq F_o$ case, as shown in Figure 6. 16 (a). In time periods [t_1,t_2] and [t_3,t_4], tank and load are decoupled. In this case, L_r is in series with L_m and the sum of the two inductances resonates with Cr, as shown in Figure 6. 16 (b).



(a)



(b)

Figure 6. 16. The relation of L_m, rectifier and output load for $F_s < F_o$. (a) In time periods [t_0, t_1] and [t_2, t_3] (b) In time periods [t_1,t_2] and [t_3,t_4].

The length of time periods [t_0, t_1] and [t_2, t_3] is the resonant period T_o and the length of time periods [t_1,t_2] and [t_3,t_4] is T_s-T_o. For the whole switching period, the modulation model can be derived by combining the modulation model of Figure 6. 16 (a) and Figure 6. 16 (b), with the ratio of T_o/T_s and $(T_s-T_o)/T_s$, respectively. The large signal modulation model is shown as Figure 6. 17.

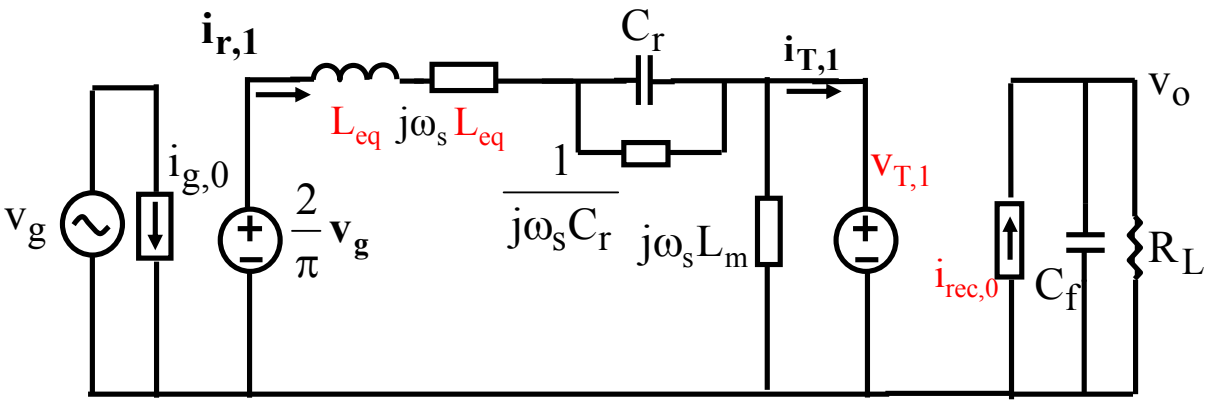
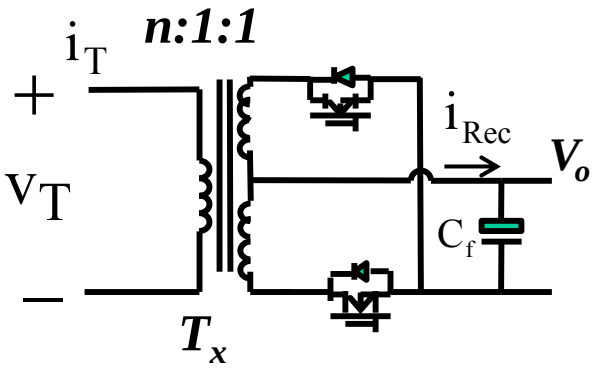


Figure 6. 17. Modulation model of LLC for Fs < F_o.

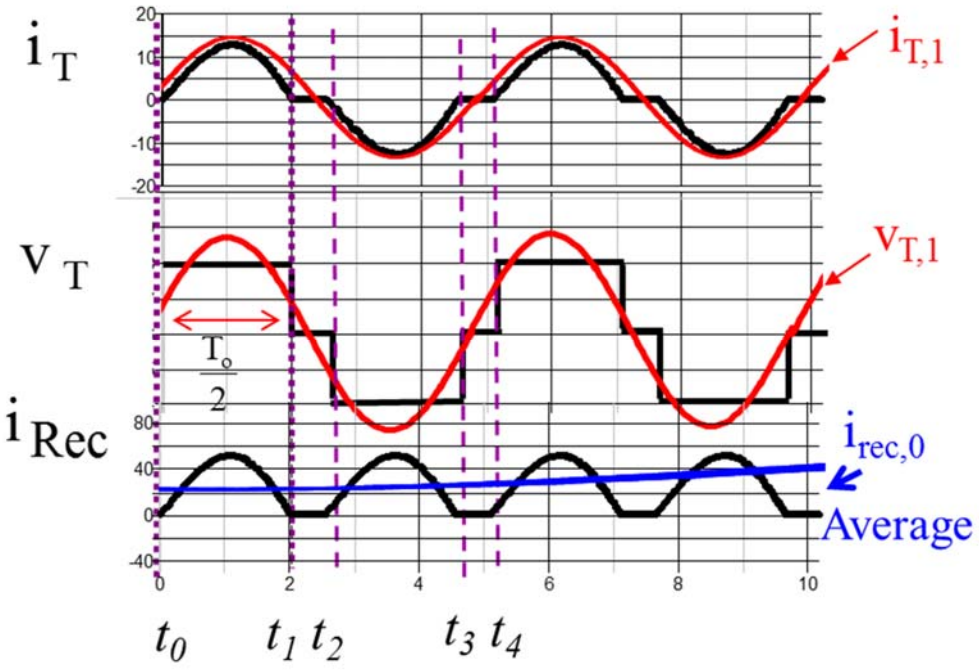
The equivalent resonant inductor, L_{eq} is related with resonant inductor and magnetizing inductor. The expression of L_{eq} is shown as (6. 7):

$$L_{eq} = L_r + L_m \frac{\Omega_o - \Omega_s}{\Omega_o} \tag{6. 7}$$

The model of the rectifier should be modified, as the voltage across the magnetizing inductor is a quasi-square wave instead of a square wave, as shown in Figure 6. 18 (b).



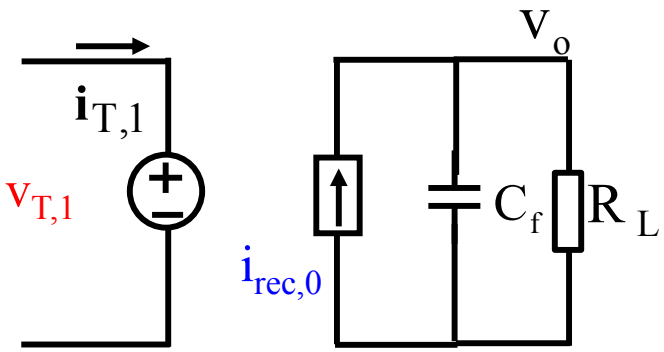
(a)



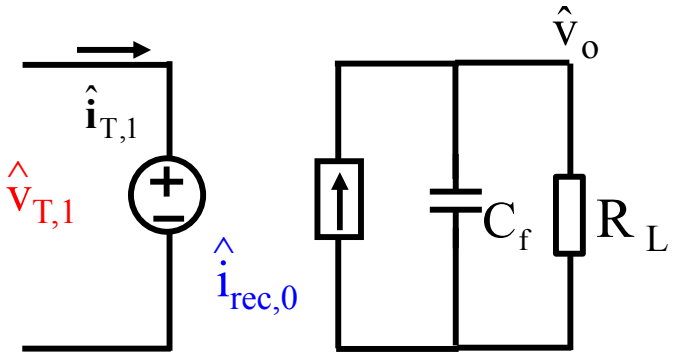
(b)

Figure 6. 18. (a) Structure (b) Waveforms of the rectifier of LLC for Fs < F_o.

The modulation model and small-signal model are shown in Figure 6. 19 and the expressions are shown in (6. 8) and (6. 9). When F_s=F_o, the quasi-square-wave of V_T becomes square wave and the model of the rectifier reduces to the model used in SRC.



(a)



(b)

Figure 6. 19. (a) Modulation model (b) Small-signal model of the rectifier of LLC for Fs < F_o.

$$v_{T,1} = \frac{4}{\pi} n v_o \sin\left(\frac{1}{2}\frac{\Omega_s}{\Omega_o}\pi\right)\frac{\mathbf{i}_{T,1}}{\|\mathbf{i}_{T,1}\|} \tag{6. 8}$$

$$i_{rec,0} = \frac{2}{\pi} n \|\mathbf{i}_{T,1}\|$$

$$\hat{v}_{T,1} = \sin\left(\frac{1}{2}\frac{\Omega_s}{\Omega_o}\pi\right)\left(k_{vo}\hat{v}_o + k_{is}\hat{i}_{T,s} + k_{ic}\hat{i}_{T,c}\right) \tag{6. 9}$$

$$\hat{i}_{rec,0} = k_s\hat{i}_{T,s} + k_c\hat{i}_{T,c}$$

With the modified model of the rectifier, the steady-state model of LLC for F_s < F_o can be derived, shown as Figure 6. 20.

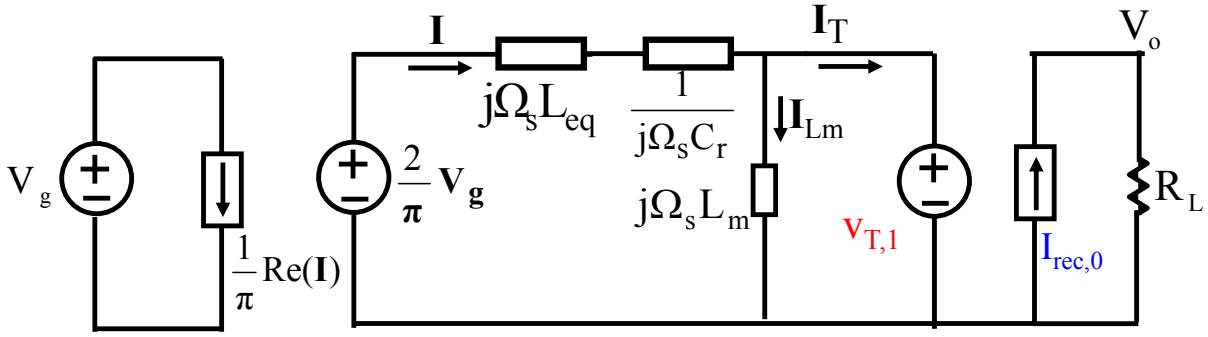


Figure 6. 20. Steady-state model of LLC for Fs < Fo.

The voltage conversion ratio can be derived from Figure 6. 20, shown as (6. 10):

$$M=\frac{2nV_o}{V_g}=\frac{1}{\sin(\omega_n\pi/2)}\left\|\frac{j\omega_n L_n}{j\omega_n\left(L_n+1-\frac{1}{\omega_n^2}\right)+\frac{\pi^2}{8}Q\frac{1}{\sin(\omega_n\pi/2)}(1-\omega_n^2))L_n\omega_n}\right\| \quad (6.\ 10)$$

$$\omega_n=\frac{\Omega_s}{\Omega_o}=\frac{F_s}{F_o},L_n=\frac{L_m}{L_r},Q=\frac{\sqrt{L_r/C_r}}{n^2\cdot R_L}$$

Combine (6. 1) and (6. 10), the voltage conversion ratio can be plotted as shown in Figure 6. 21. When Fs<Fo, the DC Gain is greater than 1 and it shows the characteristic of Parallel Resonant Converter (PRC). As shown later in this chapter, the voltage conversion ratio derived in this manner is more accurate than traditional fundamental analysis [F1][F31]--[F34]. However, as fundamental approximation is still used in this approach, at low switching frequency, the gain curve starts to lose accuracy as there is more harmonics in the resonant variables. In this case, more precise steady-state analysis based on describing method and mode analysis can be employed to improve accuracy [F35]-[F39].

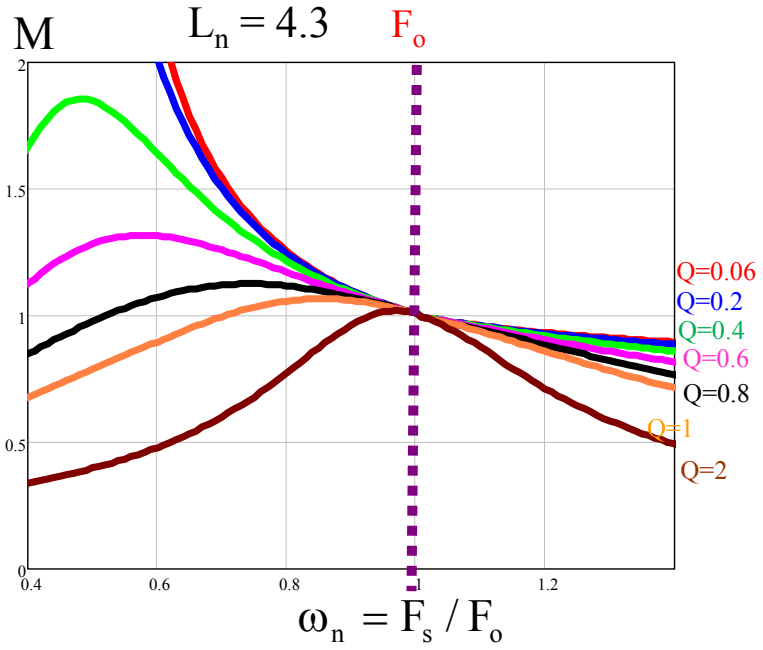


Figure 6. 21. Voltage conversion ratio of LLC.

The small-signal model is shown in Figure 6. 22 and the expression of L_{eq} is shown in (6. 7).

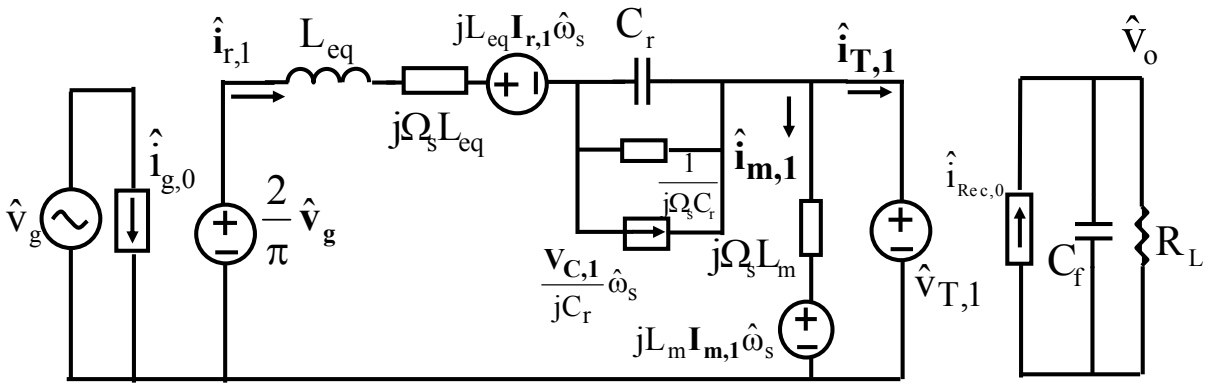


Figure 6. 22. Small-signal model of LLC for Fs < Fo.

Similar as previous case, the resonant capacitor behaves like an equivalent inductor with respect to modulation frequency. Therefore, the resonant tank can be simplified as shown in Figure 6. 23.

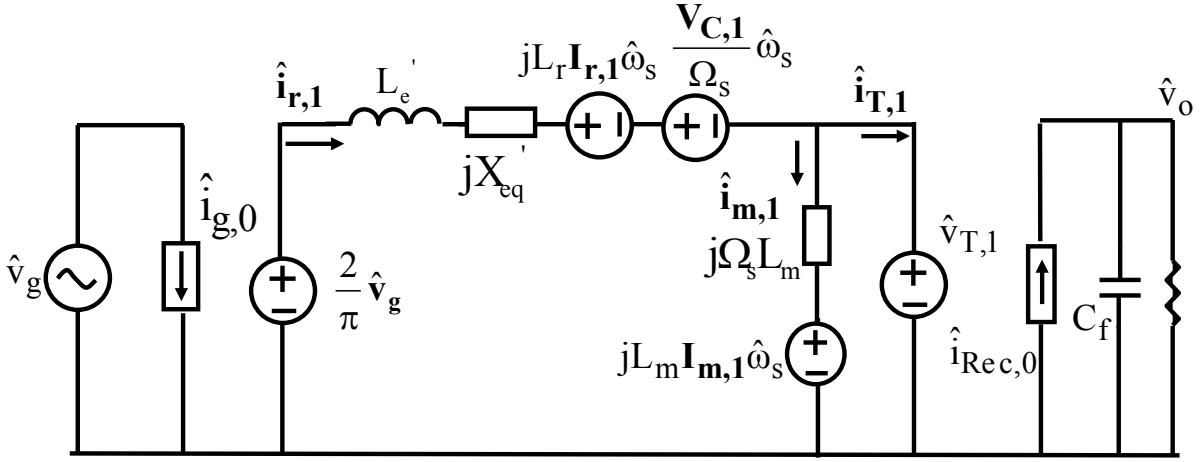


Figure 6. 23. Small-signal model of LLC for $F_s < F_o$ with simplified resonant capacitor branch.

The expression of equivalent inductor L_e'and impedance X_{eq}' is modified by L_m and shown as (6. 11).

$$\begin{aligned} L_e' &= L_r + L_m\frac{\Omega_o-\Omega_s}{\Omega_o} + \frac{1}{C_r\Omega_s^2} = L_r(1+\frac{1}{\omega_n^2}) + L_m(1-\omega_n) \\ X_{eq}' &= \Omega_s(L_r + L_m(1-\omega_n)) - \frac{1}{\Omega_s C_r} \end{aligned} \tag{6. 11}$$

Following the similar methodology as previous case, the complex terms can be eliminated by separating the resonant tank into sine part and cosine part, shown as Figure 6. 24.

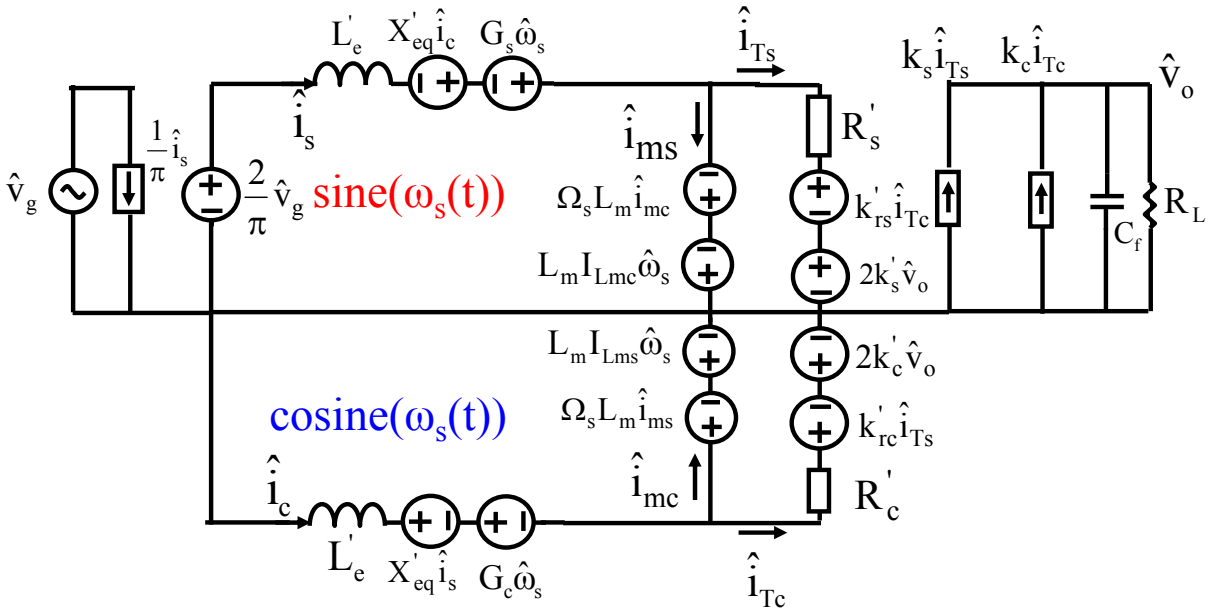


Figure 6. 24. Separated equivalent circuit model of LLC for $F_s < F_o$.

The expressions are shown in (6. 12):

$$\begin{aligned} R_s' &= R_s \sin(\frac{\pi}{2}\omega_n), R_c' = R_c \sin(\frac{\pi}{2}\omega_n) \\ k_{rs}' &= k_{rc}' = k_{rs} \sin(\frac{\pi}{2}\omega_n) \\ k_s' &= k_s \sin(\frac{\pi}{2}\omega_n), k_c' = k_c \sin(\frac{\pi}{2}\omega_n) \end{aligned} \tag{6. 12}$$

Similar as previous case, the superposition theorem is applied to derive a non-coupled equivalent circuit model. The non-coupled equivalent circuit is shown as Figure 6. 25.

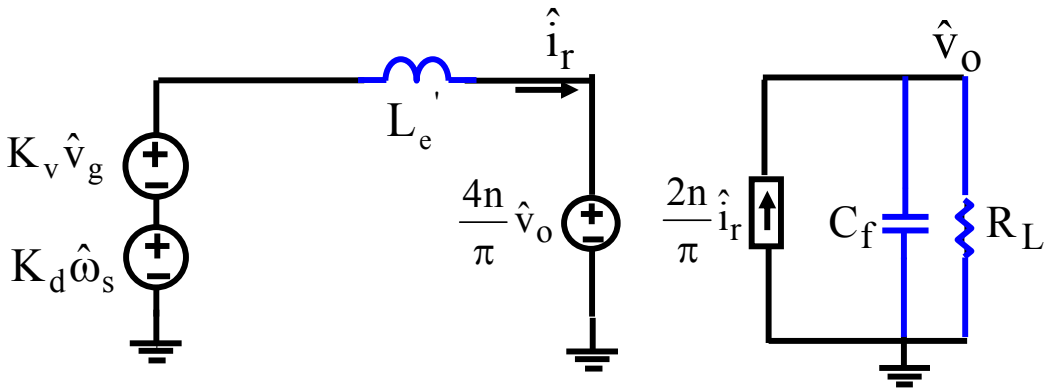


Figure 6. 25. Non-coupled equivalent circuit model of LLC for $F_s < F_o$.

In this case, there is no beat frequency dynamics and the circuit is especially second-order. The expressions of L_e', Kv, and K_d are shown as (6. 13).

$$L_e' = L_r\left(1+\frac{1}{\omega_n^2}\right)+L_m(1-\omega_n)$$

$$K_d = \frac{2V_g}{\pi}\frac{L_n}{\omega_o}\left[\frac{\left[\left(\frac{1}{\omega_n^2}-\omega_n^2\right)\left(\frac{\pi^2}{8}Q_rL_n\right)^2-\left(L_n+1-\frac{1}{\omega_n^2}\right)\left(\frac{2}{\omega_n^2}\right)\right]\frac{1}{\omega_n}\cdot\frac{1}{\sin(\frac{\pi}{2}\omega_n)}}{\left[\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left(\left(\frac{1}{\omega_n}-\omega_n\right)\frac{\pi^2}{8}Q_rL_n\right)^2}\right]^3}+\frac{\left(-\frac{\pi}{2}\frac{\cos(\frac{\pi}{2}\omega_n)}{\sin^2(\frac{\pi}{2}\omega_n)}\right)}{\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left(\left(\frac{1}{\omega_n}-\omega_n\right)\frac{\pi^2}{8}Q_rL_n\right)^2}}\right] \quad (6.\ 13)$$

$$K_v = \frac{2}{\pi}\frac{L_n}{\sin(\omega_n\pi/2)}\frac{1}{\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left(\left(\frac{1}{\omega_n}-\omega_n\right)\frac{\pi^2}{8}Q_rL_n\frac{1}{\sin(\omega_n\pi/2)}\right)^2}}$$

6.2.3 Unified equivalent circuit model of LLC

The steady-state voltage conversion ratio for $F_s \geq F_o$ shown in (6. 1) and $F_s < F_o$ in (6. 10) can be conbined as shown in (6. 14) and can be ploted as shown in Figure 6. 21.

$$M = \frac{1}{\sin(\alpha/2)}\left\|\frac{j\omega_nL_n}{j\omega_n\left(L_n+1-\frac{1}{\omega_n^2}\right)+\frac{\pi^2}{8}Q\frac{1}{\sin(\alpha/2)}(1-\omega_n^2))L_n\omega_n}\right\|, \quad (6.\ 14)$$

$\alpha = \omega_n\pi$ for $F_s < F_o$

$\alpha = \pi$ for $F_s \geq F_o$

The small-signal models shown in Figure 6. 13 and Figure 6. 25 can be combined to obtain a model which is valid both for $F_s \geq F_o$ and $F_s<F_o$. The unified equivalent circuit model is shown in Figure 6. 26. The expressions of L_e, Re, Ce, are shown as (6. 15). The expressions of K_v, G_v, K_d and G_d are shown in (6. 6) and (6. 13).

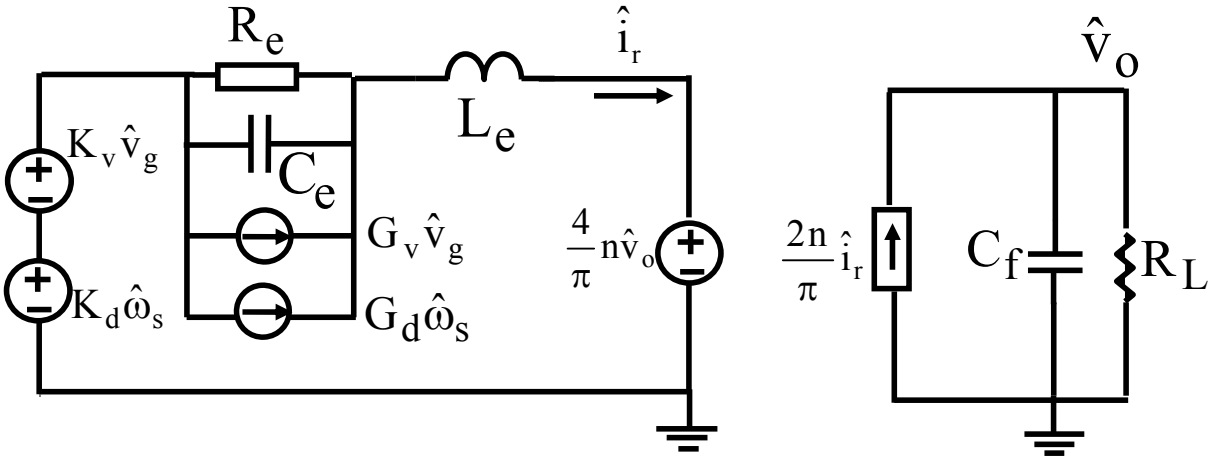


Figure 6. 26. Unified equivalent circuit model of LLC.

$$L_e = \begin{cases} (1+\frac{1}{\omega_n{}^2})L_r & \text{for } \omega_n \geq 1 \\ (1+\frac{1}{\omega_n{}^2})L_r + (1-\omega_n)L_m & \text{for } \omega_n < 1 \end{cases}$$

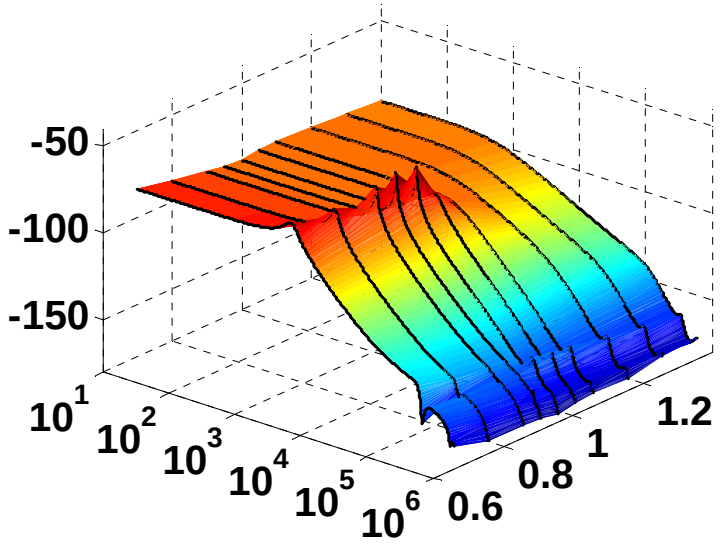
$$R_e = \begin{cases} \frac{L_e\left|X_{eq}\right\|\Omega_s-\Omega_o\right|}{R_{eq}}, & \text{for } \omega_n \geq 1 \\ 0, & \text{for } \omega_n \leq 1 \end{cases} \qquad (6.\ 15)$$

$$C_e = \frac{1}{L_e(\Omega_s-\Omega_o)^2}$$

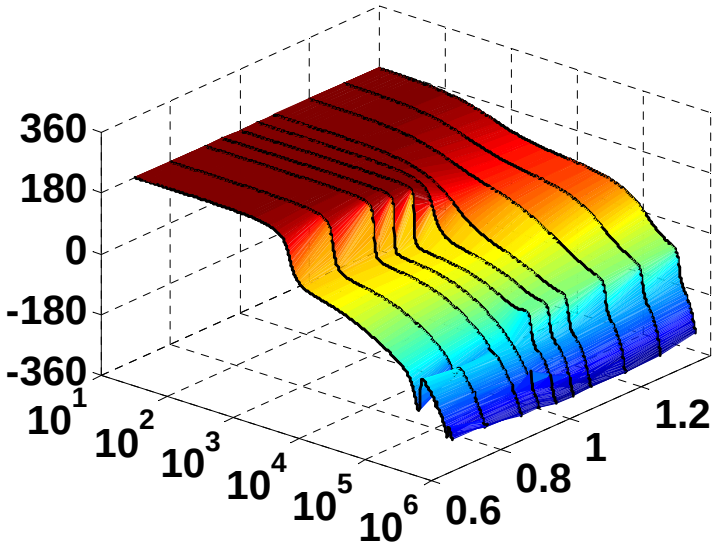
6.3 Discussion and Predictions of Proposed Equivalent Circuit Model

6.3.1 DC gain and beat frequency dynamics

With the help of Figure 6. 26, the 3D-plot of control to output voltage transfer function can be plotted as Figure 6. 27:



(a)



(b)

Figure 6. 27. 3D Bode plot of control-to-output voltage transfer function (a) Gain plot. (b) Phase plot.

The DC gain and poles can be explained clearly using the proposed non-coupled equivalent circuit model shown in Figure 6. 26.

From Figure 6. 26, the DC gain of the control-to-output voltage transfer function can be derived easily.The DC gain can be related with the slope of the voltage conversion ratio curve by the relations shown in (6. 16):

$$G_{DC} = \frac{\partial V_o}{\partial \Omega_s} = \frac{V_g}{2n\Omega_o}\frac{\partial M}{\partial \Omega_s} \tag{6. 16}$$

As shown in Figure 6. 28, as ZVS is preferred, When $\Omega_s > \Omega_o$, shown as the red point, the slope is negative and the starting phase in Figure 6. 27 is 180 degrees. When $\Omega_s = \Omega_o$ shown as the blue point, the slope is still negative due to the help of magnetizing inductor L_m. Therefore, the starting phase is still 180 deg and there is still certain amount of DC gain for the control to output transfer function. As a result, no canyon is observed for LLC resonant converter. This is an important difference compared with SRC, where the DC gain is zero at this point and there is a canyon in 3D graph in Figure 5. 19. When $\Omega_s < \Omega_o$ shown as the black point, the slope is still negative, and the circuit is still operated at ZVS region. This is also different compared with SRC, where the circuit operates at ZCS region when $\Omega_s < \Omega_o$.

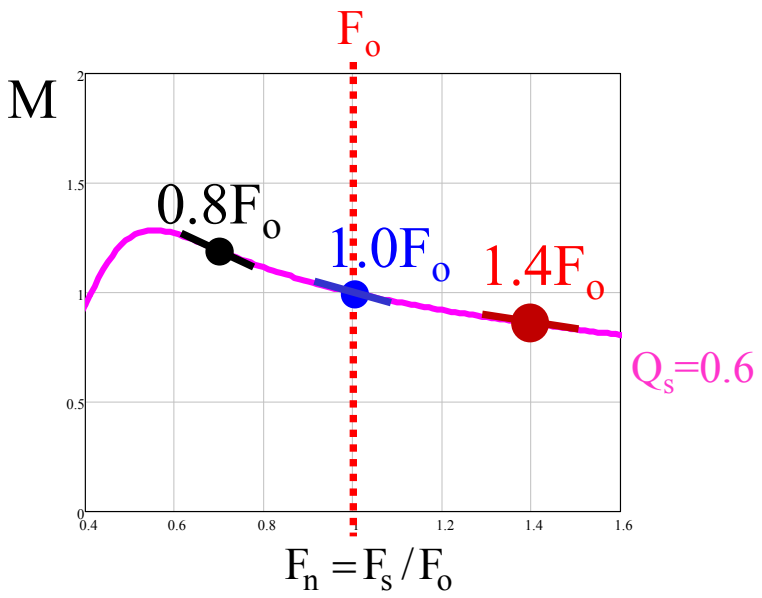


Figure 6. 28. Slope of voltage conversion ratio Vs. switching frequency.

The beat frequency dynamic performance of the circuit can also be well explained by the equivalent circuit. The components R_e, C_e and L_e represent beat frequency dynamics. The equivalent inductor L_e is probably resonant with the equivalent output capacitor or the equivalent capacitor C_e, depending on the value of R_e.

When switching frequency F_s is much larger than resonant frequency F_o, R_e is large. L_e is resonant with C_e, which forms the beat frequency double pole. The output capacitor and load resistor forms a single pole on the load side. In this case, the double pole position its quality factor can be easily derived from Figure 6. 26 as in (6. 17). Note that the position and quality factor of beat frequency double pole is same as SRC. This is reasonable as when F_s>>F_o, LLC behaves like SRC and L_m does not participates in resonance, therefore the effect of L_m on beat frequency double pole is very little.

$$\omega_p = \left|\Omega_s - \Omega_o\right|, Q_p = \frac{\left|\Omega_s L_r - \frac{1}{\Omega_s C_r}\right|}{R_{eq}} \tag{6. 17}$$

When switching frequency F_s is larger than F_o but close to F_o, R_e is small. The double pole caused by L_e and C_e will be damped out and split, one moves to high frequency and the other one moves to low frequency. This low frequency pole will combine with low pass filter pole and forms a double pole. In other words, L_e resonates with equivalent output capacitor C_f and load resistance determines the damping factor of this double pole. In this case, the double pole position and its quality factor are shown as (6. 18).

$$\omega_p = \sqrt{\frac{1}{L_e \frac{\pi^2}{8n^2} C_f}}, Q_p = \frac{8n}{\pi^2} R_L \sqrt{\frac{C_f}{L_e}} \tag{6. 18}$$

$$L_e = (1 + \frac{1}{\omega_n^{\ 2}}) L_r$$

When switching frequency F_s is below F_o, in this case, no beat frequency double pole exists. L_e resonates with equivalent output capacitor C_f and load resistance determines the damping factor of this double pole. However, in this case, L_e is modified by L_m according to (6. 11) as there is a certain time period that L_m also participated in resonance. As a result, the double pole moves to a lower frequency with reduced quality factor. In this case, the double pole position and its quality factor are shown as (6. 19):

$$\omega_p = \sqrt{\frac{1}{L_e \frac{\pi^2}{8n^2} C_f}}, Q_p = \frac{8n}{\pi^2} R_L \sqrt{\frac{C_f}{L_e}}$$
$$L_e = L_r\left(1 + \frac{1}{\omega_n^2}\right) + L_m(1 - \omega_n) \quad (6.\ 19)$$

The following illustration example is provided to explain the beat frequency dynamics. When F_s=1.4F_o, R_e=6.5Ω is large, L_e resonates with C_e. F_{beat}=100kHz, Q_{beat}=0.6. The 2D Bode plot is shown as the red curve in Figure 6. 29, there is a beat frequency double pole at 100kHz and a single pole at low frequency caused by the output filter. When F_s=F_o, R_e=0Ω is very small. The beat frequency double pole is split. L_e resonates with output capacitor C_f. Shown as the blue curve in Figure 6. 29, the double pole formed by L_e and equivalent output capacitor, instead of beat frequency double pole, is observed. In this circumstance, the circuit is second order instead of third-order. When F_s=0.8F_o, the double pole reduces to around 3kHz due to the increase of the equivalent resonant inductance. There is no beat frequency double pole in region $F_s < F_o$.

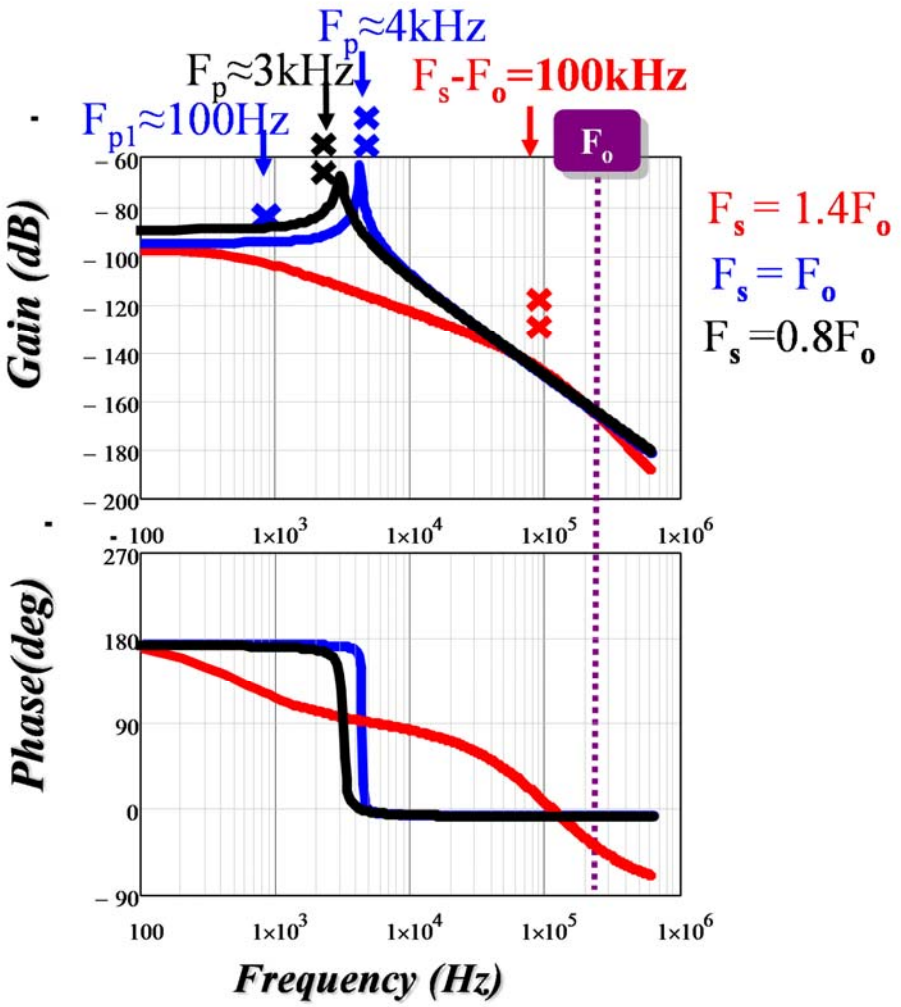


Figure 6. 29. Bode plots of control-to-output voltage transfer functions for LLC.

6.3.2 Analytical Expressions of Transfer Functions

All the analytical transfer functions can be derived from Figure 6. 12, Figure 6. 24 and Figure 6. 25. The analytical transfer functions are provided in Table 6. 1 and Table 6. 2 for easy reference. These transfer functions are very helpful in designing the outer feedback compensator. For $F_s \geq F_o$, the transfer functions are generally third-order and can be reduced to second order when F_s is close to F_o. For $F_s < F_o$, the transfer functions are second-order.

Table 6. 1 Analytical transfer functions of LLC resonant converter for $F_s \geq F_o$

$\frac{\hat{v}_o(s)}{\hat{\omega}_s(s)} = G_{DC} \frac{X_{eq}^2 + R_{eq}^2}{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}$ $G_{DC} = \frac{V_g}{2n} \frac{L_n}{\omega_o \omega_n} \frac{(\frac{1}{\omega_n^2} - \omega_n^2)\left(\frac{\pi^2}{8} Q_r L_n\right)^2 - \left(L_n + 1 - \frac{1}{\omega_n^2}\right)\left(\frac{2}{\omega_n^2}\right)}{\left[\sqrt{\left(L_n + 1 - \frac{1}{\omega_n^2}\right)^2 + \left((\frac{1}{\omega_n} - \omega_n)\frac{\pi^2}{8} Q_r L_n\right)^2}\right]^3}$ $L_e = (1 + \frac{\Omega_o^{\ 2}}{\Omega_s^{\ 2}}) L_r, R_{eq} = \frac{8}{\pi^2} n^2 R_L, X_{eq} = \Omega_s L_r - \frac{1}{\Omega_s C_r}, Q = \frac{\sqrt{L_r / C_r}}{n^2 \cdot R_L}, L_n = \frac{L_m}{L_r}$	(6. 20)
$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{2n} M_{st} \frac{R_{eq}^{\ 2} + X_{eq}^2 + L_e R_{eq} s}{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}$ $M_{st} = \left\| \frac{j\omega_n L_n}{j\omega_n \left(L_n + 1 - \frac{1}{\omega_n^2}\right) + \frac{\pi^2}{8} Q(1 - \omega_n^2) L_n} \right\|$	(6. 21)
$Z_o(s) = R_L \frac{s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2}{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}$	(6. 22)
$Z_{in}(s) = \frac{\pi^2}{2} \frac{(s^2 L_e^{\ 2} + sL_e R_{eq} + X_{eq}^2)(1 + R_L C_f s) + R_{eq}(sL_e + R_{eq})}{s^2 L_e C_f R_L + sL_e + sC_f R_L \frac{R_{eq}^{\ 3}}{R_{eq}^{\ 2} + X_{eq}^2} + R_{eq}}$	(6. 23)

Table 6. 2 Analytical transfer functions of LLC resonant converter for $F_s < F_o$

$\frac{\hat{v}_o(s)}{\hat{\omega}_s(s)} = G_{DC}\frac{1}{1+\frac{s}{Q_p\omega_p}+\left(\frac{s^2}{\omega_p^{\ 2}}\right)}$ $G_{DC} = \frac{V_g}{2n}\frac{L_n}{\omega_o}\left[\frac{\left[(\frac{1}{\omega_n^2}-\omega_n^2)\left(\frac{\pi^2}{8}Q_rL_n\right)^2-\left(L_n+1-\frac{1}{\omega_n^2}\right)\left(\frac{2}{\omega_n^2}\right)\right]\frac{1}{\omega_n}\cdot\frac{1}{\sin(\frac{\pi}{2}\omega_n)}}{\left[\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left((\frac{1}{\omega_n}-\omega_n)\frac{\pi^2}{8}Q_rL_n\right)^2}\right]^3}+\frac{\left(-\frac{\pi}{2}\frac{\cos(\frac{\pi}{2}\omega_n)}{\sin^2(\frac{\pi}{2}\omega_n)}\right)}{\sqrt{\left(L_n+1-\frac{1}{\omega_n^2}\right)^2+\left((\frac{1}{\omega_n}-\omega_n)\frac{\pi^2}{8}Q_rL_n\right)^2}}\right]$ $Q_p = \frac{8n}{\pi^2}R_L\sqrt{\frac{C_f}{L_e}}, \omega_p = \sqrt{\frac{1}{L_e\frac{\pi^2}{8n^2}C_f}}, L_e = L_r(1+\frac{1}{\omega_n^2})+L_m(1-\omega_n)$	(6. 24)
$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{2n}M_{st}\frac{1}{1+\frac{s}{Q_p\omega_p}+\left(\frac{s^2}{\omega_p^{\ 2}}\right)}$ $M_{st} = \frac{1}{\sin(\omega_n\pi/2)}\left\|\frac{j\omega_nL_n}{j\omega_n\left(L_n+1-\frac{1}{\omega_n^2}\right)+\frac{\pi^2}{8}Q(1-\omega_n^2))\frac{1}{\sin(\omega_n\pi/2)}L_n\omega_n}\right\|$	(6. 25)
$Z_o(s) = \frac{sL_e\frac{\pi^2}{8n^2}}{1+\frac{s}{Q_p\omega_p}+\left(\frac{s^2}{\omega_p^{\ 2}}\right)}$	(6. 26)
$Z_{in}(s) = \frac{\pi^2}{2}(sL_e+\frac{\frac{8n^2}{\pi^2}R_L}{R_LC_fs+1})$	(6. 27)

6.4 Simulation and Experimental Verifications

The SIMPLIS simulation tool is used to verify the voltage conversion ratio and small-signal analysis. Circuit parameters are shown as follows: V_g=400V, Lr=14uH, Cr=30nF, F_o=250kHz, C_f =660μF, n=4, R_L=2.3Ω, the corresponding Q=0.6.At resonant frequency, the output voltage is around 48V with 1kW full power.

Figure 6. 30 shows the comparison of the voltage conversion ratio using analytical equations (6. 1) and (6. 10) and simulation results. The analytical solutions have good accuracy when Fs ≥ 0.8 F_o. However, as fundamental approximation is still used in this approach, at low switching frequency, the gain curve starts to lose accuracy as there is more harmonics in the resonant variables.

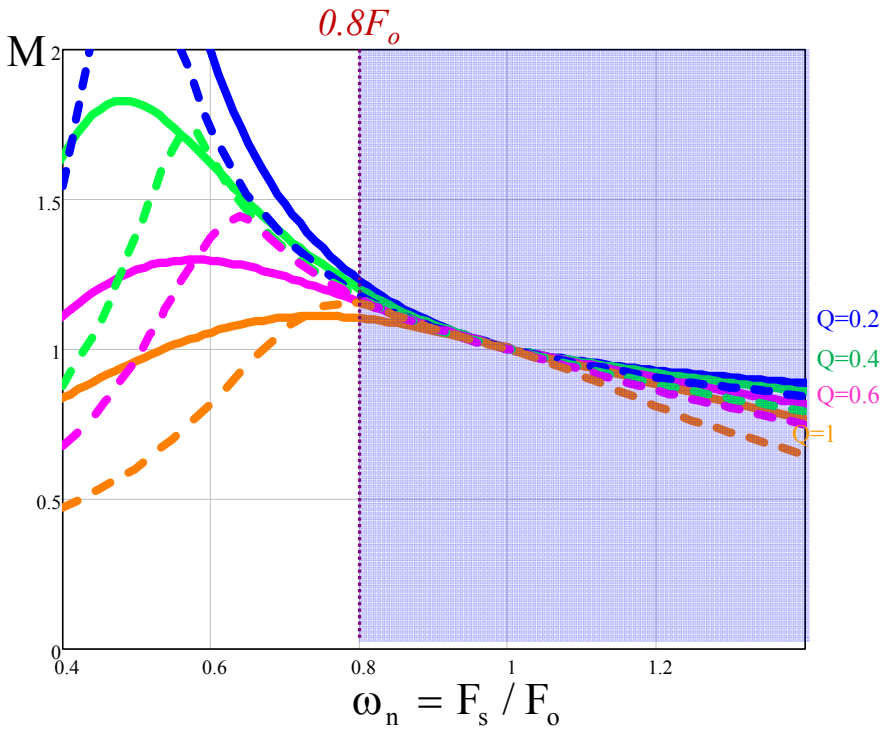


Figure 6. 30. Simplis verification of voltage conversion ratio for LLC converter.

Figure 6. 31 shows Simplis verification of control to output voltage transfer function for F_s=1.4F_o, Fs=Fo and Fs=0.8Fo. In all three cases, the model match very well with simulation

results. As previous analysis shows, when Fs=1.4Fo, there is still a beat frequency double pole; when Fs=Fo, the beat frequency double pole splits and a new double pole formed by Le and equivalent output capacitor C_f shows up; when Fs=0.8Fo, the double pole moves to a little lower frequency as equivalent resonant inductor is increased to include the effect of magnetizing inductor.

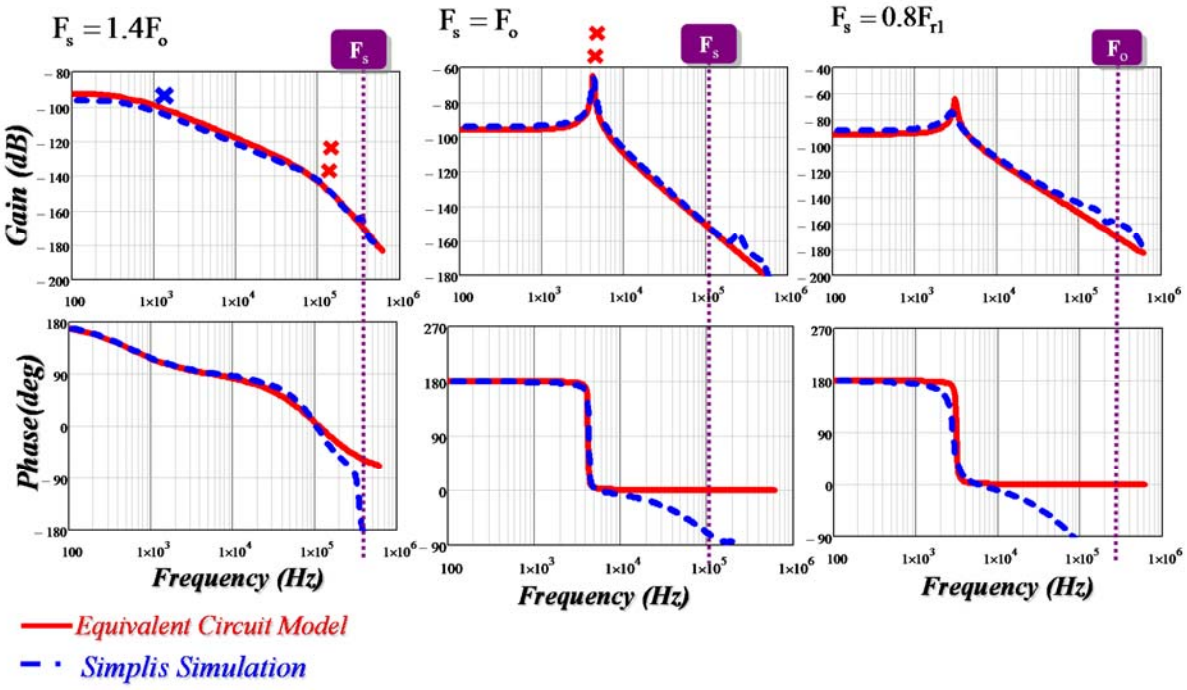


Figure 6. 31. Simplis verification of control-to-output transfer function for F_s=1.4F_o, Fs=Fo and Fs=0.8Fo

To verify other transfer functions, Figure 6. 32, Figure 6. 33 and Figure 6. 34 shows the comparison of all the transfer functions between the equivalent circuit model and simulation results for F_s=1.2F_o, F_s=F_o and F_s=0.9F_o, respectively. All the transfer functions match very well.

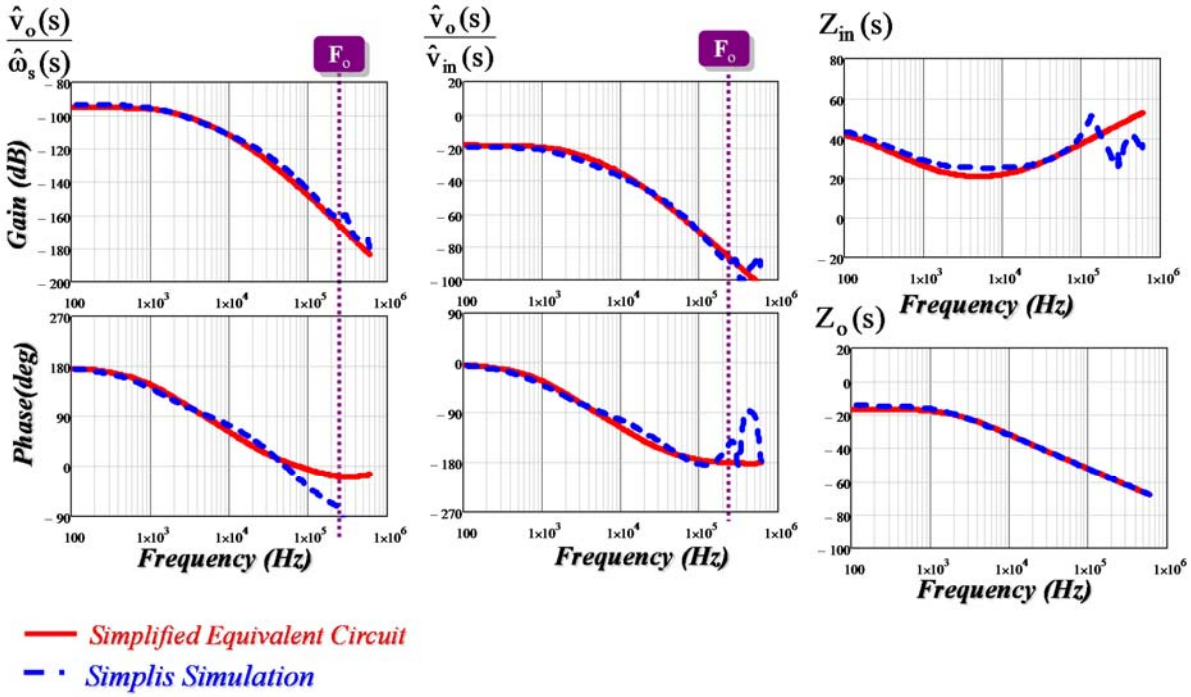


Figure 6. 32. Simplis verification of small-signal equivalent circuit model for $F_s=1.2F_o$.

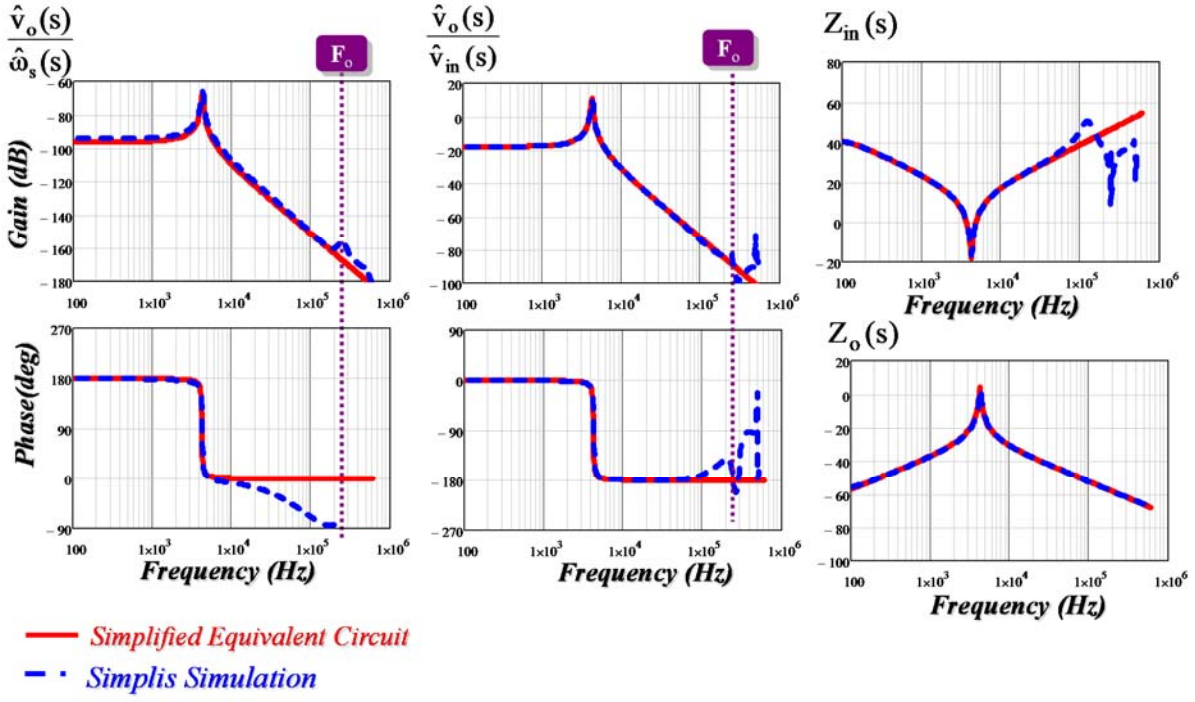


Figure 6. 33. Simplis verification of small-signal equivalent circuit model for Fs=Fo.

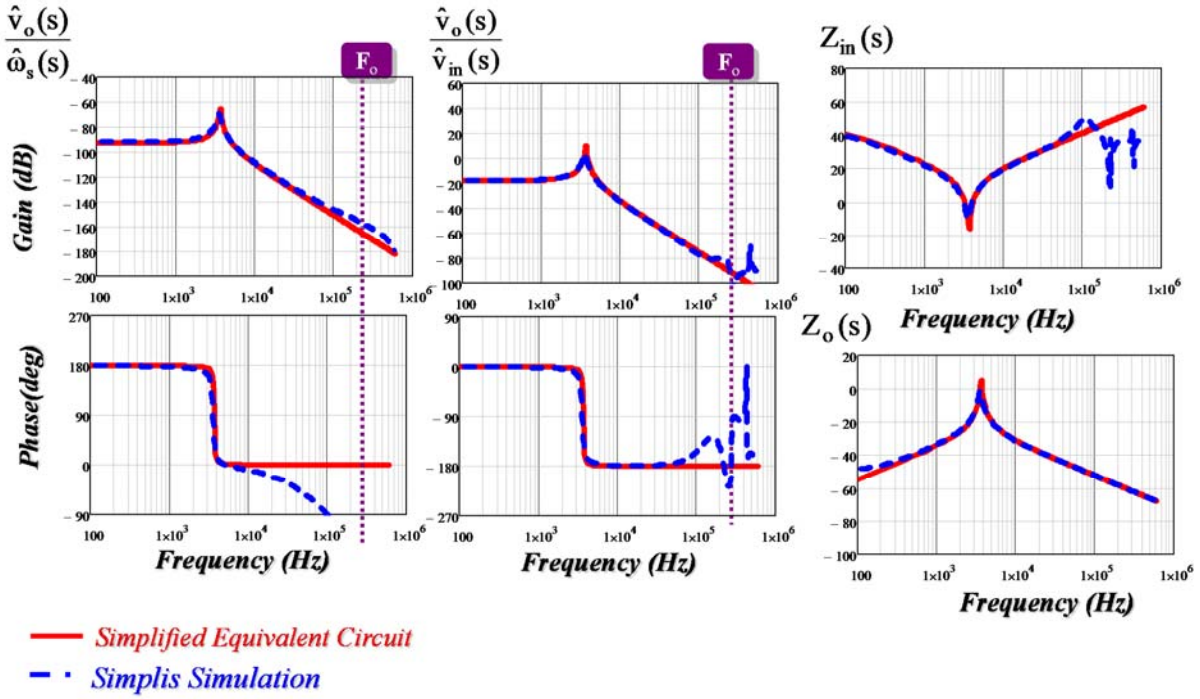


Figure 6. 34. Simplis verification of small-signal equivalent circuit model for Fs=0.9Fo.

The experimental verification of control to output voltage is shown as Figure 6. 35. The circuit parameters of the hardware are as follows: V_{in}=50V, L_r = 360nH, L_m = 2.1uH, C_r = 110nF, C_f = 50uF, n=5:1, R_L=1Ω, the corresponding Q=0.07, f_o=800kHz, f_s=1.1MHz. From Figure 6. 35, the small-signal model matches very well with the experimental data.

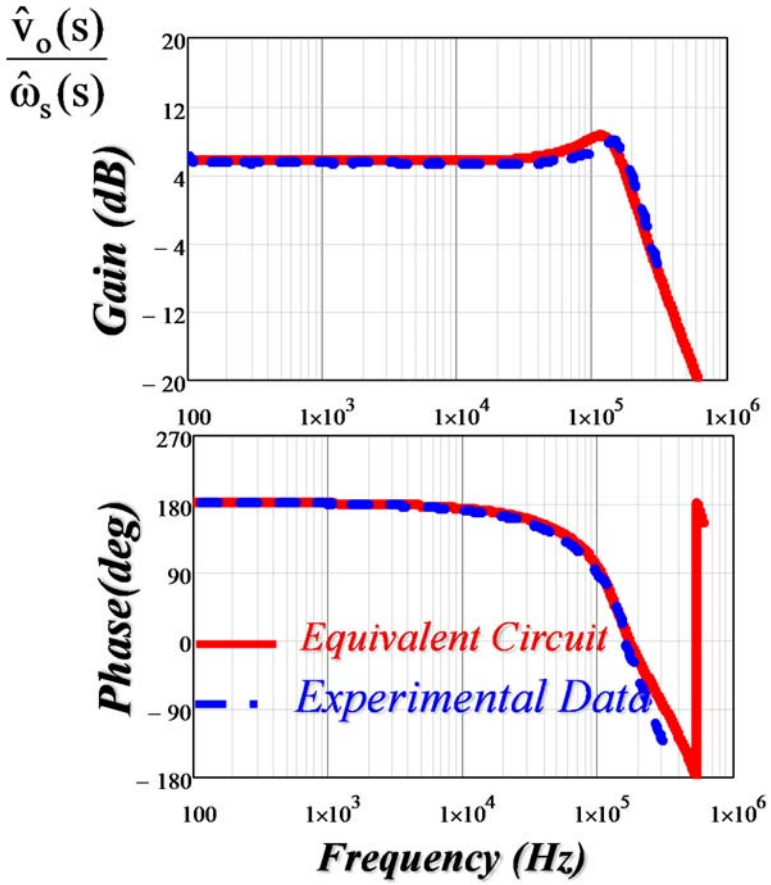


Figure 6. 35. Experimental verification of control-to-output transfer function.

6.5 Summary

This chapter proposes an equivalent circuit model for LLC resonant converter. When $F_s \geq F_o$, L_m is clamped by the output voltage and LLC behaves very similar as SRC. As a result, the dynamic behavior is similar as SRC: when switching frequency is larger than resonant frequency, the beat frequency double pole show up and the circuit is third-order; when switching frequency is close to resonant frequency, beat frequency double pole disappear and a new double pole formed by equivalent inductor L_e and equivalent output capacitor C_f show up. The circuit reduces to second order. When $F_s<F_o$, L_m participates in resonance and the circuit is essentially a multi-resonant structure. An approximated model is proposed where the equivalent resonant inductor is

modified to include the effect of L_m. As a result, the double pole will move to a little lower frequency. For the first time, analytical solutions are provided for all the transfer functions which are very helpful for feedback design. Simulation and experimental results verify that the equivalent circuit model can well predict the dynamic behavior when switching frequency is below, close to or above resonant frequency.

Chapter 7. Summary and Future Works

7.1 Summary

Distributed power system (DPS) is widely adopted in Power supplies for the telecom, computer and network applications. Constant on-time current mode control and V^2 control are widely used as POL converters and VR regulators in DPS systems. Series resonant converters are widely used in aerospace systems and LLC resonant converters are widely used as Front-end converters in DPS systems. The technological innovations bring increasing demand for optimizing the dynamic performance of the switching regulators in these applications. There has been a strong desire to develop simple and accurate equivalent circuit models to design these converters.

Current-mode control has been widely used in POL and VRM converters. For multi-phase application, external ramp is required to improve jittering performance using pulse distribution method. Chapter II analyzes the effect of external ramp on small-signal model of constant on-time current mode control. It is found that external ramp brings additional dynamics by introducing a moving pole and a static zero. Next, a three-terminal switch model is proposed based on non-ideal current source concept, where the non-idealness of the current source is presented by a R_{e2}-L_{e2} branch. Based on the proposed model, design guidelines are proposed based on either worst case design strategy or auto-tuning strategy.

V^2 control has advantages of simple implementation and fast transient response and is widely used in industry for Point-of-Load and Voltage Regulator applications. However, the capacitor voltage sideband effect, which casues the instability problem when ceramic capacitors are employed, also needs to be taken into consideration in modeling. Chapter III proposed a unified equivalent circuit model of V^2 control, the model is built based on non-ideal voltage source concept.

The model represents capacitor voltage sideband effect with a R_{e2}-L_{e2} branch, which forms the double pole by resonating with output capacitor. The equivalent circuit model is a complete model and can be used to examine all the transfer functions. Bsed on the unified equivalent circuit model, design guidelines for VR applications and general point-of-load applications are provided in Chapter IV, for both constant on-time V^2 control and constant frequency V^2 control.

For resonant converters, the small-sginal modelling is very challenging as some of the state variables do not have dc components but contain strong switching frequency harmonics and therefore the average concept breaks down. For SRC, the equivalent circuit model proposed by E. Yang in [E26] based on the results by the extended describing function concept is the most successful model. However, the order of the equivalent circuit model is too high and the transfer functions are still derived based on numerical solution instead of analytical solutions. Chapter V proposes a methodology to simplify the fifth-order equivalent circuit of SRC to a third-order equivalent circuit. The proposed equivalent circuit model can be used to explain the beat frequency dynamics: when switching frequency is far away from resonant frequency, beat frequency will occur; when the two frequencies are close, beat frequency will disappear and another double pole which is determined by equivalent inductor and output capacitor will be formed. For the first time, analytical solutions are provided for all the transfer functions which are very helpful for feedback design.

For LLC, no simple equivalent circuit model is available and no analytical expressions of transfer functions are presented. Chapter VI proposes an equivalent circuit model for LLC resonant converter. When $F_s \geq F_o$, L_m is clamped by the output voltage and LLC behaves very similar as SRC. As a result, the dynamic behavior is similar as SRC: when switching frequency is larger than resonant frequency, the beat frequency double pole show up and the circuit is third-order; when

switching frequency is close to resonant frequency, beat frequency double pole disappear and a new double pole formed by equivalent inductor L_e and equivalent output capacitor C_f show up. The circuit reduces to second order. When $F_s<F_o$, L_m participates in resonance and the circuit is essentially a multi-resonant structure. An approximated model is proposed where the equivalent resonant inductor is modified to include the effect of L_m. As a result, the double pole will move to a little lower frequency. For the first time, analytical solutions are provided for all the transfer functions which are very helpful for feedback design.

In conclusion, the works shown in this dissertation focus on small-signal equivalent circuit modeling for Buck converters with advanced control schemes and also resonant converters. The models are simple and accurate up to very high frequency range (1/2 f_{sw}).

7.2 Future Works

The research in this dissertation including the equivalent circuit models for constant on-time current mode control, V^2 control and resonant converters. The following research can be regarded as the future works:

1. For PWM converters: The equivalent circuit modeling for ramp pulse modulation (RPM) schemes [C41][C42]. RMP is another variable frequency control method and has better transient response compared with Constant-on-time control. However, the dynamic property is still unclear and no small-signal equivalent circuit model is available.
2. For resonant converters: The equivalent circuit modeling for other resonant converters, such as parallel resonant converter (PRC). For these resonant converters, the analytical transfer functions are still lacking and no simple equivalent circuit models are available for design.

Appendix A: Derivation of Non-coupled Equivalent Circuit Model for SRC

In this appendix, the superposition theorem is applied to derive a non-coupled equivalent circuit model, starting from the simplified third-order equivalent circuit model, shown as in Figure A. 1.

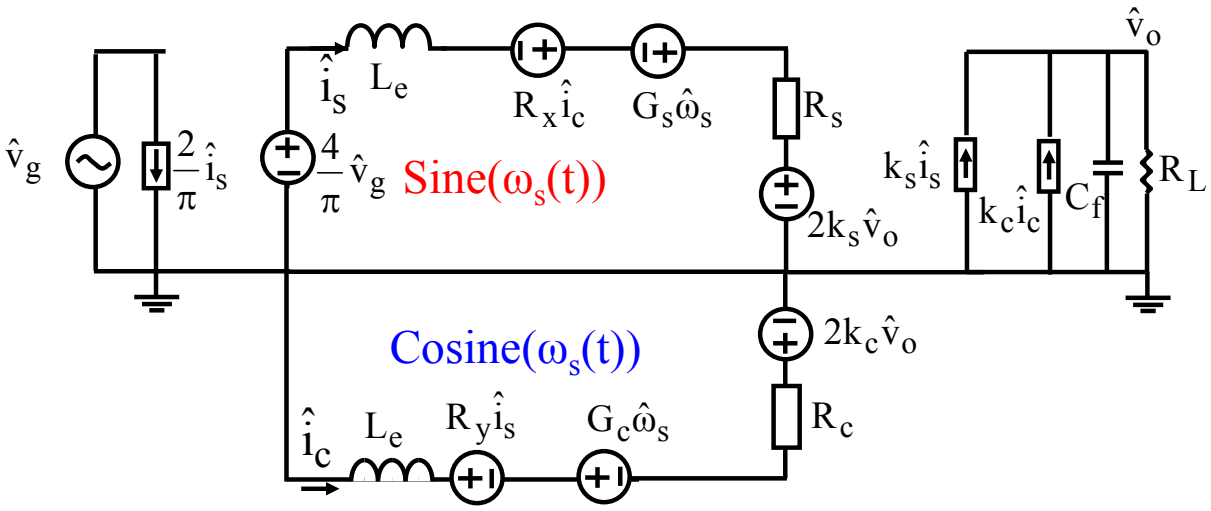


Figure A. 1. Simplified third-order equivalent circuit model of series resonant converter.

The output current is affected by the input voltage perturbation, output voltage perturbation and switching frequency perturbation, as shown in (A. 1):

$$\hat{i}_{rec}(s)=G_{vg}(s)\hat{v}_g(s)+G_{vs}\hat{\omega}_s(s)+G_{vo}(s)\hat{v}_o(s)$$
$$G_{vg}=\left.\frac{\hat{i}_{rec}(s)}{\hat{v}_g(s)}\right|_{\hat{v}_o=0,\hat{\omega}_s=0},G_{vs}=\left.\frac{\hat{i}_{rec}(s)}{\hat{\omega}_s(s)}\right|_{\hat{v}_g=0,\hat{v}_o=0},G_{vo}=\left.\frac{\hat{i}_{rec}(s)}{\hat{v}_o(s)}\right|_{\hat{v}_g=0,\hat{\omega}_s=0} \quad \text{(A. 1)}$$

G_{vg}, G_{vs} and G_{vo} are first derived separately using circuit techniques, then the total response of output current is obtained by adding the individual response.

Step 1: Derivation of G_{vg}.

The perturbation of v_o and ω_s are set to be zero for derivation of G_{vg}. Then Figure A. 1 can be simplified to Figure A. 2.

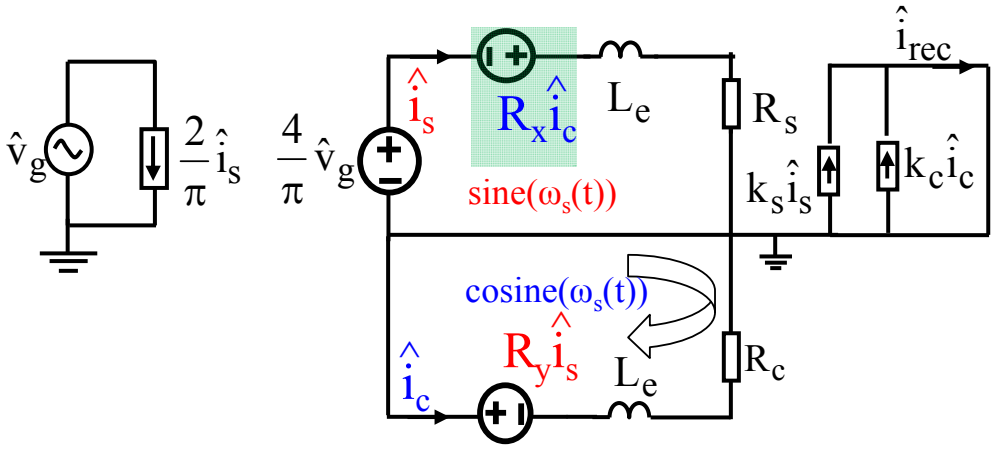


Figure A. 2. Equivalent circuit model for derivation of G_{vg}.

To decouple Figure A. 2, the focus is on the coupled term. Using KVL of cosine part circuit, the relation of sine part current and cosine part current can be derived, as shown in (A. 2).

$$\hat{i}_c = -\frac{R_y \hat{i}_s}{sL_e + R_c} \tag{A. 2}$$

Then the coupled voltage source controlled by cosine part current which is in light blue shade in Figure A. 2 can be expressed as (A. 3).

$$\begin{aligned} -R_x \hat{i}_c &= \hat{i}_s \left(R_{e1} // C_{e1}\right) \\ R_{e1} = \frac{R_x R_y}{R_c}&, C_{e1} = \frac{L_e}{R_x R_y} \end{aligned} \tag{A. 3}$$

Therefore, this voltage source can be replaced by an impedance comprised by an equivalent resistor and equivalent capacitor, shown as Figure A. 3. The coupling effect is represented by an equivalent R-C branch. From the output current point of view, the two output current source can be further combined and simplified, as shown in Figure A. 4.

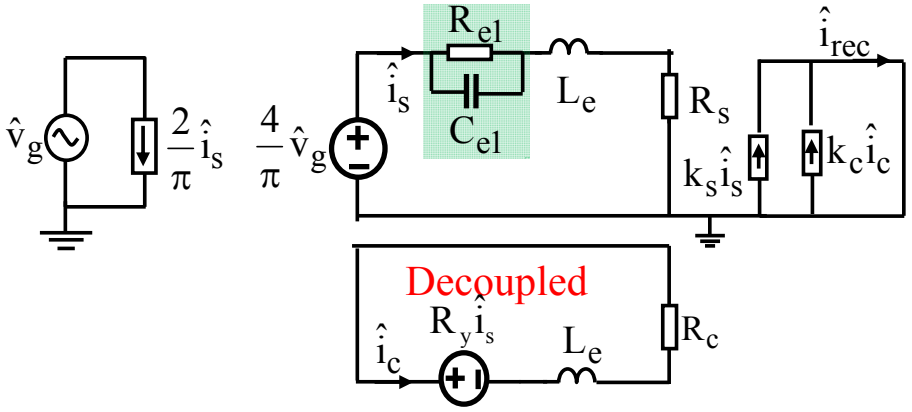


Figure A. 3. Equivalent circuit model using equivalent R-C branch for derivation of G_{vg}.

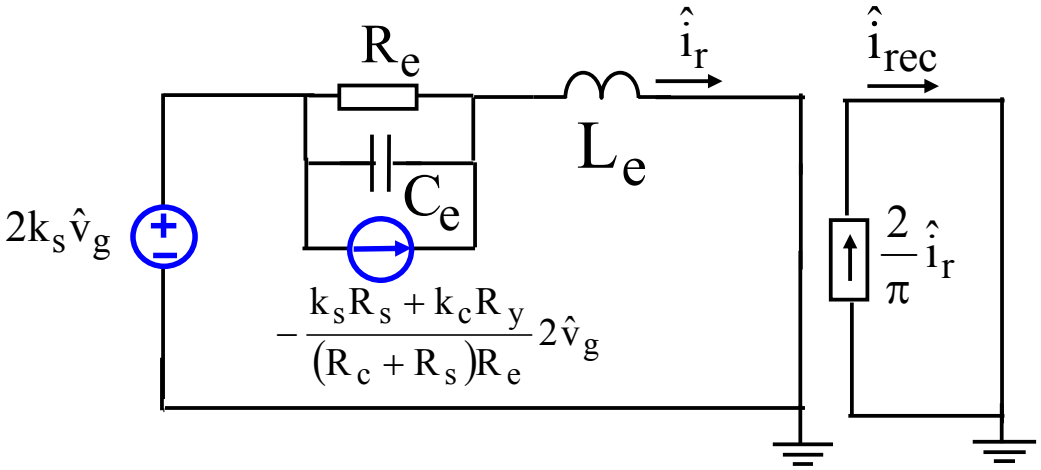


Figure A. 4. Non-coupled equivalent circuit model for G_{vg}.

The expressions of R_e and C_e are shown in (A. 4):

$$R_e = \frac{R_{el}+R_s}{1+R_{el}C_{el}R_s/L_e} = \frac{R_xR_y+R_sR_c}{R_s+R_c}$$
$$C_e = C_{el}\frac{R_{el}}{R_{el}+R_s} = \frac{L_e}{R_xR_y+R_sR_c} \quad \text{(A. 4)}$$

This concludes the first step.

Step 2: Derivation of G_{vs}:

The perturbation of v_o and v_g are set to be zero for derivation of G_{vs}. Then Figure A. 1 can be simplified to Figure A. 5:

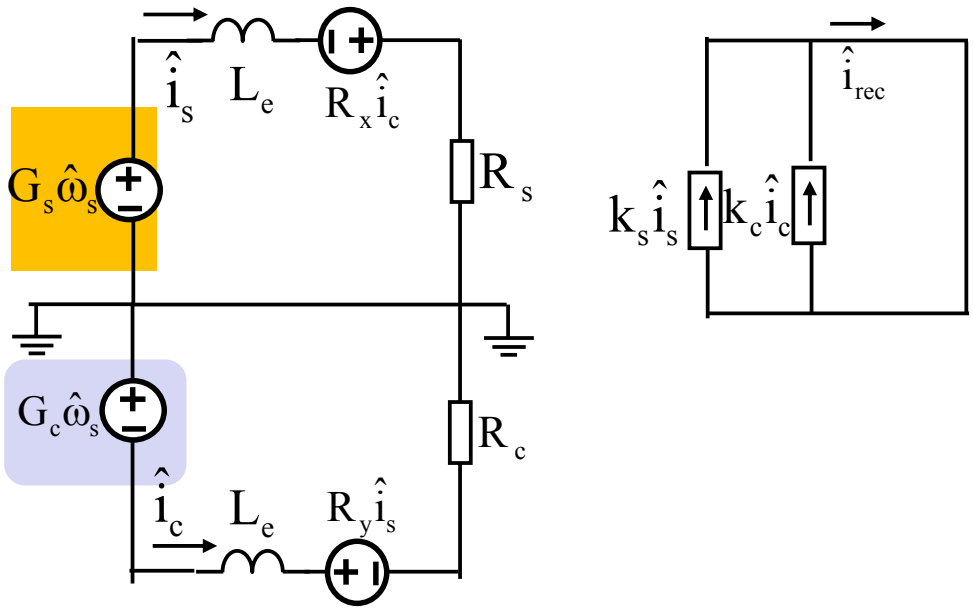


Figure A. 5. Equivalent circuit model for derivation of G_{vs}.

There are two controlled voltage sources related with perturbation of ω_s, one in sine branch and the other in cosine branch. Therefore, superposition theory can be used again in this step as the output current can be expressed as (A. 5).

$$\hat{i}_{rec}(s) = K_{Gs}G_s\hat{\omega}_s(s) + K_{Gc}G_c\hat{\omega}_s(s) \tag{A. 5}$$

For sine part voltage source, the derivation methodology is similar and the result is shown in Figure A. 6.

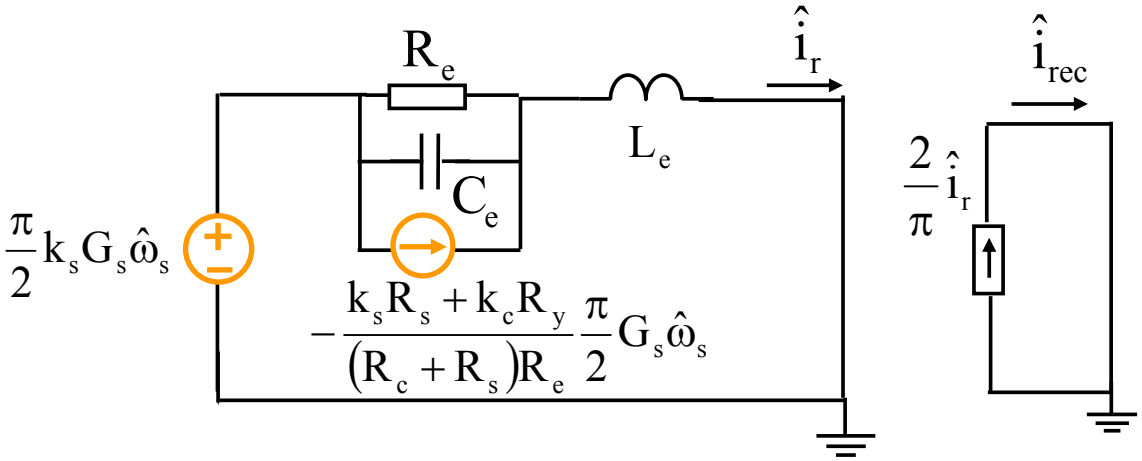


Figure A. 6. Non-coupled equivalent circuit model for sine part of Gvs: K_{Gs}.

For cosine part voltage source, the derivation methodology is similar and the result is shown in Figure A. 7.

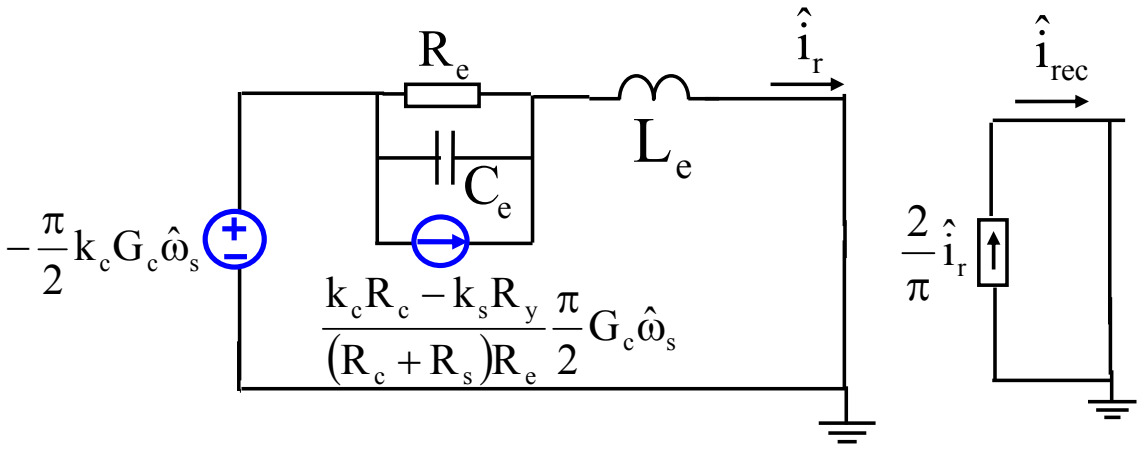


Figure A. 7. Non-coupled equivalent circuit model for cosine part of G_{vs}: K_{Gc}.

Combine Figure A. 6 and Figure A. 7, the non-coupled equivalent circuit model for G_{vs} is shown in Figure A. 8 and the expression of G_d is shown in (A. 6).

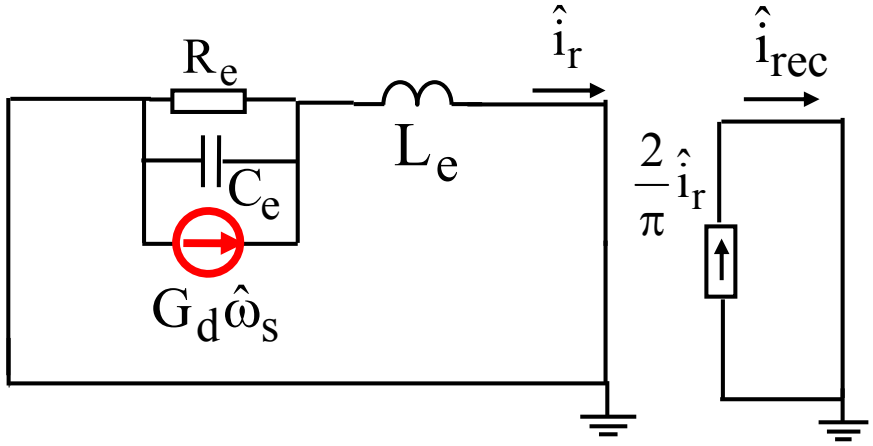


Figure A. 8. Non-coupled equivalent circuit model for G_{vs}.

$$G_d = -\frac{4}{\pi}\frac{V_g}{\Omega_s\sqrt{R_{eq}^{\ 2}+X_{eq}^2}}\frac{\Omega_s^2+\Omega_o^2}{\Omega_s^2-\Omega_o^2} \quad \text{(A. 6)}$$

This concludes the second step.

Step 3: Derivation of G_{vo}:

For derivation of G_{vo}, the scenario is exactly the same as derivation of G_{vs} except that the controlled voltage source is on the right side of the equivalent inductor instead of the left side. The result is shown as Figure A. 9.

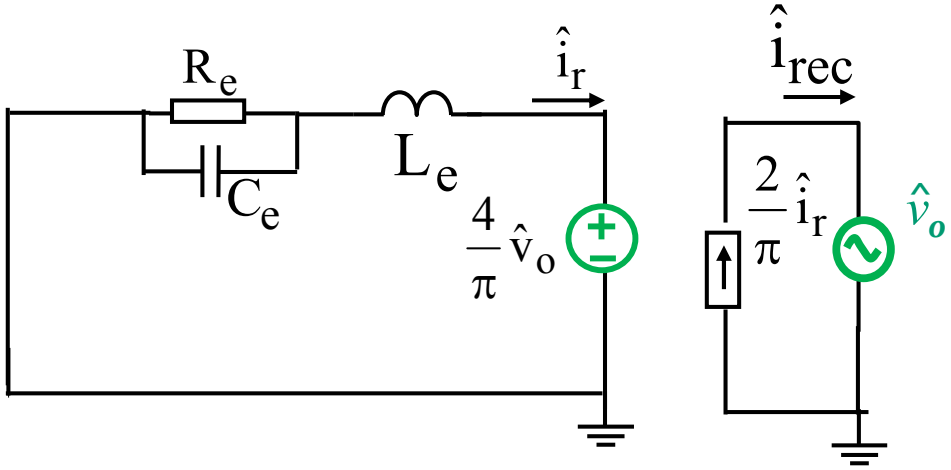


Figure A. 9. Non-coupled equivalent circuit model for G_{vo}.

This concludes the third step.

The final equivalent circuit model can be derived by combination of Figure A. 4, Figure A. 8 and Figure A. 9 using superposition theory. The final equivalent circuit is shown as Figure A. 10 and the expressions are shown in (A. 7). Note that Figure A. 10 is same as Figure 5. 17 and (A. 7) are same as (5. 13).

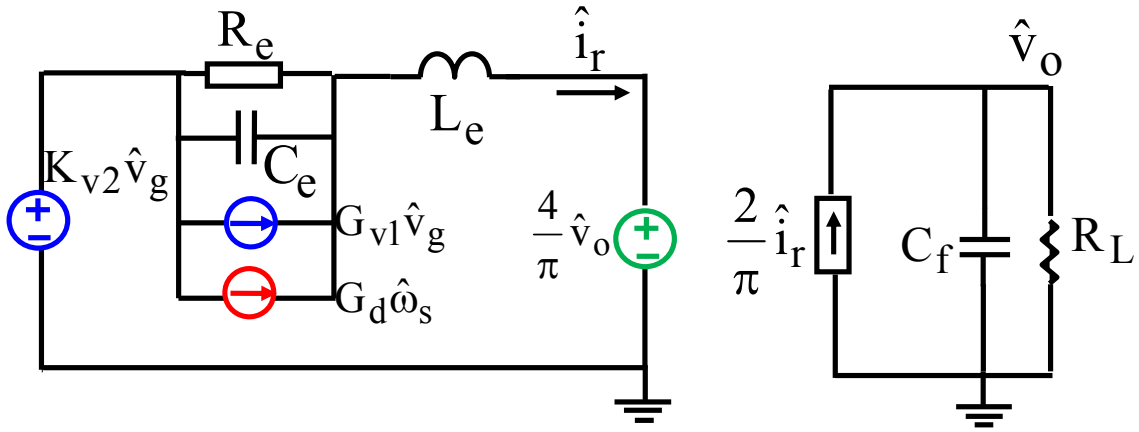


Figure A. 10. Final non-coupled equivalent circuit model for SRC.

$$L_e = L(1+\frac{\Omega_o^2}{\Omega_s^2}), C_e = \frac{1}{L_e(\Omega_s - \Omega_o)^2}, R_e = \frac{L_e|X_{eq}||\Omega_s - \Omega_o|}{R_{eq}}$$

$$G_d = -\frac{4}{\pi}\frac{V_g}{\Omega_s\sqrt{R_{eq}{}^2 + X_{eq}^2}}\frac{\Omega_s^2 + \Omega_o^2}{\Omega_s^2 - \Omega_o^2}, \quad \text{(A. 7)}$$

$$G_{v1} = \frac{2}{\pi}\frac{X_{eq}}{\sqrt{X_{eq}{}^2 + R_{eq}^2}}, K_{v2} = \frac{4}{\pi}\frac{R_{eq}}{\sqrt{X_{eq}{}^2 + R_{eq}^2}},$$

$$R_{eq} = \frac{8}{\pi^2}R_L, X_{eq} = \Omega_s L - \frac{1}{\Omega_s C}$$

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