

A TWO-MODE BUCK CONVERTER TOWARD HIGH EFFICIENCY FOR  
ENTIRE LOAD RANGE FOR LOW POWER APPLICATIONS

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## ABSTRACT

In order to extend the battery life of smart cameras, it is essential to increase the efficiency of power converters, especially at light load. This thesis research investigated a power converter to supply power for the microprocessor of a smart camera. The input voltage of the converter is 5 V, and the output voltage is 1.2 V with the load ranging from 10 mA (12 mW) to 1200 mA (1440 mW). The conventional buck converter is typically optimized for high efficiency at maximum load at the cost of light-load efficiency. A converter is investigated in this thesis to improve light load efficiency, while being able to handle heavy load, to prolong the battery life of smart cameras.

The proposed converter employs two modes, a baby-buck mode and a heavy-load mode, in which each mode is optimized for its respective load range to achieve high efficiency throughout entire range. The heavy-load mode converter adopts the conventional synchronous buck approach, as it generally achieves high efficiency at heavy load. However, the synchronous buck approach is inefficient at light load due to the large switching, driving, and controller losses. The proposed baby-buck mode converter employs the following schemes or technique to reduce those losses. First, the baby buck mode converter adopts pulse frequency modulation (PFM) with discontinuous conduction mode (DCM) to lower the switching frequency at light load, so frequency-dependent switching and driving losses are reduced. Second, a simple control scheme, constant on-time  $V^2$  control, is adopted to simplify the controller and hence minimize the controller power dissipation. Third, the top switch of the baby-buck mode uses a small MOSFET, which is optimized for light load, and the bottom switch uses Schottky diode in lieu of a MOSFET to simplify the COT  $V^2$  controller. Fourth, the proposed converter combines the heavy-load and baby-buck mode converter into a single converter with a shared inductor, capacitors, and the feedback controller to save space. Finally, a simple and low power feedback controller with an optimum mode selector, a COT  $V^2$  controller, and gate drivers are designed.

The optimum mode selector selects an appropriate mode based on the load condition, while shutting down the opposing mode.

The proposed converter was fabricated in CMOS 0.25  $\mu\text{m}$  technology in two phases. Phase 1 contains design of the proposed converter with open loop, and its functionality is verified through measurements of test chips. Phase 2 includes the entire converter design with the feedback controller. Since the test chips of phase 2 are not delivered, yet, its functionality during the steady state and transient responses are verified through simulations. Simulation results indicate that the efficiency of the proposed converter ranges from 74% to 93% at 12 mW and 1440 mW, respectively. This result demonstrates that the proposed converter can achieve higher efficiency for the entire load range when compared to an off-the-shelf synchronous buck converters.

*To my parents and grandmother*

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# Chapter 1

## Introduction

### 1.1 Motivation

Battery-powered devices such as car event data recorders (also called car black-box), cellular phones, cameras, and smart watches are ever growing. High efficiency of step-down converters to power microprocessors embedded in those devices is essential to increase the battery life and enhance the operation time. Those microprocessors are often operating under light load or in sleep state to save power. Therefore, higher efficiency converters under light load are particularly important.

The car black-box is a smart camera to record front and rear views of the car. The smart camera mostly stays in sleep mode while waiting for an event. Upon detection of an event, the camera wakes up to active mode and starts to record the video. When the scene does not have any further motion, it goes back to sleep mode to save power. Typically, the camera stays in the sleep mode for 80-90% of the operation time [1]. Since a car black box is powered by the car battery and operate mostly in sleep mode, enhancing the efficiency of the DC-DC converter, especially the efficiency of light load, is crucial for maximizing the run time of the black-box. The proposed research work in this thesis is to improve the light load efficiency of the step-down power converter for the microprocessor of the car black-box developed by Korean Advanced Institute of Science and Technology (KAIST) in Korea, while being able to handle heavy load efficiency.

### 1.2 Step-down DC/DC Converter

Figure 1.1 shows the general block diagram of a step-down DC/DC converter. Various

topologies for the power stage are available depending on input and load requirement and the feedback controller block regulates the output voltage. The common goal of all converters is to minimize the total power dissipation and hence improve the efficiency.

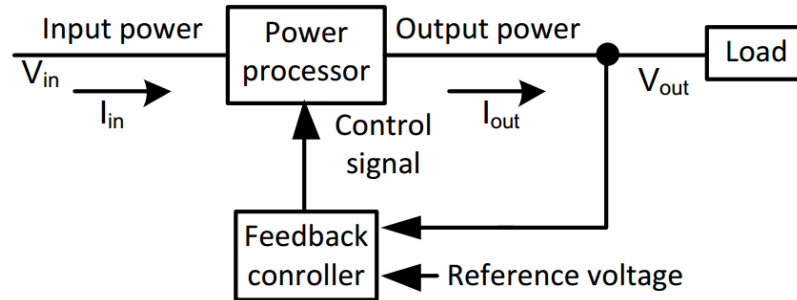


Figure 1.1: Block diagram for a power converter system from N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3<sup>rd</sup> ed. New Jersey: John Wiley & Sons Inc., 2003. Used under fair use, 2015.

The synchronous rectifier buck topology as the power stage and constant frequency pulse width modulation (PWM) as the control scheme are commonly used for a step down DC/DC converter. A synchronous rectifier buck generally achieves high efficiency for a low output voltage due to the small conduction losses of two MOSFET switches [3]. However, the conventional synchronous rectifier buck is optimized for heavy load efficiency, at the cost of light load efficiency. The light load efficiency suffers due to the higher conduction loss and gate driver loss [3]. In addition, the controller loss of the PWM voltage mode or current mode control is relatively small in comparison to load power for heavy load with relatively more power consumption. Nevertheless, the light load efficiency also suffers from the controller loss where the load power is no longer dominant at light load.

### 1.3 Technical Contributions of the Proposed Research

A DC/DC buck converter steps down an input voltage to a lower output voltage. Two stage approach is usually taken to step down a 12 V car battery input voltage down to lower voltages for a car black-box. The first stage steps the battery voltage down to a regulated 5 V for USB hosts and the camera. The second stage steps down the 5 V to various voltages including 1.2 V for the microprocessor. This thesis research focuses on the second stage DC/DC converter



with 5 V input voltage and 1.2 V output voltage. The major design objective of the proposed converter is to improve light load efficiency, while being able to manage heavy load efficiency.

A two modes converter, a heavy-load mode converter and a baby-buck mode converter, are proposed to achieve higher efficiency at both light load and heavy load. The synchronous rectifier buck with continuous conduction mode (CCM) operation optimized for heavy-load generally achieves higher efficiency at heavy load. Therefore, the proposed converter adopts conventional synchronous buck approach as heavy-load mode and adds a dedicated baby-buck mode which is used for light load operation to mitigate shortcomings of the conventional synchronous buck approach at light load. Therefore, both modes are optimized for its specific load range.

The following schemes or technique are proposed to increase the light load efficiency of the baby-buck mode, and they are the technical contributions of the research as following. First, the baby buck mode converter adopts pulse frequency modulation (PFM) with discontinues conduction mode (DCM) to lower the switching frequency at light load and hence reduce switching and driving losses. Second, the simplest control scheme, constant on-time (COT)  $V^2$  control, is adopted to minimize fixed losses from the control blocks. Third, the top switch of baby-buck mode use a small MOSFET optimized for light load and the bottom switch uses Schottky diode in lieu of a MOSFET to simplify the COT  $V^2$  controller by eliminating zero current detector (ZCD) control block so that the controller loss is reduced. Fourth, the proposed converter combines the heavy-load and baby-buck mode converter into a single converter with shared inductor, capacitors, and a feedback controller to save space. Last, a simple and low power dissipation feedback controller with an optimum mode selector, a COT  $V^2$  controller and gate drivers are designed. The optimum mode selector selects an appropriate mode based on the load condition, while shutting down the opposing mode. The COT  $V^2$  controller reduces switching frequency as load decrease at light load. The simple gate driver embeds build-in dead time by introducing different rise and fall time of the buffer.

The proposed converter was fabricated in CMOS 0.25  $\mu\text{m}$  technology with two phase, Phase 1 contains design of the proposed converter with open loop which was fabricated in February and its test chip demonstrates correct operation of the proposed design through measurement. Phase 2 includes the entire converter design with the feedback controller. Since

the test chips of phase 2 are not delivered yet. Its functionality is verified through simulation and the result indicates possibility to achieve better performance in comparison to other off-the-shelf converters.

## 1.4 Organization of the Thesis

The organization of the thesis is as follows. Chapter 2 provides background and preliminaries for the proposed research. This chapter discusses the design requirements of the car black-box smart camera applications, and review light load efficiency drawbacks of traditional synchronous buck converters along with downfalls of previous research activities on improving light load efficiency. The COT  $V^2$  control with DCM, which is adopted control scheme for proposed converter, is reviewed and compared to other control schemes. Finally, the advantages of integration are exhibited in this chapter. Chapter 3 presents design of the baby-buck mode converter, the heavy-load buck converter, and detailed block level operation of proposed converter with combination of the baby-buck and heavy-load mode converter. SIMPLIS simulation verifies system level functionality of the proposed converter with ideal components. Chapter 4 fully explains the off-chip components selection, the optimal size design of power MOSFETs, and the design of each IC building block used for the proposed converter. The final layout of the converter is also presented in this chapter. Chapter 5 presents simulated functionality and efficiency of the proposed converter with real components and measurement results of phase 1 are reported in this chapter. Lastly, Chapter 6 draws a conclusion on the proposed two-mode buck converter design and suggests directions for future research.

# Chapter 2

## Preliminaries

This chapter provides preliminary information and previous research works that are necessary to understand the proposed two-mode converter and the contributions of this thesis research. Section 2.1 describes the design requirements of the target car black-box's smart camera application. Section 2.2 reviews the traditional buck converter and its shortcomings at light load. Section 2.3 reviews an existing multiphase converter with a baby-buck, optimum number of phases (ONP) control and its drawbacks. Section 2.4 describes constant on-time control schemes. Section 2.5 provides Zhou's methods to improve light load efficiency. Section 2.6 discusses the shoot-through problem and the conventional solution. Section 2.7 illustrates the benefits of integration where the proposed converter is being integrated to have these benefits. Section 2.8 summarizes the chapter.

### 2.1 Design Requirements

The target smart camera system is powered by a regulated 5 V voltage source, in which the first stage converter steps down the car battery voltage from 12-14 V to 5 V. A microprocessor (Cortex-M3), with supply voltage of 1.2 V, dissipates power in the range from 12 mW to 1.44 W. Therefore, the proposed step-down converter for the microprocessor steps down 5 V to regulated 1.2 V. The output ripple must be within the processor input specification of 30 mV, with load transient requirement of 60 mV. The power block diagram for the target smart camera system is shown in Figure 2.1. The 3.3 V, 2.8 V, 2.5 V, and 1.8 V blocks are designed by Korea Advanced Institute of Science and Technology (KAIST), which adopts the single inductor multiple output (SIMO) approach. Each converter output is regulated independently and shares the same inductor to transfer energy to the load [4]. A 5 V to 1.2 V step-down converter in the figure is the interest of this thesis.

The main design objective of the proposed converter is to extend the battery life for the smart camera system. Therefore, it is important to design a high efficiency converter, especially for light load, as the processor is mostly in sleep mode. This leads to the major challenge of proposed converter, high efficiency for the entire range of the load. The proposed converter in this thesis is designed to achieve high efficiency at both heavy load and light load. A converter with small size and weight is also important for this car block box application.

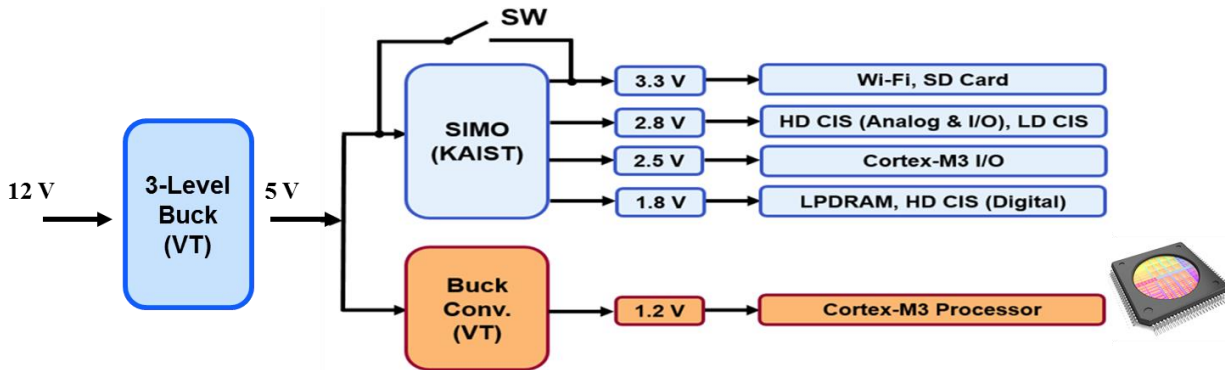


Figure 2.1: Power block diagram for target smart camera system from T. Yeago, *A Two-Mode Buck Converter with Optimum Mode Selection for Low Power Applications*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2014. Used under fair use, 2015.

## 2.2 Conventional synchronous buck converter

Voltage regulators can be realized using a linear regulator or a switching power supply, with the latter being more efficient and commonly used. A typical topology to step down a voltage is the buck converter. The switch is periodically on and off, so the input voltage is periodically connected to the inductor. The output voltage is therefore the average value of voltage at the switching node. The switching node is the node between the MOSFET and the diode and an asynchronous buck converter is shown in Figure 2.2. This topology has one active and one passive switch. When the input switch is closed, the inductor and the output capacitor are charged, and the load current is supplied by the input voltage source. The inductor and output capacitor supply the load when the switch is open. The charging and discharging of the inductor current and output capacitor voltage repeat in each switching cycle as the asynchronous buck converter works at steady state.

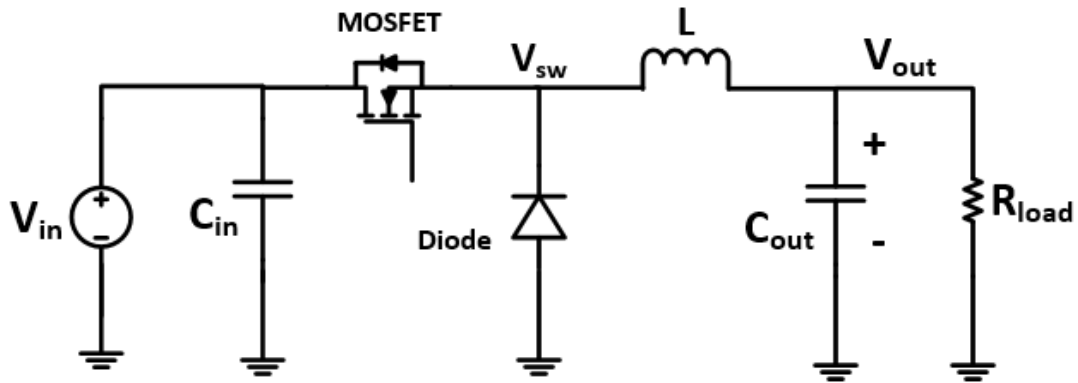


Figure 2.2: Asynchronous buck converter

The diode only allows the current to flow in one direction. Therefore, the inductor current generally operates in Continuous Conduction Mode (CCM) at heavy load and operates in Discontinuous Conduction Mode (DCM) at light load for an asynchronous buck converter. CCM operation refers to a power converter whose inductor current is always greater than zero during a switching cycle. Conversely, DCM operation refers to a power converter where the inductor current becomes zero during a certain period of a switching cycle. The crossover point between these modes is referred to as the critical boundary, and operating under this condition is referred to as boundary-conduction-mode (BCM). These operation conditions are illustrated in Figure 2.3 with the load current decrease from heavy to light [5].

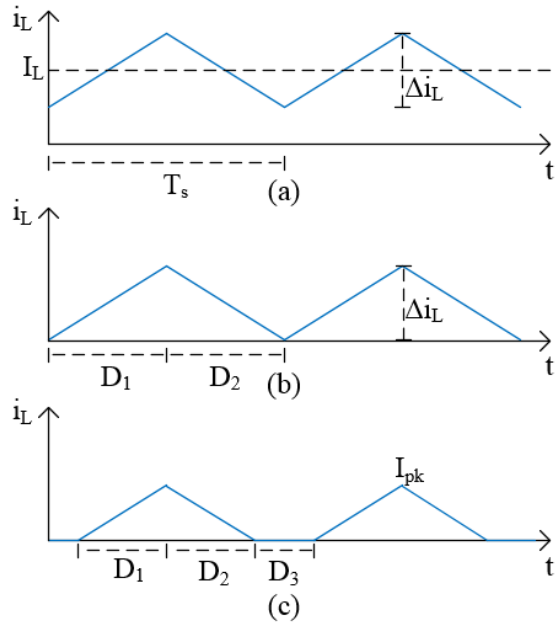


Figure 2.3: Inductor current waveforms (a) during CCM operation, (b) during BCM operation, and (c) during DCM operation from T. O'Connor, *Power Management Circuit Design for Vibration Energy Harvesting from Freight Railcars*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2015[5]. Used under fair use, 2015.

### 2.2.1 Synchronous buck converter

Replacing the diode with a MOSFET forms another topology of buck converters. This topology shown in Figure 2.3 is called a synchronous buck converter. The switching signal on the bottom MOSFET is commonly complementary of the top MOSFET switching signal.

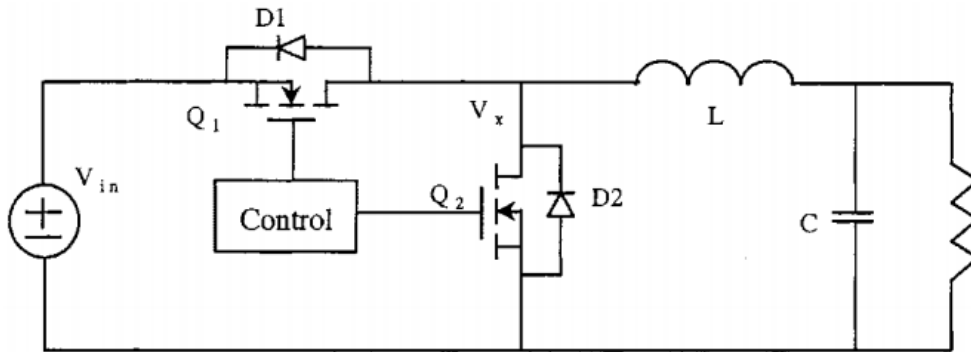


Figure 2.4: Synchronous buck converter from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in

Most low-output-voltage DC/DC converters use the synchronous rectifier buck topology to increase the efficiency by reducing the high conduction loss of a diode to the relatively small conduction loss of a MOSFET [3]. The basic operation of both asynchronous and synchronous buck converters is similar at heavy load. However, due to the bi-directional conduction of the MOSFET, the synchronous buck still operates in CCM at light load without additional control. The operation conditions of a synchronous buck converter are illustrated in Figure 2.5 with the average load current decrease from heavy to light.

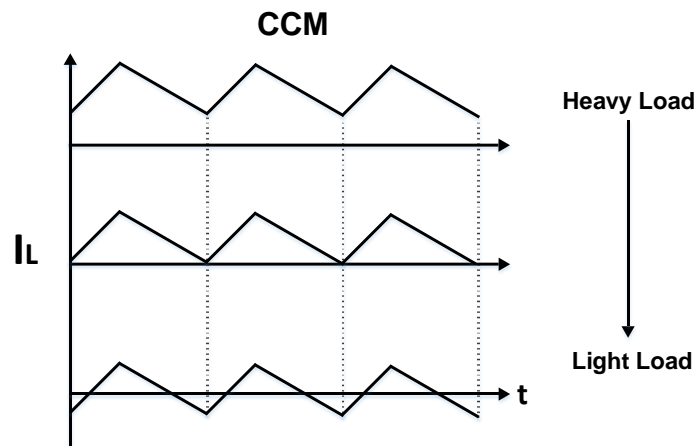


Figure 2.5: The inductor current waveform of a synchronous buck converter when load current decreases to light load

Fixed frequency Pulse Width Modulation (PWM) is often used for heavy load. Typically, a buck converter is optimized for high efficiency at heavy load. Therefore, synchronous buck converter with PWM and operates in CCM is widely adopted topology for power converters. CCM operation is desired for heavy load operation as it achieves higher efficiency than DCM operation due to a smaller RMS inductor current [6]. However, a buck converter generally adopts variable frequency Pulse Frequency Modulation (PFM) to reduce switching frequency for light load and hence to increase light load efficiency. A PFM control scheme reduces the switching frequency in proportional to the load current as shown in Figure 2.6. As a result, the switching loss and driving loss associated with the switching frequency reduces.

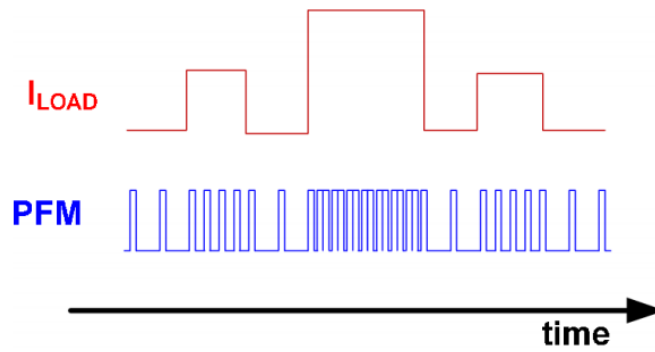


Figure 2.6: PFM signal with respect to load current variation from V. G. Madhuravasal, *Extreme Temperature Switch Mode Power Supply based on Vee-square Control Using Silicon Carbide, Silicon on Sapphire, Hybrid Technology*, Ph.D. dissertation, ECE, Oklahoma State University, Stillwater, OK, 2009. Used under fair use, 2015.

### 2.2.2 Shortcomings of Synchronous Buck

The major limitation of a synchronous buck with PWM is low efficiency at light load due to higher conduction loss and gate drive loss. For a synchronous buck, the two MOSFET switches are complementarily and hence its inductor current can be negative at light load as shown in Figure 2.5. Negative current incurs the circulating energy, which leads to a larger conduction loss and lower efficiency at light load [3]. Besides, the relatively fixed controller loss, gate drive loss and switching loss is no longer negligible as load becomes small. A synchronous buck converter with PWM leads low efficiency at light load.

A synchronous buck power stage optimized for heavy load costs the light-load efficiency. This is because the MOSFET switches are designed to have low  $R_{dson}$  to minimize the conduction loss for heavy load. The conduction loss can be calculated using Equation (1). However, smaller  $R_{dson}$  leads to higher gate charge  $Q_g$ . The Figure of Merit (FOM), the most significant indicator of MOSFET performance, shown in Equation (2) would remain the same. Higher gate charge results in higher gate driving loss and switching loss as shown in Equation (3) and (4). Switching losses are created as a result of a simultaneous exposure of a MOSFET to high voltage and current during a transition between the high and low states. The gate driving loss is the lost energy used to charge and discharge the gate capacitance of the MOSFET at each switching event.



$$P_{cond} = I_{load}^2 * R_{dson} \quad (1)$$

$$FOM = Q_g * R_{dson} \quad (2)$$

$$P_{gate} = Q_g * F_{sw} * V_{gs} \quad (3)$$

$$P_{sw} = \frac{1}{2} V_{in} * I_{out} * F_{sw} * \frac{Q_g}{I_{driver}} \quad (4)$$

At heavy load, the conduction loss dominates due to the high  $I_{load}$ . At light load, the gate driving loss and switching loss dominate due to the relatively small conduction loss. Figure 2.7 shows the loss breakdown versus load. A small  $R_{dson}$  is desired for full load to reduce conduction loss. Conversely, at light load, small  $Q_g$  is desired to reduce the gate driving loss and switching loss. There is a tradeoff between  $R_{dson}$  and gate charge to achieve highest possible efficiency for the targeted load range.

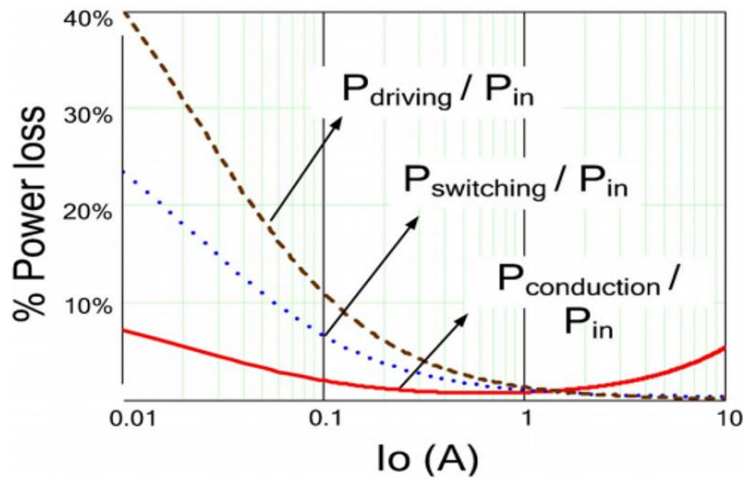


Figure 2.7: Losses breakdown vs. load from T. Yeago, *A Two-Mode Buck Converter with Optimum Mode Selection for Low Power Applications*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2014. Used under fair use, 2015.

The proposed converter adopts a converter with two-modes due to the tradeoff mentioned above. The heavy-load mode adopts the synchronous buck converter approach for high efficiency at heavy load, and baby-buck mode adopts PFM control with DCM operation to reduce switching frequency, implements a simple controller to save controller loss, and optimizes baby-buck power switches for higher efficiency at light load.

## 2.3 Wei's Multiphase converter with baby-buck and ONP Control

Wei proposed a two stage buck converter for the laptop voltage regulator applications shown in Figure 2.8. The first stage generates a bus voltage to allow a lower voltage conversion for the second stage. Typically, a two stage buck converter is more efficient for a larger step down conversion ratio. The first stage steps down from 9 – 19 V to 6 V, and the second stage from 6 V to 1.3 V. This laptop application has a voltage regulator to provide 60 W of power.

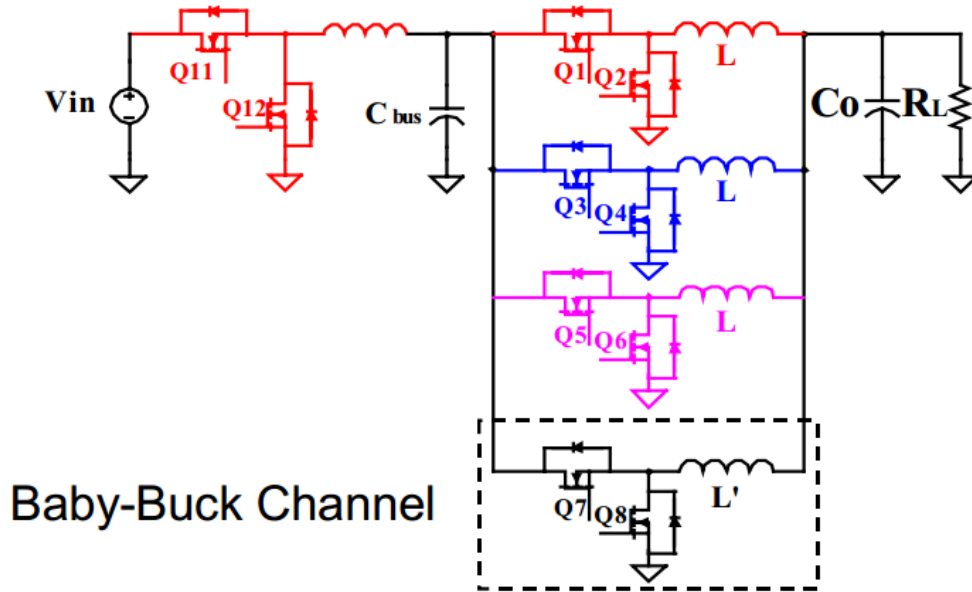


Figure 2.8: Three phase converter with baby-buck phase from J. Wei, *High Frequency, High Efficiency Voltage Regulators for Future Microprocessors*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

Wei introduced a multiphase converter including a baby-buck phase for the second stage step down conversion. This multiphase converter shares current between all modes, reducing stress placed on components. When all phases are active, it becomes inefficient at light load. A four-phase converter with a dedicated baby-buck phase improves the light load efficiency. The baby-buck converter is always active, while an optimal number of phases (ONP) is selected dynamically depending on the load current [8]. Upon light load, less than 3A for Wei's design, the baby-buck phase is active and all other phases shut down to improve efficiency. For heavy load, the baby-buck phase is still active with a current limiting function, while other phases share the remaining current. The constant frequency control is considered for this multiphase

converter, and the baby-buck channel is realized using a monolithic buck converter, TI's TPS54612 [9]. Figure 2.9 demonstrates the improved light efficiency with this approach.

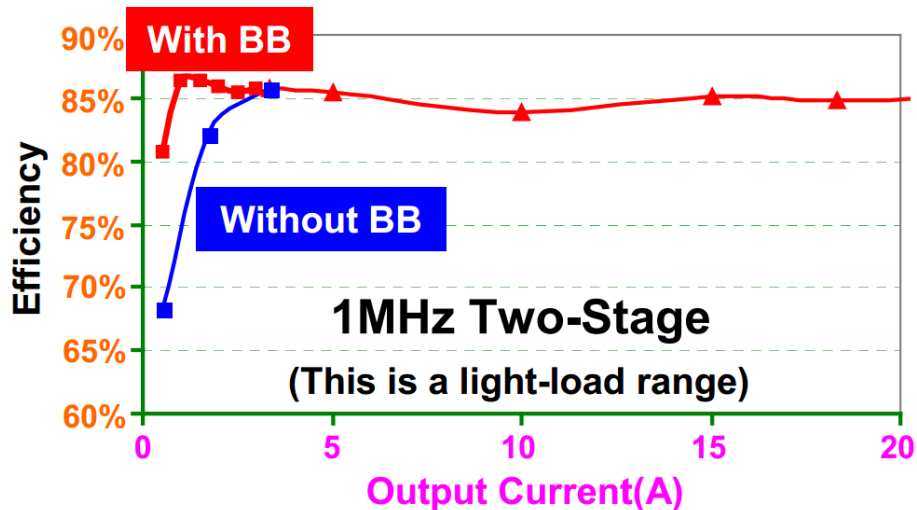


Figure 2.9: Efficiency comparison with and without baby-buck concept from J. Wei, *High Frequency, High Efficiency Voltage Regulators for Future Microprocessors*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

Dynamically change of the number of phases is explored further in [10], focusing on design issues for practical implementation. Design issues include uneven current sharing upon connecting phases and poor transient performance during load variations when disconnecting and connecting phases.

### 2.3.1 Shortcomings of Wei's Design

There are two major limitations of Wei's design when adopted by low power applications such as the target application with maximum power of only 1.4 W. The first drawback is the phase shedding approach with ONP control, and the second limitation is the constant frequency approach for the baby-buck phase.

Wei uses optimum number of phases (ONP) control or phase shedding approach where the number of active phases reduces with decrease of load current [8]. Losses from the controllers of multiple active phases are relatively small compared to load power considered for Wei's high power applications. However, efficiency can suffer for low-power applications, where load power is no longer dominant. The power consumed by the baby-buck controller and its

MOSFETs become apparent at medium to heavy load of the targeted low power application (< 1.4 W). For example, if the sum of switching losses, gate driving losses, conduction loss and controller losses of baby-buck is 10 mW, the efficiency will suffer by 4% at 250 mW load and by 0.7% at 1.4 W full load. Therefore, it is necessary to reduce the losses from the baby-buck phase for medium to heavy load. The second drawback is that the number of inductors, controllers and gate drivers is equal to the total number of phases, and inductors and controllers are bulky and lossy.

The constant frequency control of 1 MHz with CCM makes the converter inefficient for very light load. For light load condition under CCM, unnecessary loss results from the reverse conduction of the inductor current. Also, 1 MHz switching frequency results in large gate driving loss and switching loss. In addition, the constant frequency controls are usually complicated to result in complex controller blocks and hence relatively large power dissipation. The 13 mW quiescent controller loss from TI TPS54612 is insignificant for Wei's target application, but significant for the target application at the light load (12 mW). The controller loss significantly impacts the light load efficiency.

PFM control reduces the switching frequency as load current decreases and hence reduces the loss associated with switching frequency. A simpler control scheme with a simple controller also reduces the controller power dissipation. Therefore, the proposed converter adopts PFM control and implements a simple controller to improve light load efficiency.

## 2.4 PFM control schemes

For applications mostly operating at light load or sleep mode, PFM is more efficient than PWM due to a lower switching frequency at light load. For a synchronous buck converter, PFM control can only be realized under DCM, when the average inductor current is less than half of its peak-peak current ripple. DCM requires turning off the synchronous MOSFET to prevent the reverse conduction of the inductor current, which causes additional losses. During the on state, the inductor current is charging from the source. During the off cycle, the inductor current discharges its energy into the load until it reaches zero. An inductor current zero crossing detector detects this instance, and the gate driver shuts down the synchronous MOSFET to block

the reverse current and to operate in DCM. Both top and bottom switch are turned off while the output capacitor provides energy to the load. When both switches are off, there is no loss during this period. PFM control in DCM reduces the switching frequency in proportion to the load current. DCM is naturally realized for an asynchronous buck converter due to blocking of the reverse inductor current by the diode. A shortcoming of asynchronous buck converters is higher conduction loss due to larger forward voltage drop across the diode during inductor discharging.

A reduced switching frequency lowers gate driving losses, switching losses,  $C_{oss}$  losses, reverse recovery losses, and other switching related losses for both switches. Thus, efficiency can be improved under light load.

Popular PFM methods adopted by industry in recent years are constant on-time (COT) and constant off-time control [11][12]. Both schemes allow the switching frequency to vary, and a one-shot timer triggers a constant on or off pulse. The name of each control scheme refers to the top switch status. For COT control, the top switch is on for a designated period, the off time is modulated. For constant off-time control, the top switch is off for a designated period, the on-time is modulated. COT control tracks the valley threshold value. Once the detected value is below the threshold, a COT pulse is generated to turn on the top switch for the designated period as shown in Figure 2.10. Conversely, constant off-time control tracks the peak threshold value. Constant off-time control uses trailing edge modulation, resulting in delayed transient performance for load step-up [13]. Thus, COT control is generally more preferred by industry. In addition of reduction of the switching frequency at light load, COT control requires only a comparator for feedback loop rather than an oscillator, an error amplifier and a compensator required for conventional PWM control. Thus, COT control leads to a simple implementation to save many building blocks.

COT control can be realized with two distinct control methods, current mode control and voltage mode control. The former compares the inductor current with the reference value and the latter the output voltage with the reference value as shown in Figure 2.10. COT current mode control is more complex, because it requires sensing the inductor current ripple and compares with error information generated by voltage compensator. The advantage of current mode control is small output capacitor and low ESR output capacitance without introducing stability issue. Current mode controls are advantageous if the application requires the inductor current

information. For the target application, the inductor current information is unnecessary, and the loss of the inductor current sensor is not negligible. The proposed converter adopts the voltage sensing scheme called  $V^2$  control, which is described in detail in the following.

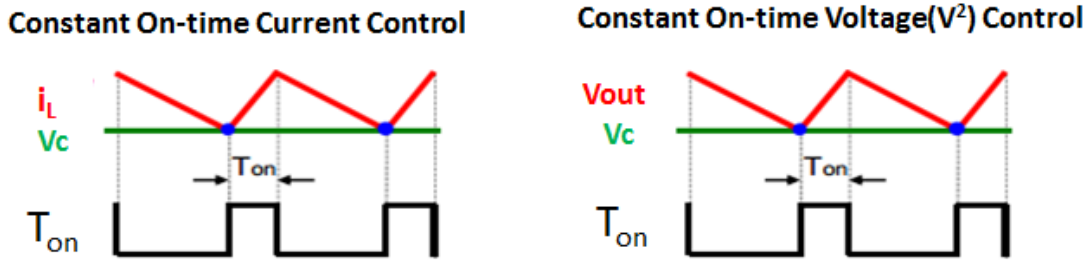


Figure 2.10: Two different implementation schemes of COT control from S. Tian, *Small-signal Analysis and Design of Constant-on time  $V^2$  Control for Ceramic Caps*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

#### 2.4.1 Constant-on time $V^2$ Control

The COT  $V^2$  control scheme captures the inductor current information through sensing output voltage. As shown in Figure 2.11, the architecture of a COT  $V^2$  control, the output voltage is sum of the voltage across the Equivalent Series Resistance (ESR) of capacitor and the voltage of the capacitor. The capacitor voltage stays nearly constant which represents the DC output voltage. The capacitor ESR ripple voltage is generated by the inductor current charging and discharging.  $V^2$  control utilizes the ESR ripple voltage to acquire the inductor ripple information from the output voltage.

The advantage of  $V^2$  control is its ultra-fast transient performance as shown in Figure 2.11. There are two voltage feedback loops for  $V^2$  control. The inner loop directly feeds the voltage signal into the modulator and the outer loop sends the voltage signal through a compensation network to generate the error information. The primary purpose of the outer loop is to eliminate the steady state error which equals to half of the output voltage ripple [14]. For applications where the steady state error is not critical, the outer loop can be omitted as described in [15][16].

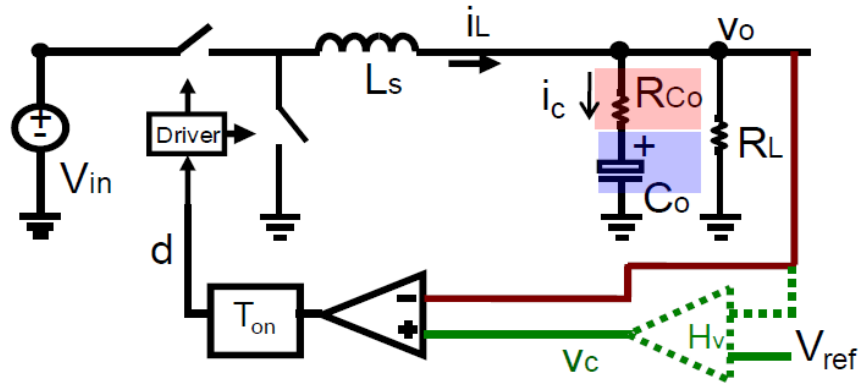


Figure 2.11: The architecture of a COT  $V^2$  control from S. Tian, *Small-signal Analysis and Design of Constant-on time  $V^2$  Control for Ceramic Caps*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

When the output voltage changes due to the disturbance either from the input voltage or the load variations, the controller responds immediately. This is because the output voltage is directly connected to the controller through the inner feedback loop. Hence, COT  $V^2$  control has faster load transient response than COT current mode control in which the controller is connected to the current sensor. An ultra-fast transient response of the  $V^2$  control is illustrated in [17].

Another advantage of  $V^2$  control compared with the current mode control is easy implementation thanks to its simplicity over current mode control. First, the  $V^2$  control does not require a current sensor network as shown in Figure 2.11, which eliminates an inductor current sensing IC, a sense resistor, or a DCR current sensing network [18]. Second, current mode control requires a compensation network to improve the bandwidth and stability margin, where the bandwidth of  $V^2$  control is naturally up to half of its switching frequency. Figure 2.12 shows the stability bode-plot comparison between COT current mode control on left and COT  $V^2$  control on right. The bandwidth of COT  $V^2$  control is obviously higher as the bandwidth of COT current mode control is only few kHz before compensation. The complex compensator network can be eliminated for  $V^2$  control. Due to the advantages, COT  $V^2$  control is widely employed in industry [19][20][21][22][23]. Light load efficiency can be improved by COT control.

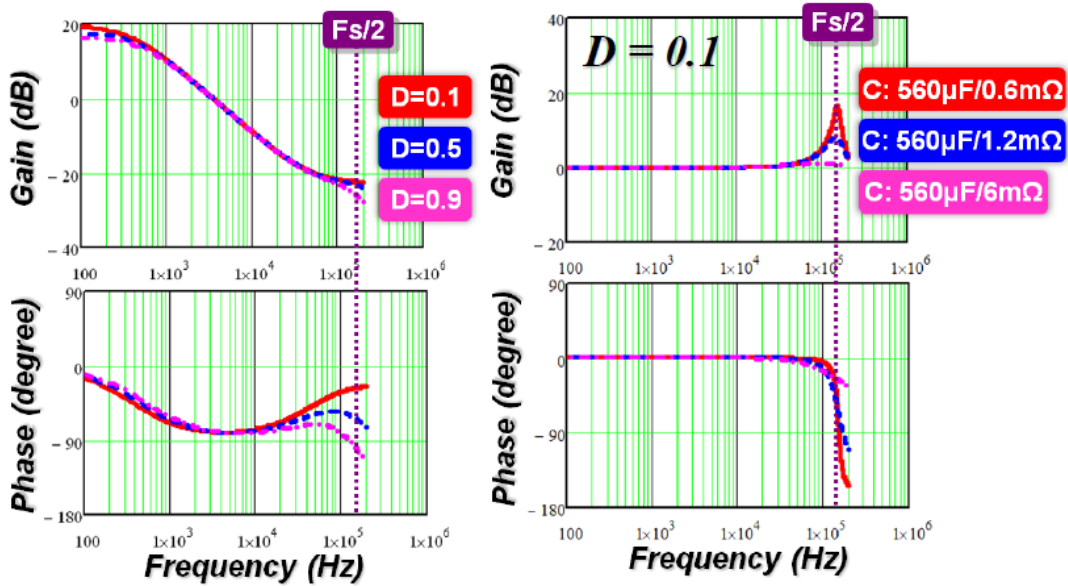


Figure 2.12: The stability bode-plot comparison between current mode control on left and  $V^2$  control on right from S. Tian, *Small-signal Analysis and Design of Constant-on time  $V^2$  Control for Ceramic Caps*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

Although  $V^2$  control has several advantages over current mode control,  $V^2$  control may suffer from instability if the voltage ripple on the capacitor ESR is not sufficiently large. As shown in Figure 2.13, the sensed output voltage contains two parts: The red triangular waveform is the ESR voltage ripple. The inductor current ripple flows through the ESR resistor and hence generates ESR voltage ripple, so the ESR ripple voltage represents the inductor current ripples information which can be used to modulate the switching signal. The blue waveform is the capacitor voltage as the second part of the output voltage. This voltage is formed by integration of the current flow through the capacitor, and this voltage has 90 degree phase delay compared with ESR ripple information. Therefore, the information of the output voltage fed into controller is not only the inductor ripple current, but also the capacitor voltage ripple. When ESR ripple dominates the capacitor ripple, the output voltage well represents the inductor current information and the circuit is stable.



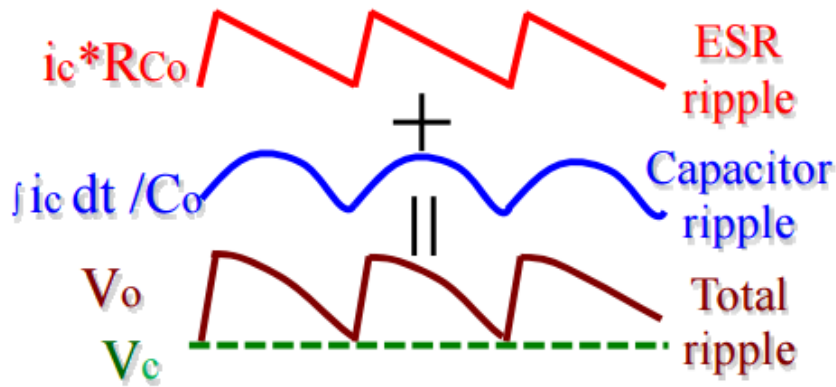


Figure 2.13: Output Voltage waveform of  $V^2$  control from S. Tian, *Small-signal Analysis and Design of Constant-on time  $V^2$  Control for Ceramic Caps*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

However, when the capacitor ripple dominates the ESR ripple shown in Figure 2.14, sub-harmonic oscillation can be observed due to the phase delay of the capacitor [14]. The output voltage cannot reflect true inductor current information, and the circuit is no longer stable. So, in order to stabilize the system, it is critical to design the output capacitor to ensure the ERS ripple dominates the capacitor ripple.

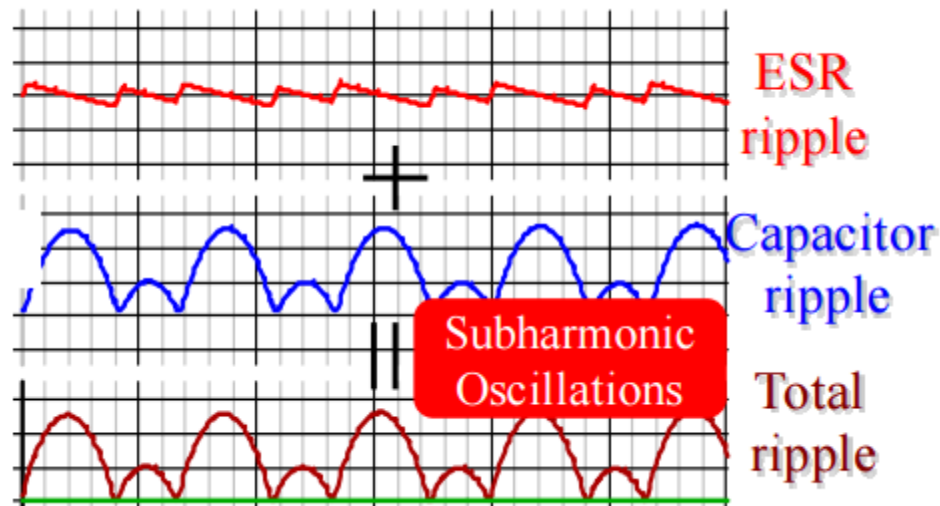


Figure 2.14: Output Voltage waveform of  $V^2$  control with sub-harmonics from S. Tian, *Small-signal Analysis and Design of Constant-on time  $V^2$  Control for Ceramic Caps*, M.S. thesis, ECE, Virginia Tech, Blacksburg, VA, 2004. Used under fair use, 2015.

COT  $V^2$  control is chosen for the proposed converter due to its ability to modulate the switching frequency, increasing light load efficiency, simple implementation, and ultra-fast transient response. To ensure stability of the system, selection of a right capacitor is the key design issue, which is discussed in section 4.1.

## 2.5 Zhou's Approaches to improve light load efficiency

Zhou discussed major drawbacks in light load efficiency for the synchronous buck converter topology [3]. Zhou attempted to improve the light efficiency by introducing four different methods. Three of Zhou's best attempts to improve light load efficiency are discussed in this section. Zhou's first approach uses a Schottky diode in parallel with the bottom MOSFET [3]. Figure 2.15 shows the schematic of the proposed converter, which operates in constant switching frequency (specifically PWM) at heavy load. The bottom MOSFET is shut down completely when the average load current decreases below a threshold value. The threshold value is based on the inductor current by determining when the inductor current begins to reverse in direction or load current enters light load. When the bottom MOSFET is completely off, the Schottky diode has much lower forward voltage drop than the body diode of the bottom MOSFET. So the inductor current flows through the Schottky diode which effectively becomes an asynchronous buck converter. Complete shutdown of the bottom MOSFET reduces the driving loss of the converter. Figure 2.15 compares the efficiency between normal CCM operation and DCM operation with the Schottky diode.

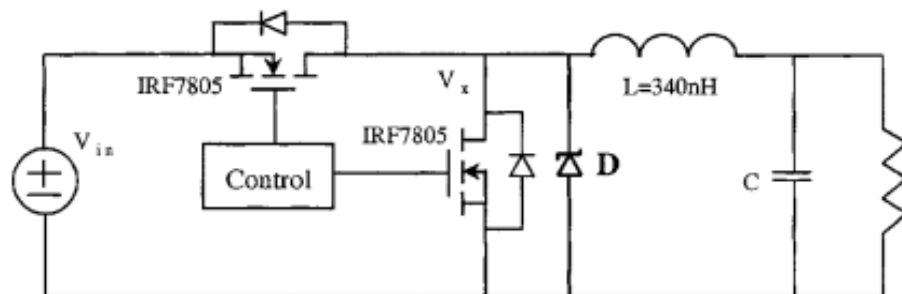


Figure 2.15: Schematic of Zhou's hybrid technique converter from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage

Regulator Module," in *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826-834, 2000. Used under fair use, 2015.

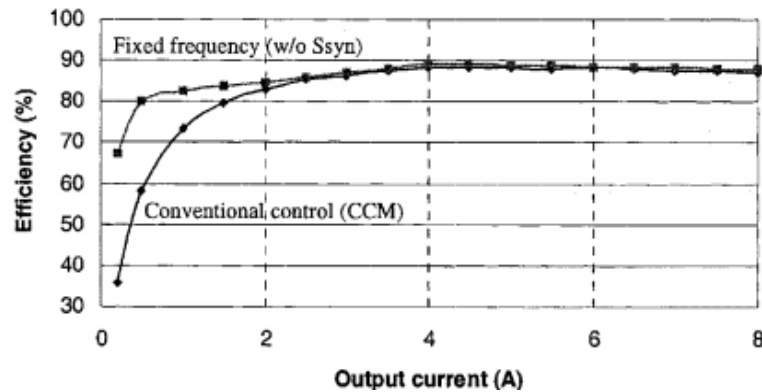


Figure 2.16: Efficiency of CCM and Schottky diode DCM (w/o Ssyn) from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826-834, 2000. Used under fair use, 2015.

The second approach, called a hybrid mode control, further improves the light load efficiency [3]. Like the first approach, the hybrid mode operates at the constant frequency above the threshold load current. As the load decreases below the threshold load current, the bottom MOSFET shut down completely and the parallel Schottky diode carries the load current. Differing from the first method, the switching frequency of the top MOSFET decreases according to the load current. This is achieved by utilizing the pulse frequency modulation (PFM), which is aforementioned in section 2.2. As the switching frequency decreases, switching loss and gate driving loss and other losses associated with frequency also reduces. Figure 2.17 shows improvement of the light load efficiency for the hybrid method, owing to reduction of the switching frequency at light load. The converter achieves better light load efficiency than the first Schottky diode with fix frequency DCM approach and much higher efficiency than conventional CCM approach respectively.

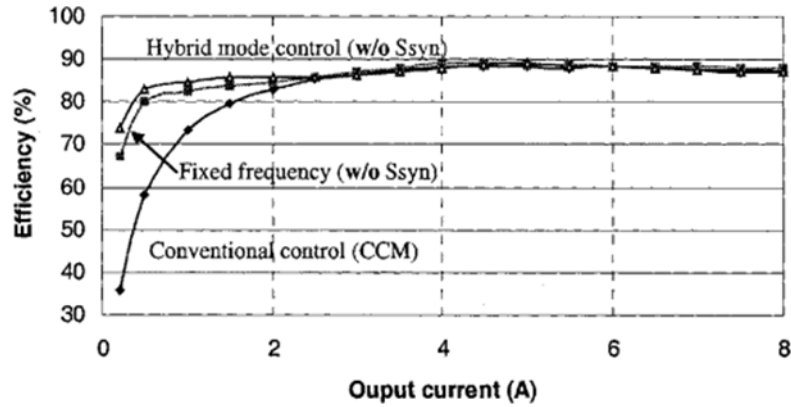


Figure 2.17: Efficiency comparison among different approaches from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826-834, 2000. Used under fair use, 2015.

The third approach eliminates the parallel Schottky diode and further improves efficiency by switching the bottom MOSFET appropriately. When the inductor current reaches zero, the controller turns off the bottom MOSFET. And the bottom MOSFET turns on again after the top MOSFET turns off, repeating the same process. This approach adopts PFM to reduce frequency and eliminates the Schottky diode to reduce the conduction loss from the forward drop across the Schottky diode. Figure 2.18 shows the efficiency of the third approach annotated as “hybrid mode control (w/ Ssyn)” compared to conventional control (CCM) and the hybrid diode approaches annotated as “Hybrid mode control (w/o Ssyn)”. The drawback of this approach is that the converter requires more complex controller to detect the zero crossing point of the inductor current and smartly controlling the synchronous MOSFET. The extra controller block loss is smaller than Schottky diode conduction loss for Zhou’s 0.2 Amp light load case, but it may not be the case as the load decreases to 10 mA for the target application.

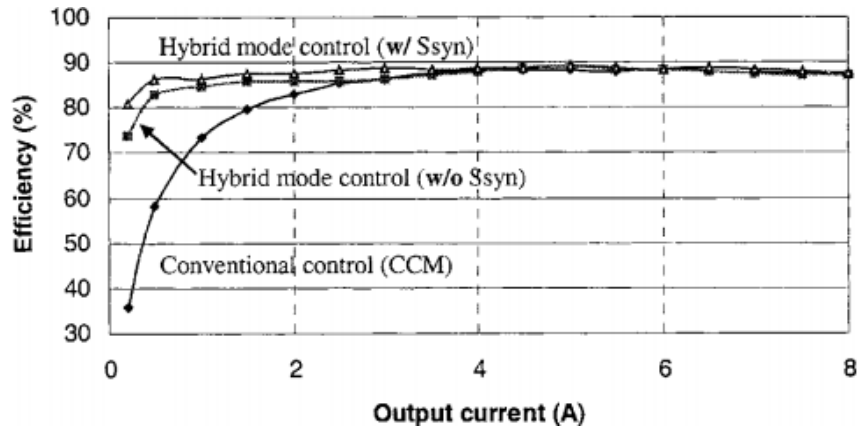


Figure 2.18: Efficiency of the hybrid MOSFET (w/ Ssyn) and hybrid Schottky diode (w/o Ssyn) method from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826-834, 2000. Used under fair use, 2015.

## 2.6 Shoot-through and Its Conventional Solution

A shoot-through problem may occur for a synchronous buck converter, which is a direct path from the input to ground. Shoot-through conduction occurs when both top and bottom MOSFETs are fully or partially turned on at the same instant, providing a path for current to “shoot through” from power supply to GND. Any shoot-through would result in lower efficiency and could even damage the system. In order to minimize shoot-through, the synchronous buck converter controller generally employs a dead-time or time delay before turn on a MOSFET. During the dead-time, both power MOSFETs are off to prevent the cross conduction. Unfortunately, by introducing the dead-time does not fully eliminate the shoot-through problem. The high  $dv/dt$  event at the  $V_{sw}$  node as shown in Figure 2.19 due to a rapid turn-on of the top MOSFET may also cause undesired turn-on of the bottom MOSFET and can create the shoot-through problem. The detailed reason for a  $dv/dt$  induced shoot-through is illustrated in [24].

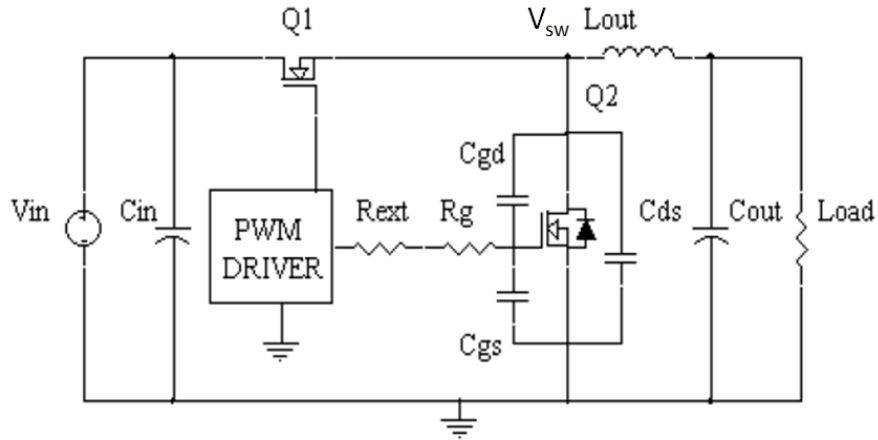


Figure 2.19: Detailed representation of bottom MOSFET in asynchronous buck regulator from T. Wu, "Cdv/dt induced turn-on in synchronous buck regulations," Tech. Rep., International Rectifier, 2007 [Online]. Available: <http://www.irf.com/>. Used under fair use, 2015.

One popular solution to solve this problem is to slow down the turn on speed of the top MOSFET and reduce the ratio of  $dv/dt$  at the  $V_{sw}$  node. Its effectiveness is demonstrated in [25]. A simple way to introduce dead time and to slow down the turn on speed of the top MOSFET is illustrated in Figure 2.20 [26]. A diode parallel with the resistor is in series with the cap to introduce a turn on delay and fast turn off. In this circuit, the RC delay allows adjustment of the dead time and MOSFET turn-on speed. During turn off, the anti-parallel diode shunt out the resistor.

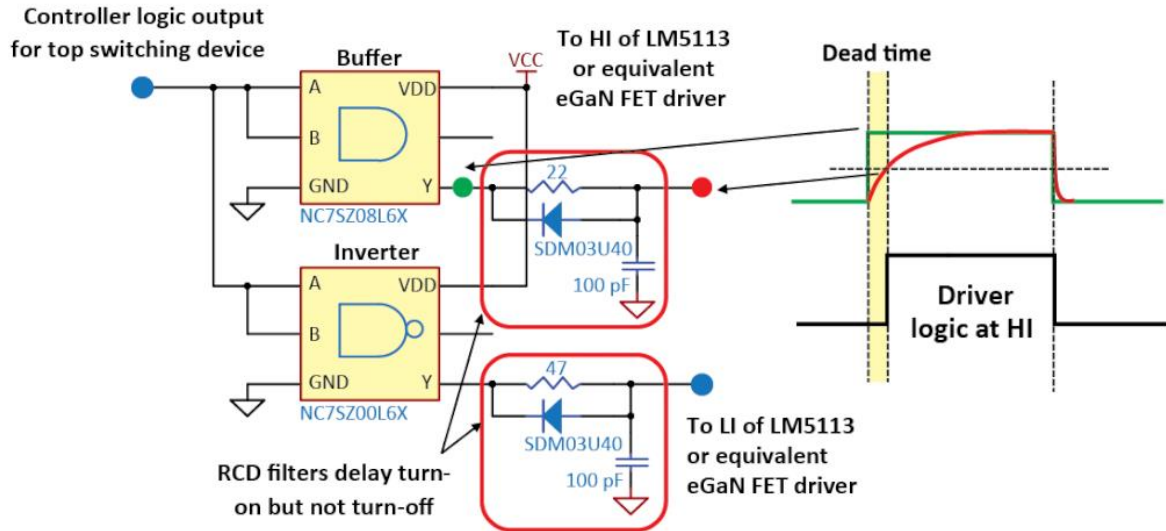


Figure 2.20: Simple turn-on and turn-off speed enhancement circuit from J. Klein, ““Shoot-through” in Synchronous Buck Converters,” Fairchild Semiconductor Appl. Note AN-6003, Apr. 2003. Used under fair use, 2015.

Optimization of those components is important in this circuit because the goal is to minimize the loss. Moreover, those components are generally bulky and lossy which dramatically increase the circuit complexity and the space. The proposed gate driver in Section 4.2.3 introduces a built-in dead time and slows the turn on speed.

## 2.7 Advantages of the Integrated Power Converter

For low power applications, research activities and efforts are focusing on the integrated converter solution. When a converter is integrated, the size is greatly reduced in comparison to a PCB converter with many discrete components. A smaller size reduces the overall material cost of the converter, which reduces the cost. Also the highly integrated technique increases manufacturability and is easier to automate the process. Equally importantly, the efficiency also increases with an integrated circuit as it is possible for the designer to optimize power losses on each control block for the target application. The tradeoff is that the design complexity and efforts increases substantially. For these reasons, the demand for high integrated and high efficiency power converter is increased dramatically, especially for the target battery-operated application. The integrated power converter could soon replace the conventional discrete

component power supplies modules [27].

The research activities discussed in this section are based on discrete components. The proposed converter design attempts to take the advantages of the integration by integrating the converter power stage and control blocks into a single chip. The proposed converter also adopts a two-mode converter consisting of a baby-buck mode and a heavy-load mode, with constant on-time  $V^2$  control and optimum mode selection (OMS) control to improve the efficiency, particularly at light load.

## 2.8 Chapter Summary

Previous research activities related to the proposed work were reviewed in this chapter. Section 2.1 overviews the design objective of the target smart camera system, with focuses on prolonged battery life via increased light-load efficiency. Section 2.2 discussed conventional synchronous buck converter approach and its shortcoming. Section 2.3 describes Wei's baby-buck concept and ONP control to improve light load efficiency. Then, the limitation of Wei's approach is also discussed. Section 2.4 explored two control methods including constant on-time  $V^2$  control which is adopted for the proposed converter to improve efficiency. Section 2.5 section illustrated Zhou's methods for efficiency improvement at light load efficiency. Section 2.6 mentioned a conventional solution to mitigate the shoot-through problem occurred in synchronous buck converter. And lastly, the advantages of integration and the trend of designing power converter are shown in section 2.7. The primary goal of this research work is to design a converter with the combination of two modes, a baby-buck mode and a heavy-load mode, to improve the light load efficiency.



# Chapter 3

## Proposed Two-Mode Buck Converter

This chapter describes the system level design of the proposed converter. Section 3.1 specifies the design requirement with the goal of improving overall efficiency, especially at light load, of the converter. Section 3.2 introduces a two-mode approach to accomplish the design objective. Section 3.3 describes techniques applied to each mode to increase the efficiency at its respective load range, and Section 3.4 explains the operation principle of proposed converter at the block level. Section 3.5 describes verification of the functionality of the proposed converter. Section 3.6 summarizes the chapter. The proposed converter was design and fabricated in CMOS 0.25  $\mu\text{m}$  technology.

### 3.1 Specification of the Proposed Converter

The specifications of the proposed DC-DC buck converter are given in Table 1. The proposed converter is designed to regulate the output voltage at 1.2 V, with an input of 5 V. The load current ranges from 10 mA to 1200 mA. The peak-to-peak output ripple must be within the processor input requirement of 30 mV, with load transient requirement of 60 mV. Most buck converters suffer from low efficiency at light load, and hence the major design objective of the proposed converter is to improve light load efficiency, while being able to manage heavy load with reasonably high efficiency.

Table 1: Specifications of the Proposed Buck Converter

Specification	Requirement
---------------	-------------

Input / output voltage	5 V / 1.2V
Minimum / maximum load current	10 mA / 1200 mA
Output voltage steady/ transient peak-peak ripple	30 mV/ 60 mV

### 3.2 The Proposed Converter with Two-mode Approach

This thesis work intends to achieve high efficiency for both light and heavy load. The proposed converter consists of two modes: a baby buck mode and a heavy load mode as shown in Figure 3.1 and each mode is optimized for its respective load range. The mode selector senses the load condition and turns on the appropriate mode while shutting down the other mode to save the loss. At light load, the baby-buck mode is selected and the feedback controller regulates the control signal ( $D_{baby}$ ) to control output voltage. Conversely, the heavy-load mode is active at heavy load, and the feedback controller regulates heavy-load mode power stage ( $D_{heavy}$ ) to adjust output voltage.

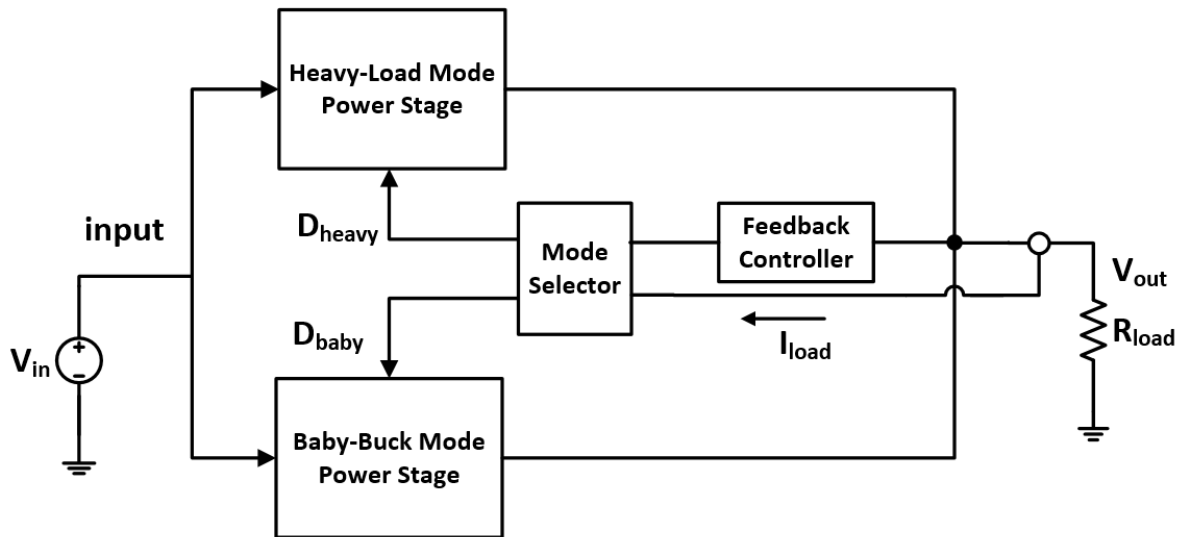


Figure 3.1: Top level block diagram of the proposed two-mode converter

### 3.3 Design of the Proposed Two-mode Converter

This section describes design of the proposed two-mode converter, in which the design is split into design of the baby-buck mode converter and design of the heavy-load mode converter.

#### 3.3.1 Design of the Baby-Buck Mode Converter

Design of a high efficiency baby-buck mode converter is crucial to improve the overall efficiency. A schematic diagram of the baby-buck mode converter is shown in Figure 3.2. The converter consists of a nonsynchronous buck power stage and a feedback loop to regulate the output voltage at 1.2V. The following schemes or technique are adopted or proposed for the baby-buck mode converter to increase the light load efficiency.

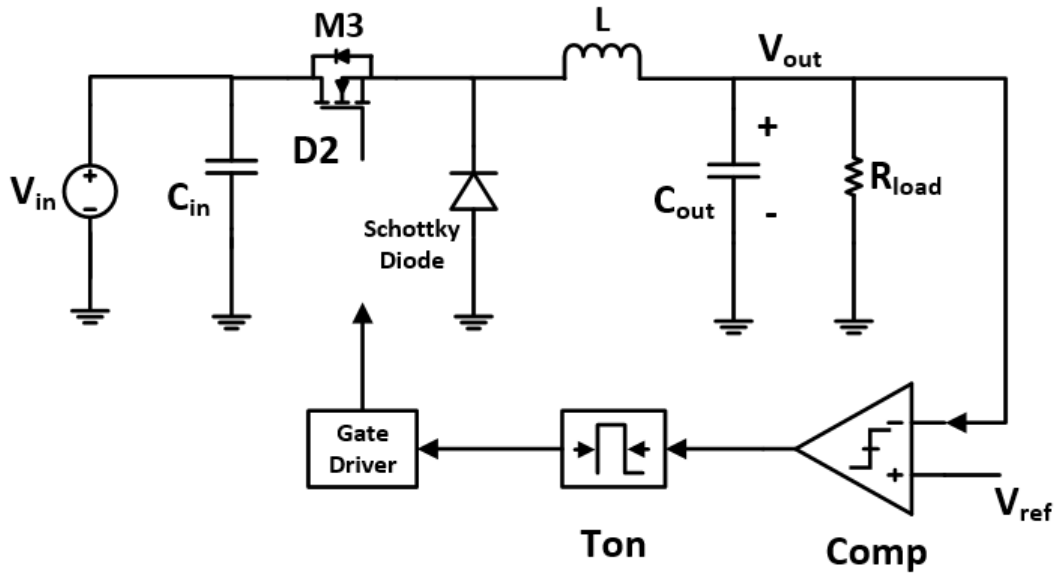


Figure 3.2: Schematic of the proposed baby-buck mode converter

Firstly, the baby-buck mode handles the load current below the critical current, where the load current is smaller than the peak inductor current ripple. Therefore, the baby-buck mode converter adopts pulse frequency modulation (PFM) in discontinues current mode (DCM) to reduce conduction and switching losses at light load. The PFM control lowers the switching frequency as the load current decrease and hence reduces switching and driving losses. DCM operation reduces the conduction loss by preventing from circulating energy mentioned in Section 2.2.2 under CCM operation. Secondly, the quiescent power of the controller impacts the overall efficiency as the load decreases. For example, 1 mW power dissipation in the controller

decreases the efficiency by 8% for the target light load of 10mA (12 mW). Thus, constant on-time  $V^2$  control, the simplest PFM control method, is implemented to reduce the quiescent power dissipation. The optional compensate network is also omitted for the same purpose. A simple constant on-time  $V^2$  control scheme as shown in Figure 3.2 reduces the number of building blocks and hence the power dissipation.

Thirdly, the current on power switch is small at light load. Therefore, the control power switch, the power MOSFET (M3), is optimized to have low  $Q_g$  at the cost of relatively higher  $R_{dson}$ . Low  $Q_g$  reduces switching and gate driving losses. Note that the conduction loss due to  $R_{dson}$  is negligible in comparison to switching and driving losses at light load. The bottom power switch is a Schottky diode instead of a MOSFET to avoid the zero current detect (DCM) block which is necessary for a synchronous buck to enter DCM. In addition, the Schottky diode brings additional benefit to heavy load efficiency which will be illustrated in section 3.4.1.

### 3.3.2 Design of the Proposed Heavy-Load Mode Converter

As a conventional synchronous buck generally achieves high efficiency at heavy load, the proposed heavy-load mode converter adopts the design of the conventional synchronous buck converters. It implements constant switch frequency control in CCM. Figure 3.3 shows the proposed heavy-load mode converter. The converter consists of a synchronous buck power stage with two power MOSFETs and a feedback loop to regulate the on time of the top MOSFET (M1) and bottom MOSFET (M2). Both M1 and M2 are optimized for heavy load with smaller  $R_{dson}$  at cost of higher  $Q_g$ . Note that the  $R_{dson}$  has more influence on efficiency at heavy load.

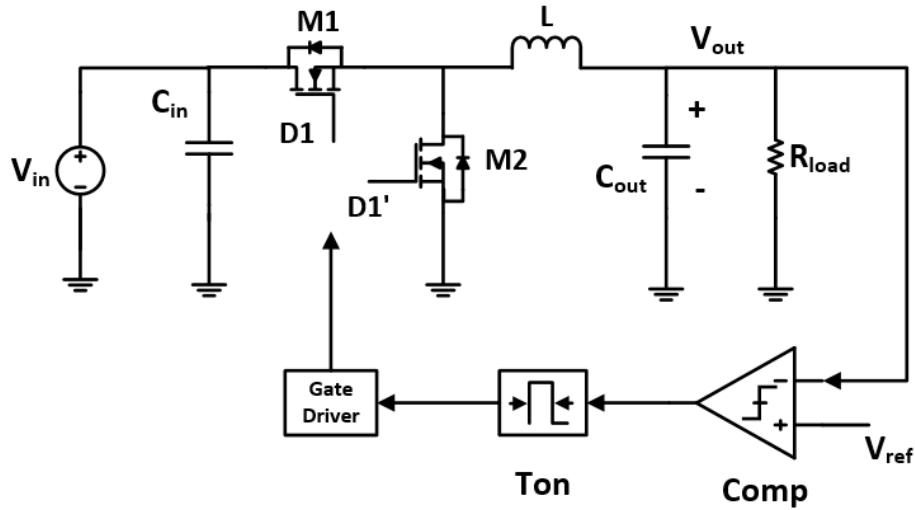


Figure 3.3: Schematic of the proposed heavy-load mode converter

The proposed heavy-load converter reuses the same COT  $V^2$  controller implemented for the baby-buck mode converter, while achieving constant switching frequency with CCM operation. This is possible for the proposed design because the voltage conversion ratio is the same for both baby-buck and heavy-load converters and hence a fixed on-time in COT  $V^2$  control. Since the off-time is also fixed at the steady state, the switching frequency also remains constant at the steady state. Note that the off-time is shortened to increase the frequency for a load step up transition, and it is opposite for the load step down. The CCM operation is realized in a synchronous buck converter as long as the two MOSFETs are complementary to each other.

The CCM operation at heavy load and DCM operation with a reduced frequency at light load is illustrated in Figure 3.4.  $D_1$  and  $D_1'$  are the on time for M1 and M2.  $D_2$  is the on time for M3 and  $D_2'$  is the conduction time for the Schottky diode. At heavy load, because the average load current is larger than the peak ripple of the inductor current, the converter operates in CCM and the switching frequency is fixed. At light load, the diode blocks the reverse current. The converter enters DCM operation with a reduced frequency, as the average load current decrease below the peak ripple of the inductor current.

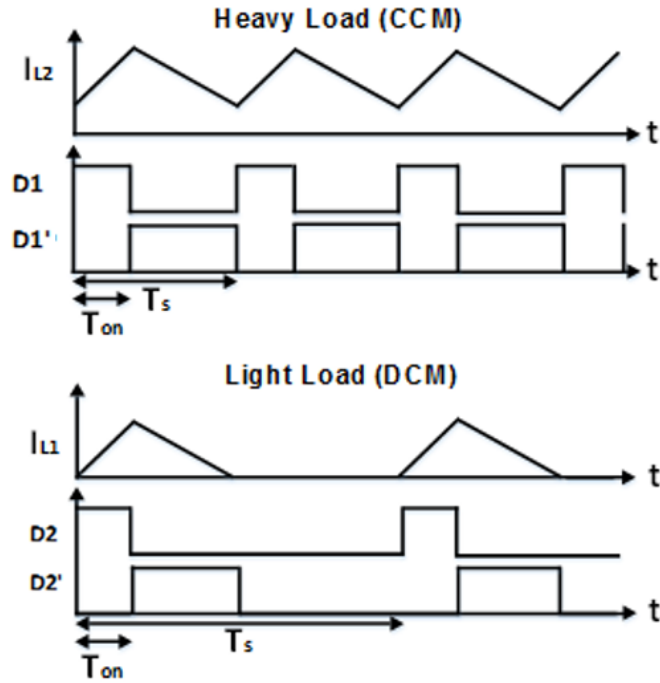


Figure 3.4: Waveforms of the inductor current and the control signals

### 3.4 Operation of the Proposed Converter: Combination of the Two Converters

The proposed converter combines both heavy-load and baby-buck mode converters into a single converter as shown in Figure 3.5. The power stage consists of two converters with a shared inductor  $L$  and two shared capacitors,  $C_{in}$  and  $C_{out}$ . The feedback network shares the COT controller consisting of a comparator and a COT pulse generator, the mode selector, and the startup building block.

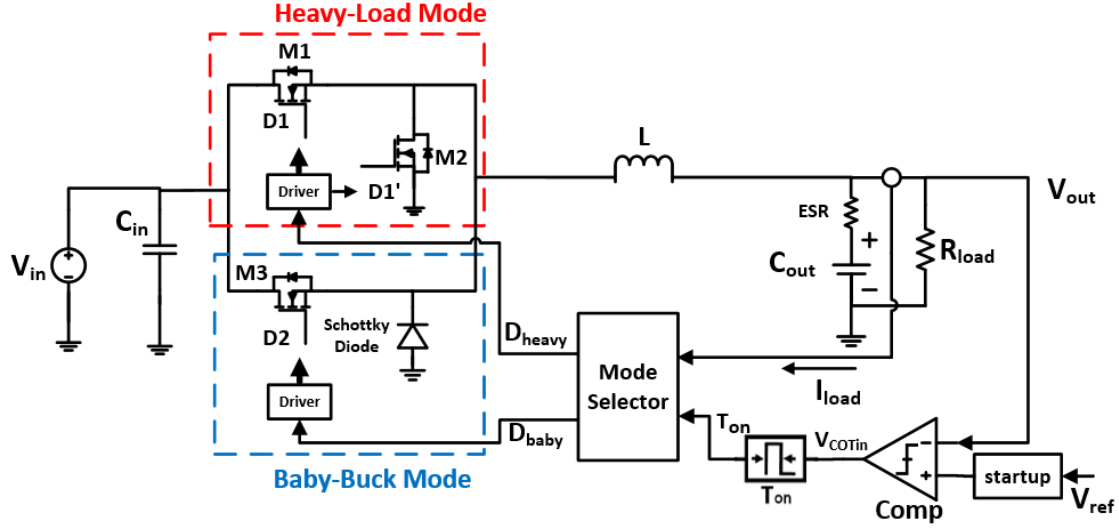


Figure 3.5: The structure of proposed two-mode single converter

The proposed converter intends to use a minimal number of off-chip components to reduce the size. With shared inductor, two capacitors and controller, the proposed two-mode converter reduces the number of off-chip components in comparison to a multiphase converter with baby-buck or conventional two separated converters.

### 3.4.1 Operation of the Power Stage

The power stage of the proposed converter is shown in Figure 3.5. The heavy-load mode switches achieve maximum efficiency for load current ranging from 180 mA (216 mW) to 1200 mA (1.4 W) and the baby-buck mode switches are optimized for high efficiency at light load for load current from 10 mA (12 mW) to 180 mA (216 mW). At heavy load, when switch M1 is on and switch M2 is off, the inductor and the capacitor are charged from the input source. Conversely, when M1 is off and M2 is on, the load is supplied through discharging of the inductor and the capacitor. The light load operation is similar to heavy load operation. The inductor is charging when switch M3 is on, and the inductor is discharging when the diode is on. The difference is that the diode blocks the reverse inductor current. So, when the inductor current discharges to zero, the baby-buck mode naturally turns into DCM. DCM improves efficiency at light load, while CCM operation achieves higher efficiency than DCM at heavy load [6]. The boundary between light load and heavy load is designed at 180 mA for the proposed design, which ensures the heavy modes to operate under CCM and the baby-buck mode works under DCM.

The peak inductor current ripple is the same for both heavy and light load due to the shared inductor, which is given in (5) [6]. If the peak-peak inductor current ripple remains at 360 mA while the load or average output current decreases to 180 mA, the baby-buck mode is turned on. When the valley of current ripple touches zero at the point, the current does not become negative because of the baby-buck diode. So the converter works under DCM. This also explains why the proposed converter can manage the CCM operation at heavy load and DCM operation at light load.

$$\frac{\Delta I_L}{2} = \frac{(V_{in} - V_{out}) * D}{F_s * L} \quad (5)$$

By introducing the Schottky diode at baby-buck mode, it simplifies the controller design due to eliminating the control block of entering DCM. In addition, this diode in parallel with M2 improves the efficiency during the dead time under heavy load. Both M1 and M2 are deactivated during the dead time, and the current flows through the parallel Schottky diode rather than the body diode of M2, thus reducing the conduction loss. Figure 3.6 shows the current flow during the dead time under heavy load.

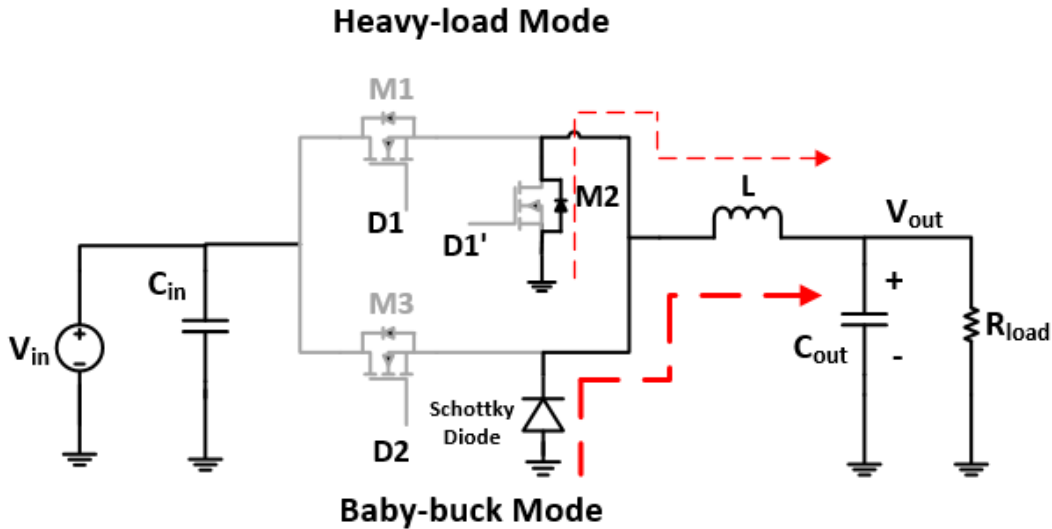


Figure 3.6: The current flow during the dead time of heavy load

The output capacitor periodically charges and discharges the energy. An appropriate size capacitor is crucial for the stability of the proposed converter, and it will be discussed in section 4.1. Design of the gate drivers with build in dead time is described in section 4.2.3.



### 3.4.2 Constant On-time $V^2$ Control

The feedback network shown in Figure 3.5 includes the startup block, the COT  $V^2$  controller, and the mode selector. The basic operation of the feedback network is summarized below. The startup block is a RC delay circuit, which has no impact on  $V_{ref}$  during steady state, but it prevents the circuit from being overcharged during startup (Refer to Section 4.2.1). The comparator and the COT pulse generator form the COT  $V^2$  controller and regulate the output voltage to stay at the desired value. The output voltage ( $V_{out}$ ) compares with the reference voltage ( $V_{ref}$ ), and the result wakes up the COT block to generate a COT pulse ( $T_{on}$ ) which is used to turn on and off the power switches. The mode selector detects the load condition, either at light load or heavy load, based on the sensed load current and delivers the constant on pulse ( $T_{on}$ ) signal to the corresponding mode. The design of the mode selection is discussed in Section 4.2.4.

The proposed converter adopts the COT  $V^2$  control, where the controller consists of a COT pulse generator and a comparator. As mentioned earlier, the controller is shared to reduce the controller complexity and hence save the power.  $T_{on}$  signal generated by the COT block passes through the mode selector and regulates the on period of top switches of both modes. When the output voltage  $V_{out}$  drops below the desired value (1.2 V), the comparator output goes high and turns on the COT block to charge the capacitor for the designated period. Then  $V_{out}$  starts to increase during the period. After this period expires, COT block turns back to off, and  $V_{out}$  starts to drop until it drops below 1.2 V. This process repeats to regulate the output voltage at desired value. The corresponding waveforms are shown in Figure 3.7.

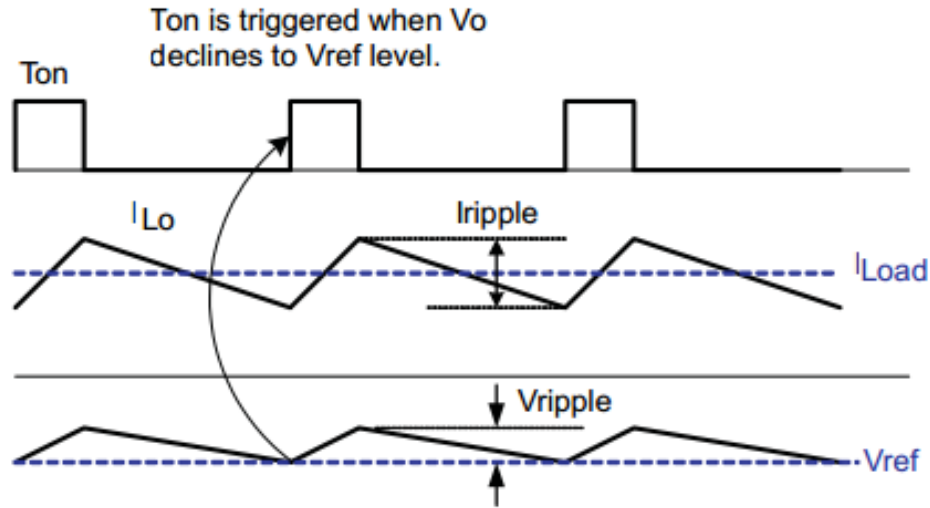


Figure 3.7: Waveforms of COT  $V^2$  control at the steady state from C. Ni, T. Tetsuo, “Adaptive constant on-time (D-CAPTM) control study in notebook applications,” Texas Instruments, Dallas, TX, Appl. Rep. SLVA281B, Jul. 2007. Used under fair use, 2015.

The COT  $V^2$  controller works the same for the light load, but the slope of the falling capacitor voltage reduces for lower discharging current at light load under DCM. Hence  $t_{off}$  time becomes longer and switching frequency lower. The baby-buck mode in DCM with lower switching frequency reduces switch related losses. The COT pulse generator block is the key element of COT  $V^2$  control. A COT pulse generator with a designated on time and a minimum off time is discussed in Section 4.2.2.

### 3.5 Functionality Verification with SIMPLIS

SIMPLIS is used to verify regulation of the output voltage at steady states and transient responses at the system level. The circuit design of the proposed converter in SIMPLIS is shown in Figure 3.8. The circuit with ideal components in SIMPLIS simplifies the design complexity, and it is sufficient to verify its functionality. The power stage uses ideal switches switching at 250 kHz to emulate its functionality. The mode selection block turns off the other mode by sensing load current. The COT  $V^2$  control block generates the switching signals with constant on time and minimum off time.

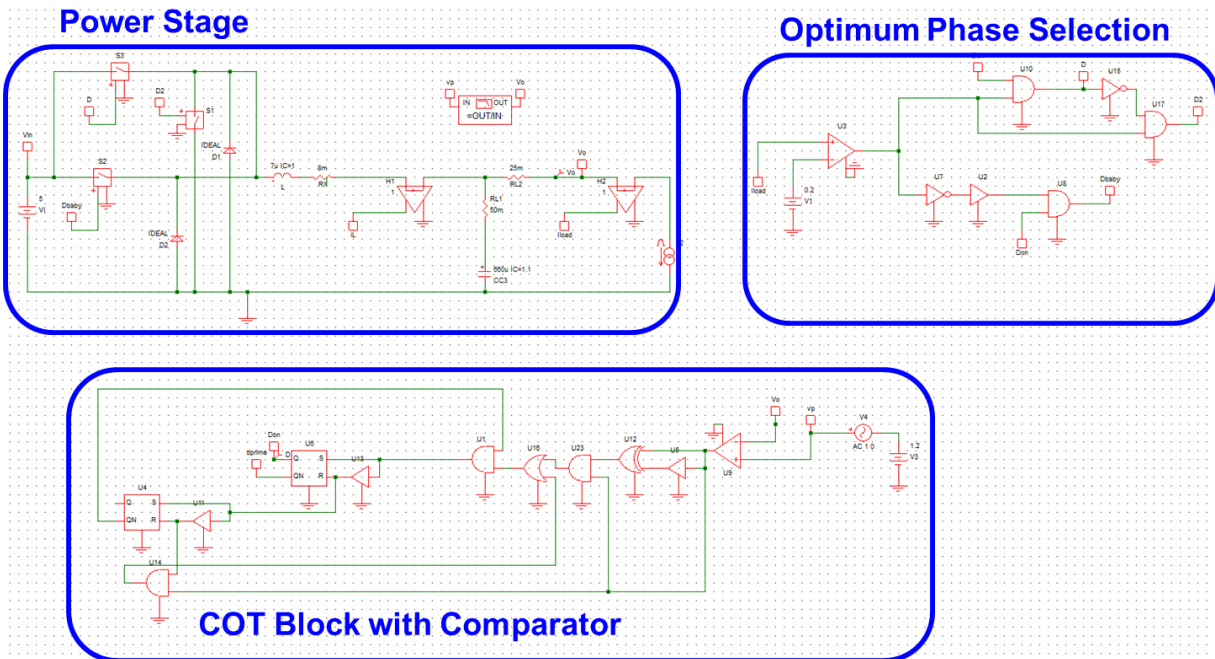


Figure 3.8: The proposed converter in SIMPLIS

Proper transient functionality during transition between the two modes is the key of the proposed design. Transient functionality between the two modes is simulated by SIMPLIS. Figure 3.9 shows the load step down from 600 mA to 100 mA. The green curve representing the control signal for the heavy-mode is shut down, while the blue curve representing the control signal for the baby-buck mode becomes active with a reduced frequency. Note that the output voltage remains around 1.2 V during the transition. Figure 3.10 shows the load step up from 100 mA to 600 mA, and the opposite operation occurs to verify its functionality.

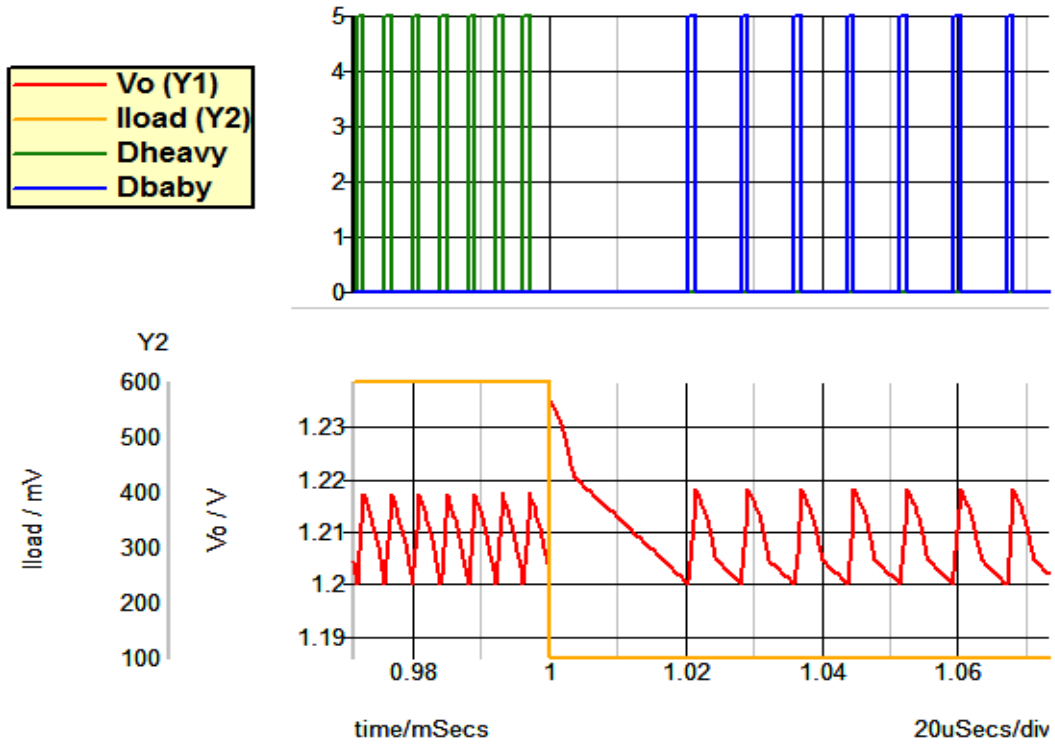


Figure 3.9: Load current step down from 600 mA to 100 mA

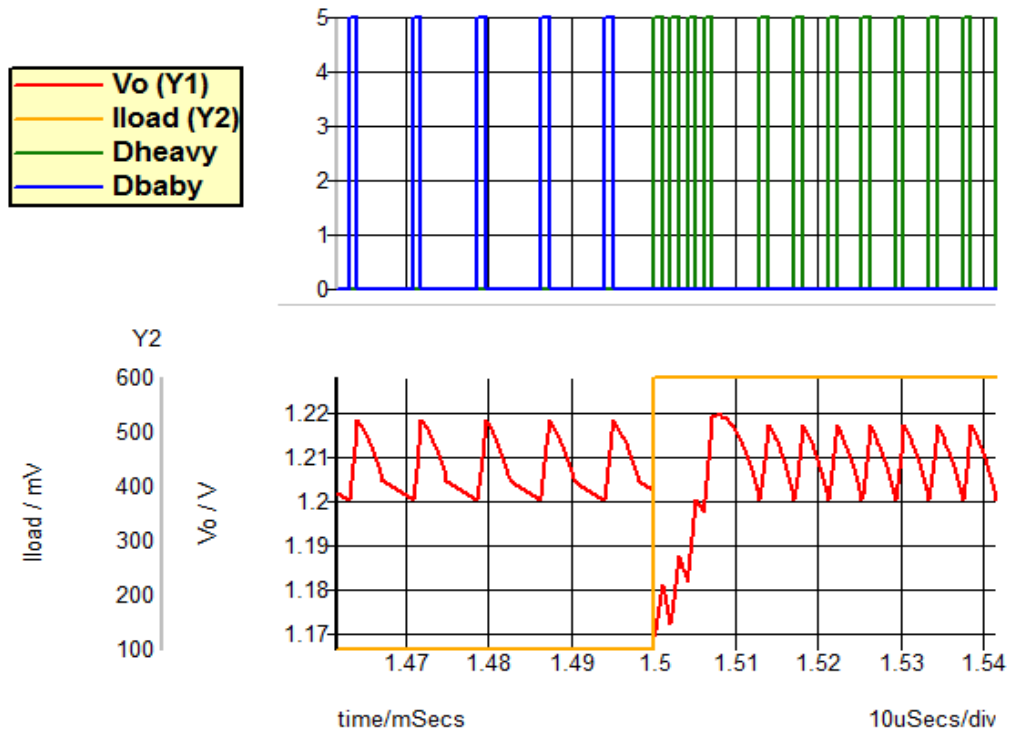


Figure 3.10: Load current step up from 100 mA to 600 mA

The Bode plot of the control loop is shown in Figure 3.11 **Error! Reference source not found.** The bandwidth indicates how quickly the device can respond to a transient change. The phase margin represents the stability against to disturbance. The bandwidth of the control loop is almost as wider as half of its switching frequency of the converter. The phase margin of the converter is also large enough to handle the unexpected disturbance. The bode plot shows the great stability of the converter up to its half switching frequency. However, the plot represents an ideal case due to use of ideal components.

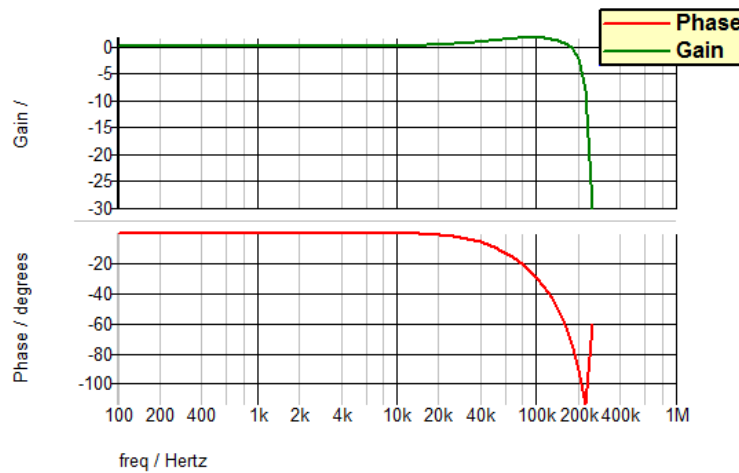


Figure 3.11: Stability bode plot of proposed convert in SIMPLIS

### 3.6 Chapter Summary

The chapter describes the system level design of proposed two-mode buck converter. The baby-buck mode is designed to optimize the light load efficiency and the heavy-load mode is designed to optimize at the maximum power consumption for the target processors. The proposed converter integrates the two modes into one converter with shared inductor, capacitor and controller. The design procedure and the operation of the power stage and controller are described. Lastly, simulation results verify the functionality and transition performance during transition between the two modes.

# Chapter 4

## Circuit Level Design of the Proposed Two-Mode Buck Converter

This chapter describes detailed circuit/transistor level design of the proposed two-mode converter. Section 4.1 describes components selection based on the design specifications and the design of three MOSFETs. Section 4.2 discusses design of major building blocks for the proposed converter and Section 4.3 describes design of other remaining building blocks. The proposed converter is designed and fabricated in 0.25  $\mu\text{m}$  CMOS technology. Section 4.4 presents the layout of the proposed converter with highlighted main blocks. Lastly, Section 4.5 summarizes the chapter.

### 4.1 Power Stage Component Selection and Design

The heavy-load mode is optimized to maintain high efficiency for its load current range of 180 mA or greater, and the baby-buck mode for its load range of 10 mA to 180 mA. The power stage consists of an inductor, an input capacitor, an output capacitor, and power switches including a diode and three integrated MOSFETs as shown in Figure 3.6. The main task is to select proper components for the power stage. In general, the inductor size dictates the current ripple and the transition point from CCM to DCM, and the output capacitor size determines the output voltage ripple and stability of the COT  $V^2$  control. Additionally, the input capacitor size affects the input voltage ripple due to discontinuous input current, and design of the MOSFETs has the major impact on the efficiency for a given mode. We follow the above order to design the proposed power stage.

The proposed converter is designed to operate at a relatively low switching frequency of 250 kHz for heavy mode in CCM. A low switching frequency reduces the impact of parasitics

and switching loss of the MOSFETs at the cost of large inductor and capacitor size. It should be noted that the small size is not a major design objective for the target application, but the efficiency.

#### 4.1.1 Off-chip Components Selection

The inductor is the first component to be selected, and its value decides the current ripple as shown in (5). A large inductance reduces the current ripple, but a reasonable magnitude of the ripple is necessary for the baby-buck to enter DCM. Also, the COT  $V^2$  controller requires inductor current ripple information to regulate the output voltage. A smaller inductance increases the current ripple, which in turn increases the conduction loss due to the increased RMS current. The inductance value can be obtained from (6) [6].

$$L = \frac{(V_{in} - V_{out}) \cdot D}{F_{sw} \cdot \Delta I_L \cdot I_{out\_max}} \quad (6)$$

A good estimation for the inductor current ripple  $\Delta I_L$  is 20-40% of the maximum output current [29]. So  $\Delta I_L = 30\%$  is chosen for the baby-buck to enter DCM at load current of 180 mA. With  $V_{in} = 5$  V,  $V_{out} = 1.2$  V,  $D = 0.24$ ,  $F_{sw} = 250$  kHz,  $\Delta I_L = 30\%$ ,  $I_{out\_max} = 1200$  mA for heavy-load mode, the inductance is obtained as 10.1  $\mu$ H. For a buck converter operating in CCM, the duty cycle  $D$  is the ratio of the output voltage to the input voltage (i.e.  $D = V_{out}/V_{in} = 1.2/5 = 0.24$ ). An inductance of 10  $\mu$ H with small maximum DCR of 16 m $\Omega$  was selected for the proposed power stage as 10  $\mu$ H inductors are available as an off-the-shelf component. With this inductance value, Equation (7) [6] is used to verify the theoretical critical load current for CCM / DCM boundary, which is obtained as 180 mA for the design.

$$I_{o\_crit} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{F_{CCM} \cdot 2L \cdot V_{in}} \quad (7)$$

Next the output capacitance is selected. The ESR and size of the output capacitor determines the output voltage ripple. The capacitor voltage ripple is a function of the capacitance value, the inductor current ripple, and the switching frequency as shown in (8) [6]. The ESR voltage is decided by the inductor current ripple and ESR value as shown in (9).

$$\Delta V_{Co} = \frac{\Delta I_L}{8 \cdot F_{sw} \cdot C_o} \quad (8)$$

$$\Delta V_{esr} = R_{esr} \cdot \Delta I_L \quad (9)$$

$$C_{o\_min} = \frac{\Delta I_L}{8 \cdot F_{sw} \cdot V_{ripple}} \quad (10)$$

In general, the output capacitor ESR is chosen as small as possible to minimize the ESR ripple. Thus, the minimum output capacitance can be simply selected based on (10). However, unlike other control schemes, the COT  $V^2$  control adopted for the proposed converter utilizes the ESR ripple as the inductor current information. As mentioned in Section 2.4.1, the ESR voltage ripple needs to dominate the capacitor voltage ripple to ensure that the inductor current is not distorted by the capacitor ripple and prevent the controller from being unstable. Generally, if the ESR voltage ripple is eight times larger than the capacitor voltage ripple, the circuit is stable [30]. The proposed converter has output voltage ripple specification of 30 mV, so 18 mV ESR voltage ripple results in 50  $m\Omega$  ESR resistance, and 2 mV capacitor voltage ripple results in 90  $\mu\text{F}$  output capacitance. An OSCON capacitor (P16418CT-ND) with 82  $\mu\text{F}$  and 45  $m\Omega$  ESR is selected for the proposed power stage. The OSCON cap has a long life span, and its ESR is stable from  $-55^\circ\text{C}$  to  $105^\circ\text{C}$ , which is important for the target design as the control information is based on the ripple across the ESR. Simulation results indicate that the chosen capacitance value provides good stability and keeps the output voltage ripple within the specification throughout the entire load range.

When selecting the input capacitor, the RMS current and the voltage rating, rather than the capacitor value, is the main consideration. The worst case of RMS current is  $I_{out}/2 = 600 \text{ mA}$ . Therefore, the OSCON capacitor (P16379CT-ND) of 100  $\mu\text{F}$  with rated voltage of 16 V and the rated ripple current of 4.68 A is selected as input capacitor.

The off-the-shelf Schottky diode is chosen to minimize the loss. Generally, Schottky diodes are better for low power applications than conventional diode because of the low forward voltage and no reverse recovery loss. A Schottky diode (LSM115J) is chosen due to its low forward voltage drop with maximum value of 0.22 V.

#### 4.1.2 Integrated Power Stage MOSFETs Design



MOSFETs are the switching elements for a DC/DC converter and therefore have losses associated with them in addition to the conduction loss. A simplified breakdown of MOSFET losses are conduction power loss ( $P_{cond}$ ), gate charge loss ( $P_{gate}$ ), switching power loss ( $P_{sw}$ ), MOSFET's output capacitance loss ( $P_{Coss}$ ), and reverse recovery loss from the body diode ( $P_{QRR}$ ), where these losses can be expressed as (11)-(15) [31].

$$P_{cond} = I_{load}^2 \cdot R_{dson} \quad (11)$$

$$P_{sw} = \frac{V_{off} \cdot I_{out}}{2} \cdot F_{sw} \cdot t_{sw} = \frac{V_{off} \cdot I_{out}}{2} \cdot F_{sw} \cdot \left( \frac{Q_g}{I_{driver}} \right) \quad (12)$$

$$P_{gate} = Q_g \cdot F_{sw} \cdot V_{gs} \quad (13)$$

$$P_{coss} = \frac{C_{oss} \cdot V_{off}^2 \cdot F_{sw}}{2} \quad (14)$$

$$P_{cond} = Q_{RR} \cdot F_{sw} \cdot V_{off} \quad (15)$$

Conduction losses depend on the square of the load current, meaning conduction loss dominates at heavy load with  $I_{out}$  from 180 mA to 1200 mA. Therefore, the design goal for heavy-load mode is to have small  $R_{dson}$  to reduce conduction loss. For Gate driving losses, switching losses,  $C_{oss}$  losses, and reverse recovery losses depend on the switching frequency. Therefore, a lower frequency also lowers these losses. These losses are also a function of the gate charge, reverse recovery charge, and capacitance. A small MOSFET ensures a low  $Q_g$ ,  $C_{oss}$  and  $Q_{RR}$ . Therefore, the baby-buck mode should be designed with low gate charge to reduce these losses, which are dominant at very light load compared to conduction losses [1].

In general, conduction power loss ( $P_{cond}$ ), switching power loss ( $P_{sw}$ ), and gate charge loss ( $P_{gate}$ ) are major losses on MOSFETs [31]. As shown (11)-(13), the total loss of MOSFETs depends on two parameters, gate charge  $Q_g$  and on-resistance  $R_{dson}$ . The product of the gate charge and the on-resistance is constant for a MOSFET device and called the Figure of Merit (FOM) shown in (16) [32].

$$FOM = Q_g * R_{dson} \quad (16)$$

The above equation shows the tradeoff between the two parameters. Therefore, in order to reduce MOSFET losses, it is essential to select devices with a low FOM. MOSFETs of the

proposed converter are designed using TI 0.25  $\mu\text{m}$  PDK LBC7. Among all available MOSFETs in LBC7 library, the Lateral Diffused MOS (LDMOS\_7V) type is selected for the proposed converter due to its low FOM of 28.4  $\text{m}\Omega\text{-nC}$ . Since the input voltage is 5 V, the  $V_{\text{ds}}$  breakdown voltage of this type device is 7 V which provides 40% margin from overshooting at switch node.. The length and width of a MOSFET determines the gate charge and the on-resistance. To design MOSFETs with the lowest overall loss, the gate charge and the on-resistance were iteratively varied to find the optimum point. Design of the three integrated MOSFETs are in the following order, baby top MOSFET, heavy bottom MOSFET, and heavy top MOSFET. Through simulations in Cadence, the parameters of three MOSFETs were found to obtain their minimum overall losses.

The top baby MOSFET is designed first because the baby-buck power stage contains only one MOSFET. The efficiency of the baby-buck power stage at light load (120 mA) is simulated with previously selected external devices while varying the gate charging and on-resistance of the MOSFET. Figure 4.1 shows the efficiency curve of the baby-buck at 100 mA with different sizes (finger numbers) of the top baby MOSFET, and the width of each finger is 1055  $\mu\text{m}$ . The size of the baby MOSFET is therefore chosen for the finger number of 60, which leads to the minimum overall loss.

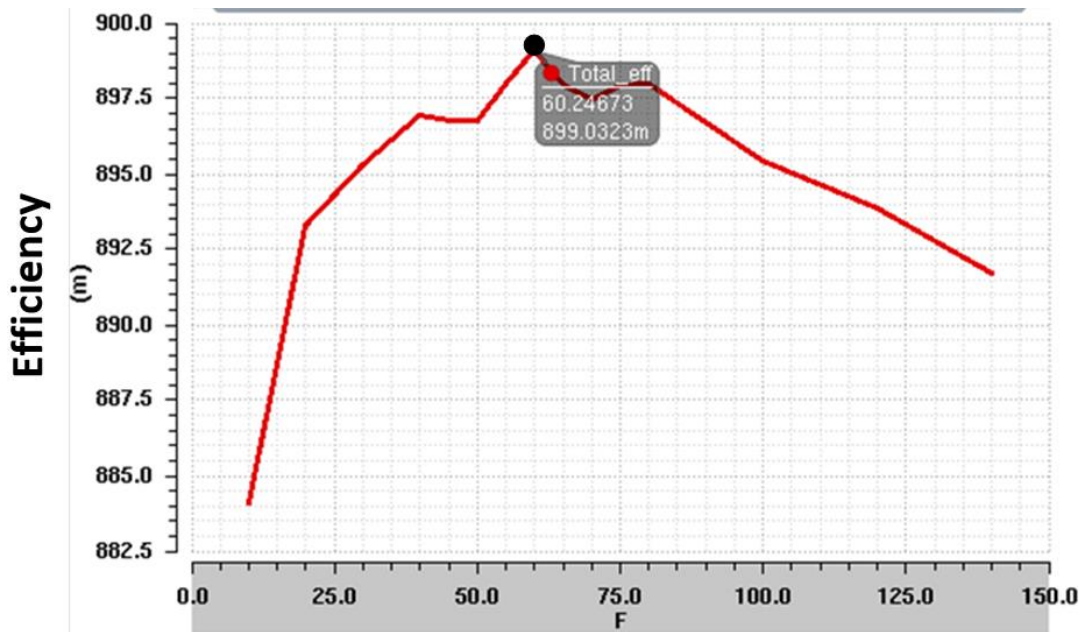


Figure 4.1: Efficiency versus number of fingers (F) of the top baby MOSFET (the width of each finger is 1055  $\mu\text{m}$ )

Next, the sizes of the two MOSFETs for the heavy buck converter are determined. The bottom heavy MOSFET is determined first because switching losses and reverse recovery loss of the bottom MOSFET is negligible for a synchronous buck [31]. Figure 4.2 shows the efficiency of the heavy buck power stage at full load with different sizes of the bottom heavy MOSFET. The finger number of 188 is chosen, as the efficiency is already saturated beyond the point. Likewise, the corresponding efficiency waveform of top heavy MOSFET is shown in Figure 4.3. The size of top heavy MOSFET is chosen at finger number of 120 due to the same reason.

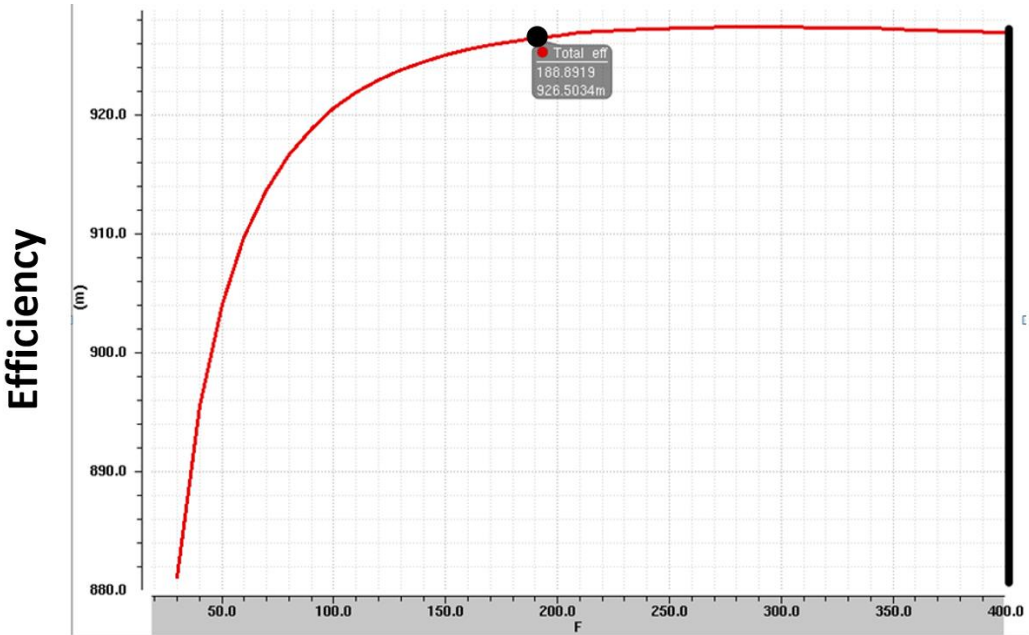


Figure 4.2: Efficiency versus number of fingers (F) of the bottom heavy MOSFET (the width of each finger is 1055  $\mu\text{m}$ )

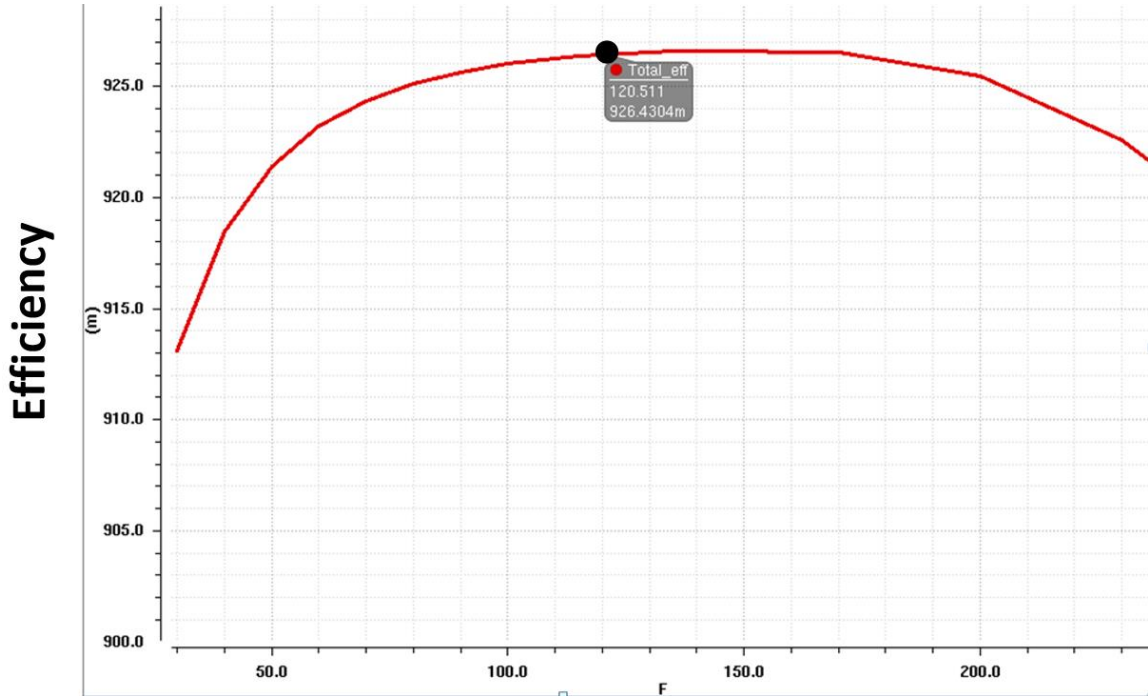


Figure 4.3: Efficiency versus number of fingers (F) of the top heavy MOSFET (the width of each finger is 1055  $\mu\text{m}$ )

The selected MOSFETs follow the general design trends in (11)-(13). For light-load case, the gate charge has the biggest impact on MOSFET losses. The proposed top baby MOSFETs has a small  $Q_g$  of 666 pC. For heavy load case, the on-resistance must be kept low to prevent excessive conduction loss. The on-resistance  $R_{\text{dson}}$  is 21  $\text{m}\Omega$  for the top heavy MOSFET, and it is even lower, 14  $\text{m}\Omega$ , for bottom MOSFET due to a longer conducting period. The gate charge for the top heavy MOSFET is 1.35 nC and that for the bottom MOSFET is 2.03 nC.

## 4.2 Circuits for Major Building Blocks

A block diagram of the feedback network for the proposed converter is shown in Figure 3.5, and this section illustrates design of major building blocks including the COT pulse generator, the optimum mode selector, gate drivers, and the startup block. Other necessary building blocks are described in Section 4.3. The COT pulse generator creates a fixed on-time pulse ( $T_{\text{on}}$ ) with variable off-time once it is triggered. The optimum mode selector detects the load condition and delivers the COT pulse ( $T_{\text{on}}$ ) signal to the gate driver of the corresponding mode, heavy load and baby buck. The gate driver captures the ( $T_{\text{on}}$ ) signal from the optimum

mode selector and amplifies the signal to quickly turn on and off the power MOSFET. The startup block is a RC delay circuit, which prevents the circuit from overcharge during a startup. The proposed major building blocks are designed in the above order.

#### 4.2.1 Constant On-time Pulse Generator

The COT pulse generator creates a fixed on-time pulse and hence a timing circuit is required for this block. However, the conventional R-C timing circuits are not suitable for target application because the accuracy is poor for a resistor in CMOS technology. Note that a capacitor typically offers better stability and reliability compared to resistor in CMOS fabrication. Another simple, but relatively accurate, timing circuit is based on charging or discharging a capacitor through a current source [33]. The voltage across a capacitor is equal to the charge divided by the capacitance. Thus, if a constant current source is charging the capacitor, the voltage on this capacitor rises at a constant rate. Based on the current and the capacitance, we can predict how long it will take to reach a certain voltage. This voltage can be used as the timing information for the proposed COT pulse generator. The proposed COT block adopts the scheme of constant current charging to create a timer.

A circuit diagram of the proposed COT pulse generator is shown in Figure 4.4. It consists of a few logic gates, three SR latches, and two timers. The operation of the COT pulse generator is briefly summarized as follows. The front logic gate ensures a clean “set” signal to SR1, when  $V_{COTin}$  is high. This SR latch sets the output Q to high and the complementary QZ output to low. This Q represents the COT pulse signal ( $T_{on}$ ) and the QZ starts to count the time period. When QZ becomes low, it turns off the transistor ( $M_{on}$ ) and the capacitor ( $C_{on}$ ) voltage starts to rise at a constant rate due to the constant current source ( $I_{b1}$ ) until its voltage reaches  $V_{ref}$ , turning the comparator (Comp1) output to high. Then, the high signal of Comp1 output travels back to reset SR1. Hence, the Q becomes low and the QZ becomes high to discharge  $C_{on}$ . The on time of  $T_{on}$  is therefore the period from the moment of  $C_{on}$  starts charge to the moment of  $C_{on}$  reaches  $V_{ref}$ . The time for  $C_{on}$  voltage rises to  $V_{ref}$  is a function of its capacitance and charging current shown in (17). In this case,  $V_{ref}$  is 1.2 V, the capacitance is 8.3 nF, and current is 10 uA, the on time of  $T_{on}$  is therefore 1  $\mu$ s which is the desired on time for the target operation frequency of 250 kHz under heavy-load mode, the on-time of 1  $\mu$ s would stay constant at each  $V_{COTin}$  high event as long as the  $V_{ref}$ , the capacitance, and the charging current do not vary.

$$t = \frac{C \cdot V}{I} \quad (17)$$

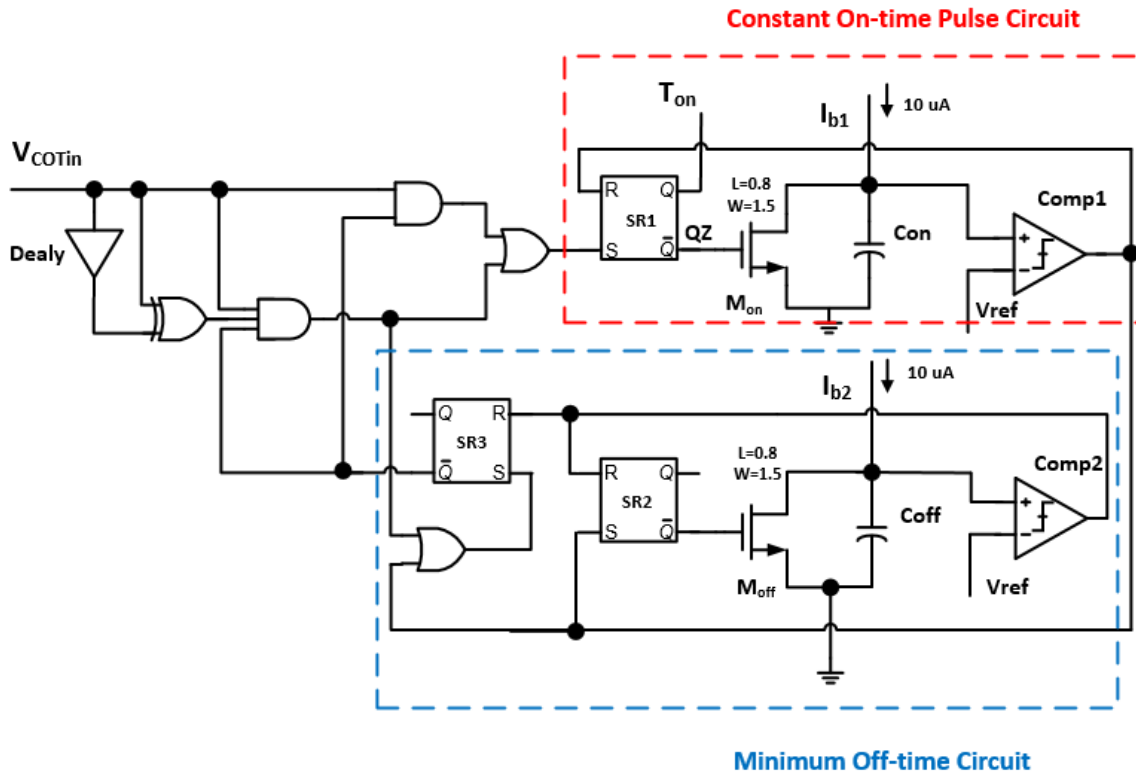


Figure 4.4: The circuit diagram of the COT pulse generator

If a second  $V_{COTin}$  high signal comes immediately after the COT pulse expires, there is insufficient time for  $C_{on}$  to discharge. To protect the  $C_{on}$  from not being discharged completely, the minimum off time (MOT) circuit shown in Figure 4.4 is adopted. The MOT circuit employs the same technique as the one used in COT pulse circuit and the minimum off time is 300 ns for the proposed design. This MOT circuit triggers right after the constant on time expires and it forces  $T_{on}$  to stay low for the designated period. Even if the  $V_{COTin}$  is always high during the startup or other load step up variation, the MOT circuit enables the generator to create on pulses with maximum duty cycle of 77 %.

The COT pulse generator stays low until it is triggered. Once it is triggered, it creates a designated on time period. Once the on time period expires, the generator goes back to low for a minimum amount of time independent of the condition of the generator. Another designated on time period occurs if the generator is still triggered and the minimum off time period has expires.

Through simulations under different scenarios, the designed block operates robustly to generate designated on pulses to support the COT  $V^2$  control for the proposed converter.

#### 4.2.2 Optimum Mode Selector Block

The entire optimum mode selection block shown in Figure 4.5 consists of two parts: a current sensor and a selector, with the current sensor block is highlighted in blue. A small current sensor resistor in series with the load senses the load current [18]. To reduce the power dissipation on the sensor resistor, a 22 m $\Omega$  small sensor resistor is selected. Then, a high gain differential amplifier senses a differential voltage across the sense resistor,  $V_{load+}$  and  $V_{load-}$ . Therefore, the output of the differential amplifier is load current information represented in voltage  $V(I_{Load})$ . This  $V(I_{Load})$  is then compared to the reference current  $V(I_{ref})$  through a comparator, where  $V(I_{ref})$  represents the boundary between the light and heavy load, which is 180 mA. The value of  $V(I_{ref})$  is set to 1.2 V as it is the same to reference voltage ( $V_{ref}$ ) of the feedback network, and the differential amplifier gain ratio is set to 303 obtained from  $V(I_{ref})/(R_{sense} * I_{boundary})$ .

The mode selector block highlighted in red in Figure 4.5 selects the appropriate mode based on the load current and applies the control signal to the gate drivers.  $T_{on}$  is the COT pulse signal generated by the COT controller.  $d1$  and  $d1'$  are the control signal for the heavy mode gate driver, where  $d1$  is for switch M1 and  $d1'$  for switch M2. The control signal  $d2$  is for the baby-buck mode gate driver, specifically for switch M3. If the load current is large enough to turn comparator high,  $d1$  is same as  $T_{on}$  and  $d1'$  is the complimentary of  $T_{on}$ . Under the light load, the output signal of the inverter\_1 is high, as the comparator output is low. Therefore, the control signal  $d2$  is active, and the signal of  $d1$  and  $d1'$ s are deactivated. To conclude, if the load current is large, the optimum mode selection block activates the heavy mode, while deactivating the baby-buck mode by disabling  $d2$ , and vice versa.

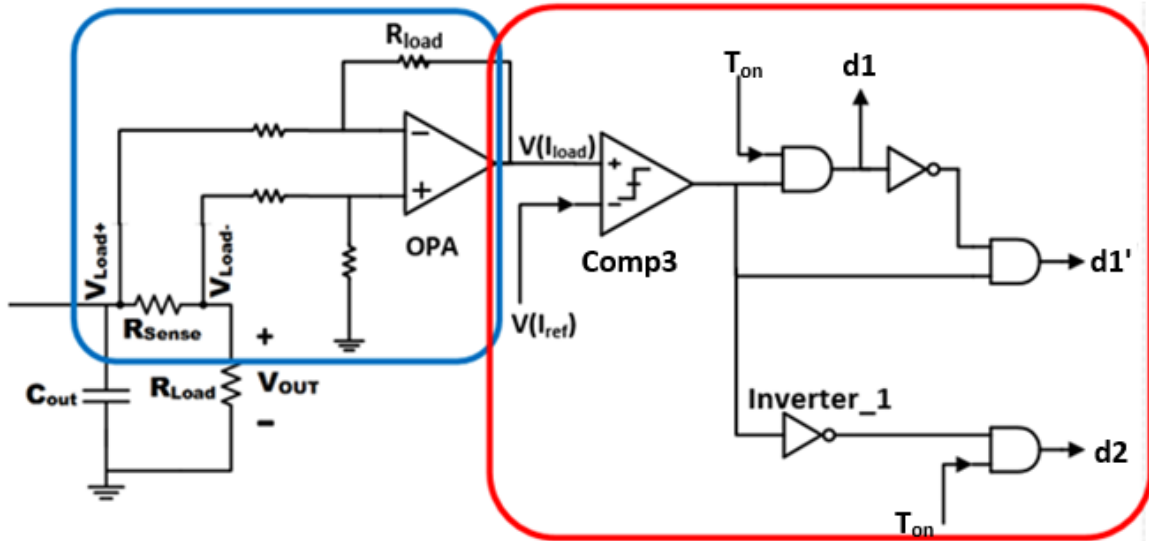


Figure 4.5: Design of the optimum mode selection block

### 4.2.3 Gate Driver Design

As the current from the controller is too small to drive a power MOSFET with large parasitic gate capacitor,  $C_{gs}$ , gate drivers are necessary to amplify the control signal for power MOSFETs. As shown in (12), the switching loss is proportional to reciprocal of  $I_{drive}$ . Therefore, the gate driver design is important to the efficiency of the proposed converter. The proposed gate driver not only amplifies the control current, but also provides the dead time. Since there are three MOSFETs in proposed converter, three gate driver designs are presented as follows.

Starting from the heavy bottom MOSFET, the gate driver for the MOSFET is highlighted in red in Figure 4.6. The controller signal  $d1'$  in Figure 4.6 passes through two inverters to reach the gate of the bottom MOSFET (M2). The width of the second inverter is larger than that of the first one to amplify the control signal, so that the current at the gate of M2 is large enough to quickly turn on and off M2.



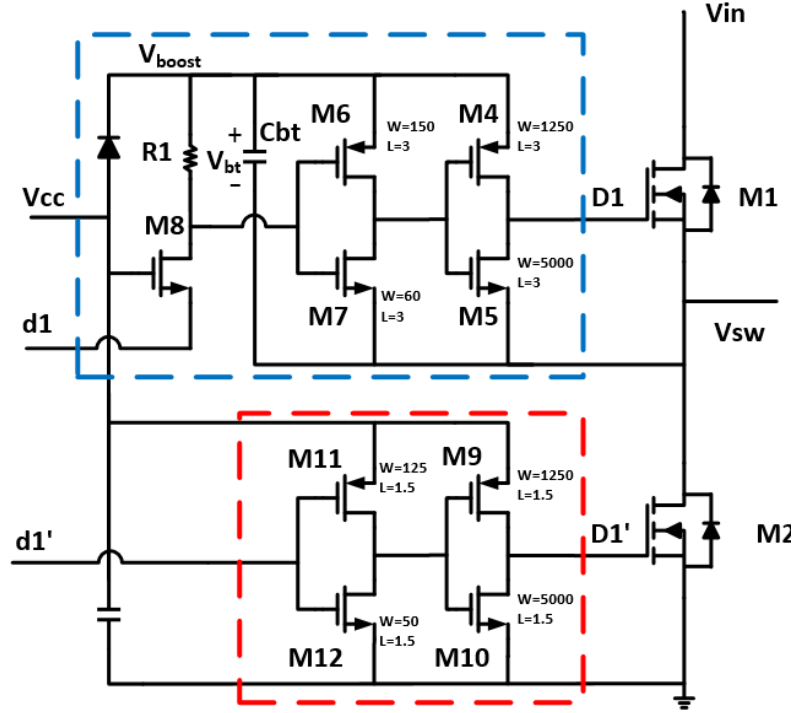


Figure 4.6: The structure of the heavy mode buck gate driver.

Majority of synchronous buck converters including the proposed one use an N-channel MOSFET as the top switch owing to high switching speed and a low FOM. The gate driver for an N-channel MOSFET becomes more complicate as the source of M1 ( $V_{sw}$ ) is not grounded. A bootstrap scheme is usually employed to address the problem. The gate driver highlighted in blue in Figure 4.6 adopts a bootstrap circuit, which is comprised of a bootstrap capacitor  $C_{bt}$ , a diode, a resistor, and a common gate amplifier M8 [34]. The basic operation of the bootstrap is explained briefly in the following. Suppose that the initial voltage of  $V_{sw}$  is an arbitrary positive voltage  $V_{sw0}$ , and let's ignore the voltage drop across the diode. When the control signal  $d1$  is 0 V, transistor M8 is turned on, and the drain of M8 becomes 0 V. The voltage  $V_{boost}$  is equal to the supply voltage  $V_{cc}$ . The following two inverters powered by  $V_{cc}$  set the gate voltage  $D1$  equal to  $V_{sw0}$ , specifically by turning on M5. So the top MOSFET M1 is turned off. Meanwhile, the bottom MOSFET is turned on by control signal  $d1'$ , and the voltage  $V_{sw}$  becomes 0 through the bottom MOSFET M2. Meanwhile, the bootstrap capacitor  $C_{bt}$  is charged to  $V_{cc}$ .

Now, the control signal  $d1$  goes high, transistor M8 is turned off. The voltage at the drain of M8 is equal to  $V_{boost}$ , which is  $V_{cc}$ . As  $V_{boost}$  is  $V_{cc}$  and  $V_{sw}$  is 0 V, the two inverters operate

normally and set the gate voltage of D1 to  $V_{cc}$ . The top MOSFET M1 is turned on, and the voltage  $V_{SW}$  starts to increase toward  $V_{in}$ , while the bottom MOSFET being turned off. The voltage  $V_{boost}$ , which is equal to  $(V_{bt} + V_{SW})$ , also starts to increase above  $V_{cc}$  owing to the diode. As the voltage difference  $V_{boost}$  and  $V_{SW}$  remains  $V_{cc}$  or the bootstrap capacitor voltage independent of  $V_{SW}$ , the current state of the transistors is maintained in spite of the rise of  $V_{SW}$ . Note that the bootstrap capacitor supplies the power for the two inverters during this period [34].

Lastly, the gate driver of the top baby MOSFET (M3) is shown in Figure 4.7, which is similar to the gate driver for M1. As M3 is smaller than M1, a smaller baby gate driver including smaller bootstrap capacitor  $C_{bbt}$  and inverters are used. The benefit of a smaller gate driver for M3 is to save the loss from the gate driver. The simulation results shows a gate driver is reduced in size for the baby gate driver, the power dissipation also is reduced to 0.5 mW power from 2 mW power. The saving is significant considering the power dissipation for the minimum load is only 12 mW.

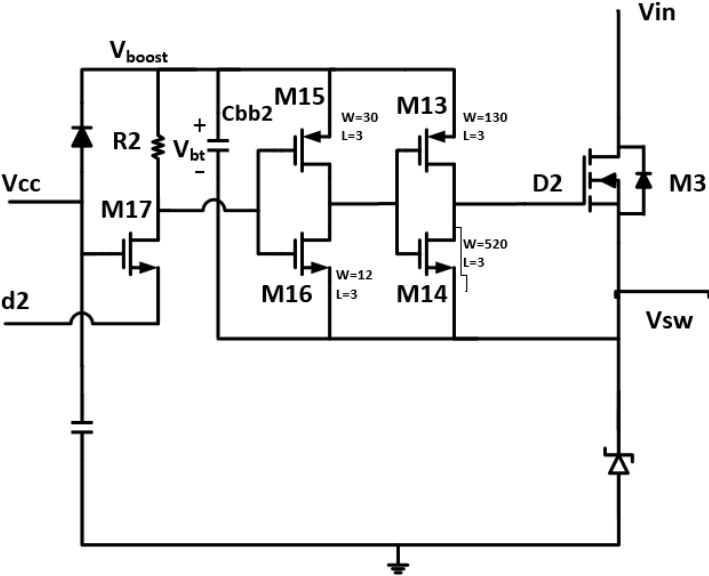


Figure 4.7: The structure of the baby-buck gate driver

In addition, the proposed gate driver intends to address the problems mentioned in Section 2.6 by fully utilizing the parasitic of the MOSFETs. The proposed gate driver design not only eliminates using the above elements to achieve the same function as limited turn-on speed and fast turn-off speed, but also embeds built-in dead-time. Figure 4.8 shows turn on and off transition of the low side gate driver and illustrates how the parasitics help the gate driver

achieve these functions.

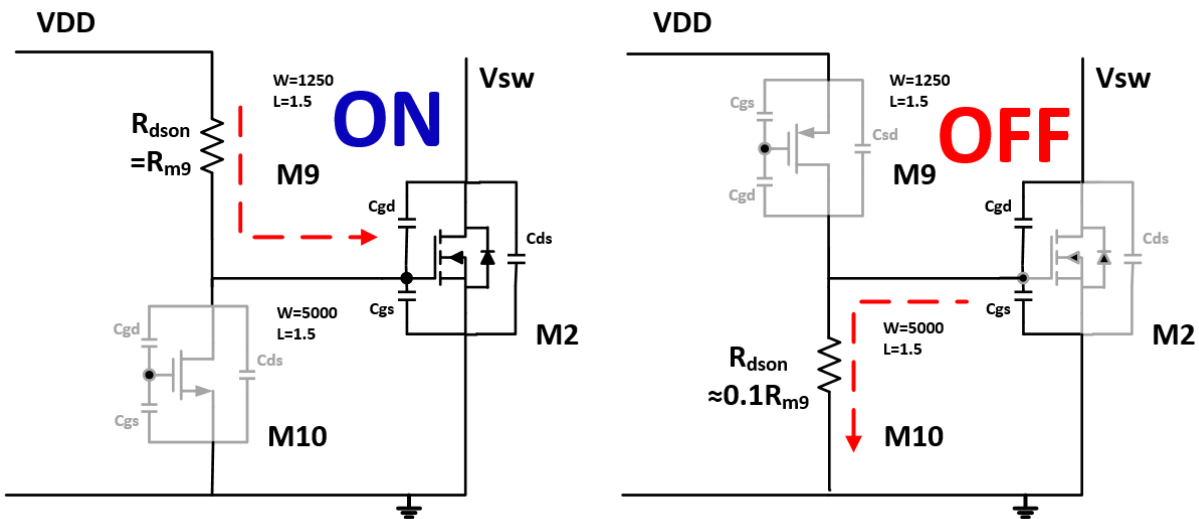


Figure 4.8 The width and length ratios and parasitic capacitances in the heavy top MOSFET

In the above circuit, the width of M9 is 4 times smaller than the width of M10. Taking the inverter consist of M9 and M10 as an operation example: during the turn on time of the M1, the M4 is on and current is charging into the  $C_{gs}$  of M2 through  $R_{dson}$  of M9. Conversely, at the turn off transit of M2, the M10 is on and the current is discharging from  $C_{gs}$  of M2 through the  $R_{dson}$  of M10. Due to the width of PMOS M9 is 4 times smaller than the width of NMOS M10, the  $R_{dson}$  of M9 is approximately 10 times larger than the  $R_{dson}$  of M10, therefore the charging speed is limited by a larger  $R_{dson}$  while the current can be quickly discharged through M10 with a smaller  $R_{dson}$ . In addition, the  $R_{dson}$  of M10 and  $C_{gs}$  of M2 create a small RC delay network. So, the turn on event is delayed while the turn off delay is negligible due to the much smaller RC network constructed by  $R_{dson}$  of M6 and  $C_{gs}$  of M2. At the stage of M11 and M12, the  $R_{dson}$  of M12 and  $C_{gs}$  of M9 forms another delay network which could further amplifies the turn on delay time. Through simulation, the turn on delay is further amplifies to the desired value (20 nS) with proposed width and length ratio in Figure 4.8. With this kind of structure applied to both the high side gate driver and low side gate driver, a delay only happens at a turn on event, act exactly as the dead time provided by the solution mentioned in Section 2.6; however this solution eliminates extra components such as resistors and diodes.

## 4.2.4 Startup Circuit

In section 3.5, the proposed converter demonstrated its ability to regulate the output voltage during transient and steady states through SIMPLIS simulation. However, during the startup, when there is no initial voltage or current applied to capacitor and inductor, the inductor current (/L0/PLUS in Figure 4.9) will be overcharged to 12.5 A at beginning from the cadence simulation. This is because the capacitor voltage or output voltage could not rise quickly to its 1.2 V reference voltage ( $V_{ref}$ ) during this startup period. When the capacitor voltage or output voltage is not high enough to trigger the comparator to turn off  $V_{CO\text{Tin}}$ , the top switch (Q signal in Figure 4.9) is turned on at its maximum duty ratio to charge the inductor and almost no off time for inductor current to be discharged. Therefore, the inductor current continues rise until  $V_{out}$  is greater than  $V_{ref}$ . The overcharged inductor current may damage the inductor itself and introduce current stress on other components.

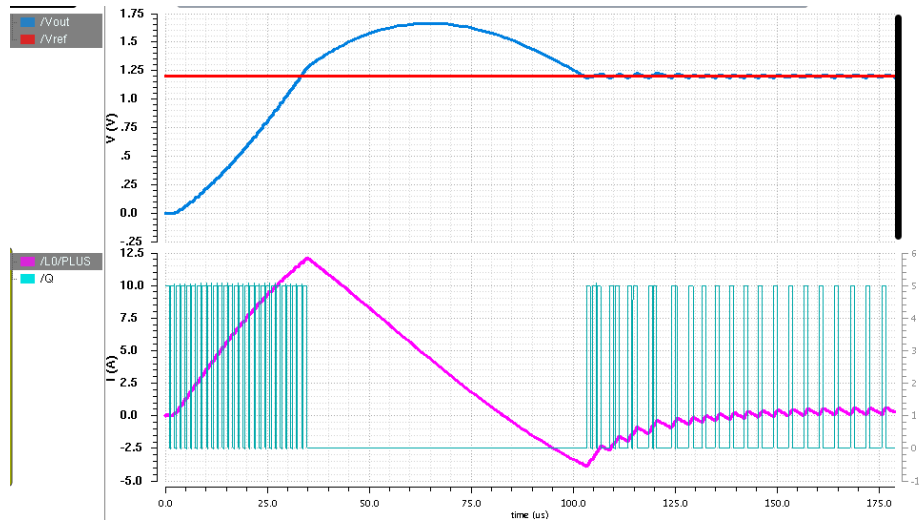


Figure 4.9: The waveform of the inductor current and capacitor voltage (w/o start up circuit)

In order to mitigate this problem, a RC network startup circuit is designed shown in Figure 4.10 to prevent inductor current from overcharged. The intuitive function of this circuit is to introduce a slowly ramped up reference voltage ( $V_{soft}$ ). If this  $V_{soft}$  ramps up slowly, the capacitor voltage is able to reach  $V_{soft}$  at much shorter time and then the controller can turn off the top switch. Therefore, the inductor current will have sufficient time to be discharged during startup as shown in Figure 4.11, and the inductor current is no longer overcharged. Even though

the startup circuit slows down the speed of the converter to reach its steady state, the 1 ms start up time for this RC circuit is negligible in real life.

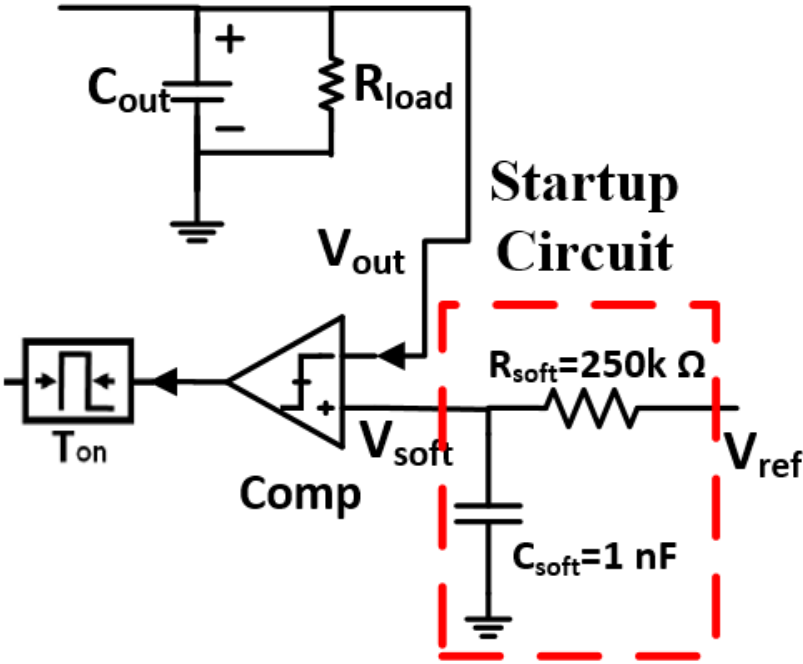


Figure 4.10: R-C start up circuit

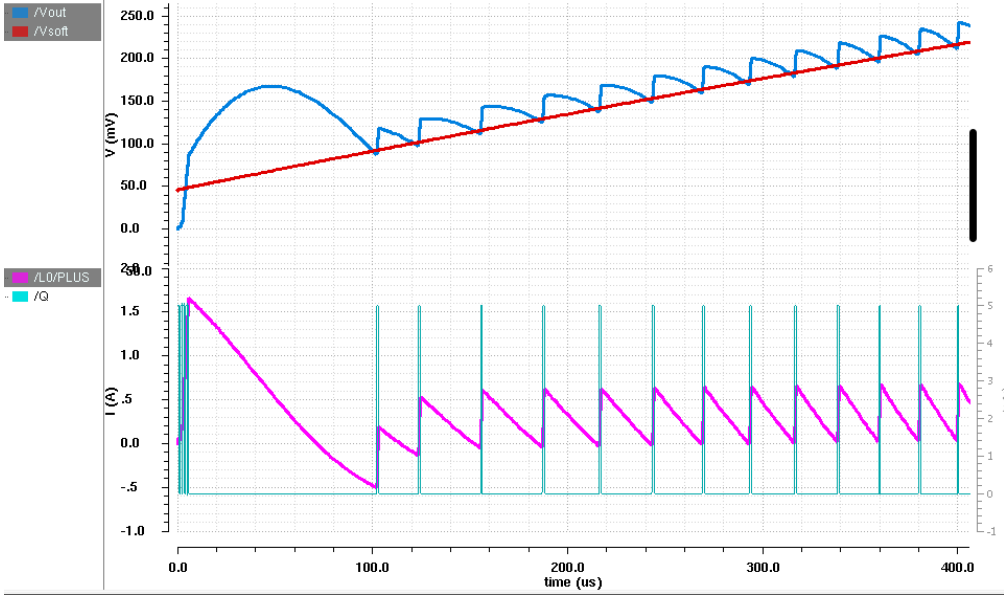


Figure 4.11: The waveform of the inductor current and capacitor voltage (w/ start up circuit)

To be noted, the reference current  $V_{(iref)}$  node is connected to  $V_{soft}$  node as mentioned in 4.2.2. By applying the soft start block to the comparator, the optimum mode selector is also soft

started which has a positive effect on the proposed converter. This is because the heavy-load mode should be active to quickly load up the inductor current and capacitor voltage during startup period. However, at the beginning of that period, the load current is very small which may cause false information to turn on the baby-buck mode. The ideal case is to force the heavy mode to be active even though the load current is small during startup. The soft start circuit just achieves this function by the slowly ramping up the reference current  $V_{(Iref)}$ . As long as the  $V_{(Iref)}$  is smaller than detect load current, the heavy-load mode is selected to be active. Therefore, the designed RC startup circuit is also helpful for the optimum mode selector during startup period.

### 4.3 Other blocks

Other blocks mentioned before are also indispensable to form the entire converter. The necessary blocks are designed in the following orders: comparator, op-amp, and current reference.

Four comparators are implemented in the proposed converter design as two used for COT pulse generator, one used for comparing output voltage shown in Figure 3.5, and one used for the mode selector. Although these four comparators are not quite same due to the usage of different purposes, the basic topologies for these comparators are similar, as they are based on a book reference [35]. By adopting the topology in [35], the proposed comparator is able to achieve fast speed and internal hysteresis because of its positive feedback and Schmitt trigger circuit at second stage. The detailed operation of this type of comparator is illustrated in [35]. In addition to achieve fast speed, these comparators are considered to maintain low power dissipation for improving the overall efficiency of the converter. Thus, the total power dissipation of each comparator is designed to be less than 0.4 mW under 5 V supply voltage while maintaining the propagation delay within 40 ns with a 100 mV overdrive voltage. Figure 4.12 shows detail structure of a comparator example used to compare to the output voltage. In this example, a p-type comparator is adopted because the input common mode voltage range requirement is from ground to reference voltage  $V_{soft}$ , which starts from 0 V as shown in Figure 4.10.

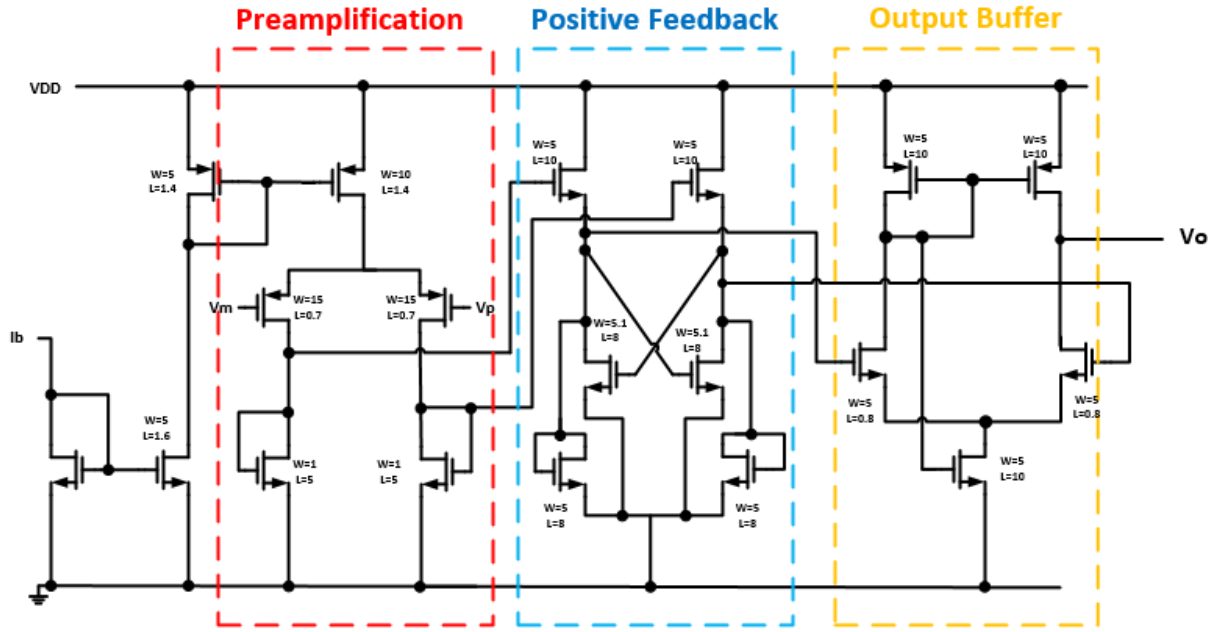


Figure 4.12 The structure of the comparator used to compare to the output voltage

Next, a basic two stage op-amp is designed for current sensor circuit as shown in Figure 4.5. The role of this op-amp is to compose a differential amplifier and the purpose of this differential amplifier is demonstrated in section 4.2.2. According to the target application requirement, the op-amp is designed and the topology of this op-amp is adopted from [36]. The detailed procedure of designing such an op-amp is illustrated in [36]. The additional design consideration of the op-amp is to reduce its power dissipation and achieve high DC gain. The structure of the designed op-amp is shown in Figure 4.12 and its key performances of the proposed op-amp are indicates in table 2 with DC power supply of 5 V. The p-type op-amp is chosen due to the same reason of input common mode voltage range requirement.

Table 2: The key performances of the proposed op-amp

TI 0.25 $\mu\text{m}$ PDK LBC7 CMOS	Performances Specifications
DC Power Supply	5 V
DC Gain (Open-loop gain):	94.7 dB
Bandwidth and Unit gain Bandwidth:	143 Hz and 7.8 MHz
Power dissipation:	0.2 mW
Mode margin and gain margin:	73.8° and 5.5 dB
CMRR:	155 dB
PSRR:	96.1 dB
Slew rate:	4.4 V/ $\mu\text{sec}$
Input common mode range	0 to 3.7 V
Output swing voltage:	3.4 V peak-to-peak



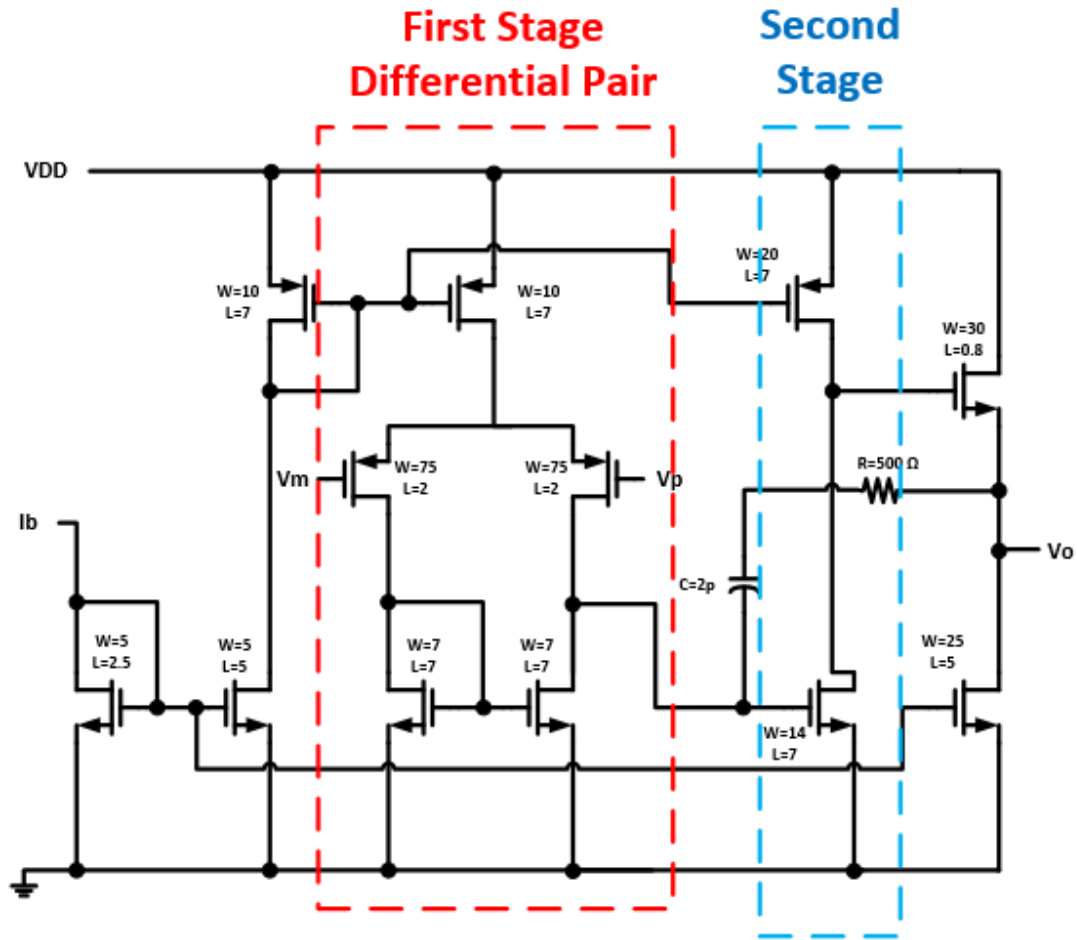


Figure 4.13: The structure of the designed op-amp

Lastly, a current reference circuit with the ability of providing a constant current is designed, because many IC blocks in proposed converter need a reference current. Furthermore, the accuracy of this constant current source is particularly important for the constant on-time pulse generator because the on time of  $T_{on}$  is directly impacted by this current. The Figure 4.14 shows the proposed current reference circuit which adopts the structure in the book [36]. From the analysis of this circuit in [36], the output current of this circuit is independent of the VDD variation, but still a function of process and temperature in CMOS technology. This current reference circuit consistently provides 10  $\mu A$  current to the COT pulse generator and 10  $\mu A$  reference current to other IC blocks.

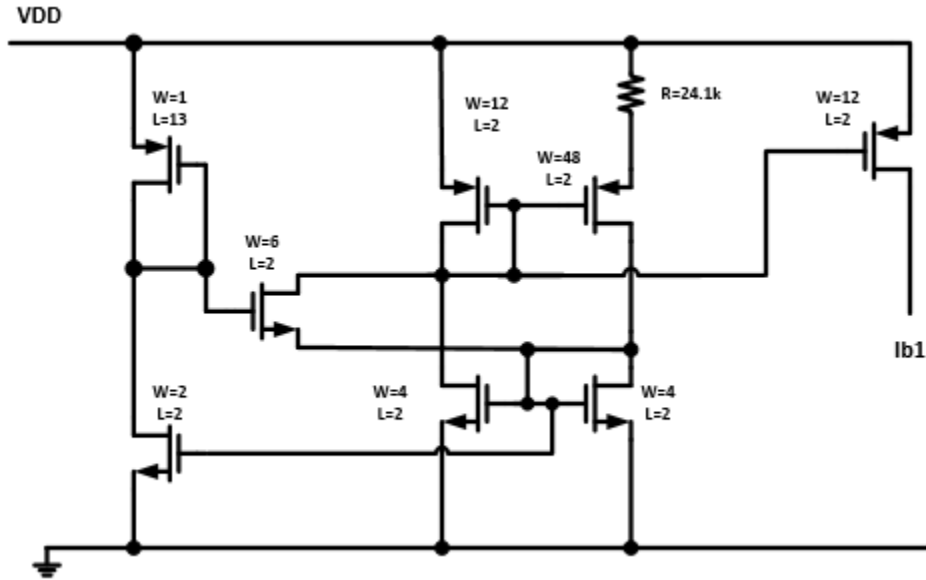


Figure 4.14 The structure of the reference current generator

All the required IC components for the proposed converter are designed and their individual functionality is verified through simulation at different scenarios. The proposed converter was constructed with designed power stage and IC building blocks and the functionality of the converter is illustrated in chapter 5.

#### 4.4 Layout

The structure or appearance of an integrated circuit is revealed only under high magnification. The blueprint of this circuit is called layout and contains the intricate wire connections, silicon doping of the components, and geometric shapes of the semiconductor layers, and the automation process of constructing this integrated circuit is based on the information given by the layout. The layout is often as important as the circuit design of the converter because the behavior of final fabricated integrated circuit chip largely depends on the positions and interconnections of the geometric shapes of the layers [38]. The layout of the proposed design was drawn on the platform of TI 0.25  $\mu\text{m}$  PDK LBC7 and the design of this layout is referenced from the book [38]. The entire layout of the circuit is shown in Figure 4.15 with highlighted main blocks and the entire size of the integrated circuit is 2mm\*2mm. The ESD protection circuit along with the pad was also extracted from the library and embedded into this

layout. The entire design of the proposed converter has been finished and sent to the factory for manufacture in May 2015.

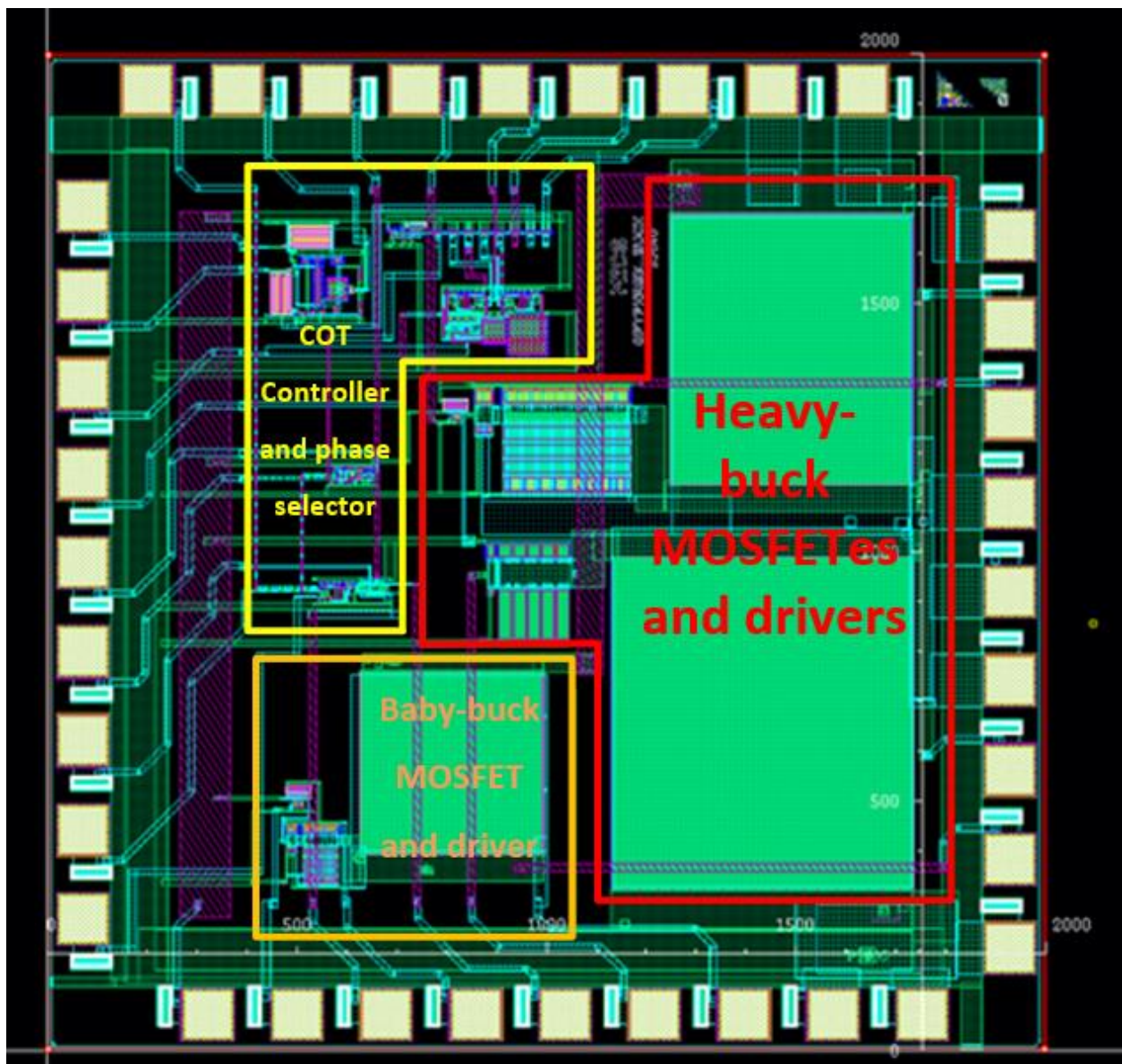


Figure 4.15 the layout of the proposed IC with major blocks highlighted.

## 4.5 Chapter summary

This chapter describes the transistor level circuit designs of the proposed two-mode MOSFET buck converter. The components power stage is selected/ designed to meet the design requirements and achieve high efficiency at different load range. The detailed structure, operation principle, and design consideration of IC blocks are presented in Section 4.2 and 4.3.

Lastly, the entire design was constructed using Cadence tools and the TI 0.25  $\mu\text{m}$  CMOS technology. The final layout has been sent to TI factory for manufacture. The goal of this chapter is customizing all components/circuit blocks to minimize losses, and hence the efficiency of the converter is improved.

# Chapter 5

## Simulation and Measurement Results

This chapter describes the functionality of the proposed converter through simulation. The details of the functionality include steady state waveforms at heavy load and light load, proper mode section and transient response at load variations. Section 5.2 simulates the efficiency of proposed converter throughout the entire load range and this efficiency is compared to conventional buck converter and ON Semiconductor off-the-shelf converter. The chip of Phase 1 is measured and the result is presented in section 5.3. Section 5.4 offers some suggestions on future improvements. Lastly, section 5.5 summarizes the chapter.

### 5.1 Functionality Verification Through Simulation Using Real Components

The functionality of proposed two-mode buck converter was verified by SIMPLIS with ideal components while the proposed converter intends to implement in 0.25  $\mu\text{m}$  CMOS process. Figure 5.1 shows the test bench in Cadence to validate the functionality of the entire circuit and all components are real and from TI library except external components. The proposed converter IC contains many external pins to help testing, and hence each building block used to implement the control network can be isolated from other circuits and fed its own power supply. Therefore, the performance and the power consumption of each control block can be verified individually during measurement. The first step in verifying the operation of this converter IC is to obtain its steady state waveform.

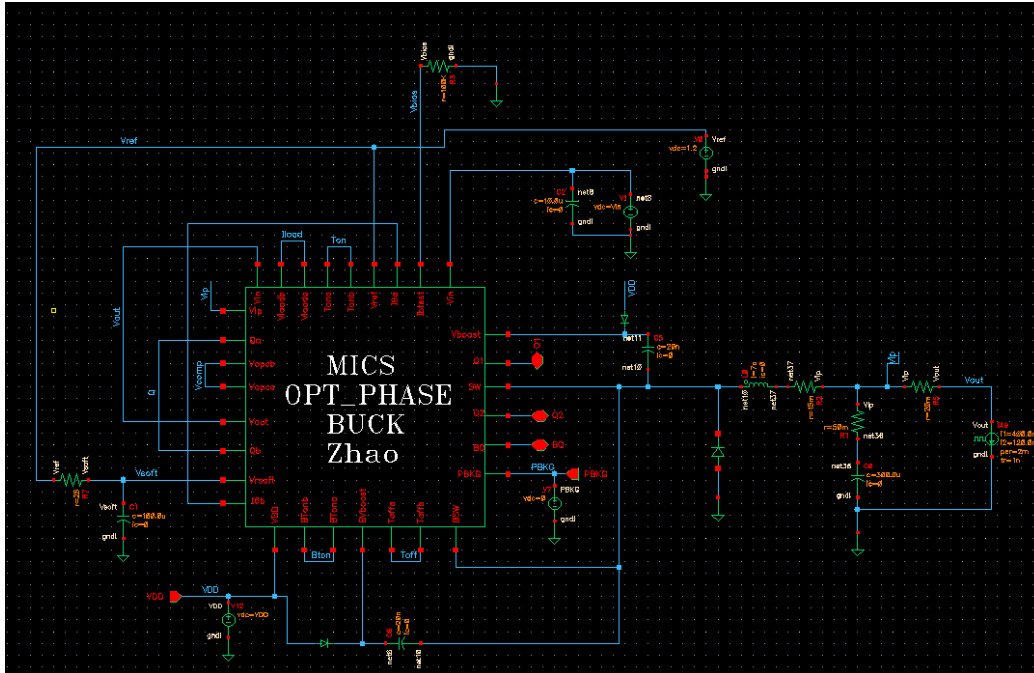


Figure 5.1: The circuit of the proposed converter

### 5.1.1 Steady State Waveform

The above test bench is supplied with an input voltage of 5 V and reference voltage of 1.2 V. The corresponding steady state waveforms of the inductor current, the output voltage, the COT pulse under heavy load (1.2 A) are shown in Figure 5.2. The inductor current in pink in Figure 5.2 indicates that the converter operates in CCM with peak to peak inductor current of 356 mA and the average output voltage is 1.2 V with peak to peak voltage ripple of 16 mV. The on-time of the COT pulse (Q in Figure 5.2) is 0.98  $\mu$ s and the switching frequency of the converter is 265 KHz which is close to the targeted 1  $\mu$ s on time and 250 kHz respectively. The waveform of  $V_{sw}$  is also shown in Figure 5.2.

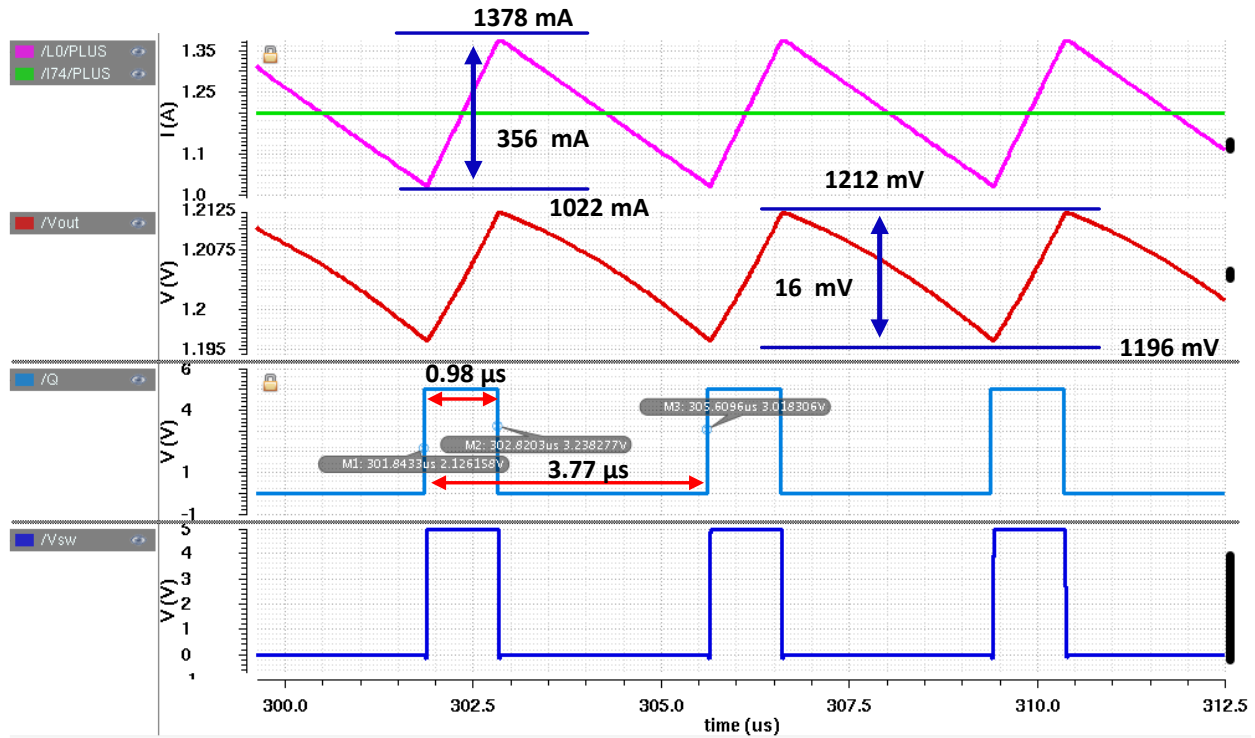


Figure 5.2: The steady state waveforms under full load (1.2 A) of the proposed converter

With the same input and reference voltage setting, the steady state waveform under light load (50 mA) is shown in Figure 5.3. The  $V_{sw}$  voltage and inductor current in pink in Figure 5.3 represents the converter operates under DCM. The peak to peak inductor current remains to be 358 mA while the average output voltage is still around 1.2 V with peak to peak voltage ripple of 17 mV. The on-time of the COT pulse is unchanged at  $0.98 \mu\text{s}$ , but the switching frequency of the converter is reduced to 81 kHz as expected. The reduction in switching frequency comes from increased off-time and helps reduce losses under light load.

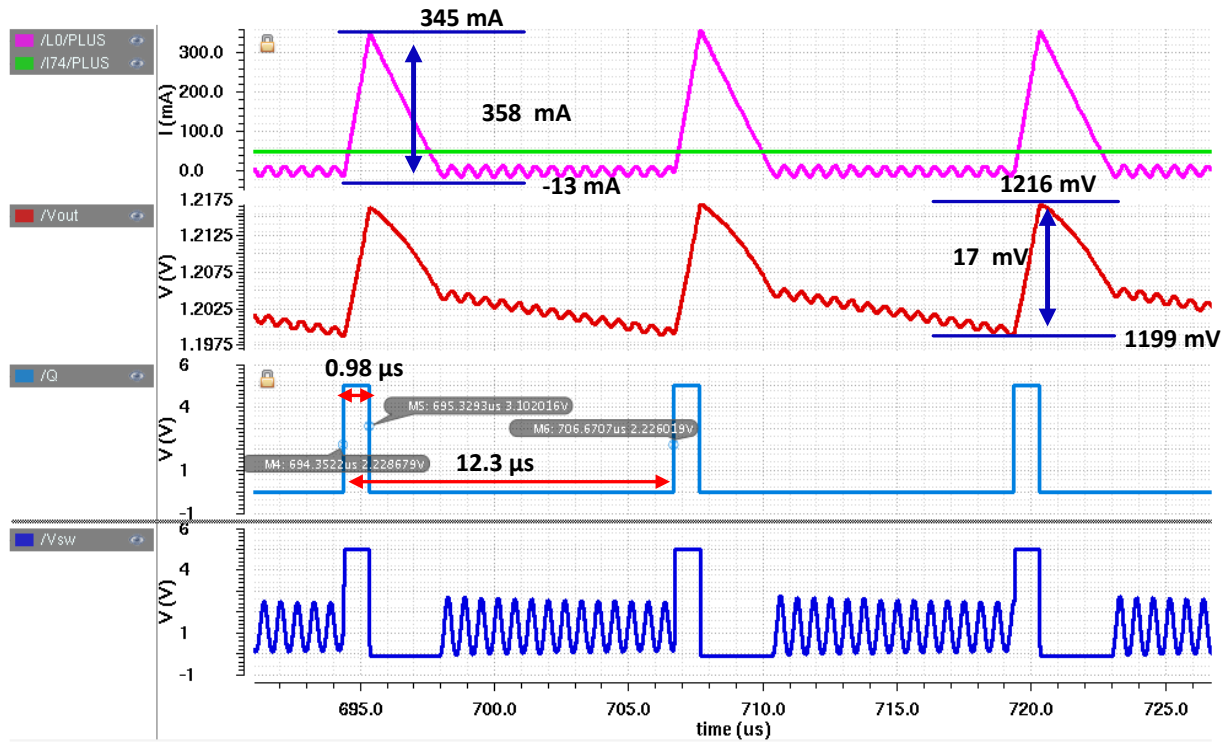


Figure 5.3: The steady state waveforms under light load (50 mA) of the proposed converter

### 5.1.2 The Mode Selection and Transient Response

The ability of the mode selector to choose the proper mode and maintain good transient response during a load variation is also validated through simulation in Figure 5.4 and Figure 5.5. Figure 5.4 displays the transient responses of a load step down from heavy load (600 mA) to light load (100 mA). During this transient, the control signal for heavy buck signal ( $D_{\text{heavy}}$ ) is turned off after little delay. Then the baby-buck control signal ( $D_{\text{light}}$ ) is activated and the switching frequency is reduced accordingly. The output voltage ripple is increased to 34 mV during the mode transition but still within the specification. Figure 5.5 indicates a load step up transition from light load (100 mA) to heavy load (600 mA), the baby-buck control signal becomes off and the heavy buck control signal turns on with an increased switching frequency. The output voltage ripple is 47 mV which is the worst case as the load changes at lowest point of the voltage ripple but still within 60 mV specification.



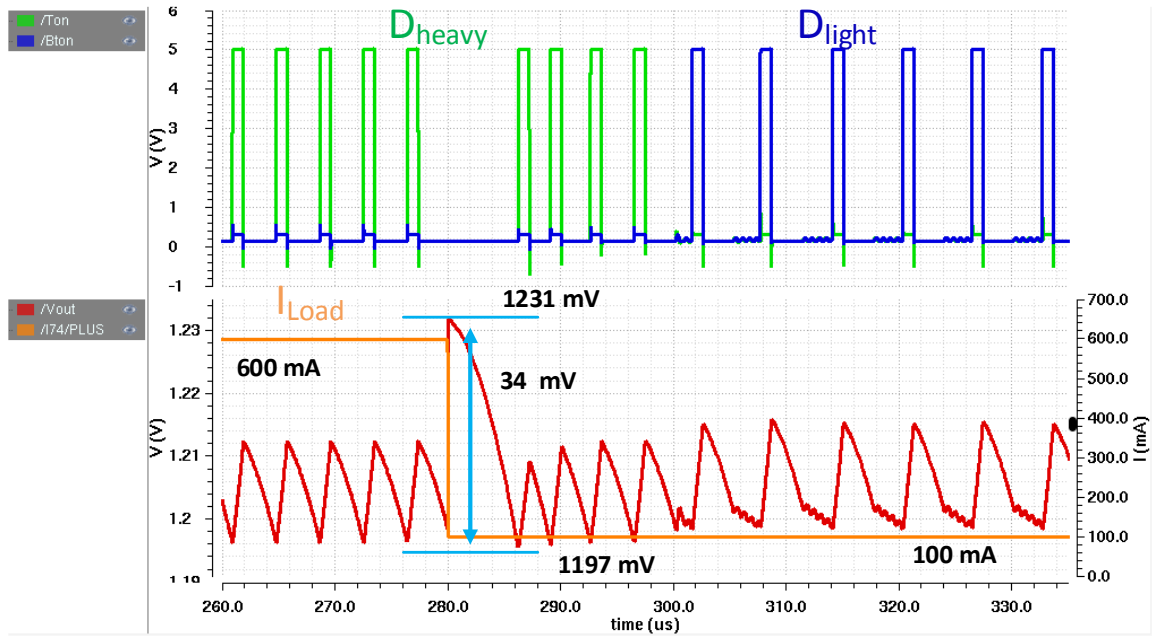


Figure 5.4: Load transient response of a load step down from 600mA to 100 mA

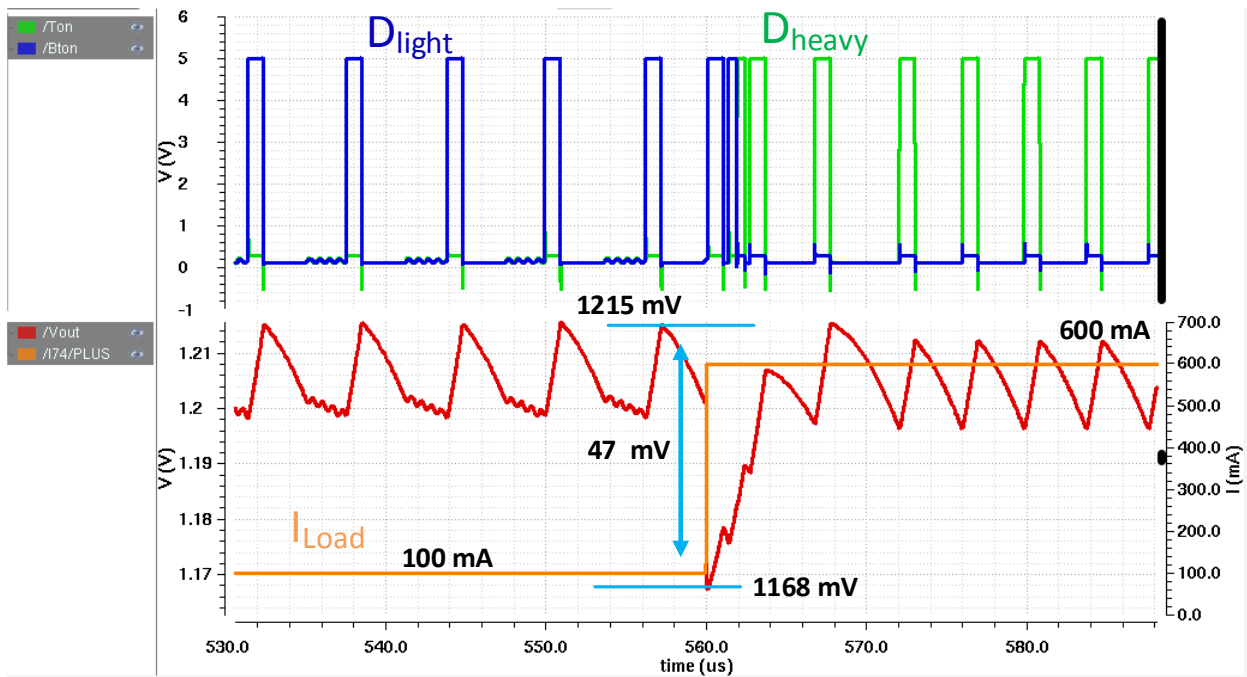


Figure 5.5: Load transient response of a load step up from 100mA to 600 mA

The above waveforms validate the functionality of the proposed converter. Figure 5.2 and Figure 5.3 shows that the converter is stable in different conditions without suffering any

subharmonic oscillation. Figure 5.4 and Figure 5.5 indicate that two modes transition is proper during load changes and transient overshoot/undershoot is within the specification.

## 5.2 Efficiency Through Circuit Level Simulations

The efficiency of the proposed converter is simulated based on the same test bench shown in Figure 5.1. The converter is powered by a 5 V input voltage source and the power for control ICs is supplied by another 5 V control voltage source. The efficiency of the converter is acquired by the load power over the total supply power from input voltage source and control voltage source. Figure 5.6 shows the overall efficiency of the proposed converter through the entire load range. It can be seen that the efficiency is above 70% for the entire load range, with maximum efficiency of 95.5% at load current of 500 mA. The efficiency of entire heavy load from 180 mA to 1.2 A is achieved above 93 %. The lowest efficiency of 73.9% happens at 10 mA load current and the efficiency increase steadily as the load increases.

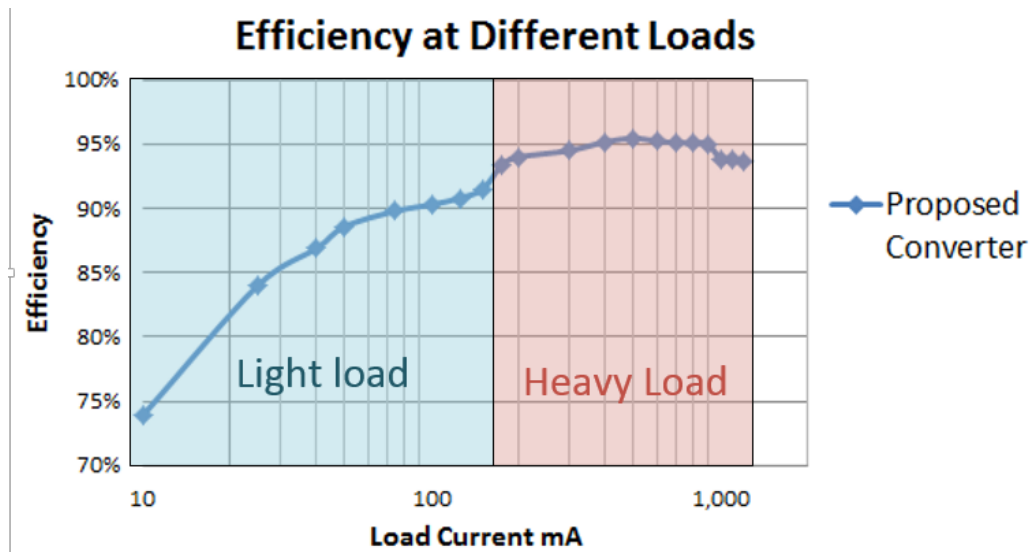


Figure 5.6: Overall efficiency of the proposed converter at different loads

### 5.2.1 Efficiency Comparisons

Figure 5.7 shows the efficiency curve of NCP1597B, a comparable off-the-shelf converter manufactured by ON Semiconductor. This converter has similar structure to the

proposed converter, which integrated its power MOSFETs and controller, and left the inductor and output capacitor as external components. And the operation range is also similar in terms of input voltage, output voltage, and output current load range. The difference is that NCP1597B operates at 1 MHz frequency and the proposed converter has a switching frequency of 250 kHz. For the same voltage conversion of 5 V to 1.2 V, the proposed converter is more efficient throughout the entire range comparing to the NCP1597B.

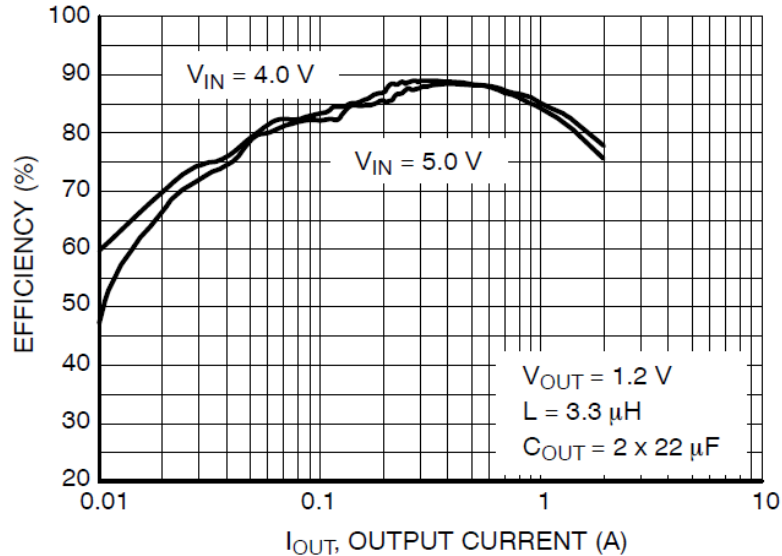


Figure 5.7: Efficiency vs. Output Current for  $V_{out} = 1.2V$  from ON Semiconductor, “1 MHz, 2 A Synchronous Buck Regulator,” NCP1597B datasheet. [Online]. Available: <http://www.onsemi.com/PowerSolutions/product.do?id=NCP1597B>. Used under fair use, 2015.

Another synchronous converter was constructed in order to compare the difference between the proposed converter and the conventional synchronous buck converter approach. The constructed synchronous buck converter consists of exactly same heavy buck power stage and controller as the proposed converter but eliminating the baby-buck and mode selector. Figure 5.8 shows comparisons among the proposed converter, the synchronous converter under same test condition.

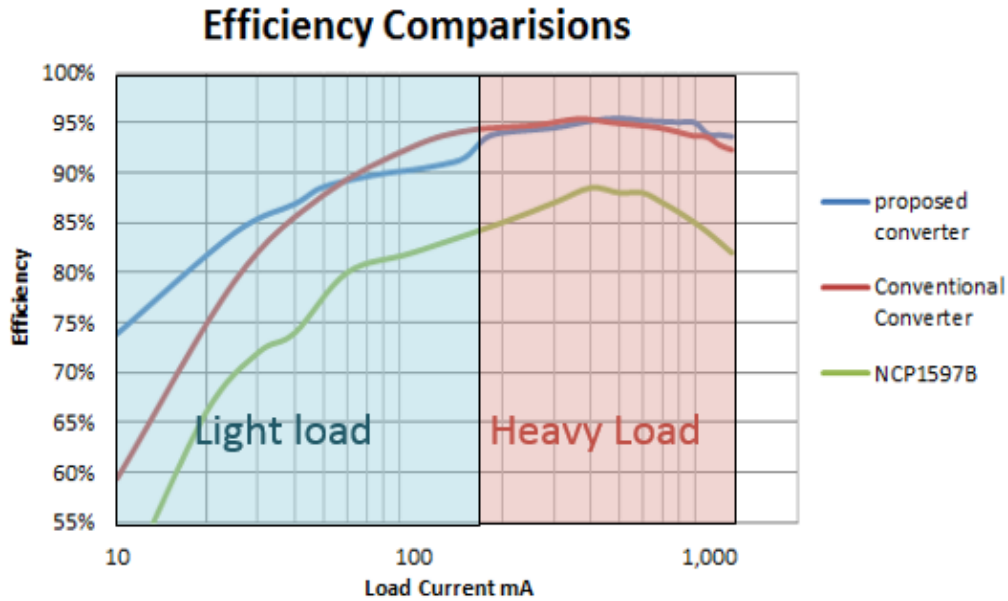


Figure 5.8: Efficiency comparisons

The proposed converter is more efficient throughout the entire range compared to the NCP1597B and it is also 1% higher than the synchronous buck converter near the full load due to the advantage of parallel Schottky diode. Under light load, especially very light load, the proposed converter achieves much higher efficiency than the synchronous buck converter, but there is a slight efficiency drop during the transition from heavy load to a light load. This is because when the proposed converter enters light load, the Schottky diode of the baby-buck takes over the heavy bot MOSFET (M2). However, M2 still has advantage over a Schottky diode in term of loss near load current of 180 mA. The solutions to levitate this issue are provided in detail in section 5.4 and can be implemented in the future fabrications.

### 5.3 Measurement Results of Tape out I

The proposed converter was fabricated in two phases: Phase 1 and Phase 2. The goal of first Phase 1 is to manufacture the converter with open loop which contains the power stage and gate drivers, and Phase 2 is to fabricate the entire converter with close loop including the controller. The chip of Phase 1 has successfully shipped back with its packaging but the chip of Phase 2 is still in the process of manufacture. Phase 1 consist of three blocks: a power stage consist of two MOSFETs, a heavy buck with its gate drivers, and a baby-buck with its gate

driver. All these three blocks are measured to verify their functionalities.

### 5.3.1 Functionality of the Baby-buck and Heavy-buck with Gate Driver

The functionality of the baby-buck with the 5 V input voltage and 5 V gate driver voltage supply is displayed in Figure 5.9 and the 250 kHz PWM signal is generated from function generator. As shown in Figure 5.9, the  $V_{\text{boost}}$  in (green) is always equal to  $(V_{\text{bt}}+V_{\text{sw}})$ , which indicates the bootstrap gate driver works properly. The  $V_{\text{sw}}$  waveform in pink also indicates the converter enters DCM at light load of 100 mA. The right graph of Figure 5.9 shows the waveforms of on time of top MOSFET. The functionality of the heavy buck with same power supply is also displayed in Figure 5.10. Figure 5.10 shows the signal of top gate voltage (D1) in green, control voltage (d1) in pink, and switch node voltage ( $V_{\text{sw}}$ ) in orange for Heavy-buck. The waveform of top MOSFET on period is also shown in Figure 5.10. The waveform of  $V_{\text{sw}}$  indicates the converter operates in CCM which matches the expectation and the D1 is  $(V_{\text{bt}}+V_{\text{sw}})$  when it is on.

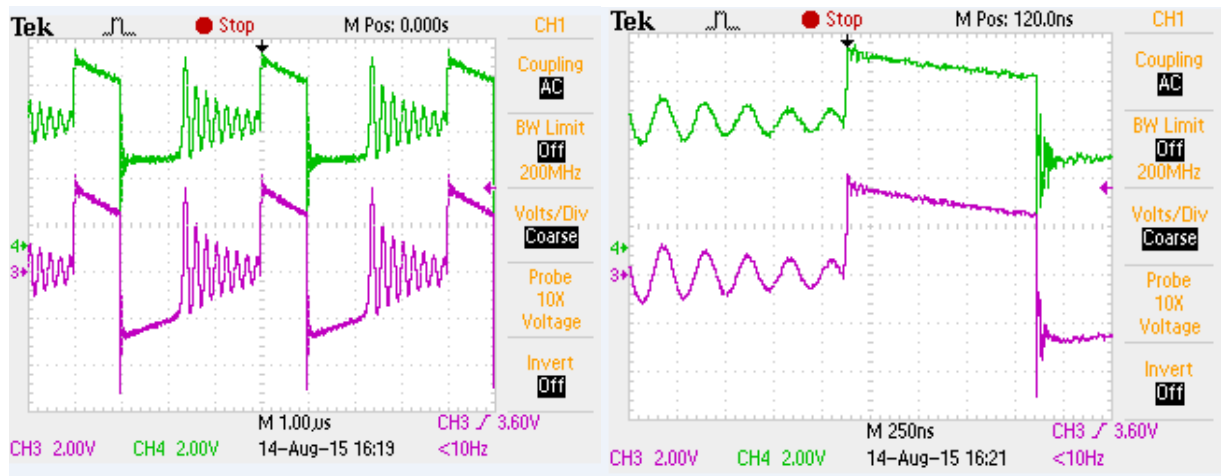


Figure 5.9: Baby-buck  $V_{\text{boost}}$  (green) and Baby-buck  $V_{\text{sw}}$  voltage (pink), and on period of top baby MOSFET

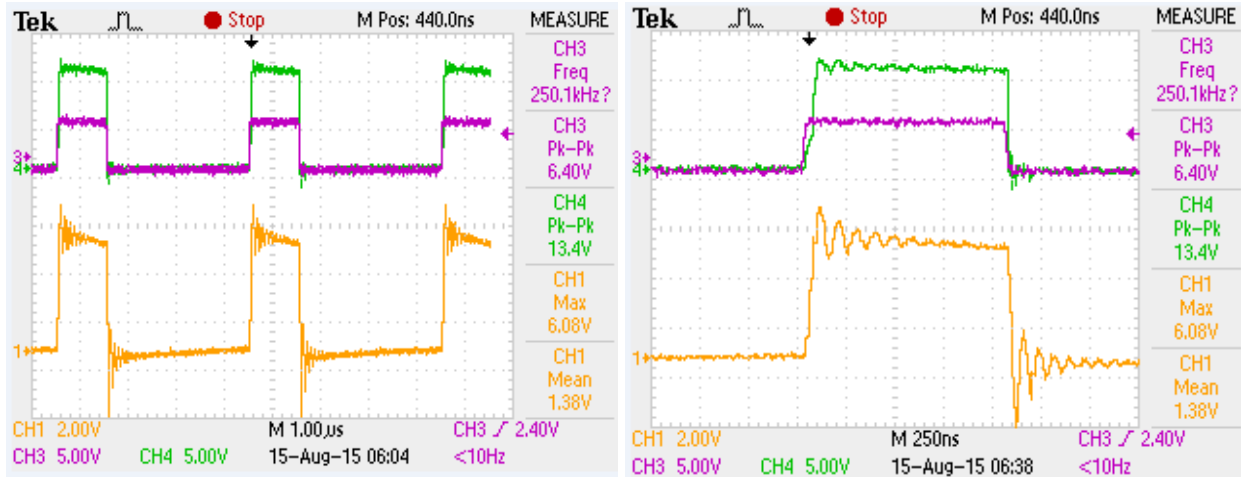


Figure 5.10: Heavy-buck top gate voltage, control voltage and switch node voltage, and on period of top heavy MOSFET

Figure 5.9 and Figure 5.10 demonstrates the functionality of the proposed design in Phase 1. However, due to the large ringing at turn on and turn off instance of  $V_{sw}$  shown in Figure 5.9 and Figure 5.10, the efficiency suffers. Besides, a larger ringing may damage the device or create a shoot through. This issue is further discussed in section 5.4 and will be improved during future fabrication.

### 5.3.2 Measured functionality and efficiency of power stage

The two MOSFETs power stage works fine and the efficiency of this circuit in Phase 1 is measured as shown in Figure 5.11 and it peaks at 87% with 280 mA (330 mW) load. This circuit is measured by directly connecting the two gates of two power MOSFETs to a function generator, and the function generator provides two control signals with dead time and control the gate to turn on and turn off the device. Despite this power stage is directly driven by the function generator which introduces a lot of turn-on and turn-off losses due to its limited drive current capability and sufficient amount of dead time (3%) applied to avoid shoot through, the efficiency is reasonable okay for this power stage to be used as a backup power stage in Phase 1.

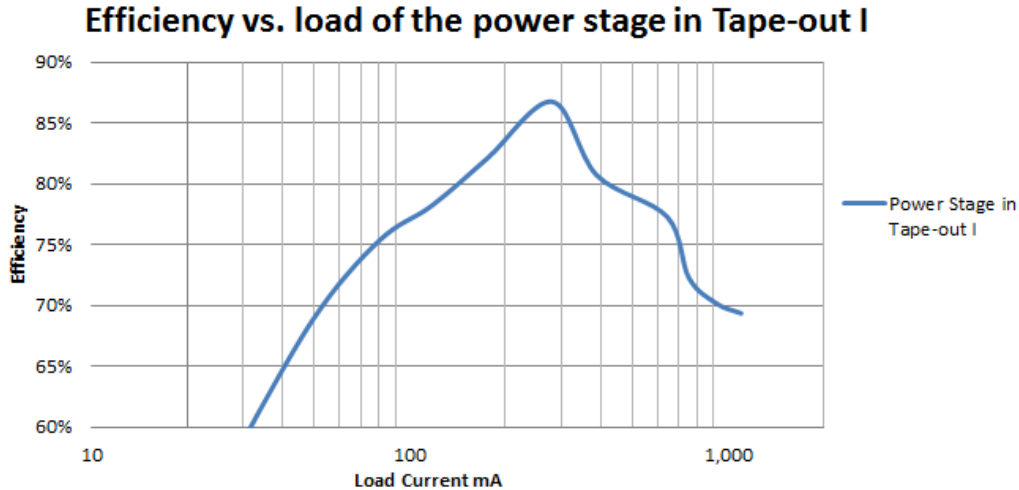


Figure 5.11: Efficiency vs. load of the power stage in Phase 1

## 5.4 Future improvements

As mentioned in section 5.2.1, efficiency drops at the transition point from heavy load to light load due to the bigger conduction loss contributed by the Schottky diode. In Zhou’s method, discussed in section 2.5, the Schottky diode proves its benefits of simple implementation and improves light load efficiency by entering DCM. In this case, the simplest solution is to adjust the transition point to a lower load current such as 70 mA where the diode becomes more advantaged than the CCM operation MOSFET. A more complicate method is to replace the proposed diode baby-buck to a synchronous baby-buck which means replace the Schottky diode to a small MOSFET, and include a low power zero current detector (ZCD) to shut down bot MOSFET when inductor current reach zero. Designing the ZCD must be done with power consumption in mind and it is still a challenge task. The study of ZCD circuit is still a hot topic [40][41][42] now. By adopting this method, the efficiency will boost at 180 mA transition point. However, the efficiency might drop at light load due to the power consumption of ZCD control circuit. Furthermore, the heavy load efficiency might suffer slightly during the dead time of two switches. A more advanced solution is presented as shown in in Figure 5.12, which the small MOSFET (M4) is not used to replace the diode but added in parallel with the diode. The heavy load efficiency will remain high as the operation stays unchanged. At middle to light load, M3 and M4 will be activated with ZCD control to improve transition efficiency and reduce

frequency. At very light load, the converter can shut down the ZCD control, only the Schottky diode and M3 are active for power conversion which will be more efficiency at very light load. For other high power applications, a third or even more modes can be integrated to the proposed converter to boost the overall efficiency.

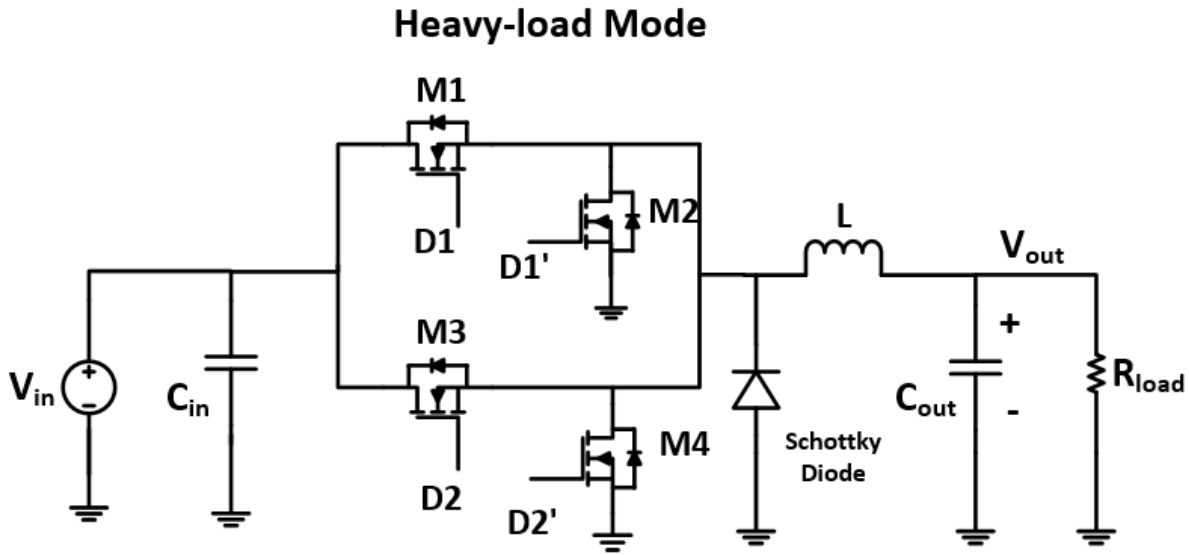


Figure 5.12: The schematic of the proposed method for future tape-outs.

In section 5.3.1, two issues are discovered. The first issue is the switch node turn off ringing. This ringing is caused by the turn off ringing of high side gate voltage. As the input voltage increases, this undesired gate voltage turn off ringing is also increased and may introduce a turn on moment for top MOSFET, which creates a shoot through and may damage the system. The application note [43] mentioned that this ringing maybe from trace parasitic inductance created by the long traces or poor layout between the gate driver and the gate of MOSFET. This layout issue was not been aware of during the first tape-out, but for the future tape-outs, the drawing on layout for this part should be particularly careful. Another issue is the switch node turn on ringing which is very common for all synchronous buck converters. The simplest solution is to select the MOSFET with a higher breakdown voltage margins to handle it at the cost of high FOM. [44] [45] provided several methods to reduce switch node ringing which will be implemented in the future tape-outs.



## 5.5 Chapter Summary

This chapter presents the performance of the proposed integrated optimized MOSFET buck converter. Because the chip of Phase 1 is still in the process of manufacture, the simulated waveform of the converter at steady state, reaction of the mode selector between mode transition, and transient response from a load variation are used for validation the functionality of the circuit. The efficiency of the proposed converter is also simulated and the results meet the design objective of improving light load efficiency. In addition, this efficiency is good when compared to an off-the-shelf product. The measured results of Phase 1 validate the functionality of the fabricated circuit and the efficiency of power stage is also presented.

# Chapter 6

## Conclusion

The power consumption of target smart cameras application varies significantly between sleep mode and active mode, and smart cameras operate in sleep mode or light load for majority of time. Therefore, In order to extend the battery life of smart cameras, it is essential to increase the efficiency of power converters, especially for light load. This thesis research investigated a power converter to supply power for the microprocessor of a smart camera. The input voltage of the converter is 5 V, and the output voltage is 1.2 V with the load ranging from 10 mA (12 mW) to 1200 mA (1440 mW). The conventional buck converter is typically optimized for high efficiency at maximum load at the cost of light-load efficiency. A converter is investigated in this thesis to improve light load efficiency, while being able to manage heavy load, to prolong the battery life of smart cameras.

The proposed converter employs two modes, a baby-buck mode and a heavy-load mode, in which each mode is optimized for its respective load range to achieve high efficiency throughout entire range. The heavy-load mode converter adopts the conventional synchronous buck approach, as it generally achieves high efficiency at heavy load. However, the synchronous buck approach is inefficient at light load due to the large switching, driving, and controller losses. The proposed baby-buck mode converter employs the following schemes or technique to reduce those losses. First, the baby buck mode converter adopts pulse frequency modulation (PFM) with discontinuous conduction mode (DCM) to lower the switching frequency at light load, so that switching and driving losses are reduced. Second, the simplest control scheme, constant on-time  $V^2$  control, is adopted to simplify the controller and hence minimize the controller power dissipation. Third, the top switch of the baby-buck mode uses a small MOSFET, which is optimized for light load, and the bottom switch uses Schottky diode in lieu of a MOSFET to simplify the COT  $V^2$  controller. Fourth, the proposed converter combines the heavy-load and baby-buck mode converter into a single converter with a shared inductor, capacitors, and the feedback controller to save space. Finally, a simple and low power feedback

controller with an optimum mode selector, a COT  $V^2$  controller, and gate drivers are designed. The optimum mode selector selects an appropriate mode based on the load condition, while shutting down the opposing mode. The COT  $V^2$  controller reduces switching frequency as load decrease at light load. The simple gate driver embedded build-in dead time by introducing different rising and falling time of the buffer.

The proposed converter was fabricated in CMOS 0.25  $\mu\text{m}$  technology in two phases. Phase 1 contains design of the proposed converter with open loop, and its functionality is verified through measurements of test chips. Phase 2 includes the entire converter design with the feedback controller. Since the test chips of phase 2 are not delivered, yet, its functionality during the steady state and transient responses are verified through simulations. Simulation results indicate that the efficiency of the proposed converter ranges from 74% to 93% at 12 mW and 1440 mW, respectively. This result demonstrates that the proposed converter can achieve higher efficiency for the entire load range when compared to an off-the-shelf synchronous buck converter.

A few future research areas to improve the proposed two-mode buck converter are suggested below.

- Although the light load efficiency is improved compared to conventional buck converter, the transition load efficiency still leaves room for future improvement. Adding a ZCD and a synchronous MOSFET in parallel with the Schottky diode is one possible solution. ZCD allows synchronous buck converter to enter DCM and reduce frequency. To be in mind, the ZCD design must be done with low power consumption.
- The layout and packaging in phase 1 introduce significant amount parasitics which cause large ringing at turn on and turn off instance and may damage the device. Further investigations and studies in layout and packaging could reduce parasitics and alleviate issues from ringing.
- The load current sense resistor and current sense IC for mode selector consume considerable power at maximum load, (2.2% power at 1440 mW load). Further investigation into ZCD to control mode selector could increase heavy efficiency.

The above items are left for future research upon proposed converter for low power

applications.

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