Design Optimization of Hybrid Switch Soft-Switching Inverters using Multi-Scale Electro-Thermal Simulation

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Abstract

The development of a fully automated tool that is used to optimize the design of a hybrid switch soft-switching inverter using a library of dynamic electro-thermal component models parameterized in terms of electrical, structural and material properties is presented. A multi-scale electro-thermal simulation approach is developed allowing for a large number of parametric studies involving multiple design variables to be considered, drastically reducing simulation time.

Traditionally, electro-thermal simulation and analysis has been used to predict the behavior of pre-existing designs. While the traditional approach to electro-thermal analysis can help shape cooling requirements and heat sink designs to maintain certain junction temperatures, there is no guarantee that the design under study is the most optimal. This dissertation uses electro-thermal simulation to guarantee an optimal design and thus truly minimizing cooling requirements and improving device reliability.

The proposed optimization tool is used to provide a step-by-step design optimization of a two-coupled magnetic hybrid soft-switching inverter. The soft-switching inverter uses a two-coupled magnetic approach for transformer reset condition [1], a variable timing control for achieving ZVS over the entire load range [2], and utilizes a hybrid switch approach for the main device [3].

Design parameters such as device chip area, gate drive timing control and external resonant capacitor and inductor are used to minimize device loss subject to design constraints such as converter minimum on-time, maximum device chip area, and transformer reset condition. Since the amount of heat that is dissipated has been minimized, the optimal cooling requirements can be determined by reducing the cooling convection coefficients until desired junction temperatures are achieved.

The optimized design is then compared and contrasted with an already existing design from the Virginia Tech freedom car project using the generation II module. It will be shown that the proposed tool improves the baseline design by **16%** in loss and reduces the cooling requirements by **42%**. Validation of the device model against measured data along with the procedures for device parameter extraction is also provided. Validation of the thermal model against measured data is also provided.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

Model Based Engineering (MBE) is a new industry wide initiative where computer based modeling and simulation is being used more and more for design optimization of power converters for reduced size, weight, power, and cost (SWAP$). MBE allows the designer the ability to conduct parametric studies using design of experiments (DOE) tools and engineering optimization algorithms early in the design phase to achieve the most cost effective and optimized design. Having reliable, fast and high fidelity simulation models is very important for MBE studies. This dissertation considers electro-thermal simulations using a multi-scale simulation approach to achieve design optimization of power electronic circuits, in particular the optimization of a hybrid switch soft-switching inverter.

Electro-thermal simulations have been used extensively in research publications. The main objective, typically, is to accurately predict the junction temperature of a power electronics module. In order to do so, a device model capable of calculating the dissipated power is coupled with a thermal component model that uses the dissipated power from the electrical model as an input to calculate junction temperature. The junction temperature prediction can be the instantaneous junction temperature within a switching cycle, the junction temperature averaged over a switching cycle, or the junction temperature averaged over the switching cycle and inverter cycle. Most electrical device models average the dissipated power over a switching cycle and therefore the electro-thermal model can only predict junction temperature variation within the inverter line cycle [4].

Chapter 1

The pursuit of increased power density in high temperature environments such as electric vehicle drive requires multi-chip power modules. In order to achieve these densities within multichip power modules containing single-phase and three-phase inverter bridges, soft-switching techniques are required. Soft-switching techniques allow for the reduction or elimination in switching loss by turning a device on under zero voltage switching (ZVS). High density soft-switching modules may contain multiple IGBT, MOSFET, and diode chips mounted on a common direct bond copper (DBC) and baseplate layers. As a result of the close proximity of the IGBT, MOSFET, and diode chips, lateral heat spread due to thermal coupling between chips must be considered within the electro-thermal models. Therefore electrical device models are combined with multi-dimensional thermal component models capable of representing any thermal geometry and boundary condition. The thermal component models in this dissertation are based on a 3-D FDM solution to the heat conduction equation for a multichip module which considers the imperfect thermal contact between materials and thermal-dependent parameters such as the nonlinear thermal conductivity of silicon. The electrical models are physics-based with behavior based temperature dependent parameters extracted over temperature.

Chapter 2 Literature Review

2.1 Electro-thermal Model – Electrical

The current state of art electro-thermal models in literature are based off electrical models which are either behavior models consisting of ideal switch with appropriate on-state resistance if MOSFET or constant voltage drop if IGBT or diode in parallel with a linear or nonlinear capacitor. Unlike the behavioral SPICE model proposed in [5], most behavior models have no way to predict instantaneous dissipated power. Most behavioral models such as the ones given by vendors calculate power by multiplying the voltage across the device by the current through the device. It is incorrect to assume that the result is the instantaneous dissipated power. This is because many applications use soft-switching techniques and therefore the energy may be circulated through the capacitance with external resonant elements in the circuit and may not dissipate. Therefore an average operator over the entire switching cycle is necessary. In-sight into the power dissipated during the switching dynamics is therefore lost.

The most widely used method for implementation of the electrical device models is to use lookup tables or curve fits based on loss estimations obtained from a device datasheet [6] , [7] , [8] and [9]. This method is reasonable for determining conduction loss since conduction loss is easily modeled with a linear relationship to a device parameter such as threshold voltage and R_{dson}. When using the device look up tables for determining switching loss however, the energy curves available have already been averaged over a switching cycle under a specific test condition such as gate drive resistance and voltage. This may be good enough if the device model is used in the same manner such as a hard switching application. However the energy curves are not valid for conditions where soft-switching techniques or gate drive timing

techniques are used to reduce switching loss. There is no way to reproduce the instantaneous power form a datasheet provided energy curve. This can be a major drawback if design optimization is desired. Design optimization where the device can be modified through parametric study is not achievable with this method. In addition studying the instantaneous junction temperature during the switching events is not possible either.

The only way to actually capture the instantaneous dissipated power is to use physics-based device models capable of calculating dissipated power at any instant in time during the switching cycle. With that said, the physics-based device models can be used to generate energy curves, proposed in this dissertation, under the conditions of soft-switching and gate drive specific timing as this lends itself to faster simulation while conducting the parametric studies. This will be discussed later.

A physics-based electrical model is proposed in [10] where the ambipolar diffusion equation, describing the dynamic charge, is solved for the IGBT using a Fourier-series-based solution method. After finding the excess carrier concentration, the voltage drop across the junction and depletion region are computed. This model provides an accurate description of the physics of the device but parameter extraction for the internal device parameters or instruction on scaling parameters is not described. It is not easily used by the engineer if parametric study is desired.

A physics-based model with scalable parameters lends itself to design optimization. This dissertation considers the Hefner IGBT model proposed in [11] . One of the major advantages of this model is that it offers a reference area parameter which can be used for design optimization. This allows a particular device to be characterized under a known device area and the user can then explore parametrically the effects of a larger or smaller device area under similar device fabrication. Typically devices with the same voltage rating qualify as the same device

fabrication. The parameters for the physics-based device model are captured and characterized over temperature using the techniques in [12] allowing parametric studies to include the effects of temperature in the design optimization. It is noted that the temperature dependence of the physics-based parameters are based on curve fit from measurement. In other words, while the electrical device is physics-based, the temperature dependence of those parameters are behavioral. A physics-based model for a CoolMOS MOSFET is developed from the Hefner model in [13] since the internal Hefner IGBT model contains an equivalent internal MOSFET. Therefore the same parameter extraction tools can easily be extended to the CoolMOS MOSFET. A similar physics-based device model is available for the diode is presented [14]. Device parameters are extracted over temperature using very similar procedures and test circuits as the Hefner IGBT model. Device scalable parameters are also available for parametric evaluation for the diode and MOSFET models.

2.2 Electro-thermal Model - Thermal

The current state of art for the thermal portion of the electro-thermal model is to use either Fourier series based solutions to the heat conduction equation, finite difference solutions to the heat conduction equation or RC ladder networks derived from thermal transient impedance curves or 3D FEM simulations.

Fourier series-based thermal models proposed in [10] , [15] , [16] , [17] and [18] are parameterized in terms of structural and material properties but valid only for 1D or 2D single chip configurations where there is only a single heat source. However this method, when appropriate, is very fast in that a numerical iteration is not required to compute the Fourier series. It is in essence a “closed-form” or analytical solution. In [19], [20] and [21] a 3D Fourier series-

based thermal model with multiple heat sources and multiple layers with different cross sectional area is considered. Feedback loops are used to force the appropriate boundary conditions between multiple layer interfaces involving different materials. Material interfaces with different cross-sectional area are accounted for by increasing or decreasing the number of Fourier terms appropriately. This method is not a full analytical solution to the heat conduction equation and still relies on some numerical solution to determine the Fourier coefficients. Therefore, an ordinary differential equation (ODE) solver is still required from a simulator such as MATLAB Simulink. The increased simulation speed that typically results from a Fourier-based solution is further decreased by requiring an additional feedback loop to ensure the proper boundary conditions between material interfaces. The accuracy of the solution is therefore determined by the size of the feedback gain, which results in longer simulation time as the gain is increased. While Fourier-based methods are advertised to be much quicker than finite difference methods (FDMs), the computation savings may not be as obvious once a full 3-D multichip chip configuration is considered requiring large feedback gains and a large number of Fourier terms solved numerically for accurate solutions. In addition, the Fourier-based solutions do not consider the imperfect contact that may exist between materials that can result in significant temperature differences. Also, it is not easy to include temperature-dependent properties such as the nonlinear thermal conductivity of silicon.

The most widely published electro-thermal models in past literature assume single-chip configurations where assumed one-dimensional (1-D) heat conduction is all that is required to predict junction temperatures. The authors in [22] and [23] a theoretical analysis known as the TRAIT method uses the first n terms of a time-constant spectrum obtained from thermal transient measurements to generate equivalent Cauer RC cells. The thermal transient measurements are

generated from a heat source caused by a down step variation of heating power. It is noted that only the Cauer cells contain R and C values with true physical meaning contrary to the Foster cells. This is only true however if the body is considered one dimensional. Additional thermal influences such as plastic coverage is considered using the same TRAIT algorithm however the calculation of all the Rs and Cs cannot be applied with physical meaning. In the second paper by the same authors, the TRAIT method is applied to structures involving heat fluxes with three dimensional dependence. The conclusion was the Cauer method can still be applied for three dimensional structures but the resulting Rs and Cs do not have any physical meaning beyond one dimensional heat conduction. In [24], the extraction of thermal time constants for a Cauer thermal network much like the method in TRAIT however the method for the extraction is simplified. The uniqueness of the RC compact model is an introduction of time constant based on Elmore delay, which faithfully represents the propagation delay of the heat flux through each layer in the total system. Each of these methods results in com-pact models parameterized in terms of structural and material properties. But these models are only valid for a 1-D thermal profile where only a single chip is considered and an additional model synthesis step is required from measurement or three-dimensional (3-D) FEM analysis. In order to model lateral heat spread due to thermal coupling within multichip modules, a method that includes multidimensional (>1-D) heat conduction has to be considered.

The most widely used method for thermal modeling of multichip power modules involve curve fitting Foster RC cell net-works from data sheet provided thermal transient curves or 3-D FEM solvers like Kojima et al. [25], [26], [27] and [28]. The Foster network cells are determined from a thermal impedance matrix extracted from a 3-D FEM solver. The impedance matrix describes the self-heating of each chip within the module and the heating of a single chip due to the heating

of neighboring chips. Therefore, a full 3-D model that faithfully represents the lateral thermal interaction among neigh-boring chips is achieved. This method faithfully describes a 3-D module and the strong thermal coupling between chips but re-quires a full 3-D FEM and model extraction for any new module configuration resulting in an extra model synthesis step.

Walkey et al. [29] and [30] present a multichip compact thermal model using voltage controlled voltage sources to represent chip to chip thermal coupling. A multi-chip compact thermal model using voltage controlled voltage sources to represent chip to chip thermal coupling. Each device is modeled with a thermal resistance related to the geometry of the device and its own power dissipation and a coupling coefficient, implemented with voltage controlled voltage sources which define the relationship between the temperature of each device and its contribution to the temperature of the coupled device. The generation of the model still involves extraction of parameters from either an analytical or numerical solution to the heat equation to generate a per device thermal model but does not require further synthesis steps for different power distributions.

In [31] the addition of current sources representing chip to chip coupling are inserted at various locations into a foster net-work. The locations of these current sources are determined from 3D FEM and are not necessarily valid if the power levels change significantly in the circuit simulation.

The method presented in [32] results in a compact thermal model where 3-D heat flow is accounted for by using appropriate symmetry in the discretization of the heat equation. The thermal package model, for example, describes the two-dimensional (2-D) later heat spreading by considering an effective heat flow area approach. This method was extended to thermal component models for multichip considerations in [33] where neighboring chips sharing a

common DBC were assumed to have the same power dissipation. However, in conditions where there are multiple chips with varying power dissipation sharing a common DBC, the effective heat flow area is not well known ahead of time. And in these cases, 1-D heat flow cannot necessarily be assumed.

The authors in [34] presented a boundary dependent circuit model and compared the results to results obtained from the method in [32]. The author concludes that the popular method of assuming a fixed heat spread angle [35] is not as accurate when certain boundary conditions are imposed. A series of factorial designs is conducted using 3D FEM with mesh optimization capability to obtain the effective heat flow area based on different boundary conditions. The results are mapped to Cauer networks where the thermal resistances and capacitances are determined from polynomial fits obtained from the factorial design iteration. This method proves to be very accurate and can be realized with simple Cauer circuits which can run fast in simulation. However it is pointed out that the proposed method forces neighboring die to be sufficiently far away from each other to avoid thermal interaction. This does not necessarily lend itself to dense power module design where adjacent chips will see strong interference between each other, but does prove to be more accurate than the traditional approach of assuming fixed heat spread angles without consideration of boundary condition. In addition an additional synthesis method is required through 3D FEM to generate the thermal model.

In [36], an analytical based solution to the heat equation based on a greens function representation of the temperature field of a three dimensional system was presented. However the solution requires matrices to be determined through a least squares fit to a thermal transient heating curve.

Finite difference methods (FDM) offer the most flexibility in representing thermal component models parameterized in terms of structural and material properties that faithfully can represent chip to chip thermal coupling. The results are compact thermal models that can be used as building blocks for any multichip module configuration without requiring additional modeling synthesis steps involving thermal transients or 3-D FEM models like the thermal model proposed in [37]. It is often referenced in literature that FDM methods require too much computing time and cannot coexist with an electrical simulation making dynamic electro-thermal models impossible. A recent method where increased computation time of an FDM-based model was desired was proposed in [38]. A set of N first-order finite difference equations describing the heat equation was converted to a set of M equations, where M<<N. This is done by applying a generalized minimized residual (GMRES) algorithm where the reduced number of equations can be represented by equivalent M Foster cells. The application of the GMRES algorithm is another synthesis step, however, and may not be easily included in a compact thermal model.

This dissertation considers FDM models to be directly coupled into the electrical model. The FDM models are validated against measured data resulting from a newly developed high-speed double chip temperature-sensitive parameter (TSP) transient measurement. By using the device threshold voltage as a time-dependent TSP, the thermal transient of a single device, along with the thermal coupling effect among nearby devices sharing common (DBC) substrates, can be studied under a variety of pulsed power conditions. This technique allows hardware model validation under short-term high-power dissipation levels to be captured along with the thermal time constants resulting from the chip to chip coupling over longer term power dissipations without the use of thermal couples.

What once used to be a major obstacle for trying to implement a FDM model, multi-core processing and cluster networks now allow fairly accurate FDM networks with dense meshes to be run within the electrical simulator. This dissertation will consider the first FDM based thermal component model for optimization using electro-thermal simulation.

2.3 Electro-thermal Simulations

Using electro-thermal models to predict junction temperature within an inverter has been extensive in research. Typically the device junction temperature is only predicted within an inverter line cycle and not within the higher frequency switching interval of the electrical device. There are many methods for running electro-thermal system simulations. Average power loss based simulations as suggested by the authors of [4] predict junction temperature within an inverter line cycle. Average power dissipated by the device is determined ahead of time and used with a corresponding thermal model. This method cannot predict instantaneous power dissipation which is required for parametric evaluation for design optimization.

Instantaneous power loss based simulations which consider both the small time steps (<1us) required by the electrical switching devices and the longer time steps needed for thermal transient (>100ms) are proposed in [39] and [40]. Iterative approaches are required for arriving to a thermal steady state. These methods are not practical for running multiple simulations for parametric evaluation. The major problem is simulation speed. If only considering short term high dissipated power effects like short circuit condition [41] and [42], instantaneous power loss based simulation is the only method available. However in these cases the long thermal time constants were not required. So depending on what the goal of the electro-thermal simulation is going to be used for will also determine the time scale resolution of the models.

In [41], a method for achieving faster simulation times using a fast memory less convolution algorithm is proposed for electro-thermal analysis with Foster networks. However this method is not easily extended to more complicated switching circuits such as the soft switching inverter.

As it pertains to aiding as a design tool, there is a bit of literature that uses electro-thermal simulation to aid in design of power electronic circuits. In [43] the authors use electro-thermal simulations to determine the cooling requirements for a traction motor in a hybrid vehicle. System cooling was adjusted subject to the constraint of junction temperatures below 115 °C ensuring sufficient device reliability. This was achieved through variation and study of the switching frequency only and access to device parameters were not available for parametric evaluation.

The author in [44] used electro-thermal based simulation to optimize the printed circuit board layout of a hard switching boost converter, however device parameters were not available for parametric evaluation.

The design of a two-coupled magnetic non hybrid soft-switching inverter for a photovoltaic was presented in [45]. Due to the power level however, only MOSFETs were considered for the main devices. Design optimization of this particular design only considered conduction loss since the turn-on and turn-off losses could be neglected. Calculations were all that were necessary and electro-thermal simulation was not required.

Using compact electro-thermal models, the authors in [46] performed a parametric study on a hybrid silicon IGBT and silicon carbide JBS diode hard switching power module. The chip areas of the IGBT and diode along with switching frequency and gate drive resistance allowed for a parametric trade-off to achieve an optimized design of the half-bridge module. Soft-switching or

external circuit elements were not considered and optimization is based on the traditional hard switching application.

This dissertation extends this study to a soft switching application where chip areas are used to minimize total device loss of a hybrid switch operating under soft switching condition. In addition, gate drive timing effects under soft switching operation are used to further minimize the total device loss as suggested in [47].

2.4 Multi-Scale Electro-thermal approach

Historically simulating the electrical and thermal characteristics of power electronics circuits in the same simulation has resulted in major challenges with regards to simulation speed and convergence. The reason is because the electrical characteristics of power electronics circuits require very small time constants (<1us) to capture the switching behavior of the circuit while the thermal time constant typically require very long time constants (>1s) to reach thermal steady state. The end result is a simulation running with microsecond time steps for several seconds in simulation time resulting in hours to days of actual elapsed real time. This presents a significant challenge if electro-thermal simulation is to be used to parametrically evaluate multiple design variables with multiple design constraints for design optimization. A decoupling of the thermal and electrical model during the parametric evaluation is necessary without losing the thermal effects of the temperature dependent electrical parameters. To achieve this, a “multi-scale” approach is required.

A multi-scale approach refers to combing different type of analysis and or analysis with different time scales together. However a “multi-scale” approach can mean many different things depending on the application.

For example the authors have considered “multi-scale” simulation approaches for simulating power electronic circuits in [48]. A computational homogenization approach was used to derive the effective material properties for the complex heterogeneous interconnect stack of a power electronic device such as a state of the art trench MOSFET. A quasi-1D thermal problem is imposed by assigning the appropriate boundary conditions to a “unit” cell. By imposing a 1D thermal problem, the results of a steady state static 3D FEM analysis can be used with Fourier’s conduction law to extract the effective thermal conductivity. Following the determination of the thermal conductivities from a static thermal analysis, a thermal transient analysis is then performed in an iterative fashion to extract the specific heat capacity through curve fit to a thermal transient response. The “multi-scale” approach used separated the static and transient analysis in order to arrive at the effective material properties within the device. This could be useful in this work as a means to extract the material properties of the DBC, but is not the same “multi-scale” approach suggested in this dissertation for design optimization.

The average power loss based simulations mentioned earlier, as suggested by the authors of [4] and [49], decouples the instantaneous power from the thermal model by averaging the instantaneous power over a switching cycle. This technique is a “multi-scale” approach in that the instantaneous power from a separate analysis with a small time scale is averaged and used with a thermal simulation model with a much larger simulation time step. However the average dissipated loss is obtained from using datasheet and lookup table methods as described earlier. In this manner, there is no method for reproducing the instantaneous junction temperature within a switching cycle. Since this dissertation uses electrical models capable of calculating instantaneous power, full electro-thermal simulations can be performed using the results from average power based simulations as initial conditions such that the time to achieve thermal

steady state using the small time step required by the electrical switching circuits (<1us) is very reasonable (only 1 inverter line cycle). Running the full electro-thermal simulation is important because the switching effects can be studied in greater detail. Instantaneous turn-on and turn-off power can be very high during a switching edge (>10kW), especially if hard switching, resulting in potentially dangerous instantaneous junction temperature rises at the very top of the device. It is important to verify the design performance and, if necessary, revisit the design optimization procedure again and redefine design constraints accordingly.

The authors in [40] and [50] use a multi-scale approach to run the electrical simulation separately from a 3D thermal FEM simulation tool. The authors of [50] even consider parallel computing of multiple computer processors to evaluate the FEM results to reduce computation time. However this approach would not work for the design optimization. The optimized result of the parametric evaluation in this dissertation becomes part of a full electro-thermal simulation where instantaneous junction temperature can be evaluated. It is not possible to couple the 3D FEM analysis tool into the electrical simulation where the instantaneous power dissipation is a dynamic heat flux. While the 3D FEM analysis tool could be used during the design optimization for determine the cooling coefficient, the tool is not capable of evaluating a full electro-thermal simulation where the appropriate initial conditions can be used to achieve thermal steady state. The authors in [51] also separate the electrical and thermal simulation using a multi scale approach but use FDM models with the discrete mesh generated from separate mesh generation tools. The mesh generation tool was necessary to deal with the complicated geometric structure. This would not be easily extended into the building block approach proposed in this dissertation. The geometric structures of power electronics modules considered in this dissertation typically are more symmetric and can be realized using rectangular based finite differences. However if a

more complicated geometry was necessary to describe, using a mesh generation tool is certainly reasonable but will result in a longer design optimization time.

The multi-scale approach proposed in this dissertation uses instantaneous power based simulations for determination of the design variables that result in the minimized total device loss subject to the defined design constraints. Next, average power based simulations are used to determine the cooling convection coefficients to keep the junction temperatures at the defined levels assumed during the design optimization. Finally, a full electro-thermal simulation, using initial conditions from the average power based simulation, is run to evaluate and check the design performance, especially the instantaneous junction temperatures of the device.

Chapter 3 The Application

3.1 Inverter Circuit

Fig. 3-1 shows a couple-magnetic type soft-switching inverter circuit adopting a hybrid switch. The hybrid switch is comprised of a MOSFET in parallel with an IGBT. The concept of the hybrid switch in a soft-switching inverter is to have the MOSFET act as the main switch and the IGBT to conduct the higher currents within the inverter cycle. The idea is the lower current range of the inverter line cycle conducts mostly through the MOSFET since the *Rdson* times the current is small compared to the constant voltage across the IGBT. However, at the higher currents within the inverter line cycle the IGBT maintains a constant voltage drop and is smaller than the voltage drop resulting from a higher current times the R_{dson} of the MOSFET [3].

The purpose of the coupled-magnetic is to facilitate the soft-switching action through the auxiliary switch by storing energy in the leakage inductance of the transformer which resonates with the capacitance across the main switch, aligning the hybrid switch with zero volts prior to turn-on resulting in zero voltage switching (ZVS). A two-coupled magnetic approach is adopted to solve the magnetizing current reset problem [1]. The turns ratio, n, is chosen to achieve enough energy in the leakage inductance to achieve ZVS over the entire load range.

A variable timing scheme is adopted to turn-on the hybrid switch at the moment the voltage across the switch is detected to be zero [2]. This variable time delay is the delay between the auxiliary switch turning on and the main hybrid switch. The timing is variable because the amount of time for the voltage to reach zero is dependent on the load current and resonant inductance. The turn-on switch loss is eliminated with this technique, thereby drastically

decreasing the overall switch loss resulting in increased module efficiency and minimizing EMI within the system.

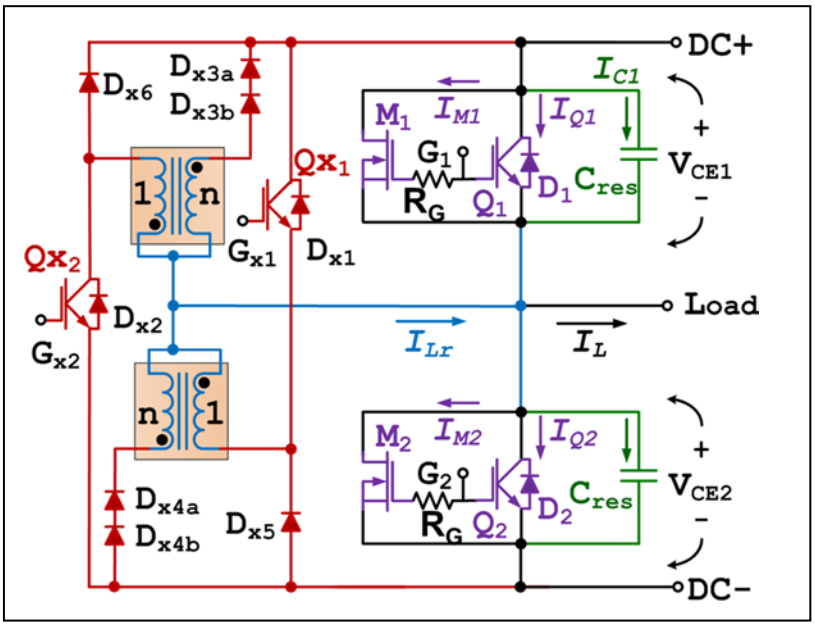

Fig. 3-1 Phase leg of the coupled-magnetic type soft-switching inverter

Referring to Fig. 3-1, each module contains the main switching elements of the inverter circuit made up of IGBTs Q_1 and Q_2 operated in parallel with MOSFETs M_1 and M_2 respectively. Free-wheeling diodes for the main switching elements are also included and designated D_1 and D_2. In addition, to the main switching elements, auxiliary IGBTs Q_{x1} and Q_{x2} and auxiliary diodes D_{x3} and D_{x4} are also included in each module.

3.2 Packaging

Each module utilizes DBC technology where copper is directly bonded to a ceramic substrate such as ALN. The thermal analysis in this paper focuses on two chips exhibiting strong thermal coupling due to their proximity to each other and different power distributions. The different power distributions are a result of the different circuit function each chip performs in the inverter circuit. The power distribution of M_1 and Q_1 exhibit the traditional inverter switch loss minus the

turn-on loss due to ZVS condition. The power distribution of G_{x1} is much different and has a very large peak power for a short duration to charge the resonant element used for enabling ZVS of the main switch. The chips that are the focus of the thermal model development in this dissertation are the auxiliary IGBT G_{x1} and main switching MOSFET M_1 in Fig. 3-1. Both chips share a common DBC and are relatively close together shown in Fig. 3-2 outlined in the dotted dashed line.

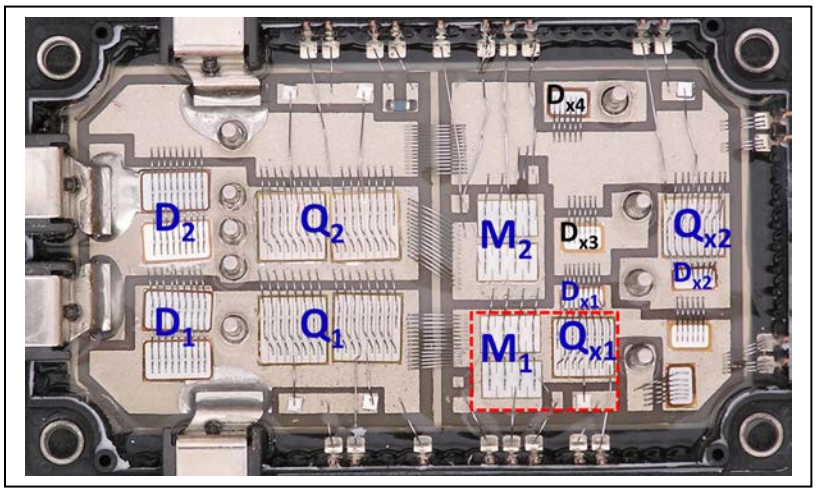

Fig. 3-2 Module components of soft-switching module.

It is desired to have a compact thermal model parameterized in terms of structural and material properties. Table 3-1shows the material information for each layer of the DBC.

Table 3-1 Thermal Model Device Parameters

Material Units	Thermal Conductivity (W/(cm-K))	Density (g/cm^3)	Specific Heat (J/g-K)	Thickness (cm)
Silicon	1.56	2.33	0.71	0.0275
AlN	2.17	3.24	1.05	0.0635
Copper	4.01	8.98	0.39	0.0305
Solder	0.57	8.17	0.16	0.162

The DBC materials and associated material thicknesses and dimensions for the two chips G_{x1} and M_1 are shown in Fig. 3-3. The individual power distribution for each chip is assumed evenly distributed at the top of each chip, but the two chips do not have the same power distribution.

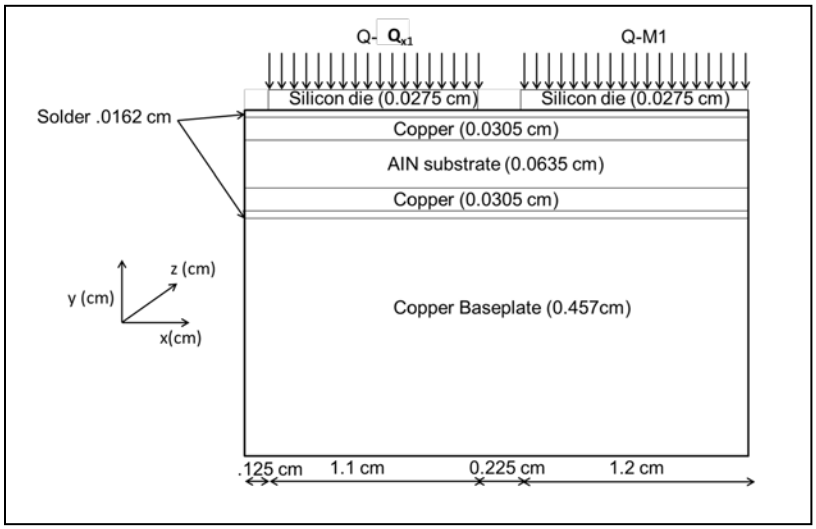

Fig. 3-3 DBC stack up of soft-switching module.

3.3 Electro-Thermal Model Development

Each semiconductor device within the circuit should have a suitable electro-thermal model with parameters that have been extracted over temperature. The process for electro-thermal device model development is summarized in the following flow chart:

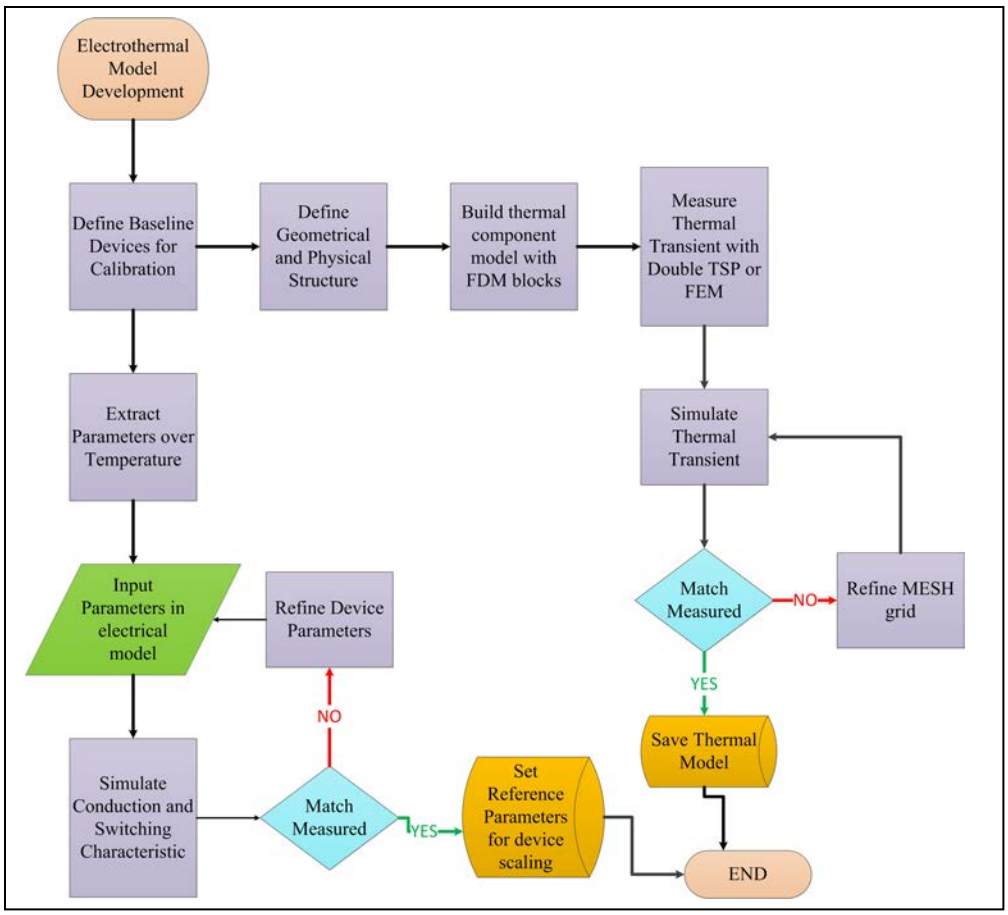

Fig. 3-4 Electro-Thermal Model Development Flow Chart

The electro-thermal model development begins by defining a set of baseline devices where the parameters can be extracted over temperature and used as a reference point for scaling during the design optimization process. Device parameters extracted over temperature are used as inputs into the electrical device models for model validation. Model parameters are refined until device validation is achieved by comparing the measured switching and conduction characteristics of the device with the model prediction.

At the same time thermal component models parameterized in terms of structural and material information are developed using a grid of finite difference equations. The density of the grid is referred to as the mesh. A thermal transient is measured using actual baseline devices using the

double TSP method (to be described in Chapter 4) or from a 3D FEM analysis of the device structure. The mesh grid is refined until validation is achieved by comparing the measured thermal transient from double TSP or 3D FEM of the device with the model prediction.

Chapter 4 Thermal Model

4.1 Fourier's Law 1D Heat Conduction

Fourier's law is used to quantify conductive heat flow. It states that the rate of heat flow equals the product of the area normal to the heat flow path, the temperature gradient along the path, and the thermal conductivity of the medium [52]. In one dimension: and referring to Fig. 4-1.

$$Q_k = -kA_k \left.\frac{\partial T}{\partial z}\right|_z \tag{4.1}$$

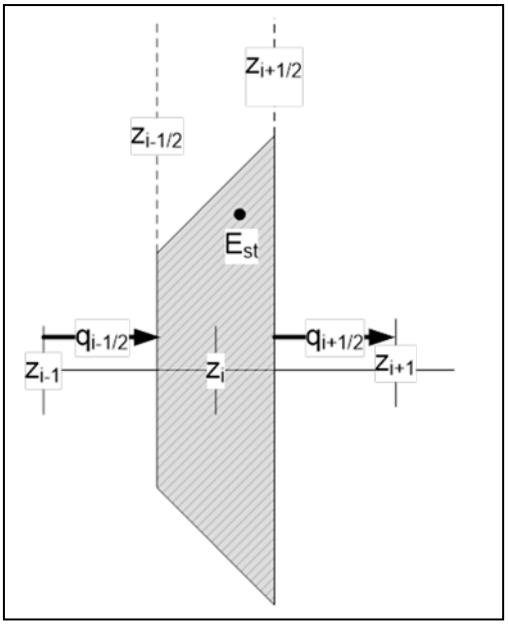

Fig. 4-1 Fourier's Law in One Dimension

Where:

Q_k = heat transferred (watts)

A_k = cross-sectional area of heat flow path, cm^2

$\frac{\partial T}{\partial z}$ = temperature gradient, K/cm

k = thermal conductivity , watts/K•cm

The energy balance method is used to develop finite difference equations to the element of volume:

$$\dot{E}_{in} - \dot{E}_{out} = \dot{E}_{stored} \tag{4.2}$$

The energy in and out of the element of volume is given by Fourier's law:

$$\dot{E}_{in} = q_{i-1/2} = -k_{i-1/2}\left(\frac{A_i + A_{i-1}}{2}\right)\left.\frac{\partial T}{\partial y}\right|_{i-1/2} \tag{4.3}$$

$$\dot{E}_{out} = q_{i+1/2} = -k_{i+1/2}\left(\frac{A_{i+1} + A_i}{2}\right)\left.\frac{\partial T}{\partial y}\right|_{i+1/2} \tag{4.4}$$

The rate at which energy in the element volume is stored is given as:

$$\dot{E}_{st} = \rho_i c_i \underbrace{A_i\left(z_{i+1/2} - z_{i-1/2}\right)}_{volume}\frac{\partial T_i}{\partial t} \tag{4.5}$$

Where:

ρ_i = thermal density (g/cm^3)
c_i = specific heat (J/g/K)

Substituting(4.3),(4.4), and (4.5) into (4.2)

$$\left(-k_{i-1/2}\left(\frac{A_i + A_{i-1}}{2}\right)\left.\frac{\partial T}{\partial y}\right|_{i-1/2}\right) - \left(-k_{i+1/2}\left(\frac{A_{i+1} + A_i}{2}\right)\left.\frac{\partial T}{\partial y}\right|_{i+1/2}\right) = \rho_i c_i A_i\left(z_{i+1/2} - z_{i-1/2}\right)\frac{\partial T_i}{\partial t} \tag{4.6}$$

Using Taylor series, the partial derivatives can be approximated by:

$$\left.\frac{\partial T}{\partial y}\right|_{i-1/2} = \frac{T_i - T_{i-1}}{z_i - z_{i-1}} \tag{4.7}$$

$$\left.\frac{\partial T}{\partial y}\right|_{i+1/2} = \frac{T_{i+1} - T_i}{z_{i+1} - z_i} \tag{4.8}$$

Substituting (4.7) and (4.8) into (4.6)

$$\left(-k_{i-1/2}\left(\frac{A_i + A_{i-1}}{2}\right)\frac{T_i - T_{i-1}}{z_i - z_{i-1}}\right) - \left(-k_{i+1/2}\left(\frac{A_{i+1} + A_i}{2}\right)\frac{T_{i+1} - T_i}{z_{i+1} - z_i}\right) = \rho_i c_i A_i \left(z_{i+1/2} - z_{i-1/2}\right)\frac{\partial T_i}{\partial t} \quad (4.9)$$

Let us define a thermal resistance and capacitance:

$$R_{i-1,i} = \frac{z_i - z_{i-1}}{k_{i-1/2}\left(\frac{A_i + A_{i-1}}{2}\right)} \quad (4.10)$$

$$R_{i,i+1} = \frac{z_{i+1} - z_i}{k_{i+1/2}\left(\frac{A_{i+1} + A_i}{2}\right)} \quad (4.11)$$

$$C_i = \rho_i c_i A_i \left(z_{i+1/2} - z_{i-1/2}\right) \quad (4.12)$$

Substituting(4.10),(4.11), and (4.12)

$$\left(\frac{T_{i+1} - T_i}{R_{i,i+1}}\right) - \left(\frac{T_i - T_{i-1}}{R_{i-1,i}}\right) = C_i \frac{\partial T_i}{\partial t} \quad (4.13)$$

Equation (4.13) can be represented by an equivalent circuit known as the “Cauer” circuit shown in Fig. 4-2. It is noted that only the Cauer cells contain *R* and *C* values with true physical meaning contrary to the “Foster” cells described later in this chapter. This is only true however if the body is considered one dimensional. Cauer cells can still be applied for three dimensional structures but the resulting *R*s and *C*s do not have any physical meaning beyond one dimensional heat conduction.

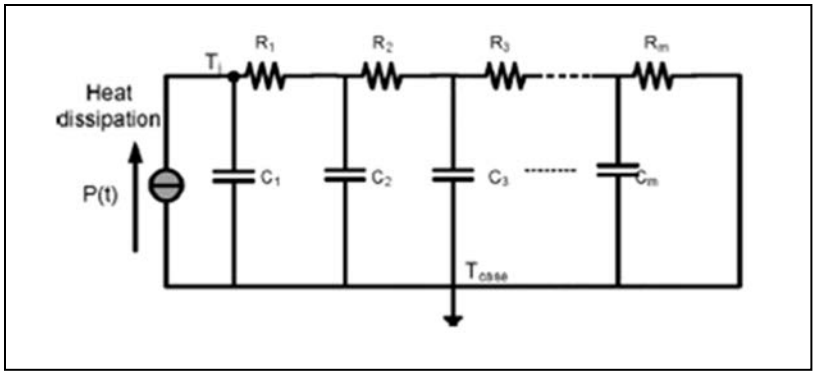

Fig. 4-2 Cauer Circuit Type

In the discretization process of (4.13), it is assumed that the temperature gradient and thermal conductivity do not vary substantially between adjacent grid points. Therefore, the accuracy of the thermal component model is determined by the number and locations of the thermal nodes within the component. For high power dissipation levels during short periods of time (e.g. transients), the silicon chip surface temperature rises faster than the heat diffuses into the chip, and a high density of thermal nodes is required at the silicon chip surface. However, the thermal gradients disperse as the heat diffuses through the chip, so a grid space that increases logarithmically with distance from the heat source (silicon chip surface) results in the minimum number of thermal nodes is required to describe the temperature distribution for the range of applicable power dissipation levels.

4.2 Heat Spreading

By placing a high thermal conductivity material in the heat path, the heat flow in the X and Y horizontal directions is greater than that in the Z or vertical direction. Therefore, the heat will spread with the result of increasing the effective thermal cross sectional area of a relatively poor thermally conducting material. Referring to Fig. 4-3:

$$\alpha = \tan^{-1}\frac{k_1}{k_2}$$

α = spreading angle (degrees)

$k1$ = thermal conductivity of current layer

$k1$ = thermal conductivity of underlying layer

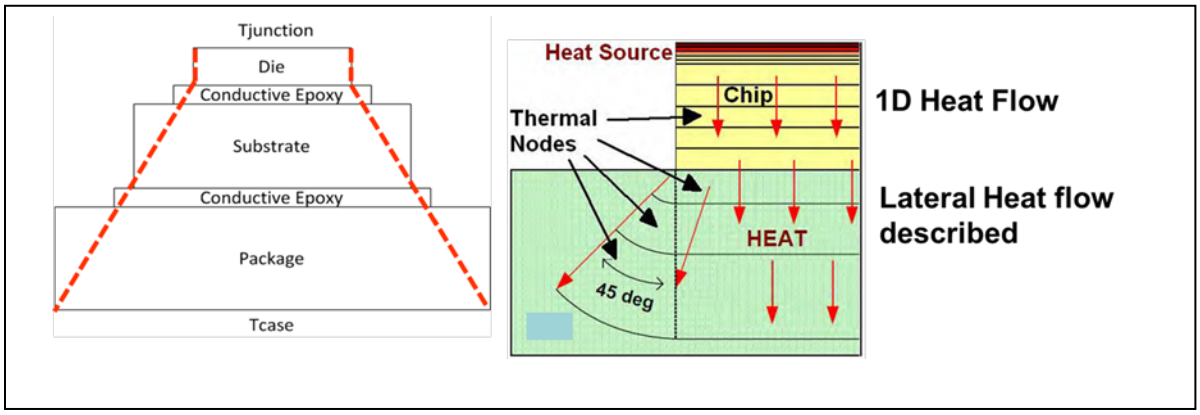

Fig. 4-3 Heat Spreading within a package.

By using Cauer networks, the package shown in Fig. 4-3 can be discretized and mapped into a series of interconnecting Cauer networks as depicted in Fig. 4-4. A thermal network for each material has been created and connected in series. The heat flow area at the bottom of each material is used as the “header” area in the next material. The “header” area can be calculated using the effective heat flow area approach [32] for 1D conduction problems.

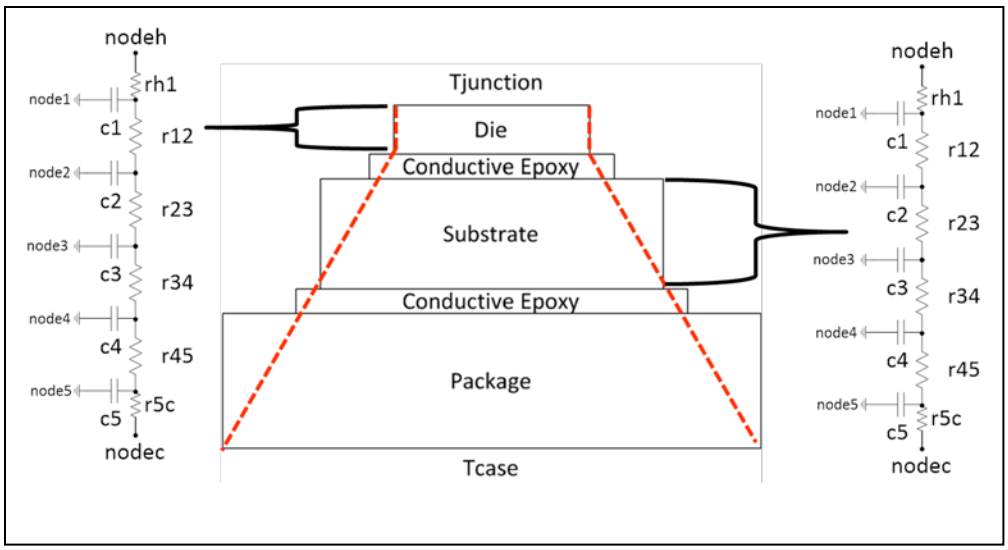

Fig. 4-4 Discretized Cauer Networks

4.3 Effective Heat Flow Area

In order to accurately model the 3 dimensional heat spreading effect within the module using a 1D Cauer circuit, the effective heat flow area approach is used for calculating the required thermal areas used in the thermal resistance and capacitance calculations. The effective heat flow approach describes a heat flow area that increases with depth into the package. This is done by combining the components of heat flow area due to cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip known as the "header" area. For the top of the package the header area is the area of the chip. For subsequent material layers, the header area is the effective heat flow area of the bottom of the previous material. The heat flow area can be visualized by Fig. 4-5:

The components of the heat flow area are calculated as:

$$A_{cylzi} = \frac{\pi}{4} W_{header}(r_{ymzi} + r_{ypzi}) + \frac{\pi}{4} L_{header}(r_{xmzi} + r_{xpzi}) \tag{4.14}$$

$$A_{sphzi} = \frac{\pi}{4}\left((r_{ymzi} + r_{ypzi}) \cdot (r_{xmzi} + r_{xpzi})\right) \tag{4.15}$$

$$A_{rectzi} = A_{header} \tag{4.16}$$

Where the boundary conditions for the heat flow radius in the lateral directions are given as:

$$r_{xpzi} = \begin{cases} z_i & \text{for } z_i \le x_{chedp} \\ x_{chedp} & \text{for } z_i > x_{chedp} \end{cases} \quad \text{etc...} \tag{4.17}$$

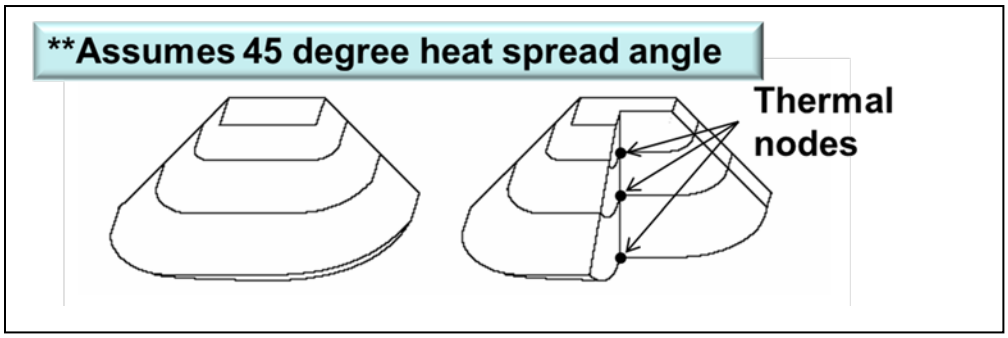

Fig. 4-5 Effective Heat Flow Area

The lateral boundary conditions are depicted in Fig. 4-6.

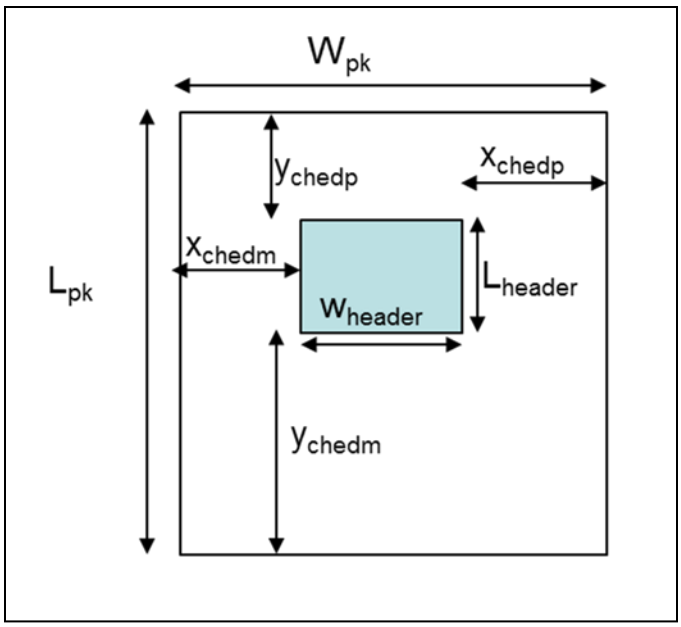

Fig. 4-6 Lateral Boundary Conditions.

The effective heat flow area approach works well for symmetrical thermal problems where the heat spread area can be well characterized and 1D thermal circuits can be used. In packages where the heat flow is not symmetrical or thermal coupling results due to neighboring chips sharing common DBC area, the three dimensional heat equation needs to be considered. Using just Fourier's Law is no longer adequate.

4.4 Foster Network Generation

Another method for capturing the 3D heat spreading using 1D thermal networks is to adopt the "Foster" cell. The author in [22] points out that only the Cauer circuits are suitable for faithfully representing the system from the physical point of view. In the electrical circuit, the current flowing across the capacitor during a dynamic regime is the same on both sides of the device due to the symmetrical variation of the positive and negative electric charges. Thermal circuits have no quantities equivalent to negative electric charge. Only the heat flow on one side of the capacitor has a real meaning, therefore the Cauer networks, with the capacitors grounded on one side, are more suitable as a thermal analogy. A foster cell no longer represents the layer sequence meaning you cannot access internal temperatures of the material sequence. The network nodes do not have any physical significance. "A foster network is only shows a behavior characteristic of the system, and does not correlate directly with the physical parameters of the package materials and geometry. Furthermore, this topology does not correspond to physical reality where heat flow (and corresponding temperature rise) to the device case (copper layer) is delayed due to the inherent heat capacity and thermal resistance of various layers away from the die" [18]. A foster cell can be transformed back into a Cauer cell through transformation methods [53] but will not gain physical reality in doing so.

A Foster cell is usually obtained from a thermal transient measurement or 3D FEM simulation and consists of an *R* and *C* in parallel as opposed to the Cauer circuit where the *R* and *C* are in series. Fig. 4-7 shows a foster cell:

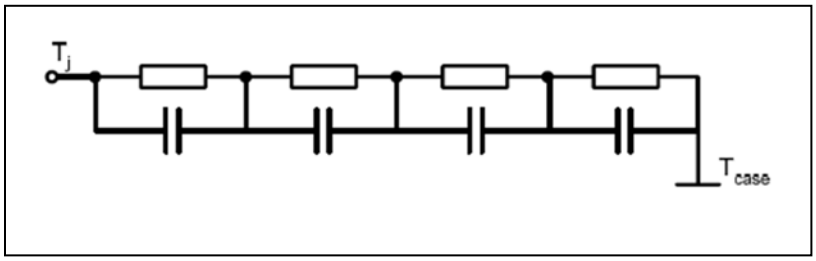

Fig. 4-7 Foster Network.

The following equation shows the equivalent model used to fit a foster network to a thermal transient measurement.

$$Z_{thjc}(t) = \sum_{i=1}^{n} r_i \times \left(1 - e^{\frac{-t}{\tau_i}}\right) \tag{4.18}$$

Where:

$\tau_i = r_i * c_i$ Given in datasheet as pair

The junction temperature can be now calculated from:

$$T_j(t) = P(t) * Z_{thjc}(t) + T_{case}(t) \tag{4.19}$$

A typical thermal transient measurement given by a device datasheet is shown in Fig. 4-8:

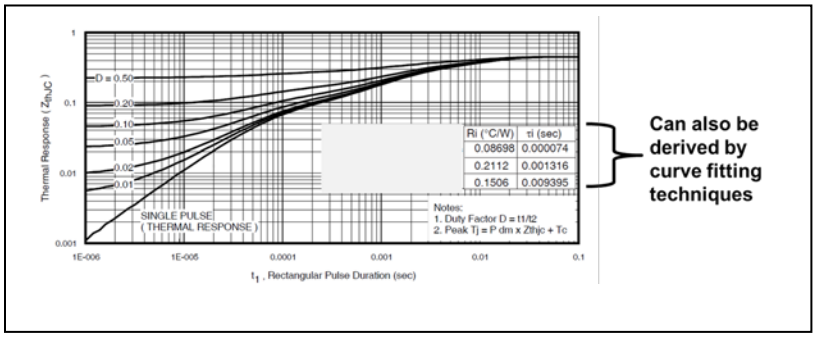

Fig. 4-8 Transient Thermal Impedance.

For 3D and lateral thermal coupling consideration, additional foster cells can be added to account for the heat generated through coupling from adjacent chips sharing a common DBC stack up. A thermal interference matrix approach is suggested in [26] for describing packages with multiple heat sources. Fig. 4-9 shows the package considered in [26].

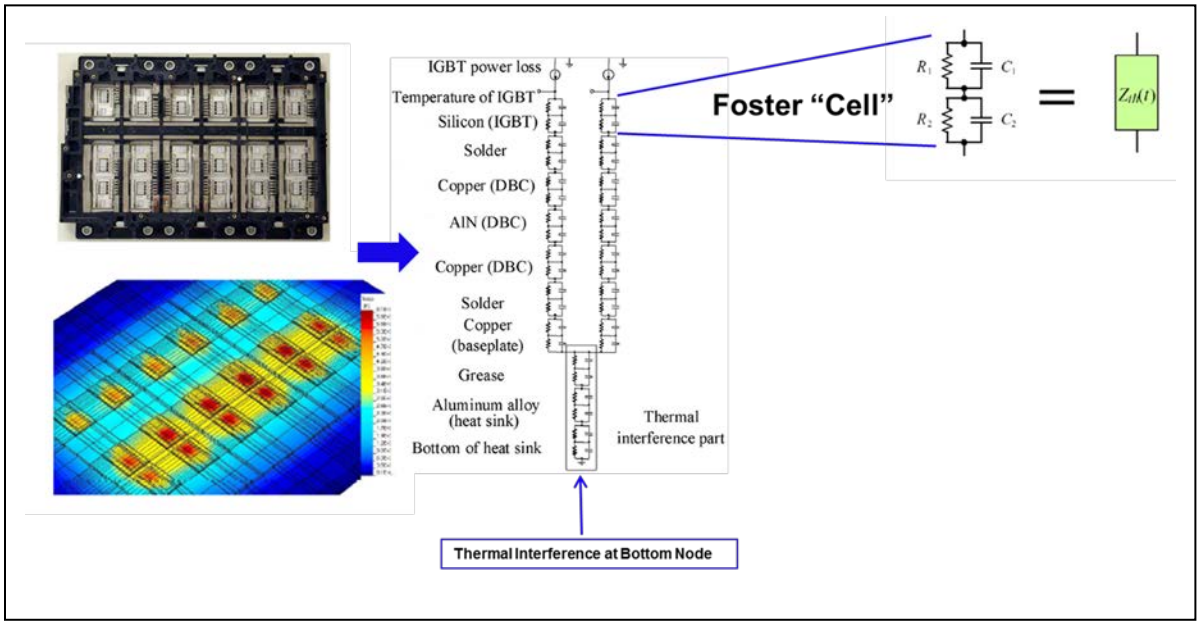

Fig. 4-9 Foster Network Generation for multi heat source package [26].

The "thermal interference" cells are placed at the bottom of the foster latter networks generated for each heat source within the module. A thermal impedance matrix is used to represent the thermal interferences among the many chips inside the module and is shown below.

$$\begin{bmatrix} T_1 \\ T_2 \\ \bullet \\ T_j \\ \bullet \\ T_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \bullet & Z_{1j} & \bullet & Z_{1n} \\ Z_{21} & Z_{22} & \bullet & Z_{2j} & \bullet & Z_{2n} \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ Z_{i1} & Z_{i2} & \bullet & Z_{ij} & \bullet & Z_{in} \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ Z_{n1} & Z_{n2} & \bullet & Z_{nj} & \bullet & Z_{nn} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \bullet \\ P_i \\ \bullet \\ P_n \end{bmatrix} \tag{4.20}$$

In (4.20), P_i is the loss generated by the *i*th chip and T_j is the temperature rise of the *j*th Si chip. T_j is related to P_i by the thermal impedance matrix element Z_j which means the thermal interference between the *i*th chip and the *j*th chip. The diagonal element in the thermal impedance matrix, for example Z_{ii}, means self-heating of the *i*th chip [26].

4.5 3D Heat Conduction

Referring to Fig. 3-3, the heat is assumed to be generated on top of the silicon chip and conducted through the different layers. This is a multilayer, multidimensional heat conduction problem. The resulting 3-D transient heat diffusion equation, assuming no internal heat generation, at a particular layer *i* in Cartesian coordinates is shown as follows:

$$\begin{aligned}&\frac{\partial}{\partial x}\left(k_i\frac{\partial T_i(x,y,z,t)}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_i\frac{\partial T_i(x,y,z,t)}{\partial y}\right)\\&+\frac{\partial}{\partial z}\left(k_i\frac{\partial T_i(x,y,z,t)}{\partial z}\right)=\rho_i c_i\frac{\partial T_i(x,y,z,t)}{\partial t},i=1...m\end{aligned}\tag{4.21}$$

In (4.21), ρ_i is the thermal density, c_i the specific heat of the material, respectively, and m represents the number of layers. It is often possible to simplify (4.21) if the thermal conductivity k_i of the material is constant. However, in silicon, the thermal conductivity is nonlinear and is modeled by [32].

$$k_i(T_i(\mathrm{x},\mathrm{y},\mathrm{z},\mathrm{t}))=1.5486\left(\frac{300}{T_i(x,y,z,t)}\right)^{4/3}\tag{4.22}$$

To solve (4.22) for the module considered in this paper, certain boundary conditions are required. A constant surface temperature is maintained at bottom of the module resulting in a Dirichlet boundary condition as shown:

$$T_m(x,y,z,t)\big|_{y=y_{m+1}}=T_A\tag{4.23}$$

The top layer of the module corresponds to the heat flux (Watt per square centimeter) generated from the power distribution of each chip where all the heat is assumed to flow into the top boundary of the silicon chip resulting in a Neuman condition shown as follows:

$$-k_1 \left.\frac{\partial T_1(x,y,z,t)}{\partial y}\right|_{y=y_1=0} = q''(t) \tag{4.24}$$

The sides of the module and in the areas with no heat flux generated on the top of the module, adiabatic boundary conditions exist and result in a special case of the Neuman condition as follows:

$$\left.\frac{\partial T_1(x,y,z,t)}{\partial y}\right|_{y=y_1=0} = 0 \tag{4.25}$$

Finally, if perfect thermal contacts exists between layers of different materials

$$T_i(x,y_{i+1},z,t) = T_{i+1}(x,y_{i+1},z,t) \tag{4.26}$$

and

$$k_i \left.\frac{\partial T_i(x,y,z,t)}{\partial y}\right|_{y=y_{i+1}} = k_{i+1} \left.\frac{\partial T_{i+1}(x,y,z,t)}{\partial y}\right|_{y=y_{i+1}} \tag{4.27}$$

4.6 3D FDM Thermal Model

The finite difference form of the heat equation in (4.21) is used to solve the corresponding 3-D temperature distributions within the multichip module shown in Fig. 3-2. The finite difference equations are derived using the energy balance method described in [54]. This approach enables one to analyze many different phenomena such as problems involving multiple layers and exposed surfaces that do not align with an axis of the coordinate system. The finite difference equation for a node is obtained by applying conservation of energy using simplified forms of

Fourier's law to a control volume about the nodal region. Therefore, the entire volume of the package is discretized into a finite number of nodes. The number of nodes in the y-direction is *sizey*, the number of nodes in the x-direction is *sizex* and the number of nodes in the z-direction is *sizez*. A variable grid size is used for determining the number of nodes and results in an optimized computation time. A finite difference equation using the conservation of energy is written to a control volume about an interior node *T(i,j,k)* in (4.28) where *i* = 1:*sizey*, *j* = 1:*sizex* and k = 1:*sizez*. The implicit form of a finite difference equation is used to approximate the time derivative, while evaluating all other temperatures at the new (p +1) time, instead of the previous (p) time. Relative to the explicit method, the implicit formulation has the advantage of being unconditionally stable [54]. The corresponding control volume and associated dimensions are shown in Fig. 4-10.

$$\begin{aligned} &k_{avg}A_{yz}\frac{\left(T_{i,j+1,k}^{p+1}-T_{i,j,k}^{p+1}\right)}{d_{xR}}+k_{i-1}A_{xz}\frac{\left(T_{i-1,j,k}^{p+1}-T_{i,j,k}^{p+1}\right)}{d_{yB}}+\\ &k_{avg}A_{yz}\frac{\left(T_{i,j-1,k}^{p+1}-T_{i,j,k}^{p+1}\right)}{d_{xL}}+k_{i+1}A_{xz}h_{ci}\frac{\left(T_{i+1,j,k}^{p+1}-T_{i,j,k}^{p+1}\right)}{h_{ci}d_{yT}+k_{i+1}}b_c\\ &+k_{avg}A_{xy}\frac{\left(T_{i,j,k+1}^{p+1}-T_{i,j,k}^{p+1}\right)}{d_{zF}}+k_{avg}A_{xy}\frac{\left(T_{i,j,k-1}^{p+1}-T_{i,j,k}^{p+1}\right)}{d_{zB}}=E_{xyz}\frac{T_{i,j,k}^{p+1}-T^{p}{}_{i,j,k}}{\Delta t}+q''A_{xz}(b_c-1)\end{aligned} \tag{4.28}$$

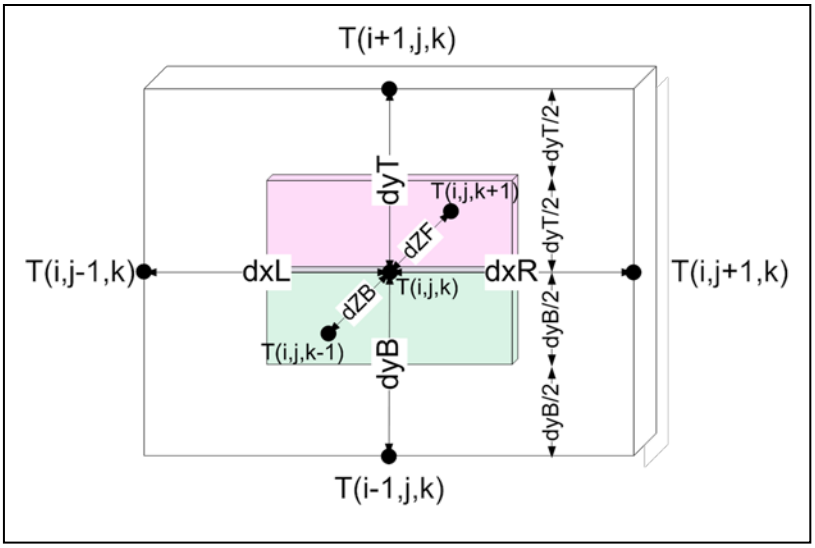

Fig. 4-10 Interior control volume at a material interface.

In (8), b_c = 1 for interior nodes and b_c = 0 for the top of the silicon chips where a heat flux q'' is present. For this model, the heat flux is determined simultaneously by the electrical simulator representing the instantaneous dissipated power of a particular device and is an input port to the model. The areas A_{yz} , A_{xz} , and A_{xy} represent the cross-sectional areas of the control volume.

$$A_{yz} = \left(\frac{d_{yT} + d_{yB}}{2}\right)\left(\frac{d_{zB} + d_{zF}}{2}\right), A_{xz} = \left(\frac{d_{xL} + d_{xR}}{2}\right)\left(\frac{d_{zB} + d_{zF}}{2}\right), \\ A_{xy} = \left(\frac{d_{xL} + d_{xR}}{2}\right)\left(\frac{d_{yT} + d_{yB}}{2}\right) \tag{4.29}$$

The stored energy E_{xyz} within the control volume is given as

$$E_{xyz} = \frac{1}{8}\left(d_{zF} + d_{zB}\right)\left(d_{xL} + d_{xR}\right)\left(\rho_{i-1}c_{i-1}d_{yB} + \rho_{i+1}c_{i+1}d_{yT}\right) \tag{4.30}$$

The average thermal conductivity taking into account the average thermal conductivity at material interfaces is given by

$$k_{avg} = \frac{d_{yB}k_{i-1} + d_{yT}k_{i+1}}{d_{yT} + d_{yB}} \tag{4.31}$$

As mentioned earlier, contact resistance represents the imperfect thermal contact between materials. The existence of a finite contact resistance is due to surface roughness effects between materials resulting in a temperature drop across the interface. In high-power applications, this drop is not negligible and can result in significant temperature rise and should be accounted for in the thermal model. The contact resistance is included in (4.28) by including the thermal contact conductance coefficient h_{ci} .This coefficient is a function of the two interface materials and the medium between the materials (i.e. air or thermal grease, etc.). The model in this paper included thermal contact resistance between the DBC and the module baseplate. In addition, thermal resistance was included between the module and the temperature-controlled heat sink.

To determine the unknown nodal temperatures at $t+\Delta t$, the corresponding nodes must be solved simultaneously at each time step. The nodal equations in this paper were implemented in MATLAB, and the matrix inversion technique was used to solve the corresponding nodal equations at each time step. In this manner, materials with nonlinear thermal conductivities such as silicon given by (4.22) can be updated at each time step.

4.7 2-D Discrete Fourier Series Model

A discretized, 2-D temperature field was used to model (1), since it lends itself to a straightforward, approximate specification of an arbitrary, dynamic heat flux at the upper surface boundary. The temperature grid was $N \times N$, N odd, with a sufficiently high grid resolution to reduce approximation error. In this particular application, a square wave function was used to model the applied surface heat flux distribution. It was modeled using a discrete Fourier series (DFS). Due to the extremely fine grid resolution used in the validation modeling, all discrete

derivatives were approximated using continuous derivatives. Fig. 4-11 illustrates the geometry that was used in the development of the 2-D, six-layer validation model.

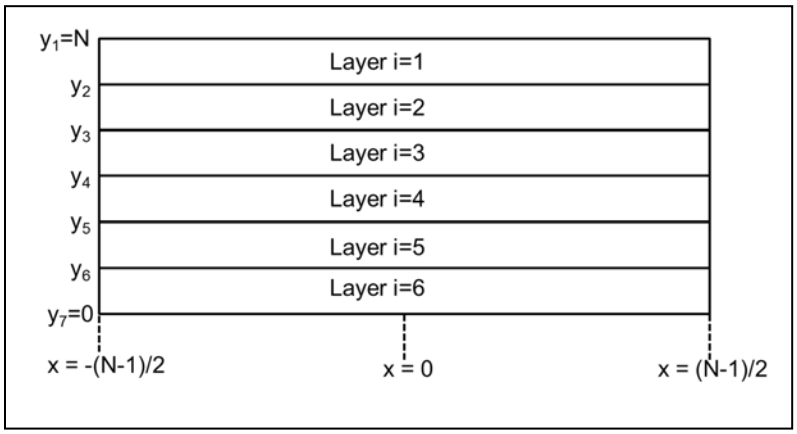

Fig. 4-11 2-D, 6 six-layer validation model.

The total solution to (4.21) was sought that contained both a transient T_{rr} and a steady-state T_{ss} solution, i.e.

$$T\left(x_m, y_n, t\right) = T_{TR}\left(x_m, y_n, t\right) + T_{SS}\left(x_m, y_n\right) \tag{4.32}$$

A 2-D, DFS form of the transient solution can be written as

$$T_{TR}\left(x_m, y_n, t\right) = \sum_{\mathrm{jk}} C_{\mathrm{jk}} \cdot \sin\left(\lambda_j \cdot y_n\right) \cdot \cos\left(\lambda_k \cdot x_m\right) \cdot e^{-\kappa \cdot \lambda_{\mathrm{jk}}^2 \cdot t} \tag{4.33}$$

Where $\lambda_{j\,\mathrm{k}}^2 = \lambda_j^2 + \lambda_{\mathrm{k}}^2$ and the individual eigenvalues satisfy the applied homogenous boundary conditions, i.e., zero heat flux at the upper and lateral sides of the chip, and zero temperature at the base of the chip. The DFS coefficient C_{jk} satisfies the initial boundary condition for the transient solution at time t = 0.

A 2-D, DFS form of the steady state solution for a certain layer *(i)* can be written as

$i = 1$:

$$T_{SS,1}(x_m, y_n) = \tfrac{1}{2} \cdot (a_{1\,0} \cdot y_n + b_{1\,0}) + \sum_{j=1}^{\frac{N-1}{2}} \begin{pmatrix} a_{1\,j} \cdot \sinh\left(j \cdot 2\pi \cdot \left(y_n - y_1\right) / N \right) + \\ b_{1\,j} \cdot \cosh\left(j \cdot 2\pi \cdot \left(y_n - y_1\right) / N \right) \end{pmatrix} \cdot \cos\left(j \cdot 2\pi / N \cdot x_m \right) \quad (4.34)$$

$i > 1$:

$$T_{SS,i}(x_m, y_n) = \tfrac{1}{2} \cdot (a_{i\,0} \cdot y_n + b_{i\,o}) + \sum_{j=1}^{\frac{N-1}{2}} \begin{pmatrix} a_{i\,j} \cdot \sinh\left(j \cdot 2\pi \cdot \left(y_n - y_{i+1}\right) / N \right) + \\ b_{i\,j} \cdot \cosh\left(j \cdot 2\pi \cdot \left(y_n - y_{i+1}\right) / N \right) \end{pmatrix} \cdot \cos\left(j \cdot 2\pi / N \cdot x_m \right) \quad (4.35)$$

The DFS coefficients in (4.34) and (4.35) are solved by satisfying the interfacial boundary conditions, i.e., matching heat flux and temperature at each of the layer interfaces; and the surface and bottom boundary conditions, including Fourier's Law of heat conduction and a constant base temperature, respectively. The insulated boundary conditions at $x_m = \left(+(N-1)/2 , -(N-1)/2 \right)$ are satisfied using the $\cos(2\pi j / N \bullet x_m)$ function.

4.8 Model Validation

The DFS model is used for validation of the FDM model under controlled dimensions and boundary conditions for a two chip asymmetrical heating condition. The 3-D FDM model was reduced to 2-D for this validation. This was done by applying the appropriate heat flux boundary condition on the top surface of the module that results in a two dimensional heat conduction problem. Figs. 6 and 7 show a surface temperature versus time plot, and a temperature versus x dimension plot, respectively, at each layer interface. Both Fig. 4-12 and Fig. 4-13 illustrate excellent agreement between both the FDM model and the DFS validation model.

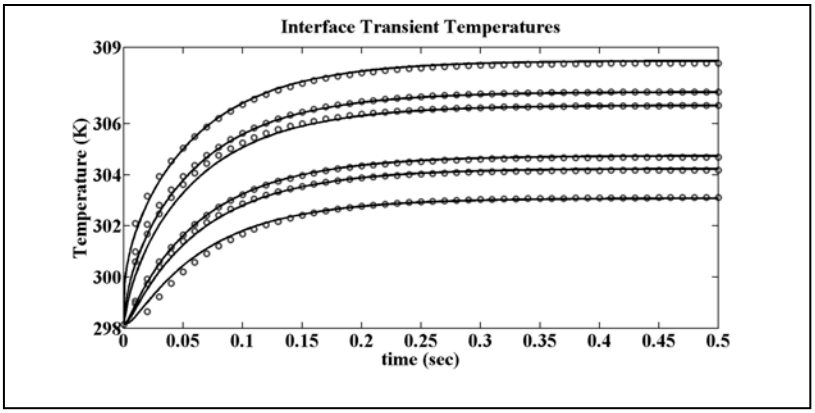

Fig. 4-12 Transient interface temperatures.

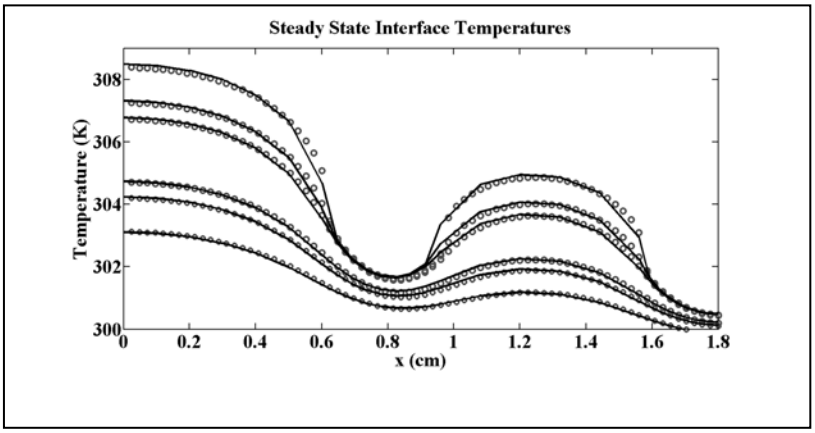

Fig. 4-13 Steady-state interface temperatures versus x dimension.

4.9 Measured and Simulated Results

4.9.1 Test Circuit

For the thermal cross-coupling experiment, an auxiliary IGBT Q_{x1} and a main bridge MOSFET M_1 are chosen due to their close proximity and common DBC layers. M_1 is made up of two chips—MOS1A and MOS1B—and is shown in Fig. 4-14.

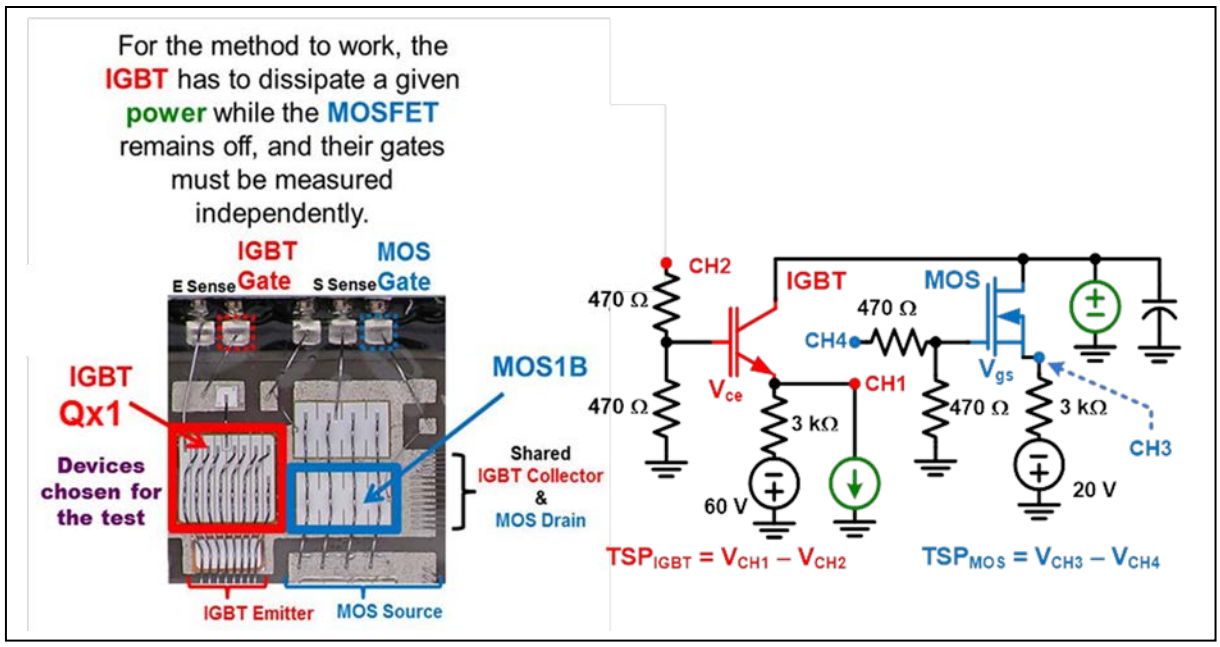

Fig. 4-14 Thermal coupling TSP measurement circuit.

Also, shown in Fig. 4-14 is the test circuit used to measure the transient heating and lateral coupling where the IGBT and MOS under test are the chosen devices Q_{x1} and MOS1B, respectively. Q_{x1} and MOS1B are biased with small auxiliary currents comprised of the 60 and 20 V power supplies along with the 3 kΩ resisters to establish an initial threshold voltage measurement shown as V_{ge} and V_{gs} in Fig. 4-14 and provide the corresponding TSPs for Q_{x1} and MOS1B. The 470 Ω gate resistor serves as a damping resistor to prevent oscillation. The threshold measurements are set up as differential measurements from the data acquisition system because a substantial common mode voltage spike appears on the gate and cathode during switching. This is due to gate charging current interacting with the gate resister used to prevent oscillation. The small bias currents also provides for the capability of using the TSP measurement during the cooling phase. A heavily bypassed voltage power supply is used to maintain a constant voltage across both the Q_{x1} and MOS1B. Q_{x1} is pulsed from the small bias

current to a large current from a custom-made precision current source that features high-speed gating and current control in 0.1 A increments up to 25.5 A [55].

The power dissipation in Q_{x1} due to the large pulsed current and constant device voltage causes the device to heat up causing the TSP of Q_{x1} to change. At the same time, the TSP of MOS1B changes due to the heat source provided by the dissipation in Q_{x1}. The measured temperature rise in MOS1B due to the power dissipation in Q_{x1} allows model validation of lateral thermal heat coupling between chips in close proximity.

4.9.2 Test Procedure

The measurement of the IGBT and MOSFET transient heating requires two parts. First, the TSP of each device must be calibrated at known operating conditions and at a series of known temperatures. Second, with the heat sink at a fixed and known temperature, the IGBT is subjected to a longer transient heating pulse where the IGBT temperature increase will result in the MOSFET temperature increase through thermal coupling within a common DBC. The TSP for the IGBT Q_{x1} is the measured gate to emitter voltage V_{ge} in Fig. 4-14. The TSP for the MOSFET MOS1B is the measured gate to source voltage V_{gs} in Fig. 4-14. Fixed temperatures are achieved by having the DUT mounted on a temperature-controlled heat sink. The same test circuit shown in Fig. 4-14 can be used for the calibration and transient heating measurement; the difference between these is determined by the pulse width.

For the calibration curve, the operating conditions that need to be specified include the collector to emitter voltage and collector current. Using a temperature-controlled baseplate temperature, a very short pulse width is applied to the IGBT to avoid significant chip heating and the TSP of the IGBT and MOSFET are recorded over temperature. The result is shown in Fig. 9 for Q_{x1} and MOS1B.

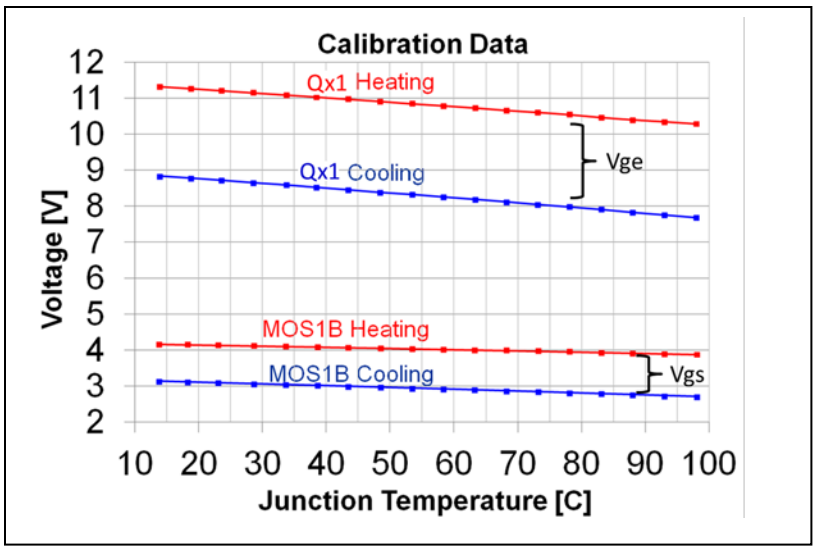

Fig. 4-15 Calibration data double TSP experiment.

The TSP is measured for each device during a heating and cooling phase. The heating phase refers to the TSP that is measured during the pulse duration and the cooling phase refers to the TSP that is measured after the pulse is removed. The result of this calibration curve is an established relationship between chip temperature and the corresponding TSP values of the IGBT and MOSFET.

For the transient heating measurement, the current and voltage conditions are the same as was for the TSP calibration. The temperature of the heat sink is held constant at one temperature for all heating measurements. The current pulse width of Q_{x1} is increased long enough to show significant chip heating of both Q_{x1} and MOS1B. The TSP values for both Q_{x1} and MOS1B are recorded as a function of time, and the voltage waveforms are mapped into temperature as a function of time by using the calibration data. Each IGBT and MOSFET operating condition requires a new calibration. Due to the time consuming process of calibration, a fully automated system has been developed at NIST.

4.9.3 Operating Conditions

Q_{x1} is pulsed with a peak power of 100 W under a variety of pulse width conditions to provide multiple points of validation for both Q_{x1} and MOS1B. The TSP of Q_{x1} and MOS1B are monitored while Q_{x1} is pulsed. The average power applied to the IGBT is varied by using different power pulse widths of constant power amplitude and multiple successive pulses are also used to capture dynamic transient heating of the IGBT and neighboring MOSFET. The pulse repetition frequency is made low enough to capture and study the thermal time constant of the heat propagation from the IGBT to the MOSFET. Much higher speed shorter pulses can be used to capture the resolution required to validate the silicon chip thermal model under a high power short condition.

In [55], the cooling effects had not been measured and only transient heating was studied under very short power duration. The new system with cooling functionality allows successive pulse trains to be generated where the temperature of the device does not return to the heat sink temperature before the next pulse. Therefore, a thermal steady state can be generated and used for further model validation and study of thermal coupling.

4.9.4 Measured Data Versus Model Prediction

The FDM compact model was simulated with the dimensions from Fig. 3-3 and the material properties from Table 3-1. A pulsed heat flux was applied to *Qx1* and the junction temperature of *Qx1* and MOS1B were monitored in the model under the same peak power and duty cycle conditions from the experiment. The module was mounted onto a baseplate constructed of two copper plates with piping and heaters installed in the bottom plate. The two copper plates are joined together by thermal grease and screws. Cold water is run through the piping and the heater is controlled by applying a voltage to the heater. This voltage is the output from a feedback

controller measuring the temperature of a thermal couple located in the bottom baseplate. For our experiment, we chose not to run the heater and applied the highest water pressure possible to bring the baseplate temperature below room temperature. This, however, does not guarantee the entire baseplate is at the same temperature. Therefore, the thermal mass and resistance of the two copper plates were included as an additional layer in the model with a constant temperature assumed at the very bottom.

In addition, contact resistance was added to represent the poor thermal contact at the interface between the two copper baseplates. The thermal contact conductance coefficients were not determined experimentally. Therefore, an assumption on the conductance coefficient is assumed based on a copper to copper interface and then adjusted within reason to achieve the correct offset temperature resulting from the measured data. A copper to copper interface thermal conductance coefficient of 5.5 W/(cm2·K) [28] was applied at the interface of the two copper baseplates and adjusted to 1.2 W/(cm2·K). This implies very poor contact between the two copper to copper interfaces. Future measurements should remove this interface. The module to baseplate coefficient was adjusted from 5.5 to 10 W/(cm2·K), which implies better thermal contact between the module and baseplate.

Fig. 10 shows the measured versus simulated data under a variety of pulse widths of *Qx1*, and Fig. 13 shows the resulting MOS1B temperature resulting from the heating of *Qx1*. There is excellent agreement between the measurement and measured data with the biggest error within a few degrees. Both the heating and cooling portions of the curves show very good agreement thus validating the entire DBC under a variety of conditions. In addition, the thermal coupling temperature and time constant from *Qx1* to MOS1B are captured very nicely with the new model. It should be noted that the measurement points within the model were taken at the center

of the chip. This may not be as accurate for capturing the MOSFET temperature due to coupling since there is a temperature gradient across the top of the chip. Therefore, computing the average temperature of the top of chip may result in a closer match in Fig. 11.

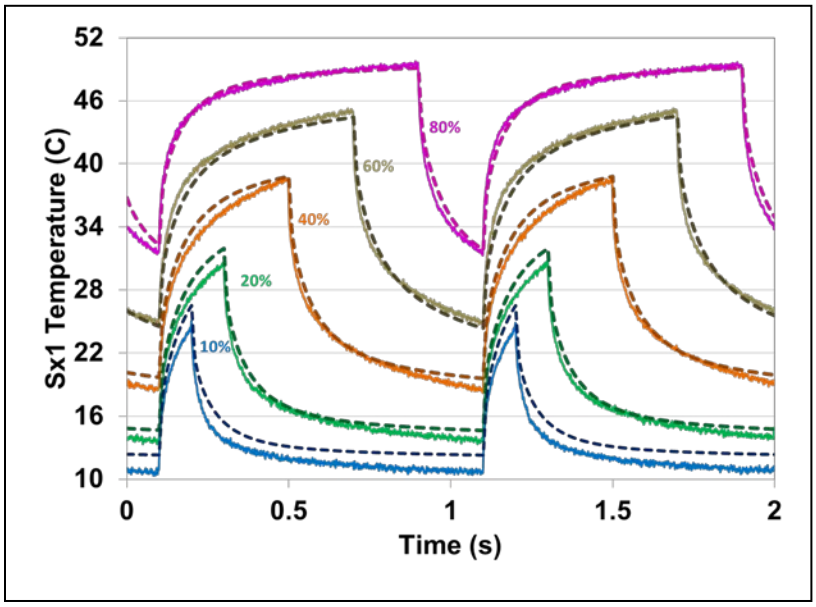

Fig. 4-16 *Qx1* transient heating measured versus simulated.

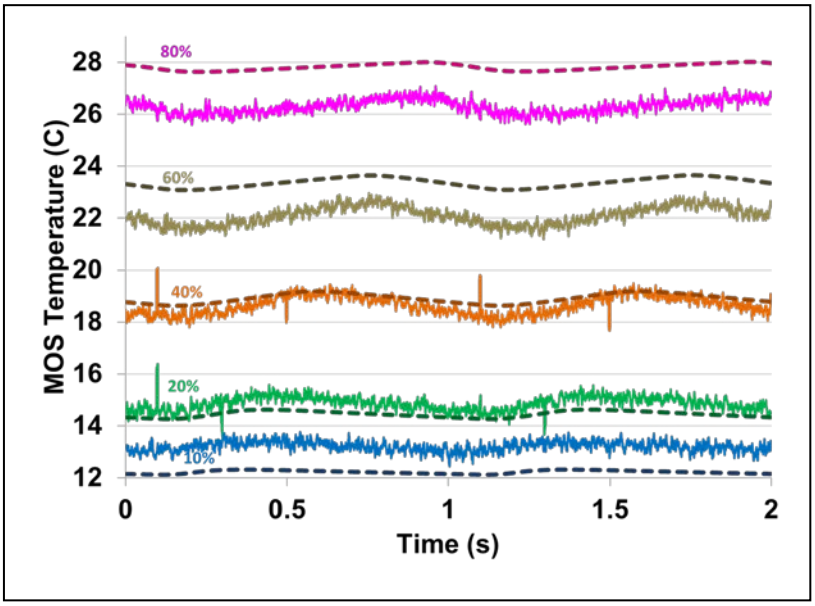

Fig. 4-17 MOS1B transient heating measured versus simulated.

Chapter 5 Electrical Model Parameter Extraction and Validation

5.1 Introduction

The devices that make up the generation 2 soft-switching module in Fig. 3-1 are summarized in Table 5-1 . The electrical models used in this work are based on the available physics-based electrical models available in the SABER® circuit simulator. The IGBT model is based upon the model developed by Hefner [56]. The diode models are based upon the model developed in [14]. The MOSFET uses the model developed in [13] and [57] which is based on the MOSFET model within the Hefner IGBT model but has been modified for a CoolMOS device. In particular the highly non-linear device capacitance inherent to CoolMOS technology has been captured. This is very important to accurately capture the output capacitance of the device since it directly affects the soft-switching behavior of the device which is essential in this work.

This chapter discusses the required device parameters and extraction procedures for the electrical device models used in modeling the generation 2 soft-switching module.

Table 5-1 Soft-switching Module Devices

Reference Designator	Rating	Part Number
Q1 + Q2	600V,200A	CM200DY-12NF
M1+M2	650V,60A	IPW60R045CP
D1+D2	600V,150A	CM200DY-12NF
Qx1+Qx2	600V,150A	CM150DY-12NF
Dx1+Dx2	600V,75A	CM75TL-12NF
Dx3+Dx4	1200V,100A	CM100DY-24NF
Dx5+Dx6	1200V,50A	CM50TL-24NF

The traditional way of modeling semiconductor models in SPICE-based circuit simulators has been to use linear approximations to describe the forward and reverse operating characteristics. While there are some SPICE-based physics-based semiconductor models, the temperature used by the device models are chosen by the user prior to simulation and remains constant during the simulation. The models used in this work contain temperature dependent model parameters obtained by using extracted values of the model parameters versus temperature. An accurate extraction sequence is needed to resolve the temperature dependence of the model parameters. The advantage of using physics-based models for semiconductor devices is that the well-known temperature dependent properties of silicon can be used to describe the temperature dependence of the model, and only a few temperature dependent model parameter expressions must be developed to describe the device to be modeled.

The electrical models developed in this chapter are coupled with the thermal models developed in Chapter 4 to create a fully coupled dynamic electro-thermal model to be used in the soft-switching inverter simulation.

5.2 Diode Model

The extracted diode parameters and temperature dependent coefficients are used in an existing electro-thermal unified diode model in SABER® [14] and [58]. The unified diode model represents the unification of low-power, microelectronic diode modeling technology and the latest developments in high-power diode modeling. This model allows the user to describe either low or high power diodes.

We begin with describing the forward-bias operating region. The DC characteristics are shown in Fig. 5-1. The effects shown are low-level depletion recombination, normal low-level injection, high-level injection, emitter recombination, and series resistance.

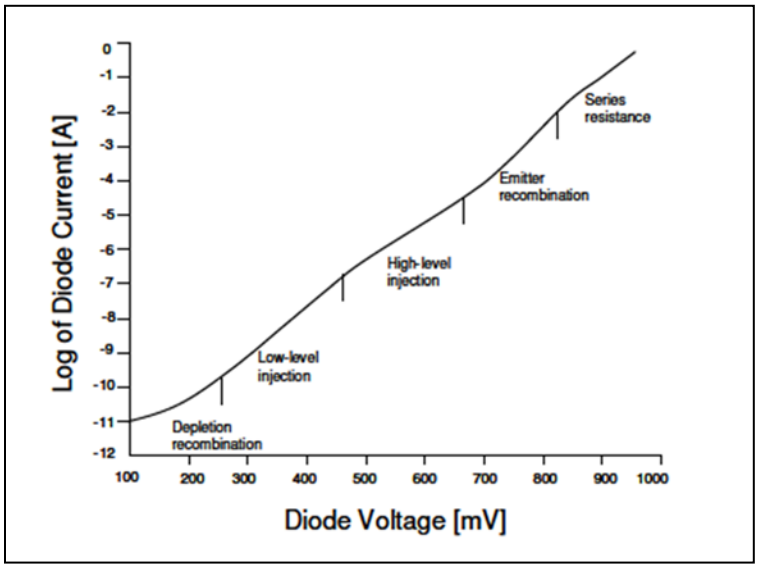

Fig. 5-1 Forward dc characteristic of diode model [14].

The objective of the thesis is to describe a process of electro-thermal system simulation. Therefore, it is not important for us at this time to describe the entire diode forward characteristic as seen in Fig. 5-1. For now we will concern ourselves with modeling more the diode operating region we expect in system level simulation. This does not include the current densities that would be described by the depletion region recombination or the emitter recombination. More importantly, we will include the low-level and high-level injection and series resistance effects typically seen in power diodes. We remove the recombination effect by setting the diode parameter, *ISR*, to be zero. We will also not include the emitter recombination effect by setting the diode parameter, *ISE*, to be zero. The following expression is the classical expression describing low-level injection [14].

$$i_{Ldiode} = ISL \cdot (e^{\frac{V_j}{NL \cdot V_T}} - 1) \tag{5.1}$$

An equivalent expression is used for high level injection. This effect is present in the power diodes and should be modeled. For now we will make use of (5.1) to describe as closely as possible both the low and high level injection regions. The equation describing high level injection is the same equation as (5.1) with *ISL* and *NL* replaced with *ISH* and *NH* respectively.

Fig. 5-2 shows the measured forward I-V curves over several temperatures for a typical. It can be seen from the curves that the saturation current goes up as a function of temperature. This has the effect of shifting the curves to the left. Also, the mobility goes down with temperature causing the on resistance, R_{on}, to increase thus decreasing the slop of the I-V curve in the higher current region.

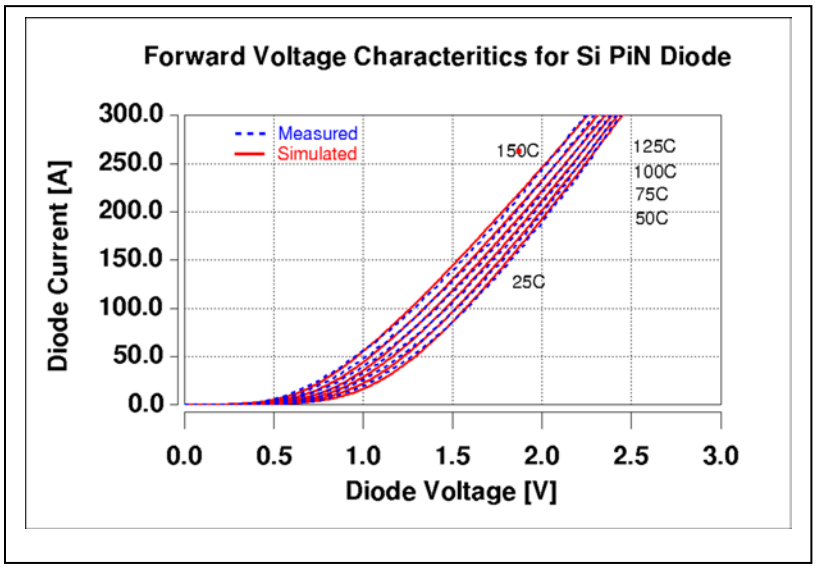

Fig. 5-2 Measured forward IV curves over temperature.

From (5.1) the parameters *NL* and *ISL* need to be determined. Both of these parameters are a function of temperature and need to be extracted and described over temperature. We note that

the parameter V_T is also a function of temperature and is a well-known property of silicon and not described in this chapter.

The first step in extracting the above mentioned parameters is to determine the diode equivalent series resistance. This is proportional to the inverse slope of the forward I-V curve in the high level injection region (higher current). Fig. 5-3 shows the equivalent series resistance and how the junction voltage of the diode, V_j, and the actual measured voltage, V_D, are related.

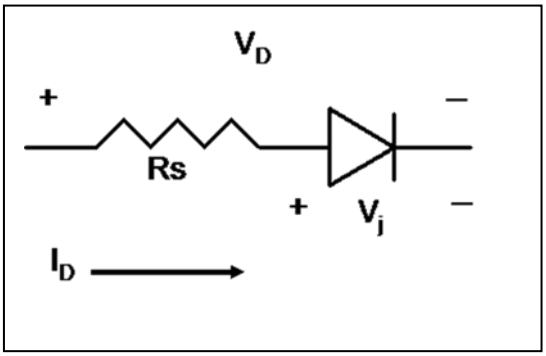

Fig. 5-3 Diode Equivalent Series Resistance.

The junction voltage, *Vj*, is calculated from Fig. 5-3.

$$V_j = V_D - I_D \cdot R_s \tag{5.2}$$

The measured diode voltage, $V_{D,}$ and the measured diode current, $I_{D,}$ are used with (5.2) in (5.1) to extract the diode parameters *ISL* and *NL*, where i_{Ldiode} is replaced with the measured data I_D. Taking the log of (5.1):

$$\log I_D = \log(ISL(e^{\frac{V_j}{NL \cdot V_T}} - 1)) \tag{5.3}$$

Expanding (5.3) and simplifying:

$$2.3\log I_D = 2.3\log(ISL) + \frac{V_j}{NL \cdot V_T} \tag{5.4}$$

Equation (5.4) is a linear relationship and the slope and y intercept of the data points can be used to determine *NL* and *ISL*.

The next step is to determine the temperature dependent behavior of *Rs*, *NL* and *ISL*. The temperature dependence of all the following temperature dependent diode parameters is given in. The temperature dependence of *Rs* is given by:

$$Rs(T) = Rs(T_{nom}) \cdot (1 + TRS1(T - T_{nom}) + TRS2(T - T_{nom})^2) \tag{5.5}$$

The temperature dependent coefficients needed are *TRS1* and *TRS2*. The temperature dependence of *NL* is given by:

$$NL(T) = NL(T_{nom}) \cdot (1 + TNL1(T - T_{nom}) + TNL2(T - T_{nom})^2) \tag{5.6}$$

The temperature dependent coefficients extracted from (5.6) are *TNL1* and *TNL2*. The temperature dependence of *ISL* is given by:

$$ISL(T) = ISL(T_{NOM}) \cdot \left(\frac{T}{T_{NOM}}\right)^{\frac{XTI}{n}} \cdot e^{\left(\frac{T}{T_{NOM}} - 1\right) \cdot \left(\frac{E_g}{n \cdot V_T}\right)} \tag{5.7}$$

Where the bandgap voltage, E_g, is a well predicted temperature dependent semiconductor property. *XTI* describes the temperature dependence of *ISL*.

The unified diode models the reverse bias operating region, but again from a standpoint of system level simulation, this region of operation is not necessary to describe. The reverse bias operating area does not contribute to the overall losses when compared to the forward and transient losses; therefore we disable this feature by setting *ISZ* to be undefined.

The most important feature to capture in the diode model is the transient characteristic. The diodes behavior during transients directly contributes to the high energy losses that occur in real system behavior. The diode reverse recovery characteristic for example directly relates to the

high turn-on losses seen by the IGBT in inverter applications. The peak current that the IGBT has to handle is directly related to how well the diode behaves during the reverse recovery. The next discussion describes the modeling of the diode reverse recovery behavior.

Reverse recovery occurs when a forward conducting diode is rapidly turned off. The charge that is built up in the diode while it is forward biased must be removed before the device can settle into steady state. Fig. 5-5 shows the power diode, PIN, carrier distribution profile and potential distribution for high level injection conditions.

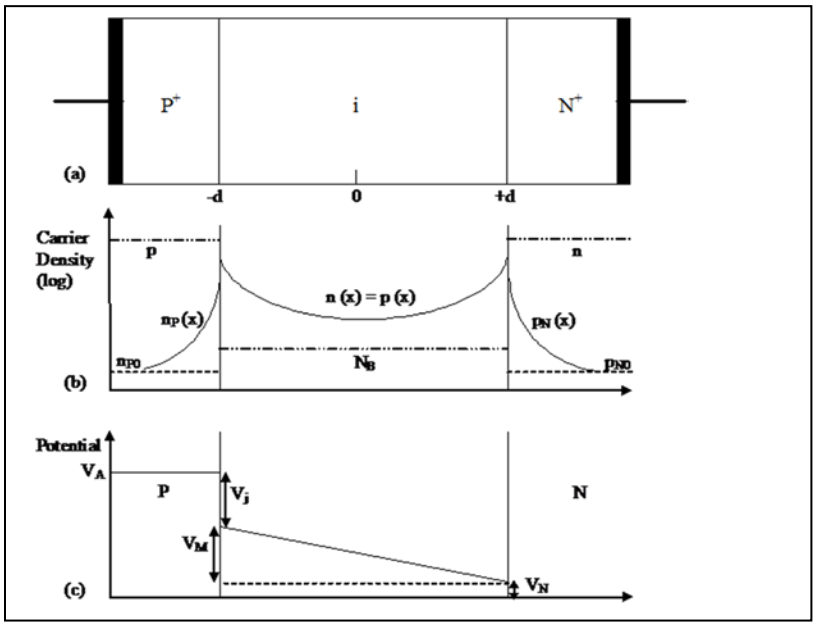

Fig. 5-5 . (a) PiN diode representation, (b) corresponding carrier distribution.

During forward bias, charge is distributed in the lightly doped i region in catenary fashion such that *n(x)=p(x)*. When the device is switched off, charge can either recombine, diffuse out of the lightly doped region, or be swept out due to a high field. The unified diode model accounts for all of these possibilities [14]. Either way, a large reverse current has to account for this charge removal. Fig. 5-6 shows the relationship between the diode voltage and current when

commanded to turn-off. The diode does not start to block voltage until the diode hits the peak reverse recovery current.

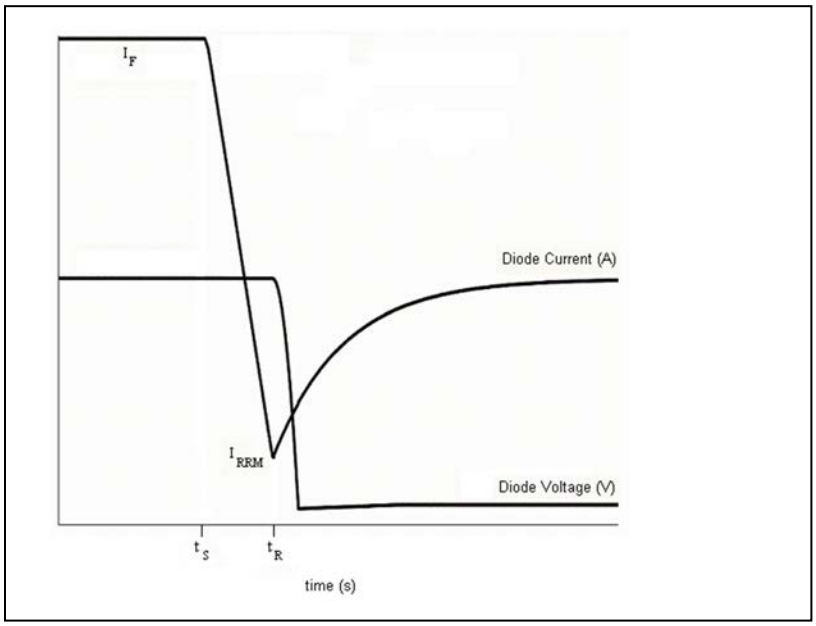

Fig. 5-6 Ideal reverse recovery characteristics for PiN diode.

The model parameters *TSW* and *TM*, along with *TT*, control the charge sweep out effect and diffusion effect, respectively. The two time constants seen in Fig. 5-6 are calculated as follows:

$$\tau_1 = \frac{TT \cdot TSW}{TT + TSW} \tag{5.8}$$

$$\tau_2 = \frac{TT \cdot TM}{TT + TM} \tag{5.9}$$

Fig. 5-7 shows the test circuit used for characterizing the Si diodes for reverse recovery, and Fig. 5-8 shows the behavioral representation including parasitic elements used for diode model validation. It is important to note that the test circuit in Fig. 5-7 is well-characterized, meaning that the values of all circuit components and parasitic elements are known. To operate the test circuit in Fig. 5-7, first the vacuum tube is turned on to establish the test current i_L in the inductor *L*. Once the test current is reached, the tube is ramped off and the inductor current is commutated

to the Device Under Test (DUT). To initiate the reverse recovery test, the tube is ramped on with a well-controlled di_Q/dt at the tube anode. This results in a negative di_D/dt being applied to the DUT. As the diode begins to recover the diode voltage v_D rises toward the power supply voltage V_{drive} completing the recovery test [59].

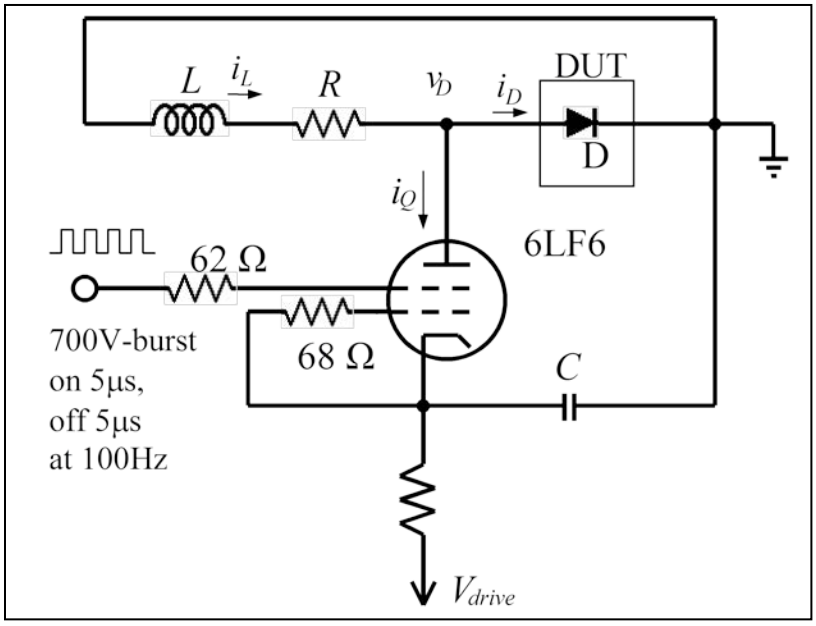

Fig. 5-7 High-speed reverse recovery test circuit.

The circuit of Fig. 5-7 uses a 6LF6 vacuum tube as a driver device in place of the usual MOSFET to achieve low parasitic capacitance at the DUT anode and an extremely fast switching speed. The 51 Ω resistor R isolates the DUT from the parasitic capacitance of the 30 mH inductor L and is also used to quickly reset the inductor current to zero after each test. The dv/dt of the square wave applied to the tube screen is varied to achieve different di_D/dt values for the DUT [59].

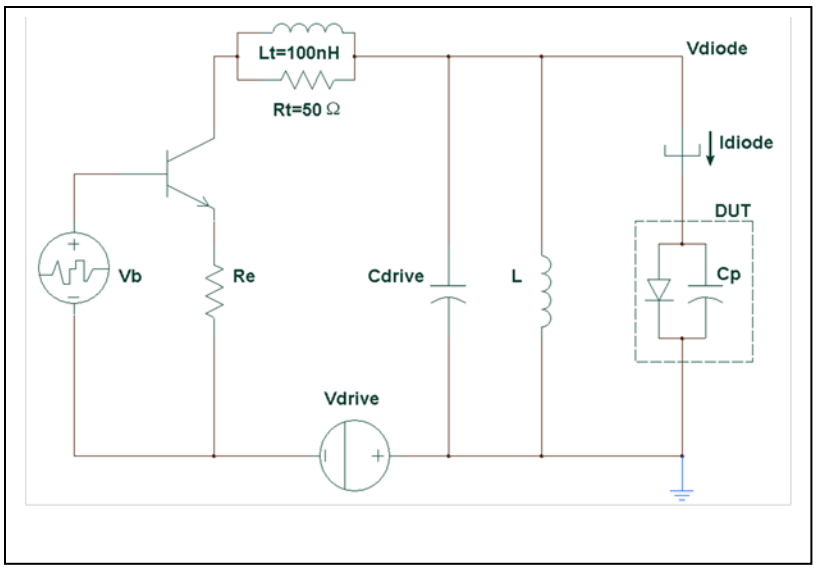

Fig. 5-8 Behavioral model of reverse recovery test circuit.

Fig. 5-8 uses an ideal bipolar transistor model with an emitter follower resistor, R_e, to emulate the di_D/dt applied by the tube. The bipolar transistor model capacitance parameters are set to zero and replaced by the 40 pF output capacitance of the tube combined with C_{drive}. The next most important parasitic elements of the test circuit are the 100 nH tube inductance L_t and the 50 Ω tube resistance R_t that result in a small voltage overshoot near the end of the diode current recovery waveform. The inductor L remains at 30 mH as in Fig. 5-7. The pulse width of the signal generator V_b is varied to determine the forward current for the reverse recovery test, and the rise time of V_b determines the di_D/dt applied to the DUT at turn-off [59].

Fig. 5-9 shows the measured results of a diode reverse recovery over different temperatures. The peak reverse recovery increases in magnitude with temperature. This will lead to greater losses in the inverter simulation as temperature increases because the IGBT will have to support a larger current at turn-on along with the bus voltage. This is because lifetime increases with temperature. Therefore more charge is present in the base region and needs a greater amount of reverse current to remove all the charge.

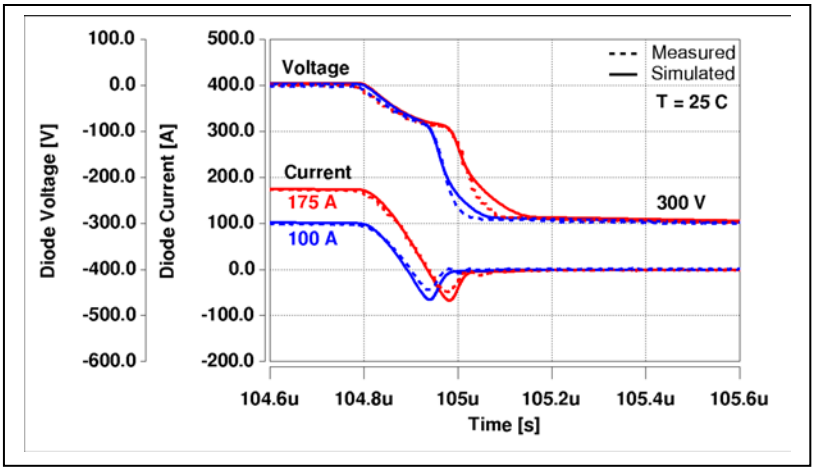

Fig. 5-9 Measured Reverse Recovery of diode.

The circuit in Fig. 5-8 is implemented in SABER® to extract the diode parameters *TT*, *TM*, and *TSW* over temperature. The parameters are varied until the simulated results produce the same time constants and reverse peaks as the measured results seen in Fig. 5-9. The diode parameter, *TT* has a temperature dependence. The temperature dependence of *TT* is known to be the following [59]:

$$TT(T) = TT(T_{nom}) \cdot \left(\frac{T}{T_{nom}} \right)^{\beta} \tag{5.10}$$

5.3 IGBT Model

The electrical parameters for the IGBT model, developed by Hefner for the SABER® simulator, are described in this section. Fig. 5-10 shows one-half of the symmetric IGBT cell consisting of the MOSFET and bipolar equivalent circuit components [11]. An n-channel IGBT behaves as a pnp bipolar transistor that is supplied base current by an n-channel MOSFET.

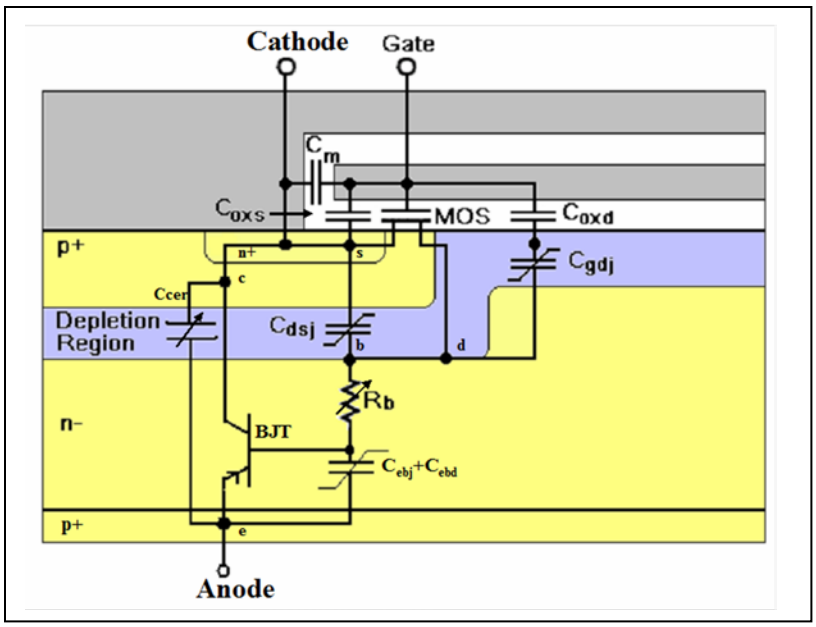

Fig. 5-10 IGBT equivalent circuit model superimposed on one half of the symmetric IGBT cell [56].

In Fig. 5-10, MOS represents the MOSFET channel, *Rb* is the undepleted base or drift region resistance, *Cdsj* is the non-linear drain-source junction capacitance, *Cgdj* is the non-linear gate-drain overlap depletion capacitance, *Coxd* is the constant gate-drain overlap oxide capacitance, *Coxs* is the constant gate-source overlap oxide capacitance, and *Cm* is the constant gate-source metallization capacitance. *Cebd* is the emitter-base diffusion capacitance and *Cebj* is the Emitter-base depletion capacitance. *Ccer* is the collector-emitter redistribution capacitance. The BJT represents the equivalent pnp transistor that exists within the IGBT [11].

A positive gate bias applied will cause the p-base region underneath the gate to invert thus allowing electrons to flow from the n+ to the n-drift region. This provides the base current for the vertical P-N-P transistor in the IGBT structure. Holes are injected from the p+ region on the Anode side to the n-base region. Thus the characteristics of both the MOSFET and internal PNP transistor will determine the overall current capability of the IGBT [11].

To model a particular IGBT, an extraction sequence is needed to determine the values of all of the model parameters from electrical measurements. The extraction process divided into a sequence of steps where only a few unknown parameters are obtained at each step. This is done by selecting electrical characteristics that isolate a few unknown parameters at a time and fitting the measured data to the corresponding model equation. The parameters obtained at each step are then used as known values in subsequent steps. In general, dynamic measurements are used first to access the internal bipolar transistor. The internal MOSFET characteristics are then calculated using the bipolar current gain characterized in previous extraction steps. Table 5-2 is a list of IGBT model parameters, the electrical characteristics that are used to extract each parameter, and the name of the automated extraction program that implements the extraction step. The parameters are listed in the order that they are extracted [12]. In the first step, the device active area is extracted by visual inspection of the chip size.

Table 5-2 Parameters, Extraction Programs and Characteristics

Parameter symbol	Parameter name	Program	Extraction Characteristic
A	Device active area		Chip Size
τ_{HL}	Lifetime	LFTMSR	Low V_A decay rate
I_{sne}	Emitter Electron Saturation Current	BTAMSR	Tail Size vs. Current Tail Size vs. V_A
W_B	Metallurgical base width		Tail Size vs. V_A
N_B	Base Doping concentration		
V_T	Threshold voltage	SATMSR	Saturation current vs. Vgs Saturation current vs. Vgs
$K_p = K_{psat}$	Saturation region transconductance		High saturation current vs. Vgs
θ	Transverse electric field parameter		Low saturation current vs. Vgs
K_{fl}	Low current transconductance factor		Low saturation current vs. Vgs
dV_{Tl}	Low current threshold voltage differential		
$K_{plin} = K_p \cdot K_f R_s$	Linear region transconductance parameter	LINMSR	On-state voltage vs. Vgs
N_b	Drain series resistance		On-state voltage vs. Vgs
	Drift region dopant density		On-state voltage vs. Vgs
$C_{gs}C_{oxd}$	Gate-source capacitance	CAPMSR	Gate charge at low gate voltage
A_{gd}	Gate-drain overlap oxide capacitance		Gate charge at high gate voltage
V_{Td}	Gate-drain overlap depletion threshold		Gate-drain charge Gate-drain charge

5.3.1 LFTMSR

To extract the minority carrier lifetime parameters, τ_{HL} and $I_{K,\tau}$, the turn-off tail current for a constant voltage condition is first measured and transferred to the appropriate software. The exponential current decay rate versus current of the data is fitted to the model equation for constant voltage current decay [12].

$$\frac{d\ln I_T}{dt} \equiv \frac{dI_T}{I_T} = -\frac{1}{\tau_{HL}}\left(1+\frac{I_T}{I_{k,\tau}}\right) \tag{5.11}$$

The anode turnoff current, I_T, waveform is generated using a clamped large inductive load test circuit shown in Fig. 5-11.

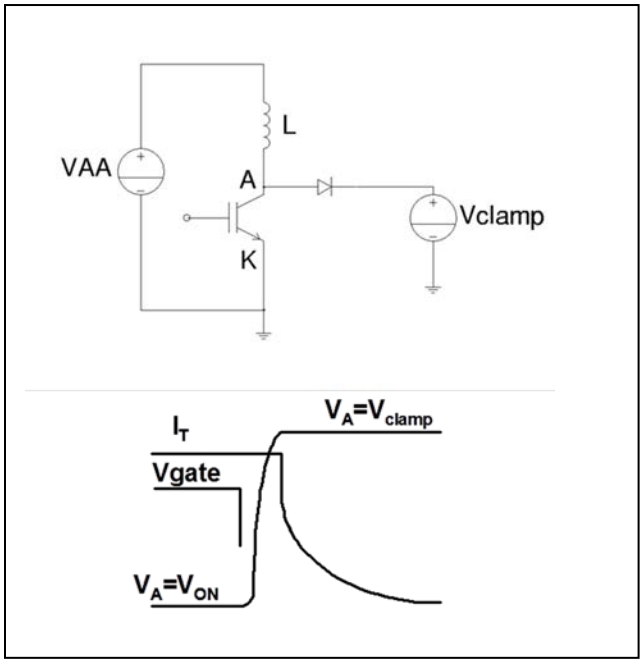

Fig. 5-11Clamped Inductive Load Test Circuit and waveforms.

This circuit is ideal because it simulates an actual power switching interval for the device where a constant voltage/current condition exists at turn-off. The power dissipation during turn-off of the IGBT is directly related to the minority carrier lifetime. The lifetime determines how fast the minority carriers in the IGBT base region, n- in Fig. 5-10, can be removed.

A large inductor is used because it results in a large current tail and maintains a constant current. Fig. 5-11 shows the test circuit along with the appropriate Anode voltage and Anode current generated at turn-off. Initially, the IGBT is turned on and the inductor is charge up to an

appropriate load current, I_T. When the gate voltage is turned off, the Anode voltage rises to the clamp voltage. The diode then clamps the anode voltage to the clamp voltage and the constant current from the inductor is maintained in the diode. When the clamp voltage is reached, the anode current of the IGBT initially drops very rapidly due the majority carrier MOS channel being removed. The remainder of the current, minority carriers in the IGBT base-region, tails off slowly, where the time constant of this decay is given by (5.11).

The IMPACT program to measure the tail current is called LFTMSR. First the tail current is captured from the scope and transferred to the software. Fig. 5-12 shows the user interface panel used by the LFTMSR program. Note that we are not using a buffer layer device. The top of the panel shows the measured turn-off tail captured from the scope and transferred to the LFTMSR program. The bottom panel shows the resulting current decay rate data versus current (green) obtained from the left hand side of (5.11). The number of points used in the numerical derivative calculation is specified by the user. The red curve in the bottom panel shows the least squares fit of the data to the equation on the right hand side of (5.11) where the values of τ_{HL} and $I_{K,\tau}$ calculated from the fit are displayed in the numerical display boxes. The zero current intercept is equal to $1/\tau_{HL}$ and the slope is used to extract $I_{K,\tau}$. The *Imaxlim* and *Iminlim* are needed to eliminate the high and low current effects not described in (5.11) [12].

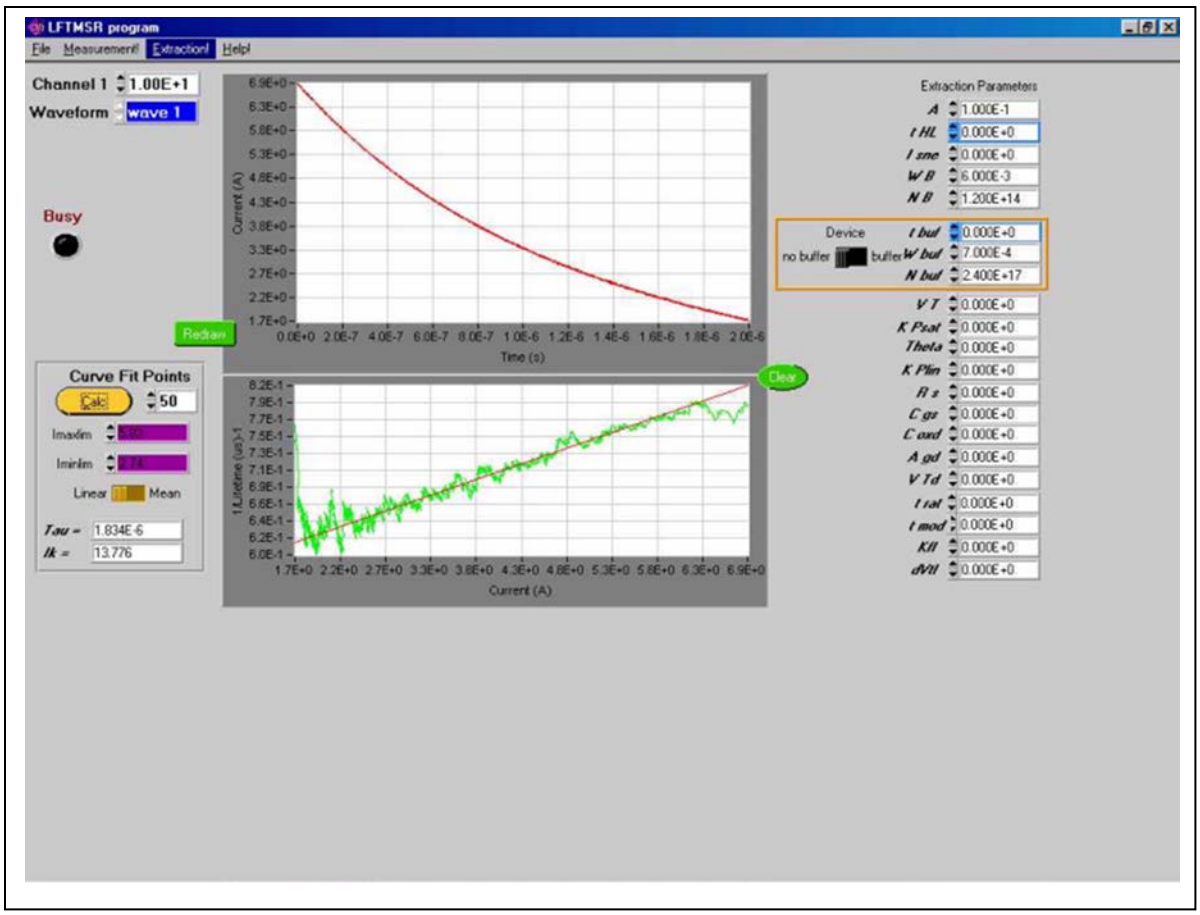

Fig. 5-12 LFTMSR user interface [12].

The lifetime parameter, τ_{HL}, is a function of temperature. Therefore this parameter needs to be extracted over temperature and its temperature dependent parameter needs to be calculated from the following equation:

$$\tau_{HL}(T_j) = \tau_{HLO}\left(\frac{T_j}{T_o}\right)^{\tau_{HL1}} \tag{5.12}$$

The lifetime increases with temperature and this will result in a larger current tail during turn-off thus increasing the switching turn-off loss.

5.3.2 BTAMSR

The relative size of the turn-off current tail versus anode current and anode voltage is used to extract the emitter electron saturation current I_{sne}, the metallurgical base width W_b, and the base doping concentration *Nb*. The extraction software determines the relative size of the tail by using the following equations [12]:

$$\beta_{tr,V} = \frac{I_T(0^+)}{I_T(0^-) - I_T(0^+)}\Big|_{VA=constant} = \beta^{\max}{}_{tr,V}\left(1 + \frac{I_T(0^+)}{I_k}\right)^{-1} \tag{5.13}$$

Where:

$$\beta^{\max}{}_{tr,V} = \left(\left(\frac{W}{L}\right)^2 \frac{\coth(\frac{W}{L})}{2\tanh(\frac{W}{2L})} - 1\right)^{-1} \tag{5.14}$$

And

$$I_{sne} \equiv \frac{\tanh^2(\frac{W}{2L})}{(\frac{W}{L})^4}\left(\frac{(4qn_iAD_p)^2}{L^2(1+\frac{1}{b})}\right)\cdot\frac{1}{\beta^{\max}{}_{tr,V}I_k} \tag{5.15}$$

First the BTAMSR program plots the tail current waveform and determines the initial current $I_T(0+)$ and the initial current drop off magnitude $I_T(0-)$. This information is used to build the β_{tr} versus the initial tail current relationship. Fig. 5-13 shows the user interface of the BTAMSR program. The top panel shows the measured tail current for two different initial currents, $I_T(0+)$. β_{tr} is then determined and the inverse is plotted versus initial tail currents $I_T(0+)$ seen in the bottom panel of Fig. 5-13. A least squares fit is performed on the date and the resulting relationship is linear with a slope of $1/(I_k\, b^{max}{}_{tr})$ and with a zero current intercept of $1/\, b^{max}{}_{tr}$.

The slope is used with (5.15) to calculate I_{sne} and the zero current intercept is used to obtain the value of W at the given anode voltage from (5.14) [12].

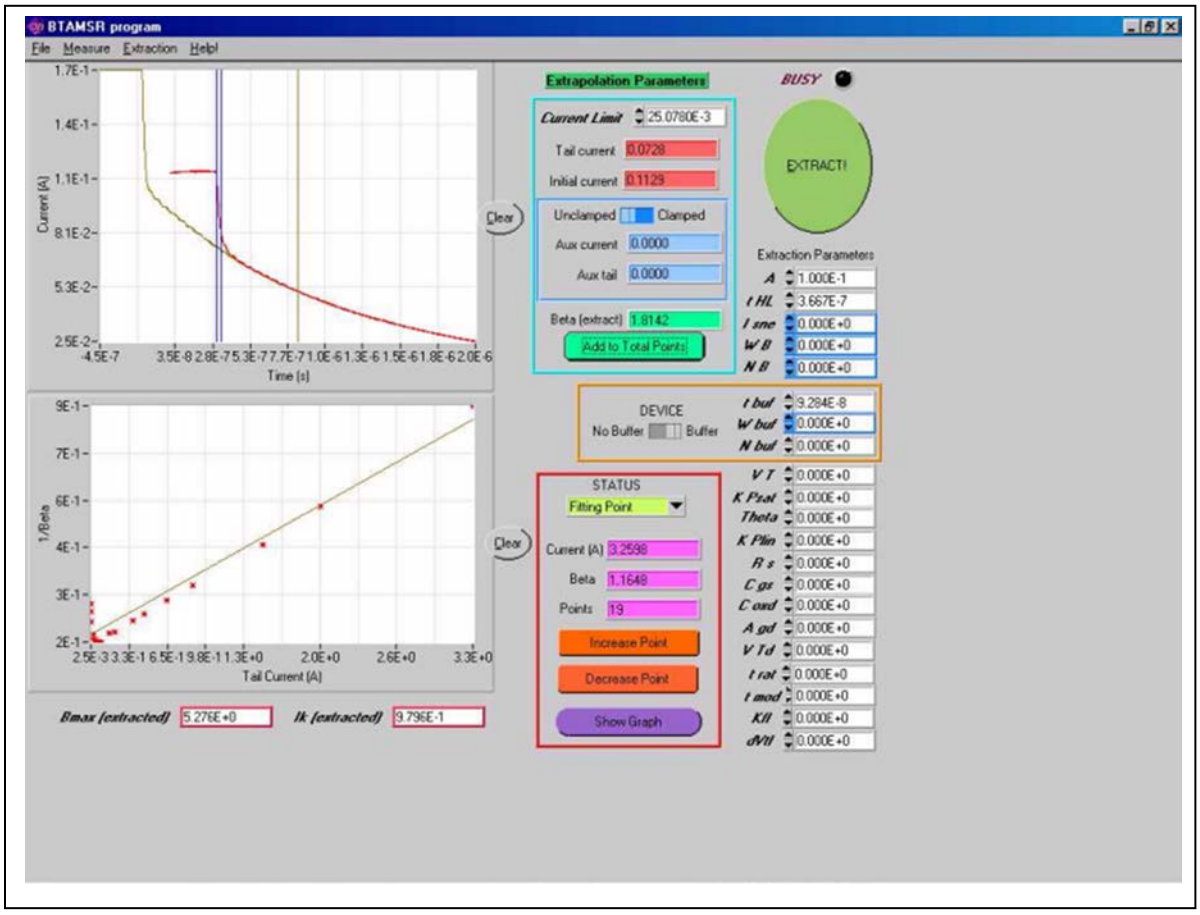

Fig. 5-13 BTAMSR user interface [12].

Fig. 5-14 shows the BTAMSR sub-panel to extract W_B and N_B. The emitter electron saturation current is also a function of temperature and is given as follows:

$$I_{sne}(T_j) = \frac{I_{sneo}\left(\frac{T_j}{T_o}\right)^{I_{sne1}}}{\exp\left(14000(1/T_j - 1/T_o\right)} \tag{5.16}$$

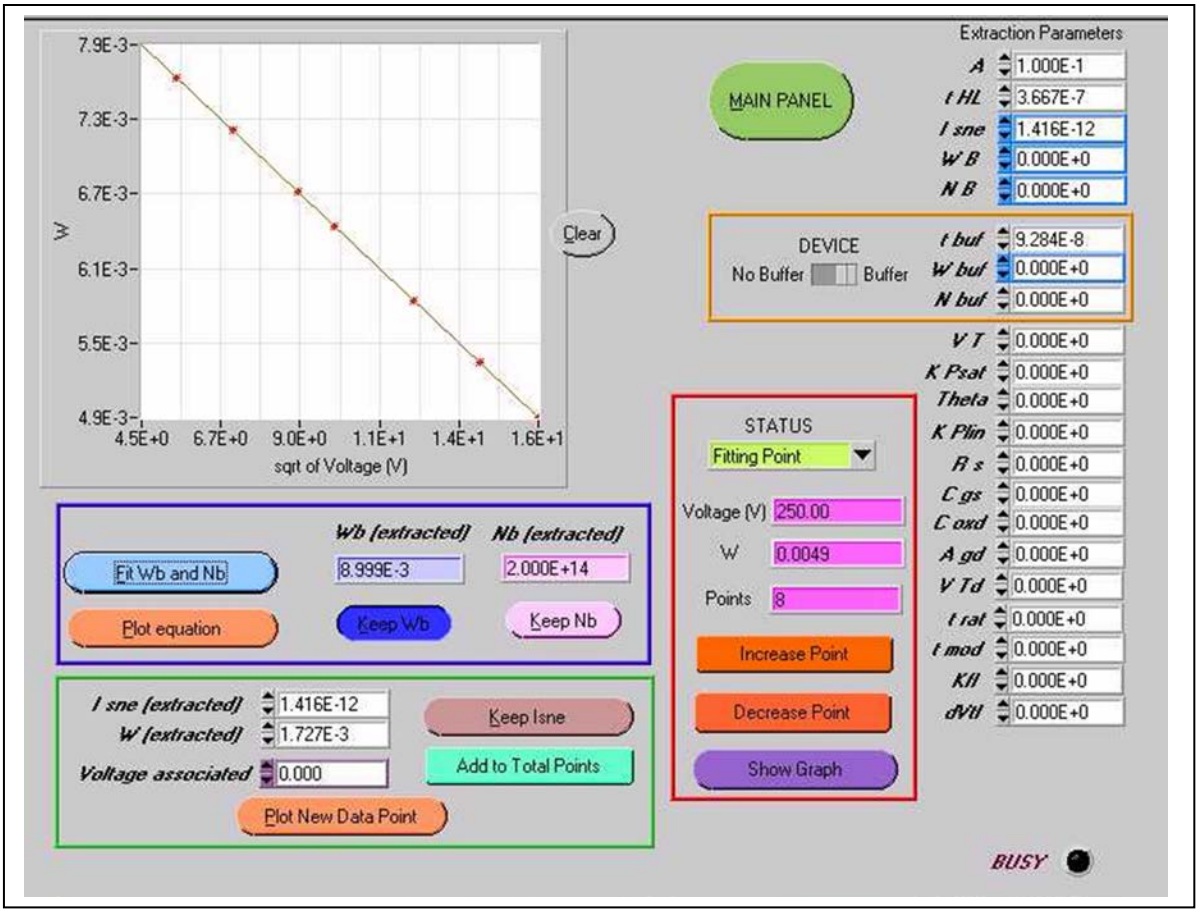

Fig. 5-14 BTAMSR subpanel to calculate WB and NB [12]

5.3.3 SATMSR

The saturation current versus gate voltage is used to extract the internal MOSFET transconductance parameters for the saturation region K_{psat}, the high current region θ, the low current region K_{fl} and d_{VTl}, and the threshold voltage V_T.

To perform the extraction, the IGBT saturation current is measured versus gate voltage and divided by the current gain of the internal bipolar transistor (calculated using the parameters obtained by the previous two extraction programs) to obtain the internal MOSFET saturation

current I^{sat}_{mos}. The value of the square root of I^{sat}_{mos} versus gate voltage is then used to extract the parameters of the internal MOSFET [12].

Fig. 5-15 shows the user interface for the SATMSR program. The upper curve shows the saturation current versus gate voltage obtained from the TEKTRONIX curve tracer. The internal transistor gain is calculated first and then the MOSFET saturation current is extracted using the following relationship [12].

$$I^{sat}_{moss} = I^{sat}_{T}(1+\beta_{ss}) \tag{5.17}$$

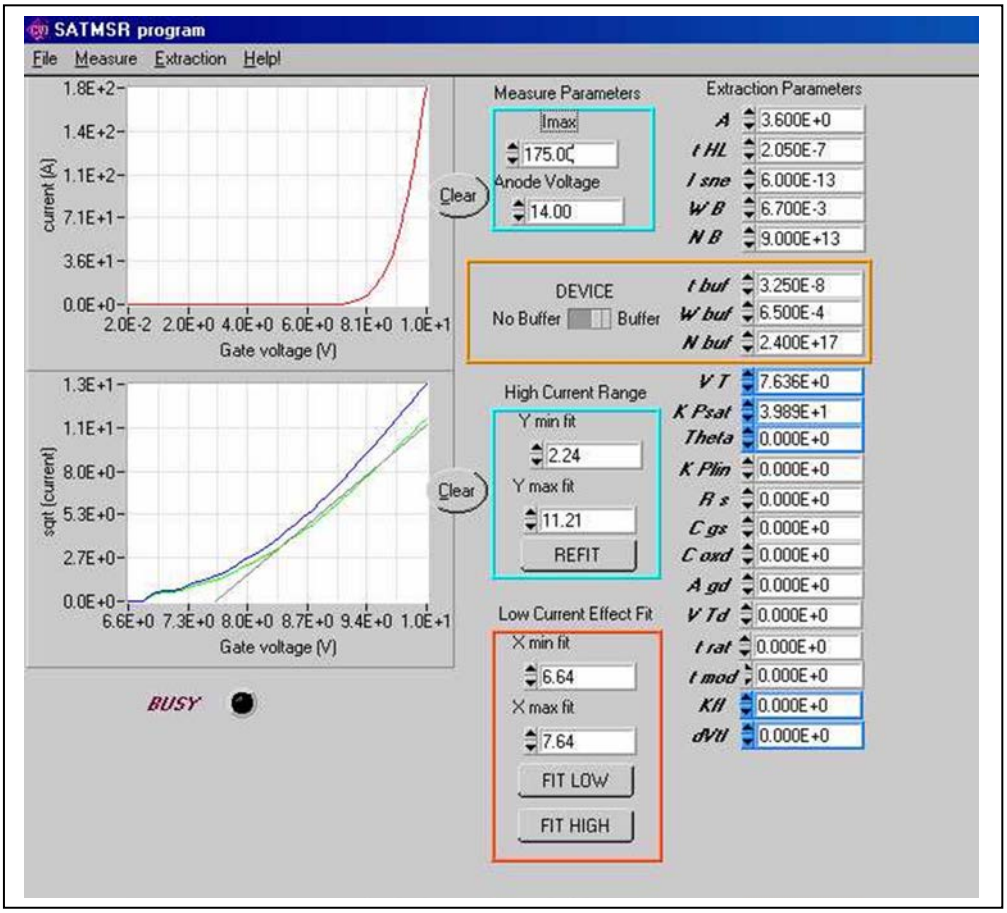

Fig. 5-15 User interface for SATMSR [12]

The square root of I^{sat}_{mos} and I^{sat}_{T} are plotted in the bottom curve (green and blue curves respectively) of Fig. 5-15.

A least squares fit is then performed on the following equation to extract V_T and K_{Psat} [12].

$$\sqrt{I_{mos-sat}} = \sqrt{\frac{K_{psat}}{2}}(V_{gs} - V_T) \tag{5.18}$$

The saturation transconductance, K_{psat} , and threshold voltage V_T is a function of temperature and given by :

$$K_{psat}(T_j) = K_{posat}(T_o / T_j)^{K_{p1sat}} \tag{5.19}$$

$$V_T(T_j) = V_{TO} + V_{T1}(T_j - T_o) \tag{5.20}$$

5.3.4 LINMSR

The linear region on-state voltage versus gate voltage for a constant anode current is used to extract the linear region transconductance K_{plin} [12].

Fig. 5-16 shows the user panel for the LINMSR program. The curve generated in the top of the panel is the anode voltage versus gate voltage pairs that result in constant current. The bottom curve shows a least squares fit to the parameter equation describing the linear region of the device [12].

$$V_{on} = V_r + \frac{I_T}{K_{plin}\left(V_{gs} - V_T\right)} \tag{5.21}$$

Where

$$V_r = (R_b + R_s)I_d + \frac{I_d\theta}{K_{plin}} \tag{5.22}$$

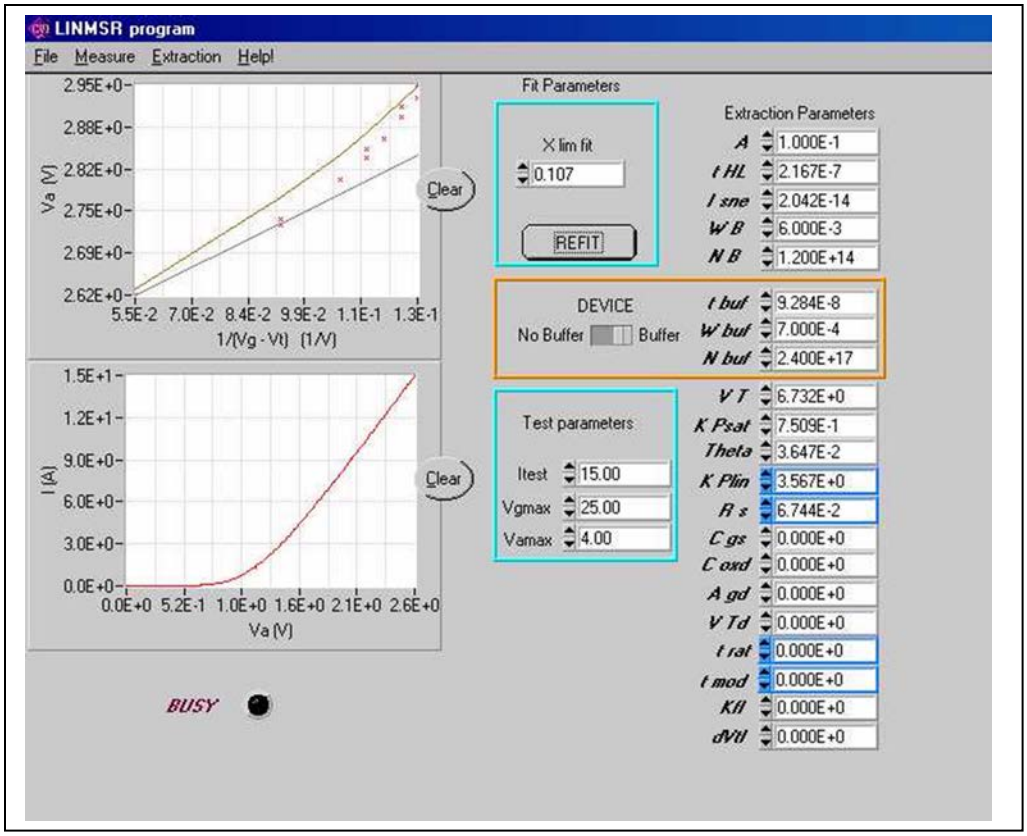

Fig. 5-16 LINMSR user interface [12].

The slope of the linear fit determines K_{plin} and the intercept determines V_r. The temperature dependence for K_{plin} is given by (5.23):

$$K_{plin}(T_j) = K_{polin}(T_o / T_j)^{K_{p1lin}} \tag{5.23}$$

5.3.5 CAPMSR

To begin the extraction of the transient parameters, the gate charge characteristics are captured on the oscilloscope. The gate charge characteristics are acquired by applying a constant gate current to the gate of the IGBT. These waveforms are shown in the top graph of the front panel for the CAPMSR program, illustrated in Fig. 5-17. This program uses the gate- and gate-drain charge characteristics including the effects of negative gate voltage inversion of the gate-drain overlap region to extract the gate-source capacitance C_{gs}, the gate-drain overlap oxide

capacitance C_{oxd}, the gate-drain overlap area A_{gd}, and the gate-drain overlap depletion threshold V_{Td} [12].

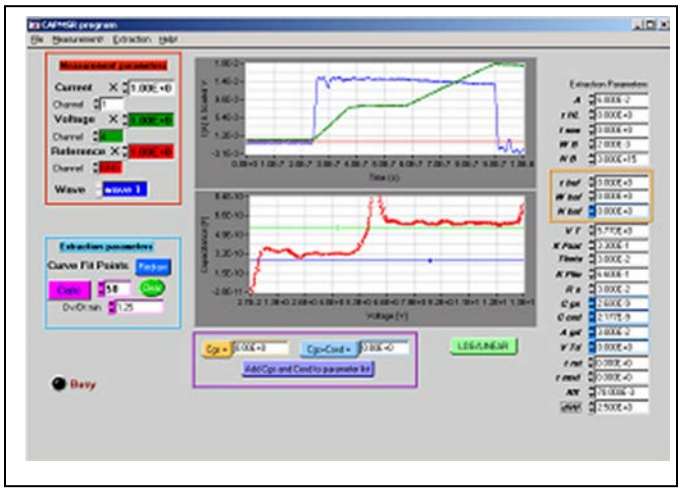

Fig. 5-17 CAPMSR user interface [12].

The first step in the extraction involves the extraction equation:

$$C(V) = \frac{I}{dV/dt} \tag{5.24}$$

Using equation (5.24), the program calculates C(V) vs. voltage curve, as shown in the bottom graph on the front panel in Fig. 5-17. The user controls the minimum value of *dV/dt* and the number of derivative points for each calculation. The values of C_{gs} and C_{oxd} are determined from I_g and *dVgs/dt* during the positive voltage portion of gate charge curve. For positive values of gate voltage, there are essentially three distinct phases in the gate voltage waveform. During the first phase, V_{gs} rises with a constant slope as the constant gate current charges the constant gate-source capacitance C_{gs}. Therefore, it is during this portion of the gate voltage waveform that C_{gs} is extracted by dividing the digitized values of the gate current waveform by the time rate-of-change of the digitized gate voltage waveform.

During the second phase or plateau region of the gate voltage waveform, V_{gs} remains relatively constant, and V_d falls as the gate current charges the two-phase, voltage dependent gate-drain capacitance C_{gd}. Therefore, the voltage dependence of the gate drain depletion capacitance is obtained by dividing the digitized values of the gate current waveform by the time rate-of-change of the gate-drain voltage computed from the digitized values of gate and anode voltage waveforms.

During the third phase of the gate voltage waveform, V_d remains relatively constant, and V_{gs} rises as the gate current charges the sum of the gate-drain overlap oxide capacitance C_{oxd} and the gate source capacitance C_{gs}. Now, it is possible to extract C_{oxd} from the previously extracted value of C_{gs} in the first phase.

In the bottom graph of Fig. 5-17, the cursors are placed on the flat portions of the numerically calculated capacitance versus voltage curve that corresponds to the section of the gate voltage waveform that is due to C_{gs} and that due to C_{gs} and C_{oxd}, as explained above.

5.4 Power MOSFET

The power MOSFETS used in the hybrd switch of the generation 2 module shown in Fig. 3-1 is an INFINEON CoolMOS^{TM} device. CoolMOS devices have similar on-state performance to that of the conventional power MOSFET while having a much lower on-resistance but similar blocking capabilities. The CoolMOS MOSFET model developed in [13] is based upon the internal MOSFET formulation utilized in the Hefner IGBT model with minor changes to some of the model equations. Therefore the MOSFET parameters and parameter extraction procedures used for the IGBT were readily available. The extraction programs described in the previous

section for the IGBT; SATMSR, LINMSR, and CAPMSR are used for the parameter extraction for the MOSFET.

The biggest deviation from the conventional MOSFET model formulation to the CoolMOS model is the nonlinear capacitance versus voltage behavior. The conventional MOSFET model is not sufficient enough to interpret the nonlinear Capacitance versus voltage behavior of the CoolMOS transistor. This behavior is essential in accurately capturing the soft-switching behavior of the soft-switching inverter used in this work. A new modeling approach has been developed to model the inter-electrode capacitances of CoolMOS in [57]. Due to the complexity of the numerical model described for the nonlinear capacitance in [57], the model implemented in SABER has been simplified and linearized using Taylor series. Additional fitting parameters have been included to gain better accuracy than the numerical model in the areas of transition points going from the accumulation to depletion regions.

Table 5-3 lists the model parameters that were used for modeling the inter-electrode capacitance for the CoolMOS model in Saber. The parameters are derived from the CAPMSR extraction sequence.

Table 5-3 Primary model parameters used for inter-electrode capacitances [13]

	Model Parameter	Comments
C_{gd}	C_{oxd_eff}	Gate-drain effective capacitance
	V_{FBD}	Drain flat band voltage
	A_D	Effective depletion width fitting parameter for drain
	B_D	Linearization fitting parameter for drain
	U_{FD}	Normalized Fermi potential for drain
C_{gs}	C_{oxs_eff}	Gate-source effective oxide capacitance
	V_{FBS}	Source flat band voltage
	A_S	Effective depletion width fitting parameter for source
	B_S	Linearization fitting parameter for source
	U_{FS}	Normalized Fermi potential for source
C_{ds}	C_{j0}	Zero-bias junction capacitance
	V_ς	Junction potential
	m	Grading coefficient

5.5 Model Validations against Experimental Data

The critical electrical device validations are shown in this section. A device validation prior to design optimization using electro-thermal simulations is critical to ensure accurate results. Parameters have been extracted over temperature for each device required to describe the soft-switching module. Given that the actual desired devices may not be available prior to design, a set of parameters can be extracted from devices with similar device fabrication and scaled using the reference area parameter in the device model. Table 5-4 shows the baseline devices that are used for characterizing devices within the generation II module shown Fig. 3-2. The parameters are extracted over temperature from the baseline devices in Table 5-4 and scaled using the chip area scaling parameter, a_{ref}, in the device model to correspond to the actual chip areas used in the

generation II module. The MOSFET area for the generation II module is 1.14 cm^2. The main IGBT area is 2.88 cm^2 while the auxiliary IGBT area is 1.16 cm^2. The area for the silicon Diode is 1.7 cm^2.

Table 5-4 Reference Chips for Parameter Extraction

Chip	Rating	Part Number
IGBT	600V,300A	CM300DY-12NF
CoolMOS	600V,60A	SDB06S60
Si Pin Diode	600V,150A	CM300DY-12NF

5.5.1 IGBT Output Characteristic

The output characteristic vs. measurement of the IGBT at 25 degree C is shown in Fig. 5-20. The output characteristic of the IGBT at 125 degree C is shown in Fig. 5-19. Good agreement is reach between the model and measurement and shows the model accurately captures the temperature dependence.

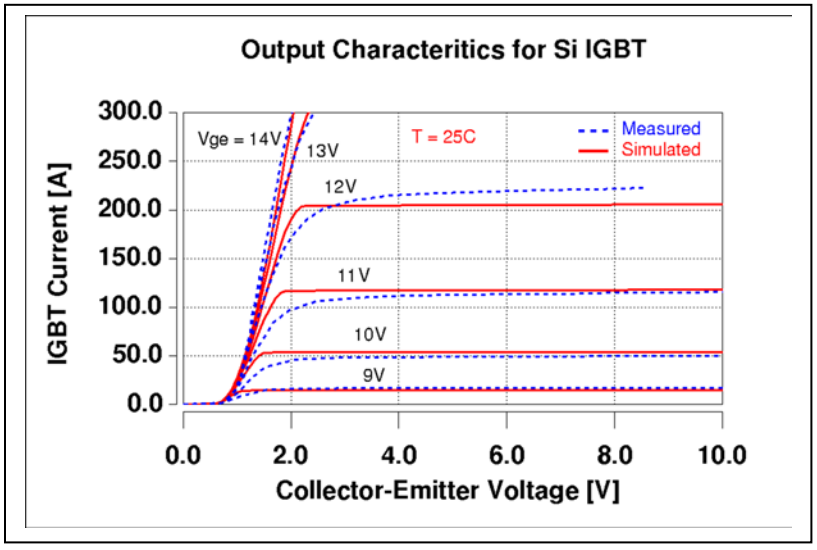

Fig. 5-18 Output Characteristic of IGBT at 25 Degree C Model vs. Measured

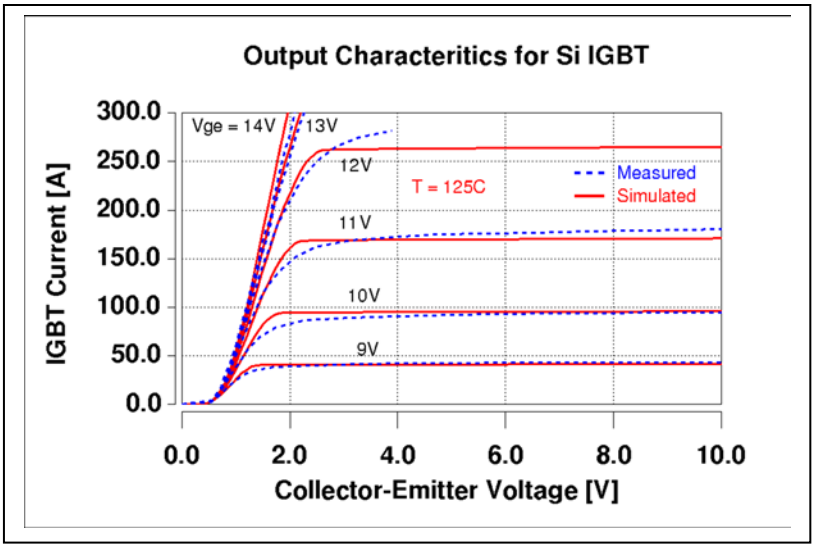

Fig. 5-19 Output Characteristic of IGBT at 125 Degree C Model vs. Measured

5.5.2 Switching Characteristic IGBT

The clamped inductive load is used to capture the turn-on characteristic of the IGBT at two different current levels vs. measured and is shown in Fig. 5-20. Good agreement is reach between the model and measured. Fig. 5-21 shows the turn of characteristic of the IGBT. The turn-off tail associated with the IGBT has been captured in the model and verified with measurement.

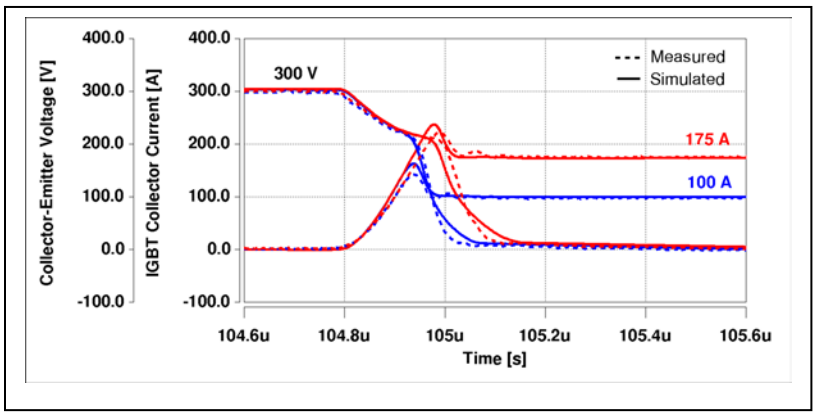

Fig. 5-20 IGBT Turn-on Characteristic Model vs. Measured

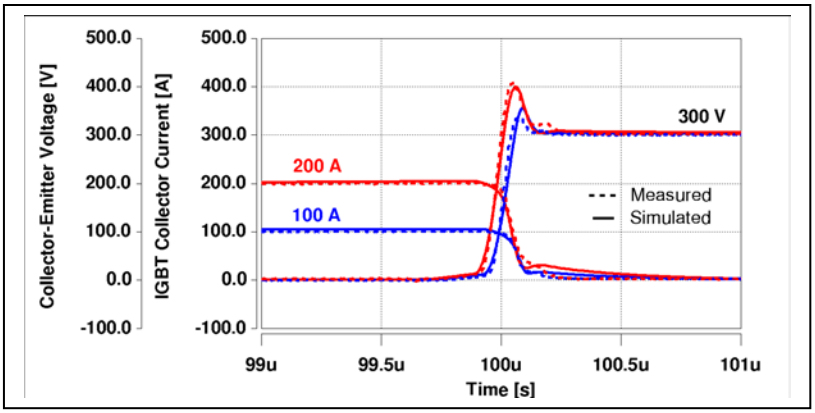

Fig. 5-21 IGBT Turn-off Characteristic Model vs. Measured

5.5.3 Diode Forward Voltage Characteristic

The forward voltage characteristic for the silicon PiN diode over temperature vs. measured is shown in Fig. 5-22. The model accurately captures the voltage dependence over temperature.

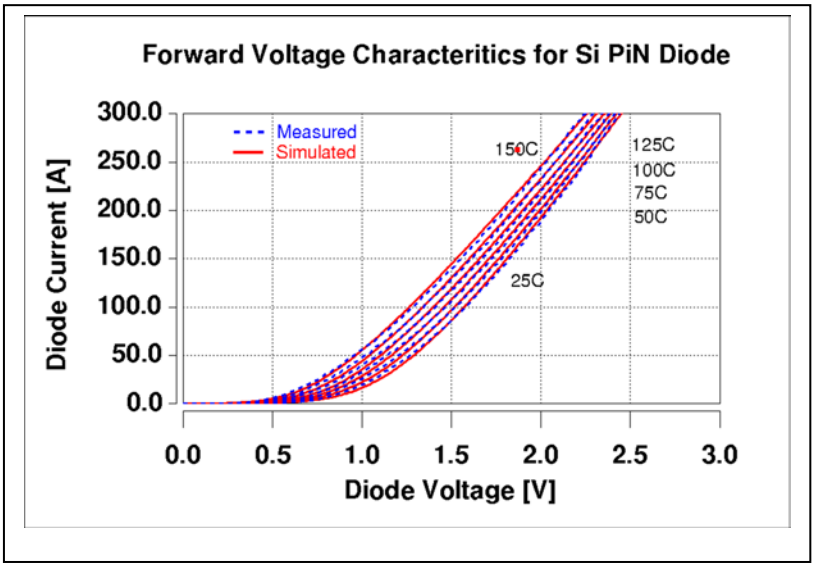

Fig. 5-22 Forward Voltage Characteristics Si PiN Diode Model vs. Measured

5.5.4 Diode Switching Characteristic

The reverse recovery effect of the diode during turn-off has been measured and modeled and is shown in Fig. 5-23.

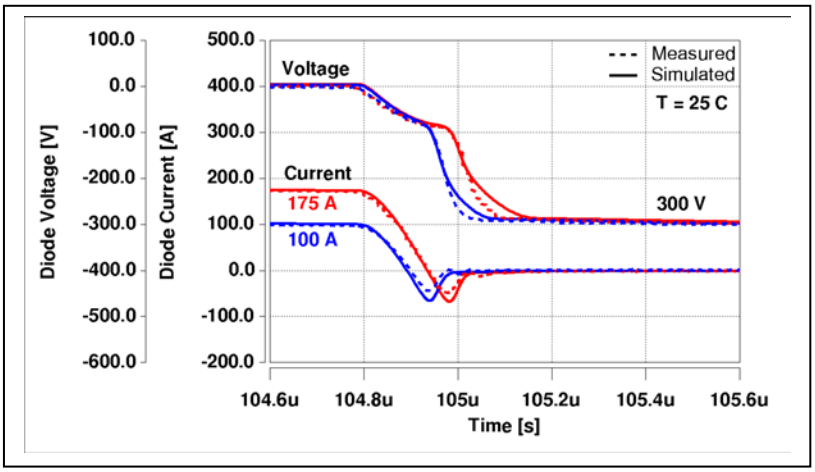

Fig. 5-23 Reverse Recovery Diode Model vs. Measured

5.5.5 CoolMOS Output Characteristic

The output characteristic vs. measurement of the MOSFET at 25 degree C is shown in Fig. 5-24. The output characteristic of the MOSFET at 150 degree C is shown in Fig. 5-25. Good agreement is reach between the model and measurement and shows the model accurately captures the temperature dependence.

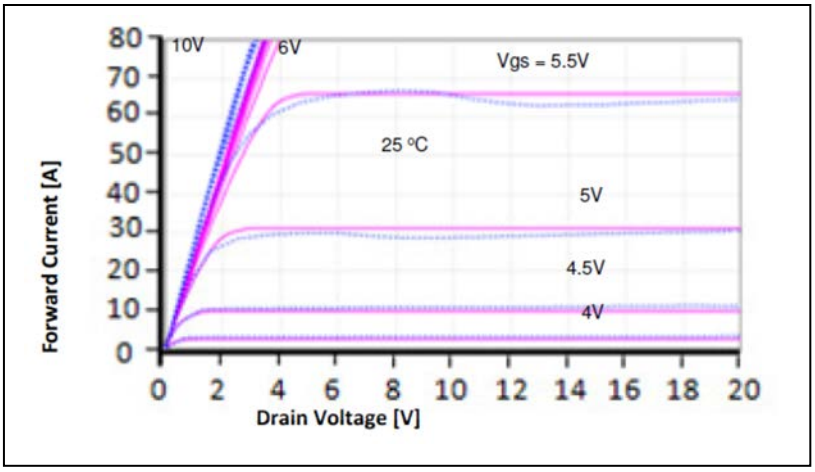

Fig. 5-24 Comparison between measured (dotted) and simulated (solid) 25 degree C [13].

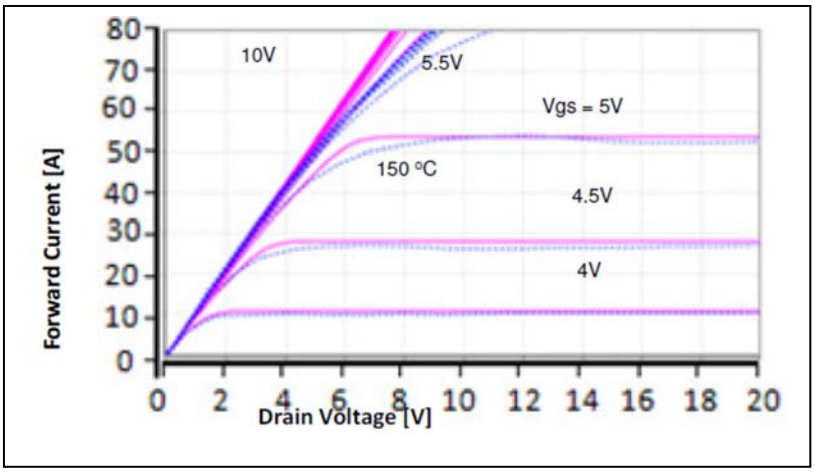

Fig. 5-25 Comparison between measured (dotted) and simulated (solid) 150 degree C [13].

5.5.6 Switching Characteristic MOSFET

The clamped inductive load is used to capture the turn-off characteristic of the MOSFET vs. measured and is shown in Fig. 5-27. Good agreement is reached between the model and measured. Fig. 5-28 shows the nonlinear capacitance associated with CoolMOS accurately in the model.

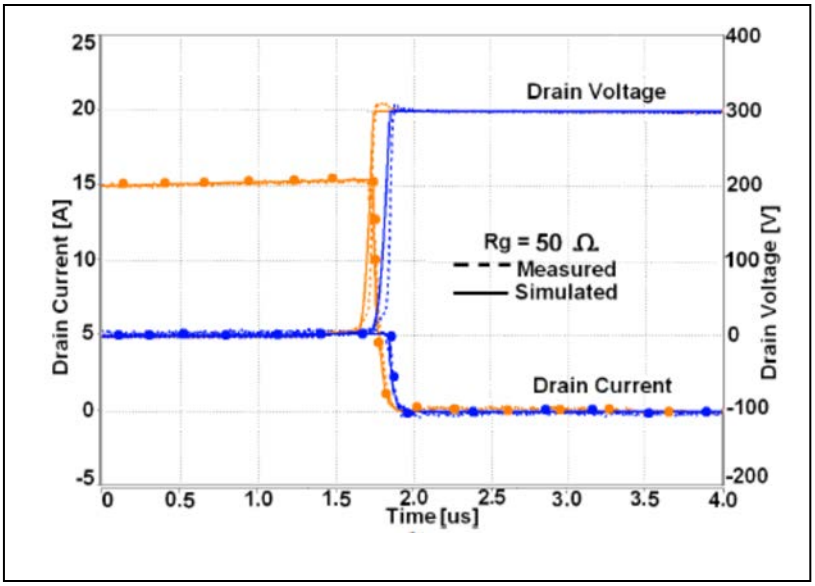

Fig. 5-27 Simulated (solid) and measured (dashed) switching turn-off waveforms 25 Degree C [13].

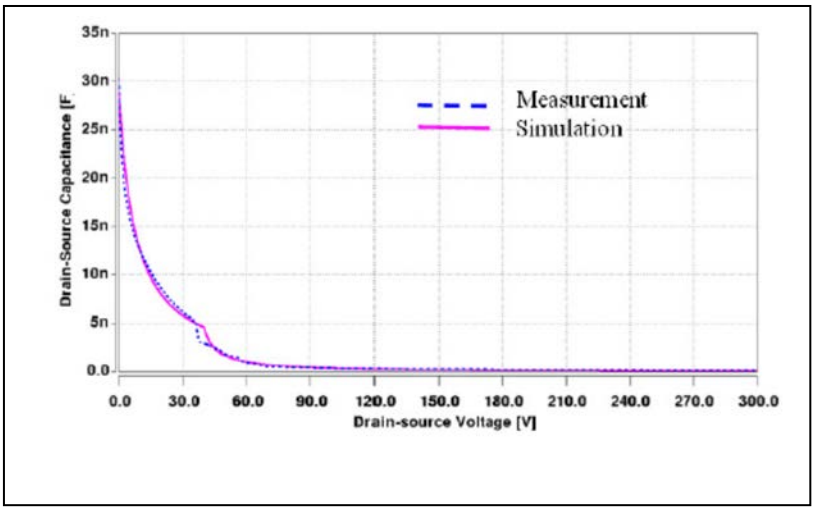

Fig. 5-28 Drain-Source capacitance vs. drain-source voltage 25 Degree C [13].

5.5.7 Hybrid Model Validation

The validated device models from Table 5-4 are used to scale the parameters for the actual devices used in the Generation II power module in Table 5-1. This is done by using the chip area of the validated device model as the reference area, a_{ref}, for the newly scaled IGBT, DIODE, and MOSFET device models. The scaled MOSFET and IGBT models are connected in parallel to create the hybrid switch and the on-state characteristics has been compared against measurement with the result shown in Fig. 5-29 . Fig. 5-29 shows the individual on-state characteristics of the IGBT and MOSFET along with the resulting combined hybrid switch. The agreement is very good indicating device scaling by using the reference chip area parameter works well. This lends itself to parametric study without having to validate new devices during each parametric evaluation during the design optimization process.

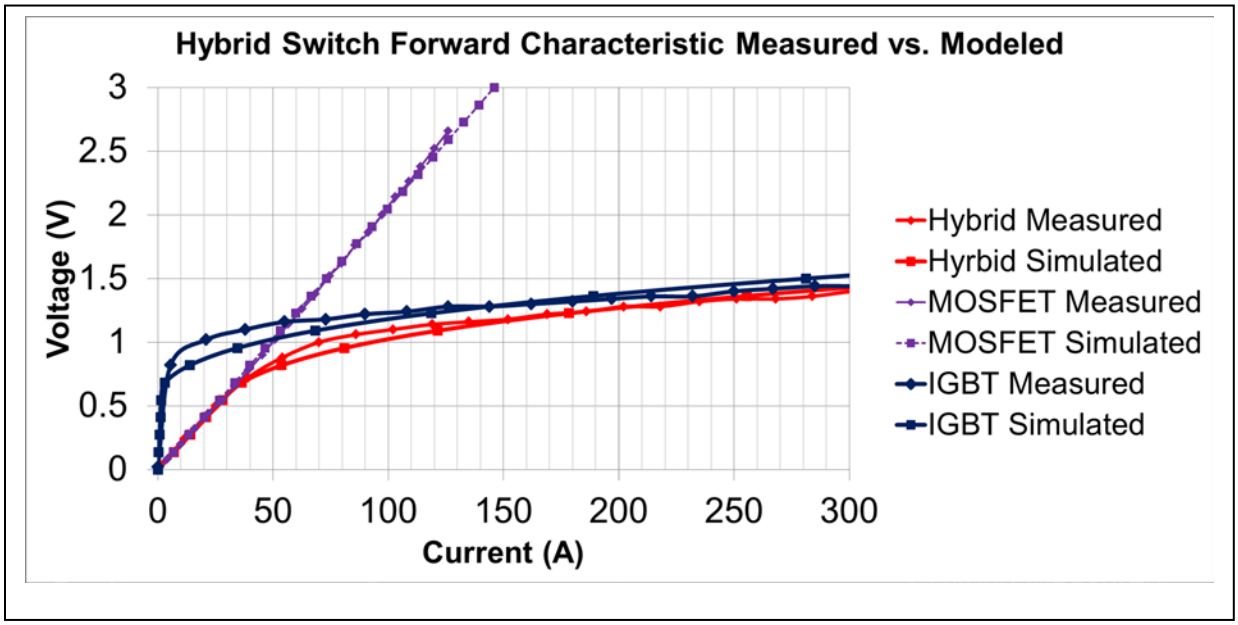

Fig. 5-29 Hyrbid Switch on-state characteristic vs. measurement.

A switching characteristic comparing the device model vs. measurement of the hybrid switch operating under soft switching condition is shown in Fig. 5-30. The hybrid switch device voltage (V_{CE}) is shown with the transformer current (I_{LR}) and device gate voltage (V_{GE}). The parasitic package inductance is evident in the switch device voltage and has been accurately captured in the device model.

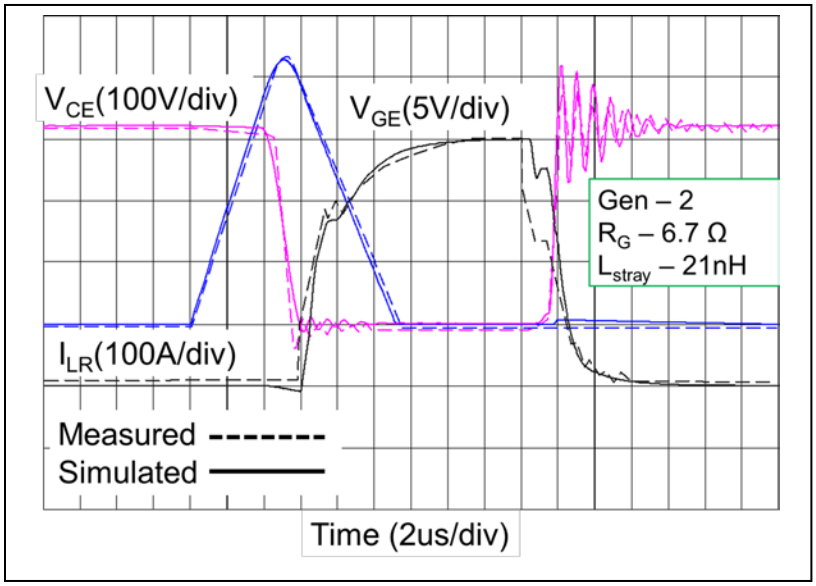

Fig. 5-30 Hybrid Gen II switching characteristic vs. measurement.

Chapter 6 System Simulation

6.1 Introduction

To perform electro-thermal simulations using the SABER® circuit simulator, the compact electro-thermal models for power semiconductors devices are connected to both the electrical and thermal networks. For example, the IGBT electro-thermal model has three electrical terminals (gate, collector, and emitter) and one thermal terminal for the junction temperature. The IGBT electrical terminals are connected to other electrical network components of the inverter, and the thermal terminal is connected to the thermal network component models such as the chip, six-pack module package, and heat sink.

In order to couple the electrical and thermal networks, the IGBT electro-thermal model describes the instantaneous electrical behavior in terms of the instantaneous temperature of the device silicon chip surface T_j (temperature at the device thermal terminal). The temperature dependent electrical model is based upon temperature dependent IGBT model parameters and the temperature dependent physical properties of silicon. The IGBT electro-thermal model also calculates the instantaneous power dissipation that supplies heat to the surface of the silicon chip thermal model through the thermal terminal. The electrical type terminals have units of voltage (V) across the terminals and units of current flowing through the terminals, whereas the thermal terminals have units of temperature (K) across the terminals and units of power (W) flowing through the terminals. Fig. 6-1 shows a diagram of the structure of the electro-thermal semiconductor device models. Self-heating is achieved since the instantaneous junction temperature is being updated at the same time as the temperature dependent device model.

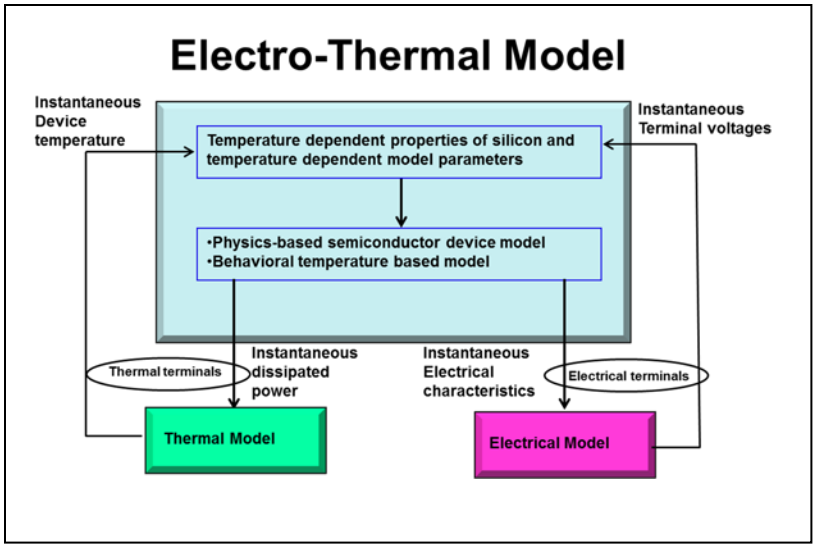

Fig. 6-1 Diagram of the structure of the electro-thermal semiconductor device models

6.2 Inverter Loss Consideration

The major losses in an inverter are due to conduction loss and switching loss. The major switching loss is due to diode reverse recovery induced turn-on loss and IGBT turn-off current induced turn-off loss. Turn-on switching loss due to voltage and current crossover during commutation can be reduced with soft-switching control. The IGBT turn-off loss can result in large instantaneous power dissipation while the tail current is decaying and the IGBT is supporting a large voltage. This large instantaneous turn-off loss can result in device failure in some cases due to a large instantaneous junction temperature. This effect is one of the major motivations behind dynamic electro-thermal modeling. The thermal model proposed in this study can coexist with the physics-based device models in an electrical switching simulation and predict instantaneous junction temperature within a switching cycle. In addition, short-circuit or failure modes can be studied. The electro-thermal model, therefore, becomes a valuable tool to the engineer during the design process and can help aid the engineer in predicting system efficiency and system reliability.

6.2.1 Inverter Average Loss

All thermal models require a power dissipation function. One such manner in which to realize a power dissipation function is to map the device datasheet provided energy curves into power dissipation. However in this case, the resulting loss has been averaged over a switching cycle and therefore can only predict average junction temperature within an inverter line cycle. The datasheet derived conduction loss and switching loss for an inverter averaged over a switching cycle is given by:

$$p_{cond}(t) = \mathrm{I_m}\sin(\omega t)\left[V_t + R_{ce}\left(\mathrm{I_m}\sin(\omega t)\right)^{\beta}\right]\left[0.5 + 0.5M\sin(\omega t + \phi)\right] \tag{6.1}$$

$$p_{sw}(t) = \mathrm{f_{sw}} \bullet \alpha\left(\mathrm{I_m}\sin(\omega t)\right)^{\beta} \tag{6.2}$$

Where the total average loss if averaged over an inverter line cycle is given by:

$$P_{cond-IGBT} = \mathrm{I_m}\, V_t\left(\frac{1}{2\pi} + \frac{1}{8}M\cos\phi\right) + \mathrm{I_m}^{2}\, R_{ce}\left(\frac{1}{8} + \frac{M}{3\pi}\cos\phi\right) \tag{6.3}$$

$$P_{sw-on} = \frac{1}{2\sqrt{\pi}}\, f_{sw}\alpha_{on}\, \mathrm{I_m}^{\beta_{on}} \frac{\Gamma\left(\frac{\beta_{on}+1}{2}\right)}{\Gamma\left(\frac{\beta_{on}}{2}+1\right)} \tag{6.4}$$

$$P_{sw-off} = \frac{1}{2\sqrt{\pi}}\, f_{sw}\alpha_{off}\, \mathrm{I_m}^{\beta_{off}} \frac{\Gamma\left(\frac{\beta_{off}+1}{2}\right)}{\Gamma\left(\frac{\beta_{off}}{2}+1\right)} \tag{6.5}$$

where I_m is the peak output current, V_t is the IGBT fixed voltage drop under zero current condition, R_{ce} is the IGBT on-drop resistance, M is the modulation index, and ϕ is the power factor angle, where k_g is the gate drive stiffness factor, f_{sw} the switching frequency, α and β are the turn-on and turn-off energy coefficients, and V_{dc} and V_{test} represent the dc-bus voltage and

test voltage for switching energy coefficients, respectively. The energy coefficients are readily available from the energy curves given by the IGBT data sheets. Note in using (6.3)-(6.5), only average junction temperature over the entire inverter line cycle can be predicted.

6.2.2 Example Inverter Loss and Junction Temperature Prediction

An example showing the difference in predicted junction temperature when using either (6.1) and (6.2) to predict average junction temperature within a line cycle versus using (6.3)-(6.5) to calculate average junction temperature over the inverter line cycle has been conducted using MATLAB Simulink. The example application is a three phase inverter with the following parameters:

$V_{DC} = 280V$
$F_{sw} = 10kHz$
$P_o = 55 - kW$ Three Phase
$PF = 0.83$

An IGBT with the following device parameters has been chosen for the main inverter switching device:

IGBT CM400DY-12NF
Device Parameters:
$Vt = 0.983$
$Rce = 0.00182$
$\alpha_{on} = 0.0355$
$\alpha_{off} = 0.0444$
$\beta_{on} = 0.9325$
$\beta_{off} = 0.9918$

The IGBT is assumed to be a square silicon chip 0.245 x 0.245 x 0.01 in centered on an ALN substrate measuring 0.25 x 0.25 x 0.025in mounted on a 0.3 x 0.3 x 0.05 in copper package

baseplate. The transistor is attached to the substrate with 0.002 in solder and the substrate attach material is also solder 0.002 in thick.

The thermal network for this example problem is calculated using the effective heat flow area approach as outline in Chapter 4. The following effective heat flow area, thermal resistances, and thermal capacitances for the nodes within the thermal circuit are calculated and tabulated in Table 6-1.

Table 6-1Thermal Network for example problem

Area	silicon	Network		Area	Aln	Network		Area	Copper	Network	
0.372		rh1	0.004	0.384		rh1	0.008	0.429		rh1	0.008
	node1	c1	0.003		node1	c1	0.017		node1	c1	0.038
0.372		r12	0.009	0.396		r12	0.015	0.484		r12	0.014
	node2	c2	0.003		node2	c2	0.017		node2	c2	0.043
0.372		r23	0.009	0.396		r23	0.015	0.543		r23	0.012
	node3	c3	0.003		node3	c3	0.017		node3	c3	0.048
0.372		r34	0.009	0.396		r34	0.015	0.543		r34	0.012
	nod4	c4	0.003		nod4	c4	0.017		nod4	c4	0.048
0.372		r45	0.009	0.396		r45	0.015	0.543		r45	0.012
	node5	c5	0.003		node5	c5	0.017		node5	c5	0.048
0.372		r5c	0.028	0.396		r5c	0.03	0.543		r5c	0.007

Note that the heat flow area increase with depth into package. Fig. 6-2 shows the thermal result using the different loss calculations. It is clear that including the inverter line cycle variation in the power dissipation function using (6.1) and (6.2) gives much more information on the actual variation of the junction temperature within an inverter line cycle as compared to just using the overall average dissipation function.

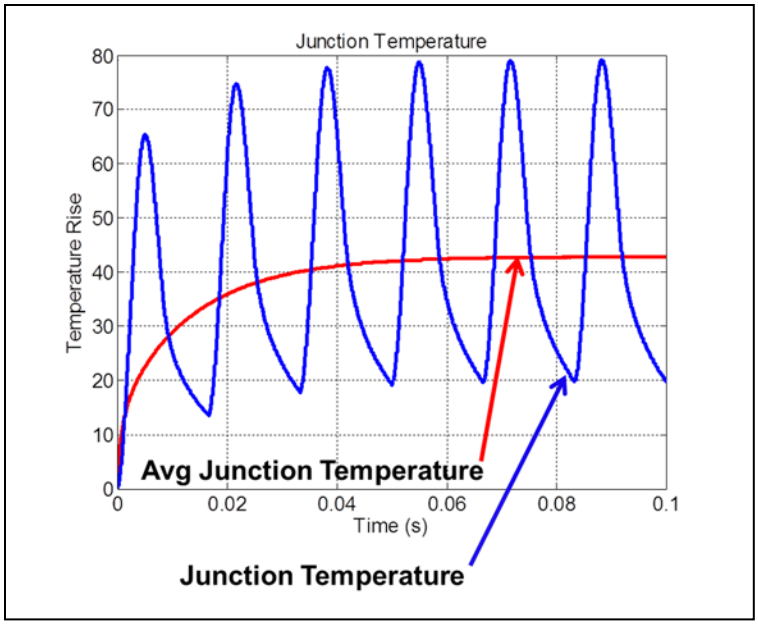

Fig. 6-2 Junction Temperature Prediction.

There is almost a 30 degree difference in junction temperature between the two methods. Important junction temperature variation can be missed.

6.2.3 Inverter Instantaneous Power Dissipation

The physics-based models that can calculate instantaneous dissipated power allow junction temperature rise prediction within a switching cycle. This allows for high frequency effects such as loss dissipated due to hard switching or short circuit condition to be included in the model. Referring to Fig. 6-3, typical instantaneous power is calculated by multiplying the voltage across a device and the current through a device. This is an invalid assumption and is common in literature. The result of this multiplication does not necessarily represent loss that is dissipated. For example, soft-switching condition circulates energy in the parasitic capacitance with external resonant elements of the circuit and is never dissipated as heat within the device.

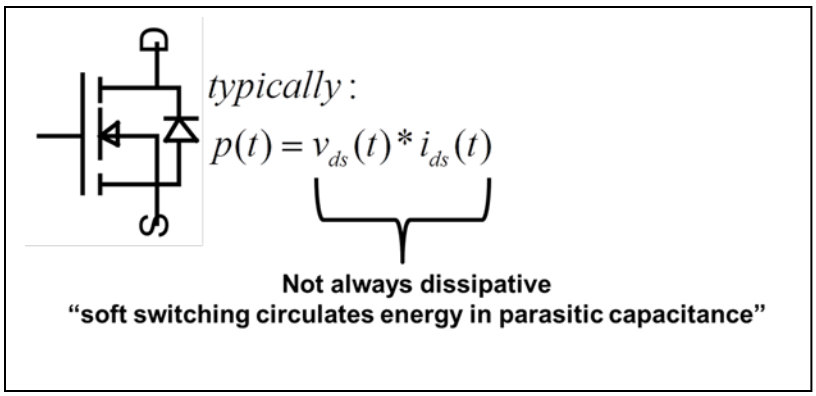

Fig. 6-3 Instantaneous Power Calculation Misconception.

An example of the instantaneous energy and dissipated power profile for a hard switching inverter condition using a physics-based device model which properly calculates dissipated power and applying to the thermal network based on the effective heat flow approach is shown in Fig. 6-4.

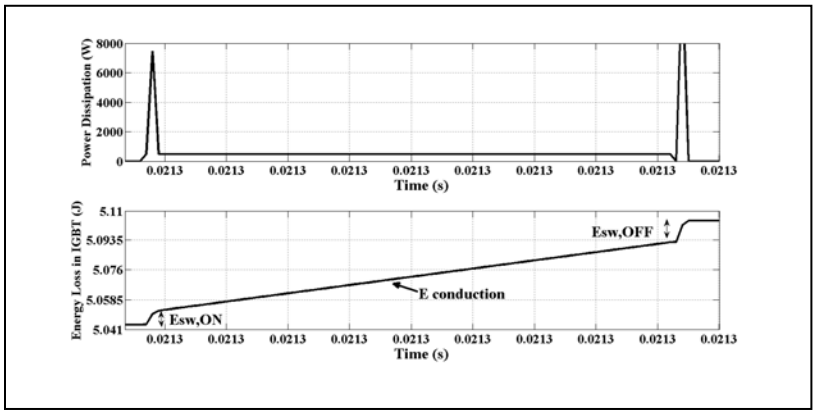

Fig. 6-4 Loss profile applied to FDM model. Power (top) and energy (bottom).

The result in Fig. 6-4 shows the effect of switching loss on instantaneous power dissipation. Large spikes result at both turn-on and turn-off which can lead to large junction temperature spikes.

Chapter 7 Design Problem

7.1 Design Variables/Inputs

The circuit in in Fig. 3-1 represents a single phase module operating in a three phase system (i.e. three modules total). Each semiconductor device within the circuit should have a suitable electro-thermal model with parameters that have been extracted over temperature. Validation of an individual device model with a given set of parameters allows for parametric studies to be performed for certain scalable parameters. One such scalable parameter that this paper considers is the device chip area. The device chip area of a known validated device model becomes the "reference" chip area for a new device model assuming a similar fabrication process. In this manner parametric studies of the affects that the device chip has on the overall device loss can be considered without requiring a new device fabrication and model validation. This allows for design optimization with reduced design cycle cost.

The design variables considered for the optimum design of the soft-switching module are shown in Table 7-1. Table 7-2 shows the design inputs for the soft-switching inverter design. For this study, the auxiliary IGBT chip area is chosen as a fixed value. The designer has flexibility of course in choosing the design variables and inputs depending on the specific design goal.

Table 7-1 Design Variables

Design Variable	Independent Variable	Symbol
IGBT chip die area	Yes	A_q
MOSFET chip die area	Yes	A_m
Diode chip area	No	A_{diode}
Resonant capacitor	Yes	C_{res}
Transformer primary leakage	No	$L_{lk\text{-}pri}$
Convection Coefficient	Yes	h_c

Table 7-2 Design Inputs

Design Inputs	Symbol	Value
Bus voltage	V_{dc}	280 V
Power	*Power*	61 kW
Power factor	*pf*	0.83
Output voltage	V_{out}	80 V_{rms}
Auxiliary IGBT chip die area	A_{aux}	1.16 cm^2
Sine-triangle SPWM frequency	f_{sw}	20 kHz
Max Junction temperature	$T_{operating}$	90°C
Transformer magnetizing inductance	L_M	293 uH
Total Device Area	A_{max}	5.72 cm^2
Primary turns for coupled magnetic	N_1	14
Secondary turns for coupled magnetics	N_2	19
Cooling Temperature	T_α	30°C
IGBT gate resistance	R_G	6.7 Ω
Stray Inductance	L_{stray}	21 nH

7.2 Design Optimization flow

The design objective is to minimize the total device loss and stress of the coupled-magnetic type soft-switching inverter under a certain max junction operating temperature, $T_{operating}$. This is achieved by using the chip area of the IGBT, MOSFET and diode along with the turn-off snubber capacitor to minimize the total conduction and switching loss. This objective function is subject to two design constraints; the maximum chip area and the minimum on-time condition.

Once the design has been optimized for a particular max operating junction temperature, the cooling requirements can be derived such that the optimized design operates at the junction temperature assumed during the optimization process. The average loss over an inverter line cycle from the optimized design is calculated and used as an input to the thermal model. The baseplate convection coefficient is then adjusted until the max device temperature is reached. This minimizes the required convection coefficient which in turn translates to improved cooling requirements at lower cost.

Fig. 7-1 shows the design flow for the design optimization.

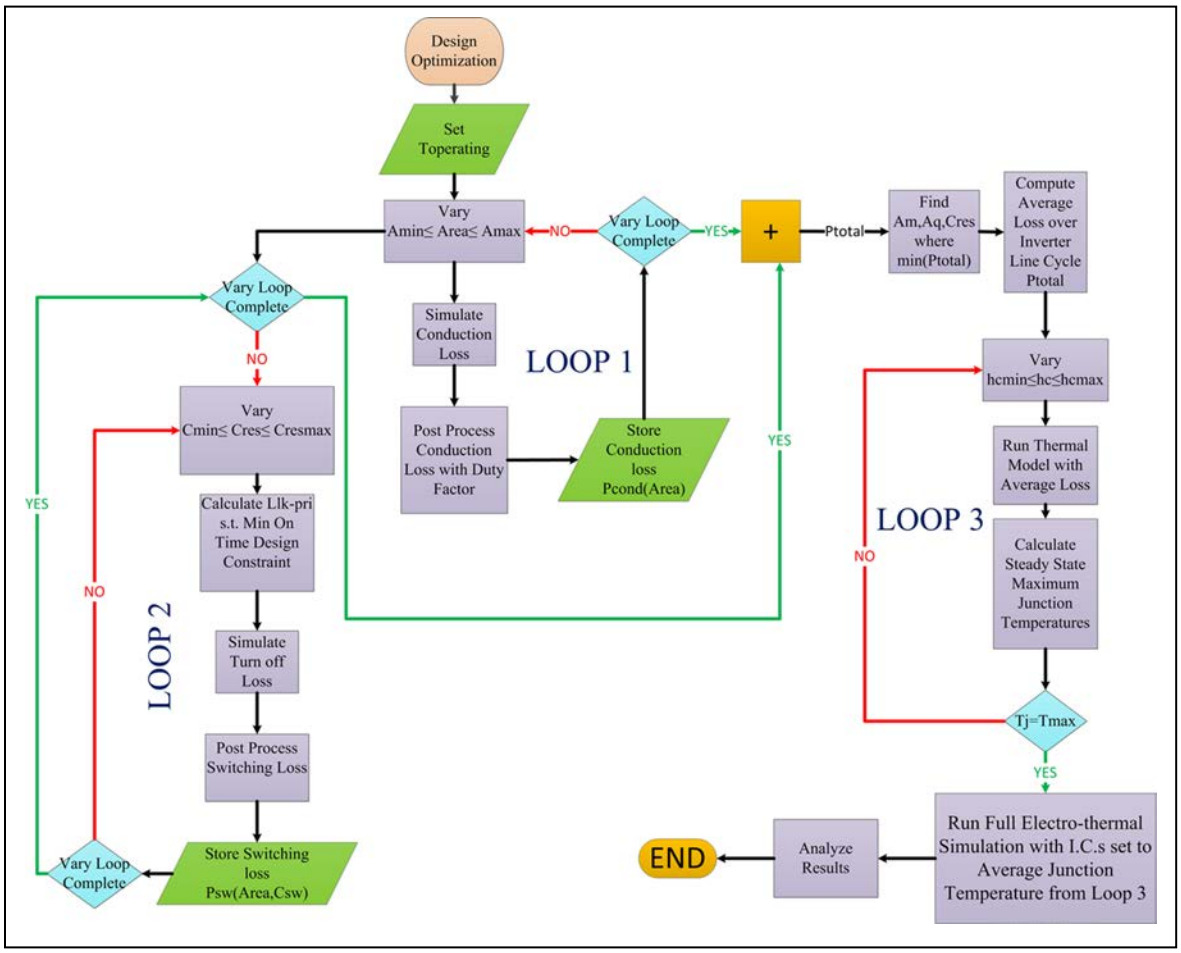

Fig. 7-1 Optimization Process for Hybrid Switch Soft-switching Inverter

A multi-scale simulation approach using three simulation loops is proposed to maximize design time and simulation time. For example calculating conduction loss does not require a switching simulation. And by the same argument, calculating switching loss does not require an entire pulse width modulated (PWM) simulation. And minimizing the convection coefficient only requires a thermal model where the input is the average dissipated power over an inverter line cycle. Each loop is optimized for simulation time allowing the entire optimization process to conclude in minutes rather than hours.

7.2.1 Loop 1 – Conduction Loss Calculation

The first loop is used to calculate the conduction loss. The chip areas for the MOSFET, IGBT, and DIODE are varied under the defined operating junction temperature. This is done by using the area scaling parameter, *a_ref*, within the Hefner IGBT model. The chip area of the known validated device model becomes the reference area. The user then only needs to set the device active area parameter, *a*, to the new desired area and the device model will scale the new model appropriately based on the reference chip area. The reference MOSFET area for the Gen-2 module is 1.14 cm^2. The reference main IGBT area is 2.88 cm^2 while the auxiliary IGBT area is 1.16 cm^2. The reference area for the silicon Diode is 1.7 cm^2.

To perform the parametric study for calculating conduction loss, the following simulation is used.

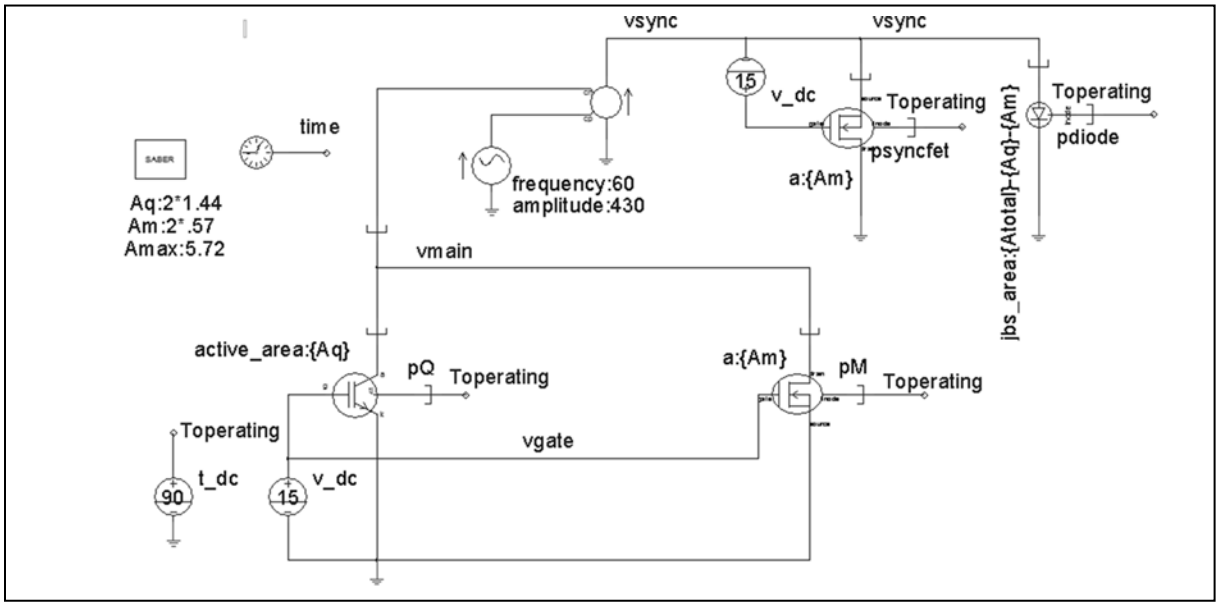

Fig. 7-2 Test Circuit for Calculating Conduction Loss

Shown in the simulation is the main hybrid switch made up of a CoolMOS MOSFET electro-thermal model and in parallel with an IGBT electro-thermal model. In addition, the devices used

for conducting during the free-wheel period are modeled and consist of the CoolMOS MOSFET in parallel with silicon DIODE. The device areas are given parameter names A_q for the IGBT, A_m for the MOSFET and A_{diode} for the Diode. Each device is a four terminal device. Three of the terminals connect to the electrical circuit and the fourth terminal is the thermal terminal and represents the junction temperature of the device. This terminal has the dissipated power as a through variable and temperature defined as the across variable. The terminal connects to the thermal model. For the Loop 1 analysis the thermal terminal connects to a constant temperature source which keeps the junction temperature constant at 90 degree C. A thermal network will be connected after the design optimization is complete during Loop 3 where the heat flow convection coefficient will be varied until 90 degree C is observed at the junction.

A sine wave current source depicting the inverter load current is used to flow through the hybrid switch biased on with a gate drive voltage of 15V to generate the on-state dissipated power. This represents the current which is conducting through the hybrid switch during the main conduction period. The current source also flows through another CoolMOS MOSFET model in parallel with a silicon DIODE. These models represent the devices which conduct current during the free wheel portion of the inverter load current. The total conduction loss is determined from the loss that incurs as a result of main conduction and the loss that is incurred during the free wheel portions of the conduction cycle. The IGBT is not required for the free wheel portion since it cannot conduct current in the other direction. Thus the number of models the simulation has to calculate is minimized thus optimizing simulation speed. The device dissipated powers are designated p_Q, p_M, $p_{syncfet}$, and p_{diode}. The junction temperature represented by the fourth terminal on the device model is connected to a fixed temperature $T_{operating}$ representing the desired max junction temperature for which the design is to be optimized.

In this study the assumption is made to constrain the total hybrid device die area, A_{max}, to an input set by the designer. This allows the designer to determine how much of the total switch area should be made up of IGBT, MOSFET or DIODE to result in the smallest overall device loss. With the MOSFET area and IGBT areas defined as design variables, and given the total device area, the diode area is calculated from the following design constraint.

$$A_{\max} = A_{diode} + A_q + A_m \tag{7.1}$$

The design space for the MOSFET and IGBT chip areas are determined from the input A_{max}. An algorithm shown in (7.2) is used to sweep the IGBT and MOSFET chip areas parametrically and adjusting the areas accordingly as to not exceed the maximum chip area A_{max}.

$$\begin{aligned}
&\text{Vary } A_m : 0 \to A_{\max} \\
&\text{Vary } A_Q : 0 \to A_{\max} \\
&\text{if}\,(A_m + A_q \geq A_{\max})\{ \\
&\qquad \text{if}(A_m \geq A_q)\{ \\
&\qquad\quad A_m = A_m \\
&\qquad\quad A_q = \max(0, A_{\max} - A_m) \\
&\qquad \text{else} \\
&\qquad\quad A_q = A_q \\
&\qquad\quad A_m = \max(0, A_{\max} - A_q) \\
&\qquad\qquad\quad \} \\
&\quad \}
\end{aligned} \tag{7.2}$$

Fig. 7-3 shows design space of the IGBT and MOSFET chip areas as a result of the algorithm in (7.2). The conduction loss simulation is for each design within the design space.

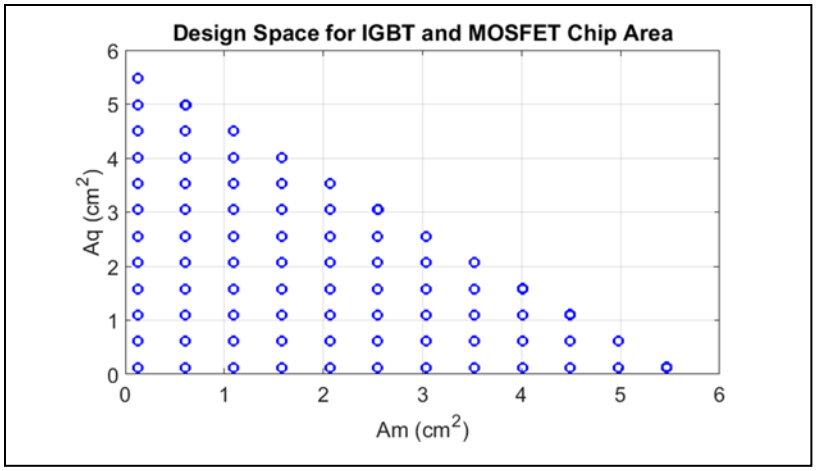

Fig. 7-3 Design Space for IGBT and MOSFET chip Area

The total conduction loss of the hybrid switch is driven by the overall on-state characteristic of the hybrid switch comprising the IGBT and MOSFET and the on-state characteristic of the freewheel devices comprising of the MOSFET, operating under synchronous conduction, and the parallel silicon diode.

The conduction losses for the main and free-wheel cycles are determined from the simulation. The on-state voltage resulting from main conduction period, v_{main}, is determined from models biased with a current source representing the inverter load current. The on-state voltage that results from the free-wheel conduction period, v_{sync}, is also determined from models biased with a current source representing the inverter load current. The resulting on-state voltages from the simulation are post processed to take into account the duty cycle variation that would occur in a pulsed width modulated simulation and are given by:

$$P_{c-main} = \frac{1}{2\pi}\int_{0}^{\pi} \underbrace{v_{main}(t) I_{peak} \sin(\omega t)}_{p_Q + p_M} \left[0.5 + 0.5M \sin(\omega t + \phi)\right] d\omega t \tag{7.3}$$

$$P_{c-free-wheel} = \frac{1}{2\pi}\int_{\pi}^{2\pi} \underbrace{v_{sync}(t) I_{peak} \sin(\omega t)}_{psyncfet + pdiode} \left[0.5 - 0.5M \sin(\omega t + \phi)\right] d\omega t \tag{7.4}$$

Where I_{peak} is the peak load current, M is the modulation index, and ϕ is the phase shift due to power factor. Note that in (7.3) and (7.4) the resulting on-sate drops multiplied by the current source should be equal to the simulated dissipated powers p_Q, p_M, $p_{syncfet}$,and p_{diode} because in this case all the power is dissipated in the device.

Post processing the on-state voltages in this manner results in a much faster simulation for optimization study since switching of the device models is not necessary to study the optimum conduction loss. The total conduction loss is the sum of (7.3) and (7.4)

$$P_{cond}(\mathrm{A}_Q, \mathrm{A}_\mathrm{m}) = P_{c-main}(\mathrm{A}_Q, \mathrm{A}_\mathrm{m}) + P_{c-freewheel}(\mathrm{A}_Q, \mathrm{A}_\mathrm{m}) \tag{7.5}$$

Fig. 7-4 shows the simulation result of the instantaneous loss for the IGBT and MOSFET ,(p_Q+p_M), for a half inverter conduction cycle and the MOSFET operating under synchronous conduction in parallel with free wheel DIODE ,($p_{syncfet}$,+ p_{diode}), calculated at each chip area within the design space . Clearly there is significant loss depending on the chip area configuration thus validating the need for an optimal design set. The waveforms shown in Fig. 7-4 are post processed based on (7.3) and (7.4).

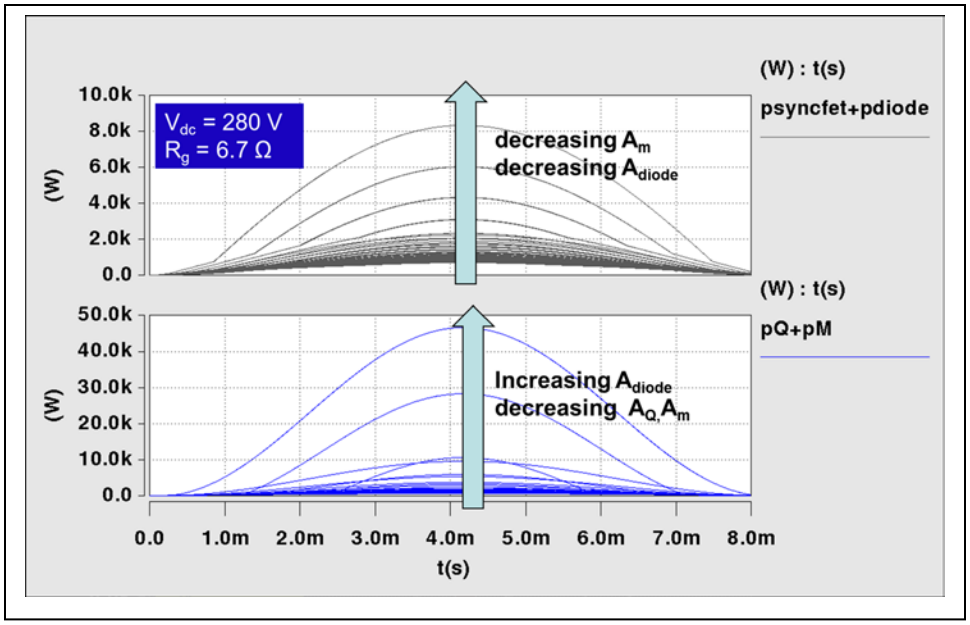

Fig. 7-4 Simulated Instantaneous Conduction Loss within chip Area Design Space

7.3 Loop 2 Switching Loss Calculation

Soft-switching allows for the reduction of turn-on loss by aligning the main switch with zero volts prior to turn-on. However turn-off loss can still be significant due to the IGBT turn-off tail. And this loss is very dominant especially at higher temperatures where the loss associated with IGBT turn-off tail is increased. There are several ways to reduce the turn-off loss. One method is to introduce a snubber capacitor which provides an alternate current path so that the IGBT anode voltage rise is slowed, thus resulting in reduced turn-off loss.

In addition, since a hybrid switch is being used, the IGBT can be turned off earlier than the MOSFET so that the IGBT turn-off tail current induced loss is minimized. This is assuming that the MOSFET has been adequately sized to support the full load during this time. The delay between the MOSFET and IGBT turn-off is the design variable, T_{doff}, which is determined from a design constraint discussed a little later. The simulation calculates this delay accordingly at the

beginning of each parametric simulation run and is a function of the resonant capacitor and resonant inductor.

Loop 2 determines the turn-off switching loss using a different simulation test circuit shown in Fig. 7-5.

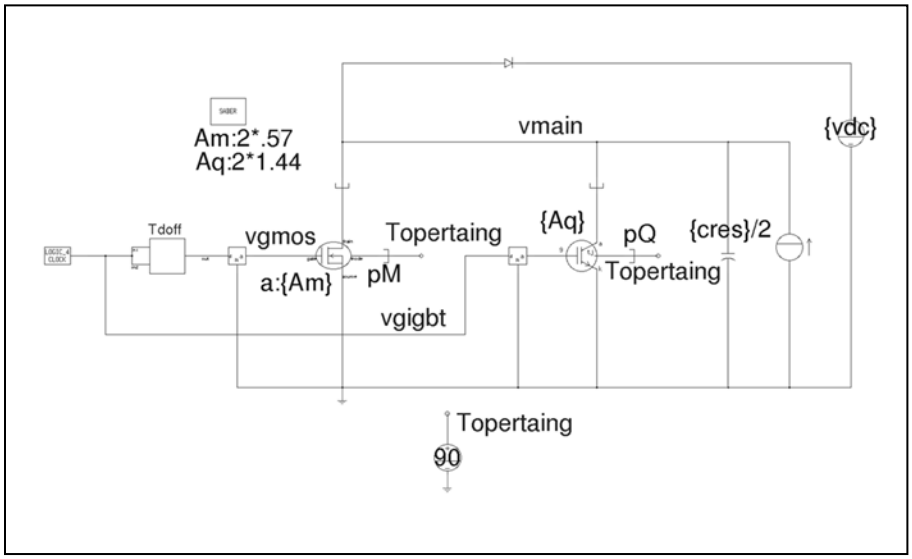

Fig. 7-5 Test Circuit for Calculating Switching Loss

The chip area is still varied in the same manner as Loop 1. However the resonant snubber capacitor is also varied along with load current from zero to full load. The devices are biased with constant current at time zero. The gate drive for the IGBT is removed at time zero followed by the removal of the MOSFET after a time delay, T_{doff} . The dissipated powers, *pM* and *pQ*, are integrated to determine the switching energy vs. load current relationships for each resonant snubber capacitor. The required simulation time, t_f, can be very short (<4us) such that all the parametric sweeps including chip Area, snubber capacitor, and load current can finish in minutes. The switching energy is fit to a fourth order polynomial during the post processing. Starting with the integration of the dissipated power to determine the turn-off energy:

$$E_{off}\Big|_{A_m, A_q, c_{res}, I_{load}} = \int_0^{t_f} \underbrace{p(t)}_{pQ,\, pM}\, dt \tag{7.6}$$

The energy is calculated at each load current to develop the energy vs. load current, I_{load}, relationship for each resonant snubber capacitor configuration. Fig. 7-6 shows the resultant turn-off energy for the MOSFET over the entire design space for chip area at a given resonant snubber capacitor. Note in Fig. 7-6 the turn-off energy is a result of the MOSFET turning off prior to the IGBT and having to handle the entire load current. The energy during this time is due mostly to conduction for that time interval. For every chip area within the design space and resonant capacitor, an energy vs. current curve is generated. Fig. 7-7 shows the energy vs. current relationship over the chip area design space for the IGBT. In this case the energy is due to the carriers having to recombine in the IGBT resulting in tail current induced loss.

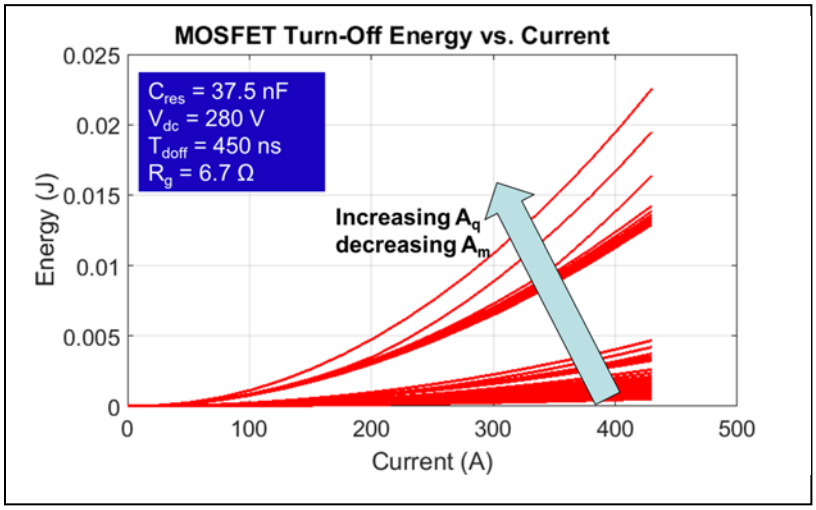

Fig. 7-6 MOSFET Turn-off Energy vs. Current evaluated within chip Area Design Space

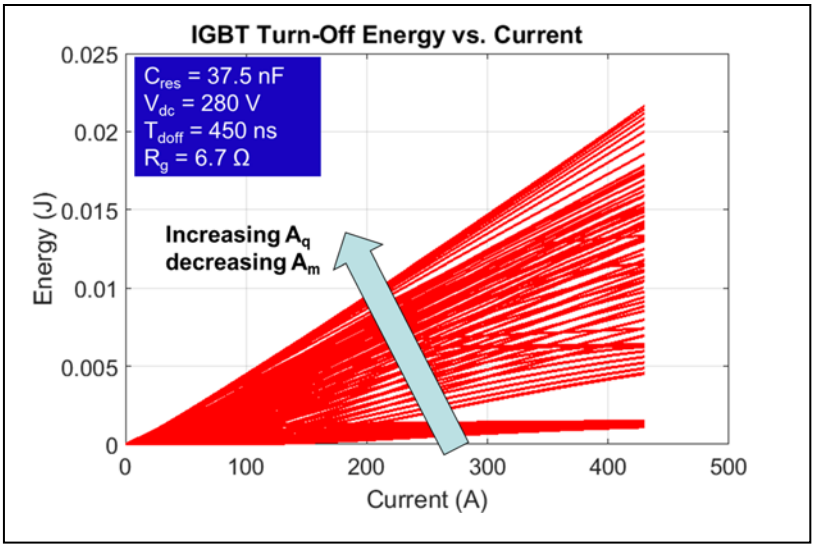

Fig. 7-7 IGBT Turn-off Energy vs. Current evaluated within chip Area Design Space

Each curve generated in Fig. 7-6 and Fig. 7-7 can be approximated with a fourth-order polynomial:

$$E_{off} = a_4 Ioad^4 + a_3 Ioad^3 + a_2 Ioad^2 + a_1 Ioad^1 + a_0 \tag{7.7}$$

Where the coefficients a_0-a_4 are determined from curve fitting algorithm. The average dissipated loss of the main switch under inverter operation can be determined from the following:

$$P_{sw-main} = \frac{1}{2\pi}\int_0^{\pi} f_{sw}\begin{pmatrix} a_4\left(I_{o\max}\sin\omega t\right)^4 + a_3\left(I_{o\max}\sin\omega t\right)^3 \\ +a_2\left(I_{o\max}\sin\omega t\right)^2 + a_1\left(I_{o\max}\sin\omega t\right)^1 + a_0 \end{pmatrix} d\omega t \tag{7.8}$$

Where I_m is the peak inverter load current. The integral in (7.8) is evaluated using a trapezoidal numerical integration approximation during the post processing. The total switching loss for the post processing tool also includes the loss induced in the auxiliary switch during turn-on. The total switching loss is given by:

$$P_{swtotal}(A_m, A_q, C_{res}) = P_{sw-main}(A_m, A_q, C_{res}) + P_{sw-aux}(C_{res}) \tag{7.9}$$

Where $P_{sw\text{-}aux}$ is discussed a little later.

During the vary loop of Loop 2 two design constraints need to be satisfied when considering the resonant capacitor. They are discussed below.

7.3.1 Design Constraint – Transformer Reset Time- T_{doff}

The transformer must be reset every switching period. This is achieved by ensuring proper voltage-second balance of the transformer magnetizing inductance. The worst case reset time required for the coupled magnetics is under the maximum load current I_{omax} and minimum dc-link voltage V_{dcmin} and is given by (7.10):

$$T_{R\max} = \frac{L_m + L_r}{L_m}\frac{N_1}{N_1 + N_2} \times \left\{ \begin{array}{l} \frac{L_r}{Z_r}\left[\pi - \cos^{-1}\left(\frac{N_1}{N_2}\right) + \left(\frac{N_2}{N_1}\right)\sqrt{1-\left(\frac{N_1}{N_2}\right)^2} \right] \\ + \frac{L_r}{V_{dc\min} / I_{o\max}}\left(2 + \frac{N_1}{N_2} + \frac{N_2}{N_1}\right) \end{array} \right\} \tag{7.10}$$

Where:

$$Z_r = \sqrt{\frac{L_r}{(2C_{res})}} \tag{7.11}$$

$$L_r = 2L_{lk-pri}\left(\frac{N_2 / N_1}{1 + N_2 / N_1}\right)^2 \tag{7.12}$$

L_m is the transformer magnetizing inductance and I_{omax} is the maximum peak load current.

In order for this reset time to be achieved and reset every PWM switching cycle, a fixed turn-off delay time between the main switch and the auxiliary switch is required to be larger than the constant T_{Rmax}, thus the design constraint:

$$T_{doff} \geq T_{R\max} \tag{7.13}$$

A gate drive timing diagram is shown in Fig. 7-8 shows the gate drive timing taking into account the design constraint(7.13). Also shown in Fig. 7-8 is the instantaneous dissipated power

result from the Loop 2 simulation. The time delay between the turn-off of the IGBT and MOSFET increases the MOSFET turn-off loss since the MOSFET takes the full load current. Also shown is the current bump in the IGBT waveform. Since the T_{doff} delay already exists to satisfy the transformer reset condition, the designer can use this delay to turn the IGBT off prior to turning off the MOSFET. The idea is to reduce the IGBT turn-off tail current induced loss. The IGBT is turned off at the same time the auxiliary switch is turned off. The turn-off delay results in a zero-current window and is similar to the one described in [47] for zero-current turn-off soft-switching schemes. The zero-current window refers to the time duration between the time the anode current is removed from the IGBT and the time when voltage is applied to the IGBT. In the scheme depicted in Fig. 7-8, anode current is interrupted in the IGBT when the IGBT gate is turned off and current is transferred entirely to the MOSFET. Voltage will not be applied to the IGBT until the MOSFET is turned off. This results in a large tail-current bump if the carriers in the IGBT have not had time to fully recombine. The current-tail bump is larger for narrower time durations of T_{doff}, and also larger for higher temperatures.

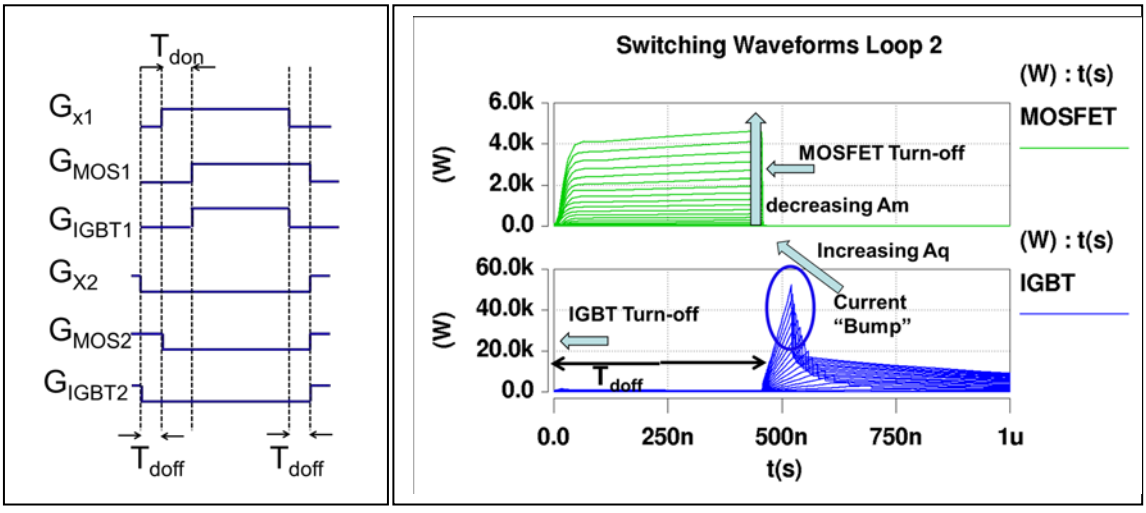

Fig. 7-8 (a) Gate drive timing diagram (b) Loop 2 Simulation Result

7.3.2 Gate Resistance

In a hard switching application where an IGBT is used, the gate drive resistance has a big impact on the device switching loss at turn-on and turn-off. Losses in the channel during the switching edges are dependent on how fast the device can switch on and off, typically described in datasheets by the parameters t_{on} and t_{off}. As it relates to switching loss, a fast turn-on and turn-off time is desired to reduce the cross over loss at the switch edges. This is accomplished by reducing the gate resistance which results in an increased drive capability. However, decreasing the gate resistance has consequences on other circuit performance criteria such as EMI and voltage stress. Switching very fast increases the *dv/dt* and *di/dt* in the circuit. An increased *dv/dt* in the circuit causes EMI challenges in the system. And an increased *di/dt* results in voltage stress on the IGBT at turn-off due to stray inductances in the circuit layout. In addition, an increased *di/dt* also results in larger reverse recovery induced loss in the IGBT from the free-wheeling diode. In addition to increasing the switching losses, an increased gate resistance also can lead to a potential shoot thru condition between the top and lower device of an inverter bridge. The increased fall time may be longer than the programed dead time between the upper and lower device, resulting in a short circuit condition. Increasing the dead time to accommodate a longer fall time is not practical as this affects the maximum duty cycle of the converter. So in summary, if considering a hard switching application, a gate resistance is added to improve EMI, reduce voltage stress on the main switch at turn-off and reduce reverse recovery induced loss in the main switch from the free-wheel diode.

The hybrid switch soft-switching inverter in this dissertation operates under soft-switch condition during turn-on. Therefore the turn-on loss is approximately zero. The only switching loss is due to turn-off loss. Resonant snubber capacitors connected across the hybrid switch slow

down the device voltage slew rate, reducing the turn-off loss. In addition the gate drive delay, T_{doff}, is added so the IGBT turn-off tail current induced loss is minimized [3].

The hybrid switch of the Gen II module includes a gate drive resistance, R_G in Fig. 3-1, for the main IGBT measured at approximately 6.7 Ω. Due to the soft-switching operation of the inverter, the switching edges are "soft" due to the resonant transition removing the EMI problems associated with hard switching applications. The *di/dt* is still a concern for voltage stresses on the hybrid switch as a result of the stray inductance in the circuit. The stray inductance, L_{stray}, for the Gen II module is measured to approximately 21 nh. Fig. 5-30 shows the switching characteristic of the Gen II module vs. measured using the measured gate drive resistance and stray inductance measured. The voltage stresses seen on the main hybrid switch were well below the voltage rating (600V) of the device. And since the inverter is operating under soft-switching condition, the free-wheel diode current is diverted to the opposite-side diode before the opposite switch is turned on; therefore, the reverse recovery is no longer an issue [3]. Therefore the only reason to add a gate resistance in a hybrid soft-switching inverter is to reduce voltage stress seen on the main switch. Having a very good layout reduces the stray inductance resulting in a minimized gate resistance.

To study the impact of the gate resistance on the hybrid soft-switching inverter, two experiments are run using the switching circuit used for Loop 2. First, the turn-off energy is calculated as a function of gate resistance from 0-10 Ω for several designs within the chip area design space. The curves represent constant hybrid switch area such that increasing the IGBT chip area for example results in a reduced MOSFET area such that the total hybrid switch area is kept constant. The snubber capacitor, C_{res}, is fixed at 37.5 nF and the current in the switch prior to turn-off is 430 A. The fixed timing delay, T_{doff}, is fixed at 450 ns. The bus voltage is fixed to

250V. Fig. 7-9 shows the result for the hybrid switch condition. The impact of the turn-off energy as function of gate resistance is not as significant as that of a hard switching application. The reason is the turn-off loss has been minimized already by the snubber capacitor and gate drive timing delay scheme as discussed earlier. The design space where mostly MOSFET is used (green), the gate drive resistance does not make a difference since the IGBT is essentially out of the circuit and the MOSFET does not use a gate resistance. The turn-off energy in all cases for the MOSFET is almost negligible.

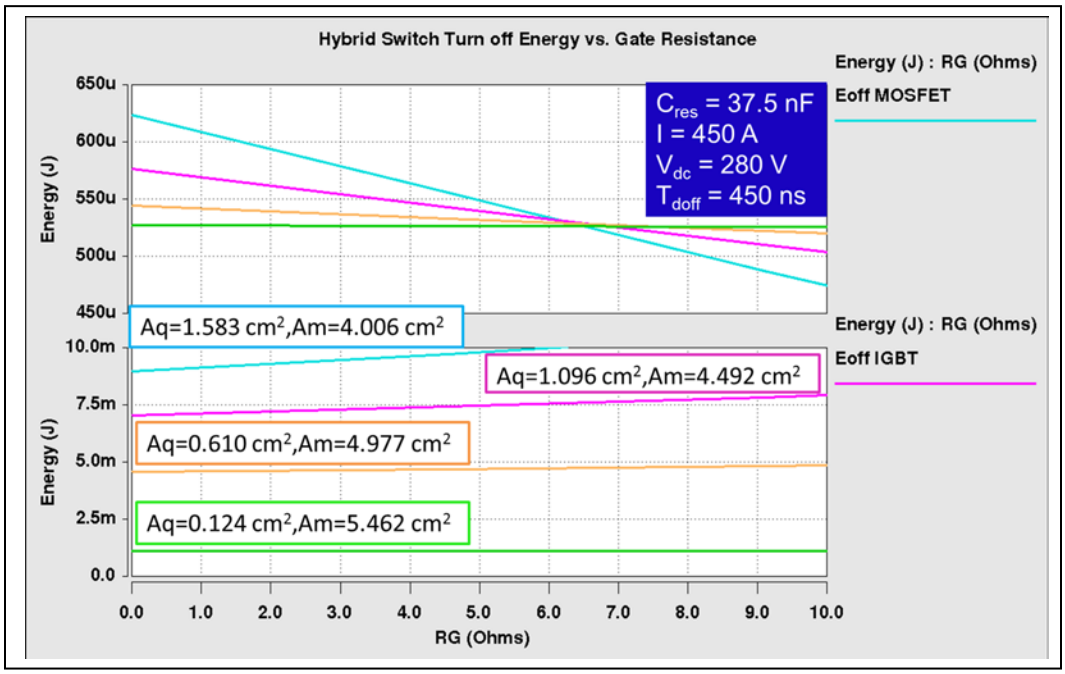

Fig. 7-9 Turn-off Energy vs. Gate resistance Hybrid Switch

As a comparison, the second experiment runs the same design space of chip area but without a snubber capacitor and the gate drive timing delay is removed. Fig. 7-10 shows the result. In this case, the gate resistance has a bigger impact on the turn-off energy. The change in energy as a function of gate resistance range is almost 7 times that of the previous result. Therefore it can be concluded that an increased gate resistance using a snubber capacitor and gate drive timing

strategy does not result in significant turn-off loss. However the gate resistance still should be kept at a minimum to avoid having to increase the dead time.

In the design optimization proposed in this dissertation, the gate resistance is not used as a design variable, but rather a design input. However the optimization strategy and multi-scale simulation approach makes it easy to include the gate resistance as a design variable if desired.

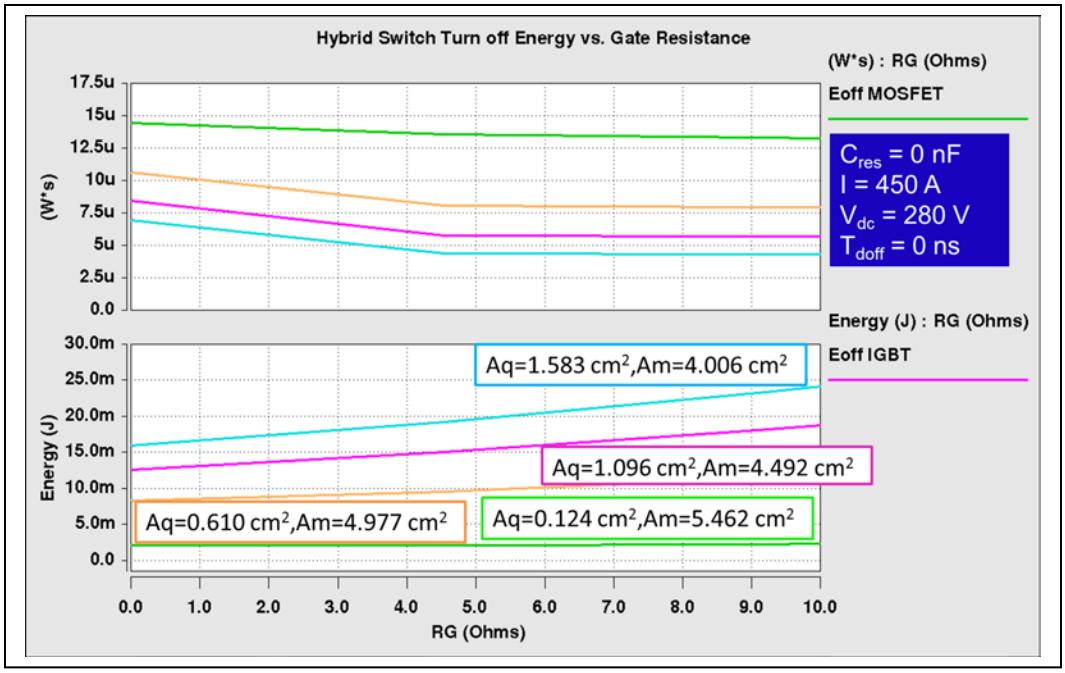

Fig. 7-10 Turn-off Energy vs. Gate resistance Hybrid Switch

7.3.3 Design Constraint – Minimum Turn-on

The gate drive timing strategy described above has a direct impact on the minimum turn-on requirement. The minimum on time requirement has to allow enough time for a proper resonant transition to achieve zero voltage switching and enough time for the coupled magnetics to properly reset. This minimum on time impacts the regulation of the inverter and should be kept to a minimum. Therefore, the minimum on time should be less than 3% of the PWM period. This results in a minimum time constraint given by:

$$T_{on\min} = T_{R\max}(\le T_{doff}) + T_{resperiod} = \left(1 + \frac{N_1}{N_1 + N_2}\right) T_{R\max} < 3\% \frac{1}{f_{sw}} \tag{7.14}$$

Where the resonant period, $T_{resperiod}$, is given by:

$$T_{resperiod} = \left\{ \begin{array}{l} \frac{L_r}{Z_r}\left[\pi - \cos^{-1}\left(\frac{N_1}{N_2}\right) + \left(\frac{N_2}{N_1}\right)\sqrt{1 - \left(\frac{N_1}{N_2}\right)^2}\right] \\ + \frac{L_r}{V_{dc\min} / I_{o\max}}\left(2 + \frac{N_1}{N_2} + \frac{N_2}{N_1}\right) \end{array} \right\} \tag{7.15}$$

7.3.4 Design Trade-offs

Given the constrain in (7.14) , and given a resonant capacitor, c_{res}, the resonant inductor, L_r, has to adjust such that the sum of the turn-off delay and the resonant transition time does not exceed 3% of the total switching period. Therefore the resonant inductor becomes a dependent variable based on the independent variable c_{res}. The resonant inductor is related to the primary leakage inductance design variable by (7.12).

A design trade-off exists as the resonant capacitor is varied. Increasing the snubber capacitor, $C_{res,}$ reduces the losses associated with the current tail bump of the IGBT, but results in increased current stress in the auxiliary switch. The peak current in the auxiliary switch is directly proportional to the resonant surge impedance, Z_r , and shown below:

$$I_{auxpeak} = \frac{N_2}{N_1 + N_2}\left(I_{o\max} + \frac{N_2}{N_1 + N_2}\frac{V_{dc}}{Z_r}\right) \tag{7.16}$$

Assuming a fixed turn-off delay that meets the constraint (7.13), the leakage inductance can be calculated as a function of the resonant capacitor. The relationship is nonlinear and a Newton-Raphson method is required to solve for the leakage inductance as a function of the resonant capacitor. In order to illustrate the design trade-offs, Fig. 7-11 shows the leakage inductor vs.

resonant capacitor to maintain the design constraint (7.14) and also shown is the peak auxiliary current.

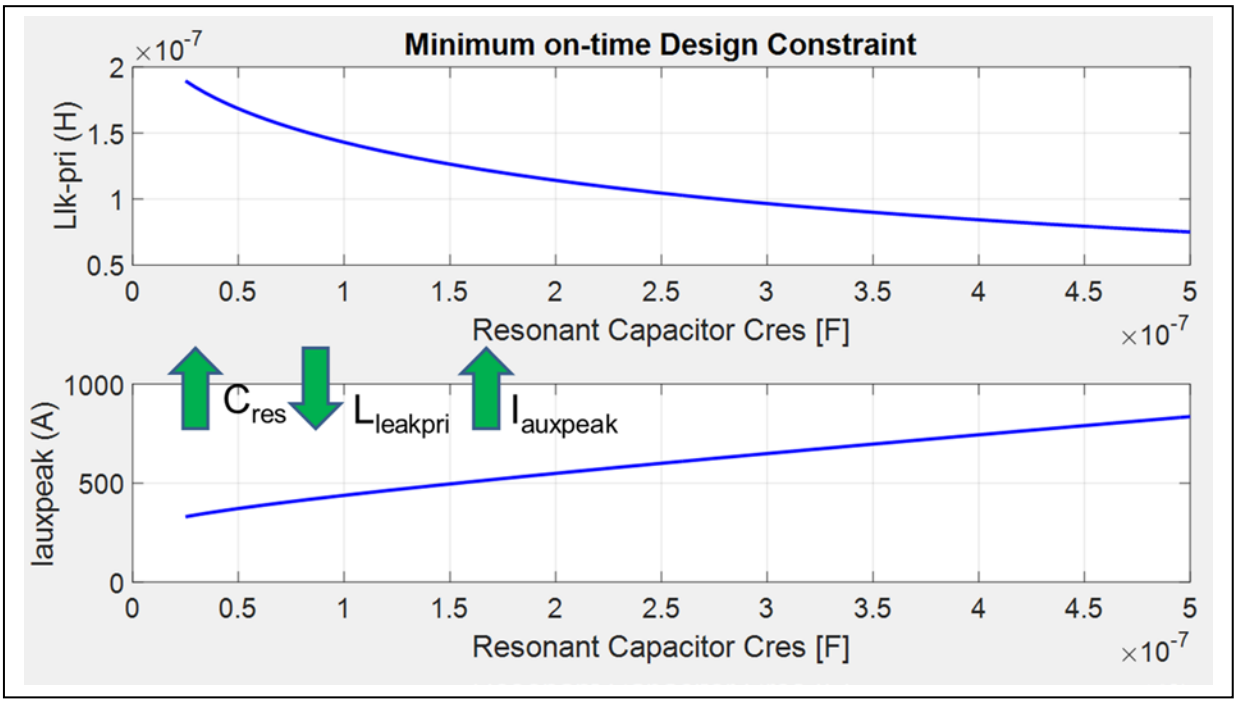

Fig. 7-11 Primary leakage inductance and auxiliary current vs. resonant capacitor

It can be seen that the required resonant inductor becomes smaller as the resonant capacitor increases. This results in an increased peak auxiliary current. As the peak current increases in the auxiliary IGBT, the device begins to enter the active region of operation where the voltage drop is significantly increased. Not only does this increased voltage drop increases the conduction loss of the auxiliary switch resulting in possible thermal failure, it also reduces the amount of voltage available to charge the leakage inductance resulting in reduced energy available for soft-switching of the main switch. Therefore, it is concluded that the design trade-off becomes reducing the IGBT turn-off loss with a larger capacitor, but at the expense of the current stress seen by the auxiliary IGBT and increased hard switching induced turn-on loss of the main

switch. Therefore, an optimum design point is achievable. To capture this design trade-off the total device switching loss, P_{sw}, should include the auxiliary IGBT conduction loss.

The turn-off delay, T_{doff}, can be increased to assist with IGBT turn-off loss but again results in design trade-offs. An increased turn-off delay requires a smaller leakage inductance to allow for faster ZVS resonant transition to meet the design (7.13) constraint. An increased turn-off delay requires a smaller leakage inductance to allow for faster ZVS resonant transition to meet the design (7.13) constraint. However, this becomes a *di/dt* trade-off. A faster resonant transition increases the *di/dt* controlling the turn-off of the MOSFET body diode, resulting in higher loss due to body diode recovery induced loss in the main switch. In addition, *di/dt* can falsely trigger the voltage sensitive circuits used for ZVS detection to due noise pickup. Care should be taken to keep the *di/dt* to a minimum. The di/dt can be calculated by the following:

$$\frac{di}{dt} = \frac{N_2}{N_1 + N_2} \frac{V_{dc}}{L_r} \tag{7.17}$$

7.3.5 Auxiliary Switch Loss

The turn-off loss simulation circuit did not include the auxiliary switch since loss incurs in the auxiliary switch during turn-on. Since the main switch turns on with zero volts, a separate turn-on loss simulation is not necessary. All the loss that incurs in the auxiliary switch is due to conduction. The waveform for the auxiliary current is reconstructed from the following figure:

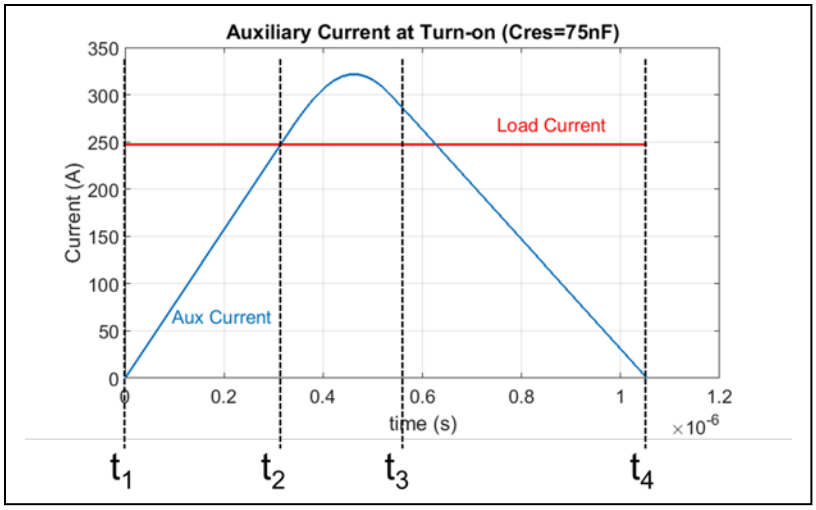

Fig. 7-12 Auxiliary Current at Turn-on Cres=75nF

At time t_1 the auxiliary switch is turned on and the resonant inductor is charged with a scaled bus voltage through the turns ratio and linearly charged until the resonant current equals the load current, I_{load} ,at t_2. The resonant current, $i_{LR}(t)$, during the resonant charging time from t_1 to t_2 is given by:

$$i_{LR}(t) = \frac{I_{load}}{t_{21}} t \tag{7.18}$$

Where

$$t_{21} = I_{load} \frac{L_r}{kV_{dc}} \tag{7.19}$$

Once the resonant current equals the load current, the resonant period begins where the capacitance of the main switch begins to discharge due to the excess energy in the resonant inductance, L_r. The voltage and current are in resonant transition until the voltage across the main switch has discharged to zero at t_3. During the resonant transition from t_2 to t_3 the resonant current and resonant voltage across the switch are given by the following:

$$i_{LR}(t) = I_{load} + \frac{\sin(\omega_r t) kV_{dc}}{Z_r} \tag{7.20}$$

$$v_c(t) = kV_{dc}\left(1 - \cos(w_r t)\right) \tag{7.21}$$

Where

$$\omega_r = \frac{1}{\sqrt{L_r 2C_{res}}} \tag{7.22}$$

$$k = \frac{N_2}{N_1 + N_2} \tag{7.23}$$

The time from t_2 to t_3 is calculated by solving the time where the voltage across the device, $v_c(t)$,reaches zero.

$$t_{32} = \frac{1}{\omega_r}\cos^{-1}\left(\frac{k-1}{k}\right) \tag{7.24}$$

Substituting (7.24) into (7.20) the current where the voltage reaches zero:

$$I_x = \frac{kV_{dc}}{Z_r}\sin\left(\cos^{-1}\left(\frac{k-1}{k}\right)\right) + I_{load} \tag{7.25}$$

At t_3, the main switch is turned on with zero volts and the resonant current decays to zero from t_3 to t_4.The resonant current is calculated:

$$i_{LR}(t) = \mathrm{I_x} - \frac{V_{dc}}{L_r}(1-k)t \tag{7.26}$$

The time from t_3 to t_4 is determined where the resonant current has decayed to zero is calculated by:

$$t_{43} = T_{resperiod} - t_{21} - t_{32} \tag{7.27}$$

Where $T_{resperiod}$ is given by (7.15).

To calculate the dissipated loss in the auxiliary switch due to conduction at turn-on the energy relationship vs. load current is first established just as was the case for the turn-off energy for the main switch. The turn-on energy of the auxiliary switch is calculated vs. load current:

$$E_{aux-on} = \int_0^{t_5} \underbrace{\frac{n}{n+1} i_{LR}(t)}_{i_{lk-pri}} v_{saux}(t)dt \tag{7.28}$$

Where n is the transformer turns ratio of the coupled magnetic. It is noted in (7.28) that the current in the auxiliary switch, $i_{lk\text{-}pri}$ is the reflected current of the resonant current through the transformer by ($n/n+1$). The auxiliary on-state voltage $v_{saux}(t)$ can be determined by an on-state simulation of the auxiliary device model:

$$v_{saux}(t) = \mathrm{V_t} + \mathrm{R_{ce}} \underbrace{\frac{n}{n+1} i_{LR}(t)}_{i_{lk-pri}} \tag{7.29}$$

Where V_t is the IGBT fixed voltage drop under zero current condition. R_{ce} represents the IGBT on-drop resistance. Substituting (7.18)-(7.29) into (7.28) the energy of the auxiliary switch vs load current is given by:

$$\begin{aligned} E_{aux-on} = & \int_{t1}^{t2} \frac{n}{n+1} \frac{I_{load}}{t_{21}} t \left(\mathrm{V_t} + \mathrm{R_{ce}} \frac{n}{n+1} \frac{I_{load}}{t_{21}} t \right) dt + \\ & \int_{t2}^{t3} \frac{n}{n+1} \left(I_{load} + \frac{\sin(\omega_r t) kV_{dc}}{Z_r} \right) \left(\mathrm{V_t} + \mathrm{R_{ce}} \frac{n}{n+1} \left(I_{load} + \frac{\sin(\omega_r t) kV_{dc}}{Z_r} \right) \right) dt + \\ & \int_{t3}^{t4} \frac{n}{n+1} \left(\mathrm{I_x} - \frac{V_{dc}}{L_r} (1-k)t \right) \left(\mathrm{V_t} + \mathrm{R_{ce}} \frac{n}{n+1} \left(\mathrm{I_x} - \frac{V_{dc}}{L_r} (1-k)t \right) \right) dt + \end{aligned} \tag{7.30}$$

Using a trapezoidal numerical integration to compute (7.30) during post processing, the average dissipated power, P_{sw-aux}, can be calculated using (7.7) and (7.8).

7.4 Results Loop 1 and Loop 2

The total loss from Loop 1 and Loop 2 are summed together per the flow diagram in Fig. 7-1.

$$P_{total}(A_m, A_q, C_{res}) = P_{swtotal}(A_m, A_q, C_{res}) + P_{cond}(A_m, A_q) \tag{7.31}$$

The chip area and resonant capacitor that minimizes the total device loss subject to the constraints outlined is shown in Table 7-3.

Table 7-3 Optimized Design Variables at 90 Degree C

Design Variable	Value
A_M	*4.56 cm^2*
A_Q	*1.04 cm^2*
A_{diode}	*0.1 cm^2*
C_{res}	*37.5 nF*
$L_{lk\text{-}pri}$	*178 nH*
T_{doff}	*450 ns*

Fig. 7-13 shows the total loss at the optimal design points for the chip area as a function of C_{res} and the result if the auxiliary chip loss is not considered. In the optimized design with aux chip consideration the total losses start to increase at a resonant capacitor value of 100 nF. The reason for this is because a larger capacitor, while reducing the turn-off loss in the IGBT, results in a larger peak auxiliary current as shown in Fig. 7-11. The auxiliary losses start to dominate as a result of forced linear active conduction. The voltage drop increases considerably in the linear region and can even result in less energy available to charge the resonant inductor. This may lead to hard switching of the main switch in some cases. If the auxiliary chip loss is not considered or if the auxiliary chip is made large enough to avoid entering the active region of operation the IGBT turn-off loss would continue to decrease with increased snubber capacitor.

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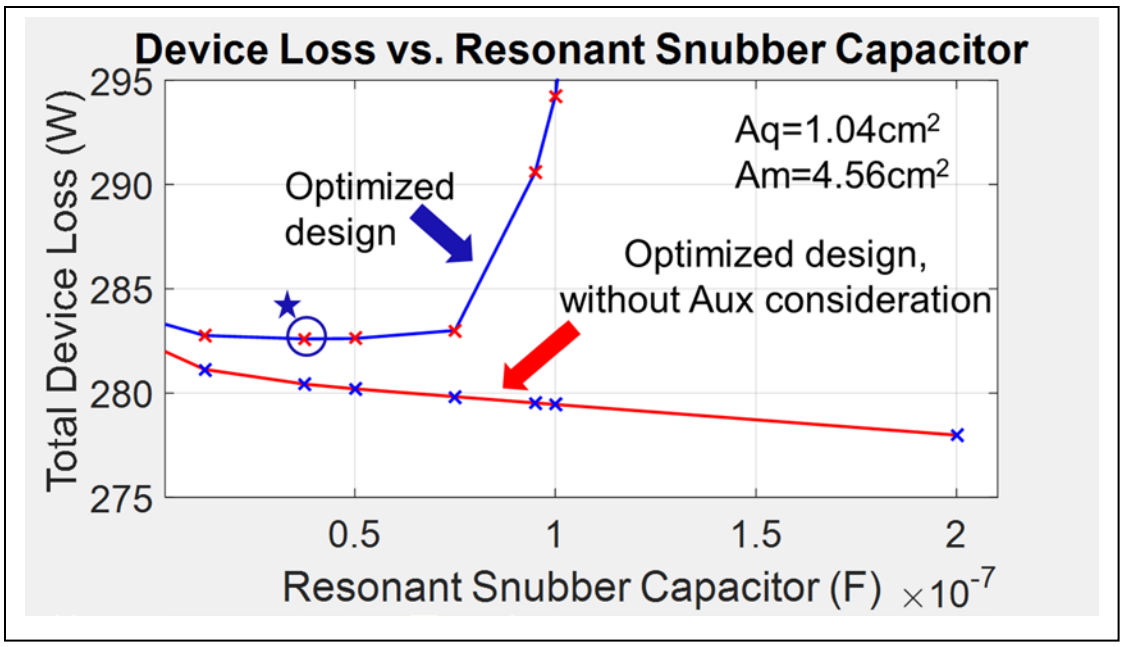

Fig. 7-13 Total Loss vs. Resonant Capacitor

Fig. 7-14 shows the total loss at the optimal design point for the resonant capacitor C_{res} as a function of A_q and A_m.

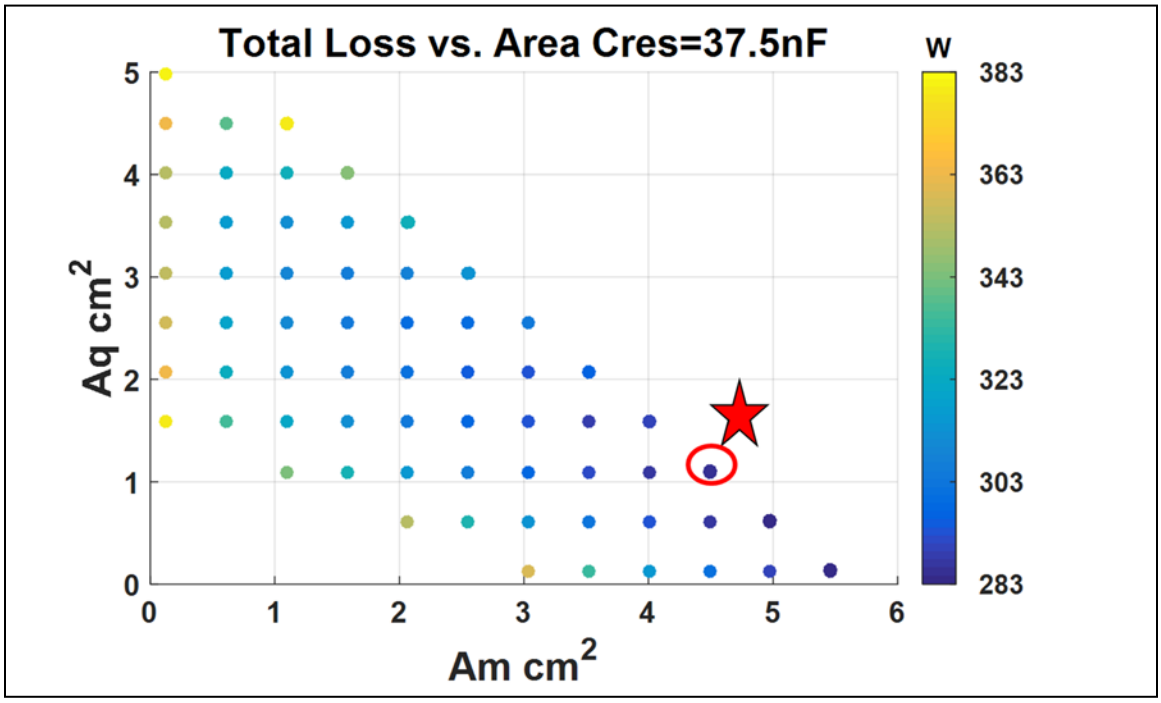

Fig. 7-14 Total Loss vs. Chip Area (C_{res}=37.5nF)

Fig. 7-15 shows a breakdown of conduction loss and switching loss. The results indicate that if one was only considering conduction loss at 90 degree C, the IGBT wants to be the bigger area as compared to the MOSFET. This makes sense since the R_{dson} of the MOSFET increases with temperature and the threshold voltage for the IGBT decreases with temperature. However there is a big penalty to pay for switching loss at high temperature for the IGBT. If the IGBT is larger than it conducts much higher currents. Therefore there is a much larger turn-off loss due to the tail current induced losses which is worse at higher temperatures.

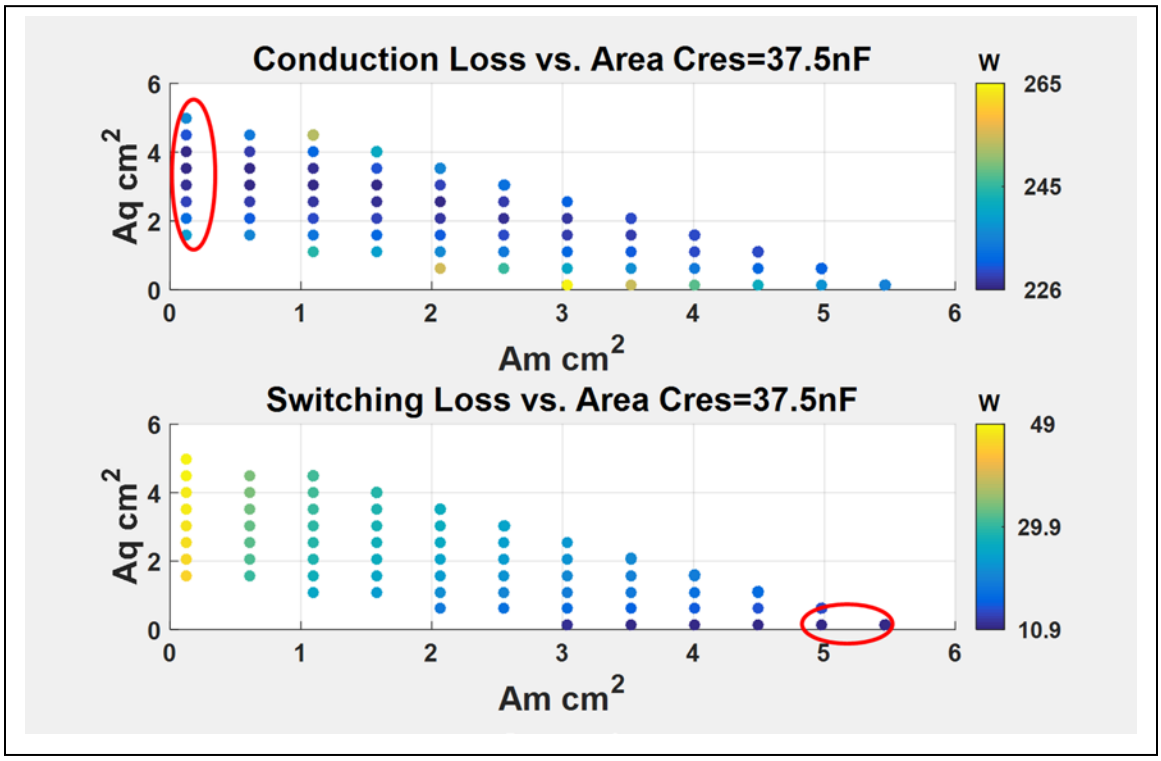

Fig. 7-15 Conduction Loss vs. Switching Loss (C_{res}=37.5nF)

7.5 Loop 3

The final loop involves optimizing the cooling system. Since the design has already been designed for minimum loss implies the cooling system already has been optimized because the amount of dissipated power as heat has been minimized. The only parameter that has to be

adjusted is the convection coefficient, h_c, until the maximum junction temperature during an inverter load cycle is equal to the set operating temperature. In this case the operating temperature and the temperature for which the design has been optimized have been chosen as 90 degree C.

The loop 3 simulation is run with the average dissipated power, calculated over a switching cycle determined from Loop 1 and Loop 2, as an input to the thermal model based on finite differences as described in Chapter 4. The finite difference equations are programmed in the SABER® MAST language and are parameterized in terms of structural and material geometry. Also included are temperature dependent parameters such as the nonlinear thermal conductivity of silicon. The SABER® model can be used as a building block for any 1-3 D configuration. Each SABER® MAST block represents one finite difference nodal equation in rectangular coordinates with connections to all three dimensions with heat stored at the center node. All one has to do is connect the building blocks accordingly to build the module. The result is a multi-dimensional thermal model based on the boundary conditions within the module. Fig. 7-16 shows a snapshot of the thermal model made up of individual FDM blocks written in MAST.

For the Loop 3 study, each chip is assumed to be decoupled from each other with .225 cm on either adjacent side to allow adequate heat spreading without thermal interference from neighboring chips. The individual material layer depths and thermal properties are given in Table 3-1. A convection boundary condition is forced at the bottom of the copper baseplate layer. The convection coefficient, h_c, is left variable and will be adjusted until the peak junction temperature during steady state has reached the operating temperature which the design optimization assumed. The assumed cooling temperature liquid is 30 degree C. The convection boundary

condition is also implemented with a finite difference equation and connecting to the bottom nodes of the DBC.

The number of nodes is chosen to reflect where the largest temperature gradients occur. The silicon chip is represented with 5 vertical and horizontal nodes. The silicon layer just 1. The substrate ALN layer is also represented with 5 vertical and horizontal nodes. The copper layers assume 3 vertical and 3 horizontal nodes. This node density was chosen based on the model validation achieved in Chapter 4. Fig. 7-17 shows a transient analysis showing the temperatures at the top of each layer obtained from the proposed SABER FDM model and the FEM model. The agreement, with the suggested node density, agrees very well.

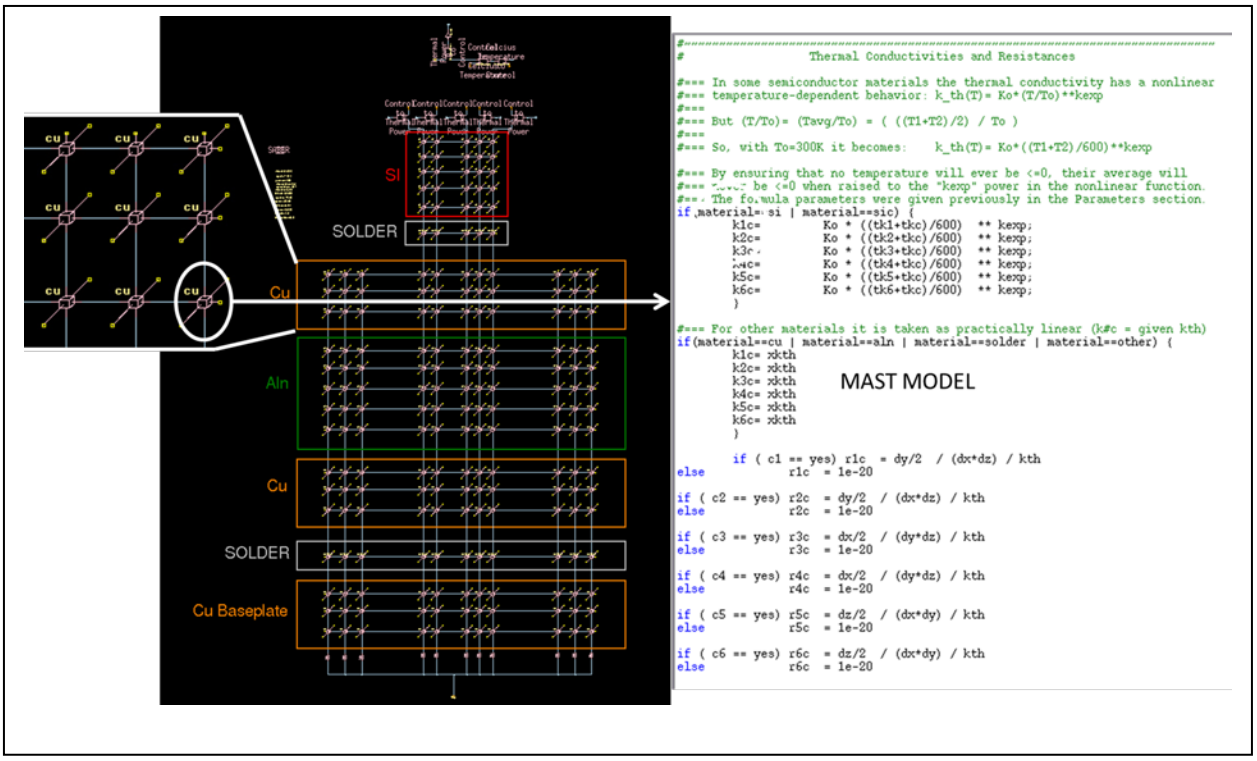

Fig. 7-16 Multidimensional Thermal Model

Table 7-4 summarizes the RMS error of the temperatures at the top of each layer under transient and steady state condition between the proposed FDM Saber model and FEM analysis. The errors are very small validating that the mesh density of the proposed SABER FDM model is more than adequate.

Table 7-4 RMS Error Transient and Steady State FDM vs. FEM

Layer	Transient RMS error	Steady-State RMS error
Silicon	0.2032	0.0296
Solder	0.2026	0.0325
Copper	0.2013	0.0305
ALN	0.2003	0.0314
Copper	0.1924	0.0315
Solder	0.1894	0.0294
Copper Plate-Top	0.1821	0.0339
Copper Plate-Bot	0.0994	0.2357

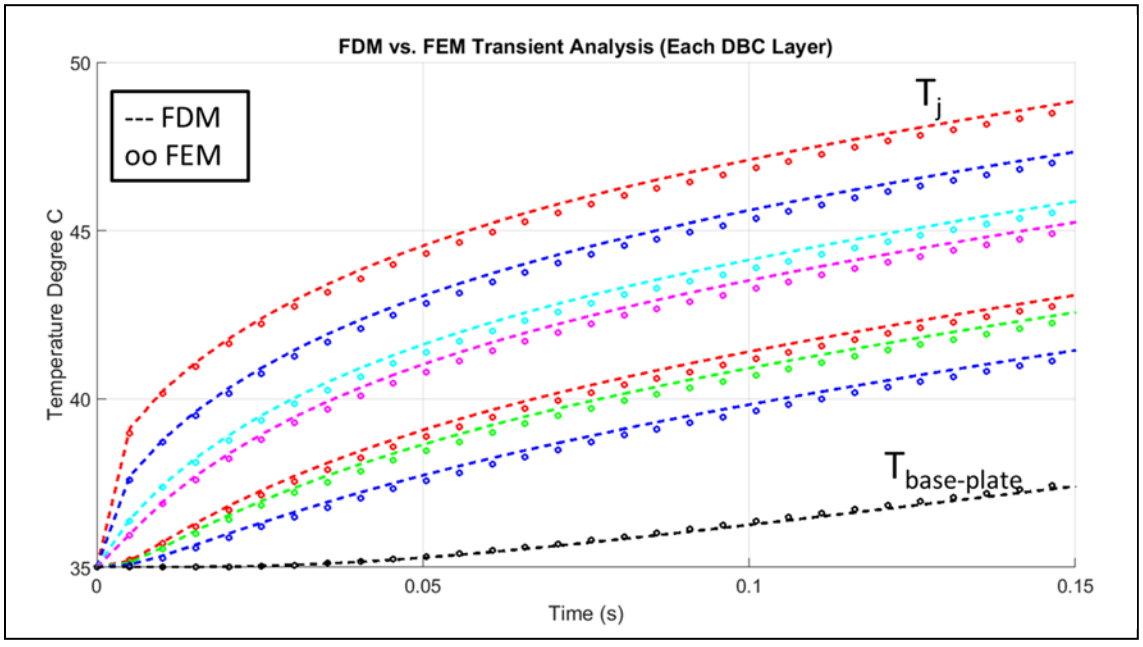

Fig. 7-17 FDM vs. FEM Transient Analysis

7.5.1 Temperature Gradient Effect

While this dissertation considers physics-based models for the electrical portion of the electro-thermal model, the temperature dependent parameters are behavioral curve fits based on the parameter extraction measurements. Scaling the chip area during the optimization procedure also scales the temperature dependent parameters such as the saturation transconductance. This is done by the Hefner IGBT model [11]. There is some question, when "lumping" the entire chip area into one actual device model, as to what temperature to use as the feedback for the electrical device model. The procedure outlined in this dissertation considers the center of the chip for the feedback temperature point for the device model. And when considering multi-chip situations lumped into one electrical device model, the assumption is the most interior chip center is the highest temperature and used as the feedback point. This is true if the outer edge of the chip or outer edge of the most exterior chip, when considering multi-chip, is not coupled thermally to another adjacent chip. Since the outer edge runs cooler, a temperature gradient can occur across the chip depending on the outer most edge boundary conditions. The thermal models modeled in this dissertation assumes 0.225 cm on the outermost edges of the total heat source. Fig. 7-18 shows the steady state temperature gradient across the top surface of the MOSFET. For purposes of considering the worst case thermally, as it pertains to the most interior chip center, the distance between the adjacent MOSFET chips was assumed to be 0 cm. The gradient in this case is only about 5 degrees from the center of the most interior chip to the edge of the outermost chip. In the event that the gradient is much higher, the electro-thermal models would have to be separated into smaller elements and the appropriate temperature outputs of the FDM model would serve as the individual feedback points. The building block approach in this dissertation

allows very easily for this modification if determined necessary based on the thermal boundary conditions.

When considering multiple chips as it relates to current sharing, it is pointed out that paralleling MOSFETs should provide adequate current sharing since the R_{dson} of the chip increases with temperature. Therefore the temperature should be evenly distributed. When considering multiple IGBTs, it is noted the threshold voltage decreases with temperature and if the IGBT is used on the active mode where the gate voltage is near threshold, the inner most chip center could potentially "hog" the current and result in thermal run-away. However the optimization in this work uses the IGBT at gate voltages well above the threshold voltage since the application is a switching application.

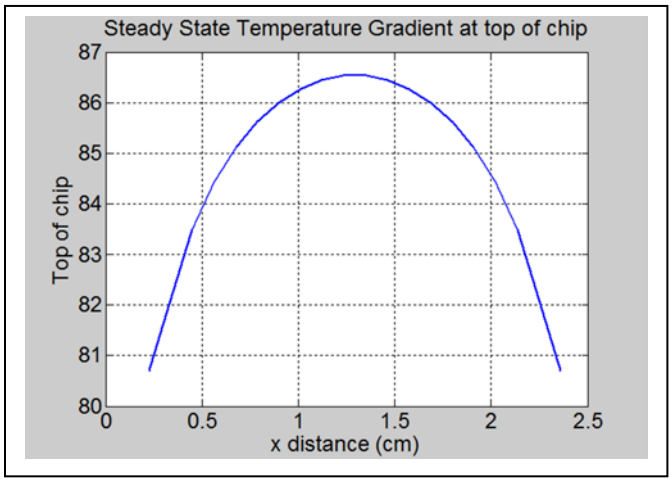

Fig. 7-18 Temperature gradient across top surface of MOSFET

7.5.2 Loop 3 Simulation Result and Comparison to Baseline Design

Fig. 7-19 shows the Loop 3 simulation where the thermal model in Fig. 7-16 is underneath the SABER® hierarchal blocks. The power from Loop 1 and the energy curves mapped to power dissipations from Loop 2 are averaged over a switching period using the relationships earlier and implemented as power sources into the thermal model for each device.

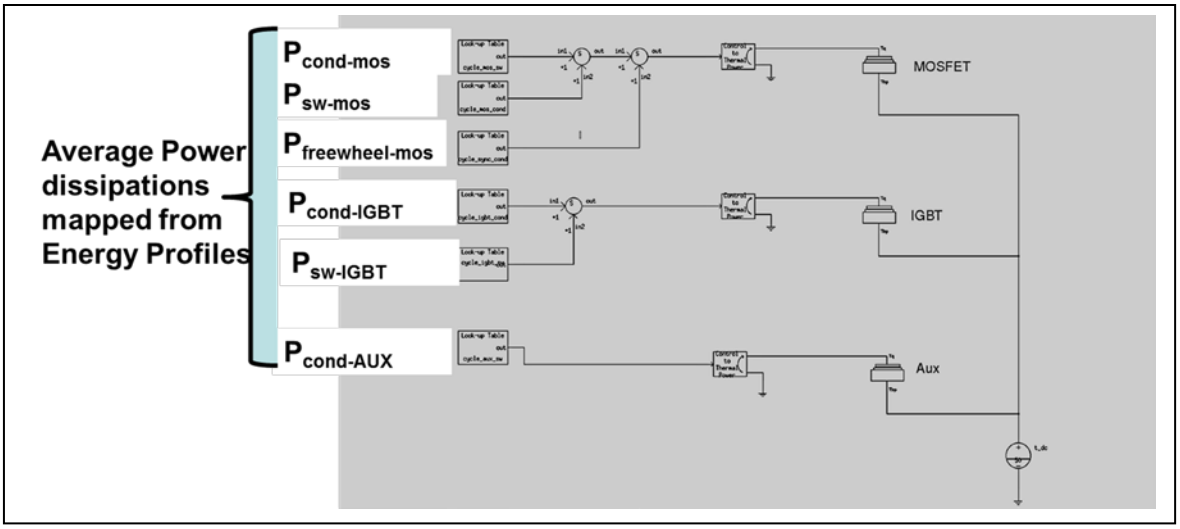

Fig. 7-19 Loop 3 Thermal Simulation.

Table 7-5 shows a design comparison with the baseline generation 2 soft-switching module and the proposed optimized design. The results show an improvement over the current generation 2 design of almost **16%**. The total chip area remained the same but an additional **52W** was saved by reallocating the individual device areas. In addition, the baseline design required a heating coefficient **42%** higher than the optimized proposed design to keep the hottest junction temperature, in this case the IGBT, at 90 degree C. The baseline design results in a "hotspot" since the IGBT incurs a larger percentage of the loss thus driving the cooling requirements. The new proposed design distributes the heat better reducing the required cooling coefficient.

In the baseline design most of the losses were due to conduction in the IGBT, but due to the amount of current in the IGBT, the turn-off loss of the IGBT was much higher than the proposed optimized design. In the proposed design most of the loss is due to conduction in the MOSFET. And since the MOSFET conducts most of the current, there is less turn-off loss in the IGBT

where the savings are noticed. The take away here is that a recommendation of adding more MOSFET area will improve the losses at higher temperature.

Table 7-5 Comparison Baseline Design and Proposed Optimized Design

Design Variables	Optimized	Base-line Gen 2
C_{res}	37.5 nF	100 nF
A_M	4.56 cm^2	1.14 cm^2
A_Q	1.04 cm^2	2.88 cm^2
$L_{lk\text{-}pri}$	178 nH	168 nH
A_{diode}	0.1 cm^2	1.7 cm^2
A_{aux}	1.16 cm^2	1.16 cm^2
$T_{d\text{-}off}$	450 ns	450 ns
h_c	25000 $W/m^2/°C$	43000 $W/m^2/°C$
IGBT Loss P_{SW}	25 W	94 W
IGBT Loss P_{Cond}	47 W	137 W
MOSFET Loss P_{SW}	3 W	9.5 W
MOSFET Loss P_{Cond}	200 W	38 W
Aux-IGBT Loss	2 W	2.4 W
Diode Loss	5 W	53 W
Total Loss	**282 W**	**334 W**

Fig. 7-20 shows the transient response for the IGBT, MOSFET, and auxiliary junction temperatures. It takes almost 4 seconds to reach steady state. By applying the averaging operator to the dissipated power over the switching period, running a simulation this long with a full FDM model is not unreasonable at all. The cooling coefficient was adjusted so the hottest part, in this case the MOSFET, operates under steady state at the given operating temperature input of 90 degree C. As shown in the figure, the MOSFET conducts during the main and free-wheel portions as evident by the temperature rise when the IGBT is cooling.

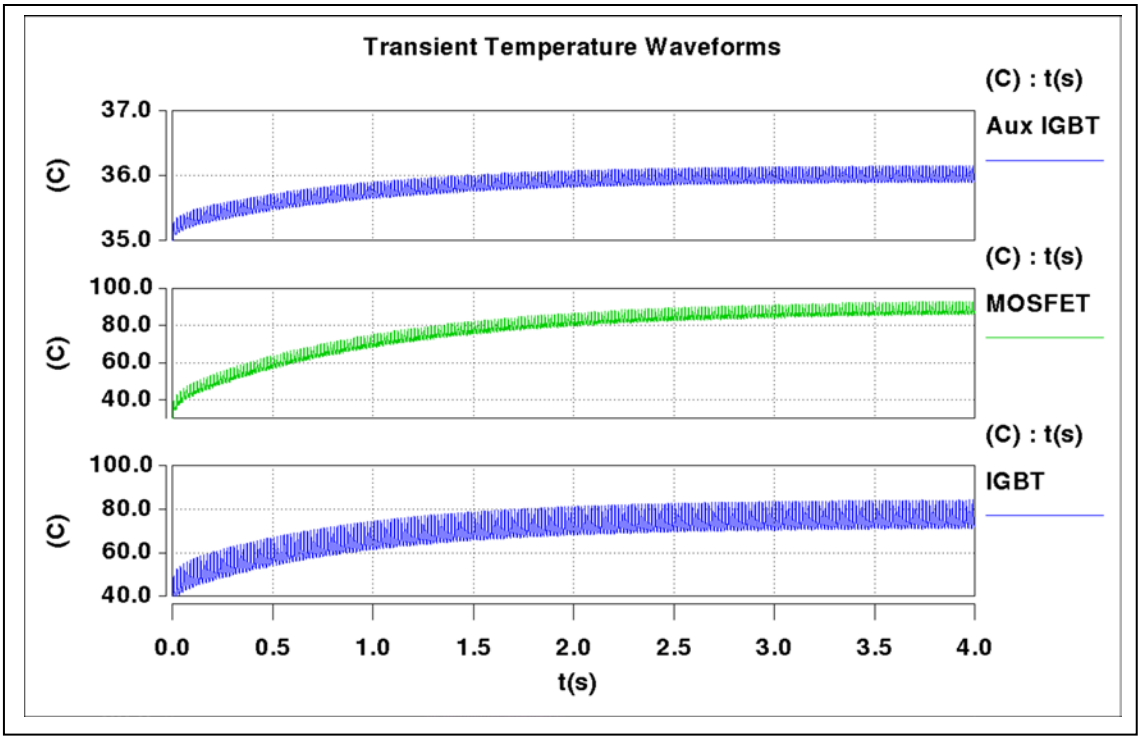

Fig. 7-20 Loop 3 Transient Response

Fig. 7-21 shows the temperatures zoomed in during steady-state.

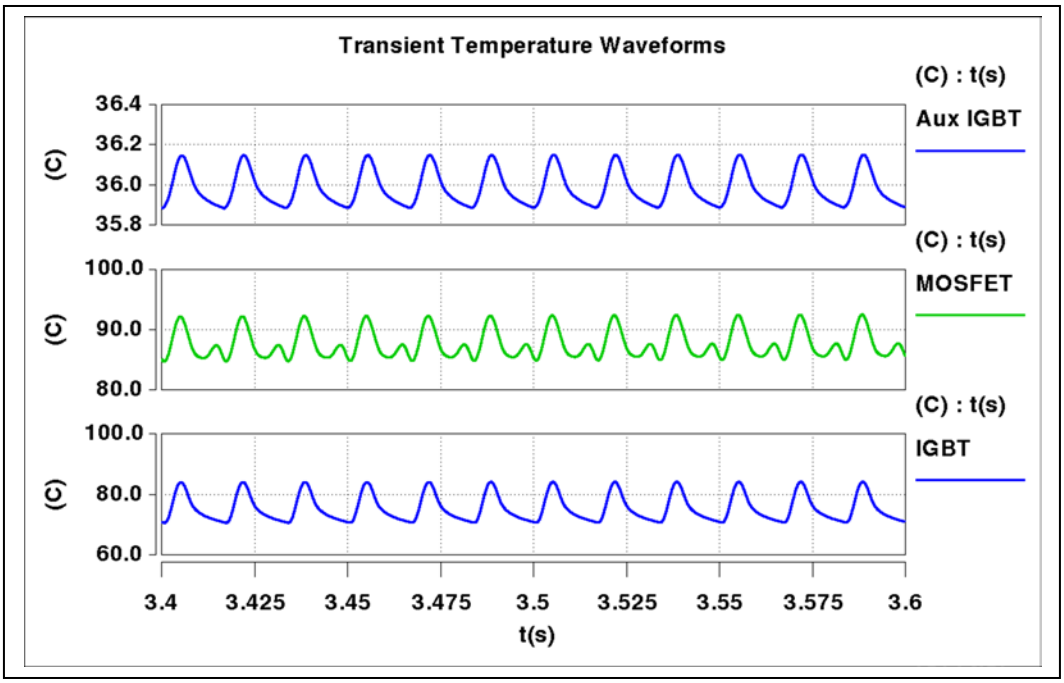

Fig. 7-21 Loop 3 Steady State Response

Using the same chip die available in the generation II baseline soft-switching module, the same die chips are rearranged per the optimized design result. The chip area for the main MOSFET has increased from two chips to eight per the new proposed design. The main diodes are all but removed from the module. The main IGBT is reduced from two chips to slightly less than 1 chip. The auxiliary chips remain the same between the two designs. The recommended layout change to the generation II module is shown in Fig. 7-22. The design is conceptual at this point but the total chip area remains the same between the two modules. The big takeaway and recommendation is to improve the design by adding more MOSFETS and less IGBT.

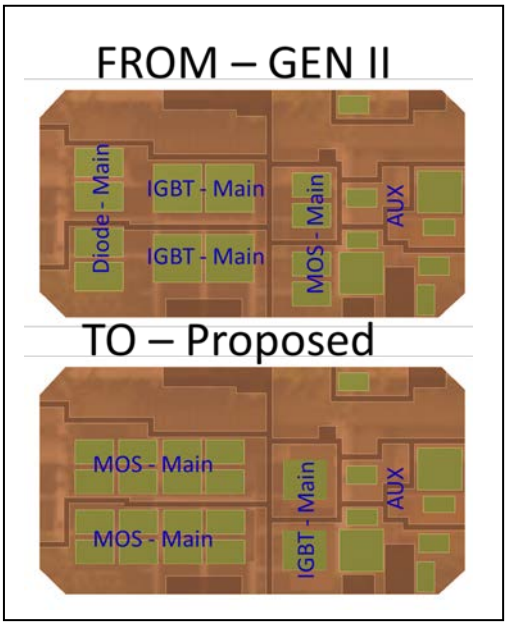

Fig. 7-22 Gen II Module vs. Proposed

7.5.3 Full Electro-thermal Simulation

Now that the optimum design has been reached and the convection coefficient has been determined to maintain the operating junction temperature of the inverter, a full electro-thermal simulation where the instantaneous dissipated power is determined within the switching cycle can be run. Since the simulation takes much longer due to the required small time step to

adequately represent the switching waveforms, initial conditions can be used to bring the inverter to steady state temperature right away. This is done by using the Loop 3 simulation. The average steady state temperature is determined and used as an initial condition in the full electro-thermal simulation. This allows only a few inverter cycles (<100ms) as compared to the Loop 3 simulation which required 4 seconds of simulation time to reach steady state. This a huge advantage by using separate simulations during the optimization flow charts.

Fig. 7-23 shows the steady state MOSFET and IGBT temperatures operating at the designed temperature of about 90 degree C. Only a few inverter cycles were required for steady state since the correct initial condition determined from the Loop 3 simulation was used. Large temperature spikes occur within the IGBT and represent the energy dissipated at turn off of the IGBT. This is due to the tail current loss, which has been minimized using the time delay between the MOSFET and IGBT. It is noted these temperature spikes do not occur during the turn-on since the devices turn on under zero-voltage switching condition.

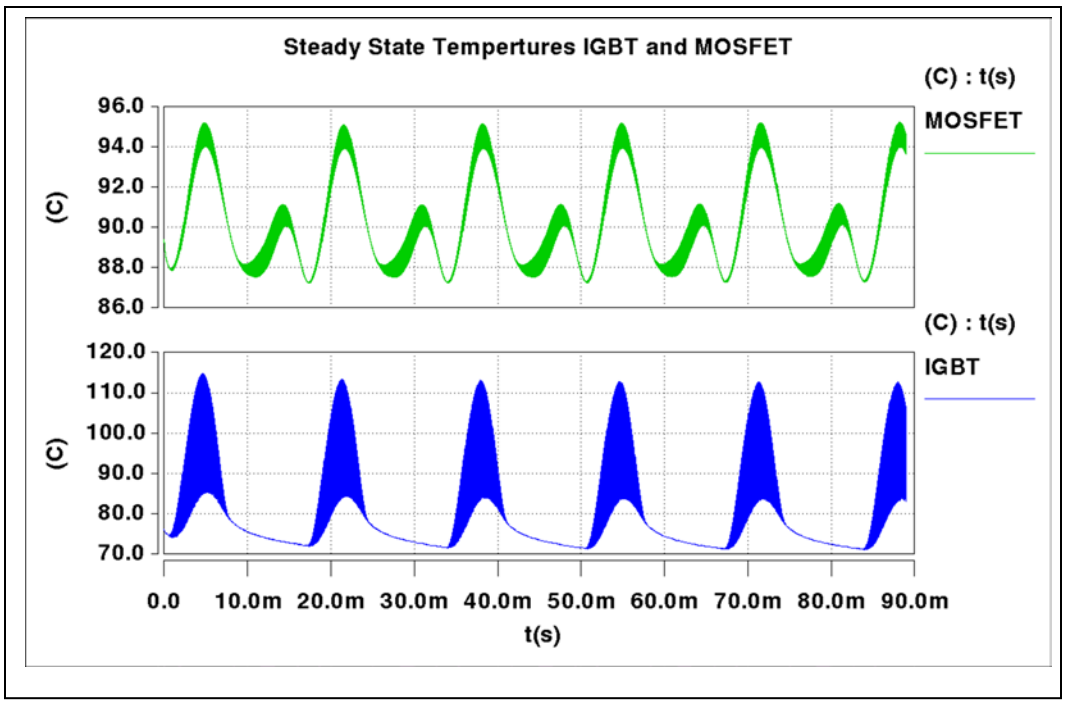

Fig. 7-23 Steady State Temperatures IGBT and MOSFET

To observe the effects of energy leading to dissipated power within the switching cycle, Fig. 7-24 shows the IGBT energy along with temperature and gate voltage for one switching cycle. It is observed that there is no increase in energy incurred at turn-on further validating that the device is operating under soft-switching condition. Turn-off shows the large increase in energy due to the turn-off tail induced loss leading to the temperature spikes seen in Fig. 7-23. Fig. 7-25 shows the energy profile for the MOSFET. As expected, there is no energy rise at turn-on due to ZVS. But there is a small increase in energy observed at turn-off resulting from the MOSFET having to conduct the full load current when the MOSFET was turned off prior to the IGBT. Both sets of waveform show the energy rise during conduction.

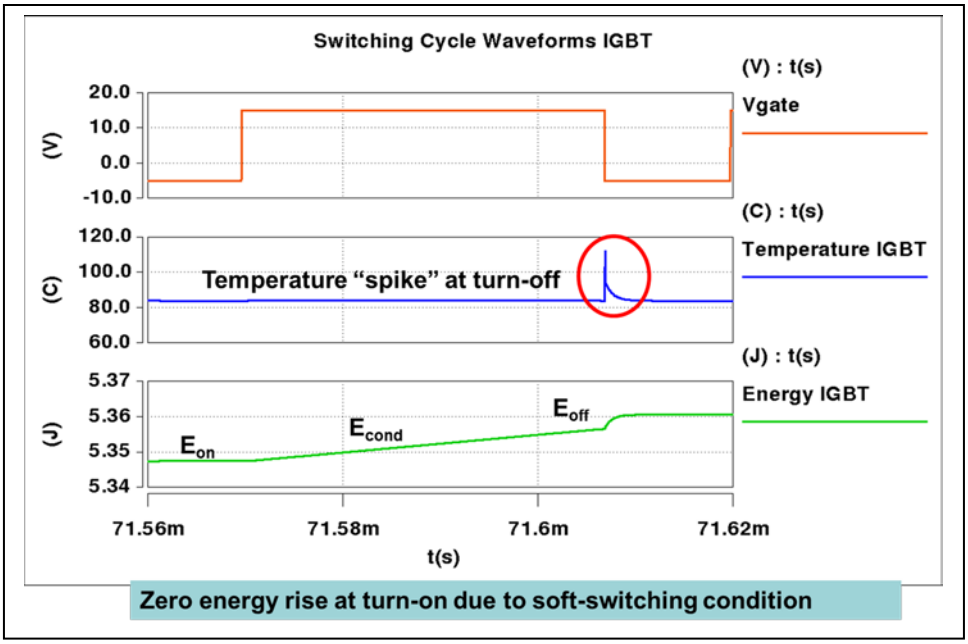

Fig. 7-24 Electro-thermal Waveforms within switching cycle - IGBT

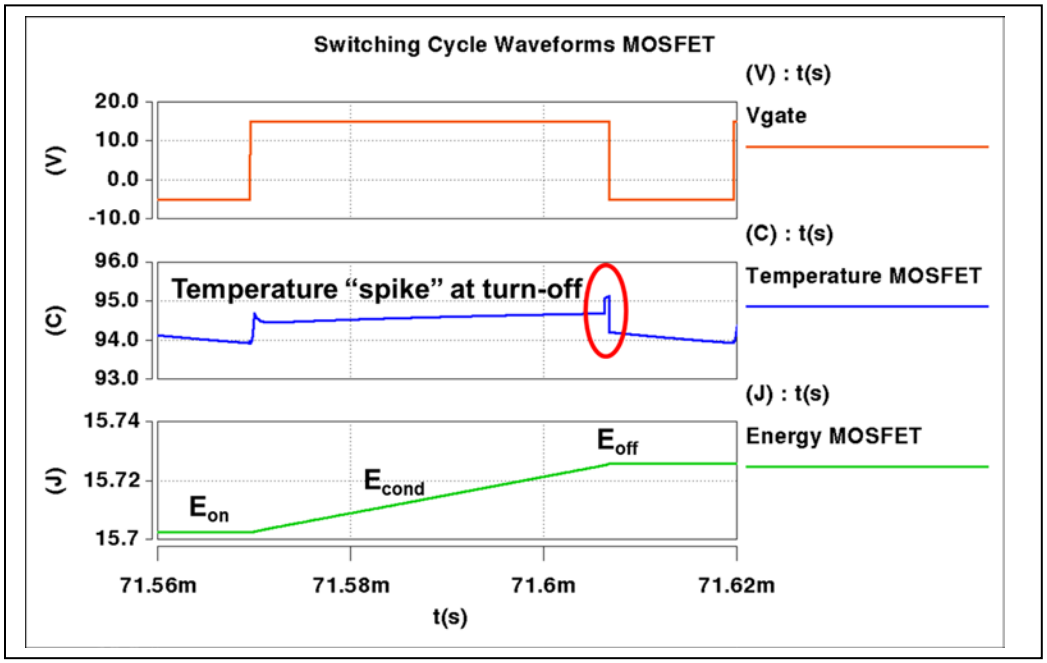

Fig. 7-25 Electro-thermal Waveforms within switching cycle - MOSFET

As a comparison to the baseline design a full electro-thermal simulation is run with the required cooling coefficient, 25000 W/cm^2/°C, from the proposed optimized design. The

junction temperatures are plotted and shown in Fig. 7-26. The baseline IGBT temperature under the same cooling coefficient is much higher than the proposed optimized design. While the MOSFET of the baseline design runs cooler, the heat distribution is not as good since all the heat is dissipated in the IGBT.

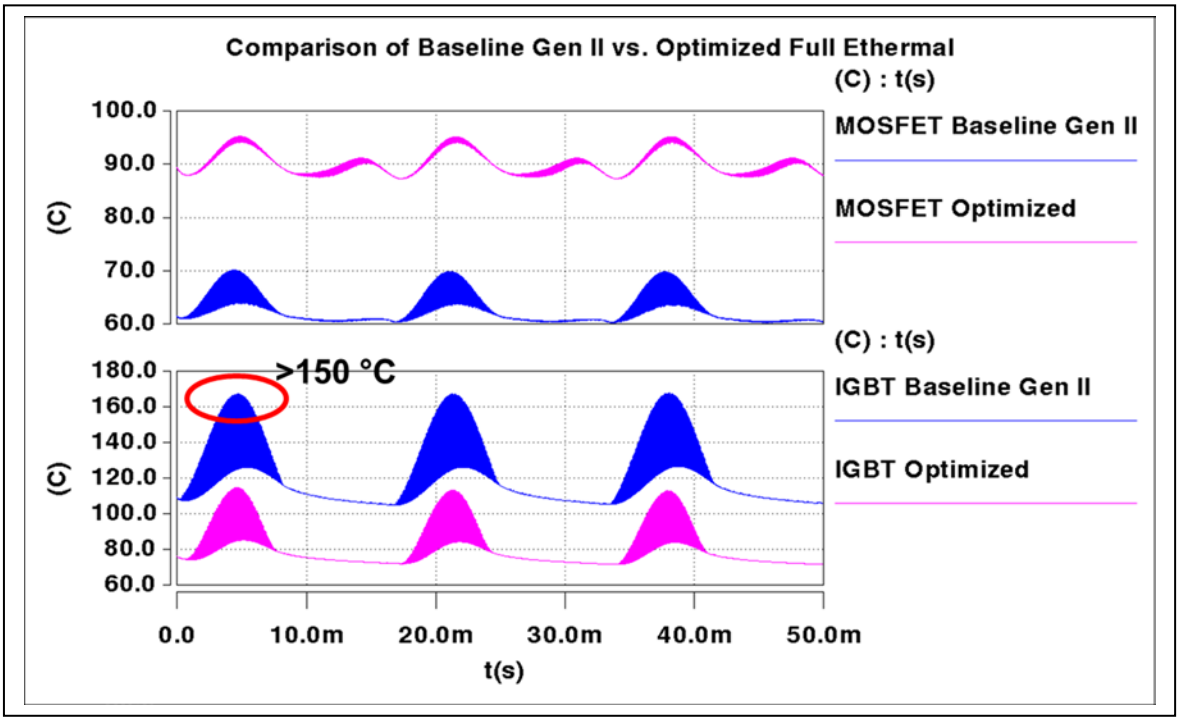

Fig. 7-26 Comparison of Baseline Gen II vs. Optimized Design – Full Electro-thermal

Chapter 8 Conclusions and Future Work

8.1 Conclusions

This dissertation developed a tool for design optimization through electro-thermal simulation. A process whereby a library of dynamic electro-thermal component models parameterized in terms of electrical, structural and material properties were used to optimize the design of a hybrid soft-switching inverter. The entire process was streamlined by separating the analysis into three separate simulations. An automated post processing tool was developed suing the output of each of the three analyses to determine the optimal design variables. The design variables included the IGBT chip area, the MOSFET chip area, external resonant capacitor and inductor and finally the cooling convection coefficient. The optimal design was pursued subject to design constraints such as transformer reset condition, minimum on-time consideration, and maximum chip area. A full design space of chip areas was considered such that an optimal design was achievable.

Electro-thermal model device parameters were extracted over temperature and used were used as inputs into existing simulation library component models where a scalable chip area parameter is made available for parametric study. Validation with measurement was achieved for the device models under switching and static conditions. The proposed thermal model used finite differences to solve the heat conduction equation and directly couple into the electro-thermal simulation without the need for extra synthesis steps. This offers the best and most flexible solution when it comes to design optimization. Using finite difference methods have yet to be attempted by many of the current literature due to fear of simulation and computation time. Using the process proposed in this dissertation, simulating using actual finite differences was shown to be achievable with very reasonable simulation times. The FDM model was first used

with average switching loss calculated over a switching period such that the simulation time step could run on the order of milliseconds. The steady state result of this simulation could then be used as an initial condition for a full electro-thermal simulation where the simulation time step can be reduced to microseconds. This allows one to study the effects of the dissipated power during the switching event as well the instantaneous junction temperature. Since the correct initial condition is used, the entire inverter can reach thermal steady state in a minimum of one line cycle.

The FDM model was validated against measured data resulting from a newly developed high-speed double chip temperature-sensitive parameter (TSP) transient measurement. By using the device threshold voltage as a time-dependent TSP, the thermal transient of a single device, along with the thermal coupling effect among nearby devices sharing common (DBC) substrates, can be studied under a variety of pulsed power conditions.

The process developed in this dissertation was used to compare an existing soft-switching module design. The existing module was based on the generation II freedom car module from Virginia Tech. The result of the optimization process recommended a design where heat could be better distributed avoiding “hot-spots”, which drive cooling requirements, by recommended more percentage of MOSFET chip area and reduced diode and IGBT area. The result was a **16%** improvement in device loss, and a **42%** reduction in required cooling convection coefficient.

In conclusion, this dissertation pulled every aspect of electro-thermal modeling together creating a process where the engineer can gain valuable insight early on in the design phase. The tool makes electro-thermal simulation very flexible and practical for engineers. No longer is electro-thermal simulation just used to predict temperatures but now as a way to make valuable recommendations to the engineer in a very reasonable amount of time.

8.2 Future Work

While this dissertation presented a process for optimizing the design of a hybrid soft-switching inverter by considering the device chip areas and external circuit parameters, the power of the thermal component models were not used to optimize module layout. This process could certainly be extended to module layout. The thermal boundary conditions for example could be used to minimize the overall device package.

Also, while this dissertation focused on the design of a hybrid soft-switching inverter, the process could certainly be extended to other topologies. Soft-switching is not a pre-requisite by any means. Any power electronics applications where semiconductors are used are candidates for optimization through electro-thermal simulation.

Another consideration is different operating temperatures. The tool defines the operating temperature as an input making the temperature a candidate for parametric evaluation to determine the best design if the module may operate over many different temperatures.

Other design considerations may involve the magnetic design. Constraints could be imposed constraining peak currents seen by the resonant inductor for example. This would drive the auxiliary switch and resonant capacitor along with minimum on-time consideration.

The possibilities are endless when it comes to design optimization using electro-thermal simulation.

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