Smart Power Module for Distributed Sensor Power Network of an Unmanned Ground Vehicle

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Abstract

Energy efficiency is a driving factor in modern electronic design particularly in power conversion where conversion losses directly set the upper limit of system efficiency. A wide variety of commercially available DC-DC conversion elements have efficiencies in the 90-97% range. The efficiency range of most common commercial-off-the-shelf (COTS) power supplies is 75-85%, highlighting the fact that COTS power supplies have not kept pace with efficiency improvements of modern conversion elements.

Unmanned ground vehicles (UGVs) is an application where efficiency can be crucial in extending tight power budgets. In autonomous ground vehicles, geographic diversity with regard to sensor location is inherent because sensor orientation and placement are crucial to performance. Sensor power, therefore, is also distributed by nature of the devices being supplied.

This thesis presents the design and evaluation of a smart power module used to implement a distributed power network in an autonomous ground vehicle. The module conversion element demonstrated an average efficiency of 96.7% for loads from 1-4A. Current monitoring and an adjustable output current limit were provided through a second circuit board within the same module enclosure. The module processing element sends periodic updates and receives commands over a CAN bus. The smart power modules successfully supply critical sensing and communication components in an operational autonomous ground vehicle.

Acknowledgments

I thank God above all who sustains my life and continues to bring every work of mine to completion. I must thank my father and mother who have provided a true example of love, hard work and heroic sacrifice throughout my life. Their continual support and encouragement has been with me through every stage of my education. Finally, I thank my 3 sisters and 6 brothers who are each a blessing to me and have taught me how to live as a blessing for others. *Totus tuus ut prosim* (totally yours that I may serve).

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List of Acronyms

Acronym	Definition
AC	Alternating Current
BGA	Ball Grid Array
CAN	Controller Area Network
CMMR	Common Mode Rejection Ratio
CMOS	Complementary Metal–Oxide–Semiconductor
COTS	Commercial Off-The-Shelf
DARPA	Defense Advanced Research Projects Agency
DC	Direct Current
DPS	Distributed Power System
ESR	equivalent series resistance
FET	Field Effect Transistor
GPIO	General Purpose Input/Output
GPS	Global positioning system
GUSS	Ground Unmanned Support Surrogate
I/O	Input and Output
IC	Integrated Circuit
IMU	Inertial Measurement Unit
INS	Inertial Navigation System
LED	Light Emitting Diode
LGA	Land Grid Array
LIDAR	Light Detection and Ranging
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSOP	Micro Small Outline Package
NMOS/NMOSFET/N-FET	N-Channel Metal Oxide Semiconductor Field Effect Transistor
OCU	Operator Control Unit
PMOS/PMOSFET/P-FET	P-Channel Metal Oxide Semiconductor Field Effect Transistor
PPU	Power Processing Unit
PWM	Pulse Width Modulation
SISO	Single Input Single Output
SMPS	Switching Mode Power Supply
SOIC	Small Outline Integrated Circuit
SPDT	Single-Pole Dual-Throw
TSSOP	Thin Shrink Small Outline Package
TVS	Transient Voltage Suppression
UGV	Unmanned Ground Vehicle
ZVS	Zero Voltage Switching

Chapter 1: Motivation for distributed sensor power

This section examines the feasibility of implementing a distributed network of power supplies so that each sensor can receive regulated power from a converter in close proximity. A literature review presents developments in distributed power supply (DPS) architectures from 1986 onward. The advantages a distributed approach are reduced transmission losses, efficiency improvement, superior thermal performance and tighter voltage regulation. Advances in DPS capabilities have always been driven by applications requirements, particularly low voltage computing needs. Sensor power is the application of interest in this work. In order for such a power network to be practical, the size of the conversion elements would have to be small in comparison to the sensors so that they could be conveniently placed. A certain amount of uniformity in the sensor power needs would also be required so that a standard conversion element could supply the full sensor suite.

Important terms are then defined in the context of this work. A wired power system is one where a conduction path is established between the supply and load through non-permanent connection points. Commercial off-the-shelf is used to represent a device that is available for purchase and able to interface directly with a wired power system. A power supply is considered to be a complete energy conversion device built around a conversion element and able to interface to a wired power system. A conversion element cannot interface directly with a wired power system and this quality distinguishes a conversion element from a power supply. The power supply developed in this work is defined as a smart power module by nature of its two distinct circuit board components.

A survey of power requirements is presented for the sensors used in the top place finishers of the DARPA Urban Challenge. The results show that the necessary uniformity is present in sensor power requirements with the majority of sensors drawing less than 50W. This fairly low power level also lends itself to the use of small conversion elements, making the requirement of convenient placement attainable.

Publications from the Urban Challenge provided a degree of detail into vehicle sensors unavailable for the most recent Unmanned Ground Vehicles (UGVs) in development. One exception being the Ground Unmanned Support Surrogate (GUSS) vehicle because it was developed by the Virginia Tech Unmanned Systems Lab and TORC Technologies. The sensor power needs of GUSS are presented providing insight into power requirements of a post Urban Challenge UGV which support the above trend. The experience gained through the development of GUSS further emphasizes the need for improved conversion efficiency and physical distribution of heat sources for thermal performance.

1.1 Literature review

Distributed power systems have been a growing area of research since the mid 1980's. Two excellent overviews of distributed power architectures are presented in [1] and [2]. Centralized power systems are defined as having one conversion stage in one physical location from which multiple outputs are generated and bussed to various loads [1]. In contrast to centralized power, distributed power systems are characterized by division of power processing functions among many power processing units (PPUs) [2]. The advantages of a distributed power approach include improved thermal management, space savings, reduced EMI, modularity, system flexibility and improved regulation at points of load[1][2][3].

The avionics industry made the first widespread use of distributed power systems motivated by reductions in wiring complexity, size and weight [4]. Gradually, as digital technology required new and more numerous voltage levels distributed power became attractive for other markets. Distributed power is presented in [5] as an improved means of supplying 5 V and 12 V inputs to digital switches used in the telecommunications industry in 1986. At these low voltages, it became impractical to send high currents over the long distances from the plant to the switches located in separate rooms. Published in 1991, [4], not only correctly predicted the continued growth of distributed power but also the cause speculating that the computer industry would serve as the impetus for distributed power architectures.

Throughout the 1990s and into the present distributed power architectures have advanced to meet the stringent power demands of emerging computers[6][7][8]. Advanced sub-micron CMOS technology emerged in the early 90's changing the power supply requirements from traditional +5Vdc and +3.3V supplies to multiple non-standard low voltage supplies (2.5V,1.8V, 1.2V, etc.) with high load currents being demanded by advanced microprocessors [6]. Introduction of energy saving features pushed power supplies to the limit as the load step transient waking out of low power sleep modes could span 10% to 90% of the converters rated load [7]. Despite these rapid and severe load transients, voltage regulation of ±2% was demanded [7]. Considerations for power supplies to meet these stringent requirements are presented in [8] emphasizing that converters must be located next to their loads. Meeting these challenges has led to significant advances in DC-DC conversion technology.

It was further recognized in [7] that on board power modules can regulate only one point via remote sense so that even a distributed power approach was limited. This has led to multiple converters being required on a single printed circuit board at each point of load (POL). The spectrum of distributed power supplies now spans from separations of hundreds of feet down to inches of separation for high performance POL converters located on the same circuit board.

Implementation of distributed power architectures has always been application specific and motivated by performance improvement. Modern DPS converters have been shaped, most significantly, by low voltage processing advances only made possible by advances in DPS capabilities. The cutting edge of DPS converters have evolved to meet specific needs overlooking some applications where DPS architecture is desired but economic considerations are an overriding factor [2]. Distributed sensor power, the focus of this work, is one such application. The challenge has been to adapt modern, high efficiency conversion elements to make them suitable for UGV sensor power applications. The crux of the problem is that the desired, commercially available, conversion elements are designed to interface directly with printed circuit boards.

Because sensors are most often pre-packaged with existing connectors a sensor power supply must be packaged with connectors in order to interface. If the target load resided on a custom printed circuit board, full advantage could be taken of the desired conversion elements. This work presents the process of integrating a state of the art DPS conversion element into the sensor power system of an unmanned ground vehicle.

1.2 Definition of terms

As stated in the preceding section, distributed power architectures are implemented in relation to a specific application. Several terms used in this work must be defined in within a context of distributed sensor power in an unmanned ground vehicle. A wired power system is one in which the power supplies are connected to loads by a conductor held in place by non-permanent connectors. This means that a connectorized wiring harness is preset between supply and load rather than both residing on the same printed circuit board.

COTS stands for commercial off-the-shelf. The definition of COTS is examined in [9] which concludes that COTS has to remain a term of broad coverage. Three attributes presented in [9] are applicable to the use of COTS in this work. The device exists a priori, is available to the general public and can be bought or leased [9]. “Commercial” is the key aspect of COTS devices, that is, they are available for sale to the general public. “Off-the-shelf” needs some further definition. The term COTS in [9] encompasses both devices that are functional without modification from the user and those that must be modified and configured before function. This thesis endeavors to present definitions based on the user experience associated with implementation. This work defines off-the-shelf as something that can perform its desired function without requiring any physical modification by the user. If a device can be purchased and placed into a system without alteration it is considered a COTS device. Otherwise it is only a commercial device because it is not functional off-the-shelf.

The terms power supply and converter are used interchangeably to denote a device that converts electrical energy from one form to another. Both converters and power supplies are considered complete entities which perform a desired function. A conversion element refers to the base device about which a converter is realized. Conversion elements do not perform their desired function without the addition of external components.

The conversion element is the central component of every power supply but does not constitute a power supply in itself. A conversion element is often an integrated circuit which is not designed to interface directly with a wired powers system. However, when combined with external components and connectors, a conversion element becomes a complete power supply. In some cases, a half brick converter for example, all components of a functioning converter are contained within one package. This would still be considered a conversion element because it cannot interface directly with a wired power system. This is illustrated in Figure 1. The half brick converter could function unmodified if alligator clips were attached to the pins but, for all practical purposes, is only useful after the addition of a custom printed circuit board. This distinction is arises because of the specific application of UGV sensor power.

Figure 1. Half brick conversion element and custom circuit board photo by author, 2014.

A smart power module is a device that combines a power supply with additional features such as output protection and current limiting. The power supply circuit board is separate from the printed circuit board which enables the additional features so that the two boards are distinct, modular, components. For this reason, the distributed power supply developed in this work is called a smart power module rather than a smart power supply.

1.3 Power environment of UVG sensors

In unmanned ground vehicle applications, closely regulated DC power is only required by certain delicate components such as sensors and communications equipment. Hardier components such as actuators and motor controllers can tolerate the variations in voltage of an unregulated bus. In a UGV, physical separation between sensors, unavoidable in achieving a complete field of view, is often on the order of the full vehicle length. Traditionally, sensors receive power from a regulated converter in a centralized location, which is capable of supplying the full sensor current load. Voltage regulation is one drawback of this centralized approach as sensors further from the source experience the greater voltage drop across long wire lengths. Adequate heat dissipation presents, perhaps, the most serious drawback of a centralized converter. Because the converter supplies the full sensor load, heat dissipation is both large and concentrated in a central location, often requiring removal by active cooling.

A brief examination of the typical sensor power requirements in an unmanned ground vehicle shows that a distributed power network has many advantages over a centralized approach. The input power needed by individual sensors is generally small, less than 50W. If 10 sensors each drawing 50W are supplied by a single DC-DC converter with 85% efficiency, 75W of heat would have to be removed from the converter. If, instead, each sensor was powered by a single DC-DC converter in close proximity, only 7.5W of heat would be removed from each converter. Though the losses are the same, cooling is greatly simplified as the geographic separation allows the 7.5W heat sources to be cooled individually. Thermal design is simplified since less power is dissipated in each unit [2]. By distributing the sources, of heat generation thermal management can take advantage of conducted and radiated cooling, sometimes eliminating the need for air moving equipment [1]. Wiring losses are also reduced due to the close proximity of the power supplies to their loads.

1.4 Survey of sensor power in DARPA Urban challenge

The 2007 DARPA Urban Challenge has provided research papers detailing the design, construction and operation of the autonomous ground vehicles, which competed[10][11][12]. The top three competition vehicles are considered here. Finishing first place, Boss, was built by the Tartan Racing team, which was composed of students, staff, and researchers from several entities, including Carnegie Mellon University, General Motors, Caterpillar, Continental, and Intel [10]. Junior, the second place finisher, was built by Stanford University. Finishing third place was Odin built by Team Victor Tango, a partnership between Virginia Tech and TORC Technologies.

Of particular interest, these papers list the primary sensors used to achieve autonomous operation. Table 1[10][11][12] shows the sensors used for perception and autonomy in Boss, Junior and Odin. Where possible, the maximum power draw has been listed for each sensor as identified from respective datasheets. The power requirements range from 1.25W to 60W. Excluding the 60W Applanix GPS/IMU used in Boss, the remaining sensors require less than 50W individually. All the sensors operate from either12V or 24V inputs.

Table 1. Survey of sensor power requirements for sensors used in DARPA Urban Challenge C. Urmson, J. Anhalt, D. Bagnell, C. Baker, R. Bittner, M. N. Clark, J. Dolan, D. Duggins, T. Galatali, C. Geyer, M. Gittleman, S. Harbaugh, M. Hebert, T. M. Howard, S. Kolski, A. Kelly, M. Likhachev, M. Mcnaughton, N. Miller, K. Peterson, B. Pilnick, R. Rajkumar, P. Rybski, B. Salesky, Y. Seo, S. Singh, J. Snider, A. Stentz, W. R. Whittaker, Z. Wolkowicki, J. Ziglar, H. Bae, T. Brown, D. Demitrish, B. Litkouhi, J. Nickolaou, V. Sadekar, W. Zhang, J. Struble, and M. Taylor, "Autonomous driving in urban environments : Boss and the urban challenge," *J. F. Robot.*, vol. 25, no. February, pp. 425–466, 2008. Used with permission of John Wiley and Sons, 2014. M. Montemerlo, J. Becker, S. Bhat, H. Dahlkamp, D. Dolgov, S. Ettinger, D. Haehnel, T.Hilden, G. Hoffmann, B. Huhnke, D. Johnston, S. Klumpp, D. Langer, A. Levandowski, J.Levinson, J. Marcil, D. Orenstein, J. Paefgen, I. Penny, A. Petrovskaya, M. Pflueger, G.Stanek, D. Stavens, A. Vogt, S. Thrun, S. Artificial, and S. Cs, "Junior : The Stanford Entry in the Urban Challenge," *J. F. Robot.*, vol. 25, no. 9, pp. 569–597, 2008. Used with permission of John Wiley and Sons, 2014. A. Bacha, C. Bauman, R. Faruque, M. Fleming, C. Terwelp, C. Reinholtz, D. Beach, T. Alberi, D. Anderson, S. Cacciola, P. Currier, A. Dalton, J. Farmer, J. Hurdus, S. Kimmel, P. King, A. Taylor, D. Van Covern, and M. Webster, "Odin : Team VictorTango ' s Entry in the DARPA Urban Challenge," *J. F. Robot.*, vol. 25, no. 8, pp. 467–492, 2008. Used with permission of John Wiley and Sons, 2014.

Vehicle	sensor	voltage (V)	max current (A)	max power (W)
Boss	Applanix POS-LV 220/420 GPS/IMU	10-34	-	60
	SICK LMS 291-S05/S14 LIDAR	24	1.8	43.2
	Velodyne HDL-64 LIDAR	12	4	48
	Continental ARS 300 Radar	14	0.5	7
	IBEO Alasca XT LIDAR	12	1	12
	Point Grey Firefly	24	0.05	1.25
	Velodyne HDL-64 LIDAR	12	4	48
Junior	SICK LMS 291-S14	24	1.8	43.2
	RIEGL LMS-Q120	24	2	48
	SICK LD-LRS range scanner	24	1.5	36
	IBEO Alasca XT LIDAR	12	1	12
	BOSCH Long Range Radar (LRR2)	12	0.18	2.16
Odin	IBEO Alasca XT LIDAR	12	1	12
	SICK LMS 291	24	1.8	43.2
	IEEE 1394 color camera	24	1.5	36
	Novatel Propak LB+ GPS/INS	12	0.31	3.7 (typical)

Diversity of sensor placement is illustrated in Figure 2 [10][11][12] with sensors mounted to the roof, front, rear and sides of the three cars. The orientation and location of each sensor was carefully chosen to achieve a desired field of view. Placement was dictated by the autonomy capability and the maximum separation between sensors is on the order of the full vehicle lengths. Front and rear sensors are placed almost 174 inches (14.6ft) apart in the case of Odin and up to 202 inches (17ft) for Boss [13],[14].

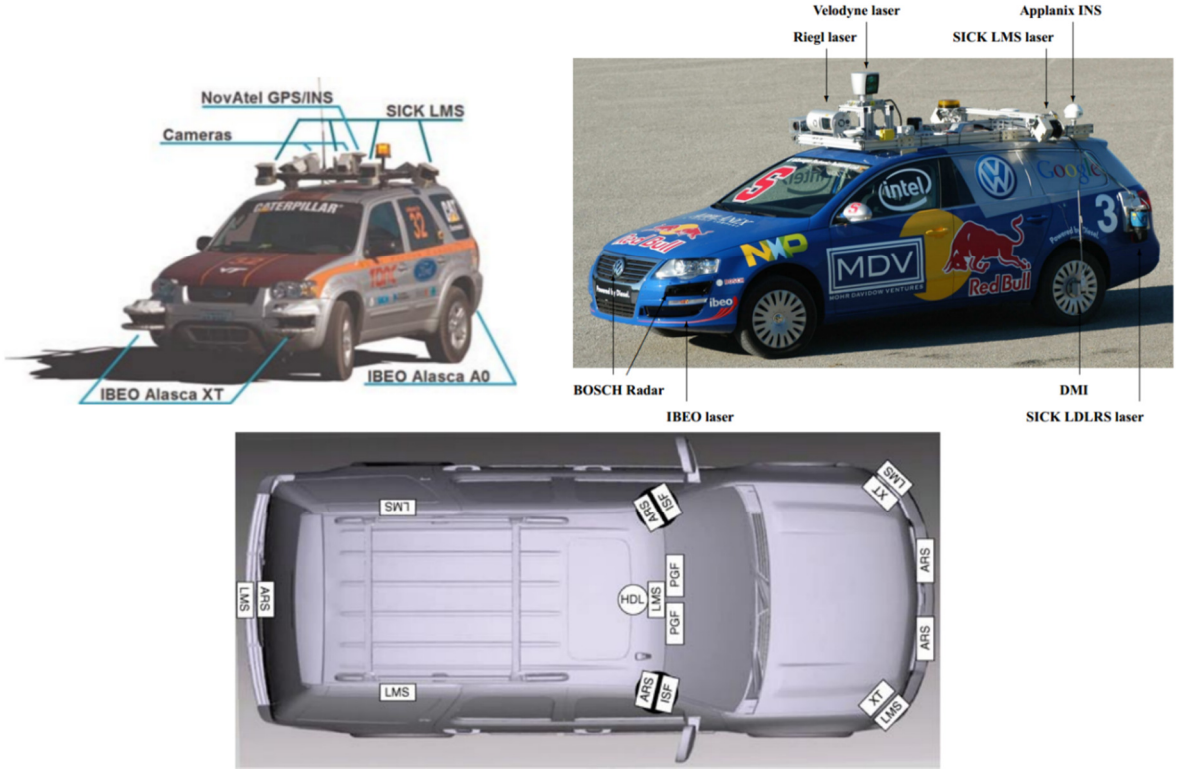


Figure 2. Sensor placement on the three winning vehicles of the 2007 DARPA Urban Challenge. Odin (top left), Junior (top right) and Boss (bottom) C. Urmson, J. Anhalt, D. Bagnell, C. Baker, R. Bittner, M. N. Clark, J. Dolan, D. Duggins, T. Galatali, C. Geyer, M. Gittleman, S. Harbaugh, M. Hebert, T. M. Howard, S. Kolski, A. Kelly, M. Likhachev, M. Mcnaughton, N. Miller, K. Peterson, B. Pilnick, R. Rajkumar, P. Rybski, B. Salesky, Y. Seo, S. Singh, J. Snider, A. Stentz, W. R. Whittaker, Z. Wolkowicki, J. Ziglar, H. Bae, T. Brown, D. Demitrish, B. Litkouhi, J. Nickolaou, V. Sadekar, W. Zhang, J. Struble, and M. Taylor, "Autonomous driving in urban environments : Boss and the urban challenge," *J. F. Robot.*, vol. 25, no. February, pp. 425–466, 2008. Used with permission of John Wiley and Sons, 2014.
M. Montemerlo, J. Becker, S. Bhat, H. Dahlkamp, D. Dolgov, S. Ettinger, D. Haehnel, T.Hilden, G. Hoffmann, B. Huhnke, D. Johnston, S. Klumpp, D. Langer, A. Levandowski, J.Levinson, J. Marcil, D. Orenstein, J. Paefgen, I. Penny, A. Petrovskaya, M. Pflueger, G.Stanek, D. Stavens, A. Vogt, S. Thrun, S. Artificial, and S. Cs, "Junior : The Stanford Entry in the Urban Challenge," *J. F. Robot.*, vol. 25, no. 9, pp. 569–597, 2008. Used with permission of John Wiley and Sons, 2014. A. Bacha, C. Bauman, R. Faruque, M. Fleming, C. Terwelp, C. Reinholtz, D. Beach, T. Alberi, D. Anderson, S. Cacciola, P. Currier, A. Dalton, J. Farmer, J. Hurdus, S. Kimmel, P. King, A. Taylor, D. Van Covern, and M. Webster, "Odin : Team VictorTango ' s Entry in the DARPA Urban Challenge," *J. F. Robot.*, vol. 25, no. 8, pp. 467–492, 2008. Used with permission of John Wiley and Sons, 2014.

The Urban Challenge literature, understandably, is centered on sensing and autonomy. Some information is given about the power systems of the three finishing vehicles, but no details are provided on specific power components. An auxiliary 24V DC system along with a 120V inverter were added to the native 12V battery bus in Boss[10]. The power server for Junior was located in the trunk of the vehicle, as shown in **Error! Reference source not found.** [11] . Perhaps the most important detail, it is stated that thermal management for Boss was achieved with the stock vehicle air conditioning system [10]. Use of native air conditioning for cooling purposes was commonplace for all the urban challenge vehicles. Modification was sometimes necessary. Specialized ducts had to be added to increase air flow cooling the trunk components of Stanley, the winning vehicle, of the previous DARPA Grand Challenge [15]. This represents a case where the stock air conditioning system was just sufficient to provide cooling for internal electronics.

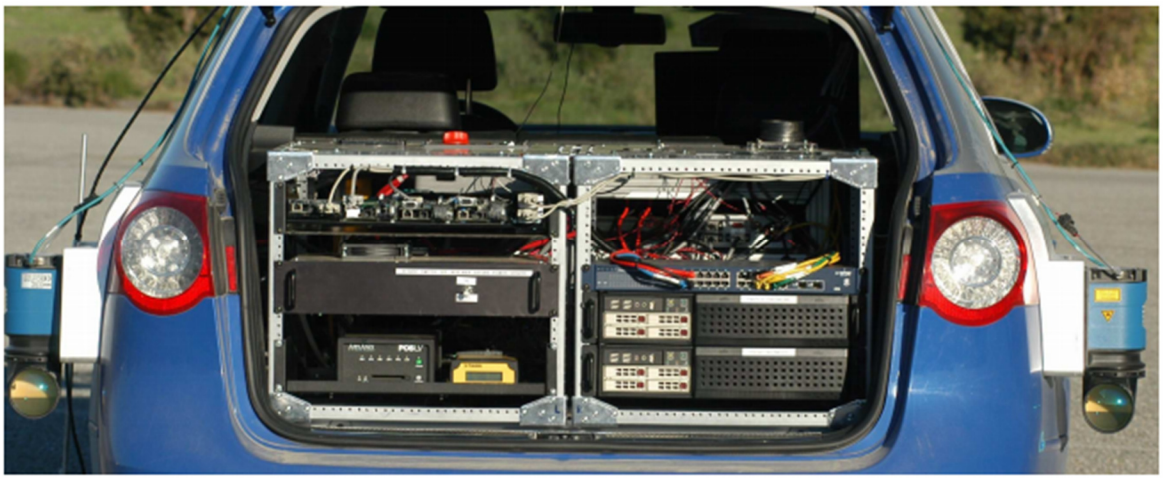


Figure 3. Power server located in rear of Junior vehicle. M. Montemerlo, J. Becker, S. Bhat, H. Dahlkamp, D. Dolgov, S. Ettinger, D. Haehnel, T.Hilden, G. Hoffmann, B. Huhnke, D. Johnston, S. Klumpp, D. Langer, A. Levandowski, J.Levinson, J. Marcil, D. Orenstein, J. Paefgen, I. Penny, A. Petrovskaya, M. Pflueger, G.Stanek, D. Stavens, A. Vogt, S. Thrun, S. Artificial, and S. Cs, "Junior : The Stanford Entry in the Urban Challenge," *J. F. Robot.*, vol. 25, no. 9, pp. 569–597, 2008. Used with permission of John Wiley and Sons, 2014.

1.5 GUSS Vehicle

The Ground Unmanned Support Surrogate (GUSS) became the direct beneficiary of the autonomy capabilities demonstrated by Virginia Tech and TORC Technologies during the DARPA Urban Challenge. GUSS was an autonomous vehicle designed to support a squad of dismounted marines in a variety of missions including resupply, "follow me," casualty evacuation and reconnaissance [16]. Built on an existing Polaris MVRS700 6x6, GUSS could operate autonomously or be driven directly by a human [17]. GUSS is shown in Figure 3 with the prominent sensors visible on the roll bar. The sensor power requirements of GUSS are shown in Table 2. Only one device, a PTZ camera, draws more than 50W. Overall, the trend is toward smaller and lower power sensors with none of the large Sick LIDARs prevalent in the Urban Challenge.

Figure 3. GUSS vehicle Robot Living, "Automated Golf Carts Head To War," 2010. [Online]. Available: http://www.robotliving.com/military/automated-golf-carts-head-to-war/. Used under fair use, 2014

Table 2. Sensor power requirements for GUSS vehicle

ITEM	Voltage (V)	Current (A)	Power (W)
Camera	24.5	3.0	73.5
Sick 1	13.0	0.6	7.8
Sick 2	13.0	0.6	7.8
Sick 3	13.0	0.6	7.8
Velodyne	13.0	1.0	13.0
GPS IMU	13.0	0.5	6.5
Localization Board	13.0	0.5	6.5
Waysight	13.0	0.5	6.5
Radio	13.0	3.0	29.0
Operator control unit	13.0	2.5	32.5

Cooling for electronic components became a significant concern now that the base vehicle was an open frame Polaris without an air conditioning system to provide convenient heat removal. The situation was compounded by the close proximity of the power supplies to the vehicle computers. Cooling was accomplished through the addition of heat exchangers and fans, which ultimately comprised 14% of the total vehicle power load.

The experience gained from GUSS highlighted the importance of power supply efficiency and location in autonomous ground vehicle performance. Efficiency is the most fundamental way to reduce losses and extend vehicle power budget. Thermal concerns are also mitigated in that less heat is lost in conversion. The location of power supplies also plays a crucial role in determining the cooling requirements. Even with low losses, a centralized supply may require special cooling if sensor power draw is large. Splitting up power supplies and locating them close to the spatially diverse sensors can eliminate the need for active cooling entirely.

This section has examined state-of-the-art in terms of autonomous ground vehicle sensing and determined that the majority of sensors in use require less than 50W individually. Sensors

are inherently spread out across the chassis of autonomous ground vehicles in order to provide full fields of view. In a ground vehicle, this can equate to separations of up to 17 feet between sensors. While sensors are spatially distributed, power is generally centralized. A distributed approach to sensor power has the benefit of improved thermal performance through physical dispersion of heat sources. In order to be effective, the distributed power supplies would have to be small to afford convenient placement. Because the majority of sensors draw less than 50W, it is feasible to implement a distributed power network utilizing small, highly efficient, DC-DC conversion elements.

1.6 Overview of thesis

The remainder of this thesis presents the theory, design, and testing of a smart power module intended for use in a distributed power system. Chapter 2 provides a high-level overview of switching mode DC-DC conversion, covering both theory and practical implementation. Ideal switching mode power supplies (SMPS) are evaluated in steady state conditions, emphasizing the importance of switching action in voltage conversion. Next, some of the intricacies of realizing the practical converter are discussed including MOSFET switching sequences, gate drive considerations, feedback control and compensation techniques.

Chapter 3 presents the DC-DC converter in its practical form in which many of the components from Chapter 2 are combined in a single integrated circuit (IC). It is at this integrated circuit level, which most users will interact with a conversion element in a design process. All converter ICs can be classified as either internally or externally compensated devices. This fundamental distinction is explained and its implications for the user are discussed.

Required functionality and attributes are defined for the smart power modules at the start of Chapter 4 along with the six elements that comprise a smart power module. The remainder of Chapter 4 presents component selection and overall module design. The design methodology placed priority on physically demonstrating functionality supplemented by circuit simulation with design optimization given last priority. In this manner, a functioning smart power module was realized allowing optimization of system functions to follow in two subsequent revisions.

Chapter 5 covers results and the evaluation of the smart power modules. Efficiency, load regulation, output ripple, and thermal performance are measured for the conversion elements. Output current monitoring and current limiting features are implemented and tested. Inrush current spikes, which were discovered following installation in the vehicle, are discussed along with resulting adjustments to module operation. User interface and control through CAN is verified.

Lastly, Chapter 6 presents future work related to the smart power modules. These include expansion of current sampling capabilities to allow power health feedback and anomaly detection as well as general reduction of the processing power of each module. The smart power modules developed in this work are successfully supplying the power needs of an operational autonomous ground vehicle.

Chapter 2: Theory of DC-DC converter operation

A DC-DC converter is a device that receives a DC voltage input and produces a DC output at a different voltage level. DC-DC converters can be classified into three main categories based on their voltage transfer functions. If the output is always larger than the input then the device is a step-up or boost converter. If the output is always less than the input then the device is a step-down or buck converter. Lastly, if the output can be greater or less than the input, the device is a buck-boost converter.

In what follows, the theory and background of switching mode power conversion is presented. Switching is the fundamental action, which produces voltage conversion. Any desired input-output voltage relation can be achieved by changing the position of passive inductors and capacitors in relation to the switch [19]. The voltage transfer function for an ideal buck converter in steady state operation is derived as an example. The fundamental concept of SMP operation is not difficult to understand a DC voltage is broken into an AC waveform by a switching sequence, recombined through passive inductors and capacitors and filtered to produce a DC output at a different level.

After presenting a relatively straightforward theory, the intricacies involved in realizing a practical converter are discussed.

The basic theory of the MOSFET, which provides the crucial switching action, is reviewed. The charge controlled nature of the FET is established with regard to the multi stage ON-OFF transitions of the FET under clamped inductive switching. Switching losses are analyzed. Factors important to gate driver design are considered. The last section covers feedback control, stability and compensation. An intuitive understanding of feedback control is presented using insight from pulse width modulation (PWM) hardware. The basic feedback block diagram of a converter is established. Stability criterion and compensator design are discussed along with how to identify the three most common compensation schemes.

This chapter is intended to give the reader a solid grasp of what is being accomplished by each function of a DC-DC converter. Ultimately, the details of how these functions are accomplished are well outside the scope of this work. Though some of the most relevant, the practical considerations brought up here are by no means exhaustive. Their primary value is to provide awareness of the complexity of practical implementation which might otherwise be underestimated.

2.1 Steady state analysis of Ideal DC-DC converters

This section presents the basic operation of switched mode DC-DC converters. Voltage conversion, the purpose of the DC-DC converter, is accomplished through switching action, the fundamental mechanism of all switched mode topologies. The conversion process is presented beginning with a switch and, later, adding capacitors and inductors. Voltage and current waveforms are derived for the ideal buck converter operating in steady state. Though only the buck converter is analyzed, the methods presented are applicable to any topology.

The fundamental building block of every DC-DC converter is a single-pole dual-throw (SPDT) switch. The switching action drives the conversion and the orientation of the SPDT switch in relation to supporting components determines the voltage transfer function. The simplest principle of DC-DC conversion is illustrated by the single switch of Figure 4. The output voltage will equal the input voltage while the switch is connected to terminal 1 and equal

zero while the switch is connected to terminal 2. If the switch is connected to terminal 1 for a period of T1 and terminal 2 for a period of T2 the waveform on the right will be produced. A conversion has taken place because the average output voltage is less than the input over the switching cycle.

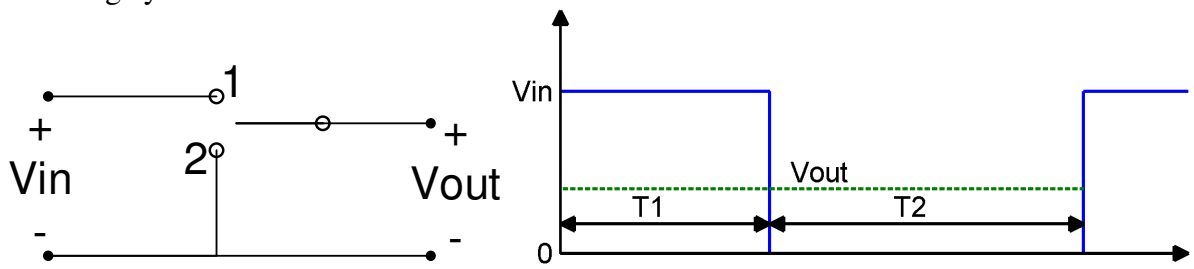


Figure 4.Basic step down converter from SPDT switch

The average voltage over the switching cycle is

$$V_{avg} = V_{out} = V_{in} * \frac{T_1}{T_1 + T_2} \quad \textbf{(1)}$$

It can be seen from (1) that a step-down conversion has been produced because the output is always less than or equal to the input voltage. To simplify further analysis, the switching cycle will hereby be described as a pulse width modulated (PWM) function in terms of a duty cycle D and period T.

The period T is defined as

$$T = T_1 + T_2 \quad \textbf{(2)}$$

The duty cycle is defined as

$$D = \frac{T_1}{T} \quad \textbf{(3)}$$

The circuit in Figure 4 is not a true DC-DC converter because the switching action has introduced a substantial AC component to the output. Therefore, it is necessary to remove this unwanted AC component with an output filter. Every DC-DC converter is, in actuality, a DC-AC-DC converter because of the switching action. Adding an output low pass filter to remove the AC component produces the basic SPDT switch model of the buck converter, shown in Figure 5.

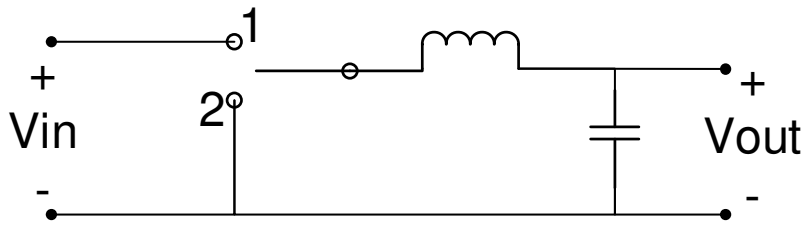


Figure 5. SPDT model of buck converter.

Even with the addition of a filter, it is not possible to completely remove the AC component at the switching frequency and its harmonics from the converter output [19]. Therefore, a small amount of ripple will always be present. Given that the purpose of the conversion is to produce a DC output, this AC ripple, for any well designed converter, must be very small in relation to the DC component, generally less than 1% [19]. This allows us to make use of the small ripple approximation.

$$v(t) = V_{DC} + v_{ripple}(t) \left\| v_{ripple}(t) \right\| \ll V_{DC} \tag{4}$$

$$v(t) \cong V_{DC} \tag{5}$$

Any signal v(t) is composed of a DC component V_{DC} and a ripple component $v_{ripple}(t)$. The small ripple approximation states that the signal can be approximated by its DC component only because the magnitude of V_{DC} is much greater than that of $v_{ripple}(t)$. The steady state operation of the buck converter will now be analyzed for a resistive load using the small ripple approximation. Two circuits are formed depending on the position of the switch as shown in Figure 6.

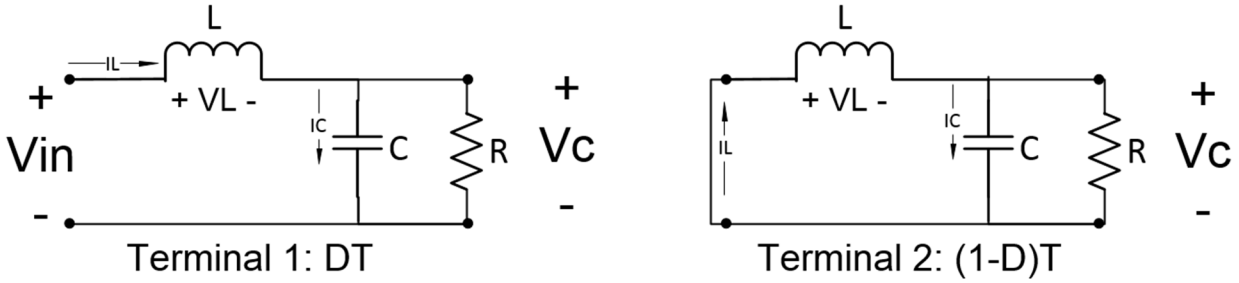


Figure 6. Two circuits formed during buck converter switching period

The inductor voltage during the time interval DT is equal to

$$V_L = V_{in} - V_C \tag{6}$$

During the interval (1-D)T, the inductor voltage VL is

$$V_L = -V_C \tag{7}$$

The relation between voltage and current for an inductor is

$$V_L = L\frac{di_L}{dt} \tag{8}$$

Using (8), we can find the changes in inductor current for each period. For the time interval DT, the slope of the inductor current will be

$$\frac{di_L}{dt} = \frac{V_{in} - V_C}{L} \tag{9}$$

Since the inductor voltage is constant under the small ripple approximation, the slope of the inductor current is also constant. The current will increase linearly during the period DT. For the period (1-D)T, the current slope is

$$\frac{di_L}{dt} = \frac{-V_C}{L} \tag{10}$$

Thus, the inductor voltage decreases linearly over the period (1-D)T with the slope found in (10). The inductor current and voltage waveforms are shown in Figure 7.

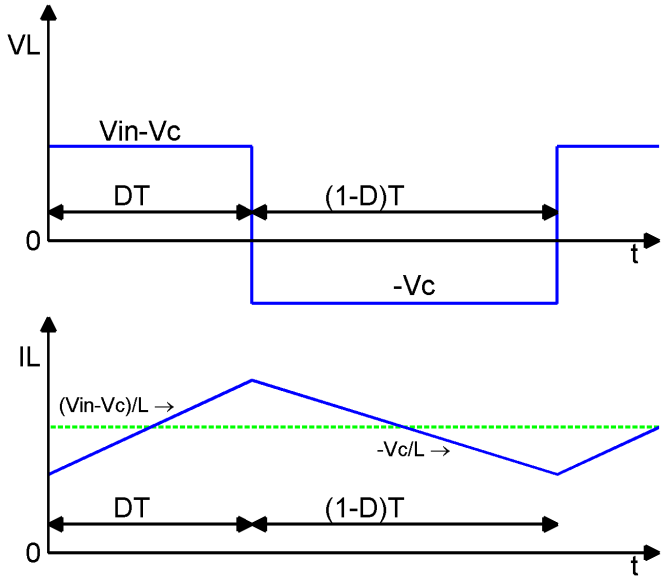


Figure 7. Steady state inductor voltage and current waveforms

The steady state current waveform is periodic and, thus, the inductor current at the beginning of the cycle is equal to the inductor current at the end of the cycle. From (8), we can relate the change in inductor current over one cycle to the change in inductor voltage over one cycle from nT to (n+1)T.

$$0 = i_L((n+1)T) - i_L(nT) = \frac{1}{L}\int_{nT}^{(n+1)T} V_L(t)dt \quad (11)$$

Since the left hand side of (11) is equal to zero, the integral of inductor voltage VL must also be zero. This principle is called inductor volt-second balance so named because (11) has the units of Volt seconds. This principle is intuitive because the inductor current would continuously increase if the integral of inductor voltage were not zero for a full cycle[20]. The same principle holds for the current flowing through the output capacitor in steady state the change in voltage over one cycle must be zero. This is called the principle of capacitor charge balance.

$$0 = V_C((n+1)T) - V_C(nT) = \frac{1}{C}\int_{nT}^{(n+1)T} i_C(t)dt \quad (12)$$

Volt second balance now provides a simple means of finding the voltage transfer function of the buck converter. We now know that the product of voltage and time for the inductor must sum to zero over the cycle. (13)

$$(V_{in} - V_c) * DT + (-V_C) * (1-D)T = 0$$

$$DV_{in} - DV_C - V_C + DV_C = 0 \quad (14)$$

$$\frac{V_c}{V_{in}} = D \quad (15)$$

The voltage transfer function (15) is identical to that found in (1) The small ripple approximation cannot be used to find the output voltage ripple for a two-pole low pass filter as is the case with the output of a buck converter [19]. The DC current will flow only into the load resistance while the AC current ripple will flow through the load resistor and the output capacitor. For a properly designed converter, the capacitor impedance at the current ripple frequency will be much smaller than the impedance of the load so that nearly all ripple current flows into the capacitor. The current waveform of the capacitor therefore will be the same as the inductor current waveform with the DC component removed as shown in Figure 8.

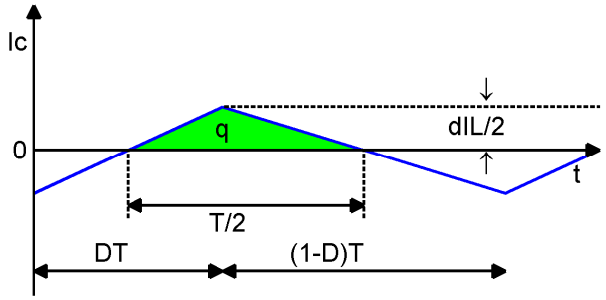


Figure 8. Capacitor current waveform

A charge q is stored in the capacitor over the interval T/2 during which the ripple current is positive. The charge is equal to the integral of the capacitor current over the time interval T/2, which is the area of the green triangle.

$$q = \frac{1}{2} * \frac{dI_L}{2} * \frac{T}{2} \tag{16}$$

The relation between charge and voltage for a capacitor is

$$Q = CV \tag{17}$$

The charge is related to the change in capacitor voltage by

$$q = C * dV_C \tag{18}$$

Using (16) and (18), the change in capacitor voltage is found to be

$$dV_C = \frac{dI_L T}{8C} \tag{19}$$

It is possible to produce any desired DC output using a passive network of inductors, capacitors and embedded switches [19]. The three most common DC-DC converters are shown in Figure 9 with their conversion ratios as a function of duty cycle. The boost converter produces an output, which is always higher than the input. The buck-boost converter produces an output of opposite polarity that is either higher or lower than the input voltage. It is important to note that each of these DC-DC topologies is composed of only capacitors inductors and an SPDT switch. In their ideal form, these elements are not dissipative and, thus, the theoretical efficiency of these DC-DC converters is 100%. Though many non-idealities are present in practical converters, advances in semiconductor design and converter control are pushing real efficiencies ever closer to the lossless ideal.

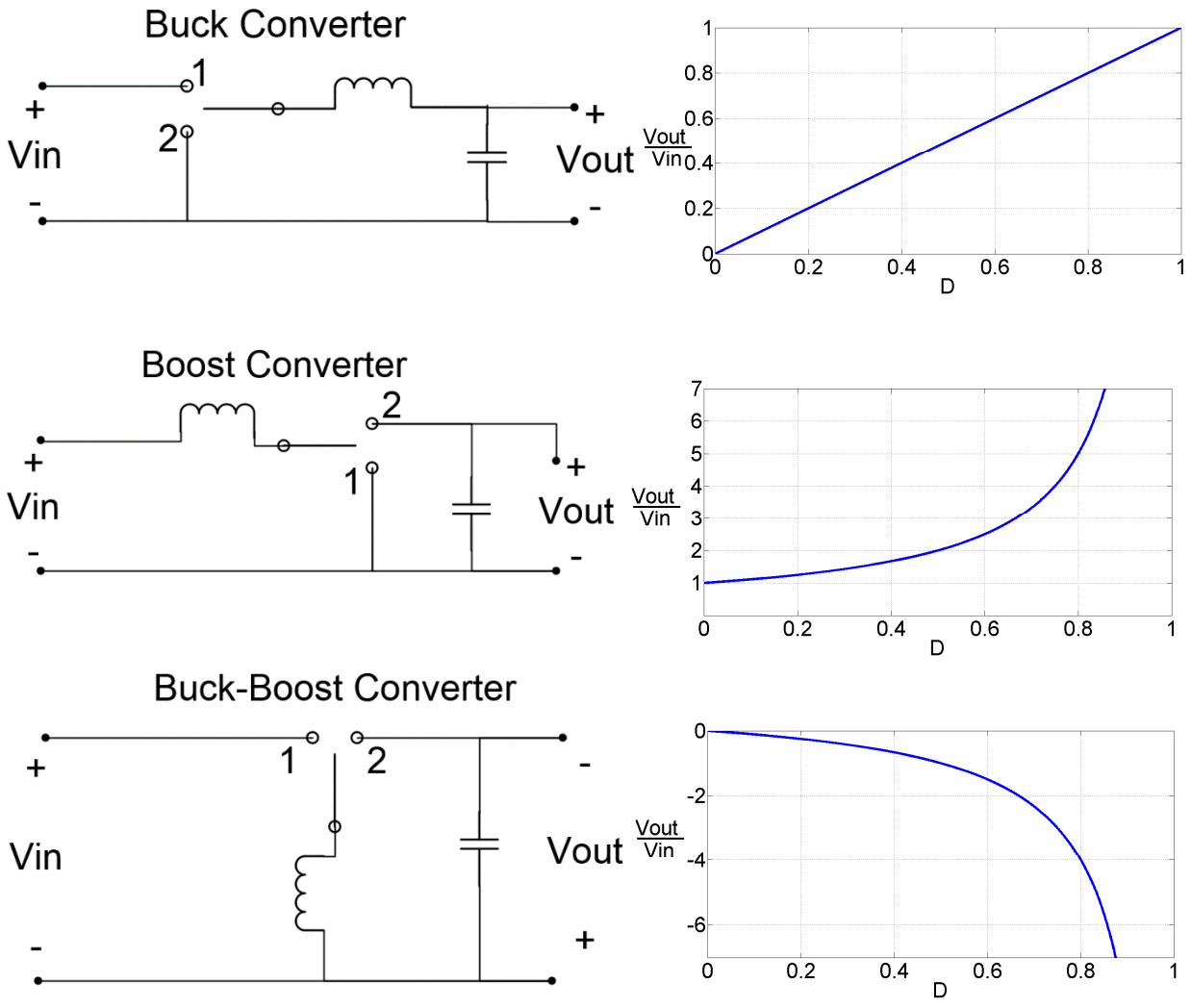


Figure 9.Three ideal DC-DC converter models showing SPDT switch location and orientation. The ideal voltage conversion ratio is shown for each converter as a function of duty cycle.

Ideal switching mode DC-DC conversion is not complicated to understand. DC voltage is broken into an AC waveform through a switching action, manipulated by a network of passive components and filtered to extract a desired DC output. On the surface, the concept does not seem daunting. The crucial transition from theory to real world application is an art that can take the power supply designer a lifetime to master.

2.2 SPDT switch realization

The SPDT switch is realized using discrete components either a transistor and diode pair or a pair of transistors. When a diode is paired with a transistor, the converter is called "asynchronous" because the diode will conduct while the FET is in the cut-off region and block current while the FET conducts. In this manner, the diode is a passive terminal that does not require any synchronization with the FET gate drive signal. A second FET can be used in place of the diode in what is called a "synchronous" converter. For this case, both FETS must be actively driven with synchronized signals that are inverted with respect to each other.

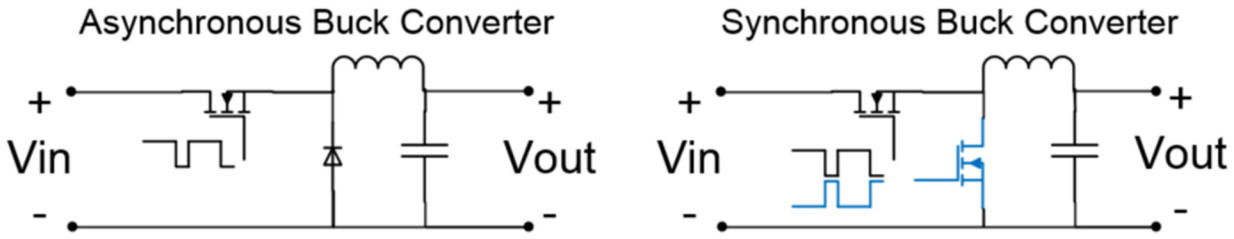


Figure 10. Asynchronous and Synchronous realization of the buck converter SPDT switch

2.3 Basic MOSFET operation

MOSFET is an acronym for Metal Oxide Semiconductor Field Effect Transistor. The MOSFET is a charge controlled semiconductor device. There are four different basic types of MOSFETs: n-channel enhancement mode, p-channel enhancement mode, n-channel depletion mode, and p-channel depletion mode. The basic composition of an n-channel enhancement mode MOSFET (or NMOSFET) is shown in Figure 11 a large substrate of P-type semiconductor contains two smaller regions of N-type semiconductor separated by a channel length L. A metal layer called the gate terminal is insulated from the channel substrate to form a capacitor. Metal terminals called the drain and source are directly connected to each of the N-type regions. A fourth metal layer, the body terminal, is connected to the substrate base. The NMOSFET symbol with its four terminals G, D, S and B is shown on the right of the image.

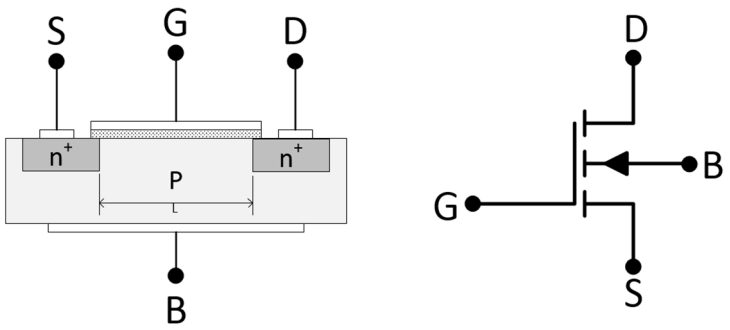


Figure 11.NMOS transistor with cross sectional view and circuit symbol

The charge of the gate capacitor controls the conductivity of the channel region. When the voltage difference between the Gate and Source terminals reaches a critical threshold called V_{TH}, a conductive inversion layer is formed connecting the drain and source terminals. In this manner, the NMOSFET acts as a charge controlled switch.

The I-V characteristics of the NMOSFET are shown in Figure 12. When V_{GS} is less than V_{TH}, the transistor is in the cut off region and only a small leakage current flows between the drain and source. When V_{GS} exceeds V_{TH} the conductive inversion layer is formed allowing current flow from the drain to the source. While V_{DS} is below the pinch-off locus, $V_{DS} \leq V_{GS}-V_{TH}$, the transistor operates in the Linear Region and the terminals are connected by a resistive channel. Once the voltage drop from drain to source exceeds $V_{GS}-V_{TH}$, the FET channel pinches off, no longer connecting the terminals. This is called the saturation or pinch-off region.

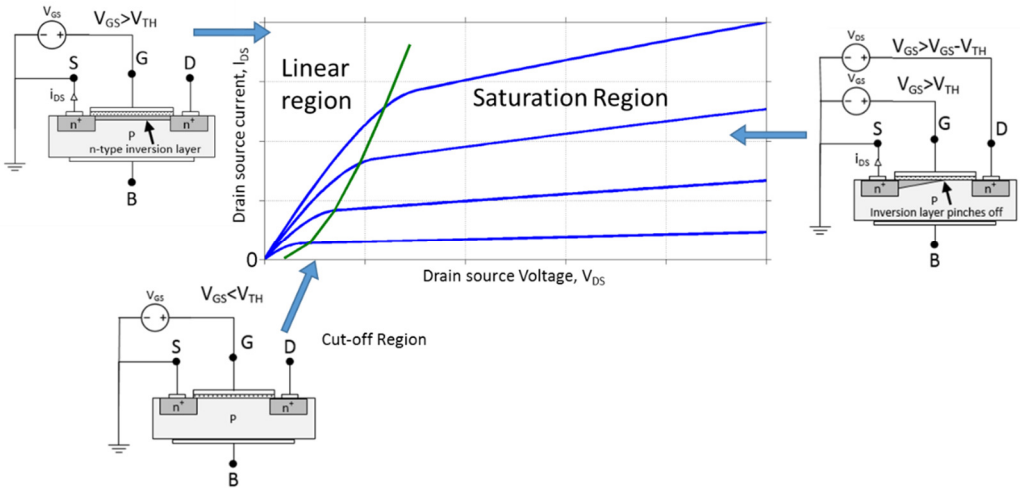


Figure 12. I-V characteristics of NMOS transistor

2.4 MOSFET switching transitions for clamped inductive switching

An ideal switch transitions between states of infinite resistance and 0 resistance instantaneously. For any a practical switch however the transition periods and ON/OFF resistances must be carefully examined. A switching model for the power MOSFET is shown in Figure 13 [21]. The three most crucial components are the capacitors C_{GD}, C_{GS} and C_{DS}. Because the FET is a charge controlled device the switching time is ultimately determined by how fast the voltages can be changed on these capacitors. The Gate-Source capacitance, C_{GS}, is a constant defined by the physical geometry of the gate and source electrodes of the transistor. The Gate-Drain capacitance, C_{GD}, is comprised of a constant term, from the physical overlap of the gate electrode and channel region, and a nonlinear term from the capacitance of the depletion layer. The Drain-Source capacitance, C_{DS}, is the non-linear capacitance of the body diode. A gate mesh resistance, $R_{G,I}$ represent the resistance to the gate signal distribution within the device. $R_{G,I}$ directly impedes the gate current and can have a significant effect in high speed switching [21]. It must also be mentioned that gate driver impedance, R_{HI}, and external series resistance, R_{GATE} will influence switching performance. The parasitic inductances, L_D and L_S, are mainly package dependent, resulting from the parasitic inductances of internal wire bonds.

The particular type of switching most common in SMPS is clamped inductive switching for which a simplified model is shown in Figure 14 [21]. The DC current source represents the inductor current, which is considered constant for the brief switching time. The diode allows conduction during the off time of the FET and clamps the drain voltage to the output voltage represented by the battery. This model would be valid for an asynchronous switching mode power supply.

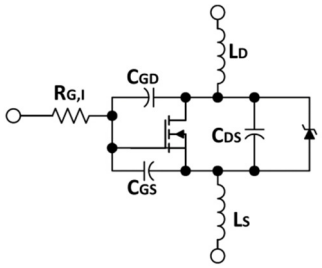


Figure 13. Switching model of MOSFET B. L. Balogh, "Design And Application Guide For High Speed MOSFET Gate Drive Circuits." Texas Instruments, Dallas, 2001. Used under fair use, 2014.

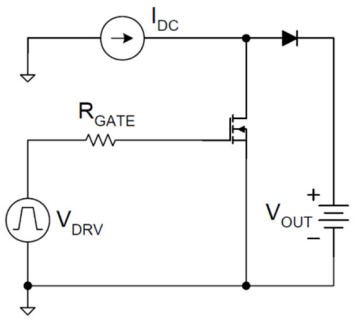
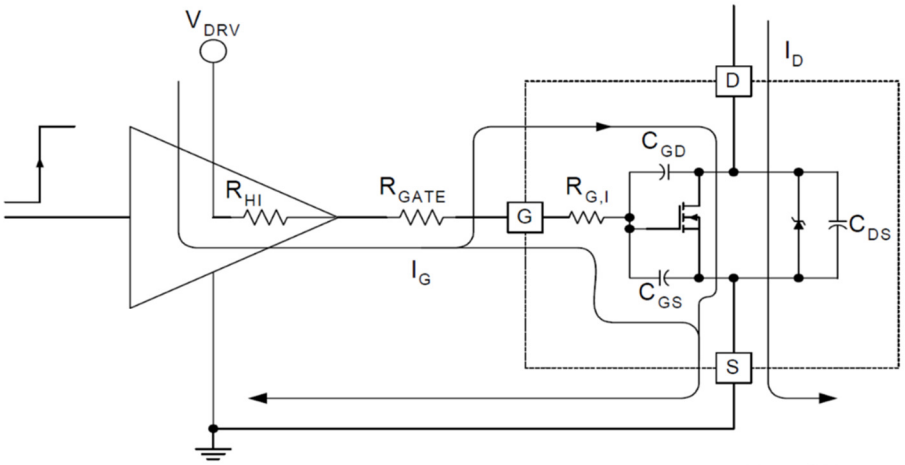


Figure 14. simplified model for clamped inductive switching B. L. Balogh, "Design And Application Guide For High Speed MOSFET Gate Drive Circuits." Texas Instruments, Dallas, 2001. Used under fair use, 2014.

The turn-on sequence is divided into four separate segments as shown in Figure 15 [21]. In segment 1, the majority of the driver current, I_G, flows into C_{GS}. As the capacitor charges, the gate voltage rises from 0 to V_{TH}. Some current also flows into C_{GD}. Segment 1 is called the turn-on delay because the gate signal has been applied but the drain current and drain voltage remain unchanged. During the second segment, V_{GS} rises from V_{TH} to the miller plateau voltage. On the input side, current continues to flow into C_{GS} and C_{GD}. On the output side, the FET begins to conduct and drain current rises to a maximum. This transition corresponds to the linear region of Figure 12 [21] where current is proportional to gate voltage. Throughout this second period, the drain voltage remains unchanged because it is clamped by the diode. Only after all the current flows into the drain is the diode able to block voltage. The third segment of the turn-on cycle, called the Miller plateau region, sees a constant V_{GS}. All available driver current is diverted to discharge C_{GD} in order to rapidly lower V_{DS}, which falls to nearly zero. During the final fourth segment, the driver current into C_{GS} and C_{GD} drops to zero as V_{GS} is charged to the level of the drive voltage, fully enhancing the FET.



	FET state	V_{GS}	I_G	V_{DS}	I_D
1	Cut off	rises to VTH as C_{GS} and C_{GD} are charged	most flows to charge C_{GS} small part charges C_{GD}	clamped at Vout	no change from small leakage value
2	Linear Region	rises from V_{TH} to Miller Plateau	flows to charge C_{GS} ans C_{GD}	clamped at Vout	rises from leakage value to full load current
3	Saturation	constant across Miller Plateau	flows entirely to discharge C_{GD}	drops from Vout to I_D*$R_{DS(ON)}$	constant
4	Saturation	rises to V_{DRV} fully enhancing the FET	decreases to zero as C_{GS} charges fully	remains at resistive drop I_D*$R_{DS(ON)}$	constant

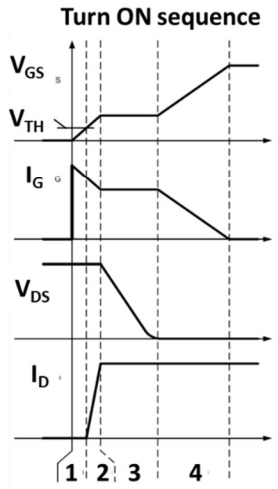
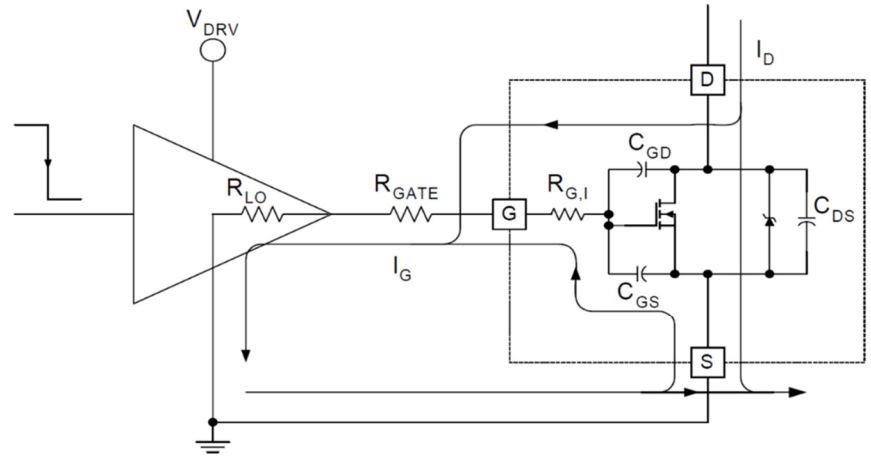


Figure 15. FET switching model with table and graph of turn on sequence B. L. Balogh, "Design And Application Guide For High Speed MOSFET Gate Drive Circuits." Texas Instruments, Dallas, 2001. Used under fair use, 2014.

In order to turn off the FET, the above process must be reversed as shown in Figure 16 [21]. In the first segment of the turn-off sequence, the gate voltage is discharged from the driver voltage, V_{DRV}, to the level of the Miller plateau. The gate drive voltage, V_{GS}, falls as C_{GS} and C_{GD} discharge. Once again, this first segment is a turn-off delay because both I_D and V_{DS} remain unchanged. In the second segment, V_{GS} remains constant across the Miller plateau; thus, a drive current I_G is applied to charging C_{GD}. V_{DS} rises from the small resistive drop of the FET to its final value V_{DSOFF}. The drain current remains unchanged during the second segment. In the third segment, the diode turns on providing an alternate route for the inductor current. The FET passes through the linear region where I_D is proportional to V_{GS}. I_D drops from the full load current to nearly zero as V_{GS} discharges from the Miller plateau to the threshold voltage. Lastly, the driver sinks the remaining current, I_G, as C_{GS} discharges to zero in the fourth segment.



	FET state	V_{GS}	I_G	V_{DS}	I_D
1	Saturation	falls from V_{DRV} to V_{GS} Miller	flows from discharging C_{GS} and C_{GD}	remains at resistive drop I_D*$R_{DS(ON)}$	no change from full load current
2	Saturation	remains constant across Miller Plateau	flows entirely to charge C_{GD}	rises from I_D*$R_{DS(ON)}$ to Vout	no change from full load current
3	Linear	falls to V_{TH}	flows from discharging C_{GS}	clamped at Vout	drops to small leakage level
4	Cut off	falls to zero	drops to zero as C_{GS} fully discharges	clamped at Vout	remains at leakage level near zero

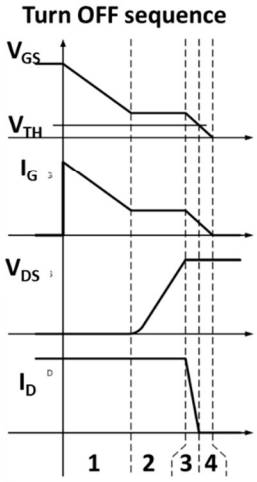


Figure 16.FET switching model with table and graph of turn off sequence B. L. Balogh, "Design And Application Guide For High Speed MOSFET Gate Drive Circuits." Texas Instruments, Dallas, 2001. Used under fair use, 2014.

2.5 MOSFET power loss

Now that the switching sequence of the MOSFET has been established, the FET power loss during the switching transitions can be understood. During segments 2 and 3 of both the turn-on and turn-off sequences, drain current and drain voltage change at separate times. FET power consumption, the product of current and voltage, is, therefore, large during these transition periods. When fully turned on, the MOSFET is characterized by an on resistance $R_{DS(ON)}$, which is dependent on the physical properties of the FET as well as the gate voltage.

For a fixed gate voltage, the on state FET loss will be the product of drain current and V_{DS}. On state losses are generally small because VDS is equal to the voltage drop of the small $R_{DS(ON)}$ resistance. During the OFF state of the FET, the losses are given by the product of the leakage current and V_{DS}. In this case, V_{DS} is large but the leakage current is small resulting in very slight losses in the OFF state.

2.6 Gate drive operation

The gate driver is as important as the switching FET itself. Recalling the definition of an ideal switch, the objective is to transition the FET from its highest to lowest resistance states as quickly as possible. The FET is a charge controlled device for which the switching transition is accomplished by changing the voltage on several intrinsic FET capacitors to deposit or remove this charge. For a capacitor, voltage changes as a function of current given by

$$i_C = C\frac{dv_C}{dt} \tag{20}$$

For a fixed capacitance, C, and change in voltage, dVc, the necessary transition time is inversely proportional to the current

$$dt = \frac{1}{i_C} * Cdv_C \tag{21}$$

As shown by (21), driver source/sink current capability is the most important factor determining transition time.

Another important factor influencing gate drive implementation is the orientation of the MOSFET within the circuit. Because NMOS turn on is determined by the gate source voltage it may be necessary to produce a voltage higher than the converter input under certain conditions. Consider the asynchronous buck and boost converters of Figure 17. The boost converter has its source tied to ground so that the gate drive signal can also be referenced to ground. For the buck converter however the source is only a resistive drop less than the input voltage when the FET is in its low resistance or ON state. The driver signal can no longer be referenced to ground because a voltage higher than Vin would be required to turn on the FET. Rather, the gate drive signal of the buck converter must be referenced to the FET source terminal. The circuitry for ground referenced gate drive is simpler than for a non-ground referenced driver.

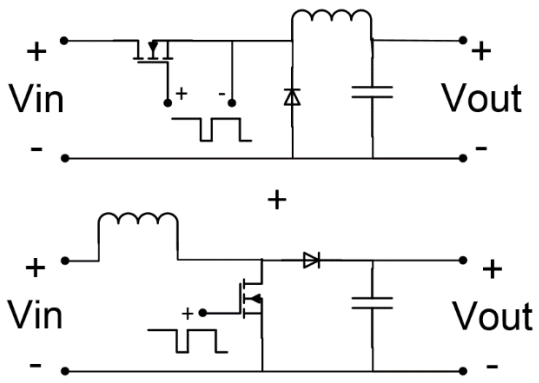


Figure 17. Gate drive references for asynchronous buck and boost converters.

The charge Qg required to raise the FET gate voltage to the driver level V_{DRV} is constant. The driver power consumption arises from the resistive losses as the drive current passes through the internal impedance, R_{HI} and R_{LO}, the gate drive resistance R_{GATE} and the FET gate mesh resistance $R_{G,I}$.

2.7 Control

Feedback control is an essential part of practical DC-DC converters. Control provides the ability for a converter to maintain its output at a desired level despite variations in input voltage and load. This section presents both theory and hardware to provide an intuitive understanding of control function and purpose. The basic elements of the loop transfer function, or converter plant, are discussed. Stability criteria are established. Finally, the influence of the feedback system to compensate the open loop plant in a beneficial manner is conveyed. The three most common types of compensation network are shown for easy identification.

This discussion of control is by no means exhaustive and perhaps risks oversimplification. In practice, control remains a subject of extensive research with intricacies that confound even the most knowledgeable in the field. The simplified overview of control presented here is justified precisely because this complex research has yielded great benefit for the engineer. Integrated circuit technology has streamlined the compensation process to such a high degree that the power supply designer can achieve exceptional performance with only a high level understanding of control theory.

2.7.1 Feedback from perspective of PWM hardware

Up to this point, DC-DC converters have been analyzed as open loop systems. Using steady state analysis the voltage transfer functions were derived for several topologies in terms of duty cycle. Because the output is a function of input voltage and duty cycle the duty cycle of the PWM converter can be adjusted to compensate for input variations. This is the basic concept of control in a switching mode power supply. Negative feedback is employed to maintain a set output in spite of input and load variations.

A basic hardware knowledge of the converter PWM generator is beneficial to understand feedback control. The central component, a high speed comparator, operates like a one bit analog to digital converter. When the non-inverting input is higher than the inverting input the output is high otherwise the output is low. A fixed frequency PWM signal is generated by comparing an oscillating ramp to a fixed reference input as shown in Figure 18 [22]. The frequency of the PWM signal is the same as that of the oscillator and the duty cycle is set by the ratio of $V_{control}$ to V_{ramp}.

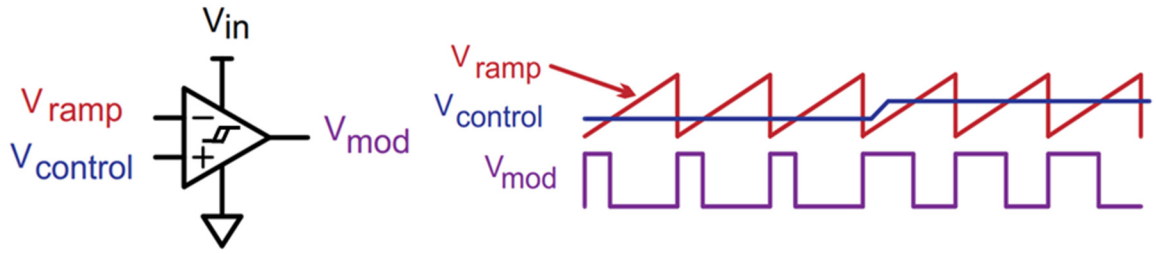


Figure 18. Pulse width modulator formed by comparator and oscillating ramp input D. Meeks, "Loop Stability Analysis of Voltage Mode Buck Regulator With Different Output Capacitor Types – Continuous and Discontinuous Modes," no. April1. Texas Instruments, Dallas, 2008. Used under fair use, 2014.

Negative feedback is provided by an inverting differential amplifier which senses the difference between a fixed reference and a feedback voltage. The inverse of the sensed difference multiplied by the amplifier gain is output as an error voltage V_e. The error voltage V_e becomes the reference input to the PWM comparator closing the loop. The most common feedback control schemes are voltage mode control where the output voltage is used as feedback and current mode control where the inductor current is used as a feedback signal.

The basic layout of a buck converter with voltage mode control is shown in Figure 19. The output voltage is sensed through the voltage divider formed by R1 and R2. The output reference is input to the error amplifier stage and compared to a fixed reference voltage V_{ref}. The error voltage V_e, output from the amplifier, is used as the input to the PWM comparator which drives the FET.

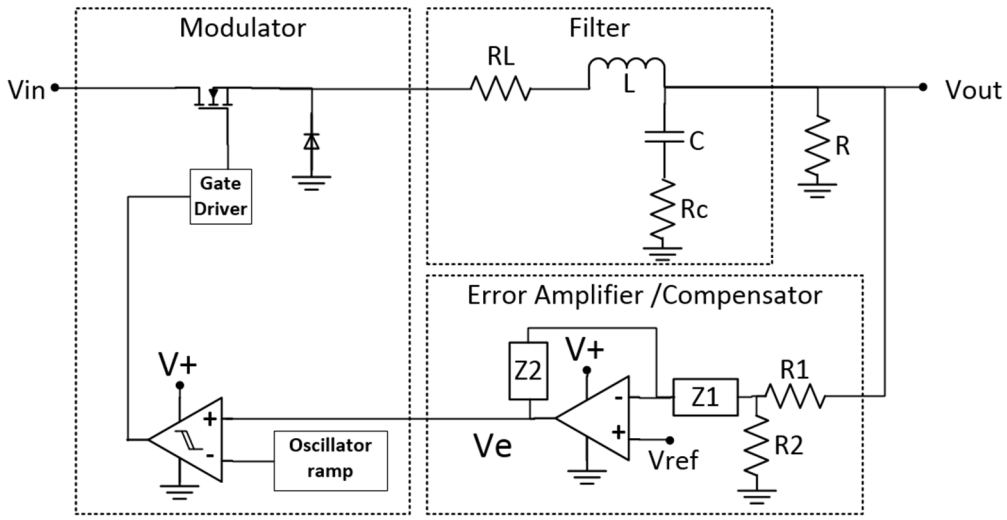


Figure 19. Buck converter with voltage mode feedback control

2.7.2 Stability and loop compensation

The purpose of control is to maintain a desired output in the presence of input voltage and load variations. The frequency transfer characteristics of the converter and controller are important because, by nature, the system must respond to non-DC disturbances. Any converter system can be represented by the closed loop block diagram of Figure 20 [23]. The dynamic performance and stability of the power supply can now be evaluated in the same manner as any SISO control system.

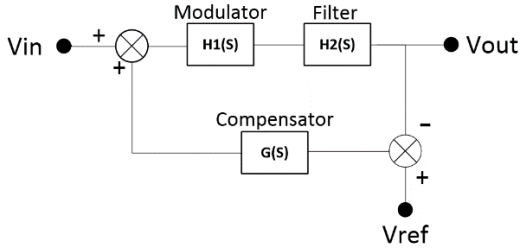


Figure 20. Closed loop block diagram of switching mode power supply. M. Brown, *Practical switching power supply design*. San Diego: Academic Press, 1990. Used under fair use, 2014.

The criteria for stability is that the phase delay cannot be greater than 360° whenever the gain is greater than or equal to 1. Because negative feedback contributes 180° of lag this means that any additional lag cannot exceed 180°.Though any lag less than 180° is theoretically stable, the general rule is to have at least 45° of phase margin both to limit overshoot and to provide a safety margin. The Modulator and Filter transfer characteristics comprise what is called the loop transfer function or control-to-output transfer function. The compensator placed in the feedback path can be used to shape the open loop transfer function to a desired closed loop transfer function.

A graphical example is shown in Figure 21. The loop transfer function of the modulator and output filter are shown along with the transfer function of the compensator. When the loop is closed the compensator adds phase boost at the cross over frequency to improve the overall system response. Figure 21 is presented as a visual representation of the compensation process to illustrate the steps that must be executed by the compensation designer. The plot is unrelated to the physical converter design presented in Chapter 4.

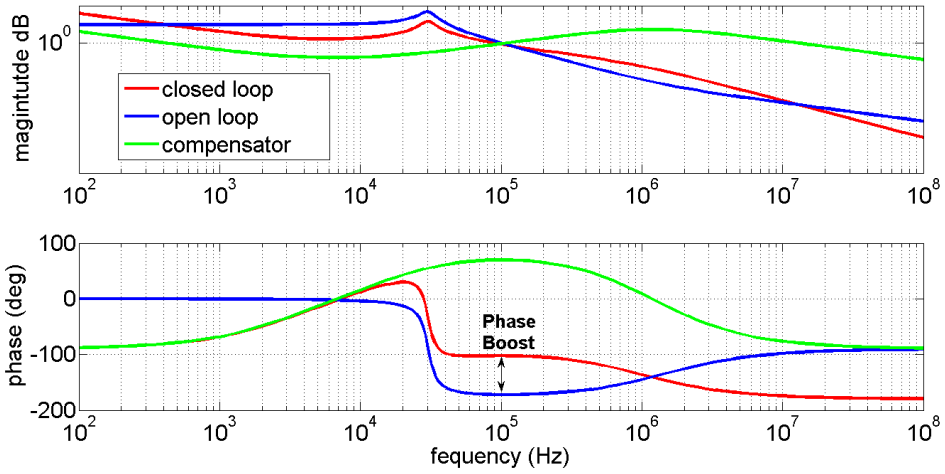


Figure 21. The compensator adds phase boost to adjust the closed loop transfer function

2.7.3 Identifying basic compensator types

The three most common compensation schemes are classified by the number of compensator poles. In electrical engineering, it is standard practice to refer to these compensation schemes as type I, type II and type III [19] [22] [24]. These compensation schemes are different from the definitions of type I, II and III systems within the controls community, where the term relates to steady state error when a system is excited by different kinds of inputs.

Type I compensation, with a single pole, is seldom used because a low bandwidth results in poor transient response. Type II compensation adds a second pole and a zero to significantly extend the bandwidth. This compensation scheme is widely used in switching mode power supplies. Lastly, type III compensation has three poles and two zeroes allowing for more phase boost and adjusting the steep roll off of the filter stage. These compensation types are achieved by adding resistors and capacitors to the error amplifier as shown in Figure 22 [24].

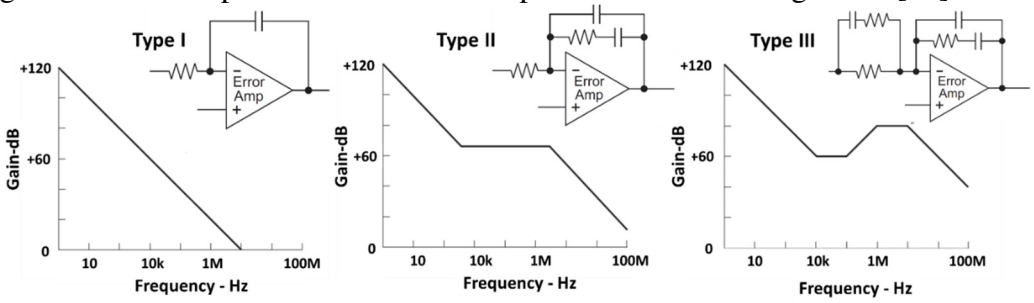


Figure 22. Three most common compensator types and their magnitude plots M. Day, "Optimizing Low-Power DC / DC Designs – External versus Internal Compensation," *Portable power design seminar*. Texas Instruments, Dallas, 2004. Used under fair use, 2014.

This section has presented the basic concepts of feedback control in switching mode powers supplies. This very simplified approach is intended to give an intuitive understanding of the purpose and function of control in switching mode power supplies. A desired output is maintained using an error amplifier to control the duty cycle through means of a PWM comparator reference. The system response to high frequency disturbances is crucial as perturbations are by nature non-DC. The modulator and filter stages of the power supply provide an intrinsic AC response called the loop transfer function. Capacitors and resistors can be added to the feedback amplifier so that the closed loop AC response compensates and improves the performance of the basic loop transfer function.

Care must be taken not to oversimplify control, though its purpose can be readily understood, the practical implementation of control is neither straightforward nor intuitive. The intricacies of controller design and realization are well beyond the scope of this work. The fortunate reality is that much of the heavy lifting in regard to control has already been done by dedicated power supply engineers. Integrated circuits which are the principle component of practical converters contain nearly all feedback amplifier and modulator circuitry. In some cases the compensation network is also provided internally. With such tools available a basic understanding of the controller function and purpose is generally sufficient to construct a converter which meets all design requirements.

Chapter 3: DC-DC converter Integrated circuits

The majority of the components discussed in the previous chapter are contained in a single integrated circuit which forms the nucleolus of every practical converter. At a minimum this IC contains the error amplifier, functions for DC output voltage sensing and correction, a voltage-to-pulse width converter, a stable reference voltage, an oscillator, overcurrent shutdown protection, and gate drivers for the power switch [23]. Some ICs even contain an internal FET in addition to gate drivers. The remaining challenge for the user is to understand the IC datasheet and how to select proper external components.

This section begins by differentiating internal and external FET devices. Next, all converter ICs are divided into two categories based on their compensation networks. Externally compensated converters allow the user direct access to the compensation loop while internally compensated converters offer no means of adjusting compensator poles and zeroes. Examples are presented for each converter type showing internal block diagrams and necessary external components. The benefits and downsides of each are explained.

External compensation affords the user the greatest degree of flexibility and highest overall performance. Longer design cycles are required for external compensation in which the competence of the user very much determines whether a high performing or a non-functioning supply is produced. Internally compensated devices are simpler to use but can suffer lower performance as an uncertain plant must be accounted for by a more conservative compensation scheme. The tradeoff is largely theoretical however as the performance of modern internal compensation now rivals any externally compensated design.

The only significant distinction is packaging and the complexity of printed circuit board assembly. Externally compensated device ICs are commonly available in SOIC, TSSOP and MSOP packages which are simpler to assemble because all leads are visible on the sides of the packages. Most variants have 8, 10 or 24 pins. Though some internally compensated ICs are available in the above packages the highest performing devices are produced almost exclusively in BGA and LGA packages with up to 200 pins all located beneath the packages. The large number of pins, inaccessible from the top of the package, make internally compensated devices difficult to assemble without an industrial process. Overall, internal compensation offers distinct advantages of readily attainable performance with minimal design cycle time.

3.1 Internal vs. external FET ICs

Integrated circuits for power electronics fall into two broad categories internal FET devices and external FET devices. As the name implies, internal FET devices have one or more power MOSFETS integrated into the wafer inside the package while external FET devices do not. The major advantage offered by internal FET devices is design simplification. The burdens of gate drive and power MOSFET selection are completely removed from the applications engineer because driver and FET are internal and carefully paired. The universal downside to internal FET devices is reduced power ratings compared to external FET designs. The overall power rating of the FET is sometimes limited by the need to process the FET on the same wafer as the driver and other circuitry. The power limit is usually further lowered by the thermal performance of the package. Integrated FET ICs generally have a small fraction of the exposed thermal pad that is present in a dedicated power MOSFET to provide a cooling path.

The opposite is true for external FET devices. Design is still simplified because the gate driver and control circuitry are included in the IC but the critical power FET must still be chosen. Recommendations are generally given in the datasheet but the selection process is still complex. Greater care must also be given to printed circuit board layout to avoid parasitic effects. The principle advantage is that higher power FETs can be chosen and adequate heat sinking can more readily be provided.

3.2 Externally compensated converters

An externally compensated converter is defined as any converter in which the user must directly provide the feedback compensation as part of the design. Externally compensated converters are the most challenging design category in terms of physical implementation despite many efforts to simplify their use. Design is centered on a single integrated circuit containing at a minimum a gate driver, modulator and error amplifier. The TPS 54331 shown in Figure 23 [25] is a good representation of an internally compensated converter IC. The TPS 54331 is an asynchronous internal FET buck converter manufactured by Texas Instruments. Contained within the small 8 pin SOIC package are an error amplifier, slope compensation, current sensing, PWM comparator, gate drive logic, PWM latch, gate driver and Internal FET.

Figure 24 [25] is a typical application circuit showing the minimum external components that the user must select to produce a functioning power supply. The flyback diode, output filter, feedback voltage divider, boot strap capacitor, compensation network, slow start capacitor and an input voltage divider must all be selected by the user, 13 components in all. The user has direct access to the compensation network through the COMP pin. A type II compensation network comprised of C1, C2 and R3 is shown connected to COMP. This is the crucial feature that defines the TPS 54331 as an externally compensated converter.

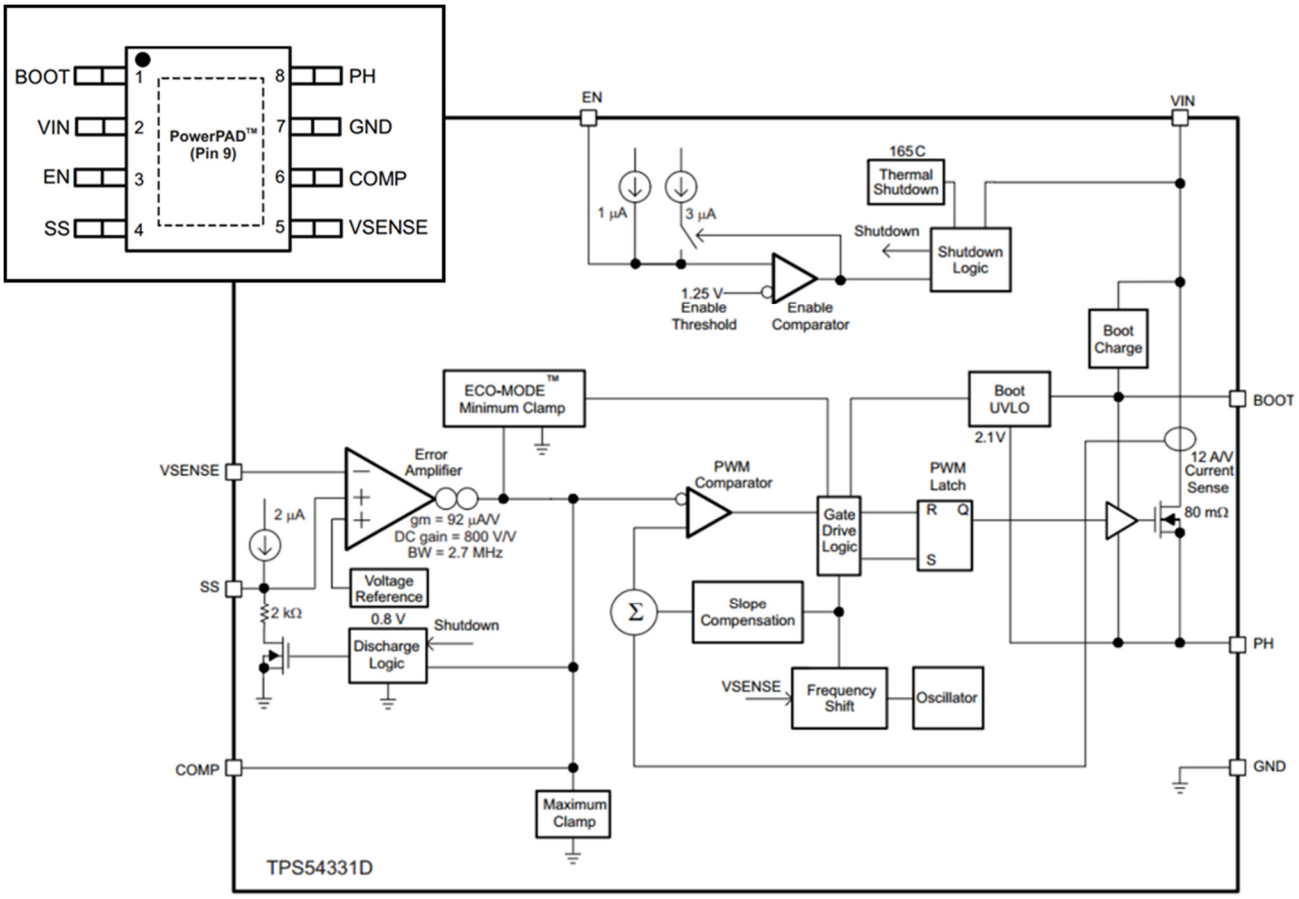


Figure 23.Block diagram of TPS54331 Texas Instruments, "3A , 28V INPUT , STEP DOWN SWIFT ™ DC / DC CONVERTER WITH ECO-MODE ™ TPS54331," no. July 2008. Texas Instruments, Dallas, 2012. Used under fair use, 2014.

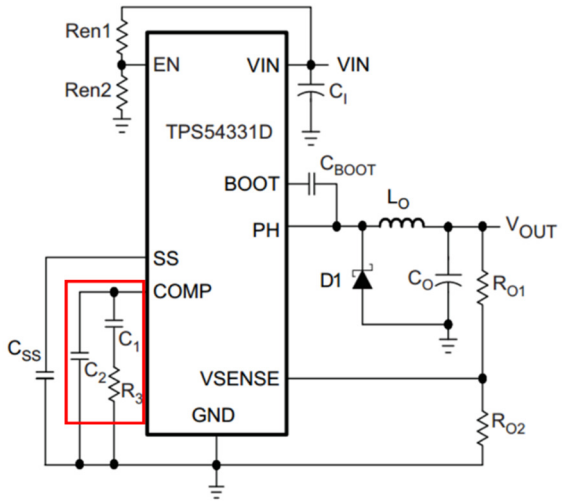


Figure 24.Application circuit for externally compensated TPS54331 Texas Instruments, "3A , 28V INPUT , STEP DOWN SWIFT ™ DC / DC CONVERTER WITH ECO-MODE ™ TPS54331," no. July 2008. Texas Instruments, Dallas, 2012. Used under fair use, 2014.

3.3 Internally-compensated converters

An internally-compensated converter is defined as any DC-DC converter for which the user has no direct access to the compensation network. The required external components vary widely depending on the converter IC. In some cases the whole output filter is internal to the chip ensuring that the plant is known. More commonly, only the FETs are internal and filter components must be selected by the user. A good example of an internally compensated converter is the PI3312-X0 produced by Vicor. The converter block diagram is shown in Figure 25 [26].

The PI3312-X0 is a synchronous step down converter with two internal FETs. Significantly less detail is given on the device internals primarily because the user does not need to understand the zero voltage switching (ZVS) controller. It only remains for the user to select input capacitors and an output filter. Detailed guidelines are provided in the datasheet for selecting the filter components so that very little calculation is required on the part of the designer.

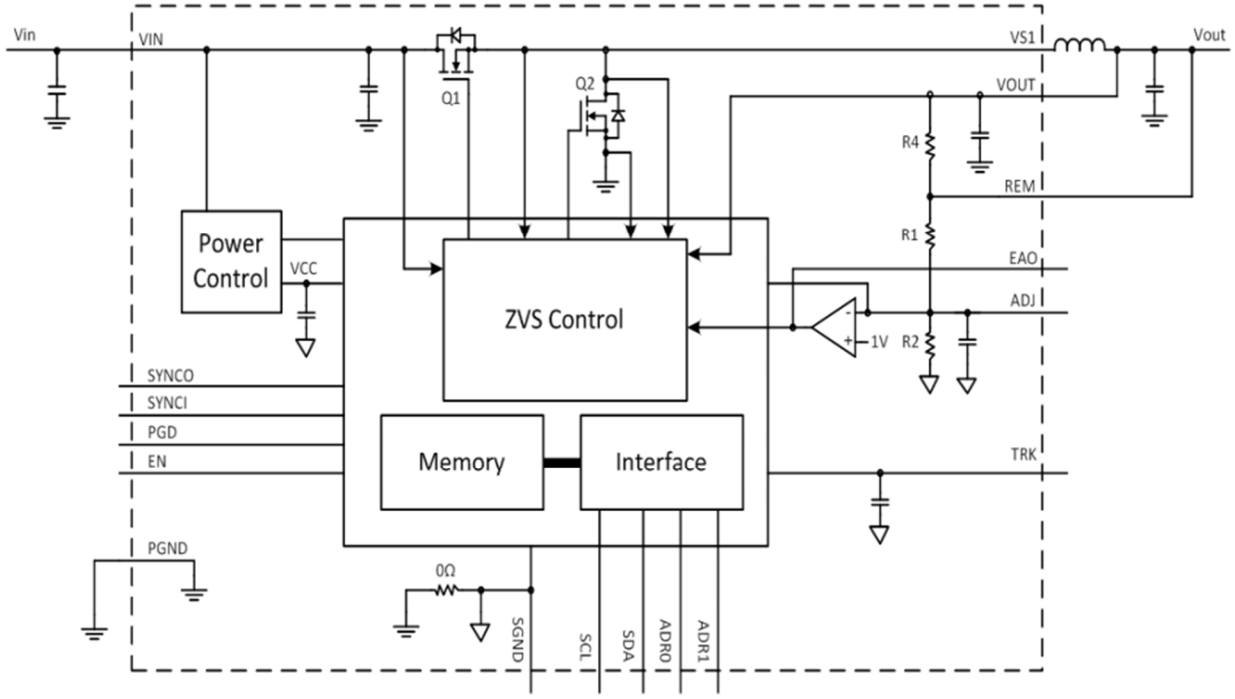


Figure 25. Block diagram of internally compensated PI3312-X0 Vicor, "PI33XX-X0 8V to 36Vin Cool-Power ZVS Buck Regulator," 2013. [Online]. Available: http://cdn.vicorpower.com/documents/datasheets/Picor/ds_pi33xx.pdf. Used under fair use, 2014.

3.4 Benefits of internal vs. external compensation

Fundamentally, the choice between internal and external compensation is a classic trade-off between simplicity and performance. In reality the performance advantages of external compensation are rarely attained even with multiple design iterations. For anyone other than a dedicated power supply designer internal compensation offers equal performance with significant time savings.

The performance improvement of external compensation can be understood in terms of the power supply block diagram of Figure 20 [23]. The user has the ability to change both the filter stage and the compensator stage of the power supply. This allows improved transient response and possibly lower ripple voltage [27]. The most significant drawback is design complexity as the designer must have the competence to shape the filter and compensation responses to achieve these performance gains. This requires the designer account for non-ideal parameters such as capacitor equivalent series resistance (ESR) and inductor winding resistance in all calculations. Layout is also crucial for performance as parasitic inductances from poor layout can completely degrade performance.

A suggested layout for the TPS54331, from a TI evaluation board, is sown in Figure 26 [28]. The total size is large compared to the size of the IC, U1. The physical placement of the components is crucial to performance. An evaluation board layout serves as a good starting point but in some cases this is not available and multiple layout revisions may be needed before a functioning supply is produced. Ultimately, no modeling can completely account for component tolerances and layout effects. If the desired performance is not achieved system identification may be necessary to determine the true plant dynamics and adjust compensation accordingly.

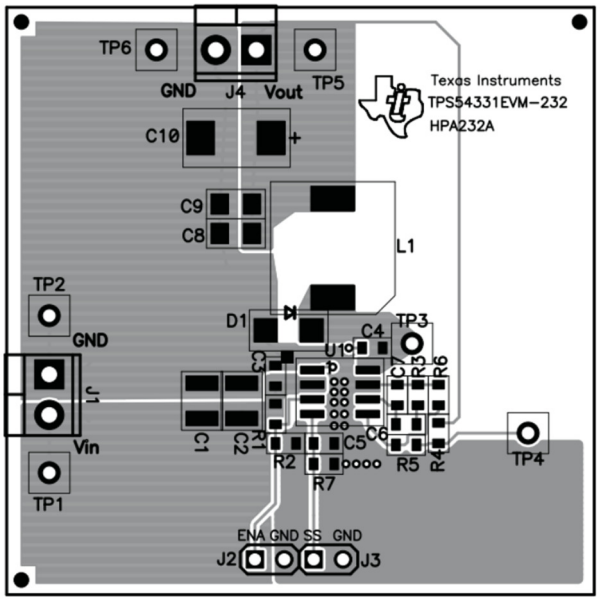


Figure 26. Circuit board layout of TPS54331 Texas Instruments, "TPS54331EVM-232 3-A , SWIFT ™ Regulator Evaluation," no. July. Texas Instruments, Dallas, p. 11, 2008. Used under fair use, 2014.

Internally compensated devices, though significantly simpler to use, are not less complex overall than externally compensated devices. The important difference is that the heavy lifting in compensator design has been done by engineers working for the IC manufacturer. This is the primary advantage of internally compensated converters, the most challenging design aspects have been done for the user, often by a more qualified designer. These engineers did not know the ultimate application however and had to make assumptions about the overall converter plant to design compensation. By nature then, the internal poles and zeroes must be more conservative to guarantee stability when the actual open loop plant is determined by the user [27].

As consequence the user must work within a set of filter component guidelines. This is the primary drawback of internal compensation the freedom of the designer to select power stage components is reduced. If the filter inductance, capacitance and ESR are not properly selected the resulting filter response will not match the internal compensator response and instability or performance degradation will result [27]. In many cases the exact filter component values and even specific part numbers are provided in the datasheets of internally compensated converters. Rather than a design restriction this is more often a blessing for users who do not want to consider every design aspect to produce a working solution.

Even the distinction in performance between internal and external compensation is diminishing with improvements in power electronics technology. The most advanced internally compensated converter chips now rival external compensation in every regard. One factor contributing to these advances is tighter control over the converter plant through integrated filter components and larger BGA type packaging. Consider the layout of thePI3312-X0of Figure 27 [26]. The package is a 123 pin land grid array (LGA) with all the pads underneath the chip. The simple layout depicts two rows of capacitors and one inductor in an optimal layout for the switching current path. Both capacitor and inductor model numbers are provided in the Vicor datasheet. The converter open loop plant is almost completely know to the Vicor engineer, provided the user follows the recommended layout and component selection. This detailed knowledge of the open loop plant means a much less conservative, higher performance compensation can be attained.

Additional uncertainty form printed circuit board layout is minimized because the large LGA package defines the current return paths and relative geometry. The packaging however is a case where the IC designer is benefited at the cost of user. An LGA package requires one of the most difficult soldering processes because all pins are located beneath the package and are not pre-balled. Assembly then presents the only significant downside of modern internally compensated converters. This is more of a concern for small scale production such as in a laboratory setting using basic solder station equipment. LGA packaging would not present any difficulty for an industrial assembly process.

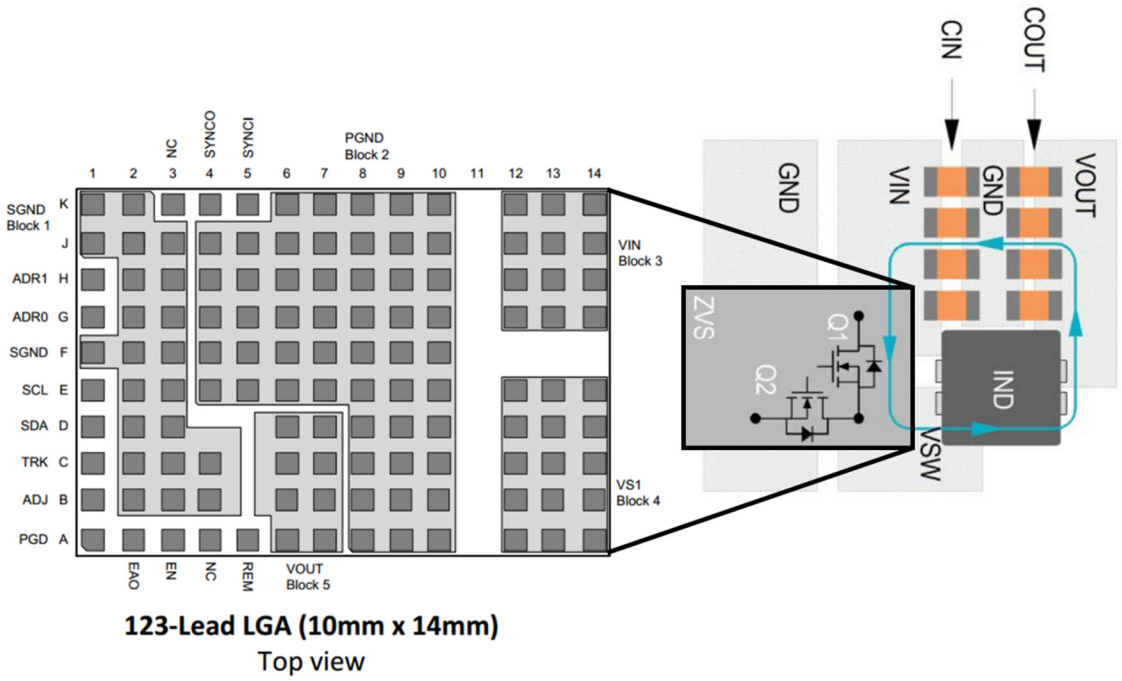


Figure 27. IC package and layout of PI3312-X0 converter Vicor, "PI33XX-X0 8V to 36Vin Cool-Power ZVS Buck Regulator," 2013. [Online]. Available: http://cdn.vicorpower.com/documents/datasheets/Picor/ds_pi33xx.pdf. Used under fair use, 2014.

Chapter 4: Design of smart power module

This chapter begins by presenting the research objectives, required features, and six functional elements of a smart power module. The vehicle components in need of regulated power are identified defining the distributed power budget. The requirements of the conversion element are established based on the vehicle conditions and desired performance. Details of design and selection are then presented for each of the six smart power module elements.

The conversion element, a Linear Technology LTM8027, was chosen based on its high efficiency and wide input range. External component selection follows the datasheet guidelines. Power conditioning is primarily achieved external to the modules by a high power transient voltage suppression (TVS) diode on the vehicle that clamps voltage spikes to below 55V. Secondary protection is provided by an internal TVS diode which will suppress any spikes above the LTM8027s max input of 60V.

Power management, the element requiring the most detailed design is covered in five subsections. Power management encompasses current measurement, current limit adjustment, overcurrent detection, and output protection. Current measurement is addressed first, with the selection of a shunt resistor and shunt amplifier. Next, overcurrent detection is attained by means of a comparator which is selected based on a set of features including latching, complementary outputs. A digital potentiometer is chosen to allow current limit adjustment by varying the reference input of the overcurrent comparator. A P-channel MOSFET is selected to provide the necessary high side disconnect for output protection. Lastly, a gate driver for the output FET is designed and simulated using LTspice to achieve low continuous losses and rapid transition time.

CAN is chosen as the industry standard communications interface. The processing element is selected from the C2000™ family of microcontrollers having CAN peripherals and convenient programming support through TI's Code Composer Studio. A two color Red-Green LED was selected as the module status element to provide a wide range of simple messages by varying both color and blinking pattern. The decision to provide three individually controllable outputs from each module is discussed based on the size of the conversion element and large number of available microcontroller I/O. A two circuit board design is adopted to improve heat sinking and full space utilization within a standard extruded aluminum enclosure. The presence of the two distinct circuit boards is the modular aspect of the smart power module. Images of the two circuit board layouts and enclosure are shown highlighting considerations made for convenient assembly and streamlined testing.

The design process was shaped by a philosophy which held physical demonstration of functionality paramount followed by simulated demonstration of functionality with optimization of this functionality as the last priority. Because it was written after three revisions of the smart power circuits this design section is presented in the reverse order with theory and optimization coming before simulation and verification. Design is presented in this order for clarity not to give the impression that each aspect of the design was carefully evaluated before implementation. Ultimately, the performance of some of the features was evaluated for the first time as these sections were written.

The most important aspect of the smart power module, high conversion efficiency, was carefully designed to and achieved. The other required features were designed to a sufficient degree to be implemented in a physical circuit. Additional revisions can be initiated if further

optimization is desired. With physical demonstration paramount, the smart power module designed in this section has been confirmed in its ability to supply the full sensor power needs of an operational UGV.

4.1 Requirements of smart power module

A set of research goals and required features was provided at the project onset. The six elements which comprise a smart power module were defined as shown in Figure 28. Power conditioning pertains to any necessary input regulation such as input filtering or transient voltage suppression. The power supply element is the DC-DC conversion element and all necessary supporting components. Power management refers to all output monitoring and protection features. The internal processing element monitors and controls the module operation. Communications interface is the means for the module to receive commands and transmit information over an established protocol. The module status element displays the state and operation of the module separately from the communications interface. The requirements for the smart power module are presented in Table 3.

High conversion efficiency was the most crucial requirement with a minimum value of 90% for all anticipated loads (1-4A). Reduction in temperature rise relates to the ability of heat sinking to reduce the temperature difference between the module and the ambient air. The goal is to improve temperature rise in the converter by 50% through the addition of heat sinking. Current limiting is desired with a minimum of 255 set points and a limit accurate to ±10% of the set point. Current monitoring within ±5% is necessary. The input range must accommodate the native power bus generally within 24-36V but up to 55V under transient conditions. A configurable output between 3.3V and 24V was to be investigated though only a fixed 12V output was necessary. The desired output ripple is 0.5% or 60mV. The power modules must meet all mission requirements with a minimum output power of 35W and maximum of 100W.

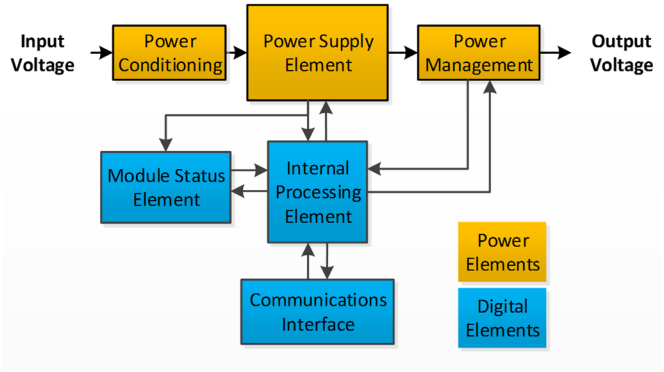


Figure 28.Six functional elements which comprise a smart power module

Table 3. Design requirements for smart power module operation

Requirement	Unit	Ideal value	Marginal value
Small printed circuit board size	in^2	2x3	3x5
Compact enclosure for circuit board	in^3	2.5x.3.5x1	3.5x5.5x2
High conversion efficiency at anticipated loads	%	95%	90%
Reduce temperature rise over output load	%	50%	20%
Temperature sensing	ºC	±1	±3
Programmable current limiting	bits	10	8
Current limit range	%error	±5%	±10%
Output current monitoring	% error	±2%	±5%
Run off of native power bus	V	23.5-55	24-36
Provide configurable output at point of consumption	V	3.3-24V	12V
Regulated output voltage	mVp-p	60 (±0.5%)	240 (±2%)
Smart power subsystem shall be designed to meet all mission power requirements	W	100	35
Industry standard communications interface	binary		
Each module must operate independently of other modules	binary		
Processing element must be sufficient to support all necessary computational requirements	binary		

4.1.1System power requirement

Eight system components were identified as requiring a higher degree of power regulation than that of the base vehicle power bus. These components and their power consumption are listed in Table 4.The input voltage of all components is 12V. The total regulated power draw is a continuous 91W. The largest power draw of any individual component is 29W for the radio. The relative locations of the components are also listed, four components on the roof, 1 in the front and three in the back of the vehicle. The majority of the power is needed by the roof sensors, 64.5W, leaving only13W for the front sensors and 13.4W for the rear sensors.

Table 4. List of vehicle sensors supplied by smart power modules

device	location	voltage (V)	current (A)	power (W)
Radio	roof	12.0	2.4	29
video switch	roof	12.0	1.8	22
perception camera	roof	12.0	0.6	7
OCU	roof	12.0	0.54	6.5
Velodyne 1	front	12.0	1.1	13
Velodyne 2	rear	12.0	1.1	13
wheel encoder 1	rear	12.0	1.8E-02	0.216
wheel encoder 2	rear	12.0	1.8E-02	0.216
		Total	7.6	90.932

4.1.2 Requirements of conversion element

In order to design the DC-DC converter several key requirements must be defined the input voltage range, output voltage, output power, output ripple, and conversion efficiency. The input voltage of the nominal 28V vehicle bus ranges from 24V at an absolute minimum up to 55V the clamping voltage of the vehicle TVS diode. The output voltage is 12V. The minimum output power must exceed the highest continuous load of 29W. A minimum output power of 35W was chosen. A minimum conversion efficiency of 90% was chosen for loads above 1A.

The maximum acceptable voltage ripple requirement was determined from the devices being powered which require a minimum of 5% or 600mV peak to peak at 12V. The chosen max ripple value however was 0.5% or 60mV peak to peak. To reduce design complexity the converter must be internally compensated. No initial requirement was set for switching frequency. The converter target specifications are shown in Table 5.

Table 5. Requirements for conversion element

Input voltage range	24-55V
Output voltage	12V
Minimum output power	35W
Output regulation	±0.5% (60mV pk-pk)
Conversion efficiency	< 90% (for Iout> 1A)
Compensation	Internally compensated

4.2 Conversion element

The selection of the conversion element was driven by desire for design simplicity and efficiency. The most restricting requirement for the conversion element was the input voltage maximum of 55V. The value comes from the clamping voltage of the vehicle's TVS diode. Under the worst case operating conditions an input voltage of 55V could be applied to the module for nearly 1 full second. Because of the very long duration of this high voltage the only viable solution was to select a device rated for a continuous input voltage higher than 55V.

This notably limited the options for conversion element as seen in Table 6. Using the Digikey search filters for internally compensated converters with a 12V output shows that the nominal input of 28V fits more readily into a range of converters either 18-36V input or 9-36V input. Accounting for the possibility of a 55V input limited the potential options by more than two thirds.

Table 6. Availability of conversion elements based on input voltage range

Vin min (V)	Vin max (V)	# of Digikey devices
18	36	133
9	36	132
18	75	113

Efficiency, the next most crucial design criteria, was more difficult to characterize. Conversion efficiency is a function of load current and input voltage. For a step down converter overall efficiency improves as the difference between input and output voltage gets smaller. For a given input and output level conversion efficiency generally varies with load current as seen in Figure 29. The curve is split into three regions. The light load region is always characterized by low but increasing efficiency. The peak region is defined as the region where efficiency reaches its maximum. As load increases efficiency drops off and may reach a third region where the efficiency falls below an acceptable level. The threshold determining the regions is arbitrary, based on the application. For this design 90% efficiency was chosen as the threshold with 1A as the start of the peak region.

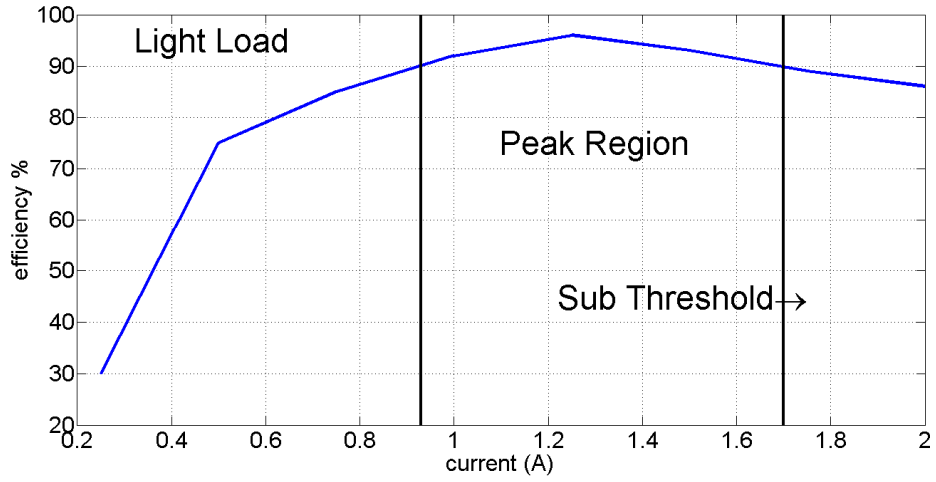


Figure 29.Generic efficiency plot for buck converter

The conversion element chosen was the LTM8027 an internally compensated buck converter from Linear Technology's µModule® family. The LTM 8027 represented the only solution identified which met the necessary input voltage range and efficiency requirements. Table 7 shows that the LTM 8027 meets all the additional requirements for the conversion element.

Table 7. Comparison showing how the LTM8027 specifications match the conversion element requirements

	Requirement	LTM8027 spec
Input voltage range	24-55V	16V-60 V
Output voltage	12V	12V
Minimum output power	35W	48W
Switching frequency	Not defined	100-500 kHz
Output regulation	±0.5% (60mV pk-pk)	0.2% typical
Conversion efficiency	< 90% (for I_{out}> 1A)	< 90% (for I_{out}> 1 A)
Compensation	Internally compensated	Internally compensated

The LTM8027 is a synchronous buck converter with two internal FETs and an internal inductor as shown in Figure 30 [29]. The device is current mode controlled with adjustable switching frequency and output voltage. Like any internally compensated device, the details of the control loop are not provided. An internal regulator is present to provide power to the control circuitry.

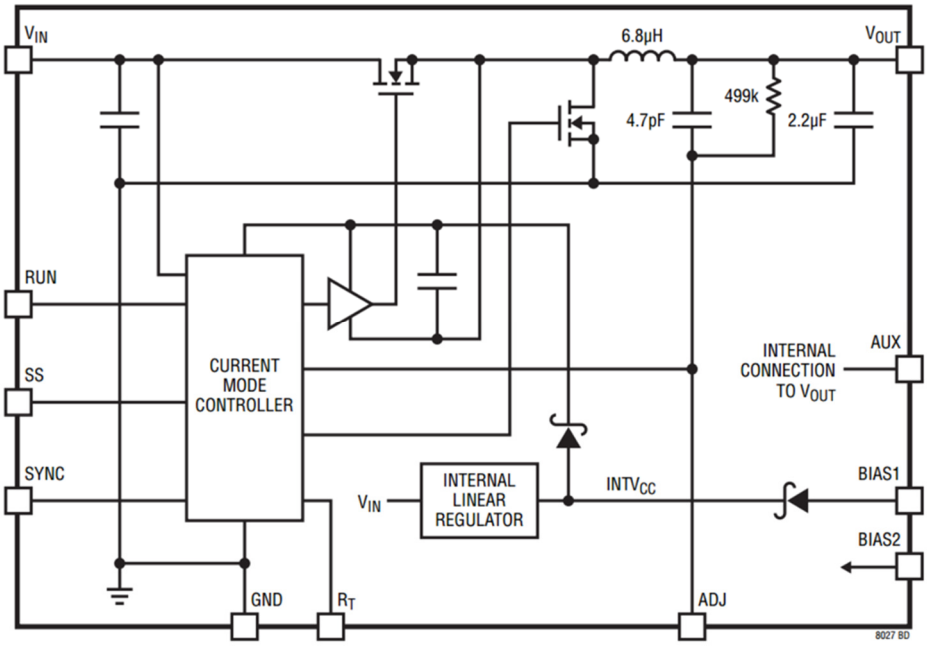


Figure 30. Block diagram of LTM 8027 LinearTechnology, "LTM8027 60V, 4A DC/DC µModule Regulator." Linear Technology, Milpitas, 2009. Used under fair use, 2014.

The selection of supporting components was guided by the LTM2807 datasheet. The datasheet schematic is shown in Figure 31 [29]. Five external components where required with recommended values supplied. One 48.7kΩ resistor sets the switching frequency to the recommended 300 kHz. Another resistor, 56.2 kΩ, sets the output voltage to the desired 12V. The remaining resistor, 1MΩ, pulls up the enable pin to ensure the device is always on when input voltage is supplied. Lastly, two 4.7µF input and four 22µF output capacitors are required.

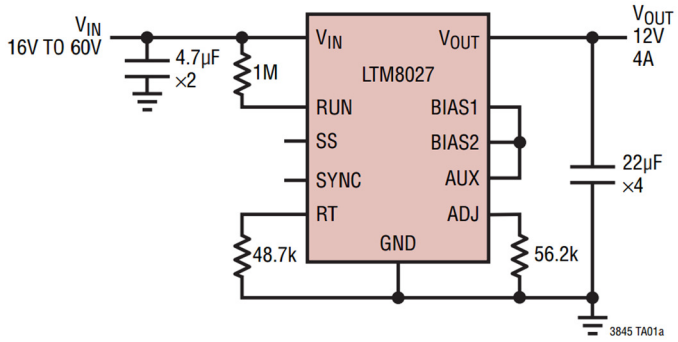


Figure 31. Application schematic for LTM8027 LinearTechnology, "LTM8027 60V, 4A DC/DC µModule Regulator." Linear Technology, Milpitas, 2009. Used under fair use, 2014.

4.3 Power conditioning element

The primary power conditioning was provided by the vehicle power system in the form of a high power TVS diode. TVS stands for transient voltage suppression which is a certain type of diode designed to provide overvoltage protection to sensitive electronics. Like any diode, a TVS diode provides a high impedance when reversed biased. Unlike a regular diode the break down voltage of a TVS is carefully set to a desired threshold. When the protection threshold is exceeded the junction undergoes an avalanche breakdown providing a low impedance path for the excess current. In this manner transient current is diverted away from sensitive components and shunted through the TVS diode [30]. The operation of a TVS diode is illustrated in Figure 32.

Four factors are important in the selection of a TVS diode. The reverse standoff voltage is the voltage below which the diode will always present a high impedance. Reverse breakdown voltage is the voltage at which the device will begin to undergo avalanche breakdown and present a low impedance path. The peak pulse current is the maximum current that the TVS can withstand without damage. Lastly, the clamping voltage is the maximum voltage drop across the diode for a given peak current pulse [31]. A high power TVS diode was installed on the 28V bus of the main vehicle. The vehicle TVS has a breakdown voltage of 49V and a maximum clamping voltage of 55V. Because the LTM8027 was able to accept an input up to 60V additional input voltage protection was not required.

For redundancy, an additional TVS diode was added to the converter input. The diode selected was the 1.5SMC62CA produced by Littelfuse. Reverse standoff voltage for this diode was 53V and the minimum breakdown voltage was 58.9V up to a 65.1V maximum. The absolute maximum input voltage to the LTM8027 is 65V so the maximum breakdown is slightly over this limit. This overvoltage risk had to be weighed against the alternative that the breakdown voltage be too low. If the minimum breakdown voltage of the converter diodes were ever less than 55V the converter diodes would supplant the main TVS in protecting the 28V

power bus. This would destroy the module diodes as they cannot be rated to withstand the transients of the full vehicle bus. Thus the minimum breakdown of 58.9V, which always exceeds 55V, takes precedence over the small possibility that breakdown voltage reach 65.1V. Ultimately, transient protection is achieved by the main vehicle TVS which will suppress transient voltages to a maximum of 55V.

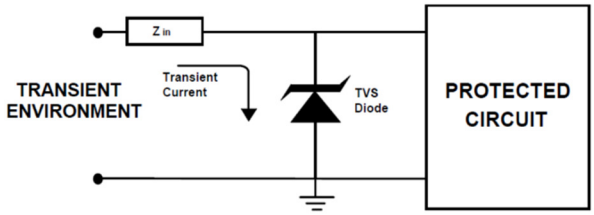


Figure 32. Operation of transient voltage suppression (TVS) diode Semtech, "Surging Ideas TVS Diode Application Note SI96-01." Samtech, www.semetech.com, 2000. Used under fair use 2014.

4.4 Power management element

4.4.1 Current sensing

Current monitoring will provide an analog reference for the overcurrent protection circuitry as well as the input to be sampled by the processing element ADC. The maximum signal voltage is set by the digital power supply to 3.3V. A shunt resistor was chosen as a simple and reliable method for current measurement.

A shunt resistor must be chosen in relation to a current shunt amplifier. The critical parameters for a current sense amplifier are common mode range, common mode rejection ratio and input offset voltage. Common mode range specifies the input voltage rating of the operational amplifier with respect to the amplifier ground. When sensing the current through a 12V line the common mode range must be greater than 12V. Common mode rejection ratio (CMMR) is defined as the ratio in dB of the differential gain of the amplifier to the common mode gain. CMMR is a measure the amplifier's ability to separate the small differential signal across the input terminals from the often large common mode signal present at both terminals. Input offset voltage is defined as the voltage that must be applied across the two input terminals to obtain an output of zero volts [32].

Input voltage offset is caused by an inherent mismatch between the input transistors and internal components of the op-amp. General op-amp offset voltages are in the order of mV for lower quality op amps down to tens of micro-volts for the highest quality components. This offset represents a DC bias that directly affects the accuracy and therefore the minimum voltage drop of a shunt measurement system. Measuring a shunt drop of 10mV using a cheap op-amp with 1mV offset would produce roughly a 10% error. The tradeoff then is between op-amp cost and shunt power loss. Power loss is proportional to shunt voltage drop so it is desirable keep the differential voltage to a minimum which requires an op amp with a very low offset voltage to preserve accuracy.

The desired low voltage drop of the shunt means that the amplifier must also provide gain to boost the signal to a useful range. In this amplification process a certain amount of gain error is introduced due to manufacturing and component tolerances. The gain error becomes the dominant error term as the differential voltage increases. Figure 33 [33] shows a plot of total error as a function of differential voltage for op-amps of differing offset voltage and gain error.

At lower differential voltages, offset error is the dominant effect. As differential voltage increases, the error converges to the gain error of the op amp.

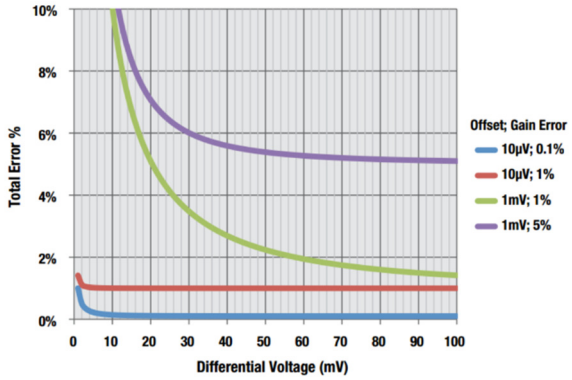


Figure 33. Plot of total error vs. differential input voltage for op-amps with different offset voltages and gain errors Texas Instruments, "Current Shunt Monitors," 2014. [Online]. Available: http://www.ti.com/lit/ml/slyb194a/slyb194a.pdf. Used under fair use, 2014.

With the offset and gain errors of the shunt amplifier established the effects of the sense resistor value can be explored. Figure 34 illustrates the relationship. Shunt voltage drop is a linear function of current with a slope set by the resistance value. Shunt amplifier error decreases exponentially toward the gain error limit. A curve of constant power is defined as the product of the current and shunt voltage drop. A usable range is defined by setting a maximum error and maximum power loss. The bottom limit is defined by the shunt amplifier error and the top limit is defined by the shunt voltage drop.

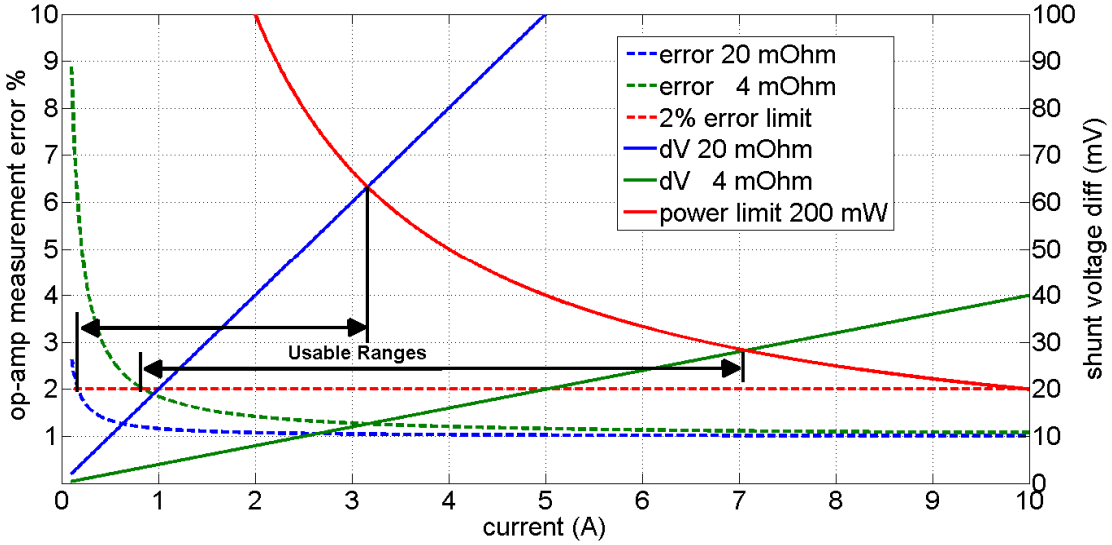


Figure 34. Amplifier measurement error and shunt voltage drop as a functions of current. With maximum power and error limits defined a usable range can be determined for any value of sense resistor.

The current sense amplifier chosen was the INA213A produced by Texas instruments. The INA213 has a common mode range from -0.3 V to 26 V quite sufficient for the 12V application. The minimum common mode rejection ratio is 100dB. The maximum offset voltage is ±100 µV with a typical value of ±5µV. The INA213 has fixed gain of 50 V/V with a maximum gain error of ±1% and a typical error of 0.02%. A 10 mΩ sense resistor was chosen to simplify the gain calculations. With a 4A max current the shunt power loss will be less than 200 mW. For typical values of offset voltage and gain error the measurement error will be less than 1% over the measurement range.

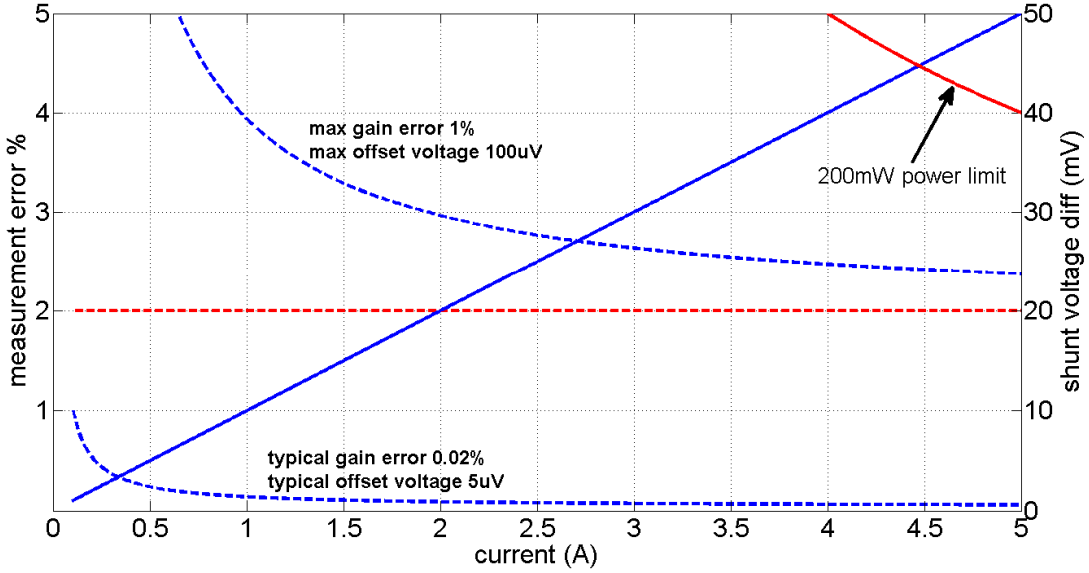


Figure 35.Maximum and typical error from INA213 over expected measurement range

The current to voltage conversion of the shunt measurement system is determined by the sense resistor value and the amplifier gain. The current sense resistor of 1 mΩ will provide a current to voltage ratio of 0.01. Multiplying this number by the amplifier gain will produce a total current to voltage ratio of 0.5. The full scale current range of 0-4 A will produce a 0-2 V output from the INA213 sense amplifier.

4.4.2 Comparator selection

The shunt amplifier output will also supply the analog reference for overcurrent protection. A comparator will be used to detect an overcurrent condition by comparing this shunt amplifier signal to a set reference. A comparator operates like a one bit analog to digital converter. When the non-inverting input is higher than the inverting input the output is high, otherwise the output is low. A current fault indicator can be created by referencing the non-inverting input to the shunt amplifier output and referencing the inverting input to a voltage representing the current limit. This will produce a logic high whenever the sensed current exceeds the limit.

The comparator state will enable and disable the output causing a continuous oscillation without a latching feature. When current rises above the threshold the output is disabled causing

the current to fall which in turn re-enables the output and allows current to trip the threshold again. A latching feature must be present so that the comparator will trip on the first overcurrent condition and remain in the OFF state until triggered by an external signal. Many comparator ICs have a built in latching feature allowing them to maintain their present state without regard to input changes.

Initial latching is triggered by the comparator output, as this is the fault indicator. Any signal originating from the comparator will be held constant after latching. Therefore, at least one additional external signal must be provided to un-latch the comparator when re-enabling the output is desired. A two input logic gate can be used to accomplish both these tasks. A truth table can be generated for the desired states as shown in Table 8. An exclusive logic gate is required because the output must be unlatched under two conditions. The output will be unlatched while both inputs are low and will unlatch again, as a reset, when both inputs are high. The specific logic levels will be determined by the comparator IC.

Table 8.Truth table for comparator latching feature

Comparator output	Reset signal	Latch state
Low	Low	Unlatched
High	Low	Latched
Low	High	Latched
High	High	Unlatched

Selection of the comparator was feature driven. As stated above a latching pin was required. Complementary outputs were desired to eliminate the need for an inverter. The device needed to operate on a 3.3V supply. An industrial temperature rating -40-85°C was essential. It was also critical to find a package that was not difficult to assemble with hand soldering techniques such as an SOIC 8 package. The desired features are summarized in Table 9.

The MAX 961 comparator was selected because it incorporated each of these features. The propagation delay of the comparator, an extremely fast 4.5ns, is more than sufficient for rapid transitions. A high logic latches the comparator so that an exclusive OR gate will provide the function of Table 8.

Table 9.Comparator features

Comparator features
Latching pin
Complementary outputs
3.3V supply
-40-85°C min temperature range
Simple package
Shutdown pin

4.4.3 Current limit adjustment

An adjustable current limit can be attained by varying the fixed reference to the overcurrent comparator. The current limit will be adjusted by means of a voltage divider with a digital potentiometer as seen in Figure 36. A two channel, 50 kΩ, 256 position digital potentiometer, the AD5243, was chosen to adjust the limit reference. To ensure a constant reference voltage for the set point a precision 2.5V reference was used as the voltage divider input rather than the main 3.3V supply. The voltage divider was designed to adjust the reference between 0 and 2V corresponding the maximum output current of the LTM8027. Using a 12.4kΩ value for the fixed resistor, produces a voltage range corresponding to a 0.156A to 4.013A current limit range. The current limit value is plotted as a function of wiper position in Figure 37.

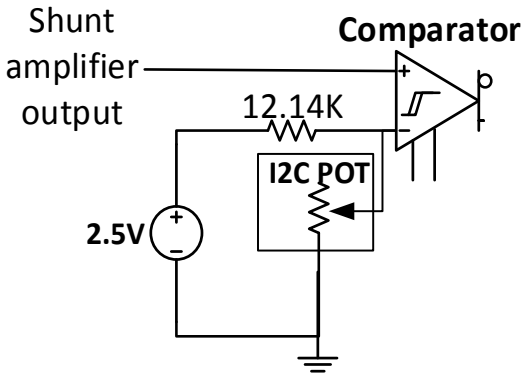


Figure 36. Current limit adjustment circuit using digital potentiometer

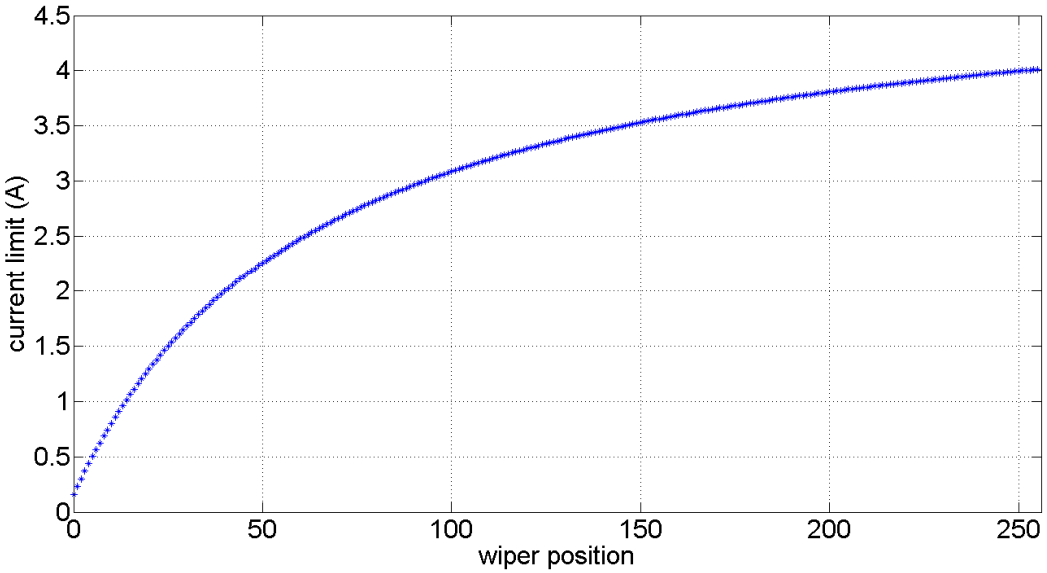


Figure 37. Current limit set point as a function of potentiometer wiper position

4.4.4 FET selection for output protection

To provide output protection, a device needs to be placed in the output path to disconnect the load in the event of an overcurrent condition. The location of the disconnect point in relation to the load, either high side or low side, must be considered carefully. High side refers to placement between the power source and load whereas low side refers to placement between the load and ground. Both locations will break the conduction path through the load.

For a low side break the device remains connected to the power supply output and thus energized. A high side break directly disconnects power from the load. High side placement is safer in general for both the power supply and load at the price of higher voltage ratings for the disconnect device. It was deemed essential for this application that both the power supply and load be protected. A low side disconnect cannot protect the power supply if a secondary path is established to ground. In a vehicle where the chassis is grounded it is conceivable that a secondary path could be established shutting down the power supply after its internal current limit is exceeded. A high side disconnect is necessary to protect the power supply and maintain any additional independent outputs.

With placement determined, the disconnect device can be chosen. The requirement for an adjustable current limit eliminates any form of resettable fuse from consideration. Mechanical and solid state relays are unsuitable due primarily to their large size compared to ICs. Power semiconductor devices are well suited to this application because many feature small size, high power ratings and convenient logic level interfaces.

Either an N-channel or P-channel FET could be used for this purpose. N-channel devices can be manufactured with low on resistances much more easily than P-channel devices. An online component search using the Digikey website provides a simple ballpark comparison of availability. In addition to N-channel and P-channel the devices were filtered using $R_{DS(ON)}$ less than or equal to 10mΩ and continuous drain currents greater than 10 A (these were added to ensure the devices were suitable for power applications). The search returned roughly 9000 results for N-channel devices and 500 results for P-channel devices. With an order of magnitude more low resistance devices, N-channel FETs offer greater design flexibility as well as the lowest possible on resistances. The downside to using N-channel FETs in high side applications is that they require a complex gate drive circuit as the gate voltage must be raised higher than the source which is equal to the input voltage when the FET is on. Though P-channel devices offer a more limited selection, they are simpler to drive in high side applications as the gate voltage need only be pulled lower than the source to enable the output.

The output protection FET, though it does need to switch rapidly, does not need to switch continuously as was the case for SMPS gate drivers. This allows greater margin for switching losses and power consumption since switching occurs infrequently during normal operation. Continuous losses however, such as the drain–source resistance heating must be minimized, as the FET will conduct for the majority of the time.

The basic parameters can be readily determined from the output conditions. The continuous drain current must exceed 4A. The blocking voltage must be greater than 12V when the output is off. The gate charge, and ON resistance should be as low as possible, likely around 5-10 mΩ. Another important requirement is that a SPICE model be available from the manufacturer for simulation purposes.

A P-FET from Vishay Siliconix the Si7143DP was chosen meeting these specifications. The gate charge is a low 24.6 nC and the ON resistance is 10 mΩ at a V_{GS} of -10V. The

continuous current is 35A and the blocking voltage is 30V. The threshold voltage is a 2.8V maximum. Most importantly, the Si7143DP has a spice model supplied by Vishay for simulation purposes.

4.4.5 Gate driver for output FET

A level shifted P-channel MOSFET driver was selected to drive the Si7143DP as presented in [21]. The level shifter is comprised of R1, R2, Q1, Q2, and M2. The gate drive signal is input to the FET M2 to drive the gate of the primary FET M1. The resistors R1 and R2 determine the switching speed of the FET M1. The ratio of R1 and R2 sets the voltage at the base of the transistors and the sum of R1 and R2 controls the current flow through both the transistors and resistor divider. Both the switching speed and FET power loss are determined by R1 and R2.

The goal of resistor selection is to reach an acceptable balance between the continuous losses when the FET is on and the switching time of the FET. The continuous losses are comprised of two components. The first is from the gate drive level shifting components which can be well approximated by just considering the resistive losses of R1and R2. The second continuous loss component is the resistive loss in the primary P-channel FET M1.

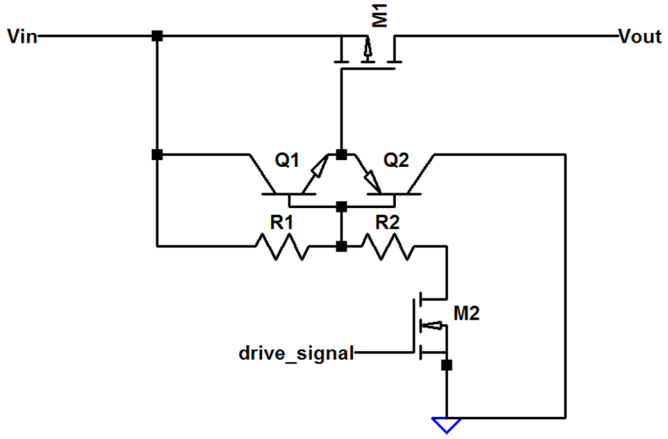


Figure 38. P-channel level shifting gate driver

The losses of the level shifter will be considered first. The largest component of these driver losses is the resistive loss of the R1 R2 voltage divider. The steady state power consumption of R1 and R2 can be calculated as

$$P = \frac{Vin^2}{R1 + R2} \tag{22}$$

These losses are plotted in Figure 39 as a function of total resistance (R1+R2). When the total resistance is low, significant power is lost because continuous current flows through the voltage divider. As total resistance increases the power loss approaches zero. Significant power savings are obtained as resistance increases from 2.4k to around 24k after which, further increase yields diminishing returns.

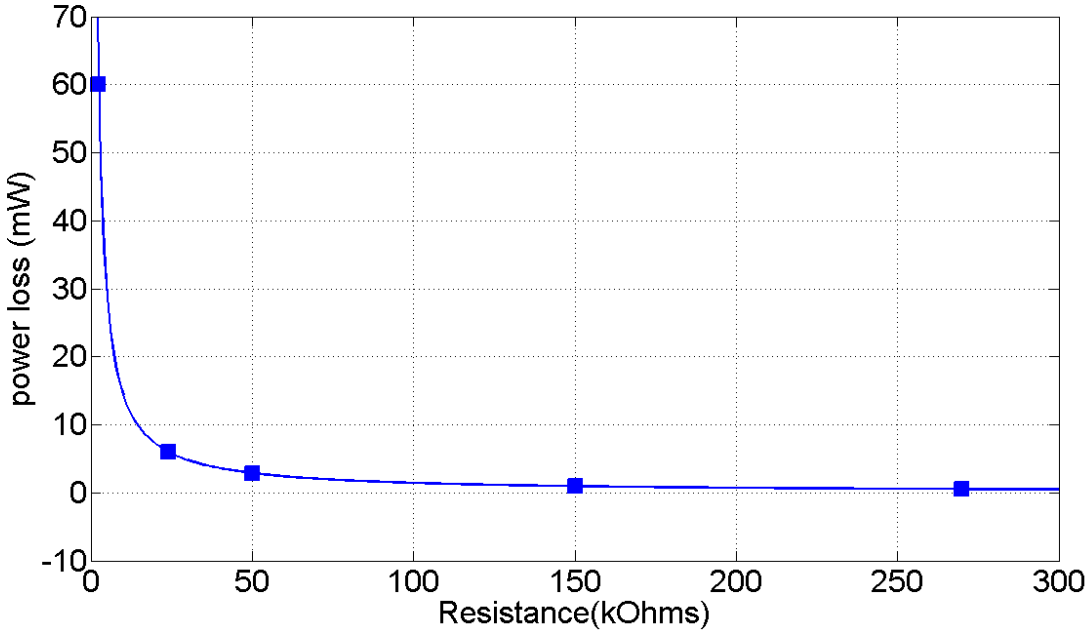


Figure 39. The continuous power loss is inversely proportional to total resistance.

The losses in the FET are proportional to the drain source resistance, R_{DS}, of the MOSSFET M1. The relationship between R_{DS} and the gate source voltage V_{GS} is illustrated in the datasheet where R_{DS} is given for two values of V_{GS}. For the Si7143DP, R_{DS} is 10mΩ when V_{GS} is -10 V and 18.6 mΩ when V_{GS}=-4.5V. In general then R_{DS} decreases as the voltage difference between the gate and source increases.

The FET losses are determined by V_{GS} which is proportional to the voltage divider ratio R2/(R1+R2). The FET losses as a function of V_{GS} were simulated in LTspice by changing the ratio of R1 and R2. Figure 40shows the simulated results for a continuous current of 4A. The FET losses are reduced by more than half as $|V_{GS}|$ is increased from 3V to 11.4V. These two relations show that ideally R2 should be small in comparison to R1 so that V_{GS} will be close to -12 V and the sum of the two resistors should be sufficiently large, around 24kΩ, to reduce the continuous losses through R1 and R2.

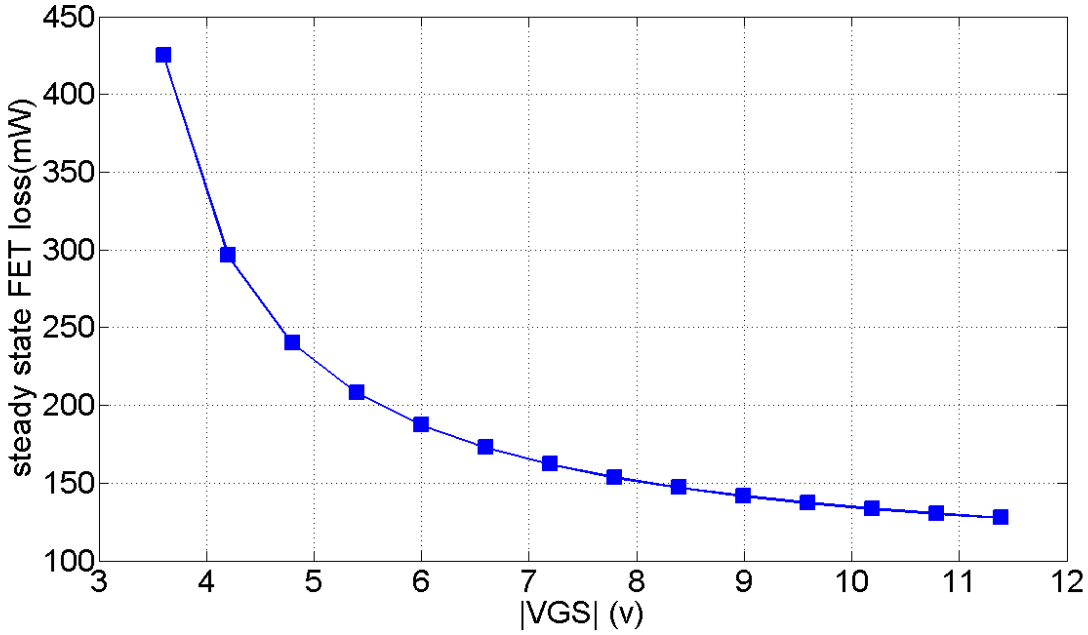


Figure 40. Simulated steady state power loss of output FET as VGS increase from the threshold to -11.4V

The last factor to consider in resistor selection is the switching time required for the FET to turn off. MOSFETs are charge controlled devices as discussed in section 2.4. The transition time is therefore determined by the gate capacitance of the FET and the amount of current available to charge and discharge this gate capacitance. The gate charge is determined by the characteristics of the Si7143DP so that transition time can only be affected by the amount of gate drive current supplied.

Current flows into and out of the gate of M1 through the emitters of the transistor pair Q1 and Q2. The emitter current is proportional to the current entering the base of the transistors which is a related to the current flow through R1 and R2. Therefore, the lower the sum of R1 and R2 the faster the FET can transition.

These effects were simulated by changing the sum of R1 and R2 while keeping the ratio, R2/R1, constant at 0.526% to reduce R_{DSON} of the main FET. The results are plotted in Figure 41. As expected, the 10% settling time t_s increases with total resistance R_t in a nonlinear fashion. Somewhat surprisingly, the FET is unable to transition after the total resistance becomes sufficiently large around 270 kΩ.

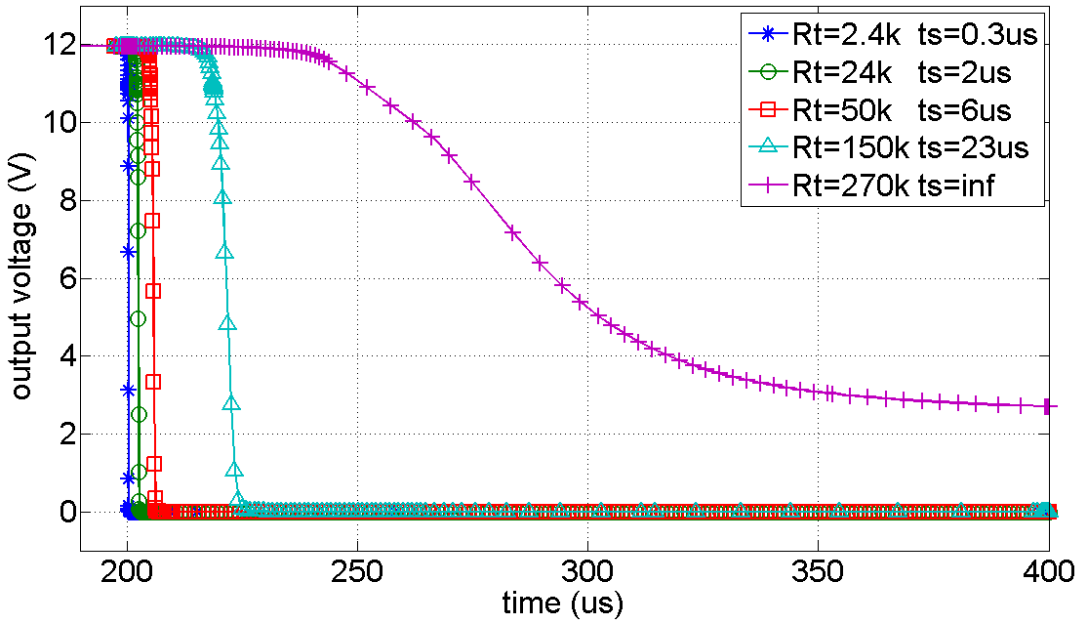


Figure 41.Simulated output voltage transitions for five different values of total resistance (R1+R2) and constant ratio (R2/R1) of 0.0526

This inability to switch arises from the real world non-ideal behavior of the semiconductor devices which is reflected in the simulation models. For hand calculations the FET M2 is considered to be an open switch when the output FET M1 is in the off state. In actuality, there is a finite leakage current into the drain of M2. A more realistic model for M2 would be a bi-valued resistor. In the on state, the resistance is very low, equal to R_{DS} of M2 around 100mΩ, in the off state the resistance is very high, around 1MΩ, when calculated in simulation. This means that two voltage dividers are present in the circuit giving two equations for the voltage at the base of the transistors.

$$V_B = V_{in} * \frac{R2 + RDS_{M2ON}}{R1 + R2 + RDS_{M2ON}} \quad RDS_{M2ON} \ll R2 \tag{23}$$

$$V_B = V_{in} * \frac{R2}{R1 + R2} \tag{24}$$

$$V_B = V_{in} * \frac{R2 + RDS_{M2OFF}}{R1 + R2 + RDS_{M2OFF}} \quad RDS_{M2OFF} \gg R2 \tag{25}$$

$$V_B = V_{in} * \frac{RDS_{M2OFF}}{R1 + RDS_{M2OFF}} \tag{26}$$

When M2 is on, the resistance is small compared to R2 so the base voltage is given by the voltage divider of R1 and R2 equation (24). The resistance of M2 in the OFF state is very large compared to R2 so that the base voltage is given by the resistor divider of R1 and $R_{DSM2OFF}$ equation (26). As can be seen from equation (26), if R1 is sufficiently large, the base voltage will not rise high enough to exceed V_{TH} and the FET will not enter the cut-off region. Because the currents flowing during the M2 off state are very small, in the 10μA range, the voltage divider, equation (26), will be effected by leakage currents such as those into the transistor bases. Equation (26) only illustrates the effect of R1 on the gate source voltage of the FET and cannot be used to calculate a specific R1 value above which transition is prevented.

The final values for R1 and R2, 47kΩ and 2.2kΩ respectively, were chosen to balance transition speed and continuous power loss. The sum of R1 and R2 is close to 50kΩ reducing the resistive divider losses to nearly 3mW. The sum is not so high that transition speed suffers. A 10 % settling time around 6us should be expected. The .0468 resistance ratio will result in a VGS lower than -11V minimizing the conduction losses of the FET.

4.5 Communications interface

CAN was chosen as the industry standard communications interface over which the modules send messages and receive commands. A CAN bus was already present on the base vehicle and CAN is a standard protocol for automotive applications. Three wires are required to form the bus, CAN high, CAN low and ground. The low number of wires was beneficial in reducing the number of pins needed for the input connector.

4.6 Processing element

The processing element was chosen based on a set of desired features rather than specific performance requirements. The processing element is used to execute user commands and oversee the protection and current monitoring features of the smart power module. Though a microcontroller was selected for this purpose, the processing element in no way affects the internal control loops and compensation of the LTM8027 conversion element. The microcontroller is housed on a smart current board separate from the conversion element on the smart power board. As can be seen in Figure 42**,** the microcontroller only has connections to the current sensing and current limiting aspects of the smart current board with only a temperature sensor on the smart power board.

The most crucial requirement was that the microcontroller be well supported in terms of programming environment, online support and laboratory expertise. Laboratory expertise was mostly limited to Texas Instruments and Atmel product lines, both of which are well supported by online resources and programming environments. The next most limiting requirement was dictated by the choice of CAN as the communications interface as the majority of microcontrollers do not include peripherals for CAN. This narrowed the search to the Texas Instruments C2000™ and ARM® lines of microcontrollers. The C2000™ model had the added advantage of extended operating temperature ranges of -40-125°C. The smallest C2000™ model which still had the desired CAN peripherals was chosen as the processing element, the 64 pinTMS320F28030.

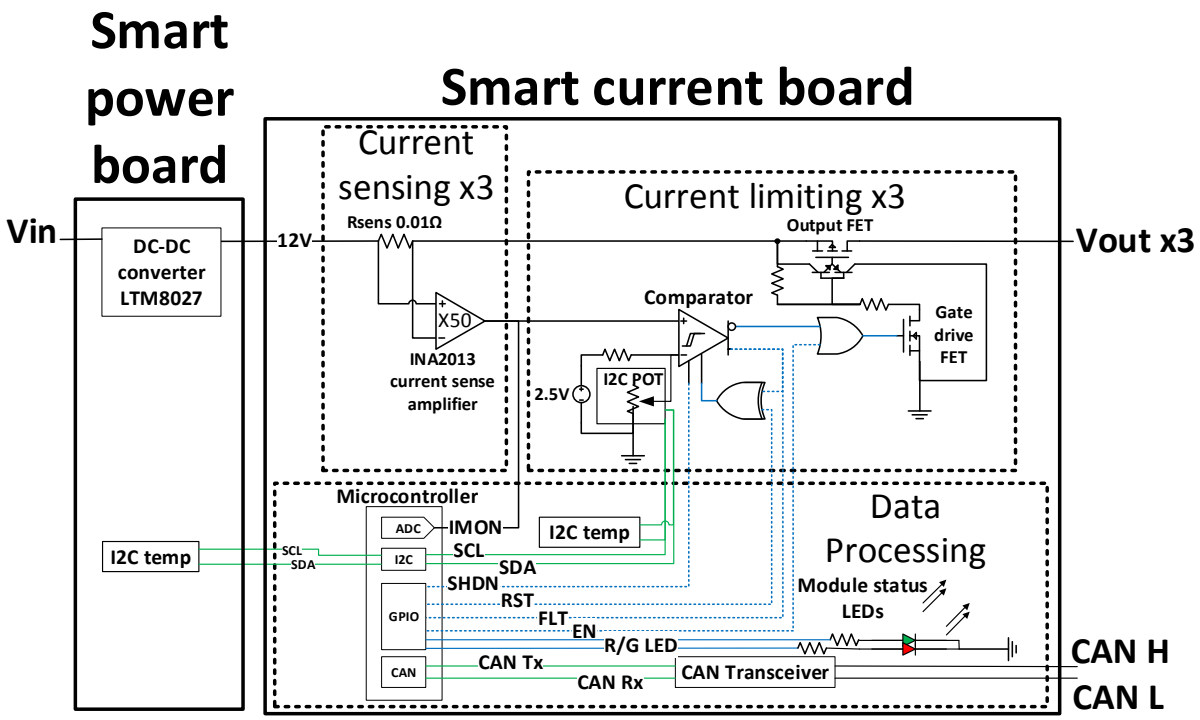


Figure 42. Functional diagram of smart power module

4.7 Module status element

Arguably the most important feature, an LED was chosen for the module status element. LEDs provide visual information through both color and pattern. Color provides perhaps the clearest indication of module state with green indicating proper function and red indicating the presence of a fault condition. A single two color LED will be used to conserve space. Taking into account the possibility of blinking the LED this provides at least 5 different messages that can be easily conveyed to the user as seen in Table 10.

Table 10.Summary of LED visual messages

Visual messages
Solid red
Solid green
Blinking read
Blinking green
Red-green alternating

The primary requirement for the LED was that it could be directly driven by the micro controller pins with only the addition of current limiting resistors. This meant that the forward voltage of the LED had to be less than 3.3V. A three wire design with a dedicated ground was preferred over a two wire design. The size of the LED needed to be small 5mm or less to conserve space. Lastly, the LED had to be a panel mount variety. The device chosen was the SSI-LXR4815IGW3B15 manufactured by LUMEX.

4.8 Module output considerations

To implement a practical distributed power network, a compromise needed to be reached between module size and the number of module outputs. The power conversion element and the processing element both have flexibility for multiple outputs. At 48W continuous power the LTM 8027 could power up to three of the device in the roof location from Table 4. Assessing the IO requirements per channel of output protection, it was found that the TMS320F28030 could support up to 3 outputs as well. Given the space overhead already needed to accommodate the conversion element, processing element, connectors and module status element additional output channels could be added without increasing the overall enclosure size. Given these considerations, it was decided that each smart power module would have three independently controlled and monitored output channels. Thus two modules could be located in the roof to supply the roof power needs and one module each could be located in the front and rear of the vehicle.

4.9 Enclosure selection

For convenience, an IP65 extruded aluminum electronics box was chosen from Hammond Manufacturing. The box is comprised of a central aluminum extrusion with card guides and two end caps with seals in between. The two end caps provide the possibility to gain access through the back side without removing connectors on the front a feature that proved invaluable during device testing. The overall external dimensions of the box were 3.54 x 2.44 x 1.34 inches. This left ample internal dimensions of 3.11 x 2.2 x 1 inches.

The only significant draw back to the extruded aluminum enclosure was thermal performance. Thermal conduction is achieved by maximizing surface contact between the printed circuit board and the metal enclosure acting as the heat sink. The ideal enclosure thus would have a means to apply pressure to hold a circuit board against a flat metal surface. The card guides provide very little contact for heat removal and no means of applying pressure. To address thermal concerns, a two circuit board design was adopted. The most significant heat source, the conversion element, would be constructed on a separate board from the other circuit elements. This converter board would be connected to a heat sink baseplate by means of several screws. The baseplate would then be epoxied to the base of the extruded aluminum enclosure to provide a direct cooling path to the case.

The second circuit board, for which cooling was not a concern, would be inserted using the card guides. Figure 43 shows a picture of an assembled smart power module next to a CAD model with a cutaway to revel the two internal circuit boards. Only the front panel needed to be altered to accommodate the connector and status LED providing easy back panel accesses to the debugging interface.

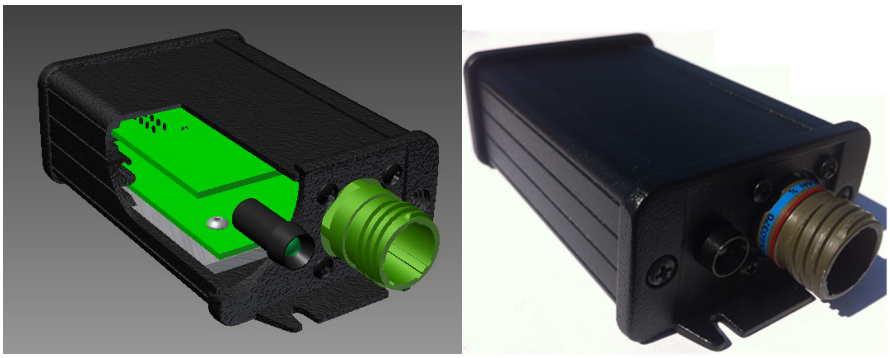


Figure 43. Enclosure for smart power module with cutaway showing two printed circuit board

4.10 Circuit board layout

The smart power board, containing the conversion element, and the smart current board, providing the monitoring and protection features, are shown in Figure 44. The smart current board was designed so that all of the ICs were located on the top side of the PCB for easy assembly using a hot plate. A single 20 pin Molex connector is located on the bottom side of the board with a 3.3V converter and eight capacitors and resistors. A 40 pin header, located on the back edge of the board, contains the programming pins and any signals important for debugging. This connector can be easily accessed when the back panel of the smart power module is removed.

The smart power board contains the LTM8027 and its external components. The board was designed to match the layout recommended in the datasheet. Many thermal vias are present beneath the conversion element providing a conduction path to the heat sink beneath. The 12pin connector contains input and output power connections as well as I2C lines and a 3.3V input for the LM73 temperature sensor. Convenient test points are located near the input and output capacitors for accurate voltage measurement during efficiency testing. An extra set of test points is placed where it can be reached through the back panel.

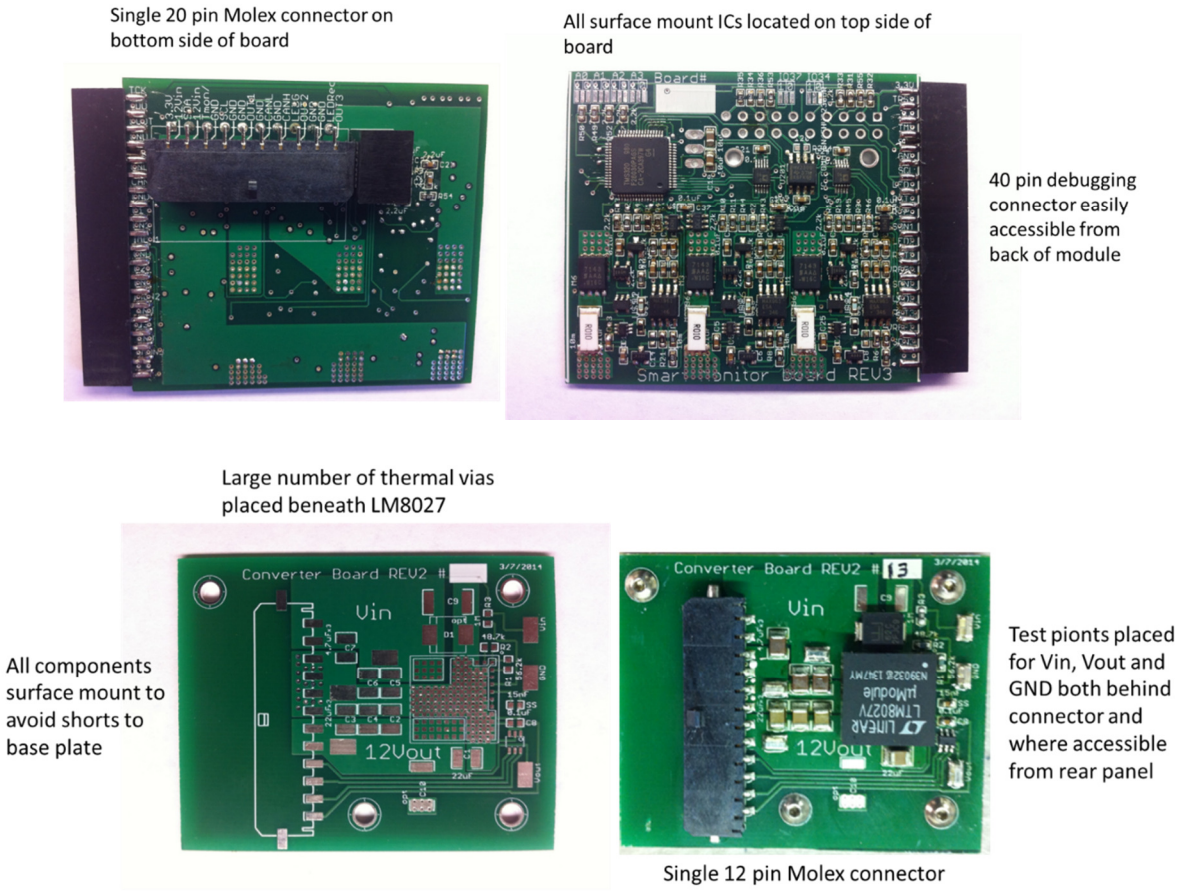


Figure 44. Images of smart current board (top) and smart power board (bottom) photo by author, 2014.

Chapter 5: Results

This section details the testing and implementation of the smart power modules. First the conversion efficiency of the LTM8027 is evaluated and the measurement setup is explained. An average efficiency of 96.7%, above a 1A load, was calculated from eight different conversion elements with 24V inputs and 12V outputs. Load regulation is calculated from the same data as 0.447% an acceptable value slightly higher than the datasheet listing of 0.2%. The output ripple was measured using oscilloscope features to be 49mV peak-peak at max load comfortably below the targeted maximum of 60mV. Thermal performance of unmodified conversion elements closely matched the datasheet trend rising from14°C to 60°C above ambient over the full load range. A nearly 70% reduction in temperature rise was achieved when the conversion elements were secured to a heat sink in contact with the aluminum enclosure. The new temperature rise of 4-22°C provides ample margin for smart power module operation in environments with elevated temperature.

The gate driver turn off time of the output protection is verified against the simulation. The measured turn off time of 18.4µs was roughly three times larger than the simulated 6.1µs. Output protection and overcurrent detection are verified showing scope images of module operation. Following installation in the vehicle, it was discovered that transient inrush current spikes up to 26A were tripping the over current protection and preventing startup of vehicle sensors. The spikes were measured and characterized using an external shunt. A fault tolerance was added through software by extending the reset pulse to allow brief overcurrent spikes to subside. User control through CAN commands is verified. Lastly, the efficiency cost of the processor overhead is calculated to be a 5-7% reduction from that of the 96.7% conversion element efficiency.

5.1 Conversion element efficiency

Efficiency is defined as the ratio of input power to output power which is the product of voltage and current in an electrical system. Four quantities then, input voltage, output voltage, input current and output current must be known in order to calculate efficiency. Each of these quantities was measured using a four channel Agilent Technologies InifiniiVision digital oscilloscope as shown in Figure 45. Input and output voltages were measured directly. The outputs of two INA213 amplifiers provided voltage representations for the input and output currents. All the grounds were connected in common. The scope was set to capture 2000 data points for each input quantity at a sampling rate of 4 kHz. The voltage data along with the time stamp was saved to a flash drive for analysis.

The load current was varied using a resistive load bank composed of up to 10 resistors in parallel. The resistors were varied in sets of two in order to reduce the number of load values to 5 per converter. Efficiency data was collected for eight converter modules in a randomized order. The order of the five load values was randomized for each converter along with the specific resistors that made up each load value. Two replicates were taken for each converter. The average input voltage, output voltage, input current and output current was found for each data set and used to calculate a single efficiency point per data set. With two replicates a total of eighty efficiency points were calculated. The results are shown in Figure 46. The average efficiency, represented by the black line, reaches a maximum value of 97.46% at a load of 2.66A. The overall mean efficiency is 96.67%.

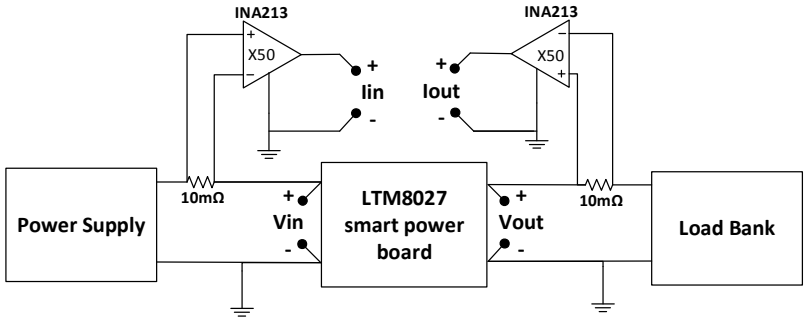


Figure 45.Measurement set up used to calculate conversion efficiency of smart power board

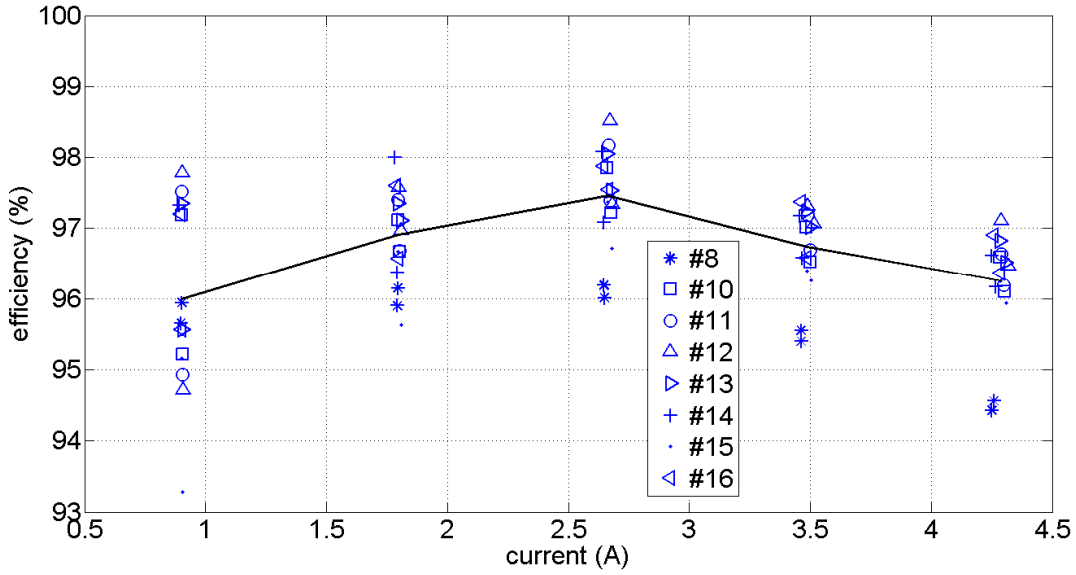


Figure 46.Calculated efficiency for eight LTM8027 converter modules Vin=24V Vout=12V

5.2 Load regulation

Load regulation refers to the ability of a converter to maintain a fixed output voltage across changing load conditions. Load regulation is defined as

$$\%\ load\ regulation = \frac{Vout_{\max load} - Vout_{\min load}}{Vout_{nominal}} * 100 \quad (27)$$

Load regulation was measured using the same data set collected for efficiency calculations. Figure 47 shows the output voltage as a function of load current for the eight converters measured. The total average output voltage was 12.15V with a variance of 3.0426e-05V. The output increases slightly with load, a trend consistent across converters. For each converter the five voltage data points were sorted in order of increasing load. The nominal load was defined as the middle point of this data set. Load regulation could then be calculated by taking the difference of the first and last values and dividing by the middle value. The average load regulation was calculated to be 0.447% with a variance of 0.0022%.

The calculated load regulation of 0.447% was larger than the datasheet value of 0.2% by more than a factor of 2. The voltage conditions were nearly identical to those of the datasheet, 24V input and 12V output. The load conditions were different however with datasheet range of 0≤Iout≤4A while measured conditions were 0.89A≤Iout≤4.32A. Some difference can be expected considering the test conditions exceeded the max rated current of the device. With the increasing voltage trend, extending the load range would produce a higher load regulation. The measured load regulation is still better than 0.5%, more than adequate for the intended application.

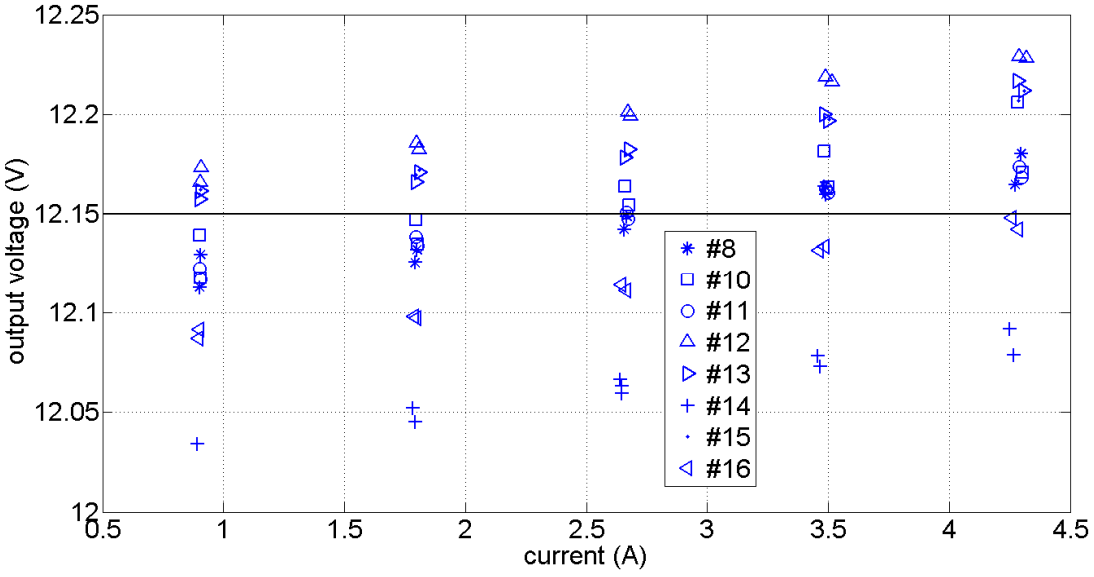


Figure 47. Converter output voltage as a function of load current

5.3 Output ripple

Converter output ripple was measured using the InifiniiVision digital oscilloscope. Ripple voltage was measured at two load levels. The low load was 2 resistors in parallel approximately 1A and the high load was 10 resistors in parallel close to 4.3A. The measurement features of the scope were used to measure the frequency and peak to peak ripple of each waveform. Scope images were saved for each test. At low load the average peak to peak ripple was 36mV increasing slightly to 49.46mV at high load. The peak to peak ripple at max load is ±0.2% of the average output voltage at full load, 12.19V. The calculated voltage ripple is less than the ±0.5% target requirement. An example scope image of the maximum output ripple is shown in Figure 48.

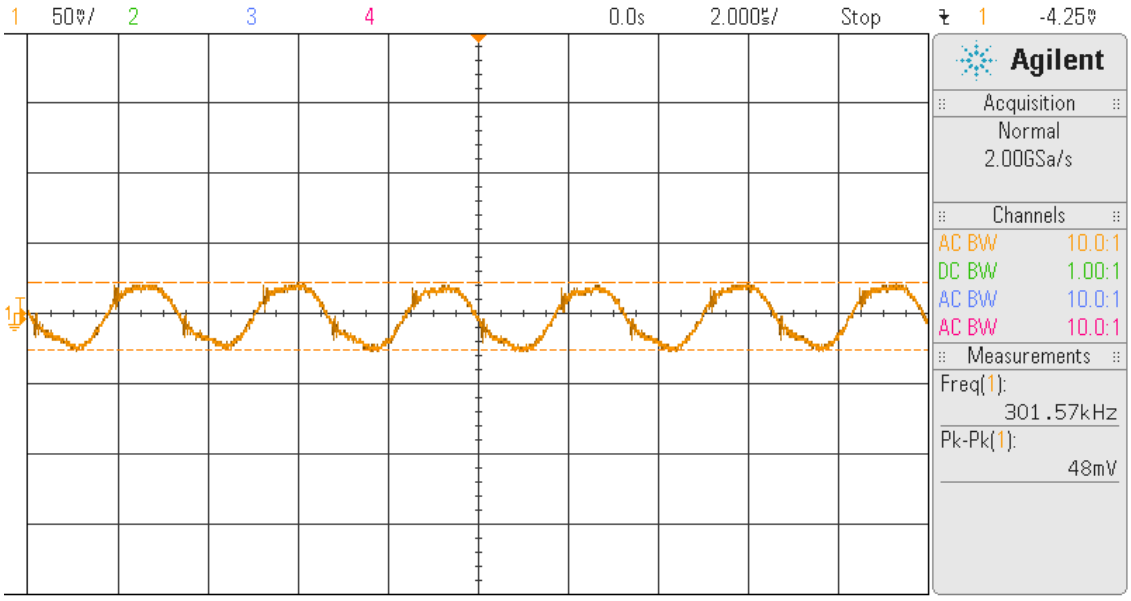


Figure 48. Scope image of output voltage ripple at 4.3A maximum load

5.4 Thermal Performance

The goal of thermal evaluation was to determine the effectiveness of using the enclosure as a heat sink and to estimate the temperature rise from ambient for the heat sink enclosure. The temperature of the converter boards was monitored using the LM73 temperature sensor located on the surface of the smart power boards. An external circuit board was used to read the temperature values over the I2C bus and display them to an LCD screen. First the circuit boards were run without any thermal enhancement. The boards were suspended in a vice with rubber ends to minimize conduction paths. The load was varied from 0 to 4.2A. Sufficient time was given for the temperature to reach a steady state after each load increase.

The temperature rise from ambient calculated for each load level is shown in Figure 49. The LTM8027 datasheet provides an estimated temperature rise. The unmodified boards demonstrate temperature rise similar to that of the datasheet with slightly higher values above 2A loads. The temperature rose from about 14°C above ambient at no load to 60°C above ambient at 4.2A output.

Heat sinking was then added by connecting each board to an aluminum baseplate which was epoxied into an extruded aluminum enclosure. Thermal compound was spread between

each material interface to improve conduction. The enclosure containing the circuit board was suspended in a vice in the same manner as the unaltered boards. The temperature was recorded at each load in the same manner as before to calculate a temperature rise from ambient. The temperature rise for the converter with heat sinking varied from 4°C up to 22°C above ambient. This is a reduction of 10-38°C compared to the unmodified boards.

The results of this thermal analysis show that the unmodified boards demonstrate thermal performance comparable to thermal data provided in the LM8027 datasheet. Heat sinking to the enclosure reduced the temperature rise by 60-70% compared to the unmodified boards. With nearly 25°C temperature rise at full load, ample margin is provided for operation at elevated ambient temperatures without approaching the 125°C max operating temperature of the LTM8027.

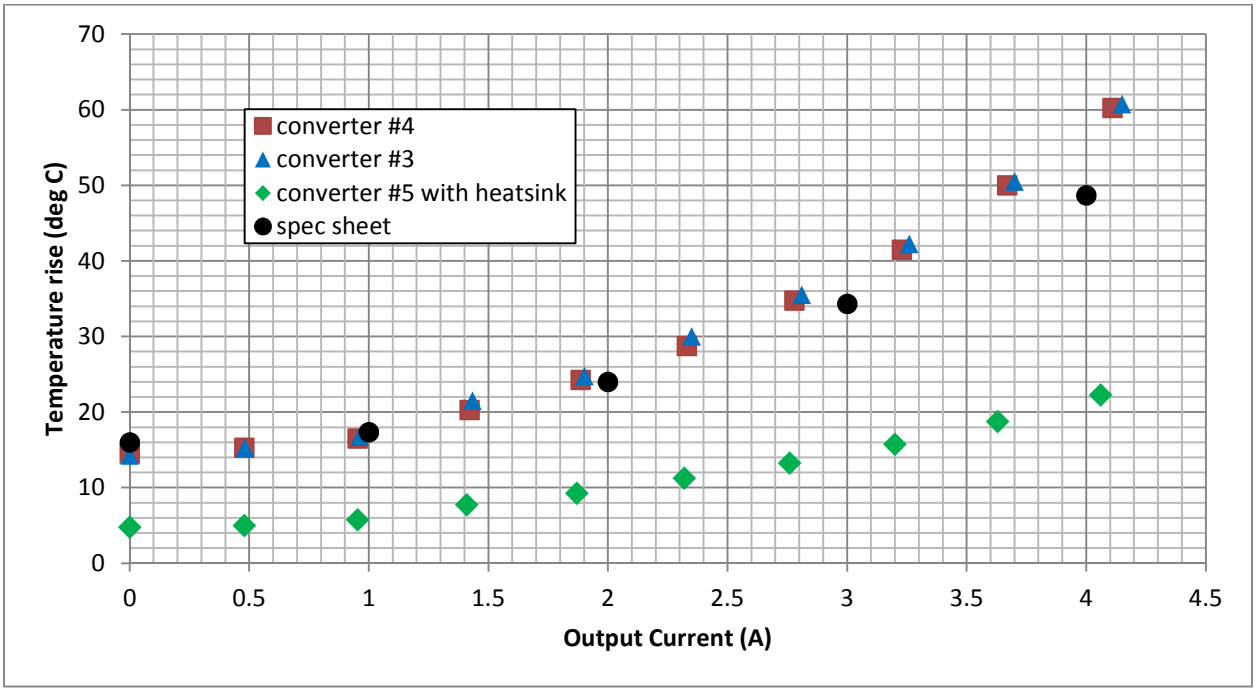


Figure 49. Thermal evaluation of smart current boards showing temperature rise from ambient

5.5 Gate driver verification

A single output FET and gate driver was assembled on a printed circuit board and tested against the simulation model. The physical values of R1 and R2 were measured using a digital multimeter as 46.8kΩ and 2.18kΩ. The resistance of the load bank was measured to be 5.7Ω. The simulation model was updated with these values as shown in Figure 50. An Agilent Technologies InifiniiVision digital oscilloscope was used to measure the waveforms of the physical circuit and provide the gate dive trigger signal. The trigger signal used was a 2.5 kHz waveform pulse of 200µs width and 3.3V amplitude. This pulse signal was applied to the gate of the FET M2. The output voltage and the gate voltages of FETs M1 and M2 were measured and saved to a CSV file. The measured trigger signal VG2 was converted to a PWL file and used as the gate drive source, V2, in the simulation model.

Measured and simulated results are compared in Figure 51. The turn off transitions measured in the physical circuit follow the expected trends from simulated behavior. Timing

differences exist between the real and simulated waveforms. The simulated output voltage has a 10% settling time of 6.1µs while the 10% settling time of the measured output voltage is 18.4µs nearly three times larger. The settling time can be divided into two regions one where the output remains constant and one as the voltage transitions. For comparison purposes, the transition time was characterized by the time required for the voltage to fall from 90% to 10 % of its initial value. The delay time was then defined as the difference between the 10% settling time and the transition time. The transition time of the simulation is 0.964µs making the delay time 5.14µs. Measured transition time was found to be 3.95µs giving a delay time of 14.48µs. For each of these comparisons the difference is roughly a factor of three shown by the percent error between the simulated and measured settling times of -201.85%. This large difference must be placed in the proper context by considering that the model is accurate to within 13µs.

The differences between simulated and measured results can be attributed to several factors. The presence of ringing in the measured output is the result of parasitic inductance within the physical circuit, not accounted for in the simulation. The transition time is most directly influenced by the intrinsic capacitances of the output FET which cannot be fully captured in the model. The ability of the simulation to show transition time to within 13µs is certainly superior to any approach using hand calculations. Simulation succeeded in providing a solid understanding of the gate drive operation and reasonable expectation of performance.

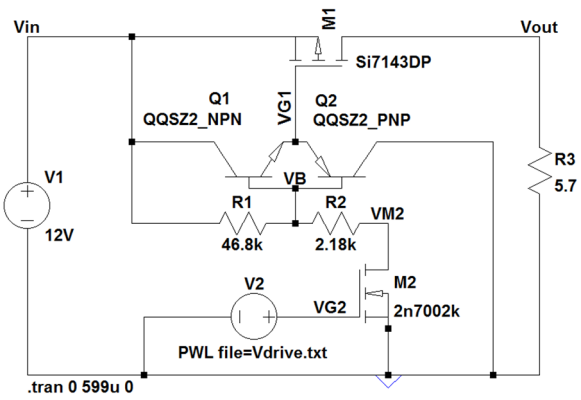


Figure 50. LT spice circuit used for gate drive validation. The resistors have been updated with their measured values.

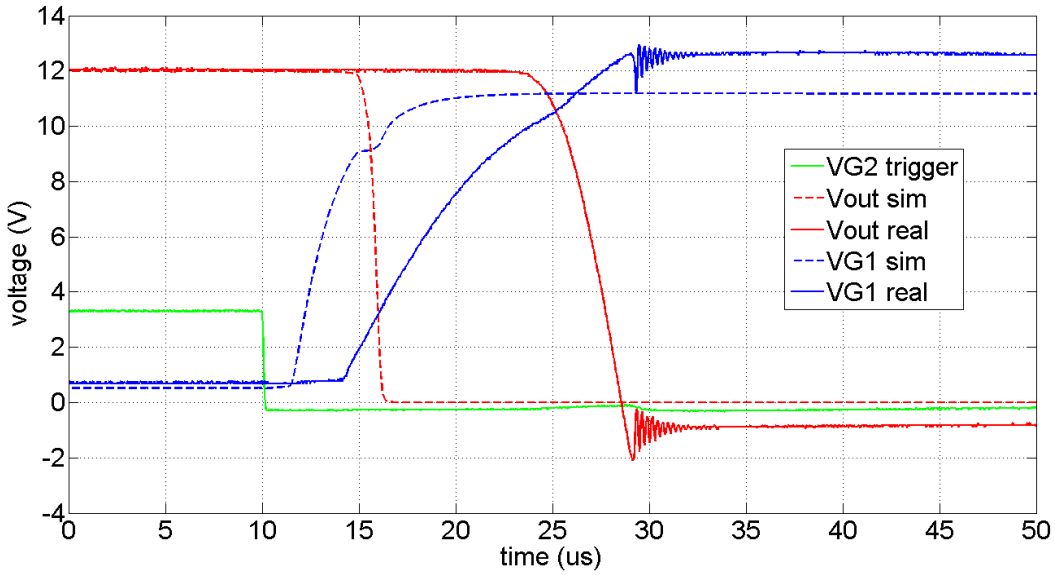


Figure 51. Comparison of simulated and measured gate drive waveforms.

5.6 Output Protection

Gate drive testing verified that the analog circuitry was capable of protecting the outputs from overcurrent conditions. The digital interface was necessary to integrate this protection ability in an effective manner. This section outlines the current limiting protection features as they function in the real operation of the smart power modules. The modules were programmed to provide immunity to intermittent faults by initiating a set number of reset attempts. After the number of resets is exhausted the channel is disabled until further user input. Overcurrent trips and resets are shown by means of scope capture images.

Throughout this section, the module operation will be illustrated by means of scope images. Figure 52 shows the physical meaning of the scope traces within the actual circuit. Imon and Vref are the two inputs of the comparator. Vref sets the current limit threshold to which Imon, the shunt amplifier output, is compared. FLT is the output of the comparator which is fed to one input of the XOR gate which latches the comparator. RST is a digital output from the microcontroller which allows the comparator to be unlatched and reset. The four traces are colored to match the colors of the scope images for convenient identification.

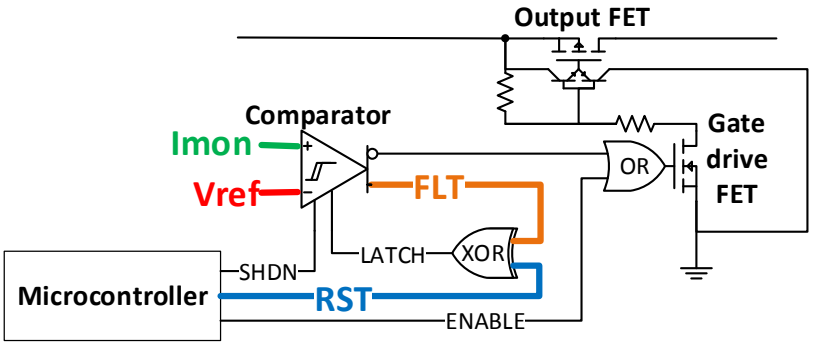


Figure 52.Physical meaning of scope traces Imon, Vref, FLT and RST within the circuit

An overcurrent trip is shown in Figure 53. As Imon exceeds the reference threshold, the comparator output, FLT, rises indicating a fault. Not shown in the image, the complementary output to FLT falls turning off the main output FET indicated by the falling voltage on the Imon pin. The output current falls to zero in less than 25us after the overcurrent is detected. The rising edge of the comparator output, which could rise as quickly as 3-5ns, was slowed by the addition of a 0.1µF capacitor for a rise time closer to 5µs. The capacitor was added to provide filtering and slow the transition time to reduce ringing. As later sections will explain, the small delay introduced has no detrimental effect on the practical performance of the output protection.

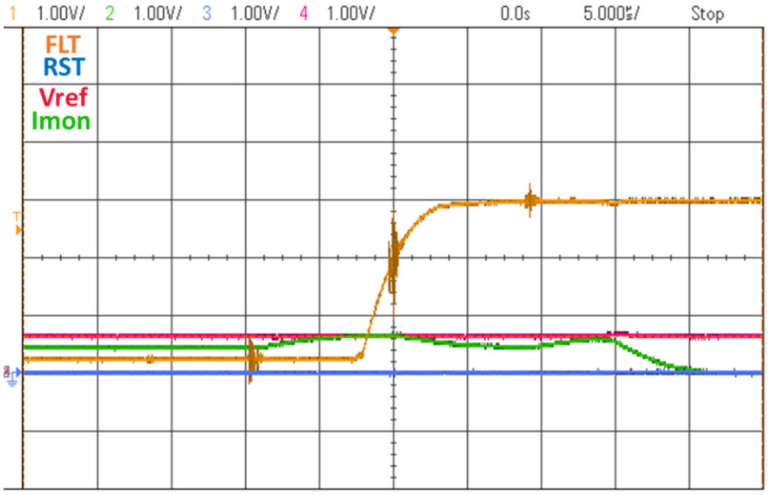


Figure 53. Overcurrent trip: as Imon exceeds Vref, the voltage of FLT rises shutting down the output FET and causing Imon to fall to zero

A reset sequence is examined next in Figure 54. At the rising edge of the reset pulse, the comparator is unlatched because both inputs of the XOR gate are high. Because Imon is still zero FLT returns to a logic low. The output is re-enabled and Imon rises again to a level exceeding Vref. The rising of Imon illustrates an important function of the reset pulse. Only the rising edge of the pulse is needed to clear the fault, when RST and FLT are high together for a matter of nanoseconds. Immediately following the rising edge then, the reset pulse itself latches the comparator in an un-faulted state allowing current higher than the limit to flow to the load.

This situation could be prevented by making the length of the reset pulse less than 6µs so that it would unlatch the comparator before Imon began to rise. In this manner, it could be ensured that very little current was allowed to flow in excess of the limit. As explained in the next section, the ability to allow overcurrent conditions for brief intervals proved essential in practical implementation.

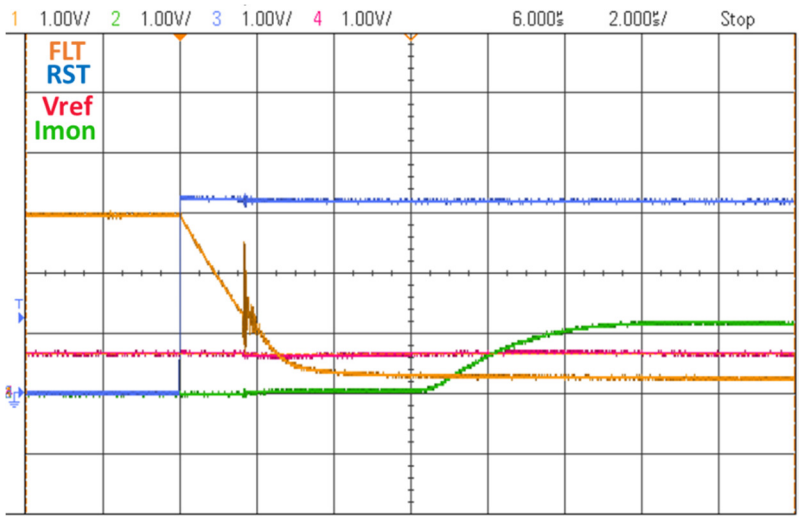


Figure 54. The rising edge of the reset pulse clears FLT allowing current to rise as the output is re-enabled

After the falling edge of the reset pulse, the comparator is again unlatched and able to function. If the overcurrent is present, as is the case of Figure 55, the comparator almost immediately returns to a faulted state. This causes the output FET to shut off and Imon fall to zero again. Imon reaches zero almost exactly 24µs after the falling edge of RST. This is an increase of only 6µs from the turn off time measured in the gate drive verification of section 5.5.

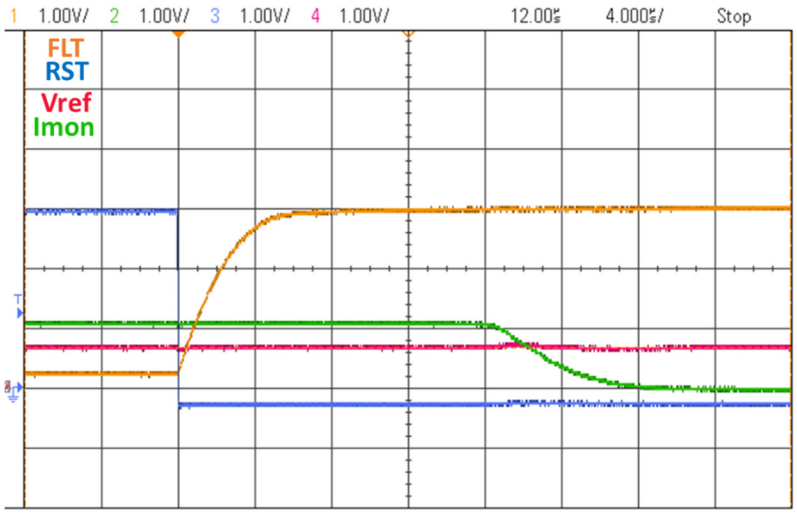


Figure 55. Falling edge of reset pulse with the overcurrent still present FLT immediately rises to a logic high disabling the output

With the high sensitivity of the modules, some software provisions had to be made to handle intermittent faults and brief current spikes. This was accomplished by the addition of an overcurrent counter which kept track of the number of times the current limit was tripped. Following an initial fault, a reset pulse is sent and it is noted by the microcontroller whether or not the fault returns. If the fault returns, the overcurrent counter is incremented and additional

resets follow. After a total of ten faults, that is, nine reset attempts, the microcontroller disables the output flagging it as a continuous fault.

A continuous fault is shown in Figure 56. Nine resets are attempted 250µs apart, after which FLT remains in a high state. Figure 57 shows an intermittent fault which is successfully cleared by the reset pulses of the microcontroller. The addition of the overcurrent counter allows intermittent faults to be cleared by the microcontroller without the intervention of a user command. If a continuous fault is detected the output is disabled until further user input is provided.

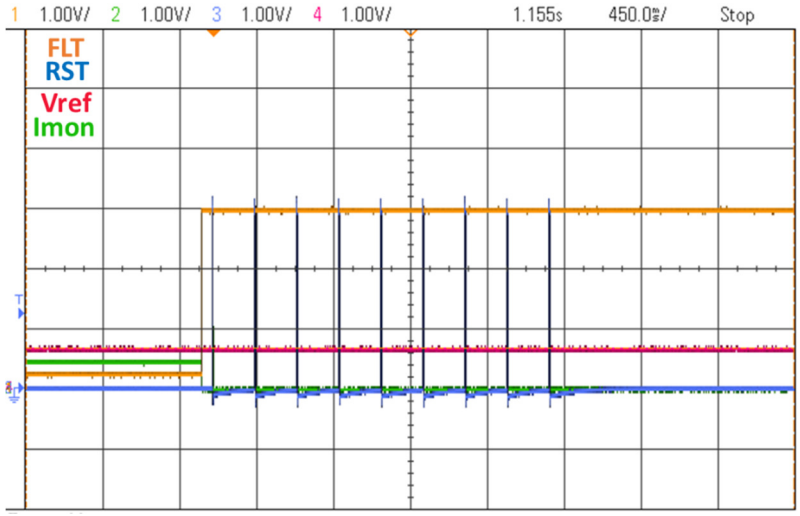


Figure 56. Continuous fault with nine automatic reset attempts initiated by the microcontroller

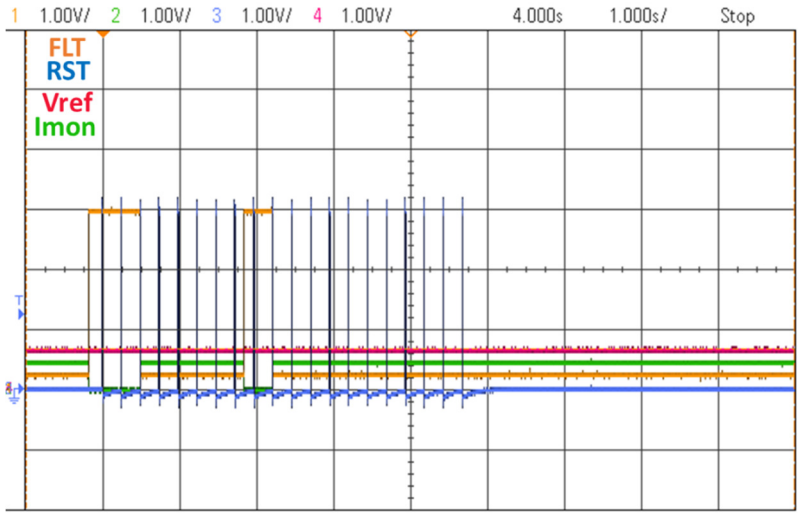


Figure 57. An intermittent fault which is cleared successfully by the microcontroller

5.7 Detection of inrush current transients

Once integrated into the vehicle power system the measurement sensitivity of the smart power modules provided unexpected insights into sensor operation. It was discovered that the power up sequences of several vehicle components were preceded by high inrush current spikes (up to 26A) of very short duration (50-100µs). Initially, the smart power modules prevented startup of all but one Velodyne sensor due to the current limiting protection. After further investigation, the current spikes were discovered and measured. A software fix was implemented which used the latching feature of the comparator to provide an overcurrent delay much like a slow blow fuse.

When the smart power modules were first installed in the vehicle, only one sensor, a Velodyne in the rear, was able to power successfully. The other sensors were disabled by the overcurrent protection of the modules. The oscilloscope image of Figure 58 shows an unsuccessful start up attempt of the front Velodyne. (The colors differ from the previous analysis with Imon now being blue and RST green) The fault is cleared on the rising edge of a 100µs reset pulse. While the reset pulse is high, the comparator is latched in the low state allowing the shunt amplifier output to exceed the 4A reference and rise to the power supply rail. The fault returns immediately following the falling edge of the reset pulse when the comparator unlatches. Railing of the shunt amplifier indicates that a current larger than 6.6A is being supplied to the sensor. This was unexpected in itself considering the continuous current rating of the module was only 4A.

By disabling the fault protection of the smart power module the full startup current could be measured using an external 100mΩ shunt resistor. The voltage difference was measured using a single oscilloscope probe referenced to the low side of the shunt. Figure 59 shows four measured start up transients from the rear Velodyne. The full transient duration is about 160µs but the18.5A peak current is reached in less than 20µs. The four startup current spikes are very similar in shape and duration indicating that a consistent transient is present during each power up sequence. The transient is most likely the results of reactive components within the Velodyne which is an actuated, rotating sensor.

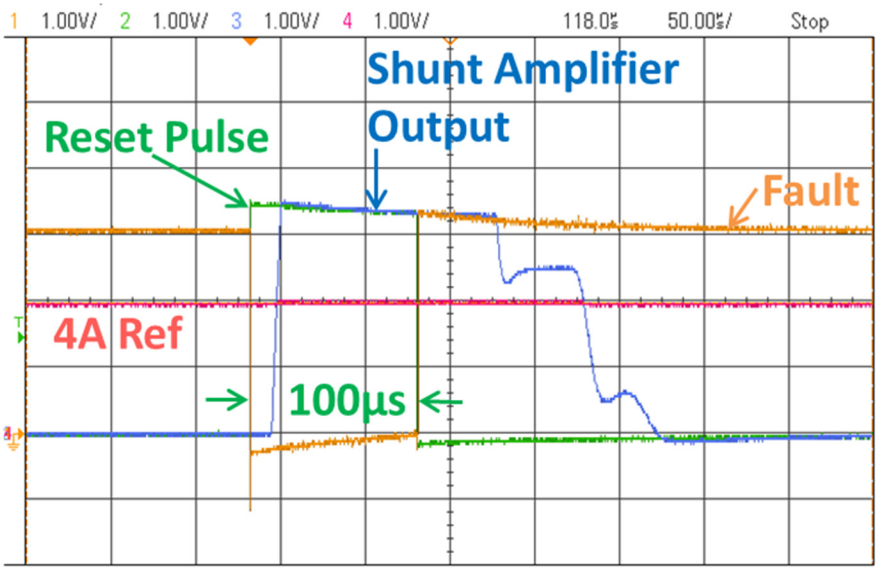


Figure 58. Scope capture from unsuccessful front Velodyne start up

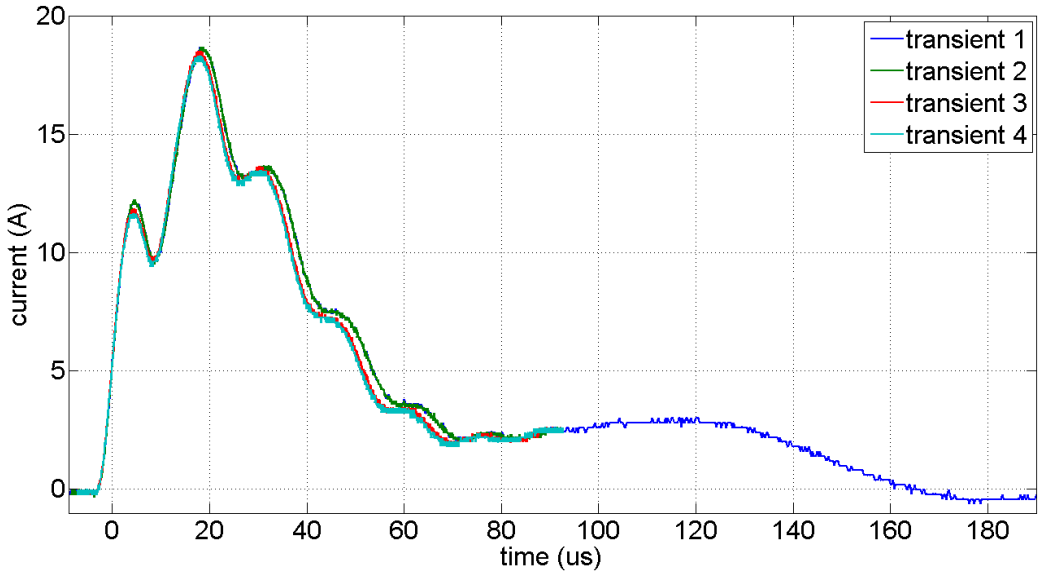


Figure 59. Four start up transients from rear Velodyne consistent in shape and duration

5.8 Overcurrent tolerance through reset pulse

Successful power up had to be ensured for all sensors. The amplitude of the current spikes, 18.5A, ruled out a measurement adjustment solution. It was unreasonable to extend the range past the expected operating conditions by more than 5 times just to measure 50µs transients. A simple solution was presented in the successful startup of the rear Velodyne. The reset pulse affects the comparator in two ways. The rising edge of the pulse releases the comparator from its faulted state while the remainder of the pulse latches the comparator in its new un-faulted state. In Figure 60, like the previous sequence, the fault is cleared on the rising edge of the reset pulse. The reason that the fault remains cleared is that the transient falls and remains below 4A before the 100µs reset pulse ends. Thus the length of the reset pulse provides a window in which overcurrent conditions are ignored and transients can subside. In this manner, the output protection acts like a slow blow fuse with a tunable fault time. All that remained was to measure the startup transients of each smart power component and set an appropriate pulse duration.

It was found that the vehicle radio also exhibited a consistent current spike with a peak of 26A and duration of 160µs. These two consistent current spikes are shown together in Figure 61. Both the perception camera and the video encoder experienced start up transients though not of a constant nature. The video encoder sometimes had a double current spike requiring a 700µs pulse duration to enable start up. Two resets of the video encoder are shown in Figure 62 one of which displays a double spike. It appeared that the startup spikes of the video encoder and camera were not completely random but rather related to the power history of the components. It seemed that different spikes were exhibited on initial power up than those seen following a power cycle.

Because the goal was only to ensure proper startup, no study was undertaken to confirm or characterize any time dependence of the inconsistent devices. A pulse with of 700µs was sufficient to ensure proper startup of all the vehicle components supplied by smart power

modules. The final pulse length however was extended to 5ms to safeguard against future anomalies and possible changes in operating conditions.

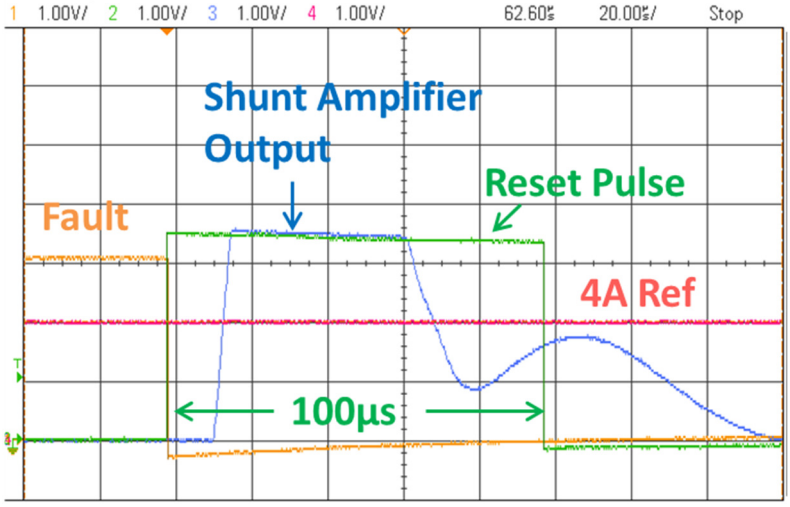


Figure 60.Successful startup of rear Velodyne

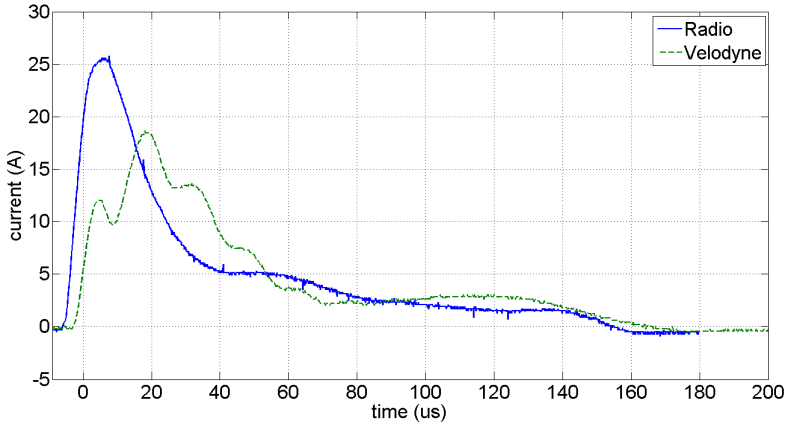


Figure 61. Startup current spikes from Velodyne and vehicle radio

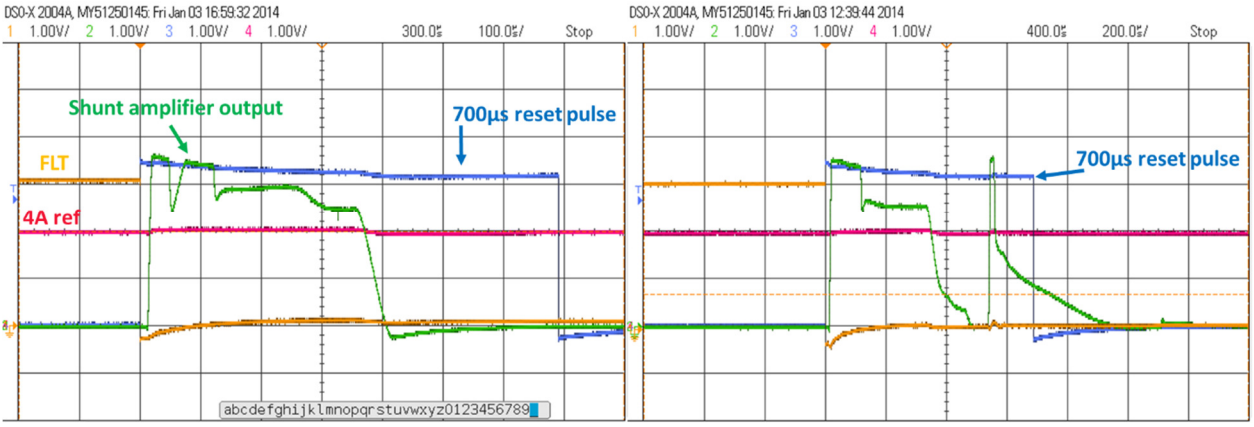


Figure 62. Two video encoder reset sequences taken on the same day. One subsides in less than 400µs while the other needs more than 600µs due to the second spike.

5.9 Module interface over CAN

The CAN bus provides a means for the module to send pertinent data to the vehicle computer and receive commands from the user. Each smart power module sends two periodic update messages both at a rate of 0.5 Hz. The first contains information regarding whether any intermittent or continuous faults have occurred and the ADC value for the output current of each channel. The second message contains the temperature values of the two temperature sensors, one for the power supply and the other for the monitoring board.

Command messages can also be sent by the user to each smart power module. The messages give the user the ability to control any of the smart power module features affecting the output conditions. This includes adjustment of the current limit threshold, enabling and disabling of the output, resetting of the output following a continuous fault and bypass of the current limiting feature. Figure 63 shows the adjustment of the current limit threshold by means of a CAN message. Once the message is received by the smart power module the module processor sends an I2C command changing the reference through the digital potentiometer.

The current limiting feature can be disabled by means of a CAN command as shown in Figure 64. This is accomplished using a GPIO as the second input of the OR gate controlling the gate drive FET of Figure 52. When ENABLE is high Imon is able to rise despite the state of the comparator. A command can be sent to restore the current limit allowing the comparator to drive the output FET and disable the channel.

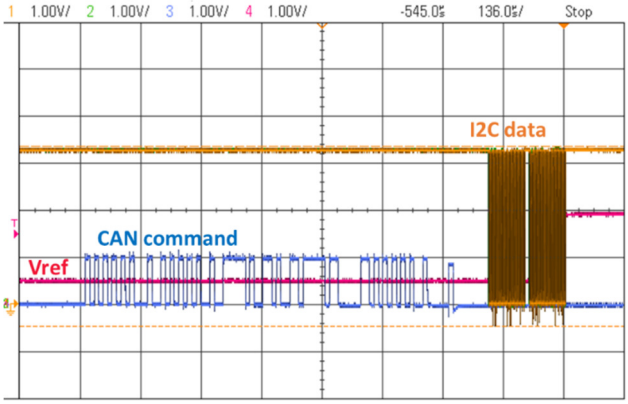


Figure 63.Adjustment of the current limit threshold by means of a CAN message

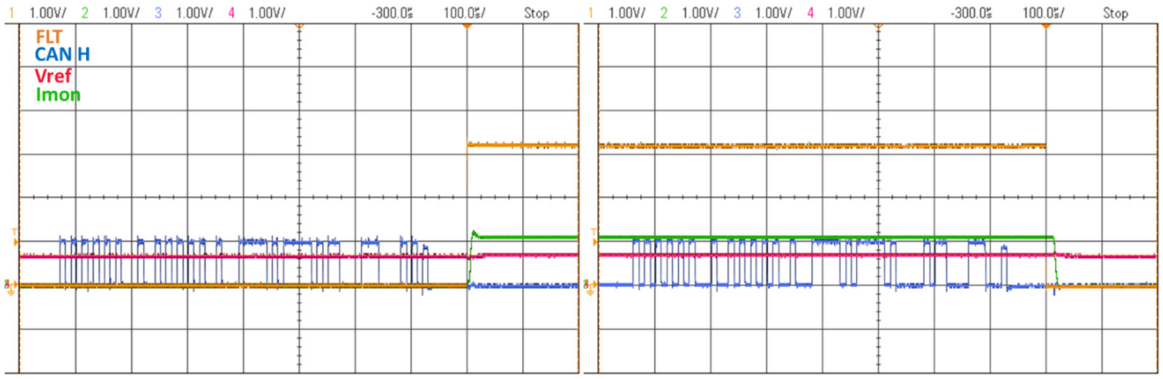


Figure 64. CAN message sent to bypass the comparator (left) and disable the comparator bypass (right). The first command is a means to ignore the current limit and forcibly enable the output while the second restores the protection feature.

5.10 Efficiency cost of current monitoring features

This section calculates the power overhead of the current monitoring features. The overhead is calculated in terms of efficiency loss by measuring the efficiency of the complete smart power module and subtracting this from the efficiency of the conversion element alone. The efficiency of the full smart power module was measured by the same method and configuration used for the conversion elements in section 5.1. The only difference being that the output voltage was measured at the output connector of the smart current board.

The efficiency was calculated for conversion elements #14 and #16 each paired with the same current monitor board. The comparison is shown in Figure 65. The green data points are the calculated efficiencies for conversion elements #14 and #16 while the lower blue data points represent efficiencies calculated for smart power modules #14 and #16. The efficiency cost is taken as the average difference between the two data sets ranging from 6.7-4.9%. The shape of the efficiency cost corresponds to a constant current offset. A smart current board draws close to 70mA at 12V. At lower output currents this 70mA offset represents a higher percentage of the total load current and thus a larger efficiency cost. It is important to understand the cost of adding protection features. The benefits of current monitoring and protection are valued above the 5-7% efficiency reduction.

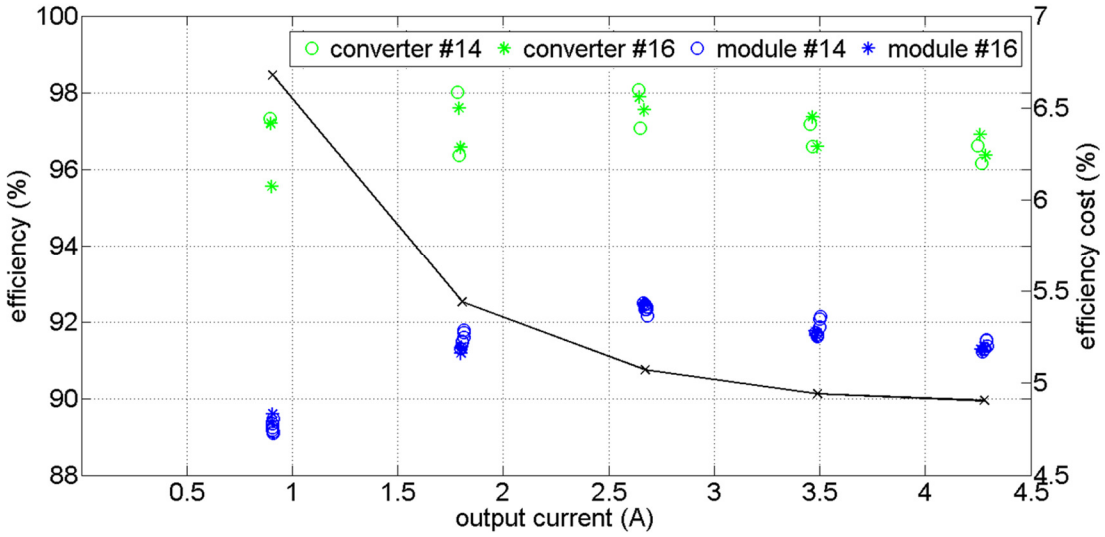


Figure 65. The efficiency cost of monitoring and protection features as a function of output current

Chapter 6: Conclusion and future work

The necessary hardware has been established to realize high efficiency, current measurement, current limiting, and output protection. Future work on the smart power modules will focus primarily on software development to expand the module capabilities. The present firmware of the modules handles basic functions of current monitoring, output control and communication. The processor will perform automatic functions such as resetting intermittent faults as well as executing user commands including current limit adjustment, output enabling and comparator bypassing to disable current limiting. A status message containing the current monitor ADC values and state of each output is sent at a 0.5 Hz rate.

Expanding the current monitoring capability could enable power health monitoring and anomaly detection for the vehicle sensors. The dynamics and intricacies of sensor operation are reflected in the current being supplied to each sensor. By increasing the sampling rate of each channel these intricacies can be examined and classified. The module software would need to be upgraded to handle the resulting increase in data collection. Possibly an SD card or other solid state memory could be added to allow large current buffers to be stored within each smart power module and read out, when desired, to provide high resolution current profiles.

The expansion of module features however must be considered in light of efficiency cost. Steps can be taken to streamline the existing firmware to reduce processing power consumption. Further improvement may be gained by the selection of a lower power processing element. Choosing a new microcontroller would present an excellent opportunity to integrate and simplify the module analog and digital interfaces using the experience acquired up to this point. Components could be reduced by using comparators within the processor instead of analog ICs. A serial or CAN boot loader could be implemented to update firmware without gaining physical access to each module.

6.1 Power health monitoring

The current monitoring feature of the smart power module has the ability to provide detailed insight into the operation of the vehicle sensors. The intricacies of sensor operation are visible in the current profile of each device. Figure 66 shows a scope image of current supplied to the four sensors in the roof of the vehicle, measured using the smart power module shunt amplifiers. The scope image shows that two components, the radio and waysight, have a cyclic nature to their supply current. Both the waysight and radio communicate wirelessly to the vehicle operator. The cyclic current may correspond to transitions between a low power receive mode and a higher power send mode. As Figure 66 illustrates, the operation of each sensor is imprinted in the supply current. Current monitoring then provides a very basic means of measuring and characterizing sensor operation.

Current monitoring history is invaluable as a debugging aid during vehicle development. When a component fails in testing it is imperative to have a hard data log to diagnose the cause of failure, rather than resorting to speculation. Data logging can also be used to characterize the expected operation of the vehicle sensors for the purposes of anomaly detection. With this data it could become possible to detect sensor degradation, and other unexpected behavior.

The smart power modules send current information at a rate of 0.5 Hz, sufficient to convey the average current on each channel but not fast enough to capture the current dynamics of each sensor. The base measurement hardware is present in the smart power modules to achieve the high sampling rates needed for power health feedback. Software would need to be developed to manage the high volume of data produced. Streaming such a large number of data points would be impractical and unhelpful in the general vehicle operation. A more reasonable approach might be to store a large buffer of high resolution current data within each smart power module which could then be transmitted to the vehicle computers when an anomaly such as a fault was detected.

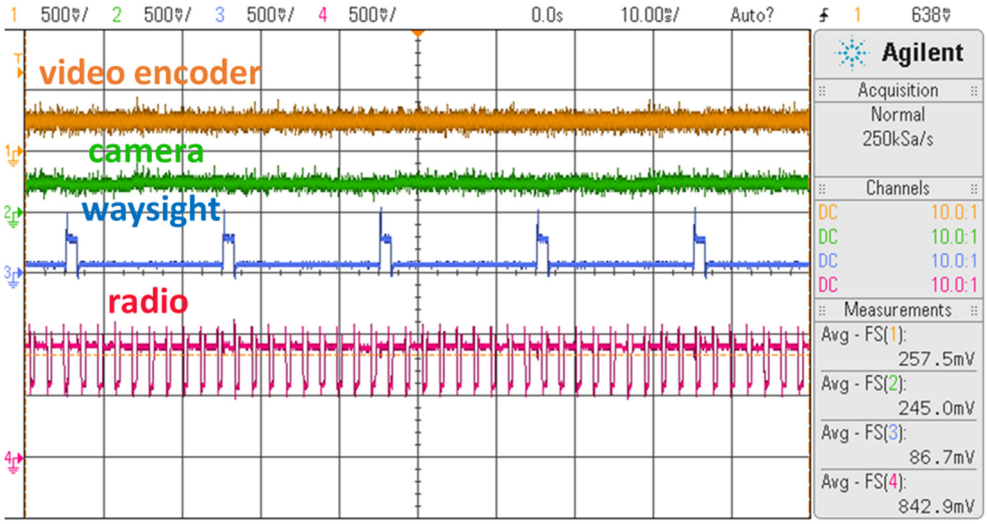


Figure 66. Current draw profiles of roof rack sensors measured using the smart power modules

6.2 Sampling

The sampling rate of the current sensors has to be increased to allow for the full range of the current sense amplifiers. As shown in Figure 67 [34] INA213 has the lowest gain in its amplifier family allowing measurement of dynamics up to 30 kHz. The roll-off of the amplifier gain bandwidth product will be used to provide an anti-aliasing filter. Using a sampling rate of 700 kHz would provide 20 dB of rejection above the Nyquist frequency. The 60MHz clock of the TMS320F28030 can easily accommodate a 700 kHz sample rate.

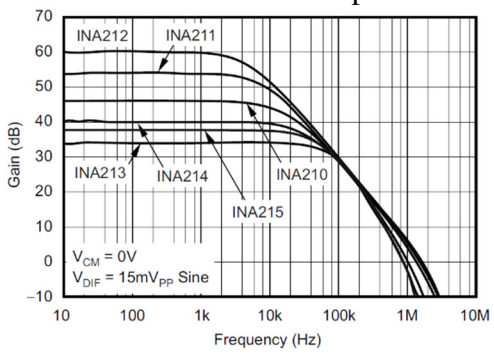


Figure 67. Gain-bandwidth product of INA213 Texas Instruments, "INA21x Voltage Output , Low- or High-Side Measurement , Bidirectional , Zero-Drift Series , Current-Shunt Monitors." Texas Instruments, Dallas, 2014. Used under fair use, 2014.

6.3 Reduction of measurement cost

Reducing the efficiency cost of the smart power module features is an area for further development. The power draw of the processing element is the primary contributor to the measurement related efficiency loss. Methods can be explored to streamline the existing code to reduce computational power consumption. New microcontrollers can also be considered which are specifically designed for low power operation. This would leave many factors open to reconsideration in light of the design experience gained.

Consideration could be given to a new communications protocol. CAN was selected as the industry standard communications interface for the smart power modules somewhat arbitrarily. The decision was influenced by the fact that a CAN bus was already present on the base vehicle. When the system architecture was defined, the smart power CAN bus was made separate from that of the base vehicle negating this advantage. The choice of CAN notably limited the options available for a processing element. Removing the requirement for CAN could open up potential for simpler processing elements with lower power consumption.

More thought could be devoted to the programming interface. The firmware of the smart power modules was uploaded using a Blackhawk XDS100V2 j-tag programmer. This j-tag programmer is only suited for development purposes due to its large number of connections (seven) and short wire length between target and programmer (6 inches). In order to update the firmware the back panel of each smart power module needed to be removed to access the seven programming connections. Once the modules were installed in the vehicle, it became very difficult to remove modules from the roof to upload new firmware. Future development would benefit from the ability to upload firmware without gaining physical access to the modules. Implementation of a CAN or serial boot loader could be explored in conjunction with selection of a new processing element.

6.4 Conclusion

Sensors are spatially distributed in unmanned ground vehicles by distances up to the full body length, 15-17 feet in many cases. Sensor power however is generally supplied from a centralized location where one or more large conversion elements are housed. This centralized approach has a detrimental effect on thermal performance by concentrating all the heat lost in conversion at a single location. For many vehicles used in the 2007 DARPA urban challenge cooling was accomplished through the stock air conditioning systems without modification. In subsequent work on open frame Polaris vehicles such as the GUSS system, heat removal from the centralized power electronics became a significant concern. Ultimately, 14% of the GUSS power budget was dedicated to active cooling of the electronics enclosure. Distributing sensor power by placing power supplies in close proximity to the geographically diverse sensors offered a distinct advantage for passive cooling.

A survey of sensors used on GUSS and vehicles of the DARPA Urban challenge revealed that the majority of devices require less than 50W individually. This result confirmed that a sufficient degree of uniformity is present to implement a standard power module in a distributed network. The relatively low power requirement of 50W was also conducive to using small conversion elements which could be conveniently mounted near sensor locations.

A smart power module was developed to provide distributed sensor power in an unmanned ground vehicle. The module used a highly efficient LTM8027 µModule® as a conversion element demonstrating an average efficiency of 96.67% above 1A loads. Current

sensing was achieved using a low offset voltage current shunt amplifier. The analog shunt reference was input to a high speed comparator for overcurrent detection. The current limit was made adjustable by means of an 8 bit digital potentiometer. Output protection was achieved using a P-channel, level shifted gate driver to rapidly shut off a high side FET. The measured turn off time was 18.4μs, within 13μs of the simulated value.

The smart power modules have been successfully installed and tested in the distributed power system of an operational unmanned ground vehicle. The initial sensitivity of the modules was too high. Unknown current spikes up to 26A magnitude and 60μs duration caused module current limits to trip on startup. A fault tolerance was added to the modules by means of an extended reset pulse which allowed these transients to subside. Since the addition of fault tolerance the smart power modules have successfully powered all system components without exception during extensive testing.

All the hardware is in place to achieve the desired module functions of current monitoring, adjustable current limiting and output protection. Future efforts can now focus on expanding the software to make full use of the hardware capabilities. Power health feedback and anomaly detection are two possible applications achievable through the introduction of increased sampling rates and data storage. These capabilities are not available free of charge, as the processor current draw reduces the overall module efficiency by 5-7% in the present configuration. Future efforts will be directed towards decreasing the computational power overhead through improved coding and possibly the implementation of new low power processing elements.

The smart power modules have achieved their primary objective in that they supply all mission power needs. Additional features of current monitoring, current limiting, and output protection have provided diagnostic tools and safeguarded sensors throughout the development of an unmanned ground vehicle. High efficiency of the conversion elements has enabled smart power modules to operate entirely under free convection. By leveraging advances in internally compensated conversion elements compact smart power modules present a new capability for distributed sensor power in autonomous ground vehicles.

References

[1] S. Luo and I. Batarseh, “A review of distributed power systems part I: DC distributed power system,” *Aerosp. Electron. Syst. Mag. IEEE*, vol. 20, no. 8, pp. 5–16, 2005.

[2] W. A. Tabiszt, M. M. Jovanovits, and F. C. Leet, “Present and future of distributed power systems,” in *Applied Power Electronics Conference and Exposition, 1992. APEC ’92. Conference Proceedings 1992., Seventh Annual*, 1992, pp. 11–18.

[3] B. Mammano, “Distributed Power Systems,” in *Unitrode Power Supply Design Seminar (SEM-900)*, 1993, pp. 1–11.

[4] C. C. Heath, “The market for distributed power systems,” *[Proceedings] APEC ’91 Sixth Annu. Appl. Power Electron. Conf. Exhib.*, pp. 225–229, 1991.

[5] W. T. Rutledge, “DISTRIBUTED POWER ‘TIME FOR A SECOND LOOK,’” in *International Telecommunications Energy Conf*, 1986, pp. 369–375.

[6] E. Lam, R. Bell, and D. Ashley, “Revolutionary Advances in Distributed Power Systems,” in *Applied Power Electronics Conference and Exposition, 2003. APEC ’03. Eighteenth Annual IEEE*, 2003, vol. 00, no. C, pp. 30–36.

[7] A. F. Roman, K. J. Fellhoelter, and B. Laboratories, “Circuit Considerations for Fast , Sensitive , Low-Voltage Loads in a Distributed Power System .,” *Appl. Power Electron. Conf. Expo. 1995. APEC ’95. Conf. Proc. 1995.*, vol. 1, pp. 34–42, 1995.

[8] M. T. Zhang, S. Member, M. M. Jovanovic, and F. C. Lee, “Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits,” *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 328–337, 1996.

[9] M. Morisio, M. Torchiano, D. Automatica, P. Torino, and C. Duca, “Definition and classification of COTS : a proposal,” in *International Conference on Composition-Based Software Systems (ICCBSS)*, 2002, pp. 1–10.

[10] C. Urmson, J. Anhalt, D. Bagnell, C. Baker, R. Bittner, M. N. Clark, J. Dolan, D. Duggins, T. Galatali, C. Geyer, M. Gittleman, S. Harbaugh, M. Hebert, T. M. Howard, S. Kolski, A. Kelly, M. Likhachev, M. Mcnaughton, N. Miller, K. Peterson, B. Pilnick, R. Rajkumar, P. Rybski, B. Salesky, Y. Seo, S. Singh, J. Snider, A. Stentz, W. R. Whittaker, Z. Wolkowicki, J. Ziglar, H. Bae, T. Brown, D. Demitrish, B. Litkouhi, J. Nickolaou, V. Sadekar, W. Zhang, J. Struble, and M. Taylor, “Autonomous driving in urban environments : Boss and the urban challenge,” *J. F. Robot.*, vol. 25, no. February, pp. 425–466, 2008.

[11] M. Montemerlo, J. Becker, S. Bhat, H. Dahlkamp, D. Dolgov, S. Ettinger, D. Haehnel, T. Hilden, G. Hoffmann, B. Huhnke, D. Johnston, S. Klumpp, D. Langer, A. Levandowski, J. Levinson, J. Marcil, D. Orenstein, J. Paefgen, I. Penny, A. Petrovskaya, M. Pflueger, G. Stanek, D. Stavens, A. Vogt, S. Thrun, S. Artificial, and S. Cs, “Junior : The Stanford Entry in the Urban Challenge,” *J. F. Robot.*, vol. 25, no. 9, pp. 569–597, 2008.

[12] A. Bacha, C. Bauman, R. Faruque, M. Fleming, C. Terwelp, C. Reinholtz, D. Beach, T. Alberi, D. Anderson, S. Cacciola, P. Currier, A. Dalton, J. Farmer, J. Hurdus, S. Kimmel, P. King, A. Taylor, D. Van Covern, and M. Webster, “Odin : Team VictorTango ’ s Entry in the DARPA Urban Challenge,” *J. F. Robot.*, vol. 25, no. 8, pp. 467–492, 2008.

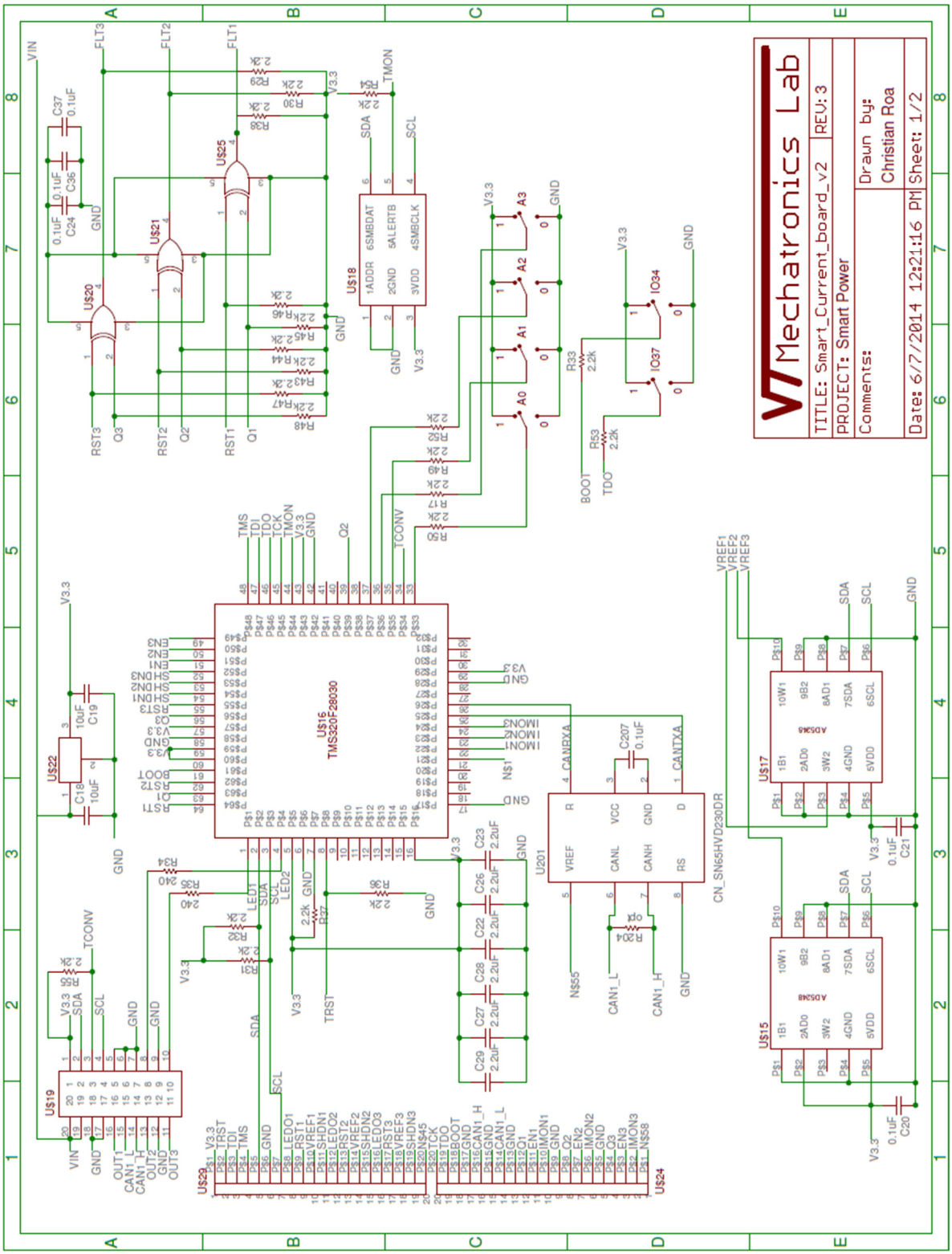
[13] The Car Connection, “2005 Ford Escape - Dimensions,” 2014. [Online]. Available: http://www.thecarconnection.com/specifications/ford_escape_2005_4dr-103-wb-2-3l-xls_dimensions.

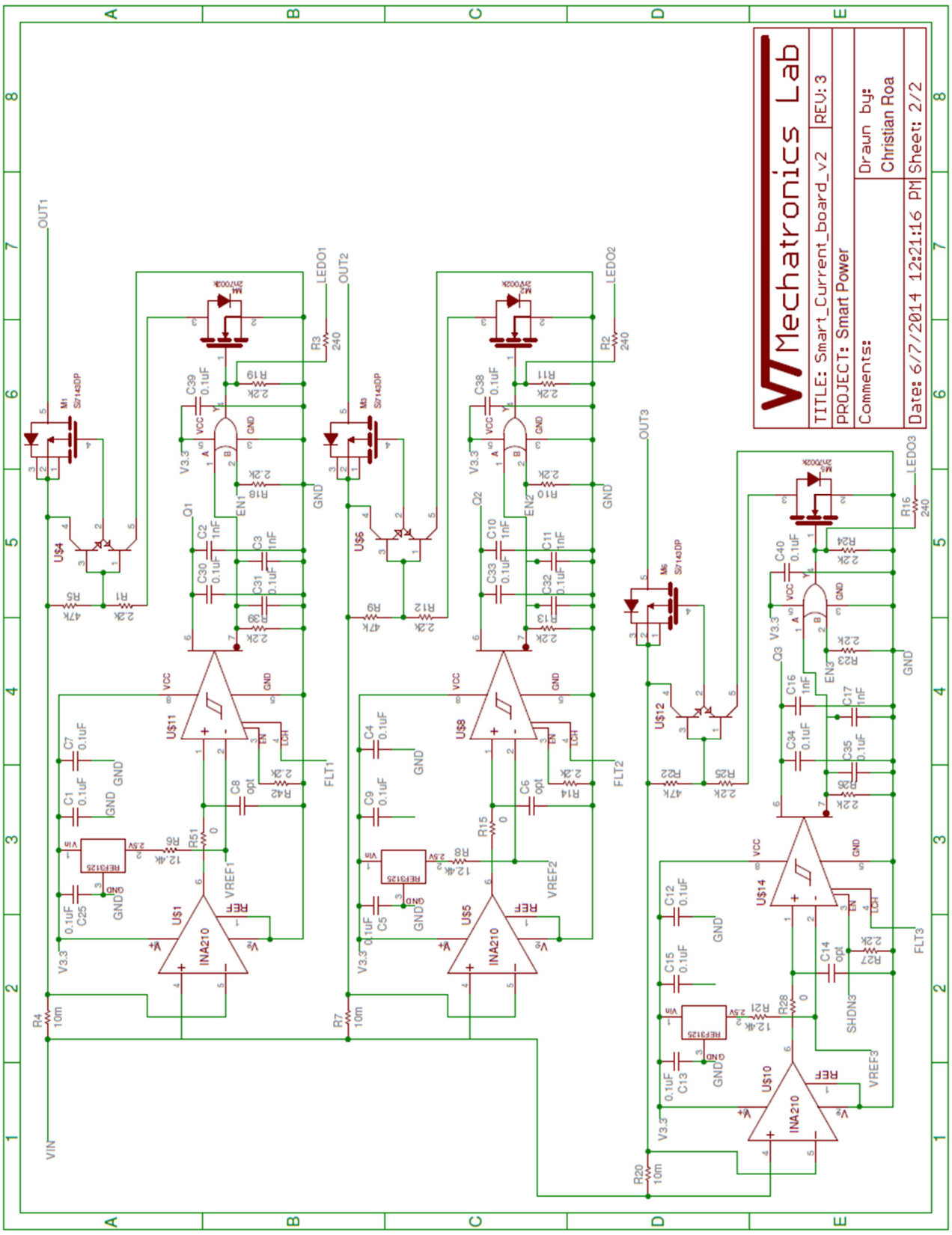
[14] Cars.com, “2007 Chevrolet Tahoe,” 2014. [Online]. Available: http://www.cars.com/chevrolet/tahoe/2007/specifications.
[15] S. Thrun, M. Montemerlo, H. Dahlkamp, D. Stavens, A. Aron, J. Diebel, P. Fong, J. Gale, M. Halpenny, G. Hoffmann, K. Lau, C. Oakley, M. Palatucci, V. Pratt, P. Stang, S. Strohband, C. Dupont, L. Jendrossek, C. Koelen, C. Markey, C. Rummel, J. Van Niekerk, E. Jensen, P. Alessandrini, G. Bradski, B. Davies, S. Ettinger, A. Kaehler, A. Nefian, and P. Mahoney, “Stanley : The Robot that Won the DARPA Grand Challenge,” vol. 23, no. April, pp. 661–692, 2006.
[16] US Navy, “US Navy Marines Test Autonomous Unmanned Ground Vehicles,” 2010. [Online]. Available: http://www.defencetalk.com/us-navy-marines-test-autonomous-unmanned-ground-vehicles-27996/.
[17] TORC Robotics, “Ground Unmanned Support Surrogate, Optionally Unmanned & Autonomous Vehicles, Lighten the Load for Dismounted Warfighters,” 2010. [Online]. Available: http://www.torcrobotics.com/case-studies/ground-unmanned-support-surrogate.
[18] Robot Living, “Automated Golf Carts Head To War,” 2010. [Online]. Available: http://www.robotliving.com/military/automated-golf-carts-head-to-war/.
[19] R. W. Erickson and D. Maksimović, *Fundamentals of power electronics*. Norwell, Mass.: Kluwer Academic, 2001.
[20] S. Ang and A. Oliva, *Power-Switching Converters*. Boca Raton: CRC press, 2005.
[21] B. L. Balogh, “Design And Application Guide For High Speed MOSFET Gate Drive Circuits.” Texas Instruments, Dallas, 2001.
[22] D. Meeks, “Loop Stability Analysis of Voltage Mode Buck Regulator With Different Output Capacitor Types – Continuous and Discontinuous Modes,” no. April1. Texas Instruments, Dallas, 2008.
[23] M. Brown, *Practical switching power supply design*. San Diego: Academic Press, 1990.
[24] M. Day, “Optimizing Low-Power DC / DC Designs – External versus Internal Compensation,” *Portable power design seminar*. Texas Instruments, Dallas, 2004.
[25] Texas Instruments, “3A , 28V INPUT , STEP DOWN SWIFT ™ DC / DC CONVERTER WITH ECO-MODE ™ TPS54331,” no. July 2008. Texas Instruments, Dallas, 2012.
[26] Vicor, “PI33XX-X0 8V to 36Vin Cool-Power ZVS Buck Regulator,” 2013. [Online]. Available: http://cdn.vicorpower.com/documents/datasheets/Picor/ds_pi33xx.pdf.
[27] B. Shaffer, “Internal Compensation – Boon or Bane ?,” *Power Supply Design Sem. (SEM 1300)*. Texas Instruments, Dallas, 2000.
[28] Texas Instruments, “TPS54331EVM-232 3-A , SWIFT ™ Regulator Evaluation,” no. July. Texas Instruments, Dallas, p. 11, 2008.
[29] LinearTechnology, “LTM8027 60V, 4A DC/DC µModule Regulator.” Linear Technology, Milpitas, 2009.
[30] Semtech, “Surging Ideas TVS Diode Application Note SI96-01.” Samtech, www.semetech.com, 2000.
[31] Semtech, “Surging Ideas TVS Diode Application Note SI96-02.” Semtech, www.semetech.com, 2000.
[32] R. Palmer, “DC Parameters : Input Offset Voltage (V IO),” no. March. Texas Instruments, Dallas, 2001.
[33] Texas Instruments, “Current Shunt Monitors,” 2014. [Online]. Available: http://www.ti.com/lit/ml/slyb194a/slyb194a.pdf.

[34] Texas Instruments, “INA21x Voltage Output , Low- or High-Side Measurement , Bidirectional , Zero-Drift Series , Current-Shunt Monitors.” Texas Instruments, Dallas, 2014.

Appendix A: smart power module schematics and layout

A1 smart current board schematic




Mechatronics Lab
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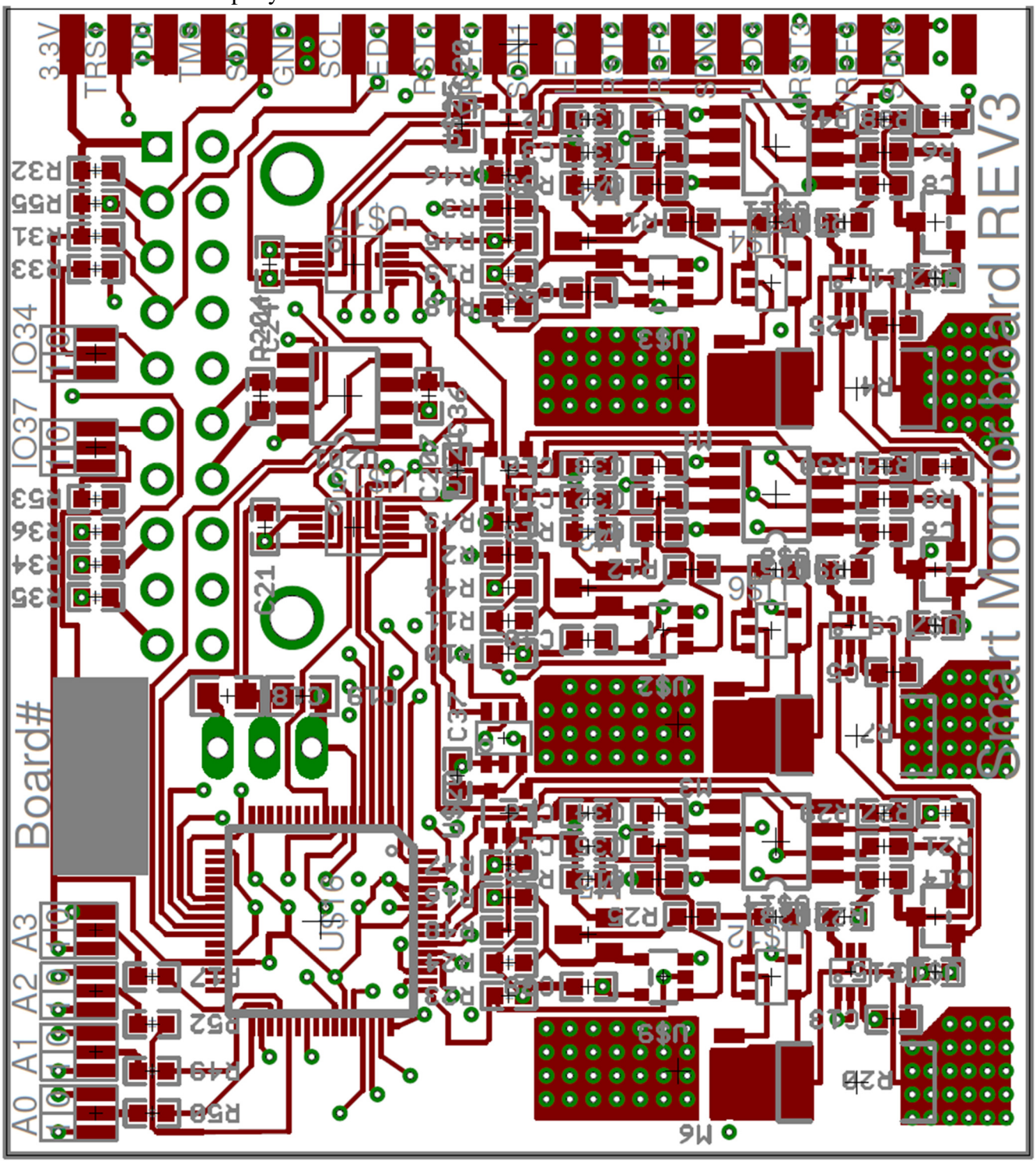
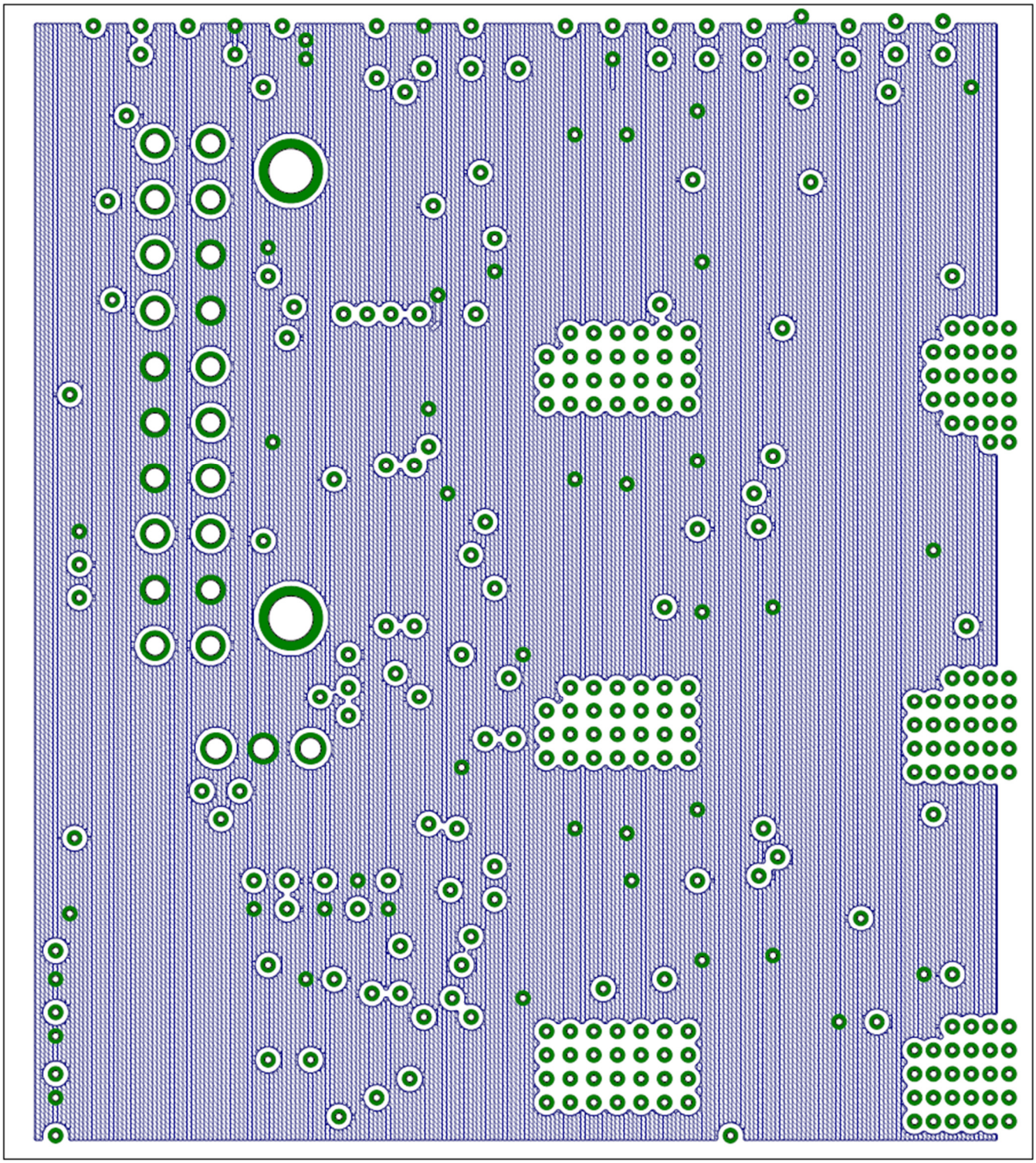
REV: 3
PROJECT: Smart Power
Comments:
Drawn by: Christian Roa
Date: 6/7/2014 12:21:16 PM
Sheet: 2/2
VIN
OUT1
OUT2
OUT3
LEDO1
LEDO2
LEDO3
FLT1
FLT2
FLT3
V3.3
GND
VREF1
VREF2
VREF3
SHDN3
INA210
REF3125
SI7002A
SI4435DDY

A2 Smart current board layout:

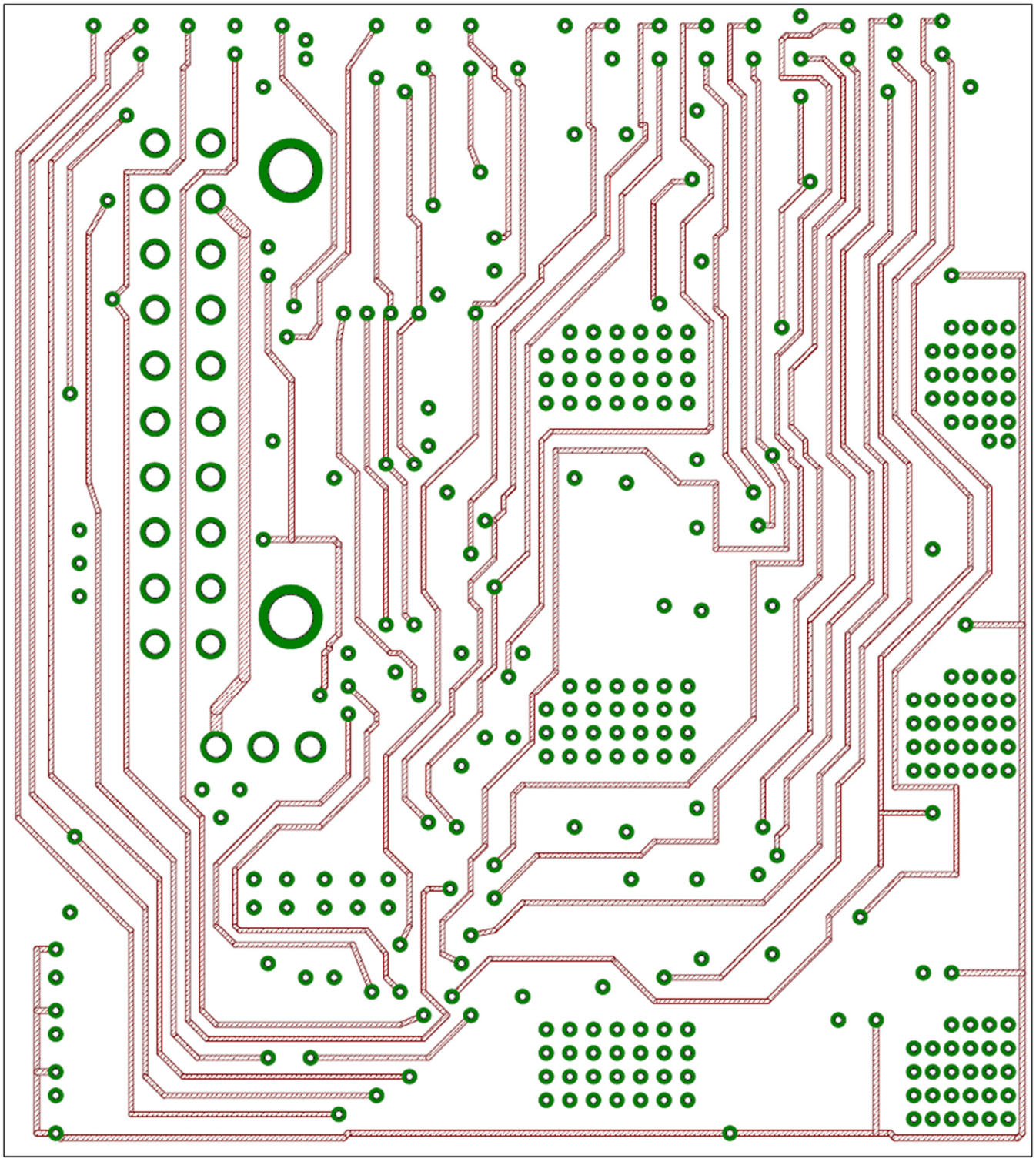
Smart current board: top layer



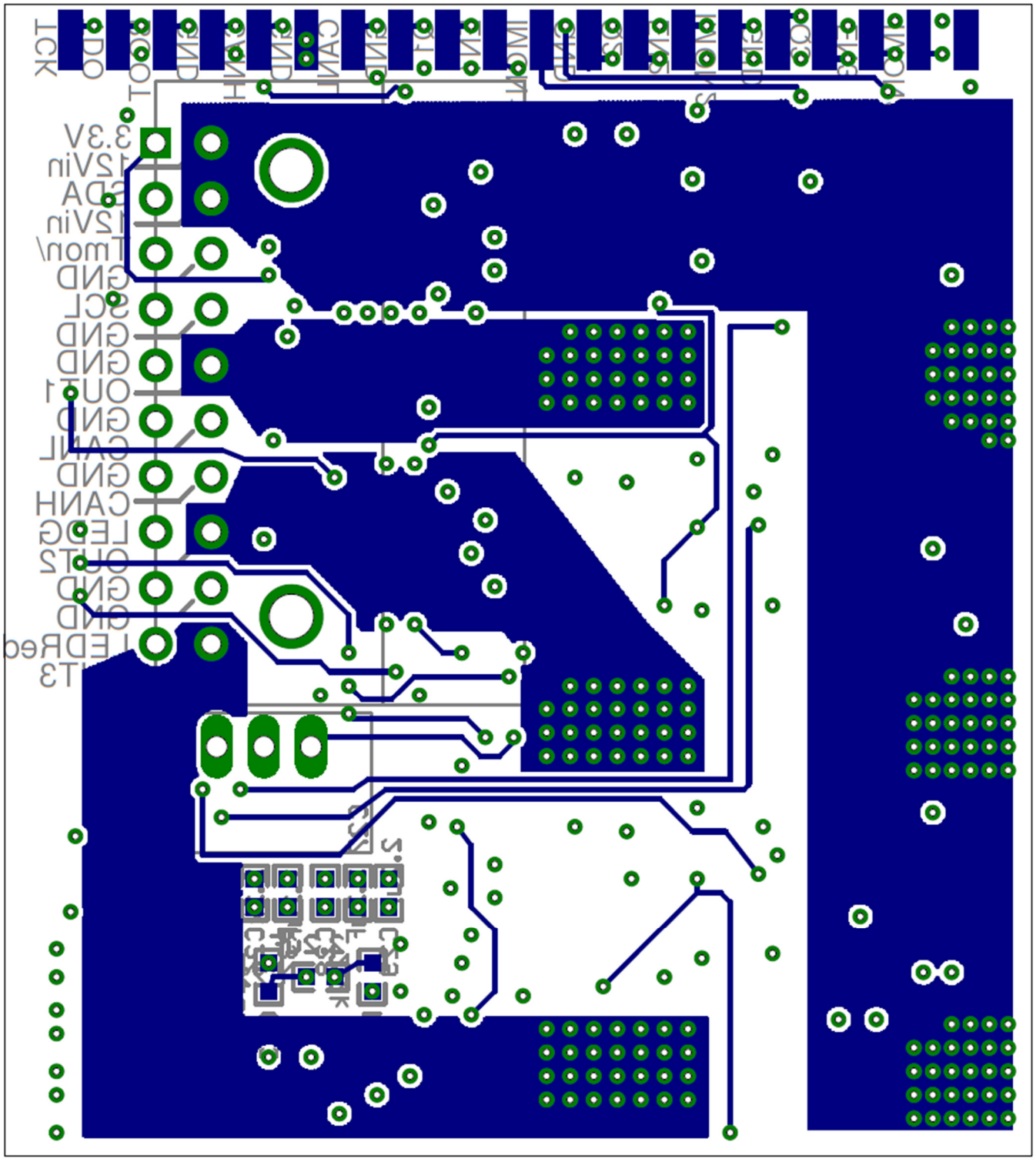
Smart current board: second layer



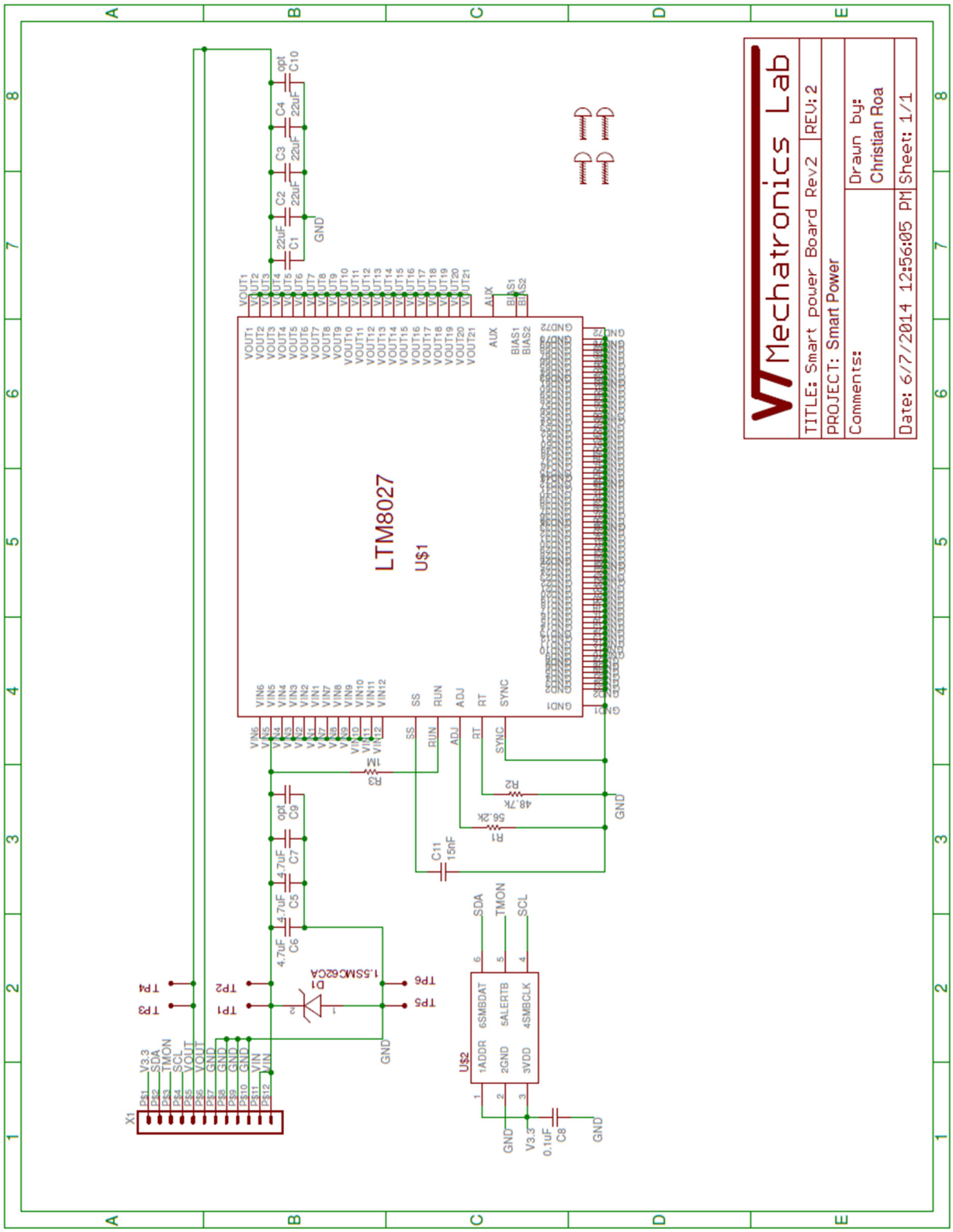
Smart current board: third layer



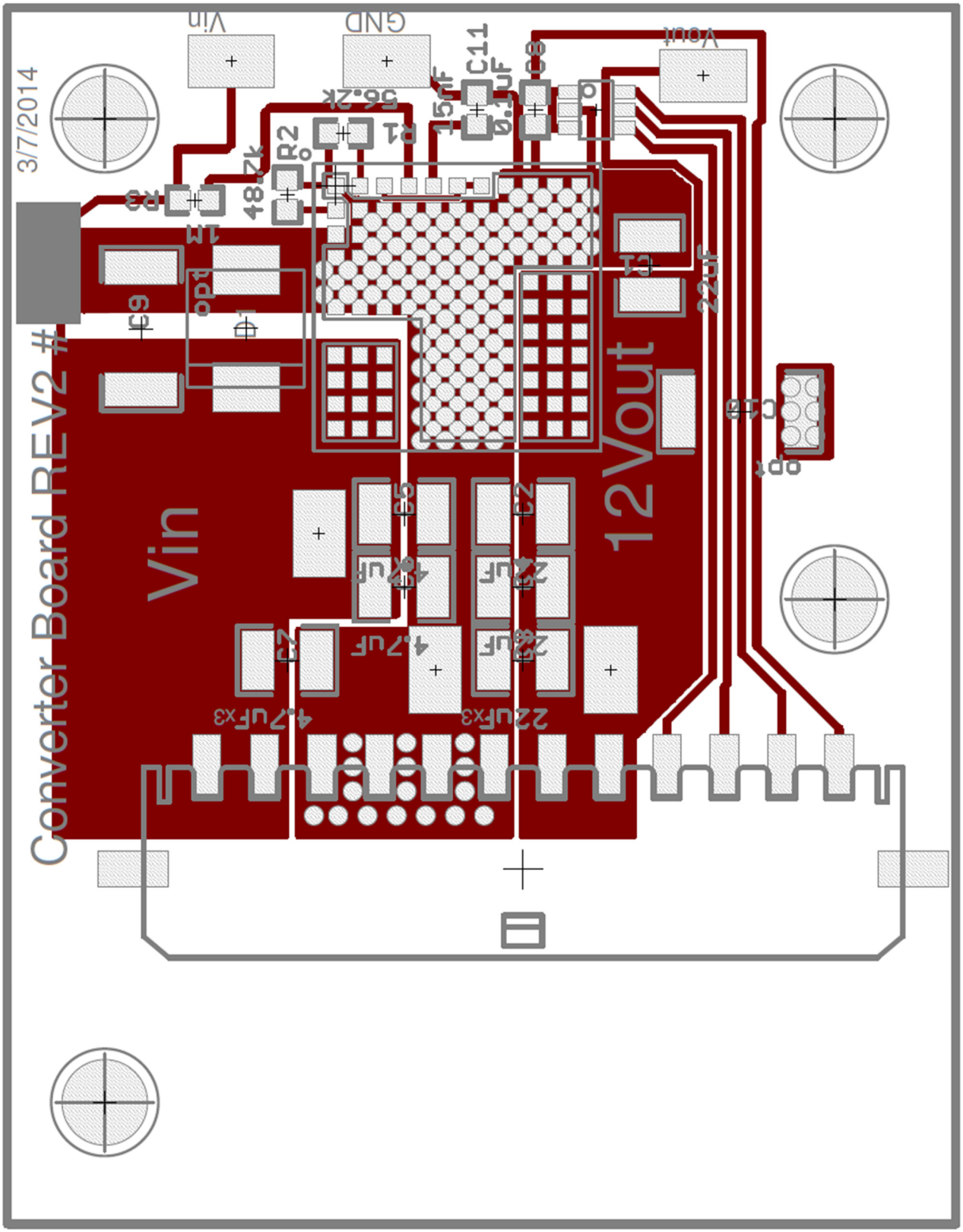
Smart current board: bottom layer



A3 Smart power board schematic



Smart power board: top layer



Smart power board: bottom layer