

**Design, Analysis, and Experimental Verification of a Mechanically Compliant
Interface for Fabricating Reliable, Double-Side Cooled, High-Temperature,
Sintered Silver Interconnected Power Modules**

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Dissertation submitted to the faculty of
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Materials Science and Engineering

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August 13th, 2014
Blacksburg, Virginia

Keywords: Three-dimensional packaging, double-side cooled, planar, power module packaging, thermal resistance, thermal impedance, sintered silver, quarter-bridge, half-bridge.

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Abstract

This research developed a double-side power electronics packaging scheme for high temperature applications exemplified by 1200 V, 150 A silicon devices. The power modules, based on both quarter and half-bridge topologies, were assembled using sintered silver device attachment rather than conventional solder alloys. Thermomechanical stresses in the double-side architecture were mitigated with a compliant layer fabricated from elliptical silver tubes.

This research presents an introduction to conventional packaging techniques and their weaknesses. These shortcomings provide the basis for a module design which improves upon module thermal management while also addressing electrical and reliability requirements. The optimum package design enhances heat dissipation with the addition of a substrate bonded to the top electrical pads of the semiconductor devices. The use of sintered silver also increases the useful application temperature by avoiding the creep failure mechanisms of solder alloys.

The modules were characterized extensively to quantify thermal and electrical performance. In the case of thermal characterization, the double-side architecture required multiple testing configurations to fully understand the parallel heat flow paths. These results were compared to models constructed using finite element analysis (FEA). The FEA models were also utilized for

measurement of strains in multiple package designs to better determine the effects of increased compliance on the relative package cycling lifetime. These lifetimes were then assessed, in part, using experimental passive and cycling tests on functional double-side packages.

The resulting power modules exhibited significant decreases in thermal resistance when they are cooled, as designed, from both sides of the module. Even single sided cooling options reveal significant advantages and transient thermal impedance was found to be significantly lower. Power module models revealed the compliant layer was successful in reducing the device shear stresses which was experimentally validated through the use of DC power stage testing. It was found, through double pulse testing and electrical modeling, that parasitic inductances were reduced by utilizing planar bonding and planar symmetrical traces. Finally, modeling of the double-side package with added tube compliance revealed a decrease in plastic and shear strains when compared to other single and double-side package designs. This reduction directly translates to increased cycling lifetime using well known strain based fatigue models.

Acknowledgements

I would like to thank my family and friends who helped me get to this point. I especially want to thank my wife Lori and my son Christian for their continued support and guidance. I hope this endeavor has served to illustrate to my son the importance of education and most importantly, how attainable it can be given sufficient determination.

None of this would have been possible without the faculty, staff and alumni of the Materials Science and Engineering Department. I am grateful to have been a member of the MSE Department and have benefitted greatly from our relationship. Through this tie, I have met and befriended countless students, faculty and staff which have contributed and continue to contribute to my personal and professional success. I could not be more blessed.

Funding for this project was provided by the High Density Integration Mini-Consortium through the Center for Power Electronics Systems at Virginia Tech. The Mini-Consortium member partner for this work was Mitsubishi Electric Corporation.

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Table of Contents

Abstract	ii
Acknowledgements	iv
Table of Contents	v
List of Figures	viii
List of Tables	xviii
Chapter 1. Introduction	1
1.1. Significance	1
1.2. Overview of Power Electronic Packaging Techniques	4
1.2.1. Wirebonding	4
1.2.2. Deposited Metallization	6
1.2.3. Controlled Collapse Chip Connection	8
1.2.4. Conductive Epoxy.....	9
1.2.5. Solders and alloys	11
1.2.6. Low Temperature Joining Technologies.....	12
1.2.7. Summary of Selected Power Packaging Technologies	20
1.2.8. Shortcomings of Current Solder Technologies	22
1.2.9. Shortcomings of wirebond technology	23
1.3. Introduction to Three-dimensional Circuit Architecture	26
1.4. Motivation for Double-Side Packages using Sintered Silver LTJT	28
1.5. Objectives and Significance of Study.....	29
1.6. Organization of Dissertation	30
1.7. Publications and Patents	31
Chapter 2. Design of a Double-Side Cooled Power Module	32
2.1. Prior Arts in Double-Side Integration	32
2.2. Investigation of Double-Side Structure for Multichip Power Modules	37
2.2.1. Thermal Contributions	37
2.2.2. Parasitic Contributions.....	40
2.2.3. Double-Side Stress Evaluation.....	42
2.2.4. Stress Reduction in Double-Side Packaging.....	47
2.3. Modeling and Design of Stress Reducing Interface	49
2.3.1. Thermal Modeling.....	50

2.3.2.	Parametric Study of Thermal Conductivity	62
2.3.3.	Thermomechanical.....	64
2.3.4.	Parametric Study of Thermomechanical Design.....	70
2.3.5.	Alternative Materials for Thermomechanical Design.....	79
2.3.6.	Parasitic Investigation	81
2.3.7.	Parasitic Model Results.....	82
Chapter 3.	Process Development and Fabrication.....	85
3.1.	Module Configuration	85
3.1.1.	Half-Bridge Summary	85
3.1.2.	Quarter-Bridge Summary.....	87
3.2.	Chip Level Metallization.....	89
3.3.	Compliant Corrugated Interface Construction	93
3.4.	Double-Side Package Workflow	98
3.5.	Additional Hardware for Integration	103
3.6.	Encapsulation	105
3.6.1.	Selection.....	105
3.6.2.	Encapsulation Processing and Integration	110
Chapter 4.	Module Characterization and Testing	112
4.1.	V-I Testing	112
4.1.1.	Experimental Setup.....	112
4.1.2.	Results.....	114
4.2.	DC Power Stage Testing	115
4.2.1.	Experimental Setup.....	116
4.2.2.	Results.....	118
4.3.	Double Pulse Testing.....	121
4.3.1.	Experimental Setup.....	122
4.3.2.	Experimental Results	126
4.4.	Three-Phase Inverter Integration.....	130
4.4.1.	Experimental Setup.....	130
4.4.2.	Results.....	132
4.5.	Thermal Spectrometry Analysis	133
4.5.1.	Experimental Setup.....	139
4.5.2.	Results.....	141

Chapter 5. Reliability Evaluation: Testing and Modeling	149
5.1. Finite Element Model Parameters	156
5.2. Active Cycling (Accelerated Reliability) Model.....	158
5.2.1. Model Results	160
5.2.2. Active Cycling Parametric Model Results	172
5.3. Passive Cycling (Thermal) Model.....	173
5.3.1. Model Results	175
5.4. Measurement of Device Temperature Sensitive Parameters	185
5.5. Active (Power) Cycling Experimental	188
5.5.1. Experimental Procedure	190
5.5.2. Nondestructive Analysis and End of Life Criteria	192
5.5.3. Summary	203
5.6. Passive (Thermal) Cycling Experimental.....	203
5.6.1. Experimental Procedure	204
5.6.2. Nondestructive Analysis	207
5.6.3. Destructive Analysis	213
5.6.4. Summary	215
Chapter 6. Further Developments in Double-Side Cooling	216
6.1. Integration of New Materials.....	217
6.2. Manufacturing Improvements	221
6.3. Future Designs.....	222
Chapter 7. Summary and Conclusions	223
7.1. Design and Development of Double-side Planar Power Modules	224
7.2. Electrical Evaluation of Prototype Modules.....	225
7.3. Experimental and Numerical Analysis of the Structure	225
Original Contributions	226
References.....	228
Appendix A.....	234

List of Figures

- Figure 1: Double-side device connection using sintered silver LTJT. The top electrical connection is made from silver ribbon attached with sintered silver rather than traditional wirebonding techniques.([38] M. Knoerr, S. Kraft, and A. Schletz, "Reliability assessment of sintered nano-silver die attachment for power semiconductors," in Electronics Packaging Technology Conference (EPTC), 2010 12th, 2010, pp. 56-61.) Used under fair use, 2014..... 20
- Figure 2: Examples of common wirebond failure mechanisms. a) metallurgical damage b) heel cracking c) wirebond fracture and d) wirebond liftoff.([2] V. Smet, F. Forest, J. J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani, "Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 4931-4941, 2011) Used under fair use, 2014..... 24
- Figure 3: Example of attempted 3D packaging using wirebonding for multilevel device connection.([45] J. Sylvester. (2012, 10/22/13), Electronic Components and Technology Conference (ECTC)). Used under fair use, 2014..... 26
- Figure 4: Schematic of one of the earliest proposed 3D circuit architectures. This structure is called the Metal Posts Interconnected Parallel Plate Structure (MPIPPS) and is fabricated using conventional solders. ((www.cpes.vt.edu) Accessed 5/19/14) Used under fair use, 2014. 27
- Figure 5: One example of similar double-side cooling attempt using a single switching quarter-bridge module fabricated with (a) solder copper tubes between the devices and top heat sink. The final package with top heat sink (b). ([49] J. F. Li, A. Castellazzi, A. Solomon, and C. M. Johnson, "Reliable Integration of Double-Side Cooled Stacked Power Switches based on 70 micrometer Thin IGBTs and Diodes," in Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on, 2012, pp. 1-6) Used under fair use, 2014..... 33
- Figure 6: Side view (top) and top view (bottom) of prototype three-dimensional module showing one switching unit (IGBT and diode) attached directly above another switching unit using arrays of soldered copper spheres called power bumps. ([55] M. Mermet-Guyennet, "New structure of power integrated module," in Integrated Power Systems (CIPS), 2006 4th International Conference on, 2006, pp. 1-6.) Used under fair use, 2014. 34
- Figure 7: Patent application illustration from patent application number 13/547937 submitted by Liang et al on January 24, 2013.([56] Z. X. Liang, Martino, L., Ning, P., Wang, F., "POWER MODULE PACKAGING WITH DOUBLE SIDED PLANAR INTERCONNECTION AND HEAT EXCHANGERS," 2013) Used under fair use, 2014..... 35
- Figure 8: Image of prototype double-side cooled power module from patent application 13/547937 submitted by ORNL researchers.([56] Z. X. Liang, Martino, L., Ning, P., Wang, F., "POWER MODULE PACKAGING WITH DOUBLE SIDED PLANAR INTERCONNECTION AND HEAT EXCHANGERS," 2013) Used under fair use, 2014. 36
- Figure 9: Double-side single diode package using only sintered silver for attachment of the top and bottom substrates. Work and photograph courtesy of Masson et al.([57] A. Masson, S.

Azzopardi, F. Le Henaff, J. Y. Deletage, E. Woirgard, S. Bontemps, and J. Joguet, "Processing and Characterization of a 100% Low-Temperature Ag-Sintered Three-Dimensional Structure," in Power Electronics and Applications (EPE), 2013 15th European Conference on, 2013, pp. 1-9.) Used under fair use, 2014.	37
Figure 10: Thermal FEA of proposed power module footprint and device placement revealing negligible thermal superposition effects during application.	40
Figure 11: Illustration of proposed electrical layout for minimizing the parasitic contributions from induction, resistance and capacitance.	42
Figure 12: Failure of double-side device by excess shear stress during fabrication temperature changes. [1] (J. Li, G. Q. Lu, and K. Ngo, "Study of Robustness for Double-Sided Module with Rigid Substrates on Both Sides," presented at the Center for Power Electronics Annual Conference, Virginia Tech, Blacksburg VA., 2012) Used under fair use 2014.	46
Figure 13: Illustration of constructed paths for plotting the heat flow through the wall of the tube (top) and the heat flow through the opening in the tube (bottom).	52
Figure 14: Colored thermal distribution plot output from FEA thermal simulation to determine the steady state thermal distribution using 100W applied to the device.	53
Figure 15: Comparison of steady state package temperature profile for each configuration. The heat path begins on the left at the bottom of the substrate (z-position = 0). The device junction temperatures are indicated with the black rectangle.	54
Figure 16: Modeled single dimension thermal profiles for each of three unencapsulated module cooling configurations; top-cooled, bottom-cooled and top plus bottom cooled.	56
Figure 17: Modeled three-dimensional thermal distributions for each of three cooling configurations; a) bottom-cooled, b) top-cooled and c) top plus bottom cooled.	57
Figure 18: Modeled single dimension thermal profiles for each of three encapsulated module cooling configurations; top-cooled, bottom-cooled and top plus bottom cooled.	59
Figure 19: Modeled three-dimensional thermal distributions for each of three encapsulated cooling configurations; a) bottom-cooled, b) top-cooled and c) top plus bottom cooled.	60
Figure 20: Illustration of using the junction to bottom case and junction to top case thermal resistance values to calculate the thermal resistance of the instance when both the top and bottom substrates are force cooled.	62
Figure 21: Change in thermal conductivity of tubing interface as a function of changing wall thickness for a 1 mm tubing height where 0.5 mm wall thickness is a solid round of bulk silver.	64
Figure 22: Colored plot revealing equivalent von Mises stress distribution when the entire unencapsulated module cools from the fabrication temperature.	67

Figure 23: Stress distribution plot showing the calculated equivalent Von Mises stress distribution in an unencapsulated module reheated after fabrication.	68
Figure 24: Stress distribution plot showing the calculated equivalent von Mises stress distribution in an encapsulated module reheated after fabrication.	69
Figure 25: Stress distribution plot showing the calculated equivalent von Mises stress distribution in an unencapsulated module reheated after fabrication.	70
Figure 26: An illustration of the tube height, width and wall thickness and how it changes the stress state on the surface of the device.	72
Figure 27: Equivalent von Mises stress on the device in the area between tubes (red) and directly underneath the tube (blue).	74
Figure 28: Equivalent von Mises stress distribution (between the attached tubes and directly underneath tubes) for various tubing heights.	76
Figure 29: The deformation behavior of tube structures in direct contact versus those tube with spacing to avoid contact.	78
Figure 30: Three-dimensional structures used for modeling the electrical parasitics in the double-side package connection with labels showing assigned source and sink locations.	82
Figure 31: Schematic of quarter bridge module with simulated inductance values included.	84
Figure 32: Representative commercially available half-bridge power module. (http://www.micros.com http://www.micros.com/ accessed 5/17/14) Used under fair use, 2014.	85
Figure 33: Electrical schematic illustrating the current flow in the double-side half-bridge module.	86
Figure 34: Proposed design for fabrication based on design constraints.	87
Figure 35: Electrical schematic illustrating the current flow in the double-side quarter-bridge module.	87
Figure 36: Quarter-bridge module design.	88
Figure 37: Illustration of coupling quarter-bridge modules for half-bridge configurations. The symmetry also places the active IGBT far from the opposing IGBT which should enhance the packages thermal properties.	89
Figure 38: IGBT device parameters and stainless steel mask for applying UBM using PVD.	91
Figure 39: X-ray photoelectron spectrometry (XPS) of the as-received die (top) and the die cleaned using argon sputtering (bottom).	92

Figure 40: Non-contact profilometer results of as-received (left) and metallized (right) devices.	93
Figure 41: Patent application diagrams for proposed compliant tube interface indicating the design variables for accommodating multiple interconnection schemes.	94
Figure 42: Custom fabricated tube cutting fixture.	94
Figure 43: Custom fabricated tubing press for adjusting the tubing height to accommodate different device thicknesses.	95
Figure 44: Tubes constructed for attachment to the IGBT (left) and the diode (right).	96
Figure 45: Workflow for die application on the bottom substrate.	99
Figure 46: Hot press and temperature profile used for pressure sintering.	100
Figure 47: Workflow for tube application on the top substrate.	100
Figure 48: Wirebonding of the IGBT gate and emitter to the patterned digits on the bottom substrate.	101
Figure 49: The leveling block pressing arrangement used for making the final attach of the double-side module.	102
Figure 50: Images of sintered quarter-bridge modules (left) and a half-bridge module (right).	102
Figure 51: Custom fabricated alignment fixture for reflowing input and output power tabs as well as gate and emitter headers.	103
Figure 52: Modules (Half-Bridge, left and Quarter-Bridge, right) with reflowed connections before encapsulation.	104
Figure 53: Close up stitched image showing the complete quarter-bridge geometry.	104
Figure 54: Pushrod dilatometer for measuring coefficients of thermal expansion to high temperatures.	106
Figure 55: Epoxy bars cast in 1 inch sample sizes for Orton pushrod dilatometer testing.	107
Figure 56: A comparison plot summarizing CTE measurements for each candidate epoxy formulation.	108
Figure 57: The glass transition (shown as large slope change) of each candidate epoxy.	109
Figure 58: Workflow of encapsulating both the quarter-bridge and half-bridge modules using XNR two part epoxy.	111
Figure 59: Flexible silicon mold fabricated for curing the encapsulated module.	111

Figure 60: Tektronix 371A High Power Curve Tracer with a probe station for measuring a range of packaged and unpackaged devices.	113
Figure 61: V-I measurements of the IGBT before and after packaging.	114
Figure 62: V-I measurements of encapsulated and unencapsulated diode packages overlaid with datasheet values for comparison.	115
Figure 63: Schematic of the DC power stage test showing data collection points.	117
Figure 64: Custom fabricated DC power stage test system for testing both quarter and half-bridge modules.	118
Figure 65: V-I output of each device in a half-bridge module using DC power stage test system for inducing device self-heating.....	119
Figure 66: The recorded IGBT junction temperature under a constant 90A DC current.	120
Figure 67: (left) An IGBT held at 200°C for 90 minutes using applied DC current; (right) The temperature differential in the package during the constant temperature IGBT test.	121
Figure 68: Double pulse test system electrical schematic.	123
Figure 69: Two quarter-bridge modules arranged in half-bridge configuration required for dynamic switching characterization.....	123
Figure 70: Images of the complete double pulse test system and components.	124
Figure 71: Guidelines on industry standard boundaries for calculating turn off energy loss (E_{off}), turn on energy loss (E_{on}), rise time (t_r), fall time (t_f), turn on delay time ($t_{d on}$), and turn off delay time ($t_{d off}$). ([78] "IGBT Applications Handbook," vol. HBD871/D, O. Semiconductor, Ed., 2 ed. www.on-semi.com: On Semiconductor, 2012.) Used under fair use, 2014.....	126
Figure 72: The measured turn on (left) and turn off (right) switching characteristics of a commercially available Powerex module using 600V and 150A.	127
Figure 73: Full double pulse output waveform for one quarter-bridge module.	128
Figure 74: Turn-off switching results for quarter-bridge module in custom test system.	129
Figure 75: Turn-on switching results for quarter-bridge module in custom test system.	129
Figure 76: Laboratory constructed inverter package with (left) and without (right) the driver board connected.	131
Figure 77: Diagram of the necessary inverter testing components.	132
Figure 78: Three phase inverter output using a laboratory constructed inverter populated with three half-bridge modules.	133

Figure 79: Example of simple stacked structure common in semiconductor device packages. . 134

Figure 80: Experimental test setup suggested by JEDEC Standard JESD51-14.([88] JEDEC, "JESD51-14 Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path," vol. JESD51-14, ed. <http://www.jedec.org/standards-documents/results/51-14>: Joint Electron Device Engineering Council, November 2012, p. 46) Used under fair use, 2014..... 136

Figure 81: Transformation of linear temperature relationship to log scale which reveals small transitions for each material in stacked structure..... 137

Figure 82: Example measurement provided in JEDEC Standard JESD51-14 for illustrating the thermal resistance calculation of a TO package using dry and wet TIM materials. ([88] JEDEC, "JESD51-14 Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path," vol. JESD51-14, ed. <http://www.jedec.org/standards-documents/results/51-14>: Joint Electron Device Engineering Council, November 2012, p. 46) Used under fair use, 2014..... 138

Figure 83: Required measurement configurations for accurate assessment of a double-side cooled package. 140

Figure 84: Test setup used by Mentor Graphics for testing the double-side cooled power module referring to JEDEC standard JESD51-14. 141

Figure 85: Repeatability testing results of the quarter-bridge module using the dual interface test method..... 142

Figure 86: Transient cooling curves and the power settings used for heating of each of the three possible module cooling configurations. 143

Figure 87: Characteristic thermal impedance curves for the wet and dry interface material. The point at which the two curves diverge is used to determine the case of the module. 144

Figure 88: Experimentally measured structure functions for each of the three possible cooling scenarios for the double-side module. 145

Figure 89: De-convoluted cooling curves showing the experimental structure functions for each cooling scenario; a) bottom cooled b) top cooled and c) both surfaces cooled. A schematic illustrating the cause of variations in structure functions is shown in d)..... 146

Figure 90: Two dimensional graphic representing the equivalent von Mises maximum distortion energy. The Rankine and Tresca boundaries are included for comparison. 151

Figure 91: FEA cycling model reduction using model symmetry..... 156

Figure 92: The simplified cycling model with FEA mesh for the double-side package with compliant tube interface above the die. 157

Figure 93: Active cycling profile including fabrication thermal step used for FEA model. Entire package was exposed to thermal loads for fabrication ($t < 30s$), and device was used as heat source for active cycle ($t > 30s$).	160
Figure 94: Comparison of device shear stress as a function of cycles in active cycling regime. 162	
Figure 95: Comparison of package von Mises stress for each package configuration as a function of active cycles.....	163
Figure 96: Von Mises stress maxima locations for different package configurations.....	164
Figure 97: Accumulation of plastic strain in the sintered silver interface between the die and substrate for various package configurations as a function of active cycles.	165
Figure 98: Third cycle changes in plastic strain at various points in the interface directly below the die for each package configuration.	167
Figure 99: The shear strain magnitudes in the sintered silver interface between die and substrate for each package configuration as a function of active cycles.....	168
Figure 100: Shear strain magnitudes above and below the die in the package with compliant tube interface.....	170
Figure 101: Colored plot illustrating shear strain distribution in the sintered silver interface between the die and the tube in the compliant tube package.....	171
Figure 102: Von Mises stress distribution in the compliant silver tube interface.	172
Figure 103: Fourth cycle von Mises stress measurements for module components for modules constructed of different tubing wall thickness (1 mm high interface).	173
Figure 104: Passive cycling profile including fabrication thermal step used for FEA model. Entire package was exposed to thermal loads for both fabrication and cycling.	174
Figure 105: Device shear stress for each package configuration as a function of passive cycles.	176
Figure 106: Comparison of package von Mises stresses for each configuration as a function of passive cycles.....	177
Figure 107: Location of von Mises maxima in passively cycled package configurations.	178
Figure 108: Plastic strain accumulation in various package configurations as a function of passive cycles.....	178
Figure 109: Third cycle changes in plastic strain at various points in the interface directly below the die for each package configuration.	180

Figure 110: The shear strain magnitudes in the sintered silver interface between die and substrate for each package configuration as a function of passive cycles.	181
Figure 111: Colored plot illustrating shear strain distribution in the sintered silver interface between the die and the tube in the compliant tube package.	183
Figure 112: Von Mises stress distribution in the compliant silver tube interface.	184
Figure 113: Prototype module constructed for measuring accurate junction temperatures during temperature sensitive parameter experiments.	186
Figure 114: A plot of the changing gate emitter voltage (V_{ge}) as temperature is cooled from 175°C.	187
Figure 115: Linear fit of operational portion of the TSP curve using an ABB IGBT.	188
Figure 116: Representative cycle profile for power cycle testing.	189
Figure 117: Schematic of the power cycling experiment.	191
Figure 118: Labview screenshot of the symmetric active cycling profile used for the active cycling experiment.	192
Figure 119: A schematic representation of the experimental thermal impedance test bed. This is the same test setup used by others.([103] C. Gang, H. Dan, M. Yun-Hui, C. Xiao, W. Tao, C. Xu, and L. Guo-Quan, "Transient Thermal Performance of IGBT Power Modules Attached by Low-Temperature Sintered Nanosilver," Device and Materials Reliability, IEEE Transactions on, vol. 12, pp. 124-132, 2012) Used under fair use, 2014.	195
Figure 120: FEA model of transient heat flow with a 10W, 40ms pulse applied to the device. The model illustrates the depth of heat flux for thermal impedance analysis.	196
Figure 121: Comparison of heat distribution for 40ms (top) and 100ms (bottom) heating pulses in encapsulated (right) and unencapsulated (left) device packages.	197
Figure 122: The measured change in thermal impedance with 100ms pulsed power as a function of active heating cycles. The heating cycle was a 5 minute symmetric cycle with a temperature range from 40°C to 160°C.	198
Figure 123: A large area scan of a fabricated half-bridge module using X-ray Computed Tomography (CT).	200
Figure 124: A large area scan of a fabricated quarter-bridge module using X-ray Computed Tomography (CT).	201
Figure 125: A large area scan of a fabricated quarter-bridge module showing uniform bonding of tubes (enlarge area) and voids in SAC solder using X-ray Computed Tomography (CT).	201

Figure 126: Tube substrate interface (a) and tube die interface (b) X-ray images of a quarter-bridge module that has been actively cycled for 10,000 cycles.....	202
Figure 127: Representative temperature profile for thermal cycle test conditions.	204
Figure 128: Image of passive cycling experimental setup using a constant ambient temperature in a chamber and a hotplate for applying heating pulse of cycle.....	205
Figure 129: The temperature chamber and control system used for passive thermal cycling experiments.	205
Figure 130: Samples constructed for passive thermal cycling experiments. Four samples with encapsulation (top) and eight without encapsulation (bottom) were constructed.....	206
Figure 131: Forward voltage (Vf) change of passively cycled (-55°C to 175°C) encapsulated double-side diode packages.	207
Figure 132: Forward voltage (Vf) change of passively cycled (-55°C to 175°C) unencapsulated double-side diode packages.	208
Figure 133: Images of failed diode package sample 6 showing combination of failure modes at die and tube surfaces.	209
Figure 134: Failure surface of double-side diode package showing excessive amounts of moisture at the top sintered interface.	209
Figure 135: CT X-ray image of failed unencapsulated diode package.....	210
Figure 136: Low resolution CT X-ray images of encapsulated double-side module packages which survived 1000 thermal cycles.....	211
Figure 137: High resolution CT X-ray image of the tube-substrate interface for the encapsulated sample number four which survived 100 thermal cycles.....	211
Figure 138: SAM images of failed unencapsulated diode modules for inspection of the DBC (left) and the die attachment (right).	213
Figure 139: Die shear evaluation of tube bond integrity before cycling.	215
Figure 140: Outline of possible improvements for securing the future of double-side power modules using sintered silver device interconnection.	217
Figure 141: Quarter-bridge module improvements utilizing metallized DBA substrates with Si3N4 isolation layer.....	219
Figure 142: Comparison of high power silicon IGBT to high power silicon carbide MOSFETS.	220
Figure 143: Single-sided prototype SiC packages using sintered silver devices and leads.....	221

Figure 144: Alternative half-bridge configuration by further expansion in the Z-direction..... 223

Figure 145: Summary dimensions for FEA model generated by CHTEP at Tianjin University.
..... 234

Figure 146: The von Mises stress in the fourth cycle of the active cycling regime which does not
adjust convection conditions to account for added thermal mass. 235

Figure 147: The actual device temperature in the fourth cycle of the active cycling regime when
convection conditions are not altered to account for added thermal mass. 236

List of Tables

Table 1: Summary of wire bonding requirements [10].....	5
Table 2: Comparison of available materials for wirebonding. [11-13]	6
Table 3: Available solder candidates for higher temperature applications and selected material properties [25, 26].....	12
Table 4: Common material systems used for transient liquid phase bonding technologies.([27] W. Welch, III, C. Junseok, L. Sang-Hyun, N. Yazdi, and K. Najafi, "Transient liquid phase (TLP) bonding for microsystem packaging applications," in Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05. The 13th International Conference on, 2005, pp. 1350-1353 Vol. 2) Used under fair use, 2014.	13
Table 5: Material property comparison of bulk silver and porous sintered silver.	18
Table 6: Comparison of material properties for selected die attachment technologies.	19
Table 7: Advantages and disadvantages of selected power packaging technologies. [42, 43].....	21
Table 8: Thermal properties of the materials used for analyzing module footprint.	39
Table 9: Estimates of parasitic induction contributions from power module components.....	41
Table 10: Selected mechanical properties for module materials.	43
Table 11: Selected thermal properties of materials for module assembly [66].	47
Table 12: Material properties of module materials used for the FEA thermal analysis [66].....	51
Table 13: Summary of modeled thermal characteristics for modules in different cooling configurations.	61
Table 14: Mechanical properties for materials used in developing a structural FEA model.....	65
Table 15: The sintered silver temperature dependent Young's Modulus relationship used in FEA model construction.([71] K. L. Xiao, Thomas; Wang, Tao; Chen, Gang; Ngo, Khai; Lu, GuoQuan, "Creep Behavior of Sintered Nanosilver Paste" unpublished.) Used under fair use, 2014.....	65
Table 16: Candidate materials for tube compliant interface substitution [70].....	79
Table 17: Comparison of device stress for copper substitution in tube compliant interface.....	80
Table 18: DC inductance matrix for planar tube connected device trace.	83
Table 19: DC resistance matrix for planar tube connected device trace.....	84

Table 20: Tube quantity selection criteria for a footprint measuring 8 mm on one side for a fixed aspect ratio.	97
Table 21: Various encapsulant materials and qualitative properties.	106
Table 22: The measured CTE and glass transition temperature (T_g) of each candidate epoxy and how it compares to the CTE values present in our proposed system.....	110
Table 23: Comparison of material change in length based on the CTE of the material and the temperature experienced in the DC power stage test.....	116
Table 24: Comparison of Powerex datasheet values with measured values from the custom fabricated test setup.....	127
Table 25: Comparison of measured switching characteristics for a packaged quarter-bridge module and the datasheet values provided by ABB, the manufacturer of the devices.	130
Table 26: Calculated thermal resistance and capacitance values for module materials.	148
Table 27: Summary of strain based fatigue models specifically for evaluating fatigue in electronic packages [91].	153
Table 28: Mechanical properties of solid bodies utilized in FEA thermomechanical cycling model.....	157
Table 29: Anand viscoplastic model parameters for sintered silver device attachment published by Yu et al.([92] D.-j. Yu, X. Chen, G. Chen, G.-q. Lu, and Z.-q. Wang, "Applying Anand model to low-temperature sintered nanoscale silver paste chip attachment," Materials & Design, vol. 30, pp. 4574-4579, 2009) Used under fair use, 2014.....	158
Table 30: Third cycle plastic strain change, $\Delta\epsilon_p$, for each package configuration.	166
Table 31: Third cycle strain ranges (in ascending order) for sintered silver interface below die for each package configuration.....	169
Table 32: Thermal time constant (τ) calculated for each of the materials used in the passively cycled module package.	175
Table 33: Third cycle plastic strain change, $\Delta\epsilon_p$, for each package configuration in ascending order.	179
Table 34: Third cycle strain ranges (in ascending order) for sintered silver interface below die for each package configuration.....	182
Table 35: Comparison of Thermal Impedance measurement of the single and double-side quarter-bridge modules before any cycling has occurred.	197
Table 36: Die shear testing of four failed passively cycled unencapsulated double-side diode packages.....	214

Chapter 1. Introduction

1.1. Significance

With increased interest in the reduction of carbon emissions and their effect on the environment, a greater emphasis has been placed on alternative energy sources. This has been seen in numerous government policies aimed at promoting more efficient and more diverse energy sources. In the United States, the American Recovery and Reinvestment Act invested more than 80 billion dollars to increase energy generation, improve the electric grid and enhance vehicle technologies to reduce fuel consumption. Both, the United States and the European Commission have proposed energy plans that will see significant decreases in greenhouse gas emissions while promoting large gains in power generation through renewable sources[3]. These alternative methods of power generation rely heavily on new power conversion technologies for storage and transmission as well as replacement of older, less efficient infrastructure.

A variety of strategies can be used for changing direct current power to multi-phase alternating current or vice versa, but most commonly it consists of variations on a half-bridge inverter circuit. The half-bridge circuit consists of two transistors, one controlling the high-side of the waveform and the other controlling the low-side. The power semiconductor commonly used for the switching is the Insulated Gate Bipolar Transistor (IGBT) because its widespread use makes it more affordable. The IGBT is a silicon device with a theoretical upper operating limit of 210°C [4]. In real inverter topologies, the IGBT is usually accompanied by an antiparallel power diode called a Freewheeling Diode (FWD). The diode is also a silicon device. Silicon devices,

although commonplace, possess switching and conduction losses that increase the temperature of the entire package during operation [5]. There have been numerous efforts recently to move to wide bandgap devices (WBD) made from gallium nitride (GaN) and silicon carbide (SiC) which push the operation temperature to 250°C while reducing the heat dissipated as losses. However, these devices are not yet rated for high temperature use and are more expensive which is a barrier for large scale manufacturing. Even if SiC devices were to become widespread, their use is limited by the temperature rating of the balance of the material in the package.

Obviously, the inverter topology is an integral part of universal energy initiatives and advances in power electronics devices are certainly necessary. However, power electronic packaging must meet or exceed gains made in semiconductor device technology for the energy segment to reach its full potential. A good example of packaging requirements can be seen using the electric vehicle. With the advances in electric vehicles and the increased interest from the major automakers, the number of electrically assisted vehicles on the road is predicted to reach nearly 17 million by 2015. This value is predicted to grow further to almost 50 million by 2020. This represents a growing inverter market when considering the power electronics in these vehicles can be as much as 20% of the cost [5]. The push from inverter suppliers is to reduce the cost of the inverters which means a reduction in the footprint translating to less heat dissipation. Also, an increase in switching speeds results in higher heat from losses. In the case of hybrid vehicle systems, inverters can be exposed to ambient temperatures in excess of 105°C (coolant temperature for engine compartment) or require an extra cooling loop to bring the ambient temperature to 65°C. Although, weight and volume will be reduced, the addition of cooling systems may nullify the savings in inverter packaging. [5, 6]

If it were possible to use silicon devices at higher ambient temperatures or reduce the cooling requirements, electrically assisted vehicles could see large gains by reductions in weight and volume coupled with increases in efficiency. This may be accomplished by simply reevaluating the package architecture. Current power module packaging inhibits cooling from the top side of the devices. Instead, the top of devices use unreliable wirebonds for the electrical connection and the assembly is sealed with encapsulant that has low thermal conductivity. To make innovations in packaging it is necessary to move to architectures that increase top side cooling and remove wirebonds. Several three-dimensional (3D) architectures have been proposed in the past, but their reliance on solder technology has been a barrier to large scale production [7]. By implementing a new die attachment technology like Low Temperature Joining Technology (LTJT) the manufacturing could be made simpler. LTJT using sintered silver as the die connection has greater benefits in that sintered silver possesses higher thermal and electrical conductivity and lower homologous (T_H) than solder alloys.

This document presents a comprehensive approach to the design, manufacture and characterization of functional power module topologies in three-dimensional packages. The modules will utilize large area silicon devices and LTJT for die attachment. This approach required the design of a compliant interface to minimize thermomechanical stresses. The constructed modules with compliant interface will be characterized to determine the effect, if any, on package reliability using cyclic changes in thermomechanical stress. The following material summarizes the power electronics background information and establishes the motivation for the new design.

1.2. Overview of Power Electronic Packaging Techniques

1.2.1. Wirebonding

The wire bond is the most common chip-level interconnect used in power electronics today. Wirebonding was first utilized by Bell Laboratories in 1957 [8]. The technique quickly evolved to incorporate thermosonic and ultrasonic techniques allowing for easier bonding of thermally sensitive devices. Many advances in wirebond alloys and wirebonding machines have been made in the last 50 years and it has quickly become the predominant method for chip level connection[9]. Wirebonding boasts the lowest cost per connection and can easily accommodate new circuit designs.

For power module construction, the wirebonding represents a second order material. The first order materials in basic power modules are the semiconductor devices, the substrate, the baseplate and the bonding material for attaching the semiconductor devices [4]. Other second order materials would consist of encapsulation or polymer casing. The most common devices used in the multichip power module are the IGBT and free-wheeling diodes. These devices are attached to a substrate which consists of an electrically insulating ceramic layer (Al_2O_3 , Si_3N_4 , or AlN) with copper or aluminum metallization attached to both sides. After the devices are attached to the substrate, the top electrical pad can be wirebonded for connection to the outer circuit layout. Common wirebonding processes and their limitations are shown below in Table

1.

Table 1: Summary of wire bonding requirements [10].

Wirebonding	Wire	Pressure	Temperature	Ultrasonic Energy	Forming Gas
Ultrasonic	Al, Au	Low	RT	Yes	No
Thermosonic	Au,Cu,Ag	Low	100°C-150°C	Yes	Yes
Thermocompression	Au,Cu	High	300°C-500°C	No	No

Ultrasonic wirebonding uses a combination of downward force and high frequency (60 kHz-120 kHz) ultrasonic energy to bond wires to the surface of the device. The ultrasonic energy scrubs the device surface allowing the wire to penetrate through any oxides or thin passivation layers on the device surface. The ultrasonic energy is applied with a tool that vibrates mechanically. Thermocompression bonding involves heating the semiconductor device to high temperatures and pushing the wire against the bonding surface at high pressures. Thermosonic processes combine the heat and force of thermocompression bonding with the mechanical scrubbing of the ultrasonic bonding process.

In the past, the two most common wire types for wirebonding were gold and aluminum. Gold wire is normally used for ball or ball-wedge bonding which uses combinations of thermosonic and ultrasonic techniques. Aluminum wire is used only with ultrasonic wedge bonding techniques. Most recently, copper wirebonding has increased in popularity. Copper wire, in addition to being more economical than gold wire, has lower resistance than aluminum and is beneficial in high current applications. However, copper wire is much harder than aluminum or gold wires and exposes the bonding surface to high stresses making it undesirable for sensitive devices. As a means to bridge the gap between cost and performance, silver wire has been proposed as well. Silver is much softer than copper, more affordable than gold and its increased

electrical and thermal conductivities reduce limitations on bond pad complexity and size. A comparison of wirebond material properties is shown in Table 2. [11-13]

Table 2: Comparison of available materials for wirebonding. [11-13]

Material	Ag	Au	Al	Cu
Coefficient of Thermal Expansion (ppm/°C)	19	14.2	23.6	17
Thermal Conductivity (W/m.°C)	428	318	243	398
Electrical Conductivity (MS.m ⁻¹)	62.6	42.6	37.4	59.8
Tensile Elastic Modulus (GPa)	71	78	62	124
Vickers Hardness (MPa)	245	245	147	490

1.2.2. Deposited Metallization

Deposited metallization techniques are those interconnect technologies that rely on deposited metal, through physical deposition and/or chemical plating, for construction of device interconnections. These methods eliminate the wirebonds and any parasitics associated with them. Metallization interconnects are deposited directly on the device electrodes. Because metal deposition techniques are capable of covering large patterned areas simultaneously, the technology is ideal for assembly of modules with intricate patterns and multiple devices. One of the most common packaging schemes using deposited metallization is called power overlay (POL) packaging. The POL technique was developed by General Electric (GE) for high I/O pin count chips. The interconnection density can be very high with normal via-hole diameters as low as 0.25 mm (10 mil).

The POL technology proposed by GE sought to eliminate wirebonds to decrease parasitic inductance and resistance brought on by increased connections. The dense structure, metallized connections and planar contacts lower both the package inductance and resistance by two orders

of magnitude when compared to a wirebond structure. The original POL package was a multilayer structure, which includes power semiconductor devices soldered to a direct bond copper (DBC) substrate from the backside, the polyimide dielectric layer, and the deposited copper on the topside. Differences in device thickness are compensated by copper-tungsten or molybdenum shims [14].

High power POL modules can be made in much the same way as the original POL, but requires more robust elements. Both types of module begin by attaching the power dies to a DBC using solder. A dielectric overlay of polyimide is then placed on the top of the devices and backfilled with a thermoplastic or thermoset resin for increased dielectric strength. In the case of high voltages, the polyimide thickness can be increased. Connections for the top side of the devices are made through a series of vias cut through the polyimide using laser ablation. The vias are metallized by first sputtering a barrier layer of titanium and seed layer of copper. For increased power applications, an additional thicker layer of copper can be electroplated to the seed layer. Topside circuit patterns are fabricated by wet-etching the deposited metal layers. [14]

Another notable interconnect strategy making use of the metal deposition method is labeled embedded power and was developed in the Center for Power Electronic Systems (CPES) center at Virginia Tech [15]. The embedded power technique replaces the polyimide films of the POL with dielectrics screen printed onto thin ceramic substrates. The structure is divided into three sections. The bottom section of the structure is a DBC which allows for solder connection to the bottom of the power semiconductor die. The dies are part of the power stage which is embedded in the center of the structure and connected through patterned metallization layers and ceramic

frames. The remaining area is filled with dielectric. The control circuit can then be arranged directly on top of the structure by solder connecting individual components.

Both structures boast increased connection density and reduced parasitics which translate to increased electrical performance and efficiency and represent early attempts at moving the package architecture into three dimensions. However, both processes are very complex requiring many processing steps and materials.

1.2.3. Controlled Collapse Chip Connection

Controlled Collapse Chip Connection (C4), sometimes referred to as Flip Chip (FC) bonding, is another die bonding technique which seeks to increase the interconnection density by utilizing a dense array of connections. The connection of the device is made with an array of electrically conductive bumps. The bumps can be constructed of conductive epoxy or solders. Conductive epoxy presents a more affordable solution at the expense of reliability. Solder alloys with different proportions of lead and tin have normally been selected for the bump composition in the past, but due to growing environmental concerns, the industry is moving to lead free alternatives.

The solder bumps are created at the wafer level of processing using photolithography techniques. A metallization layer, also known as Under Bump Metallurgy (UBM), is applied to the device surface. A layer of photoresist is then used to define a well for adding a solder seed. Solder is plated in the open well before the remainder of the photoresist is removed. The final step is to

heat the device to solder melting temperature which allows the solder seed to form a natural sphere [16].

After the bump array is created, the device is attached by placing the chip onto the connection pads face down, e.g. flipped chip. Sometimes flux is applied to the bump array before the final reflow step. After attachment, an underfill layer is added by dispensing at the chip edge. The underfill easily penetrates the bonding interface using capillary action. [17] The underfill reduces moisture penetration and helps to reduce fatigue of the bump joint due to Coefficient of Thermal Expansion (CTE) mismatches in application. The benefits to the flip chip technology are the reduction in package inductances due to small bump height and an increase in connection density.

1.2.4. Conductive Epoxy

Electrically conductive adhesives (ECA) offer an alternative to solders and have grown in popularity with the mandate to reduce lead in solder used in electronics. Electrically conductive adhesives consist of conductive fillers embedded in a polymeric matrix. The polymer provides the mechanical strength of the bond while the fillers provide the conductive paths. This varies from the normal interconnection scheme which uses the conductive metal to also provide the package integrity. The ECA matrix can be either a thermoset or a thermoplastic. The thermoplastic resins soften above their glass transition point (T_g) which means epoxy selection weighs heavily on application temperatures. Thermoset resins, which create a three-dimensional irreversible cross link structure, are stable at higher temperatures. There are advantages and

disadvantages to each matrix and proper material selection is crucial. Thermoplastic resins offer the ability to perform rework and repair, but are less susceptible to relaxation which may change electrical properties of the connection over time.

Conductive networks within the resins are provided by metal spheres consisting mostly of gold, silver, nickel, indium, copper, chromium, and even lead free solders [18]. These fillers are usually micron scale spheres, but other aspect ratios like rods, flakes and whiskers have been proposed. The silver filled ECA is most common due to the high electrical conductivity and has low reactivity with oxygen [19].

Conductive epoxies can be separated into two distinct groups, isotropically and anisotropically conductive. Isotropic conductive adhesives (ICA) have the conductive fillers spread evenly throughout the matrix and have the same electrical conductivity in all directions. The filler loading in ICA composites determine the conductivity, but the relationship is not linear. Typically, when the volume fraction of the loading reaches between 25 and 30% the resistivity drops abruptly. This quantity is the critical filler concentration or percolation limit [20].

Anisotropically conductive adhesives (ACA) align conductive paths to provide high conductive paths in one direction and low or no conductivity in the opposing directions. Many different ACA techniques exist, but one notable conductive column technique is proposed by Nitto Denko. Microscale conductive columns are formed in a thermoplastic polymer resin with high glass transition (T_g) temperature. Alignment of the conductive paths helps to overcome the percolation limit [21].

1.2.5. Solders and alloys

Solders are alloys of two or more metals which are used to fuse two metal pieces together. The alloy melting temperature can be much lower than the melting points of the constituents. This can be seen by referencing the binary phase diagram of a well-known solder alloy containing lead and tin [22]. The left and right axes of the phase diagram represent the melting points of pure lead and tin, respectively. The liquidus line marks the melting point of the alloy as the composition is altered by moving along the x-axis from left to right. The minimum melting point is found at a 61.9 wt% tin and 38.1 wt% lead. The composition with the minimum melting point is referred to as the eutectic of the system.

The melting temperature for eutectic lead-tin solder is approximately 183°C. The recommended processing temperature for this alloy is 220°C. Obviously, the recommended application temperature must stay below 183°C or joints could reflow. Solders should not be utilized at temperatures that exceed 80% of their melting temperature in units of Kelvin. In the case of lead-tin eutectic solder the application temperature must not exceed 91.8°C. This alloy is desirable for processing because of its low melting temperature, but it isn't capable of high temperature operation. The applications are limited further with increased restrictions on lead containing solders.

In 2006, the European Union Waste Electrical and Electronic Equipment Directive (WEEE) and Restriction of Hazardous Substances Directive (RoHS) began prohibiting the addition of lead to

electronics [23, 24]. Alternative alloys based on the tin-silver-copper ternary system were then adopted. These solders are termed Sn-Ag-Cu (SAC) solders. The melting temperature of the ternary eutectic point in this system is 217°C at a composition containing 3wt% silver, 0.5 wt% copper and the balance of tin. For increased reliability, the application temperature should not exceed 119°C. This composition is known as SAC 305.

Solder alloys explicitly for use at high temperatures are difficult to find. For reliable use at application temperatures of 175°C, the melting temperature of the solder must be greater than 287°C. Several candidates with higher melting temperatures can be seen in Table 3 below.

Table 3: Available solder candidates for higher temperature applications and selected material properties [25, 26].

Solder Alloy (wt%)	Liquidus (°C)	Thermal Conductivity (W/m.K)	Coefficient of Thermal Expansion (ppm/K)
Sn-3.5Ag	221	55	~30
Sn-3.0Ag-0.5Cu	217	63	21.6
Sn-0.7Cu	227	66	21.5
Sn-5Sb	240	48	23
AuSn	280	57	16.5
AuGe	356	44	14

1.2.6. Low Temperature Joining Technologies

1.2.6.1. Transient Liquid Phase (TLP)

Transient liquid phase diffusion bonding (TLPDB) is sometimes called diffusion soldering. In TLPDB a low melting temperature interlayer is placed between metals that are to be bonded. When the interlayer melts it reacts with the parent metals applied at the joining surfaces and

creates intermetallics. The intermetallics have much higher melting temperatures than the original interlayer allowing the joint to withstand application temperatures much higher than the processing temperatures. Further heating allows the joint to become more uniform in composition.

Parent metals for the TLPDB bonding technique needed to be applied to their respective surfaces using electroplating or evaporation techniques. Also, in addition to the processing requirements listed below, many times a pressure needs to be applied during processing and the atmosphere may need to be removed or controlled to discourage oxide formation. Common material systems and their processing requirements are listed below in Table 4 [27].

Table 4: Common material systems used for transient liquid phase bonding technologies.([27] W. Welch, III, C. Junseok, L. Sang-Hyun, N. Yazdi, and K. Najafi, "Transient liquid phase (TLP) bonding for microsystem packaging applications," in Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05. The 13th International Conference on, 2005, pp. 1350-1353 Vol. 2) Used under fair use, 2014.

Material System	Processing Requirements	Joint Remelt Temperature (°C)
Copper-Indium	4 min @ 180°C	>307
Copper-Tin	4 min @ 280°C	>415
Silver-Tin	60 min @ 250°C	>600
Silver-Indium	120 min @ 175°C	>800
Gold-Tin	15 min @ 260°C	>278
Gold-Indium	0.5 min @ 200°C	>495
Nickel-Tin	6 min @ 300°C	>400

In addition to cost barriers, the processing requirements can be intricate and vary widely for each system.

1.2.6.2. Sintered Silver

The Sintered Silver Low-Temperature-Joining-Technique (LTJT), was first introduced by Schwarzbauer [28, 29] nearly two decades ago, in the late 1980's. Schwarzbauer's technique employed the use of silver particles and flakes which were sintered, rather than melted, for joining of large-area silicon devices with molybdenum plates. The melting temperature for bulk silver is 960°C so joints created at lower temperatures must rely on diffusion processes rather than liquid phase reactions like solder. Sintering by solid state diffusion is called solid state sintering and can theoretically occur in three distinct steps yet in practice the steps overlap. The initial stage allows for particle rearrangement to increase interparticle contact and allow for neck formation. In the second stage, densification occurs and the network formed in stage one grows while the pores decrease in size. When the pores reach a minimum the second stage ends and third stage begins. In the final stage of sintering the remaining isolated pores will disappear and grain growth begins. Large grains will grow at the expense of the smaller grains. It is in the final stage that the density begins to approach the theoretical value.

When utilizing silver particles, agglomeration and aggregation are inhibited by thoroughly coating the particles with an organic capping material. This organic material will be burned away if the process exceeds 210°C in air. A sufficient amount of oxygen must be present in the sintering atmosphere for the organics to burn away and allow interparticle contact for sintering to be achieved. Early experiments with sintering of silver flakes or micron scale silver particles required high pressures and high temperatures so binder removal was not an issue. To decrease the sintering pressure, an increase in sintering temperature is required and vice versa. Neither

the use of high pressures nor high temperatures is desirable when considering silver sintering as a viable device interconnect technique. Schwarzbauer had found that adequate conductivity and sintered density could be achieved by sintering at 650°C. It was later found that the addition of 40 MPa pressure during sintering allowed ample densification at 250°C [29-32]. The improvement in sintering temperature with applied pressure allows the interconnection to be formed at or below the reflow temperatures of available solders. With the applied pressure, the silver interconnection also has a much lower homologous temperature because the bond temperature represents approximately 1/4th of the melting temperature. Silver was already a desirable interconnect material because it possesses a threefold higher thermal and electrical conductivity than solder attachment. Yet, with a processing temperature comparable to solder reflow temperatures and a small homologous temperature, sintered silver is desirable from a manufacturing and reliability point of view.

Further reduction of the sintering pressure has been the topic of much research. One technique was to adjust the particle size as a means to increase the driving force for sintering. The solid state sintering for silver particles follows the Mackenzie-Shuttleworth sintering model where the change in density over time ($\frac{d\rho}{dt}$) is given by

$$\frac{d\rho}{dt} = \frac{3}{2} \left(\frac{y}{r} + P_{applied} \right) \times (1 - \rho) \left(1 - \alpha \left(\frac{1}{\rho} - 1 \right)^{\frac{1}{3}} \times \ln \frac{1}{1 - \rho} \right) \frac{1}{\eta} \quad (1)$$

where γ is the surface energy; r is the particle radius; and P_{applied} is external pressure or stress [33]. The driving force is represented by the terms containing the applied pressure $\left(\frac{\gamma}{r} + P_{\text{applied}}\right)$ which is normally adjusted by applying an external pressure during sintering. The surface energy in this term can be increased by simply lowering the particle radius, r . If the particle radius moves from micron scale to nanometer scale, the driving force can be increased 10 fold. It is this mechanism which allows further reduction in sintering pressures utilizing the nanoscale LTJT or sintered nanosilver. In the case of small area interconnection the pressure requirement has fallen to zero. For large scale attachment ($> 10 \text{ mm} \times 10 \text{ mm}$), the applied pressure has been lowered to only a few MPa [34].

There also exist special requirements for surface preparation when using LTJT techniques. Because the sintering bonding strength is based on the atomic diffusion of silver into joined materials, the bonded surface must be metallized with silver or gold. The diffusivity of silver atoms in these metallization layers must be reasonably high so that the as-formed bonding has good mechanical strength. In addition, the bonded materials must exhibit oxide-free surfaces. These requirements normally present a barrier to integration of sintered silver as a viable interconnection for large scale manufacturing. However, recent research efforts have shown that attachment on easily oxidized bare copper surfaces is possible by controlling the sintering atmosphere. Even so, aluminum coated or passivated die still require metallization which is normally prepared by applying a diffusion barrier consisting of nickel and a thin noble metal finish or high purity electroless plating of silver, gold or platinum. Two common UBM schemes which have proven compatibility with sintered silver are 1) titanium and silver and 2) chromium, nickel and silver [9].

The standard LTJT process for pressure sintering consists of the following steps.

1. Application of silver paste by stencil printing.

Silver paste can be applied by screen printing, stencil printing, spray coating, automated dispensing, or through application of a preform.

2. Drying to remove low temperature organic solvent.

The silver particles are suspended in organic solvent with a viscosity adjustable to the respective application method. After applying the silver paste, the organic solvent has to be evaporated at a relatively low temperature, approximately 180°. By removing the organic solvent, the green density of the silver flakes is significantly increased and will allow for increased densification during the sintering process.

3. Components are aligned and placed.

Components or devices are placed on top of the paste after the drying stage. Layers of aluminum foil and rubber are placed on the devices for protecting the devices during the pressing process. The aluminum foil is employed to prevent the rubber layer from sealing the edges of the mounting and preventing oxygen flow needed for binder removal.

4. Sintering of the silver paste, with pressure assistance.

The pressure needed for sintering is applied with a hydraulic press which can be adjusted to apply a range of pressures allowing for both large and small device footprints.

The process for pressure-less sintering is further simplified. The silver paste can still be applied by screen printing, stencil printing, spray coating, automated dispensing, or preform. The bond line can be controlled using a bond line controller and the entire package is then heated to sintering temperature. In the case of copper attachment, this process would take place in a controlled atmosphere.

Due to the porosity of the sintered interconnect, which approaches 15-20% in most cases, the properties of the sintered silver deviate from those of pure (bulk) silver. A comparison of sintered and bulk silver property is shown in Table 5 below. Data, not in agreement, have their sources indicated.

Table 5: Material property comparison of bulk silver and porous sintered silver.

	Bulk Silver	Sintered Silver (80-85% theoretical density)
Melting Temperature	960°C	960°C
Density	10.49 g/cm ³	8.9 g/cm ³
Electrical Conductivity	63 MS/m	25-41 MS/m ^[19, 35]
Thermal Conductivity	429 W/m.K	175-250-290W/m.K ^[19, 35, 36]
Specific Heat	0.234 ^[13]	0.233-0.245 ^[19, 37]
Coefficient of Thermal Expansion	18.9 ppm/K	18.9 ppm/K ^[35]
Young's Modulus (Elastic Modulus)	76-83 GPa ^[13]	10-40 GPa ^[35]
Tensile Strength	125 MPa	43 MPa-55 ^[19, 37]
Yield Stress	55 MPa ^[13]	43-60 MPa ^[35]

Even considering the effect of porosity, LTJT possesses superior thermal and electrical conductivity. Table 6, below, shows a property comparison of sintered silver and common soft solders.

Table 6: Comparison of material properties for selected die attachment technologies.

	Eutectic lead-tin solder	Lead-free solder	Eutectic gold-tin solder	Conductive Epoxy	Nanosilver paste
Bonding Mechanism	Liquidus reflow	Liquidus reflow	Liquidus reflow	Epoxy cure	Sintering/solidus interdiffusion
Peak Process Temperature	214°C	220°C	320°C	150°C	275-290°C
Composition	Pb37Sn63	Sn96.5Ag3.0Cu0.5	Au80Sn20	Silver filler with organic resin and hardener	Pure silver >99.8 wt%
Maximum use temperature	<180°C	<175°C	<280°C	<150°C	<960°C
Electrical Conductivity	$0.69 \times 10^5 (\Omega\text{-cm})^{-1}$	$\dagger 1.0 \times 10^5 (\Omega\text{-cm})^{-1}$	$0.62 \times 10^5 (\Omega\text{-cm})^{-1}$	$0.1 \times 10^5 (\Omega\text{-cm})^{-1}$	$2.6 \times 10^5 - 4.1 \times 10^5 (\Omega\text{-cm})^{-1}$
Thermal Conductivity	51 (W/m.K)	33 (W/m.K)	58 (W/m.K)	~0.1 (W/m.K)	175-290 (W/m.K)
Coefficient of Thermal Expansion	25 (ppm/K)	~23(ppm/K)	16 (ppm/K)	~25(ppm/K)	18.9(ppm/K)
Elastic Modulus	16 GPa	50 GPa	68 GPa	<1 GPa	10-40 GPa
Yield Strength	27MPa	34.2 MPa	N/A	N/A	43-60 MPa
Tensile Strength	27MPa	41.1 MPa	275 MPa	~10 MPa	43-55 MPa

The large difference between processing and melting temperature for LTJT suggests the effects of creep at application temperatures will be negligible which leads to increased reliability. Devices attached using LTJT have shown large improvements in temperature cycling performance with 10 times improvement over solder lifetime using max cycling temperatures of both 125°C and 175°C [38, 39]. Power cycling improvements were seen as well. Packages utilizing a sintered connection (Figure 1) on both the top and bottom of the die experienced approximately 17 times improvement in lifetime. Soldered packages in the same experiment failed by wire bond lift-off [38].



Figure 1: Double-side device connection using sintered silver LTJT. The top electrical connection is made from silver ribbon attached with sintered silver rather than traditional wirebonding techniques.([38] M. Knoerr, S. Kraft, and A. Schletz, "Reliability assessment of sintered nano-silver die attachment for power semiconductors," in Electronics Packaging Technology Conference (EPTC), 2010 12th, 2010, pp. 56-61.)
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The reliability improvements using a double-side device attachment further promotes the benefits of utilizing the entire top electrical pad for bonding. This type of connection is sometimes referred to as a planar or area connection [40]. It was just these benefits which led to the increased connection density used in flip chip technology. The solder ball area arrays of flip chip packaging decrease contact resistance, decreased parasitic inductance, larger and more uniform current handling and decreased cost [40].

1.2.7. Summary of Selected Power Packaging Technologies

With a wide range of interconnect technologies available, it should be relatively easy to find a solution for any power electronics package. A summary of selected interconnection schemes are listed in Table 7. The table presents an overview of the advantages and disadvantages of each technology discussed.

Table 7: Advantages and disadvantages of selected power packaging technologies. [41, 42]

Technology	Pros	Cons
Wirebond	Most familiar technology; flexible when design changes; low cost; fewest requirements for wafer processing.	Poor thermal management; low reliability, increased parasitics, current crowding; not readily compatible with 3D packaging.
Solders and Alloys	Ease of processing; emerging alloys for increased temperature.	Unreliable at high temperatures; special processing for void free joints; low thermal conductivity.
Power Overlay	Shorter electrical paths reduce inductance; multi-level integration for quasi 3D package.	Complex and costly processing, large thermal mismatch, increased parasitic capacitance.
Embedded Power	Compatible with thick film processing; Shorter electrical paths reduce inductance; multi-level integration for quasi 3D package.	Complex and costly processing, large thermal mismatch, increased parasitic capacitance; limited in voltage and current level.
Conductive Epoxy	Wide array of configurations and compositions; low temperature process	Application temperatures are limited by low Tg of compositions. Low thermal conductivity; low current and voltage capability.
Flip Chip (Area Solder Arrays)	High package density and lower interconnect lengths lead to decreased parasitics; lower cost than deposited metallization; increased reliability;	Requires wafer level processing; Fatigue of solder joints; limited in current and voltage levels.
Transient Liquid Phase Bonding	Low temperature joining technology for high temperature applications.	Expensive parent metals; Intricate processing parameters; Not easily commercialized.
Sintered Silver LTJT	High thermal and electrical conductivity; Processing requirements are simple; Processing temperature is equivalent to solder reflow temperatures. High melting temperature for increased reliability, lower relative cost;	Rework is difficult.

Two of the most familiar technologies are commonplace in power packages today; wirebonding and soldering. These technologies have the advantage of being relatively easy to process and inexpensive. However, the disadvantages of these two technologies are that they present a barrier to new architectures and reliability at higher application temperatures.

1.2.8. Shortcomings of Current Solder Technologies

Current module architectures consist of semiconductor devices attached to a substrate utilizing a number of different die attachment materials. Most often the die connection material is one of a range of available solder alloys. The available solder alloys, however, have narrowed as power electronics manufacturers' move from using lead based solders to avoid environmental concerns. The most commonly used of the remaining lead-free alloys consist mostly of tin with small amounts of copper or silver. These lead-free alternatives reflow at around 220°C [38]. However, solders should not be used at temperatures greater than 80% of their absolute melting temperature (in Kelvin) due to increased creep which translates to decreased reliability. This means that solder alloys for application temperatures of 200°C must have melting temperatures greater than 318°C. This additional requirement severely limits an already narrow field of alloys. As previously discussed, alloys for these applications do exist, but are plagued by excessive cost and/or difficult processing [38]. The temperature demands and unavoidable creep fatigue is the reason solder joint fatigue failure is second only to wirebond failure as the most common cause for failed packaging.

The mechanical properties of solder in packages are not just temperature dependent, but are also greatly affected by strain rates, microstructure (grain size) and thermal history. Additionally, solder under large mechanical strains, induced from active and passive cycled thermal mismatch of materials, will ultimately fail from low cycle fatigue. If cycling profiles contain dwell periods at larger temperatures, the solder alloy will also exhibit relaxation. This effect sometimes reduces stresses from fabrication and reduces the device curvature. However, relaxation also

decreases the amount of recoverable strain which lowers the stress required on each successful reheating to produce a similar strain. This effect slowly reduces the elastic strain.

High temperature, low cycling fatigue includes pure fatigue, creep, stress relaxation, stress recovery, diffusion processes and corrosion. Increased temperature and stress can allow diffusion processes to occur at bond interfaces where undesirable intermetallics can form with metals from the bond pads. One example of this is tin migration into the gold metallized surfaces allow for a weak Au-Sn intermetallic formation at the interface. With lead containing alloys, migration of the other metal leaves behind a lead rich phase with reduced creep and fatigue properties and even suffers from oxygen embrittlement at cracks and grain boundaries.

Because of the mobility of solder at higher temperatures, solders used in packaging are sometimes referred to as soft solder alloys and are usually modeled using viscoelastic model parameters. This viscoelastic model implies the ductile metal will experience only a very small amount of work hardening under cycling conditions. Common fatigue models used for solder alloys are the inelastic strain amplitude models (Coffin-Manson type), the total inelastic strain energy models (hysteresis area) and Crack growth models.

1.2.9. Shortcomings of wirebond technology

Three-dimensional power electronics have been proposed for some time as a means to push the limits of power semiconductor devices. The largest driving force for moving the circuit upward

is the reduction of wire bonds [43]. Wire bonds are cited as the most common failure mechanism in power electronics module packages [2].

Cyclic loading within the module results in wire-bond lift-off, increased flexural stresses in the wires, failure at each bonding site due to increased shear stresses and even work hardening of the aluminum wire. Examples of the most common wirebond failure mechanisms are given by Smet et al and pictures of these are shown in Figure 2 [2].

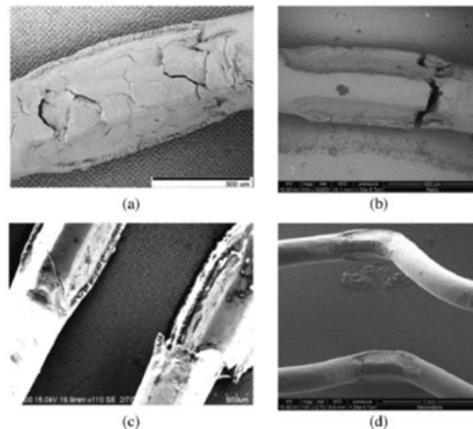


Figure 2: Examples of common wirebond failure mechanisms. a) metallurgical damage b) heel cracking c) wirebond fracture and d) wirebond liftoff. ([2] V. Smet, F. Forest, J. J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani, "Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 4931-4941, 2011) Used under fair use, 2014.

Additionally, non-uniform heating of wirebonded devices can arise from wirebonds having limited connection areas, when compared to large area device pads. These localized welded connections result in differences in wire impedance based on mutual coupling effects and current crowding. Electrically, the wire bonds add additional parasitic inductance [44]. Each wirebond can contribute as much as 10 nH of parasitic inductance and the large silicon die sizes require many wirebonds per device [4, 43]. Added inductance can lead to higher switching losses and

high device turn off spikes. These combined effects may in turn lead to shoot-through failure of the connected devices.

The issues wirebonding presents for single sided device connection are widespread. These problems are exaggerated further with attempted integration into 3D architectures. For single sided attachment, wirebonding uses the tops of the devices inefficiently and does not contribute to reductions in thermal resistance. Additionally, after wirebonding the top of the dies, a flexible encapsulant is added to protect the top surface of the dies and delicate wirebonds. The encapsulant is selected, not for its thermal qualities (thermal conductivity of the encapsulate could be as low as 1 W/mK), but instead, for its modulus and dielectric strength and also fails to add additional thermal benefits. Manufacturers of power modules ignore thermal top side thermal resistance altogether and instead dwell on only the thermal resistance from junction to case ($R_{th\ j-c}$) and/or the thermal impedance for a transient period reference the junction to case of the module ($Z_{th\ j-c}$) [4]. Attempts to use wirebonds in three-dimensional packages (Figure 3), which have already proven to added parasitic resistance and inductance per unit length of wire, require much longer wires spanning much larger distance.

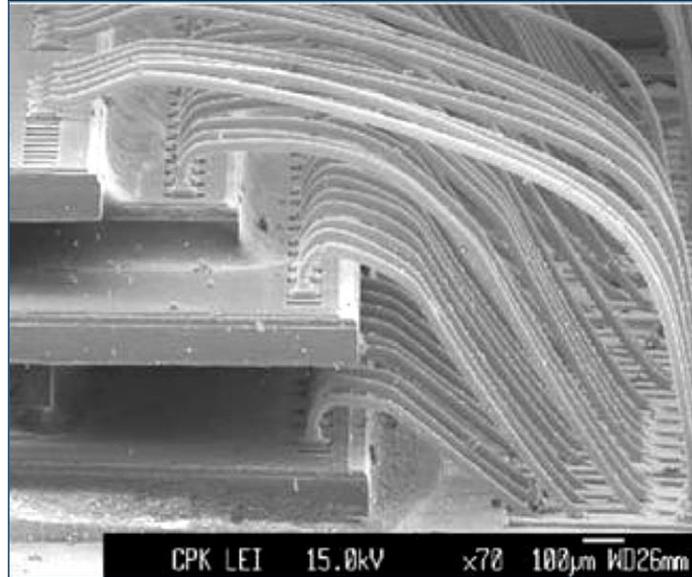


Figure 3: Example of attempted 3D packaging using wirebonding for multilevel device connection.([45] J. Sylvester. (2012, 10/22/13), Electronic Components and Technology Conference (ECTC)). Used under fair use, 2014.

It is obvious from these observations that wirebond technology presents a barrier to further progress of the current module packaging scheme even with myriad attempts to keep the technology viable.

1.3. Introduction to Three-dimensional Circuit Architecture

With the continued improvements in power semiconductor devices and advanced high thermal conductivity substrates, high performance systems capable of high temperature operation are a real possibility. The barrier to system performance is now an issue of proper electronic packages. Conventional module construction, regardless of materials selected, fail to efficiently dissipate heat, reduce circuit parasitics, and take advantage of the entire package volume. To increase heat dissipation on the device, many have proposed area attachment of heat sinks to the

top of semiconductor devices [7, 43, 46-49]. Efficient use of the device top and bottom increases the silicon efficiency which is defined as the heat sink surface area divided by the device footprint area. In a true 3 dimensional package, the silicon efficiency approaches 200%. The Multi-Chip Module (MCM) planar packages using three-dimensional topologies also boast 40-50 times size and weight reduction [50].

Three-dimensional structures have been researched in the past citing many of the benefits already discussed. One notable structure was developed at Virginia Tech in the Center for Power Electronics (CPES) and was termed the Metal-Posts Interconnected Parallel-Plate Structure (MPIPPS) [7, 41, 46]. The bottom half of the structure is much like the conventional power module construction in that devices are secured to a DBC substrate using solder. However, electrical connections on the top of the die are made using soldered copper posts which utilize the entire top surface of the device. The top of the copper posts are then soldered to substrate identical in composition as the bottom substrate. A schematic of the structure can be seen in Figure 4.

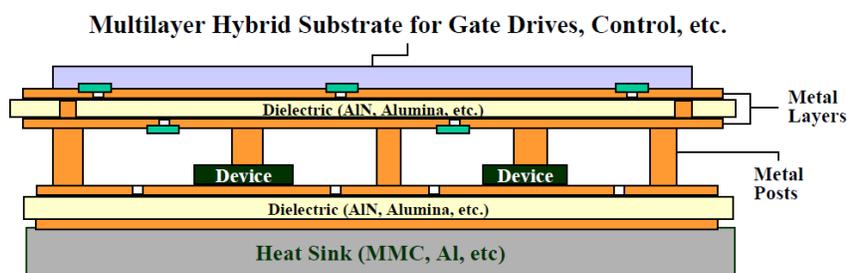


Figure 4: Schematic of one of the earliest proposed 3D circuit architectures. This structure is called the Metal Posts Interconnected Parallel Plate Structure (MPIPPS) and is fabricated using conventional solders. ((www.cpes.vt.edu) Accessed 5/19/14) Used under fair use, 2014.

This structure has eliminated the wirebonds altogether and by bonding the entire area of the device, contact resistance of the connections has been reduced [40]. Additionally, the use of the top substrate as a conductor with similar dimensions as the bottom conductor, not only has the parasitic wirebond inductance been decreased, but the symmetrical layout of current paths lowers inductance further [51]. Additional reduction in package parasitic inductance and capacitance result from reduction of interconnect length. The signal delay reduction as a result of 3D packaging can be as much as 300% [50]. Simulations comparing half-bridge circuits packaged in 3D structures to that of the more common wirebond structure have shown reductions in critical parasitic impedance and inductance. These improvements also lead to faster switching times [52]. The largest benefit of the structure, however, is the thermal improvements. Heat generated in these devices can now escape through both the top and bottom paths more efficiently. Additionally the open space between the two layers can be force cooled using dielectric fluids allowing for larger thermal benefits. Although this is the forerunner to 3D packaging, more recent contributions will be discussed in Chapter 2.

1.4. Motivation for Double-Side Packages using Sintered Silver LTJT

It is clear that packaging architecture requires improvements if it is to keep pace with material and substrate technologies. More efficient use of the silicon footprint and package volume is one of the technology drivers; however increased heat dissipation and reliability are paramount to progress. Quasi three-dimensional structures like POL and Embedded Power architectures are moving in the correct direction, but fall short in current capability, manufacturability and material mismatch. True three-dimensional architectures have illustrated great benefits

thermally and allow for efficient use of the package volume, but still rely on solder technology which severely limits the application temperatures and/or reliability.

1.5. Objectives and Significance of Study

In this study, we design and fabricate functional three-dimensional power module switching units using sintered silver LTJT with a stress relieving compliant interface. The specific objectives of this work are as follows:

- 1. To design power module packages which operate at 1200 V, 150 A and utilize a three-dimensional architecture for enhanced cooling capability.**
- 2. To create a FEA model of the power module design for evaluation of thermal properties and thermomechanical stress.**
- 3. To fabricate functional three-dimensional power modules based on LTJT processing parameters and design constraints.**
- 4. To characterize the thermal and electrical properties of the functional power module.**
- 5. To integrate fabricated prototype power modules into a working inverter system.**
- 6. To characterize the package reliability by exposure to large temperature extremes using active thermal cycling testing.**
- 7. To characterize the package reliability by exposure to large temperature extremes using passive thermal cycling testing.**

- 8. To compare and contrast failure mechanism predictions from FEA models with actual package failure conditions.**

1.6. Organization of Dissertation

This dissertation is organized into seven chapters using the following scheme. The current chapter (Chapter 1) provides a background review of the research topics and current state of the technology. This overview provides the motivation for the research topic and its significance.

Chapter 2 will begin by reviewing several of the most successful attempts, to date, of 3 dimensional power module packaging with the goal of decreasing thermal resistance. This review will introduce many of the constraints for the design of the double-side sintered planar power module and its integration into applications. Other design parameters will be discussed with an emphasis on the thermomechanical stress contributions during fabrication and integration into commercial applications.

Chapter 3 will outline the fabrication of both a half-bridge and quarter-bridge power module package. This chapter will include all steps need to produce the final functioning prototypes of each.

Chapter 4 will discuss electrical characterization of the module during and after fabrication. Extended discussion of thermal characterization techniques used to properly assess the thermal benefits of a double-side package will also be discussed in detail.

Chapter 5 will present approaches to assess the reliability of the packaged module with an emphasis on the proposed corrugated tube structure. FEA models will be utilized for assessment of strain parameters in different package configurations. These parameters will be compared in order to make inferences on the relative changes to configuration lifetimes. The model parameters will attempt to mimic those of the actual experiments. Experimental procedures for both active and passive cycling experiments will be discussed as well as failure criteria.

Chapter 6 looks to the future of the double-side packaging using sintered silver LTJT and the benefits from further improvements in the design, the materials and the devices.

Chapter 7 presents a summary and conclusions.

1.7. Publications and Patents

Patent Submission. Title: Methods of Components for Connecting Planar Power Electronics.

Submitted May 7, 2012. Application number 61643423. Attorney Docket Number A0138.6001

Chapter 2. Design of a Double-Side Cooled Power Module

2.1. Prior Arts in Double-Side Integration

The MPIPSS module was a pioneer of three-dimensional packaging and was evaluated at a time when solder was the predominate first level die attachment method. More recent developments can be readily found in literature. Another package which is based on the original MPIPSS structure reduces the thermal path lengths further by scaling down the height of the copper post interconnects. This system is referred to as the Micro Post Interconnection (MPI) package and utilizes copper posts only 60 microns tall. Rather than using solder technology as the device interconnection, the structure uses copper diffusion bonding under high pressures and inert atmosphere. The fabrication of this structure is very complex, but has also proven that a dense structure reduces thermal paths and parasitics [53].

Another development in double-side design which still utilizes solder as its primary interconnection also uses spacers between top and bottom substrates. A copper solid square, tube or solid round is soldered between the top of the device and the top substrate. The copper spacer reduces the stresses while attempting to maintain heat flow through the top of the device [49]. The dimensions of the device and the package presented by Li et al. can be seen in Figure 5.

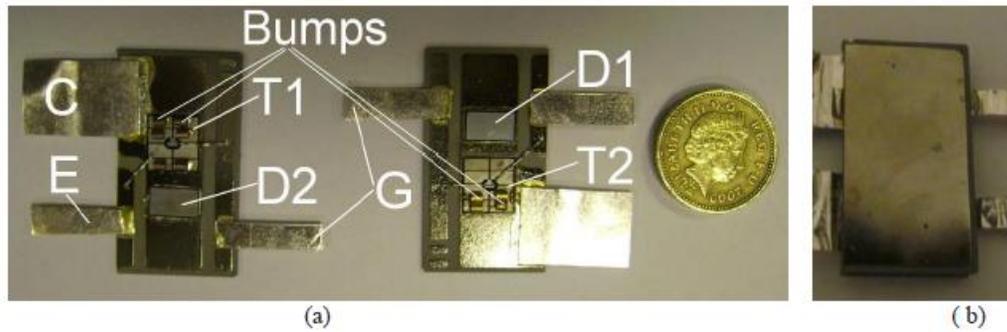


Figure 5: One example of similar double-side cooling attempt using a single switching quarter-bridge module fabricated with (a) solder copper tubes between the devices and top heat sink. The final package with top heat sink (b). ([49] J. F. Li, A. Castellazzi, A. Solomon, and C. M. Johnson, "Reliable Integration of Double-Side Cooled Stacked Power Switches based on 70 micrometer Thin IGBTs and Diodes," in *Integrated Power Electronics Systems (CIPS)*, 2012 7th International Conference on, 2012, pp. 1-6) Used under fair use, 2014.

Researchers at ALSTOM Power Electronics Associated Research Laboratory (PEARL) have also fabricated prototype double-side modules using solder technology. Their earlier work was very closely related to the previous example and also utilized small copper posts or spacers to attach a top-side heat sink. Citing the need to reduce thermomechanical stress, additional electrically isolated copper posts were added around the interior perimeter to prevent failure from thermomechanical stress [54]. The exact dimensions of the spacers used in this project were not disclosed nor were the solder alloys used, but images suggest spacers measure less than 1 mm in height. More recently, this same research group has fabricated prototype modules based on a much larger copper sphere called a power bump. These power bumps are spherical solids soldered between the top of the device and the bottom of the top substrate to complete a half bridge three-dimensional switch. Although these power bumps seem larger in scale than earlier attempts, the dimensions are not disclosed. This work boasts lower electrical resistance in the bump connection when compared to conventional wirebond connections. The cycling lifetime was assessed as well. The passive cycling lifetime was found to be 500 cycles (-40°C to 125°C)

even though substrate delamination occurred well before at 300 cycles. The active cycling lifetime was measured to be 100000 cycles with a ΔT of 80 K [54]. The most recent work on the ALSTOM power bump was the implementation of module stacks. These modules used the power bump technology to push the packaging further upwards. To do this, multiple switching units were stacked on top of each other using soldered power bumps for each interface [55]. An example of the prototype can be seen in Figure 6. The top view reveals the scale of the power bumps when compared to the device size which suggests the spheres are on the order of millimeters. The bottom view indicates the electrical schematic and footprint. The exact dimensions and the device ratings were not specified.

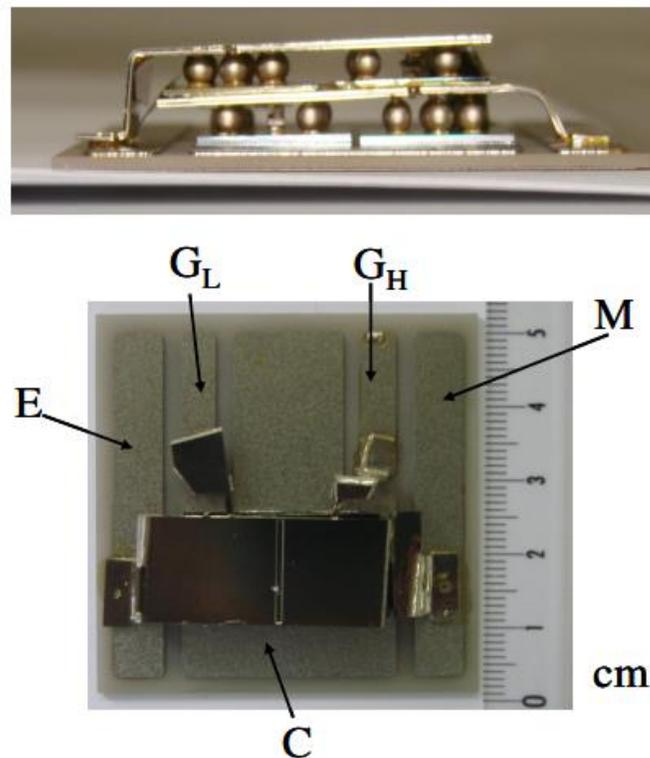


Figure 6: Side view (top) and top view (bottom) of prototype three-dimensional module showing one switching unit (IGBT and diode) attached directly above another switching unit using arrays of soldered copper spheres called power bumps. ([55] M. Mermet-Guyennet, "New structure of power integrated module," in Integrated Power Systems (CIPS), 2006 4th International Conference on, 2006, pp. 1-6.) Used under fair use, 2014.

A double-side package has also been developed by Oak Ridge National Labs (ORNL), but specifies a wide variety of possible die attachment techniques up to, and including, transient liquid phase bonding and sintered silver LTJT. The ORNL module labels the module connection the planar bond all technique. This module specifies integrated cooling channels on the top and bottom of the sandwich structure and boasts integrated forced cooling capability [56]. The patent illustrations from the patent application (13/547937) submitted in January 24, 2013 describing the package components in detail can be seen in Figure 7.

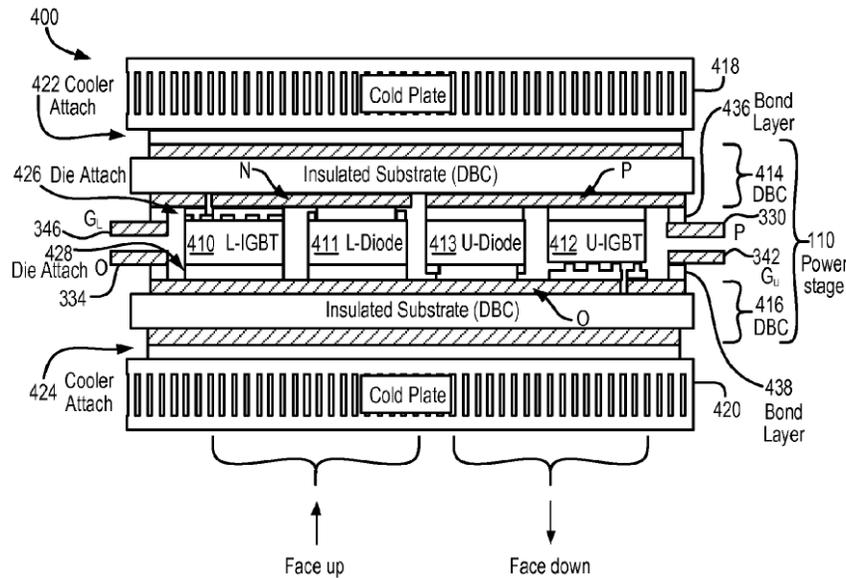


Figure 7: Patent application illustration from patent application number 13/547937 submitted by Liang et al on January 24, 2013. ([56] Z. X. Liang, Martino, L., Ning, P., Wang, F., "POWER MODULE PACKAGING WITH DOUBLE SIDED PLANAR INTERCONNECTION AND HEAT EXCHANGERS," 2013) Used under fair use, 2014.

In the ORNL patent application the structure is described as a half-bridge power module using two pairs of IGBTs and diodes. One switching unit is arranged face down and the other is arranged face up. The relative scale of the module can be seen in a photograph (from the patent

application) in Figure 8. Two sets of gate and emitter pins leave the front of the module and input and output tabs are located together on the back of the structure. The cooling channels in this prototype are fabricated of copper.



Figure 8: Image of prototype double-side cooled power module from patent application 13/547937 submitted by ORNL researchers.([56] Z. X. Liang, Martino, L., Ning, P., Wang, F., "POWER MODULE PACKAGING WITH DOUBLE SIDED PLANAR INTERCONNECTION AND HEAT EXCHANGERS," 2013) Used under fair use, 2014.

The most recent sintered silver structure reviewed closely resembles that of this research topic. This package, fabricated using only sintered silver on the top and bottom interfaces, contains a diode. The diode measured only 3.5 mm by 3.5 mm (small area die) and was purchased with Ti/Ni/Ag top metallization expressly for compatibility with sintered silver processing. The assembly process utilized pressure, but there is no quantity specified. [57] A picture of the double-side product is seen in Figure 9.



Figure 9: Double-side single diode package using only sintered silver for attachment of the top and bottom substrates. Work and photograph courtesy of Masson et al.([57] A. Masson, S. Azzopardi, F. Le Henaff, J. Y. Deletage, E. Woirgard, S. Bontemps, and J. Joguet, "Processing and Characterization of a 100% Low-Temperature Ag-Sintered Three-Dimensional Structure," in *Power Electronics and Applications (EPE)*, 2013 15th European Conference on, 2013, pp. 1-9.) Used under fair use, 2014.

Although these attempts at three-dimensional packaging are similar to the work shown in this document, the true judge of the technology's success depends on their reliability, thermal resistance, ease of processing, and system integration.

2.2. Investigation of Double-Side Structure for Multichip Power Modules

In this research a double-side module for high power large area silicon semiconductor devices is considered. The package must be capable of pushing the silicon device to upper application temperatures (175°C) using high voltage (1200 V) and high current (150 A) devices.

2.2.1. Thermal Contributions

The module footprints in this study begin by closely emulating the footprints for MPIPPS modules from previous research [48]. The MPIPPS module layout utilized a square footprint

50.8 mm by 50.8 mm. This footprint divided into fourths for placement of the diodes and IGBTs. This layout provides a guideline on a recommended layout for integration.

The distance between the IGBT and diode within this footprint is a compromise between structural integrity, thermal optimization and integration into existing inverter topologies. The device placement should avoid thermal superposition effects from device self-heating during operation while stabilizing the top and bottom substrates. [4] The ideal structural placement for the devices is very close to the outside edge, but that position is not the best thermally because heat is not dissipated equally from all sides. The dies are therefore placed equidistance from each other and from the edges (with consideration given to input and output tab attachment).

A finite element analysis (FEA) thermal model was constructed using ANSYS® Workbench™ Academic Research, Release 14.0 [58]. The results from the model were used to validate the device position. Device losses provide an estimate of boundary conditions for single sided thermal simulation. Normally, losses can be divided into three categories; switching losses, conduction losses and blocking losses. Blocking losses are usually considered negligible and disregarded. Loss calculations for each device in the module can be readily calculated from data sheet parameters. Most data sheet explicitly list switching losses and conduction losses can be calculated from published I-V plots. However, this estimate disregards real losses seen in applications [59]. The losses experienced in application models accounting for Pulse Width Modulation (PWM) scenarios and duty cycles in actual inverters are more accurate and should be utilized when possible. Models utilizing ABB simulation tools for similarly rated devices in working switches provide more accurate loss parameters. Referring to these models, the losses

calculated for 50 Hz sinusoidal inverter output current, a switching frequency of 250 Hz with a modulation of 0.90, 150 A output current and a DC link voltage of 600 V show total losses in the IGBT and diode are 134 W and 29 W, respectively [60].

The necessary material thermal properties for this assessment are shown in Table 8 below [35, 61]. The material properties reflect silicon diodes (350 μm thick) and IGBTs (140 μm thick) attached to a DBC substrate with an alumina thickness of 0.62 mm and copper thickness of 0.30 mm. The DBC footprint measures 50.8 mm x 50.8 mm. The diodes each measure 10 mm by 10 mm and the IGBT have footprints measuring 13.5 mm x 13.5 mm each.

Table 8: Thermal properties of the materials used for analyzing module footprint.

Material	Thermal Conductivity (W/m.K)
Silicon (device)	149
Alumina 96%	25
Copper	400
Sintered Silver Paste	175

The half-bridge single side model boundary conditions are 1) heat sink boundary condition (10,000 $\text{W}/\text{m}^2\cdot\text{K}$) at the bottom surface of the single sided module and 2) typical air convection on the top surfaces (10 $\text{W}/\text{m}^2\cdot\text{K}$). A colored plot showing the temperature distributions at application temperatures is shown in Figure 10. The simulation reveals insignificant thermal superposition effects at the die positions as indicated by the temperature gradient.

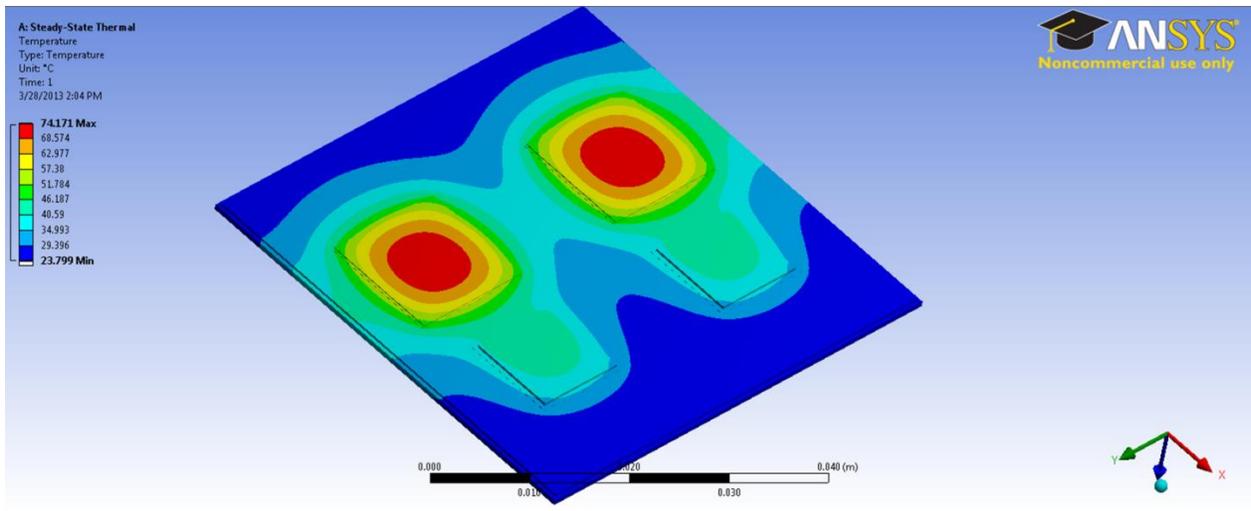


Figure 10: Thermal FEA of proposed power module footprint and device placement revealing negligible thermal superposition effects during application.

2.2.2. Parasitic Contributions

The interconnection parasitics have a large effect on the overall performance of a power module. Parasitic inductance can cause large voltage overshoots that exceed the safe rating of the device and result in permanent damage. The wire bond contribution to parasitic inductance in conventional power modules is significant. Additionally, the wirebond mutual inductance also can result in uneven current distribution causing bonds on the exterior of the die to carry more current than wirebonds on the interior. Even with the contributions from many wirebonds, the bulk of the undesirable inductance, when considering the entire package, comes from the connection tabs. Common parasitic contributions were researched by Xing et al. and are summarized in Table 9. [51] Recent research of a single sided half-bridge module with identical devices utilizing sintered silver die attachment modeled the top side wirebonding inductance

between devices to be approximately 1.36 nH. This results in a total half-bridge loop inductance of 57.23 nH which was found by adding each contribution along the entire path. [62]

Table 9: Estimates of parasitic induction contributions from power module components.

	Wire bond	Emitter Trace	Collector Trace	Terminal Connections
Parasitic Inductance	10-15 nH	5-7 nH	4-5 nH	30-40 nH

Additionally, many have suggested that the double-side design may also be affected by parasitic capacitance. This may be an issue when using a thin dielectric layer between symmetrical overlapping current paths [48].

Many of the parasitic contributions can be minimized through good design practices following recommendations from others. [51] First, attention has been given to creating large flat electrical traces for reduction of parasitic impedance. Where possible, current paths are overlapped in an effort to subtract parasitic inductances when current is reversed. The tabs for outside connections will be reduced in height to minimize inductance based on observations previously noted. DBC substrates already offer the advantage of having an equal and opposite “companion” conductor which acts as a ground plane which helps to lower the overall equivalent inductance. A large variable opening between the top and bottom substrates should allow for possible reduction of parasitic capacitances. A schematic of the design parameters for reduction of parasitics can be seen in Figure 11. The overlapping current paths are marked with arrows. The blue arrows indicate current direction when the IGBT is in the “on” state and red arrows show the current direction when the IGBT is in the “off” state.

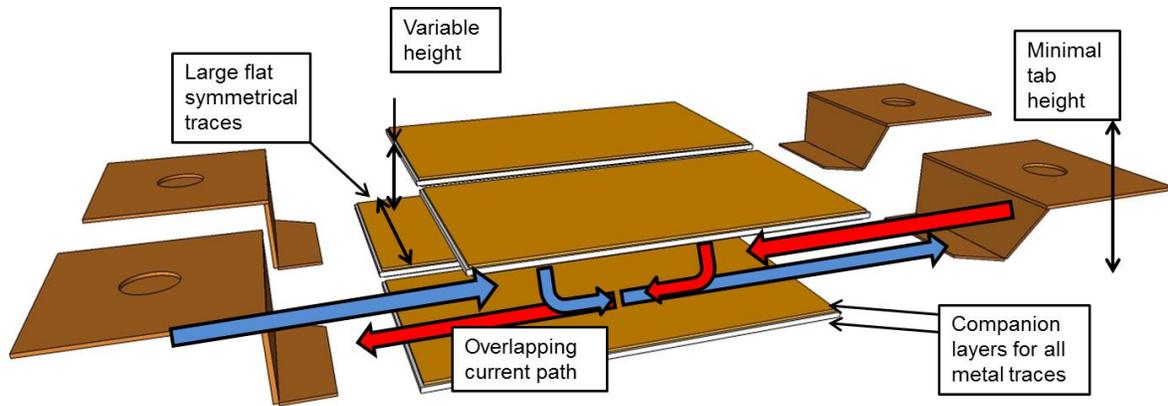


Figure 11: Illustration of proposed electrical layout for minimizing the parasitic contributions from induction, resistance and capacitance.

2.2.3. Double-Side Stress Evaluation

The substrates chosen for the power module were not optimized for thermal benefits. Rather, preference was given first, to price and secondly, to the structural advantages. For this reason, the choice of substrate was a DBC with Al_2O_3 as the isolation layer. The silicon IGBT is the predominant transistor for high power modules so 1200 V 150 A ABB IGBTs were chosen for the switch of the module. The interconnection method throughout the module is nanosilver LTJT. Using the thermal material properties and processing temperature requirements, the thermomechanical stresses could be estimated. The processing temperature, which should account for tooling, must reach 290°C for sintering.

Ideally, for the double-side configuration, the best electrical and thermal performance would be achieved by reduction of the spacing between the top of the die and the bottom of the topmost substrate. However, the spacing needs to be adjusted for various reasons the most important

being the reduction in thermomechanical stresses which arise during the fabrication steps. Additionally, the difference in device thickness requires adjustment to ensure planarity when attaching the top substrate. For electrical characterization before encapsulation, it is necessary to separate the top and bottom traces to inhibit electrical breakdown in air. Additional constraints may be imposed for encapsulation application or internal connections.

During fabrication, the paste will sinter at temperatures between 250°C and 290°C. To accommodate the thermal consumption of our fixturing the higher temperature was utilized. The difference in thermal expansion of the module materials causes a large residual stress when cooled. Much research has already been published on this form of single side attachment and the stress distribution in the die attach layer when cooling from the processing temperature. The maximum stress in the die will appear at the corners of the die [4]. Mechanical properties of the materials considered in our structure are given in Table 10 below.

Table 10: Selected mechanical properties for module materials.

	Young's Modulus (E) (GPa)	Bulk Modulus (K) (GPa)	Shear Modulus (G) (GPa)	Poisson's ratio (ν)	CTE (ppm/K)
Alumina 96%	299.28	172.00	123.67	0.21	8.2
Bulk Silver	78.00	100.00	28.46	0.37	18.9
Copper	134.40	140.00	50.15	0.34	16.5
Sintered Silver ^[35]	40.00	30.30	15.62	0.28	18.9
Silicon	155.79	91.17	64.10	0.22	2.34

The maximum shear stress can be calculated using the simplified equations derived by Suhir. [9, 63]

$$\tau = \Delta\alpha * \Delta T * G_D (\tanh \beta L) / \beta t_D \quad (2)$$

$$\beta = \sqrt{\frac{G_D}{t_D} \left(\frac{1}{E_C t_C} + \frac{1}{E_S t_S} \right)} \quad (3)$$

Where $\Delta\alpha$ is the difference in material thermal expansion between substrate and die. The difference in temperature is ΔT . The maximum chip dimension is L . The variable β is calculated using the shear modulus of the die interconnection alloy (G_D), the Young's Modulus of the substrate and device (E_S and E_C) and their respective thicknesses (t_D , t_S , t_C). Once β approaches a sufficiently large number then the \tanh of β approaches unity and the stress is no longer dependent on device size.

These expressions help to determine the shear strength in the die, but are not sufficient to predict the die failure as a result of shear stresses. The failure is dependent on the device quality and flaw shapes and sizes. For brittle materials like silicon the critical stress is given by:

$$S = Y \frac{K}{\sqrt{a\pi}} \quad (4)$$

Where K represents the fracture toughness of the material ($\text{MPa}\cdot\text{m}^{1/2}$); a represents the length of the flaw and Y is a unitless indication of the flaw location in the device. The variable Y has a

value of 1.3 for an edge flaw, 1.4 for a surface flaw and 1.56 for an embedded flaw. It is commonly thought a good assumption for flaw size from dicing processes is on the order of 3 μm . If the critical die stress is calculated using a flaw size of 3 μm (edge flaw), the largest shear a 13.5 mm x 13.5 mm die can tolerate is 398 MPa. This calculation is based on the material properties from Table 10. Larger shear stresses or flaw sizes will likely result in catastrophic device failure.

An FEA model for calculating shear stress in a large area IGBT attached to a 25.4 mm x 25.4 mm square DBC substrate was constructed. The device was bonded at the fabrication temperature (290°C) and cooled to room temperature. The model reveals a shear stress value of approximately 55 MPa which occurs at the die corner. Based on the previous critical stress calculation, the die should withstand this level of shear stress. This does not consider curvature or peel stresses which are much lower in magnitude.

For completion of the double-side fabrication, another DBC needs to be attached to the top of the devices in a separate pressure sintering step that reaches 290°C. From calculation, the shear stresses accumulated in the extra heating and cooling steps can reach levels that exceed the critical stress for the silicon device. Early experiments by Li et al. using single dies confirmed the stress amplitude. Diodes measuring 10 mm x 10 mm were mounted directly between opposing DBC substrates measuring 16 mm by 16 mm. The device failed by shearing the device along its center plane during cooling from the fabrication temperature. The sintered silver die attachment on both substrates was unaffected [1]. The failure surfaces can be seen in Figure 12.

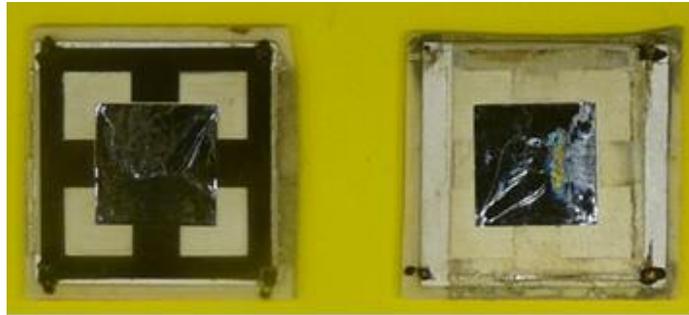


Figure 12: Failure of double-side device by excess shear stress during fabrication temperature changes. [1] (J. Li, G. Q. Lu, and K. Ngo, "Study of Robustness for Double-Sided Module with Rigid Substrates on Both Sides," presented at the Center for Power Electronics Annual Conference, Virginia Tech, Blacksburg VA., 2012) Used under fair use 2014.

It is clear that stresses can exceed the strength of the device and need to be mitigated for successful manufacture. Suhir further suggests that compliant interfaces may not be necessary where normal stresses are concerned, but that shear stress is always decreased by increasing the interface compliance [63]. An FEA model constructed for the instance when another DBC is attached directly to the top of the device in a second fabrication step reveals a shear stress of greater than 500 MPa at the die corner which confirms possible device failure. The materials properties utilized in the model are shown in Table 11.

Others have reported the effects on the die attachment uniformity and thickness for varying stresses seen by the die [64]. These techniques are effective when using solders whose thickness can be changed more readily, but thickness control of sintered silver layers is more difficult. Danfoss, a German manufacturer of power modules, boasts increased reliability with sintered silver thickness as large as 100 micron which they conclude is optimal [39]. For this module, the minimum top area bond thickness must, at least, accommodate the difference in device heights

which is approximately 210 microns, using datasheet thicknesses. The normal sintered silver bond line is a fourth of that before sintering.

Table 11: Selected thermal properties of materials for module assembly [65].

Material	Coefficient of Thermal Expansion (CTE) (ppm/K)	Thermal Conductivity (W/m.K)	Density (kg/m³)
Silicon (device)	2.34	149	2329
Alumina 96%	8.2	25	3800
Copper	16.5	400	8933
Sintered Silver	18.9	175	8500

2.2.4. Stress Reduction in Double-Side Packaging

From earlier sections, it can be seen that solder technology has many limitations. Because the solder is subject to deteriorating diffusion mechanisms like relaxation and creep which occur at relatively low temperatures and stresses, many have researched mitigation of stress in the solder joints. The positive aspect of using a ductile solder as connection to a brittle semiconductor device is the added compliance it provides the working device. If the solder were to be “harder” than it may well transfer stresses to the device leading to catastrophic failure.

Much research has been accumulated on tailoring the interface stresses within a bonded structure exposed to large differences in CTE. It is known that the largest stresses occur at the device edges or corners and with large area devices; the maximum stress level within the interface is practically independent of device size. Sujan et al. presented analytical models for stresses between bonded rigid bodies. These derivations refer to previous work on beam theory and include discussion on both shear stress, in the plane of the die connection, and peeling stress,

which is oriented normal to the die. Derivations by Sujana et al. confirmed that shear stress is indeed a maximum at the chip edges and decreases in a parabolic fashion moving towards the center of the die. Peeling stresses were also found to be the largest at the edges of the die. Comparisons were made with calculated stresses using a ΔT of 120°C and bond materials with different compliance properties (axial and shear) and shear modulus. The compliant layer had properties similar to gold-tin solders. It was found that the compliant layer reduced the peeling stress and the shear stress by more than 30%. Even better, both peeling and shear stress were further reduced by increasing the thickness of the bond layer. Doubling the thickness had dramatic reductions in stress levels at the free end of the die [66].

It is clear the stress levels can be altered by increasing the compliance, bond line thickness or a combination of both. Experimental evidence on the bond line thickness effect on crack growth was also modeled and studied. The finite element modeling of the solder material, defined as an elasto-plastic body, revealed that increasing solder thickness to 200 μm revealed large decreases in equivalent strain at the device edge. Continued height changes revealed little or no additional benefits. Experimental verification of the model found that crack growth rate for thermally cycled samples (-50°C to 125°C) followed a similar trend with increased crack growth rate in thinner bond lines. Although the model predicted little to no gains in stress relief for bond lines thicker than 200 μm , the crack growth for the 320 μm bond line was small enough to be negligible. Additionally, the same study mentioned the difficulty in increased bond thickness while maintaining uniformity. Uniform increases in thickness are essential to reaping the benefits of stress reduction. [64]

Based on previous solder research, it is clear that large and more compliant bond lines reduce both the shear and peeling stresses of the device interconnection. Based on previous calculations, a double-side package will require stress remediation using some combination of increased height and compliance. The compliance of the sintered silver cannot be changed without also deteriorating the benefits of reliability, and electrical and thermal conductivity. Alterations to the bond line thickness are difficult as well. Some have experimented with sintered silver bond line thicknesses of 100 μm and reported increased reliability and reduced crack growth. However, increases in bond line thickness also reduce the shear strength of the sintered silver attachment.

The stress reduction solution addressed in this report is the creation, through mechanical means, of a more compliant interface with variable height. Additionally, the material selected is compatible with sintered silver attachment, possesses a low modulus and exhibits high thermal and electrical conductivity.

2.3. Modeling and Design of Stress Reducing Interface

Regardless of the type of finite element analysis (FEA) modeling, each FEA model construction can be divided into six steps:

- 1) Construction of a 3D scale model of the system.
- 2) Selection of meshing (resolution).
- 3) Material and material property selection.

- 4) Establish reasonable boundary conditions, e.g., thermal loads, convection surfaces, supports.
- 5) Solve models.
- 6) Analyze results.

These steps are used for each of the finite element models in this document. The thermomechanical modeling utilizes the ANSYS® Workbench™ software suite. Induction models will be constructed with the same general outline Ansys® Q3D Extractor®. Finally, thermal spectrometry was modeled using a FloTherm® software suite distributed by Mentor Graphics® [67].

2.3.1. Thermal Modeling

When constructing the geometry for the FEA analysis of the full module, it is not necessary to construct the entire module. The geometry can be simplified using the symmetry of the module to save analysis time and increase resolution. A 3D model was constructed for one double-side IGBT device attached using a plurality of shaped tubes. The device attachment, tube interconnects and tubes are drawn to match the dimensions of the actual module. The tube height in this model is fixed at 1 mm tall with tubing wall thickness of 0.2 mm and a tube face width of 2 mm. The constraints on the number of tubes and their dimensions will be discussed in detail in the following section. For this model, the elliptically shaped tubes are bonded between the copper on the DBC substrate and the device using a 35 micron layer of sintered silver assumed to be 85 % dense. The die is attached to the bottom substrate with the same

sintered silver thickness. The silver layer, being sintered rather than reflowed, does not allow wetting of curved surfaces. For this reason, the silver tubes in the model and in actual manufacturing must possess flattened areas to increase bonding strength. The bonding flats on the tubes in this model are 1 mm wide and the tubing length is 10 mm. This allows for a 10 mm² bonding area for each tube. Four tubes 2 mm wide are centered on the 13.5 mm die. The electrical pad on the ABB IGBT does not cover the entire surface and to insure the silver does not reach the edge guard ring, a 10 mm by 10 mm square of sintered silver is centered in the electrical pad for attachment of the tubes. The top and bottom substrates have dimensions of 25.4 mm by 25.4 mm which is sufficiently large enough to avoid edge effects.

For the thermal model, the thermal properties needed to be linked to the material in the model. The material thermal properties used for the thermal model are shown in Table 12.

Table 12: Material properties of module materials used for the FEA thermal analysis [65].

	Density (kg/m³)	Specific Heat (J/kg.C)	Thermal Conductivity (W/m.C)	CTE (ppm/C)
Alumina 96% ^[68]	3800	880	25	8.2
Bulk Silver	10490	233	429	18.9
Copper	8933	385	400	16.5
Sintered Silver ^[35]	8500	233	175	18.9
Silicon	2329	710	149	2.3
Encapsulation ^[69]	1993	1300	0.18	22.8

This model seeks to establish the junction temperature of the device with a thermal load. The thermal load for this experiment is a heat flow condition of 100 W emanating from the device surface. A convection condition of 10000 W/m².K is placed on the bottom of the package to emulate a force cooled heat sinking condition. The top is open to air and has a natural

convection condition of $100 \text{ W/m}^2\cdot\text{K}$ on all exposed surfaces. For ease of tabulating internal package temperatures vertical path geometry was defined in the model. The calculated temperature values along the established path can be plotted to reveal the internal temperature profile. Two paths are necessary with the tube structure; one path through the bulk of the tube and another reflecting the opening in the tube. The defined paths can be seen in Figure 13.

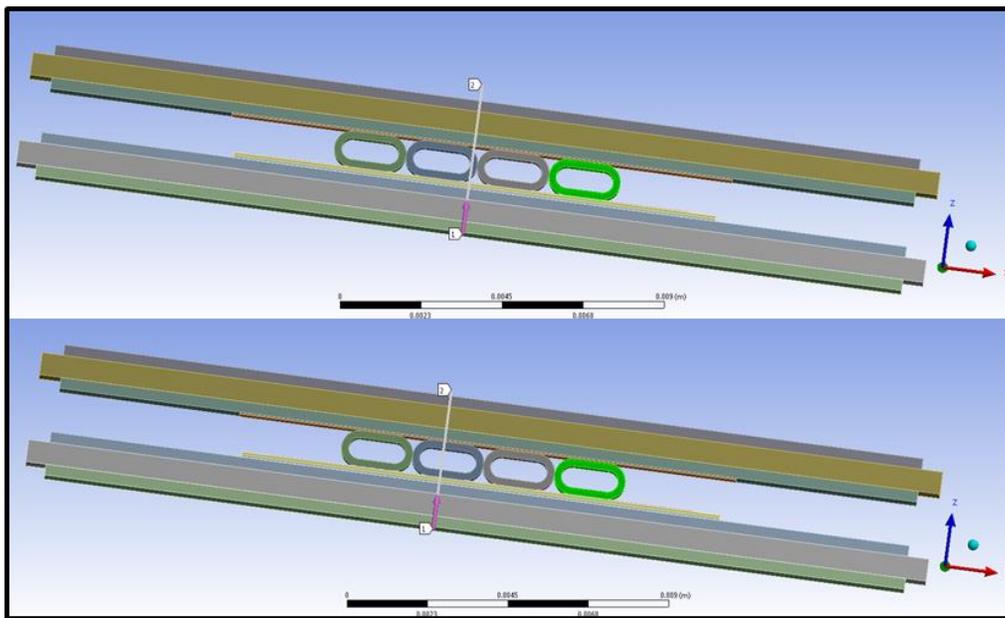


Figure 13: Illustration of constructed paths for plotting the heat flow through the wall of the tube (top) and the heat flow through the opening in the tube (bottom).

The device is assigned 100 W of output power evenly across the device surface. The steady state package temperature distribution is shown in the plot of Figure 14. The device junction temperature reaches a maximum temperature of 58.14°C .

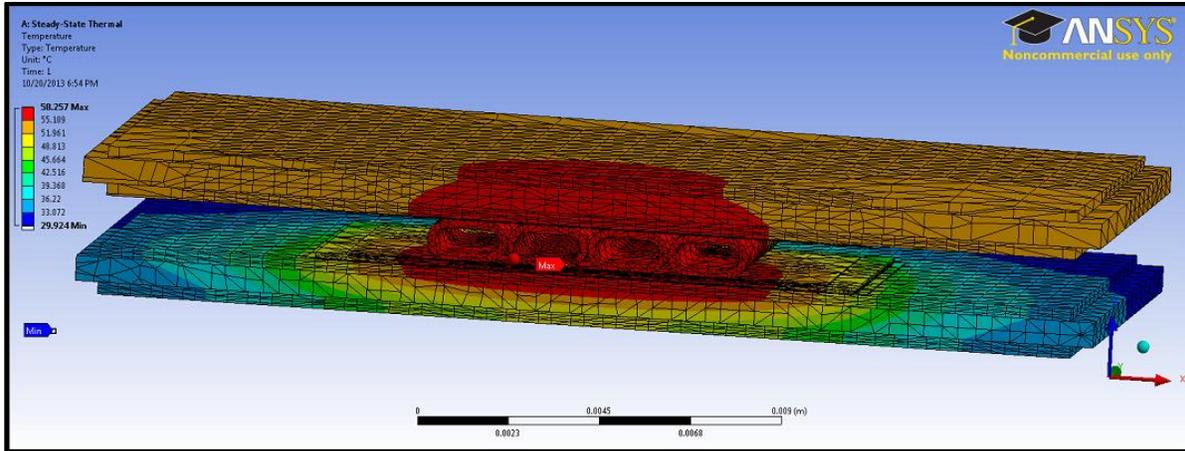


Figure 14: Colored thermal distribution plot output from FEA thermal simulation to determine the steady state thermal distribution using 100W applied to the device.

For comparison, single side packages with identical die connection and die size were also modeled and simulated with identical thermal boundary conditions. One model was constructed with the device and a row of 2 mil aluminum wirebonds attached to the top surface. The wirebonds are added to assess their contribution to the surface temperature of the die. An additional model was constructed with silver elliptically shaped tubes attached to the top, but without an additional top substrate.

All three models had similar paths added to the construction geometry. The paths can be compared up to the junction temperature of the device which is indicated by the highlighted rectangular region in Figure 15. The temperatures after the junction differ greatly because of the differences in geometry above the device. A comparison plot of the thermal paths for all three models is shown in the graph of Figure 15. The temperature at the device is lowest for the double-side package. The wirebond junction is approximately 4 °C greater for the same conditions for the entire path which translates to higher case temperatures at the heat sink bottom.

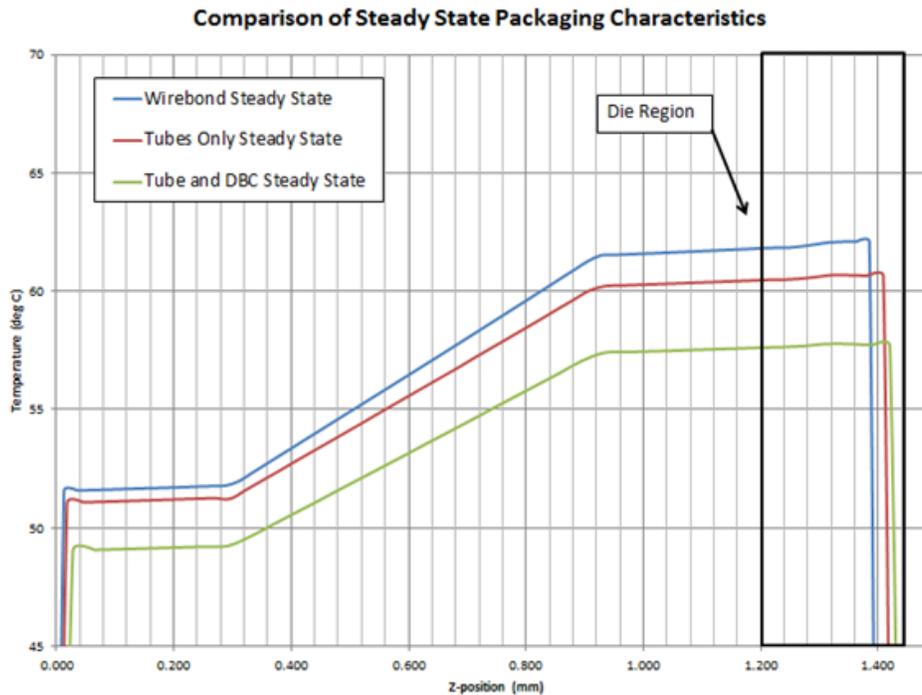


Figure 15: Comparison of steady state package temperature profile for each configuration. The heat path begins on the left at the bottom of the substrate (z-position = 0). The device junction temperatures are indicated with the black rectangle.

In actual devices, encapsulation will be added to the interior of the module. The encapsulation is a poor thermal conductor and it is expected to show little to no positive contributions to heat dissipation.

To further model the benefits of double-side cooling and compare to empirical steady state thermal resistance measurements in Chapter 4, the model was performed again with constraints closely matching the experimental testing. For thermal resistance testing, the module will require one or both sides maintain a fixed temperature and a minimum of added convection will be used ($100 \text{ W/m}^2\cdot\text{K}$) on exposed surfaces. The heat source from the device will be 150 W. Both the encapsulated and unencapsulated modules were modeled using the same geometry path

profiles which are centered on the model and extends from the bottom of the bottom substrate to the top of the top substrate. This path, because it is centered, will align with the junction of the innermost tubes. Three models were performed for each state; bottom cooling, top cooling and cooling on both surfaces.

A comparison plot of each testing configuration for the unencapsulated model is shown in Figure 16. The distance from the bottom module case is plotted on the x-axis and the y-axis represents the temperature increase above room temperature (25°C). The device junction is marked with an additional blue line for easy reference. The discontinuities in temperature data above the device junction are due to the two openings where the innermost tubes meet.

The plot reveals cooling both sides at the same time results in the smallest rise in device junction temperature. The bottom side cooling is slightly less effective at reducing junction temperature and top cooling is least effective. This is not surprising based on the asymmetrical nature of the interface and the relatively large thermal resistance of the top connection when compared to the bottom connection.

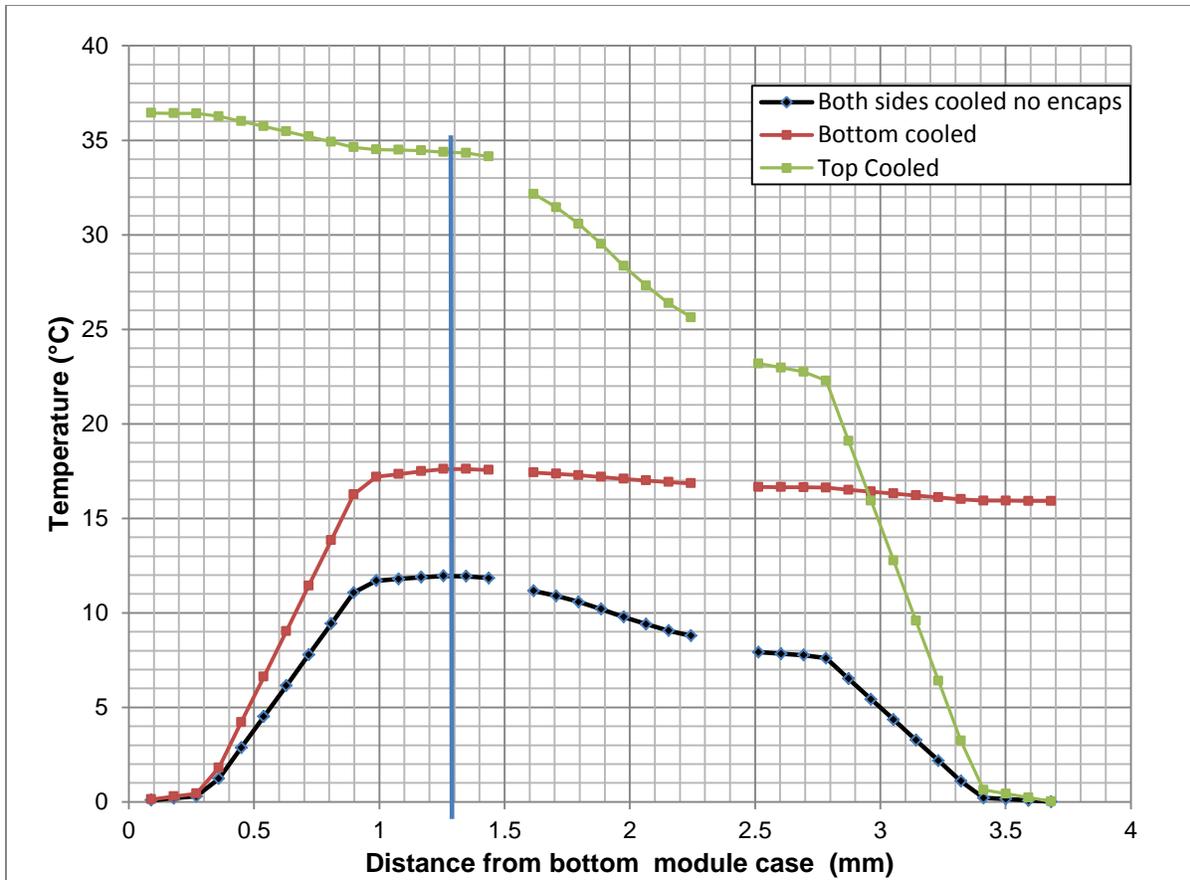


Figure 16: Modeled single dimension thermal profiles for each of three unencapsulated module cooling configurations; top-cooled, bottom-cooled and top plus bottom cooled.

The path chosen for temperature probing was directly in the center of the device because most thermal model relies only on one dimensional heat flow assumptions. This is a good assumption when considering stacked structures of homogenous materials. Based on the thermal distribution for each of the three cooling scenarios, a three dimensional heat flow model is required when analyzing this structure. The colored thermal distribution plots showing the three-dimensional heat flow for each of the three conditions are shown in Figure 17 below.

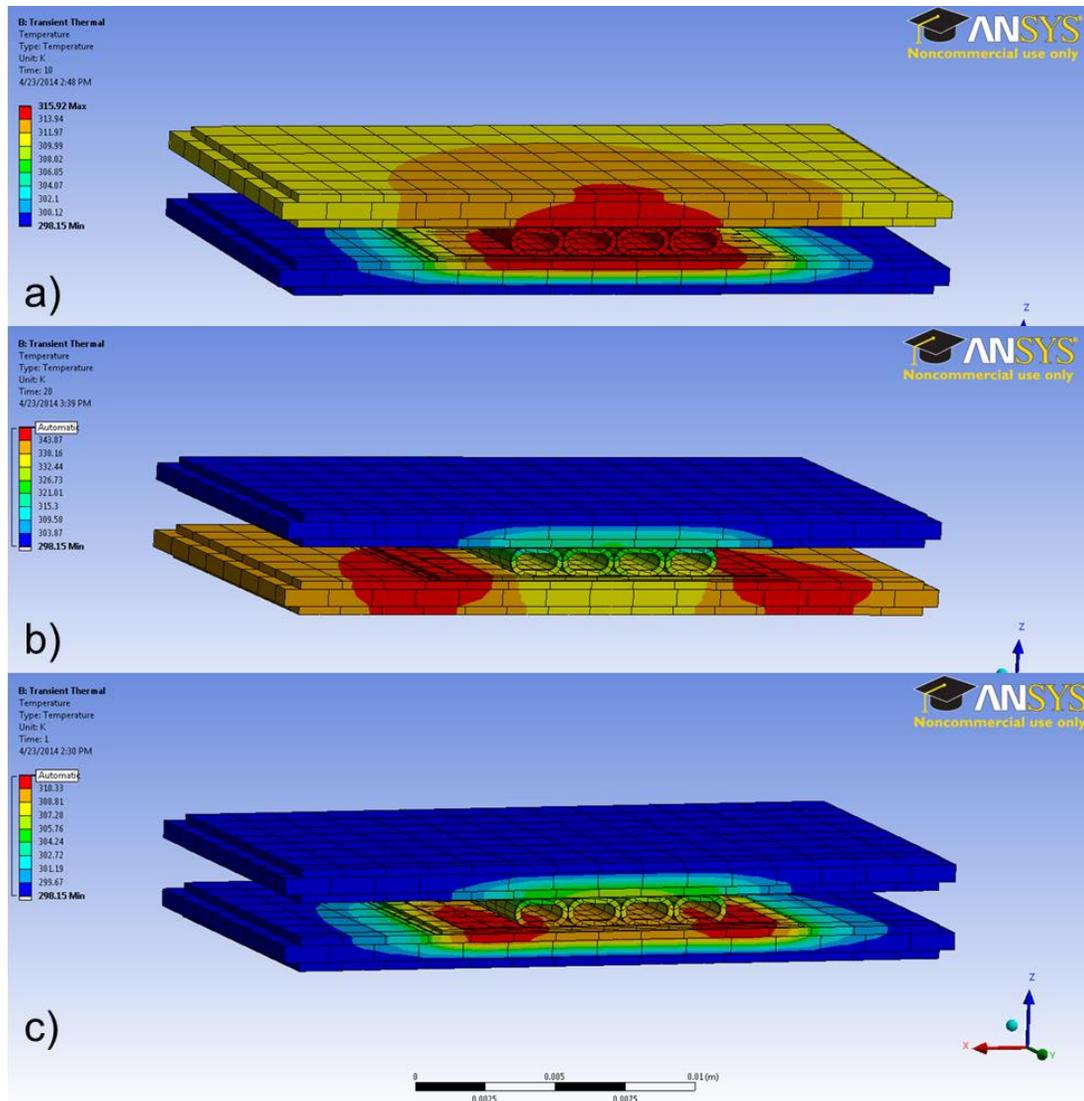


Figure 17: Modeled three-dimensional thermal distributions for each of three cooling configurations; a) bottom-cooled, b) top-cooled and c) top plus bottom cooled.

Figure 17(a) shows the thermal distribution for the case in which the bottom of the device is force cooled. The excess heat moves directly to the top substrate which acts a heat sink. A one dimensional model would accurately predict this response. Figure 17 (b) and (c) reveal heat flows predominately in the x and y directions which offer less thermal resistance than the z-direction in these cooling scenarios. This heat spreading effect leads to disagreement with the conventional one-dimensional heat flow models because the junction is at a lower temperature in

the center of the assembly than is expected. From the above images, it is obvious that the tubes significantly lower the junction temperature of the die, but only where the tubes are attached. The areas of the tube that are not covered show increased temperature which reinforces the need to optimize the coverage of the device surface with tubes.

The same three testing configurations were modeled for the encapsulated module as well. A plot of the temperature profile of each configuration for the encapsulated model is shown in Figure 18. The device junction is again marked with a blue line for reference. The dips in the cooling curve correspond to the same tube openings, but because the encapsulation has filled the voids, there are now temperature values rather than discontinuities.

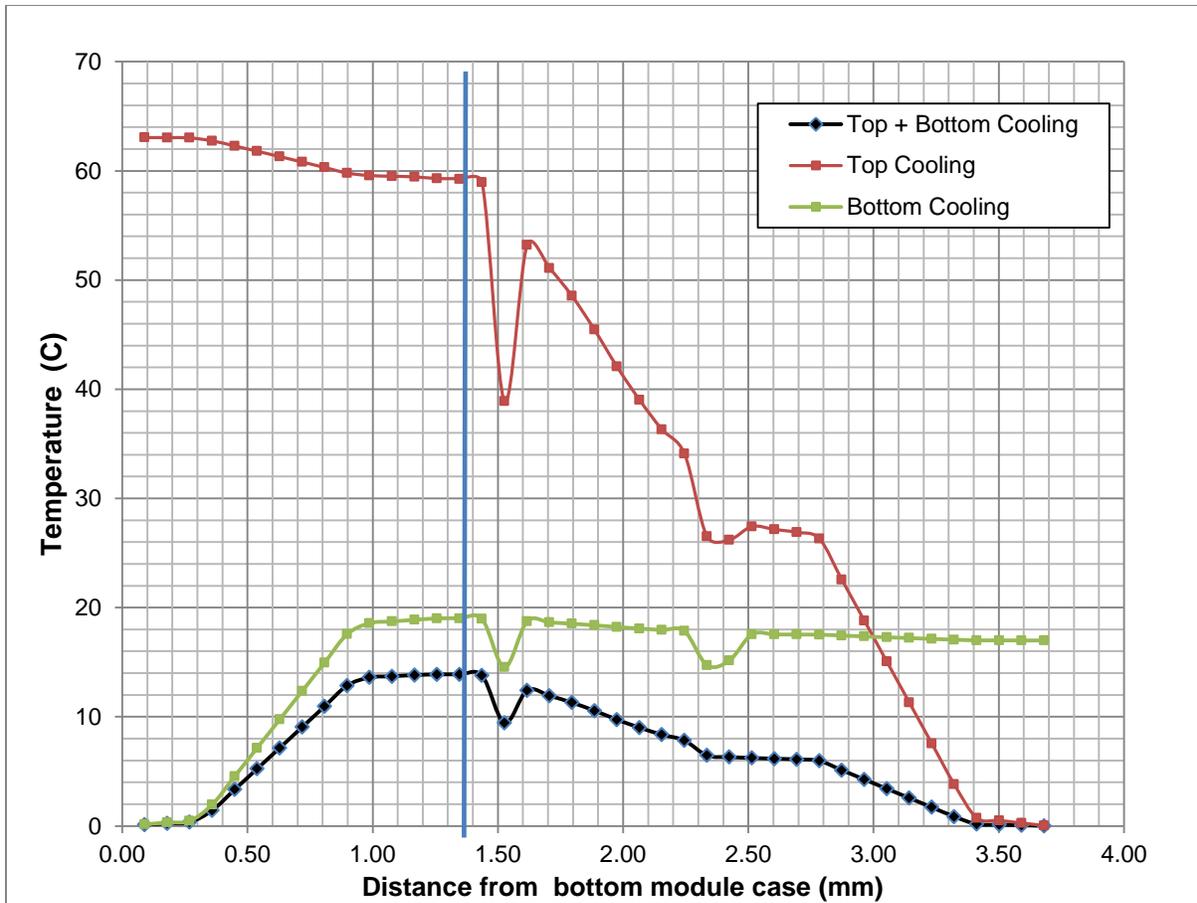


Figure 18: Modeled single dimension thermal profiles for each of three encapsulated module cooling configurations; top-cooled, bottom-cooled and top plus bottom cooled.

The encapsulated module shows a similar trend but with different values owing to the small increase in thermal conductivity of the encapsulant relative to air. The configuration for having both sides cooled remains the optimum condition. As with the unencapsulated module, it is also necessary to view the three-dimensional thermal distributions to better understand how the compliant layer affects heat spreading. The thermal distributions for the three configurations with encapsulation are shown in Figure 19. The module has a slice plane included to better reveal the internal heat spreading.

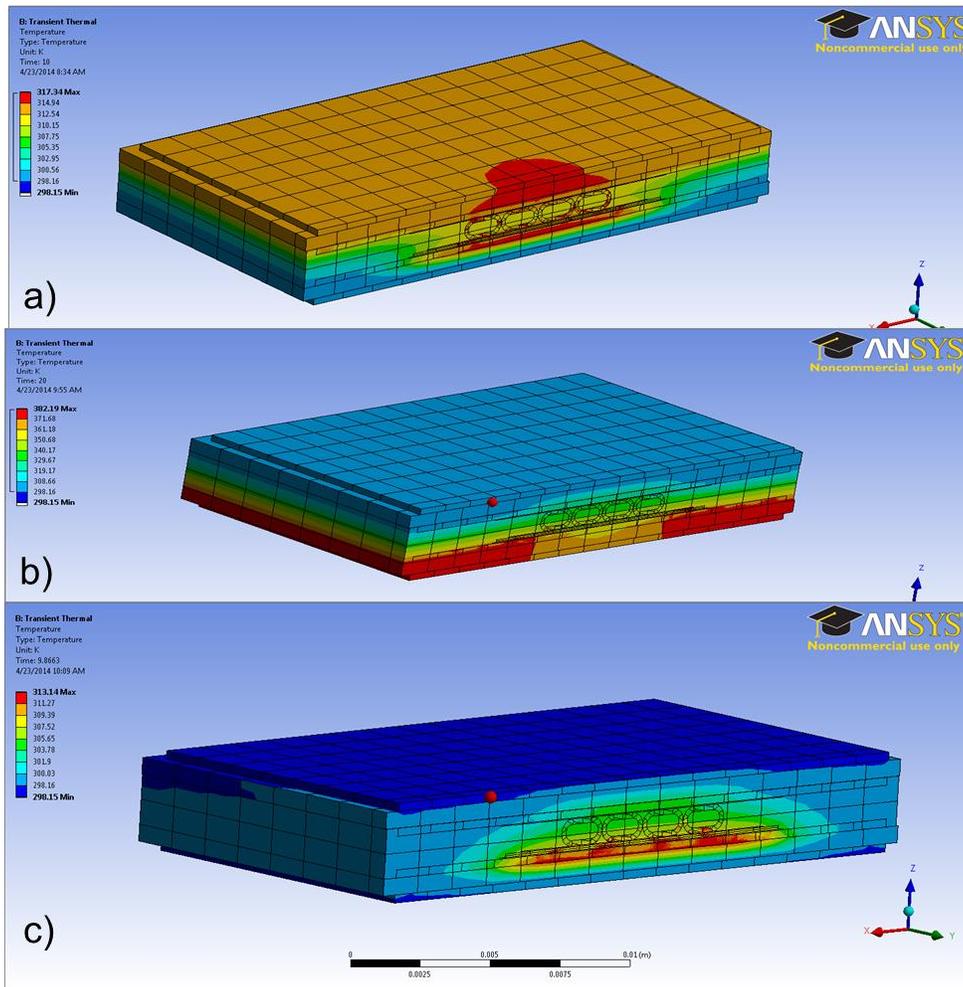


Figure 19: Modeled three-dimensional thermal distributions for each of three encapsulated cooling configurations; a) bottom-cooled, b) top-cooled and c) top plus bottom cooled.

In the encapsulated module model cooling from the top and from both sides more closely adheres to the conventional one dimensional heat flow assumption. However, when the top is cooled (Figure 19b), a large amount of heat has again spread to the edges of the device. This model helps to understand the tube contribution to the heat flow and more importantly, the heat flow direction. To improve the thermal distribution and lower the junction temperature for the entire device, the tube structure should be bonded over the entire surface area of the die.

A summary of these modeling results are shown in Table 13 below. The optimum condition is, of course, cooling from both sides, regardless of whether encapsulation is used. The encapsulation was found to inhibit heat spreading away from the die junction in the case of top side cooling which is most likely due to both the low thermal conductivity of the encapsulation and the absence of convection cooling. This encapsulated configuration also shows the largest increase in junction temperature.

Table 13: Summary of modeled thermal characteristics for modules in different cooling configurations.

	Without Encapsulation			With Encapsulation		
	Max Junction Temperature (°C)	ΔT -junction to cooled case (°C)	ΔT /Applied Power (°C/W)	Max Junction Temperature (°C)	ΔT -junction to cooled case (°C)	ΔT /Applied Power (°C/W)
Top Cooling	59.14	34.14	0.2276	84.30	59.30	0.3930
Bottom Cooling	42.56	17.56	0.1171	44.01	19.01	0.1264
Top Bottom Cooling +	36.84	11.84	0.0789	38.98	13.88	0.0918

A common method of assessing the thermal benefits of the device is to calculate the thermal resistance. This is normally a very straightforward calculation when the rise in temperature from the case of the module to the device junction is measured and divided by the power required. In the case of the double-side structure, two cases exist so two thermal resistance values require calculation. Using a single dimension heat flow assumption these two thermal resistance values could be combined using a parallel electrical resistor analogy to predict the thermal resistance when cooling was applied to both sides. An illustration of how these resistance are arranged in the module can be seen in Figure 20

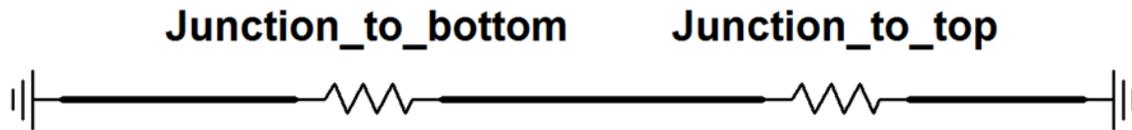


Figure 20: Illustration of using the junction to bottom case and junction to top case thermal resistance values to calculate the thermal resistance of the instance when both the top and bottom substrates are force cooled.

Using the parallel resistance calculation with the values of the unencapsulated top and bottom cooling scenarios from Table 13 above, a double-side cooled thermal resistance is found to be 0.0773 K/W which is lower than the measured thermal resistance of 0.0789. The discrepancy is due to the thermal spread in the x and y directions.

These results and a more in-depth explanation of the one dimensional heat flow model will be discussed further in the experimental thermal characterization section of Chapter 4.

2.3.2. Parametric Study of Thermal Conductivity

The minimum tubing height was initially constrained by the need to accommodate dielectric breakdown in air during high voltage testing which is commonly accepted to be 3000 V per millimeter. With the possible need to test breakdown voltages to 1200 V, the minimum opening height had to be at least 0.40 mm. Yet, actual modules when fabricated require one set of wirebonds to travel between substrates to the gate and emitter pads. These wirebonds will be used to switch the IGBT and require a substrate spacing of at least 1 mm. With the final tube

height fixed, the geometry of the tube was adjusted to provide large flattened areas on the top and bottom specifically for using sintered silver processing. For a parametric study of the thermal conductivity of the tubing interface, a tube height of 1 mm was initially inspected. Considering the thermal conductivity of the interface will approach its maximum for a plurality of silver solids and a minimum for an infinitely thin walled silver tube, the conductivity relationship can be simply represented by inspection of only one tube in the array. Using a singular tube of a fixed length, the thermal conductivity of that tube can be represented by the reduction in silver volume over the total available silver volume or bulk silver. Because the length scales are identical, the relationship can be further simplified using the area fraction and shown in the equation,

$$\kappa_{interface} = (A_f * \kappa_{silver}) + ((1 - A_f) * \kappa_{air}) \quad (5)$$

Where A_f represents the fraction of the interface containing silver and the remaining area is assumed to contain air which has a room temperature thermal conductivity of approximately 0.026 W/m.K.

$$A_f = \left(\frac{l * h}{(l - 2t) * (h - 2t)} \right) / 100 \quad (6)$$

Where t is the wall thickness, l is the length of the tube and h represents overall tubing height. The elliptical tubing shape more closely resembles a rectangle than a pure ellipse so the area calculation is simplified to reflect only rectangular geometry. As the wall thickness approaches

twice of the height, the thermal conductivity approaches that of bulk silver which is 490 W/m.K.

A plot of this relationship can be seen in Figure 21.

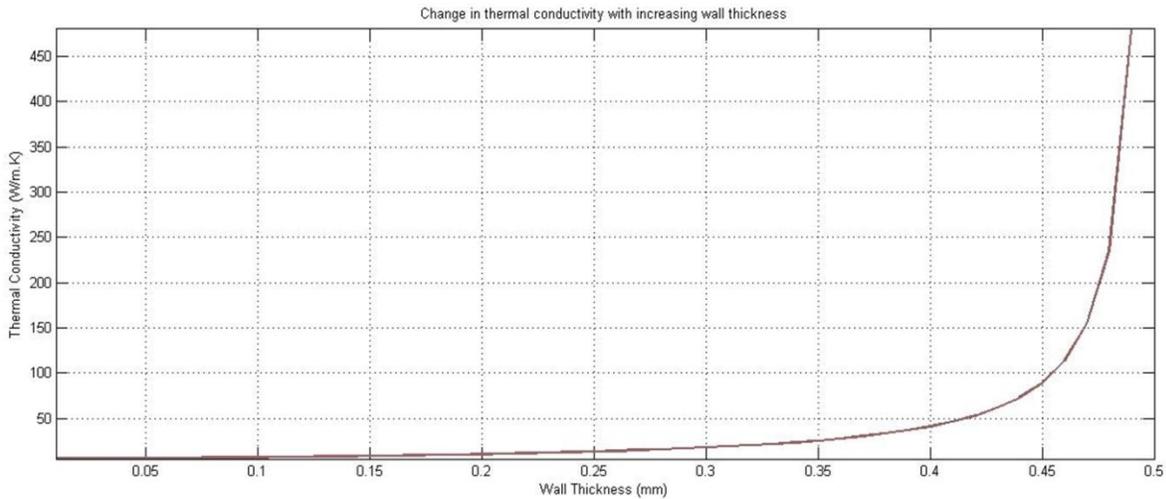


Figure 21: Change in thermal conductivity of tubing interface as a function of changing wall thickness for a 1 mm tubing height where 0.5 mm wall thickness is a solid round of bulk silver.

Changes in interface height were not necessary because this relationship is independent of height assuming aspect ratio of the tubes remains fixed. In each instance changes to the wall thickness, regardless of height, will yield a maximum at twice the wall thickness (solid) after rising exponentially.

2.3.3. Thermomechanical

The geometry of the thermomechanical model is the same as the previous experiment on thermal transfer. Additional material properties will be required, but the dimensions and materials are identical. The material properties chosen for the module components are outlined in Table 14 .

Although the sintered silver layer properties are sometimes compared to bulk silver properties, the density of the sintered layer plays a large role in the material properties. This model assumes the sintered silver has a density equal to 85% of bulk silver. Material properties for sintered silver have been reported by multiple references. The modulus values listed for 85% dense sintered silver are from an Oak Ridge National Laboratory (ORNL) study on the properties of bulk sintered silver. [35]

Table 14: Mechanical properties for materials used in developing a structural FEA model.

	Young's Modulus (E) (GPa)	Bulk Modulus (K) (GPa)	Shear Modulus (G) (GPa)	Poisson's ratio (ν)
Alumina 96%	299.28	172.00	123.67	0.21
Bulk Silver	78.00	100.00	28.46	0.37
Copper	134.40	140.00	50.15	0.34
Sintered Silver ^[35]	18.00	30.30	15.62	0.28
Silicon	155.79	91.17	64.10	0.2152
Encapsulation ^[69]	0.59	0.702	0.217	0.36

Also, the effect of temperature on sintered silver modulus values has also been previously researched. These values are shown in Table 15 and will be tabulated at these points and used as continuous relationship in the FEA model. [70, 71]

Table 15: The sintered silver temperature dependent Young's Modulus relationship used in FEA model construction.([70] K. L. Xiao, Thomas; Wang, Tao; Chen, Gang; Ngo, Khai; Lu, GuoQuan, "Creep Behavior of Sintered Nanosilver Paste" unpublished.) Used under fair use, 2014.

Temperature	Young's Modulus (E) (GPa)
25°C	18
50°C	16
100°C	11
150°C	5
200°C	3

For each model the contact surfaces are assumed to be bonded. For determining the package stresses after fabrication it is necessary to establish a zero stress state in the model materials at the processing temperature of 290°C. For modeling the thermomechanical stresses in the module, a frictionless support was added to the top and bottom of the structure. No convection conditions were stipulated. The mesh resolution in the FEA can be controlled in a coarse fashion by choosing high, medium or low resolution. Additional resolution can be adjusted as needed by defining regions of interest for finer mesh. The mesh shape in this model uses adaptive controls to optimize the surface of interest. In this model the internal interfaces had a very fine mesh and the outer substrates were assigned a coarse mesh. In addition to the tabulated encapsulation mechanical properties in Table 14, the experimentally determined CTE value of 22.8 ppm was used and assumed to be linear until the glass transition temperature of 175°C [72].

The first solution is found by application of a thermal load applied to all bodies simultaneously forcing them all to a temperature of 25°C from 290°C. A color enhanced map of the equivalent von Mises stress distribution is shown in Figure 22 with exaggerated deformation showing the stress relief response. The largest stresses occur in the wall of the silver tube structure. The maximum equivalent von Mises stress in the tubes is calculated to be approximately 1.585 GPa. The equivalent von Mises stress in the sintered silver connection below the tubes is calculated to be approximately 0.273 GPa. The sintered silver directly above the tubes experience a von Mises stress of only 0.367 GPa. The shear stress on the device underneath the tube flat is approximately 1 MPa. The shear stress between tube flats is a negative 0.52 MPa.

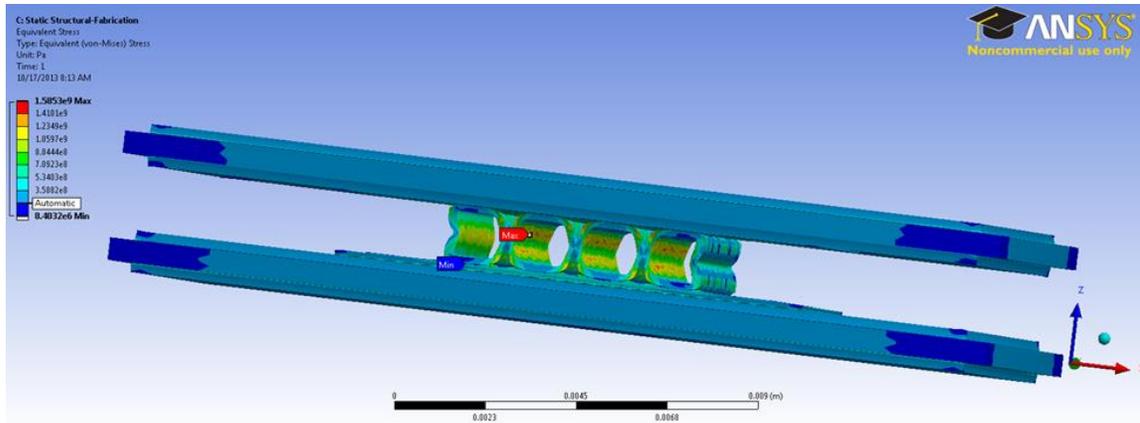


Figure 22: Colored plot revealing equivalent von Mises stress distribution when the entire unencapsulated module cools from the fabrication temperature.

By comparison, a FEA model utilizing the same temperature profile for the double-side package that does not employ the compliant tube structure was found to have a device shear value of 491 MPa at the center and 517 MPa at the corner. This is approximately 500 times that of the shear values in the compliant package. The equivalent von Mises stress for the device in the noncompliant package reached a maximum of 1.06 GPa. Additionally, this maximum stress value was on the device whereas the maximum von Mises stress in the compliant package exists away from the device in the walls of the tube structure.

This same sample was then reheated to 250°C. The goal of reheating is to view the net stress state at high application temperatures after consideration of the residual stress from fabrication. This model uses the same frictionless supports on the top and bottom and as before, no convection conditions are stipulated. The calculated equivalent von Mises stress for the package is shown in the color plot of Figure 23. The maximum von Mises stress is found between the top tube attachment and the top substrate. The von Mises stress on the device underneath the tube

flats is calculated to be 0.378 GPa. The shear stress on the device in the region underneath the tube flats is negative 2.436 MPa. The shear stress between tube flats is a positive 1.04 MPa.

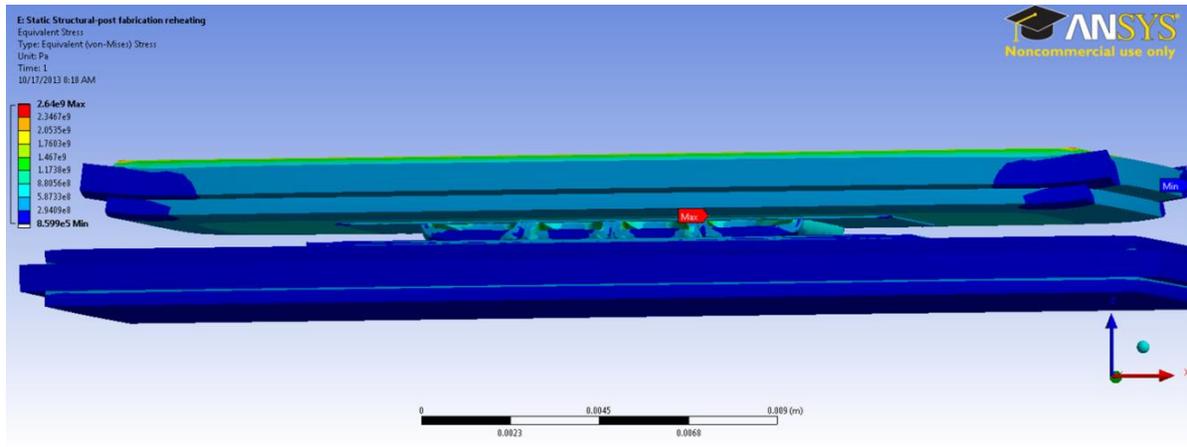


Figure 23: Stress distribution plot showing the calculated equivalent Von Mises stress distribution in an unencapsulated module reheated after fabrication.

Based on the deformation in the tube layer from the first solution, the deformation upon reheating is expected. The interior structure will attempt to shrink in size because the CTE mismatch between the bonded tube and substrate causes decreased curvature in the silver tube.

Functional devices will require an underfill/encapsulation within the package. The encapsulation will completely surround the tubular structure. The encapsulation which will ultimately be used for fabrication of the functional module cures at approximately 150°C and has a glass transition temperature of approximately 175°C. It is very important to note that this encapsulation is not physically compatible with these modeled temperatures, but in an effort to compare the stress levels when the tube curvature is restricted, the model was performed anyway. To model the effect of added encapsulation restricting the tube curvature, the same post-fabrication cooling step was applied to the geometry with added encapsulation. The equivalent von Mises stress of

the package can be seen in Figure 24. The interior details are hidden but the intended deformation is clear. The same expansion of the interface occurs even with encapsulation, the stress in the tube structure is calculated at 0.804 GPa which is approximately half that of the von Mises stress without encapsulation. The equivalent von Mises stress in the encapsulation is 1.783 MPa. The von Mises Stress on the device beneath the tubing flats is calculated to be 0.49 GPa. And the shear stress on the device in the region of the tubing flats is further reduced to 0.36 MPa.

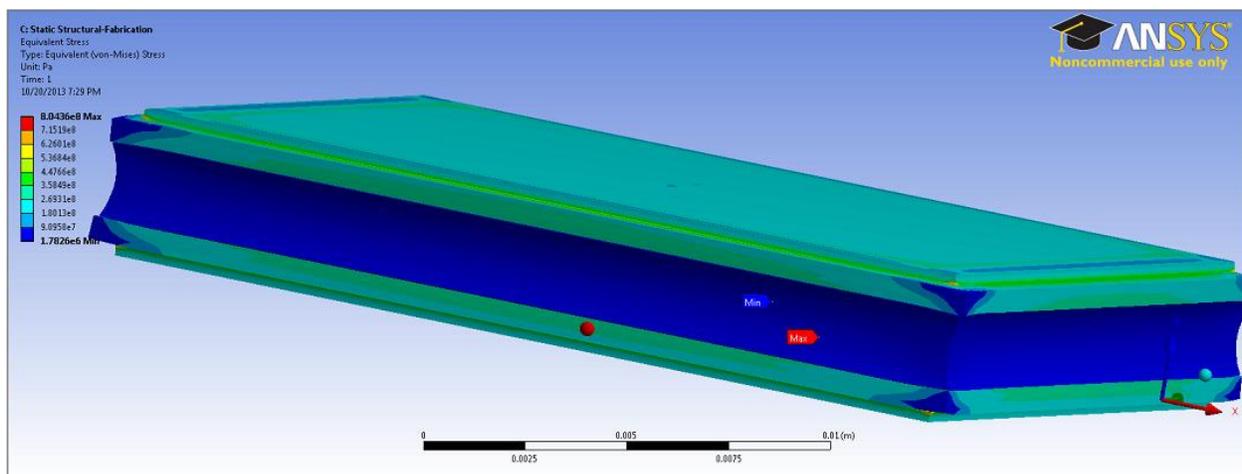


Figure 24: Stress distribution plot showing the calculated equivalent von Mises stress distribution in an encapsulated module reheated after fabrication.

Upon reheating to 250°C and observing the stress state (including the post fabrication thermomechanical stress) with encapsulation, it can be seen (Figure 25) that the maximum stress actually occurs on the outer substrate of the package. The stress at the tube junction is

approximately equal to the equivalent von Mises stress in the encapsulation which is calculated to be only 2.099 MPa.

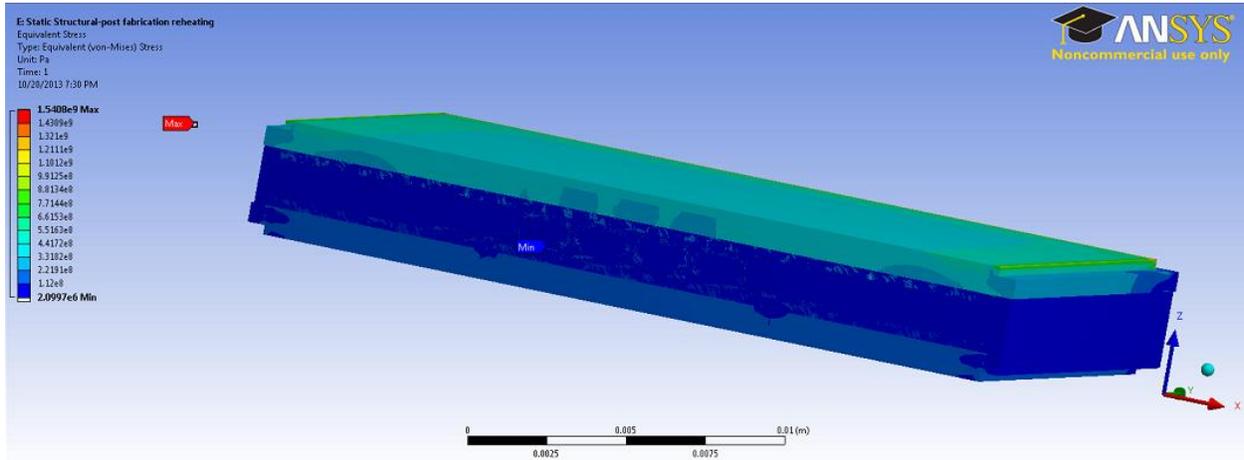


Figure 25: Stress distribution plot showing the calculated equivalent von Mises stress distribution in an unencapsulated module reheated after fabrication.

From this, it can be seen that the encapsulation hinders the thermal dissipation, but plays a large role in decreasing the stress of the tubing and tube-sintered silver interface.

2.3.4. Parametric Study of Thermomechanical Design

After the analysis of the compliant interface, it is clear that an open tube structure benefits the entire package by reducing the device junction stresses. It is unclear that this structure is optimized for the package stresses and the heat dissipation. The results of the previous FEA models show the ability of the tube walls to alter curvature when exposed to CTE mismatch stresses. This curvature allows for a decrease in stresses as seen from the device. The effects of increasing tubing wall thickness or height on the stress mechanisms is not obvious from the

previous study. For package optimization, it is necessary to consider the tubing parameters and their effect on the level of stress relief.

The minimum tubing height, as explained in the thermal modeling section, was initially constrained by the need to accommodate dielectric breakdown in air during high voltage testing. Dielectric breakdown in air occurs at 3000 V per millimeter. With the possible need to test breakdown voltages to 1200 V, the minimum opening height had to be at least 0.40 mm. Yet, actual modules when fabricated require one set of wirebonds to travel between substrates to the gate and emitter pads. These wirebonds will be used to switch the IGBT and require an opening between substrates of approximately 1 mm. With the increased substrate spacing, the high viscosity encapsulation could also easily be added. Additionally, the device junction can be accessed with thermocouples when required. Using 1 mm as the recommended opening height a search of commercially available high purity silver tubes was performed. The available candidates narrowed the available aspect ratios considerably. Of the tubing candidates, several were pressed to determine the optimum aspect ratio for use in modeling. The goal of pressing the tube was to provide large flattened areas on the top and bottom specifically for using sintered silver processing while maintaining some wall curvature for stress mitigation. The specifics of the fabrication process will be discussed in detail in Chapter 3.

To aid in designing the optimum tubing interface, an additional FEA model was employed. The model was used to characterizing the equivalent von Mises stress on the device with variations in interface height and wall thickness. The model was necessary because the tube attachment isn't uniform across the entire device connection. This non-uniformity can be clearly seen in the

model screenshot in Figure 26. It is difficult to establish one clear analytical expression for the complex von Mises stress state along the entire device surface. To best present a complete picture of the stress state on the device, the stress will require measurement at two different points; beneath and between the tubes. Figure 26 shows the two areas of interest and defines the quantities that will be adjusted for modeling; the wall thickness (t), the interface height (h) and the length of the tubing face (l).

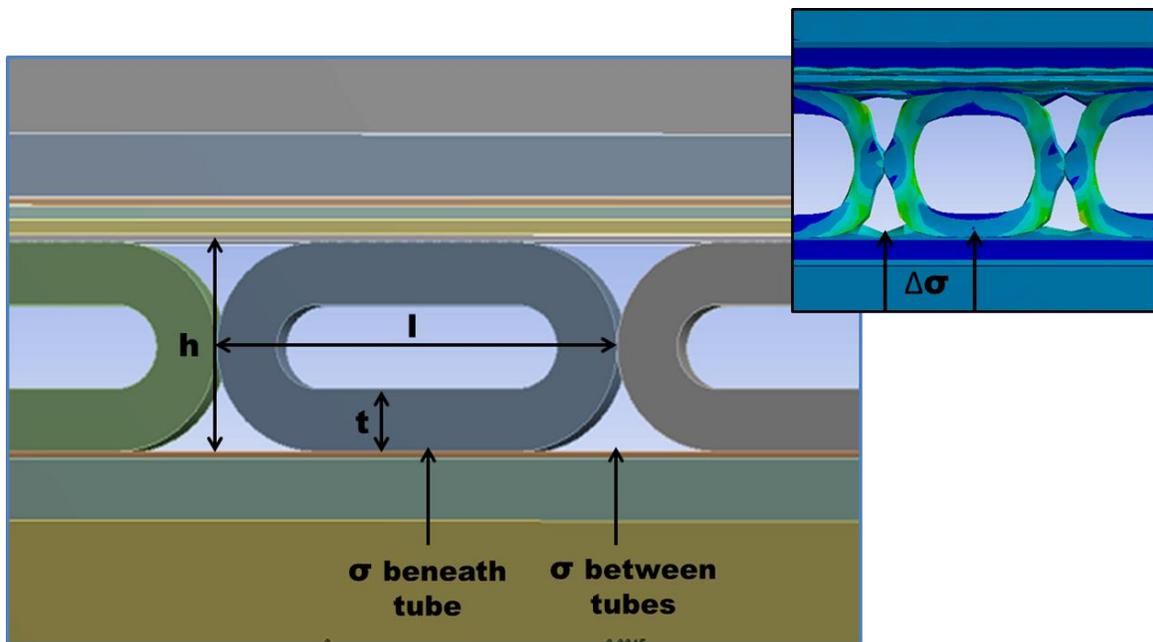


Figure 26: An illustration of the tube height, width and wall thickness and how it changes the stress state on the surface of the device.

The FEA model was constructed to model accumulated von Mises stress during the fabrication step where thermomechanical stresses are at their highest. The model assumes all materials are bonded in a stress free state at the fabrication temperature of 290°C . The entire structure is then cooled to room temperature (25°C) while monitoring the von Mises stress and deformation of the structure. Modeling of the von Mises stress beneath and beside one of the innermost tubes

provides the stress state for all of the tubes in the interface with the exception of the outermost tubes. Values from this model can then be used to predict tubing stresses regardless of the quantity of tubes in the interface.

The modeled von Mises stress values along both paths of interest can be seen in Figure 27 presented as a function of increasing tube wall thickness. A wall thickness of half the height will result in a solid structure. The blue line in the plot represents the stress on the device directly beneath the tube and the red line, the device stress between the tubes. It can be seen from the graph that some values of tube wall thickness will result in large von Mises stress differentials. A differential stress on the device is also undesirable. However, there are two wall dimensions which result in equal stress values on the device surface regardless of measurement position. This can be seen in the plot below (Figure 27) where the lines intersect. This plot, for a tube height of 1 mm, shows equal stress values for wall thicknesses of 0.1 mm and 0.43 mm. A wall thickness of 0.43 mm represents an 86% solid tube.

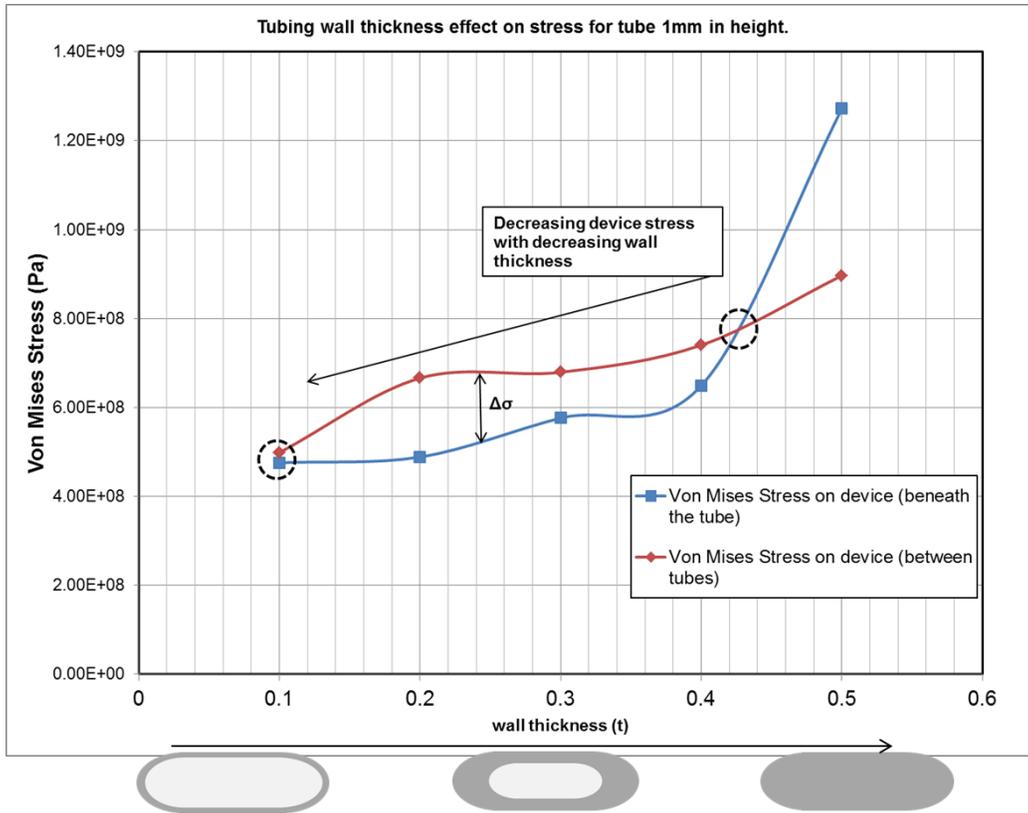


Figure 27: Equivalent von Mises stress on the device in the area between tubes (red) and directly underneath the tube (blue).

The other obvious trend in the graph is that regardless of the stress differential along the device surface, the total stress on the device decreases as the wall thickness decreases. Although this trend aids in designs for minimizing stress on the device, the reduction in wall thickness also results in lower thermal conductivity which needs to be considered. Previous sections describe the benefits of wall thickness to thermal conductivity.

Additional FEA models were then constructed to assess stress as a function of wall thickness for other tube heights. The stress models were performed for tubing heights of 0.8 mm, 1.0 mm and 1.2 mm. The aspect ratio for each of the three interface heights was maintained in an effort to

have the bonding flat area no less than half the total tubing width. These interface heights were chosen based on the current ideal height of 1 mm allowing for an assessment of stress when the interface is slightly increased and decreased which is necessary to accommodate device height differences.

The results of the models are summarized in Figure 28. Each tubing height possesses two distinct wall dimensions where the stress differential on the device surface is minimized. For the 0.8 mm tubing height, these two wall thickness measurements would be approximately 0.1 mm and 0.36 mm. A wall thickness of 0.36 mm represents approximately 90% solid tube. For tubes with a height of 1.2 mm, these two regions are found at tube wall thicknesses of 0.05 mm and 0.56 mm. A wall thickness of 0.56 mm represents a 93% solid tube. For each of the three conditions, the decrease in surface stress from a solid to a thin wall tube is considerable. From the plot below it can be seen that the device attached with a 1.0 mm solid round experiences a von Mises stress of 1.28 GPa. Using a 1.0 mm tube with a wall thickness of 0.1 mm reduces this von Mises stress to 0.5 GPa. This translates to more than a two-fold reduction in stress from the device perspective.

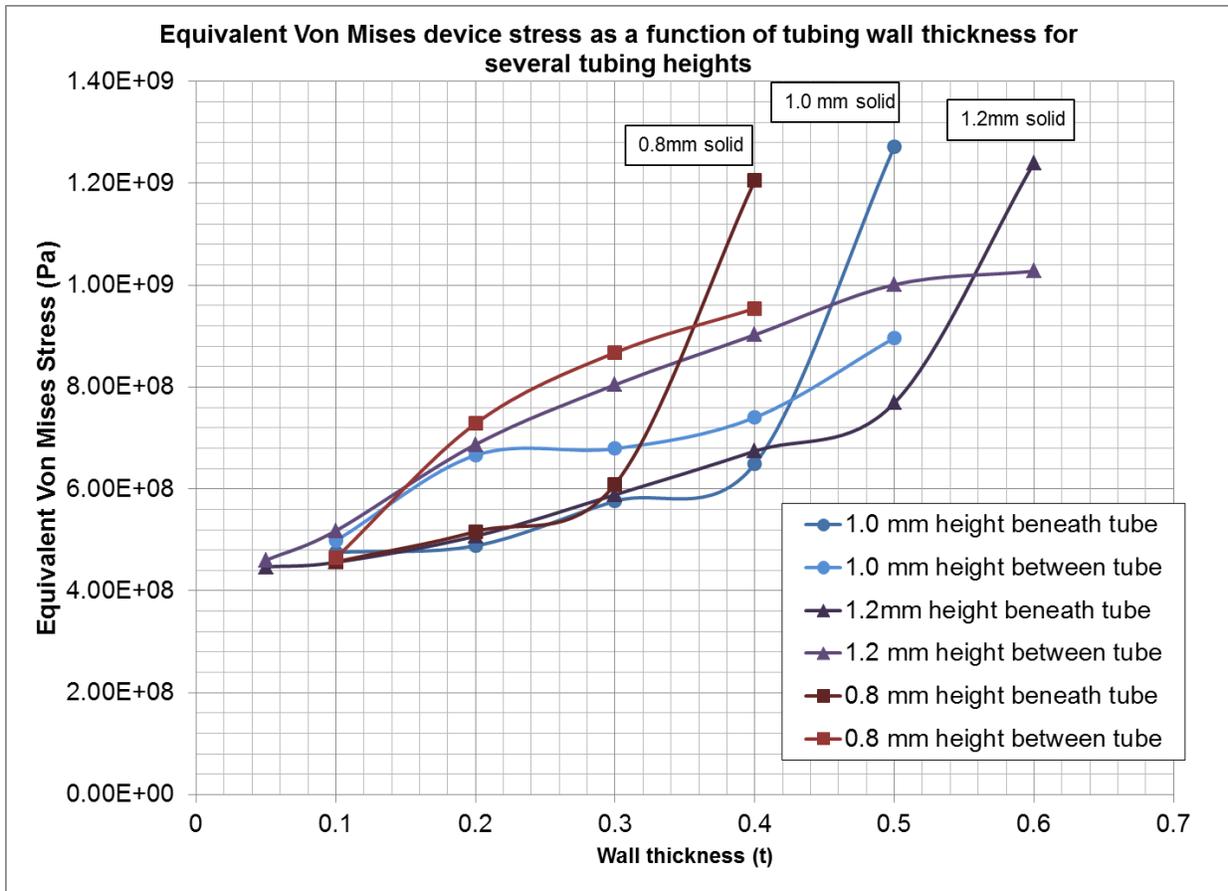


Figure 28: Equivalent von Mises stress distribution (between the attached tubes and directly underneath tubes) for various tubing heights.

From the graph, it can also be seen that the von Mises stress trend for each tubing height is predictable and scalable. These models can be used as a design tool when considering alternative heights. These stress parameters are independent of tube quantity in the interface assuming a fixed tubing aspect ratio is maintained. For example, in the case of a tube height of 0.4 mm (the lowest interface height for avoided dielectric breakdown in air at 1200V) the face width of the tube would be 0.8 mm with bonding flats of 0.4 mm. Each innermost tube can be expected to have a threefold increase in von Mises stress as the tubing approaches a solid. The solid value von Mises stress is expected to be on the order of 1.2 GPa and the stress between and

under the tubes will agree at two values of tubing wall thickness. The higher of the two is expected to be approximately 90% of the solid rod or 0.36 mm.

When viewing the expected curvature change of the tubing under stress from fabrication, it can be seen that the curvature increases. This mechanism was illustrated in previous sections as a means to accommodate the CTE stress and is responsible for a reduction in stress at the device interface. The tubing walls have previously been modeled to represent the actual fabricated prototype which has tube walls in direct contact with each other along the interface in the plane. When viewing the deformation with the model at these contact points it can be seen that the tubing wall is constrained at the contact and is forced to buckle above and below the contact point which may undermine the change in curvature which reliefs device stress. In an effort to determine if this additional pinning of the tubing wall imposed additional stress on the device surface, alternative tube spacing was modeled as well. In the alternative spacing, a small (0.5 mm) space was inserted between adjacent tubes. The results of the two models can be seen in Figure 29. From the results, the tubes in direct contact (top) show buckling at the interior contact points which is different from the outer walls where no contact is made. The tubes with no direct contact (bottom) reveal unconstrained buckling at each of the tube walls. The stress profiles are different with the spaced pattern of tubes revealing lower von Mises stress both directly beneath and between the tubes.

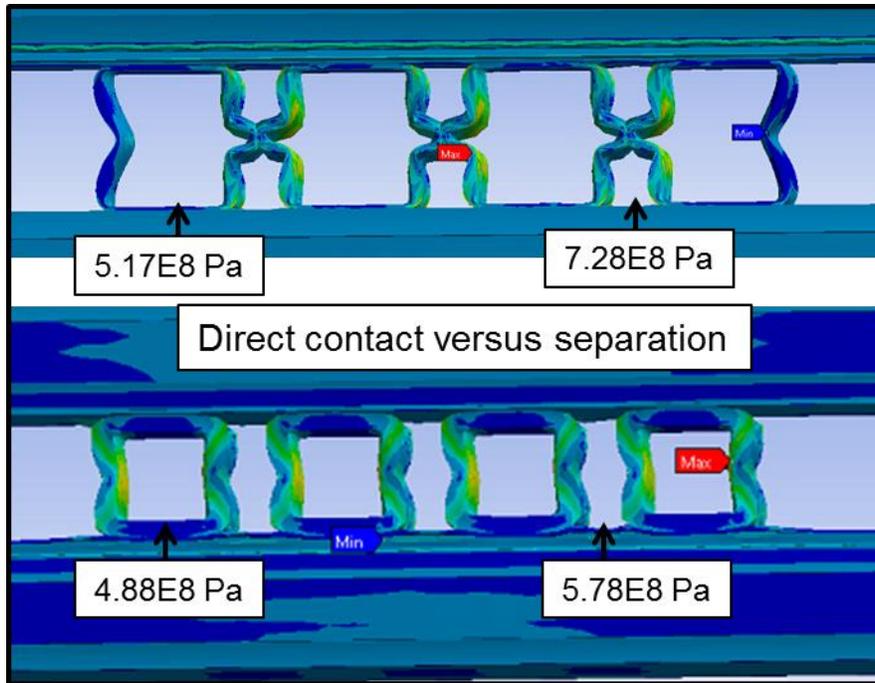


Figure 29: The deformation behavior of tube structures in direct contact versus those tube with spacing to avoid contact.

The result of this model aids in calculating the stress of a singular tube which may be used in place of a plurality of tubes for this aspect ratio. For a large area device with a surface of 10 mm by 10 mm, the single tube required for this connection would be 10 mm wide and have bonding flats of only 5 mm. The height would also be much higher at nearly 5 mm total causing the thermal conductivity to suffer accordingly. Models for far different aspect ratios were not considered within the scope of this work. The combination of the von Mises stress trend along with a relationship for the thermal conductivity of the interface will aid in designing the optimum interface. However, the thermal conductivity is weighted too largely for larger wall thicknesses resulting only in candidates containing upward of 80% silver which has been shown in this section to increase device stress regardless of interface height.

2.3.5. Alternative Materials for Thermomechanical Design

The use of silver as the tube compliant layer may be a cost barrier to high yield manufacturing. Alternative metal tubes which are less costly may be substituted, but certain requirements still exist. Because the metal tubes will be used electrically, it is paramount that resistivity be minimized. It is, therefore, not surprising that many of the candidate metals when filtered by resistivity are already utilized in power electronics packaging. A list of viable candidates with their respective cost and thermal, mechanical and electrical properties of interest are shown in Table 16.

Table 16: Candidate materials for tube compliant interface substitution [69].

Metals	Thermal Conductivity (W/m.K)	CTE (ppm)	Resistivity ($\mu\text{ohm.cm}$)	Elastic (Young's Modulus (GPa)	Yield Strength (MPa)	Fatigue Strength @ 10^7 cycles (MPa)	Cost (\$/gm)
Gold(soft)	314	13.5-14.5	2-3	76-81	20-40	40-65	\$40.00
Soft Silver	416-422	19.5-19.9	1.67-1.81	69-73	45-65	65-105	\$0.80
Hard Silver	416-422	19.5-19.9	1.67-1.81	69-73	190-300	100-170	\$0.80
Copper (soft)	353-401	16.8-17.3	1.7-1.74	120-125	45-55	70-90	\$0.23
Copper (hard)	390-398	16.8-17.3	1.7-1.74	128-135	180-340	115-125	\$0.23
Aluminum (wrought)	239-249	22.9-24.1	2.6-2.8	69-72	24-26	26.5-28.7	\$0.02
Sterling Silver	357-365	19.0	1.94-1.98	70-80	124	95-150	\$0.77
Coin silver	355-363	18.5-19.3	1.99-2.03	70-80	140-175	95-155	
Cu76Ag24	400-410	17.4-17.6	2.12-2.31	115-122	900-950	450-475	

Of these materials, coin silver and silver-copper alloys like Cu76Ag24 pose reasonable substitutions, but are not commercially available. Aluminum is the least expensive, yet has the lowest thermal conductivity and still requires special processing to be compatible with sintered silver LTJT. The best material for substitution is copper and simulations were performed using the hard copper because of the higher yield strength and fatigue life.

FEA simulation was performed for analyzing device stress changes when the tubing compliant interface material is replaced with copper. Two different stresses are important to observe because the tubing interface is not homogenous. The device stress directly beneath the tubing flat and the stress on the device between two tubes were evaluated. The results of the analysis for the tube height and wall thickness used in the fabricated modules are shown in Table 17.

Table 17: Comparison of device stress for copper substitution in tube compliant interface.

	Cost (\$/gm)	Tube height (mm)	Wall thickness (mm)	von Mises stress on device directly beneath tube base (Pa)	von Mises stress on device beneath tube separation (Pa)
Silver (pure)	0.80	1.00	0.20	4.89E+08	6.66E+08
Copper (hard)	0.23	1.00	0.20	4.94E+08	7.37E+08
		Change		+5.47E+06	+7.10E+07

The copper tubes have a slight increase in von Mises stress on the device for this wall thickness. The previous modeled relationships for wall thickness and height may help mitigate these additional stresses. Yet, copper still requires a UBM scheme or special sintering atmosphere control to be compatible with sintered silver.

2.3.6. Parasitic Investigation

Inductance, capacitance and resistance were modeled using an ANSOFT software suite called Q3D Extractor. A three-dimensional model was constructed to scale from the actual dimensions of the entire quarter-bridge module. However, the planar quarter-bridge circuit requires separation for accurate modeling. In application, the current path when the IGBT is in the on-state is different from the current path in the off-state. But, due to the module symmetry, the path dimensions for each state are identical. The current path in the IGBT on-state starts on the bottom trace, moves through the IGBT and then along the length of the top trace to the output. In the off-state, the flow is reversed and is commutated from the top trace to the bottom trace through the freewheeling diode. To model only one of the two possible paths, the diode and tube connection for the diode were removed from the model. The structure minus the diode can be seen below in Figure 30. The source and sink assignments are also shown in Figure 30. For the copper traces on the DBC, the source and sinks are assigned to the end faces rather than utilize a wire connection. In module prototypes the current will be applied with a long tab covering the entire copper trace uniformly. The source and sink assignments were made to stay consistent with the functional module. The goal of this model was to assess only the tube interface electrical quantities so extraneous hardware was left out of the assembly.

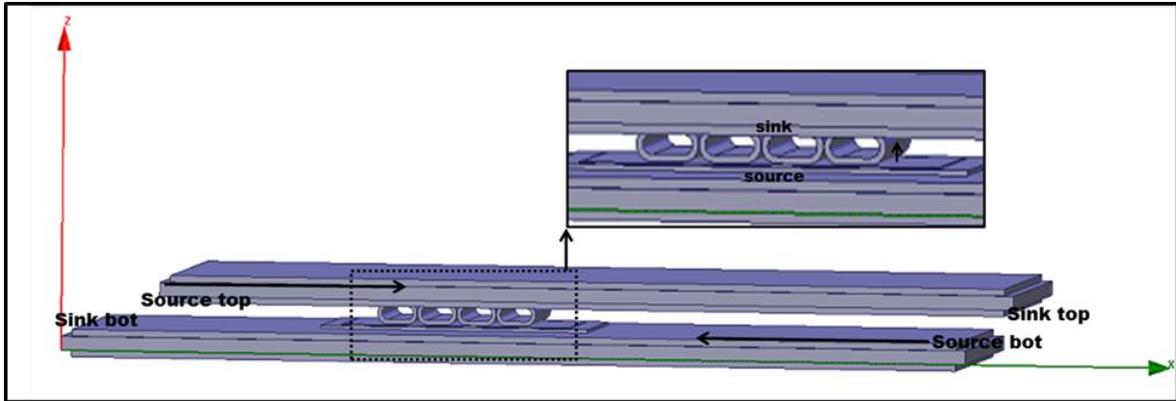


Figure 30: Three-dimensional structures used for modeling the electrical parasitics in the double-side package connection with labels showing assigned source and sink locations.

2.3.7. Parasitic Model Results

The quantities of interest were the parasitic loop inductance and resistance. Ansys[®] Q3D Extractor[®] software provides a matrix for each quantity in the model. The elements in the diagonals of the matrix are the self-resistances and inductances. The other elements in the matrix represent the mutual resistance and inductance. The DC inductance matrix for a 1 MHz simulation is shown in Table 18. The DC inductance for the entire loop can be found by adding the diagonal elements for the entire system. This results in a total loop inductance of 25.16 nH for the IGBT leg of the circuit. From the matrix, it can be seen this inductance is split into 8.84 nH contribution from the bottom trace and 16.33 nH result from the tube connection and the top trace. The average tube contribution to inductance is 0.056 nH.

Table 18: DC inductance matrix for planar tube connected device trace.

DC Inductance Matrix (nH) 1 MHz	bottom substrate top copper trace	tube 1	tube 2	tube 3	tube 4	top substrate bottom copper trace
bottom substrate top copper trace	8.8366	0.00020522	-0.00021094	-0.00056039	0.00033968	9.1861
tube 1	0.00020522	0.05625	0.034371	0.021001	0.01535	0.00039884
tube 2	-0.00021094	0.034371	0.056326	0.034258	0.021065	-0.00036227
tube 3	-0.00056039	0.021001	0.034258	0.055981	0.034174	-0.00063085
tube 4	0.00033968	0.01535	0.021065	0.034174	0.056069	0.00032823
top substrate bottom copper trace	9.1861	0.00039884	-0.00036227	-0.00063085	0.00032823	16.102

Using these simulated values a schematic of the quarter bridge circuit with modeled inductance values can be constructed. The quarter bridge schematic with modeled inductance values is shown in Figure 31. The model did not include the connection tabs into the module which have been shown to have a large contribution in conventional module architectures. Other research has explored the modeling of parasitic inductances in double-side architectures. Olszewski et al. reported a modeled loop inductance of only 6.3 nH for a three-dimensional module package and 19.75 nH for a conventional Toyota Prius inverter module. [73] Another research group, Shengnan et al., reported modeled inductance values of 26.53 nH for a three-dimensional package [74]. These efforts mark the highest and lowest known published values of modeled parasitic inductances in packages with two sides. Other groups have reported modeled values between 12 and 20 nH [75]. With the sensitivity of the model to small changes in geometry and boundary conditions it is very difficult to make comparisons from model to model.

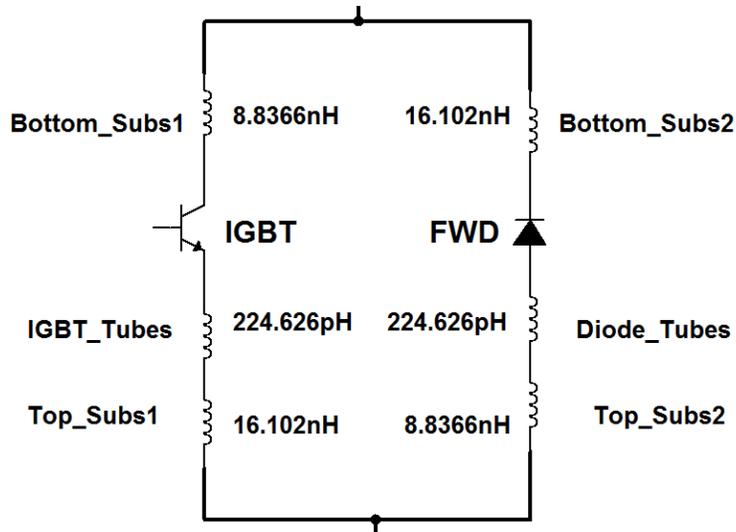


Figure 31: Schematic of quarter bridge module with simulated inductance values included.

The DC resistance matrix is shown in Table 19. The resistance contribution from the tubes in the tube array above the IGBT contributes only 20 $\mu\Omega$ to the loop. The traces contribute approximately 0.1 $\mu\Omega$ each.

Table 19: DC resistance matrix for planar tube connected device trace.

DC Resistance (Ω) Matrix 1 MHz	bottom substrate top copper trace	tube 1	tube 2	tube 3	tube 4	top substrate bottom copper trace
bottom substrate top copper trace	0.000065951	0	0	0	0	0
tube 1	0	5.6302E-06	0	0	0	0
tube 2	0	0	5.6269E-06	0	0	0
tube 3	0	0	0	5.6364E-06	0	0
tube 4	0	0	0	0	5.6386E-06	0
top substrate bottom copper trace	0	0	0	0	0	0.00010213

Chapter 3. Process Development and Fabrication

3.1. Module Configuration

3.1.1. Half-Bridge Summary

Many half-bridge modules are offered commercially. One such module rated at 1200V and 150A is offered by Micross Components. The module footprint and interior circuit is shown in Figure 32. This module represents a half-bridge configuration and shows two inputs for the DC voltage, one tap for the output, and two taps for the gate and emitter signal to each IGBT. The pins shown are the minimum necessary connections for a half-bridge module.

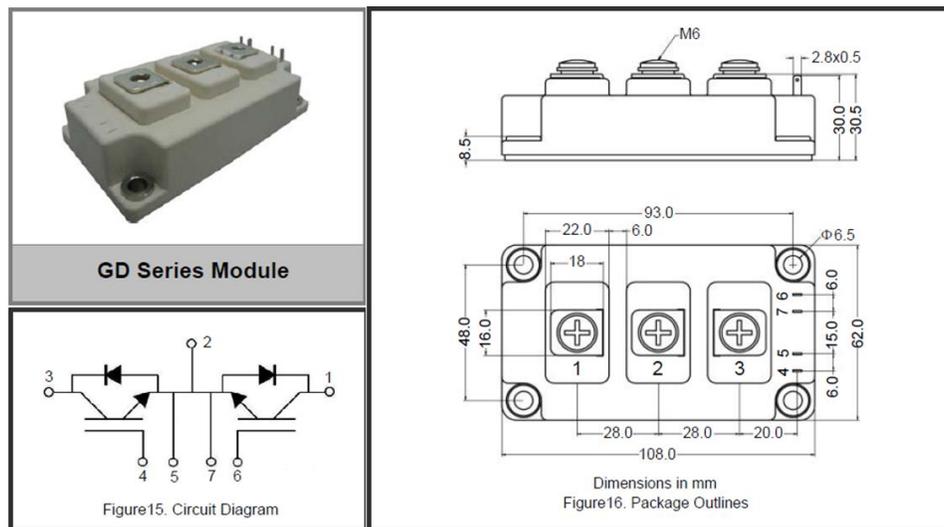


Figure 32: Representative commercially available half-bridge power module.
(<http://www.micross.com><http://www.micross.com>/ accessed 5/17/14) Used under fair use, 2014.

The circuit for the half-bridge double-side module looks identical to the circuit in Figure 32. The module will contain one IGBT and one diode for each switching unit. Output connection tabs

will be placed for accessing the DC link voltage and for the output. A pair of gate-emitter terminals is necessary for driving each IGBT. The electrical schematic illustrating the current flow in the double-side half-bridge design is shown in Figure 33.

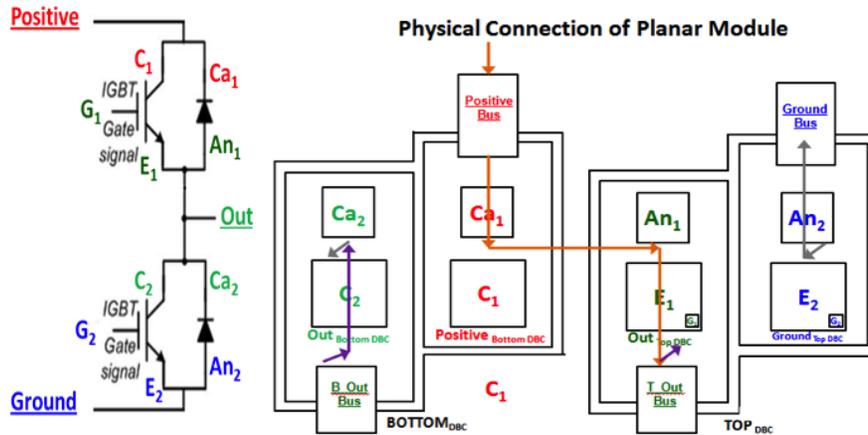


Figure 33: Electrical schematic illustrating the current flow in the double-side half-bridge module.

Referencing the die placement from the thermal assessment, the reduced parasitic layout and the compliant interface stress evaluation, a final design for fabrication was established. The final half-bridge configuration resembles the diagram in Figure 34. The disadvantage of this design is the gate bias terminal locations. These two connections are accomplished by one wirebond from both the gate and emitter device pads to a male header which will be attached to the outside surface of the top substrate.

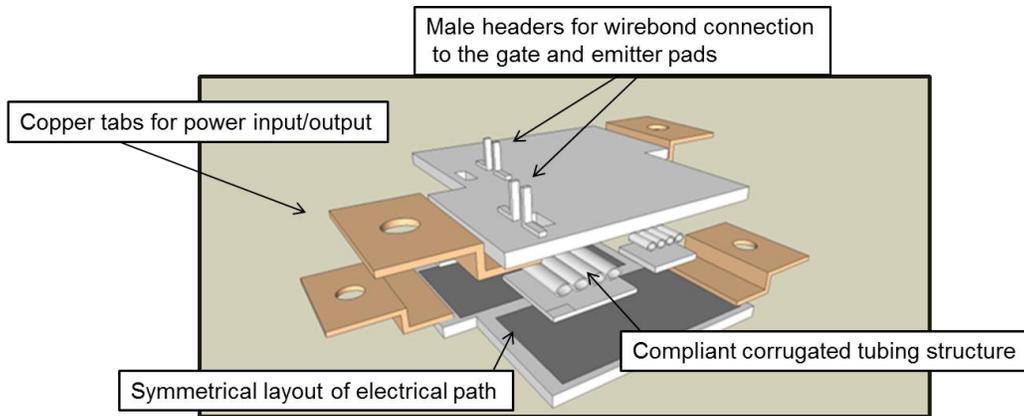


Figure 34: Proposed design for fabrication based on design constraints.

3.1.2. Quarter-Bridge Summary

The quarter-bridge design was optimized for integration. The benefits gained from dividing the half-bridge into two parts were 1) easier fabrication 2) decreased requirement for planarity 3) increased yield 4) increased surface area and 5) more thermally desirable placement of devices. The design constraints on the die placement die stresses and module footprint are all similar to that of the half-bridge. The quarter-bridge electrical schematic with current flow is shown below (Figure 35). It is clear that the symmetry of the half-bridge configuration allowed the entire structure to be easily halved.

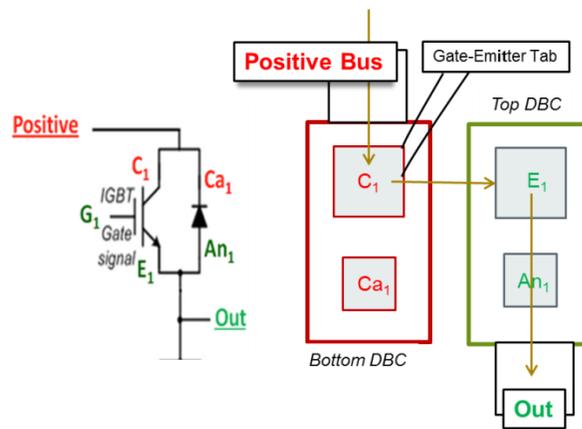


Figure 35: Electrical schematic illustrating the current flow in the double-side quarter-bridge module

However, the quarter-bridge design also allowed for improved gate and emitter pin locations. Both pins have been moved to the bottom substrate and pushed closer to the edge (Figure 36). This one change allows a larger unimpeded surface area for cooling with attached heat sinks.

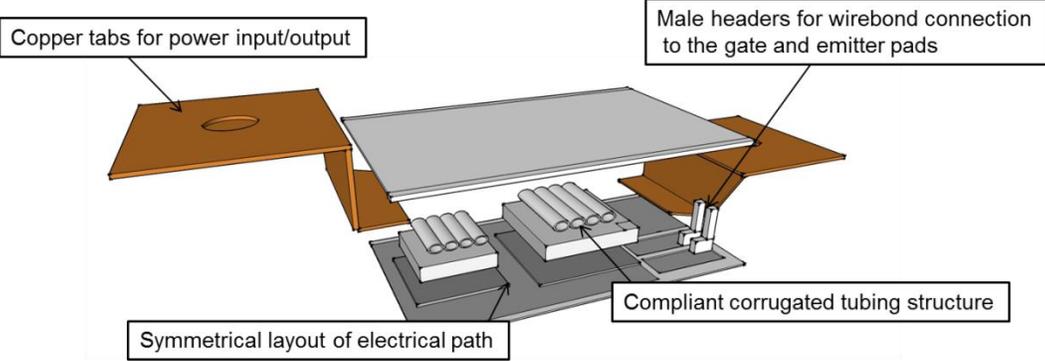


Figure 36: Quarter-bridge module design.

This quarter-bridge module can still be used to make a full-bridge configuration by rotating an identical quarter-bridge module 180° and mounting it adjacent. This symmetry also places the IGBT and diodes of the adjacent module 180° from each other which is more ideal thermally (Figure 37). IGBTs of the low and high-side switches will usually operate 180° out of phase and this should better distribute heat during application.

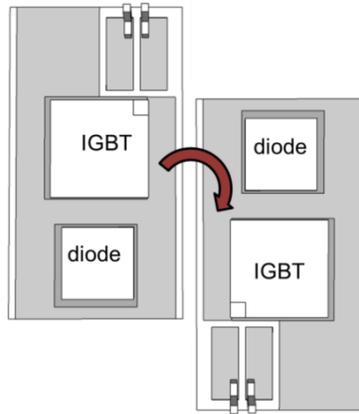


Figure 37: Illustration of coupling quarter-bridge modules for half-bridge configurations. The symmetry also places the active IGBT far from the opposing IGBT which should enhance the packages thermal properties.

3.2. Chip Level Metallization

Most power silicon devices in bare die form (IGBTs, MOSFETs and diodes) are vertical devices with electrical terminals on both the top and bottom surfaces. The bottom surfaces are normally deposited with gold for compatibility with solder for attachment to the substrate. The top surface electrical pads are normally made from aluminum and passivated with a thin layer of dielectric for protection. The passivated aluminum surface works well for wirebonding technologies because the bonding process will easily penetrate through the passivation to the aluminum layer. For sintered silver compatibility, the top surfaces need to be metallized. This metallization is called Under Bump Metallurgy (UBM).

The UBM layer needs to provide good adhesion to aluminum, act as a diffusion barrier and provide an oxide free surface which is compatible with silver sintering. To accomplish these

tasks effectively it is necessary to use different metals. Commonly used UBM schemes are listed below [20, 31, 76].

- Cr--> Cr:Cu-->Au
- Ti-->Cu
- Ti:W-->Cu
- Ti-->Ni:V
- Cr-->Cr:Cu-->Cu
- Al-->Ni:V-->Cu
- Ti:W-->Au
- Ti-->Ag
- Cr-->Ni-->Ag

The UBM can be applied to the die surface using evaporation, sputtering or electroless plating methods. Sputtering is preferred because the added kinetic energy (100 eV versus 0.5 eV for sputtering) aids in adhesion.

The back electrical pads of the as-received ABB devices for this work were already metallized with layers of Al/Ti/Ni/Ag. The top electrical pads, however, were metallized with a 4 micron layer of 1% AlSi which is not compatible with solder or sintered silver processing. To add the UBM, the top die surfaces were masked to 1) allow for cleaning passivation layer from only the electrical pads and 2) to insure metallization does not reach the guard ring of the device causing device failure. Masks were constructed of 5 mil stainless steel and designed for metallizing

multiple IGBTs and diodes. Pictures of the masks fabricated for metallizing the IGBTs are shown in Figure 38 below.

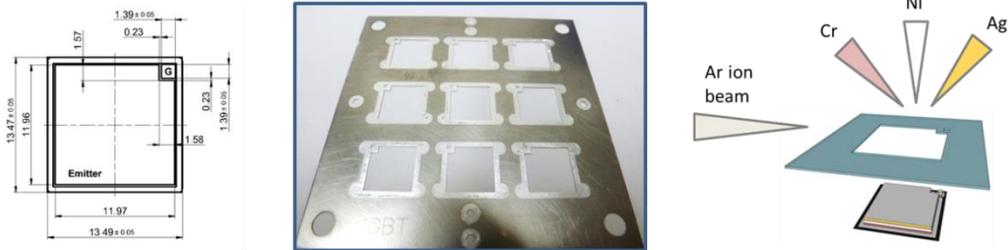


Figure 38: IGBT device parameters and stainless steel mask for applying UBM using PVD.

Before metallization schemes can be added to the device surfaces any passivation layers need to be removed. The ABB dies used for our study are passivated with polyimide. Ineffective removal of the passivation layer has been shown to increase terminal resistance and may lead to poor adhesion of the UBM metallization [77]. Experiments to confirm the presence of passivation were performed using X-ray Photoelectron Spectroscopy (XPS). XPS on the as-received die reveals low concentrations of aluminum in addition to surface carbon contamination (top plot of Figure 39). After argon sputtering for 20 seconds using a 3kV beam, the surface carbon contamination has disappeared and strong concentrations of aluminum can be seen (bottom plot of Figure 39). The argon sputtering proved successful for cleaning the surface prior to metallization deposition.

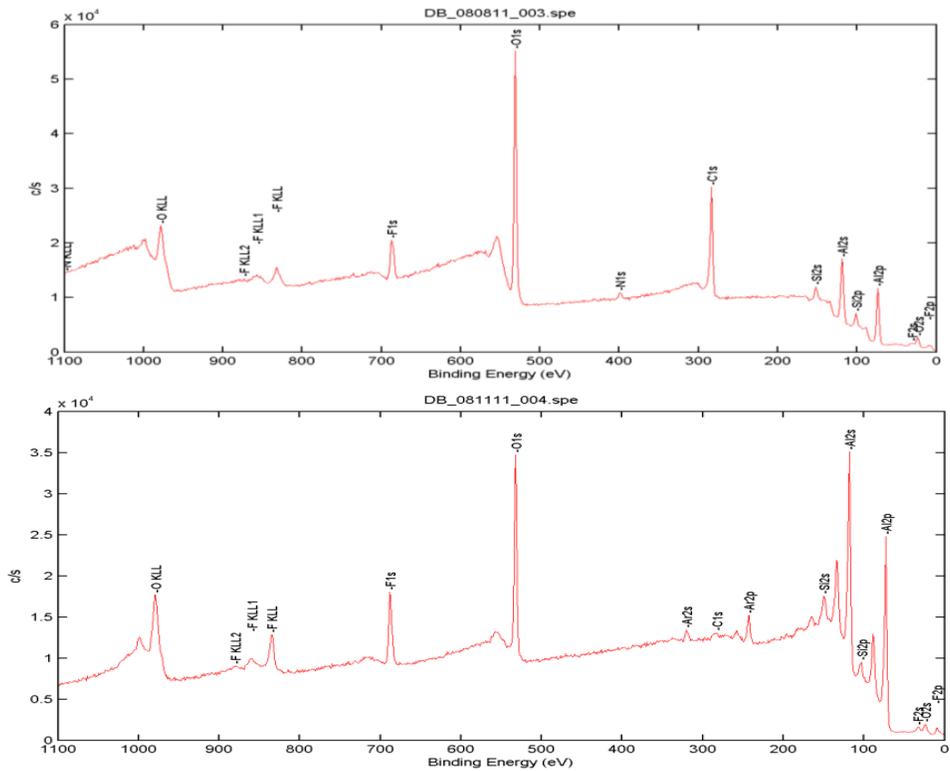


Figure 39: X-ray photoelectron spectrometry (XPS) of the as-received die (top) and the die cleaned using argon sputtering (bottom).

The Pulsed Vapor Deposition (PVD) technique was used for metallization. The masked surfaces were first cleaned with an Argon ion beam before applying 150 nm of Cr for adhesion to the AlSi layer, another 200 nm of Ni for a diffusion barrier and finally 250 nm of Ag for insuring a good bond to the sintered silver die attachment.

For confirming layer thickness and alignment, a non-contact Zygo profilometer was used. The profilometer scans can be seen in Figure 40. This test is necessary for determining the accurate metallization depth and to verify the metallization has not reached the guard ring of the gate or emitter pads.

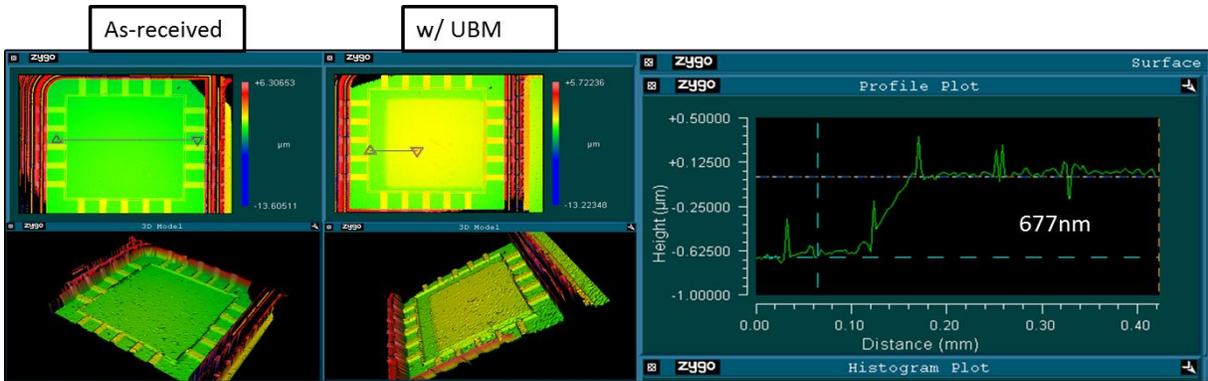


Figure 40: Non-contact profilometer results of as-received (left) and metallized (right) devices.

3.3. Compliant Corrugated Interface Construction

The compliant interface designed for stress remediation consists of a plurality of tubes bonded on the tops of the devices. Tubes of any inside or outside diameter can be used with attention given to the effects on device stresses as mentioned in Chapter 2. The height (h) of the interconnect is controlled by pressing the tubes into elliptical shapes. The length (l) is chosen to maximize connection to the top electrical pad of the device. The period (p) reflects the repeating units and can be adjusted to reflect more or less contact with the device surface. The wall thickness is adjusted by subtracting the outer diameter (O.D) from the inner diameter (I.D.) and dividing by two. These design variables are illustrating more clearly in the patent application drawing shown in Figure 41. For our experiment 99.9% pure silver tubes were chosen.

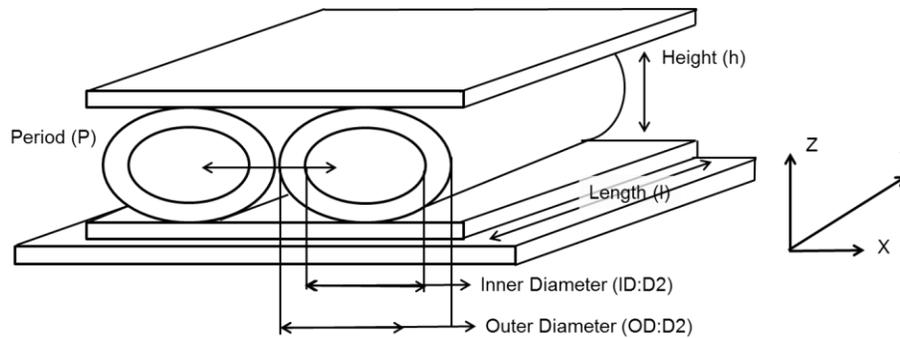


Figure 41: Patent application diagrams for proposed compliant tube interface indicating the design variables for accommodating multiple interconnection schemes.

One issue that has plagued module manufactures attempting to utilize double-side cooling is the difference in device heights [4]. Normally, diodes and IGBTs of similar ratings will have device thickness differences of several hundred microns. It has, in the past, been difficult to assemble these devices in a planar assembly without the use of solid spacers. For the corrugated tube interconnect, the thickness can be controlled by changing the pressing height. The length (l) will be adjusted to fit the device electrical pad of the diode (6 mm) and IGBT (10 mm). A fixture for cutting repeatable adjustable lengths was fabricated and is shown in Figure 42.

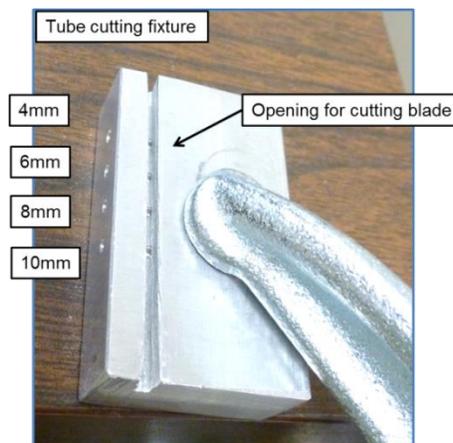


Figure 42: Custom fabricated tube cutting fixture.

The press shown in Figure 43 was also custom fabricated for pressing tubes to elliptical shapes of different heights while leaving flat areas on the top and bottom of the tube shape for bonding. The leftmost press opening is 1200 microns and the rightmost opening is 700 microns. The 100 micron divisions allow for coarse adjustment of height differences for bonding different devices when necessary.

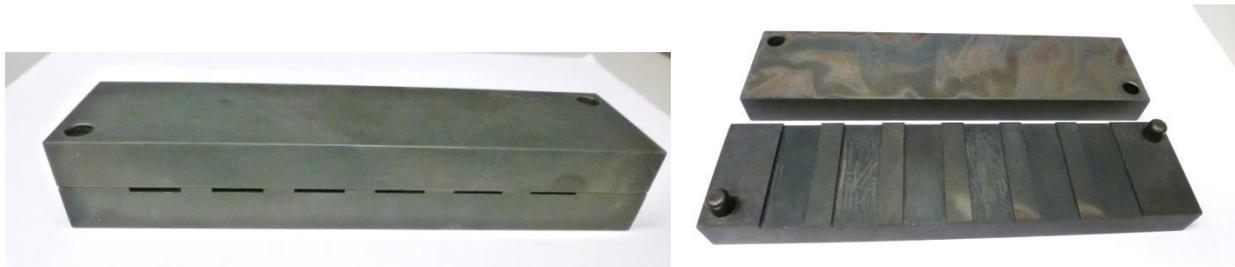


Figure 43: Custom fabricated tubing press for adjusting the tubing height to accommodate different device thicknesses.

The datasheet device thicknesses for the IGBT and diode were 140 microns and 350 microns, respectively. For this experiment, the difference between the top of the devices and the electrical trace on the top substrate was chosen to be 1100 microns. Tubes for attachment to the IGBT had an O.D. of 1.72 mm with a wall thickness of 0.30 mm. These tubes were pressed using the press to be approximately 1100 microns tall. The tubes for the diode had an O.D of 1.47 mm and a wall thickness of 0.30 mm. These tubes were pressed to be approximately 900 microns tall. The different tube diameters were chosen to allow ample open space inside the tubes after pressing. Directly after pressing, the tubes were lightly polished to insure the bonding areas were uniform and flat. These flats are polished one additional time after attachment to the top substrate. This extra polishing step is necessary to correct any misalignments which may have occurred in the previous sintering step. The tube flats are measured relative to the attached substrate and are

polished to at least a 15 micron tolerance. The pressed tubes after attachment to the top substrate and polishing can be seen in Figure 44.

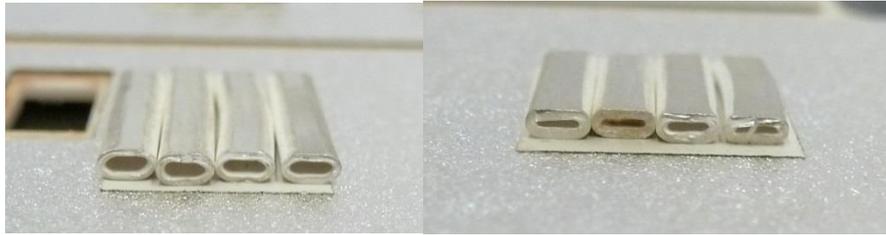
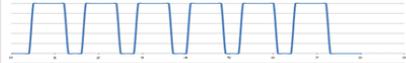
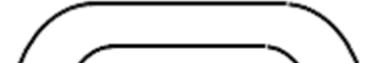


Figure 44: Tubes constructed for attachment to the IGBT (left) and the diode (right).

For accurate modeling, the tubes are measured at this point in the fabrication process using open source image analysis software. The dimensions from this measurement are used in the FEA models in Chapter 2.

For this work, four tubes for each of the attachment footprints were chosen. The decision to use four tubes was based on a combination of the interface opening constraints, commercially available silver tubing, encapsulation viscosity, structural stability, thermal conductivity and cost. The diode cathode footprint utilized was approximately 8 mm by 8 mm which maintained a safe distance from the device guard ring. The IGBT emitter footprint utilized for attachment was rectangular measuring approximately 8 mm by 10 mm. This area was necessary because of the guard ring and gate pad on the device. An image of the footprints is shown in the following section in Figure 48. After the tube aspect ratio was chosen, the choice of tube quantity was decided based on these footprint dimensions. A table outlining the possible tube quantities for fabrication is included as Table 20.

Table 20: Tube quantity selection criteria for a footprint measuring 8 mm on one side for a fixed aspect ratio.

Coverage of 8 mm footprint width	Interface height and bonding flat width (mm)	Bond distribution
	0.80	
	1.00	
	1.33	
	2.00	
	4.00	

From the table, it can be seen that decreasing the tube quantity for a given aspect ratio increases the interface height. An increased interface height reduces thermal conductivity, and increases weight and volume. Although, the same amount of bonding flat area exists in each of the five proposed periods listed above (4 mm bonding flat per 8 mm width), the distribution changes. The wider the distribution, the more structural instability exists during and after fabrication. For the instance requiring 8 mm length of coverage and a target interface height of 1 mm, four tubes is the best choice.

3.4. Double-Side Package Workflow

The fabrication process can be broken into 5 segments, 1) die attach, 2) tube attach, 3) top and bottom attachment, 4) connector assembly and 5) encapsulation. The quarter-bridge module is designed to be one half of the half-bridge module therefore the assembly workflow has identical fabrication steps.

The devices are first attached to the bottom substrate. The substrates are fabricated using a laser cutter and etching. Kapton tape is used to protect the substrates during fabrication. The IGBT and diode used in this experiment have bottom electrical pads measuring 13.5 mm by 13.5 mm and 10 mm by 10 mm, respectively. A stencil for each device is scribed in the protective Kapton tape layer using a laser cutter. This allows very accurate and repeatable placement of the devices. These squares are removed and the remaining surface cleaned. This opening will now serve as the stencil for printing nanosilver paste with a thickness of 50 microns. After paste application and tape removal the substrate is heated to 70°C until uniformly dry. This process helps to remove excess solvent and avoid squeeze out during the pressure sintering step. Devices are placed onto the paste footprint using alignment fixtures. A schematic of the workflow for this step is shown in Figure 45.

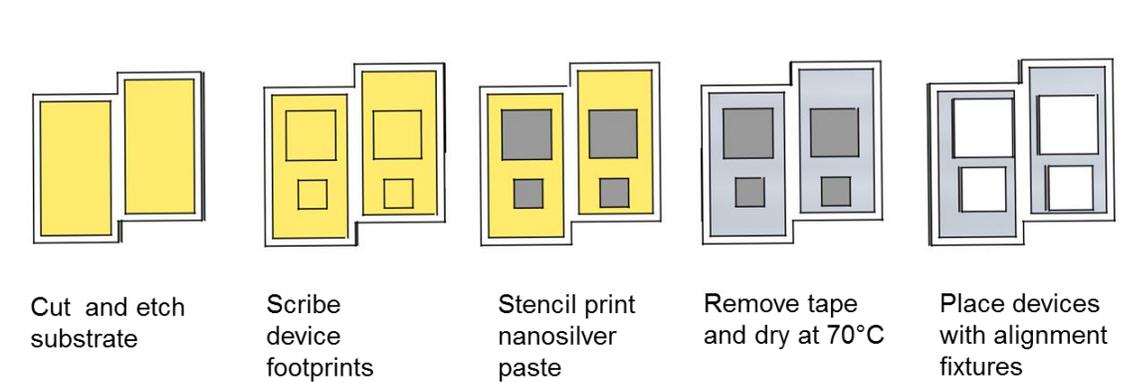


Figure 45: Workflow for die application on the bottom substrate.

The entire substrate is then pressure sintered for 5 minutes using the hot press shown in Figure 46 with a bottom platen temperature of 290°C. The sintering pressure used for this attachment was 3 MPa which is calculated from the overall attachment area. The higher temperature is needed to accommodate the temperature drop across the tooling and substrate. After the dies are attached, a 50 micron thick layer of nanosilver paste is stencil printed onto the top electrical pads. This layer is dried at a temperature of 180°C. This step removes solvent and binder which increases the density of the paste layer and forms a protective barrier for future sintering.

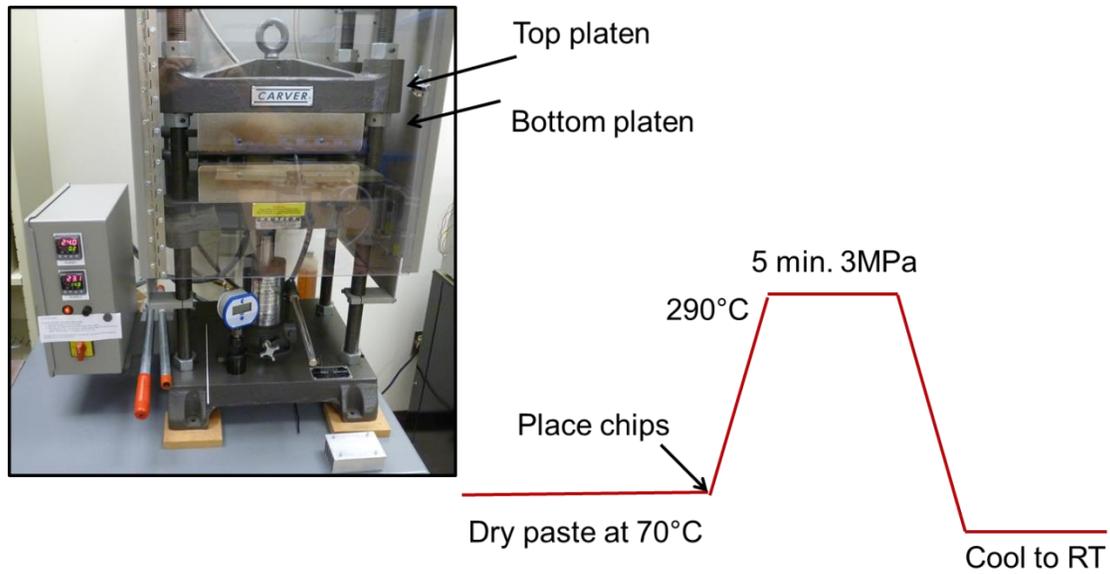


Figure 46: Hot press and temperature profile used for pressure sintering.

The tube attachment is much the same. The footprints are again scribed with a laser for accurate placement. These footprints are smaller to accommodate the smaller top electrical pad of both devices. In the case of the IGBT tubes, the gate pad (located at the top corner) should not be covered. A schematic of the workflow for the tubing attachment process is shown below in Figure 47.

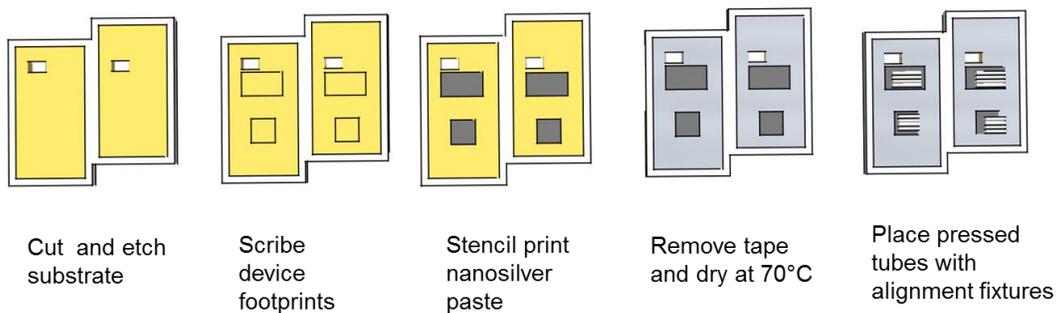


Figure 47: Workflow for tube application on the top substrate.

The entire substrate is then pressure sintered for 5 minutes using a hot press with a bottom platen temperature of 290°C. The sintering pressure used for this attachment was also 3 MPa which is calculated from the tube attachment area or “flats” of each tube.

At this point in the workflow, the quarter-bridge module wirebonding is performed while the two pieces are still apart. A 2 mil aluminum wire is wedge bonded from the gate and emitter pads to digits patterned on the bottom substrate as shown in Figure 48.

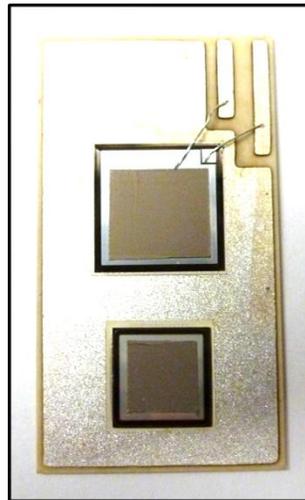


Figure 48: Wirebonding of the IGBT gate and emitter to the patterned digits on the bottom substrate.

The third step, the attachment of the top and bottom substrates, requires a high degree of planarity. To accomplish this, a leveling block has been fabricated which insures the entire package is perfectly parallel when pressure is applied. Because the block is needed on the bottom platen, the top platen is heated to 290°C. The pressing arrangement can be seen in Figure 49. With the largest amount of thermal mass being the half of the assembly containing the attached tubes, the substrate with the devices is on the top of the stack in direct contact with the

top platen. The combined pieces are sintered at 290°C for 5 minutes with 3 MPa applied. The surface area for this calculation is the tube “flats”.

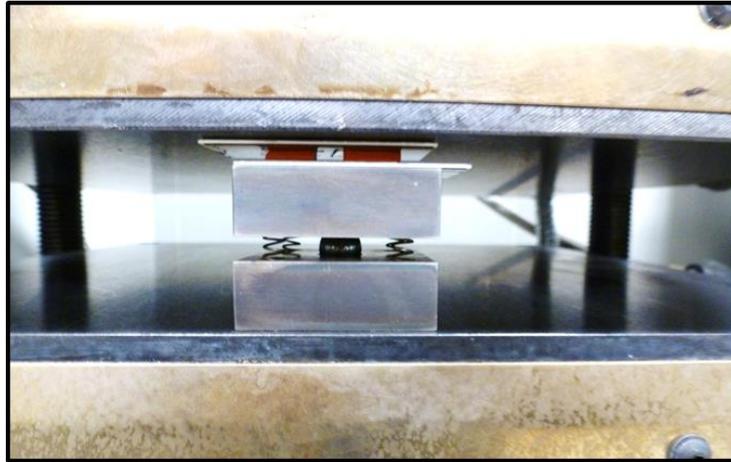


Figure 49: The leveling block pressing arrangement used for making the final attach of the double-side module.

The quarter-bridge module sintering is finished at this point. However, the half-bridge still requires wire bonding through the open holes to the gate and emitter pads below. The differences in the two configurations can be seen in the images of finished modules shown below (Figure 50).

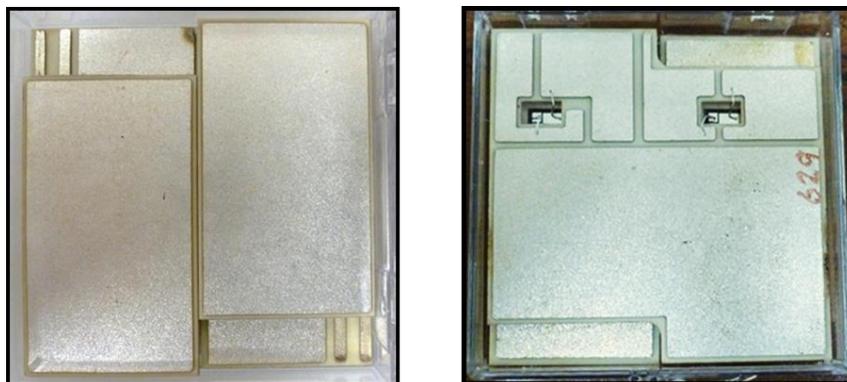


Figure 50: Images of sintered quarter-bridge modules (left) and a half-bridge module (right).

3.5. Additional Hardware for Integration

To complete the module packages for integration into systems, tabs must be attached for power input, outputs and gate-emitter signals. The tabs are cut from 20 gauge copper sheet using a metal shear. The tabs are cut 32 mm long by 22 mm wide and bent to shape using a bench hand bender. The tabs must be made as short as possible to reduce package inductance and the voltage drop per terminal should not be larger than 0.05V per terminal at rated current [4]. After bending, ¼ inch diameter holes are punched with a hand press. The hole diameter is chosen to be compatible with commercial module hardware [4]. The gate-emitter connector is a male header with a standard pitch of 0.1 inch.

The tabs and gate-emitter headers are attached by reflowing SAC solder. An alignment fixture accurately holds all the connections in place and SAC solder paste is applied to each connection. The alignment fixture can be seen in the left image of Figure 51.

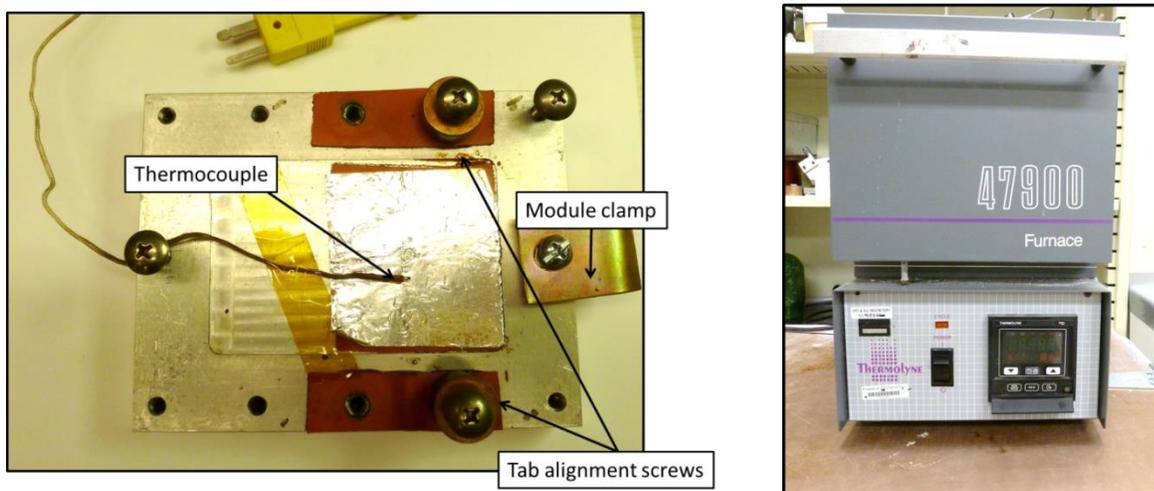


Figure 51: Custom fabricated alignment fixture for reflowing input and output power tabs as well as gate and emitter headers.

The entire fixture is placed into the muffle furnace (right image of Figure 51:) at 400°C. A thermocouple placed directly underneath the module is monitored and the fixture is removed when the module reaches 290°C. Half-bridge and quarter-bridge modules without encapsulation are shown in Figure 52 and Figure 53 showing the reflowed connecting hardware and interior tube geometry.

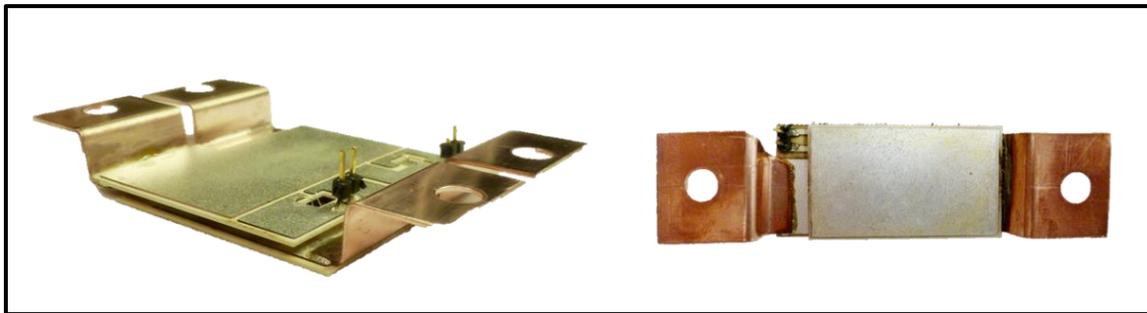


Figure 52: Modules (Half-Bridge, left and Quarter-Bridge, right) with reflowed connections before encapsulation.

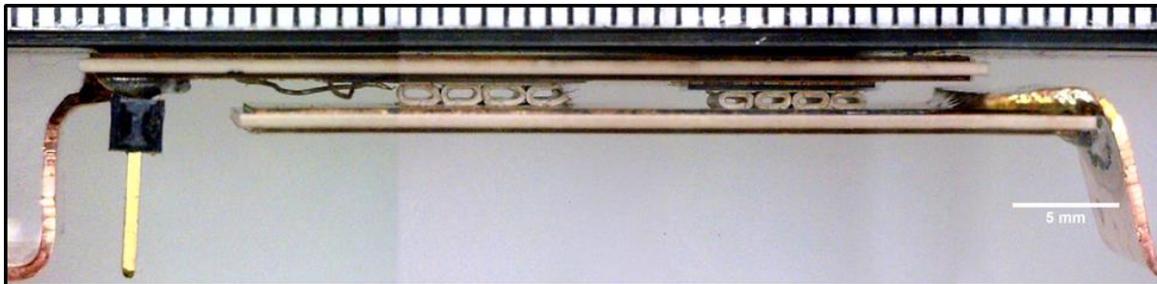


Figure 53: Close up stitched image showing the complete quarter-bridge geometry.

3.6. Encapsulation

3.6.1. Selection

The primary function of the encapsulant in a power module is to protect the semiconductor devices. Other criteria when selecting encapsulants are thermal properties, dielectric strength, chemical resistance, moisture absorption and gas permeability. Other factors equally as important are manufacturing friendliness, toxicity and cost. Very few encapsulants fulfill all the criteria well so there is always trade-offs when selecting. [4]

For this study, the semiconductor devices will be shielded by the substrates on the top and bottoms of the package so device protection is not an issue. Encapsulation modulus is especially important when coating wirebonds, but the double-side module connections are accomplished without wirebonds. Our largest constraints on module encapsulation are viscosity, cure temperature, CTE and high temperature performance. There are several encapsulation technologies available for every coating option. Table 21 below shows some of the advantages and disadvantages of each [9].

Table 21: Various encapsulant materials and qualitative properties [9].

	Silicone Gel	Silicone	Parylene	Silicon Nitride	Acrylic	Polyurethane	Epoxy
Ease of Application	B	C	D	D	A	B	B
Chemical Removal	C	D	-	D	A	B	D
Thermal Removal	-	D	D	-	A	B	C
Abrasion Resistance	B	B	B	D	D	A	A
Mechanical Strength	D	C	B	B	D	A	A
Temperature Resistance	B	A	A	A	D	D	B
Humidity Resistance	B	A	A	A	B	A	C
Pot Life	C	D	-	-	A	B	D
Cure (RT)	C	C	-	-	A	B	B
Cure (Elevated Temperature)	C	C	-	-	A	B	B

The epoxy group is ideal for use inside the double side module. The temperature resistances of epoxies have increased since the table was constructed and the CTE of the epoxies more closely resemble those in our system. Several epoxy encapsulants were studied for selection. To determine the optimum temperature resistance and CTE, a push rod dilatometer made by Orton Ceramics was used. An image of the dilatometer is shown in Figure 54.

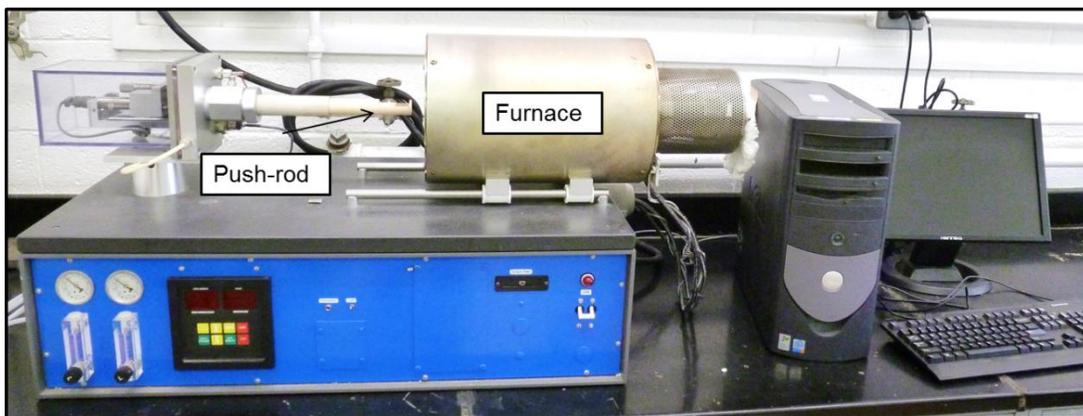


Figure 54: Pushrod dilatometer for measuring coefficients of thermal expansion to high temperatures.

Dilatometry is a technique that uses a high purity alumina rod to push against the sample as the sample is heated in a furnace. The change in length versus temperature is recorded using a sensitive Linear Variable Differential Transformer (LVDT) for sensing position. The alumina CTE is known and easily subtracted from the data to reveal the CTE of the material tested.

The Orton Dilatometer used was calibrated for 1 inch samples. A sample of cured encapsulation is shown in Figure 55. Each candidate epoxy had a 1 inch sample fabricated and the measured CTE of each is shown in the plot of Figure 56.

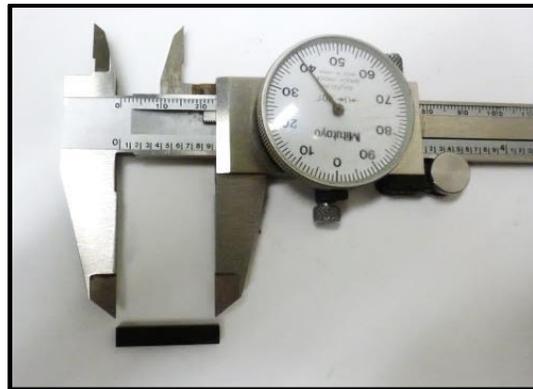


Figure 55: Epoxy bars cast in 1 inch sample sizes for Orton pushrod dilatometer testing.

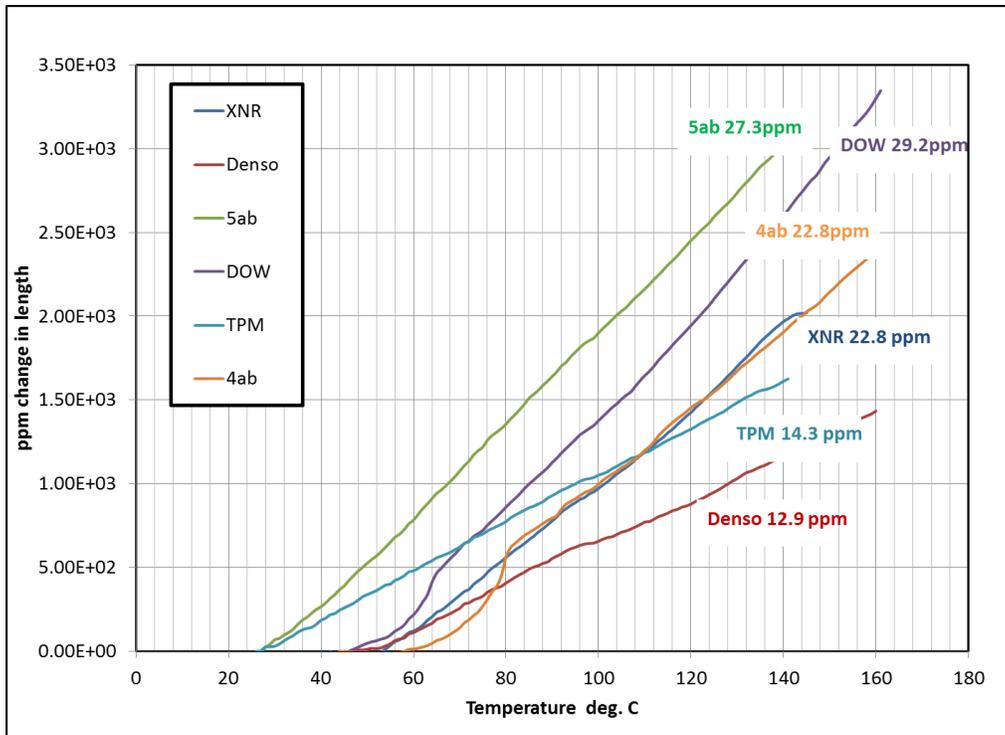


Figure 56: A comparison plot summarizing CTE measurements for each candidate epoxy formulation.

The glass transition temperature (T_g) of the material under test can also be seen in the data as a change in slope. During the glass transition, the epoxy will lose structure and soften. The push rod will then be allowed to deform the material and this is seen as a large change in length or a very positive slope. The glass transition regions for each candidate epoxy can be clearly seen in the plot of Figure 57.

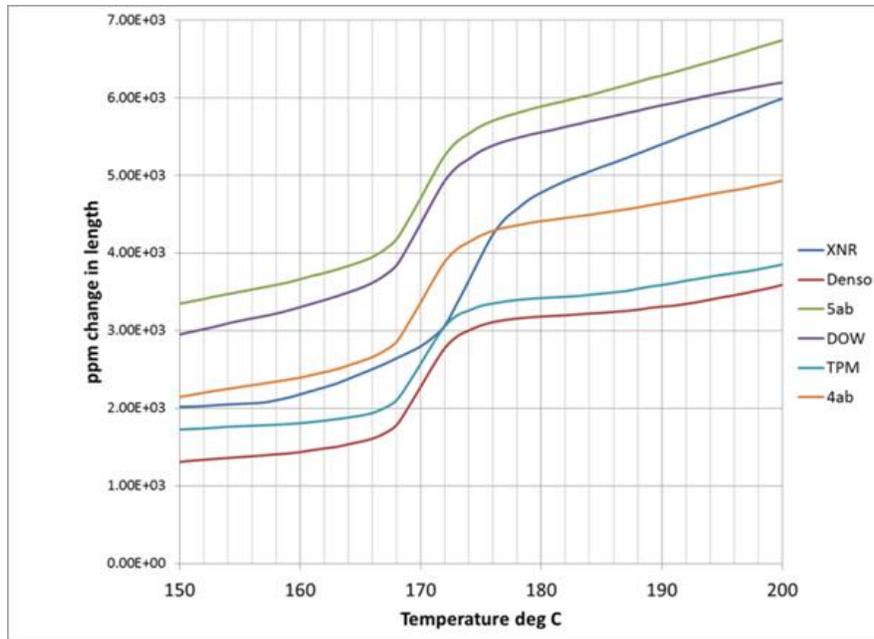


Figure 57: The glass transition (shown as large slope change) of each candidate epoxy.

The onset of T_g and the CTE of the six available epoxy candidates were tabulated for material selection. A summary of the data is shown in Table 22 along with a comparison of how the CTE of the epoxy fairs with the CTE values found in the proposed module system. The XNR formulation revealed the highest T_g and its CTE more closely matched that of the silver tubes in the compliant interface. These parameters will be used for FEA simulations which include encapsulation. The CTE can be assumed to be linear above and below the glass transition temperature [72]. Based solely on CTE, this formulation should result in less thermomechanical stresses within the interface and allow operation to 175°C.

Table 22: The measured CTE and glass transition temperature (T_g) of each candidate epoxy and how it compares to the CTE values present in our proposed system.

Encapsulation Candidates	Measured CTE (ppm/K)	Glass Transition Temperature Range (T_g) °C	Δ CTE (compared to Ag 19 ppm/K)	Δ CTE (compared to DBC 6.0 ppm/K)
XNR	22.8	172-176	+3.8	+16.8
5ab	27.3	166-174	+8.3	+21.3
4ab	22.8	168-174	+3.8	+16.8
Denso	12.9	166-174	-6.1	+6.9
Dow	29.2	166-174	+10.2	+23.2
TPM	14.3	166-174	-4.7	+8.3

3.6.2. Encapsulation Processing and Integration

For module encapsulation, the two part thermoset epoxy from Nagase Chemtex was chosen. The epoxy, called XNR, has a recommended mixing ratio of 100% XNR5021 (black) to 85% XNH5021 (white). The two parts were mixed thoroughly before application. The opening between top and bottom substrates in both the quarter-bridge and half-bridge modules is large enough that epoxy was added using a miniature syringe. The epoxy is added with syringe to the opening in one side of the module and held on its side until it travels through the tube interface to the other side. A graphical representation of the encapsulation process can be seen in Figure 58.

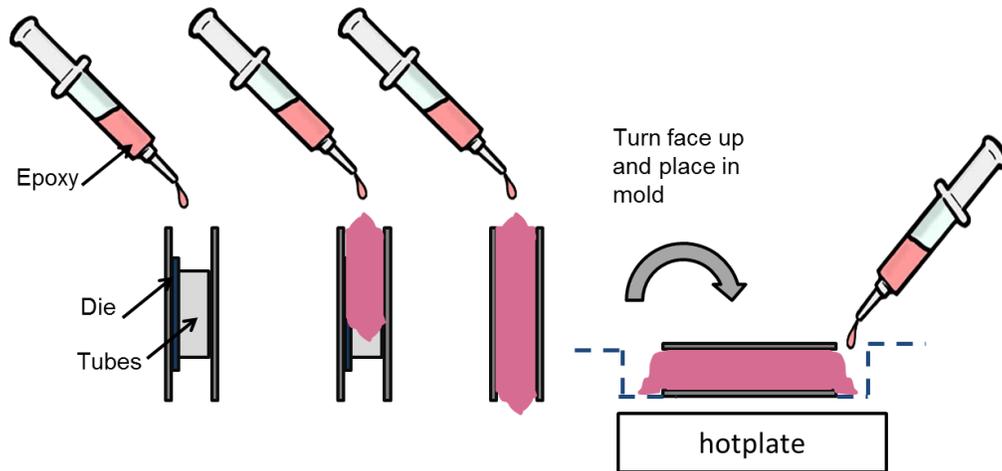


Figure 58: Workflow of encapsulating both the quarter-bridge and half-bridge modules using XNR two part epoxy.

The modules are then placed into a flexible silicone mold (Figure 59). The mold is made from a high temperature chemical resistant silicone, Silpak 2374 and is placed onto a thin piece of aluminum for good heat transfer to the bottom of the module.

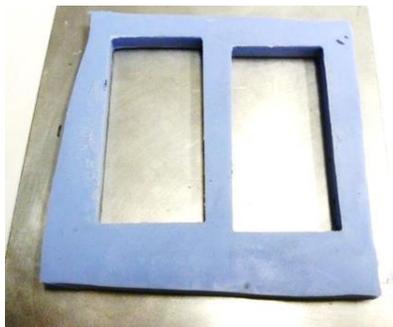


Figure 59: Flexible silicon mold fabricated for curing the encapsulated module.

When the epoxy is warmed the viscosity is reduced and more epoxy is added as needed to cover the edges of the top substrate. The curing profile for XNR requires 1 hour at 100°C and an additional 3 hours at 150°C. Epoxy cannot be added after the module has been at 100°C for more than 30 minutes.

Chapter 4. Module Characterization and Testing

4.1. V-I Testing

One of the most referenced electrical parameters of semiconductor devices is the relationship between the direct current (DC) and the applied voltage. A range of pulsed voltage is applied to a device and the resulting current is measured. The dependent variable is the current (I) and the voltage (V) is the independent variable. For this reason, the output is referred to as a V-I curve or trace. The V-I characteristics can be used to determine the turn on voltage (in the case of a diode) or transistor output as a function of gate bias. For the transistor, the output curves as a function of gate bias makeup a V-I family of curves. A linear segment of a measured curve can be used to determine resistance by simply using Ohm's Law.

4.1.1. Experimental Setup

V-I measurements for electrical characterization are performed on a Tektronix 371A High Power Curve Tracer with a probe station (Figure 60). A four point Kelvin sensing arrangement was utilized for removing the added resistance from the measurement leads.

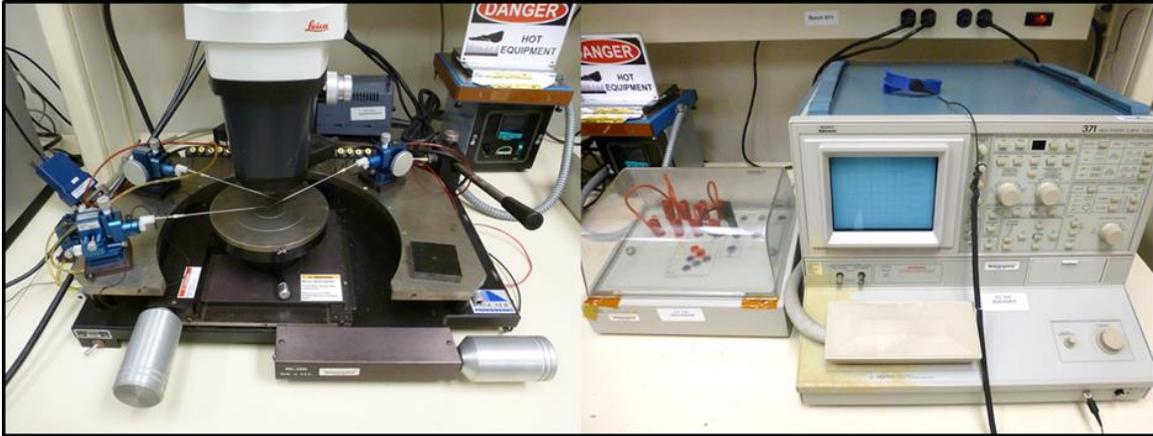


Figure 60: Tektronix 371A High Power Curve Tracer with a probe station for measuring a range of packaged and unpackaged devices.

When using Kelvin sensing it is important to place the sensing leads as close to the die as possible. With the probes station and probes available, the probes can be used as sensing leads and placed within the unencapsulated double-side package.

For testing the V-I characteristic curves of the IGBT, a double-side package of a single device was constructed without encapsulation to allow easy placement of leads and reduce unnecessary contributions from excess packaging. For assessing the diode V-I characteristics, the double-sided diode packages from thermal cycling experiments were measured. Of these eight samples; four were packaged in encapsulation and four were packaged without. The sensing leads for the encapsulated samples were placed as close to the encapsulation as possible.

4.1.2. Results

The V-I characteristics of the double-side packaged IGBT (red) can be seen in Figure 61. The V-I curve for the same device before packaging is plotted on the same graph for comparison. These two measurements are in close agreement and reveal no additional resistance from either the sintered silver area connection of the silver tube interface.

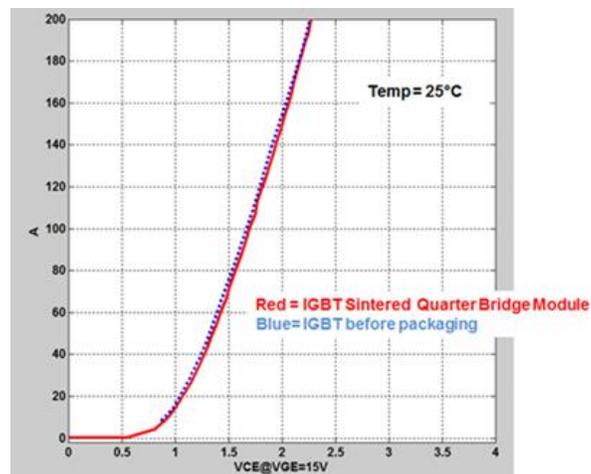


Figure 61: V-I measurements of the IGBT before and after packaging.

The V-I characteristics of all the diode packages are plotted together in Figure 62. The datasheet V-I characteristics are included for comparison. Each sample is in close agreement with the datasheet value and reveals no added package resistance. Four of the eight samples are also encapsulated and has no effect on the resulting V-I characteristics.

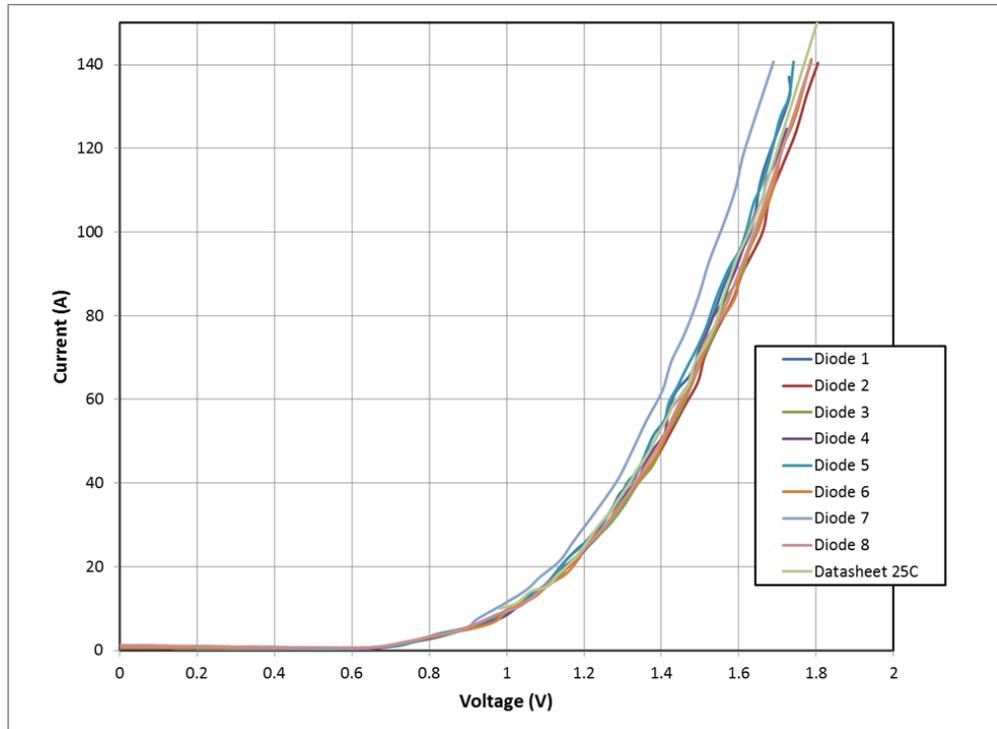


Figure 62: V-I measurements of encapsulated and unencapsulated diode packages overlaid with datasheet values for comparison.

4.2. DC Power Stage Testing

V-I measurements are done with a curve tracer because the curve tracer applies pulsed DC voltage rather than continuous DC voltage. The pulsed measurement is done to avoid device self-heating from conduction losses in the device. If device self-heating is required, as in the case of power cycling, a continuous DC power stage is recommended.

The goal of this testing is to purposely stress the device and the interconnection through device self-heating. The heating at the junction of the device creates high thermomechanical stresses

directly above and below the device. The tests are done without encapsulation to find the true bond integrity. It is easier to visualize the extent of junction stresses by looking at the expected change in length of the bonded components with the temperature changes experienced during the DC power test (Table 23).

Table 23: Comparison of material change in length based on the CTE of the material and the temperature experienced in the DC power stage test.

Material	CTE (ppm/K)	ΔT (during power cycle)	ΔL
IGBT (Silicon)	2.34	175°C	4.0 μm
Diode (Silicon)	2.34	115°C	2.7 μm
Sintered Silver	19.0	175°C	33.3 μm
Alumina DBC	6.0	155°C	9.3 μm

4.2.1. Experimental Setup

A DC power stage test system was constructed in the laboratory for proper evaluation of the module using high current. This DC power stage consists of a high current, low voltage DC power supply connected directly to the device under test (DUT) which is mounted to a finned heat sink. For an IGBT, a separate 15 V power supply is required for switching the device on (+15 V) and off (0 V). For diode conduction the forward voltage is increased until the diode conducts (+0.7 V to 0.9 V). To allow for easy data acquisition, a 4 channel Data Acquisition (DAQ) is used. A schematic of the circuit with the DAQ channels is shown in Figure 63.

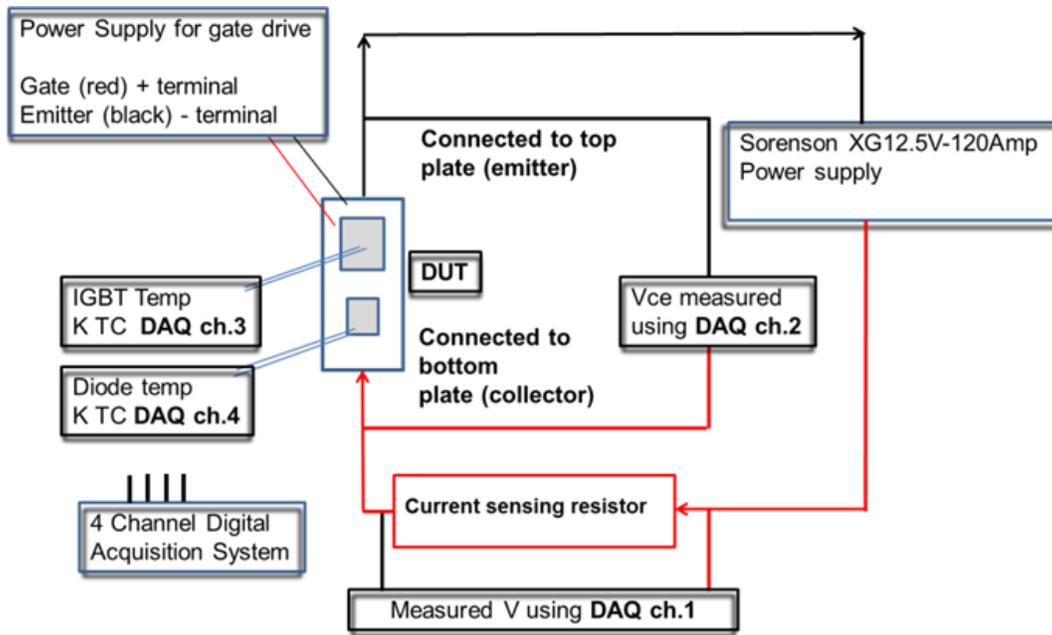


Figure 63: Schematic of the DC power stage test showing data collection points.

Accurate junction temperatures are normally difficult to sense in a double-side package because the junctions are inaccessible. To overcome this obstacle, the temperature of the IGBT (channel 3) and the diode (channel 4) are monitored by placing fine gauge thermocouples directly into the tube which have been bonded to the top of the chips. The current is monitored using the voltage drop across a current sensing resistor (channel 1). And finally, the voltage across the terminals is measured on channel 2 of the DAQ. Because the freewheeling diode is anti-parallel to the IGBT, the positive and negative terminals are switched for testing the diode.

A picture of the custom fabricated DC power stage is shown in Figure 64.

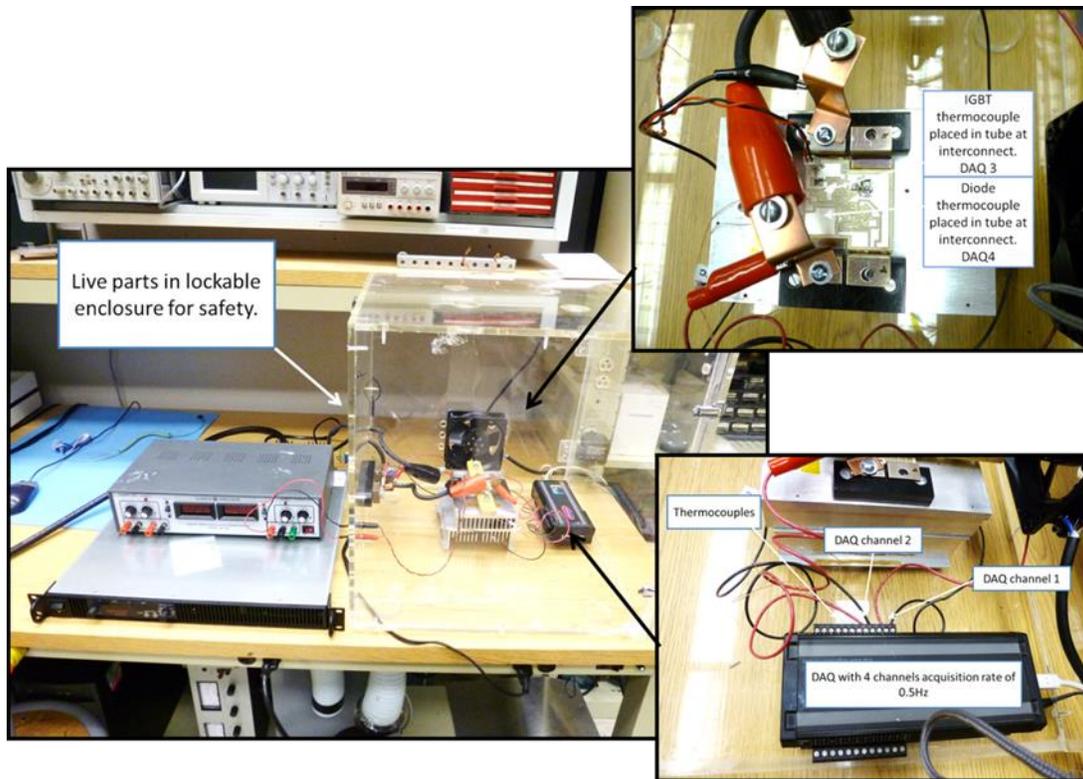


Figure 64: Custom fabricated DC power stage test system for testing both quarter and half-bridge modules.

4.2.2. Results

For each fabricated module, a standard device operation experiment is made using constant currents to at least 60 Amps. For a half-bridge configuration, this results in four tests; two for the IGBT and two with the current reversed for measuring the diodes. The measured data which is characteristic of every half-bridge test is shown in Figure 65. The output can roughly be compared to the datasheet V-I curves, but device self-heating will change the resistance values very quickly resulting in continued change of slope.

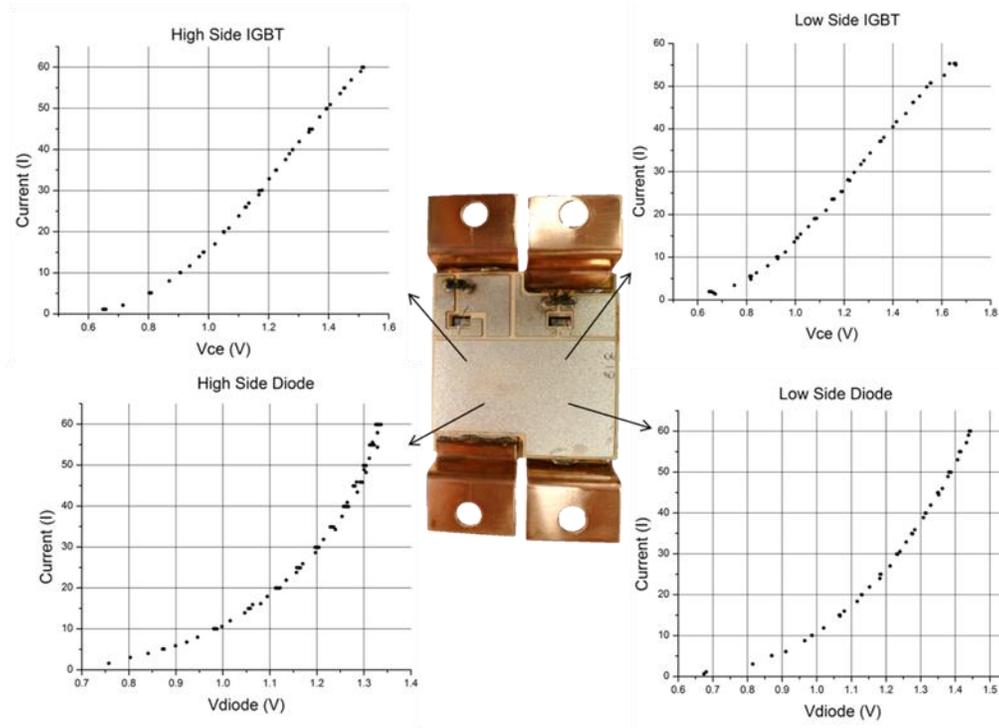


Figure 65: V-I output of each device in a half-bridge module using DC power stage test system for inducing device self-heating.

However, the goal of the test is to thoroughly stress the junction interconnect with high device self-heating. Temperature and applied current output for a test which raised the IGBT junction to temperatures of 200°C can be seen in Figure 66. Current was gradually ramped until the IGBT reached 200°C. In this experiment, 90 A DC was used to heat the device and junction and didn't result in device or package failure.

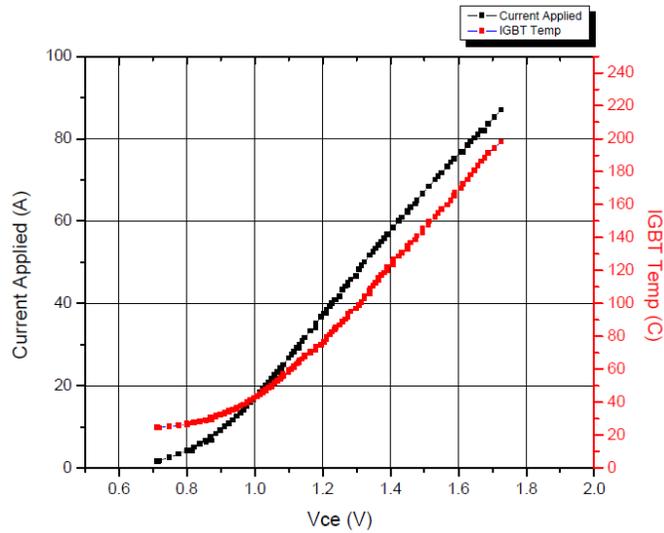


Figure 66: The recorded IGBT junction temperature under a constant 90A DC current.

Experimental results from endurance experiments forced the IGBT to maintain 200°C for a period of 90 minutes. The results of the experiment can be seen in the plots of Figure 67. Due to changes in the electrical and thermal properties of the system, the current required adjustment to maintain the proper IGBT temperature. This is seen in the left plot of Figure 67. The temperature results of both the IGBT (red) and diode (black) can be seen in the right hand plot of Figure 67.

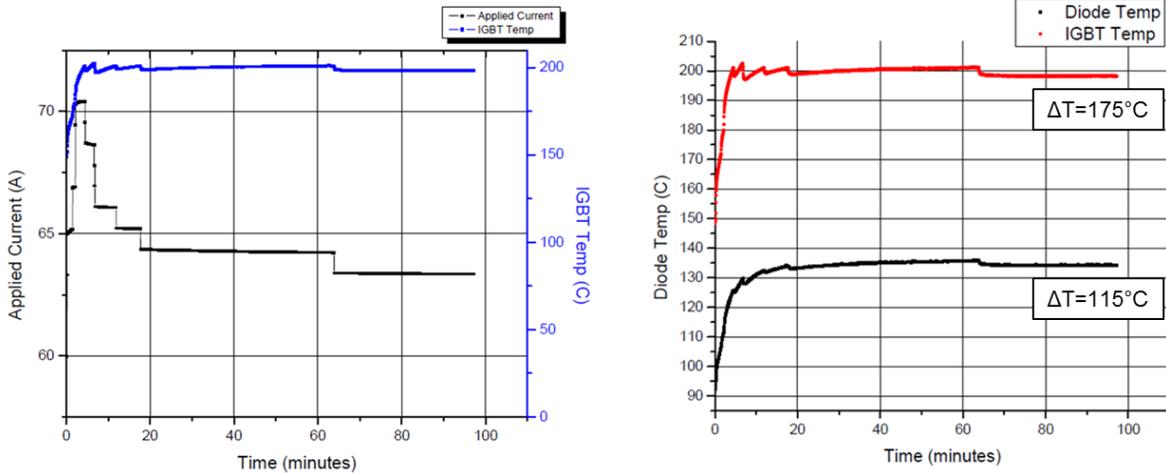


Figure 67: (left) An IGBT held at 200°C for 90 minutes using applied DC current; (right) The temperature differential in the package during the constant temperature IGBT test.

4.3. Double Pulse Testing

In industry power modules undergo basic electrical tests in an effort to assess how the module will perform. Two of the most common testing scenarios are static (DC power stage) and dynamic (AC switching) electrical tests. The additional tests, Safe Operating Area (SOA) and short circuit tests are done on a random basis. [4] The AC switching test is sometimes referred to as a double pulse test. The dynamic test is especially important because it relates directly to the switching loss of the IGBT but doesn't require populating a full inverter for testing. It can also be useful in determining package parasitic inductance, resistance and capacitance [75, 78].

The measurement utilizes a half-bridge module or one full phase leg. One side of the module, high-side switch or low-side switch, is tested at any one time. In the schematic in Figure 68, the low-side IGBT is being driven by an arbitrary function generator. An inductive load is placed across the high-side IGBT for this test. A voltage is applied to the low-side IGBT allowing the

inductive load to charge to the full testing current. When the IGBT is quickly turned off, the inductive load discharges through the diode in the high-side switch. This discharging gives the freewheeling diode its name. The IGBT is then turned back on quickly. The turn-off and turn-on characteristics are used to determine useful switching characteristics like rise time (t_r), fall time (t_f), turn-on loss (E_{on}), turn-off loss (E_{off}), turn on delay time ($t_{d\ on}$), turn off delay time ($t_{d\ off}$), and total energy loss (E_{tot}).

4.3.1. Experimental Setup

A double pulse testing setup was custom fabricated for these measurements. The test voltage and current for this measurement was 600 V and 150 A. These were chosen primarily for comparison against data sheet values. Although, most often dynamic switching tests are performed at half the rated voltage and the full rated current. The first pulse duration in the switching test is chosen based on the inductive load (0.22 mH) applied (plus any parasitic inductances in the system) and the time necessary to charge the inductive load to the proper testing current (150 A). For our system, the first pulse time was experimentally determined to be 36 μ s. The following off pulse time and on pulse time were fixed at 10 μ s each. A schematic of the test circuit is shown below in Figure 68. The low-side switch is being driven in this schematic requiring the high-side gate-emitter connection to be shorted (not shown).

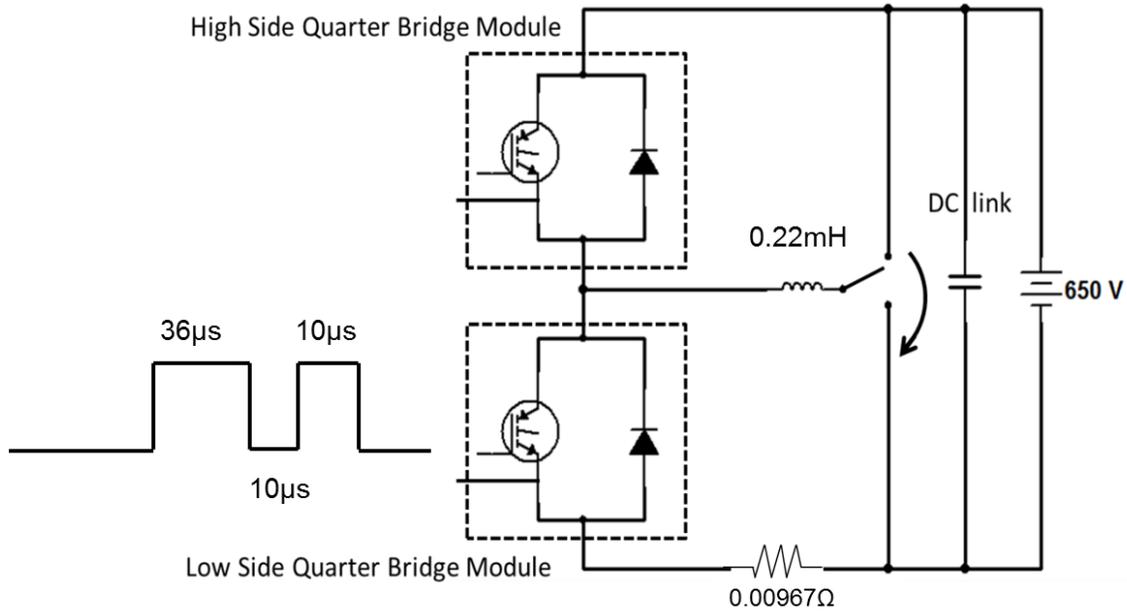


Figure 68: Double pulse test system electrical schematic.

Because the free-wheeling diode of the high-side of the phase leg is necessary for testing the low-side, and vice versa, it was necessary to combine two quarter-bridge modules for testing. The quarter-bridge testing configuration is shown in Figure 69 below.

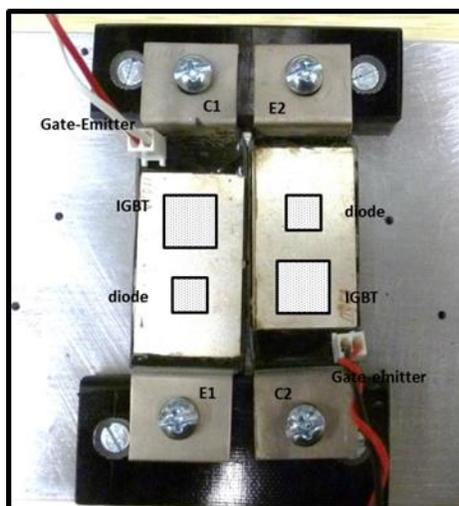


Figure 69: Two quarter-bridge modules arranged in half-bridge configuration required for dynamic switching characterization.

A 1000 V, 2 mA DC power supply was used for supplying the DC link voltage. A separate dual channel power supply was used for powering a commercial Powerex BG2C gate driver (5 V) and supplying the voltage for the IGBT gate signal (15 V). The IGBT driving signal was supplied with a programmable arbitrary waveform generator. A DC choke coil with 0.22 mH of inductance was chosen for the inductive load. All measurements were taken using a Tektronix 500 MHz oscilloscope. The collector current (I_c) which was measured using the voltage drop across a shunt resistor (0.00967 Ω). A decoupling capacitor is connected between the capacitor bank across the DC power supply and the DUT. The connection length was minimized and a flat circuit profile was constructed in an effort to reduce undesirable circuit inductance. Images of the experimental test system are shown in Figure 70.

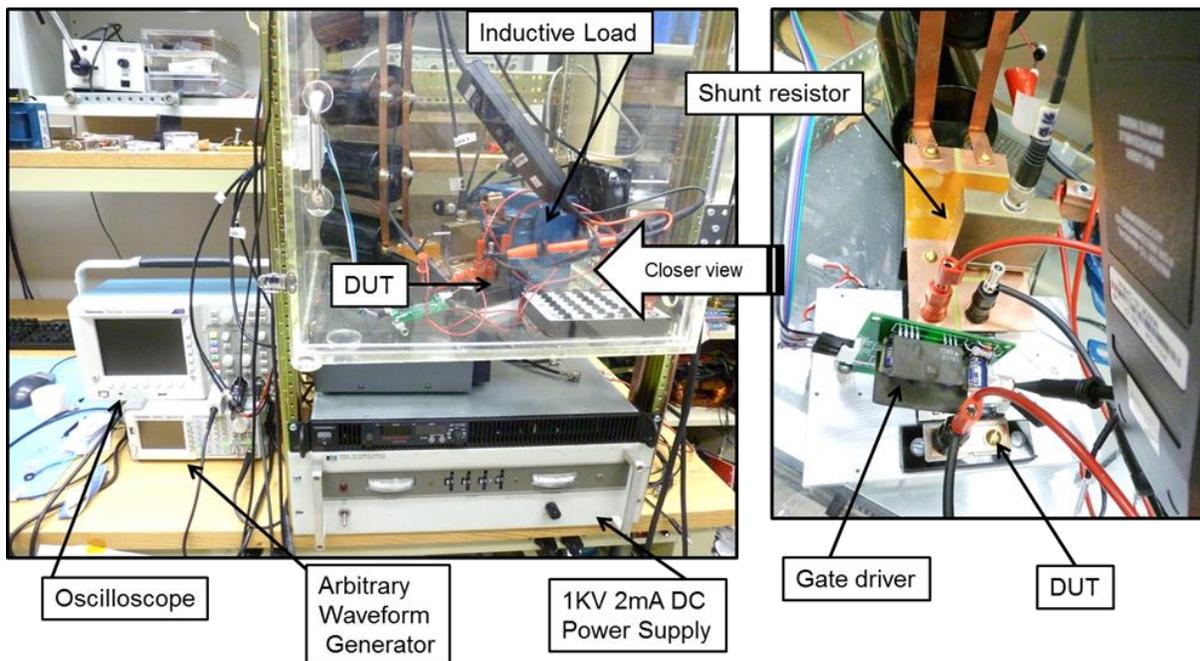


Figure 70: Images of the complete double pulse test system and components.

Industry standard methods of determining the dynamic characteristics are referenced when analyzing the resulting waveforms. After recording the entire pulse pattern, the test is repeated and resolution is increased to take snapshots of data bounded by the dotted red line. The two signals of interest are the turn-off and turn on waveforms.

When the resolution is increased, the waveforms will resemble the waveforms in Figure 71. The waveform in the left is the turn-on waveform and the right picture shows the turn-off waveform [78]. The diagrams are marked with the pertinent industry standard boundary values. The turn-on loss (E_{on}) is calculated by integrated the power dissipation ($V_{ce} * I_c$) in the time period bounded by 10% of collector current and 5% of the total V_{ce} as shown in the left diagram of Figure 71. The turn-off loss (E_{off}) uses a similar approach by integrating power ($V_{ce} * I_c$) in the time bounded by the values marking 10% of the total V_{ce} and 5% of the total I_c (right image of Figure 71). The losses are plotted for both scenarios at the bottom of the diagrams in Figure 71. The total switching loss is the sum of E_{off} and E_{on} .

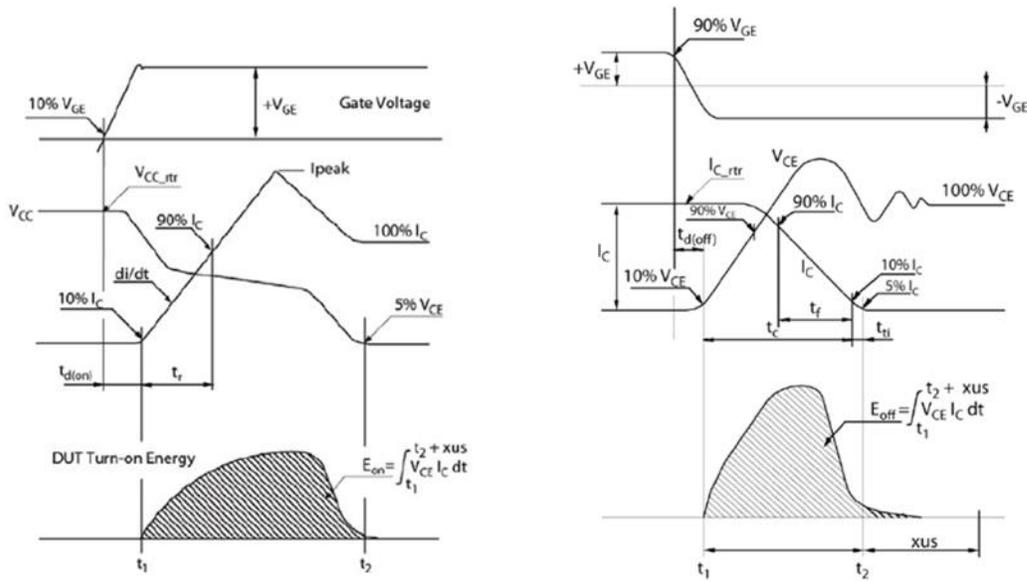


Figure 71: Guidelines on industry standard boundaries for calculating turn off energy loss (E_{off}), turn on energy loss (E_{on}), rise time (t_r), fall time (t_f), turn on delay time ($t_{d on}$), and turn off delay time ($t_{d off}$). ([78] "IGBT Applications Handbook," vol. HBD871/D, O. Semiconductor, Ed., 2 ed. www.on-semi.com: On Semiconductor, 2012.) Used under fair use, 2014.

Other values for comparison to datasheet values are fairly straightforward. The rise time (t_r), fall time (t_f), turn-on delay time ($t_{d on}$), and turn-off delay time ($t_{d off}$) can be read directly from the measurement data.

4.3.2. Experimental Results

A benchmark module containing similar rated ABB devices in two device quarter-bridge configurations or four device half-bridge configurations are not available. To test the testing setup, a commercial 150 A 1200 V Powerex half-bridge module (CM150U-24NFH) was measured. The results of the turn-off (right) and turn-on measurements (left) for the commercial module at 600 V and 150 A are shown in Figure 72. The switching energy loss plot is shown in

the inset of each plot. The turn-on loss (E_{on}) was measured at 2.68 mJ and the turn-off loss (E_{off}) was measured to be 6.97 mJ. These measurements closely match the datasheet values for the power module. The voltage overshoot measured (right plot of Figure 72) is approximately 220 V.

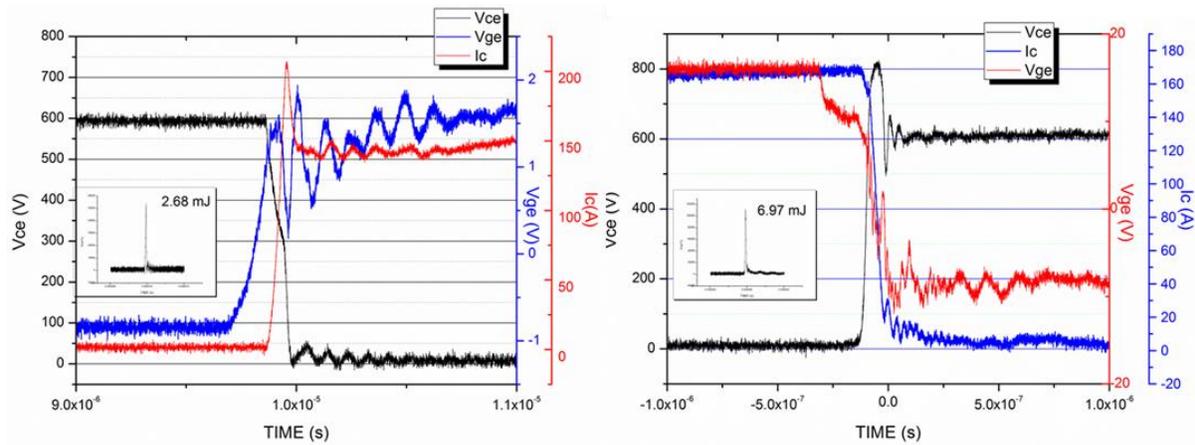


Figure 72: The measured turn on (left) and turn off (right) switching characteristics of a commercially available Powerex module using 600V and 150A.

A comparison of the other datasheet quantities compared to the experimental quantities measured using the custom test setups are shown in Table 24.

Table 24: Comparison of Powerex datasheet values with measured values from the custom fabricated test setup.

Powerex Datasheet		Test Fixture Measurements	
$t_{d(on)}$	150 ns	$t_{d(on)}$	111 ns
t_r	80 ns	t_r	48 ns
$t_{d(off)}$	400 ns	$t_{d(off)}$	180 ns
t_f	150 ns	t_f	126 ns

The full test at 600 V and 150 A for the fabricated quarter-bridge module in the half-bridge testing configuration is shown in Figure 73.

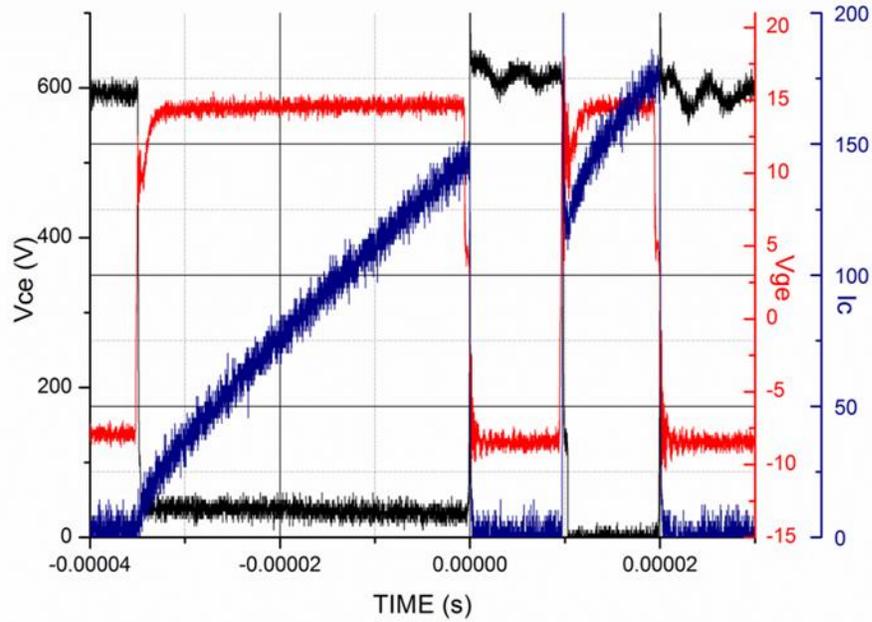


Figure 73: Full double pulse output waveform for one quarter-bridge module.

The turn-off waveform for the low-side quarter-bridge module is shown in Figure 74. The voltage overshoot in the plot is 120 V. The turn-off loss (E_{off}) is plotted in the inset of the graph and was calculated to be 9.03 mJ.

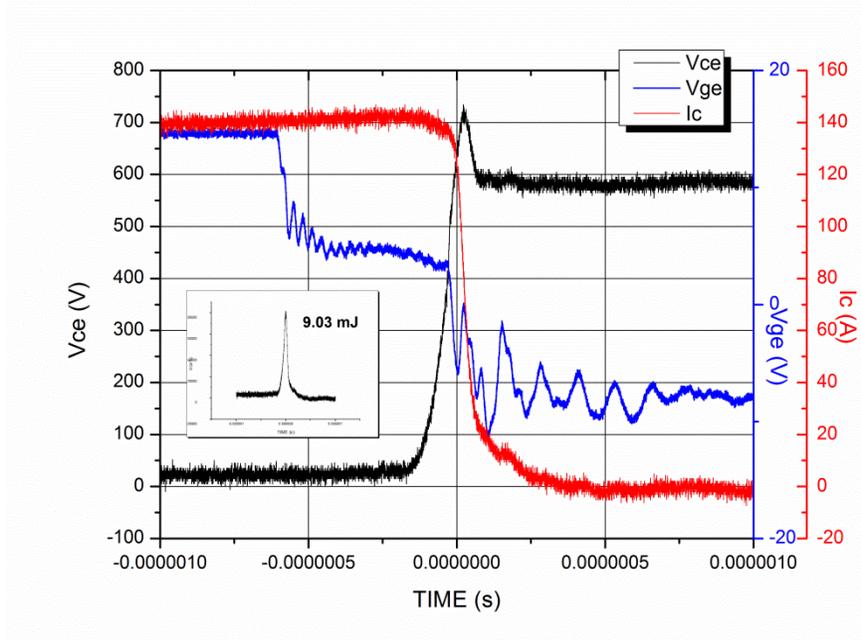


Figure 74: Turn-off switching results for quarter-bridge module in custom test system.

The turn-on waveform for the low-side quarter-bridge module is shown in Figure 75. The turn-on loss (E_{on}) is plotted in the inset of the graph and was calculated to be 6.68 mJ.

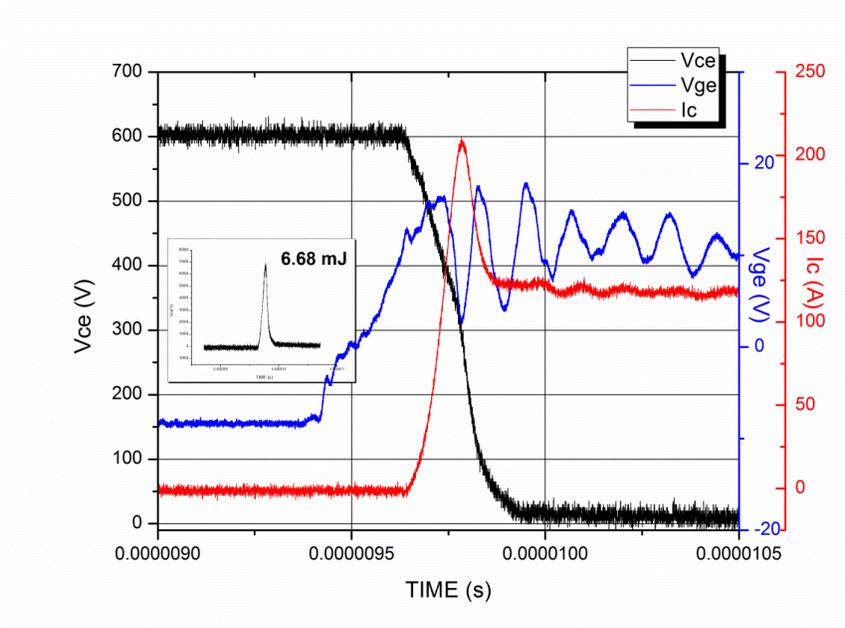


Figure 75: Turn-on switching results for quarter-bridge module in custom test system.

A comparison of the ABB datasheet values and the measured values using the lab test setup are shown in Table 25.

Table 25: Comparison of measured switching characteristics for a packaged quarter-bridge module and the datasheet values provided by ABB, the manufacturer of the devices.

ABB Datasheet		Test Fixture Measurements	
$E_{(off)}$	9.4 mJ	$E_{(off)}$	9.03 mJ
$E_{(on)}$	16 mJ	$E_{(on)}$	6.68 mJ
$t_{d(on)}$	200 ns	$t_{d(on)}$	129 ns
t_r	70 ns	t_r	68.2 ns
$t_{d(off)}$	460 ns	$t_{d(off)}$	460.0 ns
t_f	50 ns	t_f	149.8 ns

4.4. Three-Phase Inverter Integration

The end application for the modules constructed for this study is population of full inverter packages for conversion of high DC voltages (>600 V) to AC output.

4.4.1. Experimental Setup

For this study, a full inverter test bed was created, which would allow easy integration of both full and quarter-bridge module configurations. The base of the inverter is a large heat finned aluminum heat sink with a footprint designed to accommodate three half-bridge modules. The heat sink top was equipped with custom fabricated bus bars for screw connections to the modules. The heat sink was uniformly force cooled using two 12 V DC fans sized for full

coverage of the heat sink volume. The benefit of using double-side cooled modules is that the top surface allows for additional cooling. Therefore, another finned aluminum heat sink is secured to the tops of all the mounted modules. A commercial gate driver board (APS 1491) was purchased from Applied Power Systems. To minimize the length of gate driver connections, the driver board was mounted as close as possible to the top of the modules. Decoupling capacitors were added to the DC input of each phase. The output of each phase leg is accomplished by shorting the high-side emitter connection to the low-side collector. This is accomplished on the output side of the package with added connection for attachment of the load. The total inverter package measures 8 inches wide by 6 inches deep and 8 inches high and can be seen with (left) and without (right) the driver board connected in Figure 76.

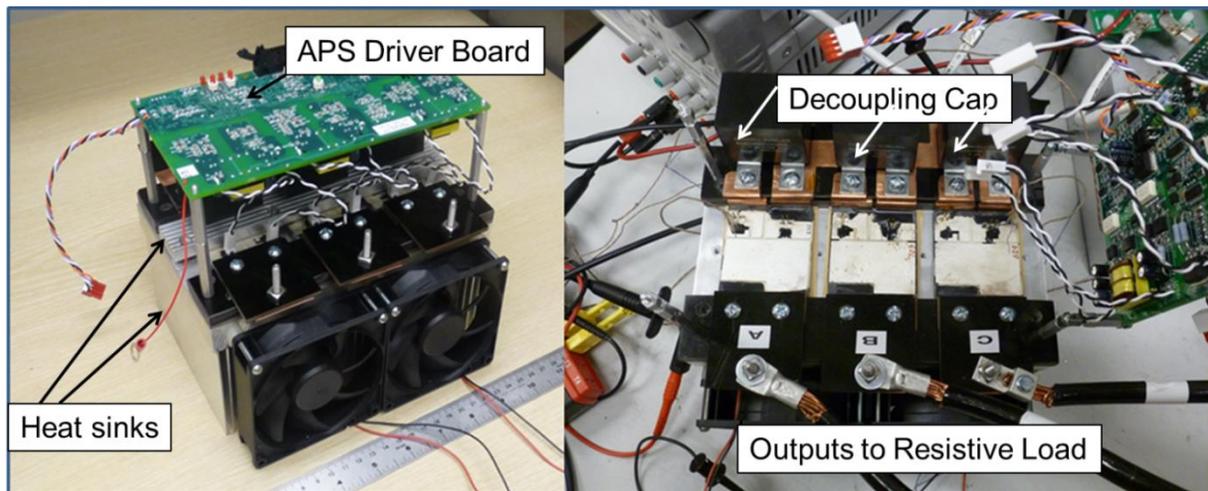


Figure 76: Laboratory constructed inverter package with (left) and without (right) the driver board connected.

The power source for testing the functioning inverter utilizing the double-side cooled modules was a Magna Power 1000 V DC power supply capable of supplying 240 Amps. Two 30 kW fan cooled resistor banks were used for the resistive load. The load was split equally among the three phases. A diagram of the entire system is shown in Figure 77.

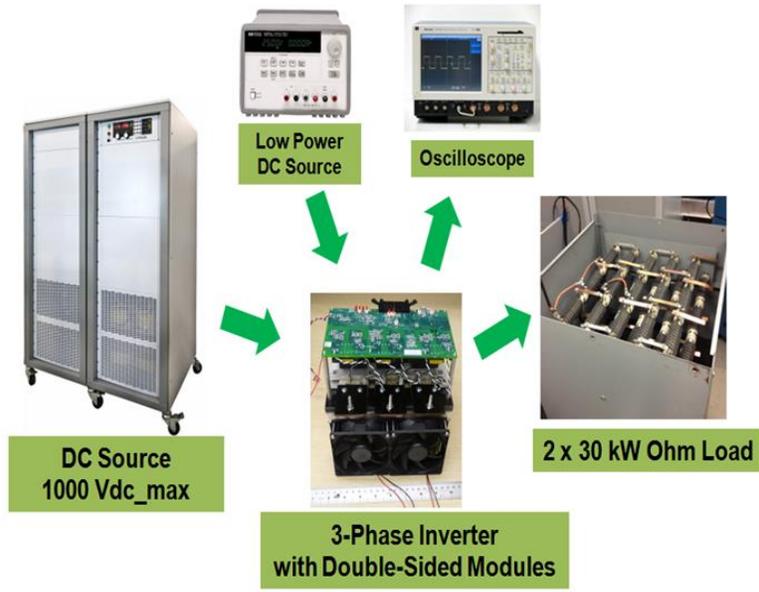


Figure 77: Diagram of the necessary inverter testing components.

4.4.2. Results

For inverter testing, the inverter driver board was driven using a six step waveform at a frequency of 100 Hz. The power supply power was slowly increased collecting a waveform at each interval. The maximum power used was 55,270 W at a voltage of 753 V and a current of 73.4 A. The output at this power is shown in Figure 78.

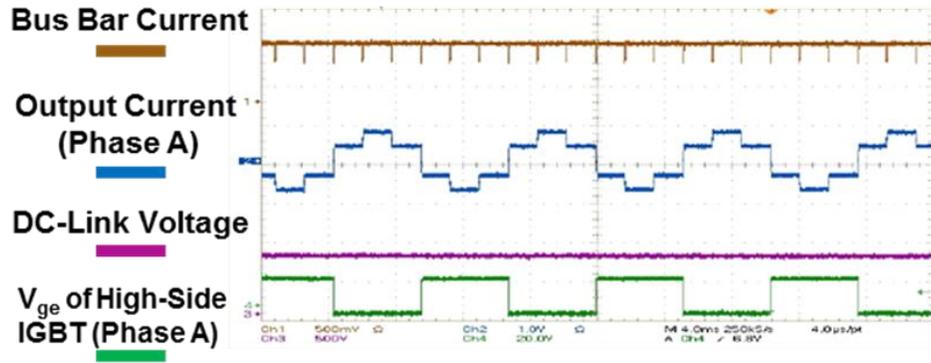


Figure 78: Three phase inverter output using a laboratory constructed inverter populated with three half-bridge modules.

4.5. Thermal Spectrometry Analysis

The steady state thermal characteristics of a power module are the most cited parameter in module datasheets. This parameter, thermal resistance (R_{th}), is important because it establishes the boundary conditions for the application power. The units of thermal resistance are $^{\circ}\text{C}/\text{W}$ or K/W and reflect the temperature increase in the package versus power applied. The temperature references are the junction of the device and the lowest part of the packaged stack, the case, R_{thj-c} . If the junction and case temperature can accurately be measured, thermal resistance is calculated by

$$R_{thj-c} = \frac{T_j - T_c}{P_{applied}} \quad (7)$$

When measuring a packaged semiconductor device, the thermal stack may contain several layers. An example of a common thermal stack with seven materials and six interfaces is seen in Figure 79.

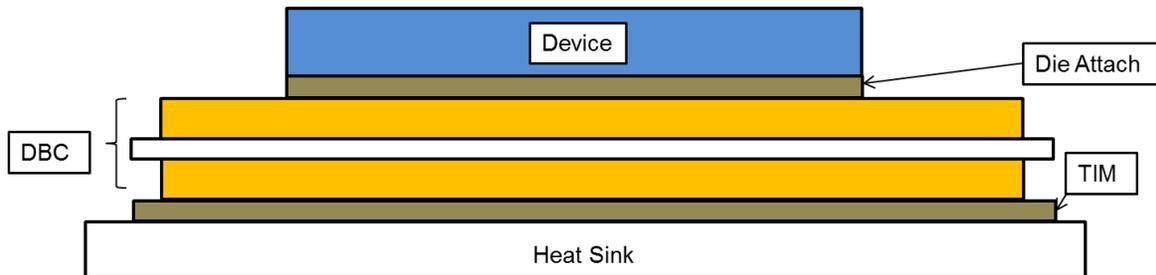


Figure 79: Example of simple stacked structure common in semiconductor device packages.

Because the stack thicknesses are very small in comparison to the area, the thermal path can be approximated with one dimensional heat flow from the junction of the device to the case. [79] One method for the measurement of R_{th} is very similar to the transient thermal impedance measurement which will be discussed in Chapter 5. The temperature of the junction can be accurately monitored using a device electrical parameter which has a linear relationship with changing temperature. This electrical parameter can be measured and compared to the temperature of the case which can be force cooled to maintain a constant temperature. After the temperature reaches a steady state value, the resistance is calculated. Also, similar to thermal impedance, Foster and Cauer networks can be constructed to approximate the thermal resistance and/ or steady state time periods. [79-84]

The difficulty with a one dimensional heat flow assumption is that it assumes planar surfaces in intimate contact. A more intricate structure requires characterization of the anisotropic heat flow. In the case of a double-side cooled structure, multiple cooling scenarios exist and therefore

three possible junction to case quantities can exist. It is no longer straightforward to simply state the thermal resistance of the module. A closer and more thorough understanding of the thermal benefits are researched here.

Thermal spectrometry is a technique for inspecting each stack element through precise measurement of the transient thermal analysis characteristics as the heat flow approaches steady state [79, 80, 82, 85-87]. These measurements are sometimes referred to as heating or cooling curves in commercial settings [4]. The proper measurement and analysis protocols are defined in the JEDEC Standard JESD51-14 [88].

First, a dual interface transient thermal measurement is performed (TDIM). This test is performed by mounting the sample to a heat sink and measuring two times using two different thermal interface materials (TIM). Pressure is applied to the sample to insure the optimum module case contact with the cold plate. The temperature of the case must be kept at a constant value through the entire test. An example JEDEC standard experimental setup is seen in Figure 80.

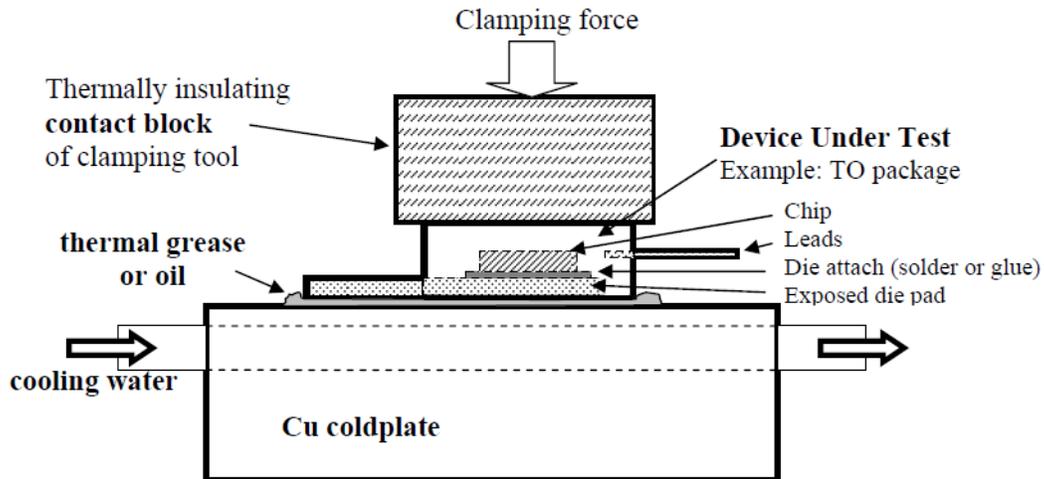


Figure 80: Experimental test setup suggested by JEDEC Standard JESD51-14. ([88] JEDEC, "JESD51-14 Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path," vol. JESD51-14, ed. <http://www.jedec.org/standards-documents/results/51-14>: Joint Electron Device Engineering Council, November 2012, p. 46) Used under fair use, 2014.

The device temperature sensitive parameter (TSP) is again used as a reliable method for measuring the temperature of the junction. The device is used as the heat source and power is applied in discrete accurate steps. The temperature at each step is collected. When plotted on a linear scale, the steady state region is clearly defined. Using discrete power steps, the response can be plotted on log scale to better resolve material responses which would otherwise not be seen at low resolution (Figure 81).

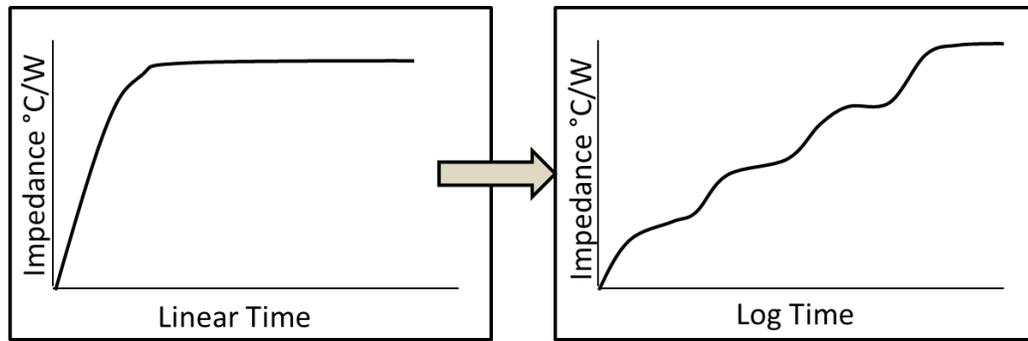


Figure 81: Transformation of linear temperature relationship to log scale which reveals small transitions for each material in stacked structure.

The dual interface method uses the log time data of both measurements to accurately determine the time at which heat reaches the TIM. This can be seen in the graph in Figure 82 which is a plot of a TO-263 package measured with thermal grease (1) and without thermal grease (2). [88]

The separation of the two lines marks the thermal interface layer and the thermal resistance of the package can be calculated at this point. The separation of the two lines is calculated using the difference of the derivatives of the curves. More simply, when the curves are overlapped the heat flow is in a structure that is common to both packages. When the curves deviate, the structures no longer have that material in common. The deviation in this case happens when heat reaches the different TIM layers.

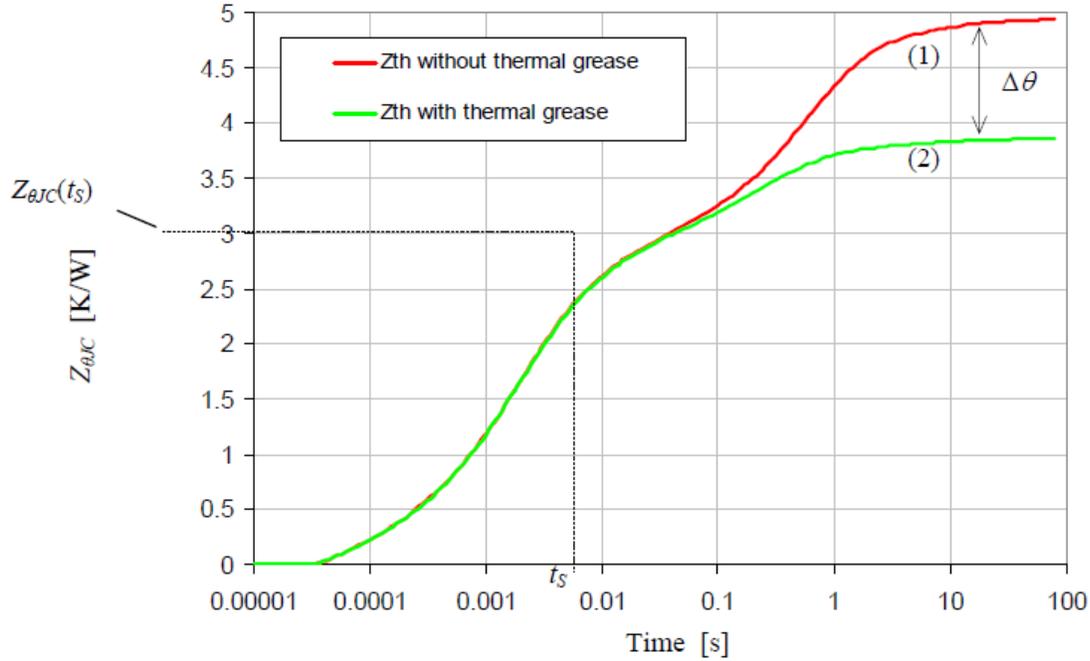


Figure 82: Example measurement provided in JEDEC Standard JESD51-14 for illustrating the thermal resistance calculation of a TO package using dry and wet TIM materials. ([88] JEDEC, "JESD51-14 Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path," vol. JESD51-14, ed. <http://www.jedec.org/standards-documents/results/51-14>: Joint Electron Device Engineering Council, November 2012, p. 46) Used under fair use, 2014.

After data collection and case determination, curves can be used to establish structure functions of the package. Each material, as discussed previously, can be approximated using a one stage RC network. If a power is applied to the RC network of one material its temperature will rise according to

$$T(t) = \Delta P_H * R_{th} * [1 - \exp(-t/\tau)] \quad (8)$$

where

$$\tau = R_{th} * C_{th} \quad (9)$$

Using the heating curve, time constants, τ , can be extracted for each of the materials. These values can be used to build a structure function based on a Cauer RC network model. The Cauer model is preferred because it references a single node rather than the Foster network which assumes node to node heat flow [88].

4.5.1. Experimental Setup

Thermal spectrometry for a double-side cooled power module requires analysis for several different device mounting schemes to thoroughly inspect the material response and hence develop accurate experimental structure functions. These mounting schemes are illustrated in Figure 83. In addition to the standard bottom junction cold plate mounting (a), measurements are required for the scenario in which the top surface is mounted to the cold plate (b). To measure the module as it was intended for application, measurements are taken with both top and bottom surfaces force cooled (c).

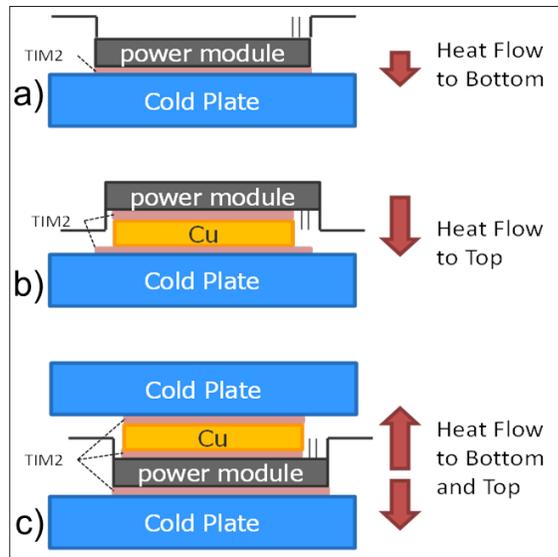


Figure 83: Required measurement configurations for accurate assessment of a double-side cooled package.

For measuring the module using JEDEC Standard JESD51-14, a thermal transient system called T3Ster from Mentor Graphics was used with T3Ster Master Software. Additional thermal FloTHERM Computational Fluid Dynamics (CFD) software tools were used for thermal characterization. The T3Ster system was specifically designed to implement the JEDEC standard JESD51-14 static test (or continuous measurement) method.

The module is placed on a cold plate which maintains a constant temperature. Two different thermal interface materials (TIM) are placed between the chilled plate and the module; LF200 (dry) and Silicone (wet). The module is forced onto the cold plate using a pressurized piston (Figure 84). The temperatures were measured using the changes in collector-emitter voltage which has a linear relationship with temperature. The sensing current for this test is 500mA (rather than 2-8 mA for the thermal impedance test setup). The power levels required to heat the

module to 155°C were on the order of 300 W or above. The test setup with the electrical parameters is shown in Figure 84.

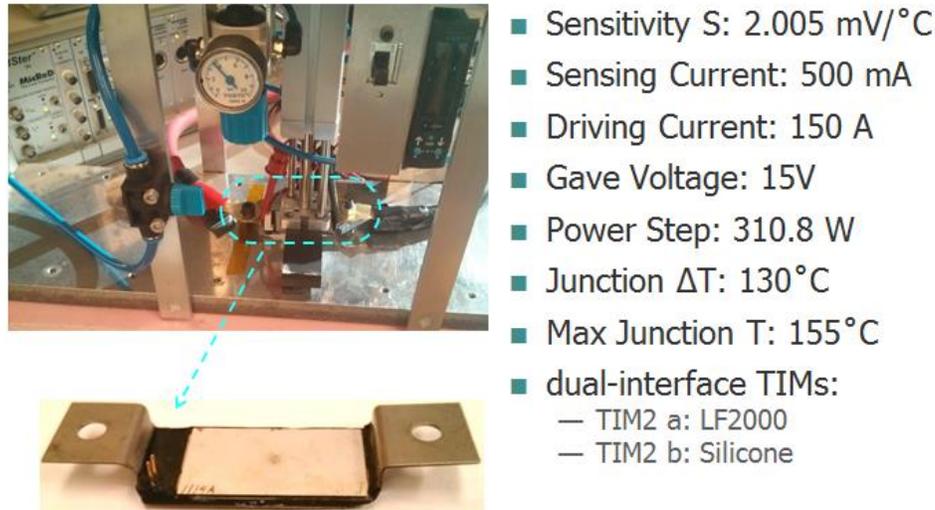


Figure 84: Test setup used by Mentor Graphics for testing the double-side cooled power module referring to JEDEC standard JESD51-14.

4.5.2. Results

Characteristic cooling curve profiles for the bottom cooled testing configuration experiment using both TIMs are shown in Figure 85. Several tests were performed to determine the testing variability. These tests are repeated for each of the three cooling configurations. The overlapping curves show the repeatability of the two scenarios. The curves for the LF2000 (top) and the silicone (bottom) converge finally at the lower end of the temperature scale.

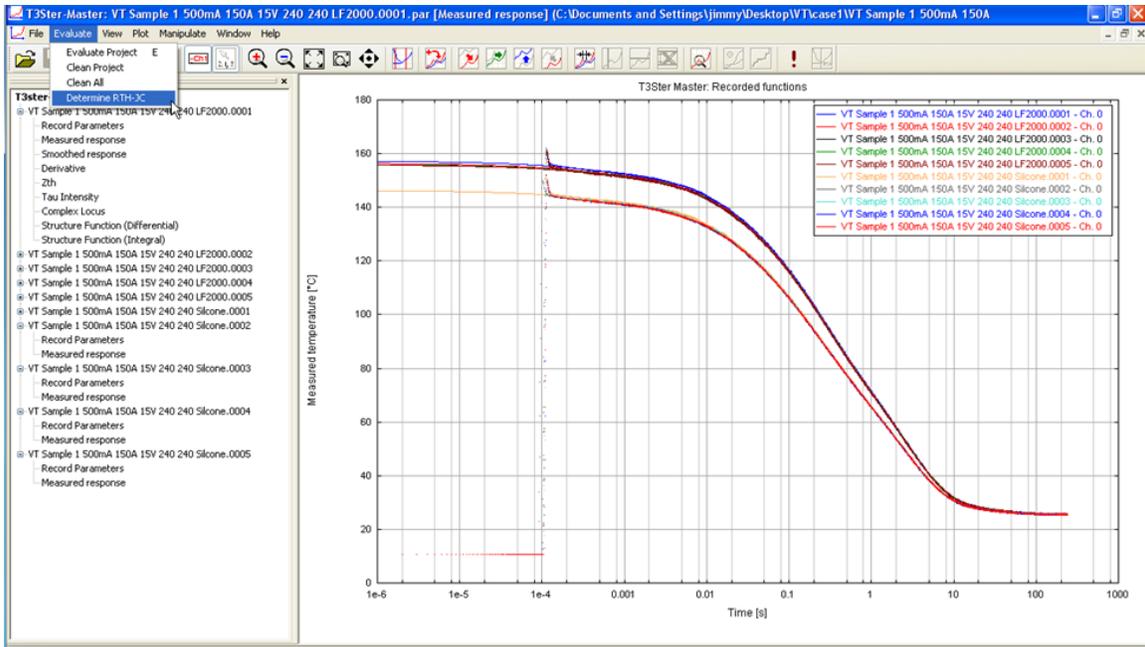


Figure 85: Repeatability testing results of the quarter-bridge module using the dual interface test method.

The transient cooling curves for each of the three cooling configurations are summarized in Figure 86. The power used to heat the module was the rated device power of 150 A in each case except the case in which only the top of the device was being cooled. The die temperatures were much higher at a reduced power in this configuration because of the added tube compliant layer between the die and the top substrate. The power of each test and the maximum active die temperature is shown in Figure 86.

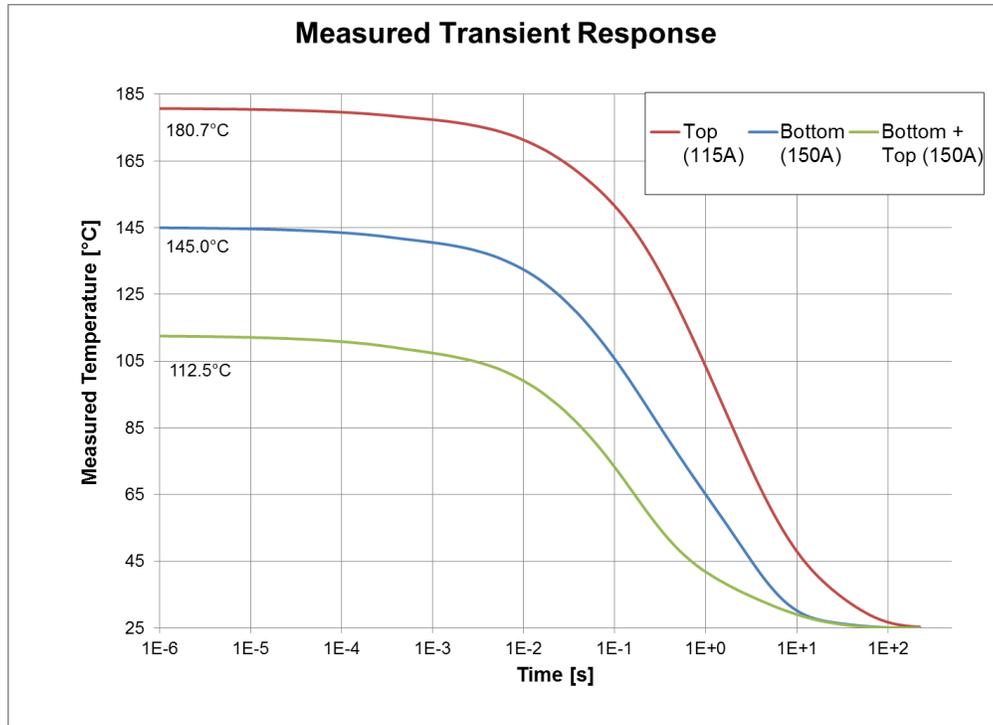


Figure 86: Transient cooling curves and the power settings used for heating of each of the three possible module cooling configurations.

The measurements were post-processed with the Mentor Graphics T3Ster Master software, which computes the structure functions and determines the junction-to-case thermal resistance, R_{thJ-C} . The structure function is a graphical representation of a heat flow path and is computed by de-convolution of the thermal impedance transient to an RC (resistor and capacitor) network model (time constant or frequency domain). This function is represented as a curve plotted on thermal resistance (K/W) and thermal capacitance (W•s/K) axes (Figure 87). Where the curves overlap, the structure is common to both tests. The separation of the curves marks the point in the stacked structure where the thermal path has been altered by a layer with different thermal impedance. This divergence marks the point at which the heat flow has reached the case of the module.

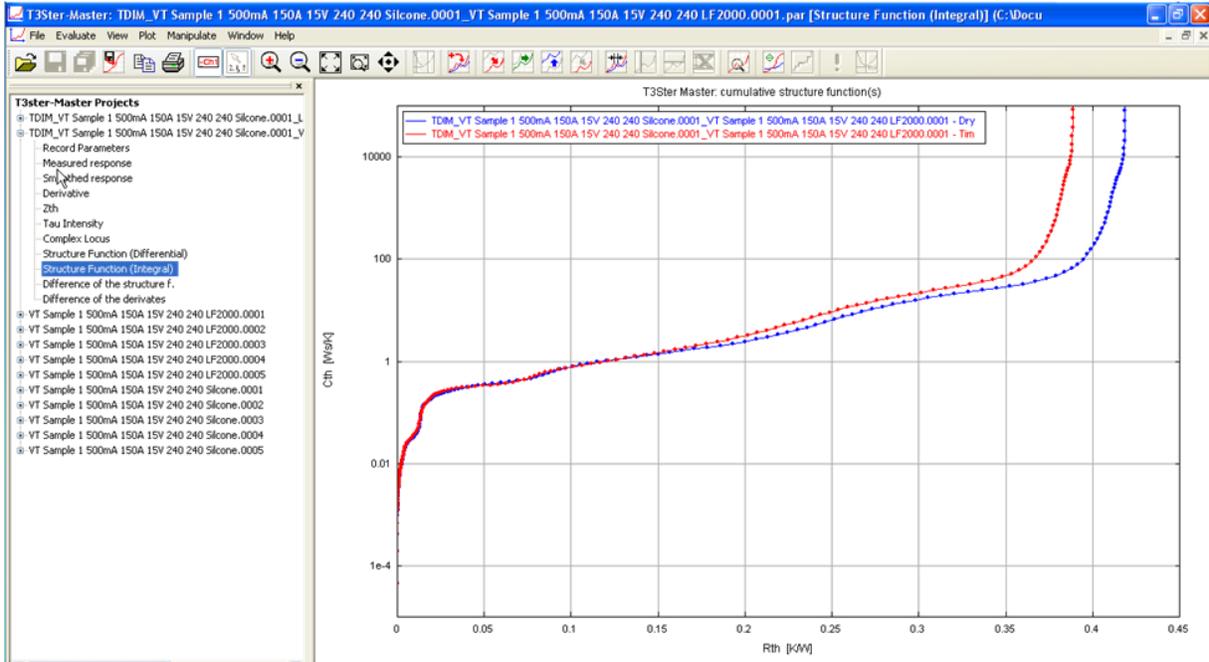


Figure 87: Characteristic thermal impedance curves for the wet and dry interface material. The point at which the two curves diverge is used to determine the case of the module.

At the divergence point, or case, the thermal resistance can accurately be measured. The thermal resistance in the bottom cooled configuration calculated at the curve divergence point is 0.126 K/W.

This technique was reproduced for each of the transient cooling curves which results in three R_{thj-c} values; one for the top, one for the bottom and one for both. Plots of all three deconvoluted transient structure function curves from Figure 86 are shown in Figure 88.

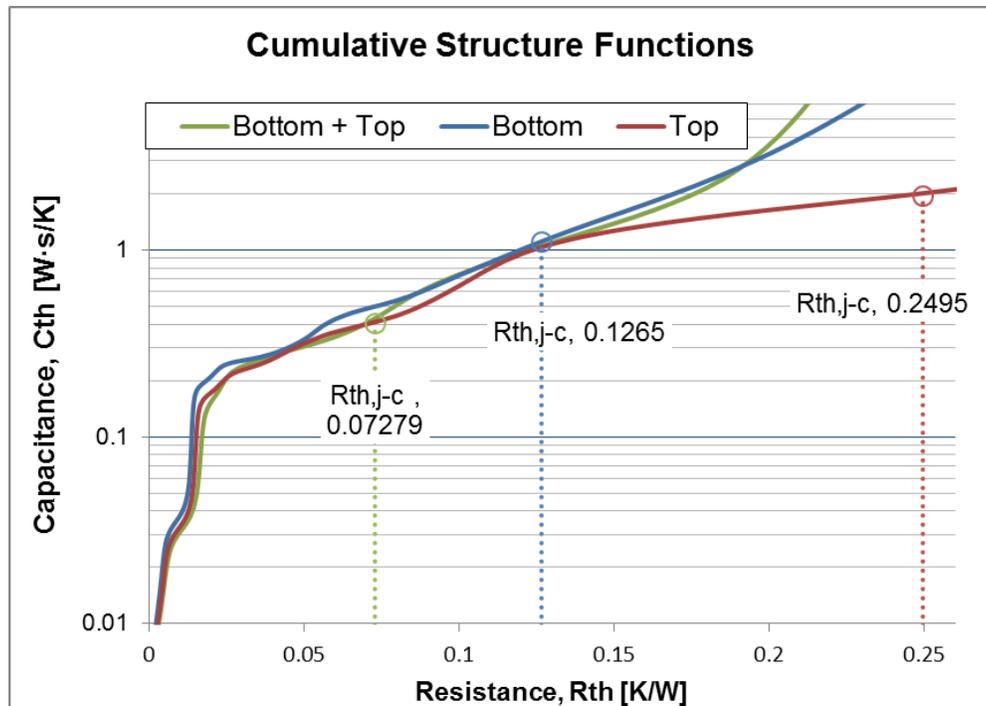


Figure 88: Experimentally measured structure functions for each of the three possible cooling scenarios for the double-side module.

The plots in Figure 88 show the differences in measured $R_{th,j-c}$ for each cooling scenario. The highest thermal resistance exists when only the top of the device is cooled. The asymmetrical design and location of the compliant layer is obvious when comparing the bottom and top thermal resistance values. If the module thermal characteristics adhered to the Cauer RC network model for one-dimensional heat flow then the double-side cooled scenario could easily be calculated using parallel resistances. This calculation was performed on the modeled data in Chapter 2. The calculated $R_{th,j-c}$ for cooling both sides, based on the measured values for top cooling and bottom cooling, would be 0.0839 K/W. The experimentally measured value of $R_{th,j-c}$ is much less at 0.0728 K/W. This reduction confirms the modeled findings in Chapter 2 that the heat flow moves in the x and y-directions and deviates from the one-dimensional heat flow assumptions commonly used in power electronics packages.

The plots in Figure 88 show some similarity at the lower thermal resistance values and then deviate more as the resistance increases. If these curves are separated and viewed closer, the internal structure should reveal itself with changes in the thermal time constant. The curves were plotted separately in Figure 89. To ease in accurately determining the changes in the experimental curves, the derivative of each curve was also plotted. The case resistances are determined using the TDIM measurement and their respective values are marked as well.

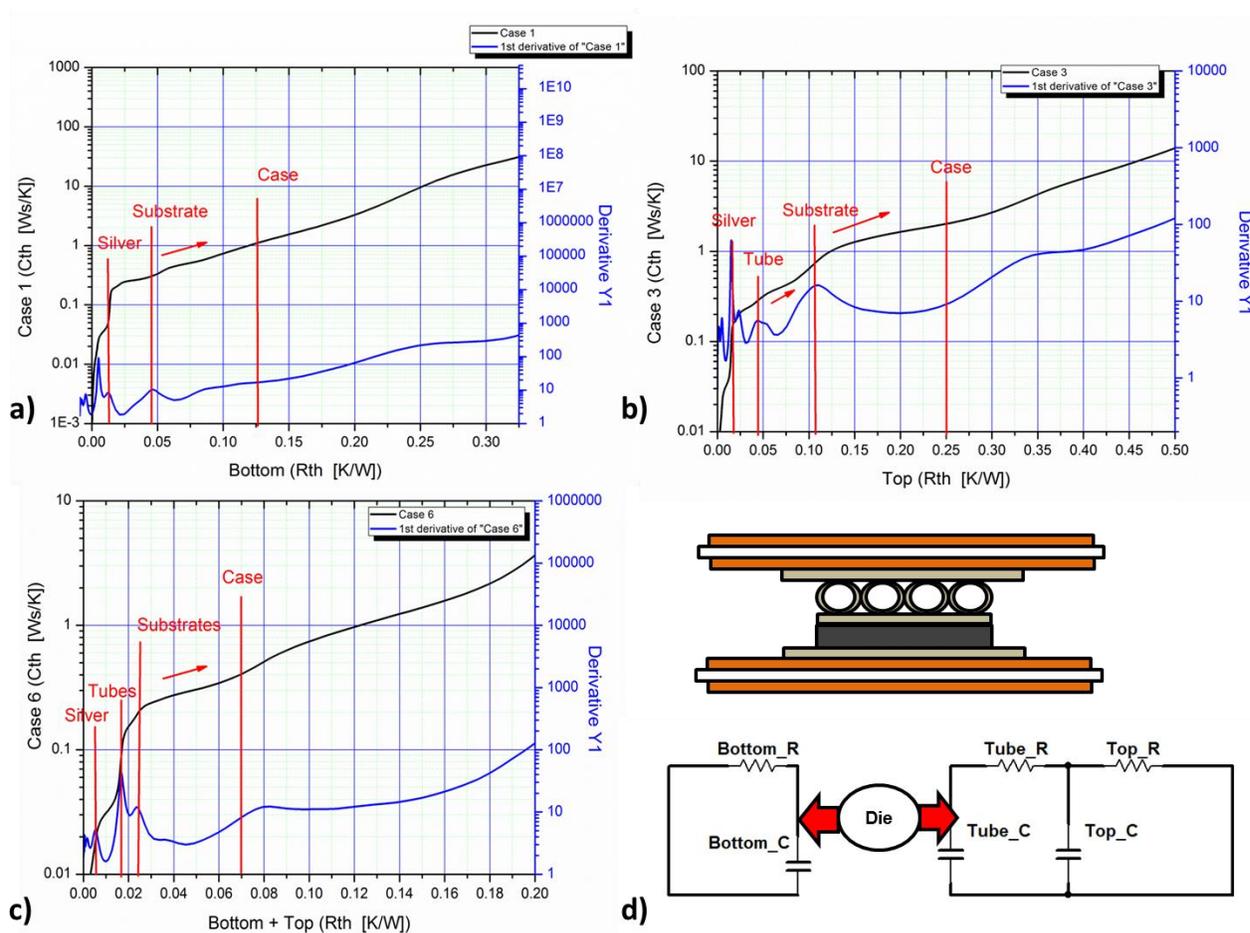


Figure 89: De-convoluted cooling curves showing the experimental structure functions for each cooling scenario; a) bottom cooled b) top cooled and c) both surfaces cooled. A schematic illustrating the cause of variations in structure functions is shown in d).

The easiest configuration to interpret is the bottom cooled scenario (Figure 89a) because it contains the minimum amount of variables. The transitions from die to silver and silver to substrate can easily be distinguished. Because the top configuration also contains the same silver layer and substrate, inferences could be made about their contributions and these transitions were marked. The transitions for the configuration having both sides cooled were made solely on changes indicated by the derivative curve. Comparison of these three results show the resistance contribution of each of the components from the first two scenarios is nearly halved in the third configuration (Figure 89c).

In an effort to confirm the resistance and capacitance indicated in the experimental structure functions, the expected values were calculated. The thermal capacitance and resistance of each material in the stack can be calculated using the material dimensions, specific heat, c_v , and thermal conductivity, λ using equation (10) and (11). However, these quantities are not known for the encapsulation material. These quantities can be used to construct either a Foster or Cauer network.

$$R_{TH} = L/(A * \lambda) \quad (10)$$

$$C_{TH} = V * c_v \quad (11)$$

The calculated quantities for a 14 mm square footprint are shown in Table 26. These calculations confirmed the assumptions used in determining the transitions in the experimentally determined structure functions for top and bottom cooling scenarios. It should be noted that the magnitude

of the thermal resistance for the sintered silver layer is extremely small when compared to the substrate materials and the tubing compliance layer. Therefore, the one additional silver layer on the top of the die is indistinguishable in the experimental data.

Table 26: Calculated thermal resistance and capacitance values for module materials.

Material	Thermal Conductivity (k)	Specific Heat Capacity (c)	Mass Density (ρ)	Thickness / Height	Area	Volume	Resistance (R)	Capacitance (C)
	W/m.C	J/kg.C	kg/m ³	mm	mm ²	mm ³	K/W	J/K
Silicon	149	712	2329	0.14	196	27.44	4.79×10^{-03}	4.55×10^{-02}
Sintered Silver	429	233	10490	0.035	196	6.86	4.16×10^{-04}	1.68×10^{-02}
Copper	400	390	8933	0.32	196	62.72	4.08×10^{-03}	2.19×10^{-01}
Alumina 96	25	880	3720	0.63	196	123.48	1.29×10^{-01}	4.04×10^{-01}
Copper	400	390	8933	0.32	196	62.72	4.08×10^{-03}	2.19×10^{-01}

With this data, it can be seen that given only single sided cooling, cooling the bottom surface is the best option. The tube compliant layer adds additional resistance and this layer should be optimized to gain less thermal resistance while maintaining compliance. However, if the bottom cooled resistance value of 0.1265K/W were assumed to exist on the top as well (a purely symmetric structure without tube compliance) the resulting double-side cooling could be calculated, based on one-dimensional parallel heat flows, to be exactly half. This would mark the optimum condition for this structure possessing the minimum of thermal resistance. The optimal condition results in an R_{th} of 0.06325 K/W and the measured value of our configuration is 0.0729 K/W translating to a difference of 0.00965K/W or 14.8% above optimum.

Chapter 5. Reliability Evaluation: Testing and Modeling

The goal of Finite Element Analysis (FEA) modeling the power module connections is to inspect the various stress and strain states within each package design due to the thermomechanical stresses which arise at non-ambient temperatures. Because the design is more intricate than the common planar stack model, a FEA model is useful. The FEA analysis is accomplished by first constructing a scale model of the geometry to be analyzed. The body is then divided into finite elements, or mesh, which are connected at nodes. The unknown stress and strains at each node can be calculated using matrices. Current FEA software analysis provides the user with an array of data for analysis and modern computing allows for less computing time. For this model, the most important quantities to consider are the yielding, or flow, of the sintered silver interface or the tube structure, the shear stresses on the semiconductor die and the stress states of the complete package with all materials.

For inspection of cycled power electronics packages, it is necessary to not only determine the stress states but also verify if these states will contribute to failure. To examine this further, we can refer to the standard stress-strain curve for a material exposed to a tensile stress. In a tensile test there is initially a linear region where incremental changes in stress correspond to incremental changes in strain. This region is the elastic region and it is reversible. When the material is stressed beyond this region (normally indicated by a 0.2% offset in strain) it undergoes yielding and enters a nonreversible plastic region. For power electronics packaging, yielding of the interfaces is undesirable and several criteria exist for probing the yielding of the interfaces and the compliant tube structure. When previously deformed material, for example

metals that have been work hardened, reach their plastic region it is referred to as plastic flow because the yield point varies as a function of work hardening. The three major flow criterion proposed to quantify the degree of stress needed to translate to undesirable plastic deformation are the maximum stress criterion, the maximum distortion energy criterion and the maximum shear stress criterion. The maximum stress criterion, or Rankine Criterion, states that plastic flow takes place when the greatest principal stress in a complex stress state exceeds the stress found from uniaxial tensile stress tests. The maximum shear stress criterion, or Tresca Criterion, states that plastic flow takes place when the maximum shear stress in a complex state reaches a value greater than the value found from uniaxial tensile tests. The third criterion, the von Mises Criterion, states that plastic flow takes place when the total distortional deformation energy in a complex stress state exceeds the distortional deformation energy of a uniaxial stress test (tension or compression).

The von Mises Criterion is the one most often utilized when expressing the complex stress state in device interconnection. Derivation of the deformation energy for isotropic materials yields a scalar invariant represented by the equation for equivalent von Mises stress where σ_n represents one of three principal stresses.

$$\sigma_e = \sqrt{1/2[(\sigma_1 - \sigma_2)^2(\sigma_2 - \sigma_3)^2(\sigma_3 - \sigma_1)^2]} \quad (12)$$

Yielding will occur when any of the stresses in a complex stress state exceed this equivalent stress. Equivalent von Mises stress can be graphically represented by a circle for two dimension analysis and a cylinder for three dimensions. Figure 90 shows the two dimension graphical

representation with x and y intercepts showing the values of the ultimate stress for an isotropic material.

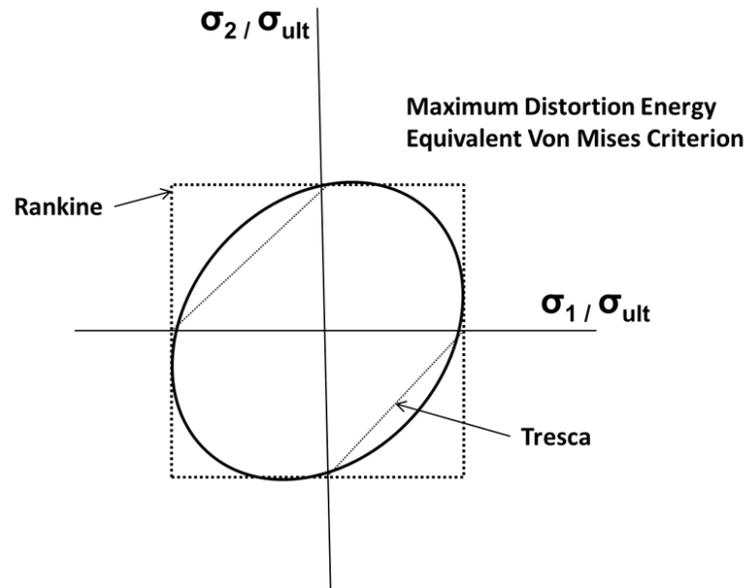


Figure 90: Two dimensional graphic representing the equivalent von Mises maximum distortion energy. The Rankine and Tresca boundaries are included for comparison.

This representation is greatly affected by the hardening mechanism of the material. The yielding bounded by the surface in Figure 90 will change if the material exceeds the elastic region of the material. In the case of isotropic hardening, the yield region will expand and kinematic hardening will shift the surface depending on the extent of plastic yielding.

Ductile metals like aluminum, copper and silver tend to follow the equivalent von Mises yield criterion closely so it will be used in these models [89]. Where necessary, the bulk silver is assumed to react to stress much like copper and aluminum which experience kinematic hardening.

For evaluating package lifetime it is necessary to consider the effects of cycled stress and strain. When the entire package is exposed to changing temperatures and therefore changing thermomechanical stresses, it begins to fatigue. The stress-strain characteristics discussed previously in the case of a tensile test mark the material yielding for one cycle. However, cycled packages are known to fail at values much lower than the yield stress when repeatedly cycled. It has, in the past, been of great interest to understand the fatigue failure of solder interconnects in increasingly smaller electronic packages. The solder joints in these smaller packages need to provide continued electrical connection and structural integrity. Failure in solder joints in these packages are a direct result of the changing thermomechanical stresses which arise from the differences in CTE of the package materials. FEA analysis is often used to assess or predict electronics package failure because the areas of interest are normally too small to accurately observe and measure. This is also the case with the double-side planar module package which shields accurate observation by placing the interfaces of interest between two substrates.

The first step in utilizing FEA for fatigue analysis is to determine the failure model. FEA fatigue models are separated into five categories which are based on the failure mechanism of interest. The five fatigue model categories are: 1) plastic strain based models 2) creep strain based models 3) stress based models 4) energy accumulated models and 5) damage accumulation models. [90] Because the mechanism of interest in this research is the resulting strain from the mismatched packaged CTEs when exposed to changing temperatures, the strain based approach is optimal. Of the two strain models, the creep strain is not likely to be applicable. Creep strain is applicable for solder joints which exceed their useful temperature range. When a solder alloy is exposed to temperatures exceeding 80% of their melting point, creep fatigue plays a dominant role in

failure. However, the sintered silver interface possesses a melting temperature of 961°C and both proposed cycling regimes fall well below 30% of that temperature. Therefore, any effects from creep strain in sintered silver die attachment should be negligible.

The five most prominent strain based fatigue models for evaluating electronics packaging are shown in Table 27. Each of these models concentrates on a different strain contribution to package fatigue although many of the constitutive equations have variables in common. The lifetime is found in cycles to failure, N_f .

Table 27: Summary of strain based fatigue models specifically for evaluating fatigue in electronic packages [90].

Fatigue Model	Constitutive Equation	Parameter of Interest
Coffin Manson	$\frac{\Delta \epsilon_p}{2} = \epsilon_f' (2N_f)^c$	Change in plastic strain (measured in third cycle)
Basquin	$\frac{\Delta \epsilon}{2} = \frac{\sigma_f'}{E} (2N_f)^b$	Change in elastic strain range (measured in third cycle)
Total Strain	$\frac{\Delta \epsilon}{2} = \frac{\sigma_f'}{E} (2N_f)^b + \epsilon_f' (2N_f)^c$	Change in both plastic and elastic strain (measured in third cycle)
Solomon	$\Delta \gamma_p N_p^\alpha = \theta$	Change in shear plastic strain (strain in x-y plane)
Englemaier	$N_f = \frac{1}{2} \left[\frac{\Delta \gamma_t}{2 \epsilon_f} \right]^{1/c}$	Change in total shear strain (strain in x-y plane)
Miner	$\frac{1}{N_f} = \frac{1}{N_p} + \frac{1}{N_c}$	Superposition of both plastic and creep strain

The Coffin Manson and Basquin equations are the two models most often associated with fatigue and, it can be seen from above, the combination of the two make up the Total Strain equation.

The Coffin Manson equation considers the effect of plastic deformation on the number of reversals to failure while the Basquin equation considers elastic deformation. In the case both plastic and elastic contributions are present then the sum of their contributions can be used for failure prediction.

Fatigue characteristics are normally described using the S-N (stress-life) curve, which are published for many materials. The y-axis represents the stress amplitude and the x-axis represents cycles to failure. Ferrous alloys have a low stress boundary termed the endurance limit below which the material can be cycled infinitely without failure. However, the endurance limit does not exist for nonferrous alloys for which we are primarily concerned in this study. From the graph above, the linear forms of the Coffin Manson and Basquin equations are convenient ways to easily assess cycling lifetime. The slope for the Coffin Manson relationship is denoted by the fatigue ductility index, c , and is an indication of cycle frequency and mean temperature. The fatigue ductility index can be expressed as

$$c = -0.442 - (6 \times 10^{-4})T_m + (1.74 \times 10^{-2}) * (\ln(1 + f)) \quad (13)$$

Where T_m is the mean temperature and f is the cycle frequency in cycles per day. The y-intercept is the fatigue ductility, ϵ'_f and the lifetime (reversals to failure) is denoted by N_f on the x-axis. The slope of the linear form of the Basquin relationship is denoted by the fatigue strength exponent, b which is tabulated for each material and its y-intercept is the fatigue strength coefficient, σ'_f . The variable, E , is the elastic modulus. In this form, it can easily be seen that

given similar fatigue ductility terms for identical cycling regimes, the lifetime can be evaluated in a relative manner by comparing differences in plastic strain, ε_p , or strain range, ε . This is particularly helpful when using a material like sintered silver whose properties have not been as thoroughly documented as solder alloys. A reliable fatigue ductility analysis for this material is outside the scope of this project, but by using the same material for identical cycling regime models, the relative lifetime can be predicted by relative changes in FEA strain values.

The Solomon and Englemaier techniques can be used in much the same way. It can be seen from the Solomon equations that a change in the plastic shear strain, γ_p , will result in an increase in θ , which represents the inverse of the fatigue ductility coefficient. A comparison of two materials can then predict the lifetime by changes in measured plastic shear strain without knowing the value of, a , which is a material constant and not available for the sintered silver material. Finally, the Englemaier relationship can be used to evaluate the contributions to lifetime in a relative manner by measuring the changes in total shear strain, γ_t .

The goal of FEA modeling the power module packaging configurations is not for quantification of lifetime. The objective, rather, is to look at the strengths and weaknesses of the different package configurations by measuring the von Mises stress distributions in the package and the degree of shear stress on the semiconductor device while also making estimates of relative lifetime based on changes in plastic strain and total shear strain. Each of these parameters will be examined using a three cycle FEA model for both passive and active cycling regimes.

5.1. Finite Element Model Parameters

The finite element model construction for the cycling models very closely resembles the steps outlined in Chapter 2 for the fabrication thermomechanical model and the thermal evaluation. However, the computing time necessary for evaluating a full model through three thermal cycles is unreasonably large. For this reason, the model must be simplified further. Because the original model possessed a great deal of symmetry, the thermal model can be reduced to $\frac{1}{4}$ of the original through symmetry planes. The reduction of the model using symmetry is illustrated in Figure 91 using the model for a single die attached to one substrate.

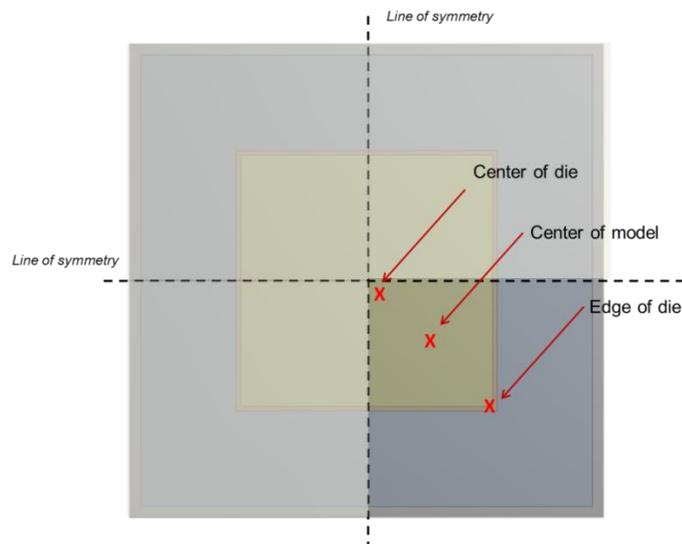


Figure 91: FEA cycling model reduction using model symmetry.

For the double-side package model that contains the compliant tube interface it was necessary to place only one tube centered on the die vs two tubes (dictated by symmetry). An illustration of the simplified double-side tube model with meshing can be seen in Figure 92. This simplified model also allows for an increase in mesh detail which is necessary for model convergence of

intricate geometries. The symmetrical planes in this model are to the left and rear of the image. The silver tube is partially hidden at this angle.

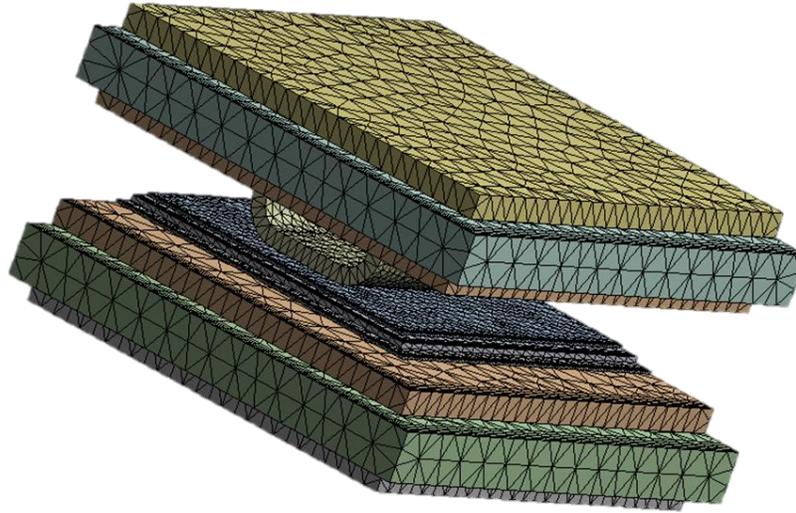


Figure 92: The simplified cycling model with FEA mesh for the double-side package with compliant tube interface above the die.

The mechanical properties used in the FEA analysis in Chapter 2 were also used in this model. The table of properties (Table 28) from Chapter 2 is shown again in this section for clarity.

Table 28: Mechanical properties of solid bodies utilized in FEA thermomechanical cycling model.

	Young's Modulus (E) (GPa)	Bulk Modulus (K) (GPa)	Shear Modulus (G) (GPa)	Poisson's ratio (ν)	CTE (ppm/K)
Alumina 96%	299.28	172.00	123.67	0.21	8.2
Bulk Silver	78.00	100.00	28.46	0.37	18.9
Copper	134.40	140.00	50.15	0.34	16.5
Sintered Silver ^[35]	40.00	30.30	15.62	0.28	18.9
Silicon	155.79	91.17	64.10	0.22	2.34

Recent research on the mechanical properties of sintered silver has concluded that sintered silver interconnection can be accurately modeled using an Anand viscoplasticity model. A viscoplastic material exhibits rate-dependent inelastic behavior. The resulting plastic deformation is especially important in transient applications and cycling regimes. For this reason, additional Anand model parameters were added to the sintered silver mechanical properties. A list of the Anand model parameters used, which were given by Yu et al, are listed in Table 29 below [91].

Table 29: Anand viscoplastic model parameters for sintered silver device attachment published by Yu et al. ([91] D.-j. Yu, X. Chen, G. Chen, G.-q. Lu, and Z.-q. Wang, "Applying Anand model to low-temperature sintered nanoscale silver paste chip attachment," Materials & Design, vol. 30, pp. 4574-4579, 2009) Used under fair use, 2014.

Nanoscale silver paste Anand model parameters		
A(s⁻¹)	Pre-exponential Factor	9.81
Q (J/mol)	Activation Energy	47,442
m	Strain Rate Sensitivity of Stress	0.65720
n	Deformation Resistance	0.00326
ξ	Multiplier of Stress	11
ŝ (MPa)	Coefficient of Deformation Resistance Saturation	67.389
h₀ (MPa)	Hardening/Softening Constant	15800
s₀ (MPa)	Initial Deformation Resistance	2.768
a	Strain Rate Sensitivity of Hardening/Softening	1

5.2. Active Cycling (Accelerated Reliability) Model

For the active cycling regime, it was important to mirror the active cycling experimental conditions as close as possible. In active cycling, the die itself generates the heat needed to cycle the package. The experimental active cycling conditions dictated a symmetric cycle period of approximately 300 seconds with 150 seconds heating and 150 second for cooling. The maximum junction temperature from experiments was 160°C and the minimum junction temperature was 40°C. This heating profile was the basis for the FEA modeling profile. For

fatigue analysis, the mean temperature, T_m , for this experiment is 100°C and results in a fatigue ductility index, c , of -0.4034. It was also quite necessary to include the fabrication step within the model as well to insure the residual stresses after module fabrication are included. To accomplish this, the zero stress state of each material and all bonded interfaces was set to 290°C which is the sintering temperature. The entire package was then brought to room temperature very quickly (30 s). Stress evaluation is not performed in this initial time period, but the stress state is transferred to the next step. Inclusion of this step should mimic closely the real stress state before the cycling regime begins. For the next three cycles, only the die junction temperature is increased using the profile set forth in Figure 93. This die temperature change was accomplished by directly changing the device body temperature rather than impose a heat flux or power requirement. This condition was preferred because the packages were drastically different in thermal impedance. Had the heat flux or power been chosen to remain constant, the device junction temperature for each configuration would not have been the same. These differences would reflect the thermal resistance difference in the package, but may not provide an accurate comparison of CTE stress at the interface of interest due to differing device temperatures. This type of loading has been used in previous package cycling analysis for similar reasons [92]. For modeling the cycling regimes at least three thermal cycles are required for stress and strain to stabilize [93, 94]. The temperatures of all bodies at each step are then transferred to the FEA structural analysis module for stress analysis.

Additionally, all materials in this model are assumed to be homogeneous and isotropic. All the interfaces are assumed to be perfectly bonded and the convection conditions are the same on all the exposed surfaces in each configuration. A large deformation is assumed to ease model

convergence and in the double-side packages an additional friction free support is used on the top of the package. In the encapsulated double-side package with the tube interface, additional assumptions were made and encapsulation was added to the geometry during the fabrication step. This, however, does not accurately match the fabrication profile. In actual module fabrication, encapsulation is added at 150°C in a separate heating step and would not be capable of handling temperatures greater than 175°C.

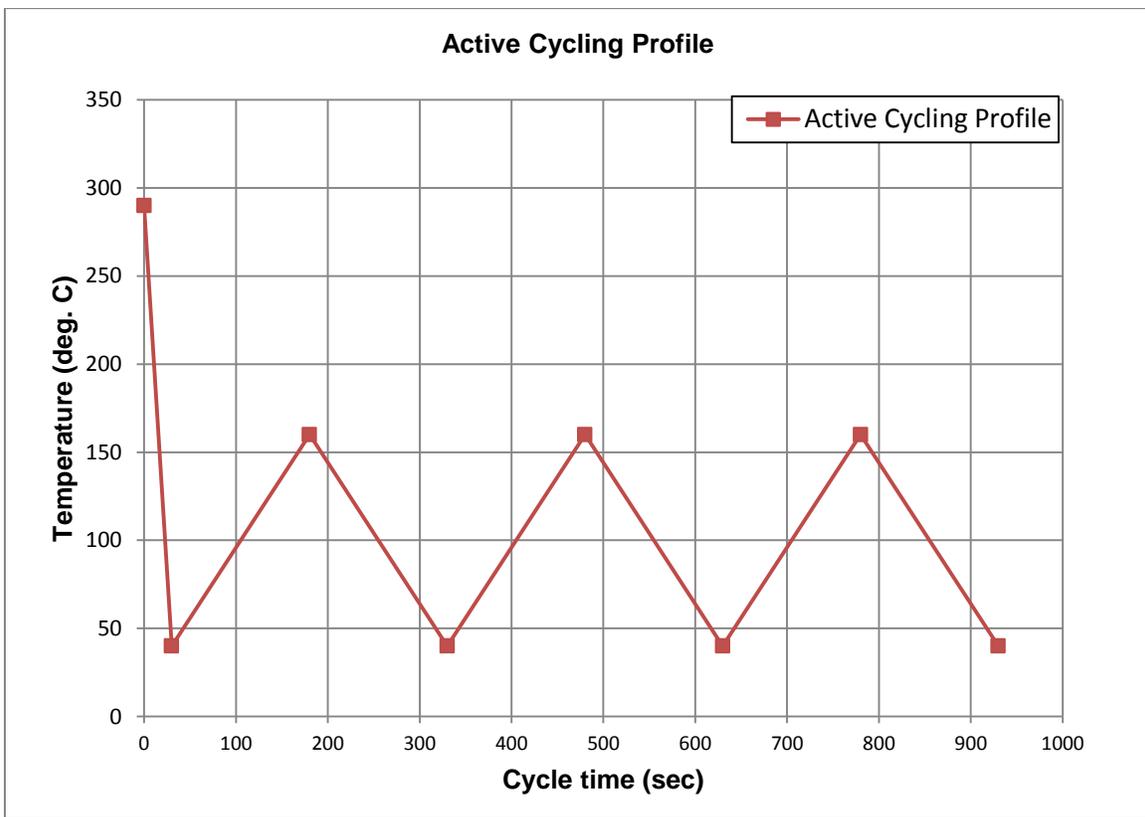


Figure 93: Active cycling profile including fabrication thermal step used for FEA model. Entire package was exposed to thermal loads for fabrication ($t < 30s$), and device was used as heat source for active cycle ($t > 30s$).

5.2.1. Model Results

The largest issue with implementing the double-side planar package is the quantity of shear stress that develops in the device during cooling from fabrication temperatures. This shear stress is also a concern during cycling protocols. It can be seen from the modeling results (Figure 94) that device shear stress rises to a maximum on the heating portion of the cycle and falls to a minimum on the cooling portion for each configuration. The configuration which yields the lowest shear strength is the single sided die attachment. It is common for the single sided attachment to undergo curvature stresses, but not experience a large degree of shear stresses. As for the other three configurations, the device shear stresses are highest in the encapsulated package using the compliant tube layer and lowest in the package with the compliant layer alone. The encapsulated configuration modeling assumptions are greater and therefore may be less accurate as a result. The double-side package without a compliant tube interface has shear values between the encapsulated and unencapsulated tube package. The maximum third cycle device shear in the package with compliant tube structure is 7.87×10^7 Pa whereas the package without the tube interface yields 1.41×10^8 Pa which represents a 35% increase in device shear stress.

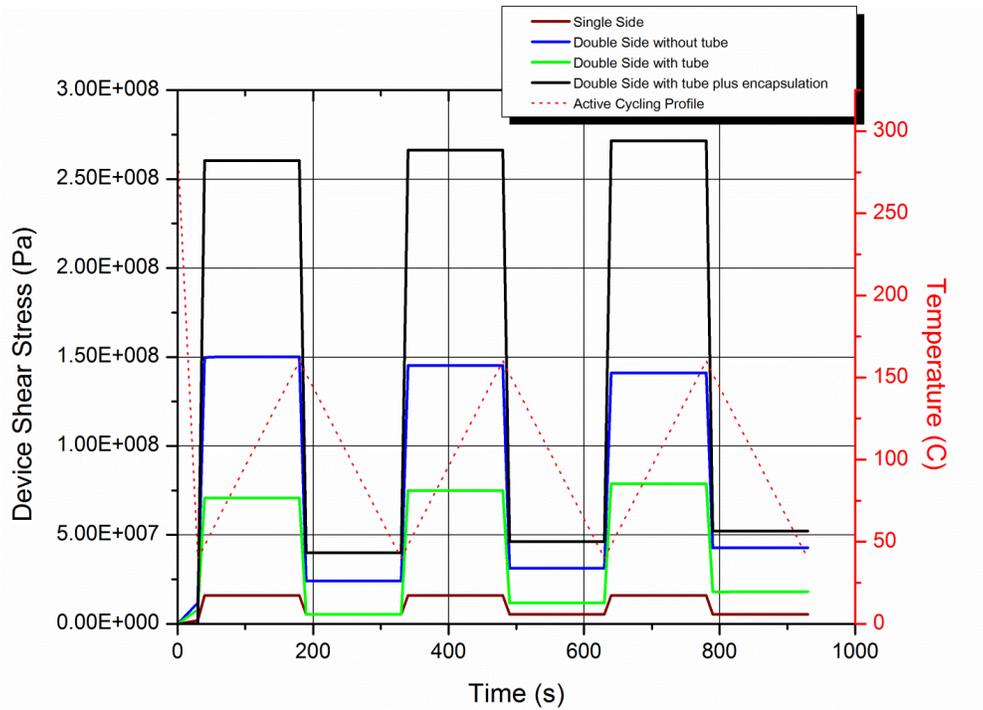


Figure 94: Comparison of device shear stress as a function of cycles in active cycling regime.

As discussed earlier, the von Mises stress helps to translate complex stress states by including all stress orientations. It then provides a convenient method for assessing the overall package for areas of increased stress regardless of geometry. The von Mises stress of the entire package was plotted in Figure 95 below to illustrate the magnitude of package stresses and at which point they arise in the cycling profile. It can be seen that the largest von Mises stresses develop during the heat cycle of the active profile. During the cooling portion of the curve, each configuration falls closer to zero. The highest stresses (2.25×10^9 Pa) are found in the double-side package without a compliant layer. The lowest, however, is not the single-sided package but the double-side tube package without encapsulation which is 4.45×10^8 Pa.

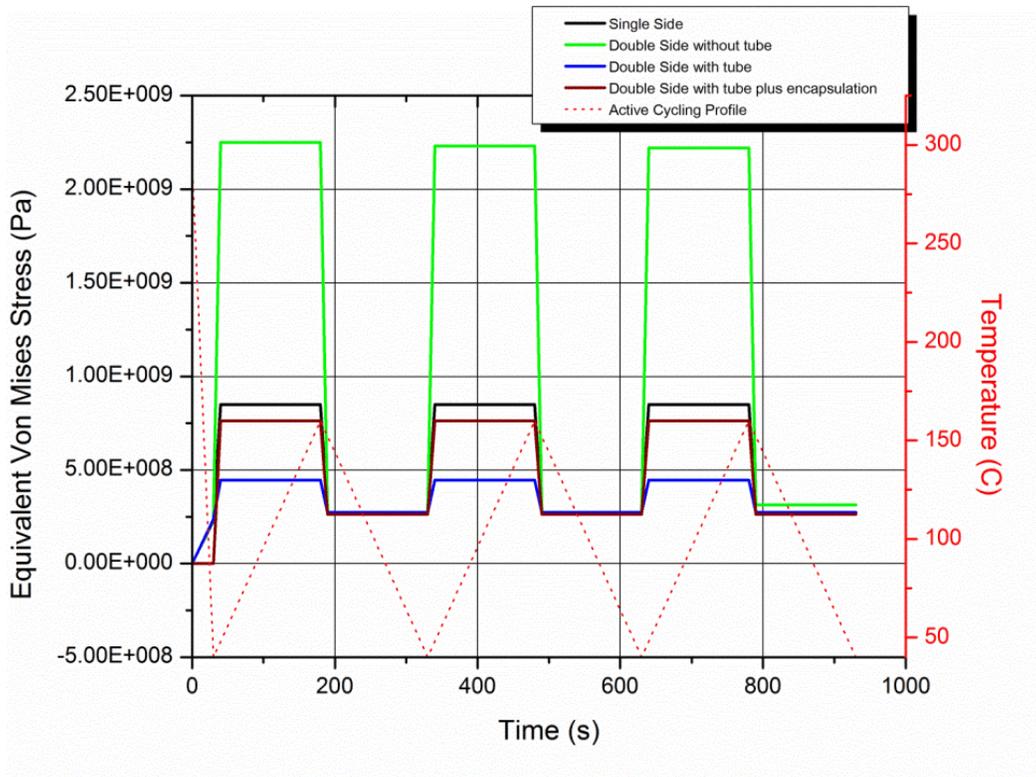
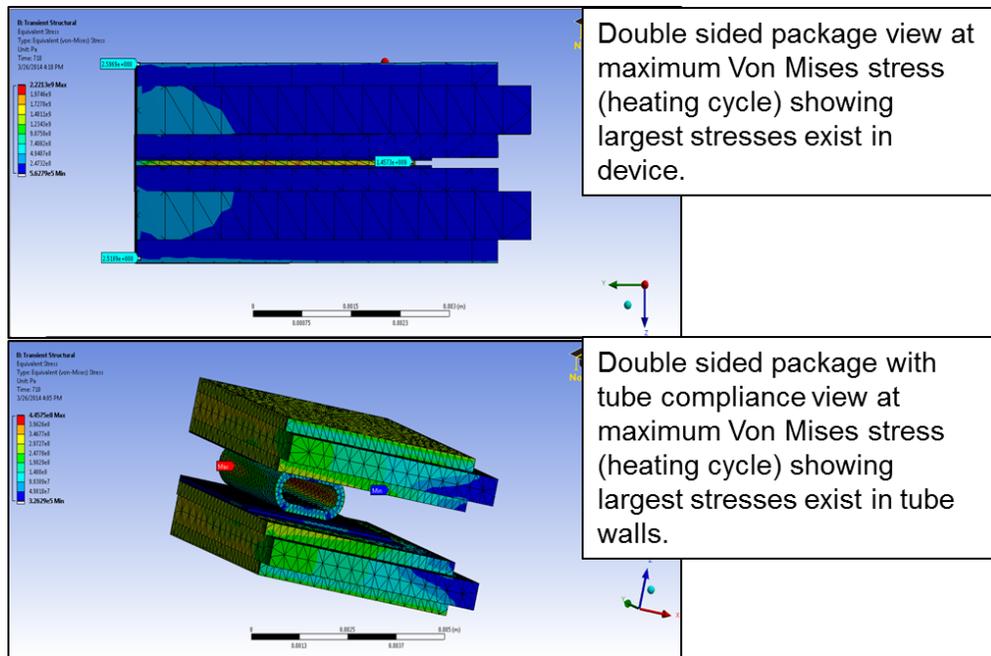


Figure 95: Comparison of package von Mises stress for each package configuration as a function of active cycles.

Although this seems promising at first glance, it is necessary to view the von Mises stress distribution to determine the locations of the maximums and minimums. For example, if the maximum stress is on the device in one package it may be more detrimental than if the maximum stress is on the substrate in another. A comparison of the von Mises stress distributions in Figure 96 reveals that in the package with the compliant tube layer, the tubing walls possess the largest von Mises stress. In the double-side package without the compliant layer, the semiconductor device experiences the largest von Mises stress.



Double sided package view at maximum Von Mises stress (heating cycle) showing largest stresses exist in device.

Double sided package with tube compliance view at maximum Von Mises stress (heating cycle) showing largest stresses exist in tube walls.

Figure 96: Von Mises stress maxima locations for different package configurations.

For lifetime assessment using the Coffin Manson equation, the parameter of interest is the plastic strain accumulation. As discussed earlier, with all material properties equal, the largest plastic strain translates to the lowest number of cycles to failure. The evolution of the plastic strain in the sintered silver die attachment between the die and the bottom substrate of each package is shown in Figure 97.

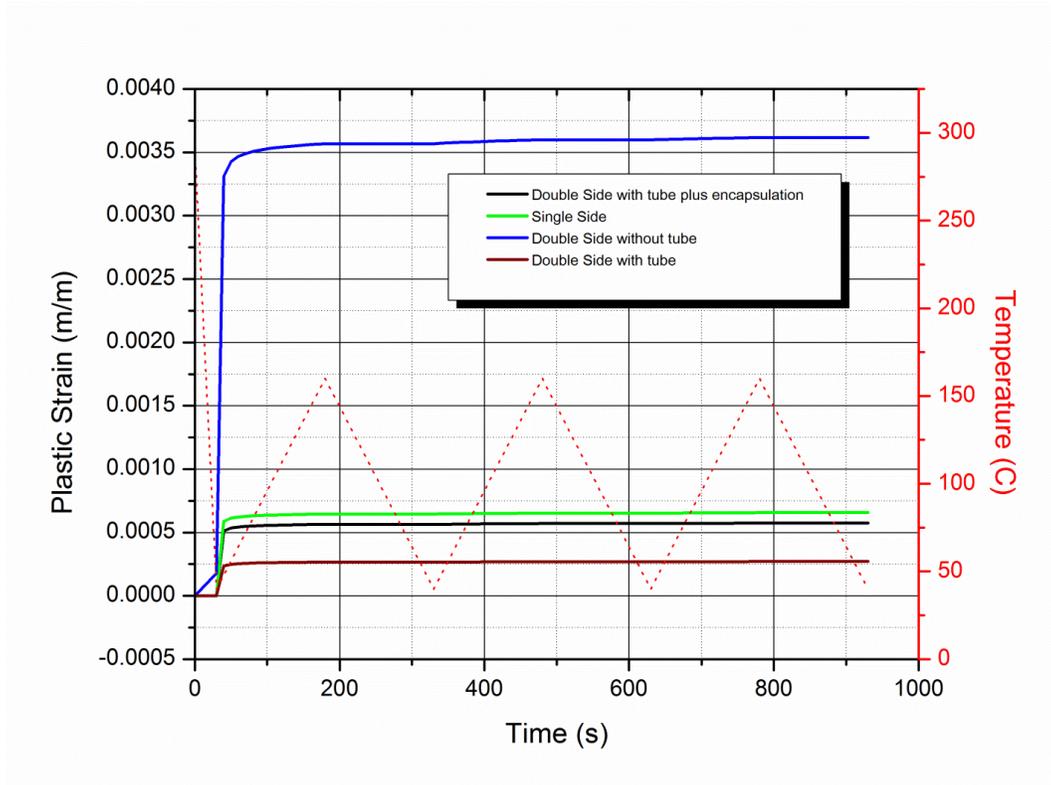


Figure 97: Accumulation of plastic strain in the sintered silver interface between the die and substrate for various package configurations as a function of active cycles.

Because three cycles are required for stress and strain equilibrium, the plastic strain used for lifetime evaluation is the change in plastic strain during the last heating and cooling profile. Although the change in the third cycle is not apparent on the graph above, the overall change in plastic strain for the entire set of cycles can easily be seen. The smallest overall plastic strain is seen in the double-side package with the tube compliant interface. The change in plastic strain, $\Delta\epsilon_p$, of each for the third cycle is shown in Table 30 from lowest to highest.

Table 30: Third cycle plastic strain change, $\Delta\epsilon_p$, for each package configuration.

	$\Delta\epsilon_p$ (3rd cycle change in plastic strain) (m/m)
Double-side attachment with compliant tube structure	1.10×10^{-6}
Single side attachment	3.30×10^{-6}
Double-side attachment with compliant tube structure plus encapsulation	3.97×10^{-6}
Double-side attachment without compliant tube structure	1.70×10^{-5}

These values reflect the maximum plastic strains in the interface, but it is common for the maximum strain values to be found outside the die attachment footprint at the edges or corners of the die. To qualify these results it is essential to measure and compare the third cycle changes in plastic strain at various points in the attachment interface directly beneath the die. Third cycle plastic strains were measured at three different points in the interface beneath the die; the center of the die (corner of the model), the center of the model (a point halfway between the center and die edge) and at the die corner. A comparison of the plastic strain changes of each are shown in Figure 98 below.

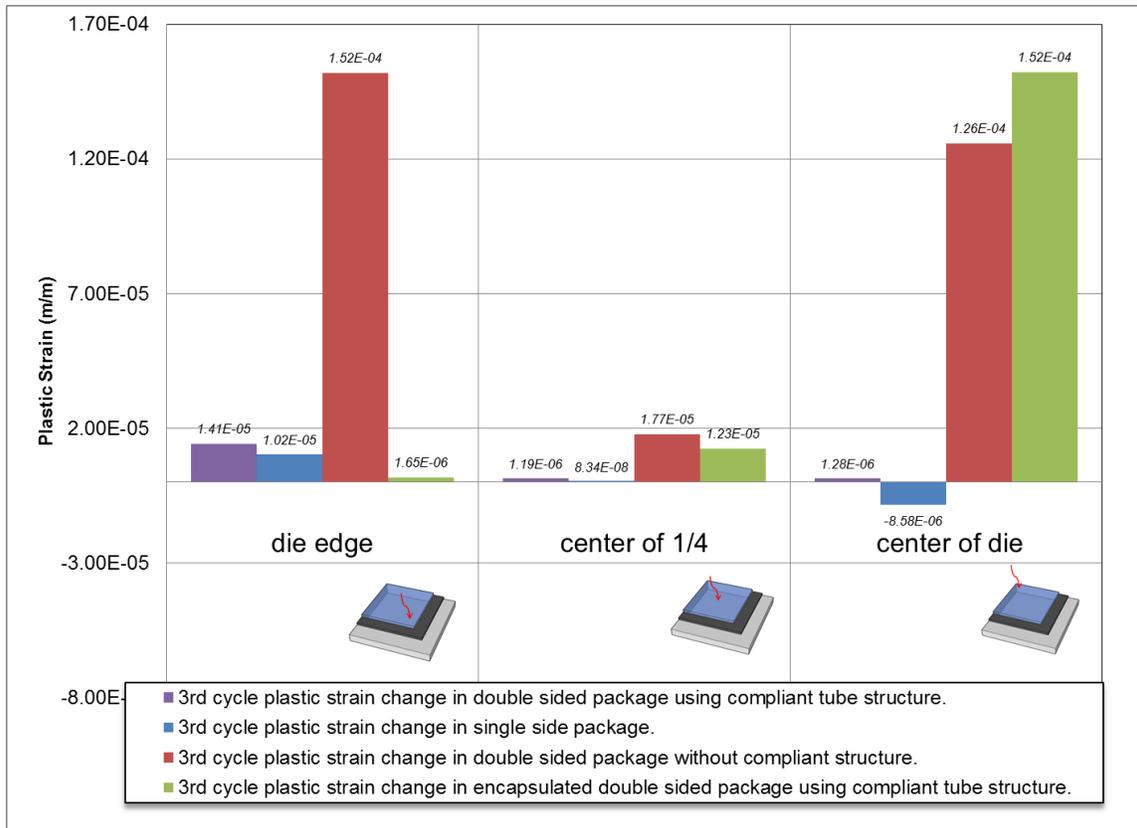


Figure 98: Third cycle changes in plastic strain at various points in the interface directly below the die for each package configuration.

These measurements confirm the decrease in plastic strain range for the double-side package without encapsulation. The encapsulated package plastic strain ranges are highest at the center of the die, but fall as the measurement moves outward. The double-side package without added compliance is consistently higher.

Both the Solomon and Englemaier equations use accumulated shear strain as the basis for lifetime prediction. These too can be used for relative comparisons given similar material properties. The shear strain (strain in the x-y plane) of the sintered silver interface beneath the die was probed at the center of the model which represents a quarter of the overall model. This

point corresponds to an actual distance halfway between the die edge and the center. The shear strain values at this point are plotted for each configuration with the cycling profile in the Figure 99 below.

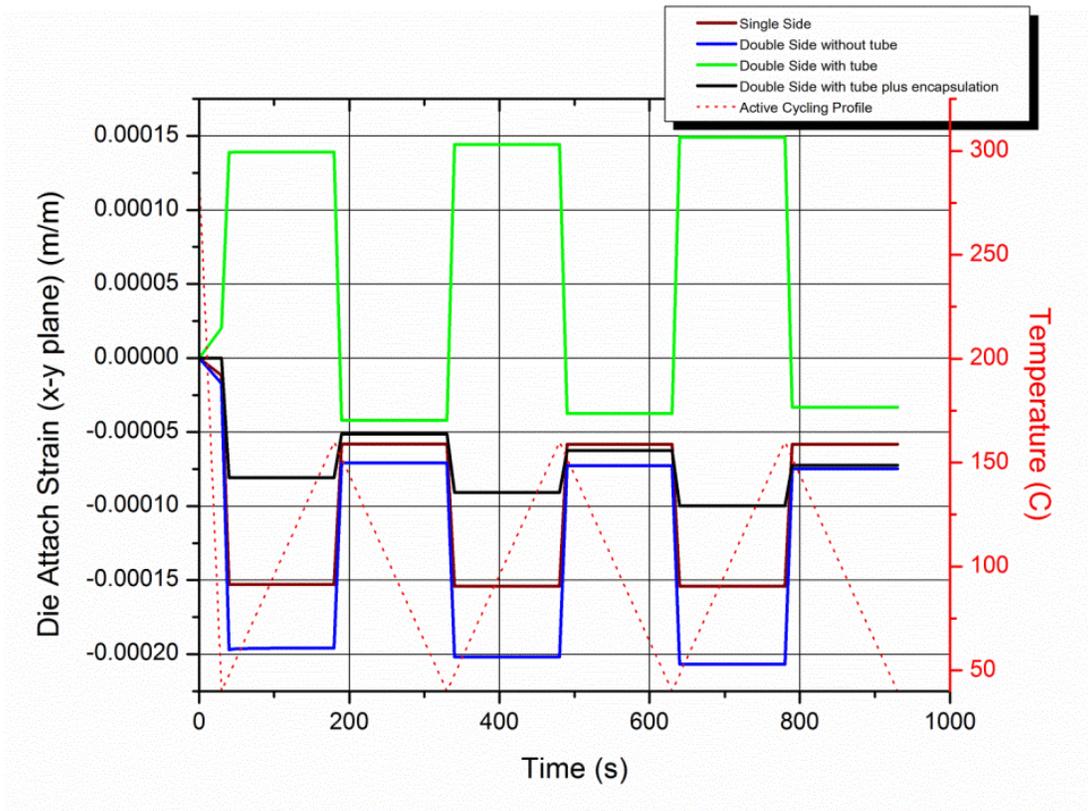


Figure 99: The shear strain magnitudes in the sintered silver interface between die and substrate for each package configuration as a function of active cycles.

From the plot, it can be seen that the shear strains for each configuration are quite different. The package with the tube interconnect becomes more positive (tensile) during the heating profile while the other configurations become more negative (compression). Although, the trends are not similar, the shear strain change magnitudes are in close agreement. The changes in shear strain for the interface below the semiconductor die are tabulated in Table 31 from lowest to highest overall strain range.

Table 31: Third cycle strain ranges (in ascending order) for sintered silver interface below die for each package configuration.

	$\Delta\gamma$ (3rd cycle change in shear strain) (m/m)
Double-side attachment with compliant tube structure plus encapsulation	2.73×10^{-5}
Single side attachment	9.57×10^{-5}
Double-side attachment without compliant tube structure	1.31×10^{-4}
Double-side attachment with compliant tube structure	1.82×10^{-4}

For the package without the tube compliant layer, one may infer that the strain in both the interface above and below the die possess identical plane shear strain profiles. In the package with the tube compliance, the asymmetrical structure means the sintered interface above the die will experience a different shear strain profile when probed at the same x-y position. A comparison of the shear strain above and below the die is shown in Figure 100 below.

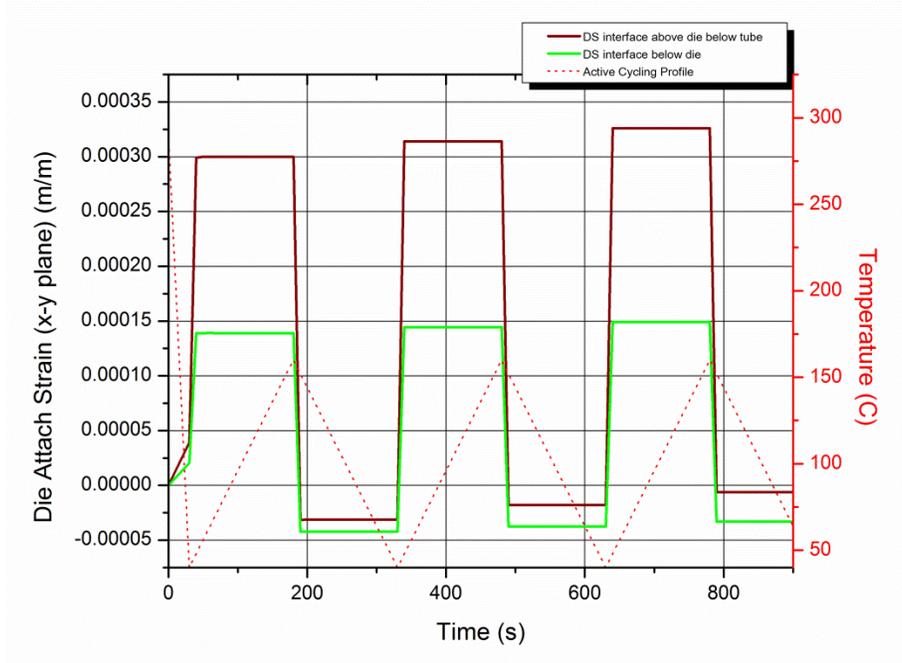


Figure 100: Shear strain magnitudes above and below the die in the package with compliant tube interface.

It is clear from these results that the shear plane strain in the interface above the device is nearly double of that below the device. The trend is still the same as that of the lower interface with a tensile shear in the heating cycle and a compressive shear in the cooling cycle. However, these values represent the maximum across the entire interface and are a good approximation for the homogeneous planar bond between the die and the substrate. The shear strain distribution in the interface above the die is not uniform and the maximum value cannot be characteristic of the entire surface. To illustrate this point a color distribution plot of the shear strain magnitude in the interface between the tube and the die is shown in Figure 101 .

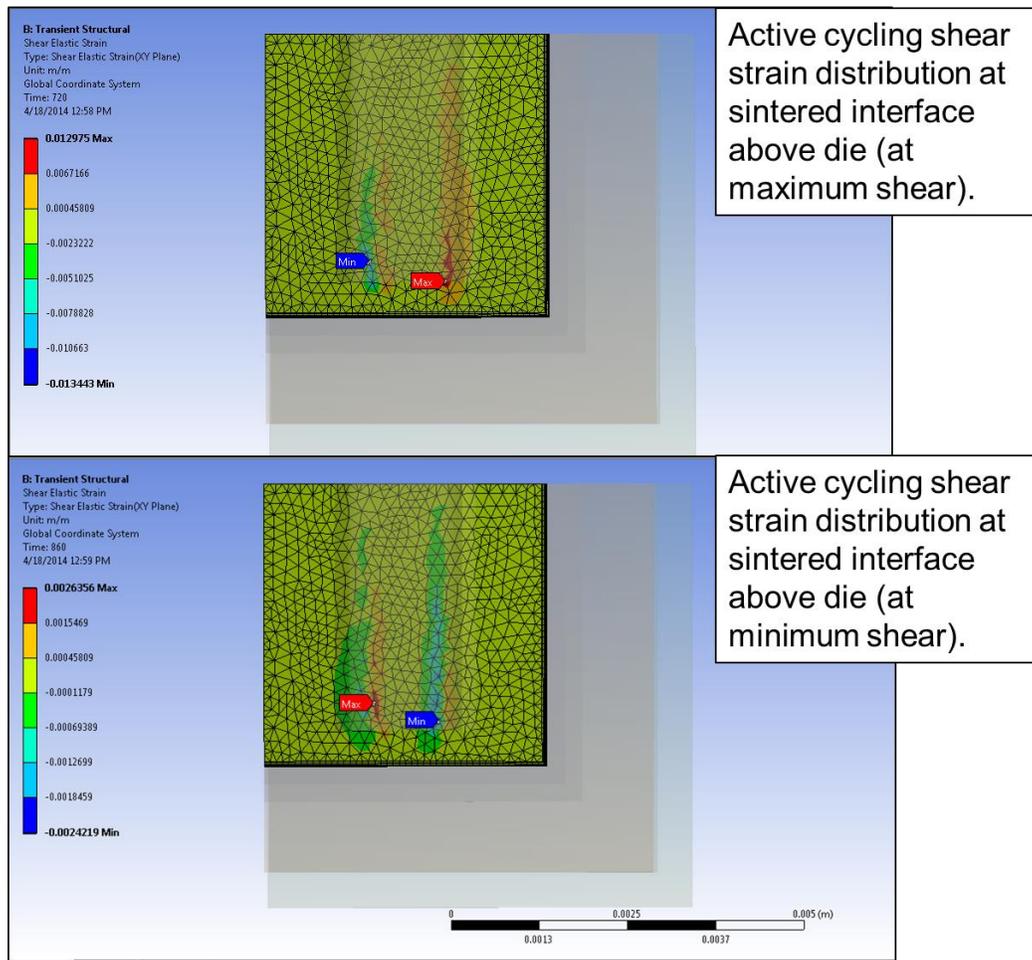


Figure 101: Colored plot illustrating shear strain distribution in the sintered silver interface between the die and the tube in the compliant tube package.

It can be seen that the maximum value of strain is found beneath the edge of the tube and is very different than the bulk of the strain magnitudes in this interface. Solomon or Englemaier life prediction models may predict significant decrease in failure lifetime for these points in the interface above the die.

It is also important to note that no attempt to measure the fatigue life of the silver tube in the compliant tube interface was performed. Although the tube walls experienced the largest von Mises stresses in this cycling profile (Figure 102), they were not sufficiently large to induce

plastic strain. With this in mind, the tube failure by fatigue was most unlikely so the fatigue life of the interfaces were the focus of the model.

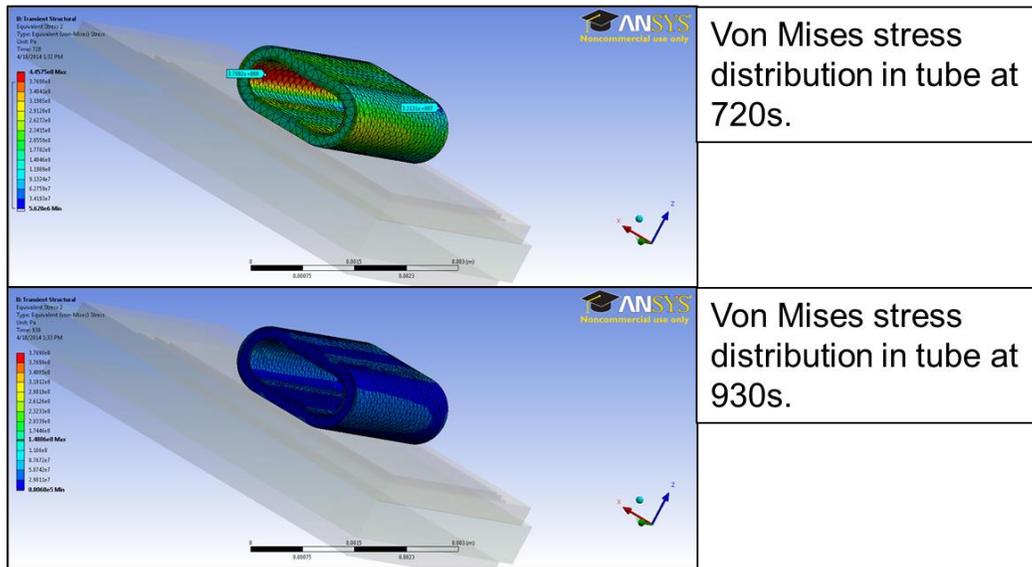


Figure 102: Von Mises stress distribution in the compliant silver tube interface.

5.2.2. Active Cycling Parametric Model Results

It is also important to understand how the lifetime is affected by changes in tubing parameters like wall thickness. An FEA model was created to perform a parametric evaluation of the von Mises stress after four active cycles (5 second power pulses) with a temperature range of 50°C to 150°C. This study was done by collaborators at the Center of High Temperature Electronic Packaging at the School of Materials Science and Engineering at Tianjin University in China. The details of the study conditions are outlined in more detail in Appendix A.

The results of the model for a true active cycling profile indicate that the von Mises stress on the device increases as the tubing wall thickness is increased for a given aspect ratio. The interface

height used in this model was 1 mm. Additionally, the die and the die interconnection experience increased stress as the tubing wall is increased. A summary of the results is shown in Figure 103 below.

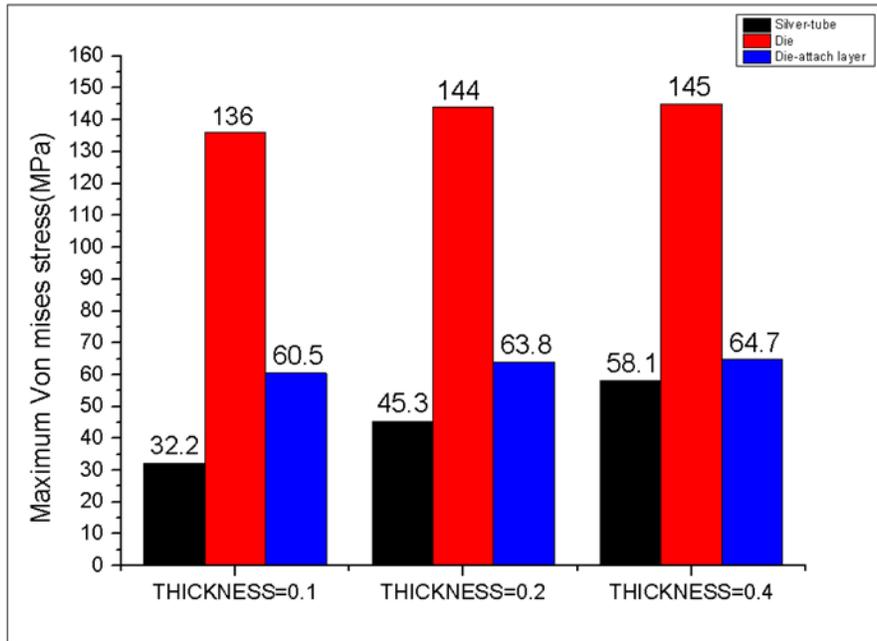


Figure 103: Fourth cycle von Mises stress measurements for module components for modules constructed of different tubing wall thickness (1 mm high interface).

5.3. Passive Cycling (Thermal) Model

Unlike, active cycling, the passive thermal cycling regime requires the entire package be exposed to the same temperature changes. The model material parameters and assumptions do not change from the active cycling scenario. The initial fabrication temperature step is also included in this model for consideration of the residual stresses present in the package after fabrication. Each body follows the same cycling ramps whereas before in the active cycle only the device was cycled in temperature. The passive experimental scheme, shown in Figure 104, includes

much larger temperature differences. The cycling parameters for the model reflect the experimental cycle from -55°C to 175°C . One complete heating and cooling cycle is 2400 seconds long. This cycling scheme results in a mean temperature, T_m , of 60°C and a fatigue ductility index, c , of -0.415 .

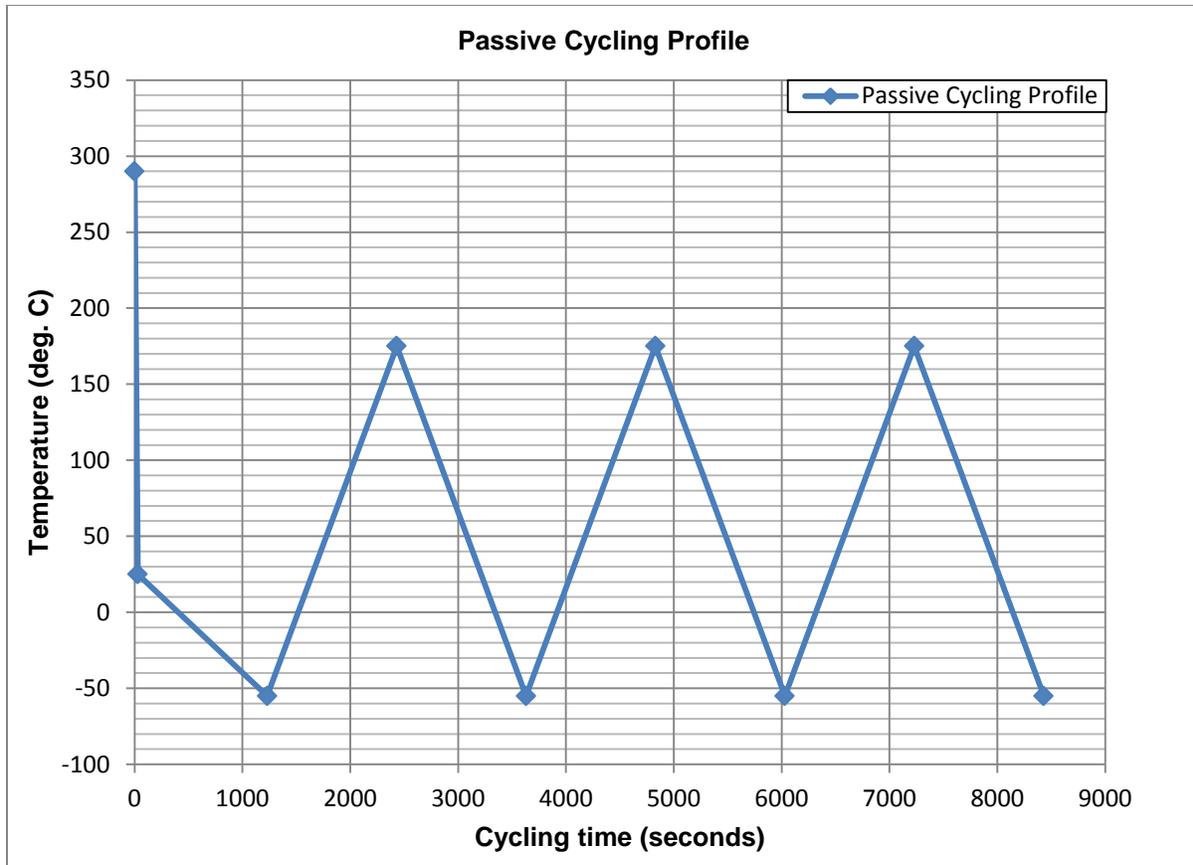


Figure 104: Passive cycling profile including fabrication thermal step used for FEA model. Entire package was exposed to thermal loads for both fabrication and cycling.

For passive cycling a double-side package it is important to insure the cycle time is greater than the expected transient thermal response of the package. The thermal time constant can be calculated to predict the thermal response of each of the materials in the package. The time constant is simply the product of the material's thermal resistance and capacitance. The thermal

capacitance and resistance for each of the package materials for the modeled dimensions were tabulated in Table 26 of Section 4.5.2. The time constant calculated for each of these materials is shown below in Table 32.

Table 32: Thermal time constant (τ) calculated for each of the materials used in the passively cycled module package.

Material	Resistance (R)	Capacitance (C)	Time constant (τ)
	K/W	J/K	s
Silicon	4.79×10^{-03}	4.55×10^{-02}	2.18×10^{-04}
Sintered Silver	4.16×10^{-04}	1.68×10^{-02}	6.99×10^{-06}
Copper	4.00×10^{-03}	2.19×10^{-02}	8.76×10^{-05}
Alumina 96	1.29×10^{-01}	4.04×10^{-01}	5.21×10^{-02}
Copper	4.08×10^{-03}	2.19×10^{-01}	8.94×10^{-04}

The material with the largest time constant, or slowest thermal response, is the alumina isolation layer for the substrates. Five time constants are required to reach a near steady state condition, which for the alumina substrate would be 260 ms. The cycle times for both the passive cycle model and experiment are >4500 times the thermal response time so effects attributed to thermal transients of the package can be disregarded.

5.3.1. Model Results

As previously discussed, the goal of the tube compliance layer was to minimize the shear stresses seen by the semiconductor device. The device shear stresses are recorded during the cycling model and plotted in Figure 105 below. The trends for the passive cycling shear stress follow closely those of the active cycling shear stress.

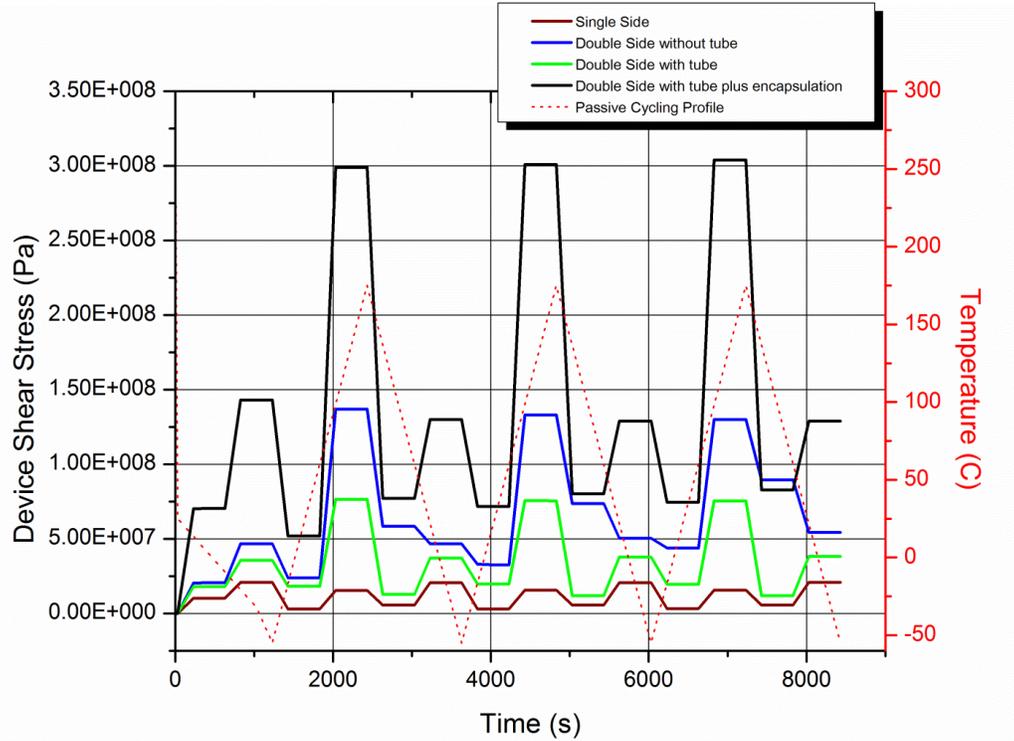


Figure 105: Device shear stress for each package configuration as a function of passive cycles.

The maximum shear stresses arise during the heating cycle in each case with the highest shear stresses being found in the encapsulated package containing the compliant interface. The encapsulated package, again, may lack accuracy due to various extra modeling assumptions. Of the two double-side packages without encapsulation, the package containing the compliant layer had the lowest device shear stresses. The maximum third cycle shear stress in this package was 1.19×10^7 Pa whereas the package without the added compliance measured nearly seven times higher at 8.95×10^7 Pa.

The von Mises stress was used to survey the entire package during the cycling profile for determination of the most intense stresses and their locations. A plot of the maximum von Mises stress for each configuration is shown in Figure 106 below.

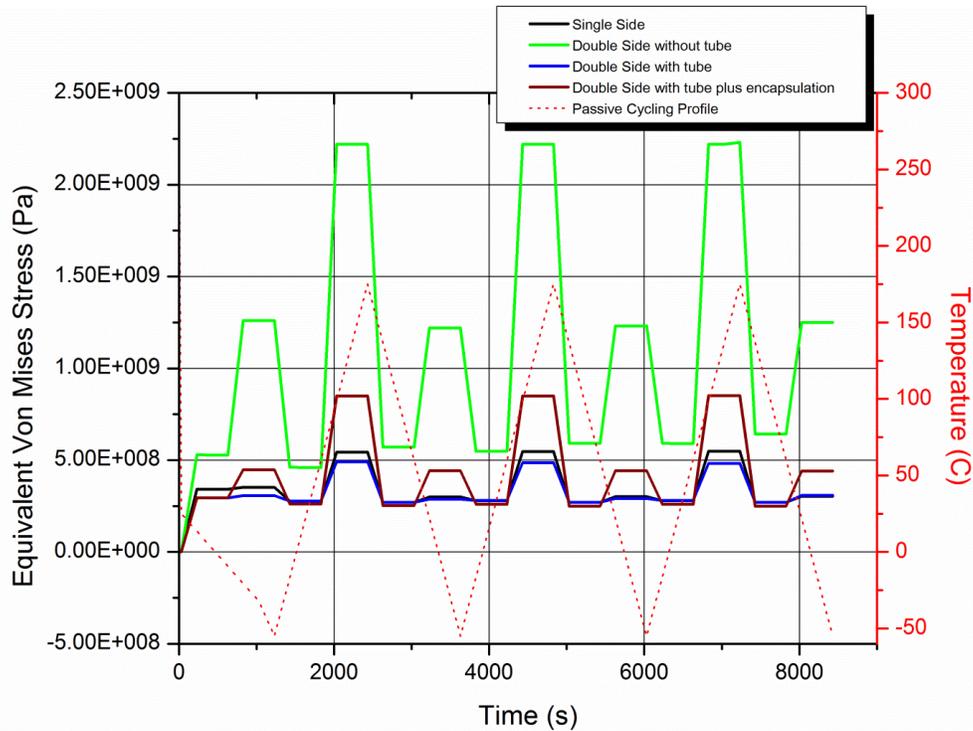


Figure 106: Comparison of package von Mises stresses for each configuration as a function of passive cycles.

The trend for the passive cycling follows that of the active cycling with the largest von Mises stresses being found in the package without the tube compliant interface. The magnitude of the von Mises stress in this package in the third cycle is 2.29×10^9 Pa. The unencapsulated package with the compliant interface has a third cycle magnitude of 3.09×10^8 Pa. This represents one order of magnitude decrease in von Mises stress. This indicates only the extent of the overall stress state in the package with no indication of the stress location. A colored distribution plot (Figure 107) of the von Mises stress for each configuration reveals the stress maxima locations in the package. The maximum von Mises stress in the package without the added compliance is on the semiconductor device which is undesirable.

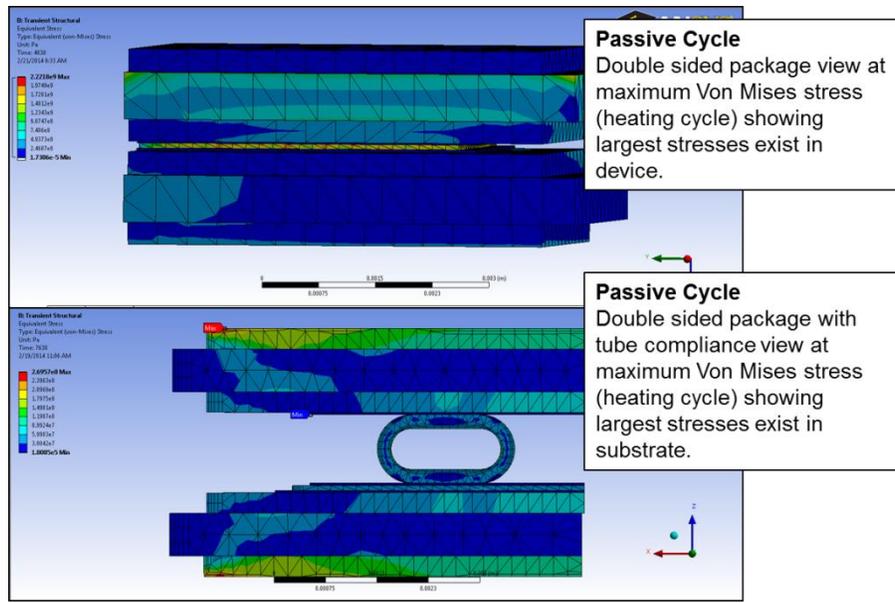


Figure 107: Location of von Mises maxima in passively cycled package configurations.

The plastic strain is also used as an indication of the cycling lifetime for the passive cycled model. A plot of the plastic strain accumulation is shown in Figure 108 below.

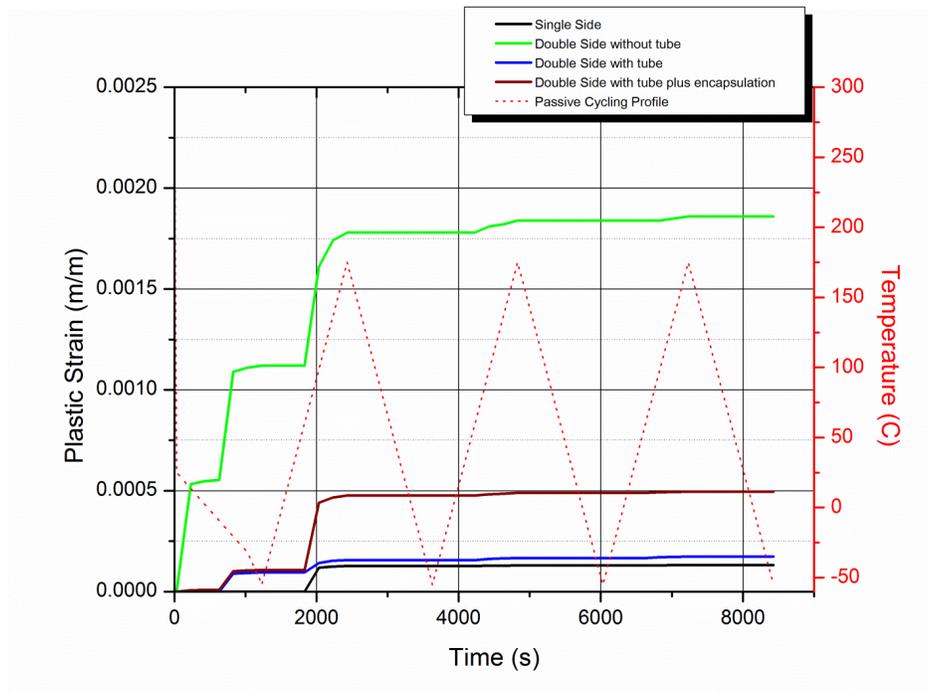


Figure 108: Plastic strain accumulation in various package configurations as a function of passive cycles.

The trends for plastic strain also follow closely that of the active cycling model. It is obvious from the plot that the largest plastic strain accumulation exists in the interface below the die of the double-side package without added compliance. The changes in plastic strain, $\Delta\epsilon_p$, for the third cycle are tabulated and listed in order of increasing magnitude in Table 33 below. The plastic strain in the double-side package without compliance is more than three times higher than the package containing the added tube interface.

Table 33: Third cycle plastic strain change, $\Delta\epsilon_p$, for each package configuration in ascending order.

	$\Delta\epsilon_p$ (3rd cycle change in plastic strain) (m/m)
Single side attachment	1.06×10^{-6}
Double-side attachment with compliant tube structure	6.66×10^{-6}
Double-side attachment with compliant tube structure plus encapsulation	6.98×10^{-6}
Double-side attachment without compliant tube structure	2.31×10^{-5}

As with the active cycling measurements, these plastic strain values represent only the maximum values in the interface which most often do not occur directly beneath the die. It is important to examine the plastic strain differences at specified points beneath the die and compare their trends for confirmation. The changes in plastic strain at three points underneath the die for each of the four configurations are shown in the bar graph in Figure 109.

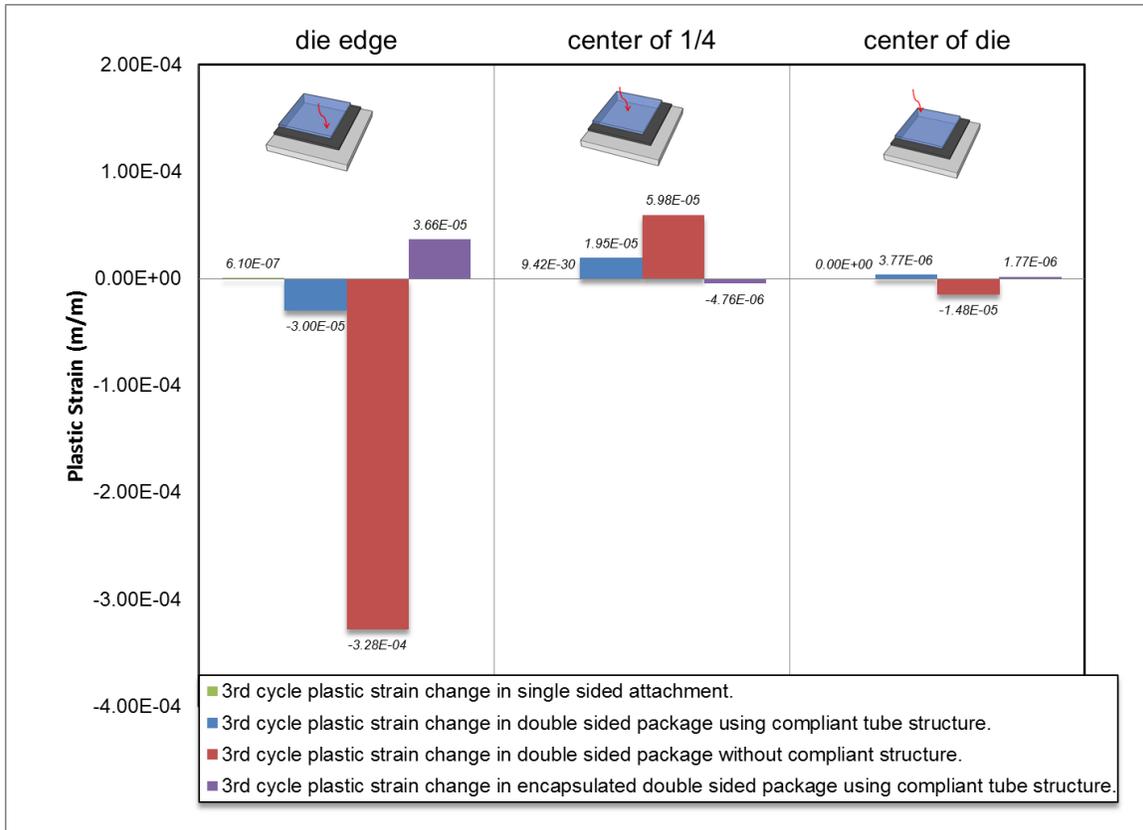


Figure 109: Third cycle changes in plastic strain at various points in the interface directly below the die for each package configuration.

A comparison of the third cycle plastic strain range values confirms the trends seen in Figure 108. The double-side package with the compliant structure maintains a small plastic strain accumulation regardless of sampling coordinates.

For determining the effect on lifetime (cycles to failure) using the Solomon and Englemaier constitutive equations, it is necessary to see the changes in the plane shear strain, $\Delta\gamma$, during the third cycle. The shear strain is again probed in the interface below the die at the center of the model. Because the model represents one quarter of the whole, this corresponds to a distance approximately halfway between the die edge and the center. This position was chosen to avoid

edge effects. A plot of the plane shear strain in this position for each configuration is shown below in Figure 110. For each configuration, the shear strain oscillates around zero with a positive (tensile) strain during the cooling portion of the cycle and a negative (compressive) strain during the heating portion of the cycle.

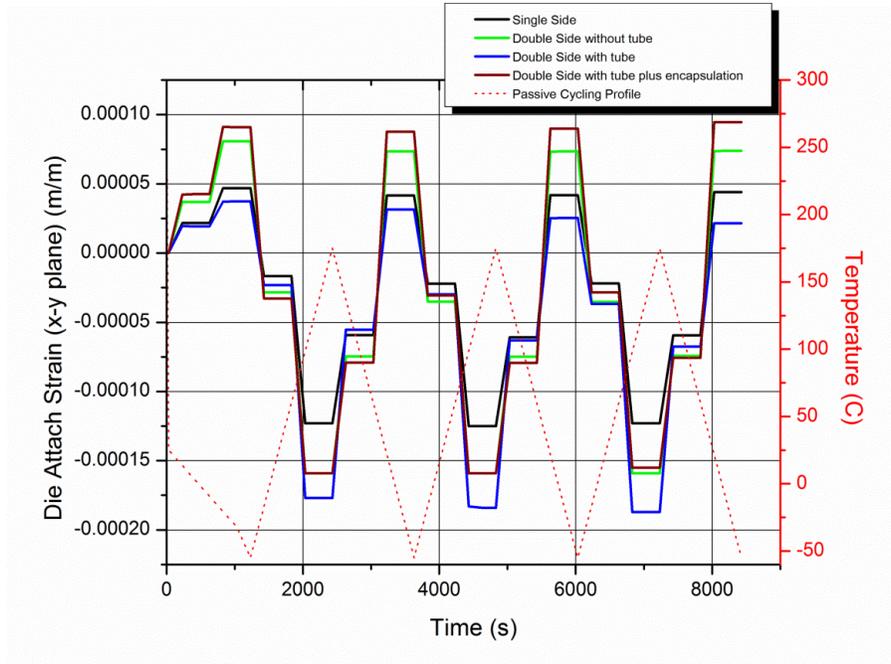


Figure 110: The shear strain magnitudes in the sintered silver interface between die and substrate for each package configuration as a function of passive cycles.

From these results, the change in strain, $\Delta\gamma$, for the third cycle can be found for each configuration. These values are tabulated in Table 34 below.

Table 34: Third cycle strain ranges (in ascending order) for sintered silver interface below die for each package configuration.

	$\Delta\gamma$ (3rd cycle change in plane strain) (m/m)
Single side attachment	1.67×10^{-4}
Double-side attachment with compliant tube structure	2.09×10^{-4}
Double-side attachment without compliant tube structure	2.33×10^{-4}
Double-side attachment with compliant tube structure plus encapsulation	2.49×10^{-4}

These values are in close agreement because where one configuration experiences a high magnitude strain during the cooling cycle, it then has an equally lower magnitude on the heating cycle. Because of the close agreement, any change to lifetime predictions based on shear strain range of passive cycling would be difficult.

The interface above the die should be evaluated as well. In the asymmetric package using the compliant tube structure, the interface above and below cannot be assumed to experience identical shear strain ranges. To understand this interface, it is necessary to view the shear strain distribution at the maximum (cooling cycle) and the minimum (heating cycle) shear strain values. A color distribution plot of the shear strain on the interface above the die is shown in Figure 111.

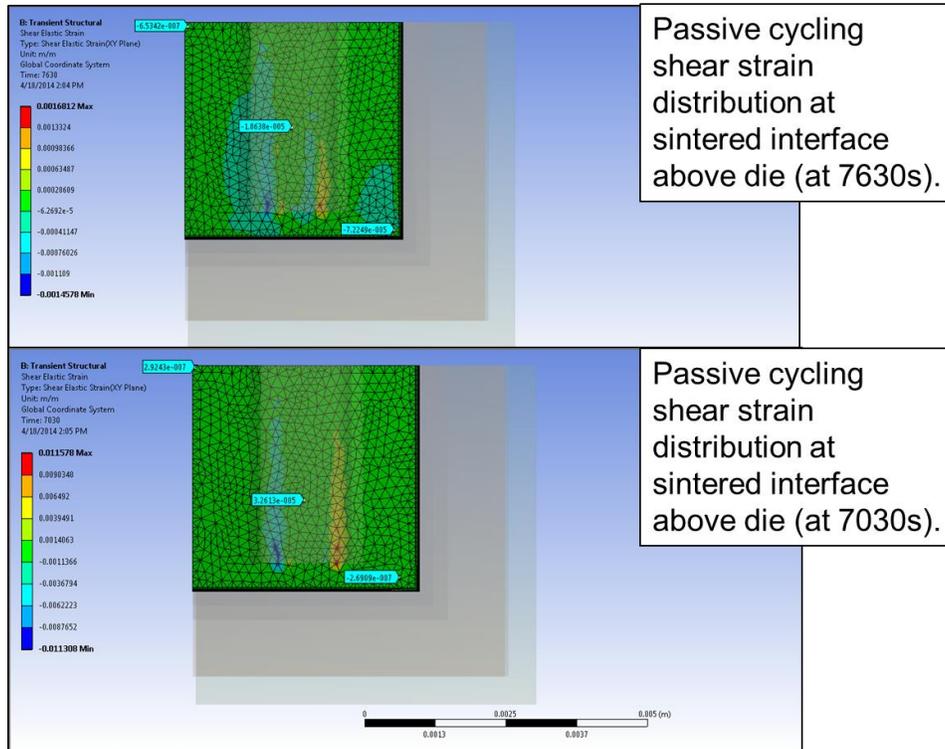


Figure 111: Colored plot illustrating shear strain distribution in the sintered silver interface between the die and the tube in the compliant tube package.

It is clear from the plot that the shear strain in the interface above the die is not homogenous. The areas directly underneath the tube walls have alternating low and high shear strains. Solomon and Englemaier fatigue models suggest these areas will contribute to a decrease in package lifetime (cycles to failure).

As in the active cycling models, the silver tube of the compliant interface was not a focus of the failure assessment. The von Mises stress distributions of the passive cycling profile resemble those of the active cycling profile (Figure 112). And although the stresses are at a maximum in the tube walls, they are still not sufficiently high to induce plastic strain at these locations.

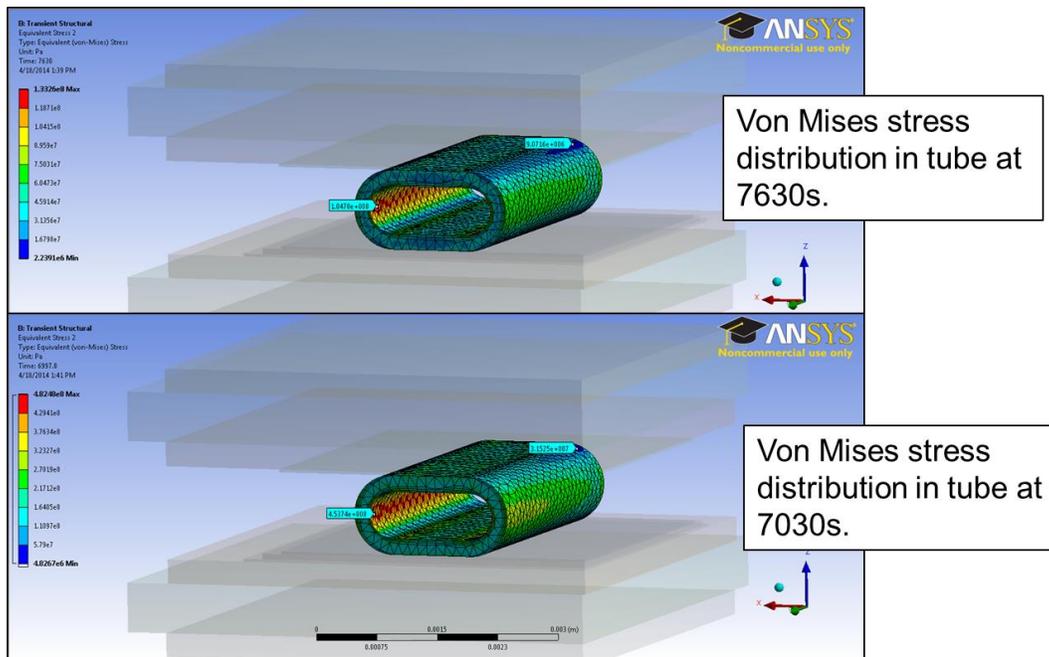


Figure 112: Von Mises stress distribution in the compliant silver tube interface.

In summary, the FEA model for both active and passive cycling regimes indicates a decrease in overall von Mises stress for the package with the tube compliance. The stress distributions for the tube package also suggest that the von Mises stress and shear stress as seen by the device are significantly reduced. Using the measured plastic (Coffin Manson and Basquin) and shear strain (Solomon and Englemaier) values as an indication of relative cycling lifetime reveals an increase in lifetime for the die-substrate sintered interface for packages utilizing the compliant tube structure. The interface between the tube and die in the compliant package possesses a nonhomogeneous stress distribution which may lead to a decrease in lifetime or crack initiation through localized fatigue.

5.4. Measurement of Device Temperature Sensitive Parameters

There are several experiments which require fast and accurate measurements of the device junction temperature and active cycling is one. Rather than attempt to use a thermocouple or temperature sensitive resistor, an electric device parameter that predictably changes with temperature is utilized. This parameter is sometimes referred to as the Temperature Sensitive Parameter (TSP) or K-factor. A common TSP for the IGBT is the temperature dependent gate-emitter voltage (V_{ge}) and the proper measurement protocols are outlined in military standard MIL-STD-750D [95]. The IGBT collector-emitter voltage (V_{ce}) also fluctuates with temperature and can be used as a TSP when properly calibrated.

A proper K-factor measurement requires measuring the gate-emitter voltage as temperature is decreased from a sufficiently high temperature [96]. This requires proper placement of the thermocouple which is difficult in a double-side package because the device junction is not accessible. To accomplish an accurate junction temperature a module was constructed with thermocouples embedded directly into the tube interface above the junction of both devices. This same technique was used for measuring the temperature in the DC power stage testing. The module with thermocouples can be seen in Figure 113. This module was then heated on a lab hotplate to 175°C. Labview was used to record the V_{ge} of the IGBT as the module is slowly cooled to room temperature. To record the change in V_{ge} a small bias current must be applied to the gate to allow for sampling the changing voltage, but not contribute to device self-heating.

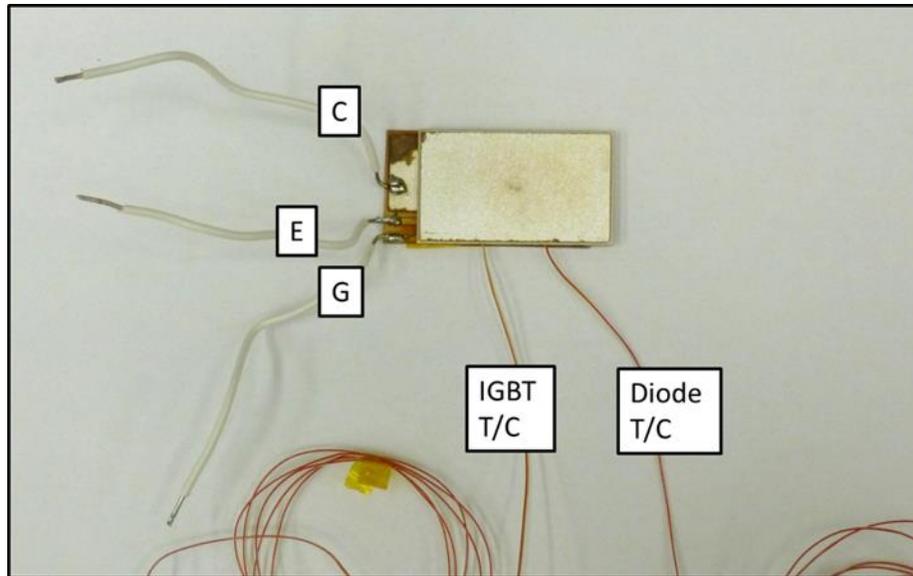


Figure 113: Prototype module constructed for measuring accurate junction temperatures during temperature sensitive parameter experiments.

The ABB IGBT used in this investigation has a maximum working temperature of 150°C. Traditionally, silicon devices were thought to be functional at 175°C and device physics suggest the theoretical temperature limit is >200°C. The original active cycling scheme had a maximum junction temperature of 175°C. When the V_{ge} was sampled using 2 mA of gate current, it fell quickly to 0 V at a temperature of only 145°C. This decrease was due to a change of the V_{ge} threshold with temperature. Using a higher V_{ge} current of 8 mA, the TSP can be recorded to a higher temperature. The results of the TSP measurement at 8 mA can be seen in Figure 114. It is clear from these measurements that the TSP is not applicable above 162°C.

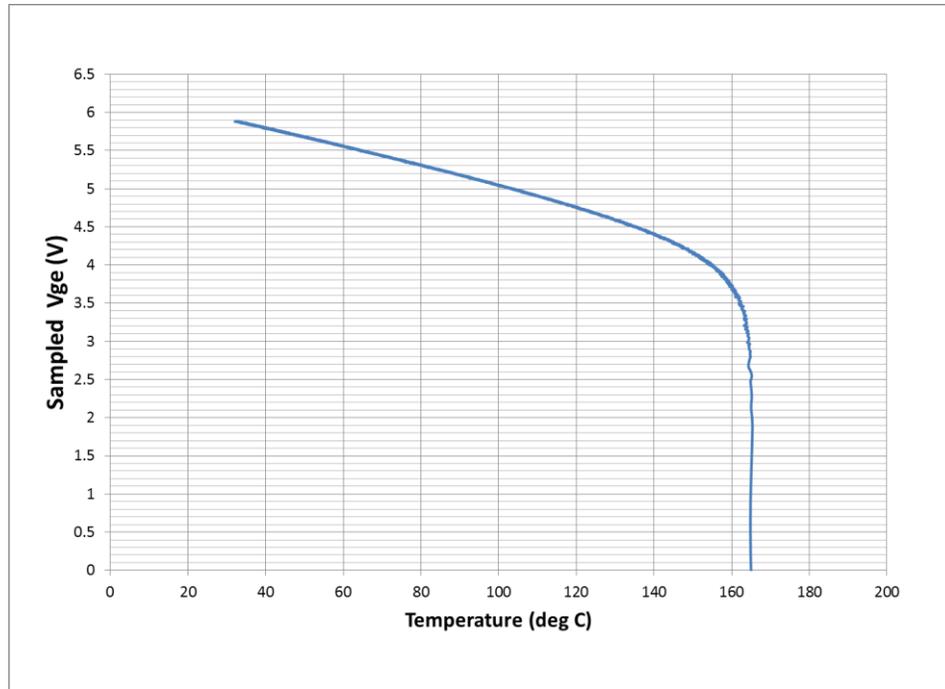


Figure 114: A plot of the changing gate emitter voltage (V_{ge}) as temperature is cooled from 175°C.

Below 162°C, the curve is very close to linear. Figure 115 shows a plot of the linear portion of the data. The right plot is obtained by using the Labview linear fit function which is an option on the experimental setup. This data was found to have a y-intercept of 6.32567 V and a slope of 13.00 mV/°C.

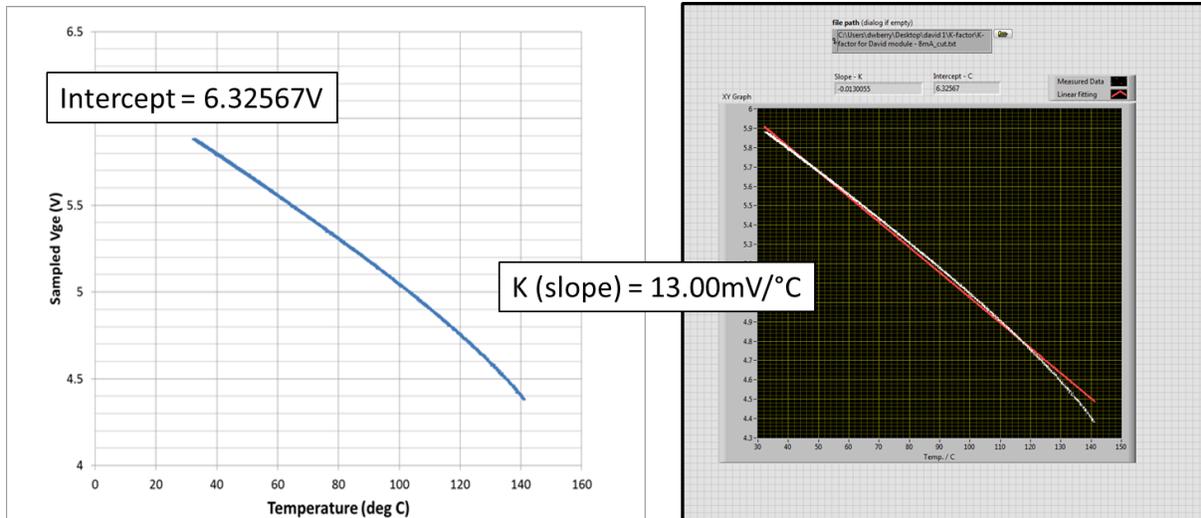


Figure 115: Linear fit of operational portion of the TSP curve using an ABB IGBT.

The K-factor, or TSP, which will be used for all experiments with these devices is 13.00 mV/°C. These relationships will be used in the thermal impedance testing and the power cycling scheme.

5.5. Active (Power) Cycling Experimental

Active cycling of the package uses the device losses to generate heat for increasing the junction temperature of the device rather than heating the entire package with an exterior heater. The heat generated at the junction of the device creates thermomechanical stress unlike stresses that arise when the entire package is heated. For this reason, thorough reliability testing requires both cycling regimes. Active cycling schemes are outlined in the Joint Electron Device Engineering Council (JEDEC) standards and limited in their recommended maximum temperatures to no greater than 150°C. [97] A diagram from the standard on power cycling illustrating common heating and cooling methods is shown below in Figure 116.

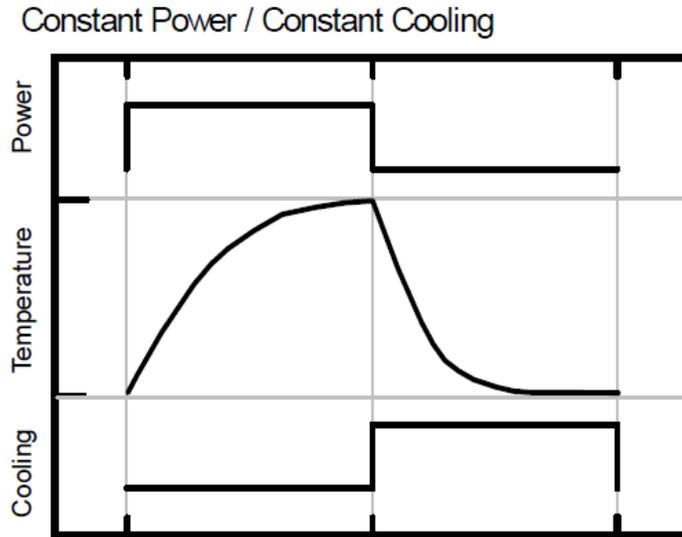


Figure 116: Representative cycle profile for power cycle testing.

Maximum junction temperatures for evaluating reliability of silicon device packages are pushing the boundaries of the device and commonly reach 175°C or higher. The JEDEC standards allow for exceeding the explicit JEDEC maximum temperature recommendations and provide guidelines for doing so.

In past research with cycle times less than one minute, single sided LTJT attachment has been reported to last beyond 66,000 cycles [30]. The failure criteria chosen for that research were marked changes in relative forward voltage and thermal resistance. Another reference stated that devices had not failed before the experiment end of 200,000 cycles [38]. Lifetimes of modules are not only sensitive to cycling temperature range but are also largely affected by the mean temperature and cycling rate [30]. Failure of a sample is most often defined as a significant change in thermal resistance, die shear strength, thermal impedance or delamination area beneath

the attached die. Although these criteria are used to assign failure, no standard definition exists and most measurements reflect relative, rather than absolute, values.

5.5.1. Experimental Procedure

The measured TSP or K-factor is used in power cycling for setting the upper and lower temperature limits of the cycle. To heat the device, the IGBT is switched on fully and a large power ($\approx 10\text{-}12\text{ W}$) is applied to the device. The V_{ge} is sampled during this period and compared to the $V_{ge\text{ max}}$ which has been translated from the measured TSP. When $V_{ge\text{ max}}$ is reached, the device power is decreased and a small current (8 mA) is applied to the gate for biasing the transistor which allows sampling of the gate-emitter voltage (V_{ge}). When V_{ge} is equal to the $V_{ge\text{ min}}$ translated from the TSP, one cycle has completed and will begin again. The time of the cycle can be adjusted by changing heating power or altering cooling with a fan or chilled plate. The cycling range temperatures can be adjusted by changing the $V_{ge\text{ min}}$ and $V_{ge\text{ max}}$ (which are directly translated to temperature using the K-factor). A schematic of the cycling process is shown below in Figure 117.

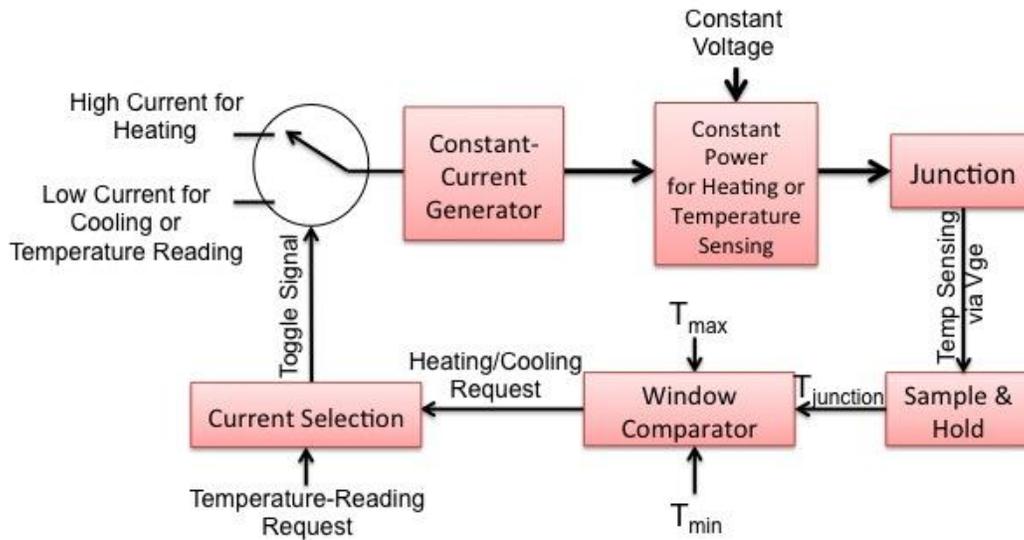


Figure 117: Schematic of the power cycling experiment.

The optimum cycle times largely depend on the package characteristics and the power limits of the test setup. The encapsulated module is difficult to heat and cool because of the large volume compared to single sided bare device attachments. It was found that approximately 10 W of power for the heating pulse allowed the module to reach 160°C in approximately 150 seconds. To make the cooling portion of the cycle symmetric, as suggested by JEDEC standards, a fan was used and the device was not attached to any heat sinking material. The Labview data monitor showing a symmetric cycle measuring approximately 300 seconds is shown in Figure 118.



Figure 118: Labview screenshot of the symmetric active cycling profile used for the active cycling experiment.

5.5.2. Nondestructive Analysis and End of Life Criteria

For package evaluation, a nondestructive method of monitoring package change as a function of cycles is necessary. The commonly accepted electrical criterion for the power module end of life is the reduction of the V_{ce} saturation voltage in the IGBT by 5%. For two terminal devices like the diode, this can mean increases in measured forward voltages of 5%. [37, 98-101]

However, a thermal criterion can also be used. If the power module steady state junction to case resistance, R_{thj-c} , increases by 20%, the module is considered “failed”. The thermal and electrical criteria occur very close to each other in time because the decrease in electrical parameters is a direct result of bond line die attachment degradation. The die attachment begins to separate from the substrate at the edges of the bond pad. This “pulling away” action is termed

delamination. As the die attachment delaminates, the area beneath the device in intimate contact decreases which translates to a proportional increase the thermal resistance.

Transient thermal measurements like thermal impedance (Z_{th}) for active devices offer another possibility for end of life assessment. The thermal impedance has been shown to accurately reflect a change in bond line delamination from cycling [102]. Other non-destructive techniques like Computed Tomography (CT) X-ray and Scanning Acoustic Microscopy (SAM) can also nondestructively measure and calculate the delaminated area beneath the device. These techniques provide a quick and accurate means for end of life determination, but can be costly.

5.5.2.1. Nondestructive Analysis using Thermal Impedance

The thermal characteristics of packaged semiconductor devices are very important in that they define the boundary conditions on the operating power. Many datasheets will report the thermal resistance parameters of their module to assist designers in observing these boundary parameters. The most often cited thermal parameter is the thermal resistance (R_{th}) which was discussed in detail in Chapter 4. Thermal resistance is a steady state measurement of how effectively heat is dissipated from the device for a given power and yields information about the entire system including devices, substrates and die interconnection. Thermal impedance (Z_{th}) is the non-steady state or transient measurement of this quantity. The motivation for utilizing thermal impedance analysis is as a means to probe only the thermal quality of the device interconnection rather than assess the thermal efficiency of all materials in the stacked structure.

Both of these models take advantage of the electrical analogies of the thermal quantities to construct RC networks which mimic the thermal RC networks of the series connected materials in a module stack. By using this characteristic of the materials in series, it is possible to assess the die interconnection by adjusting the applied power pulse time. This has been used by others as a means to evaluate the thermal benefits of sintered silver device interconnection when compared to solder [102, 103].

The thermal impedance test can be performed using the custom fabricated K-factor and power cycling test circuit and hardware. A similar test system has been used by others [102, 103]. To reduce system and user error, all measurements are performed on the same system without removing the sample.

The thermal impedance calculation is,

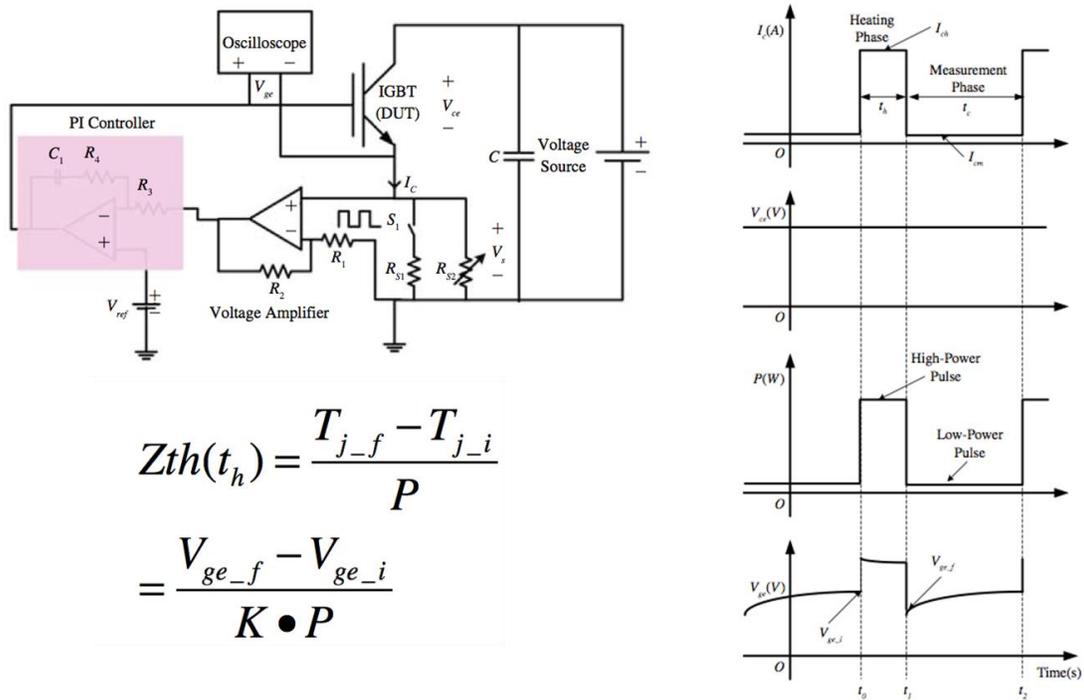
$$Z_{th} = \frac{T_{j-f} - T_{j-i}}{P} \quad (14)$$

Where T_{j-f} is the final temperature of the device junction, T_{j-i} is the initial junction temperature of the device junction and P is the power applied. Using the K-factor relationship (K), this equation can be changed to

$$Z_{th} = \frac{V_{ge_f} - V_{ge_i}}{P * K} \quad (15)$$

Thermal impedance can then be measured by applying a pulse of known power and measuring the V_{ge} before and after the pulse. The thermal impedance circuit allows the user to specify the power of the pulse and the time duration which is called the heating pulse. The remainder of the

time the gate-emitter voltage is sampled by applying a continuous 8 mA to the gate. A schematic of the circuit and an example waveform is shown in Figure 119. Due to quick cooling, linear regression analysis is performed on the data sample immediately after the heating waveform at V_{ge_f} to extrapolate the most accurate temperature. Also, a 2% duty cycle is used to avoid thermal accumulation in the device from multiple heating pulses.



$$Z_{th}(t_h) = \frac{T_{j-f} - T_{j-i}}{P}$$

$$= \frac{V_{ge-f} - V_{ge-i}}{K \cdot P}$$

Figure 119: A schematic representation of the experimental thermal impedance test bed. This is the same test setup used by others. ([103] C. Gang, H. Dan, M. Yun-Hui, C. Xiao, W. Tao, C. Xu, and L. Guo-Quan, "Transient Thermal Performance of IGBT Power Modules Attached by Low-Temperature Sintered Nanosilver," Device and Materials Reliability, IEEE Transactions on, vol. 12, pp. 124-132, 2012) Used under fair use, 2014.

The heating pulse time is carefully selected to allow heat to penetrate the die connection layer without fully passing through the substrate underneath. Many have found from previous research that a transient time of 40ms using 10 W of applied power is sufficient to thoroughly probe a single sided die interconnection [103-105]. Measurements at this time period for a

selection of materials yielded values in close agreement with calculations which include interfacial thermal impedance. An FEA model (Figure 120) of the transient thermal behavior of a large area device attached to a DBC substrate with sintered silver reveals a 40 ms pulse time allows heat to penetrate through the die attach layer without passing through to the bottom surface of the DBC. The case temperature in this simulation was fixed to a heat sink and the device was heated using 10 W of power.

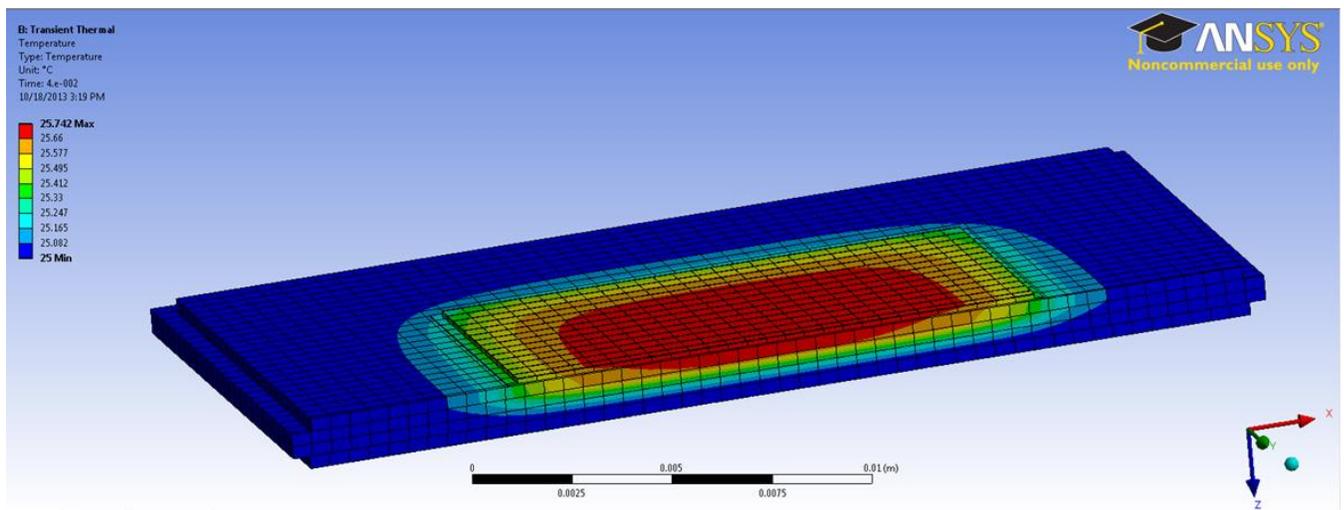


Figure 120: FEA model of transient heat flow with a 10W, 40ms pulse applied to the device. The model illustrates the depth of heat flux for thermal impedance analysis.

Transient thermal impedance measurements have been performed on single sided quarter-bridge modules during the fabrication workflow process for comparison with double-side packages. The double-side measurement was performed with the same bottom substrate and devices, but a heat sink was added between measurements. A comparison of the package thermal impedance results for both uncycled packages is shown in Table 35.

Table 35: Comparison of Thermal Impedance measurement of the single and double-side quarter-bridge modules before any cycling has occurred.

	Single Side Quarter-Bridge	Double-side Quarter-Bridge
Transient Thermal Impedance (40ms heating pulse)	0.1104 K/W	0.0735 K/W

The 40 ms heating pulse works well for single sided attachment, but with the large thermal mass attached to the top of the device, it is not known how well this heating pulse will accurately probe the top die attachment interfaces. In an effort to capture changes in bond quality for the top side tubing interface and consider the effects of encapsulation, the heating pulse was increased to 100 ms. A comparison of the different time intervals can be seen in the FEA transient thermal analysis plots below in Figure 121.

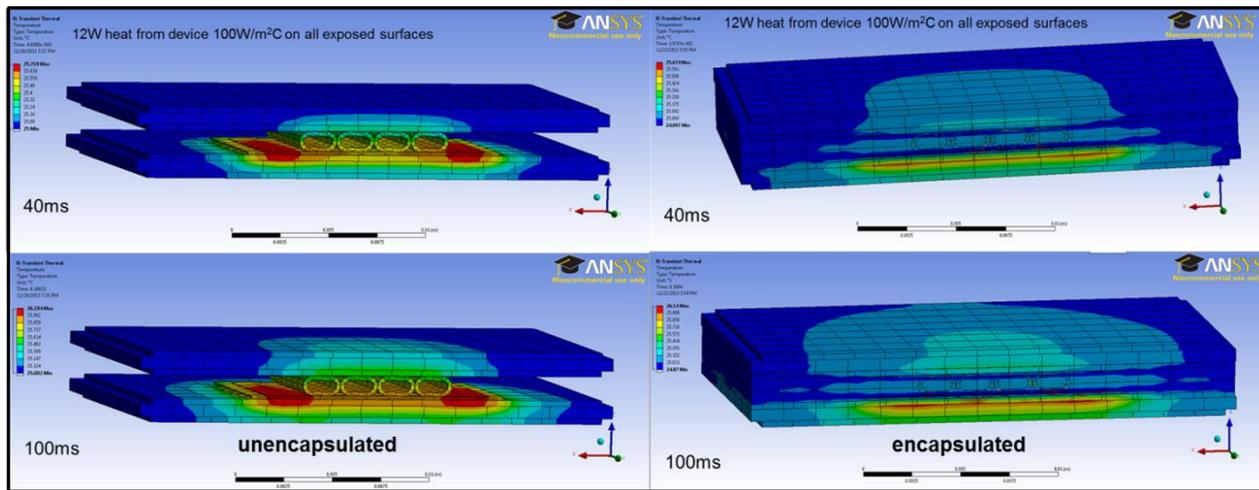


Figure 121: Comparison of heat distribution for 40ms (top) and 100ms (bottom) heating pulses in encapsulated (right) and unencapsulated (left) device packages.

By utilizing the same test setup for power cycling and thermal impedance measurement, the test could be stopped easily at specified cycling periods for ex-situ Z_{th} measurements. At each sampling period, ten thermal impedance measurements were performed. The average is plotted

with error bars indicating one standard deviation above and below the average. The results of the thermal impedance trend versus power cycles can be seen in Figure 122.

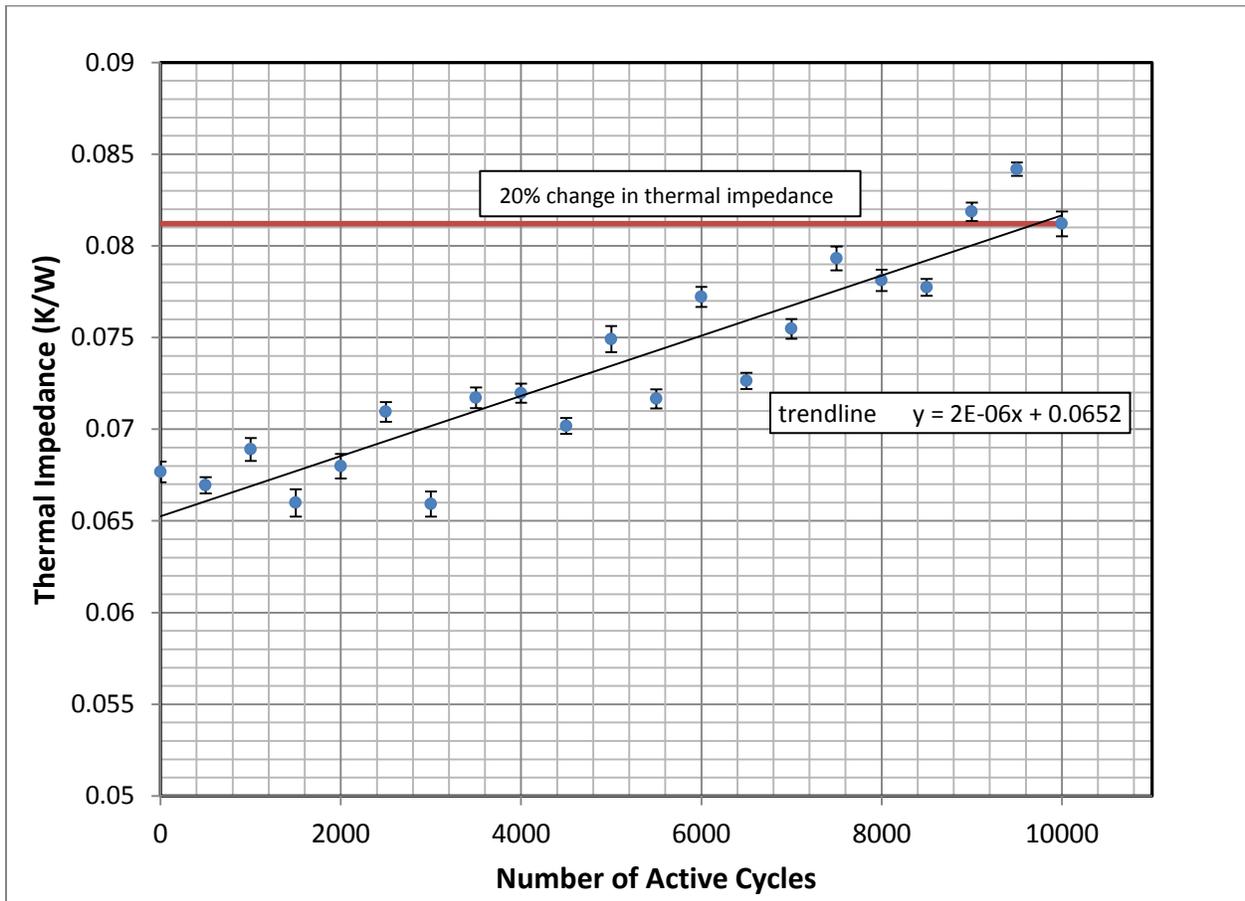


Figure 122: The measured change in thermal impedance with 100ms pulsed power as a function of active heating cycles. The heating cycle was a 5 minute symmetric cycle with a temperature range from 40°C to 160°C.

In the graph, a red line was added marking a 20% increase in Z_{th} from the 0 cycle Z_{th} measurement. A trend line was also added to aid in calculating future thermal impedance measurements as a function of cycles. Although, the Z_{th} measurement indicates a failure in the module, it is not clear how the accepted definition applies to the double-side package. For example, the Z_{th} measurement in this case is an assessment of not one, but two interfaces. With

Z_{th} measurements alone it is impossible to determine which interface has failed and to what degree.

5.5.2.2. Nondestructive Analysis Results using X-ray Computed Tomography

For power cycling, a functioning switch (IGBT) is heated using the device losses. Functional power modules have very large footprints and the devices themselves are both large area devices with footprints exceeding 10 mm x 10 mm square. The X-ray Computed Tomography (CT) technique is capable of performing X-ray analysis on very large specimens making it an ideal nondestructive technique for inspection of the module interfaces.

An example of a large area X-ray image of a full half-bridge module can be seen in Figure 123. This is an image of a module that has not yet been cycled and the focus plane is between the tube and top substrate. This large view presents X-ray images characteristic of both sintered silver interfaces and soldered connections. The pores and voids in the SAC 305 solder, used for tab attachment on both sides, are apparent and large. No voids can be seen in the sintered interface at or around the tube structures.

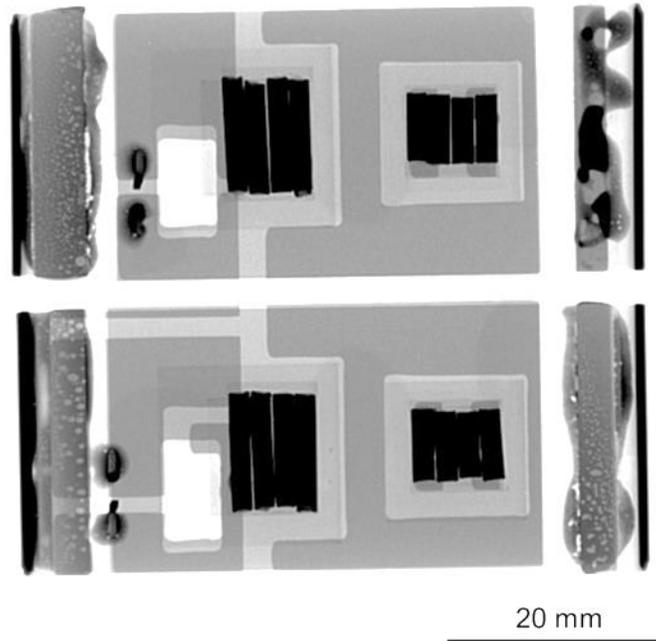


Figure 123: A large area scan of a fabricated half-bridge module using X-ray Computed Tomography (CT).

Figure 124 and Figure 125 show X-ray images of an uncycled quarter-bridge module's tube-die interface. These two images show no visible voids in the sintered silver layer. All of the tube "flats" in Figure 125 are uniform in color with no appreciable voids which verify the integrity of the joint.

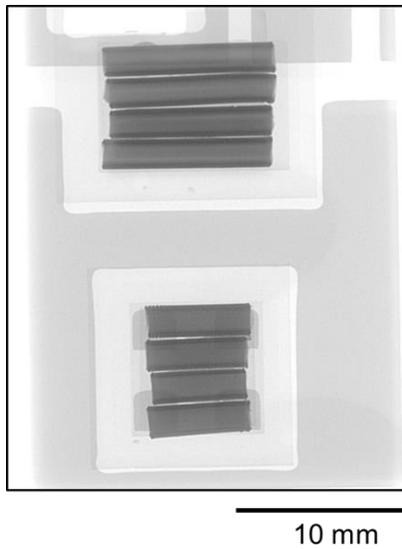


Figure 124: A large area scan of a fabricated quarter-bridge module using X-ray Computed Tomography (CT).

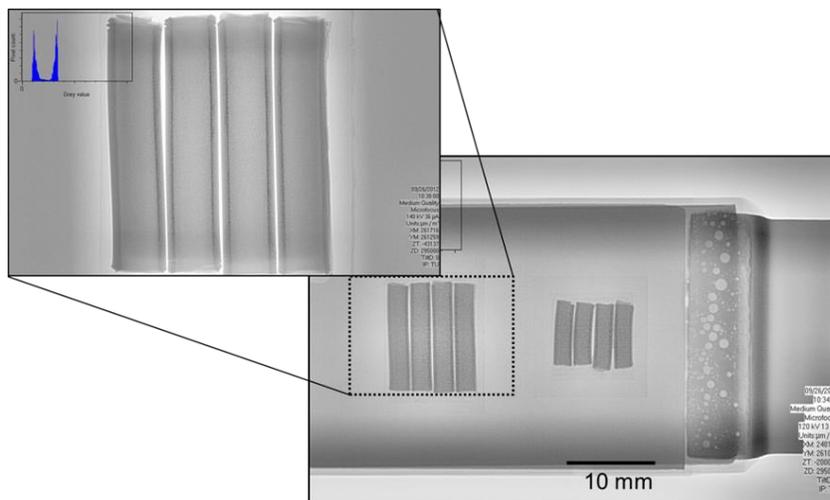


Figure 125: A large area scan of a fabricated quarter-bridge module showing uniform bonding of tubes (enlarge area) and voids in SAC solder using X-ray Computed Tomography (CT).

Multiple X-ray images are necessary for inspecting all interfaces in the double-side planar package. X-ray images of the cycled quarter-bridge module can be seen in Figure 126. This module survived 10,000 active cycles before an increase in thermal impedance indicated failure. The upper image (Figure 126a) reveals the embedded thermocouples which were used for K-

factor temperature calibration and DC power testing. This image is focused on the sintered silver bond line between the top substrate and tube flats. The lower image (Figure 126b) is focused on the sintered silver bond line between the IGBT and tube.

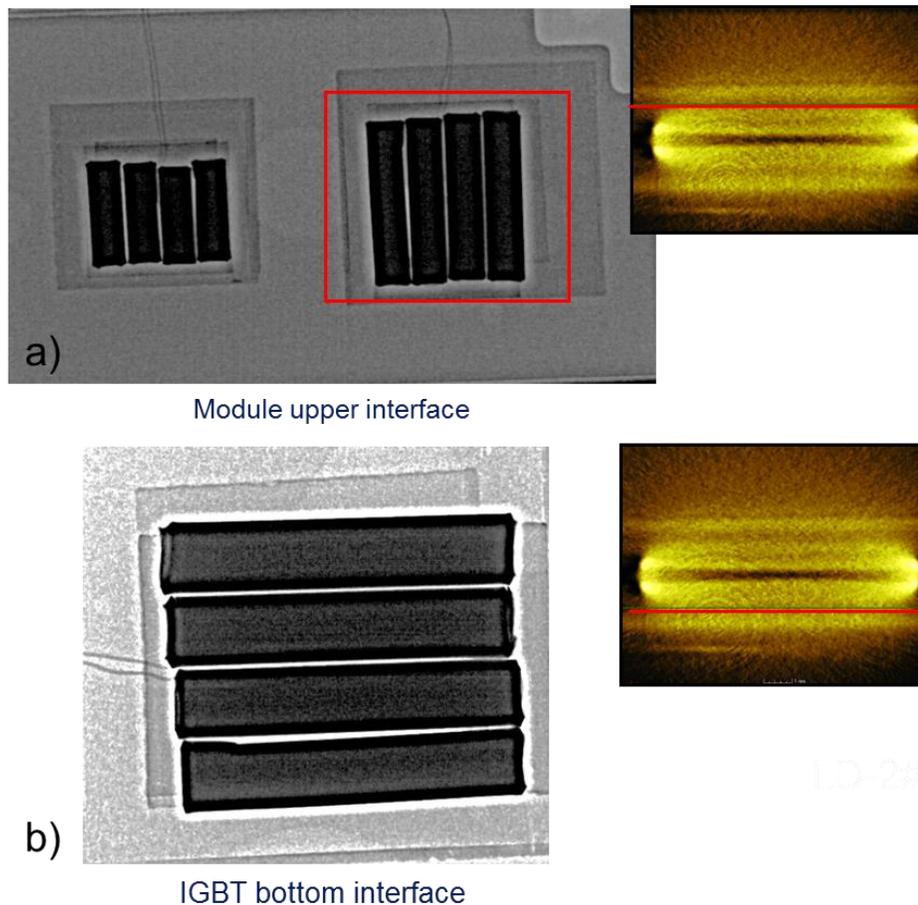


Figure 126: Tube substrate interface (a) and tube die interface (b) X-ray images of a quarter-bridge module that has been actively cycled for 10,000 cycles

The IGBT interface is of great interest because this device was used for providing the heat required to actively cycle the package and the thermal impedance measurements are a direct reflection of these interfaces. The diode thermal impedance was not measured because the measurement test bed was not capable of performing measurements on two terminal devices.

Observations of the tube interfaces above the IGBT do not strongly suggest any delamination. The border of each tube is dark revealing the elliptical shape of the structure, but the bonding flats of each tube are light and uniform in color indicating a complete bond without delamination. Closer examination reveals some “grainy” texture inside these areas, but it isn’t clear if these are voids or surface texture from tube fabrication.

5.5.3. Summary

In summary, the double-side power module survived 10,000 active (power) cycles from 40°C to 160°C. The cycling routine consisted of symmetric heating and cooling pulses for a total cycle time of 300 s. The frequency and mean temperature do not allow direct comparison with other benchmark tests. Nondestructive thermal impedance, Z_{th} , testing indicated module failure which has been previously defined as an increase in thermal impedance of 20%. Nondestructive X-ray CT images were used to verify joint integrity in an effort to determine which interfaces are responsible for changes in Z_{th} . These images did not reveal any loss of bond integrity on either interface within the quarter-bridge module.

5.6. Passive (Thermal) Cycling Experimental

Passive thermal cycling is the process of repeatedly exposing the entire package to a range of temperatures. This can be accomplished by placing the entire package in a furnace which ramps up to a setpoint temperature and then immediately cools down to a lower setpoint temperature. Cycling schemes with outlines on ramp rate and accuracy are outlined in the Joint Electron

Device Engineering Council (JEDEC) book of standards [106]. An example cycling protocol from the JEDEC thermal cycling standard is shown in Figure 127.

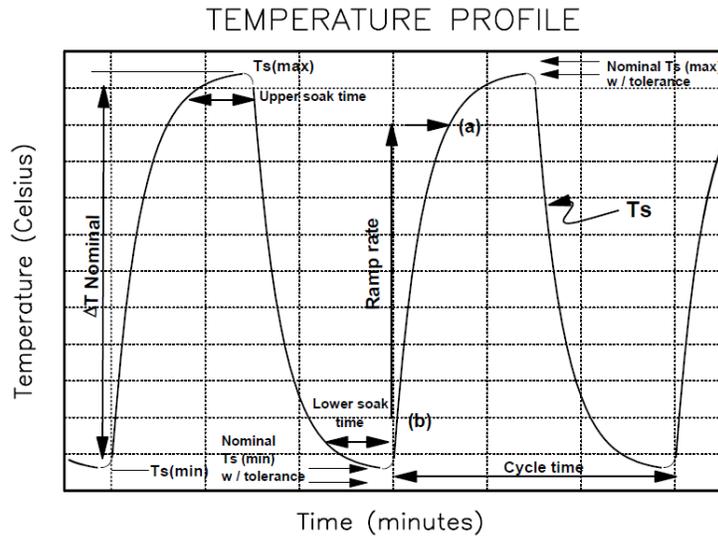


Figure 127: Representative temperature profile for thermal cycle test conditions.

However, the suggested standard passive profiles are limited to maximum temperatures of 150°C. The minimum temperatures for standard profiles are as low as -60°C. Increasingly, in an effort to push the limits of the package and devices, the maximum cycling temperature for packaged silicon devices has approached 175°C. [39, 107]

5.6.1. Experimental Procedure

To accomplish a temperature range of -55°C to 175°C in a reasonable amount of time, a thermal cycling scheme was developed using a Tenney environmental chamber and a heating plate. The chamber is capable of maintaining a constant low temperature of -65°C. The samples are placed

on a heating plate inside with thermal interface paste. A hot plate with samples mounted is shown in Figure 128.

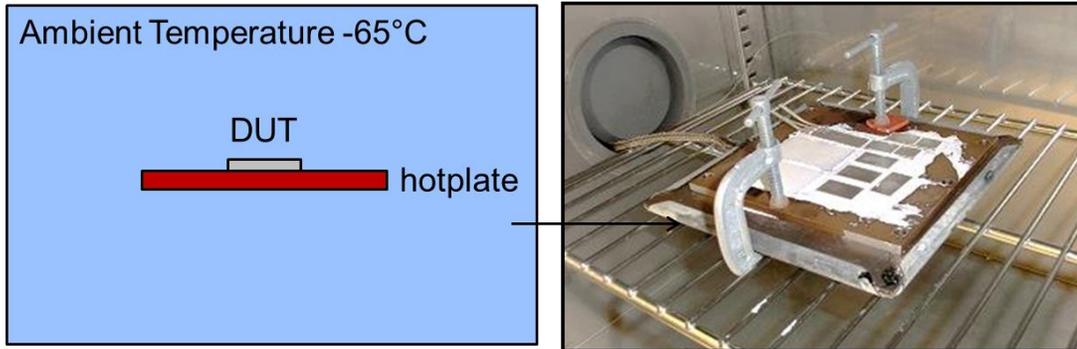


Figure 128: Image of passive cycling experimental setup using a constant ambient temperature in a chamber and a hotplate for applying heating pulse of cycle.

A controller, timer and counter directly outside the chamber control the temperature and cycle time. Heating plate power is controlled by adjusting input power. The temperature is monitored using four thermocouples attached to various places on the hot plate and recorded using a iOTech DAQ with software. The chamber and controller system is shown in Figure 129.

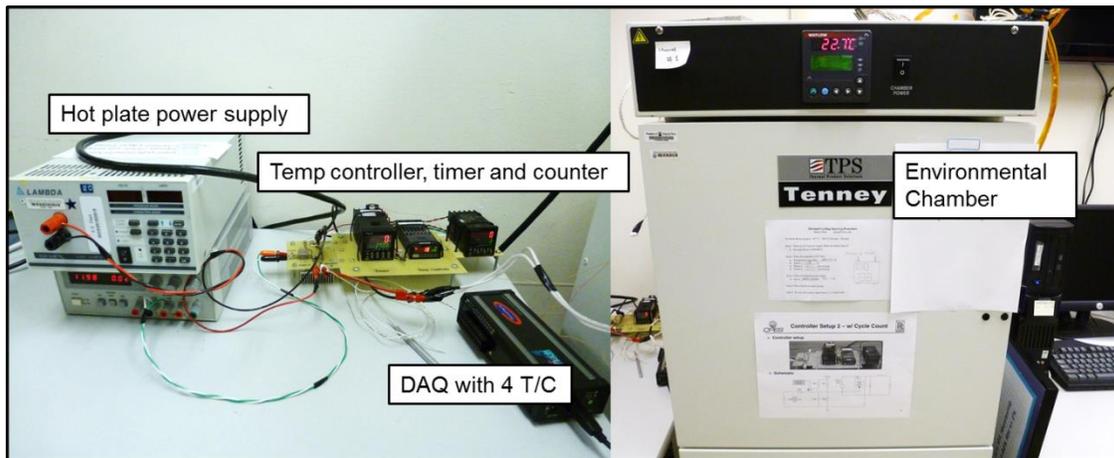


Figure 129: The temperature chamber and control system used for passive thermal cycling experiments.

Lifetimes for thermally cycled packages vary widely and are strongly influenced by cycle rate and dwell times at the maximum and minimum temperatures. Many references utilize a dwell time at the top and bottom temperature which result in decreased lifetimes. References exposing single sided sintered silver LTJT samples to a cycling range of -40C to 125°C have reported failure times approaching 1500 cycles [39]. Others using more extreme cycling ranges of -50°C to 175°C have reported lifetimes approaching 650 cycles [38].

For the task of passive cycling, twelve diodes were packaged in the double-side package with the corrugated tube structure between the device and the top substrate. Four of the packages were encapsulated using the same encapsulation outline in the fabrication section. Characteristic packaged samples are shown in Figure 130. Package I-V characteristics were recorded before cycling and the forward voltage (V_f) of the diodes were measured periodically in an effort to establish a relationship between deteriorating bond quality and interface resistances. A second method to monitor package failure uses nondestructive X-ray imaging at different cycling intervals.



Figure 130: Samples constructed for passive thermal cycling experiments. Four samples with encapsulation (top) and eight without encapsulation (bottom) were constructed.

5.6.2. Nondestructive Analysis

5.6.2.1. Forward Voltage Measurement Results

One nondestructive quantity that has been used in previous research as an indication of die attachment deterioration is the change in the forward voltage of the packaged devices [30, 108]. The V-I characteristics of the twelve double-side diode packages were measured with a Tektronix high power curve tracer every 50 cycles. The forward voltage (V_f) change at 10 A was monitored and recorded. The encapsulated diode packages are plotted separately (Figure 131) from the unencapsulated packages (Figure 132) because of the expected difference in lifetimes. Each graph has additional lines marking the expected datasheet and failure ($\Delta V_f=20\%$) values.

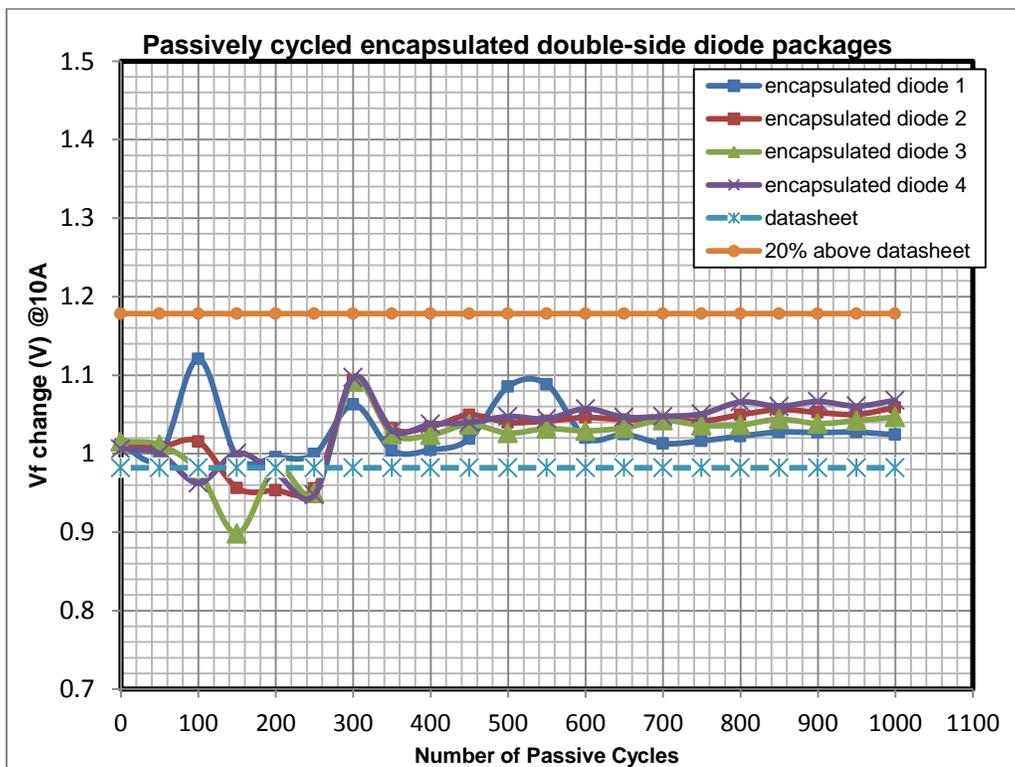


Figure 131: Forward voltage (V_f) change of passively cycled (-55°C to 175°C) encapsulated double-side diode packages.

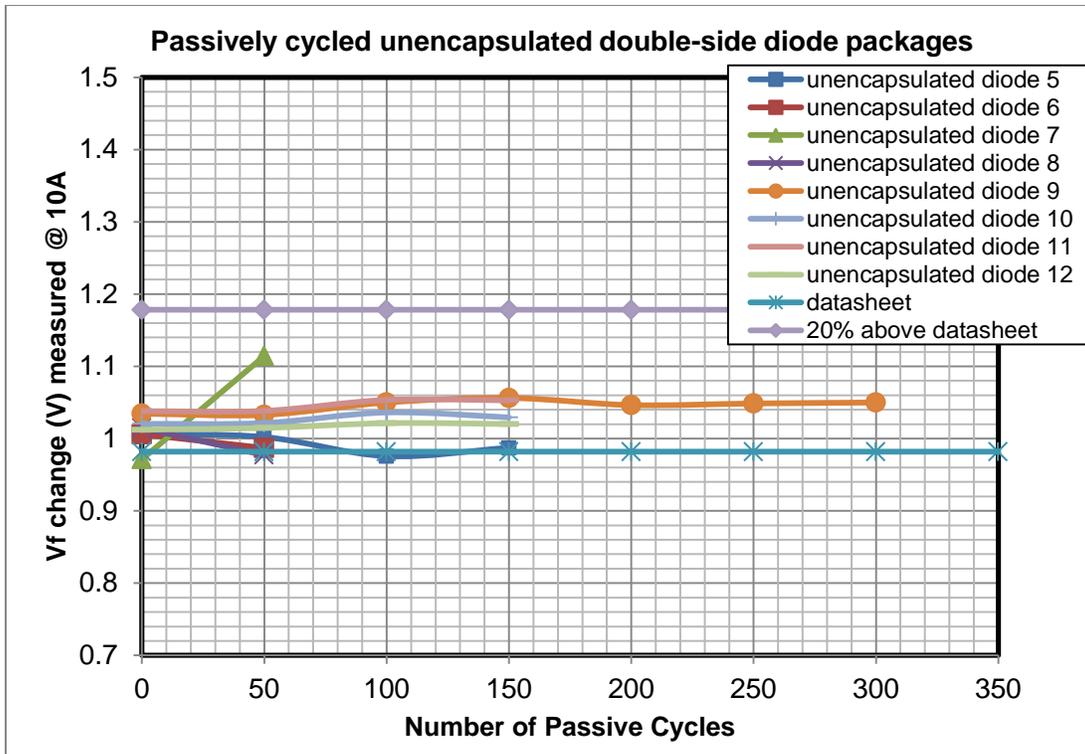


Figure 132: Forward voltage (Vf) change of passively cycled (-55°C to 175°C) unencapsulated double-side diode packages.

The obvious differences in lifetime between packages with and without encapsulation can be seen in the graphs. For the unencapsulated packages, most of the packages did not exceed 150 cycles. One outlying sample survived 300 cycles before failure. Failure in each package was catastrophic and forward voltage measurements gave no indication of imminent failure. Encapsulated packages experienced no failures or significant changes in forward voltage measurements to 1000 thermal cycles.

5.6.2.2. Optical Microscopy

The failed unencapsulated diode modules were not difficult to inspect. Failures in each of the modules occurred at the interface between the tube and die. These surfaces indicate a mix

between failure at the die surface and failure at the tube surface. The failure surfaces can be seen in Figure 133.



Figure 133: Images of failed diode package sample 6 showing combination of failure modes at die and tube surfaces.

Without encapsulation, these surfaces were exposed to moisture and failed samples revealed large amounts of condensation at the silver interface which is thought to have further contributed to decreased lifetimes.

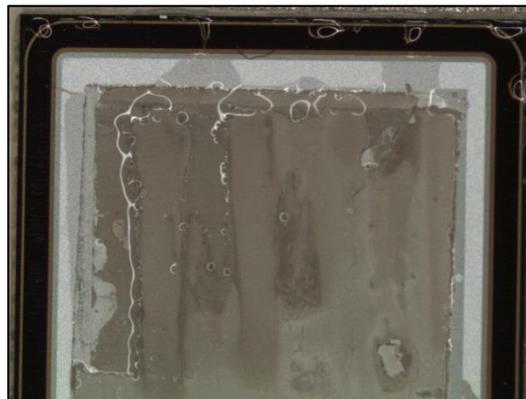


Figure 134: Failure surface of double-side diode package showing excessive amounts of moisture at the top sintered interface.

5.6.2.3. Computed Tomography X-ray

X-ray techniques were used to assess degradation of the interfaces in both types of module packages. Because the unencapsulated modules failed catastrophically and their failure surfaces are easily accessible, the X-ray was employed to look at the hidden interfaces between the die and substrate or substrate and tubes. The X-ray images of the failed unencapsulated modules did not reveal any deterioration of the underlying die-substrate or tube- substrate interfaces. An example X-ray image of a failed package can be seen in Figure 135.

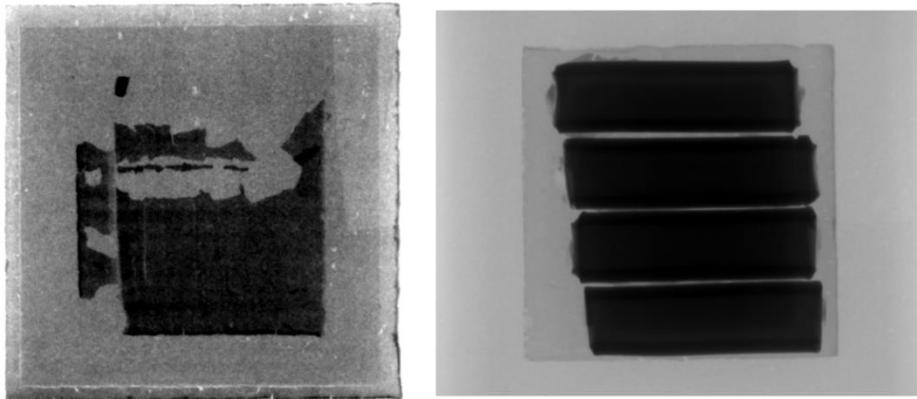


Figure 135: CT X-ray image of failed unencapsulated diode package.

For the encapsulated modules, X-ray offers a nondestructive way to view each of the interior interfaces. All four of the encapsulated samples survived 1000 passive cycles with no indication of interface failure from forward voltage measurements. Images of the top tube-substrate bond line for all four encapsulated modules can be seen in Figure 136. The cathode and anode connections to the substrates can also be seen clearly. These silver ribbon connections were sintered to the bottom and top substrates for electrical testing. The sintering profiles were identical to the diode and tube attachment.

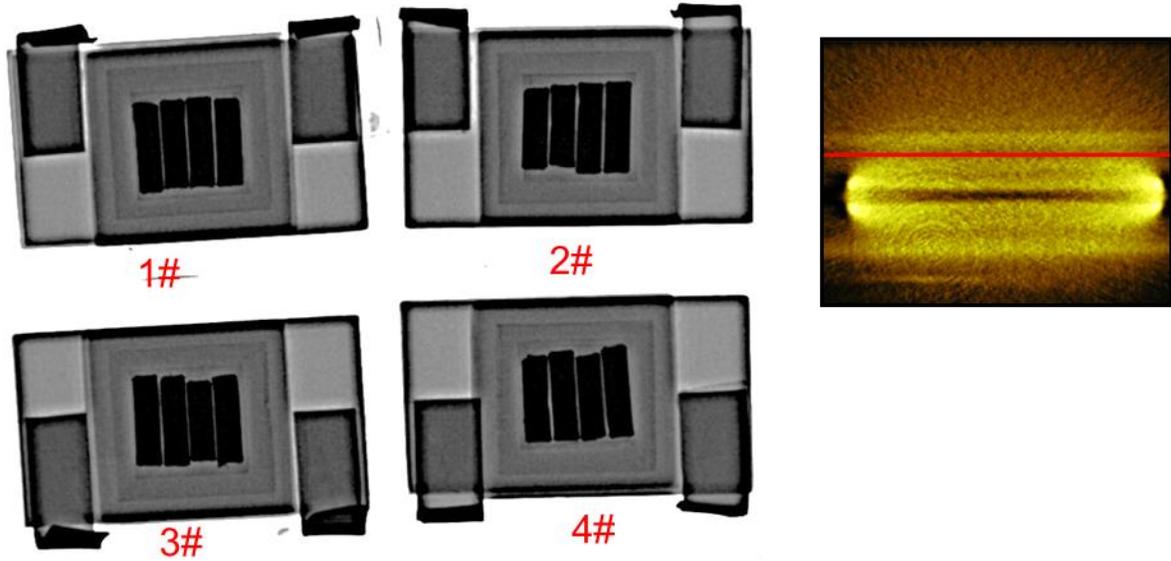


Figure 136: Low resolution CT X-ray images of encapsulated double-side module packages which survived 1000 thermal cycles.

The top interfaces in these samples are difficult to view because of the compliant layer thickness. The lower interface, the tube-diode bond line, reveals a much clearer image. An image characteristic of this lower interface can be seen in Figure 137.

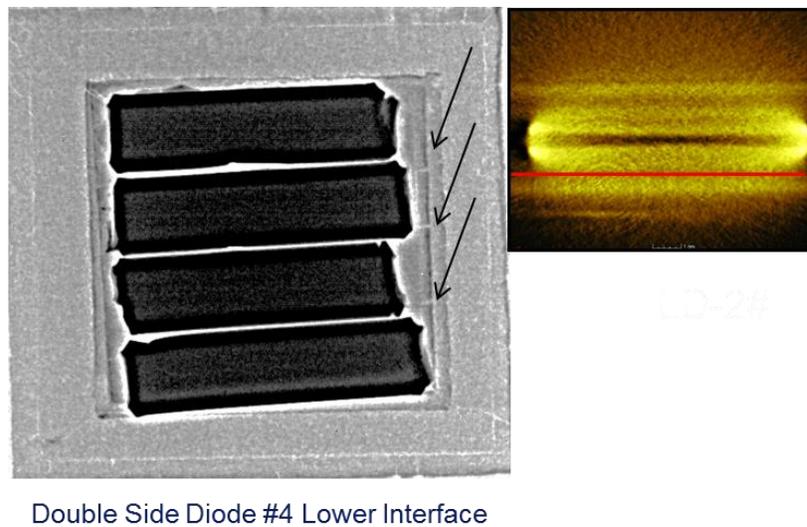


Figure 137: High resolution CT X-ray image of the tube-substrate interface for the encapsulated sample number four which survived 100 thermal cycles.

The lighter inner rectangular regions of the tube are the bonding flats. The darker regions around the edges are the elliptical tubing walls that are not bonded to either surface. The inner rectangular regions appear “grainy”, but no obvious delamination has occurred at the edges or ends of the tubes. Closer examination of the sintered silver footprint outside the area of the bonded tubes seems to show signs of small crack propagation (indicated by arrows). These cracks appear to be aligned with the tubing ends. It is unclear from these images which of the two interfaces are affected by these cracks and to what degree. Cracking was not observed in any of the other three samples.

5.6.2.4. Scanning Acoustic Imaging

Scanning Acoustic Microscopy (SAM) provides another method to probe the hidden interfaces in a power electronics package. Many times it is necessary to utilize the combination of X-ray and SAM for accurate interface analysis. The X-ray images of failed unencapsulated modules in the previous section revealed very little information about the interfaces. SAM imaging was used to look specifically at the interface between the die and substrate as well as any delamination within the substrate. It is known that alumina based DBC substrates fail very quickly in a passive cycling regime by delamination. SAM images of failed modules can be seen in Figure 138.

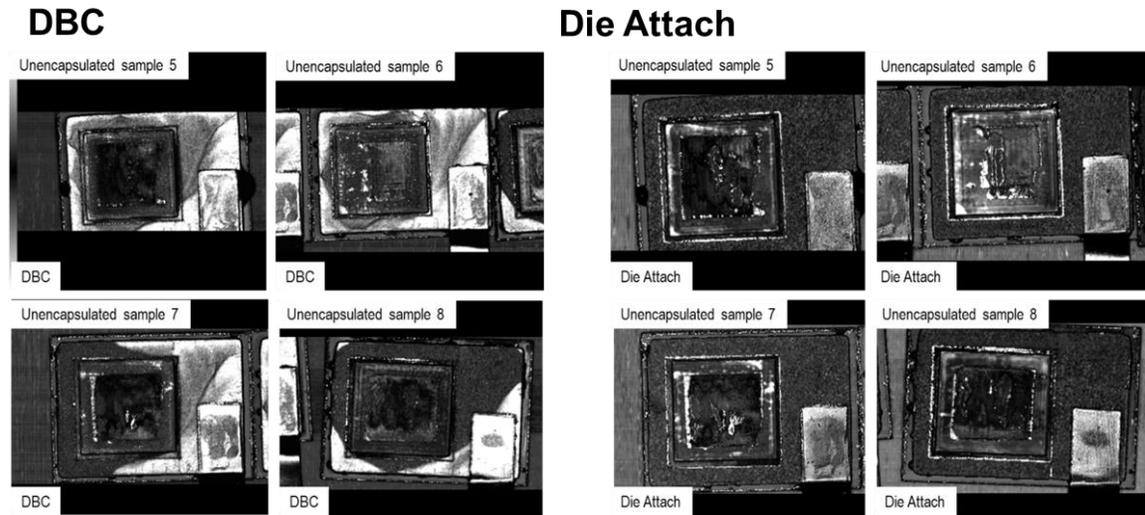


Figure 138: SAM images of failed unencapsulated diode modules for inspection of the DBC (left) and the die attachment (right).

A significant amount of substrate delamination can be seen in the left-hand SAM images of Figure 138. By contrast, the SAM images on the right reveal no delamination of the die attachment.

5.6.3. Destructive Analysis

A common destructive method for evaluating die attachment strength is to measure the required amount of shear stress to remove the device from the substrate. It is not clear that a target die shear strength standard exists, but it is commonly thought that higher die shear strength is preferred. Poor die shear strengths are normally associated with delamination, poor thermal quantities and higher than average electrical resistance. Die shear testing for large area devices (>100 mm²) requires special equipment because the forces involved are much higher. The diodes for this experiment are 10 mm x 10 mm and high die shear forces are expected. The die shear data for four of the eight failed unencapsulated packages is shown in Table 36.

Table 36: Die shear testing of four failed passively cycled unencapsulated double-side diode packages.

Sample	Die Size (mm ²)	Test Shear (kg)	Shear Stress (N/mm ²)	Observations
5	100	192.7	18.89	Entire chip removed
6	100	121.0	11.86	½ the chip remained on substrate
7	100	469.0	45.99	Majority of chip remains on substrate
8	100	511.6	50.17	Majority of the chip remains on substrate

The data for the die shear shown above are largely promising in that three of the four tests broke the device before breaking the sintered interface. The fourth value (sample 5) had a die shear strength of 18.89 MPa even after module failure.

To evaluate the strength of the tube-substrate bonding, a destructive shear test was also performed on 16 tubes sintered to a DBC substrate using similar processing parameters as the double-side diode packages. The tubes attached to the substrate, failure surfaces and shear stress data can be seen below in Figure 139. Because the tubes had different bonding areas, the failure surfaces were measured and the shear stress was calculated based on the measured bond area.

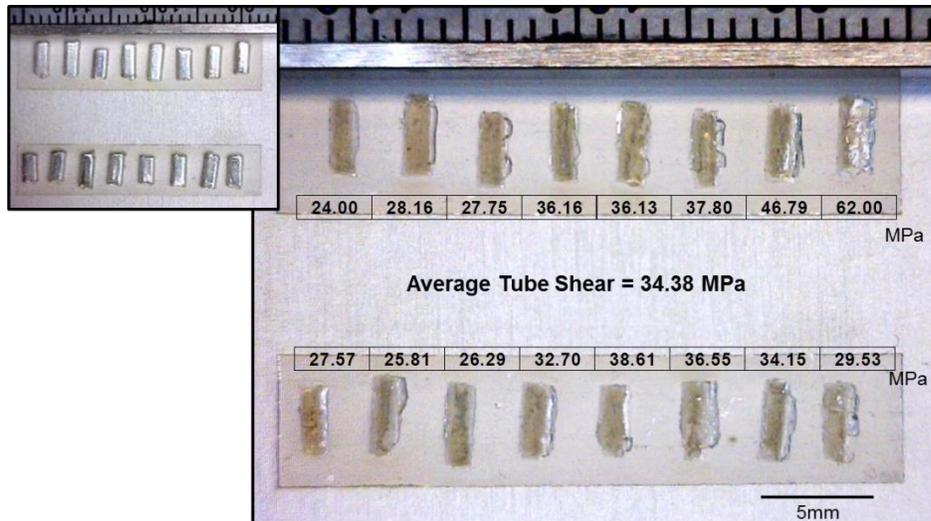


Figure 139: Die shear evaluation of tube bond integrity before cycling.

The average tube shear strength was measured to be 34.38 MPa. Although these tubes were not cycled, the magnitude of initial shear strength suggests failure will not likely occur in the interface above the tube compliance layer.

5.6.4. Summary

In summary, the double-side diode modules without encapsulation failed, on average, at 150 passive thermal cycles although at least one survived 600 cycles. Utilizing nondestructive methods it was found that the mixed mode failure at the die tube sintered interface was most likely a combination of moisture penetration and DBC delamination. Both destructive and nondestructive analysis of these samples confirms the die attachment was largely unaffected. The encapsulated diode modules had not failed by the test end of 1000 cycles. Due to the encapsulation, only nondestructive X-ray analysis was used to probe the interfaces.

Chapter 6. Further Developments in Double-Side Cooling

This research successfully fabricated functional planar power modules which utilize double-side cooling to improve their thermal performance and reliability. The entire structure was made possible by using sintered silver LTJT and a compatible compliant interface. More than just proving the feasibility of the structure, it also verifies that sintered silver LTJT can successfully replace solder and wirebond technology in large scale power electronics package manufacturing. Even as this document was being written, more progress was being made in lowering the manufacturing barriers for utilizing sintered silver. A new nanoscale silver paste formulation has recently been introduced that will allow the entire fabrication process outline in Chapter 3 to be simplified further by removing the applied pressure during sintering.

In reality, this project utilized silicon devices and low cost alumina DBC substrates as proof of concept. There are many improvements that are now possible to make better double-side modules using this research as a guideline. The topics of greatest importance for the future double-side modules are shown in the flowchart of Figure 140 which outlines this chapter.

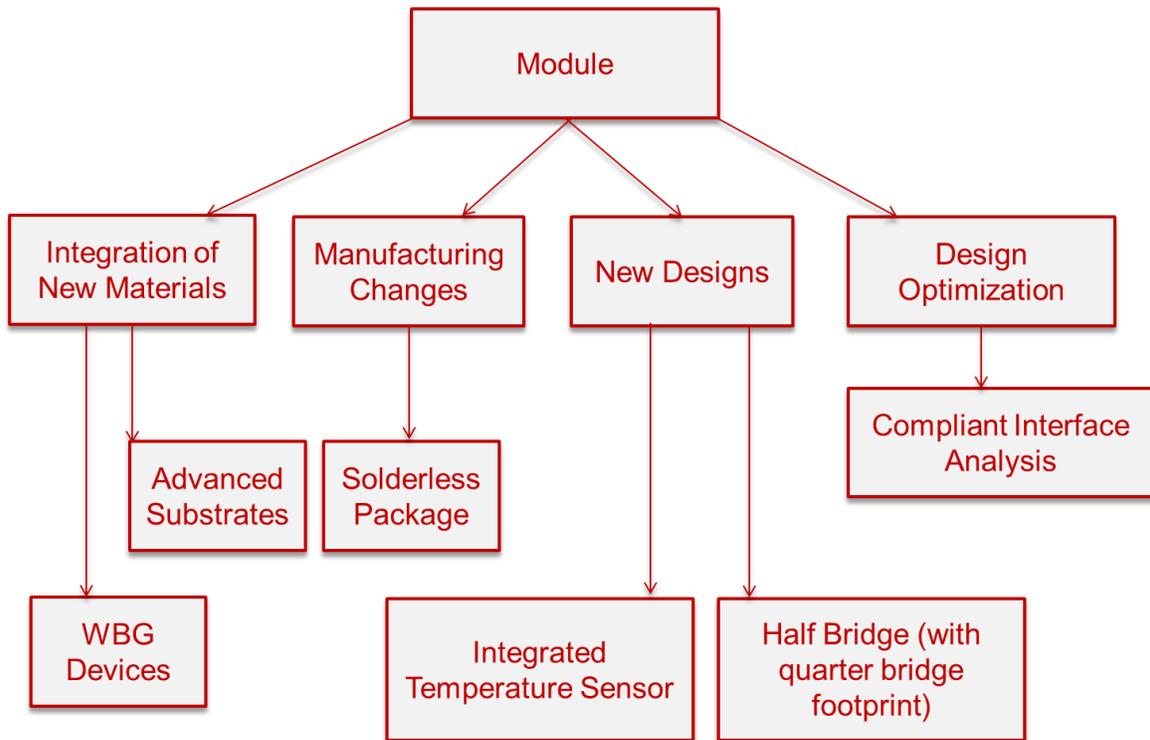


Figure 140: Outline of possible improvements for securing the future of double-side power modules using sintered silver device interconnection.

6.1. Integration of New Materials

Substrate technology has provided the power electronics packaging community with a great number of alternative high temperature and high reliability substrates. First, DBC technology has seen increased competition from new direct bond aluminum (DBA) substrates. The DBA substrates have revealed longer cycling lifetimes due to the lower modulus of aluminum which reduces fatigue from work hardening. The DBC eutectic copper bonding process has also been improved with newer DBCs being constructed using active metal brazing (AMB) of the copper

cladding. The AMB DBC boasts significant cycling lifetime improvement over previous eutectic bonded DBCs.

The insulating layer in the DBC has shown the largest improvements recently with new ceramics for increasing fracture toughness and thermal conductivity. The most common insulating ceramic layer today is alumina and it is relatively inexpensive and very easy to obtain. Silicon nitride (Si_3N_4) is more costly, but has nearly twice the fracture toughness making its expected cycling lifetime greater than alumina. Silicon nitride has almost double the thermal conductivity of alumina.

By simply using a thinner substrate made from DBA with an insulating ceramic of silicon nitride, the lifetime, and thermal conductance of the module will be increased while reducing the weight and volume further. Figure 141 shows the first prototype of a double-side quarter-bridge power module constructed using a silicon nitride DBA provided by DOWA Electronics Materials. In the past, the difficult process of making the DBA surface compatible with the sintered silver LTJT was too great to make large scale production feasible. These substrates were provided by DOWA with the surface metallized for direct substitution into the process workflow. The improvements in material properties are also shown in Figure 141.

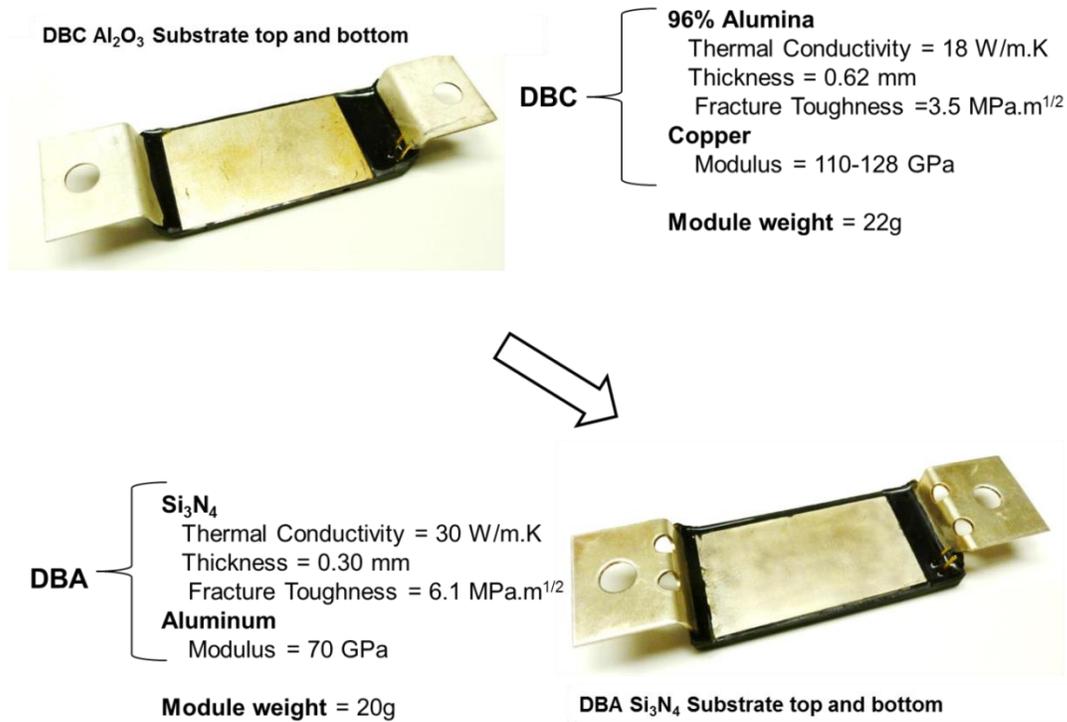


Figure 141: Quarter-bridge module improvements utilizing metallized DBA substrates with Si₃N₄ isolation layer.

Available semiconductor devices are also progressing quite rapidly. With the increased application temperatures of wide bandgap devices like silicon carbide, many have simply started substituting the devices into the older more conventionally constructed module packages which only negate their high temperature benefits. To reach their full potential, it is necessary to not limit their performance with failure prone solder and wirebond packages. And although these devices are limited in their current and voltage ratings, their power density is significantly higher. The silicon IGBT used in this study has an available footprint measuring 182.3 mm². The power density is therefore, 988 W/mm². Available SiC devices have footprints 10X smaller with current ratings of about 20-35% that of the silicon devices. This translates to approximately 3X the power densities of silicon devices. A power density comparison of commercially available silicon carbide MOSFETs to the silicon IGBT is seen in Figure 142.

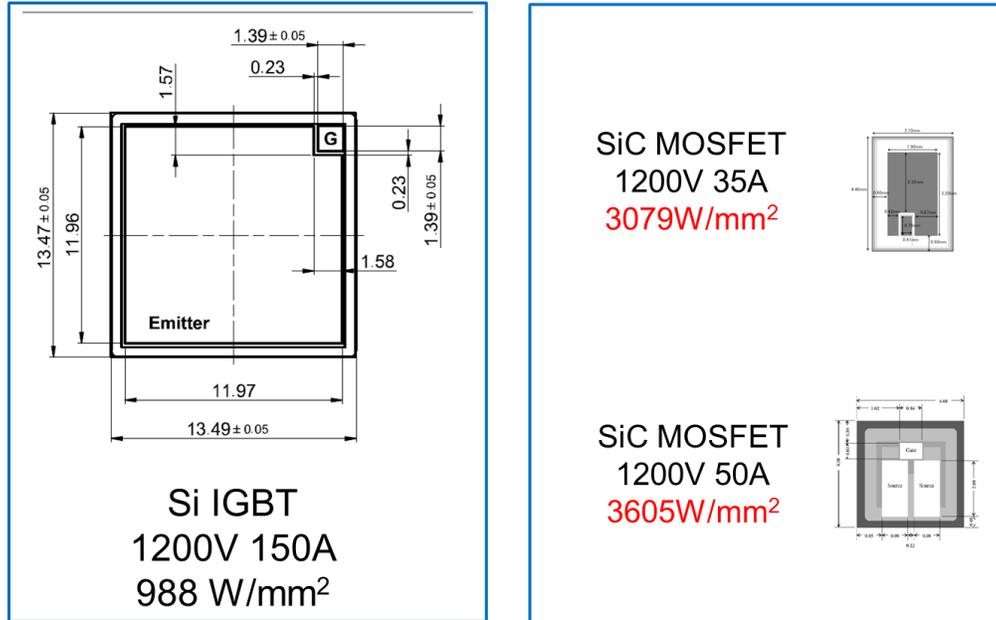


Figure 142: Comparison of high power silicon IGBT to high power silicon carbide MOSFETS.

With the large increases in power density come large increases in heat and SiC power electronics packages will undoubtedly require increased thermal management. The decreased thermal resistance of double-side cooling coupled with the benefits of sintered silver device attachment is well-suited for meeting the future needs of SiC packages. Early prototype SiC packages using sintered silver attachment for the devices and the leads can be seen in Figure 143. The devices in this image are mounted onto a Si₃N₄ AMB DBCs for enhanced lifetime. The future packages are destined to include a SiC diode and a top heat sink. Research on appropriate UBM schemes and processing are ongoing.

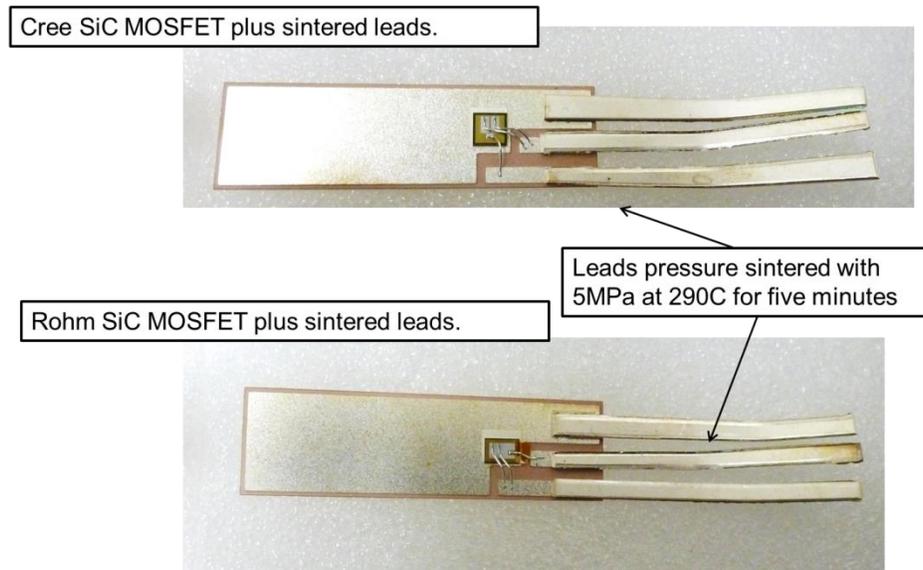


Figure 143: Single-sided prototype SiC packages using sintered silver devices and leads.

6.2. Manufacturing Improvements

Sintered silver LTJT has not, in the past, been labeled as a commercially viable technology. Although the cited barrier to manufacturing has been the need for pressure during sintering, the true barrier has, in many ways, been the displacement of the solder and wirebond technologies which are mainstays in manufacturing. The module workflow for this research illustrates the ease of integrating the sintered silver workflow into a production process. Each part of the module can easily be constructed in mass by current module suppliers. However, on a small scale, certain improvements in the fabrication will make the module better.

The largest improvement in fabrication is in the module tab alloy and attachment scheme. The nondestructive analysis of the double-side module in this research revealed the large voids of the

SAC solder used in both the tab and gate-emitter pin attachment. Additionally, the tabs are oversized for the application and the gate-emitter tabs are not an industry standard connection. In the future, the package would benefit from sintered terminal connections. The downside to sintering the terminals is choosing an affordable metal that is still compatible to sintered silver. Attempts have already been made to implement these improvements. Some of the improvements can be seen in Figure 141. The electrical tabs have had stress relief holes punched at the bends to reduce bending stress and the alloy for the tabs are a silver clad copper which reduces cost but continues to be compatible with silver sintering. The leads in Figure 143 were added using pressure sintering processes which should be viable for larger tabs as well. With these improvements, the modules will be solder-free and easier and cheaper to manufacture.

6.3. Future Designs

To push the three-dimensional architecture even further, a half-bridge configuration based on two quarter-bridge switching units has been proposed. The symmetry of the quarter-bridge module has already been shown to allow for in-plane half-bridge configurations. By arranging the symmetrical units in the z-direction, a half-bridge configuration can be realized in the same footprint as the original quarter-bridge module. An illustration of this configuration can be seen in Figure 144.

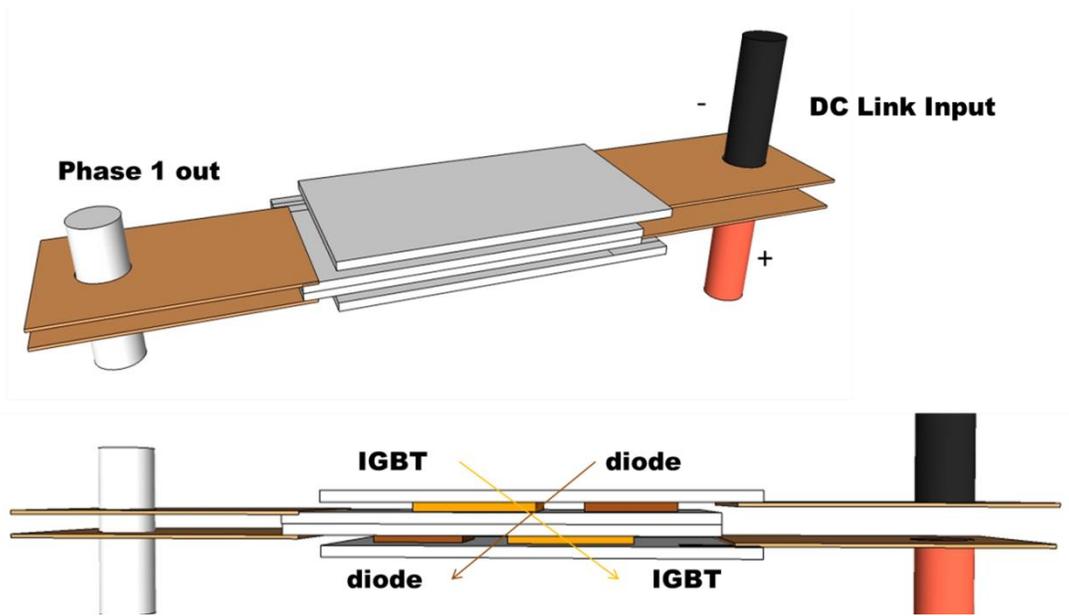


Figure 144: Alternative half-bridge configuration by further expansion in the Z-direction.

With this configuration, cooling can be added to the bottoms of both modules. The input DC bus voltage connections will be located together on one side of the module. The phase output can be realized from shorting the terminal at the other end (high-side emitter and low-side collector terminals). The IGBT devices will be located 180° from each other which is ideal thermally. The only real barrier for this configuration is the gate-emitter signal input locations.

Chapter 7. Summary and Conclusions

The future of power electronics requires innovations in packaging architecture as well as new materials. The planar power module clearly pushes the architecture in the right direction; upward. This research has presented a novel three-dimensional design that is made possible using a compliant interface and sintered silver LTJT. This research has investigated the double-

side structure with emphasis on the electrical and thermal benefits of the design, the compliant interface, and the sintered silver die attachment.

This investigation has accomplished:

1. Design of a three-dimensional power module architecture based solely on sintered silver die interconnection using 1200 V, 150 A silicon power semiconductor devices.
2. Design of an alternative compliant interconnection which is compatible with sintered silver device attachment and specifically designed to alleviate thermomechanical stresses in double-side packaging.
3. Electrical evaluation of the double-side power module using static and dynamic measurement techniques.
4. Experimental and numerical evaluation of the package thermal characteristics and thermal contributions of the compliant interface.
5. Experimental and numerical evaluation of the reliability of the alternate interconnection scheme under power cycling and temperature cycling conditions.

7.1. Design and Development of Double-side Planar Power Modules

In this section, a 1200 V, 150 A power module design was constructed based on half-bridge and quarter-bridge inverter circuits. The constraints for the design were discussed and implemented to achieve a low profile power module with increased structural stability while maintaining the enhanced thermal benefit. The design was implemented by designing a three step processing workflow using sintered silver paste and pressure assisted sintering. The completed power

module was further prepared for integration with the addition of electrical connections compatible with test fixtures and encapsulation. Encapsulation was evaluated and chosen to compliment the high temperature application target.

7.2. Electrical Evaluation of Prototype Modules

Using the constructed prototype modules, electrical test setups were custom fabricated for evaluating the appropriate prototype static and dynamic electrical quantities. These experimental setups and measurements were V-I characteristics, DC power stage testing, double pulse dynamic switching performance, and full inverter evaluation at >55KW. Testing revealed excellent switching characteristics with lowered package inductance, robust die attachment when exposed to device self-heating of constant DC power and module repeatability for population of multi-module inverters.

7.3. Experimental and Numerical Analysis of the Structure

Experimental analysis of the module thermal characteristics, the stress relieving compliant structure and their contributions to relative cycling lifetime were performed. The module thermal impedance and thermal resistance were significantly lower with the additional cooling surface above the device. These test results were confirmed using FEA models.

Modules were tested for cycling reliability using both active and passive thermal cycles. Active cycling exposed the quarter-bridge module to 10,000 cycles (40°C to 160°C) before thermal impedance indicated interface failure. Both encapsulated and unencapsulated packages were passively cycled from -55°C to 175°C. Unencapsulated packages revealed no change in forward voltages up to 1000 cycles. The cycling thermomechanical stresses were also modeled using finite element analysis.

The stress reductions achieved with the compliant interface were found to reduce die attachment plastic and shear strains which leads to increased cycling lifetime. Additionally, use of the compliant interface expose devices to much lower von Mises and shear stresses compared to other proposed double-side structures.

Original Contributions

This thesis offers the following original contributions:

1. Proposed a compliant interface fabricated from a plurality of silver tubes which allows for successful implementation of the proposed three-dimensional double-side planar power modules by reduction of thermomechanical CTE stresses during fabrication and cycling regimes.
2. Proposed and fabricated a double-side planar power electronics package based on large area silicon power devices for reduction of weight, volume and electrical parasitics. The module design enhances heat dissipation allowing for higher temperature operation and offering more flexible cooling configurations.

3. Developed a solder free fabrication process for module construction using pressure assisted sintered silver LTJT for large area devices and integrating the proposed compliance structure.

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Appendix A

A parametric study investigating the effect of the tubing wall thickness on the active cycling von Mises stress was performed by Dr. Joe Mei at the Center for High Temperature Electronic Packaging at the School of Materials Science and Engineering at Tianjin University in China. The FEA model dimensions are the same as the ones used for FEA models performed at Virginia Tech. The tubes, however, are spaced 3 mm apart for this model rather than place them in direct contact as previously modeled. A summary of the dimensions are shown in Figure 145. The model was performed for wall thicknesses of 0.1, 0.2 and 0.4 mm.

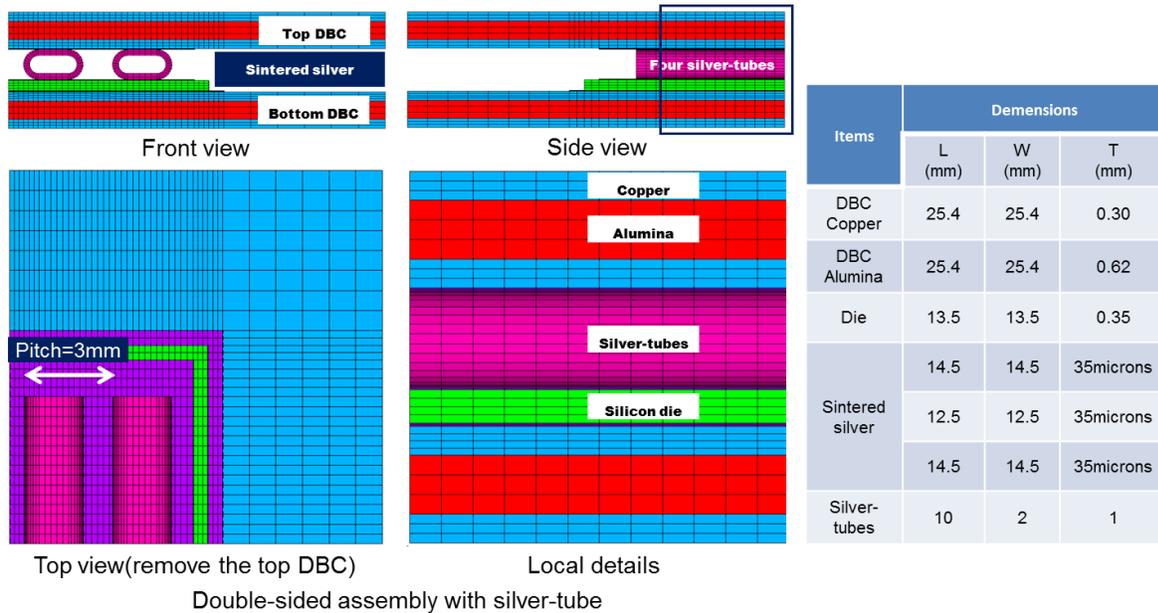


Figure 145: Summary dimensions for FEA model generated by CHTEP at Tianjin University.

The model was performed for active cycling the device junction in cycles from 50°C to 150°C. This cycling was accomplished with an alternating symmetric 5 second square power pulse.

Four cycles were performed to insure stresses reach a steady state. However, the model was performed for two different sets of boundary conditions. One condition was the commonly accepted power cycling condition which adjusts the convection conditions to maintain the same device junction temperature profile regardless of added thermal mass e.g. extra tubing wall thickness. The other condition was to leave convection boundary conditions unchanged during the test for each parameter which would result in a lower junction temperature as silver was added for thicker tubing walls. The outcomes for the two conditions were very different. For a true power cycling model, the von Mises stress on all the package components increased as the wall thickness increased. This graph is shown in Section 5.2.2. For the other condition, the von Mises stress decreased on the die and die attach. The trend is seen in Figure 146.

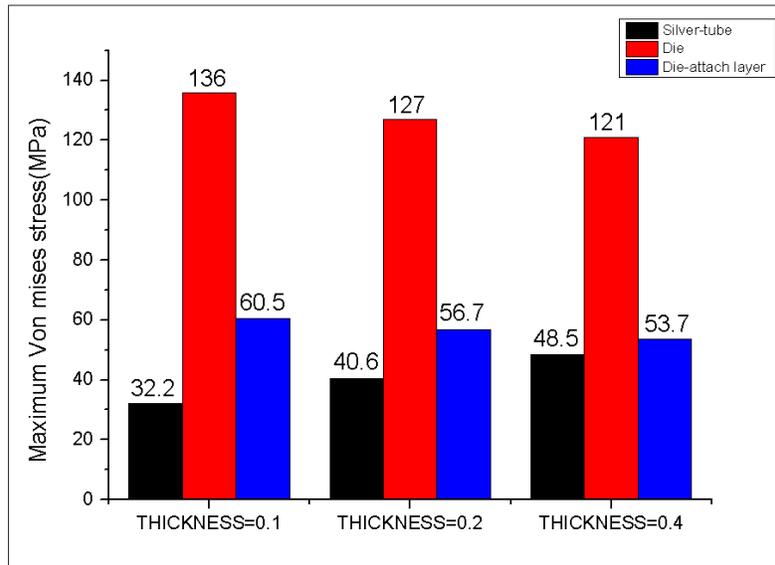


Figure 146: The von Mises stress in the fourth cycle of the active cycling regime which does not adjust convection conditions to account for added thermal mass.

This trend is most likely due to the decreased junction temperature which is a result of the added thermal mass. The device junction temperatures were tabulated for each measured parameter to

show how the thermal mass lowers the device temperature. The actual junction temperatures for each parameter tested are shown in Figure 147.

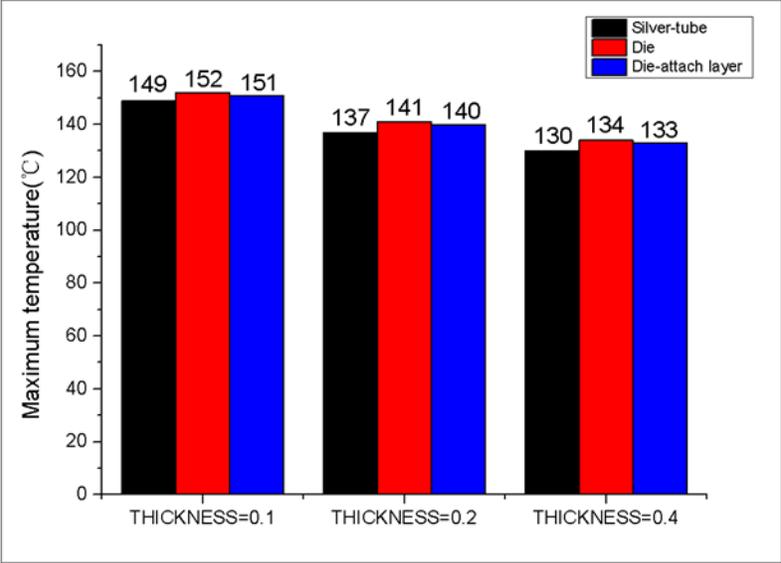


Figure 147: The actual device temperature in the fourth cycle of the active cycling regime when convection conditions are not altered to account for added thermal mass.