RAYTHEON PB 440 DISK INTERFACE DESIGN

by

Paris Herschel Wiley

Thesis submitted to the Graduate Faculty of the

Virginia Polytechnic Institute

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

APPROVED:

Dr. W. Scott Bennett

Dr. A. Wayne Bennett

Dr. H. H. Hull

Date

March, 1970

Blacksburg, Virginia

KLB 7-25-77

ACKNOWLEDGMENTS

The author wishes to express gratitude to

, for his help and encouragement in writing this thesis.

TABLE OF CONTENTS

LIST OF FIGURES

SECTION I

INTRODUCTION

The Raytheon PB 440 computer referred to in this thesis has a total core storage capacity of only 4608 words. Since additional storage capacity is required to meet the needs of the general user, it was decided to add a disk storage unit to the PB 440. A disk offers high speed and high capacity at a fraction of the cost of an equivalent amount of core. The problem was that the PB 440 was not designed to be used with a disk; therefore, an original design of disk/computer interfacing electronics was required.

A major problem solved with this design was a timing difficulty encountered in coupling the high speed disk to the medium speed computer. Normally, data is transmitted from the disk much faster than it can be received by the computer. This difficulty was overcome by modifying the PB 440 input/output system.

Sections 2 and 3 deal with relevant details of the PB 440 computer and the disk storage unit, respectively. These sections provide sufficient background to clarify decisions made later. Section 4 is a description of the interfacing electronics and is intended to serve as a reference for its maintenance.

SECTION 2

COMPUTER CHARACTERISTICS AFFECTING INTERFACING

2.1. Scope of Section

This Section provides pertinent details concerning the operation of the PB 440 arithmetic and control (A & C) unit and the input/output system. The logic level converters are described, and a discussion is made of the signals necessary to accomplish a data transfer between the computer and disk.

2.2. Arithmetic and Memory Design

The arithmetic circuits of the PB 440 are constructed to handle 24 bit words in the parallel mode. The working registers are also 24 bits in length. The computer performs standard binary computations, as well as, partial word add, complement, increment, decrement, and shift operations.

The PB 440 incorporates a dual memory. The smaller (512 word) memory is of biaxial design and employs non-destructive readout. The main memory (4096 words) is of conventional design employing destructive readout.

2.3. Operating Times

The master clock generator of the PB 440 is a crystal-controlled oscillator with a frequency of one megahertz.

Most instructions can be executed within the one microsecond clock interval. Memory access time differs for high speed (biaxial) and main memory. The high speed memory can be read during every clock pulse interval. The main memory has an access time of two microseconds, but, due to rewrite time, can be read only every three microseconds. However, the last microsecond of this period, called shadow time, can be used for computation or manipulation while rewrite takes place. High speed memory write time is eight microseconds, and main memory write time is two microseconds plus one microsecond shadow time.

The time required to execute a data transfer depends on the type of device addressed and whether or not the device is ready to respond. The data transfer execution period will last until the first clock pulse following the return of an "echo" signal from the device.

2.4. Input/Output Buses

Transfer of data into and out of the computer is accomplished via two data buses: the Q bus, a twenty bit parallel data output bus, and the R bus, an eight bit parallel data input bus. However, in order to interface the disk in the most efficient manner, it is necessary that the input and output buses each have the full twenty-four bit capacity. Otherwise, it would be necessary to transmit each word eight bits at a time and construct the

full word in a working register. However, the time interval between words from the disk is not sufficient to accomplish this construction.

To eliminate the need for input/output buses, the disk interfacing electronics was placed in the arithmetic and control (A & C) unit. Connections can be made directly to appropriate points. The output (Q bus) signals can be taken directly from the inputs to the Q bus drivers. All twenty-four of these are present in the A & C unit (although only twenty are connected to receivers in the I/O chassis).

The input (R bus) signal connection points must be made differently. Although all twenty-four R bus receivers are in the A & C unit, they have double-ended, or differential, inputs. However, a suitable point for the insertion of the R bus signal is shown on the schematic diagram of Fig. 2.4-1. When this point is grounded (a logical "0"), the output becomes -8 volts (a logical "1"); otherwise, the output is a logical "0."

The integrated circuits incorporated in this design have a logical "0" level of zero volts and a logical "1" level of +4.0 volts. Since these levels are not compatible with those of the PB 440, it was necessary to design logic level converters.

The schematics for the logic level converters are shown in Fig. 2.4-2. Part "a" shows the computer output (Q bus) converter which produces an output of +4 volts

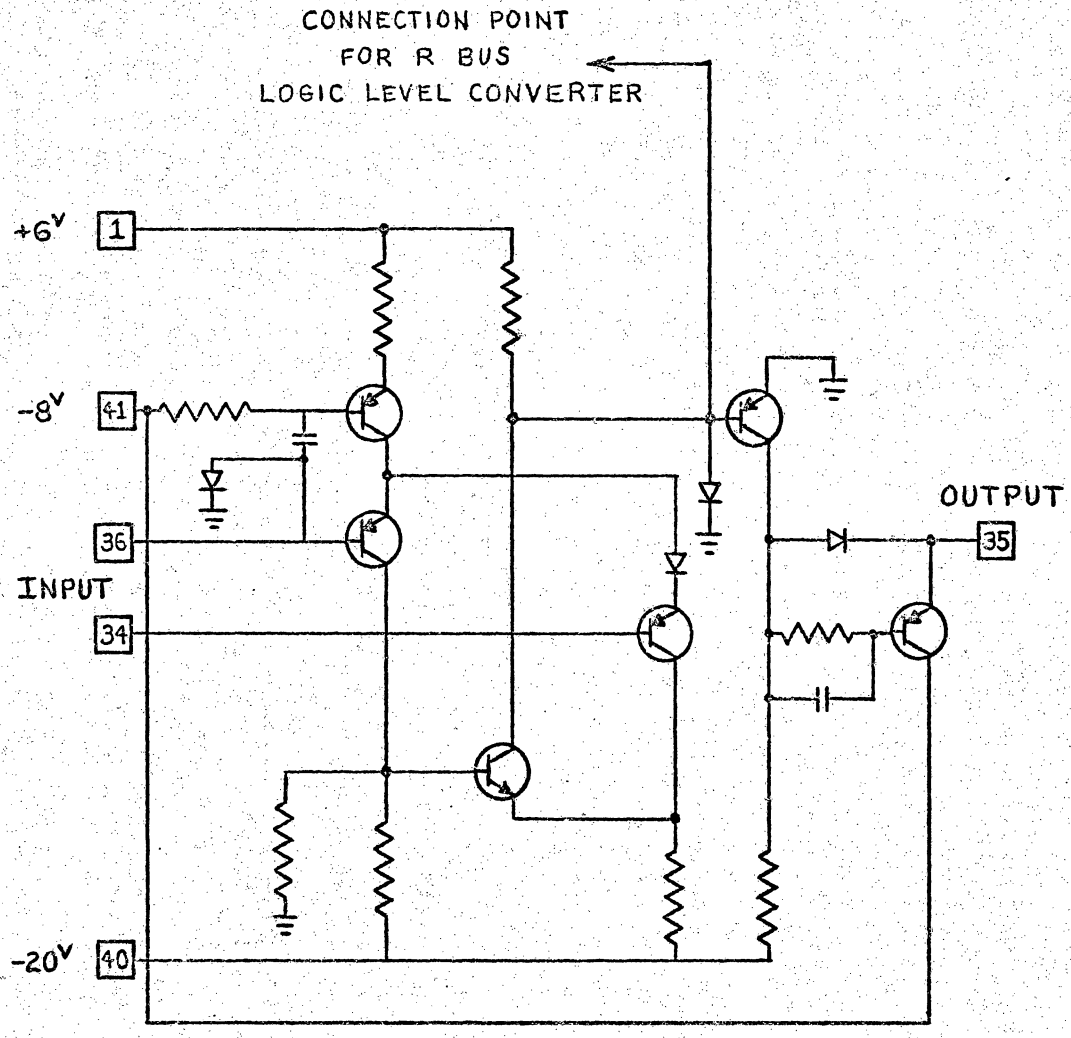
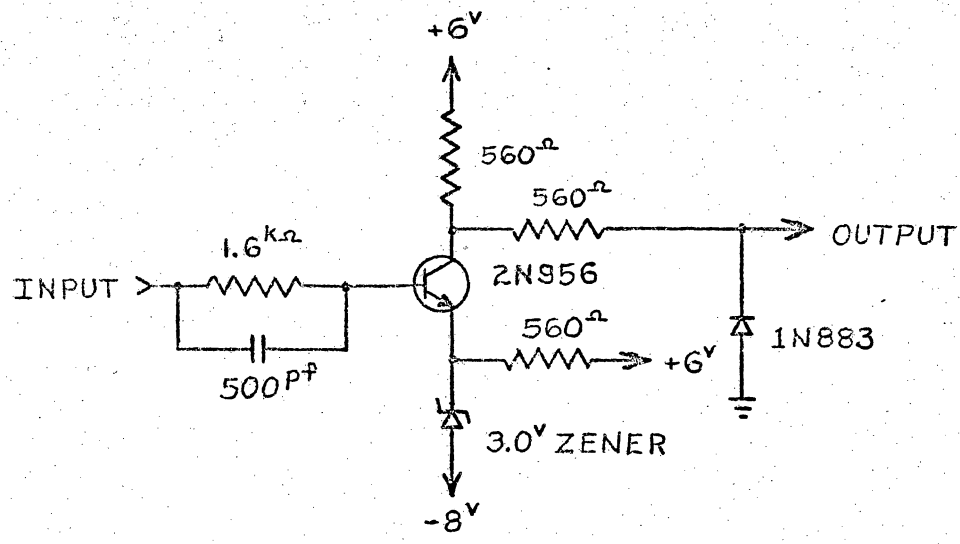
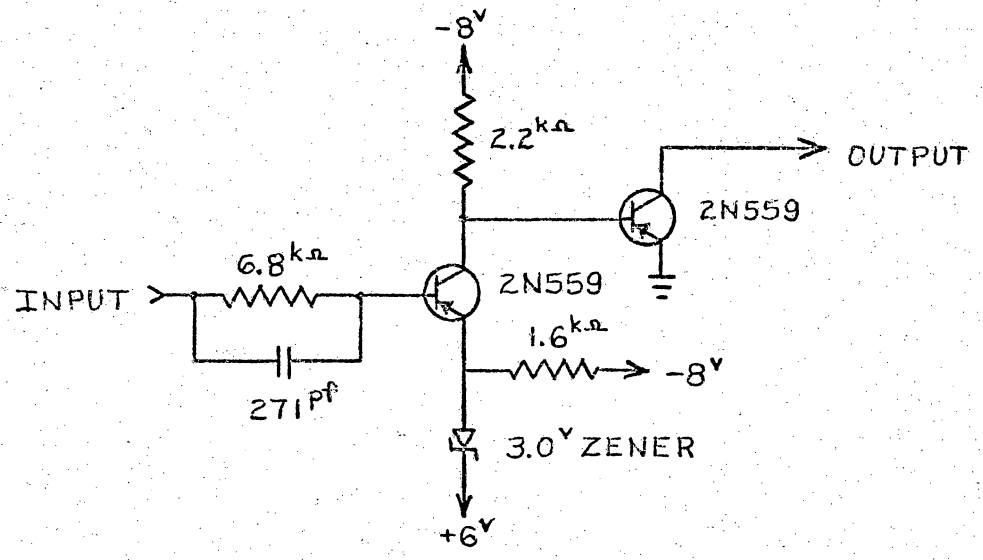


FIG. 2.4-1. R BUS INPUT RECEIVER SCHEMATIC



A. Q BUS CONVERTER



B. R BUS CONVERTER

FIG. 2.4-2. LOGIC LEVEL CONVERTER SCHEMATICS

(into a 1000 ohm load) when the input is more negative than -5 volts. Part "b" shows the computer input (R bus) converter which produces an output of zero volts when the input is more positive than +3 volts. This logical inversion is necessary since the signal is also inverted by the input receiver of Fig. 2.4-1.

2.5. Input/Output System Operation

Four channels are provided for communication between the computer and the various peripheral devices. Each channel contains an "interrupt" line and an "enabling" line. The interrupt line allows the device controller assigned to that channel to signal the computer when it is ready for a data transfer. The enabling line is used by the computer to enable the controller assigned to that channel to accept a data transfer command. Data transfer commands are sent to all controllers but only the enabled controller will act on the command.

The four communication channels should not be confused with data transfer buses. One output (Q) bus is shared by all output devices, and one input (R) bus is shared by all input devices. The communication channels allow several devices to be connected to the input and output buses at the same time.

2.6. Input/Output Device Selection

The disk is always selected on channel three. This is not a handicap because the computer cannot operate any device simultaneously with the disk. The selection of a particular device is accomplished by using a select code word which specifies the device, controller number, channel assignment, and whether the device is to be selected for input or output. The normal format for this select word is shown in Fig. 2.6-1(a). The select word format modified for use with the disk is shown in Fig. 2.6-1(b). As can be seen, a major modification was to incorporate a track address into the select word. The disk is the only data transferring device which requires a starting address.

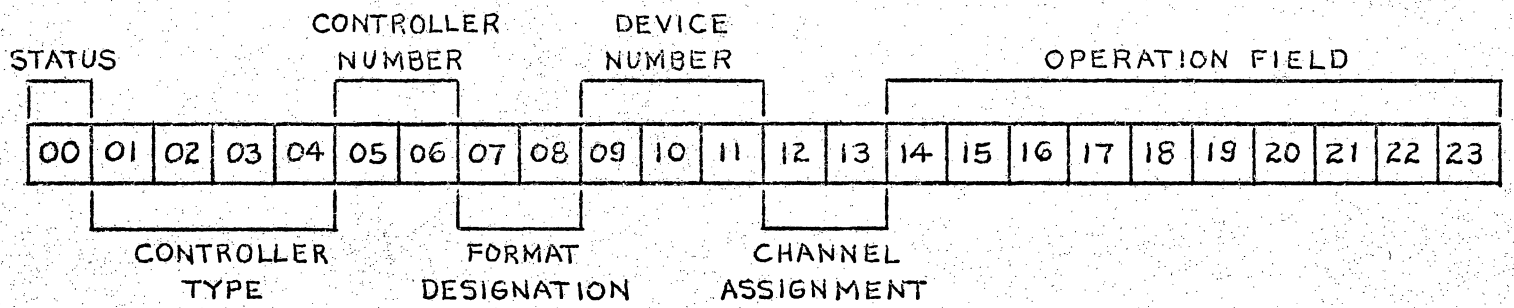
2.7. Data Transfer Operation

The signal lines (excluding buses) necessary for the execution of a data transfer are NABL3, DXFOUT, DXFN, DSC, QSEL, EKO, and SPL.

NABL3 is the enabling signal for devices selected on channel three. This signal enables any device on channel three to respond to a data transfer command.

DXFOUT is generated whenever the data transfer command requires data to be transferred from the computer. This signal, in conjunction with NABL3, gates the data on the Q bus into the disk controller.

A. I/O DEVICE SELECT WORD FORMAT



B. DISK SELECT WORD FORMAT

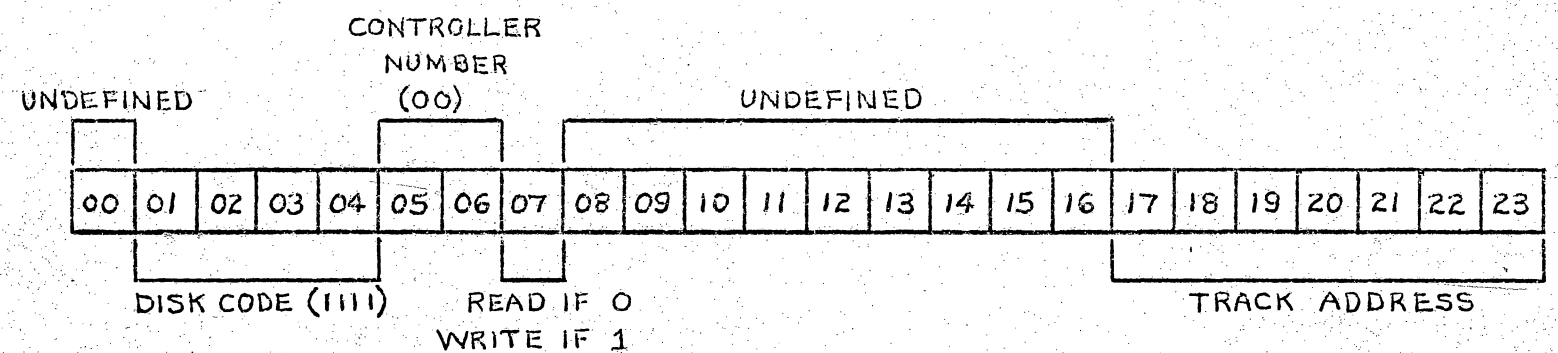


FIG. 2.6-1. SELECT WORD FORMAT

DXFN is generated whenever data is to be transferred into the computer. This signal, in conjunction with NABL3, gates the data from the disk controller onto the R bus.

DSC, in conjunction with NABL3, is used to disconnect devices selected on channel three.

QSEL is the signal which identifies the word on the Q bus as a select code word.

EKO is the signal returned from the disk controller indicating that the operation order by the computer has been completed. Once the data transfer command has been executed, the computer will delay until the EKO signal is received. This is used to keep the computer synchronized with the disk during the scanning of a track on the disk.

SPL is the signal which, when false during a data transfer, causes the next instruction to be skipped. When the disk is selected, SPL is held "true" which allows an instruction to be executed in the time that would ordinarily be wasted in skipping to the next instruction. This shortens the execution time of any program written for the disk.

The block diagram of Fig. 2.7-1 shows the signals involved in the transfer of data to and from the disk. The logic level converters shown are those described in Section 2.4. One converter is required for each of the above described signals and forty-eight are required to connect the Q and R buses.

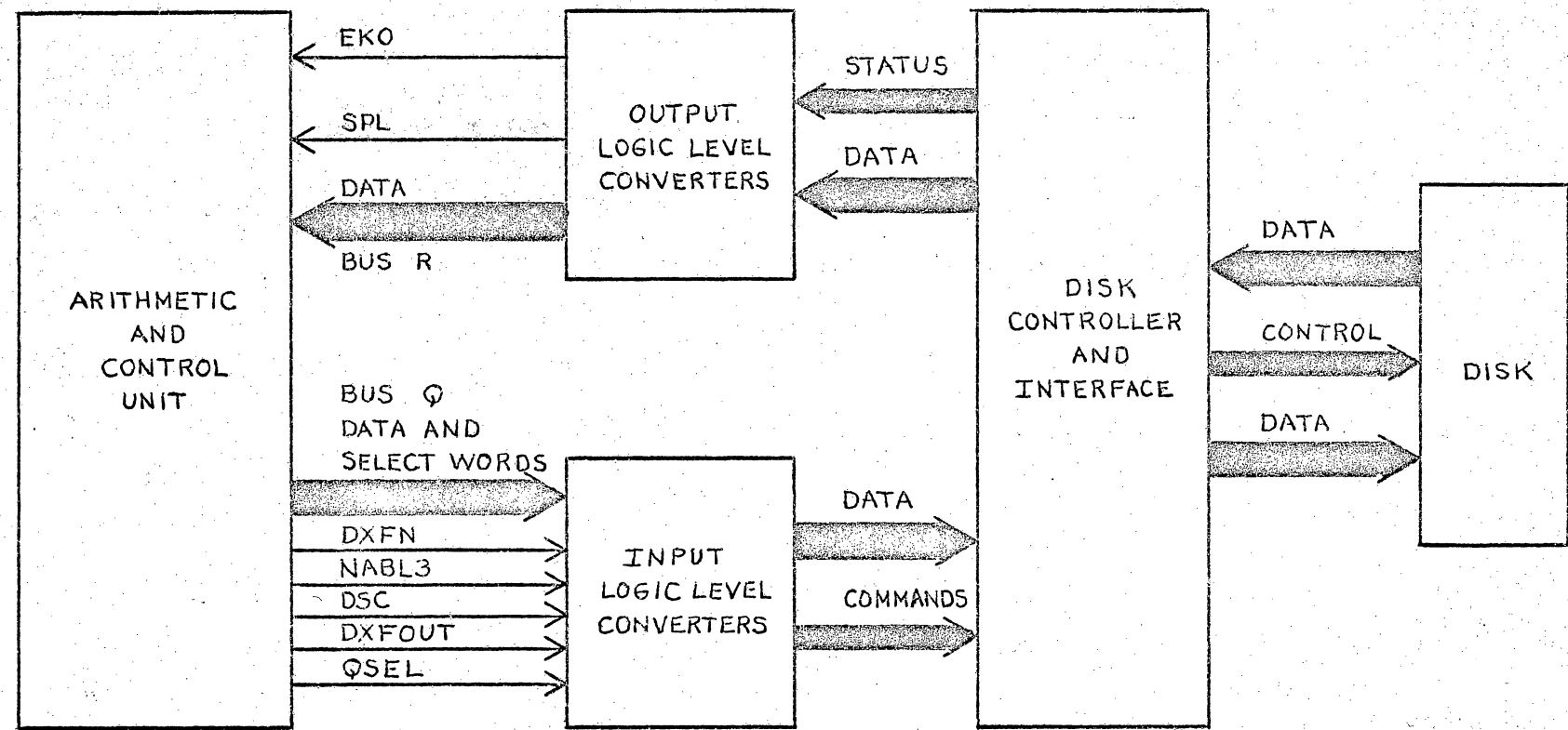


FIG. 2.7-1. I/O SYSTEM BLOCK DIAGRAM

SECTION 3

THE ROTATING DISK MEMORY UNIT

3.1. Scope of Section

This Section describes pertinent characteristics of the disk and associated electronics, followed by a discussion of the requirements placed on the interfacing electronics.

3.2. General Description of the Disk

The disk storage unit is a fast, non-destructive, random access system which includes address decoding, track selection, data encoding, recording, recovery, and data decoding electronics. The basic storage element is a 13 inch diameter aluminum alloy disk. The magnetic surface is nickel-cobalt overcoated with a hard protective film.

The maximum capacity without format is 36,840 bits per track. At 3450 revolutions per minute, the transfer rate is 2.1 megahertz. The bits of a given data word are recorded in serial form on the same track. Each track is divided into 36,840 equal parts called bit cells. A logical "0" is recorded as one flux reversal per bit cell while a "1" is recorded as a double flux reversal per bit cell. The boundaries of the bit cells are indicated by a clock track on the disk.

3.3. Disk Electronics

The disk electronics facilitate interfacing. Included are all necessary read/write amplifiers, a head select matrix, data encode/decode electronics, and address decode electronics. A block diagram of the electronics, which consist largely of transistor-to-transistor (TTL) integrated circuits, is shown in Fig. 3.3-1.

3.4. Interface Requirements

The logic levels of the TTL integrated circuits used in the disk electronics are compatible with those of the diode-to-transistor (DTL) integrated circuits used in the interface electronics. Hence, direct connections can be made.

Addressing a particular track on the disk is accomplished by placing a seven bit binary word on the address input lines. This address must be present during the entire read or write operation. The disk is normally in the read mode. A logical zero applied to the write enable line is required to change to the write mode. Transitions in the write enable signal must occur at least 20 microseconds before the beginning of a read or write operation. Thus, the disk cannot be used to store single words efficiently; an entire track must be transferred with no change in mode.

As the recording head passes over the center of a bit cell in the write mode, a "1" or a "0" will be recorded

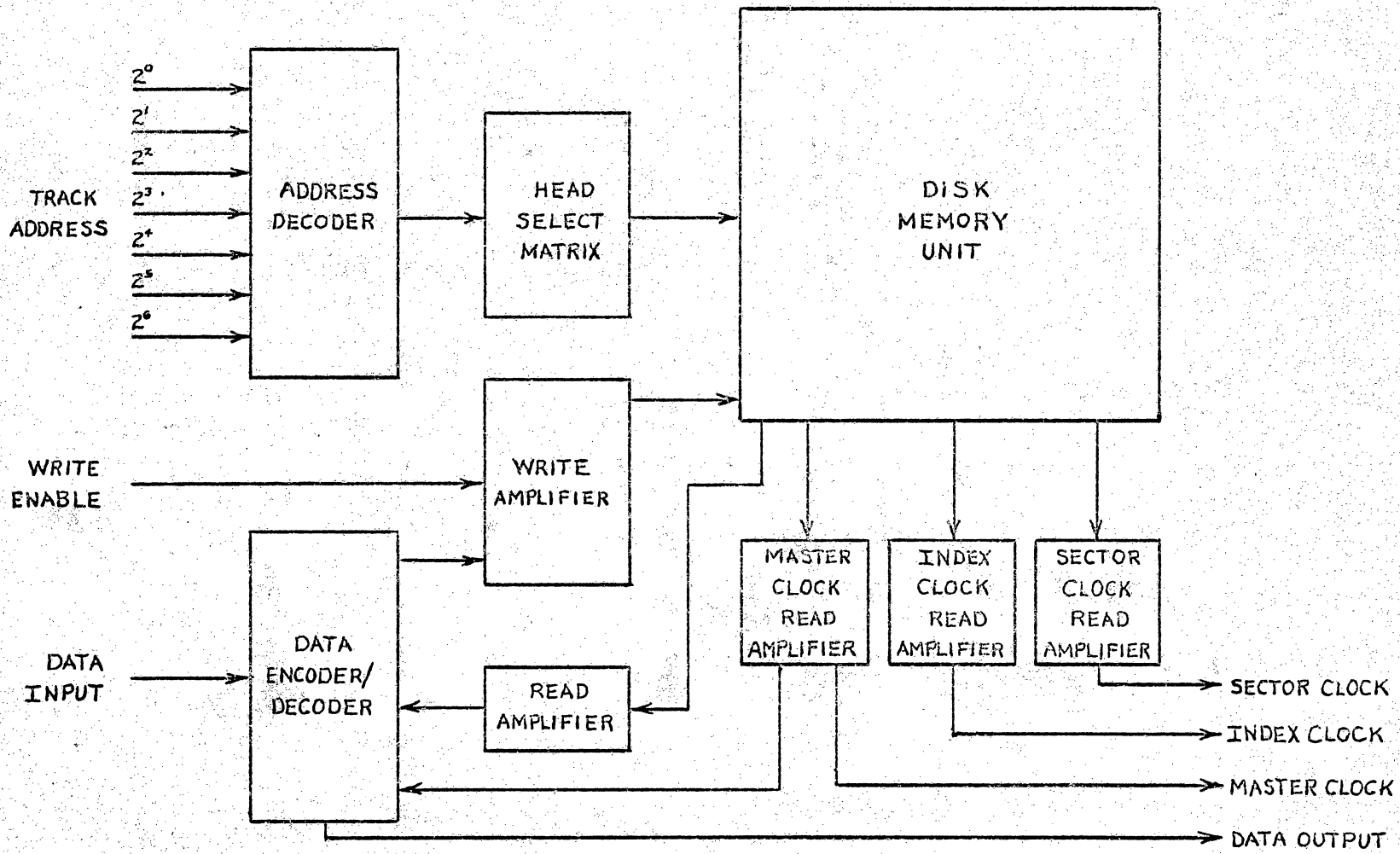


FIG. 3.3-1. DISK ELECTRONICS BLOCK DIAGRAM

according to the state of the data input line at that time. Transitions in the data input pattern must occur within 150 nanoseconds after the beginning of a bit cell to insure that the transition will be recorded in that bit cell.

As seen from Fig. 3.3-1, there are three clock tracks recorded on the disk to facilitate data storage and recovery. The index clock track has one pulse recorded which marks the beginning of the other tracks. The master clock track has pulses recorded that mark the beginning and center of each bit cell, and pulses available at one-half the master clock frequency mark bit cell boundaries. The sector clock track is recorded to mark the beginning of each data word; one pulse occurring every 34th bit cell. Fig. 3.4-1 is a timing diagram which illustrates the inter-relationship of the signals discussed above.

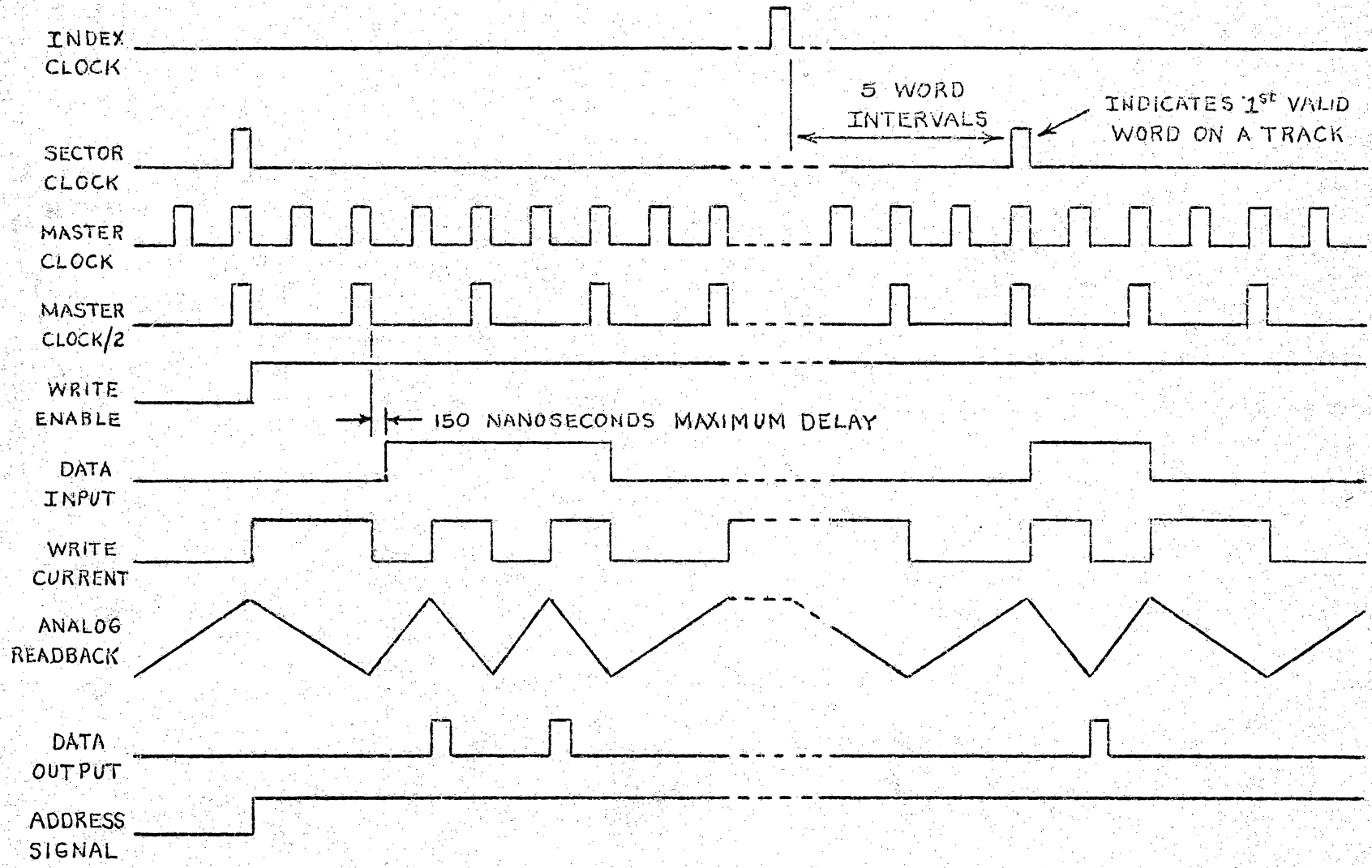


FIG. 3.4-1. DISK TIMING DIAGRAM

SECTION 4

DISK INTERFACING ELECTRONICS

4.1. Scope of Section

This Section contains a discussion of the disk interfacing electronics: the logical circuits used and the theory of their operation. The discussion is divided into four sections; the disk select logic, the disk function-control logic, the data formatting logic, and the data handling logic.

4.2. Specifications for Operation

The major concern in choosing a data format (word spacing) and speed (1725 or 3450 rpm) for the disk was to allow the computer sufficient time to process each word before the end of the next word interval. Due to physical limitations of the disk, once a data exchange is begun, the contents of an entire data track must be exchanged. Since 1024 words are stored on each track, data is exchanged in blocks of 1024 words. After a data exchange is completed, the track involved is read and compared with the data in core memory to detect errors. Appendix II contains the micro-programs which accomplish the data transfers and checks. The check program requires 12 microseconds for execution; therefore, the minimum word interval is 12 microseconds.

The data format (word spacing) on the disk is 34 bit cells per word. The manufacturer recommends at least 3-6 blank bit cells at the beginning and end of each word. The system so designed is much more reliable than if the words were placed end to end. A total of 10 blank bit cells (three at the beginning and seven at the end) was chosen which allows a total of 1024 words per track, and produces a word interval of 16 microseconds with a disk speed of 3450 rpm. To allow time for the read/write amplifiers to stabilize, valid data begins with the 5th word space on a track. The following paragraphs describe the operation of the disk interfacing electronics during a data exchange. Fig. 4.2-1 will aid in understanding this description.

First, the disk is selected for input or output. (This follows the execution of a "SEL" command using the select command word described in Section 2.6.) The proper device and controller codes (in the select word) accompanied by "QSEL" enables the disk controller. The 7th bit of the select word sets up the disk for either read or write, and the track address (bits 17-23) are stored in the address register.

The read or write cycle begins with the next index clock pulse after selection. In the interval before a valid word space is reached, a data transfer command is executed and the computer is waiting for a response. When the disk controller is ready for a data transfer,

it generates an echo signal (EKO) which causes the data to be transferred and terminates the command. The computer must do all necessary data processing and execute the next data transfer command before the disk controller is ready. As long as the computer executes data transfer commands at intervals of less than the disk word interval (16 microseconds) the disk and computer will remain synchronized.

The valid data on a disk track does not begin until the 5th word space (word spaces are marked by the sector clock). Also the first 3 bits and the last 7 bits in each word are irrelevant. The counters shown in Fig. 4.2-1 are used to determine valid data intervals. The diagram of Fig. 4.2-1 is somewhat simplified, thus all signals are not shown.

4.3. Disk Select Logic

4.3.1. Scope

This Section contains an analysis of the disk select logic with input and output signals defined. Included are logic diagrams and a discussion of the theory of operation.

4.3.2. Function

There are two basic functions of the disk select logic: the first is to allow the disk to be selected for input or output in the same manner which the PB 440 selects other I/O devices;

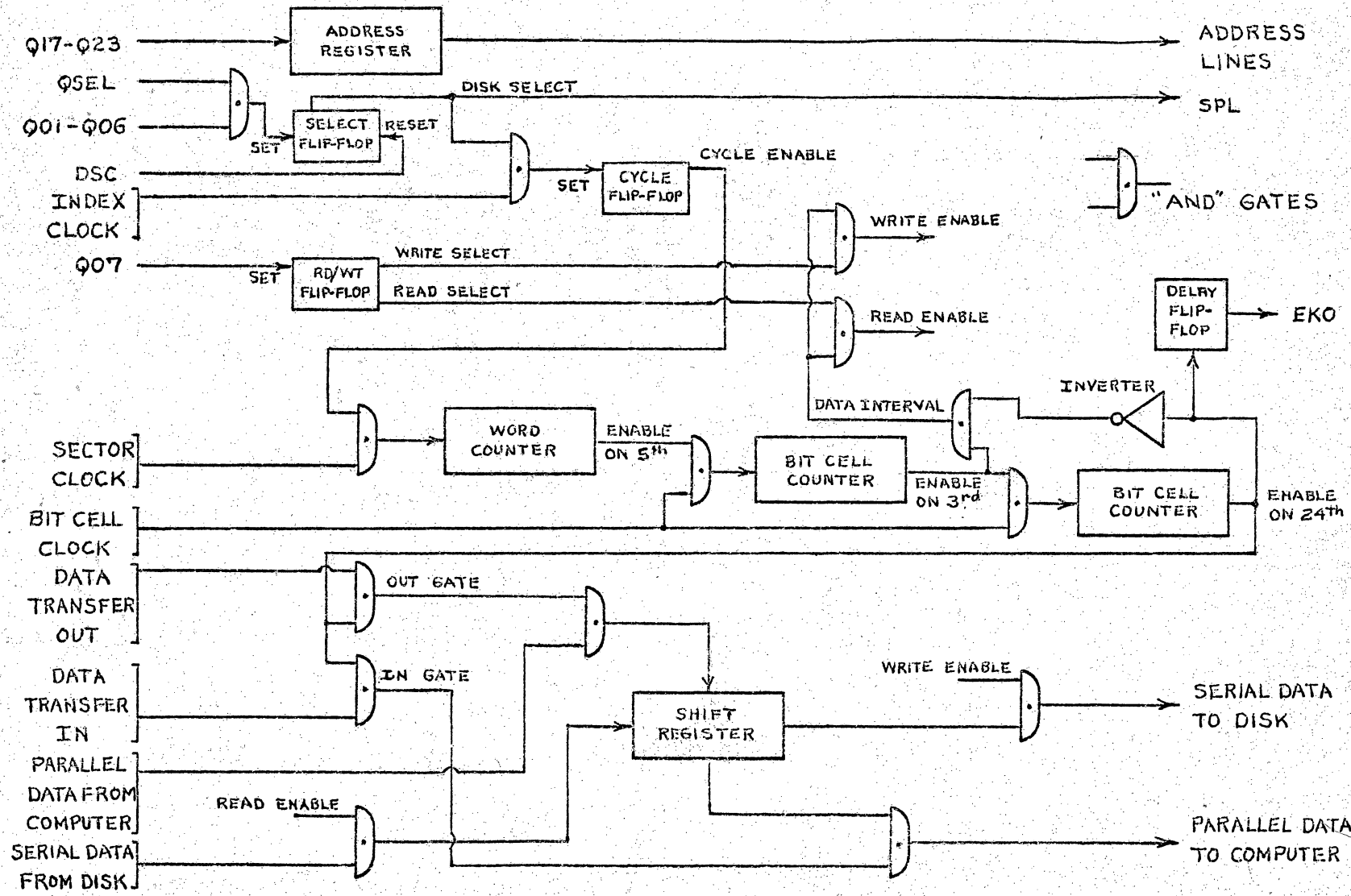


FIG. 4.2-1. INTERFACING ELECTRONICS BLOCK DIAGRAM

the second is to retain necessary information contained in the select code word so that it will be available for future use by the disk controller.

4.3.3. Input and Output Signals

The following signals are necessary to the proper operation of the disk select logic and have not yet been defined. (See Appendix I for a complete signal list.)

(1) TAOUTn is the seven bit track address signal which is applied to the address line of the disk electronics. This signal must be present during an entire read or write cycle.

(2) RDSEL is the signal indicating that the disk has been selected for input.

(3) WTSEL is the signal indicating that the disk has been selected for output.

(4) SEKO is the echo signal which indicates that the select command executed by the computer has been successful in selecting the disk. This signal is used by the computer to terminate the select command.

(5) DSEL exists only during the execution of a select command and indicates that the proper select code word is present for the selection of the disk.

(6) DFSEL is the output of the select flip-flop and indicates that the disk has been selected.

(7) Q17-Q23 are the last seven bits of the Q bus from which the track address is taken during the select operation.

(8) Q11-Q14 are Q bus inputs which contain the device code (1111 for the disk) during the select operation.

(9) Q15-Q16 are Q bus inputs which contain the controller code (00 in this case) during the select operation.

(10) Q07, during the select operation, indicates whether the disk is to be selected for read (0) or write (1).

(11) QSEL is the signal from the computer which identifies the word on the Q bus as a select word.

(12) MRSET is the master reset signal which occurs when the disk is deselected after a read or write cycle.

(13) M2CLK is a signal at one-half the master clock frequency which is used to clock J-K flip-flops or to indicate the boundaries of bit cells.

4.3.4. Theory of Operation

With reference to Fig. 4.3.4-1, assume that a disk select command is executed at any time relative to the M2CLK signal of the disk. The first result is that DSEL will become true indicating that the disk is to be selected. DSEL will

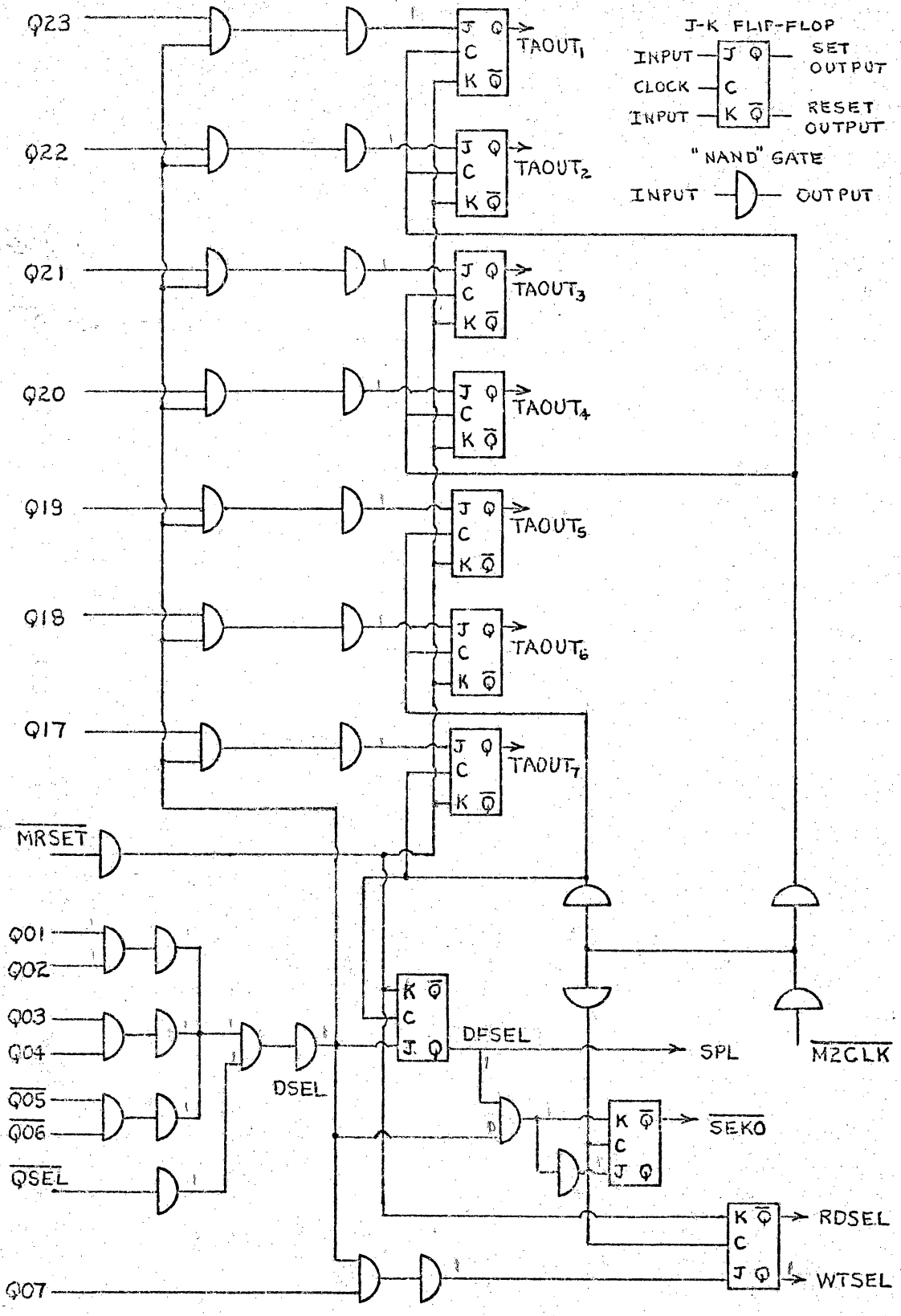


FIG. 4.3.4-1. SELECT LOGIC DIAGRAM

make the J input of the select flip-flop a logical 1, and will also gate the address signal, Q17-Q23, into the J inputs of the respective flip-flops. The result is that, on the next M2CLK pulse, the select flip-flop will be set to a one (DFSEL = 1), and the track address will enter the address storage flip-flops and be applied to the address line of the disk electronics.

At this point, DSEL and DFSEL will both be true since the select command will not have terminated. This combination will make the SEKO flip-flop set on the next M2CLK clock pulse. SEKO will then be true which will terminate the select command. DSEL will be false after the termination of the select command and the J-K inputs to the SEKO flip-flop will be reversed allowing SEKO to go false on the next M2CLK pulse. If, during the select operation, the Q07 bit had been a logical 1, then the WTSEL flip-flop would have been set making WTSEL true and indicating that the disk had been selected for output or write. Otherwise, the WTSEL flip-flop will remain reset and RDSEL will be true as an indication that the disk was selected for input or read. The MRSET signal is generated when the disk is deselected and serves to reset all the flip-flops.

4.4. Disk Function-Control Logic

4.4.1. Scope

This Section contains an analysis of the function-control logic with all input and output signals defined. Included are logic diagrams and a discussion of the theory of operation.

4.4.2. Function

The function-control logic provides signals for control of the various functions of the disk. This Section describes most of the combinational logic which combines signals originating in other parts of the controller.

4.4.3. Input and Output Signals

The following signals are important to the operation of the function-control system. Those signals which have been previously defined are not repeated. (See Appendix I.)

(1) CYSET indicates the start of a data track when the disk has been selected.

(2) CNABL is the signal which becomes true at the beginning of a data track and which enables the rest of the system for a read or write cycle.

(3) RDABL is the signal which gates serial data from the disk into the shift register during a valid data interval.

(4) WTABL is the signal which gates serial data from the shift register onto the disk during a word interval.

(5) SHIFT is the clocking signal which causes data to be shifted to the right in the shift register.

(6) EKO is used by the computer to terminate the select and data transfer commands.

(7) INGAT is the gating signal which gates parallel data from the shift register onto the R bus.

(8) OUTGAT is the gating signal which gates parallel data from the Q bus into the shift register.

(9) WNABL is the signal applied to the disk electronics to enable the write amplifiers.

(10) DEKO is the signal which causes termination of the data transfer command.

(11) IXCLK is the clock signal from the disk indicating the start of a data track.

(12) NABL3 is the signal which causes a data transfer on channel three of the computer I/O system.

(13) DSC is the signal generated by the computer during a deselect command.

(14) RSET is the signal generated by the reset button on the computer control console.

(15) DATAI is the signal indicating that the recording head is passing over a valid data interval.

(16) NWORD indicates the end of a word interval on the disk.

(17) DXFN is a signal originating in the computer when an input data transfer is executed.

(18) DXFOUT is a signal originating in the computer when an output data transfer is executed.

4.4.4. Theory of Operation

The following discussion is keyed to the logic diagram of Fig. 4.4.4-1. Most of the logic in this section is standard combinational logic and requires no explanation. The only exceptions are the circuits which generate CNABL and EKO.

When the disk has been selected, DFSEL is true and the gate is enabled so that the next index clock pulse, IXCLK, will be passed and will set the CNABL flip-flop. CNABL is then true and the rest of the controller will be enabled to execute a cycle.

As can be seen from Fig. 4.4.4-1 the EKO signal is generated whenever either SEKO or DEKO is true. The SEKO signal comes directly from the disk select logic and initiates the end of the select command. The DEKO signal is used to terminate both the data transfer and the deselect commands. It is desired to terminate the data transfer command at the end of a word interval when the disk controller is ready for the data transfer. When NWORD occurs, marking

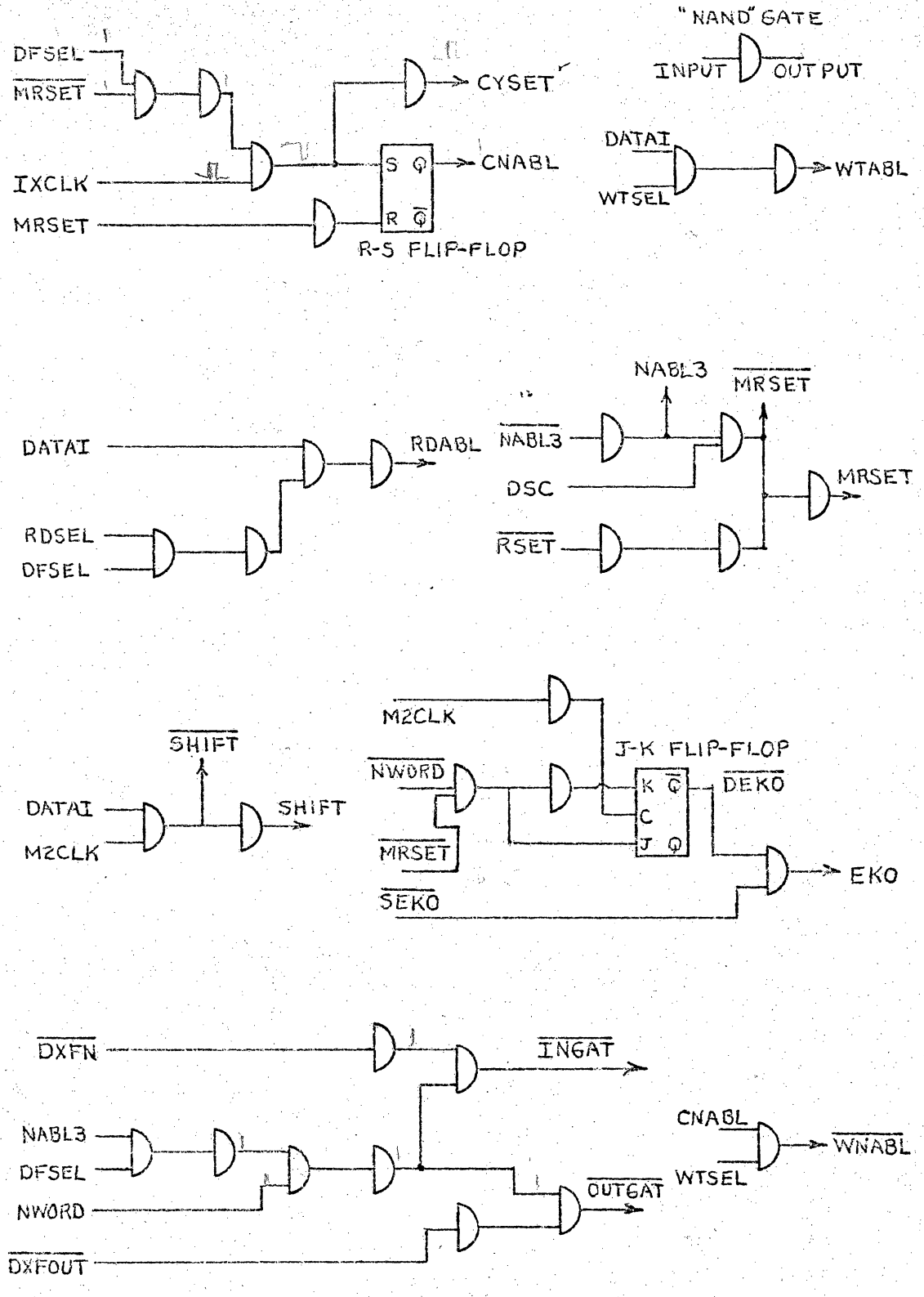


FIG. 4.4.4-1. DISK FUNCTION-CONTROL LOGIC DIAGRAM

the end of a word interval, or when MRSET occurs during a deselect command, the J input of the DEKO flip-flop becomes true and DEKO becomes true on the next M2CLK pulse. DEKO remains true until one M2CLK pulse after the end of NWORD or MRSET when the input to the J-K flip-flop is reversed.

4.5. Data Formatting Logic

4.5.1. Scope

This Section contains an analysis of the data formatting logic section of the disk controller. Input, output, and intermediate signals are defined and a logic diagram and theory of operation are included.

4.5.2. Function

The function of the data formatting logic is to act as a timing unit for the recognition of valid data intervals on the disk. In order to determine a valid data interval, the index clock must be monitored and the sector and master clock pulses must be counted in order to choose the proper 24 bits from the 34 bits in each word interval.

4.5.3. Input and Output Signals

The following paragraphs define the input, output, and intermediate signals which appear

in the data formatting logic and which have not been previously defined. (See Appendix I for a complete signal list.)

(1) WRSET is the word reset signal which resets the data formatting circuitry at the end of each word.

(2) SECT4 is the signal denoting the forth sector clock pulse after the index clock.

(3) BIT2 is the signal denoting the second bit cell in each word interval.

(4) BIT23 is the signal denoting the twenty-third bit cell in each word interval.

4.5.4. Theory of Operation

The following description of operation is keyed to the logic diagram of Fig. 4.5.4-1 and the timing diagram of Fig. 4.5.4-2. Assume first that the disk has been selected as described in Section 4.3. At some subsequent time, the beginning of a track will be reached, and an index clock pulse will occur. If the disk has been selected for write, WTSEL will be true and CYSET will set the first flip-flop in sector clock counter A to the true state. This will advance the count by one and cause the first data transfer to occur before the fifth word interval rather than after it. Also, when the index clock pulse occurs, CNABL becomes true and gates the sector clock pulses into sector

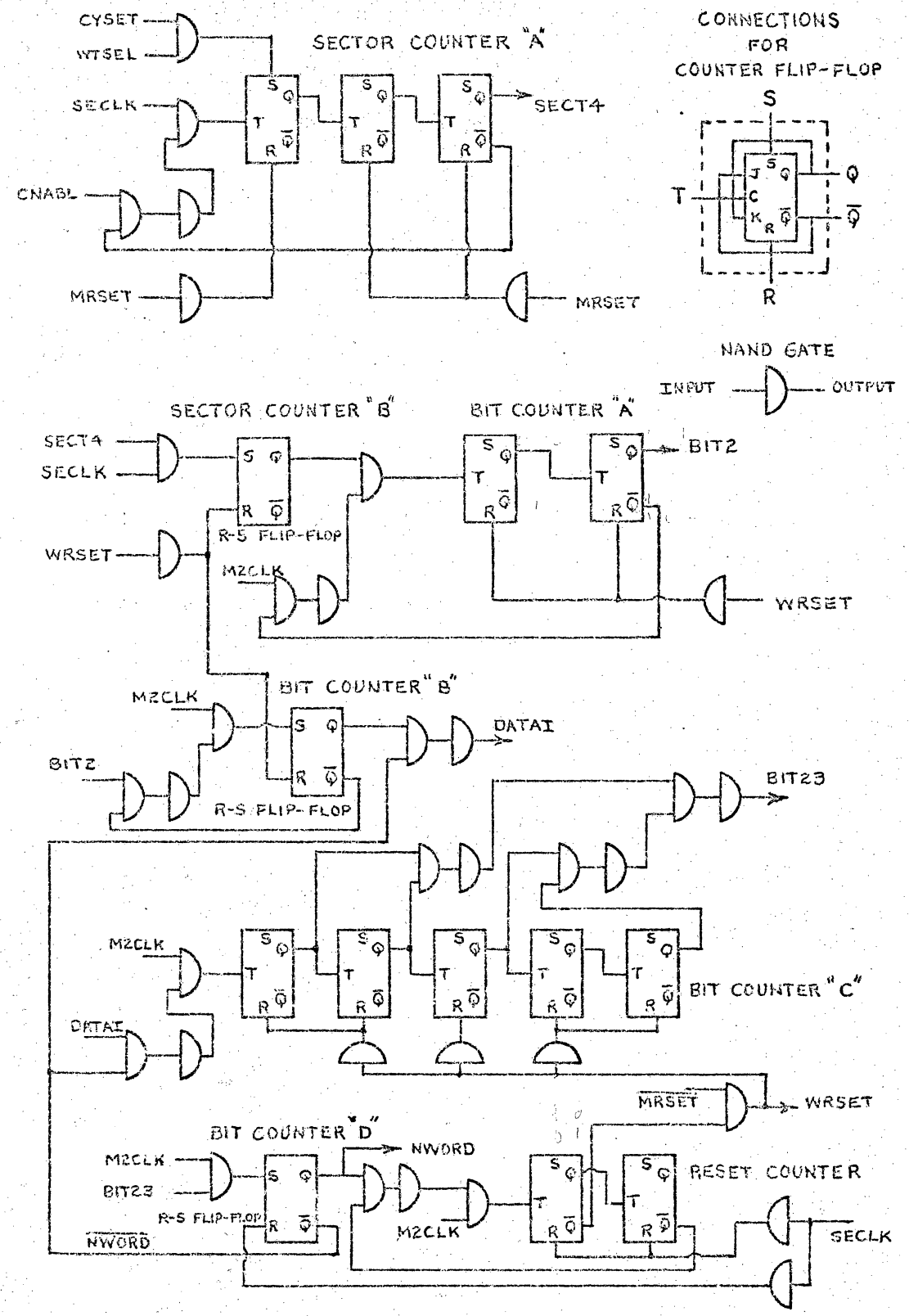


FIG. 4.5.4-1. DATA FORMATTING LOGIC DIAGRAM

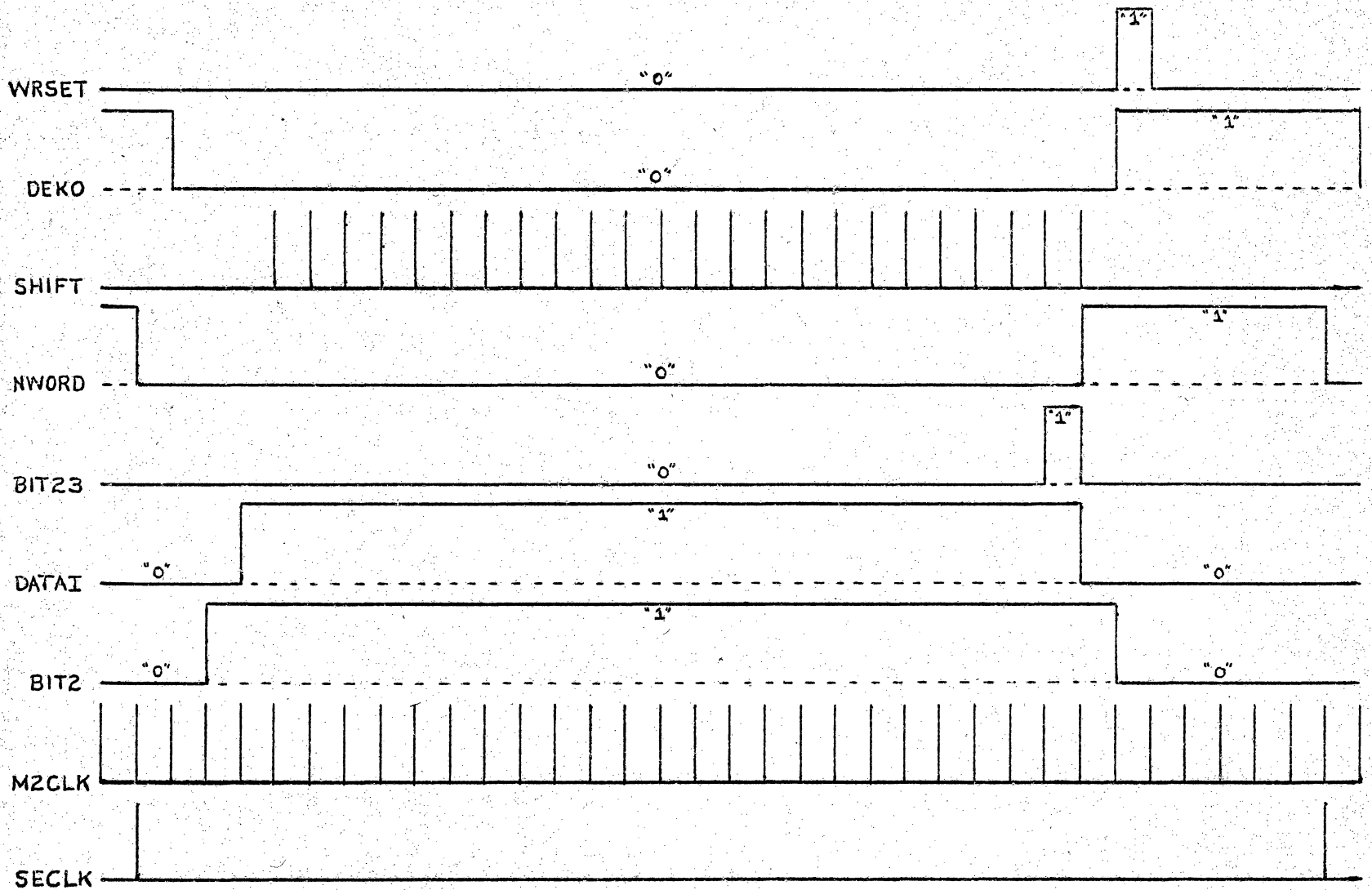


FIG. 4.5.4-2. DATA FORMATTING LOGIC TIMING DIAGRAM

counter A. When the count reaches four, SECT4 becomes true and the counter latches. SECT4 then enables the gate allowing the next sector clock pulse to set sector counter B. This count, as well as those which follow, is done in two stages in order to reduce the propagation delay time normally associated with a non-synchronous counter.

When sector counter B becomes true, the gate is enabled allowing M2CLK pulses into bit counter A. When the count reaches two, bit counter B is enabled and the next M2CLK pulse sets bit counter B and generates DATAI. At this point, DATAI enables bit counter C which then counts 23 M2CLK pulses and generates BIT23. Bit counter D is then set by the next M2CLK pulse generating NWORD.

The next M2CLK pulse after NWORD becomes true will set the first cell of the reset counter and WRSET will become true. On the next M2CLK pulse, the count in the reset counter will increase so that the first cell will be false and the second cell will be true. WRSET will return to the false state and the reset counter will latch until reset by the next SECLK pulse.

4.6. Data Handling Logic

4.6.1. Scope

This Section contains an analysis of the data handling logic and definitions of new signals. Also included are a logic diagram and a description of the theory of operation.

4.6.2. Function

The primary function of the data handling logic is to provide serial to parallel and parallel to serial data conversion through the use of a shift register. Also included in this Section is the gating required to connect the shift register to the serial input and output lines of the disk, and also to the parallel data bus lines of the computer.

4.6.3. Input and Output Signals

The following paragraphs define signals which are necessary to the understanding of the data handling logic and which have not been previously defined. (See Appendix I for a complete signal list.)

(1) SIDAT is the serial data which is gated from the shift register onto the disk.

(2) R00-R23 are bits of the computer input bus.

(3) SODAT is the serial data which is gated off the disk and into the shift register.

(4) Q00-Q23 are bits of the computer output bus.

4.6.4. Theory of Operation

The gating of signals in Fig. 4.6.4-1 is straightforward and requires no further explanation. However, operation of the shift register will be explained.

When the read enable signal, RDABL, is true, SODAT, the serial data from the disk, is gated into the shift register. The timing is such that the data pulse occurs midway between two consecutive M2CLK pulses. If the first data bit is a one, a pulse is present and sets the first flip-flop to the true state; if the first data bit is a zero then no data pulse will occur and the flip-flop will remain reset. When the SHIFT pulse occurs, every flip-flop after the first acquires the state of the one immediately to the left, and the data is shifted one cell to the right. The SHIFT signal is in phase with the M2CLK pulses and so the shift occurs midway between data pulses.

The first flip-flop is also reset by the occurrence of the M2CLK pulse. The additional inverters in series provide delay to insure that the data gets shifted out before the flip-flop is reset.

When the data word has been assembled in the shift register, it is gated onto the R bus by the INGAT signal.

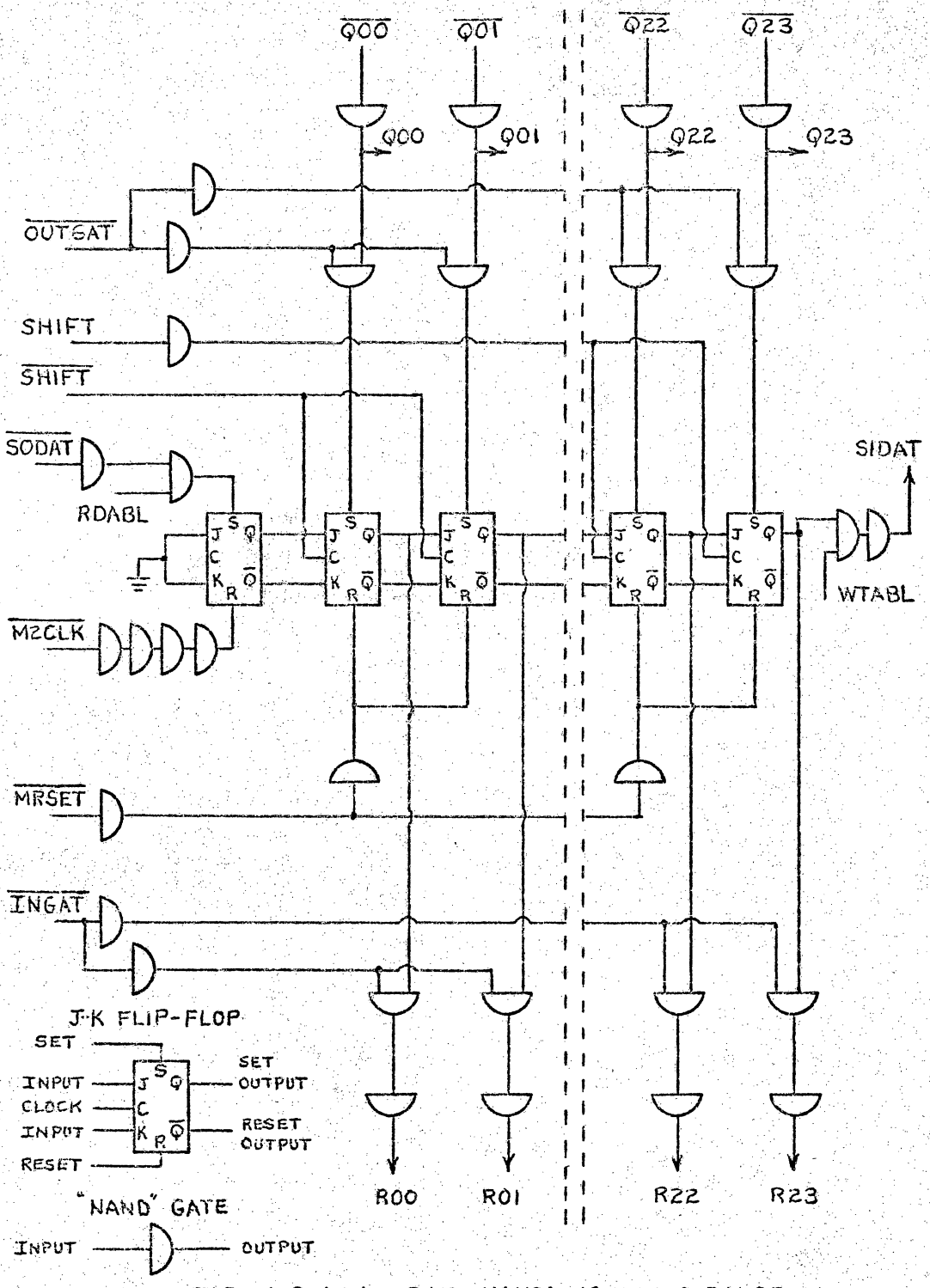


FIG. 4.6.4-1. DATA HANDLING LOGIC DIAGRAM

During a write operation, computer output data is gated into the shift register by the OUTGAT signal. WTABL then becomes true and the data is shifted in serial form onto the disk by the SHIFT signal.

SECTION 5

RESULTS AND CONCLUSIONS

As a result of the study and research pertaining to this project, it was determined that all major objectives could be accomplished. The initial goals were two. The first was to decide whether or not it was feasible to interface a disk to the Packard-Bell 440 computer. The second was to design the interface electronics provided the project was found to be feasible. Both these objectives were accomplished.

It was found that the computer has sufficient speed and capability to effectively use a disk memory. Also a plan of operation was devised that required no changes to the PB 440.

In phase two, the actual logic circuitry was designed using available components. Each logic circuit was built as described, tested at operating speeds, and found to perform as indicated herein.

Once the disk is installed, it will increase the storage capacity of the PB 440 from 4096 words to over 32,000 words.

APPENDIX I

SIGNAL LIST

APPENDIX II

DISK SOFTWARE

The following micro-programs were actually run on the PB 440 to determine the time required for execution. These are the sub-programs which must be a part of any program written for the disk because they are critical to the disk timing. They are based on a data transfer non-skip.

READ PROGRAM

Command	Time, us	Code
10114455	3 + 1	DTR CIL
24513057	2 + 2	STI TNZ
14750000	1 + 1	BTR NOP
16000000	0 + 0	FTR NOP
	10	

WRITE PROGRAM

Command	Time, us	Code
26514455	2 + 1	LDI CIL
10213057	3 + 2	DTR TNZ
14750000	1 + 1	BTR NOP
16000000	0 + 0	FTR NOP
	10	

CHECK PROGRAM

Command	Time, us	Code
10114455	3 + 1	DTR CIL
26325712	2 + 1	LDI XOR
30271600	1 + 1	TNZ FTR
30571474	1 + 2	TNZ BTR
16000000	0 + 0	FTR NOP
	12	

The vita has been removed from the scanned document

RAYTHEON PB 440 DISK INTERFACE DESIGN

Paris H. Wiley

Abstract

This thesis describes interfacing electronics designed to couple the Magnafile 8502 disk storage unit to the Raytheon PB 440 computer. The computer can use the disk for both data storage and recovery. However, data must be exchanged in blocks of 1024 words (one complete track on the disk). The interfacing was designed incorporating diode-to-transistor logic (DTL) integrated circuits.

The PB 440 computer has sufficient speed and capability to effectively use the disk storage unit at an operating speed of 3450 rpm (1725 rpm is also available). The bit transfer rate is approximately 2.1 megahertz. The 32,768 word disk capacity (expandable to 131,072 words) extends the capability of the PB 440 to include commonly used general programming languages.