VHF BIPOLAR TRANSISTOR POWER AMPLIFIERS: MEASUREMENT, MODELING, AND DESIGN

by

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CHAPTER 1

Introduction

Radio frequency power amplifiers are used in communication equipment, navigation equipment, and in instruments. Currently available design techniques for such power amplifiers range from the very simple to the highly complex. The more complicated design techniques have not found general acceptance in the engineering community. The simple techniques are widely used but yield results which are approximate.

Most designers of RF power amplifiers are able to develop circuits having adequate performance. The design is often initiated by one of the simple techniques, and then completed by empirical methods or by relying on previous experience. This approach always leaves the doubt as to whether a better design could be attained. Therefore one can see that a non-empirical design technique is needed which, unlike those above, is simple but accurate.

1.1 Purpose of Project

The goal of the research to be reported in this dissertation is to develop a new approach for the design of VHF power amplifiers using bipolar junction transistors

(BJT). The design technique is to be based upon a transistor model which is simple enough to be useful for design, but which is sufficiently accurate to predict performance at high frequencies.

Work is restricted to circuits using the BJT because this device is overwhelmingly dominant in its use in present-day VHF power amplifier designs. The cost of the BJT is sufficiently less than that of the field effect transistor (FET) to warrant this dominance [Glenn, 1985].

The VHF frequency range is chosen because of the large amount of radio communication conducted there. Even though work is specific to this range of frequencies, most results presented in this report should be directly applicable to HF amplifiers, and applicable to UHF circuits if effects of certain transistor parasitic reactances are included.

Additionally, the emphasis of work is placed on non-saturating amplifiers. The original intention was to investigate only the class B amplifier. The motivation for this was based on the need for a linear RF power amplifier to be used in a VHF single-sideband communication service. In the process of investigation little distinction among the actual operating characteristics of the class A, class AB, and class B amplifiers was found. Therefore the scope of investigation was expanded to include the three classes listed above, and additionally to include the

non-saturating class C amplifier.

1.2 Survey of Current Techniques

The terms "design technique" and "design approach" as they are used in this dissertation refer to the method of determining the required values of source and load impedances to be presented to the power transistor in order to attain some specified performance. Once one has completed the steps of a design technique one must still choose a circuit topology and choose bias network elements. A discussion of these two topics is deferred to Chapter 4 of this report.

There are a number of design techniques presented in the literature, all of which have some useful aspect. On the other hand, all of these techniques possess some drawback.

An example of a simple approach will illustrate a popular technique. A brief discussion of background material is necessary first. A common emitter amplifier with a choke-fed collector supply will have a quiescent collector voltage equal to the supply voltage, V_{CC}. Upon application of a sinusoidal base drive the instantaneous collector voltage will decrease, the minumum voltage attainable will be limited by the saturation voltage of the transistor, V_{sat}. The largest negative peak swing is

therefore given by $V_{CC}-V_{sat}$. The resonant network connected to the amplifier output will guarantee a positive peak voltage swing equal to the negative swing.

The expression for the power output of such an amplifier is

$$P = \frac{(V_{CC} - V_{sat})^2}{2R_L} \tag{1.1}$$

This can be rearranged into the well known equation which gives a design value for the amplifier load resistance,

$$R_L = \frac{(V_{CC} - V_{sat})^2}{2P} \tag{1.2}$$

This result is implicitly based on the assumption that the transistor output can be modeled as an ideal current source. It will be shown in this dissertation that such an assumption is unfounded for many types of RF power transistors.

Actually, this approach is only a partial design technique since it does not address the optimum driving impedance. Additionally, this technique yields relatively poor results [Pitzalis, 1973]. In spite of these drawbacks, this technique is quite prevalent in the literature [Hejhall, 1982; Krauss, 1980; Litty, 1978; Leighton, 1973; RCA, 1971].

Another approach to the design of an RF power amplifier is to use the manufacturer's specified values of input and output impedances [Glenn, 1985; Hejhall, 1982; Krauss, 1980; Lange, 1972; Vincent, 1965]. The manufacturer arrives at values for these input and output impedances by constructing a test amplifier which has wide range input and output tuning networks, then adjusting the amplifier for some desired degree of performance. The transistor is next removed from the circuit and the values of impedances which were presented to the transistor can be measured. The complex conjugates of these quantities are called by the manufacturer "the input and output impedances" of the transistor. The true transistor impedances might be significantly different from these, but the manufacturer's specified "input and output impedances" still provide useful design information.

Drawbacks to this technique are twofold. First, the desired degree of performance is somewhat of an arbitrary judgement. Second, the manufacturer's "input and output impedance" values are strictly valid only for a circuit topology identical to that used by the manufacturer [Glenn, 1985].

A variety of two-port-network measurement and design techniques appear in the literature. Houselander [1970] discusses a large signal Y-parameter technique. Leighton

[1973] and Webb [1973] propose measuring S-parameters under large signal conditions and then to proceed with design using the theory developed for small-signal transistors.

The principal problem with these two-port approaches lies in the technique applied to the measurement of parameters. By their very nature, the two-port parameters must be measured under conditions far removed from typical operating conditions for a transistor. For example, the required termination for typical S-parameter measurements is 50 Ohms and the required Y-parameter termination is a short circuit. Also, in S-parameter measurements, the low impedance of most transistors and the resulting near unity reflection coefficients require extraordinarily high accuracy in the measurement system. Leighton proposes alleviating these problems by measuring S-parameters in a system whose impedance is closer in value to that which is expected for the transistor.

Finally, another major problem arises in the measurement of parameters at the output port of a transistor. These parameters are measured by driving only port two of the device, therefore port one is not excited and the transistor may not even be turned on. A two-signal method of measuring S-parameters has been suggested to eliminate this problem.

In the two-signal method [Takayama, 1976; Mazumder,

1977; Mazumder, 1978] both ports of the transistor are driven simultaneously. Mazumder presents equations which yield the numerical values of the S-parameters from the two-signal data. Mazumder proposes two design procedures using these S-parameters. One [Mazumder, 1978] follows the procedure of Leighton where design is done using the small-signal linear S-parameter equations. The other [Mazumder, 1977] uses a trial-and-error approach to design.

In the two-signal method of measuring S-parameters, the resulting values of the S-parameters are dependent upon the amplitudes and the relative phase of the two driving signals. One disadvantage of this method is a result of the uncertainty as to what are the proper drive levels to use. Presumably this is the reason why Mazumder proposed the trial-and-error approach to design.

One additional disadvantage to the two-signal method is that a relatively complicated and high power measurement setup is needed. It must be said, though, that amplifiers designed from the two signal data appear to perform reasonably closely to the design specification [Mazumder, 1977].

In the two-signal method of measuring S-parameters, the signal which is driven into the output port of the device can be viewed as simulating the reflection from a load. From this point of view the two-signal method is

essentially similar to a method of transistor characterization called "load-pull" [Takayama, 1976]. In the load-pull technique [Belohoubek, 1969; Belohoubek, 1970; Presser, 1972; Pitzalis, 1973; Cusack, 1974; Abe, 1979] one connects a variable load to the output of a transistor and then adjusts the load through a range of values. Data are taken which allow various amplifier performance quantities such as power output, efficiency, and gain to be plotted as functions of the load impedance. Typically these functions are plotted as contours on a load reflection coefficient plane (Smith chart). The design of an amplifier then proceeds by selecting the value of load impedance which corresponds to desired amplifier performance as plotted on the Smith chart.

The load-pull technique provides a complete characterization of the output port of a transistor and therefore must be considered as being an effective way to design the output circuit of an amplifier. On the other hand there are two problems associated with this technique. First, load-pull provides little information about the input characteristics of a device. Second, the load-pull approach is almost universally acknowledged as being a very laborious and tedious procedure. One solution to this last problem is to have an automated setup to take data [Cusack, 1974].

Finally, many researchers have proposed relatively complicated transistor models suitable for computer simulation and computer aided design. These models are often so complicated that it would be difficult to devise a measurement procedure which would adequately characterize the device.

1.3 Overview

One can see that there are a number of design procedures available for radio frequency power amplifiers. Also apparent is that these procedures yield results; but the adequacy of these results is typically in direct proportion to the difficulty of the design technique. One can see that a design procedure is needed which is relatively simple in its application, but which yields results which are accurate. Also, a desirable situation would be to have an approach to design which would give insight into the actual physical processes taking place within the transistor.

To reiterate from Section 1.1, the goal of the project reported herein is to develop a design technique which is simple but accurate. Additionally, the goal is to base this design procedure on a transistor model with as few elements as possible, and more importantly each element should be characterized by a constant numerical value which

is easily measured.

The approach taken in the development of the model (and also the order of presentation of this dissertation) is to begin by taking measured data on a typical VHF power transistor. The transistor used for this initial investigation is a TRW PT8828, a 10 Watt, 175 MHz BJT. Most measurements are made at 175 MHz, but some data from other frequencies are used. Next, basic semiconductor device theory is applied in an effort to explain measured phenomena. The device model to be used in a design process comes about easily once a correspondence between measurement and theory is found. Finally, design approaches are developed around the model.

Details of the measurement technique as well as the results of such measurements are presented in the next chapter. The development of the theoretical model is covered in Chapter 3, and an overall design procedure is discussed in Chapter 4.

CHAPTER 2

Measurements

The important qualities of a radio frequency power amplifier are its input and output impedances, its gain, its power output, and its efficiency. The measurement of the input reflection coefficient, the forward transmission coefficient, the load reflection coefficient, the power in the wave leaving the amplifier, and the DC collector current is sufficient to be able to determine these important qualities. A diagram of the setup used to measure the input reflection coefficient, forward transmission coefficient, load reflection coefficient, and power in the wave leaving the amplifier is shown in Figure 2.1 along with the flowgraph representation of the system.

Directional couplers (Hewlett-Packard 778D) are used to isolate the forward and reverse traveling waves along the 50 Ohm transmission lines which are connected to the transistor under test. A Hewlett-Packard 8405A vector voltmeter is used to measure the voltages present at the directional coupler measurement ports. These measured voltages are proportional to the voltages of the forward and reverse traveling waves. Ratios of measured voltages

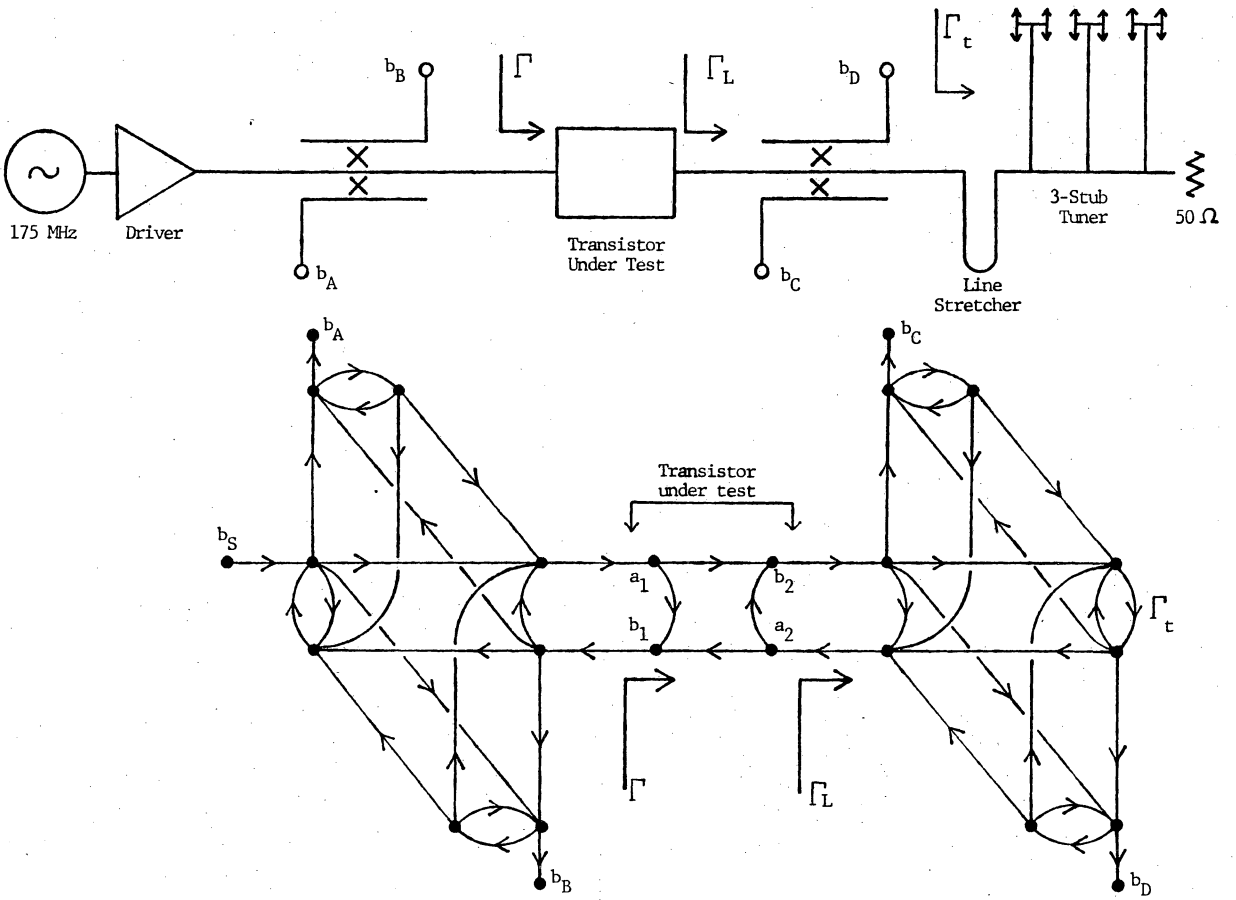

Figure 2.1 RF power amplifier measurement system.

can be used to compute reflection and transmission coefficients, and the absolute values of the measured voltages can be used to compute the powers in traveling waves on transmission lines of known characteristic impedance.

An experiment was performed to check the measurement linearity of the Hewlett-Packard 8405A vector voltmeter. This was done by measuring the reflection coefficient of a fixed termination under a number of different incident power levels identical to those used for transistor measurements. The results of this indicated no discernible variation in the measured quantities, therefore the voltmeter was assumed to be adequately linear.

A three stub tuner terminated in a 50 Ohm power resistor allows adjustment of the load seen by the transistor to almost any desired value. Theoretically, the three stub tuner can be tuned to any impedance having a positive real part, but losses in the materials used to construct the tuner prevent attaining reflection coefficients very close to unity. In situations where near unity reflection coefficients are desired, another load arrangement is used. This arrangement is configured as a short circuit terminating a transmission line of fixed loss.

A section of adjustable length transmission line is

inserted between whatever load is used and the output of the device under test. This allows for easy adjustment of the phase angle of the load without disturbing the magnitude of the load reflection coefficient.

There are no harmonic filters in the measurement system. One might expect that under large signal (i.e. power) conditions the nonlinear characteristic of a bipolar junction transistor would generate high levels of harmonic energy, but there is ample evidence in the literature that this is not the case for RF power transistors of the type used here [Belohoubek, 1971; Lange, 1972; Chaffin, 1973; Leighton, 1973].

The initial approach to measurement was to proceed on the basis that harmonic content is low. Once the measurement system was operating, the actual harmonic levels could be measured in an attempt to justify the initial assumption. Upon doing this all harmonics were found to be at least 25 dB lower in strength than the fundamental signal. These measurements were taken under the condition of maximum signal drive with no transistor saturation. Neglecting the effects of harmonics upon the measured quantities was therefore considered legitimate. A justification of such low harmonic levels which is based on semiconductor device theory appears in chapter 3 of this report.

Returning to the diagram of Figure 2.1 one can see that the measurement setup can be separated into two parts. The first part consists mainly of the input directional coupler and is used to measure the input impedance of a device and the input incident power. The second part of the setup is centered around the output directional coupler. This is used to measure the values of load impedance, amplifier gain, and output power. The operation and calibration of these two parts will be discussed respectively in the following two sections of this chapter.

Also, presented in the third and fourth sections of this chapter are actual results of transistor measurements.

2.1 The Input Coupler

Figure 2.2 shows a flowgraph representation of the input portion of the measurement system. The reflection coefficient Γ at the right side of the flowgraph represents the unknown which is to be measured. Application of Mason's non-touching-loop rule to the flowgraph yields the following expression:

$$\frac{b_B}{b_A} = \frac{a' + b'\Gamma}{1 + c'\Gamma} \qquad (2.1)$$

This is a reasonable result because the basic form of Mason's rule is that of a bilinear transform.

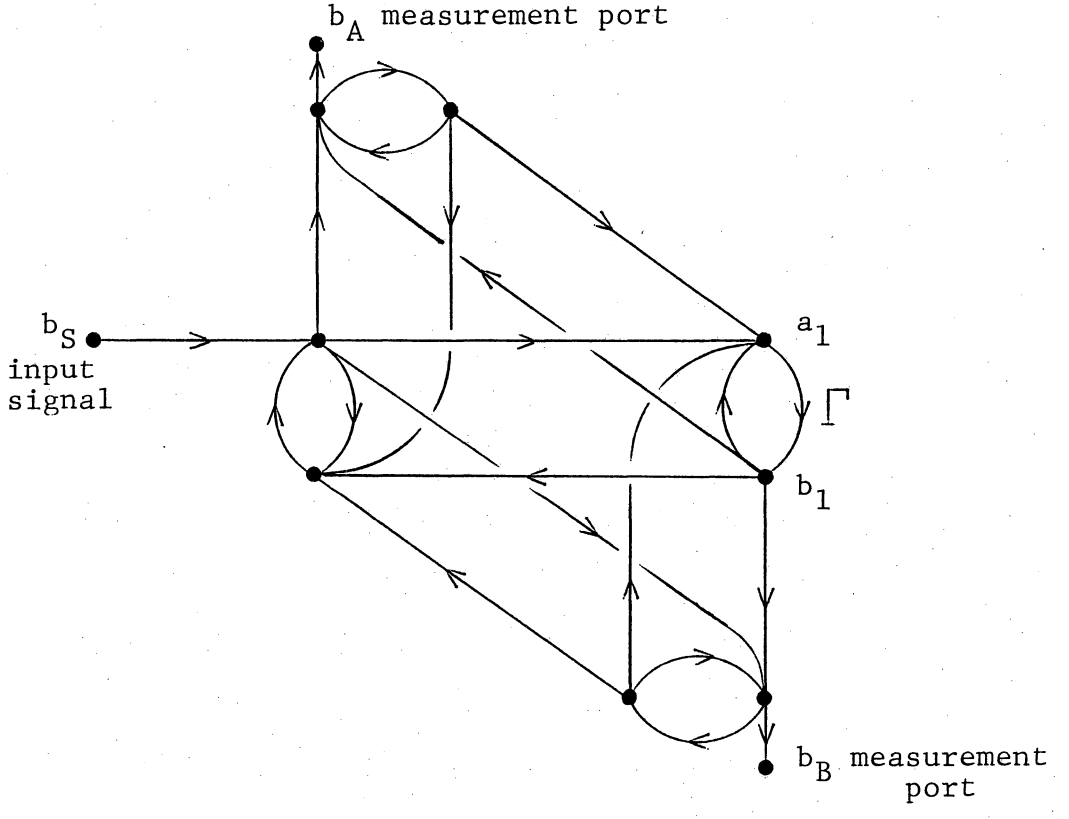

Figure 2.2 The input portion of the measurement system.

If the values of the constants a', b', and c' are known then any unknown reflection coefficient can be deduced from the voltages b_A and b_B taken at the coupler measurement ports. A rearrangement of Equation 2.1 illustrates this.

$$\Gamma = \frac{a' - b_A/b_B}{c' \, b_A/b_B - b'} \tag{2.2}$$

The calibration of the measurement system yields the values of a', b', and c'. Placing three different known reflection coefficients on the right-hand port of the system and reading the respective measurement-port voltages, one can construct three equations in three unknowns, a', b', and c'. (Actually this represents six equations in six unknowns because all quantities are complex.) The ideal known reflection coefficients to use would be those of an accurate 50 Ohm load, an accurately located short-circuit termination, and an accurately located open-circuit termination. In this experiment a short-circuit termination and a 50 Ohm termination were used, but unfortunately an accurate open circuit termination was unavailable. In place of this, a short connected to an approximately one-eighth wavelength transmission line and a short connected to an approximately one-quarter wavelength transmission line were used.

Because the exact lengths of these transmission lines are unknown, only the magnitudes of the measurements using these two terminations were used, thus providing the fifth and sixth equations.

The solution of the resulting equations for a', b', and c' is relatively straightforward. For the case of the 50 Ohm termination (which has a reflection coefficient equal to zero), Equation 2.1 immediately yields the value of a'. The remaining four equations are solved algebraically by substitution of one equation into another. Actual numerical calculations are done using a computer.

Again applying Mason's rule to the flowgraph of Figure 2.2 the following result can be obtained:

$$\frac{a_1}{b_A} = \frac{g'}{1 + c' \Gamma} \qquad (2.3)$$

The constant c' appearing in the denominator is already known, one additional measurement is necessary to determine the constant g'. This is done by placing a 50 Ohm termination on the system (forcing the reflection coefficient Γ to zero), measureng the voltage a_1 across this termination, and forming the ratio of a_1 to the measured quantity b_A. This ratio is identically the constant g'.

Equation 2.3 can be solved for the value of a_1.

$$a_1 = b_A \frac{g'}{1 + c'\Gamma} \tag{2.4}$$

Knowing the constants c' and g' one can use this equation along with the measured voltage at the forward port of the coupler to compute the power incident upon the unknown port of the system when any arbitrary device is connected. This is the case because the power is proportional to the square of the voltage, a_1.

2.2 The Output Coupler

Figure 2.3 is a flowgraph representation of the output coupler portion of the measurement system. The reflection coefficient Γ_t represents the three stub tuner. The reflection coefficient Γ_L represents the load presented to the output terminals of the device under test. By applying Mason's rule a relation between the load reflection coefficient and the coupler measurement-port voltages can be derived,

$$\frac{b_D}{b_C} = \frac{a + b\Gamma_L}{1 + c\Gamma_L} \tag{2.5}$$

Again there are three constants which must be determined in a calibration process. The situation presented here is similar to that found in the calibration

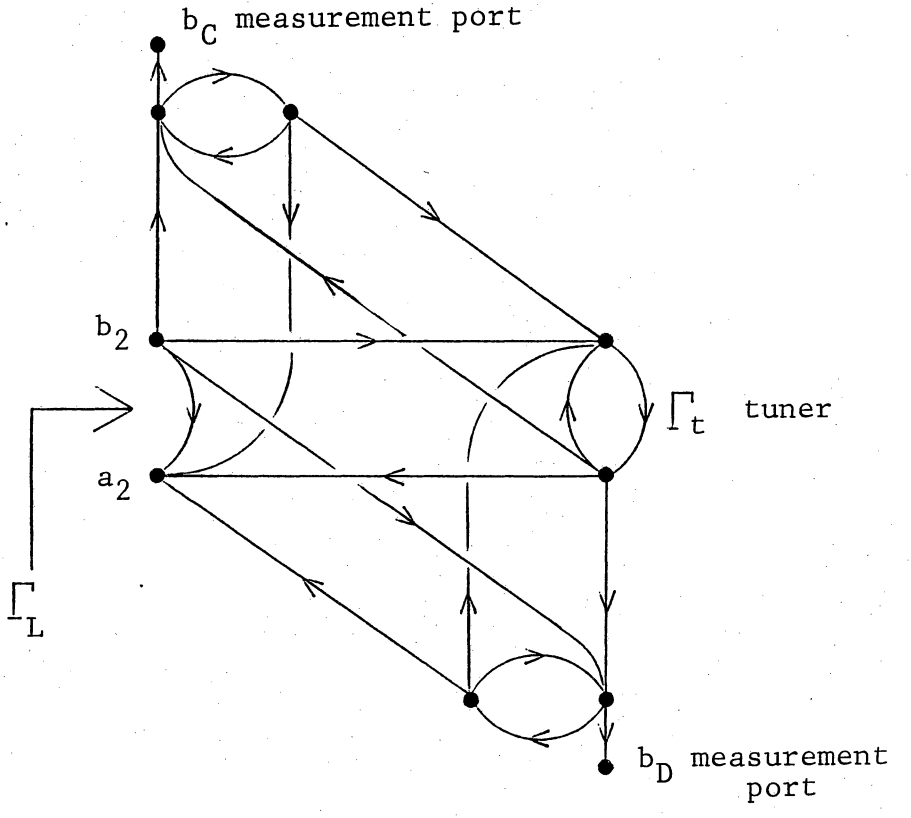

Figure 2.3 The output portion of the measurement system.

of the input coupler. Three different reflection coefficients (Γ_L) yield respective measured ratios (b_D/b_C) thus providing three complex equations in three complex unknowns. The case at hand does not require three accurately known standard terminations, though. In this case the three stub tuner is adjusted to three convenient values, and the resulting reflection coefficients (Γ_L) can be measured with the previously calibrated input coupler.

The resulting equations are more difficult to solve than those for the case of the input coupler calibration. This is so because none of the three adjustments of the three stub tuner will necessarily correspond to a zero reflection coefficient (Γ_L in Equation 2.5). Therefore all six equations must be solved simultaneously in contrast to the simultaneous solution of only four equations in the input calibration. In this experiment the six equations were solved using a Gauss elimination procedure.

A rearrangement of Equation 2.5 indicates that once the three constants are known, the reflection coefficient presented to the device under test for any adjustment of the three stub tuner can be determined from the voltages read at the coupler measurement ports.

$$\Gamma_L = \frac{a - b_D/b_C}{c\, b_D/b_C - b} \tag{2.6}$$

Finally, referring to the flowgraph of the overall system in Figure 2.1, an expression relating the transmission coefficient, $\tau = b_2/a_1$, to the two measured forward port voltages can be derived.

$$\frac{b_C}{b_A} = \frac{b_C}{b_2} \times \frac{b_2}{a_1} \times \frac{a_1}{b_A} = \frac{b_C}{b_2} \times \tau \times \frac{a_1}{b_A} \tag{2.7}$$

Equation 2.3 provides an expression for the third factor of Equation 2.7, and Mason's rule is used to find an expression for the first factor in this equation. Thus,

$$\frac{b_C}{b_A} = \frac{1 + c\,\Gamma_L}{e + f\,\Gamma_L} \times \tau \times \frac{g'}{1 + c'\,\Gamma} \tag{2.8}$$

(Note that b_C appears in the denominator of Equation 2.5 and in the numerator of Equation 2.7, thus the factor $(1+c\Gamma_L)$ is in the denominator of Equation 2.5 and in the numerator of Equation 2.8)

Two additional constants, e and f, appear in the expression of Equation 2.8. A procedure is necessary to solve for these. Connecting the output of coupler one to the input of coupler two is equivalent to placing a network with a unity transmission coefficient between the couplers, and at the same time forcing Γ to be equal to Γ_L. Making such substitutions in Equation 2.8, one can see that taking measurements with two different values of Γ results in two

complex equations which are are sufficient to solve for e and f.

Equation 2.8 can be solved for the transmission coefficient τ in terms of measured quantities. Now that e and f are known, the transmission coefficient of any arbitrary two-port can be computed from measured quantities. Additionally, if the power incident on port one of the device under test is known and if the transmission coefficient is known, then the power leaving port two of any device under test can be computed.

2.3 Measurement Philosophy

The transistor was mounted on a piece of fiberglass-epoxy copperclad board. The copper coating on one side was left intact to act as a ground-plane for 50 Ohm microstrip transmission lines on the opposite side of the board. The transistor and bias network were connected between two sections of this microstrip line.

Two reference measurements were made before the transistor was mounted. First, the board with only a through section of 50 Ohm transmission line was measured in order to determine its phase delay and to determine any reflections from discontinuities along the line. Once known, these effects could later be subtracted from measured transistor data. Second, the bias network alone

was measured so that its effects could later be removed.

Two sources of error are inherent in the mounting technique used. First, if the impedance of the microstrip transmission line is not exactly 50 Ohms its effect is to act as an impedance transformer of unknown transformation ratio. This effect is virtually impossible to remove by any sort of calibration. Therefore care was taken in constructing the 50 Ohm transmission line and any small factor of error (probably not more than one or two percent) was accepted.

The second source of error arises because the leads manufactured on the transistor do not have a characteristic impedance of 50 Ohms when placed above the ground-plane, the impedance is actually 32 Ohms. The length of the leads is short and any detrimental effects originally were assumed to be negligible. This assumption was erroneous, upon the completion of measurements this short section of 32 Ohm transmission line was discovered to be introducing a constant phase error into the results.

There are three potential solutions to this problem. One would be to mount the transistor on a material where the transistor leads would have a characterisitc impedance of 50 Ohms. Another solution is to mount the transistor between two tapered transmission lines which would act as transformers of known transformation ratio between the 50

Ohm measurement system and the 32 Ohm transistor leads. In this latter case all reflection coefficients must be referenced to 32 Ohms instead of 50 Ohms. Either of these solutions would have to be done from the outset of an experiment.

A third solution may be used after the experiment is completed. Figure 2.4 shows a flowgraph representation of the situation created by the transistor leads. The angle ϕ can be estimated from physical measurement of the lengths of the transistor leads. The measured value of, say, a reflection coefficient can be translated leftward along a length of 50 Ohm transmission line and then translated back through the circuit represented by the flowgraph of Figure 2.4. This yields the actual reflection coefficient. One should note that this actual reflection coefficient is referenced to a 32 Ohm transmission line. The expression used to perform the correction discussed above is

$$\Gamma_{actual} = \frac{\Gamma - \Gamma_f e^{-j(2\pi-\phi)}}{\tau_f\tau_r - \Gamma_f\Gamma_r + \Gamma\Gamma_r e^{-j2\phi}} \qquad (2.9)$$

Application of Mason's rule to the flowgraph of Figure 2.4, followed by some algebraic manipulation, was used to derive this equation. All of the data presented in the following section were corrected using this expression.

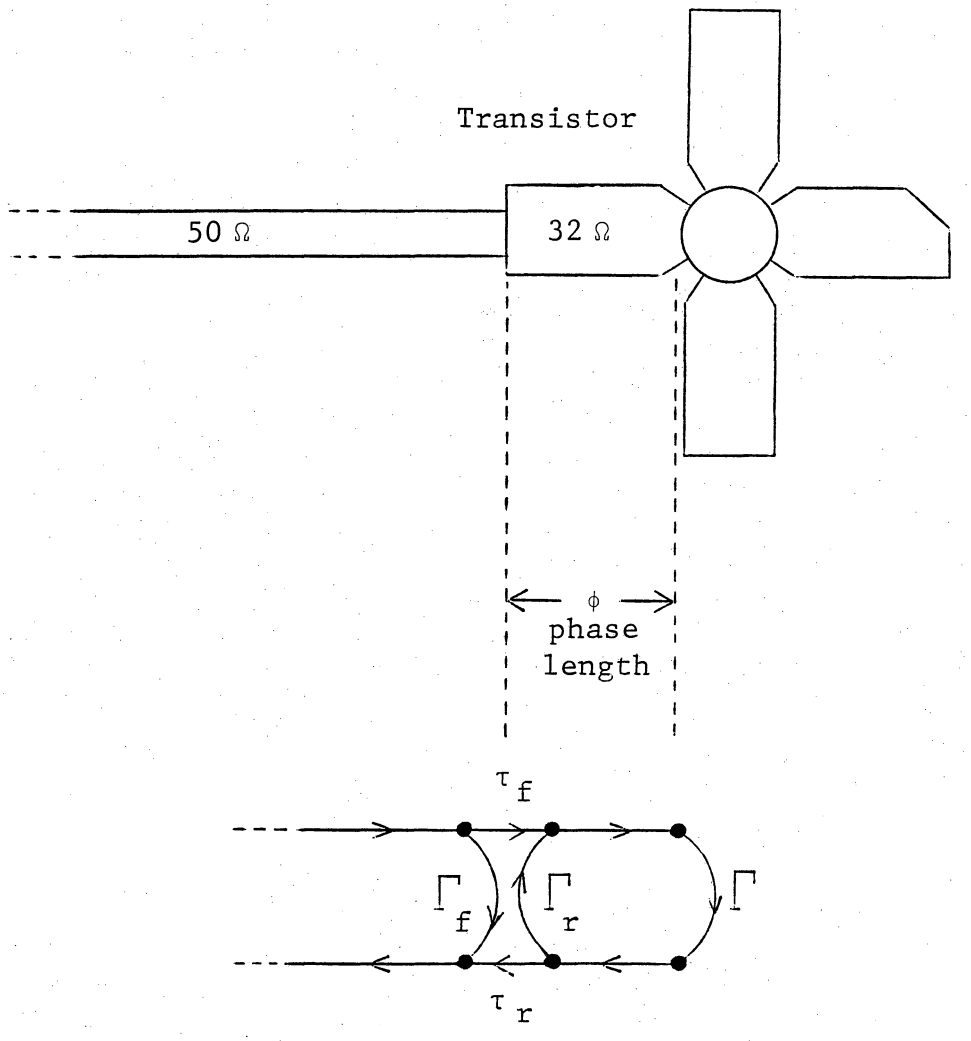

Figure 2.4 Flowgraph for lead correction.

All transistor data presented in this report were measured at a frequency of 175 MHz. In the process of investigation some data were taken at other frequencies when such measurements aided in the determination of transistor characterisitics. All transistor measurements presented herein were made with a collector voltage, V_{CC}, of 12 Volts, and a quiescent collector current of 10 milliamperes. This quiescent condition essentially biases the transistor for class B operation even though in a strict sense this bias results in class AB operation. One can see that it is reasonable to assume class B bias because the 10 milliampere quiescent current is sufficiently small when compared to the nominal operating current of the transistor (on the order of Amperes) to classify the transistor as being in cutoff. Again, in several cases during the investigation, measurements with other bias conditions were useful.

Care was always taken to avoid saturating the transistor. This was done by monitoring the collector voltage waveform with a high frequency oscilloscope. The onset of saturation is readily apparent upon viewing this waveform. Additionally, the onset of saturation as viewed on the oscilloscope has been correlated with observed changes in transistor input impedance and observed changes in DC collector current, both also indicating saturation.

2.4 Results of Measurements

The first step in the measurement sequence was to determine the effect of the load upon the operation of the transistor. As a preliminary to this, the largest value of signal drive was determined which would guarantee operation in the non-saturation region under all load conditions of interest. Then the drive level was fixed at this value for all of the measurements in this portion of the experiment. Later it was determined that the important result from this portion of the experiment (i.e. the determination of the optimum load impedance for the transistor) is relatively insensitive to drive level as long as saturation does not occur.

The input (base) impedance of a power BJT is quite low. In the measurement setup this low impedance is driven from a 50 Ohm source, therefore the transistor can be viewed as being driven by a current source. The importance of this lies in the fact that the drive current to the transistor will be only minimally affected by any load changes which might be coupled to the input through any feedback mechanism.

The measurement procedure followed was this: 1) a value for the magnitude of the load reflection coefficient was selected and obtained using the three stub tuner, 2) the phase angle of the load reflection coefficient was

varied by changing the length of the adjustable length transmission line until maximum power output was obtained, 3) data were taken by measuring voltages at the four directional coupler measurement ports, 4) then the process was repeated for a different magnitude of reflection coefficient.

Results of this procedure are plotted on the Smith chart of Figure 2.5 where the reflection coefficients for maximum power are shown. Each point represents a different magnitude of reflection coefficient or, alternately, one can say that each point represents a load impedance with a different real part. The important thing to note is that the imaginary part of the load impedance which is required to yield maximum power is always very nearly +j4.0 Ohms, independent of the value of the resistive part. This implies that some sort of resonance effect is taking place. This will be discussed in the next chapter.

The values of output power associated with each point of figure 2.5 were computed. The result of this is presented in Figure 2.6 which shows a plot of the output power as a function of the resistive component of the load impedance. The maximum power point occurs at a load resistance of approximately 12.0 Ohms. If one compares the measured data of Figure 2.6 to a plot of power delivered to a resistor driven from a 12.0 Ohm Thevenin source (dashed

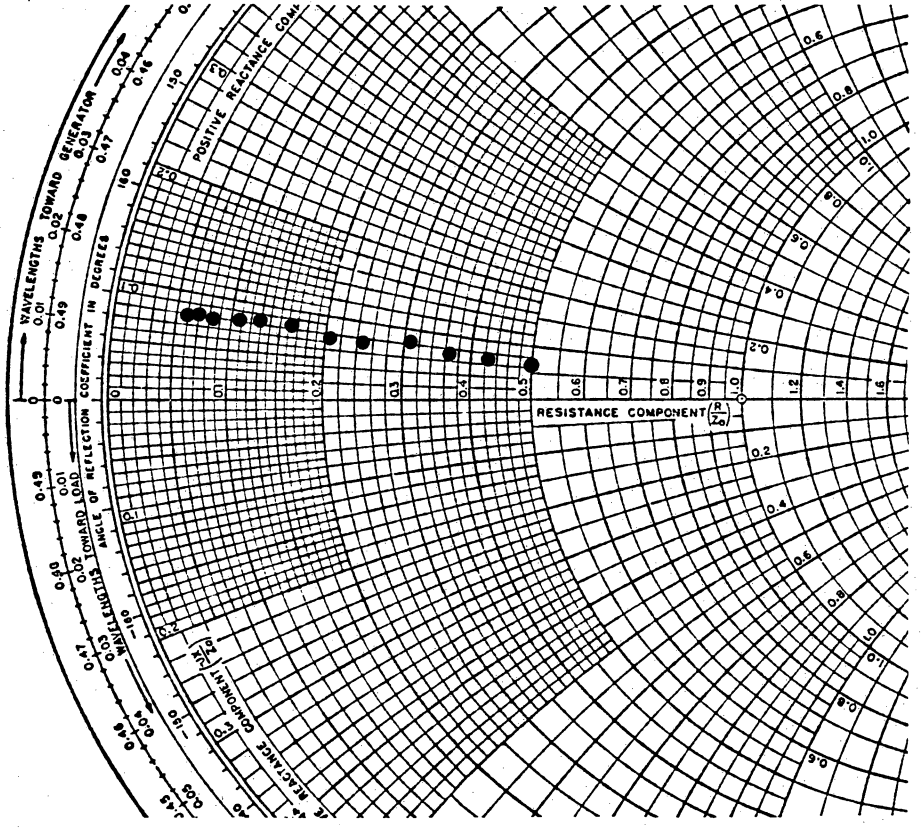

Figure 2.5 Loads which yield maximum output power. All values are normalized to 50Ω. The Smith chart is courtesy of Phillip H. Smith of Analog Instruments Co., New Providence, N.J.

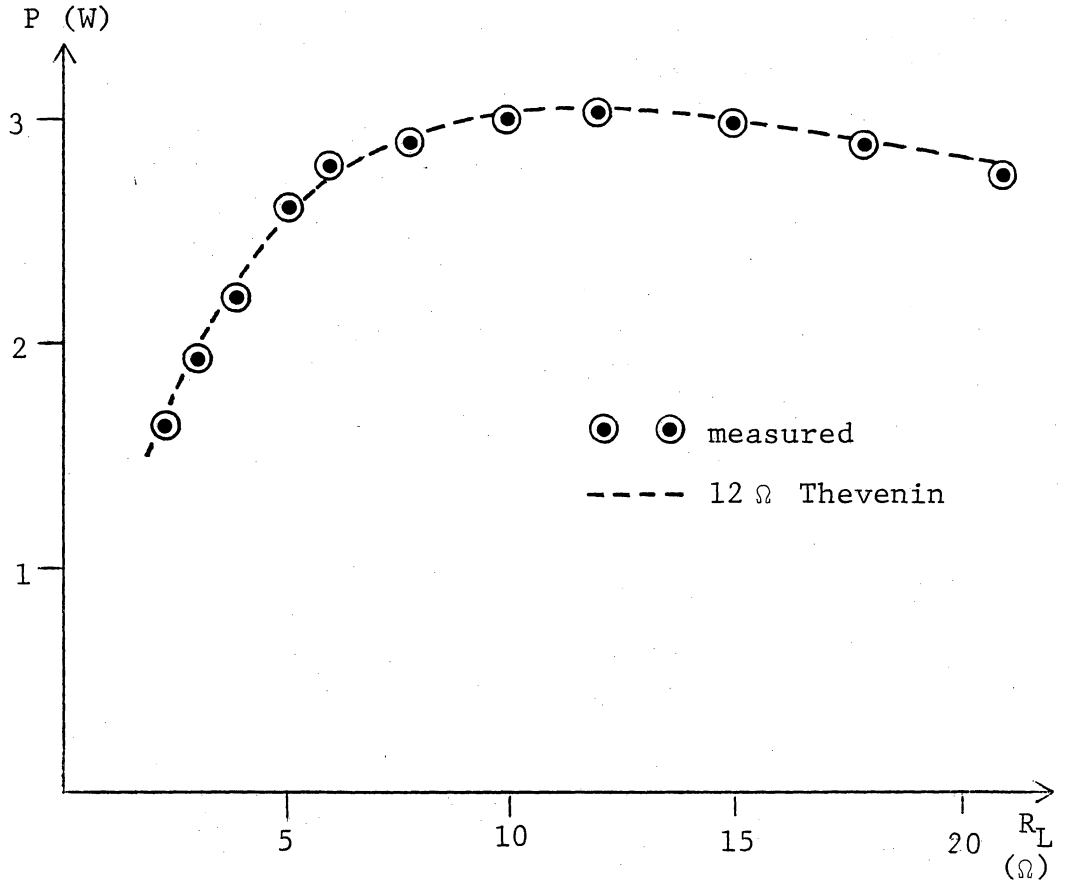

Figure 2.6 Output power versus load resistance.

curve of Figure 2.6), one can see that the two plots are virtually identical. This, along with the resonance phenomena discussed above, implies that a complex conjugate match is required in order to obtain maximum power from the transistor.

This result might not seem to be particularly special, but it is indeed significant in light of the typical view of an RF power transistor. This result is in direct opposition to the ideal current source model of a BJT. An explanation of the observed phenomenon is presented in Chapter 3.

One should again note that this result is relatively insensitive to drive level. Data were taken over a range of drive levels down to a factor of 30 smaller than that used to take the data of Figures 2.5 and 2.6. No discernible difference in the imaginary part of the optimum load impedance was noted. The procedure for determining the optimum real part of the load impedance is much more difficult. Therefore data were taken over a 3 to 1 range in drive level, again with no discernible change in the optimum load resistance. Worthwhile noting is that the plot of output power versus load resistance as shown in Figure 2.6 exhibits a very broad peak. One could reasonably extrapolate from this that the optimum load resistance would be a mild function of other quantities,

such as drive level.

The next step in the measurement procedure was to fix the load at its optimum value of 12.0 +j4.0 Ohms and then investigate the input characteristics of the transistor. This was done for a variety of drive levels. The results of this are tabulated in Table 2.1 and also plotted in Figure 2.7 where the device input impedance versus drive level is shown. The upper point on the Smith chart corresponds to maximum drive (just short of saturation) and the lower point corresponds to a drive level which is a factor of 30 smaller. This range of drive levels is adequate for characterizing RF power amplifiers used in typical communication applications. Note that there is only a small variation in the input impedance as a result of changes in drive level.

Data were also taken for the cases of load impedances different from the optimum value. A plus or minus variation of five Ohms in both the real and the imaginary part of load impedance did have a very small effect on measured input impedance. The variation of input impedance with load changes was on the order of the variation of input impedance with drive level. This effect is considered negligible in terms of its impact on a practical design. This is substantiated by DeMaw's [1984] statement that there is little interaction between the input and

Table 2.1

Summary of Measured Data

Pinc (W)	Re{Zin} (Ohms)	Im{Zin} (Ohms)	$\|\tau\|$	$\angle\tau$ (degrees)	Pout (W)	Ic (mA)	η (%)
0.014	1.17	-2.22	2.3	-272.4	0.048	63	6.4
0.046	1.45	-1.72	2.8	-273.9	0.22	137	13.5
0.14	1.66	-1.43	3.1	-275.9	0.85	281	25
0.25	1.85	-1.29	3.2	-276.8	1.59	393	34
0.46	1.78	-1.15	3.3	-278.0	2.99	554	45

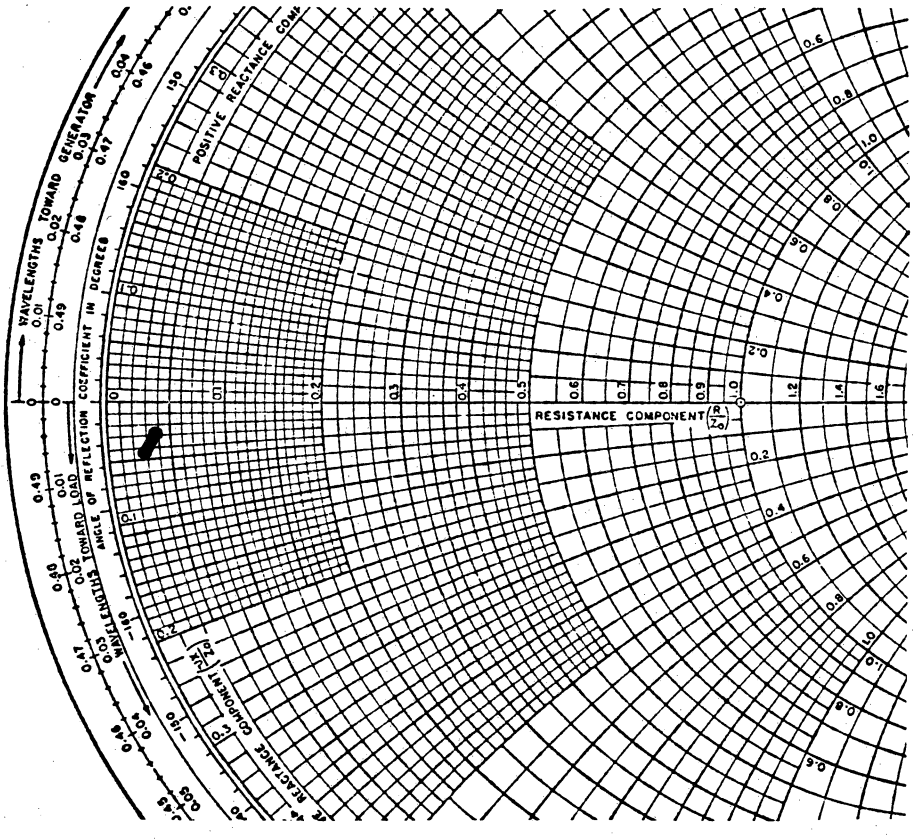

Figure 2.7 Input impedance versus drive level. Maximum drive is at top. All values are normalized to 50Ω.

output tuning of typical VHF power amplifiers.

In the process of these measurements, data required to compute the forward transmission coefficient were also taken. The values of transmission coefficients corresponding to different drive levels are tabulated in Table 2.1. Other important quantities, specifically the DC collector current, the power output, and the efficiency are also tabulated there. All of these quantities are tabulated for easy future reference. All of these will be compared to theoretical predictions using the model which will be developed in Chapter 3.

2.5 Summary

A measurement system and a calibration procedure were developed. The measurement system is a combination of the standard two coupler S-parameter setup and the variable load "load-pull" system. A significant aspect of the measurement system is the method by which the load presented to the transistor can be easily determined without actually removing the load. Most techniques presented in the literature require removal of the load from the system in order to determine the load impedance. Also of general importance is the fact that the calibration procedure for the measurement system is flexible in that it is adaptable to the reference standards available at

hand.

Results of physical measurements were also presented. The most noteworthy result is that a complex conjugate match is required on the amplifier output in order to obtain maximum power. It is noteworthy because one would expect the supposed current source nature of the transistor to allow increasing power for decreasing load resistance. One might also expect the maximum power transfer theorem not to hold for the case of the supposed nonlinear BJT.

In the next chapter a theoretical model for the transistor is developed. The justification for this model will rest upon its being able to predict results which are consistent with the measurements presented in this chapter. The model will also provide insight into many of the processes taking place within the transistor.

CHAPTER 3

Transistor Model

A model for the transistor must be based on sound semiconductor theory. The model must accurately predict actual operating characteristics, particularly the phenomena presented in the previous chapter. Finally, the model should be simple enough to make it useful as a basis for a design procedure.

Such a model is developed in this chapter. It is a version of the well known Ebers-Moll model. No credit is taken for the actual conception of the model; credit is taken only for the particular application presented in this dissertation.

3.1 Background Theory

The frequency characteristic of the common emitter forward current gain β is shown in Figure 3.1. The three dB corner frequency is f_β and the unity gain frequency (the transition frequency) is f_T. If one were to plot the reverse gain of a transistor it would be an increasing function of frequency. This is the case because the major reverse transmission mechanism in a transistor is

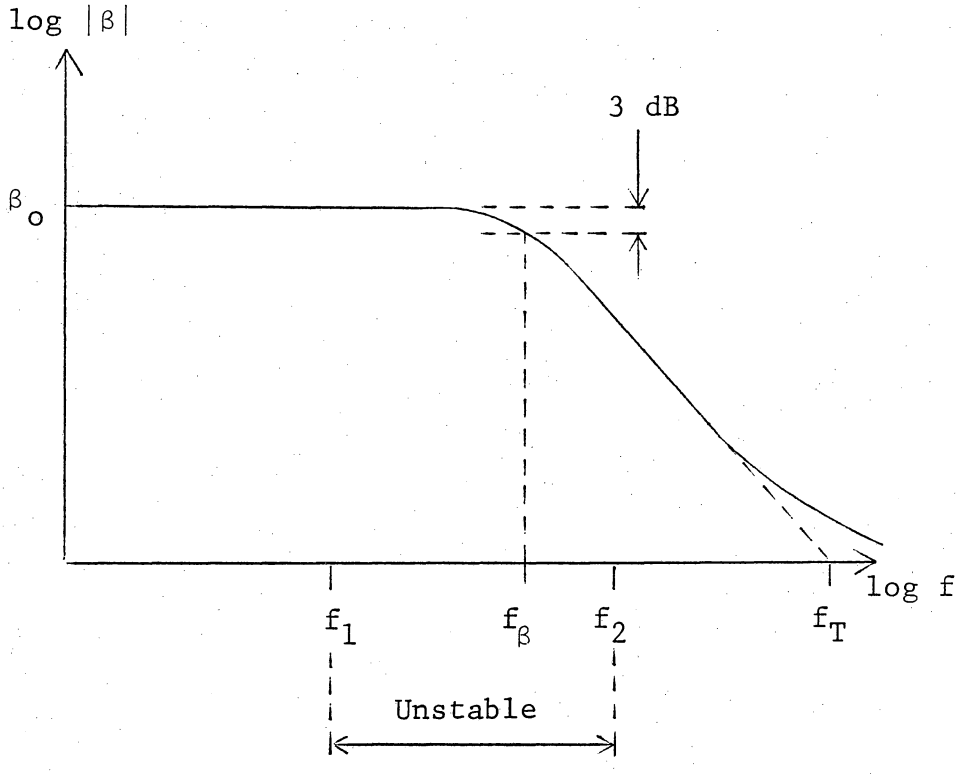

Figure 3.1 Common emitter forward current gain.

capacitive.

A region of instability is indicated on the plot of Figure 3.1. The reason that the transistor is stable at low frequencies is because the reverse transmission is small enough to result in a loop gain of less than unity. Similarly, at high frequencies the forward gain is small enough to create a less than unity loop gain. Only in the intermediate range of frequencies is the product of forward and reverse gains sufficient to cause instability.

As an interesting side-line one might note that frequency f_1 defining the lower limit of instability is proportional to the DC value of transistor collector current, and the upper limit f_2 is inversely proportional to this current [Muller, 1967]. Therefore the region of instability expands when the collector current is decreased. Typically, the DC collector current and drive level of an amplifier are related. This is the reason why an amplifier which is stable at one drive level might become unstable at a different drive level.

Virtually all radio frequency power amplifiers are operated in the upper region of stability. The difficulty of manufacturing power transistors with extremely high values of f_T precludes the use of the lower region of stability. The frequency f_1 is typically somewhere between one one-hundredth and one one-thousandth of the value of f_T

[Muller, 1967]. If a 175 MHz power amplifier were operated below frequency f_1 it would require a transistor with an f_T on the order of many Gigahertz. For comparison, the TRW PT8828 used for the measurements of Chapter 2 has an f_T of about 450 MHz.

There are two important implications of operating transistors at high relative frequencies. First, the common emitter forward current gain β will have a small magnitude and a phase angle of nearly 90 degrees. The small magnitude of current gain is the reason why most RF power amplifiers have small power gains. Second, the fact that the operating frequency is greater than f_2 (which itself is greater than f_β) implies that the period of the signal waveform is much shorter than the minority carrier base recombination time.

This last statement can be proven. The transition frequency of a transistor is related to the time taken by a carrier to travel across the base region [Pedin, 1970]. This time is called the base transit time and is represented by the symbol τ_1.

$$f_T \approx \frac{1}{2\pi\tau_1} \tag{3.1}$$

The three dB corner frequency and the transition frequency are related by

$$f_T = \beta_o f_\beta \tag{3.2}$$

where β_o is the low frequency common emitter current gain. Finally, from Gray [1964], the low frequency common emitter current gain, the base transit time, and the base minority carrier recombination time τ_β are all related by

$$\beta_o = \tau_\beta / \tau_1 \tag{3.3}$$

Therefore,

$$f_\beta = \frac{1}{2 \pi \tau_\beta} \tag{3.4}$$

Because of the inverse relationship between signal frequency and period one can see that if the signal frequency is much greater than f_β then the signal period must be small compared to the recombination time.

Turning now to a basic charge-control model of a transistor [Gray, 1964; Koehler, 1967; Holt, 1978], this model predictes that the collector current of a transistor operating in the active mode is given in terms of the stored base charge, q, by

$$i_C = q/\tau_1 \tag{3.5}$$

This is quite reasonable because a net charge of q moves completely through the base in the period of time τ_1, the base transit time.

The charge-control model shows the base current as having two major components, a recombination component which is given by the first term in the following equation, and a component proportional to the time rate of change of stored base charge.

$$i_B = q/\tau_\beta = dq/dt \tag{3.6}$$

(Transition capacitance charging currents are neglected in the two charge-control equations above. This current has only a small effect when related to the large operating currents present in power transistors. Further justification for this will be presented.)

The fact has already been shown that for the case of a transistor operated at a frequency much greater than f_β, the period of the signal waveform is much shorter than the base carrier recombination time. This being the case, the first term in the previous equation is very small compared to the second term. This implies that recombination is a

minor effect in a transistor operated in a fashion such as this.

A combination of the previous two equations will be important in the work to follow in this report.

$$i_B = \frac{\tau_1}{\tau_\beta} i_C + \tau_1 \frac{di_C}{dt} \tag{3.7}$$

(Interestingly, one might note that the inverse of the factor multiplying i_C is the low frequency current gain, β_o, {reference Equation 3.3.} One can also see that Equation 3.7 implies a current gain i_C/i_B whose magnitude decreases with increasing frequency and whose phase angle tends toward -90 degrees with increasing frequency.)

The charge-control model is essentially a mathematical model for the transistor. In the next section attention will be focused on a circuit model which will be amenable to circuit analysis. The charge-control results developed in this section will be applied to the analysis of this circuit model.

3.2 The Transistor Model

The circuit model settled upon for the work of this project is shown in bold lines in Figure 3.2. The basis for this model is the forward portion of the Ebers-Moll transistor model. To this has been added the effect of the

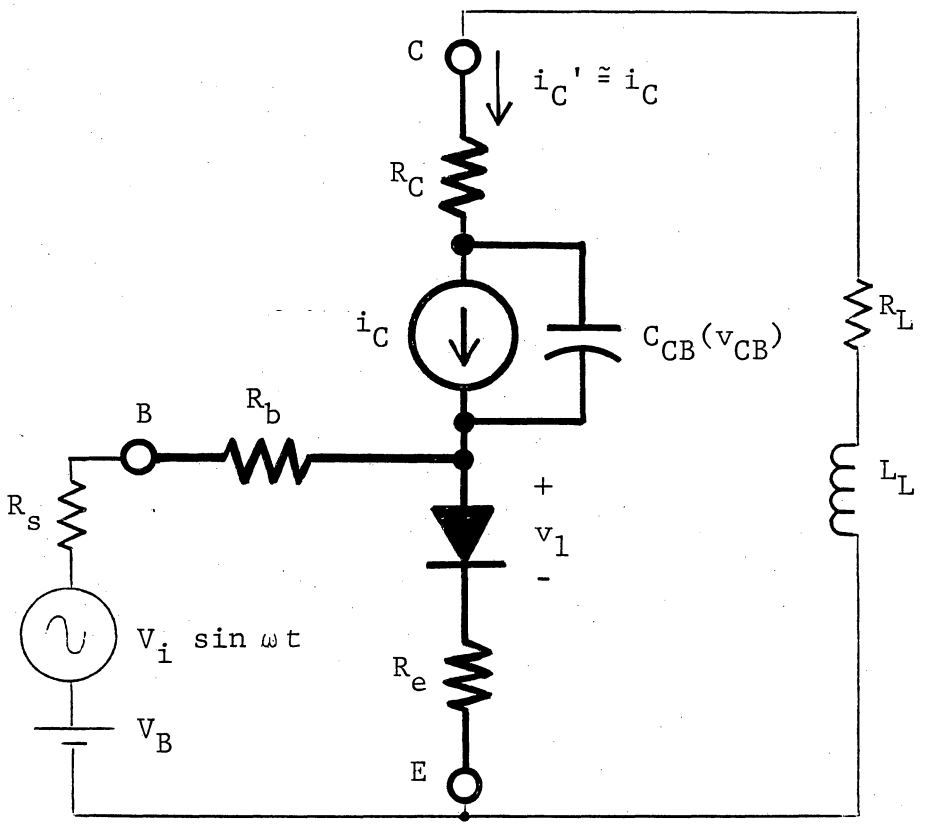

Figure 3.2 The transistor model.

reverse biased collector-base junction capacitance $C_{CB}(v_{CB})$. Note that this capacitance is voltage dependent. Also added to the basic model are bulk semiconductor resistances.

The Ebers-Moll model gives the current due to the current source as an exponential function of the voltage appearing across the base-emitter diode. This function can be solved for the voltage.

$$v_1 = \frac{kT}{e} \ln \left\{ \frac{i_C}{I_S} + 1 \right\} \tag{3.8}$$

The remainder of the circuit in Figure 3.2 represents a simplified version of an amplifier. The voltage source V_B is whatever value is necessary to bias the transistor at its quiescent point, 10 milliamperes or essentially class B in the case considered. The load is shown as having an inductive component. This always will be the case in order to resonate the transistor output capacitance.

A loop equation around the base-emitter circuit under the quiescent (no-signal) condition is

$$-V_B + I_{BQ}(R_s + R_b) + \frac{kT}{e} \ln \left\{ \frac{I_{CQ}}{I_S} + 1 \right\} + (I_{BQ} + I_{CQ}) R_e = 0 \tag{3.9}$$

Taking the same loop, but with an applied signal yields

$$-V_B - V_i \sin \omega t + i_B (R_s + R_b)$$

$$+ \frac{kT}{e} \ln \left\{ \frac{i_C}{I_S} + 1 \right\} + (i_B + i_C) R_e = 0 \qquad (3.10)$$

Two quantities, V_B and I_S can be eliminated by substituting Equation 3.9 into Equation 3.10. Then the charge-control relationship between base and collector currents, Equation 3.7, can be substituted yielding a first order nonlinear differential equation. Finally the time derivative can be manipulated into a derivative with respect to the angle $\theta = \omega t$,

$$\frac{di_C}{dt} = \frac{1}{\omega \tau_1 (R_b + R_s + R_c)} \left\{ V_i \sin \omega t - \frac{kT}{e} \ln \left\{ \frac{i_C + I_S}{I_{CQ} + I_S} \right\} \right.$$

$$\left. - (i_C - I_{CQ}) R_e - \left\{ \frac{i_C}{\tau_\beta / \tau_1} - I_{BQ} \right\} (R_b + R_s + R_e) \right\} \qquad (3.11)$$

This equation and its derivation are similar to those of Meyer [1967].

A representative solution to this differential equation is shown in Figure 3.3. This solution was formed using typical element values (those measured for the TRW PT8828; see Section 3.3) and a typical drive level (equivalent to maximum drive with no saturation as discussed in Chapter 2). A time stepping numerical method

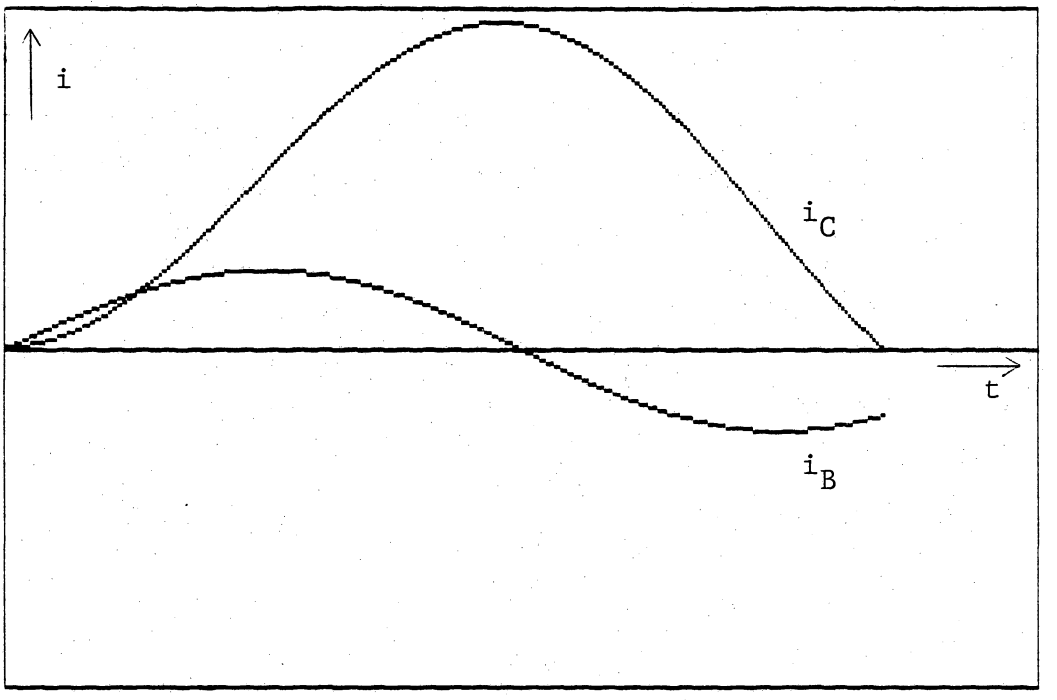

Figure 3.3 Current solution of the differential equation.

of solution was used.

Disregarding for the moment the portion of the collector current waveform to the far right, the waveform appears nearly sinusoidal. This collector current waveform is consistent with waveforms measured and/or predicted by others for similar amplifiers [Meyer, 1967; Bailey, 1970; Pedin, 1970; Johnston, 1972].

The solution for the base current waveform is also shown in the figure and it is nearly sinusoidal. (The base current waveform will drop to zero a short time after the collector current reaches zero. This time delay is associated with the discharging of the two junction transition capacitances. This phenomenon is not included in the model from which Equation 3.11 is derived, therefore the exact base current decay is not shown here.)

Several additional points about the equation and its solution are worth noting. First, confusion can be eliminated by realizing that the current I_{CQ} which appears in the equation is the quiescent collector current. This is different from the DC value of operating current under applied signal conditions. Referring to the collector current waveform of Figure 3.3, one sees that this waveform has a significant DC component. Second, the current flowing through the collector-base capacitance $C_{CB}(v_{CB})$ is relatively small compared to the current-source current

during most of the period. Therefore the amplifier load will have only a marginal impact upon the waveforms predicted by Equation 3.11. This will be discussed further, and proof will be given for neglecting the small current flowing through C_{CB}.

Because the transistor is biased for class B operation one would expect a collector current waveform which is a rectified half-sinusoid, not the waveform shown which has a 310 degree conduction angle. The intuitive explanation for this result is based on the fact that recombination of base charge is negligible and that time is required to remove residual base charge through the base lead. Collector current will flow until this charge is removed, thus the collector current will flow longer than half of a period.

This intuitive explanation can be substantiated by looking at the time relationship between base and collector currents as presented in Figure 3.3. One can see that during the time of positive base current (i.e. when the base charge store is increasing) the collector current increases. At the time that the base current drops to zero, the collector current reaches its maximum. (Actually, the very small amount of recombination moves the maximum just slightly ahead of the point of zero base current.) Then when base current becomes negative (charge is being removed from the base) the collector current

decreases.

This transistor possesses a self-biasing mechanism because of the charge storage effect occuring in the base. Even though the transistor is biased to operate class B, it is essentially operating as class A. In true class A operation, current flows during the full signal period, and the DC or average collector current is midway between the maximum and minimum values of instantaneous collector current. Normally, an external voltage or current must be applied to the transistor base in order to achieve class A operation, but in the case of this RF power transistor the charge storage phenomenon maintains the requisite value of DC current for nearly class A operation. If the transistor were externally biased to operate class AB or nonsaturating class C one would find the same result as seen here for external class B bias.

A confirmation of this class A operation is available. The theoretical maximum efficiency of a class A amplifier is 50%. Reference to the data in Table 2.1 shows an efficiency of just under 50% for the case of an amplifier operated with sufficient drive. Additionally, a review of manufacturer's data for VHF power transistors shows that most amplifiers have efficiencies on the order of 50% [Motorola, 1982]. DeMaw [1984] also notes the 50% typical efficiency.

A Fourier series analysis on the collector current waveform of Figure 3.3 yields a second harmonic component which is approximately 18 dB smaller in magnitude than the fundamantal component of current. The second harmonic component of terminal current in an actual operating amplifier will be even smaller than this because the inductive load in the collector loop will tend to keep current flowing even longer than that shown in the figure. (Any additional component of current would flow through C_{CB}). Actually, it will be proven later that the load inductance forms a resonant circuit along with the transistor capacitance. This resonance would ideally force the collector terminal current waveform to be sinusoidal. One correctly would expect the harmonic output of an amplifier operated in this fashion to be quite small.

Solutions to the differential equation for a variety of drive levels yield a fundamental component of collector current which is virtually linearly related to drive level. The implications of this for linear amplification are obvious. On the other hand, practical considerations, such as the temperature and current dependence of transistor characterisitics, will offset this and cause distortion.

One should note that the Fourier analysis also yields a value of DC collector current. Its magnitude will be large (on the order of Amperes) for a power amplifier. If

this large current were used to compute the dynamic resistance of the base-emitter junction of the transistor it would be found to be very small. Additionally, the reactance associated with base-emitter diffusion capacitance would also compute to be very small. The dynamic resistance and the diffusion reactance are incremental quantities and therefore have no bearing on the large signal characteristics presently under consideration. This incremental characterisitic of the base-emitter diode will be applied later, though.

Turning attention now to the base current waveform, Figure 3.4 shows a plot of this current (duplicated from Figure 3.3) along with a plot of the voltage at the base terminal. This figure also includes another voltage which will be discussed shortly. Very important to note is that there is a phase difference between the base current and the AC component of base voltage. This phase difference corresponds to the capacitive input impedance of a transistor of this type. This is a significant result and can be used to predict the input impedance of an RF power transistor if some basic model resistances are known.

An explanation of the base voltage-current phase difference follows. The solution to the differential equation can be used to yield values for the voltage v_A at the internal node of the transistor model. This is the

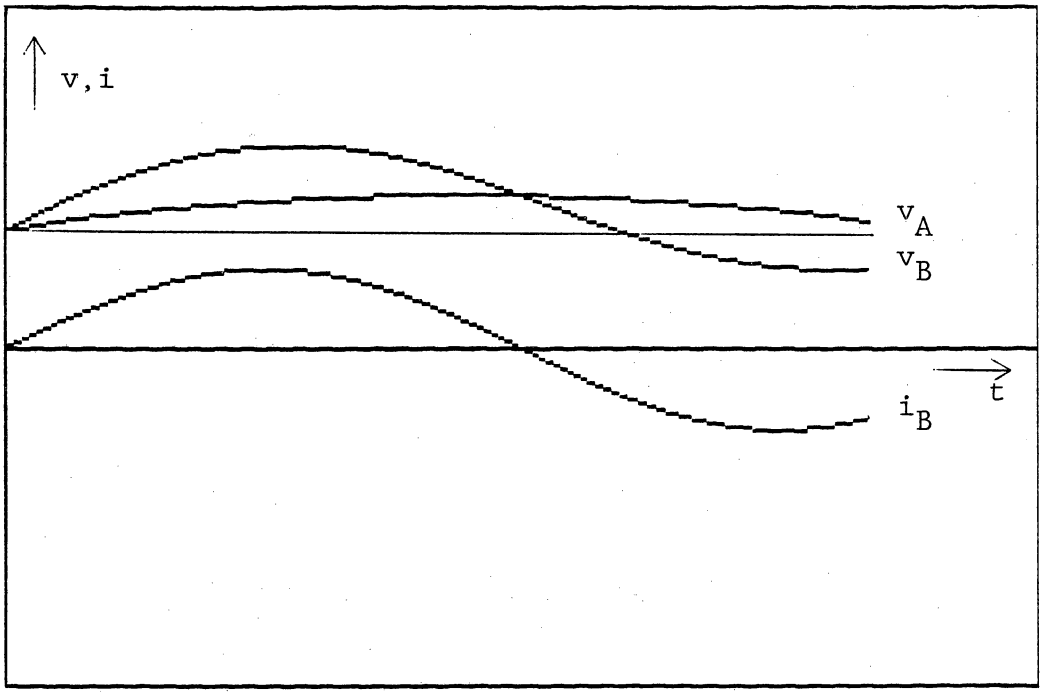

Figure 3.4 Base voltage-current relationship.

other voltage shown in the plot of Figure 3.4. The base terminal voltage is simply the sum of the voltage v_A and the voltage developed across the base ohmic resistance. This voltage across R_b is nearly sinusoidal and is in phase with the nearly sinusoidal base current waveform. The voltage v_A is a logarithmic function of the collector current, and it is seen to have a lagging component. Therefore the sum of v_A and the voltage across R_b will have a lagging component when compared to the base current.

Worthwhile emphasizing is that the base ohmic resistance R_b in conjunction with the nonlinear voltage developed across the base-emitter junction is the primary determining factor in the base voltage-current relationship. This factor is what creates an apparent capacitance at the input terminal of the transistor. This capacitive effect is not the result of any of the physical transistor capacitances (transition or diffusion) as is widely believed.

Also note that because the internal base node voltage goes as the logarithm of the current, errors incurred by neglecting the relatively small current through the capacitance $C_{CB}(v_{CB})$ will be minimal. This is substantiated by measurements of input impedance presented in Chapter 2. To see this, consider the fact that the mechanism of load-input interaction is through transistor

feedback, and this feedback is predominantly a result of current flow through $C_{CB}(v_{CB})$. The fact that the input impedance of the transistor is only lightly affected by load variations implies that feedback is minimal and thus the current through C_{CB} is small and can legitimately be neglected.

Now focusing attention on the output portion of the transistor model, Figure 3.5 shows the model with the applied base signal suppressed, with the load removed, and with a constant collector-base capacitance. The analysis to follow represents a perturbation about a typical operating point, therefore it will be assumed that the transistor is conducting a sufficiently large current to treat the very small base-emitter dynamic resistance and very large diffusion capacitance as incremental short circuits.

An applied AC voltage source, V, is shown connected to the output terminals. This voltage source will be used in anlaysis to determine the output impedance of the circuit. This is done by computing the current I and then forming the ratio of V to I. In this analysis the relative sizes of the base and emitter resistances allow neglecting any very small current through R_b. Also, the applied voltage will be assumed small enough to legitimately model the base-emitter diode by its incremental impedance.

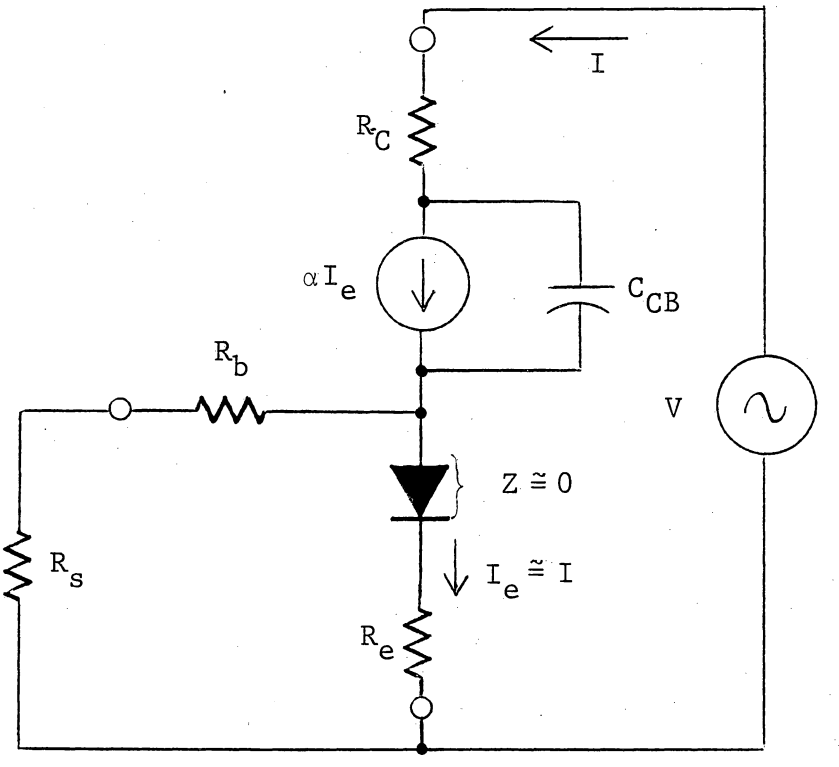

Figure 3.5 Circuit for determination of output impedance.

The result of such an analysis is shown,

$$Zo = R_c + R_e + (1 - \alpha) \frac{1}{j\omega C_{CB}} \tag{3.12}$$

This result is reasonable because a current $(1-\alpha)I$ flows through the capacitor.

The common-base current gain, α, of the transistor can be represented as having a single pole roll-off versus frequency [Lange, 1972].

$$\alpha = \frac{\alpha_o}{1 - j\ f/f_\alpha} \tag{3.13}$$

This implies that at the relatively high operating frequency of a typical RF power device the α will have a significant negative phase angle. Multiplying the imaginary impedance of the capacitor by $(1-\alpha)$ results in the output impedance, Zo, having a real component. This will aid in explaining the fact that there exists an optimum real part of the load for maximum output power. (Recall that the measurements of Chapter 2 indicate a conjugate match is necessary in order to obtain maximum amplifier output power. With the theory developed up to this point, one now sees that there is theoretical justification for this conjugate match phenomenon. Specifically, the nearly class A operation, along with the

approximately sinusoidal base and collector currents, implies that properties of a linear system are in effect. One should note that the transistor should not be driven into saturation if this is to hold true.)

The important implication of Equation 3.12 is that if the value of collector-base capacitance and the values of R_c and R_e are known (all three are easy to measure at low frequencies), then the value of the transistor output impedance can be predicted. This is a significant result. An illustration of the accuracy of this statement will be presented in the next section.

Finally, a side aspect of this phenomenon of output impedance is discussed by Choma [1969]. If an additional phase shift mechansim (such as a time delay) is present in the circuit, an output impedance with a negative real part can result. This will impact the stability of the amplifier. One might expect that this effect would be important only at UHF and microwave frequencies. At such frequencies time delays due to the finite physical size of a device are significant compared to the signal period.

3.3 Comparison of Measurement and Theory

In order to make meaningful comparisons of measurement and theory, some basic physical parameters of the transistor must be known with reasonable accuracy.

Specifically, these parameters are R_b, R_c, R_e, $C_{CB}(v_{CB})$, f_T, and the low frequency current gain β_o. The values of R_c, R_e, and β_o are easily measured on a curve tracer [Getreu, 1978]. The values of R_c and β_o are measured in the common emitter mode; R_c is given by the slope of the line defining saturation and β_o is determined from the separation of two adjacent curves of constant base current. Resistance R_e is not measured in the common emitter mode but in an alternate mode of operation of the curve tracer. The value of R_e is given by the slope of a line representing base current versus collector-emitter voltage for the case of collector current equal to zero. The values measured for the TRW PT8828 of Chapter 2 are: R_c = 1.0 Ohm, R_e = 0.05 Ohm, and β_o = 37.5.

The value of f_T is easily determined by measuring the current gain at some frequency higher than the 3 dB corner frequency. In the case at hand, data at three different frequencies of 125 MHz, 150 MHz, and 175 MHz were taken, all yielding the same value for f_T = 450 MHz. Worth noting is that the values of β_o and f_T presented above correspond to a corner frequency f_β of 12 MHz. The operating frequency of 175 MHz is indeed much greater than this, and therefore as previously discussed the signal period is small with respect to base recombination time.

The resistance R_b is a very difficult parameter to

measure. It is frequency dependent, current dependent, and temperature dependent [Krishna, 1968: Burton, 1969]. For the work to follow, its value was estimated. This estimate was based on the fact that the value of R_b can be no larger than the magnitude of the input impedance of the RF amplifier. The estimate used is R_b = 0.9 Ohm at room temperature. More details on how this estimate was made will be presented later.

Obtaining an accurate knowledge of the value of R_b is the most difficult aspect of the design procedure which was developed in the course of this project. The manufacturers of transistors could be of help here because R_b might be predicted based on a knowledge of transistor geometry.

The collector-base capacitance $C_{CB}(v_{CB})$ can be determined from measurements of the impedance of a reverse biased collector-base diode with the emitter lead open. First, the parasitic impedance of a dummy transistor package was measured so that its effect could be subtracted from the data. The impedance measurements were done at two frequencies, 10 MHz and 100 MHz. These frequencies were chosen because of the limitation on the equipment available for measurement. The results indicate that the capacitance is essentially frequency independent. This is consistent with the findings of Pitzalis [1973] which indicate that measurement at any low frequency is satisfactory.

An expression which accurately represents the measured data is given in Equation 3.14. This expression was arrived at by fitting measured data to an equation of the form predicted by semiconductor theory.

$$C_{CB}(V_{CB}) = \frac{49.4\ pF}{\sqrt{V_{CB} - 0.7}} \tag{3.14}$$

This result is almost identical to capacitance data which are presented on the transistor manufacturer's data sheet.

The collector-base voltage of an operating amplifier will be continuously changing with time, therefore the collector-base capacitance can be viewed as a function of time. Having a constant or an effective value for this capacitance would be desirable. Such a value was arrived at by analyzing a simple circuit containing a voltage-variable capacitance.

A sinusiodal voltage (representative of the voltage present on the output terminal of an actual amplifier) was applied to the voltage-variable capacitance. A time domain analysis was used to compute the functional form of the current flowing through the capacitance, then a Fourier series analysis was performed to determine the fundamantal component of this current. The ratio of the magnitude of the applied sinusoidal voltage and magnitude of the

fundamental current yields a value for the effective capacitive reactance. From this, the effective value of capacitance can be computed at the fundamental frequency.

The computed collector-base capacitive impedance for the PT8828 at 175 MHz is -j34 Ohms, corresponding to a capacitance of 26.7 pF. Interestingly, this value of effective capacitance is the same as that which would be computed if the quiescent collector voltage (V_{CC} = 12 Volts) was used in the expression for capacitance of Equation 3.14. Pitzalis [1973] observed that his measured value of effective capacitance was the same as the quiescent capacitance, an observation consistent with the findings above. Pitzalis had no explanation for his observation.

Another aspect of the voltage variable capacitance was investigated. One would expect that a capacitance of this type when placed in a resonant network would give rise to a nonsinusoidal response to a sinusoidal forcing function. In fact, many researchers indicate that in an amplifier the collector-base voltage variable capacitance is the dominant effect in determining the output waveform [Krauss, 1980; DeMaw, 1984; Glenn, 1985]. But upon solving the differential equation for an R-L-C(V) network using the capacitance expression of Equation 3.14 and using values of R and L which would be expected for a typical RF power

amplifier (R = 12 Ohms, inductive reactance = 6 Ohms), the harmonic components of the circuit response were found to be in excess of 35 dB below the fundamental component. This is another theoretical justification for the low measured values of harmonics in VHF RF power amplifiers. The statements made by Krauss, DeMaw, and Glenn most likely will be more appropriate in the case of saturating amplifiers.

Returning attention to the prediction of amplifier characteristics, with the information now at hand it is possible to predict the transistor input and output impedances. First the input impedance will be investigated.

The differential equation of Equation 3.11 can be solved for actual cases of interest now that the values of all constants in the equation are known. This was done for a variety of drive levels. These correspond to the drive levels used in the transistor measurements which were presented in Chapter 2. Base current and base voltage waveforms of the type shown in Figure 3.4 result. A Fourier series analysis for the voltage and current yields values of the fundamental frequency components of these quantities. The ratio of the fundamental components gives the predicted input impedance of the transistor. The results of such analysis are shown in Figure 3.6 where the

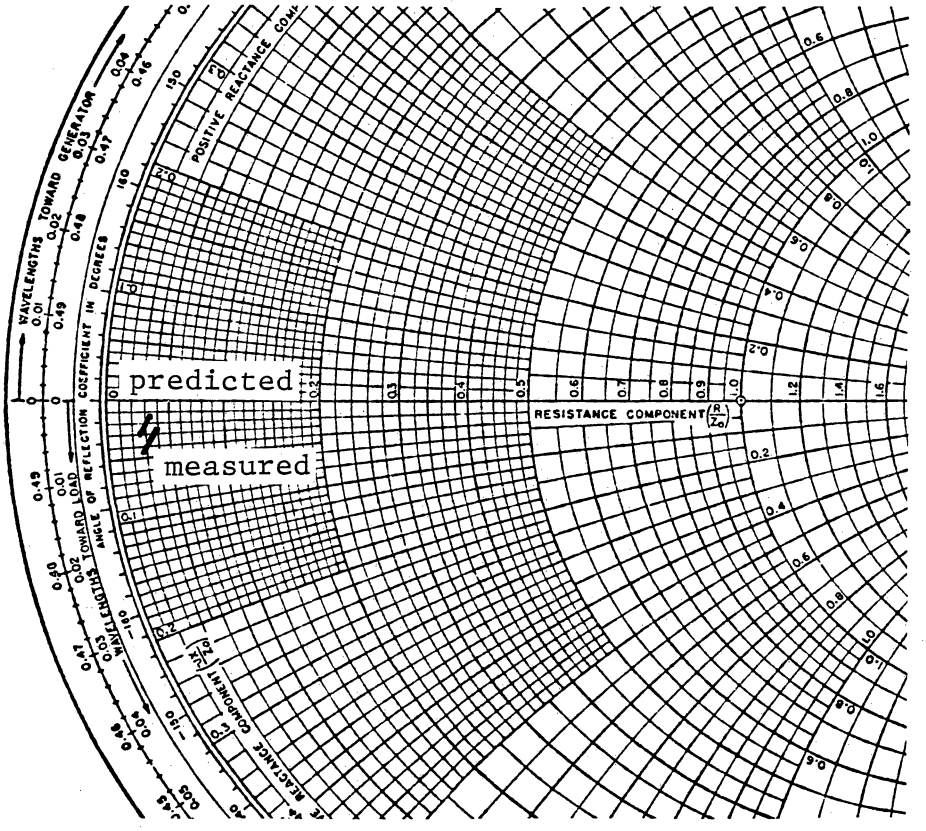

Figure 3.6 Predicted and measured values of input impedance. All values are normalized to 50Ω.

predicted values of input impedance are plotted on a Smith chart. (The impedance of the base bias network, which appears in parallel with the transistor input, is approximately 100 Ohms as determined from the measurements of Chapter 2. This is considered to be large compared to the transistor input impedance and is not included in the results. Bias networks will be discussed further in Chapter 4.) For reference, the measured values of input impedance (from Figure 2.7) are included in Figure 3.6. The upper point of each plot corresponds to the maximum drive level. The excellent agreement between prediction and measurement is apparent.

(One might be aware of the fact that UHF power transistors have inductive inputs. This is because of the series combination of lead inductance and the phenomenon of Equation 3.11. Again, the input impedance can be predicted by adding the lead inductive reactance to the results of the technique discussed above.)

A discussion on how the value for R_b was estimated is now in order. Direct measurement of R_b was found to be impossible, therefore the value of R_b at room temperature was chosen to force the measured and predicted input impedances to be as close as possible for the case of lowest drive level. The lowest drive level condition results in the transistor chip being essentially at room

temperature. Even though an approximate coincidence between prediction and measurement was forced, one should note that both real and imaginary parts of both measurement and prediction match closely at this point.

The temperature of the transistor chip is easily estimated for different drive level conditions. Each drive level results in a different value of collector current. Collector current is then used to compute power dissipation, which, along with a knowledge of the heat sink thermal resistance, allows computation of temperature. These estimates of temperature were taken along with published data on the temperature characteristics of bulk semiconductor material [Burton, 1969] to compute the value of R_b at different drive levels. These values for R_b were used in the computation of the predictions of Figure 3.6.

Even though an approximate coincidence between prediction and measurement was forced at the low drive point, please note that the variations with drive level of both measurement and prediction are nearly identical.

To conclude the discussion of input impedance, one must state that the predictions of Figure 3.6 include a moderate (25%) variation of transistor current gain, β, with temperature. Even though β does not explicitly appear in the differential equation of Equation 3.11, the transit time which does appear in this equation is directly

related to β.

Now turning attention to the output impedance of the transistor, Equation 3.12 can be put into a slightly different form by using the standard relationship between α and β. The result is

$$Zo = R_c + R_e + \frac{1}{\beta + 1} \quad \frac{1}{j\omega C_{CB}} \tag{3.15}$$

Now assuming a single pole roll-off for β,

$$\beta = \frac{\beta_o}{1 + j\beta_o f/f_T} \tag{3.16}$$

with the measured values of f_T = 450 MHz, R_c = 1.0 Ohm, and R_e = 0.05 Ohm, the output impedance can be predicted. In the results to follow, the effect of the collector bias network (Z = +j144 Ohms, measured during the experiment of Chapter 2) is included in parallel with Zo of Equation 3.15 (See one of Figures 4.1, 4.3, 4.4, 4.5, or 4.7). The effect of the bias network is included here because its impedance is only about ten times larger in magnitude than the Zo of Equation 3.15 and therefore its effect is considered significant.

The result of the computation yields a predicted impedance of 12.8 -j4.1 Ohms. Assuming that the circuit has properties of a linear network, the optimum load

impedance for maximum delivered power would be 12.8 +j4.1 Ohms. The results discussed earlier concerning the nearly class A operation of the device (a class A amplifier is linear), the essentially sinusoidal current waveforms, and the low harmonic content confirm the appropriateness of approximating the network as linear.

Recall that the measured value of optimum load impedance as presented in Chapter 2 is 12.0 +j4.0 Ohms. The predicted value of impedance and the measured value of impedance are extremely close.

As an experimental confirmation of the output impedance from Equation 3.15, the measurement setup of Chapter 2 was used to measure the reflection coefficient at port two of the transistor with no drive applied to port one. The DC biasing circuit was adjusted to give a quiescent collector current identical in value to the operating DC collector current for the amplifier with input drive. The reflection coefficient was then used to compute the output impedance. The result of this is Z = 11.8 -j5.6 Ohms. Exact correspondence was not expected because the transistor was not operating under a realistic set of conditions. Specifically, the internal current distribution for DC is different than that for AC, and the current gain α is dependent on this current distribution.

This measurement discussed above gives some insight

into a proper way to measure output-port S-parameters. One should make such S-parameter measurements under a condition of DC collector current equal to the value expected for the operating amplifier. However, there need be no drive to port one of the transistor.

In summary, the implication of the results presented in the preceeding five paragraphs is that indeed a conjugate match between the transistor output impedance (of a non-saturating device) and its load impedance is necessary in order to obtain maximum power. A conjugate match requires not only equal values of source and load resistances but also a resonance condition between source and load reactances. Again, emphasis should be placed upon the fact that even though this might seem to be a reasonable result, it is a result that is not widely known among users of RF power devices.

The forward transmission coefficient of an amplifier can also be predicted using the model. Figure 3.7 shows a representation of the amplifier with the optimum load. Knowing the load reflection coefficient, a relationship between the b_2 wave and the voltage V_c can be derived. Circuit analysis yields a relationship between the collector terminal voltage V_c and the transistor current source. Finally, the solution of the differential equation of Equation 3.11 yields a relationship between the

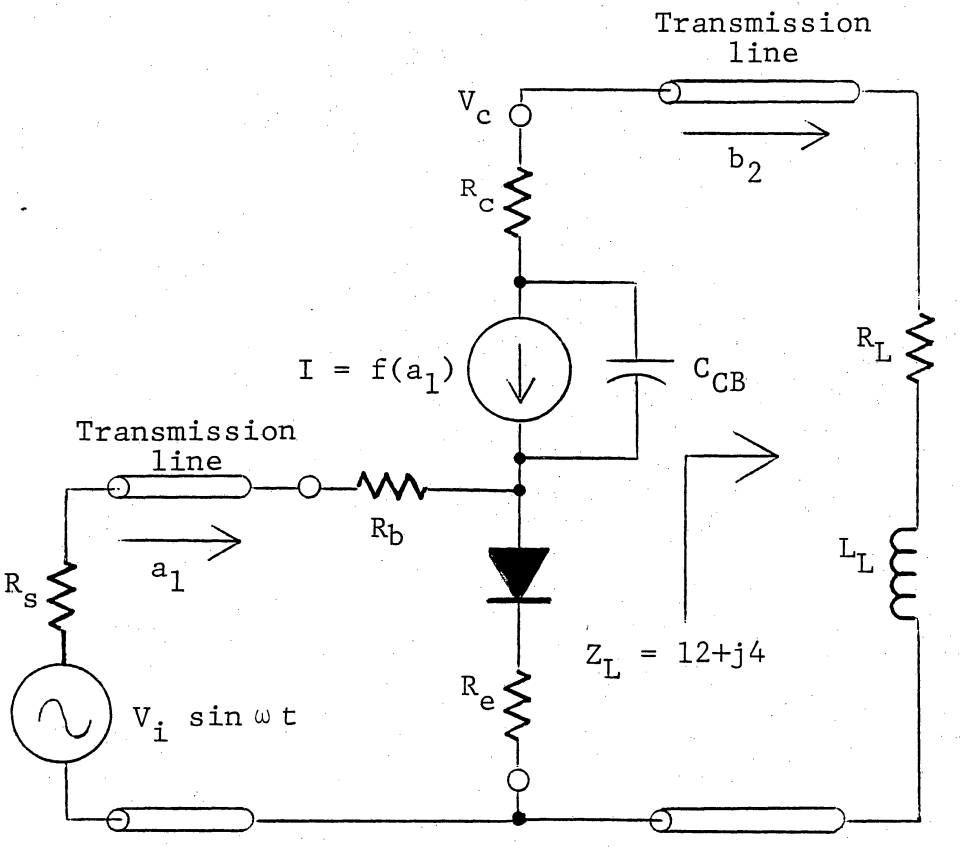

Figure 3.7 Circuit for the determination of transmission coefficient.

transistor current source and the input drive which is in turn proportional to the wave a_1. All of these taken together can be used to predict the relationship between b_2 and a_1, that is, the transmission coefficient.

Computations were done for the case of high drive level (just below saturation) and again for the case of low drive level (a factor of 30 smaller). The predicted transmission coefficient for the high drive level case is 3.1 at an angle of -278.5 degrees, that for the low drive condition predicts to be 2.65 at an angle of -276 degrees. Comparing these results to the measured results presented in Table 2.1 (3.25 at -278 degrees for high drive, and 2.3 at -272.4 degrees for low drive) is further justification for the model.

One more piece of information can be gleaned from the model by referring to the amplifier circuit of Figure 3.7. Even though a resonance condition is in effect in this circuit, from the point of view of the transistor model's current source a reactance is seen. For this circuit the impedance seen by the current source is 14.1 -j1.6 Ohms. The voltage appearing across the model's current source will not be of the proper phase to guarantee maximum efficiency. Maximum efficiency occurs when the AC components of the voltage and current are 180 degrees out of phase; such a situation guarantees the smallest

voltage-current product and therefore the smallest dissipated power.

3.4 Self Biasing, Comparison of Measurement and Theory

The self biasing mechanism seen to operate in the transistor causes operation which is essentially class A. To reiterate, this phenomenon is because of the charge storage mechanism present in the base region of the transistor. Experimental results which tend to directly confirm this are now presented.

Table 3.1 lists the measured values of DC collector current for various drive level conditions. These data are reproduced directly from Table 2.1. Additionally, Table 3.1 shows the measured values of peak AC collector voltage. These values of AC voltage were taken using a high frequency oscilloscope with an FET probe.

Figure 3.8 shows a family of 12.0 Ohm AC load lines for the transistor. (Here the effective load is assumed to be real.) Each load line corresponds to a different value of average or DC collector current. These average values are shown.

Selecting a case from Table 3.1 and finding the load line in Figure 3.8 with a corresponding average current one can see that the measured value of peak voltage swing indicates that the transistor goes into cutoff for a very

Table 3.1

Data Confirming Self-Biasing Phenomenon

Incident Power	Collector Current	Peak Voltage
0.014 W	63 mA	1.1 V
0.046 W	137 mA	2.3 V
0.140 W	281 mA	4.0 V
0.250 W	393 mA	6.0 V
0.460 W	554 mA	8.0 V

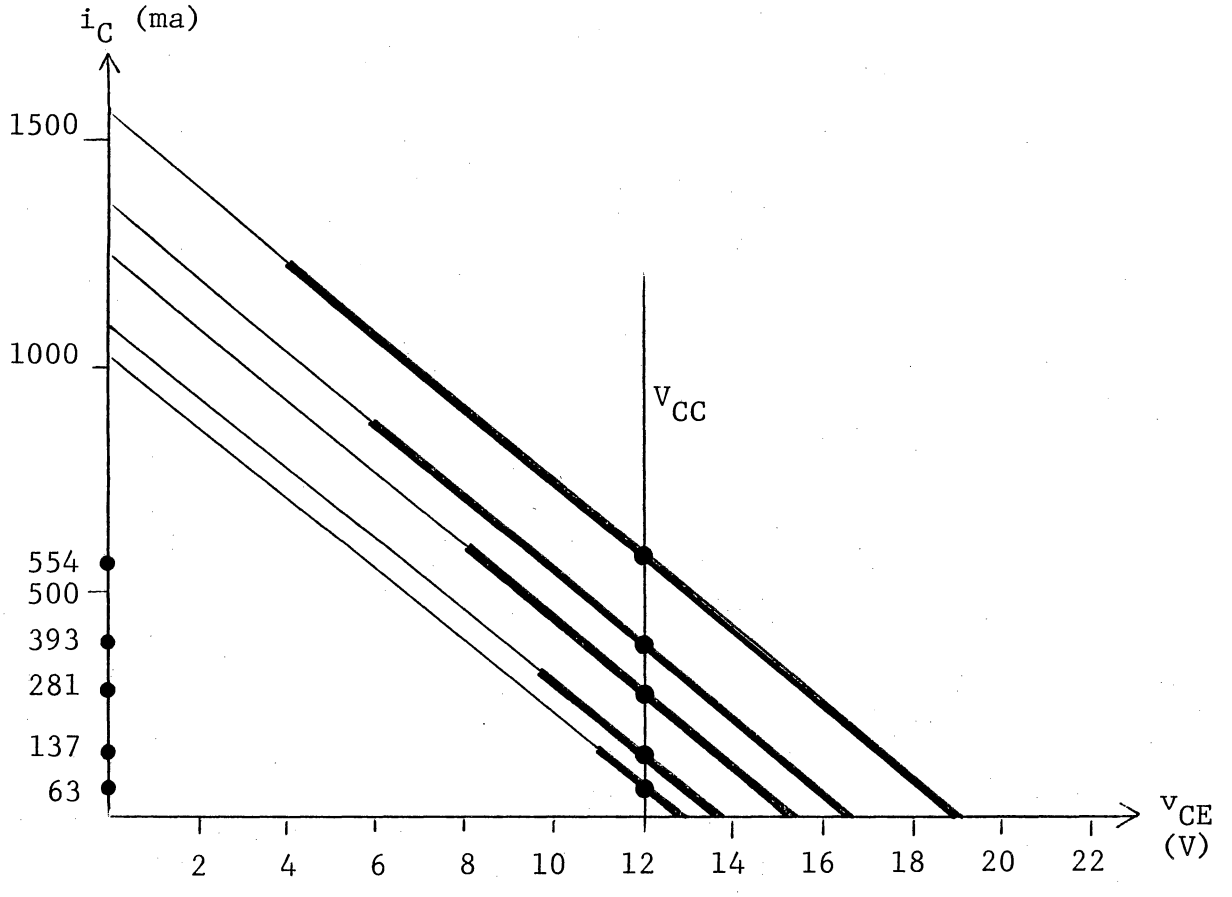

Figure 3.8 An illustration of the self biasing phenomenon.

small portion of the cycle. This corresponds to the small portion of the plot of collector current in Figure 3.3 where the current is zero. The fact that the period of cutoff (as determined from the load line) is so small is a confirmation of the nearly class A operation of the transistor, and also a confirmation of the self biasing effect.

Finally, as a point of interest, the load lines of Figure 3.8 illustrate a useful characterisitic of this type of power amplifier. The effective quiescent point (Q-point) automatically adjusts itself to allow class A operation for different drive levels. For example, if the signal level is increased, the Q-point will automatically move upward. Not only does this phenomenon allow for collector current flow over nearly a full cycle, but under less than full drive conditions it results in an amplifier which has a higher efficiency than an externally biased class A amplifier.

3.5 A Comment On Saturating Amplifiers

The case of the saturating amplifier is probably the most important situation not heretofore covered in this report. On the other hand, the previous work can be extended to yield approximate results for saturating amplifiers. This statement is substantiated in part by

observations made in the laboratory.

Figure 3.9 is a Smith chart representation of the measured input impedance of the test amplifier as a function of drive level. The lower portion of the curve duplicates the data which were presented in Figure 2.7 (transistor restricted to active mode operation). The point on the curve of Figure 3.9 where the data diverges from a straight line corresponds to the onset of saturation. Above this deflection point the transistor is well into saturation. The drive level at the uppermost point on the plot is approximately a factor of ten greater than that required to initiate saturation.

Again, one can see that even in saturation the variation in input impedance is minimal. The now forward biased base-collector junction and its associated current flow have little effect upon the input impedance. This is so because the voltage at the internal base node of the transistor (see Figure 3.2) is proportional to the logarithm of current. In other words, this voltage and its effect on the input impedance of the transistor is only a mild function of any currents flowing from the collector. (In a loose sense this is the same as saying that the impedance of the base emitter diode is small enough to be considered that of a short circuit. This would place the internal node at AC ground potential and would isolate the

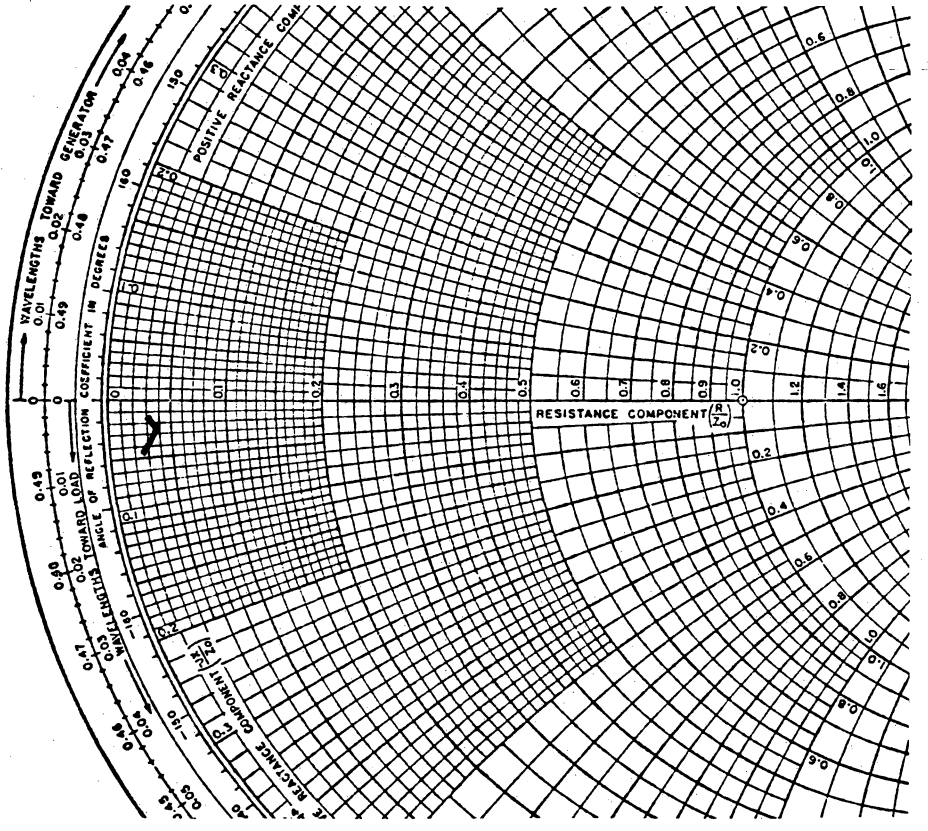

Figure 3.9 Input impedance. The upper portion of data corresponds to the case of transistor saturation. All values normalized to 50Ω.

collector junction from the the transistor input. As a side aspect, note that this also would isolate the input from any load variations.) The implication of all of this is that only a small error will be incurred if the input impedance prediction method of previous sections is applied to a saturating amplifier.

Now considering the output portion of a saturating amplifier, a review of the manufacturer's data sheet for the transistor used in this experiment indicates that under a saturation condition the recommended load impedance is 7.0 + j4.25 Ohms. Note that the imaginary part is virtually identical to the prediction for a non-saturating amplifier, but the real part is considerably smaller. In this case the actual output impedance of the transistor is formed by the parallel combination of the active mode output impedance (the same as before) and the resistance of the now forward biased collector-base junction.

The collector-base junction is forward biased over a small portion of the signal period and its effect can be viewed as periodically switching a finite resistance across the transistor output. In order to predict an effective value of resistance one would have to know further information about the characteristics of the collector-base junction, and one would have to know the switching duty cycle.

Further work could be done in this area, but one must keep in mind from the outset that the conjugate match properties of a linear system come into question when applied to a saturating amplifier which is inherently nonlinear.

3.6 Summary

In this chapter a transistor model was developed. This model is simple and accurate in predicting the radio frequency characteristics of a VHF power transistor. Agreement between all measured phenomena and model predictions was shown. Additionally, insight into many other aspects of high frequency transistor operation was gained.

The model along with some basic low frequency measurements comprise the bulk of a valid design approach which can be applied to radio frequency power amplifiers. Any difficulty posed by not knowing an accurate value for the base resistance R_b can be overcome easily in the laboratory. Obtaining the input impedance of a transistor by direct measurement would be a simple matter. Such a measurement will yield accurate results once the predicted optimum load is connected to the transistor collector.

The practical aspects of amplifier design will be discussed in the next chapter.

CHAPTER 4

Practical Considerations

The total design process for a radio frequency power amplifier would begin with the determination of the optimum values for the source and load impedances to be presented to the transistor. The results of the preceeding chapter indicate a method for predicting the input and output impedances of a VHF power BJT. Justification has been given in the previous chapter for approximating a VHF power bipolar transistor as a linear system. Therefore the maximum power transfer theorem holds and the optimum source and load impedances would be the complex conjugates of the transistor input and output impedances.

The terms used in the literature (and also in the immediately preceeding discussion) relating to the input portion of the amplifier are somewhat misleading. In reality, given a device with known input impedance the maximum power transfer theorem does not apply to the selection of the optimum source impedance. The optimum source impedance for maximum power transfer would be zero. In the case of the amplifier, though, one is actually working with a fixed source impedance. By forcing a complex conjugate match at the input terminals of the

transistor one is really adjusting the "load" impedance (load in this case refers to the transistor input terminal) through a transformer network to be the conjugate of the fixed source impedance.

The prediction approach of Chapter 3 depends upon knowing certain physical parameters of the transistor. Determination of the paramaters needed to predict the output impedance poses no difficulty. Determination of the base ohmic resistance needed to predict the input impedance might present some difficulty, though. As discussed in Section 3.6, a direct measurement of this impedance is a legitimate means of circumventing the problem.

Once the optimum source and load impedances for the transistor are known, design proceeds by first determining a network to provide bias voltages and currents to the transistor. Finally one would select and then design matching networks to transform typically 50 Ohm terminations into the desired source and load impedances.

Figure 4.1 shows the arrangement of the transistor, the bias networks, and the matching networks for a common emitter amplifier. The emitter lead of the transistor is directly grounded. No DC bias stabilization resistance is present in series with the emitter lead because of the difficulty of adequately bypassing such an element at very high frequencies. Also, such bias stabilization is

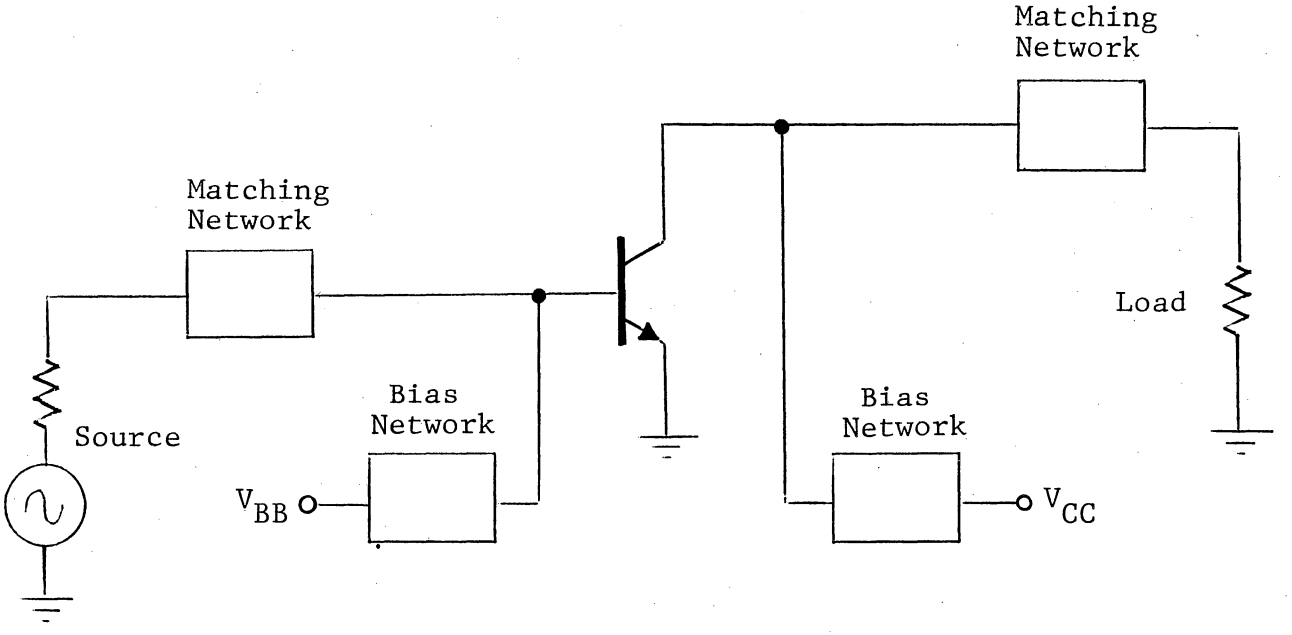

Figure 4.1 Basic common emitter power amplifier.

inappropriate for any amplifier where the DC current varies with applied drive level.

The bias networks are represented in Figure 4.1 by blocks. The major function of the bias networks is to isolate the DC and the AC portions of the circuit. In other words, the bias networks prevent AC signals from entering the DC supplies. This is important for three reasons. First, because the AC impedances of the supplies are unknown their effect on the circuit cannot be predicted. Second, if the base and collector supply are derived from the same source, any AC path to the DC supply provides a feedback mechanism and the potential of oscillation. Third, if more than one amplifier is powered from the same source, any AC path through the bias networks provides undesirable interaction between the amplifiers. The function of the bias networks in preventing these problems is called "decoupling."

The matching networks, shown as blocks in Figure 4.1, provide two functions. They act as impedance transformers to change given terminating impedances into the optimum source and load impedances for the transistor. They also provide a means to limit the frequency response of the amplifier, that is, to set the amplifier bandwidth.

Circuit topologies and design techniques for matching networks are well developed. A discussion of the basic

network types which are suited for use with low impedance BJT's will be given in Section 4.3. The choice of topologies and element values for bias networks will be presented in Section 4.2.

The bias network has an important influence on the stability (freedom from oscillation) of the amplifier, not only because of the decoupling function of the networks, but also because of parasitic resonant circuits which are often inherent in bias networks. The matching networks can also impact the stability of an amplifier because of parasitic resonances. Before any of these effects can be adequately discussed, and therefore before bias and matching network design can be addressed, the topic of stability must be investigated.

4.1 Stability

The term "stability" as used here refers to the lack of circuit oscillation. There are a number of mechanisms of RF amplifier instability; many of these are nicely summarized by Muller [1967]. The important mechanisms will be discussed in this report. Fortunately most of the different causes of instability can be cured by the same treatment.

The unstable region of Figure 3.1 indicates that there is inherent within a transistor a sufficient amount of

feedback to cause oscillation if certain other conditions are met. Therefore, this region should actually be termed a region of "potential instability." The major additional condition which is required to actually create an oscillation is to have a circuit which is resonant somewhere within the range of potential instability. The resonant matching networks will have their primary resonance at the amplifier's operating frequency, and, as discussed in Chapter 3, this frequency will be well above the unstable region. On the other hand, the possibility exists that the matching networks as well as the bias networks will have parasitic resonances within the unstable region. In order to avoid oscillations one must prevent such undesired resonances, both parallel and series. If such resonances are unavoidable, resistively loading the circuit is often sufficient to prevent oscillation. Specific examples will be given in the following sections.

The potentially unstable region of Figure 3.1 represents the effect of feedback only within the transistor. A potentially unstable situation may be created by introducing feedback through the circuit outside of the transistor. Poor circuit layout and inadequate decoupling are the major culprits here. Circuit layout should be such as to prevent magnetic field or electric field coupling between excessively long element leads, and

to prevent magnetic coupling between the inductors of the resonant matching networks. Decoupling at the operating frequency should be substantial. (Particular attention must be paid to decoupling at the operating frequency because input and output resonances are indeed present at this frequency; poor decoupling at this frequency almost always will lead to oscillation.)

There is a danger in designing a bias network to provide adequate decoupling at the operating frequency while neglecting to provide decoupling at other frequencies. Decoupling at VLF and audio frequencies is also especially crucial. The reason for this is because the gain of an RF transistor is typically very high at low frequencies. This can be seen by referring to the plot of gain in Figure 3.1. Instabilities at these low frequencies are often the result of relaxation types of oscillations. Resonant networks are not necessary in this case. Specific examples of both operating frequency and low frequency decoupling will be given.

An interesting type of instability often noted in RF power amplifiers is a subharmonic oscillation. This phenomenon was actually observed in the amplifier used to make the measurements of Chapter 2. (Obviously, the problem was cured before valid data were taken.) There are several potential explanations for the phenomenon, but the

circuit cure in all cases is the same; avoid or load down parasitic resonances.

One of the causes of an oscillation at one-half of the operating frequency (the case observed above) is illustrated in Figure 4.2. A transistor with even a mild nonlinearity is separated into a linear element and a nonlinear element. The effect of the nonlinear element is to provide for the heterodyning, or mixing, of two frequencies. The input frequency to the amplifier is ω; if a signal (initiated by noise) at the frequency $\omega/2$ is fed-back then the difference frequency leaving the mixing circuit will be $\omega/2$. One can see that a feedback loop at this half-frequency is created [Ahamed, 1976]. Often in a practical amplifier parasitic circuit resonances aggravate the feedback path around the amplifier. This illustrates that elimination of such parasitic resonances typically will cure the problem.

One easily can show that another source of subharmonic oscillation is the parametric negative resistance effect of a voltage-variable capacitor [Hilibrand, 1959]. The reverse biased collector-base junction capacitance of a BJT provides this.

The expression for the transition capacitance of a reverse biased PN junction is of the form

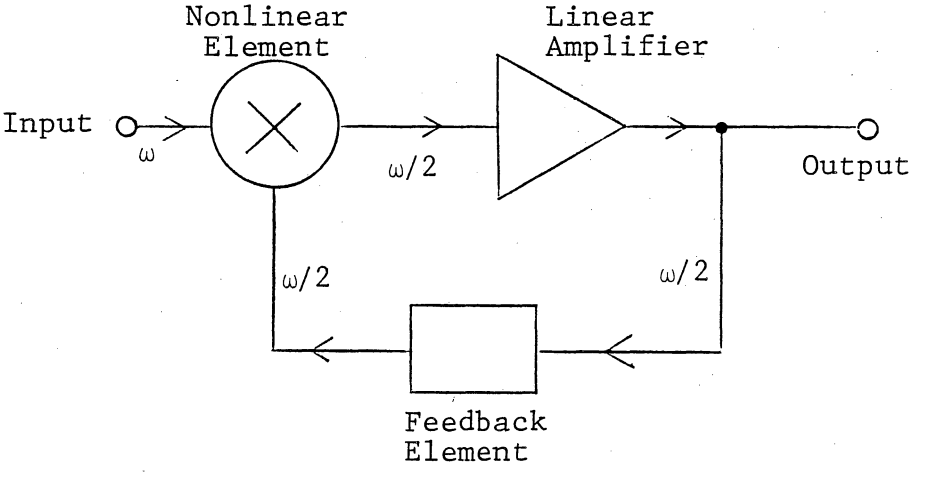

Figure 4.2 A half-frequency feedback loop.

$$C(v) = \frac{C_o}{n\sqrt{V_o + v}} \tag{4.1}$$

This can be expanded in a Taylor series in the voltage v.

$$C(v) = a_o + a_1 v + a_2 v^2 + a_3 v^3 + \ldots\ldots \tag{4.2}$$

The current flow through the capacitance is given by

$$i = C(v) \frac{dv}{dt} \tag{4.3}$$

The capacitance does not appear inside the time derivative operation because the PN junction transition capacitance is itself defined as the derivative of charge with respect to voltage.

Now analysis continues by applying a voltage of the following form to the capacitor,

$$v = V_p \cos \omega t + V_s \cos \left(\frac{\omega}{2} t + \phi\right) \tag{4.4}$$

where the "desired" frequency is ω, and the signal at frequency $\omega/2$ would represent noise. The result of the analysis yields a current with several important components. As expected, there are current components at frequencies ω and $\omega/2$ which lead the applied voltages by 90

degrees. There is also a component of current at frequency $\omega/2$ which is 180 degrees out of phase with the applied voltage. This represents a negative resistance. Such negative resistance is the principle upon which the parametric amplifier operates. In the case at hand, though, this negative resistance when coupled to a parasitic resonant network can give rise to oscillation at half the frequency of the desired signal.

Again the cure for such a problem is obvious; eliminate the parasitic resonances. If doing this is not possible, loading the resonance with enough positive resistance to cancel the effect of the negative resistance would be sufficient.

4.2 The Bias Network

Figure 4.3 shows a basic bias network for a transistor. The radio frequecny chokes (RFC's) should provide high series impedances at the signal frequency, and the capacitors C_1 and C_2 should provide low impedance paths to ground at the signal frequency.

Guidelines presented in the literature specify that RFC_2 should provide an impedance of five to ten times the value of load resistance presented by the output matching network. Obviously, having this choke present a large impedance at the signal frequency in order to prevent loss

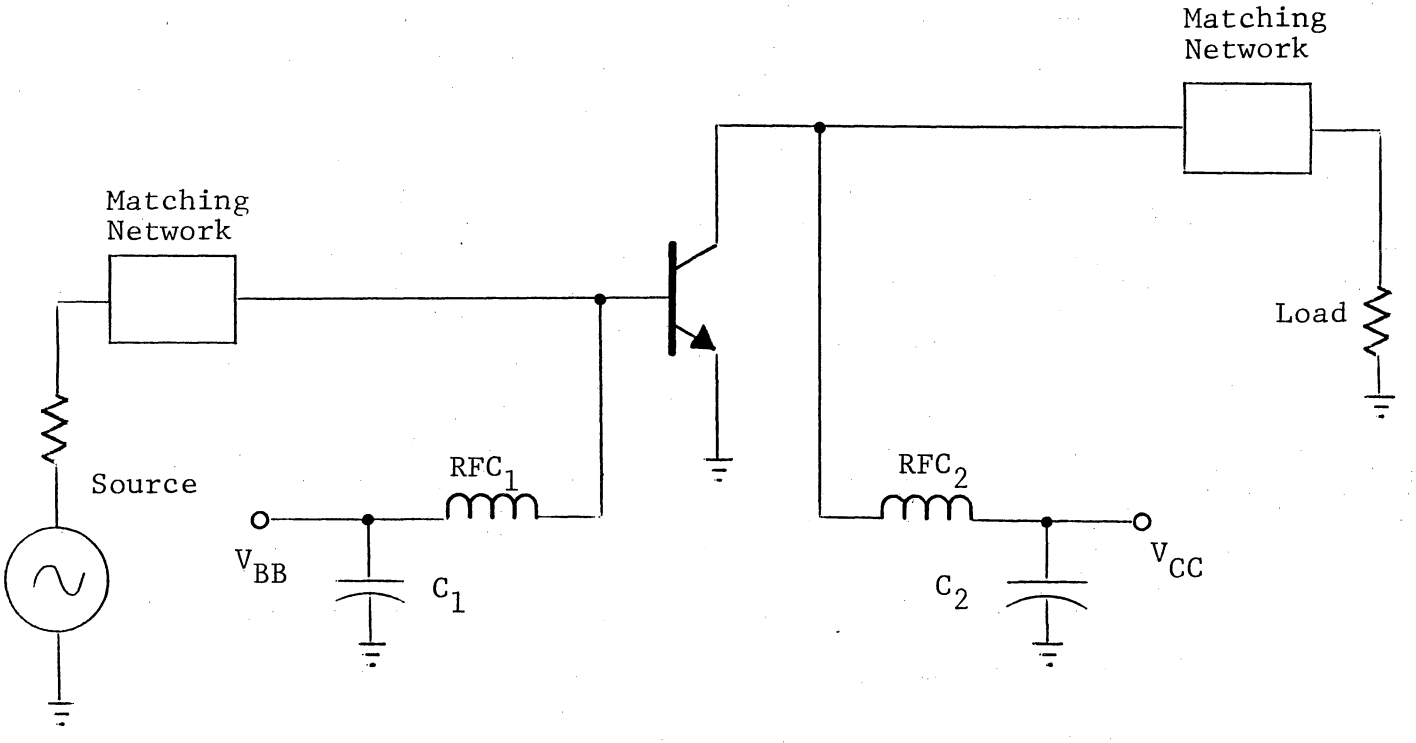

Figure 4.3 A bias network providing decoupling at operating frequency.

of load current is desirable. But one must realize that there is inter-winding capacitance in such an RFC, and if an attempt is made to make the choke too large in inductance, then this capacitance will destroy the choke's effectiveness. Similar statements can be made for the base choke, RFC_1; its impedance should be on the order of five to ten times the magnitude of transistor input impedance. In the test amplifier constructed for measurements, the initially chosen values of the chokes were: RFC_1 = .04 μH (45 Ohms), and RFC_2 = .115 μH (130 Ohms).

The capacitors have an associated parasitic series inductance. In choosing these capacitors this inductance must be considered. The ideal situation would be to have these capacitors nearly series resonant at the signal frequency. The values of C_1 and C_2 used in the test amplifier are 110 pF.

Many designers specify that the base RFC should be lossy (have a low Q) [Hayward, 1977; DeMaw, 1984]. This can be accomplished either by shunting the choke with a resistor, or by replacing the choke with a lossy ferrite bead threaded onto a piece of wire. The reason given for specifying a lossy choke is to enhance stability by loading down any resonances. Indeed, the test circuit constructed with the elements listed above did exhibit a self oscillation which was cured by replacing RFC_1 with a

ferrite bead having a nearly real impedance of 140 Ohms.

There are several possible explanations for the initial oscillation and the cure. It is possible for the orininal .04 μH choke to form a parallel resonance with the transistor input capacitance. This computes to be approximately 85 MHz, a frequency on the order of that which was observed in the laboratory. A similar resonance effect on the output of the transistor could form a tuned-input-tuned-output oscillator. Another possible explanation for the oscillation is that the base choke and the 110 pF capacitor form a series resonance at about 75 Mhz. Such a series resonance could provide a path for current feedback. Finally, another possibility is a resonance in the loop alternately from the collector, through RFC_2, the 110 pF capacitor, "ground", the base 110 pF capacitor, RFC_1, then to the base. This is a resonant circuit appearing across the collector-base voltage variable capacitor and its associated negative resistance. The resonant frequency computes to be on the order of half of the signal frequency.

(The term "ground" is placed in quotes above because circuit parasitic reactances will prevent this node from actually being at true ground potential. Therefore the ground node can be part of a feedback path.)

The cure for the instability discussed above was to

replace the base RFC with a lossy ferrite bead. This had the effect of eliminating the resonance. Replacing the collector RFC with a lossy element would be undesirable. This is so because such a lossy element would rob output power from the load. This is the case in spite of any potential resonances associated with this choke.

The circuit presented in Figure 4.3 does not provide adequate decoupling at low frequencies. At such frequencies the chokes will appear as short circuits, and the capacitors will appear as open circuits. Additional decoupling networks as shown in Figure 4.4 need to be added. RFC_3 and RFC_4 should have large impedances at low frequencies, and capacitors C_3 and C_4 should have small impedances at low frequencies. These requirements are difficult to attain because the "low frequency" range spans many decades. The problem can be alleviated by placing several different values of capacitors in parallel to form C_3 and C_4. Large values of capacitance will provide low impedances at low frequencies, and medium values of capacitance will be effective at the upper end of the low frequency range. There is some danger in paralleling capacitors, though. For example, the inductance associated with large values of capacitors can form resonant circuits with the smaller capacitors. In the case of the test amplifier, capacitors C_3 and C_4 were each formed by the

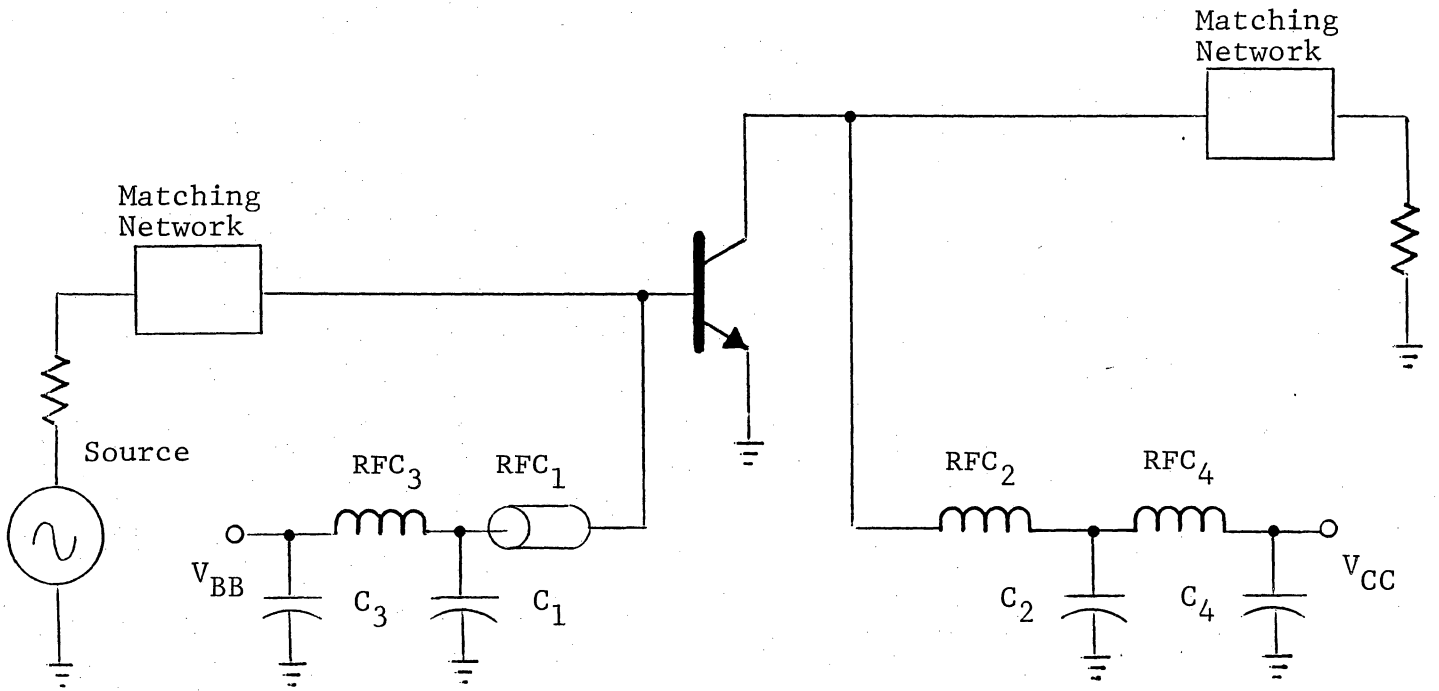

Figure 4.4 Low frequency decoupling.

parallel combination of 3300 pF and 10 μF capacitors.

Another potential problem exists with the circuit as it is presented in Figure 4.4. Capacitances C_3 and C_4 will be almost short circuits at low frequencies, C_1 and C_2 will be nearly open, and the chokes RFC_1 and RFC_2 will be almost short circuits. There exists a potential low frequency parallel resonance between RFC_3, C_1, and the transistor input capacitance. A similar potential exists on the output portion of the circuit. In order to alleviate the problem associated with these resonances, the two chokes RFC_3 and RFC_4 should be made lossy. Ferrite beads are ideal in this case because not only are they lossy, but their frequency characteristics are more broadbanded allowing them to be effective as chokes over a large range of low frequencies.

For completeness, the final configuration of the bias network for the test amplifier is shown in Figure 4.5. Also shown in this figure is the circuit used to derive the base bias voltage.

In order to bias the transistor with a quiescent current (10 milliamperes in the case of the test amplifier) it is necessary to provide a voltage of approximately 0.7 Volt to the base terminal. The value of this voltage is critical because of the exponential DC current versus DC voltage characterisitc of a bipolar transistor. The

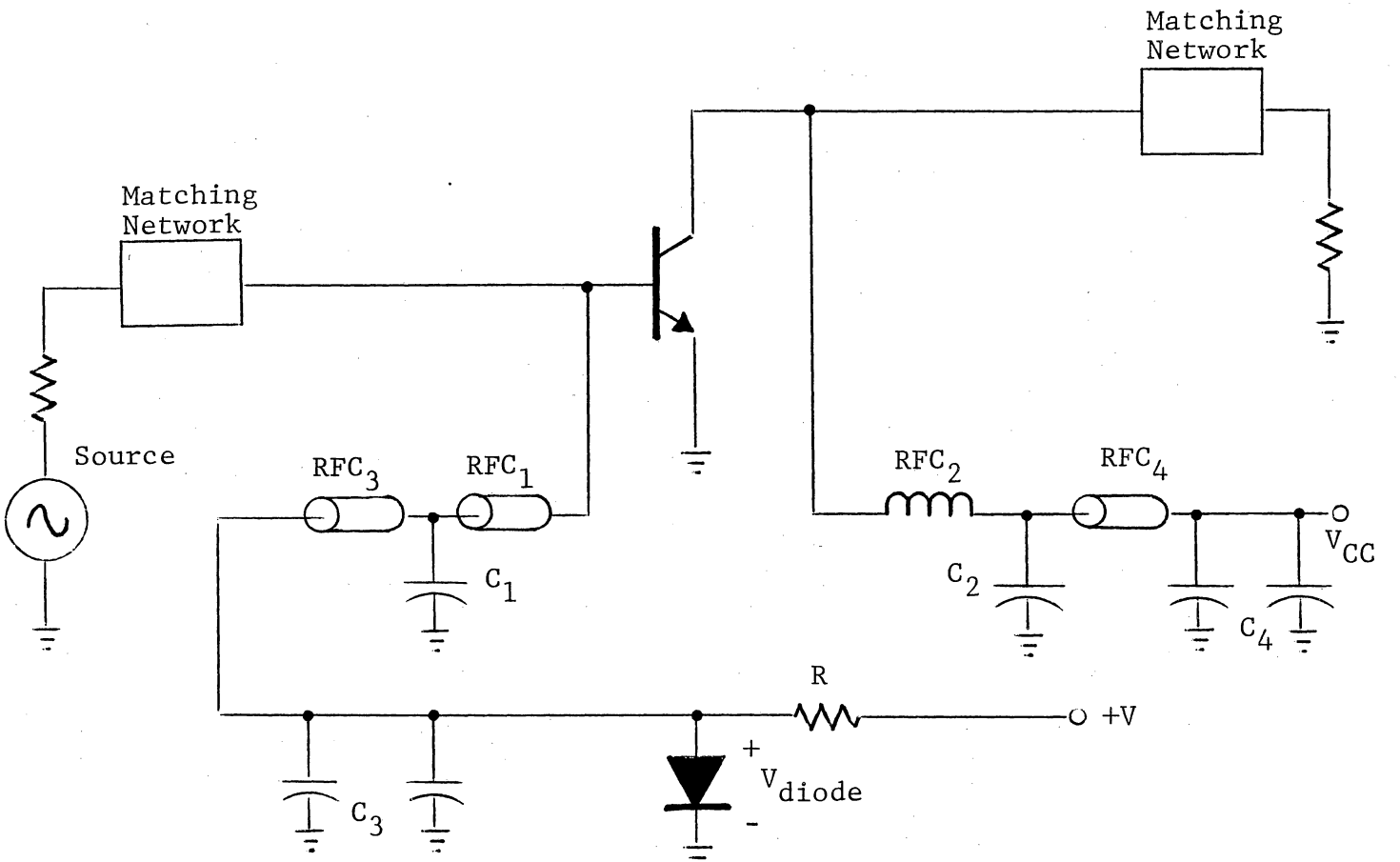

Figure 4.5 A power amplifier bias network.

exponential characterisitc is strongly temperature dependent, therefore some form of temperature tracking for the base voltage is necessary. In the case of the test amplifier this was accomplished by deriving the base voltage from the drop across a silicon diode. This diode was physically coupled to the transistor through the heatsink in order to provide for nearly equal temperatures.

Other possibilites for deriving the base bias voltage are to use various forms of voltage regulator circuits. The most convenient of these is the monolithic integrated circuit regulator. In all cases some form of temperature compensation should be included.

4.3 Matching Networks

Design procedures for LC matching (impedance transformation) networks are presented in almost any good radio engineering text; such material will not be duplicated here. Topics particular to the RF power amplifier will be presented in this report, though.

The input and output impedanecs of power BJT's are typically small. Terminating impedances for amplifier circuits are typically on the order of 50 Ohms. Therefore similar types of matching networks can be used on both the input and output of an amplifier. In the discussion to follow, no distinction will be made between the input and

output network until the very end of the discussion where differences between the two will be presented.

The complexity of matching networks is usually dependent upon bandwidth requirements, broadband amplifiers require multi-section networks. Again, the theory for such networks is well developed and will not be repeated here. Basic single-section and dual-section networks will be discussed. A single section network would be an "L" network (series inductor, shunt capacitor), and a dual section network might be of a "T" or a "PI" configuration.

The "PI" type of impedance transformation network can be viewed as a back-to-back combination of two "L" networks (thus the classification of dual-section) where the intermediate impedance is smaller than either of the terminal impedances. Because of the low transistor impedance, the resulting very low intermediate impedance makes the "PI" configuration unsuitable for use with RF power amplifiers.

The fact that harmonic levels are small in VHF amplifiers using transistors operated well above their 3 dB corner frequencies has already been shown in this report. Such harmonic levels were measured on the test amplifier to be on the order of 25 dB below the fundamental. Federal regulations for radio transmitters specify harmonic outputs to be in excess of 60 dB below the fundamantal in order to

prevent potentially serious interference to sensitive receivers. Often filters are placed externally to a power amplifier in order to attain the requisite harmonic rejection, but one can still see that the use of impedance matching networks having low-pass characterisitcs would be of benefit. Networks with series inductors and shunt capacitors are low-pass in nature.

Taking all of these things into consideration, the two forms of impedance matching networks shown in Figure 4.6 are appropriate for VHF power amplifiers. The "L" network is simple and easy to design, but one has no control over its bandwidth. The "T" network is somewhat more flexible and will be easier to adjust in the laboratory because of the two variable capacitors.

Sometimes the "L" network is modified by placing a capacitor in series with the inductor. This provides for easier adjustment because of the additional tuning element. Also, the Q (quality factor) and resulting bandwidth of the network can now be selected. Another reason for adding this series capacitor is to enhance the physical realizibility of the otherwise typically very small inductance. With the series capacitor, the value of the inductor will be larger than without.

Also shown in Figure 4.6 is the two-"L" approximation of the "T" network. For low and moderate Q networks, the

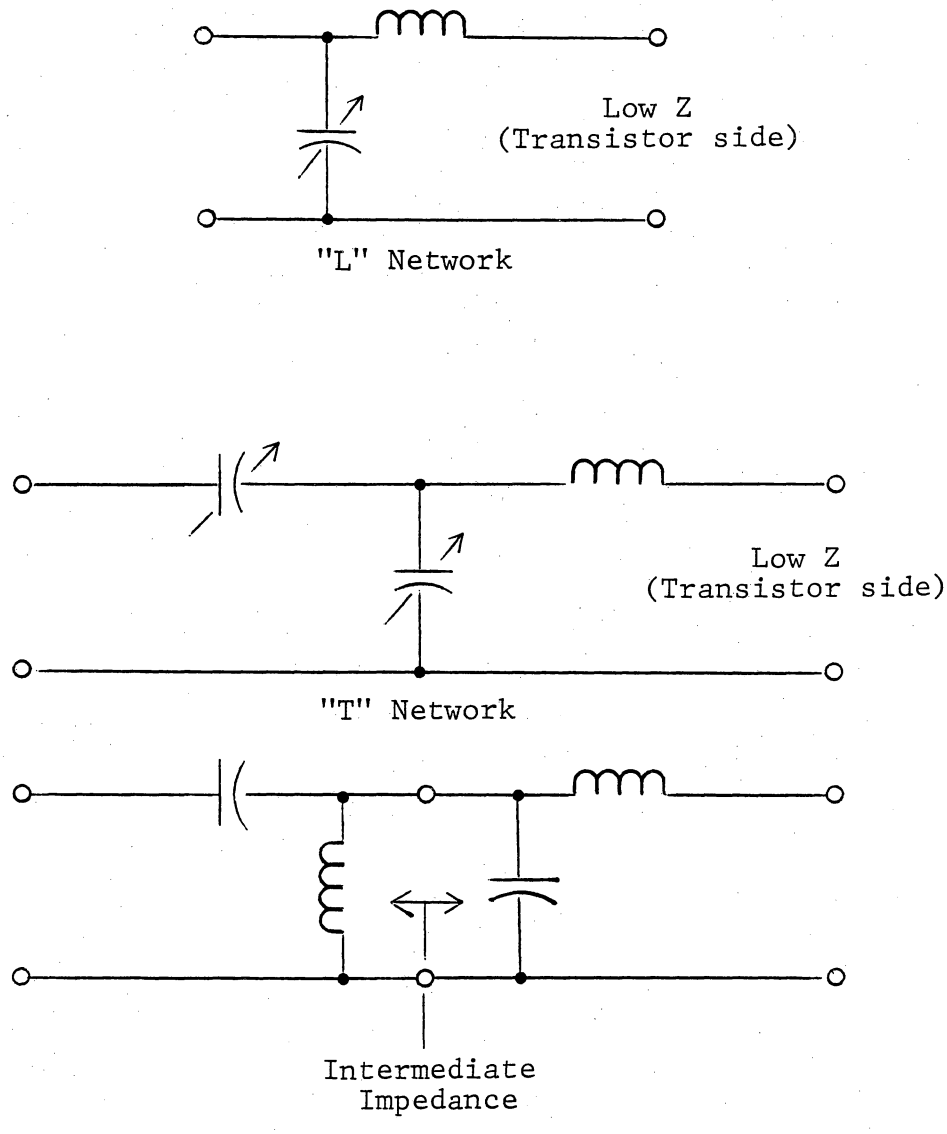

Figure 4.6 Matching networks appropriate for RF power amplifiers.

major impedance transformation in a typical circuit takes place in the right-hand "L" network. This implies that element values in the "T" network will be close to those found for the "L" network elements. Therefore there appears to be no advantage in terms of practical realizibility of one network over the other. Additionally, there probably will be only a marginal difference in performance between the two networks.

An ultimately practical advantage to the "T" network and to the "L" network with a series capacitor-inductor combination is that no DC blocking capacitor is needed to isolate the source or load from bias voltages. Such blocking is inherent in the series capacitors of the matching networks. On the other hand, these series capacitors typically will be very small in value. At low frequencies these capacitors will be nearly open circuits. This will aggravate instability problems at low frequencies because the resulting high impedances will not provide for loading of any parasitic resonances which might be present. Additionally, any small feedback currents will result in high voltages across such high impedances, again aggravating such feedback.

If a standard "L" network (or any network which requires DC blocking capacitors) is used, care must be exercised in the choice of these capacitors because of the

large currents which flow in high power, low impedance circuits [Glenn, 1985].

The differences between input and output networks are twofold. First, and obviously, the size and power handling capability of components at the output side must be larger. Second, some designers specify a capacitor to be placed directly from the base terminal to ground [Bailey, 1970; DeMaw, 1984]. The purpose of this capacitor is to provide a path for harmonic currents to flow. Even though the magnitudes of such currents are small in a transistor of the type discussed in this report, without the shunt capacitor undesirably large voltages can be developed across the series inductor of the input matching network. Such large voltages could even lead to emitter-base breakdown. Harmonic currents at the transistor output have a path through the output capacitance of the transistor. Occasionally, though, one sees a circuit where a shunt output capacitor has been included.

Placing a shunt capacitor across the input of a transistor makes the design of the input matching network more difficult. The real part of a power bipolar transistor's input impedance is small. The shunt capacitor has the effect of transforming this to an even smaller value, thus placing more severe constraints on the matching network. This author recommends avoiding the shunt input

capacitor if possible.

4.4 A Design Implementation

In order to provide a final confirmation of the measurements of Chapter 2, the predictions of Chapter 3, and the practical aspects of this chapter, a tuned power amplifier was designed and constructed. The bias network was already in place, therefore the completion of the amplifier involved only the design of the input and output matching networks.

The input and output matching networks were designed to transform the 50 Ohm impedances of laboratory measurement instruments into the required transistor terminating impedances, 12.0 +j4.0 Ohms for the collector, and 1.77 +j1.15 Ohms for the base. These values are derived from the measured quantities of Chapter 2, but are essentially identical to the predicted quantities of Chapter 3.

The "L" type of matching networks were chosen for both the input and output of the amplifier. These were chosen because of their simplicity and because the "L" network is the most broadbanded of the simple network types. This latter aspect makes tuning easier. The inductors of the matching networks were realized using sections of transmission lines. The capacitors of the matching

networks were variable ceramic capacitors. Leadless ceramic "chip" capacitors were used for input and output coupling capacitors. The complete diagram of the power amplifier is shown in Figure 4.7.

The variable capacitors of the matching networks were pre-set to the required values in the laboratory. Upon application of a signal to the power amplifier, only a very minor adjustment of these variable elements was necessary in order to achieve maximum power from the amplifier. This fact represents a confirmation of the design technique.

Performance measurements are tabulated in Table 4.1. The tabulated input reflection coefficient is somewhat in error because it includes the effect of harmonics. Harmonics cause a significant error in the case where the fundamental reflection is small, that is, when the reflection coefficient is small. The spectrum of the wave reflected from the amplifier input showed a fundamental voltage of approximately 0.04 times the incident wave voltage.

The output power of the amplifier and the amplifier's efficiency are somewhat less than those measured in Chapter 2, where transistor characterization measurements were taken (3.0 Watts output, 45% efficiency). The principal reason for this is because of loss in the matching networks. Presumably, the greatest source of loss is in

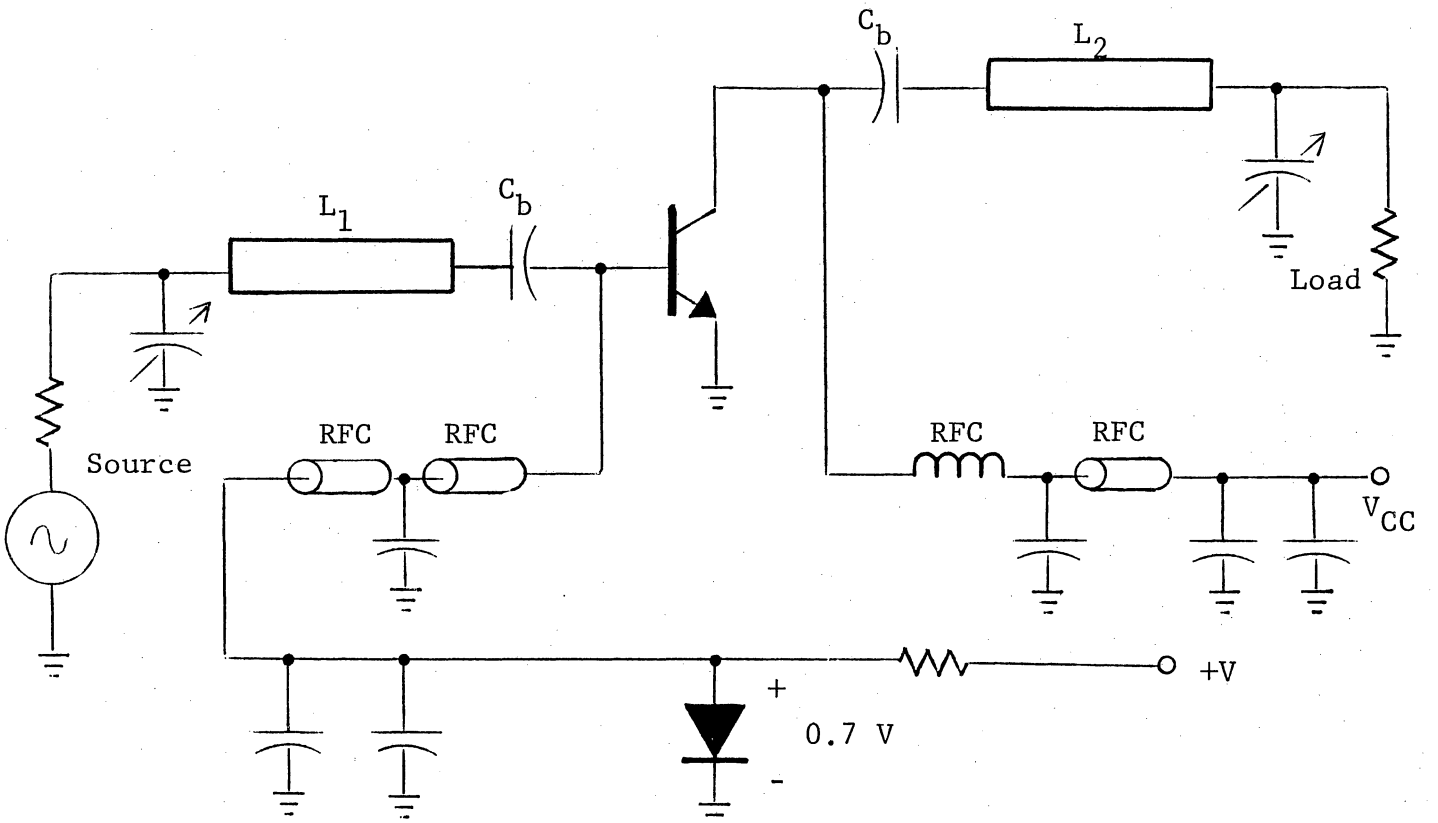

Figure 4.7 A practical RF power amplifier.

Table 4.1

Performance Characteristics of Operating Power Amplifier

Input Impedance	52.7 -j6.3	Ohms
Input Reflection Coefficient	0.067 $\angle -63^\circ$	
Input Power	0.084	Watt
Output Power	2.27	Watts
Power Gain	14	dB
DC Collector Current	527	mA
Efficiency	36	%
2nd Harmonic Output	-34	dB
3rd Harmonic Output	-33	dB
4th Harmonic Output	-34	dB
5th Harmonic Output	-38	dB

the ceramic variable capacitors; the output capacitor became hot to the touch. One would suppose that nearly 3 Watts could be obtained from this amplifier if low loss components were available.

One might note the 3 Watt power output and ask the question: why is this value so small compared to the 10 Watt rating given by the manufacturer? The answer is that there is a fundamental limitation on the output capability of a transistor if non-saturation operation is to be maintained. (The 10 Watt rating is under saturation conditions.) Two factors come into play here. First, the load for maximum power is fixed by conjugate match considerations, and second, saturation and breakdown limit the maximum load voltage swing. In the case of the amplifier being discussed, substantially greater power output was obtained by driving the transistor into saturation.

Finally, the spectrum of the amplifier output confirms the low harmonic content of the transistor output, and it also confirms the low-pass filter characterisitc of the "L" network. All harmonics are in excess of 33 dB below the fundamental signal.

In conclusion, one can see that the resulting amplifier performs quite well. The amplifier tunes smoothly, and it is stable.

4.4 Summary

Practical considerations of circuit stability, choice of bias network elements, and choice of matching network topology have been discussed in this chapter. One very practical consideration which was not discussed is circuit board layout. The reader is referred to DeMaw [1984] who nicely summarizes guidelines for such layout.

CHAPTER 5

Conclusion

5.1 Summary of Work Completed

Work completed in the course of this project includes the development of measurement, modeling, and design techniques for VHF power amplifiers using bipolar junction transistors. This was done in fulfillment of the proposal presented in Chapter 1 of this dissertation.

First, a measurement procedure was developed. The measurement procedure is uniquely suited for RF power amplifiers in that it provides information which is directly related to the important characteristics of power amplifiers. These characteristics are gain, power output, efficiency, input impedance, and load impedance. In conjunction with the measurement setup, a calibration procedure was developed. This calibration procedure is of interest because it uses only the reference standards which were available at hand; no new parts were purchased.

Results which were totally unexpected were obtained from measurements on a test amplifier. These results were unexpected in the context of the common view that most engineers have of RF power amplifiers. The important results are: 1) a complex conjugate match is required on

the output of a VHF power transistor in order to obtain maximum power, 2) the input impedance of a power transistor shows little variation with drive level, and 3) the harmonic level of the amplifier output is small. On the other hand, the common view of an RF power transistor would predict: 1) an increasing output power with decreasing load resistance because of the supposed current source nature of a transistor, 2) a large variation of input impedance with drive level because of the supposed grossly nonlinear base-emitter junction, and 3) high levels of harmonic output because of the supposed exponential input-output relationship of a BJT and the rectifying effect of class B amplification.

In spite of the apparent discrepancies with the common "popular theory" this report has shown that all measured phenomena are indeed consistent with accepted semiconductor theory. This was done by adapting a transistor model to the explanation of observed phenomena. The fundamental feature of the model is the inclusion of the charge storage effect which occurs in the base region of the transistor. This charge storage effect is a direct result of the negligible minority carrier recombination within the base when the period of the signal waveform is short compared to recombination time. The model gives extremely good insight into many of the phenomena taking place within the

transistor. For example, the model explains the self biasing phenomenon, the reason for the input current-voltage phase difference, and the reason for the real part of output impedance. Even though certain approximations are inherent in the model and in the measurements used to determine model element values, the model should be considered accurate because of the agreement between model predictions and measured phenomena.

An amplifier design procedure arose naturally from the model. The model enables prediction of the optimum load based on several very easy measurements of model parameters. Use of the model to predict input impedance is more difficult, but a viable alternative exists in direct measurement of input impedance. This measurement is legitimate as long as the optimum load is connected to the transistor output.

In Chapter 1, a summary of currently used techniques illustrated a need for a new approach. The need existed because of the inaccuracies and uncertainties of the old techniques. The technique developed during the course of this project has been shown to be accurate. Additionally, there are no uncertainties associated with the technique developed herein (for example, uncertainties as to the proper drive levels to use in measurement). Such uncertainties are inherent especially in the two-port

modeling approaches.

Many practical considerations in amplifier design were discussed. These included amplifier stability, choice of biasing circuitry, and choice of impedance matching topology. One generally cannot find these practical aspects articulated in a unified fashion in the literature.

5.2 Significant Aspects of the Work

There are five results of the work which are considered to be significant contributions. The first of these is the ability to predict the input impedance of a radio frequency power amplifier. Whereas in the literature there appear collector current solutions for nonlinear differential equations similar to that of Equation 3.11, none of the researchers has followed through by solving for base current and comparing this result to the base voltage. This relationship between the base current and base voltage enables the impedance prediction.

The second contribution is the ability to predict the output impedance of an RF power transistor. Even though this result now appears quite reasonable it is not a result which is clearly presented in the literature. An associated contribution is the articulation of the fact that a conjugate match is required in order to obtain maximum output power, again, a fact which is not clearly

presented in the literature.

The third significant aspect of the work is the explanation of the essentially class A operation of the transistor. This operation is a result of the self biasing phenomenon which in turn is a result of the charge storage occuring in the transistor base. Muller [1967] hints at the class A aspect, but he does not expand on the topic, nor does he give a physical explanation or theoretical reason for the phenonenon. An associated aspect of the self bias class A operation is the improved amplifier efficiency over an externally biased class A amplifier.

The fourth aspect of the work which is important in its contribution is the basic measurement philosophy used. The measurement approach has as its basis a combination of the standard S-parameter measurement technique (the two directional couplers) and a load-pull measurement technique (the variable load). Both of these are individually well documented in the literature, but the combination of the two is not discussed in relation to power amplifiers. The method presented in this dissertation of using the output directional coupler to measure the load presented to the transistor also possesses merit.

The fifth and final significant contribution is probably the most important. It is much more general in nature than the other four. The work presented in this

report has given insight into the basic operation of high frequency power amplifiers, and more importantly has provided an understandable and unified explanation of this basic operation. This work has answered many questions about phenomena which are observed by many engineers (e.g. the ability to tune a power amplifier for maximum output power), but phenomena for which engineers typically have no intuitive explanation.

5.3 Final Results

As a confirmation of the theory and practical aspects developed in the preceeding chapters, a 175 MHz power amplifier was designed and constructed. The performance characterisitics of the amplifier are tabulated in Table 4.1. These final results agree with model predictions and are indicative of an amplifier which performs well.

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VHF BIPOLAR TRANSISTOR POWER AMPLIFIERS: MEASUREMENT, MODELING, AND DESIGN

by

William Patton Overstreet

(ABSTRACT)

Widely used design techniques for radio frequency power amplifiers yield results which are approximate; the initial design is usually refined by applying trial-and-error procedures in the laboratory. More accurate design techniques are complicated in their application and have not gained acceptance by practicing engineers. A new design technique for VHF linear power amplifiers using bipolar junction transistors is presented in this report. This design technique is simple in its application but yields accurate results.

The design technique is based upon a transistor model which is simple enough to be useful for design, but which is sufficiently accurate to predict performance at high frequencies. Additionally, the model yields insight into many of the processes which take place within the typical RF power transistor. The fundamental aspect of the model is the inclusion of charge storage within the transistor base. This charge storage effect gives rise to a nearly sinusoidal collector current waveform, even in a transistor

which ostensibly is biased for class B or nonsaturating class C operation.

Methods of predicting transistor input and output impedances are presented. A number of other topics related to power amplifier measurement and design are also included. A unique measurement approach which is ideally suited for use with power amplifiers is discussed. This measurement approach is a hybrid of the common S-parameter measurement technique and the "load-pull" procedure. Practical considerations such as amplifier stability, bias network design, and matching network topology are also included in the report.

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