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(54) **POWER CONVERTERS HAVING CAPACITOR RESONANT WITH TRANSFORMER LEAKAGE INDUCTANCE**

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**H02M 3/335** (2006.01)

(52) **U.S. Cl.** ..... **363/21.14; 363/17**

(58) **Field of Classification Search** ..... **323/271, 323/222, 282-287; 363/17-20; 315/291, 315/307, 293, 224**

See application file for complete search history.

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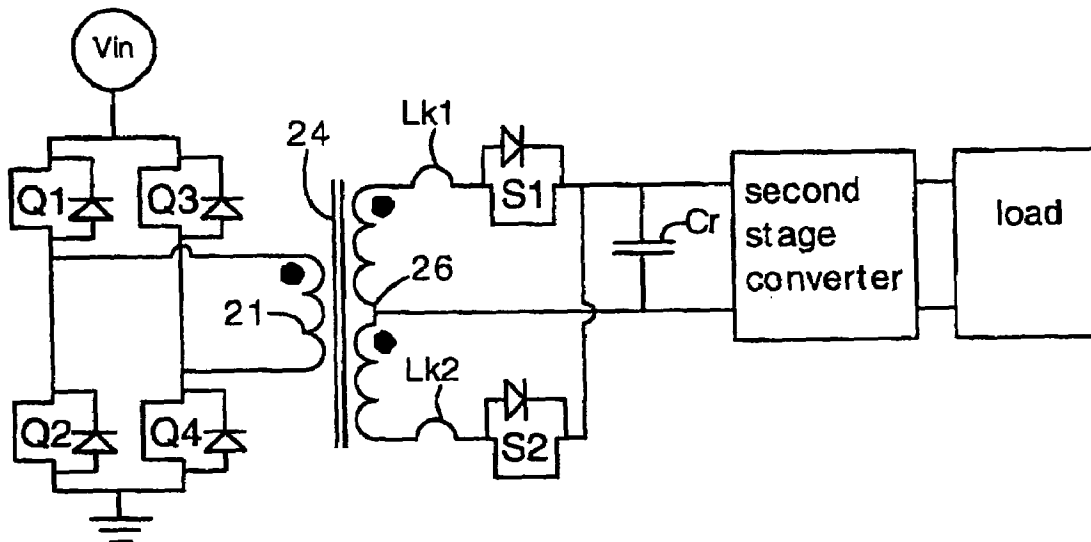
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(57) **ABSTRACT**

Power converters having reduced body diode conduction loss, reduced reverse recovery loss and lower switching noise, among other benefits, have a resonant capacitor Cr connected across an unfiltered output. The resonant capacitor Cr resonates with the leakage inductance Lk of the transformer. The resonant capacitor and leakage inductance are selected such that 1/2 a LC resonance period is equal to an ON time of each secondary switch S1 S2. The resonance provides zero current switching for secondary switches S1 S2, eliminates zero body diode conduction during dead times, and eliminates reverse recovery losses in the secondary switches. The present invention is applicable to many different circuit topologies such as full bridge, active clamp forward, push-pull forward, and center-tap secondary. The present converters provide high energy conversion efficiency and high frequency operation.

**22 Claims, 7 Drawing Sheets**



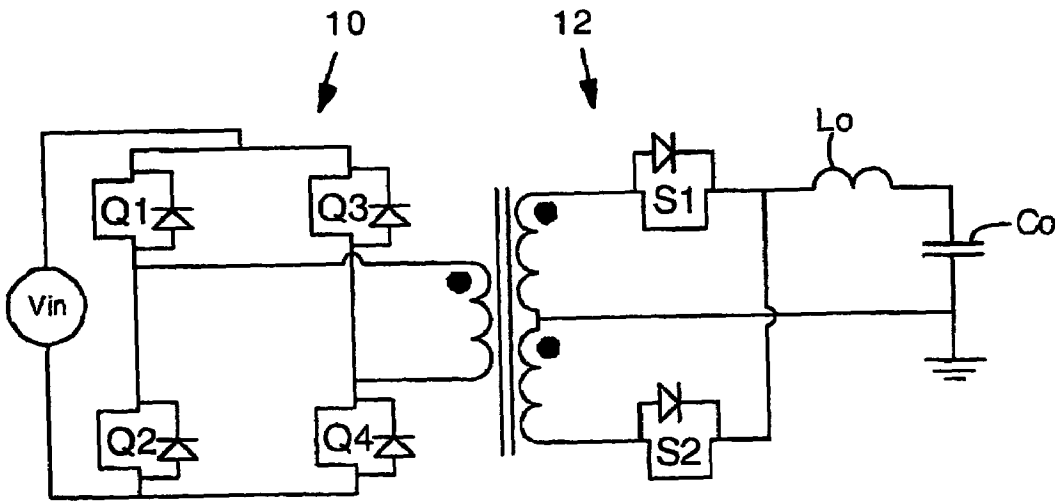


Fig. 1  
Prior Art

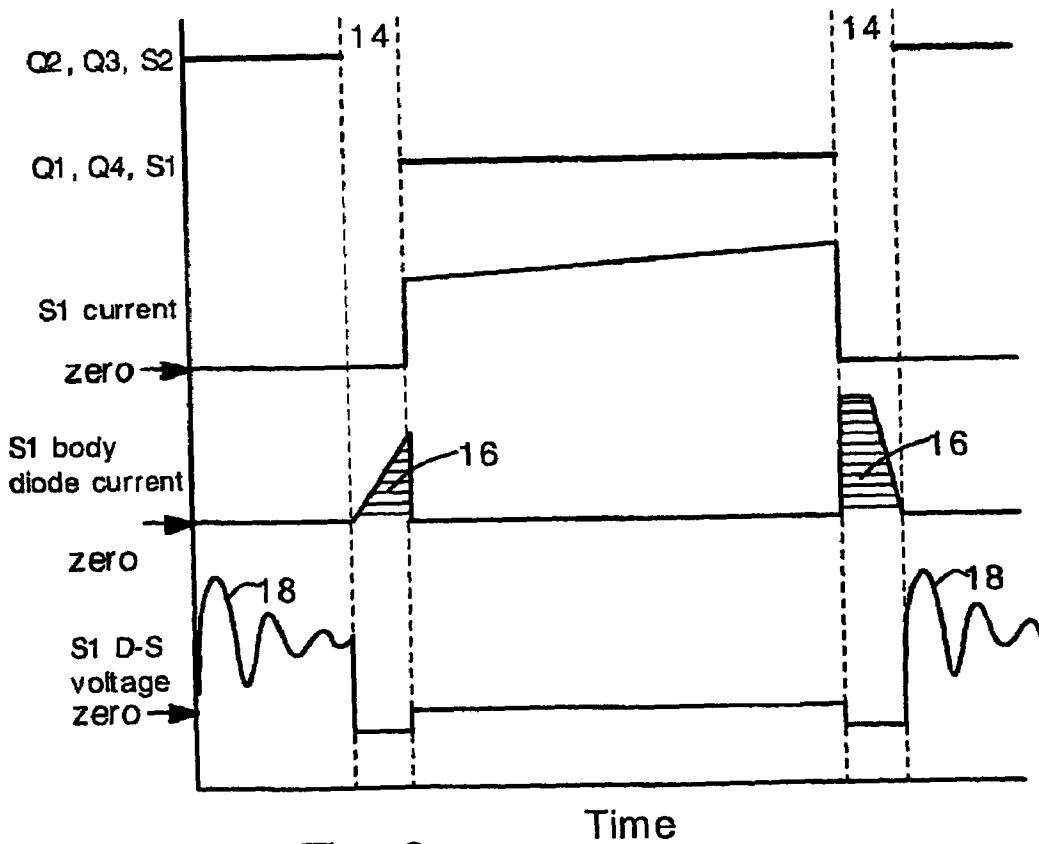


Fig. 2  
Prior Art

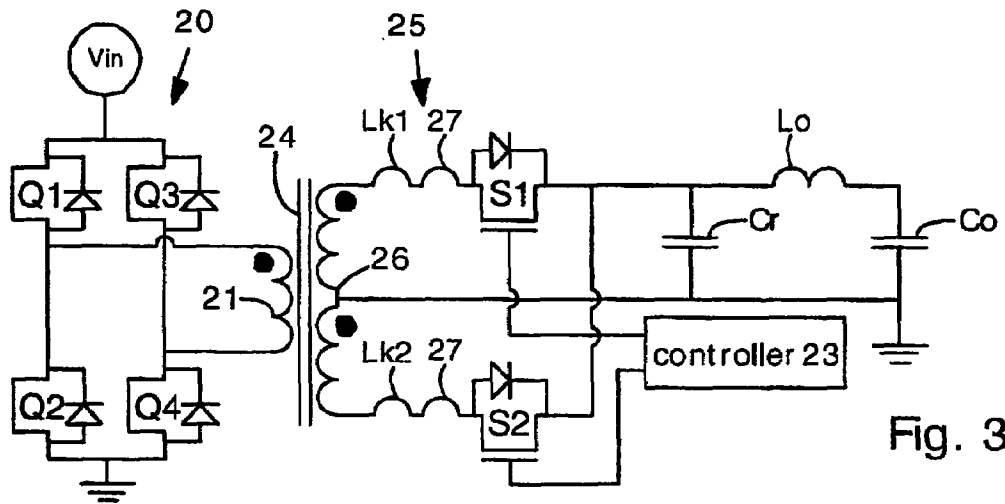


Fig. 3

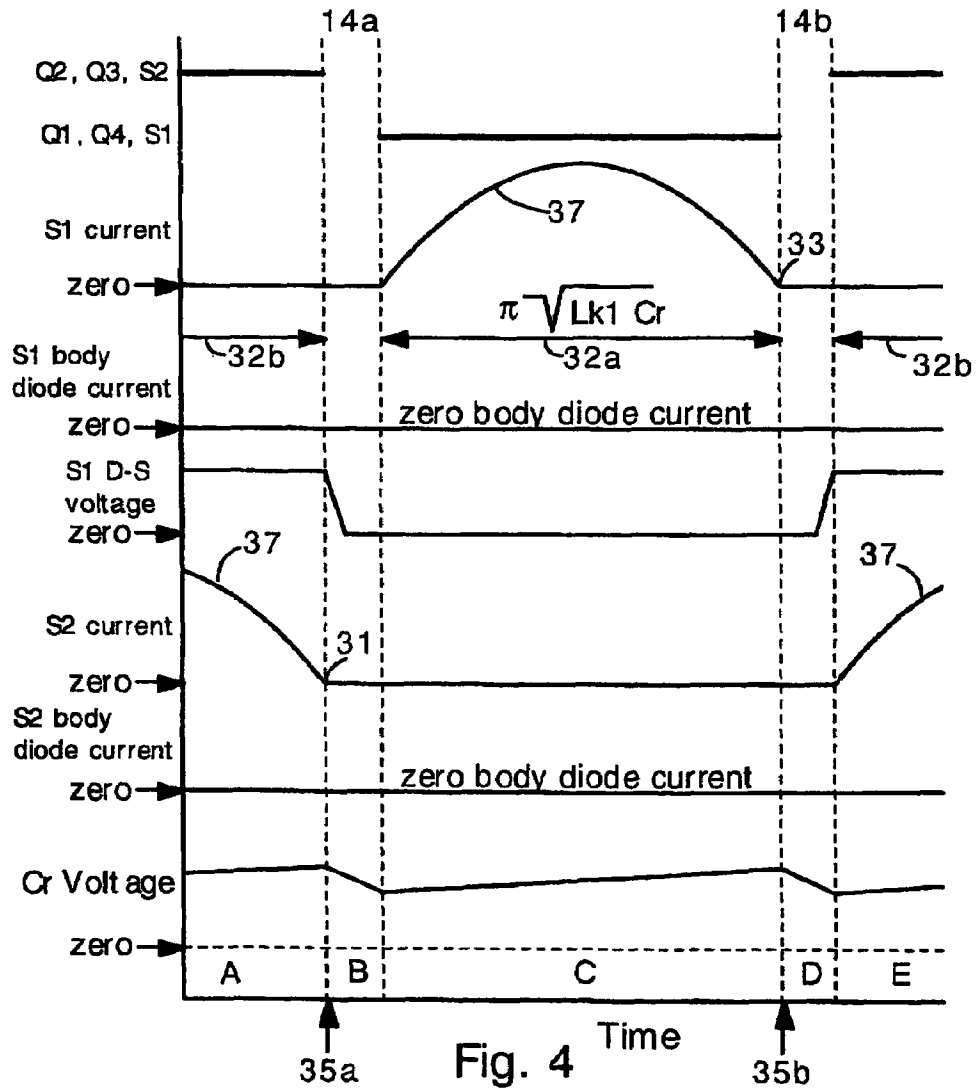
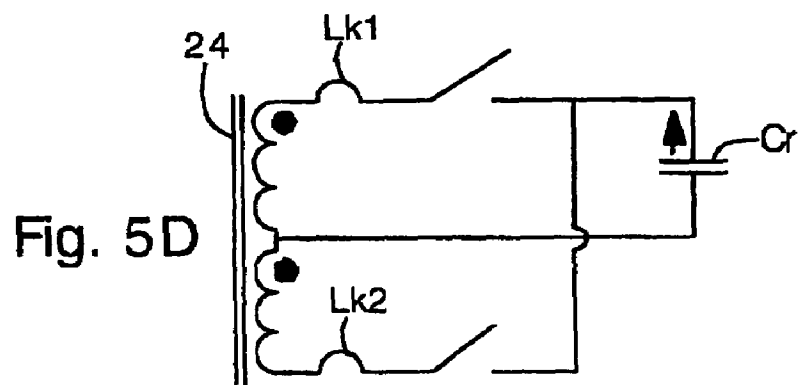
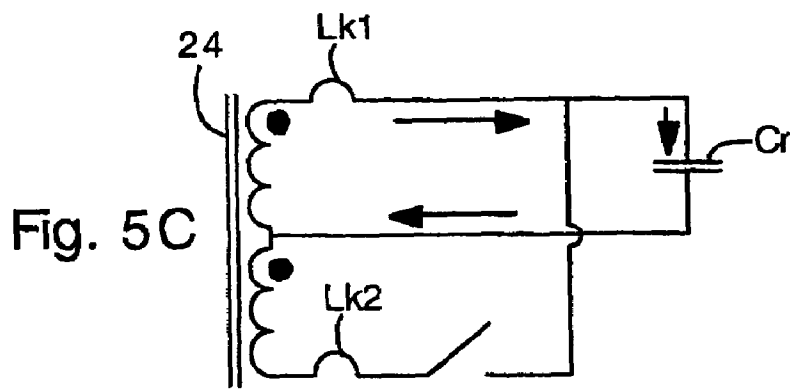
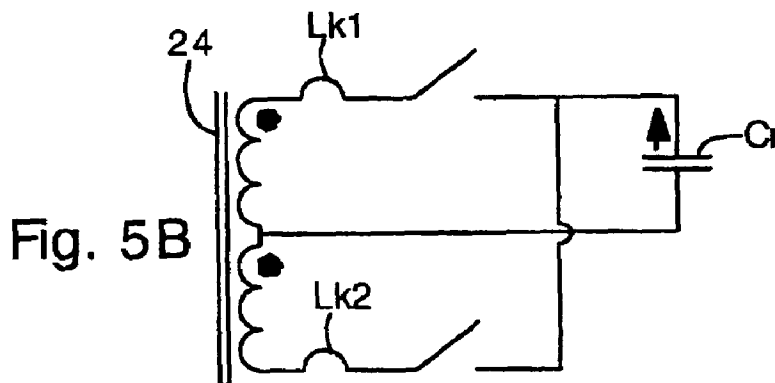
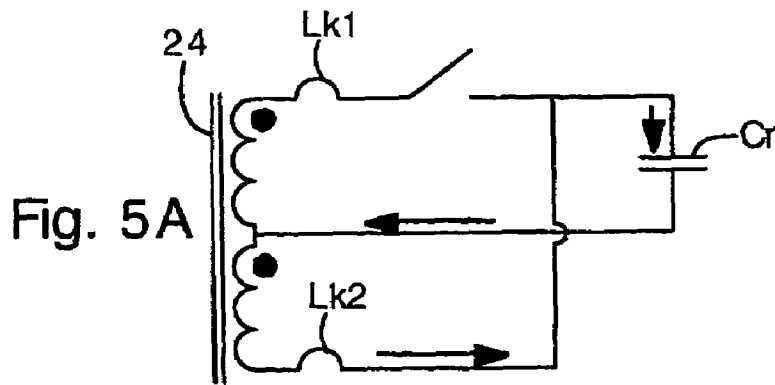
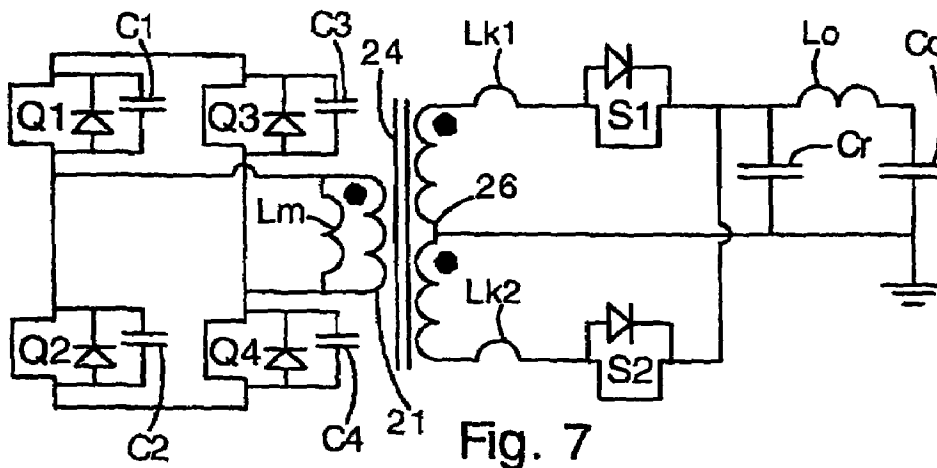
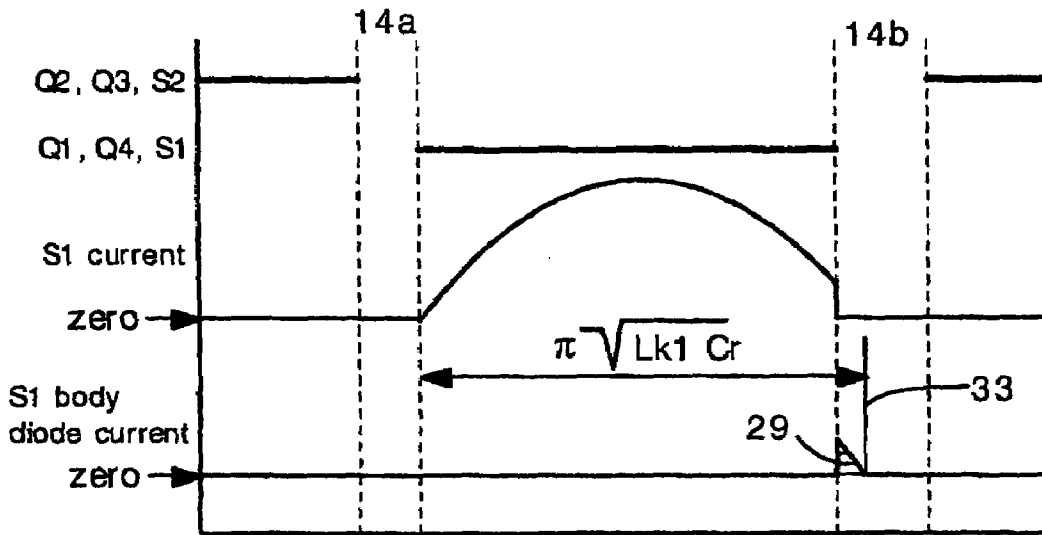
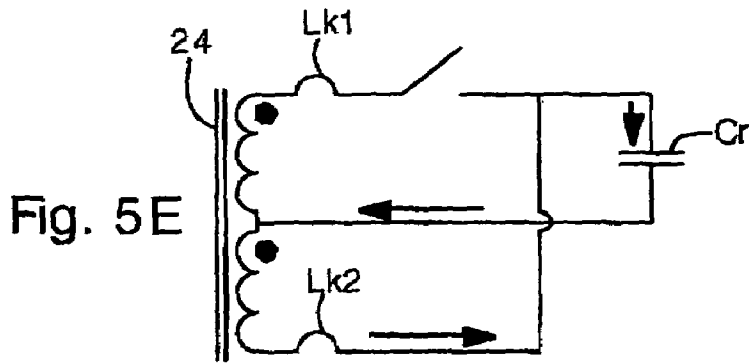


Fig. 4





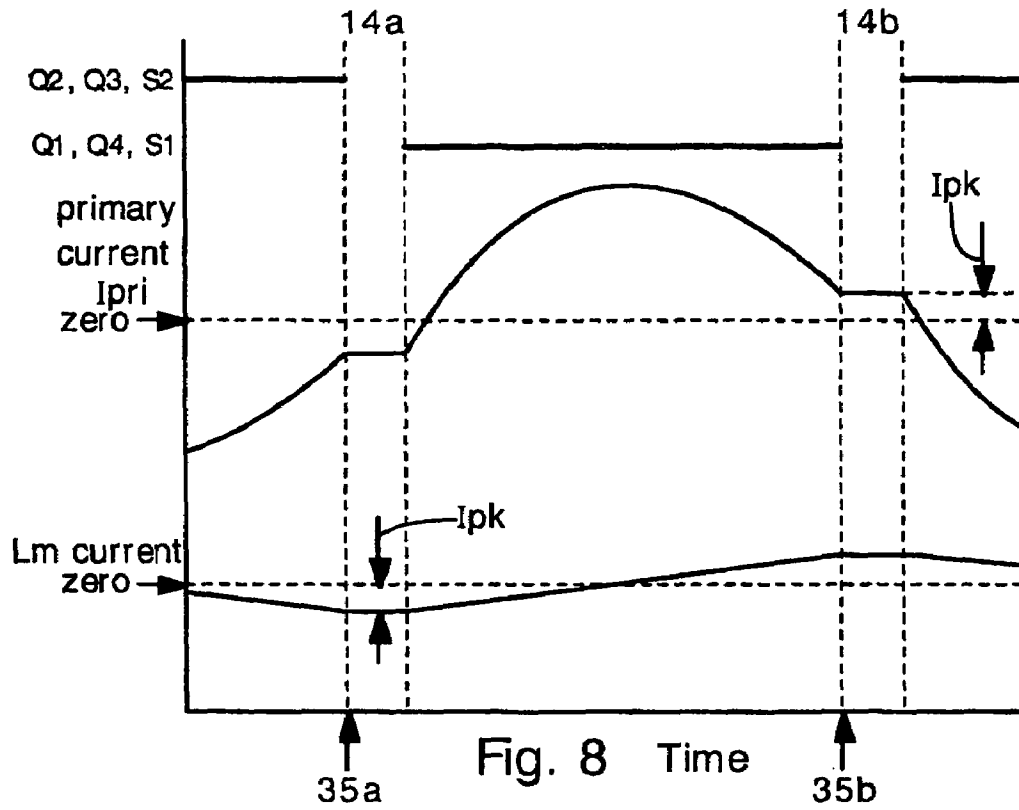


Fig. 8 Time

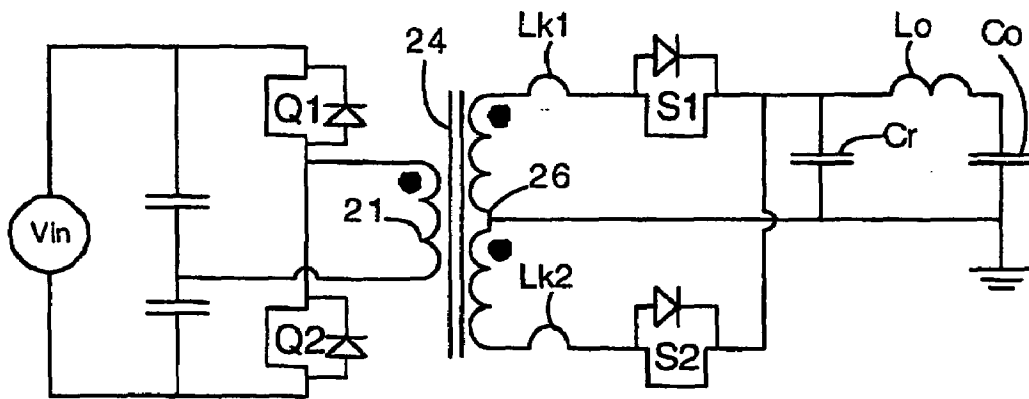


Fig. 9

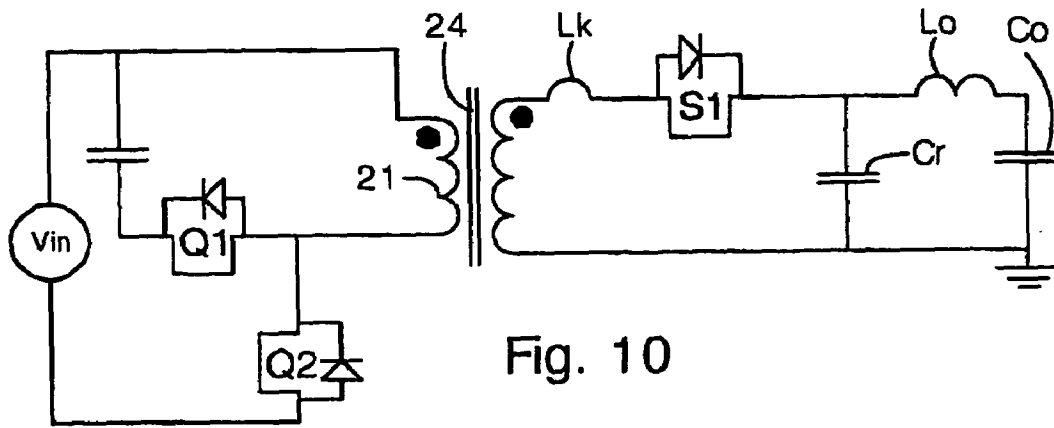


Fig. 10

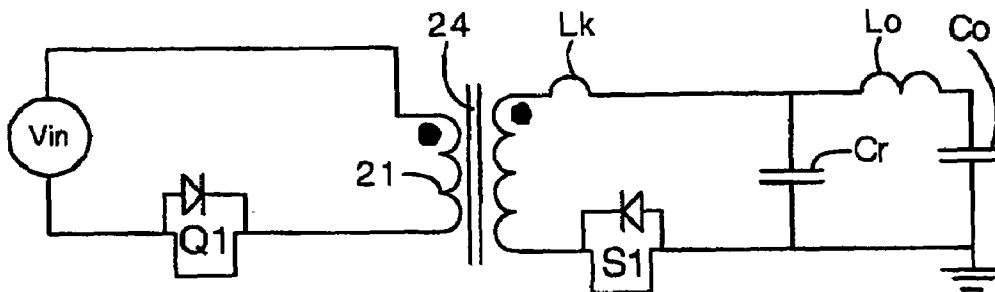


Fig. 11

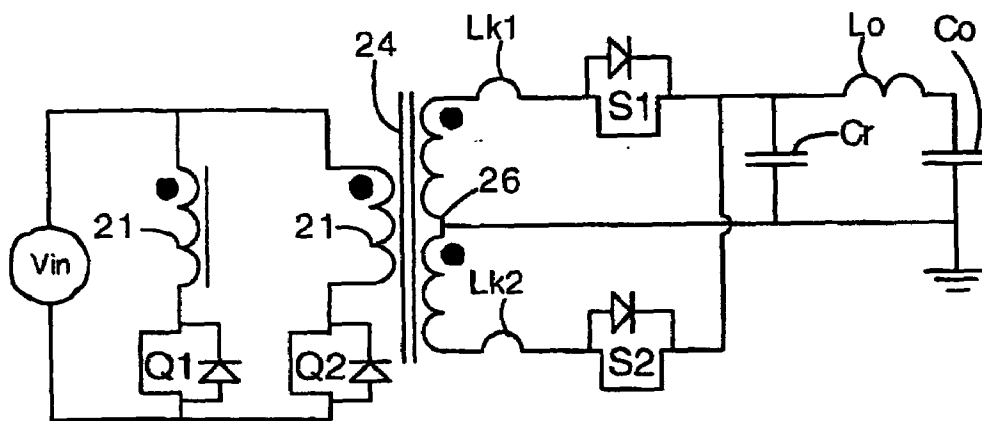
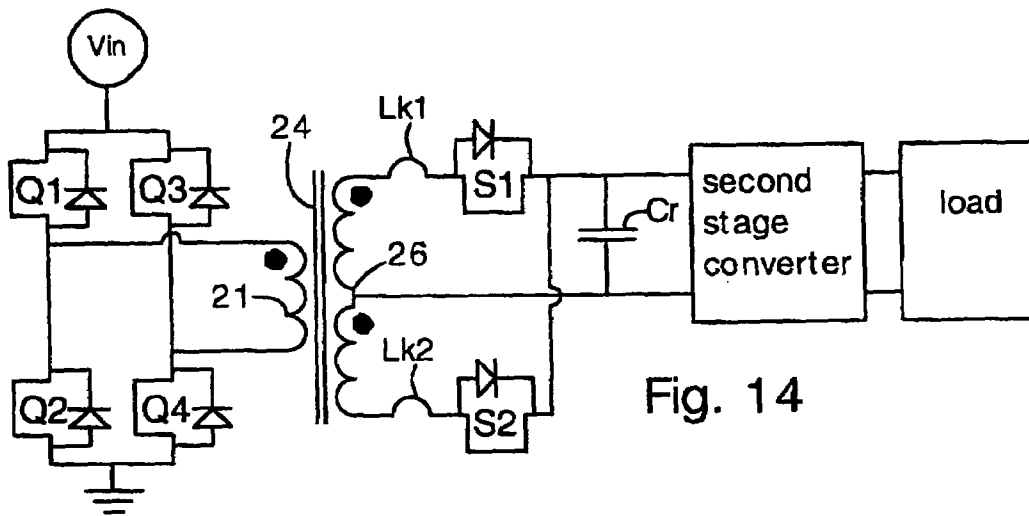
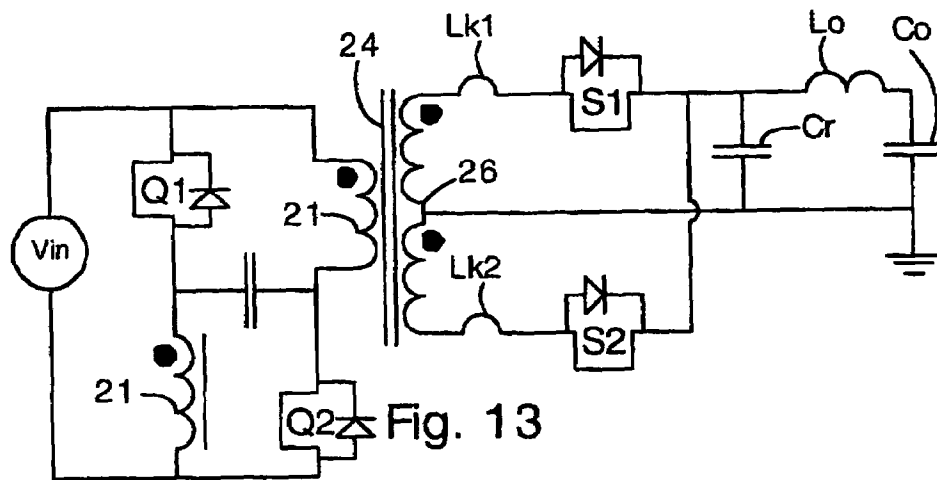


Fig. 12





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## POWER CONVERTERS HAVING CAPACITOR RESONANT WITH TRANSFORMER LEAKAGE INDUCTANCE

### FIELD OF THE INVENTION

The present invention generally relates to synchronous power converters. More particularly, the invention relates to a family of power converters having no requirement for an output inductor, and having a resonant output capacitor. The present converters have a high power conversion efficiency.

### BACKGROUND OF THE INVENTION

Synchronous power converters are widely used in computer and telecommunication electronics. Such power converters typically convert 48 volt bus power to lower voltages (e.g. 12V, 5V and 1.2V) needed for operating microprocessors and the like.

Modern electronics are decreasing in size and typically require increased operating current at lower voltages. As a result, power converters must provide more power while occupying less circuit board space. In order to meet these requirements, power converters must operate at higher frequencies. A high operating frequency allows for smaller passive components. However, high operating frequencies greatly increase body diode conduction losses, reverse recovery losses and switching losses. These losses must be reduced in order to increase the operating frequency of next-generation power converters.

Another problem with high frequency operation is switching noise. The reverse-recovery charge of the switches creates high voltage spikes. When high voltage spikes are present, switches tolerant of high voltages must be used. High voltage-rating switches typically have high ON-state resistance ( $R_{ds(on)}$ ) and therefore higher conduction loss. Hence, a reduction of the voltage spikes would allow the use of low voltage, low loss switches and would provide an increase in operating efficiency.

FIG. 1 shows a conventional power converter with a full bridge primary circuit **10** and a center-tapped secondary circuit **12**. The secondary circuit has an output capacitor  $C_o$  and an output inductor  $L_o$ . The output capacitor is as large as possible, with typical values of about 300 microfarads. A load (not shown) is connected across the output capacitor  $C_o$ . FIG. 2 shows a timing diagram illustrating the typical operation of the circuit of FIG. 1. Horizontal lines indicate the ON times of switches **Q1 Q2 Q3 Q4 S1** and **S2**. During dead times **14**, the body diodes of secondary switches **S1 S2** conduct current pulses **16**, resulting in substantial energy loss and reverse recovery loss. Also, high voltage spikes **18** and ringing occur across the switches **S1 S2**. The body diode conduction loss and reverse recovery loss increase as operating frequency increases, and result in lower power conversion efficiency.

It would be an advance in the art of power conversion to provide a power converter with reduced body diode conduction loss, reduced reverse recovery loss and reduced switching noise. Such circuits could operate at high frequency and have very small size.

### SUMMARY OF THE INVENTION

The present invention provides a power converter having a primary circuit and a secondary circuit coupled through a transformer. The primary circuit and secondary circuits each have at least one switch. The transformer has primary and

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secondary windings. The circuit has an inductance in series with either the primary winding or secondary winding. The inductance can be a leakage inductance of the transformer. A resonant capacitor is connected across an unfiltered output of the secondary circuit. The resonant capacitor and inductance are resonant such that  $\frac{1}{2}$  of an LC resonant period is approximately equal to an ON time of the switch in the secondary circuit. This resonance results in a sinusoidal or nearly sinusoidal current pulse through the secondary switch.

The inductance may be a discrete inductor connected in series with the primary winding or secondary winding.

The secondary circuit may include an output inductor and output capacitor downstream of the resonant capacitor.

The primary circuit may be a half-bridge circuit, a full-bridge circuit, an active clamped forward circuit, a resonant-reset forward circuit, a push-pull circuit, and a push-pull forward circuit.

The secondary circuit may be a center-tapped circuit, or forward-type rectifier circuit.

The ON time of the secondary switch may be slightly shorter than  $\frac{1}{2}$  the LC resonant period. For example, the ON time of the secondary switch may be 0–10 nanoseconds shorter than  $\frac{1}{2}$  the LC resonant period. The ON time of the secondary switch may be within 10% of  $\frac{1}{2}$  the LC resonant period (e.g., preferably within  $\pm 10\%$ , and more preferably within  $\pm 5\%$ ).

The transformer may have a magnetizing inductance large enough to provide zero voltage switching (ZVS) for the primary side switch. The magnetizing inductance provides ZVS by absorbing energy from the capacitance of the primary side switch.

In another embodiment of the present invention, the secondary switch is operable to have an ON time approximately equal to  $\pi\sqrt{LKCr}$  (e.g., preferably within  $\pm 10\%$  or more preferably within  $\pm 5\%$ )

### DESCRIPTION OF THE FIGURES

FIG. 1 (Prior Art) shows a conventional converter comprising a full bridge primary and center-tapped secondary circuit.

FIG. 2 (Prior Art) shows a timing diagram illustrating the operation of the circuit of FIG. 1, and undesirable body diode conduction and high voltage spikes.

FIG. 3 shows an embodiment of the present invention having a full bridge primary circuit and a center-tapped secondary circuit.

FIG. 4 shows a timing diagram illustrating the operation of the circuit of FIG. 3.

FIGS. 5A–5E illustrate circuit conditions during time periods A, B, C, D, and E illustrated in FIG. 4.

FIG. 6 illustrates a small amount of body diode conduction that occurs when switches are turned off slightly early.

FIG. 7 illustrates the effect of transformer magnetizing inductance on zero voltage switching capability.

FIG. 8 shows a timing diagram illustrating the current in the primary winding and the magnetizing current  $I_m$  associated with the magnetizing inductance of the transformer.

FIGS. 9–13 illustrate alternative embodiments of the present invention with various primary circuits.

FIG. 14 shows the present converter in combination with a second stage converter.

DETAILED DESCRIPTION OF THE  
PREFERRED EMBODIMENTS OF THE  
INVENTION

The present invention provides a power converter with reduced body diode conduction loss, reduced reverse recovery loss and reduced voltage spikes. Additionally, the present power converters can also have zero-voltage switching (ZVS) operation and reduced turn-off loss. The present power converters can operate at high frequencies (e.g. 1–2 Mhz), and can therefore have small passive components and high power density. The present power converters provide exceptionally high efficiency.

In the present invention, the secondary circuit comprises a resonant capacitor. The resonant capacitor resonates with leakage inductance of the transformer. The resonant frequency is selected such that  $\frac{1}{2}$  of a LC resonant period is the same duration as an ON time of a secondary switch. The resonance between the resonant capacitor and leakage inductance produces a sinusoidal (or nearly sinusoidal) current pulse through the secondary switches. The sinusoidal pulse shape results in greatly reduced body diode conduction, reduces voltage spikes and ringing, reduces or eliminates reverse recovery loss, and reduces turn-off loss. Additionally, the present invention can provide zero voltage switching (ZVS) for all switching devices.

FIG. 3 illustrates a power converter circuit according to the present invention. The converter has a full bridge primary circuit 20 comprising 4 switches Q1 Q2 Q3 Q4, and a center-tap secondary circuit 25 comprising two secondary switches S1 S2. A transformer 24 has a primary winding 21 and a center-tapped secondary winding 26. An optional output capacitor Co and an optional output inductor Lo are connected to the secondary circuit 25 and provide noise filtering. A load (not shown) is connected across the output capacitor Co. The converter has a switch controller 23 for controlling the secondary switches S1 S2.

The switches are preferably low on-resistance MOSFET switches, as known in the art. The transformer can be an integrated magnetic ferrite-core transformer, also well known in the art.

The transformer 24 necessarily includes leakage inductances Lk1 Lk2. The leakage inductances should have a known, predetermined value. The leakage inductances Lk1 Lk2 preferably have the same value. Also, it is well known that the leakage inductances Lk1 Lk2 are equivalently modeled in the primary circuit 20 or secondary circuit 25. For convenience, the leakage inductances Lk1 Lk2 are shown in the secondary circuit 25.

Significantly, the secondary circuit 25 includes a resonant capacitor Cr connected across an unfiltered output of the circuit (i.e. connected directly to secondary switches S1 S2). The resonant capacitor Cr and leakage inductances Lk1 Lk2 resonate and thereby shape the current pulses that travel through the secondary switches S1 S2. The resonant capacitor Cr capacitance and leakage inductances Lk1 Lk2 are selected so that they resonate at a specific frequency. If the leakage inductances Lk1 Lk2 of the transformer do not have high enough inductance, then separate, discrete inductors 27 can be added in series with the leakage inductances Lk1 Lk2. The discrete inductances 27 can be located in the primary circuit or in the secondary circuit.

FIG. 4 shows a timing diagram illustrating the operation of the circuit of FIG. 3. Dark horizontal lines illustrate ON times of switches Q2, Q3, S2 and switches Q1 Q4 S1. A first dead time 14a and a second dead time 14b occur between ON times of switches Q2, Q3, S2 and Q1 Q4 S1. Switch S2

turns OFF at a first turn off time 35a (i.e. the beginning of first dead time 14a). Switch S1 turns OFF at a second turn off time 35b (i.e. the beginning of second dead time 14b). The S2 body diode current (during the first dead time 14a) is zero or very small because the switch S2 is turned OFF at a zero current crossing 31. Similarly, the S1 body diode current (during the second dead time 14b) is zero or very small because the switch S1 is turned OFF at a zero current crossing 33.

The leakage inductances Lk1 Lk2 and resonant capacitor Cr are selected so that  $\frac{1}{2}$  of an LC resonance period is approximately equal to an ON time 32a 32b of the secondary switches S1 S2. Expressed mathematically, the ON time 32a 32b of the secondary switches S1 S2 should be approximately equal to  $\pi\sqrt{LkCr}$ , where Lk is the inductance of each leakage inductance Lk1 Lk2 (in combination with the inductance of the discrete inductor 27, if present), respectively, and Cr is the capacitance of the resonant capacitor Cr. The resonance effect produces sinusoidal or nearly sinusoidal current pulses 37 through the switches S1 S2. Also, the resonant effect assures that the leakage inductances Lk1 Lk2 (and discrete inductors 27, if present) are discharged, or nearly discharged, at the turn off times 35a 35b (i.e. at the beginning of each dead time 14a 14b). Therefore, there will be zero or nearly zero current flowing through secondary switches S1 S2 at turn off and during the dead times 14a 14b.

The zero current turn off condition for switches S1 S2 results in zero or nearly zero body diode conduction, and zero or nearly zero reverse recovery loss. Hence, power conversion efficiency is greatly improved.

Preferably, the leakage inductances Lk1 Lk2 are equal. If they are not equal, then the ON times 32a 32b of switches S1 S2 can be different so that the ON times 32a 32b each match  $\frac{1}{2}$  the resonant period  $\pi\sqrt{LkCr}$  for each leakage inductance Lk1 Lk2. For example, if leakage inductance Lk1 is larger than Lk2, then switch S1 can have a longer ON time than switch S2.

The timing diagram of FIG. 4 is divided into 5 time periods: A, B, C, D, and E. FIGS. 5A, 5B, 5C, 5D and 5E illustrate secondary circuit conditions within the circuit of FIG. 3 during the time periods A, B, C, D, and E, respectively:

FIG. 5A: Switch S2 is ON. Current through S2 drops as leakage inductance Lk2 discharges and resonant capacitor Cr becomes charged.

FIG. 5B: Switch S2 turns OFF at the zero current crossing 31 of the S2 current. During the first dead time 14a, there is no freewheeling current and therefore no body diode conduction through switch S2. Resonant capacitor Cr discharges through output inductor Lo.

FIG. 5C: Switch S1 turns ON and current through switch S1 rises gradually as leakage inductance Lk1 is charged. Current through switch S1 drops and resonant capacitor Cr becomes charged.

FIG. 5D: Switch S2 turns OFF at the zero crossing 33 of the S1 current. During the second dead time 14b, there is no freewheeling current and therefore no body diode conduction through switch S1. Resonant capacitor Cr discharges through output inductor Lo.

FIG. 5E: Switch S2 turns ON and current through switch S2 rises gradually as leakage inductance Lk2 is charged.

In typical power converter circuits, the leakage inductances Lk1 Lk2 will typically have inductance values of about 3–7 nanohenries. For operation at frequencies in the range of about 1–2 Mhz, the resonant capacitor can have values in the range of about 1–20 microfarads, for example.

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The voltage on the resonant capacitor is illustrated in FIG. 4. The voltage on the resonant capacitor Cr is essentially a DC voltage with a small AC ripple voltage imposed. The average voltage on the resonant capacitor Cr will be approximately  $V_{in}/N$ , where  $V_{in}$  is the input voltage, and N is the turns ratio of the transformer 24. The resonant capacitor Cr provides current to the output inductor L<sub>o</sub> during the dead times 14a 14b. The resonant capacitor Cr is charged when either secondary switch S1 or S2 is ON.

It is important to note that the drain-source (D-S) voltage across switches S1 S2 does not experience high voltage spikes 18 in the present invention. This is because the switches S1 S2 experience zero current (or near zero current) at turn-off times 35a 35b. Zero current at turn-off times 35a 35b greatly reduces the amount of high voltage spikes and noise. Consequently, the present invention permits the use of switches (primary side Q1 Q2 Q3 Q4 and secondary side S1 S2 switches) having a lower voltage rating, and therefore lower ON-state resistance (R<sub>ds(on)</sub>). Employing switches with low ON-state resistance substantially increases the power conversion efficiency. Hence, the low current at turn-off times 35a 35b contributes to increased power conversion efficiency.

FIG. 6 illustrates an alternative embodiment in which the switches Q1 Q4 and S1 turn off early, i.e. before the zero current crossing 33. In this case, there will be a small amount of body diode current 29. The amount of body diode current 29 will increase with earlier turn off of switches Q1 Q4 and S1. Therefore, in order to minimize body diode conduction, avoid reverse recovery loss and increase efficiency, the switches Q1 Q4 and S1 should turn off as close to the zero current crossing 33 as possible. Turning off switches too early will excessively increase body diode conduction, and will greatly increase reverse recovery loss. Of course, the same considerations apply to switches Q2 Q3 and S2.

It is highly undesirable to turn off switches S1 S2 after the zero current crossings 31 33. If switches S1 S2 are ON after the zero current crossings 31 33, then a current reversal will occur (i.e., current will reverse direction and flow backwards through the secondary switches S1 S2). A current reversal will tend to greatly reduce operating efficiency because the reversed energy flow will be completely wasted in the primary side circuit 20. By comparison, body diode conduction wastes only a portion of energy passing through a body diode. Hence, late turn off of switches S1 S2 tends to reduce operating efficiency more than early turn off of switches S1 S2.

Therefore, in view of unavoidable timing errors and jitter, it is generally preferred in the present invention to operate the circuit with a slightly early turn off of switches S1 S2 and small body diode conduction. A slightly early turn off will assure that a current reversal does not occur even in the event of small timing errors. The secondary switches S1 S2 can be turned off up to 10 or 20 nanoseconds early, for example.

The present invention is capable of providing zero voltage switching (ZVS) for all the switches Q1 Q2 Q3 Q4 S1 S2. A particular and substantial advantage of the invention is that ZVS can be provided for any load condition. No matter how much energy is drawn by the load, ZVS for all the switches can be assured.

By comparison, prior art converter circuits (e.g. the circuit of FIG. 1) typically provide ZVS for only a specific load condition. This is because, in the prior art converter circuits, the energy stored in the leakage inductors Lk1 Lk2 is used to provide ZVS.

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FIG. 7 illustrates how load-independent ZVS is provided in the present invention. The transformer 24 intrinsically has magnetizing inductance L<sub>m</sub> in parallel with the transformer primary 21. The primary switches Q1 Q2 Q3 Q4 each have junction capacitors C1 C2 C3 C4, as is well known in the art. During the dead times 14a 14b the magnetizing inductance L<sub>m</sub> draws current from junction capacitors C1 C2 C3 C4 so that they are completely discharged, or nearly discharged at turn on. In order to provide this effect, the magnetizing inductance L<sub>m</sub> of the transformer 24 must be able to store all the energy of the four capacitors C1 C2 C3 C4. This requires a relatively small magnetizing inductance L<sub>m</sub> because a smaller magnetizing inductance L<sub>m</sub> will conduct more current, and thereby store more energy than a large magnetizing inductance. This effect is independent of the load. Hence, the present invention will provide load-independent ZVS for the primary side switches if the magnetizing inductance L<sub>m</sub> has a small enough value.

Specifically, in order to provide ZVS, the magnetizing inductance should satisfy the following relationship:

$$\frac{1}{2}(L_m I_{pk}^2) \geq 4 * (\frac{1}{2}(C V_m^2))$$

where L<sub>m</sub> is the magnetizing inductance, I<sub>pk</sub> is the peak magnetizing inductance current (which occurs during the dead times 14a 14b), C is the capacitance of the junction capacitors C1 C2 C3 C4 (assumed to be equal), and V<sub>in</sub> is the input voltage. The left hand side of the equation represents the energy storage capacity of the magnetizing inductance, and the right hand side of the equation represents the energy storage capacity of the junction capacitors C1 C2 C3 C4.

Another advantage of the present invention is that turn off loss of the primary switches Q1 Q2 Q3 Q4 can be greatly reduced. Turn off loss is approximately proportional to current in the primary winding 21 at the turn off times 35a 35b. In the present invention, the primary winding current is relatively small at the turn off times 35a 35b, and hence the turn off loss is small. FIG. 8 shows a timing diagram illustrating the primary winding current I<sub>pri</sub> and magnetizing inductance current (L<sub>m</sub> current). The primary current I<sub>pri</sub> rises and falls in the same manner as the current flowing through the secondary switches S1 S2. The magnetizing inductance L<sub>m</sub> current is superimposed on the primary current I<sub>pri</sub>. At the turn off times 35a 35b, the only current flowing through the primary winding 21 is the peak magnetizing current I<sub>pk</sub>, which is associated with the magnetizing inductance L<sub>m</sub>. Since the peak magnetizing current I<sub>pk</sub> is relatively small (compared to the total primary winding current) at the turn off times 35a 35b, the turn off loss is relatively small.

The peak magnetizing current I<sub>pk</sub>, and hence the turn off loss, is reduced by large values of magnetizing inductance L<sub>m</sub>. Therefore, in order to reduce the turn off loss, the magnetizing inductance should have a relatively large value.

As noted above, load-independent ZVS requires a small value for magnetizing inductance L<sub>m</sub>. Therefore, the magnetizing inductance value L<sub>m</sub> should be selected to be small enough to provide ZVS, but still large enough to provide relatively small turn off loss. The advantages of load-independent ZVS and advantages of small turn off loss must be balanced in the converter design. Properly selecting the value of magnetizing inductance will provide a converter with both low turn off loss, and load-independent ZVS operation. For typical converter circuits operating at about 1 Mhz, the transformer can have a magnetizing inductance in the range of about 3000–7000 nanohenries.

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The present invention includes many circuit topologies other than the full bridge/center tapped circuit of FIG. 3. The resonant capacitor  $C_r$  can be included in many different kinds of converter circuits to provide the advantages described herein: reduced body diode conduction, reduced reverse recovery loss, load-independent ZVS for all switches, reduced switching noise, and reduced turn off loss. In particular, the resonant capacitor of the present invention can be used with primary circuits such as the half-bridge, push-pull, push-pull forward, active-clamped forward, and resonant reset forward, in combination with secondary circuits such as center-tapped rectifier and forward-type rectifier.

FIG. 9, for example, shows a converter with a half bridge primary circuit and center-tapped secondary circuit according to the present invention.

FIG. 10 shows a converter with an active-clamp forward primary circuit and forward rectifier secondary circuit according to the present invention.

FIG. 11 shows a converter with a resonant-reset forward primary circuit and forward rectifier secondary circuit according to the present invention.

FIG. 12 shows a converter with a push-pull primary circuit and center-tapped secondary circuit according to the present invention.

FIG. 13 shows a converter with a push-pull forward primary circuit and center-tapped secondary circuit according to the present invention.

The circuits of FIGS. 9, 10, 11, 12, and 13 all have a resonant capacitor  $C_r$  and can all provide the advantages of reduced body diode conduction, reduced reverse recovery loss, load-independent ZVS for all switches, reduced switching noise, and reduced turn off loss.

It is noted that the circuits of FIGS. 9, 10, 11, 12, and 13 can alternatively illustrate the leakage inductance  $L_k$  in series with the primary winding 21. The leakage inductance  $L_k$  is intrinsic to the transformer and can be considered to be within either the primary circuit or secondary circuit. This characteristic of the leakage inductance  $L_k$  is well known in the art.

FIG. 14 illustrates another embodiment of the invention in which the output inductor  $L_o$  and output capacitor  $C_o$  are absent. A second stage converter 50 is connected downstream of the resonant capacitor  $C_r$ . The second stage converter can be a buck converter or any other non-isolated DC/DC converter. With a second stage converter, typically no output inductor or output capacitor is necessary because the inductance (and, optionally, capacitance) of the second stage converter provides filtering of the power provided to the load.

The present invention can provide converters with exceptionally high power conversion efficiency in the range of about 96–98%. Typically, the present power converters provide a 5–6% boost in power conversion efficiency compared to similar conventional converters lacking the resonant capacitor.

It will be clear to one skilled in the art that the above embodiment may be altered in many ways without departing from the scope of the invention. Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents.

What is claimed is:

1. A power converter, comprising:

- a) a primary circuit including at least one switch;
- b) a secondary circuit including at least one switch;
- c) an inductance in one of said primary circuit and said secondary circuit;

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- d) a controller for controlling said at least one switch in said secondary circuit to deliver power; and
- e) a capacitor connected to be resonant with said inductance, wherein the resonant capacitor and inductance are resonant such that  $\frac{1}{2}$  of an LC resonant period is approximately equal to an ON time of the switch in the secondary circuit.

2. The power converter of claim 1 wherein the inductance is a leakage inductance of a transformer.

3. The power converter of claim 1 wherein the inductance includes inductance of a discrete inductor.

4. The power converter of claim 1 further comprising an output inductor and output capacitor downstream of the resonant capacitor and inductance.

5. The power converter of claim 1 wherein the primary circuit comprises a circuit selected from the group consisting of a half-bridge circuit, a full-bridge circuit, an active clamped forward circuit, a resonant-reset forward circuit, a push-pull circuit, and a push-pull forward circuit.

6. The power converter of claim 1 wherein the secondary circuit comprises a circuit selected from the group consisting of center-tapped circuit or forward rectifier circuit.

7. The power converter of claim 1 further comprising a second stage converter downstream of the resonant capacitor.

8. The power converter of claim 1 wherein the ON time of the secondary switch is 0–10 nanoseconds shorter than  $\frac{1}{2}$  the LC resonant period.

9. The power converter of claim 1 wherein the transformer has a magnetizing inductance, and wherein the magnetizing inductance is small enough to provide ZVS for the primary side switch.

10. The power converter of claim 1 wherein the ON time of the secondary switch is within 10% of  $\frac{1}{2}$  the LC resonant period.

11. A power converter, comprising:

- a) a primary circuit including at least one primary switch;
- b) a secondary circuit including at least one secondary switch;
- c) an inductance, wherein the inductance has an inductance value  $L_k$ ; and
- d) a capacitor connected to be resonant with said inductance, wherein the capacitor has a capacitance value  $C_r$ ; and wherein the secondary switch is controlled to have an ON time approximately equal to  $\pi/\sqrt{L_k C_r}$ .

12. The power converter of claim 11 wherein the inductance is a leakage inductance of a transformer coupling said primary circuit and said secondary circuit.

13. The power converter of claim 11 wherein the inductance is an inductance of a discrete inductor separate from the transformer, wherein the discrete inductor is connected in series with the primary winding or secondary winding.

14. The power converter of claim 11 further comprising an output inductor and output capacitor downstream of the resonant capacitor and inductance.

15. The power converter of claim 11 wherein the primary circuit comprises a circuit selected from the group consisting of a half-bridge circuit, a full-bridge circuit, an active clamped forward circuit, a resonant-reset forward circuit, a push-pull circuit, and a push-pull forward circuit.

16. The power converter of claim 11 wherein the secondary circuit comprises a circuit selected from the group consisting of center-tapped circuit or forward rectifier circuit.

17. The power converter of claim 11 further comprising a second stage converter downstream of the resonant capacitor.

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18. The power converter of claim 11 wherein the ON time of the secondary switch is 0–10 nanoseconds shorter than it  $\pi\sqrt{LkCr}$ .

19. The power converter of claim 11 wherein the ON time of the secondary switch is within 10% of it  $\pi\sqrt{LkCr}$ .

20. The power converter of claim 11 wherein the transformer has a magnetizing inductance, and wherein the magnetizing inductance is small enough to provide ZVS for the primary side switch.

21. The power converter of claim 2 wherein the inductance includes inductance of a discrete inductor separate

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from the transformer, wherein the discrete inductor is connected in series with the primary winding or secondary winding.

22. The power converter of claim 12 wherein the inductance includes inductance of a discrete inductor separate from the transformer, wherein the discrete inductor is connected in series with the primary winding or secondary winding.

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