VOLTAGE-TO-DIGITAL CONVERTER DESIGN

by

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I INTRODUCTION

Background

This thesis has been written as an outgrowth of voltage-to-digital converter development done by the author for his employer. The development work was done because commercially available converters lacked the ability to operate in a 70°C temperature environment and/or they seemed deficient in temperature and long term stability, and because economic considerations appeared to justify the design effort.

Description and Application of Voltage-to-Digital Converters

An analog-to-digital converter is a device which accepts an analog quantity at its input and then provides a digitized output that is proportional to or otherwise representative of its input quantity.

The output voltage of transducers such as tachometers, potentiometers, shunts and thermocouples are analog voltage signals that are typically, respectively representative of the analog quantities of speed, position, torque, and temperature. These analog quantities and many others are typical of quantities which one might wish to display and/or record and/or use for references or feedback in control systems.

A common display voltage device is the D'Arsonval or similar meter and a common voltage recording device is the pen recorder. The

meter and recorder present their information in an analog manner. The previously mentioned transducers are frequently used directly as references and feedbacks in analog control systems.

The totally analog instrumentation, recording, and control system can often be outperformed,or at least outperformed for a given cost, by combined use of analog and digital techniques. This introduction will not treat system considerations versus analog and digital techniques versus economics, but it will suggest the role of analog-to-digital converters in some hybrid applications. In particular, the applications will be related to voltage-to-digital converters which accept a voltage input and then output combinations of two-state voltage levels that the converter has generated and coded to be linearly proportional to its input voltage.

First, consider applications where voltage instrumentation and/or recording is required. Except possibly for go/no-go types of instrumentation, a man can usually comprehend only one set of numerical data at any one time, thus serial indication is often useful indication. For such applications, a number of voltages can be serially collected with a voltage sampler that outputs to a voltage-to-digital converter. The converter's output can then operate lamp indicators that are visible at a convenient location. The system's equipment consists of one sampler item, perhaps a relay or stepping switch interlock for each system analog device, one voltage-to-digital converter and one indicator. The system can indicate with three to

four digit accuracy and only one piece of accurate equipment, the converter, is required. Recording applications can be satisfied with the same equipment except that an electrically controlled printer or typewriter will be substituted for the indicator and a piece of serializing equipment might have to be inserted between the converter and the printer or typewriter. The sampler of these systems can be made to operate sequentially or under random command of a person collecting the system's data.

Even though they may be basically analog systems, many of today's control systems are complex enough to require, or at least economically justify, internal loops that contain digital computing equipment. The sequential scanner and voltage-to-digital converter provide a means of collecting and distributing to the digital equipment system information that has been converted from voltage signals. The scanning in these systems may be under a system command or under the computing equipment's command.

The analog-to-digital converter of an indicating or recording system will be about the same kind of device as the converter of a control system; however, the control system may require a converter that makes conversions more rapidly than is necessary for indicating and recording purposes. Also, it may be desirable to use different converter output codes for the two purposes. For example, the computer may be supplied with binary inputs, whereas indicating and recording equipment often requires an input code that is separated

into digits, an example of which is the 1-2-4-8 binary coded decimal code.

Definitions of Functional Performance Characteristics

The following definitions provide a basis for specifying the quality of the performance of a voltage-to-digital converter. In some instances, the definitions conform to the terminology of a set of tentative analog-to-digital converter specifications that has been prepared by members of the AIEE's Component Specification Committee.[1]

1. Full scale: the maximum value of a positive or negative input or output quantity.

2. Full range: the maximum value of positive and negative full scales.

3. Code: the relationship between the converter's quantized output and the value of the continuous input they represent.

4. Count: the digital output reading of the converter, one count is one quantum of the output.

5. Conversion time: the time required for making one voltage-to-digital conversion.

6. Quantization error: is that part of an output quantum(s) that is not discernable between successive output numbers. The quantization error is at least one-half count. (See Figure 1).

7. Offset error: a fixed voltage offset when referred to the converter's input, after correcting for quantization error (see figure 2).

8. Noise error: variation in conversions due to stray coupling to magnetic and electrical signals and due to inherent electrical noise of components.

9. Gain error: the discrepancy between ideal and actual full scale values after correcting for quantization, offset and noise errors (see figure 3).

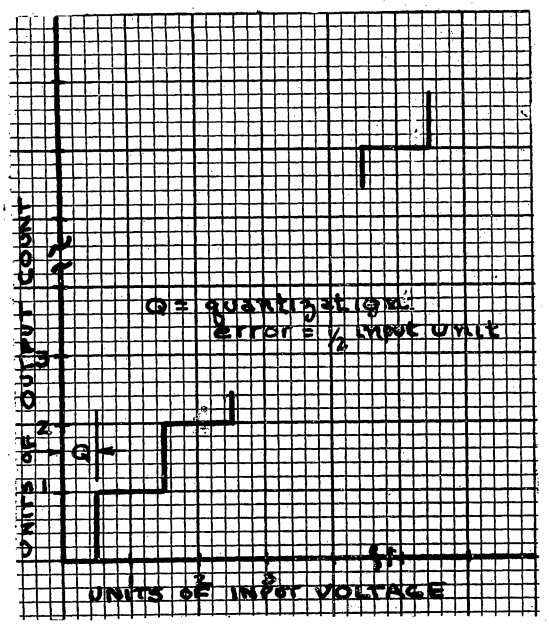


Figure 1. Quantization Error

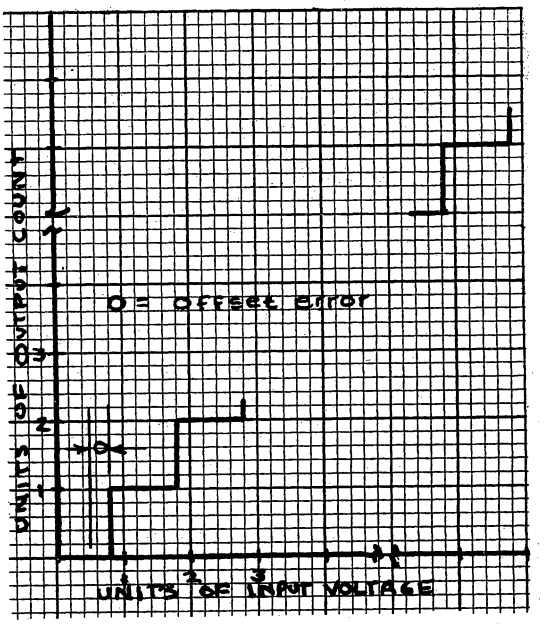


Figure 2. Offset Error

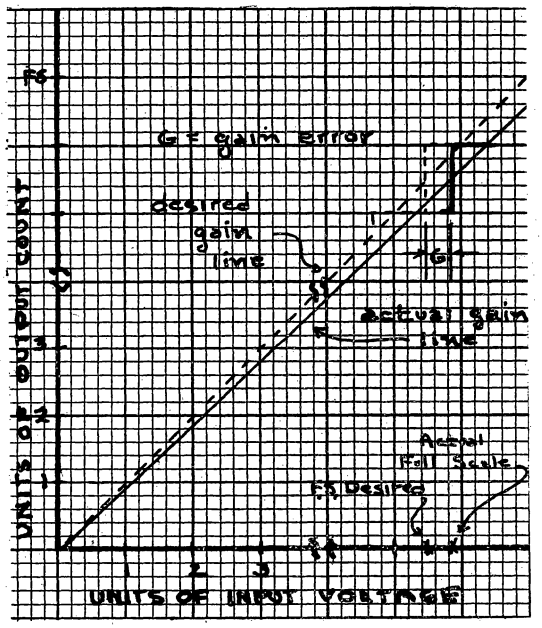


Figure 3. Gain Error

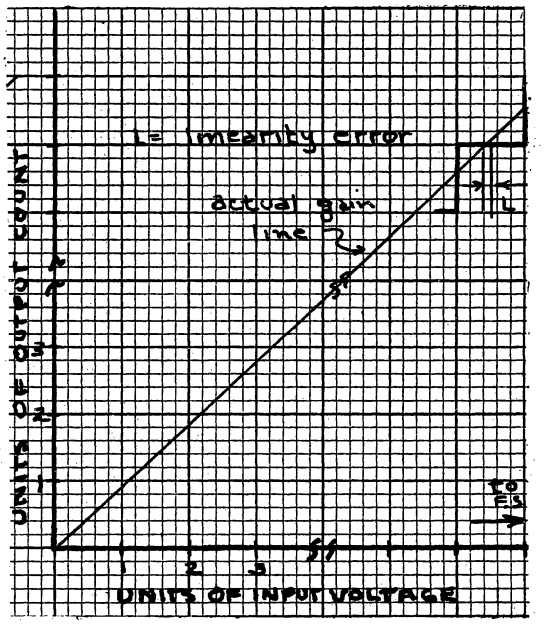


Figure 4. Linearity Error

10. Linearity error: is the difference between the actual input quantity at which a change in count occurs and the input quantity that would have caused the change if the change had occurred on a straight line between zero and full scale value after correcting for quantization, offset, noise and gain errors (see figure 4).

11. Deviation: is specified separately for various performance items. Deviation states the change in offset, gain, etc., that may occur because of a change in operating conditions.

Functional Specifications for Voltage-to-Digital Converter Design

The following specifications are applicable to the converter to be designed:

1. Input voltages: ± 20 volts full scale (40 volts full range) and ± 10 volts full scale (20 volts full range)

2. Input impedance (minimum): 10,000 ohms, resistive, for 20 volts full scale and 5,000 ohms, resistive, for 10 volts full scale

3. Source impedance: zero ohms maximum for specified performance

4. Output count: 4,000 full scale with 95 overrange

5. Output code: natural binary for negative input voltages; 2's complement of natural binary for positive input voltages

6. Type readout: parallel for 12 bits plus sign

7. Voltage levels output: "1" is ± 5 to ± 12 volts
"0" is 0 to 0.4 volts

8. Environment: a. operating temperature: 0°C to 70°C
b. rate of change of temperature: 15°C per hour
c. long term time: six months after initial two weeks

9. Conversion time: 0.6 millisecond

10. Quantization error: ± ½ count due to digital resolution

11. Offset and noise error: less than $\leq$ .005% of full scale at 25°C

12. Offset deviation: less than .01% of full scale in the environment of specification #8

13. Gain error: less than .02% of full scale at 25°C (gain is count/volt, with volt as defined by National Bureau of Standards, Washington, D.C.)

14. Gain deviation: less than .02% of full scale in the environment of specification #8

15. Linearity error: less than .01% of full scale in the environment of specification #8

16. Component type: principally solid state, semiconductors are to be silicon

17. External power available: a. $\leq$ 50 volts $\leq$ 1%
b. $\leq$ 28 volts $\leq$ 7%
c. logic power
(voltage tolerances include line and load regulation, and deviation due to environment per specification #8)

II REVIEW OF LITERATURE

Three types of literature were of importance for the design work presented in this thesis.

The first concern of the designer was to establish a means of accomplishing voltage-to-digital conversion. At least one book and several magazine articles were available on the subject of voltage-to-digital conversion techniques. These are used as references for Section III of this thesis.

The next concern was to design circuits that permitted implementing a selected conversion technique. Circuit design theory and component operating theory from textbooks, periodicals, and manufacturers' application notes were invaluable in this phase of the design work. In addition, the circuit design work has required liberal use of manufacturers' specifications on numerous components. In general, specification literature has not been referenced in the thesis. In many instances the component characteristics are sufficiently known to make referencing unnecessary. In other instances component design tolerances are listed in the thesis and, in some cases, identification of components, such as semiconductors, by their type number will provide an automatic reference to nationally registered specifications.

III TECHNIQUES FOR VOLTAGE-TO-DIGITAL CONVERSION

Introduction

This section presents several basic voltage-to-digital conversion techniques that seem to have been, or seem to be, popular methods of accomplishing linear voltage-to-digital conversions. Variations of these techniques and other methods are being used for voltage-to-digital conversion. References to some of these techniques are given in the Literature Examined section of this thesis.

"Anodige" Converter

The "Anodige" converter apparently takes its name from the prime words of its function, analog and digital. The converter was developed by the National Bureau of Standards and publicly documented by them in 1951, according to Suskind.[3] The "Anodige" block diagram of figure 5 is quite similar to that given by Suskind.[3]

To understand how the converter operates, assume that an input voltage is present and that a "start conversion" command is given. The "start conversion" command causes the counter and the staircase generator to be respectively reset to zero count output and zero voltage output. Following the resets, the logic causes one of the gate's inputs to be enabling. Pulses from the oscillator are accumulated in the counter and simultaneously they cause a staircase type of voltage incrementing of the staircase generator's output voltage. When the staircase voltage is approximately equal to the

input voltage, the comparison circuit's output changes state. Upon this change of state, the gate becomes inhibited by logic that senses the change of state of the comparison circuit and then removes the initial enabling logic signal.

"Sawtooth Comparison" Converter

A block diagram of the "sawtooth comparison" voltage-to-digital[4] converter is given in figure 6. This converter differs from the "Anodige" in that the latter compares its input voltage to a feedback voltage quantity to determine its comparison null while the former compares its input voltage to a voltage-time reference quantity to obtain its comparison null. The reference voltage-time quantity is a voltage that increases linearly with time. During the time that the comparison circuit detects a reference that is less than the input voltage, oscillator pulses of a known frequency are gated to, and accumulated in, the converter's counter. The number of pulses accumulated in the counter will be directly proportional to the oscillator's frequency and the time during which the oscillator pulses are gated to the counter. The counter will cease to receive pulses when the reference voltage equals the input voltage, thus the period of time that the counter receives pulses is determined by the input voltage and the time rate of change of the reference voltage. With constant oscillator frequency and voltage reference, the converter's stored data will be proportional to the input voltage when a conversion cycle has been executed.

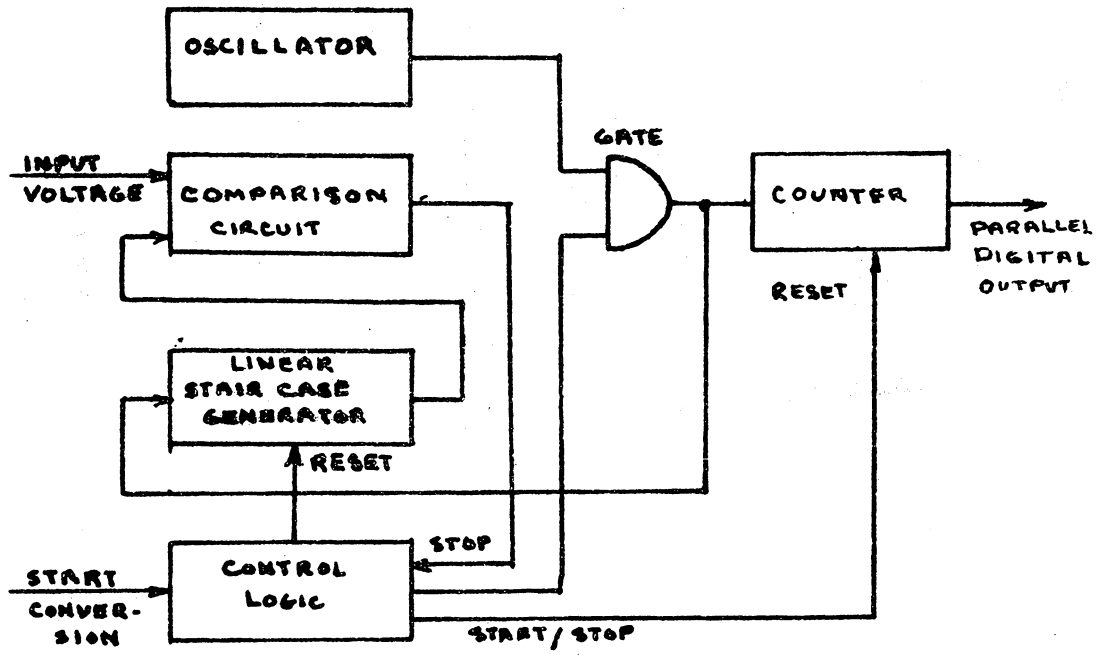


Figure 5. Block Diagram of the "Anodige" Converter

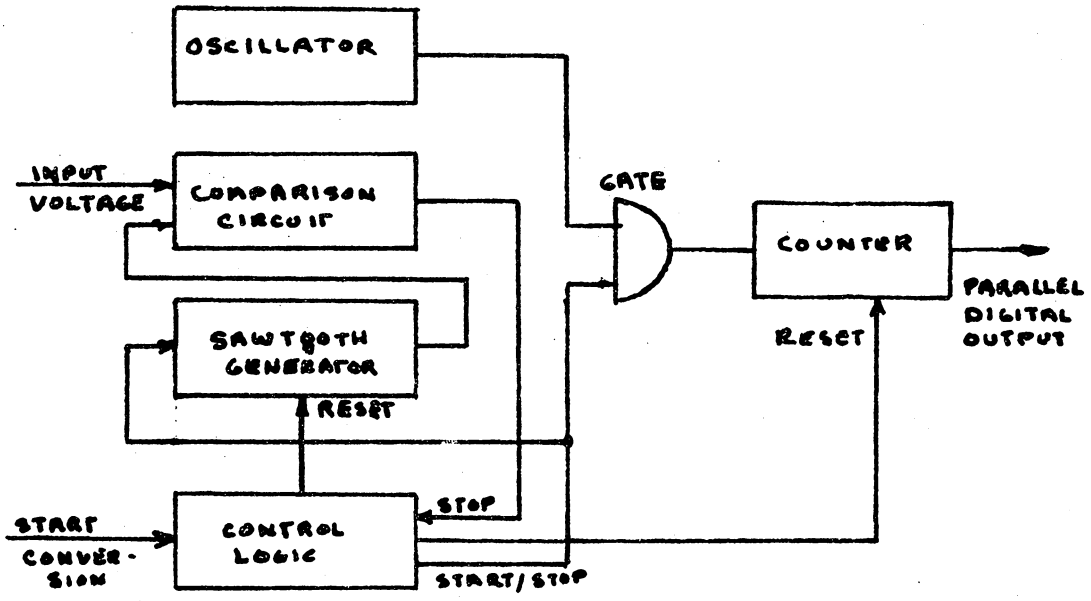


Figure 6. Block Diagram of The "Sawtooth Comparison" Converter

Counter Decoding Converters

The converter shown in figure 7 is similar to the "Anodige" converter. The basic difference is in the method of feeding back to the comparator, a voltage that has been derived from digital-to-voltage decoding. The "Anodige" fed back an analog voltage that was derived from digital pulses. The converter of figure 7 feeds back a voltage that has been derived from data that has been accumulated in its counter. Quite likely, the decoder will change the counter's data to a proportional voltage with a resistive network.

Wald[5] presents a converter that is similar to the one of figure 3. This converter uses a resistive network for its digital-to-voltage decoding.

Platzek, Lewis and Mielke[6] provide a converter that will continuously track its input voltage. This converter is illustrated in figure 8. Its comparison circuit gates oscillator pulses to a reversing counter in a manner that will cause the counter's data to increase or decrease, depending on the relationship of the decoder's output voltage to the converter's input voltage. The counter's data will be increased when the input voltage is greater than the decoder's output, and the counter's data will be decreased when the input voltage is lower than the decoder's output voltage.

"Successive Approximation" Converter

The voltage-to-digital converters that have been described thus far formulate their digital output one quantum at a time. These

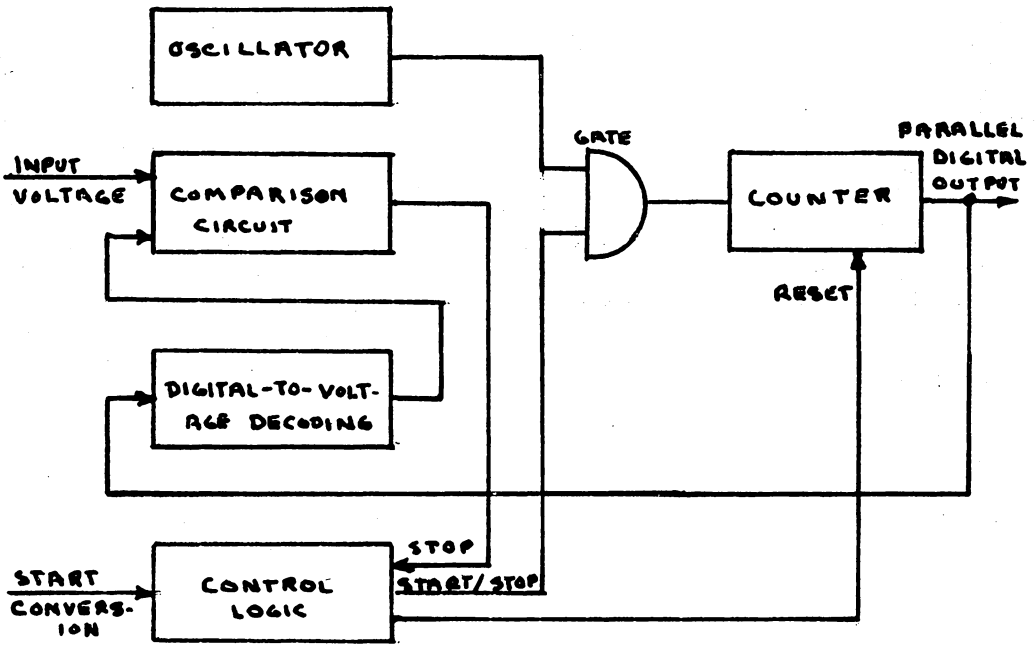


Figure 7. Block Diagram of a Counter Decoding Converter

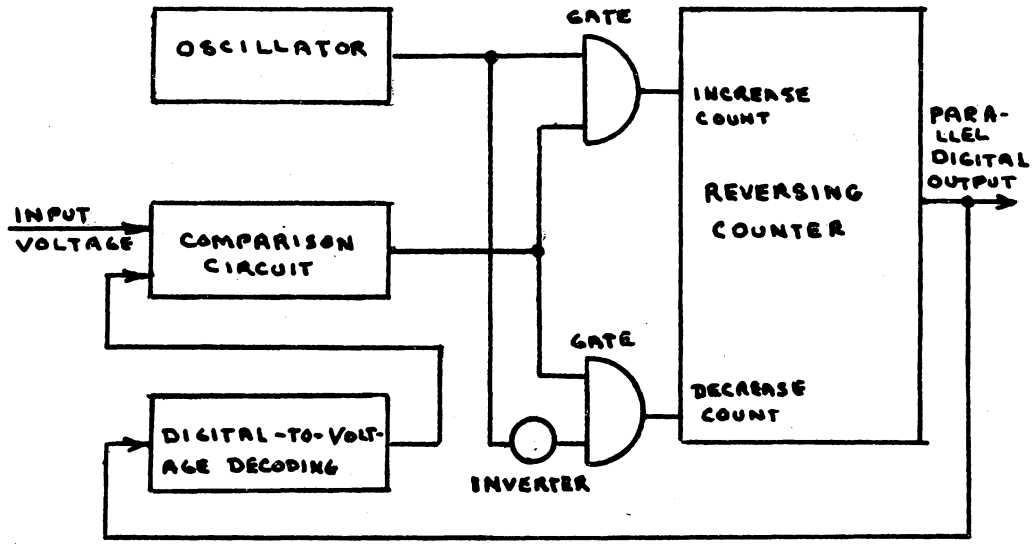
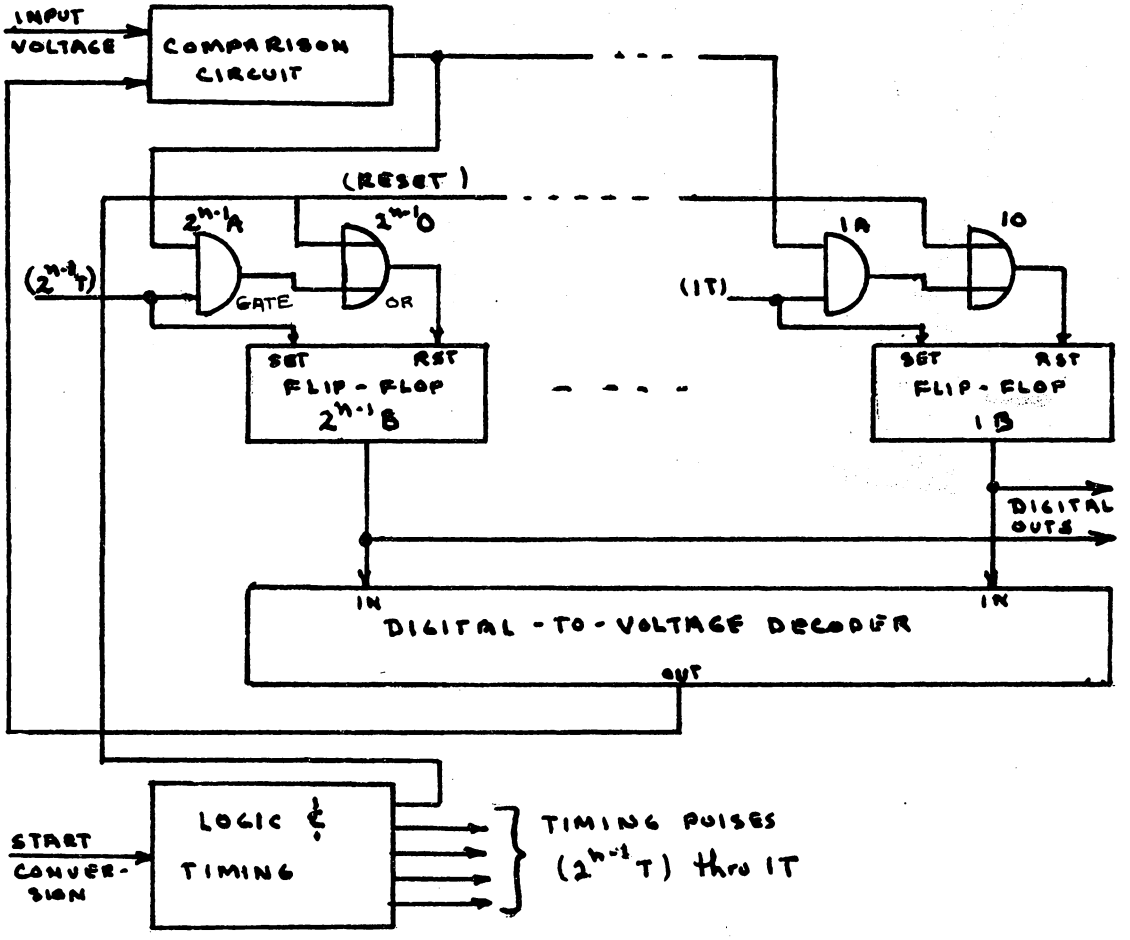


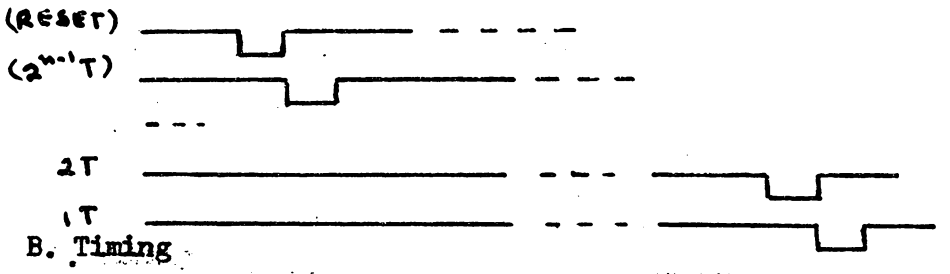
Figure 8. Block Diagram of a Continuous Tracking Converter

converters will perform one thousand operations for a full scale conversion with one-tenth per cent resolution. A converter with one-tenth per cent resolutions has ten binary bits (1024 combinations including zero) of binary information. The most heavily weighed bit of a ten bit binary number is the bit with a 512 weight. All of the nine remaining bits have a maximum combined weight of 511. Similarly the maximum combined weight of all bits of lower order than any particular bit, b_n, of a binary number will be one less than the weight of b_n. This arrangement of weight can be conveniently used to increase the operating speed of a voltage-to-digital converter. Wald[7] provides a description of a converter that illustrates the manner in which the faster conversion can be accomplished. Wald classifies this type of converter as a "digit-at-a-time" converter. This classification is appropriate enough, but if sales literature is used as a guide, a more common name seems to be "successive approximation."

Figures 9a and 9b accompany the following description of the "successive approximation" voltage-to-digital converter. Assume that an input voltage is present at the converter's input and assume that a "start conversion" command has been given. The "start conversion" command causes the generation of the series of pulses shown in figure 9b. First the digital data flip-flop (hold or storage devices) are reset and the decoder's output goes to zero. The comparison circuit's output has a polarity that is enabling to the gate circuitry



A. Block Diagram



B. Timing

Figure 9. The "Successive Approximation" Converter

when the converter's input voltage exceeds the decoder's voltage. Following the reset pulse, flip-flop $2^{n-1}B$ is set by pulse $2^{n-1}T$. This energizes the most significant bit of the decoder. If this bit has a voltage that is less than the input voltage, then pulse $2^{n-1}T$ is inhibited from energizing gate $2^{n-1}A$. If the $2^{n-1}B$ bit causes a decoder voltage that is greater than the input voltage, then pulse $2^{n-1}T$ passes through the "or" unit $2^{n-1}O$ to reset flip-flop $2^{n-1}B$. Following one of these two operations, $2^{n-2}B$ is set and the procedure is repeated until flip-flop 1B has been set (and possibly reset as required by the output of the comparison amplifier). By the time that operation is complete at 1B, the decoder output voltage has been forced to be equal to or not more than the equivalent of one bit weight of voltage less than the input voltage. The one bit excess of voltage can be reduced to one-half of a bit by biasing the decoder's output voltage with one-half of a bit's quota of voltage with a polarity that is the same as the input voltage. The complete conversion has been made in 10 steps (11 including the initial reset) and if the circuit time constants are low enough, the "successive approximation" converter's conversion time can be much less than that of the "quantum-at-a-time" converters.

Cascaded Bit Converter

Figure 10 illustrates a converter that should be faster than the "successive approximation" converter.[8] The converter requires a comparison circuit, an analog switch, and a subtractor with a gain of

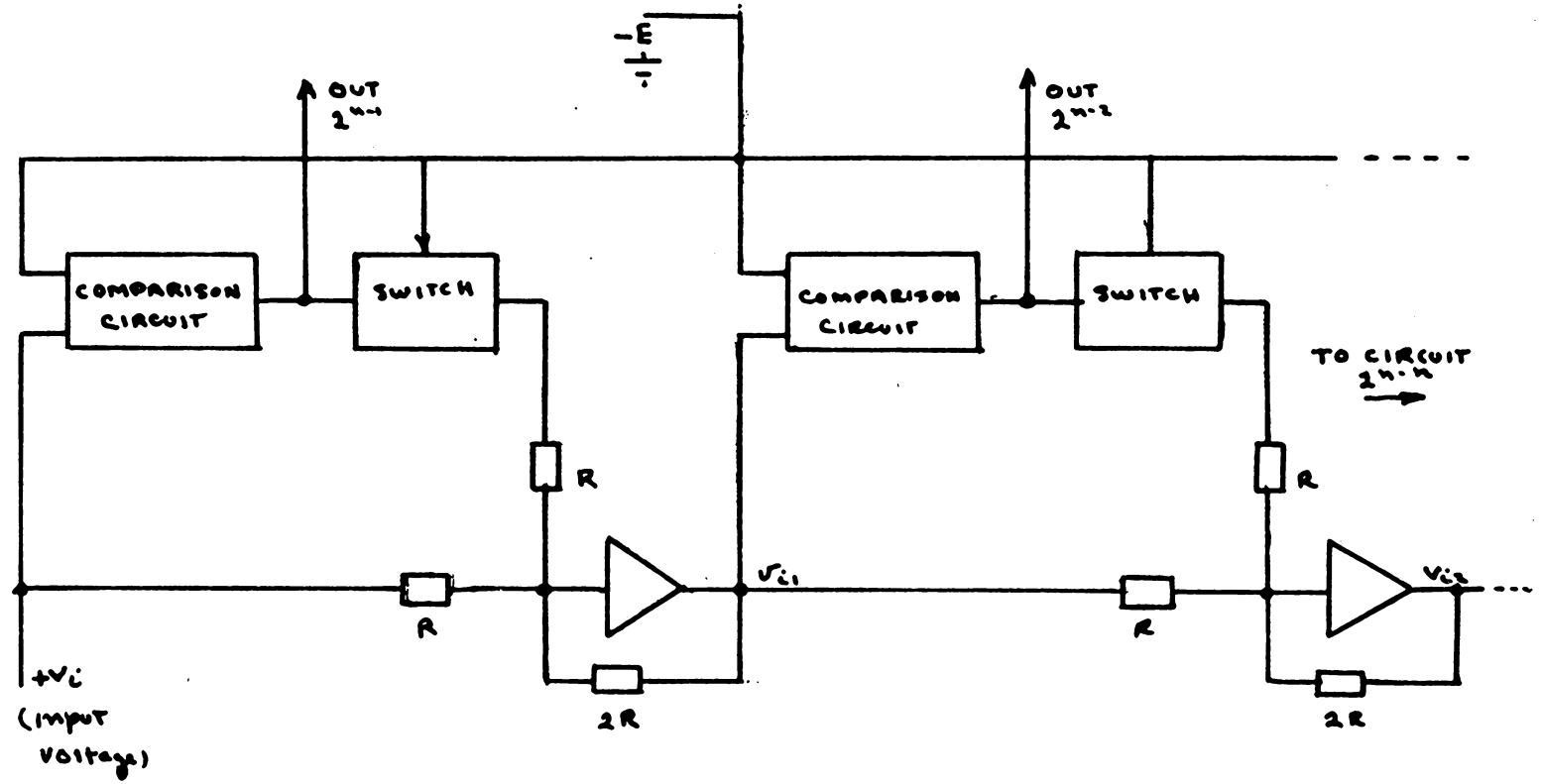


Figure 10. Block Diagram of Cascaded Bit Converter

two for each of its bits. The switch of each bit circuit has (-E) volts out when the V_i into its comparison circuit is greater than [-E] and zero volts out otherwise, where the converter's full scale input voltage, V_i', is selected such that:

$$V_i' = |-E| (2^n-1)/2^{n-1} \qquad \text{III-1}$$

n= number of converter bits

The converter outputs a "1" when the switch of a bit outputs (-E) volts.

The conversion time of the cascaded bit converter is limited by the time required for the various bit signals to propagate through the comparison, switch, and subtractor circuits.

Voltage to Frequency Converter with Period Counter

A voltage-to-frequency converter outputs a digital pulse train with a frequency that is directly proportional to its input voltage. The digital pulses can be accumulated in a period gated counter to provide a digital number, the size of which is determined by the frequency that is input to the counter and the length of time (period) for which the input was permitted. If the period is known, then the number stored in the counter can be interpreted in terms of counter input frequency and thus, converter input voltage. Figure 11 provides a block diagram of such a system. The output of the period logic is enabling during the period timing and inhibiting at other times.

Figure 12 presents a block diagram of a voltage to frequency converter that is manufactured by the Hewlett Packard Company.[9,10]

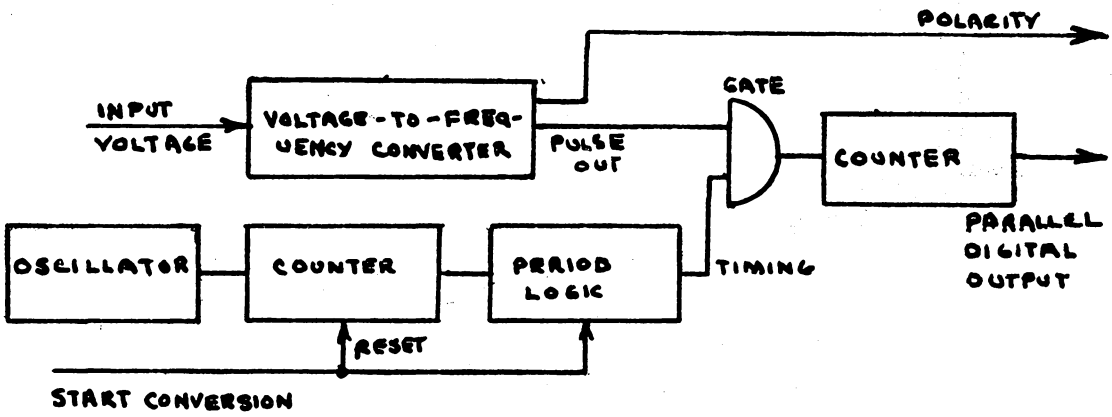


Figure 11. Block Diagram of a Voltage-to-Digital Converter with Internal Voltage-to-Frequency Conversion

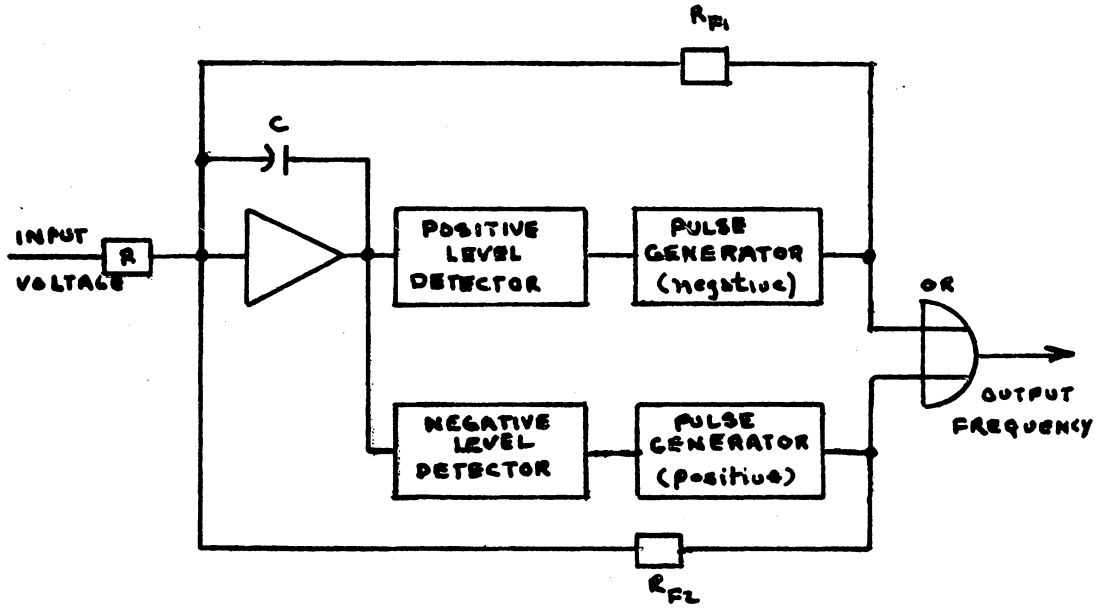


Figure 12. Block Diagram of Voltage-to-Frequency Converter

The converter's input voltage is integrated by an operational amplifier type of integrator and when this integrator reaches a predetermined level, a pulse generator feeds a pulse to the integrator's input. This pulse has a fixed voltage-time product and a polarity opposite to that of the input voltage. If the integrator time constant and the predetermined level also have fixed values, then the converter's output frequency can be determined as follows:

$$V_L - V_X = V_i t_X / \tau_I \qquad \text{(at the end of a feedback pulse)}$$

when V_L = constant voltage level
V_i = input voltage quantity
τ_I = fixed integrator time constant
V_X = voltage quantity that existed at integrator's output at the end of the previous feedback pulse
t_X = time required for integration to level V_L from voltage V_X

$$V_X = V_L + (V_i - V_f)\, T_P / \tau_I$$

T_P = constant pulse width of feedback pulses
V_f = constant amplitude of feedback pulses $|V_f| \geq |V_i|$

$$-V_L + V_i t_X / \tau_I = -V_L - (V_i - V_f) T_P / \tau_I$$

$$V_i (t_X + T_P) = V_f T_P$$

$$t_X + T_P = V_f T_P / V_i$$

now $(t_X + T_P) = 1/f$ where f is the frequency at which the integrating cycle will repeat, therefore:

$$f = V_i / V_f T_P \qquad \text{III - 2}$$

The integrating voltage-to-frequency converter can be used in a manner that will give excellent rejection of certain noise frequencies that may be superimposed on d.c. For example, suppose that the period over which the counter is accumulating has been fixed

at one-tenth of a second. Noise of 10, 20, 30, 40, 50, etc., cycles-per-second frequencies will be presented to the converter for an exact and even number of positive and negative half cycles. The output frequency of the converter will vary with the noise but the converter will accumulate as many high frequency pulses as low frequency pulses and the noise will be averaged out of the d.c. signal. If the positive and negative half cycles of noise are symmetrical, as might well be the case with 60 cycle power noise, the noise component of an input signal can almost be completely eliminated.

With its single output, the voltage to frequency converter can be easily isolated from digital elements that it might output to. If the power supplies of the converter are also isolated, then the complete converter is easily isolated from a system's common or ground. The common mode rejection of a voltage to digital converter is greatly improved by isolating its analog section. High common mode rejection is frequently a necessity in systems that collect data from remotely located sources.

The conversion time of the analog to digital converter illustrated in figure 11 is a function of the voltage to frequency converter's output frequency, the desired resolution of converted data and the noise frequencies that are to be rejected by the averaging procedure previously described.

Summary

Excluding the "sawtooth" and "cascaded" converters, all converters discussed in this section accomplished their conversion by comparing an input quantity to a feedback quantity that the converter had generated in a preorganized manner. The "sawtooth" and "cascaded" converters are open loop devices with a stable reference. The converters accomplished their conversion in one of the following manners:

1. one quantum at a time.
2. about fifty per cent of all untried quantums at a time.
3. with a voltage-to-frequency intermediate conversion.

IV SELECTION OF VOLTAGE-TO-DIGITAL CONVERSION TECHNIQUE FOR DESIGN

The previous section presented several techniques that have been used in voltage-to-digital conversion. The specifications (see Section I) for the converter design require that a 4000 count conversion be made in 600 microseconds. One counter increment and one voltage comparison are required each 0.15 microseconds during the conversion when the conversion is made one quantum at a time. It is difficult to count, let alone count and compare at this speed, thus the "quantum-at-a-time" technique seems like an impractical method of satisfying the converter's specifications. With the voltage-to-frequency conversion technique, the integrator's output will have to be about seven megacycles per second and this seems to be an extremely excessive integrating rate. The "successive approximation" technique must achieve its converted output with one flip-flop set/reset operation and one voltage comparison each 50 microseconds during the conversion. This seems like a reasonable operating time and in lieu of the elaborateness of the faster, "cascaded bit" converter, the "successive approximation" conversion technique was selected as the technique to be used for the specified converter's design.

The most apparent disadvantages of selecting the "successive approximation" technique are that it requires more digital logic than the counting techniques and it does not have the noise removal

features of the voltage-to-frequency approach to conversion. If necessary, high frequency noise can be removed from the "successive approximation" converter's input with input filters and low frequency noise can be removed from the converter's output by digital smoothing if the system that the converter is used in has a low enough frequency response characteristic. Digital smoothing requires additional digital equipment, but this is frequently available in systems that have voltage-to-digital converters. The design of the "successive approximation" converter could include an isolated analog section but isolation can probably be more easily accomplished with an external isolating amplifier.

Besides conversion rate, the "successive approximation" converter has an advantage over the voltage-to-frequency apparatus in that the former converter's decoder can be used as a separate circuit for digital-to-analog conversion applications if it is so designed.

V BASIC DECODING, COMPLEMENTING, AND COMPARING TECHNIQUES AND CIRCUITRY

Introduction

The object of this section is to present an examination of techniques and circuits that can provide the "successive approximation" converter's decoding, complementing, half-count offset and comparing functions. An analysis of several decoding techniques reveals that one type of decoder circuit can be made to decode with less gain error and non-linearity than others. Further analysis shows that the output of this decoder is quite compatible with a technique that is well suited to the design of the converter's complementing, offsetting and comparing circuits.

To some extent, the cause and amount of errors and deviations in a "successive approximation" converter can be analyzed without much knowledge of the converter's circuitry. The results of the analysis should be an aid in defining the characteristics of the techniques and circuits that can best satisfy the requirements of the converter.

Thermal emfs and error in the half-count bias are two sources of offsets in the converter. The comparison circuit is essentially a bistable, signal polarity detector. A circuit of this nature inherently has some deadband and this deadband can be offset from a desired operating level. The deadband and its undesired offset contribute to the converter's offset. The decoder can have other offsets that are not predictable without further knowledge of the

circuit. Electrical noise in either the decoder or comparator will have to be overcome by the converter's input signal as sensed at the input of the comparator. Unfiltered noise will have an effect similar to an increased comparator's deadband and filtered noise can have an effect similar to offsetting the comparator's deadband.

The decoder causes part of the converter's gain error, and inaccurate transfer of the converter's input and decoder signals for comparison, causes the remainder of the gain error.

Both the decoding and comparison circuitry can cause linearity errors in the converter. The nature of non-linearity in the decoder is not predictable without more knowledge of the technique or circuit involved. The comparison circuitry can cause linearity errors by failing to recover from large differences between input and decoder signals in time to detect a small difference between the two signals. To satisfy a 0.6 millisecond conversion time, the converter requires a comparison operation each 50 microseconds or so. Lack of recovery can cause converted outputs such as "257" to be correct, "001" to be correct and "256" to be incorrect. The error occurs because the comparison at "256" lacked settling time and the difference in time between comparing "256" against the input and "256" plus "001" against the input is long enough to permit the comparator to settle. A tenth of one count is .0025% of a 4000 count conversion. A .0025% maximum error requires that the comparator detect the difference between the converter's input and decoder signals to a difference of

one part in 40,000 of its maximum input. Further, the comparator must be able to detect this difference within 50 microseconds after having sensed up to 20,000 parts of difference between the input and decoder. It will be shown later than bipolar converters can have inputs to the comparator that are greater than 20,000 times the signal it must detect during the next comparison operation. If an unattenuated input signal is compared with the decoder signal, the comparator will have to operate properly from a signal that is less than 250 microvolts (10 x (1/40000) volts) if the non-linearity is not to exceed .0025%. The signal will be less if the input signal is attenuated before it is compared to the decoder's signal.

Even though complementing has hardly been considered, it is obvious that there will be circuit problems in designing a converter with .005% offset error, .02% gain error and .01% linearity.

There will also be problems associated with maintaining .01% offset deviation and .02% gain deviation with linearity error that does not exceed .01% during the varying environment and time span of the specification.

Humidity, temperature change, and natural long term characteristics affect the chemical and physical properties of the converter's components to cause the converter's deviations. Temperature can be assessed in terms of its effect per degree centigrade of change. An ambient that varies from 0°C to 70°C will require for each $\leq$.01% of deviation, that the deviating characteristic have a temperature

coefficient that is about .0002% per degree centigrade in the 25°C to 70°C ambient and a temperature coefficient that is about .0004% per degree centigrade in the 25°C to 0°C ambient. Semiconductor devices are not particularly stable in an ambient that varies so widely, thus a large part of the specified offset and gain deviation may be allocated to temperature drift. Even so, the deviation specifications are stringent enough that the temperature of some of the circuitry will almost undoubtedly require temperature compensation or an environment that has much less than seventy centigrade degrees of change. A controlled circuit temperature can be provided in specially designed enclosures.

Decoding

The function of the decoder is to accept a digital input and then output an analog quantity that is linearly proportional to the digital input. The analog output must have a magnitude and polarity such that the full scale decoder output can be compared with the full scale converter input to generate a null that indicates that the conversion has been made.

The specifications require that the converter's input be a voltage quantity. Without justification, it seems reasonable to assume that the simpliest decoding and comparing will be accomplished electrically and accordingly energy conversion techniques are excluded for the decoder discussion that follows.

Figure 13 illustrates a circuit[11] that accomplishes decoding of

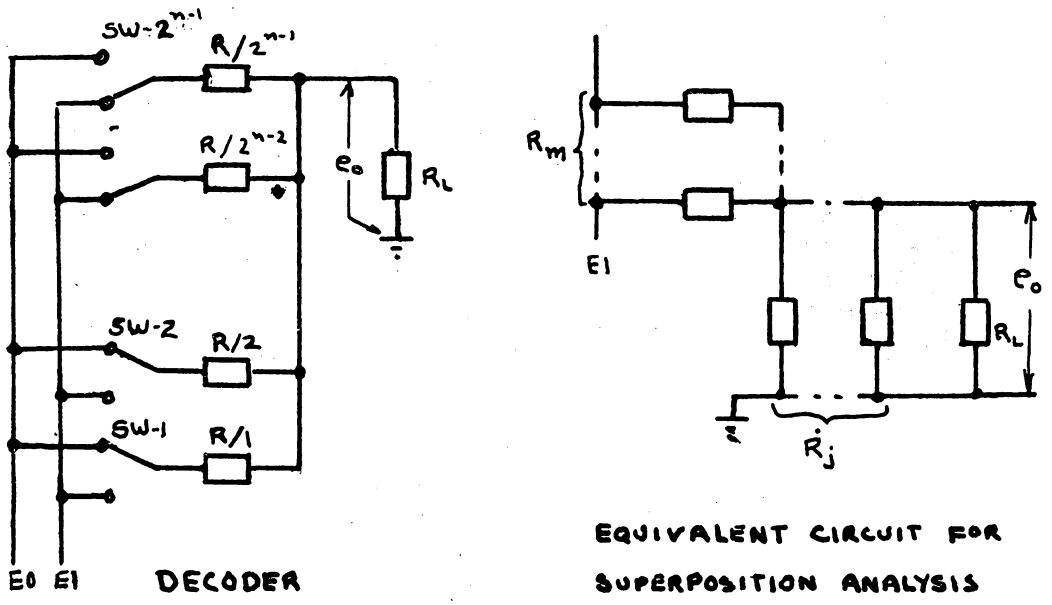


Figure 13. Weighted Resistor Decoder

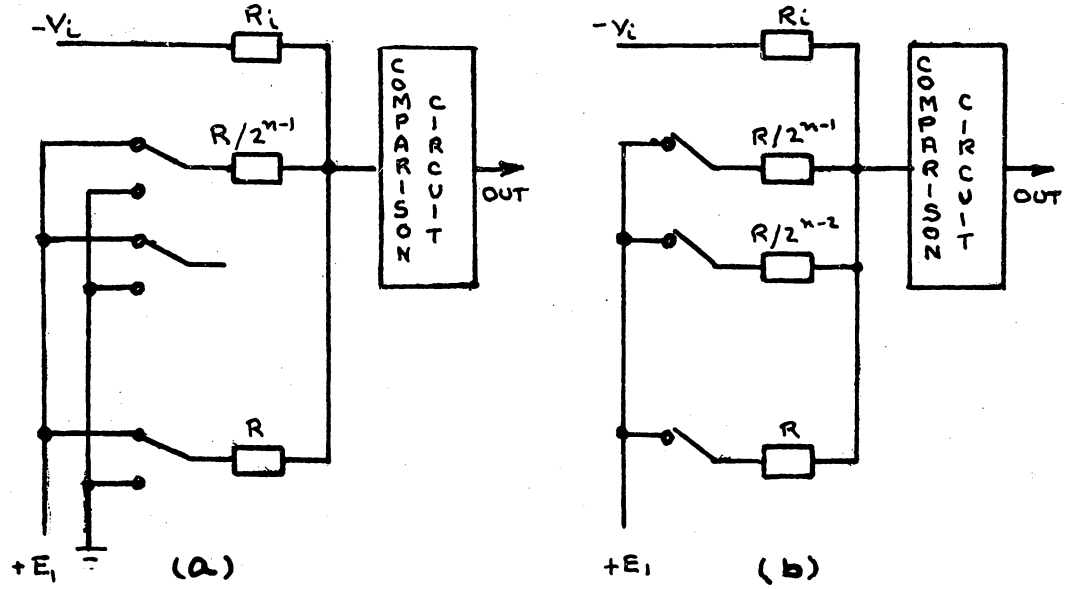


Figure 14. Decoding and Comparing with Current Weighted Resistive Circuits

a digital number by a voltage division technique. The digital input is from a single pole, double throw switch. The two switch positions are the two binary states of the input. Using superposition, the circuit can be analyzed as follows:

Assume that $E_0 = 0$ volts = common voltage; e_{oa} the decoder's output voltage:

$$e_{oa} = E_1 \frac{\frac{1}{1/R_L + \Sigma 1/R_j}}{\frac{1}{\Sigma 1/R_m} + \frac{1}{1/R_L + \Sigma 1/R_j}} \qquad V-1$$

where $\Sigma 1/R_m$ = equivalent admittance of resistors connected to voltage E_1

$\Sigma 1/R_j$ = equivalent admittance of resistors connected to voltage E_0 ($E_0 = 0$ for superposition purposes)

$$e_{oa} = E_1 \frac{\frac{1}{1/R_L + \Sigma 1/R_j}}{\frac{1/R_L + \Sigma 1/R_j + \Sigma 1/R_m}{(\Sigma 1/R_m)(1/R_L + \Sigma 1/R_j)}}$$

with binary weighed resistors as shown in figure 13:

$$\Sigma 1/R_j + \Sigma 1/R_m = \sum_{k=0}^{n-1} 2^k/R = 1/R \sum_{k=0}^{n-1} 2^k$$

$$\Sigma 1/R_m = \sum_{m=0}^{n-1} 2^m/R$$

but m exists only for resistors connected to E_0

$$= P/R$$

where P = binary number to be decoded if E_1 is the "1" or true binary input connection voltage.

now: $1/R \sum_{k=0}^{n-1} 2^k/R = 1/R \left(2^0 + 2^1 + \cdots 2^{n-1}\right)$

$$= 1/R \left(2^n - 1\right), \text{ then}$$

$$e_{oa} = \frac{E_1 P R}{1/R_L + 1/R\,(2^n - 1)} = \frac{E_1 P}{R/R_L + 2^n - 1}$$

Now if e_{ob} is the decoder's output voltage with $E_1 = 0$ volts

$$e_{ob} = \frac{E_o \Sigma\, 1/R_j}{1/R_L + \Sigma\, 1/R_j + \Sigma\, 1/R_m}$$

$$= \frac{E_o\,(2^n - 1 - P)}{R/R_L + 2^n - 1}$$

$$e_o = e_{oa} + e_{ob}$$

$$e_o = \frac{E_o\,(2^n - 1) + P\,(E_1 - E_o)}{R/R_L + 2^n - 1} \qquad \text{V - 2}$$

Now, e_o will be a maximum when R_L is infinite and e_o will be zero when R_L is zero. A zero R_L is not as useless as it might at first appear. It is obvious from the circuit of figure 13 that if E_o is zero, then the short circuit output current of the circuit is proportional to the digital number being decoded by the circuit. It is also obvious that this current is proportional to the number being decoded even if the E_o voltage is absent, that is, the switches can be made single pole switches. Suskind[12] points out that the voltage deviding network ($R_L > 0$) is not accurate without a second voltage bus. In an unrestricted sense this is true, however, a voltage-to-digital converter provides something of a special application of a decoder in that decoder needs good accuracy only when the converter's input is nulled against the decoder's output. If E_o is made either common voltage or an open circuit, the comparison performance of the circuit of figure 14a and 14b will be the same <u>if the null comparison occurs with common potential</u> at the input of the comparison circuit. There is a difference between the comparisons made with and without

E_o. The decoder of figure 14b has an output resistance that varies inversely as its decoded output while the decoder of figure 14a has an output resistance that is constant and independent of the number it decodes. The comparison circuit may be sensitive to its source resistance.

Figure 15 provides another example of weighted resistor decoding that can be used in a converter's comparison operation if the comparison occurs at ground potential. As in figure 14a, the decoding of figure 15 requires single pole, double throw switching. The decoder of figure 14a acquired a constant output resistance by use of the double throw switching while the decoder of figure 15 acquires constant power supply loading through use of double throw switching. Constant loading of the supply has possibilities of simplifying the design of a decoder's reference voltage supply. Further the decoder of figure 15 keeps constant power on its resistors and thus resistance variation due to "self-heating" change of temperature of the resistor is avoided.

Figure 16 presents another binary voltage dividing decoder. The switch nearest R_L is that of the most heavily weighted binary bit. Switches to the left are successively lower weighted bits. It can be shown[13] by techniques similar to those used in analyzing the decoder of figure 13 that:

$$e_o = \frac{E_1 R_L P}{2^n (R_L + 3/8\, R)} \qquad V-3$$

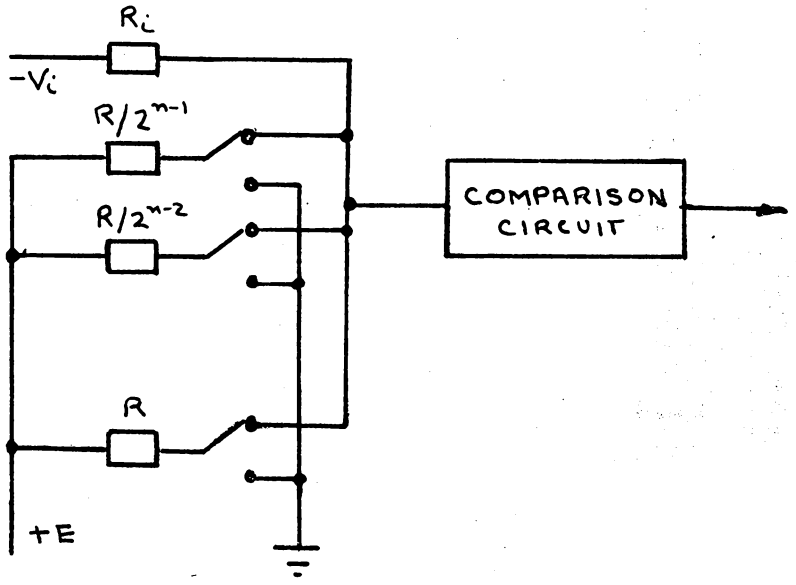


Figure 15. Decoding and Comparing with a Constant Load, Current Weighted Resistive Circuit

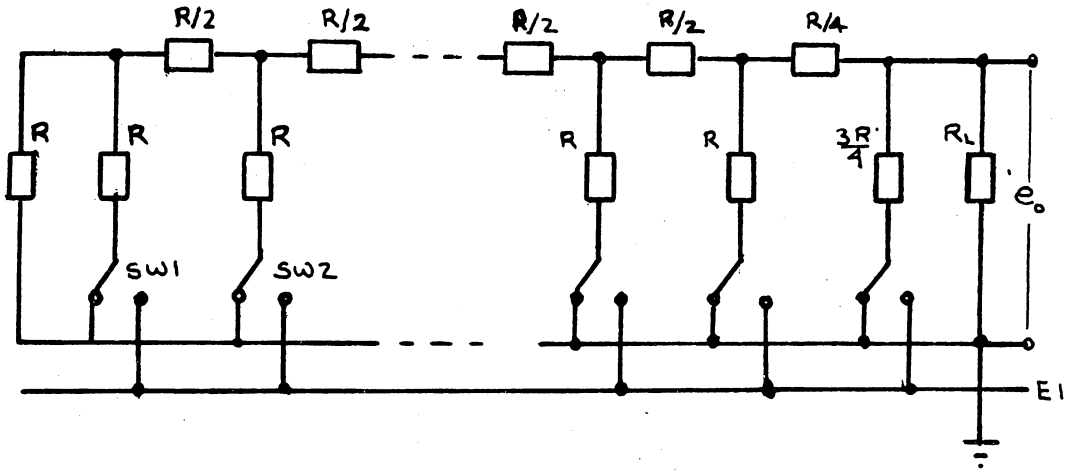


Figure 16. A Resistive "Ladder" Decoder

where P is the binary number being decoded and E_1 is the voltage connected to the input switch when the switch is in its "1" or true position. If the decoders of figures 13, 14, 15, and 16 are to have linearities that are a constant percentage of full scale output, then the resistors associated with the lower weighted bits can be less accurate than those of the higher weighted bits. If the decoders are to have linearities that are a constant percentage of each output, then the decoder of figure 16 might have an economic advantage over the others through quantity purchasing of fewer types of resistors even though there are about twice as many resistors in the converter of figure 16. Also, high ohmic value resistors of good quality are more expensive than low ohmic value resistors. The decoders of figures 13, 14, and 15 can require some high valued resistors if the decoded word has very many bits and if the circuit is not modified from that shown.

Figure 17 provides a decoder circuit with a low output impedance that is obtained from an operational amplifier.[14] The same output impedance could be obtained, if needed, by combining the previously discussed decoders with an amplifier. The decoder of figure 17a, however, loads its reference power supply with a constance current while most of the previous decoders do not. The steady state transfer function of an operational amplifier can be derived with the aid of the simplified circuit of figure 17b, where:

$$E_i'' = E_i / R_i / (R_1 + R_i)$$

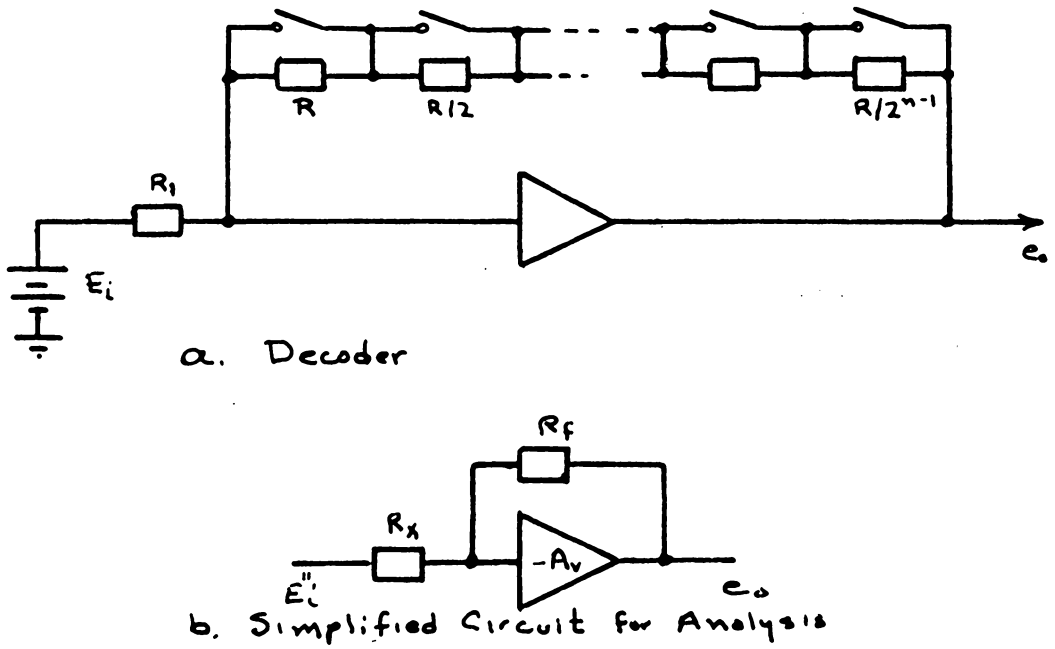


Figure 17. Feedback Amplifier Decoder

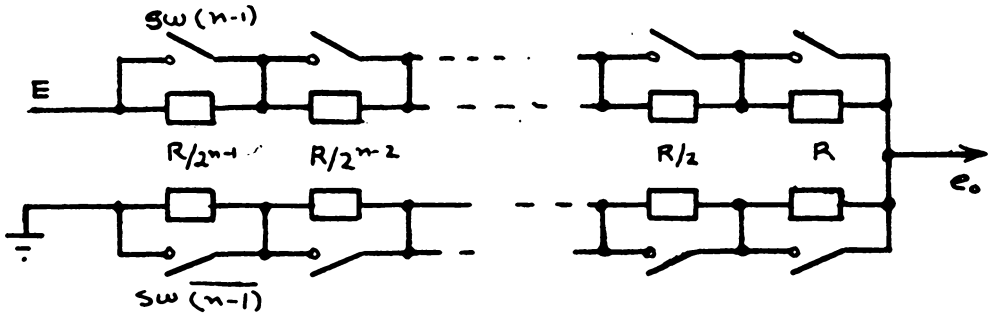


Figure 18. Potentiometric Decoder

R_i = input resistance of the amplifier

Let : $R_x = R_1 R_i / (R_1 + R_i)$, then

$$\left[E_i'' - (e_o + E_i'') \cdot \frac{R_x}{R_x + R_f} \right] A_v = e_o$$

$-A_v$ = steady state, open loop, amplifier gain

$$\frac{e_o}{E_i} = -\frac{R_f}{R_1} \left[\frac{1}{1 - \frac{R_1 R_i + R_f R_1 + R_f R_i}{R_1 R_i A_v}} \right]$$

and if $A_v \gg 1$

$$\frac{e_o}{E_i} \simeq -\frac{R_f}{R_1} \left[\frac{1}{1 - \frac{R_f (R_1 + R_i)}{A_v R_1 R_i}} \right] \qquad \text{V-4}$$

The last equation makes evident that the decoder's output varies directly as R_f. Unfortunately, the gain accuracy and linearity of the decoder are poorest when the decoder is decoding its most significant binary information. The gain accuracy and linearity of the decoder will deviate with deviations in A_v, R_1, R_1, and R_f. The deviation due to A_v and R_i is extra in the sense that they are not present on the previously discussed resistive decoders. The gain range of the amplifier and the range of the decoder are one and the same. For wide range decoding, R_f/R_1 must vary widely. The best gain accuracy and linearity will be had if $R_f (R_1 \neq R_i)/R_1 R_i$ or most probably R_f is made low; however, for a given amplifier, the minimum value of R_f is determined by the higher frequency roll offs of the amplifier if the amplifier is to be non-oscillatory.

Figure 18 provides a decoder that has been used in a "successive

approximation" voltage-to-digital converter.[15] The decoder operates as an incremental potentiometer with switch (n-1) being open when switch $\overline{(n-1)}$ is closed, etc. At first glance the circuit appears a bit complicated but the decoder outputs voltage and loads the reference supply with a constant d.c. load, and the decoder does this without an amplifier or double throw switching. The switching operation warrants further comment. The voltage decoders of figures 13 and 15 require either a single pole, double throw switch or careful sequencing of normally open and/or normally closed interlocks if shorting of the reference power supply is to be avoided. Careful sequencing of the highest order switch of the potentiometric decoder will limit its transient load to a maximum of twice the normal reference load.

An operational disadvantage of the potentiometric decoder is that output loading causes the decoder to be non-linear.

Several decoders have been discussed thus far. Each contains a resistive network and a reference voltage supply. The decoders can be classified by output (voltage or current), output resistance (constant or variable), load on the reference supply (constant or variable), and by switch type (single or double throw). Table 1 summarizes the decoder study by tabulating the decoders in accordance with these characteristics.

Table 1. Comparison of Decoder Characteristic

Type	Figure	Output	Output Res.	Ref. Loading	Variable Self Heating	Switch
weighted	13, 14a	volt./cur.	const.	yes	yes	DT**
weighted	14b	cur.	var.	yes	yes	ST
weighted	15	cur.	var.	no	no	DT**
ladder	16	volt./cur.	const.	yes	yes	DT**
amplifier	17	volt./cur.*	const.	no	yes	ST
potentio-metric	18	volt.	var.	yes	no	2-ST

* if resistor is connected to output

** 2 - single throw (ST) can be used but timing is critical if shorting of reference supply is to be avoided

There are probably many other types of decoding circuits. A decoding circuit can undoubtedly be designed with current supplies and current switching circuits; however, good current supplies are fairly difficult to design, whereas feedback techniques can be used in the design of semiconductor voltage supplies to provide a voltage supply with a low output impedance that is needed to varying degrees by the decoding circuits that have been presented thus far. Accordingly, the decoders considered for the design of voltage-to-digital converter will be limited to those that have voltage references, and further decoder study will be limited to the types of table 1 in the belief that this collection provides a general set of design problems.

Each decoder considered thus far is as inaccurate and unstable as its reference voltage supply is inaccurate and unstable. Inaccuracy of the supply's voltage causes converter gain error. For the most part, the inaccuracy of a supply is caused by having

inaccurate instrumentation with which to set the supply's voltage and/or poor resolution in the circuitry that permits the supply to be set. Deviation of the supply's voltage will cause converter gain deviation and perhaps some non-linearity. The supply deviation is generally caused by deviation of the supply's load and/or internal reference and/or feedback and/or gain and/or d.c. biasing and/or input line voltage. Selected zener diodes can provide internal reference voltage stabilities that are better than .002% per thousand hours with temperature coefficients that are less than .0005% per degree centigrade.[16] Controlling the temperature of the zener reference, feedback elements (generally a resistor network) and a few gain stages following the zener, should give adequate protection against a major portion of the supply's deviation. Deviation due to gain, load and line voltage variation can be made low with a feedback around high gain amplification in the forward loop of the supply.

The decoding circuitry other than the voltage supply affects the supply's accuracy and stability only by the quantity of reference voltage and loading that it requires. The effect of decoder voltage quantity on the power supply performance is not readily appraised but it is certain that larger, non-constant, bit loading on the supply will cause larger decoding non-linearity; however, supply load regulation may well cause less conversion errors than would occur if a converter's decoding circuit was selected on the basis of minimum supply loading. The bit loading on the supply generally occurs in

small steps that usually cause accumulative supply loading as the conversion process is being accomplished. Both transient and steady state loading of the reference voltage supply are important performance factors. It is difficult to evaluate the transient regulation of the supply at this time, but a feel for the steady state regulation can be had by assuming that the output disturbance will be 1/GH of the unregulated disturbance, where GH is the loop d.c. gain of the voltage supply. For a 100% current step (current to cause the supply without closed H loop to drop to zero volts), a GH of 100,000 will cause the supply to have a steady state load regulation of .001%. A GH of 100,000 is not an unreasonable design requirement and with loading that occurs in small steps at 50 microsecond intervals, it would seem reasonable to estimate that a voltage supply can be designed with transient and steady state line regulation that causes little linearity error. The specifications require that the decoder have a gain accuracy, and a gain deviation, each less than .02%, and a linearity error less than .01%. A voltage supply can probably be designed to be compatible with these specifications if the design of the remaining decoder circuit is reasonable.

The ideal switch for a fast, highly accurate decoder is difficult to find. The high open impedance, and low closed impedance that provides good accuracy can be had with relays, but the speed requirement of a converter comparison each fifty microseconds is not compatible with relay operating time. The switching speed of

semiconductor transistors and diodes is compatible with the converter's speed requirement. By giving careful consideration to the transistors' and diodes' open and closed characteristics in conjunction with the decoder's circuit, the semiconductor switch can be decently applied in decoding circuits. In addition to fast operation, the semiconductor switch can without wearout provide many more operations than a mechanical switch. This is certainly desirable since a fast operating decoder may be required to provide many operations during its useful life.

The diode can be considered a high impedance device when it is reverse biased and a low impedance device when it is forward biased. Figure 19 provides equivalent d.c. circuits for a forward and reverse biased diode.[17]

In general, R_{op} of figure 19 can be considered a very high resistance that represents the leakage resistance of an "open" switch. R_{cl} can be considered to be a low resistance that represents the resistance of a closed switch. I_{op} and V_{cl} are respectively low current and voltage sources.

The transistor can be considered a high impedance device when it is biased for cut-off operation and a low impedance device when it is biased for saturated operation. Figure 20 presents a simplified equivalent circuit for a cut-off transistor and a saturated transistor with normal emitter-base bias and collector load current. In addition, figure 20 presents an equivalent circuit for a saturated

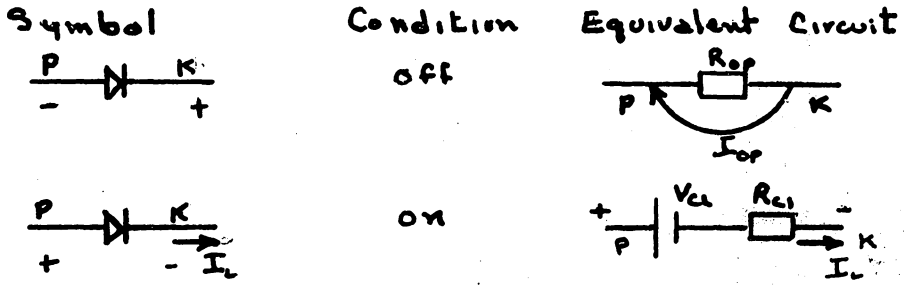


Figure 19. Semiconductor Diode with Equivalent Circuits

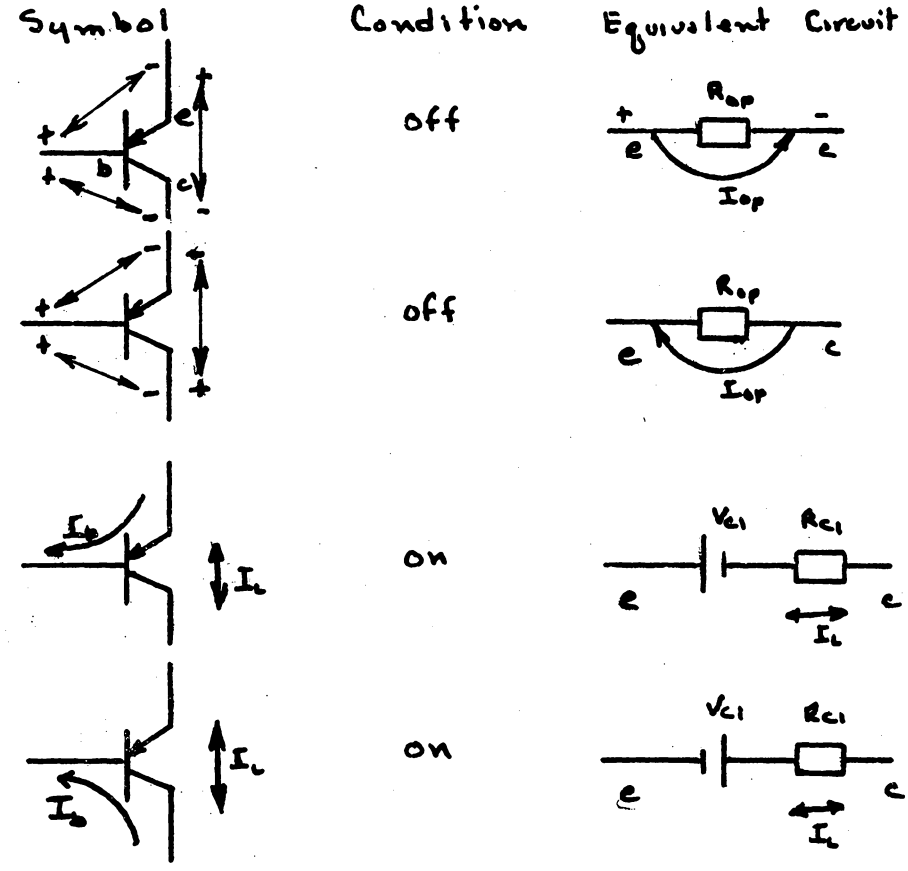


Figure 20. Transistor with Equivalent Circuits

transistor that operates with a collector-base current bias and emitter load current. This connection is inverted from the normal connection and the reason for its being shown will be provided later. The equivalent circuits of the saturated transistor are given with the assumption that the base currents of the transistor are constant for given circuit parameters. The effect of base current on the equivalent circuit will be discussed later.

The simple equivalent circuits of the switched diodes and transistor are essentially alike in figures 19 and 20, but the values of the electrical elements in the circuits will generally be different. Briefly stated, R_{cl} and V_{cl} of the transistor will be lower than that of the diode while R_{op} and I_{op} of the transistor may be higher than that of the diode; however, the diode will usually be able to withstand a higher reverse voltage than the transistor. The equivalent circuit of the transistor and diode are useful even without circuit element values because the equivalent circuit can be used to establish that certain types of decoder circuits are not as well suited to semiconductor switching as are other decoder circuits. The semiconductor switches to be studied require at least one transistor or diode per switch pole, per throw.

The discussion that follows assumes that V_{cl}, R_{cl}, I_{op}, and R_{op} are constants, thus the discussion is concerned mostly with decoder aspects that are related to the decoder's initial gain error and linearity. The stability of V_{cl}, R_{cl}, I_{op}, and R_{op} will be treated

after the previously studied decoder circuits have been considered for adaptability to semiconductor switching.

Some of the decoder circuits are such that their switches are in series with their decoding resistor. If this decoding resistor is appreciably greater than R_{cl} of the closed switch, then the effect of R_{cl} can be eliminated if the decoding resistance is reduced by an amount that is equal to the ohmic value of R_{cl}. This can be accomplished if the decoding resistor is permanently reduced by the maximum expected value of R_{cl} and then seriesed with a trimmer rheostat that can be varied to provide any resistance up to the maximum expected resistance of R_{cl}. The total decoding resistance is thus the series resistance of the fixed decoding resistor, the switch R_{cl}, and the trimmer resistance that has been adjusted to provide an overall series resistance that is correct for the decoding function. The circuits of the potentiometric and feedback amplifier do not lend themselves to this type of compensation for their switches' R_{cl} since the switches of these circuits are in shunt with their decoding resistors. It is likely that double throw switching will require two trimmer rheostats for correction of errors due to R_{cl}.

The effect of the closed switches V_{cl} can be corrected for with a voltage in series with the switch if this voltage is equal in magnitude and opposite in polarity to V_{cl}. In some circuits, V_{cl} can be corrected for by adjusting the rheostat used for correcting the decoding resistance if the ohmic value of the rheostat is properly

selected in conjunction with the current through the rheostat. It is apparent in the weighted resistor circuits of figures 14b and 15 that such a correction can be made because these circuits output a fixed "1" current for each bit and they output no "0" current. In other circuits, an external current can be forced through R_{cl} of the switch to cause a total switch drop of zero volts. This is particularly true if V_{cl} must be corrected for with zero decoding current through the switch; however, if the switch is closed with zero current through it, compensation of R_{cl} is not required. Further if the zero current switch is connected to a voltage bus, then the current that corrects for V_{cl} can come from another bus that is referenced to the first mentioned bus and the second bus can provide correction current for a number of switches. The weighted decoder of figure 14a can fit the categories of bus connected switches, with a fixed "1" current through one closed switch with zero "0" current while the other switch has zero "1" and "0" current. If the decoding switches are not connected to a bus, then compensation of V_{cl} in a manner similar to that of the other decoders will probably require that an external current from an isolated power supply be forced through the switch. The potentiometric and feedback amplifier decoders require an isolated external current since the switches are in series and both sides of the switch are connected to a varying potential (except two switches of the potentiometric decoder where one side of the switch is at a fixed potential). The design of switches for these two

decoders will probably require an isolated supply for each switch in order to obtain the desired switching and perhaps each supply can be used to provide the current for V_{cl} correction for its switch.

Recent advance in silicon semiconductor technology has made possible the production of transistors and diodes that have low cut-off leakage currents, but at high temperature these currents can have appreciable effect in some decoding circuits. In some circuits such as those of figures 14b and 15, the open switch "0" leakage current flows directly out of the decoder as if it were a "1" current. The circuit of figure 15 has an advantage over that of 14b because the cut-off switch voltage can be kept low but even so, the leakage from the I_{op} generator and through R_{op} will affect the decoder's output. Much of this effect can be eliminated by refrigerating the switch component but refrigerating is a troublesome design requirement.

The effect of switch leakage current can be made small with double throw, single pole switching without the aid of refrigeration. The double pole switch of figure 21 transfers resistor $R/2^{n-1}$ between voltage busses V1 and V2 and in particular $R/2^{n-1}$ is connected to V2 in figure 21. The leakage current I_{op} of the open switch will affect the decoding only if part of I_{op} passes through resistor $R/2^{n-1}$. If the resistance between V1 and V2 is negligible, the current I_{op} will be divided between R_{cl} and $R/2^{n-1}$. If R_{cl} is much less than $R/2^{n-1}$, then most of I_{op} is shunted thru R_{cl} and I_{op} has little effect on the circuit's decoding. Likewise most of the

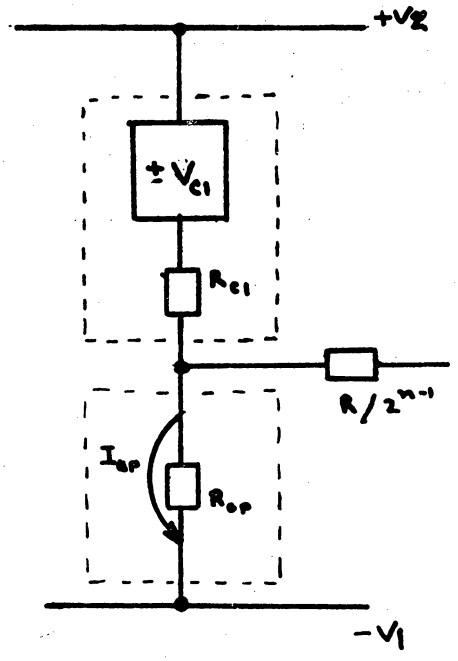


Figure 21. Single Pole, Double Throw Switch

current through R_{op} goes through R_{cl}. I_{op} and R_{op} will have less and less effect on the circuit's decoding as R_{cl} approaches zero ohms. The ladder of figure 16 and the weighted resistor decoder of figure 13 use double throw switching between voltage buses, thus the effect of their switches I_{op} and R_{op} can be reduced by the shunting effect as described.

The effect of switch leakage current in current decoders such as those of figures 14a, 14b, and 15 lends itself to some general evaluation. With a minimum input converter resistance of 10,000 ohms at 20 volts input, the maximum current per quantum (.025% of full scale current) will be one-half of a microampere. The combined leakage current through the decoder's switch resistors should be small compared to E1/R and E1/R will be no greater than one-half of a microamp. It is difficult to be general about the effect of leakage current in voltage decoders because the effect will vary with the value of the resistors used and these are not predictable from the specifications.

Table 2 coordinates the previously discussed decoders with the R_{cl}, V_{cl}, I_{op}, and R_{op} corrections that can be made in the manners described. An X indicates that the corrections are applicable. V_{cl}-1 correction is made by adjusting the rheostat that corrects for switch resistance; V_{cl}-2 correction requires an external source and V_{cl}-3 is made with an isolated external source for each switch.

Table 2. Decoder Switch Corrections

Decoder		Correction					
Type	Figure	R_{cl}	V_{cl}-1	V_{cl}-2	V_{cl}-3	I_{op}	R_{op}
Weighted	13	X	X	X		X	X
Weighted	13 (V_o = const.)	X	X	X		X	X
Weighted	14	X	X				
Weighted	15	X	X				
Ladder	16	X		X		X	X
Amplifier	17				X		
Potentiometric	18				X		

It will be shown later that the second listed decoder requires one V_{cl}-1 and one V_{cl}-2 correction for the pair of devices of its double throw switch.

More detailed knowledge of the characteristics of diodes and transistors is required before giving further consideration to decoder switching circuitry.

The junction characteristics of semiconductor diodes and transistors have been published.[18] The equation that describes a PN (diode) junction is: $I = I_s (e^{qv/kT} - 1)$ V-5

where kT/q = .026 volts at 25°C
T = Kelvin temperature
$I_s = -I_o$ of figure 19

and if v is somewhat greater than .026 volts:

$$I = I_s e^{qv/kT} \qquad V\text{-}6a$$

while a large negative v causes:

$$I = -I_s$$

equation V-5 can be solved for v to yield:

$$V = \frac{kT}{q} \ln (I/I_s) \qquad V\text{-}7$$

from which it can be seen that a decrease in reverse leakage current causes an increase in the forward voltage drop and vice versa.

An approximate dynamic resistance for the diode can be determined by differentiating equation V-7 with respect to current, I.

$$\frac{dV}{dI} = KT/qI = R_{dd} \qquad V\text{-}8$$

The transistor has two PN junctions. When both of these junctions are forward biased, the transistor is operating in a saturated mode and the sum of the junction voltage is $(V_{ce})_j$ and:

$$(V_{ce})_{Nj} = \pm \frac{PKT}{q} \ln \left\{ \frac{\alpha_I \left[I_b - I_c \left(\frac{1-\alpha_N}{\alpha_N} \right) \right]}{\left[I_b - I_c (1-\alpha_I) \right]} \right\} \qquad V\text{-}9^*$$

1. $(V_{ce})_{Nj}$ = the voltage from the collector to emitter of a <u>normally</u> operated transistor as depicted in the <u>common emitter</u> connection of figure 22a. $(V_{ce})_{Nj}$ of this equation is solely the voltage due to diode <u>junction</u> voltages and as such it excludes real ohmic voltage drops.

2. I_b and I_c are positive when in the direction of the solid arrow in figure 22a, negative when reversed from the arrows.

3. α_N = normal d.c., short circuited output, common base current gain.

4. α_I = inverse d.c., short circuited output, common base current gain.

5. Equation V-9 is subject to the following approximations:
   a. space change widening effects are negligible.
   b. the base emitter and base collector diodes each separately obey equation V-5.
   c. emitter efficiency is not dependent upon emitter current.

6. The $\pm$ sign of equation V-9 is applicable for PNP transistors while the $-$ sign is applicable for an NPN transistor.

* Equation V-9 is a redefined version of work presented in reference 19.

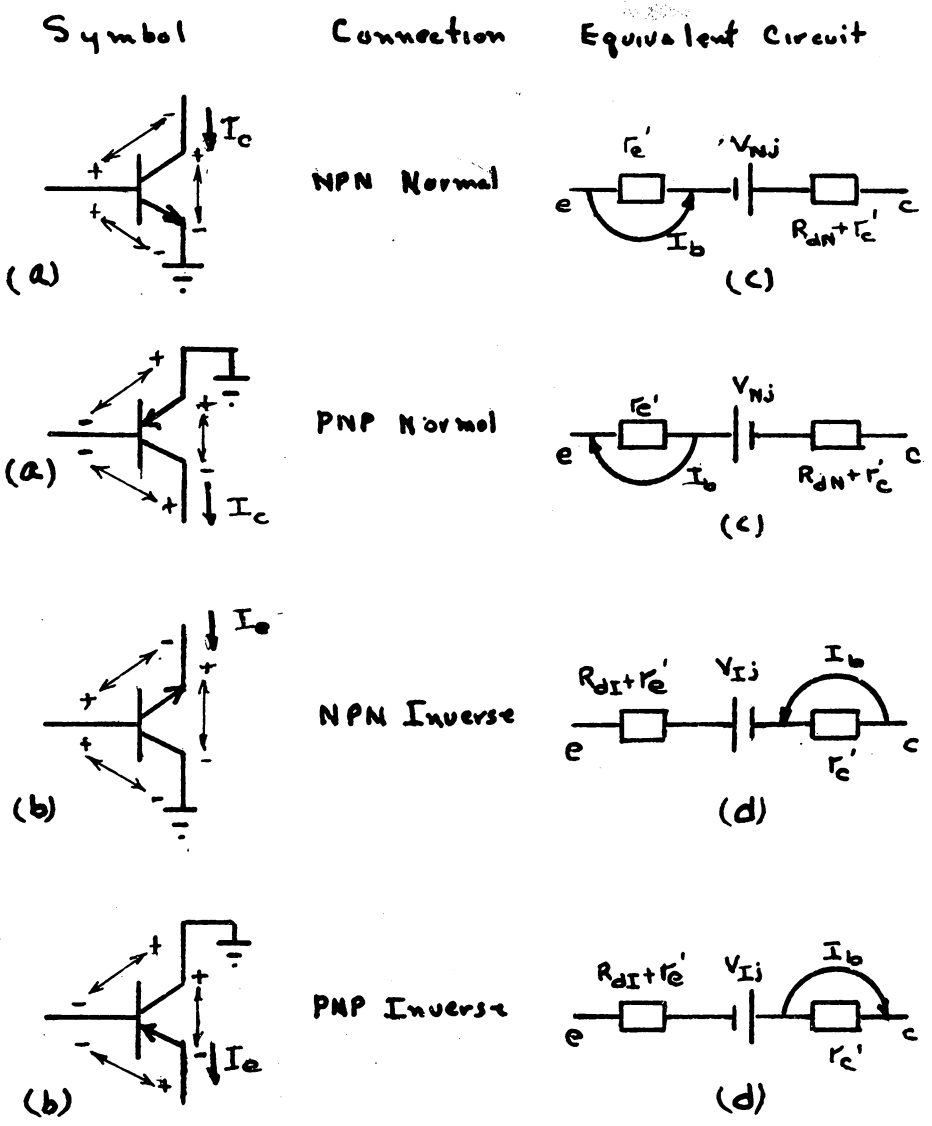


Figure 22. Positive Notations for Saturated Transistors

7. P is approximately 1 for germanium transistors and P is between 1 and 2 for silicon transistors.[20]**

If the transistor is operated in an inverted manner as shown in figure 22b, equation V-9 can be modified to give the transistor's collector emitter voltage by exchanging emitter and collector notations and normal and inverse notations, thus:

$$(V_{ce})_{Ij} = \pm \frac{PKT}{q} \ln \left\{ \frac{[I_b + I_e(1-\alpha_N)]}{\alpha_N [I_b - I_e(\frac{1-\alpha_I}{\alpha_I})]} \right\} \qquad V-10$$

and the + sign is applicable for a PNP transistor while the - sign is applicable for an NPN transistor.

The inverted connection is a common collector connection and it is of particular interest when I_b is opposite to I_e of figures 22b because V_{ce} can become zero with such an I_b bias.

The dynamic impedance of the saturated transistor can be determined by differentiating its collector-emitter voltage with respect to the collector or emitter current that establishes the voltage. For the normal connected transistor:

$$\frac{d(V_{ce})_{Nj}}{dI_c} = +\frac{PKT}{q}\left[\frac{-M}{(I_b - MI_c)} - \frac{Q}{(I_b + QI_c)} \right]$$

where $M = \frac{1-\alpha_N}{\alpha_N}$ $\qquad Q = (1-\alpha_I)$

$$\frac{d(V_{ce})_{Nj}}{dI_c} = \pm\left(-\frac{PKT}{q}\right)\left\{ \frac{1-\alpha_N}{\alpha_N[I_b - I_c(\frac{1-\alpha_N}{\alpha_N})} + \right.$$

$$\left. \frac{1-\alpha_I}{I_b + I_c(1-\alpha_I)} \right\} = -\frac{d(V_{ec})_{Nj}}{dI_c} \qquad V-11$$

** It seems likely that a constant with the effect of P should appear in equations V-5 through V-8.

Similarly: $$\frac{d\,(V_{ce})_{Ic}}{d\,I_e} = -\frac{d(V_{ec})_{Ij}}{d\,I_e} = \pm\frac{PKT}{q}\left\{\frac{1-\alpha_I}{\alpha_I\left[I_b - \frac{(1-\alpha_I)I_e}{\alpha_I}\right.}\right.$$

$$\left. + \frac{1-\alpha_N}{I_b + (1-\alpha_N)I_e}\right\} \qquad V\text{-}12$$

where the (/) sign preceding equation V-12 is applicable for a PNP transistor while the (-) sign is applicable for an NPN transistor.

For most transistors:

$$\frac{(1-\alpha_N)}{\alpha_N} I_c \ll I_b$$

if I_c is comparable to or less than I_b. For switching transistors it should be reasonably valid to assume that:

$$\frac{(1-\alpha_I)}{\alpha_I} I_e \ll I_b$$

when I_e is comparable to or less than I_b. If so, then:

$$(V_{ce})_{Nj} \simeq \pm\frac{PKT}{q} \ln \alpha_I \qquad V\text{-}13$$

$$(V_{ce})_{Ij} \simeq \pm\frac{PKT}{q} \ln \alpha_N \qquad V\text{-}14$$

$$\frac{d\,(V_{ce})_{Nj}}{d\,I_c} = R_{dN} \simeq \pm\left(\frac{-PKT}{q}\right)\left[\frac{1-\alpha_I\alpha_N}{\alpha_N}\right] \qquad V\text{-}15$$

$$\frac{d\,(V_{ce})_{Ij}}{d\,I_e} = R_{dI} \simeq \pm\left(\frac{PKT}{q}\right)\left[\frac{1-\alpha_I\alpha_N}{\alpha_I}\right] \qquad V\text{-}16$$

where the (/) signs preceding the equations are applicable to PNP transistors and the (-) signs are applicable to NPN transistors.

Table 3 lists several values of $\ln \alpha$ and $\frac{\alpha}{1-\alpha}$ as a function of α. The ratio $\frac{\alpha}{1-\alpha}$ is the low frequency current gain of a transistor operated in the common emitter or collector configuration. High values of α are those that might be typical of α_N while low values might be typical of α_I.

Table 3. Transistor α Versus $\ln(\alpha)$ and $\frac{\alpha}{1-\alpha}$

α	.98	.95	.9	.85	.8	.5
$\alpha/(1-\alpha)$	49	19	9	5.7	4	1
$\ln \alpha$	.02	.054	.1	.16	.22	.7

The data of Table 3 can be used to compare the normal common emitter transistor connection to the inverse connection. Suppose that a transistor has an α_N of .98 and an α_I of .8. The normal connection has a dynamic resistance that is about 23% less and a $(V_{ce})_j$ that is about 1100% greater than that of the inverse connection.

In addition to its dynamic resistance, the saturated transistor has resistance caused by the resistivities of the transistor's collector and emitter elements. The transistor's base current passes through one or the other of the two elements.

Figure 22 c and d provide an equivalent circuit for the saturated transistor operation that has been presented. The resistors, r_c' and r_e' are the resistances of the transistor's collector and emitter elements. The circuit is limited by the assumptions presented for equations V-9 through V-16 but various work has shown that the circuit is reasonably valid with selected operating currents for the PNP and NPN germanium alloy [21, 22], PNP silicon alloy [23],

some silicon planar and planar epitaxial [24] transistors.

The equations that determine the cut-off or open transistor performance are the same for normal and inverted transistor connections but the output current of interest is different. The usual output current of a normally connected transistor is its collector current while the output current of an inverted transistor is its emitter current. Assuming that both transistor junctions are reverse biased by more than a few tenths of a volt and neglecting leakage resistance across the transistor [25]:

$$I_e = \frac{I_{eo}(1-\alpha_N)}{1-\alpha_N\alpha_I} \qquad V-17$$

$$I_c = \frac{I_{co}(1-\alpha_I)}{(1-\alpha_N\alpha_I)} \qquad V-18$$

where I_{eo} = leakage current of the emitter-base diode
I_{co} = leakage current of the collector-base diode

Usually α_N and α_I will be very low when the transistor is cut off [25, 26] thus:

$$I_e \simeq I_{eo} \qquad V-19$$

$$I_c \simeq I_{co} \qquad V-20$$

In general, I_{eo} of low level switching transistor is less than I_{co}.

The value of R_{op} is not predictable by equation, but it has been determined [27] for a silicon PNP alloy 2N2185, a transistor of the type that might be used for an inversely operated switch. At 25°C, the transistor's leakage resistance is 2×10^{11} ohms. For comparison, R_{op} of the same transistor is 10 times greater when the transistor is operated with normal bias.

Table 4 presents data that is useful in comparing the switching characteristics of a diode and transistor that could be used in a decoder's switch. The data is typical (except as noted), 25°C data published by the device manufacturer. V_{cl}, R_{cl}, I_{op} and R_{op} are defined in Figures 19 and 20. The diode data has been approximated by straight lines imposed upon a typical diode characteristic in its zero to two milliampere region. The transistor data is for inverted operation and it can be referenced to Figure 22 as follows:

$$V_{c1} = (V_{ce})_{Ij} + I_b r_e'$$

$$R_{c1} = R_{dI} + r_e' + r_c'$$

V_{op} is the voltage across an open switch.

Table 4. Diode and Inverted Transistor Switching Characteristics

Device	Manufacturer	$\pm V_{c1}$ (Mv)	R_{c1} (Ohms)	$I_{op} \neq V/R_{op}$ (10^{-9} Amps)	V_{op} (Volts)	Comments
1N457A	Hughes	590	60	.8	50	Low Leakage Diode
2N2185	Philco	1.2	14	1.0 (Max.)	10	I_b = 1 MA, PNP alloy

It is easily concluded that functionally, the transistor is a better "closed" switch than the diode at 25°C.

Equations V-7 and V-14 show that the absolute voltage variation as a function of temperature is much less for the transistor than for the diode when the current through the devices is much larger than 10^{-9} amperes and the current of a decoder switch will generally be

larger than 10^{-9} amperes.

For a given current, I, the diodes dynamic resistance varies as its ambient's Kelven temperature varies (see V-8). The dynamic resistance of a transistor may vary more or less percentage-wise than the diode since:

$$R_{dr} \simeq \frac{\rho K T}{q I_b}\left[\frac{1-\alpha_r \alpha_n}{\alpha_r}\right]$$

$$\simeq \frac{\rho K T}{q I_b}\left[1/\beta_r\right] \quad \text{where } \beta_r = \alpha_r/(1-\alpha_r) \quad \text{V-21}$$

where β_r is the inverse current gain of the transistor. β_r is temperature sensitive. At any rate, if the current I through the diode is near the same value as I_b, the absolute resistance variation of the transistor's dynamic resistance will be less than that of the diode. The data of Table 4 reveals that much of R_{cl} may be bulk rather than dynamic resistance and this part of the resistance will have the temperature coefficient of resistance of silicon material.

The current $I_{op} \neq V/R_{op}$ of the diode and transistor probably changes with temperature in similar manners since the current in the transistor is a diode current.

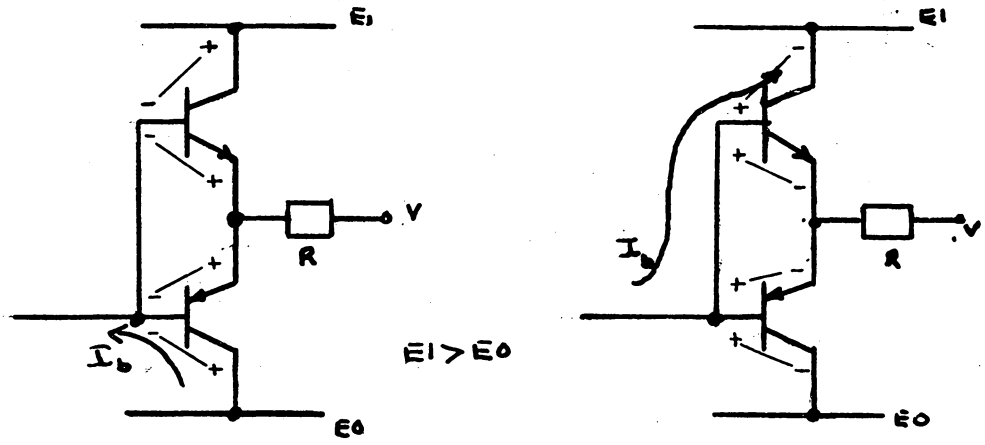
Unfortunately, the effect of aging on V_{cl}, R_{cl}, I_{op}, and R_{op} is not generally well documented by manufacturers of diodes and transistors.

As explained previously, the effect that the switch has on accuracy can in some circuits, be corrected for with a series trimmer but the trimming must be kept small if the resolution of the trimmer is to provide acceptable adjustment. The resolution of the trimmer

for V_{c1} and R_{c1} compensation should probably give a decoder output resolution of a few thousandths of a per cent, and accomplishing this with commonly used rheostats could limit series rheostat resistance to a few tenths of a per cent of the decoding resistance. To correct for $\pm$ one hundred millivolts of initial switch drop variation, as might well be required for the diode, would push the reference voltage to a hundred volts and this is not a very practical voltage for semiconductor reference voltage supplies.

It would seem that the transistor switch is more practical than the diode switch for the performance required. A double throw switch that uses a pair of transistors with inverse transistor connection has been used in decoding functions.[28] This switch is illustrated in Figure 23.

When the PNP transistor is saturated, as in Figure 23a, one side of R is connected to bus EO and the NPN transistor is cut off. The NPN transistor is saturated while the PNP transistor is cut off in Figure 23b. The switch efficiently utilizes the transistor's ability to withstand cutoff voltage. Most transistors can withstand higher reverse bias on their base-collector junction than on their emitter-base junction and the circuit of Figure 23 limits the emitter-base reverse bias to the voltage of a forward biased diode (emitter-base of the saturated transistor) while the collector-base junction withstands ($E1 - Eo \pm V_{cb}$) volts, where V_{cb} is the forward base-collector voltage of the saturated transistor.



(a) R switched to E0 (b) R switched to E1

Figure 23. Single Pole, Double Throw Transistor Switch

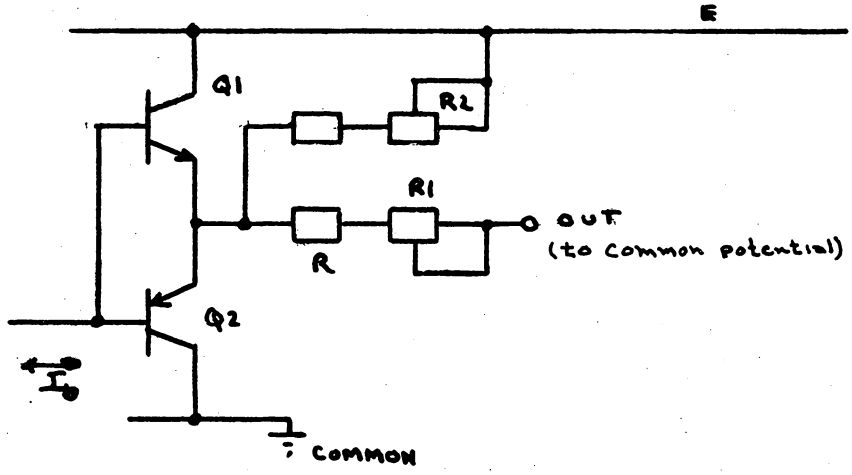


Figure 24. Compensation for Switch when Outputting to a Junction at Common Potential

A study of the decoder analysis thus far presented would seem to indicate that the decoder of Figure 13, with a switch similar to that of Figure 23, used in the converting manner of Figure 14a, offers better performance or possibilities of better performance than any of the other decoders. Figure 13's resistor network is as simple as any. Considering its performance, the switch of Figure 23 is quite simple and the nature of the decoder and current summing into a point of common potential permits the use of minimum compensating components. Figure 24 provides a circuit that has a "1" output current (Q1 inversely saturated) that can be adjusted to a desired value by setting the resistance of R1 such that $(E \neq V_{c11})/(R \neq R_{c11} \neq R1)$ gives a desired output current into an output point that is at common potential. R2 provides current from reference voltage E to cause a drop across R_{c12} that cancels V_{c12} when Q2 is inversely saturated ("0" output). A conversion error can be caused by R_{c12} if current flows in R when Q2 is saturated because $(R_{c12} \neq R \neq R1)$ is not equal to $(R_{c11} \neq R \neq R1)$, but the error diminishes as the comparison circuit's input potential approaches common potential. As previously explained, the double throw switch greatly reduces the conversion errors due to transistor I_{op} and R_{op}. The apparent disadvantages of this decoder are that it loads its power supply and it has variable self-heating of its resistors. If required, the latter disadvantage can be minimized by using a resistor with a low temperature coefficient and high thermal dissipation and by operating

the resistor at low power. For simplest operation, the base current of the NPN transistor of this switch loads into the reference voltage supply. This loading is the cost of simplicity and if the supply's regulation warranted, the loading could be eliminated by driving each switch of the decoder with an isolated power supply. Actually the loading that the switch causes on the power supply can be used to good advantage in reducing the overall loading on the supply. The base current of the NPN flows into the supply while the decoder's output current flows out of the supply, thus the two currents tend to cancel each other. Section VI provides a decoding circuit that utilizes the concept of current cancelling to reduce the loading on the reference voltage supply.

Assuming then that self-heating and supply loading are not serious problems with the current output, weighted resistor decoder, then it would seem that this decoder should be used in the converter if it is compatible with the converter's comparing, complementing and half-count offset biasing functions with dual, bipolar input voltages ($\pm$ 10 volts and $\pm$ 20 volts).

Complementing and Comparing

An equivalent circuit of the weighted resistor decoder of Figure 13, is given in Figure 25. R_d of this circuit is the equivalent parallel resistance of all resistors of the decoder, (2^n-1) is the full scale count of the decoder; P is the weight of the number being decoded $(0 \leq P \leq 2^n-1)$, and (E) is the decoder's reference voltage.

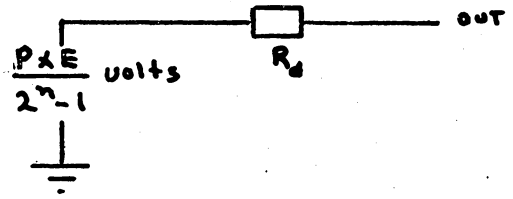


Figure 25. Equivalent Circuit of Weighted Resistor Decoder

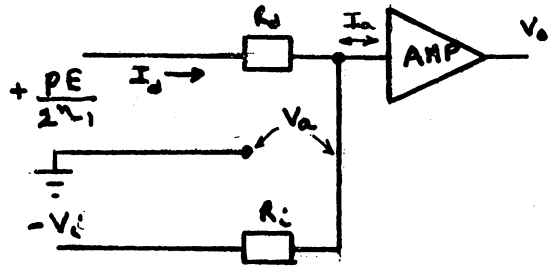


Figure 26. Comparing Operation

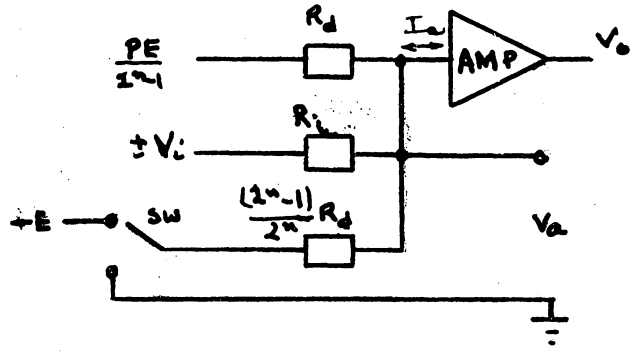


Figure 27. A Comparing and Two's Complementing Circuit

If the converter's input voltage has a polarity opposite to that of (E), then the converter's comparing functions can be achieved in the manner illustrated in Figure 26. The converter's input voltage is shown as $-V_i$ in Figure 26. The converter's comparison function is accomplished with the aid of a high sensitivity, voltage amplifier. Neglecting any voltage drops through R_d and R_i caused by I_a, the amplifier's output voltage has two distinguishable states, one of which is associated with each polarity of V_a with respect to common. If I_a is other than zero for D-C biasing, then the amplifier detects the polarity of a voltage such as V_a about some D-C level other than common. A constant source impedance makes this offset operation consistent without regard to the value of P. It will be shown later that the effect of I_a $[I_a = f(V_i)]$ is to reduce V_a and cause a small conversion error because the converter's switch $R_{cl2} \neq R_{cl1}$. The circuit of Figure 26 should be designed such that:

$$\frac{E}{R_d} = \frac{|-V_i'|}{R_i}$$

where $-V_i'$ is the full scale input voltage of the converter. If the amplifier's output voltage and the converter's logic cause a P such that the conversion is correct when V_a is approximately zero volts then:

$$\frac{PE}{2^{n-1}} \times \frac{1}{R_d} \simeq \frac{|-V_i|}{R_i} \qquad V\text{-}22$$

$$\frac{P}{2^{n-1}} \times \frac{|-V_i'|}{R_i} \simeq \frac{|-V_i|}{R_i}$$

or

$$\frac{P}{2^{n-1}} \simeq \frac{V_i}{V_i'} \qquad V\text{-}23$$

which is the desired proportionality for a normal conversion.

The specifications require that the converter's digital output be the 2's complement of its input voltage when the input voltage is positive. By definition, the 2's complement of P is (2^n-P). Figure 27 provides a circuit that gives a normal conversion when V_i is negative by closing SW to common and a complemented conversion when V_i is positive by closing SW to (-E) (Where $|E| = |-E|$). The amplifier's initial output can be used to determine the necessary position of SW. The circuit of Figure 27 should be designed such that:

$$\frac{E}{R_d} = \frac{|-V_i'|}{R_i}$$

In normal operation with V_a at approximately zero volts:

$$\frac{1}{2}\left(\frac{PE}{2^n-1}\right) \simeq \frac{|-V_i|}{R_i} \qquad V-24$$

and

$$\frac{P}{2^n-1} \simeq \frac{V_i}{V_i'} \quad \text{as before}$$

In complement operation with V_a at approximately zero volts:

$$\left|\frac{E}{R_d} \times \frac{P}{2^n-1} - \frac{E}{\frac{R_d(2^n-1)}{2^n}}\right| \simeq \frac{V_i}{R_i} \qquad V-26$$

$$\left|\frac{E}{R_d}\left(\frac{P-2^n}{2^n-1}\right)\right| \simeq \frac{V_i}{R_i}, \text{ and}$$

$$\frac{2^n-P}{2^n-1} \simeq \frac{V_i}{V_i'} \qquad V-27$$

thus the circuit complements as expected. It is worth noting that the cost of complementing as compared to the non-complementing circuit has been to add a switch and another reference voltage. In addition the value of V_a that results from a given difference between

V_i/R_i and PE/R_d is reduced since R_i of Figure 27 looks into a lower circuit resistance. In return, the complementing circuit has been doubled the full scale conversion ability of the converter while providing the converter with a full range voltage input that is centered about common.

Figure 28 offers a simpler complementing scheme because its complementing switch is like that of the decoder. This complementing circuit attenuates V_a more than that of Figure 27.

The effect of I_a is much the same as that of adding another summing resistor to the network. If I_a causes a voltage drop V_x with respect to common ($V_x = I_a\,(1/(1/R_i + 1/R_d + - -))$ and if the amplifier is adjusted so that its output changes state as V_a changes polarity about V_x rather than common, the complementing and comparing operation is still accurate. Using Figure 28 as an example with negative V_i and an I_a thatis into the amplifier and an amplifier adjustment such that P is stopped when V_a equals V_x:

$$\frac{\frac{PE}{2^n-1} + V_x}{R_d} + \frac{E+V_x}{\frac{(2^n-1)R_d}{2^n}} - \frac{(E-V_x)}{\frac{(2^n-1)R_d}{2^n}} - \frac{V_i-V_x}{R_i} - I_a = 0$$

$$\left\{ \frac{PE}{(2^n-1)R_d} + \frac{E}{\frac{(2^n-1)R_d}{2^n}} - \frac{E}{\frac{(2^n-1)R_d}{2^n}} - \frac{V_i}{R_i} + \frac{V_x}{R_d} + \right.$$

$$\left. \frac{V_x}{\frac{(2^n-1)R_d}{2^n}} + \frac{V_x}{\frac{(2^n-1)R_d}{2^n}} + \frac{V_x}{R_i} - I_a \right\} = 0$$

$$\frac{PE}{(2^n-1)R_d} = \frac{V_i}{R_i} \quad \text{and} \quad \frac{P}{(2^n-1)} = \frac{V_i}{V_i'} \qquad \text{V - 28}$$

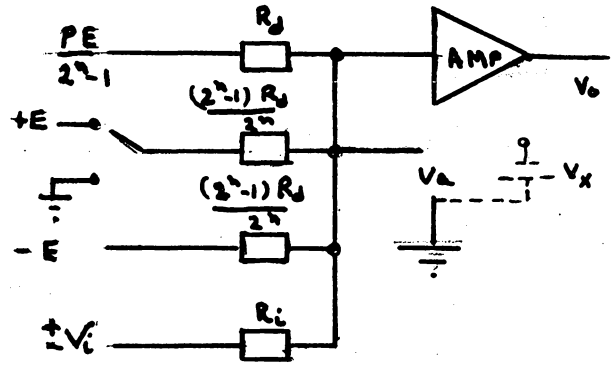


Figure 28. Modified Comparing and Two's Complementing Circuit

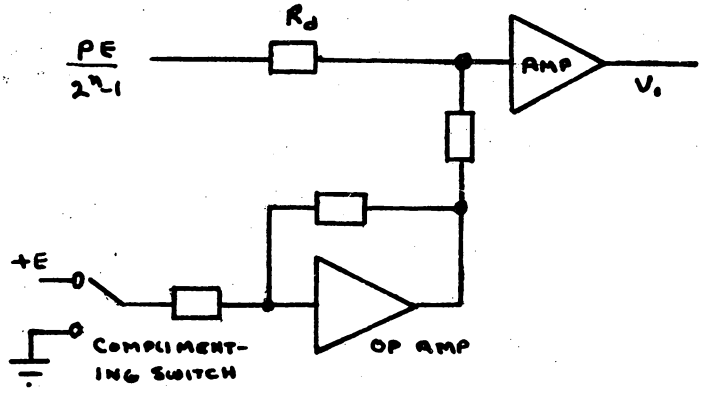


Figure 29. Comparing and Complementing Without a Second Reference Supply

which is the proper operation for a negative Vi. Similarly, it can be shown that the circuit operates properly with positive V_i.

By postulate, the amplifier's input resistance is high, thus I_a is low. The input signal attenuation effect of I_a can be considered as being due to a reduction of the resistance that loads the converter's input resistance. If I_a is independent of V_x, then I_a does not reduce the signal to the amplifier; however, the small signal input current of the amplifier will probably do so.

The converter's half count offset can be obtained by connecting a resistor from (-E) to the input of the amplifier. This offset technique biases the decoder in the same manner as the complementing technique.

In conclusion, the circuit of Figures 27 or 28 with an added half count bias will provide the comparing and complementing functions of the voltage-to-digital converter that is to be designed. For this converter:*

$$0 \leq P \leq 4095$$

thus

$n = 12$ = number of decoding bits without complementing bit

$2^n - 1$ = full scale = 4095

$2^{n+1} - 1$ = full range = 8191

and if R is the value in ohms of the converter's "1" bit

*(Full scale of 4095 has been redefined somewhat from that specified in Section I. The full scale input voltages of the converter just defined will be $\pm 20 \times 4095/4000$ or $\pm 10 \times 4095/4000$ volts).

$R/(2^n-1) = R/2048$ = resistance of highest order bit (excluding complementing bit)

$R_d(2^n-1)/2^n) = R/2^n$ = resistance of complementing resistor

$2R$ = resistance of half-count offset resistor

The greatest disadvantage of the converter circuitry just proposed is that the (-E) voltage supply is required. This supply can be eliminated from the converter with a circuit such as that of Figure 29, but the added amplifier will increase the converter's initial comparison settling time and its circuit is probably as complicated, or more so, than that of the (-E) voltage supply.

Figure 30 outlines a less complicated method of eliminating the (-E) voltage supply. The transistors shown in Figure 30 are the first stage transistors of an amplifier that compares the converter's input with the decoding and complementing signals. The voltage difference between the two transistor collectors is essentially proportional to the voltage difference at the base of the two transistors if the collector voltages have been made equal when the base voltages are equal. For normal conversions, the complementing switch pole is connected to common and V_i is positive. With balance collector voltage, (V_{out} is zero):

$$\frac{KPE}{2^n-1} = \frac{R_2}{R_1+R_2} V_i \qquad V-29$$

and at full scale

$$\frac{P}{2^n-1} = 1 \qquad V-30a$$

$$V_i = V_i' \qquad V-30b$$

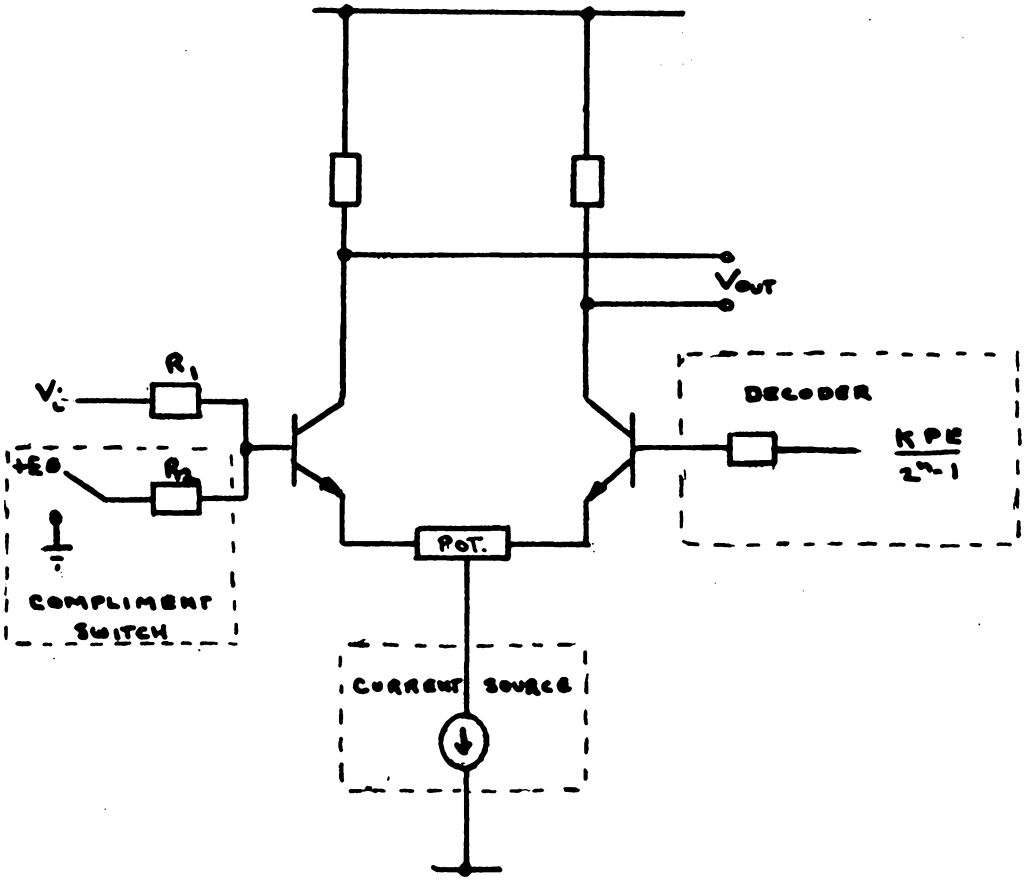


Figure 30. Voltage Comparing and Complementing with Differentially Connected Transistors

and if the circuit is designed such that

$$KE = \frac{R_2}{R_1 + R_2} V_i' \qquad V - 31$$

then $\frac{PE}{2^n - 1} = \frac{V_i}{V_i'}$ which is the desired relationship for normal conversions. For complemented operation, the complementing switch pole is connected to ($\not E$) and V_{out} will be zero when:

$$E - (E + V_i)\frac{R_2}{R_1 + R_2} = \frac{KPE}{(2^n - 1)} \qquad V - 33$$

$$\frac{ER_1}{R_1 + R_2} - \frac{V_i R_2}{R_1 + R_2} = \frac{KPE}{(2^n - 1)}$$

$$\frac{R_1}{K(R_1 + R_2)} - \frac{V_i}{V_i'} = \frac{P}{2^n - 1} \qquad V - 34$$

Now if the circuit is designed such that:

$$\frac{R_1}{K(R_1 + R_2)} - \frac{P}{(2^n - 1)} = \frac{2^n - P}{2^n - 1}$$

or $$\frac{R_1}{K(R_1 + R_2)} = \frac{2^n}{2^n - 1}$$

then $\frac{2^n P}{2^n - 1} = \frac{V_i}{V_i'}$, $V - 36$ which is the desired relationship for complemented conversions. A converter with comparing and complementing as in the circuit of Figure 30 has several disadvantages. One is that the decoder must be accurate for a wide range of output voltage thus switch compensation is complicated. Probably a greater problem is that the transient response of the differentially connected transistors will not be good for large input voltage levels. The collector of the transistors remains at a relatively constant

D-C level regardless of input voltage level, but the emitter of the transistor changes with input voltage level, and thus the power in the transistor can vary appreciably. Unless the input voltage and the complementing signal can be made to continuously track at the transistor bases, the power in the transistors can differ appreciably and self-heating of the transistors can cause a conversion error. This tracking is not natural in a "successive approximation" converter. Typically, 1/100 of a degree centigrade change in a transistor base temperature will cause about 20 microvolts of input voltage change and 1/100 of degree temperature change will result from 10 to 20 microwatts of power change in transistors of the type that would generally be used for the differential operation. Reducing the transistor power change by reducing the input voltage range reduces the input signal by a corresponding amount, and reducing the power change by reducing the transistor current reduces the frequency response of the transistor and increases the conversion errors that the I_{co}'s of the transistors cause. The wide voltage range at the amplifier's input will most likely cause saturation of the transistors during various conversion operations and saturation will appreciably slow down the operating speed of the amplifier.

It will be shown in the next section that a diode clamp from the output of an amplifier to its input can limit the change of input voltage to a small value when the comparing and complementing

of a converter are done at one junction point as in the circuits of Figures 26, 27 and 28.

VI CIRCUIT DESIGN

Introduction

The circuits examined in this section are for a voltage-to-digital converter with a current output, weighted resistor decoder of a type shown in figure 14a, section V. The complementing and decoding switches are the single pole, double throw types shown in figures 23 and 24. The decoder's output is summed with an input resistor and complementing network as shown in figure 28, section V. The comparison amplifier of the converter is a high gain, high input resistance amplifier with an input potential near zero volts with respect to the converter's input common potential.

Decoder and Complementer

The wire wound resistor is one of the more accurate and stable electronic components. Resistors with a ±.0002% per degree centigrade, temperature coefficient are available, but 45°C of ambient change (25°C to 70°C) will cause up to ±.01% change in the current of each such resistor used for decoding, complementing and input resistors. Since the total currents of the decoding and complementing resistors are up to thrice that of the input current, a full scale conversion error of ±.04% can result if all temperature coefficients contribute their maximum detrimental effect. At a premium cost, resistors with "matched" temperature coefficients can cause the resistors to track one another within ±.0001% per degree

centigrade of temperature change. This temperature coefficient can cause too much conversion error, thus the temperature of at least part of the converter's decoding, complementing and summing resistors should be controlled. In addition, the controlled temperature can be applied to the converter's switch transistors to eliminate R_{cl} and V_{cl} changes if the controlled temperature does not cause errors associated with I_{op} and R_{op}. Errors due to R_{cl} and V_{cl} variations can be reduced if the decoder's reference voltage is high enough but high reference voltage has several disadvantages that will be discussed later.

Resistors are available with good enough accuracy to satisfy the converter's gain error and linearity without trimming in a 25°C controlled ambient. A 25°C ambient would be ideal from the standpoint of using untrimmed resistors while maintaining an atmosphere conducive to near optimum reliability.

It has been previously shown that the resistance trimming used for adjusting the converter's switched resistors can also be used for correcting for switch transistor errors. It will be shown that silicon switch transistors require this correction, thus trimming circuits will be required regardless of the temperature of the controlled ambient.

The reliability of silicon transistors and wire wound resistors is good in an environment somewhat above 70°C, and the cost and space requirements of a heated chamber are appreciably less than that of a

heated/refrigerated chamber. Accordingly the following approach has been used in designing the converter's decoding and complementing circuits:

1. Provide the most significant switches and resistors with an environment that is temperature controlled somewhat above 70°C.
2. Use resistors of relatively low accuracy.
3. Use resistors of relatively high temperature coefficients.
4. Use relatively low voltage switch transistors.
5. Correct for the errors of the more significant switches and resistors with trimmer rheostats as shown in figure 24.

This design approach will be considered in further detail.

Figure 31 presents data taken from one of 33 Sprague Electric Company, silicon precision alloy PNP 2N2163 transistors. Figure 32 presents data taken from one of 101 passivated epitaxial planar, NPN transistors that were selected for high normal gain from General Electric Company transistors similar to the 2N2713-14. Both figures present data taken at 23°C from average inversely operated transistors. The inversely saturated, equivalent circuit characteristics (see figure 22) of the transistors can be approximately determined from numerical solutions of the following equations (see figure 31 for nomenclature):

$$r_c' \simeq \frac{(V_2 - V_1)}{I_{b2} - I_{b1}} \qquad \text{VI - 1}$$

$$\pm (V_{ce})_{IJ} \simeq (V_1 - I_{b1} r_c') \simeq (V_2 - I_{b2} r_c') \qquad \text{VI - 2}$$

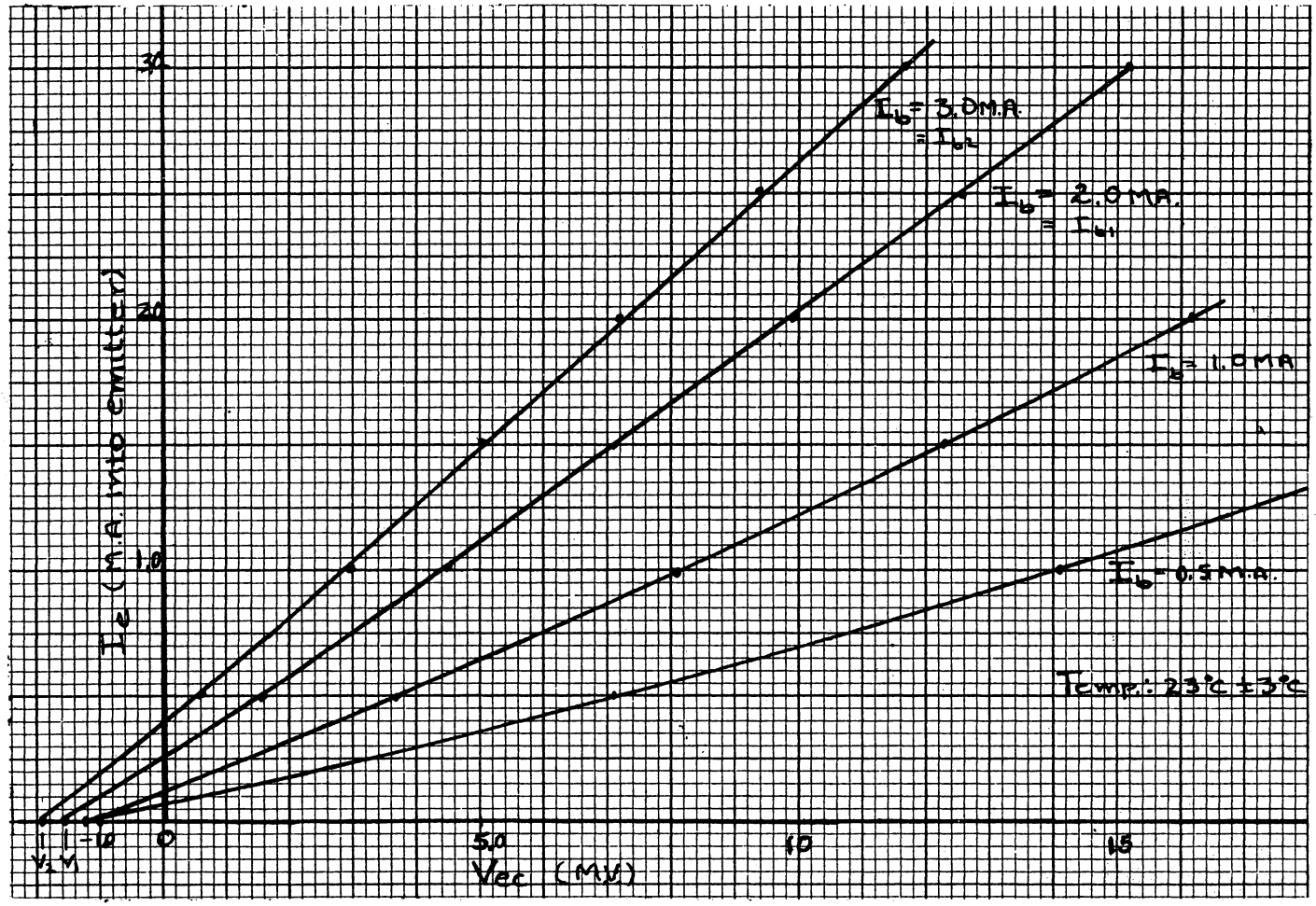


Figure 31. Saturated PNP Characteristics

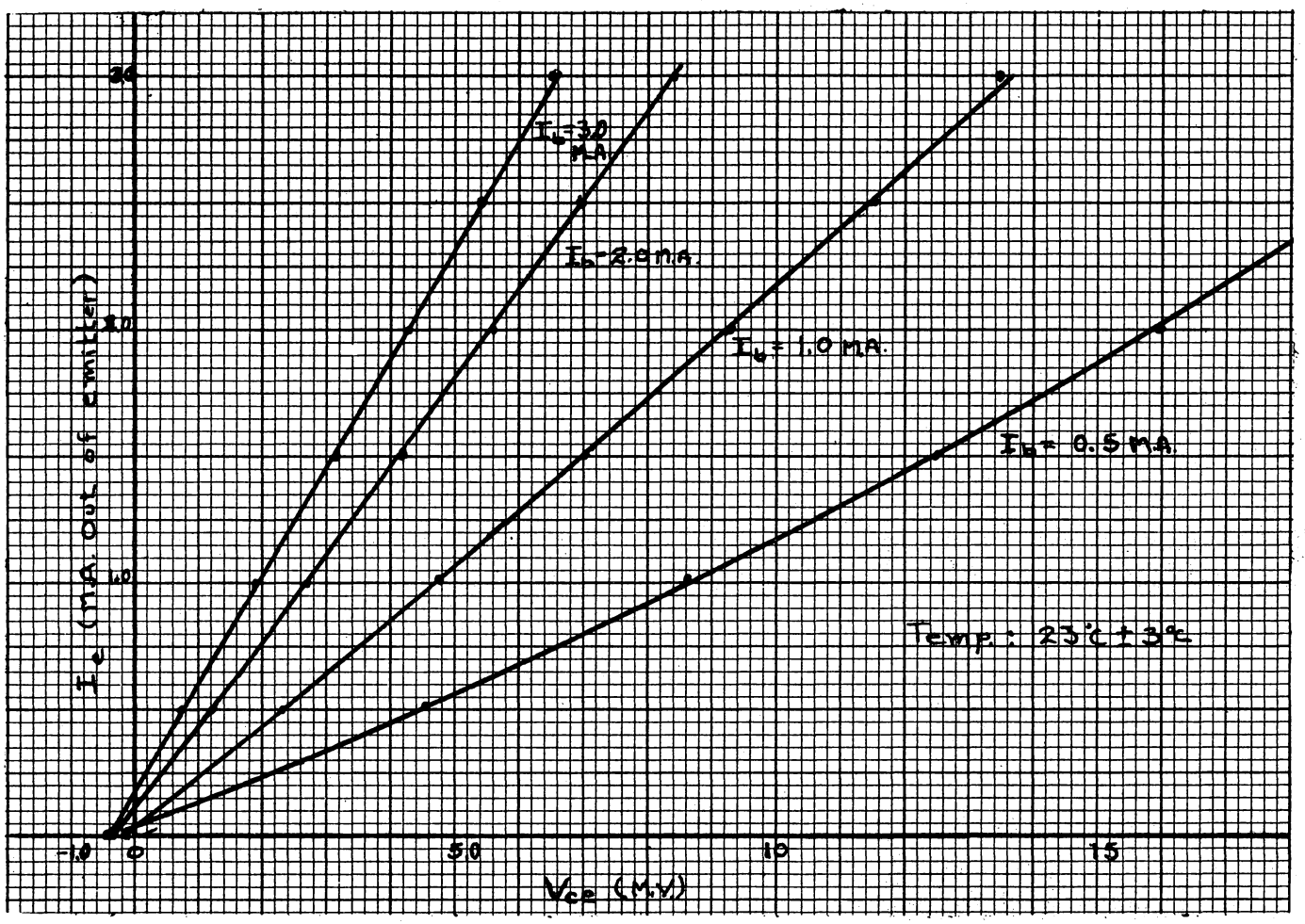


Figure 32. Saturated NPN Characteristics

$$R_{ce} = R_{c1} = R_{dI} + r_c' + r_e' \simeq \left[\frac{\Delta V_{ce}}{\Delta I_e}\right] \text{ for each } I_b \qquad \text{VI-3}$$

and $R_{dI} = f(1/I_b)$ thus let $R_{dI} = V_x / I_b$

$$\text{then } r_e' + V_x/I_b = R_{ce} - r_c' \qquad \text{VI-4}$$

Equation VI-4 is an equation with two unknowns, V_x and r_e'. Solving this equation with the data from two curves such as that of I_{b1} and I_{b2} will provide values for V_x and r_e'. The inverse saturated parameters, $(V_{ec})_{Ij}$, R_{c1} and r_c' are easily determined from a few points of measured data as needed for solving equations VI-1 through VI-3. Table 5 lists 23°C values of $(V_{ec})_{Ij}$, R_{c1} and r_c' from measurements taken on the previously mentioned 33 silicon, PNP 2N2163's and 101 silicon, NPN transistors.

Table 5. Inversely Saturated Transistor Parameters

Transistor	Parameter	No. Sam.	I_B	I_E	Min.	Max.	Ave.
NPN	R_{c1}	93	3.0MA	1MA-2MA	1.1Ω	7.5Ω	2.0Ω
NPN	R_{c1}	12	3.0MA	1MA-2MA	1.1Ω	7.5Ω	2.6Ω
NPN	R_{c1}	12	1.0MA	1MA-2MA	2.0Ω	10.8Ω	4.5Ω
NPN	r_c'	101	-	1MA-2MA	.05Ω	1.4Ω	.15Ω
NPN	$(V_{ec})_{Ij}$	101	-	1MA-2MA	.08MV	.28MV	.13MV
PNP	R_{c1}	33	3.0MA	1MA-2MA	3.2Ω	6.0Ω	4.5Ω
PNP	R_{c1}	8	3.0MA	1MA-2MA	3.2Ω	6.0Ω	4.8Ω
PNP	R_{c1}	8	1.0MA	1MA-2MA	6.1Ω	10.3Ω	8.5Ω
PNP	r_c'	33	-	1MA-2MA	.30Ω	.80Ω	.46Ω
PNP	$(V_{ec})_{Ij}$	33	-	1MA-2MA	.80MV	1.7MV	.88MV

The transistor that provided the maximum R_{c1} of 7.5 ohms for the NPN

transistors was not particularly typical. For example, its resistance varied by fifty per cent depending upon the direction of load current through the transistor, while the resistance of the other NPN samples was not dependent upon direction of current through the transistor. The NPN sample with next to the highest resistance had an R_{cl} of 3.6 ohms. The table gives data to compare R_{cl} as a function of I_b for an I_b of one and three milliamperes. With three milliamperes of base current, about 60% of the NPN transistors and 50% of the PNP transistors R_{cl} is due to r'_e, r'_c leads, etc. This relationship of R_{cl} to I_b is essentially true for each individual transistor of the small sample lot (excluding the 7.5 ohm NPN) as well as for the average of the transistors tested.

Values of $(V_{ec})_{Ij}$ and R_{cl} depend upon the current gain of the transistor. The current gain is a function of I_e and data given in Table 5 is for an I_e of one to two milliamperes but the table data should be reasonable valid for I_e's from a few tenths to ten or so milliamperes.

The effect of temperature on the parameters of the saturated transistors was determined from a limited sample of the available transistors. For the NPN transistor, an increase in temperature from $0^{\circ}C$ to $80^{\circ}C$ caused a 10% to 30% increase in its three milliampere R_{cl}'s, a 40% to 50% decrease in $(V_{ec})_{Ij}$'s and a 15% to 25% increase in r_c's. For the PNP transistor, a like change in temperature caused about 15% increase in its three milliampere R_{cl}'s, less than 10%

decrease in $(V_{ec})_{Ij}$'s and 10% to 15% increase in r_c's.

The conversion errors and deviations caused by the switch transistors will be reduced as the converter's reference voltage is increased. It should be noted that the selection of reference voltage in conjunction with the already specified converter input voltage per count establishes the voltage that is input to the comparison amplifier per count of difference between the converter's input and decoder signals. The amplifier input voltage, V_a/count, can be easily determined. Assume that the amplifier has infinite input impedance and:

R' = resistance of each complementing resistor, and thus R'is very nearly equal to the parallel equivalent resistance of the decoding resistors

E = reference voltage with respect to common

V_i' = converter input voltage

V_i'' = converter input voltage per count ((20/4000) or (10/4000) volts per count)

R_i = converter input resistance

$$\frac{V_a}{\text{COUNT}} = \frac{V_i' \cdot R'/3}{R_i + R'/3} \simeq \frac{R' V_i''}{R' + 3R_i}$$

$$R_i = R' V_i'/E \qquad \text{(see equation following equation V-22)}$$

$$\frac{V_a}{\text{COUNT}} = \frac{E V_i''}{3V_i + E} \qquad \text{VI-5}$$

The value of V_a/count is dependent only on E and V_i' and V_i' and V_a/count approaches a maximum as E approaches infinity. In general, transistors with the desired saturated switch characteristics are

chopper transistors. Chopper transistors are usually applied in low voltage circuits and thus they are not available with high voltage ratings or else they are high priced in conjunction with a high voltage rating. High reference voltage can create reference voltage supply design problems, and high reference voltage has the further disadvantage of causing increased converter non-linearity because of increased self-heating of the converter's decoding, and complementing resistors unless the resistance value of these resistors is increased as the square of the reference voltage increase. Increasing the resistance of the switched resistors reduces the conversion errors and deviations caused by switch R_{c1}, but increasing the value of a wire wound resistor increases its cost and frequently decreases its reliability because the resistance increase is obtained by winding the resistor with more turns and/or smaller diameter wire. Higher decoding, complementing, and input resistances also increases the converter deviation caused by input current drift of the comparison amplifier.

The NPN transistor of table 5 has an 18 volt V_{ceo} rating and the PNP transistor has a 15 volt V_{cex} rating. If for no reason other than economics, these voltage ratings were used as the criterion for selecting a maximum reference voltage and the transistors of table 5 were used for the converter's switch transistors. There is little point in selecting a lower reference with the intent of reducing the resistance of the converter's resistors to reduce amplifier drift

because the minimum amplifier drift has been established by the maximum converter input current of two milliamperes. Accordingly, the converter's reference voltages were made 12 volts, positive and negative, with respect to the converter's input common.

If V_{cl} of the PNP transistor is no higher than indicated by table 5, it can be as high as 1.7 millivolts plus $I_b r'_c$ volts and 1.7 millivolts alone is appreciably more V_{cl} than is desired with a 12 volt reference voltage, thus the PNP transistor of the most significant converter switches should be trimmed as shown in figure 24.

To some extent, the error of NPN transistor's V_{cl} is cancelled by its R_{cl}, and the NPN transistor will cause no error if:

$$(V_{ce})_{Ij} + I_b r'_c = I R_{cl} \qquad \text{VI-6}$$

where I is the current through the decoding or complementing resistor in series with R_{cl}. A voltage difference of two-tenths of a millivolt or so, between the two equated values of VI-6 will provide satisfactory converter operation but the difference is not likely to remain this low without trimming since $(V_{ce})_{Ij}$ varies two-tenths of a millivolt and r'_c, I, and R_{cl} also vary. Trimming is required for the NPN transistors of the converters most significant bits.

The converter's most significant switch and resistor circuits should be designed for minimum converter deviation if the errors associated with the switch and resistor are to be eliminated by trimming.

The major conversion deviations that the converter's switch

transistors and resistor circuits effect will be due to $I_b r'_c$ variation, R_{c1} variation in conjunction with the trimmer (PNP) or fixed resistor (NPN) with which it is in series, and input current drift of the comparison amplifier. Optimum performance demands compromises since large I_b contributes to large $I_b r'_c$ variation while small I_b increases R_{c1}, and most likely, variation in R_{c1}. Minimizing the effect of R_{c1} variation by increasing the resistance in series with R_{c1} is limited by amplifier drift for the NPN transistor and by $(V_{ce})_{I_j}$ at least for the PNP transistor. Other compromising might be necessary because of cost, reliability, and self-heating problems associated with the converter's resistors. Ignoring these latter problems for the present, the circuit design can be somewhat optimized on the basis of minimizing the major conversion deviations with due regard being given to circuit design problems that might result from the minimization.

The ohmic variation in R_{c1} likely depends upon the ohmic value. There are several ways in which R_{c1} might be chosen.

A first method of selecting R_{c1} for minimum deviation might be to drive R_{c1} to a minimum by switching the transistor with a high I_b, thus:

$$R_{c1} = \text{absolute minimum} \qquad \text{VI-7}$$

This approach to selecting R_{c1} may provide a less stable switch than that of the optimum if I_b is appreciably different than I because variations in r'_c can cause appreciable V_{c1} variation. Also I_b

changes can cause appreciable V_{cl} variation. Another factor in operating with high I_b is that providing a high I_b may cause problems with the design of the circuit providing I_b. High I_b also increases the self-heating of the switch transistor and this is not as negligible as the equivalent circuit indicates because the base current flows through the transistor's base circuit, and the base-emitter or base-collector voltage drops of silicon transistors will generally exceed six-tenths of a volt.

Another method of selecting R_{cl} is to select I_b such that the voltage variation across the transistor will be a minimum when I_b varies. Optimum I_b for this condition can be found as follows:

$$V_{ce} = I\left(r_c' + r_e' + V_x/I_b\right) - I_b r_c' - (V_{ec})_I;$$

where I = emitter current

$$\frac{d V_{ce}}{d I_b} = -\frac{V_x I}{I_b^2} - r_c' \simeq \frac{\Delta V_{ce}}{\Delta I_b}$$

now if the circuit providing I_b is designed such that $\Delta I_b = K I_b$, then:

$$\Delta V_{ce} \simeq \left(-\frac{V_x I}{I_b} - r_c' I_b\right) K$$

and minimum ΔV_{ce} for changes in I_b will result when:

$$(I_b)_{opt} = \left(\frac{V_x I}{r_c'}\right)^{1/2} \qquad \text{VI - 8a}$$

or if the circuit is designed such that $\Delta I_b = K$, then minimum ΔV_{ce} will result when:

$$(I_b)_{opt} = \infty \qquad \text{VI - 8b}$$

Still another way to select R_{c1} would be to cause nominal:

$$I_b \Delta r_c' = I \Delta R_{c1} \qquad \text{VI-9}$$

and thus minimize the switch voltage error that occurs across the transistor due to variation in r_c' and R_{c1} ($\Delta r_c'$ and ΔR_{c1}).

The data of table 5 related to the NPN transistor indicates that for an I_b of three milliamperes I_b should be an average of about twelve times greater than I for minimum error. This probably implies a rather high I_b and certainly satisfaction of equations VI-7 and VI-8b implies a high I_b, but doubling I_b from three milliamperes to six milliamperes will only reduce R_{c1} by about twenty-five percent and an I_b greater than three milliamperes may not be justified when consideration is given to the circuit that must provide the current. To investigate the value of increasing I_b, the overall conversion problem can be considered with an I_b of 0 thru three or more milliamperes.

The switch and resistor circuits of the converter can be designed to provide minimum conversion deviations due to R_{c1} and amplifier input current variations, to the extent that the variations are known. Conversion deviations due to variation of the amplifier's input voltage and the PNP's V_{c1} are a function of the converter's Va/count and not its resistive circuitry and if the comparison amplifier's input resistance is sufficiently high, the variation of the PNP's R_{c1} will not cause a conversion deviation that is related to the converter's resistive circuitry. Accordingly the conversion

deviations caused by the amplifier's input voltage level and PNP transistors are not considered in the minimization procedure. Further, it is assumed that r'_c of the NPN transistor is low enough that variations in V_{c1} due to $\Delta(I_b-I)r'_c$ do not cause a conversion error that is large enough to warrant increasing R_{c1} by decreasing I_b. If the minimization analysis results in a complementing current or full scale decoder current that is appreciably different than I_b, the error due to r'_c should be given consideration.

Let R' = resistance of each complementing resistor then $R' \simeq$ parallel equivalent resistance of all decoding resistors.

R_i = input resistor of converter.

E = reference voltage with respect to common.

I_a = comparison amplifier's input bias current.

V_i = converter's input voltage.

V_a = voltage at the comparison amplifier's input due to V_i' with infinite amplifier input impedance.

V_d = voltage drift at summing junction due to ΔI_a.

$$V_a \simeq \frac{V_i' \cdot R'_{13}}{R_i + R'_{13}} \qquad \text{VI-10}$$

$$V_d \simeq 2\Delta I_a \cdot \frac{R_i \times R'_{13}}{R_i + R'_{13}} \qquad \text{VI-11}$$

where the factor 2 is included to refer the input bias change of the non-input transistor of a differential input pair to the amplifier's input (see comparison amplifier discussion of this section). The transistors of the amplifier are in a temperature controlled chamber.

$$\text{deviation due to } \Delta I_a \simeq 2\Delta I_a \frac{R_i \cdot R'_{/3}}{R_i + R'_{/3}} \Big/ \frac{V_i' \cdot R'_{/3}}{R_i + R'_{/3}}$$

$$\simeq \frac{2\Delta I_a R_i}{V_i'} \qquad \text{VI - 12}$$

$$\text{deviation due to } \Delta R_{c_1} \simeq \frac{K \Delta R_{c_1}}{R'} \qquad \text{VI - 13}$$

where K = complementing (that is, NPN switch to complementing resistor is not used).

K = 2 when naturally converting

and for correct conversions:

$$\frac{V_i'}{R_i} = \frac{E}{R'} \qquad \text{VI - 14}$$

total error = error due to ΔI_a + error due to ΔR_{cl}:

$$\text{" " } = \frac{2\Delta I_a R_i}{V_i'} + \frac{K \Delta R_{c_1} V_i'}{E R_i} \qquad \text{VI - 15}$$

differentiating with respect to R_i and equating the deviation to zero yields:

$$(R_i)_{\substack{\min. \\ dev.}} = V_i' \left(\frac{K \Delta R_{c_1}}{2e\ \Delta I_a} \right)^{1/2} \qquad \text{VI - 16}$$

The values of ΔI_a and ΔR_{cl} are not easily determined. Variations of I_a and R_{cl} with temperature are not particularly important because the temperature of the amplifier's input transistor and the switch transistors under study are controlled. The amplifier's input transistor's current gain and d.c. bias and leakage current establishes I_a and the switch transistor's inverse current gain is directly related to about half of R_{cl}. If it assumed that the current gains have long term stabilities that are similar and that the amplifier's leakage current deviation is small compared to its

bias current deviation, then it might be reasonable to assume that:

$$.7\,\Delta R_{c1}/R_{c1} = \Delta I_a/I_a \qquad \text{VI-17}$$

where the 0.7 factor reduced the effect of instability of ΔR_{c1} because part of R_{c1}, r'_e and r'_c, should have better stability than the resistance determined by current gain. It is shown later in this section that a typical I_a is about 1.3 microamperes. Resistor R_{c1} will typically be about two ohms with an I_b of three milliamperes. Solving equations VI-16 and VI-17 for a K of 1 and a V_i' of 10 volts yields an optimum R_i of 3000 ohms and with a K of 2, the optimum R_i will be 4200 ohms. An input voltage of 20 volts requires that R_i have twice the resistance as that of the 10 volt, V_i'. To satisfy the specifications, R_i should be 5000 ohms minimum for 10 volt sources and 10,000 ohms minimum for 20 volt sources. The converter's resistive circuitry will not be far from optimum if these values are used for R_i. If R_i is 5000 ohms, then R will be about 6000 ohms. If R is 6000 ohms and I_b is three milliamperes and R_{c1} is two ohms average, a one per cent change in all 13 of the converter's R_{c1}'s can cause a conversion error of about .000?%. This error per per cent change in two ohm R_{c1}'s seems small enough for a safe design even for higher R_{c1}. Reducing R_{c1} by increasing I_b does not seem worthwhile since the majority of the conversion error is determined by the minimum R_i and the amplifier drift, and since the fixed part of R_{c1} is sufficiently large that I_b cannot efficiently reduce R_{c1}.

The current bias of the trimmed PNP switch transistor is

selected for minimum nominal voltage drop with minimum voltage variation due to variation in I_b. Accordingly:

$$(I_b)_{opt} = \left(\frac{V_x I_e}{r_c'}\right)^{1/2} \quad \left(\text{See } \underset{\Delta I_b = K I_b}{\text{VI - 8a}}\right)$$

$$(V_{ec})_{IJ} + I_b r_c' = I_e(r_e' + r_c' + V_x/I_b) \qquad \text{VI - 18}$$

and satisfying both equations yields:

$$I_e = (V_{ec})_{IJ} / (r_e' + r_c') \qquad \text{VI - 19}$$

which gives an I_e of .39 milliamperes and an I_b of 2.4 milliamperes if $r_e' \neq r_c'$ is 2.25 ohms and V_x is 2.25 x 3 x 10^{-3} volts (see Table 5).

The effect of I_{op} and R_{op} can be investigated at this time. The NPN transistor has higher leakage current than the PNP and the PNP has higher R_{cl}. The NPN has a specified maximum I_{cbo} of fifteen microamperes with eighteen volts of collector voltage at 100°C. In an ambient below 80°C, the I_{ebo} should be less than four microamperes. If all 13 of the converter's PNP transistors have six ohms of R_{cl} and all 13 of the NPN I_{ebo}'s change two microamperes, the conversion deviation caused by the change will be about:

$$\frac{2 \times 10^{-6} \text{ amps} \times 6 \text{ ohms}}{12 \text{ volts}} \times 100\% = .0001\%$$

It seems safe to assume that a controlled temperature up to 80°C will not cause appreciable conversion deviations because of switch transistor leakage current.

The conversion errors due to self-heating of the converter's switch transistors can be investigated with the design choices thus far made.

The power loss in the switch transistor's R_{c1} is negligible compared to that of the transistor's base. The NPN transistor has a power derating factor of 2.6 milliwatts per degree centigrade and a base collector voltage drop that is about seven-tenths of a volt. The change on temperature of the transistors due to self-heating will be

$$\Delta \text{temp.} = (3\times10^{-3}\times .7)\ \text{watts} \times 1^{\circ}\text{C} / 2.6\times10^{-3}\ \text{watts} = 0.8^{\circ}\text{C}$$

The PNP transistor has a power derating factory of 1.3 milliwatts per degree centigrade and a base collector voltage that is about one volt. The change in temperature of the PNP transistor will be

$$\Delta \text{temp.} = (2.4\times 1)\ \text{watts} \times 1^{\circ}\text{C} / 1.3\times10^{-3}\ \text{watts} = 1.9^{\circ}\text{C}$$

The transistor temperature data following table 5 can be used in calculating the change in the switch transistor's equivalent circuit parameters due to self-heating. The errors caused by this self-heating is not very large.

The circuit of figure 33 shows a trimmed switch with its base current driver. When Q3 is cut off, current flows from reference common through the collector-base junction of Q2 to the -50 volt supply. This base current causes Q2 to saturate. The current is about ((50 volts - V_{be2})/18.2) milliamperes or about 2.7 milliamperes. The base-emitter junction of Q1 is reverse biased by the forward biased base-emitter junction of Q2, thus Q1 is cut off. Q1 becomes saturated when Q3 saturates. While Q3 is saturated, the base current of Q1 is about I2 $\not$ (I1 - I4) -I3. The emitter of Q3 is

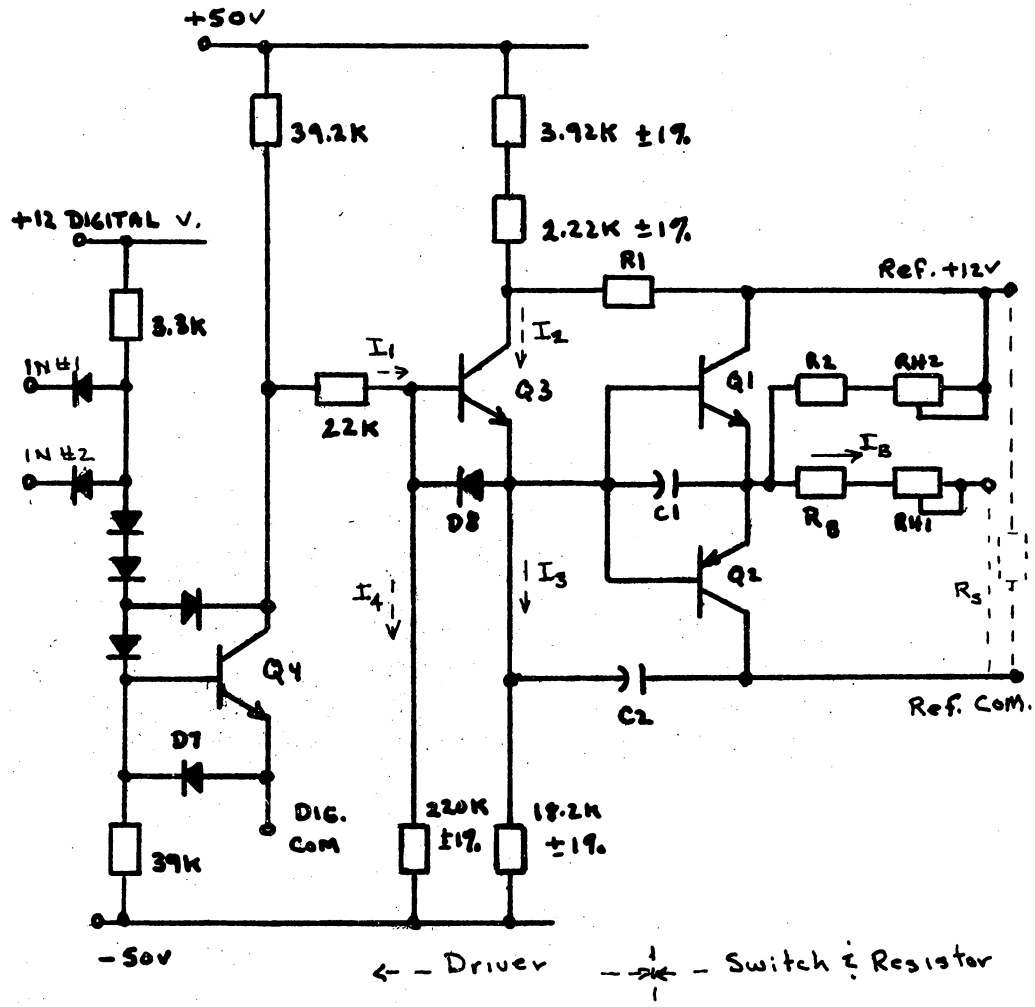


Figure 33. Switch and Driver Circuit for Most Significient Converter Bits

clamped to +12 volts by the base-collector diode of Q1 and the saturated drop of Q3 is about one-tenth of a volt, thus the base current to Q1 will be about three milliamperes.

The logic of the switch and driver is NAND logic with a "one" being defined as +5.5 to +12 volts. With "ones" on IN #1 and IN #2, Q4 is saturated; Q3 is cut off and Q2 is saturated. With a "zero" on IN #1 or IN #2, Q1 will be saturated.

Diodes D7 and D8 limit the base-emitter voltage of Q4 and Q3 to prevent voltage breakdown of their base-emitter junctions. The NPN transistor used in the switch has fairly poor carrier storage characteristics and if Q2 begins to conduct too quickly after Q1 has been conducting, a high transient current will flow from the +12 reference bus through Q1 and Q2 to common. Capacitors C1 and C2 slow down the transfer action of Q1 and Q2 to prevent the high transient current.

The switch and driver have been designed for light loading of the +12 volt reference supply. When Q1 is saturated, the +12 volt current will be about 3 milliamperes less the decoding or complementing current, I_B, ($2MA > I_B > 0$). The current thru the R1 and R2 branches will be small when Q1 is saturated. A resistor, e.g. R_S, can cause the total load on the 12 volt bus to be zero if I_B plus the current through R_S is three milliamperes. When Q3 cuts off, I2 and I_B become zero and a current flows from +50 thru R1 to the +12 volt reference bus. Also current flows from the +12 volt reference bus thru R2 to common. If the current thru R_S and R2 equals the current

thru R1, then the loading on the reference power supply is about zero. A nominal value of current through R2 is assumed for the purpose of selecting R1 in conjunction with R2 and the R_s that has been selected in conjunction with Q1's base current and current I_B. Most circuit packaging has some problem with IR drop in leads to the circuit. If R1 and the 50,000 ohm rheostat in series with R2 and the /12 volt lead to Q1 are each connected to a main bus, then the effect of Q1's lead IR drop on current I_B can be corrected for by adjusting RH1 since current will flow in the lead to Q1 only when Q1 is saturated. Similarly IR drop in the lead to Q2 can be corrected for by adjusting RH2 because current flows in this lead only when Q2 is saturated.

The stability of the base current to Q1 and Q2 is controlled by metal film resistors in the paths of I1, I2, I3 and I4 and by the stability of the positive and negative 50 volt supplies. These supplies are designed for .25% stability under conditions of loading and input line variations that are worse than typical of the systems in which the voltage-to-digital converter is used.

The resistor network of the decoder is shown in Figure 34. The continuous doubling of resistors as the bit order of the resistor decreases has been limited to four or five bits and then repeated. The continuous doubling process soon leads to very large valued resistances that are impractical to use and the repeated use of same valued resistors had decent economical advantages. That the circuit

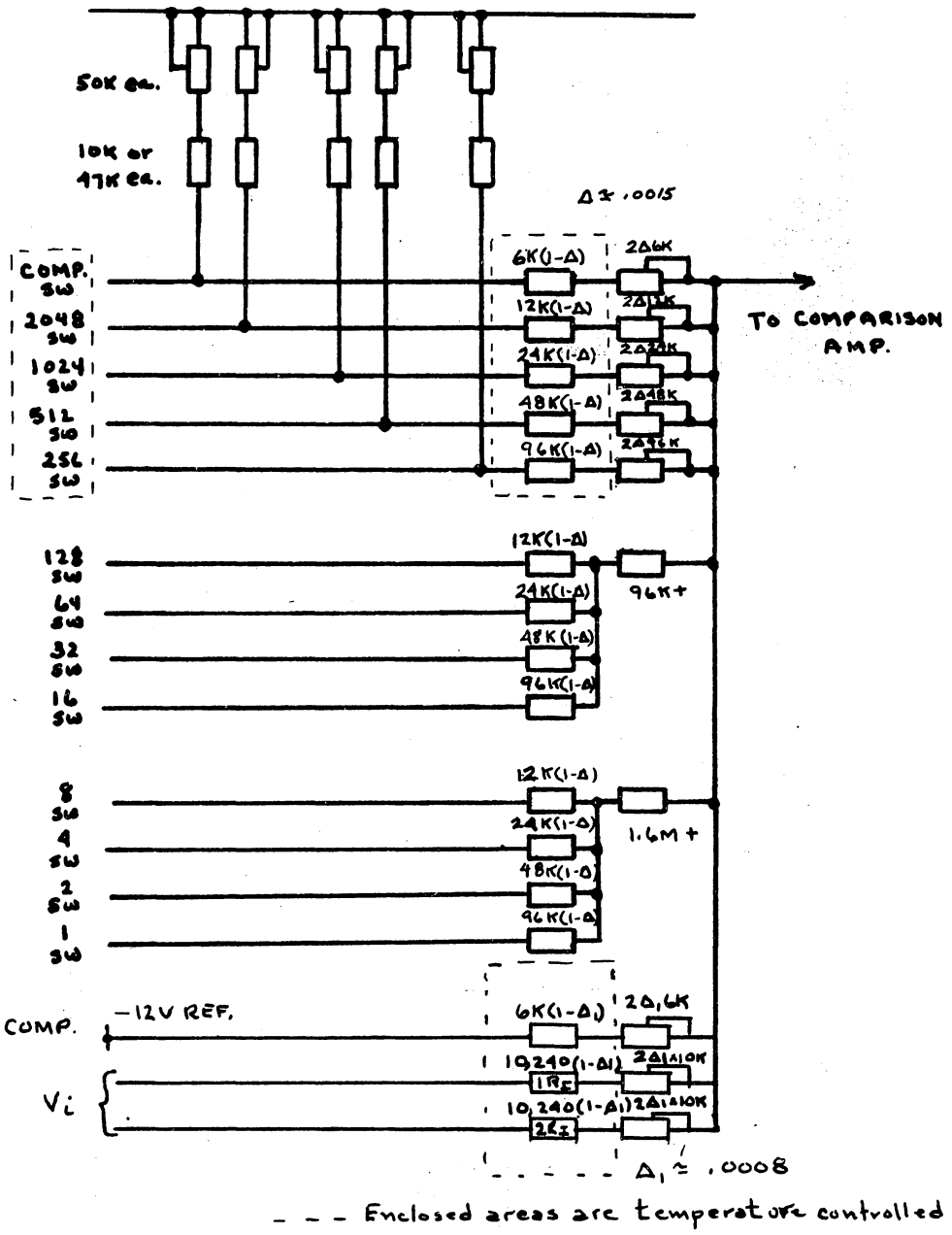


Figure 34. Converter Resistive Network

is workable can be readily seen from figure 13 where the derivation shows that e_o is proportional to the number being decoded. If e_o is proportional to the number being decoded, then the current through R_L is proportional to the number being decoded. The same circuit principals are applicable to the groups of resistors with "scaling" resistors connected between their output and the fixed potential at the amplifier's input, and thus the current out of the group's resistors is proportional to the number being decoded by the group's inputs. The main disadvantage of a scaled circuit is that the circuit is a voltage divider on the input side of the scaling resistor, and switch errors cannot easily be corrected for. In the application shown in figure 34, these errors are not particularly important because the total decoding contribution of the uncorrected switch is only a small part, about six percent, of the total 4095 count decoding signal. The switch and driver used with the 1 through 128 bit resistors is the same as that of figure 33 without the rheostats and controlled temperature. A more optimum base bias current of Q1 and Q2 could be selected but it was not done because errors contributed by not doing so are small enough that a different design did not seem worthwhile.

The converter's ten volt input connection is with the input voltage connected to $1R_i$ and $2R_i$ of figure 34. The twenty volt input connection is with the input voltage connected to $1R_i$ (or $2R_i$) while $2R_i$ (or $1R_i$) is connected to common. Connecting one of the input

resistors to common keeps the comparison amplifier's source resistance constant as desired, but the amplifier's input voltage will be somewhat less than calculated by equation VI-5 when the twenty volt input is used.

The resistors used for the converter's input, complementing and decoding functions are for the most part half watt, .01% accurate resistors with a .0005%/° centigrade maximum temperature coefficient. These resistors have a specified one year stability of .005% when operated at 50% power in the environmental conditions stated in the converter's specifications. The resistors that scale the eight least significant bits are somewhat less accurate and stable.

The temperature controlled chamber used for maintaining the temperature of components so noted in figures 33 and 34 is capable of holding $\pm 1^{\circ}C$ or so when its ambient varies from $25^{\circ}C$ to $70^{\circ}C$ or from $25^{\circ}C$ to $0^{\circ}C$. The thermal properties of the .01% resistors are such that their temperature rises $100^{\circ}C$ per watt of applied power. The worst error due to self-heating of the switched resistors will be due to switching of the complementing resistor. This error will be:

$$\frac{(12)^2}{6000} \text{ watts} \times \frac{100^{\circ}C}{\text{watt}} \times \frac{5 \times 10^{-4}\%}{1^{\circ}C} = .0012\% \text{ maximum}$$

The 2048 bit resistor can change .006% maximum, etc., thus the maximum change of the total decoder and complementing current will be about .0012%. Other conversion errors and deviations, due to resistance characteristics, can be readily calculated from the resistor specifications just given.

A pair of 12 volt supplies is required for referencing the converter's decoder and complementing circuits. The supplies designed for the reference function are shunt regulated circuits with the -12 volt supply designed to track the +12 volt supply. Positive and negative 50 volt supplies provide the bulk unregulated voltage for the reference supplies. The shunt regulator design keeps low voltage across the reference supplies' output transistors and since the current of the positive reference voltage flows in and out of the supply, the efficiency of this supply can be as great as that of a series regulated supply. The tracking feature of the -12 volt reference supply reduces conversion errors due to reference supply deviation by about one-third. It can be shown also that the maximum conversion deviation due to power supply deviation with tracking reference supplies is no greater for a two branch complementing circuit, as in Figures 35 and 27, than for a one branch complementing circuit as in Figure 26. (The one and two branch circuits have a maximum error of $(\Delta E R_1 + \Delta(-E) R_1)/R_c$ when P is zero and both supplies vary whereas the two branch circuit has more error than the one branch if the reference supplies are non-tracking (see tables 6 and 7). A further advantage of the tracking power supply is that its reference can be resistive and thus the cost and the reference deviation of the supply should be less than that of an independently referenced supply.

A schematic of the reference supplies is given by Figure 36.

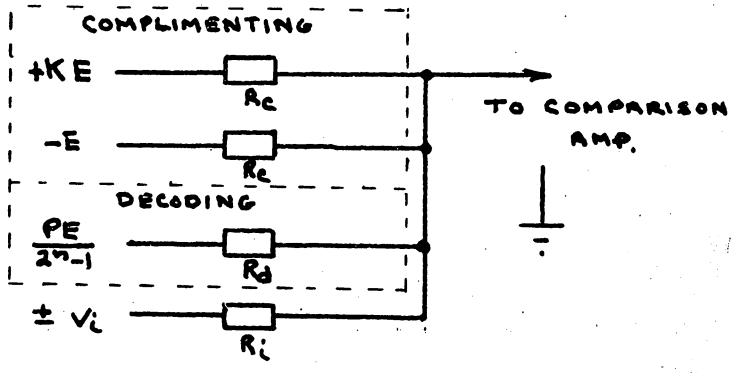


Figure 35. Equivalent Converter Resistive and Reference Network

Table 6. Input Voltage Deviation Versus Converter Operating State With Tracking Reference Supplies

V_i	K	P	Dev. Sup.	V_i Deviation
-Max.	1	2^n-1	$\neq E$	$\Delta ER_i/R_d$
-Min.	1	0	$\neq E$	0
$\neq$Min.	0	2^n-1	$\neq E$	$\Delta ER_i(R_c-R_d)/R_cR_d \simeq 0$
$\neq$Max.	0	0	$\neq E$	$\Delta ER_i/R_c$
-Max.	1	2^n-1	-E	$\Delta ER_i/R_c$
-Min.	1	0	-E	"
$\neq$Min.	0	2^n-1	-E	"
$\neq$Max.	0	0	-E	"

Table 7. Input Voltage Deviation Versus Converter Operating State With Nontracking Reference Supplies

V_i	K	P	Dev. Sup.	V_i Deviation
-Max.	1	2^n-1	$\neq E$	$\Delta ER_i(1/R_d \neq 1/R_c)$
-Min.	1	0	$\neq E$	$\Delta ER_i/R_c$
$\neq$Min.	0	2^n-1	$\neq E$	$\Delta ER_i/R_d$
$\neq$Max.	0	0	$\neq E$	0
-Max.	1	2^n-1	-E	$\Delta ER_i/R_c$
-Min.	1	0	-E	"
$\neq$Min.	0	2^n-1	-E	"
$\neq$Max.	0	0	-E	"

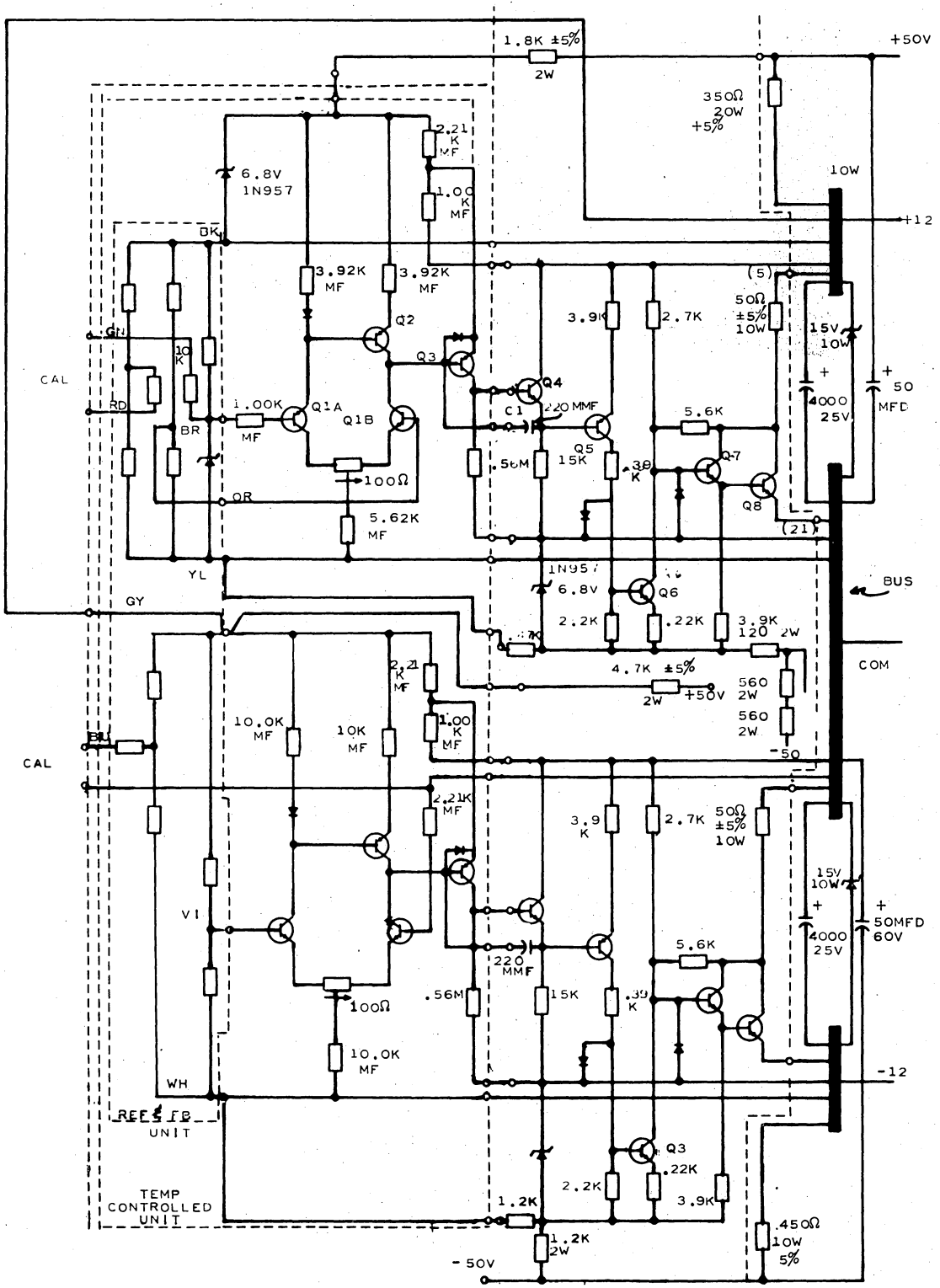


Figure 36. Circuit of Reference Supplies

These supplies are designed for ±50 milliamperes of output current. This current is appreciably more than required for the converter, but it permits broader applications of the supplies.

The operation of the ±12 volt supply can be explained with the aid of Figures 37 and 38. Figure 37 is a simplified block diagram that presents the basic elements of a closed loop circuit that is typical of the reference voltage supply circuit. The reference and feedback of this diagram are voltage elements. The gain between the output of the reference/feedback summing junction and the output begins with a voltage to current conversion. This stage is followed by current gain elements that include a major stabilizing time constant T3. The output of the current gain element is summed with output current and this sum feeds a RC element that provides current to voltage conversion and system stabilization. The output of the RC network is the power supply's output voltage and this is fed back to the reference/feedback summing junction by a resistor bridge of element H. Time constant T1 provides the supply's lowest low frequency roll off. This break is terminated when the internal resistance in capacitor C is equal to the capacitive reactance of C. The termination occurs at $\omega = 1/T2$. Time constant T3 provides a second roll off which causes GH of the power supply to cross the unity gain axis. The supply's frequency response characteristic is designed to cross the unity gain axis at a frequency that is safely lower than the break frequencies of the circuit transistors

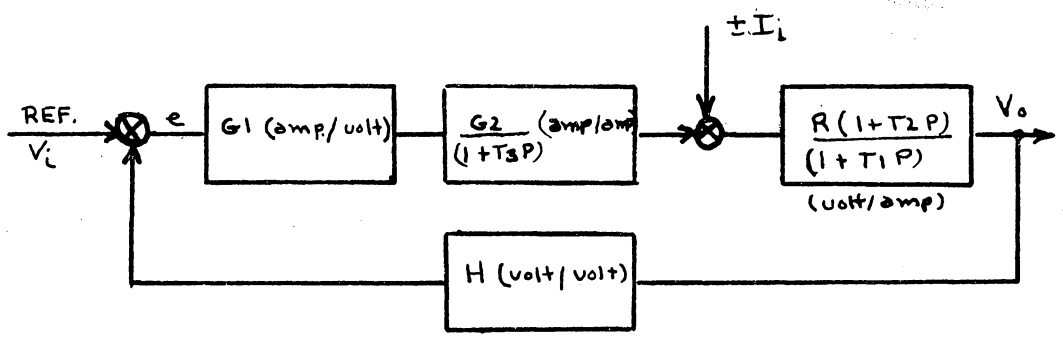


Figure 37. Block Diagram of Reference Power Supply

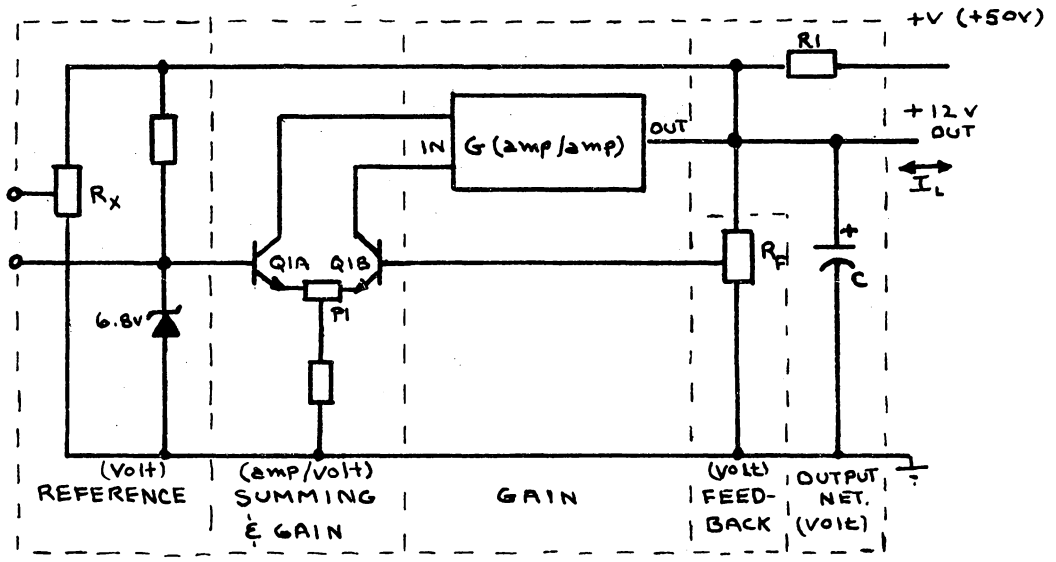


Figure 38. Hybrid Block/Schematic Diagram of Reference Power Supply

and miscellaneous circuit elements.

Figure 38 provides a diagram that is something of a block diagram and schematic hybrid of the ∕12 volt supply. The reference and gain elements of the supply receive their operating power from the ∕12 volt bus of the supply. Because the output voltage of the supply is very stable, it would be difficult to improve the performance of the supply with external reference power. There is some interplay between the reference and circuit power functions of the ∕12 volt reference supply, but the effect is of secondary nature. The ∕12 volt bus is used to bias a 6.8 volt zener diode. The dynamic impedance of this zener is low compared to the resistor that biases it, thus in spite of 12 volt bus variations, the zener's output voltage is a stable reference source for transistor Q1A. Tapped resistor R_T feeds part of the output voltage back to the base of Q1B. Resistor R_T is designed such that its tapped output voltage is equal, ∕_.1%, to the zener voltage when R_T and the zener bridge are connected across 12 volts, thus the base voltages of Q1A and Q1B are almost equal. Gain element G amplifies the difference of current that exists between the collector current of Q1A and the collector current of Q1B. For the power supply to have an output voltage of 12 volts, the current difference should be about

$$\frac{\frac{50-12}{R1} - \frac{12}{R_F} - I_{reg} \pm I_L}{G} \qquad \text{VI - 20}$$

Where I reg = bias current to the elements of G, zener, etc.

I_L = load current.

Potentiometer P1 is adjusted to offset the collector bias currents of Q1A and Q1B to satisfy the above equation and cause the supply's output to be 12 volts.

With fixed resistors in the output stage, the current from G must change by an amount exactly equal to any I_L change if the power supplies output voltage is to be unaffected by I_L changes. The supply is by design a type zero regulator and as such it does not have an output voltage that is completely independent of I_L but the supply regulates well enough that the output voltage is almost independent of I_L. The regulation is achieved as follows: Notice that the base voltage of Q1B changes when the output voltage changes. This changes the base, emitter and collector currents of Q1B. The change in Q1B's emitter current changes the voltage at the slider of P1. The base of Q1A is at a fixed potential and the change of voltage at the slider of P1 causes the emitter current of Q1A to change in an opposite manner to the Q1B emitter current change. To take an example:

1. I_L decreases (less current out of the supply).
2. V out increases (goes positive).
3. Base voltage of Q1B increases.
4. Emitter and collector currents of Q1B increase.
5. P1 slider voltage increases.

6. Emitter and collector currents of Q1A decrease.

Thereafter, G amplifies the current difference of the Q1A and Q1B collector currents. The supply is designed such that an output voltage change of less than one-tenth of a millivolt will be amplified to compensate for a 50 milliamp change in I_L. Line voltage changes are much the same as I_L changes since a change in ΔV has the effect of changing the voltage across R1 and this changes the current summing at the output junction.

The output voltage also changes whenever a component in the supply changes in value, gain, operating bias, etc. For the most part, the output voltage change occurs when the supply's reference or feedback or summing junction bias changes. The latter of these items is the least obvious. The summing junction bias will change when Q1A and Q1B change their relative operating points. The major causes of the operating point changes are transistor gain change, leakage current change and emitter base voltage change. To minimize these transistor variations, Q1A and Q1B are purchased as a pair of transistors in a single package with matched (more or less) gain, base voltages and base voltage temperature coefficients. Transistor parameters are particularly sensitive to temperature variation. To reduce the effect of temperature variations, Q1A, Q1B and 2 of G's transistors are packaged in an environment that is maintained at 80°C. (The use of differential transistors for low level amplification is given further consideration in the comparison amplifier

discussion of this section). The reference zener, feedback and a calibrating bridge (see next paragraph) network are also packaged in this controlled environment.

The accuracy of the voltage supply is established by comparing the reference voltage to a voltage that is taken from an unloaded resistor bridge, R_X, that is similar to the feedback bridge. The zener diode that provides the reference voltage is an aged device that is selected for good expected stability. The calibrating resistor bridge, R_X, is designed in conjunction with the selected zener to have an output voltage that is the same as that of the zener when 12 $\pm$.005% volts are applied across the bridge and the zener with its series bias resistor. The voltage of the $\pm$12 volt supply is set by adjusting P1 until there is no voltage between the zener and bridge outputs. The resolution of the adjustment is about .0005%. The calibrating technique just described permits adjusting the $\pm$12 volt reference supply's voltage without a voltage standard other than the supplies reference zener. This makes possible "in use" adjustment of the supply where laboratory standards are not available. The adjustment will eliminate practically all deviations of the power supply except those of the zener and calibrating bridge. The zener and calibrating bridges are specified to track with not more than .005% per year correction of the $\pm$12 volts.

The resistor bridge is designed to provide an output voltage equal to the zener voltage when the 12 volt supply has 12 $\pm$.005%

volts output. These voltages are made equal when the resistor bridge and the zener are at temperature in the temperature controlled environment. The IR drop of the wires leading from the output to the reference calibrating and feedback circuits are canceled by bias currents into or out of the exact point at which the reference and feedback voltages were measured when the circuit was manufactured. In the +12 volt supply, cancelling current enters the +12 volt junction through a 6.8 volt zener diode. An almost equal current leaves the network through 470 ohms to -6.8 volts and through the 3.21K ohm bridge between +18.8 and +12 volts and through the summing stage (see Figure 36).

The -12 volt supply is very similar to the +12 volt supply. The major differences are in the reference, feedback and summing stage. The summing stage of the supplies are not as different as it might seem. The 10K ohm resistors in the -12 volt supply's summing stage give the differential transistors (Q2A - Q2B) about the same current bias as that of the differential transistors of the +12 volt supply. The reference and feedback summing function of the -12 volt supply is accomplished by taking the difference of voltage that exists between common and a resistor bridge output (with respect to common), that is, about 50% of the algebraic difference of the +12 volt and -12 volt bus voltages. The -12 volt supply's output is adjusted with a potentiometer in its summing stage until the -12 volt output is such that a null voltage

exists between the common bus and an unloaded 50% tapped resistor bridge between +12 and -12 volts. The initial accuracy of the bridge tap is .003% and the deviation of the bridge is specified to be less than .001% per year. The -12 volt supply has its reference, calibrating and feedback line drops canceled in a manner similar to that of the +12 volt supply. The resolution of the voltage adjustment is about .0005%.

The -12 volt supply takes bias current from the -50 volt supply through 450 ohms and the 6.8V zener network that is biased from -50 volts. The current provided by these two paths is about the same as would be obtained from one 350 ohm path as was done for the +12 volt supply.

The ±12 volt supplies can be shorted from output buses to common or output bus to bus (+12 to -12). When this happens, current from the 50 volt buses bypasses the regulating parts of the power supply and the regulator collapses for lack of bias. Fifteen volt zener diodes are connected across the outputs of the power supplies. These zeners limit the output voltage to about 15 volts if the supply's regulator opens. In addition, the forward biased zeners keep the output buses within a volt or so from common when the +12 and -12 volt buses become shorted.

The load regulation, servo stability and temperature drift of the reference supply are aspects of the design that require further explanation.

It was stated in Section V that a GH up to 100,000 is required for .001% voltage regulation. Figure 37 can be used to verify the need of a GH of 100,000. Further the gains required of G1, G2 and H can be established from Figures 36, 37 and 38. From Figure 37:

$$e = V_i - V_o H$$

$$V_o = e(G_1 G_2 R) + I_L R$$

$$= (V_i - V_o H)(G_1 G_2 R) + I_L R$$

$$= \frac{V_i G_1 G_2 R}{1 + G_1 G_2 R} + \frac{I_L R}{1 + G_1 G_2 R H} \qquad \text{VI-21}$$

If the supply has no excess load capability:

$$\frac{V_i}{H} \simeq I_L R \qquad \text{VI-22}$$

and if V_o is to vary no more than .001%, $1 + G_1 G_2 R H$ must be 100,000 minimum.

For .001% or better load regulation:

$$\frac{I_L R}{1 + G_1 G_2 R H} \leq .12 \times 10^{-3} \text{ volts}$$

and approximately:

$$\frac{I_L R}{G_1 G_2 R H} \leq .12 \times 10^{-3} \text{ volts}$$

Given: $I_L = .05$ Amps

$$G_1 G_2 \geq \frac{.05}{.5 \times .12 \times 10^{-3}} = 832 \text{ amps/volt}$$

it is shown in Appendix A that G1 (see appendix for definition of components of G1) has a minimum gain that is about (1/125) amperes

per volt for the ±12 volt supply; therefore G2 must have a minimum gain of about 104,000 amps per amp. It can be verified with some effort, that the gain of G2 is greater than 104,000. The minimum no load GH of the reference supply is:

$$GH_{\text{allowable min.}} > G162\,RH$$
$$> 822 \times 136 \times .5$$
$$> 55,000$$

when R is shown to be 136 ohms in Appendix B. The GH of 55,000 is adequate for .001% regulation because the .05 ampere load on the supply is about 50% of the supply's total output current.

The frequency response characteristics of a high gain, voltage supply must be well controlled until the high frequency loop gain ($G(\omega)\,H(\omega)$) is less than unity with sufficient phase margin for the supply to remain stable for varying component values. The controlled frequency response of the supply must be unity with the desired phase margin at some frequency that is less than the uncontrolled roll off or lead frequencies of the various components and wires of the supply. Good transient response, however, requires that the unity gain frequency be high.

As usual in power supply design, the output capacitor of the supply provides the lowest frequency roll off of the circuit. The characteristics of capacitor are such that the roll off frequency will be relatively constant but the characteristics of forward gain transistors are such that the gain at which the roll off occurs can be quite variable. Higher gains at roll off require

lower roll off frequencies if the gain is to be unity at a frequency that is near to that of the uncontrolled frequency response elements of the supply. It is not uncommon to have a seven to one gain spread for a single type of transistor that is subjected to an ambient that varies from 0°C to 70°C. For the most part, gain variation in the reference supply is minimized with localized D-C emitter and collector feedback. The output filter has the no-load transfer function derived in Appendix B:

$$\frac{V_o}{e_i} = \frac{R\,(1 + 120\times10^{-4}P)}{(1 + 4000\times10^{-6}RP)} \qquad \text{VI - 23}$$

where without load, R is about 136 ohms, thus:

$$\frac{V_o}{e_i} = \frac{136\,(1 + 120\times10^{-4}P)}{(1 + .54P)}$$

R can vary appreciably with load changes but the effect of changes in R on the unity gain frequency of the supply is small because both the gain at roll off and the roll off frequency vary directly as R. The lead and lag of the output filter are about 1600:1 apart and if GH is 50,000 or more, the output filter of the supply does not cause the high frequency gain of the supply to be unity. A lag around transistors Q3 and Q4 attenuates the high frequency gain of the supply to cause a unity loop gain at about 180,000 radians. The transfer functions of the Q3-Q4 stage will be about

29. $$\frac{e_{o4}}{e_{b3}} = \frac{A_{i3\text{-}4}}{1 + A_{i3\text{-}4}(Z_L/Z_f)} = \frac{A_{i3\text{-}4}}{1 + A_{i3\text{-}4}\times15\times10^{3}\times220\times10^{-6}P} \qquad \text{VI - 24}$$

Both the gain and lag time constant of Q3-Q4 stage vary directly as the open loop D-C current gain A_{i3-4} and thus, variation in A_{i3-4} will not affect the frequency at which the supply approaches unit gain. The nature of the high frequency stabilization is such that D-C stabilization is not required for Q3-and Q4, accordingly these two transistors are operated at almost full gain to improve the D-C regulation of the supply.

The differential base voltage drift of transistors Q1A and Q1B is about 15 microvolts per degree centigrade, and Q1A and Q1B have minimum current gains of about 30 at 25°C and a gain ratio $\beta 1A/\beta 1B$ that is greater than 80% if Q1A is the lowest gain transistor of the pair. Transistors with better characteristics for temperature stability are available and certain circuit techniques are available for reducing the temperature drift of differential pairs of transistors. Q1A and Q1B have been placed in the temperature chamber that contains the reference in lieu of improved transistor or more complicated circuit techniques. Likewise Q2 and Q3 were placed in the chamber. The need for temperature control of Q2 and Q3 can be studied as follows. It can be shown in a manner similar to that used for calculation the effect of a load disturbance on the power supply that a temperature disturbance current I will effect a supply's output voltage such that:

$$\Delta V_o = \frac{\Delta I \, G_F}{1 + G_F G_B H} \simeq \frac{\Delta I}{G_B H} \qquad \text{VI-25}$$

Where G_F = gain forward of ΔI

G_B = gain behind ΔI

If ΔI occurs between Q2 and Q3 at the base of Q3, then from equation VI-25:

$$\Delta V_o \simeq (\Delta I \times 125)/.5 \simeq 250 \Delta I$$

where $G_B = 1/125$ from APPENDIX A

and a ΔI of one microamp will cause about .002% output voltage change.

Transistor Q3 is biased at thirty microamperes and at this bias it has a minimum h_{FE} of about thirty. The I_{CO} of Q3 is about .01 microamperes maximum at 25°C. If the temperature of Q3 is increased from 25°C to 70°C, the current into the base of Q3 can be expected to decrease by something like a half of a microampere and the voltage supply's output voltage will change about .001%. An .001% voltage change in the reference supply is tolerable, but Q3 was heated since space in the temperature chamber permitted. Q4 will cause less output voltage deviation than Q3 because of temperature change, Q5 less than Q4, etc.

Comparison Amplifier

The comparison amplifier is essentially a voltage polarity detector. The amplifier must detect voltage polarity with a small input signal and it must recover quickly from having sensed a large input signal. The magnitude of an input signal per count of difference between the converter's input and decoder's output is

calculated as follows:

$$\frac{V_a}{\text{COUNT}} = \frac{V_i}{4000} \times \frac{R1}{R1 + R_i}$$

$$\frac{1}{R1} = \frac{1}{R_c} + \frac{1}{R_i} + \frac{1}{R_d}$$

R_c = complementing resistance = 6K ohms
R_d = parallel equivalent decoder resistance 6K ohms
R_i = converter's input resistance

$$\left.\frac{V_a}{\text{COUNT}}\right|_{V_i = 10V} = 2.5 \times 10^{-3} \times \frac{2000}{7000} = 715 \times 10^{-6} V$$

$$\left.\frac{V_a}{\text{COUNT}}\right|_{V_i = 20V} = 5 \times 10^{-3} \times \frac{1.67}{11.67} = 715 \times 10^{-6} V$$

The maximum signal to the comparison amplifier can be 8000 times that of a single count error if the decoding, complementing and input currents have certain values that can occur, for example, if the converter's decoding and switched complementing current is zero from a previous conversion and the converter's input voltage is negative by a full scale amount. It is desirable that the comparison amplifier detect the polarity of a signal that is five to ten per cent or less of a count. If the comparison amplifier has full scale output for ten per cent of a count, its maximum input will be 80,000 times greater than that required for full scale. The amplifier must have good transient response to recover from maximum input in time to detect ten per cent of a count. The time permitted

for a comparison can be made longer for comparisons with higher order decoder bits but this complicates the logic and timing circuits of the converter. It will be shown later that the logic and timing of the designed converter provides 90 microseconds for comparisons with its complementing bit and 40 microseconds for conversions with other bits.

The comparison amplifier must be designed with good D-C stability if it is to operate from a fifty microvolt or so signal. The usual technique for providing D-C gain stability in an amplifier is for the open loop amplifier to have excess gain that is decreased to a desired value by negative feedback. Linear, negative feedback reduces the D-C drift of a linear amplifier by the same amount as it reduces the amplifier's open loop gain. The comparison amplifier is essentially a high gain switch that needs only two values of output voltage and thus feedback is of no obvious value in reducing the drift of the amplifier if it reduces its gain by a like amount.

Figure 39 shows the circuit used for the converter's comparison amplifier. Feedback is used in several parts of the circuit for reasons that will be explained later. Most of the amplifier's drift will be due to drift in the first or first and second stages of the amplifier. Differential transistor packages as used in the first stage of the comparison amplifier are being strongly advocated as a means of avoiding the transient and noise problems associated with low level D-C amplifiers that use chopper techniques for achieving

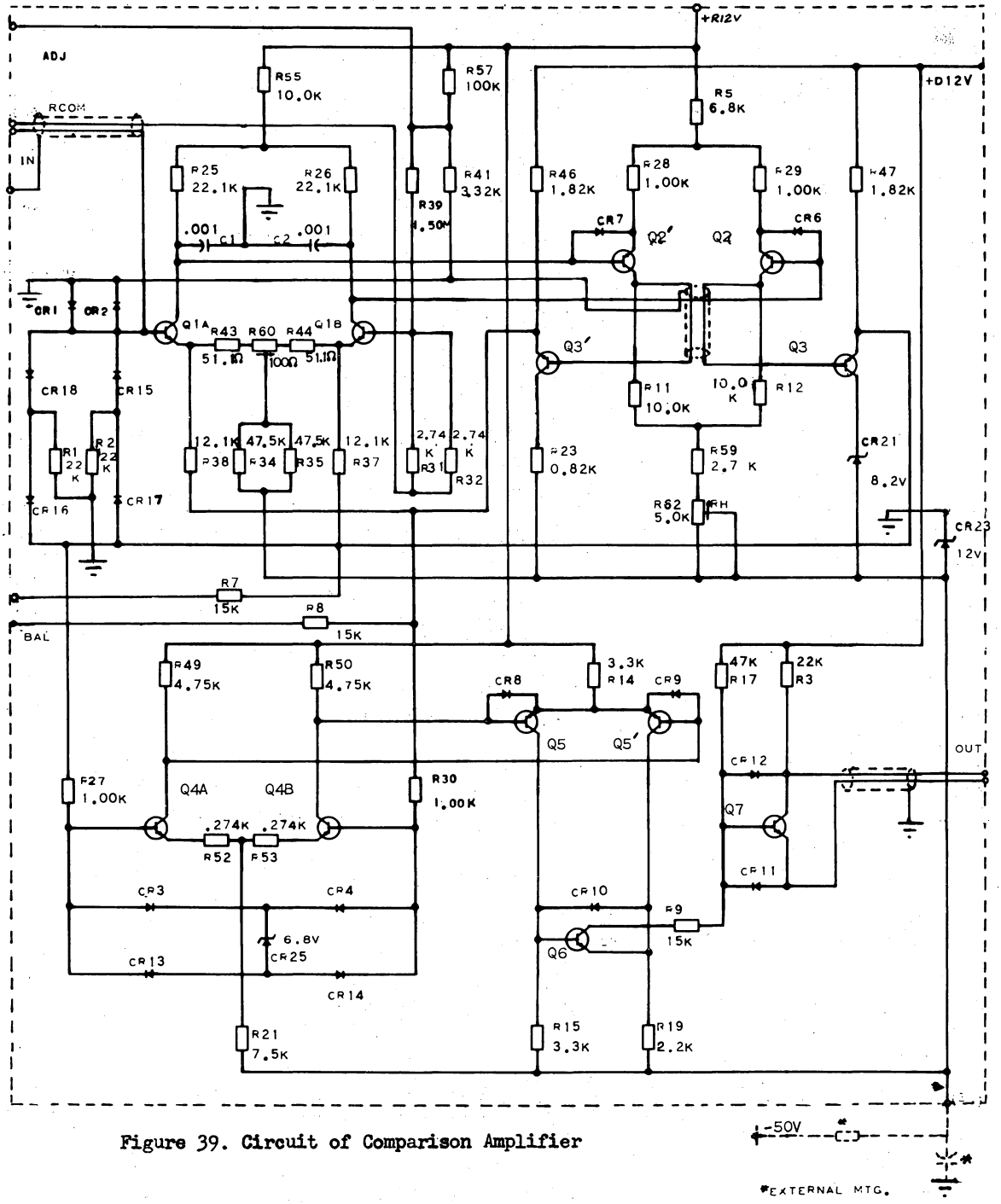


Figure 39. Circuit of Comparison Amplifier

low drift operation [30, 31]. The differential transistor circuit is particularly well known for its temperature stability, but these transistors are not temperature stable enough for the comparison amplifier unless temperature compensation or temperature control is provided for the transistor pair. A self-compensating, low frequency amplifier that utilizes the base-emitter diode's temperature coefficients of differential transistors has been built with an equivalent input drift of .05 microvolts per degree centigrade [32]. This circuit and probably most other temperature compensated circuits of good quality require that the compensation be adjusted while the transistor pair is subjected to a varying ambient. The comparison amplifier uses temperature control in lieu of compensation as a means of providing a circuit with low drift in a varying ambient. In spite of decreased need for stable temperature operation because of temperature control, the characteristics of differential transistors are still desirable in the comparison amplifier. The matched gain characteristic of the pair of transistors reduces amplifier deviation due to line voltage variations and the matched gain combined with matched base-emitter voltages make it possible to adjust the D-C bias of an amplifier with a simple adjustment that has good resolution. Also differential transistors have inherent reliability, low leakage currents, low noise and high gain with low D. C. bias currents [33]. The high gain and low leakage characteristics permit the transistors to have low D. C. base, emitter

and collector current biases. Low bias makes the transistor's output voltage less sensitive to changes in its D-C current gain, thus a major cause of drift can be reduced.

The input transistors (Q1A and Q1B) of the comparison amplifier are a pair of passivated planar transistors in a single package. The h_{FE}'s of the transistor are matched within 20%, the base-emitter voltages are matched within five millivolts and the relative change between base voltages is less than 20 microvolts per degree centigrade of difference in temperature of the transistors. The transistors have a minimum 25°C gain of 100 with 100 microamperes of collector current and the maximum I_{cbo} is $.01 \times 10^{-6}$ ampere at 45 volts and 25°C.

The input differential transistors of the comparison amplifier of Figure 39 are biased with a collector current of 200 microamperes and an emitter-collector voltage of four volts. This bias, combined with temperature control and the above mentioned characteristics makes a decent input stage for the comparison amplifier. The effect of input stage h_{FE} changes on the conversion is readily calculated. The transistors are in 80°C controlled ambient, thus their h_{FE}'s will be about 150 minimum. The amplifier input current bias will be about 1.3 microamps into the base of each transistor. The converter's input, decoding, and complementing resistors have about 1420 ohms of parallel equivalent resistance, thus the amplifier's input bias voltage is about two millivolts. Two millivolts is

equivalent to the voltage of 3 counts of signal. The circuit is designed with 1440 ohms at the base of the transistor opposite to the input base, thus, a 1% change in gain of the transistor's relative to each other will cause a .0007% offset error.

The comparison amplifier is designed to operate as follows. The circuit is essentially a series chain of four differentially operated pairs of transistors and two output transistors Q6 and Q7. Initially, the amplifier's 100 ohm potentiometer and 5000 ohm rheostat are adjusted until the voltages at the emitters of Q3 and Q3' are at common potential. A clamp consisting of diodes CR14, CR15, CR16, and CR18 prevent these emitters from changing more than ± 1.5 volts with respect to common. Transistors Q4A and Q4B are each biased at 0.75 milliamperes, thus, their collector voltages are about 8.5 volts positive with respect to common and their base potential. Assume that the signal to Q4A is positive going and thus tending to saturate Q4A. The signal to Q4B will tend to cut off Q4B. The collector of Q4B goes positive 3.5 volts and the transistor cuts off. Q4A's base collector bias is now about 5.0 volts. When Q4B cuts off, the gain of Q4A shifted from 4,750/300 to 4,750/7800, thus Q4A cannot possibly saturate with a base signal that goes to a positive 1.5 volts. The change of gain prevents saturation of Q4A and thus improves the transient performance of the amplifier. The transistor stages with Q5 and Q5' avoid saturation in much the same manner, although gain non-

linearities due to diodes CR8, CR9 and CR10 and the base-emitter diode of Q6 have an effect on the operation.

The transient response of the amplifier is largely determined by the amplifier circuit between the input terminal and diodes CR14 through 18. Ignore the function of R37, R39 and R57 for the present. The emitter of Q3 is at common potential when the input signal is zero, thus no current flows through CR14, CR15, CR16 and CR18, and current will not flow through these diodes when the amplifier senses small input signals, therefore, the circuit has full gain for small input signals. As the input signal becomes larger, the diodes conduct and tend to reduce the signal at Q1A's base. This provides a clamping action that limits the voltage change of Q3 and Q3' emitters to about one and one-half volts each for an input signal that is as large as twice the decoder's full scale signal.

Derivations in Appendix C show that the small signal, low frequency, double ended output gain of the amplifier circuit through Q3 and Q3' is one hundred and four if the diode clamp is open, while the gain is seven hundred and eighty if the clamp and pair of 12,100 ohm feedback resistors are open. The .001 microfarad capacitor of Q1A and Q1B causes these transistors to roll off with a twenty microsecond time constant, thus the open clamp, open loop roll off frequency is about fifty thousand radians per second and the open diode, closed loop roll off is about three hundred and seventy-five thousand radians per second or sixty thousand cycles per second.

The gain of the amplifier from its input to the output of Q3 is about fifty-two, thus, the unity gain crossover frequency due to the input transistor's lag will be near three megacycles. The four PNP transistors have minimum gain bandwidth products of 300 megacycles (at 20 milliamperes of I_e) and maximum output capacitances of 4×10^{-12} farads. These transistors should not contribute appreciable to the frequency response of the amplifier at frequencies less than three megacycles, thus, the amplifier will be stable with a diode clamp that provides nearly unity gain operation.

In operation, a positive three volt equivalent decoding, complementing, and input signal will cause the emitter of Q3 to be negative by one and one-half volts. If the comparison amplifier is to settle properly, an input voltage change to a negative fifty microvolts should cause the amplifier to change states in about forty-five microseconds or less. If the amplifier can D-C switch output states with a sixty microvolt deadband ($\pm$ 30 microvolts), the emitter of Q3 must settle to a positive one and one-half millivolts within the given forty-five microseconds. To do so with a fifty microvolt input signal, the emitter must settle to within one millivolt of its final value, (that is, to within $1 \times 10^{-3} \times 100\%/1.5 =$ (.067% of its final value). The time elapsed for linear settling to .067% requires the time of about 7.3 time constants. With the diode clamp not conducting, the amplifier's time constant due to the .001 microfarad capacitor is about 1 second/(375×10^3)

or about 2.7 microseconds. Since the diode does speed the amplifier's change of state, the amplifier should always be able to change output states in less than twenty microseconds plus the settling time of the transistors that follow Q3 and Q3' if the amplifier has an input D-C deadband of sixty or less microvolts and if the input signal it is to detect is fifty or more microvolts. It is shown in Appendix C that the amplifier's gain is probably in excess of 7×10^6 volts per volt and thus the amplifier has more than adequate gain for the required deadband. It is actually necessary though that the input signal of the amplifier be large enough to satisfy the deadband requirements of the amplifier over and above the internal noise of the amplifier as referred to the amplifier's input. It is stated in Section VII that a measured D-C input signal required to switch the amplifier from one output state to the other was twenty microvolts in a test rig and forty microvolts when the amplifier was operated in the converter, thus the noise is sufficiently low to permit the amplifier to operate as calculated.

The 100 ohm trimmer and two 51.1 ohm resistors in series with the emitters of Q1A and Q1B increase the amplifier's input resistance and provide a means of canceling the effect of unbalanced components in the amplifier. The voltage gain of the first stage is made fairly high to reduce the effect of drift in Q2 and Q2' and then feedback through the two 12,100 ohm resistors is used to decrease the gain and increase the bandwidth of the amplifier loop

inside of the diode feedback clamp. The increased bandwidth is necessary to permit the amplifier to settle as it comes out of clamped operation. The feedback through the 12,100 ohm resistors also increases the amplifier's D. C. and dynamic input resistance.

Feedback is used in the emitters of Q4A and Q4B to reduce the loading on Q3 and Q3' and to provide a controlled gain for the non-saturating operation previously described.

Resistors R39, R41, and R57 provide the converter's half count offset. The comparison amplifier is adjusted to have an uncertain output when all decoder bits are "0", the input voltage is zero volts, the complementing resistors have equal and opposite currents, and the amplifier's "adjust" terminal is connected to common. The common to "adjust" connection is opened after the amplifier is adjusted and 362 microvolts is caused across R31 and R32. This voltage causes about one-half count offset with polarity that is the same as that of the input voltage during a normal conversion.

VII VOLTAGE-TO-DIGITAL CONVERTER CIRCUITRY

Operation

The decoding, complementing, and comparing operation of the successive approximation converter have been given enough consideration that the circuit connections associated with these operations should require only minor explanation. These connections are shown in Figure 40.

The logic of the converter has thus far been given only the brief treatment in Section III. Figure 41 provides a logic diagram for the converter. The following notations are used on the logic diagram:

1. Type logic is shown by abbreviation in the center of each logic symbol (box).
   a. SR is shift register.
   b. FF is flip flop (storage function).
   c. SS is single shot (monostable vibrator or one-shot).
   d. OR is inclusive "or" logic for true inputs.
   e. AND is "and" logic for true inputs.
   f. INV is inverter (negator).
   g. DELAY is propagation type delay that is used for logic purposes.
2. Inputs are to the left top, or bottom, of a logic symbol.
3. Outputs are to the right of a logic symbol.

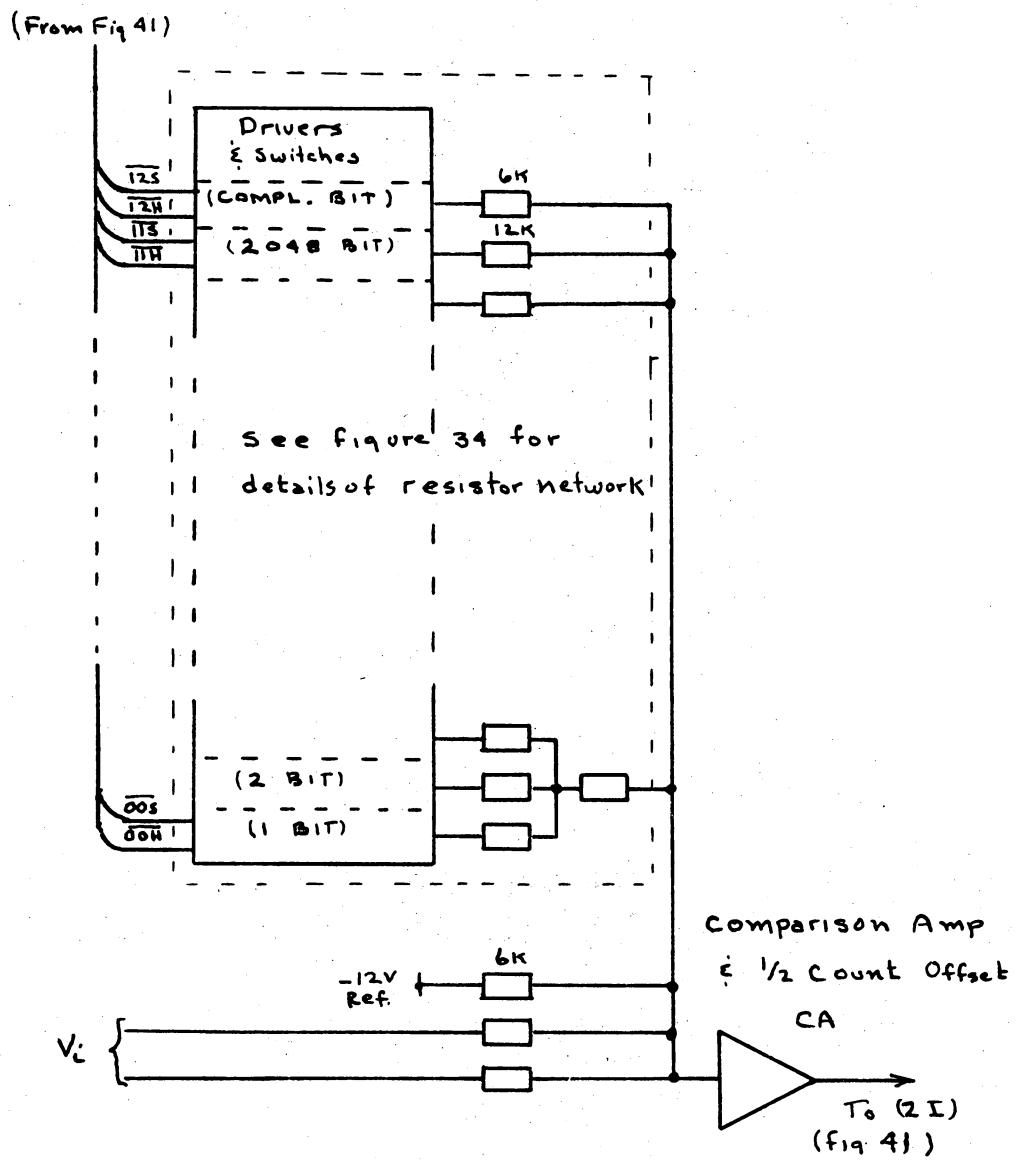


Figure 40. Analog Circuitry of the Converter

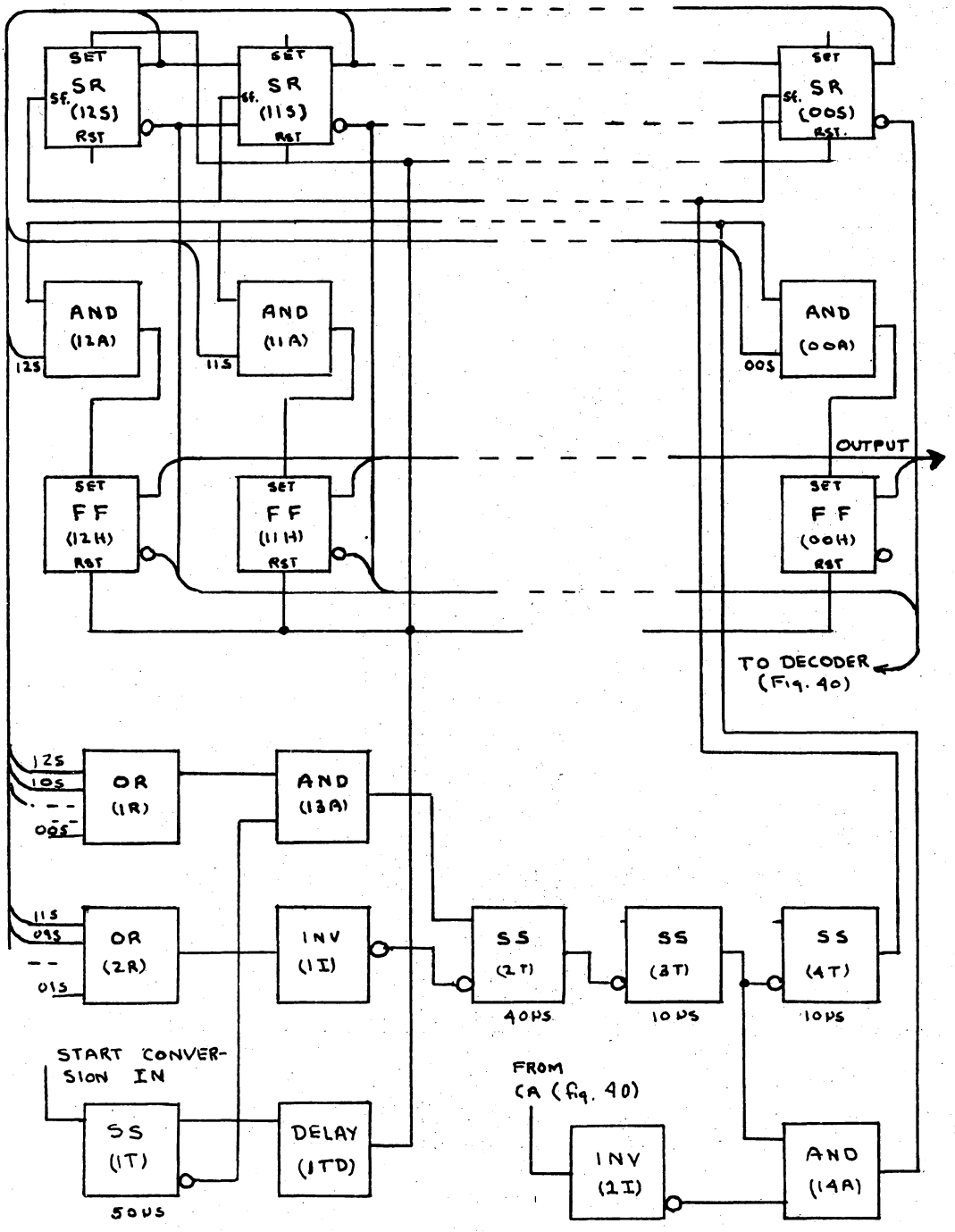


Figure 41. Converter Logic

4. A circle at an input indicates that the desired logic is performed for a "0" rather than a "1" input. A circle input is called an inverse input, a non-circle input is called a normal input.
5. A circle at an output indicates that the logic is true for "0" at the circle output. A circle output is called an inverse output, a non-circle output is called a normal output.
6. A "1" at a shift register or flip flop set terminal will cause the normal output of the unit to assume a "1" state. A "1" at the reset terminal will cause the normal output to assume a "0" state.

The logic of the complementing and decoding switches is such that the switch outputs a "1" current with "0" OR "0" at their two inputs. One input of the most significant switch (complementing switch) is connected to shift register bit 12S and the other input of this switch is connected to flip flop 12H. The inputs of the 2048 switch are connected to 11S and 11H, etc.

The 13 bit shift register of the logic is operated as a ring counter to cause trial operation of succeedingly lower order converter bits. If the comparison amplifier indicates that the total decoder and complementing signal, including signal from the trial bit, is less than the input signal, the flip flop corresponding to the trial bit is set and the decoder bit remains a "1" until a

new conversion is made.

The logic operates as outlined by the following steps:

1. The converter receives a "1" start conversion signal.
2. 1T outputs a normal and inverse fifty microsecond pulse. The inverse pulse causes 13A to have "0" out. 2TD delays the normal pulse for a few microseconds and then resets all flip flop and shift register bits except 12S. 12S is set by 1TD.
3. The pulse from 1T ceases.
4. The normal input of 2T goes to a "1" since 12S causes 1R to output a "1", and 13A thus outputs a "1" because 1R AND inverse 1T are "1"'s.
5. 2T outputs a forty microsecond pulse.
6. 3T outputs a ten microsecond pulse that follows the trailing edge of the pulse from 2T.
7. The ten microsecond pulse from 3T is "AND"ed with an inverted signal from the comparison amplifier, CA, at logic unit 14A. If CA indicates that the decoder signal is small, then the output of 14A becomes enabling to the 13 "AND" units that serve as gates to the set terminal of the 13 flip flops. The "AND" unit associated with 12H's set terminal will output a "1" since 12S outputs a one. 12H becomes set. If CA indicates that the decoder signal is large, 14A will inhibit the setting of 12H. Notice that

the comparison amplifier has had at least forty microseconds of settling time from the beginning of the pulse from 2T and ninety or so microseconds from the beginning of the conversion.

8. 4T outputs a ten microsecond pulse that follows the trailing edge of the pulse from 3T.

9. The "1" of 12S is shifted to 11S by the leading edge of the pulse from 4T.

10. The 2048 decoder bit outputs a "1" signal for trial purposes.

11. The output of 1R becomes "0" when 12S became 0. The output of 2R became "1" when 11S became 1.

12. The inverse input of 2T goes to "0" and 2T again outputs a forty microsecond pulse. The use of two inputs to 2T is required because the inputs to the single shot circuit are internally capacitively coupled to the monostable circuit of the unit.

13. The "1" in the shift register is now in a cyclic mode that continues until 00S has been made "1" and then finally left as a "0" by a shift pulse from 4T.

14. The normal outputs of 12H through 00H provide the output data of the converter. The state of 12H provides sign information for the data.

In summary, the logic provides ninety microseconds for the comparison amplifier to determine the polarity of the converter's input voltage and then it sequentially enables each succeedingly lower order decoder bit for forty microseconds. The comparison amplifier detects the difference between the converter's input signal and the decoder's signal during this time. If at the end of the forty microseconds, the comparison amplifier's output indicates that the input signal is in excess of the decoder's signal, the logic of the converter causes the enabled decoder bit to remain enabled for the remainder of the conversion. Table 8 illustrates the conversion procedure with a ten volt full scale converter that has -1.601 input volts. The digital equivalent of -1.601 volts is correctly shown to be -640 counts.

The logic of Figure 42 is symbolic only. The actual logic used in the converter was "NAND" type with special circuit provisions for shift register and single shot logic.

TABLE 8. CONVERTER OPERATION CHART

Trial Number	Input Signal (Counts)	Offset Signal (Counts)	Compl./ Decoder Signal (Counts)	Comparison Input (Counts)	"1" Bits
0	-640.4	-.5	-4096	-4736.9	
1	-640.4	-.5	0	- 640.9	C
2	-640.4	-.5	≠1024	≠ 383.6	C, 1024
3	-640.4	-.5	≠ 512	- 128.4	C, 512
4	-640.4	-.5	≠ 768	≠ 117.6	C, 512, 256
5	-640.4	-.5	≠ 640	- .9	C, 512, 128
6	-640.4	-.5	≠ 704	≠ 63.1	C, 512, 128, 64
7	-640.4	-.5	≠ 672	≠ 31.1	C, 512, 128, 32
8	-640.4	-.5	≠ 656	≠ 14.1	C, 512, 128, 16
9	-640.4	-.5	≠ 648	≠ 7.1	C, 512, 128, 8
10	-640.4	-.5	≠ 644	≠ 3.1	C, 512, 128, 4
11	-640.4	-.5	≠ 642	≠ 1.1	C, 512, 128, 2
12	-640.4	-.5	≠ 641	≠ .1	C, 512, 128, 1
13	-640.4	-.5	≠ 640	- .9	C, 512, 128

VIII RESULTS OF CIRCUIT AND CONVERTER EVALUATION

Introduction

It is generally desirable to verify extensive circuit analysis or synthesis with operating circuits.

The comparison amplifier, reference power supply, and decoder switch with driver were initially built in a breadboard fashion and evaluated. These circuits were then packaged on epoxy base, etched circuit boards and evaluated again. The effect of wire routing and lengths was of particular interest at that stage of development.

The comparison amplifier, reference supply and 13 switching bits were then assembled with digital logic to make a voltage-to-digital converter. The converter's performance was then evaluated.

The object of this section is to briefly present some of the results obtained during the circuit and converter evaluation. It is to be expected that the performance of the circuits will not usually approach the limits allowed by the specifications. In cases where several circuits are designed to contribute a small amount of a single conversion error or deviation, the instrumentation used in evaluating the circuits was marginal, but for overall performance measurements the instrumentation seemed satisfactory. Voltage measurements were made by comparing a divided reference voltage against the voltage quantity to be measured. The measuring equipment and its specified performance is listed below.

1) Voltage Reference

   a. Voltage: $\leq$ 50 volts

   b. Accuracy: $\leq$.005% absolute, long term

      $\leq$.002% absolute, short term

      $\leq$.002% relative

   c. Temperature coefficient: .0002%/°C

   d. Type: FVS 105

   e. Manufacturer: Julie Research, Inc.

2) Voltage Divider (Kelvin-Varley)

   a. Accuracy: $\leq$.001%; 15°C to 35°C

   b. Input resistance: 100,000 ohms $\leq$.01%

   c. Type: VDR 105

   d. Manufacturer: Julie Research, Inc.

3) Nine-series Resistors (to reduce range of VDR105)

   a. Initial relative accuracy compared to VDR105 input resistance: .0001%

   b. Ratio stability: .005%/year

   c. Temperature coefficient: .00025%/°C

   d. Manufacturer: Julie Research, Inc.

4) Null Detector

   a. Scales: 100×10^{-6}, 300×10^{-6}, 1×10^{-3} —— 10^{3} volts

   b. Input impedance: 10×10^{6} ohms on 100×10^{-6} V. scale

      30×10^{6} ohms on 300×10^{-6} V. scale

      100×10^{6} ohms on all other

c. Accuracy: ±1%

d. Isolation: battery operation

Decoder and Complementer

An initial switch and driver design did not have capacitors C1 and C2 (see figure 33), and instead, it had a 220 micro-microfarad capacitor around the 22,000 ohm resistor at the base of Q3, thus the initial circuit was appreciably faster than the final circuit. The faster circuit tended to short the switches reference busses when a saturated NPN switch condition was changed to a saturated PNP condition. The shorting action would seem to be caused by carrier storage in the NPN transistor. The NPN unit with the worst storage characteristic was selected from 100 available samples. A circuit was breadboarded as shown in Figure 33, and the capacitors C1 and C2 were selected to give safe non-shorting switching with the worst transistor in an 80°C ambient. Prior to adding C1 and C2, the switch current was as high as 40 milliamperes in the 80°C ambient. The time required for the switch to change from one output to another was measured and found to be about three microseconds when C1 and C2 were in the circuit, and the input rise or fall time was 0.3 microseconds and the measured switching time was measured from the beginning of the input pulse to the time that the output was five per cent away from its final value.

The effect of ambient temperature on driver input voltage to cause a one millivolt change in the switches output was measured and

found to be quite good. The output voltage transfer from a millivolt change to the opposite state in either direction was maintained within an input voltage band between 1.5 and 2.1 volts in an ambient that varied from 0°C to 70°C. This band was maintained for 13 circuits.

Most of the calculable switch and resistor performance as outlined in Section VI was verified by measurements.

An attempt was made to check the effect of ambient temperature on the ±12 volt reference supply. The measured deviation of the ±12 volt supply was found to be one-tenth of a millivolt for a 0° to 75°C ambient change on the unheated components of the supply. A similar measurement indicated two-tenths of a millivolt variation for the -12 volt supply. These deviations are smaller than could be reliably measured with the test equipment, but they are probably accurate within 50% or so.

The transient response of the supply was evaluated by applying step loads to the supply's output while varying C1 (see figure 36). For large values of C1, the supply is a second order system and the phase margin can be determined from tables that are available in many servomechanism textbooks. The phase margin for low values of C1 is of more interest but more difficult to analytically appraise or measure. The step response on the supplies output should cause transient voltage surges due to current changes in the output capacitors ESR, wire inductance, wire and connection resistance, etc.

A step 50 milliampere load was applied to the supply output by a mercury wetted relay's interlock. A five millivolt per centimeter oscilloscope with a ten megacycle bandpass and a 200 microvolt per centimeter oscilloscope with a 100 kilocycle bandpass were used to measure the step response of the supply. As near as could be determined with the available scopes, the output voltage jumped up one millivolt and decayed with an eight microsecond time constant when C1 was 220 micro-microfarads (final value of C1). Similar performance was obtained for both reference supplies with breadboard and final packaging. All four supplies were stable with C1 reduced to 22 micro-microfarads.

Comparison Amplifier

A well filtered, battery supply was used to measure the input voltage required for D.C. switching of the final packaged, comparison amplifier. This voltage was found to be about 20 microvolts ($\pm$10 microvolts) with the amplifier in a test rig and about 40 microvolts ($\pm$20 microvolts) at the converter's input when the comparison amplifier input was varied in an operating converter. The measured switching signal was about correct for overcoming noise that was measured in linear stages of the amplifier.

The dynamic switching time was found to be fairly consistent with that calculated in Section VI. Fifty microvolts of reverse input caused the two breadboard and the final packaged amplifier to

recover from twice the decoder's full scale output in 35 microseconds.

Voltage-to-Digital Converter

For the most part, the converter performed as expected; however, the evaluation was somewhat rushed because the converter was needed for a system prototype.

The converter was first operated with a much slower single-shot than those of Figure 41. This provided performance information essentially equivalent to D.C. operation except for self-heating errors. The converter's gain, offset, noise and linearity errors were in total better than .004% of full scale when the converter's reference supplies were adjusted against the measuring reference voltage and the quantization error was assumed to be one-half of a count. At rated speed, the total errors approached .01%. The worst conversion error occurred at 4095 counts of complemented output (a positive 1 count equivalent input).

The stability of the converter was quite good. The total deviation seemed to be less than .003% or so for a period of one week.

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A number of General Electric people contributed directly to the design of the converter discussed in the thesis. The author had the project of developing a similar converter with germanium semiconductors in 1961-1962. At that time, and did a large part of the circuit design work for the converter's decoder and comparison amplifier, and this work provided a valuable background for the silicon converter of this thesis. and are to be credited with much of the experimental evaluation of the converter's circuits and the components used in them while and are to be recognized for collecting the data on the NPN and PNP switch transistors of table 5.

Credit for the design of the logic elements, flip-flop, shift registers, etc., used in the digital portion of the converter is to be given to and of the General Electric Company.

The author would like to thank of the General Electric Company for circuit design advice given at various times and

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APPENDIX A. TRANSFER FUNCTION OF THE REFERENCE SUPPLY DIFFERENTIAL STAGE

The derivation of this appendix provides the small signal, low frequency, gain of the reference voltage supplies' differential input stage. Unless otherwise noted, all voltage, current, and β notations are small signal notations. Refer to figure A1:

if $V_{be1} << V'$ and $\beta_x = (h_{fe})_x$

$$i_{e1} \simeq \frac{V_{i1} - V'}{KR + r_{e1} + R_{s1}/(1+\beta_1)}$$

where: r_{e1} = emitter resistance of Q1 = K/I_{e1}

I_{e1} = d.c. emitter bias of Q1

$i'_{c1} = i_{e1} - i'_{b1} \simeq i_{e1}$ if $\beta_1 >> 1$

also: $i_{c3} \simeq i_{e3}$

Assuming that $R_x << r_{c1}/\beta_1$, where:

r_{c1} = collector resistance of Q1

$$\frac{i_{c3}}{i_{c1}} \simeq \frac{\beta_3 R_L}{R_x + \beta_3 R_L} \times \frac{r_{c3}/\beta_3}{R_L + r_{c3}/\beta_3}$$

and if $\beta_3 >> 1$

$$\frac{i_{c3}}{i_{c1}} \simeq \frac{r_{c3}/\beta_3}{R_L + r_{c3}/\beta_3}$$

$$i_o = i_{c3} - i_{c2}$$

$$i_{c2} = \frac{i_{e2} \times r_{c2}/\beta_2}{R_L + r_{c2}/\beta_2}$$

$$i_{e2} = \frac{V_{i2} - V'}{(1-K)R + r_{e2} + R_{s2}/(1+\beta_2)}$$

$$i_o \simeq \frac{r_{c3}/\beta_3}{R_L + r_{c3}/\beta_3}\left[\frac{V_{i1} - V'}{KR + r_{e1} + R_{s1}/\beta_1}\right] - \frac{r_{c2}/\beta_2}{R_L + r_{c2}/\beta_2}\left[\frac{V_{i2} - V'}{(1-K)R + r_{e2} + R_{s2}/\beta_2}\right]$$

The assumptions made thus far are reasonably valid for the circuit of figure 36. Further:

$R_{s1} = R_{s2} = R_s$

$V_{i1} = 0$ (or $V_{i1} = 0$ because of stable reference)

$r_{e1} \simeq r_{e2} \simeq 25/.5 = 50\Omega$ (assume maximum)

and given: $\beta = \beta_1 \simeq \beta_2 \simeq 40$ minimum

It should not cause too much error to assume that K = (1-K), and that $r_{c3}/\beta_3 \gg R_L$ and $r_{c2}/\beta_2 \gg R_L$, then:

$$i_o \simeq \frac{-V_{i2}}{R/2 + 50 + R_s/\beta}$$

For the positive 12 volt supply:

$$\frac{i_o}{V_{i2}} \simeq \frac{-1}{50 + 50 + 25} \simeq \frac{-1}{125} \text{ amp/volt (minimum } \beta \text{ calculation)}$$

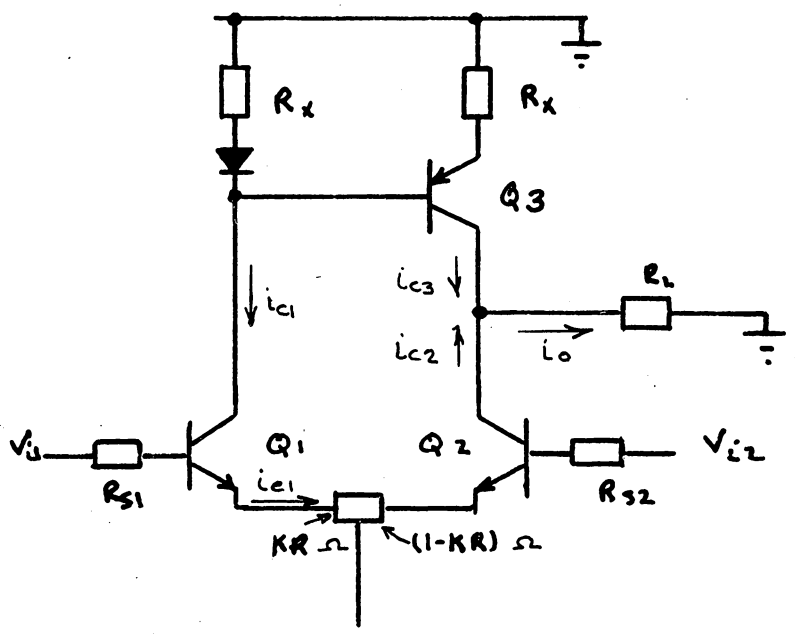

Figure A1. Differential Amplifier with Single-Ended Output

APPENDIX B. TRANSFER FUNCTION OF THE REFERENCE SUPPLY OUTOUT FILTER

This appendix derives the transfer function of the reference supplies' output filter. The filter is shown in figure B1. Resistor, R, is the open loop output resistance of the supply and R_c is the internal ESR of capacitor C. Capacitor C is recognizable in figure 36 as a 4000 microfarad capacitor. From the circuit of figure B1:

$$V_o = R \times i_c \times \frac{R_c + 1/pC}{R + R_c + 1/pC}$$

$$\frac{V_o}{i_c} = \frac{R(1 + R_c Cp)}{[1 + (R + R_c)Cp]}$$

R_c of a typical capacitor is about .03 ohm. Given that the regulator and bridge circuits of the supplies take about .02 amperes each, the no load R of the supply can be found:

$$R = 12 \text{ volts} / \left(\frac{38 \text{ volts}}{350 \text{ ohms}} - .02 \text{ amp.}\right)$$

$$= 136 \text{ ohm}, \text{ and}$$

$$\frac{V_o}{i_i} = \frac{136\,(1 + 120 \times 10^{-6} p)}{(1 + .54p)} \frac{\text{volts}}{\text{AMP}}$$

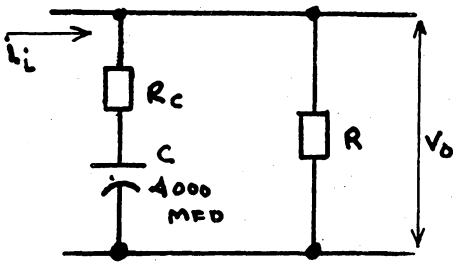

Figure B1. Output Circuit of Reference Power Supply

APPENDIX C. COMPARISON AMPLIFIER GAIN

The small signal, low frequency gain of the comparison amplifier is derived in this appendix. Equations 1 through 15 are used in the derivation of the circuit gain through the first six transisrors with feedback to the emitters of the differential transistors. The remainder of the amplifier's gain is derived thereafter. Unless otherwise noted, all voltage, current and β notations are small signal notations. A simplified small signal circuit for the circuit with the amplifier's first six transistors is given in figure C1.

Given: $\beta_x = (h_{fe})_x$

$\beta_2 \gg 1 \quad \therefore \quad R_2 = r_{e2} + \text{ext. emit. R}$

$$i'_{c2} \simeq \frac{e_{c2} - V''}{R_2} \qquad (1)$$

$$i'_{c2} \simeq \alpha_2 i'_{a2} \simeq i'_{e2} \qquad (2)$$

Assume: $R_{L2} << \frac{r_{c2}}{\beta_2}$ (r_{c2} = collector resistance of Q2)

$$e_{o2} \simeq i'_{c2} \times \frac{1}{1/R_{L2} + \frac{1}{\beta_3 \frac{R_{L3} R_{F3}}{R_{L3} + R_{F3}}}}$$

For the circuit of figure 39:

$$e_{o2} \simeq i'_{c2} R_{L2} \qquad (3) \text{ and from 1}$$

$$e_{o2} \simeq \left(\frac{e_{c2} - V''}{R_2}\right) R_{L2} \simeq e_{o3} \qquad (4)$$

$$e_{i2} \simeq i_{c1} \frac{R_{L1} \times r_{i2}}{R_{L1} + r_{i2}} = i_{c1} R_L$$

where r_{i2} = resistance into base of Q2

From (4)

$$e_{o3} = (\beta_1 i_{b1} P R_{L1} - V'') \frac{R_{L2}}{R_2}$$

$$i_{b1} = \frac{(e_{o3} R_2 + V'' R_{L2})}{\beta_1 i_{b1} R_L} \qquad (5)$$

$$i'_1 = (\beta_1 + 1) i_{b1} + i_f \simeq \beta_1 i_{b1} + \frac{e_{o3}}{R_{F3}} \qquad (6)$$

and: $$i_{b1} \simeq \frac{e_{i1} - [V' + i_1 KR + \beta_1 i_{b1} r_{e1}]}{R_{s1}} \qquad (7)$$

KR = pot. resistance from slider to Q1

r_{e1} = emitter resistance of Q1

$$i'_{b1} = \frac{e_{i1} - V' - i_1 KR}{R_s + \beta_1 r_{e1}} \qquad (8)$$

From (6) & (8)

$$i'_{b1} (R_s + \beta_1 r_{e1} + \beta_1 KR) + \frac{e_{o3} KR}{R_{F3}} = e_{i1} - V' \qquad (9)$$

combining (5) & (9)

$$\frac{e_{o3} R_2 + V'' R_{L2}}{\beta_1 R_L R_{L2}} (R_{s1} + \beta_1 r_{e1} + \beta_1 KR) + \frac{e_{o3} KR}{R_{F3}} =$$

$$e_{i1} - V'$$

Assuming that primed and unprimed circuit components are identical and operating 180° out of phase:

and $K = .5$ & $(1-K) = .5$

$e'_{o3} = |-e_{o3}|$ & $e_o = e_{o3} - e'_{o3}$, then

$$\frac{e_o R_2}{\beta_1 R_L R_{L2}} \left(R_{S1} + \beta_1 r_{e1} + \beta_1 KR \right) + \frac{e_o KR}{R_{F3}} \simeq e_{i1} \quad (11)$$

$$\frac{e_o}{e_i} \simeq \frac{R_{F3}}{KR} \frac{1}{1 + \frac{R_{F3}}{KR} \frac{\left(R_S + \beta_1 r_{e1} + \beta_1 KR \right) R_2}{\beta_1 R_L R_{L2}}} \quad (12)$$

For the circuit of figure 39:

$R_L \simeq 9 R_{L1}$, $r_{e1} \simeq 150\,\Omega$

$\beta_1 \simeq 150$ minimum at 80°C

$R_{S1} \simeq 1400\,\Omega$, other values as shown

$$\frac{e_o}{e_i} = \frac{12{,}000}{100} \wedge \frac{1}{1 + 120\left[\frac{1400 + 150(150+100)}{19 \times 150 \times 22{,}000 \times 10{,}000}\right]^{1000}}$$

$$= \frac{120}{1 + .154} = 104 \text{ min.} \quad (13)$$
$$\pm \text{res. tol. errors}$$

If $R_f = \infty\,\Omega$

$$\left(\frac{e_o}{e_i}\right)_{\substack{\text{open} \\ \text{loop}}} \simeq \frac{\beta_1 R_{L1} R_{L2}}{\left(R_S + \beta_1 r_{e1} + \beta_1 KR\right) R_2} \simeq \frac{120}{.154} \simeq 780 \quad (15)$$

Refer to figure 39 for the circuit and nomenclature of the gain derivation of the remaining stages of the amplifier.

Given: $\beta_{4A} >> 1$ $\beta_{4A} \simeq \beta_{4B}$

$$R_{49} << \frac{r_{c4A}}{\beta_{4A}} >> R_{50}$$

$r'_{e4A} \simeq r_{e4B} \simeq 27/.75 = 36\,\Omega$

$V_{i4A} \simeq -V_{i4B}$

$$i_{c4A} \simeq \frac{V_{c4A}}{274+3G} \simeq -i_{c4B}$$

And for Q5, Q5', Q6 & Q7, assume that

$$\beta \gg 1 \quad \& \quad R_L \ll r_c/\beta$$

$$i_{cs} \simeq \beta_5 i_{b5} \simeq \frac{\beta_5 \times 4750}{4750 + \beta_5 r_{e5}} \times i_{c4A}$$

Given $\beta_5 = 100$ minimum

$$i_{cs} \simeq \frac{V_{c4A}}{310} \times \frac{4750}{47.5+26} = .208\, V_{c4A}$$

$i_{cs} \simeq -i_{cs'}$ (somewhat erroneous)

Given: $\beta_6 = 50$ min., $\beta_7 = 70$ min.

Use superposition to calculate $(i_{c6})'$ due to i_{cs} and $(i_{c6})''$ due to $i_{cs'}$:

$$i_{c6} = (i_{c6})' + (i_{c6})''$$

$$(i_{c6})' \simeq i_{cs} \times \frac{\beta_6 \times 2200}{3300 + \beta_6 \times 2200} \simeq \frac{i_{cs} \times 2200}{2265}$$

$$(i_{c6})'' \simeq \frac{\beta_6}{1+\beta_6} i_{cs'} = .98\, i_{cs'}$$

$$i_{c6} \simeq 1.95\, i_{cs} \simeq .405\, V_{c4A}$$

and

$$i_{c7} \simeq \frac{\beta_7 \times 47{,}000 \times i_{c6}}{47000 + \beta_7 \times r_{e7}}$$

Given that: $R_{L7} = 20K$ in parallel with $7.5K$

$$r_{e7} = 13\ \Omega$$

$i_{c7} \simeq 59\, i_{cc} = 2.9 V_{ia}$

$V_{out} \simeq 24 \times V_{i4a} \times 5600 = 134{,}000$

$V_{i4a} \simeq 52 \times V_i$ (from eq. 13)

where V_i = input to Q1A

$\left(\frac{V_{out}}{V_i}\right)_{cA} \simeq 7 \times 10^6$ volts/volt with min. β & nominal R_o

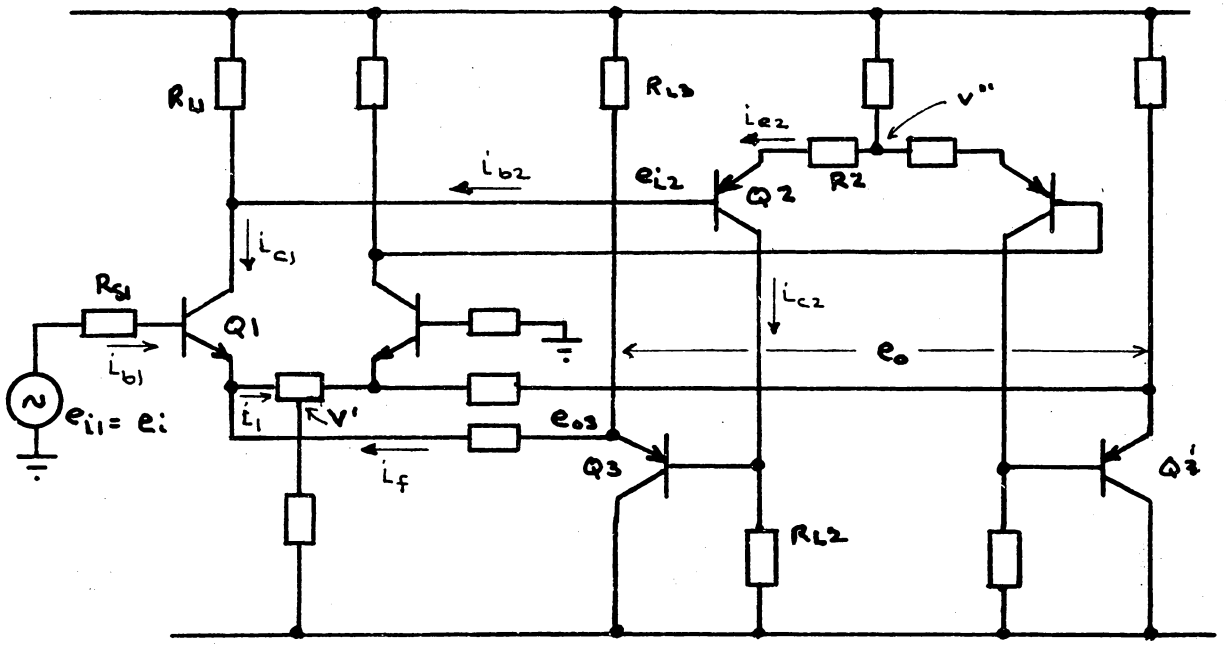

Figure C1. Low Level Amplification of Comparison Amplifier

ABSTRACT

This thesis treats broad aspects of voltage-to-digital converter design. Particular emphasis is placed on material related to designing a converter to satisfy a set of converter specifications that is given in the introduction of the thesis.

The converter design is first considered in terms of basic conversion techniques. One technique, known as "successive approximation," seems best to satisfy the requirements of the design specifications. The "successive-approximation" voltage-to-digital converter requires that its input voltage be compared to a voltage that is systematically generated within the converter. The voltage generated within the converter is derived from digital information. When the internal voltage equals the external applied voltage, a conversion is accomplished and the converter can output its digital information as the numerical equivalent of its input voltage. A major part of the thesis is concerned with basic approaches that might be used in generating a voltage from digital information in a manner that is fast, accurate, stable, and compatible with a fast, accurate, stable comparison operation. Another major part of the thesis presents analysis of specific circuits that are used in the construction of a converter designed to satisfy the introduction's specifications. A report on the performance of a converter built with the just mentioned circuits is included.