A CAPABILITY FOR CONTINUOUS TOPOLOGY TRANSIENT ANALYSIS IN SCR SWITCHING-MODE POWER SUPPLIES

by

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INTRODUCTION

Dissertation Topic

Application of computer aided design and analyses, CADA, to high power processing electronics is limited by the absence of an adequate computer model for the silicon controlled rectifier, SCR.

This dissertation explores and develops an electronic network analog for the SCR and a means of determining parameters for that analog so as to provide a continuous topology non-linear computer model for the SCR.

The SCR model developed is a general purpose high-power SCR model which may be tailored through its parameters to simulate a specifically designated device and which may be applied to CADA using a variety of advanced network analysis programs such as SPICE2[4] and SCEPTRE[6].

Background

In recent years, the field of power processing electronics has emerged as a new and rapidly growing member of the electrical engineering family of disciplines.

Electrical power, the driving force of our modern society, is seldom found in its origination or at its point of access in a form acceptable to usage by the myriad of semi-conductor electronic

devices which dominate the application of this power to productive roles in society.

The power processor thus emerges as the means of shaping and filtering the raw power of the generating source to conditions of palatability by the utilizing load.

Switching mode power processors, a family of power processors which inject measured pulses of raw power into a filtering and processing network which then adapts this power to the needs of the load, have come to dominate the field of power processing. This is because the last two decades have seen the development of semiconductor switching devices to serve as a high speed and highly reliable means of implementing this technology. Thus one arrives at the nomenclature "power processing electronics" or "power electronics". These terms connotate the design and analysis of the power switching circuits and filters through which the bulk power flows and also, the design and analysis of the feedback and control networks needed to make the power stage responsive to changing conditions of load and/or source.

Given a strong steady power source and a fixed load, the problem of design of such circuits is not enormously difficult and may be handled by a skilled engineer using the intuitive approach.

Such is not the case, however, in the presence of a highly dynamic source or load. Power processors to meet these applications are analytically described by non-linear time varying

expressions which make their utilization in design a highly advanced engineering task. This complexity of the design task coupled with the surging demand for production of wide range rapid response power processors has placed the task of developing more useful design techniques in the forefront of engineering research and development.

At the present time, three major analysis techniques are emerging as the primary design tools of switching mode power regulators. They are the state space averaging technique, the discrete multiple topology approach, and the continuous topology approach. The first of these is a closed form manual analysis technique while the latter two are both computer analysis techniques.

The state space averaging technique is a method of obtaining an equivalent linear system to the non-linear system. The approach is to treat the power switch as ideal, either open or closed, and to examine each of the discrete topologies resulting as the system switches are varied through all 2^n possible positions. The state variables associated with each topology are then time averaged in proportion to the fraction of each complete switching cycle for which the topology exists. The analyst then examines the behavior of the "averaged state" of the system in response to perturbation of the system. It's usage is limited to system dynamics which occur at a low frequency with respect to switching frequency. Its major advantage is that being a

frequency domain technique, slow transient behavior of the system may be analyzed from closed form "s" domain expressions.

The discrete multiple topology approach is a piecewise linear system analysis technique. Again the switch is treated as ideal, thus, each discrete topology resulting from switch alteration is a linear network with initial conditions determined by the final state of the previous topology. Computer analysis is used to compute the system's state transition during each topological configuration. The technique is currently the most widely used CADA method in power processing electronics. With advanced CADA programs, it may be used with preassigned switching time or internally sensed switching conditions. Its primary limitations are that it assumes switching device time constants are very short with respect to system time constants, it assumes the switch responds properly to the control signal under any circuit conditions, and it is cumbersome to use to analyze transients requiring more than a few cycles of the power switch to settle. In this latter respect it is somewhat complementary to the state space averaging technique.

The continuous topology approach to power processing electronics analysis is an extension of the discrete multiple topology approach in which the switch is treated as a non-linear circuit element which alternates states through a finite but non-zero interval along a well-defined path thus eliminating discontinuous changes in system topology. This technique of analysis has the limitations that it also is cumbersome for transient analysis beyond a few switching

cycles, it requires an advanced non-linear network analysis host program with a variable time step numerical integration routine, and at this time it is faced with a lack of accurate non-linear switch models for proper switch characterization.

What then are the reasons for pursuing continuous topology analysis of power processing electronics? The answer is straightforward. It is the ideal complement of the state space averaging technique. State space averaging allows one to address system transients occurring slowly with respect to the switching period dealing only with slow variations about an averaged steady state. On the other hand continuous topology analysis is specifically to address system transients occurring rapidly with respect to switching period in a possibly non-steady state condition. It is very useful in the analysis of systems where transient behavior occurs so slowly (or so rapidly) as to improperly inhibit (or initiate) desired switching behavior as determined by the switch control signal.

In the past decade researchers have made steady progress in developing the tools of continuous topology switching circuit analysis. Powerful non-linear circuit analysis programs such as SPICE2 and SCEPTRE have lowered the computational barriers by developing automatic system equation formulation for non-linear network descriptions. Additionally the numerical methods of these programs use variable time step algorithms to select time steps conditional to system dynamics. As opposed to fixed time step algorithms which

limit time steps to less than the shortest system time constant, variable time step algorithms allow long time steps during periods of relatively static behavior, but adjust to shorter time steps during periods of highly dynamic behavior such as switching. Improved solution accuracy is obtained during long transients by means of implicit quadrature algorithms.

Declining cost and miniaturization of computing systems has brought wide spread industry acceptance of CADA. This growing availability of economical CADA has spurred the demand for power semi-conductor models to facilitate continuous topology analysis.

Modelers having the advanced skills and theoretical knowledge to tackle the modeling task have done much to facilitate the need for low power semi-conductor models. Bipolar junction transistor and FET models are in advanced stages of development.

In the high power semi-conductor model area, a gulf remains however. The high power electronic power processing area is dominated by SCR technology. Previous attempts to produce an adequate high power SCR model have fallen short of the mark.

The requirements of a good computer model for the SCR are that it accurately represent important terminal characteristics of the device, it must be computationally efficient, and it must be easy to use by modelers not possessing advanced theoretical and numerical skills.

This point concludes the background summary and arrives again to the topic of this dissertation which is summarized in the following objective statements.

Objective

It is the general objective of the research presented in this dissertation to provide a valuable analytical tool to the high power processing electronics industries of motor controls, pulse power, uninterruptible power supplies, industrial welding and many others which are dominated by SCR technology. More specifically, the objective is to advance the capabilities of CADA in the area of continuous topology analysis of switching power processors by developing a circuit anolog and method of parameter estimation for a computer model of the SCR.

The desired characteristics of the computer model of the SCR are:

- It should be completely general purpose with respect to providing the ability to simulate any high power SCR device of either amplifying gate or non-amplifying gate construction.
- It should be applicable to both phase control and inverter types of SCRs.
- It should provide accurate simulation of important SCR terminal characteristics with special emphasis on turn-on, dV/dt, and commutation.
- It should have an easy to use analytical parameter estimation procedure oriented to a readily available data base such as manufacturer's specification sheet data.

- It should have a circuit anolog composed of a minimum number of circuit elements. The PNPN structure should be easily recognizable in the circuit anolog and elements should clearly suggest the physical properties they represent. Fulfillment of this objective will not only facilitate ease of understanding of the models functioning, but will also provide maximum flexibility for future improvement or adaptation to alternate semi-conductor technology such as Triacs, GTOs, and RCTs.
- It should be computationally efficient and applicable to use with any of the currently-in-use advanced circuit analysis CADA programs such as SPICE2 and SCEPTRE.

Method of Study

The material presented in this report is a sequential documentation of the search for a computer model for the SCR suitable to fulfill the above stated objectives.

The thesis is organized into nine chapters each one successively dependent on those preceding for clarity of material presented.

As preliminary work, a comprehensive search to establish the state of development in SCR computer modeling revealed that two SCR models stood significantly in advance of all other efforts [1,2,3,8,12,36]. They were an SCR modeling technique specifically

for use with SPICE2[4] developed by C. Hu[12] at the University of California, Berkeley and an SCR model developed specifically for use with SCEPTRE[6] by H. Nienhus[8] at the University of South Florida. As is summarized in detail in Chapter 8, both models fell somewhat short of satisfying the list of previously stated objectives, making it apparent that extended developmental work would be required.

The model by Hu appeared to be the more advanced effort. It claimed a generalized analytical parameter estimation procedure and a circuit analog based on the two-transistor representation of the SCR. The two-transistor anolog being the most widely accepted vehicle of explaining the regenerative nature of SCR turn-on and dV/dt behavior[1,11,14,22,29,31,32], it represents a logical starting point in the investigation to determine the best general purpose circuit anolog for computer applications.

Noting that the two most advanced SCR models were developed for specific application, one to SPICE2 and the other to SCEPTRE, then these two advanced CADA programs are also the natural choices to provide a vehicle of test and verification of a more general purpose model uniformly applicable to both programs as well as to other advanced CADA programs for electronic circuit analysis[5]. Additionally these two programs are the most popular advanced circuit analysis programs in use today[28]. Together they represent the most complete non-linear systems analysis capability available to CADA at this time.

Chapter 1 provides a general introduction of the formulation of network analogs to the bipolar junction transistor, BJT, as required to meet programming techniques applicable to SPICE2 and SCEPTRE. The BJT model applicable SPICE2 is then illustratively configured into the 2-BJT analog for the SCR suitable for use with SPICE2. From the appropriate model equations, the parameters for which values must be determined are extracted.

Chapter 2 examines the SCR model for SPICE2 developed by Hu[12], denoted the "Hu-ki Model". Inaccuracies in the model are analyzed and improvements implemented to result in the "Modified Hu-ki Model".

Chapter 3 provides SPICE2 demonstration of the "Modified Hu-ki Model" through simulation of a basic SCR resonant charging circuit. Performance of the model is observed with and without snubber.

Chapter 4 presents a SPICE2 study of circuit simulations of basic SCR circuit building blocks having two SCRs in the unit block. The study demonstrates the capability of the "Modified Hu-ki Model" of the SCR to allow SPICE2 simulation of troublesome device interaction typical of SCR circuits.

Chapter 5 treats the evolution of the "Modified Hu-ki Model", a two-transistor circuit anolog for SPICE2, into a three junction (i.e. three diode) circuit analog best suitable to SCEPTRE programming constraints. The resulting "3-Junction SCR Model" for application to SCEPTRE is in form similar to Nienhus' model[8] while having

a parameter estimation procedure derived from that developed by Hu[12]. This sets the stage for development of a unified modeling procedure applicable to both CADA programs.

Chapters 6 and 7 demonstrate the "3-Junction SCR Model" through SCEPTRE simulation of AC and DC resonant charging circuits for pulse power applications.

Chapter 8 presents the central topic of this dissertation. Drawing from the experiences documented in Chapters 1 through 7, the J^3 SCR model, a unified SCR modeling procedure designed to be uniformly applicable to either SPICE2 or SCEPTRE as well as fulfilling the stated objectives of this dissertation is developed. The chapter presents the model's circuit analog, derivation of the parameter estimation procedure, and verification testing of the model's ability to simulate important SCR characteristics.

Chapter 9 concludes this dissertation with a demonstration of the application of the J^3 SCR model to simulation of a series resonant inverter circuit. This simulation demonstrates the fulfillment of the dissertation statement by providing a capability for continuous topology transient analysis of switched mode power processors in which device properties influence the performance characteristics of the entire circuit.

CHAPTER 1

TWO-TRANSISTOR SCR MODELS FOR SPICE2 AND SCEPTRE

The advanced CAD programs, SPICE2 and SCEPTRE, each have available transistor models based on the well known Ebers-Moll equations[1][6]. Since the two programs use different equation formulation techniques, their respective transistor models have been configured differently to meet formulation requirements. When constructing a two-transistor model of the SCR, this naturally leads to different network representations of the SCR model for each program. A discussion of this process follows; however, thorough treatment of the SCR model implementation in SCEPTRE is reserved until Chapter 5.

1.1 The Bipolar Junction Transistor Model

Development of the SCR models begins with the large signal bipolar junction transistor model. This BJT model is a variation of the Ebers-Moll one dimensional model (Fig. 1.1) in which junction capacitances are added to account for charge storage in the depletion regions and diffusion capacitances are added to account for charge storage in the neutral regions due to diffusion time across the regions.

The equations describing the components in the Fig. 1.1 model are:

$$C_{BC} = \frac{\tau_R \alpha_R I_{CS}}{\theta} e^{V_{BC}/\theta} + C_{jCo}\left(\frac{1}{\sqrt{1 - V_{BC}/\phi_C}}\right) \tag{1.1}$$

$$C_{BE} = \frac{\tau_F \alpha_F I_{ES}}{\theta} e^{V_{BE}/\theta} + C_{jEo}\left(\frac{1}{\sqrt{1 - V_{BE}/\phi_E}}\right) \tag{1.2}$$

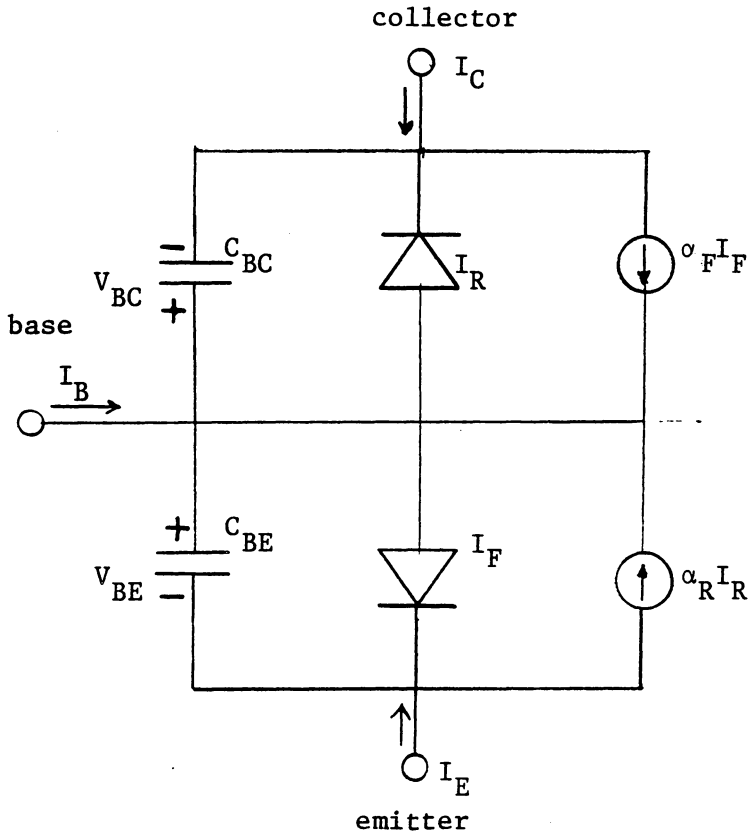


Fig. 1.1. MODIFIED EBERS-MOLL BIPOLAR JUNCTION TRANSISTOR MODEL (INJECTION MODEL)

$$I_C = \alpha_F I_F - I_R \tag{1.3}$$
$$= \alpha_F I_{ES}(e^{V_{BE}/\theta} - 1) - I_{CS}(e^{V_{BE}/\theta} - 1)$$

$$I_E = \alpha_R I_R - I_F \tag{1.4}$$
$$= \alpha_R I_{CS}(e^{V_{BC}/\theta} - 1) - I_{ES}(e^{V_{BE}/\theta} - 1)$$

List of Parameters

α_F = proportion of current injected from emitter into the base that diffuses to the base-collector junction.

τ_F = transit time for carriers injected by the emitter into the base to diffuse to the base-collector depletion layer boundary.

I_{ES} = base-emitter saturation current for reverse biased base-emitter junction.

C_{jEo} = zero bias base-emitter depletion layer capacitance.

θ = physical constant (at a fixed temperature) = .0259 v @ 300°K.

ϕ_E = emitter junction potential (.6 - .8 v) - a physical property.

α_R = proportion of current injected from the collector into the base that diffuses to the base-emitter junction.

τ_R = transit time for carriers injected by the collector into the base to reach the base-emitter depletion layer boundary.

I_{CS} = base collector saturation current for reverse biased base-collector junction.

C_{jCo} = zero bias base-collector depletion layer capacitance.

ϕ_C = collector junction potential (.6v to .8v) - a physical property.

m = the junction capacitance gradient factor. For heavily doped semiconductors $m \simeq .5$. For lightly doped semiconductors $m \simeq .33$.

The modified Ebers-Moll model as given is the basic model as applied to SCEPTRE. It is referred to as the injection model, because the reference currents I_R and I_F are the currents injected into the base region from the collector and emitter respectively.

SPICE2 incorporates a mathematically identical model, but, the SPICE2 MODEL is referenced to the proportion of the injected currents (I_R, I_F) which actually arrive at their respective collecting junctions ($\alpha_R I_R \longrightarrow$ called I_{EC}, $\alpha_F I_F \longrightarrow$ called I_{CC}). For this reason, it is referred to as the charge transport model (meaning that the reference currents are those actually transported across the base region).

Utilizing the reciprocity relationship:

$$\alpha_F I_{ES} = \alpha_R I_{CS} \triangleq I_S \tag{1.5}$$

The BJT model equations are then rewritten utilizing this relationship

$$I_C = I_S(e^{V_{BE}/\theta} - 1) - \frac{I_S}{\alpha_R}(e^{V_{BC}/\theta} - 1) \tag{1.6}$$

$$= I_{CC} - I_{EC}/\alpha_R$$

$$I_E = I_S(e^{V_{BC}/\theta} - 1) - \frac{I_S}{\alpha_F}(e^{V_{BE}/\theta} - 1) \tag{1.7}$$

$$= I_{EC} - I_{CC}/\alpha_F$$

$$C_{BC} = \frac{\tau_R I_S}{\theta} e^{V_{BC}/\theta} + C_{jc_o} \left[1 - V_{BC}/\phi_C\right]^{-m} \tag{1.8}$$

$$C_{BE} = \frac{\tau_F I_S}{\theta} e^{V_{BE}/\theta} + C_{jE_o} \left[1 - V_{BE}/\phi_E\right]^{-m} \tag{1.9}$$

This modification is advantageous in that one less parameter determination is required and that numerical methods are simplified due to an increase in the range of linearity of logarithmic calculations based on the reference current I_S [10].

Note. There is no physical or mathematical modification, only a notation modification.

Still further modification in form is made for the SPICE2 model while keeping the model mathematically identical. The two reference currents (current collected at the emitter I_{EC} and current collected at the collector I_{CC}) are combined to form a single reference current (current collected total I_{CT}). This I_{CT} is defined by

$$I_{CT} = I_{CC} - I_{EC} = I_S(e^{V_{BE}/\theta} - e^{V_{BC}/\theta}) \tag{1.10}$$

The combining of the transport current into a single term requires that the diodes have only base connections at their anode points (NPN model) and therefore an expression for base current must be formed so that the diode currents may be expressed correctly. Referring to Fig. 1.2.

$$I_B = -I_C - I_E \tag{1.11}$$

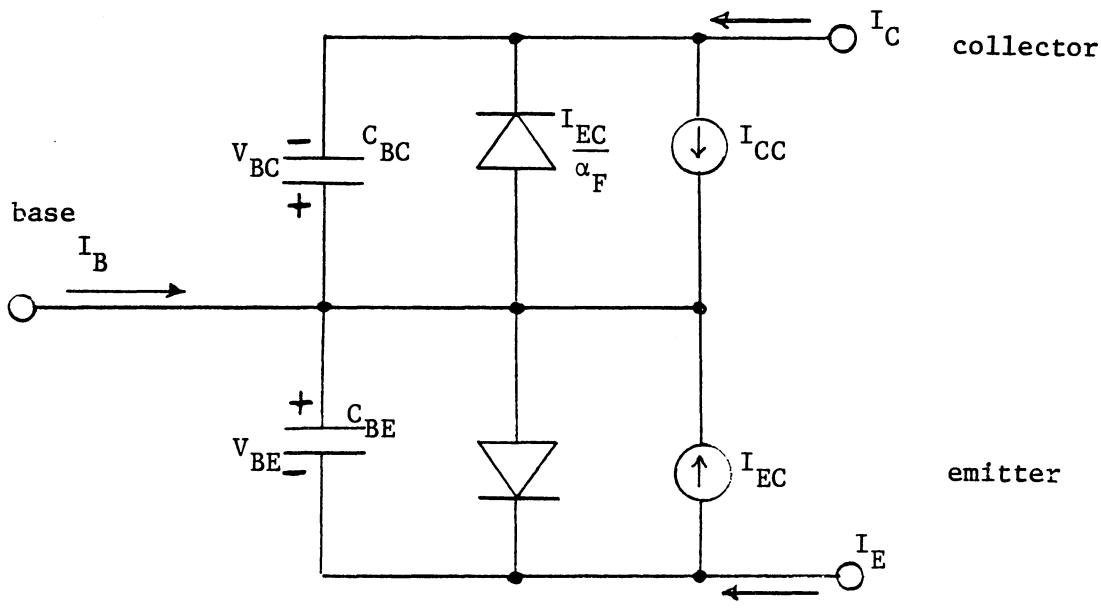


Fig. 1.2. MODIFIED EBERS-MOLL BJT MODEL (TRANSPORT MODEL)

$$I_B = (\frac{1}{\alpha_F} - 1)\ I_{CC} + (\frac{1}{\alpha_R} - 1)\ I_{EC} \tag{1.12}$$

$$I_B = \frac{I_{CC}}{\beta_F} + \frac{I_{EC}}{\beta_R} \tag{1.13}$$

The model now appears as Fig. 1.3.

The model terminal equations are now

$$I_C = I_{CT} - \frac{I_{EC}}{\beta_R} \tag{1.14}$$

$$= I_S(e^{V_{BE}/\theta} - e^{V_{BC}/\theta}) - \frac{I_S}{\beta_R}(e^{V_{BC}/\theta} - 1)$$

$$I_E = -I_{CT} - \frac{I_{CC}}{\beta_F} \tag{1.15}$$

$$= I_S(e^{V_{BC}/\theta} - e^{V_{BC}/\theta}) - \frac{I_S}{\beta_F}(e^{V_{BE}/\theta} - 1)$$

$$I_B = \frac{I_{CC}}{\beta_F} + \frac{I_{EC}}{\beta_R} \tag{1.16}$$

$$= \frac{I_S}{\beta_F}(e^{V_{BE}/\theta} - 1) + \frac{I_S}{\beta_R}(e^{V_{BC}/\theta} - 1)$$

The terminal characteristic model used in SPICE2 is then given in terms of I_B and I_C. This model is shown in Fig. 1.4, with contact resistances r_b, r_c, and r_e added.

1.2 The SCR Model in SPICE2

The SCR model is developed in SPICE2 by connecting TWO BJT models (a PNP and a NPN) as shown in Fig. 1.5. In addition to the two

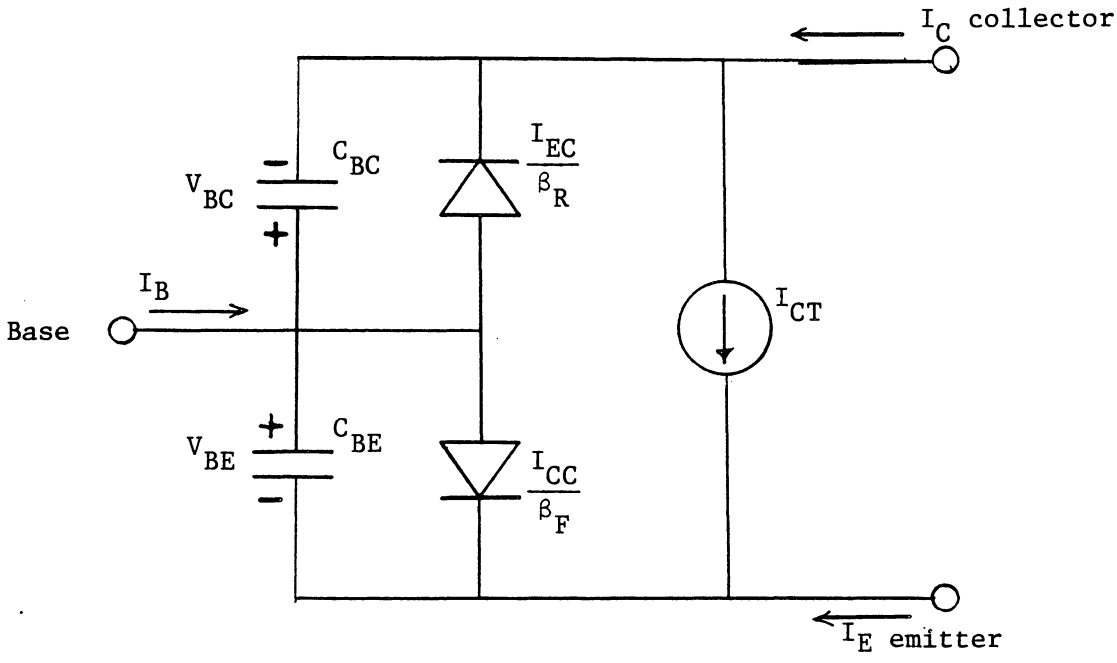


Fig. 1.3. MODIFIED EBERS-MOLL BJT MODEL

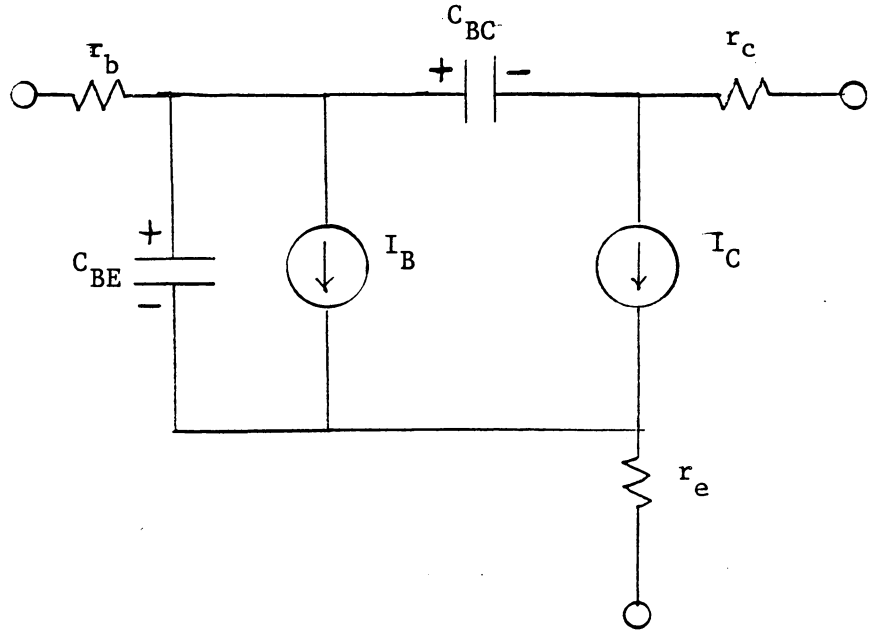


Fig. 1.4. SPICE2 MODIFIED EBERS-MOLL BJT MODEL (TERMINAL CURRENTS MODEL)

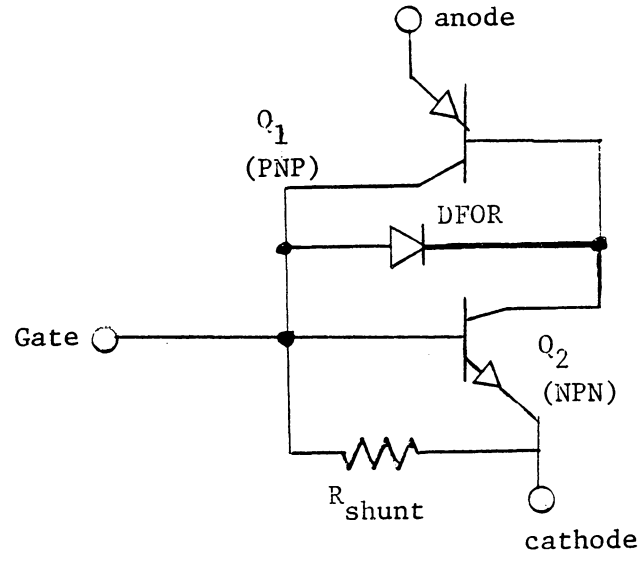


Fig. 1.5. A SPICE2 SCR MODEL BASED ON THE TWO BJT MODEL

transistors, a resistor R_{shunt} is added to the model. Since the SPICE2 BJT model has no capability to simulate the reverse breakdown of the p-n junctions, then a diode DFOR must be added to simulate the forward breakover voltage of the SCR[1].

When using the SPICE2 BJT AND DIODE MODELS, there are a large number of parameters that may be specified (28 for the BJT, 14 for the Diode). W. Ki and C. Hu have developed a method of determining 11 of these parameters from SCR specification sheet data[1]. The rest are given SPICE2 built in default values. A summary of this method is given in Chapter 2 along with a modification to the method of Ki and Hu. The SPICE2 SCR MODEL equivalent circuit is shown in Fig. 1.6 with applicable default values of Ki's and Hu's method applied to circuit elements.

The 10 circuit components of Fig. 1.6 are described by the following equations in which any SPICE2 default values used in the model have been applied to the equations. (θ = Einstein's Relation = .0259 V at 300°K)

$$r_{e_1} = r_{e_1} \tag{1.17}$$

$$I_{C_1} = I_{S_1} (e^{V_{EB_1}/\theta} - e^{V_{CB_1}/\theta}) - \frac{I_{S_1}}{\beta_{R_1}} (e^{V_{CB_1}/\theta} - 1) \tag{1.18}$$

$$I_{B_1} = \frac{I_{S_1}}{\beta_{F_1}} (e^{V_{EB_1}/\theta} - 1) + \frac{I_{S_1}}{\beta_{R_1}} (e^{V_{CB_1}/\theta} - 1) \tag{1.19}$$

$$C_{BE_1} = \frac{\tau_{f_1} I_{S_1}}{\theta} e^{V_{EB_1}/\theta} \tag{1.20}$$

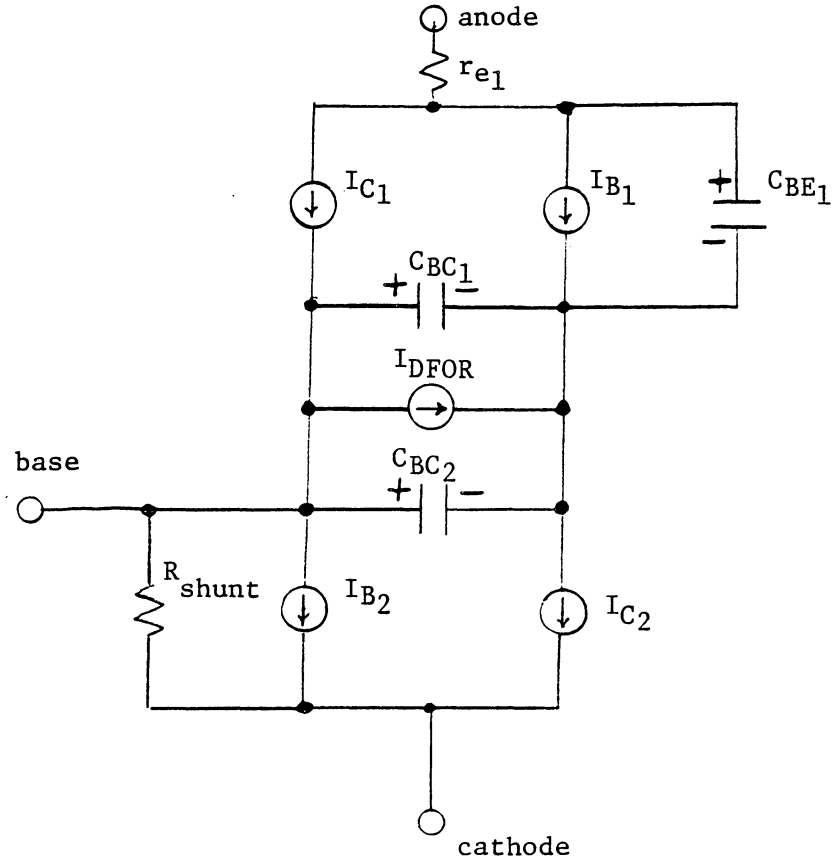


Fig. 1.6. THE SPICE2 SCR MODEL EQUIVALENT CKT

$$C_{BC_1} = \frac{\tau_{R_1} I_{S_1}}{\theta} e^{V_{CB_1}/\theta} \tag{1.21}$$

$$I_{DFOR} = \frac{I_{S_{diode}} (e^{V_{CB_1}/\theta} - 1)}{1 + \left(\frac{V_{CB_1}}{V_{BO}} \right)^6} = \frac{I_{S_{diode}} (e^{V_{BC_2}/\theta} - 1)}{1 + \left(\frac{V_{BC_2}}{V_{BO}} \right)^6} \tag{1.22}$$

$$I_{C_2} = I_{S_2} (e^{V_{BE_2}/\theta} - 2e^{V_{BC_2}/\theta} + 1) \tag{1.23}$$

$$I_{B_2} = \frac{I_{S_2}}{\beta_{f_2}} (e^{V_{BE_2}/\theta} - 1) + I_{S_2} (e^{V_{BC_2}/\theta} - 1) \tag{1.24}$$

$$C_{BC_2} = C_{jc_2} (1 - V_{BC_2})^{-.5} \tag{1.25}$$

$$R_{shunt} = R_{shunt} \tag{1.26}$$

From these 10 equations, one develops the following list of parameters that must be provided in order for the SPICE2 model to function.

List 1.1

Parameters to be determined by the "Hu-Ki Method" for implementing the two transistor SCR Model in SPICE2.

1. r_{e_1}
2. I_{S_1}
3. β_{f_1}
4. β_{R_1}

5. τ_{f_1}

6. τ_{R_1}

7. $I_{S_{diode}}$

8. V_{BO}

9. I_{S_2}

10. β_{f_2}

11. C_{jC_2}

The method of determining these parameter values is given in Ref. 1 and summarized in Chapter 2.

1.3 Summary and Conclusions

This chapter has provided general background information to support modeling the SCR using the two-transistor circuit analog.

The modified Ebers-Moll model of the bipolar junction transistor, BJT, was shown to be expressible in three different equivalent network formats while remaining mathematically identical. The three networks are denoted as the injection, the transport, and the terminal characteristics versions of the BJT model.

In relation to the two CADA programs of interest here, SPICE2 and SCEPTRE, the injection version of the BJT model is generally preferred with SCEPTRE and the terminal characteristics version of the model is the basic internal library model used with SPICE2.

Two BJT models, an NPN type and a PNP type, may be connected in a regenerative feedback configuration to provide the well-known two-transistor circuit analog to the SCR. The SPICE2 library version of the BJT has limitations which make it necessary to add additional elements to the basic two-transistor analog in order to effectively simulate the SCR. One method of modeling the SCR with SPICE2 was developed by C. Hu and W. Ki[1,8] which adds a diode to obtain junction breakdown simulation and a resistor to provide gate to cathode shunt simulation.

In order to tailor a model's performance to a specific device the parameters of the model equations may be varied. The SCR circuit analog developed by Hu and Ki in terms of SPICE2 semiconductor library elements was reduced to a more basic two terminal elements network description. The equations for each element were resolved. From these equations, a list of the minimum number of parameters necessary to individually characterize an SCR were extracted. A method of determining the eleven parameters in this list was developed by Hu and Ki. Analysis and modification of the "Hu-Ki" SCR model is the subject of the next chapter.

CHAPTER 2

MODIFICATION OF THE "HU-KI METHOD" OF MODEL PARAMETER DETERMINATION

The two-transistor model of a SCR was presented in Chapter 1. Also, the parameters required to implement this model in SPICE2 were presented. The list of required parameters (i.e. List 1.1) was extracted from analysis of the method developed by Hu and Ki for modeling the SCR using SPICE2. As a result of attempts to use the "Hu-Ki Method" SPICE2 SCR model to simulate AC RESONANT Charging Circuits, it was determined that additional development was required. This chapter presents that development.

2.1 The "Hu-Ki Method"

The SCR model of Fig. 1.5 has four device models from the SPICE2 model library interconnected to simulate the SCR. Table 2.1[12] lists the devices, the parameters necessary for input to SPICE2, and the SCR specification sheet quantities from which the required parameters may be obtained. The eleven critical model parameters of Table 2.1 are determined by the following nine step procedure developed by Hu and Ki[1][12] given in List 2.1.

2.2 Simulation of an AC RESONANT Circuit with the "Hu-Ki Method"

SPICE2 computer simulation of an AC RESONANT Charging Circuit (Fig. 2.1) was performed using the "Hu-Ki Method" to determine the parameters of a GE C602 LM SCR. The SCR chosen was one for which the "Hu-Ki Method" was verified by W. Ki in reference 1.

Table 2.1

Model Element	Critical Model Parameters	Obtainable From								
		I_H	I_{GT}	t_r	(t_{on})	V_T	R_{on}	V_{BO}	dv/dt	t_q
R	R		x							
D	BV							x		
Q_1	$\alpha_1 = \alpha_{R1}$	x	x							
	τ_{F1}			x						
	I_{S1}	x	x			x				
	R_{E1}						x			
	τ_{R1}									x
Q_2	I_{S2}	x	x			x				
	C_{jc2}	x			(x)				x	
	$\alpha_2 = 0.9$									

Table 2.1 Model Elements and Critical Parameters for the "Hu-Ki Model"

Each of the critical model parameters may be calculated from one or a combination of the thyristor specifications as shown. All other model parameters may be left unspecified. I_H: holding current, I_{GT}: gate trigger current, t_r: rise time, t_{on}: turn-on time, V_T and R_{on} are from the on-state I-V characteristics: $V = V_T + IR_{on}$, V_{BO}: forward break-over voltage, α_1: current gain of transistor 1, R_{E1}: emitter resistance of transistor, τ_F: forward transit time, C_{jc}: collector junction capacitance, I_S: $I_C = I_s e^{qV_{BE}/kT}$, etc. (Table is taken from Ref. 12, p. 175)

List 2.1. The "Hu-Ki Method" nine step procedure for determining SCR model parameters not defaulted to SPICE2 default values. Procedure is taken from Ref. 12, p. 175.

The model parameters can be obtained by following this procedure:

Part I: "normal model" characteristics:

Step 1. Given I_{GT}, find R from $R = 0.75(V)/I_{GT}$

Step 2. Set $\alpha_2 = 0.9$ or 0.95

Step 3. Given I_H and I_{GT}, find α_1 from

$$\alpha_1 = 1 - \alpha_2 + \frac{I_{GT}}{\alpha_2 I_H}$$

If $\alpha_1 > 0.9$, set $\alpha_1 = 0.9$. Find α_{R1} from $\alpha_{R1} = \alpha_1$.

Step 4. Given t_r and α_1, α_2 from Steps 1, 3, find τ_{F1} from

$$\tau_{F1} = (\beta_1\beta_2 - 1)t_r/(1.8\ \beta_1)$$

Step 5. Given V_T, find I_{S1}, I_{S2} from

$$I_{S1} = I_{S2} = 10^{-(V_T + 0.74)/0.11} \quad (A)$$

Step 6. Given R_{on}, find R_{E1} from $R_{E1} = R_{on}$

Part II: "failure mode" characteristics:

Step 7. Given t_q, find τ_{R1} from $\tau_{R1} = 9t_q$

Step 8. Given I_H, dv/dt, t_{on} (if only t_r given, assume $t_{on} = 3t_r/2$) find C_{jc2} from

$$C_{jc2}(f) = 0.4I_H(A)\sqrt{t_{on}\Big/\frac{dV}{dt}}$$

Step 9. Given V_{BO}, find diode BV from $BV = V_{BO}$

Table 2.2

Data sheet specifications		Model parameters
I_H = 100 mA		R = 9.375Ω
I_{GT} = 80 mA	following proposed	α_2 = 0.9
t_r = 3.6 μs	procedure	$\alpha_1 = \alpha_{1R}$ = 0.9
V_T = 1.1V		τ_{F1} = 17.8 μs
R_{on} = 0.005Ω		$I_{S1} = I_{S2} = 10^{-16.65}$ A
V_{BO} = 2700V	⟶	R_{E1} = 0.005Ω
dV/dt = 500V/μs		τ_{R1} = 1125 μs
t_q = 125 μs		C_{jc2} = 4000 pF
		BV = 2700V

Parameter Values for the GE C602 LM SCR Model Using the "Hu-Ki Method"

The parameter values are listed in Table 2.2.

The results of the SPICE2 simulation of the circuit of Fig. 2.1 are given in Fig. 2.2. The simulation is considered very good from the SCR triggering at 100 μs until the device commutation start at 455 μs. Where an actual device would have shown a damped oscillatory behavior in the primary current for a few micro-seconds following start of commutation, the circuit simulation presented an erratic high amplitude oscillatory behavior during this period. Circuit elements were checked closely and found to be of reasonable values. Variation of circuit values produced only slight perturbations in this erratic oscillatory behavior.

Another striking feature of the model's transient behavior following commutation was the enormously high base-emitter voltages of the NPN transistor (V(5,7) in Fig. 2.2). This voltage was also erratic in behavior indicating that nearly all of the primary current was being carried by R_{shunt} during periods of reverse current.

2.3 The Turn-off Transient of a SCR

The problems noted in simulating the AC RESONANT Circuit in section 2.2 appeared centered on the "Hu-Ki Method" SCR model's ability to simulate the SCR's turn-off transient behavior. This conclusion was supported by the results given by Hu in reference [12] which noted the model's SCR turn-off transient simulation required additional development.

Modifications to the Hu-Ki model were made to provide better

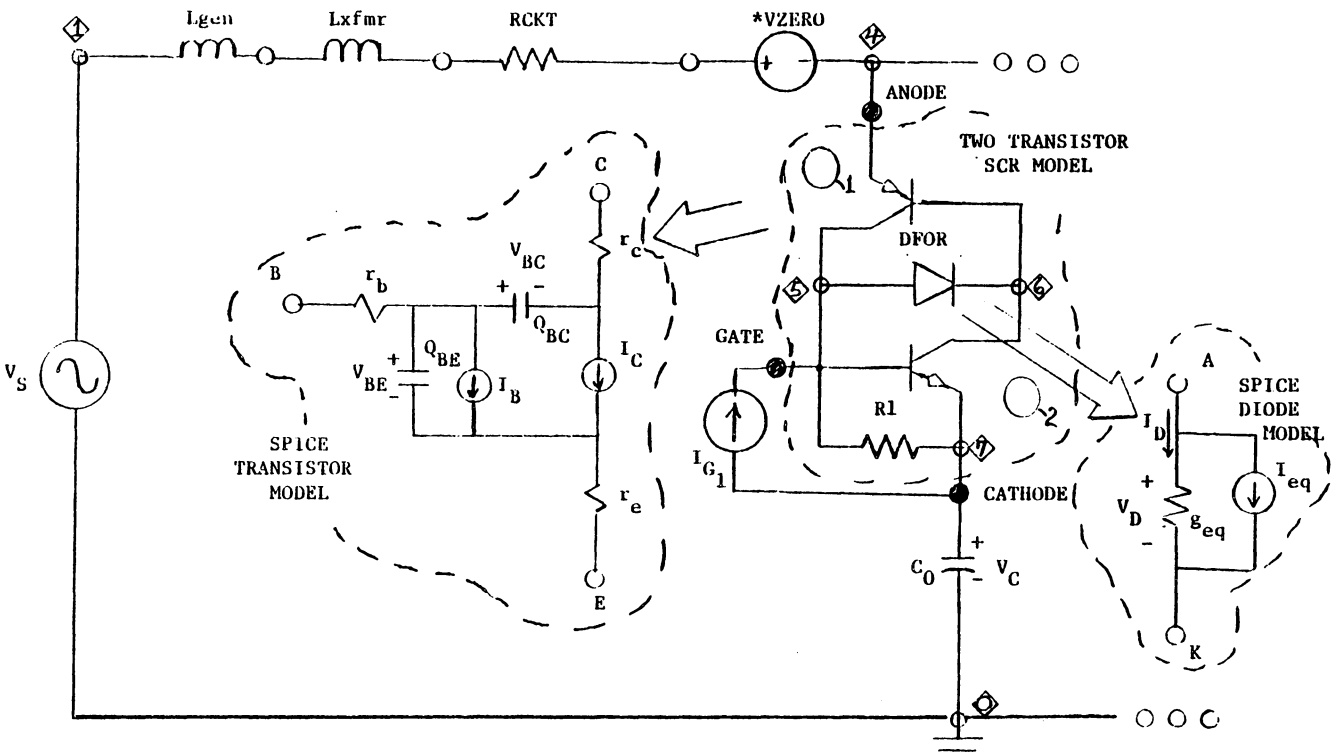


Fig. 2.1. SPICE Circuit Diagram for the Single Loop AC Resonant Charging System

*VZERO is a zero value voltage source which provides a method of simulating a test point in SPICE2

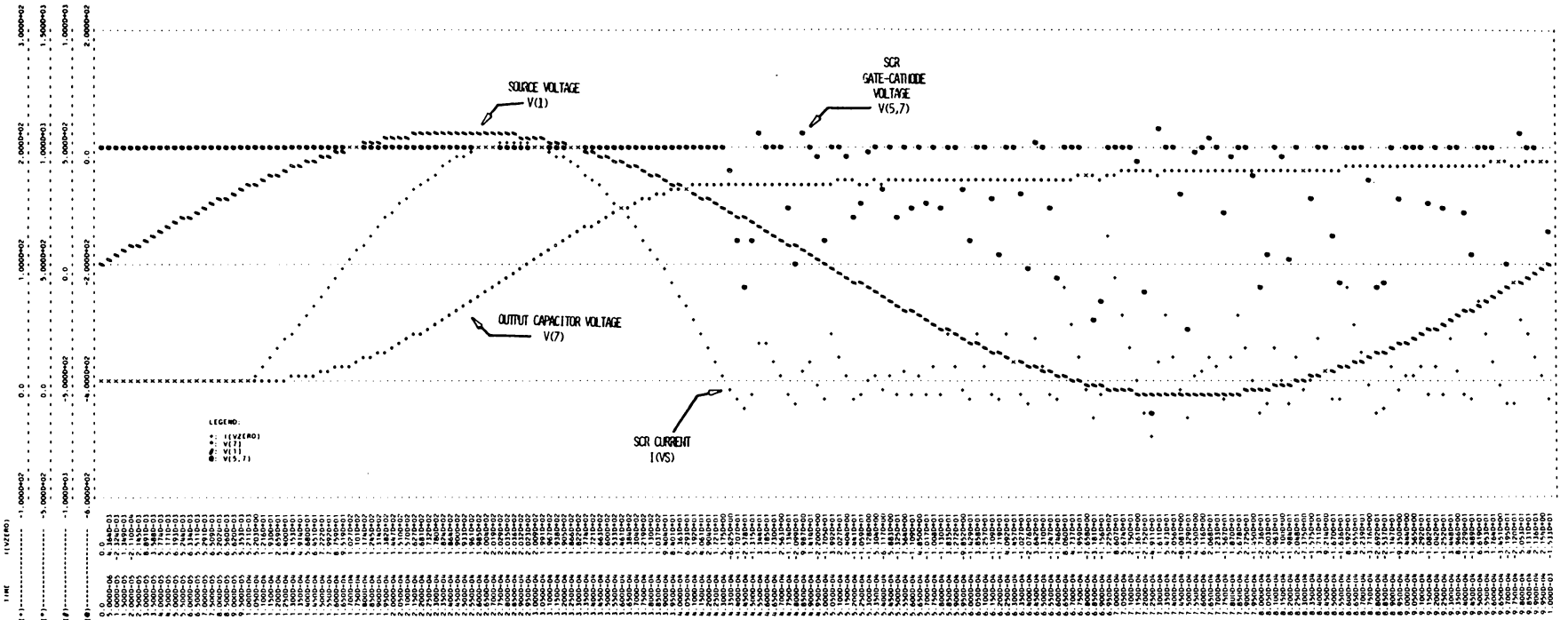


Fig. 2.2. SPICE2 Simulation of the AC Resonant Charging Circuit of Fig. 2.1.

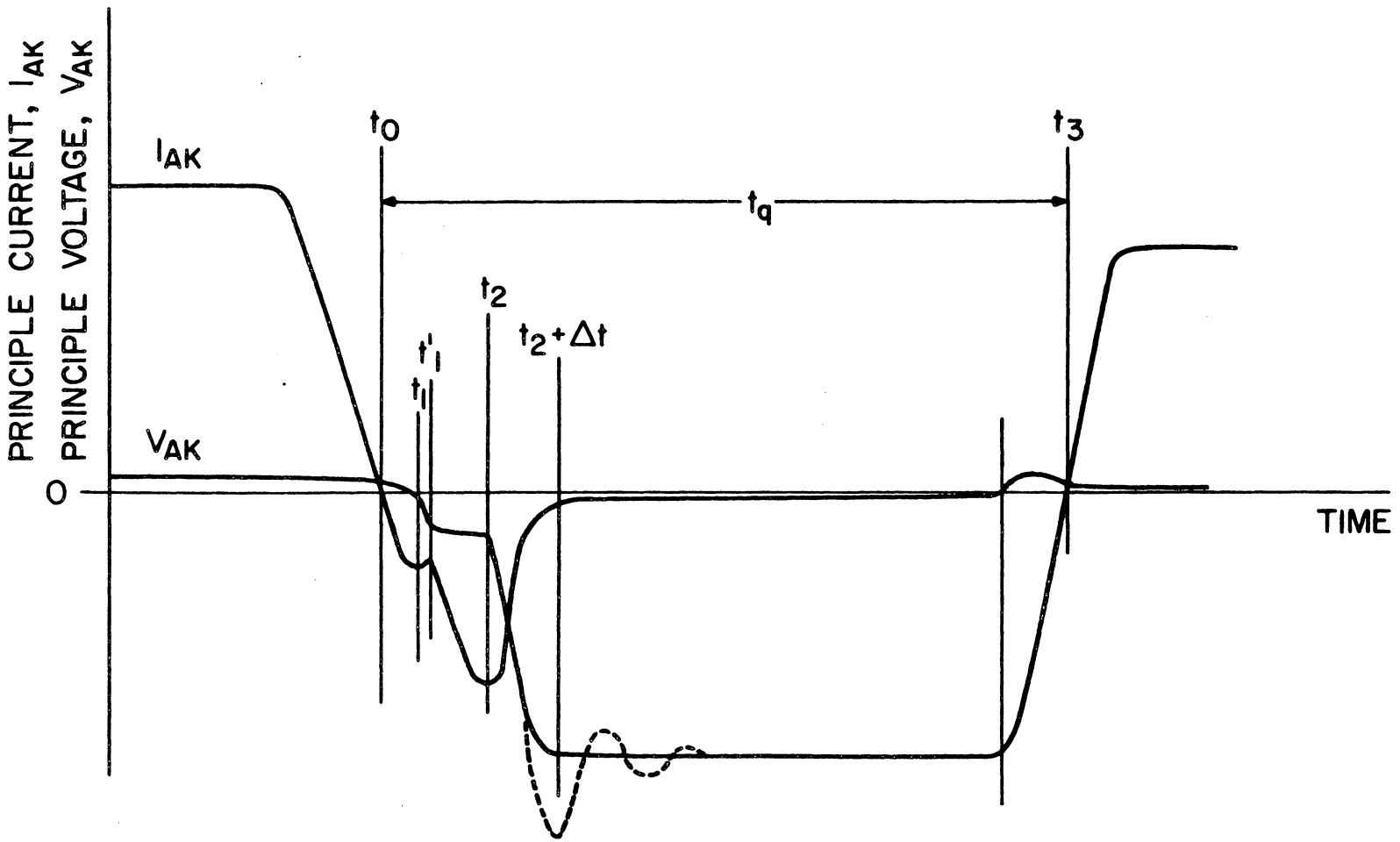


Fig. 2.3. TURN-OFF TRANSIENT OF A SCR[11, p.89].

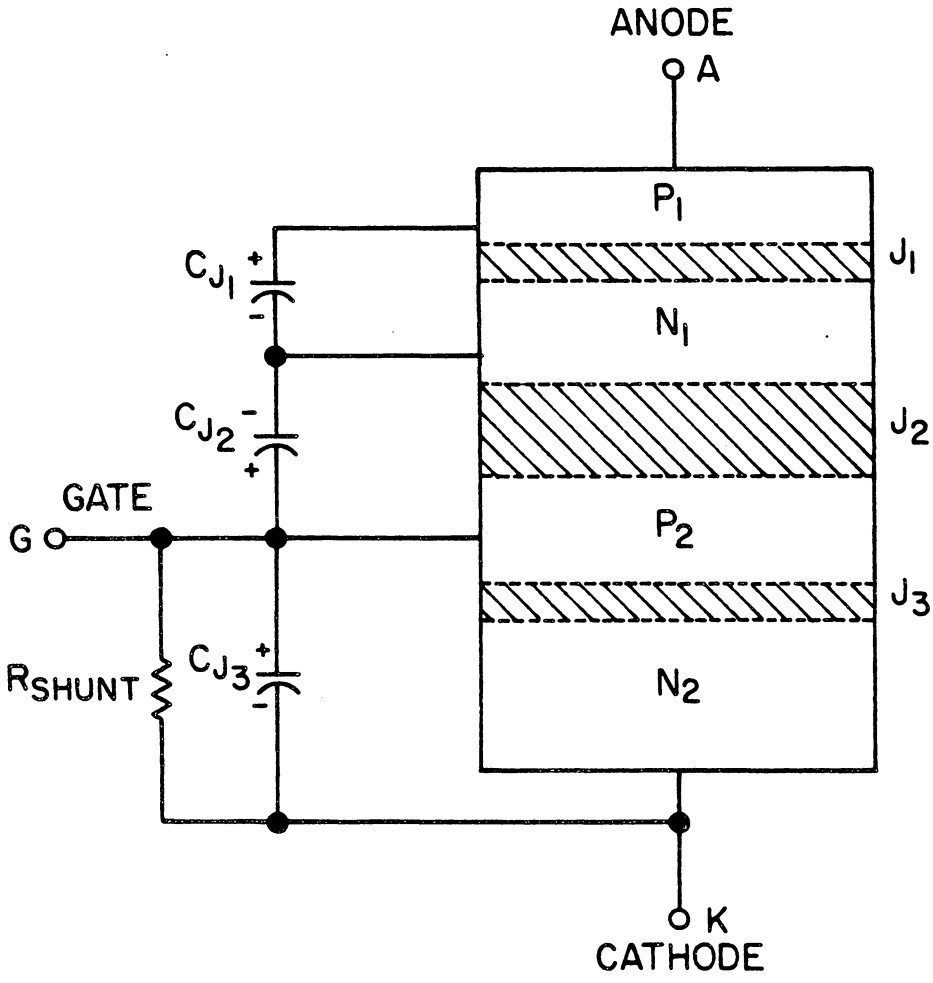


Fig. 2.4. SCR REPRESENTATION SHOWING JUNCTION CAPACITANCES AND POLARITY OF CHARGE DURING SCR ON STATE.

simulation of the reverse transient behavior of a SCR as depicted in Fig. 2.3[11]. Modifications were limited to those necessary to simulate gross behavior of the device with minor effects left unsimulated. The reverse transient behavior of a SCR and corresponding modifications to the model are described as follows.

Figure 2.4 is used for illustrative purposes in the following discussion. Each of the three junction capacitances, C_J, are composed of two terms, a diffusion term and a depletion layer term as in Eqns. 1.1 and 1.2. Where significant forward current flows through the forward biased junction, the diffusion term is much larger than the depletion layer term. However, when the junction is reverse biased, the diffusion term becomes an extremely small value while the depletion layer term continues to be significant.

Now, using Figures 2.3 and 2.4, the turn-off transient (denoted by the period t_q in Fig. 2.3) is traced in terms of events occurring within the SCR.

(1) t_o to t_1 - Excess carriers are being swept out of C_{J_1} and C_{J_3}

(2) t_1 to t_1' - C_{J_3} which is much smaller than C_{J_1} starts to reverse charge polarity. V_{AK} starts to become negative. Note that this voltage drop is entirely supported by J_3.

(3) t_1' - J_3 experiences avalanche breakdown.

- In simulating the SCR reverse transient, C_{J_3} is small enough to be neglected. The avalanche breakdown of J_3 is very significant, however. As shown in Fig. 2.2 by V(5,7), failure to simulate this

breakdown may result in serious distortion of the reverse transient voltage drop across J_3. Since SPICE2 has no capability to simulate a junction breakdown in its transistor model, then a diode (for which breakdown is modeled in SPICE2) must be added in parallel with J_3. J_3 is the base-emitter junction of Q_2 in the "Hu-Ki Model". Addition of this diode is illustrated in Fig. 2.5 as DJCTN1.

SCR specification sheet data frequently specifies a maximum reverse gate voltage. This limitation of $-V_G$ gives an indication of the J_3 breakdown voltage. If this specification is given, then set the breakdown voltage of DJCTN1 (V_{BO}) equal to 1.1 x max{$-V_G$} otherwise use V_{BO} = 5V.

$$V_{BO_{DJCTN1}} = \left\{ \begin{array}{l} 1.1 \text{ x } \max\{-V_G\} \\ \text{or 5V [11, p. 87]} \end{array} \right\} \tag{2.1}$$

To minimize influence of the diode on forward biasing of the Q_2 base-emitter junction, set the saturation current of the diode ($I_{S_{DJCTN1}}$) to less than 10% of the Q_2 saturation current (I_{S_2} of Table 2.1).

$$I_{S_{DJCTN1}} \leq .1\ I_{S_2} \tag{2.2}$$

(4) t_1' to t_2 - carriers being swept out of J_1.

(5) t_2 to $t_2 + \Delta t$ - J_1 becoming reverse biased as charge on C_{J_1} is being reversed.

- The "Hu-Ki Model" uses only a diffusion term to describe C_J (Ref. Eqn. 1.20, sec. 1.2). When the device is used in LC circuits

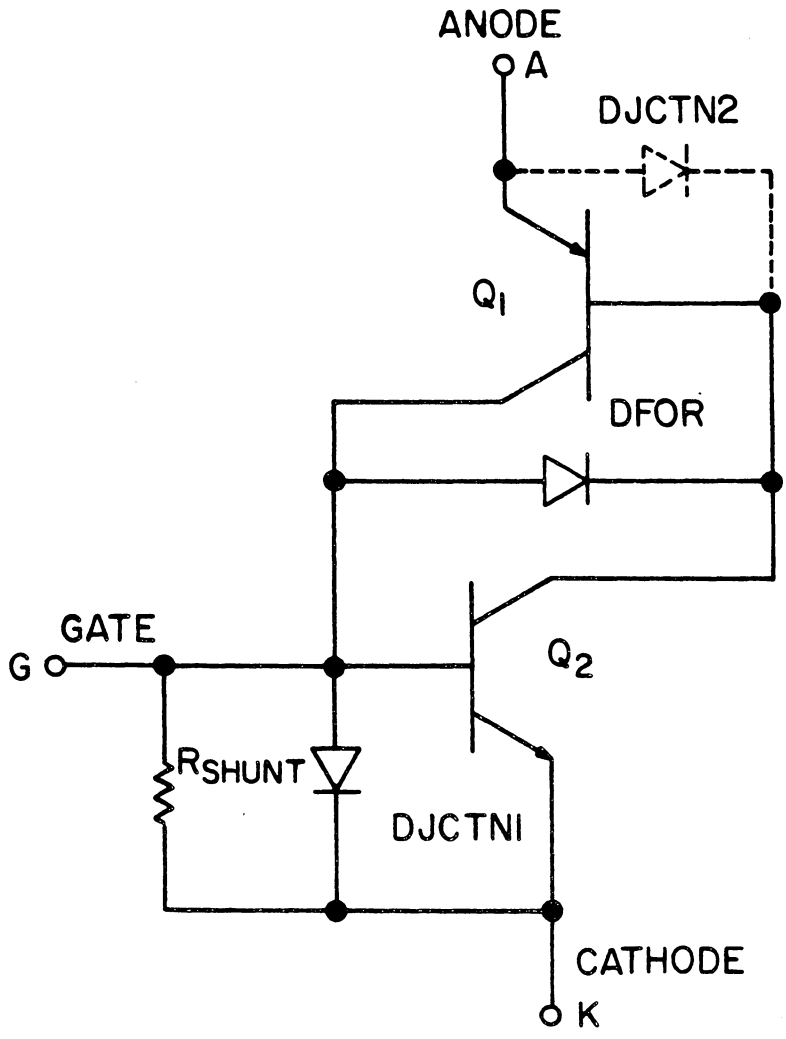


Fig. 2.5. "MODIFIED HU-KI MODEL" OF THE SCR FOR SPICE2.

such as illustrated in Fig. 2.1, energy is stored in the inductor when I_{AK} goes negative. This energy must eventually be transferred to the J_1 capacitance. Since this capacitance, as described by Eqn. 1.20, is becoming extremely small as J_1 (the emitter-base junction of Q_1 in the two-transistor model) is reverse biased, then the voltage across J_1 must become extremely large in order to contain the energy (in actuality, the junction would breakdown before reaching such a voltage). This accounts for the erratic oscillatory behavior seen in Fig. 2.2 following device commutation.

Correction of the model's simulation of SCR behavior requires two modifications. Adding a depletion layer capacitance term to Eqn. 1.20 will allow the inductive energy to be stored in J_1 without reaching excessive reverse V_{AK} in a properly designed circuit. Equation 1.20 becomes:

$$C_{BE_1} = \frac{\tau_{f_1} I_{S_1}}{\theta} \left(e^{V_{EB_1}/\theta} - 1\right) + C_{JE_1}\left(1 - V_{EB_1}\right)^{-1/2} \qquad (2.3)$$

depletion layer term

In the event that junction breakdown voltage should be exceeded, then a diode ((DJCTN2) in Fig. 2.5) may be added in parallel with the emitter-base junction of Q_1.

With this result, three more parameters must be supplied to the model.

$$C_{JE_1} \left\{ \begin{array}{l} \geq .5\ C_{JC_2} \\ \leq C_{JC_2} \end{array} \right\} \qquad (2.4)$$

where C_{JC_2} is that determined in step 8 of the "Hu-Ki Method". Since J_1 and J_2 are typically reasonably similar junctions[14].

$$I_{S_{DJCTN2}} \leq .1\ I_{S_1} \qquad (I_{S_1} \text{ from step 5 of the "Hu-Ki Method"}) \qquad (2.5)$$

$$V_{BO_{DJCTN2}} \approx V_{BO} \qquad (V_{BO} \text{ from step 9 of the "Hu-Ki Method"}) \qquad (2.6)$$

As with DJCTN1 discussed earlier, care must be taken to avoid the diode influencing the forward characteristics of the Q_1 emitter-base junction.

Note: The addition of DJCTN2 is purely optional in that it only models a failure of the SCR during a reverse transient.

(6) $t_2+\Delta t$ - Reverse principal current decreases to a very low value. Fig. 2.3 is mainly illustrative to facilitate discussion of the turn-off transient. Many actual circuits are not overdamped and some small damped oscillation would be observed in this area.
J_1 supports the full reverse voltage ($-V_{AK}$) at this time.

(7) $t_2+\Delta t$ to t_3 - Excess carriers (primarily in the N_1 region, Fig. 2.4) must recombine before the device will support a reapplication of forward voltage.

(8) t_3 - the SCR supports reapplied forward voltage and commutation is considered complete.

- The $t_2 + \Delta t$ to t_3 period is typically the major portion of the commutation interval. During this period, very little primary (terminal) current flows.

In this region one must be fully conscious of the fact that the SCR model is a functional one and does not simulate the true physical processes within the device. The physical process of excess carrier combination which occurs without current flow, in the circuit sense, is modeled thru the device of a capacitor discharging around a loop.

In the "Hu-Ki Model" the capacitance is the diffusion term in the base-collector capacitance of Q_1 given by Eqn. 1.21 in Chapter 1. The discharge loop has four parallel paths indicated by P_1, P_2, P_3 and P_4 in Fig. 2.6. Noting that the current in P_4 is principal current, then this current must be very small. Since P_4 current is derived via third quadrant operation of Q_1 and Q_2 then small P_4 implies very small P_2 and P_3 currents. From this, we see that P_1 current must provide the dominant discharge path for C_{BC_1}, the base-collector diffusion capacitance of Q_1, which represents the excess charge stored in the N_1 region of the $P_1N_1P_2N_2$ device.

P_1 current is the current through DFOR (Fig. 2.5). This diode provided in the "Hu-Ki Model" to simulate the high voltage turn-on of an SCR is conveniently in position to allow control of the re-combination interval of the commutation time while maintaining low values of principal current. To do this, the saturation current of

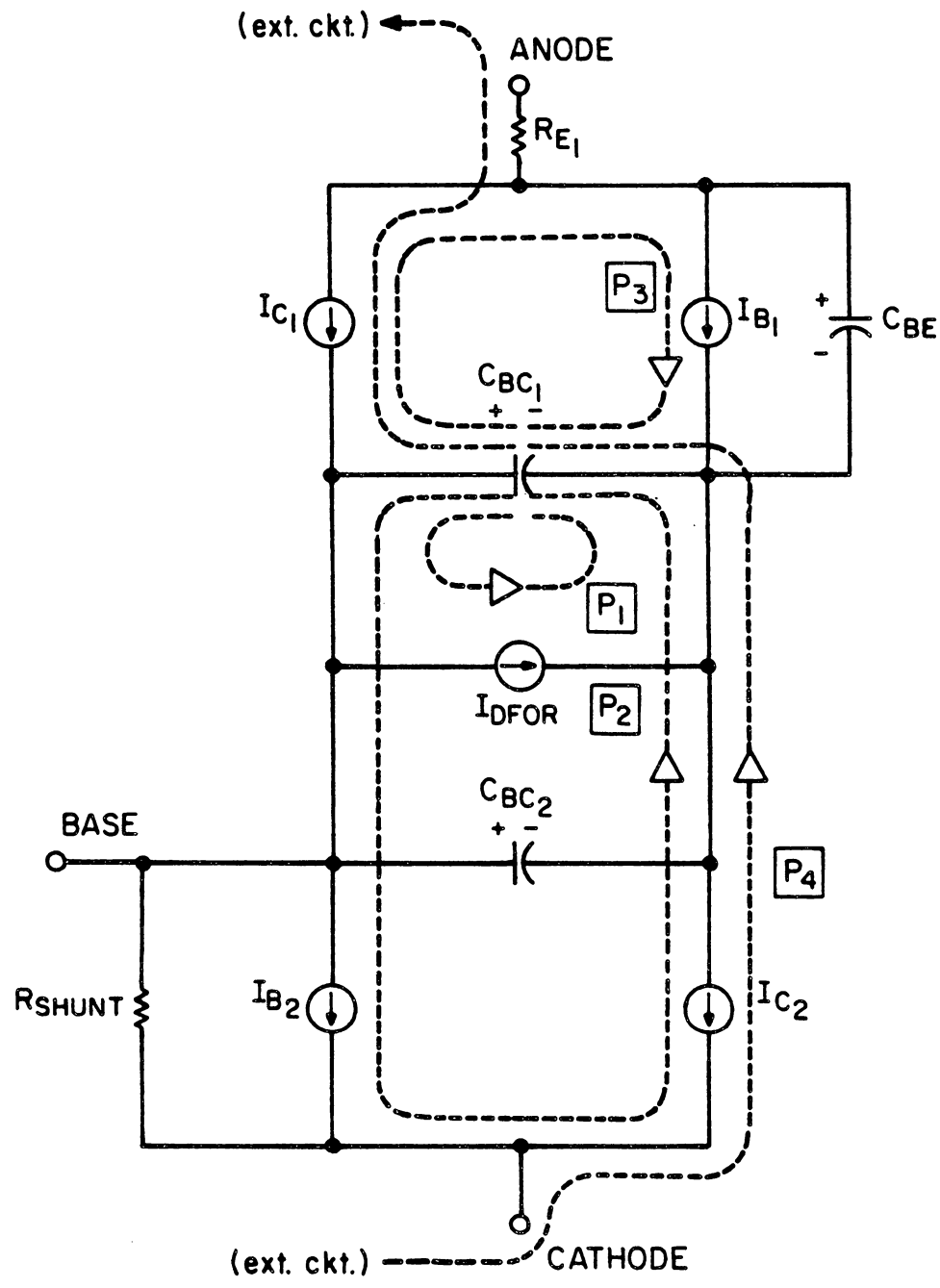


Fig. 2.6. DISCHARGE PATHS FOR C_{BC_1} IN THE "HU-KI MODEL".

DFOR, $I_{S_{DFOR}}$, must be made much greater than the saturation currents of Q_1 and Q_2 (I_{S_1} and I_{S_2} respectively).

$$I_{S_{DFOR}} >> I_{S_1} = I_{S_2} \tag{2.7}$$

The "Hu-Ki Model" uses the SPICE2 default value of 10^{-14} for $I_{S_{DFOR}}$. Since step 5 of List 2.1 is used to determine I_{S_1} and I_{S_2}, it is evident that the condition that $P_1 >> P_4$ may not always hold by the "Hu-Ki Method".

One way of improving the model would be to assign $I_{S_{DFOR}}$ some arbitrarily greater value than I_{S_1} and I_{S_2}. For example, let $I_{S_{DFOR}} = 10^3 \times I_{S_1}$. Then adjust the diffusion capacitance term (via τ_{R_1} of Eqn. 1.21, Chapter 1) to meet the commutation time criteria. An alternative method is to preset the diffusion capacitance term then determine some method of selecting an appropriate $I_{S_{DFOR}}$. Since the "Hu-Ki Method" provides the diffusion capacitance term (i.e. τ_{R_1}, Eqn. 1.21), then the latter approach is selected here.

Using Fig. 2.7 for illustration, the following discussion presents an analytic method of determining an appropriate value for $I_{S_{DFOR}}$ using two network constraints as apply to Fig. 2.7.

$$V_{AK} = V_{J_1} + V_{J_2} + V_{J_3} = V_{EB_1} + V_{BC_1} + V_{BE_2} \tag{2.8}$$

$$I_{DFOR} = \alpha_1 I_A - (1 - \alpha_2)(I_A - I_R) \tag{2.9}$$

Noting that $I_{S_1} = I_{S_2}$, $\theta \simeq .0259V$ @ 300°K then:

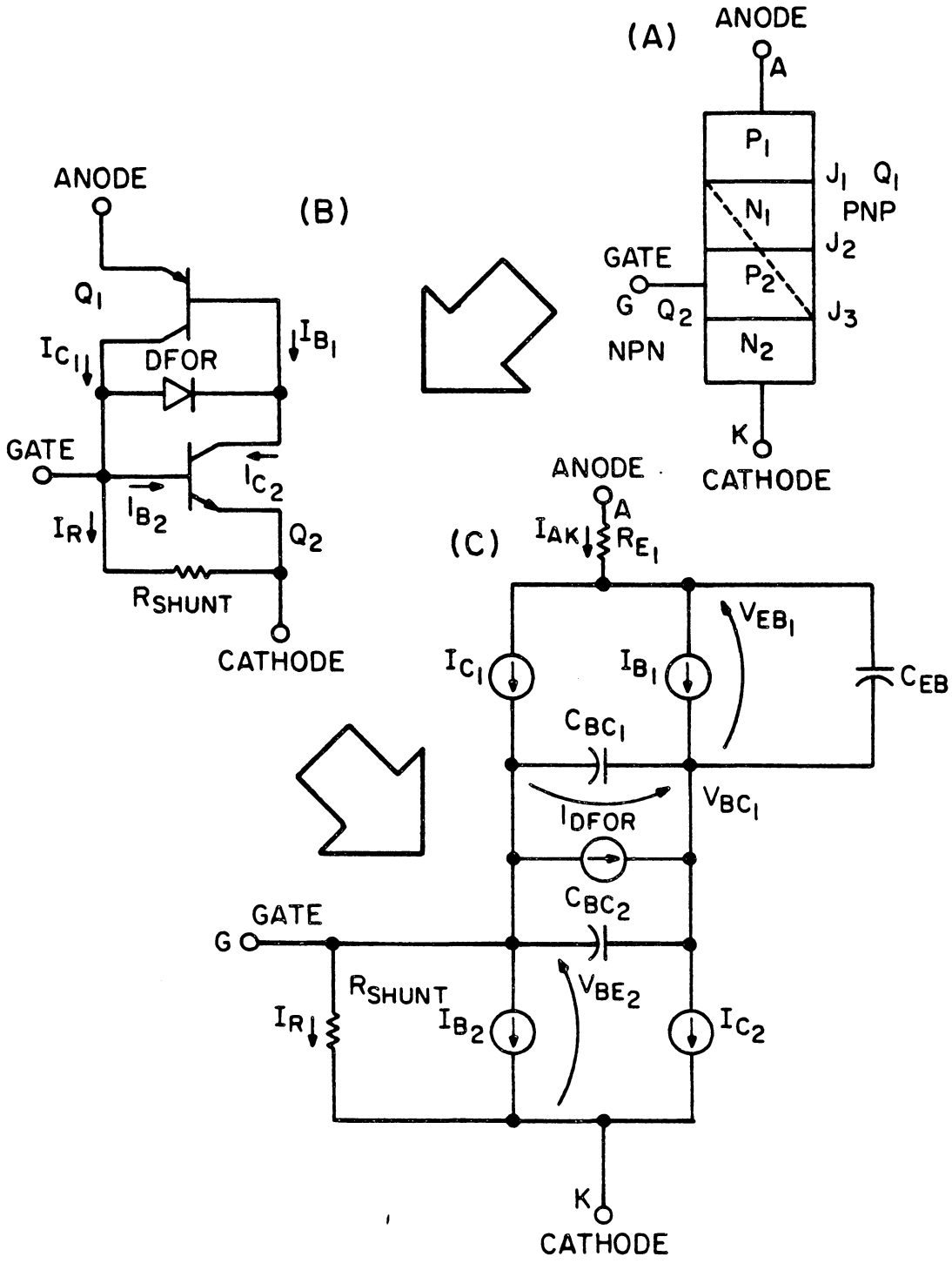


Fig. 2.7. SPICE2 SCR MODEL BASED ON "HU-KI METHOD".

$$I_A = I_S(e^{\frac{V_{EB_1}}{\theta}} - 1) \approx I_S\, e^{\frac{V_{EB_1}}{\theta}} \tag{2.10}$$

gives:

$$V_{EB_1} = \theta \ln\left(\frac{I_A}{I_S}\right) \tag{2.11}$$

Also:

$$(I_A - I_R) = I_S(e^{\frac{V_{BE_2}}{\theta}} - 1) \approx I_S\, e^{V_{BE_2}/\theta} \tag{2.12}$$

gives:

$$V_{BE_2} = \theta \ln\left(\frac{I_A - I_R}{I_S}\right) \tag{2.13}$$

Now:

$$I_{DFOR} = I_{S_{DFOR}}(e^{\frac{-V_{BC_1}}{\theta}} - 1) \approx I_{S_{DFOR}}\, e^{\frac{-V_{BC_1}}{\theta}} \tag{2.14}$$

and Eqn. 2.9 gives

$$V_{BC_1} = \theta \ln\left(\frac{I_{S_{DFOR}}}{\alpha_1 I_A - (1 - \alpha_2)(I_A - I_R)}\right) \tag{2.15}$$

Referring to Fig. 2.8 which gives the V-I characteristic of a SCR, the known point (I_H, V_H) available from the specification sheet data may be used to develop the relation between $I_{S_{DFOR}}$ and I_S.

Using Eqns. 2.8, 2.11, 2.13, and 2.15,

$$V_{AK} = V_H = \theta \ln\left(\frac{I_H}{I_S}\right) + \theta \ln\left(\frac{I_{S_{DFOR}}}{\alpha_1 I_H - (1-\alpha_2)(I_H - I_R)}\right) + \theta \ln\left(\frac{I_H - I_R}{I_S}\right) \tag{2.16}$$

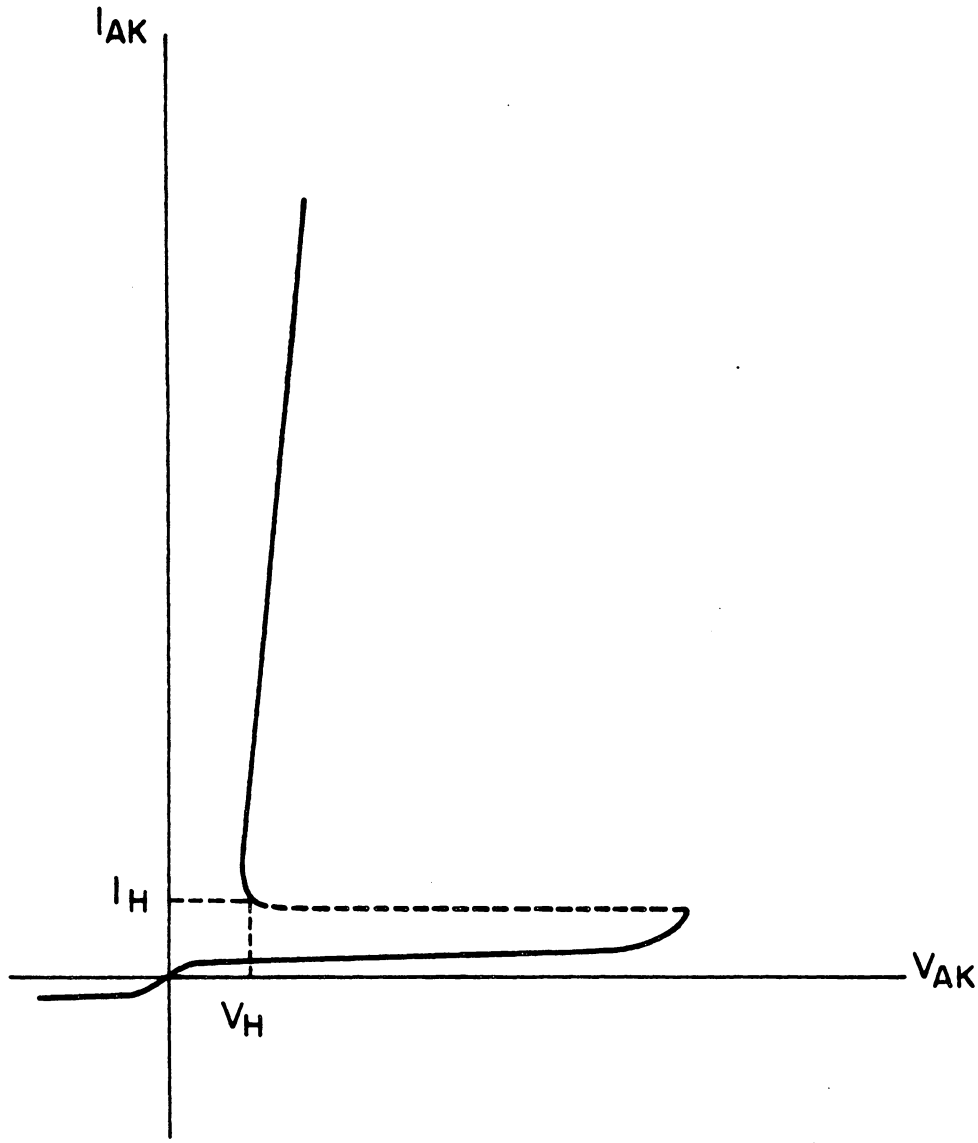


Fig. 2.8. SCR V-I CHARACTERISTIC CURVE.

Now at $I_A = I_H$, $I_R \simeq I_{GT}$ [1, p. 46] a specification sheet value. Substitution into Eqn. 2.16 gives

$$I_{S_{DFOR}} = \exp\left(\frac{V_H}{\theta}\right) - \ln\left(\frac{I_H}{I_S}\right) - \ln\left(\frac{I_H - I_{GT}}{I_S}\right) + \ln(\alpha_1 I_H - (1-\alpha_2)(I_H - I_{GT}) \quad (2.17)$$

With the development of Eqn. 2.17 the parameters $I_{S_{DFOR}}$ may not be provided to the SPICE2 SCR model bringing the total to 17 parameters (15 if DJCTN2 is omitted).

2.4 The Modified "Hu-Ki Method" of Parameter Determination for SPICE2 SCR Model

Ki demonstrated the turn-off transient behavior of the "Hu-Ki Model" for a Motorola 2N685 in Reference 1. Comparative test simulation has been done using the "modified Hu-Ki Model". Results of the comparison test are given in Figs. 2.10 and 2.12. The "modified Hu-Ki Model" is observed in Fig. 2.12 to give substantially more realistic results with respect to peak reverse current and primary current amplitude during the recombination interval. Since no specific specifications are normally given in the SCR spec. sheet then qualitative judgement is the basis for this opinion.

One phenomenon was observed with the modified model in that the addition of the J_1 depletion layer capacitances resulted in a slightly higher value of high voltage turn-on behavior than for the unmodified model. This phenomenon is not yet explained.

```
MOTOROLA 2N685 - COMMUTATION TIME TEST CIRCUIT - KI'S EXAMPLE

      INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


R  0  1  125
RL  4  7  1
L  6  7  10UH
VS  2  0  PWL(0  11.371  40US  11.371  40.001US  -50  70US  -50  75US  200)
VZERO  2  8  DC  0
DFOR  1  3  DMOD1
Q1  1  3  4  QMOD1
Q2  3  1  0  QMOD2
.MODEL  DMOD1  D(BV=200)
.MODEL  QMOD1  PNP(BF=9,BR=9,IS=1.0E-17.65,RE=0.012,TF=6.3US,TR=270US)
.MODEL  QMOD2  NPN(BF=9,IS=1.0E-17.65,CJC=920PF)
.OPTIONS  NOMOD  NOPAGE  LVLTIM=1  ITL5=10000  LIMPTS=10000
.TRAN  10S  70US  35US
.PRINT  TRAN  V(2)  V(4)  I(VZERO)
.PLOT  TRAN  I(VZERO)  V(2)  V(4)
.END
```

Fig. 2.9. Motorola 2N685 - Commutation Time Test Circuit - Ki's Example

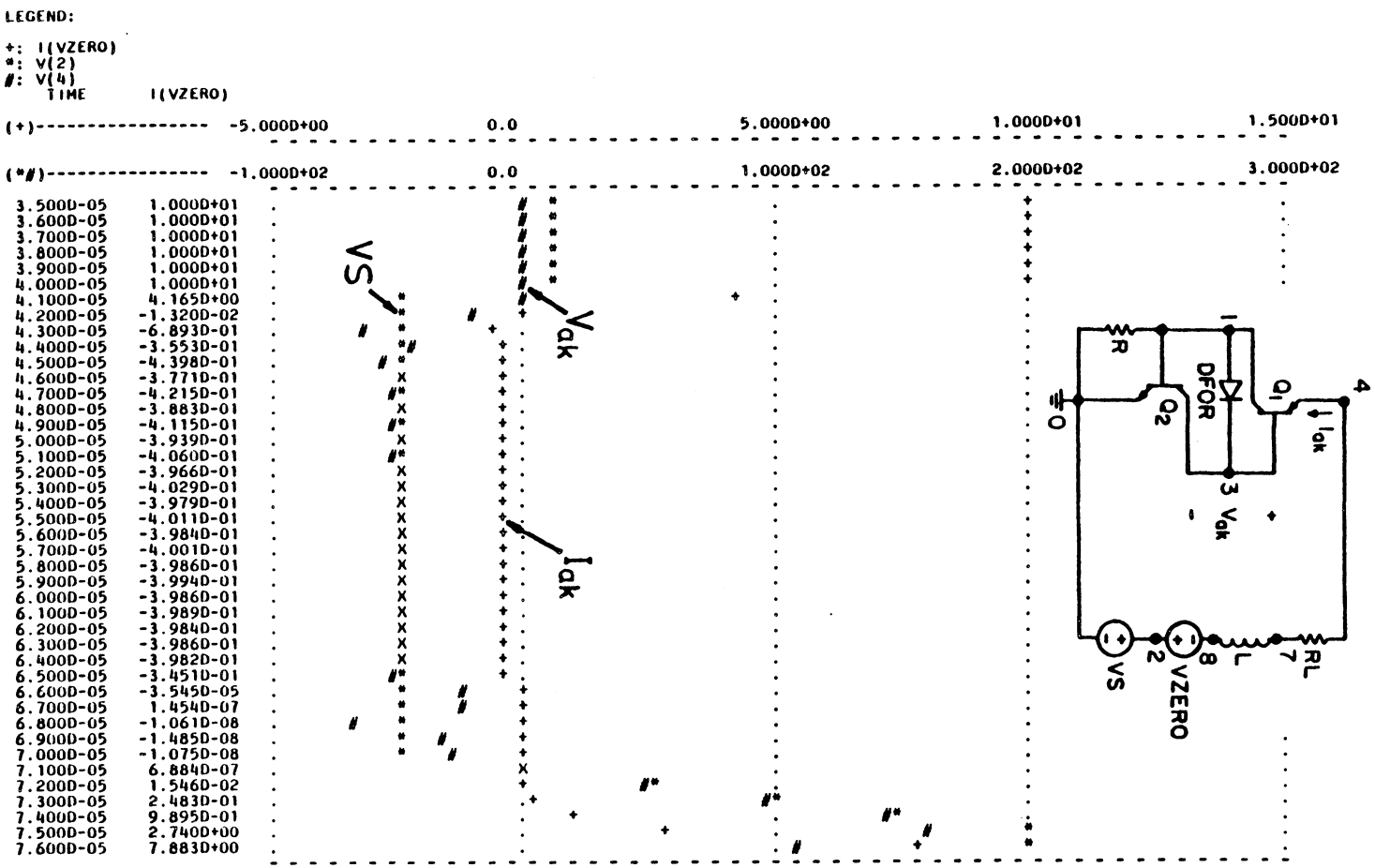


Figure 2.10 SPICE2 Simulation of the Turn-off Transient of the "Hu-Ki Model" as Given in Figure 2.9.

```
MOTOROLA 2N685 - COMMUTATION TIME TEST CIRCUIT - MODIFIED MODEL

     INPUT LISTING                              TEMPERATURE =    27.000 DEG C

*******************************************************************************


R  0  1  125
RL  4  7  1
L  8  7  100H
VS  2  0  PWL(0  11.371  40US  11.371  40.001US  -50  70US  -50  75US  20)
VZERO  2  8  DC  0
DFOR  1  3  DMOD1
DJCTN  1  0  DMOD2
.MODEL  DMOD2  D(IS=1E-18.65,BV=5)
Q1  1  3  4  QMOD1
Q2  3  1  0  QMOD2
.MODEL  DMOD1  D(BV=200,IS=7.62E-15)
.MODEL  QMOD1  PNP(BF=9,BR=9,IS=1.0E-17.65,RE=0.012,TF=8.3US,TR=270US,CJE=920PF)
.MODEL  QMOD2  NPN(BF=9,IS=1.0E-17.65,CJC=920PF)
.OPTIONS  NOMOD  NOPAGE  LVLTIM=1  ITL5=10000  LIMPTS=10000
.TRAN  10US  70US  35US
.PRINT  TRAN  V(2)  V(4)  I(VZERO)
.PLOT  TRAN  I(VZERO)  V(2)  V(4)
.END
```

Fig. 2.11. Motorola 2N685 - Commutation Time Test Circuit - Modified Model

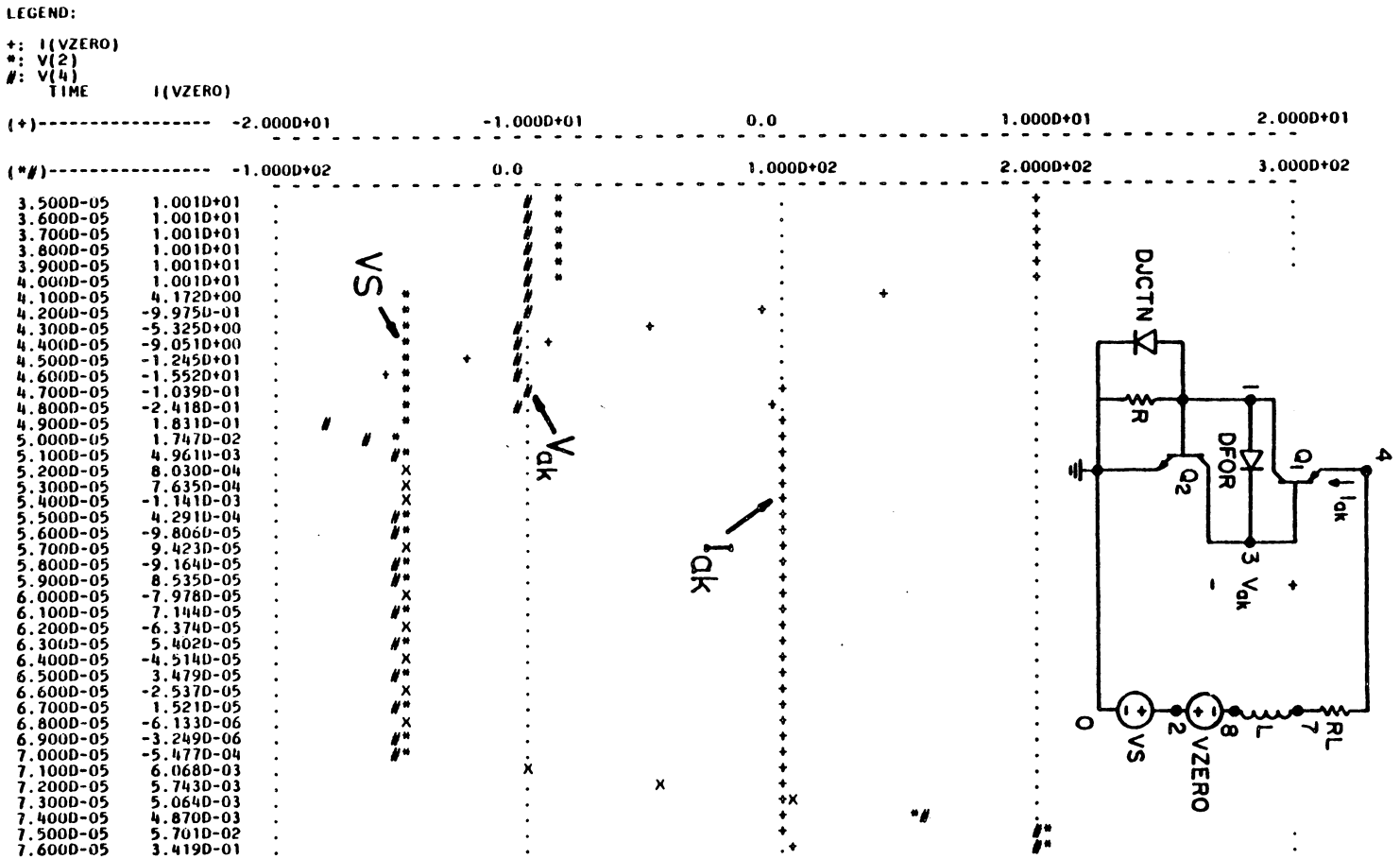


Figure 2.12 SPICE2 Simulation of the Turn-off Transient of the "Modified Hu-Ki Model" as Given in Figure 2.11.

Chapters 3 and 4 demonstrate the performance of the "modified Hu-Ki Model" when used to simulate AC Resonant Charging Circuits including a comparative example to the results shown in Fig. 2.2 for the unmodified model.

2.5 Summary and Conclusions

This chapter has analyzed and developed modifications to a method of modeling the SCR with SPICE2. The modeling procedure was originally proposed by C. Hu and W. Ki[1,8]. This approach called for an SCR circuit analog composed of four SPICE2 internal model library elements; a NPN transistor, a PNP transistor, a diode, and a resistor. Hu and Ki developed a combination analytical and graphical method of estimating the eleven required parameters (ref. list 1.1) for the model using manufacturer's specification sheets for a data base.

An attempt to model an AC resonant charging circuit with the "Hu-Ki" SCR model revealed problems with the model's ability to simulate SCR turn-off behavior. Analysis showed the problem to be an inadequate description of the P_1N_1 junction (i.e. anode junction) depletion layer capacitance and inadequate description of the P_2N_2 junction (i.e. cathode junction) avalanche breakdown during the device turn-off transient. Corrections were incorporated into the model along with other improvements. Other improvements were an analytical method of determining the center

junction reverse saturation current, and the anode junction reverse breakdown. The altered circuit analog and the corresponding parameter estimation procedure were denoted the "modified Hu-Ki" model. The device turn-off transient simulation was much improved by the modifications incorporated. A series of typical phase-control-SCR-circuit-simulation demonstrations are presented in the next two chapters to assess this SPICE2 SCR modeling capability in actual applications.

The modeling capability achieved at this point can not meet the thesis objectives. Two major shortcomings are that it is not general purpose since it is restricted to use with SPICE2 and that achieving adequate SCR simulation has resulted in a rather bulky extension in the element count beyond the basic two-transistor circuit analog. The latter shortcoming complicates understanding of the model and makes alteration to alternative technology awkward if not prohibitive. These problems are treated in Chapter 5.

CHAPTER 3

SPICE2 SIMULATIONS OF SINGLE LOOP AC RESONANT CIRCUITS

This chapter presents the results of simulating a single loop AC Resonant Charging Circuit using SPICE2. SPICE2 simulations are done with the "Modified Hu-Ki Model" of the SCR.

3.1 SPICE2 Single Loop Simulation Results

Chapter 2 presented the results of a simulation of an AC Resonant Charging Circuit using the unmodified "Hu-Ki Model" (ref. Fig. 2.2). A comparative example is given in Fig. 3.2 which illustrates the results of simulating the circuit of Fig. 3.1 using the "Modified Hu-Ki Model" developed in Chapter 2. Striking improvement is noted in the turn-off simulation results during the period following start of SCR commutation at approximately 500 μs.

The circuit of Fig. 3.3 (corresponding results are in Fig. 3.4) has a snubber added to demonstrate a means of suppressing the damped oscillatory behavior following SCR commutation. Such oscillatory behavior may be detrimental to some circuit configurations as illustrated by the two loop circuit simulations presented in Chapter 4.

```
GE C602 LM SCR - ONE BRANCH AC RES CHG'NG CKT - DESCRETE - NO SNUBBER

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************


VS 1 0 SIN(0 566 1K )
VZERO 3 4 SIN(0 0 0)
IG1 7 5 PULSE(0 .5 100US 0 0 100US )
LXFMR 1 2 5MH
RCKT 2 3 5.0
Q1 5 6 4 QMOD1 OFF
Q2 6 5 7 QMOD2 OFF
DFOR 5 6 DMOD1 OFF
DJCTN1 5 7 DMOD2
RSH1 5 7 9.375
C01 7 0 5.0UF
.MODEL DMOD1 D(BV=2700,IS=5.58E-15)
.MODEL DMOD2 D(BV=5 IS=1.0E-16)
.MODEL QMOD1 PNP(BF=9,BR=9,IS=1.0E-16.65,RE=.005,TF=17.6US,TR=112.5US,CJE=4000PF)
.MODEL QMOD2 NPN(BF=9,IS=1.0E-16.65,CJC=4000PF)
.TRAN 5US 100US
.PRINT TRAN I(VZERO) V(7,0) V(1) V(4,6) V(5,6) V(5,7)
.PRINT TRAN V(5,6) V(4,6)
.PLOT TRAN I(VZERO) V(7,0) V(1)
.OPTIONS NOMOD NOPAGE LVLTIM=1 ITL5=10000 LIMPTS=10000
.END
```

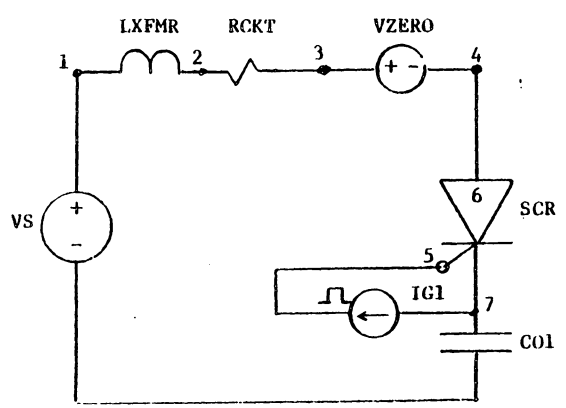


Figure 3.1. Single Loop Circuit Without Snubber

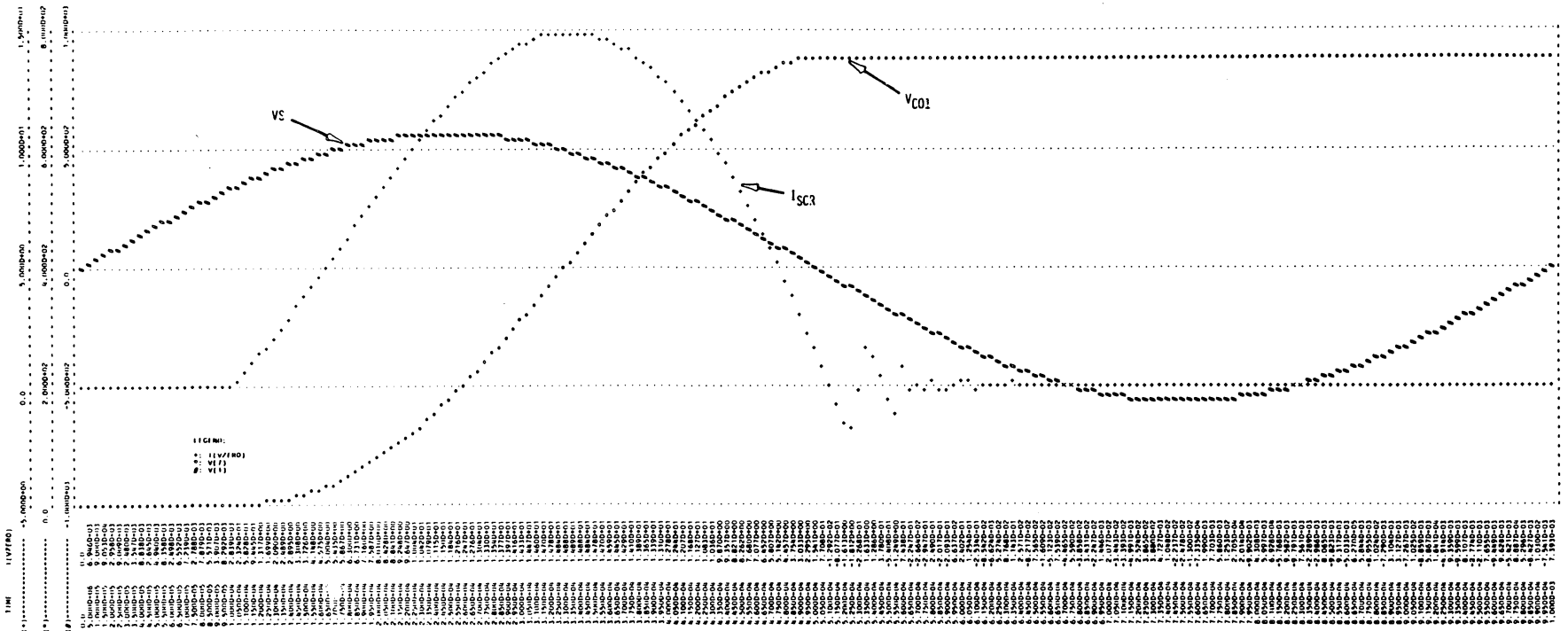


Figure 3.2 SPICE2 Simulation of a Single Loop AC Resonant Charging Circuit (Figure 3.1) using the "Modified Hu-Ki Model" of a SCR.

```
GE C602 LM SCR - ONE BRANCH AC RES CHGING CKT - DESCRETE - WITH SNUBBER

     INPUT LISTING                          TEMPERATURE =    27.000 DEG C

*******************************************************************************


VS 1 0 SIN(0 566 1K )
VZERO 3 4 SIN(0 0 0)
IG1 7 5 PULSE(0 1.0 100US 0 0 50US )
LXFMR 1 2 5MH
RCKT 2 3 5.0
Q1 5 6 4 QMOD1 OFF
Q2 6 5 7 QMOD2 OFF
DFOR 5 6 DMOD1 OFF
CS 9 3 0.1UF
RS 9 7 100
DS 9 7 DMOD1 OFF
RSHT1 5 7 9.375
C01 7 0 50F
.MODEL DMOD1 D(BV=2700,IS=5.56E-15)
.MODEL QMOD1 PNP(BF=9,BR=9,IS=1E-16.65,RE=.005,TF=17.8US,TR=1125US,CJE=4000PF)
.MODEL QMOD2 NPN(BF=9,IS=1E-16.65,CJC=4000PF)
.TRAN 50S 10000S
.PRINT TRAN I(VZERO) V(7,0) V(1) V(5,7)
.PLOT TRAN I(VZERO) V(7,0) V(1)
.OPTIONS NOMOD NOPAGE LVLTIM=1 ITL5=10000 LIMPTS=10000
.END
```

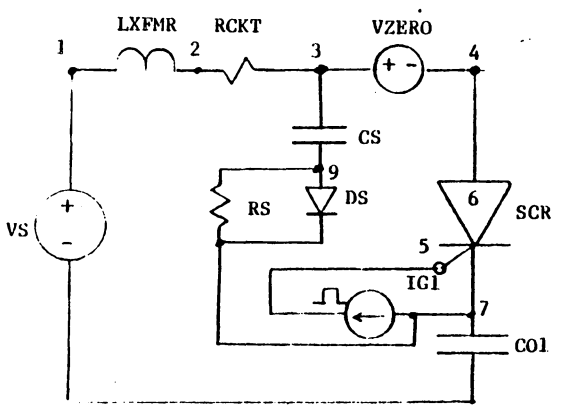


Figure 3.3 Single Loop Circuit with Snubber

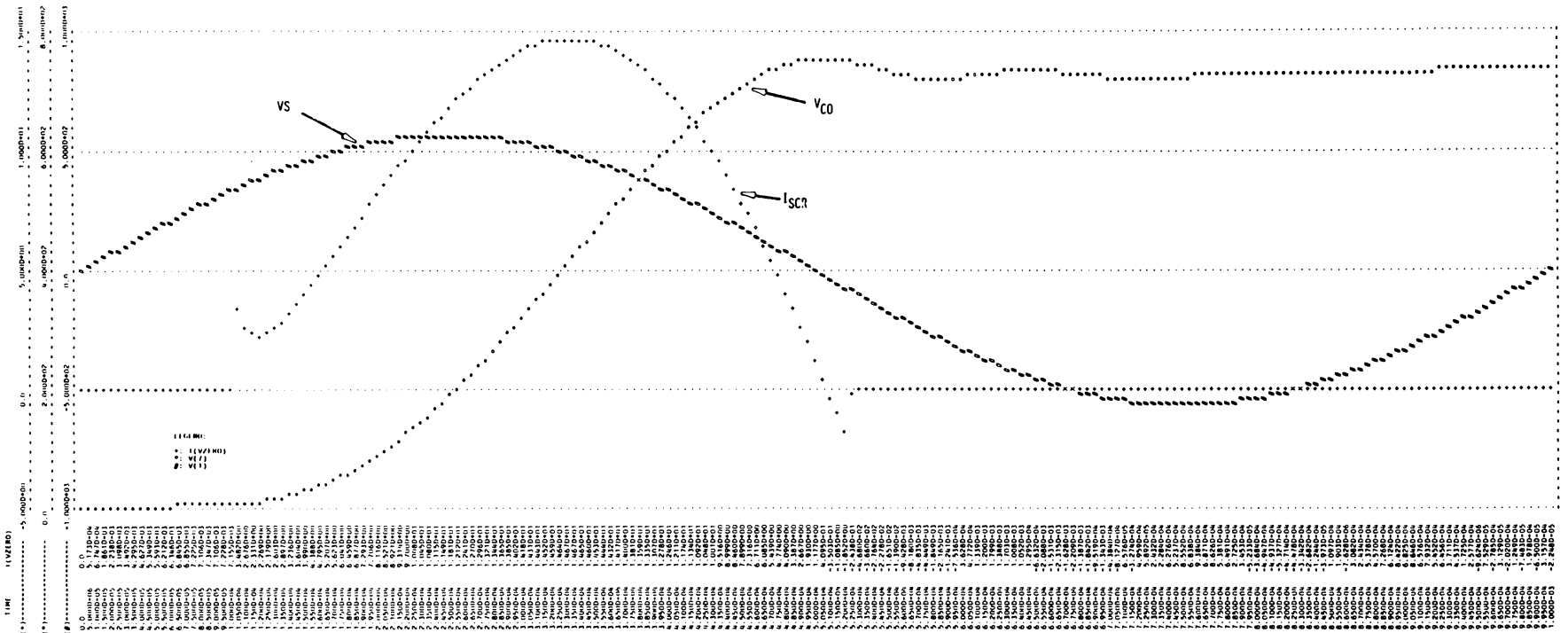


Figure 3.4 SPICE2 Simulation of Single Loop AC Resonant Circuit with a Snubber (Figure 3.3). The "Modified Hu-Ki Model" was used.

3.2 Summary and Conclusions

This chapter has examined the performance of the "modified Hu-Ki" model of the SCR in SPICE2 simulation of a basic LC resonant loop denoting an AC resonant charging circuit. The simulation employed a single phase control SCR, the GE C602 LM, as a controlled rectifer in the circuit.

Simulation results showed the model's capability of simulating the SCR's turn-off transient when subjected to sudden high amplitude anode to cathode terminal voltage reversal. A simulation of turn-off without a snubber showed the transient controlled by model internal time constants. Providing a snubber circuit resulted in a turn-off transient controlled by the snubber time constants.

CHAPTER 4

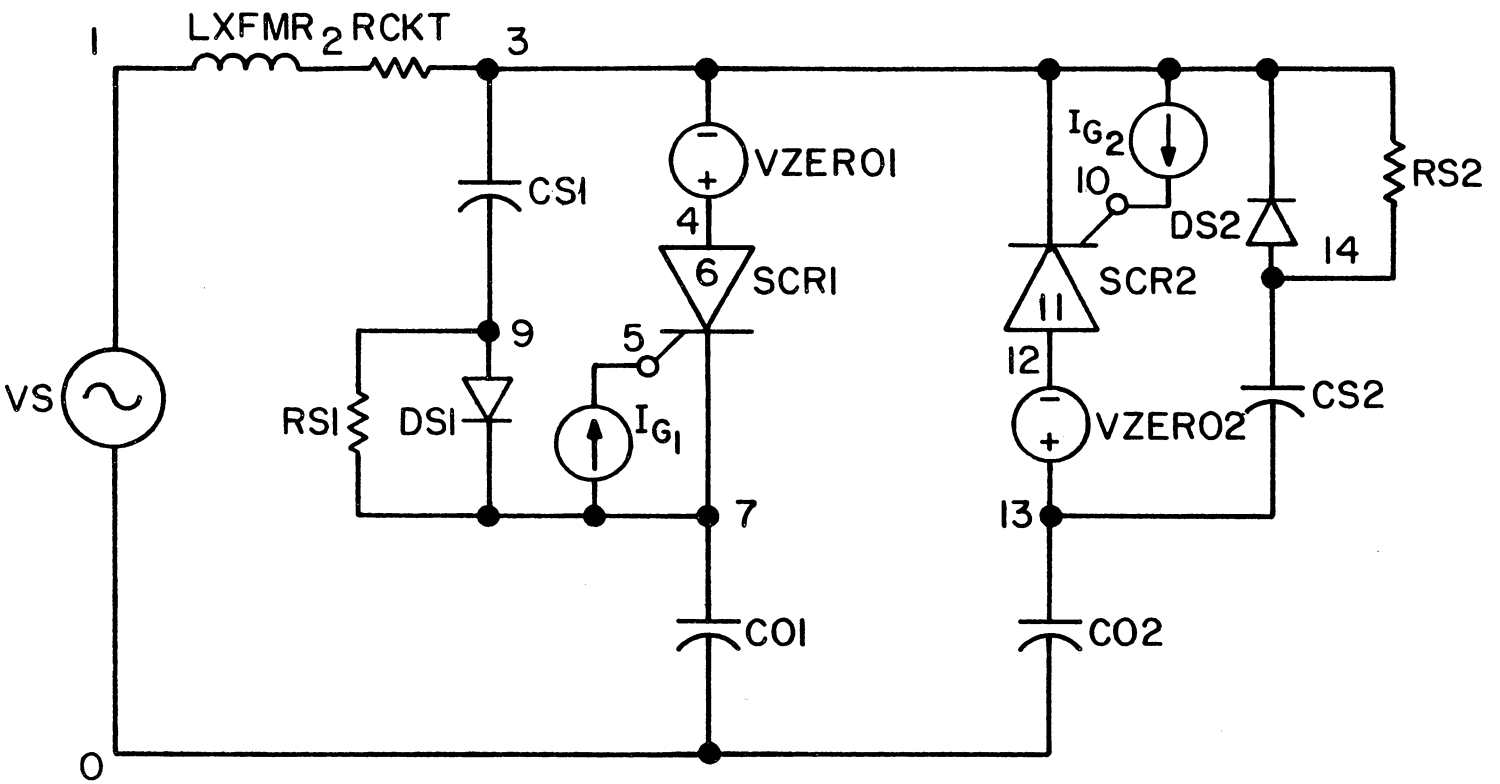
SPICE2 SIMULATION OF AC RESONANT CHARGING CIRCUITS HAVING TWO SCR'S

As was demonstrated in Chapter 3, the "modified Hu-Ki Model" provides an adequate tool for simulating single loop AC Resonant Charging Circuits with SPICE2. Chapter 4 presents additional verification of the models performance through simulation of three basic two-device AC Resonant Charging Circuits. They are: a two loop circuit, a single loop circuit with two SCR's in parallel, and a single loop circuit with two SCR's in series.

4.1 SPICE2 Simulation of a Two Loop AC Resonant Charging Circuit

A two loop AC Resonant Charging Circuit is shown in Fig. 4.1. The results of simulating this circuit without snubbers is shown in Fig. 4.3. As was indicated in section 3.1, the oscillatory behavior of the SCR turn-off transient in an inductive circuit can cause undesirable operation of some circuits. The two loop circuit is such a circuit. The second branch SCR is programmed (ref. Fig. 4.2) to receive a gate trigger pulse from IG1 at 600 μs. SCR2 begins conduction at 505 μs (95 μs prematurely). This occurs because the J_1 junction of SCR1 is supporting a rapidly rising reverse voltage which is seen by SCR2 as a rapidly rising forward voltage and therefore causes a dv/dt turn-on of SCR2.

The problem is corrected by adding snubber circuits. The desired operation is then obtained as is illustrated in Fig. 4.5.



**Refer to Figure 2.5 for the SPICE2 SCR Model Circuit Diagram.

*VZERO - A Zero Valued Voltage Source used as a Current Monitor in SPICE2 Programs.

Figure 4.1 The SPICE2 Circuit Diagram for the Two Loop AC Resonant Charging System.

```
GE C602 LM SCR - TWO BRANCH AC RES CHG'NG CKT - DESCRETE - NO SNUBBER

      INPUT LISTING                          TEMPERATURE =    27.000 DEG C

*******************************************************************************


VS 1 0 SIN(0 566 1K )
IG1 7 5 PULSE(0 1.0 100US 0 0 5US )
IG2 3 10 PULSE(0 1.0 600US 0 0 5US )
VZERO1 3 4 SIN(0 0 0)
VZERO2 13 12 SIN(0 0 0)
LXFMR 1 2 5MH
RCKT 2 3 5.0
Q1 5 6 4 QMOD1 OFF
Q2 6 5 7 QMOD2 OFF
Q3 10 11 12 QMOD1 OFF
Q4 11 10 3 QMOD2 OFF
DFOR1 5 6 DMOD1 OFF
DFOR2 10 11 DMOD1 OFF
DJCTN1 5 7 DMOD2 OFF
DJCTN2 10 3 DMOD2 OFF
RSHT1 5 7 9.375
RSHT2 10 3 9.375
C01 7 0 4UF
C02 0 13 4UF
.MODEL DMOD1 D(BV=2700,IS=5.58E-15)
.MODEL DMOD2 D(BV=5,IS=1.E-16)
.MODEL QMOD1 PNP(BF=9,BR=9,IS=1.0E-16.65,RE=.005,TF=17.8US,TR=1125US,CJE=4000PF)
.MODEL QMOD2 NPN(BF=9,IS=1.0E-16.65,CJC=4000PF)
.TRAN 5US 1000US
.PRINT TRAN I(VS) V(1) V(5,7) V(7,0) V(10,8) V(0,13) I(VZERO1) I(VZERO2)
.PLOT TRAN V(1) I(VZERO1) I(VZERO2)
.OPTIONS NOMOD NOPAGE LVLTIM=1 ITL5=10000 LIMPTS=10000
.END
```

Fig. 4.2. SPICE PROGRAM LISTING FOR CIRCUIT OF FIGURE 4.1 WITHOUT THE SNUBBER CIRCUITS. SIMULATION RESULTS ARE GIVEN IN FIG. 4.3.

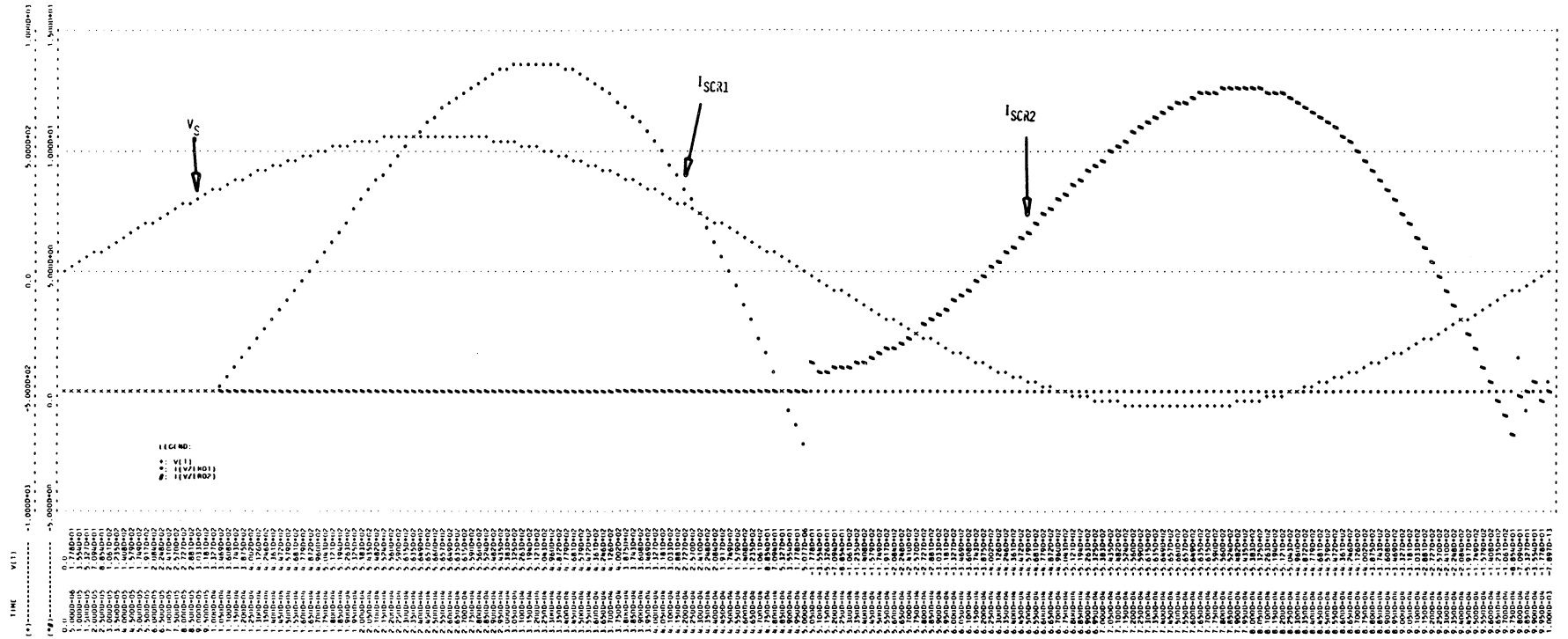


Figure 4.3 SPICE2 Simulation of a Two Loop AC Resonant Charging Circuit Without Snubber (Figure 4.1). NOTE: Conduction of SCR2 Starting at 505 Microseconds. Gate Signal is Not Applied Until 600 Microseconds.

```
GE C602 LM SCR - TWO BRANCH AC RES CHG'NG CKT - DESCRETE - WITH SNUBBER

     INPUT LISTING                          TEMPERATURE =    27.000 DEG C

******************************************************************************


VS 1 0 SIN(0 566 1K )
IG1 7 5 PULSE(0 1.0 100US 0 0 5US )
IG2 3 10 PULSE(0 1.0 600US 0 0 5US )
VZERO1 3 4 SIN(0 0 0)
VZERO2 13 12 SIN(0 0 0)
LXFMR 1 2 5MH
RCKT 2 3 5.0
Q1 5 6 4 QMOD1 OFF
Q2 6 5 7 QMOD2 OFF
Q3 10 11 12 QMOD1 OFF
Q4 11 10 3 QMOD2 OFF
DFOR1 5 6 DMOD1 OFF
DFOR2 10 11 DMOD1 OFF
RSHT1 5 7 9.375
RSHT2 10 3 9.375
DJCTN1 5 7 DMOD2 OFF
DJCTN2 10 3 DMOD2 OFF
C01 7 0 5UF
C02 0 13 5UF
CS1 9 3 0.1UF
RS1 7 9 15.
DS1 9 7 DMOD1
CS2 13 14 0.1UF
RS2 14 3 15
DS2 14 3 DMOD1
.MODEL DMOD1 D(BV=2700,5.58E-15)
.MODEL DMOD2 D(BV=5.,IS=1E-18)
.MODEL QMOD1 PNP(BF=9,BR=9,IS=1E-16.65,RE=.005,TF=17.8US,TR=1125US,CJE=4000PF)
.MODEL QMOD2 NPN(BF=9,IS=1E-16.65,CJC=4000PF)
.TRAN 5US 1000US
.PRINT TRAN V(1) I(VZERO1) I(VZERO2)
.PLOT TRAN V(1) I(VZERO1) I(VZERO2)
.OPTIONS NOMOD NOPAGE LVLTIM=1 ITL5=10000 LIMPTS=10000
.END
```

Fig. 4.4. SPICE2 PROGRAM LISTING FOR CIRCUIT OF FIG. 4.1 WITH SNUBBERS. SIMULATION RESULTS ARE SHOWN IN FIG. 4.5.

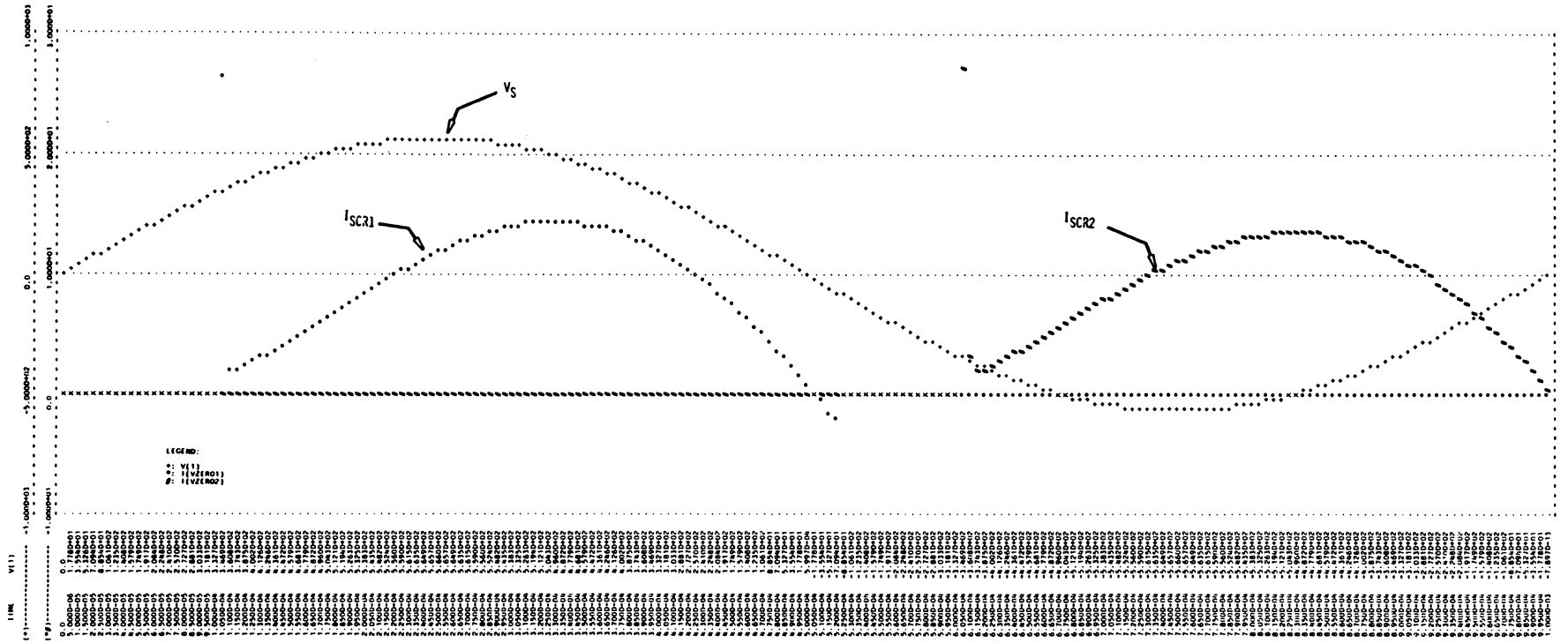


Figure 4.5 SPICE2 Simulation Results of a Two Loop AC Resonant Charging Circuit With Snubbers (Figure 4.1). NOTE: Conduction of SCR2 Starts at 600 Microseconds at the Time the Gate Pulse is Applied.

4.2 SPICE2 Simulation of a Single Loop AC Resonant Charging Circuit Using Two SCR's in Parallel

Figure 4.6 illustrates a basic circuit application of two SCR's in parallel. Such circuit applications occur when load current requirements exceed the current rating of the chosen SCR type.

Problems with using SCR's in parallel occur mainly due to slight differences in device characteristics among SCR's of the same type. This can result in one SCR turning on faster than the other. The corresponding principal voltage drop may then result in insufficient V_{AK} of the other device to insure turn on. This situation is illustrated in Fig. 4.8 for which SCR1 and SCR2 have been programmed (Fig. 4.7) to have slightly different parameters. In Fig. 4.8, it is seen that SCR2 (I(VZERO2)) begins to conduct more quickly than SCR1 (I(VZERO1)). Since the series balancing resistance (RSER) is essentially zero (actually .0001 ohms) then V_{AK} for SCR1 drops in correspondence with V_{AK} for SCR2. V_{AK} for SCR1 falls below the required value for turn on before SCR1 primary current reaches the holding current and therefore, the SCR1 does not turn on.

This situation may be prevented (although at a loss of efficiency) by inserting sufficient balancing resistance (RSER) in series with each SCR. This was done (ref. Fig. 4.9 - RSER1 = RSER2 = .5 ohms) and the results are given in Fig. 4.10. Both SCR's turn on since an increase in the current of one SCR causes an increase in the voltage drop across the other and a subsequent increase in its current.

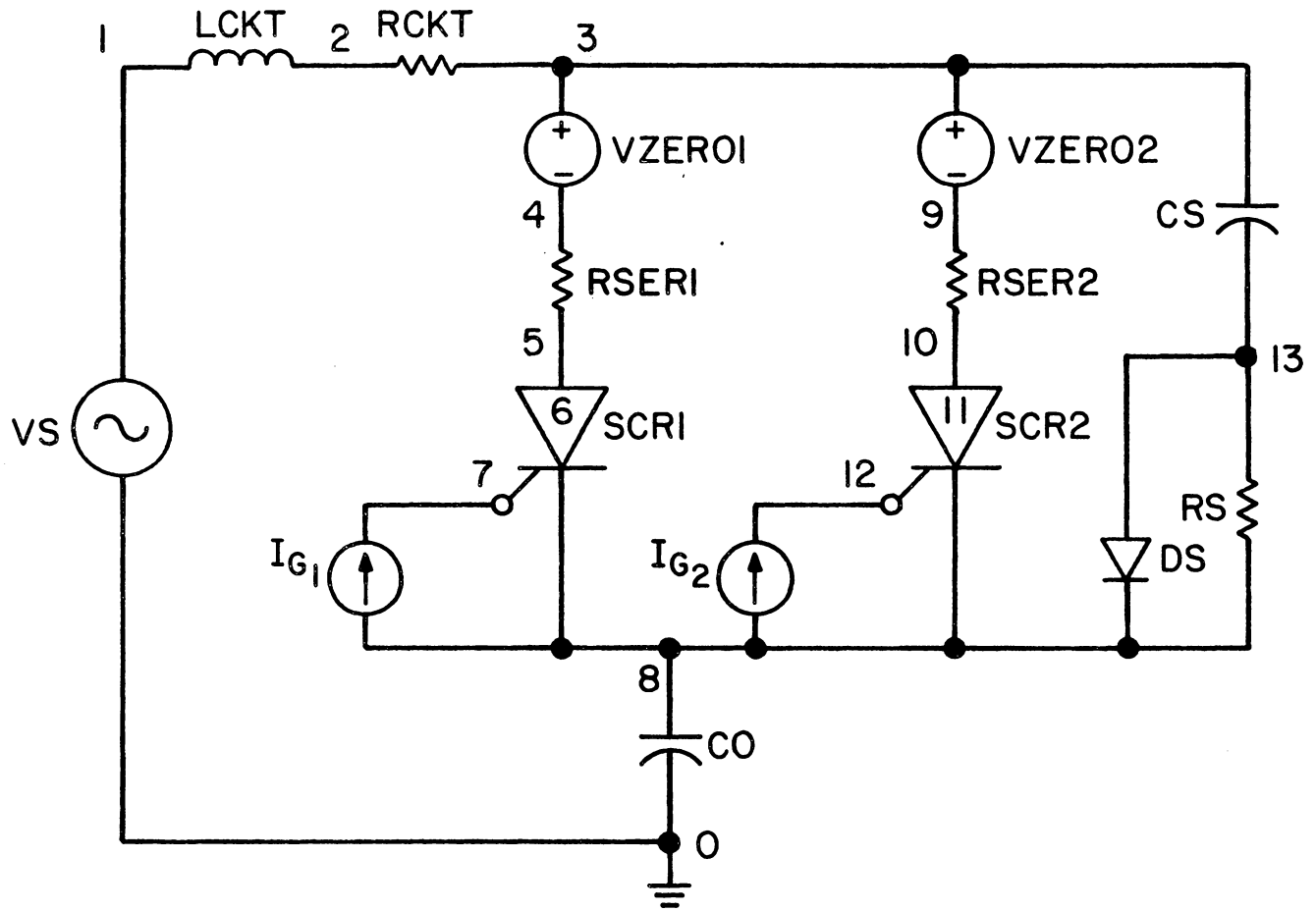


Figure 4.6 SPICE2 Circuit Diagram for Two SCR's in Parallel in a Single Loop AC Resonant Charging Circuit.

```
GE C602LM SCR - PARALLEL SCR SINGLE LOOP AC RES CH'GNG CKT

      INPUT LISTING                          TEMPERATURE =    27.000 DEG C

******************************************************************************


VS  1  0  SIN(0  566  1K )
VZERO1  3  4  SIN(0  0  0)
VZERO2  3  9  SIN(0  0  0)
IG1  6  7  PULSE(0  .099  100US  0  0  70US )
IG2  8  12  PULSE(0  .099  100US  0  0  70US)
LCKT  1  2  5MH
RCKT  2  3  5.0
RSER1  4  5  .0001
RSER2  9  10  .0001
RSHT1  7  6  9.375
RSHT2 12  8  9.375
RS  13  8  100
Q1  7  6  5  QMOD1  OFF
Q2  6  7  8  QMOD2  OFF
Q3  12  11  10  QMOD3  OFF
Q4  11  12  8  QMOD4  OFF
DFOR1  7  6  DMOD1  OFF
DJCTN1  7  8  DMOD2  OFF
DFOR2  12  11  DMOD1  OFF
DJCTN2  12  8  DMOD2  OFF
DS  13  8  DMOD1  OFF
CO1  8  0  5.00F
CS  3  13  .01UF
.MODEL  DMOD1  D(BV=2700,IS=5.56E-15)
.MODEL  DMOD2  D(BV=5  IS=1.0E-16)
.MODEL  QMOD1  PNP(BF=9,BR=9,IS=1.3E-16.65,RE=.005,TF=17.3US,TR=1125US,CJE=4000PF)
.MODEL  QMOD3  PNP(BF=9.1,BR=9,IS=1E-16.,RE=.0049,TF=16.805,TR=1125US,CJE=3000PF)
.MODEL  QMOD2  NPN(BF=9,IS=1E-16.65.,CJC=4000PF)
.MODEL  QMOD4  NPN(BF=9.2,IS=1E-16,CJC=4000PF)
.TRAN  5US  100US
.PRINT  TRAN  I(VZERO1)  I(VZERO2)  V(8,0)  V(1,0)
.PLOT  TRAN  I(VZERO1)  I(VZERO2)  V(8,0)  V(1,0)
.OPTIONS  NOMOD NOPAGE  LVLTIM=1  ITL5=10000  LIMPTS=10000
.END
```

Fig. 4.7. SPICE2 LISTING FOR CIRCUIT OF FIG. 4.6 WITH RSER1 = RSER2 = .0001 OHMS. SIMULATION RESULTS ARE SHOWN IN FIG. 4.8.

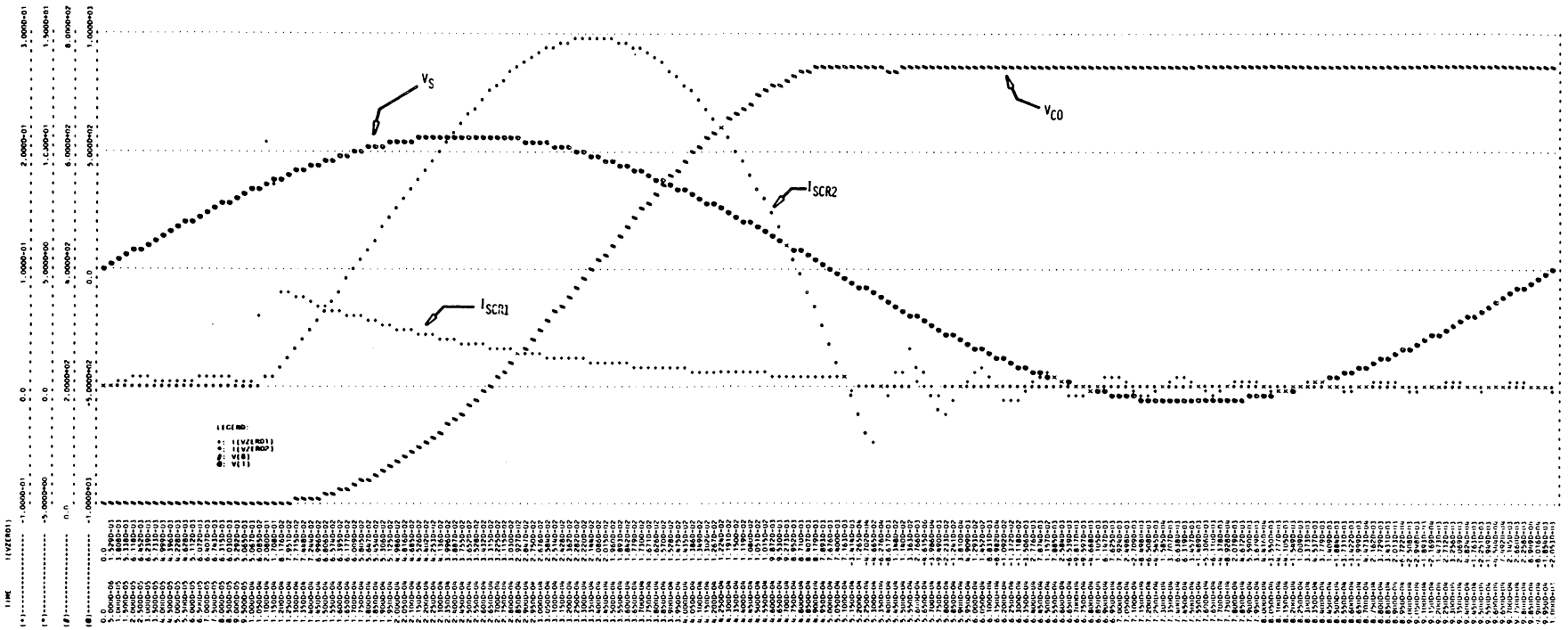


Figure 4.8 SPICE2 Simulation of a Single Loop AC Resonant Charging Circuit Using Two Parallel SCR's (Figure 4.6). NOTE: For Insufficient Series Balancing Resistance (RSER) One SCR2 Turns on Faster With the Result that SCR1 Fails to Turn on.

```
GE C602LM SCR - PARALLEL SCR SINGLE LOOP AC RES CH'CNG CKT

      INPUT LISTING                              TEMPERATURE =    27.000 DEG C

*******************************************************************************


VS 1 0 SIN(0 566 1K )
VZERO1 3 4 SIN(0 0 0)
VZERO2 3 9 SIN(0 0 0)
IG1 8 7 PULSE(0 .099 100US 0 0 70US )
IG2 8 12 PULSE(0 .099 100US 0 0 70US)
LCKT 1 2 5MH
RCKT 2 3 5.0
RSER1 4 5 .5
RSER2 9 10 .5
RSHT1 7 8 9.375
RSHT2 12 8 9.375
RS 13 8 100
Q1 7 6 5 QMOD1 OFF
Q2 6 7 8 QMOD2 OFF
Q3 12 11 10 QMOD3 OFF
Q4 11 12 8 QMOD4 OFF
DFOR1 7 6 DMOD1 OFF
DJCTN1 7 6 DMOD2 OFF
DFOR2 12 11 DMOD1 OFF
DJCTN2 12 8 DMOD2 OFF
DS 13 8 DMOD1 OFF
CO1 8 0 5.00F
CS 3 13 .01UF
.MODEL DMOD1 D(BV=2700,IS=5.59E-15)
.MODEL DMOD2 D(BV=5 IS=1.0E-16)
.MODEL QMOD1 PNP(BF=9,BR=9,IS=1.0E-16.65,RE=.005,TF=17.8US,TR=1125US,CJE=4000PF)
.MODEL QMOD3 PNP(BF=9.1,BR=9,IS=1E-16.,RE=.0049,TF=16.3US,TR=1125US,CJE=3000PF)
.MODEL QMOD2 NPN(BF=9,IS=1E-16.65.,CJC=4000PF)
.MODEL QMOD4 NPN(BF=9.2,IS=1E-16,CJC=4000PF)
.TRAN 5US 1000US
.PRINT TRAN I(VZERO1) I(VZERO2) V(8,0) V(1,0)
.PLOT TRAN I(VZERO1) I(VZERO2) V(8,0) V(1,0)
.OPTIONS NOMOD NOPAGE LVLTIM=1 ITL5=10000 LIMPTS=10000
.END
```

Fig. 4.9. SPICE2 LISTING FOR CIRCUIT OF FIG. 4.6 WITH RSER1 = RSER2 = .5 OHMS. SIMULATION RESULTS ARE SHOWN IN FIG. 4.10.

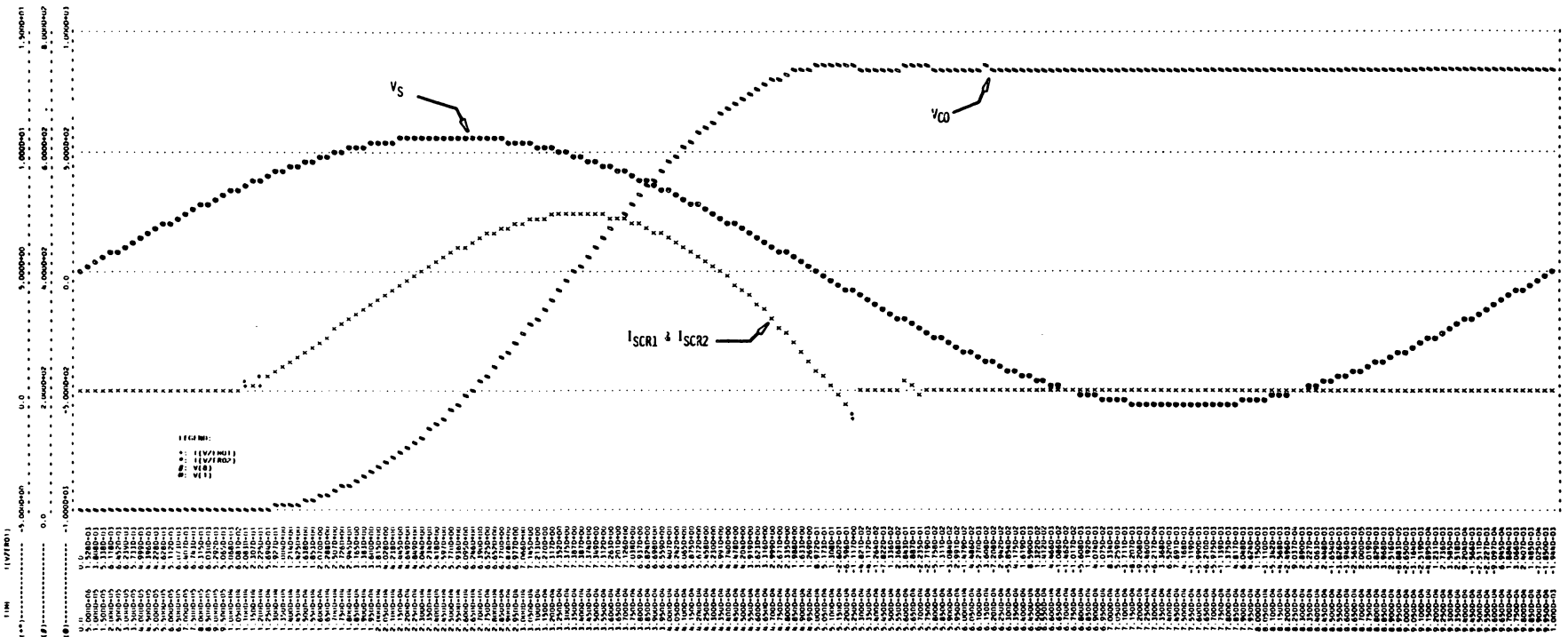


Figure 4.10 SPICE2 Simulation of a Single Loop AC Resonant Charging Circuit Using Two Parallel SCR's (Figure 4.6). NOTE: Series Balancing Resistors (RSER) are of Sufficient Value to Insure Turn-on of Both SCR's.

4.3 SPICE2 Simulation of a Single Loop AC Resonant Charging Circuit Using Two SCR's in Series

Sometimes circuit applications call for SCR's to block voltages which exceed the blocking voltage rating of the device (either forward or reverse). Such an application is illustrated in the AC Resonant Charging Circuit of Fig. 4.11 where the reverse voltage to be blocked may be as high as three times the forward voltage of 1000V peak. The GE C602 LM SCR which has a blocking voltage rating of only 2700V may not be able to block the peak reverse voltage of this circuit which might reach 3000V. To insure adequate blocking, two GE C602 LM SCR's are connected in series as shown in Fig. 4.11.

As in the case of parallel SCR's, slight variations in device characteristics may cause problems in circuit operation. In this case primary concern is to insure sharing of the voltage to be blocked in such a manner as to avoid exceeding the rating of either SCR. For this purpose, the balancing network composed of RBAL1, RBAL2, for forward balancing and CS1, CS2, RS1, and RS2, for reverse balancing is provided. Notice that the reverse balancing network provides a snubber system in the forward direction.

Simulation results for the circuit of Fig. 4.11 are shown in Fig. 4.12. Prior to application of the gate trigger at 100 μs both SCR's carry very nearly equal voltages (V(4,7) and V(9,12) in Fig. 4.12). During the on period (100 μs to 505 μs), V_{AK} for both SCR's is a very low forward value. At the start of commutation (505 μs) the charge stored in each SCR differs due to slight parameter

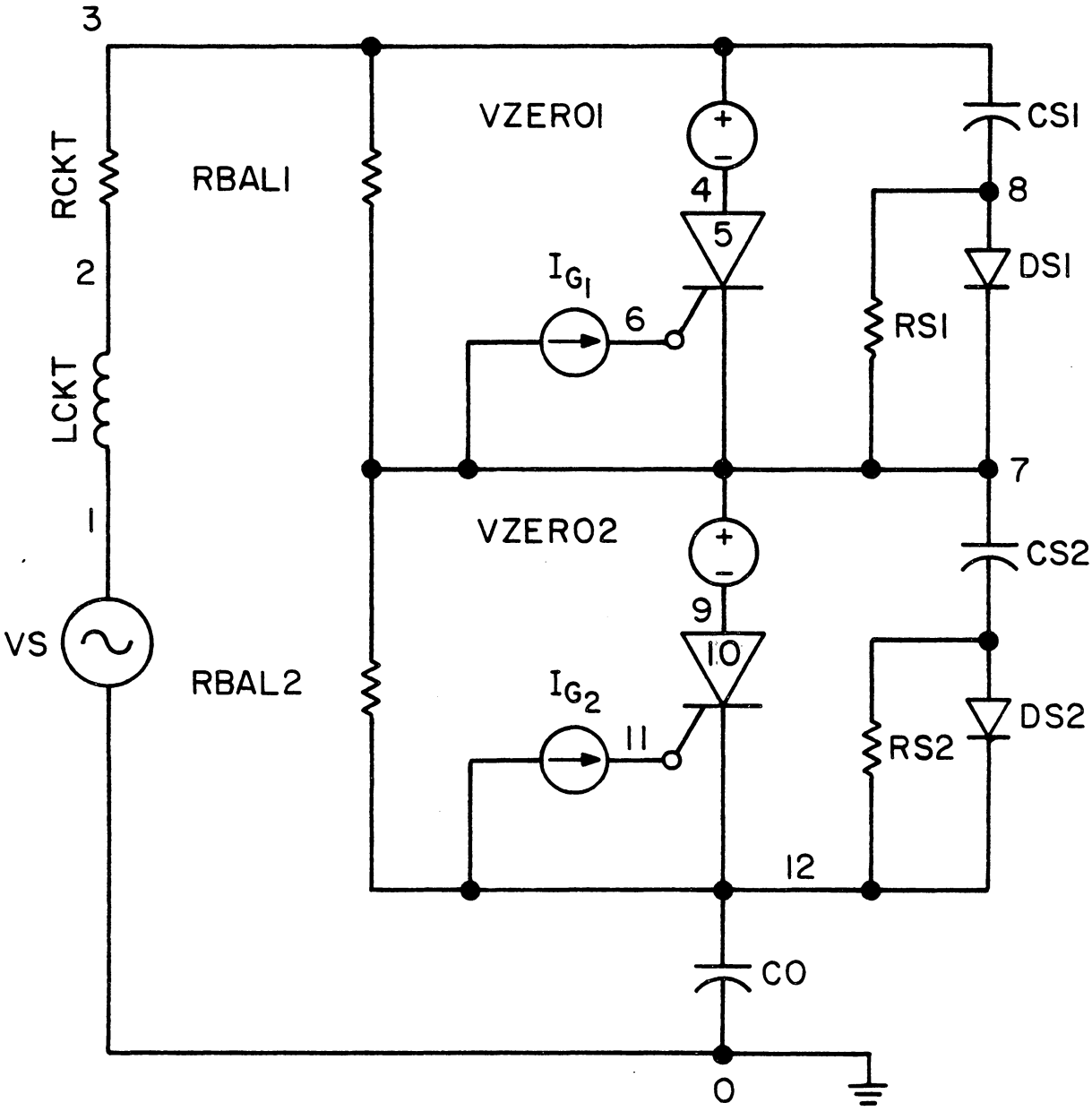


Figure 4.11 (a) SPICE2 Circuit Diagram for a Single Loop AC Resonant Circuit Having Two SCRs in Series.

```
GE C602LM SCR - 2 SERIES SCR'S IN SINGLE LOOP AC CKT

     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


VS 1 0 SIN(0 1000 1K )
IG1 7 6 PULSE(0 1.0 100US 0 0 50S )
IG2 12 11 PULSE(0 1.0 100US 0 0 50S )
VZERO1 5 4 SIN(0 0 0)
VZERO2 7 9 SIN(0 0 0)
LCKT 1 2 5MH
RCKT 2 3 5.0
Q1 6 5 4 QMOD1 OFF
Q2 5 6 7 QMOD2 OFF
Q3 11 10 9 QMOD3 OFF
Q4 10 11 12 QMOD4 OFF
DFOR1 6 5 DMOD1 OFF
DFOR2 11 10 DMOD1 OFF
RSHT1 6 7 9.375
RSHT2 11 12 9.375
RBAL1 3 7 17.14K
RBAL2 7 12 17.14K
DJCTN1 6 7 DMOD2 OFF
DJCTN2 11 12 DMOD2 OFF
CG1 12 0 50F
CS1 3 8 0.1UF
RS1 7 8 100.
DS1 8 7 DMOD1
CS2 13 7 0.1UF
RS2 12 13 100
DS2 13 12 DMOD1
.MODEL DMOD1 D(BV=2700,IS=15.58E-15)
.MODEL DMOD2 D(BV=5.,IS=1E-16)
.MODEL QMOD1 PNP(BF=9,BR=9,IS=1E-16.65,RE=.005,TF=17.8US,TR=1125US,CJE=4000PF)
.MODEL QMOD2 NPN(BF=9,IS=1E-16.65,CJC=4000PF)
.MODEL QMOD3 PNP(BF=9.1,BR=9,IS=1E-16.6,RE=.006,TF=17.0S,TR=1120US,CJE=3900PF)
.MODEL QMOD4 NPN(BF=9.1,IS=1E-16.6,CJC=3900PF)
.TRAN 50S 10000S
.PRINT TRAN I(VS) V(1) V(4,7) V(9,12) V(12,0)
.PLOT TRAN V(1) I(VS) V(4,7) V(9,12)
.OPTIONS NOMOD NOPAGE LVLTIM=1 ITL5=10000 LIMPTS=10000
.END
```

Figure 4.11 (b) SPICE2 Program Listing for the Circuit Diagram for Figure 4.11 (a).

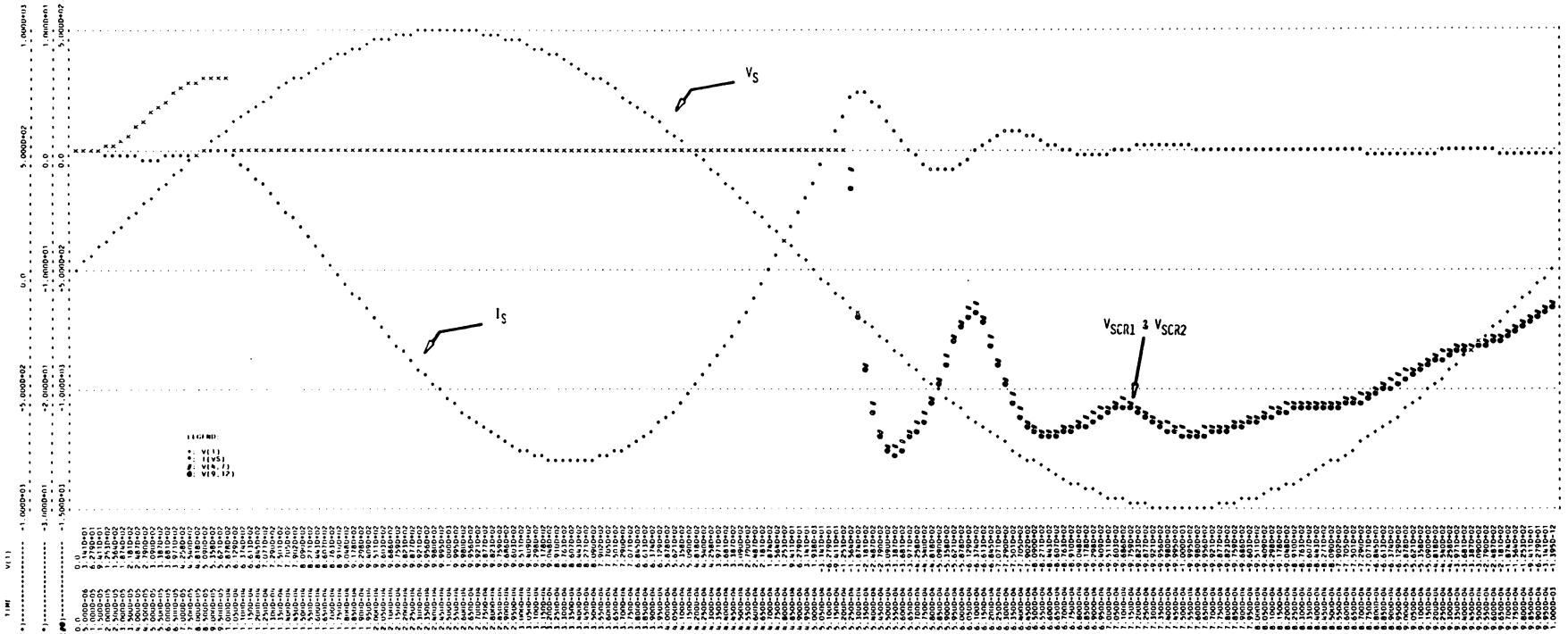


Figure 4.12 SPICE2 Simulation Results for Single Loop AC Resonant Circuit With Two SCR's in Series (Figure 4.11).

variations. As a result, the charge transferred to the two equal valued capacitors in the reverse voltage balancing network is different. The resulting unbalance in the reverse voltages is seen in the V(4,7) and V(9,12) curves in Fig. 4.12.

4.4 Summary and Conclusions

This chapter has covered phase-control-SCR-circuit simulations demonstrating the "modified Hu-Ki" model's ability to provide visibility of the interaction between two SCRs during switching transients.

First, two SCRs, one acting as a switch for each half cycle of the AC source, were incorporated into a two-loop AC resonant charging circuit. Initial simulation was without snubbers. Voltage transients during SCR commutation in resonant charging circuits may be very sharp with sustained high amplitudes. Results showed the SCR model capable of simulating a dV/dt turn-on by the SCR in the second loop due to the steep voltage transient occurring during commutation of the SCR in the first loop. Snubbers were shown to correct the circuit problem.

For the next two demonstrations, the model parameters for two GE C602 LM SCRs were perturbed differently within the 25% range of variation characteristic of this popular SCR type. The two SCR models were then used to simulate a turn-on transient for two SCRs in parallel. Results showed an accurate prediction that one

device turning on faster than the other would result in current hogging by the leading device and subsequent failure of the other device to turn on. Inclusion of resistive balasting in the simulation resulted in both devices turning on.

The final demonstration in this chapter used the two perturbed SCR models in a series configuration. Unbalanced turn-off behavior was demonstrated in a properly designed compensating network.

Having demonstrated the "modified Hu-ki" SCR models capability to provide SPICE2 simulation of several transient phenomena peculiar to SCR circuits, it is concluded that this SPICE2 model is a valuable CAD tool providing a continuous topology transient analysis capability not previously available to the circuit designer.

It is now time to turn attention to expanding this capability to a more general purpose posture. From the perspective of the power electronics circuit analyst, SPICE2 is a rather limited program when treating the large signal non-linearities of power processing circuits. Magnetic saturation effects are an example of these concerns. While SPICE2 is unable to model such non-linearities, SCEPTRE is. This thesis does not treat magnetic non-linearities, but, is aimed at providing an SCR modeling capability in a computational environment which can treat them.

On to SCEPTRE!

CHAPTER 5

The SCR Model in SCEPTRE

Chapters one through four give extensive treatment to transistor model configurations and the development of a two transistor SCR model for application with SPICE2. SPICE2 is a fast, efficient, user oriented circuit analysis program; however, SCEPTRE provides additional versatility for non-linear network simulation through its subprogram capabilities. Also, SPICE2 has built in models for transistors and diodes. The SCR model in SPICE2 was constructed to the constraints of those models. SCEPTRE does not have built in models, but it does have programming constraints which should be observed to effect good efficient modeling. To achieve the expanded versatility of SCEPTRE, the SPICE2 SCR model is reconfigured to a SCEPTRE SCR Model. The "modified Hu-ki" parameter determination technique for SPICE2 is adapted for use with this SCEPTRE SCR Model.

5.1 Reconfiguration of the SPICE2 SCR Model into a SCEPTRE SCR Model.

As mentioned previously SCEPTRE, while having no built in model constraints, does have programming constraints to which modeling must adhere. The constraints of particular importance in converting the SPICE2 SCR Model configuration to a SCEPTRE SCR Model configuration are as follows.

1. Semiconductor PN junctions should be modeled as primary dependent current sources using the DIODE EQUATION special value expression of the SCEPTRE input format.
2. Primary dependent current sources should have a capacitor in parallel so that the independent variable, capacitor voltage, will be

a state variable.

3. All capacitors inserted in the model to satisfy 2 should be as large as possible to avoid unnecessarily small time steps.

4. Injected, collected, or breakdown currents should be modeled as secondary dependent current sources as defined in the SCEPTRE input format.

Constraints 1 through 4 result in a substantially larger equivalent circuit network for the SCR Model in SCEPTRE than for the model in SPICE2.

Figure 5.1 illustrates the first step in developing the SCR model configuration for SCEPTRE. Two transistor models, a PNP and a NPN, are connected in a regenerative feedback configuration to effect the SCR switching action. In order to satisfy the programming constraints 1 through 4 , the transistor model is the injection configuration of the modified Ebers-Moll model discussed in chapter 1.[6][10] For the NPN transistor, the PN junction represented by I_F must be modeled as a primary dependent current source and therefore must have a capacitor in parallel. For this reason, C_{BE} of the npn transistor may not be neglected as it was in the SCR Model for SPICE2. Also, the PNP transistor model is shown with a non-zero emitter resistance, R_E, used to model the on state resistance of the SCR.

Fig. 5.2 shows the addition of I_{DFOR} to model the diode DFOR of the SPICE2 SCR Model and R_{shunt} to correspond to R_{shunt}. Now, additional elements must be added to complete a SCEPTRE SCR Model.

Fig. 5.3 shows these additional elements. I_{DFOR} reflects the diode DFOR's (of the SPICE2 Model) forward conducting characteristics, but provides no reverse breakdown simulation capability. Therefore, to simulate SCR high-voltage break-over in SCEPTRE, the secondary dependent

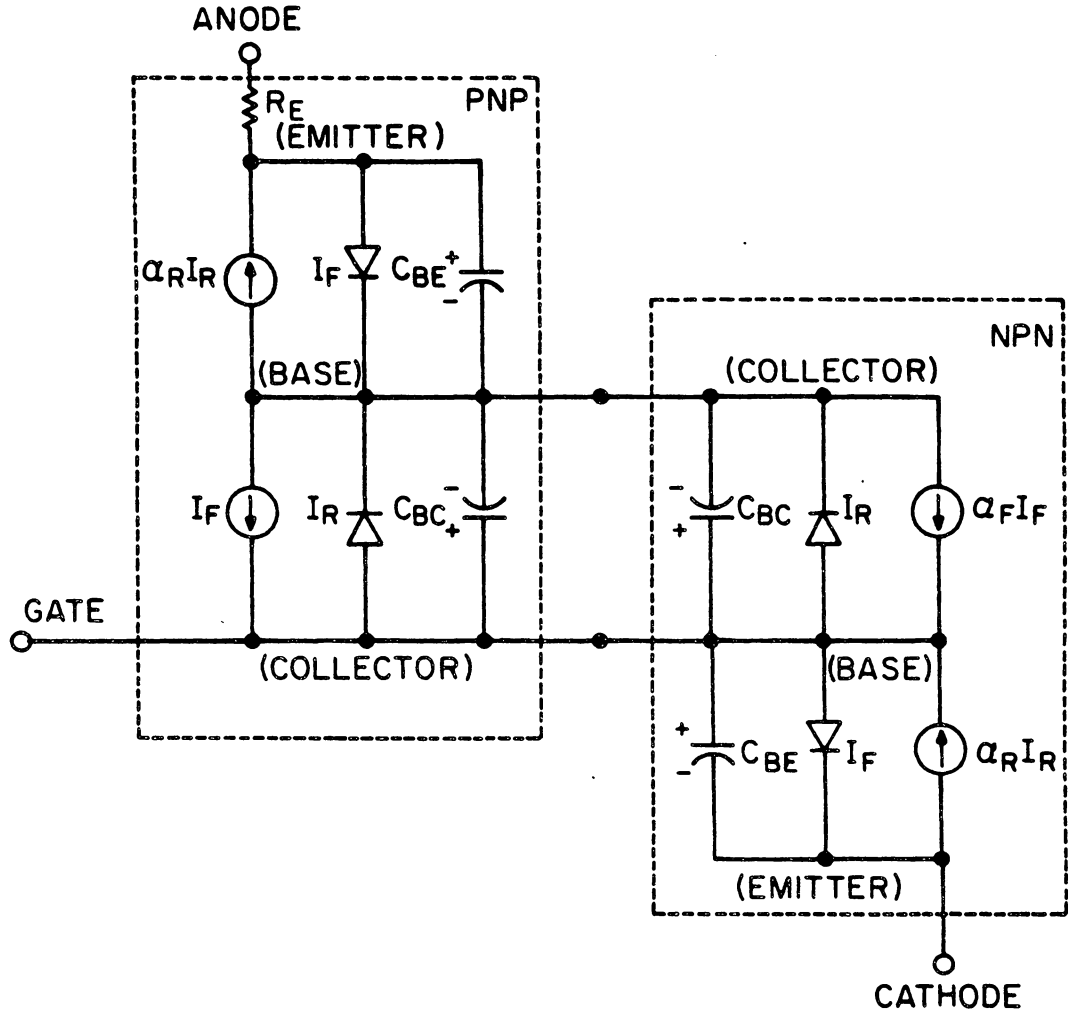


Fig. 5.1. SCEPTRE TWO BJT SCR MODEL USING "INJECTION" VERSION OF THE "MODIFIED" EBERS-MOLL BJT MODEL.

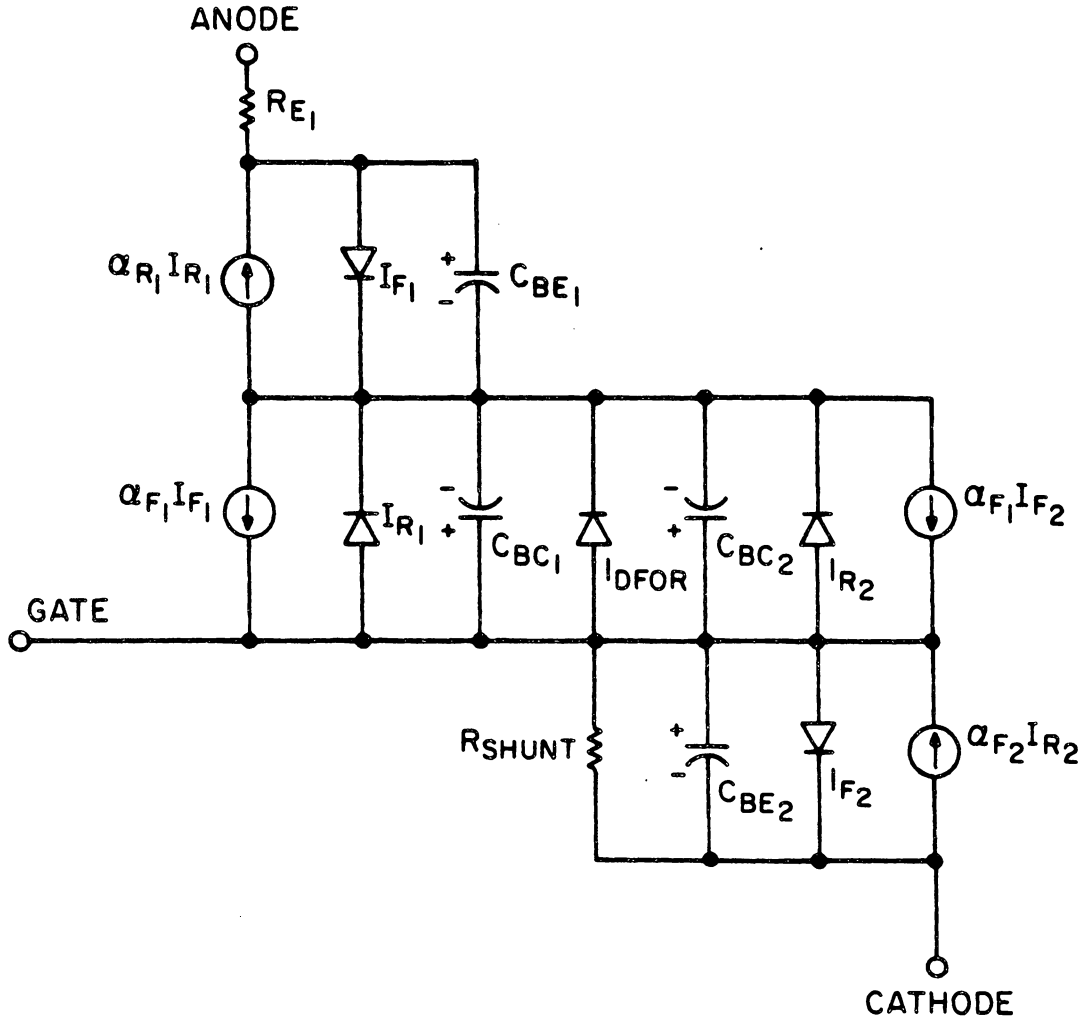


Fig. 5.2. DIRECT CONVERSION OF THE SPICE2 MODEL NETWORK TO SCEPTRE MODEL NETWORK.

current source I_{BD_C} is added to the model. To simulate the reverse breakdown of the gate to cathode junction during turn-off, I_{BD_K} is used instead of D_{JCTN1} of the SPICE2 SCR Model. The SCEPTRE SCR Model is functionally complete at this point; however, to avoid computational delays, RA and RC are high value resistors added to meet SCEPTRE programming requirements.

When programming in SCEPTRE, model element names should be as short as practical to allow maximum flexibility in the main circuit description. The SCEPTRE SCR model network is shown in Figure 5.4, with resistors, capacitors, and primary dependent current sources assigned appropriate designators for SCEPTRE input format. The secondary dependent current sources are shown as functions of the primary dependent current sources. Fig. 5.5 shows all of the model elements designated by their SCEPTRE input format designator. SCEPTRE Model description node assignments are indicated in parenthesis.

The circuit of Fig. 5.3 is unnecessarily complicated. A reduction of the circuit size is made to result in Fig. 5.4. The reduction made results in a change from the 2-transistor configuration to what is called the 3-Junction Model. As seen in Figure 5.4, there are only three PN junctions modeled by primary dependent current sources JA, JC, and JK. It is felt that this representation more closely illustrates the true physical construction of an SCR.

The circuit reduction is accomplished by the following. Diodes (primary dependent current sources) I_{R_1}, I_{DFOR}, and I_{R_2} of Figure 5.3 are lumped together as a single diode, JC, in figure 5.4. Capacitors, C_{BC_1} and C_{BC_2} of Figure 5.3 are lumped together as a single capacitor, CC of Figure 5.4.

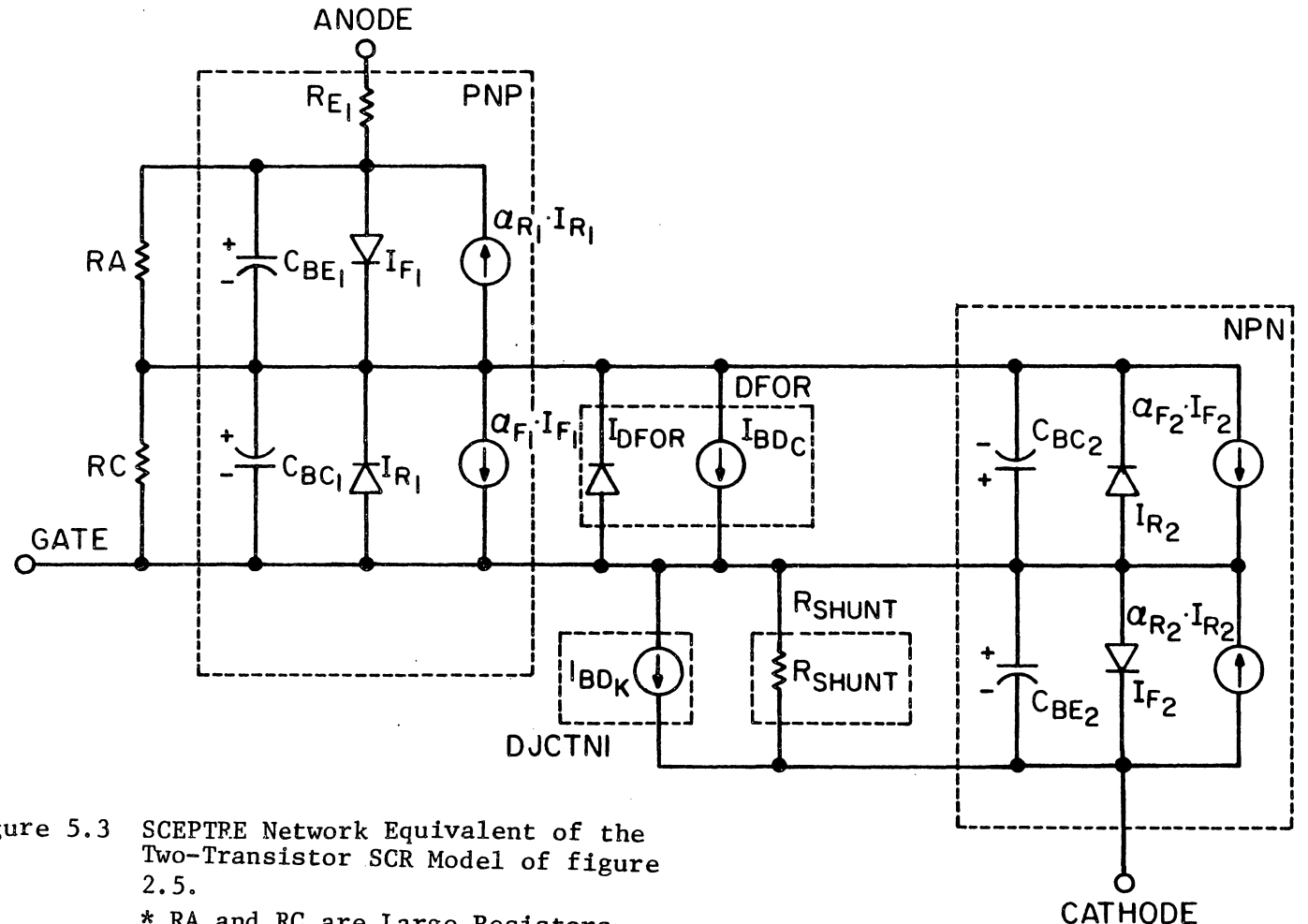


Figure 5.3 SCEPTRE Network Equivalent of the Two-Transistor SCR Model of figure 2.5.

* RA and RC are Large Resistors Added to Meet Programming Requirements Only.

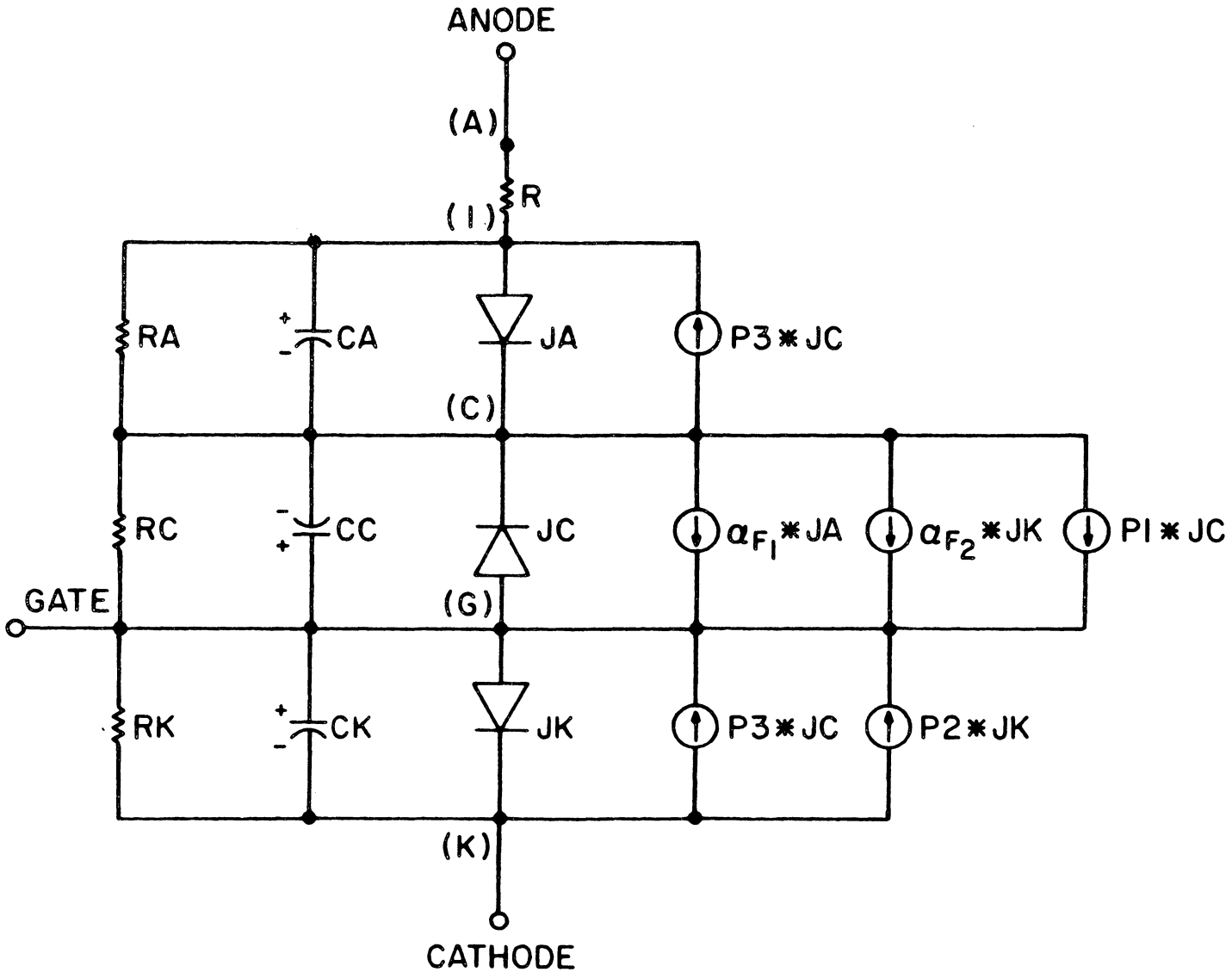


Fig. 5.4. THE SCEPTRE 3-JUNCTION SCR MODEL NETWORK REPRESENTATION with elements defined according to SCEPTRE element name.
* (x) denotes network node designation assigned for SCEPTRE INPUT DATA.

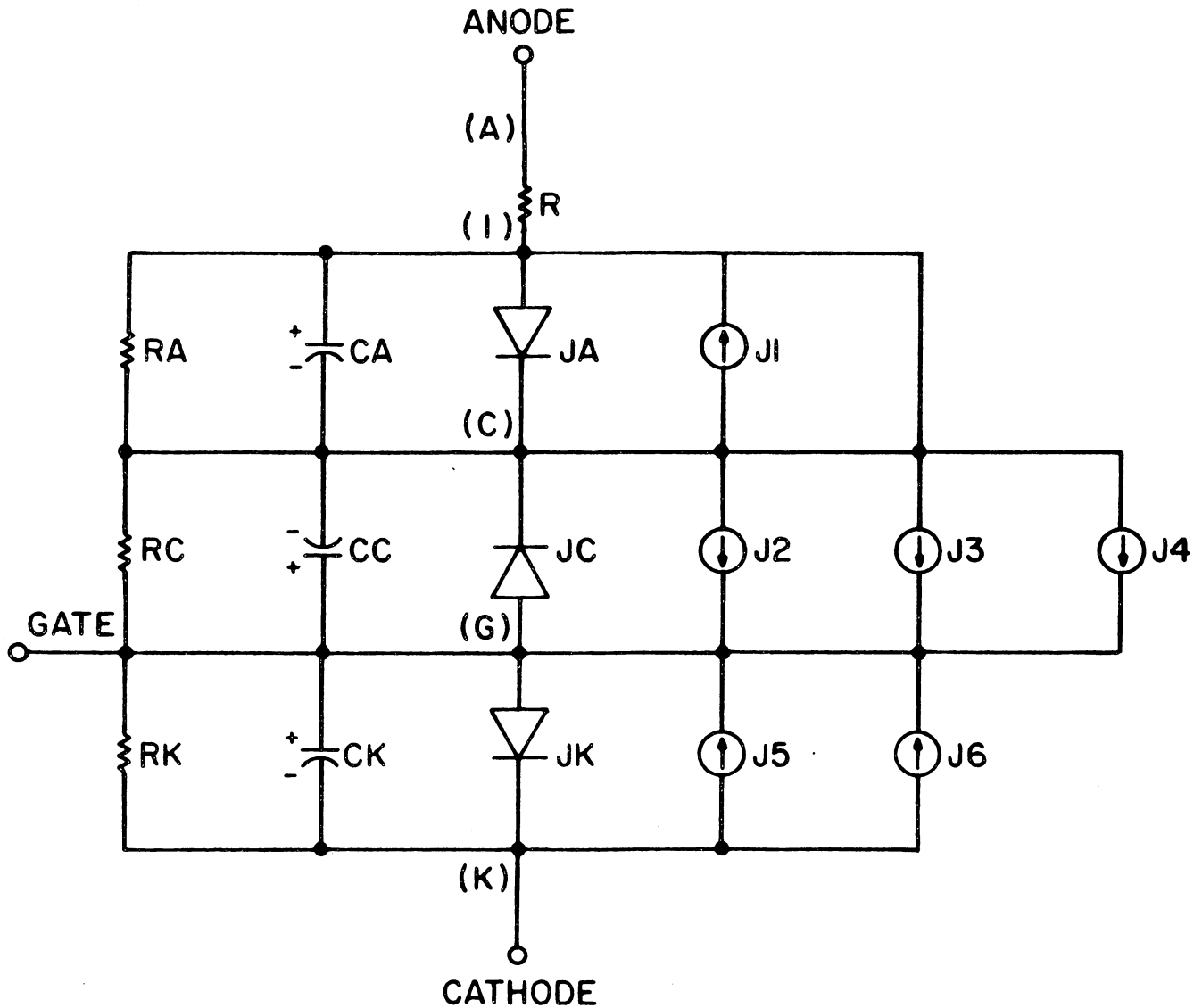


Fig. 5.5. THE SCEPTRE 3-JUNCTION SCR MODEL NETWORK REPRESENTATION with elements defined for SCEPTRE input format.

Necessarily, all the secondary dependent current sources and non-linear capacitors dependent upon the three primary current sources of figure 5.3 must have parameter corrections to insure appropriate dependence on the single primary dependent current source, JC, of figure 5.4. The appropriate parameter determination technique for this SCEPTRE 3-Junction SCR Model is given in section 5.2.

Table 5.1 gives the cross-correlation between the circuit elements of figures 5.3, 5.4, and 5.5.

When simulating SCR circuits, the SCR's are usually protected from transients by snubber circuits. To simplify programming circuits having more than one SCR with identical snubber circuit, the snubber may be included in the model description as shown in figure 5.6 by the elements CD, JD, RS, and CS connected by dotted lines. Determination of snubber element parameters is a part of the circuit design and is not discussed in this report.

Table 5.2 lists all the elements of the SCEPTRE 3-Junction SCR Model of figure 5.5 with optional snubber. The elements are listed in appropriate SCEPTRE input format, and are defined in generalized parameters. The method of computing these generalized parameters is discussed in section 5.2.

5.2 Determination of parameters for the SCEPTRE 3-Junction SCR Model.

The procedure for determining parameters for the SCEPTRE 3-Junction SCR Model of figure 5.6 is an adaptation of the "Modified Hu-ki" procedure used for determining parameters for the SPICE2 2-Transistor SCR Model discussed in chapters 1, 2, 3, & 4 of this report. The adaptation consists primarily of adjusting SPICE2 model parameters to reflect the reconfiguration

Table 5.1

SYMBOL CONVERSION CHART

FIG 5.3	FIG 5.4	FIG 5.5
R_{E_1}	R	R
$\alpha_{R_1} I_{R_1}$	P3 * JC	J1
I_{f_1}	JA	JA
C_{BE_1}	CA	CA
RA	RA	RA
$\alpha_{f_1} I_{f_1}$	α_{f_1} * JA	J2
$I_{R_1}+I_{DFOR}+I_{R_2}$	JC	JC
$C_{BC_1}+C_{BC_2}$	CC	CC
$\alpha_{f_2} I_{f_2}$	α_{f_2} * JK	J3
I_{BD_C}	P1 * JC	J4
RC	RC	RC
R_{Shunt}	RK	RK
C_{BE_2}	CK	CK
I_{f_2}	JK	JK
$\alpha_{R_2} I_{R_2}$	P3 * JC	J5
I_{BD_K}	P2 * JK	J6

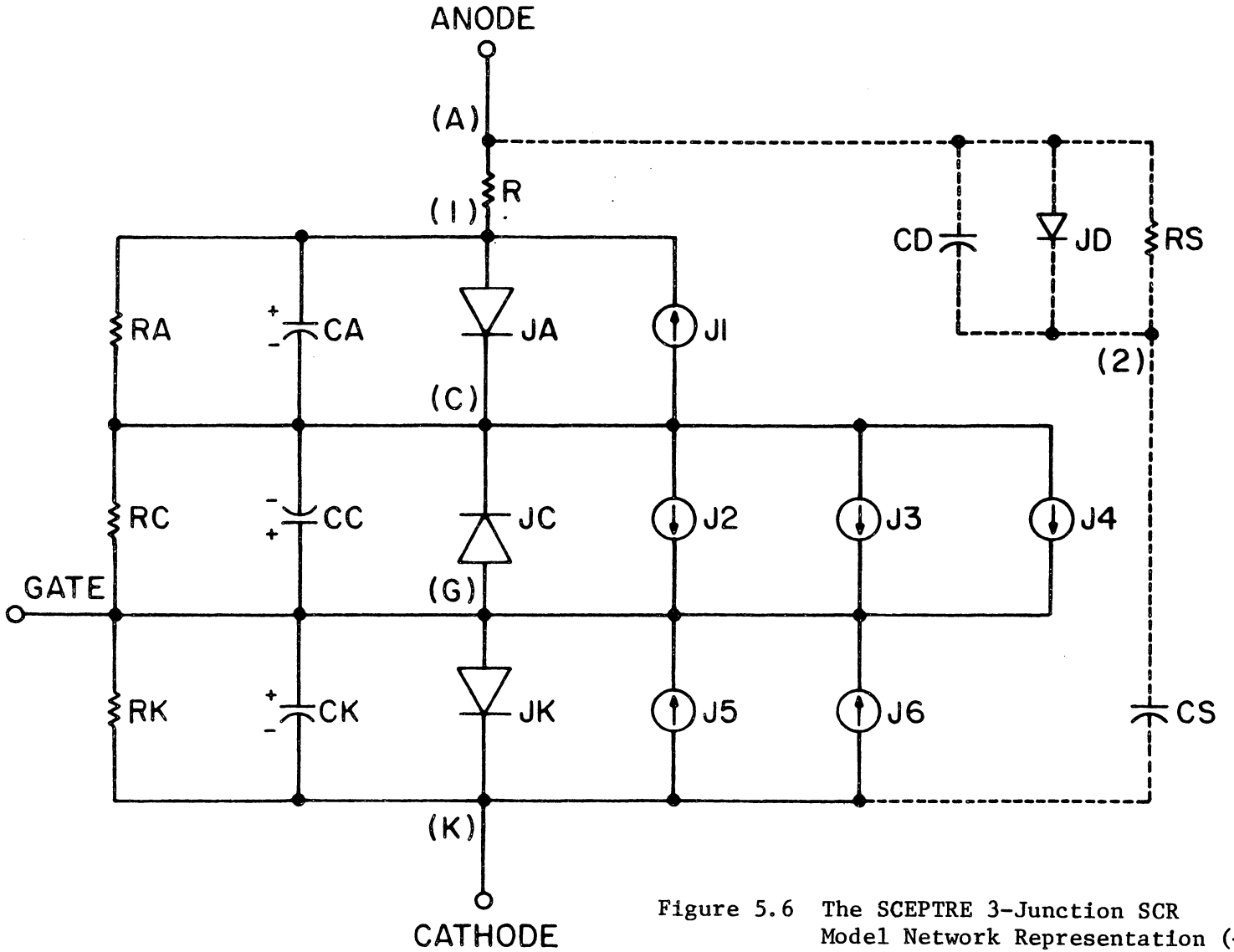


Figure 5.6 The SCEPTRE 3-Junction SCR Model Network Representation (—) With Optional Snubber (---).

Table 5.2

SCEPTRE SCR MODEL CIRCUIT ELEMENT DESCRIPTION
FOR THE 3-JUNCTION MODEL OF FIG. 5.6

RESISTORS

R,A-1 = R
RA,1-C = 1.D6
RC,C-6 = 1.D6
RK,G-K = RK

PRIMARY DEPENDENT SOURCES (PN JUNCTIONS)

JA ,1-C = DIODE Q(I_{AS},θ)
JC ,G-C = DIODE Q(I_{CS},θ)
JK ,G-K = DIODE Q(I_{KS},θ)

SECONDARY DEPENDENT SOURCES (COLLECTED CURRENTS & REVERSE BREAKDOWN CURRENTS)

J1 ,C-1 = P3 * JC
J2 ,C-G = α_{f_1} * JA
J3 ,C-G = α_{f_2} * JK
J4 ,C-G = P1 * JC
J5 ,K-G = P3 * JC
J6 ,K-G = P2 * JK

CAPACITANCES (JUNCTION DEPLETION LAYER AND NEUTRAL REGION EXCESS CHARGE STORAGE [DIFFUSION])

CA,1-C = FCJ(τ_{f_1}, I_{AS}, θ, JA, VCA, C_{JAO}, CMIN)
CC,G-C = FCJ(τ_{R1}, I_{CS}, θ, JC, VCC, C_{JCO}, CMIN)
CK,G-K = CK

DEFINED PARAMETERS (REVERSE BREAKDOWN MULTIPLIERS)

P1 = FBD(VCC,VBOC)
P2 = FBD(VCK,VBOK)

SNUBBER ELEMENTS (OPTIONAL)

RS ,A-2 = VALUE IN OHMS
CS ,2-K = VALUE IN FARADS

ALSO IF USING DIODE SNUBBER:

JD ,A-2 = DIODE Q(DIODE SAT. CURRENT, THERMAL VOLTAGE)
CD ,A-2 = VALUE IN FARADS

Table 5.3

PROCEDURE FOR DETERMINING PARAMETERS FOR THE SCEPTRE 3-JUNCTION SCR MODEL OF FIGURE 5.6

STEP 1. Obtain the following nine parameters from manufacturer's specifications data sheets.[22]

I_H - Holding current.

I_{GT} - Gate trigger current.

$t_r(t_{on})$ - t_r; rise time: t_{on}; turn-on time.

V_T - Minimum on-state voltage.

R_{on} - On-state resistance (use inverse slope of i_{AK} vs. v_{AR} curve).

V_{BD} - Break-over voltage.

dv/dt - Maximum rate of rise of forward blocking voltage.

t_q - Circuit commutated turn-off time.

V_{GRM} - Maximum reverse gate voltage.

STEP 2.

$$RK = .75V/I_{GT} \text{ ohms.}$$

STEP 3.

$$\alpha_{R_2} = .5$$

$$\alpha_{f_2} = .9 \text{ or } .95$$

$$\alpha_{f_1} = \min \left\{ .9 \text{ or } 1 - \alpha_{f_2} + \frac{I_{GT}}{\alpha_{f_2} I_H} \right\}$$

$$\alpha_{R_1} = \alpha_{f_1}$$

STEP 4.

$$\tau_{f_1} = (\beta_1\beta_2 - 1)t_r/1.8\beta_1 \text{ seconds.}$$

where: $\beta_1 = \frac{\alpha_{f_1}}{1-\alpha_{f_1}}$, $\beta_2 = \frac{\alpha_{f_2}}{1-\alpha_{f_2}}$

STEP 5.

$$\Theta = q/KT \approx 38.61 \text{ V}^{-1} \text{ at } 300°K$$

$$I_S = 10^{-(V_T + .74)/.11} \text{ Amps.}$$

$$I_{AS} = I_S/\alpha f_1 \text{ Amps.}$$

$$I_{KS} = I_S/\alpha f_2 \text{ Amps.}$$

$$I_{CS} = I_S/R_1 + I_S/R_2 + \exp\left[\frac{V_H}{\Theta}\right] - \ell n\left[\frac{I_H}{I_S}\right] - \ell n\left[\frac{I_H - I_{GT}}{I_S}\right] + \ell n[\alpha f_1 I_H - (1 - \alpha f_2)(I_H - I_G)] \text{ Amps.}$$

$$P3 = I_S/I_{CS}$$

STEP 6.

$$R = R_{on} \text{ ohms.}$$

STEP 7.

$$\tau_{R1} = 9 t_q P3 \text{ seconds.}$$

STEP 8.

$$C_{JC_O} = .4 I_H (t_{on}/(dV/dt))^{\frac{1}{2}} \text{ farads.}$$

where: $t_{on} = 1.5\ t_r$

dV/dt is volts/second.

$$C_{JA_O} = \{.5 C_{JC_O} \leq C_{JA_O} \leq C_{JC_O}\} \text{ farads.}$$

$$CK \leq C_{JC_O} \text{ farads.}$$

STEP 9.

$$V_{BOC} = V_{BO} \text{ volts.}$$

$$V_{BOK} = V_{GRM} \text{ (or 5V if not given) volts.}$$

STEP 10.

$$C_{MIN} = C_{JC_O}/(V_{BO})^{\frac{1}{2}} \text{ farads.}$$

or: 1.0-10

Note: This precedure adapted from that presented by Hu and Ki in reference [1]

of the SPICE2 2-Transistor SCR Model into the SCEPTRE 3-Junction SCR Model.

Table 5.3 summarizes the entire procedure for determining parameters for the SCEPTRE 3-Junction SCR Model of figure 5.6.

Using the procedure described in table 5.3, the parameters for the GE C602 LM SCR are calculated and tabulated in table 5.4.

The model description as entered in a SCEPTRE input deck is listed in figure 5.7. In order for the model to function properly as listed, two special subroutines, FCJ and FBD must be provided in the input deck. These subroutines are listed in figure 5.8 and figure 5.9 respectively.

Computer simulation test verification of the model for a GE C602 LM SCR is presented in Table 5.5 The parameters to be verified are listed in the table along with the manufacturer's specified value and SCEPTRE simulation results.

NOTE

Default accuracy requirements of SCEPTRE may not always be adequate to insure proper simulation results. Erroneous results are most likely to occur in simulating circuits with high dv/dt (either forward or reversed) without a snubber circuit. Reducing error tolerance under Run Controls will solve the problem; however, longer run times are to be expected for greater accuracy criterion.

Table 5.4

SCEPTRE 3-JUNCTION SCR MODEL PARAMETERS OBTAINED USING THE PROCEDURE OF TABLE 5.3 FOR A GE C602 LM SCR.

RK	9.375Ω	I_{CS}	5.65D-15 A
α_{R_2}	.5	P3	4.4D-3
α_{f_2}	.9	R	5.D-4 Ω
α_{f_1}	.9	τ_{R_1}	4.95D-6 S
α_{R_1}	.9	C_{JC_O}	4.D-9 F
τ_{f_1}	1.780-5 S	C_{JA_O}	4.D-9 F
θ	38.61 V^{-1}	CK	1.D-9 F
I_S	2.239D-17 A	V_{BOC}	2.7D3
I_{AS}	2.488D-17 A	V_{BOK}	5.
I_{KS}	2.488D-17 A	C_{MIN}	1.D-10

Table 5.5

MANUFACTURER'S SPECIFICATIONS FOR A GE C602 LM SCR AND SCEPTRE COMPUTER SIMULATION SPECIFICATION PREDICTIONS.

Quantity	Manufacturer's specifications	SCEPTRE simulation value
I_H	100 ma	100 ma
I_{GT}	80 ma	87 ma
$t_r(t_{on})$	3.6μs(5.4μs)	4μs(7μs)
V_T	1.1V	1.1V
V_{BO}	2700V	2700V
dv/dt	G.T.500V/μs	G.T.500V/μs
tq	L.T.125μs	L.T.125μs

```
MODEL DESCRIPTION
MODEL SCR(A-G-K)
  THIS MODEL IS CALLED THE 3-JUNCTION SCR MODEL FOR SCEPTRE. IT IS DEVEL-
OPED TO UTILIZE A PARAMETER DETERMINATION PROCEEDURE WHICH IS BASED ON
THE MODIFIED HU-KI PROCEEDURE OF PARAMETER DETERMINATION FOR THE 2-TRAN-
SISTOR SCR MODEL FOR SPICE2.
  THIS MODEL IS REFERED TO AS THE THREE JUNCTION MODEL SINCE ALL SECOND-
ARY DEPENDENT CURRENT SOURCES ARE REFERENCED TO THREE PRIMARY DEPENDENT
CURRENT SOURCES (PN JUNCTIONS).
UNITS: OHMS, FARADS, HENRIES, SECONDS, AMPS, VOLTS
ELEMENTS
R,A-1=5.D-3
RA,1-C=1.D6
RC,C-G=1.D6
RK,G-K=9.375
JA,1-C=DIODE Q(2.488D-17,38.61)
JC,G-C=DIODE Q(5.65D-15,38.61)
JK,G-K=DIODE Q(2.488D-17,38.61)
J1,C-1=4.4D-3*JC
J2,C-G=.9*JA
J3,C-G=.9*JK
J4,C-G=P1*JC
J5,K-G=4.4D-3*JC
J6,K-G=P2*JK
CA,1-C=FCJ(1.78D-5,2.488D-17,38.61,JA,VCA,4.D-9,1.D-9)
CC,G-C=FCJ(4.95D-6,5.65D-15,38.61,JC,VCC,4.D-9,1.D-9)
CK,G-K=4.D-9
RS,A-2=10.
CS,2-K=.1D-6
DEFINED PARAMETERS
P1=FBD(VCC,2.7D3,5.65D-15)
P2=FBD(VCK,5.,2.488D-17)
OUTPUTS
VCA,VCC,VCK,PLOT
```

Fig. 5.7. SCEPTRE INPUT LISTING FOR A GE C602 LM SCR MODEL USING THE PARAMETERS OF TABLE 5.4 IN THE MODEL NETWORK OF FIGURE 5.6.

```
      DOUBLE PRECISION FUNCTION FCJ(TAU,IS,THT,J,VC,CJO,CMIN)
C SUBROUTINE FCJ CALCULATES THE NON-LINEAR INCREMENTAL CAPACITANCE ASSOCIATED
C WITH THE CHARGE STORAGE OCCURRING ABOUT A PN JUNCTION. IF THE JUNCTION IS
C FORWARD BIASED THE DEPLETION LAYER TERM IS HELD CONSTANT WHILE THE DIFFUSION
C CALCULATED. CONVERSELY IF THE JUNCTION IS REVERSE BIASED ONLY A DEPLETION
C TERM IS CALCULATED. FOR A REVERSED BIASED JUNCTION THE CAPACITANCE IS LIMITED
C TO A MINIMUM VALUE, CMIM, TO AVOID UNREASONABLY SMALL TIME CONSTANTS IN THE
C CIRCUIT SIMULATION. PARAMETERS ARE; TAU = THE EXCESS CARRIER LIFETIME IN THE
C NEUTRAL REGIONS ABOUT THE JUNCTION, IS = JUNCTION SATURATION CURRENT, THT =
C EINSTEIN'S CONSTANT (Q/KT = 38.61 @ 300 DEG K.), J = CURRENT SOURCE SIMULATING
C THE PN JUNCTION FOR WHICH CAPACITANCE IS BEING CALCULATED, VC = VOLTAGE ACROSS
C CAPACITOR WHOSE VALUE IS BEING CALCULATED, CJO = ZERO BIAS VALUE OF THE
C DEPLETION LAYER CAPACITANCE, CMIN = MINIMUM VALUE OF JUNCTION CAPACITANCE TO
C BE ALLOWED.
      IMPLICIT REAL*8(A-Z)
      IF(VC.GT.0.) GO TO 10
      FCJ=CJO/(1.-VC)**.5
      IF(FCJ.GE.CMIN) RETURN
      FCJ=CMIN
      RETURN
   10 FCJ=TAU*THT*(J+IS)+CJO
      RETURN
      END
```

Fig. 5.8 Special subroutine FCJ used to calculate non-linear junction capacitances of the SCEPTRE 3-Junction SCR Model.

```
      DOUBLE PRECISION FUNCTION FBD(VJ,VBD,IS)
C FBD IS A SUBROUTINE TO DETERMINE IF THE REVERSE BREAKDOWN VOLTAGE OF A PN
C JUNCTION HAS BEEN EXCEEDED AND IF SO TO CALCULATE A MULTIPLIER TO REFLECT
C AVALANCHE CURRENTS IN THE PN JUNCTION. THIS MULTIPLIER IS USED AS THE
C COEFFICIENT OF A SECONDARY DEPENDENT CURRENT SOURCE IN PARALLEL WITH THE
C PRIMARY DEPENDENT CURRENT SOURCE WHICH SIMULATES THE PN JUNCTION. PARAMETERS
C ARE; VJ = THE VOLTAGE ACROSS THE JUNCTION, VBD = THE BREAKDOWN VOLTAGE
C OF THE JUNCTION, IS = JUNCTION SATURATION CURRENT.
C     THE JUNCTION AVALANCHE BREAKDOWN MULTIPLIER IS THEORETICALLY ESPRESSED AS
C (-1/(1-(VJ/VBD)**6)); HOWEVER,TO ACHIEVE SHORTER RUN TIMES, AN EXPONENTIAL
C MULTIPLIER,-DEXP(100.*(-VBD-VJ)), IS USED IN THIS CASE.
      IMPLICIT REAL*8(A-Z)
      IF(VJ.GT.(-VBD))GO TO 10
      A=100.*(-VBD-VJ)
      IF(A.LE.40.) GO TO 30
      A=40.
   30 FBD=-DEXP(A)
      GO TO 20
   10 FBD=0.0
   20 RETURN
      END
```

Fig. 5.9 Special subroutine FBD used to calculate junction breakdown currents for the SCEPTRE 3-Junction SCR Model.

5.3 A SCEPTRE 3-JUNCTION SCR Model with a reduced number of current sources in the model.

Sections 5.1 and 5.2 presented the development of an SCR model for use in SCEPTRE which is functionally equivalent to the SPICE2 SCR Model developed in Chapters 1 through 4. This SCEPTRE 3-Junction SCR Model is, however, quite imposing with respect to the number of elements contained in the network representation of the model as given by Figure 5.6.

A major objective of the research of this project was to simulate high voltage resonant charging pulse power circuits. Since typical high power SCR's have maximum blocking voltage ratings on the order of 3000V, high voltage circuits are developed using a number of SCR's in series to meet the voltage blocking requirements.

Also, pulse power circuits may have a number of parallel or anti-parallel branches each having several SCR's. The basic controlled 3-ϕ rectifier circuit is an example. In order to provide controlled rectification of a 7000V, 3-ϕ source, typically 18 SCR's of 3000V blocking capability might be employed.

The problem presented to simulation of this type of circuit using the SCR model of Figure 5.6 is that SCEPTRE internal limitations on the number of sources the program can accommodate may be exceeded.

This problem required some experimentation with SCEPTRE capabilities before a satisfactory solution was achieved. Initially, attempts were made to formulate each of the three junction currents as a mathematical equivalent to the total of the sources in parallel representing each junction. This approach was in violation of the SCEPTRE suggested programming constraints listed in section 5.1. Not only was the mathematical formulation rather imposing, but, the end result was that an exact

formulation of the model of Figure 5.6 as three current sources resulted in the following.

1. Run times for identical problems increased in some cases as much as 200% to 300%.

2. The failure to adhere to constraints 1 through 4 of section 5.1 made initial conditions solutions available only through the transient approach, i.e. using RUN IC VIA IMPLICIT. Without special operator input, the effects of this on CPU time to calculate initial conditions was drastic. Even small networks were observed to require as much as 15 mins. CPU time to complete initial conditions solutions. Long CPU times resulted due to the extremely small time step required (less than 10^{-30} sec.) to handle the steep transients of the non-linear circuit elements such as junction capacitances and due to the large number of multiply operations necessary in each iteration necessary to calculate values of the junction current sources described by the long and complex math expressions defining the sources.

The primary and secondary dependent current source approach to defining junction relationships as shown in Figure 5.6 is inherently more efficient. The reason being that a relatively simple non-linear expression defines the primary dependent current source thereby minimizing the number of multiply operations by the computer. Secondary dependent current sources are either linear or simple non-linear multiples of the primary dependent current sources. In the case of non-linear secondary dependence, SCEPTRE offers the use of subroutines. Through this device, logic statements may be used to test the need for non-linear versus linear secondary dependence

before initiating the calculation. For these reasons, the model of Figure 5.6 having a larger network was judged superior to a three current source model using a mathematical equivalent formulation to the nine current source model of Figure 5.6.

A second approach was then conceived to effect the goal of a reduced number of sources in the model. This second approach was judged successful and is summarized as follows:

1. The secondary dependent current sources, J1 and J5 are equivalent to $\alpha_{R_1} \cdot I_{R1}$ and $\alpha_{R_2} \cdot I_{R_2}$ of Figure 5.3. It is most easily visualized through the 2-transistor basis of the model of Figure 5.3 that these two current sources model third quadrant operation of the PNP and NPN transistor respectively. Since even at high currents, the SCR center junction (JC of Figure 5.6) and $I_{R_1} + I_{DFOR} + I_{R_2}$ of Figure 5.3 reaches a substantially lower forward biased state than do the outer junctions JA and JK, then it is reasonable to neglect the J1 and J5 secondary dependent current sources.

2. The two secondary dependent current sources, J2 and J3, are linearly dependent upon the primary dependent current sources JA and JK respectively. Since the calculation of both JA and JK must precede the calculation of J1 and J3 due to the SCEPTRE calculation procedure, then a simple summation of J1 and J2 into a single source seemed reasonable although SCEPTRE literature seemed to exclude this possibility[16 p.13]. Experiment proved the approach feasible, however.

3. The secondary dependent current sources J4 and J6 used to model junction breakdown were handled by a more novel approach.

Considering the DIODE EQUATION (X1,X2) special value expression used in SCEPTRE to define primary dependent current sources modeling PN junctions, the parameters X1 and X2 are presented in SCEPTRE users literature to be constants. X1 represents the diode reverse saturation current, and X2 represents the junction thermal voltage. Since classical PN junction theory expresses the PN junction reverse saturation current as a function of the junction voltage, then it was deemed desirable to express X1 as a function of the junction voltage.

Again SCEPTRE's calculation heirarchy was used to effect this result. Defined parameters are the first quantities calculated at the beginning of each time step and are then provided to the network as constants. Also defined parameters may be evaluated through the subroutine capability, thereby allowing a logical test to be made before consuming CPU time to evaluate functions.

With this approach, J4 and J6 were eliminated from the model and the PN junction breakdown capability was developed by developing a functional relationship for X1 through the defined parameter technique.

It is noted that the success of this approach will also admit the possibility of semiconductor thermal behavior studies through developing a functional relationship for the thermal voltage parameter X2. Also a functional relationship for X2 would permit distinction between high level and low level injection and β variations.

The result of the modifications just summarized is the model network illustrated in Figure 5.10. It has four dependent current sources versus the nine dependent sources of the model network shown in Figure 5.6.

Table 5.6 gives a generalized listing of the element descriptions in SCEPTRE input format for the SCR model of Figure 5.10.

The parameters for the reduced 3-Junction SCR model of Figure 5.10 are determined by the procedure of Table 5.3 in exactly the same manner as the parameters for the 3-Junction SCR Model of Figure 5.6. The only difference being that the α_{R_1} and α_{R_2} parameters of step 3 and the P3 parameter of step 5 are not required for the reduced 3-Junction model of Figure 5.10.

A SCEPTRE model description for a GE C602 LM SCR model is given in Figure 5.11, a special subroutine FIS required to evaluate defined parameters PX1 and PX3 of the reduced 3-Junction SCR Model is shown in Figure 5.12.

Model validation tests were done to verify computer prediction of manufacturers specification data used to determine model parameters. Computer simulation values for the reduced 3-Junction model were not distinguishable from those predicted for the 3-Junction model and tabulated in Table 5.5.

The computer verification simulation test results are compiled in reference 39 for both the 3-Junction model of Figure 5.6 and the reduced 3-Junction model of Figure 5.10.

The run times for the reduced 3-Junction model of Figure 5.10 were observed to be approximately 5% to 10% shorter than those of the 3-Junction model of Figure 5.6.

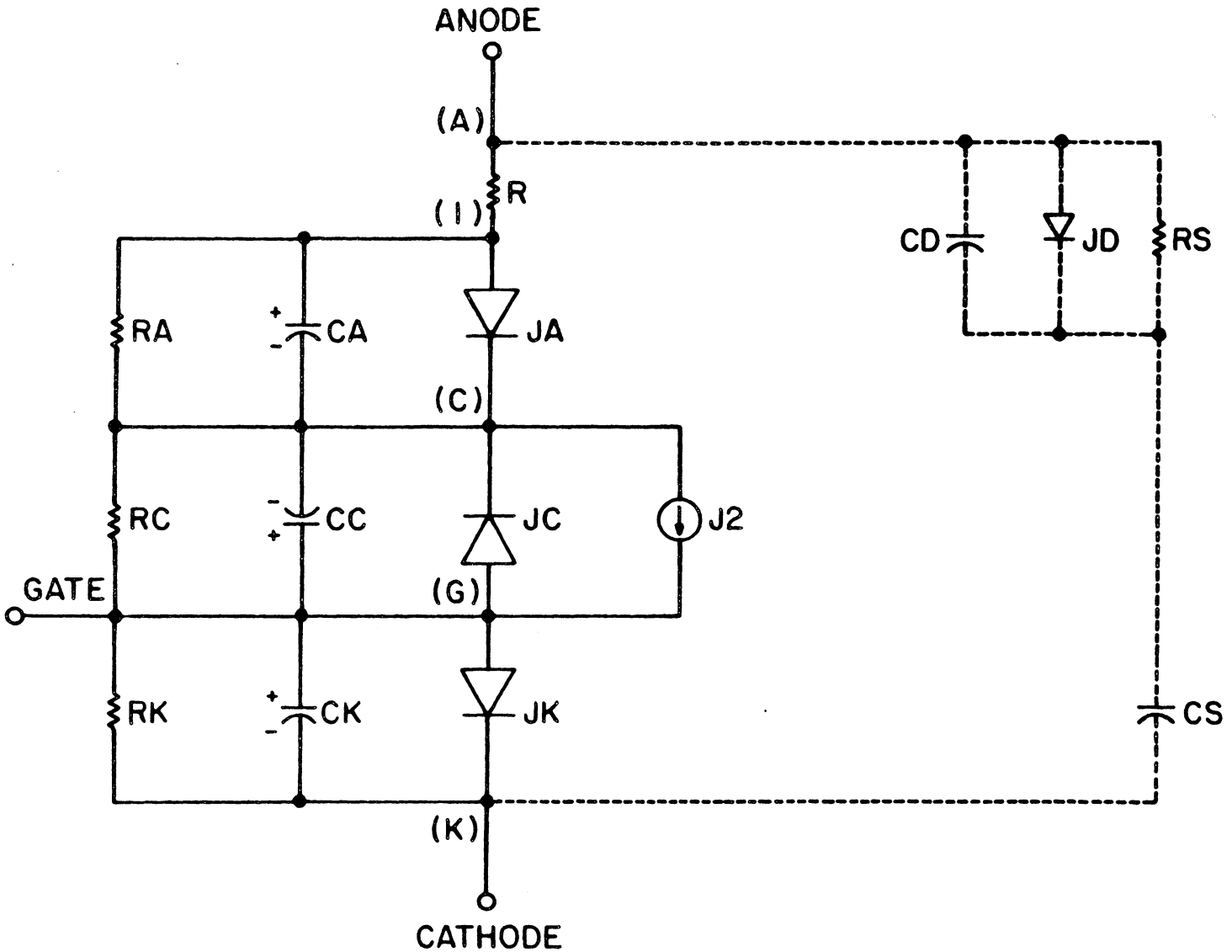


Fig. 5.10. THE SCEPTRE REDUCED 3-JUNCTION SCR MODEL WITH A REDUCED NUMBER OF CURRENT SOURCES IN THE MODEL. (—) model. (---) optional snubber.

TABLE 5.6

SCEPTRE SCR MODEL CIRCUIT ELEMENT DESCRIPTION
FOR THE 3-JUNCTION MODEL OF FIG. 5.10

RESISTORS

R,A-1 = R
RA,1-C = 1.D6
RC,C-6 = 1.D6
RK,G-K = RK

PRIMARY DEPENDENT SOURCES (PN JUNCTIONS)

JA ,1-C = DIODE Q(I_{AS},θ)

JC ,G-C = DIODE Q(PX1,PX2)
JK ,G-K = DIODE Q(PX3,PX2)

SECONDARY DEPENDENT SOURCES (COLLECTED CURRENTS & REVERSE BREAKDOWN CURRENTS)

J2 = X1(α_{f_1}*JA + α_{f_2}*JK)

CAPACITANCES (JUNCTION DEPLETION LAYER AND NEUTRAL REGION EXCESS CHARGE STORAGE [DIFFUSION])

CA,1-C = FCJ(τ_{f_1}, I_{AS}, θ, JA, VCA, C_{JAO}, CMIN)
CC,G-C = FCJ(τ_{R1}, I_{CS}, θ, JC, VCC, C_{JCO}, CMIN)
CK,G-K = CK

DEFINED PARAMETERS (REVERSE BREAKDOWN MULTIPLIERS)

PX1 = FIS(I_{CS}, VCC, VBOC)
PX2 = θ
PX3 = FIS(I_{KS}, VCK, VBOK)

SNUBBER ELEMENTS (OPTIONAL)

RS ,A-2 = VALUE IN OHMS
CS ,2-K = VALUE IN FARADS

ALSO IF USING DIODE SNUBBER:
- - - - - - - - - - - - - - -

JD ,A-2 = DIODE Q(DIODE SAT. CURRENT, THERMAL VOLTAGE)
CD ,A-2 = VALUE IN FARADS

```
MODEL DESCRIPTION
MODEL SCR(A-G-K)
  THIS IS A REDUCED ELEMENT VERSION OF THE 3-JUNCTION SCR MODEL DEVELOPED
FOR USE WITH SCEPTRE. THE PARAMETER DETERMINATION PROCEEDURE FOR THIS MODEL
IS THE SAME AS FOR THE 3-JUNCTION MODEL.
UNITS: OHMS, FARADS, HENRIES, SECONDS, AMPS, VOLTS
ELEMENTS
R,A-1=5.D-3
RA,1-C=1.D6
RC,C-G=1.D6
RK,G-K=9.375
JA,1-C=DIODE Q(2.488D-17,38.61)
JC,G-C=DIODE Q(PX1,PX2)
JK,G-K=DIODE Q(PX3,PX2)
J2,C-G=X1(.9*JA+.9*JK)
CA,1-C=FCJ(1.78D-5,2.488D-17,38.61,JA,VCA,4.D-9,1.D-10)
CC,G-C=FCJ(4.95D-6,5.65D-15,38.61,JC,VCC,4.D-9,1.D-10)
CK,G-K=1.D-9
RS,A-2=100.
CS,2-K=.1D-6
DEFINED PARAMETERS
PX1=FIS(5.65D-15,VCC,2.7D3)
PX2=38.61
PX3=FIS(2.488D-17,VCK,5.)
OUTPUTS
VCA,VCC,VCK,PLOT
```

FIG. 5.11 SCEPTRE MODEL DESCRIPTION Input for a GE C602 LM

```
      DOUBLE PRECISION FUNCTION FIS(IS,VJ,VBD)
C SUBROUTINE FIS IS USSD TO SIMULATE JUNCTION BREAKDOWN BY VARYING THE
C SATURATION CURRENT, IS, INPUT TO THE DIODE EQUATION FOR PRIMARY DEPEN-
C DENT CURRENT SOURCES.  IS = JUNCTION REVERSE SATURATION CURRENT:  VJ =
C CAPACITOR STATE VARIABLE VOLTAGE FOR JUNCTION:  VBD = BREAKDOWN VOLTAGE:
      IMPLICIT REAL*8(A-K,O-Z)
      FIS=IS
      IF(VJ.GE.-VBD) RETURN
      A=100.*(-VBD-VJ)
      IF(A.LE.40.) GO TO 10
      A=40.
   10 FIS=IS*DEXP(A)
      RETURN
      END
```

FIG. 5.12. SUBROUTINE FIS USED TO CALCULATE PX1 & PX2 OF TABLE 5.6

5.4 Excessive Under-flow and Over-flow and Subroutine Optimization

Excessive under-flow and over-flow has been determined to occur frequently in SCEPTRE internal subroutines. The problem is therefore not solvable through control of input network description. A solution would entail writing alternative subroutines and incorporating over-flow and under-flow protection in the subroutines.

The most direct approach would seem to be to take the actual SCEPTRE subroutines, copy them, develop over-flow/under-flow protection and then input them as user subroutines. The actual Fortran coding of the subroutines is available only from the SCEPTRE program tape as received from U.S.F.

The user input subroutines developed at VPI&SU appear reasonable. Extensive optimization would probably not be benefit justified.

5.5 Summary and Conclusions

This chapter has taken a step towards developing a generalized SCR model. The "Modified Hu-ki" model for use with SPICE2 was adapted to use with SCEPTRE.

Adaptation of the "Modified Hu-ki" model from SPICE2 to SCEPTRE required substantial alteration of the model circuit analog and parameter estimation procedure. The two-transistor SCR model based on the terminal characteristics version of the modified Eber-Moll transistor model which is contained in the SPICE2 model library was found unsuitable to SCEPTRE programming requirements. Subsequent

reconfiguration to the injection version of the BJT model suitable to SCEPTRE produced growth in the equivalent network of the model. Additionally, a capacitor state variable was added for the cathode junction, two resistors for initial conditions solutions were added, and voltage dependent current sources to simulate junction breakdown were added. The result was an equivalent network much too large for simulating practical SCR circuits having more than one or two SCRs.

Algebraic combination of like elements in parallel was performed to reduce the network. Some elements were completely removed from the model after analysis and test verification showed that they were inconsequential to the model performance.

Nomenclature for this SCEPTRE SCR model was established as the SCEPTRE 3-Junction SCR model. This was because the model circuit analog no longer held any resemblance to the two-transistor configuration. Instead it held a three-diode structure which strongly suggested the PNPN construction of the device. Also each of the current sources in the model was readily recognizable for the physical process which it modeled. This 3-Junction model was noted to be similar in appearance to a model by Nienhus[8] denoted the intrinsic SCR model.

The parameter estimation procedure for the "modified Hu-ki" model of SPICE2 was revised to reflect the changes and additions resulting in the SCEPTRE 3-Junction model. This resulted in some growth in the procedure, but the essential character of using manufacturer's specification sheets for a data base was preserved.

The 3-Junction model was tested via parameter prediction simulations. Simulation results showed good simulation of I_H, I_{GT}, t_{on}, V_T, and V_{BO} characterizations. The dV/dt and t_q simulation capability was seen to be degraded somewhat. These important dynamic performances are primary objectives of this thesis. Cause of the degradation was felt to be embodied in the extensive modification to the circuit analog in the transition from the "Hu-ki" model to the 3-Junction model. While no given alteration was singly at fault, the conglomerate changes resulted in the loss of accuracy. The major contributor to degraded dV/dt prediction was the addition of the capacitor state variable for the cathode junction. This additional capacitance also contributed to the degraded t_q performance since it also is a test of reapplied dV/dt, however, this complex area of turn-off dynamics involves virtually all aspects of the model.

Much of the derivation of the "Hu-ki" model was empirical. Relations were derived for the parameter estimation procedure based on simulating a wide range of device types then selecting a relationship which best fit the results for all devices.[1]

Some arbitrary shifting of the key parameters was seen to be able to provide required model performance characteristics; however, no defined procedure for readjusting parameters was established. It was decided to accept the degraded preformance as being tolerable in phase control type SCRs where parameter tolerances may be quite loose.

In order to further reduce the equivalent network for the SCEPTRE 3-Junction model, it was discovered that an undocumented capability existed in SCEPTRE which allowed dynamic variation of SCEPTRE DIODE EQUATION arguments by entering them as DEFINED PARAMETERS. This capability allowed the expression of junction breakdown by variation of the diode reverse saturation current. This was merely a network alteration with no parameter estimation procedure alteration required. This final network configuration was assigned nomenclature as the Reduced 3-Junction model.

The insight achieved in converting the SPICE2 "Hu-ki" model into the SCEPTRE Reduced 3-Junction model has lead to two conclusions. One is that the three-diode (or intrinsic) approach to modeling is preferred over the two-transistor configuration. This is due not only to the smaller equivalent network but also to the insight to model performance offered by the inherent suggestion of the three-diode basis of the model to the intrinsic three-junction physical construction of the SCR.

The other conclusion is that in order to achieve the goal of an accurate simulation capability of the three SCR dynamic performances, gate driven turn-on, dV/dt, and commutation, a fundamental development effort will be required. That development is the subject of chapters 8 and 9.

At this point, it remains to show that the SCEPTRE 3-Junction model circuit analog is useful to simulate phase-control-SCR circuits containing several SCRs.

CHAPTER 6

AC RESONANT CHARGING CIRCUIT SIMULATIONS

An SCR model for use with SCEPTRE was presented in Chapter 5. Two versions of the model were developed, one called the 3-Junction model and the other called the Reduced 3-Junction model. The simulation performance of the two models was shown to be virtually identical through the model verifications runs of reference 39. Since the run times using the reduced 3-Junction model were observed to be slightly shorter than those for the 3-Junction model, and since the likelihood of exceeding a SCEPTRE capacity limit is less with the reduced model of Fig. 5.10, then it is selected for use in doing SCEPTRE simulations of resonant charging circuits.

Circuits to be simulated in this research are adaptations of the AC and DC resonant charging circuits developed by J. Silva at AFAPL and reported in reference [15]. Silva developed his circuits using diodes as rectifier switches, however, the goal of this research is to develop a computer simulation capability to simulate controlled rectifier (SCR) circuits. This simulation capability will then serve as a design aid in development of the actual resonant charging circuits using SCRs. This report presents the development of the computer simulation capability for simulating the controlled rectifiers (SCRs) and other electronics of such circuits.

Magnetics are treated as linear elements in this report, however concurrent research is being conducted by Clemson University to enable treatment of the non-linearities of the magnetics.

In order to do controlled rectifier (SCR) circuit simulations, facsimile circuits substituting SCR's for some of the diodes in Silva's circuits were devised. The plan being to compare simulation data of the facsimile circuits to the Silva's charging system data. The considerable differences between SCR circuits and Silva's diode circuits makes direct substitution of SCR rectifiers for diode rectifiers impossible. For this reason, careful consideration had to be given to construction of proper facsimile circuits. Significant considerations are summarized as follows:

- The line voltages in Silva's circuit greatly exceed any single SCR's blocking voltage rating. Actual SCR circuits performing at the voltage levels of Silva's circuits would require a large number of SCR's to simulate a full three phase system.

  Simulation of sufficient SCR's in series (seven) to provide the needed values of blocking voltages was confronted by SCEPTRE network programming limits (on the total number of sources present in the network) when considering the total 3-Ø system (42 SCR's). While the SCR circuits may have been simulated, review with Clemson revealed that the combined system simulation would exceed SCEPTRE limits.

  A prospect to assign arbitrarily high (and unrealistic) values for device blocking voltage ratings was considered but was deemed to limit the value of the research results in the end result.

  The solution was to design facsimile circuits having the minimum number of SCR's necessary to obtain controlled rectification in Silva's resonant charging circuits. This concept involved use of SCR's to provide forward blocking prior to triggering and Diodes to provide

reverse blocking capability in series with the SCR's reverse blocking to sustain the substantially higher voltages in the reverse direction presented by the resonantly changed load capacitor voltages in series with the negative half-cycle source voltages.

Since magnetic elements are treated as linear, simulation of more than one phase bank array in the AC system is merely redundant, therefore a single phase system having a resonant charging load on one-half cycle of the source is presented in section 6.1.

- The high cost of complete transient simulations in full scale facsimile's of Silva's circuits made design and debug operations cost prohibitive. The solution to this problem required development of scaled circuits. Since the research objective was to develop and validate a simulation capacity, then scaling is both a valid and desirable approach. While a rigorous approach to scaling[25] may be performed, absolute rigor is not required in this case since the simulation is not to validate or analyze an actual circuit, but to demonstrate a simulation capability. The validity of the simulation is established by the reasonableness of results as compared to the results obtained in circuits of a similar nature. The circuits of similar nature being Silva's diode switched resonant charging circuits. In the case of AC resonant charging circuits, Silva did not obtain final results for his circuits and therefore the validity of AC resonant charging circuit simulations is established only by the consistency of results with explanation of phenomena by engineering analysis.

A scaled 3-phase AC resonant charging circuit simulation is presented in section 6.2. Scaled elements were as follows in Table 6.1.

TABLE 6.1

Quality	Silva's Diode Circuits (unscaled)	SCR Facsimile Circuits (scaled)
3-Phase AC System (section 6.2)		
Source voltage	6465.85V per phase	1000V per phase
Source frequency	400 hertz.	1000 hertz.
Resonant load inductance	.327 henries	.05897 henries
Resonant load capacitance	.43 micro-farads	.43 micro-farads
DC Resonant Load on 3-phase Source (section 7.1)		
Source voltage	6465.85V per phase	1000V
Source frequency	400 hertz.	1000 hertz.
Resonant load inductance	2.58 henries	.173 henries
Resonant load capacitance	2.58 micro-farads	.586 micro-farads

Table 6.1 also presents the scaling of a DC resonant charging system presented in Chapter 7, section 7.1.

6.1 An AC Resonant Charging Circuit with three SCRs and a Diode in Series.

A single phase single loop AC resonant charging circuit is shown in Figure 8. The circuit has 3-SCRs and a diode in series. Silva's circuits used transformer secondary phase voltages of 6500V peak at 400Hz. Simulation of the required forty-two SCRs to develop a totally SCR 3ϕ circuit of this nature exceeds SCEPTRE capacity, therefore a single phase simulation is presented to illustrate the series SCR configuration.

Seven GE C602 LM SCR's with reverse blocking voltages of 2700 voltage are required in a totally SCR circuit in order to block the reverse voltages following resonant commutation of the SCR's. However, only three SCR's are needed to block the forward voltages. As a result, the design was simplified to SCR's to provide forward blocking and controller rectification and one diode (actual circuit may use several diodes) to provide additional reverse blocking needed. Figure 6.4 gives simulation results for the circuit of Fig. 6.3. The extended oscillatory behavior following commutation is due to snubber circuit resonant behavior with the large series inductor. CAD can be a useful tool in optimizing snubber design in this type of circuit.

The SCR's, s1, s2, and s3 of Fig. 6.3 had simulation parameters perturbed varying amounts within a 25% limit of deviation. Simulation results clearly showed the results of the perturbations. This provides a design aid to the balancing network requirements. CPU time for the simulation was 41.28 seconds for the 2.5 ms transient simulation of one complete cycle of the 400Hz source. It was observed that the 3-SCR series configuration required only slightly more CPU time than that for a single SCR in the same circuit configuration. This suggests that time step and not circuit size is the dominant factor in CPU time for a simulation.

```
      DOUBLE PRECISION FUNCTION FGEN(HIGH,LOW,TD,TON,TP,TIME,MNEG)
C FGEN IS A PULSE GENERATOR SUBROUTINE. THE PARAMETERS ARE AS FOLLOWS;
C HIGH = MAXIMUM VALUE OF FUNCTION , LOW = MINIMUM VALUE OF FUNC-
C TD = TIME DELAY UNTIL START OF FIRST PULSE, TON = TIME OF PULSE DURA-
C TION , TP = TIME OF PULSE CYCLE PERIOD, TIME = TIME POINT OF CIR-
C CUIT BEING SIMULATED. PULSE VALUE IS SET TO LOW FOR TIME LESS THAN
C OR EQUAL TO ZERO IF MNEG IS NOT EQUAL TO 1. MNEG = 1 IF PULSE MAY HAVE
C NON-ZERO VALUE AT OR PRIOR TO TIME EQUAL ZERO.
      IMPLICIT REAL*8(A-L,N-Z)
      FGEN=LOW
      IF(TIME.LE.0..AND.MNEG.NE.1) GO TO 20
      N=(TIME-TD)/TP
      IF(N.LT.0.0) GO TO 20
      M=IDINT(N)
      P=(N-M)*TP
      IF(P.GT.TON) GO TO 10
      FGEN=HIGH
      GO TO 20
   10 FGEN=LOW
   20 RETURN
      END
```

Fig.6.1 : Subroutine FGEN is a pulse generator subroutine used in circuit simulations to simulate gate drives and capacitor discharge switches.

(c)
```
MODELSCR1(A-G-K)
THISISAREDUCEDELEMENTVERSIONOFTHE3-JUNCTIONSCRMODELDEVELOPE
FORUSEWITHSCEPTRE.THEPARAMETERSDETERMINEDFORTHISMODELBYTHE
SCEPTRE3-JCTNSCRMODELPARAMETERDETERMINATIONPROCEEDUREHAVEBEEN
PERTURBEDSLIGHTLYTOSIMULATEBATCHPARAMETERVARIATION.
UNITS:OHMS,FARADS,HENRIES,SECONDS,AMPS,VOLTS
ELEMENTS
R,A-1=5.D-3
RA,1-C=1.D6
RC,C-G=1.D6
RK,G-K=9.375
JA,1-C=DIODEQ(2.488D-17,38.61)
JC,G-C=DIODEQ(PX1,PX2)
JK,G-K=DIODEQ(PX3,PX2)
J2,C-G=X1(.9*JA+.9*JK)
CA,1-C=FCJ(1.78D-5,2.488D-17,38.61,JA,VCA,4.D-9,1.D-10)
CC,G-C=FCJ(4.95D-6,5.65D-15,38.61,JC,VCC,4.D-9,1.D-10)
CK,G-K=1.D-9
RS,A-2=100.
CS,2-K=.1D-6
DEFINEDPARAMETERS
PX1=FIS(5.65D-15,VCC,2.7D3)
PX2=38.61
PX3=FIS(2.488D-17,VCK,5.)
OUTPUTS
VCC,VCK,PLOT
```

(d)
```
MODELSCR3(A-G-K)
THISISAREDUCEDELEMENTVERSIONOFTHE3-JUNCTIONSCRMODELDEVELOPE
FORUSEWITHSCEPTRE.THEPARAMETERSDETERMINEDFORTHISMODELBYTHE
SCEPTRE3-JCTNSCRMODELPARAMETERDETERMINATIONPROCEEDUREHAVEBEEN
PERTURBEDSLIGHTLYTOSIMULATEBATCHPARAMETERVARIATION.
UNITS:OHMS,FARADS,HENRIES,SECONDS,AMPS,VOLTS
ELEMENTS
R,A-1=5.D-3
RA,1-C=1.D6
RC,C-G=1.D6
RK,G-K=9.375
JA,1-C=DIODEQ(2.388D-17,38.61)
JC,G-C=DIODEQ(PX1,PX2)
JK,G-K=DIODEQ(PX3,PX2)
J2,C-G=X1(.9*JA+.9*JK)
CA,1-C=FCJ(1.88D-5,2.388D-17,38.61,JA,VCA,5.D-9,1.D-10)
CC,G-C=FCJ(4.85D-6,5.65D-15,38.61,JC,VCC,4.5D-9,1.D-10)
CK,G-K=1.D-9
RS,A-2=100.
CS,2-K=.1D-6
DEFINEDPARAMETERS
PX1=FIS(5.65D-15,VCC,2.7D3)
PX2=38.61
PX3=FIS(2.488D-17,VCK,5.)
OUTPUTS
VCC,VCK,PLOT
```

Fig. 6.2: Input listing for Figure 6.3. (2-pages)
(a), (b), (c) are perturbed SCR models
(d) circuit element listing.

(a)

```
MODELSCR2(A-G-K)
THISISAREDUCEDELEMENTVERSIONOFTHE3-JUNCTIONSCRMODELDEVELOPE
FORUSEWITHSCEPTRE.THEPARAMETERSDETERMINEDFORTHISMODELBYTHE
SCEPTRE3-JCTNSCRMODELPARAMETERDETERMINATIONPROCEEDUREHAVEBEEN
PERTURBEDSLIGHTLYTOSIMULATEBATCHPARAMETERVARIATION.
UNITS:OHMS,FARADS,HENRIES,SECONDS,AMPS,VOLTS
ELEMENTS
R,A-1=5.D-3
RA,1-C=1.D6
RC,C-G=1.D6
RK,G-K=9.375
JA,1-C=DIODEQ(2.588D-17,38.61)
JC,G-C=DIODEQ(PX1,PX2)
JK,G-K=DIODEQ(PX3,PX2)
J2,C-G=X1(.9*JA+.91*JK)
CA,1-C=FCJ(1.68D-5,2.588D-17,38.61,JA,VCA,3.D-9,1.D-10)
CC,G-C=FCJ(4.90D-6,5.65D-15,38.61,JC,VCC,3.5D-9,1.D-10)
CK,G-K=1.D-9
RS,A-2=100.
CS,2-K=.1D-6
DEFINEDPARAMETERS
PX1=FIS(5.65D-15,VCC,2.7D3)
PX2=38.61
PX3=FIS(2.488D-17,VCK,5.)
OUTPUTS
VCC,VCK,PLOT
```

(b)

```
CIRCUIT DESCRIPTION
THIS CIRCUIT IS A SINGLE PHASE AC CIRCUIT HAVING 3 SCR'S AND A DIODE
IN SERIES.
ELEMENTS
EAN,0-1=X1(6465.85*DSIN(2513.2*TIME))
RA,1-2=1.
LA,2-3=.327
S1,3-4-5=MODEL SCR1
S2,5-6-7=MODEL SCR2
S3,7-8-9=MODEL SCR3
JD1,9-10=DIODE Q(1.D-6,38.61)
CD1,9-10=1.D-8
C0,10-0=.43D-6
RB1,3-5=17.5D3
RB2,5-7=17.5D3
RB3,7-9=17.5D3
RB4,9-10=1.D5
JG1,5-4=FGEN(.2,0.,1.D-4,5.D-5,2.5D-3,TIME,0)
JG2,7-6=FGEN(.2,0.,1.D-4,5.D-5,2.5D-3,TIME,0)
JG3,9-8=FGEN(.2,0.,1.D-4,5.D-5,2.5D-3,TIME,0)
OUTPUTS
EAN,VRB1,ILA,VC0,PLOT1
VCAS1,VCAS2,VCAS3,VCD1,PLOT2
VCCS1,VCCS2,VCCS3,PLOT3
RUN CONTROLS
COMPUTER TIME LIMIT = 10.
INTEGRATION ROUTINE = IMPLICIT
PLOT INTERVAL = 1.5D-5
MAXIMUM PRINT POINTS=0
STOP TIME=2.5E-3
MINIMUM STEP SIZE = 1.E-30
END
```

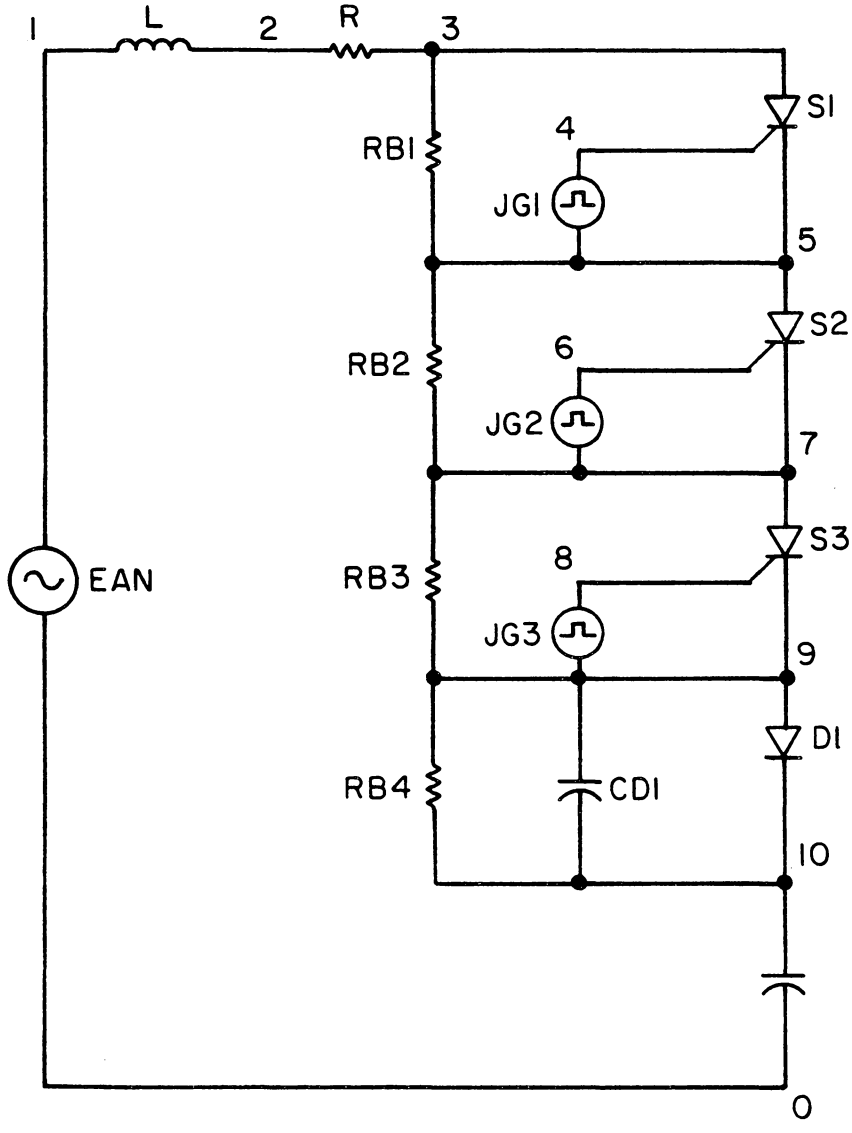


Figure 6.3 Three SCRs and a Diode in Series.

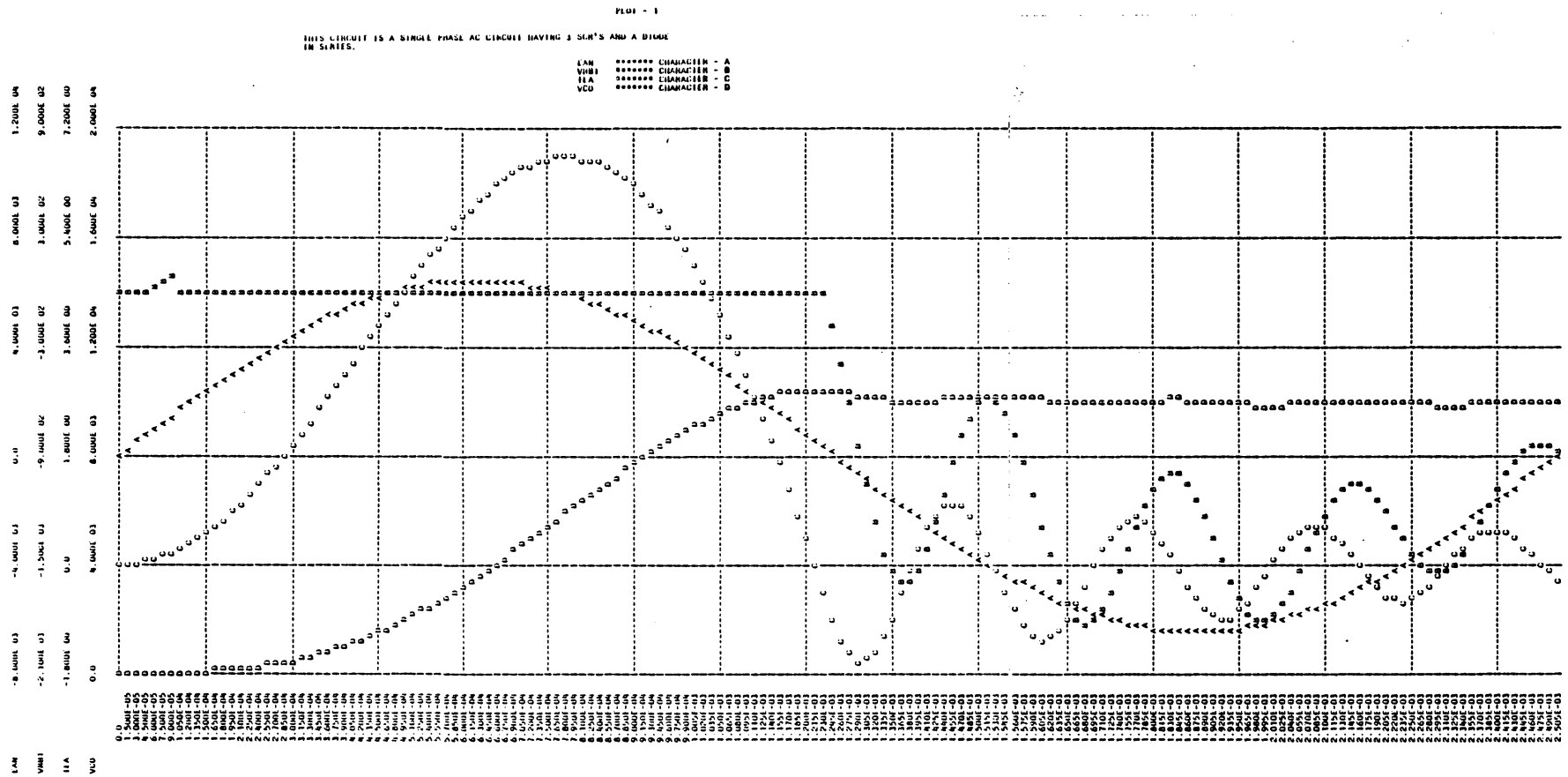


Figure 6.4 SCEPTRE Simulation Results for the Circuit of Figure 6.3 (part 1 of 2).

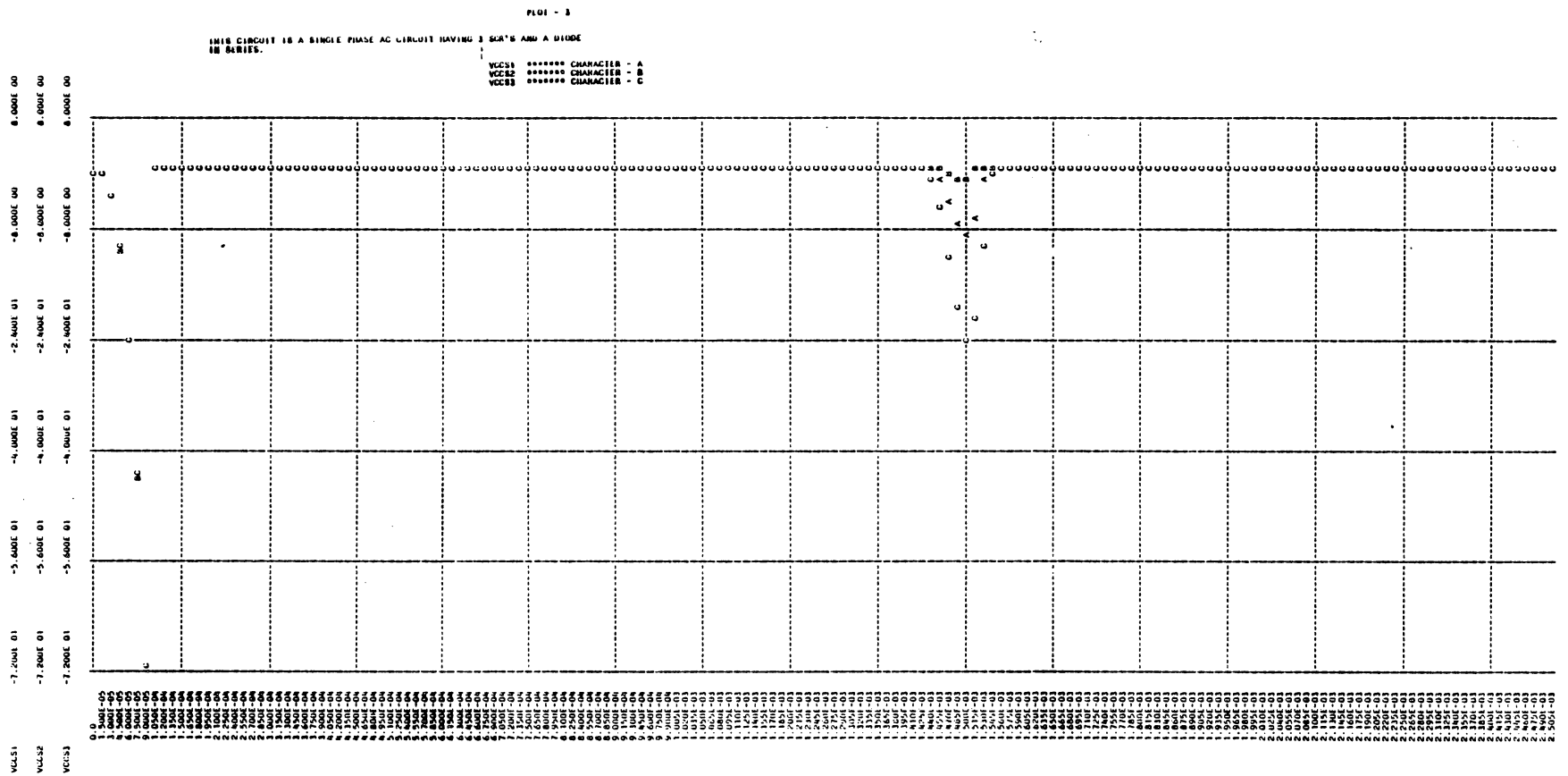


Fig. 6.4. (part 2 of 2)

6.2 A Three Phase AC Resonant Charging Circuit.

As mentioned previously, simulating Silva's circuit design requiring 42 SCR's in a 3-phase system exceeds SCEPTRE capacities using the SCR model of Fig. 5.6. Even an SCR/Diode combination such as that of Fig. 6.3 would require 18 SCR's which would again approach some SCEPTRE capacity limits. For this reason, a 3-phase ac resonant charging circuit was simulated using only six SCR's. This circuit is shown in Fig. 6.5. Phase voltages were changed to 1000V - 1000Hz to accommodate the reduced number of SCR's and to have a shorter transient CPU time for one complete cycle of the source.

Fig. 6.5 shows two branches of each phase bank charging array. The capacitors are discharged by the switches during alternate half-cycles of the phase sources. The actual circuit used thyration discharge switches, but a non-linear resistor was simulated via subroutine FGEN. (Fig. 6.1) for this report.

Preliminary circuit design revealed that the conducting half-cycle SCR would turn-off during discharge of the alternate half-cycle capacitor in each phase bank array. CAD revealed that the problem was the discharge current limiting resistors, R1A, R2A, ..., etc. These resistors were originally inserted in series with the charging capacitors, C1A, C2A, ..., between RSW1A, RSW2A, ..., when these switches were closed, the line to neutral voltage dropped suddenly causing the conducting SCR to commutate.

The solution was to move the current limiting resistors to be in series with the thyrations and neutral.

Simulation results are presented in Fig. 6.8 for each phase bank array. The usefulness of CAD is emphasized in the simulations of phases B and C.

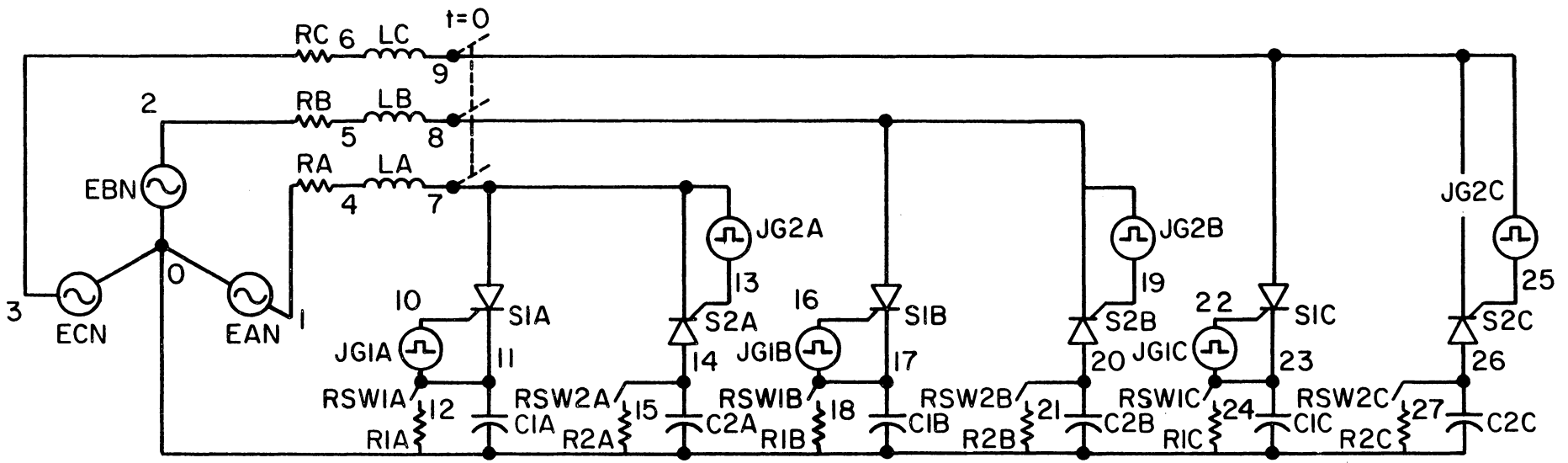


Figure 6.5 A Three Phase Resonant Charging Circuit.

```
CIRCUIT DESCRIPTION
ELEMENTS
EAN,0-1=X1(1.D3*DSIN(6285.18*TIME))
RA,1-4=1.
LA,4-7=5.897E-2
EBN,0-2=X2(1.D3*DSIN(6285.18*TIME-2.094))
RB,2-5=1.
LB,5-8=5.897E-2
ECN,0-3=X3(1.D3*DSIN(6285.18*TIME+2.094))
RC,3-6=1.
LC,6-9=5.897E-2
S1A,7-10-11=MODEL SCR
S2A,14-13-7=MODEL SCR
C1A,11-0=.43D-6
C2A,0-14=.43D-6
R1A,12-0=11.
R2A,15-0=11.
JG1A,11-10=FGEN(.2,0.,0.,1.D-4,1.D-3,TIME,0)
JG2A,7-13=FGEN(.2,0.,5.D-4,1.D-4,1.D-3,TIME,0)
RSW1A,11-12=FGEN(1.D7,0.,-2.25D-4,9.75D-4,1.D-3,TIME,1)
RSW2A,14-15=FGEN(1.D7,0.,-7.25D-4,9.75D-4,1.D-3,TIME,1)
S1B,8-16-17=MODEL SCR
S2B,20-19-8=MODEL SCR
C1B,17-0=.43D-6
C2B,0-20=.43D-6
R1B,18-0=11.
R2B,21-0=11.
JG1B,17-16=FGEN(.2,0.,3.33D-4,1.D-4,1.D-3,TIME,0)
JG2B,8-19=FGEN(.2,0.,-1.67D-4,1.D-4,1.D-3,TIME,0)
RSW1B,17-18=FGEN(1.D7,0.,-8.92D-4,9.75D-4,1.D-3,TIME,1)
RSW2B,20-21=FGEN(1.D7,0.,-3.92D-4,9.75D-4,1.D-3,TIME,1)
S1C,9-22-23=MODEL SCR
S2C,26-25-9=MODEL SCR
C1C,23-0=.43D-6
C2C,0-26=.43D-6
R1C,24-0=11.
R2C,27-0=11
JG1C,23-22=FGEN(.2,0.,6.67D-4,1.D-4,1.D-3,TIME,0)
JG2C,9-25=FGEN(.2,0.,1.67D-4,1.D-4,1.D-3,TIME,0)
RSW1C,23-24=FGEN(1.D7,0.,-5.58D-4,9.75D-4,1.D-3,TIME,1)
RSW2C,26-27=FGEN(1.D7,0.,-.58D-4,9.75D-4,1.D-3,TIME,1)
OUTPUTS
EAN,VC1A,VC2A,ILA,PLOT1
EBN,VC1B,VC2B,ILB,PLOT2
ECN,VC1C,VC2C,ILC,PLOT3
RUN CONTROLS
INTEGRATION ROUTINE = IMPLICIT
PLOT INTERVAL = 1.E-5
MAXIMUM PRINT POINTS=0
STOP TIME=1.E-3
MINIMUM STEP SIZE = 1.E-30
END
```

Fig. 6.6. SCEPTRE INPUT CIRCUIT DESCRIPTION FOR THE CIRCUIT OF FIGURE 6.5.

AC RESONANT CHARGING SYSTEM TIMING DIAGRAM

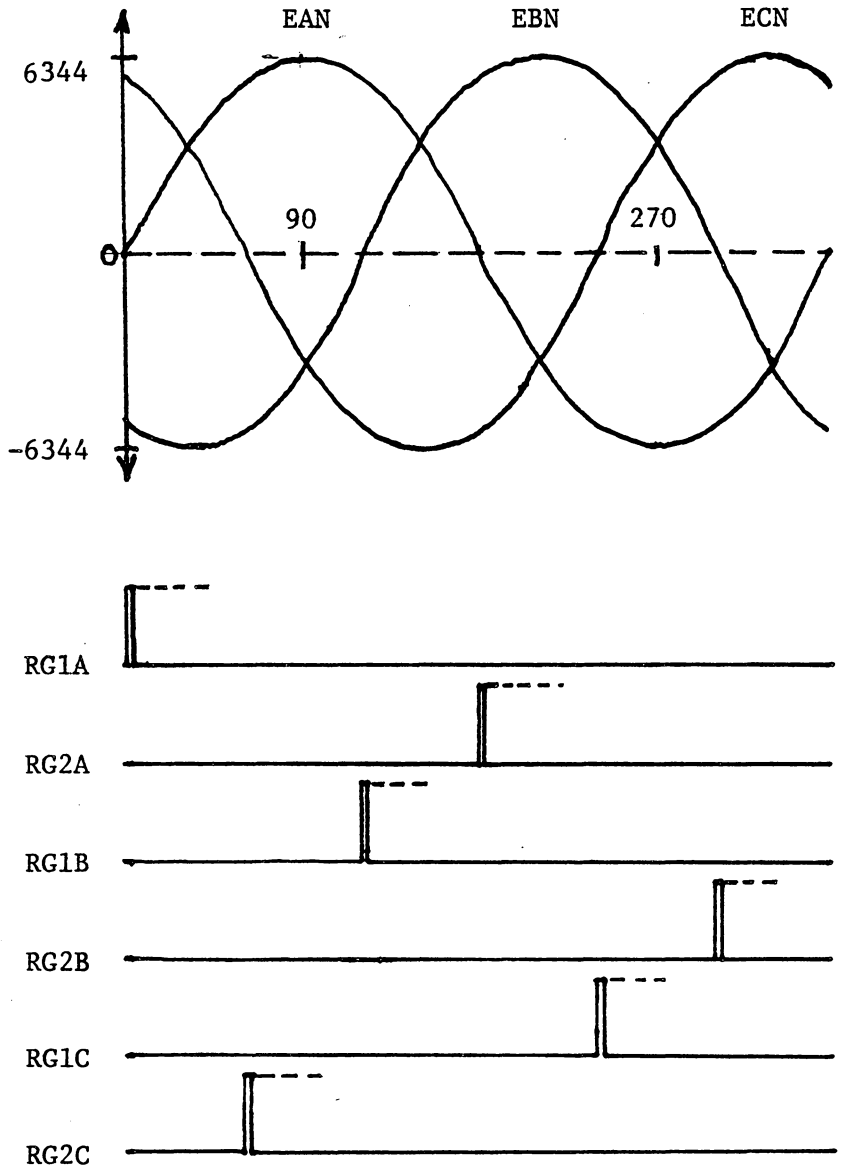


Fig. 6.7. TIMING DIAGRAM FOR GATE SOURCES OF FIG. 6.5

EAN	-1.000E 03	-6.000E 02	-2.000E 02	2.000E 02	6.000E 02	1.000E 03
VC1A	0.0	4.000E 02	8.000E 02	1.200E 03	1.600E 03	2.000E 03
VC2A	-2.000E 02	2.000E 02	6.000E 02	1.000E 03	1.400E 03	1.800E 03
ILA	-3.000E 00	-1.800E 00	-6.000E-01	6.000E-01	1.800E 00	3.000E 00

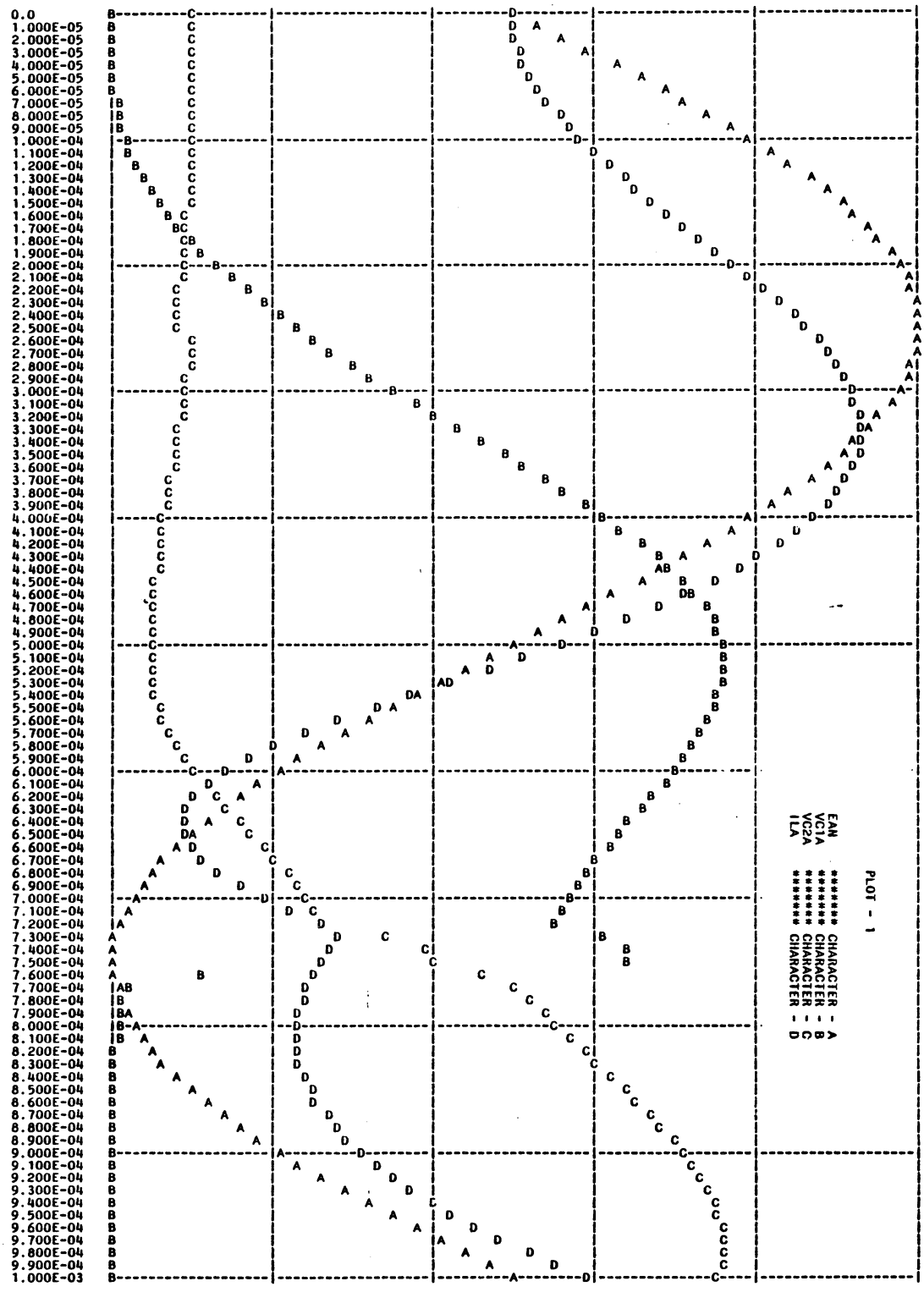


Figure 6.8 SCEPTRE Simulation for the Three Phase AC Resonant Charging Circuit of Figure 6.5 (page 1 of 3). Phase A.

EBN	-1.000E 03	-6.000E 02	-2.000E 02	2.000E 02	6.000E 02	1.000E 03
VC1B	-2.000E 02	2.000E 02	6.000E 02	1.000E 03	1.400E 03	1.800E 03
VC2B	-1.800E 02	0.0	1.800E 02	3.600E 02	5.400E 02	7.200E 02
ILB	-3.000E 00	-1.800E 00	-6.000E-01	6.000E-01	1.800E 00	3.000E 00

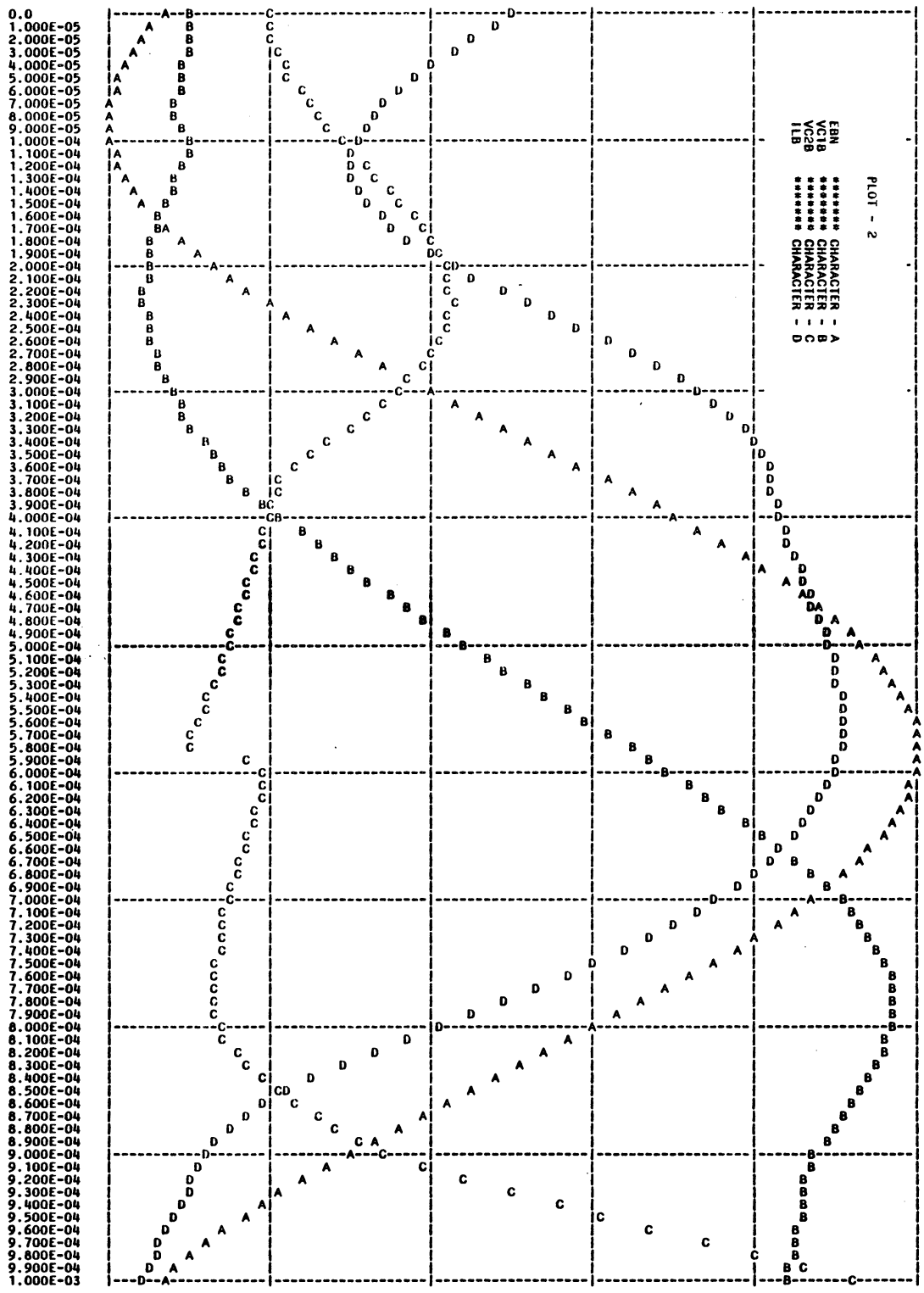


Figure 6.8 (page 2 of 3) Phase B.

ECN	-1.000E 03	-6.000E 02	-2.000E 02	2.000E 02	6.000E 02	1.000E 03
VC1C	-2.000E 02	2.000E 02	6.000E 02	1.000E 03	1.400E 03	1.800E 03
VC2C	-2.000E 02	2.000E 02	6.000E 02	1.000E 03	1.400E 03	1.800E 03
ILC	-3.000E 00	-1.800E 00	-6.000E-01	6.000E-01	1.800E 00	3.000E 00

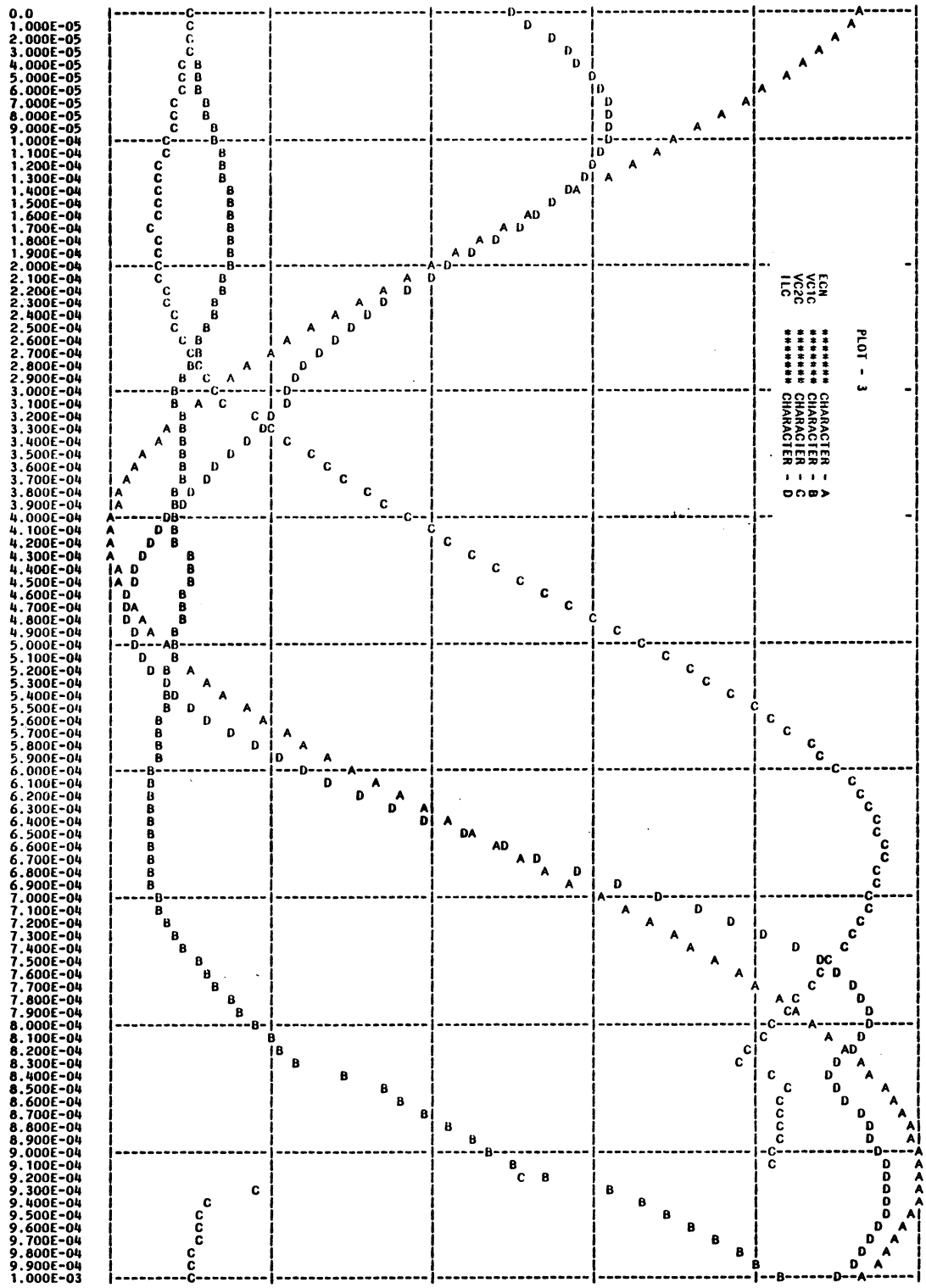


Figure 6.8 (page 3 of 3) Phase C.

The charging array is brought on line at time t = 0, but SCR firing is synchronized to phase voltage zero crossing. Consequently, phase inductance/snubber capacitor resonant behavior results in non-zero phase inductor currents at the time of firing of the appropriate SCR.

CPU time for one cycle of the 1KHz sources was 16 min., 8.9 seconds.

6.3 Summary and Conclusion

This chapter has presented an investigation into simulation of large SCR circuits with SCEPTRE.

It was determined that in general some form of scaling may be required to reduce simulation run times.

Looking at simulating three SCRs in series, it was observed that the time step selection appears to be the dominant cause of CPU time usage rather than network size for this configuration. It was determined that a 3-Ø AC resonant charging system containing six SCRs could be simulated without exceeding SCEPTRE network size constraints or encountering numerical problems.

In spite of the degraded accuracy of the dV/dt and t_q prediction, the model was shown to be a useful SCEPTRE design aid in situations where the potential for such a problem exists. This potential was shown here when a circuit design error in the

discharge path of the output capacitor of a 3Ø AC resonant charging circuit produced unexpected commutation of a conducting SCR.

It is important to note that the referred to inaccuracies in the model are not inabilities to simulate dV/dt and t_q but the inability of the parameter prediction procedure to produce accurate parameters for the characterizations.

CHAPTER 7

A DC RESONANT CHARGING SYSTEM

Fig. 7.1 shows a DC resonant charging system. A full-bridge controlled rectifier circuit provides DC voltage to a resonant charging load circuit. As for the 3Ø AC system discussed previously, Silva's circuit source was 6465V/400Hz whereas the simulation circuit is 1000V/1000Hz. The switch SW1 simulates a thyration discharge switch.

One cycle of the source is simulated to demonstrate each rectifier switch firing, then the charging capacitor is discharged. Simulation results are shown in Figure 7.4.

CPU time for the simulation was 17 min., 33.84 seconds.

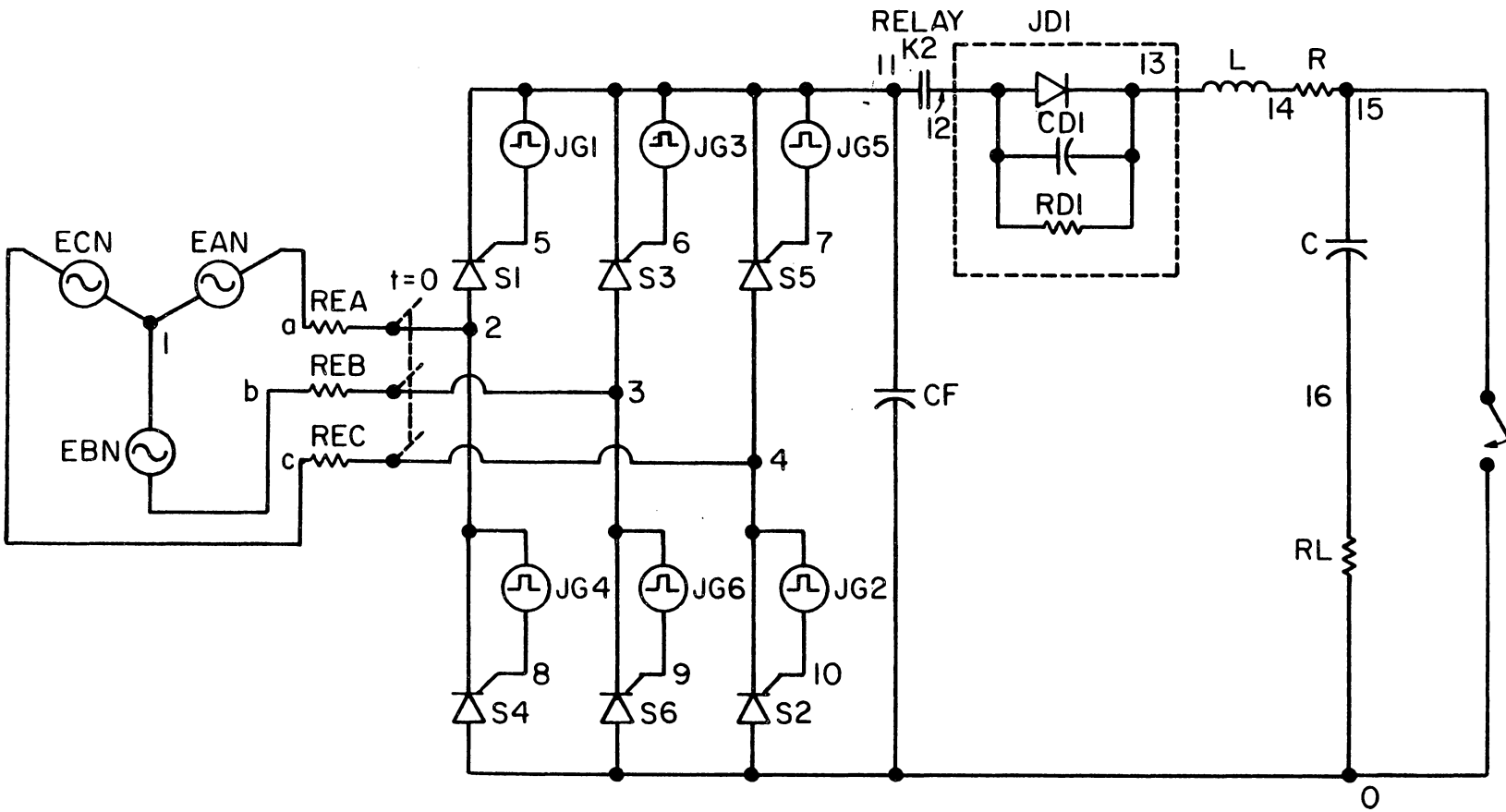


Figure 7.1 A DC Resonant Charging System.

DC RESONANT CHARGING SYSTEM TIMING

DIAGRAM

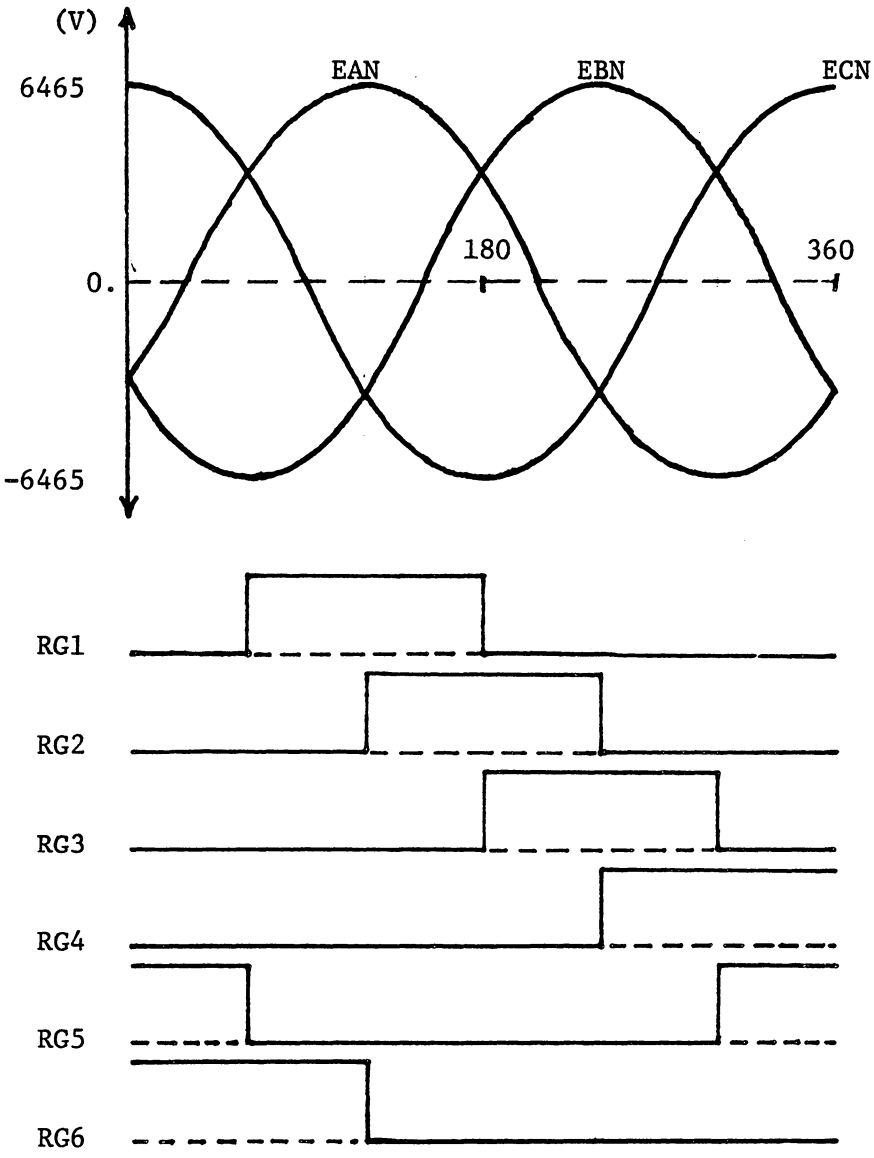


Fig. 7.2. GATE TRIGGER DIAGRAM FOR FIG. 7.1.

```
MODEL DESCRIPTION
MODEL RLY1(1-2)
THIS MODEL REPRESENTS RELAY K2 IN JAMIE SILVA'S CIRCUIT
ELEMENTS
R,1-2=TABLE 1
FUNCTIONS
TABLE 1
0.,1.E8,2.5E-5,1.E8,2.5E-5,0.,2.E-3,0.
MODEL DESCRIPTION
MODEL RLY2(1-2)
THIS MODEL REPRESENTS SWITCH SW1 IN JAMIE SILVA'S CIRCUIT
ELEMENTS
R,1-2=TABLE 1
FUNCTIONS
TABLE 1
0.,0.,2.0E-5,0.,2.5E-5,1.E8,1.E-3,1.E8,1.E-3,0.,1.02E-3,0.,1.02E-3,
1.E8,2.E-3,1.E8
CIRCUIT DESCRIPTION
THIS CIRCUIT SIMULATES A 1000V/1KHZ RESONANT CHARGING PULSE POWER
SYSTEM.
ELEMENTS
EAN,1-A=X1(1.D3*DSIN(6285.18*TIME-5.236D-1))
REA,A-2=1.
EBN,1-B=X2(1.D3*DSIN(6285.18*TIME-2.618))
REB,B-3=1.
ECN,1-C=X3(1.D3*DSIN(6285.18*TIME+1.5708))
REC,C-4=1.
S1,2-5-11=MODEL SCR
S2,0-10-4=MODEL SCR
S3,3-6-11=MODEL SCR
S4,0-8-2=MODEL SCR
S5,4-7-11=MODEL SCR
S6,0-9-3=MODEL SCR
JG1,11-5=FGEN(.2,0.,1.67E-4,3.33E-4,1.E-3,TIME,1)
JG2,4-10=FGEN(.2,0.,3.33E-4,3.33E-4,1.E-3,TIME,1)
JG3,11-6=FGEN(.2,0.,5.00E-4,3.33E-4,1.E-3,TIME,1)
JG4,2-8=FGEN(.2,0.,6.67E-4,3.33E-4,1.E-3,TIME,1)
JG5,11-7=FGEN(.2,0.,-1.67E-4,3.33E-4,1.E-3,TIME,1)
JG6,3-9=FGEN(.2,0.,0.,3.33E-4,1.E-3,TIME,1)
CF,11-0=7.5E-9
K2,11-12=MODEL RLY1
JD1,12-13=DIODE Q(1.D-8,38.61)
CD1,12-13=5.D-9
RD1,12-13=1.D4
L,13-14=.173
R,14-15=1.E-2
SW1,15-0=MODEL RLY2
CO,15-16=.586E-6
RL,16-0=1.82
OUTPUTS
EAN,VCF,IRL,VCO,PLOT1
IREA,IREB,IREC,PLOT2
RUN CONTROLS
RUN INITIAL CONDITIONS
INTEGRATION ROUTINE = IMPLICIT
PLOT INTERVAL = 1.E-5
MAXIMUM PRINT POINTS=0
STOP TIME=1.02E-3
MINIMUM STEP SIZE = 1.E-30
END
```

Fig. 7.3. SCEPTRE INPUT LISTING FOR THE DC RESONANT CHARGING SYSTEM OF FIG. 7.1.

EAN	-1.000E 03	-6.000E 02	-2.000E 02	2.000E 02	6.000E 02	1.000E 03
VCF	1.140E 03	1.260E 03	1.380E 03	1.500E 03	1.620E 03	1.740E 03
IRL	-2.800E 00	-1.400E 00	0.0	1.400E 00	2.800E 00	4.200E 00
VCO	0.0	8.000E 02	1.600E 03	2.400E 03	3.200E 03	4.000E 03

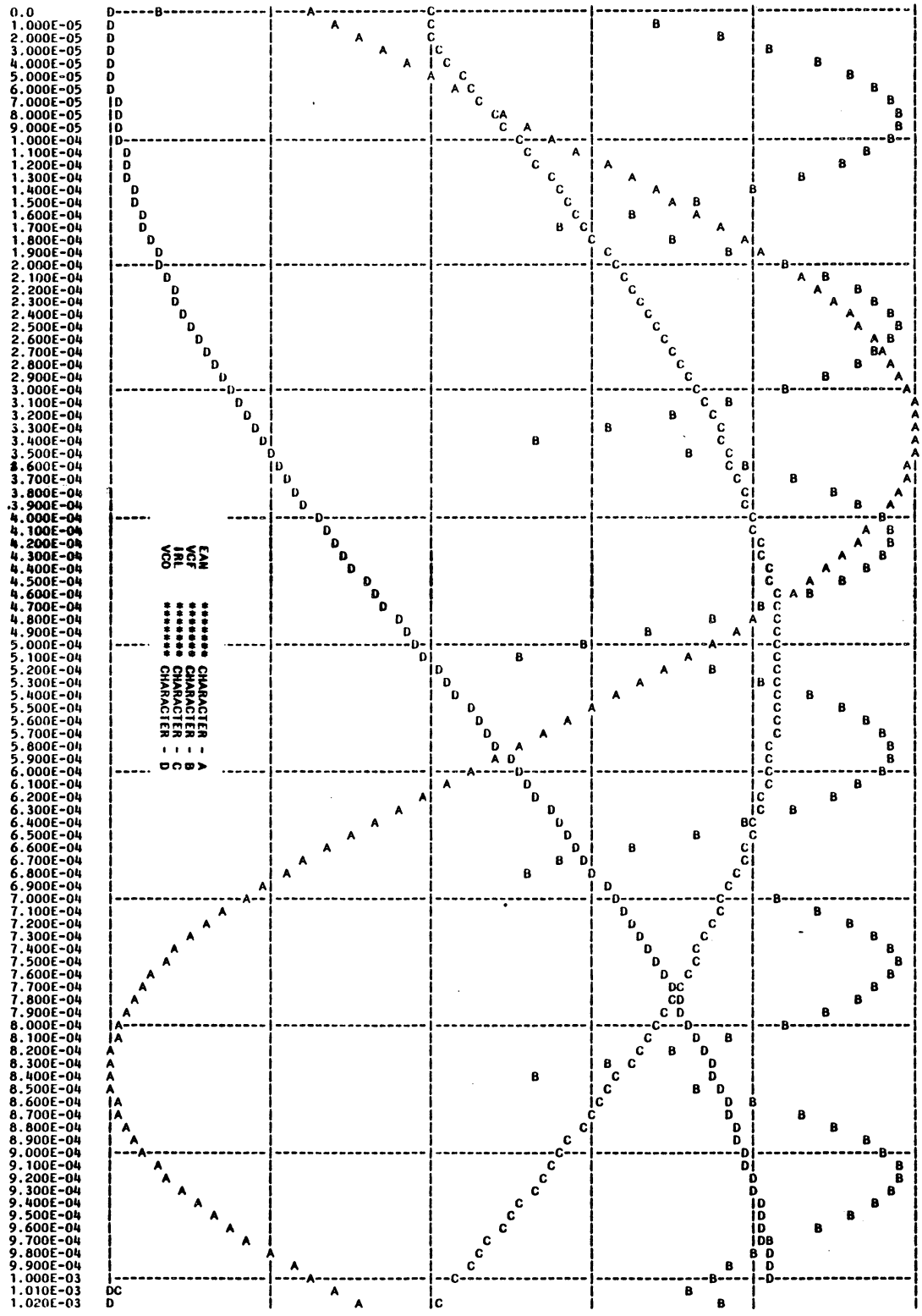


Figure 7.4 Simulation Results of the DC Resonant Charging System of Figure 7.1 (page 1 of 2). Output Voltage.

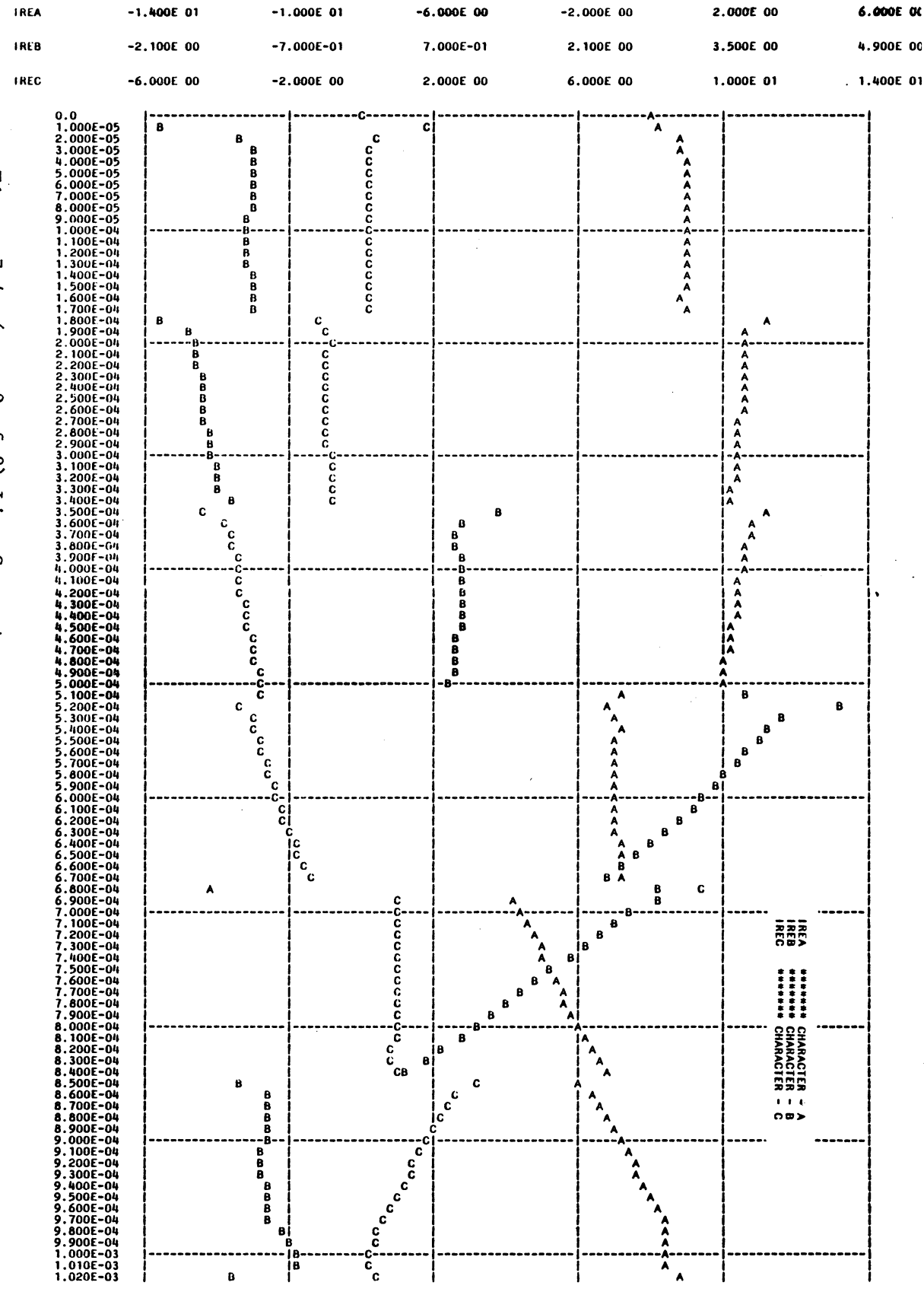


Figure 7.4 (page 2 of 2) Line Currents.

CHAPTER 8

A UNIFIED SCR MODEL FOR CONTINUOUS TOPOLOGY CADA

8.1 Introduction

The SCR continues to be a work horse of the high-power processing electronics industry. More and more designers are turning to CADA to tackle the complexities of design of the intricate SCR circuits. SPICE2 and SUPER-SCEPTRE have emerged as offering a combined across the board circuit analysis capability [28]. Non-linear circuit element SCR models for SPICE2 typically employ a two-transistor configuration [1,12,23,28] to take advantage of the parameter specification capability of the built in transistor model. On the other hand SCR modeling for use with S*S (SUPER-SCEPTRE) is typically structured around a three diode (or more) configuration [2,8,24] which is representative of the intrinsic three P-N junction structure of the PNPN SCR construction.

This chapter presents the J^3 SCR model (J^3 - notation used to denote the use of the intrinsic three-junction configuration), a uniform circuit model analog and parameter estimation procedure to both SPICE2 and S*S. This uniformity enhances the circuit designers flexibility in shifting his analysis selectively among the two programs thus optimizing utilization of each programs respective merits. The intrinsic three-junction configuration provides better visualization of the models performance and understanding of the significance of the parameters. Additionally, correlation of device characteristics and parameters to the physical properties of each junction provides a more

flexible model for future enhancement or alteration to model new or alternative devices.

The J^3 SCR model provides improved simulation of SCR dv/dt and commutation characteristics. Previous models [1,2,3,8,12] provide extensive treatment of SCR turn-on characteristics but lose rigor when approaching the turn-off transient. This is because turn-on starts from a known state but turn-off is significantly more difficult to quantify. The previously referenced models have treated this area primarily from a trial and error approach until arriving at a set of parameters which produced reasonable results for the devices selected for simulation. Selection of another device or alteration of some interactive parameter of the model can lead to poor performance of the model. Close examination of the models network dynamic equations is performed to establish the critical parameters necessary to define turn-off behavior in terms of commutation time and reapplied dv/dt performance. An analytical basis for parameter quantification is established.

8.2 Advantages vs. Disadvantages of Neinhus' and Hu's SCR Models

The J^3 SCR model unifies the conceptual approaches to modeling used by Neinhus [8] and that used by Hu [12]. The resulting model is thus endowed with their respective advantages while extended development has been performed to remove some of their disadvantages.

Neinhus' and Hu's SCR models are summarized

Neinhus' SCR model [8]

Advantages

- Built around intrinsic three junction structure thus providing flexibility for adaptation to other CAD programs and/or modifications of the model.
- Highly accurate turn-on transient simulation of delay time, rise time, and spreading time of the SCR anode current.
- Highly accurate on-state anode to cathode non-linear voltage drop simulation.
- Simulates SCR characteristics of t_d, t_r, t_s, t_q, I_{GT}, I_H, I_L, and V_{on}.
- Model is convertible to SPICE2 with moderate effort.

Disadvantages

- Determination of parameters requires laboratory measurements of an actual device. The procedure requires approximately two days to perform via an expensive laboratory facility [37].
- Model network is too large to allow SCEPTRE simulations requiring several SCR's.
- dv/dt, V_{BO}, $V_{(BR)R}$, V_{GRM}, and turn-off transient either not simulated or not well defined.
- Extremely small network time constants lead to inefficient computational performance [9].
- May need to specify initial conditions of junctions at start-up [8].

Hu's SCR model [12]

Advantages

- Simulates SCR characteristics of t_r, I_H, I_{GT}, V_T, R_{on}, $V_{(BO)}$, dv/dt, t_q.
- Uses SPICE2 built in transistor model in basic two-transistor representation of SCR [14]. This results in good computational efficiency when used with SPICE2 and eliminates the need to specify detailed initial conditions.
- Parameter estimation procedure is easily accomplished by a short calculation and graphical procedure based on manufacturer's spec sheet data. No physical measurement is required.

Disadvantages

- SCR turn-off transient simulation is inaccurate and may have stability problems [23].
- Conversion of the node voltage based model to use with state variable based analysis is not straight-forward [24]. The resulting network is too large to allow simulation of circuits containing several SCR's. Also additional approximations are required when making the conversion which degenerate the models accuracy. Key areas of degenerated performance are:
  - The addition of a state-variable capacitor [24] from gate to cathode to meet SCEPTRE programming requirements causes degraded dv/dt performance.

- Substantial rearrangement of the circuit configuration of the "modified Hu-ki" model (Fig. 2.5) and removal of all non-essential elements to reduce the equivalent network to the three junction model (Fig. 5.10) results in degraded t_q prediction.

This loss of accuracy while not intolerable is undesirable.

- The turn-on characteristic curve predicted by Hu's model has a notable lack of a delay time, t_d, feature.
- $V_{(BR)R}$, V_{GRM}, I_L, and t_s not simulated.
- Model is not keyed to intrinsic three junction structure of the SCR. This makes alteration or expansion of the model awkward.
- Parameter estimation procedure employed much empirical practice in its development.

8.3 Development of the J^3 SCR Model

To develop the J^3 SCR model a new look is taken at the fundamental development of both Hu's model and Neinhus' model. The objective is to develop a non-linear SCR model circuit analog and parameter estimation procedure that:

. provides reasonably accurate computer prediction of the three major dynamic performance characteristics of the SCR, gate driven turn-on, static dv/dt turn-on, and the turn-off

. predicts commutation interval as determined by reapplied dv/dt.

. is applicable to high power phase control and inverter SCR's.

- allows use of manufacturer's spec sheet data and basic semiconductor theory to assign model parameters.
- has numerical computational efficiency emphasized during development.
- uses a minimum number of elements in the circuit analog in order to allow simulation of large circuits by programs with total topology restrictions.
- has a uniform or near uniform topology when adapted to use with various CADA programs.
- uses the diode representation of PN junctions as the fundamental building block of the circuit analog. This is particularly important in SPICE2 which requires use of built in element models. SPICE2 has no junction breakdown simulation in PN junction models other than in its diode model.
- provides reasonable simulation SCR characterizations such as R_{on}, I_{GT}, I_H, V_{on}, $V_{(BO)}$, $V_{(BR)R}$, and V_{GRM}.
- is a terminal characteristics model.

The expressions "SCR model" and "model" as used in this work denote both the circuit analog and the parameter estimation procedure of the model.

Generally speaking, no SCR model is unique. That is to say that the operation of modeling is an exercise in non-linear circuit design. If it is properly designed, then the computer simulation of the circuit can do little more or less than to reproduce the numbers which were used to design the circuit.

The CADA programs to be used in development and analysis of the J^3 model are SPICE2 and SUPER-SCEPTRE. These two programs are selected because combined they represent an across the board non-linear circuit analysis capability and are widely known and accepted in practice [28]. The model is, however, universal in its development around the basic diode relations without orientation to any specific computer program.

Choice of a uniform circuit configuration for the J^3 SCR model is suited to the more topologically restrictive program, SUPER-SCEPTRE. The 300 element, 301 node limitation of circuit size [7], the capacitor state variable dependence requirement for voltage dependent non-linear current sources [7], the number of sources limitation [16], and the DC initial conditions solution requirements [19] for SUPER-SCEPTRE make the intrinsic three diode circuit configuration (Fig. 5.10) the better choice over the two transistor configuration (Fig. 2.5).

Due to the variety of SCR devices available, simulation, while based on semi-conductor physical properties (at 25°C), is aligned to first order terminal characteristics with dv/dt and commutation of primary interest.

8.4 J^3 SCR Model Circuit Analog

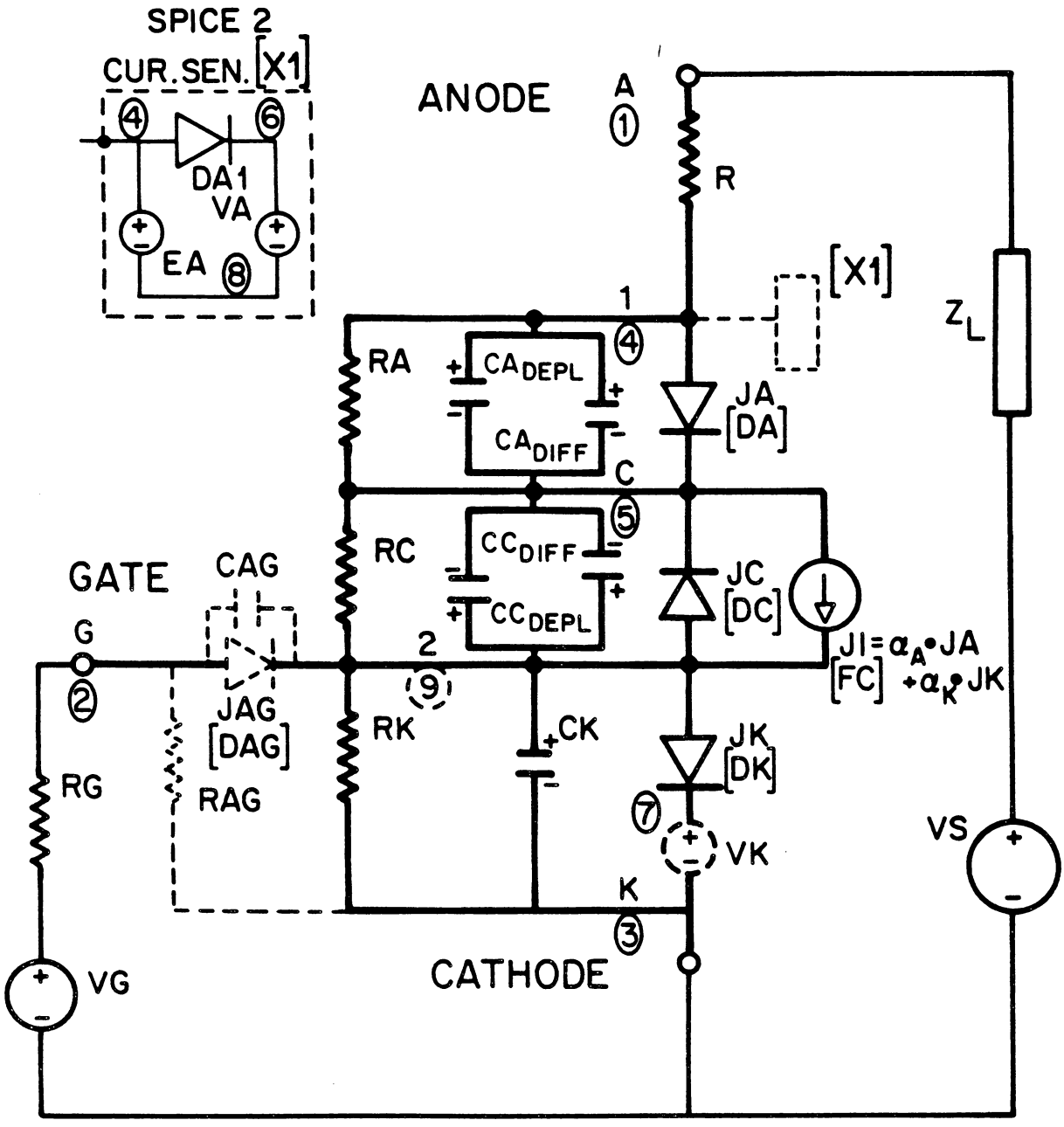
The circuit analog for the J^3 model is shown in Fig. 8.1. The model is shown with a common cathode connection with external gate and anode circuits. Elements are designated by symbols appropriate to SPICE2 and SCEPTRE input format.

Current Sensors for SPICE2

Elements DA1, EA, and VA shown as X1 in Fig. 8.1 are a programming aid to SPICE2. They act as a current sensor for DA current, one of the two independent variables for the linearly dependent current source, FC, used in SPICE2 input. SPICE2 provides that for current dependent current sources, the independent current variable must be the current through a voltage source [38]. Zero valued voltage sources VA and VK are provided for that purpose. The need for DA1 and EA arises from the use of the SPICE2 built in diode model to simulate the anode junction and its associated capacitances, CA_{DEPL} and CA_{DIFF}. In order to avoid inclusion of capacitance displacement currents in the independent current variable representing the injected currents of DA in FC, an auxiliary diode element, DA1 is used to provide the required independent current variable flowing through VA.

A similar operation of the gate to cathode junction simulated by DK is only required if the junction capacitance is included in the diode model. Since CK has been made linear in the J^3 model, then the current sensor voltage source, VK, may be placed in series with DK and CK inserted as a parallel capacitor external to the diode model.

SCEPTRE current dependent current sources may use any branch current as the independent variable. No special action is required.



---- JAG,RAG, & CAG are optional Model Elements. EA, DA1, VA & VK are SPICE 2 programming aids only.

O SPICE 2 node numbers. Add node (9) if using amplifying gate elements.

[ ] SPICE 2 Circuit Element Designator if different from SCEPTRE.

Fig. 8.1. The J^3 SCR Model.

Optional Amplifying Gate Structure

Also appearing as dotted lines in the model are the elements, JAG[DAG], CAG, RAG. These elements are optional. Two purposes are served by their inclusion. Including the diode, JAG[DAG], prevents reverse gate current as is the case in the amplifying gate SCR. Since SCEPTRE has a requirement to provide a voltage state variable as the source of the independent variable in a primary voltage-dependent-current-source, then CAG must be provided with SCEPTRE.

The resistor, RAG, in conjunction with the diode, JAG[DAG], and capacitor, CAG, also provide a means of correcting an error that may occur in computer simulation of the DC gate threshold current, I_{GT}, characteristic for some SCRs. This is discussed more thoroughly in a later section.

Initial Conditions Convergence Aids

The resistors RA and RC are provided in the model as programming aids to allow good convergence of DC initial conditions solutions when using SCEPTRE. RA and RC are assigned high values to avoid influence on the model performance.

The user may change these values if desired, however, it is recommended that the ratio RA/RC remain very small in order to insure that the initial conditions solution has negligible forward bias to JA[DA]. Otherwise, the model will have degraded turn-on transient performance.

Primary Model Elements

The remaining eleven circuit elements of the model are the primary concern of this thesis. Although the optional elements are to be included, generally speaking, the J^3 SCR model as developed here will give only token consideration to these elements. This is because they are not particularly significant to overall model performance and may be the prohibiting factor in simulating large circuits having several SCRs.

One other thing should be noted at this time. Virtually all SCRs have snubber circuits. The circuit modeler is well advised to include the snubber circuit as part of the model, thereby eliminating a great deal of tedious network programming as input to SPICE2 or SCEPTRE.

The circuit analog for the SCR model was derived through the results of previous chapters and the conclusions of the references.

The parameter estimation procedure is analytically derived in this chapter. As has been previously stated, the fundamental building block of the model is the basic diode model as defined by equations (8.1) and (8.2).

8.4.1 Basic Diode Equation

$$I_D = \left.\frac{I_s\left(e^{V_D/\theta} - 1\right)}{1 - \left(V_D/V_{BO}\right)^n}\right| \approx \left. I_s e^{V_D/\theta}\right|_{V_D>0} \qquad (8.1)$$

$$\left.\begin{array}{l} \theta = .026V \text{ @ } 300°K \\ 1.5 < n < 6.5 \\ V_{BO} < V_D < 0 \end{array}\right|$$

The denominator term $1 - (V_D/V_{BO})^n$ in (8.1) is used to model diode breakdown theoretically. It is impractical in computer simulation since convergence to a solution point with $|V_D| > |V_{BO}|$ will result in an erroneous result. Even with use of special routines to avoid V_{BO} overshoot, time step values often become extremely small thus destroying numerical efficiency.

Typically, an exponential relation is substituted for the true theoretical expression thus making a small sacrifice in accuracy to avoid overshoot and provide a somewhat less stiff transient for the numerical algorithm.

8.4.2 Diode Incremental Capacitance

$$C_D = (d/dV_D)[Q_{DEPL} + Q_{DIFF}]$$

$$= C_{DEPL_o}/[1 - V_D/\psi_o]^{1/2}\Big|_{V_D < \psi_o} + (\tau_D I_S/\theta)e^{V_D/\theta}\Big|_{V_D > 0} \qquad (8.2)$$

$$\Big|_{\psi_o \approx .75V(\text{defaulted to } 1.0)}$$

In many cases, the values of the capacitance terms control the system time constants and consequently the numerical algorithm time step. SPICE2 and SCEPTRE have variable time step algorithms which allow the time step to be controlled by system dynamics. In this case, it is only during the periods of high dynamic activity such as SCR switching or commutation that the model's capacitance terms should control the time step in order to assure accurate transient simulation.

In previous models, the depletion layer incremental capacitance terms as defined by C_{DEPL} in (8.2) have been made very small (usually arbitrarily small) on the order of picofarads. This is contradictory to the objective of having long time steps in periods of rapid transient behavior. The J^3 model will therefore be oriented to maximizing the depletion layer incremental capacitance terms.

Analysis of the models network analog is done using the basic Kirchoff's current and voltage laws along with the principle of superposition. The following nodal and loop equations are generated to facilitate analysis (refer to Fig. 8.1 for network reference numbers) of the model without the optional gate circuit components.

8.4.3 Node Current Equations

NODE A [1]

$$I_A = [VS - I_A Z_L - V_{CA} + V_{CC} - V_{CK}]/R \tag{8.3}$$

NODE 1 [2]

$$= I_{CA} + JA = \frac{d\,Q_{CA}}{dt} + JA$$

$$= \left[\frac{CA_{DEPL_0}\,(1-V_{CA}/2)}{(1-V_{CA})^{3/2}} + \frac{\tau_A I_{SA}}{\theta_A}\, e^{V_{CA}/\theta_A}\right] \frac{d\,V_{CA}}{dt}$$

$$+ I_{SA} e^{V_{CA}/\theta_A} \tag{8.4}$$

NODE C [3]

$$= -I_{CC} - J_C + \alpha_A JA + \alpha_K JK$$

$$= -\left[\frac{CC_{DEPL_0}\,(1-V_{CC}/2)}{(1-V_{CC})^{3/2}} + \frac{\tau_C I_{SC}}{\theta_C}\, e^{V_{CC}/\theta_C}\right] \frac{d\,V_{CC}}{dt}$$

$$- I_{SC} e^{V_{CC}/\theta_C} + \alpha_A I_{SA} e^{V_{CA}/\theta_A} + \alpha_K I_{SK} e^{V_{CK}/\theta_K} \tag{8.5}$$

NODE G [4]

$$= -I_G + I_{RK} + I_{CK} + JK$$

$$= -I_G + \frac{V_{CK}}{RK} + CK\frac{d\,V_{CK}}{dt} + I_{SK} e^{V_{CK}/\theta_K} \tag{8.6}$$

NODE K [5]

$$I_K = I_A + I_G \tag{8.7}$$

8.4.4 Voltage Loop Equations

Load Loop

$$0 = VS - I_A Z_L - I_A R - V_{CA} + V_{CC} - V_{CK}$$

which is most useful expressed as:

$$VS(t_o) + \frac{dVS}{dt}\, t = (Z_L + R) I_A \Big| + \int_{t_o}^{t} \left(dV_{CA} + dV_{CC} + dV_{CK}\right) \qquad (8.8)$$

$$Z_L = \left\{ L_L \frac{d}{dt} + \frac{1}{C_L} \int_{t_o}^{t} dt + R_L \right\}$$

where for simplicity it is constrained that

$$Z_L = R_L$$

Gate Loop

Gate source is assumed to be a fixed amplitude pulsed voltage or current source.

$$0 = VG - I_G RG - V_{CK} \qquad (8.9)$$

$$= V_G - I_G RG - \int_{o}^{t} \frac{I_G - I_{RK} - JK}{CK}\, dt$$

8.4.5 Number of Required Parameters

Equations (8.1) → (8.9) show eighteen model parameters and seven external source and circuit parameters which must be known in order to program the network for computer solution. Three additional parameters, not shown in the equations, are required to provide the optional gate circuit elements. Also three special programming parameters for the SPICE2 current sensing components must be known along with two parameters for the DC initial conditions solution components.

The total of 33 parameters must be determined. Fortunately only 16 of these must be analytically determined. The remaining 17 may be given fixed values or read from specification sheets.

The methods for obtaining the parameters is developed in the following sections.

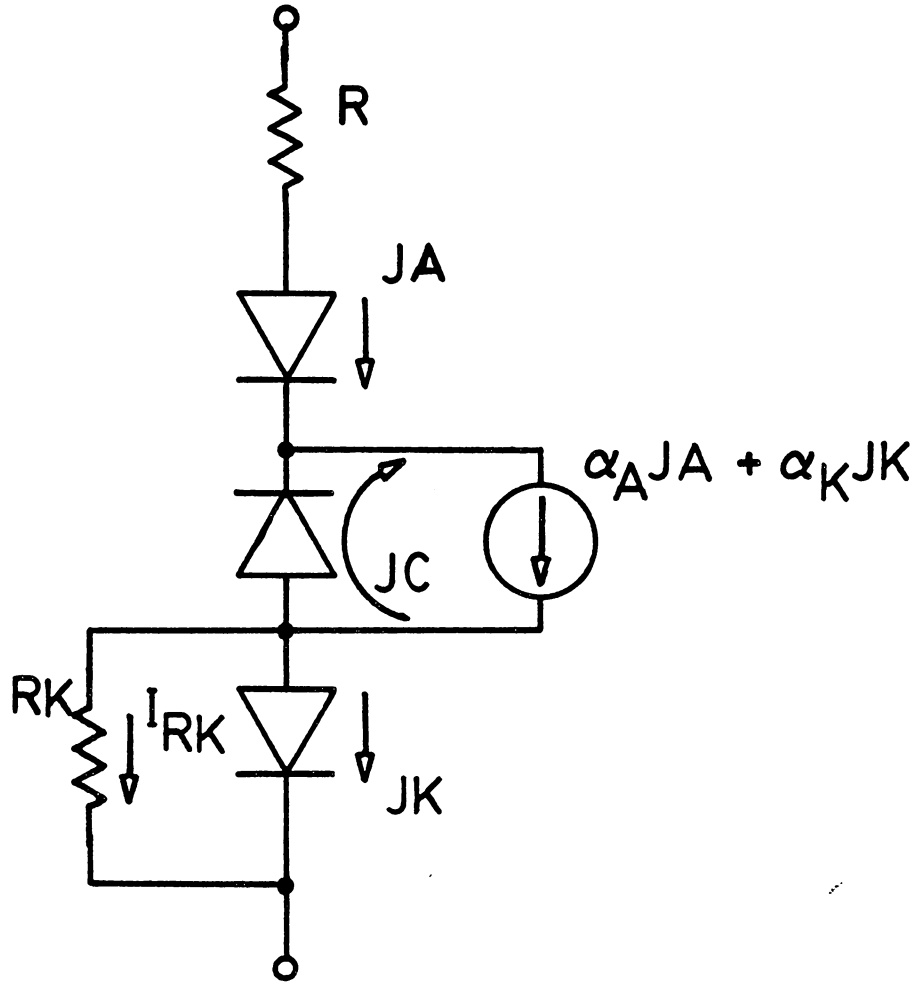


Fig. 8.2. Static State Equivalent Model.

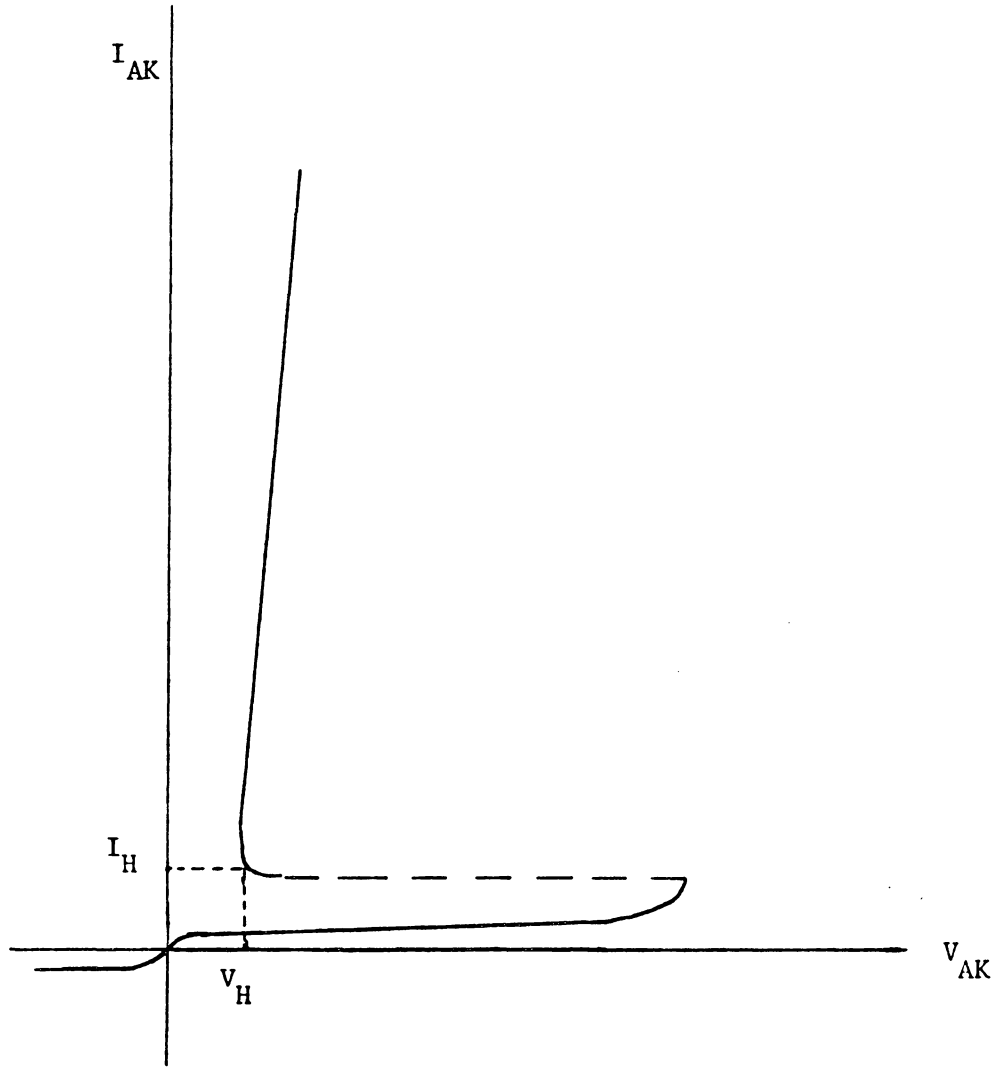


Fig. 8.3. SCR V-I CHARACTERISTIC CURVE.

8.5 Static Analysis

Static operation of the SCR model is defined as an operating state of which the $\frac{dv}{dt}$ of the capacitance terms is zero and I_A equals some constant value. The effective static model is given by Fig. 8.2.

Analysis of the static state model must be referenced to some known operating point. Specification sheet data provides such an operating point in the on-state operating point (V_H, I_H) depicted in Fig. 8.3.

At the operating point chosen, the dynamic equations (8.3) through (8.7) reduce to:

$$VS - I_H R_L = V_{AK} \qquad \therefore \quad I_H R_L \approx 0$$

$$\begin{aligned} I_A &= \left(V_{AK} - V_{CA} + V_{CC} - V_{CK}\right)/R = JA \\ &= -JC + \alpha_A JA + \alpha_K JK \\ &= I_{RK} + JK \end{aligned} \tag{8.10}$$

Using JA = I_H, and

$$RK = .75V/I_{GT} \quad [1],[8] \tag{8.11}$$

the equations in (8.10) produce the relationship

$$JC = (\alpha_A + \alpha_K - 1)I_H - \alpha_K I_{GT} \tag{8.12}$$

For the operating point, (V_H, I_H), the parameters α_A and α_K are at their maximum values [14]. The J^3 model does not provide for low current decrease in α. Although this effect could be modeled by adding an element between nodes G and 1 to simulate low current recombination in the gate and collector regions [8], it is not modeled to minimize the total element count. Also spec sheets do not provide adequate data to estimate required parameters.

The high current decrease in α values due to recombination in the gate and collector neutral regions does have a vehicle of simulation in the conduction of the then forward biased JC.

In order for the α's to be at their maximum values at (V_H, I_H), JC must be zero. For numerical purposes, a value much smaller than I_H, but still large enough to avoid numerical problems with predicting V_{CC} is selected as the value of JC instead of zero.

$$JC = .00001 \text{ A} = .10 \text{ ma} \tag{8.13}$$

This choice of JC will cause a .01 ma error in I_H simulation.

Using (8.13) in equation (8.12) and rearranging gives:

$$\alpha_A = 1 - \alpha_K + (\alpha_K I_{GT} + .01 \text{ ma})/I_H \qquad (8.14)$$

I_{GT}, I_H in ma

To insure the validity of the assumption in (8.11) that $I_{RK} = .75V/I_{GT}$ [1], α_K must be very near unity. This is physically reasonable based on the typically narrow gate region construction of the SCR. Values of $.9 < \alpha_K < 1.0$ would satisfy this constraint. For the convenience of decoupling the gate pulse current from JK, the value of $\alpha_K = 1.0$ appears desirable. Caution must be exercised here to insure that $\alpha_K = 1.0$ will not cause problems such as excessive V_{CK} during turn-on or greater dv/dt sensitivity. As will be shown later, there need not be any problems so the relation is made:

$$\alpha_K = 1.0 \qquad (8.15)$$

It appears that a direct subsitution of (8.15) into (8.14) will give a relationship from which to determine α_A from specification sheet data.

Before proceeding, however, an examination of data sheet values for I_{GT} and I_H reveals a quirk. Both quantities are usually given minimum, typical and maximum values. Investigation reveals that the relationship $I_{GT\text{-}max} < I_{H\text{-}max}$ is consistant. On the other hand the relationship between $I_{GT\text{-}typ}$ and $I_{H\text{-}typ}$ is inconsistant. This may result from manufacturer's measurement techniques or from unaccounted for factors in the model. This issue is not to be debated. The fact is that α_A cannot exceed, or for that matter, reach unity.

To resolve this dilemma, constraints are placed on the method of estimating α_A. Using typical values given in data sheets

$$\alpha_A = \begin{cases} (I_{GT} + .01 \text{ ma})/I_H & \text{for } I_{GT} \leq .95\ I_H \\ .95 & \text{for } I_{GT} > .95\ I_H \end{cases} \tag{8.16}$$

This brings up the function of RAG. In order to more accurately model the data sheet value of $I_{GT\text{-}typ}$ when $I_{GT\text{-}typ} > I_H$, the model user may add the resistor RAG along with diode JAG (DAG in SPICE2).

The required value of RAG is just

$$\text{RAG} = \begin{cases} 1.5 \text{ V}/(I_{GT} - .95\ I_H) & \text{if } I_{GT} > I_H \\ \infty & \text{if } I_{GT} < I_H \end{cases}$$

The parameter for JAG[DAG] is I_{SDAG} which is determined by having $V_{JAG} \approx .75V$ at $I_G \approx .1A$. This requires

$$I_{SDAG} \approx 3.0 \times 10^{-14} \text{ A}$$

$$\text{with } \theta = .026V$$

When JAG is used with SCEPTRE, CAG must be provided. CAG should be as large as practical without disturbing the rest of the model. One may get by with something on the order of one-tenth the value of CK to be determined later.

$$\text{CAG} \leq .1 \times \text{CK}$$

It is preferred that these elements be omitted and the decrease in accuracy of simulation for the gate circuit parameters be tolerated.

The values of JA, JC, and JK at (V_H, I_H) are predicted by (8.1). For each junction this requires the determination of two parameters I_S and θ. The determination of the parameters is constrained by the following.

In order for the SCR to be in static on-state, the center junction must not be negative biased. At (V_H, I_H) this means

$$V_{CC} = V_{CA} + V_{CK} - V_H \geq 0 \tag{8.17}$$

Since values of $V_{CA} = V_{CK} = .75V$ will ensure (8.17) for typical SCR's in static on-state,

$$V_{CC} = 1.5 - V_H \ .$$

Observing (8.13) and (8.17) parameter estimation for JA, JC, and JK begins with assigning certain parameter values which will be held constant no matter what device is being modeled. These parameters are assigned values normal to the device being modeled. While actual devices have some allowable range of variation for these parameters, the values to be used are chosen arbitrarily with convenience as the main criteria.

The parameter θ may range from .025V to .04V [8] depending on the width of the depletion region and the degree of two sided injection across the junction. The ideal, narrow depletion region single side injection assumption is used so that,

$$\theta_A = \theta_C = \theta_K = .026V \ @ \ T = 25°C = 300°K \tag{8.18}$$

These are SPICE2 Default Values

The model is developed with T = 25°C and no attempt is made to assess the effect of temperature variation although power SCRs may typically operate at T = 125°C.

The determination of I_{SA}, I_{SC}, and I_{SK} is by

$$I_{SA} = I_H e^{-.75V/\theta_A}$$

$$I_{SC} = 1.0 \times 10^{-5} e^{(V_H - 1.5V)/\theta_C} \quad \therefore \; I_{GT}, I_H \text{ in ma} . \tag{8.19}$$

$$I_{SK} = |I_H - I_{GT}| e^{-.75V/\theta_K} \quad \therefore \; I_{GT} \leq .95 \, I_H$$

The parameter, R, is the on-state anode resistance which, although non-linear, is treated as linear due to the problems of excessive computational time involved in use of non-linear resistors in computer analysis. For SCEPTRE this means inverting the system formulation matrix at every time step solution [19]. Fortunately, the use of small constant valued saturation currents in (8.19) provides a device for simulating low current on-state resistance non-linearities.

A lumped value R is suitable to provide simulation of high current on-state V_{AK} in the region $.1 \, I_{TM} < I_A < I_{TM}$.

To determine R,

$$R = \frac{V_T(I_{TM}) - V_T(.1 \, I_{TM})}{I_{TM} - .1 \, I_{TM}} \tag{8.20}$$

The values needed by (8.20) are obtained from manufacturer's literature as illustrated in Fig. 8.4.

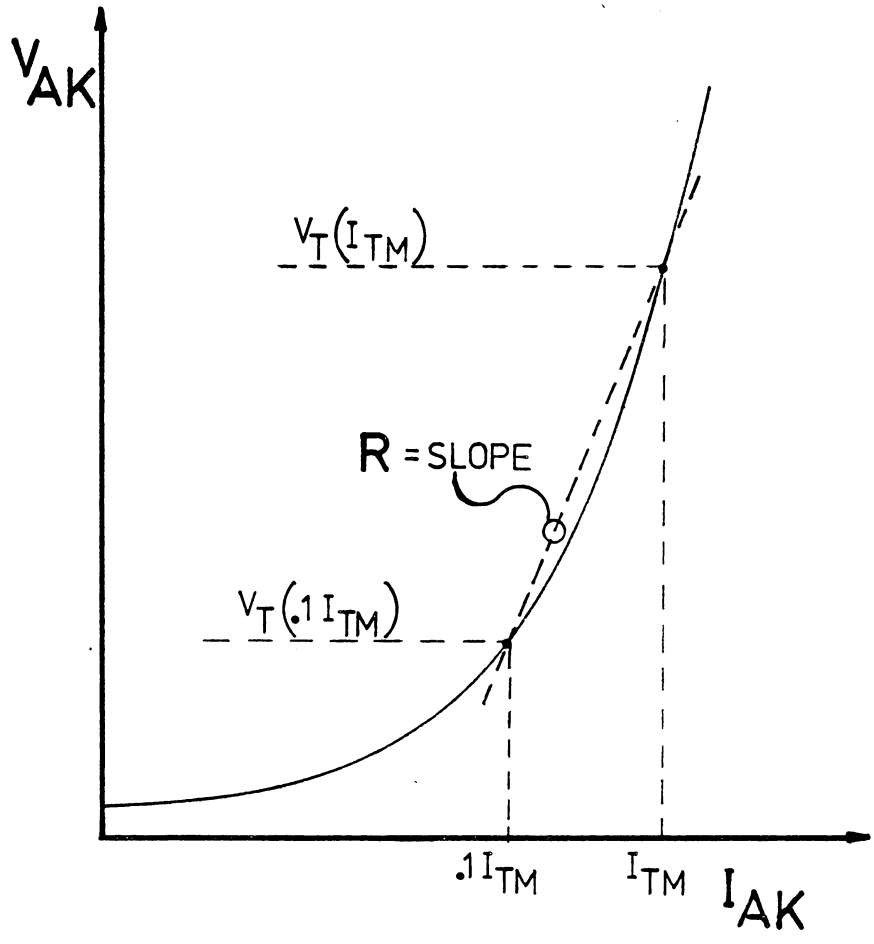


Fig. 8.4. Illustration of Data Sheet On-state Voltage vs. Current Characteristic.

8.6 Dynamic Analysis

The dynamic performance criteria of particular interest are depicted graphically in Fig. 8.5.

8.6.1 Turn-on Analysis

The SCR is subject to four modes of turn-on, normal gate pulse, static dv/dt, reapplied dv/dt and high voltage breakdown. The latter is usually defined as a failure mode although some PNPN devices are operated normally by avalanche turn-on.

8.6.1.1 Gate Driven Turn-on

The first area of device dynamics to investigate is gate turn-on. Gate turn-on is characterized as DC trigger current or pulse trigger. The specification I_{GT} is a DC trigger current specification which specifies the minimum DC gate current required to turn the SCR on without specification of the time required to accomplish turn-on.

Model Behavior for $I_G \leq I_{GT}$

To examine the validity of the model, it is necessary to establish analytically that turn-on will not occur at some current below I_{GT} and that turn-on will occur at I_{GT}.

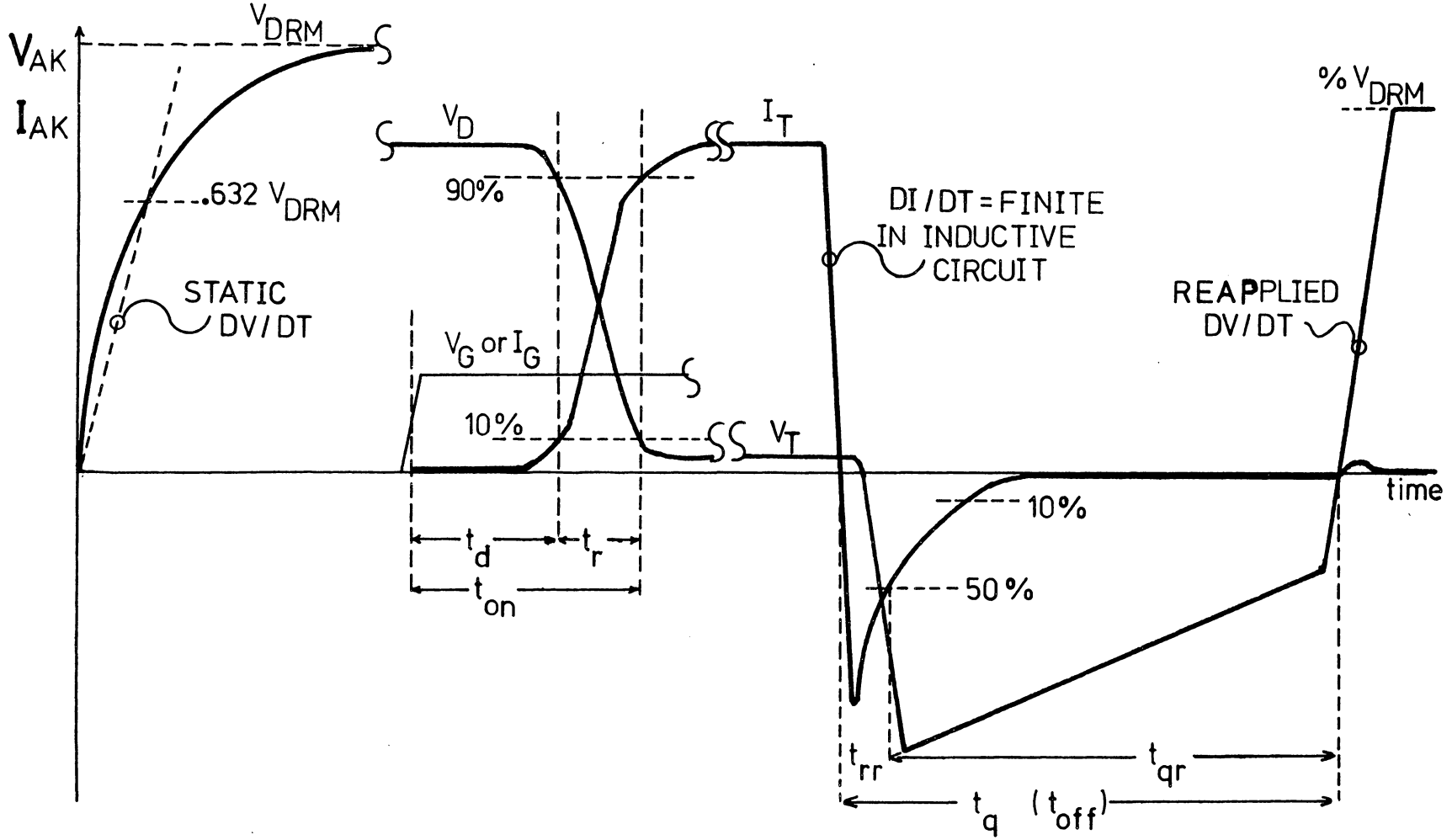


Fig. 8.5. Dynamic Operational Characteristics of the SCR to be Simulated by the J^3 SCR Model, (T = on-state, D = off-state, M = Maximum).

The circuit for a static off-state device with $I_G < I_{GT}$ is given in Fig. 8.6. An applied gate current $I_G < I_{GT}$ with $\alpha_K = 1$ produces a voltage drop $.75\ I_G/I_{GT}$ across RK. The response is JK_0;

$$JK_0 = (I_H - I_{GT})e^{\left(\frac{I_G}{I_{GT}} - 1\right)\frac{.75}{0}} \tag{8.21}$$

$J1 = \alpha_K/(1-\alpha_K)*JK$ and for $\alpha_K = 1$ $J1 = I_H/(I_H-I_{GT})*JK$

$RK = .75/I_{GT}$

$I_X = (\alpha_A+\alpha_K-1)/(1-\alpha_A)$ and for $\alpha_K = 1$ $I_X = I_{GT}/(I_H-I_{GT})$

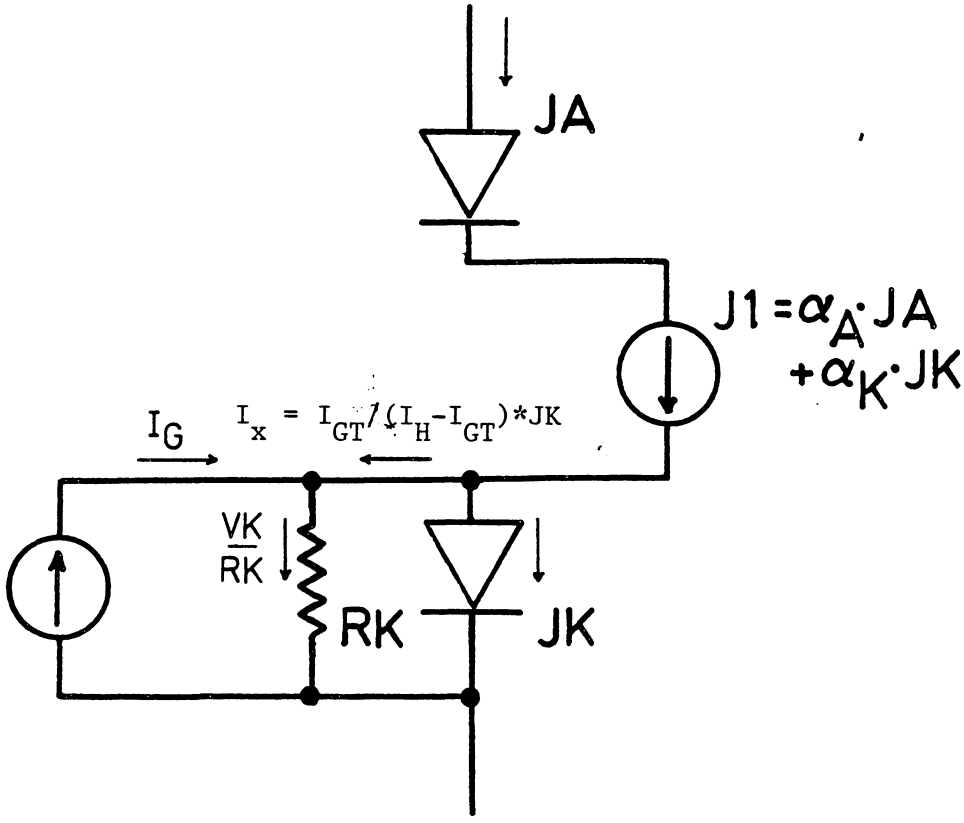


Fig. 8.6. Static device with $I_G < I_{GT}$.

This current JK_0 will flow through J1 triggering a regenerative action causing the current in JK to increase and vice versa. Obviously without the presence of RK, the system would become unstable and JK would increase indefinitely until caused to stabilize due to the other nonlinearities of the total system.

In this case, however, the presence of RK shunts a portion of the current, $[I_{GT}/(I_H-I_{GT})]JK$, of J1 through RK. Thus the regenerative cycle may stabilize to some value of $JK > JK_0$ but with the device still in the stable off-state of Fig. (8.6).

This may be shown as follows. The voltage drop across RK is due to the sum of the current, I_G, plus the current from J1.

$$V_{RK} = [I_G + \frac{I_{GT}}{(I_H-I_{GT})} JK] \frac{.75}{I_{GT}} = [\frac{I_G}{I_{GT}} + \frac{JK}{(I_H-I_{GT})}] .75 \qquad (8.22)$$

If the device is in the off-state then $V_{RK} < .75V$ therefore using (8.21) and (8.22)

$$JK_0 < JK = JK_0 \, e^{[JK/(I_H-I_{GT})](.75/\theta)} < (1-\frac{I_G}{I_{GT}})(I_H-I_{GT}) \qquad (8.23)$$

The equation (8.23) is transcendental and defines the zone in which any stable node of JK must lie if one exists. Examining equations (8.21) and (8.23), the ability of a stable node to exist is seen to depend on the ratio I_G/I_{GT}.

The proof of the stability of JK in the zone defined by (8.23) assumes that given I_G/I_{GT} sufficiently small, then the trajectory of JK from the initial $JK_0(I_G/I_{GT})$ is unique. Therefore, if a stable node lies in the zone defined by (8.23), then it will lie on the trajectory of JK. JK will then progress to that stable node and remain there unless otherwise disturbed.

The transcendental equation (8.23) has been empirically examined to show that JK will stabilize for $I_G/I_{GT} \leq .87$. In terms of SCR parameters, this reveals the value of I_{GD}, the maximum gate current for which the device will remain off. This parameter is not normally given in manufacturers data sheets.

In summary, it is seen that equation (8.23) predicts $I_{GD} \approx .87\ I_{GT}$ as the highest gate current for which the model will remain off. It is deduced from this that I_{GT} being in the unstable region of equation (8.23), then the model is predicted to turn on at $I_G = I_{GT}$.

Model Behavior for $I_G > I_{GT}$

Proceeding next to analyze model behavior for $I_G > I_{GT}$, it is first necessary to examine the models dynamic elements qualitatively in order to simplify the applicable equivalent circuit to be analyzed during discrete regions of the turn-on transient behavior

> This mode of turn-on must be analyzed somewhat interactively with dv/dt since these two effects are concerned with common elements in the model. CC_{DEPL} and CK are two particular common elements.

Fig. 8.7 gives the anode current characteristic associated with a gate pulse turn-on. Analysis will begin by looking at the flat low current region of $0 < t < .8t_d$.

For this interval, it is seen immediately that all the elements of the so-called gate loop described by equation (8.8) and relating to figure 8.1 must be considered. This calls for the entry of elements VG, RG, CK, RK, and JK into figure 8.8.

Now, a disturbance of the node voltage at CK must have offsetting shifts in other system node voltages. Observing from figure 8.1 that CC and CA are in series with external load loop elements, then node voltage shifts must involve these two elements. Since $I_A \approx 0$ in this $0 < t < .8t_d$ interval, then essentially all of the disturbance must be contained in these two elements.

Considering SCR physical construction (i.e., doping properties, etc.), the fact that the device is off, and that CC is reverse biased to a value $V_{CC} \approx -V_{AK}$, then it is seen that these two capacitances consist only of depletion layer terms at this time, and that $CC_{DEPL} << CA_{DEPL}$. The expectation is therefore that a voltage disturbance at V_{CK} has a corresponding offset voltage disturbance in V_{CC}, with essentially no disturbance to V_{CA} during $0 < t < .8t_d$.

CC_{DEPL} therefore appears in figure 8.8. To emphasize that very little anode circuit activity occurs during most of this time, CC_{DEPL} is shown as a dotted line element in series with J1 and JK. This illustrates that virtually all of the charge injected from the cathode into the gate-collector region is lost by recombination.

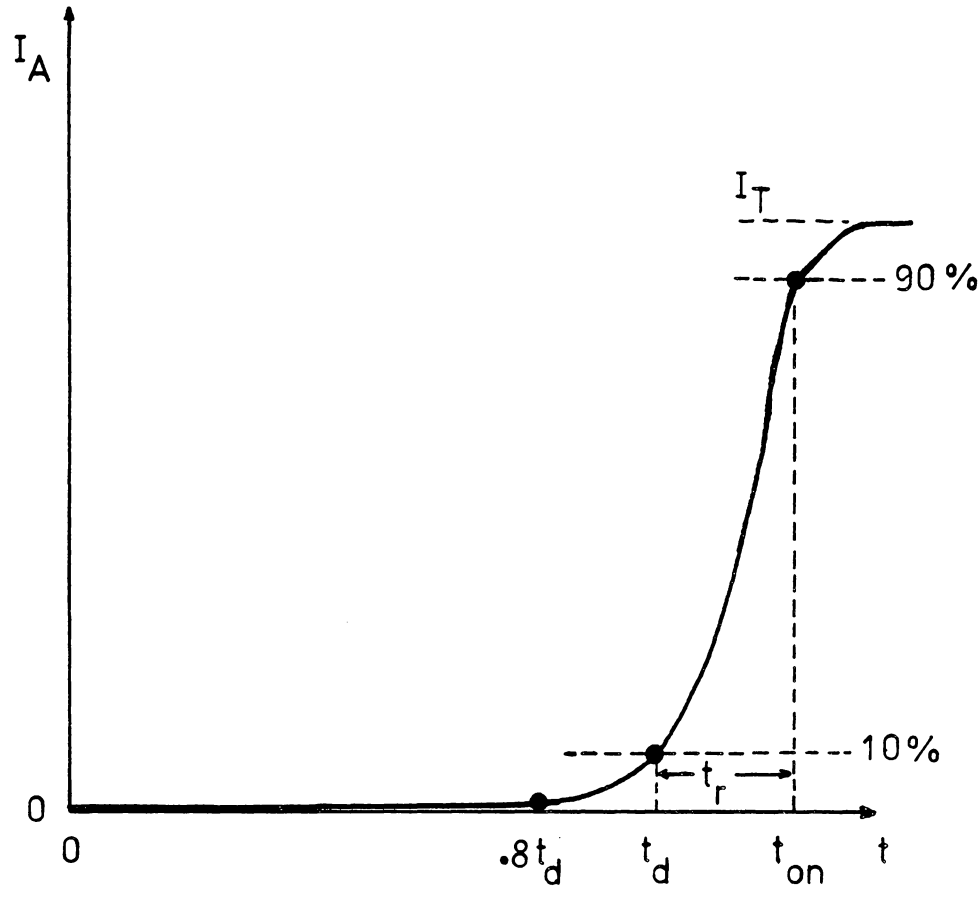


Fig. 8.7. Anode Current from Start of Gate Trigger.

It is noted that in general the qualitative nature of the influence of CC_{DEPL} on gate pulse turn-on is that as V_{AK} (and hence $-V_{CC}$) increases the pulse gate drive requirements decrease [22].

As has been noted, $CA_{DEPL} >> CC_{DEPL}$ at $V_{CC} \approx -V_{AK}$, however, more must be said about CA_{DEPL} to insure proper model operation and for that matter to simplify parameter estimation.

The first point to note about CA_{DEPL} (with respect to the J^3 model) is that it must be sufficiently large to insure that the small currents of the anode region do not much disturb V_{CA} from a very near zero value. This will then insure that the initial turn-on transient is a gate controlled feature.

Another factor to note is that latching current at the spec sheet gate pulse turn-on data is approximately $3xI_H$ [22]. Although this model does not quantify I_L simulation, a suggested area to look for I_L simulation is the CA_{DEPL} capacitance term. A sufficiently large CA_{DEPL} will delay $\alpha_A JA$ becoming sufficiently large to provide $V_{CK} = I_{GT}RK$ required for sustained regeneration leading to turn-on.

Tentatively a value for CA_{DEPL} obeying (8.25) will be required.

$$CA_{DEPL_0} \geq CK \tag{8.25}$$

CA_{DEPL} will be made nonlinear to avoid excessive oscillatory behavior during reverse transients [31]. This was observed to

happen when simulating reverse transients with the "Modified Hu-Ki Model" using constant value $CA_{DEPL} < 10^4$ pF. Alternatively to achieve good numerical performance, the minimum reverse biased value of CA_{DEPL} is desired to not fall below $\approx$ 100 pF. To insure this an additional criteria

$$CA_{DEPL_0} \geq 10^{-10} \left[V_{(BR)R} \right]^{1/2} pF \tag{8.26}$$

is tentatively established. CA_{DEPL} will be examined more closely in rise time analysis.

Quantification of CK

Specification sheets usually provide pulsed gate turn-on data as follows.

$$t_d \ @ \ V_{AK} \ @ \ V_G \ \& \ R_G \ (\text{or } R_S) \tag{8.27}$$

The dynamics of gate pulse triggering are that the gate-cathode junction must become forward biased sufficiently such that anode current reaches 10% of I_T at t_d. This is shown graphically in Fig. 8.5 and Fig. 8.7. I_T is usually much larger than I_G so that

while I_G dominates initial turn-on, it is a dynamically varying influence to the point of little significance as $I_A \rightarrow I_T$.

During the greater portion of the interval t_d the anode current I_A is very small (i.e. $I_A < I_L \simeq 3 \times I_H$) [22]. Also, due to the delay in reaching significant forward bias to JA caused by the charging delay in CA_{DEPL}, JK is initially the dominant control junction in the regenerative action currents of J1. To determine model parameters for predicting t_d, the device equivalent circuit during $0 < t \lesssim .8\ t_d$ is that shown in Fig. 8.8 [8,22].

The time $.8\ t_d$ is arbitrarily chosen as the dividing point before which removal of the gate pulse will result in failure of the SCR to turn-on and after which the device will continue to turn-on even though gate pulse is removed. In other words $I_A = I_L$, the latching current.

To determine the required value of $C = CC_{CEPL} + CK$ for the value of JK to reach $3 \times I_H$ at $.8\ t_d$

$$V_{CK}\ (.8\ t_d) = \theta\ \ln \left\{ \frac{3 \cdot I_H}{I_{SK}} \right\} \tag{8.28}$$

$$= .75V + \theta\ \ln\ (3)$$

$$= .7786\ .$$

It is evident that the model must provide a shunt path for I_G to avoid a very rapid rise of JK once $V_{CK} > .75V$. This path as seen from Fig. 8.1 is through CC then through J1 and Jk to close the gate current loop.

RG, VG = spec sheet values

normally $CC_{CEPL} << CK$

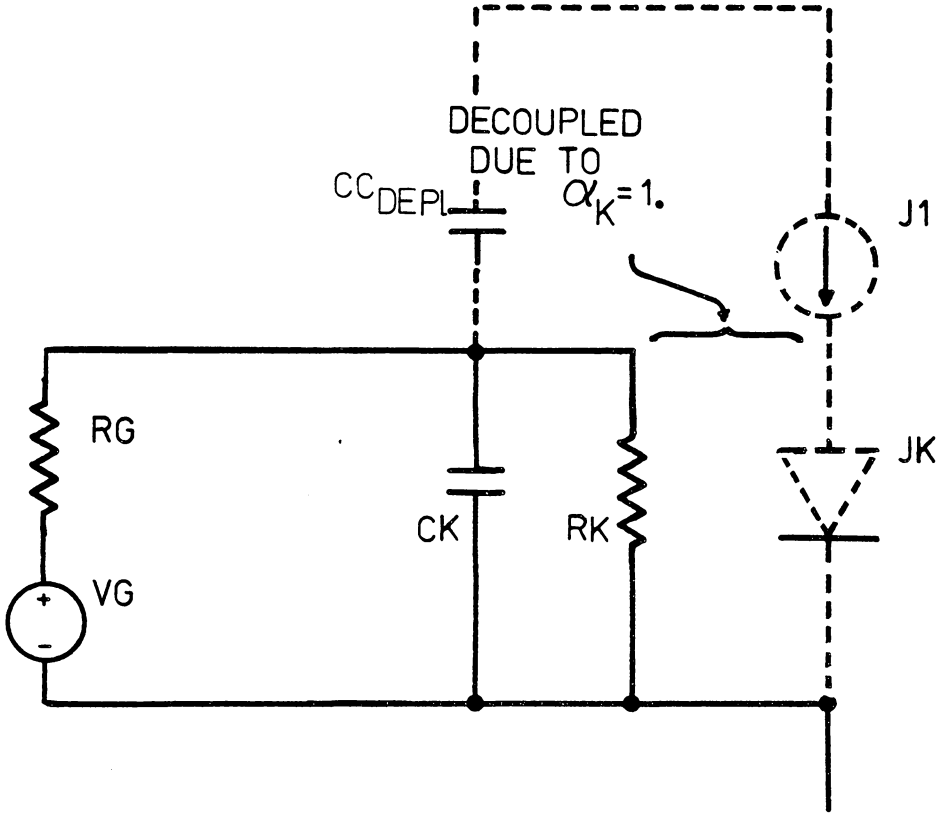


Fig. 8.8. SCR Equivalent Gate Circuit for $0 < t < .8\ t_d$.

The device dynamic equations (8.3) through (8.9) reduce to the following for the interval $0 < t < .8\ t_d$.

Input Loop Equation

$$VG - RG\left(C\frac{dV_{CK}}{dt} + \frac{V_{CK}}{RK}\right) - V_{CK} = 0$$

Solving gives:

$$v_{CK}(t) = \frac{v_G\ RK}{RG+RK}\left(1 - e^{-t/[(RG//RK)(CK+CC_{CEPL})]}\right) \tag{8.29}$$

By (8.29) and $CK \simeq CK+CC_{CEPL}$

$$CK = \frac{-.8\ t_d}{\frac{RG\ RK}{RG+RK}\ln\left(1 - \frac{.78}{VG}\frac{(RG+RK)}{RK}\right)} \tag{8.30}$$

Using the fact that due to physical structure of the SCR in conjunction with the reverse biased condition of CC_{DEPL}, the value of $CC_{CEPL} << CK$, CK is extracted from (8.30) by omitting CC_{CEPL}.

A similar analysis to include the amplifying gate structure yields

$$CK = \left| \frac{(1/RK + 1/RAG + 1/RG)t_d}{\ln\ (1 - .75/V_{CK}^{\infty})} \right|$$

where

$$V_{CK}^{\infty} = \frac{VG - .75\left(1 + \frac{RG}{RAG}\right)}{\left(1 + \frac{RG}{RAG} + \frac{RG}{RK}\right)} \tag{8.30a}$$

8.6.1.2 Static dv/dt Turn-on

Before proceeding further in gate driven turn-on analysis, it is necessary to analysis static dv/dt parameters due to the critical nature of CC_{DEPL} to this behavior. dv/dt turn-on is primarily due to displacement currents $\frac{d}{dt}(CC \cdot V)$, during rising V_{AK}, providing charge injection into the gate region. The J^3 SCR model has, by (8.25), a nonlinear CA_{DEPL} which has a forward biased value $CA_{DEPL_0} > CK$. Since the dv/dt transient must start from a static off-state, neither CA_{DEPL_0} nor CK has any significant initial charge. Both junctions are essentially zero-biased.

During the initial dv/dt transient, displacement current $\frac{d}{dt}(CC \cdot V)$ flows through CA_{DEPL} and CK. Neither JK nor JA is sufficiently forward biased to provide sufficient injection currents to affect turn-on. The nonlinear nature of CA_{CEPL}

$$CA_{DEPL} = \left.\frac{CA_{DEPL_0}}{\left[1 - V_{CA}\right]^{1/2}}\right|_{V_{CA} << 1} > CK \qquad (8.31)$$

causes the forward biasing of JA to lag behind the forward biasing of JK. Thus the analysis of the initial transient may be limited to analysis of the charge displacement from CC required to charge CK and thus forward bias JK*.

*The assumption will be experimentally verified.

Static dv/dt, that is a dv/dt rating for devices initially in a static off-state, is characterized by manufacturers by two methods, exponential dv/dt and linear dv/dt, as illustrated in fig. 8.10. The static $\frac{dv}{dt}$ parameter will be denoted as $\frac{dv_s}{dt}$. Since the SCR is in the static off-state at the time of application of $\frac{dv_s}{dt}$, only the depletion layer term, CC_{DEPL}, of CC is present. We have then for $V_{CC}(t) \leq 0$ and $V_{CC}(0) \approx 0$.

$$I_{CC_{DEPL}} = \frac{d}{dt}\left\{CC_{DEPL}\ V_{CC}\right\} = \frac{CC_{DEPL_0}\left\{1 - \frac{1}{2}\frac{dV_s}{dt}\ t\right\}}{\left\{1 - \frac{dV_s}{dt}\ t\right\}^{3/2}}\ \frac{dV_s}{dt} \qquad (8.32)$$

where: $\frac{dV_s}{dt}$ is linear static $\frac{dv}{dt}$.

Most spec sheets define $\frac{dV_s}{dt}$ based on the exponential dv/dt curve illustrated in Fig. (8.10) and provide either τ or $\frac{dV_s}{dt}$ values in spec sheets. For analysis it is seen that

$$\frac{d\ V_{CC}(t)}{dt} \approx \frac{d\ V_{AK}(t)}{dt} = \frac{V_{DRM}}{\tau}\ e^{-t/\tau}\Bigg|_{\tau} = \frac{.632\ V_{DRM}}{\frac{dV_s}{dt}} \qquad (8.33)$$

$$\frac{d\ V_{CC}(t)}{dt} = 1.58\ \frac{dV_s}{dt}\ e^{-t/\tau}$$

This gives for CC

$$I_{CC_{DEPL}} = \frac{d\ Q_{CC_{DEPL}}}{dt} = \frac{d}{dt}\left\{\frac{CC_{DEPL_0}}{\left[1 - V_{CC}\right]^{1/2}} \cdot V_{CC}(t)\right\}$$

$$= \frac{CC_{DEPL_0}}{2\left[1 - V_{CC}\right]^{3/2}}\ \frac{d\ V_{CC}}{dt}\ V_{CC}(t) + \frac{CC_{DEPL_0}}{\left[1 - V_{CC}\right]^{1/2}}\ \frac{d\ V_{CC}}{dt}$$

$$= \frac{CC_{DEPL_0}}{\left[1 - V_{CC}\right]^{1/2}} \times \left\{\frac{1 - \frac{V_{CC}}{2}}{1 - V_{CC}}\right\} \times 1.58\ \frac{dV_s}{dt}\ e^{-t/\tau} \qquad (8.34)$$

which for V_{CC} large

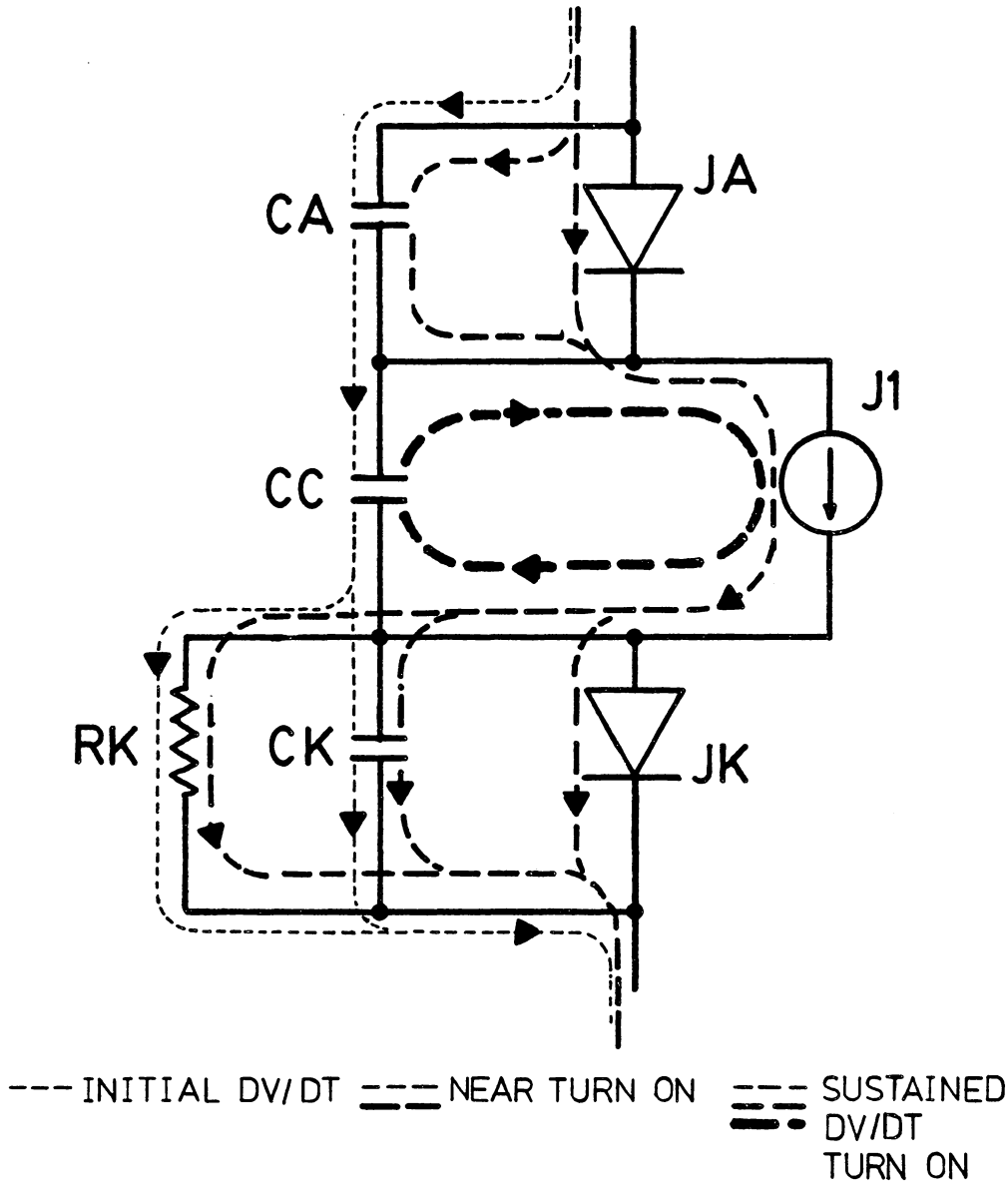


Fig. 8.9. Static dv/dt Transient Equivalent Circuit Showing Turn-on Currents Sequence for J^3 SCR Model.

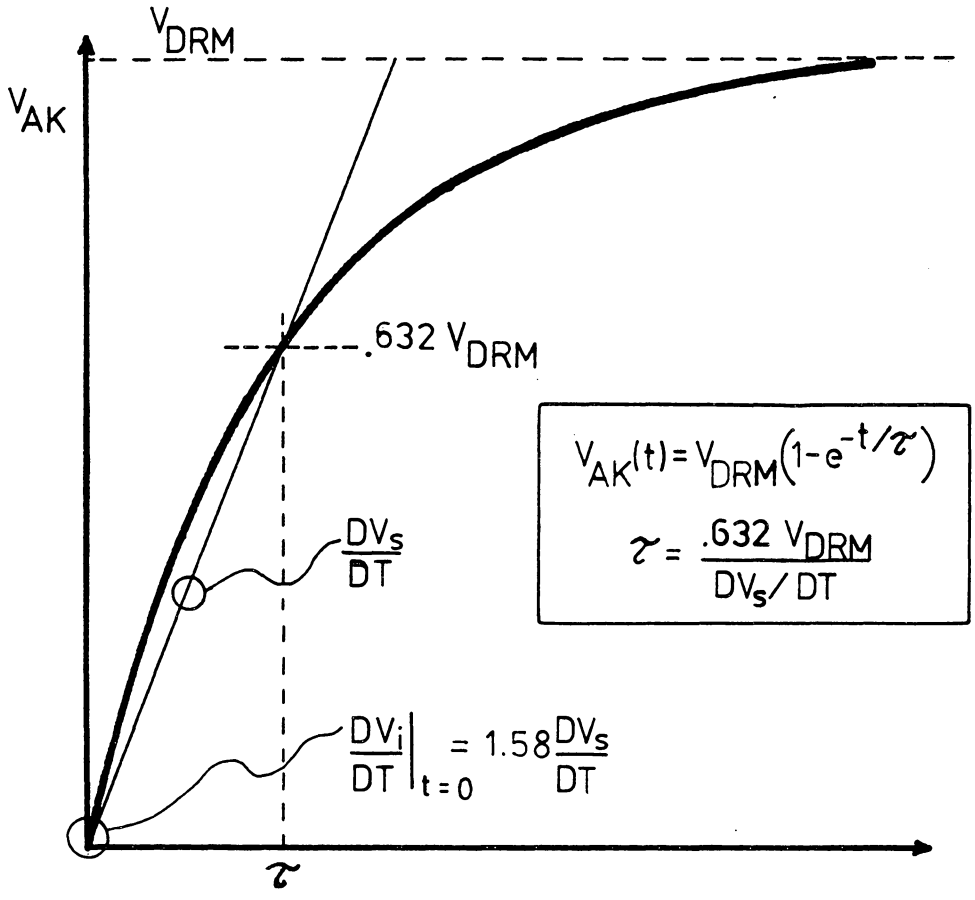


Fig. 8.10. Exponential dv/dt Definition.

$$I_{CC_{DEPL}} \approx \frac{CC_{DEPL_0}}{(V_{CC})^{1/2}} \left[\frac{1}{2}\right] \left[1.58 \frac{dV_s}{dt}\right] e^{-t/\tau}$$

The current through CK is

$$I_{CK} = \frac{d\ Q_{CK}}{dt} = I_{CC_{CEPL}} - \frac{Q_{CK}}{CK\ RK}$$

which gives

$$\frac{d}{dt} Q_{CK} + \frac{Q_{CK}}{CK\ RK} = I_{CC_{DEPL}} \tag{8.35}$$

or $$CK \frac{d\ V_{CK}}{dt} + \frac{V_{CK}}{RK} = I_{CC_{DEPL}}.$$

During the interval $0 < t < 5\tau$, V_{CK} must remain less than .75 volts if the SCR is to remain off

$$V_{CK} = \frac{1}{CK} \int_0^{5\tau} \left(I_{CC_{DEPL}} - \frac{V_{CK}}{RK} \right) dt < .75V$$

The problem is treated from the charge transfer approach. If the SCR is to remain off during the $\frac{dV_s}{dt}$ transient, then the total displacement charge removed from CC_{DEPL} is a combination of transfer to CK and passage through RK.

$$\left| \int_0^{5\tau} \left\{ \left(\frac{d}{dt} Q_{CK} \right) dt + \frac{V_{CK}}{RK} dt \right\} \right| = \left| \int_{Q_{CC}(0)}^{Q_{CC}(5\tau)} d\ Q_{CC_{DEPL}} \right|$$

First treating the charge displaced from CC_{DEPL} ,

$$\int_{Q_{CC}(0)}^{Q_{CC}(5\tau)} d\,Q_{CC_{DEPL}} = \int_{Q(0)}^{Q(5\tau)} d\left\{\frac{CC_{DEPL_0}}{\left[1 - \frac{V_{CC}(t)}{\psi_0}\right]^{1/2}} \times V_{CC}(t)\right\}$$

$$= \int_{Q(0)}^{Q(5\tau)} d\left\{\frac{CC_{DEPL_0} \times V_{DRM}\left(1 - e^{-t/\tau}\right)}{\left[1 - \frac{V_{DRM}}{\psi_0}\left(1 - e^{-t/\tau}\right)\right]^{1/2}}\right\}$$

$$= \frac{CC_{DEPL_0} \times V_{DRM}}{\left[1 - \frac{V_{DRM}}{\psi_0}\right]^{1/2}} \simeq \left|CC_{DEPL_0}\left[V_{DRM}^{1/2}\right]\right| [\psi_0]^{1/2}$$

and for ψ_0 defaulted to unity

$$\Delta Q_{CC_{DEPL}} = \left|CC_{DEPL_0} \times \left[V_{DRM}\right]^{1/2}\right| \text{ coulombs} \qquad (8.36)$$

Quantification of CC_{DEPL}

A lower boundary can be placed on CC_{DEPL_0} by assuming that the entire $Q_{CC_{DEPL}}$ is transferred to CK and that the charge transferred through RK is negligible. In order for the device to remain off, the result of this charge transfer is

$$\frac{Q_{CK}}{CK} < .75V \qquad (8.37)$$

Using equality

$$|.75\ CK| = |Q_{CK}| = \left| CC_{DEPL_0} \times \left[V_{DRM}\right]^{1/2} \right|$$
$$\min$$

which leads to the result

$$CC_{DEPL_0} = \left| \frac{.75\ CK}{V_{DRM}^{1/2}} \right| \text{ Farads} \qquad (8.38)$$
$$\min$$

Example. For the GE C602LM SCR

$$CC_{DEPL_0} = \left| \frac{.75\ (3.22\ \mu F)}{[2700\ V]^{1/2}} \right| = 4.65 \times 10^{-8}\ F$$
$$\min$$

which is an order of magnitude larger than the Hu-Ki model prediction [1].

An upper boundary may be placed on CC_{DEPL_0} by observing that the bulk of the charge transfer occurs early in the dv/dt transient when the non-linear CC_{DEPL} is at its larger values and the rate of rise of the exponential dv/dt is at its greater value.

V_{CK} then reaches its upper value near .75V very early in the transient. This allows an approximation of the losses due to current through RK during the dv/dt transient. The time constant RK CK is typically long with respect to τ.

$$RK\ CK >> \tau$$

so that V_{CK} having been charged to near .75V will discharge only moderately during the period 5τ. An estimate for the charge shunted through RK is therefore

$$Q_{RK} \simeq \frac{.75V}{RK} \times 5\tau = \frac{3.16\ V_{DRM} I_{GT}}{dV_s/dt} \tag{8.39}$$

This illustrates the effect of the shunted gate to cathode structure in desensitizing devices to dv/dt turn-on.

The charge shunted by RK may be added to that stored in CK to form the total allowable displacement charge from CC_{DEPL}.

$$\left|\Delta Q_{CC}\right| = \left|.75\ CK\right| + \left|\frac{3.16\ V_{DRM} I_{GT}}{dV_s/dt}\right| = \left|CC_{DEPL_0} \times \left[V_{DRM}\right]^{1/2}\right| \tag{8.40}$$

Solving (8.40) for $CC_{DEPL_{0\ max}}$ gives

$$CC_{DEPL_{0\ max}} = \frac{\left|.75\ CK\right|}{\left[V_{DRM}\right]^{1/2}} + \left|\frac{3.16\left[V_{DRM}\right]^{1/2} I_{GT}}{dV_s/dt}\right| \tag{8.41}$$

Example. For the GE C602 LM SCR the $CC_{DEPL_{0\ max}}$ is

$$CC_{DEPL_{0\ max}} = 4.65 \times 10^{-8} + 2.63 \times 10^{-8} = 7.28 \times 10^{-8} F$$

For this case the boundary values of CC_{DEPL_0} differ by approximately 50% due to the presence of RK.

The estimation for $CC_{DEPL_{0\ max}}$ represents the more physically appropriate value under the assumption of negligible influence of the anode junction during a dv/dt transient. This is only a partially correct assumption. It must be taken into account that static dv/dt turn-on is unlike the gate controlled turn-on where CK charging currents are provided by the gate circuit so that the anode circuit remains static during initial CK charging. This has the effect of delaying anode region activity by the time required to charge CA.

On the other hand static dv/dt charging current for CK must flow through the anode circuit thus providing some simultaneous charging of CA. The effect of this is that due to the non-linearity of the CA, the anode junction JA does not reach activation as early as does JK, however, a substantial amount of the lag time is removed, as compared to gate driven turn-on.

Experiment suggests that a value of approximately .4 → .5 of that predicted by equation (8.41) is the proper choice for CC_{DEPL_0}.

$$CC_{DEPL_0} = .45 \left| \frac{.75\ CK}{\left[V_{DRM}\right]^{1/2}} + \frac{3.16\ \left[V_{DRM}\right]^{1/2} I_{GT}}{dV_s/dt} \right| \text{ Farads} \qquad (8.42)$$

where $I_{GT} \leq .95\ I_H$

Example. For the GE C602

$$CC_{DEPL_0} \approx 3.27 \times 10^{-8} F\ .$$

Parameter Adjustments

When simulating highly non-linear dynamic effects such as dv/dt, the model user should always do initial model verification tests on these parameters. The analytical parameter estimation procedure is primarily a tool to locate the approximate values for simulation. Due to the extremely wide variation in device structures and to some degree manufacturer's spec. procedures, these parameter estimates usually require adjustment. Adjustments of 20-25% are reasonable variations from prediction.

Parameter adjustments should be made conservatively. That is parameters adjustments should be made in a manner to reveal device performance which may adversely affect circuit behavior. In the case of the dv/dt behavior, it is generally better that the model predict a premature dv/dt turn-on than to have an insensitivity to dv/dt. Snubber compensation for dv/dt will then ensure adequate protection.

Approximation of CC_{DEPL} as a Constant

It is interesting to investigate the feasibility of using a linear approximation to CC_{DEPL} to enable modeling of dv/dt phenomena. This linear approximation is a useful check on the non-linear estimate for CC_{DEPL}. Again, one starts with displacement current during the initial transient.

$$\left|I_{DIS}\right| = \left|CC \frac{dV_{CC}}{dt}\right| = \left|CK \frac{dV_{CK}}{dt} + \frac{V_{CK}}{RK}\right| \tag{8.43}$$

or

$$\left|\frac{dV_{CK}}{dt} + \frac{V_{CK}}{RK\ CK}\right| = \left|\frac{CC}{CK}\ 1.58 \left(\frac{-dV_s}{dt}\right) e^{-t/\tau}\right| \tag{8.44}$$

which has solution

$$V_{CK}(t) = V_{CK_0} e^{-t/RKCK} + [\tau RK/(RKCK+\tau)]CC\ 1.58\left(\frac{-dV_s}{dt}\right)e^{-t/\tau} \qquad (8.45)$$

Applying the initial condition $V_{CK}(0) = 0$, then

$$V_{CK}(t) = (1.58\tau RKCC)/(RKCK+\tau)\left(\frac{-dV_s}{dt}\right)\left[e^{-t/\tau} - e^{-t/RKCK}\right] \qquad (8.46)$$

The trajectory of $V_{CK}(t)$ for the initial transient is that given in Fig. 8.11. The marginal case is that for which V_{CK} just reaches .75V. Below that, the SCR will not turn-on. Above .75V on V_{CK}, the SCR will turn-on, and (8.46) is no longer valid as suggested by the dotted line extension for this case in Fig. 8.11.

Now to analyze the marginal case (i.e. that for which an infinitesimal increase in V_{CK} above V_{CK-max} will case turn-on), it is seen that the point of zero slope describes the point of V_{CK-max} which for the marginal case is approximately .75V. This provides another boundary condition thus allowing solution for CC.

Applying boundary condition $dV_{CK}(t_{peak})/dt = 0$ to (8.46) gives

$$0 = 1.58\tau RKCC/(RKCK+\tau)\left(\frac{-dV_s}{dt}\right)\left[-\frac{e^{-t/\tau}}{\tau} + \frac{e^{-t/RKCK}}{RKCK}\right]\Bigg|_{t=t_{peak}} \qquad (8.47)$$

which is readily solved for t_{peak} by

$$t_{peak} = [RKCK\ \tau\ \ln(\tau/RKCK)]/(\tau-RKCK) \qquad (8.48)$$

which requires $RKCK > \tau$.

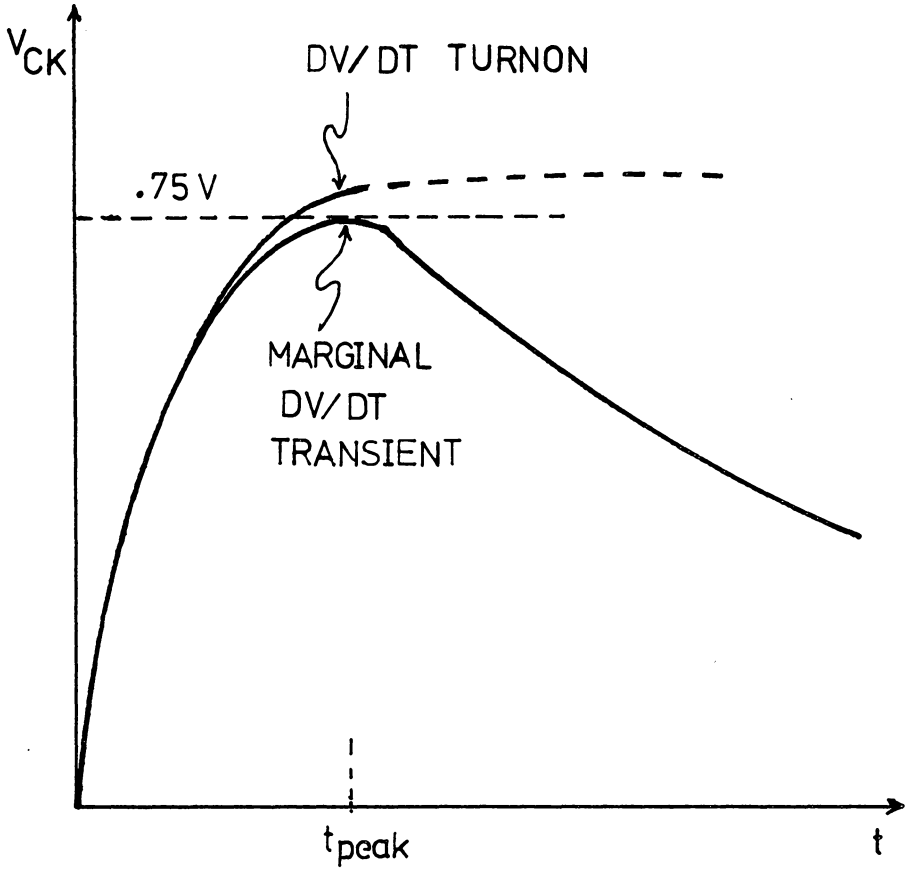


Fig. 8.11. J^3 Model V_{CK} Transient Due to $\frac{dv}{dt}$.

Then for $V_{CK}(t_{peak})$ to just reach .75V, (8.48) is used for t in (8.46) to give

$$.75V = [(1.58\tau RKCC)/(RKCK+\tau)]\left(\frac{-dV_s}{dt}\right)\left[e^{-t_{peak}/\tau} - e^{-t_{peak}/RKCK}\right] \quad (8.49)$$

Solving for $CC_{DEPL} = CC$

$$CC_{DEPL} = [.75V(RKCK+\tau)]/\left[1.58\tau RK\left\{\frac{-dV_s}{dt}\right\}\left(e^{-RKCK\lambda} - e^{-\tau\lambda}\right)\right] \quad (8.50)$$

where

$$\lambda = \ln(\tau/RKCK)/(\tau-RKCK) \quad (8.51)$$

Example. For the GE 602LM SCR, this predicts

$$RKCK = 30.18\ \mu s$$

$$\tau = 3.28\ \mu s$$

$$\lambda = .0825\ \mu s^{-1}$$

and $$CC_{DEPL} = .0142\ \mu F\ .$$

Comparing this value to that predicted for the non-linear case in (8.42) it is seen that for $|V_{CC}| \lesssim |20V|$ that the non-linear capacitance is larger, but for $|V_{CC}| \gtrsim |50V|$ the constant approximation is larger. Since better numerical performance might be expected using CC_{DEPL} constant and the non-linear capacitance, while bounded, is not so exactly defined, then it might seem that the linear approach is preferred. Unfortunately, this restricts modeling of the rise time transient and dynamic on-state voltage characteristics as discussed

later. The linear approximation is therefore useful only to check the non-linear calculations.

8.6.1.3 A Digression on Simulation of the Latching Current Phenomena, I_L

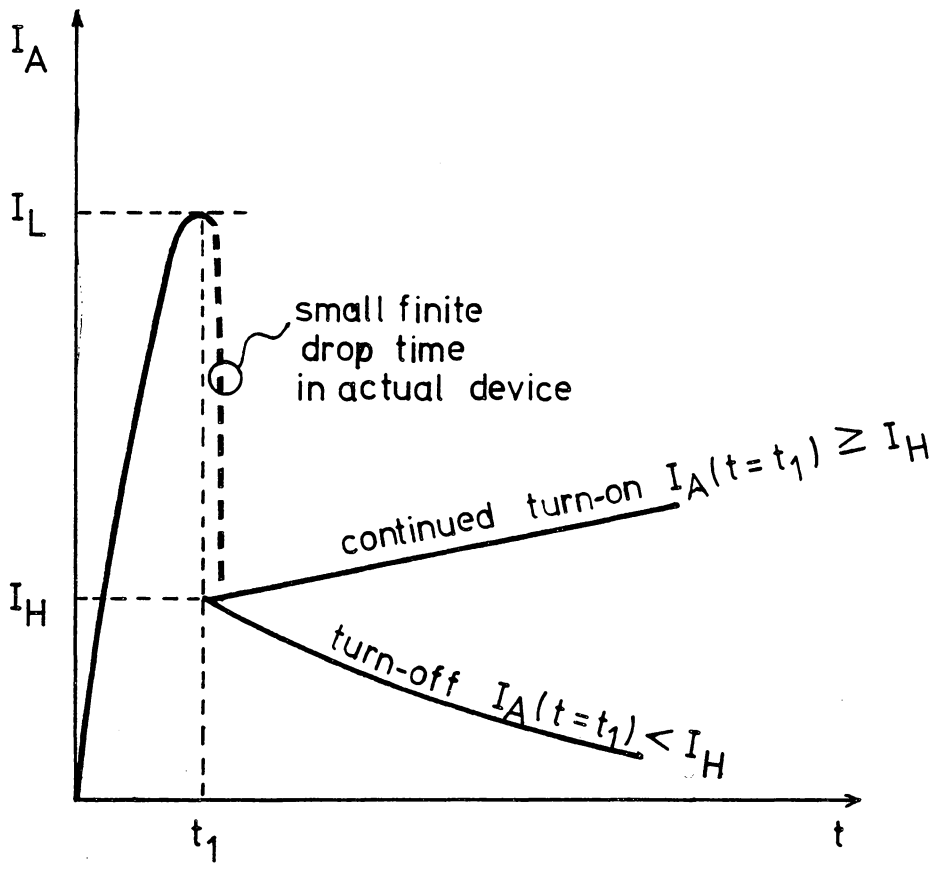
Spec sheets give sparse data on the latching current characterization. It is therefore not included quantitatively in the J^3 model.

It is interesting, however, to examine a possible source of control if a quantitative simulation were to be developed. Examination of the J^3 model suggests the anode junction capacitance, CA, as a possible control variable in the model.

The latching current characteristic as it appears in the anode current, I_A, is illustrated in Fig. 8.12. As illustrated, a rapid drop in anode current follows removal of the gate pulse at t_1.

Examining the system dynamic equation (8.3) through (8.9) and the J^3 model of Fig. 8.1, it is seen that the dynamic equivalent circuit at time t_1 is that given in Fig. 8.13. Note that for gate pulse value equal to that defined in the spec sheets for t_d characterization, then as previously discussed, the value of t_1 corresponds to .8 t_d in the J^3 model.

The time t_1 corresponds to the time when V_{CK} has become essentially static at slightly greater than .75V. The bulk of the gate current then flows through CC with a small component, $\approx I_{GT}$, flowing through RK. This is the critical point at which $V_{AK} \approx -V_{CC}$ is just starting to drop, but still has only small negative slope (ref. Fig. 8.5).



t_1 = time gate pulse removed

Fig. 8.12. Latching Current Characteristic.

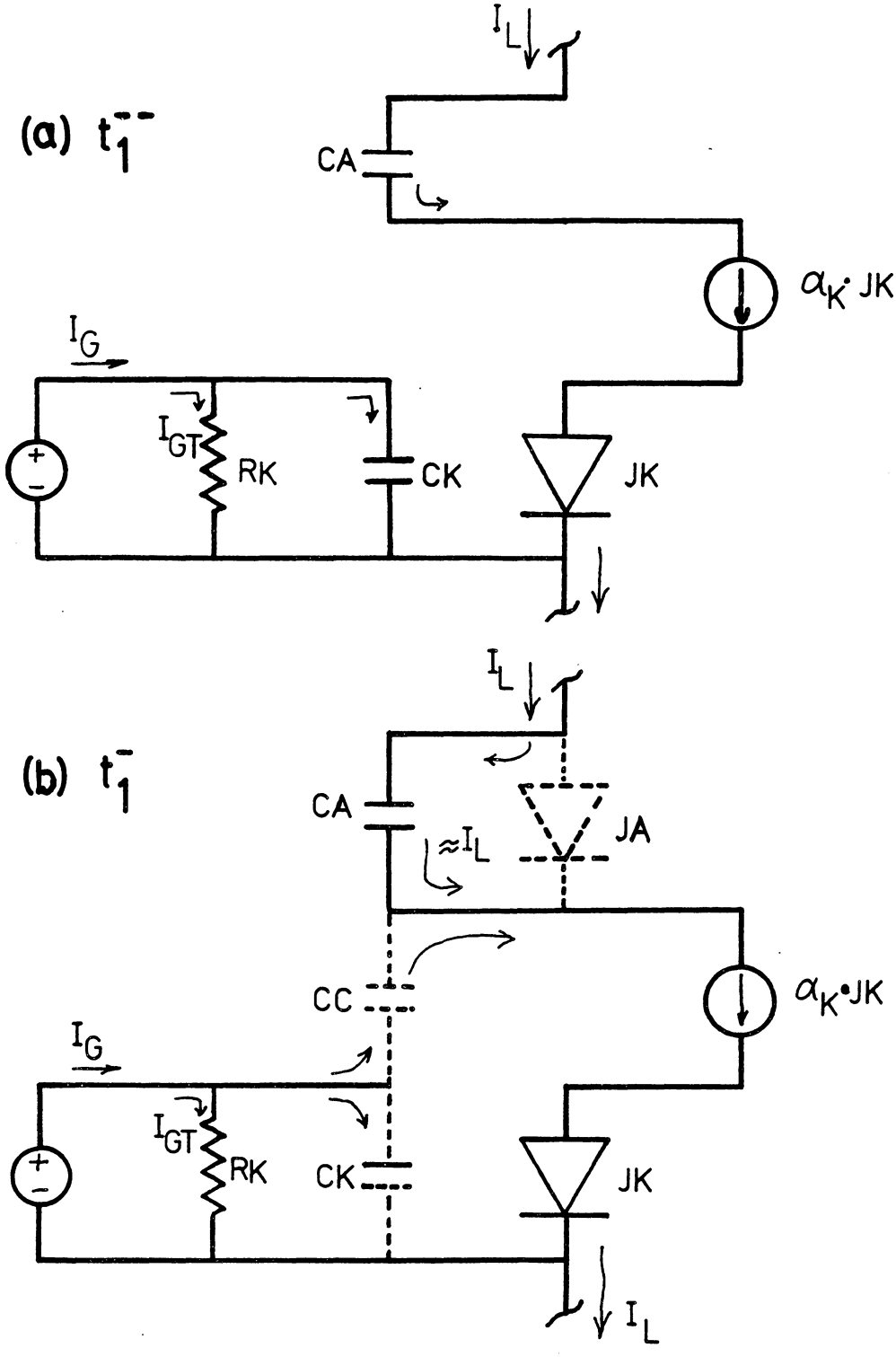


Fig. 8.13. J^3 Model Behavior Immediately Before Removal of Gate Pulse at t_1 as Anode Current Approaches I_L.

As has previously been discussed, the voltage on CA, V_{CA}, lags behind V_{CK} consequently, the current through JA is negligibly small at time t_1. This is the reason JA is shown with dotted lines in Fig. 8.13. It is on the threshold of becoming significant.

From Fig. 8.13(b) at t_1^-

$$\alpha_A JA + \alpha_K JK \simeq I_L + I_G - I_{GT} \tag{8.56}$$

which for JA $\simeq$ 0 and $\alpha_K = 1$

$$JK \simeq I_L + I_G - I_{GT} \tag{8.57}$$

where

$$I_{CA} = dQ_{CA}/dt \simeq I_L \tag{8.58}$$

Since JA $\simeq$ 0, then CA has only a depletion layer term, therefore

$$I_L \simeq \left[CA_{DEPL_0} \left(1 - \frac{1}{2}\right) V_{CA} / \left(1 - V_{CA}\right)^{3/2}\right] \left(dV_{CA}/dt\right) \tag{8.59}$$

It is seen from (8.59) that three variables influence I_L. They are CA_{DEPL_0}, $V_{CA}(t_1)$, and $dV_{CA}(t_1)/dt$.

Consider now, the instantaneous removal of the gate pulse. As illustrated in Fig. 8.14, the circuit (i.e. model) adjusts rapidly to a new dynamic operating point. The initial action of the model is as illustrated in Fig. 8.14(a) as time t_1^+. The control variable for JK, V_{CK}, can not change instantaneously as suggested in Fig. 8.12 by the finite drop time of I_A. In order to balance the current equations, CK discharges via CC and RK. Since the drop in V_{CK} must not be more

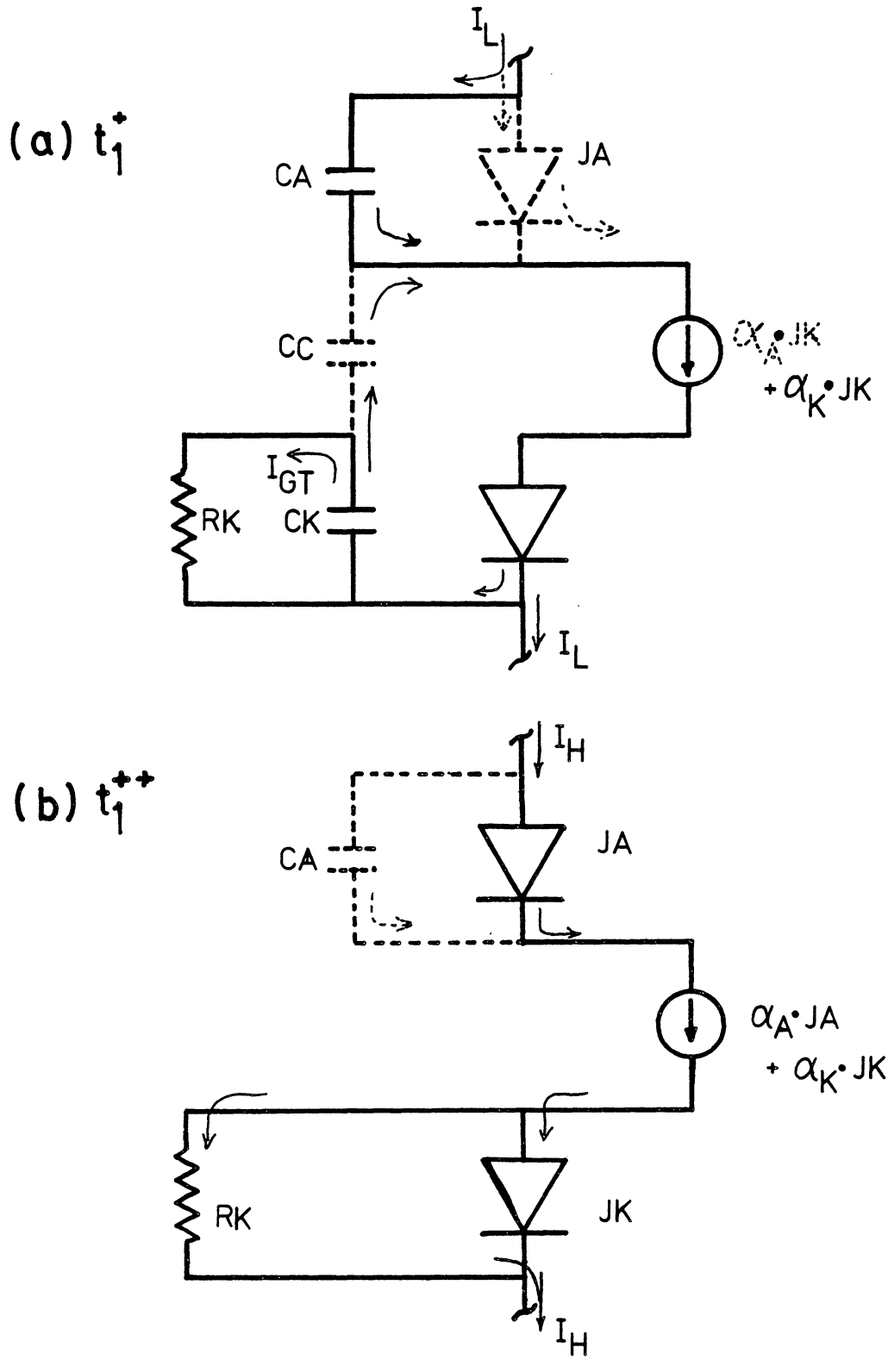


Fig. 8.14. J^3 Model Behavior Immediately After Removal of Gate Pulse at t_1. Anode Current Drops Rapidly from I_L to I_H.

than a few hundredths of a volt, the transient is very short to reach the minimum voltage of V_{CK} for which the SCR model may remain on.

The relationship of CA to this transient is that CA must continue to charge to a sufficient voltage during this very brief interval so as to bring JA into the on state. Fig. 8.14(b) illustrates JA in conduction so that the anode current does not drop below I_H.

Quantitative analysis is not pursued, but might well provide a potential area of future model improvement.

It is seen by this analysis that the latching current phenomena is related to the shunting effect of CA during initial anode current rise. As discussed previously, the junction capacitance terms (CA_{diff}, CC_{diff}) are the mechanism of modeling storage time and transit time delay effects in the SCR and the combination of these terms with a parallel diode provide carrier recombination simulation. The point being that while theory holds that low α_A and α_K are the cause of I_L phenomena, one may look further to see what causes $\alpha_A < \alpha_{Amax}$ and $\alpha_K < \alpha_{Kmax}$. The cause is the implicit relation between charge build-up near the anode junction and anode current itself. From this implicit relation, it is seen that the model does provide a first order simulation of reduced current injection into the collector-gate region from the anode during low current operation of the turn-on transient.

8.6.1.4 Rise Time Analysis

Definition of Rise Time

SCR rise time is a complex dynamic behavior which involves both the load loop defined by equation (8.8) and the gate loop defined by equation (8.9). The device equivalent circuit for $t_d < t < (t_d + t_r)$ is shown in Fig. 8.15.

Rise time is slightly a misnooner in that it is typically defined as the time for V_{AK} to drop from .9 V_D to .1 V_D with V_D given in spec sheet data. For the case of a purely resistive Z_L, the terminology is appropriate, however. Spec sheet data usually specifies either I_T or R_L.

Influence of Gate Pulse on Rise Time

The gate pulse is typically present during t_r. In this sense t_r is a gate driven characterization. It is influenced substantially by I_G in turn-on to low I_T. Due to the influence of parasitic inductances in switching high currents, rise time specs are usually to relatively low I_T. Some specs give a low gate drive spec and a high gate drive spec. The appropriate gate drive parameters for use in the model are those most nearly consistant with gate drive used to determine t_d.

Spec sheet data required to analyze t_r are V_G, R_G, I_{GT}, I_T (or R_L), V_D, t_r.

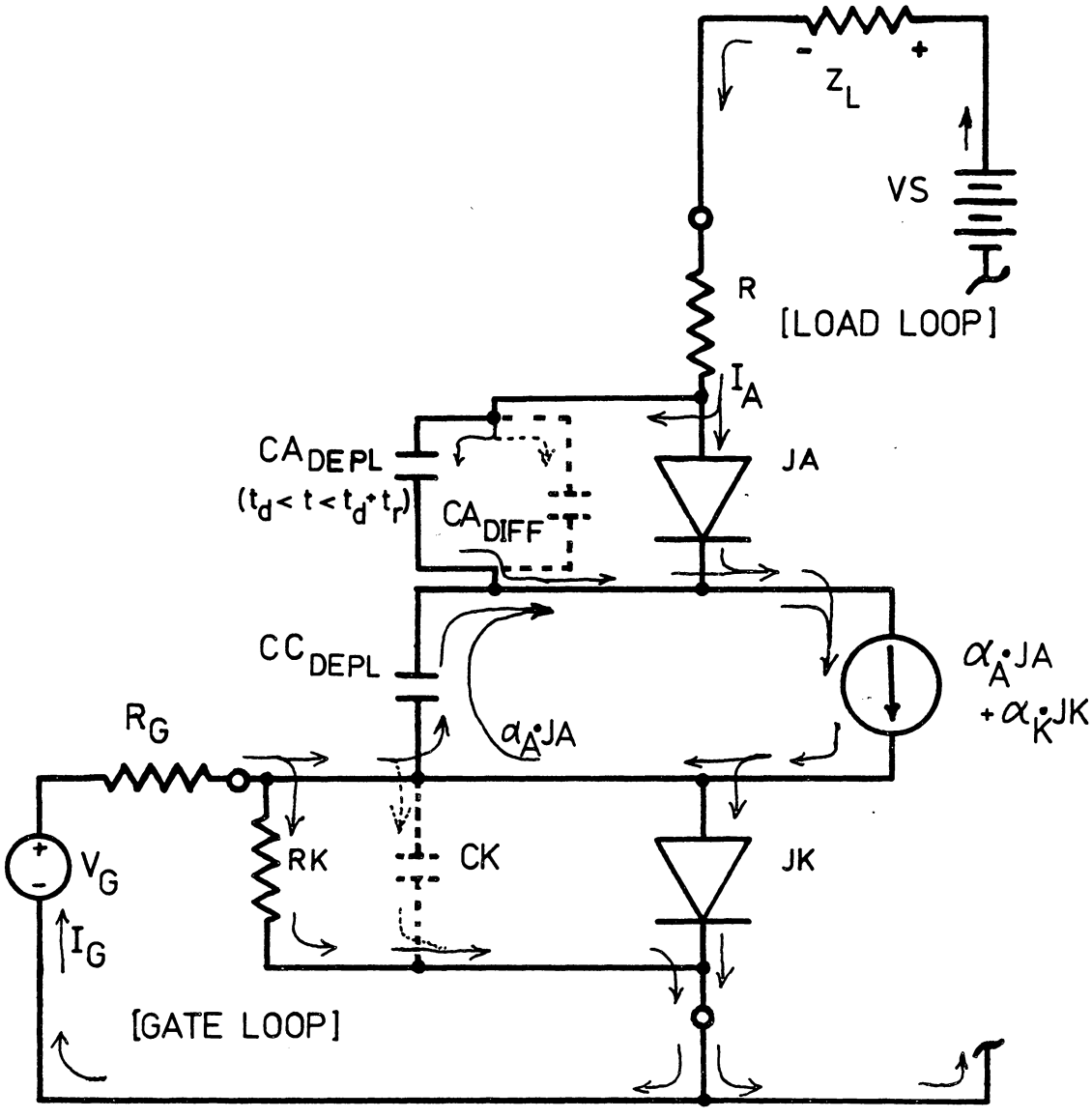


Fig. 8.15. Rise Time Dynamic Model.

From Fig. 8.15 it is seen that rise time is the time required to change the charge on CC from approximately

$$\frac{-.9\ CC_{DEPL_0} V_D}{[.9\ V_D]^{1/2}} \quad \text{to} \quad \frac{-.1\ CC_{DEPL_0} V_D}{[.1\ V_D]^{1/2}} \ .$$

This change is accomplished by current $I_G - I_{GT} + \alpha_A JA - CK\frac{dV_{CK}}{dt}$ flowing through CC_{DEPL}. Clearly the influence of I_G while $\alpha_A JA$ is small is substantial.

Influence of $\alpha_A JA$ on Rise Time

The current $\alpha_A JA$ is a dynamic quantity exponentially dependent on the voltage V_{CA}. V_{CA} is in turn dependent on the charge build-up in CA as controlled by

$$\frac{V_S - V_{CC}}{Z_L} - JA \ .$$

The response time of JK is faster than that of JA (due to $CK \leq CA_{DEPL}$, $V_{CA} > 0$) so consequently it need not be closely analyzed in the highly regenerative portion (rise time) of turn-on behavior.

The rise time process may thus be summarized as follows. A drop in V_{CC} due to charging by I_G and $\alpha_A JA$ produces an increase in $I_A - JA$ which charges CA to a higher V_{CA} thus increasing JA and consequently $I_G + \alpha_A JA$. The cycle then repeats until limited by the external resistance, Z_L.

Influence of Junction Capacitances on Rise Time

The complexity of rise time analysis is due to the presence of the three non-linear capacitance terms, CA_{DEPL}, CA_{DIFF}, and CC_{CEPL}. The following analysis is used to define the transient.

CC_{DEPL} During Rise Time

Using a linear approximation for the fall in V_{AK} during t_r and noting that during this period $V_{CC} \simeq V_{AK}$ then (reference fig. 8.16)

$$I_{CC} \simeq CC_{DEPL} \frac{(.9\ V_D - .1\ V_D)}{t_r} \qquad (8.60)$$

$$\simeq CC_{DEPL} \frac{(.8\ V_D)}{t_r}$$

which is on the order of amperes even for very small CC_{DEPL}.

This provides support for use of the α_K = unity assumption because CC_{DEPL} provides a shunting path for I_G during t_r thus preventing drastic rise in V_{CK} during t_r. This is consistant with true physical behavior.

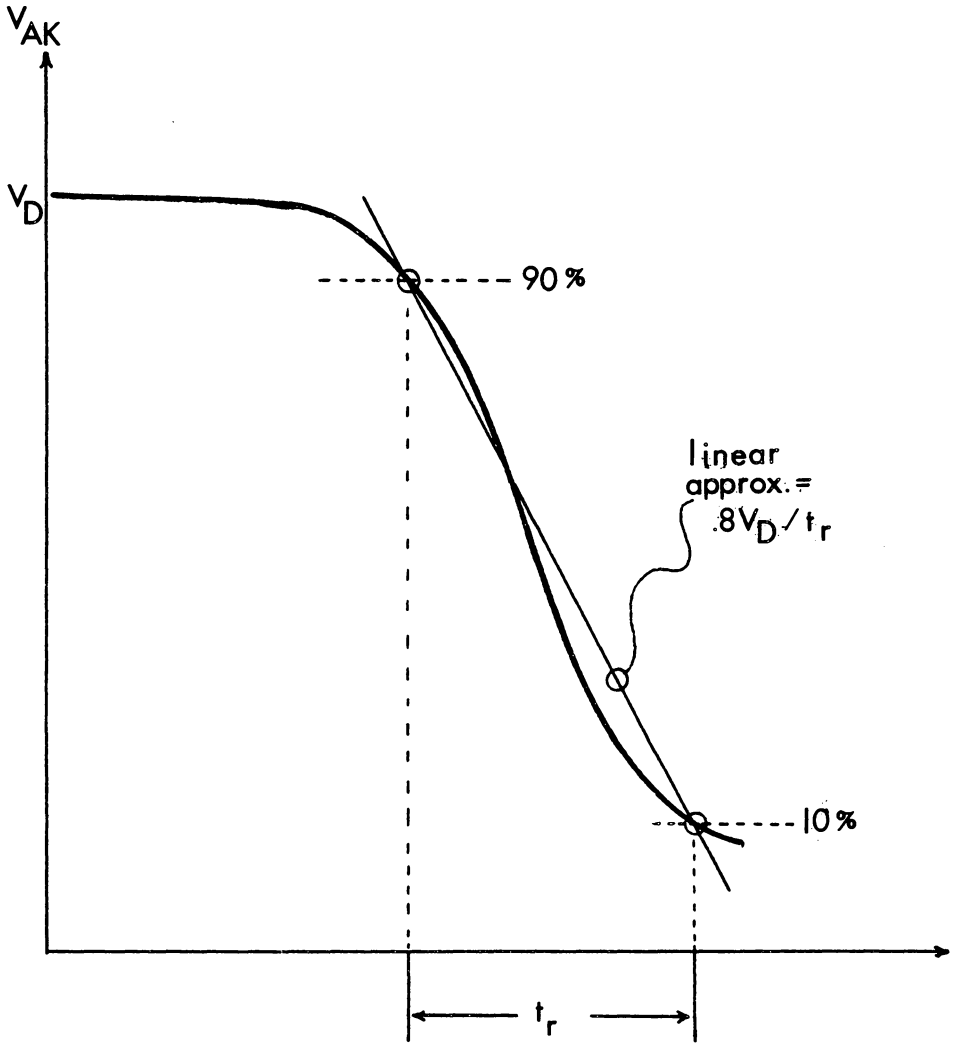


Fig. 8.16. Anode Voltage Characteristics During SCR Turn-on

Here too is the critical rationale leading to a choice between a linear and a non-linear CC_{DEPL}. A non-linear CC_{DEPL} provides the dynamic on state anode-cathode voltage characteristic which is illustrated in Fig. 8.16. V_{AK} drops rapidly from the 90% V_D to the 10% V_D value, continued decline in V_{AK} is much slower. The characteristic is consistant with the dynamic variation in CC_{DEPL} as a $[V_{CC}]^{-1/2}$ non-linearity.

Previous modeling efforts [1,8] have consigned this effect to current spreading resulting in resistivity modulation of the bulk regions. Agreed that it is a two dimensional effect. This model is built on the hypothesis that the dominant two dimensional effect is the charging of junction capacitance as successively greater regions of the device collector region are brought into conduction.

To achieve simulation of the spreading characteristic, one might add a dynamic area factor multiplier to the depletion layer capacitance CC_{DEPL}. No attempt to do that is made here.

CA_{DEPL} and CA_{DIFF} During Rise Time

Having previously bounded CA_{DEPL} by equation (8.25), analysis of t_r consists of defining CA. This capacitance consists of two terms as defined by (8.2)

$$CA = \frac{CA_{DEPL_0}}{\left[1 - V_{CA}\right]^{1/2}} + \frac{\tau_A}{\theta} I_{SA} e^{V_{CA}/\theta} \qquad (8.61)$$

A theoretical digression on the respective influence of these terms is as follows.

The diffussion term significance is a function of two variables τ_A and V_{CA}. τ_A is typically on the order of micro-seconds and therefore the diffussion term may start to become relatively significant only after V_{CA} is positive by a few tenths of a volt.

Physically, τ_A is the combination of two time constants. One, τ_d, is the time for holes, injected from P1 region into the N1 (ref. Fig. 8.17), to diffuse to the edge of the collector junction depletion layer. The other, τ_r, is the life time before recombination with an election in bulk neutral region of N1 between the anode and collector junction depletion layers. This later is a material property.

For $-V_{CC}$ large (i.e. wide collector depletion region) and V_{CA} small positive (i.e. anode depletion region not yet reduced to minimum) τ_d is very small. Conversely as $|-V_{CC}|$ decreases during turn-on and V_{CA} increases, the width of the N1 neutral region increases and τ_d increases correspondingly.

Usually τ_d is on the order of micro-seconds while τ_r may be on the order of milliseconds. The effective time constant is

$$\tau_A = \frac{\tau_d \tau_r}{\tau_d + \tau_r} \simeq \tau_d \qquad (8.62)$$

From manufacturer's spec sheet data, it is surmized that the turn-on transient is usually defined from relatively high V_{AK}.

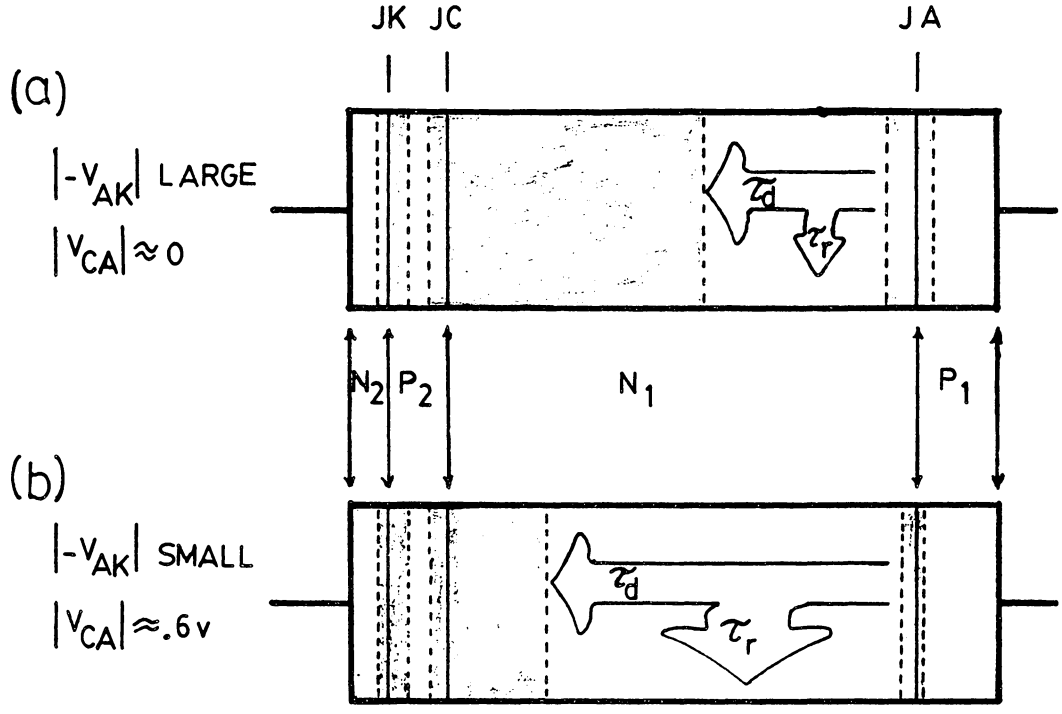


Fig. 8.17. Variation of τ_A with Junction Depletion Layer Width.

The influence of the CA_{DIFF} in the J^3 model is therefore constrained to be insignificant during the initial rise time transient. In order to establish a boundary point for relative significance, the arbitrary definition is made

$$CA_{DIFF}(.1\ V_D) \approx CA_{DEPL}(.1\ V_D) \tag{8.63}$$

The effect of this is that the two terms are of equal significance at the end of the rise time interval. This point marks the start of the spreading interval characterized by a slowed increase in I_A to I_T.

In terms of J^3 model performance, the increasing size of CA, due to CA_{DIFF}, at high currents provides a shunting effect to JA thus somewhat reducing the rate of increase of charging currents to CC. It was previously discussed, however, that a special nonlinearity to CC would be a vehicle of simulating spreading effects. The J^3 model does not have simulation of spreaded developed here.

The major potential role of CA_{DIFF} is to provide a vehicle for quantitative simulation of charge recovery in the terminal characteristics during commutation.

Spec sheets sometimes provide data on charge recovery. It is strongly dependent on forward current and rate of anode current turn-off. Both of these factors are represented in CA_{DIFF} which is a linear function of the JA. Future development is suggested to improve the model in this respect.

The J^3 model functions of CA_{DEPL} and CA_{DIFF} are now defined. CA_{DEPL} is quantified to define rise time, t_r, and CA_{DIFF} provides a qualitative simulation of reverse recovery currents in the anode current characteristic.

Quantification of CA_{DEPL_0}

Equation (8.25) set a constraint on the value of CA_{DEPL} which must be maintained since J^3 operational development to this point has included that constraint. The task at this point is to examine the functioning of CA_{DEPL} to see what if any additional quantifying guidelines may be developed.

The investigative procedure will proceed similarly to previous development. That is, the J^3 model circuit analog behavior will be examined to determine defined operating points in terms of spec sheet data. In the event of no exact references or well known theoretical concepts, arbitrary definition will be established to facilitate progress.

It is important to keep in mind that the modeling process is the designing of a circuit analog to function in a manner which will simulate specified SCR characteristics. It aids user understanding of the models performance if the circuit is constructed to resemble in structure and operational principle the actual device being modeled. Exact duplication of physical theory is not always possible and is frequently not practical. In such cases, approximation "the tool of engineering" must be employed without reservation.

From the static analysis in section 8.6.1.3 it was shown that in order for the model to continue to turn-on in the event of removal

of the gate pulse, the current through JA must conform to the relation, $\alpha_A JA > I_{GT}$. It was also defined that current in JA must reach the value at $.8\ t_d^{++}$ without gate drive. Consider then that with gate drive, $\alpha_A JA$ must reach a value greater than I_{GT} even sooner, say $.8\ t_d^{+}$, or simply at $.8\ t_d$.

This operating point at $.8\ t_d$ was arbitrarily established, however proceeding in time to the next identifiable operating point, that point is at $(t_d,\ .9\ V_D,\ .1\ I_T)$.

The question is, can some analytical judgement be made to distinguish that portion of the terminal current, $.1\ I_T$, which flows through JA in the model from the CA displacement currents.

The following relationships are examined

$$\alpha_A JA(.8\ t_d) \approx I_{GT}$$

$$\frac{dQ_{CA}}{dt}(t_d) + JA(t_d) = .1\ I_T \tag{8.64}$$

In order for the first part of (8.64) to hold, then,

$$\begin{aligned} V_{CA}(.8\ t_d) &\approx .026\ \ln\left\{\frac{I_{GT}}{I_{SA}}\right\} = .75V + .026\ \ln\left\{\frac{I_{GT}}{I_H}\right\} \\ &= .75V + .026\ \ln\ (\alpha_A) \\ &\approx .75V \end{aligned} \tag{8.65}$$

Examining the second part of (8.64) consider that the anode current in the interval $.8\ t_d < t < t_d$ will increase approximately an order of magnitude from $I_A(.8\ t_d)$ on the order of tenths of amperes to

$I_A(t_d)$ on the order of amperes. Given t_d on the order of 1. to 2. micro-seconds, then the interval in question is on the order of .2 to .4 microseconds.

It has been previously stated that it is J^3 modeling strategy to have CA_{DEPL} of sufficiently large value so as to force initial rise time transient to be a gate controlled behavior via the charging of CC_{DEPL} by gate current.

Satisfying this requirement means that CA_{DEPL} must absorb much of the anode current during this interval, $(.8\ t_d,\ t_d)$ without experiencing sufficient rise in voltage so as to cause JA to become significant.

Arbitrarily limiting $JA(t_d)$ to be

$$JA(t_d) \simeq .02\ I_T$$
$$\simeq 200 \text{ ma typical} \qquad (8.66)$$

will satisfy the above mentioned concerns.

Using (8.66) the second part of (8.64) is now,

$$\frac{d}{dt} Q_{CA}(t_d) \simeq .08\ I_T \qquad (8.67)$$

Now to form a linear approximation for the charge absorbed in CA_{DEPL} during the interval, $(.8\ t_d,\ t_d)$, let the displacement current vary linearly from zero at $.8\ t_d$ to $.08\ I_T$ at t_d. The charge absorbed in CA_{DEPL} is approximated by

$$\Delta Q_{CA} = \frac{1}{2}\ (.08\ I_T)(.3\ \mu s) = 12\ I_T \times 10^{-9} C \qquad (8.68)$$

At $V_{CA} \approx .75V$, CA_{DEPL} has a nominal value of,

$$CA_{DEPL}(V_{CA} = .75V) = 2\ CA_{DEPL_0}. \tag{8.69}$$

Allowing only a .02 to .03 increase in V_{CA} due to absorption of ΔQ_{CA} as given by (8.68) requires,

$$CA_{DEPL_0} \approx \frac{(12I_T \times 10^{-9}C)}{(2)(.02V)} = \left|.3I_T\right| \mu F \tag{8.70}$$

which for $I_T \geq$ 10A is very close to expected values of CK.

It remains then to examine the status of the anode junction terms near the end of rise-time, (t_d+t_r).

The operating point to be examined is $((t_d+t_r), .9V_D, .9I_T)$. The main concern is to assure that the current $\alpha_A JA$ becomes the dominant charging current for CC_{DEPL} near the end of rise time thus replacing I_G as the most significant factor in controlling turn-on behavior.

In numerical algorithms, the diode junction capacitance depletion layer term is usually limited in its maximum forward biased value both to provide numerical stability and to conform to physical reality as predicted by Gummel-Poon PN junction theory.[10]

In SPICE2, this limit is set by limiting $V_{FB} \approx .9\psi_0$ which for ψ_0 defaulted to 1. gives $V_{FB} = .9$. Applying this to equation (8.2) gives

$$C_{DEPL\text{-}max} \approx 3\ C_{DEPL_0} \tag{8.71}$$

In the rise time interval

$$CA \approx CA_{DEPL} = CA_{DEPL_0}/[1-.77-\Theta\ln(JA/.02I_T)]^{1/2} \tag{8.72}$$

Using (8.70) in (8.72) gives

$$CA \approx .3I_T/[.33-\Theta\ln(JA/.02I_T)]^{1/2}\mu F \tag{8.73}$$

From (8.73) it is seen that JA may reach approximately 1400 Amps before incurring this boundary, therefore it need not be given special consideration here during rise time estimations.

Now at $((t_d+t_r), .1V_D, .9I_T)$, let

$$\alpha_A JA(t_d+t_r) \approx I_G \Rightarrow JA(t_d+t_r) \approx \frac{I_G}{\alpha_A} \tag{8.74}$$

This requires that

$$V_{CA}(t_d+t_r) = .75V + \Theta\ln\left\{\frac{I_G}{\alpha_A I_H}\right\} \tag{8.75}$$

$$= .75V + \Theta\ln\left\{\frac{I_G}{I_{GT}}\right\}$$

which for typical values of $I_G = 2A$ and $I_{GT} = .1A$ gives,

$$V_{CA}(t_d+t_r)_{typ} = .83V \tag{8.76}$$

Now taking a linear approximation of dV_{CA}/dt during rise time to be

$$dV_{CA}/dt\Big|_{\text{linear approx}} = (V_{CA}(t_d+t_r) - V_{CA}(t_d))/t_r \tag{8.77}$$

which for typical values of (8.66) and (8.76) gives

$$\begin{aligned} \Delta V_{CA}/\Delta t\Big|_{\text{typ.}} &= .02 + \Theta \ln\{I_G/I_{GT}\} \\ &= .07/t_r \end{aligned} \tag{8.78}$$

Observe that $JA \approx I_G/\alpha_A \approx I_G << I_T$ so that for the anode junction at (t_d+t_r)

$$.9I_T \approx dQ_{CA}/dt \approx CA_{DEPL_0}\left(\frac{\Delta V_{CA}}{\Delta t}\right)\frac{(1-V_{CA}/2)}{(1-V_{CA})^{3/2}} \tag{8.79}$$

Using (8.78) and (8.76) in (8.79) gives

$$CA_{DEPL_0} \approx |1.5\ I_T t_r|\ F \tag{8.80}$$

Comparing (8.80) to (8.70), it is seen that the use of the clumsy linear approximations produces predictions of CA_{DEPL_0} which are well within an order of magnitude. Both predictions when considering typical values of I_T and t_r call for CA_{DEPL_0} on the order of CK. This is consistent with (8.25).

One other avenue exists by which to examine the interaction of I_G and $\alpha_A JA$ during the turn-on rise time transient.

Take the system dynamic equations (8.4), (8.5), and (8.6) and perform some algebra to obtain, (α_K=1., $I_{RK} \approx I_{GT}$),

$$\frac{d}{dt}Q_{CA} + (1-\alpha_A)JA - JK + \frac{d}{dt}Q_{CC} = 0 = -I_G + I_{GT} - \alpha_A JA + \frac{d}{dt}Q_{CC} + \frac{d}{dt}Q_{CK} \tag{8.81}$$

The right portion of (8.81) gives

$$JA = (1/\alpha_A)[\frac{d}{dt}Q_{CC} - I_G + I_{GT} + \frac{d}{dt}Q_{CK}] \tag{8.82}$$

It is the objective to try and identify a relationship between dQ_{CC}/dt and $\alpha_A JA$ during the t_r transient. Since I_G and I_{GT} are easily identified to a close approximation, then attention must first be given to dQ_{CK}/dt.

From the circuit of figure 8.1 it is seen that the load loop current flows entirely through JK. The total current through JK is given by (refer. figure (8.13)),

$$JK = I_{SK}e^{V_{CK}/\Theta} = I_A + I_G - I_{GT} - CK\frac{dV_{CK}}{dt} \tag{8.83}$$

Observe that

$$dI_A/dt = dJK/dt = (I_{SK}/\Theta)e^{V_{CK}/\Theta}(dV_{CK}/dt)$$
$$= (JK/\Theta)(dV_{CK}/dt) \tag{8.84}$$

Now looking external to the model, it is seen that

$$dI_A/dt = |dV_{AK}/dt|/Z_L \approx |dV_{CC}/dt|/Z_L \tag{8.85}$$

Using the linear approximation as illustrated in figure 8.16 and combining (8.84) with (8.85) gives

$$.8V_D/(t_r Z_L) = (JK/\theta)(dV_{CK}/dt) \tag{8.86}$$

Using (8.83) for JK and some algebra yields the quadratic equation

$$(dV_{CK}/dt)^2 + ((I_{GT}-I_A-I_G)/CK)(dV_{CK}/dt)$$
$$+ .8\Theta I_T/(t_r CK) = 0 \tag{8.87}$$

Roots for (8.87) are

$$(dV_{CK}/dt) = \frac{1}{2}\left\{\frac{(I_A+I_G-I_{GT})}{CK} \pm \left[\left(\frac{I_A+I_G-I_{GT}}{CK}\right)^2 - \frac{.0832\ I_T}{t_r CK}\right]^{1/2}\right\} \tag{8.88}$$

units: V/S

Obviously, the solution to (8.88) must be real for the model to function. Also observe that the concern is for $.1I_T < I_A < .9I_T$. It is not clear which of the solutions to (8.88) will hold. Resolution of that question will require consideration of other factors beyond those given at this time (in particular, the behavior of dQ_{CA}/dt).

Rewriting (8.82) to reflect (8.24) and the linear approximation to dV_{CC}/dt gives,

$$JA = (1/\alpha_A)\left[\frac{CC_{DEPL_0}(1-V_{CC}/2)}{(1-V_{CC})^{3/2}}\left(\frac{.8V_0}{t_r}\right) - I_G + I_{GT} + CK(dV_{CK}/dt)\right] . \tag{8.89}$$

Careful examination of (8.89) in conjunction with both possible solutions to (8.88) reveals that in the presence of a strong I_G and the fact that CC_{DEPL_0} is approximately two orders of magnitude less than CK, $|V_{CC}|$ must be approaching zero (relative to V_D) for JA to exceed I_G.

Although no closed form analytical solution for CA_{DEPL_0} has been derived, it is felt that the exploratory efforts to this point provide adequate support for the defining relationship of (8.25). It is therefore applied to the J^3 model.

Quantification of the Anode Diffusion Constant, τ_A

All is not complete for the anode junction, however. Quantification of τ_A, the anode injection current diffusion time constant, must be provided.

In keeping with the constraint of (8.63) and previous discussion that CA_{DIFF} will serve the J^3 model as the source of reverse recovery currents, then since,

$$\alpha_A JA(t_d+t_r) \approx I_G \approx (V_G-.75)/RG \tag{8.90}$$

Then,

$$\tau_A = (\Theta/I_G)\left\{CA_{DEPL_0}/(1-V_{CA}(t_d+t_r))^{1/2}\right\} \tag{8.91}$$

$$\tau_A = (\Theta R_G/(V_G-.75))\left\{CA_{DEPL_0}/(.25-\Theta \ln\left\{\frac{V_G-.75V}{\alpha_A R_G I_H}\right\})^{1/2}\right\} \tag{8.92}$$

8.6.2 Turn-off Transient Analysis

The turn-off transient of the SCR is the most difficult of its dynamic preformances to characterize. This difficulty is embodied in the diversity of physical structures (in terms of semi-conductor properties) utilized by manufacturers to achieve desirable device operation appropriate to application intended.

Since turn-off commutation time, t_q, is typically the most critical parameter in circuit design applications and also the parameter for which manufacturers data sheets provide the best characterization, it is the term to be quantified by the J^3 model.

The t_q as shown in fig. 8.5 is the time from which anode current goes to zero with negative di/dt until the device regains the ability to support a forward voltage reapplied at a specified dV/dt.[22,29,31]

As shown in fig. 8.5, the terminal characteristic of the SCR has two prominent features during the t_q interval. The first of these is the t_{rr} which features a negative current pulse. The device behavior giving rise to this pulse was detailed in [23] and Chapter 2. Only qualitative simulation of this feature is provided by the J^3 SCR model. via CA_{DIFF}.

The second prominent feature of t_q as shown in fig. 8.5 is the long period of very low $-I_A$ denoted t_{qr}. The device physical behavior during this interval is also described in Chapter 2. Additional digression on this subject is provided here, however, in order to support the rationale of the J^3 model.

Circuit Variables Used in Quantifying t_q

As mentioned previously, turn-off, and in particular, t_q, is difficult to quantify. This is because t_q is a function of five circuit controlled quantities [22] as well as device temperature. This rendition of the J^3 model has temperature as a parameter in the diode equation thermal voltage, Θ, but is held constant at 25°C. Of the five

circuit controlled parameters, only three, forward current, I_T, reapplied dV/dt and reapplied forward voltage level are utilized in quantifying t_q with the J^3 model. The other two parameters are reverse di/dt and reverse voltage $-V_{AK}$. While not quantified in the analysis of Vt_q, both of the latter quantities affect t_q qualitatively in the appropriate directional trend.[22, p. 624]

Reverse di/dt only moderately affects t_q[22,29,31] and therefore is not discussed here.

On the other hand reverse voltage may significantly affect t_q as will be illustrated in the digression on device turn-off to follow. Unfortunately while the J^3 model does possess a vehicle for simulating reverse voltage effects via CA_{DEPL} the spec sheet does not provide sufficient data to support analytical modeling.

8.6.2.1 A Digression on SCR Turn-off Behavior

Turn-off Phases I, II, III, and IV

As explained in Chapter 2[1,8,11,14] the SCR turn-off behavior may be segregated into four phases (ref. fig. 8.18(a)).

The first phase is short in duration and concerns the charge removal, reverse biasing and avalanche breakdown of the gate to cathode junction, JK (ref. fig. 8.118(b)).

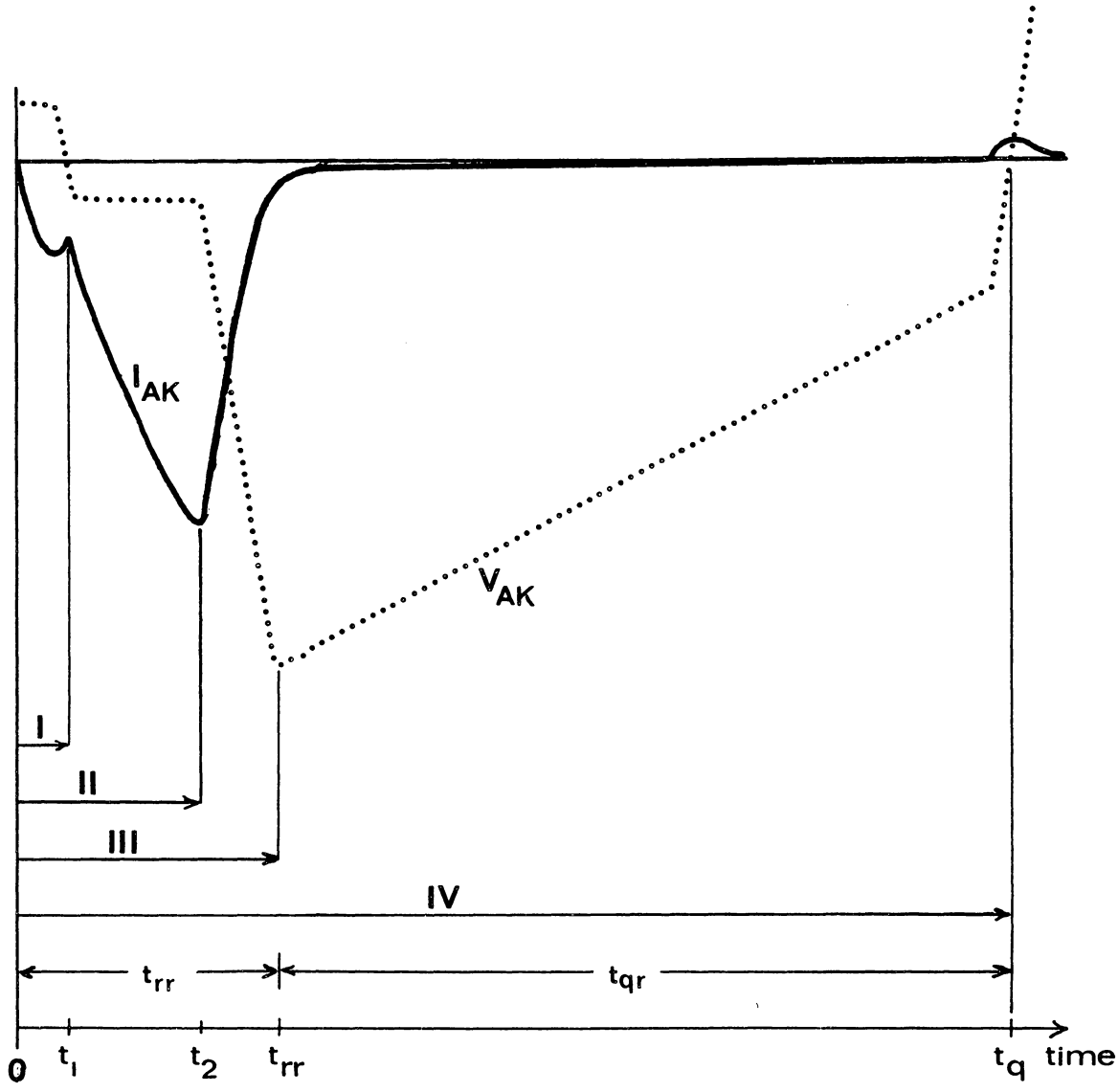


Fig. 8.18(a). Relationship Between Turn-off Transient Phases.

TURN OFF PHASES

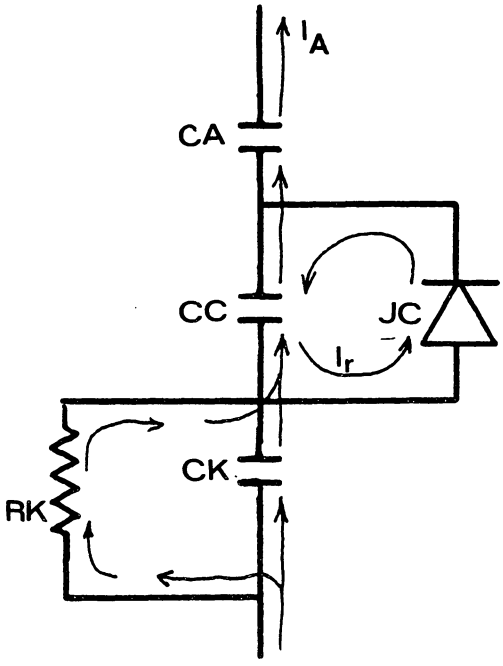


Fig. 8.18(b).
Phase I, II, III, IV.

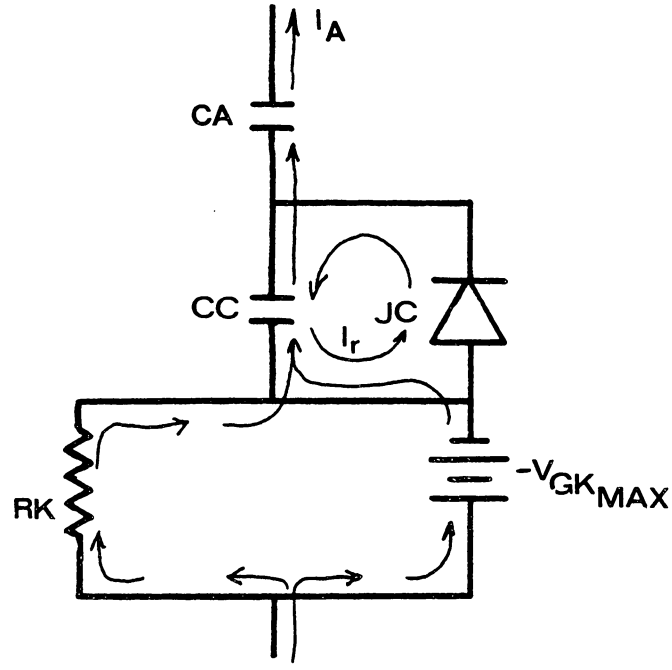


Fig. 8.18(c).
Phase II, III, IV.

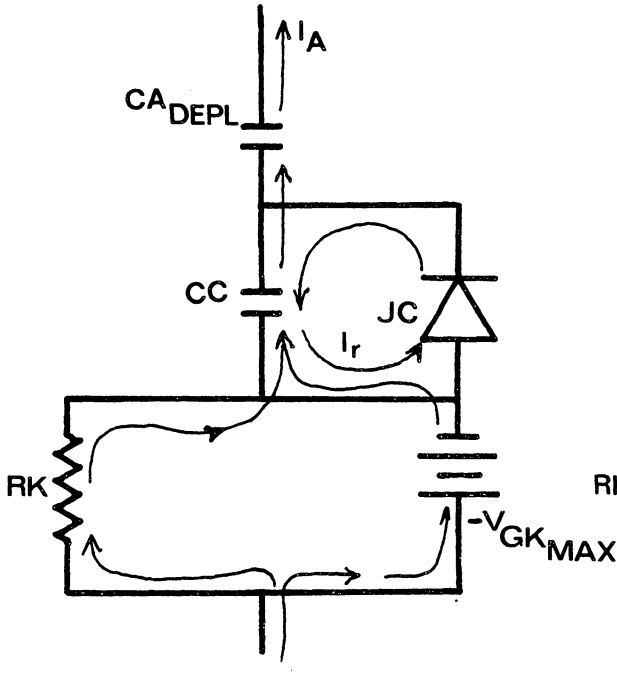


Fig. 8.18(d).
Phase III, IV.

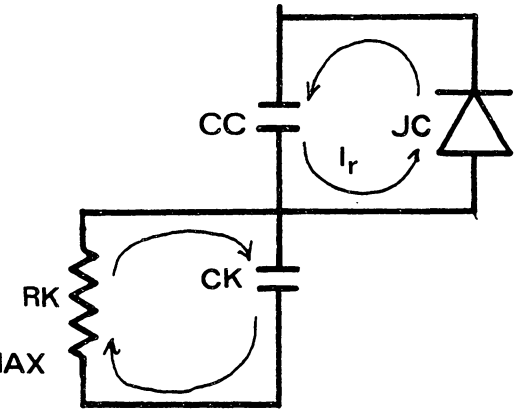


Fig. 8.18(e)
Phase IV.

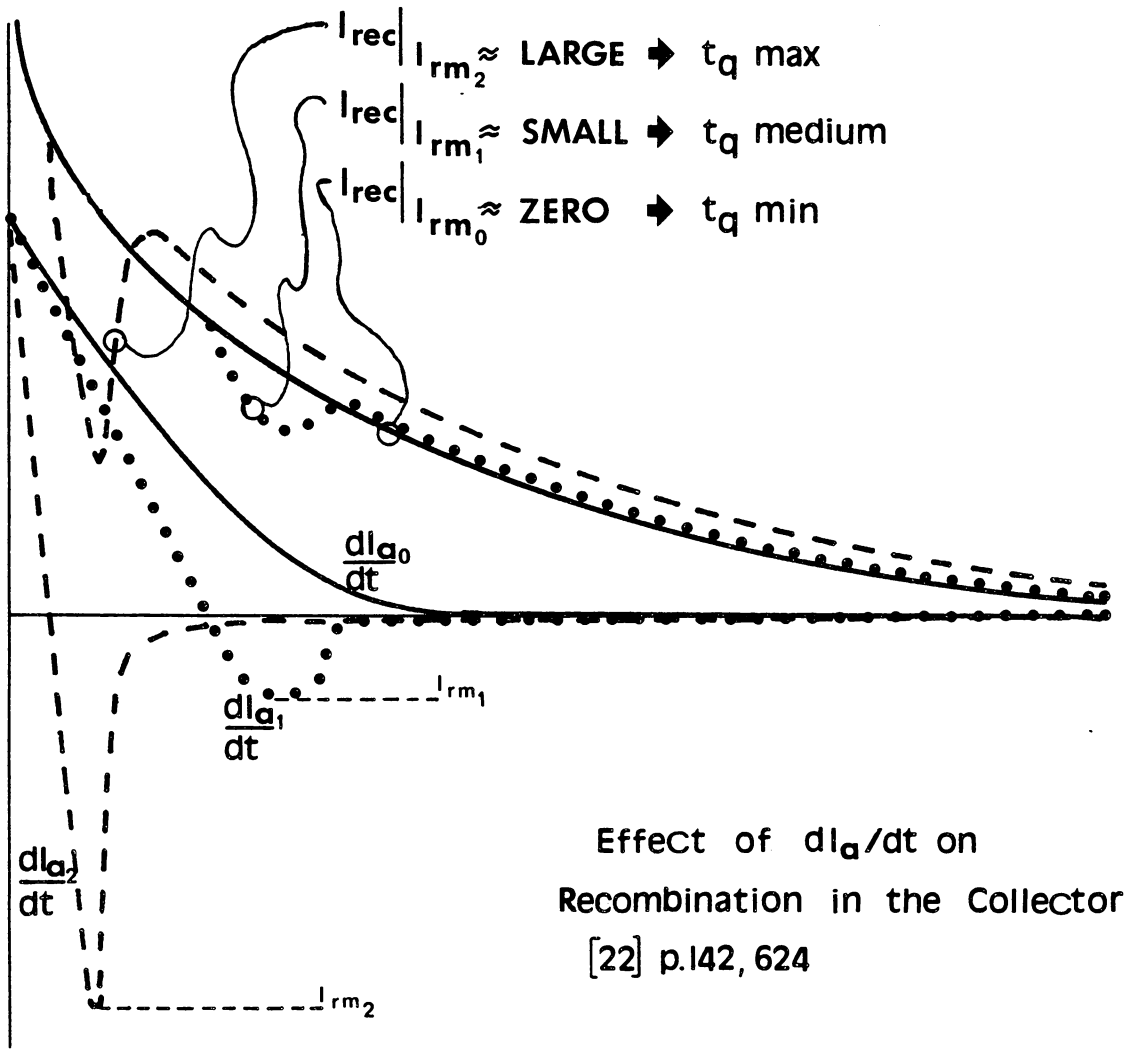


Fig. 8.18(f). Effect of di_A/dt on Recombination in Collector.

All parameters to be used in modeling for this phase have previously been determined with the exception of the JK junction breakdown voltage. This parameter is determined identically to the "modified Hu-Ki" Model[23]

$$V_{BO_K} = \left\{ \begin{array}{l} 1.1\ X - V_{GK}\ \text{(spec. sheet)} \\ \\ \text{or 5V [11, p. 87]} \\ \\ \text{1.V for very short } t_q \text{ devices.} \end{array} \right\} \qquad (8.93)$$

The second phase is the storage time of the anode junction diffusion capacitance which is also very short in duration and is manifested in terminal characteristics by rising reverse anode current while the device remains unable to support a negative voltage more than the JK breakdown voltage. This phase is also short in duration with respect to t_q (ref. fig. 8.18(c)).

During the third phase, the device begins to support reverse voltage as the JA junction becomes reverse biased. Reverse anode current results from displacement currents in CA_{DEPL_0}. The device terminal behavior is characterized by rising $-V_{AK}$ and falling anode current, I_A (ref. fig. 8.18(d)).

Phase four is the period required for the stored charge in the bulk collector region to recombine to a sufficiently low level such that displacement currents resulting from reapplied dV/dt do not inject sufficient charge into the base region so as to trigger regenerative action leading to turn-on (ref. fig. 8.18(e)).

Analysis of Turn-off Phases by Superposition

Although it is useful to discuss the four phases as being distinct, they are intersecting events in time. It is useful, although not entirely correct, to apply the concept of superposition to allow segregated analysis of each of the phases. Fig. 8.18 illustrates the relationship of each of the four phases with respect to time and the terminal behavior they define.

The justification of the use of superposition is that the events of each of the phases are physically separated within the device.

There are two primary errors affecting the superposition approach. The first is that due to reverse current through the device, there is some degree of coupling between the charge storage behavior of each of the regions. The second error is that the boundary between regions is not necessarily distinct.

Description of Turn-off Mechanism in Phases II, III, and IV

Turn-off behavior of an SCR is described assuming that $t_1 << t_2$ (ref. fig. 8.18(a)).[11,14,23] This is pretty much a standard assumption when analyzing SCR turn-off behavior. The justification is given in Chapter 2.

During turn-off the direction of external applied voltage is such that it tends to forward bias JC and to reverse bias JA. As such the collector bulk region near JC tends to remain in a state of high level injection while that region near JA tends to become depleted of excess charge. The removal of excess charge from near JA occurs as a function of competing lifetimes as was described earlier in turn-on analysis.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_D} + \frac{1}{\tau_r} \quad [33] \tag{8.94}$$

The charge either disappears due to recombination or leaves the region as a displacement current. The latter is manifested as terminal current. The model assumption is that the phase II behavior is localized to very near the JA junction and therefore may be lumped into the model element CA_{DIFF}. It is the magnitude of -di/dt which determines whether τ_D or τ_r is the dominant time constant of phase II. Since -di/dt effects are not quantified in the model, the turn-on time constant, τ_A, is used.

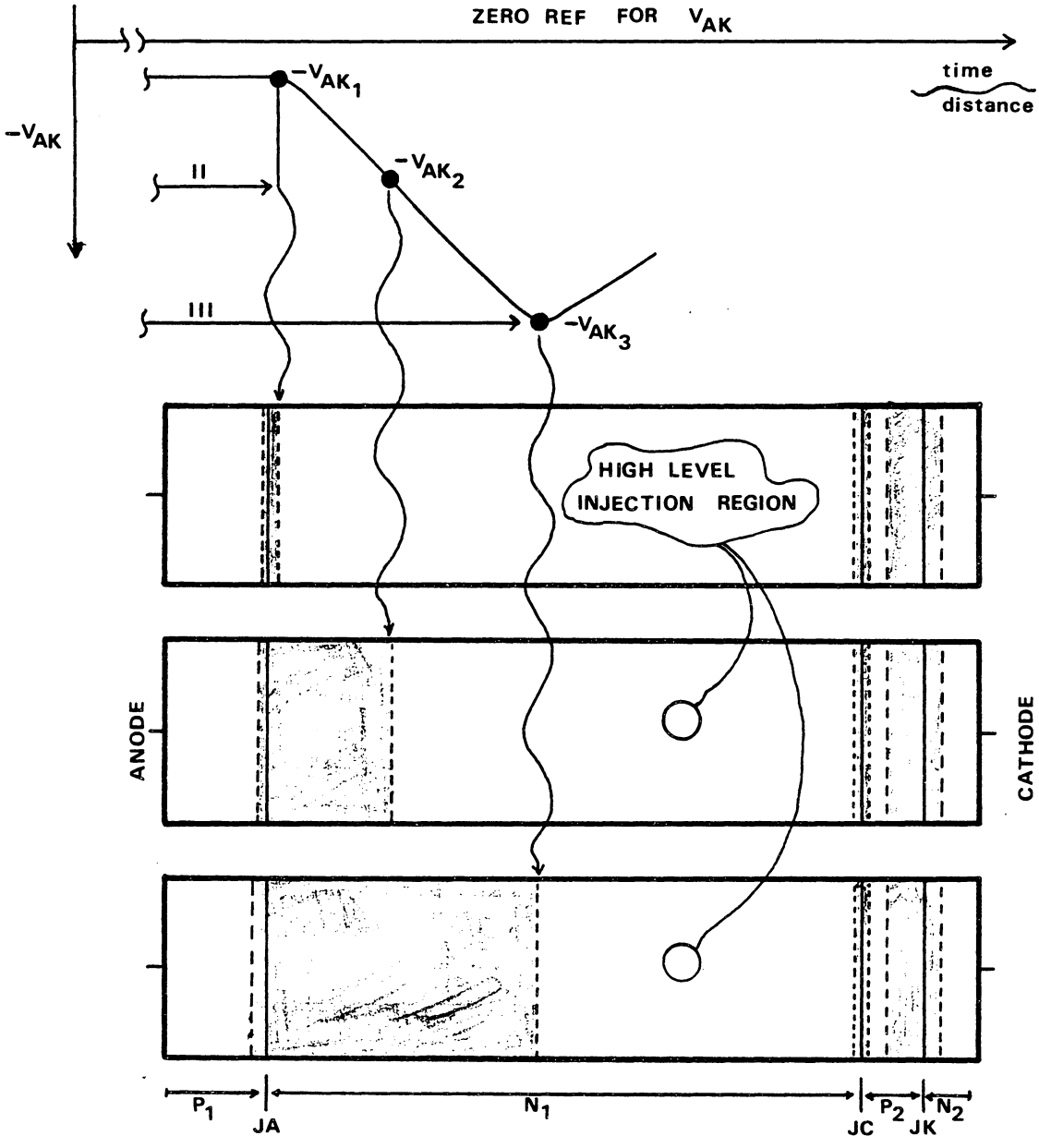


Fig. 8.19. Extension of Anode Depletion Region Into Collector (N1) Bulk Region During Exclusive Portion of Phase III.

Concurrent with the removal of the diffusion charge from the JA region, the ionized layer about the anode junction is being reestablished.

Phase II effectively ends as the Phase III depletion layer charge approaches its equilibrium value. At this point, the depletion layer begins to extend rapidly into the bulk collector region as JA begins to support reverse voltage. Fig. 8.19 depicts this event graphically.

That portion of Phase III exclusive of Phases I and II is characterized by rising $-V_{AK}$ and falling $-I_A$. This Phase III extension of the depletion layer into the collector (N1) region explains the inverse relation of t_q to the magnitude of $-V_{AK}$ applied. The nondepleted bulk collector region, which for the most part is still in a state of high level injection at t_{rr}, is made physically smaller by larger $-V_{AK}$. Therefore, the excess charge contained in the region is less at t_{rr}. Also, the nearer proximity of the depletion region boundary (for large $-V_{AK}$) increases the probability of diffusion out of the region as opposed to remaining in the region until recombination. Again the effect of two competing lifetimes results in a lower effective lifetime and subsequently shorter t_q.

Spec sheet values for $-V_{AK}$ at which t_q is rated are typically much less than the rated reverse blocking voltage. To avert the danger of punch through, devices are usually designed with wide collector regions. Also, the depletion layer widening is a function of $(V_{JA})^{1/2}$ [32] for the abrupt junction approximation. For these reasons $-V_{AK}$ ceases to have much effect on t_q when $|-V_{AK}| \gtrsim 50V$.[22] Most t_q ratings are given for $|-V_{AK}| \geq 50V$. Due to the use of large CA_{DEPL} in the J^3 model, the effects of $-V_{AK}$ appear qualitatively in the model; however, no mechanism is present to simulate the coupling between CA_{DEPL} and CC_{DIFF}.

In the on-state the SCR collector region is subjected to double ended high level injection such that excess charge builds up in the region until recombination equals excess injection. From the J^3 model parameters of α_A and α_K with $\alpha_K = 1$, it is apparent that the steady-state recombination rate must be given by

$$I_{rec.} = \alpha_A I_T = \alpha_A JA \tag{8.95}$$

and that

$$Q_{CC_{DIFF}} = \alpha_A \tau_C JA \tag{8.96}$$

During the turn-off transient, injection into the collector (N1) region occurs only at JC. It is therefore single ended injection. In order for terminal current to be continuous, all carriers injected at JC must emerge at JA.

This suggests that the reference time for beginning recombination of $Q_{CC_{DIFF}}$ is at the point of zero cross-over for I_A.

Now for a recap. It is the objective of the J^3 model to simulate spec sheet t_q. This effect is to be simulated by the discharging of CC_{DIFF} thru JC. Physically, this corresponds to the recombination of the excess charge in the bulk collector region not penetrated by the JA depletion layer during reverse bias due to $-V_{AK}$. This event is denoted phase IV and is decoupled from other turn-off transient events occurring within the device. While this event spans the entire t_q, it is only manifested at the device terminals during the exclusive portion of phase IV illustrated in fig. 8.18 as t_{qr}.

8.6.2.2 Estimation of J^3 Model Parameter τ_C, the Collector Excess Carrier Lifetime

Physically the excess carrier recombination lifetime varies substantially during the turn-off transient. While the region is in a state of high level injection, the recombination lifetime is shorter than that for lower excess carrier concentrations.[32]

The J^3 model assumes one constant characteristic carrier lifetime for the entire interval. Typically τ_C is in the range from .1μs to 10^3μs[22, p. 10].

Estimation of $V_{CC}(t)$ for $V_{CC}(t_q) > V_{CC}(t) > 0$

The analysis begins with estimation of the forward bias of JC (i.e. V_{CC}) necessary to simulate the recombination rate at anode current, I_T.

From (8.95) and $0 \leq t \leq t_q$ (ref. fig. 8.18)

$$V_{CC}(0) \approx \theta \ln(\alpha_A I_T / I_{SC}) \qquad \therefore \ di_A/dt \text{ large.} \tag{8.97}$$

Use of typical values for CC_{DEPL_0} on the order of 10^{-8} - 10^{-7}F and values of τ_C on the order of 10^{-6}S in equation (8.2) reveals that $CC_{DIFF} >> CC_{DEPL}$ for values of $V_{CC} > .5$V. This means that if

$V_{CC}(t_q) > .5V$ then CC_{DIFF} may be expected to influence the reapplied dV/dt rating. On the other hand if $V_{CC}(t_q) \lesssim .5$ then reapplied dV/dt rating is expected to be almost entirely a function of CC_{DEPL}. The latter case implies a reapplied dV/dt rating on the order of the static dV/dt rating.

In order to assess the nature of the decline of $V_{CC}(t)$ from $V_{CC}(0) > .5V$ during $0 < t < t_q$, it desired to determine the slope of $V_{CC}(t)$ during this interval.

Assuming an initial $V_{CC}(t) > .5V$ then analysis of the J^3 model recombination current loop (fig. 8.20) may initially exclude CC_{DEPL} as relatively insignificant. This gives

$$I_{rec} = -\frac{d}{dt} Q_{CC_{DIFF}} = JC \qquad (8.98)$$

One must be careful to avoid the pitfall of applying the definition, $Q(V) = C(V)V$, to the $Q_{CC_{DIFF}}$. Instead, $Q_{CC_{DIFF}} = \tau_C JC$, therefore (8.98) becomes

$$-\tau_C \frac{dJC}{dt} = JC \tag{8.99}$$

Preforming the indicated differentiation and some algebra yields

$$-\int_0^t \frac{\theta}{\tau_C} dt = \int_{V_{CC}(0)}^{V_{CC}(t)} dV_{CC} \tag{8.100}$$

which has solution for $V_{CC}(t)$

$$V_{CC}(t) = V_{CC}(0) - \frac{\theta}{\tau_C} t \tag{8.101}$$

This relationship is shown graphically in fig. (8.20). Experimental results given in [29, p. 2-7] show that the terminal voltage of a diode, turning off from high forward current without reverse current, decays linearly with slope proportional to $-\frac{\theta}{\tau_C}$ until the terminal voltage nears .3V.

Equation (8.101) is then restricted to

$$V_{CC}(0<t<t_q) = V_{CC}(0) - \frac{\theta}{\tau_C} t \tag{8.102}$$

$$\text{for} \quad V_{CC}(t) > .3V$$

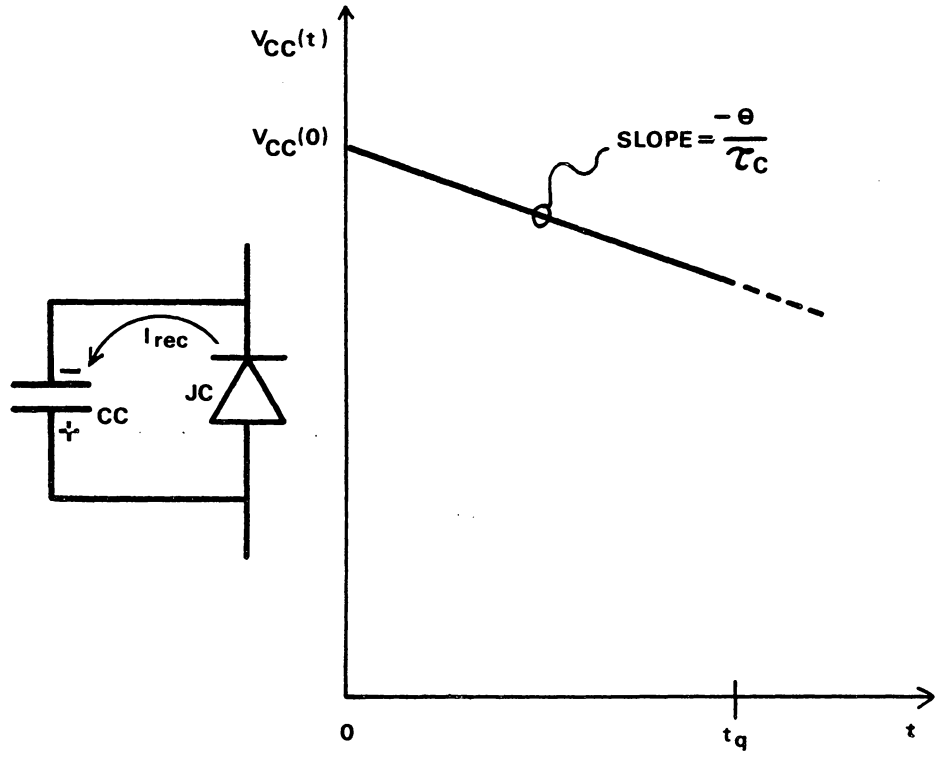


Fig. 8.20. Phase IV Equivalent Circuit and V_{CC} Characteristic During $0 < t < t_q$.

At this point, the boundary value $V_{CC}(0)$ and the transient description for $V_{CC}(0<t<t_q) \gtrsim .3V$ has been established by equations (8.97) and (8.102). Experimental data given in [29, p. 2-7] shows a very rapid decline in $V_{CC}(t)$ after it reaches approximately .3V.

No analysis of this change in $V_{CC}(t)$ dynamics will be attempted. It will be treated, should the need arise, as a discontinuity with $V_{CC}(t) > .3V$ given by (8.102) and for actual $0 < V_{CC}(t) < .3V$, an approximation of $V_{CC}(t) = 0$ will be used.

Manufacturers' Reapplied DV/DT and t_q Ratings

As mentioned previously, the influence of CC_{DIFF} on reapplied dV/dt is expected to be of little impact after $V_{CC}(t) \lesssim .5V$.

Manufacturers' commutation time, t_q, specifications are given as the maximum time required for the device to regain the ability to support a reapplied dV/dt. Commonly occurring values of dV_r/dt are 10, 20, 25, 100, and 200 V/μs. Also the values of t_q which range between 5 to 300 μs are almost invariably integral multiples of 5 μs which suggests a conservative rounding off to some higher value of t_q above actual device capability or alternatively a rounding off of actual device dV_r/dt capability to some lower value.

The point here being that the device commutation ratings are based on choices of operating criteria for which spec sheets give no indication as to the objectivity of the choices. As such, these operating points must be considered as arbitrary choices of either t_q or dV_r/dt with measurement of the corresponding dV_r/dt or t_q rounded off conservatively.

The modeling approach taken here will be to take the spec sheet value of t_q as the fixed point and then adjust model parameter to achieve the specified dV_r/dt rating at this operating point, $(t_q, dV_r/dt)$.

A further observation of spec sheet data reveals that dV_r/dt ratings vary widely as compared to the static dV/dt rating denoted dV_s/dt here.

As mentioned previously, the ratio of dV_r/dt to dV_s/dt is an indicator of the relative significance of CC_{DIFF} to this rating.

The analysis of static dV/dt rurn-on (sec. 8.6.1.2) treated the event as a charge controlled event. That is charge stored in the gate-collector region is transferred to the gate-cathode region by dV_s/dt transient displacement current. Such analysis assumed that the dV/dt transient was short with respect to other system time constants.

One expects that for a dV_r/dt rating very near to the dV_s/dt rating, then essentially the same collector region dynamics exist for both events. This implies very little CC_{DIFF} charge present at the time of application of the dV_r/dt.

On the other hand, a dV_r/dt rating very much less than the dV_s/dt will not allow the assumption that the dV/dt transient is short with respect to the time constants governing removal of charge from the gate-cathode region. In such a case, the charge transferred from CC_{DEPL} after the junction, JC is reverse biased very early in the dV/dt transient is expected to have only a moderate influence on the devices ability to sustain the dV_r/dt transient.

Instead one must observe that the total charge associated with CC while the junction is still forward biased, $Q_{CC_{DEPL}}(t_q)$ + $Q_{CC_{DIFF}}(t_q)$, is transferred to the gate-cathode region virtually as an impulse at the start of the dV_r/dt transient. This impulse of charge transfer is expected to substantially influence the devices dV_r/dt behavior.

A scan of manufacturers' literature giving static and reapplied dV/dt ratings reveals a trend in these specifications. Typically, the ratings tend toward two groupings. One, usually associated with inverter SCRs, in which $dV_r/dt \approx dV_s/dt$ and another, usually associated with phase control devices, in which $dV_r/dt \leq (1/5)dV_s/dt$.

Development of a parameter estimation procedure treats one uniform case applicable to all dV_r/dt ratings. Attempts to correlate the dV_r/dt to dV_s/dt ratio have not been successful.

Analytical Determination of τ_C

Analytical analysis of the dVr/dt phenomena is done using charge control concepts as was done for dV_s/dt.

At time t_q, the total charge held in the collector region is given by the following expression.

$$Q_{CC}(t_q) = \frac{CC_{DEPL_0}\left[V_{CC}(0)-\theta\frac{t_q}{\tau_C}\right]}{\left[1-V_{CC}(0)+\theta\frac{t_q}{\tau_C}\right]^{1/2}} + \tau_C \alpha_A I_T e^{-t_q/\tau_C} \quad (8.103)$$

$$V_{CC}(0) = \theta \ln\left\{\frac{\alpha_A I_T}{I_{SC}}\right\}$$

As was done in the static dV/dt case, analysis must treat the marginal case. That is the case for which the device very nearly approaches turn-on, but remains off.

For this case the transient time is given by

$$T_{trans} = \frac{\%V_{DRM}}{dV_r/dt} \quad (8.104)$$

where: $\%V_{DRM}$ = spec sheet value for percent of V_{DRM} to which voltage is reapplied.

The dV_r/dt transient is externally driven, therefore the time for which CC remains forward biased is very short and therefore only a small fraction of the interval, T, given by (8.104). The bulk of the interval T is spent with CC rising in reverse bias towards $V_{CC} = \%V_{DRM}$ as shown in fig. 8.5.

With this in mind, it is seen that the charge described by equation (8.103) is removed from the collector region into the gate-cathode region as a virtual impulse of charge at the initiation of the dV_r/dt transient.

While CC is increasing in reverse bias, an additional amount of charge is displaced from the collector region into the gate-cathode region. That charge is given by a relationship similar to equation (8.36).

$$\Delta Q_{CC}(0>V_{CC}>-\%V_{DRM}) \approx \left| CC_{DEPL_0}[\%V_{DRM}]^{1/2} \right| \qquad (8.105)$$

Therefore, the total charge removed from the collector is the sum of equations (8.103) plus (8.105).

Since the analysis is for the marginal off case and due to the non-linearities of the charge transfer causing the bulk of charge transfer to occur early in the transient, then charge loss from the gate-cathode region during this period may be treated in a manner similar to that used for static dV/dt analysis.

V_{CK} is assumed to very nearly approach .75V early in the dV_s/dt transient and to remain very near but less than that value throughout the transient.

RK is the only path for loss of charge from the gate-cathode region represented by CK. This loss has upper boundary value

$$Q_{loss\text{-}RK} = (.75V)T/RK$$
$$= \frac{.75V}{RK}\left(\frac{\%V_{DRM}}{(dV_r/dt)}\right) . \tag{8.106}$$

The nominal charge stored in CK has an upper bound value of

$$Q_{stored\text{-}CK} = (.75V)CK \quad . \tag{8.107}$$

Combining the charge expressions of (8.103), (8.105), (8.106) and (8.107) algebraically provides a charge balance expression.

$$Q_{CC}(t_q) + \Delta Q_{CC}(0>V_{CC}>-\%V_{DRM}) = Q_{loss\text{-}RK} + Q_{stored\text{-}CK} \tag{8.108}$$

It is convenient to note that the contribution of the charge due to the forward biasing of CC_{DEPL} at t_q is sufficiently small relative to other terms to justify its omission in order to simplify math.

Arranging terms of (8.108) to express the contribution of $Q_{CC_{DIFF}}$ as a sum of the other charge terms gives and dividing by $\alpha_A I_T$ gives

$$\tau_C e^{-t_q/\tau_C} = \frac{1}{\alpha_A I_T}\left[\frac{(.75V)\%V_{DRM}}{RK(dV_r/dt)} + (.75)CK - \left|CC_{DEPL_0}[\%V_{DRM}]^{1/2}\right|\right] \tag{8.109}$$

The equation (8.109) must be solved for τ_C, the collector region time constant. This is easily done by trial and error after calculating the right hand side of (8.109) using spec sheet parameter values.

In order to facilitate solution of equation (8.109), a family of curves has been developed in figure (8.21). Use of the curve is demonstrated in the following example and on the graph.

Example

For the GE C602 LM SCR

$$\frac{dV_s}{dt} = 500V/\mu s >> \frac{dV_r}{dt} = \frac{25V}{\mu s}$$

Calculate the right-hand side of Equation (8.109) using spec sheet values to obtain

$$\tau_C e^{-t_q/\tau_C} = 1.55 \times 10^{-8}$$

Locate this value on the horizontal axis of fig. 8.21 and move up to locate the curve corresponding to spec sheet t_q (i.e. 125 μs in this example).

Locate τ_C on the left vertical axis labeled carrier lifetime. For the GE C602 LM, the carrier lifetime is

$$\tau_C = 17.7 \text{ μs} \quad .$$

This estimate of τ_C may be checked as follows.

Using equations (8.102) and (8.97) to obtain $V_{CC}(t_q)$, then the GE C602 has

$$V_{CC}(t_q) = V_{CC}(0) - \frac{\theta}{\tau_C} t_q$$

$$= .668 \text{ V}$$

which certainly satisfies the requirement of $V_{CC}(t_q) > .5V$ for dominate CC_{DIFF}.

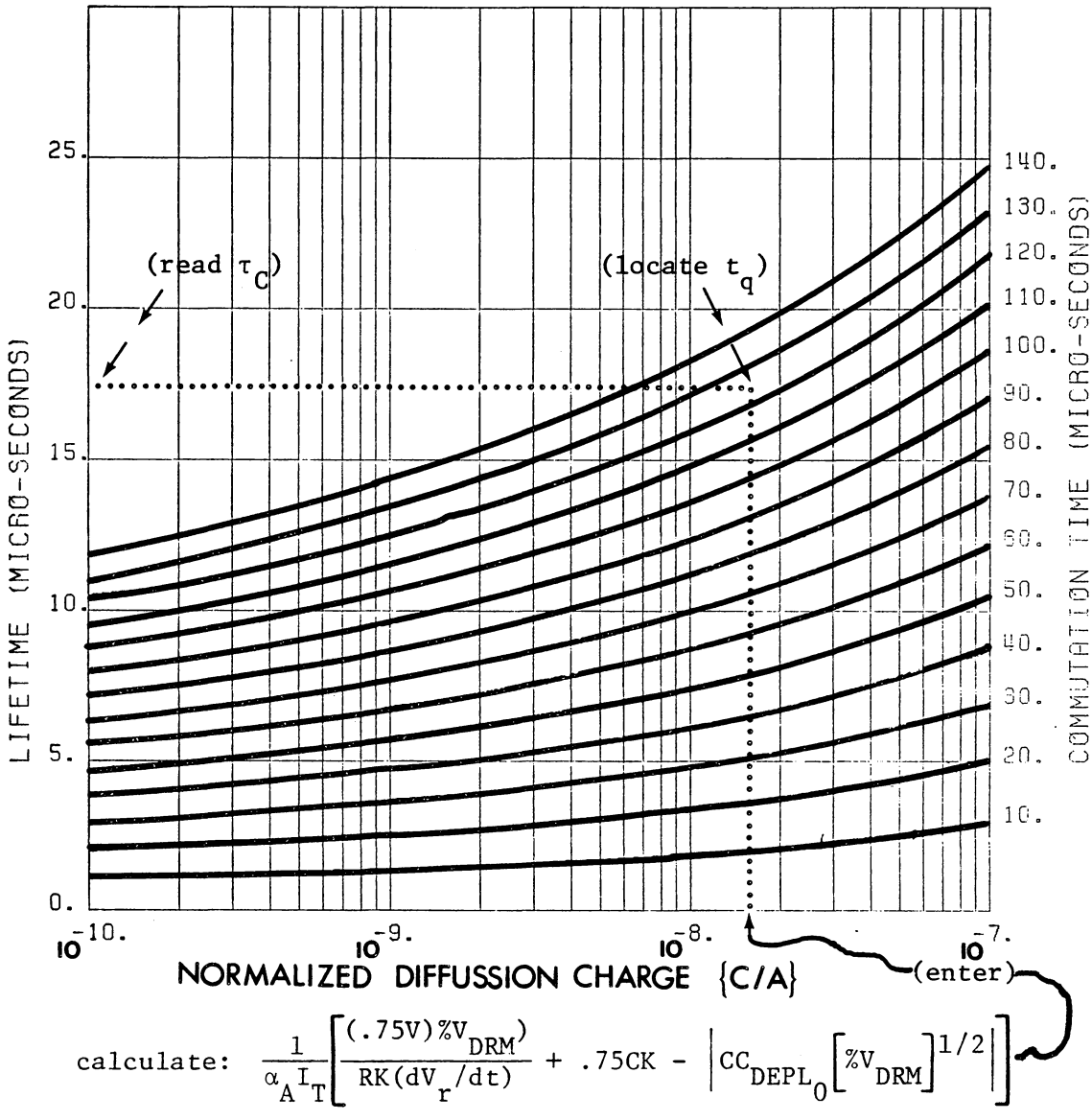


Fig. 8.21. Graph of Solutions to Equation (8.109) to Obtain τ_C.

With this τ_C, an impulse of charge

$$Q_{CC_{DIFF}} = \tau_C JC(t_q)$$

$$= (17.7\ \mu s)(2.08 \times 10^{-12}) e^{.668/.026}$$

$$= 5.30\ \mu C$$

is injected into CK at the start of the dV_r/dt transient.

A charge of this magnitude injected into CK is sufficient to raise the voltage on CK to

$$V_{CK} = 1.62\ V \quad .$$

This would, of course, result in immediate turn-on.

Things are not so bad as they may at first appear, however. A similar calculation as has just been preformed but with t_q set equal to 132 μs will predict $V_{CK} = .75$ with $\tau_C = 17.7$ μs.

One might simply adjust τ_C to a smaller value, say, $\tau_C \approx 17.0$ μs and obtain a prediction of $V_{CK} \approx .75$ V at $t_q = 125$ μs. In order that the model be conservative in this respect, the value $\tau_C = 17.7$ μs is used here.

8.7 Failure Mode Parameters

Two paremeters, the peak forward blocking voltage, and the peak reverse blocking voltage remain to determine.

Determination of these parameters is straight forward. They are read off the spec sheet.

In the J^3 model, the peak forward blocking voltage is the breakdown voltage of JC.

$$BV_{JC} = V_{DRM} \tag{8.110}$$

The peak reverse blocking voltage is the breakdown voltage of JA.

$$BV_{JA} = V_{RRM} \ (V_{DRM} \text{ if } V_{RRM} \text{ not given}) \tag{8.111}$$

Development of parameters for the J^3 SCR is now complete. The following sections provide verification and testing of the model.

8.8 Verification and Testing of the J^3 SCR model

Verification of the J^3 SCR model is done by preforming computer simulation of two SCR types. One phase control SCR, the GE C602 SCR and one inverter SCR, the GE C185 are simulated.

The choice of these two devices for model verification is based on their representing two widely differing SCR types in terms of construction, commutation time, etc.

Verification testing of the model is primarily the process of performing three basic dynamic performance characterization tests, gate driven turn-on, static dV/dt, and commutation using spec sheet data. The non-dynamic preformances are given cursory examination merely to verify proper model functioning. Models for the two chosen SCR specimens are formulated using the J^3 SCR modeling procedure and tested in characterization test circuits via computer simulation using SPICE2 and SCEPTRE.

Dynamic test results are evaluated on the accuracy to which computer simulation conforms to physical device behavior as indicated by spec sheet values.

A sample of a cursory examination of the non-dynamic preformances for the GE C185N is included in the data to illustrate the test procedure.

8.8.1 Summary of the J^3 SCR Model Formulation Technique

Formulation of the J^3 SCR model is essentially a three-step process.

The first step is to obtain from manufacturer's literature of the device to be modeled the specifications listed in figure 8.22. In the event that one merely wants to formulate a generalized model to do non-critical circuit simulation, figure 8.22 provides a list of suggested default values to service as arguments in the parameter estimation equations of figure 8.23.

The second step is to calculate the required J^3 model parameters as outlined in figure 8.23. Solution for all of the parameters is straight forward with the exception of estimation of the collector lifetime constant, τ_C. The indicated transcendental equation must be solved by trial and error. This is a very easy operation with a simple engineering-oriented pocket calculator. A set of curves is provided in figure 8.21 to aid this process.

The third step is to enter the parameters estimated in step two into the applicable input statement listing for SPICE2 and/or SCEPTRE illustrated in figure 8.24 (a) and (b) respectively.

It is suggested that the results of step three be experimentally verified using the test circuit input listings illustrated in the next section. The test circuit input listings must of course be modified to conform to the applicable test requirements of the device under consideration. Notes in the manufacturer's spec sheets are usually a good source of applicable test parameters.

SPEC SHEET QUANTITY	DEFAULT VALUES
$V_T(I_{TM})$, $V_T(.1I_{TM})$, $.9I_{TM}$ — read from on-state V_{AK} vs I_{AK} curve	Use R = .005
I_{GT}	75 ma
I_H	100 ma
V_H	Use minimum voltage given on V_{AK} vs I_{AK} curve (or 1.0V)
RG	10 ohms
t_d	1.0μs
V_G	20V
dV/dt (static - dV_s/dt) or τ	500V/μs (τ depends on V_{DRM})
V_{DRM}	1000V or 2500V
dV/dt (reapplied at t_q)	Phase control 25V/μs Inverter 200V/μs
t_q	Phase control 100μs Inverter 20μs
I_T before start of turn-off	250 Amps.
$\%V_{DRM}$ reapplied	500V or 1250V
V_{RRM}	Omit
V_{GRM}	1.0V

Fig. 8.22. Spec Sheet Data Required to Formulate the J^3 SCR Model

Resistors

$RA = 10^5$ ohms

$RC = 10^{10}$ ohms

$R = [V_T(I_{TM}) - V_T(.1I_{TM})]/.9I_{TM}$ ohms

$RK = .75V/I_{GT}$ ohms $\quad \Delta\ I_{GT} \leq .95\, I_H$

Transport Factors

$\alpha_K = 1.0$

$$\alpha_A = \begin{cases} (I_{GT} + .01\text{ ma})/I_H & \text{for } I_{GT} \leq .95\, I_H \\ .95 & \text{for } I_{GT} > .95\, I_H \end{cases}$$

Optional Amplifying Gate Elements

$I_{SDAG} \approx 3.0 \times 10^{-14}$ amps. with $\theta = .026V$

$$RAG = \begin{cases} 1.5V/(I_{GT} - .95I_H) & \text{if } I_{GT} > I_H \\ \infty & \text{if } I_{GT} < I_H \end{cases} \text{ ohms}$$

$CAG \leq .1 \times CK$

Reverse Saturation Currents

$I_{SA} = I_H e^{-.75V/\theta_A} = I_{SDA1}$ (SPICE2)

$I_{SC} = 1.0 \times 10^{-5} e^{(V_H - 1.5V)/\theta_C}$

$I_{SK} = |I_H - I_{GT}| e^{-.75V/\theta_K}$

units = amps
I_{GT}, I_H amps
$I_{GT} \leq .95 I_H$

Thermal Voltages

$\theta_A = \theta_C = \theta_K = .026V$ @ T = 25°C = 300°K

These are SPICE2 Default Values

Invert to 1/θ for SCEPTRE

Linear Capacitor

Amplifying Gate: $$CK = \left| \frac{(1/RK + 1/RAG + 1/RG)t_d}{\ln(1 - .75/V_{CK}^{\infty})} \right| \text{ F.}$$

Where: $$V_{CK}^{\infty} = \{VG - .75\,(1 + \frac{RG}{RAG})\}/(1 + \frac{RG}{RAG} + \frac{RG}{RK})$$

Non-amplifying Gate: $$CK = \frac{-.8\, t_d}{\frac{RG\ RK}{RG+RK} \ln\left(1 - \frac{.78}{VG}\frac{(RG+RK)}{RK}\right)} \text{ F.}$$

Depletion Layer Zero-Bias Capacitance

$$CC_{DEPL_0} = .45 \left| \frac{.75\ CK}{[V_{DRM}]^{1/2}} + \frac{3.16[V_{DRM}]^{1/2} I_{GT}}{dV_s/dt} \right| \text{ F.}$$

where $I_{GT} \leq .95\, I_H$

$CA_{DEPL_0} \geq CK$

Diffusion Capacitance Lifetime Constants

$$\tau_C e^{-t_q/\tau_C} = \frac{1}{\alpha_A I_T}\left[\frac{(.75V)\%V_{DRM}}{RK(dV_r/dt)} + (.75)CK - \left|CC_{DEPL_0}[\%V_{DRM}]^{1/2}\right|\right] \text{ S.}$$

(solve using figure 8.21)

$$\tau_A = (\theta R_G/(V_G - .75))\left\{CA_{DEPL_0}/(.25 - \theta \ln\left(\frac{V_G - .75V}{\alpha_A R_G I_H}\right))^{1/2}\right\} \text{ S.}$$

Junction Reverse Break-down Voltages

$BV_{JA} = V_{RRM}$ (V_{DRM} if V_{RRM} not given)

$BV_{JC} = V_{DRM}$

$BV_{JK} = V_{GRM}$ (spec. sheet) or 5V [11, p. 67] or 1.V for very short t_q devices.

Fig. 8.23. Summary of the J^3 SCR Model Parameter Estimation Procedure

```
.SUBCKT  "NAME"  1  2  3

R  1  4  [R]
RA  4  5  [1.E5]
RC  5  9  [1.E10]
RK  9  3  [RK]

*  *  *  Current Sensors  *  *  *
DA1  4  6  DA1  IC = OFF
.MODEL  DA1  D(IC = [I_SA])
EA  4  8  4  5  1.
VA  6  8  0.
VK  7  3  0.
* - - - - - - - - - - - - - - - - -

DA  4  5  DA  IC = OFF
DC  9  5  DC
FC  5  9  POLY(2)  VA  VK  0.  [α_A]  [α_K]
DK  9  7  DK  IC = OFF
CK  9  3  [CK]

*  *  *  Amplifying Gate  *  *  *
DAG  2  9  DAG
RAG  2  3  [RAG]
* - - - - - - - - - - - - - - - - -

.MODEL  DA  D(IS = [I_SA], CJO = [CA_DEPL_0], TT = [τ_A], BV = [BV_JA])

.MODEL  DC  D(IS = [I_SC], CJO = [CC_DEPL_0], TT = [τ_C], BV = [BV_JC])

.MODEL  DK  D(IS = [I_SK],  BV = [BV_JK])

.MODEL  DAG  D(IS = [I_SDAG])

.ENDS
```

(a) Generalized SPICE2 Input Format for the J^3 SCR Model.
[--] = Parameter to Be Determined

Note: Without amplifying gate elements, node 9 = node 2

Fig. 8.24. Generalized Input Listings for SPICE2 and SCEPTRE Formulations of the J^3 SCR Model

```
MODEL DESCRIPTION
MODEL  "NAME"  (A-G-K)
UNITS:  OHMS, FARADS, HENRIES, SECONDS, AMPS, VOLTS.
* * * *
ELEMENTS
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
R, A-1 = [R]
RA, 1-C = [1.D5]
RC, C-2 = [1.D10]
RK, 2-K = [RK]
RAG, G-K = [RAG]
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
JA, 1-C = DIODE Q(PJA, PTHT)
JC, 2-C = DIODE Q(PJC, PTHT)
JK, 2-K = DIODE Q(PJK, PTHT)
J1, C-2 = X1([αA] * DABS(JA) + [αK] * JK)
JAG, G-2 = DIODE Q([ ISDAG ], PTHT)
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
CA, 1-C = FCJ([τA], [ISA], PTHT, JA, VCA, [CADEPL0], [CMIN])

CC, 2-C = FCJ([τC], [ISC], PTHT, JC, VCC, [CCDEPL0], [CMIN])

CK, 2-K = [CK]

CAG, G-2 = [CAG]
* * * * * * * * *
DEFINED PARAMETERS
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
PJA = FIS([ISA], VCA, [BVJA])

PJC = FIS([ISC], VCC, [BVJC])

PJK = FIS([ISK], VCK, [BVJK])

PTHT = [1/θ]
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

(b) Generalized SCEPTRE Input Format for the J^3 SCR Model.
[--] = Parameter to Be Determined

Note: With amplifying gate, node 2 = node G

If a test does not yield the desired results, then following a check on calculated values, model parameter adjustments should be made. It has been found that a five to ten percent adjustment usually provides adequate adjustment. A larger adjustment of as much as 20% is not considered extreme, however.

Suggested adjustments to parameters are as follows: t_d - adj. CK; t_r - adj. CA_{DEPL_0}; dV/dt - adj. CC_{DEPL_0}; t_q - adj. τ_C; Reverse recovery charge - adj. τ_A.

8.8.2 J^3 Model SPICE2 Verification Tests and Results

SPICE2 GE C602 LM and GE C185N SCR dynamic test circuit input listings are shown in fig. 8.25 (a) thru (f). SPICE2 subckts containing the model input listings for these two SCRs are given in fig. 8.25 (g) and (h).

Dynamic verification test results are shown for SPICE2 in fig. 8.26. Results are presented in the order turn-on test, static dV/dt test, and turn-off test for the GE C602 LM followed by the GE C185N.

Turn-on test results (fig. 8.26 (a) and (f)) have clear t_d and t_r features conforming very well to specifications. A slight over shoot in I_{AK} is unexplained behavior.

Static dV/dt testing is shown in fig. 8.26 (b), (c), (g) and (h). GE C602 results show the ability to withstand exponentially applied dV/dt rated at 500V/μs whereas 600V/μs results in device turn-on. The GE C185 results differ somewhat. The C185 properly remained off at its rating of 500V/μs. It also remained off when tested at 600V/μs, but turned on at 750V/μs. Since manufacturer's literature provides dV/dt for which the device is assured to remain off, but does not provide the exact point of turn-on, the test results are considered positive.

It is important to note that the parameter prediction procedure is based on charge control analysis and as such is primarily useful to produce close estimates for parameters and not exact calculation. Although, as the above results indicate, the prediction is quite good, some "fine turning" of parameters should be performed if dV/dt simulation is critical.

Commutation test results are shown for the C602 SCR in figure 8.26 (d) and (e) and for the C185 SCR in figure 8.26 (i) and (f). The first test point for each devices shows that the device failed to commutate at rated t_q and rated reapplied dV/dt.

Such behavior was predicted in analytical development of the formulation procedure in section 8.6.2.2. A correction for this behavior was not included in the parameter estimation procedure so that the procedure would be conservative in this respect.

As is noted in the commutation test results for both devices, successful commutation was observed to occur within a few microseconds beyond rated t_q. The exact point of commutation was not determined since it would provide no significant additional data.

(a)

```
GEC602LM TURN-ON TEST

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************



VS 0 1 -900.
RL 1 2 45.
X1 2 3 0 GEC602LM
RG 4 3 10.
VG 4 0 PULSE(0. 20. 1.US .1US .1US 20.US 50.US)
.TRAN .1US 10.US
.PLOT TRAN I(VS) I(VG) V(2,0) V(3,0)
.OPTIONS NOMOD LIST
```

(b)

```
GEC602LM DV/DT TEST

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************



VS1 1 0 EXP(0.,2700.,.1US,3.34US,17.5US,.1US)
VZ 1 2 0.
RL 2 3 270.
X1 3 4 0 GEC602LM
RG 0 4 1.E6
.TRAN 1.US 20.US
.PLOT TRAN I(VZ) V(4,0) V(3,0) V(1,0)
.OPTIONS NOMOD LIST
```

(c)

```
GEC602LM TURN-OFF TEST

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************



VS1 1 0 PULSE(1350.,-75.,75.US,.1US,57.US,125.US,300.US)
VZ 1 2 0.
RL 2 3 3.
X1 3 5 0 GEC602LM
**** CAUTION OVERDRIVING THE GATE CIRCUIT MAY CAUSE NUMERICAL PROBLEMS ***
VG 6 0 PULSE(0.,3.0,.1US,.1US,.1US,20.US,300.US)
RG 6 4 1.
DG 4 5 D OFF
.MODEL D D(IS=1E-8)
.TRAN 5.US 300.US 70.US
.PLOT TRAN I(VZ) V(4,0) V(3,0) V(1,0)
.OPTIONS NOMOD LIST
```

Fig. 8.25. SPICE2 Input Listings for Dynamic Tests of J^3 SCR Models

(d)

```
GEC185N TURN-ON TEST

     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


VS 1 0 800.
VZ 1 2 0.
RL 2 3 16.
X1 3 4 0 GEC185N
RG 5 4 20.
VG 5 0 PULSE(0. 20. .1US .1US .1US 20.US 50.US)
.TRAN .1US 5.US
.PLOT TRAN I(VZ) I(VG) V(2,0) V(3,0)
.OPTIONS NOMOD LIST LIMPTS=400 ACCT
```

(e)

```
GEC185N DV/DT TEST

     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


VS1 1 0 EXP(0.,800.,.1US,1.01US,8.US,.1US)
VZ 1 2 0.
RL 2 3 80.
X1 3 4 0 GEC185N
RG 0 4 1.E6
.TRAN .5US 10.US
.PLOT TRAN I(VZ) V(4,0) V(3,0) V(1,0)
.OPTIONS NOMOD LIST LIMPTS=400 ACCT
```

(f)

```
GEC185N TURN-OFF TEST

     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


VS1 1 0 PWL(0US 800. 50US 800. 71.25US -50. 91.25US 0. 95.25US 800. 100US 800.)
VZ 1 2 0.
RL 2 3 3.2
X1 3 4 0 GEC185N
VG 5 0 PULSE(0. 20. .1US .1US .1US 20.US 300.US)
RG 5 4 20.
.TRAN 2.US 110.US 46.US
.PLOT TRAN I(VZ) V(4,0) V(3,0) V(1,0)
.OPTIONS LIST LIMPTS=400 ACCT
```

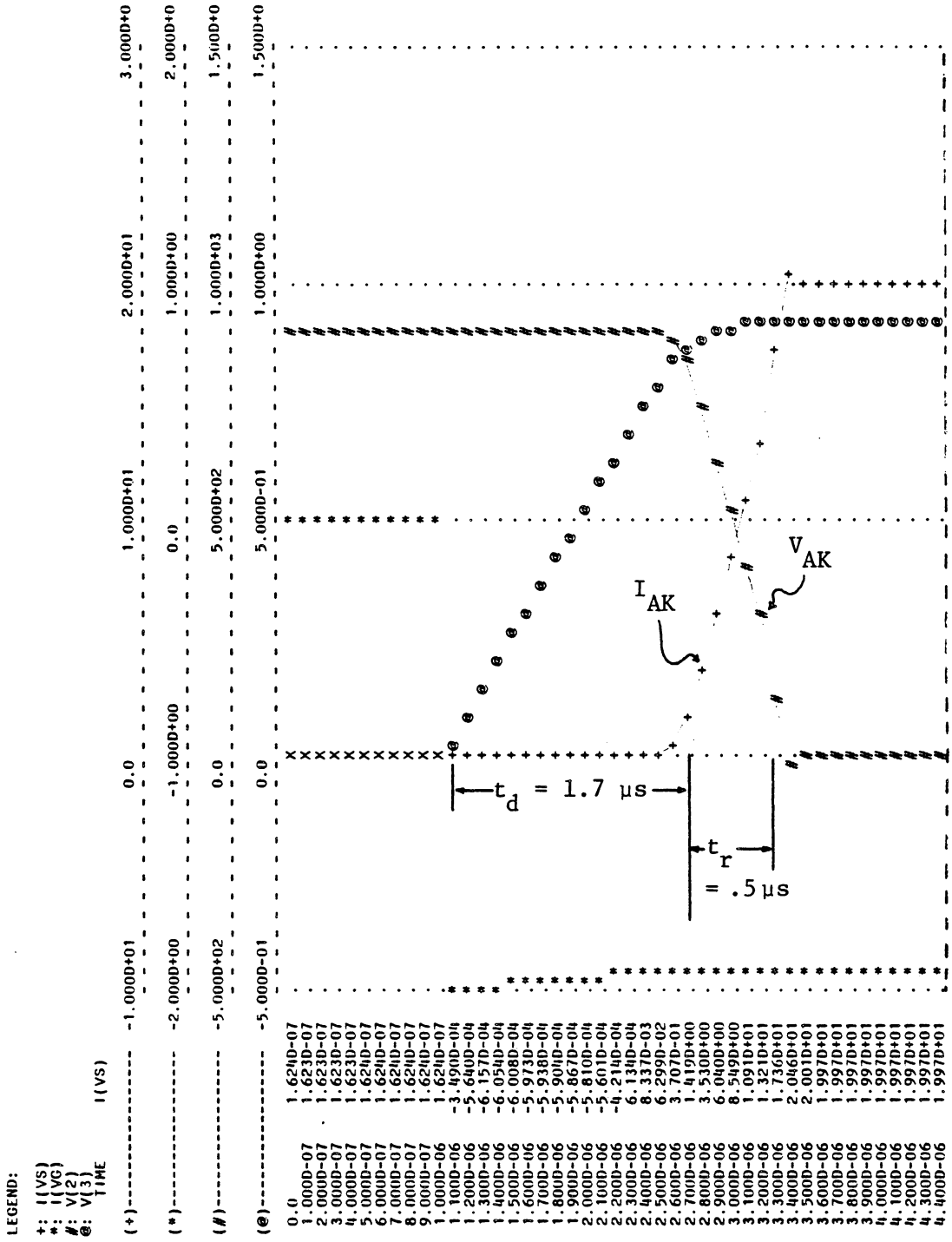
(g)

```
.SUBCKT GEC602LM 1 2 3
R 1 4 .0005
RA 4 5 1.E5
RC 5 2 1.E10
RK 2 3 9.375
DA 4 5 DA IC=OFF
*-------------------------------------------------------------------------------
*DA1,EA,&VA ARE USED TO SENSE DA CURRENT *** VK IS USED TO SENSE DK CURRENT.
DA1 4 6 DA1 IC=OFF
.MODEL DA1 D(IS=2.967E-14)
EA 4 8 4 5 1.
VA 6 8 0.
VK 7 3 0.
*-------------------------------------------------------------------------------
DC 2 5 DC
FC 5 2 POLY(2) VA VK 0.0 .8 1.0
DK 2 7 DK IC=OFF
CK 2 3 3.54UF
.MODEL DA D(IS=2.967E-14,CJO=3.54E-6,TT=1.06E-7,BV=2700.)
.MODEL DC D(IS=2.082E-12,CJO=3.27E-8,TT=17.7E-6,BV=2700.)
.MODEL DK D(IS=5.933E-15,BV=5.)
.ENDS
```

****

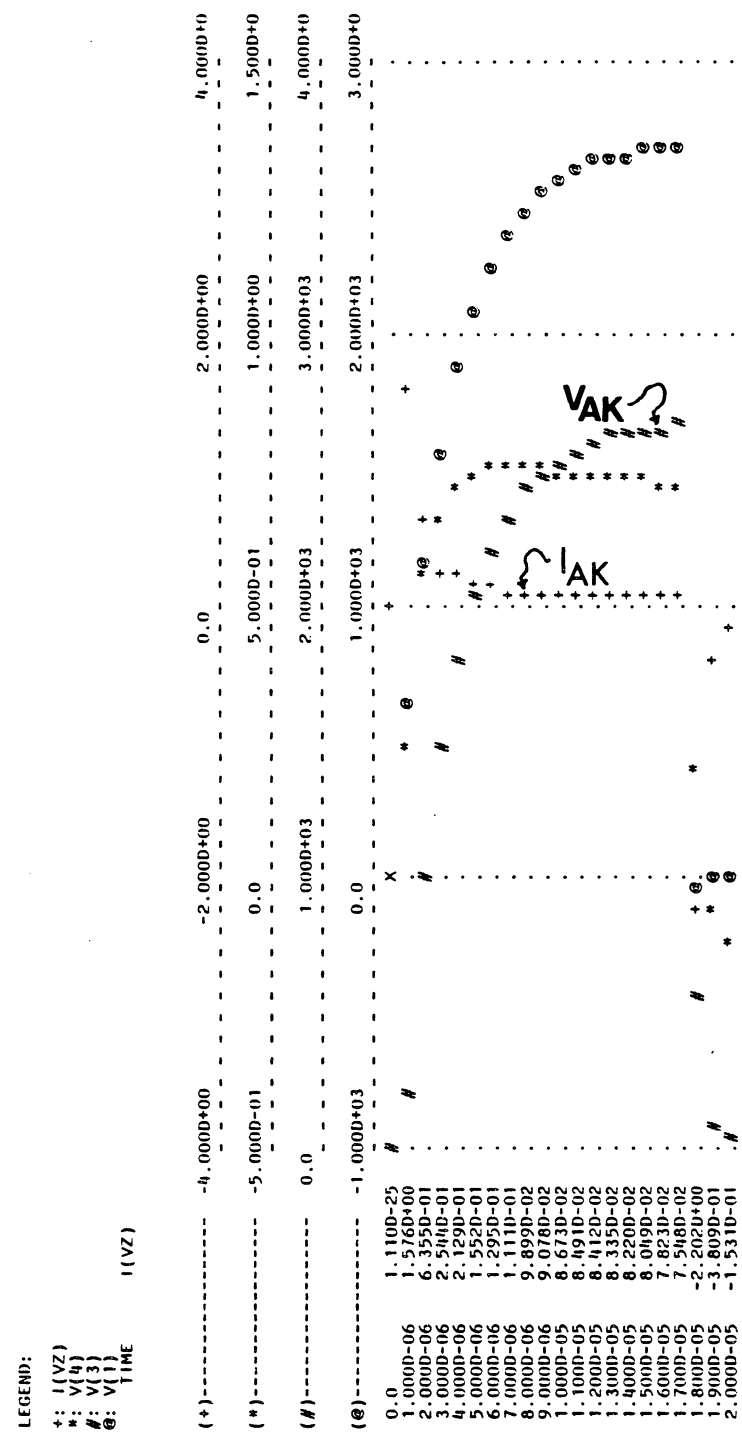
(h)

```
.SUBCKT GEC185N 1 2 3
R 1 4 .0008
RA 4 5 1.E5
RC 5 9 1.E10
RK 9 3 10.53
DA 4 5 DA IC=OFF
*-------------------------------------------------------------------------------
**DA1,EA,&VA ARE USED TO SENSE DA CURRENT *** VK IS USED TO SENSE DK CURRENT**
DA1 4 6 DA1 IC=OFF
.MODEL DA1 D(IS=2.22E-14)
EA 4 8 4 5 1.
VA 6 8 0.
VK 7 3 0.
*-------------------------------------------------------------------------------
DC 9 5 DC
FC 5 9 POLY(2) VA VK 0.0 .95 1.0
DK 9 7 DK IC=OFF
CK 9 3 1.14UF
*-------------------------------------------------------------------------------
**RAG & DAG ARE OPTIONAL AMPLIFYING GATE ELEMENTS**
DAG 2 9 DAG
RAG 2 3 27.91
*-------------------------------------------------------------------------------
.MODEL DA D(IS=2.22E-14,CJO=1.14E-6,TT=7.2E-8,BV=970.)
.MODEL DC D(IS=4.336E-19,CJO=1.93E-8,TT=2.1US,BV=808.)
.MODEL DK D(IS=1.11E-15,BV=1.0)
.MODEL DAG D(IS=2.11E-14)
.ENDS
```

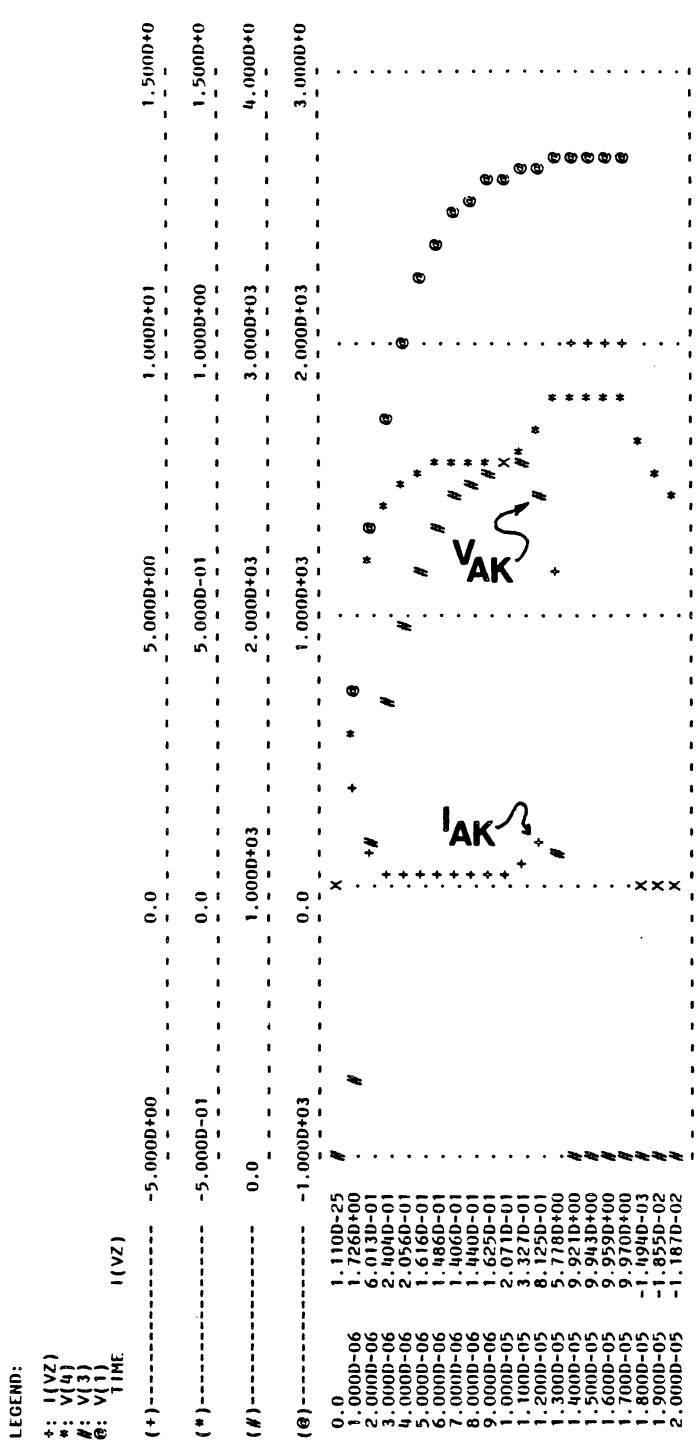


(a) GE C602 LM Turn-on Transient

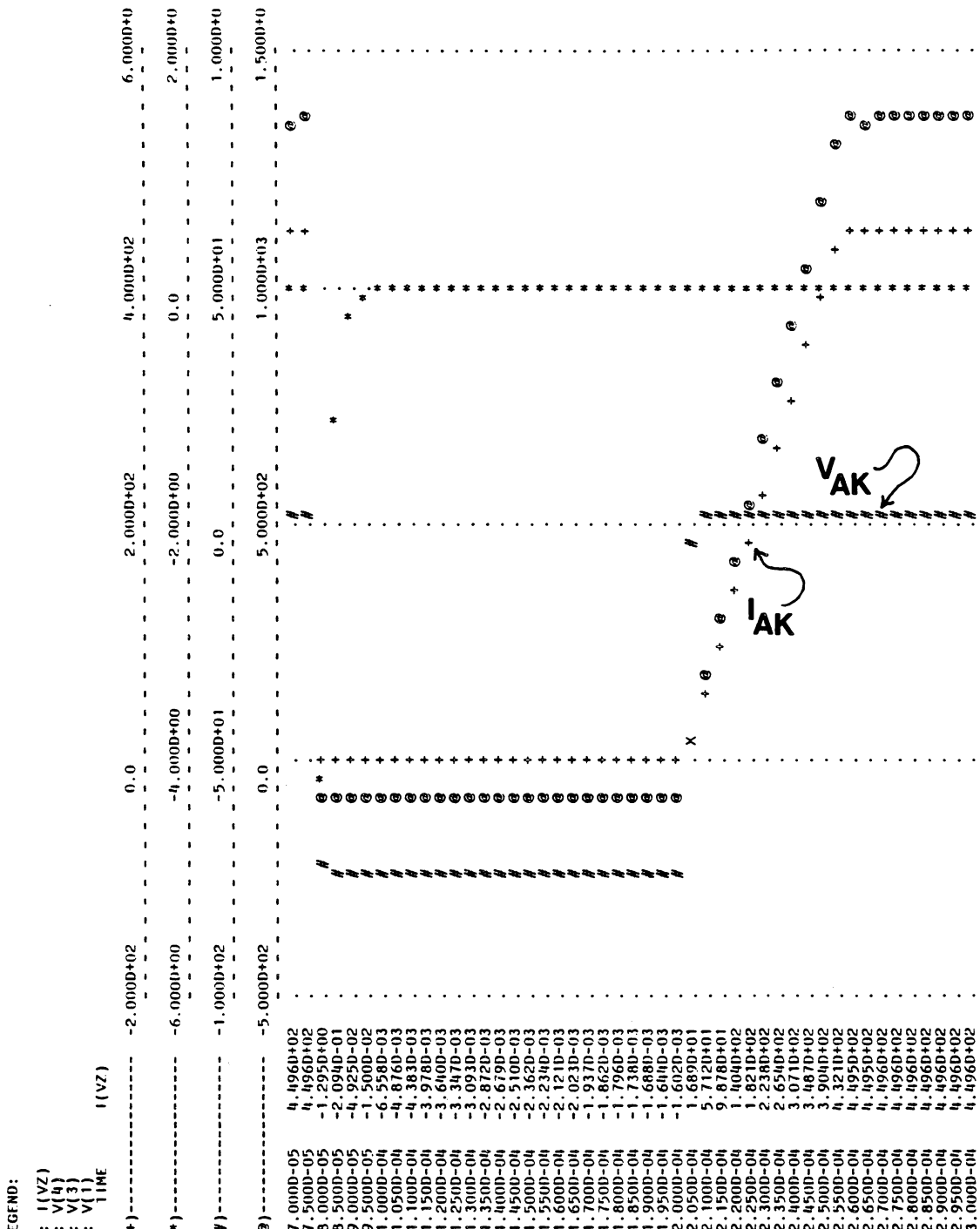
Fig. 8.26. SPICE2 J3 SCR Model Dynamic Performance Verification Waveforms



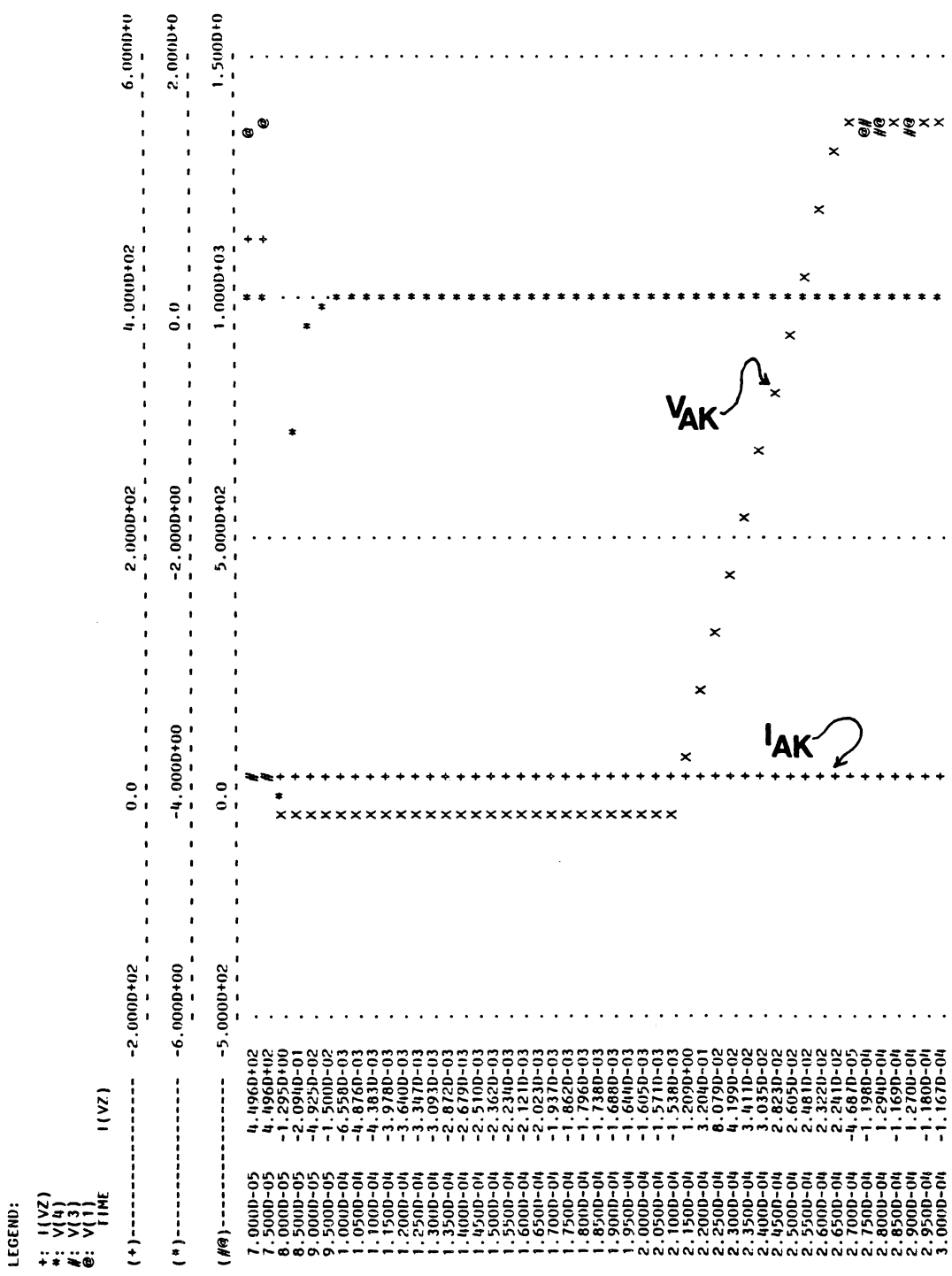
(b) GE C602 LM DV/DT Test at 500V/μs (Passed)



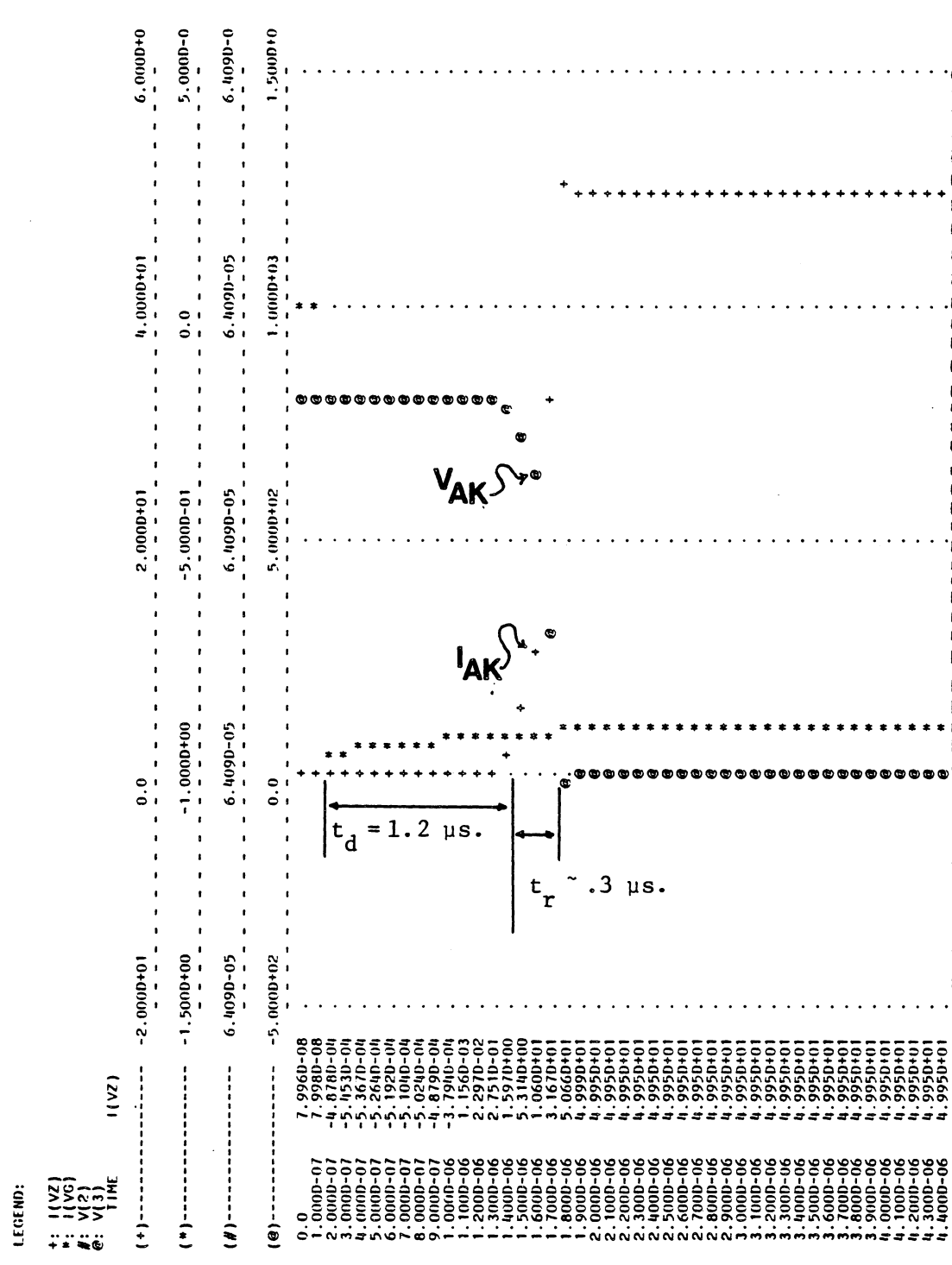
(c) GE C602 LM DV/DT Test at 600 V/μs (Failed)



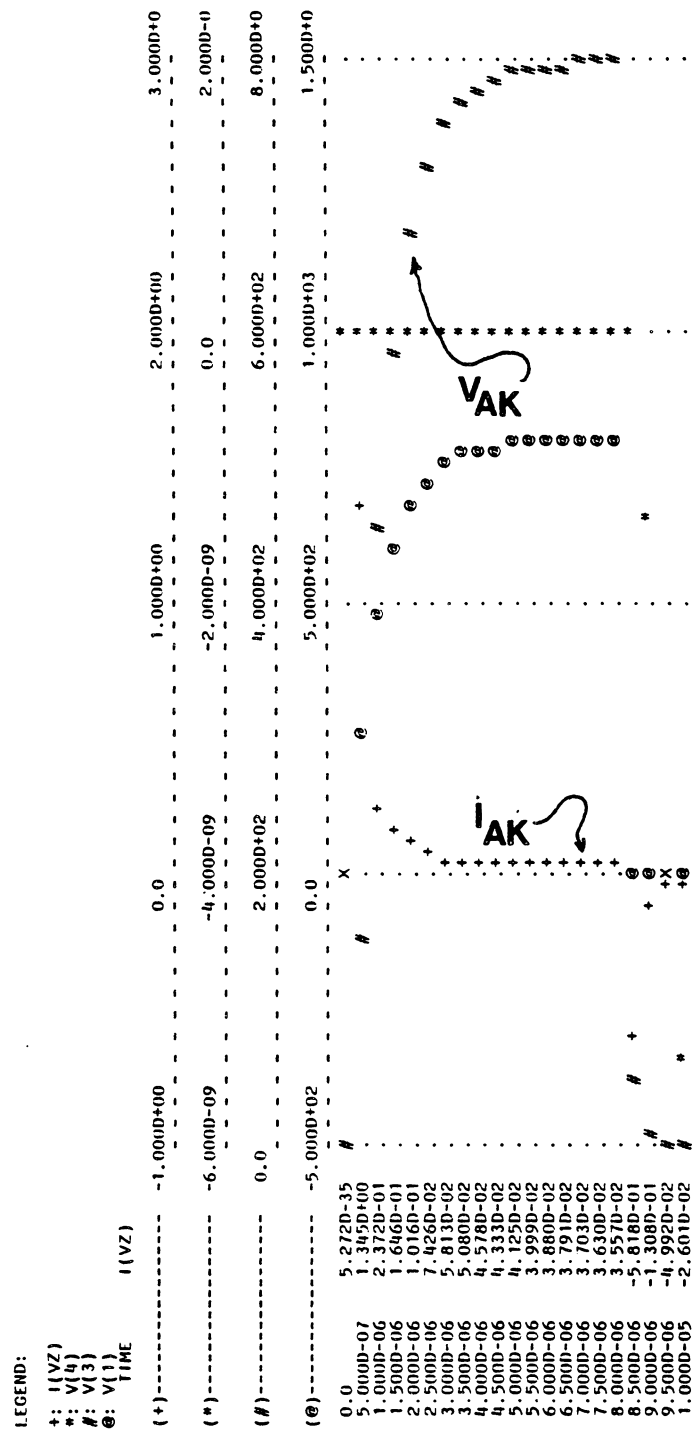
(d) GE C602 LM Commutation Test at dV_r/dt = 25V/μs
Reapplied at 125 μs. (Unsuccessful)



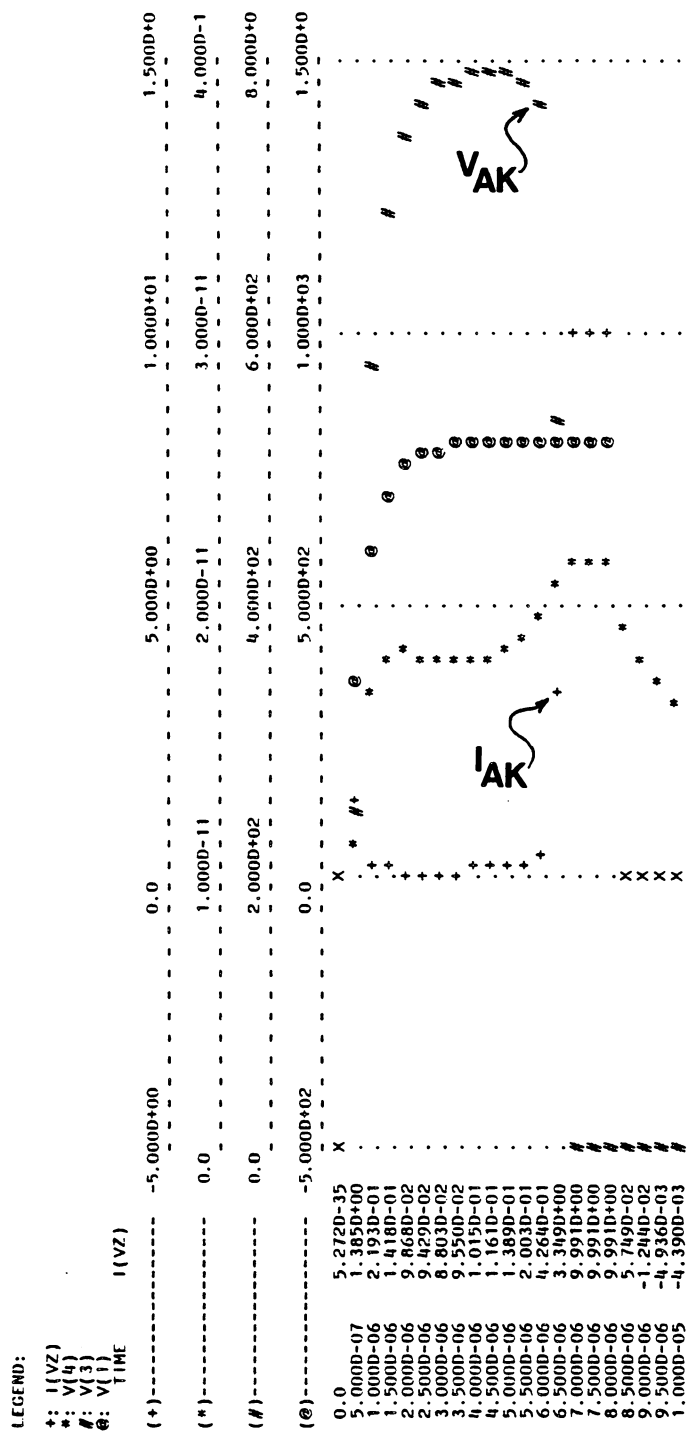
(e) GE C602 LM Commutation Test at dV_r/dt = 25V/μs Reapplied at 135 μs. (Successful)



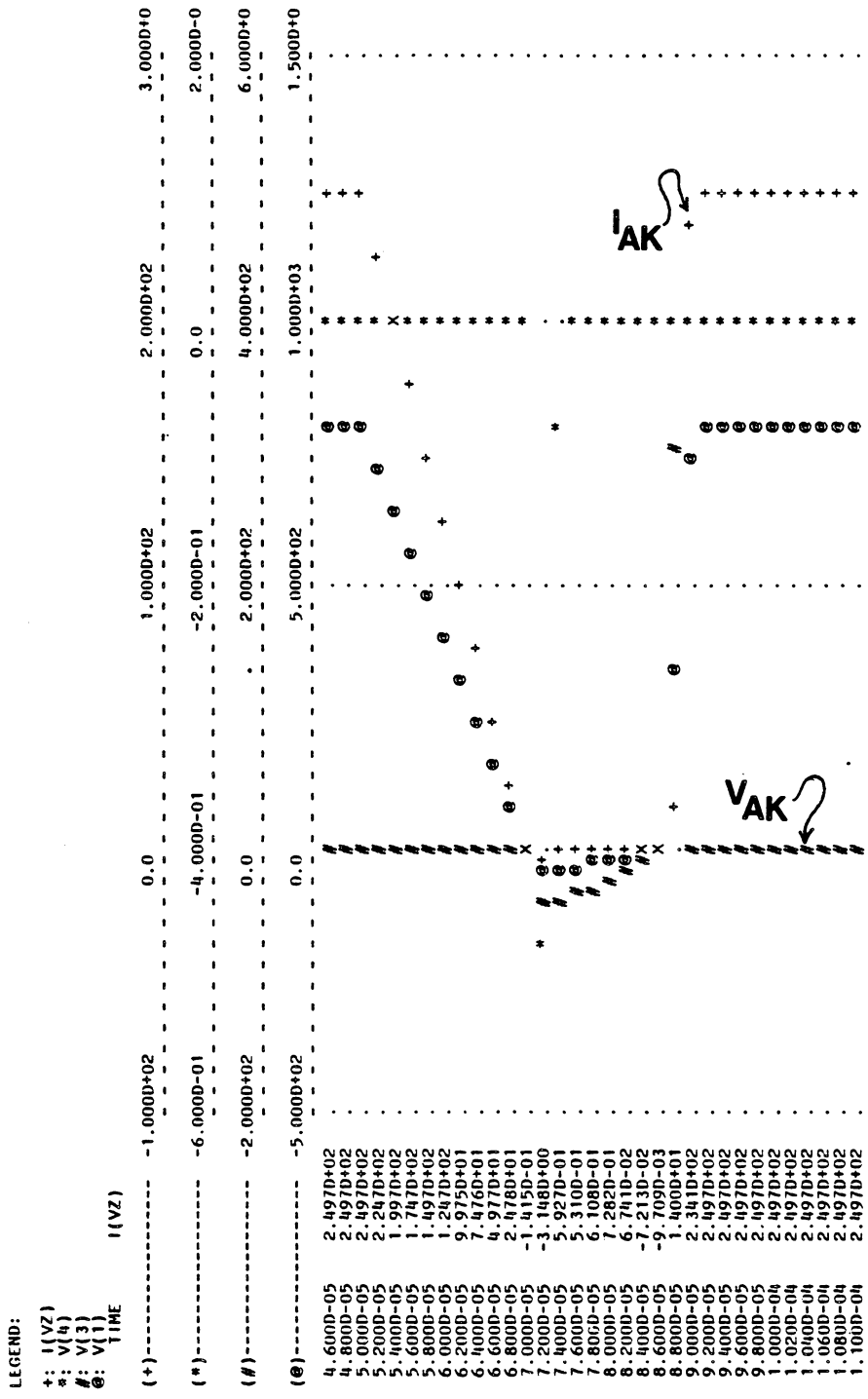
(f) GE C185N Turn-on Transient



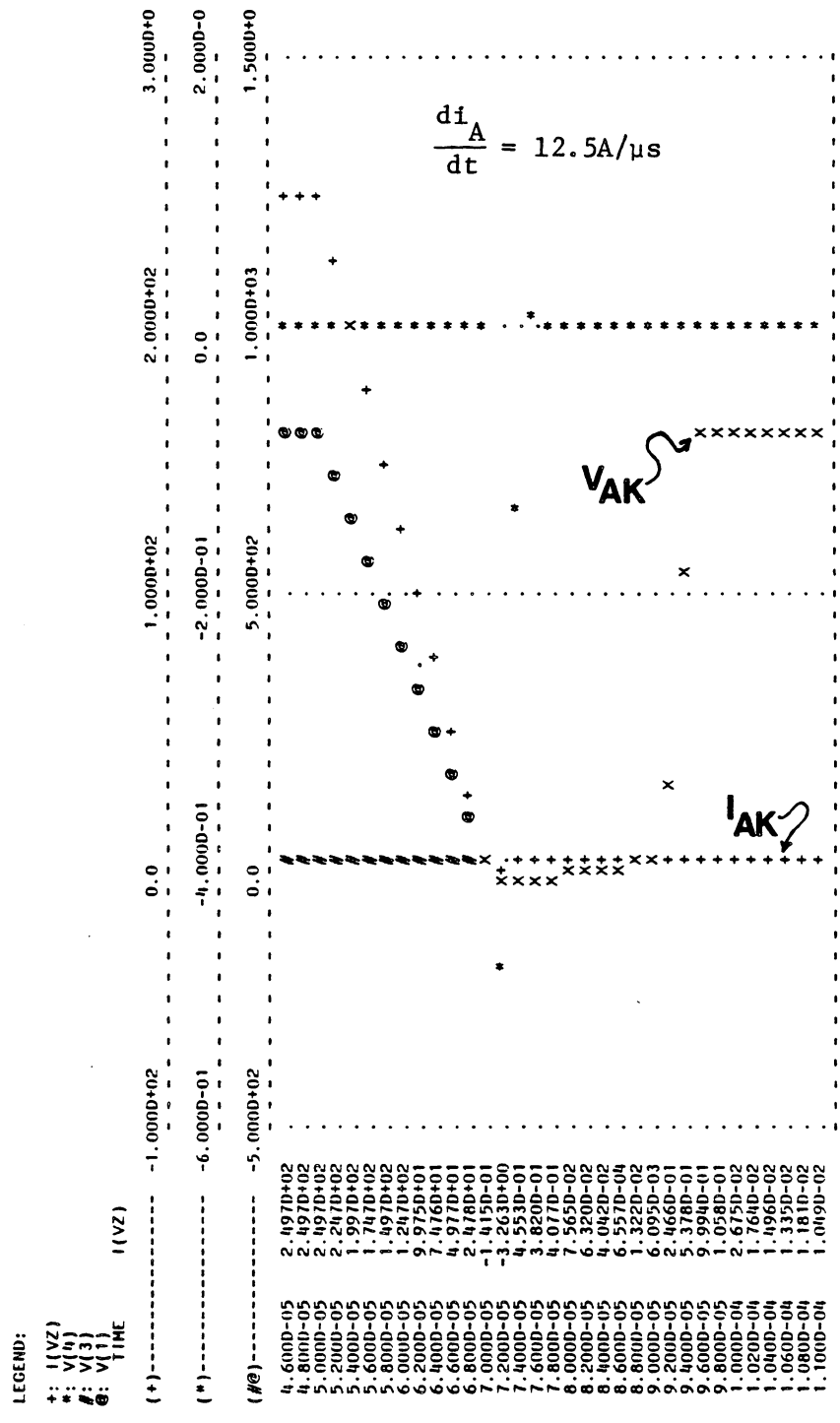
(g) GE C185N DV/DT Test at 500 V/µs. (Passed)



(h) GE C185N DV/DT Test at 750 V/μs. (Failed)



(i) GE 185N Commutation Test at DV_r/DT = 200V/μs
Reapplied at 15 μs. (Unsuccessful)



(j) GE C185N Commutation Test at DV_r/DT = 200V/μs Reapplied at 20 μs. (Successful)

The following observations are considered relevant data pertaining to commutation characteristics:

BV_{JK} - the use of a linear CK may result in a long time constant for removal of reverse charge on CK due to the turn-off transient. Short t_q devices should have a low BV_{JK} value used to insure good commutation performance. A value of 1V. has proven adequate. Since short t_q devices tend to be amplifying gate devices, this poses no inaccuracy in reverse gate voltage limitations. The intuitive choice of 0.V for BV_{JK} is not appropriate to SPICE2 which interprets this latter choice as having no BV_{JK} at all (i.e. ∞).

$-V_{AK}$ - the magnitude of $-V_{AK}$ and the recent time history of $-V_{AK}$ at the time of reapplied dV/dt is observed to affect the commutation time of the device. The direction of influence is consistent with the theory of section 8.6.2.1 [22, p. 624]. An example in point is the t_q test of the GE C185N as illustrated in figure 8.25 (i). With dV/dt reapplied from zero volts V_{AK} at 15μs, the SCR failed to commutate. Identical test parameters except that dV/dt was reapplied from -40 volts V_{AK} resulted in successful commutation at 15μs. Exact t_q was determined to be 11.5μs under the latter condition of $-V_{AK}$.

$|di_A/dt|$ - t_q is observed to decrease with decreasing $|di_A/dt|$. This is consistent with theory [22, p. 624].

8.8.3 J^3 Model SCEPTRE Verification Tests and Results

Having verified the model performance with SPICE2 in the previous section, then the validation of the parameter estimation procedure is done.

Model verification with SCEPTRE is required therefore not so much to verify the parameter estimation procedure, but to verify the user supplied subroutines and model input listing formulation to be used with SCEPTRE.

A generalized input listing for the SCEPTRE formulation of the J^3 model was given in figure 8.24 (b). The specific formulation for the GE 185N inverter SCR with amplifying gate construction is shown in figure 8.27.

Special subroutines necessary to provide calculation of the non-linear junction capacitances and junction reverse breakdown are shown in figure 8.28. Also shown in figure 8.28 is a pulse generator subroutine useful to provide cyclic pulsed behavior for any generalized SCEPTRE quantity.

Dynamic test simulation results for turn-on, dV/dt, and t_q are shown in figure 8.29 (a) thru (e) for the GE C185N. Additionally non-dynamic performance data is tabulated in figure 8.29 (f).

Turn-on test results in figure 8.29 (a) are essentially like SPICE2 results. A marked difference in results is the absence of the overshoot in anode current which was observed to occur in SPICE2 turn-on simulation data. Again, no explanation has been determined for this effect.

The results of testing the response of dV/dt applied from a static off-state are shown in figure 8.29 (b) and (c). Applying the dV/dt transient exponentially at the C185 rating of 500V/μs produces the manufacturer's specified result that the device remains off.

SCEPTRE and SPICE2 results differ by more than 25%, however, when determining dV/dt which produces device turn-on. The SPICE2 results showed turn-on at 750V/μs whereas SCEPTRE required a transient rating of 1000V/μs to produce turn-on.

Investigation of this inconsistency suggests the leading culprit to be the mathematical formulation used to describe CA_{DEPL}. SPICE2 uses a linear mathematic formulation for computing forward biased values of CA_{DEPL} [4, p. A2.54]. The formulation used in SCEPTRE is the theoretical non-linear mathematical description given by equation (8.2). Use of a linear expression to calculate CA_{DEPL} via subroutine "FCJ" revealed results consistent with SPICE2 following some trial and error with the slope of the linear function.

After some reflection, it was decided to retain the non-linear expression for computing junction depletion layer terms in SCEPTRE and to allow the discrepency in results since it is not excessive.

The C185 commutation simulation with SCEPTRE shown in figure 8.29 (d) and (e) was observed to correspond well with that observed with SPICE2 simulations.

Non-dynamic performance data for SCEPTRE simulation of the C185 is tabulated in figure 8.29 (f). The test data recorded is a result

of selecting an arbitrary operating point in the near vicinity of a critical point and conducting simulation to see if the model behaved in the expected manner. Desirable behavior resulted in all cases as recorded.

One key point was observed in simulating junction breakdown behavior. Substantially better numerical performance is achieved if the SCEPTRE "ABSOLUTE ERROR TOLERANCE" under "RUN CONTROLS" is set to a very close tolerance.

Setting the tolerance to 10^{-6} vs 10^{-3} resulted in a 20 to 1 improvement in the number of time steps required to achieve a breakdown transient simulation.

Explanation of this behavior is suspected to involve the operational technique of the SCEPTRE multiple order GEAR algorithm and automatic time step adjustment applied to the implicit numerical integration routine. It has not been resolved.

```
MODEL DESCRIPTION
MODEL GEC185N(A-G-K)
 THIS IS A SCEPTRE SCR MODEL USING THE J3 SCR MODEL PARAMETER ESTIMATION
PROCEDURE. THE MODEL REQUIRES SPECIAL SUBROUTINES 'FCJ','FIS', AND 'FBD'
TO FUNCTION.
                    * * * * * * * * * * *
** NOTE: IF NOT USING V(BR)R PARAMETER, USE J1,C-2=X1(.95*JA+JK). **
                    * * * * * * * * * * *
UNITS: OHMS, FARADS, HENRIES, SECONDS, AMPS, VOLTS
ELEMENTS
R,A-1=8.D-4
RA,1-C=1.D5
RC,C-2=1.D10
RK,2-K=10.51
RAG,G-K=27.91
JA,1-C=DIODE Q(PJA,PTHT)
JC,2-C=DIODE Q(PJC,PTHT)
JK,2-K=DIODE Q(PJK,PTHT)
J1,C-2=X1(.95*DABS(JA)+JK)
JAG,G-2=DIODE Q(2.11D-14,PTHT)
CA,1-C=FCJ(7.2D-8,2.22D-14,PTHT,JA,VCA,1.14D-6,1.D-9)
CC,2-C=FCJ(2.1D-6,4.34D-19,PTHT,JC,VCC,1.93D-8,5.D-10)
CK,2-K=1.14D-6
CAG,G-2=1.14D-8
DEFINED PARAMETERS
PJA=FIS(2.22D-14,VCA,970.)
PJC=FIS(4.34D-19,VCC,808.)
PJK=FIS(1.11D-15,VCK,1.)
PTHT=38.61
OUTPUTS
VCA,VCC,VCK,PLOT
```

Fig. 8.27. SCEPTRE Model Description for the GE C185N SCR

```
C ********************************************************
C SUBROUTINE FIS IS USED TO SIMULATE JUNCTION BREAKDOWN BY VARYING THE
C SATURATION CURRENT, IS, INPUT TO THE DIODE EQUATION FOR PRIMARY DEPEN-
C DENT CURRENT SOURCES.
      ******* PARAMETERS *******
C     IS=JUNCTION REVERSE SATURATION CURRENT:
C     VJ=CAPACITOR STATE VARIABLE VOLTAGE FOR JUNCTION:
C     VBD=BREAKDOWN VOLTAGE:
C NOTE: SET 'MINIMUM ABSOLUTE ERROR = .00001' FOR BREAKDOWN SIMULATION
C --------------------------------------------------------
      DOUBLE PRECISION FUNCTION FIS(IS,VJ,VBD)
      IMPLICIT REAL*8(A-K,O-Z)
      FIS=IS
      IF(VJ.GE.-VBD) RETURN
      A=100.*(-VBD-VJ)
      IF(A.LE.40.) GO TO 10
      A=40.
   10 FIS=IS*DEXP(A)
      RETURN
      END
C ********************************************************
C SUBROUTINE FCJ CALCULATES THE NON-LINEAR CAPACITANCE ASSOCIATED
C WITH A PN JUNCTION. IF THE JUNCTION IS FORWARD BIASED CAPACITANCE
C HAS DEPLETION AND DIFFUSION TERMS CALCULATED.
C   CONVERSELY IF THE JUNCTION IS REVERSE BIASED ONLY DEPLETION
C CAPACITANCE IS CALCULATED.  REVERSED BIASED JUNCTION CAPACITANCE
C IS LIMITED TO A MINIMUM VALUE, CMIM, TO AVOID UNREASONABLY SMALL
C TIME CONSTANTS IN THE CIRCUIT SIMULATION.
C       ******* PARAMETERS *******
C     TAU=THE EXCESS CARRIER LIFETIME IN THE NEUTRAL REGIONS
C     IS=JUNCTION SATURATION CURRENT
C     THT=EINSTIEN'S CONSTANT (Q/KT=38.61 INVERSE VOLTS @ 300 DEG K.)
C     J=CURRENT SOURCE SIMULATING THE PN JUNCTION FOR WHICH
C       CAPACITANCE IS BEING CALCULATED
C     VC=VOLTAGE ACROSS CAPACITOR WHOSE VALUE IS BEING CALCULATED
C     CJO=ZERO BIAS VALUE OF THE DEPLETION LAYER CAPACITANCE
C     CMIN = MINIMUM VALUE OF JUNCTION CAPACITANCE TO BE ALLOWED
C --------------------------------------------------------
      DOUBLE PRECISION FUNCTION FCJ(TAU,IS,THT,J,VC,CJO,CMIN)
      IMPLICIT REAL*8(A-Z)
      IF(VC.LT..9) GO TO 9
      FCJ=CJO*3.162278
      GO TO 10
    9 FCJ=CJO/(DSQRT(1.-VC))
      IF(VC.GT.0.) GO TO 10
      IF(FCJ.GE.CMIN) GO TO 11
      FCJ=CMIN
      RETURN
   10 FCJ=(TAU*THT)*(J+IS)+FCJ
   11 RETURN
      END
C ********************************************************
C FGEN IS A PULSE GENERATOR SUBROUTINE. THE PARAMETERS ARE AS FOLLOWS;
C     ********** PARAMETERS **********
C     HIGH = MAXIMUM VALUE OF FUNCTION
C     LOW = MINIMUM VALUE OF FUNCTION
C     TD = TIME DELAY UNTIL START OF FIRST PULSE ( MAY BE NEGATIVE )
C     TON = TIME OF PULSE DURATION
C     TP = TIME OF PULSE CYCLE PERIOD
C     MNEG = 1 --->  FGEN = HIGH AT TIME = ZERO
C          = 0 --->  FGEN = LOW AT TIME = ZERO
C --------------------------------------------------------
      DOUBLE PRECISION FUNCTION FGEN(HIGH,LOW,TD,TON,TP,MNEG)
      IMPLICIT REAL*8(A-L,N-Z)
      COMMON/CNTRLS/TIME
      IF(MNEG.EQ.1) GO TO 30
      IF(TIME.EQ.0.) GO TO 10
   30 N=(TIME-TD)/TP
      IF(N.LT.0.0) GO TO 10
      M=IDINT(N)
      P=(N-M)*TP
      IF(P.GT.TON) GO TO 10
      FGEN=HIGH
      GO TO 20
   10 FGEN=LOW
   20 RETURN
      END
C --------------------------------------------------------
```

Fig. 8.28. Special Subroutines Required for SCEPTRE Simulations Using the J^3 SCR Model

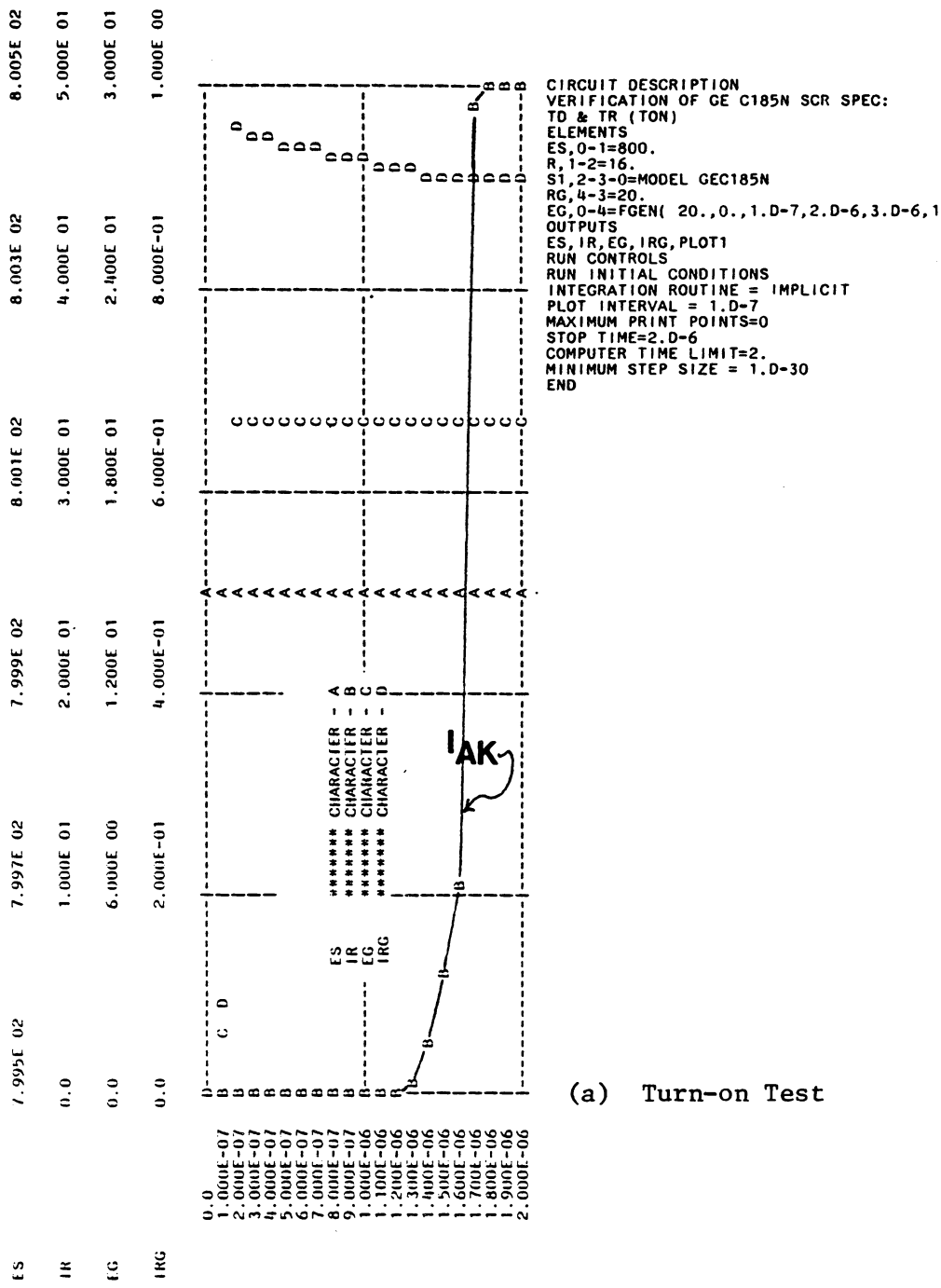
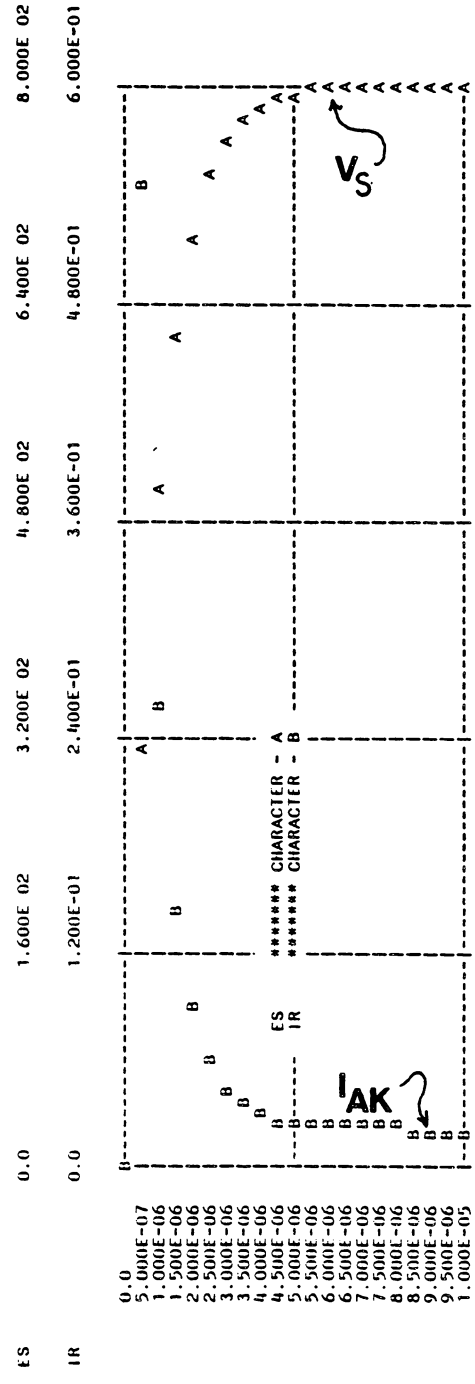
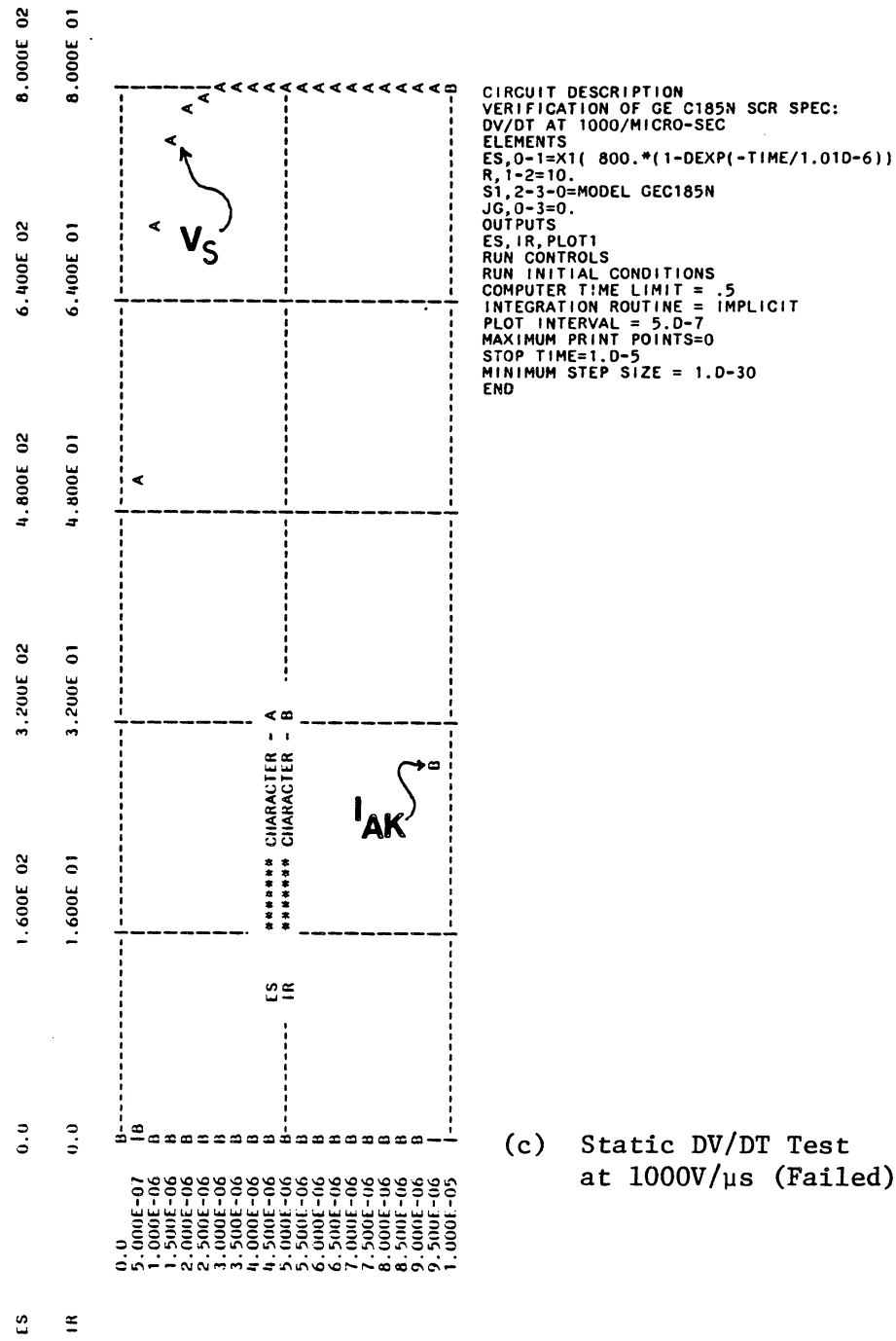


Fig. 8.29. SCEPTRE J[3] SCR Model Performance Verification for the GE C185N SCR

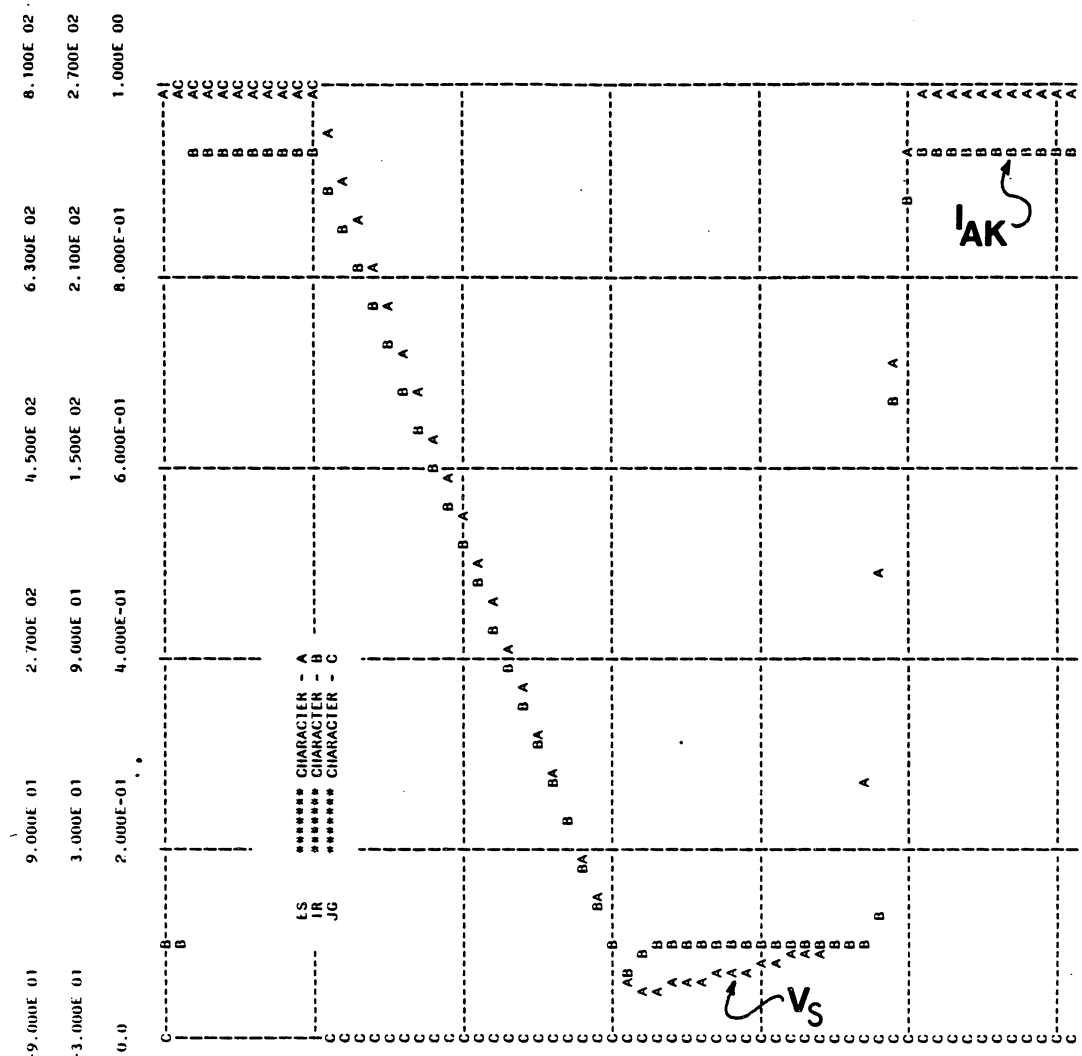



```
CIRCUIT DESCRIPTION
VERIFICATION OF GE C185N SCR SPEC:
DV/DT AT 500/MICRO-SEC
ELEMENTS
ES,0-1=X1( 800.*(1-DEXP(-TIME/1.01D-6)))
R,1-2=10.
S1,2-3-0=MODEL GEC185N
JG,0-3=0.
OUTPUTS
ES,IR,PLOT1
RUN CONTROLS
RUN INITIAL CONDITIONS
COMPUTER TIME LIMIT = .5
INTEGRATION ROUTINE = IMPLICIT
PLOT INTERVAL = 5.D-7
MAXIMUM PRINT POINTS=0
STOP TIME=1.D-5
MINIMUM STEP SIZE = 1.D-30
END
```

(b) Static DV/DT Test at 500V/μs (Passed)

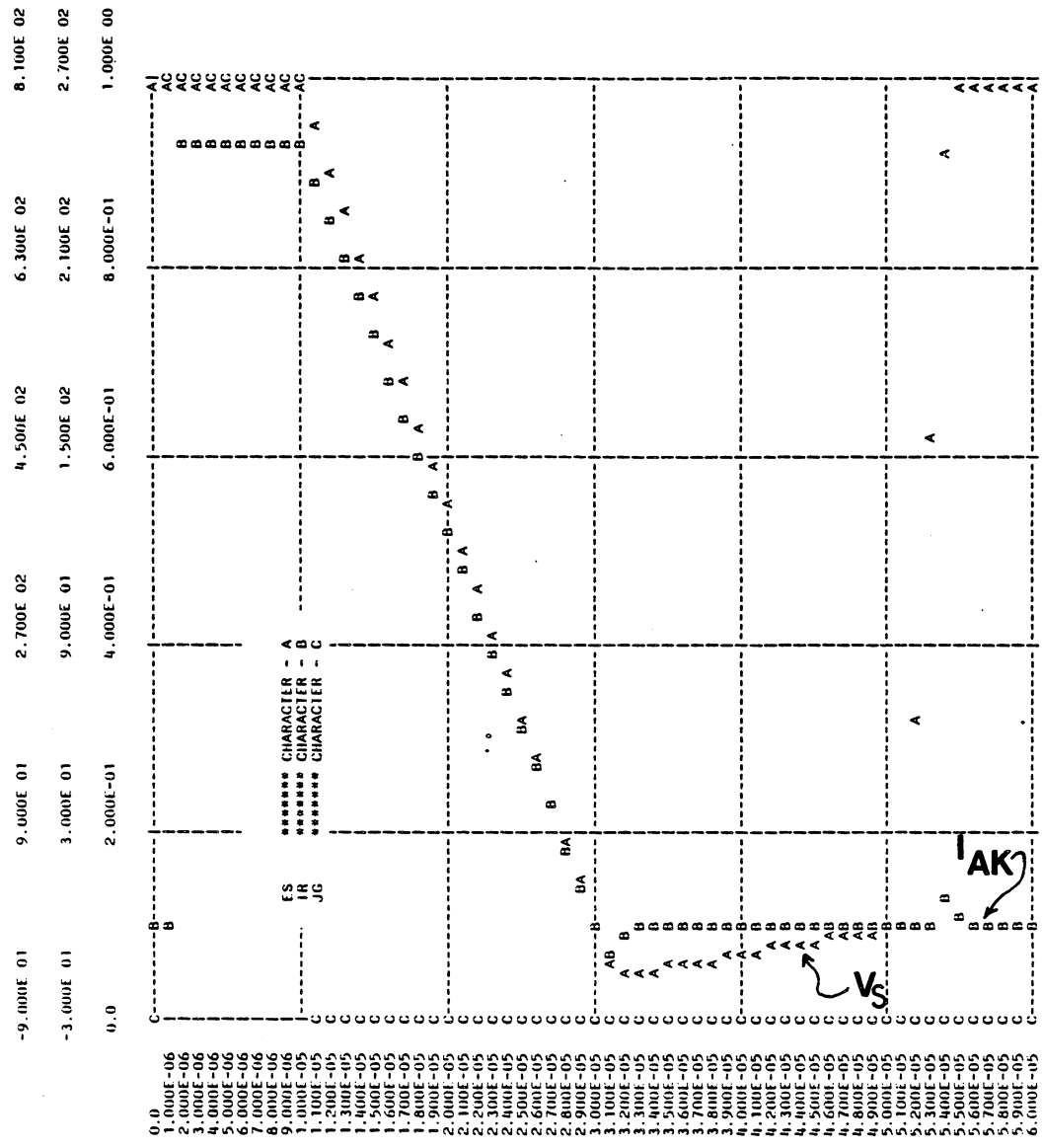


(c) Static DV/DT Test
at 1000V/μs (Failed)




```
CIRCUIT DESCRIPTION
VERIFICATION OF GE C602 LM SCR SPEC: TQ
ELEMENTS
ES,0-1=TABLE 1
R,1-2=3.2
S1,2-3-0=MODEL GEC185N
JG,0-3=FGEN( 1.,0.,0.,1.D-5,100.D-6,TIME,1)
FUNCTIONS
T1=0.,800.,1.D-5,800.,31.25D-6,-50.,46.25D-6,0.,50.25D-6,800.,1.D-4,800.
OUTPUTS
ES,IR,JG,PLOT1
JAS1,JCS1,JKS1,PLOT2
RUN CONTROLS
RUN INITIAL CONDITIONS
INTEGRATION ROUTINE = IMPLICIT
PLOT INTERVAL = 1.D-6
MAXIMUM PRINT POINTS=0
STOP TIME=60.D-6
MINIMUM STEP SIZE = 1.D-30
END
```

(d) Commutation with $dV_r/dt = 200V/\mu s$ at 15μs (Unsuccessful)




```
CIRCUIT DESCRIPTION
VERIFICATION OF GE C185N SCR SPEC: TQ
ELEMENTS
ES,0-1=TABLE 1
R,1-2=3.2
S1,2-3-0=MODEL GEC185N
JG,0-3=FGEN( 1.,0.,0.,1.D-5,100.D-6,1)
FUNCTIONS
T1=0.,800.,1.D-5,800.,31.25D-6,-50.,51.25D-6,0.,54.25D-6,800.,1.D-4,800.
OUTPUTS
ES,IR,JG,PLOT1
JAS1,JCS1,JKS1,PLOT2
RUN CONTROLS
RUN INITIAL CONDITIONS
INTEGRATION ROUTINE = IMPLICIT
PLOT INTERVAL = 1.D-6
MAXIMUM PRINT POINTS=0
STOP TIME=60.D-6
MINIMUM STEP SIZE = 1.D-30
END
```

(e) Commutation with dV_r/dt = 200V/μs at 20μs (Successful)

GE C185N Non-dynamic Performance Data

Performance Quantity	Spec. Sheet or Input Value	J^3 Model Simulation Result
I_{GT}	125 ma.	100 ma D.C - off 130 ma D.C - on
I_H	75 ma.	80 ma - on 70 ma - off
V_T	.7V @ 1 Amp. 1.2V @ 150 Amp.	.85 @ 1 Amp. 1.23 @ 150 Amp.
$V_{(BO)}$	808 V.	808.5V
$V_{(BR)R}$	970 V.	971.5V

(f) Verification of Non-dynamic Performance Specifications

8.9 Summary and Conclusions

The SCR remains the dominant high power semi-conductor electronic power processing device. As more and more power processing circuit designers turn to CADA to tackle the intricacies of non-steady state transient analysis, the acute need for an adequate non-linear switch model to facilitate continuous topology analysis of these circuits is a first order limitation to effective design via CADA. The J^3 SCR Modeling technique has been developed to provide a major stride in bringing the benefits of CADA nearer at hand to the SCR power processing electronics designers.

The J^3 SCR Model is a non-linear circuit anolog to the SCR for which a "user friendly" analytical parameter estimation procedure requiring only manufacturer's specification sheet data has been developed.

Two quite different SCR models, one being Nienhus' Model[2] built around the intrinsic three-junction SCR structure and developed for SCEPTRE, the other being Hu's Model[12] employing the two-transistor SCR anolog and developed for SPICE2, have provided corner stones for this unified SCR model, the J^3 Model, applicable to both SPICE2 and SCEPTRE.

While incorporating the intrinsic three-junction structure of Nienhus' model for a circuit anolog and applying the principle established by Hu of parameter estimation from specification sheet data,

the J^3 SCR Model is otherwise a unique SCR model in its own right. The network anolog is simplified with respect to Nienhus's model, however, the parameter estimation procedure is slightly more complex than that proposed by Hu. This latter being the penalty of improved accuracy in simulating SCR switching dynamics.

The major features of the J^3 SCR Model are that it:

- o Is a high power SCR model, emphasizing reasonably accurate computer simulation of the three major SCR dynamics, gate-pulse turn-on, dV/dt, and t_q.
- o Uses the principle although not the procedure of parameter estimation from specification sheet data as developed by Hu.
- o Has a small equivalent network based on the Nienhus intrinsic three junction structure of an SCR thus allowing SCEPTRE simulation of several SCR's in a network.
- o Has small number of non-linearities to optimize computational efficiency.
- o Is developed by analysis of the model network dynamic equations and semi-conductor physical properties to define model parameters.
- o Provides reasonably accurate simulation of the secondary SCR characteristics of I_{GT}, I_H, V_{on}, $V_{(BO)}$, $V_{(BR)R}$, and V_{GRM}.
- o Is user oriented, analytically determined, and suitable for expansion or alteration to simulate advancing or alternative technology.

- o May be used with any non-linear circuit analysis program capable of handling exponential non-linearities.
- o Is a useful SCR model for simulation of inverter SCR's where turn-off is a critical parameter.
- o May be used with both amplifying gate and non-amplifying gate SCR structures.

Model performance has been tested by computer simulation in all the above listed performance categories using both SPICE2 and SCEPTRE. Simulation results are consistent with manufacturer's specifications for the devices tested.

Although the basic J^3 SCR Model has been developed and its performance verified through computer simulation of simplified single loop test circuits, it has yet to stand the test of applications simulation. Since a major impetus for the development of this model was to be able to do accurate simulation of resonant inverter circuits, then this report will provide that test in the following chapter.

Several potential areas of model improvement have been suggested in the text. Some highlights of possible improvements are:

- o Analytical quantification of reverse recovery charge via τ_A estimation procedure.
- o Implementation of non-constant α's to provide spreading effects. The multi-dimensional polynomial method of formulation may provide an avenue to accomplish this.

CHAPTER 9

SIMULATION OF A SERIES RESONANT DC-DC CONVERTER USING THE J^3 SCR MODEL

9.1 Introduction

The objective of this chapter is to provide a demonstration of the usefulness of the J^3 SCR Model for continuous topology transient analysis. The circuit selected for demonstration is the "Schwarz" converter,[40] a state of the art converter employing a series resonant inverter as an integral part of the power processing operation.

Background and Terminology

The task of power processing electronics is to perform a matching operation of the electrical energy source voltage, current, frequency, and phase characteristics to those of the load circuit. In high-power circuits, it is important to minimize the losses by the power processing circuit. The impetus for efficient power conversion is not only motivated by the desire for energy conservation but also to protect the power processing circuit from excessive internal heating.

Pulse mode power processing circuits are typically the most efficient electronic power processing circuits in use today. Such circuits make use of the principle that the energy dissipation

rate of a circuit is the product of the voltage across the circuit times the current through the circuit. Efficiency is achieved by gating energy through the circuit by complementary alternation of each of the two variables between low and high values with the transition made as rapidly as possible. The pulses of energy are then input to a reactive element filtering network which is designed to pass only those quantities of voltage, current, frequency and phase which are suitable to the load circuit (see figure 9.1).

Consider the need to process high power (greater than 10 KW) from a DC source to a DC load. Two areas of the power processing circuit must be selected appropriately. First considering the filter which consists essentially of passive reactive elements, a great deal of flexibility is available in this area in terms of size and configuration of components. With this thought it seems that the more restrictive area, the gate mechanism may receive first consideration. Typical high-power semi-conductor gating devices are SCRs, BJTs, and MOSFETs.

A comparative analysis of these three switching devices is contained in the following table.[47-51]

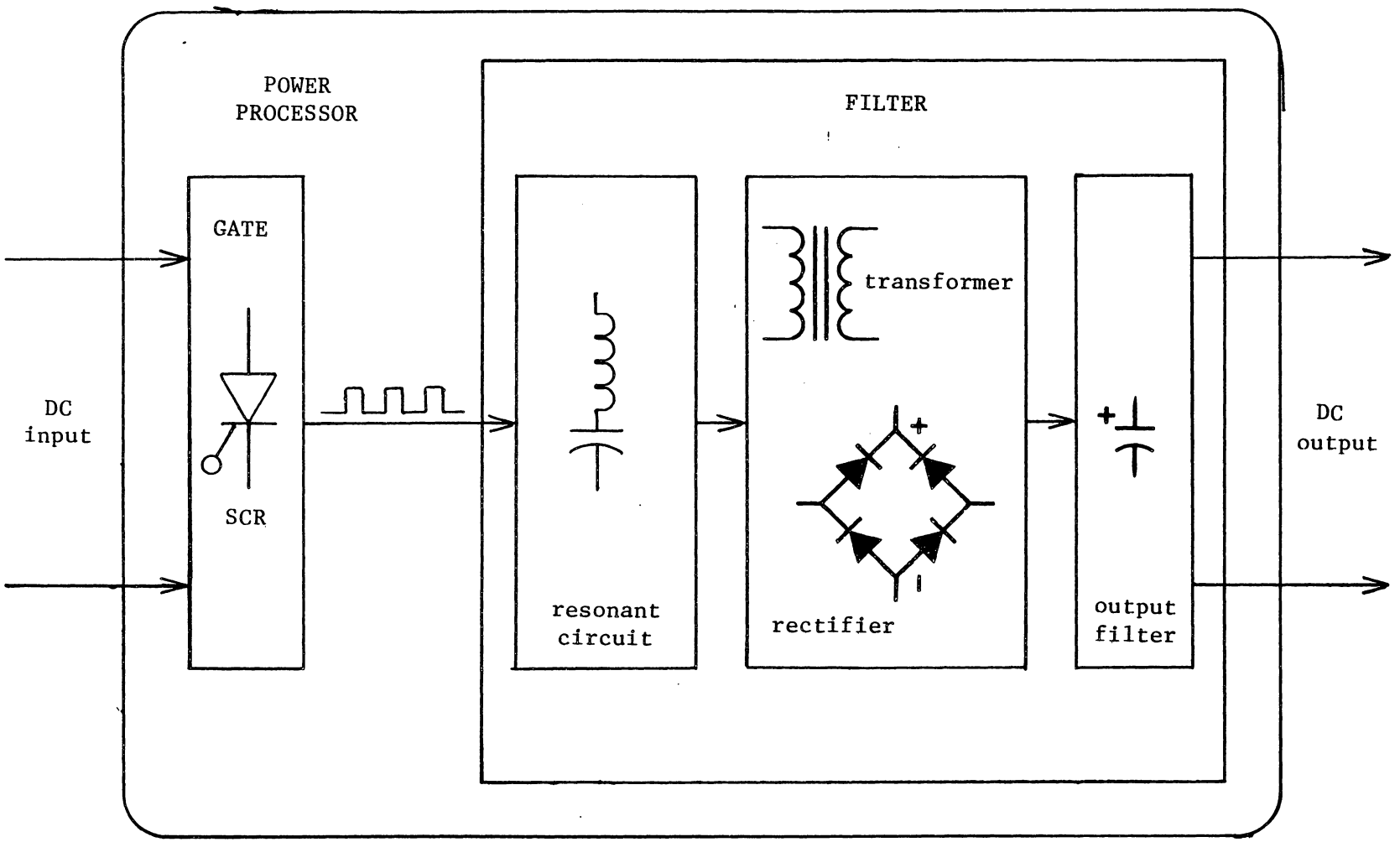


Fig. 9.1. Block Diagram of a Resonant Commutated DC-DC Converter.

Table 9.1 Comparison of SCRs, BJTs, and MOSFETs

Characteristic	Inverter SCRs	BJTs	MOSFETs
Blocking Voltage Forward Reverse	~ 1400 V ~ 1400 V	~ 500 V ~ 5-10 V	~ 500 V ~ .7 V
Max I_{RMS}	~ 750 A	~ 200 A	~ 30 A
Max I_{surge}	~ 7500 A	~ 400 A	~ 70 A
On-stage Voltage drop @ 100 A	Typical 2.5V	2.5V @ β=5	Dev. Not Avail. @ 100 A
Turn-off Time	4-60μs	1-5μs	.5μs
Turn-on Time	3-7μs	.3-1.5μs	.1-.5μs
Series Connection	Easy	Difficult	Easy
Maximum Switching Frequency	100 KHz[52]	200 KHz	500 KHz p.22[50]
Control power @ 100 A	none (pulse turn-on)	High @ β=5	none (pulse turn-on) but Dev. not avail.
Control Turn-off	with GTO device only	Yes	Yes
di/dt limit	Yes	No	No
dv/dt limit	Yes	Usually Not	Usually Not
need transient protection	Yes	Yes	Yes
parallel operation	Yes	Condition-al [49]	Yes
best power level	> 2 KW	< 10 KW	< 1 KW

*specifications in table are generalized and are intended for comparison within the characterization only. Cross comparison between characteristics is not necessarily valid.

From the table 9.1 summary, it is evident that the SCR is a very desirable candidate for the gating device, provided the problem of how to turn the switch off can be solved.

Since the SCR is commutated (turned-off) by reversing the terminal voltage across the device, this is an important problem in performing a DC-DC power processing task.

Commutation techniques for SCRs may be generally categorized in three classifications:

(a) line commutated where polarity change of the source voltage acts to reverse bias the SCR.

(b) load commutated where resonant behavior of the load circuit provides the reverse bias action of the SCR.

(c) force commutated where special circuitry is provided to reverse bias the SCR.

The DC source eliminates (a). The load characteristic can not be relied on to provide resonance behavior so (b) is eliminated leaving (c) as to commutation method.

Typical force commutation circuits are auxiliary commutation circuits. Auxiliary commutating circuits are complex circuits which momentarily remove the load currents from the main SCR and provide reverse biasing so that the device may commutate. Resonant commutation involves the insertion of LC resonant circuitry in the normal load path of the SCR. This type of commutation is similar to load commutation with the distinction being that the commutation circuitry in this case is an integral part of the power processor and not the load.

The simplicity of the resonant commutation technique is attractive and since the pulsed power filtering network has not yet been determined, the possibility of combining the commutating and filtering functions has great appeal.

The power processing scheme is as follows:

> Energy pulses are injected into the filter by the SCR switch. A resonant circuit in the filter forms the pulses into an ac waveform, and, commutates the SCR. The ac is then suitable for conversion to the proper voltage or current magnitude by transformer action. The ac output of the transformer is then converted to DC by a rectifier circuit and smoothed by an output capacitor to form a steady DC.

Although not strictly defined as such, typical power processing electronics nomenclature has been established as follows:

Processing Operation	Designator
DC to DC	converter
AC to AC	transformer, inverter or cycloconverter
AC to DC	rectifier
DC to AC	static inverter (usually just "inverter")

The DC to DC converter just described is an integration of all four processing operations. The operations of transforming and rectifying are basically straightforward. The inverter operation may, however, be very sophisticated. Since the inverter operation controls commutation of the SCRs, then it may also be an integral part of the control mechanism of a regulated power processor.

9.2 Steady State Analysis of the "Schwarz" Converter

Resonant inverter technology has received substantial attention in power electronics research in the past few years.[8,40-46,52] Their light weight and good dynamic performance have made them attractive for aviation and spacecraft applications. Additionally, the exploding computer industry is experiencing a strong need for reliable, efficient, and economical uninterruptible power supplies.

As discussed in the introduction, inverters used in high-power converters use SCRs as the power switch. The selection of resonant commutation for the SCR further restricts the choice of inverter technology to that of a resonant inverter.

This section is an analysis of the inverter configuration selected by Schwarz for use in a resonant converter[1] (term implies use of resonant inverter integral to the converter). The inverter chosen for use by Schwarz is classified as a half-bridge-series-resonant-capacitor-commutated inverter. Also the inverter

employs a split capacitor and single inductor (other inductors may be included as switch protection), with over-voltage protection diodes. The basic power circuit of this inverter is given in Figure 9.2.

The objective of analysis presented here is to obtain a description of the inverter transient while the converter is in steady-state. This analytically derived transient description is to serve as reference for the computer transient calculations of the next section.

The circuit of figure 9.2 is analyzed with the following methodology.

- The circuit is divided into four discrete topologies as determined by switching configurations occurring during a normal operating cycle.
- Since the output filter capacitor, CO, and the load, RL, have a long time constant with respect to the inverter resonant circuit, then the voltage across the primary of the transformer appears as a constant value in the inverter circuit. That value is different for each topology (i.e. e_o, $-e_o$)
- Using Thevinen's equivalent circuits for each topological configuration, each topology appears as a doubly excited reactive circuit. Device protection elements LS1, LS2,

CSN1, CSN2, RSN1 & RSN2, and source impedance, RS, are omitted for simplicity.

- Analysis is then directed towards determining the boundary conditions of each topological region and an analytical description of key circuit variables' transitions through the topological configuration.
- Some operational constraints may be assessed from analytical expressions, but the results are primarily intended to support a graphical interpretation of the cyclic behavior of the inverters.
- The transformer winding ratio has been constrained to 1:1 simply to avoid carrying an additional term in the analysis.

Key definitions of quantities and symbols used in the analysis are as follows.

- w_r - The resonant frequency the LC circuit would exhibit in the absence of any switching (i.e. $1/\sqrt{LC}$).
- w_o - The frequency of the fundamental of the fourier expansion of the waveform describing the cyclic behavior of the switched inverter circuit.
- ρ_{i_o} = The form factor, defined as the ratio I_{RMS}/I_{avg}, of the output current, i_o.
- Series Resonant Inverter - Commutating capacitor in series with the load circuit.
- Doubly excited - Two sources.

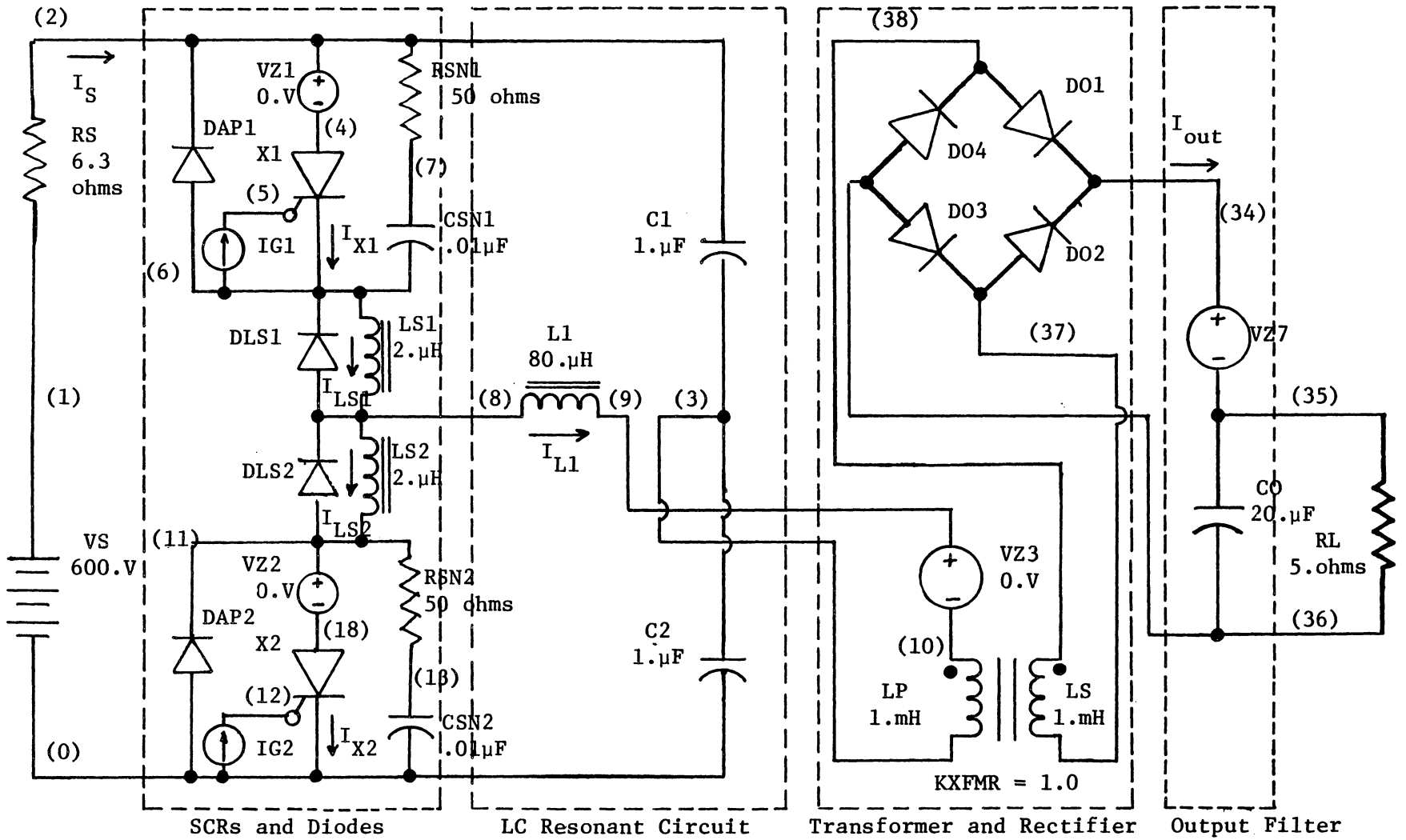
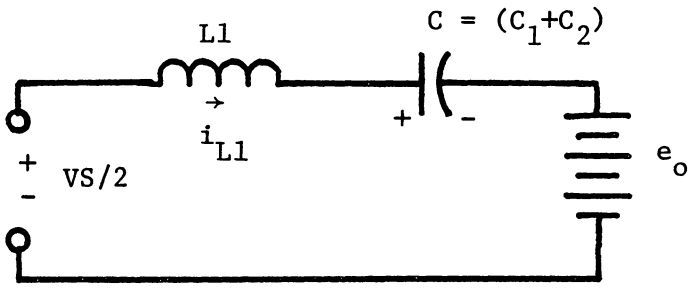


Fig. 9.2. "Schwarz" DC-DC Converter Employing Series Capacitor Commutated Inverter

```
*              SERIES RESONANT INVERTER SIMULATION

     INPUT LISTING                      TEMPERATURE =   27.000 DEG C

********************************************************************************


VS 1 0 600.
RS 1 2 6.3
C1 2 3 1.UF   IC=700.
C2 3 0 1.UF   IC=-150
VZ1 2 4 0.
X1 4 5 6 GEC185N
IG1 6 5 PULSE(0.,1.,10.US,.1US,.1US,10.US,120US)
DAP1 6 2 D
CSN1 6 7 .01UF
RSN1 7 2 50.
LS1 6 100 2.UH
DLS1 100 6 D
VZ4 100 8 0.
L1 8 9 80.UH
RL1 8 9 10.K
VZ3 9 10 0.
VZ5 8 101 0.
LS2 101 11 2.UH
DLS2 11 101 D
VZ2 11 18 0.
X2 18 12 0 GEC185N
IG2 0 12 PULSE(0.,1.,70.US,.1US,.1US,10.US,120US)
DAP2 0 11 D
CSN2 0 13 .01UF
RSN2 13 11 50.
RP 10 3 10.K
LP 10 3 1.MH
LS 38 37 1.MH
KXFMR LP LS 1.
DO1 38 34 D
DO2 37 34 D
DO3 36 37 D
DO4 36 38 D
.MODEL D D
VZ7 34 35 0.
CO 35 36 20.0UF   IC=100.
RL 35 36 5.
RGND 36 0 10.MEG
.TRAN 2.US 200.US UIC
.WIDTH OUT=80
.PLOT TRAN I(VZ1)(-1,150) I(VZ2)(-1,150) I(VZ3)(-150,150) I(VZ7)(0,150)
.PLOT TRAN I(VZ4)
.PLOT TRAN I(VZ5)
.PLOT TRAN V(2,3)(-500,1000) V(3,0)(-500,1000) V(35,36)(0,1000)
.PLOT TRAN V(2,6)(-10,1000) V(11,0)(-10,1000)
.OPTIONS LIST LIMPTS=400 ACCT METHOD=GEAR MAXORD=6 ITL5=10000

            ".SUBCKT of figure 8.25(h)"

.END
***************03/26/83 ************************  SPICE 2E.2 (26SEP78)
```

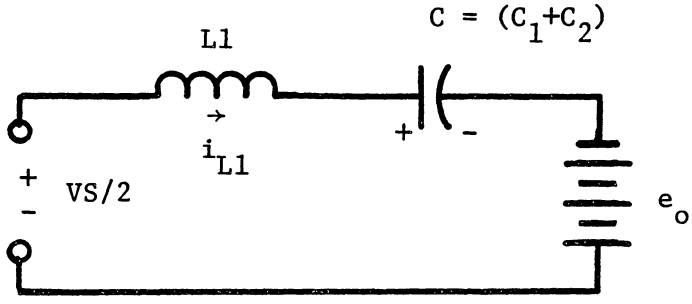
Fig. 9.3. SPICE2 Input Listing for Circuit of Figure 9.2.

Note: RGND is added to meet programming requirements; RL1 & RP are added to improve numerical performance; VZ4 & VZ5 are added to monitor I_{LS1} & I_{LS2} respectively.



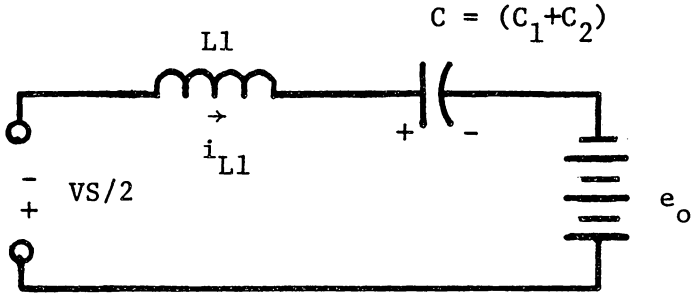
(a) $0 \leq t \leq t_1$: DAP1,2 off

X1 on, X2 off, $i_L(t_1) = 0$



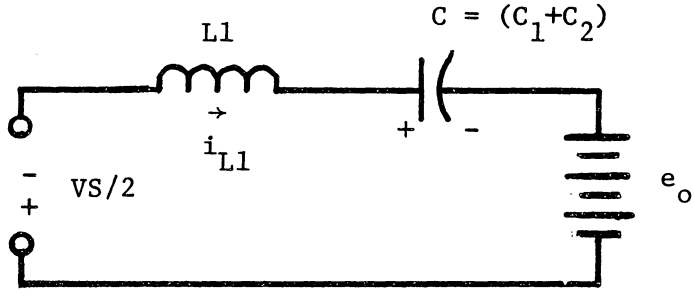
(b) $t_1 \leq t \leq \frac{\pi}{w_o}$: DAP1 on,

DAP2 off, X1,2 off.



(c) $\frac{\pi}{w_o} \leq t \leq t_2$: DAP1,2 off,

X1 off, X2 on, $i_L(t_2)=0$.



(d) $t_2 \leq t \leq \frac{2\pi}{w_o}$: DAP1 off,

X1,2 off, DAP2 on.

Fig. 9.4(a),(b),(c),(d). Doubly Excited Equivalent Circuits for Each Topological Configuration Occurring During One Complete Steady-state Cycle for the Converter of Figure 9.2.

Analysis of the circuit of figure 9.2: definitions, constraints, relations, and assumptions.

(i) $w_r = 1/\sqrt{L1 \cdot C}$ assuming L1, C ideal.

(ii) $C = C1 + C2$

(iii) $w_o = 2\pi/(t_{X1\ on} + t_{DAP1\ on} + t_{X2\ on} + t_{DAP2\ on})$

(iv) $V_{C1} + V_{C2} = VS$ and $V_{C1Avg} = V_{C2Avg} = VS/2$

(v) $Q_C = CV_C = C1(-V_{C1}) + C2(V_{C2})$

(vi) $C1 = C2$

(vii) $Q_{C_{Avg}} = V_{C_{Avg}} = i_{L_{Avg}} = 0$

Although out of sequence with the equivalent circuits of figure 9.4(a),(b),(c),(d), a good starting point for the analysis is time t_1 at which $i_{L1}(t_1) = 0$.

Consider figure 9.4(b). In order for the circuit to oscillate:

(1) $V_C(t_1)$ is greater than $VS/2 + e_o$ $\therefore$ VS and $e_o \simeq$ constant also; by using (ii), (iv) through (vii)

(2) $V_C = \frac{C1}{C}(-V_{C1}) + \frac{C2}{C}(V_{C2}) = \frac{1}{2}(V_{C2}-V_{C1})$

$V_C = \frac{1}{2}(V_{C2}-[VS-V_{C2}]) = V_{C2}-VS/2 = VS/2 - V_{C1}$

comparing to (1) gives operating constraints

(3) $-V_{C1}(t_1)$ is greater than e_o and $V_{C1}(t_1)$ is less than $-e_o$

$V_{C2}(t_1)$ is greater than $VS + e_o$

The transient from t_1 to π/w_o is governed by the loop equation.

$$(3)\quad VS/2 - L1(di_{L1}/dt) - 1/C \int_{t_1}^{t} i_{L1}dt - V_C(t_1) + e_o = 0$$

letting $i_{L1} = C(dV_c/dt)$ gives.

$$(4)\quad L1\cdot C(d^2V_c/dt) + \int_{t_1}^{t} dV_c + V_c(t_1) = VS/2 + e_o$$

solving the integral then using Laplace transforms, L{}

$$(5)\quad V_C(S) = \frac{1/(L1\cdot C)[VS/2+e_o]}{S(S^2+1/(L1\cdot C))} + \frac{SV_C(t_1)}{(S^2+1/(L1\cdot C))}$$

Now taking L^{-1} {} yields

$$(6)\quad V_C(t_1 < t < \frac{\pi}{w_o}) = [V_C(t_1) - VS/2 - e_o]COS(w_r(t-t_1)) + [VS/2 + e_o]$$

at $\frac{\pi}{w_o}$ the boundary condition is

$$(7)\quad V_C(\frac{\pi}{w_o}) = [V_C(t_1) - VS/2 - e_o]COS((w_r/w_o)\pi - w_r t_1) + [VS/2 + e_o]$$

which provides some insight into relation between w_r and w_o.

Now looking at i_{L1}.

$$(8)\quad i_{L1}(t_1 < t < \frac{\pi}{w_o}) = [C/L1]^{1/2}[VS/2 + e_o - V_C(t_1)]Sin(w_r(t-t_1))$$

and

$$i_{L1}(\frac{\pi}{w_o}) = [C/L1]^{1/2}[VS/2 + e_o - V_C(t_1)]\text{Sin}((w_r/w_o)\pi - w_r t_1)$$

Proceeding to treat the interval $\frac{\pi}{w_o} < t < t_2$, observe that there are now two non-zero boundary conditions $V_C(^{\pi}/w_o)$ and $i_{L1}(^{\pi}/w_o)$. Close observation of the circuit provides solution to the describing equations in this region.

- The ckt has only a reversal of the polarity of VS/2 · i.e. VS/2 = -VS/2.
- The result is that the system trajectory will still be a sinusoidal with frequency w_r but there will be a new resonant peak amplitude and a discontinuity in phase of the oscillatory trajectory.

Shifting the time reference to $t = {}^{\pi}/w_o$ and letting VS/2 = -VS/2 gives.

$$(9)\quad V_C(\frac{\pi}{w_o} < t < t_2) = [V_C(\frac{\pi}{w_o})/\text{COS}\ \psi + VS/2 - e_o]\text{COS}(w_r(t-\frac{\pi}{w_o})+\psi) + [e_o - VS/2]$$

$$(10)\quad i_{L1}(\frac{\pi}{w_o} < t < t_2) = [C/L1]^{1/2}[e_o - VS/2 - V_c(\frac{\pi}{w_r})/\text{COS}\ \psi] \times \text{Sin}(w_r(t-\frac{\pi}{w_o})+\psi)$$

where:

$$(11)\quad \psi = \mathrm{Sin}^{-1}\left\{\frac{VS/2 + e_o - V_C(t_1)\mathrm{Sin}((w_r/w_o)/\pi - w_r t_1)}{-VS/2 + e_o - V_C(\frac{\pi}{w_o})/\mathrm{COS}\ \psi}\right\}$$

when ψ is small, the transcendental eq'n, (11) may be approximated by letting

$$(12)\quad \mathrm{COS}\ \psi \simeq 1.$$

The equations (1) thru (12) describe one-half cycle, π/w_o, of the operation of Schwarz's [1] inverter circuit used in the converter in figure 9.2. Since steady-state operation is symmetric, then further analysis is redundant. Figure 9.5 is a graphical representation of this analysis.

The analysis of the inverter was limited to steady-state behavior operating into a voltage stiff load. Also boundary conditions were chosen to ease calculation. Removal of either of these constraints make the analysis by hand prohibitive. Such a task is well suited for a computer problem. Additionally a computer analysis might well deal with the subject of load transient analysis and control.

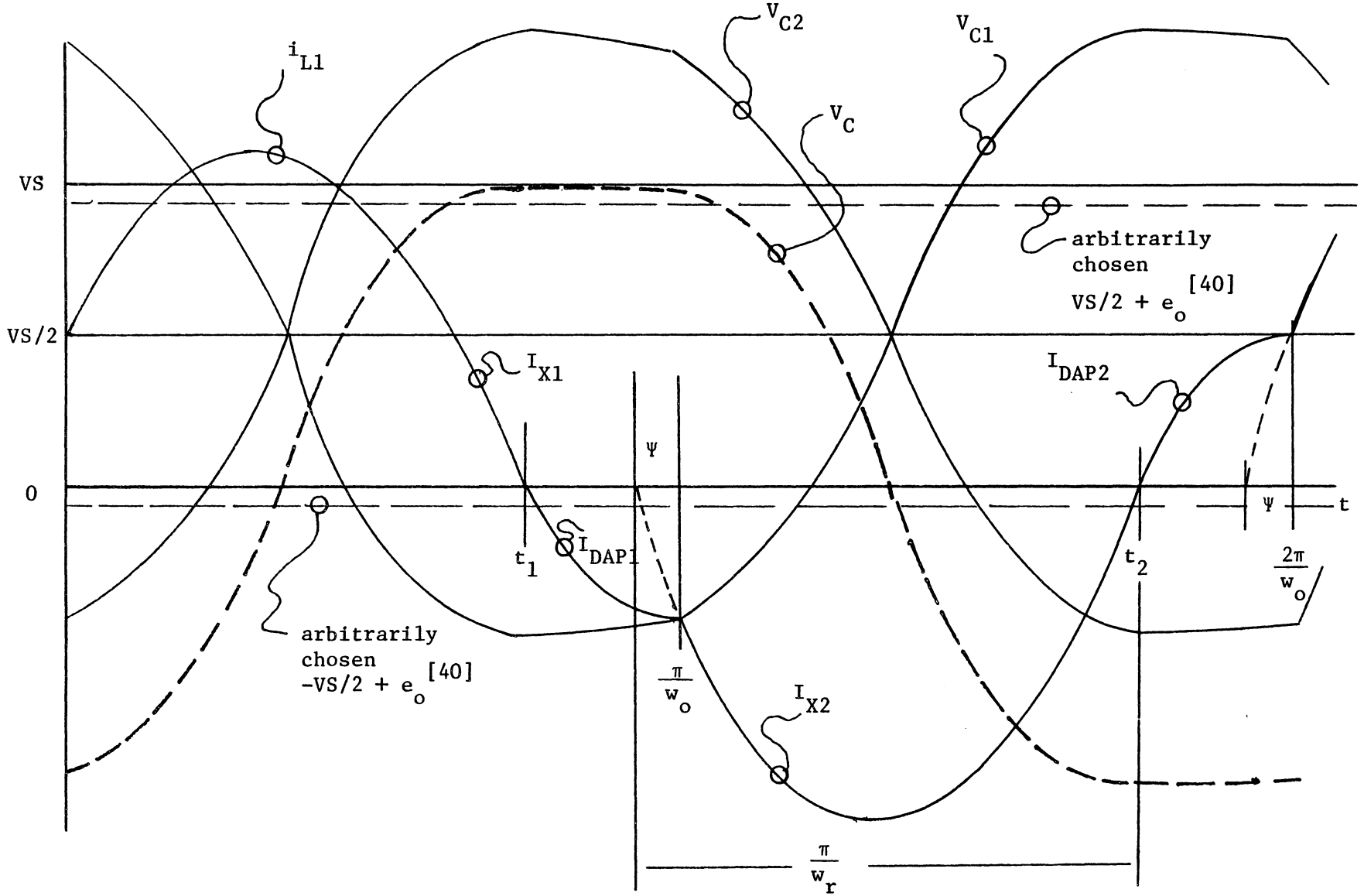


Fig. 9.5. Graph of One Cycle of Steady-state Operation of the Inverter Circuit Contained in the Converter of Figure 9.2.

9.3 Simulation of the "Schwarz" Converter

The "Schwarz" converter simulated in this section is illustrated in figure 9.2. The primary component values are those used in the simulation of the same circuit by M. Dougherty in reference [8]. Dougherty's simulation employed SCEPTRE as the CAD program whereas SPICE2 is used here. Use of SPICE2 requires a few changes in the circuit. For instance, the inductors LS1 and LS2 are each 160 μH saturable reactors in Dougherty's work. Unfortunately SPICE2's nonlinearity simulation capability is inadequate to formulate the saturation characteristic in this case. For this reason, 2.μH inductors with diodes DLS1 and DLS2 in parallel are used instead. Since these components provide switch transient suppression and should have only minor influence on resonant behavior, the substitution is acceptable.

Other changes from Dougherty's circuit such as the transformer turns ratio, output filter capacitor and load resistor have been made to illustrate inverter performance.

The SPICE2 input listing for the circuit of figure 9.2 is given in figure 9.3. That listing is for a simulation with the inverter operating in near steady-state.

The simulations presented in this section treat three different conditions of operation. The first and second are fault conditions for which simulation results are illustrated in figures 9.6 and 9.7. The third is the near steady-state operation of a properly operating converter. Results for the latter are shown in figure 9.8.

Simulation of a t_q Failure

A commutation failure is demonstrated in figure 9.6(a) through (d). The SCR used in the "Schwarz" converter simulations is the GE C185N, an inverter SCR with a typical t_q rated at 15μs. The J^3 SCR model for the C185N was shown in chapter 8 to predict t_q between 11.5μs and 20μs depending on the value of reverse voltage applied.

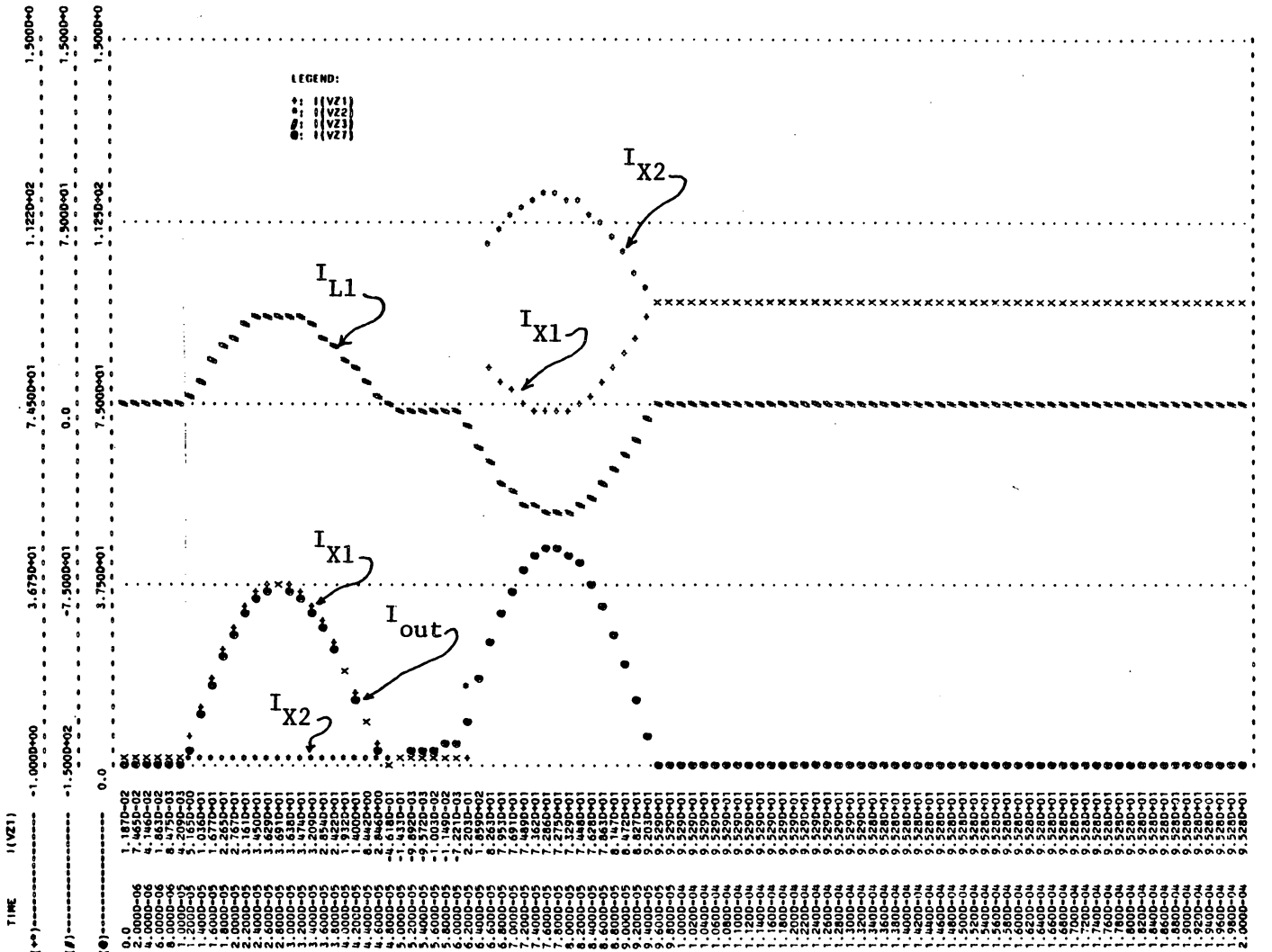
The "Schwarz" converter clamps $|-V_{AK}|$ to one diode drop due to DAP1 and DAP2. This condition results in maximum t_q [22].

The transient simulation has the circuit of figure 9.2 started from an off state at time zero. The gate pulses IG1 and IG2 are applied with the first pulse occurring at t = 10μs and repeated at 100μs intervals.

The data in figure 9.6(a) shows that X1 turns on properly and proper resonant behavior occurs in the interval 10μs to 46μs at which time I_{L1} reverses by conduction of DAP1. This behavior is also proper and continues until t = 60μs.

At t = 60μs, X2 is fired by IG2. The firing of X2 results in both SCRs X1 and X2 conducting. Analysis of the voltage on X1 (i.e. V_{X1} in figure 9.6(a)) shows that only 10μs duration was available for device commutation which is less than the rated t_q for the C185N.

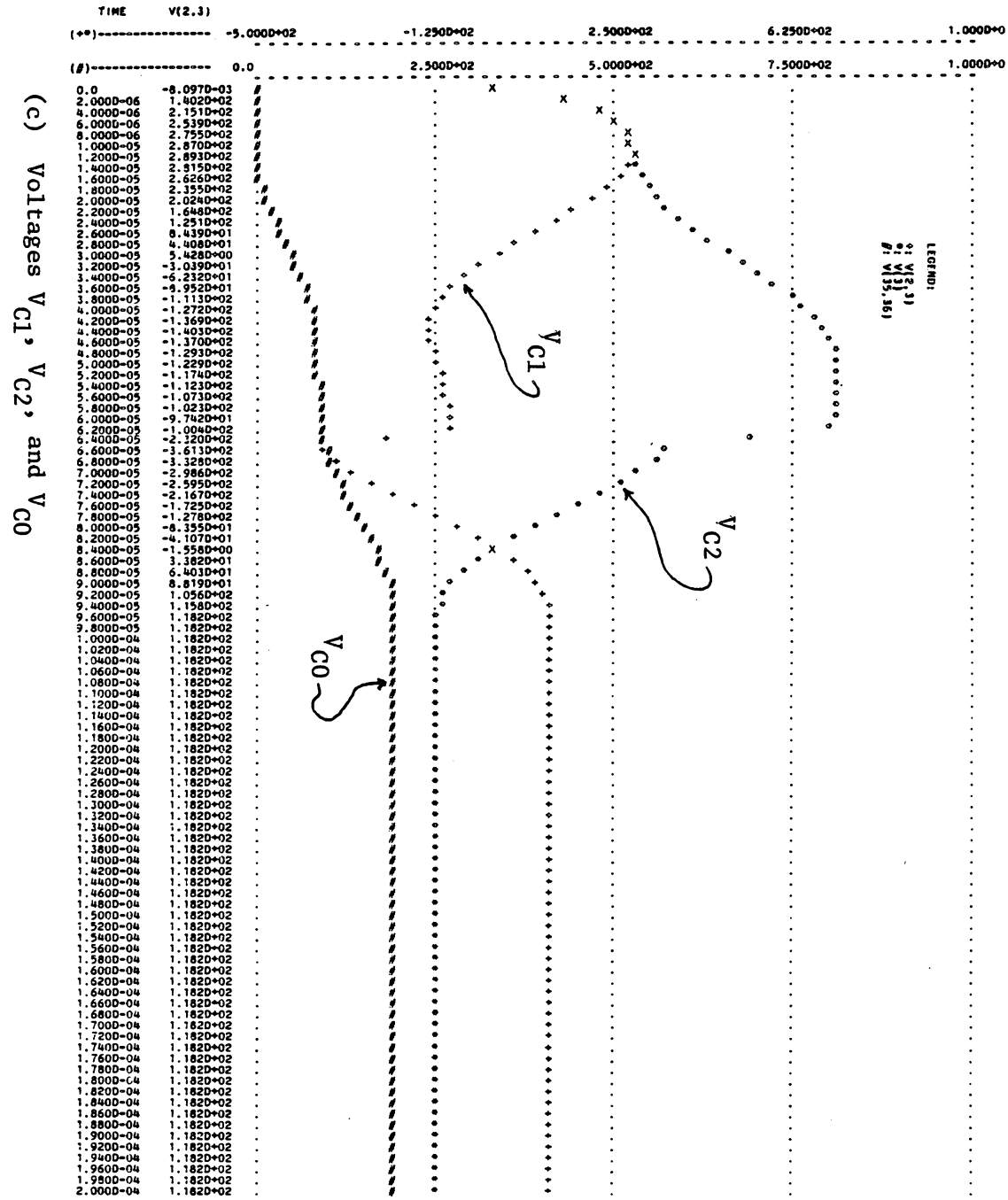
It is seen by this demonstration that the J^3 SCR model accurately predicts a commutation failure and the detrimental effects on circuit behavior.



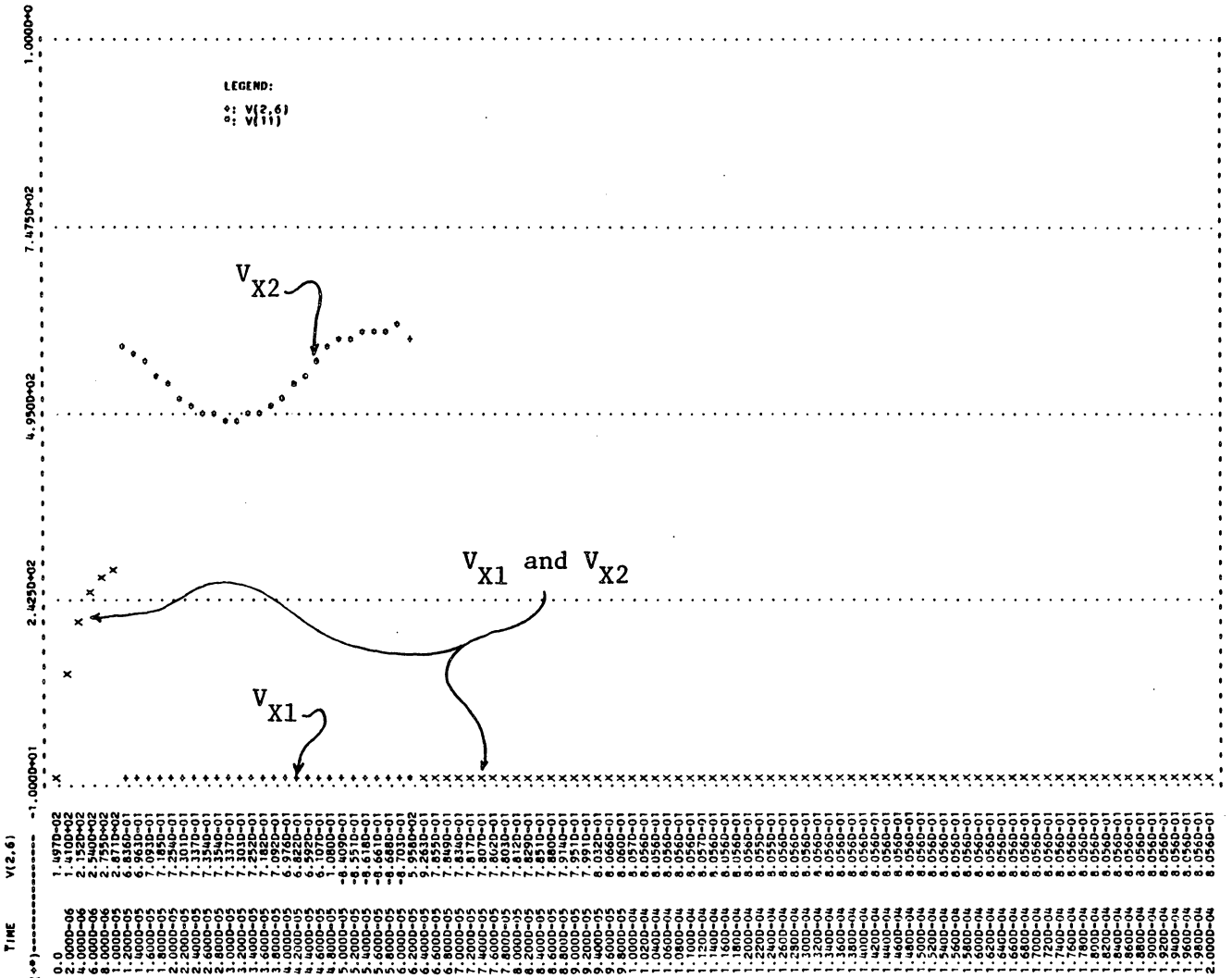
(a) Currents I_{X1}, I_{X2}, I_{L1}, and I_{out}

Fig. 9.6. "Schwarz" Converter with Insufficient SCR Commutation Time

(b) Currents $I_{LS1} + I_{DLS1}$ and $I_{LS2} + I_{DLS2}$



(c) Voltages V_{C1}, V_{C2}, and V_{C0}



(d) Voltages V_{AK} for X1 (i.e. V_{X1}) and V_{AK} for X2 (i.e. V_{X2})

Simulation of a Light Load Failure

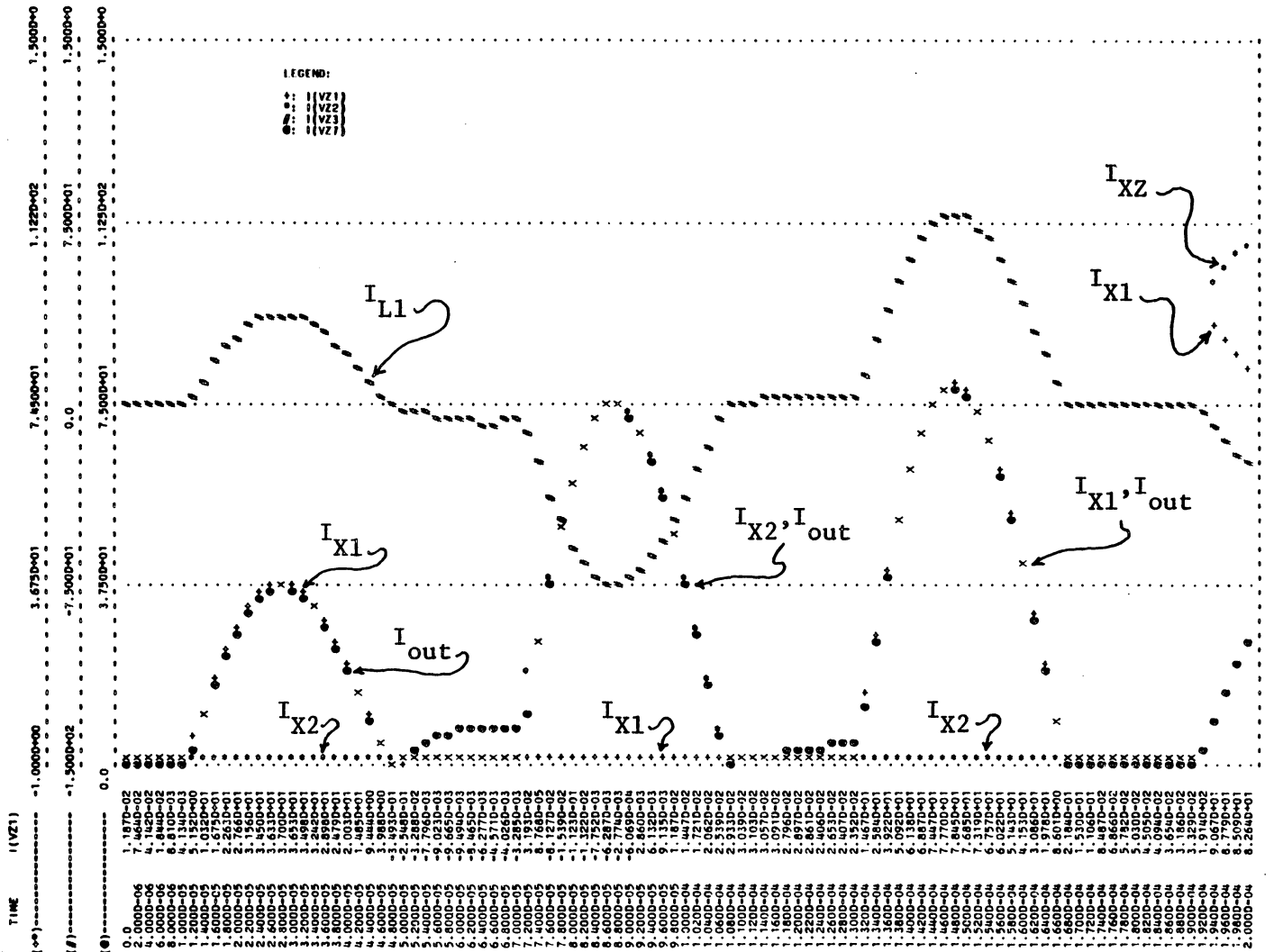
For the circuit of figure 9.2, the output capacitor and load resister are made to be CO = 10.μF and RL = 10Ω. Also, the period for pulses IG1 and IG2 is increased to 120μs thus providing a 10μsec increase in time available for SCR commutation.

Simulation for this configuration is again started from an off state at t = 0. The simulation data is shown in figure 9.7(a) thru (e).

SCR X1 is seen to successfully commutate as illustrated by the proper resonant behavior of the current waveform, I_{L1}, in figure 9.7(a) from t = 0 until t = 168μs. At 168μs, I_{L1} is observed to not reverse polarity as is expected for the interval in which DAP1 should be conducting. In fact the current waveform for I_{X1} (figure 9.7(a)) and I_{LS1} (figure 9.7(b)) shows that the current through X1 does not go to less than zero as expected, but instead remains greater than I_H for the C185N until 176μs and is only less than I_H for 14μs occurring between 176μs and 190μs. This is insufficient time for the device to recover a forward blocking capability at rated dV/dt reapplied.

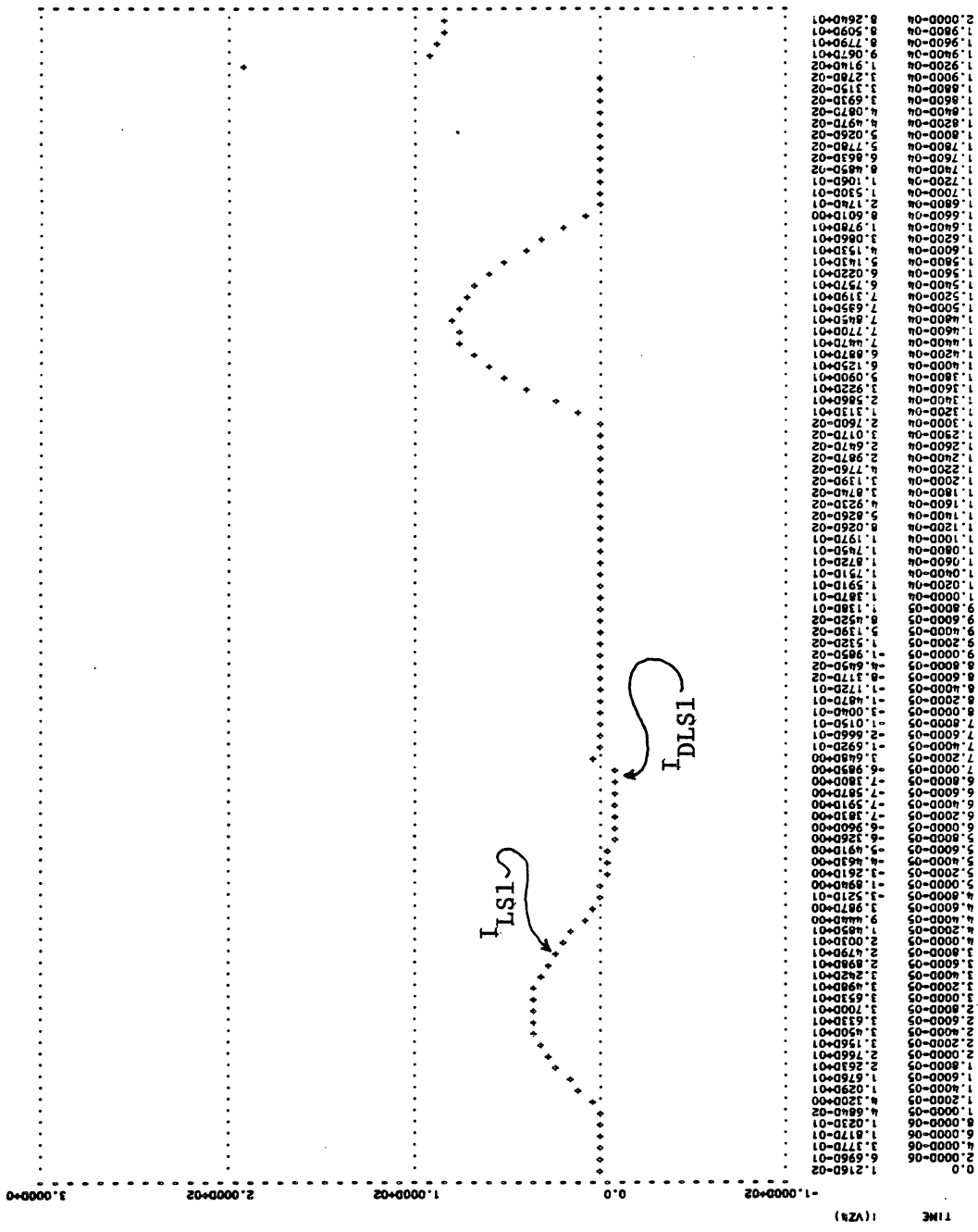
The waveform for I_{LS2} in figure 9.7(c) shows it to be of essentially the same magnitude as I_{X1} and I_{LS1} consequently the current in I_{X1} is a leakage current through DAP2 and X2.

The root cause of circuit failure is seen by examining the waveform for V_{CO} and V_{C2} in figure 9.7(d) and observation that the source voltage is 600V. It is seen that $V_{CO}(t = 190\mu s) \approx 210V$ and



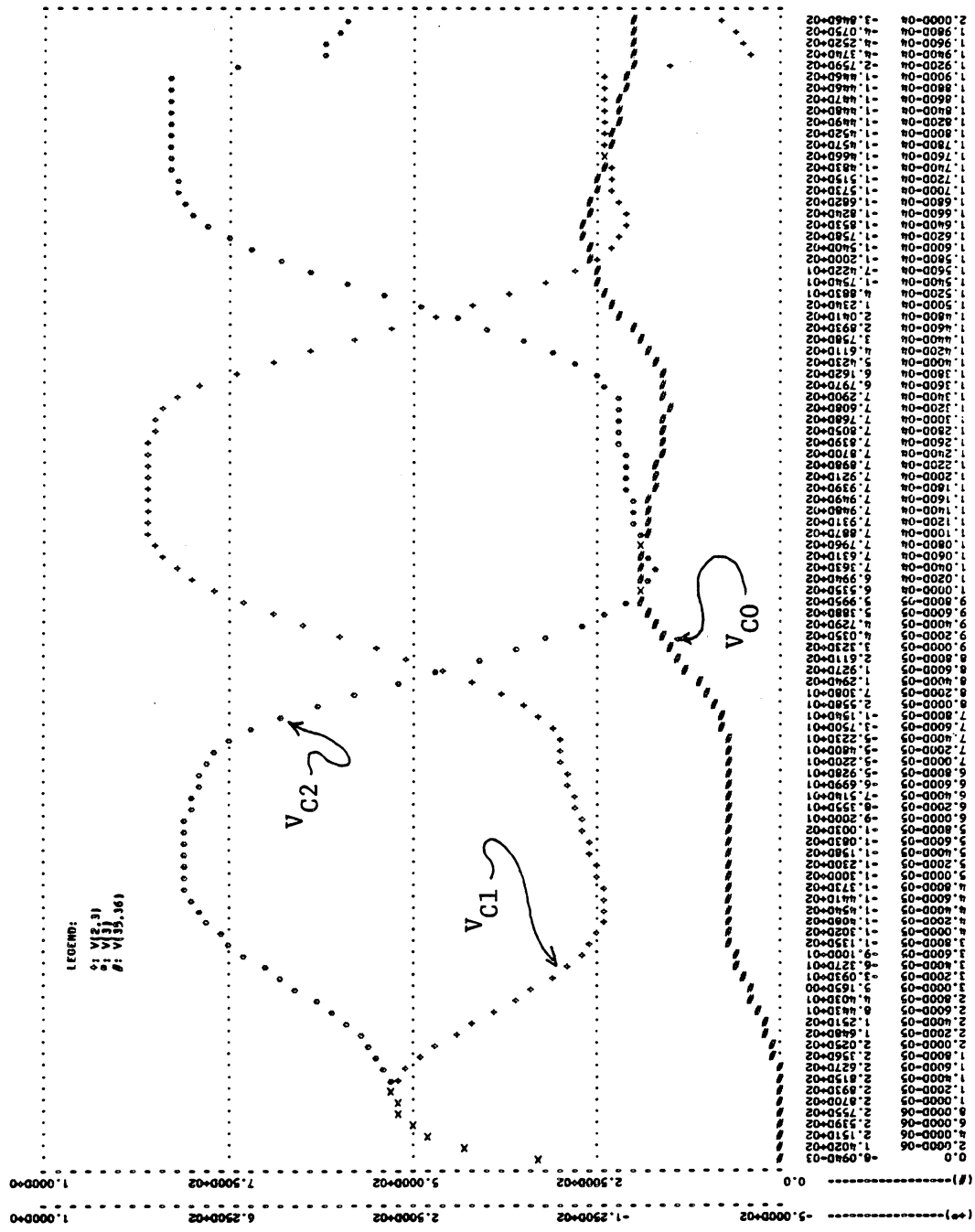
(a) Currents I_{X1}, I_{X2}, I_{L1}, and I_{out}

Fig. 9.7. "Schwarz" Converter With RL Too Large

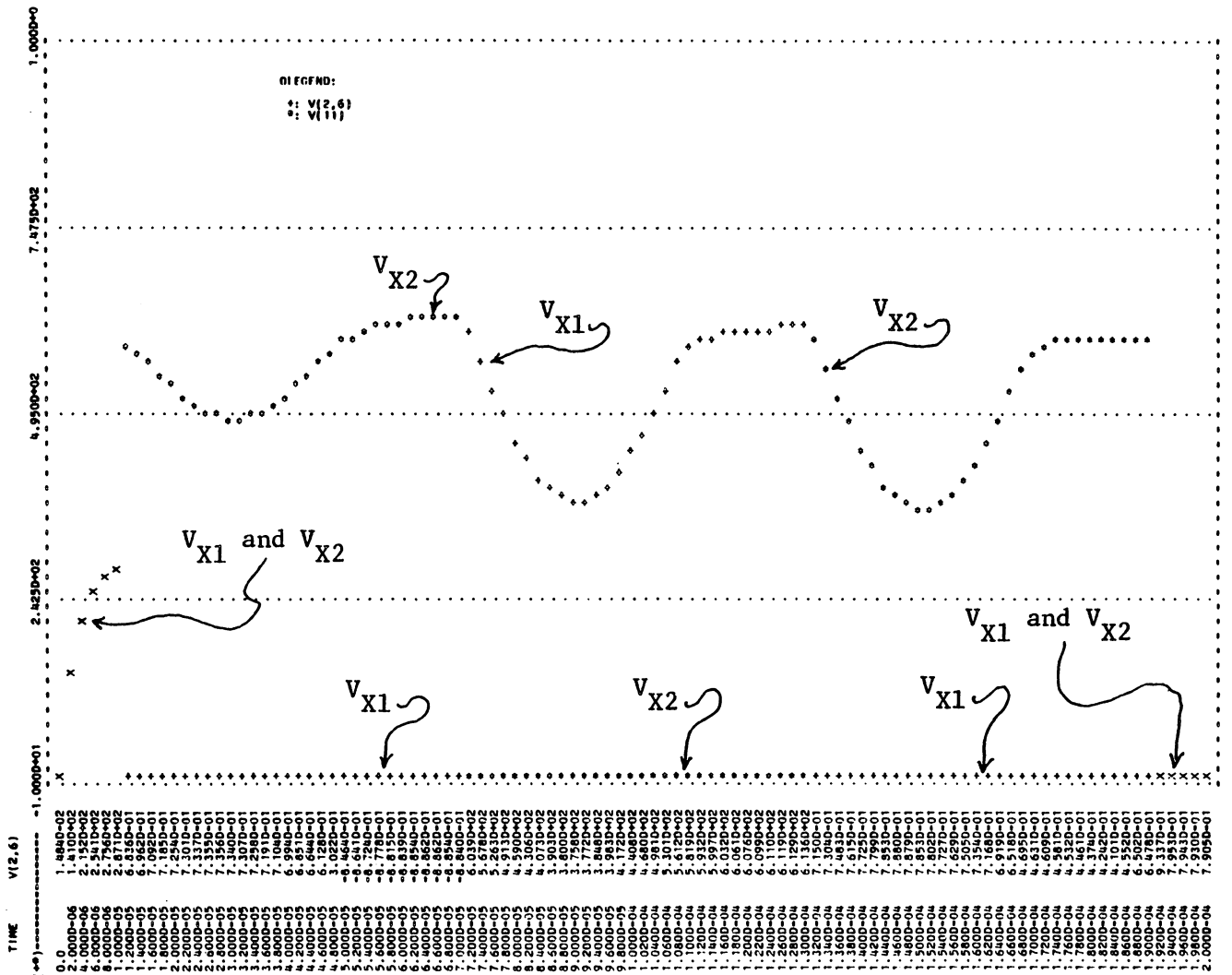


(b) Currents I_{LS1} + I_{DLS1}

(c) Current $I_{LS2} + I_{DLS2}$



(d) Voltages V_{C1}, V_{C2}, and V_{C0}



(e) Voltages V_{AK} for X1 (i.e. V_{X1}) and V_{AK} for X_2 (i.e. V_{X2})

V_{C1} (t = 190μs) ≈ 745V. The conclusion is that V_{C1} has insufficient voltage to initiate reversal of current through L1 and DAP1 in order to reverse bias X1. The high voltage on V_{CO} is due to RL being too great to adequately load CO. This condition is termed an "overdamped" inverter.

The application of the IG2 pulse at 190μs brings both SCRs into conduction simultaneously and consequent inverter failure. A regulated converter would detect this high V_{CO} condition and delay X2 firing.

Simulation of a Properly Operating "Schwarz" Converter

Having demonstrated that the J^3 SCR model is useful in simulating an incorrectly operating "Schwarz" converter, it is desirable to demonstrate simulation of a properly operating circuit.

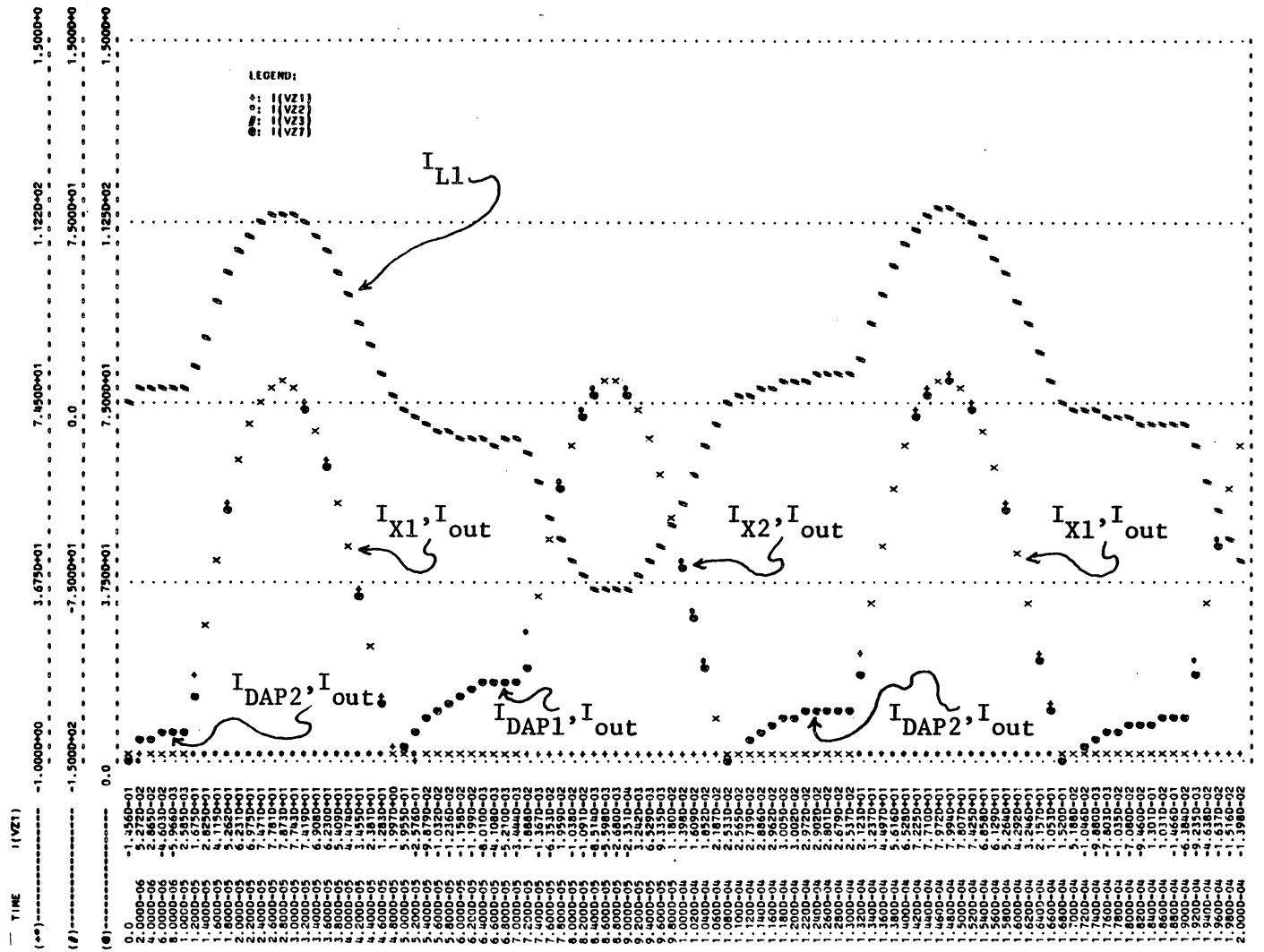
Changes in the circuit input data to SPICE2 are as follows. RL is decreased to 5.ohms to increase the circuit loading thereby eliminating the overdamped condition of the previous simulation. CO is increased to 20.μF in order to maintain the output circuit time constant to be longer than one-half the period of the resonant circuit. At the same time, the choice of the output circuit time constant is kept short enough to provide good visibility of output circuit dynamics with a few switching cycles of the converter.

Non-zero initial conditions are also provided in the input listing in order to move the simulation interval nearer to projected

steady-state cyclic behavior. Initial conditions provided are V_{C1} = 700.V, V_{C2} = -150.V, and V_{C0} = 100.V. These values were arbitrarily chosen from examination of previous results. They were observed to be values close to those occurring during a cycle of operation. The choice of the sum of V_{C1} and V_{C2} to be less than 600V was to allow for V_{RS} drop due to source current.

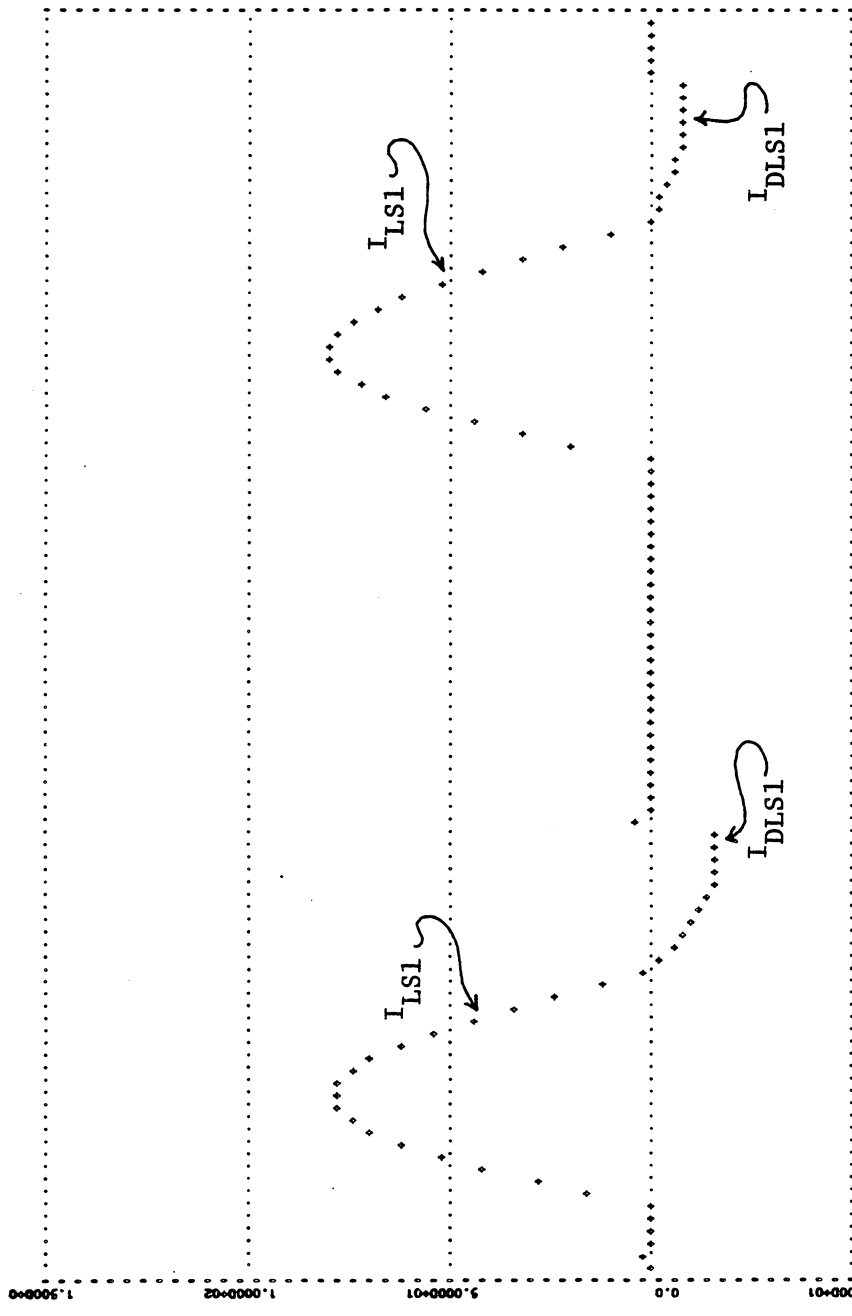
Simulation data is shown in figure 9.8(a) thru (e). Figure 9.8(a) shows that I_{L1} current varies through two switching cycles in a manner suggestive to that predicted in the analytical prediction for steady-state behavior shown in figure 9.5. The circuit is not in complete steady-state as is evidenced by the change in the antiparallel diode currents, I_{DAP1} and I_{DAP2} illustrated in figure 9.8(a). It is approaching steady-state, however, since the relative change from cycle to cycle is becoming relatively less. Figures 9.8(b) and (c) show the currents through the SCR and antiparallel diode pairs during intervals applicable to each one-half switching cycle. These currents show a properly operating circuit with ample commutation time (approx. 24μs) available to the SCRs.

Figure 9.8(d) shows the voltages V_{C1} and V_{C2} to follow trends very much like the analytically predicted trends illustrated in figure 9.5. An interesting variation from analytical prediction occurs at the SCR firing times of 10μs, 70μs, 130μs, and 190μs. At these times, C1 and C2 alternately show an inflection in the voltage of the negatively charged capacitor which does not appear in the voltage of the positively charged capacitor. This suggests

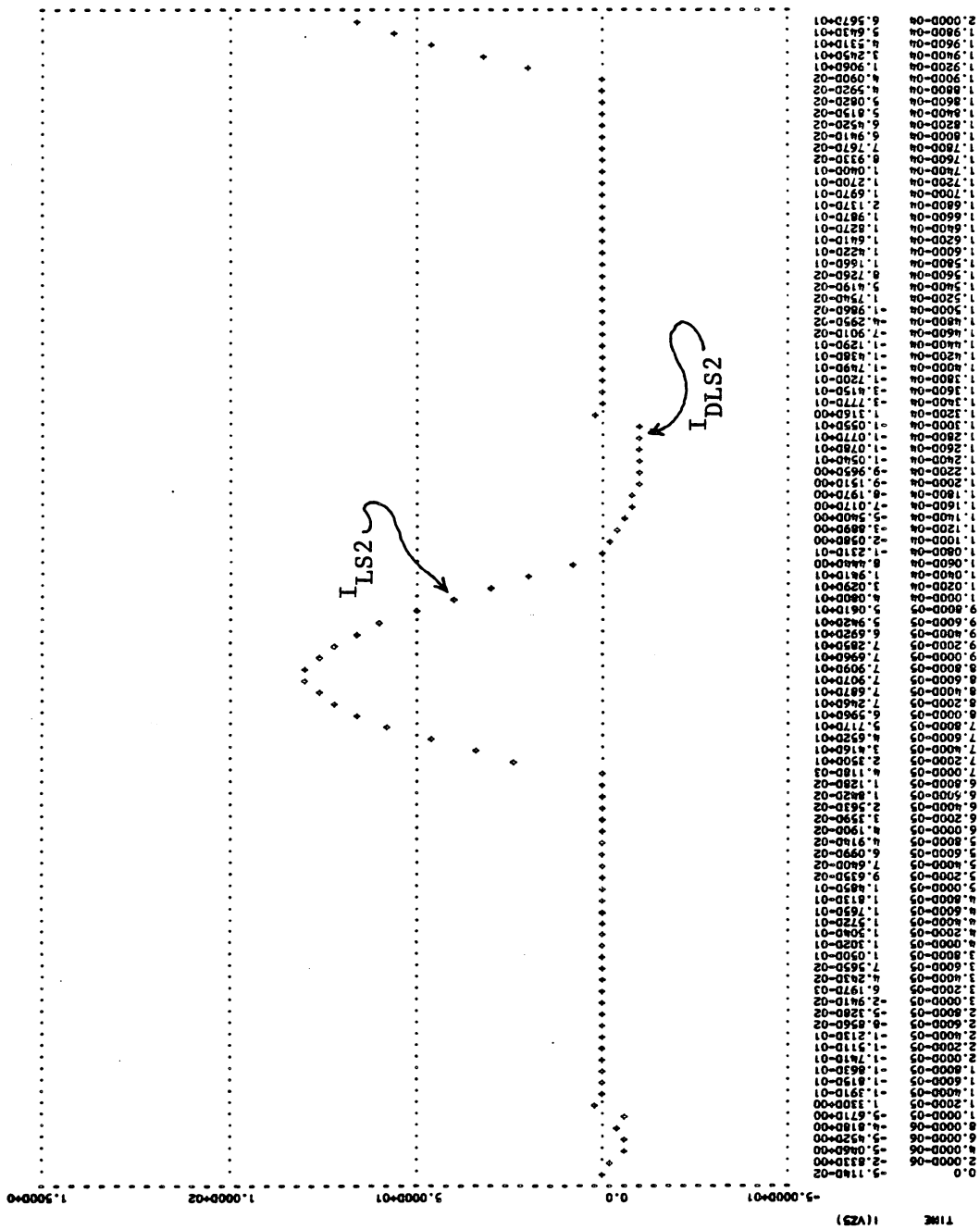


(a) Currents I_{X1}, I_{X2}, I_{L1}, and I_{out}

Fig. 9.8. "Schwarz" Converter in Near Steady-State

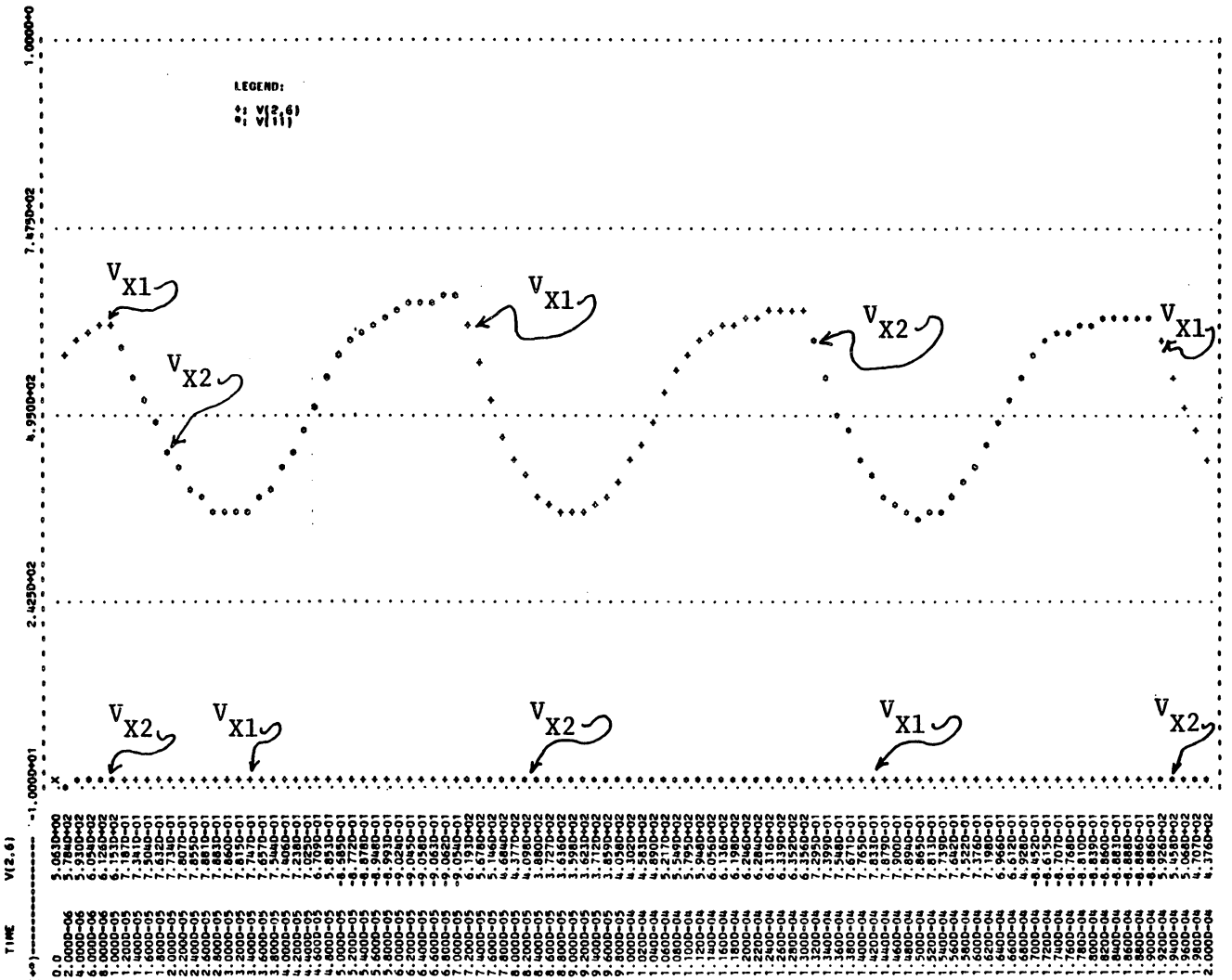


(b) Currents $I_{LS1} + I_{DLS1}$



(c) Current $I_{LS2} + I_{DLS2}$

(d) Voltages V_{C1}, V_{C2}, and V_{C0}



(e) Voltages V_{AK} for X1 (i.e. V_{X1}) and V_{AK} for X2 (i.e. V_{X2})

a change in node to node voltage which is not shared equally by the two capacitors. Since the inflection coincides with SCR switching, it is seen to correspond to an increase in source current causing a voltage drop across RS. The negatively charged capacitor is in the source current loop at this time whereas the positively charged capacitor is not. Consequently the negatively charged capacitor experiences a voltage change which does not have a corresponding change in the positively charged capacitor.

SCR terminal voltages, V_{X1} and V_{X2}, are monitored in figure 9.8(c). No evidence of excessive dV/dt or overvoltage is apparent in these waveforms.

9.4 Summary and Conclusion

The simulation demonstration presented in this chapter is for a half-bridge series-resonant inverter integral to a DC-DC converter popularly known as a "Schwarz" converter.

Two failure conditions involving circumstances under which the conducting SCR may fail to commutate have been demonstrated. These simulations would not have been possible without an SCR model which was accurately able to predict SCR commutation time, t_q. The J^3 SCR model has proven its ability to provide that capability.

Simulation of a properly operating converter has also been provided here for comparison to an analytical prediction of the "Schwarz" converter based on a discrete multiple topology analysis technique.

In this technique a simplified equivalent circuit of the converter was determined for the four topologies occurring in a normal steady-state cycle of operation. The correspondence of computer simulation and analytical results serves to establish the validity of the simulation. Deviation of simulation results from analytical prediction of ideal circuit behavior was shown to be explainable as a consequence of inclusion of non-ideal elements in the simulation. Two were examined. They were the effects of the load voltage which varied in a manner inconsistent with the stiff output voltage approximation and the effects of a non-ideal source voltage which included a source resistance.

The simulation demonstrations in this chapter all required less than 35 cpu seconds of computer time to simulate two cycles of inverter operation.

This simulation exercise demonstrates the usefulness of a non-ideal switch model to serve as a design aid in inverter circuit design. A literature search in this area shows no previous documentation of such a capability as is offered by the J^3 SCR model.

SUMMARY AND CONCLUSIONS

This report presents research to develop a general purpose non-linear computer model for the SCR. The research effort deals with development of both a network anolog and a parameter estimation procedure for the model. The model developed as the end result of this research is a general purpose model within the computational environment for which it is intended. That environment is the electronic circuit analysis capabilities offered by currently in use advanced non-linear CADA programs such as SPICE2 and SCEPTRE.

Research was conducted in three distinct phases. Groupings of chapters in the text are associated with each of these phases.

Chapters 2 through 4 present the first phase of research in which an SCR model developed by Chemning Hu [1,12] is modified to improve its performance.

It is shown in Chapter 2 that Hu's model denoted the "Hu-ki model"performs poorly in simulating SCR turn-off transient behavior. An improved SCR model denoted the "Modified Hu-ki model" was developed as part of this thesis. Both the "Hu-ki model" and the "modified Hu-ki model" are for specific application to SPICE2. Each utilizes the two-transistor analog to the SCR and requires the use of the SPICE2 built-in bipolar junction transistor model in order for the parameter estimation procedure to be valid.

Another inaccuracy in the "Hu-ki model" was noted but was not dealt with since correction would perturb the entire parameter estimation procedure for the model. That inaccuracy is the lack

of distinct delay time, t_d, and rise time, t_r, features in the turn-on transient simulation. Overall turn-on time corresponds well to actual devices specifications, therefore the inaccuracy is tolerated.

The "modified Hu-ki model" performs satisfactorily for SPICE2 simulation of AC resonant charging circuits for pulse power applications. Satisfactory performance was demonstrated by simulations showing the distinct activity of each SCR with respect to: dV/dt sensitivity in a two-loop application and correction by snubber circuit; uneven turn-on of two paralleled SCRs having slightly perturbed parameters; and uneven turn-off of two SCRs in series having slightly perturbed parameters.

The conclusions of this phase are that the "modified Hu-ki model" is an adequate design aid for SPICE2 CADA of SCR switched mode circuits. On the other hand it is exclusively a SPICE2 tool and thus does not fulfill the goal of a general purpose SCR model.

Chapters 5 through 7 present the second phase of this research task in which the "modified Hu-ki model" of the SCR is used as the basis for development of an SCR model for use with SCEPTRE.

SCEPTRE is a more general purpose CADA program than SPICE2 and offers a much greater non-linear analysis capability than SPICE2. This is particularly important in CADA application to non-linear magnetic effects such as core saturation. SPICE2 offers very limited capability to simulate such effects. On the other hand, power processing circuits are frequently designed to utilize such effects as part of their primary operating principles.

Having at hand the "modified Hu-ki model" of the SCR, the next logical step in progress towards a generalized SCR model was to convert the SPICE2 two-transistor SCR model into a two-transistor SCR model for use with SCEPTRE. In order to maintain the validity of the parameter estimation procedure of the "modified Hu-ki model", the SCEPTRE capability of accepting circuit element descriptions in terms of any mathematical formulation expressible in a Fortran statement was utilized. An equivalent SPICE2 model was constructed as input to SCEPTRE. The results were successful, but at a price of an order of magnitude increase in CPU time when tested in device turn-on transient simulation. This approach was abandoned. An alternative approach was taken. The two-transistor circuit analog was adapted from the SPICE2"terminal characteristics"bipolar junction transistor model to the SCEPTRE compatible "injection" configuration of the "modified Ebers-Moll" bipolar junction transistor model. Adaptation of the parameter estimation procedure was also accomplished.

This accomplishment improved computational efficiency over direct mathematical formulation by a factor of approximately 5 to 1. This improvement is credited to use of the SCEPTRE DIODE EQUATION, a built in capability for SCEPTRE computations involving PN junctions. Penalties were imposed by this approach to conversion from SPICE2 to SCEPTRE. Major penalties were the necessity to specially formulate junction reverse breakdown capabilities and non-linear capacitance expressions, the inclusion of additional capacitance

and resistance terms to meet SCEPTRE programming requirements, and the obtaining of an imposingly large equivalent network for the two-transistor configuration of the model. The latter of these proved to be prohibitively large when attempting SCEPTRE simulation of circuits having more than a few SCRs. This being due to SCEPTREs 300 element 301 node circuit size limitation.

The problem of circuit size was dealt with by operating the model through various transients over a wide dynamic range of currents and voltages. Elements inherent to the two-transistor configuration but which were observed to contribute little to model performance were removed. Also, all like elements (i.e. capacitors, resistors, diodes, current sources) placed in parallel in the network and associated with a common PN junction were lumped as single elements. This latter operation resulted in a network configuration very similar to that proposed by Nienhus as the "intrinsic" SCR model. The nomenclature, intrinsic, denotes the suggestion by the three diodes of the model of the intrinsic PNPN construction of the SCR.

The parameter estimation procedure was again revised to reflect changes to the model's circuit analog. To avoid confusion, the model was designated the "SCEPTRE 3-Junction SCR Model" or the "3-Junction Model".

Still another reduction in the model equivalent network was discovered by experimentation with SCEPTRE DIODE EQUATION arguments. It was discovered (although undocumented in SCEPTRE literature) that the arguments could be entered as variables through the DEFINED PARAMETER capability of SCEPTRE. Although reducing the network, this

approach sometimes required slightly more cpu time. The parameter estimation procedure was essentially unaltered through this network reduction. Nomenclature for this latter version of the model is the "Reduced 3-Junction SCR Model".

Both versions of the SCR model for SCEPTRE were tested via computer simulation of SCR operational characteristics of I_H, I_{GT}, t_{on}, V_T, V_{BO}, dV/dt, and t_q. A summary table of results is given in Chapter 5, but extensive data documentation is given in reference [39]. The results were considered adequate, but dV/dt and t_q performance was questionable. Some iterative searching for the right parameters to obtain simulation of these parameters was required. The cause for this is primarily related to two factors. First, the adaptation of the "modified Hu-ki model" to SCEPTRE required the addition of a capacitor across the gate to cathode junction to meet programming constraints. Second, the original "Hu-ki model" derived the method of obtaining parameters critical to t_q by an empirical process without analytical basis. The successive alterations of the model disturbed the model operation sufficiently so as to degenerate the accuracy of the parameter estimate.

The model was used to do simulation of a 3Ø AC resonant charging system and a DC resonant charging system obtaining DC from a 3Ø controlled rectifier. These simulations revealed the model to be an adequate tool for SCEPTRE simulation of SCR switching mode circuits.

Chapters 8 and 9 present the third phase of the research. Drawing from the experience in phases one and two, a generalized SCR model denoted the J^3 SCR model is developed.

A great deal was said in summary paragraphs dealing with phase two research to bring to light problems with evolving an existing model into a generalized SCR model. Two things stand out, however, as a result of the work in phases one and two. First of these is that the three diode (i.e. intrinsic) circuit analog to the SCR is preferred as a uniform model since it has a smaller element count suitable to programs with restricted network size and since it is representable in SPICE2, SCEPTRE, and other programs having PN junction non-linearity simulation capability.

Second is that a parameter estimation procedure from manufacturers specification data is feasible.

Although two adequate SCR models were developed at this point, one for SPICE2 and one for SCEPTRE, neither model was judged suitable to fulfilling the objectives of this thesis. To meet those objectives, a fundamental development task was undertaken to incorporate the experiences of phases one and two into a "from ground up" derivation of a more acceptable culmination of the dissertation objectives.

The J^3 SCR Model, a non-linear circuit anolog to the SCR for which a "user friendly" analytical parameter estimation procedure requiring only manufacturer's specification sheet data has been developed in this dissertation.

Two quite different SCR models, one being Nienhus' Model[2] built around the intrinsic three-junction SCR structure and developed for SCEPTRE, the other being Hu's Model[12] employing the two-transistor SCR anolog and developed for SPICE2 have provided cornerstones for this unified SCR model, the J^3 Model, applicable to both SPICE2 and SCEPTRE.

While incorporating the intrinsic three-junction structure of Nienhus' model for a circuit anolog and applying the principle established by Hu of parameter estimation from spec sheet data, the J^3 SCR Model is otherwise a unique SCR model in its own right. The network anolog is simplified with respect to Nienhus's model, however, the parameter estimation procedure is more complex than that proposed by Hu. This latter being the penalty of improved accuracy in simulating SCR switching dynamics.

The major features of the J^3 SCR Model are that it:

- Is a high power SCR model, emphasizing reasonably accurate computer simulation of the three major SCR dynamics, gate-pulse turn-on, dV/dt, and t_q.
- Uses the principle although not the procedure of parameter estimation from specification sheet data as developed by Hu.
- Has a small equivalent network based on the Nienhus intrinsic three junction structure of an SCR thus allowing SCEPTRE simulation of several SCR's in a network.
- Has small number of non-linearities to optimize computational efficiency.

- Is developed by analysis of the model network dynamic equations and semi-conductor physical properties to define model parameters.
- Provides reasonably accurate simulation of the secondary SCR characteristics of I_{GT}, I_H, V_{on}, $V_{(BO)}$, $V_{(BR)R}$, and V_{GRM}.
- Is user oriented, analytically determined, and suitable for expansion or alteration to simulate advancing or alternative technology.
- May be used with any non-linear circuit analysis program capable of handling exponential non-linearities.
- Is a useful SCR model for simulation of inverter SCR's where turn-off is a critical parameter.
- May be used with both amplifying gate and non-amplifying gate SCR structures.

Model performance has been tested by computer simulation in all the above listed preformance categories using both SPICE2 and SCEPTRE. Simulation results are consistent with manufacturer's specifications for the GE C602 LM, a phase control SCR, and the GE 185N, an inverter SCR. These devices were chosen to verify the model since they represent opposites in the SCR spectrum in terms of construction and application.

The utility of the J^3 SCR Model to the circuit designer is demonstrated through simulation of the "Schwartz" series resonant inverter. This state of the art power processing circuit is

currently receiving close attention for its potential application to high power DC to DC converters. Simulation results demonstrate the J^3 SCR Model to be a useful design aid to analyze this circuit in which dV/dt and commutation are crucial device performances.

It is the conclusion that the objectives of this research task have been successfully achieved.

BIBLIOGRAPHY

[1] Waiman, F., Ki, "A SPICE Model for the SCR", Master Thesis, Department of Electrical and Computer Science, University of California-Berkeley, Dec. 1979.

[2] Nienhus, H. A., J. C. Bowers, and M. S. Ziemacki, "A Computer Model for a High Power SCR", Final Report, AFAPL-TR-75-106, Dec. 1975.

[3] Sayle, W. E., "Silicon Controlled Rectifier Large Signal Model", Report No. AFAPL-TR-75-89, Oct. 1975.

[4] Nagel, W. W., "SPICE2: A Computer Program to Simulate Semiconductor Circuits", Electronic Research Laboratory, College of Engineering, University of California, Berkeley, CA, Memo No. ERL-M520.

[5] Bowers, James, et al., "A Survey of Computer Aided-Design and Analysis Programs", Technical Report, AFAPL-TR-76-33, USAF Aero Propulsion Laboratory, AFAPL/POD, Wright-Patterson Air Force Base, Ohio, April 1976.

[6] Bowers, James C. and Stephen R. Sedore, "SCEPTRE: A Computer Program for Circuit and Systems Analysis, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1971.

[7] Bowers, James C., et al., "User's Manual for SUPER-SCEPTRE", Final Report on Contract No. DAAA-21-73-C-0655, Fuse Development and Engineering Division, Picatinny Arsenal, Dover, New Jersey, May 1975.

[8] Nienhus, H. A., and J. C. Bowers, "A General Purpose Computer Model for a High Power SCR", Technical Report AFAPL-TR-76-82, USAF Aero Propulsion Laboratory, AFAPL/POD, Wright-Patterson Air Base.

[9] Dougherty, M., "A Series Resonant Inverter Simulation using SUPER-SCEPTRE", Proceedings of the IEEE 1979 National Aerospace and Electronics Conference, NAECON 1979.

[10] Getreu, I. E., "Modeling the Bipolar Transistor", Elsevier Scientific Publishing Company, New York, 1978.

[11] Maggetto, Gaston, "Le Thyristor: Definitions, Protections, Commands", Presses Universitaires de Bruxelles, Avenue Paul Higer 42, 1050, Bruxelles, 1971.

[12] Hu, C. and W. F. Ki, "Toward a Practical Computer Aid for Thyristor Circuit Design", IEEE Power Electronics Specialists Conference, 1980.

[13] Lee, F. C., D. Y. Chen, R. L. Avant, and R. Ramanathan, Report on Phase I of the Dynamic Simulation of Airborne High Power Systems", Elec. Eng. Dept., VPI&SU, Sept. 18, 1980.

[14] Blicher, Adolf, Thyristor Physics", Springer-Verlag, New York, 1976.

[15] Silva, Jaime R., "Prime Power to Pulse Conditioning Interface Methods", Thesis for M.S.E.E., Dec. 1980, Airforce Institute of Technology, WPAFB, Dayton, Ohio.

[16] Becker, David, "Extended Sceptre, Volume I", NTIS Publication AD/A-009 594, Dec. 1974.

[17] Sedore, Stephen R., "Sceptre Support II, Volume I: Revised Users Manual", NTIS Publication AD-882 384, July 1970.

[18] Sedore, Stephen R., "Sceptre Support II, Revised Mathematical Formulation", NTIS Publication AD-882 385.

[19] Becker, David, "Extend Sceptre Volume II - Mathematical formulation", NTIS Publication AD-A009 595, Dec. 1974.

[20] Sedore, Stephen R., "Sceptre Support II, Volume I: Revised User's Manual (supplement)", NTIS Publication AD-751 518, Sept. 1972.

[21] Temple, V.A.K., F. W. Holroyd, M. S. Adler, P. V. Gray, "The Effect of Carrier Lifetime Profile on Turn-off Time and Turn-off Losses", IEEE PESC '80 Record.

[22] G. E. SCR Manual, 6th Edition, 1979.

[23] Avant, R. L., F. C. Lee and D. Y. Chen, "A Practical SCR Model for Computer Aided Analysis of AC Resonant Charging Circuits", Proceedings, IEEE Power Electronics Specialists Conference, 1981.

[24] Avant, R. L., R. Ramanathan, and F. C. Lee, "Computer Simulation of DC and AC Resonant Charging Circuits for Pulse Power Applications", PCI/MOTORCON March 1982 Conference Record.

[25] Stephenson, R. E., "Computer Simulation for Engineers", Harcourt Brace, Javonovich, Inc., New York, 1971.

[26] Collilla, A. M., M. J. O'Sullivan, D. J. Carlino, "Systems Simulation", Lexington Books, D.C. Heath and Company, Lexington, MA, 1974.

[27] "Subsystem Design Analysis Lightweight Alternator" (Model Test Program). Final Report, March 1977, AFWL-TR-75-66, Add 2.

[28] Bowers, J. C., "Circuit and System Analysis Programs", PCI '82 Proceedings, p. 69, Mosconie Center, San Francisco, March 1982.

[29] SCR Designers Handbook, Westinghouse, Sept. 1970.

[30] GE C602 LM and GE C185N Data Sheets from G. E. Semiconductor Data Handbook, 3rd Edition, 1977.

[31] SCR Applications Handbook, International Rectifier, 1977.

[32] Sze, S. M., "Physica of Semiconductor Devices", 2nd Edition, Wiley-Interscience, New York, 1981.

[33] van der Ziel, Albert, "Solid State Physical Electronics", 3rd Edition, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1976.

[34] Temple, V. A. K., "The Effect of Carrier Lifetime Profile on Turn-off Time and Turn-off Losses", IEEE PESC 1980 Record, p. 155.

[35] Chua, L. O., and Sing. Y. W., "A Non-linear Lumped Circuit Model for SCR", Memorandum No. UCB/ERL M78/41, 26 June 1978.

[36] Data Sheet for International Rectifier 2N690 SCR, D.S. #PD-3.010.

[37] Equipment list for parameter characterization and time estimate for device characterization procedure as per Dr. J. Bowers, July 1982.

[38] Cohen, E., "Program Reference for SPICE2", ERL-M592, 14 June 1976.

[39] Avant, R. L., Lee, F. C., "Dynamic Simulation of Airborne High Power Systems", Final report on contract #F 33615-79C-2047, AFAPL, Wright Patterson AFB, 1982.

[40] Schwarz, F. C., "An Improved Method of Resonant Current Pulse Modulation for Power Converters", IEEE PESC Record, 1975, p. 194.

[41] Schwarz, F. C., Klaaseus, J. B., "A Controllable Secondary Multikilowatt DC Current Source With Maximum Power Factor In Its Three Phase Supply Line", IEEE PESC Record, 1975, p. 205.

[42] Schwarz, F. C., "A 95 Percent Efficient 1 KW DC Converter With an Internal Frequency of 50 KHz", IEEE PESC Record, 1977, p. 125.

[43] Rosenberg, S. A., Dewan, S. B., "Analysis Technique for a Clamped Inverter for Induction Heating," IEEE PESC Record, 1976, p. 73.

[44] Yu, Y., Biess, J. J., Schoenfeld, A. D., "The Application of Standardized Control and Interface Circuits to Three DC-DC Power Converters", IEEE PESC Record, 1973, p. 237.

[45] King, R. J., Stuart, T. A., "Modeling the Full-Bridge Series-Resonant Power Converter", IEEE Transactions on AES, Vol. AES-18, No. 4, July 1982.

[46] Vorperian, V., Cuk, S., "A Complete DC Analyses of the Series Resonant Converter", IEEE PESC Record, 1982, p. 85.

[47] "Westinghouse SCR Designers Handbook", 2nd Edition, 1970.

[48] "General Electric SCR Manual", 5th Edition, 1972.

[49] "International Rectifier SCR Applications Handbook", 1977.

[50] "International Rectifier HEXFET Databook", 1981.

[51] BJT Power Transistor Data Sheets and Applications Notes for Fuji, Westinghouse, General Electric, and Solition Transistors.

[52] Chambers, D., "Designing High Power SCR Resonant Converters for Very High Frequency Operation", Proceedings of Powercon, 9 July 1982, Washington, D.C.

[53] Bedford, B. D., Hoft, R. G., "Principles of Inverter Circuits", John Wiley and Sons, Inc., New York, copyright 1964.

[54] Dewan, S. B., Straughen, A., "Power Semiconductor Circuits", copyright 1975, John Wiley and Sons, Inc., New York.

[55] Kaplan, W., "Operational Methods for Linear Systems", Addison-Wesley Publishing Company, Inc., Reading, Mass., 1962.

[56] Churchhill, R. V., "Operational Mathematics", McGraw-Hill, Inc., New York, New York, 1958.

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A CAPABILITY
FOR CONTINUOUS TOPOLOGY TRANSIENT ANALYSIS
IN SCR SWITCHING-MODE POWER SUPPLIES

by

Roger L. Avant

(ABSTRACT)

A general purpose computer model for the SCR is developed. The model, consisting of both a circuit analog and parameter estimation procedure, is uniformly applicable to popular computer aided design and analysis programs such as SPICE2 and SCEPTRE. The circuit analog is based on the intrinsic three PN junction structure of the SCR and is similar to Nienhus' model. The parameter estimation procedure requires only manufacturer's specification sheet quantities as a data base. It employs some of the concepts developed by Hu for a SPICE2 SCR model.

This uniform model, denoted the J^3 SCR model, is shown to be a useful design aid through computer simulation of fault transients which may occur in a "Schwarz" converter. The transients simulated would not be observable without use of a highly accurate continuous topology non-linear SCR model such as is developed here.