HIGH-FREQUENCY QUASI-RESONANT CONVERTER TECHNIQUES

by

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(ABSTRACT)

Two waveform-shaping techniques to reduce or eliminate the switching stresses and switching losses in switching-mode power conversion circuits are developed: the zero-current switching technique and the zero-voltage switching technique.

Based on these two techniques two new families of quasi-resonant converters are derived. Since the stresses on semiconductor switching devices are significantly alleviated, these quasi-resonant (QRC) converters are suitable for high-frequency operations with much improved performances and equipment power density.

Employing the duality principle, the duality relationship between these two families of quasi-resonant converters are derived. The establishment of the duality relationship provides a framework allowing the knowledge obtained from one converter family to be readily transferred to the other.

Further topological refinements are derived through the utilization of parasitic elements in the devices and the circuit. In particular, the two most significant parasitic elements, the leakage inductance of the transformer and the junction capacitances of the semiconductor switch, are incorporated as part of the

resonant-tank circuit required by these quasi-resonant converters. Consequently, the detrimental effects due to these parasitic elements are eliminated, and the converters can be operated at very high frequencies.

Acknowledgements

I would like to express my sincere appreciation to my advisor, Dr. Fred C. Lee, for his guidance, encouragement and support. His extensive knowledge and creative thinking have been an invaluable help to this research work.

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1. INTRODUCTION

In most solid-state power processing circuits, efficiency is of paramount importance. To achieve high efficiency, it is necessary to operate the power processing circuit in the switching mode in which the semiconductor devices are either completely turned on (into the saturation state) or completely turned off (into the cut-off state).

In order to achieve the desired power conversion, output voltage regulation, dc isolation, and noise suppression without sacrificing efficiency, the design of power processing circuits must rely on extensive use of magnetic components (inductors and transformers) and capacitors. Consequently, the use of inductive and capacitive elements in the power processing circuits creates extraneous burden on the power semiconductor devices.

In designing power processing circuits, there is an ever increasing demand to increase the switching frequency in order to reduce the weight and size of magnetic and capacitor components and to improve the dynamic performance of the

circuit. The demand for high power density and high performance is especially critical for the power supply circuits to be used in the computer and telecommunication equipment as well as military and aerospace applications. Due to the increasing demand of high-frequency operation and switching under harsh conditions, power semiconductor devices face two major difficulties: switching losses and switching stresses.

As the power semiconductor technology is rapidly evolving, many power devices are made available for power processing applications. Each type of power semiconductor device has its special merits and limitations. For example, the minority-carrier devices such as SCR, GTO (Gate Turn-Off thyristor) and power BJT (Bipolar Junction Transistor), have high power handling capability (higher voltage and current ratings), but are limited in switching capability. SCR devices have no turn-off capability and rely on external commutation schemes. GTO devices can turn off under a loaded condition, but require a significant amount of reverse gate current. Power BJT devices can switch faster, nonetheless they suffer from long storage time and switching loss due to the minority-carrier recombination.

The majority-carrier devices, such as the power MOSFET, have ultra-high switching speed and are ideal for high-frequency, low-power applications. Its turn-off time is very short due to the absence of carrier-recombination phenomena. Consequently, the turn-off switching loss is small. However, like all other power semiconductor devices, the MOSFET has parasitic junction capacitances.

When operated at very high frequency, the turn-on switching loss due to the discharging of junction capacitances can be a limiting factor.

Against the different switching capabilities and limitations of the minority-carrier and the majority-carrier devices, different switching-aid schemes must be implemented to improve their switching behavior. For the minority-carrier devices, the major concern is their poor turn-off behavior due to the limited turn-off capability or slower turn-off speed. Normally, some means of switching-aid is necessary, such as commutation circuits or large reverse drives. While the turn-off behavior can be improved using external circuitry, it also suffers from one or more of the following deficiencies: increased circuit complexity, increased voltage or current spikes, increased switching loss, and additionally imposed limitations on the circuit's switching frequency or its load range [A1-A23].

On the other hand, the MOSFET devices, because of their fast switching speed but limited voltage and current capability, are mostly used in lower power, higher frequency applications. The switching loss due to the turn-on discharging of the junction capacitance ($\frac{1}{2}CV^2f$) is a major concern, especially at very high switching frequencies (in the megahertz range).

To improve the switching behavior of the semiconductor devices in switching-mode, power processing circuits, two general techniques are proposed. The first is the **zero-current switching** (ZCS) technique [B8-B11]. By incorporating an LC resonant circuit, the current waveform of the switching device is forced to oscillate in a quasi-sinusoidal manner, therefore, creating zero-current switching conditions during both turn-on and turn-off instances.

The fundamental characteristics of the zero-current switching technique and the basic structure of zero-current switching circuits are described in Chapter 2.

The second is the **zero-voltage switching** (ZVS) technique [C15]. By using an LC resonant network, the voltage waveform of the switching device can be shaped into a quasi-sinewave. Consequently, a zero-voltage condition is created for the switch to turn on and turn off without incurring any switching loss.

The fundamental characteristics of the zero-voltage switching technique and the basic structure of the zero-voltage switching circuit are treated in Chapter 3.

Through the establishment of the zero-current switching technique and the proposed basic circuit structures, a large family of ZCS, quasi-resonant converters have been derived. Similarly, the zero-voltage switching technique has led to the discovery of a large family of ZVS, quasi-resonant converters.

In Chapter 4, topological variations of quasi-resonant converters are treated in detail. First, the basic PWM converter topologies are identified through the establishment of circuit constraints on converter topologies. From these basic converter circuits, many other PWM converter circuits can be derived systematically through certain topological variation and synthesis methods. Finally, by applying proper replacement of power switches in these PWM converter topologies by resonant switches, a large variety of quasi-resonant converter topologies can be generated. Furthermore, the duality relationship which exists between the zero-current switching and the zero-voltage switching techniques is highlighted after a brief review of the dual network theories and the duality principle.

In high-frequency operation, circuit parasitics, such as the leakage inductance of the transformer and the junction capacitance of the semiconductor switches, can cause severe detrimental effects to the circuits: slower response due to the parasitic elements, higher switching stress and switching loss, higher switching noise and EMI, etc. Since there is a limit to which the parasitic elements can be reduced, a viable alternative is to incorporate these parasitic elements as resonant tank elements required by the zero-current or zero-voltage switching circuit operation. Several quasi-resonant converter topologies which utilize parasitic elements are presented in Chapter 5.

2. ZERO-CURRENT SWITCHING TECHNIQUE

2.1. Historical Background

Historically, resonant converters were introduced prior to other topologies using the concept of zero-current switching. Common to all resonant converters is an LC tank circuit, which is excited repetitively by an ac power source. Output power can be tapped either from the tank's inductor current (the **Series Resonant Converter, SRC,** see Fig. 2.1) or from the tank's capacitor voltage (the **Parallel Resonant Converter, PRC,** see Fig. 2.2) [D1-D30].

The main advantage of these resonant converters is that the semiconductor switches can be naturally commutated using the sinusoidal current waveforms generated by an LC tank circuit. This zero-current switching property greatly improves the turn-off behavior of the switches, especially the minority-carrier devices. For instance, natural commutation allows SCRs to be used in high-power converter circuits without resorting to cumbersome external commutation circuits. Turn-off under zero-current conditions also reduces the amount of reverse base (or gate) current needed for BJT and GTO devices and, thus, greatly reduces switching stresses and switching losses.

For circuit simplicity and ease of control, single-ended, resonant converter topologies are desirable as are the bridge-type resonant converters (such as the SRC and the PRC). Several single-ended, resonant converter topologies have been proposed in recent years [B1-B6]. However, only a few topological circuit structures have been uncovered, and very little information on the fundamental circuit behavior has been reported in literature.

The research work associated with this dissertation discovered that the concept of the **resonant switch** leads to a unified approach of deriving a large family of single-ended, **quasi-resonant converter** topologies possessing the zero-current switching property. This new family of converters can be viewed as a hybrid of PWM and resonant converters. However, they differ from the PWM converters in that there is a resonant tank circuit present near the power switch, and the power switch has a quasi-sinusoidal current or voltage waveform. On the other hand, they differ from the conventional resonant converters in that the waveform

of the resonant capacitor voltage or the resonant inductor current is not interrupted; whereas in resonant converters, the waveform is interrupted by the turn-on's or turn-off's of power switches. Consequently, this class of converter topologies is referred to here as the class of Quasi-Resonant Converters (QRCs) in order to distinguish them from the class of PWM converters and the class of resonant converters.

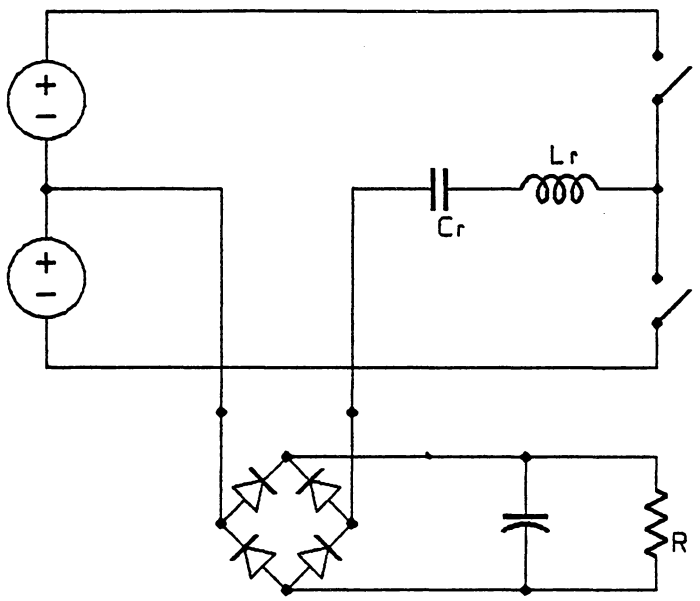


Fig. 2.1. The series resonant converter

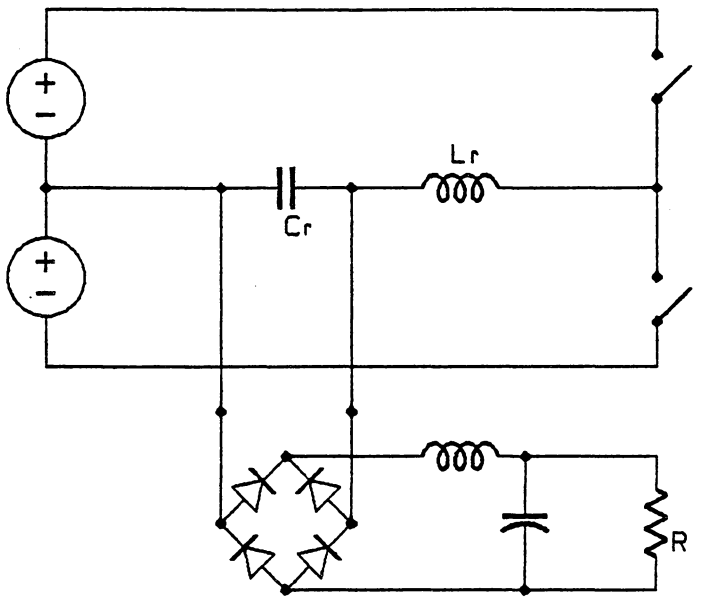


Fig. 2.2. The parallel resonant converter

2.2. *Current-Mode Resonant Switches*

The concept of the resonant switch was conceived through the following observation.

When energy is injected into an LC tank circuit, it is exchanged between the inductor and the capacitor in a periodical, sinusoidal fashion. Because of its ability to sustain a sinusoidal oscillation, an LC tank circuit can be used as a lossless (or low-loss) waveform-shaping device.

By employing an LC tank circuit to shape the current or voltage waveform of the switching device in a converter circuit, a favorable condition is created for the switching device to turn on or off. It should be pointed out that the proposed LC resonant network differs from LC networks often used as lossless snubber circuits. The former not only is employed to shape the current and voltage waveforms, it also serves as an intermediate energy storage and transfer subcircuit. Each of the two state variables of the resonant tank circuit, the inductor current and the capacitor voltage, in fact, can be used in shaping of switch's waveform. When current-waveform shaping is desired, the inductor of the resonant tank is connected in series with the switching device. The resulting composite subcircuits consisting of semiconductor switch S_1 , inductor L_r, and capacitor C_r, as shown in Fig. 2.3, are referred to as the **current-mode resonant switches.** There are two types of current-mode resonant switch configurations: the L-type and the M-type, as shown in Fig. 2.3a. In both cases, L_r is connected in series

with S_1 , and C_r is connected in parallel with S_1-L_r. L_r and C_r constitute a series-resonant circuit whose resonance occurs during the major portion of the on-time.

If the ideal switch, S_1, is implemented in a uni-directional configuration, as shown in Fig. 2.3b, the resonant switch is confined to operate in a half-wave mode. If diode D_1 is connected in anti-parallel with Q_1, as shown in Fig. 2.3c, then the resonant switch operates in a full-wave mode and the switch current can flow bi-directionally.

In essence, the LC tank circuit is used to shape the current waveform through switch S_1. At turn-on, the device voltage, (V_{ce} or V_{ds}), can be driven into saturation before the current gradually rises in a quasi-sinusoidal fashion. Because of the resonance between L_r and C_r , current through S_1 tends to oscillate to a negative value, thus, allowing S_1 to be naturally commutated.

The effect of the resonant switch on the reduction of switching stress and switching loss can be seen from the load-line trajectories. Path A in Fig. 2.4 shows a typical load-line trajectory for inductive switching with conventional forced turn-off. The path traverses through a high-stress region where the switch is subjected to high voltage and high current simultaneously. Whereas, the load-line trajectory for inductive switching with a resonant switch moves mostly along either the voltage axis or the current axis, as shown by path B. Consequently, the switching stresses and losses are greatly reduced.

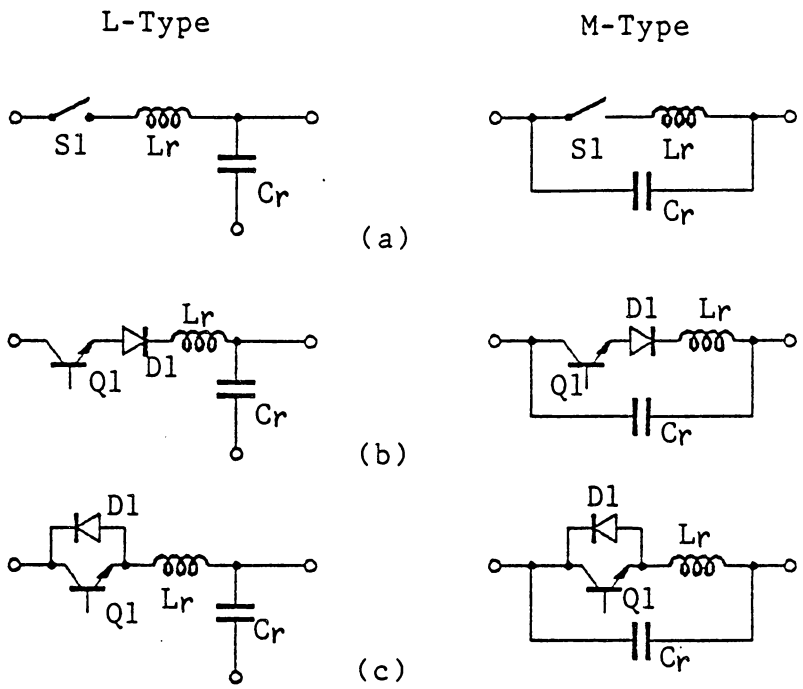


Fig. 2.3. The configurations of current-mode resonant switches
(a) general topologies
(b) half-wave configuration
(c) full-wave configuration

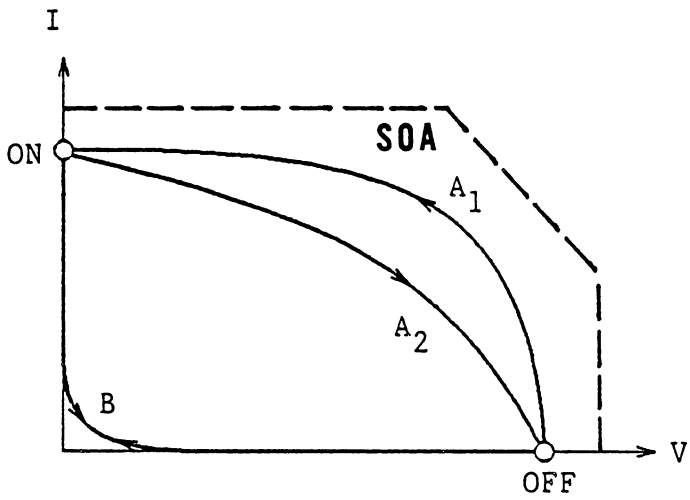


Fig. 2.4. Load-line trajectories
(A) conventional inductive load switching
(B) resonant switching

2.3. *Principles of Operation*

A conventional buck converter is shown in Fig. 2.5a. When switch S_1 is replaced by a current-mode resonant switch, S_1-L_r-C_r , a ZCS, quasi-resonant buck converter is formed, as shown in Fig. 2.5b. To analyze its steady-state circuit behavior, the following assumptions are made:

- L_o is much larger than L_r.

- Output filter L_o-C_o and the load are treated as a constant current sink, I_o .

- Semiconductor switches are ideal, i.e., no forward voltage drops in the on-state, no leakage currents in the off-state, and no time delays at both turn-on and turn-off.

- Reactive elements of the tank circuit are ideal.

The following variables are defined:

- Characteristic impedance $Z_n \equiv \sqrt{L_r/C_r}$

- Resonant angular frequency $\omega \equiv \dfrac{1}{\sqrt{L_r C_r}}$

- Resonant frequency $f_n \equiv \frac{\omega}{2\pi}$

A switching cycle can be divided into four stages. The associated equivalent circuits for these four stages are shown in Fig. 2.6. Suppose that before S_1 turns on, diode D_o carries the steady-state output current, I_o, and capacitor voltage V_{Cr} is clamped at zero. At time T_0, S_1 turns on, starting a switching cycle:

(1). **Inductor-Charging Stage** $[T_0, T_1]$ (Fig. 2.6a)

Input current I_i rises linearly and its waveform is governed by the state equation:

$$L_r \frac{dI_i}{dt} = V_i \tag{2.1a}$$

The duration of this stage, $T_{01}(= T_1 - T_0)$, can be solved with boundary conditions of $I_i(0) = 0$ and $I_i(T_{01}) = I_o$, thus:

$$T_{01} = \frac{L_r I_o}{V_i} \tag{2.1b}$$

(2). **Resonant Stage** $[T_1, T_2]$ (Fig. 2.6b)

At time T_1, the input current rises to the level of I_o, D_o is commutated off and the difference between the input current and the output current, $I_i(t) - I_o$, flows into C_r, as seen from Fig. 2.6b. Voltage V_{Cr} rises in a sinusoidal fashion.

The state equations are:

$$C_r \frac{dV_{Cr}}{dt} = I_i(t) - I_o \tag{2.2a}$$

$$L_r \frac{dI_i}{dt} = V_i - V_{Cr}(t) \tag{2.2b}$$

with initial conditions of:

$$V_{Cr}(0) = 0; \quad \text{and} \quad I_i(0) = I_o \tag{2.2c}$$

Therefore,

$$I_i(t) = I_o + (\frac{V_i}{Z_n}) \sin \omega t \tag{2.2d}$$

$$V_{Cr}(t) = V_i(1 - \cos \omega t) \tag{2.2e}$$

If a half-wave resonant switch is used, switch Q_1 will be naturally commutated at time T_a when the resonating input current, I_i (t), reduces to zero, as shown in Fig. 2.7a. If a full-wave resonant switch is used, current I_i(t) will continue to oscillate and feed energy back to the voltage source, V_i, through diode D_1, as shown in Fig. 2.7b. Current through D_1 oscillates to zero again at time T_b. The duration of this stage, T_{12} ($= T_2 - T_1$), can be solved from Eq. (2.2d) by setting I_i (T_{12}) = 0 . Thus:

$$T_{12} = \frac{\alpha}{\omega}, \quad \text{where } \alpha = \sin^{-1}\left(\frac{-Z_n I_o}{V_i}\right) \tag{2.2f}$$

$\pi < \alpha < \frac{3\pi}{2}$; and $T_2 = T_a$ for the half-wave mode

$\frac{3\pi}{2} < \alpha < 2\pi$; and $T_2 = T_b$ for the full-wave mode

From Eq. (2.2e):

$$V_{Cr}(T_2) = V_i(1 - \cos\alpha) \tag{2.2g}$$

(3). **Capacitor-Discharging Stage** $[T_2, T_3]$ (Fig. 2.6c)

Since switch S_1 is off at time T_2, C_r begins to discharge through the output loop and V_{Cr} drops linearly to zero at time T_3, as shown in Figs. 2.7a and 2.7b. The state equation during this interval is:

$$C_r \frac{dV_{Cr}}{dt} = -I_o \tag{2.3a}$$

The duration of this stage, T_{23} ($= T_3 - T_2$) , can be solved with the initial condition $V_{Cr}(0) = V_i(1 - \cos\alpha)$:

$$T_{23} = \frac{C_r V_i (1 - \cos\alpha)}{I_o} \tag{2.3b}$$

(4). **Free-Wheeling Stage** [T_3, T_4] (Fig. 2.6d)

After T_3 , output current flows through diode D_o. The duration of this stage is T_{34} ($= T_4 - T_3$), and

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{2.4}$$

where T_s is the period of a switching cycle.

Typical circuit waveforms, as shown in Figs. 2.7a and 2.7b, clearly demonstrate the zero-current switching property.

Notice that if C_r is connected between V_i and L_o, instead of in parallel with D_o, an M-type resonant switch is formed (Fig. 2.5c). Close examination of this circuit reveals it is functionally equivalent to the circuit of Fig. 2.5b.

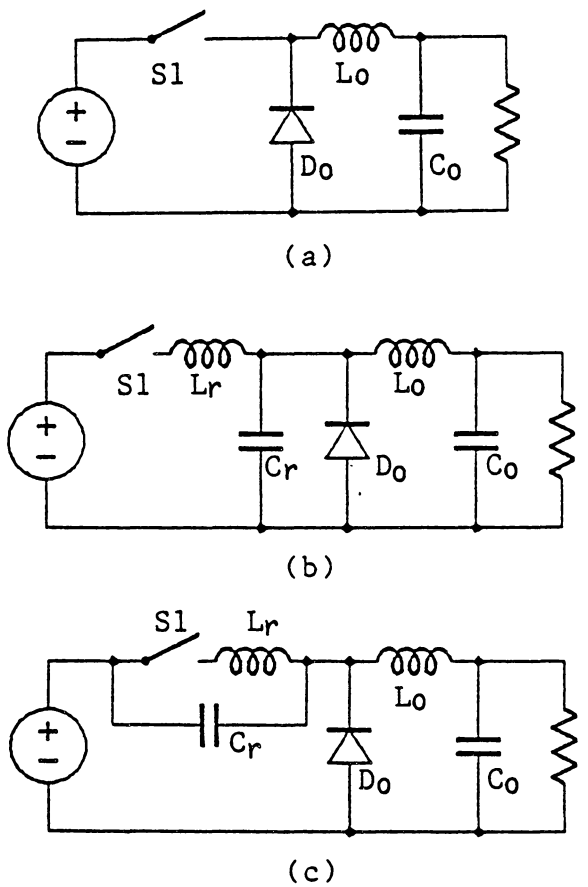


Fig. 2.5. The buck converter
(a) conventional
(b) with an L-type resonant switch
(c) with an M-type resonant switch

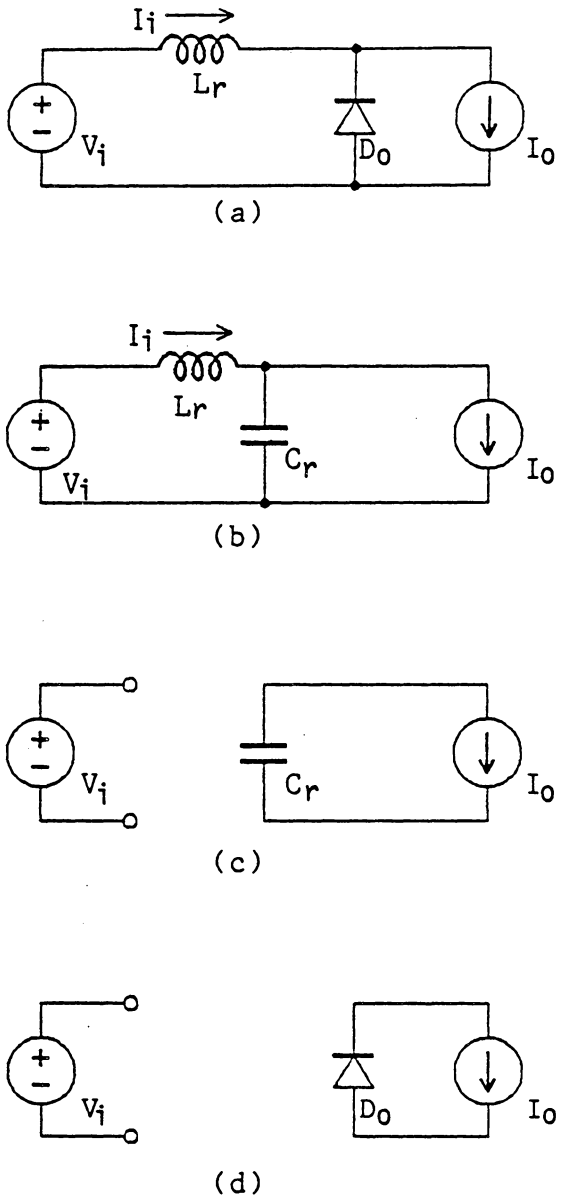
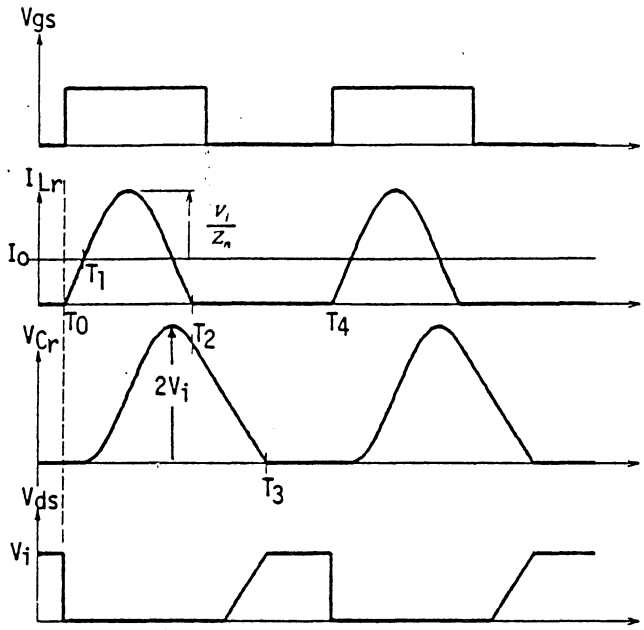
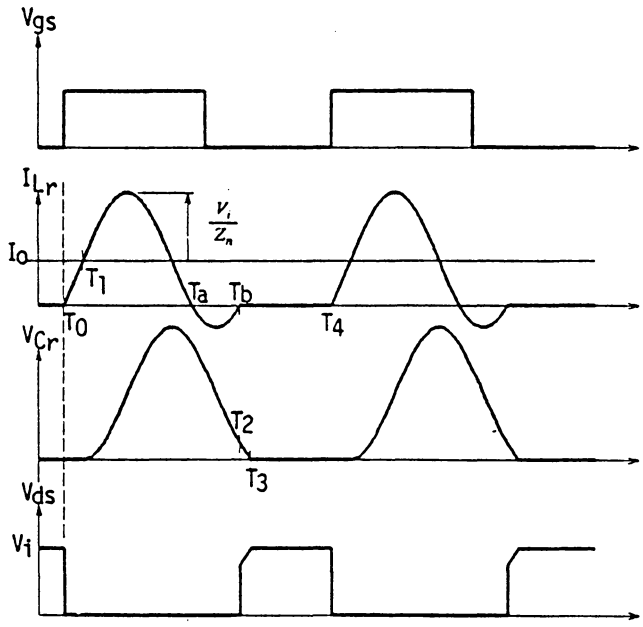


Fig. 2.6. Equivalent circuits of the ZCS, quasi-resonant buck converter during the four stages in a switching cycle (a) [T0, T1] (b) [T1, T2] (c) [T2, T3] (d) [T3, T4]



(a)



(b)

Fig. 2.7. Waveforms of the ZCS, quasi-resonant buck converter
(a) half-wave mode
(b) full-wave mode

2.4. *Zero-Current Switching, Quasi-Resonant Converters*

The concept of the resonant switch can be directly applied to a large number of conventional PWM switching converters. Simply by replacing the switch in a conventional PWM switching converter by a current-mode resonant switch, a new, ZCS, quasi-resonant converter topology is derived. Some basic converter topologies and their counterparts with resonant switches are presented in Fig. 2.8.

For a given ZCS, quasi-resonant converter, the topology using an L-type resonant switch and the topology using an M-type resonant switch have the same set of state equations. Therefore, they have the same circuit operations. The only difference is that the voltage excursion on the resonant capacitors are different. One topology may have a higher dc offset voltage across its resonant capacitor than the other topology has.

Other topological variations of ZCS, quasi-resonant converters also exist (see Sec. 4.4). A paper dedicated to this subject is Ref. [B12].

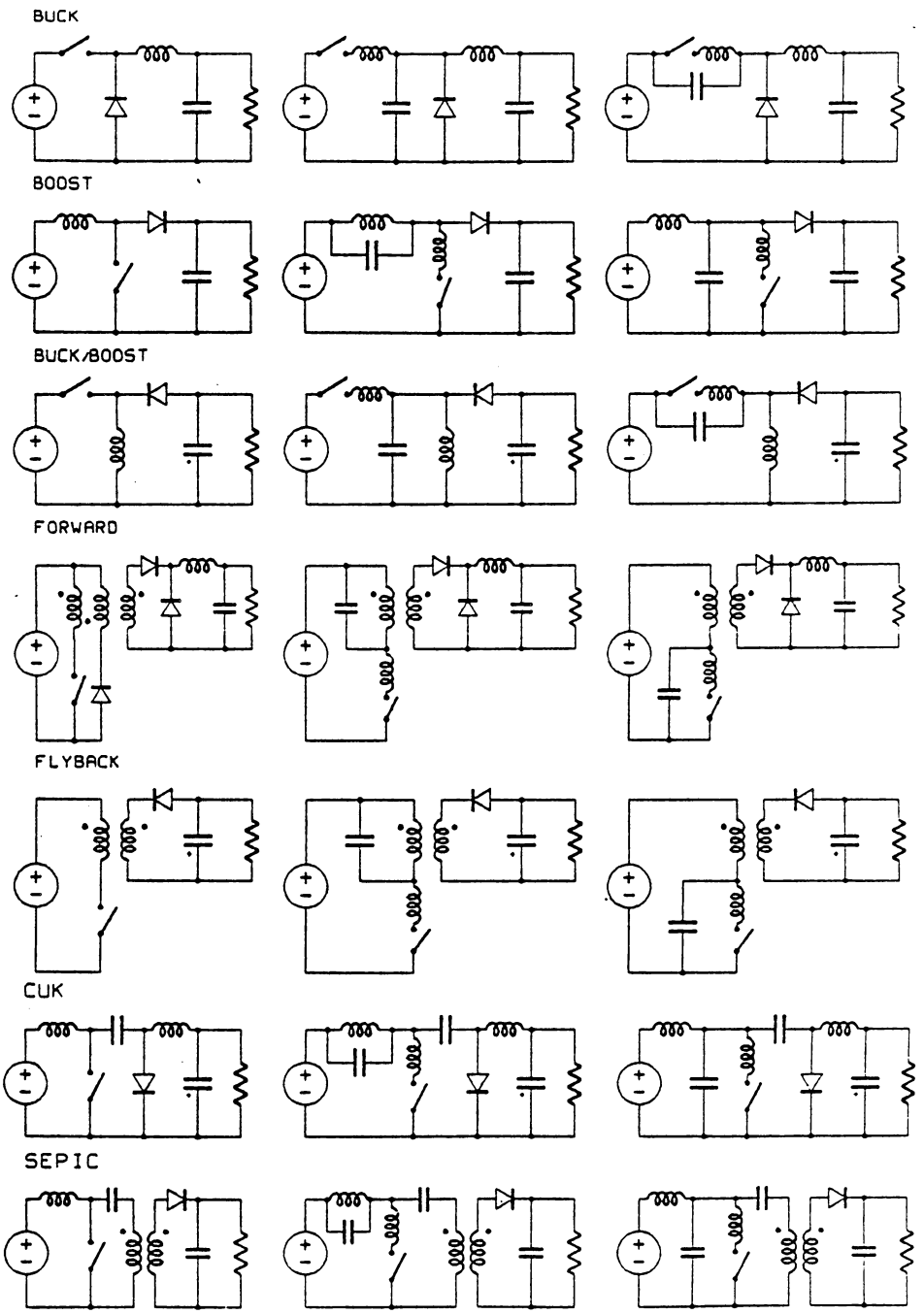


Fig. 2.8. A new family of ZCS,
quasi-resonant converters
(a) buck (b) boost (c) Buck/boost
(d) forward (e) flyback (f) Cuk (g) SEPIC

2.4.1. DC Voltage-Conversion Ratio of the ZCS, Quasi-Resonant Buck Converter

Output voltage V_o of the ZCS, quasi-resonant buck converter can be solved by equating input energy per cycle, E_i , and output energy per cycle, E_o. Where

$$E_i = V_i \left[\int_{T_0}^{T_1} I_i(t)\, dt + \int_{T_1}^{T_2} I_i(t)\, dt \right] \tag{2.5}$$

$$E_o = V_o I_o T_s \tag{2.6}$$

From Eqs. (2.1b), (2.2f), (2.2g), (2.3a) and (2.3b),

$$V_o = \frac{V_i}{T_s} \left(\frac{T_{01}}{2} + T_{12} + T_{23} \right) \tag{2.7}$$

Given the values of I_o and T_s , the values of T_{01}, T_{12}, and T_{23} can be solved from Eqs. (2.1b), (2.2a)-(2.2g), and (2.3b), and output voltage V_o can be solved from Eq. (2.7).

However, it is usually more desirable to solve the voltage-conversion ratio in terms of load resistance R and the switching frequency f_s . Since $V_o = RI_o$, Eq. (2.7) can be written as:

$$RI_o = \left(\frac{V_i}{T_s} \right) \left[\frac{L_r I_o}{2V_i} + \frac{\alpha}{\omega} + C_r V_i \frac{(1 - \cos \alpha)}{I_o} \right] \tag{2.8}$$

By defining $x \equiv \frac{V_o}{V_i}$ and $r \equiv \frac{R}{Z_n}$, Eq. (2.8) becomes:

$$x - (\frac{1}{2\pi})(\frac{f_s}{f_n})\,[\,(\frac{x}{2r}) + \sin^{-1}(\frac{-x}{r})$$

$$+ (\frac{r}{x})\,(1 + (sign)\sqrt{1 - (\frac{x}{r})^2}\,)\,] = 0 \qquad (2.9)$$

Define $\alpha \equiv \sin^{-1}(\frac{-x}{r})$, then

for the half-wave mode: $\pi < \alpha < 1.5\pi$; $sign = 1$

for the full-wave mode: $1.5\pi < \alpha < 2\pi$; $sign = -1$

Voltage-conversion ratios for the ZCS, quasi-resonant buck converter are plotted in Fig. 2.9a and Fig. 2.9b for the half-wave mode and full-wave mode, respectively. The voltage-conversion ratio in the half-wave mode is very sensitive to the load variation, while in the full-wave mode the voltage-conversion ratio is almost independent of the load variation.

A simple physical interpretation of the load insensitivity in the case of the full-wave mode is shown in the following. For the full-wave mode of operation, the waveforms of I_{Lr} ($= I_i$) and V_{Cr} under heavy load and light load conditions are shown in Fig. 2.10. When load resistance is small, the time interval for the inductor charging stage is longer and the inductor current is charged to a higher magnitude (equal to the load current). Consequently, the inductor current will oscillate to a higher magnitude during the first half-cycle of the resonant stage, and a lower magnitude during the second half-cycle. Therefore, under heavy load

condition, the energy returned from the tank circuit to the source is less. When the load resistance is increased, the initial inductor current for the resonant stage is smaller and a larger amount of energy is returned to the source, as shown in Fig. 2.10. It is intuitively obvious that the circuit is capable of regulating the output voltage against load variation without resorting to large variation of the switching frequency, while in the half-wave mode of operation, a packet of energy is transferred from the source to the tank when the switch is closed. If the load is light, it takes longer time to discharge the tank energy to the load. Therefore, the only means to regulate the output voltage is by varying the switching frequency.

The linear relation between the voltage-conversion ratio and the switching frequency for the full-wave mode of operation can also be derived mathematically in the following way. In general, the V_{Cr} waveform is very close to that of $V_i(1 - \cos \omega t)$ for a conduction angle of 2π which corresponds approximately to time interval $[T_1, T_3]$. The average value of voltage V_{Cr} during time interval T_{31} $(= T_3 - T_1)$ is approximately equal to V_i (see Fig. 2.11), and T_{31} is approximately equal to T_n ($T_n = 1/f_n$, where f_n is the resonant frequency). The voltage-conversion ratio can be derived simply by balancing the volt-seconds across inductor L_o as follows.

During T_{31} , the total value of the volt-seconds across L_o is $(V_i - V_o)T_n$. But for the linear stage $[T_0, T_1]$ and the free-wheeling stage $[T_3, T_4]$, the total value of the volt-seconds across L_o is $-V_o(T_s - T_n)$. By balancing these volt-seconds,

$$(V_i - V_o)T_n - V_o(T_s - T_n) = 0 \tag{2.10}$$

Rearranging Eq. (2.10),

$$\frac{V_o}{V_i} = \frac{T_n}{T_s} = \frac{f_s}{f_n} \tag{2.11}$$

This approximating method shows that the voltage-conversion ratio is independent of load resistance and is determined only by the normalized switching frequency, $\frac{f_s}{f_n}$. It is interesting to note that this characteristic is identical to that of the PWM converter if the control parameter $\frac{f_s}{f_n}$ is replaced by D ($= \frac{T_{on}}{T_s}$).

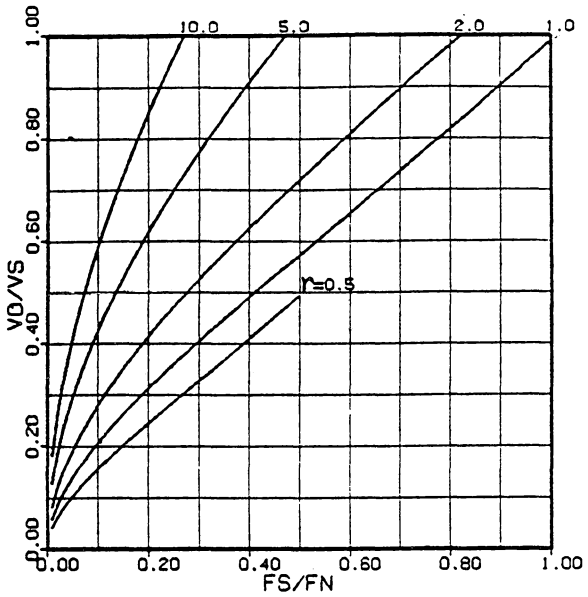
Alternatively, the approximate voltage-conversion ratio of Eq. (2.11) can also be derived from the exact expression, Eq. (2.9). By defining F(x/r) as:

$$F(\frac{x}{r}) = [\ (\frac{x}{2r}) + \sin^{-1}(\frac{-x}{r}) + (\frac{r}{x})(1 - \sqrt{1 - (\frac{x}{r})^2})\ ]$$

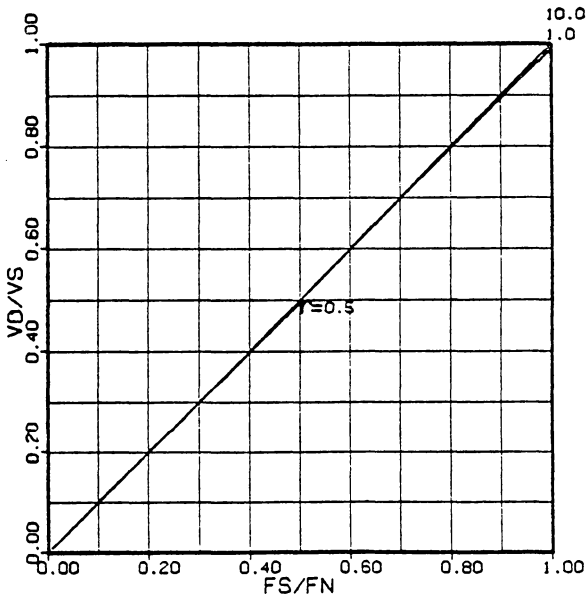
Equation (2.9) can be expressed as:

$$x - (\frac{1}{2\pi})(\frac{f_s}{f_n}) F(\frac{x}{r}) = 0$$

It is found that F(x/r) is very close to 2π for $0.0 <$ (x/r) < 0.99 (with a maximum error of less than 1.2%). If F(x/r) is substituted with 2π in the above equation, the same expression for the voltage-conversion ratio as that of Eq. (2.11) is obtained.



(a)



(b)

Fig. 2.9. DC voltage conversion ratio for the ZCS, quasi-resonant buck converter
(a) half-wave mode
(b) full-wave mode

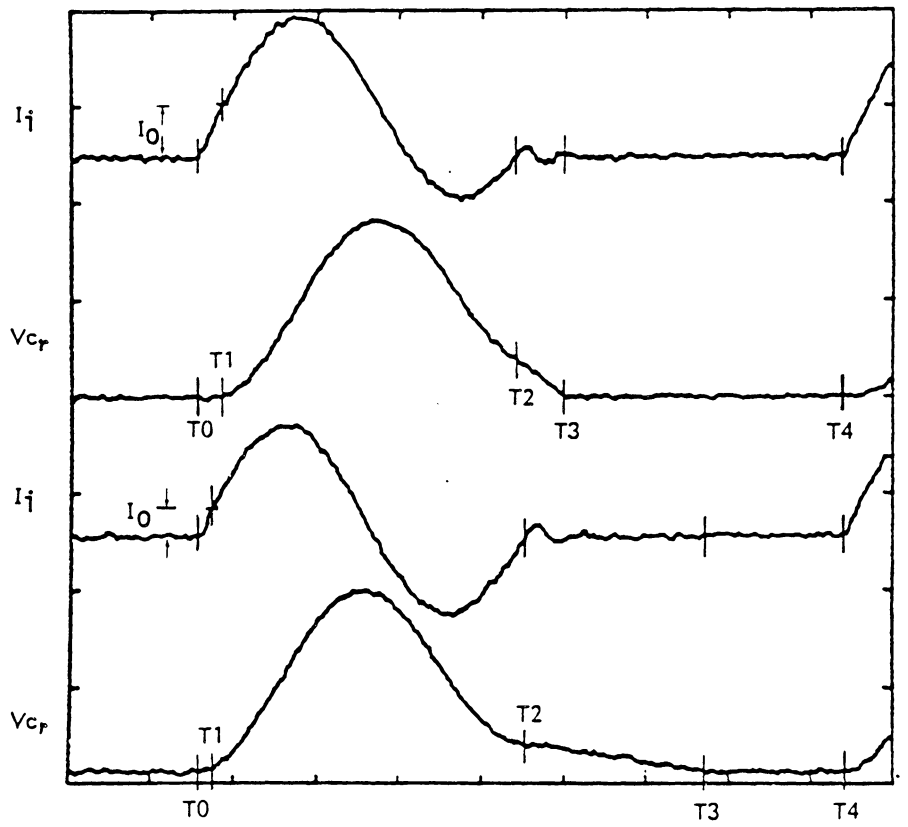


Fig. 2.10. Waveforms of the ZCS, quasi-resonant buck converter (oscillograms from an implemented circuit)
upper waveforms: heavy load
lower waveforms: light load

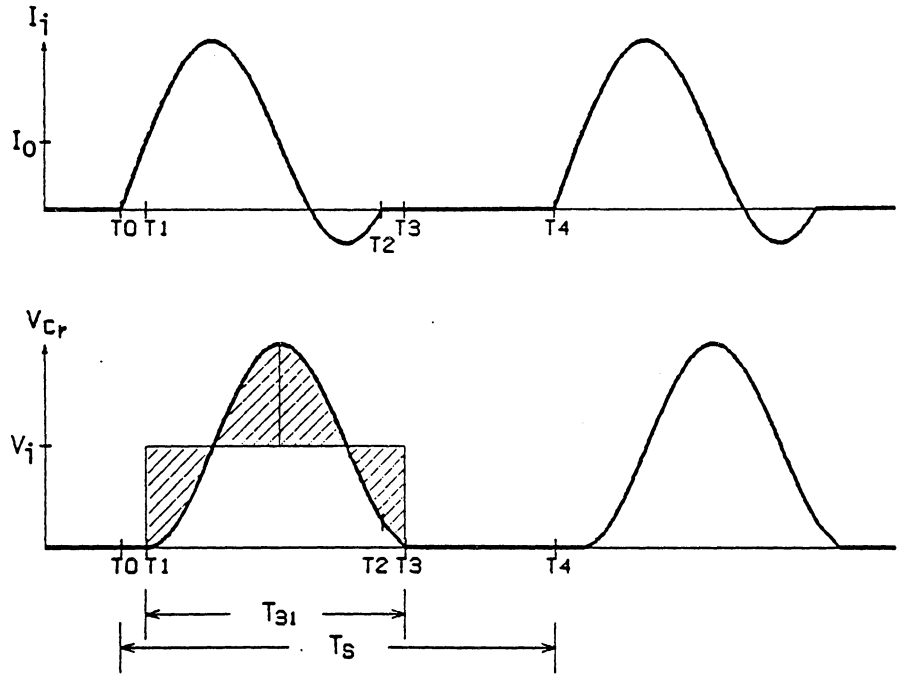


Fig. 2.11. Average value of capacitor voltage Vc

2.4.2. Multiple Conduction Cycles

The full-wave, resonant switch configuration, as shown in Fig. 2.3c, is capable of conducting multiple cycles (any even number of half-cycles) of current I_i during its on-time. The most general current-mode, resonant-switch configurations are shown in Fig. 2.12. Each configuration consists of two uni-directional switches in anti-parallel and can conduct any odd or even number of half-cycles during its on-time.

For the ZCS, quasi-resonant buck converter described above, Eq. (2.9) is still valid for determining the voltage-conversion ratio for multiple conduction cycles.

$$x - (\frac{1}{2\pi})(\frac{f_s}{f_n})\,[\,(\frac{x}{2r}) + \sin^{-1}(\frac{-x}{r})$$

$$+ (\frac{r}{x})\,(1 + (sign)\sqrt{1 - (\frac{x}{r})^2}\,)\,] = 0$$

Define $\alpha \equiv \sin^{-1}(\frac{-x}{r})$

then $3\pi < \alpha < 3.5\pi$ for the 1.5-cycle mode

$3.5\pi < \alpha < 4\pi$ for the 2.0-cycle mode

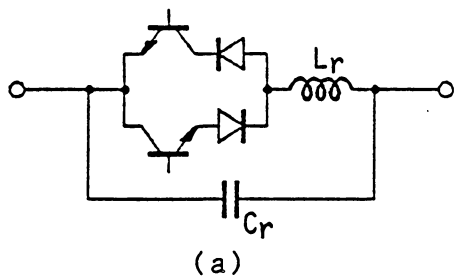
$5\pi < \alpha < 5.5\pi$ for the 2.5-cycle mode

etc.

sign = 1 for the 0.5, 1.5, 2.5 ...cycle modes

sign = -1 for the 1.0, 2.0, 3.0 ...cycle modes

Waveforms for the 1.5-cycle and 2.0-cycle modes of operation are shown in Fig. 2.13. The voltage-conversion ratios are plotted in Fig. 2.14. Notice that the voltage-conversion ratio of the 2.0-wave mode is twice that of the full-wave mode.



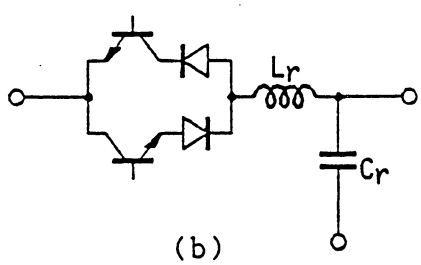
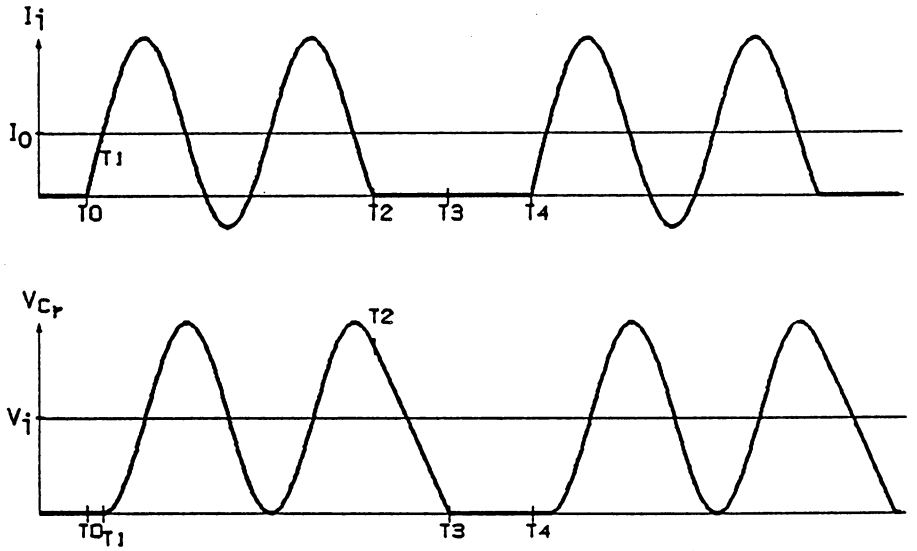
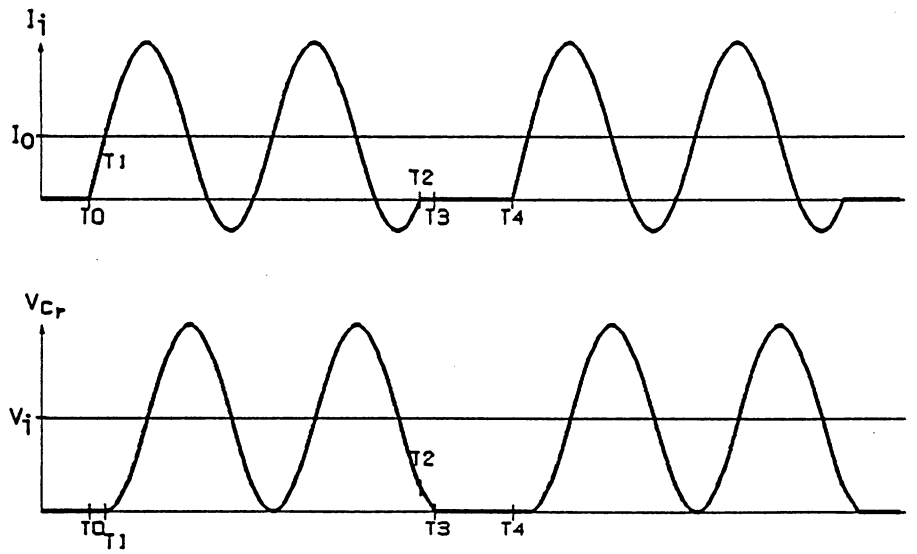


Fig. 2.12. Implementation of the general current-mode, resonant switches
(a) M-type (b) L-type



(a)



(b)

Fig. 2.13. Waveforms of the ZCS,
quasi-resonant buck converter
(a) 1.5-cycle mode (b) 2.0-cycle mode

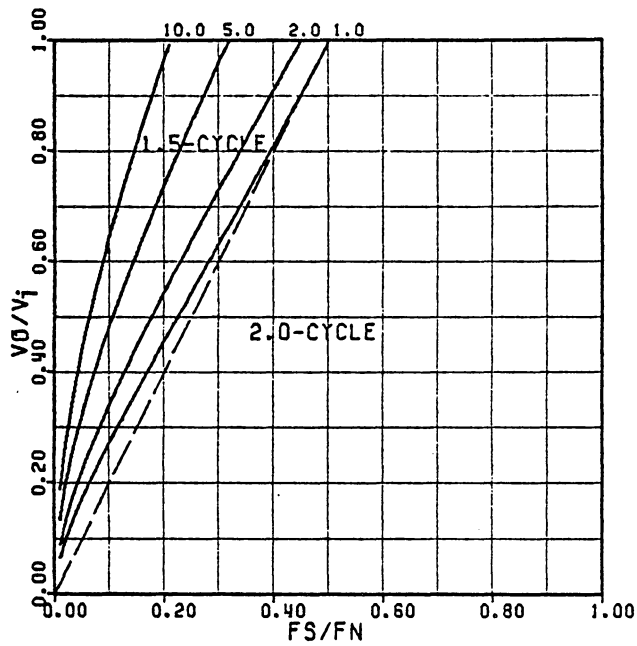


Fig. 2.14. DC voltage-conversion ratio of the ZCS, quasi-resonant buck converter -- 1.5-cycle mode and 2.0-cycle mode

2.4.3. DC Voltage-Conversion Ratios of the ZCS, Quasi-Resonant Boost and Buck/Boost Converters

DC analyses have been conducted for the ZCS, quasi-resonant boost and buck/boost converters. The derivation of the state equations of the ZCS, quasi-resonant boost converter in steady-state operation is summarized in Table 2.1. Typical waveforms of this circuit operating in the half-wave mode and the full-wave mode are shown in Fig. 2.15. The normalized voltage-conversion ratio of this circuit is governed by :

$$\frac{(x-1)}{x} - \left(\frac{1}{2\pi}\right)\left(\frac{f_s}{f_n}\right)\left[\left(\frac{x}{2r}\right) + \sin^{-1}\left(\frac{-x}{r}\right)\right.$$

$$\left. + \left(\frac{r}{x}\right)\left(1 + (sign)\sqrt{1 - \left(\frac{x}{r}\right)^2}\right)\right] = 0 \qquad (2.12)$$

Define $\alpha \equiv \sin^{-1}\left(\frac{-x}{r}\right)$, then

for the half-wave mode: $\pi < \alpha < 1.5\pi$; sign = 1

for the full-wave mode: $1.5\pi < \alpha < 2\pi$; sign = -1

The voltage-conversion ratios for the half-wave mode and the full-wave mode of operations are plotted in Fig. 2.16.

The derivation of the state equations for the ZCS, quasi-resonant buck/boost converter in steady-state operation is summarized in Table 2.2. Typical waveforms of this circuit operating in the half-wave mode and the full-wave mode

are shown in Fig. 2.17. The normalized voltage-conversion ratio of this circuit is governed by :

$$\frac{x}{(x+1)} - \left(\frac{1}{2\pi}\right)\left(\frac{f_s}{f_n}\right)\left[\left(\frac{x}{2r}\right) + \sin^{-1}\left(\frac{-x}{r}\right)\right.$$

$$\left. + \left(\frac{r}{x}\right)\left(1 + (sign)\sqrt{1 - \left(\frac{x}{r}\right)^2}\right)\right] = 0 \qquad (2.13)$$

The voltage-conversion ratio for the half-wave mode and the full-wave mode of operations are plotted in Fig. 2.18.

Again, it is interesting to point out that the conversion ratio of the quasi-resonant boost or buck/boost converter operating in the the full-wave mode is identical to its PWM counterpart if control parameter $\frac{f_s}{f_n}$ is replaced by D .

Table 2.1. ZCS, Quasi-Resonant Boost Converter

Inductor-Charging stage [T0, T1] : S_1 turns on at T_0 .

Initial Condition:

$$I_L(0) = 0 \tag{1a}$$

State Equation:

$$L_r \frac{dI_L}{dt} = V_o \tag{1b}$$

Time Solution:

$$T_{01} = \frac{L_r I_i}{V_o} = \frac{1}{\omega} \frac{Z_n I_i}{V_o} \tag{1c}$$

Resonant Stage [T1, T2] : I_L reaches I_i at T_1 , D_o cuts off.

Initial Conditions:

$$I_L(0) = I_i ; \quad V_C(0) = V_o \tag{2a}$$

State Equations:

$$L_r \frac{dI_L}{dt} = V_C ; \quad C_r \frac{dV_C}{dt} = I_i - I_L \tag{2b}$$

Time Solutions:

$$I_L = I_i + \frac{V_o}{Z_n} \sin \omega t \tag{2c}$$

$$V_C = V_o \cos \omega t \tag{2d}$$

$$T_{12} = \frac{\alpha}{\omega} \text{ , where } \alpha = \sin^{-1}\left(- \frac{Z_n I_i}{V_o} \right) \tag{2e}$$

Capacitor-Charging Stage [T2, T3] : I_L drops to zero at T_2 , S_1 turns off.

Initial Condition:

$$V_C(0) = V_o \cos \alpha \tag{3a}$$

State Equation:

$$C_r \frac{dV_C}{dt} = I_i \tag{3b}$$

Time Solution:

$$T_{23} = \frac{1}{\omega} \frac{V_o}{Z_n I_i} (1 - \cos \alpha) \tag{3c}$$

Passive Stage [T3, T4] : V_C reaches V_o at T_3 , D_o Turns on.

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{4}$$

Table 2.1. (cont.)

Input power per cycle, Ei :

$$E_i = V_i I_o T_s \tag{5}$$

Output power per cycle, Eo :

$$E_o = V_o \int_{T_0}^{T_1} (I_i - I_L)\, dt + V_o \int_{T_3}^{T_4} I_i\, dt = V_o I_i \left(\frac{T_{01}}{2} + T_{34}\right) \tag{6}$$

Also, the output power equals to $\frac{V_o^2}{R}$,

therefore, $I_i = \frac{V_o^2}{R V_i}$

From Eqs. (1c), (2e), and (3c),

$$T_{01} = \frac{1}{\omega}\frac{x}{r} \tag{7}$$

$$T_{12} = \frac{1}{\omega} \sin^{-1}\left(-\frac{x}{r}\right) \tag{8}$$

$$T_{23} = \frac{1}{\omega}\frac{r}{x}(1 - \cos\alpha) \tag{9}$$

where $x \equiv \frac{V_o}{V_i}$, $r \equiv \frac{R}{Z_n}$

By equating E_i and E_o ,

$$x \equiv \frac{V_o}{V_i} = \frac{T_s}{\frac{T_{01}}{2} + T_{34}} = \frac{T_s}{T_s - \frac{T_{01}}{2} - T_{12} - T_{23}}$$

$$\frac{1}{x} = 1 - \frac{1}{T_s}\left(\frac{T_{01}}{2} + T_{12} + T_{23}\right) \tag{10}$$

From Eqs. (7), (8), (9), and (10),

$$\frac{x-1}{x} = \frac{f_s}{2\pi f_n}\left[\frac{x}{2r} + \sin^{-1}\left(-\frac{x}{r}\right) + \frac{r}{x}(1 - \cos\alpha)\right] \tag{11}$$

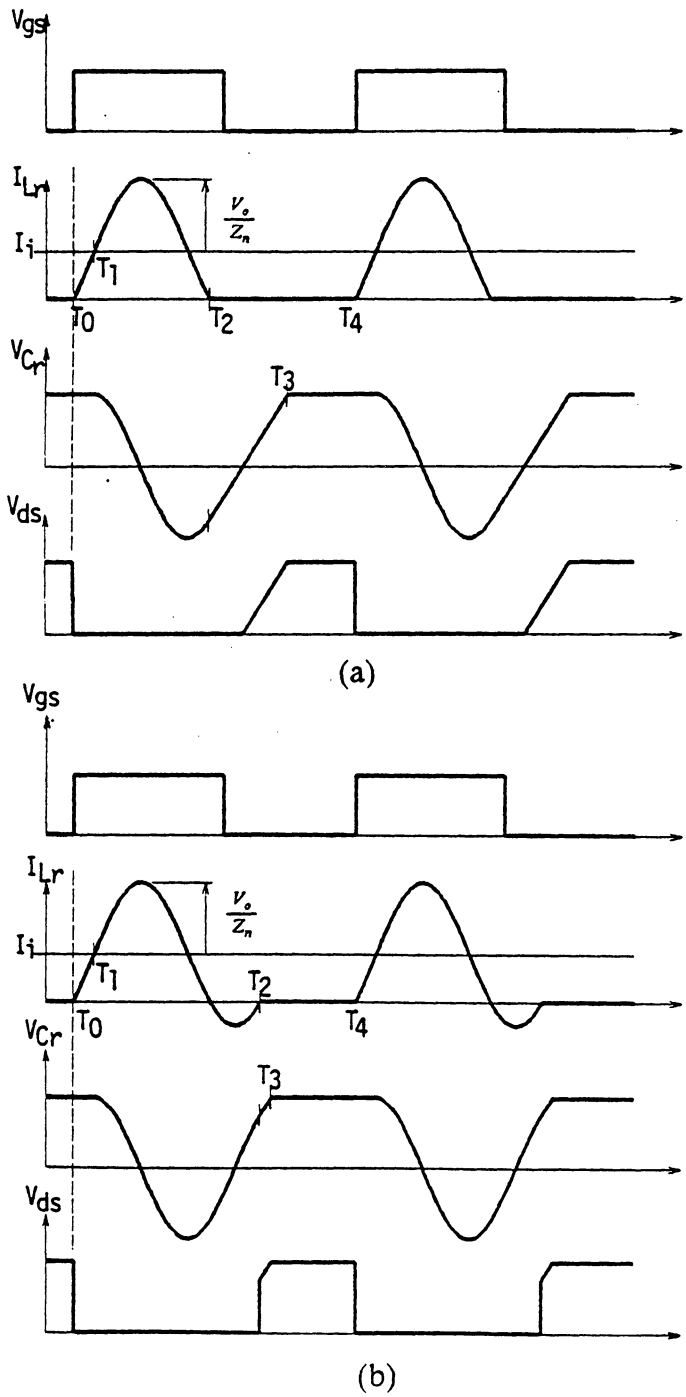
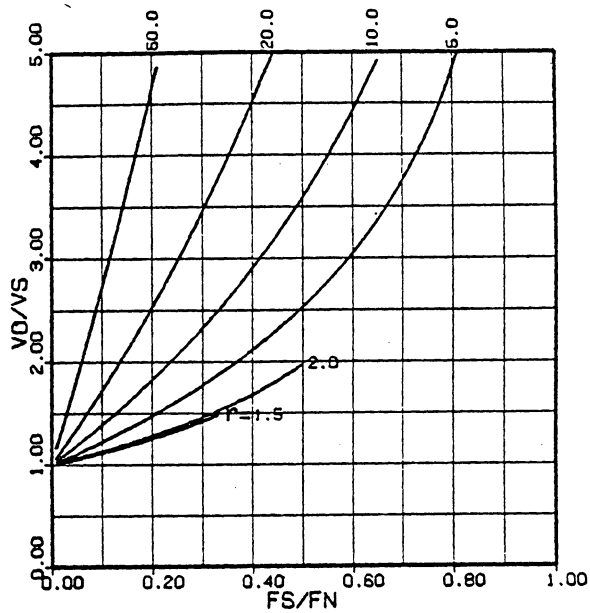
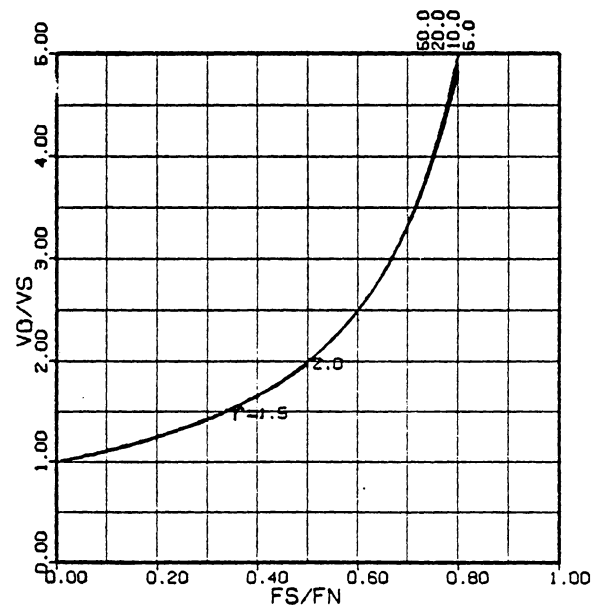


Fig. 2.15. Waveforms of the ZCS, quasi-resonant boost converter
(a) half-wave mode
(b) full-wave mode



(a)



(b)

Fig. 2.16. DC voltage-conversion ratio of the ZCS, quasi-resonant boost converter
(a) half-wave mode
(b) full-wave mode

Table 2.2. ZCS, Quasi-Resonant Buck/Boost Converter

Inductor-Charging Stage [T0, T1] : S_1 turns on at T_0.

Initial Condition:

$$I_L(0) = 0 \tag{1a}$$

State Equation:

$$L_r \frac{dI_L}{dt} = V_i + V_o \tag{1b}$$

Time Solution:

$$T_{01} = \frac{L_r I_m}{V_i + V_o} = \frac{1}{\omega} \frac{Z_n I_m}{V_i + V_o} \tag{1c}$$

Resonant Stage [T1, T2] : I_L reaches I_m at T_1, D_o turns off.

Initial Conditions:

$$I_L(0) = I_m ; \quad V_C(0) = -V_o \tag{2a}$$

State Equations:

$$L_r \frac{dI_L}{dt} = V_i - V_C ; \quad C_r \frac{dV_C}{dt} = I_L - I_m \tag{2b}$$

Time Solutions:

$$I_L(t) = I_m + \frac{V_i + V_o}{Z_n} \sin \omega t \tag{2c}$$

$$V_C(t) = V_i - (V_i + V_o) \cos \omega t \tag{2d}$$

$$T_{12} = \frac{\alpha}{\omega}, \text{ where } \alpha = \sin^{-1}\left(\frac{-Z_n I_m}{V_i + V_o}\right) \tag{2e}$$

Capacitor-Discharging Stage [T2, T3] : I_L drops to zero at T_2, S_1 turns off.

Initial Condition:

$$V_C(0) = V_i - (V_i + V_o) \cos \alpha \tag{3a}$$

State Equation:

$$C_r \frac{dV_C}{dt} = -I_m \tag{3b}$$

Time Solution:

$$T_{23} = \frac{1}{\omega} \frac{V_i + V_o}{Z_n I_m} (1 - \cos \alpha) \tag{3c}$$

Passive Stage [T3, T4] : V_C drops to $-V_o$ at T_3, D_o conducts.

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{4}$$

Table 2.2. (cont.)

Input power per cycle, Ei :

$$E_i = V_i \int_{T_0}^{T_1} I_L \, dt + V_i \int_{T_1}^{T_2} I_L \, dt = V_i I_m \left(\frac{T_{01}}{2} + T_{12} + T_{23} \right) \tag{5}$$

Output power per cycle, Eo :

$$E_o = V_o \int_{T_0}^{T_1} (I_m - I_L) \, dt + V_o \int_{T_3}^{T_4} I_m \, dt = V_o I_m \left(\frac{T_{01}}{2} + T_{34} \right) \tag{6}$$

Equating E_i and E_o ,

$$\frac{V_o}{V_i} = \frac{T_{01} + T_{12} + T_{23}}{\frac{T_{01}}{2} + T_{34}} = \frac{T_A}{T_s - T_A} = \frac{T_s}{T_s - T_A} - 1 \tag{7}$$

where $T_A \equiv \frac{T_{01}}{2} + T_{12} + T_{23}$

Also, $\frac{V_o^2 T_s}{R} = I_m V_o (T_s - T_A)$, therefore,

$$I_m = \frac{V_o (V_o + V_i)}{V_i R} \tag{8}$$

Substitute Eq. (8) into Eqs. (1c), (2e), and (3c),

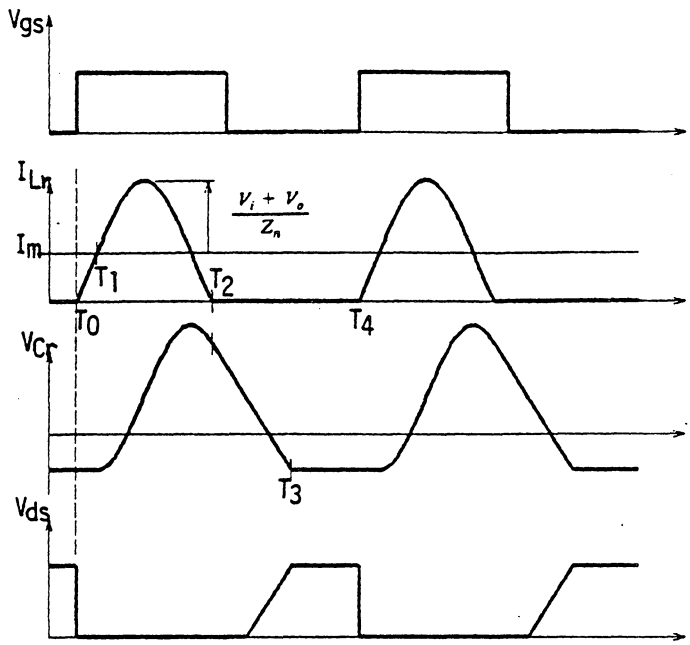
$$T_{01} = \frac{1}{\omega} \frac{x}{r} \tag{9}$$

$$T_{12} = \frac{1}{\omega} \sin^{-1} \left(\frac{-x}{r} \right) \tag{10}$$

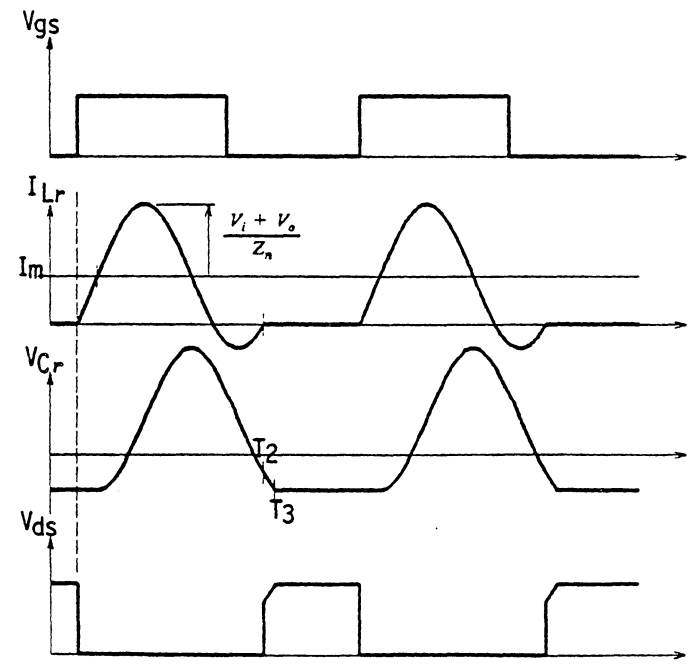
$$T_{23} = \frac{1}{\omega} \frac{r}{x} (1 - \cos \alpha) \tag{11}$$

By using Eqs. (7) to (11),

$$\frac{x}{1 + x} = \frac{f_s}{2\pi f_n} \left[\alpha + \frac{x}{2r} + \frac{r}{x} (1 - \cos \alpha) \right] \tag{12}$$



(a)



(b)

Fig. 2.17. Waveforms of the ZCS, quasi-resonant buck/boost converter
(a) half-wave mode
(b) full-wave mode

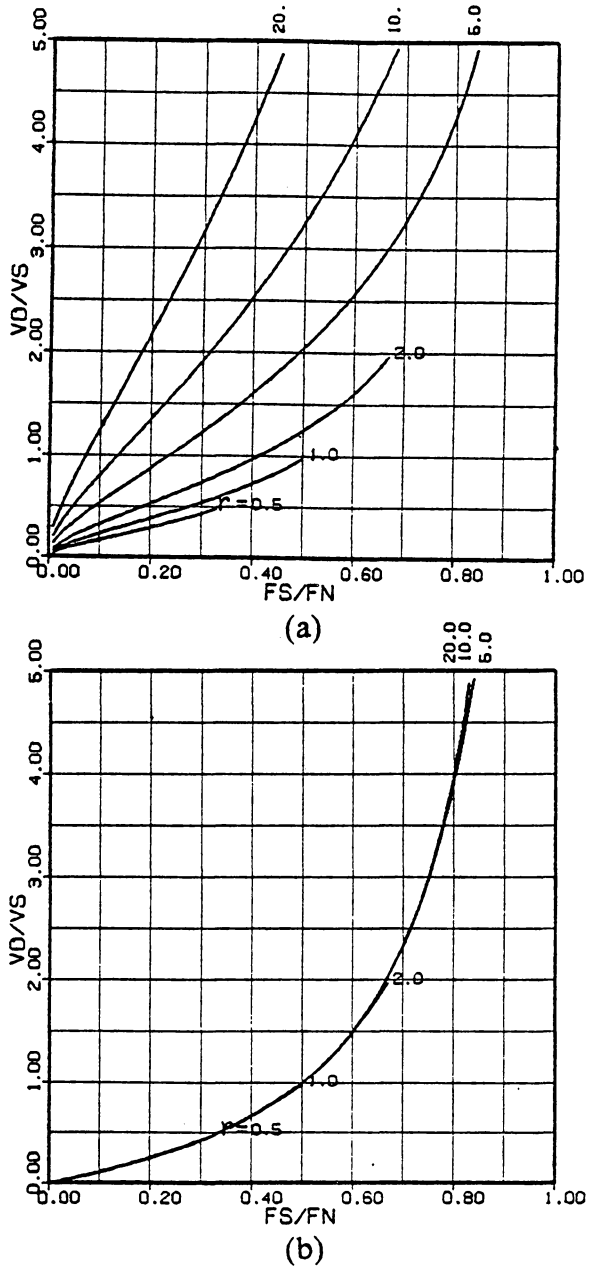


Fig. 2.18. DC voltage-conversion ratio of the ZCS, quasi-resonant buck/boost converter
(a) half-wave mode
(b) full-wave mode

2.5. *Experimental Verifications*

A 50W, ZCS, quasi-resonant buck converter operating in the half-wave mode is implemented to verify the results of the dc analysis. The circuit diagram and component values are shown in Fig. 2.19. The resonant frequency and characteristics impedance of the resonant tank circuit are set at 500kHz and 5Ω, respectively. Waveforms of this circuit operated under full load and 20% load and under different switching frequencies are shown in Fig. 2.20. The measured data are also summarized in Table 2.3.

When this circuit is modified by adding an anti-parallel diode, it becomes a full-wave, ZCS, quasi-resonant buck converter. The circuit diagram is shown in Fig. 2.21. Waveforms under different load and switching frequency conditions are shown in Fig. 2.22. The measured data are summarized in Table 2.4.

Recorded load-line trajectories (switch current vs. switch voltage) for the two previous circuits are shown in Fig. 2.23. It can be seen that the switching loci of the resonant switches indeed move roughly along the vertical and horizontal axes, i.e., across the low-stress region.

From Tables 2.3 and 2.4, it is seen the full-wave mode circuit has a lower efficiency than that of the half-wave mode circuit under a same load and same switching frequency. Since in the full-wave mode of operation, part of the energy stored in the resonant tank circuit is returned to the source and recycled repetitively, its conduction loss is higher and efficiency is lower.

Figure 2.24 shows the comparison between the measured voltage-conversion ratio and the theoretically predicted values for the half-wave and the full-wave mode of operations. For the full-wave mode of operation, the measured voltage-conversion ratios are shown to slightly increase with the load resistance (Fig. 2.24b). Several factors may contribute to the discrepancies:

- On-state voltage drops of semiconductor devices and circuit stray resistances -- both cause higher voltage drops as the load current is increased.

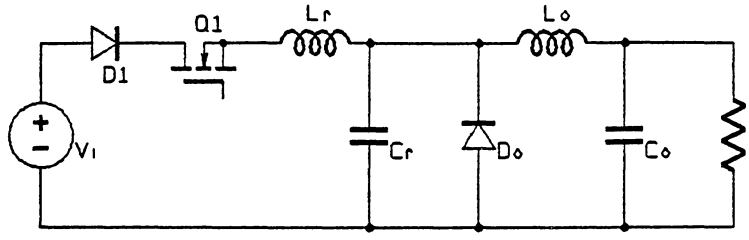
- Parasitic junction capacitance (C_{ce} or C_{ds}) -- results in additional forward-current conduction time after T_2 (as shown in the waveforms in Figs. 2.10 and 2.22) although, theoretically, the switch current is expected to stop at time T_2.

- Reverse recovery of anti-parallel diode D_1 -- also contributes to the additional forward-current conduction time.

The additional forward-current conduction time allows extra energy flow into the load and, consequently, raises the voltage-conversion ratio above the value predicted by the idealized model.

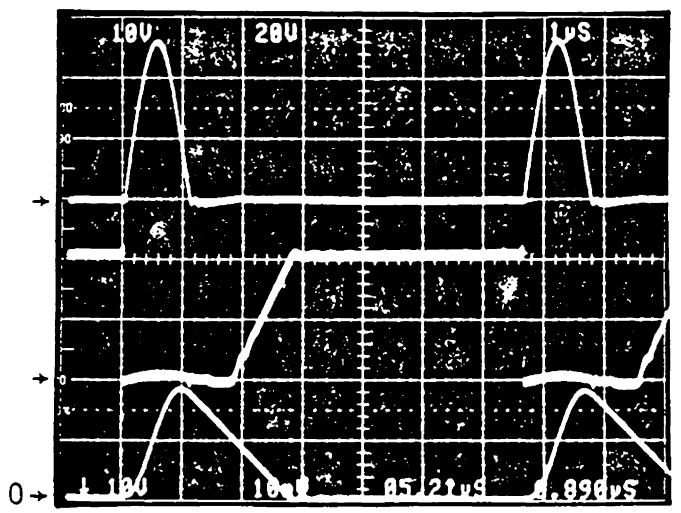
A 5.2MHz, 50W converter is implemented by changing the values of L_r and C_r of the circuit in Fig. 2.19. With values of L_r and C_r scaled down by a factor of 10, the resonant frequency becomes 5.2MHz, but the characteristic impedance remains 4.9Ω. Waveforms of this converter circuit, operating at a switching fre-

quency of 5.2MHz, are shown in Fig. 2.25. Measured efficiency at full load is about 85%.

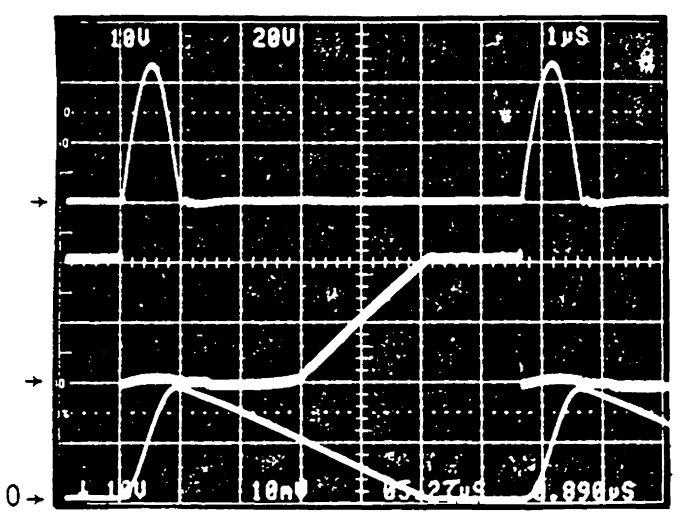


Q1 = IRF 530	Cr = 0.064 µF
D1 = IR 31DQ06	Lr = 1.6 µH
Do = IR 31DQ06	Lo = 100 µH
Vi = 20V	Co = 100 µF
fn = 500kHz	Zn = 5 Ω

Fig. 2.19. A 500kHz, half-wave, ZCS, quasi-resonant buck converter

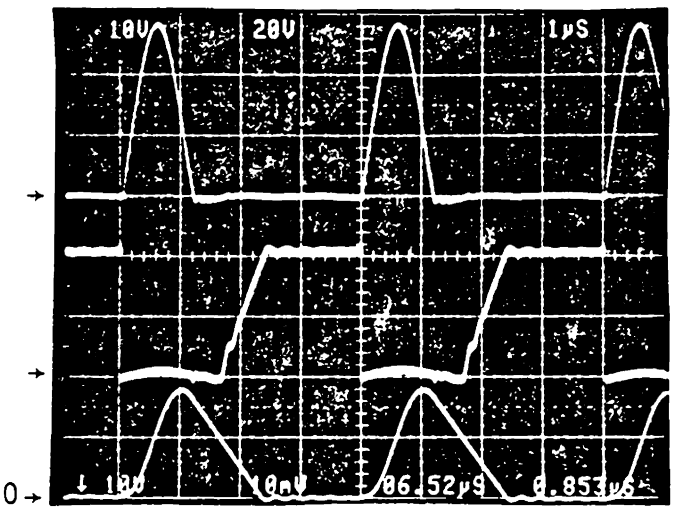


(a)

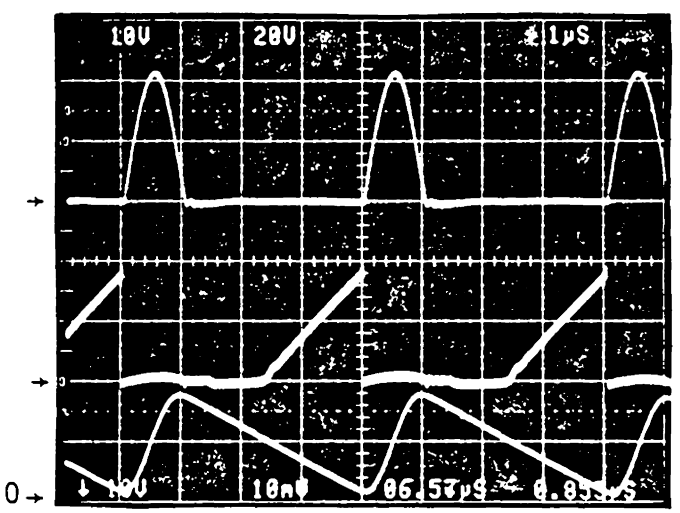


(b)

Fig. 2.20. Measured waveforms from the converter circuit in Fig. 2.19.
Top: Id(2A/div.), Middle: Vds(10V/div.), Bottom: Vcr(20V/div.)
(a) R = 5Ω, fs = 150kHz (b) R = 25Ω, fs = 150kHz

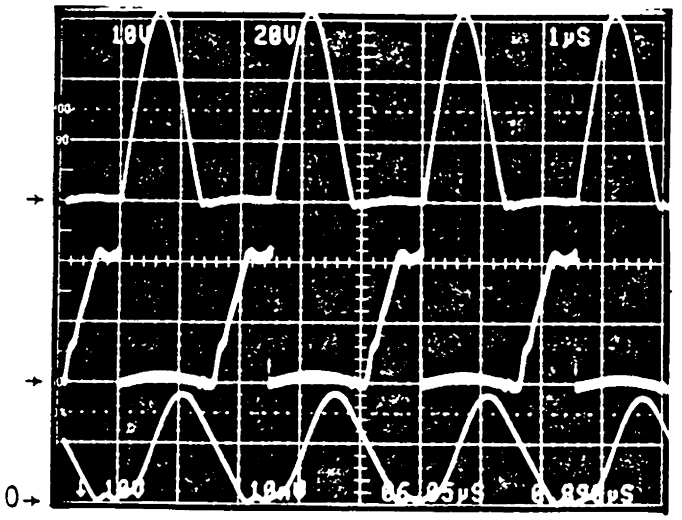


(c)

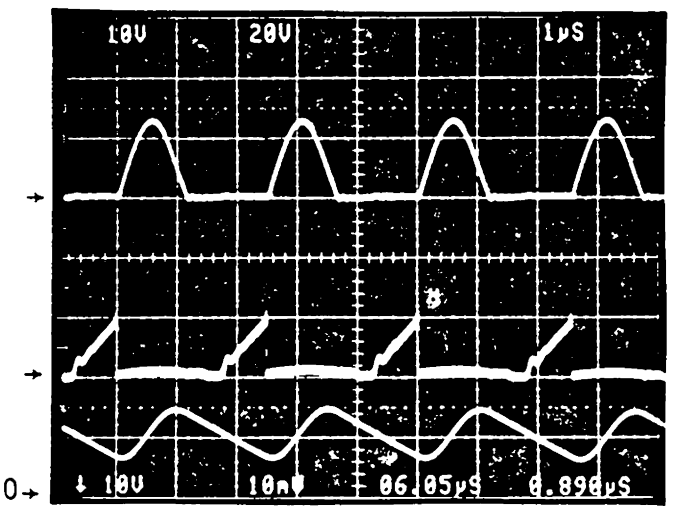


(d)

Fig. 2.20. (cont.)
(c) $R = 5\Omega$, $fs = 250kHz$ (d) $R = 25\Omega$, $fs = 250kHz$



(e)

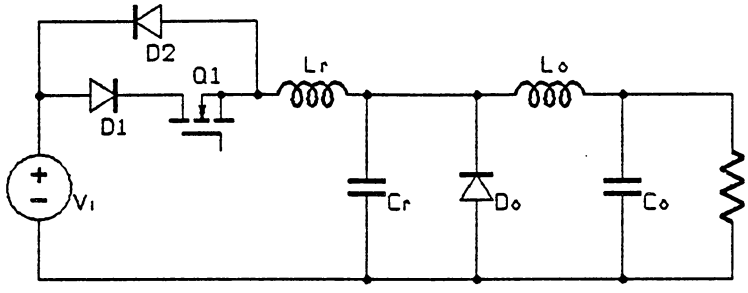


(f)

Fig. 2.20. (cont.)
(e) $R = 5\Omega$, $fs = 400kHz$ *(f)* $R = 25\Omega$, $fs = 400kHz$

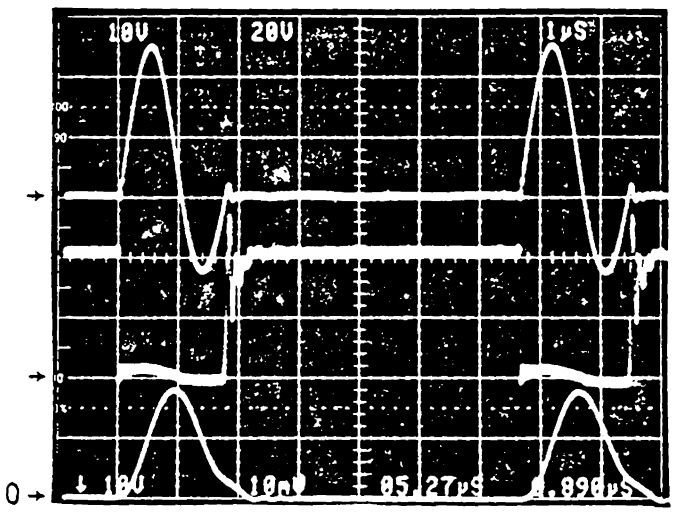
Table 2.3. Measured circuit parameters from the circuit in Fig. 2.19 under different load conditions

	Vi (V)	Ii (A)	Pi (W)	Vo (V)	Io (A)	Po (W)	efficiency
400 kHz							
5Ω	20	2.05	41.	14.0	2.58	36.1	88. %
25Ω	20	0.74	14.8	18.9	0.74	14.0	94.5%
250 kHz							
5Ω	20	1.08	21.6	10.1	1.88	19.	87.9%
25Ω	20	0.72	14.4	18.2	0.72	13.1	91.0%
150 kHz							
5Ω	20	0.56	11.2	7.3	1.35	9.86	88. %
25Ω	20	0.44	8.8	14.1	0.56	7.9	89.7%

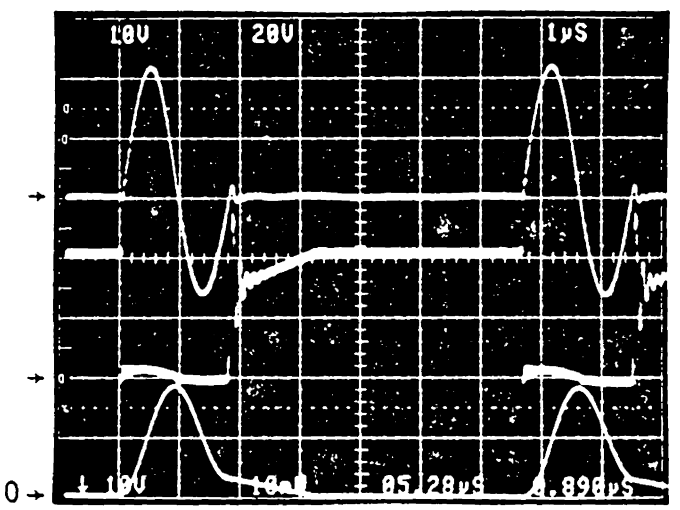


Q1 = IRF 530	Cr = 0.064 µF
D1 = IR 31DQ06	Lr = 1.6 µH
D2 = IR 31DQ06	Lo = 100 µH
Do = IR 31DQ06	Co = 100 µF
fn = 500kHz	Zn = 5 Ω

Fig. 2.21. A 500kHz, full-wave, ZCS, quasi-resonant buck converter

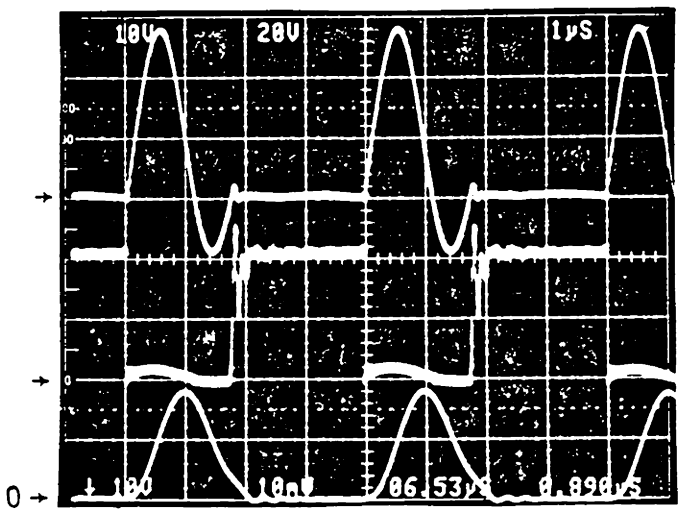


(a)

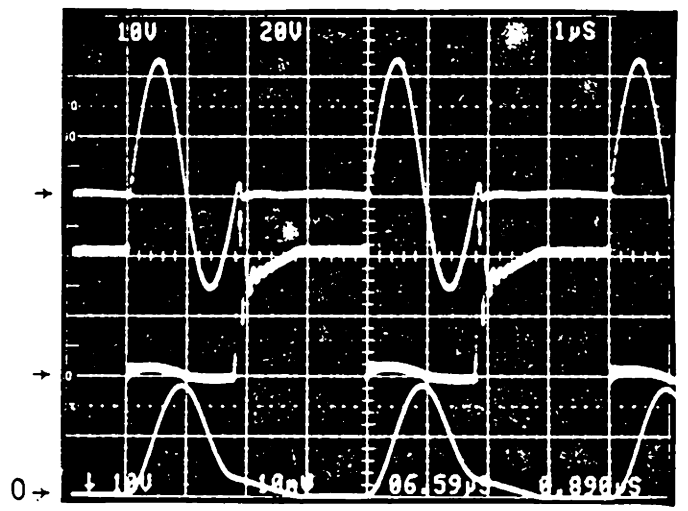


(b)

Fig. 2.22. Measured waveforms of the converter circuit in Fig. 2.21.
Top: Id(2A/div.), Middle: Vds(10V/div.), Bottom: Vcr(20V/div.)
(a) R = 5Ω, fs = 150kHz (b) R = 25Ω, fs = 150kHz

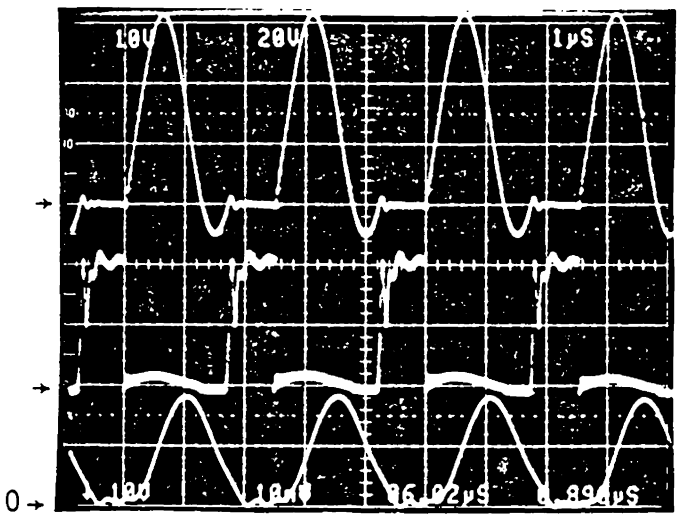


(c)



(d)

Fig. 2.22. (cont.)
(c) $R = 5\Omega$, $fs = 250kHz$ (d) $R = 25\Omega$, $fs = 250kHz$



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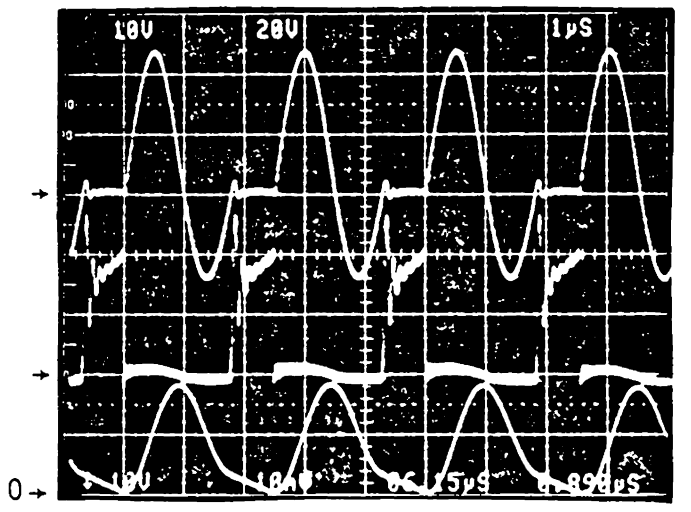


(f)

Fig. 2.22. (cont.)
(e) $R = 5\Omega, fs = 400kHz$ *(f)* $R = 25\Omega, fs = 400kHz$

Table 2.4. Measured circuit parameters from the circuit in Fig. 2.21 under different load conditions

	Vi (V)	Ii (A)	Pi (W)	Vo (V)	Io (A)	Po (W)	efficiency
400 kHz							
5Ω	20	1.94	38.8	13.4	2.5	33.5	86.3%
25Ω	20	0.59	11.8	14.9	0.6	8.94	75.8%
250 kHz							
5Ω	20	0.83	16.6	8.6	1.62	13.9	83.9%
25Ω	20	0.27	5.4	9.5	0.38	3.61	66.8%
150 kHz							
5Ω	20	0.32	6.4	5.2	0.98	5.1	79.6%
25Ω	20	0.12	2.4	5.8	0.24	1.4	58.%

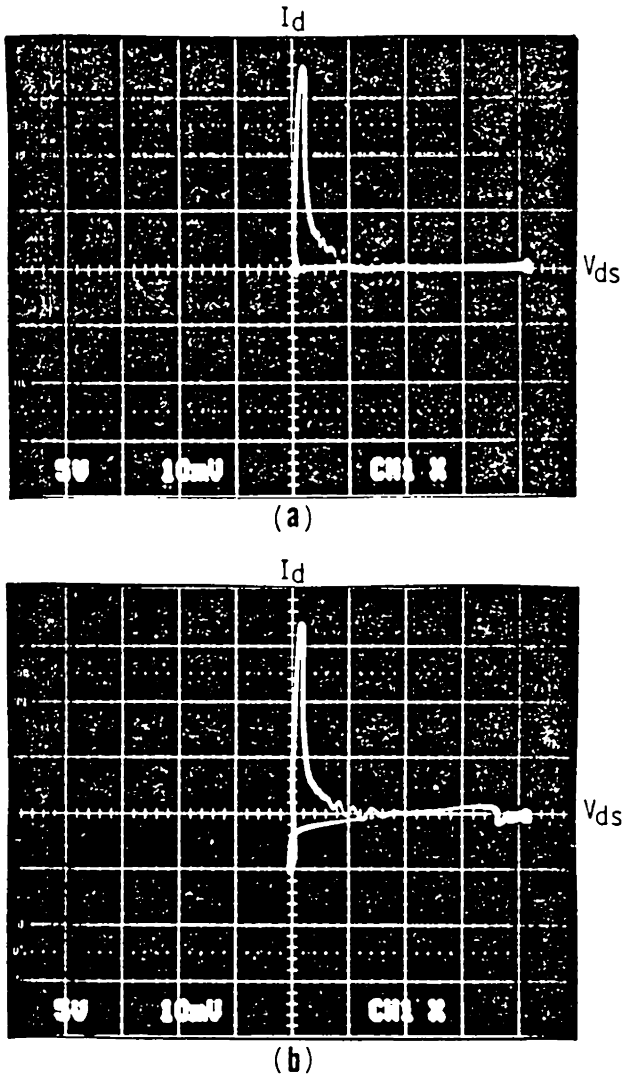
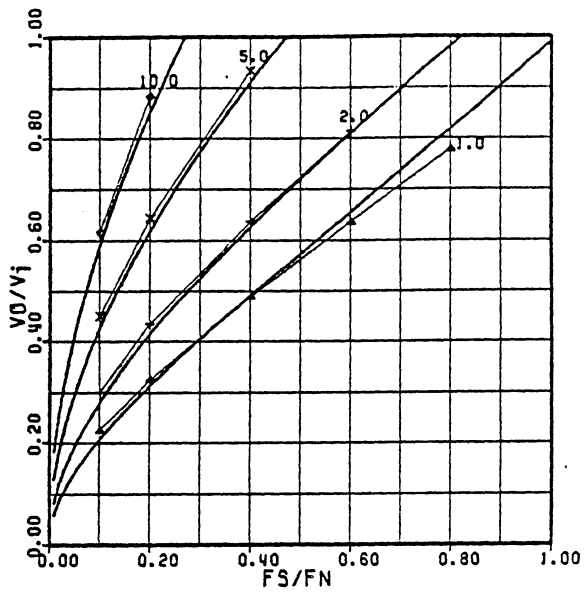
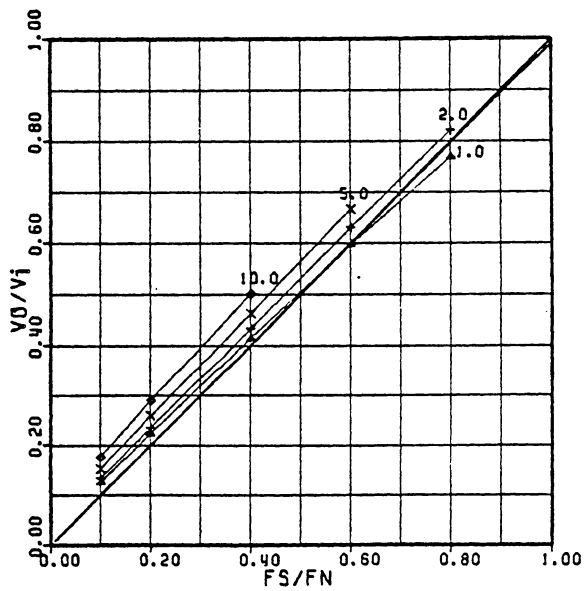


Fig. 2.23. Load-line trajectories
(a) Id vs. Vds from Fig. 2.20c.
(b) Id vs. Vds from Fig. 2.22c.



(a)



(b)

Fig. 2.24. Voltage-conversion ratio of the ZCS, quasi-resonant buck converter -- measured values vs. predicted values
(a) half-wave mode
(b) full-wave mode

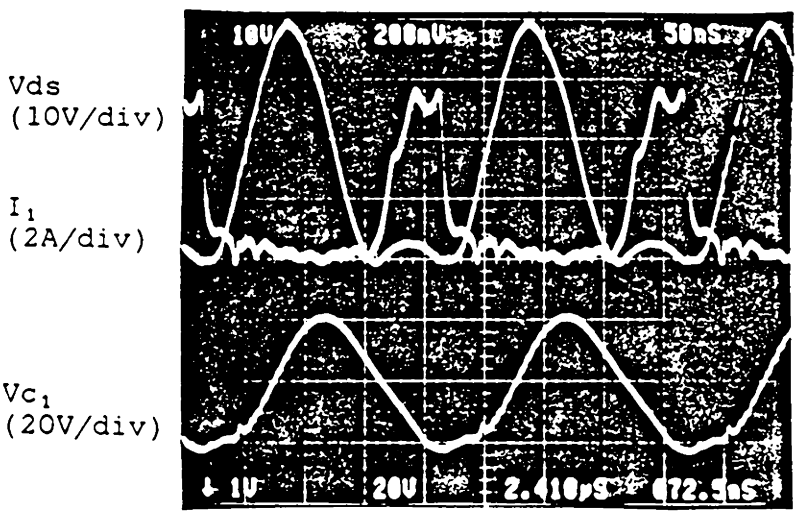


Fig. 2.25. Measured waveforms from a 5.2MHz, ZCS, quasi-resonant buck converter

2.6. *Summary*

By employing an LC tank circuit to shape the current waveform of the switching device in a converter circuit, a zero-current condition is created for the device to turn on and turn off. This zero-current switching technique offers many advantages, especially for the minority-carrier devices, which are generally more difficult to turn off:

- The zero-current switching technique provides self commutation to the switching device, and simplifies the design of the turn-off drive circuit.

- Switching under zero-current conditions greatly reduces the switching losses and switching stresses, which is evident from the load-line trajectories.

- Paralleling semiconductor devices in the zero-current switching scheme is simpler, since the device current waveform is mainly determined by the resonant tank circuit, and the dynamic current sharing problem due to the mismatch in switching speed among the paralleled devices is expected to be eliminated.

- The zero-current switching technique eliminates the need of snubber circuits.

Practical design and improved performance have been reported in circuits applying the zero-current switching technique in conventional resonant converters as well as in quasi-resonant converters [B1-B7].

When higher operating frequencies, e.g. above 1MHz, are desired, minority-carrier devices are generally too slow to be used in switching-mode power converter circuits. Currently, only power MOSFETs are capable of the switching speed required in megahertz converters. Power MOSFETs have very fast switching speed and are voltage-driven devices. Since they are majority-carrier devices, switching loss due to the carrier-recombination is no longer a problem.

On the other hand, like all other power semiconductor devices, power MOSFETs have parasitic junction capacitances. When switching at very high frequencies, the loss due to the discharging of the junction capacitances becomes the dominant one. As a result, converter circuits employing the PWM or the ZCS technique can no longer provide sufficient performance when operated in very high frequencies (above one megahertz). To resolve the problems associated with the capacitive turn-on loss, a zero-voltage switching (ZVS) technique is proposed. This technique will be discussed in detail in the next chapter.

3. ZERO-VOLTAGE SWITCHING TECHNIQUE

3.1. Voltage-Mode Resonant Switches

As explained in Sec. 2.6, in very high frequency operations, the capacitive turn-on loss is the dominant one. For example, a drain-source junction capacitance of 100pF switching at 300V will induce a turn-on loss of 4.5W at 1MHz, and 22.5W at 5MHz. The strategy in avoiding this turn-on loss, naturally, is to shape the device voltage waveform during its off-time such that a zero-voltage condition is created for the device to turn on.

It has been described in Sec. 2.2 that an LC tank circuit is a lossless waveform-shaping device. Either the resonant inductor current or the resonant capacitor voltage can be employed in waveform shaping. When voltage-waveform shaping is desired [C1-C18, E1-E16], the capacitor of the resonant tank is connected in parallel with the switching device. The resulting voltage-mode resonant switches are shown in Fig. 3.1.

As in the case of a current-mode resonant switch, the structure of switch S_1 determines the operation mode of the voltage-mode resonant switch. If ideal switch S_1 is implemented by a transistor, Q_1, and an anti-parallel diode, D_1, as shown in Fig. 3.1b, the voltage across capacitor C_r is clamped by D_1 to positive values, and the resonant switch is operating in a half-wave mode. On the other hand, if S_1 is implemented by Q_1 in series with D_1, as shown in Fig. 3.1c, and the voltage across C_r can oscillate freely, then the resonant switch is operating in a full-wave mode.

Notice that in a current-mode resonant switch, the resonant interaction between L_r and C_r occurs during the major portion of the on-time; while in a voltage-mode resonant switch, the resonant interaction occurs during the major portion of the off-time.

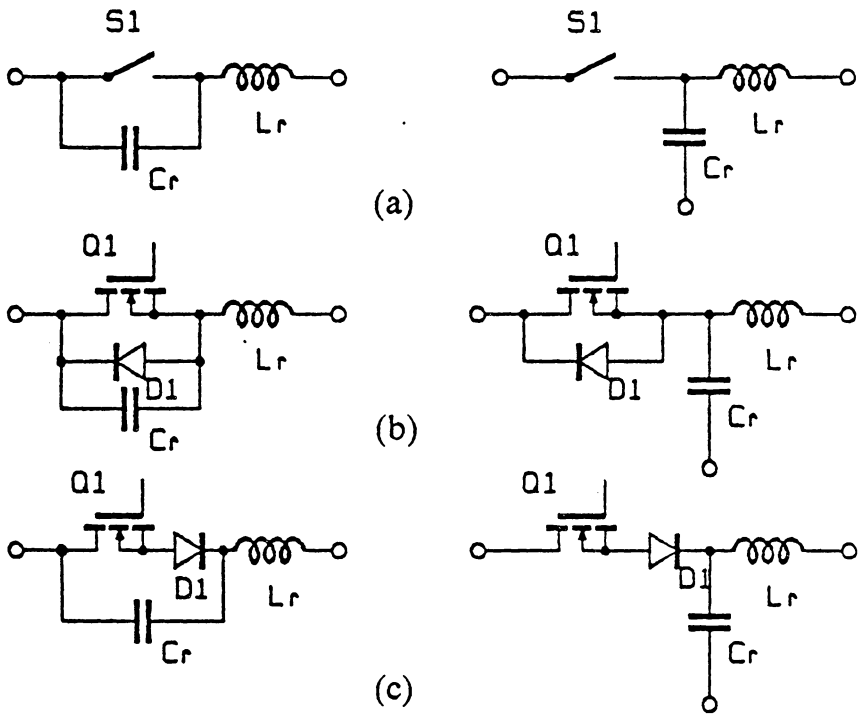


Fig. 3.1. Voltage-mode resonant switches
(a) general notation (Left: M-type, Right: L-type)
(b) half-wave mode implementation
(c) full-wave mode implementation

3.2. A Zero-Voltage Switching, Quasi-Resonant Boost Converter

In steady-state operation, a conventional boost converter, as shown in Fig. 3.2a, can be treated as a constant current source, I_i , supplying power to a constant voltage load, V_o, by means of duty-cycle control of switch S_1 , as shown in Fig. 3.2b. When switch S_1 is replaced by the voltage-mode resonant switch of S_1-L_r-C_r, a **zero-voltage switching** (ZVS), quasi-resonant boost converter is formed, as shown in Fig. 3.2c. Since the circuit's behavior is largely determined by the values of L_r and C_r, the following parameters are defined:

- Characteristic impedance $Z_n \equiv \sqrt{L_r/C_r}$
- Resonant angular frequency $\omega \equiv \frac{1}{\sqrt{L_r C_r}}$
- Resonant frequency $f_n \equiv \frac{\omega}{2\pi}$
- Normalized load resistance $r \equiv \frac{R}{Z_n}$

In steady-state operation, a complete switching cycle can be divided into four stages starting from the moment S_1 turns off. Suppose, before S_1 is turned off, it carries the input current, I_i . Diode D_2 is off and no current is flowing into the voltage load, V_o . At time T_0 , S_1 turns off, input current I_i is diverted into

capacitor C_r. The following description summarizes the circuit operation during each of the four stages:

(1). **Capacitor-Charging Stage** $[T_0, T_1]$:

S_1 turns off at T_0, current I_i flows into C_r, the voltage across C_r, V_{Cr}, rises linearly.

Initial Condition:

$$V_{Cr}(0) = 0 \tag{3.1a}$$

State equation:

$$C_r \frac{dV_{Cr}}{dt} = I_i \tag{3.1b}$$

At time T_1, V_{Cr} reaches V_o and diode D_2 conducts. The duration of this stage, T_{01}, can be determined:

$$T_{01} = C_r \frac{V_o}{I_i} \tag{3.1c}$$

The equivalent circuit of this stage is shown in Fig. 3.3a.

(2). **Resonant Stage** $[T_1, T_2]$:

D_2 turns on at T_1 , a portion of I_i starts to flow into V_o .

Initial Conditions:

$$I_{Lr}(0) = 0$$

$$V_{Cr}(0) = V_o \tag{3.2a}$$

State equations:

$$L_r \frac{dI_{Lr}}{dt} = V_{Cr} - V_o$$

$$C_r \frac{dV_{Cr}}{dt} = I_i - I_{Lr} \tag{3.2b}$$

The state equations can be solved:

$$I_{Lr}(t) = I_i(1 - \cos \omega t)$$

$$V_{Cr}(t) = V_o + Z_n I_i \sin \omega t \tag{3.2c}$$

In the half-wave mode of operation, when V_{Cr} drops to zero at T_a , it is clamped at that value by the anti-parallel diode, D_1, which carries the reverse current. While in the full-wave mode of operation, V_{Cr} continues to oscillate to a negative value and returns to zero at time T_b . For the half-wave mode, the end of this stage, T_2, is equal to T_a ; for the full-wave mode, it is equal

to T_b . The duration of this stage, T_{12} , can be solved by setting $V_{Cr}(T_2)$ to 0.

$$\text{Thus,} \quad T_{12} = \frac{\alpha}{\omega}, \quad \text{where } \alpha = \sin^{-1}\left(\frac{V_o}{Z_n I_i}\right) \tag{3.2d}$$

The value of I_{Lr} at T_2 is:

$$I_{Lr}(T_2) = I_i(1 - \cos\alpha) \tag{3.2e}$$

where $\pi < \alpha < \frac{3\pi}{2}$, $T_2 = T_a$, for the half-wave mode

$\frac{3\pi}{2} < \alpha < 2\pi$, $T_2 = T_b$, for the full-wave mode

The equivalent circuit of this stage is shown in Fig. 3.3b. The waveforms of the half-wave mode and full-wave mode are shown in Fig. 3.4a and 3.4b, respectively.

(3). **Inductor-Discharging Stage** $[T_2, T_3]$:

After T_2 , current I_{Lr} drops linearly and reaches zero at time T_3 .

Initial Condition:

$$I_{Lr}(0) = I_i(1 - \cos\alpha) \tag{3.3a}$$

State equation:

$$L_r \frac{dI_{Lr}}{dt} = -V_o \tag{3.3b}$$

The duration of this stage, T_{23}, can be determined:

$$T_{23} = \frac{L_r I_i (1 - \cos \alpha)}{V_o} \tag{3.3c}$$

The equivalent circuit of this stage is shown in Fig. 3.3c.

Normally, in the half-wave mode of operation, transistor Q_1 will turn on after V_{Cr} drops to zero at T_a and before the current through D_1 drops to zero at T_c. Otherwise, V_{Cr} will begin to be recharged and Q_1 will lose the opportunity to turn on under zero-voltage conditions. In the full-wave mode of operation, Q_1 shall turn on between T_a and T_b, when diode D_1 is blocking the negative voltage.

(4). **Input Charging Stage** [T_3 , T_4] :

After T_3, entire input current I_i flows through Q_1. I_{Q1} remains constant until Q_1 turns off again at T_4. The duration of this stage, T_{34}, is determined by:

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{3.4}$$

where T_s is the period of a switching cycle.

Notice that the voltage waveform of V_{Cr} contains a dc component of V_o and an ac component of $Z_n I_i$. Since I_i is in proportion to the load current when V_o and V_i are fixed, the peak value of V_{Cr} increases as the load current is increased. Furthermore, to maintain a larger ac component than dc component, there exists a lower bound on the load current below which the zero-voltage switching property will be lost. On the other hand, the current waveform through Q_1 is squarewave-like; and its peak value is the same as that of input current I_i. The lower rms and dc value of the switch current is advantageous, since the conduction loss is kept minimal.

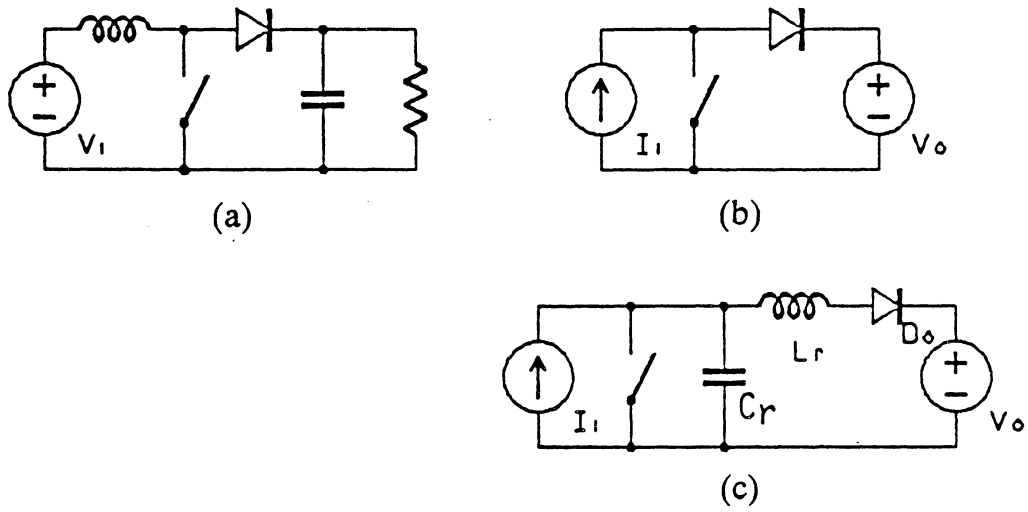


Fig. 3.2. Boost converter
(a) basic circuit structure
(b) steady-state equivalent circuit
(c) ZVS, quasi-resonant implementation

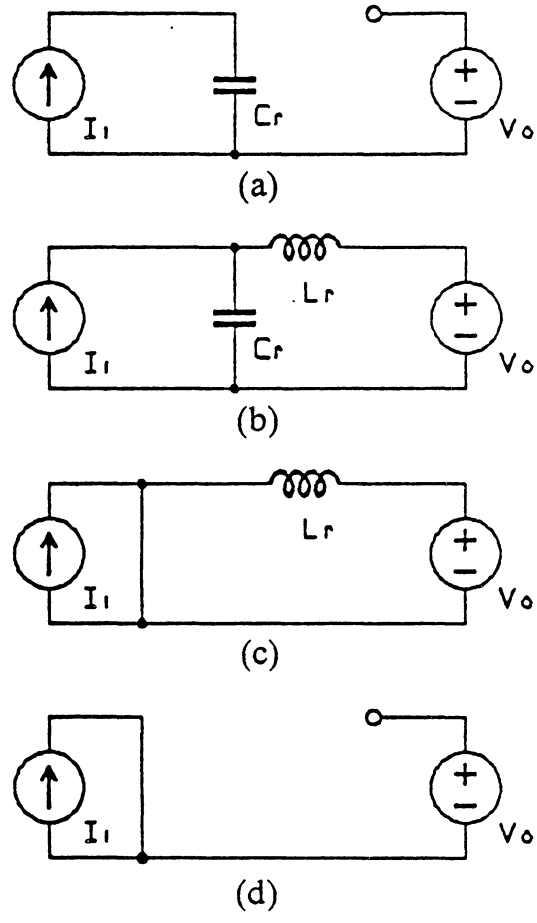
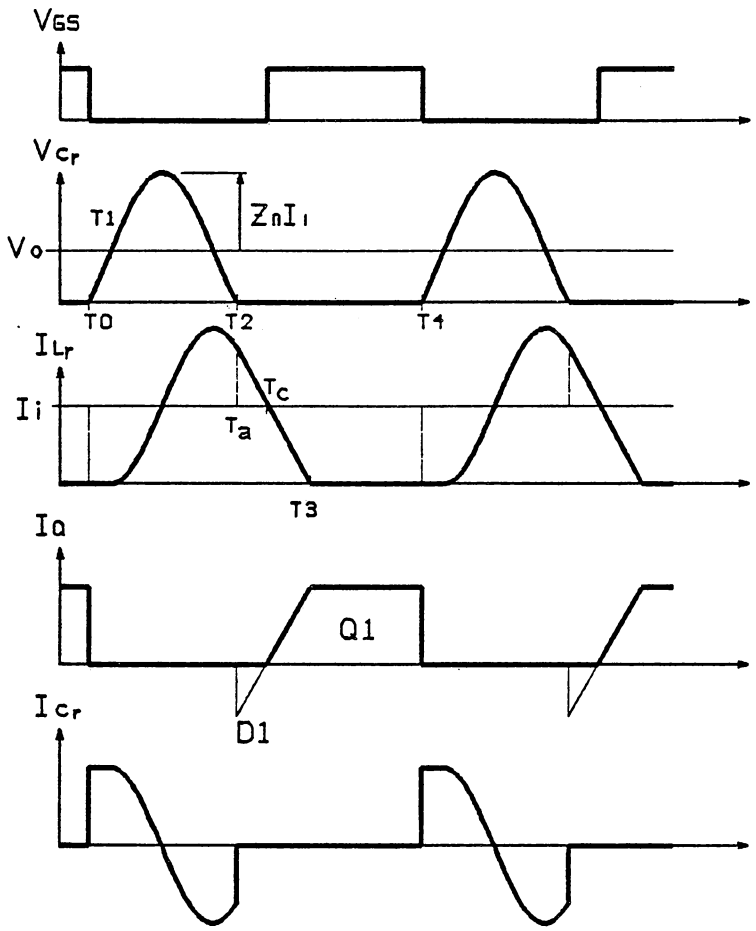
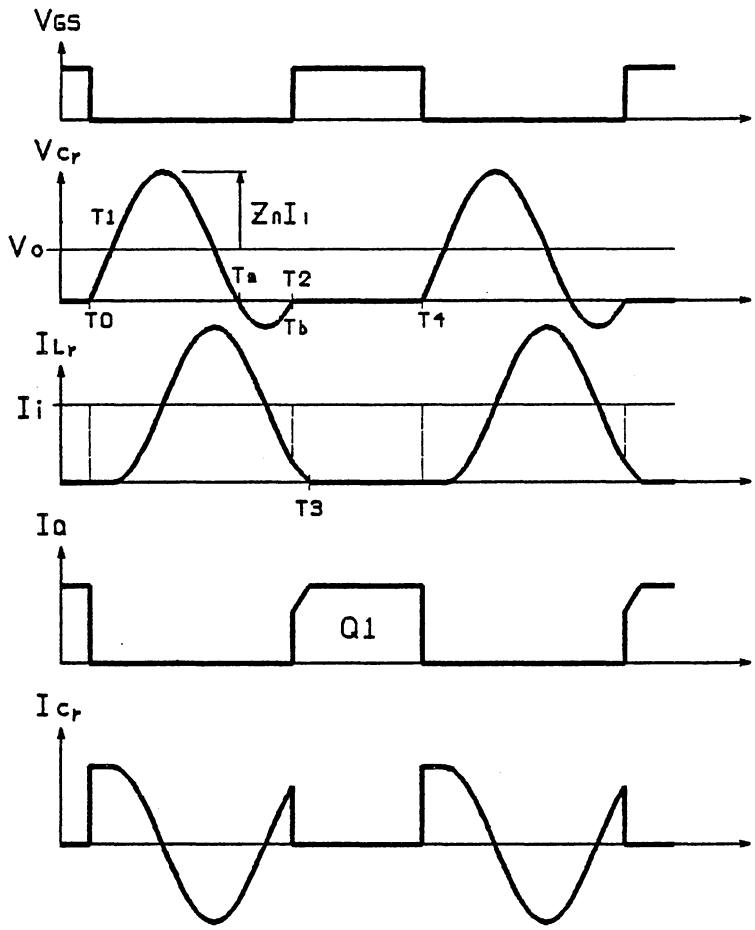


Fig. 3.3. The equivalent circuits of the ZVS, quasi-resonant boost converter in the four switching stages: (a) [T0, T1] (b) [T1, T2] (c) [T2, T3] (d) [T3, T4]



(a)

Fig. 3.4. Typical circuit waveforms of the ZVS, quasi-resonant boost converter in: (a) half-wave mode



(b)

Fig. 3.4. (cont.) (b) full wave-mode

3.3. Steady-State Characteristics

The steady-state circuit behavior can be obtained by solving the state equations of the four stages in a switching cycle. Peak voltage and peak current through the switch have been determined in the previous section. The dc voltage-conversion ratio, V_o/V_i , as a function of the load resistance and the switching frequency, can be derived by equating the input energy per cycle, E_i , and the output power per cycle, E_o .

$$E_i = V_i I_i T_s \tag{3.5a}$$

$$E_o = V_o \int_{T_1}^{T_2} I_{Lr}\, dt + V_o \int_{T_2}^{T_3} I_{Lr}\, dt \tag{3.5b}$$

From Eq. (3.2d),

$$\begin{aligned} \int_{T_1}^{T_2} I_{Lr}\, dt &= \int_0^{T_{12}} I_i (1 - \cos \omega t)\, dt \\ &= \frac{I_i}{\omega} (\alpha + \frac{r}{x}) \end{aligned} \tag{3.6a}$$

where r and x are defined as

$$r \equiv \frac{R}{Z_n}; \quad x \equiv \frac{V_o}{V_i}$$

From Eq. (3.3c):

$$\int_{T_2}^{T_3} I_{Lr}\,dt = \frac{I_i(1-\cos\alpha)}{2}T_{23} = \frac{I_i}{\omega}\left(\frac{x}{r}-\frac{r}{2x}-\frac{x}{r}\cos\alpha\right) \tag{3.6b}$$

Therefore, $$E_o = \frac{V_o I_i}{\omega}\left[\alpha+\frac{r}{2x}+\frac{x}{r}(1-\cos\alpha)\right] \tag{3.7}$$

From Eqs. (3.5) and (3.7), V_o/V_i is found:

$$\frac{V_o}{V_i} = x = \frac{1}{\frac{f_s}{2\pi f_n}\left[\alpha+\frac{r}{2x}+\frac{x}{r}(1-\cos\alpha)\right]} \tag{3.8}$$

where $\alpha = \sin^{-1}\left(-\frac{r}{x}\right)$, and $f_s = \frac{1}{T_s}$

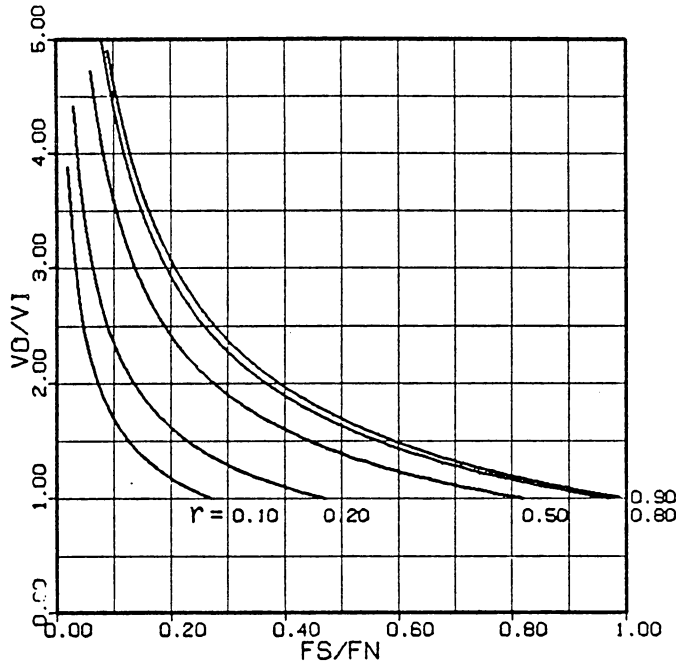
and $\pi < \alpha < \frac{3\pi}{2}$, for the half-wave mode

$\frac{3\pi}{2} < \alpha < 2\pi$, for the full-wave mode

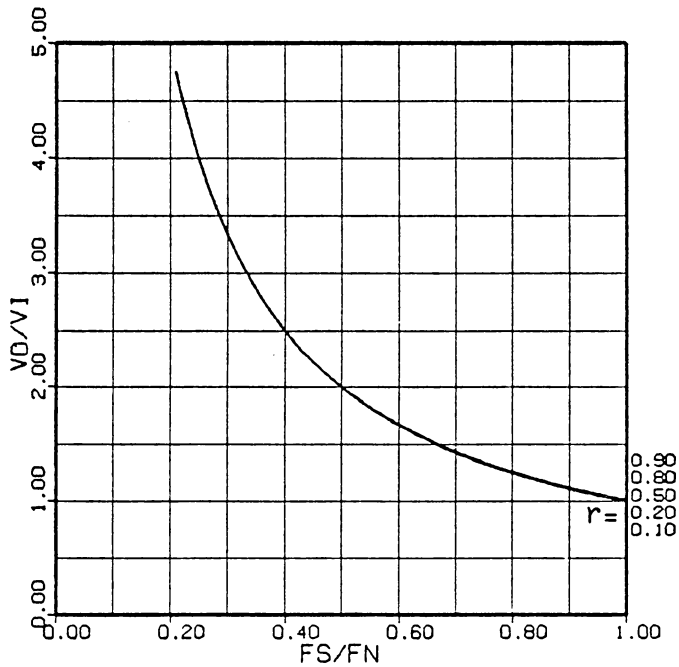
Equation (3.8) can be solved numerically. The results are plotted in Figs. 3.5a and 3.5b for the half-wave mode and the full-wave mode, respectively. It can be seen that the voltage-conversion ratio in the full-wave mode is insensitive to load variation and is more desirable. Notice in the full-wave mode implementation, as shown in Fig. 3.1c, a series diode is required to provide a reverse-voltage blocking capability. Consequently, the energy stored in the junction capacitances

of the semiconductor switch is trapped during the off-time and is dissipated internally after the switch turns on.

In practical implementations, however, due to non-ideal characteristics of semiconductor diodes, not all energy stored in the junction capacitances is actually trapped inside the switch. In fact, part of stored charge in the junction capacitance will be recovered through discharging via the junction capacitance of the series diode. Further detail in the actual behavior of the full-wave of operation will be described in Sec. 3.6.



(a)



(b)

Fig. 3.5. DC voltage-conversion ratios of the ZVS, quasi-resonant boost converter in: (a) half-wave mode (b) full-wave mode

3.4. A New Family of Zero-Voltage Switching, Quasi-Resonant Converters

By replacing the switches in the conventional PWM converters with L-type or M-type voltage-mode resonant switches, a family of zero-voltage switching (ZVS), quasi-resonant converters can be derived. A few topological variations of the ZVS, quasi-resonant converters are shown in Fig. 3.6. Notice that in the isolated versions, the leakage inductance of the transformer can be utilized as the resonant inductor, L_r. Moreover, when the junction capacitance of the switching device is used as the resonant capacitor, C_r, the circuit complexity and the number of components required are further reduced.

A particularly important topology is the ZVS, quasi-resonant flyback converter of Fig. 3.6e. When the leakage inductance of the transformer and the junction capacitance of the switching device are used as the resonant elements, this converter contains the fewest components and can still achieve the zero-voltage switching operation.

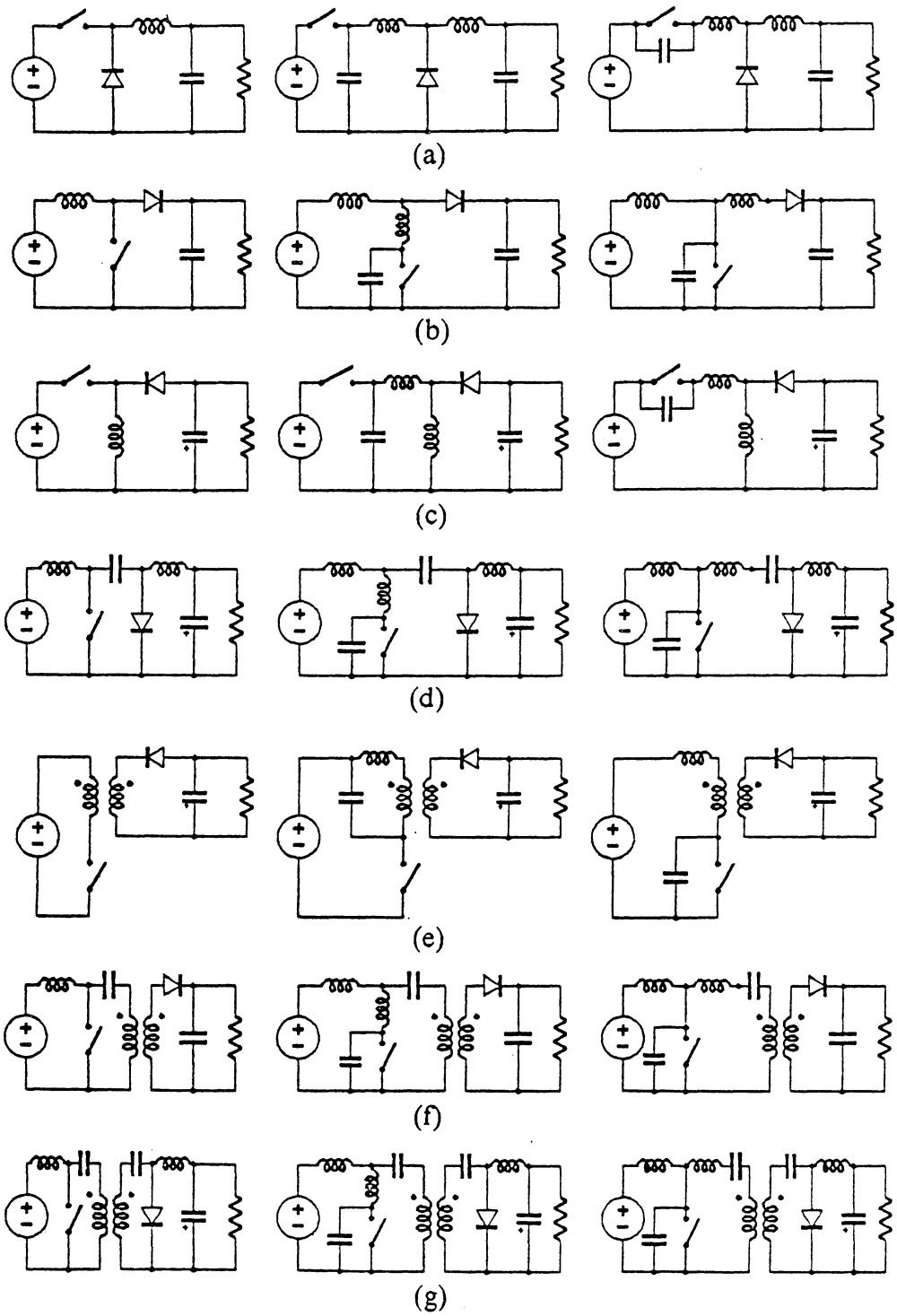


Fig. 3.6. A new family of ZVS, quasi-resonant converters: (a) buck (b) boost (c) buck/boost (d) Cuk (e) flyback (f) SEPIC (g) Cuk with transformer

3.5. DC Voltage-Conversion Ratios of ZVS, Quasi-Resonant Buck and Buck/Boost Converters

Steady-state analysis has been carried out on the ZVS, quasi-resonant buck and buck/boost converters. The derivation of the state equations of the ZVS, quasi-resonant buck converter in steady-state operation is summarized in Table 3.1. Typical waveforms of the circuit operating in the half-wave mode and the full-wave mode are shown in Fig. 3.7. The voltage-conversion ratio of this circuit is governed by:

$$\frac{V_o}{V_i} = x = 1 - \frac{f_s}{2\pi f_n}\left[\alpha + \frac{r}{2x} + \frac{x}{r}(1 - \cos\alpha)\right] \tag{3.9}$$

The voltage-conversion ratios for the half-wave and full-wave modes of operation are plotted in Fig. 3.8.

The derivation of the state equations of the ZVS, quasi-resonant buck/boost converter in steady-state operation is summarized in Table 3.2. Typical waveforms of the circuit operating in the half-wave mode and the full-wave mode are shown in Fig. 3.9. The voltage-conversion ratio of this circuit is governed by:

$$\frac{V_o}{V_i} = x = \frac{1}{\frac{f_s}{2\pi f_n}\left[\alpha + \frac{r}{2x} + \frac{x}{r}(1 - \cos\alpha)\right]} - 1 \tag{3.10}$$

The voltage-conversion ratios for the half-wave and full-wave modes of operation are plotted in Fig. 3.10.

As in the case of the ZVS, quasi-resonant boost converter, the voltage-conversion ratios are load insensitive in the full-wave mode and load sensitive in the half-wave mode.

Notice that in ZVS, quasi-resonant converters, the off-time of the switch is largely determined by the resonant frequency, f_n , and cannot be varied freely. In general, a constant off-time control is employed to regulate the output voltage against the load variation and the line variation. With constant off-time, higher switching frequency means shorter equivalent on-time and, therefore, the voltage-conversion ratio decreases as the switching frequency is increased.

Table 3.1. ZVS, Quasi-Resonant Buck Converter

Capacitor-Charging Stage [T0, T1] : S_1 turns off at T_0 .

Initial Condition:

$$V_C(0) = 0 \tag{1a}$$

State Equation:

$$C_r \frac{dV_C}{dt} = I_o \tag{1b}$$

Time Solution:

$$T_{01} = \frac{C_r V_i}{I_o} = \frac{1}{\omega}\frac{r}{x} \quad \text{where } r \equiv \frac{R}{Z_n},\ x \equiv \frac{V_o}{V_i} \tag{1c}$$

Resonant Stage [T1, T2] : V_C reaches V_i at T_1 , D_o conducts.

Initial Conditions:

$$I_L(0) = I_o\ ; \quad V_C(0) = V_i \tag{2a}$$

State Equations:

$$L_r \frac{dI_L}{dt} = V_i - V_C\ ; \quad C_r \frac{dV_C}{dt} = I_L \tag{2b}$$

Time Solutions:

$$I_L(t) = I_o \cos \omega t \tag{2c}$$

$$V_C(t) = V_i + Z_n I_o \sin \omega t \tag{2d}$$

$$T_{12} = \frac{\alpha}{\omega} \text{ , where } \alpha = \sin^{-1}\left(\frac{-V_i}{Z_n I_o}\right) = \sin^{-1}\left(\frac{-r}{x}\right) \tag{2e}$$

Inductor-Charging Stage [T2, T3] : V_C drops to zero at T_2 , S_1 turns on.

Initial Condition:

$$I_L(0) = I_o \cos \alpha \tag{3a}$$

State Equation:

$$L_r \frac{dI_L}{dt} = V_i \tag{3b}$$

Time Solution:

$$T_{23} = \frac{L_r I_o (1 - \cos \alpha)}{V_i} = \frac{1}{\omega}\frac{x}{r}(1 - \cos \alpha) \tag{3c}$$

Passive Stage [T3, T4] : I_L reaches I_o at T_3 , D_o cuts off.

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{4}$$

Table 3.1. (cont.)

Input power per cycle, Ei :

$$E_i = V_i I_o T_{01} + V_i \int_{T_1}^{T_2} I_L \, dt + V_i \int_{T_2}^{T_3} I_L \, dt + V_i I_o T_{34}$$

$$= V_i I_o (T_s - T_{12} - T_{23}) + V_i \int_{T_1}^{T_2} I_L \, dt + V_i \int_{T_2}^{T_3} I_L \, dt \qquad (5)$$

From Eq. (2c), (2d) and (2e),

$$\int_{T_1}^{T_2} I_L \, dt = \int_{T_1}^{T_2} I_o \cos \omega t \, dt = \frac{I_o}{\omega} \sin \alpha = \frac{I_o}{\omega} \left(- \frac{r}{x} \right) \qquad (6)$$

From Eq. (3c),

$$\int_{T_2}^{T_3} I_L \, dt = \frac{(I_o \cos \alpha + I_o)}{2} T_{23} = I_o \frac{(\cos \alpha + 1)}{2} \frac{1}{\omega} \frac{x}{r} (1 - \cos \alpha)$$

$$= \frac{I_o}{2\omega} \frac{x}{r} \sin^2 \alpha = \frac{I_o}{2\omega} \frac{r}{x} \qquad (7)$$

Therefore,

$$E_i = V_i I_o \left(T_s - \frac{\alpha}{\omega} - \frac{1}{\omega} \frac{x}{r} (1 - \cos \alpha) \right) + V_i \frac{I_o}{\omega} \left(- \frac{r}{x} \right) + V_i \frac{I_o}{2\omega} \left(\frac{r}{x} \right)$$

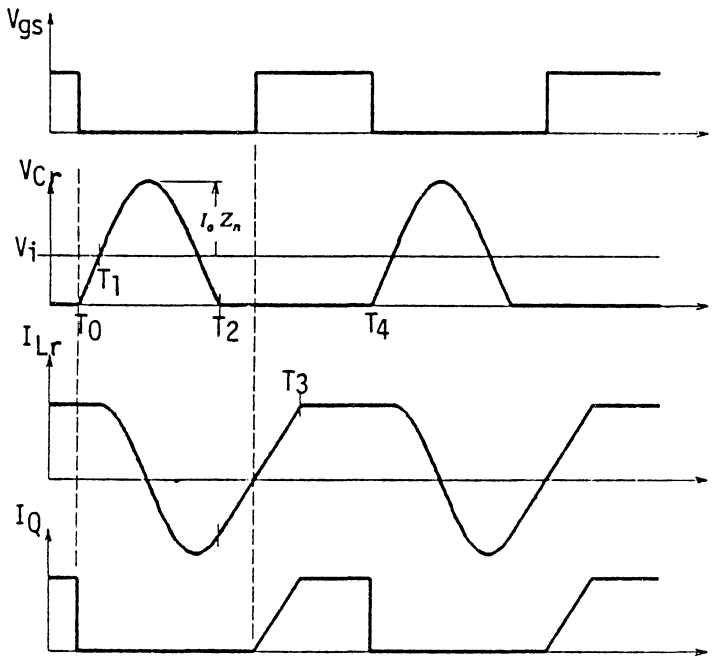
$$= V_i I_o T_s \left[1 - \frac{f_s}{2\pi f_n} \left(\alpha + \frac{r}{2x} + \frac{x}{r} (1 - \cos \alpha) \right) \right] \qquad (8)$$

Output power per cycle, Eo :

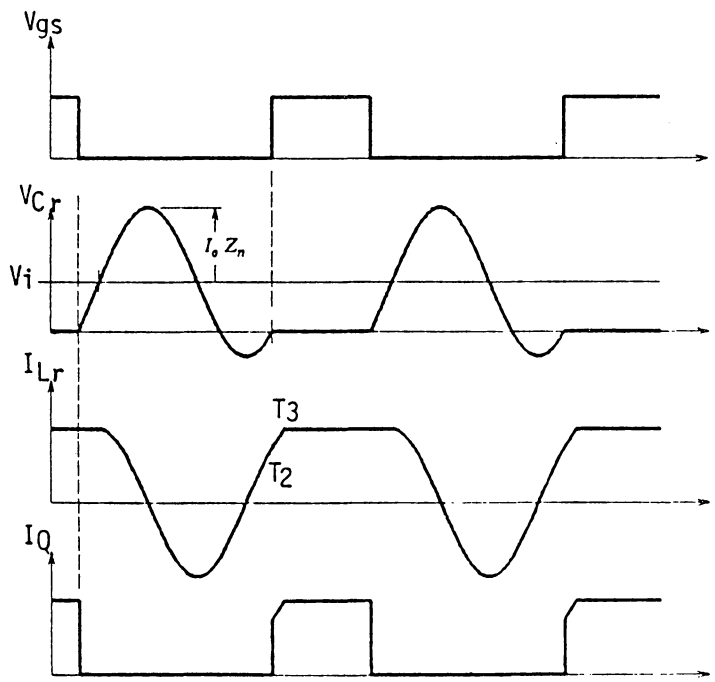
$$E_o = V_o I_o T_s \qquad (9)$$

By equating E_i and E_o,

$$\frac{V_o}{V_i} \equiv x = 1 - \frac{f_s}{2\pi f_n} \left[\alpha + \frac{r}{2x} + \frac{x}{r} (1 - \cos \alpha) \right] \qquad (10)$$

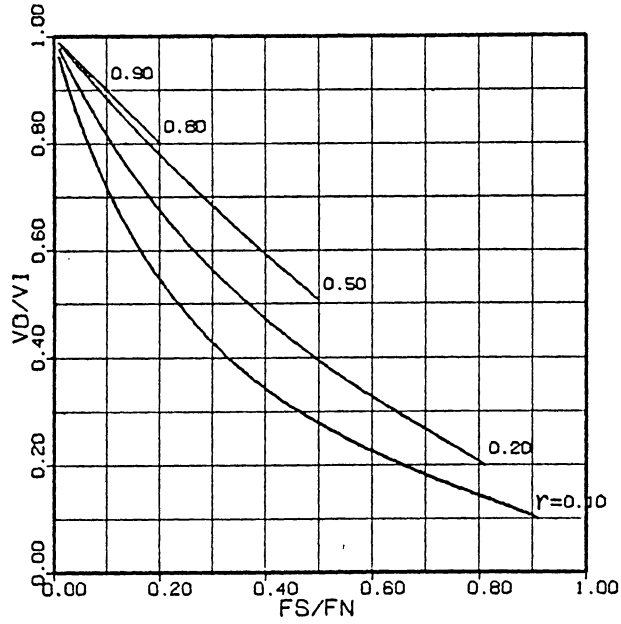


(a)

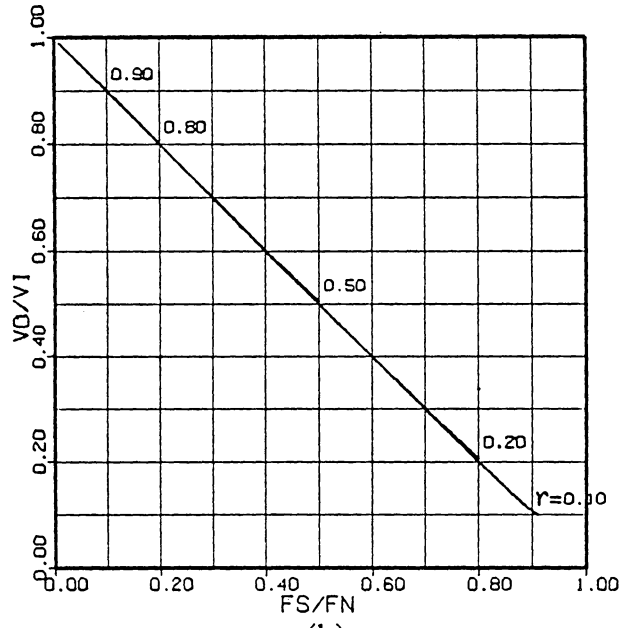


(b)

Fig. 3.7. Typical circuit waveforms of the ZVS, quasi-resonant buck converter in: (a) half-wave mode (b) full wave-mode



(a)



(b)

Fig. 3.8. DC voltage-conversion ratios of the ZVS, quasi-resonant buck converter in (a) half-wave mode (b) full-wave mode

Table 3.2. ZVS, Quasi-Resonant Buck/Boost Converter

Capacitor-Charging Stage [T0, T1] : S_1 turns off at T_0 .

Initial Condition:

$$V_C(0) = 0 \tag{1a}$$

State Equation:

$$C_r \frac{dV_C}{dt} = I_m \tag{1b}$$

Time Solution:

$$T_{01} = \frac{C_r(V_i + V_o)}{I_m} = \frac{1}{\omega}\frac{V_i + V_o}{Z_n I_m} \tag{1c}$$

Resonant Stage [T1, T2] : V_C reaches $(V_i + V_o)$ at T_1 , D_o conducts.

Initial Conditions:

$$I_L(0) = I_m ; \quad V_C(0) = V_i + V_o \tag{2a}$$

State Equations:

$$L_r \frac{dI_L}{dt} = V_i + V_o - V_C ; \quad C_r \frac{dV_C}{dt} = I_L \tag{2b}$$

Time Solutions:

$$I_L(t) = I_m \cos \omega t \tag{2c}$$

$$V_C(t) = V_i + V_o + Z_n I_m \sin \omega t \tag{2d}$$

$$T_{12} = \frac{\alpha}{\omega} \text{ , where } \alpha = \sin^{-1}\left(\frac{-V_i - V_o}{Z_n I_m}\right) \tag{2e}$$

Inductor-Charging Stage [T2, T3] : V_C drops to zero at T_2 , S_1 turns on.

Initial Condition:

$$I_L(0) = I_m \cos \alpha \tag{3a}$$

State Equation:

$$L_r \frac{dI_L}{dt} = V_i + V_o \tag{3b}$$

Time Solution:

$$T_{23} = \frac{1}{\omega}\frac{Z_n I_m}{V_i + V_o}(1 - \cos \alpha) \tag{3c}$$

Passive Stage [T3, T4] : I_L reaches I_m at T_3 , D_o cuts off.

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{4}$$

Table 3.2. (cont.)

Input power per cycle, Ei :

$$E_i = V_i I_m T_{01} + V_i \int_{T_1}^{T_2} I_L \, dt + V_i \int_{T_2}^{T_3} I_L \, dt + V_i I_m T_{34} \tag{5}$$

From Eqs. (2c), (2d), and (2e),

$$\int_{T_1}^{T_2} I_L \, dt = \int_{T_1}^{T_2} I_m \cos \omega t \, dt = \frac{I_m}{\omega} \sin \alpha \tag{6}$$

From Eq. (3c),

$$\int_{T_2}^{T_3} I_L \, dt = \frac{I_m + I_m \cos \alpha}{2} \frac{Z_n I_m (1 - \cos \alpha)}{\omega (V_i + V_o)} = \frac{Z_n I_m^2 \sin^2 \alpha}{2 \omega (V_i + V_o)} \tag{7}$$

From Eqs. (5), (6), and (7),

$$E_i = V_i I_m \left[T_{01} + T_{34} + \frac{\sin \alpha}{\omega} + \frac{Z_n I_m \sin^2 \alpha}{2\omega (V_i + V_o)} \right] \equiv V_i I_m T_A \tag{8}$$

Output power per cycle, Eo :

$$E_o = V_o \int_{T_1}^{T_2} (I_m - I_L) \, dt + V_o \int_{T_2}^{T_3} (I_m - I_L) \, dt \tag{9}$$

Similarly, by using Eqs. (2c), (2d), (2e) and (3c),

$$E_o = V_o I_m \left[\frac{\alpha}{\omega} - \frac{\sin \alpha}{\omega} + \frac{Z_n I_m (1 - \cos \alpha)^2}{2\omega (V_i + V_o)} \right] \equiv V_o I_m T_B \tag{10}$$

Notice that,

$$T_A + T_B = T_{01} + T_{34} + \frac{\alpha}{\omega} - \frac{Z_n I_m \cos \alpha}{\omega (V_i + V_o)} = T_s \tag{11}$$

By equating E_i and E_o using Eqs. (8) and (10),

$$x \equiv \frac{V_o}{V_i} = \frac{T_A}{T_B} = \frac{T_s}{T_B} - 1 \quad \rightarrow \quad T_B = \frac{V_i T_s}{V_i + V_o} \tag{12}$$

Also,

$$E_o = \frac{V_o^2 T_s}{R} = V_o I_m T_B = \frac{V_i V_o I_m T_s}{V_i + V_o} \tag{13}$$

Therfore,

$$\frac{I_m Z_n}{V_i + V_o} = \frac{x}{r} \quad \text{where } r \equiv \frac{R}{Z_n} \tag{14}$$

Using Eqs. (8) to (14),

$$x = \frac{1}{\frac{f_s}{2\pi f_n} \left[\alpha + \frac{r}{2x} + \frac{x}{r} (1 - \cos \alpha) \right]} - 1 \tag{15}$$

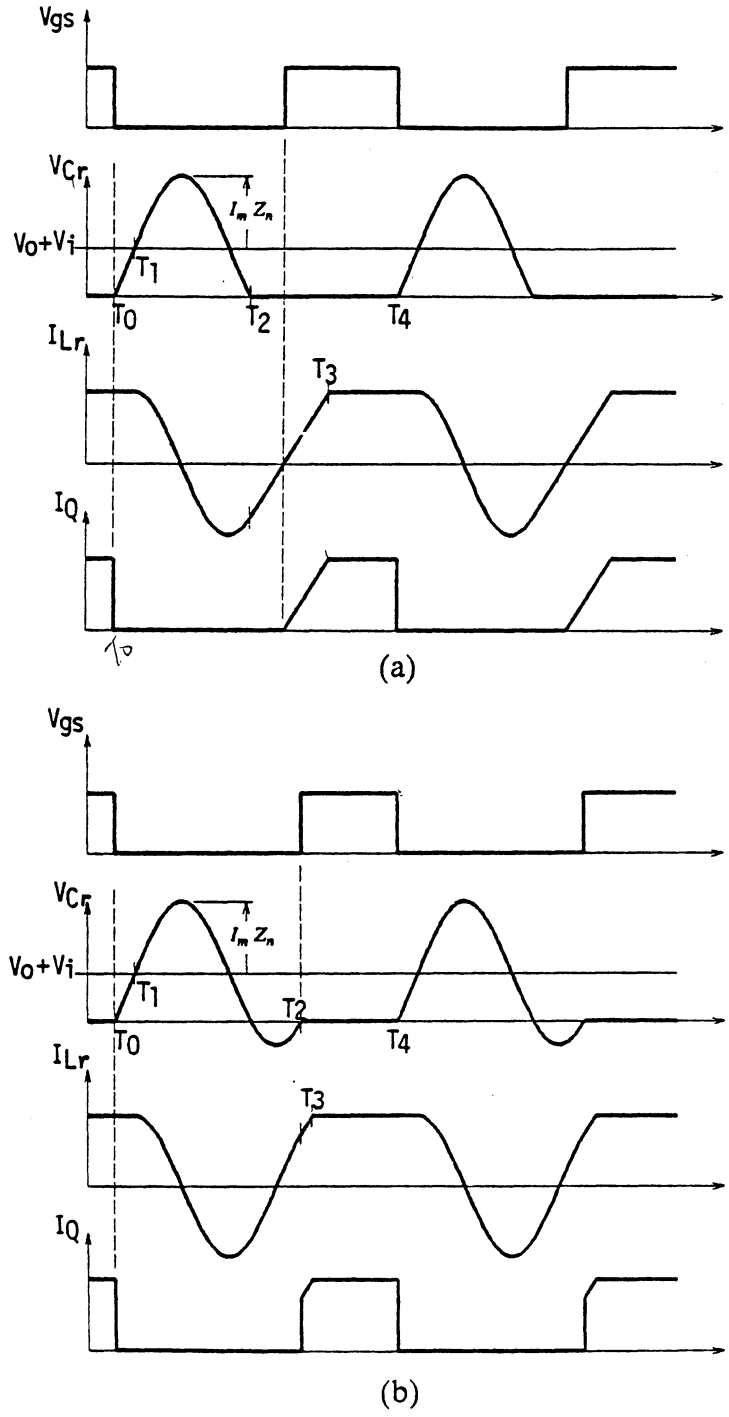
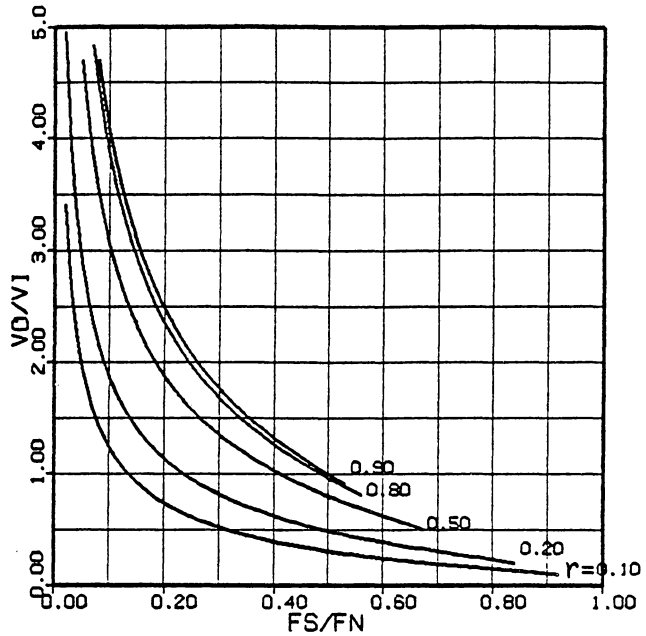
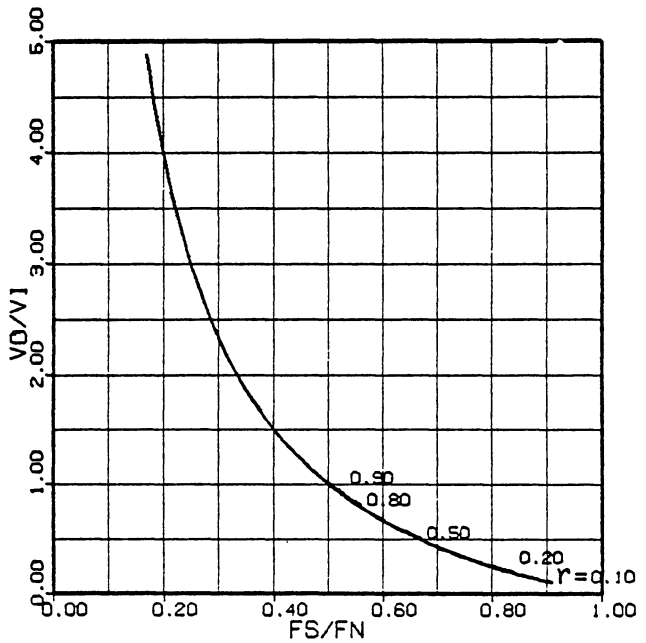


Fig. 3.9. Typical circuit waveforms of the ZVS, quasi-resonant buck/boost converter in: (a) half-wave mode (b) full wave-mode



(a)



(b)

Fig. 3.10. DC voltage-conversion ratios of the ZVS, quasi-resonant buck/boost converter in (a) half-wave mode (b) full-wave mode

3.6. Design Considerations and Experimental Results

3.6.1. The Switching Miller Effect

A MOSFET device has an insulated gate structure which results in relatively high gate-to-drain capacitance, C_{gd} , and gate-to-source capacitance, C_{gs} . Along with the junction's depletion capacitance of C_{ds} , these capacitances play important roles in the switching behavior of MOSFETs.

In a typical resistively loaded switching circuit, as shown in Fig. 3.11, assume the gate voltage is switched between V_{G1} and $-V_{G2}$ and the drain voltage is switched between 0 and V_D . Before the turn-on of the MOSFET, the voltages on capacitances C_{gd} , C_{gs} , and C_{ds} are $(V_D + V_{G2})$, $-V_{G2}$, and V_D , respectively, as shown in Fig. 3.11a. After the MOSFET is completely turned on by the gate drive, the voltages of the capacitances become $-V_{G1}$, V_{G1} , and 0, respectively, as shown in Fig. 3.11b. The voltage changes are $-(V_D + V_{G1} + V_{G2})$, $(V_{G1} + V_{G2})$, and $-V_D$. The gate-drive circuit must supply charging currents to C_{gd} as well as to C_{gs} . This phenomenon of higher gate capacitance due to the effect of C_{gd} is similar to the ***Miller effect*** occurring in amplifier circuits, although, in this case it is of a large-signal nature.

Figure 3.12a shows the waveforms of a MOSFET when switched under an ***unloaded (open-drain)*** condition. The gate voltage is switched between +12V and -5V. A small step in the V_{gs} waveform during turn-on indicates the coupling

between the drain-source channel and the gate terminal through C_{gd} . In this circuit, since V_D is zero, there is only a slight switching Miller effect which can barely be seen in the waveforms.

To simulate a resistively loaded switching condition, a load resistor of 100Ω is inserted between a 40V voltage source and the drain terminal. The waveforms are shown in Fig. 3.12b. The longer step in the V_{gs} waveform and the longer charging time in the gate-current waveform at turn-on clearly show the phenomenon of the Miller effect.

Comparing the two cases described above, it can be seen that the Miller Effect is directly related to the off-state, drain-source voltage of the MOSFET immediately prior to its turn-on. Since the Miller effect is proportional to the rate of change of the drain voltage during turn-on, it is much aggravated in high-voltage switching applications and may cause a sluggish turn-on and even uncontrolled oscillation in the gate-drive circuit.

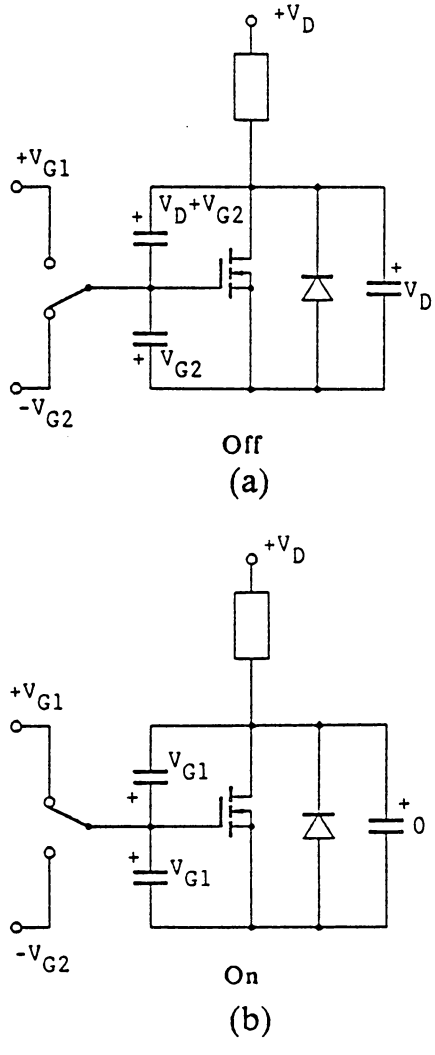
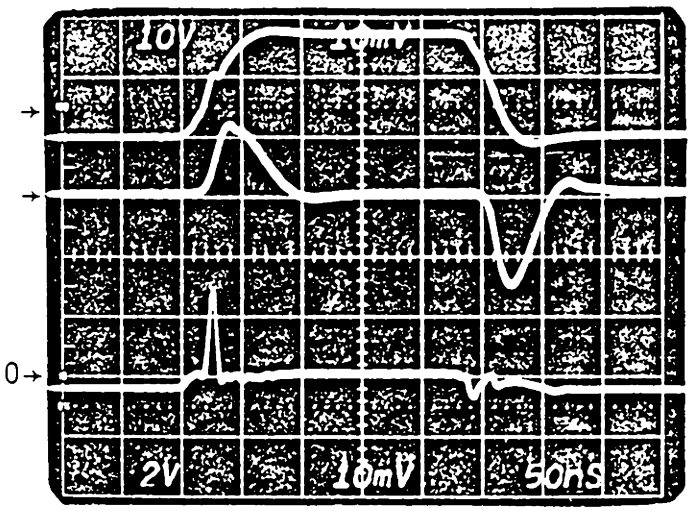
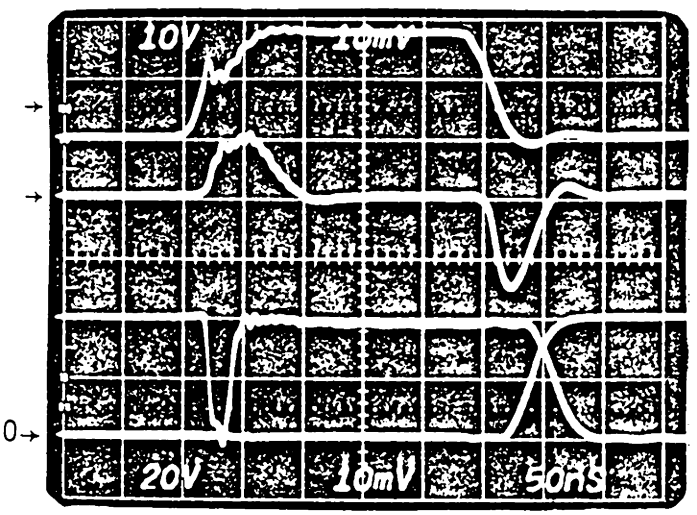


Fig. 3.11. A resistive-load switching circuit using a MOSFET
(a) voltage states before turn-on
(b) voltage states after turn-on



(a)



(b)

Fig. 3.12. Typical waveforms of a MOSFET switching
(a) under unloaded condition
upper waveform : V_{gs} (10V/Div.)
middle waveform : I_g (0.5A/Div.)
lower waveform : V_{ds} (2V/Div.)
(b) under resistive load condition
1st waveform : V_{gs} (10V/Div.)
2nd waveform : I_g (0.5A/Div.)
3rd waveform : V_{ds} (20V/Div.)
4th waveform : I_{ds} (0.2A/Div.)

3.6.2. Experimental Verifications

To verify the analytical results derived in Sec. 3.3, a ZVS, quasi-resonant boost converter was breadboarded. The circuit's schematic diagram is shown in Fig. 3.13. The characteristic impedance and resonant frequency are set at 100 Ω and 2MHz, respectively, which give the approximate values of L_r at 8μH, and C_r at 800pF. An IRF-730 MOSFET (400V, 5.5A, Rd = 1Ω) is selected as the switching device, Q_1 . Its output junction capacitance is about 150pF measured at 100V and above. To obtain a C_r of 800pF, an external capacitor, C_2 , of 680pF is connected in parallel with Q_1 . The internal source-drain diode of the MOSFET is used as the feedback diode, D_1 .

Major waveforms of the circuit operating at 1MHz and with a load resistance of 100 Ω are shown in Fig. 3.14. Because extra wire length is used to allow the insertion of a current probe to measure the current through Q_1 and C_r , higher stray inductances are introduced which cause some parasitic ringing as shown in the current waveforms. Other than the ringing, the waveforms are rather smooth and free of switching noise. This clearly demonstrates that the zero-voltage switching technique not only eliminates the switching losses, but also accomplishes a significant reduction in the electro-magnetic interference.

The same circuit operated under different load and switching frequency conditions are summarized in Table 3.3. Waveforms at load resistances of 50Ω and 100Ω are shown in Fig. 3.15.

Figure 3.15f shows when the load current is too low, the V_{ds} waveform no longer reaches zero and the zero-voltage switching property is lost. The ringing in the I_{ds} waveform is the result of resonant oscillation between external capacitor C_r and the stray inductance in the circuit when the MOSFET is turned on under a non-zero voltage condition. From Table 3.3, it can also be seen that when the circuit is not operating in the zero-voltage switching range, such as the cases when $R = 250\Omega$ and $f_s = 1.2$MHz and 1.6MHz, the efficiency becomes lower because of increased turn-on loss.

When this circuit is modified by adding a series blocking diode, it becomes a full-wave, ZVS, quasi-resonant boost converter. The circuit diagram is shown in Fig. 3.16. A TRW DSR-5500X, rated at 600V, 3A, is chosen as the series diode because of its fast reverse-recovery speed ($t_{rr} = 35$ns).

Major waveforms of the circuit operating at 1MHz and with a load resistance of 100Ω are shown in Fig. 3.17. Except for some parasitic ringing and the V_{ds} waveform, all other waveforms are very close to those predicted by the dc analysis described in previous sections.

The full-wave circuit operated under different load and switching-frequency conditions are summarized in Table 3.4. Waveforms at resistances of 50Ω and 100Ω are shown in Fig. 3.18. Notice that the waveform of V_{ds} is not clamped at its peak value during the off-time as predicted by the idealized circuit model. Instead, it follows the waveform of V_{Cr} for a while after both waveforms fall from their peak values. Voltage V_{ds} may drop to zero if the load current is large enough, as shown in the case of Fig. 3.18a. This peculiar behavior of the

V_{ds} waveform can be explained if the junction capacitance of the series diode is considered.

The series diode, DSR-5500x, is a high-voltage, p-n junction diode. When reverse biased, a depletion-region capacitance is developed across the p-n junction. This capacitance is nonlinear, it has a higher value under a low reverse-biasing voltage than when under a high reverse-biasing voltage. Typical diodes exhibit a capacitance ratio of greater than 3 to 1 as the reverse voltage varies from 2V to 30V [G5]. With the junction capacitance of this diode (C_2) included, the circuit diagram is now shown in Fig. 3.19.

After MOSFET Q_1 turns off, the inductive current flows into the external capacitor, C_r, as well as the junction capacitance C_1 of Q_1. Since diode D_2 is on, voltage V_{Cr} across C_r, is the same as the voltage across C_1, V_{C1} (= V_{ds}), as shown in Fig. 3.19a. After reaching the peak, both V_{Cr} and V_{C1} starts to drop. If C_2 did not exist, then V_{Cr} would be clamped by D_2 at its peak value until Q_1 turns on later. In practice, even after D_2 is reverse biased, C_2 will provide a conducting path for the discharging of C_1. Effectively, C_1 and C_2 forms a non-linear voltage divider during the period when V_{Cr} drops from its peak (see Fig. 3.19b).

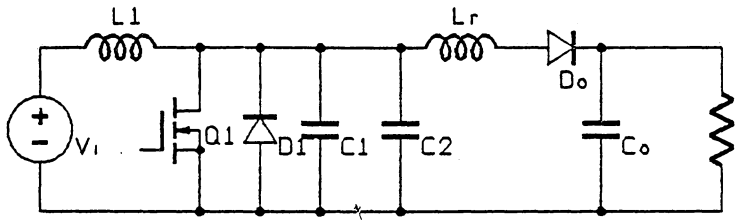
Notice that both C_1 and C_2 have non-linear capacitances. Their values are higher when the biasing voltage is low, and lower when the biasing voltage is high. Immediately after V_{C1} and V_{Cr} reach the peak, C_2 has a larger initial value, V_{C2} builds up slowly. As V_{Cr} drops, V_{C1} also discharges through C_2, since C_2 provides a high-conductivity path. After stored charges on C_2 are built up, the capacitance of C_2 begins to decrease, and voltage across C_2 rises at a faster rate.

The difference between V_{Cr} and V_{C1} is the voltage across C_2, as can be seen in the top waveforms in Fig. 3.17b.

V_{C1} (= V_{ds}) can be discharged completely if the load current is large enough. For example, in Fig. 3.18a, where $R = 50\Omega$, $f_s = 0.8$MHz, and $I_o = 0.78$A, V_{C1} drops to zero completely and is clamped by the forward conduction of the internal body diode of Q_1, D_1, as shown in Fig. 3.19c. Also in the waveforms of Fig. 3.18a, a negative current spike appears on the I_{ds} waveform, which is the reverse-recovery current through the p-n junction of the series diode when voltage across C_2 rises sharply. In this case, the MOSFET can turn on under a zero-voltage condition, which can be seen in the waveforms in Fig. 3.18a.

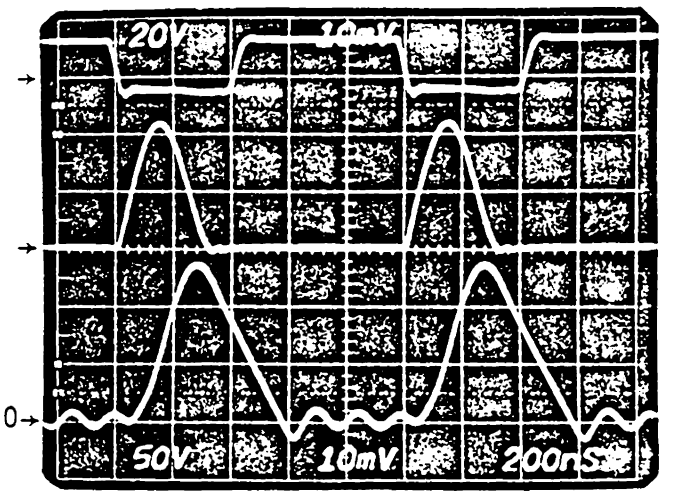
The comparison between the measured voltage-conversion ratios and the theoretically predicted values for the half-wave and the full-wave mode of operations are shown in Fig. 3.20a and 3.20b, respectively.

An interesting feature in the full-wave mode of operation is that, theoretically, all energy stored in the junction capacitance C_1 (C_{ds}), would be trapped and dissipated as heat. In reality, part or all of this energy can be recovered through the reverse recovery of the series diode, D_2, and through the depletion-region capacitance, C_2. Experimental results in Table 3.4 also show a considerable reduction in the load sensitivity compared with Table 3.3. However, whether this feature of recovering capacitive energy through the depletion-region capacitance or the reverse recovery of the series diode can be utilized to its full advantage remains a subject of future study.

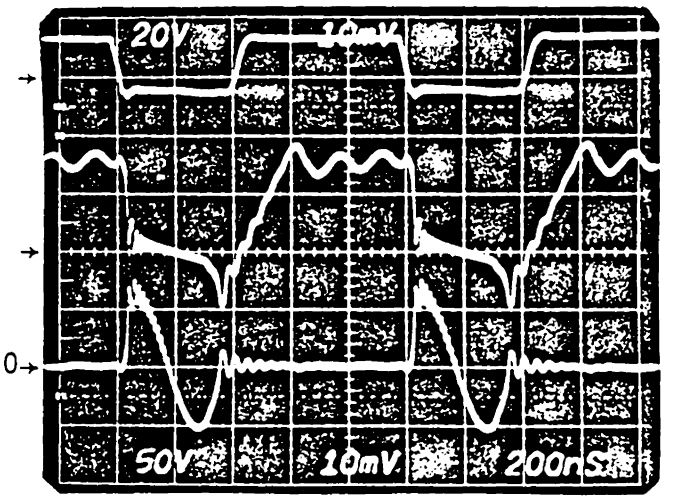


Q1+D1+C1 = IRF 730
Do = TRW DSR-5500X
L1 = 200 µH Lr = 8 µH
C2 = 680 pF Co = 10 µF
fn = 2MHz Zn = 100 Ω

Fig. 3.13. A breadboard implementation of the half-wave, ZVS, quasi-resonant boost converter



(a)

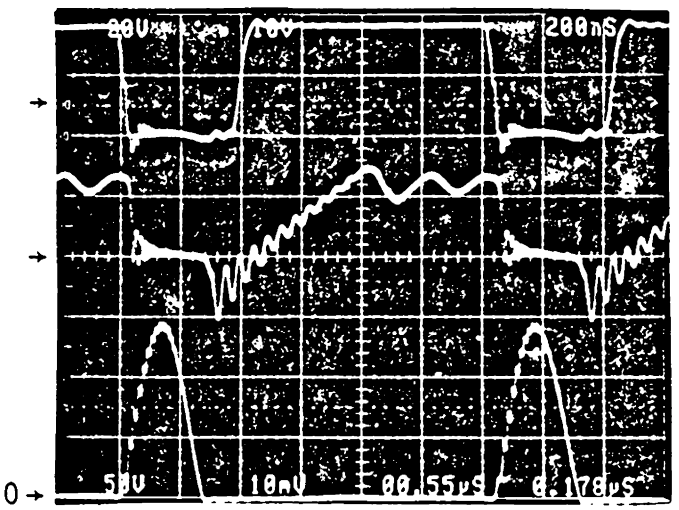


(b)

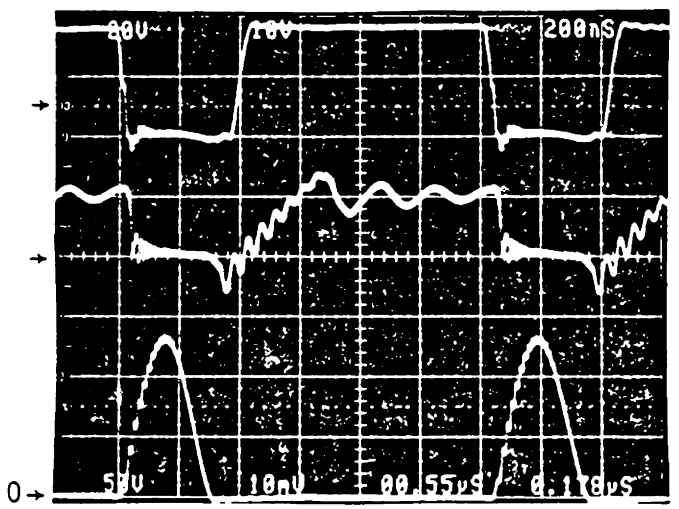
Fig. 3.14. Waveforms from the circuit of Fig. 3.13.
Vi = 20V, R = 100Ω, fs = 1MHz
(a) upper waveform : V_{gs} (20V/Div.)
middle waveform : V_{ds} (50V/Div.)
lower waveform : I_{Lr} (0.5A/Div.)
(b) upper waveform : V_{gs} (20V/Div.)
middle waveform : I_{ds} (0.5A/Div.)
lower waveform : I_{Cr} (0.5A/Div.)

Table 3.3 Measured circuit parameters from the circuit in Fig. 3.13 under different load conditions

	Vi (V)	Ii (A)	Pi (W)	Vo (V)	Io (A)	Po (W)	efficiency
1.6 MHz							
20Ω	20	0.92	18.4	18.5	0.91	16.8	91.5%
50Ω	20	0.55	11.	22.3	0.46	10.3	93.3%
80Ω	20	0.5	10.	26.6	0.34	9.04	90.4%
100Ω	20	0.42	8.4	27.	0.28	7.56	90. %
250Ω	20	0.26	5.2	32.5	0.14	4.55	87.5%
1.2 MHz							
20Ω	20	0.95	19.	18.7	0.92	17.2	90.5%
50Ω	20	0.72	14.4	25.6	0.52	13.3	92.4%
80Ω	20	0.74	14.8	32.5	0.42	13.7	92.2%
100Ω	20	0.64	12.8	34.	0.35	11.9	93.2%
250Ω	20	0.37	7.4	39.7	0.17	6.75	91.2%
0.8 MHz							
20Ω	20	1.47	29.4	22.6	1.1	24.9	84.6%
50Ω	20	1.27	25.4	33.3	0.66	22.	86.5%
80Ω	20	1.1	22.	39.3	0.5	19.7	89.3%
100Ω	20	1.06	21.2	43.3	0.44	19.1	89.9%
250Ω	20	0.69	13.8	54.9	0.24	13.2	95.5%
0.4 MHz							
20Ω	10	1.41	14.1	14.9	0.74	11.0	78.2%
50Ω	10	1.28	12.8	22.6	0.45	10.2	79.5%
80Ω	10	1.2	12.	27.9	0.36	10.	83.7%
100Ω	10	1.16	11.6	30.7	0.32	9.89	85.2%
250Ω	10	0.93	9.3	44.4	0.18	7.99	85.9%

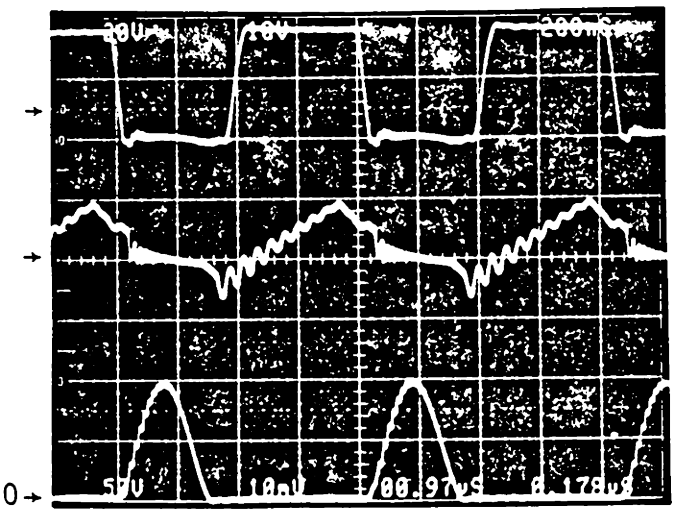


(a)

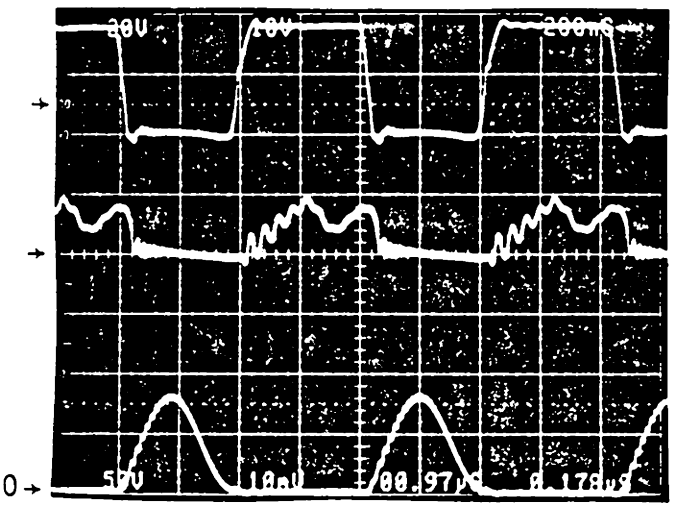


(b)

Fig. 3.15. Waveforms from the circuit of Fig. 3.13.
upper waveform : V_{gs} (10V/Div.)
middle waveform : I_{ds} (1A/Div.)
lower waveform : V_{ds} (50V/Div.)
(a) R = 50Ω, fs = 800kHz (b) R = 100Ω, fs = 800kHz

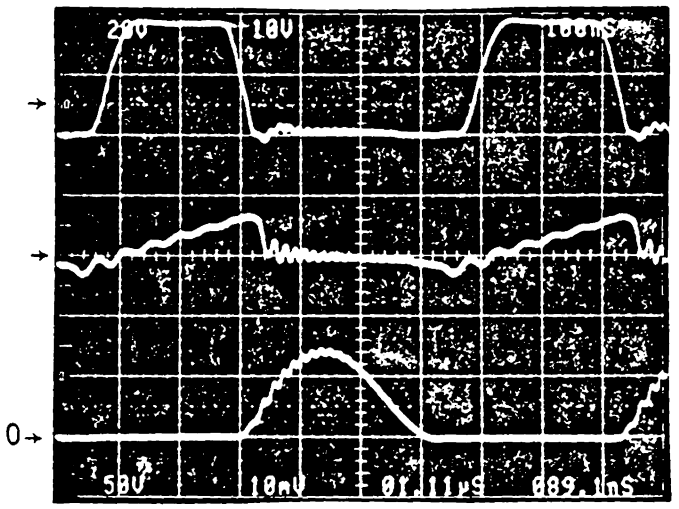


(c)

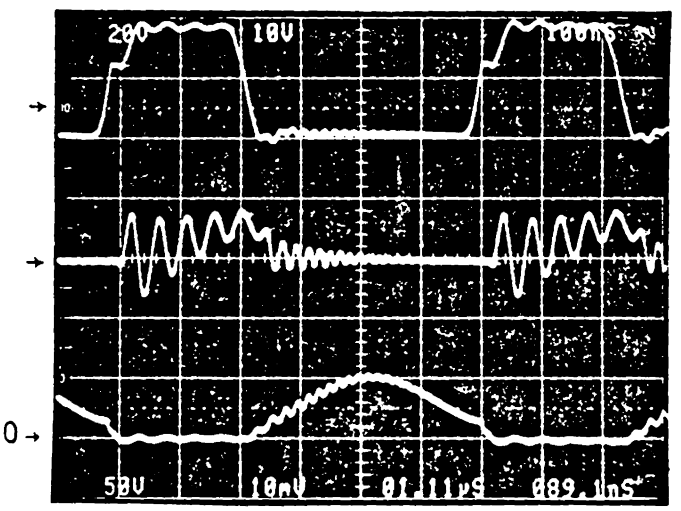


(d)

Fig. 3.15. (cont.)
(c) $R = 50\Omega$, $fs = 1.2MHz$ (d) $R = 100\Omega$, $fs = 1.2MHz$

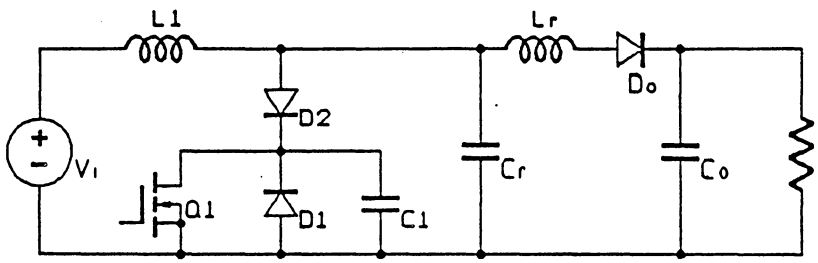


(e)



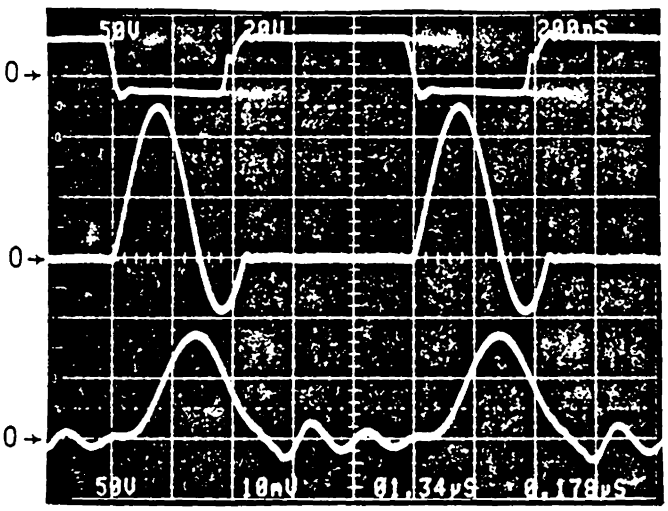
(f)

Fig. 3.15. (cont.)
(e) $R = 50\Omega$, $fs = 1.6MHz$ (f) $R = 100\Omega$, $fs = 1.6MHz$

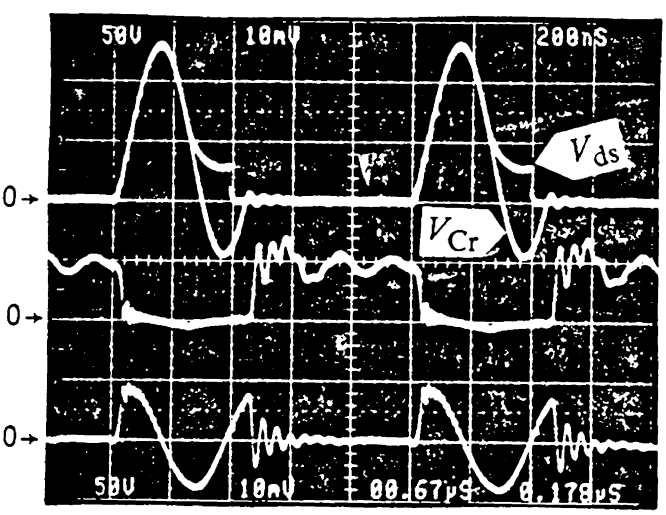


Q1+D1+C1 = IRF 730
D2, Do = TRW DSR-5500X
L1 = 200 µH Lr = 8 µH
Cr = 680 pF Co = 10 µF
fn = 2MHz Zn = 100 Ω

Fig. 3.16. A breadboard implementation of the full-wave, ZVS, quasi-resonant boost converter



(a)

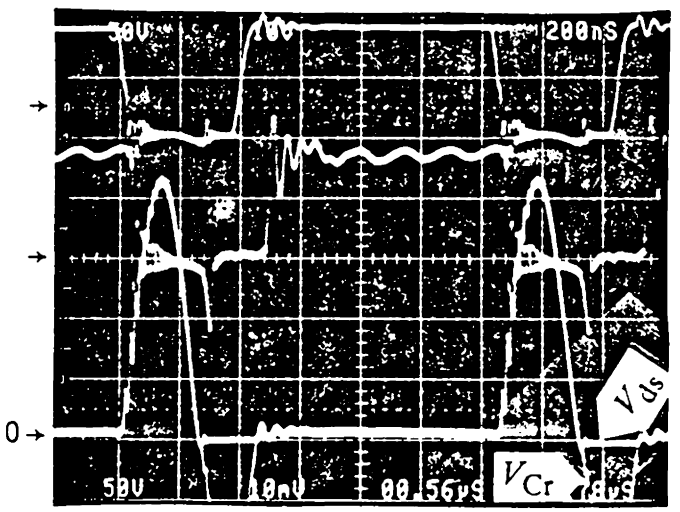


(b)

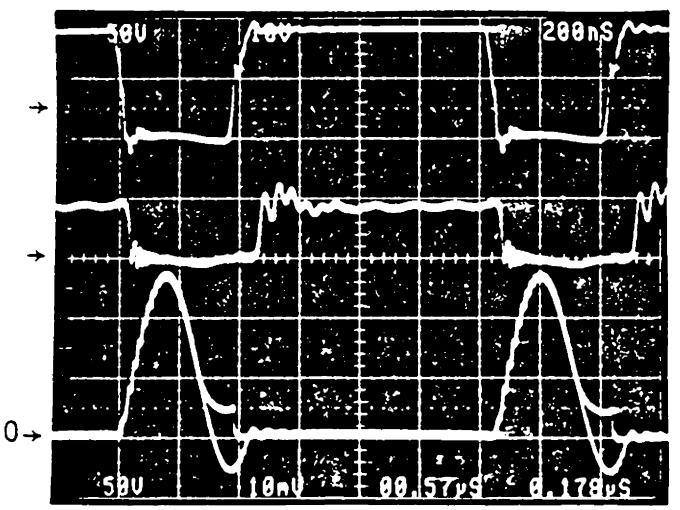
Fig. 3.17. Waveforms from the circuit of Fig. 3.16.
Vi = 20V, R = 100Ω, fs = 1MHz
(a) upper waveform : V_{gs} (20V/Div.)
middle waveform : V_{ds} (50V/Div.)
lower waveform : I_{Lr} (1A/Div.)
(b) 1st waveform : V_{ds} (50V/Div.)
2nd waveform : V_{Cr} (50V/Div.)
3rd waveform : I_{ds} (1A/Div.)
4th waveform : I_{Cr} (1A/Div.)

Table 3.4 Measured circuit parameters from the circuit in Fig. 3.16 under different load conditions

	Vi (V)	Ii (A)	Pi (W)	Vo (V)	Io (A)	Po (W)	efficiency
1.6 MHz							
20Ω	20	1.56	31.2	22.9	1.12	25.7	82.2%
50Ω	20	0.72	14.4	25.5	0.51	13.	90.3%
80Ω	20	0.46	9.2	26.0	0.33	8.58	93.3%
100Ω	20	0.39	7.8	26.7	0.27	7.21	92.4%
250Ω	20	0.24	4.8	31.8	0.14	4.45	92.7%
1.2 MHz							
20Ω	20	2.33	46.6	25.8	1.24	32.0	68.6%
50Ω	20	1.3	26.0	32.2	0.64	20.6	79.2%
80Ω	20	0.83	16.6	34.1	0.44	15.	90.4%
100Ω	20	0.69	13.8	34.9	0.36	12.7	91. %
250Ω	20	0.34	6.8	38.1	0.16	6.1	89.6%
0.8 MHz							
50Ω	20	2.1	42.	39.7	0.78	31.0	73.7%
80Ω	20	1.62	32.2	45.8	0.58	26.6	82.5%
100Ω	20	1.38	27.6	47.9	0.49	23.5	85.0%
250Ω	20	0.66	13.2	52.8	0.22	11.6	88.0%
0.4 MHz							
50Ω	5	1.22	6.12	10.9	0.22	2.4	39.%
80Ω	5	1.03	5.15	14.3	0.18	2.57	50.%
100Ω	5	0.91	4.55	15.8	0.16	2.53	55.6%
250Ω	5	0.48	2.4	20.5	0.09	1.05	76.8%

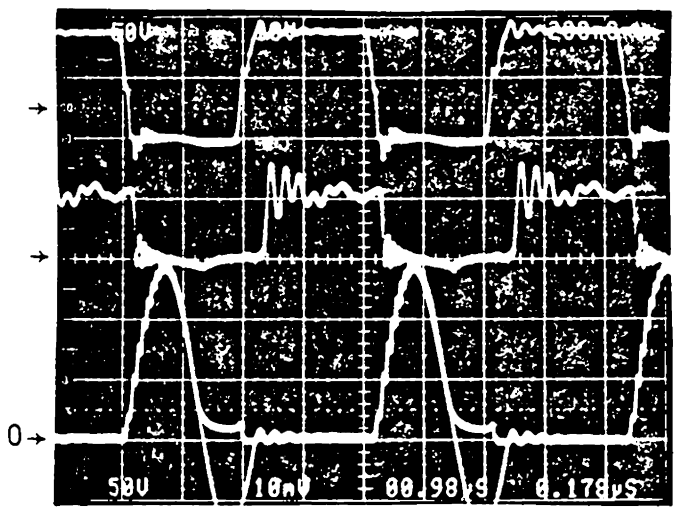


(a)



(b)

Fig. 3.18. Waveforms from the circuit of Fig. 3.16.
1st waveform : V_{gs} (10V/Div.)
2nd waveform : I_{ds} (1A/Div.)
3rd waveform : V_{ds} (50V/Div.)
4th waveform : V_{Cr} (50V/Div.)
(a) R = 50Ω, fs = 800kHz (b) R = 100Ω, fs = 800kHz



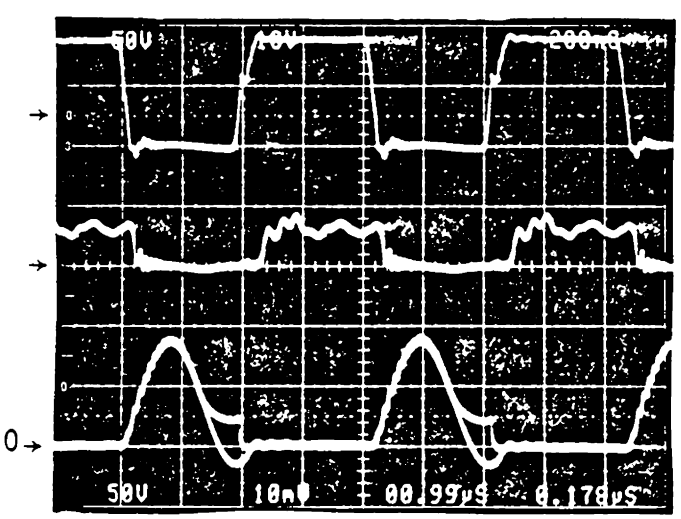
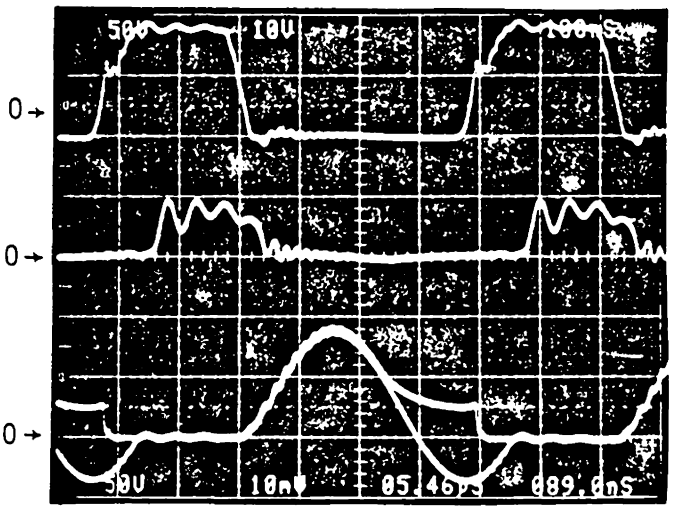
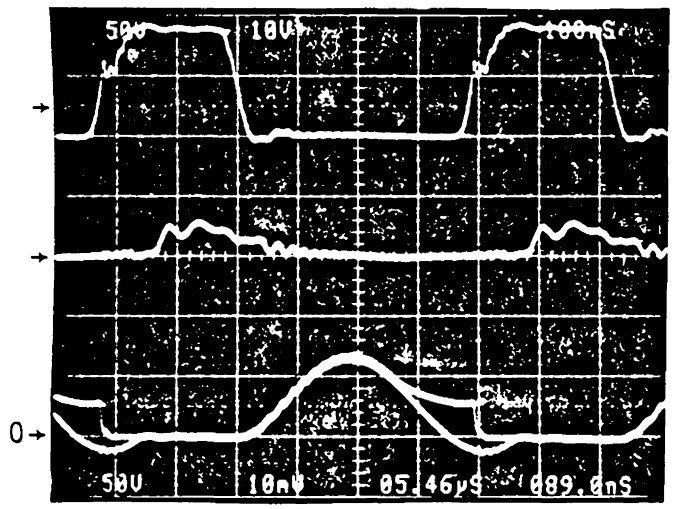


Fig. 3.18. (cont.)
(c) $R = 50\Omega$, $fs = 1.2MHz$ (d) $R = 100\Omega$, $fs = 1.2MHz$



(e)



(f)

Fig. 3.18. (cont.)
(e) $R = 50\Omega$, $fs = 1.6MHz$ (f) $R = 100\Omega$, $fs = 1.6MHz$

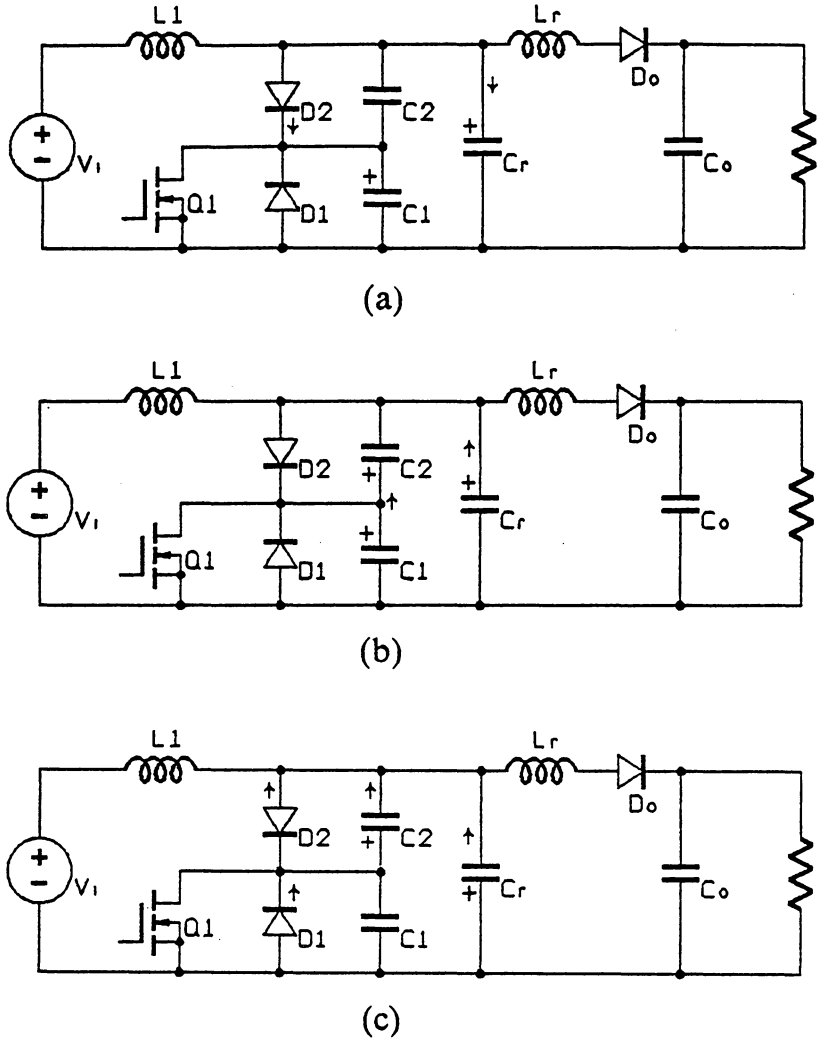
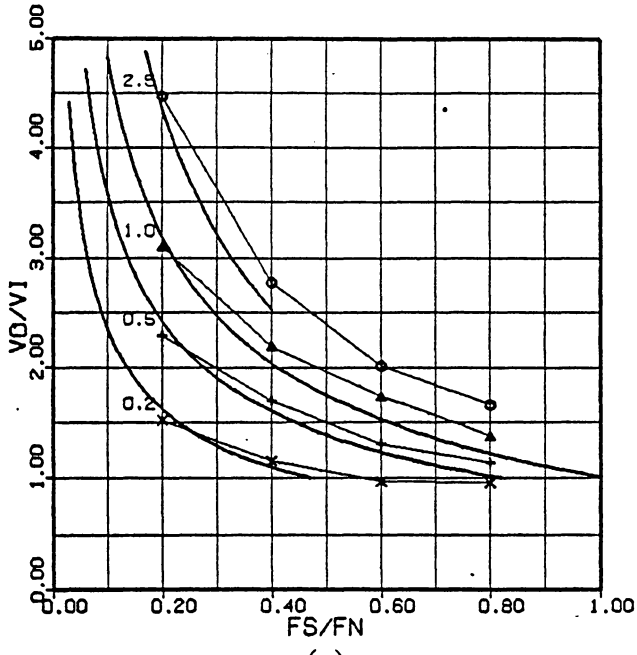
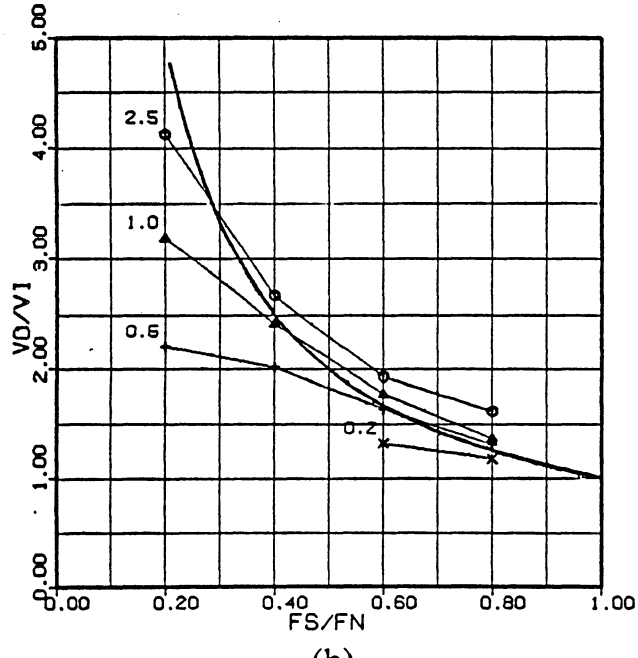


Fig. 3.19. The effect of diode's junction capacitance on the full-wave mode of operation
(a) V_{Cr} increasing
(b) V_{Cr} decreasing
(c) V_{Cr} drops below zero and V_{ds} drops to zero



(a)



(b)

Fig. 3.20. Measured values vs. predicted values in the voltage-conversion ratio of the ZVS, quasi-resonant boost converter
(a) half-wave mode (b) full-wave mode

3.7. Summary

For very high frequency power converters, only the MOSFETs can provide sufficient switching speed. Since the MOSFETs are majority-carrier devices, the turn-off loss due to the carrier-recombination phenomenon is no longer a problem. However, the turn-on switching loss due to the discharging of parasitic junction capacitances becomes the dominant loss when the switching frequency is raised beyond 1MHz.

To eliminate the capacitive turn-on loss, a waveform-shaping technique which is called the zero-voltage switching (ZVS) technique is proposed. In addition to the elimination of capacitive turn-on loss, this technique also provides the following advantages:

- It eliminates the capacitive turn-on loss while keeping the conduction loss to minimum.

- Turn-on at zero drain-to-source voltage avoids the switching Miller effect and eliminates many side effects that it causes, such as current spikes in the gate drive, higher gate-drive switching loss, slower turn-on speed, severe EMI and noises generated.

- The internal body-drain diode of the MOSFET can be utilized as the anti-parallel diode required in the half-wave mode of operation.

- The elimination of switching Miller effect and the reduction in EMI and noise simplifies the design of the gate-drive circuit.

On the other hand, these ZVS, quasi-resonant converters have two limitations:

- To cover a wide range of load variation, the design of a ZVS, quasi-resonant converter requires the peak value of the off-state voltage on the power switch to be about four to five times the input voltage. In other words, the off-state voltage across the switch is about twice as high as that of a corresponding PWM converter. This higher voltage stress requires the use of a high-voltage MOSFET switch which, generally, has a higher on-resistance.

- In general, a complete full-wave mode of operation is difficult to implement, therefore, the output voltage is load sensitive. To regulate the output voltage against load variation, a control scheme using wide-range frequency modulation is required.

Actual implementations of the zero-voltage switching technique have shown excellent performance. A 5MHz, 25W, 50V to 5V, ZVS, quasi-resonant flyback converter has been built. The circuit utilizes the leakage inductance of the transformer and the parasitic junction capacitance as the resonant-tank elements. When operated at full load, it delivers an efficiency of 83%. More detail on this circuit is presented in Chapter 5.

Recent studies also show the ZVS technique is capable of operating at even higher frequencies. A breadboard circuit operating in the 10MHz-15MHz range has been implemented [C18].

4. TOPOLOGY VARIATIONS OF QUASI-RESONANT CONVERTERS

The waveform-shaping techniques of zero-current and zero-voltage switching provide the frameworks of generating two new families of quasi-resonant converters. Given a conventional PWM converter, simply by replacing the power switch by a current-mode or a voltage-mode resonant switch, a quasi-resonant converter operating in the zero-current switching scheme or in the zero-voltage switching scheme is obtained.

In the process of seeking a large number of PWM converters to generate their counterpart topologies in the quasi-resonant converter families, questions were raised about what are the basic PWM converter topologies and what topological variation and synthesis methods are available in generating new converter circuits from the basic converter topologies. Once the basic PWM converter topologies and the topological variation and synthesis methods are identified, many new PWM converter topologies can be derived. By applying proper replacement of

power switches in these PWM converter topologies by resonant switches, a large variety of quasi-resonant converter topologies can be generated.

Many papers have been published dealing with converter topologies, their structural properties, topological variations and synthetical approaches in generating new topologies [F1-F25]. However, some of the results obtained have never been proved properly, some of the the approaches used or the claims made are not consistent, and some even have no solid ground in terms of theoretical rigorousness.

In the research work related to this dissertation, a study was made by the author to probe the basic topological properties in converter circuits. It was discovered that certain physical constraints imposing on the topological structure of converter circuits exist. Through the derivation of these constraints, it can be shown that only six basic PWM converter topologies exist.

With these six basic converter topologies, one can derive many other topologies by employing converter topological variation and synthesis approaches, such as finding the dual network, bilateral inversion, adding an isolation transformer, adding coupled inductors, and cascading or paralleling two or more converters. Furthermore, through proper replacement of power switches in these PWM converter topologies by current-mode or voltage-mode resonant switches, corresponding quasi-resonant converter topologies can be derived.

In Sec. 4.1, the constraints imposing on the converter topologies are first derived. Through the proof of these constraints, it has been concluded that there exist only six basic converter topologies. Furthermore, some of the concepts pre-

sented in this section are proved to be very useful in understanding topological properties in converter circuits.

Section 4.2 summaries the most important topological variation methods in generating new converter circuits. Synthesis approaches of combining two or more converter circuits are discussed in Sec. 4.3.

In Sec. 4.4, the technique and the procedure of transforming PWM converter circuits into ZCS or ZVS quasi-resonant converters are described.

The duality property in converter topologies has been proved to be one of the most important topological properties in the converter circuits. It not only is a powerful tool in deriving new converter topologies, but also allows the transfer of knowledge obtained from a circuit to its dual circuit. In Sec. 4.5, the basic concepts of dual networks and the duality principle are briefly reviewed. The duality in the basic PWM converters is discussed in Sec. 4.6.

Interestingly, when the dual network and the duality principle are applied to a given ZCS or a ZVS, quasi-resonant converter, its dual converter is not found in the same family but in the other family of quasi-resonant converters. The duality between the families of ZCS and ZVS, quasi-resonant converters is the subject of Sec. 4.7.

Finally, a comparison of the ZCS and the ZVS, quasi-resonant converters, their potential and limitations are discussed in Sec. 4.8.

4.1. Basic Converter Topologies

4.1.1. Historical Background

It is often claimed that there are four basic converter topologies: buck, boost, buck/boost and Cuk. So far, this claim has never been proved or disproved. On the other hand, a plethora of converter topologies have been proposed in literature [F1-F25]. In most cases, a new topology is created using a cut-and-try approach. In other cases, some forms of systematic synthesis are used.

A paper [F9] by S. Cuk is one of the earliest papers to discuss the topological properties of switching converters. In particular, he identified the duality as one of the most fundamental and general topological relationships among converter circuits. Cuk also claimed that there are four basic converter topologies and two different types of energy transfer mechanisms: inductive and capacitive. However, he did not provide theoretical support on the validity of these claims.

In their book [F24], R. Severns and G. Bloom compiled a myriad of converter topologies and classified them into three major categories: buck-derived topologies, boost-derived topologies, and combinations of converters. This classification scheme covers a large number of topologies and provides a clear overview of those converter topologies included. However, many topologies are not included, and many topologies included do not fit well into the classification scheme.

The purpose of the following section is not to propose another novel approach in synthesizing new converter topologies, nor is it to provide a new classification scheme. The intention of this section is to probe into the basic topological properties in converter circuits. In particular, the physical constraints imposing on the topological variations are derived from circuit theories. Ultimately, through these newly derived constraints, it is proved that there exist exactly six different basic converter topologies.

4.1.2. Basic Topological Structures

The only class of converters discussed here are the most often used and most fundamental, the so-called **one-active-switch, two-topology, ladder-structured** converters. In other words, each basic converter belonging to this class possesses the following properties:

1. It contains only one active switch (i.e., one power transistor) and one passive switch (i.e., one rectifier diode).

2. It has exactly two topological states, which are determined by the on-off state of the active switch. This property also implies a continuous mode of operation, where every energy storage/transfer inductor carries a nonzero dc current and every storage/transfer capacitor carries a nonzero dc voltage.

3. It contains no coupled inductors.

4. It has a planar, ladder-like structure, i.e., it consists of series branches and parallel branches denoted as S_1, S_2, P_1, P_2, and so forth. Each series branch is followed by a parallel branch, and each parallel branch is followed by a series branch. Figure 4.1. shows a typical planar, ladder-like circuit structure.

5. It contains only one power source and only one load.

6. Power flows from left to right.

Furthermore, a converter topology containing additional inductors or capacitors whose sole purpose is to provide filtering for the input or the output is not considered a basic topology.

As will be proved later, there are only six different basic converter topologies, as shown in Fig. 4.2. They are: buck, boost, buck/boost, Cuk, SEPIC, and the dual of SEPIC (which will be called the **Zeta converter** in subsequent discussions. -- Zeta is the sixth Greek alphabet). Each converter topology can be divided into two or three sections: input, middle, and output, as shown in Fig. 4.3. The buck and the boost converters have no middle sections.

Input Section

The input section consists of a voltage source or a current source and a series or parallel switch. As will be shown in the following subsection, the input section can contain no more than one source. Generally, a current source is implemented and simulated by a voltage source in series with a large input inductor.

For the voltage source, a dc current is flowing out of the positive end. For the current source, a dc voltage is maintained across its two ends.

Middle Section

The middle section consists of one or more inductor and/or capacitor elements for intermediate energy storage/transfer. Each inductor carries a nonzero dc current, and each capacitor carries a nonzero dc voltage. Dynamically, these inductors and capacitors absorb and store energy from the input section at one moment and transfer energy to the output section at another. Consequently, we can treat an energy storage/transfer inductor as a **current buffer** and an energy storage/transfer capacitor as a **voltage buffer.**

Unlike the voltage or current sources, these voltage or current buffers do not generate power, nor do they consume power. As a result of being power neutral, no dc current is flowing through a voltage buffer, and no dc voltage is applied across a current buffer. However, a voltage buffer also should never be short-circuited, and a current buffer should never be open-circuited.

Output Section

Basically, there are two types of load circuits in converters. One contains an output capacitor directly following the output rectifier. The other contains an output inductor connected between the output rectifier and the output capacitor. In the first case, the middle section or the input section sees a constant dc output voltage; therefore, we view this type of load as a **voltage load.** In the second case, the output section draws a constant dc current from the middle section or the input section; therefore, it is viewed as a **current load.**

The output section of a basic converter consists of a voltage load or a current load and a series diode or parallel diode.

A voltage load draws a dc current from the input section or the middle section into its positive end. A current load induces a dc voltage across its two ends.

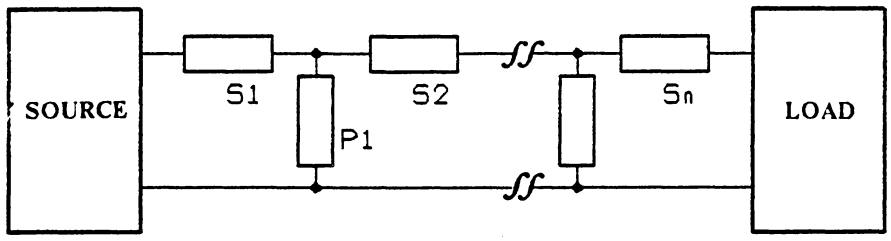


Fig. 4.1. A planar, ladder-structured converter network

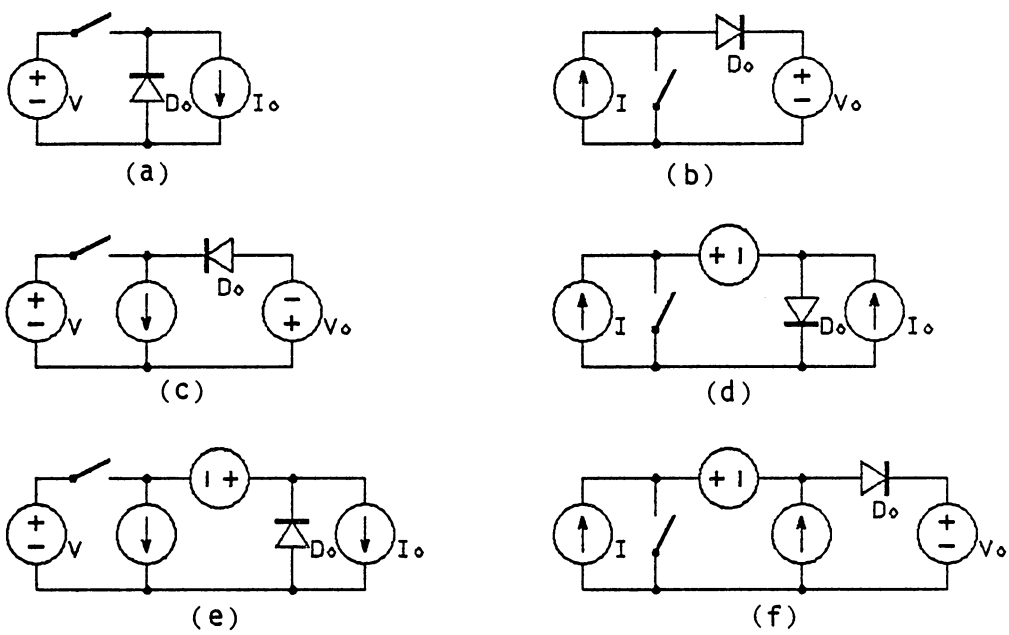


Fig. 4.2. The six basic converter topologies:
(a) buck (b) boost (c) buck/boost (d) Cuk
(e) Zeta (f) SEPIC

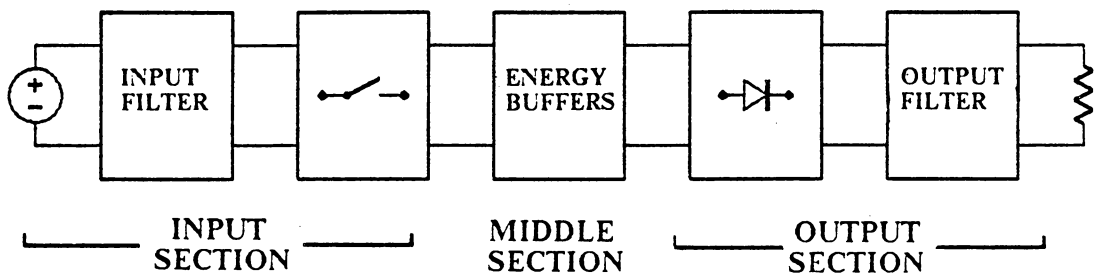


Fig. 4.3. The three sections of a basic PWM converter

4.1.3. Basic Topological Constraints

CONSTRAINT 1. Only two configurations of the input section are valid:

1. a voltage source in series with a switch (Fig. 4.4a)

2. a current source in parallel with a switch (Fig. 4.4b)

First of all, a switch cannot be connected in parallel with a voltage source, as shown in Fig. 4.4c. Otherwise, turning on the switch will result in a short circuit. Similarly, it is not viable to connect a switch in series with a current source, as shown in Fig. 4.4d, since a current source should never be open-circuited.

Furthermore, it is either a trivial case or a conflicting case when there are two or more sources connected to the left of the switch. Consider the following cases:

1. A voltage source and a current source are connected in series (Fig. 4.5a)

   -- They degenerate into a single current source.

2. A voltage source and a current source are connected in parallel (Fig. 4.5b)

   -- They degenerate into a single voltage source.

3. Two voltage sources are connected in parallel (Fig. 4.5c)

-- It is not valid if their voltage levels are different.

4. Two current sources are connected in series (Fig. 4.5d)

   -- It is not valid if their current magnitudes are different.

5. Two voltage sources are connected in series (Fig. 4.5e)

   -- They degenerate into a single voltage source whose voltage is the sum of those of the two original sources.

6. Two current sources in parallel (Fig. 4.5f)

   -- They degenerate into a single current source whose current is the sum of those of the two original sources

In addition, it can be shown that any planar, ladder-structured combination of more than two sources can be reduced to either a trivial case or a conflicting case. Thus, we have proved that only two configurations of the input section are valid (Figs. 4.4a and 4.4b).

CONSTRAINT 2. Only two configurations of the output section are valid:

1. a diode in series with a voltage load (Fig. 4.6a)

2. a diode in parallel with a current load (Fig. 4.6b)

Similarly, it can be proved that it is either a trivial case or a conflicting case when connecting two or more load circuits to the right of the diode.

Also, the diode should be connected either in series with a voltage load or in parallel with a current load.

However, depending on the particular converter topology, the load circuit may have a same polarity or an opposite polarity as that of the voltage source or current source of the input section (Figs. 4.6c and 4.6d).

CONSTRAINT 3. Each branch in the middle section contains only one voltage buffer or one current buffer.

This constraint can be proved by following the same argument as that in Constraint 1.

CONSTRAINT 4. Each series branch of the middle section is a voltage buffer; each parallel branch of the middle section is a current buffer.

It has been proved in Constraint 3 that each branch of the middle section contains only one buffer. It only needs to be proved that a series branch cannot be a current buffer, and a parallel branch cannot be a voltage buffer.

Consider first the connection of the leftmost buffer. From Constraint 1, it is shown there are only two configurations of the input section. The following cases are invalid:

1. A parallel voltage buffer is connected to a voltage source with a series switch (Fig. 4.7a)

-- If the magnitude of the voltage source, V_s, is different from the magnitude of the voltage buffer, V_b, it causes a short circuit when the switch turns on. If V_s is equal to V_b, then the switch will never conduct current and will lose its purpose.

2. A parallel voltage buffer is connected to a current source with a parallel switch (Fig. 4.7b)

   -- It causes a short circuit when the switch turns on.

3. A series current buffer is connected to a voltage source with a series switch (Fig. 4.7c)

   -- It causes an open circuit to the current buffer when the switch turns off.

4. A series current buffer is connected to a current source with a parallel switch (Fig. 4.7d)

   -- If I_s and I_b are equal, then the switch will never conduct current. If I_s and I_b are not equal, then a conflicting case results when the switch is open.

5. A series voltage buffer is connected to a voltage source with a series switch (Fig. 4.7e)

   -- Since a voltage buffer carries no dc current, this configuration blocks the flow of input current.

6. A parallel current buffer is connected to a current source with a parallel switch (Fig. 4.7f)

   -- Since there is a non-zero dc voltage across the current source, it violates the constraint that no dc voltage should be applied to a current buffer.

Therefore, only two remaining configurations are valid: a parallel current buffer connected to a voltage source with a series switch (Fig. 4.7g), and a series voltage buffer connected to a current source with a parallel switch (Fig. 4.7h).

Similarly, it can be easily shown that it is invalid to add a series current buffer to the circuits in Fig. 4.7g or Fig. 4.7h, nor is it valid to add a parallel voltage buffer to these two circuits.

By inductive proof, we can verify Constraint 4 is true for the cases when the middle section contains more than one buffer.

CONSTRAINT 5. A voltage source cannot be switched into a voltage buffer or a voltage load.

The voltage source provides a dc current to the load. When a voltage source is connected to a voltage buffer through a series switch, as shown in Fig. 4.7e, a net dc current flows into the voltage buffer which violates the power-neutral property of the voltage buffer.

When a voltage source is directly supporting a voltage load, as shown in Figs. 4.8a and 4.8b, it is either a trivial case or a conflicting case.

CONSTRAINT 6. A current source cannot be switched into a current buffer or a current load.

This constraint can be proved by an argument similar to that in Constraint 5 (see Figs. 4.7f, 4.8c, and 4.8d).

CONSTRAINT 7. A voltage buffer cannot be followed by a voltage load with a series diode; a current buffer cannot be followed by a current load with a parallel diode.

This constraint can be proved by an argument similar to that in Constraints 5 and 6 (see Figs. 4.9a and 9b).

CONSTRAINT 8. The structure of each converter follows one of the following sequences:

1. voltage -- current -- voltage -- current ...

2. current -- voltage -- current -- voltage ...

In other words, a voltage source is followed by a current load, or it is followed by a current buffer and then a voltage load, etc. A current source is followed by a voltage load, or it is followed by a voltage buffer and then a current load, etc.

This constraint is a direct result of Constraints 4, 5, 6, and 7.

CONSTRAINT 9. A middle section can contain no more than two buffers.

Suppose there are two voltage buffers and one current buffer in the middle section, as shown in Fig. 4.10a. Since the net dc currents flowing through buffer V_1 and buffer V_2 are both zero, the net dc current flowing into the current buffer will be zero. This condition leads to a degenerate case and the circuit can be replaced by a single voltage buffer whose voltage is the sum of V_1 and V_2.

Similarly, two current buffers and one voltage buffer, as shown in Fig. 4.10b, will degenerate into a single current buffer, since the dc voltages across points AN and BN are both zero.

From Constraint 1, there are only two valid configurations of the input section, one with a voltage source and the other with a current source. But from Constraint 8, it is shown that once the type of the input source is known, the type of each following buffer or load is determined. For the class of one-active-switch, two-topology, ladder-structured converters, the two converters without a middle section are the buck converter (voltage source, current load) and the boost converter (current source, voltage load). The two converters with a buffer in the middle section are the buck/boost converter (voltage source, current buffer, voltage load) and the Cuk converter (current source, voltage buffer, current load). The two converters with two buffers in the middle section are the Zeta converter (voltage source, current buffer, voltage buffer, current load) and the SEPIC converter (current source, voltage buffer, current buffer, voltage load). From Constraint 9, a middle section can contain no more than two buffers, therefore, there

are only six members in this class of converters: buck, boost, buck/boost, Cuk, Zeta, and SEPIC.

An interesting feature is that, from Constraint 4, the layout of the inductors and capacitors of the middle section resembles a high-pass LC filter. In fact, this feature can be seen from the converter topologies with a middle section, and is especially obvious in the SEPIC and the Zeta converters. In contrast, the layout of the inductors and capacitors for input and output filtering is in a low-pass filter form. Besides being a direct result of the circuit constraints we have just proved, there are two other reasons behind this unique feature. First, the purpose of the middle section is to act as an intermediate energy storage/transfer circuit. It should not hinder the normal flow of the high-frequency, ac power pulses from the input section to the output section. The second reason is that the input and the output sections generally have different dc voltage and/or dc current levels, the capacitors (voltage buffers) also serve as dc voltage decouplers, and the inductors (current buffers) serve as dc current decouplers.

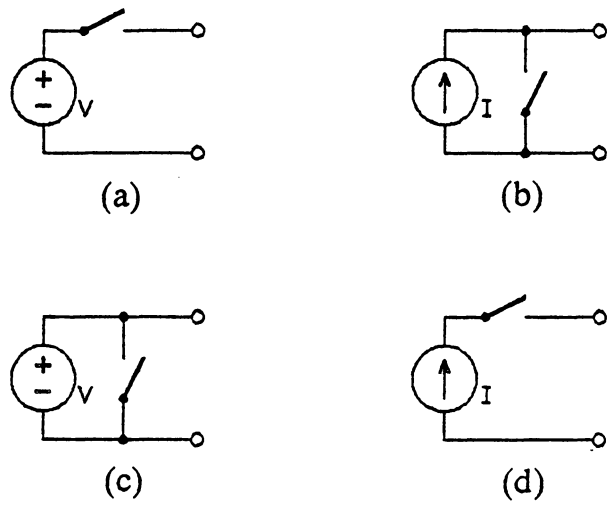


Fig. 4.4. Two valid configurations of the input section
(a) a voltage source in series with a switch
(b) a current source in parallel with a switch
Two invalid configurations of the input section
(c) a voltage source in parallel with a switch
(d) a current source in series with a switch

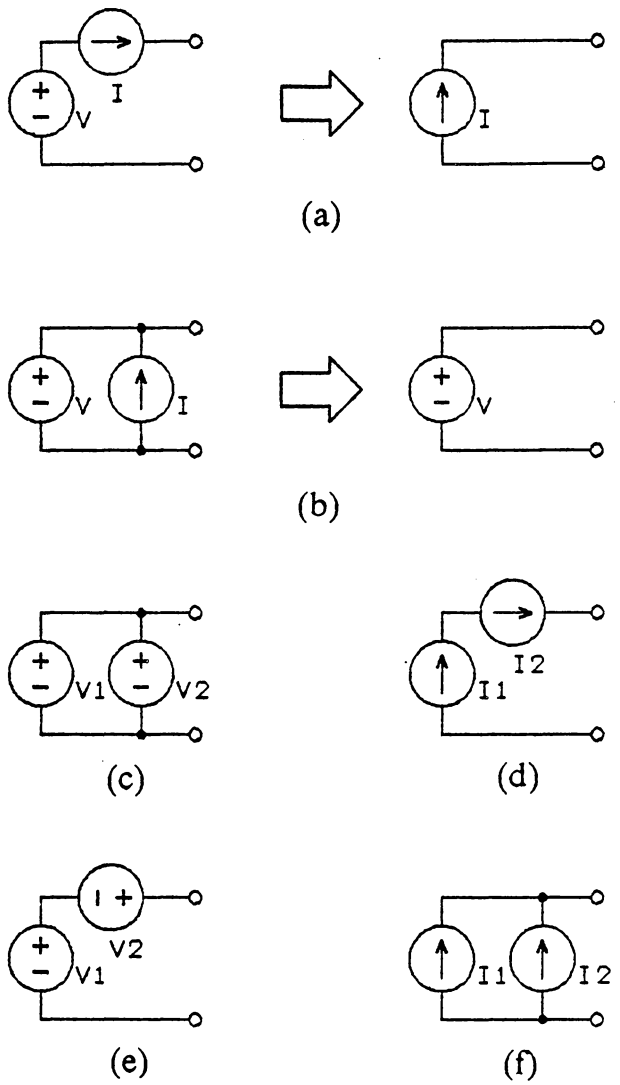


Fig. 4.5. Connecting two or more sources to the left of the switch in the input section
(a) a voltage source in series with a current source
(b) a voltage source in parallel with a current source
(c) two voltage sources in parallel (d) two current sources in series
(e) two voltage sources in series (f) two current sources in parallel

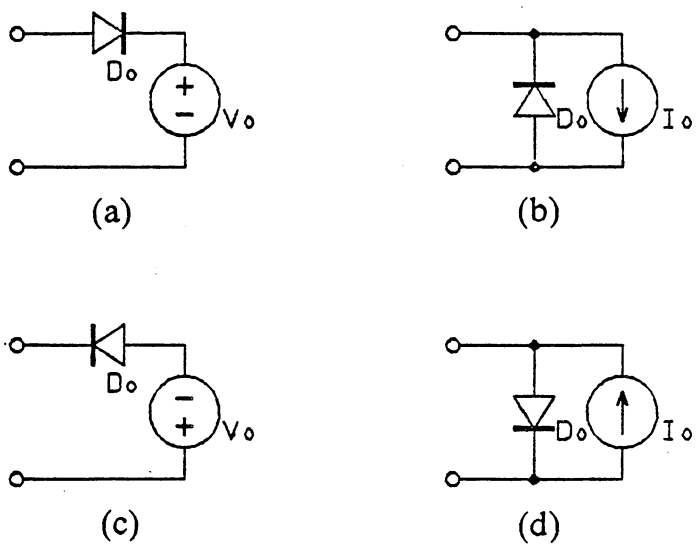


Fig. 4.6. Valid configurations of the output section
(a) a voltage load in series with a diode
(b) a current load in parallel with a diode
(c) a voltage load in series with a diode (reverse polarity)
(d) a current load in parallel with a diode (reverse polarity)

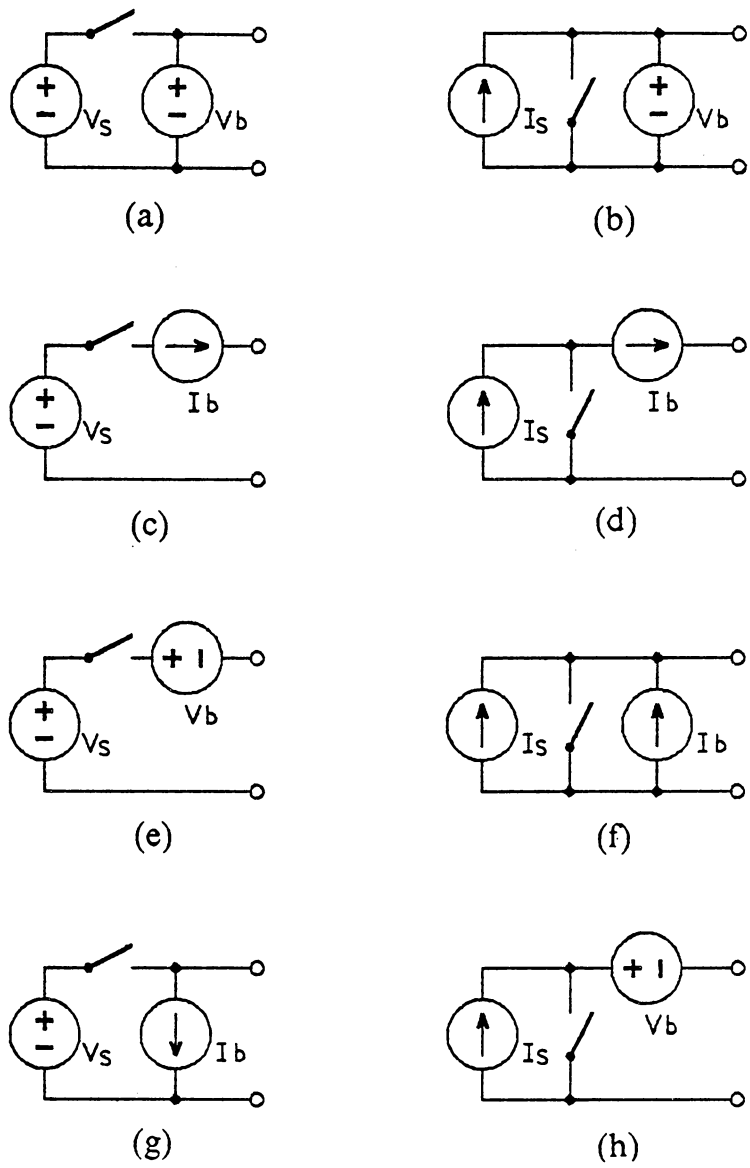


Fig. 4.7 (a)-(f) Invalid configurations of adding a voltage buffer or a current buffer to the input section (g),(h) Two valid configurations of adding a voltage buffer or a current buffer to the input section

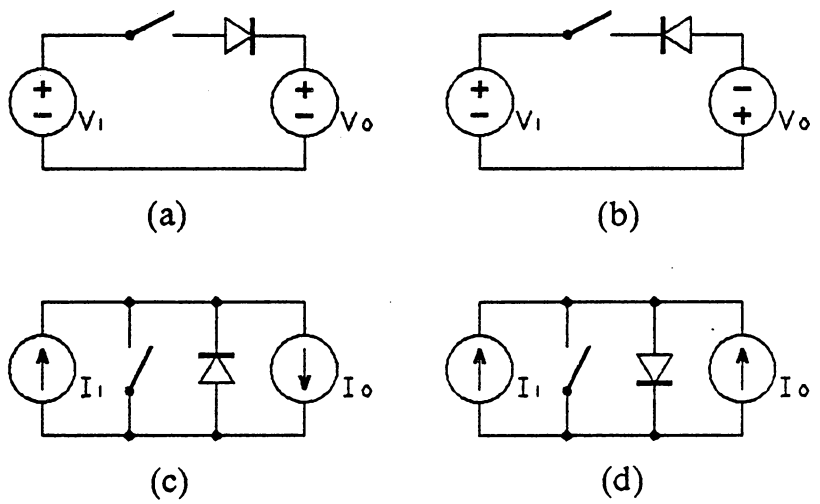


Fig. 4.8 Invalid configurations
(a),(b) a voltage source directly supporting a voltage load
(c),(d) a current source directly supporting a current load

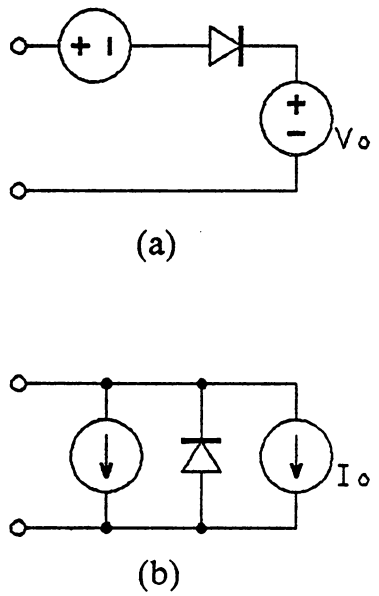


Fig. 4.9 Invalid configurations
(a) a voltage buffer followed by a voltage load
(b) a current buffer followed by a current load

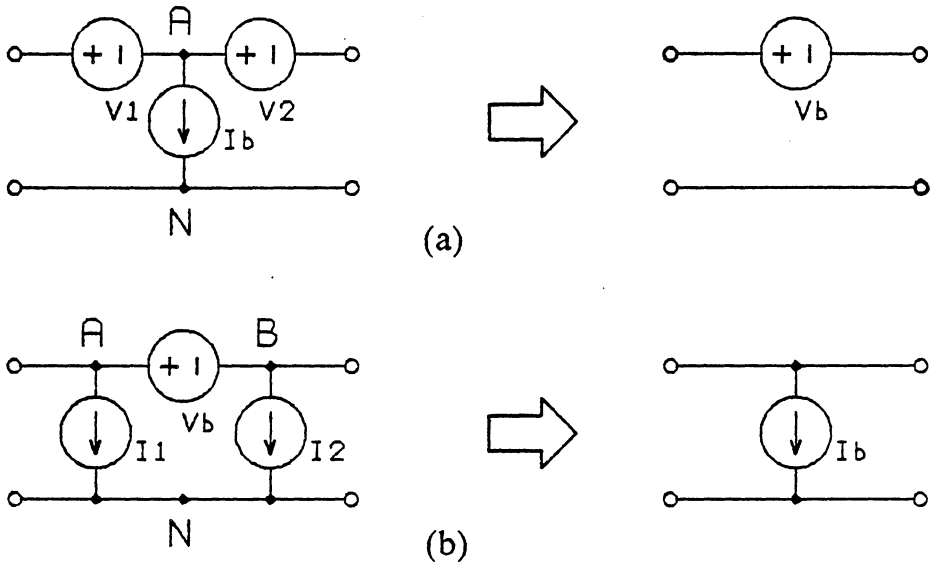


Fig. 4.10. Degenerated cases in the middle section
(a) a current buffer between two voltage buffers
(b) a voltage buffer between two current buffers

4.1.4. Inserting Transformers

In the class of one-active-switch, two-topology, ladder-structured converters, an isolation transformer should be inserted between the ground and a point where the dc voltage is zero. Otherwise, the transformer will be biased by a dc voltage, and a flux-resetting circuit is required. For instance, the buck converter has no neutral-voltage point to insert a transformer. Consequently, its isolated version, the forward converter, requires a reset winding and two additional diodes (Fig. 4.11a). Similarly, the boost converter also has no neutral-voltage point to insert a transformer.

On the other hand, for the converters with a middle section, there are two ways of inserting a transformer. One is to replace a current-buffer inductor with a transformer, such as converting a buck/boost converter into a flyback converter (see Fig. 4.11b). In this case, the transformer is actually a two-winding inductor, and a dc current flows in the primary and the secondary windings alternately. Another way is to split a voltage-buffer capacitor into two parts and insert a transformer in the middle, such as in obtaining an isolated version of the Cuk converter (see Fig. 4.11c). Apparently, the first method is simpler, since it requires less additional parts.

For the SEPIC converter and the Zeta converter, each has a voltage buffer and a current buffer, and each buffer is a proper place to insert a transformer. For example, the two ways of inserting a transformer into the SEPIC converter are shown in Fig. 4.12.

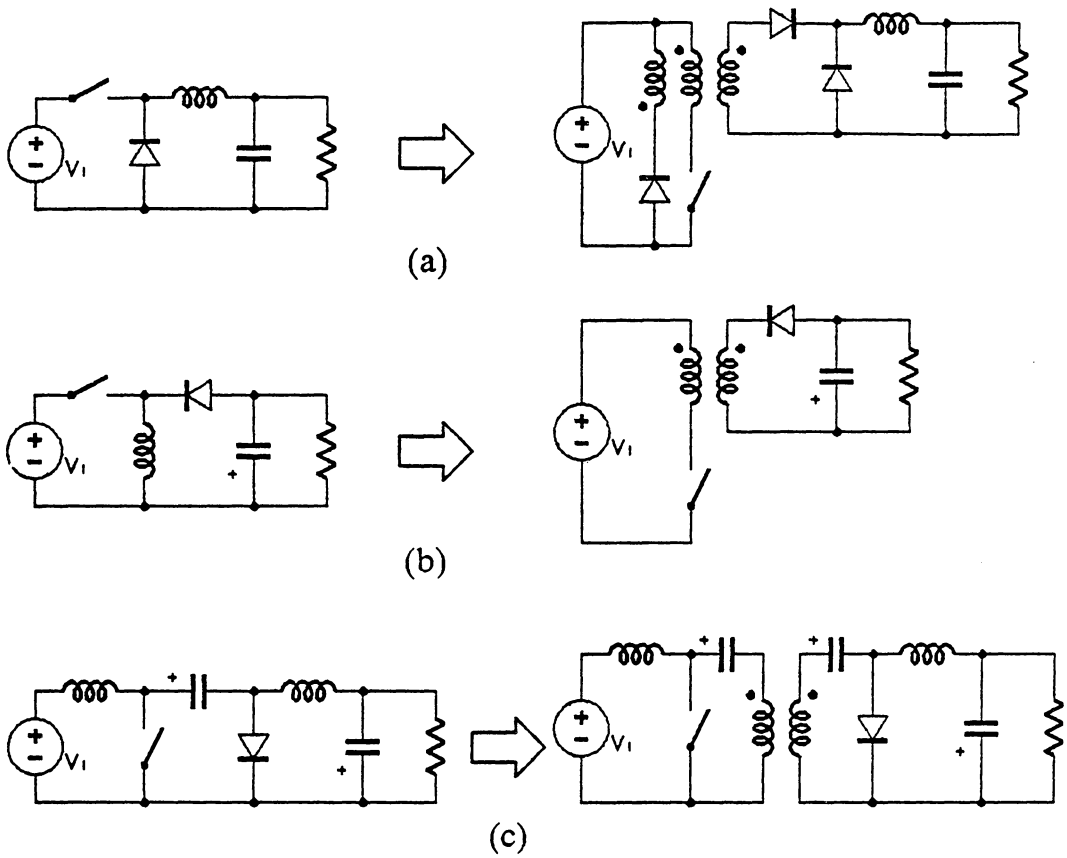


Fig. 4.11. Topological transformation by inserting a transformer
(a) buck converter to forward converter
(b) buck/boost converter to flyback converter
(c) Cuk converter to Cuk converter with isolation-transformer

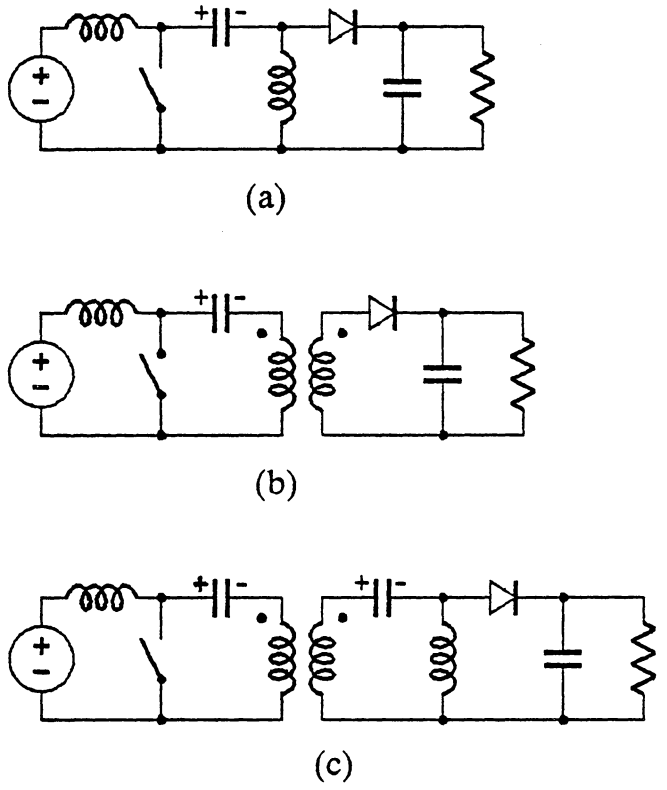


Fig. 4.12. Inserting a transformer to the SEPIC converter
(a) the non-isolated SEPIC converter
(b) replacing the current-buffer inductor with a transformer
(c) splitting the voltage-buffer capacitor and inserting a transformer

4.2. Variations of Converter Topologies

4.2.1. Bilateral Inversion

In any given converter topology, by making all switches bidirectional, i.e., adding an anti-parallel diode to a transistor and vice versa, the converter can be made to process the power bilaterally.

For example, Fig. 4.13a shows a boost converter. By adding diode D_2 to switch S_1, and switch S_2 to diode D_1, the circuit now becomes a bilateral converter which can transfer power either from left to right or from right to left, as shown in Fig. 4.13b. When the switch-diode set of S_1-D_1 is activated, the circuit degenerates into the boost converter of Fig. 4.13a, power flow is from left to right. When the switch-diode set of S_2-D_2 is activated, then the circuit degenerates into a buck converter, and power is transferred from right to left, as shown in Fig. 4.13c.

The bilateral inversion can be viewed as a special case of the duality [F7, F24]. From the standpoint of bilateral inversion, a buck converter can be seen as an inverted boost converter, and vice versa. Similarly, the inverted circuit of a SEPIC converter by applying the bilateral inversion is found to be a Zeta converter, and vice versa.

It is interesting to know that the bilateral inversion can also be applied to quasi-resonant converter topologies [B15, B16]. Figure 4.14a shows a ZCS,

quasi-resonant boost converter with an L-type resonant switch which consists of S_1, L_r, and C_r. By adding diode D_2 to switch S_1, and switch S_2 to diode D_1, the circuit becomes a bilateral converter which can transfer power in both directions, as shown in Fig. 4.14b. However, when only the switch-diode set of S_2-D_2 is activated, the circuit degenerates into a ZVS, quasi-resonant buck converter, where L_r and C_r remain as the resonant elements, as shown in Fig. 4.14c.

However, the bilateral inversion is not equivalent to the duality. Although both the dual network and the inverted network of the buck converter are the boost converter, the inverted buck/boost converter is another buck/boost converter (see Fig. 4.15a), whereas the dual version of the buck/boost converter is the Cuk converter, as will be shown in Sec. 4.6.

The inverted version of a ZCS, quasi-resonant buck/boost converter is a ZVS, quasi-resonant buck/boost converter, as shown in Fig. 4.15b.

The bilateral inversion technique is a general, topological property in converter circuits. Given a converter circuit, its inverted circuit can be constructed by following the standard procedure of switch-diode inversion. A detailed discussion on the bilateral inversion and extension of this technique can be found in Ref. [F24].

The **generalized resonant switches** which combine the concepts of zero-current switching and zero-voltage switching and bi-directional power flow in a single structure have been proposed by V. Vorperian. A more detailed discussion on this subject can be found in Refs. [B15, B16].

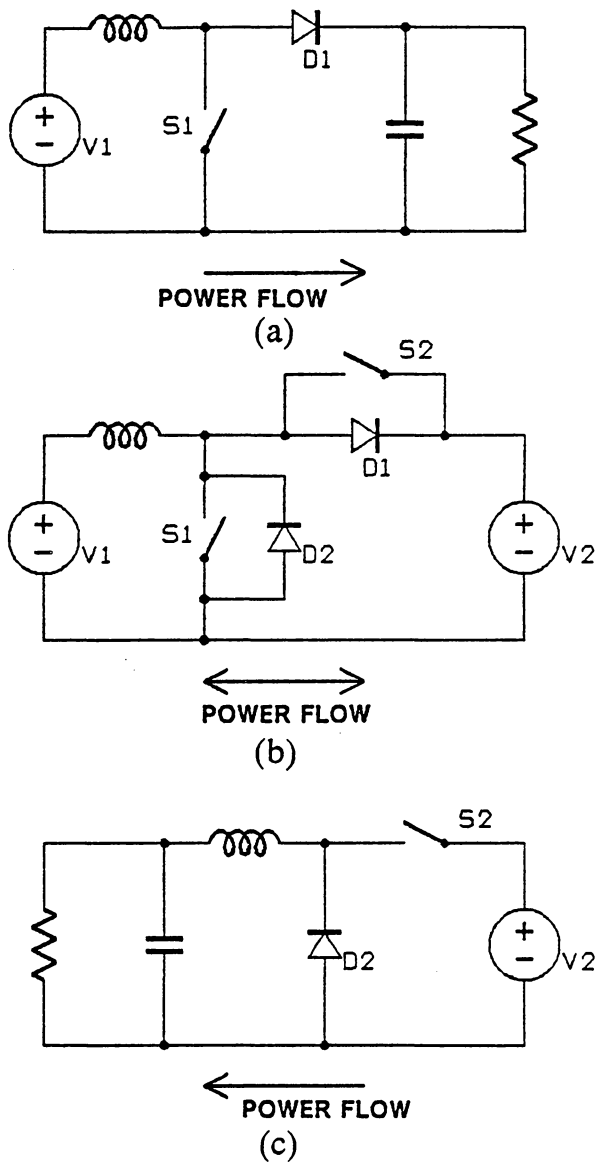


Fig. 4.13. Bilateral inversion of a boost converter
(a) boost converter
(b) bi-directional converter
(c) buck converter

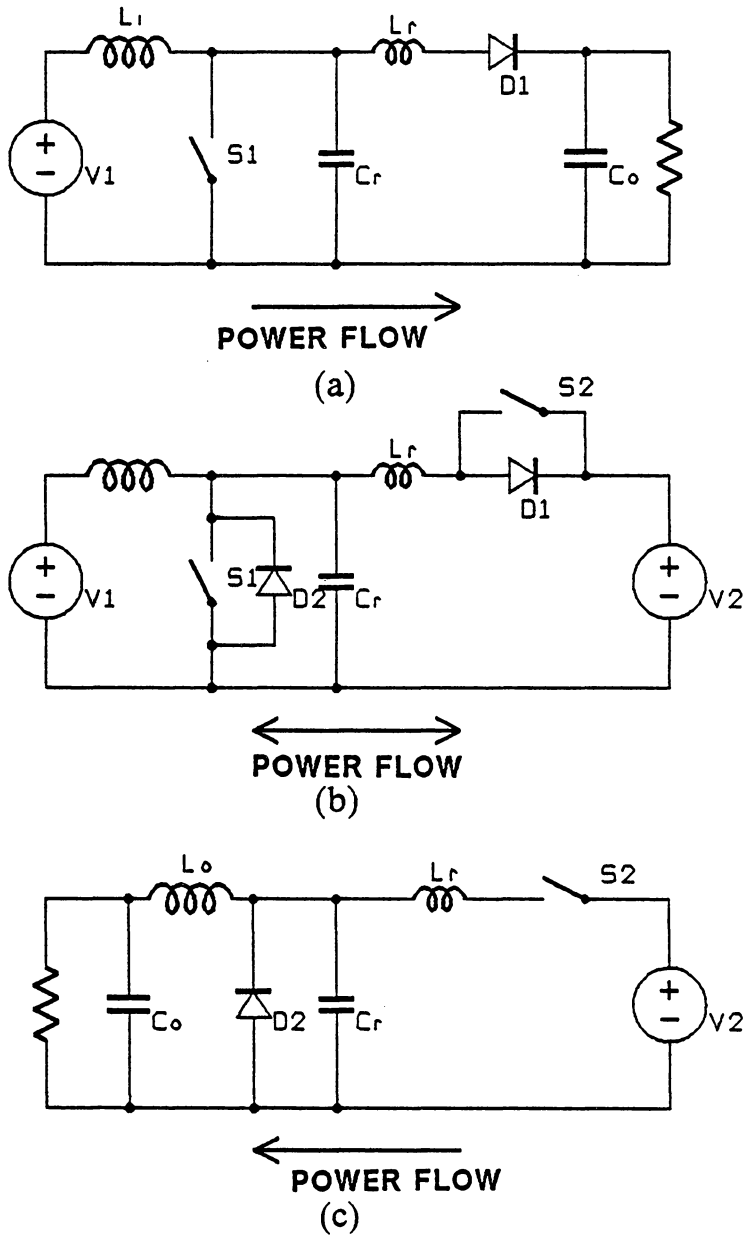
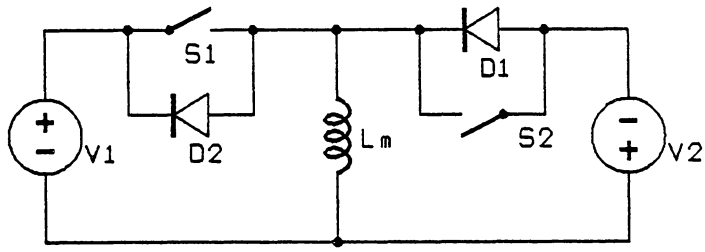


Fig. 4.14. Bilateral inversion of a ZCS, quasi-resonant boost converter

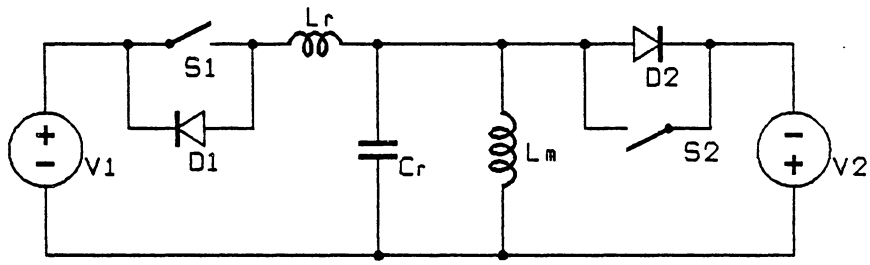
(a) ZCS, quasi-resonant boost converter

(b) bi-directional quasi-resonant converter

(c) ZVS, quasi-resonant buck converter



(a)



(b)

Fig. 4.15. (a) Bilateral inversion of the buck/boost converter
(b) Bilateral inversion of the quasi-resonant buck/boost converter

4.2.2. Adding a Power Transformer

As shown in Sec. 4.1.4, the most convenient way to insert a transformer into a single-ended converter is to split a current-buffer inductor or a voltage-buffer capacitor and place a transformer in between. But for the buck converter or the boost converter, a transformer has to be inserted at a point where there is a dc voltage bias, since these two converters have no current or voltage buffers. As a result, an additional flux-resetting circuit is required.

Different flux-resetting circuits result in many variations of converter circuits. For example, the most popular isolated version of the buck converter is the forward converter, which uses a tertiary winding to reset the magnetizing current, as shown in Fig. 4.16a. A modified version of the circuit is, instead of returning the magnetizing current to the voltage source, V_i, the tertiary winding is connected to the secondary-side circuit, and the magnetizing current is dumped to the output capacitor during the off-time, as shown in Fig. 4.16b [F16, F24].

Two ZCS, quasi-resonant versions of the forward converter are shown in Fig. 2.9d. However, no ZVS, quasi-resonant version of the forward converter has been discovered yet (see Sec. 4.4.).

Another general approach to obtain an isolated converter circuit is by inserting a dc-dc transformer which is a circuit similar to the middle portion of a push-pull converter, as shown in Fig. 4.17. However, this technique introduces additional circuit complexity, and its virtue may be justified only in several special cases. Many circuit variations derived through the application of this method are pre-

sented in Ref. [F24], where they constitute the major portion of two classes of converter circuits: the buck-derived and the boost-derived converters.

A quasi-resonant version of a dc-dc transformer is the circuit shown in Fig. 5.6b. A more detailed discussion is included in Chapter 5.

An important circuit generated from this approach is the current-fed, push-pull converter, as shown in Fig. 4.18. It is a boost converter with a dc-dc transformer inserted after the primary switch, S_a. If the duty cycles of switches S_1 and S_2 are made greater than 50%, then switch S_a can be omitted. Since the input current is restricted by the input inductor, it allows the overlapping conduction of S_1 and S_2, and the problem of unbalanced excitation of the transformer core is eliminated. Some circuit variations of the current-fed converters and their operation can be found in Refs. [F3, F11, F13, F15, F18].

Quasi-resonant converter versions of the current-fed, push-pull converter can be generated by replacing switch S_a by a current-mode or a voltage-mode resonant switch, or by replacing the dc-dc transformer by its quasi-resonant version.

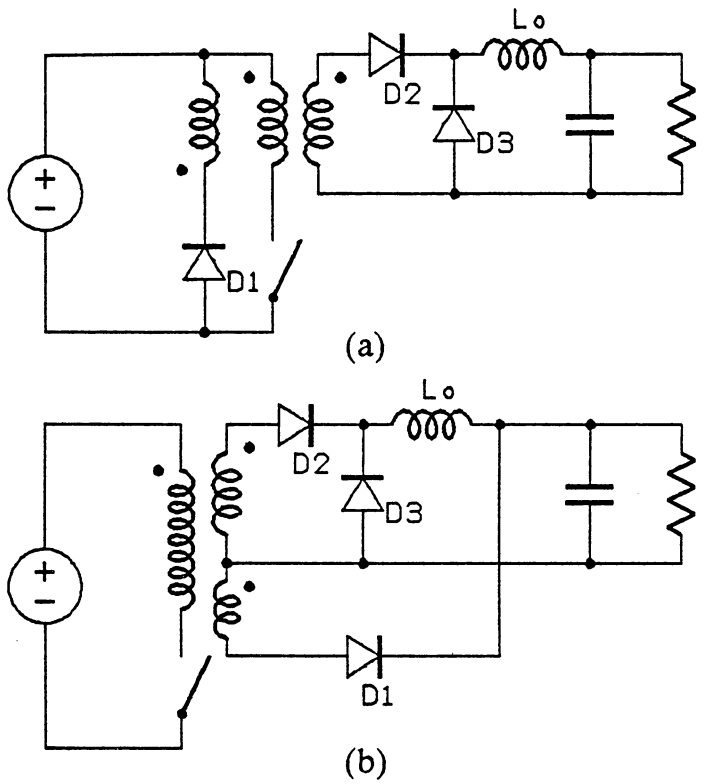


Fig. 4.16 Flux-resetting circuits of a forward converter
(a) returning the magnetizing current to the input voltage
(b) returning the magnetizing current to the output voltage

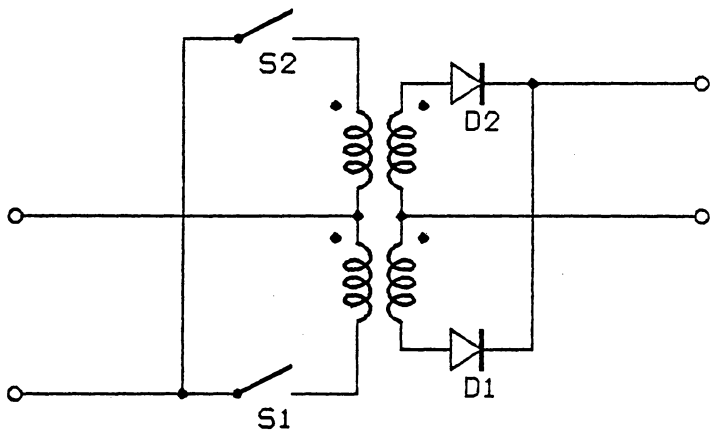


Fig. 4.17 A dc-dc transformer (S1 and S2 operating at 50% duty cycles)

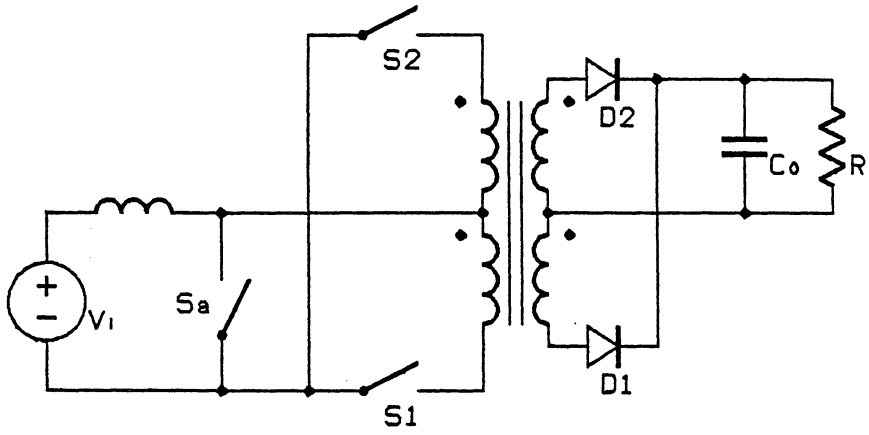


Fig. 4.18 A current-fed, push-pull converter

4.2.3. Magnetic Coupling and Tapping

Generally speaking, magnetic coupling and tapping are used to enhance some specific characteristics of a converter circuit. Typical improvements that can be achieved through magnetic coupling and tapping include: component stress reduction, steering of current ripple or voltage ripple, core-resetting, and small-signal transfer function improvement [F2, F7, F8, F12].

Inductor Tapping

A boost converter with a tapped input inductor [F2], as shown in Fig. 4.19a, is an example demonstrating the effect of inductor tapping. Suppose the turn ratio of the two sections of the inductor is n ($= \frac{N_2}{N_1}$), steady-state analysis shows that the voltage-conversion ratio of the converter with the tapped inductor is

$$\frac{V_o}{V_i} = M = \frac{1 + n D}{1 - D} \tag{4.1}$$

And the peak voltage stress on the switch, V_p, is

$$V_p = \frac{(V_o + nV_i)}{(n + 1)} \tag{4.2}$$

From Eqs. (4.1) and (4.2), it can be seen that V_o is always larger than V_i, therefore, V_p is smaller than V_o, which is the peak voltage stress on the switch in a boost converter with an untapped inductor. Although the peak voltage stress on

the switch is reduced by tapping the input inductor, the peak voltage stress on the output diode D_1 is increased [F2, F24].

A ZCS, quasi-resonant version of this converter, obtained by replacing the power switch by a current-mode resonant switch, is shown in Fig. 4.19b.

Coupled Inductors

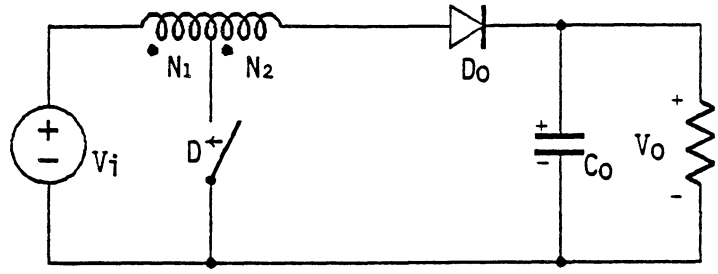
One of the common applications of the magnetic coupling is to introduce a reset mechanism to a transformer or an inductor. Typical examples include the tertiary winding in the forward converter, or the reset winding in the circuit of Fig. 4.16b.

Figure 4.20 shows a modified version of the current-fed, push-pull converter in Fig. 4.18. When switch S_a of the circuit in Fig. 4.18 is omitted, switches S_1 and S_2 can not be open simultaneously, otherwise, it will lead to an interrupt of the input inductor current. As a result, the duty cycle is limited to a range from 50% to 100%. By adding a reset winding to the input inductor, the inductor current can be carried by the secondary winding when both switches are open. Therefore, the duty cycle of this modified circuit can be varied from 0% to 100% [F13, F15, F18].

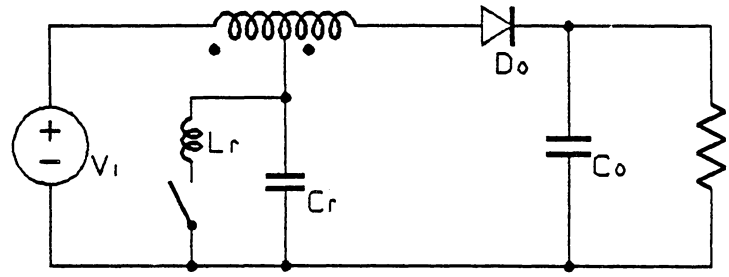
A quasi-resonant converter version of this circuit can be derived by replacing the dc-dc transformer by its quasi-resonant version, as shown in Fig. 5.6b.

Integrated Magnetics

Another important application of the magnetic coupling is the **integrated magnetics** technique proposed by S. Cuk [F7, F8, F12]. By properly introducing coupling among the inductors and transformers in a converter circuit, several advantages can be derived: core size and weight reduction, input/output ripple steering and reduction. This technique was originally applied to the Cuk converter. Subsequently, its application is extended to other converter circuits by G. Bloom and R. Severns [F22].



(a)



(b)

Fig. 4.19. (a) A boost converter with tapped inductor
(b) A ZCS, quasi-resonant boost converter with tapped inductor

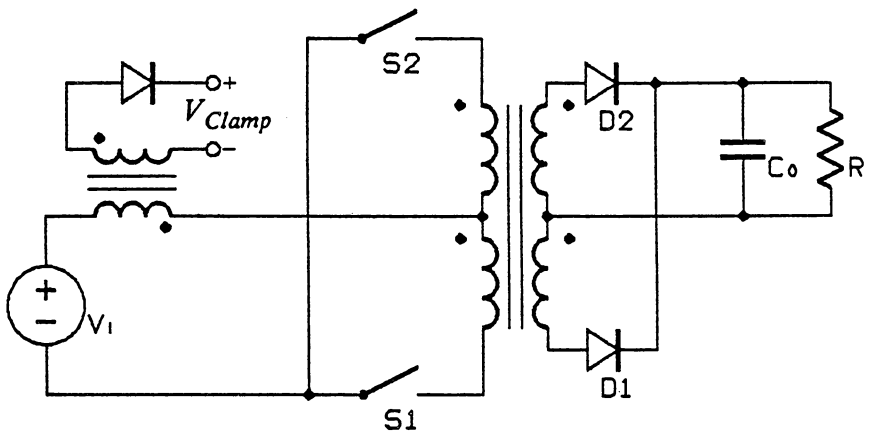


Fig. 4.20 A modified current-fed, push-pull converter with a 0% to 100% duty cycle range

4.2.4. Duality

The duality is one of the most important topological properties in converter circuits. The dual networks and the duality principle are applicable not only to PWM converters but also to quasi-resonant converters. Due to its special importance, the discussion on the duality is deferred until Secs. 4.5, 4.6, and 4.7.

4.2.5. Converter Cell Permutations

The concept of switching cells or converter cells is an approach taken by several authors in generating converter circuits [F10, F14, F19, F25]. A recent paper by R. Tymerski and V. Vorperian [F25] provides a large variety of converter cells and an extensive discussion on this subject.

A converter cell is defined as the network remaining when the input source and output load of a converter are removed. A converter cell is usually a combination of reactive elements (inductors and capacitors) and switches where the power flow is controlled. As shown in Fig. 4.21, a converter cell is treated as a three-terminal device which can be permuted and connected in six possible ways to the input source and output load, with a terminal of the converter cell connected to the common terminal to prevent the load from floating.

Figure 4.22 shows two of the many possible converter cells: (A) 2 switches and one inductor (B) 2 switches, 2 inductors and one capacitor. For converter cell A

(Fig. 4.22a), because of the symmetry of the cell, only three different configurations are generated (Figs. 4.22b-4.22d). These are the buck, the boost and the buck/boost converters. For converter cell B (Fig. 4.22e), there are also three different configurations generated (Figs. 4.22f-4.22h); each features non-pulsating input and output currents. Of these three, only one circuit is planar, ladder-structured; this is the well-known Cuk converter (Fig. 4.22h).

In Tymerski and Vorperian's paper, four classes of converter cells are considered:

1. First order, two switches (contains 1 family)

2. First order, four switches (contains 1 family)

3. Third order, two switches (contains 5 families)

4. Third order, four switches (contains 7 families)

In all, 66 different converter topologies are classified into 14 families according to their converter cell structures.

The converter cell approach provides a most resourceful way of generating converter topologies. Many new converter topologies have been discovered through this approach, some possessing very interesting characteristics. For example, several topologies (in addition to the Cuk converter) that feature non-pulsating input and output currents and several that achieve a large voltage

step-down ratio without requiring a very small duty ratio are presented in Ref. [F25].

An interesting topic for future investigation is the study of the topological constraints on the converter cells. In Sec. 4.1, the topological constraints on planar, ladder-structured converters have been fully derived. Similar constraints are believed to exist in planar converter circuits which are not ladder-structured. The revelations of these constraints may lead to a better understanding of converter structural properties and relationships among different converters.

Another topic for future study is the combination of the structures of resonant switches and converter cells. A recent study on this topic by V. Vorperian and R. Tymerski [B15, B16] has generated some interesting results. For example, a first order, two-switch, quasi-resonant converter cell is shown in Fig. 4.23a. By connecting this three-terminal network to the input, the output and the common in three possible ways, three ZCS, quasi-resonant converters are generated. If the bilateral inversion is applied to these circuits, three ZVS, quasi-resonant converters are generated.

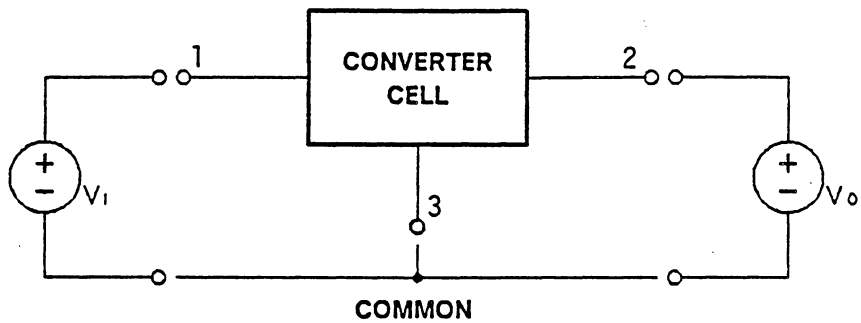


Fig. 4.21 The converter cell

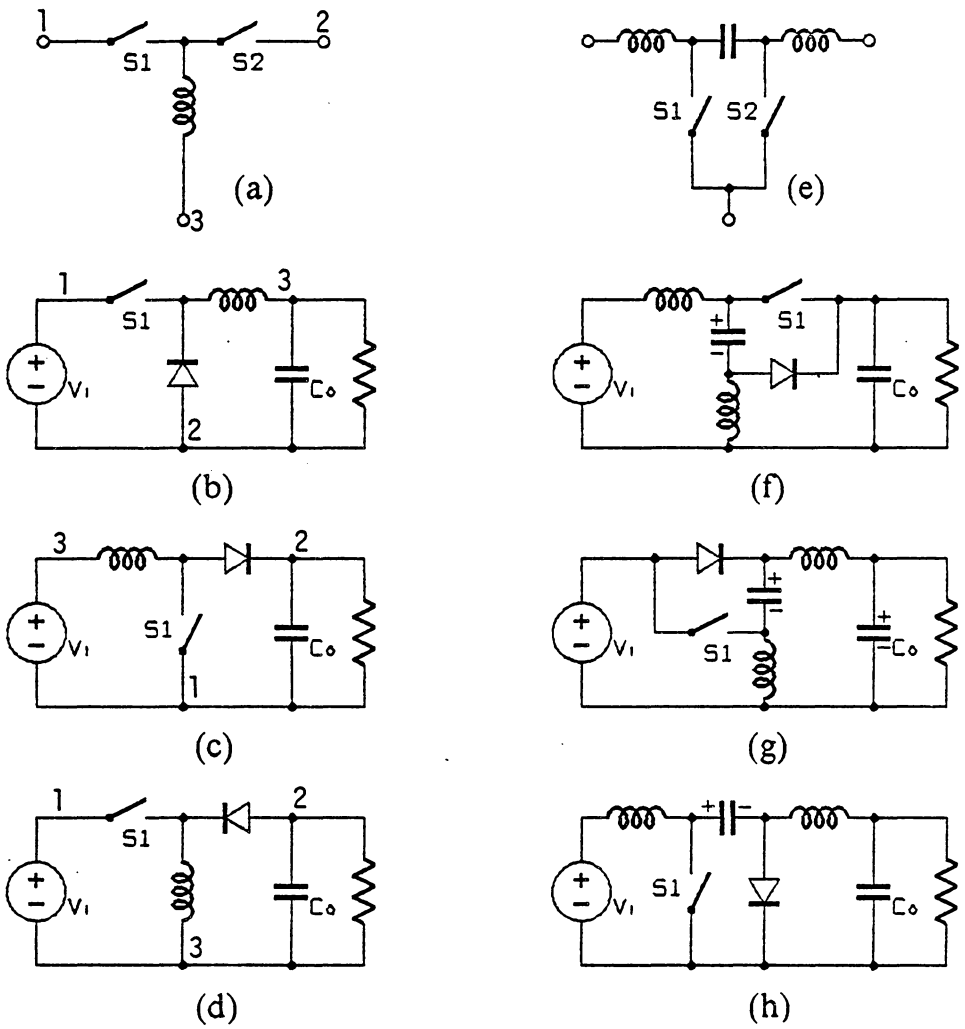


Fig. 4.22 (a) Converter cell A (2 switches, 1 inductor)
(b)-(d) Converters derived from converter cell A
(e) Converter cell B (2 switches, 2 inductors, 1 capacitor)
(f)-(h) Converters derived from converter cell B

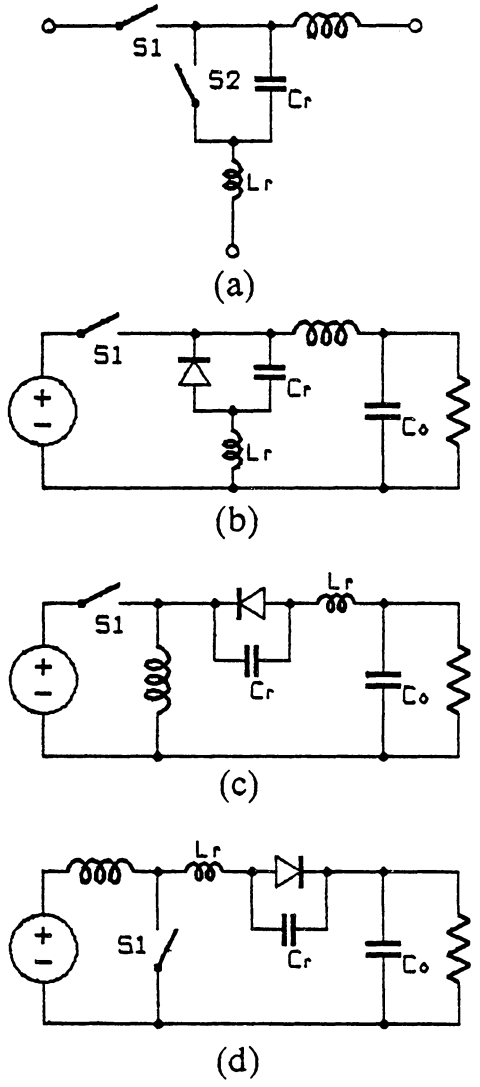


Fig. 4.23. (a) quasi-resonant converter cell (first order, two-switch)
(b) ZCS, quasi-resonant buck
(c) ZCS, quasi-resonant buck/boost
(d) ZCS, quasi-resonant boost

4.3. Topological Synthesis of Converters

Each single-input, single-output converter can be treated as a two-port network. Two such converters can be interconnected in a certain manner to create a new converter topology. In Fig. 4.24, the most common interconnections of two-port networks are shown: cascading, parallel connection, parallel input with series output, and series input with parallel output.

4.3.1. Cascading Similar Converters

In some applications, two similar converters are cascaded as a two-stage converter. Generally, one stage is driven at a constant duty cycle, providing a voltage-conversion ratio or dc isolation, and the other stage serves as a pre- or post-regulator. Figure 4.25a shows a two-stage cascaded buck converter. The concept can be extended to multi-stage cascaded converters, as shown in Fig. 4.25b [F4, F24].

A two-stage cascaded converter consisting of two ZCS, quasi-resonant buck converters are shown in Fig. 4.25c.

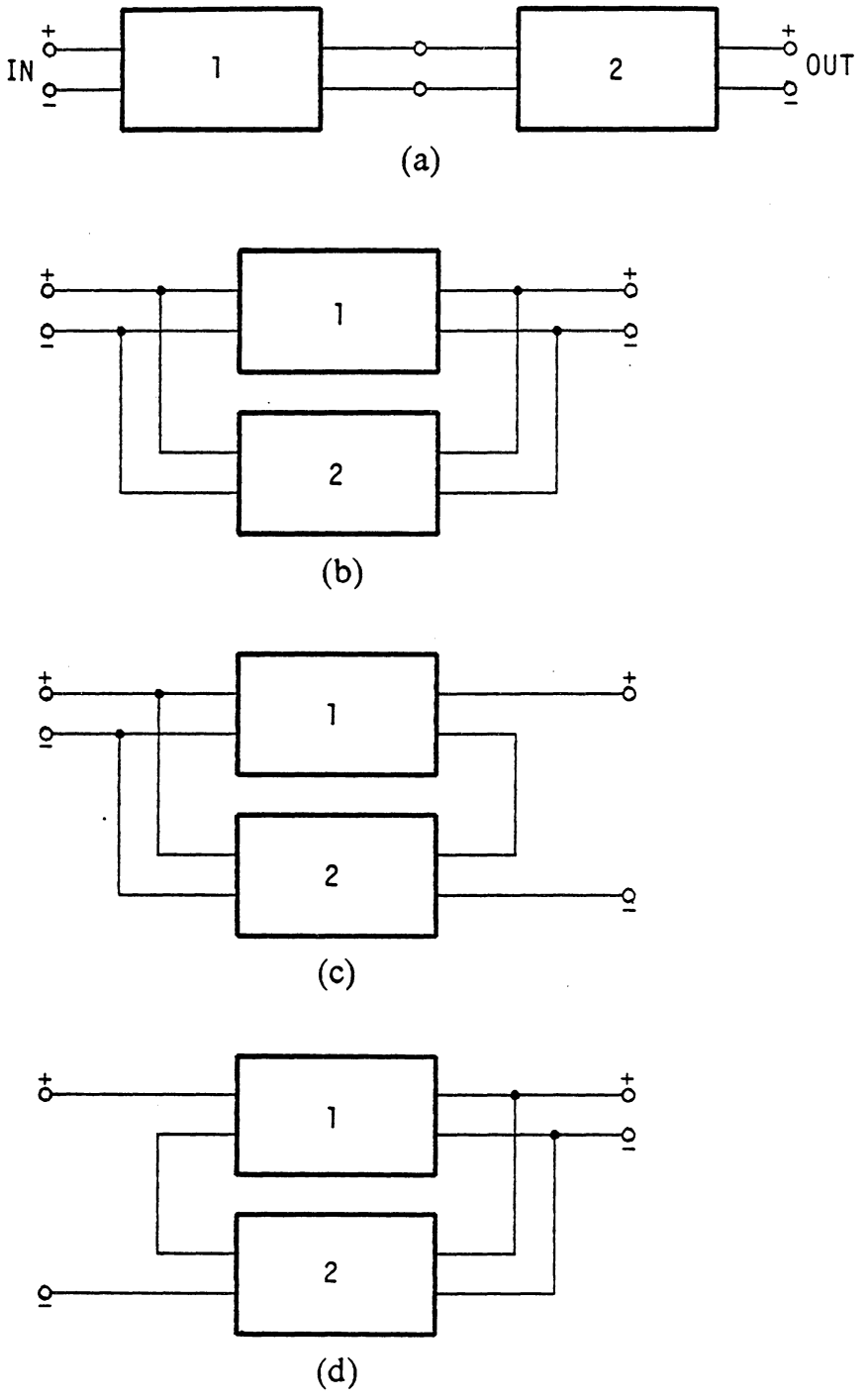


Fig. 4.24 (a) Cascade connection (b) Parallel connection (c) Parallel-input, series-output connection (d) Series-input, parallel-output connection

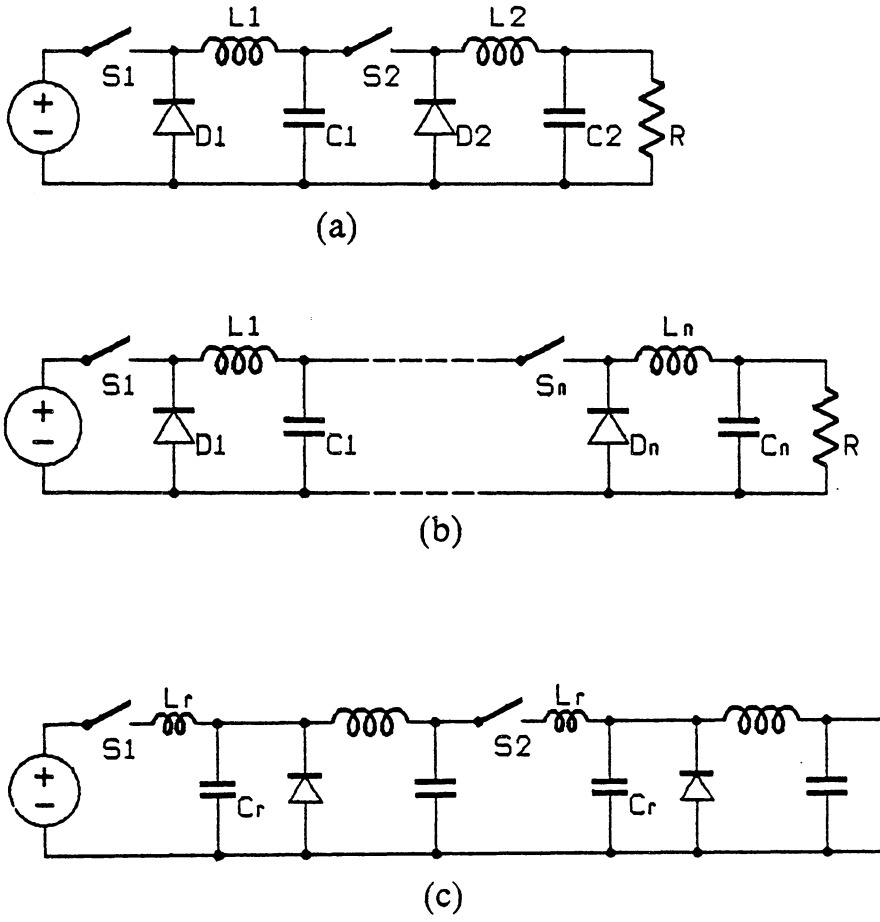


Fig. 4.25. (a) Two-stage, cascaded buck converter
(b) Multi-stage, cascaded buck converter
(c) Two-stage, cascaded ZCS, quasi-resonant buck converter

4.3.2. Cascading Dissimilar Converters

Two dissimilar converters can also be cascaded as a two-stage converter, with one stage serving as a voltage converter and the other stage as a pre-regulator or a post-regulator. More importantly, with some topological manipulation, cascading two converters can result in an entirely different converter circuit.

Figure 4.26a shows a buck converter and a boost converter. Suppose these two converter are cascaded with the output current of the buck converter directly feeding into the boost converter as its current source; the combined circuit is shown in Fig. 4.26b. Switches S_1 and S_2 in this circuit operate synchronously (they turn on and turn off at the same time), as do diodes D_1 and D_2.

The same circuit operation can be obtained by a simplified circuit, as shown in Fig. 4.26c. This circuit is derived from the circuit in Fig. 4.26b by: (a) inverting the output section, D_2 and V_o, (b) deleting switch S_2 and diode D_1, and (c) connecting the current buffer I_b as a shunt element.

The circuits in Fig.s 4.26b and 4.26c can be shown to be identical in their operation by comparing their behavior during the on-time and the off-time:

1. During the on-time, in either circuit, V_i charges current buffer I_b. The output diode is reverse biased, leaving V_o disconnected from the reset of the circuit.

2. During the off-time, in either circuit, V_i is disconnected from the circuit, and I_b discharges its energy to the output voltage, V_o.

The resulting circuit of cascading a buck converter with a boost converter, after simplification, turns out to be a buck/boost converter, i.e., another single-switch basic converter.

In his paper [F6], S. Cuk invented the **optimal dc-dc converter topology**, which is now known as the Cuk converter, by cascading a boost converter followed by a buck converter. The motivation was to develop a converter which combines the features of non-pulsating input current of the boost converter and the non-pulsating output current of the buck converter. Figure 4.27 shows the evolution of the Cuk converter. The output voltage of the boost converter is directly used as the input voltage of the buck converter, as shown in Fig. 4.27b.

Again, the two switches, S_1 and S_2, operate in a synchronous manner, so do diodes D_1 and D_2. Now, the circuit can be simplified by: (a) inverting the output section, D_2 and I_o, (b) deleting diode D_1 and switch S_2, and (c) connecting V_b as a series element. Figure 4.27c shows the final circuit.

Similarly, the circuits in Figure 4.27b and 4.27c are shown to be identical in their operation by comparing their behavior:

1. During the on-time, in either circuit, the diode(s) is(are) reverse biased. Voltage buffer V_b discharges its energy to the output current load, I_o. The input current source, I_i, is free-wheeling through switch S_1.

2. During the off-time, the diode(s) conducts. Voltage buffer V_b is charged by I_i. Output current I_o is free-wheeling through diode D_2.

The Cuk converter, first conceived through the cascading and simplification method described above, can also be derived from the buck/boost converter by applying the dual networks principle [F9], as will be described in detail in Sec. 4.6.

The cascading and simplification scheme can be extended further. By cascading a boost converter and a buck/boost converter, after simplification, the final circuit emerges to be a SEPIC converter. The evolution of this circuit is shown in Fig. 4.28. Similarly, the Zeta converter can be shown to be the simplified circuit of cascading a buck/boost converter and a buck converter.

The above observations lead to an argument that there exist only two basic converter topologies, i. e., the buck and the boost, and every other converter circuit is either derived from one of them or is a combination of two or more buck-derived or boost-derived converter circuits. This argument is reasonable, but not strong enough to exclude other viewpoints. First of all, although the buck/boost and the Cuk converter can be viewed as two topologies derived through the cascading of a buck converter and a boost converter, they possess many distinctive characteristics which can not be found in either the buck or the boost converter. For example, the buck/boost converter can be transformed into its isolated version simply by splitting its current-buffer inductor, while the isolated version of a buck or a boost converter requires an additional flux-resetting mechanism. Another example, the Cuk converter features a capacitive energy transfer mechanism which can not be found in either the buck or the boost converter.

Another counter to this argument is that the cascading and simplification scheme is not without pitfalls. Several questions are very difficult to answer by taking this approach, for example:

1. What will be the resulting circuit when cascading a Cuk converter and a boost converter? Or a buck converter and a Cuk converter?

2. Why is it impossible to cascade a buck converter and a buck/boost converter and simplify them to a new single-switch converter?

3. Is it always possible to generate a single-switch converter by simplifying any arbitrarily cascaded converters?

These questions, while very hard to answer from the cascading scheme and other established topological relationships among converter circuits, can be easily resolved by observing the constraints on converter topologies that have been described in Sec. 4.1.

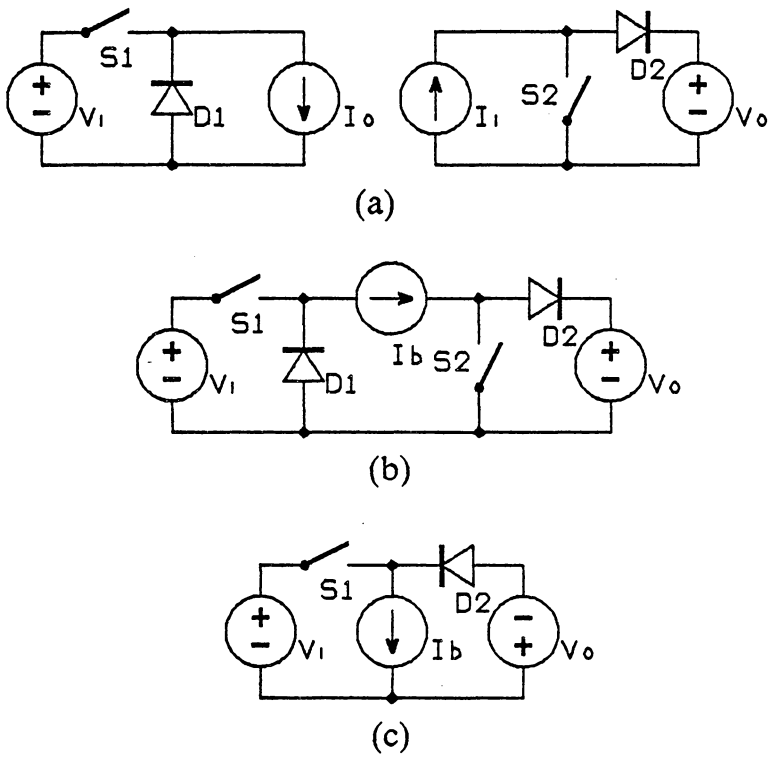


Fig. 4.26 Evolution of a buck/boost converter
(a) a buck converter and a boost converter
(b) cascaded circuit
(c) simplified circuit

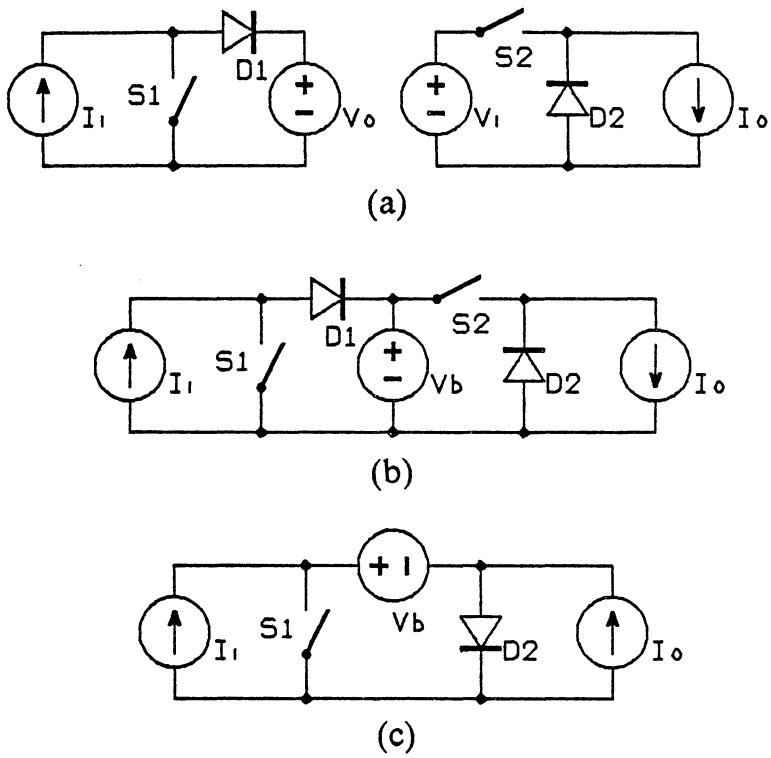


Fig. 4.27 . Evolution of a Cuk converter
(a) a boost converter and a buck converter
(b) cascaded circuit
(c) simplified circuit

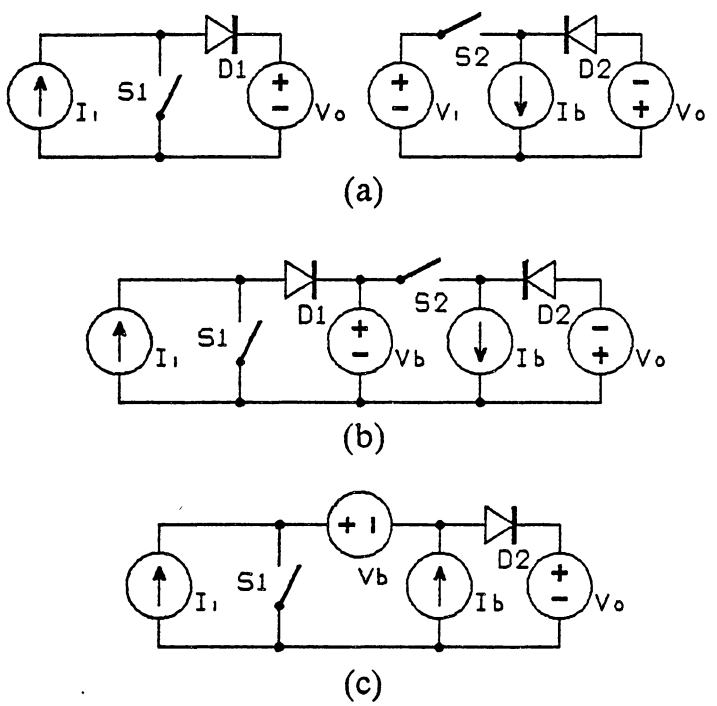


Fig. 4.28 Evolution of a SEPIC converter
(a) a boost converter and a buck/boost converter
(b) cascaded circuit
(c) simplified circuit

4.3.3. Parallel Connections

Another common interconnection of converter circuits is the parallel connection. Two of the major advantages in paralleling converters are to obtain higher power capacity and to reduce input and/or output ripple.

Figure 4.29a shows a parallel connection of three identical flyback converters. Each individual converter draws power from the same voltage source and delivers power to the same load. If the on-times of these three converters are separated evenly, the input and output ripple can be significantly reduced.

Similarly, three ZCS or ZVS, quasi-resonant flyback converters can be connected in parallel to achieve a reduction in the input and output ripple, as shown in Fig. 4.29b.

Another example of paralleling converters, although not obvious at first, is the push-pull, voltage-fed converter. Figure 4.30a shows two forward converters with their output connected in parallel and sharing a common current load. When a same voltage source is used to provide the input power for both converters, the primary-side circuits are connected in parallel as shown in Fig. 4.30b. Furthermore, diodes D_3 and D_4 in the secondary-side circuit can be removed, since the output current during the free-wheeling stage can be carried by the simultaneous conduction of diodes D_1 and D_2.

Quasi-resonant versions of push-pull or half-bridge converters are discussed in Chapter 5.

A major difficulty in paralleling converters is the current sharing among individual converters. Generally, there is no internal mechanism of distributing equal amounts of current (or power) load to individual converters. The most common approach in dealing with the current-sharing problem is through implementing a current sensing and a current-mode controlling scheme.

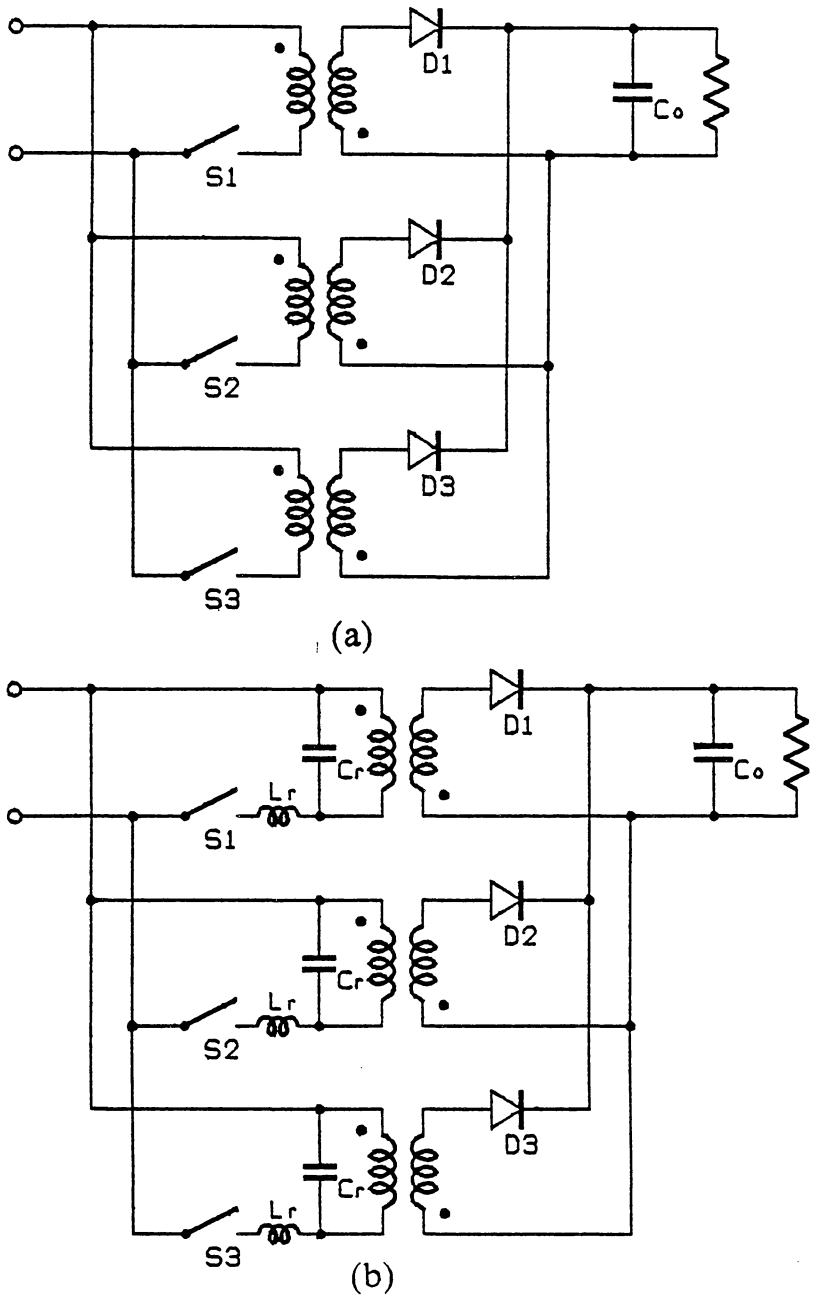
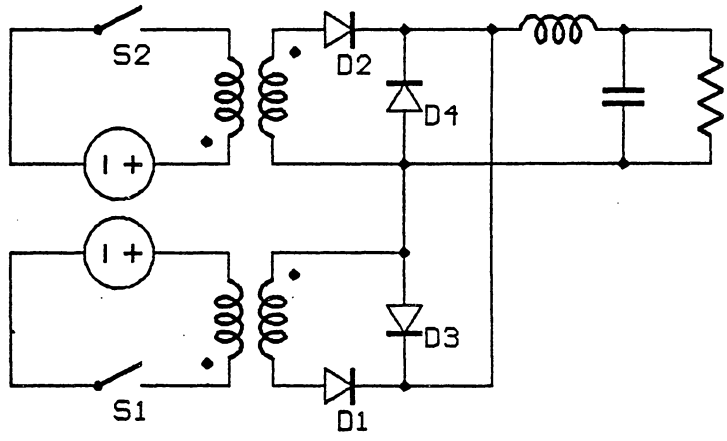
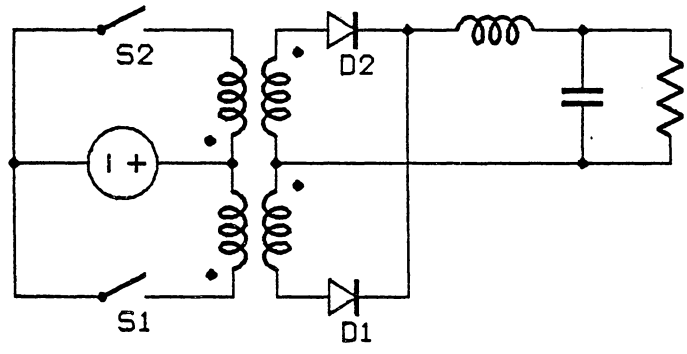


Fig. 4.29. (a) Parallel connection of three flyback converters
(b) Parallel connection of three ZCS, quasi-resonant flyback converters



(a)



(b)

Fig. 4.30 (a) Two forward converters with output circuits in parallel
(b) A voltage-fed, push-pull converter

4.3.4. Hybrid Connections

Many topological variations can be created by connecting the input or output circuits of two converter circuits in series or in parallel. Figure 4.31 shows a circuit where two push-pull converters are interconnected [F24]. The primary-side circuits of these two converters are connected in parallel, whereas the secondary-side circuits are connected in series. A special feature in this circuit is that the power load is divided evenly among the two individual converters, since their load circuits are connected in series, and a same load current is seen by the two converters.

A half-bridge, voltage-fed converter can be seen as a modified version of two forward converters with their primary-side circuits connected in series and their secondary-side circuits connected in parallel. Figure 4.32 illustrates this point of view.

Quasi-resonant versions of the half-bridge converters are discussed in Chapter 5.

Figure 4.33a shows a modified version of the half-bridge converter. When properly started, the voltage across capacitor C_1 will be charged to $\frac{V_i}{2}$. The transformer is excited in opposite directions by the alternate turning-on of switches S_1 and S_2. This circuit can also be viewed as a hybrid combination of two forward converters. A ZCS, quasi-resonant version of this circuit is shown in Fig. 4.33b.

Figure 4.34a shows a circuit which may be called a half-bridge flyback converter [F17]. In this circuit, two flyback converters are interconnected. Their primary-side circuits are stacked up in a manner similar to a half-bridge converter, and a same secondary-side circuit is shared by the two primary-side circuits. Quasi-resonant versions of this converter can be derived simply by replacing the two switches by two current-mode or two voltage-mode resonant switches. A ZCS, quasi-resonant version of this circuit is shown in Fig. 4.34b.

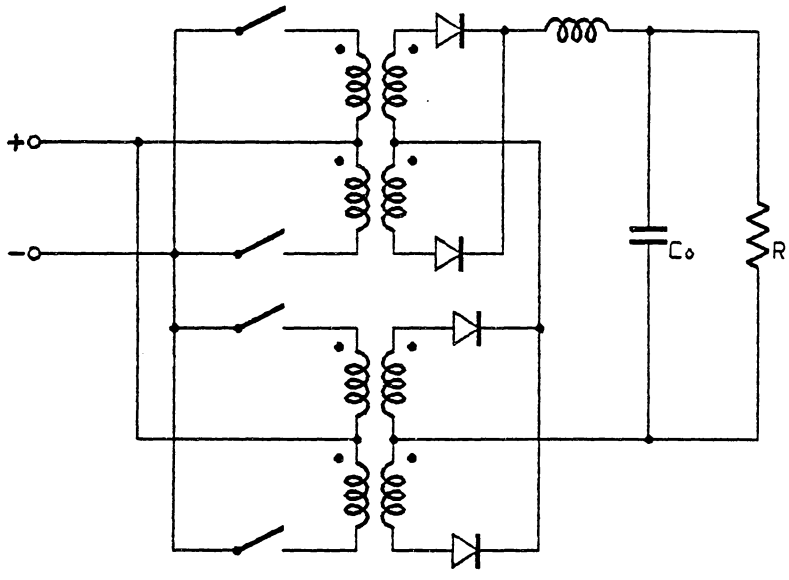


Fig. 4.31 Two push-pull converters with a parallel-input, series-output connection

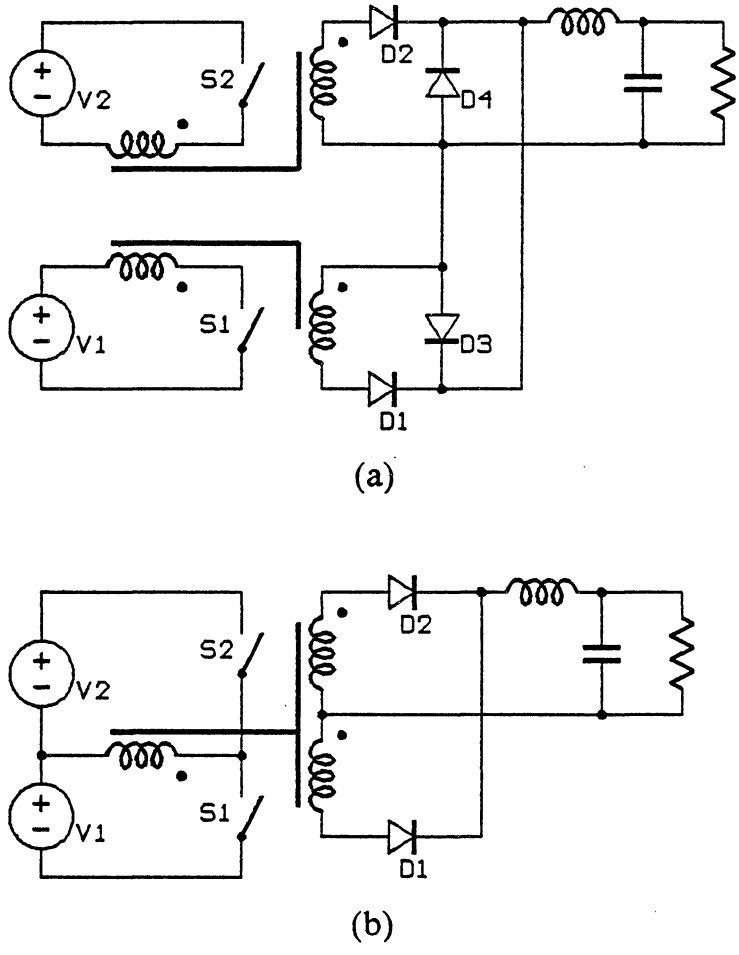


Fig. 4.32 (a) Two forward converters with output circuits in parallel (b) A half-bridge converter

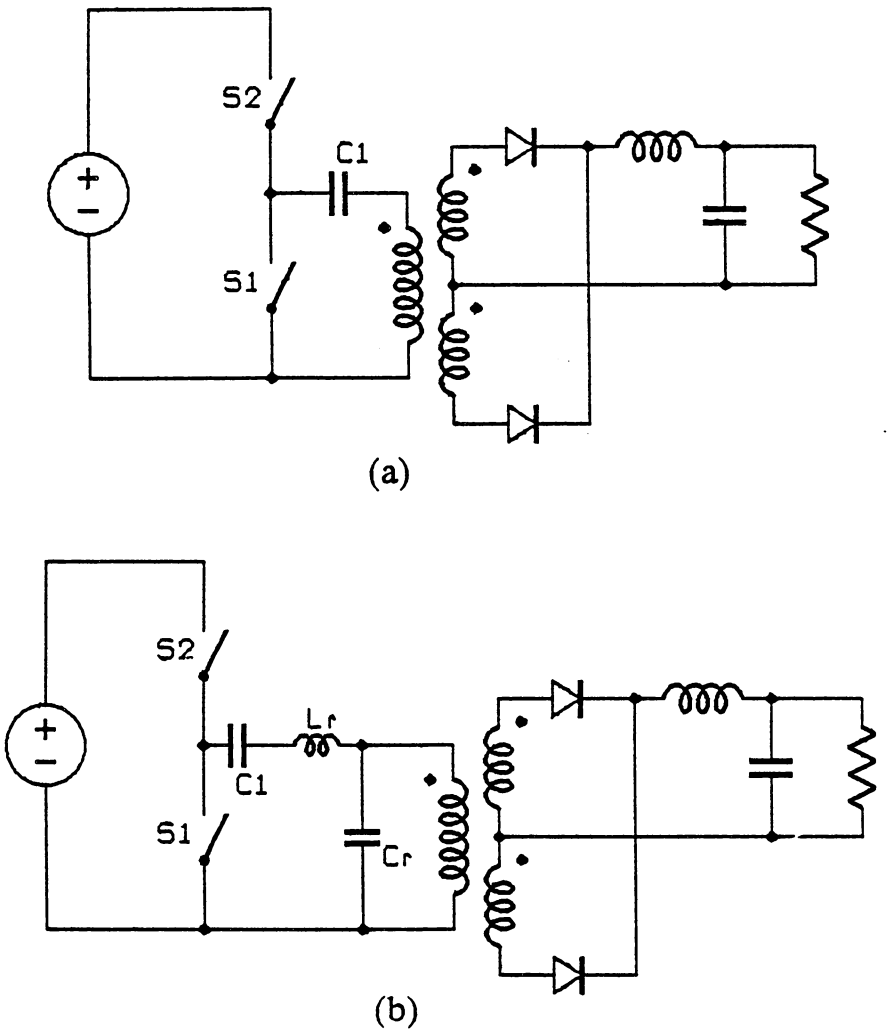


Fig. 4.33. (a) A modified half-bridge converter
(b) A modified ZCS, quasi-resonant, half-bridge converter

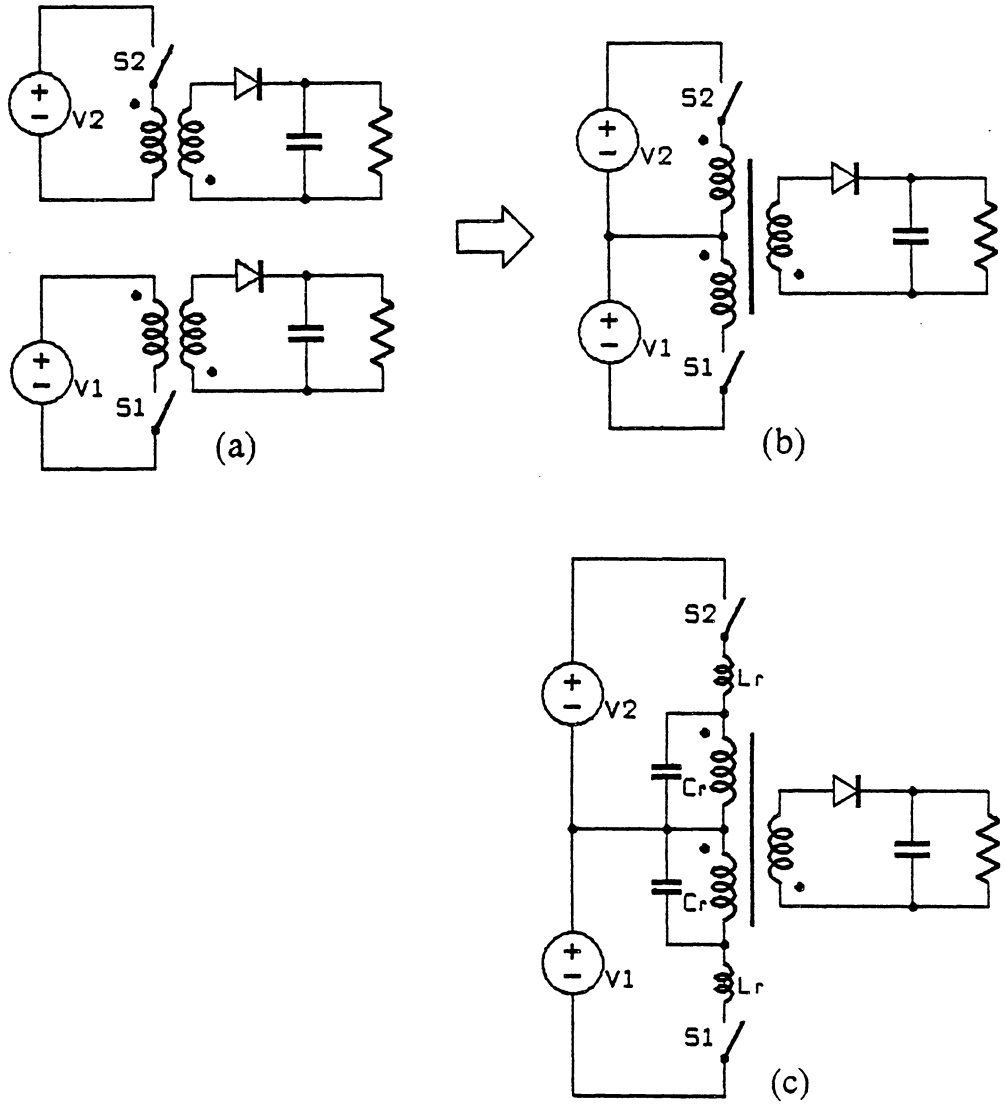


Fig. 4.34. (a) Two flyback converters
(b) A half-bridge flyback converter
(c) A ZCS, quasi-resonant, half-bridge flyback converter

4.4. *Topological Variations of Quasi-Resonant Converters*

The three previous sections have introduced the basic and derived PWM converter topologies. And from a given PWM converter circuit, simply by properly replacing the power switch by various types of resonant switches, quasi-resonant converters corresponding to that PWM topology can be derived. Although it is very powerful and applicable in most cases, this scheme of replacement of quasi-resonant switches is not universal. There are certain PWM converters which have no quasi-resonant converter counterparts, and the replacement scheme is not applicable. For example, because of the additional diode in series with the secondary winding of a forward converter (diode D_2 in Fig. 4.16a), the normal operation of a voltage-mode resonant switch is tempered. As a result, no ZVS, quasi-resonant forward converters have been discovered yet.

Another situation where the scheme of replacement of resonant switches is not very effective is in converter circuits with multiple power switches such as the bridge converters. The direct replacement of power switches by resonant switches may lead to additional circuit complexity, and even interference in the operations of the several resonant switches. In this case, a better approach is to modified the circuit such that a resonant tank circuit can be shared by two or more switches, thus, the circuit complexity can be minimized. For example, in the next chapter, it will be shown that when two ZCS, quasi-resonant forward converters are properly connected, redundant circuit elements can be removed, resulting in a much simplified circuit.

In Chapters 2 and 3, only two types of resonant switches have been considered (the M-type and the L-type) for the ZCS or the ZVS, quasi-resonant converters. In fact, from a given PWM converter, more than two ZCS and two ZVS, quasi-resonant converters can be derived. The number of the possible variations of quasi-resonant converters derived from a given PWM converter depends on its particular circuit structure. For example, it is found that there exist six ZCS and six ZVS, quasi-resonant buck converters [B12]. For the Cuk converter, it has 15 ZCS and 15 ZVS, quasi-resonant converter variations [B13].

The methods in deriving different quasi-resonant converter variations from a given PWM converter can be divided into two classes: capacitor shifting and inductor shifting [B12, B13].

The capacitor-shifting approach is based on the fact that a capacitor with an initial voltage can be treated as a capacitor with zero initial voltage in series with a dc voltage. To explain how the capacitor-shifting scheme can lead to several equivalent quasi-resonant converter variations, let's consider the ZCS, quasi-resonant buck converters.

Figure 4.35a shows a ZCS, quasi-resonant buck converter with an M-type, current-mode resonant switch, where capacitor C_r and inductor L_r are the resonant elements. The initial voltage value across capacitor C_r before switch S_1 turns on is V_i. Without affecting the circuit's behavior, capacitor C_r with initial voltage V_i can be replaced by a same capacitor without initial voltage and in series with a dc voltage of V_i.

Since the voltage on point A in Fig. 4.35b is always zero, the left end of capacitor C_r can be moved and connected to the ground, again without affecting the circuit's behavior. The resulting circuit, as shown in Fig. 4.35c, is exactly the same as the ZCS, quasi-resonant buck converter with an L-type resonant switch at the beginning of a switching cycle (see Sec. 2.3).

By following a similar procedure, the left end of capacitor C_r can be connected to another point in the circuit with a constant voltage, i.e., the positive end of the output voltage, as shown in Fig. 4.36c. From the above derivation, it can be seen that the capacitor-shifting scheme is not arbitrary. One end of the capacitor can be moved only to points where the voltages are constant (zero ac voltage). In the buck converter, there are only three points (the input voltage, the output voltage, and the ground) that satisfy the condition; therefore, there are only three different circuit variations which can be derived by using the capacitor-shifting scheme.

The inductor-shifting scheme is more involved and the derived circuit variations may have minor differences in their circuit behavior. Basically, the resonant inductor can be shifted around the **major loop** of the resonant-tank circuit. For a ZCS, quasi-resonant converter, the major loop consists of the active switch, the resonant inductor and the resonant capacitor. For a ZVS, quasi-resonant converter, the major loop consists of the passive switch, the resonant inductor and the resonant capacitor. Notice the major loops may contain dc voltage sources and/or voltage buffers.

To derive different ZCS (or ZVS), quasi-resonant converter variations from a given PWM converter, the following procedure can be taken:

1. Replace the active switch of the PWM converter by an M-type resonant switch to establish a basic quasi-resonant circuit.

2. Apply the capacitor-shifting scheme. Two or more variations derived from the basic circuit are generated.

3. Identify the major loop in the basic circuit.

4. Shift the resonant inductor to a different location in the major loop, another circuit variation is obtained. The new location of the resonant inductor must not cause uncontrolled oscillation of the resonant tank. That is, the resonant inductor and the resonant capacitor must not be in direct series.

5. Apply the capacitor-shifting scheme again, two or more variations of the circuit derived in step 4 can be generated.

6. Repeat steps 4 and 5 until the resonant inductor is shifted back to the original location.

The six ZCS, quasi-resonant buck converter variations shown in Fig. 4.36 can be generated by following the above procedure. The basic quasi-resonant circuit in Fig. 4.36a is first derived from the PWM buck converter by replacing the power switch by an M-type, current-mode resonant switch. Applying the capacitor-shifting scheme, two more circuit variations are generated, as shown in Figs. 4.36b and 4.36c. The major loop of the basic circuit in Fig. 4.36a consists

of the active switch, L_r, and C_r. Inductor L_r can be shifted around the major loop to the location as shown in Fig. 4.36d. This is another circuit variation, which has minor differences in circuit behavior from that of the circuit in Fig. 4.36a. From this circuit, two more circuit variations (see Figs. 4.36e and 4.36f) can be generated by applying the capacitor-shifting scheme.

Further shifting of inductor L_r will place it in direct series with C_r, and will result in uncontrolled oscillation after the switch is open. No valid circuit configurations can be generated with the inductor in this location. Shifting it a step further around the major loop, inductor L_r will come back to its original location as shown in Fig. 4.36a.

The six ZVS, quasi-resonant buck converters are derived by following the same procedure. Replacement of the power switch by an M-type, voltage-mode resonant switch creates the circuit of Fig. 4.37a. The application of the inductor-shifting scheme results in the circuit shown in Fig. 4.37d. Applying the capacitor-shifting scheme to the above circuits, four other variations are derived, as shown in Figs. 4.37b, 4.37c, 4.37e and 4.37f.

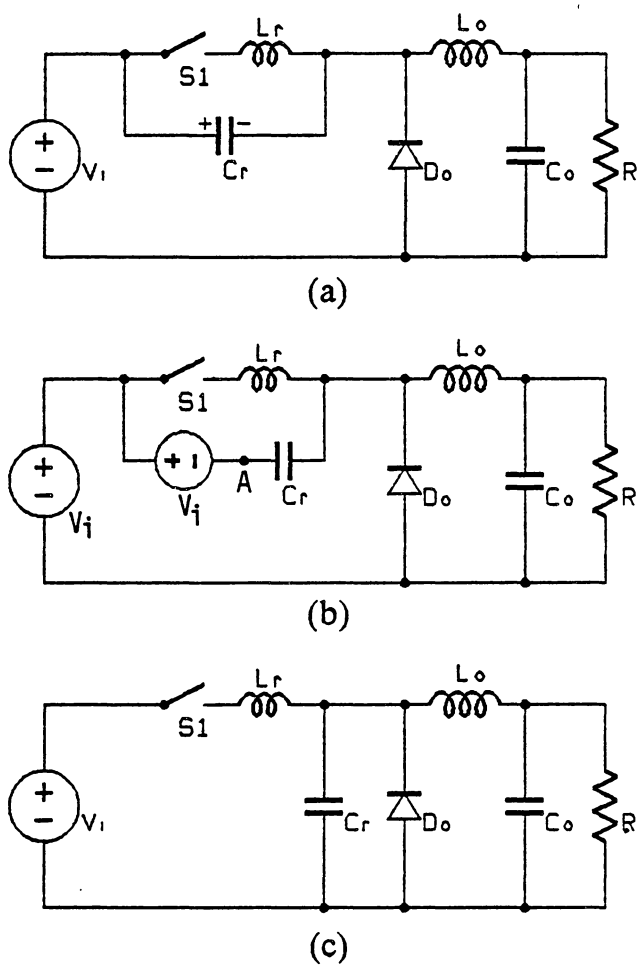


Fig. 4.35 Equivalence between two types of resonant switches
(a) a ZCS, quasi-resonant buck converter with an M-type resonant switch
(b) the capacitor with initial voltage replaced a dc voltage and a capacitor without initial voltage
(c) a ZCS, quasi-resonant buck converter with an L-type resonant switch

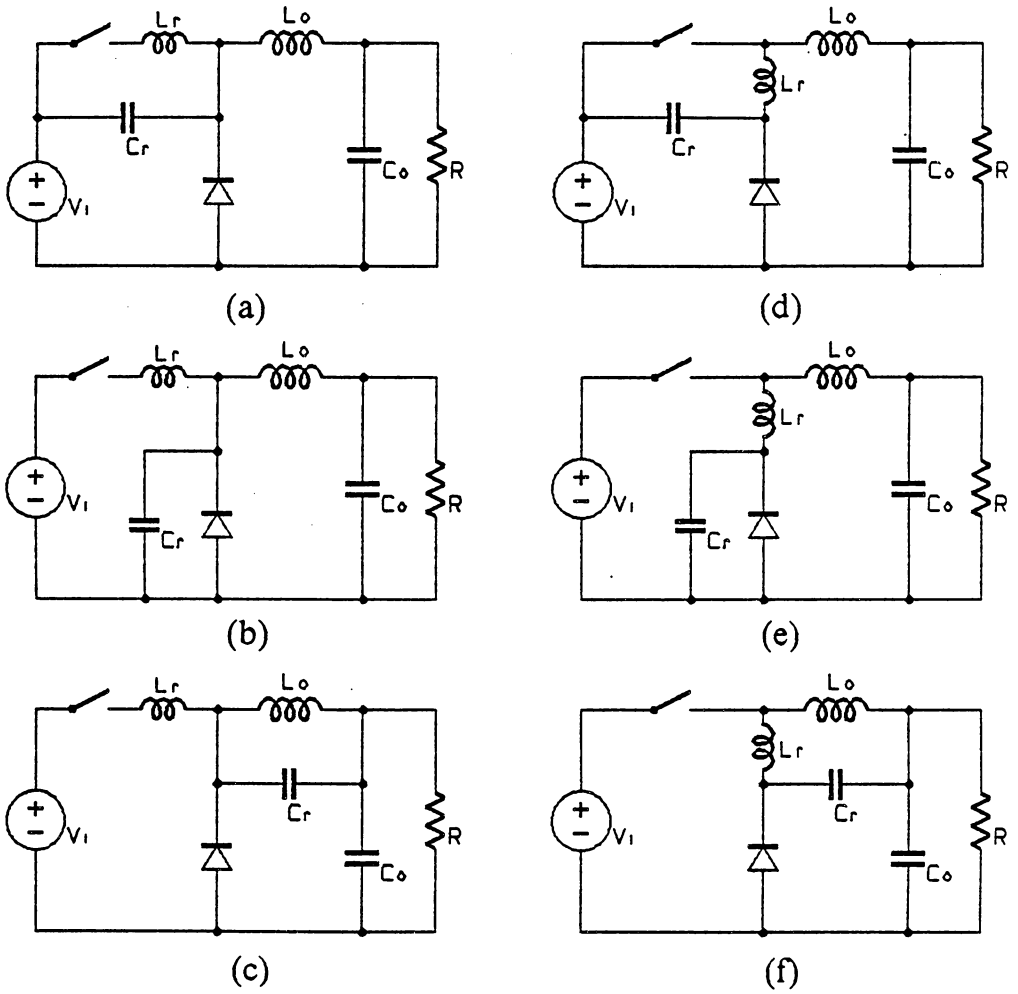


Fig. 4.36 Six variations of the ZCS, quasi-resonant buck converter

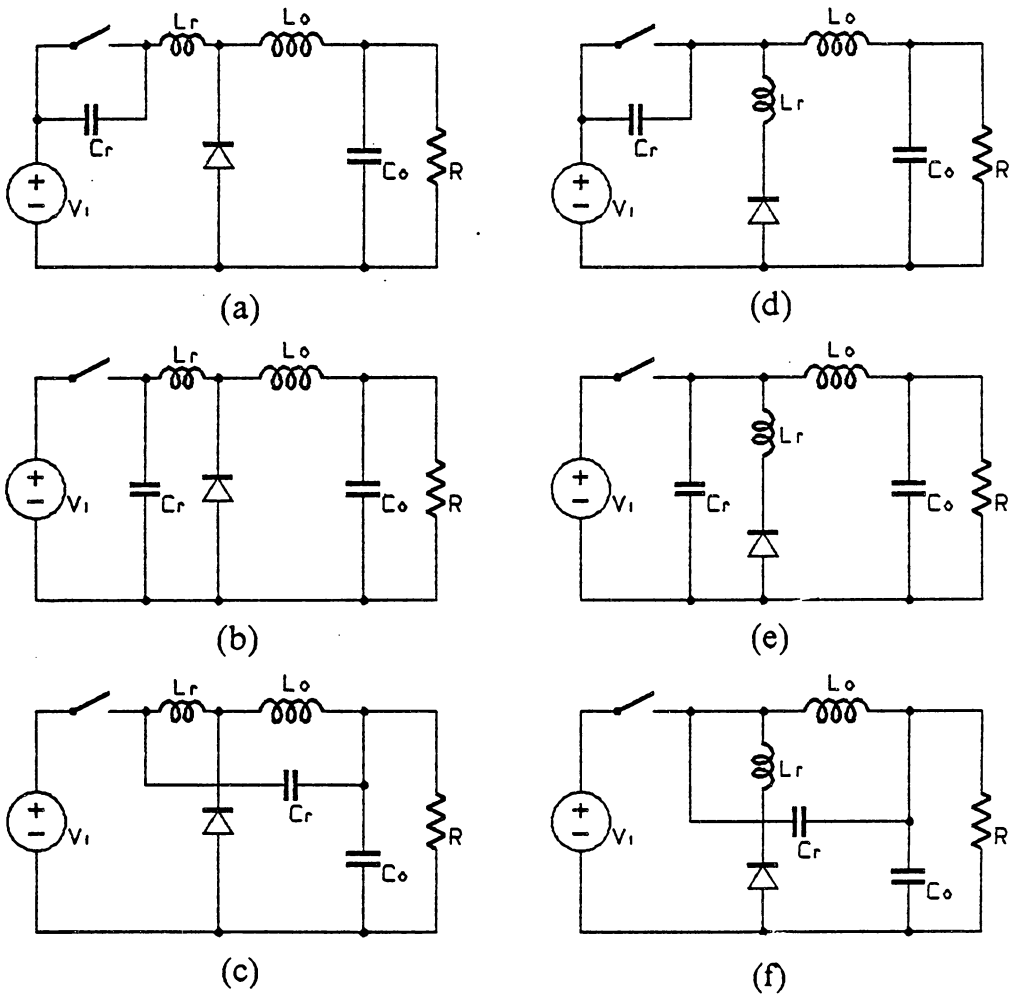


Fig. 4.37 Six variations of the ZVS, quasi-resonant buck converter

4.5. Review of Dual Networks and the Duality Principle

This sub-section reviews the basic concepts of dual networks and the duality principle. Most of the material in this section is from "Basic Circuit Theory" by Deseor and Kuh [G1]. For more detail, the original book and other textbooks on circuit theory are recommended [G2-G4].

4.5.1. Planar Graphs and Meshes

A **graph** is defined as a set of **nodes** and a set of **branches** connected in such a way that the two ends of each branch are terminated into two nodes.

A graph is said to be **planar** if it can be drawn on the plane in such a way that no two branches intersect at a point which is not a node. For example, the graph in Fig. 4.38a is a planar graph, whereas the graph in Fig. 4.38b is not.

In a planar graph, a closed loop which contains no branches in its interior is called a **mesh**. Furthermore, the loop that contains no branches in its exterior is called the **outer mesh**. For example, the graph in Fig. 4.38a contains four meshes: ***bcd, def, aeg,*** and ***abcfg***, where mesh ***abcfg*** is the outer mesh.

An unhinged graph has the property that when partitioned into two connected non-degenerated subgraphs, the subgraphs have at least two nodes in common.

The graph in Fig. 4.39a is an unhinged graph, whereas the graphs in Figs. 4.39b and 4.39c are not.

It can be shown for a connected, unhinged, planar graph the number of meshes is equal to $b - n_t + 1$.

$$l = b - n_t + 1 \tag{4.3}$$

where l is the number of meshes, b is the number of branches, and n_t is the number of nodes.

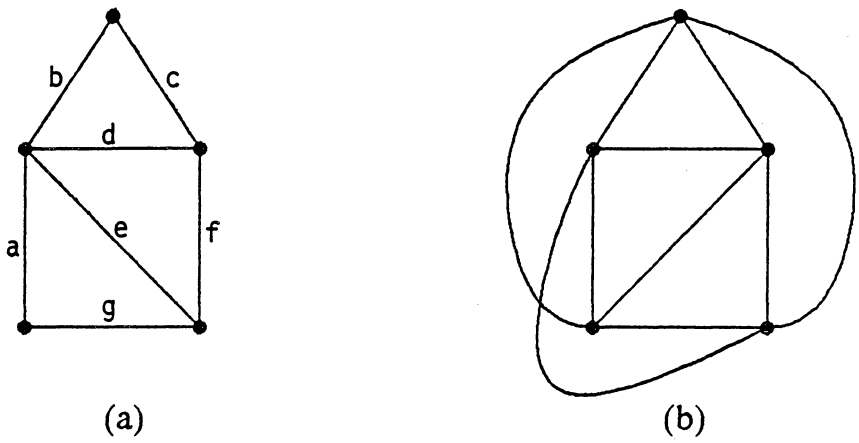


Fig. 4.38 (a) A planar graph (b) A non-planar graph

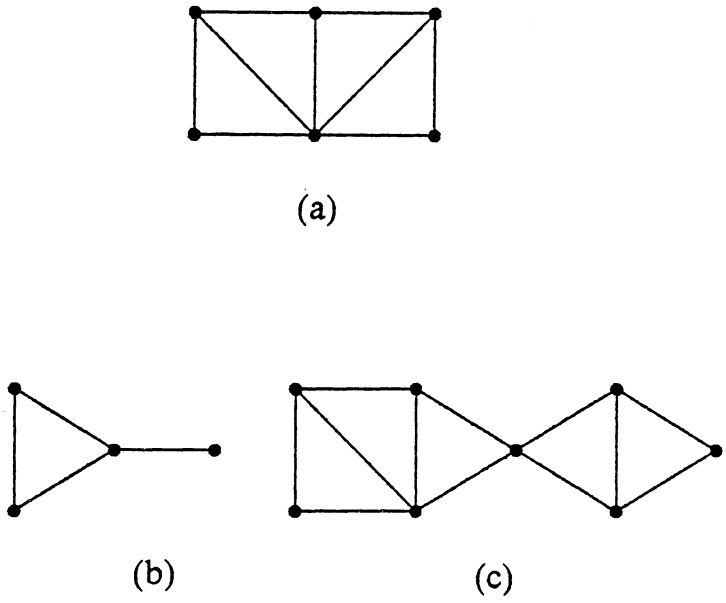


Fig. 4.39 (a) An unhinged graph (b),(c) Hinged graphs

4.5.2. Dual Graphs and Algorithm for Dual Graph Construction

Assume a topological graph, G, is a connected, unhinged and planar graph. G contains $n_t = n + 1$ nodes, b branches and, therefore, $l = b - n$ branches (not counting the outer mesh). A planar topological graph, G', is said to be a **dual graph** of G if:

1. *There is one-to-one correspondence between the meshes of G (including the outer mesh) and the nodes of G', and vice versa.*

2. *There is a one-to-one correspondence between the branches of each graph in such a way that whenever two meshes of one graph have a branch in common, the corresponding nodes of the other graph have the corresponding branch connecting these two nodes.*

From the above definition and Eq. (4.3), graph G' has b branches, $l+1$ node, n meshes, and one outer mesh. It is easily seen that if G' is a dual graph of G, then G is a dual of G'. In other words, duality is a symmetrical relation between connected, unhinged, planar topological graphs.

Given a connected, unhinged, planar graph G, its dual graph, G', can be constructed as follows:

1. *For each mesh, m_i, in G, assign a node, n'_i,* to G'.

2. *For each branch of G, e.g.* b_{jk} *, which is common to mesh* m_j and m_k *, connect a branch,* b'_{jk} , from node n'_j to node n'_k .

3. *In case the given graph G is oriented, i.e., each branch has a reference direction, the reference direction of a branch of G' is obtained from that of the corresponding branch of G by rotating the vector 90 degrees counterclockwise.*

The graphs shown in Fig. 4.40 illustrate the construction procedure of a dual graph. The graph in Fig. 4.40a has 5 branches, 4 nodes, and 3 meshes (including the outer mesh). By following the procedure described above, the construction of a dual graph is shown in Fig. 4.40b. The resulting dual graph is shown in Fig. 4.40c.

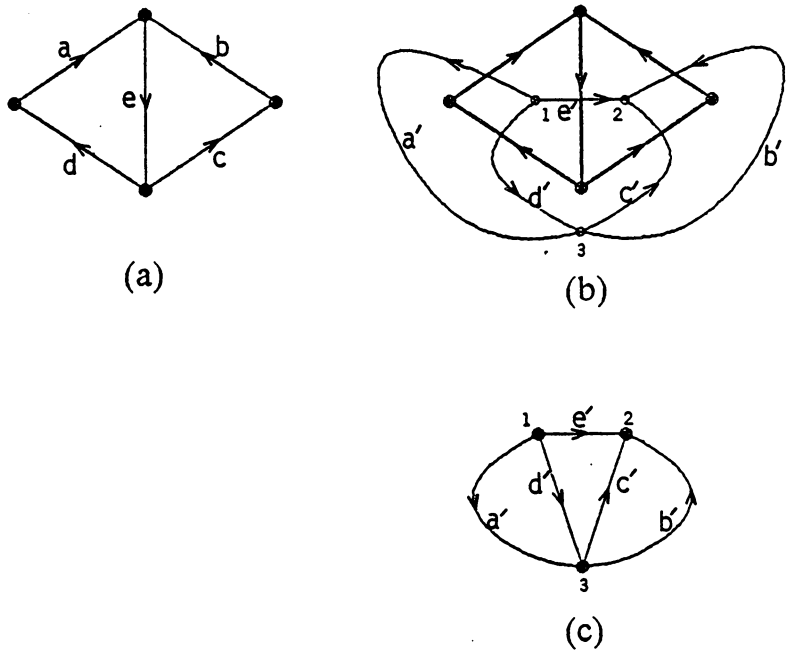


Fig. 4.40 Construction of a dual graph
(a) the original graph
(b) construction of a dual graph
(c) the resultant graph

4.5.3. Dual Networks and The Duality Principle

Network N' is said to be the dual of network N if

1. *The topological graph G' representing N' is the dual of the topological graph G representing N.*

2. *The branch equation of a branch of N' is obtained from its corresponding equation of N by performing the following substitutions:*

$$v \rightarrow j', \quad j \rightarrow v', \quad q \rightarrow \varphi', \quad \varphi \rightarrow q'$$

In other words, dual elements are obtained from the original elements by performing the following substitutions:

$$L \rightarrow C', \quad C \rightarrow L', \quad R \rightarrow G', \quad G \rightarrow R', \quad I_g \rightarrow V'_g, \quad V_g \rightarrow I'_g$$

The duality principle is a general assertion concerning a network and its dual:

Consider an arbitrary planar network, N, and its dual, N' . Let S be any true statement concerning the behavior of N. Let S' be the statement obtained from S by replacing every graph-theoretic word or phrase (node, mesh, loop, etc.) by its dual and every electrical quantity (voltage, current, impedance, etc.) by its dual. Then S' is a true statement concerning the behavior of N'.

The concept of dual networks and the duality principle are very powerful tools in studying the topological properties of converter circuits. In the following sections, the duality in the PWM converter topologies and the duality between the zero-current switching and the zero-voltage switching techniques are discussed.

4.6. Duality in Basic Converters

Each basic topology in the class of single-active switch, two-topology, ladder-structured converters contains an active switch (transistor) and a passive switch (diode). Although the dual network and the duality principles are valid when applied to any arbitrary, planar, connected network (whether it is linear or non-linear, time-invariant or time-varying), there is no direct dual substitution for a switch or a diode. This problem is resolved by finding the duals of the two equivalent circuits corresponding to the two states of the switches. (Notice that when the active switch is open, the passive switch is closed, and vice versa). By combining the two obtained dual networks, a complete dual converter is found [F9].

Figure 4.41a shows a buck converter. Its equivalent circuits during the on-time and the off-time of the active switch are shown in Figs. 4.41b and 4.41c, respectively. By applying the dual network construction procedure described in Sec. 4.5, two circuits are obtained, as shown in Figs. 4.41d and 4.41e. It can be seen that the complete dual converter is a boost converter.

Notice that a switch or a diode is modelled as an open circuit or a short circuit depending on its on-off state. An open circuit can be treated as a resistor with an infinite resistance, and a short circuit can be treated as a resistor with zero resistance. Therefore, the dual of an open circuit is a short circuit, and vice versa.

Also, notice that the on-time of the buck converter corresponds to the off-time of the boost converter, because the dual of the on-state (short circuit) of the

switch is an off-state (open circuit). Hence, in the class of two-topology converters, the duality relationship on the duty ratio can be established. That is, the dual of D is D', and vice versa.

For the buck converter, the dc voltage-conversion ratio, $\frac{V_o}{V_s}$, can be expressed as

$$\frac{V_o}{V_s} = D \tag{4.4}$$

By invoking the duality principle, we obtain, for the boost converter,

$$\frac{I_o}{I_s} = D' \tag{4.5}$$

From the input-output power balance of the boost converter,

$$V_i I_i = V_o I_o$$

where V_o, I_o are average values of the output voltage and the output current, respectively. Therefore,

$$\frac{V_o}{V_s} = \frac{1}{D'} \tag{4.6}$$

Equation (4.6) is exactly the expression for the dc voltage-conversion ratio of the boost converter.

Similarly, the duality relationships can be established between the buck/boost converter and the Cuk converter and between the Zeta converter and the SEPIC

converter. Figure 4.42 shows the evolution from the buck/boost converter to a Cuk converter by applying the dual networks construction procedure [F9].

The creation of the concept of the voltage source and the current source, the voltage load and current load has now proved to be very useful, especially in establishing the duality relationship in switching converters. It eliminates the problems associated with the duality of filter elements. For example, in his paper [F9], Cuk had to artificially create a **buck current converter** to match the duality between the buck converter and the boost converter because a proper way of dealing with the duality of filter elements was not found.

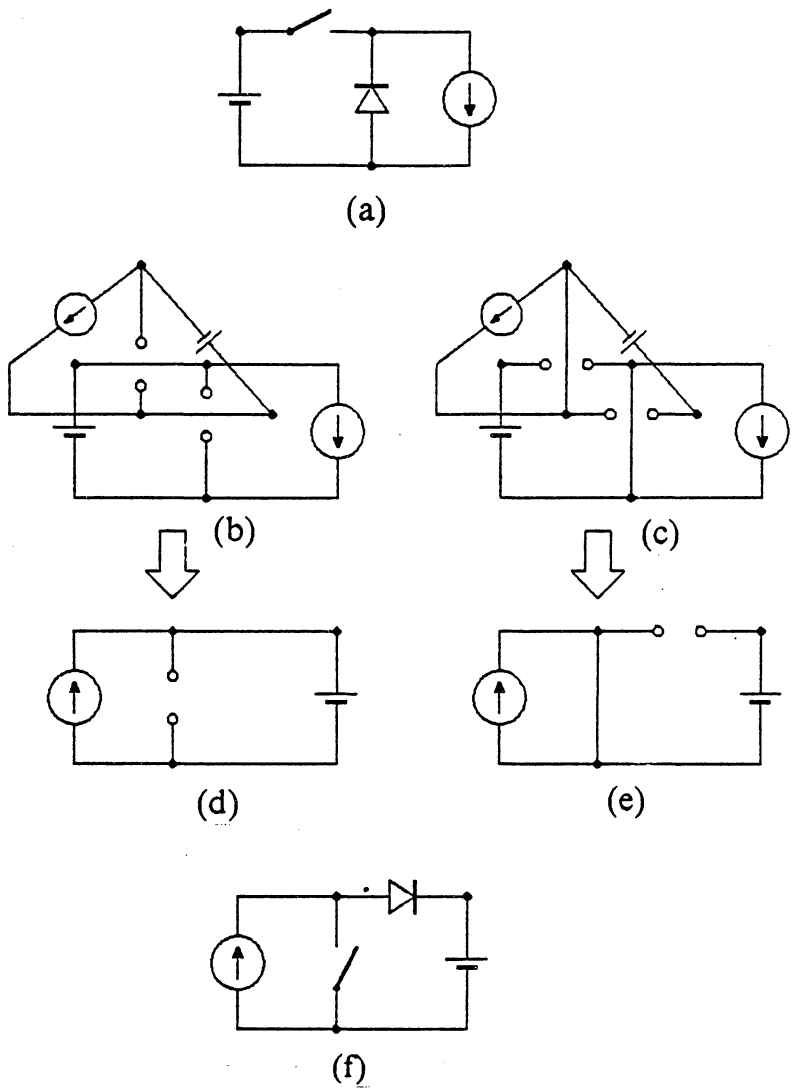


Fig. 4.41 Dual networks between the buck and the boost converters
(a) the buck converter
(b) equivalent circuit of the buck converter at on-time
(c) equivalent circuit of the buck converter at off-time
(d) dual network of the buck converter at on-time
(e) dual network of the buck converter at off-time
(f) the complete dual converter

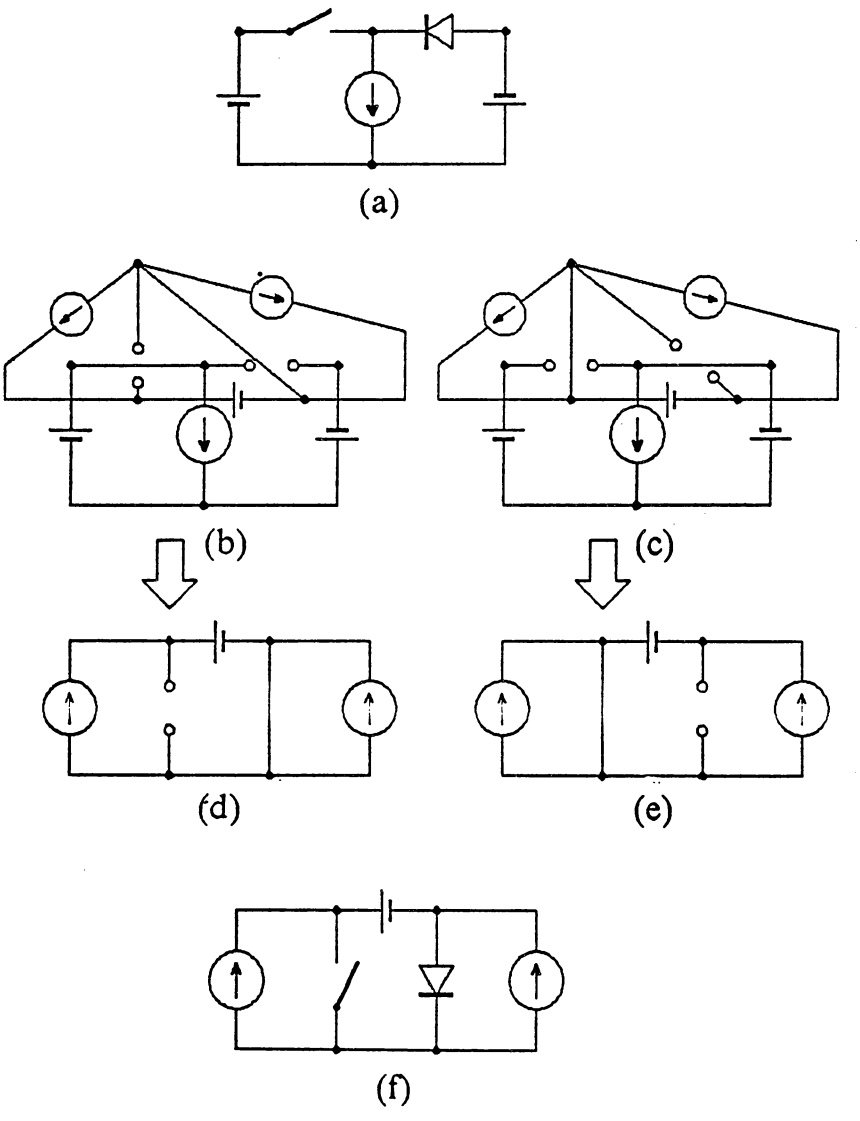


Fig. 4.42 Dual networks between the buck/boost and the Cuk converters
(a) the buck/boost converter
(b) equivalent circuit of the buck/boost converter at on-time
(c) equivalent circuit of the buck/boost converter at off-time
(d) dual network of the buck/boost converter at on-time
(e) dual network of the buck/boost converter at off-time
(f) the complete dual converter

4.7. Duality between the Families of ZCS and ZVS Quasi-Resonant Converters

Unlike the conventional PWM converter operating in a continuous mode, a ZCS or a ZVS, quasi-resonant converter has four topologies (equivalent circuits) corresponding to the four stages in a switching cycle. The addition of a resonant tank circuit allows the active switch (transistor) and the passive switch (diode) to be both on, both off, or one on and one off. Therefore, a switching cycle is divided into four stages according to the four different on-off combinations of the active switch and the passive switch. To derive a dual converter from a given converter, the dual network construction procedure is to be applied to each of the four equivalent circuits.

Interestingly, when the dual network and the duality principle are applied to a given ZCS or ZVS, quasi-resonant converter, a dual converter is found in the other family of quasi-resonant converters.

For example, Fig. 4.43a shows a ZCS, quasi-resonant buck converter. Its four equivalent circuits are shown in Figs. 4.43b-4.43e. By applying the dual network construction procedure, as described in Sec. 4.5, four dual networks for the four equivalent circuits are derived, as shown in Figs. 4.43g-4.43j. It can be seen that the equivalent circuits shown in Figs. 4.43g-4.43j are exactly the same as those in Figs. 3.3a-3.3d. Therefore, we can conclude that the ZVS, quasi-resonant boost converter is a dual of the ZCS, quasi-resonant buck converter.

Similarly, it can be proved that the duality is a general topological property existing between the family of ZCS, quasi-resonant converters and the family of ZVS, quasi-resonant converters. Table 4.1 shows the dual pairs among the basic topologies in these two families of converters.

Since we have shown a dual network of the ZCS, quasi-resonant buck converter is the ZVS, quasi-resonant boost converter, we expect the expressions for their dc voltage-conversion ratios to be dual statements. This can be verified as follows.

The voltage-conversion ratio of the ZCS, quasi-resonant buck converter operating in the half-wave mode is obtained and shown as Eq. (2.9). For convenience, Eq. (2.9) is repeated here:

$$\frac{V_o}{V_i} \equiv x = \frac{f_s}{2\pi f_n}\left[\sin^{-1}\left(\frac{-x}{r}\right) + \frac{x}{2r} + \frac{r}{x}\sqrt{1-\left(\frac{x}{r}\right)^2} \right] \tag{4.7}$$

If we take the dual of Eq. (4.7), then

$$\frac{I'_o}{I'_i} \equiv y' = \frac{f_s}{2\pi f_n}\left[\sin^{-1}\left(-y'r\right) + \frac{y'r}{2} + \frac{1}{y'r}\sqrt{1-(y'r)^2} \right] \tag{4.8}$$

From the input-output power balance of the ZVS, quasi-resonant boost converter,

$$V'_i I'_i = V'_o I'_o \tag{4.9}$$

where V'_o, I'_o are average values of the output voltage and the output current, respectively. Therefore,

$$y' \equiv \frac{I'_o}{I'_i} = \frac{V'_i}{V'_o} = \frac{1}{x'} \tag{4.10}$$

By substituting Eq. (4.10) into Eq. (4.8), we obtain

$$\frac{1}{x'} = \frac{f_s}{2\pi f_n}\left[\sin^{-1}\left(\frac{-r}{x'}\right) + \frac{r}{2x'} + \frac{x'}{r}\sqrt{1 - \left(\frac{r}{x'}\right)^2} \right] \tag{4.11}$$

Equation (4.11), which is derived directly from the duality principle, is proved to be the same as Eq. (3.8), which is derived from steady-state analysis.

Similar duality relationships can be derived between the dc voltage-conversion ratio of any given ZCS or ZVS, quasi-resonant converter and that of its dual counterpart in the other quasi-resonant converter family.

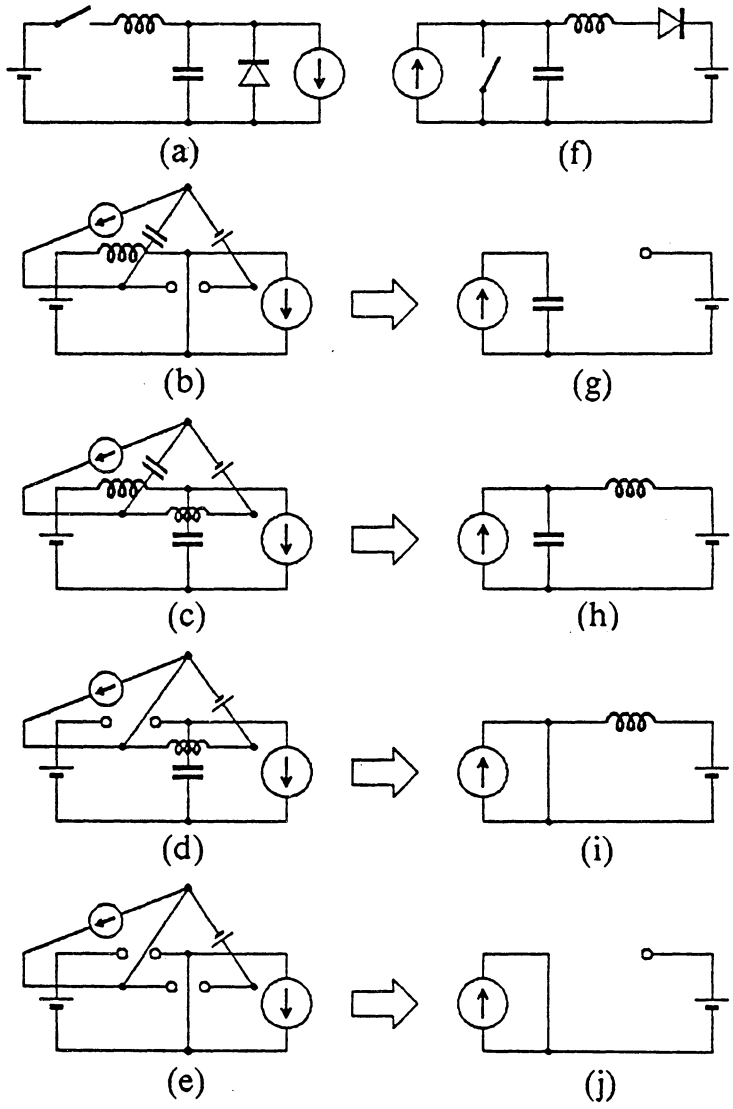


Fig. 4.43 The dual networks relationship

(a) the topology of a ZCS, quasi-resonant buck converter

(b)-(e) the equivalent circuits of the ZCS, quasi-resonant buck converter during the four switching stages

(f) the topology of a ZVS, quasi-resonant boost converter

(g)-(j) the equivalent circuits of the ZVS, quasi-resonant boost converter during the four switching stages

Table 4.1. Dual pairs between the ZCS and the ZVS quasi-resonant converter families

ZCS Quasi-Resonant	ZVS Quasi-Resonant
buck	*boost*
boost	*buck*
buck/boost	*Cuk*
Cuk	*buck/boost*
SEPIC	*Zeta*
Zeta	*SEPIC*

4.8. Comparison between ZCS and ZVS Quasi-Resonant Converters

In this section, a comparison is made on the salient features of the ZCS and the ZVS, quasi-resonant converters. This comparison not only highlights the merits and limitations of the two families of quasi-resonant converters, it also serves as a verification on the duality relationship between them.

1. **Switch's current waveform**

   A ZCS, quasi-resonant converter employs the zero-current switching technique. Its power switch has a quasi-sinusoidal current waveform, which provides a natural commutation.

   The switch in a ZVS, quasi-resonant converter has a quasi-square current waveform similar to that of a corresponding PWM converter.

2. **Switch's voltage waveform**

   The power switch in a ZCS, quasi-resonant converter has a quasi-square voltage waveform similar to that of a corresponding PWM converter.

   A ZVS, quasi-resonant converter employs the zero-voltage switching technique. Its power switch has a quasi-sinusoidal voltage waveform.

3. **Half-wave mode implementation**

To implement a half-wave, ZCS, quasi-resonant converter, a diode is connected in series with the power switch to provide reverse-blocking capability.

For a half-wave, ZVS, quasi-resonant converter, a diode is connected in anti-parallel with the power switch to provide reverse-conduction capability.

4. **Full-wave mode implementation**

To implement a full-wave, ZCS, quasi-resonant converter, a diode is connected in anti-parallel with the power switch to provide reverse-conduction capability.

For a full-wave, ZVS, quasi-resonant converter, a diode is connected in series with the power switch to provide reverse-blocking capability.

5. **Voltage stress on switch**

For a ZCS, quasi-resonant converter, the off-state voltage stress on its power switch is the same as in a corresponding PWM converter.

For a ZVS, quasi-resonant converter, the off-state voltage stress on its power switch is higher, and the peak value of the off-state voltage increases as the load current is increased.

6. **Current stress on switch**

For a ZCS, quasi-resonant converter, the peak current value during the conduction time of its power switch is higher than that in a corresponding

PWM converter. The peak current value increases as the load current is increased.

For a ZVS, quasi-resonant converter, the current stress on its power switch is the same as in a corresponding PWM converter.

7. **Voltage-conversion ratio vs. switching frequency**

In a ZCS, quasi-resonant converter, the length of on-time is kept constant. Increasing the switching frequency will increase the equivalent duty ratio, therefore, increasing the voltage-conversion ratio.

In a ZVS, quasi-resonant converter, the length of off-time is kept constant. Increasing the switching frequency will decrease the equivalent duty ratio, therefore, decreasing the voltage-conversion ratio.

8. **Sensitivity of output voltage to load variation**

For either a ZCS or a ZVS, quasi-resonant converter, when operated under a given input voltage and a given switching frequency, its output voltage is load-insensitive in the full-wave mode of operation. In the half-wave mode of operation, the output voltage is sensitive to the load variation. It increases as the load current is decreased.

9. **Regulation scheme**

In a ZCS, quasi-resonant converter, the on-time is determined by the natural frequency of the resonant tank. Therefore, a constant on-time must be maintained. To regulate the output voltage against line and load variations, the off-time is varied, i.e., a constant on-time control is used.

In a ZVS, quasi-resonant converter, the off-time is determined by the natural frequency of the resonant tank. Therefore, a constant off-time must be maintained. To regulate the output voltage against line and load variations, the on-time is varied, i.e., a constant off-time control is used.

10. **Load range**

In a ZCS, quasi-resonant converter, when the load current is increased beyond a limit, the zero-current switching property will be lost. As a result, its load range is from a minimum load resistance to a infinite load resistance (open circuit).

In a ZVS, quasi-resonant converter, when the load current is too small, the zero-voltage switching property will be lost. As a result, its load range is from a zero load resistance (short circuit) to a maximum load resistance.

5. TOPOLOGICAL REFINEMENTS BY UTILIZING PARASITIC ELEMENTS

In high-frequency operations, parasitic elements in the circuit often cause detrimental effects to the converters. Particularly, the two most predominant circuit parasitics are the leakage inductances of the transformer and the junction capacitances of the semiconductor switch. In this chapter, the techniques of incorporating these two types of parasitic elements into resonant components required by the quasi-resonant converters are presented.

5.1. Secondary-Side Resonance

In most dc-dc converter circuits a transformer is required for dc isolation and to obtain a large voltage-conversion ratio. Due to imperfect coupling between the primary and secondary windings, leakage inductances are intrinsic to all transformers. The leakage inductance often induces high switching stress and switching loss on the semiconductor switching devices. To implement isolation in resonant and quasi-resonant converters, it is advantageous to utilize the leakage inductance as a part of the resonant tank circuit.

5.1.1. Basic Resonant Converters

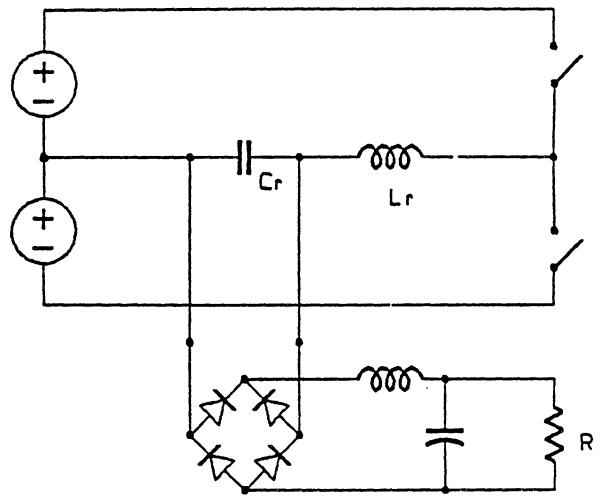
There are two basic resonant converters: the **Parallel-Resonant Converter** (PRC), and the **Series-Resonant Converter** (SRC). The PRC and the SRC both can be implemented in a half-bridge, a full-bridge, or a push-pull configuration. Figures 5.1a and 5.1b show the PRC and the SRC implemented in half-bridge configurations, respectively.

Essential to the topology of a resonant converter is an **LC resonant tank circuit** which is excited repetitively by the power source through the gating of semiconductor switches. Output power can be tapped either from the tank's capacitor

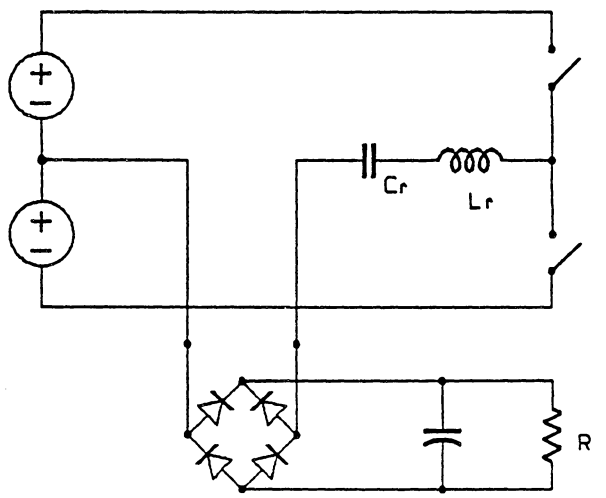
voltage or from the tank's inductor current. The former case is often referred to as the parallel-resonant converter, and the latter, as the series-resonant converter.

As described in Sec. 4.1, a load circuit appears either as a constant current or a constant voltage to the converter. Again, for ease of treatment, the load circuit with an output-filtering inductor preceding an output-filtering capacitor is regarded as a **current load** (Fig. 5.2a); while the load circuit containing only an output-filtering capacitor is regarded as a **voltage load** (Fig. 5.2b).

In general, for a PRC, the capacitor voltage is rectified and fed into a **current load**, as shown in Fig. 5.3a; while in an SRC, the tank's current is rectified and fed into a **voltage load**, as shown in Fig. 5.3b. Although a modified PRC circuit which does not contain output inductors has been proposed [D18, D26], the mode of operation in this circuit is very different from those of the conventional PRC circuits [D26].



(a)



(b)

Fig. 5.1. (a) Parallel-resonant converter
(b) Series-resonant converter

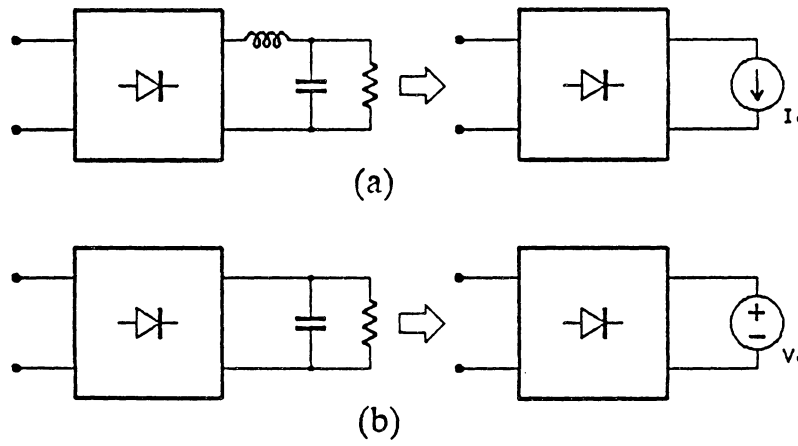


Fig. 5.2. Load types (a) current load (b) voltage load

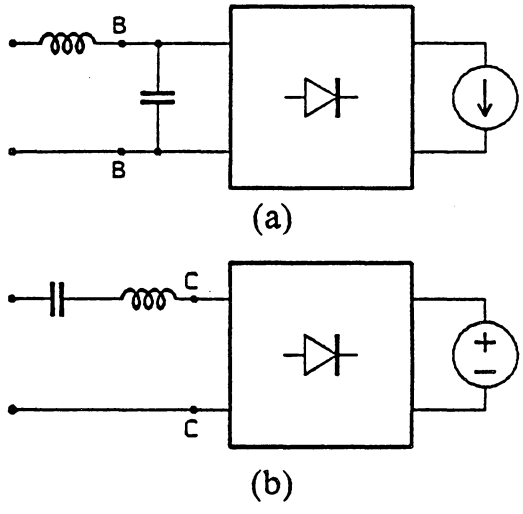


Fig. 5.3. (a) PRC with a current load
(b) SRC with a voltage load

5.1.2. Secondary-Side Resonance in Resonant Converters

To utilize the leakage inductances of the transformer as a resonant element in a PRC, the resonant capacitor must be connected across the secondary winding, as shown in Fig. 5.4a. In an SRC, the resonant capacitor can be connected either in series with the primary winding, as shown in Fig. 5.4b, or in series with the secondary winding, as shown in Fig. 5.4c.

A PRC in a half-bridge configuration with a center-tapped secondary winding is shown in Fig. 5.5a. By moving the resonant capacitor to the secondary-side, as shown in Fig. 5.5b, the resonant tank now consists of the leakage inductances of the transformer and the secondary-side capacitor; thus, it is given the name of secondary-side resonance. Since no electrical properties have been altered in the process of this topological transformation, all the operation modes and circuit characteristics of the PRC are conserved in the new topology.

Similar topological transformations employing the secondary-side resonance technique can be applied to PRC circuits implemented in the full-bridge and the push-pull configurations.

For the SRC, it is generally more favorable to connect the resonant capacitor on the primary side. The advantages of using a primary-side resonant capacitor are:

- The capacitor also serves as a dc-voltage decoupler and provides protection against flux imbalance in the transformer.

- The secondary side can use a center-tapped winding and a two-diode rectifier network, as shown in Fig. 5.6a.

- For voltage step-down applications, the size of a primary-side capacitor and its ac current can be considerably smaller than those of a secondary-side capacitor.

However, in some configurations, e.g., a push-pull SRC, the resonant capacitor can only be connected on the secondary side, as shown in Fig. 5.6b.

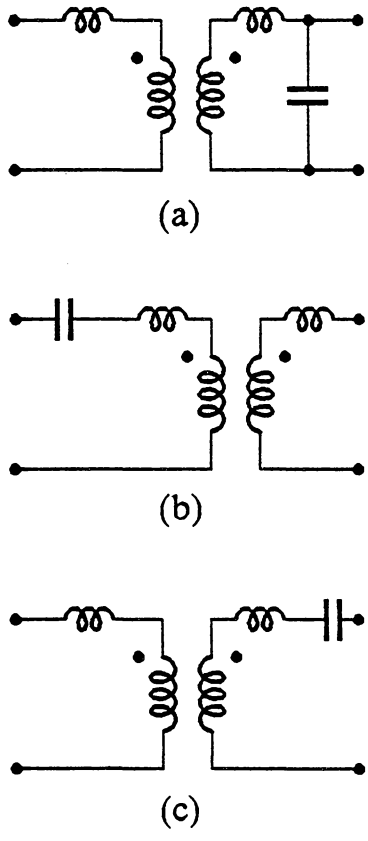


Fig. 5.4. Utilizing the leakage inductances of transformer
(a) PRC with a secondary-side resonant capacitor
(b) SRC with a primary-side resonant capacitor
(c) SRC with a secondary-side resonant capacitor

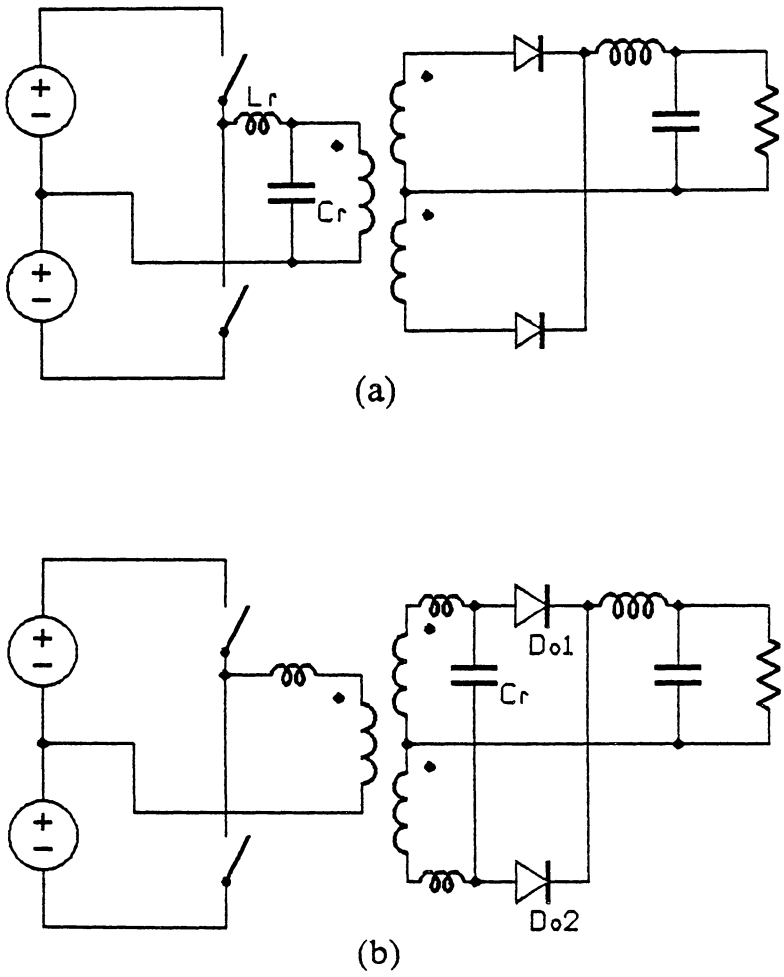


Fig. 5.5. A half-bridge PRC with
(a) resonant capacitor on the primary side
(b) secondary-side resonance

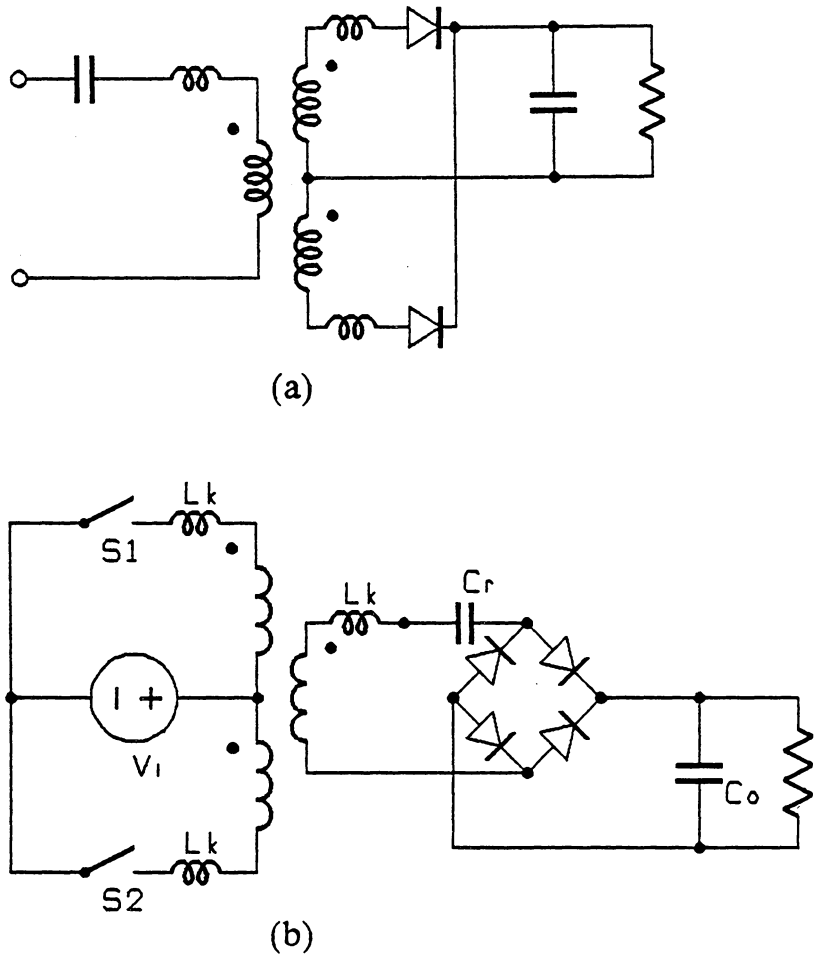


Fig. 5.6. Configuration of an SRC with the resonant capacitor
(a) on the primary side
(b) on the secondary side

5.2. Secondary-Side Resonance in ZCS, Quasi-Resonant Converters

5.2.1. Forward Converter with Secondary-Side Resonance

A ZCS, quasi-resonant forward converter is shown in Fig. 5.7a, where L_r and C_r are the resonant elements for waveform shaping. Two topologies can be derived from this circuit by moving resonant capacitor C_r to the secondary side of the transformer. Capacitor C_r can be connected directly across the secondary winding of the transformer, as shown in Fig. 5.7b, or in parallel with diode D_o, as shown in Fig. 5.7c. In both cases, the leakage inductances of the transformer are used as the resonant inductor, and for simplicity of discussion the leakage inductances of the primary and secondary windings are lumped together as a single primary leakage inductance. Notice that the circuit shown in Fig. 5.7c was invented by Dr. P. Vinciarelli of Victor Company [B6]. The detail of the Vicor circuit will be described in Sec. 5.2.2.

With the exception of the magnetizing inductance and the flux-resetting problem, this forward converter with secondary-side resonance (Fig. 5.7b) is equivalent to the ZCS, quasi-resonant buck converter. The resonant tank circuit of this converter consists of the leakage inductance of the transformer, L_k, and a capacitor, C_r, on the secondary side of the transformer.

To illustrate the operation of the forward converter with secondary-side resonance (Fig. 5.7b), the equivalent circuits of the converter during different stages in a switching cycle are shown in Fig. 5.8. Notice the power transformer is modelled as consisting of a leakage inductance reflected to the primary side, L_r , and a magnetizing inductance, L_m .

At the beginning of a switching cycle, the load current, I_o, is free-wheeling through L_m-D_3, and D_4 (see Fig. 5.8a). Voltage across C_r is zero. After switch S_1 turns on, the entire input voltage is imposed on L_r. I_{Lr} rises linearly, until it reaches the level of load current I_o. The equivalent circuit during this stage is shown in Fig. 5.8b. The predicted waveforms based on an idealized circuit are shown in Fig. 5.9.

Diode D_4 is off as soon as I_{Lr} becomes larger than I_o. Current through diode D_3 equals the output inductor current afterwards, I_{Lr} keeps increasing and part of it flows into capacitor C_r, and the voltage across C_r rises. As long as V_{Cr} is positive, the magnetizing current through L_m increases. The equivalent circuit during this stage is shown in Fig. 5.8c.

The resonance between L_r and C_r causes V_{Cr} to be charged from zero to twice of the input voltage, then I_{Lr} decreases and eventually drops to zero. Switch S_1, therefore, can turn off under a zero-current condition. The voltage on C_r keeps decreasing due to the discharging of C_r through the magnetizing inductor as well as through the output inductor. The equivalent circuit after switch S_1 turns off and before V_{Cr} drops to zero is shown in Fig. 5.8d.

After V_{Cr} drops to zero, diode D_4 cuts in and carries the load current. Diode D_3 is then reverse biased, with the magnetizing current, I_m, keeps charging capacitor C_r to a negative voltage. The equivalent circuit during this stage is shown in Fig. 5.8e.

Magnetizing current I_m gradually decreases to zero and, then, is driven to a negative value by the negative V_{Cr}, as shown in Fig. 5.8f.

Finally, V_{Cr} drops back to zero again, and diode D_3 cuts in. Part of the load current now is flowing through D_4, and part of it through L_m and D_3. The equivalent circuit of this stage is back to that of Fig. 5.8a.

The circuit operation, as illustrated in Fig. 5.8, indicates that the magnetizing current is charged to a negative value during the off-time. This property is advantageous since it leads to a better balanced excitation of the transformer core. Another advantage obtained in this circuit is that the flux-resetting is provided by the resonant capacitor, and the tertiary winding and a high-voltage, feed-back diode is no longer needed.

Experimental Results

A 30W, 800kHz forward converter with secondary-side resonance has been implemented on a breadboard [B10]. The input voltage is 120V. The full load current is 6A at 5V output. The schematic diagram of the circuit and the components used are shown in Fig. 5.10. A 600V, fast reverse-recovery diode, D_1, is connected in series with the MOSFET switch, Q_1, to disable the slow body-drain

diode of the MOSFET. Another fast diode, D_2, is connected in anti-parallel with D_1 and Q_1 to provide a reverse-conduction path.

Major waveforms of the circuit operating in the full-wave mode are shown in Fig. 5.11a. The higher voltage spike at turn-off is believed to be caused by the sharp reverse recovery of diode D_2. Major waveforms of the circuit operating in the half-wave mode (without diode D_2) are shown in Fig. 5.11b. The voltage spike at turn-off is much smaller than that of the full-wave mode of operation.

Notice that in both cases, resonant capacitor C_r across the secondary winding is charged to a negative value during the off-time. When V_{C_r} reaches its negative peak, the magnetizing current has dropped completely to zero. Before switch Q_1 turns on again, the magnetizing current is driven to a negative value. From the capacitor voltage waveform, it is seen that the magnetizing current is indeed driven to a negative value during the off-time.

In this circuit, the value of the magnetizing inductance of the transformer is selected small to allow a shorter flux-reset time. For the discussion of a similar circuit using a transformer with high magnetizing inductance, Ref. [B14] is recommended.

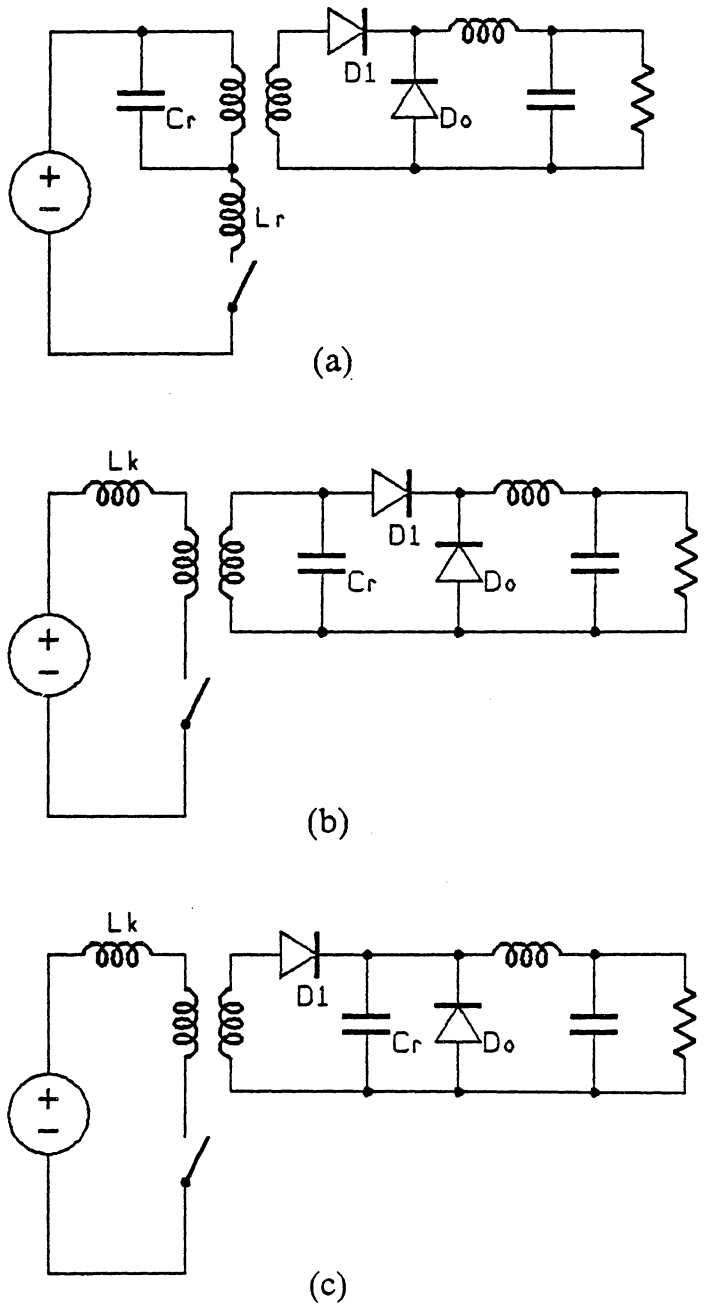


Fig. 5.7 (a) A quasi-resonant forward converter with an L-type resonant switch
(b) The forward converter with secondary-side resonance
(c) The Vicor circuit

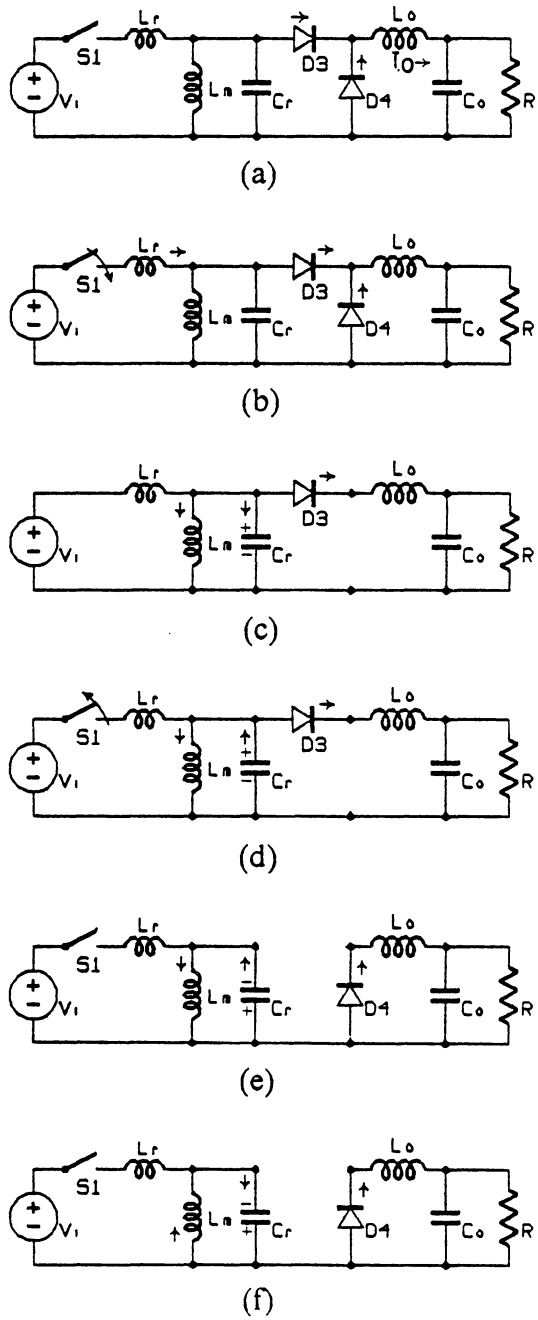


Fig. 5.8. The equivalent circuits of the forward converter with secondary-side resonance
(a) free-wheeling stage *(b) linear stage*
(c) resonant stage *(d) capacitor-discharging stage*
(e) magnetizing-current discharging stage
(f) reverse magnetizing-current stage

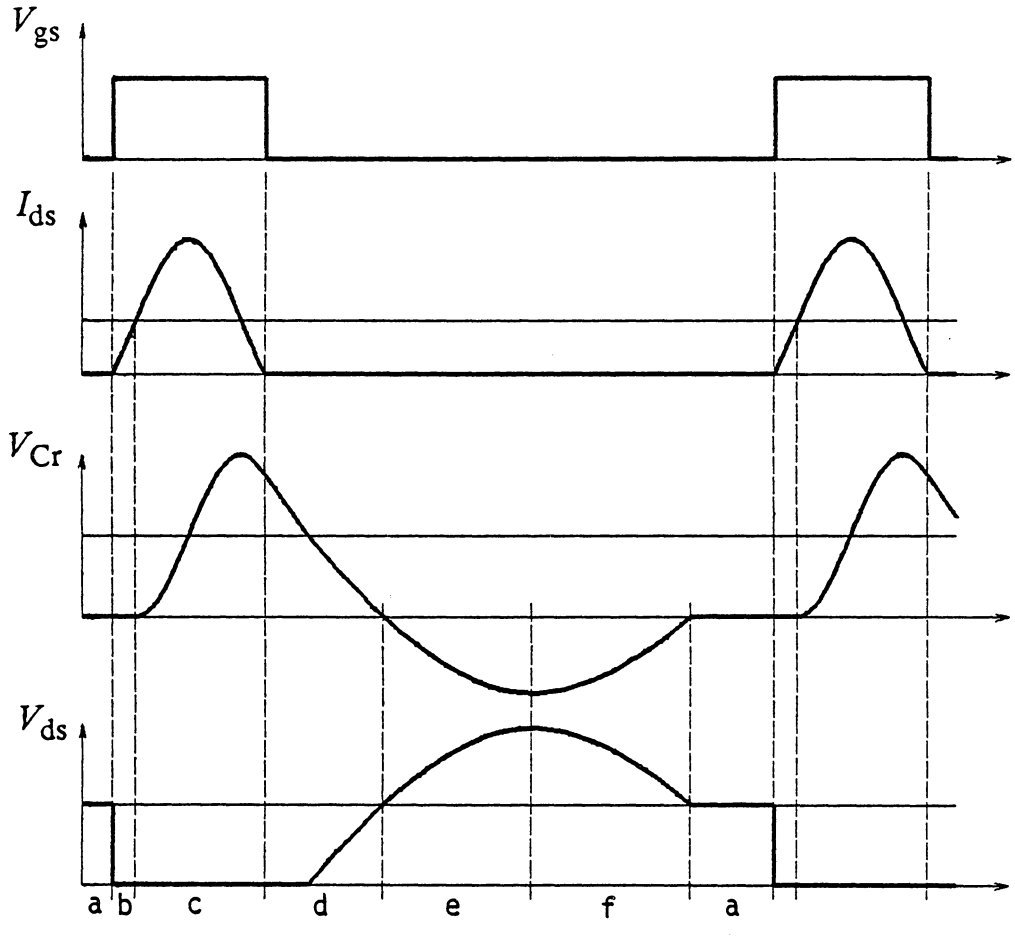


Fig. 5.9. Predicted waveforms of the forward converter with secondary-side resonance

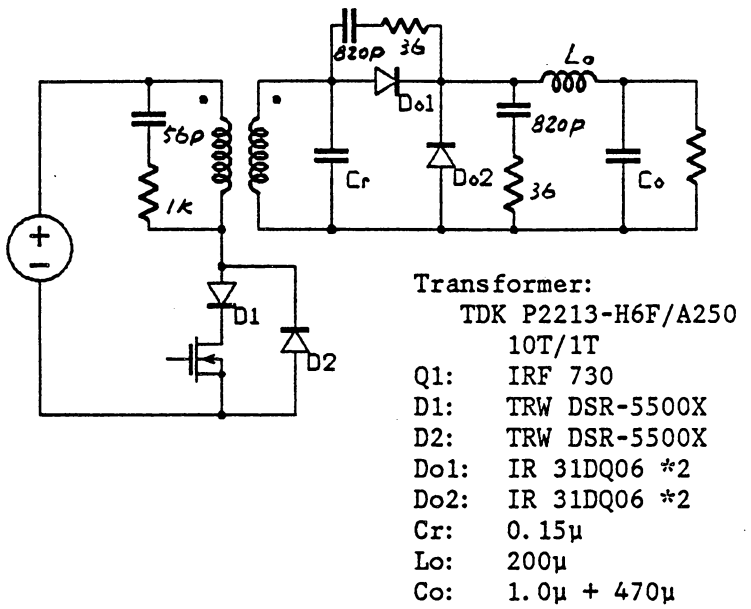
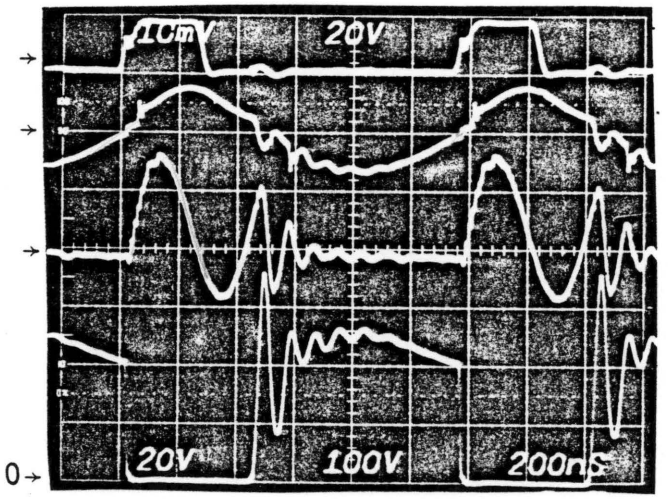
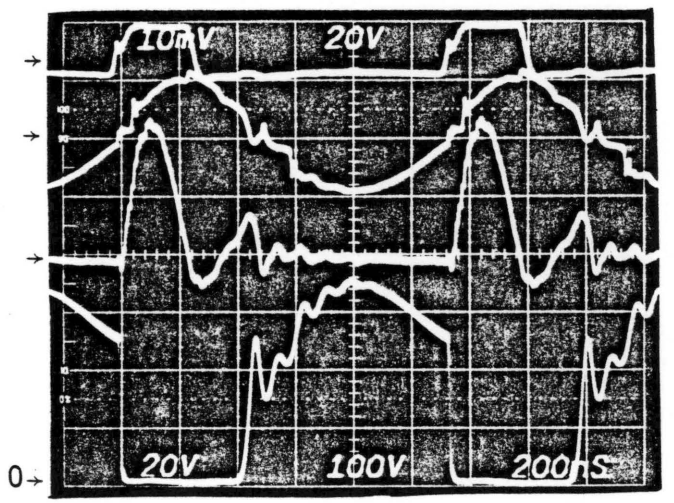


Fig. 5.10 A 800kHz, 30W forward converter with secondary-side resonance



(a)



(b)

(a) Vi = 120V, Vo = 3.56V, Io = 4.2A, fs = 856kHz,
1st waveform: Vgs (20V/div.) 2nd waveform: Vcr (20V/div.)
3rd waveform: Ip (1A/div.) 4th waveform: Vds (100V/div.)

(b) Vi = 150V, Vo = 5.24V, Io = 6.2A, fs = 856kHz,
1st waveform: Vgs (20V/div.) 2nd waveform: Vcr (20V/div.)
3rd waveform: Ip (1A/div.) 4th waveform: Vds (100V/div.)

Fig. 5.11 Waveforms from the circuit in Fig. 5.15.
(a) full-wave mode of operation
(b) half-wave mode of operation

5.2.2. Vicor Circuit

By replacing the transformer with a model consisting of the leakage inductance and the magnetizing inductance, the Vicor circuit can be simplified to the circuit shown in Fig. 5.12a. When the magnetizing inductance and its effect are neglected, the circuit can be further simplified to the half-wave mode, quasi-resonant buck converter, as shown in Fig. 5.12b.

The Vicor circuit also operates under the zero-current switching principle. However, because of the presence of diode D_1 , the Vicor circuit is limited to operation in the half-wave mode. In this circuit, each time the switch turns on, a packet of energy is transferred to capacitor C_r and, then, transferred to the load when the switch turns off. Since there is no feedback path for the energy to return to the source, the output voltage is sensitive to load variation as explained in Sec. 2.4.1. Consequently, to regulate the output voltage, the switching frequency has to be varied over a wide range.

Experimental Results

A Vicor circuit has been implemented as shown in Fig. 5.13a. The transformer has 8 turns in the primary winding and 2 turns in the secondary winding. The leakage inductance, L_k , and the magnetizing inductance, L_m , are estimated at 1.2μH and 300μH, both referred to the primary side. The resonant capacitor on the secondary side is 0.11μF. A Toshiba MOSFET, 2SK324 (400V, Rd=0.45 Ω, C_{oss}= 400pF) is used as the primary switch, S_1.

The major waveforms of the circuit operating at 300kHz are shown in Fig. 5.13b. The waveforms of V_{Cr} and I_{pri} (primary current of the transformer) clearly show the half-wave mode of operation. After S_1 turns off, and V_{Cr} drops below V_i/n (n is the turn ratio of the transformer), the magnetizing current then flows into C_{DS}. Voltage across C_{DS} rises to about 150V, and the magnetizing current is reset by the accumulated voltage across capacitance C_{DS}. Magnetizing current I_m is reset completely after about 2 μsec.

The drawback of using the junction capacitance as the reset circuit is that the time constant of the reset time is determined by the junction capacitance and the magnetizing inductance, which is generally too large. To provide a better flux-resetting mechanism, Vinciarelli invented a **magnetizing-current mirror** circuit [B7].

Magnetizing-Current Mirror

The essence of the magnetizing-current mirror is an auxiliary voltage source for flux resetting. Figure 5.14a shows a typical magnetizing-current mirror implemented on a conventional forward converter. The resetting capacitor, C_m, is connected across the secondary winding of the transformer through the gating of a MOSFET switch, S_2 (consisting of Q_2 and D_2). Generally, the value of C_m is selected large enough such that the voltage on C_m is constant throughout a switching cycle.

In normal operation, Q_1 and Q_2 turn on alternately. During the on-time of Q_1, the primary current of the transformer contains two components: the reflected

load current and the magnetizing current. After Q_1 turns off, the load current flows through the free-wheeling diode, D_{o2}. The magnetizing current, I_m, flows into capacitor C_m through diode D_2. After the magnetizing current drops to zero, it is further driven to flow in the reverse direction by the capacitor voltage, assuming Q_2 has been turned on by this time. Before Q_1 turns on and Q_2 turns off at the beginning of the next switching-cycle, I_m has already obtained a negative value.

The behavior of the magnetizing-current mirror circuit during steady-state operation can be seen more easily from the waveforms shown in Fig. 5.14b.

It can be shown that, in steady-state operation, the requirements of the flux balance on the transformer and the charge balance on the resetting capacitor will drive the voltage across C_m to $\frac{V_i D}{1 - D}$. The magnetizing current, I_m, settles down to a pure ac waveform, as shown in Fig. 5.14b.

Two observations can be made regarding the magnetizing-current mirror. First, this circuit can be implemented either on the primary side or on the secondary side of the transformer. Second, this magnetizing-current mirror technique can be applied to the conventional forward converter as well as the quasi-resonant forward converter.

The magnetizing-current mirror technique provides the following advantages:

- It eliminates the need of the flux-resetting winding and a high-voltage feedback diode.

- The duty cycle can be set to be greater than 50%.

- The transformer core is utilized bi-directionally resulting in a more balanced flux excursion and a lower flux density.

- The peak voltage applied across Q_1 is $\frac{V_i}{1 - D}$. Since the duty cycle, D, is reduced at a high input voltage, the peak voltage applied on Q_1 can be less than twice V_i at a high line voltage.

The major drawback of the magnetizing-current mirror is the addition of a MOSFET switch and its drive circuit.

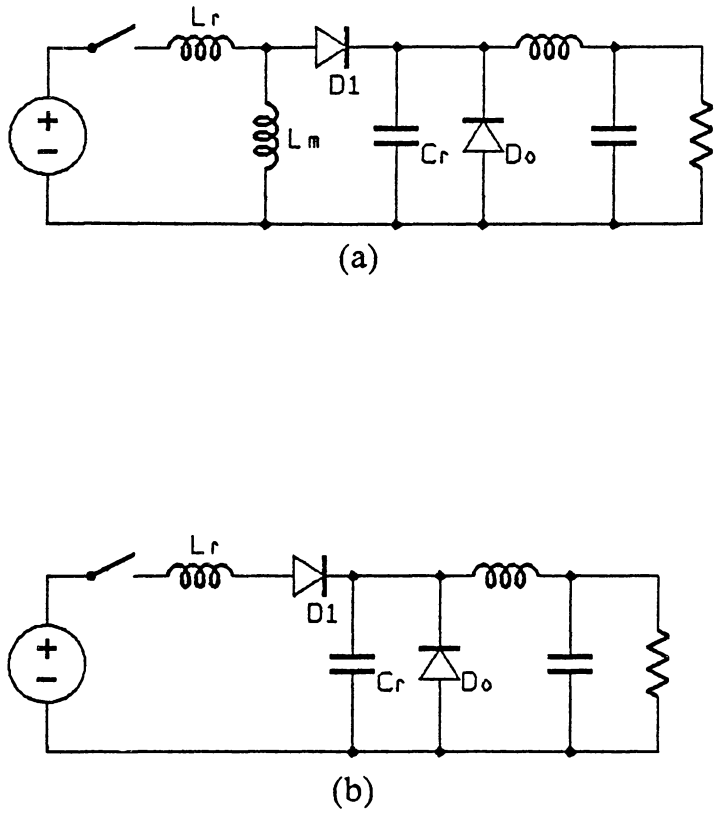
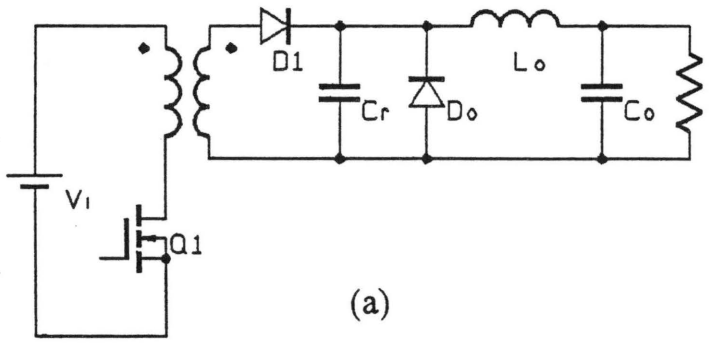
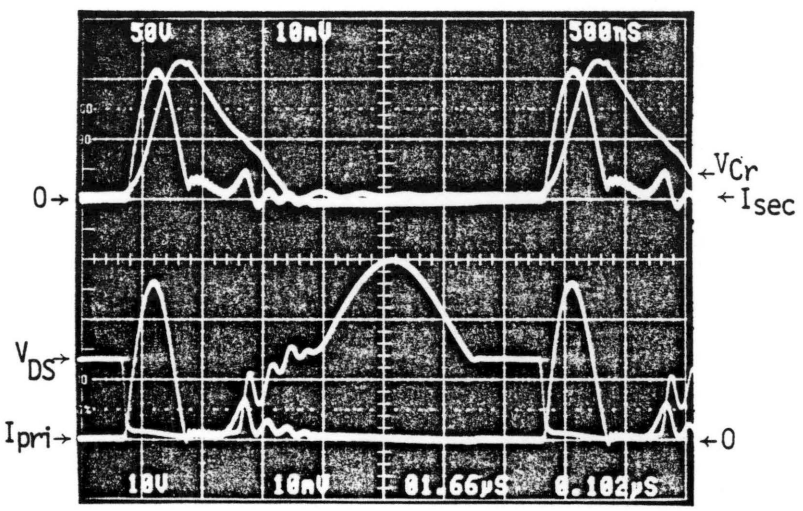


Fig. 5.12 (a) The equivalent circuit of the Vicor circuit
(b) A half-wave mode, quasi-resonant buck converter



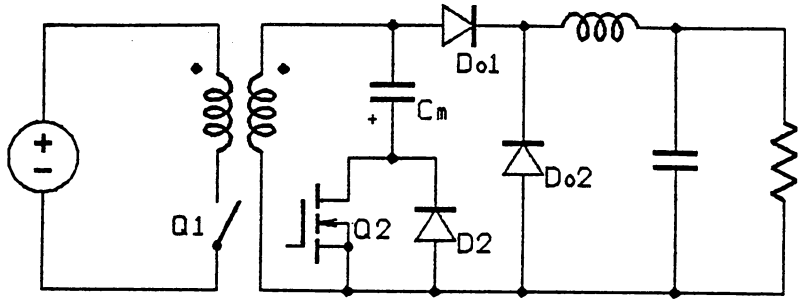
(a)

Q1: Toshiba 2SK324 (400V, 0.45Ω)
D1, Do: IR 31DQ06 (60V, 3A)
Lk: 1.2μH Cr: 0.11μF
Lo: 50.μH Co: 100.μF
Vi: 65V Vo: 4.07V
R: 1.3Ω

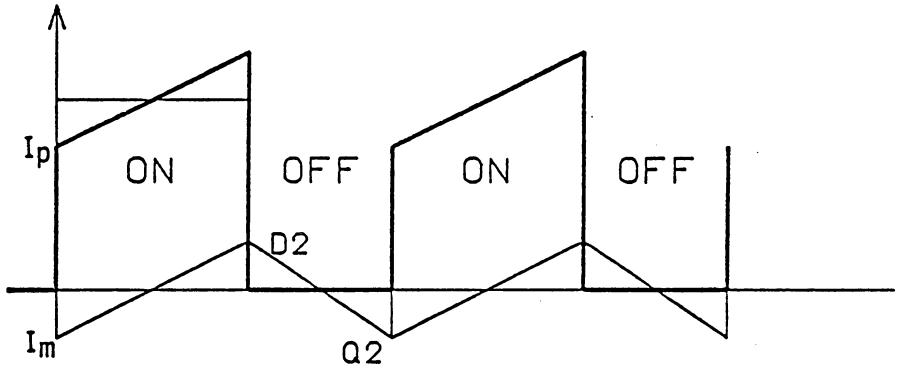


(b)

Fig. 5.13. (a) A Vicor circuit implemented
(b) Waveforms from the circuit:
Vcr (10V/div.) Isec (5A/div.)
Vds (50V/div.) Ipri (1A/div.)



(a)



(b)

Fig. 5.14 *(a) A typical magnetizing-current mirror circuit*
(b) The primary current waveform of the forward converter with a magnetizing-current mirror

5.2.3. Flyback Converter with Secondary-Side Resonance

The secondary-side resonance technique can also be applied to the flyback converter. Figure 5.15 shows the topological transformation from a ZCS, quasi-resonant flyback converter (Fig. 5.15a) to a flyback converter with secondary-side resonance (Fig. 5.15b).

When the transformer is replaced by a model consisting of a leakage inductance, L_k, and a magnetizing inductance, L_m, the circuit in Fig. 5.15b becomes a ZCS, quasi-resonant buck/boost converter, as shown in Fig. 5.15c.

The flux-resetting mechanism of this flyback converter with secondary-side resonance is similar to that of the conventional PWM flyback converter. At the on-time of Q_1, the voltage across capacitor C_r is charged to a positive value. After Q_1 turns off, the energy stored in C_r is discharged to the magnetizing inductance, increasing the magnitude of the magnetizing current. After the voltage across C_r is discharged to $-V_o$, the output diode, D_o, starts to conduct and clamps the voltage across C_r to $-V_o$. The magnetizing current, I_m, then releases the stored energy to the output. At the same time, the magnitude of I_m decreases.

Effectively, in the flyback converter or the quasi-resonant flyback converter, input energy is first transferred to and stored in the magnetizing inductance and then released to the output. The magnetizing current is set and reset alternately by the input voltage and the output voltage. Therefore, the flux-resetting mechanism is built in the flyback topologies.

Experimental Results

A 30W, 800kHz flyback converter with secondary-side resonance has been implemented [B8, B10]. The circuit diagram is shown in Fig. 5.16. Waveforms taken from the circuit at full load are shown in Fig. 5.17. Due to the the re-charging of the junction capacitance of the MOSFET switch through the leakage inductance of the transformer, there is an oscillatory voltage spike after the switch turns off. A snubber circuit is added across the primary winding of the transformer to damp this voltage spike.

This circuit can be modified to operate in the full-wave mode by connecting an external anti-parallel diode, D_2, across Q_1 and D_1. However, because of the reverse recovery of diode D_2, the voltage spike after switch Q_1 is turned off is further aggravated than in the case of half-wave mode.

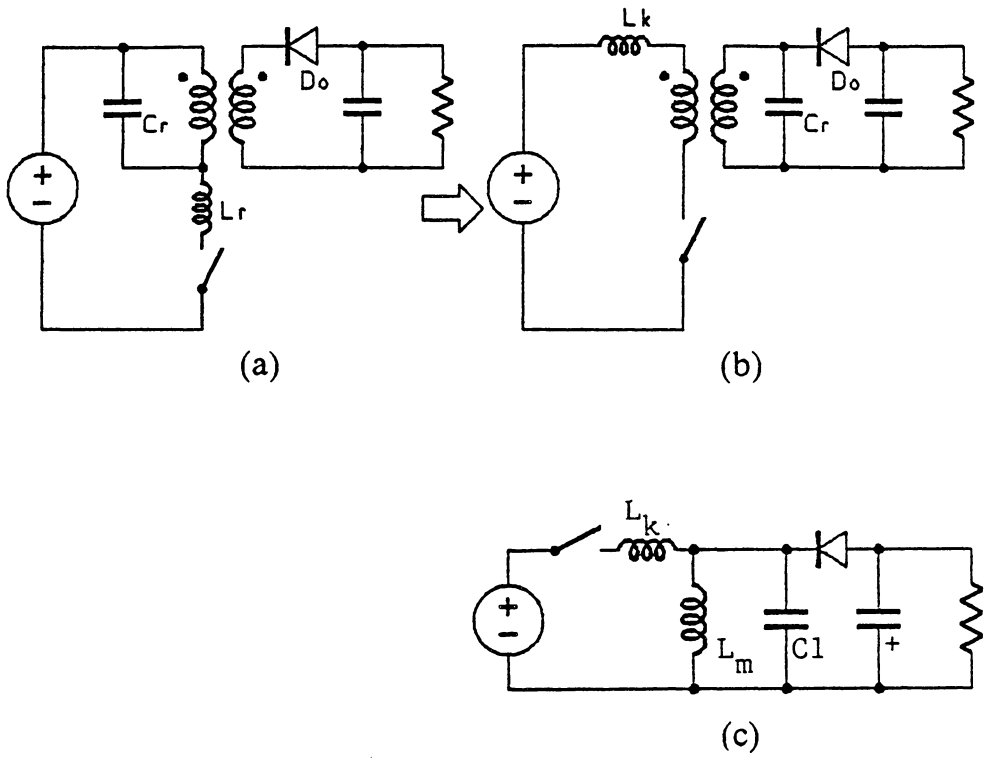


Fig. 5.15 *(a) The quasi-resonant flyback converter with an L-type resonant switch*
(b) The flyback converter with secondary-side resonance
(c) The quasi-resonant buck/boost converter

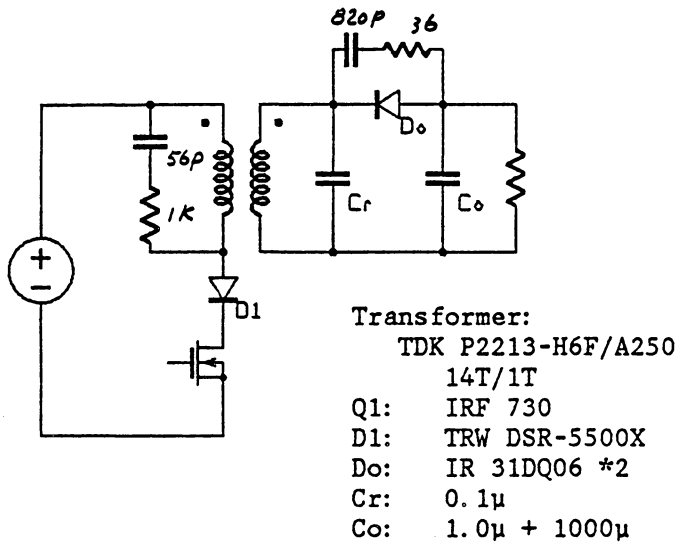
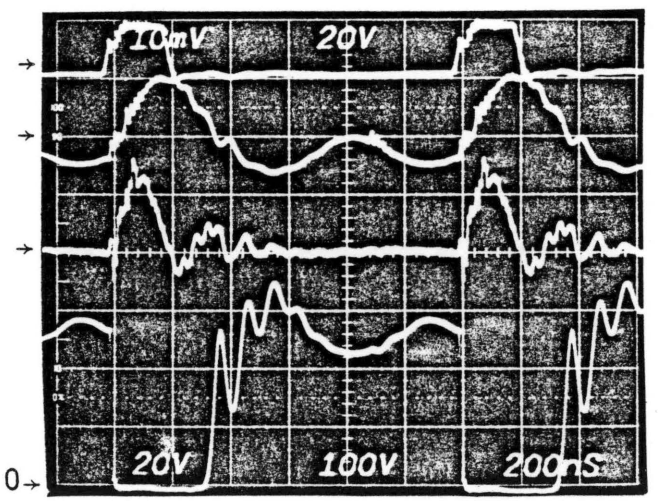


Fig. 5.16 A 800kHz, 30W flyback converter with secondary-side resonance



Vi = 150V, Vo = 4.95V, Io = 5.8A, fs = 813kHz,
1st waveform: Vgs (20V/div.) 2nd waveform: Vcr (20V/div.)
3rd waveform: Ip (2A/div.) 4th waveform: Vds (100V/div.)

Fig. 5.17 Waveforms from the circuit in Fig. 5.21 in half-wave mode of operation

5.3. Topological Links between Resonant and Quasi-Resonant Converters

A half-bridge, full-bridge, or push-pull converter can be viewed as two forward converters connected back-to-back and sharing the same output circuit. In a forward converter, the flux resetting is a major concern, and a certain type of flux-resetting mechanism needs to be implemented. There is no such requirement in a bridge converter, since the transformer is excited in both directions and the flux is reset naturally in each consecutive half-cycle.

Two versions of the half-bridge converters with secondary-side resonance can be derived from the forward converter with secondary-side resonance and the Vicor circuit.

5.3.1. Half-Bridge Converter with Secondary-Side Resonance (Full-Wave Circuit)

Figure 5.18a shows two forward converters with secondary-side resonance, connected back-to-back, sharing a common output circuit. By rearranging the circuit elements, the topology can be modified into the circuit shown in Fig. 5.18b. Further simplification can be made by merging the two resonant capacitors into a single resonant capacitor connected across the secondary wind-

ing, as shown in Fig. 5.18c. Notice that diode D_{o3} can be removed without affecting the circuit's operation since the free-wheeling output current can be carried by the simultaneous conduction of diodes D_{o1} and D_{o2}.

Incidentally, this circuit is actually a modified version of the conventional parallel resonant converter as described in Sec. 5.1.2. The resonant capacitor, C_r , is connected on the secondary side of the transformer in order to utilize the leakage inductance as the resonant inductor. Since this circuit is fully equivalent to the conventional parallel-resonant converter, there are many operational modes and control strategies available [D16, D18-D21, D26].

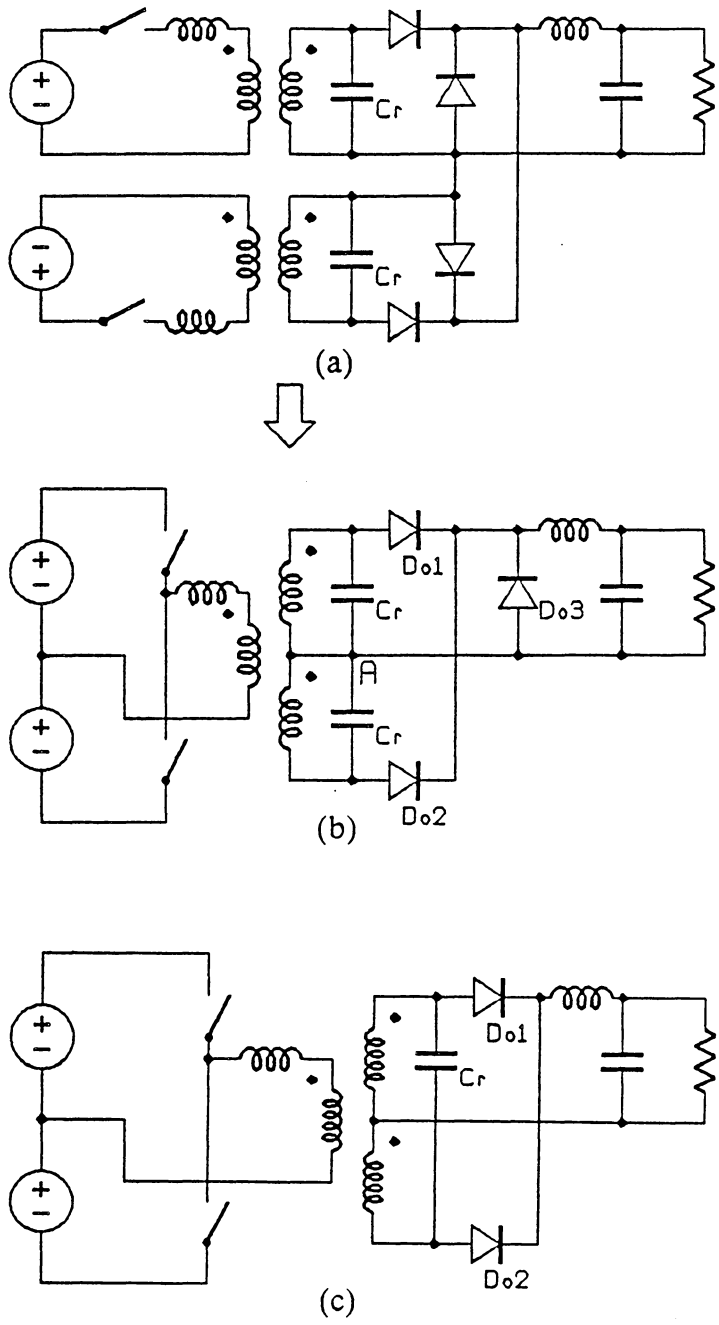


Fig. 5.18 *(a) Two forward converters with secondary-side resonance connected back-to-back*
(b) A PRC with two secondary-side resonant capacitors
(c) A PRC with a secondary-side resonant capacitor

5.3.2. Half-Bridge Converter with Secondary-Side Resonance (Half-Wave Circuit)

Two Vicor circuits can be connected back-to-back to form a half-bridge converter with secondary-side resonance. Figure 5.19 shows the topological transformation.[1] Notice the resonant capacitor is now connected on the right-hand side of diodes D_{o1} and D_{o2}. Also, diode D_{o3} can be removed without affecting the circuit's operation.

In this circuit, input power can only flow in the forward direction. No feedback of power is possible due to the blocking of diodes D_{o1} and D_{o2}. As a result, this circuit is confined to operate in the half-wave mode, and the output voltage is more sensitive to the load variation.

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[1] This circuit was proposed by Mr. Al Heyman of Digital Equipment Corporation.

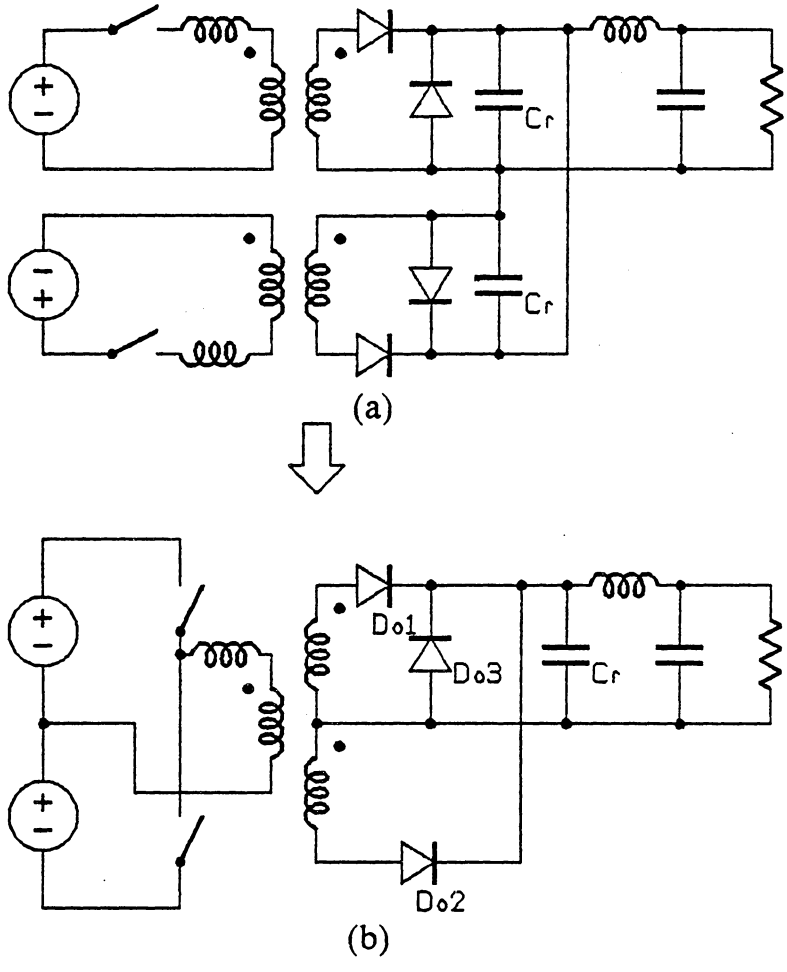

Fig. 5.19 (a) Two Vicor converters connected back-to-back
(b) A PRC with a resonant capacitor on the right-hand side of the rectifier diodes

5.3.3. A 300V-to-5V, 75W, 1.4MHz Parallel Resonant Converter with Secondary-Side Resonance

Full-Wave Mode of Operation

A high frequency, half-bridge PRC with secondary-side resonance has been designed and implemented. [2] This circuit operates from a 300Vdc input voltage and supplies a full-load current of 15A at 5V output. The switching frequency of each power switch is 700kHz at the full-load condition, giving an output ripple frequency of 1.4MHz. The circuit diagram and components used are shown in Fig. 5.20.

The switching frequency of this circuit is designed to operate below half of the natural frequency of the resonant tank; in other words, the resonant capacitor voltage always returns to zero before a switch is turned on. Consequently, the power switches are always switching at zero current. As be shown in Sec. 5.3, this circuit can be treated as two forward converters with secondary-side resonance connected in parallel. Therefore, when operated below half of the resonant frequency, this PRC has a voltage-conversion ratio which is twice as high as that of a ZCS, quasi-resonant buck converter.

The switching devices used are two SGS P365 MOSFETs. These devices are rated at 400V, 6A, with an on-resistance of 1.0Ω. Output junction capacitance of the device is about 150pF to 200pF.

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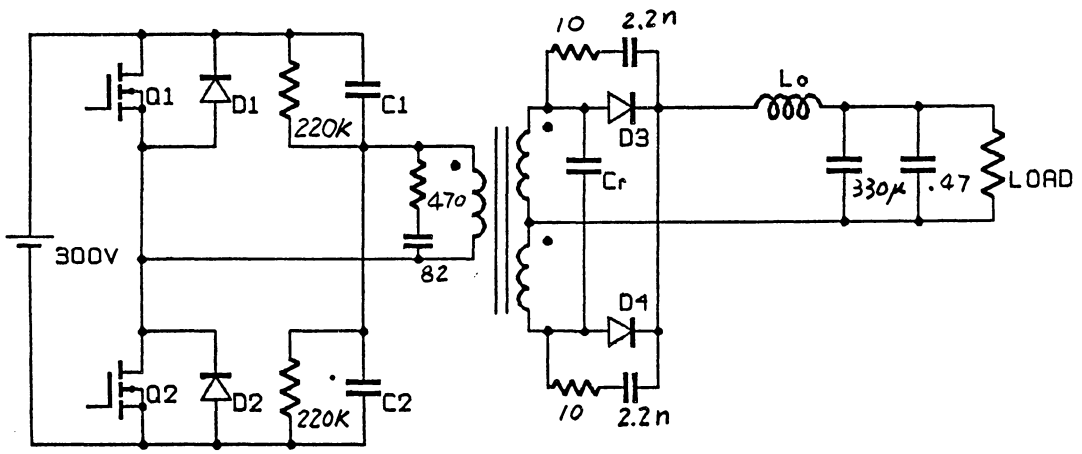
[2] The data on this circuit is prepared and provided by M. M. Jovanovic and D. C. Hopkins

The transformer design is very critical. To obtain a high power density, a low-profile LP H7C-44901 core from TDK is used. The primary winding uses two 24-turn wires in parallel, each consists of a Litz wire of 25 strands of AWG #42. The two secondary windings have two turns of copper foils each. The turn ratio is 24/2/2. Measured leakage-inductance and magnetizing inductance, both referred to the primary side, are 460μH and 4.25 μH, respectively.

Selected natural frequency of the resonant tank is 4MHz. The effective resonant inductance, L_r, which consists of the leakage inductance of the transformer and stray inductances, is about 6.0μH. The resonant capacitor, C_r, is selected at 0.033μF. The actual value of the natural frequency of the resonant tank is found to be about 4.3MHz, and the characteristic impedance, 162Ω.

Waveforms of the primary current of the transformer and the voltage across switch Q_2 are recorded under a full-load condition and a light load condition. Figure 5.21 shows the waveforms at 5.18V, 14A load condition. The switching frequency is 590kHz, measured efficiency of the power circuit is about 75.2%. Waveforms at a lighter load (5V, 2.5A) are shown in Fig. 5.22. Notice the larger reverse current during the conduction time during light load. Because of the slow reverse recovery of the internal body-drain diodes of the MOSFETs, there is considerable ringing both in the primary current and in the drain-source voltage waveforms during the off-time.



Transformer:
TDK LP-H7C 44901
24T/2T/2T

Cr: 0.033µF/200V
C1,C2: 0.1µF/200V
Lo: 5µH

Q1,Q2: SGS P365 (400V, 1.0Ω)
D3,D4: IR 28CP060 (60V, 25A)

Fig. 5.20 A 300V-to-5V, 75W, 1.4MHz PRC with secondary-side resonance (full-wave mode)

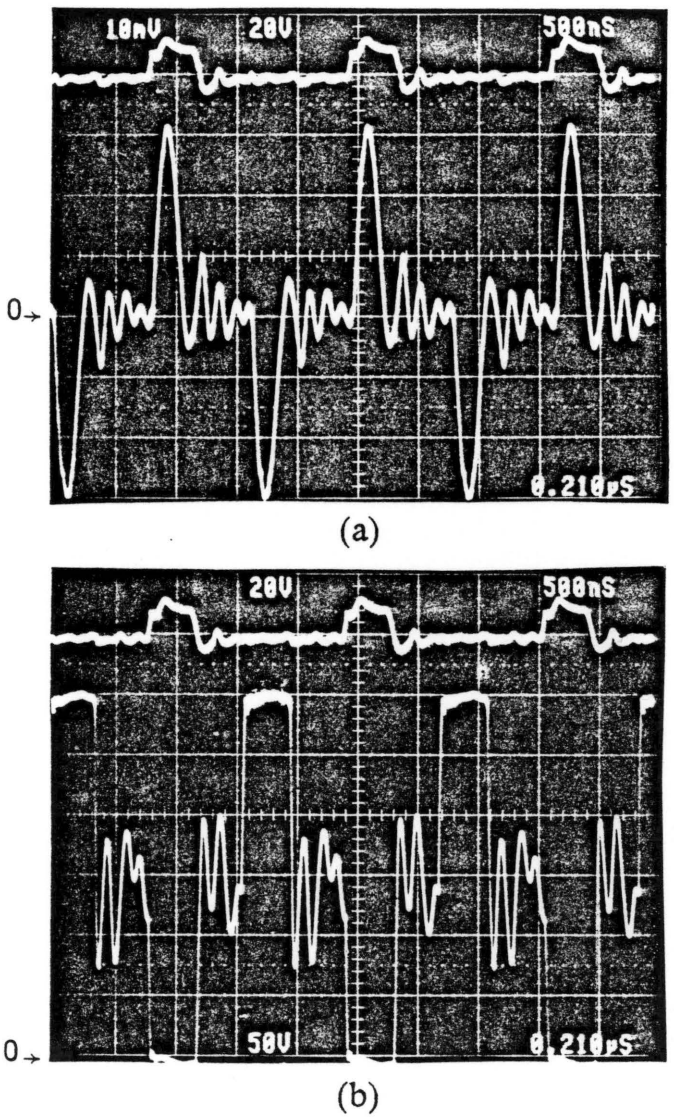


Fig. 5.21 Waveforms from circuit in Fig. 5.7.
Vo = 5V, Io = 14A, Ii = 0.31A, fs = 590kHz
(a) Vgs (20V/div.), Ip (1A/div.)
(b) Vgs (20V/div.), Vds (50V/div.)

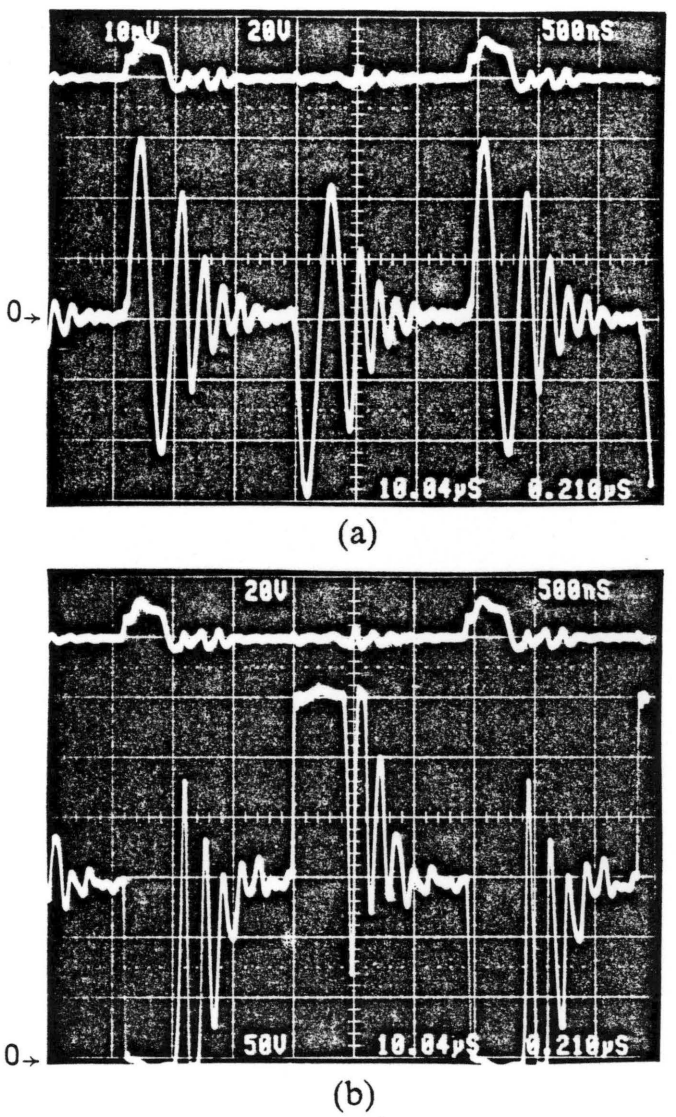


Fig. 5.22 Waveforms from circuit in Fig. 5.7.
Vo = 5V, Io = 2.5A, Ii = 0.1A, fs = 373kHz
(a) Vgs (20V/div.), Ip (1A/div.)
(b) Vgs (20V/div.), Vds (50V/div.)

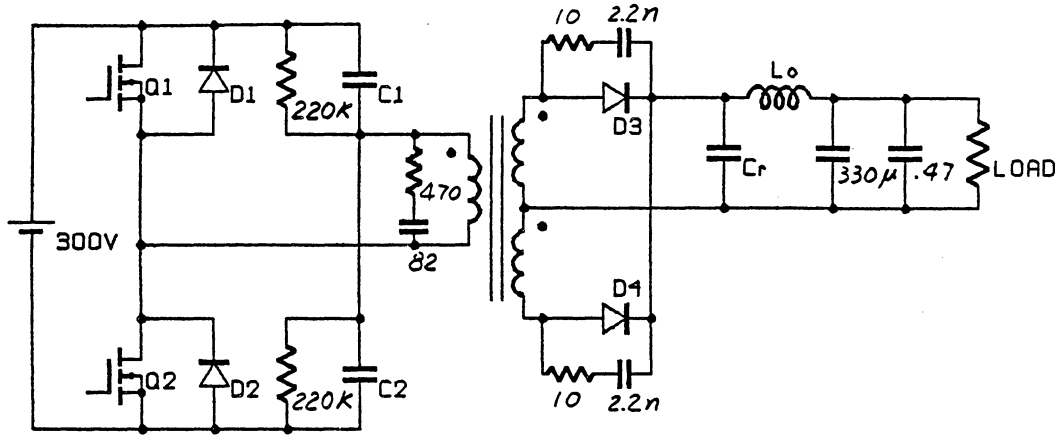
Half-Wave Mode of Operation

One way of reducing the ringing associated with the slow reverse recovery of the internal diodes of the MOSFETs is to operate the circuit in the half-wave mode of operation to avoid the reverse recovery problem associated with the diodes. There are two methods of modifying the circuit to operate in the half-wave mode : (A). adding a series diode to each primary switch, or (B). moving the resonant capacitor C_r to the right-hand side of the output rectifier. Method B (also see Sec. 5.3.2) is more favorable, since it requires no extra components. Figure 5.23 shows the circuit diagram after relocating the resonant capacitor.

Major waveforms of the PRC with secondary-side resonance operating in the half-wave mode and under full load are shown in Fig. 5.24. The switching frequency is 700kHz, with an output of 5.18V at 15.2A. Measured efficiency is 73.2%.

Compared to the full-wave mode of operation, the ringing during the time when both switches are off is much reduced. The drain-source voltage also settles down to the equilibrium value much faster. Waveforms at a light load condition are shown in Fig. 5.25.

A hybrid implementation of this circuit using thick-film technology to achieve high power density is currently under investigation. Preliminary results show power density as high as 25 W/in^3 has been achieved in a 1MHz, 80W, off-line converter [D30].



Transformer:
TDK LP-H7C 44901
24T/2T/2T

Cr:	0.033μF/200V	Q1,Q2:	SGS P365 (400V, 1.0Ω)
C1,C2:	0.1μF/200V	D3,D4:	IR 28CP060 (60V, 25A)
Lo:	5μH		

Fig. 5.23 A 300V-to-5V, 75W, 1.4MHz PRC with secondary-side resonance (half-wave mode)

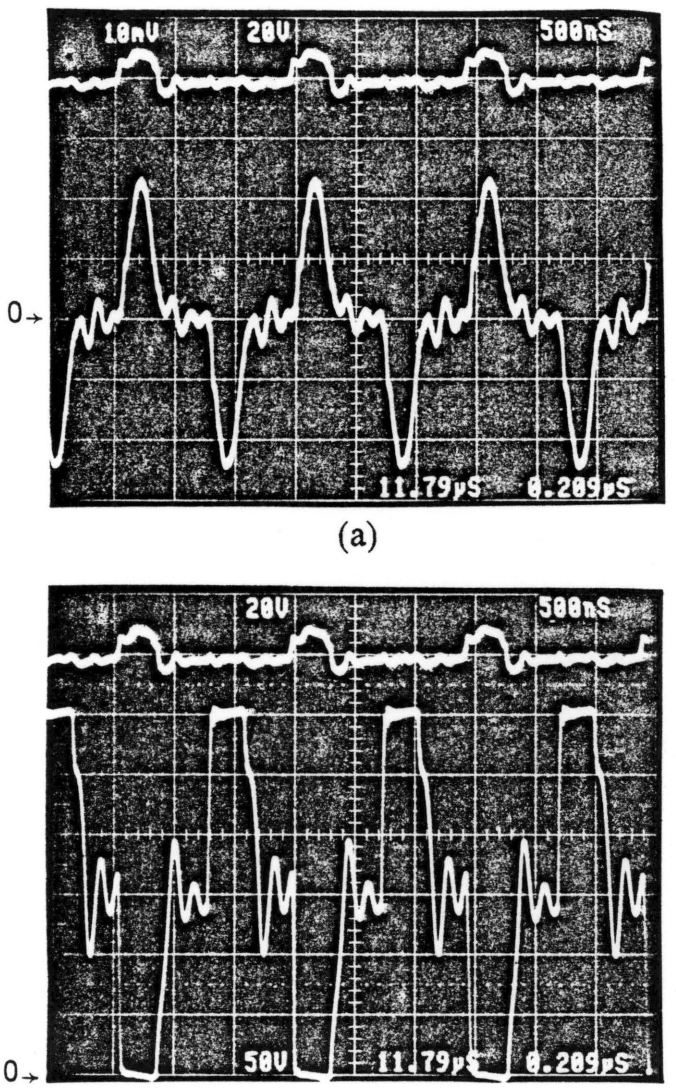
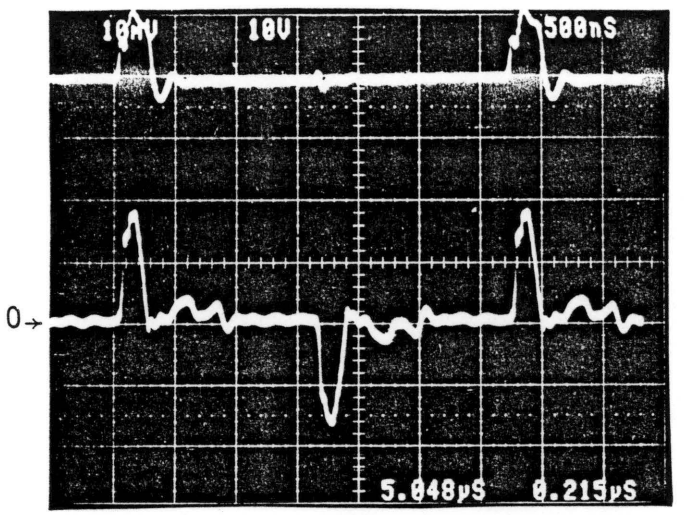
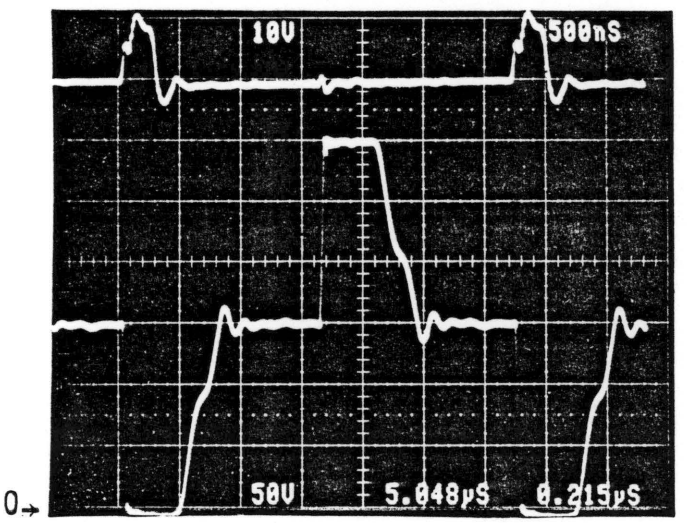


Fig. 5.24 Waveforms from circuit in Fig. 5.10.
Vo = 5.18V, Io = 15.2A, Ii = 0.36A, fs = 700kHz
(a) Vgs (20V/div.), Ip (1A/div.)
(b) Vgs (20V/div.), Vds (50V/div.)



(a)



(b)

Fig. 5.25 Waveforms from circuit in Fig. 5.10.
Vo = 5V, Io = 2.5A, Ii = 0.1A, fs = 308kHz
(a) Vgs (10V/div.), Ip (0.5A/div.)
(b) Vgs (10V/div.), Vds (50V/div.)

5.4. *Topological Refinements in ZVS, Quasi-Resonant Converters*

It has been shown in Chapter 3 that for a given ZVS, quasi-resonant converter, its voltage-conversion ratio is sensitive to load variation when operating in the half-wave mode and is insensitive to load variation when operating in the full-wave mode. Although the full-wave mode of operation is more desirable in terms of load insensitivity, it requires a diode connected in series with the semiconductor switch, since a BJT or a MOSFET device has no reverse-voltage blocking capability. As a result of adding a series diode, part of the energy stored in the parasitic junction capacitance of the semiconductor switch will be trapped and dissipated inside the switch after each switching cycle.

In high-frequency operations, the switching loss due to the parasitic junction capacitance becomes the dominant loss, therefore, it is less efficient to operate a ZVS, quasi-resonant converter in the full-wave mode of operation. Nevertheless, the parasitic junction capacitance can still be utilized as a part of the resonant capacitor required in a ZVS, quasi-resonant converter operating in the half-wave mode. Furthermore, the intrinsic drain-source diode of the MOSFET device can be used as the feedback diode required in the half-wave mode of operation.

When the parasitic junction capacitance is utilized to form part of the resonant capacitance in a ZVS, quasi-resonant converter, the switching loss due to the

capacitive turn-on is avoided, and the current spike and noise problems associated with the switching Miller effect are also eliminated.

As described in Sec. 3.4, for the isolated versions of ZVS, quasi-resonant converters, the leakage inductance of the transformer can also be utilized as a resonant element in a similar way as in the secondary-side resonance technique. For example, in Figs. 3.6e-3.6f, the configurations in the right column are the topologies where both the junction capacitance of the semiconductor switch and the leakage inductance of the transformer can be utilized as part of the resonant tank circuit.

5.4.1. A ZVS, Quasi-Resonant Flyback Converter

Among all ZVS, quasi-resonant converters, the simplest circuit is the flyback converter with an M-type, voltage-mode resonant switch as shown in the right-column circuit of Fig. 3.6e. When the leakage inductance of the transformer is used as the resonant inductor, and the junction capacitance of the semiconductor power switch is used as the resonant capacitor, this circuit contains the same number of components as a conventional flyback converter. A 5MHz, 25W, 50V to 5V breadboard circuit based on this topology has been implemented [C15]. The circuit's schematic diagram is shown in Fig. 5.26. Since in ZVS, quasi-resonant converters, the switch's current waveform has a flat top during the on-time, it allows the use of a MOSFET with a relatively low current rating.

Assume 80 percent efficiency and 50 percent equivalent duty cycle. At 25W, the peak value of the switch current is 1.25A when the input voltage is 50V. A small device, IRF-720, is chosen. Despite its high on-state resistance (1.8Ω), the conduction loss is still low.

For the transformer, a TDK P2213-H6F/A250 pot-core is used with 8 turns on the primary winding and one turn on the secondary winding. The secondary winding is made of a copper foil, 0.5mm thick and 1.0mm wide. The measured leakage inductance, referring to the primary-side, is about 1.1μH. Taking the stray inductances into account, the total value of L_r is estimated to be about 1.4μH. The output junction capacitance of IRF-720 is about 100pF when measured at 100V and above. A trimmer capacitor of 82pF is added to give C_r a total value of 180pF. The characteristic impedance and resonant frequency are calculated to be 88.2Ω, and 10.03MHz, respectively.

The waveforms of the circuit operating at 5MHz and under three load conditions are recorded, as shown in Fig. 5.27. Notice the clean and smooth waveforms in the zero-voltage switching conditions, as shown in Fig. 5.27a and 5.27b. When the load current is too low, as in the case of Fig. 5.27c, the drain-source voltage will not be able to oscillate to zero. The turn-on at a non-zero voltage condition causes noticeable switching ringing due to the Miller effect, as can be seen in the gate-source voltage waveform. Table 5.1 summarizes the important circuit parameters measured.

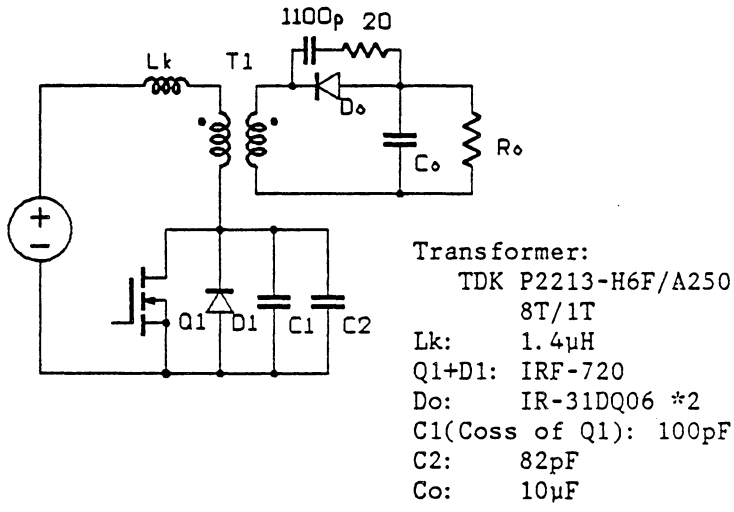
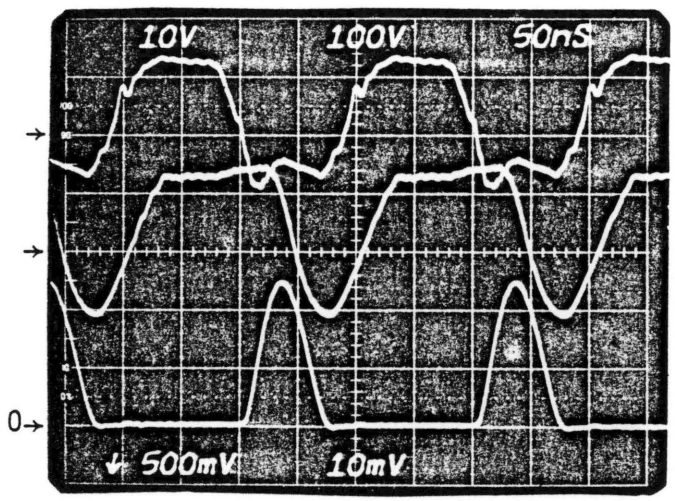
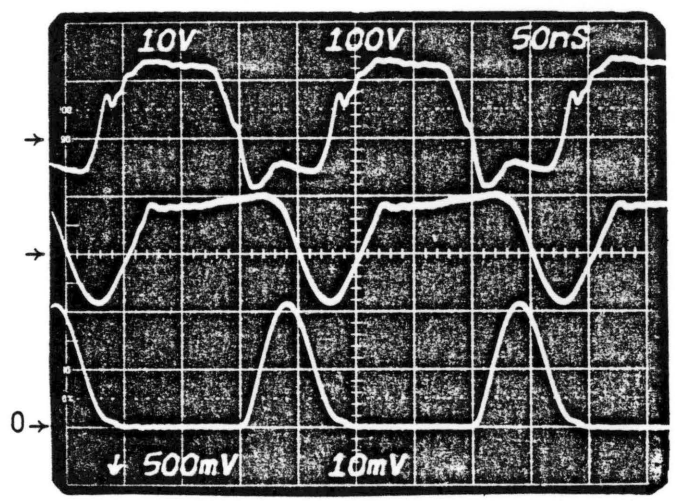


Fig. 5.26 A 5MHz, 25W, ZVS, quasi-resonant flyback converter

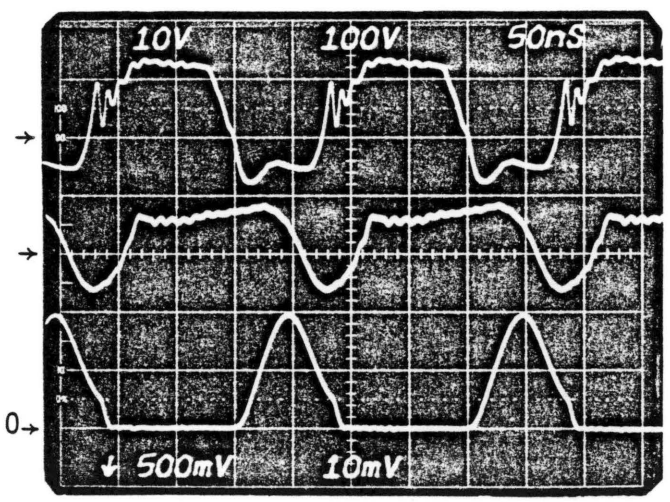


(a)



(b)

Fig. 5.27 Waveforms from circuit in Fig. 5.25.
upper: Vgs(20V/div.) middle: Ip(1A/div.) lower: Vds(100V/div.)
(a) Vi = 50V, Vo = 5.0V, Io = 4.9A
(b) Vi = 50V, Vo = 6.3V, Io = 2.9A



(c)

Fig. 5.27 (cont.)
upper: Vgs(20V/div.) middle: Ip(1A/div.) lower: Vds(100V/div.)
(c) Vi = 50V, Vo = 7.5V, Io = 1.8A

Table 5.1. Measured circuit parameters from the circuit in Fig. 5.26 under different load conditions

	Case I	Case II	Case III
Ro (nominal)	1.0 Ω	2.0 Ω	4.0 Ω
Vi	50 V	50 V	50 V
Ii	0.59 A	0.43 A	0.3 A
Pi	29.5 W	21.5 W	15 W
Vo	5.0 V	6.3 V	7.5 V
Io	4.9 A	2.9 A	1.8 A
Po	24.5 W	18.3 W	13.5 W
efficiency	83	85	90

5.4.2. A ZVS, Quasi-Resonant Half-Bridge Converter

Although the ZVS, quasi-resonant converters have a great potential to operate in very high frequencies, they have a common difficulty in becoming a widely used technology, namely, their higher voltage stress on the switching devices. As described in Chapter 3, the peak off-state voltage is usually four to five times the input voltage. For off-line switching power supply applications, they require switching devices with voltage rating of 1200V to 1500V. So far, the MOSFET devices commercially available with the highest voltage rating are 1000V devices. Furthermore, the on-state resistances of these high-voltage MOSFETs are significantly larger than those of 500V devices.

To overcome the problems associated with the high voltage stress on switching devices in single-ended, ZVS, quasi-resonant converters, an alternative which naturally emerges is to configure the converters in half-bridge or full-bridge circuits. Although the circuit simplicity of single-ended converters is sacrificed, the peak voltage stress on switching devices can be limited to no more than the input voltage in the bridge configurations.

In the past, the idea of operating a PRC or an SRC at switching frequencies higher than the resonant frequency to achieve the zero-voltage switching effect has been proposed and investigated [D14, D16, D18, D19, D26]. While this idea is not new, the application of this technique is still somewhat limited.

An earlier study by the author investigated other possible bridge configurations that can achieve the zero-voltage switching effect. It was found that a con-

ventional voltage-fed, half-bridge (or full-bridge) converter can also be operated in certain load ranges and achieve the zero-voltage switching effect. Although this circuit is still preliminary and has a voltage-conversion ratio which is very sensitive to the load variation, it has a very simple circuit topology and maintains an optimal current waveform. The discussion on this circuit is to present some insight into the zero-voltage switching technique, and to serve as a basis for future circuit modifications and improvements.

A conventional voltage-fed, half-bridge converter is shown in Fig. 5.28. Each of the two MOSFET switches comprises an enhanced forward channel (Q_1 , Q_2), a body-drain diode (D_1 , D_2), and an output junction capacitance (C_1 , C_2). The leakage inductances of the transformer is lumped into a single primary leakage inductance, L_k .

Assuming a switching cycle starts when switch Q_1 is carrying the primary current (see Fig. 5.29a). If the output inductor, L_o , is sufficiently large as is expected in normal operation, the output current is constant and flowing through diode D_{o1} initially. After Q_1 turns off, the inductive primary current is diverted into capacitor C_1. The voltage across C_1, V_{C1} , rises linearly until it reaches half of the line voltage, $0.5V_{CC}$ ($V_1 = V_2 = V_i = 0.5V_{CC}$) . The equivalent circuit during this stage is shown in Fig. 5.29b. Notice that, capacitors C_1 and C_2 are connected in series across the line voltage, V_{CC} . Therefore, the sum of V_{C1} and V_{C2} are always V_{CC} .

After V_{C1} reaches V_i , the load current flows through both secondary windings. Both output-rectifier diodes D_{o1} and D_{o2} are on, each conducts one half of the

load current. To the primary-side circuit, the secondary-side circuit appears as a short circuit. Only the leakage inductance of the transformer is seen by the primary circuit. The equivalent circuit of the converter during this free-wheeling stage is shown in Fig. 5.29c.

If the load current is large enough, the inductive current through L_k will completely charge V_{C1} to $2V_i$ and discharges V_{C2} to 0. The residual inductive current then will be carried by diode D_2. The equivalent circuit during this stage is shown in Fig. 5.29d. At the same time, with diode D_2 carrying the reverse current, Q_2 can be turned on under a zero-voltage condition.

After the energy stored in the leakage inductance is exhausted, L_k is forward biased by voltage V_2. Its current rises linearly. The equivalent circuit is shown in Fig. 5.29e. Finally, the current through L_k reaches the level of the load current, I_o , and diode D_{o1} turns off, leaving diode D_{o2} carrying the entire load current. The equivalent circuit in this final stage of the first half of a switching cycle is shown in Fig. 5.29f.

The second half of a switching cycle undergoes a similar sequence of stages. Figure 5.30 illustrates the major waveforms of the circuit during a complete switching cycle.

Detailed analysis of the circuit's steady-state operation is described in Table 5.2. The dc voltage-conversion ratio according to the results derived in Table 5.2 is plotted in Fig. 5.31 as a function of the switching frequency with the normalized load resistance, r ($= \frac{R_{\text{Load}}}{Z_n}$), as the controlling parameter.

Figures 5.32 and 5.33 show the waveforms taken from an experimental circuit operating from a 250V line voltage. The waveforms are shown to be in good agreement with the predicted waveforms (see Fig. 5.30) according to the circuit analysis described above. Also, the waveforms are very clean, free of the switching Miller effect and related noise. Each switch has an optimal current waveform (lowest rms value), resulting in a minimum of conduction loss. Figure 5.33a shows the waveforms at 250V input, 3V, 13A output. Notice the smooth drain-source waveform of the MOSFET. The I_{ds} waveform actually includes current through Q_2, D_2, and C_2. Figure 5.33b shows the waveforms at 250V input, 5.9V, 0.6A output.

This circuit demonstrates that, by properly utilize the two predominant parasitic elements in the circuit, i.e., the leakage inductances of the transformer and the junction capacitances of the power switches, a zero-voltage switching property can be achieved resulting in many desirable benefits.

However, as can be seen from the dc voltage-conversion ratio curves shown in Fig. 5.31, there are two major deficiencies in this converter: (1) The voltage-conversion ratio is very sensitive to load variation. (2) The voltage-conversion ratio is not sensitive to variation in the switching frequency. In a closed-loop converter implementation, these two features force the converter to vary the switching frequency over a wide range in order to regulate the output voltage against the load and line variations.

As described earlier, this circuit is presented only as a basis for better understanding of the zero-voltage switching technique. Future study on modifications

on this circuit to improve its voltage-conversion ratio characteristics is recommended.

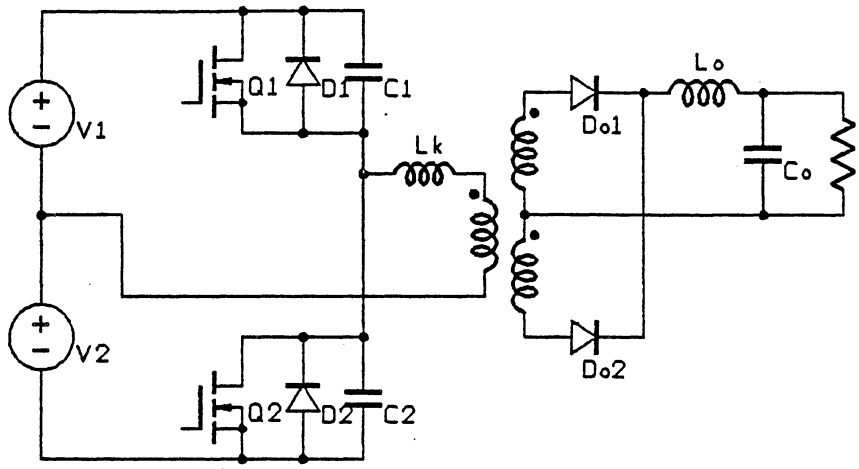


Fig. 5.28 A voltage-fed, half-bridge converter operating in the zero-voltage switching mode

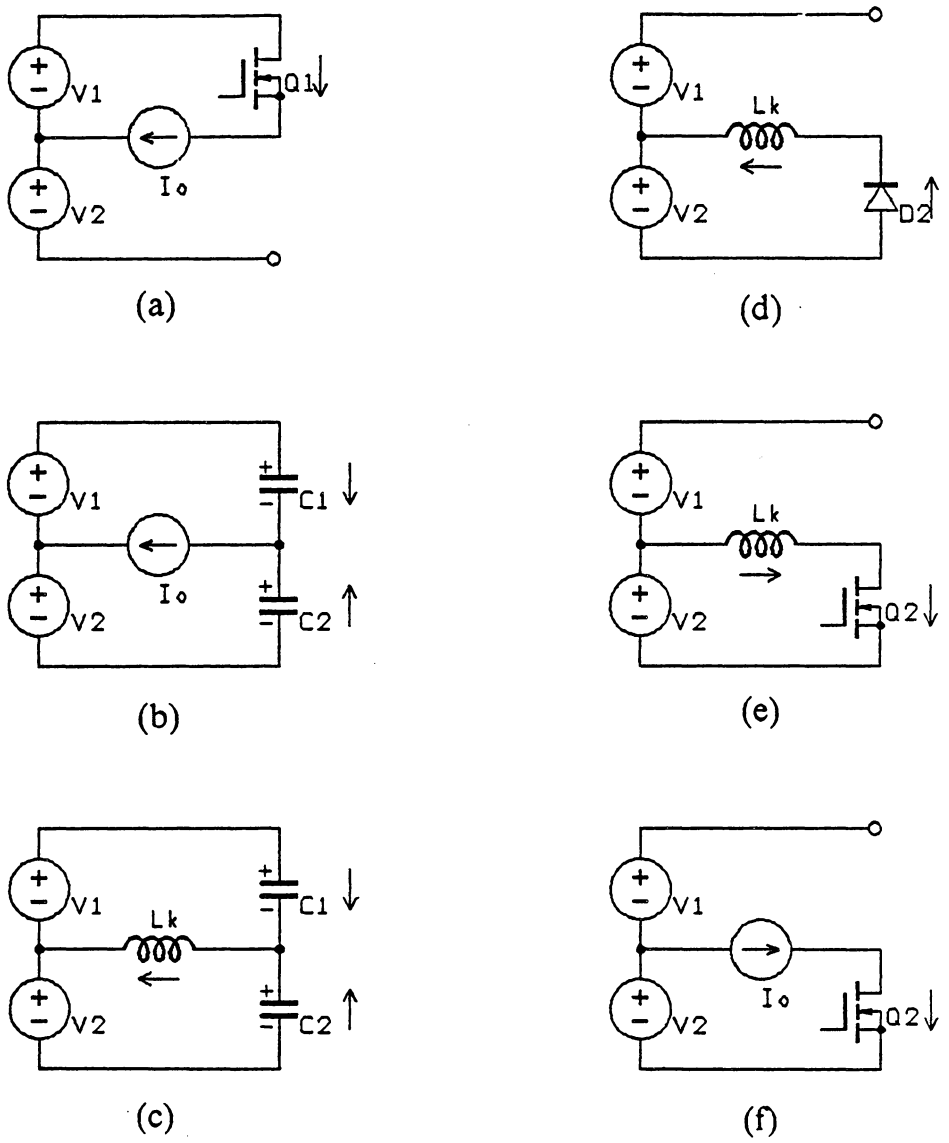


Fig. 5.29 The equivalent circuits of the half-bridge converter in the various stages in a switching cycle

(a) Q1 conducting constant current (d) D2 clamping, Q2 turns on

(b) Q1 turns off, Vc1 rises linearly (e) Im rises linearly

(c) resonant stage (f) Q2 conducting constant current

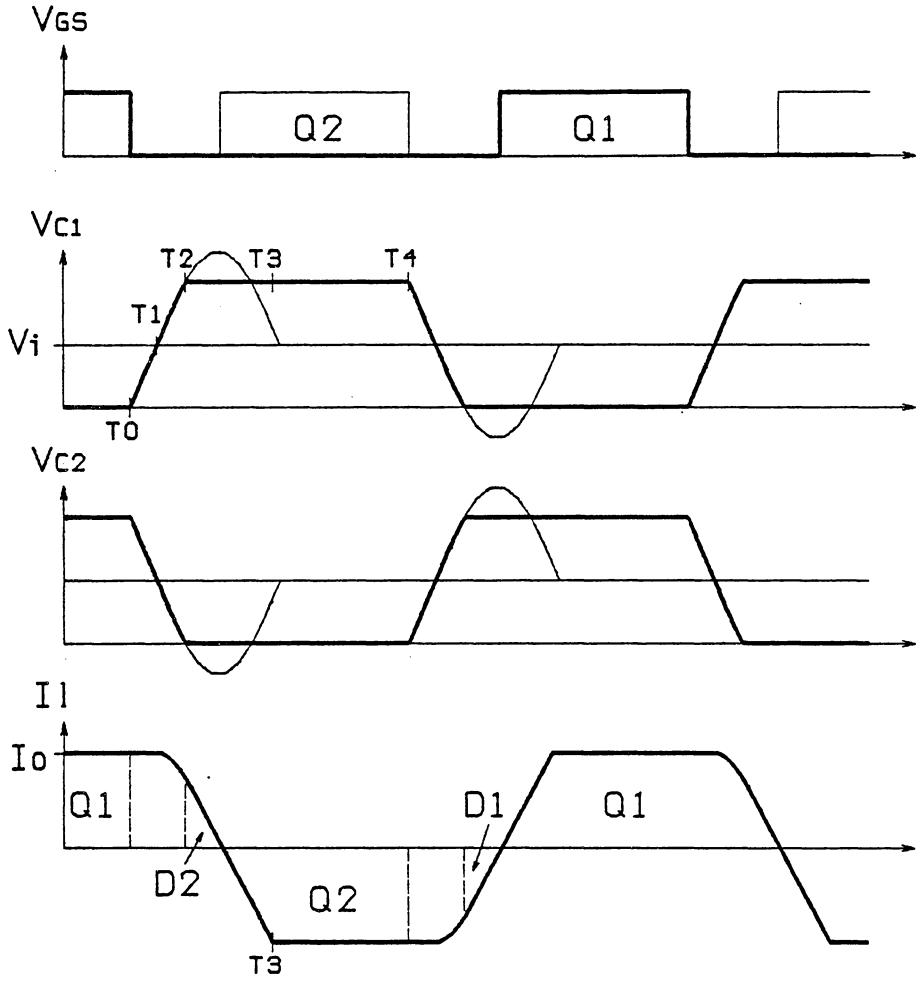


Fig. 5.30. Waveforms of the ZVS, half-bridge converter in a switching cycle

Table 5.2. ZVS, Half-Bridge Converter

Capacitor-Charging Stage [T0, T1] : Q_1 turns off at T_0 .

Initial Condition:

$$V_{C1}(0) = 0\ ;\quad V_{C2}(0) = 2V_i \tag{1a}$$

State Equation:

$$C\frac{dV_{C1}}{dt} = \frac{I_o}{2}\ ;\quad -C\frac{dV_{C2}}{dt} = \frac{I_o}{2} \tag{1b}$$

Time Solution:

$$T_{01} = \frac{2C\,V_i}{I_o} = \frac{1}{\omega}\frac{r}{x}\ ,\ \text{where}\ r \equiv \frac{R}{Z_n}\ ,\ x \equiv \frac{V_o}{V_i} \tag{1c}$$

Resonant Stage [T1, T2] : V_{C1} reaches V_i at T_1 , both D_{O1} and D_{O2} are on.

Initial Conditions:

$$I_L(0) = I_o\ ;\quad V_{C1}(0) = V_{C2}(0) = V_i \tag{2a}$$

State Equations:

$$L\frac{dI_L}{dt} = V_i - V_{C1}\ ;\quad C\frac{dV_{C1}}{dt} = \frac{I_L}{2} \tag{2b}$$

Time Solutions:

$$I_L(t) = I_o \cos \omega t \tag{2c}$$

$$V_{C1}(t) = V_i + Z_n I_o \sin \omega t \tag{2d}$$

$$T_{12} = \frac{\alpha}{\omega}\ ,\ \text{where}\ \alpha = \sin^{-1}\left(\frac{-V_i}{Z_n I_o}\right) = \sin^{-1}\left(\frac{-r}{x}\right) \tag{2e}$$

Inductor-Charging Stage [T2, T3] : V_{C2} drops to zero at T_2 , D_2 conducts, Q_2 turns on.

Initial Condition:

$$I_L(0) = I_o \cos \alpha \tag{3a}$$

State Equation:

$$L\frac{dI_L}{dt} = -V_i \tag{3b}$$

Time Solution:

$$T_{23} = \frac{L\,I_o(1 + \cos \alpha)}{V_i} = \frac{1}{\omega}\frac{x}{r}(1 + \cos \alpha) \tag{3c}$$

Constant-Current Stage [T3, T4] : I_L reaches $-I_o$ at T_3 , D_{O2} cuts off.

$$T_{34} = T_s - T_{01} - T_{12} - T_{23} \tag{4}$$

Table 5.2. (cont.)

Input power per half-cycle, Ei :

$$E_i = V_i \int_{T_0}^{T_4} I_L \, dt$$

$$= V_i I_o T_{01} + V_i \int_{T_1}^{T_2} I_L \, dt + V_i \int_{T_2}^{T_3} I_L \, dt + V_i I_o T_{34}$$

$$= V_i I_o (T_s - T_{12} - T_{23}) + V_i \int_{T_1}^{T_2} I_L \, dt + V_i \int_{T_2}^{T_3} I_L \, dt \qquad (5)$$

From Eq. (2c), (2d) and (2e),

$$\int_{T_1}^{T_2} I_L \, dt = \int_{T_1}^{T_2} I_o \cos \omega t \, dt = \frac{I_o}{\omega} \sin \alpha = \frac{I_o}{\omega} \left(- \frac{r}{x} \right) \qquad (6)$$

From Eq. (3c),

$$\int_{T_2}^{T_3} I_L \, dt = \frac{(I_o - I_o \cos \alpha)}{2} T_{23} = I_o \frac{(1 - \cos \alpha)}{2} \frac{1}{\omega} \frac{x}{r} (1 + \cos \alpha)$$

$$= \frac{I_o}{2\omega} \frac{x}{r} \sin^2 \alpha = \frac{I_o}{2\omega} \frac{r}{x} \qquad (7)$$

Therefore,

$$E_i = V_i I_o \left(T_s - \frac{\alpha}{\omega} - \frac{1}{\omega} \frac{x}{r} (1 + \cos \alpha) \right) + V_i \frac{I_o}{\omega} \left(+ \frac{r}{x} \right) + V_i \frac{I_o}{2\omega} \left(\frac{r}{x} \right)$$

$$= V_i I_o T_s \left[1 - \frac{f_s}{2\pi f_n} \left(\alpha - \frac{3r}{2x} + \frac{x}{r} (1 + \cos \alpha) \right) \right] \qquad (8)$$

Output power per cycle, Eo :

$$E_o = V_o I_o T_s \qquad (9)$$

By equating E_i and E_o,

$$\frac{V_o}{V_i} \equiv x = 1 - \frac{f_s}{2\pi f_n} \left[\alpha - \frac{3r}{2x} + \frac{x}{r} (1 + \cos \alpha) \right] \qquad (10)$$

where $0 < \alpha < \frac{\pi}{2}$

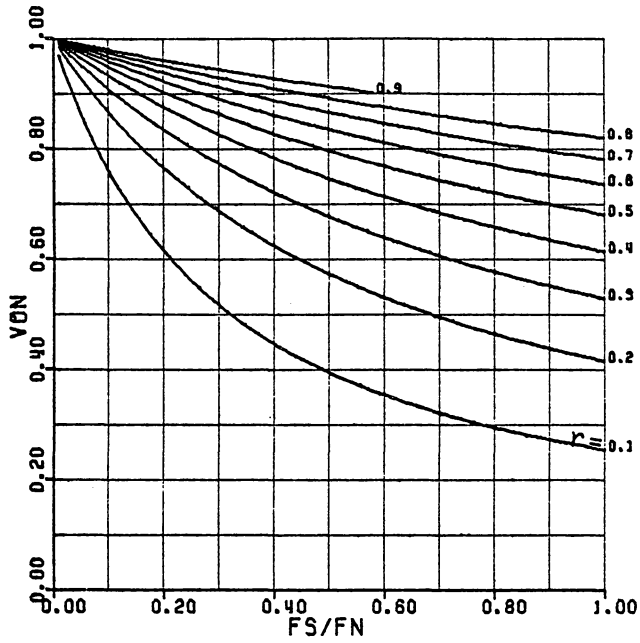


Fig. 5.31 DC voltage-conversion ratio of the ZVS, half-bridge converter

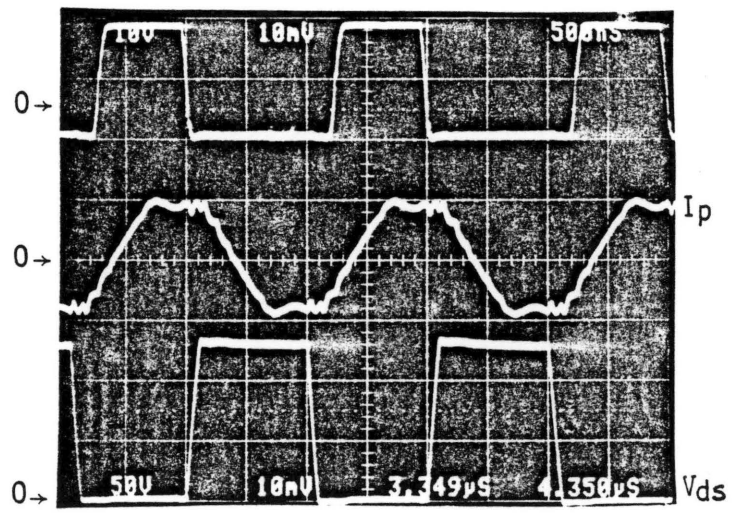


Fig. 5.32 Waveforms from the ZVS, half-bridge converter
upper: Vgs(10V/div.) middle: Ip(0.5A/div.) lower: Vds(50V/div.)
Vi = 130V, Vo = 1.26V, Io = 3.2A, fs=500kHz

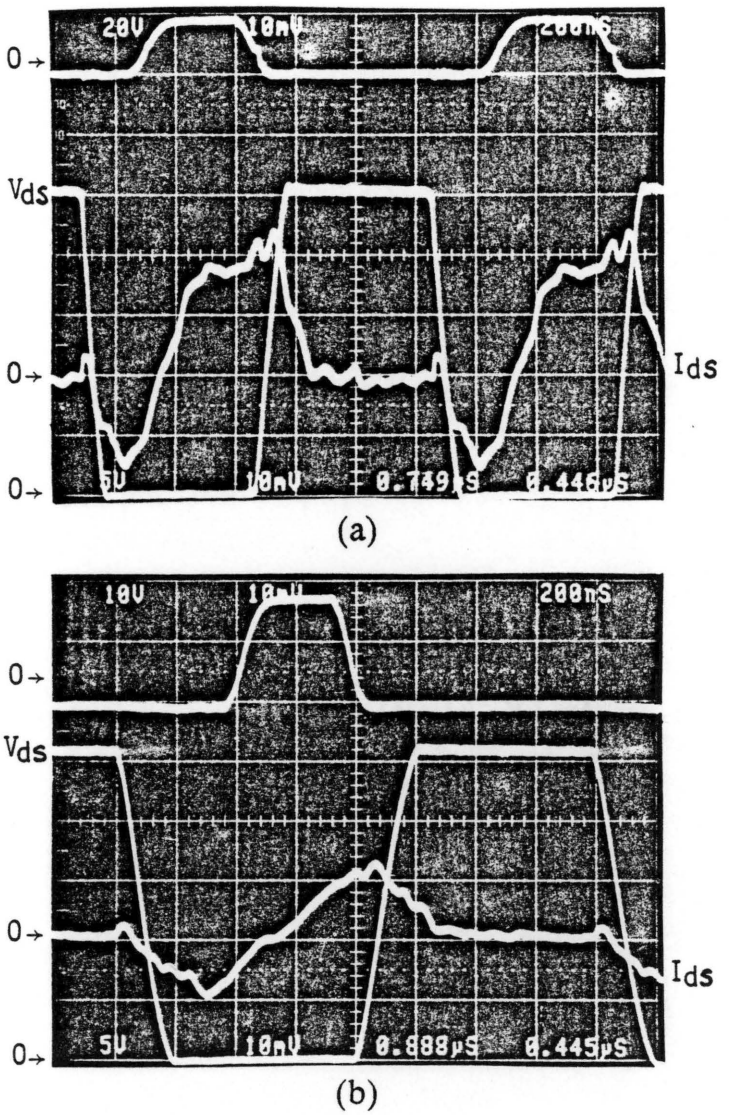


Fig. 5.33 Waveforms from the ZVS, half-bridge converter
upper: Vgs(10V/div.) middle: Ids(0.5A/div.) lower: Vds(50V/div.)
(a) Vi = 250V, Vo = 3.01V, Io = 13.5A, fs = 833kHz
(b) Vi = 250V, Vo = 5.94V, Io = 0.6A, fs = 625kHz

6. CONCLUSIONS

Switching-Mode Power Supply (SMPS) technology has made vast progress in the last two decades. As a result of better devices and components, better understanding of the topology and behavior of power converter circuits, significant improvements can be found in every facet of the SMPS: reduction in weight and size, improvement in efficiency, reliability and stability, and increase in the dynamic response, among others.

Still, when compared to the signal and data processing electronic circuits these SMPS's are supporting, the reduction in size and weight of SMPS's appears far less dramatic. With the advent of Very Large-Scale Integrated Circuits (VLSI) and High-Speed Integrated Circuits, there will be an even stronger demand for SMPS's with very high power density and very fast dynamic response.

One unique feature of the SMPS is that it is designed to process a large amount of power efficiently. To achieve the functions of power conversion, dc isolation, ripple-filtering, and noise suppression without sacrificing efficiency, a

SMPS circuit must rely on the extensive use of magnetic and capacitive components. Consequently, it is reasonable to conclude that the most effective way to increase the power density is to reduce the size of magnetic and capacitive components by designing the SMPS to operate at very high frequencies.

However, in the attempt to increase the operating frequency, we encounter two major difficulties: high switching stresses and high switching losses. The source of these difficulties is due to switching at high speeds in the harsh environment of a SMPS circuit where the power switching devices are often turned on under a capacitive load condition and turned off under a inductive load condition. These switching stresses and losses place a heavy burden on the power semiconductor devices.

Each type of power semiconductor device has its unique capabilities and limitations. The minority-carrier devices have higher power-handling capability but are generally limited in the turn-off capability and switching speed. Therefore, they are suitable for higher power, lower switching-frequency applications. The majority-carrier devices, on the other hand, have much higher switching speed but are limited in their power handling capability and are more suitable for lower power, high switching-frequency applications.

To improve the performance of SMPS circuits, different circuit strategies are needed for best utilization of semiconductor switching devices. For the minority-carrier devices operating at higher power-levels, the major concern is their inferior turn-off performance; whereas, for the majority-carrier devices in high-frequency

applications, the major difficulty is the switching loss associated with the capacitive turn-on.

In recent years, many efforts have been made in search for topological improvements in SMPS circuits. Particularly, the resonant converter technology and the zero-current switching technique have made great impacts. In this work, the research is expanded further, and it is found that the zero-current switching technique is a general technique which can be applied not only to the conventional resonant converters but, also, to virtually any PWM converter topology. Based on the concept of current-mode resonant switches, a large family of current-mode, quasi-resonant converters operating in the zero-current switching scheme have been discovered. This new family of converters can be viewed as hybrids between PWM converters and conventional resonant converters. They utilize the principle of inductive or capacitive energy storage and transfer in a similar fashion as PWM converters. However, an LC tank circuit is always present near the power switch and is used not only to shape the current and voltage waveforms but, also, to store and transfer energy from input to output in a manner similar to the conventional resonant converters.

For high power, high input voltage, and switching frequency up to 1MHz range, this zero-current switching technique is very effective, since it can eliminate the switching stresses and the turn-off switching loss. Employing the zero-current switching technique, 1MHz, 80W, off-line converter has been implemented by colleagues of the author, which achieves a power density of 25 W/in^3.

To further pursue the improvement in power density, it has been attempted to increase the switching frequency into the lower and medium megahertz range. However, to operate the semiconductor switches in very high frequencies, the capacitive turn-on loss associated with the parasitic junction capacitance of the semiconductor switches has to be avoided. Recognizing the duality relationship existing between the current-waveform shaping and the voltage-waveform shaping, the zero-voltage switching technique is developed. It is found that current-mode resonant switch structures can be modified in a very simple manner to become voltage-mode resonant switches. As a result, a novel zero-voltage technique is proposed. By shaping the device's off-state voltage waveform, this technique allows the power switches to turn on under a zero-voltage condition and, therefore, eliminate the turn-on loss associated with the parasitic junction capacitances. Consequently, practical quasi-resonant converter circuits that can operate in frequencies over 10MHz have been implemented.

The technique of replacing the power switches by current-mode or voltage-mode resonant switches has been shown to be a powerful tool in deriving new quasi-resonant converter topologies from the PWM converter topologies. In this work, the basic PWM converter topologies and their fundamental structure properties have been investigated, and many interesting results have been generated. To develop a large number of converter topologies from the basic PWM converters, topological variation and synthesis approaches are thoroughly surveyed. By applying the technique of resonant-switch replacement, a large number

of quasi-resonant converters can be generated from the numerous PWM converter topologies.

Furthermore, by investigating the fundamental characteristics of these two techniques and applying the duality principles, it has been rigorously proved that a duality relationship exists between the zero-current switching technique and the zero-voltage switching technique.

Research results have shown encouraging improvements in the performance of these two techniques over the conventional PWM converter technique. In particular, it is shown that the zero-voltage switching technique can be applied to increase the switching frequency into the 10MHz range and still maintain a high efficiency.

In summary, this dissertation has made a significant step toward the development of alternative techniques for high performance, high power-density SMPS circuits. It provides two promising topological means to alleviate the switching losses and stresses on the semiconductor devices. However, the success of developing high power-density SMPS circuits demands much more progress in all facets of power conversion technology. Among them, the following issues are believed to be most critical:

- Small-signal modelling and analysis which is critical to the design of control/regulation schemes.

- Further refinements in converter topologies, e.g., in improving the load sensitivity of the voltage-conversion ratios.

- Improvement in the semiconductor switching devices, especially in the parasitic resistances and capacitances.

- Improvement in components for high-power, high-frequency applications, particularly, in the magnetic and capacitive material and components.

- High-speed gate-drive circuits and control/regulation circuits.

- Advanced packaging and heat-sink engineering.

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