Design of a High Temperature GaN-Based Variable Gain Amplifier for Downhole Communications

Mohammed Ehteshamuddin

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Dong. S. Ha
Kwang-Jin Koh
Harpreet S. Dhillon

December 12, 2016
Blacksburg, VA

Keywords—Downhole communications, High temperature, VGA, GaN, Extreme environment, HEMT

Design of a High Temperature GaN-Based Variable Gain Amplifier for Downhole Communications

Mohammed Ehteshamuddin

ABSTRACT

The decline of easily accessible reserves pushes the oil and gas industry to explore deeper wells, where the ambient temperature often exceeds 210 °C. The need for high temperature operation, combined with the need for real-time data logging has created a growing demand for robust, high temperature RF electronics. This thesis presents the design of an intermediate frequency (IF) variable gain amplifier (VGA) for downhole communications, which can operate up to an ambient temperature of 230 °C. The proposed VGA is designed using 0.25 µm GaN on SiC high electron mobility transistor (HEMT) technology. Measured results at 230 °C show that the VGA has a peak gain of 27dB at center frequency of 97.5 MHz, and a gain control range of 29.4 dB. At maximum gain, the input P1dB is -11.57 dBm at 230 °C (-3.63 dBm at 25 °C). Input return loss is below 19 dB, and output return loss is below 12 dB across the entire gain control range from 25 °C to 230 °C. The variation with temperature (25 °C to 230 °C) is 1 dB for maximum gain, and 4.7 dB for gain control range. The total power dissipation is 176 mW for maximum gain at 230 °C.

Design of a High Temperature GaN-Based Variable Gain Amplifier for Downhole Communications

Mohammed Ehteshamuddin

GENERAL AUDIENCE ABSTRACT

The oil and gas industry uses downhole communication systems to collect important information concerning the reservoirs such as rock properties, temperature, and pressure, and relay it back to the surface. The electronics in these communication systems have to withstand temperatures exceeding 210 °C. Current high temperature electronics are not able to handle such temperatures for extended periods of time. Advancements in semiconductor technologies allow for fabrication of semiconductors that withstand high temperatures, such as GaN (Gallium Nitride). This thesis describes the design of a VGA (variable gain amplifier), which is an essential part of a downhole communication system. The VGA is designed using GaN semiconductor technology. Measured results show that the VGA shows good performance from 25 °C to 230 °C without the use of any cooling techniques, and can thus be used to design next-generation robust, high speed downhole communication systems.

Acknowledgements

I am grateful to Dr. Dong Ha for giving me the opportunity to work on this project, and for his constant guidance and support along the way. I would also like to thank Dr. Kwang-jin Koh and Dr. Harpreet Dhillon for serving on my thesis defense committee. The courses taught by these three professors have enlightened me in the fields of RF circuits and communication systems.

I would like to thank my colleagues in the Multifunctional Integrated Circuits and Systems (MICS) group for their valuable input and discussions during the course of my research. I learnt a lot from them, and was motivated by their hard work and dedication.

I am thankful for my parents. Their support and encouragement in whatever I do has been one of the biggest sources of strength and inspiration for me. I owe my achievements to them.

Table of Contents

Table of Figures

Table of Tables

Chapter 1

1 Introduction

High temperature electronics are generally used in environments where cooling is not practical. Cooling techniques may be avoided in applications that require high temperature operation along with decreased size, weight, and power dissipation, or increased reliability and efficiency. Industries such as aerospace, automotive, and oil and gas drilling have many such applications. For example, the automotive industry employs high temperature electronics for engine monitoring, on-wheel sensing, and exhaust monitoring. Similarly, the aerospace industry uses high temperature electronics and sensors near for engine control, landing gear, braking systems, etc. The oil and gas industry is the oldest user of high temperature electronics [1]. Oil drilling systems employ sensors to sense data concerning the geologic formations of the oil well, and relay the logged data to the surface using downhole communication systems. The ambient temperature of these wells is a function of the well depth. Today, the scarcity of oil resources and the need for real-time well logging has caused the oil and gas industry to drill deeper, necessitating faster and more robust communication systems.

1.1 Motivation

The continued efforts of the oil and gas industry to drill deeper to explore untapped wells have made the downhole environments harsher. The main challenge for downhole electronics is reliable high temperature operation, as the high pressure can be handled mechanically.

Fig. 1.1 shows the oil industry's well classification system based on temperature and pressure. The operation environment of the existing high temperature electronics is limited to the high pressure high temperature (HPHT) regions [2]. In fact, existing downhole electronics can operate only up to 177 °C before being brought back to the surface for cooling [2]. However, active/passive cooling and conventional heat extraction techniques are impractical to use in downhole environments due to weight, power consumption, and space constraints. As drilling operations go deeper, electronics capable of operating above 205 °C are required.

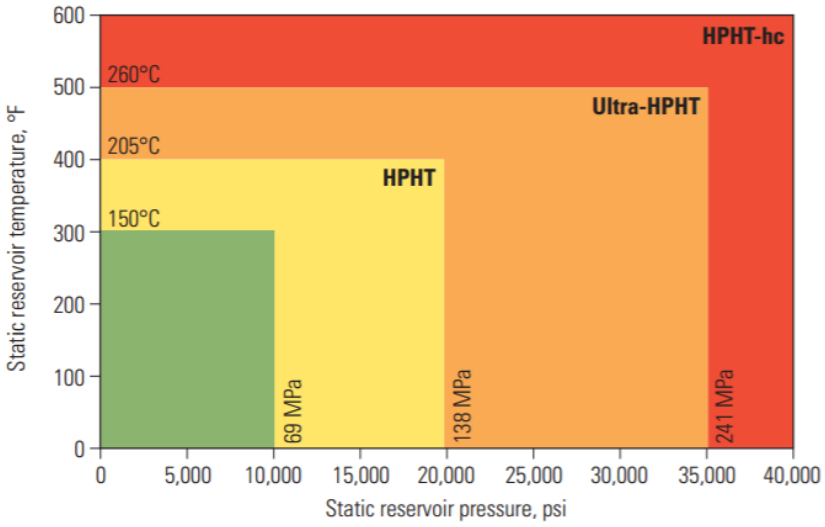


Fig. 1.1: Well classification system used in oil industry based on temperature and pressure [2].

In addition to the temperature limitation, current downhole systems can achieve data rates of only approximately 4 Mb/s at temperatures lower than 210 °C [3], which does not meet the growing demand for higher data rates due to higher resolution sensors, faster logging speeds, and additional tools available for a single wireline cable. This creates a great opportunity for the use of an RF cable modem for downhole communications.

An RF system can provide higher data rates compared to existing downhole systems, which operate at low frequencies. An essential component in the cable modem is the VGA. Downhole systems employ multiple data sensing tools at different drilling depths [3], and these tools can experience different signal attenuations due to variable depth. Thus, a VGA is required to ensure an acceptable signal level to analog-to-digital stage at different temperatures and variable cable length.

1.1.1 Thesis Statement

This thesis presents the design and testing of the first GaN-based IF VGA for an RF cable modem that operates up to an ambient temperature of 230 °C without the use of any active or passive cooling techniques. The VGA was designed as part of a downhole communication system operating in the frequency range of 230.5 – 253 MHz. The IF frequency after down-conversion is 97.5 MHz. This band was selected based on system simulation results, as there is no restriction in operating frequency range in downhole environments. This is the first IF VGA

that exists in the literature at the time of this writing designed using GaN and capable of operating at high temperatures above 200°C.

1.1.2 Technology

The operating temperature capability of a semiconductor is decided by its bandgap energy. Typical silicon device technologies are rated to maximum junction temperatures of less than 125 °C. Advancements in silicon and other common transistor technologies have allowed for extending the operating temperature limit, but these techniques are limited by the decomposition temperature of the semiconductor material itself. Wide bandgap power transistors, on the other hand, offer high junction temperatures and low total thermal resistances. Of the semiconductor technologies currently fabricated, Silicon Carbide (SiC) and Gallium Nitride (GaN) can reach the highest temperatures. SiC cannot be used for RF circuits due to low transition frequencies (f_T) [4]. GaN offers both high temperature and high frequency capabilities and is the most promising technology for the target application [4] due to its low noise figures, high linearity, and high gain [5]. Although not a common commercial technology, the increased research efforts in GaN design and fabrication shows that it has a great potential for the future. Thus, GaN technology was selected for the proposed VGA.

1.2 Thesis Organization

This thesis is organized as follows: section 2 presents the background for this thesis, which provides a brief overview of concepts and definitions used in RF circuit design, followed by high temperature circuit design considerations. This sub-section covers high temperature effects in semiconductors, review of semiconductor technologies that have potential for high temperature applications, and thermal analysis equations for designing circuit and PCB. Finally, section 2 describes some common VGA topologies and presents a literature review of existing high temperature VGA designs.

Section 3 describes the proposed VGA design. This section includes active and passive device selection, followed by specifications of the VGA. Then, the proposed VGA schematic will be shown, and circuit design will be described in detail. This section ends with layout and prototyping of the VGA design.

In section 4, the measurement setup and measurement procedures are described for various performance tests. This is followed by measurement results and analysis of the results.

Section 5 concludes the paper. Future work and potential improvements to the design will be discussed.

Chapter 2

2 Background

This chapter will cover the explanation of some basic RF circuit design concepts, high temperature circuit design considerations, review of high temperature semiconductor device technologies, and VGA circuit topologies. Finally, a literature review will be done to present existing high temperature VGA works.

2.1 Definitions and Concepts

2.1.1 S-Parameters

RF networks are characterized using travelling waves. Measurements at RF and microwave frequencies usually involve the power of a travelling wave, because the measurement of voltages and currents at high frequencies is very difficult. This is also why gain of an RF circuit is generally characterized as power gain instead of voltage gain. The scattering parameters (s-parameters) are a direct representation of these waves and give the incident, reflected, and transmitted wave powers, which are needed to characterize an RF/microwave network. Fig. 2.1 shows a two-port network, with V_1^+ and V_2^+ being the incident waves, and V_1^- and V_2^- the reflected waves.

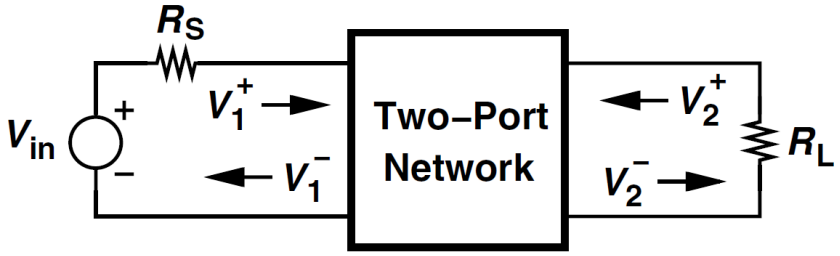


Fig. 2.1: Two port network with incident and reflected waves [6].

- S_{11} is defined as the ratio of reflected to incident wave at the input port when incident wave at output port is zero. It can be expressed as-

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} \tag{2.1}$$

$$or, S_{11}(dB) = 20log\left(\left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0}\right) \tag{2.2}$$

S_{11} is a measure of how accurately the input impedance looking in to the 2 port network is matched to the source impedance (R_s). A good match implies that the reflected wave is very small, and hence S_{11} magnitude is small.

- S_{12} is defined as the ratio of reflected wave at the input port to the incident wave at the output port, when incident wave at input port is zero. It can be expressed as

$$S_{12} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0} \tag{2.3}$$

$$or, \qquad S_{12}(dB) = 20log\left(\left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0}\right) \tag{2.4}$$

S_{12} is a measure of reverse isolation of the network, i.e., how much of output signal can couple to the input.

- S_{21} is defined as the ratio of reflected wave at the output to the incident wave at the input, when the incident wave at the output is zero. It can be expressed as

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{2.5}$$

$$or, \qquad S_{21}(dB) = 20log\left(\left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0}\right) \tag{2.6}$$

S_{21} is a measure of the forward gain of the network.

- S_{22} is defined as the ratio of the reflected wave to the incident wave at the output, when the incident wave at the input is zero. It can be expressed as

$$S_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0} \tag{2.7}$$

$$or, S_{22}(dB) = 20log\left(\left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0}\right) \tag{2.8}$$

S_{22} is a measure of how accurately the output impedance looking in to the 2 port network is matched to the load impedance (R_L). A good match implies that the reflected wave is very small, and hence S_{22} is small.

2.1.2 Noise Figure

Noise added by the circuit is generally measured in terms of the noise figure (NF) of a circuit, which is defined as the ratio of the signal to noise ratio (SNR) at the input, to the SNR at the output of the circuit. This ratio should be 1 for a noiseless circuit. The quantity inside the logarithmic function in 2.9 is referred to as the noise factor.

$$NF = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{2.9}$$

For noise figure calculation purposes, the input and output signal to noise ratios of a system can be defined in terms of the noise voltages of its individual elements. Fig. 2.2. shows such a system in which a circuit of input impedance Z_{in}, is provided an input signal by a source with resistance R_s. The signal to noise ratios at the input and output of the circuit can be calculated as-

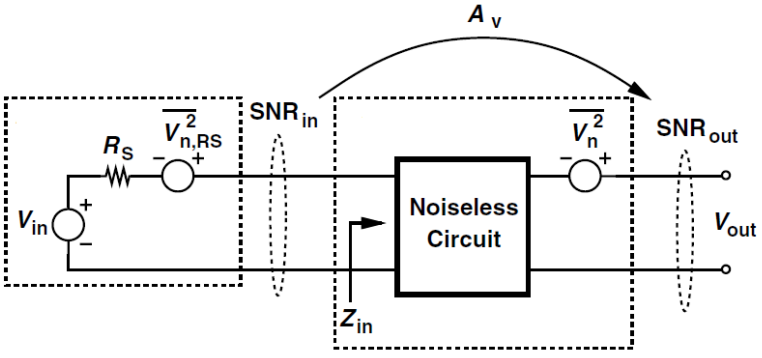


Fig. 2.2: Representation of noise in a circuit [6].

$$SNR_{in} = \frac{V_{in}^2 \alpha^2}{\overline{V_{n,RS}^2}} \tag{2.10}$$

$$SNR_{out} = \frac{V_{in}^2 \alpha^2 A_v^2}{\overline{V_{n,RS}^2} \alpha^2 A_v^2 + \overline{V_n^2}} \tag{2.11}$$

Where $\alpha = Z_{in}/(Z_{in} + R_s)$ is the attenuation factor of the source voltage due to impedance mismatch, V_{in} is source voltage, $\overline{V_{n,RS}^2} = 4kTR_s$ is the noise power of the source resistance in 1 Hz bandwidth, $\overline{V_n^2}$ is the noise power generated by the circuit in 1 Hz bandwidth, and A_v is the voltage gain of the circuit. The noise figure can be written as

$$SNR_{out} = 10 \log\left(\frac{SNR_{in}}{SNR_{out}}\right) = \frac{\overline{V_{n,RS}^2} \alpha^2 A_v^2 + \overline{V_n^2} V_{in}^2}{\alpha^2 A_v^2} . \frac{1}{4kTR_s} \tag{2.12}$$

The total noise figure of a cascaded system with 'n' stages is given by Frii's equation.

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{(NF_2 - 1)}{A_{p,1}} + \frac{(NF_3 - 1)}{A_{p,1} A_{p,2}} + \frac{(NF_n - 1)}{A_{p,1} A_{p,2} \dots A_{p,n-1}} \tag{2.13}$$

Where NF_n and $A_{p,n}$ are the noise figures and power gains of the nth stage respectively. From 2.13 we can infer that the first stage in the cascade contributes the most to the overall noise figure.

2.1.3 Linearity

Ideally, a circuit's output voltage follows its input voltage linearly. However, transistors are non-linear and the output voltage of a circuit such as an amplifier exhibits several higher order non-linearities, causing undesired effects such as gain compression, harmonic distortion, intermodulation, etc. The output of a memoryless system can be approximated as shown in 2.14.

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots \tag{2.14}$$

The first term represents DC, while the second term represent the fundamental tone. The third and fourth terms represent the second and third harmonics, respectively.

2.1.3.1 Compression

If a sinusoidal signal is provided as input to the system described by 2.14, we obtain the following output by ignoring the DC component

$$y(t) = \alpha_1 A cos(\omega t) + \alpha_2 A^2 cos^2(\omega t) + \alpha_3 A^3 cos^3(\omega t) \tag{2.15}$$

Upon solving, the fundamental component at frequency ω is obtained

$$y(t) = \left(\alpha_1 A + \frac{3\alpha_3}{4} A^3\right) cos(\omega t) \tag{2.16}$$

For a large value of input signal amplitude *A*, gain compression occurs because α_3 is negative for most RF circuits [7].

The input 1dB compression point is a measure of the compression, and hence linearity, of an RF circuit. It is defined as the input power for which the small signal gain of a circuit is reduced by 1 dB. In Fig. 2.3, $A_{in,1dB}$ represents the input 1 dB compression point.

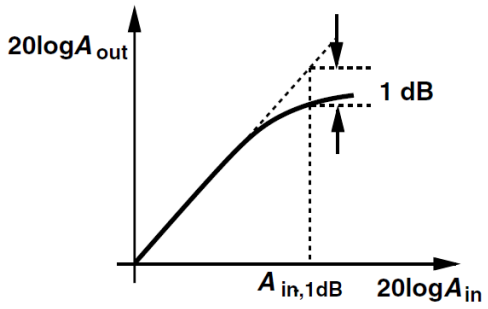


Fig. 2.3: Output power vs input power showing 1 dB compression of the gain [7].

The input 1 dB compression can be calculated by the following equation

$$20log\left|\alpha_1 + \frac{3\alpha_3}{4} A_{in,1dB}^2\right| = 20log|\alpha_1| - 1 \tag{2.17}$$

$$A_{in,1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.18}$$

Thus, 1dB compression point of an RF circuit should be high enough so that the input signal is not distorted. The input power level of an RF circuit should be several dBs below the input 1dB compression level.

2.1.3.1 Intermodulation (IP2 and IP3)

Intermodulation effects can be calculated using a two-tone input in 2.15. Due to the non-linearity of the circuit, tones can be generated at frequencies that result from the mixing of the two inputs.

$$y(t) = \alpha_1(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)) + \alpha_2(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t))^2 + \alpha_3(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t))^3 \quad (2.19)$$

The resultant expression gives the amplitude of the frequency components at the fundamental (first order) frequencies ω_1 and ω_2, the second order intermodulation (IM2) frequencies $\omega_1 \pm \omega_2$, and third order intermodulation (IM3) frequencies $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. If the frequencies of the input tones are close enough to each other, the IM2 and IM3 terms will fall close to the input frequencies. The amplitudes of intermodulation products obtained upon solving 2.19 are

$$\boldsymbol{IM2\ products}: \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)\, t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)\, t \quad (2.20)$$

$$\boldsymbol{IM3\ products}: \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)\, t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2)\, t \quad (2.21)$$

$$\boldsymbol{IM3\ products}: \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1)\, t + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 - \omega_1)\, t \quad (2.22)$$

From 2.20 – 2.22, it can be inferred that as the inputs A_1 and A_2 increase, the output power levels of IM2 and IM3 products increase at a higher rate (also shown in Fig. 2.4). For high enough input power levels, the output power levels of IM2 and IM3 meet the fundamental output power levels. These input power levels are termed as IIP2 and IIP3, respectively.

In order to measure the IIP2 and IIP3 of a circuit, tones close to each other in frequency are sent as inputs to the circuit. The output spectrum shows the inputs at the fundamental frequencies, and the intermodulation products. An example output spectrum is shown in Fig. 2.5.

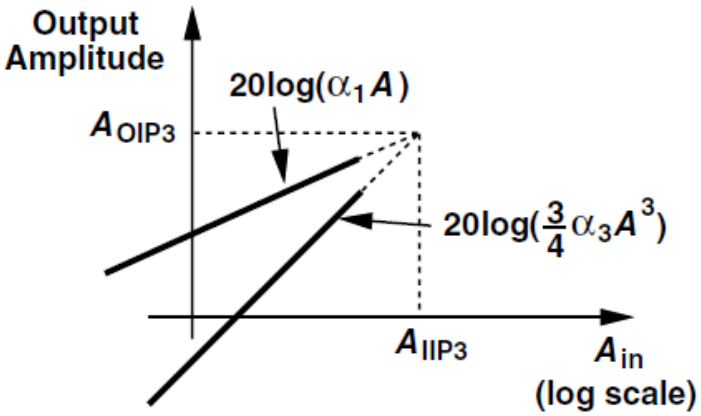


Fig. 2.4: IIP3 of an RF circuit [7].

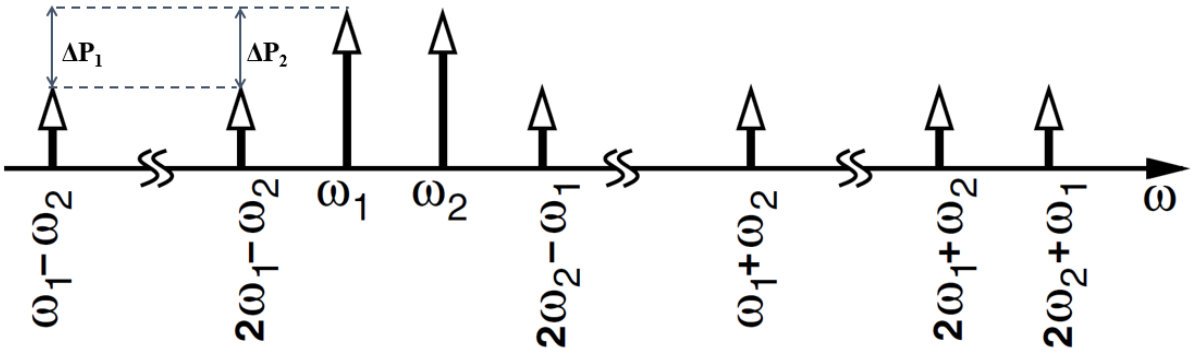


Fig. 2.5: Output spectrum of a two-tone test [7].

IIP2 and IIP3 can be calculated using the following equations

$$IIP3|_{dBm} = P_{in}|_{dBm} + \frac{\Delta P_2|_{dB}}{2} \tag{2.23}$$

$$IIP2|_{dBm} = P_{in}|_{dBm} + \Delta P_1|_{dB} \tag{2.24}$$

P_{in} is the power level of the input tones, and ΔP_1 and ΔP_2 are the differences in power levels between the IM2/IM3 tones and the output power level of fundamental tones.

In a cascaded system, the end stages dominate the overall linearity of the system. This can be seen in 2.25.

$$\frac{1}{A_{IIP3}^2} = \frac{1}{A_{IIP3,1}^2} + \frac{\alpha_1}{A_{IIP3,2}^2} + \frac{\alpha_1\alpha_2}{A_{IIP3,3}^2} + \cdots + \frac{\alpha_1\alpha_2 \ldots \alpha_{n-1}}{A_{IIP3,n}^2} \tag{2.25}$$

In the above equation, α_n and $A_{IIP3,n}$ denote the gain and IIP3 of the nth stage, respectively.

2.1.4 Stability

Stability is a critical consideration for any circuit or system. Instability may arise due to a negative impedance in a circuit or a part of the circuit. Negative impedances at the source or load of a circuit cause the source or load reflection coefficient (Γ_S or Γ_L) to be greater than or equal to 1, causing undesired oscillations, deviation from expected performance, and even circuit failure. An RF circuit can be defined as unstable, conditionally stable, or unconditionally stable. The distinction between the latter two terms is made depending on if the circuit is stable for any possible source or load impedance (unconditional stability), or for a particular range of source and load impedances (conditionally stable). RF circuits are preferred to have unconditional stability across a wide frequency range.

There are many measures of stability of a circuit (Rollet, Stern, Nyquist, etc.). The μ stability factor is another measure of circuit stability, and it only uses a single equation without the need of any auxiliary conditions. μ-factors can be calculated for the source (μ′) and load (μ) of a circuit, and the condition for unconditional stability is that either μ or μ′ > 1 [8].

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*.\Delta| + |S_{21}.S_{12}|} \tag{2.26}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*.\Delta| + |S_{21}.S_{12}|} \tag{2.27}$$

where $\Delta = S_{11}S_{22} - S_{21}S_{12}$

For μ or μ′ > 1, the circuit will not show $\Gamma \geq 1$ at either the source or the load and is unconditionally stable. For any other value of μ, the circuit may be conditionally stable, and the load and source impedances for which $\Gamma \geq 1$ can be seen from the load and source stability circles on the smith chart.

2.1.5 Impedance matching

Impedance matching is very important in RF circuits because it allows maximum transfer of power from source to the DUT, and from DUT to the load. In RF PCB design, it is almost always necessary, unlike in RF ICs. Many types of matching networks exist in both microstrip and lumped element forms. Most circuits require matching for maximum gain (maximum power transfer). Since $S_{12} \neq 0$ for transistors, the reflection coefficients at input and output are affected

by each other. Simultaneous conjugate matching is employed to achieve both input and output matching (see Fig. 2.6).

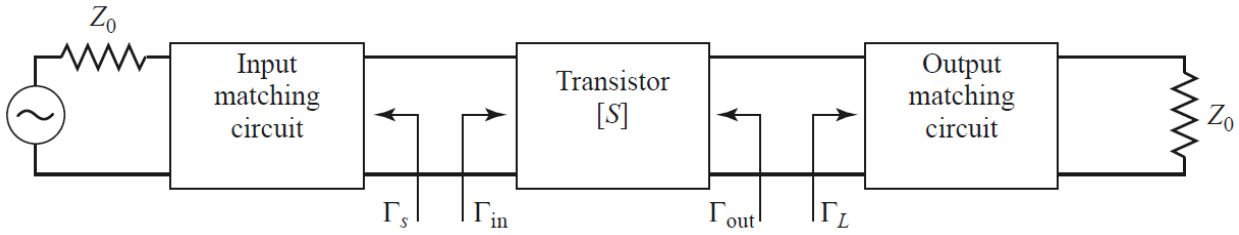


Fig. 2.6: Matching a transistor (characterized by S parameters) to source and load impedances Z_0 [9].

To achieve simultaneous matching, reflection coefficients looking in to the input (Γ_{in}) and output (Γ_{out}) of the transistor are calculated, and the matching networks are designed to exhibit reflection coefficients that are conjugate value of Γ_{in} and Γ_{out} looking from the input and output of the transistor, respectively.

$$\Gamma_s = \Gamma_{in}^* = \left(S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right)^* \tag{2.28}$$

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}\right)^* \tag{2.29}$$

Upon solving 2.28 and 2.29, the required values of Γ_S and Γ_L can be found. These values can be implemented using either microstrip lines, or lumped elements. This is determined by the matching network bandwidth and quality factor (Q) required by the application. Microstrip lines can achieve a moderate Q matching network at low frequencies, and also consume space. Lumped elements networks (L, π, T, etc.) provide more flexibility in low or high Q selection, and allow for a compact matching network, but are prone to variations with temperature. A specific Q factor set by design requirements can be achieved using a 3 element π or T matching network.

2.2 High Temperature Design Considerations

Passive and active devices employed in circuits suffer from several high temperature effects which have to be considered during circuit design. This section will describe some of the high temperature effects in semiconductors, followed by a review of the semiconductor technology

for high temperature operation. Finally, some thermal equations will be shown which will help in the circuit and PCB board design.

2.2.1 High Temperature Effects in Semiconductors

Almost all semiconductor device characteristics are effected by temperature. In this section, the effects of temperature on some critical parameters of a semiconductor device such as bandgap energy, carrier mobility, carrier density, threshold voltage, subthreshold leakage current, and drain current will be discussed briefly.

2.2.1.1 Bandgap Energy

As temperature increases, the energy bandgap of a semiconductor decreases. The dependence of bandgap energy on temperature is given by 2.30 [10]

$$E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \tag{2.30}$$

where $E_g(0)$ (in Kelvin) is the bandgap energy at absolute zero, and α_E and β_E are material-specific constants.

2.2.1.2 Carrier Density

The carrier density depends on the region of operation of the semiconductor. As temperature increases, the semiconductor moves from an extrinsic operation region, where carrier density is constant with temperature, to an intrinsic operation region, where carrier density increases with temperature. At high temperatures, the intrinsic carriers dominate. The dependence of the intrinsic carrier concentration is given by [10]

$$n_i \propto T^{1.5} \mathrm{e}^{\frac{-\mathrm{E_g}(0)}{2kT}} \tag{2.31}$$

where n_i denotes the intrinsic carrier concentration. As temperature increases, the intrinsic carrier concentration also increases.

2.2.1.3 Carrier Mobility

Mobility depends on both temperature and electric field. Effective carrier mobility depends on four scattering parameters within a semiconductor, namely, phonon scattering (μ_{ph}), surface

roughness scattering (μ_{sr}), bulk charge coulombic scattering (μ_{cb}), and interface charge coulombic scattering (μ_{int}). Using Matthiessen's rule, effective mobility can be approximated as

$$\frac{1}{\mu_{eff}(T,E_{eff})} = \frac{1}{\mu_{ph}(T,E_{eff})} + \frac{1}{\mu_{sr}(T,E_{eff})} + \frac{1}{\mu_{cb}(T,E_{eff})} + \frac{1}{\mu_{int}(T,E_{eff})} \tag{2.32}$$

At high temperatures, phonon scattering dominates due to an increase in lattice vibrations. Thus, mobility decreases at high temperatures because phonon scattering decreases ($\mu_{ph} \propto T^{-3/2}$) [10].

2.2.1.4 Threshold Voltage

Threshold voltage decreases with an increase in temperature. The threshold voltage equation is

$$V_{TH} = \left(\phi_{gs} - \frac{Q_{SS}}{C_{ox}}\right) + 2\phi_F + \left(C_{ox}\sqrt{2q\varepsilon_r N_A}\right)\sqrt{2\phi_F} \tag{2.33}$$

where $\phi_{gs} = \frac{kT}{q}\ln\left(\frac{N_A N_G}{n_i^2}\right)$ is the gate-substrate contact potential, Q_{SS} is the surface charge potential, C_{ox} is the oxide capacitance, and N_A and N_G are the substrate and gate doping concentrations, respectively, ϕ_F is the fermi energy level, γ is the body effect parameter, and ε_r is the relative permittivity of the semiconductor.

The derivative with respect to temperature of the threshold voltage equation gives

$$\frac{\partial V_{TH}}{\partial T} = \left(\frac{\partial \phi_{gs}}{\partial T}\right) + 2\frac{\partial \phi_F}{\partial T} + \frac{\left(C_{ox}\sqrt{2q\varepsilon_r N_A}\right)}{\sqrt{2\phi_F}}\frac{\partial \phi_F}{\partial T} \tag{2.34}$$

The dependence of ϕ_{gs} and ϕ_F on temperature is given by

$$\frac{\partial \phi_{gs}}{\partial T} = \frac{1}{T}\left[\phi_{gs} + \left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right)\right] \tag{2.35}$$

$$\frac{\partial \phi_F}{\partial T} = \frac{1}{T}\left[\phi_F - \frac{1}{2}\left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right)\right] \tag{2.36}$$

Filanovsky and Allam [11] show by substituting empirical values in the above equations that the threshold voltage decreases with temperature.

2.2.1.5 Subthreshold Leakage

Subthreshold current increases with temperature. It has an exponential relationship with temperature, as seen in 2.37 – 2.38 [10]

$$I_{sub} = I_0 \left(e^{\frac{qV_{DS}}{kT}} - 1 \right) \tag{2.37}$$

$$\text{and, } I_0 = ATe^{-\frac{qE_G(0)}{2kT}} \tag{2.38}$$

where A is a material dependent constant.

2.2.1.6 Electromigration

Electromigration is a failure mechanism caused by a positive feedback phenomenon in areas of high current density. As established earlier, current density increases with temperature, making the circuit prone to electromigration where atoms are moving on a wire narrow their width, further increasing current density. This phenomenon usually continues until the wire breaks and current flow is halted [10]. Electromigration is a serious cause of concern at high temperatures, and thus current values should be minimized in high temperature design.

2.2.1.7 Drain Current

The variation of drain current with temperature depends on a couple of factors. It is mainly decided by the current density, mobility, and threshold voltage. As temperature increases, the combination of increase in current density and decrease of threshold voltage will cause the drain current to increase [10]. However, the decrease in carrier mobility with increasing temperature will influence the drain current to decrease with temperature. Thus, the variation in drain current is determined by the more dominant change of the above two factors.

Moreover, gate resistance, drain resistance, and source resistance increase with temperature [12], causing an increase in the circuit added noise. These effects should be taken into account in designing circuits for high temperature operation. Furthermore, design failures are also possible at high temperatures due to electromigration and thermal runaway, which are most likely to occur at high current densities. Selecting a suitable transistor technology and designing for low power are critical to mitigate the above high temperature effects.

2.2.2 Review of Semiconductor Technologies for High Temperature Operation

This section provides a review of semiconductor technologies used at high temperatures either commercially, or in literature.

2.2.2.1 Silicon and Silicon-on-Insulator (SOI)

Due to their high integrability, cost effectiveness, and a mature fabrication process, Silicon and SOI processes have been developed for high temperature applications. A few high temperature designs using CMOS processes have been reported. Davis and Finvers [13] report a ΣΔ modulator capable of operation with 14-bit resolution at 225 °C and 13-bit resolution at 255 °C using a standard 1.5 µm CMOS process. de Jong et al. [14] report a 300°C dynamic feedback instrumentation amplifier using a junction isolated CMOS process. While have shown operability at high temperatures, CMOS based designs have not been made commercially available and are mostly limited to the 85 °C maximum temperature limit. The main drawback of Si based technologies is that PN junctions do not provide good isolation and cause a large leakage current at high temperatures [15]. Therefore, most high temperature silicon based circuits are almost exclusively done using SOI process, where transistors are surrounded by silicon dioxide. Unlike the PN junction, isolation properties of silicon dioxide do not degrade a lot with temperature and hence leakage currents are lower. Companies such as Honeywell have developed an SOI process for high temperature applications (> 200 °C), addressing the need for analog and low frequency electronics in downhole drilling applications [15]. A number of high temperature analog designs have been reported using SOI processes. However, high temperature RF circuits have not been reported using SOI processes. Due to drawbacks such as decrease of channel mobility, increase in junction leakage current, decrease in saturation current, and lateral bipolar effects due to hot carrier effects [15], SOI technologies have not found a synergy with RF electronics.

2.2.2.2 Silicon Germanium (SiGe)

SiGe devices have wide temperature ranges, and are better suited for high speed RF applications than SOI devices because of better high frequency performance, but still not as good as GaAs or GaN. SiGe Heterojunction Bipolar Transistors (HBTs) are widely used at cryogenic temperatures because of superior performance. However, efforts have been made to optimize this

technology to work at high temperatures and applications operating at temperatures as high as 300 °C have been reported [16]. Chen et al. [17] report the DC and AC characteristics of SiGe HBTs at high temperature. As far as the DC characteristics are concerned, the turn on voltage decreases as expected, and the device maintains a good current gain and high current drive capability at high temperature. However, a cause of concern is minority carrier generation in the collector-substrate junction causing parasitic leakage. In terms of AC characteristics, SiGe HBTs seem to provide acceptable transition frequencies, low frequency noise performance, current gain, and breakdown voltage [17]. However, high frequency noise, leakage current, and latch up issues keep SiGe HBTs from being widely used for high temperature RF applications. Quite often SiGe is used in a BiCMOS implementation (SiGe HBT + Si CMOS) because it offers high integrability with CMOS systems.

2.2.2.3 Gallium Arsenide (GaAs)

Due to higher bandgap of GaAs (1.4 eV) as compared to Silicon (1.1 eV), the theoretical operating temperature capability of GaAs is almost twice that of Silicon [18]. GaAs has been widely employed in modern communication and military technologies due to superior high frequency performance. GaAs is very popular for RF power and low noise circuits operating at RF and mm-wave frequencies [18]. GaAs devices are usually implemented in MESFET, HEMT, and JFET configurations. For high temperature applications, GaAs transistors are fabricated with a wide bandgap AlGaAs layer on top of an InGaAs layer below the gate of the transistors. These layers act as blocking barriers and reduce gate leakage current at high temperatures. This offers a significant advantage in terms of leakage current, which was a major drawback in SOI and SiGe technologies. Reference [18] also shows an X-band mixer that operates up to 300 °C and degrades <10dB over the entire temperature range using maximum conversion gain biasing control. While GaAs seems a very good choice for high temperature RF circuits, GaN is more promising with its higher gain, lower noise, and higher power density characteristics at high temperatures.

2.2.2.4 Silicon Carbide (SiC)

SiC is mainly used in power electronics due to its wide bandgap and high thermal conductivity. Due to the wide bandgap, SiC devices can potentially operate up to 600 °C. SiC

BJTs have demonstrated high current gains (> 50-100) and high breakdown voltages (1.2-10 kV) at 300 °C [19], and these characteristics have made them the technology of choice in power electronics applications. SiC exists in different structural configurations, namely, 4H-SiC, and 6H-SiC. Their properties are only slightly different. 6H-SiC is sometimes favored over 4H-SiC due to its superior polytype structural stability during thermal processing steps [19]. Several works utilizing SiC transistors for high temperature power electronics and analog electronics have been reported [20], [21]. However, due to low transition frequency, SiC device technology lends itself only for low frequency applications. Hence, it is not suitable for RF applications despite good high temperature performance.

2.2.2.5 Gallium Nitride (GaN)

GaN is the most promising technology in terms of both high temperature and RF performance. GaN shows many favorable characteristics such as wide bandgap, high breakdown voltage, high electron mobility, and high carrier saturation velocity across a wide temperature range, making it ideal for high frequency and high power applications [19]. Although not a commonly available commercial technology, GaN is experiencing increase in manufacturing and maturity in fabrication process. A lot of research is being conducted in terms of both fabrication and characterization to develop GaN devices for high temperature applications [12], [22]-[25].

High temperature RF circuits including power amplifiers, low noise amplifiers (LNA), and mixers designed using GaN technology have been reported, all showing very good performance at high temperatures. Carruba et al. [26] report a continuous class-E sub-waveform power amplifier that achieves up to 71% efficiency at 150 °C. Silva et al. [27] report a power amplifier for C-band applications with a high gain of 24.6 dB and output 1 dB compression of 36 dBm at an operating temperature of 205 °C. Cunningham et al. report [28] a wideband LNA capable of operating up to 230 °C with a sub 3 dB noise figure and high linearity. Salem and Ha [29] report a down-conversion mixer achieving high conversion gain and good linearity at 250 °C.

2.2.3 Thermal Analysis

At high temperatures, it is very important to consider the thermal dissipation of the circuit to avoid exceeding the junction temperature limits of the transistors and the passive components. In downhole applications, the use of active or passive cooling techniques is not feasible due to size

and power constraints. Thus, a thermal analysis of the PCB board is necessary to determine the safe power dissipation limit of the design, in order to avoid exceeding the junction temperature ratings of the transistor. The power dissipation limit can be found from the thermal equation

$$P_D = \frac{T_J - T_A}{\theta_{JA}} = \frac{T_J - T_A}{\theta_{JC} + \theta_{CA}} \tag{2.39}$$

The maximum power dissipation (P_D) that can be handled without the use of a heatsink is calculated from 2.39 by setting the ambient temperature (T_A), and the maximum safe junction temperature of the transistor (T_J). The parameter θ_{JA} represents the junction to ambient thermal resistance of the system. This quantity can be broken up into two thermal resistances, namely, junction to case thermal resistance of transistor (θ_{JC}) and case to ambient thermal resistance (θ_{CA}). As shown in Fig. 2.6, the case to ambient thermal resistance can be further represented as a sum of different thermal resistances ($\theta_{CS} + \theta_S + \theta_{SA}$) based on the layout of the transistor on the PCB.

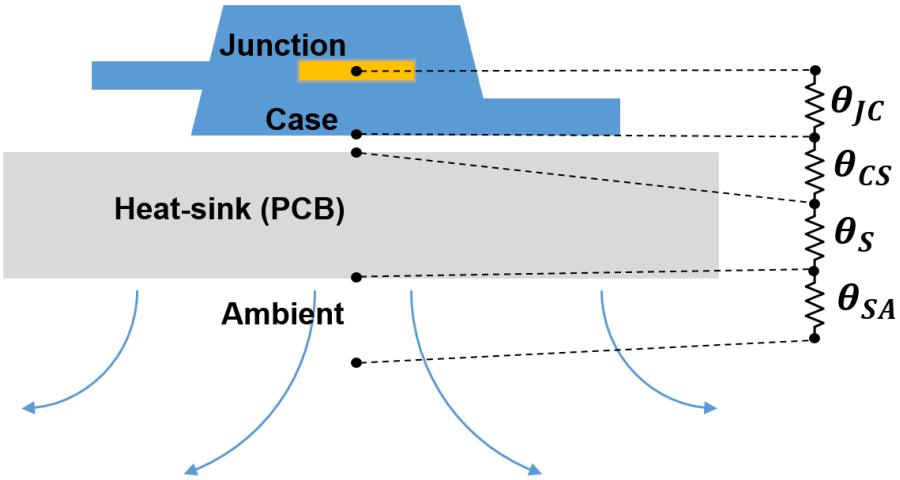


Fig. 2.7: Thermal resistances in a transistor case from the transistor junction to ambient.

2.3 VGA Topologies

Some common VGA topologies are discussed in this section. They will serve as a premise for selecting the topology for the proposed VGA, and will also provide small signal analysis that can be used in the proposed design. VGA topologies consisting of a large number of transistors such as Gilbert and Folded Gilbert cells are not discussed here. VGA design using discrete

components does not allow usage of complex topologies with a large number of transistors due to size, layout mismatch, and lack of control over the widths and lengths of transistors.

2.3.1 Variable Bias

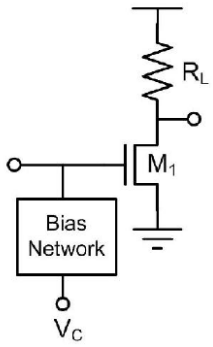


Fig. 2.8: Variable bias topology [30].

This is the simplest VGA topology, where input is provided to MOSFET M_1, and the gain is controlled by varying the gate voltage of M_1, which changes the drain current. Changing the current changes the transconductance (g_m), which effects the gain of the transistor as shown below

$$Gain = -g_m R_L = -\mu_n C_{ox} \frac{W}{L} (V_C - V_{th}) R_L \tag{2.40}$$

Where μ_n denotes electron mobility, C_{ox} is oxide capacitance, V_{th} is the threshold voltage, and W, L are transistor dimensions. The drawback of this topology is that the linearity of the amplifier strongly depends on its bias current. The advantages are compact design, low power, and low noise figure.

2.3.2 Variable Feedback

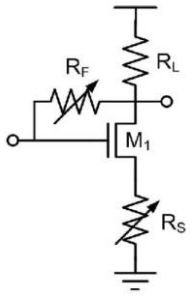


Fig. 2.9: Variable feedback topology [30].

The variable feedback topology is self-explanatory in that the gain is controlled by varying the feedback resistance. The feedback resistor can also be implemented using a MOSFET. The advantages of this topology are that it has a high potential for IP3, and requires low DC bias because of a single transistor. However, this topology can have stability problems, a low bandwidth, and a narrow gain control range [30]. Moreover, it may not be suitable for applications requiring high gain due to a single transistor and also due to the presence of feedback.

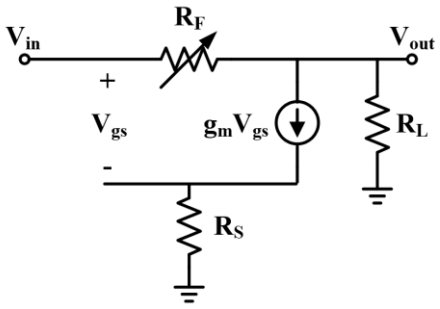


Fig. 2.10: Small signal model of variable feedback topology.

The gain of this topology can be calculated from the small signal model in Fig. 2.9.

$$\frac{(V_{in} - V_{out})}{R_F} = g_m V_{gs} + \frac{V_{out}}{R_L} \tag{2.41}$$

$$V_{in} = V_{gs}(1 + g_m R_S) \tag{2.42}$$

Using 2.42 in 2.41 and solving for gain gives

$$V_{in}\left(\frac{1}{R_F} - \frac{g_m}{1 + g_m R_S}\right) = V_{out}\left(\frac{1}{R_F} + \frac{1}{R_L}\right) \tag{2.43}$$

$$\frac{V_{out}}{V_{in}} = \frac{(R_L + g_m R_L(R_S - R_F))}{(1 + g_m R_S)(R_F + R_L)} \tag{2.44}$$

2.3.3 Cascode

This configuration consists of a common source (CS) transistor (M_1) with a common gate (CG) cascode load (M_2).

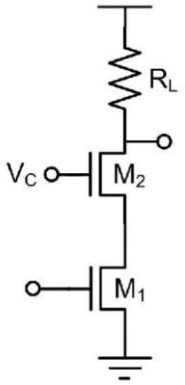


Fig. 2.11: Common source cascode topology [30].

The input is provided to the CS amplifier. The gain of the circuit is controlled by reducing/increasing the drain current by varying the gate-source voltage of M_2. Thus, V_c can be thought of as the control voltage of the circuit. M_1 operates in the triode region, and thus, increasing or decreasing V_C changes the gain of the circuit since g_m of triode transistor changes.

The gain can be derived from the small signal model in Fig. 2.11 by looking at the effective impedance at the output. Ignoring the parasitic drain source capacitors (c_{ds}), the effective output impedance is a parallel combination of the impedance looking up (R_L) and looking down ($g_{m2}r_{o1}r_{o2}$) from the output.

$$Gain = -g_{m1}[R_L||(g_{m2}r_{o1}r_{o2})] \tag{2.45}$$

The presence of only one current path also helps to reduce the overall power consumption.

2.3.4 Current Steering

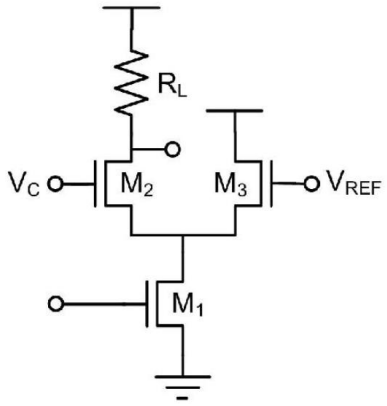


Fig. 2.12: Current steering topology [30].

This topology is similar to the cascode topology discussed earlier. It uses cascode transistors to steer current to and from the load. This allows for a high gain control range due to the addition of M_3. The small signal input is provided to M_1, while V_c controls the current through the branch.

Another advantage is a potentially lower noise figure compared to the cascode topology, especially in low gain state. In the cascode topology, the current in M_1 is very low in low gain conditions, which means the g_m of M_1 is low, resulting in a higher noise figure [30] . In the current steering topology, M_3 ensures that in low gain state, the current through M_1 is not very low and noise figure is better than cascode topology

2.4 Literature Review

Recently, there have been very few VGA designs [31], [32] capable of operating at high temperatures. Kumar et al. [31] report a temperature compensated VGA that operates up to 85 °C. The VGA consists of a fully differential three stage cascaded amplifier with DC offset cancellation. The VGA core consists of a common emitter amplifier, whose gain is controlled by its bias current. A 6-bit control word decides the bias current of the amplifier which makes this design a digitally controlled VGA. A maximum 2 dB variation in gain was reported from 25 °C to 85 °C. The linearity and noise performances are listed in table 2.1 below. Liu et al. [32] report an AGC circuit operating up to 200 °C. The AGC circuit includes a folded Gilbert VGA, DC offset cancelling block, and a post-amplifier, all of which contribute to the AGC gain of 22.5 to -12.5 dB, and dynamic range of 35 dB at 200 °C. The temperature compensation block generates an appropriate bias voltage according to the incoming signal and the ambient temperature. The temperature compensation range is -20 °C to 200 °C. Both of the aforementioned designs are implemented in SiGe BiCMOS technology which suffers from high leakage current as temperature increases, potentially causing latch-up. Furthermore, multiple amplifier stages are required to achieve the reported gains and gain control ranges. Table 2.1 provides a comparison of the above works with the performance of the proposed VGA.

TABLE 2.1: PERFORMANCE COMPARISON OF HIGH TEMPERATURE VGAS

Parameter	**This work**	**[31]**	**[32]**
Temperature (°C)	**25 to 230**	25 to 85	-20 to 200
Technology	0.25 µm GaN on SiC HEMT	0.18 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS
Frequency (MHz)	97.5	2 – 1900	0.2 – 7500
Gain (dB)	28 to -6.23	7.8 to -10.6	30 to -10
Gain Control range (dB)	34.23	18.4	~ 40
Input P1dB (dBm)	-3.63 to -15	-11 to -12.5	-
Noise Figure (dB)	7.63 – 18.9	21.4 to 27.1	-
Power (mW)	16 – 176	12.2	72

Chapter 3

3 Proposed VGA Design

In this chapter, the specifications of the VGA circuit will be discussed, and circuit component selection will be shown. Then, circuit design including core circuit, bias circuit, stability circuit, and matching network will be elaborated. Simulation and modelling results will be shown.

3.1 Device Selection

A critical step in the design of the high temperature VGA is choosing the technology that can withstand high temperature and provide reliable performance up to 230 °C. However, the choices available for commercial off-the-shelf (COTS) active and passive devices that can operate at high temperature are very limited. This section will describe the components chosen for use in the design.

3.1.1 Active Device Selection

Based on the review of high temperature capabilities of semiconductor technologies in chapter 2, it is clear that GaN offers superior performance in both high temperature and high frequency domains, and is the most promising technology for the target application. For this design, Qorvo (formerly TriQuint) T2G6000528-Q3 GaN on SiC HEMT is used (see Fig. 3.1). The transistor has a maximum junction temperature T_J of 275 °C, and a junction to case thermal resistance θ_{JC} of 12.4 °C/W. At the time of this work, this was the only commercial off-the-shelf (COTS) transistor available with such a high operation temperature capability. The main application for this device is high power amplifiers, and device characterization at V_{DS} = 28 V, I_D = 50 mA/125 mA at 25 °C and 85 °C is provided in the datasheet [34]. For the downhole communication application, the transistor will have to be biased at a lower drain current to decrease power consumption. Thus, both DC and small signal characterization will have to be done at a lower power consumption bias point.

Fig. 3.1: Selected transistor for the proposed VGA [34].

TABLE 3.1: ABSOLUTE MAXIMUM RATINGS OF QORVO T2G6000528-Q3 HEMT [34]

Parameter	Value
Breakdown Voltage (BV_{DG})	100V (Min.)
Drain Gate Voltage (V_{DG})	40V
Gate Voltage Range (V_G)	-10 to 0V
Drain Current (I_D)	2.5A
Gate Current (I_G)	-2.5 to 7mA
Power Dissipation (P_D)	15W
RF Input Power, CW, T = 25°C (P_{IN})	34dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 seconds)	320°C
Storage Temperature	-40 to 150°C

3.1.2 Passive Device and Interface Materials Selection

Capacitors from Presidio and IPDiA are used. Both capacitors are rated up to 250 °C. Presidio high temperature capacitors are made up of NP0 (negative-positive 0 ppm/°C) dielectric material, which shows little variation in capacitance over temperature, even up to 300 °C (Fig. 3.2). Their DC breakdown voltage rating is above 10 V, which is sufficient for this low power design. The datasheet also mentions that the dielectric withstanding voltage is almost 250 % of the rated DC breakdown voltage, which shows that the capacitors are very robust [35].

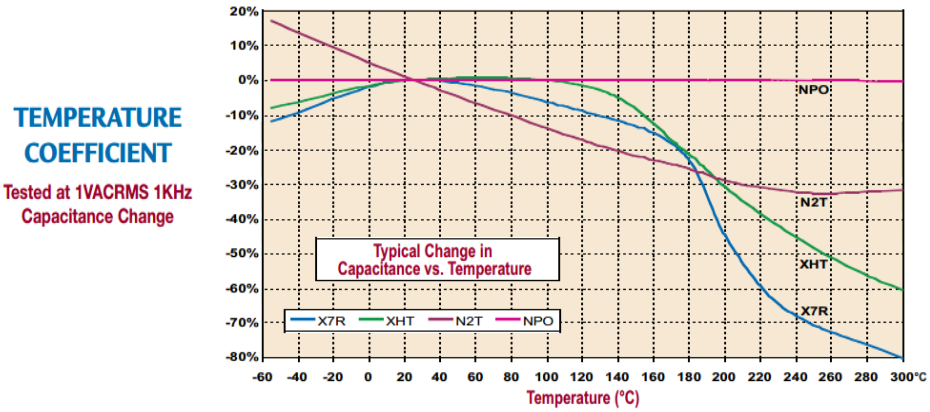


Fig. 3.2: Typical change in capacitance versus temperature for different dielectrics [34].

IPDiA capacitors were used for DC blocking in the bias network of the VGA. They are made using a passive integrated connecting substrate (PICS) technology, and the dielectric shows almost no variation in capacitance versus temperature [36]. The maximum temperature rating is 250 °C, with a temperature coefficient of < ±1.5% from -55 °C to 250 °C [36]. The breakdown voltage is 11 V and the tolerance of nominal capacitance value is 15% [36], which should not matter for DC blocking purposes.

Coilcraft iron core inductors are used as RF chokes in bias network. A 1 µH inductance value was used. According to the datasheet, the maximum operating temperature is 300 °C [37]. Fig. 3.3 shows the impedance plot versus frequency, which suggests that the self-resonant frequency of this inductor is around 350 MHz. This is well above the operating frequency of the proposed VGA.

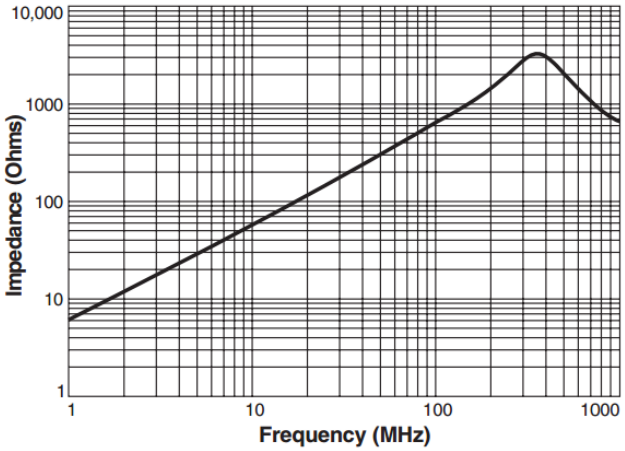


Fig. 3.3: Impedance versus frequency of Coilcraft 1 µH inductor [34].

Vishay thin film resistors, which can operate up to 250 °C [38] are used in the design. The resistors offer reasonably low tolerances of ± (0.1 – 5) %, while offering a low noise coefficient. From the power limit derating curve provided in the datasheet (shown in Fig. 3.4), it can be seen that at our maximum operating temperature of 230 °C, the power limit is derated to 20 % of maximum power.

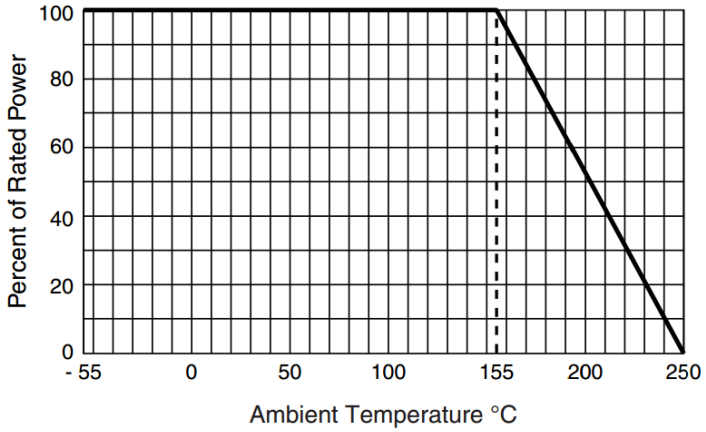


Fig. 3.4: Derating curve for Vishay thin film resistor [34].

The PCB board used for the design is Rogers 3010. The glass transition temperature of the board material is greater than 280 °C [39], which is sufficiently high to ensure structural integrity at our operating temperature. The variation of ε_r with temperature is less than 1%, which suggests stable microstrip characteristic impedances across temperature. Rogers offers other board materials which have better thermal properties than the selected (RO 3010) board. For example, the coefficient of thermal conductivity of 3010 material is 0.95 W/m/K which is higher than some of the other board materials provided by Rogers [39]. Moreover, a higher thermal coefficient of the relative dielectric constant (ε_r) compared to other boards suggests that the RO 3010 material will experience more variation in ε_r with temperature [39]. Despite these shortcomings, the RO 3010 board was chosen because of its high ε_r (11.2) [39]. This is to ensure compact microstrip lines at 97.5 MHz.

Indalloy 151 (92.5%Pb, 5%Sn, and 2.5%Ag) is used as the soldering material in the design. The melting point of this solder paste is 296 °C [40], which ensures reliable connections at the maximum operating temperature of the VGA.

3.2 Specifications

The specifications of the VGA were decided based on the downhole communication system it was designed for. The VGA is designed to operate at an IF frequency of 97.5 MHz. This frequency is obtained after downconverting the received RF signal centered at 243 MHz, using a local oscillator frequency of 340.5 MHz. The RF band of the downhole system is shown in Fig. 3.5.

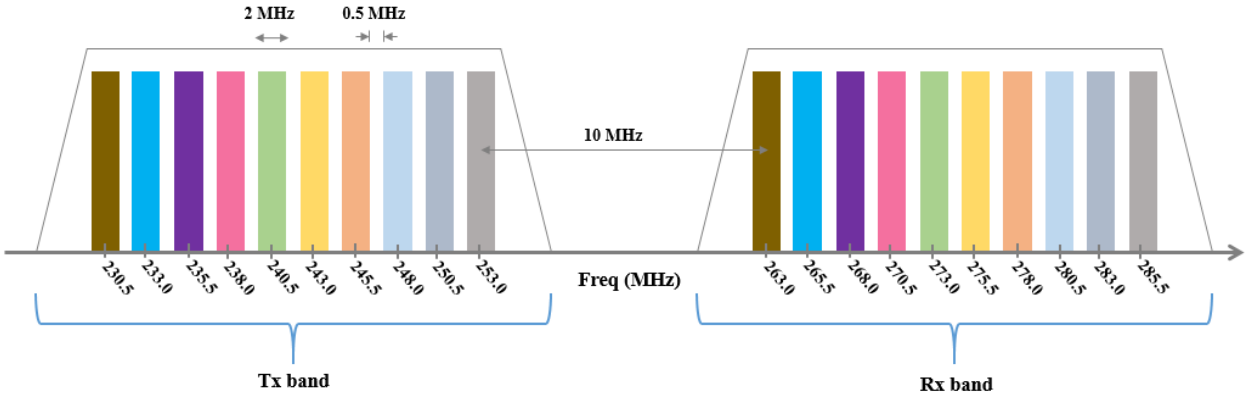


Fig. 3.5: Frequency allocation of RF bands in downhole communication system.

The 10 different channels in the RF bands represent the communication bands for each tool in the downhole system. These bands are 2 MHz wide, and separated from each other by 0.5 MHz. Each tool has an RF front end, and the proposed VGA is employed at the end of the RF chain. The entire front end comprises of an LNA, RF bandpass filter, mixer, VCO, IF filter, and the VGA. The specifications of the communication system determine the specifications of the individual components, which in turn, depend on each other. The block diagram of the downhole communication system RF modem is shown in Fig. 3.6.

It can be seen that the incoming signal power from the coaxial cable to the LNA varies due to the tools being placed at different lengths on the wireline cable. Attenuations in the ranges of 10 to 40 dB can be experienced. The receiver gain is about 10 dB, making the gain control requirement for the VGA to be 0 to 30 dB.

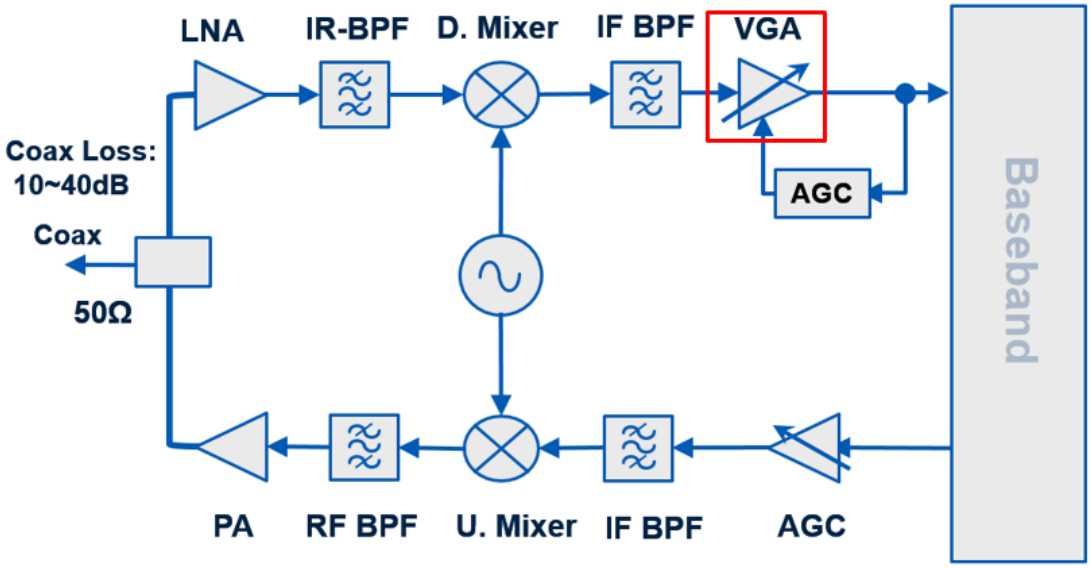


Fig. 3.6: Block diagram of RF front end of individual tools in downhole communication system.

Thus, the VGA is required to have a high gain control range so that a constant output power is provided to the analog-to-digital stage. Moreover, linearity of the VGA should be high enough to avoid distorting the high power signals in tools close to the surface. The VGA should also be sensitive enough to provide good amplification for low power signals in tools further down the coaxial cable. The specifications of the VGA are shown in table 3.2.

TABLE 3.2: DESIGN SPECIFICATIONS FOR THE VGA

Parameter	Specification
Frequency	97.5 MHz
Operating temperature	25 – 230 °C
Gain	30 – 0 dB
Gain control range	30 dB
Input return loss	≥ 10 dB
Output return loss	≥ 10 dB
Input P1dB	≥ -5 dBm

3.2.1 Calculation of Power Dissipation Limit

As mentioned in chapter 2, in order to calculate the power dissipation limit of the circuit, a thermal analysis of the PCB board needs to be performed. Simple calculations involving the

thermal resistances from the transistor junction to the ambient environment can give a good estimate of the maximum power dissipation limit of the design. As mentioned earlier, the transistor has a $\theta_{JC} = 12.4$ °C/W and T_J = 275 °C. Fig. 3.7 shows the dimensions of the transistor as shown in the datasheet [34].

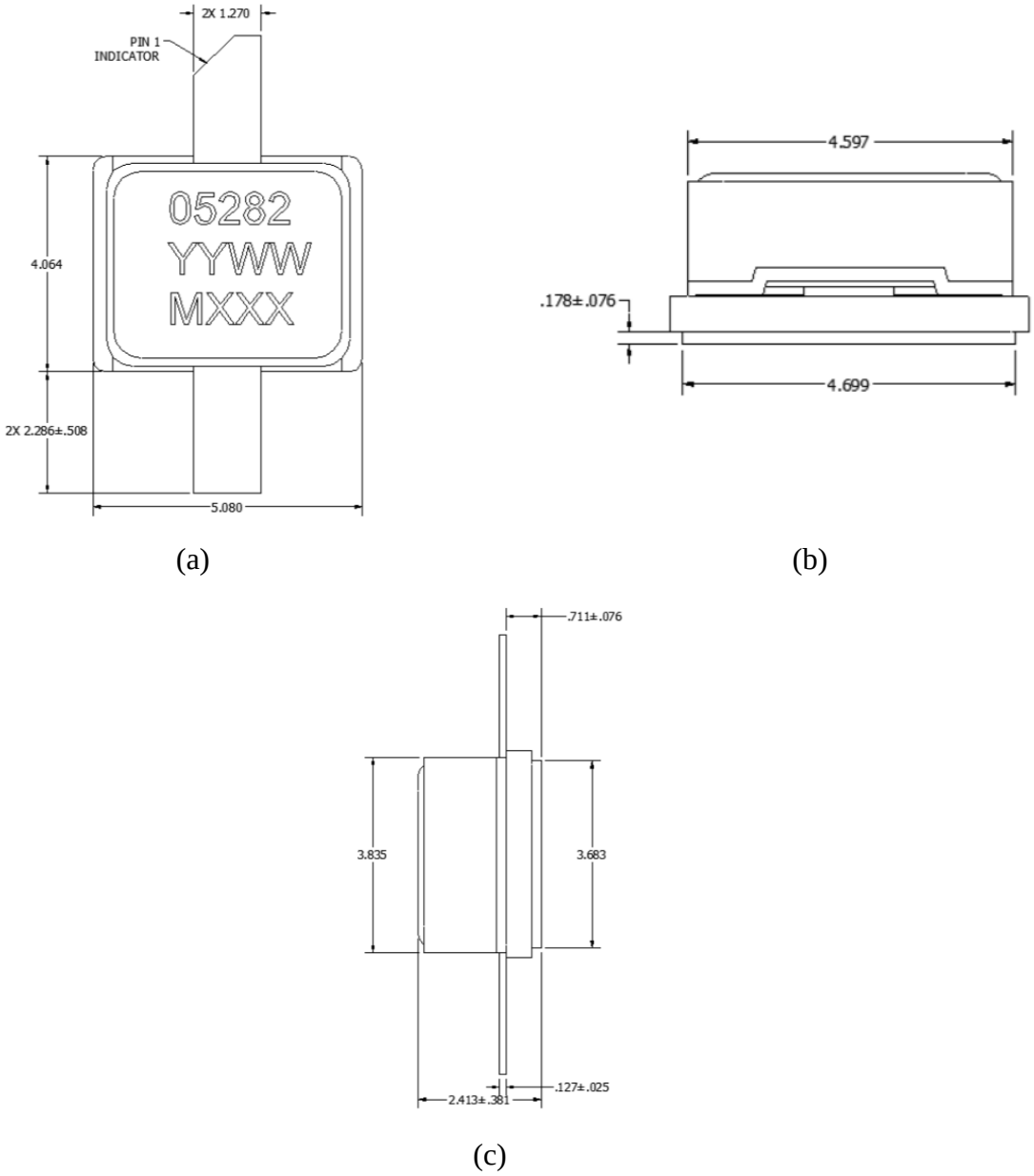
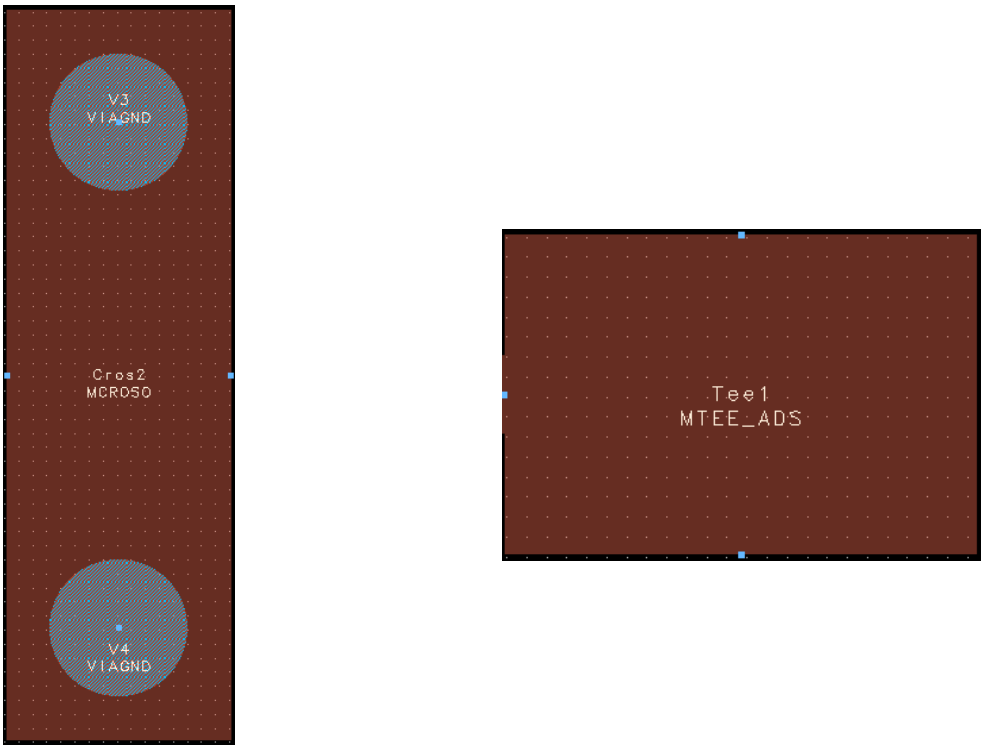


Fig. 3.7: (a) Top view, (b) side view, and (c) frontal view dimensions of Qorvo T2G6000528-Q3 [34].

Fig. 3.8 (a) shows the layout pad for a transistor with source connected to ground through vias (screws). Fig. 3.8 (b) shows the layout pad for a transistor whose source is not connected to

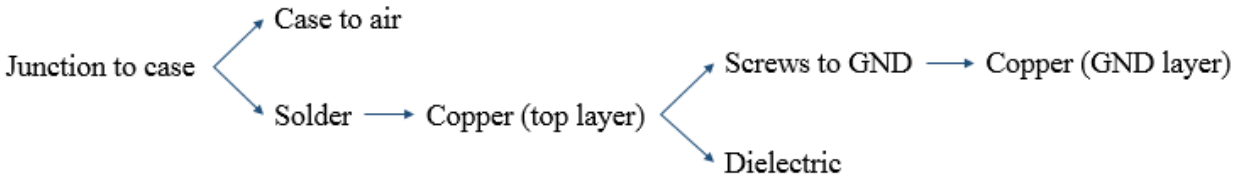
ground. These layouts will help in determining the heat flow paths from the transistor case to ambient on each of these pad configurations.



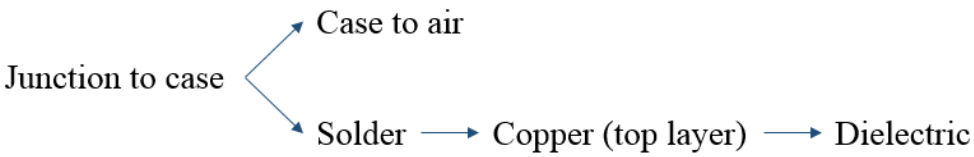
(a) (b)

Fig. 3.8: Layout pads for transistors with source (a) connected to ground (b) not connected to ground.

In Fig. 3.8 (a), V3 and V4 represent vias, which will be implemented as screws. The transistor will be soldered on the copper pad between the screws. The layout in Fig. 3.8 (b) represents a copper pad on which the transistor will be soldered. From these layouts, we can see that the layout in configuration (a) has more pad area and more thermally conductive components on the pad (screws). The heat flow pattern for this layout is:



The heat flow for layout in configuration (b) is shown below. This layout will be the dominating factor in deciding the power dissipation limit due to a lack of thermally conductive components, as seen below:



From this heat flow pattern, and using the thermal resistance and conductivity parameters of the components [34], [40]–[39] the thermal resistance representation shown in Fig. 3.9 can be obtained.

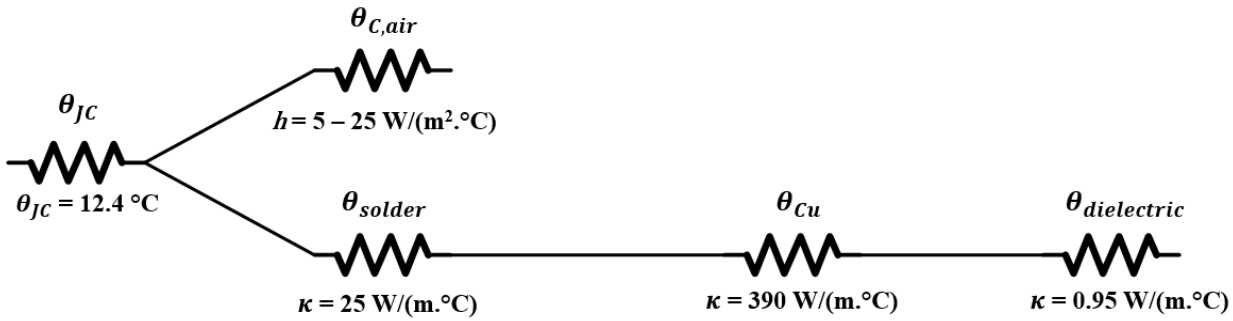


Fig. 3.9: Thermal resistance representation of the heat flow pattern for layout configuration in Fig. 3.4 (b)

The thermal resistances can be calculated from the pad and component dimensions from Fig. 3.7 and Fig. 3.8.

- Transistor plate soldered on the copper pad has dimensions 3.683mm x 4.699mm.
- Transistor case has 5 sides exposed to air (with the bottom side soldered on Cu pad), and the dimensions of the exposed sides are 4.597mm x 2.413mm, 3.835mm x 4.597mm, and 3.835mm x 2.413mm
- Thickness of copper on Rogers 3010 board is 35 µm and the thickness of the board dielectric is 1270 µm [39].
- Thickness of solder paste on copper pad is approximated to be 50 µm.

$$\theta_{solder} = \left(\frac{1}{25\ \frac{W}{m\cdot°C}}\right)\left(\frac{50\ \mu m}{3.683\ mm \text{ x } 4.699\ mm}\right) = 0.116\ °C/W \tag{3.1}$$

$$\theta_{Cu} = \left(\frac{1}{390\ \frac{W}{m\cdot°C}}\right)\left(\frac{4.699\ mm}{3.683\ \text{mm x } 35\ \mu m}\right) = 93.47\ °C/W \tag{3.2}$$

$$\theta_{dielectric} = \left(\frac{1}{0.95\ \frac{W}{m \cdot °C}}\right)\left(\frac{1.270\ mm}{3.683\ \text{mm x}\ 4.699\ mm}\right) = 103.36\ °C/W \tag{3.3}$$

Total surface area of the case exposed to air is

$$\begin{aligned} area_{case} &= 2[(4.597)(2.413) + (3.835)(2.413)] + (4.597)(3.835) \\ &= 58.32\ mm^2 \end{aligned} \tag{3.4}$$

$$\theta_{C,air} = \left(\frac{1}{25\ \frac{W}{m^2 \cdot °C}}\right)\left(\frac{1}{58.32\ mm^2}\right) = 686\ °C/W \tag{3.5}$$

The total thermal resistance from junction to ambient is then,

$$\begin{aligned} \theta_{JA} &= \theta_{JC} + (\theta_{C,air} \| (\theta_{solder} + \theta_{Cu} + \theta_{dielectric})) \\ &= 12.4 + (686 \| (0.116 + 93.47 + 103.36)) \\ &= 165.5\ °C/W \end{aligned} \tag{3.6}$$

The power dissipation limit can be calculated as

$$P_D = \frac{T_J - T_A}{\theta_{JA}} = \frac{275 - 230}{153.02} = \mathbf{272\ mW} \tag{3.7}$$

3.3 Selection of Topology

The common source cascode topology (discussed in chapter 2) is chosen for the proposed VGA. The advantages of this topology are that power consumption can be minimized because there is only one current path. This is a critical design consideration because passive cooling techniques such as heatsinks are not feasible in compact downhole environments. The variable bias topology with a single transistor seems to have a better potential for a lower power dissipation; however, from the datasheet [34] of the selected device, it was determined that a single transistor may not provide the required 30 dB gain. Increasing the V_{GS} to try to push the transistor to achieve 30 dB of gain will cause the result in high power consumption. The cascode topology, on the other hand, has a high output resistance which results in high gain even at a low

V_{GS}. Thus, common source cascode topology can provide a high gain while consuming less DC power.

Secondly, the common source cascode topology consists of only two transistors, which minimizes the small/large signal performance variation with temperature. Another advantage is that due to the low input resistance of the CG load, the gain of the CS amplifier is low, reducing the miller effect. Thus, the topology provides good reverse isolation. Another implication is that simultaneously matching the input and output is easier, and changes with respect to temperature in input impedance will not have a considerable impact on output impedance, and vice versa.

A drawback of this topology is that the linearity of the cascode topology depends significantly on the non-linearity of the CG stage [42]. Fig. 3.10 shows the small signal model of the cascode amplifier.

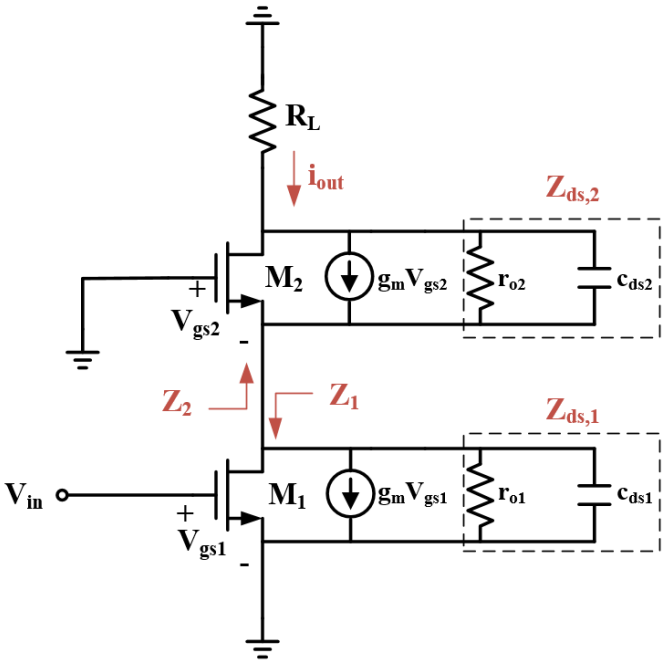


Fig. 3.10: Small signal model of cascode topology.

The drain current of CS stage, $g_{m1}V_{gs1}$ (referred as i_{d1} below), is supplied to the CG stage. The gate source voltage of the common gate stage, V_{gs2} can be expressed as

$$V_{gs2} = [Z_1||Z_2](g_{m1}V_{gs1}) \cong Z_2(i_{d1}) \tag{3.8}$$

The impedance Z_2 dominates the effective impedance because it is much smaller than the output impedance Z_1 of the CS stage. Z_2 can be expressed as

$$Z_2 = (Z_{ds,2} + R_L) \,||\, \frac{1}{g_{m2}} \tag{3.9}$$

The drain current of the CG stage in terms of its gate source voltage V_{gs2} is (approximated to third order power series)

$$\begin{aligned} i_{out} &= g_{m2,1}V_{gs2} + g_{m2,2}V_{gs2}^2 + g_{m2,3}V_{gs2}^3 + \cdots \\ &= g_{m2,1}Z_2 i_{d1} + g_{m2,2}Z_2^2 i_{d1}^2 + g_{m2,3}Z_2^3 i_{d1}^3 + \cdots \end{aligned} \tag{3.10}$$

From 2.47, it is clear that as R_L increases, the impedance Z_2 also increases, which in turn increases the nonlinear currents as can be seen in 2.48. Thus, if the output impedance $Z_{ds,2}$ is not high enough to block the non-linear currents from leaking to the output, then linearity of the design will be affected by the CG stage [42]. Nevertheless, the topology was selected because GaN is inherently highly linear.

3.4 Final VGA Schematic

The schematic of the high temperature VGA is shown in Fig. 3.11.

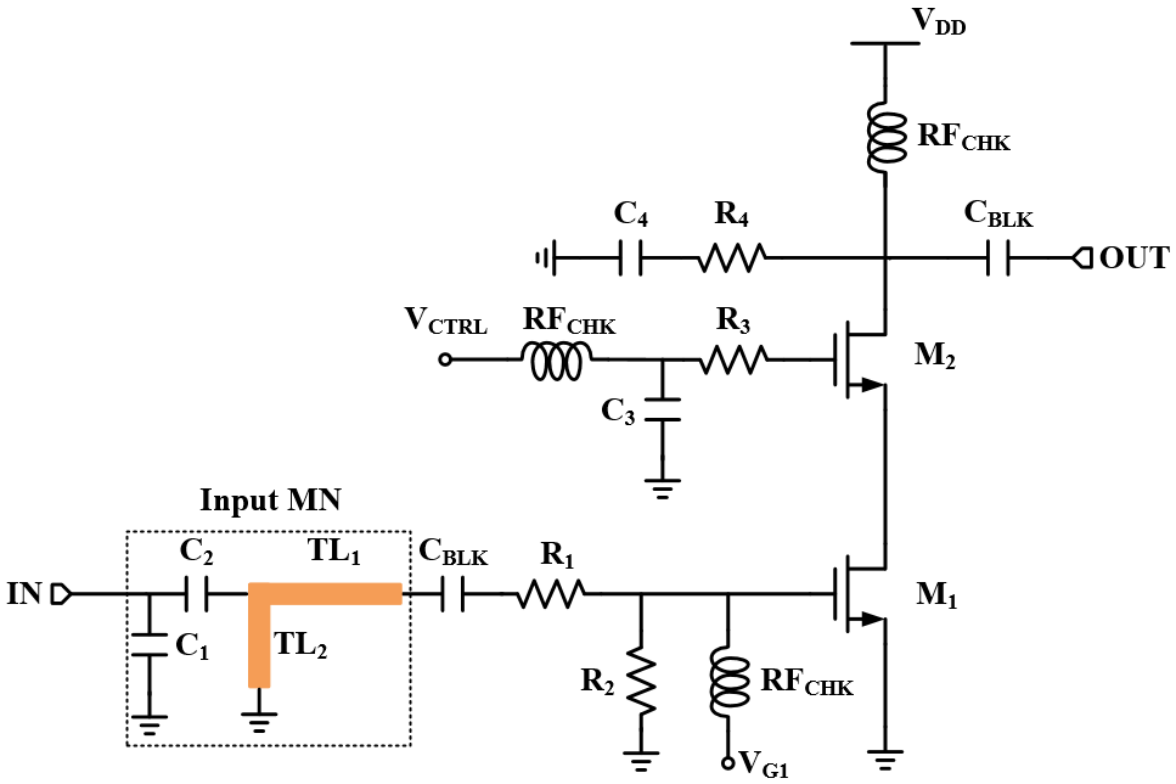


Fig. 3.11: Schematic of the proposed VGA.

In the above figure, the RF input is provided to the gate of M_1 through an input matching network consisting, a short stub TL_2, and transmission line TL_1. Capacitors C_1 and C_2 were added after initial measurements to compensate for the slight deviation in matching network response from the simulated response. The DC blocking capacitor C_{BLK} separates gate bias V_{G1} from the RF input. V_{G1} is supplied using an RF choke (RF_{CHK}). The control voltage is provided using an RF choke. Resistor R_3 is for stability, and bypass capacitor C_3 provides AC ground. R_4 and C_4 are for stability. The supply V_{DD} is provided using a bias tee. Table 3.3 provides the list of parts used in the design, and their values.

TABLE 3.3: LIST OF COMPONENTS IN THE VGA SCHEMATIC

Circuit Element	**Manufacturer**	**Value**
C_1	Presidio	20 pF (10 pF + 10 pF)
C_2	Presidio	112 pF (56 pF+ 56 pF)
C_3	IPDiA	1 µF
C_4	Presidio	90 pF (68 pF +22 pF)
R_1	Vishay	20 Ω (10 Ω +10 Ω)
R_2	Vishay	4.99 k Ω
R_3	Vishay	50 Ω
R_4	Vishay	70 Ω (50 Ω +10 Ω +10 Ω)
C_{BLK}	IPDiA	1 µF
RF_{CHK}	Coilcraft	1 µH

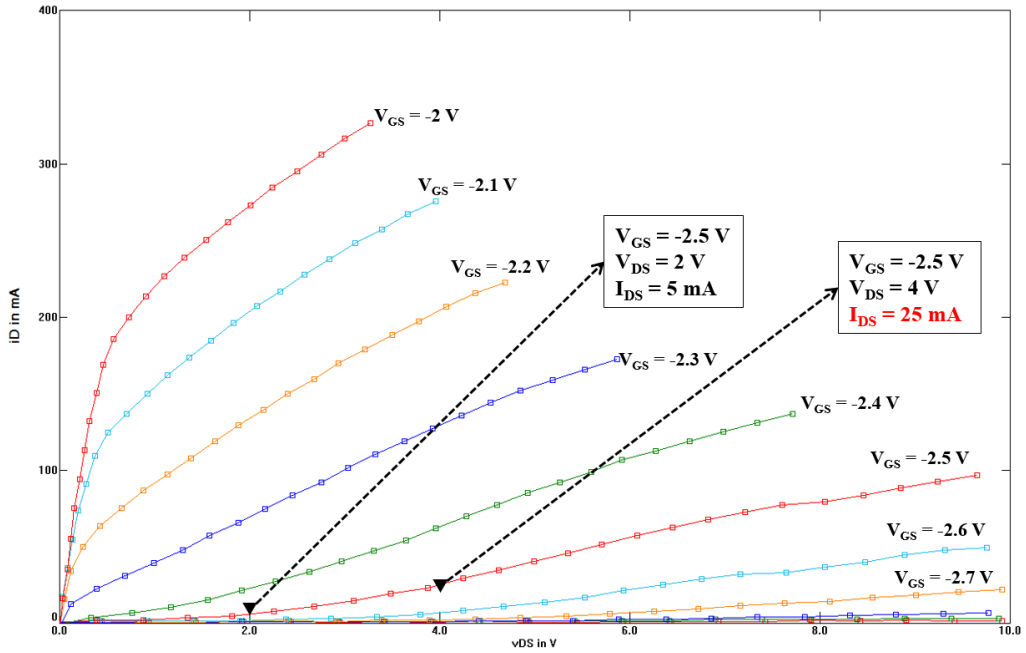
3.5 Circuit Design

This section will describe bias point selection, bias network design, stability network design, and matching network design of the VGA.

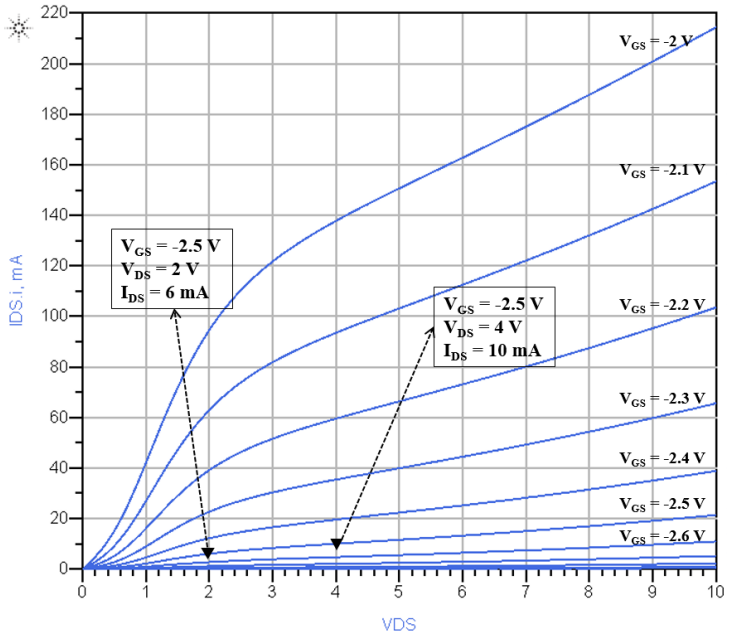
3.5.1 Bias Point Selection

The two main factors driving the bias point selection of the device are power dissipation limit and the operating region of the transistors. Bias point also determines how some large and small signal parameters, such as drain current, g_m, etc. vary with temperature. Since the VGA is to be used at 230 °C, the I-V curves obtained from simulation of the transistor up to 85 °C are not

enough to predict the drain currents at 230 °C. Therefore, I-V measurements were taken to accurately determine the DC behavior of the HEMT at 230 °C. Measurements were taken at both room temperature, and at different temperatures up to 230 °C. The measurements were taken on a curve tracer for a single transistor that was soldered on a test board. It was found that even at room temperature, the simulation results from ADS did not match the measured I-V curves. This can be seen in Fig. 3.12 which compares the curve tracer measurements with the ADS simulation result at 25 °C, and discrepancies can be clearly seen, especially at higher drain and gate voltages. The figure shows two points on the same trace (at V_{GS} = -2.5V), and it can be seen that the measured drain current value in Fig. 3.12 (a) at V_{DS} = 4 V is much higher than the simulated value in Fig. 3.11 (b). Thus, I-V curves are measured for the GaN device from 25 °C to 230 °C in order to accurately determine the drain currents and saturation region of the HEMT across the entire operating temperature range.



(a)



(b)

Fig. 3.12: I-V curves of the transistor (a) Measured (b) Simulated [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon].

The maximum power dissipation specification is 272 mW, as estimated in section 3.2.1. The bias point is selected such that the power dissipation limit is satisfied, and the variation in gain is low with respect to variation in temperature. This is important to ensure that the design exhibits the same gain and dynamic range across the entire operating temperature range. As derived in the previous chapter, the gain of cascode configuration is:

$$-g_{m1}[R_L||(g_{m2}r_{o1}r_{o2})]$$

Gain heavily depends on g_m, which is affected by temperature (as discussed in section 2.2.1.7). To achieve a constant gain at both room and high temperatures, M_1 is biased near the transconductance zero-temperature coefficient (GZTC) bias point, which refers to the bias point where g_m is independent of temperature. The GZTC point is determined as the intersection point of measured g_m versus V_{GS} curves at temperatures from 25 °C to 230 °C, as shown in Fig. 3.13.

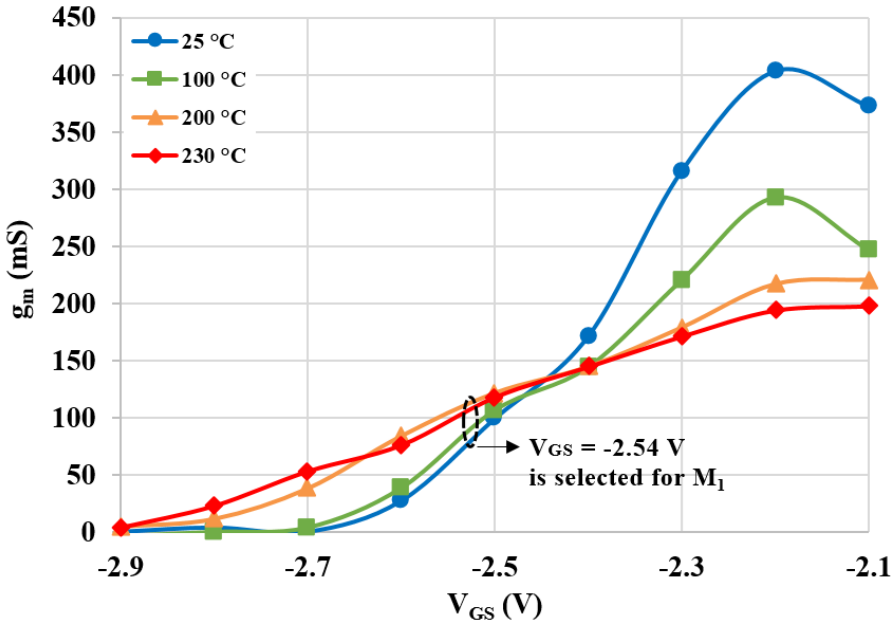


Fig. 3.13: Measured transconductance versus gate bias voltage at different temperatures.

It is observed from Fig. 3.13 that GZTC lies at approximately -2.45 V. However, from the measured I-V curves at 230 °C (Fig. 3.14), this bias point is found to exceed the power dissipation limit at 230 °C, at drain voltages ≥ 4 V. Although V_{GS} values close to -2.45 V could be selected since they show relatively less g_m variation, the power dissipation is very close to the estimated limit. Fig. 3.13 shows the power dissipation limit (272 mW) for gate bias voltages from -2.3 V to -2.6 V, and drain voltages from 2 V to 6 V.

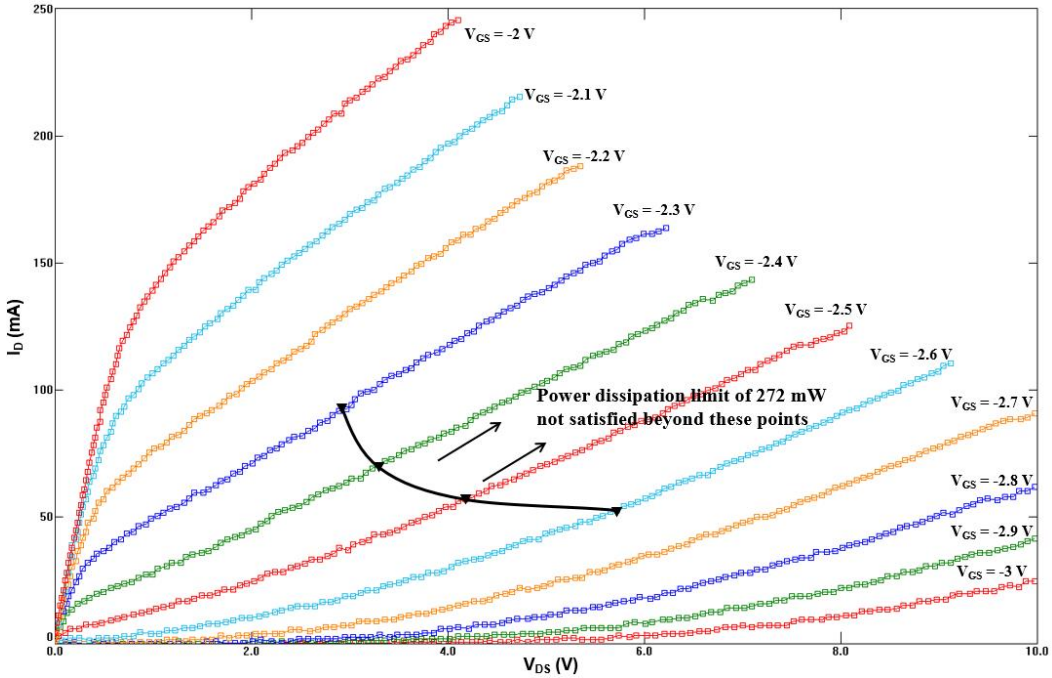


Fig. 3.14: Measured I-V curves of the transistor at 230 °C.

The calculation of the power dissipation limit was a simplified one dimensional estimation of heat flow, and biasing very close to it could be detrimental to the design due to self-heating issues in MOSFET, which were not considered in analysis due to complexity. Therefore, the bias point of V_{GS} = -2.54 V was selected for CS MOSFET M_1. This point is well within the power dissipation limit and shows relatively less g_m variation with temperature. The supply voltage V_{DD} is 4 V to ensure that V_{DS} of transistors is high enough to operate in saturation region. The drain current I_D is 17 mA at 25 °C, and 44 mA at 230 °C. The power consumption for maximum gain at 230 °C is 176 mW. The gate voltage of M_2 is the gain control voltage (V_{CTRL}) of the circuit. V_{CTRL} ranges from -0.1 V to -3.2 V, with -0.1 V providing the highest gain, and -3.2 V providing the lowest gain.

3.5.2 Bias Network Design

Bias voltage are supplied using integrated bias tees, which consist of a DC blocking capacitor and an RF choke. The capacitor and inductor values used in bias tee were 1 µF and 1 µH, respectively. A cause of concern is that large capacitors and inductors may have low self-resonant frequencies, which may fall within the operating frequency range. The self-resonant frequency of the inductor is 350 MHz [37], which is outside the operation band. The self-

resonant frequency of the capacitor can be estimated from its parasitic inductance (ESL) information from the datasheet. The datasheet suggests that the ESL is 1 nH [37].

$$SRF = \frac{1}{2\pi\sqrt{ESL * C}} = \frac{1}{2\pi\sqrt{(1nH)(1\mu F)}} = 5\ MHz \tag{3.11}$$

The capacitor will perform its DC blocking capabilities, but at the operation frequency, may attenuate signals because it behaves like an inductor beyond its self-resonant frequency. The "inductance" of the capacitor at 97.5 MHz is

$$X_c = \omega * \text{ESL} = 2\pi(97.5\ MHz)(1nH) = 0.6\ \Omega \tag{3.12}$$

This value is small enough to not cause attenuation of RF signals. The bias tees are employed at the gate of M_1 and drain of M_2. At the gate of M_2, the RF choke is used to feed the control voltage, and the 1 µF capacitor is used as bypass to provide AC ground to the CG transistor.

3.5.3 S-parameter model

The s-parameter model is available in the device model provided by Modelithics [33], but the characterization is done at V_{DS} = 28 V and I_{DS} = 50 mA and 150 mA. Since the DC simulation in ADS was found to be different from measured results, the s-parameter simulation was also done to accurately predict the response of the GaN HEMT. The simulated response of the transistor at V_{DS} = 4 V and I_{DS} = 16 mA is shown in Fig. 3.15.

Due to the discrepancy between measured and simulated models, the measured s-parameter model was incorporated in simulation, and the stability circuits, bias networks, and matching networks were designed around it. S-parameters were measured at both 25 °C and 230 °C, and the model at 230 °C was used to design the VGA circuit because that is the target temperature for the application.

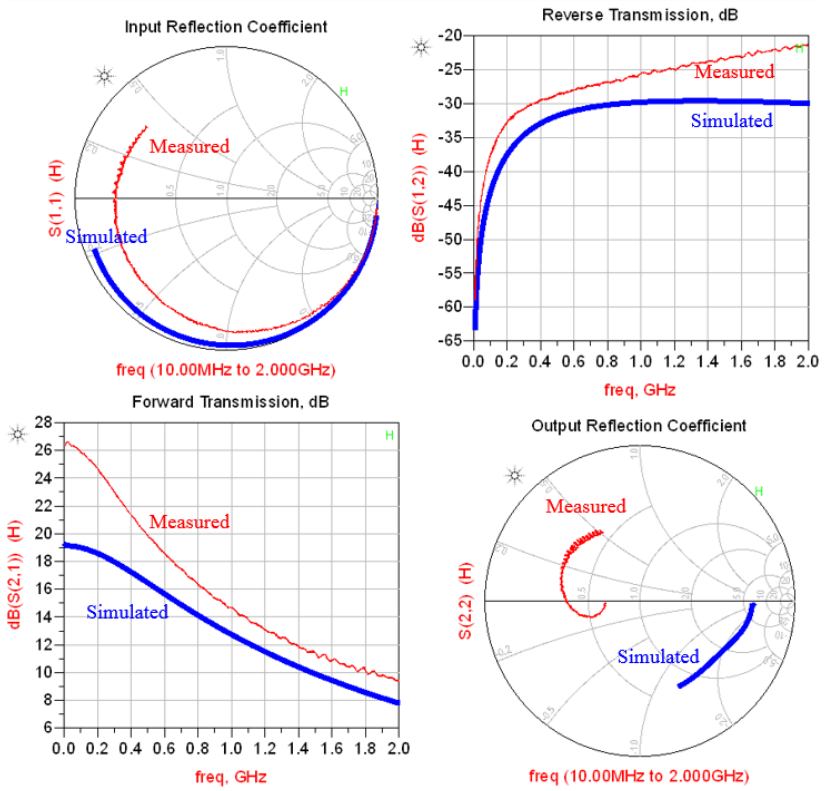


Fig. 3.15: Measured and simulated s-parameters of the transistor at 25 °C (V_{DS} = 4 V, I_{DS} = 16 mA) [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon].

3.5.4 Stability

The selected GaN transistor was found to be inherently unstable. Fig. 3.16 shows the simulated μ stability parameters with 50 Ω source and load impedances, at I_{DS} = 16 mA and V_{DS} = 4 V.

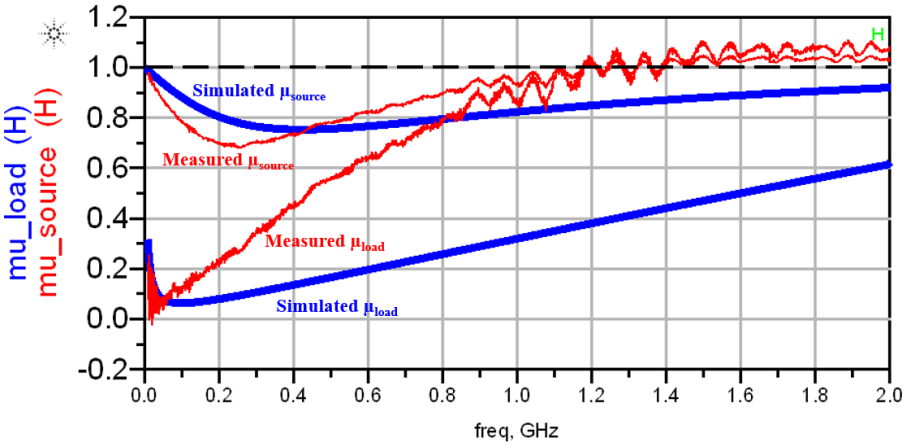


Fig. 3.16: Simulated and measured μ parameters of the transistor at 25 °C (V_{DS} = 4 V, I_{DS} = 16 mA) [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon].

The above simulation and measurement plot is for a single transistor. The cascode configuration required using multiple stability networks both at the input and output to make the VGA unconditionally stable. The measured s-parameter model at 230 °C was used to design the stability circuit in ADS, and stability was verified in simulation at both 25 °C and 230 °C to ensure stable operation across the entire temperature range.

Stabilizing resistors were added to ensure unconditional stability, while sacrificing noise performance. Since the VGA is in the IF stage of the downhole communication receiver, its noise contribution is minimal in the cascaded noise figure. In order to improve stability, series and shunt resistors $R_1 = 20\ \Omega$ and $R_2 = 4.99\ k\Omega$ are employed at the input. The RC series network of $R_4 = 70\ \Omega$ and $C_4 = 90$ pF is employed at the output to decrease gain and improve stability at higher frequencies outside the operation band. A cause of concern for cascode amplifiers is that the input impedance looking in to the gate of the cascode device (M_2) can have a negative real part, which can be calculated below. In order to calculate this impedance, the common source transistor M_1 can be represented as a parallel combination of a resistor (R_p) and capacitor (C_p), as shown in Fig. 3.17.

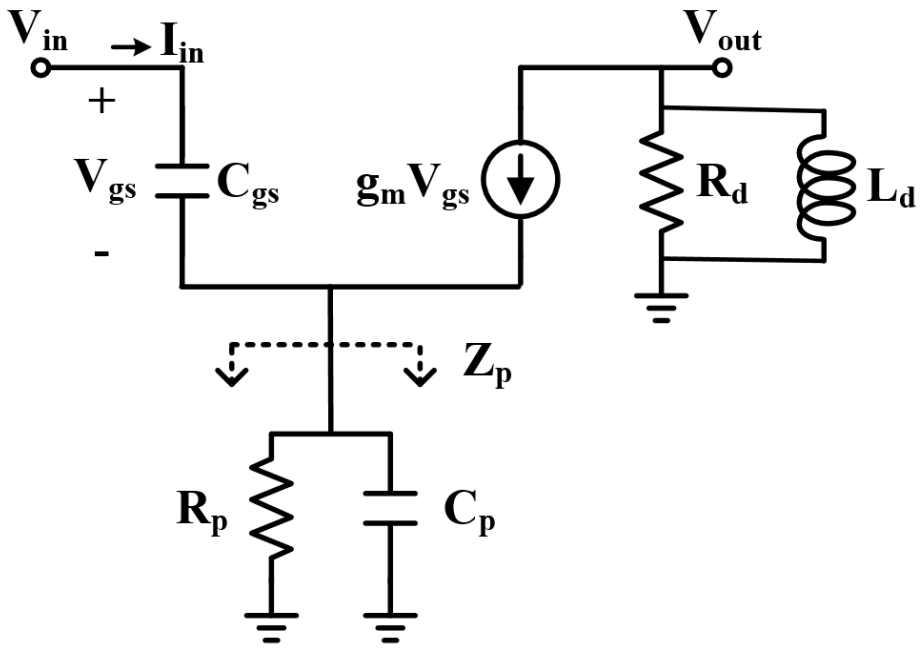


Fig. 3.17: Input impedance seen at the gate of the cascode transistor.

$$V_{in} = I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m V_{gs})Z_p = I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m \frac{I_{in}}{C_{gs}})Z_p \quad (3.13)$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{sC_{gs}} + Z_p\left(1 + g_m \frac{1}{sC_{gs}}\right) \quad (3.14)$$

The real part of Z_{in} can be calculated to be [42]

$$R_{in} \cong \frac{R_p}{(R_p C_p \omega)^2 + 1} - \frac{g_m R_p^2 C_p \omega^2 C_{gs}}{(R_p C_p C_{gs} \omega^2)^2 + (C_{gs}\omega)^2} \quad (3.15)$$

The negative resistance makes this node prone to oscillation if there is a parasitic inductance present at the gate of the cascode device. Adding a resistance will lower the Q of this oscillation, thereby increasing stability [43]. A 50 Ω resistor at the gate of M_2 improved the stability factor considerably in simulation; resistor R_3 = 50 Ω is added at the gate of M_2, and bypass capacitor C_3 provides AC ground.

The stability analysis and design of stability networks was performed in the highest gain setting because it is most prone to instability. As gain decreases, stability generally increases. μ factor also verified in simulation for other control voltages. At high temperature, the stability is expected to improve because of decrease in gain (g_m decreases with temperature).

3.5.5 Matching Network

Both input and output ports need to be matched to 50 Ω. Microstrip transmission lines are used to match the input port to 50 Ω. The main reason for using microstrip lines is that they offer negligible temperature variations compared to inductors and capacitors. The input and output impedances before matching are shown below.

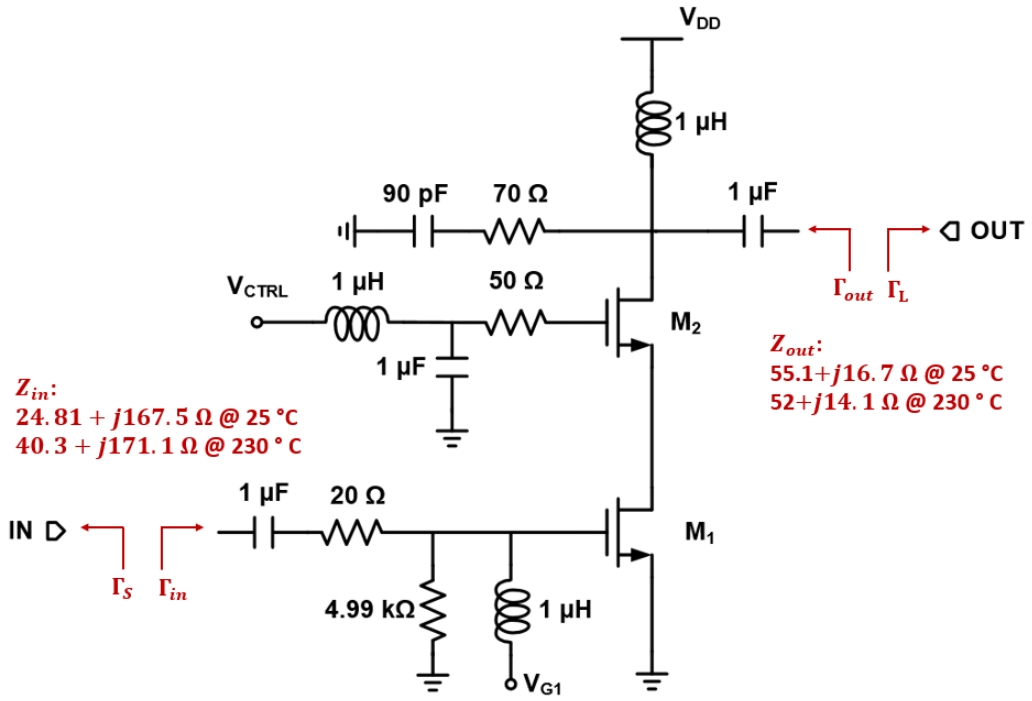


Fig. 3.18: Measured input and output impedances at 230 °C before matching (V_{G1} = -2.54 V, V_{CTRL} = -0.1V, and V_{DD} = 4V).

Due to the presence of 70 Ω resistor at the drain, the effective output impedance is close to 50 Ω, and no output matching is required. The input is conjugate matched for maximum gain (V_{CTRL} = -0.1 V) at 230 °C. As seen in Fig. 3.19, a transmission line TL_1 (17.78 cm) with short stub TL_2 (4.57 cm) make the input impedance match to 50 Ω at 97.5 MHz in simulation.

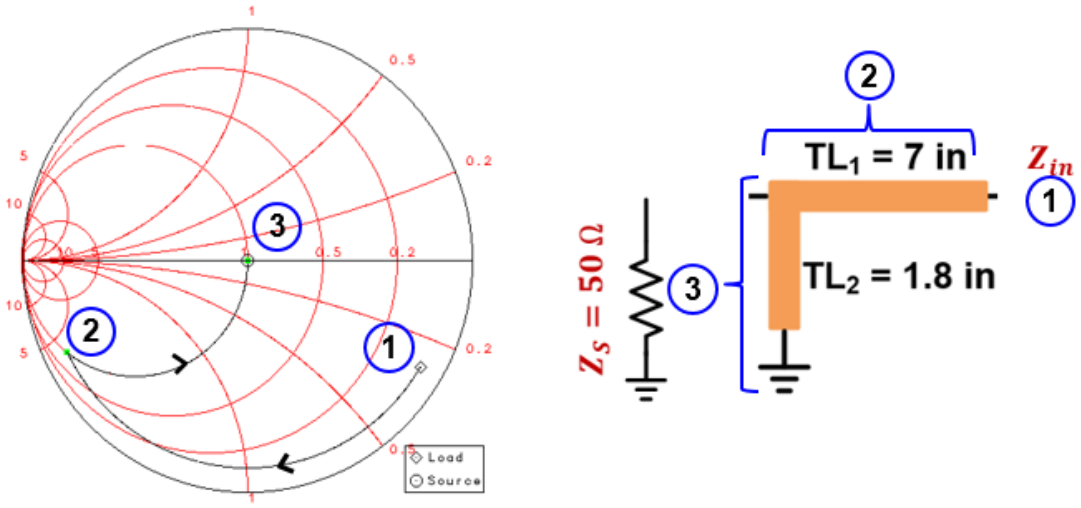
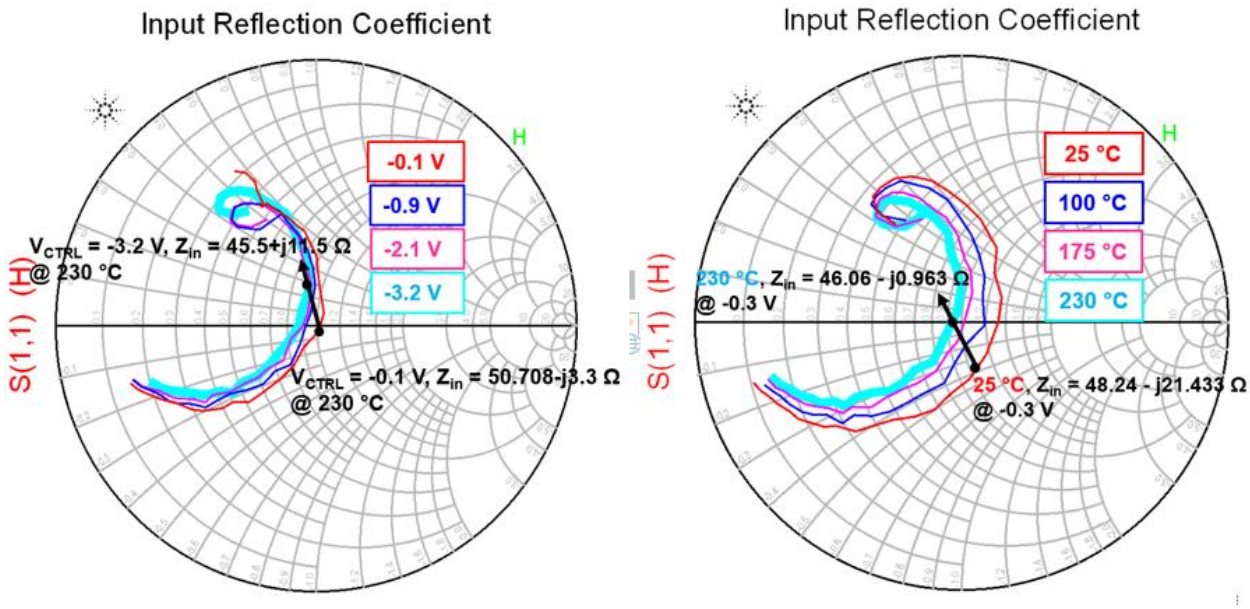


Fig. 3.19: Design of input matching network at 230 °C for maximum gain setting (V_{G1} = -2.54 V, V_{CTRL} = -0.1V, and V_{DD} = 4V).

For the matching network to work for all control voltages and across the entire operating temperature range, the variation in the matched input and output impedance of the circuit with respect to control voltage and temperature was determined. The simulated matching network results are shown in Fig. 3.20.



(a) (b)

Fig. 3.20: Variation of simulated input matching network at center frequency of 97.5 MHz (a) with respect to V_{CTRL} (b) with respect to temperature [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon].

From these variations, it can be seen that the worst case deviation of matched input impedance is within 10 % of 50 Ω. Thus, the designed matching network should give a good input return loss for all control voltages and all temperatures.

Chapter 4

4 Measurement

In this chapter the measurement setup and test procedures will be discussed, followed by the measurement results.

4.1 Measurement Setup

This section will describe the measurement setup for the various tests performed on the VGA. Both room temperature and high temperature test setups will be described. A Rohde and Schwarz (R&S) ZVA67 network analyzer is used to measure s-parameters and 1 dB compression of the circuit. The noise figure is measured using HP E4411B spectrum analyzer, and Agilent 346C noise source. The measurement procedures and setups will be further elaborated upon below.

4.1.1 S-parameters

The R&S ZVA67 was used to measure the s-parameters and 1 dB compression of the circuit. The instrument is a 4 port network analyzer. However, for our purposes, it is used in 2 port mode with port 1 being the input, and port 2 being the output port. The ports are 50 Ω and can both transmit and receive signals. The frequency range of this instrument is from 10 MHz to 67 GHz [44].

4.1.1.1 VNA Calibration

In order to measure s-parameters, the VNA ports should be calibrated to remove the effect of all the connectors and components until the desired measurement plane. For example, in order to measure s-parameters to characterize a single transistor or a passive component, all components until the component junction have to be calibrated out of the measurement. Thus, cables, connectors, and the microstrip line on the PCB from the SMA connector to the component junction should be calibrated out. A basic TOSM (thru, open, short, and match) calibration routine is performed to calibrate the cables and connectors out of the measurement. To de-embed

the transmission line on the board, the “port extension” feature on the VNA is used, where the length of the line to be de-embedded is entered along with the effective relative permittivity and loss of the substrate. This information is used by the VNA to calibrate the transmission lines out of the measurement.

4.1.1.2 Test Setup

Voltage bias for the VGA is provided using a Rigol DP832A Programmable Power Supply. Port 1 of the VNA is connected to the VGA input, and port 2 to the output. The VGA input power level is typically set to -20 dBm to measure active devices. The VNA datasheet was checked to make sure that the output power level from the VGA is well within the linearity specification of the VNA receiver.

To perform the s-parameter test at high temperatures, the VGA board is placed inside a Yamato natural convection drying furnace, which has provisions for inserting cables. The board is connected to the lab bench equipment (DC supplies, VNA) using special high temperature cables and SMA connectors. The test setup is shown below.

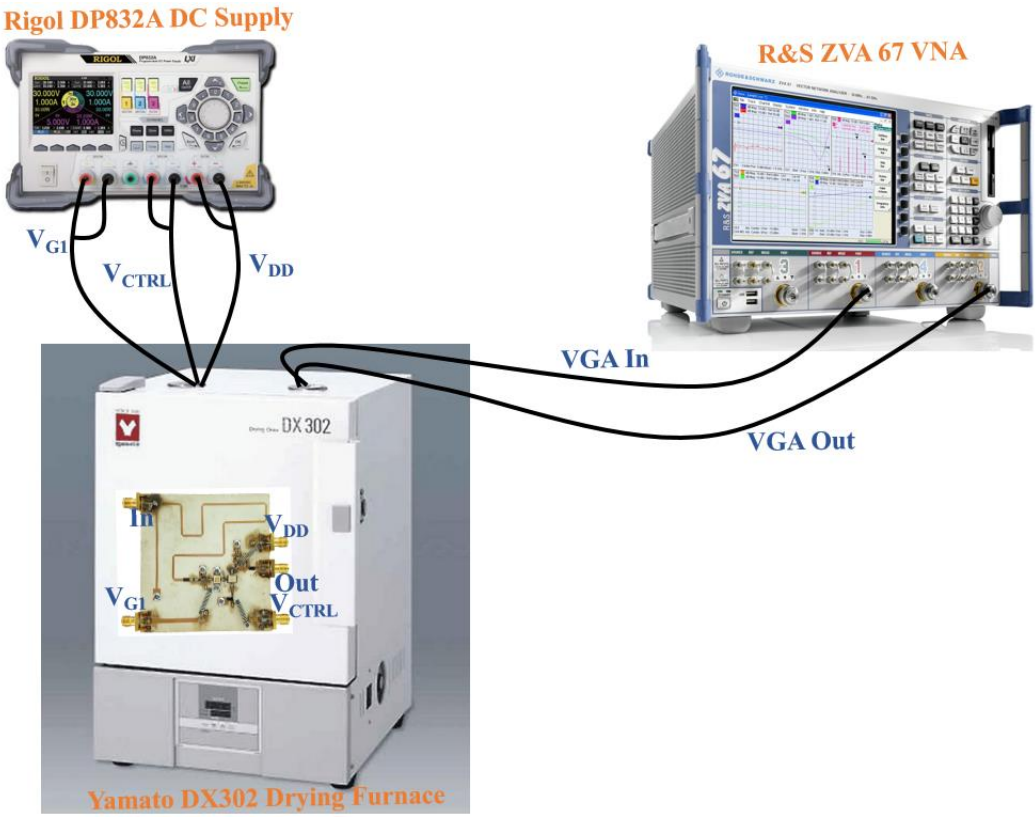


Fig. 4.1: Test setup for high temperature s-parameter measurement [44]-[46].

4.1.2 1 dB Compression

In order to measure the 1 dB compression of the circuit, the VNA is calibrated and a power sweep measurement is selected. The frequency of the input CW tone is set in the power sweep menu, along with the input power sweep range. The VGA sweeps the input power at port 1 (set as input port) and measures the output power at port 2 (set as output port) and plots gain versus input power. From this plot, the 1 dB compression of the circuit can be seen.

For this measurement, it is important to know the linearity specification of the VNA receiver, both for the safety of the VNA and the measurement accuracy. Attenuation should be added before the VNA output if the output power level from the VNA is close to the compression specification of the VNA. The test setup is similar to the s-parameter measurement.

4.1.2 Noise Figure

A few common methods for measuring the noise figure of a device are the gain method, the Y factor method, and noise figure analyzer (NFA) method. Selection of measurement method depends on the application of the circuit. The noise figure analyzer method is an accurate method for measuring very low (sub 3 dB) noise figures. The error is large when measuring relatively high noise figures. The gain method is an easy way to measure noise figure of high gain circuits, but is only favored for measuring very high noise figures. This method is also limited by the noise floor of the spectrum analyzer which is used in the measurement. The Y factor method is suitable for a wide range of noise figure, and is chosen for measuring the NF of the VGA circuit. The Y factor method involves the usage of a spectrum analyzer, and a noise source.

4.1.2.1 Spectrum Analyzer

Spectrum analyzers are very useful to look the fundamental signal spectrum, harmonics, and intermodulation products. They can also measure the noise spectral density for a specified bandwidth. Functions such as resolution bandwidth, averaging, span, and video bandwidth can be changed according to the signal for more accurate measurements. The HP E4411B spectrum analyzer, along with the Keysight (formerly Agilent) 346C noise source was used in measuring noise figure for the proposed VGA.

4.1.2.2 Noise Source

A noise source is used to product an output noise power when a DC voltage is provided to it (powered ON). The Keysight 346C noise source requires a +28 V DC input [47]. When the instrument is powered OFF, there is still thermal noise in the noise source. The difference in noise levels when the instrument is powered ON and OFF is used to measure the gain and added noise of the circuit under test [47]. Noise sources are characterized by a parameter called excess noise ratio (ENR), at many frequencies within the operation frequency range. ENR refers to the ratio between the power ON noise power, to the noise power at 290 K (17 °C). This parameter will be used in NF calculations.

4.1.2.3 Test Setup and Calculations

The test setup is as follows. The noise source is connected to a DC supply that can provide a +28 V input. The output of the noise source is connected to the input of the VGA. Bias ports of the VGA are connected to a power supply. The VGA output goes to a spectrum analyzer input to measure the noise power density. Spectrum analyzer settings are adjusted to get an accurate measurement. Averaging is turned ON, and the resolution/video bandwidths of the instrument are adjusted to achieve an accurate measurement. For high temperature measurement, the VGA is placed in the thermal furnace and high temperature cables are used to connect to the VGA ports. Fig. 4.2 shows the test setup at high temperature.

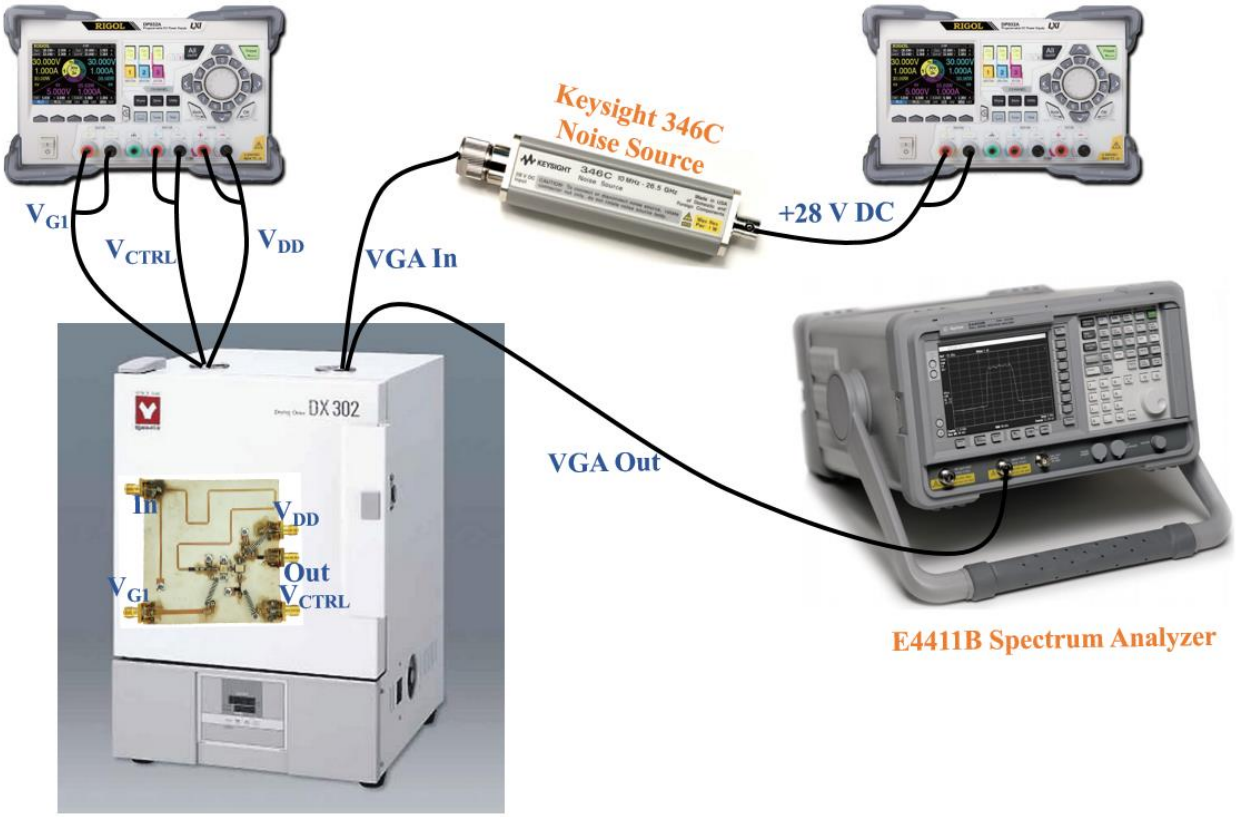


Fig. 4.2: Test setup for high temperature NF measurement [44]-[47], [49].

When the test setup shown above is achieved, the noise figure is calculated as follows [48].

$$NF = 10 * log\left(\frac{10^{\frac{ENR}{10}}}{10^{\left(\frac{Y}{10}\right)-1}}\right) \tag{4.1}$$

Where Y is the change in output noise power density (measured at spectrum analyzer) when the noise source is turned ON from the state of being OFF. ENR value at the frequency of interest is obtained from the table provided by the instrument.

4.2 Measurement Results

This section presents measured results of s-parameters (gain, input/output return loss), 1 dB compression, and noise figure for the VGA at temperatures ranging from 25 °C to 230 °C, and compares the performance at 25 °C and 230 °C.

4.2.1 S-parameters

The s-parameter measurements give the gain, input matching, output matching, and stability performance of the VGA. At 25 °C, the VGA achieves a maximum gain of 28 dB at V_{CTRL} = -0.1 V, and a minimum gain of -6.23 dB at V_{CTRL} = -3.2 V, showing a dynamic range of 34.23 dB (see Fig. 4.3). Each gain step is achieved with a 0.1 V increment in V_{CTRL}. At 230 °C, the VGA gain ranges from 27 to -2.43 dB using the same V_{CTRL} range. The dynamic range is 29.43 dB. Fig. 4.4 shows the variable gain of the VGA at 230 °C. The 3 dB bandwidth is 13.3%. Fig. 4.5 shows the linear in dB control range of the VGA at room temperature and 230 °C. It can be seen that the linear gain control range is from -0.1 V to -2.5 V, with a peak deviation from ideal linear value of 6 % (at -2.5 V) at 25 °C and 4 % (at -2.5 V) at 230 °C.

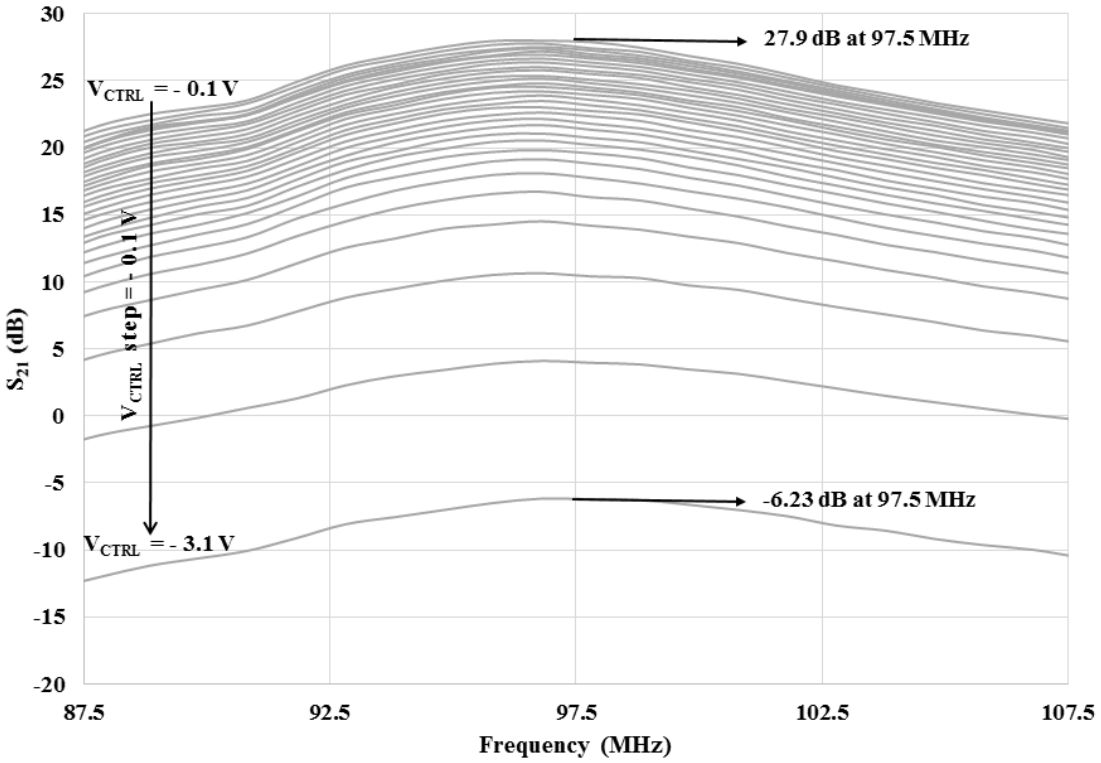


Fig. 4.3: Measured variable gain of the circuit at 25 °C, as V_{CTRL} is swept from -0.1 V to -3.2 V with 0.1 V decrements.

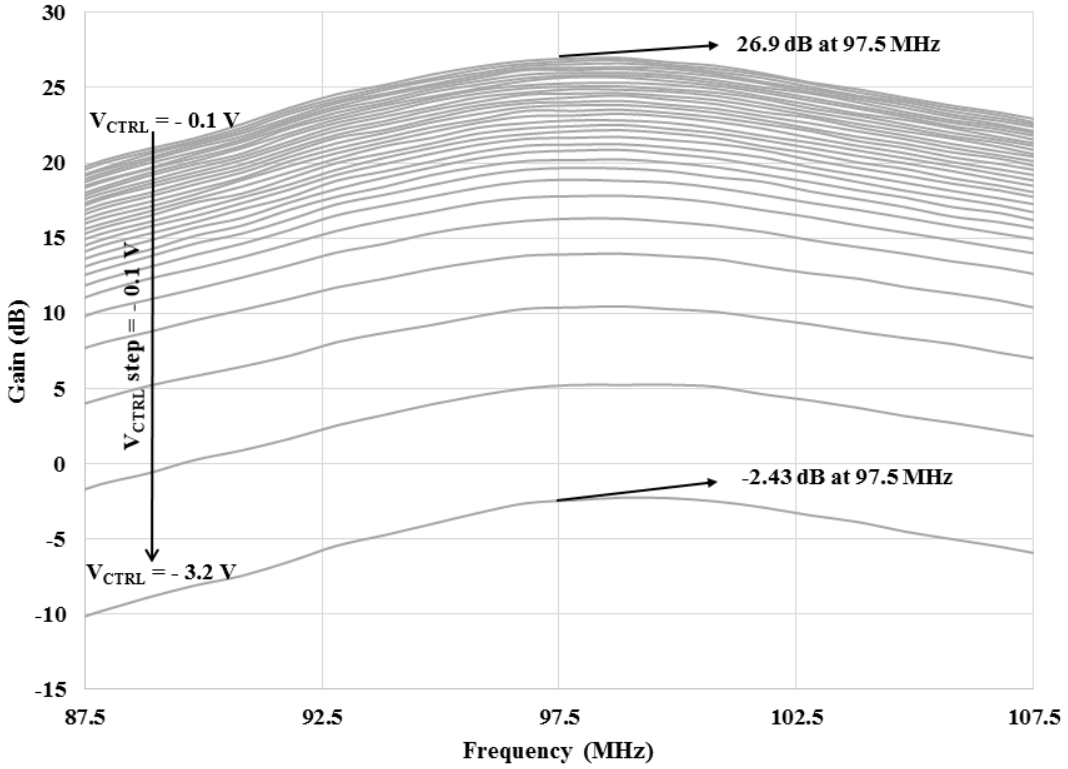


Fig. 4.4: Measured variable gain of the circuit at 230 °C, as V_{CTRL} is swept from -0.1 V to -3.2 V with 0.1 V decrements.

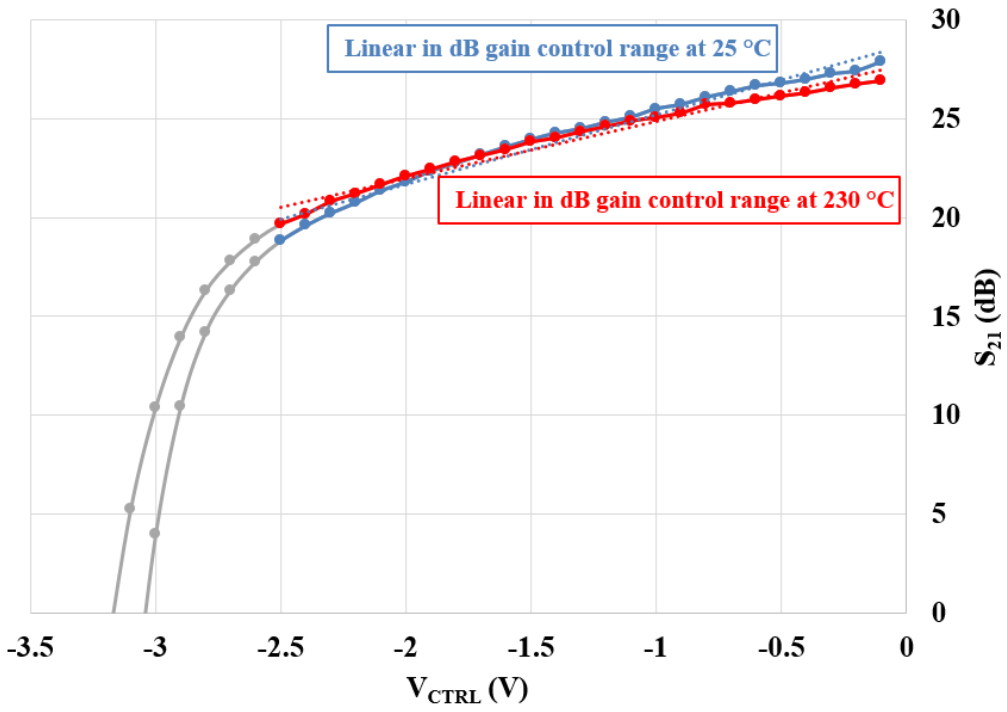


Fig. 4.5: Measured linear in dB gain control range at 25 °C and 230 °C.

Fig. 4.6 – 4.8 show the variation with temperature of s-parameters at 97.5 MHz, as the control voltage is swept across its full range. From Fig. 4.6, the variation in maximum gain (at V_{CTRL} = -0.1 V) from 25 °C to 230 °C is only 1 dB and this small variation is due to the fact that the transistor M_1 is biased near to GZTC. The maximum variation in gain across temperature is 6 dB, and occurs at -2.5 V. This variation could be minimized with adaptive biasing. The VGA achieves very good input and output matching at all control voltages and temperatures. The input and output return losses for the highest gain (V_{CTRL} = -0.1 V) at 230 °C are S_{11} = -26.37 dB and S_{22} = -12.4 dB. Both S_{11} and S_{22} for the design are below -12.3 dB -12 dB, respectively, across all gain settings and temperatures as can be seen in Fig. 4.7 and Fig. 4.8.

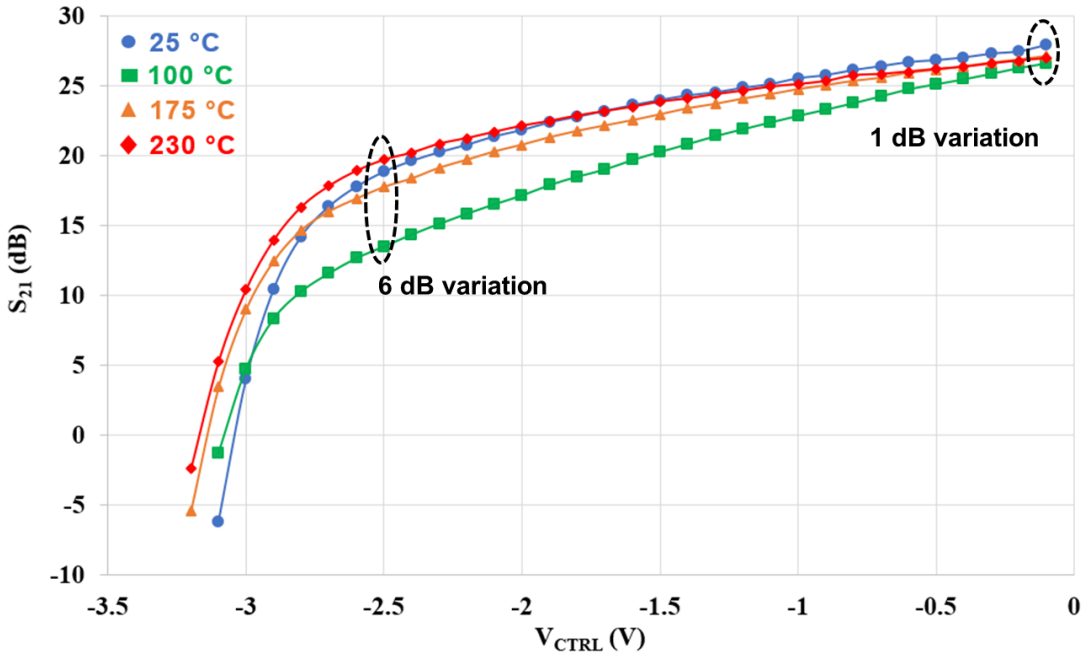


Fig. 4.6: Measured S_{21} at 97.5 MHz, at different control voltages from 25 °C to 230 °C.

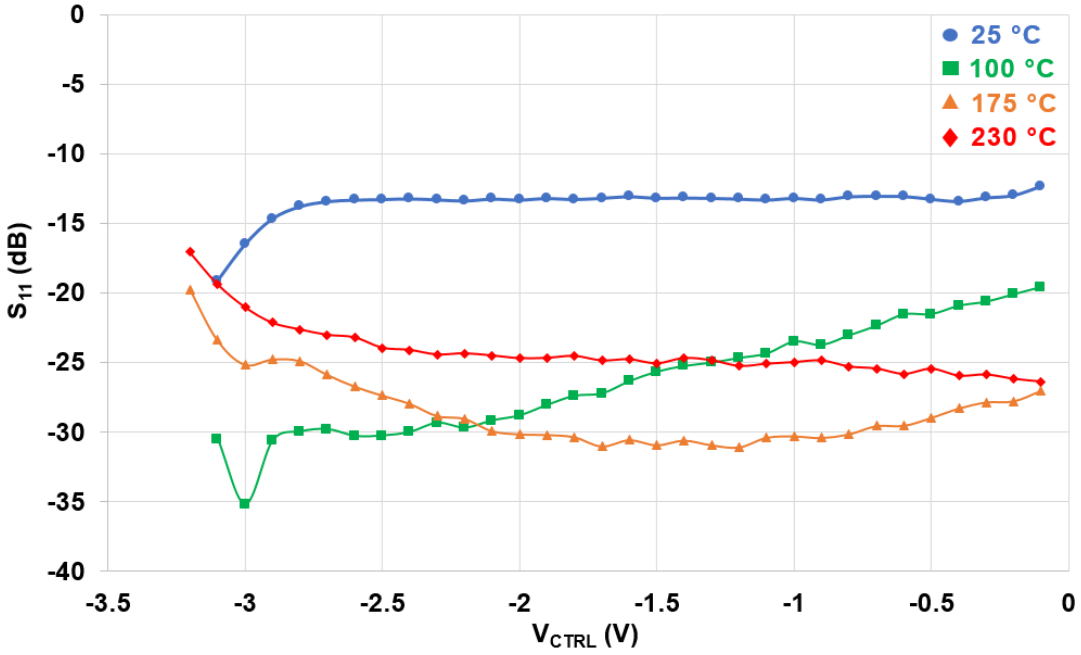


Fig. 4.7: Measured S_{11} at 97.5 MHz, at different control voltages from 25 °C to 230 °C.

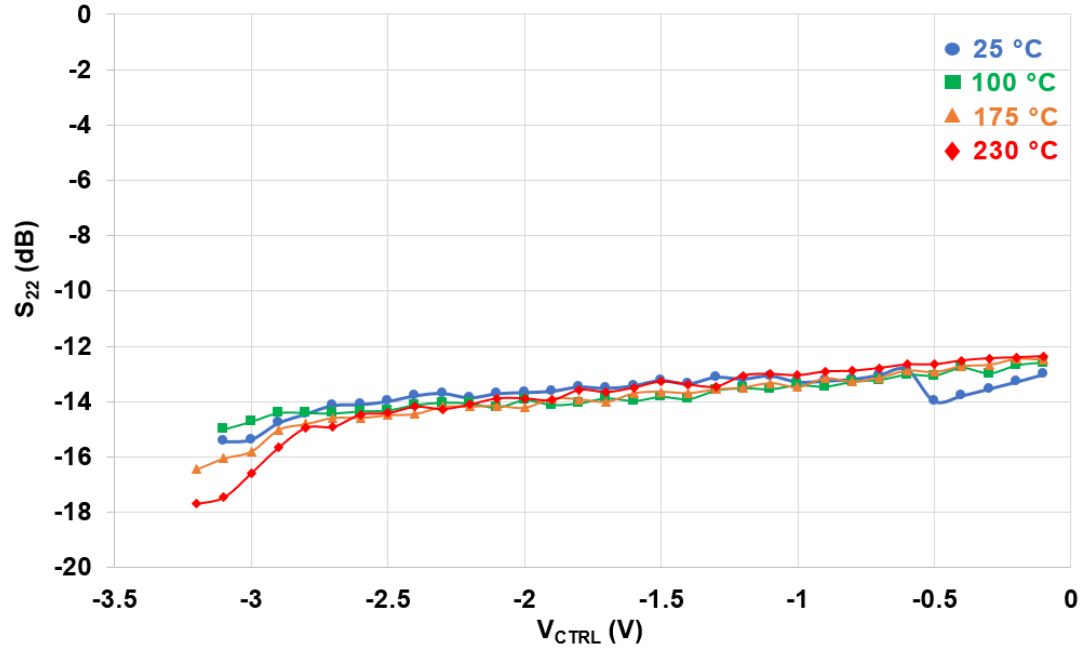


Fig. 4.8: Measured S_{22} at 97.5 MHz, at different control voltages from 25 °C to 230 °C.

4.2.2 Stability

Stability is a very critical design consideration. Stability of the VGA is verified using u stability factor for the VGA. μ factors are calculated from the measured s-parameters in ADS, and will hence be referred to as measured μ factors. Stability is measured for a wide frequency range in order to make sure that any undesired oscillations at higher frequencies do not affect the performance at the frequency of operation. Fig. 4.7 shows the measured μ_{source} and μ_{load} factors at 230 C and maximum gain. It can be seen that the VGA is unconditionally stable in the operating frequency range. A wide frequency range stability measurement was also performed (see Fig. 4.8). The VGA is conditionally stable near low frequencies and unconditionally stable in operating frequency range and at high frequencies. Although the VGA is conditionally stable (μ ≈ 0.9) at a few points at low frequencies (< 60 MHz), it is not very concerning because of very low gain at those frequencies (due to a narrow bandwidth matching network). Stability is verified at all other gain settings, and as expected, the VGA was found to be more stable at lower gain settings.

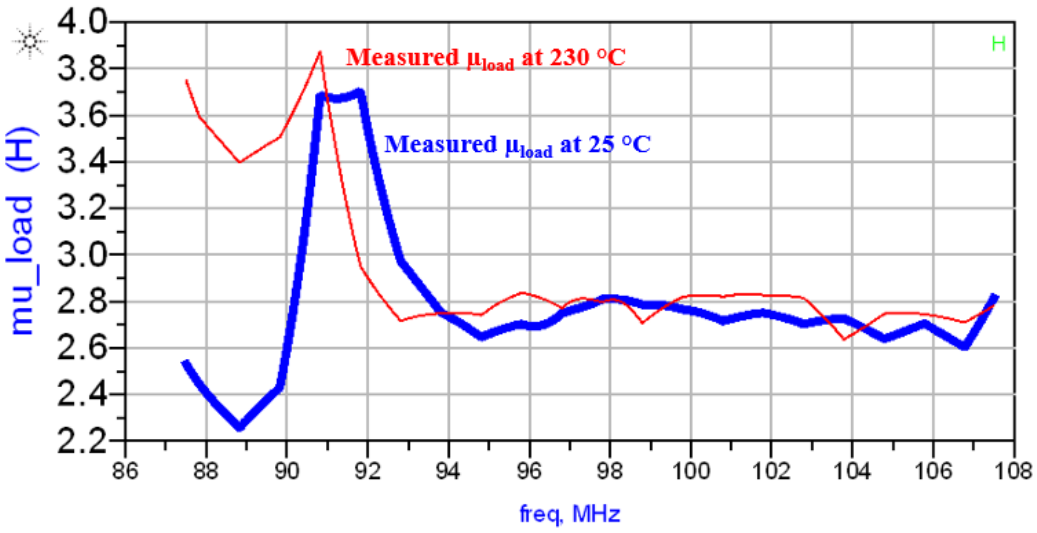


Fig. 4.9: Measured μ_{load} of the VGA circuit at 25 °C and 230 °C (V_{GS} = -2.54 V, V_{CTRL} = -0.1V, and V_{DD} = 4V) [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon].

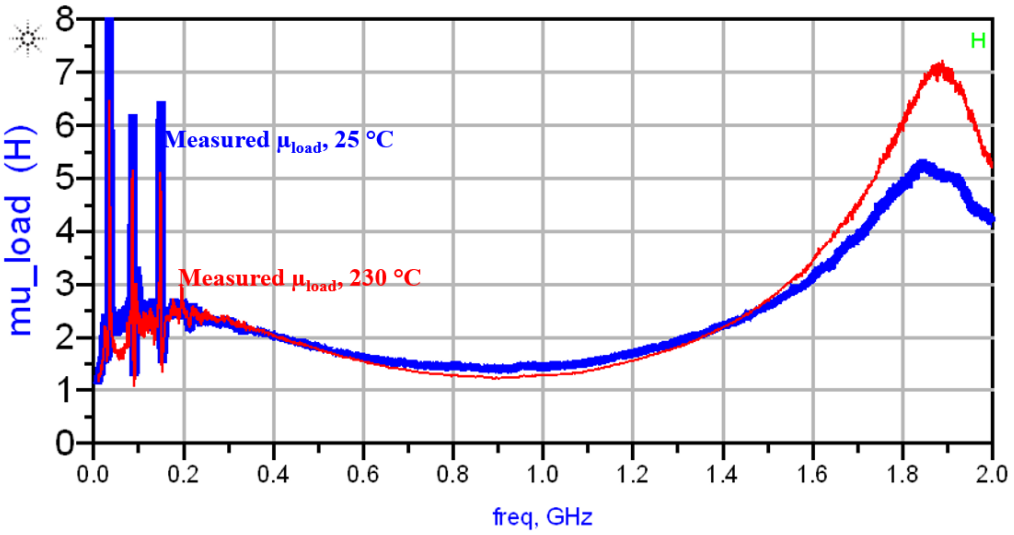


Fig. 4.10: Measured μ_{load} of the VGA circuit at 25 °C and 230 °C for a wide frequency range (V_{GS} = -2.54 V, V_{CTRL} = -0.1V, and V_{DD} = 4V) [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon].

4.2.3 1 dB Compression

The 1 dB compression test is performed to test the linearity of the circuit. Since the VGA is in the end stage of the receiver, the linearity of the VGA, along with the mixer dominates the total linearity of the system. Fig. 4.9 shows the linearity performance plot at maximum gain setting, from 25 °C to 230 °C.

At 25 °C, the input P1dB of the VGA is -3.63 dBm at maximum gain (V_{CTRL} = -0.1 V). Using a 1 dB compressed gain of 25.82 dB, the output P1dB is 22.19 dBm at maximum gain.

At 230 °C, the input P1dB of the VGA is -10.92 dBm, at maximum gain (V_{CTRL} = -0.1 V). Using a 1 dB compressed gain of 25.82 dB, the output P1dB is estimated to be 14.9 dBm at maximum gain. The input P1dB at 230 °C for minimum gain (V_{CTRL} = -3.2 V) is -11.71 dBm. At 230 °C, the input P1dB does not meet the specification of ≥ 5 dBm. Ways to improve linearity are discussed in conclusion.

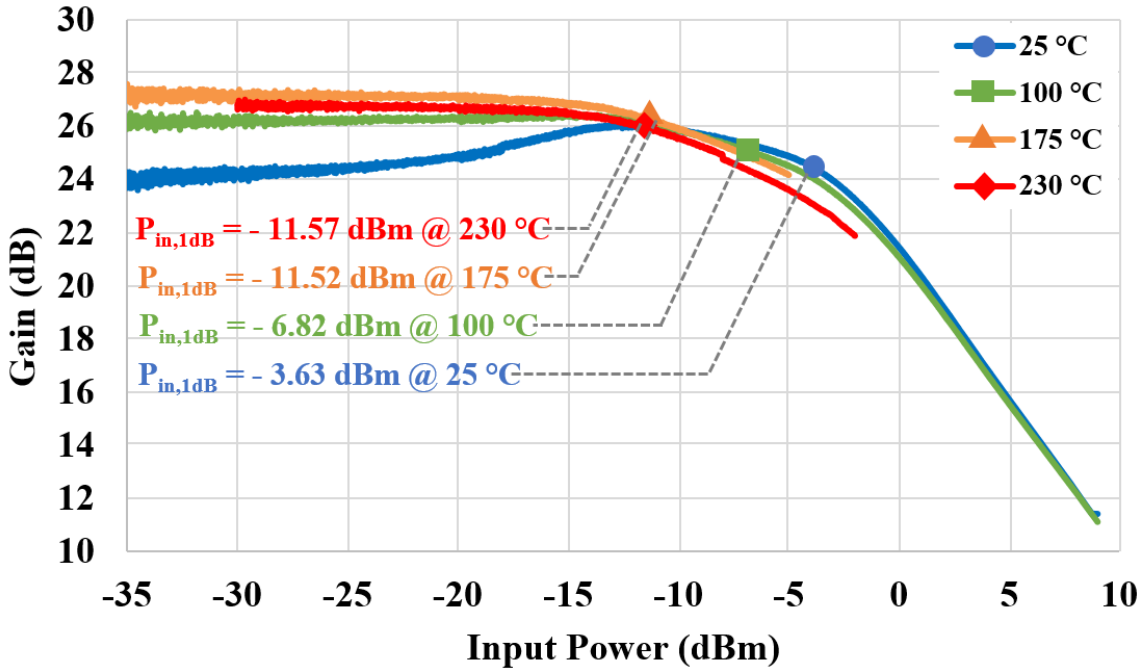


Fig. 4.11: Measured input P1dB of the VGA at maximum gain (V_{CTRL} = - 0.1 V) from 25 °C to 230 °C.

4.2.4 Noise Figure

Since the VGA is in the end of the signal chain, the noise contribution from it is minimized by the gain of components before it. Fig. 4.10 shows measured noise figure versus control voltage at temperatures from 25 °C to 230 °C. It can be seen that the NF ranges from 7.6 dB to 18 dB at 25 °C, and from 8.9 dB to 18.9 dB at 230 °C. The noise performance is reasonably good, considering that stabilizing resistors were added to make the inherently unstable transistor achieve unconditional stability.

It can be noted from Fig. 4.10 that for control voltages up to -2 V, the NFs at 175 °C and 230 °C are higher than the NFs at 25 °C and 100 °C, which is expected. As temperature increases, NF also increases. However, as the control voltage increases beyond -2 V, the NFs at 175 °C and 230 °C increase at a much slower rate than the NFs at 25 °C and 100 °C. At control voltages beyond -2.75 V, the NFs at 175 °C and 230 °C are lower than NFs at 25 °C and 100 °C. This is because as temperature increases, threshold voltage of the transistor is lowered, causing the transistor to remain in active mode for much lower values of control voltages. This can be verified from the S_{21} versus control voltage plot in Fig. 4.6. Thus, at control voltages close to the cut-off region, the gain at 175 °C and 230 °C is higher than the gain at 25 °C and 100 °C. As

gain increases, signal power at output also increases. Most of the noise sources remain constant, resulting in a higher signal to noise ratio (SNR) and hence, lower NF.

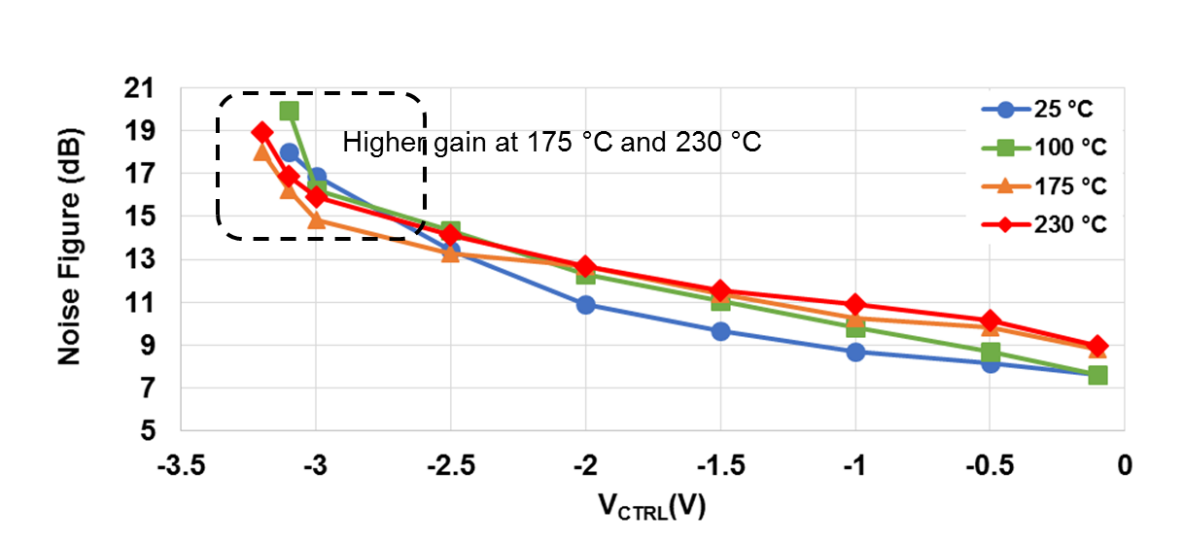


Fig. 4.12: Measured NF of the VGA at 97.5 MHz at different control voltages from 25 °C to 230 °C.

4.2.5 Summary of Results

Table 4.1 presents a summary of results at 25 °C and 230 °C.

TABLE 4.1: SUMMARY OF RESULTS

Parameter	**Spec**	**Result**	
Frequency (MHz)	96.5 – 98.5	96.5 – 98.5	
Temperature (°C)	**25 – 230**	**25**	**230**
Gain (dB)	30 to 0	28 to -6.23	27 to -2.43
Input P1dB (dBm)	≥ 5	-3.63	-11.57
Noise Figure (dB)	-	7.63 to 18	9 to 18.89
Input Return Loss (dB)	≥ 10	12.3 to 19.1	17 to 26.4
Output Return Loss (dB)	≥ 10	13 to 15.4	12.4 to 17.7
µ-factor	> 1	> 2.6	> 2.6
Power Consumption (mW)	-	16 to 68	16 to 176

Chapter 5

5 Conclusion

The design of a high temperature GaN based VGA, capable of operating from 25 °C to 230 °C is presented in this thesis. The VGA uses a cascode topology which utilizes only two transistors to minimize power consumption, and is able to operate at 230 °C without active or passive cooling techniques. The VGA achieves a high peak gain of 27 dB, and a gain control range of 29.4 dB at 230 °C. The minimum variation in gain across all temperatures is 1 dB and maximum variation is 6 dB. Input and output remain well matched with both IRL and ORL being > 12 at all gain settings from 25 °C to 230 °C. Furthermore, the VGA shows good linearity and noise performance at 230 °C. The proposed VGA is a proof of concept for high temperature circuits in GaN, and capable of operating in downhole communication systems. At the time of this writing, this is the first VGA to be reported that is capable of operating up to 230 °C, while showing good linearity and noise performance.

5.1 Future Work

From the design standpoint, improvement in linearity (1 dB compression) of the circuit is possible. Modifications to the cascode topology such as adding a resistor at the source of the common source transistor could help improve the linearity and stability at the cost of reduction in gain. Alternatively, a different topology could be implemented altogether. A source degeneration topology which offers higher linearity could be implemented with a variable resistor at the source (can be implemented using voltage controlled MOSFET in triode region).

The second and a more optimum way to extract the best performance from the circuit is to use adaptive biasing. Variations with respect to temperature can be minimized further using adaptive biasing or compensation schemes.

Implementation in IC will make the design more compact and give designers added control over transistor size (W, L) for optimum design. This is hard to achieve with discrete components. Moreover, more complex topologies with temperature compensation or adaptive biasing schemes can be implemented.

The fabrication and use of GaN technology is still in its nascent stages. As fabrication technology advances, fully integrated high temperature RF circuits are very realizable and have a tremendous potential for widespread use not just in downhole communications, but also other extreme environment applications such as monitoring automobile/aircraft engines, satellite communications, and space exploration.

References

[1] Watson, Jeff, and Gustavo Castro. "A Review of High-temperature Electronics Technology and Applications." *Journal of Materials Science: Materials in Electronics* 26.12 (2015): 9226-235. Web. 12 Nov. 2016

[2] G. DeBruijn, C. Skeates, R. Greenaway, D. Harrison, M. Parris, S. James, et al. “High-pressure high-temperature technologies.” Oilfield Review [Downhole Systems], vol. 20, no. 3, pp. 46-60.

[3] Schlumberger, “Surface systems: Data delivery,” in wireline services catalog, ed. Houston, Texas: Schlumberger, pp. 12-13, 2015.

[4] J. D. Cressler and H. A. Mantooth, Eds. Extreme Environment Electronics, CRC Press, 2012.

[5] I. Khalil, A. Liero, M. Rudolph, R. Lossy and W. Heinrich, "GaN HEMT potential for low-noise highly linear RF applications," in *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 9, pp. 605-607, Sept. 2008.

[6] B. Razavi, “Basic concepts in RF design,” in *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2011, ch. 2, sec. 6, pp. 71-75.

[7] B. Razavi, " Basic concepts in RF design," in *RF microelectronics*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2011, ch. 2, sec. 2, pp. 14-35.

[8] M. L. Edwards and J. H. Sinsky, "A new criterion for linear 2-port stability using a single geometrically derived parameter," in *IEEE Trans. Microw. Theory Tech.* vol. 40, no. 12, pp. 2303-2311, Dec 1992.

[9] D. Pozar, "Microwave amplifier design," in *Microwave Engineering*, 4th ed. Hoboken, NJ: Wiley, 2012, ch. 12, sec. 3, pp. 571-582.

[10] D. Wolpert and P. Ampadu, “Temperature Effects in Semiconductors,” in Managing Temperature Effects in Nanoscale Adaptive Systems, Rochester, NY: Springer, 2011, ch. 2, pp. 14-31.

[11] I. M. Filanovsky and A. Allam, “Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits,” in *IEEE Trans. Circuits and Syst. I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876-884, Jul 2001.

[12] M. A. Alim, A. A. Rezazadeh and C. Gaquiere, “Temperature effect on DC and equivalent circuit parameters of 0.15- μm gate length GaN/SiC HEMT for microwave applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 11, pp. 3483-3491, Nov. 2016.

[13] C. Davis and I. Finvers, "A 14-bit high-temperature ΣΔ modulator in standard CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 976-986, June 2003.

[14] P. C. de Jong, G. C. M. Meijer and A. H. M. van Roermund, "A 300°C dynamic-feedback instrumentation amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1999-2009, Dec 1998.

[15] B. Ohme, “High-temperature SOI technologies at Honeywell,” in *Extreme Environment Electronics*, J. D. Cressler and H. A. Mantooth, Eds., CRC Press, 2012, ch. 29, pp. 319-329.

[16] J. Cressler, “SiGe HBT platforms,” in *Extreme Environment Electronics*, J. D. Cressler and H. A. Mantooth, Eds., CRC Press, 2012, ch. 18, pp. 197-209.

[17] Tianbing Chen *et al*., "On the high-temperature (to 300°C) characteristics of SiGe HBTs," in *IEEE Transactions on Electron Devices*, vol. 51, no. 11, pp. 1825-1832, Nov. 2004.

[18] J. Wurfl, "Recent advances in GaAs devices for use at high temperatures," *1998 High-Temperature Electronic Materials, Devices and Sensors Conference (Cat. No.98EX132)*, San Diego, CA, 1998, pp. 106-116.

[19] J. A. Pellish and L. M. Cohn, “Technology options for extreme environment electronics,” in *Extreme Environment Electronics*, J. D. Cressler and H. A. Mantooth, Eds., CRC Press, 2012, ch. 6, pp. 49-58.

[20] A. Rahman, P. D. Shepherd, S. A. Bhuyan, S. Ahmed, S. K. Akula, L. Caley, *et al.*, "A family of CMOS analog and mixed signal circuits in SiC for high temperature electronics," in *Aerospace Conference, 2015 IEEE*, 2015, pp. 1-10.

[21] R. R. Lamichhane, N. Ericsson, S. Frank, C. Britton, L. Marlino, A. Mantooth, *et al.*, "A wide bandgap silicon carbide (SiC) gate driver for high-temperature and high-voltage applications," in *Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium on*, 2014, pp. 414-417.

[22] R. Stevenson, The world’s best gallium nitride, *IEEE Spectrum*, 47(7), 40–45, 2010.

[23] M. W. Shin and R. J. Trew, "GaN MESFETs for high-power and high-temperature microwave applications," in *Electronics Letters*, vol. 31, no. 6, pp. 498-500, 16 Mar 1995.

[24] Randall Kirschman, "GaN Based Transistors for High Temperature Applications," in *High-Temperature Electronics*, 1, Wiley-IEEE Press, 1999, pp.489-493.

[25] P. Herfurth, D. Maier, L. Lugani, J. F. Carlin, R. Rosch, Y. Men, *et al.*, "Ultrathin body InAlN/GaN HEMTs for high-temperature (600°C) electronics," *Electron Device Letters, IEEE*, vol. 34, pp. 496-498, 2013.

[26] V. Carrubba *et al*., "High-Efficiency, High-Temperature Continuous Class-E Sub-Waveform Solution AlGaN/GaN Power Amplifier," in *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 8, pp. 526-528, Aug. 2015.

[27] O. Silva, I. Angelov and H. Zirath, "4 W highly linear and reliable GaN power amplifier for C-band applications," *2015 Asia-Pacific Microwave Conference (APMC)*, Nanjing, 2015, pp. 1-3.

[28] M. L. Cunningham, D. S. Ha and K. J. Koh, "A high temperature wideband low noise amplifier for downhole applications," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 938-941.

[29] J. M. Salem and D. S. Ha, "A high temperature active GaN-HEMT downconversion mixer for downhole communications," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 946-949.

[30] C. T. Charles and D. J. Allstot, "A 2-GHz CMOS variable gain amplifier optimized for low noise," *2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, 2006, pp. 2305-2308.

[31] T. B. Kumar, K. Ma and K. S. Yeo, "Temperature-compensated dB-linear digitally controlled variable gain amplifier with DC offset cancellation," in IEEE Trans. Microw. Theory Tech., vol. 61, no. 7, pp. 2648-2661, July 2013.

[32] C. Liu, Y. P. Yan, W. L. Goh, Y. Z. Xiong, L. J. Zhang and M. Madihian, "A 5-Gb/s automatic gain control amplifier with temperature compensation," in IEEE J. Solid-State Circuits, vol. 47, no. 6, pp. 1323-1333, June 2012.

[33] Modelithics, "TriQuint GaN on SiC HEMT model," HMT-TQT-T2G6000528-Q3 datasheet, 2013 [rev. 001].

[34] TriQuint, "10W, 28V DC - 6 GHz, GaN RF power transistor," T2G6000528-Q3 datasheet, 2013 [Rev. C, Nov. 2014].

[35] Presidio Components, inc., "High temperature ceramic capacitors", datasheet, [Rev. M].

[36] IPDiA, "1206 extreme temperature silicon capacitors," XTSC427.xxxx datasheet, Feb. 2014 [doc. CL431 111 615 119].

[37] Coilcraft, "Extreme temperature coil," AT549RBT datasheet, [doc. AT098 rev. Jun. 2013].

[38] Vishay, "Precision automotive high temperature (155°C at full rated power) thin film chip resistor, AEC-Q200 qualified," PATT Thin Film Resistor datasheet, 2015 [doc. 60124 rev. Aug. 2014/Jun. 2015].

[39] Rogers Corp., "RO3000 series circuit materials," High frequency laminates datasheet, 2014 [Rev. Nov. 2014].

[40] Indium Corp., "Indium corp. Indalloy® 151 PbSnAg solder alloy," NC-SMQ51SC, Type 4 86.5%, Dispensed Paste datasheet, 2015.

[41] Engineering Toolbox, H. D. Young, R. A. Freedman, and et al. (2015, Nov.). *Thermal conductivities of some common materials* [Website; Book (University Physics, 13th ed.)].

[42] C. Cui, T. S. Kim, S. K. Kim, J. K. Cho, S. T. Kim and B. S. Kim, "Effects of the nonlinearity of the common-gate stage on the linearity of CMOS cascode low noise amplifier," *2011 IEEE Radio Frequency Integrated Circuits Symposium*, Baltimore, MD, 2011, pp. 1-4.

[43] B. Afshar and A. M. Niknejad, "X/Ku band CMOS LNA design techniques," IEEE Custom Integrated Circuits Conference 2006, San Jose, CA, 2006, pp. 389-392.

[44] Rohde and Schwarz, "R&S ZVA/R&S ZVB/R&S ZV Vector Network Analyzers," Operating Manual, [rev. Oct. 2016].

[45] Cole-Parmer. (2015). *Yamato high-temperature gravity convection oven, 0.9 cu ft, 115 VAC* [Image]. Available: http://www.coleparmer.com/Product/Yamato_High_Temperature_Gravity_Convection_Oven_0_9_Cu_Ft_115_VAC/EW-33959-00

[46] Rigol Technologies, Inc. (2015). *DP832A | triple output, 195 watt power supply* [Image]. Available: http://www.rigolna.com/products/dc-power-supplies/dp800/dp832a/

[47] Keysight Technologies (Agilent), "Operating and service manual: Agilent 346A/B/C noise source (including options 001, 002, and 004)," 346A/B/C datasheet, 2013 [rev. Aug. 2016].

[48] Maxim Integrated (2003, Nov 21). *Three methods of noise figure measurement* [Online]. Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/2875

[49] Keysight Technologies (Agilent), “ESA-L series spectrum analyzers,” datasheet, 2012 [rev. Jan. 2012].