High Frequency Isolated Power Conversion from Medium Voltage AC to Low Voltage DC

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Abstract

Modern data center power architecture developing trend is analyzed, efficiency improvement method is also discussed. Literature survey of high frequency isolated power conversion system which is also called solid state transformer is given including application, topology, device and magnetic transformer. Then developing trend of this research area is clearly shown following by research target.

State of art wide band gap device including silicon carbide (SiC) and gallium nitride (GaN) devices are characterized and compared, final selection is made based on comparison result. Mostly used high frequency high power DC/DC converter topology dual active bridge (DAB) is introduced and compared with novel CLLC resonant converter in terms of switching loss and conduction loss point of view. CLLC holds ZVS capability over all load range and smaller turn off current value. This is beneficial for high frequency operation and taken as our candidate. Device loss breakdown of CLLC converter is also given in the end.

Medium voltage high frequency transformer is the key element in terms of insulation safety, power density and efficiency. Firstly, two mostly used transformer structures are compared. Then transformer insulation requirement is referred for 4160 V application according to IEEE standard.
Solid insulation material are also compared and selected. Material thickness and insulation distance are also determined. Insulation capability is preliminary verified in FEA electric field simulation. Thirdly two transformer magnetic loss model are introduced including core loss model and litz wire winding loss model. Transformer turn number is determined based on core loss and winding loss trade-off. Different core loss density and working frequency impact is carefully analyzed. Different materials show their best performance among different frequency range. Transformer prototype is developed following designed parameter. We test the developed 15 kW 500 kHz transformer under 4160 V dry type transformer IEEE Std. C57.12.01 standard, including basic lightning test, applied voltage test, partial discharge test.

500 kHz 15 kW CLLC converter gate drive is our design challenge in terms of symmetry propagation delay, cross talk phenomenon elimination and shoot through protection. Gate drive IC is carefully selected to achieve symmetrical propagation delay and high common mode dv/dt immunity. Zero turn off resistor is achieved with minimized gate loop inductance to prevent cross talk phenomenon. Desaturation protection is also employed to provide shoot through protection. Finally 15 kW 500 kHz CLLC resonant converter is developed based on 4160V 500 kHz transformer and tested up to full power level with 98% peak efficiency.
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General Audience Abstract

Modern data center power architecture developing trend is analyzed, efficiency improvement method is also discussed. At the same time high frequency operation is preferred to reduce reactive component size like transformer and capacitor. To achieve better trade-off between high efficiency and high frequency in our research. Literature survey of high frequency isolated DC/DC power converter is given including application, circuit topology, power electronics device and magnetic transformer. Then developing trend of this research area is clearly shown following by research target.

State of art advance material based power electronics devices are characterized and compared, final selection is made based on comparison result. Mostly used high frequency high power DC/DC converter topology dual active bridge (DAB) is introduced and compared with novel CLLC resonant converter in terms of converter loss. CLLC holds smaller converter loss. This is beneficial for high frequency operation and taken as our candidate.

Medium voltage high frequency transformer is the key element in terms of insulation safety, power density and efficiency. Firstly, two mostly used transformer structures are compared. Then transformer insulation requirement is referred for 4160 V application according to IEEE standard.
Solid insulation material are also compared and selected. Material thickness and insulation distance are also determined. Thirdly transformer loss model are introduced including core loss model and winding loss model. Transformer turn number is determined based on transformer loss and volume trade-off. Transformer prototype is developed following designed parameter. We test the developed transformer under IEEE standard requirement and pass all the test.

Converter gate drive is one of our design challenge. We need to achieve symmetrical propagation delay between command signal and final drive circuit output, suppress interference from other high frequency switching devices, and protect device under short circuit condition. Gate drive IC is carefully selected to achieve symmetrical propagation delay and suppress other’s interference. Device conduction voltage is employed to compare with threshold value to determine whether it is under short circuit condition. Finally 15 kW 500 kHz CLLC resonant converter is developed based on 4160V 500 kHz transformer and tested up to full power level with 98% peak efficiency.
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Chapter 1 Introduction

In this chapter, research backgrounds, motivation and challenges will be present. Modern data center power architecture developing trend is analyzed, efficiency improvement method is also discussed. Literature survey of high frequency isolated power conversion system which is also called solid state transformer is given including application, topology, device and magnetic transformer. Then developing trend of this research area is clearly shown following by our research target. System architecture and specification are finally presented and followed by thesis outline and scope of research.

1.1 Research Background

Due to the increasing use of cloud computing and big data, the power consumption of the data center alone will reach 10% of the total electrical power consumption in the world by 2020. Considering such booming data center load development, high copper cost and conduction loss due to low voltage (480 VAC) power distribution outside sever hall need to be solved. On the other hand due to AC distribution within data center server hall, usage of multi-stage redundant power conversion stages leads to excessive losses dropping down overall efficiency obviously.

Traditionally data center take power from medium voltage (4.16kV–35kV) utility facility and step down to 480 V in site substation. All the power are distributed to sever hall through low voltage AC 480 V. For 2500 kVA data center the total distribution current can reach 3000 A. This leads to bulky and costly transmission bus and large conduction losses within the data center shown in Figure 1.1. Instead of low voltage, CCG Facility Integration proposed to use medium voltage (4160 V) distribution before server hall shown in Figure 1.2 [A1]. The distribution current is
reduced from 3000 A to only 350 A for a 2.5 megawatts facility using 4160 V AC. This will dramatically reduce copper usage as well as $i^2R$ loss on distribution cables.

Figure 1.1 Traditional Low Voltage (LVAC) Distribution before Sever Hall

Figure 1.2 Medium Voltage 4160 V (MVAC) Distribution before Sever Hall Proposed by CCG

More quantitative comparison is shown in Table 1.1 based on 2500 kVA power scale. For traditional 480V distribution 8 cable sets should be employed to conduct 3000 A current. By using 4160 V distribution before data center server hall, instead of 8 bulky cable sets only one medium voltage cable set is enough to provide 2500 kVA power and around 86% cable cost is saved. At the same time tremendous cable conduction loss is saved reducing from 54.4 kW to 6.6 kW which help increase overall efficiency by 2%.
Table 1.1 Comparison between LVAC (480 V) and MVAC (4160 V) under 2500 kVA Power Scale

<table>
<thead>
<tr>
<th></th>
<th>480V 3 Phase 4 Wire</th>
<th>4160V 3 Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Level</td>
<td>3000A</td>
<td>350A</td>
</tr>
<tr>
<td>Conductor Set</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Cable Total Across Section Area</td>
<td>417 mm$^2$</td>
<td>274 mm$^2$</td>
</tr>
<tr>
<td>Cable Total Cost</td>
<td>$864k</td>
<td>$120k</td>
</tr>
<tr>
<td>Cable Total Conduction Loss</td>
<td>54.4 kW</td>
<td>6.6 kW</td>
</tr>
<tr>
<td>Efficiency</td>
<td>97.8%</td>
<td>99.7%</td>
</tr>
</tbody>
</table>

If we take a detailed look into the power conversion in the conventional AC data center shown in Figure 1.3, we can find that multiple power conversion stages are used. First, a series connected UPS supplies power to the PDU (Power Distribution Unit) by converting AC input voltage to DC voltage and change it back to AC voltage. The 277 V AC output voltage is then stepped down to 208 VAC through the PDU’s 60 Hz transformer and distributed to the PSU (Power Supply Unit) at cabinet level. At the cabinet level, this power is again processed through multiple stages of power conversions to finally deliver the power to the processors (CPUs), memories devices (DDRs) and hard drives (HDDs) [A2, A3]. The usage of multi-stage redundant power conversion stages, as mentioned above, leads to excessive losses. The 60Hz transformer and high current distribution line leads to around 3% loss. UPS, PDU and PSU together brings about 12% loss.

1 Calculation is based on 300m distribution distance
In order to improve the power conversion efficiency inside the data center, two approaches are proposed, one developing trend is to continues to use AC distribution within server hall with paralleled UPS, another approach is that instead of AC, DC distribution within server hall is employed. Both of these two methods can reduce redundant power conversion stages.

Recently, a more streamlined power architecture has been proposed by Facebook [A4], as shown in Figure 1.4. This data center power architecture eliminates the series connected AC UPS and PDU transformer. It takes 480V AC directly to sever cabinets throughout the data center facilities. This 480 V AC is, then, converted to a 12 V DC bus and distributed to the servers at cabinet level. A 48 V DC UPS system is connected to the 12 V DC line in parallel instead of in series. This AC data center structure enables over 7% efficiency improvement. Companies like Facebook, Quanta Could Technology, and Microsoft are actively pursuing this kind of structure because it is deemed a more cost effective and energy efficient architecture.
However, with 15~20kW per rack power, over 1~2 kA current will flow through the 12 V DC bus bar, which requires very thick copper to reduce the related conduction loss [A5]. Also, a 48 V to 12 V DC/DC converter with full power is needed between the 48 V battery system and 12 V bus to discharge the battery in case of power outage. This will lead to low power density of the battery backup unit and also increasing the system cost and complexity. In order to further simplify the system structure, Google and Intel proposed an AC data center power structure with 48 V distribution bus at cabinet level, as shown in Figure 1.5. Compared with 12 V distribution, although the power conversion efficiency is almost the same, the conduction loss on the bus bar can be saved by 94% with 48 V DC bus using the same amount of copper [A5]. Or with the same amount of loss, the copper cost is saved by 94%. Also, with 48 V cabinet level distribution, the battery
backup unit can be directly connected to the 48 V bus without any voltage conversion. This also helps to reduce the total system cost and volume.

![Diagram of AC data center structure with 48 V UPS and 48 V bus proposed by Google and Intel](image)

Instead of AC distribution within server hall. The 2nd generation of data centers architecture eliminates the series connected UPS, PDU transformer and the PSU AC/DC stage by using DC distribution within server hall shown in Figure 1.6. It takes MVAC (4.16 kV AC or 13.8 kV AC) through a 60Hz transformer and distributes 480 V AC throughout the data center facilities. This 480 V AC is, then, converted to a 380 V DC bus and distributed to the servers at the cabinet level. A DC UPS system is connected to the 380 V DC line in parallel instead of in series. This DC data center structure enables a 3% efficiency improvement. Companies like NTT, Intel, Emerson, Delta,
Validus DC systems, IBM and ABB are actively pursuing the DC data center [A2, A3, A6-A10]. Based on this DC data center architecture, further improvements are pursued.

In both AC and DC data center power architectures, a line frequency transformer is employed to step down MVAC to 480 V AC and distribute 480 V AC throughout the facilities. With the ever increasing power consumption of mega data centers, presently, the 480 V AC distribution lines carry thousands of amperes of current which leads to a very bulky and costly transmission bus and large conduction loss within the data center power architecture.

Our research target is to find the most efficient and cost effective solution for the future data center. Therefore, it is our intention to demonstrate MVAC distribution before server hall and converted directly to 400 V DC distribution within server hall as shown in Figure 1.7. The crucial technology is high frequency isolated AC/DC system from MVAC to 400 V DC. This system offers insulation between MVAC and 400 V DC and totally eliminates the use of a bulky 60Hz
transformer saving 85% total space and weight. Also, the MVAC distribution can greatly reduce the distribution current and therefore greatly save $I^2R$ loss and copper cost. Total efficiency can be further improved to 84%.

![Diagram](image)

Figure 1.7 DC data center power architecture with MVAC directly to 400 V DC

1.2 Review of Solid State Transformer (SST) Research

The solid state transformer (SST) is a power electronic based equipment that replaces the traditional 50/60 Hz power transformer by means of high frequency transformer isolated AC-AC conversion technique, which is represented in Figure 1.8. The basic operation of the SST is firstly to change the 50/60 Hz AC voltage to a DC voltage by a AC/DC stage, then this DC voltage is stepped up/down by a high frequency isolated DC/DC stage with dramatically decreased volume and weight, and finally invert back into the desired 50/60 Hz AC to feed the load through a DC/AC stage. In this sense, the first advantage that SST may offer is the reduced volume and weight compared with traditional transformers. The key element within SST system is the high frequency
isolated DC/DC module which is same to our high frequency isolated AC/DC system. For our application the final stage of DC/AC is eliminated comparing to SST system. However the key element of DC/DC stage and input AC/DC stage is the common.

![Solid State Transformer Configuration](image)

**Figure 1.8 Solid state transformer configuration**

### 1.2.1 Review of SST Topologies and Devices

Considering medium voltage input for SST application and due to current power electronics device voltage rating and power rating limitation, generally multilevel converter is employed to block medium AC input voltage. Neutral point clamped topology is one of the method, however higher than 3 level is rarely used due to complexity. ERPI SST is using this topology shown in Figure 1.9 [A11, A12]. Diode clamped multilevel converter is applied for high voltage side for both rectifier stage and primary side of DC/DC stage. 18 kV/60A multilevel IGBT module is adopted. DC/DC stage is working at 20 kHz and rated at 50 kW.
Cascaded H bridge (CHB) converter is another mostly used topology to achieve this purpose. For CHB converter operation isolated DC voltage must be provided. Traditionally line frequency isolation is employed to achieve this purpose which is shown in Figure 1.10 (a), multi sets line frequency transformer is employed with bulky size and heavy weight. This structure is maturely used in medium voltage motor drive for years. However for SST system multi sets line frequency transformer is replaced with high frequency isolated DC/DC module shown in Figure 1.10(b). ABB, UNIFLEX and FREEDOM 1st Generation are all using this kind of topology [A13-A16].

ABB is using CHB structure to interface 15 kV medium voltage grid shown in Figure 1.11 for locomotive traction application. 6.5 kV IGBT is chosen as the main switch for H-bridge module.
[A13, A14]. 150 kW/ 1.5 kHz LLC resonant convert is employed as DC/DC stage without gain regulation and working at frequency (1.8 kHz) to pursue highest efficiency. Other company like ALSTON and Bombardier is also using similar CHB plus high frequency DC/DC structure for traction application [A15, A16].

UNIFLEX SST topology for smart grid application is shown in Figure 1.12 [A17]. It is a three-stage and three port power electronics converter used for UNIFLEX power management for future electricity network. The cascaded multilevel converter is adopted as the front-end stage with several interleaving dc/dc converters as the intermediate stage. It interfaces 3.3-kV distribution level voltage with low-voltage grids, such as 415 V system. 1.7 kV IGBT is used as H-bridge device Dual Active Bridge (DAB) is employed at DC/DC stage working at 2 kHz working frequency.

![Figure 1.11 ABB SST topology for traction application](image)

Figure 1.11 ABB SST topology for traction application (a) system structure (b) topology in detail [A13, A14]
FREEDOM 1\textsuperscript{st} Generation SST for smart nano grid energy router application is shown in Figure 1.13 [A18]. Three series cascaded H-bridge converter is used to block 7.2 kV medium voltage. 6.5 kV Si IGBTs are employed as AC/DC and primary side DC/DC devices. 600V/100A Si IGBTs are served as DC/DC secondary side device. AC/DC series connected input and LVDC side parallel output. DC/DC stage working as Dual Active Bridge (DAB) converter under 3 kHz working frequency is rated at 7 kW. With the development of wide band gap device especially 15kV/10A high voltage Silicon Carbide (SiC) MOSFET, FREEDM’s 2\textsuperscript{nd} generation SST is capable to simplify its cascaded multi-level structure into single H bridge converter structure shown in Figure 1.14 [A19]. This reduce control complexity and improve total reliability. Their 2\textsuperscript{nd} generation’s power level is improved to 20 kW and switching frequency is increased to 20 kHz. 15kV/10A SiC MOSFET is served as AC/DC and DC/DC primary side switches. 5 paralleled 600V/94A Super Junction MOSFETs are employed to build half-bridge at DC/DC secondary side. Finally 600V/200A Si IGBTs are employed as DC/AC inverter stage.
Figure 1.13 FREEDM 1st generation SST \[A18\]

(a) SST application for Energy Router           (b) FREEDM 1st generation SST topology

Figure 1.14 FREEDM 2nd generation SST \[A19\]

Combing NPC and cascaded multi-level topology, Dr. Kolar from ETH come up with a three phase SST topology shown in Figure 1.15 \[A20, A21\]. Five Cascaded NPC converter is capable to block 10 kV line to line medium voltage. After AC/DC 2.2 kV DC link is provided to a series resonant DC/DC stage. Total system rated power is 1 MVA with 10 kV AC line to line input and 400 V AC line to line output voltage. 1.7 kV IGBTs are employed for primary side device and 1.2 kV IGBTs are used as secondary side device. Working frequency are 1 kHz, 8 kHz and 4 kHz respectively for AC/DC, DC/DC and DC/AC stages.
For the most important DC/DC stage Dr. Kolar’s group also developed a higher working frequency 20 kHz DC/DC cell called MEGA cube shown in Figure 1.16 [A22]. 1.7 kV IGBTs are still served as primary side devices. With 2 kV DC input and 400 V DC output total stage rated power is 166 kW. They also developed SRC resonant DC/DC cell with same topology like MEGA Link SST but higher 20 kHz working frequency and 166 kW rated power [A20].
1.2.2 Review of Medium Voltage High Frequency Transformer

Besides topology and device selection, within high frequency high power DC/DC stage module, the most crucial component is the high frequency medium voltage insulated transformer from both insulation safety and power density point of view. Transformer structure and core material selection, insulation system design and winding configuration all can impact our final transformer design results in terms of safety, efficiency and power density point of view. Literature survey of high frequency medium voltage transformer is also carefully developed.

ABB’s Transformer is using UU cut core pairs to build magnetic path and integrate LLC resonant inductor $L_r$ as transformer leakage inductance [A13, A14]. Therefore both $L_r$ and $L_m$ is integrated into the medium frequency transformer. Nanocrystalline is chosen as the core material due to low loss and low sound noise. The working frequency is 1.8 kHz. Transformer air gap is carefully designed in order to achieve ZVS of primary side switches through tuning magnetizing inductance $L_m$. Transformer winding is made of litz wire, the coil diameter and space parameter is determined by both resonant leakage inductance $L_r$ value and insulation requirement. For their 15 kV application 75 kV impulse insulation test and 34.5 kV RMS dielectric test is performed on the prototype shown in Figure 1.17.
Figure 1.17 (a) Subassembly including three MFTs. (b) Oil-filled tank, which includes the start-up circuit, nine MFTs, and an input choke. [A14]

FREEDM 1st generation medium frequency transformer is shown in Figure 1.18 [A18]. The core is made of laminated amorphous (Metglas SA2605SA1) with 3 kHz working frequency and 7 kW rated power. UU core pairs are employed and gap between two core pair is designed to guarantee insulation. Jacket of litz wire winding is also designed to meet the insulation requirement. Transformer’s leakage inductance should be designed as 29.7 mH to achieve ZVS of DAB converter. Total turn ratio is 28:3 with 3.8 kV DC input and 400 V DC output.

Their 2nd generation increase both working frequency and power level to 20 kHz and 20 kW respectively [A19]. Core material is changed into laminated nanocrystalline to reduce high frequency core loss. They still use UU core sectionalized winding to guarantee insulation capability shown in Figure 1.19. Since the higher working frequency their 2nd generation occupies only one third of their 1st generation version space.
Dr. Kolar designed two version medium voltage high frequency transformer, one is using ferrite as core material and another is using nanocrystalline [A22]. EE like shape transformer is used instead of previous UU shape. It provides a better coupling between primary and secondary, at same time confine leakage flux inside magnetic cores.
The ferrite version transformer is shown in Figure 1.20(a). This design comprises 20 ferrite N87 U shape cores as magnetic material and litz wire with 9500 · 71 μm strand diameter (AWG41) where 3 parallel litz wires with two turns each are utilized in the LV side winding whereas the MV side winding is built using 6 turns of the same litz wire. The isolation is provided by a PTFE bobbin and the complete system is cooled by forced convection provided by two front 120mm fans.

The second constructed transformer is based on nanocrystalline core material and its winding cross-sectional view is shown in Figure 1.20(b). This transformer utilizes the same 9500 · 71 μm litz wire whereby two paralleled conductors with 2 turns each are used on the LV side whereas a single wire with 5 turns is utilized on the MV side. The isolation in this case is based on mica tape as often used in electrical machines. The cooling system is based on thermal conduction of heat from winding and core by means of aluminum parts that are attached to two water-cooled heat sinks.
Beside litz wire copper foil can also be employed as high frequency transformer (25 kHz/50 kW) winding shown in Figure 1.21[A23]. EE shape cores are still used and windings are surrounding on the transformer center leg. Amorphous is used as core material and partial interleave between primary and secondary is carefully designed to achieve target leakage inductance. However this kind of interleave structure is hard to implement if medium voltage insulation is needed since two much space will be occupied by insulation material for interleave structure. Ceramic heat pipes are used as heat removal plates between core and winding for thermal removal consideration.
Figure 1.21 Copper foil winding with partial interleave structure high frequency transformer \(^{(A23)}\)

Beside classic UU core structure and EE core structure, novel coaxial winding transformer is also developed by NCSU shown in Figure 1.22\(^{(A24)}\). In the coaxial structure, the flux encircles the cylindrical axis and the current flows in parallel with the cylindrical axis. Bobbin is designed to achieve insulation requirement. Although this structure is easy to control and predict the leakage inductance of the transformer by using the coaxial structure. However its disadvantages appear considering manufacture implementation and total cost. In addition, the coaxial structure is also limited by its flexibility on the turn ratio because it becomes quite difficult to design and manufacture multi turns in the low voltage side.
1.2.3 High frequency High Power Isolated DC/DC Module Developing Trend

Since the most important element of SST system is the high frequency isolated DC/DC stage, we list all the DC/DC module survey results in the Table 1.2. Traditionally mostly used devices are high voltage IGBTs, based on three level NPC topology 1.7 kV low cost IGBT is also employed in some application. Power level depends on specific application. Locomotive application holds higher power level [A13-A16, A20, A21] and smart DC nano grid [A18, A19] and charge station [A12, A25] holds lower power level. With development of wide band gap devices the DC/DC stage working frequency is going higher and higher up to 50 kHz [A25]. Mostly used topology is DAB converter [A17, A18, A19, A20], ABB is already using LLC unregulated resonant converter (DCX) [A13]. The system efficiency is also improved gradually.

From magnetic point of view, due to the increasing working frequency, nanocrystalline and MnZn ferrite are the mostly used core material. Mostly used transformer structure is still UU core shape [A13, A14, A18, A19] and EE core shape [A20, A21, A23]. All the transformer
windings are made by litz wire to reduce high frequency current conduction loss. Litz strand diameter is determined by working frequency. Most transformers are using dry type insulation method and ABB is already moving to oil immerse insulation due to its 15kV medium voltage application.

Table 1.2 High frequency DC/DC module summary

<table>
<thead>
<tr>
<th></th>
<th>Power level</th>
<th>Primary side device</th>
<th>Frequency</th>
<th>Eff.</th>
<th>Core Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALSTON 2003[A15]</td>
<td>180 kW</td>
<td>6.5kV IGBT</td>
<td>5kHz</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Bombardier 2007[A16]</td>
<td>500 kW</td>
<td>4.5kV IGBT</td>
<td>8kHz</td>
<td>97%</td>
<td>Nanocrystalline</td>
</tr>
<tr>
<td>UNIFLEX 2009[A17]</td>
<td>25 kW</td>
<td>1.7kV IGBT</td>
<td>2kHz</td>
<td>92%</td>
<td>Amorphous</td>
</tr>
<tr>
<td>FREEDM 2010[A18]</td>
<td>7 kW</td>
<td>6.5kV IGBT</td>
<td>3kHz</td>
<td>90.88%</td>
<td>Amorphous</td>
</tr>
<tr>
<td>EPRI 2012[A12]</td>
<td>50 kW</td>
<td>4.5kV IGBT</td>
<td>20kHz</td>
<td>96%</td>
<td>Ferrite</td>
</tr>
<tr>
<td>FREEDM 2012[A19]</td>
<td>20 kW</td>
<td>15kV SiC MOSFET</td>
<td>20kHz</td>
<td>94.8%</td>
<td>Nanocrystalline</td>
</tr>
<tr>
<td>ABB 2013[A13, A14]</td>
<td>150 kW</td>
<td>6.5kV IGBT</td>
<td>1.8kHz</td>
<td>93-95%</td>
<td>Nanocrystalline</td>
</tr>
<tr>
<td>ETH 2013[A20, A21]</td>
<td>166 kW</td>
<td>1.7kV IGBT</td>
<td>20kHz</td>
<td>97%</td>
<td>Nanocrystalline &amp; Ferrite</td>
</tr>
<tr>
<td>NCSU 2016[A25]</td>
<td>16 kW</td>
<td>1.2kV SiC MOSFET</td>
<td>50kHz</td>
<td>96%</td>
<td>Ferrite N87</td>
</tr>
</tbody>
</table>

According to survey results including power level and working frequency we place all their research in the Figure 1.23. Both power level and working frequency are increased recent years. However most of their research is still below 20 kHz. Compared with conventional DC/DC stage using Dual Active Bridge (DAB), CLLC resonant converter is able to achieve bi-directional power flow as well as soft switching for both primary side and second side switch. What’s more, it can greatly reduce the primary side turn off current, leading to small turn off loss. This benefit becomes significant when it comes to high frequency. We want to use newest developed SiC MOSFET and GaN devices into CLLC resonant converter to push the work frequency to unprecedented 500 kHz. Power level of each module is designed to be 15 kW.
1.3 High Frequency Isolated AC/DC System Architecture and Specification

As mentioned previously, we want to develop MVAC to 400 V DC high frequency isolated system for the future DC data center application shown in Figure 1.7. This configuration eliminates the use of a bulky 60 Hz transformer and redundant power conversion stages. Also, the MVAC distribution can greatly reduce the distribution current and therefore greatly save I^2R loss and copper cost.

The proposed SST structure is shown in Figure 1.24. Five cascade H-bridge converters together with high frequency isolated DC/DC converter are employed to convert medium voltage directly into 400 V DC. The inputs of H-bridges are in series and the outputs of the DC/DC stages are connected in parallel. The basic building block (AC/DC stage + DC/DC stage), as shown in Figure 1.24, is intended to have multiple functions, including power quality control, voltage step...
down, galvanic isolation, and output voltage regulation. Each sub-module’s rated power is 15 kW, giving one phase 5 sub-modules 75 kW and whole three phase system 225 kW.

For the AC/DC stage, a cascaded H-bridge multilevel rectifier will be used to reach desired medium voltage lines [A26-A30]. For a 4160 V AC line, the phase-to-neutral input voltage is 2.4 kV AC. With 1200 V SiC MOSFET as switch, a five H-bridge with an eleven-level staircase multilevel waveform can be established as shown in Figure 1.25. The synthesized line voltage is capable of eliminating a very high order of line frequency harmonics up to any desired level such that a relatively small inductor is sufficient to filter out the higher order harmonics. To date, the cascaded H-bridge multilevel rectifier is deemed a mature technology and can be directly applied to the proposed DC data center application. Therefore, the proposed work will be focused on the design of the DC/DC stage.
For DC/DC stage, a novel bi-directional CLLC resonant converter, instead of the popular back-to-back connected dual active bridge, will be employed. The symmetrical structure of the CLLC resonant tank, shown in Figure 1.26, enables the bi-directional power flow at its best operation mode. The switching frequency is locked at resonant frequency of the tank for its most efficient operation. Working waveform shows that the primary switch turns on under zero voltage switching (ZVS) and turns off at a relatively small current. The secondary-side switches are turned on under ZVS and turned off under zero current switching (ZCS).
1.4 Thesis Outline

As mentioned above the DC/DC stage is the key element in overall system in terms of power density and insulation point of view. This thesis will focus on 15kW 500kHz DC/DC converter including topology comparison, device characterization, transformer insulation design and magnetic loss analysis. 15 kW 500 kHz transformer with 30 kV insulation capability is developed and tested referring to IEEE Std. C57.12.01 standard. Whole 15 kW 500 kHz DC/DC converter is also designed and tested up to full power level. The detailed outline is shown as following:

In chapter 1, research backgrounds, motivation and challenges are present. Modern data center power architecture developing trend is analyzed, efficiency improvement method is also discussed. Literature survey of high frequency isolated power conversion system which is also called solid state transformer is given including applications, topologies, devices and magnetic transformer. Then developing trend of this research area is clearly shown following by our research target. System architecture and specification are finally presented and followed by thesis outline and scope of research.
In chapter 2, State of art wide band gap device including SiC and GaN devices are characterized and compared, final selection is made based on characterization result. Mostly used high frequency high power DC/DC converter topology dual active bridge (DAB) is introduced and compared with novel CLLC resonant converter in terms of switching loss and conduction loss point of view. CLLC holds ZVS capability over all load range and smaller turn off current value. This is beneficial for high frequency operation and chosen as our candidate. Device loss breakdown of CLLC converter is also given in the end.

Chapter 3 mainly focus on medium voltage high frequency transformer design. Firstly, two mostly used transformer structures are compared. Then transformer insulation requirement is referred for 4160 V application according to IEEE standard. Solid insulation material are also compared and selected. Material thickness and insulation distance are also determined. Insulation capability is preliminary verified in FEA electric field simulation. Thirdly two transformer magnetic loss model are introduced including core loss model and litz wire winding loss model. Transformer turn number is determined based on core loss and winding loss trade-off. Transformer working frequency impact is also analyzed carefully between three state of art core materials over 200–1000 kHz frequency range. Transformer prototype is developed following designed parameters. We test the developed 15 kW 500 kHz transformer under 4160 V dry type transformer IEEE Std. C57.12.01 standard requirement, including basic lightning test, applied voltage test, partial discharge test. The prototype passed all the three tests and insulation capability is verified.

In chapter 4, 500 kHz 15 kW CLLC converter gate drive is our design challenges in terms of symmetry propagation delay, cross talk phenomenon elimination and shoot through protection. Gate drive IC is carefully selected to achieve symmetrical propagation delay and high common mode dv/dt immunity. Zero turn off resistor is achieved with minimized gate loop inductance to
prevent cross talk phenomenon. Moreover desaturation protection is also employed to provide shoot through protection. Finally 15 kW 500 kHz CLLC resonant converter is developed and tested up to full power level with 98% peak efficiency.

Chapter 5 gives a summary of the thesis. Possible future work is also presented.
Chapter 2 Device Selection and Topology Comparison

State of art wide band gap device including SiC and GaN devices are compared and characterized for converter loss analysis. Traditionally mostly used high frequency high power DC/DC converter topology is dual active bridge (DAB) which is introduced and compared with novel LLC resonant converter in terms of switching loss and conduction loss point of view. LLC holds ZVS capability over all load range and smaller turn off current all of which are beneficial for high frequency operation and taken as our candidate for DC/DC stage. Device loss breakdown of LLC converter is also given in the end.

2.1 Wide Band Gap Device Candidate Determination and Characterization

As a wide-bandgap material, Silicon Carbide (SiC) and Gallium Nitride (GaN) offers a critical electric field – an order of magnitude higher than that of Si. This significantly increases the blocking capability of wide band gap material power devices, and also allows them to be fabricated with much thinner and more highly doped drift layers, which greatly reduces the on-state resistance. As a result, high-voltage (1.2 kV) SiC unipolar switches, such as JFETs and MOSFETs, have become realistic to offer much faster switching speeds than the traditional high-voltage Si devices, which have to be made in bipolar structures (e.g. BJT or IGBT) due to the material limit, without sacrificing the conduction loss. Moreover, the high thermal conductivity of SiC (4.9 W/cm·K) improves the device’s heat dissipation, and along with the wide bandgap energy (3.3 eV), allows high-temperature operation above 300 °C in theory [B1-B4]. The main properties of Si, SiC and GaN materials are compared in Table 2.1. Due to all the superior properties of wide band gap material over Silicon, SiC and GaN devices is employed for the 500 kHz 15 kW DC/DC converter.
Table 2.1 Comparison of Si, SiC and GaN Material Properties

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Si</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Energy</td>
<td>1.1</td>
<td>3.3</td>
<td>3.4</td>
<td>eV</td>
</tr>
<tr>
<td>Critical Electrical Field</td>
<td>0.23</td>
<td>2.2</td>
<td>3.3</td>
<td>MV/cm</td>
</tr>
<tr>
<td>Electron mobility</td>
<td>1500</td>
<td>650</td>
<td>2000</td>
<td>cm²/Vs</td>
</tr>
<tr>
<td>Electron saturated drift velocity</td>
<td>1.0</td>
<td>2.0</td>
<td>2.5</td>
<td>10⁷ cm/s</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>1.5</td>
<td>4.9</td>
<td>1.3</td>
<td>W/cm·K</td>
</tr>
</tbody>
</table>

2.1.1 Wide Band Gap Device Candidate Selection

As mentioned above, the DC/DC stage input DC voltage is 800 V and output DC voltage is 400 V, since then 1200 V SiC MOSFET is chosen for primary side H-bridge and 600 V GaN device is chosen for secondary H-bridge shown in Figure 2.1.

Three 1200 V SiC MOSFET device candidates are listed and compared in Table 2.2. Candidate A (C2M0025120D) come from CREE, candidates B (GE12N65L-3) and candidate C(GE12N025RF-3) come from GE. Candidate B and C from GE holds lower conduction
resistance ($R_{on}$) at 150 °C with even smaller output capacitance ($C_{oss}$). Even though they hold same $R_{on}$ under 25 °C, when temperature increases candidate A $R_{on}$ increases faster comparing to GE products. Maximum working temperature is also higher for GE products. For conduction loss consideration candidate A is ruled out. Comparison between candidate B and candidate C is that Candidate B holds TO-247 package and Candidate C holds DE-150 package shown in Figure 2.2. Unlike TO-247, DE-150 package holds decoupled MOSFET power loop and gate drive loop which means there is a Kalvin connection for device gate drive loop. This characteristic tremendously reduce interference to gate drive signal due to power loop di/dt during fast switching transient. In the other word, DE150 package make it easier for faster switching without false trigger device gate signal resulting in converter failure. However we also need to note that due to DE150 package footprint is smaller comparing to TO-247, its power dissipation capability is lower and maximum conduction current is considerably lower comparing to TO-247 package. Finally we choose candidate C (GE12N025RF-3) as our device candidate as trade-off between conduction loss and high frequency switching performance.

GaN device selection for secondary side is easier, three candidates’ parameters are shown in Table 2.3. For 15 kW high power converter in order to reduce secondary side conduction loss, lower $R_{on}$ device is preferred. Finally GS66516T from GaN System is chosen since it holds lowest $R_{on}$ among all the candidates.
Table 2.2 1200 V SiC MOSFET candidates comparison

<table>
<thead>
<tr>
<th></th>
<th>C2M0025120D (CREE)</th>
<th>GE12N65L-3 (GE)</th>
<th>GE12N025RF-3 (GE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$ (V)</td>
<td>1200</td>
<td>1200</td>
<td>1200</td>
</tr>
<tr>
<td>Package</td>
<td>TO-247</td>
<td>TO-247</td>
<td>DE-150</td>
</tr>
<tr>
<td>$R_{on}@25^\circ C$ (mΩ)</td>
<td>25</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>$R_{on}@150^\circ C$ (mΩ)</td>
<td>43</td>
<td>33</td>
<td>37</td>
</tr>
<tr>
<td>$R_{on}@200^\circ C$ (mΩ)</td>
<td>-</td>
<td>42</td>
<td>42 (175°C)</td>
</tr>
<tr>
<td>$T_J$ (°C)</td>
<td>-55 ~ 150</td>
<td>-55 ~ 200</td>
<td>-55 ~ 175</td>
</tr>
<tr>
<td>$I_D@25^\circ C$ (A)</td>
<td>90</td>
<td>100</td>
<td>61</td>
</tr>
<tr>
<td>$I_D@100^\circ C$ (A)</td>
<td>60</td>
<td>75</td>
<td>43</td>
</tr>
<tr>
<td>$I_D@125^\circ C$ (A)</td>
<td>-</td>
<td>65</td>
<td>35</td>
</tr>
<tr>
<td>$V_{GS}$ (V)</td>
<td>-10 ~ +25</td>
<td>-15 ~ +23</td>
<td>-15 ~ +23</td>
</tr>
<tr>
<td>$V_{GS_TH}$ (V)</td>
<td>3.0</td>
<td>3.2</td>
<td>3.2</td>
</tr>
<tr>
<td>$C_{iss}$ (pF)</td>
<td>2788 @$V_{DS}=1000V$</td>
<td>3659 @$V_{DS}=500V$</td>
<td>3164 @$V_{DS}=500V$</td>
</tr>
<tr>
<td>$C_{rss}$ (pF)</td>
<td>15 @$V_{DS}=1000V$</td>
<td>15 @$V_{DS}=500V$</td>
<td>21 @$V_{DS}=500V$</td>
</tr>
<tr>
<td>$C_{oss}$ (pF)</td>
<td>220 @$V_{DS}=1000V$</td>
<td>216 @$V_{DS}=500V$</td>
<td>199 @$V_{DS}=500V$</td>
</tr>
<tr>
<td>$Q_G$ (nC)</td>
<td>161 (-5/+20 V) @$V_{DS}=800V$</td>
<td>170 (0-20V) @$V_{DS}=600V$</td>
<td>170 (0-20V) @$V_{DS}=600V$</td>
</tr>
<tr>
<td>$R_G$ (Ω)</td>
<td>1.1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 2.2 Package comparison between (a) TO-247 and (b) DE150
2.1.2 Device Candidate Characterization

Both primary and secondary side device candidates are determined in previous section, we also need to know device dynamic switching performance for circuit topology selection and loss breakdown analysis. Device double pulse tester is built to evaluate device switching performance and switching loss shown in Figure 2.3. Device under test (DUT) is placed as the low side of half bridge. By adding two pulse to the bottom switch and keep low gate voltage for top device, both device turn on and turn off performance can be characterized during switching event shown in Figure 2.3. First pulse is used to establish inductor current to target test condition and at the turn off moment of first pulse device turn off performance is characterized and at the second pulse turn on moment device turn on performance is characterized. Both device turn on and turn off loss can be calculated based on integration of device current $I_{dut}$ and $V_{ds}$ during switching transient.

<table>
<thead>
<tr>
<th>GaN</th>
<th>PGA26E08 (Panasonic)</th>
<th>GS66516T (GaN Systems)</th>
<th>TPH3205 (Transphorm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$ (V)</td>
<td>600V</td>
<td>650V</td>
<td>600V</td>
</tr>
<tr>
<td>$C_{oss_tr}$ (pF)</td>
<td>98 @ $V_{DS}=400V$</td>
<td>286 @ $V_{DS}=400V$</td>
<td>170 @ $V_{DS}=400V$</td>
</tr>
<tr>
<td>$R_{on}$ @25°C (mΩ)</td>
<td>54</td>
<td>27</td>
<td>63</td>
</tr>
<tr>
<td>$Q_g$ (nC)</td>
<td>8.5</td>
<td>13</td>
<td>10</td>
</tr>
</tbody>
</table>
Both SiC and GaN device candidate characterization results are shown in Figure 2.4. The blue curve represent SiC MOSFET and red curve represent GaN device. Turn on loss is shown in dash line and turn off loss is shown in solid line. SiC is test under 800 V DC and GaN is tested under 400 V DC. With the increment of test current both turn on and turn off loss increase. However it is obvious that both SiC and GaN device hold higher turn on loss than that of turn off. Therefore ZVS turn on is very critical for these wide band gap device candidate to work at 500 kHz frequency.

![Figure 2.4 Device candidate switching loss characterization](image)

**2.2 DC/DC Topology Comparison and Selection**

According to previous chapter survey results, mostly used topology for high frequency high power DC/DC stage is Dual Active Bridge (DAB) converter [A17-A20] and recent updated research ABB already begin to using LLC resonant converter without regulation to work at DCX
mode [A13]. Resonant converter is very good candidate for high frequency operation. However LLC can’t boost gain in reverse power flow direction. A novel resonant converter CLLC with symmetrical resonant tank is proposed in [B5]. Thanks to the symmetrical resonant tank, CLLC holds same working principle for both power flow direction. Detailed comparison between DAB and CLLC is present in the following.

2.2.1 Topology Candidates Working Principle

Dual active bridge (DAB) converter is firstly proposed by Dr. DeDonker in [B6] the topology is shown in Figure 2.5. It uses active full bridge circuit at both primary and secondary. For state of art DAB converter both primary side and secondary side diagonal switch pairs are controlled with 50% duty cycle shown in Figure 2.6. By adjusting phase shift angel between primary and secondary square waveform, output voltage can be regulated smoothly. DAB can achieve ZVS turn on for both primary and secondary side devices. During the dead time between two diagonal switch pairs energy stored in isolated transformer leakage inductance is used to charge discharge output capacitance \( C_{oss} \) of commutation devices. However this converter will lose ZVS at light load due to energy stored in leakage inductance is not enough to charge and discharge \( C_{oss} \). Moreover, this converter always turn off switches at peak working current which results in high turn off loss during high frequency operation.
DAB detailed operation mode in half cycle ($t_1$~$t_4$) is shown in Figure 2.7. Before $t_1$ primary side S2 and S3 is conducting, secondary side S6, S7 is conducting. At $t_1$ moment S2 and S3 turn off at peak working current level. Since the leakage inductance exists in the working current loop, the current can’t go to zero immediately, the current will charge S2 and S3 output capacitance C2 and C3; discharge S1 and S4 output capacitance C1 and C4 shown in Figure 2.7(b). Here we need to note that during this period leakage inductance resonant with primary side device’s $C_{oss}$, the leakage inductance initial stored energy should be enough to fully achieve charge and discharge device $C_{oss}$. If the load current is small then device’s $C_{oss}$ can’t be fully charged and discharged. Then the converter will lose ZVS. When current finish fully charge and discharge primary side device’s $C_{oss}$, the current will go through device S1 and S4 body diode, then we need to turn on S1 and S4 channel with ZVS turn on. Between $t_1$ and $t_2$ shown in Figure 2.7(c), current direction is not changed, after $t_2$ current direction is reversed shown in Figure 2.7(d). At $t_3$ moment S6 and S7 turn off shown in Figure 2.7(e). Again leakage inductance current will charge C6 and C7, discharge C5 and C8. After C5 and C8 are fully discharged we turn on S5 and S8 device channel with ZVS...
turn on. After this during $t_3$~$t_4$ period, primary side $S1$ and $S4$ is conducting, secondary $S5$ and $S8$ is conduction, the energy is delivering from primary side to secondary side.

![Diagram](image1)

(a) Circuit work condition before $t_1$

![Diagram](image2)

(b) Circuit commutation transient at $t_1$ moment

![Diagram](image3)

(c) Circuit work condition between $t_1$~$t_2$

![Diagram](image4)

(d) Circuit work condition between $t_2$~$t_3$

![Diagram](image5)

(e) Circuit commutation transient at $t_3$ moment

![Diagram](image6)

(f) Circuit work condition between $t_3$~$t_4$

Figure 2.7 DAB detailed work condition equivalent circuit

The symmetrical nature of CLLC resonant tank shown in Figure 2.8 makes the converter operate symmetrically for bidirectional power flow. Same as LLC converter, CLLC employs magnetizing inductance to achieve ZVS of primary side switches for whole load range, and
synchronize rectifier (SR) control method is used for secondary side H bridge to minimize converter conduction loss. Vice versa for negative power flow. Even through working frequency can be used to regulate converter output voltage, however in order to increase DC/DC stage efficiency we want to make the CLLC work at most efficient frequency that is resonant frequency \(f_r = f_o\). The working waveform is shown in Figure 2.9 when \(f_r = f_o\). From switching loss prospective, there is only turn off loss of primary switches at the peak current value of magnetizing current.

![Figure 2.8 CLLC resonant converter](image)

![Figure 2.9 CLLC resonant converter waveform when \(f_r = f_o\)](image)
CLLC resonant converter detailed operation in one cycle is shown in Figure 2.10 when switching frequency is equal to resonant frequency ($f_s = f_o$). Since $t_0$ moment S1 and S4 is turned on, primary side working current begin to resonant, magnetizing current increase gradually, secondary side S5 and S8 is conducting in third quadrant working at synchronous rectifier status. The equivalent working circuit is shown in Figure 2.10(a). At $t_1$ moment primary side current resonant back to touch magnetizing current, primary side S1 and S4 turn off at low turn off current which is only peak current of magnetizing current. Secondary side device current $i_{SR5}$ reaches zero when we need to turn off S5 and S8 with ZCS switching. Then current in inductance including $L_{r1}$, $L_{r2}$ and $L_m$ can’t go to zero immediately, this current will charge primary side output capacitance C1, C4 and secondary side output capacitance C5, C8; discharge primary side output capacitance C2, C3 and secondary output capacitance C6, C7. Then equivalent circuit is shown in Figure 2.10(b). Considering magnetizing inductance is large enough to be taken as a current source during $t_1$~$t_2$, and load condition will not impact magnetizing current peak value which is only determined by input voltage and switching frequency. We can conclude that CLLC can always achieve ZVS turn on for whole load range as long as dead time is enough. After primary side and secondary side device output capacitance are fully charged and discharged, body diode D2, D3 and D6, D7 begin to conduct current, and then we turn on channel of S2, S3 and S6, S7 to achieve ZVS turn on for both primary and secondary. We need to note that in reality during $t_1$~$t_2$ period, secondary side current can’t be zero in order to commute current from S5, S8 to S6, S7. Part of the energy stored in $L_m$ is also used by secondary to charge and discharge output capacitance. Then another half cycle begins which is totally symmetrical to the first half cycle shown in Figure 2.10(c-d).
2.2.2 Comparison between DAB and CLLC

After detailed analysis of both DAB and CLLC resonant operation principle, we still need to make a more quantitative comparison. Based on previous device switching loss characterization results we can compare device related loss for both DAB and CLLC over different working frequency (200 kHz, 300 kHz, 500 kHz). Quantitative circuit simulation can be done for both DAB and CLLC however isolation transformer parameters should be determined firstly. Because DAB don’t need to use transformer magnetizing inductance to operate, we treat DAB’s $L_m$ as infinite large inductance.

However for CLLC the magnetizing inductance is determined by dead time and device output capacitance. We assume CLLC exactly achieve ZVS after dead time and magnetizing current is constant during dead time. Equivalent waveform is shown in Figure 2.11. The magnetizing inductance can be calculated based on equation 2.1. From this equation, it can be
observed that magnetizing inductor is proportional to the switching cycle ($T_o$) and dead-time ($t_d$), and it is inverse proportional to the equivalent junction capacitor ($C_{oss}$). Increasing dead-time or reducing MOSFET junction capacitor could result in a larger magnetizing inductor. Larger magnetizing inductance comes with smaller transformer gap distance and resulting in smaller fringing effect on transformer winding. Finally benefit transformer winding loss due to less eddy current from fringing effect. For specific device $C_{oss}$ magnetizing inductance can be determined by converter dead time.

**Figure 2.11 Equivalent current waveform for calculation**

$$L_m \leq \frac{T_o \cdot t_{dead}}{8 C_{oss}} \quad (2.1)$$

For both primary and secondary side current RMS value can be calculated based on equation 2.2 and 2.3 respectively with only one dependent variable that is dead time $t_d$. Production of conduction current and device $R_{on}$ under 100 °C, we can calculate device conduction loss with different dead time in equation 2.4 which is plotted in Figure 2.12. We can find that the conduction loss shows a U shape curve with swept dead time. When dead time is too small then $L_m$ has to be very small which will tremendously increase primary side current RMS value with huge conduction loss. However when the dead time is too large less time is used to transfer energy to
load, and converter working current RMS value will also increase with higher conduction loss. Finally optimal dead time is found around the valley region with 80 ns for our 500 kHz switching frequency. Then the magnetizing inductance can be calculated using equation 2.1 to be 28 uH.

\[
I_{pri\_RMS}(t_d) = \frac{1}{4\sqrt{2}} \frac{I_o}{N} \sqrt{\frac{64N^4C_{oss}^2(V_o/I_o)^2}{t_d^2} + 4\pi^2 + \frac{16\pi^2(T_d + t_d^2)}{T_o^2}}
\]  

(2.2)

\[
I_{sec\_RMS}(t_d) = \frac{\sqrt{6}}{24\pi} I_o \sqrt{\frac{64(5\pi^2 - 48)C_{oss}^2N^4(V_o/I_o)^2T_o^2}{T_d^2(T_o + 2t_d)} + \frac{12\pi^4T_o}{T_o + 2t_d} + \frac{48\pi^4(t_d^2 + t_0T_o)}{T_o(T_o + 2t_d)}}
\]  

(2.3)

\[
P_{con} = I_{pri\_rms}^2(2R_{dson\_pri}) + I_{sec\_rms}^2(2R_{dson\_sec})
\]  

(2.4)

![Figure 2.12 Device conduction loss VS dead time (t_d)](image)

For the transformer leakage inductance in order to make a complete comparison between DAB and CLLC two topologies, we set three different leakage combinations for both primary and secondary leakage inductance to make comparison. All the simulation condition is shown in Table 2.4. Three different comparison six simulation circuit is then conducted in Simplis platform. Both primary and secondary conducting current and turn off current are shown in Figure 2.13(a-c), Device related loss including conduction loss and switching loss are also shown in Figure 2.13. Analysis of these results will be present as following:
Table 2.4 Simulation condition for three comparisons of DAB VS CLLC

<table>
<thead>
<tr>
<th></th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input/Output voltage</td>
<td>800V/400V</td>
<td>800V/400V</td>
<td>800V/400V</td>
</tr>
<tr>
<td>Frequency</td>
<td>500 kHz</td>
<td>500 kHz</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Load condition</td>
<td>15kW</td>
<td>15kW</td>
<td>15kW</td>
</tr>
<tr>
<td>Transformer turn ratio</td>
<td>2:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>Primary leakage inductance</td>
<td>2uH</td>
<td>3uH</td>
<td>4uH</td>
</tr>
<tr>
<td>Secondary leakage inductance</td>
<td>0.5uH</td>
<td>0.75uH</td>
<td>1uH</td>
</tr>
<tr>
<td>Magnetizing inductance</td>
<td>DAB 28uH</td>
<td>DAB 28uH</td>
<td>LLC 28uH</td>
</tr>
<tr>
<td></td>
<td>Infinite</td>
<td>Infinite</td>
<td>Infinite</td>
</tr>
</tbody>
</table>

For case 1 primary leakage inductance is only 2 uH and secondary leakage inductance is only 0.5 uH. From conduction loss point of view, due to the quasi square current waveform shape of DAB, both primary and secondary side current RMS value is smaller comparing to CLLC. Therefore, CLLC holds higher conduction loss comparing to DAB converter for comparison case 1. However from switching loss point of view, as mentioned above DAB always turns off devices at the peak of working current which is larger than that of CLLC. Note that CLLC secondary devices work at SR mode, when switching frequency is equal to resonant frequency, secondary side device can achieve ZCS turn off. Therefore, DAB holds higher turn off switching loss comparing to CLLC. Finally, CLLC shows advantage over DAB considering summation of conduction loss and switching loss.

For case 2 primary leakage inductance is increased to 3uH and secondary leakage inductance is 0.75uH. Increment of leakage inductance does not influence CLLC simulation result due to its working principle when \( f_s = f_o \). For DAB converter larger leakage inductance provide higher energy to achieve ZVS for the converter under light load. However larger leakage inductance also require larger reactive energy resonant between primary and secondary which will
increase working current RMS value for both primary and secondary shown in Figure 2.13(b). Thus DAB shows higher conduction loss and switching turn off loss, CLLC shows more advantage over DAB when leakage inductance increases. Case 3 still agree with this conclusion. Due to the increment of leakage inductance, working current RMS value of DAB is even larger than that of CLLC.

Because of previous comparison results, for our application we have following conclusions. Firstly, CLLC shows lower device switching turn off loss and holds ZVS turn on over all load range, however DAB holds much higher turn off loss and might lose ZVS at light load. Secondly, when leakage inductance is small DAB converter holds lower conduction loss over CLLC due to its quasi-square working waveform and CLLC working waveform is sinusoidal shape. With the increment of leakage inductance, DAB working current increase due to large reactive energy resonant between primary and secondary. Under large leakage inductance DAB even holds higher current RMS value over CLLC. All in all, CLLC shows lower device related loss over DAB for our application and CLCL resonant circuit is chosen as our DC/DC topology candidate.
(b) DAB vs CLLC case 2 \( L_{r1} = 3 \) uH, \( L_{r2} = 0.75 \) uH

![Simulation Current Comparison](image)

![Device Loss Comparison](image)

(c) DAB vs CLLC case 2 \( L_{r1} = 4 \) uH, \( L_{r2} = 1 \) uH

Figure 2.13 DAB and CLLC simulation result and estimated device related loss comparison

Detailed device loss break down including driving loss of 15 kW CLLC over different working frequency is shown in Figure 2.14. Assume junction working temperature is 100°C and turn off external gate resistor is 0 Ohm. Even under 500 kHz switching frequency, device related loss is still below 1% of total converter power.
Figure 2.14 Device related loss breakdown over different working frequency

- $T_j=100^\circ C$
- $R_{g_{off}}=0\Omega$
- 15kW
Chapter 3 High Frequency Medium Voltage Transformer Design

The medium voltage high frequency transformer is the most important component in the whole DC/DC converter in terms of both insulation and power density. This chapter will mainly focus on transformer design including transformer structure comparison, transformer insulation design, and transformer loss design trade off. Firstly, two mostly used transformer structures UU core type and EE core type are compared to figure out transformer structure. Then transformer insulation requirement is referred for 4160 V application according to IEEE standard. Solid insulation material are also compared and selected. Material thickness and insulation distance are also determined. Insulation capability is preliminary verified in FEA electric field simulation. Thirdly two transformer magnetic loss model are introduced including core loss model and litz wire winding loss model. Transformer turn number is determined based on core loss and winding loss trade-off. Transformer prototype is developed following designed parameter. The prototype parasitic parameters are tested and insulation capability is also tested referring to IEEE standard including basic lightning test, applied voltage test, partial discharge test. Finally different working frequency impact on transformer design is also analyzed, different material’s optimal frequency is found through trade-off between magnetic loss and volume.

3.1 Transformer Structure Determination

According to our previous survey the mostly used transformer structures are still EE core and UU core structure shown in Figure 3.1. For both of these two structures sectionalized winding are employed to guarantee insulation capability. For CLLC resonant converter we need to design proper magnetizing inductance to achieve device ZVS, since then gap between two core parts can be used to insert a shielding board between primary and secondary coil to increase both clearance
and creep age distance. From magneto motive force (MMF) point of view type 1 holds two times higher MMF value comparing to type 2, moreover type1 holds shorter air flux path length \( (l_d) \), all of which result in larger leakage inductance and higher eddy current loss comparing to type 2 structure. Type 2 structure splits both primary and secondary winding into single layer to help reduce magnetic field value and leakage inductance.

**Figure 3.1** Transformer structure comparison between (a) type 1 EE core and (b) type 2 UU core

Based on previous analysis, 3D FEA simulation is done in Maxwell and the magnetic field simulation result is shown in Figure 3.2 under same scale. It is obvious that type 1 holds higher magnetic field value within the window area since it holds higher MMF value and shorter air flux path length. From quantitative leakage inductance point of view type 1 holds 12 uH leakage inductance which is two times larger than that of type 2 6.1 uH. The simulation results agree with previous analysis and type 1 winding is verified working under higher flux density which generates higher eddy current loss.
Figure 3.2 Magnetic field simulation comparison between (a) type 1 EE core and (b) type 2 UU core

Besides winding loss larger leakage inductance will also influence CLLC resonant capacitor voltage stress. According to previous leakage simulation result, we can calculate corresponding resonant capacitor value under different resonant frequency (100 kHz/ 300 kHz/ 500 kHz) shown in Figure 3.3. Then we submit the resonant tank parameters into CLLC resonant circuit simulation in Simplis under 15 kW load condition. Finally resonant capacitor voltage stress is measured and compared. For the worst case under 500 kHz 15 kW condition type 1 structure holds 1200 V voltage stress which is two times higher than that of type 2 structure 618 V. Therefore type 2 UU core structure is chosen as our candidate.

Figure 3.3 (a) Resonant capacitor value comparison and (b) resonant capacitor voltage stress comparison

<table>
<thead>
<tr>
<th>Resonant Capacitor C\textsubscript{rp} Comparison</th>
<th>Resonant Capacitor Voltage Stress</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Resonant Capacitor C\textsubscript{rp} Comparison" /></td>
<td><img src="image2.png" alt="Resonant Capacitor Voltage Stress" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>100kHz</th>
<th>300kHz</th>
<th>500kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type1</td>
<td>Type2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>211</td>
<td>23.3</td>
<td>8.4</td>
</tr>
<tr>
<td>415</td>
<td>46.1</td>
<td>16.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>100kHz</th>
<th>300kHz</th>
<th>500kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type1</td>
<td>Type2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512</td>
<td>256</td>
<td>1200</td>
</tr>
<tr>
<td>837</td>
<td>422</td>
<td>618</td>
</tr>
</tbody>
</table>
3.2 Medium Voltage Insulation Design

Whole AC/DC conversion system is shown in Figure 3.4 with medium voltage (4160 V) input voltage and 400V output voltage. For this medium voltage application system, insulation safety is crucial for overall system. The detail circuit of cascaded submodule is also shown in Figure 3.4. It is obvious that only the high frequency isolated transformer can provide insulation safety function for overall system and it should be designed based on the input medium voltage level 4160 V. Insulation between primary high voltage winding and secondary low voltage winding and transformer core should all designed based on 4160 V insulation requirement. However insulation between secondary winding and core only need to be designed based on 400 V level.

Figure 3.4 System insulation stress analysis (a) system architecture and (b) one submodule topology detail

According to IEEE Std. C57.12.01 standard [C1], there are at least 3 dielectric tests need to be passed: basic lightning impulse test, applied voltage test and partial discharge test. Lightning impulse test should have 30 kV crest value. Low frequency applied voltage test should be test up to 12 kV RMS value. The test voltage level is determined by 4160 V application according to IEEE standard shown in Table 3.1. The third insulation test is partial discharge test. The general
procedure for partial discharge test is as follows: the voltage is raised to the pre-stress level of 1.8 times rated voltage, held for 30 seconds, and is then reduced to the voltage level equivalent to 1.3 times rated voltage and held for 3 minutes. During this 3 minutes the maximum partial discharge value can’t exceed 50 pC.

Table 3.1 Insulation test level for dry type transformer of IEEE Std. C57.12.01

<table>
<thead>
<tr>
<th>Nominal 1-L system voltages (kV)</th>
<th>Low-frequency voltage insulation level (kV rms)</th>
<th>Basic Lightning impulse insulation levels(BIL ratings) in common use kV crest(1.2*50us)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>0.25</td>
<td>2.5</td>
<td>None</td>
</tr>
<tr>
<td>1.2</td>
<td>4</td>
<td>S</td>
</tr>
<tr>
<td>2.5</td>
<td>10</td>
<td>S</td>
</tr>
<tr>
<td>5.0</td>
<td>12</td>
<td>S</td>
</tr>
<tr>
<td>8.7</td>
<td>20</td>
<td>S</td>
</tr>
<tr>
<td>15</td>
<td>34</td>
<td>S</td>
</tr>
</tbody>
</table>

In order to pass IEEE Std. C57.12.01 standard, transformer clearance distance and creep age distance should be designed based on the transformer steady state operation voltage (4160V) and transient maximum peak insulation test voltage (30 kV). According to IEC 60950 standard [C2], for 4160 V operating voltage minimum creep age distance should be at least 41.6 mm; for 30 kV peak transient voltage the minimum clearance distance should be at least 42 mm. Besides these requirements all the insulation solid material thickness like insulation tape and bobbin should all designed based on maximum transient insulation requirement 30 kV voltage level.
Three different solid insulation material for transformer bobbin are also shown in Table 3.2. PTFE is chosen as insulation bobbin material with high dielectric strength (19.7 kV/mm) [C3]. On the other hand, three different insulation tape candidates are compared in Table 3.3. 3M 8943 is chosen as dielectric tape for high dielectric strength (62.8 kV/mm) and high thermal conductivity (0.4 W/mK).

<table>
<thead>
<tr>
<th>Material Candidate</th>
<th>Dielectric Strength</th>
<th>Dielectric Constant</th>
<th>Thermal conductivity</th>
<th>High working temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTFE</td>
<td>19.7 kV/mm</td>
<td>2.1</td>
<td>0.25 W/mK</td>
<td>250°C</td>
</tr>
<tr>
<td>PC</td>
<td>15 kV/mm</td>
<td>2.9</td>
<td>0.22 W/mK</td>
<td>130°C</td>
</tr>
<tr>
<td>ABS</td>
<td>16.7 kV/mm</td>
<td>2.87</td>
<td>0.17 W/mK</td>
<td>100°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Material Candidate</th>
<th>3M 8943</th>
<th>Kapton 5413</th>
<th>Mica tape</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Strength</td>
<td>62.8 kV/mm</td>
<td>102 kV/mm</td>
<td>10 kV/mm</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>0.4 W/mK</td>
<td>0.1 W/mK</td>
<td>0.2 W/mK</td>
</tr>
<tr>
<td>Stable Temperature Range</td>
<td>-40~200°C</td>
<td>-73~260°C</td>
<td>Up to 950°C</td>
</tr>
</tbody>
</table>
Note that plastic material dielectric strength reduces when material thickness increases. Rule of thumb relationship is listed in equation (3.1) [C3]. $D_s$ is dielectric strength under specific thickness $T$, $D_{sref}$ is reference dielectric strength under reference thickness $T_{ref}$. Considering 50% margin, 45kV is chosen to determine insulation thickness calculated result is shown in Table 3.4.

$$\frac{D_s}{D_{sref}} = \left(\frac{T_{ref}}{T}\right)^{0.4} \tag{3.1}$$

<table>
<thead>
<tr>
<th>Bobbin thickness</th>
<th>4 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary insulation Tape thickness</td>
<td>1 mm (6 layers)</td>
</tr>
<tr>
<td>Secondary insulation Tape thickness</td>
<td>0.35 mm (2 layers)</td>
</tr>
<tr>
<td>Primary bobbin to core spacer</td>
<td>4 mm</td>
</tr>
<tr>
<td>Secondary bobbin to core spacer</td>
<td>1 mm</td>
</tr>
<tr>
<td>Primary bobbin to secondary bobbin spacer</td>
<td>4 mm</td>
</tr>
</tbody>
</table>

Insulation space distance should be designed to avoid air breakdown during partial discharge test. Air dielectric strength is only 3 kV/mm, considering some margin 1.5kV/mm design air electrical field is chosen. Air spacer distance between primary winding and other net part is 4 mm shown in Table 3.4. Besides this we also encapsulate primary high voltage winding with epoxy material (EPIC Resin R1055/H5083) to eliminate insulation weakness and avoid moisture and dust influence on high voltage winding insulation.

Based on previous insulation design parameters. An electric field simulation is developed in Maxwell to simulate the electric field distribution among all insulation materials. Primary side high voltage winding is connected to the high insulation test voltage 30kV. Both transformer core and secondary winding is grounded. Final simulation result is shown in Figure 3.6. We can see
within the insulation solid material (bobbin, insulation tape and encapsulating material) maximum electric field is around 5.5 kV/mm which is much smaller than dielectric strength of all insulation solid material.

Figure 3.6 Electric field simulation under 30 kV test (a) test voltage connection (b) Electric field simulation results

3.3 **Transformer magnetic loss modeling and design**

According to previous analysis, transformer insulation parameters are determined. However transformer core material and transformer turn number, core cross section area is still not clear. In this section firstly transformer core materials are compared to figure out material candidate for our 500 kHz application. Then Transformer core loss and litz wire winding loss model are presented for design procedure. Based on these loss calculation models, transformer optimal turn number can be determined by transformer total loss trade off. In the end different core loss density impact on transformer design is also analyzed based on same method. Transformer turn number and core loss density is finally determined based on trade-off between transformer loss and volume.
3.3.1 Transformer Core Material Selection

For conventional line frequency transformer, core material used mostly is silicon steel and nickel-steel both of which generate dramatic loss for high working frequency. According to literature survey in the first chapter amorphous, nanocrystalline and ferrite are three main material candidates for high frequency transformer. The main requirement for core material should be low core loss at high working frequency (tens of kilo hertz). Core loss of the three materials with swept flux density are compared at 50 kHz, 100 kHz and 200 kHz working frequency respectively shown in Figure 3.7. It is obvious that amorphous holds much higher core loss at different working flux density and different frequency. Whereas superiority between ferrite and nanocrystalline varies with different flux density and different working frequency. Two curves intersect with each other and the intersection point moves with different working frequency. Generally speaking nanocrystalline is the best candidate around 50 kHz among wide interested working area ($B_m =150\text{mT-500mT}$). When frequency is higher than 200 kHz ferrite material blue line is lower than that of nanocrystalline in most flux density region (50mT-180mT). Even through from saturation flux density point of view, ferrite holds lowest value 530mT shown in Figure 3.7. However as working frequency increases, possible working flux density is going down due to core loss density thermal limitation. For 200 kHz case, the reasonable working flux density is around 80mT-160mT which is much lower than all the material saturation flux density.

(a) Core loss comparison @50kHz  
(b) Core loss comparison @100kHz
From previous comparison we can find that MnZn ferrite is our material candidate for frequency higher than 200 kHz. There are plenty of MnZn ferrite for our 500 kHz application. Four MnZn ferrite material candidates are compared in Figure 3.8 to figure out the appropriate ferrite material. 3F36 holds lower loss comparing to other competitors and is chosen as our core material.

Figure 3.8 MnZn ferrite core loss comparison @500 kHz
3.3.2 Magnetic Core Loss and Winding Loss Model

Transformer core loss is determined by working flux waveform which is excited by input voltage. Different input voltage waveform will induce different flux flowing inside the core and finally generate different core loss. CLLC resonant converter is frequency controlled DC/DC converter with square input voltage waveform. In order calculate the core loss under such waveform excitation we need to find an appropriate core loss calculation model.

The state of art core loss calculation method is Steinmetz Equation:

\[ P_v = k \cdot f^\alpha \cdot B_m^\beta \]  \hspace{1cm} (3.2)

Where \( B_m \) is the working flux density magnitude, \( P_v \) is time average power loss per unit volume, and \( f \) is the frequency of sinusoidal excitation, and \( k, \alpha, \) and \( \beta \) are constants found by curve fitting results from core loss measurement. This method cannot be directly used in CLLC resonant converter since it is only valid for sinusoidal voltage excitation. However for CLLC resonant converter square voltage excitation waveform is added on the transformer core. An exact square voltage excitation core loss model is needed.

Rectangular Extension Steinmetz Equation (RESE) is proposed by Dr. Mu to exactly predict core loss under rectangular voltage excitation [C4]. Due to squared (\( D=0.5 \)) voltage excitation for CLLC resonant converter, the core loss calculation for CLLC resonant converter can be further simplified to (3.3). According to Dr. Mu’s paper RESE model is valid for different ferrite core materials and can be used for CLLC converter transformer core loss prediction and analysis.
\[ P_{v\_rec} = \frac{8}{\pi^2} k f^\alpha B_m^\beta \]  

(3.3)

Litz wire is used in high frequency transformer since it contains separate insulated wire strands twisted or braided together, enabling low-resistance high-current conductors at frequency up to hundreds of kilo-hertz. According to Dr. Sullivan’s method [C5], there are two assumptions to calculate the litz wire winding loss due to inherent nature of litz wire. First assumption is that the field remains constant inside each strand, equivalent to the assumption that each strand diameter is not large compared to skin depth. Second assumption is that there is no eddy current flows between different strands due to proper braided litz wire construction [C5]. Based on the assumptions above, litz wire winding loss model should consider both eddy current flowing inside each strand due to external field and conduction loss neglecting eddy current effect. The latter is easy to calculate via dc resistance of conductor, therefore this thesis focus on the former.

We assume that each litz strand’s diameter is small enough that for each small strand the external magnetic field is uniform. For a cylinder conductor in a uniform flux density, The Squared Field Derivative (SFD) method is widely used to calculate instantaneous eddy current loss shown in equation (3.4) [C5]:

\[ P_{\text{eddy}}(t) = \frac{\mu_0^2 \pi l d^4}{64 \rho_c} \left( \frac{dH(t)}{dt} \right)^2 \]  

(3.4)

Where \( l \) is cylinder conductor length, \( \rho_c \) is resistivity of wire. From equation (3.4) we know that in order to calculate each litz strand eddy current loss, its corresponding external magnetic field is necessary. Then a 2D magnetic field simulation for previous mentioned type 2 UU core transformer structure is developed, magnetic field distribution is shown in Figure 3.9.
It is obvious that the magnetic field is non-linear and irregular. It is hard to find an analytical way to calculate the external field over winding region. Therefore 3D magnetic field simulation are employed to support eddy current loss calculation. Considering each litz stand is regularly twisted and braided in the 3D winding coil. Space average magnetic field should be used for loss calculation in equation (3.5).

\[
P_{\text{eddy}}(N, t) = \sum_{j=1}^{N} N_s \cdot \frac{\mu_0 \pi l_w d_s^4}{64 \rho_c} \left\langle \left( \frac{dH(t)}{dt} \right)^2 \right\rangle_j
\]

Where \( N \) is transformer turn number, \( N_s \) is litz wire strand number, \( l_w \) is length per turn, \( \left\langle \cdot \right\rangle_j \) is space average calculator over j turn winding. There is still two dependent variable \( N \) and \( t \).

From time domain point of view, the magnetic field is a quasi-sinusoidal shape and since then we assume it is sinusoidal shape and time average eddy current loss calculation is give below in (3.6)
Where \( H_m \) is peak magnetic field value for external field under peak excitation current, \( \bar{I} \) is time average calculation over whole cycle. Based on this equation static 3D magnetic field simulation result can be used to calculate litz wire winding eddy current loss. Winding working current conduction loss can also be calculated easily by equation (3.7). Finally total winding loss can be calculated by summation of equation (3.6) and (3.7) shown in expression (3.8). Note that there is only one dependent variable that is transformer turn number \( N \).

\[
P_{\text{eddy}} (N) = \sum_{j=1}^{Nc} N_s \cdot \frac{\mu_0^2 \pi l w d_s^4}{64 \rho_c} \left( \frac{dH_m \sin(wt)}{dt} \right)_j^2 (3.6)
\]

\[
P_{\text{non-eddy}} (N) = \frac{4 \rho_c N w l^2}{N_s \pi^2 d_s^2} I_{rms}^2 \quad (3.7)
\]

\[
P_{\text{winding}} (N) = \sum_{j=1}^{Nc} N_s \cdot \frac{\mu_0^2 \pi l w d_s^4}{64 \rho_c} \left( \frac{dH_m \sin(wt)}{dt} \right)_j^2 + \frac{4 \rho_c N w l^2}{N_s \pi^2 d_s^2} I_{rms}^2 \quad (3.8)
\]

Sample transformer is built to verify litz wire loss calculation method. The transformer turn number is 12:6, litz wire strand AWG is 44 and total strands number is 180. Agilent impedance analyzer is used to test AC resistance between terminals of primary winding with secondary winding shorted. By shorting the secondary winding excitation flux is almost zero and core loss can be neglected in the AC resistance test result. Based on 5A working current litz wire winding loss test result can easily be calculated by \( I^2 R \) equation, model calculation result can also be easily obtained by equation (3.8). The experiment test result (blue curve) is consistent with model calculation result (red curve) among interested frequency range shown in Figure 3.10.
3.3.3 Transformer Design and Development

Based on previous two magnetic loss calculation model, transformer optimal design can be developed. Litz wire strand AWG 44 (diameter 51um) is chosen since it is enough small considering 500 kHz skin depth 92um. According to National electrical code, litz wire strand number around $N_s=825$ is chosen for 15kW 21A RMS current application [C6]. The initial design core loss density is chosen as $P_v=300$ kW/m$^3$. Because there is only one dependent variable for both core loss and winding loss calculation which is transformer turn number N, then transformer core loss and winding loss with swept transformer turn number is plotted in Fig 3.11. Core loss decrease with increasing transformer turn number because larger turn number gives smaller transformer section area and smaller total transformer volume. Under certain core loss density condition, the core loss will decrease with reducing across section area. At same time larger
transformer turn number will increase total transformer winding length which resulting in higher winding loss. Finally summation of both core loss and winding loss contribute to transformer total loss U shape curve can be plot shown in Figure 3.11. The valley region holding lowest total loss is preferred.

![Figure 3.11 Transformer loss vs transformer turn number N](image)

Considering core loss density \( (P_v) \) impact, \( P_v \) is swept from 100 to 800 kW/m\(^3\) and transformer total loss vs transformer volume relationship is plotted in Figure 3.12. Each mark within the curve represent one specific transformer turn number design point and each curve share one same core loss density value. Considering our design target is smaller transformer total loss and smaller transformer volume, for each curve optimal design point should locate around the corner region. Therefore optimal design point for each curve can be found and marked with red dot. Relationship between these optimal design points clearly show transformer design trade-off between volume and total loss. As core loss density increases optimized transformer volume decreases, however optimal transformer total loss increases with increasing core loss density. Final design point \( (N=12, P_v=300) \) locate around the corner region as the trade-off between volume
and total loss shown in Figure 3.12. Transformer design parameters are summarized and shown in Table 3.5. Note that transformer magnetizing inductance is determined in chapter 2 for corresponding device ZVS requirement.

![Figure 3.12 Transformer core loss density ($P_v$) impact on transformer design](image)

**Table 3.5 Medium voltage high frequency transformer design parameter**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working Frequency($f_s$)</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Core Material</td>
<td>3F36</td>
</tr>
<tr>
<td>Core loss density($P_v$)</td>
<td>300 kW/m$^3$</td>
</tr>
<tr>
<td>Strand AWG</td>
<td>44</td>
</tr>
<tr>
<td>Litz wire stand number($N_s$)</td>
<td>825</td>
</tr>
<tr>
<td>Turn Number($N$)</td>
<td>12</td>
</tr>
<tr>
<td>Winding loss</td>
<td>36 W</td>
</tr>
<tr>
<td>Core loss</td>
<td>38 W</td>
</tr>
<tr>
<td>Transformer volume</td>
<td>1.02 Liter</td>
</tr>
<tr>
<td>Magnetizing inductance</td>
<td>28 uH</td>
</tr>
</tbody>
</table>

Based on above transformer design parameters shown in Table 3.5, medium voltage high frequency transformer prototype is developed shown in Figure 3.13. Note that dimension marked
includes mechanical fixture. Transformer gap value is determined by transformer magnetizing inductance. After transformer prototype is built up, parasitic leakage inductance and magnetizing inductance are measured and shown in Table 3.6. Then definition of each parasitic inductance is shown in Figure 3.14. At same time 3D FEA simulation results of leakage inductance and magnetizing inductance is also shown in Table 3.6. The prototype test results hold reasonable deviation from simulation value considering test terminal influence.

<table>
<thead>
<tr>
<th>Parasitic parameters</th>
<th>Prototype Test</th>
<th>3D FEA Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing Inductance(L_m)</td>
<td>27.78(\mu)H</td>
<td>28(\mu)H</td>
</tr>
<tr>
<td>Primary Leakage Inductance(L_{rp})</td>
<td>6.76(\mu)H</td>
<td>6.1(\mu)H</td>
</tr>
<tr>
<td>Secondary Leakage Inductance 1(L_{rs1})</td>
<td>4.33(\mu)H</td>
<td>3.6(\mu)H</td>
</tr>
<tr>
<td>Secondary Leakage Inductance 2(L_{rs2})</td>
<td>4.26(\mu)H</td>
<td>3.6(\mu)H</td>
</tr>
</tbody>
</table>

Figure 3.13 Medium voltage 500 kHz transformer prototype (a) overview (b) top view

Table 3.6 Transformer parasitic test result
3.4 Medium Voltage Transformer Insulation Test

After transformer prototype is built up, since our application is 4160 V medium voltage, insulation safety should be our first concern. In order to verify transformer insulation capability for 4160 V medium voltage application, the transformer prototype is tested under previous mentioned IEEE Std. C57.12.01 insulation standard. Three insulation test is conducted including basic lightning insulation test, applied voltage insulation test, partial discharge insulation test all of which will be talked about in the following separately.

As insulation requirement mentioned above, according to IEEE Std. C57.12.01, for 4160 V application transformer the basic lightning insulation test should be at least 30 kV. The basic lightning test equivalent circuit is shown in Figure 3.15. The voltage waveform is also presented in Figure 3.15. Within 1.2us the test voltage should be increased to 30kV peak value and gradually go down to half of peak value at 50us. During the test if the test voltage waveform is smooth and no collapse happens during the waveform going down. This means the transformer passes this lightning test.
Figure 3.15 (a) Basic lightning test equivalent connection circuit and (b) required test waveforms

Then the transformer is tested under previous mentioned condition which is shown in Figure 3.16, testing waveform is also presented. It is obvious that the test waveform meets the requirement and shapes smoothly going down. Blue and red curves represent two independent test results. Two test waveforms agree with each other and overlap very well. Based on these test results, we conclude that our transformer passes the basic lightning insulation test.
Figure 3.16 (a) Transformer basic lightning insulation test setup and (b) Impulse test waveform

The second insulation test is applied voltage test. During this test both transformer low voltage coil and transformer cores are all grounded. Primary high voltage coil is firstly shorted and then added 12 kV RMS line frequency medium voltage, connection is shown in Figure 3.17. The test condition is referred IEEE standard. After the test voltage is increased to 12 kV, the test voltage
is hold for 60 seconds and during this time there should be no flash over, spark over or puncture. During our 1 minute test, the transformer insulation is stable without any insulation failure. The trigger threshold leakage current is 75 mA, it is not triggered during the test. For this test we need one step up transformer to generate 12 kV medium voltage and voltage divider for test voltage sensing shown in Figure 3.17. Finally transformer prototype passes the applied voltage insulation test.

![Equivalent Connection Circuit](image)

**Figure 3.17** (a) Transformer under applied voltage test and (b) equivalent connection circuit

The third insulation test is partial discharge test. Partial discharges occur when the local electric field intensity exceeds the dielectric strength of the dielectric involved, resulting in local ionization and breakdown. Protracted partial discharge can erode solid insulation and eventually lead to breakdown of insulation. Partial discharge test equivalent circuit is same as previous applied voltage test, however only one more equipment is added that is partial discharge measurement unit shown in Figure 3.18. This unit can measure the transformer dynamic partial
discharge value during the whole test process. Firstly the test voltage is increased to 1.8 times rated working voltage (7.4 kV for 4160V application) and held for 30 seconds and then reduced to 1.3 times rated working voltage (5.4kV for 4160V application). The test voltage should keep 5.4kV for 3 minutes, during this period the measured partial discharge value should be below 50pC. The test voltage waveform requirement is shown in Figure 3.19. The transformer partial discharge test result is 3.8 pC which is much smaller than that of IEEE standard requirement.

Figure 3.18 (a) Transformer under partial discharge test and (b) equivalent connection circuit
We summarize all the three insulation test condition, standard requirement and test results in Table 3.7. The medium voltage transformer prototype passes all the three tests and is verified to work under 4160V system input voltage according to IEEE standard.

Table 3.7 Medium voltage transformer insulation test summary

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Standard Requirement</th>
<th>Test Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impulse Voltage (BIL) Testing</td>
<td>30 kV peak impulse (50us/1.2us) voltage added on the transformer</td>
<td>Smooth test waveform w/o collapse and two times test waveform overlaps</td>
</tr>
<tr>
<td>Applied Voltage Testing</td>
<td>12 kV RMS line frequency voltage added on transformer for 60 s</td>
<td>No voltage collapse happens during test</td>
</tr>
<tr>
<td>Partial Discharge(PD) Test</td>
<td>5.4 kV RMS line frequency voltage added on transformer for 180 s</td>
<td>Partial Discharge intensity should be below 50 pC</td>
</tr>
</tbody>
</table>

3.5 Working Frequency Impact on Transformer Design

In order to analyze the working frequency impact on transformer magnetic design, same analysis method is utilized as presented in the core loss density ($P_v$) impact analysis. However this time the design variable is working frequency. We need to note that under different working
frequency litz wire strand AWG should be different. Higher working frequency comes with lower skin depth value, the corresponding litz wire AWG value should be larger and strand diameter should be smaller shown in Figure 3.20. In order to make a reasonable comparison we assume the ratio between strand diameter and skin depth to be around 0.54 and corresponding litz wire strand AWG for different working frequency is shown in Table 3.8. Of course the total conduction area of different working frequency case is still the same around 1.65 mm² mentioned above.

![Figure 3.20 Litz wire strand diameter over different AWG](image-url)

Figure 3.20 Litz wire strand diameter over different AWG
### Table 3.8 Single wire AWG selection over different working frequency

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Skin depth</th>
<th>AWG</th>
<th>ds/6</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 kHz</td>
<td>147 um</td>
<td>40</td>
<td>0.54</td>
</tr>
<tr>
<td>300 kHz</td>
<td>119 um</td>
<td>42</td>
<td>0.53</td>
</tr>
<tr>
<td>400 kHz</td>
<td>104 um</td>
<td>43</td>
<td>0.54</td>
</tr>
<tr>
<td>500 kHz</td>
<td>92 um</td>
<td>44</td>
<td>0.55</td>
</tr>
<tr>
<td>600 kHz</td>
<td>85 um</td>
<td>45</td>
<td>0.54</td>
</tr>
<tr>
<td>700 kHz</td>
<td>78 um</td>
<td>46</td>
<td>0.52</td>
</tr>
<tr>
<td>800 kHz</td>
<td>73 um</td>
<td>46</td>
<td>0.55</td>
</tr>
<tr>
<td>1 MHz</td>
<td>66 um</td>
<td>47</td>
<td>0.54</td>
</tr>
</tbody>
</table>

Under same core loss density (300 kW/m³), same total winding conduction area (1.65 mm²) and same core material (3F36) we can plot transformer design curve (Volume VS total transformer loss) in Figure 3.21(a). As mentioned above design point closer to the corner holds better performance as the trade-off between transformer volume and total transformer loss. Each mark represent one specific transformer turn number design point. For each working frequency we can pick up one optimal design point and plot it in the Figure 3.21(b), it is obvious that under 3F36 core material and $P_v=300$ kW/m³ condition transformer volume diminishing return happens at 400 kHz and total transformer loss begin to rebound after 400 kHz.
Figure 3.21 Working frequency impact on transformer design for 3F36 material and \( P_v = 300 \text{ kW/m}^3 \)

If the flux density is changed to 500 kW/m\(^3\) for same 3F36 material the corresponding design curves over different working frequency is shown in Figure 3.22(a). Following the same method the optimal design point of different working frequency is plotted in Figure 3.22(b). It is found transformer volume does show a diminishing return behavior after 400 kHz and transformer and total loss still rebounds after 400 kHz.
We also need to note that the optimal working frequency of different core material is also different. If the core material is changed from 3F36 to 3C98 then following the same method transformer design curves of 3C98 material are plotted over different working frequency under $P_v = 300\ \text{kW/m}^3$ shown in Figure 3.23. It obvious that both transformer volume and transformer total loss rebound after 300kHz which means that the optimal working frequency of 3C98 should be around 300kHz.

![Transformer design curve over different $f_s$](image1)

![Optimal design point over different $f_s$](image2)

Figure 3.23 Working frequency impact on transformer design for 3C98 material and $P_v=300\ \text{kW/m}^3$

If we consider another material ML95S which is designed for higher working frequency range. Follow the same way transformer design curves are plotted under $P_v = 300\ \text{kW/m}^3$ shown in Figure 3.24. It is found that transformer volume shows diminishing return after 1 MHz and transformer total loss rebounds back after 800 kHz. Therefore for ML95S material, the optimal working frequency range is around 800 kHz~1MHz.
Figure 3.24 Working frequency impact on transformer design for ML95S material and $P_v=300 \text{ kW/m}^3$

Based on previous optimal design data comparison between three transformer materials 3F36, 3C98 and ML95S under same core loss density $P_v=300 \text{ kW/m}^3$ over different working frequency is shown in Figure 3.25. From transformer loss point of view we can find that 3C98 is better than 3F36 up to 300 kHz and two curves intersect with each other between 300 kHz and 400 kHz. After 400 kHz 3F36 shown its advantage over 3C98. After 500 kHz ML95S takes over and shows better performance up to 800 kHz then ML95S reaches its valley point and rebound back. From transformer volume point of view, phenomenon is similar 200 kHz and 300 kHz we can get smaller transformer volume by using 3C98 material however after 400 kHz 3F36 shows its benefit to continue reduce transformer volume. After 500 kHz ML95S takes over and continue to reduce transformer size up to 1MHz. It is obvious that pushing higher working frequency the transformer size is still shrinking however under different working frequency different core material should be chosen.
Figure 3.25 3F36 vs 3C98 vs ML95S in terms of transformer loss and volume @different frequency
Chapter 4 CLLC Resonant Converter Design and Experiment Test

This chapter CLLC resonant converter circuit will be developed based on the transformer design results. Overall 15kW CLLC resonant converter prototype structure is shown in Figure 4.1. TMS320F28075 is chosen as main controller. Considering multilevel converter with large module number and immunity to external inference to the signal during distribution, fiber optic connection is used for PWM gate signal and system fault signal. Therefore main controller is connected to a fiber interface board first and then PWM gate signal and fault signal are distributed to power stage by fiber optics. 1200 V SiC MOSFET gate drive is the crucial circuit in overall power stage which will be mainly introduced in this chapter. Finally 15 kW 500 kHz CLLC converter working waveform and efficiency are also presented which meets our design requirement.

Figure 4.1 15 kW CLLC converter hardware architecture
4.1 Drive Circuit Design and Test

Pushing 500 kHz working frequency for DC/DC stage primary side 1.2kV SiC MOSFET gate drive is one crucial challenge. Firstly for such high working frequency, a small gate driver propagation delay mismatch between rising edge and falling edge will result in large duty cycle deviation shown in Figure 4.2. For case 1 delay of rising edge is smaller than that of falling edge which results in larger driver output duty cycle comparing to command signal. Case 2 holds higher propagation delay of rising edge comparing to falling edge, gate driver output duty cycle is reduced comparing to command signal. When the working frequency increases, the total effective duty cycle period is shorter, the time mismatch influence will be more severe. The ideal case is case 3 which holds equal propagation delay of rising edge and falling edge. The duty cycle is exactly generated without deviation.

![Diagram of gate driver propagation delay mismatch](image)

Figure 4.2 Gate driver propagation delay mismatch effect analysis

In order to achieve equal propagation delay, gate driver IC selection is very critical for time delay consideration. Different driver IC chips are compared in Table 4.1 in terms of propagation delay, common mode noise immunity and insulation capability [D1-D7]. Analog Device product
ADUM4135 is finally chosen as our driver IC candidate due to its short and equal propagation delay which is only 55ns and high common mode 100V/ns dv/dt immunity that is very crucial for our high frequency fast switching characteristic.

| Manufacturer | Part No. | $t_{PLH}$ | $t_{PHL}$ | $|t_{PLH}-t_{PHL}|$ | Load Condition | Coupling Cap | Transient vol. Rating (V$_{IOTM}$) | dv/dt immunity |
|--------------|----------|----------|----------|----------------|----------------|-------------|----------------------------------|----------------|
| Avago        | ACPL-335J | 110ns    | 150ns    | 40ns           | $C_g=1nF$ $R_g=10Ω$ $ΔV=13V$ | NA          | 8000V                            | > 50V/ns        |
| Avago        | ACPL-333J | 180ns    | 180ns    | 20ns           | $C_g=10nF$ $R_g=10Ω$ $ΔV=30V$ | 1.3 pF      | 8000V                            | >15V/ns         |
| Toshiba      | TLP5214  | 85ns     | 90ns     | 5ns            | $C_g=25nF$ $R_g=10Ω$ $ΔV=30V$ | 1 pF        | 5000V                            | >35V/ns         |
| Infenion     | 1ED02012FA2 | 170ns   | 165ns    | 5ns            | $C_g=100pF$ $R_g=10Ω$ $ΔV=23V$ | NA          | 6000V                            | <50 V/ns         |
| Analog Device| ADUM4135  | 55ns     | 55ns     | 0ns            | $C_g=2nF$ $R_g=3.9Ω$ $ΔV=15V$ | 2 pF        | 8000V                            | >100 V/ns        |
| Texas Instrument | ISO5452  | 76ns     | 76ns     | 0ns            | $C_g=1nF$ $R_g=0Ω$ $ΔV=30V$ | 2 pF        | 8000 V                           | >50 V/ns         |
| Rohm         | 8M6104FV-C | 115ns    | 115ns    | 0ns            | NA             | NA          | 2500V                            | >100 V/ns        |

As mentioned above fiber optics are used to distribution PWM signal, the transmitter and receiver of fiber optics also generate 30ns delay respectively, and the current booster of driver IC also generate 50ns propagation delay. All of these delay time is symmetrical for both rising and falling edge. Therefore total delay from command signal to driver output can be calculated in equation (4.1). The driver output delay is tested in final hardware and the waveform is shown in Figure 4.3. It is obvious that the total propagation delay for rising edge and falling edge is symmetrical and total time is around 168~169ns which agree with our calculation result.

$$t_{delay\_total} = t_{trans} + t_{recei} + t_{driver} + t_{booster} = 30 + 30 + 55 + 50 = 165 \text{ns}$$ (4.1)
For the DC/DC stage CLLC resonant convert is employed to achieve ZVS of switches to eliminate turn on loss. It only holds small turn off loss due to low turn off current. Lower gate resistor is preferred to reduce switch turn off loss. Zero external turn off gate resistor is preferred. The gate driver loop need to be minimized in order to reduce gate resistor without causing resonant and failure. Under such low turn off resistor, high $dv/dt$ is generated with severe interference to the driver circuit. So high common mode noise immunity driver IC is required.

Besides interference to its own driver primary side signal, high $dv/dt$ generated by one switch will also generate interference to the driver output of its half bridge counterpart which is caused by SiC MOSFET parasitic capacitance $C_{rss}$ ($C_{gd}$). This phenomenon is called cross talk shown in Figure 4.4. When the high switch is turning on, a rising $dv/dt$ will be generated at the switch node D2 which will generated a current through $C_{rss}$ of low side device, this current go through low side turn off drive pass generate voltage along loop inductance and turn off gate resistor. The gate voltage of low side device can be calculated by equation (4.2). From the equation we can find that positive induction voltage is generated at low side device if this positive voltage
is large enough to make the gate voltage higher than that of device threshold value then low side device will be turned on to generate a shoot through of this half bridge and break devices. When the high switch is turning off, a falling $dv/dt$ will be generated at the switch node D2 which will generate a current through $C_{rss}$ of low side device similar to previous case but the current direction is reversed. The gate voltage of low side device can be calculated by equation (4.3). From the equation it is found that negative induction voltage is generated at low side device if this negative voltage is large enough to exceed device limitation then the device will also be broken. In order to get rid of these dangerous situation, we need to optimize gate drive circuit design from three aspects firstly negative -4V is chosen as turn off gate drive voltage to give us wider operation range during cross talk period considering the threshold voltage of device is 3.2V and maximum negative voltage is -15V; secondly zero external turn off resistor should be chosen to eliminate $V_{R\_OFF}$ in equation (4.2) and (4.3); thirdly turn off loop inductance should be minimized to reduce $V_{L1}$ and $V_{L2}$ value in two equations.

\[
V_{GS\_LOW} = -4V + V_{R\_OFF} + V_{L1} + V_{L2} \tag{4.2}
\]

\[
V_{GS\_LOW} = -4V - V_{R\_OFF} - V_{L1} - V_{L2} \tag{4.3}
\]
Figure 4.4 Cross talk phenomenon when high side switch (a) turn on and (b) turn off

In some applications, active miller clamp technology is used to restrict cross talk phenomenon shown in Figure 4.5. Instead of gate drive loop, by adding an external miller clamp branch as close as possible to the device gate terminal, miller current due to \( \frac{dv}{dt} \) will go through this miller clamp branch instead of previous gate drive loop. This method is useful when there is large turn off resistor. However in our 500 kHz high frequency operation zero turn off resistor is really critical from reducing turn off loss and increasing efficiency point of view. On the other hand miller clamp branch should be as close as possible to the device occupying valuable space around gate terminal which means gate drive loop have to sacrifice to get a longer drive loop. Moreover, the miller clamp switch will also increase device driving power. All in all for our high frequency fast switching converter miller clamp can be directly replaced by zero turn off resistor and minimized gate drive loop.
In order to minimize gate drive loop inductance, vertical laminated gate drive circuit is utilized shown in Figure 4.6. For device turn on loop gate drive current will go out from gate driver and go into turn on resistors and then go through board to device gate terminal; after going out from device source terminal the current will go back to driver decoupling capacitors. For device turn off loop is just reverse to turn on process, however turn on resistor is replaced with diode to achieve zero turn off resistance. The vertical laminated structure holds only one small vertical loop through board via. Total gate loop inductance simulation value is around 2.24 nH.
Another gate drive design challenge is device shoot through protection. We refer to [D5, D8] desaturation protection is utilized for our 1.2kV SiC MOSFET. Operating principle of desaturation protection can be explained through Figure 4.7. Instead of directly measuring device current, device $V_{ds}$ is sensed and compared to threshold to determine whether shoot through happens. As shown in Figure 4.7, when device is turned off by command signal desaturation protection is disabled. When device is turned on desaturation protection is enabled. Considering there is some $V_{ds}$ resonant over shooting when switch is turned on transient, in order to eliminate fault trigger a blank time mechanism is achieved by blanking capacitor $C_{\text{blank}}$. During blanking time device $V_{ds}$ touch threshold will not trigger the desaturation protection. The blanking time can be calculated by equation (4.4). $I_{\text{source}}$ is current value of internal current source inside gate driver IC. When device is turned on this small current will go through device and sensed terminal voltage $V_{\text{desat}}$ can be calculated by equation (4.5). When shoot through happens the high voltage of device $V_{ds}$ will block the current going through previous branch, instead the current will go into $C_{\text{blank}}$ and
gradually increase the $V_{\text{desat}}$ pin voltage, when this voltage touch threshold voltage (9.2V for ADUM4135) desaturation protection is triggered and after $t_{\text{desat}}$ time gate voltage is forced to low logic and after $t_{\text{digx}}$ time driver IC primary fault signal is forced to low logic to report a fault to upper controller.

$$\text{Blanktime} = \frac{C_{\text{blank}} \cdot V_{\text{th}}}{I_{\text{source}}}$$  \hspace{1cm} (4.4)\\

$$V_{\text{desat}} = V_{\text{ds}} + V_{\text{diode}} + V_{\text{zener}}$$  \hspace{1cm} (4.5)

Figure 4.7 (a) Desaturation protection equivalent circuit and (b) working waveform

The purpose of diode in desaturation brand is to block high DC 800V voltage when device is turned off. Its performance determines the performance of desaturation protection, high voltage blocking capability, small coupling capacitance and fast reverse recovery capability is required for this diode. The purpose of resistor $R_{\text{desat}}$ is to constrain current going out of IC driver chip according to [D8]. A large instantaneous forward voltage transient which exceeds the nominal forward voltage of the diode which may result in a large negative voltage spike on the DESAT pin which will draw a substantial amount of current out of the driver. To limit the current level drawn
from the gate driver, a DESAT resistor can be added (100 recommended) in series with the DESAT diode. The added resistor will not appreciably alter the DESAT threshold or the blanking time. The zener diode function is to adjust threshold voltage value shown in equation (4.5). According to device IV curve shown Figure 4.8, 1.5V $V_{ds}$ protection value is chosen as trade-off between protection speed and sensitivity. Since the device IV characteristic is influenced by temperature, the shoot through protection current threshold is also varying among different working temperature. 56A for 25°C and 36A for 175°C. Based on $V_{ds}$ protection value, zener diode zener voltage can be calculated by equation (4.5).

![Figure 4.8 GE 1200 V SiC MOSFET IV Curve @Vgs=20 V](image)

Desaturation protection function test waveform is also shown in Figure 4.9 with both whole waveform and zoom in details. Inductive load is used to do this test. When the device is turned on DC voltage is added on the inductor and current increases linearly. When it touches protected value 56 A then protection is triggered, within 200ns device gate is forced to low and after less than 500ns the fault pin of driver IC is dropped to low reporting the fault status to higher level controller.
Figure 4.9 Desaturation protection test result (a) whole waveform and (b) zoomed in waveform
4.2 500 kHz 15kW CLLC Resonant Converter Test

Finally 500 kHz 15kW CLLC resonant Converter is developed based on previous gate drive circuit design and high frequency medium voltage transformer shown in Figure 4.10. The power density reaches 48 kW/in³ which is very high comparing to industry state of art product. Detailed test waveform and efficiency will be present in next section.

![Figure 4.10 500 kHz 15 kW CLLC resonant converter prototype hardware](image)

Resonant tank capacitor value can be calculated based on previous transformer leakage inductance parasitic test result. Primary side resonant capacitor value is 14.7 nF and secondary
side is 22.8 nF for each output set. During the test converter input DC voltage is increased gradually, ZVS is achieved after 200V DC input voltage. After DC voltage increase to 800V target value, we gradually increase converter power level, we totally test four power level points including 4kW, 8.4kW, 11kW and 15kW. The working waveform of these four condition are shown in Figure 4.11(a) ~ (d). The dead time is around 80ns as we analyzed in chapter 2 and turn off current is around 12A.

(a) Primary voltage 800 V and output power 4 kW 1μs/div

(b) Primary voltage 800 V and output power 8.4 kW 1μs/div
In order to achieve high efficiency power conversion secondary side GaN device need to work at synchronize rectifier mode. Conduction time of the device channel should to be maximized in order to reduce device conduction loss. After fine tune secondary side SR the highest efficiency we can achieve is presented in Figure 4.12. Then peak efficiency at around half load is 98% which is much higher than that of state of art efficiency mentioned in chapter 1. The loss breakdown at peak efficiency point is shown in Error! Reference source not found.
Figure 4.12 500 kHz CLLC resonant converter efficiency test result
Chapter 5 Summary and Future work

High frequency isolated AC/DC system is proposed in this thesis to replace traditional line frequency transformer isolated method to improve total system power density and achieve medium voltage (4160 V) distribution outside server hall and DC 400 V distribution within server hall. Based on this distribution method total system efficiency can be improved by 11% comparing to traditional method. The DC/DC stage is the key element in overall system in terms of power density and insulation point of view. A series literature survey is presented to illustrate the developing trend in this research area in terms of transformer design, device selection and circuit topology selection. This thesis focus on 15 kW 500 kHz DC/DC converter including topology comparison, device characterization, transformer insulation design and magnetic loss analysis.

State of art wide band gap device including SiC and GaN devices are characterized and compared, final selection is determined based on comparison result. Mostly used high frequency high power DC/DC converter topology dual active bridge (DAB) is introduced and compared with novel CLLC resonant converter in terms of switching loss and conduction loss point of view. CLLC holds ZVS capability over all load range and relative small turn off current value. This is beneficial for high frequency operation and taken as our candidate.

Medium voltage high frequency transformer is the most important element in CLLC resonant converter. Two mostly used transformer structures UU type and EE type are compared, UU is chosen as our core structure candidate due to lower leakage inductance and small resonant capacitor voltage stress. Then transformer insulation requirement is referred for 4160 V application according to IEEE standard. Solid insulation material are also compared and selected. Material thickness and insulation distance are also determined based on IEC insulation standard. Based on
insulation parameter derived from previous insulation analysis, two transformer magnetic loss model are introduced including core loss model and litz wire winding loss model. Transformer turn number is determined based on core loss and winding loss trade-off. Transformer prototype is developed following designed parameter. The developed 15 kW 500 kHz transformer is tested under 4160 V dry type transformer IEEE Std. C57.12.01 standard requirement condition including basic lightning test, applied voltage test, partial discharge test. The prototype passed all the three tests and insulation capability is verified. Different working frequency impact on transformer design is also analyzed, 400 kHz is found to be the best working frequency for 3F36 material. Different material’s optimal working frequency is also different. By pushing higher working frequency transformer size can still be reduced however under different working frequency different transformer core material should be employed and transformer volume reduction diminishing return does exist.

500 kHz 15 kW CLLC converter gate drive is our design challenge in terms of symmetry propagation delay, cross talk phenomenon elimination and shoot through protection. Gate drive IC is carefully selected to achieve symmetrical propagation delay and high common mode dv/dt immunity. Zero turn off resistor is achieved with minimized gate loop inductance design to prevent cross talk phenomenon. Desaturation protection is also employed to provide shoot through protection. Finally 15 kW 500 kHz CLLC resonant converter is also developed based on previous mentioned transformer prototype and drive circuit. Converter is tested up to full power level with 98% peak efficiency.

To further extend the depth for this research area, the following topics may be continued:
1) With the newly developed wide band gap device the die size of the device is getting larger and larger which can reduce the device $R_{ds(on)}$ obviously. In the future newly developed 1200 V and 600 V level SiC and GaN devices can be applied to our converter to further increase converter efficiency and power level.

2) The DC/DC stage starts up with huge resonant tank stress without specific control. Soft startup method based on state trajectory plane analysis is fit for this application, it should combine with the control of AC/DC cascaded H bridge stage. The system level control for overall system can be further researched in the future.

3) From magnetic point of view, more transformer structure and insulation method like oil immerse should be analyzed to compare with our current design result in terms of insulation capability and power density to make improvement. Moreover newly developed core material like ML95S can also be employed to replace current core material to further reduce core loss and core volume.
Reference


[A30] Xu She; Fei Wang; Burgos, R.; Huang, A.Q., "Solid state transformer interfaced wind energy system with integrated active power transfer, reactive power compensation and voltage conversion


[C2] IEC 60950 “Safety of information technology equipment”


[C6] NFPA 70 National Electrical Code 2014 Edition. Table 310.15(B)(16) (formerly Table 310.16) page 70-161

[D1] ACPL-335J, 2.5 Amp MOSFET Gate Drive Optocoupler with Integrated Desat Over Current Sensing, Active Miller Current Clamping, FAULT and UVLO Status Feedback, Data sheet, Avago Technologies.


[D6] ISO5452 High-CMTI 2.5-A / 5-A Isolated IGBT, MOSFET Gate Driver with Split Outputs and Active Safety Features, Data sheet, Texas Instrument.
