
Modeling and Control Strategy for Capacitor Minimization of Modular Multilevel Converters

Yadong Lyu

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Fred C. Lee Chair

Qiang Li Co-Chair

Dong S. Ha

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(Abstract)

The modular multi-level converter (MMC) is the most prominent interface converter used between the HVDC grid and the HVAC grid. One of the important design challenges in MMC is to reduce the capacitor size. In the current practice, a rather large capacitor bank is required to store line-frequency related circulating energy, even though a number of control strategies have been introduced to reduce the capacitor voltage ripples. In the present paper, a novel control strategy is proposed by means of harmonic injections in conjunction with gain control to completely eliminate both the line frequency and the second-order harmonic of the capacitor voltage ripple. Ideally, the proposed method works with the full bridge topology. However, the concept also works with half bridge topology with a significant reduction of line frequency related ripple. To gain a better understanding of the nature of circulating energy and the means of reducing it, the method of state plane analysis is employed to offer visual support. In addition, the design trade-off between full bridge MMC and half bridge MMC is presented and a novel control strategy for a hybrid MMC is proposed. Finally, the work is supported with a scaled down hardware demonstration.

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(General Audience Abstract)

The modular multi-level converter (MMC) is the most prominent interface converter used between the HVDC grid and the HVAC grid. One of the important design challenges in MMC is to reduce the capacitor size. In the current practice, a rather large capacitor bank is required by the commonly used control strategy. The large capacitor bank increases the cost and the space of the MMC system. In the present paper, a novel control strategy is proposed to significantly reduce the capacitor bank in the system. Ideally, the proposed method works with the full bridge topology. However, the concept also works with half bridge topology with a significant reduction of capacitor bank. To gain a better understanding of the nature of the operating principles of capacitors, the method of state plane analysis is employed to offer visual support. In addition, the design trade-off between full bridge MMC and half bridge MMC is presented and a novel control strategy for a hybrid MMC is proposed. Finally, the work is supported with a scaled down hardware demonstration.

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Chapter 1 Introduction

1.1. Background and History

Nowadays, power electronics is playing an important role in the high power applications, especially in the electric power systems. There is increasing interest in generating electrical power from a renewable source: wind power systems and solar systems. However, some renewable sources are located a far distance from the electric power customers. For long-distance transmission, the high-voltage, direct current (HVDC) electric power transmission system has been proven to be less expensive and suffer lower electrical losses than the common alternating current (AC) system [1]. The integration between these high-voltage DC grids and the existing AC grids is a significant technical challenge. The multilevel converter is the most prominent solution to this challenge.

One family of multilevel converter is the diode-clamped (neutral-clamped) converter [2] and the capacitor-clamped (flying capacitors) converter [3]. The diode-clamped converter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter where the mid-voltage level was defined as the neutral point. A three-level NPC topology shown in Fig. 1. 1, is widely used in the industry.

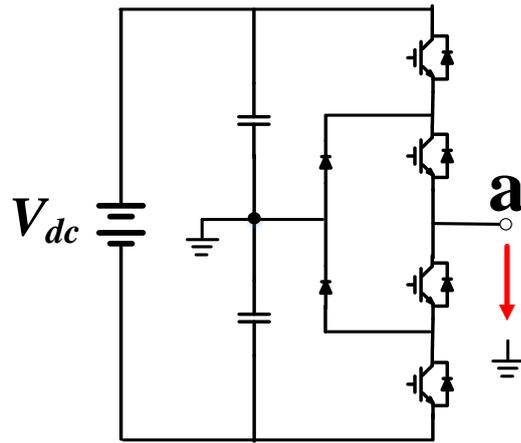


Fig. 1. 1 Three-level NPC topology

However, the topology would be way too complicated if the number of voltage levels increases, as Fig. 1. 2 shows a 5-level NPC topology [4]. The NPC topologies with high voltage levels are not practical in the industry.

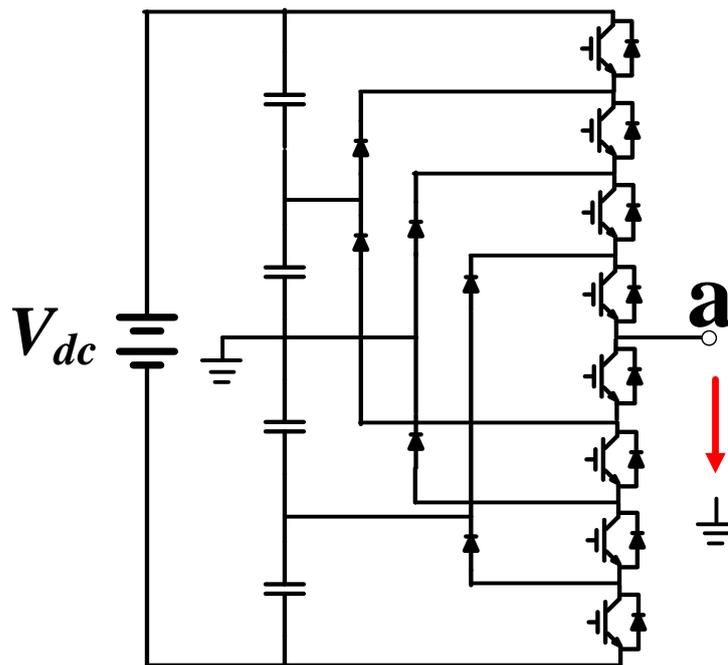


Fig. 1. 2 Five-level NPC topology

Another family of multilevel converter is the modular-type multilevel converter. The concept of cascaded modules is utilized to deal with high voltage within standardized modules. The module topology is usually full bridge topology or half

bridge topology. The first type of modular converter was introduced in [5], as shown in Fig. 1. 3. It required an independent DC power supply to generate stair-step waveforms.

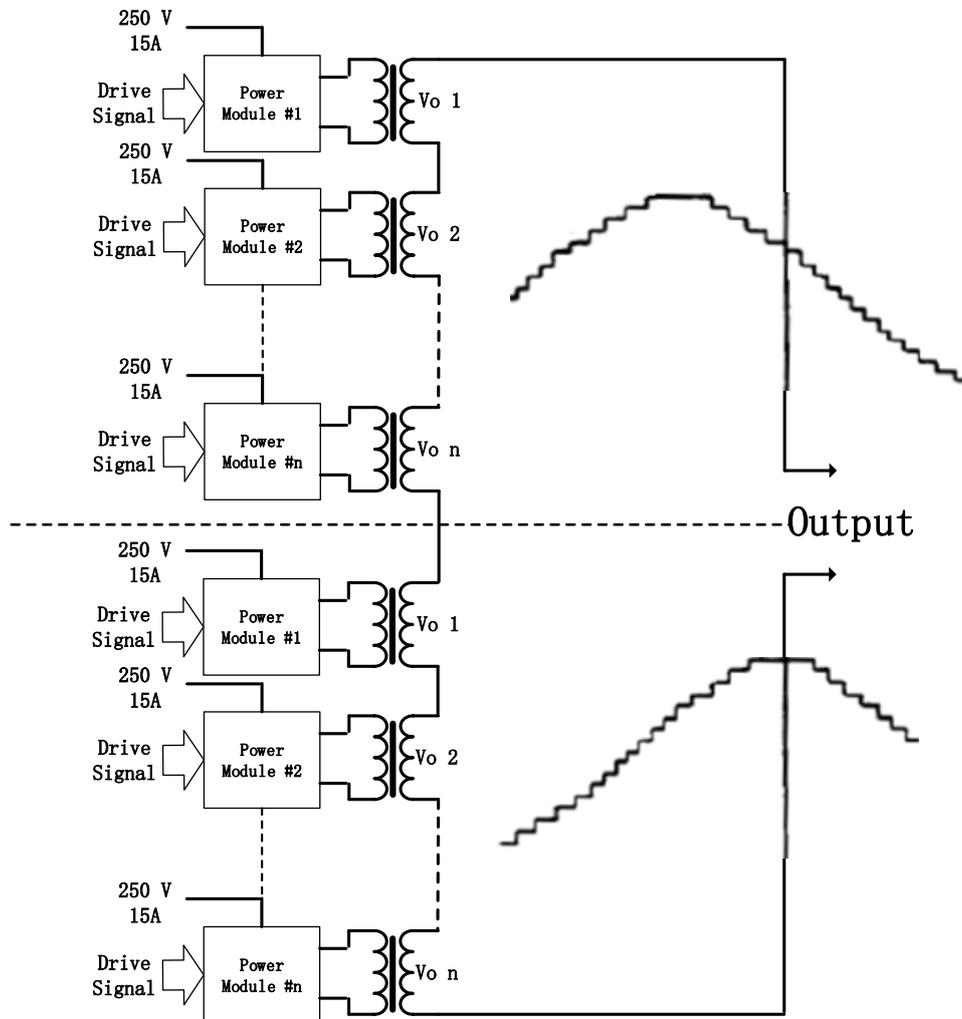


Fig. 1. 3 Original modular multi-cell converter concept

This concept was later applied in motor drives [6], namely, cascaded H-bridges, shown in Fig. 1. 4. The main drawback of the cascaded H-bridges converter is that no common DC bus is provided, so there are usually isolated transformers to provide independent DC source and it needs a sophisticated transformer with several output

windings. Separate windings supply power to each cell and the power quality at the utility side is also improved thanks to the phase shifting in the transformer [6].

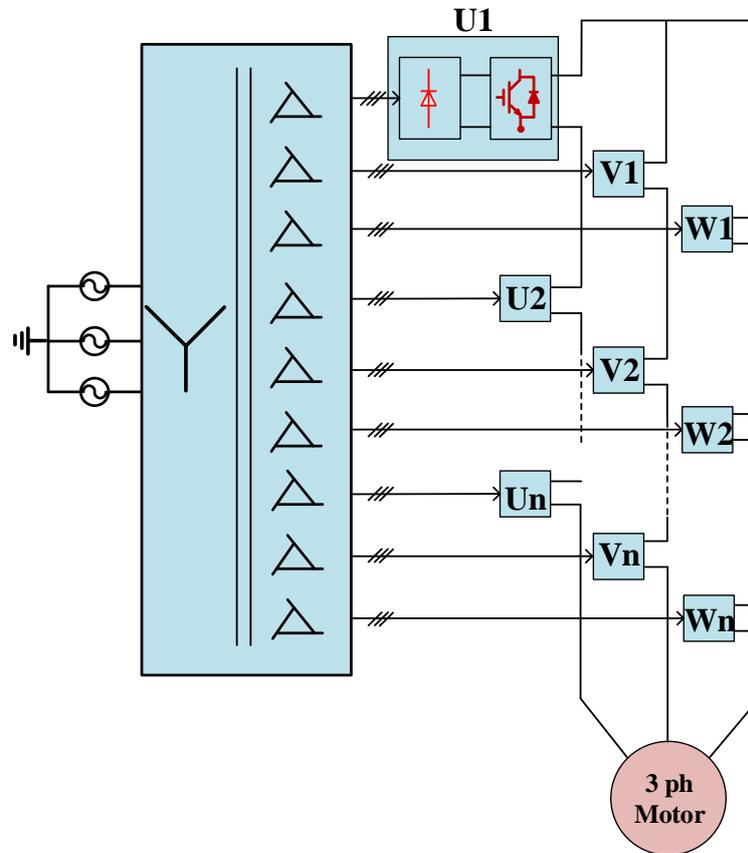


Fig. 1. 4 Cascade H-Bridge Converter for motor drive

The cascade H-Bridge converter has the advantages of modularity, scalability and increased reliability with redundancy. Contrary to the neutral-point clamped (NPC) inverter, the cascade H-Bridge converter can be implemented at dozens of voltage levels. However, without a high voltage DC bus, the cascade H-Bridge converter cannot be implemented in the application of the High Voltage DC Transmission (HVDC).

Afterwards, a modular multilevel converter (MMC) was proposed, fulfilling both active and reactive power processing without requiring a sophisticated transformer.

Professor R. Marquardt and A. Lesnicar proposed the concept of the modular multilevel converter [7]. The first topology used in the structure of the MMC was the half bridge, as shown in Fig. 1. 5. The phase-leg consists of one upper arm and one lower arm, with N submodules each. Two arm inductors are utilized to limit current ripples and fault currents.

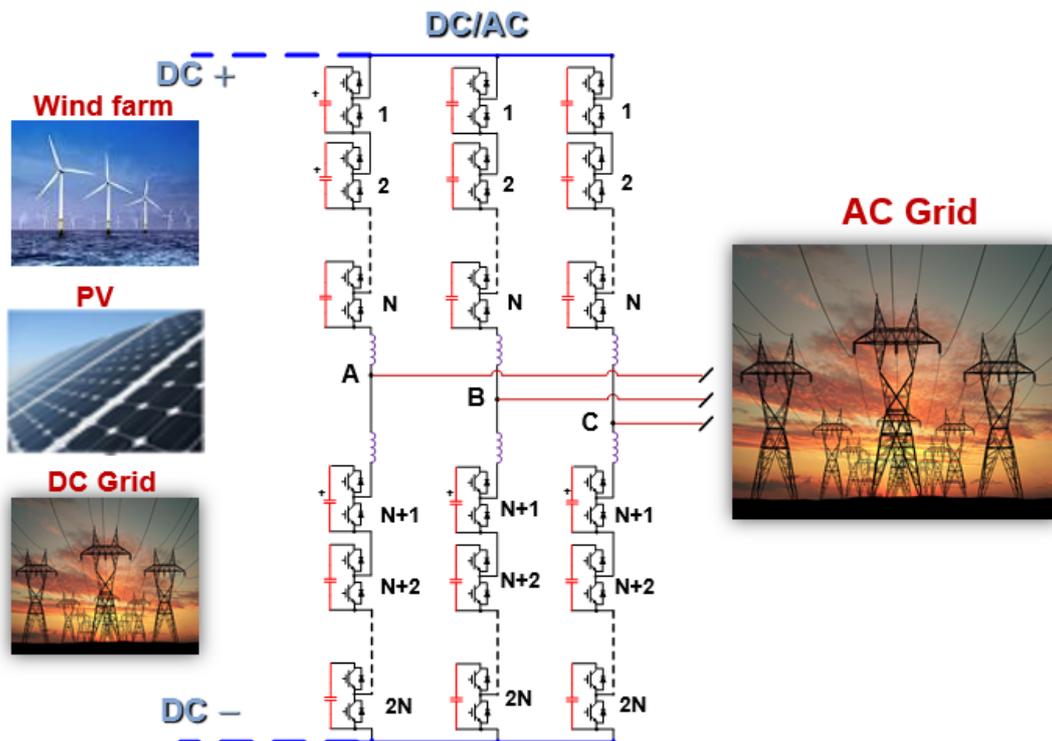


Fig. 1. 5 Half bridge modular multilevel converter

The topology of the module is not limited to the half bridge. Professor R. Marquardt also proposed a full bridge MMC later to block the fault current caused by the short circuit on the DC bus [8]. The full bridge MMC is shown in Fig 1. 6. Besides the capability of protection, the full bridge modules can also provide an additional control freedom: a larger voltage gain [9].

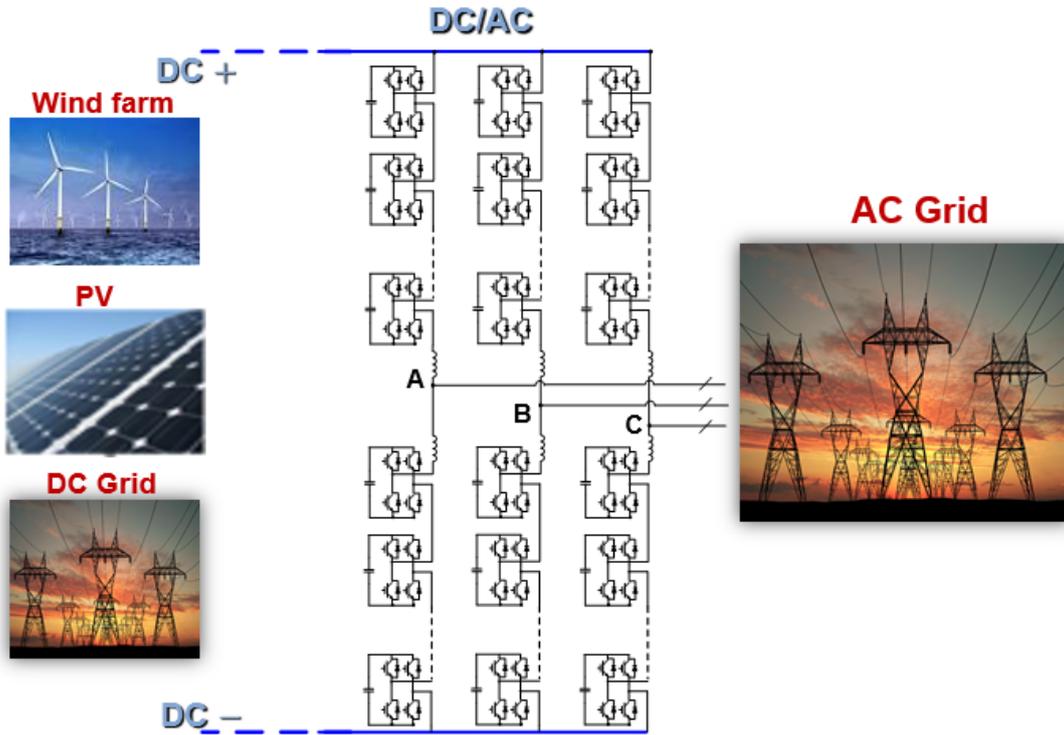


Fig 1. 6 Full bridge modular multilevel converter

1.2. Applications

Since the first MMC-HVDC system was built in California, the USA, MMC has become the dominant solution to the HVDC systems. With the increasing requirement of efficiency and renewable energy in the power systems, the number of VSC-HVDC installations keeps increasing in the world.

Table 1. 1 shows the VSC-HVDC installations in the world [10].

Table 1. 1 VSC-HVDC installations in the world

	Number of installations	Voltage rating (kV)
Europe	24	9~515
North America	5	200~500
Asia	4	18~160
Australia	2	80~150
Africa	1	350

The European Union is planning a super grid that would ultimately interconnect the various European countries and the regions around Europe's borders with HVDC power grids. Fig. 1. 7 shows the map of Europe super grid [11]. The solar energy from North Africa, as well as the off-shore wind energy in the ocean, could be transferred through HVDC transmission lines to Europe. The super HVDC power systems could reduce the cost of power transmission among countries and allow for wider use of renewable energy. The existing HVDC installations shown in Table 1. 1 would eventually be part of European Supergrid. For the connection between DC grids and AC grids, the modular multilevel converters have been proven to be the most prominent interface converter, so it can be expected that the applications of modular multilevel converters will significantly increase in the future.



Fig. 1. 7 Future: Europe Super Grid

Modular multilevel converters also provide a solution to the interface converter between two asynchronous power grids. The structure is shown in Fig. 1. 8.

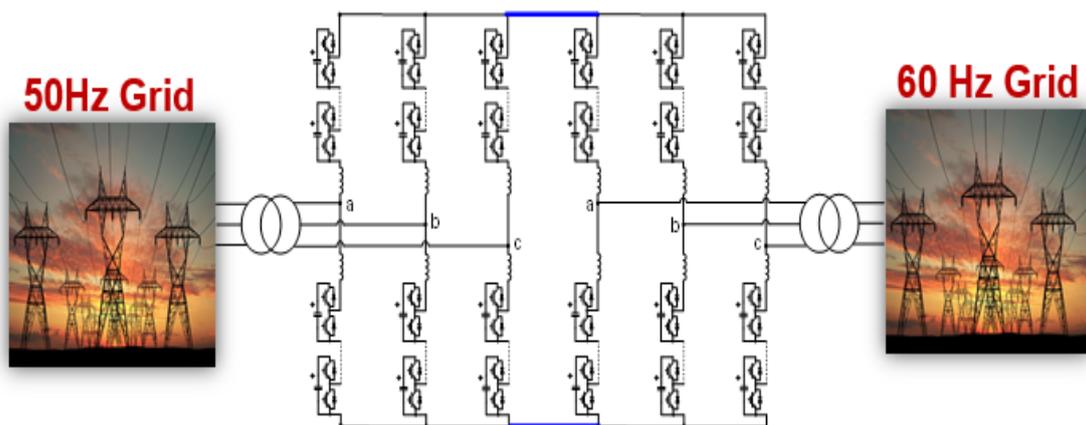


Fig. 1. 8 Applications of MMC-HVDC

1.3. Research Objectives

Since the topology of MMC was invented, the control systems have been discussed by many research groups. The control systems include the energy balance control between the upper arm and the lower arm, and the energy balance control among modules in each arm. Right now, a reliable and stable operation of the converter can be realized by the control systems proposed by Akagi's group [12] [13]. Another issue of MMC is the capability of protection against the short circuit on the DC bus. The original MMC topology was based on half bridge modules, but it lacks the ability to protect the DC short circuit. To block the short circuit current, the full bridge MMC and other alternatives were proposed [10]. However, the full bridge modules will double the conduction loss. In order to reduce the conduction loss while maintaining the capability of fault protection, a hybrid MMC [14] and a semi-full bridge topology [15] were proposed.

One research challenge in MMC is the capacitor reduction, because the capacitor bank is very significant in current commercial products. Fig. 1. 9 shows the picture of one module in the industry. The volume of the capacitor bank is more than two thirds the volume of the total module, because of large line frequency and the second-order voltage ripples. The huge capacitor bank highly increases the cost and the volume of the MMC systems.



Fig. 1. 9 A picture of one module in commercial product

Methods for reducing the capacitor voltage ripples have been widely pursued as an important research topic. Winkelkemper, Korn, and Steimer proposed a method of injecting a second-order harmonic current to minimize the second-order voltage ripple of the capacitor [16]. The benefits are limited, since there is still a significant fundamental component in the capacitor voltage ripple. The concept of injecting high-frequency voltage and circulating current was proposed by A. J. Korn, M. Winkelkemper, and P. Steimer [17] in order to facilitate the start-up of induction motors with quadratic-torque loads. However, the injected high-frequency voltage and current can be relative high and in some time it can be as high as switching frequency [18]. The high frequency components are undesired at high power grid-tied application [19]. Without considering circulating current injection, K. Ilves, S. Norrga and H. P. Nee discussed reducing or even eliminating fundamental frequency

capacitor voltage ripple at unit power factor by controlling voltage gain and utilizing full bridge modules [20]. However, the second-order capacitor voltage ripple still exists.

The research objectives of this thesis are focused on the capacitor reduction. Besides the half bridge MMC and full bridge MMC, a hybrid MMC will also be discussed. A hybrid MMC is attracting more attentions since it is a compromise solution between the loss and the capability of protection [14].

1.4. Thesis Outline

A power analysis method and a state trajectory analysis method is presented in chapter 2. Several commonly used control examples are analyzed with these two analysis tools.

Based on the previous analysis, a novel control method is proposed in chapter 3. Ideally, the proposed concept works with the full bridge MMC. With an additional voltage injection, the proposed method can be extended to the hybrid MMC.

The hardware experiments will be presented to demonstrate the aforementioned concepts in chapter 4. The hardware structure and the software structure will be addressed. The experimental waveforms verify the analysis in the previous chapters.

Chapter 2 State Space Modeling and Power Flow Analysis

To understand the nature of circulating power in this converter, the state trajectory analysis method and the power flow analysis method will be presented. With these two analysis methods, several commonly used control methods for the capacitor reduction will be evaluated.

2.1 Review Operating Principles of MMC

In order to find a method of reducing capacitors in a modular multilevel converter (MMC), an understanding of its basic operating principles is essential. The diagram of one phase of a modular multilevel converter is shown in Fig. 2. 1. Each phase leg consists of one upper arm and one lower arm. The two arms are connected in series between the DC terminals. The AC terminal is connected with the midpoint of two arms. In each arm, there are N series connected modules and one arm inductor. The modules in Fig. 2. 1 are half bridges with DC capacitors.

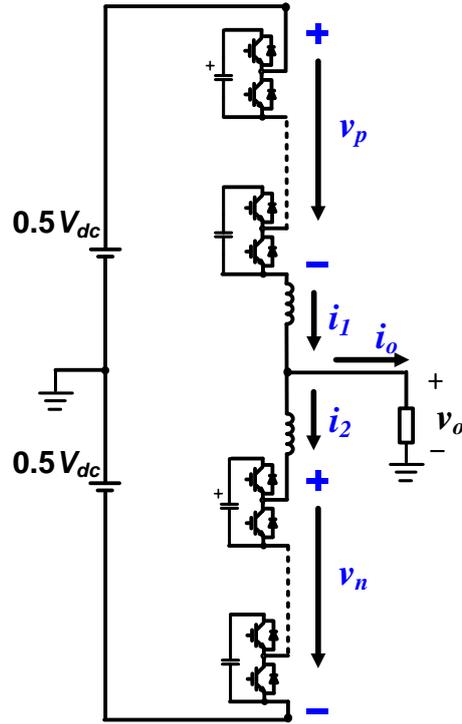


Fig. 2. 1 Single phase MMC structure

The switching ripples have little effect on the low frequency components of the capacitor voltage, thus the switching ripples are ignored in the following analysis.

If the low frequency average voltage on the inductor is ignored, the upper arm voltage v_p and the lower arm voltage v_n can be expressed as:

$$\begin{cases} v_p = \frac{1}{2}V_{dc} - v_o \\ v_n = \frac{1}{2}V_{dc} + v_o \end{cases} \quad (2.1)$$

where V_{dc} is the DC bus voltage and v_o is the line-to-neutral voltage on AC side,

$$v_o = V_o \cos \omega t, \quad (2.2)$$

where ω is the fundamental angular frequency.

The arm currents can be expressed in two components, namely, one half of the output current and the rest, circulating current [12]. In Fig. 2. 1, the upper arm current i_1 and the lower arm current i_2 can be expressed as:

$$\begin{cases} i_1 = i_{cir} + \frac{1}{2}i_o \\ i_2 = i_{cir} - \frac{1}{2}i_o \end{cases} \quad (2.3)$$

In this thesis, it is assumed that the AC current is in phase with the AC voltage for simplicity. However, the conclusion is valid for a more general case. The AC output current can be expressed as:

$$i_o = i_1 - i_2 = I_o \cos \omega t \quad (2.4)$$

i_{cir} represents circulating current, defined as:

$$i_{cir} = \frac{i_1 + i_2}{2} = I_{dc} + i_{har} \quad (2.5)$$

In the circulating current, the DC component is necessary in order to stabilize the capacitor energy. If the active power of the DC source is assumed to be equal to the active power of the AC load, the DC component can be expressed as:

$$I_{dc} = \frac{V_o I_o}{2V_{dc}} = \frac{M}{4} I_o \quad (2.6)$$

The voltage gain M is defined as:

$$M = \frac{2V_o}{V_{dc}} \quad (2.7)$$

In fact, due to the voltage ripples in the capacitor, a second-order harmonic component will appear in the circulating current if the circulating current is not controlled [21]. The harmonic components are related to a given control function [19].

There are two modulation schemes that are widely used in MMC, one is Nearest Level Modulation [22], another one is Phase Shifted Carrier PWM [12]. The Nearest Level Modulation is working at a variable switching frequency and has a higher THD when the number of modules is not enough. Meanwhile, the PSC-PWM has more flexibility and enjoys a lower THD with a higher switching frequency even though the number of modules is not large [23]. The Phase Shifted Carrier PWM modulation scheme will be used in this thesis because of the high quality of output voltage. For a MMC system with N modules per arm, the voltage command of each module will be compared with a triangular carrier wave, and the carrier wave for each module has a shifted phase angle of $2\pi/N$. Fig. 2. 2 shows the output voltage of one arm with 12 modules. The stair-case waveform ensures a small voltage steep, and the PWM modulation brings a high voltage quality.

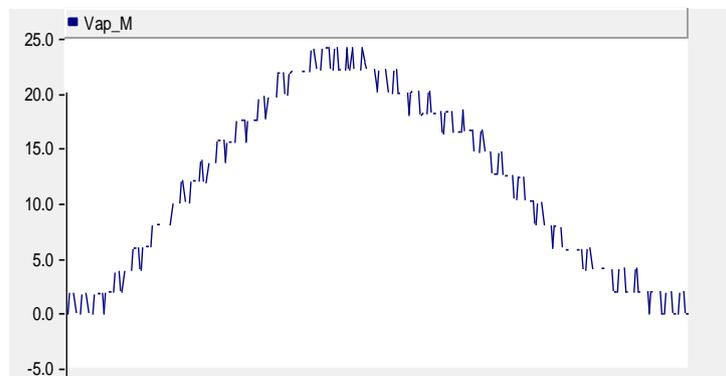


Fig. 2. 2 Arm voltage on Phase shifted carried PWM

2.2 Structure Simplification

A three phase system can be simplified to be one phase system if a symmetric system is assumed, as shown in Fig. 2. 3.

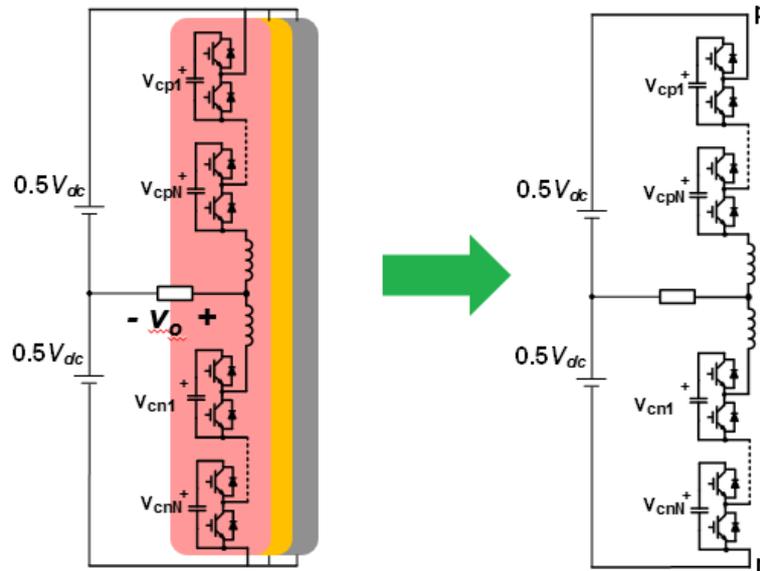


Fig. 2. 3 The symmetric 3 phase system is simplified to be one phase system

From the averages of the switching functions, an average model can be built, as shown in Fig. 2. 4. In the upper arm, d_{p1}, \dots, d_{pN} represent the duty cycles for each module, and v_{cp1}, \dots, v_{cpN} represent the capacitor voltages. In the lower arm, d_{n1}, \dots, d_{nN} represent the duty cycles for each module, and v_{cn1}, \dots, v_{cnN} represent the capacitor voltages. Each module is considered as a controlled voltage source.

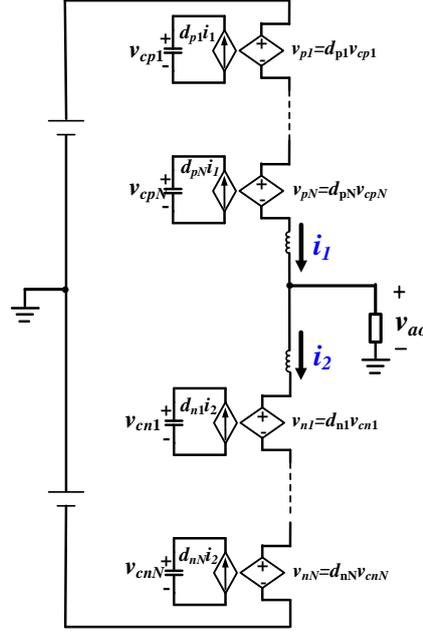


Fig. 2. 4 average model of single phase MMC

In Fig. 2. 4, the differential equations of the circuit can be expressed as:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ v_{cp1} \\ \vdots \\ v_{cpN} \\ i_2 \\ v_{cn1} \\ \vdots \\ v_{cnN} \end{bmatrix} = \begin{bmatrix} 0 & \frac{d_p}{L} & \dots & \frac{d_{pN}}{L} & 0 & 0 & \dots & 0 \\ \frac{d_p}{C} & 0 & \dots & 0 & 0 & 0 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \frac{d_{pN}}{C} & 0 & \dots & 0 & 0 & 0 & \dots & 0 \\ 0 & 0 & \dots & 0 & 0 & \frac{d_n}{L} & \dots & \frac{d_{nN}}{L} \\ 0 & 0 & \dots & 0 & \frac{d_n}{C} & 0 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & 0 & \frac{d_{nN}}{C} & 0 & \dots & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ v_{cp1} \\ \vdots \\ v_{cpN} \\ i_2 \\ v_{cn1} \\ \vdots \\ v_{cnN} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{1}{L} \\ 0 & 0 \\ \vdots & \vdots \\ 0 & 0 \\ \frac{1}{L} & \frac{1}{L} \\ 0 & 0 \\ \vdots & \vdots \\ 0 & 0 \end{bmatrix} \begin{bmatrix} 0.5V_{dc} \\ v_o \end{bmatrix} \quad (2.8)$$

If a perfect balance condition is achieved by the balance control, it can be assumed that $v_{cp1} = \dots = v_{cpN} = v_{c1}$, $v_{cn1} = \dots = v_{cnN} = v_{c2}$, $d_{p1} = \dots = d_{pN} = d_1$ and $d_{n1} = \dots = d_{nN} = d_2$. The N modules system can be represented by one module system. The differential equations (2.8) can be simplified to be:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ v_{c1} \\ i_2 \\ v_{c2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d_1}{L} & 0 & 0 \\ \frac{d_1}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{d_2}{L} \\ 0 & 0 & \frac{d_2}{C} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ v_{c1} \\ i_2 \\ v_{c2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{1}{L} \\ 0 & 0 \\ \frac{1}{L} & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} 0.5V_{dc} \\ v_o \end{bmatrix} \quad (2.9)$$

The simplified structure is shown in Fig. 2. 5.

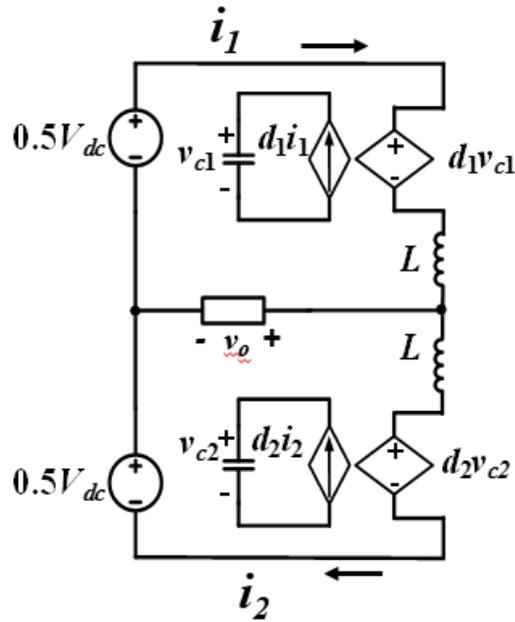


Fig. 2. 5 Simplified average model of one module per arm

The KVL equations for the upper loop and lower loop in Fig. 2. 5 can be expressed as:

$$\frac{v_{dc}}{2} - d_1 v_{c1} - i_o R_o = L \frac{d}{dt} i_1, \quad (2.10)$$

$$\frac{v_{dc}}{2} - d_2 v_{c2} + i_o R_o = L \frac{d}{dt} i_2. \quad (2.11)$$

Organize the above equations in such a way, (2.10)- (2.11)=(2.12) and

$$\frac{(2.10)+(2.11)}{2} = (2.13):$$

$$-d_1 v_{c1} + d_2 v_{c2} - 2i_o R_o = L \frac{d}{dt} (i_1 - i_2), \quad (2.12)$$

$$V_{dc} - \frac{d_1}{2} v_{c1} - \frac{d_2}{2} v_{c2} = L \frac{d}{dt} \frac{i_1 + i_2}{2}. \quad (2.13)$$

Usually the voltage ripples are designed to be much smaller than the DC bias voltage (V_c), so the capacitor voltages can be approximated to be:

$$v_{c1} = v_{c2} = V_c \quad (2.14)$$

Substitute equations (2.4), (2.5) and (2.14) into equations (2.13) and (2.14):

$$\begin{cases} \frac{d_2 - d_1}{2} = \frac{I_o R_o \cos \omega t}{V_c} + \frac{L}{V_c} \frac{d}{dt} i_o \\ \frac{d_1 + d_2}{2} = \frac{V_{dc}}{2V_c} - \frac{L}{V_c} \frac{d}{dt} i_{cir} \end{cases} \quad (2.15)$$

From equations (2.15), it can be observed that the differential component of duty cycles (d_1 and d_2) is a fundamental frequency component, controlling the output current; the common component of duty cycles is related to the DC offset of capacitor voltage (V_c) and the derivatives of circulating current (AC component). Usually, the reference of V_c is set to be V_{dc} .

A simplified simulation model was built to analyze this converter, as shown in

Fig. 2. 6.

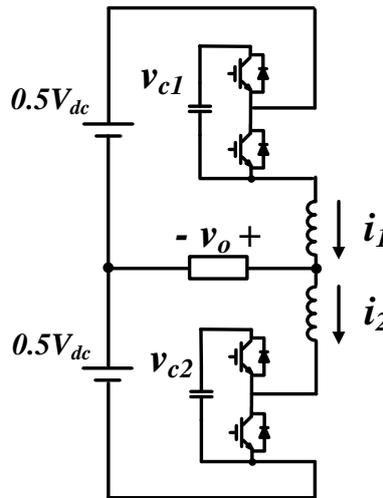


Fig. 2. 6 Single phase MMC simulation model

The parameter of the simulation model is shown in Table 2. 1.

Table 2. 1 Simulation parameters

DC source voltage	600 V
Line frequency	60 Hz
Arm inductance	2 mH
Modulation Index	0.8
SM capacitance	750 μ F
Switching frequency	5 kHz
Load Resistor	3.2 Ohms

Based on equations (2.15), a simple duty cycle control law can be assumed as:

$$\begin{cases} d_1 = 0.5 \left(1 - \frac{V_o}{0.5V_{dc}} \cos\omega t \right) \\ d_2 = 0.5 \left(1 + \frac{V_o}{0.5V_{dc}} \cos\omega t \right) \end{cases} \quad (2.16)$$

The duty cycle control law of equation (2.16) is taken as the first control example in this these. Phase Shifted Carrier PWM is used as the modulation scheme, shown in Fig. 2. 7. V_{m1} is the modulation wave for the upper module and S1 is the switching signal for the upper module. V_{m2} is the modulation wave for the lower module and S2 is the switching signal for the lower module.

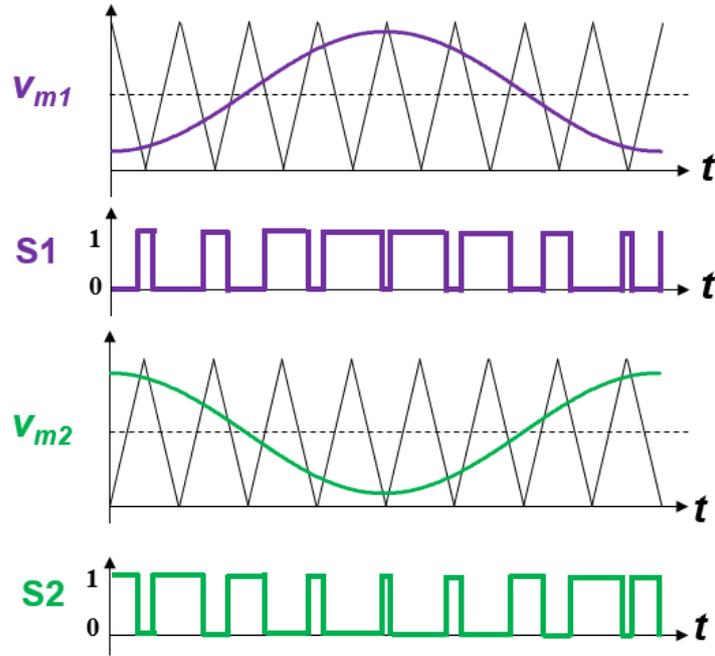


Fig. 2. 7 The modulation scheme in the simulation

With the duty cycle control law of equation (2.17) and the modulation scheme shown in Fig. 2. 7, the simulation waveforms of example 1 are shown in Fig. 2. 8.

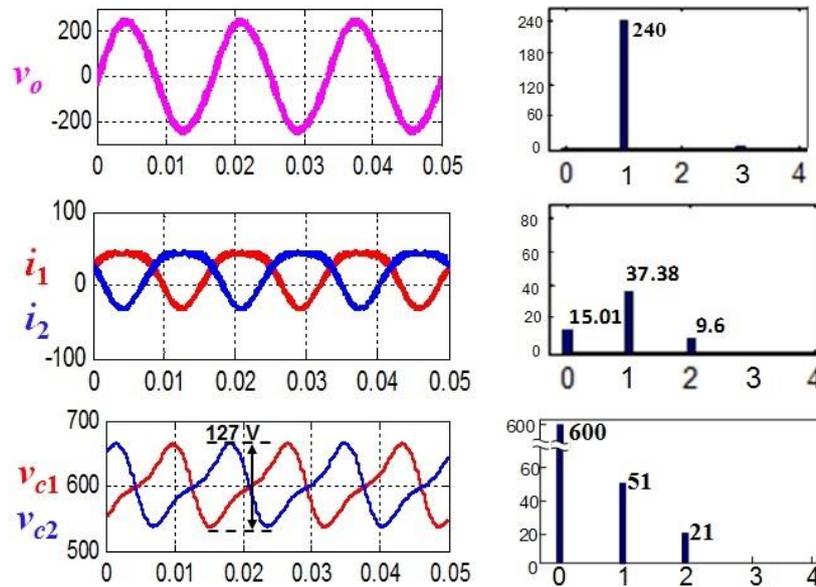


Fig. 2. 8 Simulation waveforms in example 1

As seen in Fig. 2. 8, the ripple of the capacitor voltage is significant, because of a large fundamental voltage and a considerable second-order voltage. In the circulating

current, there is a second-order component. The second-order circulating current in this example is determined by the circuit parameters [24],

$$i_{har} = -I_h \cos 2\omega t = \frac{-3I_o M(3-M^2)}{4(2M^2 - 48CL\omega^2 + 3)} \cos 2\omega t \quad (2.17)$$

2.3 Introduction of State Space Analysis [25]

Chen Li from CPES of Virginia Tech proposed a method of state trajectory analysis for MMC, in order to gain a better understanding of the nature of circulating energy and the means to reduce it [25]. The state trajectory analysis offers a graphical visualization of the effectiveness of various methods. This thesis also discusses this method of state trajectory analysis in the conjunction with the power flow analysis.

In the structure shown in Fig. 2. 5, there are four state variables i_1 , i_2 , v_{c1} , v_{c2} . Because the load current is predetermined, $i_o = i_1 - i_2$, i_1 and i_2 are not independent. Therefore, there are three independent variables i_1 or i_2 , v_{c1} , v_{c2} in the system. If i_1 , v_{c1} , v_{c2} are considered as three independent variables, the differential equation (2.9) can be simplified to be a third-order differential equation:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d_1}{L} & 0 \\ \frac{d_1}{C} & 0 & 0 \\ \frac{d_2}{C} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} \\ 0 & 0 \\ 0 & -\frac{d_2}{RC} \end{bmatrix} \begin{bmatrix} 0.5V_{dc} \\ v_o \end{bmatrix} \quad (2.18)$$

With these three variables, a 3D state space can be used to represent the system, as shown in Fig. 2. 9. The state trajectories are related to the time domain waveforms of Fig. 2. 8, under the simple duty cycle control law.

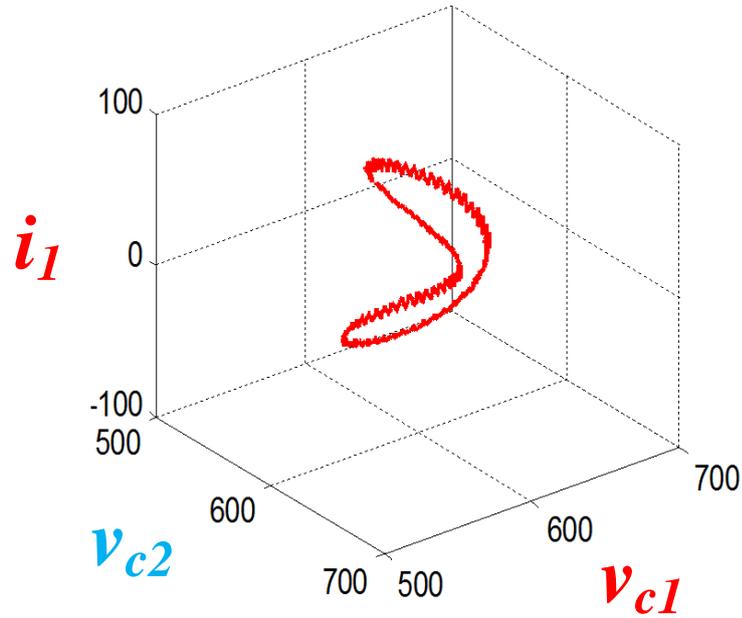


Fig. 2. 9 3D state space diagram for MMC

The projections of the 3D state space diagram are 2D state planes. The 3D state space in Fig. 2. 9 can be represented by a set of three 2D state planes to provide visual support, as shown in Fig. 2. 10.

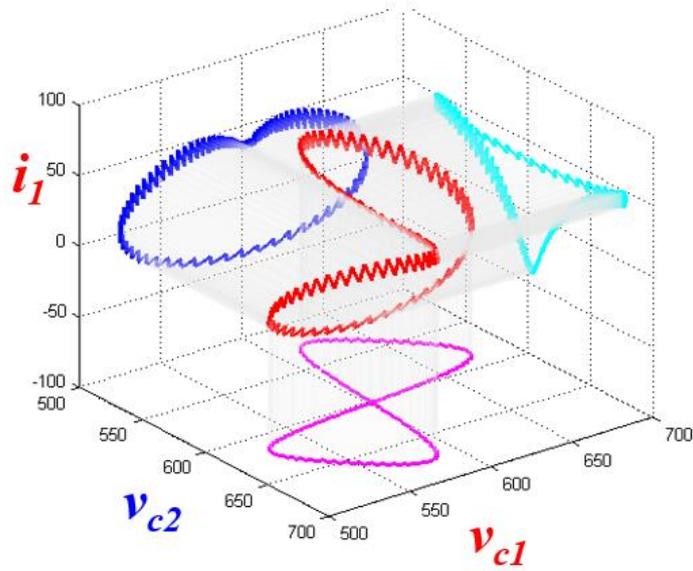
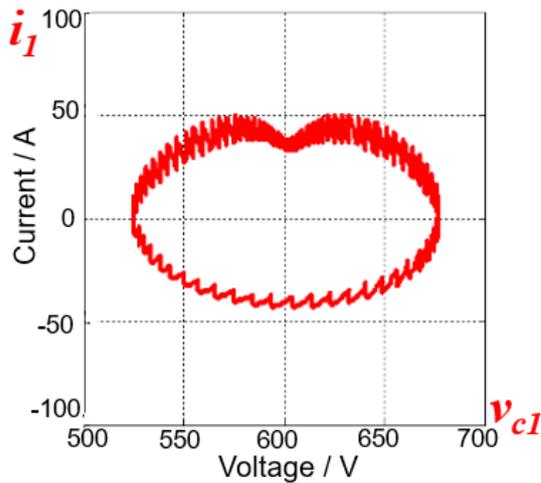
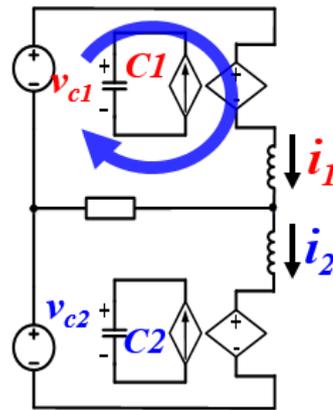


Fig. 2. 10 Projections of 3D state space diagram

The Fig. 2. 11 (a) shows the state plane of i_1 and v_{c1} . It demonstrates the resonant behavior between the module capacitor and the arm inductor. The ripple of v_{c1} is highly related to the current, i_1 , flowing through the capacitor. This phenomena is illustrated in the Fig. 2. 11 (b), showing the strong coupling relationship between i_1 and v_{c1} .



(a) The state plane of i_1 and v_{c1} ,



(b) The relationship between i_1 and v_{c1}

Fig. 2. 11 The illustration of state plane of i_1 and v_{c1}

Fig. 2. 12 shows the relationship between the state trajectory and the time domain waveforms. There are second-order harmonic components in the arm current and capacitor voltage. It should be noted that the state trajectory is biased along its x-axis with the bias voltage V_c .

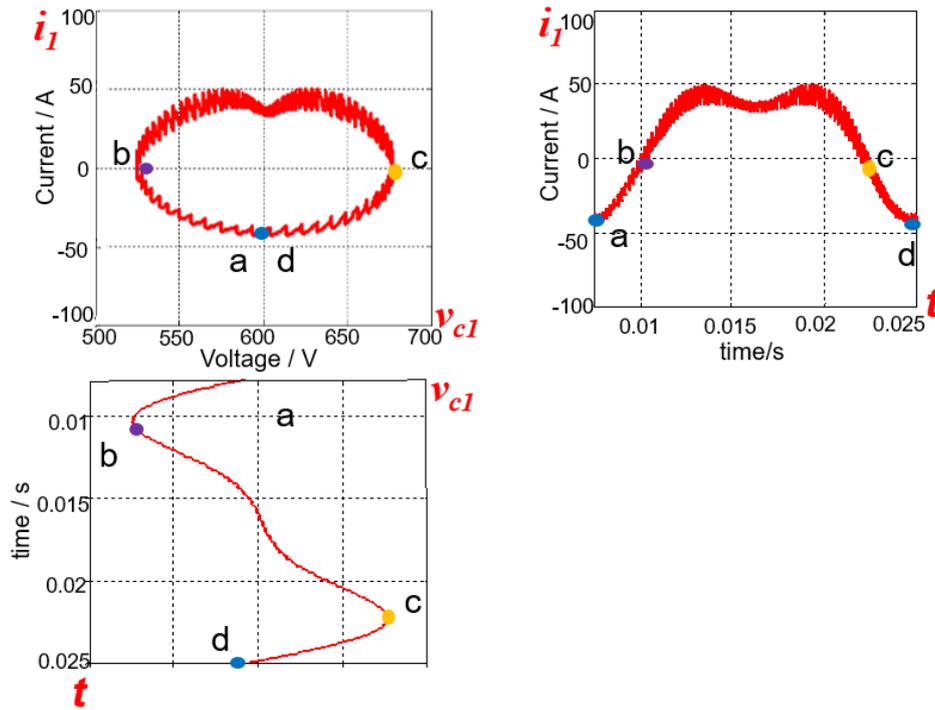


Fig. 2. 12 The state plane of i_1 and v_{c1} related to waveforms

The size of the state trajectory in one cycle of operation is proportional to its energy; i.e., a larger loop leads to a higher energy level. Fig. 2. 13 shows the state trajectory of i_1 and v_{c1} with different power ratings. It illustrates that the loop size increases with a larger load power.

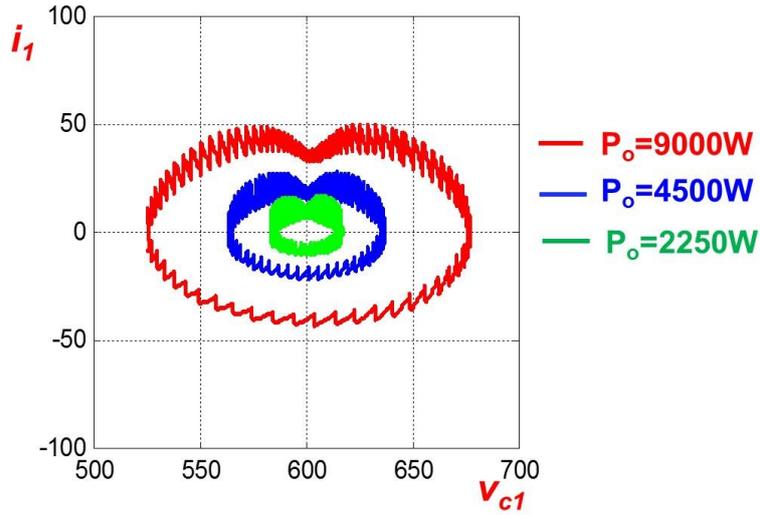
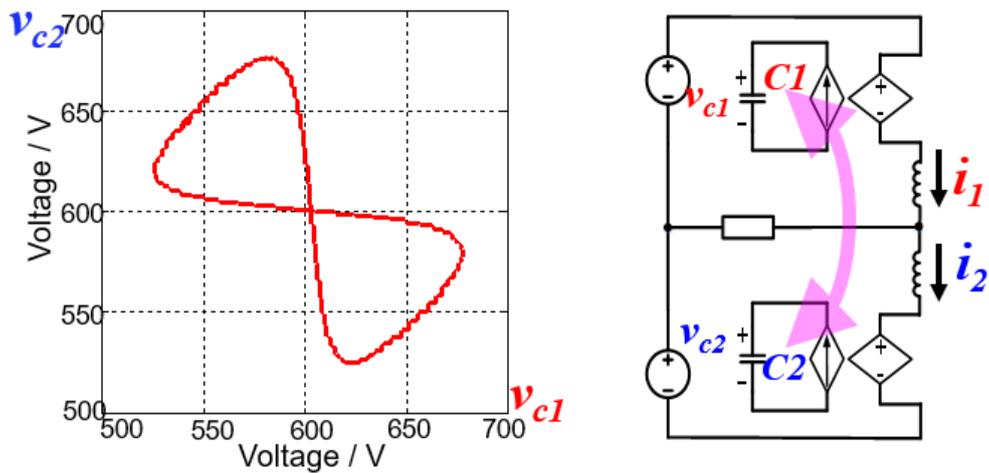


Fig. 2. 13 The state plane of i_1 and v_{c1} with different power rating

The Fig. 2. 14 (a) demonstrates the energy circulating behaviors of the two capacitors, showing the state plane of v_{c1} to v_{c2} . There is some energy exchanging between the upper capacitor and the lower capacitor during the time interval when one capacitor voltage is increasing while the other one is decreasing. This phenomena is illustrated in the Fig. 2. 14 (b), showing the relationship of exchanging energy between v_{c1} and v_{c2} .

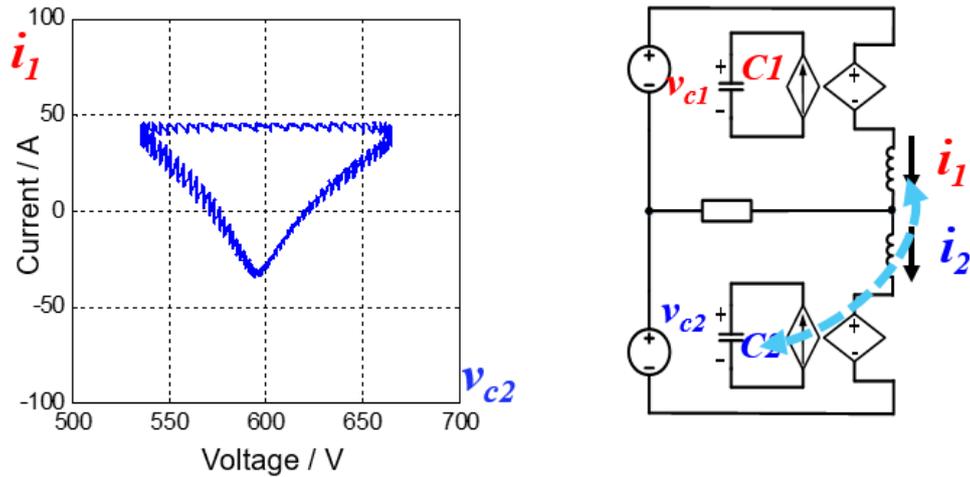


(a) The state plane of v_{c1} and v_{c2} ,

(b) The relationship between v_{c1} and v_{c2}

Fig. 2. 14 The illustration of state plane of v_{c1} and v_{c2}

The Fig. 2. 15 (a) shows the state plane of i_l and v_{c2} . It shows very weak resonant behavior between the upper arm inductor (i_l) and the lower module capacitor (v_{c2}), because of the linear behavior of the state trajectory. The diagram of this phenomena is illustrated in the Fig. 2. 15 (b).



(a) The state plane of i_l and v_{c2} , (b) The relationship between i_l and v_{c2}

Fig. 2. 15 The illustration of state plane of i_l and v_{c2}

Based on the aforementioned analysis, the informative state planes are the state plane of i_l and v_{c1} and the state plane of v_{c1} and v_{c2} . The following analysis will be focused on this two state planes.

2.4 Power Flow Analysis

A concept of power flow analysis in the conjunction with state plane analysis will be presented in this section.

The Fig. 2. 16 shows the state plane of v_{c1} to v_{c2} and the time domain waveforms.

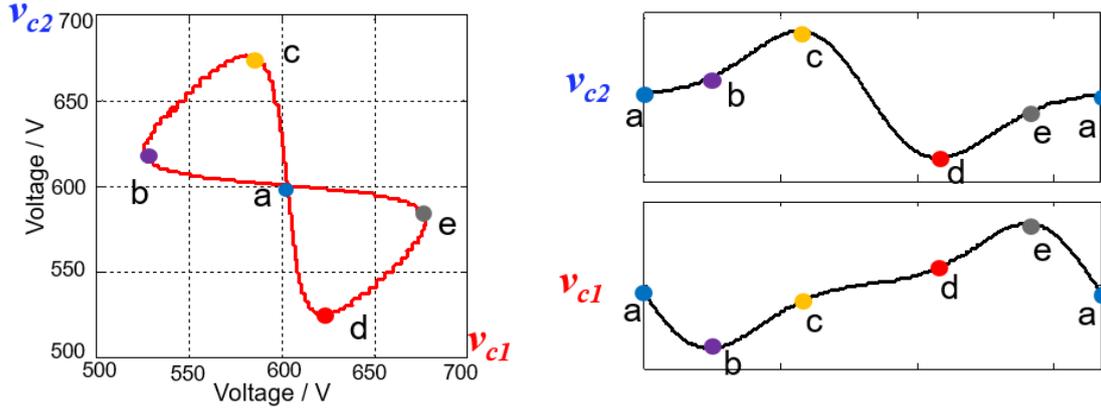


Fig. 2. 16 The state plane of v_{c1} to v_{c2} and waveforms

Based on the simulation results shown in Fig. 2. 8, the capacitor voltage can be expressed as:

$$\begin{cases} v_{c2} = V_{dc} + V_1 \sin \omega t + V_3 \sin 3\omega t - V_2 \sin 2\omega t \\ v_{c1} = V_{dc} - V_1 \sin \omega t - V_3 \sin 3\omega t - V_2 \sin 2\omega t \end{cases} \quad (2.19)$$

In order to explain the pattern of energy circulating in this converter, the α -axis and the β -axis are defined, as shown in Fig. 2. 17. The α -axis is related to the odd-order components of v_{c1} and v_{c2} , in equation (2.19), and the β -axis is related to the even-order component of v_{c1} and v_{c2} , in equation (2.19). The state plane and time domain waveforms will be discussed in three intervals to illustrate the meanings of the defined axes.

The first interval is shown in Fig. 2. 17. During this interval, the projection on the α -axis increases, related to the odd-order components in v_{c1} and v_{c2} , because they have opposite signs. The energy of C1 decreases while the energy of C2 increases, meaning that the energy is exchanged from C1 to C2. On the other hand, the projection on the β -axis decreases, related to the even-order component in v_{c1} and v_{c2} , because they

have the same sign. The total energy of C1 and C2 decreases, meaning that C1 and C2 release energy to the load.

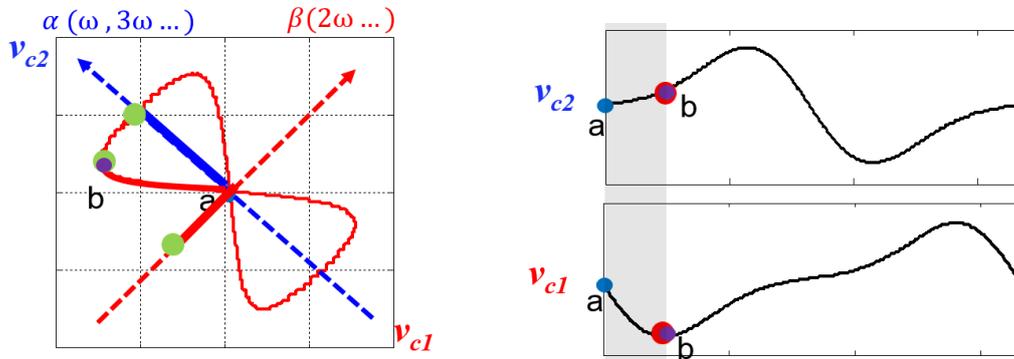


Fig. 2. 17 The interval 1 of the state plane of v_{c1} to v_{c2}

The diagram of power flow in the first interval is shown in Fig. 2. 18.

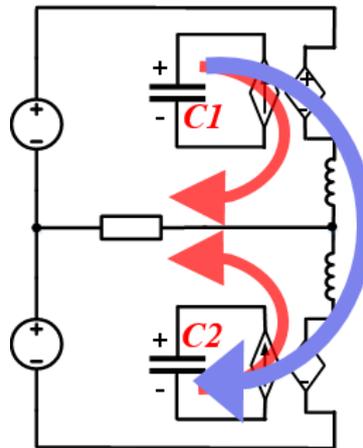


Fig. 2. 18 The diagram of power flow in the interval 1

The second interval is shown in Fig. 2. 19. During this interval, the projection on the α -axis does not change much. There is no significant energy exchange between C1 and C2. On the other hand, the projection on the β -axis increases, indicating that C1 and C2 receives energy from the sources.

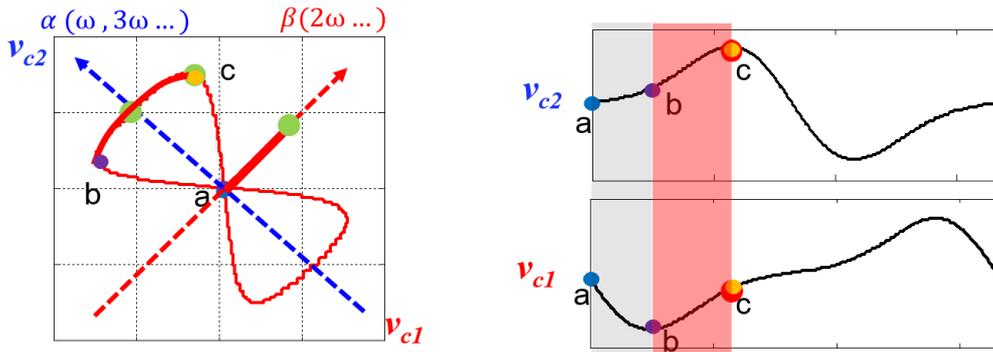


Fig. 2. 19 The interval 2 of the state plan of v_{c1} to v_{c2}

The diagram of power flow in the second interval is shown in Fig. 2. 20.

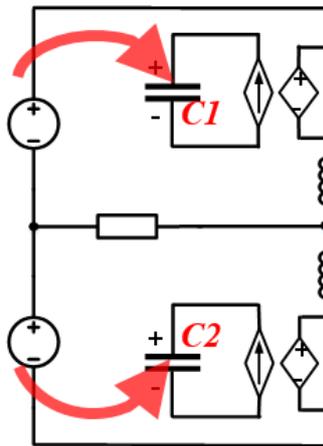


Fig. 2. 20 The diagram of power flow in the interval 2

The third interval is shown in Fig. 2. 21. During this interval, the projection on the α -axis decreases, representing the energy is exchanged from C2 to C1. The projection on the β -axis decreases, denoting that C1 and C2 release energy to the load.

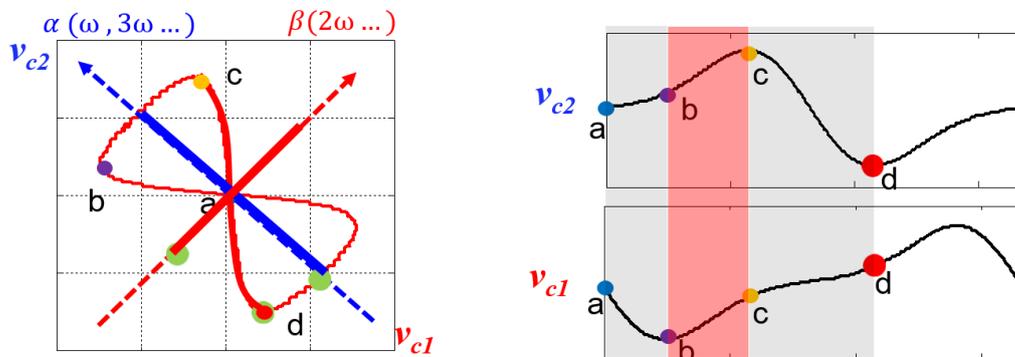


Fig. 2. 21 The interval 3 of the state plan of v_{c1} to v_{c2}

The diagram of power flow in the third interval is shown in Fig. 2. 22.

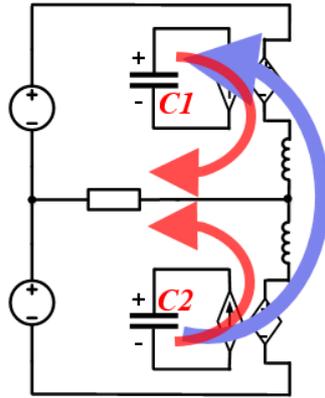


Fig. 2. 22 The diagram of power flow in the interval 3

The remaining intervals can be analyzed in the same method. Based on aforementioned analysis, the physical meanings of α -axis and β -axis can be concluded: the α -axis is related to the odd-order components of the capacitor voltage, representing the power that is being swapped between the upper module and the lower module; the β -axis is related to the even-order components of the capacitor voltage, representing the power that is being released to the load or received from the sources.

The above graphical illustration vividly explains the nature of the circulating energy that has been generated due to the nature of control. This method of analysis will be applied to evaluate control strategies in the following sections.

2.5 Capacitor Voltage and Module Power

The math relationship between the capacitor voltage and the module power will be presented in this section.

The upper module power is defined as:

$$p_p = i_l v_p \quad (2.20)$$

The energy of the capacitor in the upper module can be expressed as:

$$\frac{1}{2}Cv_{c1}^2 - \frac{1}{2}CV_c^2 = \int_0^t p_p dt \quad (2.21)$$

where V_c is the DC offset of the capacitor voltage, taken as the initial voltage; C represents the capacitance of the module.

Equation (2.21) can be organized to be:

$$\frac{1}{2}C(v_{c1} - V_c)(v_{c1} + V_c) = \int_0^t p_p dt \quad (2.22)$$

In equation (2.22), $(v_{c1} + V_c)$ is mainly DC voltage and $(v_{c1} - V_c)$ is mainly the voltage ripple. If it can be assumed that the DC bias voltage V_c is much larger than the voltage ripple, then $(v_{c1} + V_c)$ can be assumed to be $2V_c$. As a result, equation (2.22) can be organized to be:

$$CV_c(v_{c1} - V_c) = \int_0^t p_p dt \quad (2.23)$$

Equation (2.23) can be organized to be:

$$v_{c1} = V_c + \frac{1}{CV_c} \int_0^t p_p dt \quad (2.24)$$

If the lower module has the same DC offset voltage as the upper module, the capacitor voltage in the lower module can also be calculated, as a result:

$$\begin{cases} v_{c1} = V_c + \frac{1}{CV_c} \int_0^t p_p dt \\ v_{c2} = V_c + \frac{1}{CV_c} \int_0^t p_n dt \end{cases} \quad (2.25)$$

where $p_p = i_1 v_p$ and $p_n = i_2 v_n$ denote the upper module power and the lower module power.

At a particular module design, the capacitance C and the DC bias voltage V_c are predetermined, so the capacitor voltage ripple is mainly decided by the module power.

In the example 1, with current equations (2.5), (2.17) and the module voltage equation (2.1), the upper module power (p_p) and the lower module (p_n) can be expressed as:

$$\begin{cases} p_p = \left(\frac{1}{M}I_oV_o - \frac{M}{4}I_oV_o + \frac{1}{2}I_hV_o\right)\cos\omega t - \left(\frac{1}{4}I_oV_o + I_h\frac{V_o}{M}\right)\cos 2\omega t + \frac{1}{2}I_hV_o\cos 3\omega t \\ p_n = -\left(\frac{1}{M}I_oV_o - \frac{M}{4}I_oV_o + \frac{1}{2}I_hV_o\right)\cos\omega t + \left(\frac{1}{4}I_oV_o + I_h\frac{V_o}{M}\right)\cos 2\omega t - \frac{1}{2}I_hV_o\cos 3\omega t \end{cases} \quad (2.26)$$

According to (2.25) and (2.26), the odd-order AC components of p_p and p_n are related to the odd-order AC components of v_{c1} and v_{c2} respectively. Likewise, the even-order AC components of p_p and p_n related to the even-order AC components of v_{c1} and v_{c2} respectively.

2.6 Evaluation of Various Control Strategies

In this section, the state trajectory analysis and the power analysis are employed to evaluate the effectiveness of different control strategies with the intent of minimizing circulating energy and the capacitor.

Example 1: A Simple Duty Cycle Control Law

The duty cycle control law in this example is shown in equation (2.16). The simulation results are shown in Fig. 2. 8.

Table 2. 2 lists all components of the module power (2.26). In each row, the power components are introduced by the corresponding current component in that

row. While the DC components of the power is null as expected, $p_p(\omega t)$, $p_p(2\omega t)$ and $p_p(3\omega t)$ exist. The odd-order components are related to the α -axis while the even-order components are related to the β -axis. In Table 2. 2, M represents the voltage gain, defined in equation (2.7).

Table 2. 2 The module power in example 1

$i_l \backslash P_p$	$p_p(\text{DC})$	$p_p(\omega t)$	$p_p(2\omega t)$	$p_p(3\omega t)$
$\frac{M}{4} I_o$		$-\frac{M}{4} I_o V_o$		
$\frac{1}{2} I_o \cos \omega t$		$\frac{1}{M} I_o V_o$	$-\frac{1}{4} I_o V_o$	
$-I_h \cos 2\omega t$		$\frac{1}{2} I_h V_o$	$-\frac{1}{M} I_h V_o$	$\frac{1}{2} I_h V_o$

The state trajectory of i_l to v_{cl} in this case is shown in Fig. 2. 23. The areas that embody the state trajectory of i_l and v_{cl} are represented by different colors, denoting different components of power. As shown in Table 2. 2, the sum of the DC power terms is zero, which means the DC power comes from the source to the module and is immediately transferred to the load. The $p_p(\omega t)$, $p_p(2\omega t)$ and $p_p(3\omega t)$ are various components of power which are stored in the module or transferred out of the module. The fundamental power $p_p(\omega t)$ and the third-order power $p_p(3\omega t)$ are represented by the blue area. The second-order power has two components: one component is related to the source, represented by the orange area; one component is related to the load, represented by the green area.

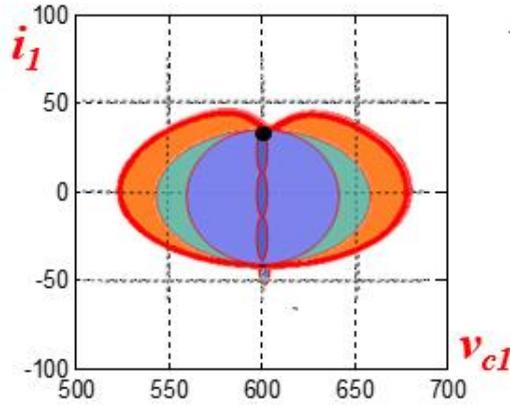


Fig. 2. 23 State trajectory of i_1 and v_{c1} in example 1

The phenomena of power circulating is clearly explained in the state trajectory of v_{c1} and v_{c2} , as shown in Fig. 2. 24. The odd-order power $p_p(\omega t)$ and $p_p(3\omega t)$ (also related to capacitor voltage) introduce the projection on the α -axis and the even order power $p_p(2\omega t)$ (capacitor voltage) introduces the projection on the β -axis.

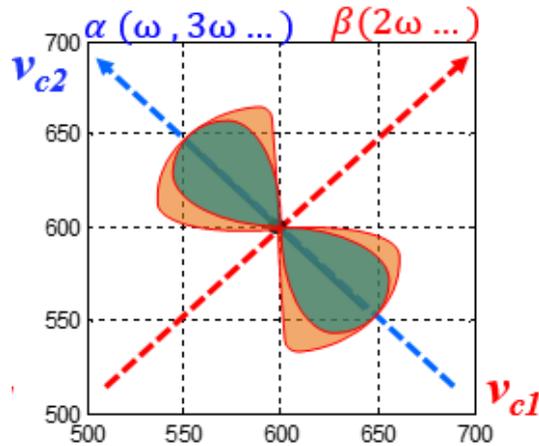


Fig. 2. 24 State trajectory of v_{c1} and v_{c2} in example 1

The above description of the circuit is further illustrated by Fig. 2. 25. Between the upper module and the lower module, there is power being swapped at the fundamental frequency and the third-order harmonic frequency. On the other hand, the two modules exchange power with the load and the source at the second-order harmonic frequency.

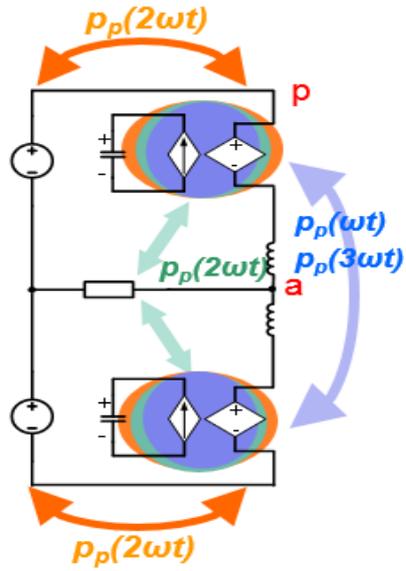


Fig. 2. 25 Power flow diagram of example 1

Example 2: Harmonic Current Suppression

In example 1, there is a second-order harmonic circulating current. In order to control the circulating current, S. Geng, Y. Gan, Y. Li, L. Hang, G. Li proposed the proportional-resonant (PR) compensator (a band pass filter with proportional gain) in the circulating current control loop [26]. The control system is shown in Fig. 2. 26.

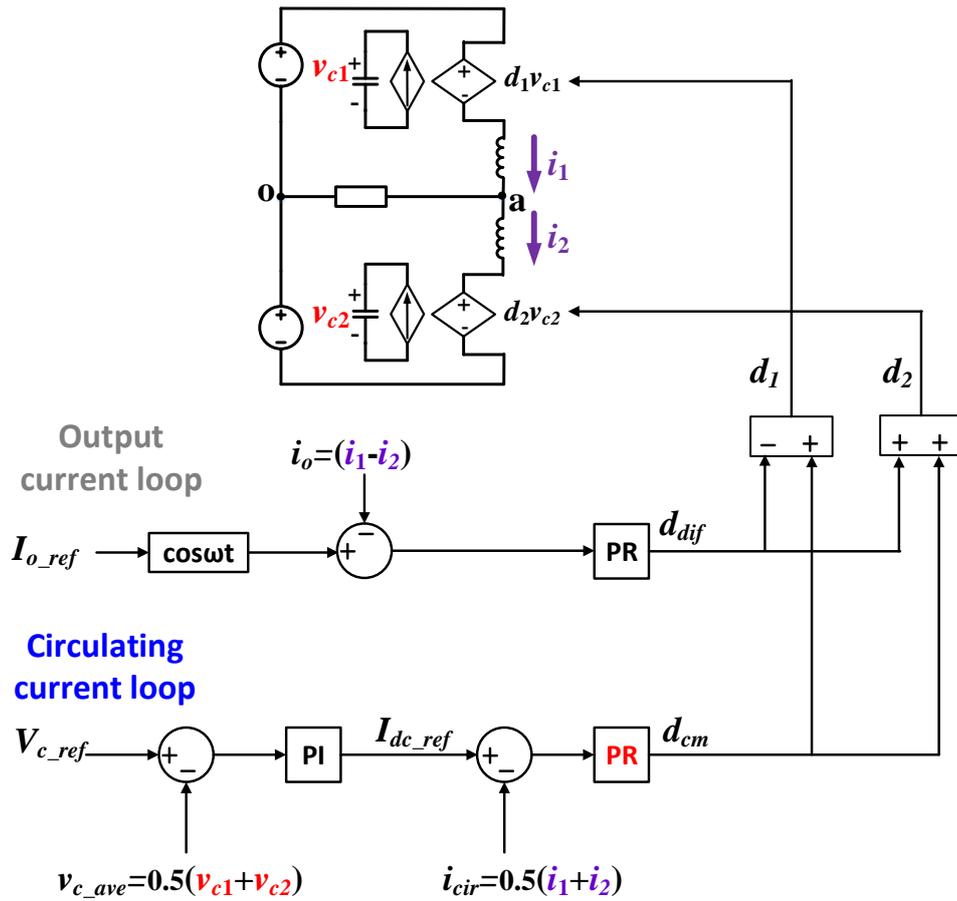


Fig. 2. 26 Current control loops in example 2

In Fig. 2. 26, the resonant frequency of the PR compensator is the defined second-order harmonic frequency, with the bode plot shown in Fig. 2. 27.

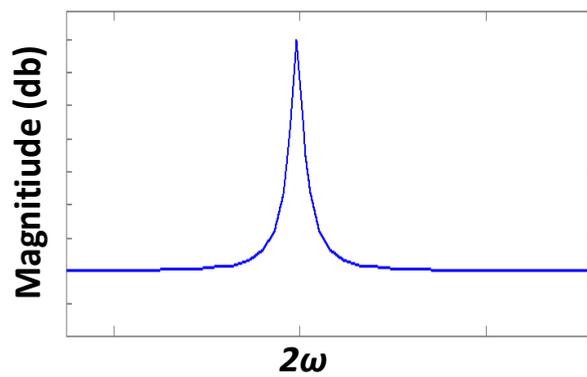


Fig. 2. 27 The magnitude figure of PR in circulating current loop

In Fig. 2. 26, the proportional-integrator (PI) compensator in the capacitor voltage loop should be designed at a low corner frequency as shown in Fig. 2. 28. This

ensures that the output of the PI compensator is mostly a DC component, which is going to be the DC component of the circulating current reference.

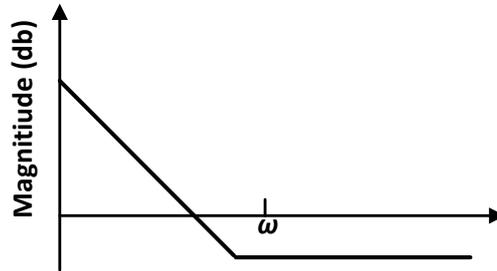


Fig. 2. 28 The magnitude figure of the bode plot of the PI compensator

With the control system shown in Fig. 2. 26, the second-order component of the circulating current is suppressed. The simulation waveforms of example 2 are shown in Fig. 2. 29. The harmonic current is eliminated. The capacitor voltage ripple is smaller than example 1, because both the fundamental voltage and the second-order voltage are smaller and there is no third-order voltage.

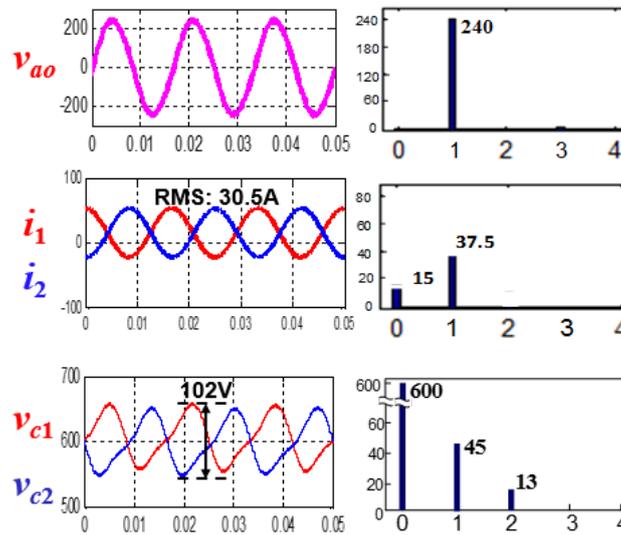


Fig. 2. 29 Simulation waveforms of example 2

Table 2. 3 lists all components of the module power in this case. Compared with example 1, with the suppression of the second-order harmonic current, both $p_p(\omega t)$ and $p_p(2\omega t)$ are smaller and there is no $p_p(3\omega t)$ existing.

Table 2. 3 The module power in example 2

$i_l \backslash P_p$	$p_p(\text{DC})$	$p_p(\omega t)$	$p_p(2\omega t)$	$p_p(3\omega t)$
$\frac{M}{4} I_o$		$-\frac{M}{4} I_o V_o$		
$\frac{1}{2} I_o \cos \omega t$		$\frac{1}{M} I_o V_o$	$-\frac{1}{4} I_o V_o$	
0		$\frac{1}{2} I_h V_o$	$-\frac{1}{M} I_h V_o$	$\frac{1}{2} I_h V_o$

The state trajectory of i_l to v_{cl} in this case is shown in Fig. 2. 30. The fundamental term $p_p(\omega t)$ is represented by the blue area, which is smaller than example 1. The second-order power is marked in the green area, denoting that this power component is transferred to the load.

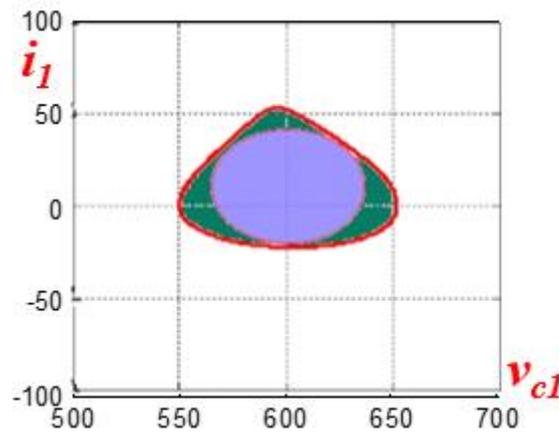


Fig. 2. 30 State trajectory of i_l and v_{cl} in example 2

The state trajectory of v_{c1} and v_{c2} in this case is shown in Fig. 2. 31. Compared with example 1, both the projection on the α -axis and the projection on the β -axis are smaller, thanks to the suppression of the second-order harmonic current.

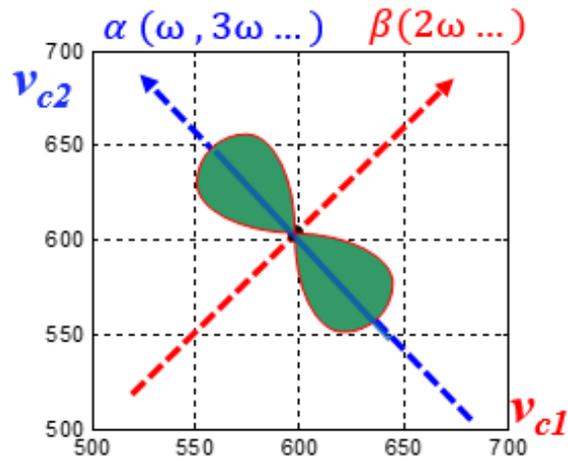


Fig. 2. 31 State trajectory of v_{c1} and v_{c2} in example 2

As discussed above, only the fundamental power are stored and exchanged between the upper and the lower module. The two modules release a second-order power to the load, as shown in Fig. 2. 32.

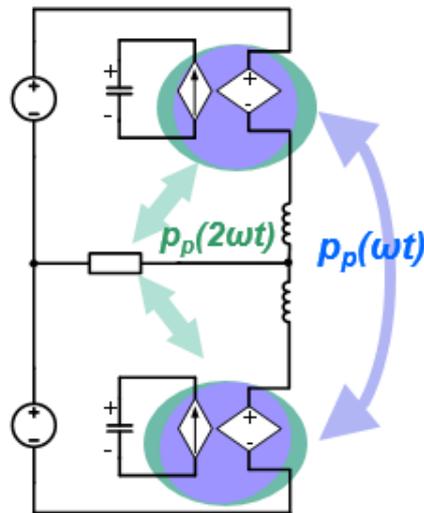


Fig. 2. 32 Power flow diagram of example 2

Example 3: Second-order Harmonic Current Injection

As discussed in example 2, the module supplies second-order harmonic power to the load. If a proper amount of second-order current is injected, the module may not

need to store the second-order harmonic related energy $p_p(2\omega t)$ [16]. With the second-order harmonic current injection from paper [16], the circulating current is:

$$i_{cir} = \frac{M}{4} I_o + \frac{M}{4} I_o \cos 2\omega t \quad (2.27)$$

In this method, the total input power can be expressed as:

$$p_{in} = \frac{1}{2} V_{dc} i_1 + \frac{1}{2} V_{dc} i_2 = \frac{1}{2} V_o I_o + \frac{1}{2} V_o I_o \cos 2\omega t \quad (2.28)$$

The load power can be expressed as:

$$p_o = \frac{1}{2} V_o I_o + \frac{1}{2} V_o I_o \cos 2\omega t \quad (2.29)$$

Since $p_{in} = p_o$, there is no second-order power required from the modules.

The control system in this case is shown in Fig. 2. 33, which is similar to example 2. The only difference is that there is a second-order component in the reference of the circulating current.

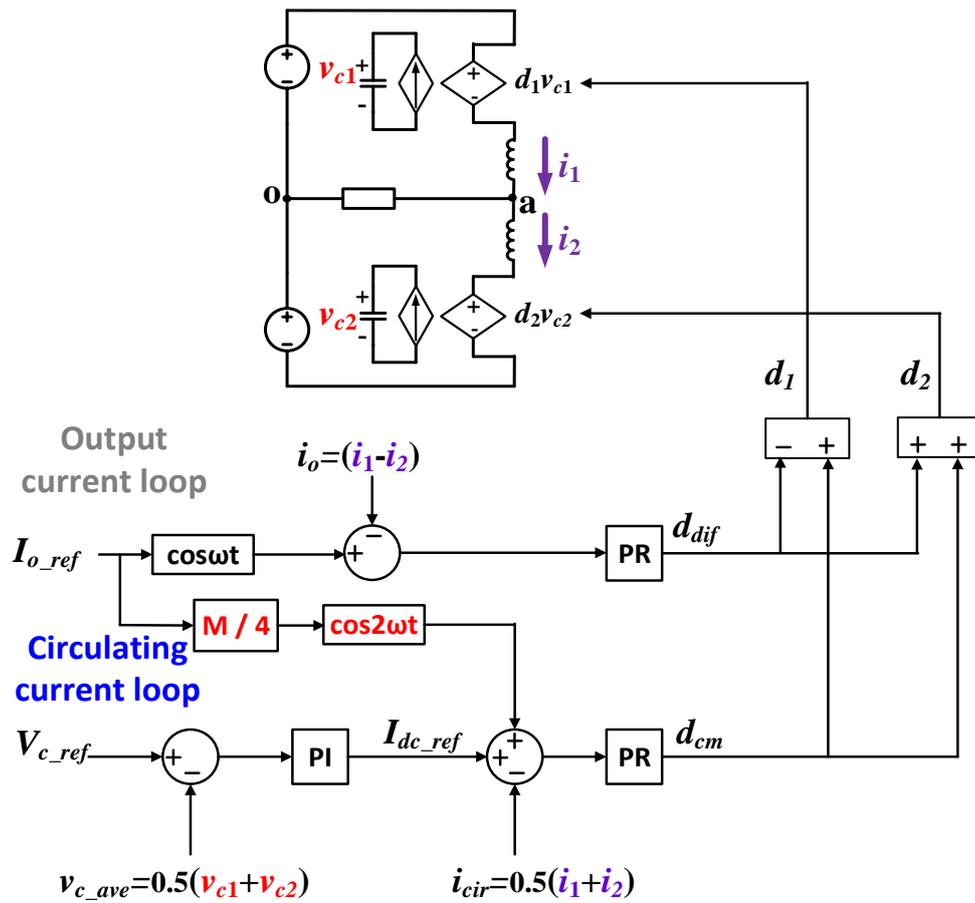


Fig. 2. 33 Current control loops in example 3

The simulation waveforms of example 3 are shown in Fig. 2. 34. A particular second-order harmonic current is injected to eliminate the second-order component of the capacitor voltage ripples.

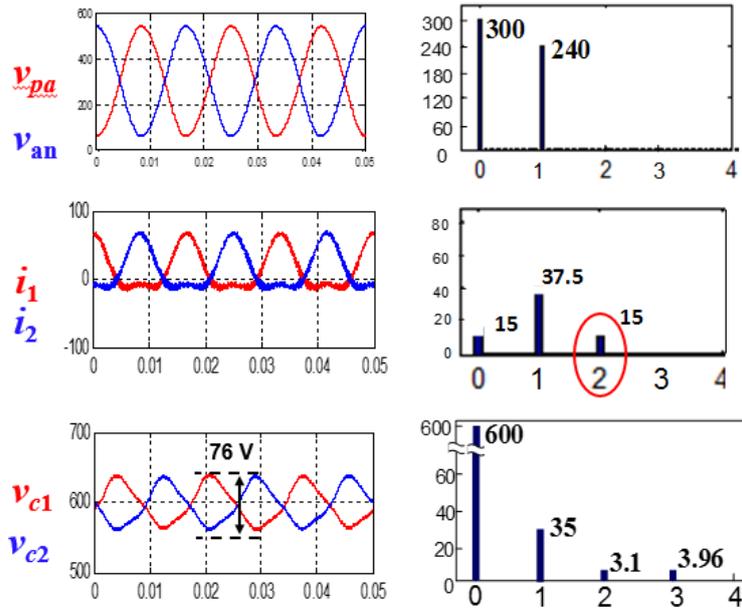


Fig. 2. 34 simulation waveforms of example 3

Table 2. 4 lists all components of the module power in this case. With this harmonic current injection, the second-order component of the module power in Table 2. 3 will cancel out each other. That means the module does not have the role of storing and transferring power to the load. This method also reduces the fundamental power at the expense of a small third-order power.

Table 2. 4 The module power in example 3

$i_1 \backslash P_p$	$P_p(DC)$	$P_p(\omega t)$	$P_p(2\omega t)$	$P_p(3\omega t)$
$\frac{M}{4} I_o$		$-\frac{M}{4} I_o V_o$		
$\frac{1}{2} I_o \cos \omega t$		$\frac{1}{M} I_o V_o$		
$\frac{M}{4} I_o \cos 2\omega t$		$-\frac{M}{8} I_o V_o$		$-\frac{M}{8} I_o V_o$

In Fig. 2. 35, the blue area is further reduced compared to Example 2. There is no green area related to the second-order power. The capacitor voltage consists of only the fundamental and the third-order harmonic voltages.

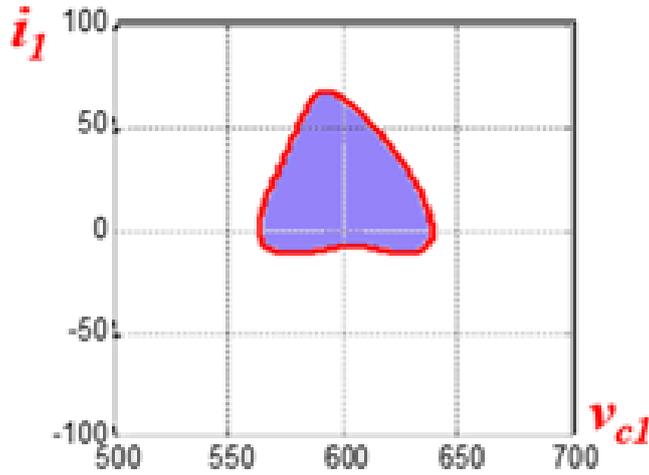


Fig. 2. 35 State trajectory of i_l and v_{cl} in example 3

Fig. 2. 36 clearly shows that, in this case, the state trajectory only travels along the α -axis; thus no even-order harmonics exists in the β -axis. Even on the α -axis, the length of projection is also shorter than example 2.

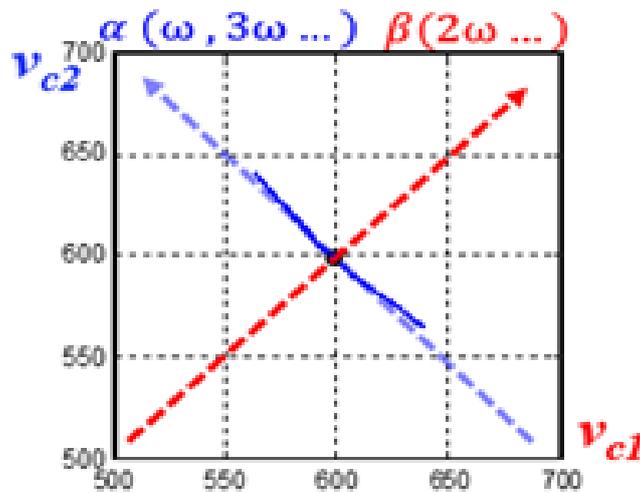


Fig. 2. 36 State trajectory of v_{c1} and v_{c2} in example 2

As discussed above, this means that no power transfers out of the phase modules to the load. Only fundamental power and third-order power are stored and exchanged between the upper module and the lower module, as shown in Fig. 2. 37.

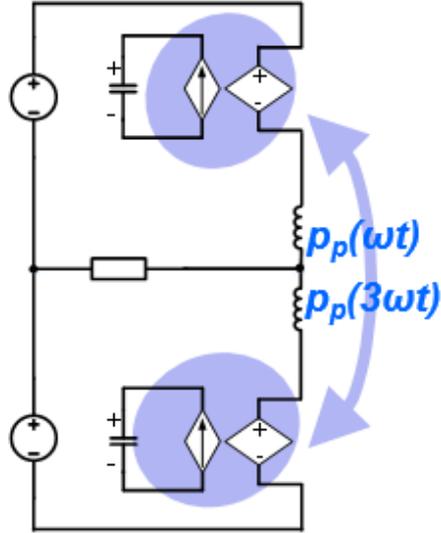


Fig. 2. 37 Power flow diagram of example 3

Example 4: Voltage Gain Control

As discussed in example 2, there is a fundamental power $p_p(\omega t)$ which is swapping between modules. If a proper voltage gain ($M=1.4$) is applied, fundamental swapping power can be eliminated [9].

With the control system in example 2, the second-order harmonic current is suppressed. As a result, the module power can be expressed as:

$$p_p = \left(\frac{1}{2M} - \frac{M}{4} \right) I_o V_o \cos \omega t - \frac{1}{2} I_o V_o \cos 2\omega t \quad (2.30)$$

According to equation (2.30), if a proper voltage gain ($M=1.4$) is applied, fundamental swapping power can be eliminated [9].

To achieve voltage gain higher than one, the module has to generate a negative voltage, which cannot be realized by the half bridge module. The full bridge module is a common selection to realize the voltage gain higher than one [9]. This phenomena is explained in Fig. 2. 38.

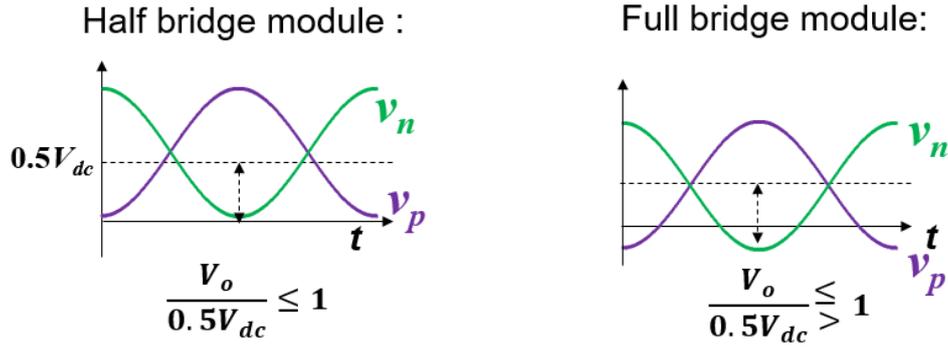


Fig. 2. 38 Average output voltages of a half bridge module and a full bridge module

The simulation waveforms of example 4 are shown in Fig. 2. 39. A higher voltage gain ($M=1.4$) increases the DC current, but eliminates the fundamental component in the capacitor voltage ripples.

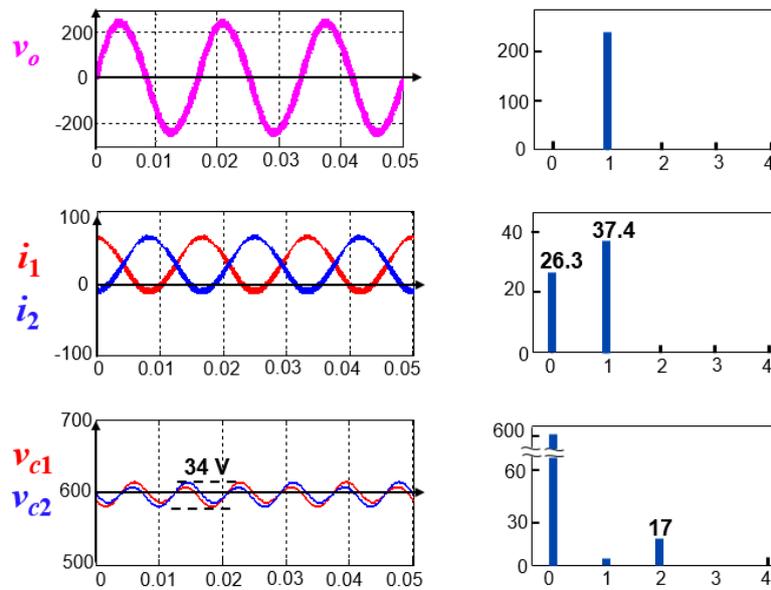


Fig. 2. 39 Simulation waveforms of example 4

In this case, the modules only provide a second-order power to the load, no fundamental power in the module, as shown in Table 2. 5.

Table 2. 5 The module power in example 4

$i_l \backslash P_p$	$p_p(DC)$	$p_p(\omega t)$	$p_p(2\omega t)$	$p_p(3\omega t)$
$\frac{M}{4} I_o$				
$\frac{1}{2} I_o \cos \omega t$			$-\frac{1}{4} I_o V_o$	
0		$M=1.4$		

In Fig. 2. 40, the blue area is eliminated. The capacitor voltage consists of only the second-order harmonic voltage, related to the green area.

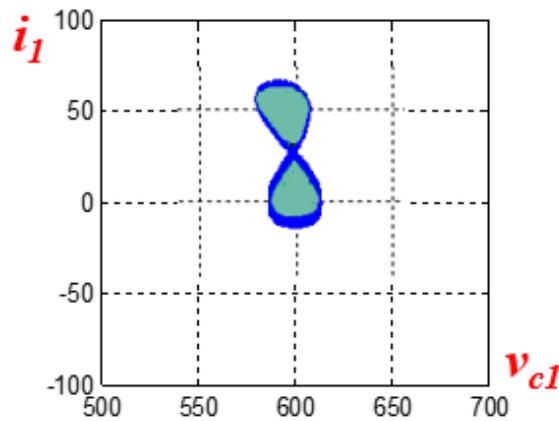


Fig. 2. 40 State trajectory of i_l and v_{c1} in example 4

Fig. 2. 41 clearly shows that in this case the state trajectory only travels along the β -axis; thus no odd-order harmonic exists in the α -axis.

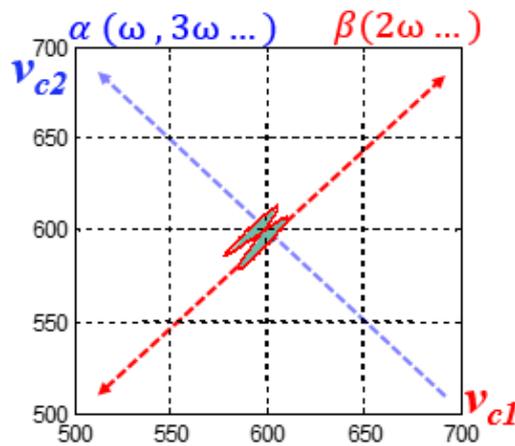


Fig. 2. 41 power flow diagram of example 4

As discussed above, there is no power swapping, but only second-order power delivered to the load from the modules, as shown in Fig. 2. 42.

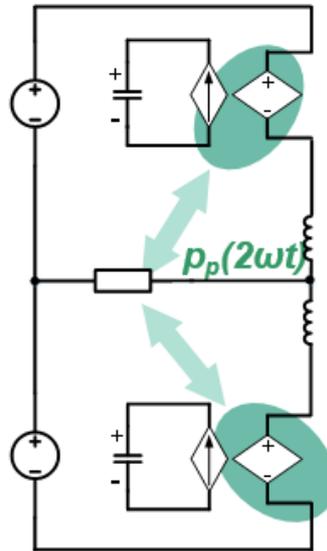


Fig. 2. 42 power flow diagram of example 4

Chapter 3 Proposed Control Strategy for Capacitor Minimization

Based on the commonly used control methods analyzed in chapter 2, a control strategy for capacitor minimization is proposed in this chapter. The proposed method can achieve a minimum voltage ripple with the full bridge MMC compared with the aforementioned examples.

3.1 Proposed Strategy: Second-order Current Injection + Gain Control

The trajectory reductions in β -axis and α -axis are considered separately in example 3 and example 4. In this proposed method, both the reductions in α -axis and β -axis are considered in order to minimize the voltage ripple. This is realized by means of controlling the voltage gain M and injecting the circulating current of the second-order harmonic.

In example 3, a second-order harmonic current is injected to eliminate the second-order order power (projection on the β -axis), but keep the fundamental and third-order power (projection on the α -axis). The equations of the arm currents can be expressed as:

$$\begin{cases} i_1 = \frac{MI_o}{4} + 0.5I_o \cos\omega t + \frac{MI_o}{4} \cos 2\omega t \\ i_2 = \frac{MI_o}{4} - 0.5I_o \cos\omega t + \frac{MI_o}{4} \cos 2\omega t \end{cases} \quad (3.1)$$

where only the injected second-order harmonic current is considered as a control freedom, since the voltage gain M is limited by being smaller than one with the half bridge MMC.

In example 4, a proper voltage gain is controlled to eliminate the fundamental power (projection on the α -axis), but keep the second-order order power (projection on the β -axis). The equations of arm currents can be expressed as:

$$\begin{cases} i_1 = \frac{MI_o}{4} + 0.5I_o \cos \omega t \\ i_2 = \frac{MI_o}{4} - 0.5I_o \cos \omega t \end{cases} \quad (3.2)$$

where the voltage gain M is controlled to 1.4 with full bridge modules, but the current injection is not considered in example 4.

In the proposed strategy with second-order harmonic injection, the arm currents are controlled to be:

$$\begin{cases} i_1 = \frac{MI_o}{4} + \frac{1}{2}I_o \cos \omega t + I_{h2} \cos 2\omega t \\ i_2 = \frac{MI_o}{4} - \frac{1}{2}I_o \cos \omega t + I_{h2} \cos 2\omega t \end{cases} \quad (3.3)$$

In the proposed strategy, both the injected harmonic current (I_{h2}) and the voltage gain (M) are considered to eliminate both the fundamental power and the second-order power in the modules.

The first step is to inject a particular second-order harmonic current, expressed as:

$$i_h = \frac{M}{4} I_o \cos 2\omega t \quad (3.4)$$

With the injected harmonic current, the module power can be expressed as:

$$p_p = \left(\frac{1}{2M} - \frac{3}{8}M \right) I_o V_o \cos \omega t - \frac{1}{8} M I_o V_o \cos 3\omega t \quad (3.5)$$

In order to eliminate the fundamental power in equation (3.5), the voltage gain (M) should be designed to be:

$$M = 1.15 \quad (3.6)$$

As a result, the module power has only a small third-order power, as expressed as:

$$p_p = \frac{1}{8} M I_o V_o \cos 3\omega t \quad (3.7)$$

The controlled voltage gain is 1.15, so the full bridge modules are required. The control system for the proposed strategy is shown in Fig. 3. 1.

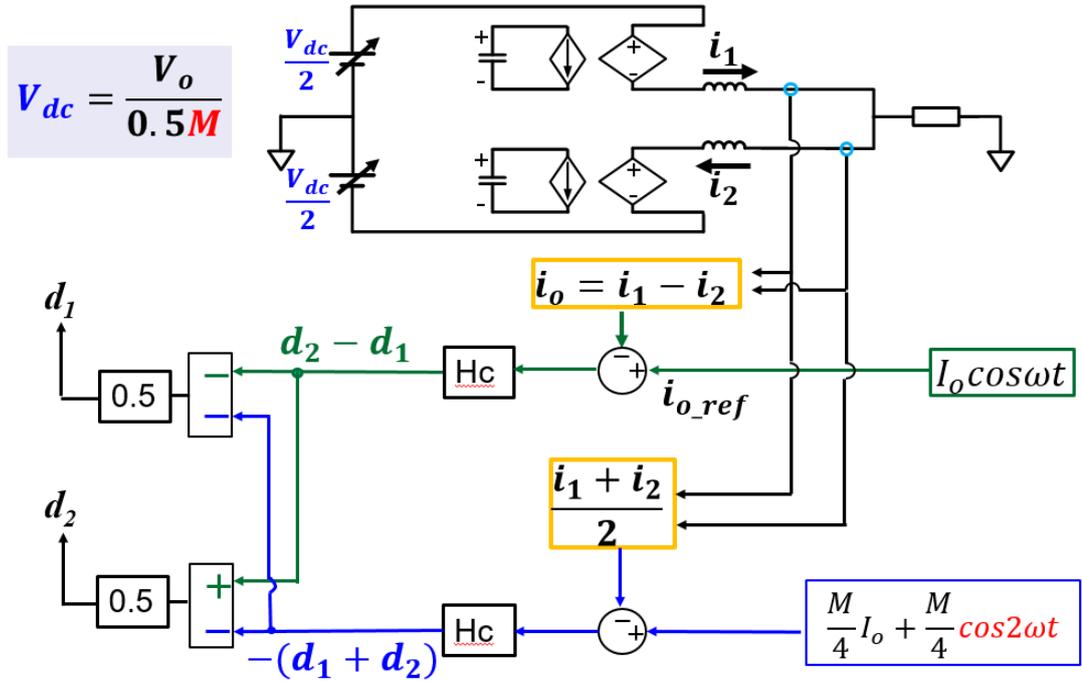


Fig. 3. 1 The control system of the proposed strategy

The simulation waveforms of the proposed control are shown in Fig. 3. 2. With a controlled voltage gain at 1.15, the DC current is larger than example 3 but smaller than example 4. A second-order harmonic component is injected in the circulating current. In the capacitor voltage ripple, there is only a small third-order component.

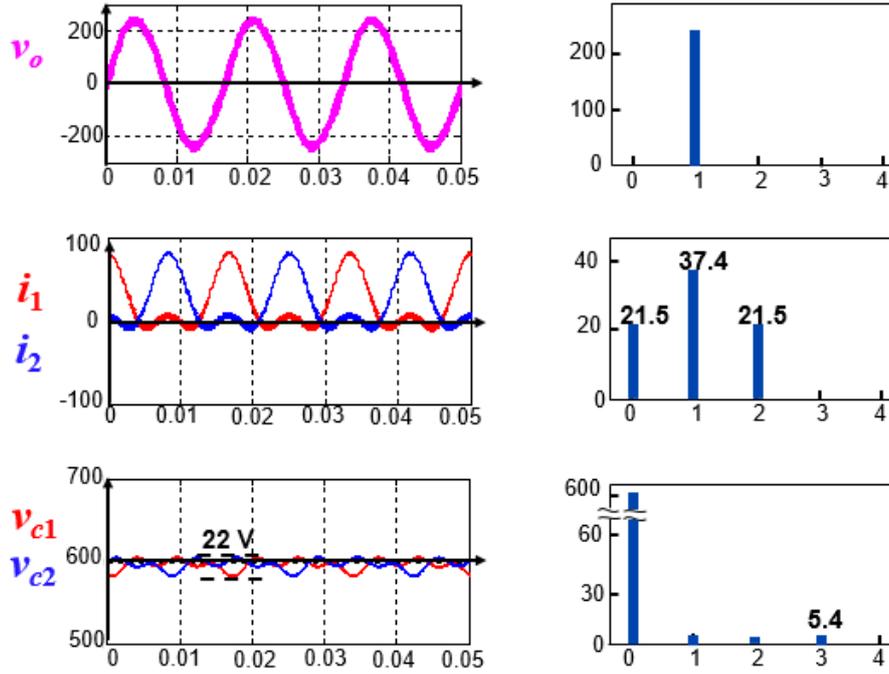


Fig. 3. 2 Simulation waveforms in the proposed control

In the proposed control, there is only a small third-order power swapping between modules. The power table is shown in Table 3. 1.

Table 3. 1 The module power in the proposed control

$i_1 \backslash P_p$	$p_p(DC)$	$p_p(\omega t)$	$p_p(2\omega t)$	$p_p(3\omega t)$
$\frac{M}{4} I_o$				
$\frac{1}{2} I_o \cos \omega t$				
$\frac{M}{4} I_o \cos 2\omega t$				$-\frac{M}{8} I_o V_o$

The state plane of i_1 and v_{c1} is shown in Fig. 3. 3, the green area is eliminated. The capacitor voltage consists of only the third-order harmonic voltage (the blue area).

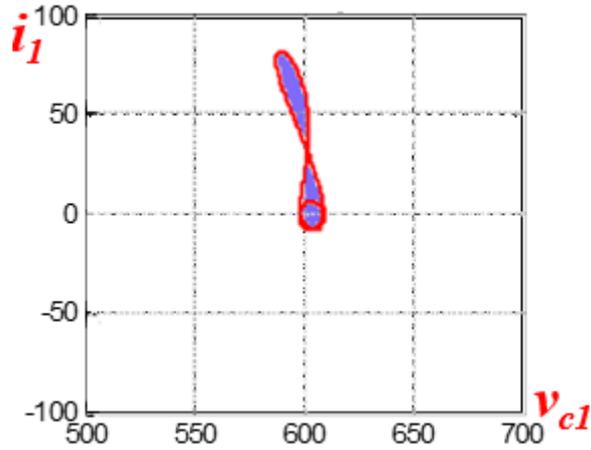


Fig. 3. 3 State trajectory of i_l and v_{c1} in the proposed control ($M=1.15$)

Fig. 3. 4 clearly shows that in this case no even-order harmonics exists in the β -axis and the state trajectory only travels along the α -axis with a small third-order component.

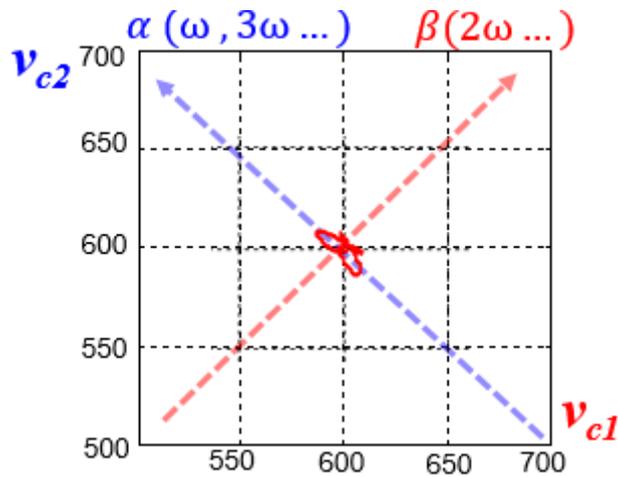


Fig. 3. 4 State trajectory of v_{c1} and v_{c2} in the proposed control ($M=1.15$)

There is no power required from the load. For the swapping power, the previous dominant fundamental power is also eliminated, and only a small amount of third-order power exists, as shown in Fig. 3. 5.

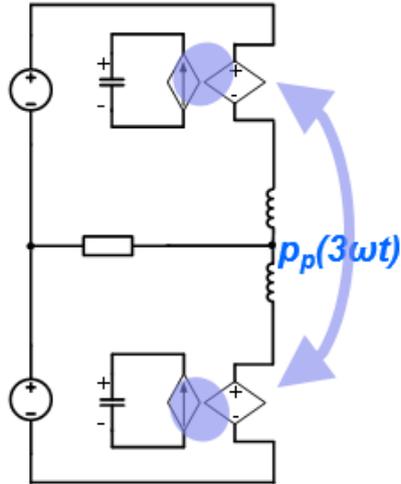


Fig. 3. 5 Power flow diagram in the proposed control ($M=1.15$)

The proposed concept is also applicable in a multilevel three phase MMC system. A simulation model with 12 modules in each arm was built to verify this concept. The parameters of the simulation model are shown in Table 3. 2.

Table 3. 2 Parameters of multilevel simulation model

DC bus voltage	7.2kV
Power rating	1MW
Switching frequency	4800Hz for HB; 2400Hz for FB
Number of modules per arm	12

The structure of the simulation model is shown in Fig. 3. 6. Both the full bridge MMC and the half bridge MMC are simulated to verify the previous analysis.

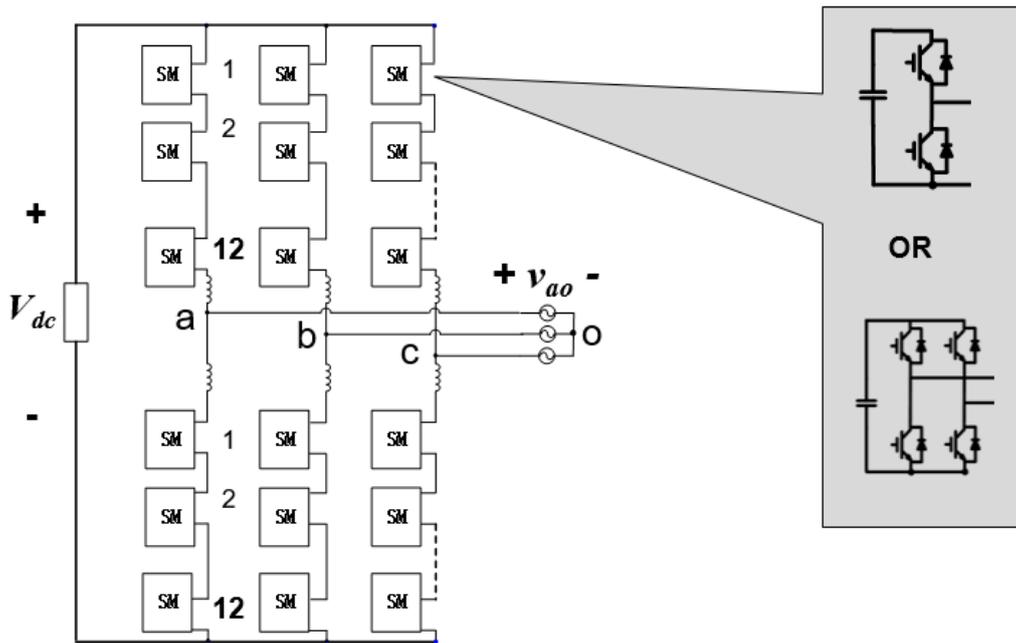


Fig. 3. 6 Structure of multilevel simulation model

The lowest capacitor voltage ripple with half bridge modules is under the control of example 3. The waveforms of the capacitor voltages are shown in Fig. 3. 7. The lowest capacitor voltage ripple with full bridge modules can be realized by the proposed control. The waveforms of the capacitor voltages are shown in Fig. 3. 8.

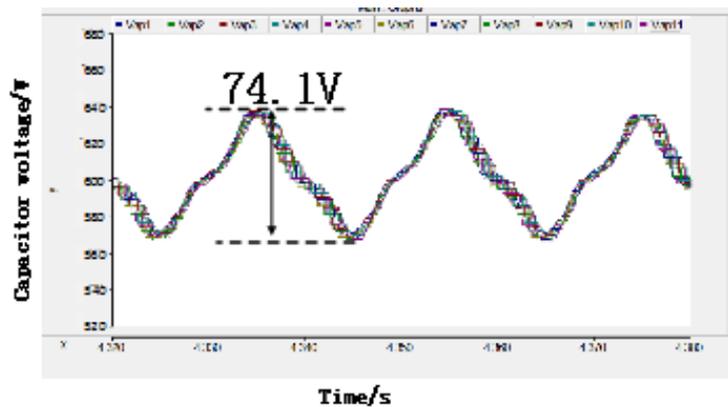


Fig. 3. 7 Capacitor voltages with half bridge modules in example 3, $M=0.9$

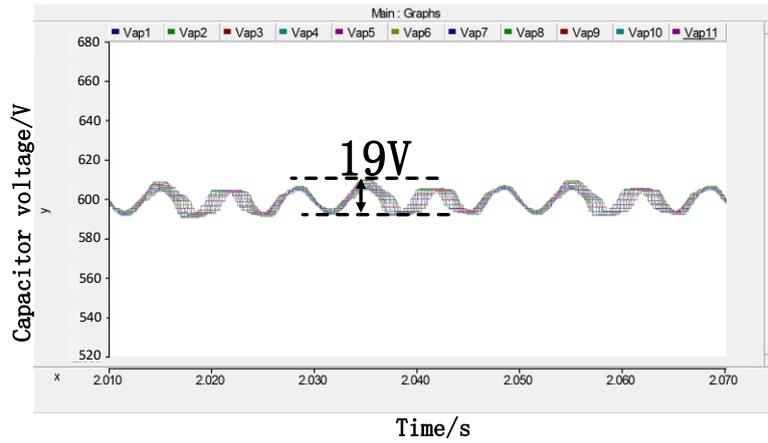
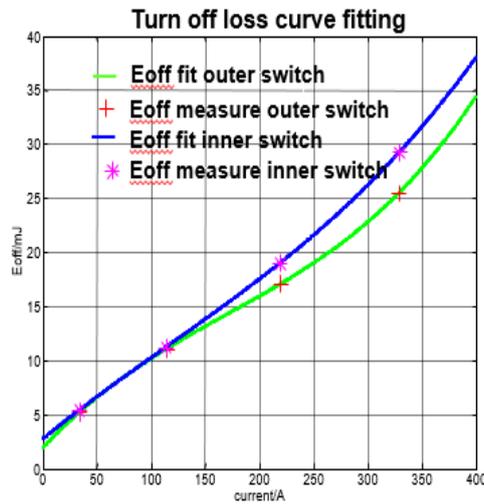
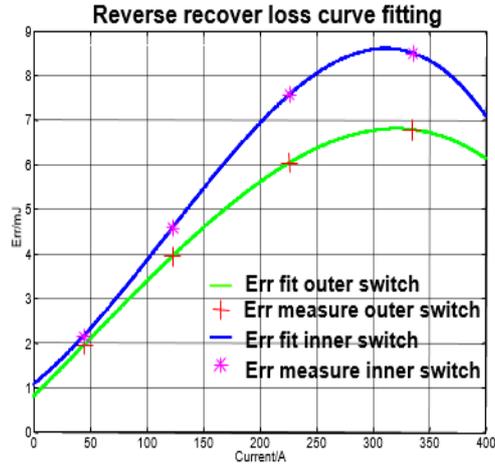


Fig. 3. 8 Capacitor voltages with full bridge modules in proposed control, $M=1.15$

The voltage ripple with the full bridge MMC is much smaller than the half bridge MMC. However, the full bridge modules will double the conduction loss. IGBT SKM400GA12V is taken as an example device to calculate the loss. As the data sheet of this device [27], the voltage rating is 1200V and the current rating is 400A. Dr. Yang Jiao from CPES of Virginia Tech presented the loss data from the double pulse test [28]. The curve fitting result of switching loss is shown in

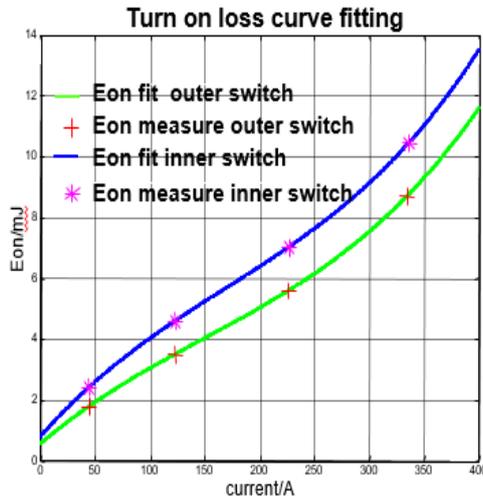


(b) The turn off loss

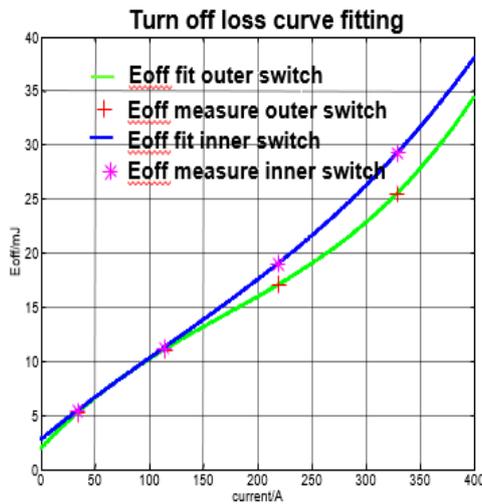


(c) The reverse recover loss

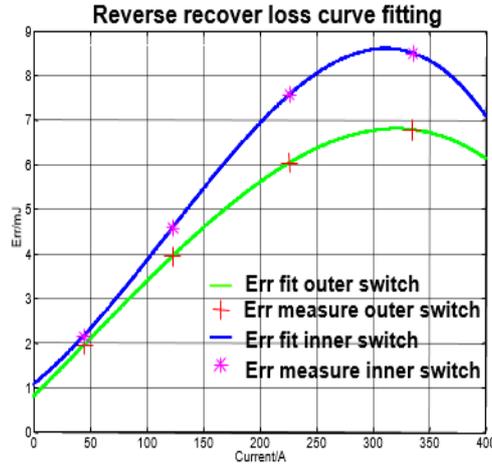
Fig. 3. 9. The data of the inner switch is used in this loss model.



(a) The turn on loss



(b) The turn off loss



(c) The reverse recover loss

Fig. 3. 9 Switching loss under different current

The loss for the half bridge MMC in example 3 and the loss for the full bridge MMC in the proposed control can be calculated, as shown in Fig. 3. 10.

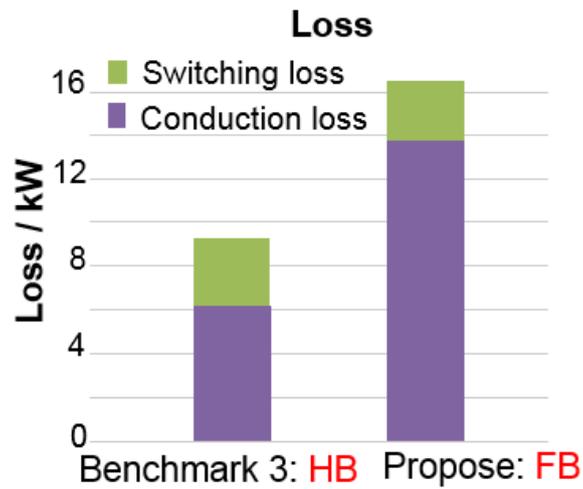


Fig. 3. 10 the loss for half bridge and loss for the full bridge

3.2 Comparison of Voltage Ripple

In example 1, example 2, and example 3 the half bridge MMC is used. Therefore, the voltage gain has to be smaller than one in these three examples. In some common

practice, the voltage gain of the half bridge MMC is designed to be 0.9 for saving some margin.

The full bridge MMC is used in example 4, so the voltage gain can be taken as a control freedom while the harmonic current is eliminated. When harmonic current is eliminated, the module power can be expressed as:

$$p_p = \left(\frac{1}{2M} - \frac{M}{4}\right)I_oV_o \cos \omega t - \frac{1}{2}I_oV_o \cos 2\omega t \quad (3.8)$$

In the proposed strategy, a particular value of second-order harmonic circulating current is injected, the module power can be expressed as:

$$p_p = \left(\frac{1}{2M} - \frac{4M}{8}\right)I_oV_o \cos \omega t - \frac{M}{8}I_oV_o \cos 3\omega t \quad (3.5)$$

As discussed in the previous section, the capacitor voltage ripple is decided by the module power. The relationship is shown in equation (3.9):

$$\begin{cases} v_{c1} = V_c + \frac{1}{CV_c} \int_0^t p_p dt \\ v_{c2} = V_c + \frac{1}{CV_c} \int_0^t p_n dt \end{cases} \quad (3.9)$$

By substituting the power equation (3.8) and (3.5) into (3.9) respectively, the peak-to-peak value of the capacitor voltage ripple can be calculated for the different control methods.

Fig. 3. 11 shows the normalized peak-to-peak value of the capacitor voltage ripples under different control methods. The author of example 4 found an optimized value of M for minimizing the voltage ripple. The discussion in this thesis extends the range of M . By substituting the power equation (3.8) into (3.9), the voltage ripple can be calculated at a different value of M , as the blue curve in Fig. 3. 11. The red curve is

from the proposed control. By substituting the power equation (3.5) into (3.9), the voltage ripple can be calculated at a different value of M , as the red curve.

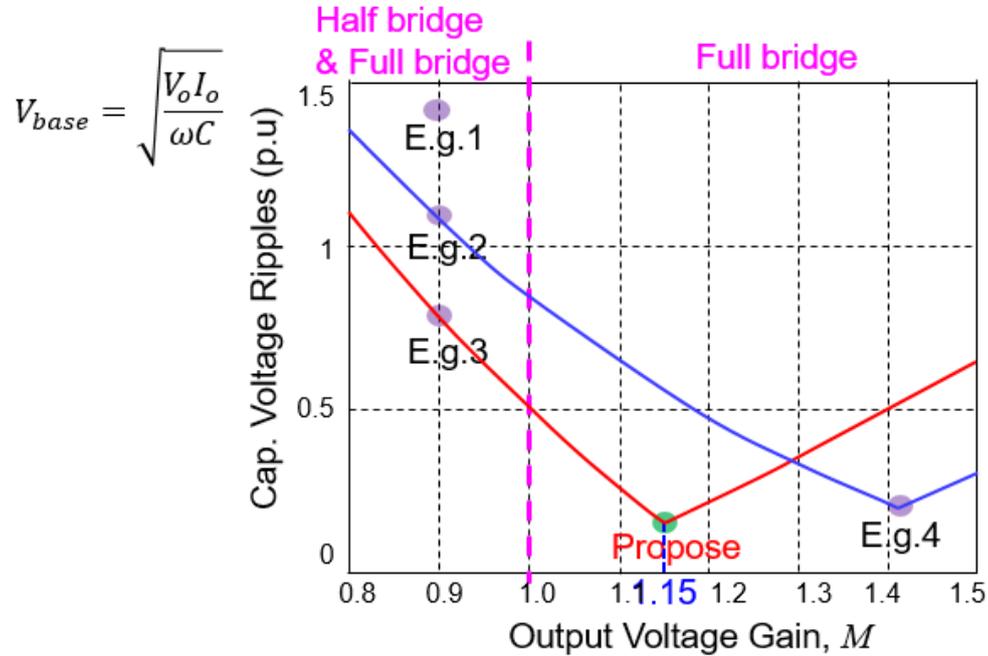


Fig. 3. 11 Comparison of different control methods

In Fig. 3. 11, the voltage gain of the half bridge MMC can only be controlled in the range of lower than one, while the voltage gain of the full bridge MMC can be controlled in the whole range. M is usually designed to be around 0.9 if the half bridge topology is employed for the MMC, to provide some margin for the duty cycle control.

Fig. 3. 11 clearly shows that the proposed control can achieve the lowest voltage ripple, at the optimized point of $M=1.15$. The proposed method (red curve) also enjoys a lower capacitor voltage ripple than the method in example 4 (blue curve) even when the voltage gain is smaller than 1.15. In the proposed method, the voltage ripple is being reduced rapidly with the increasing of M before the optimized point ($M=1.15$).

3.3 Can the Proposed Control Method Be Extended to Eliminate the Third-order Power?

Is it possible to further eliminate the third-order power? A logical extension is to inject:

$$i_{har} = \frac{M}{4} I_o \cos 2\omega t - \frac{M}{4} I_o \cos 4\omega t \quad (3.8)$$

where the voltage gain (M) is still 1.15. The third-order power can be eliminated, but additional fourth-order power and fifth-order power are created:

$$p_p = -\frac{1}{4} I_o V_o \cos 4\omega t + \frac{M}{8} I_o V_o \cos 5\omega t \quad (3.9)$$

Fig. 3. 12 shows the comparison of the capacitor voltage ripples between the proposed method (2nd order injection) and the method of 2nd & 4th order injection. The proposed method has a smaller voltage ripple than the method of 2nd & 4th order injection. In this case, there is no benefit from the higher order current injection.

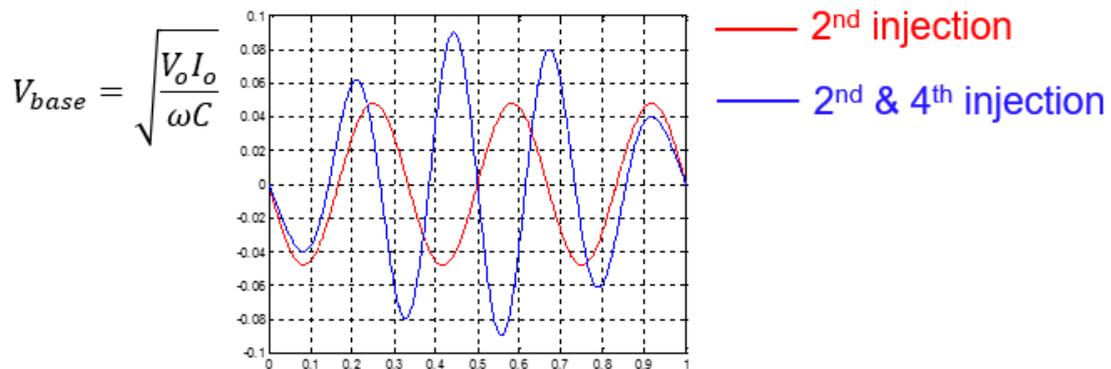


Fig. 3. 12 Voltage ripple with higher order current injection

Fig. 3. 13 shows the voltage ripple with 2nd & 4th order current injection, compared with the proposed control (2nd injection). At a different value of M , the fourth-order current always increases the voltage ripple even though it can eliminate the third-order power.

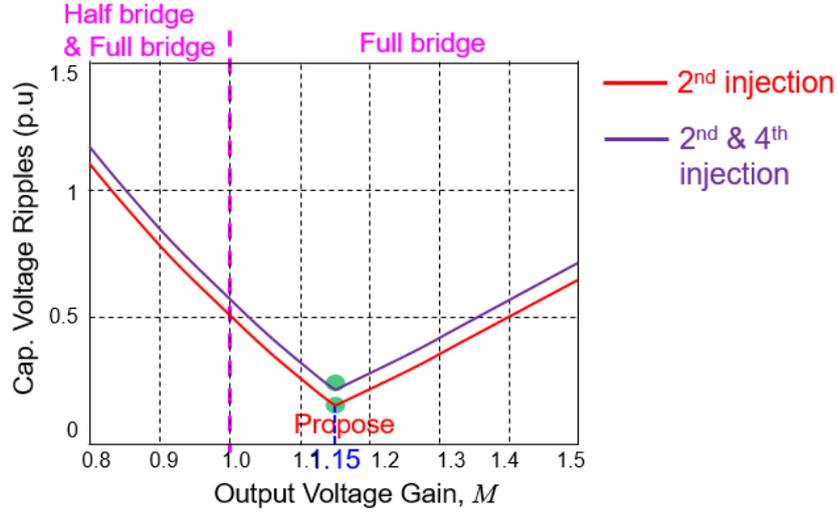


Fig. 3. 13 Comparison between the 2nd order injection and 2nd & 4th order injection

3.4 Discussion of the Reactive Load

The previous discussion was based on the active load for simplicity. However, the conclusion is valid for a more general case. For a reactive load, the load current can be expressed as:

$$i_o = I_o \cos(\omega t + \varphi) \quad (3.10)$$

where φ is the phase angle of the load current.

To eliminate the second-order power in the module, a proper second-order circulating current should be injected, expressed as:

$$i_{har} = \frac{M}{4} I_o \cos\varphi (\cos 2\omega t) - \frac{M}{4} I_o \sin\varphi (\sin 2\omega t) \quad (3.11)$$

As a result, the module power can be expressed as:

$$\begin{aligned}
p_p = & \frac{1}{2} I_o V_o \cos\varphi \left[\left(\frac{1}{M} - \frac{3M}{4} \right) \cos\omega t - \frac{M}{4} \cos 3\omega t \right] \\
& + \frac{1}{2} I_o V_o \sin\varphi \left[\left(\frac{1}{M} - \frac{M}{4} \right) \sin\omega t - \frac{M}{4} \sin 3\omega t \right]
\end{aligned} \tag{3.12}$$

In equation (3.12), the factor of “ $\cos\omega t$ ” is different from the factor of “ $\sin\omega t$ ”, so controlling M cannot eliminate all the fundamental components if neither “ $\cos\varphi$ ” nor “ $\sin\varphi$ ” is zero. However, an optimized value of M can be found to realize the minimum voltage ripple for any value of φ , as shown in Fig. 3. 14. At two special points, all the fundamental power can be eliminated: one is the pure active load ($\varphi = 0$); one is the pure reactive load ($\varphi = \frac{\pi}{2}$).

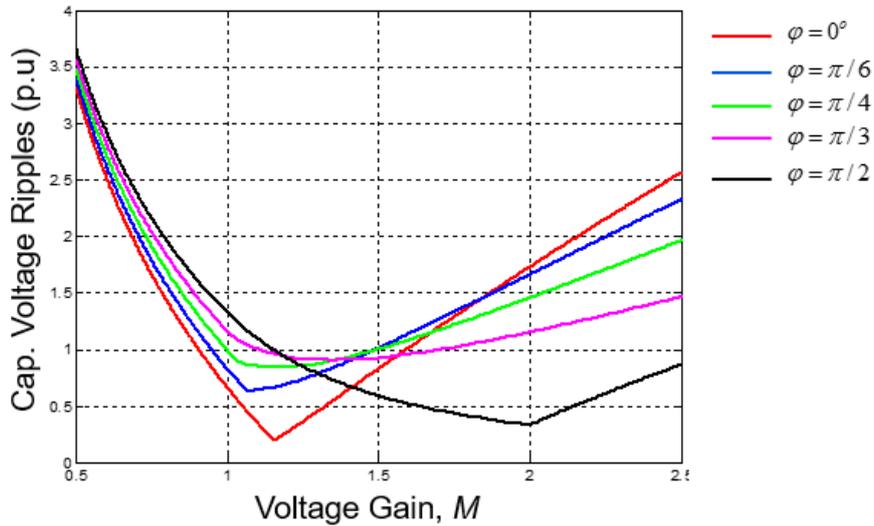


Fig. 3. 14 Voltage ripple at a different phase angle of the load current

A 3D figure can be derived to demonstrate the influence of voltage gain and phase angle on the voltage ripple, as shown in Fig. 3. 15. One horizontal axis is the voltage gain, M ; another horizontal axis is the phase angle, Rad. For any values of the voltage gain and the phase angle, the capacitor voltage ripple can be calculated, which is the vertical axis. The minimum voltage ripple is at the active load ($\varphi = 0$) and $M=1.15$.

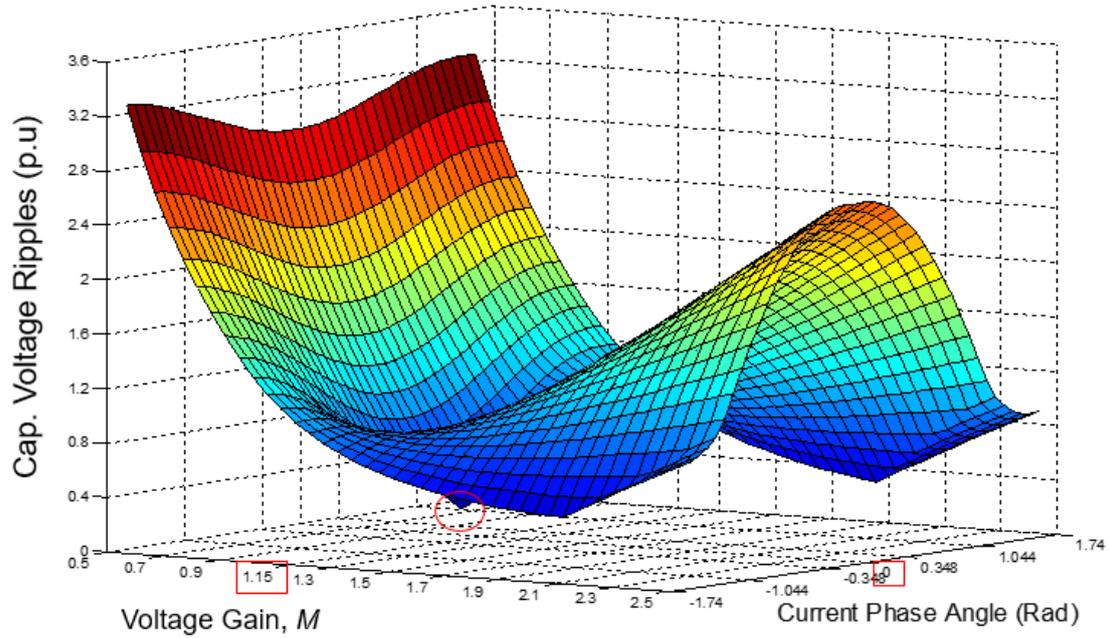


Fig. 3. 15 Voltage ripple vs. voltage gain and phase angle

3.5 Introduction of Topologies on Fault Protection

For the safety and reliability, DC fault protection is a rising requirement in HVDC systems [29]. The widely used half bridge MMC has the advantage of a lower loss, but it cannot provide fault protection. When there is a short-circuit fault on the DC bus in the half bridge MMC, although all the switches are turned off, the diodes are still conducting the fault current. This phenomena is shown in Fig. 3. 16.

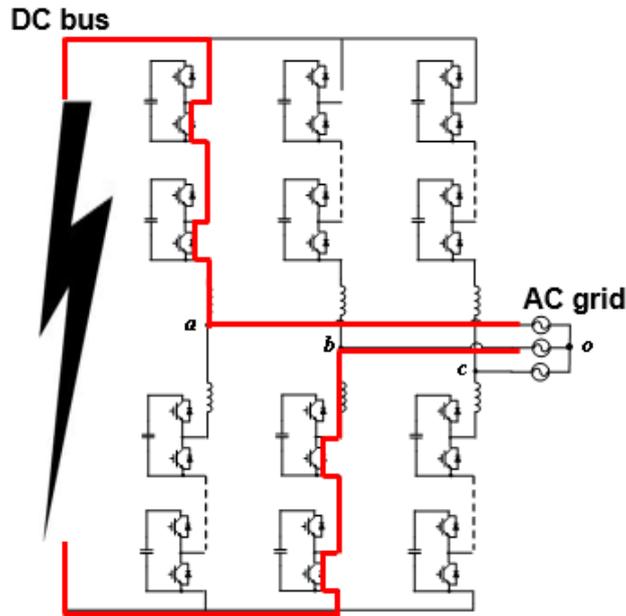


Fig. 3. 16 DC bus fault under the half bridge MMC

The fault protection can be provided by the full bridge MMC. When there is a short-circuit fault, the full bridge MMC forces the current to flow through the diodes into the capacitors, shown in Fig. 3. 17. As long as the summation of all the capacitor voltages is larger than the line-to-line voltage of the grid, the diodes will be blocked and the fault current will be cleared in this path.

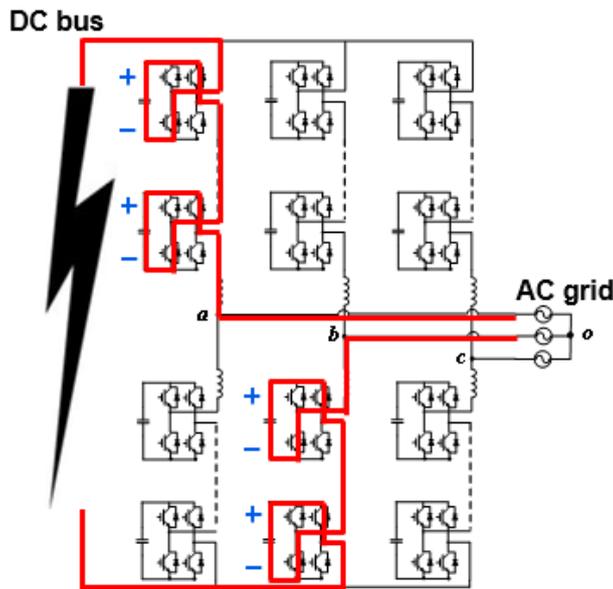


Fig. 3. 17 The path of fault current in full bridge MMC

3.6 Discussion of Hybrid MMC

The half bridge MMC has the benefit of a low conduction loss, whereas the full bridge MMC has the DC fault clearing capability. Therefore, a hybrid MMC, in which a combination of half bridge modules and full bridge modules, as shown in Fig. 3. 18 was proposed [29]. In such manner, the converter has a reasonable loss but still has the DC fault clearing capability.

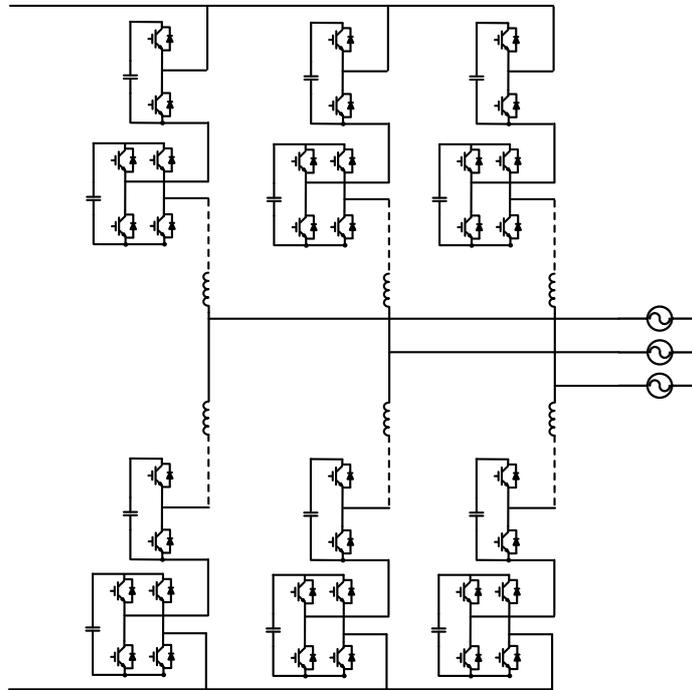


Fig. 3. 18 Structure of hybrid MMC

When there is a short-circuit fault, the fault current will still flow through the capacitors of the full bridge modules. The current path is shown in Fig. 3. 19. If the summation of the capacitor voltages in the full bridge modules is larger than the line-to-line voltage, the fault current will be cleared.

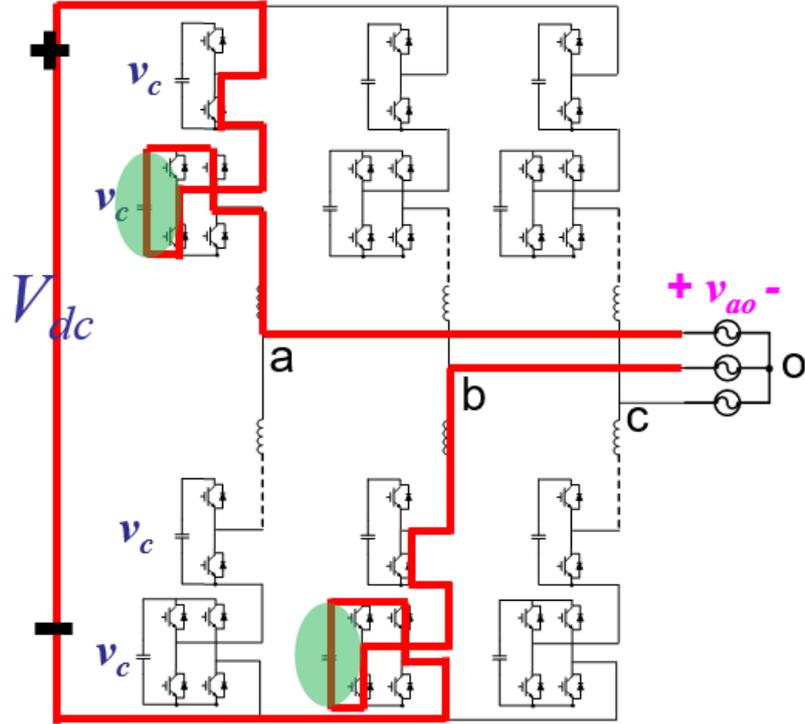


Fig. 3. 19 Fault current path in hybrid MMC

To calculate the minimum number of full bridge modules for protection, the following notations are defined:

N: the total number of modules in one arm;

F: the number of full bridge modules in one arm.

In Fig. 3. 19, $v_{ao} = V_o \cos \omega t$ represents the output voltage. The output voltage of the upper arm can be expressed as:

$$v_p = \frac{1}{2} V_{dc} - v_{ao} \quad (3.13)$$

The peak voltage of the output voltage of the upper arm can be expressed as:

$$v_{p_peak} = \frac{1}{2} V_{dc} (1 + M) \quad (3.14)$$

where $M = \frac{V_o}{0.5V_{dc}}$ represents the voltage gain.

In the following analysis, the capacitor voltage in each module is assumed to be the same, v_c .

The capacitor voltage should be larger than the output voltage of the modules,

$$Nv_c \geq v_{p_peak}, \quad (3.15)$$

so the minimum capacitor voltage is:

$$V_{cMIN} = \frac{V_{dc}(1+M)}{2N} \quad (3.16)$$

Assuming that the capacitor voltage is designed to meet the minimum requirement, which is $v_c = V_{cMIN}$, the DC-fault blocking condition is

$$2Fv_c \geq V_{ab} = \sqrt{3}V_o, \quad (3.17)$$

where V_{ab} represents the peak value of the line-to-line voltage in the AC grid.

The required ratio of full bridge modules can be expressed as:

$$\frac{F}{N} \geq \frac{\sqrt{3}}{2} \frac{M}{1+M} \quad (3.18)$$

The required ratio of full bridge modules is shown in Fig. 3. 20. If the design is located in the green area, the hybrid MMC has the fault protection ability. In a common design, the voltage gain is around one, so the ratio is usually designed as $F/N = 0.5$.

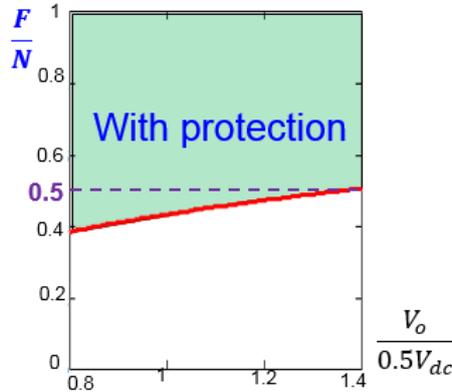


Fig. 3. 20 The required ratio of full bridge modules

3.7 Capacitor Reduction for Hybrid MMC

Referring to Fig. 3. 21, the output voltage for each half bridge (HB) module, v_h , and full-bridge (FB) module, v_f , are controlled using the same duty cycle control law [14]. Since the output voltage of the half bridge module has to be greater than zero, a voltage gain (M) is always less than one.

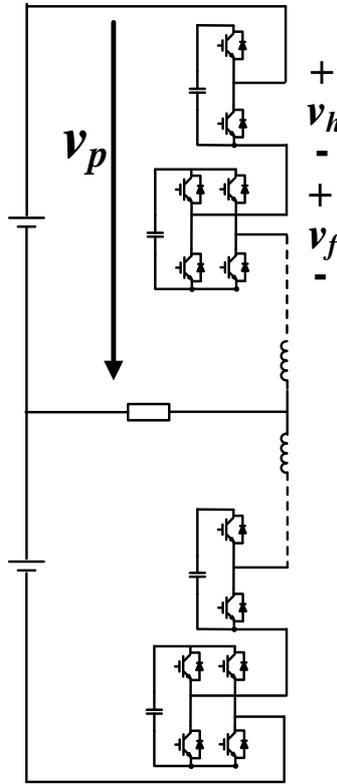


Fig. 3. 21 The structure of a single phase Hybrid MMC

In order to achieve a more desired condition, $M > 1$, Yi-Hsun Hsieh from CPES of Virginia Tech proposed that a third-order harmonic voltage is injected in v_h and v_f :

$$\begin{cases} v_h = \frac{1}{F+H} \frac{V_o}{M} [1 - M \cos \omega t + yM \cos 3\omega t] \\ v_f = \frac{1}{F+H} \frac{V_o}{M} [1 - M \cos \omega t - \frac{H}{F} yM \cos 3\omega t] \end{cases} \quad (3.19)$$

where H is the number of half bridge modules, F is the number of full bridge modules; y represents the amplitude of the injected voltage, and the optimum value of y will be determined later.

Although there is third-order voltage in each module, the summation of module output voltages is still:

$$v_p = Hv_h + Fv_f = \frac{1}{2}V_{dc} - v_{ao} \quad (3.20)$$

With the help from the full bridge submodules, the voltage gain, M , now can be greater than one while the outputs of the half-bridge modules are still always positive.

To explain this concept in detail, a simplified model is built, shown in Fig. 3. 22, where there is one full bridge module and one half bridge module in each arm.

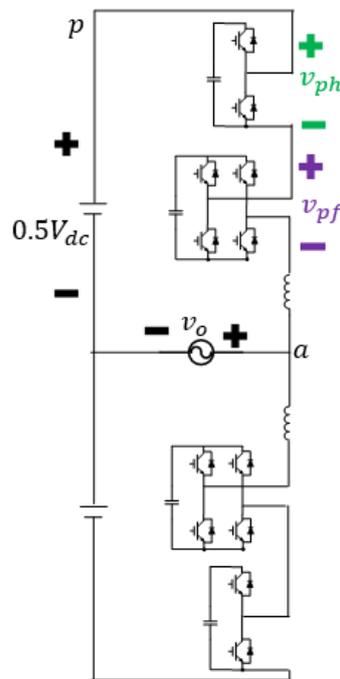


Fig. 3. 22 The example of two modules hybrid MMC

The output voltage of the upper arm is the summation of the half bridge module and the full bridge module:

$$v_p = v_{pf} + v_{ph} \quad (3.21)$$

Based on KVL, the output voltage of the upper arm can be expressed as:

$$v_p = \frac{V_o}{M} - V_o \cos \omega t \quad (3.22)$$

Yi-Hsun Hsieh proposed a third-order harmonic injection in the full bridge module, such that

$$v_{pf} = \frac{1}{2} v_p - y \cos(3\omega t), \quad (3.23)$$

and a third-order harmonic injection in the half bridge module, such that

$$v_{ph} = \frac{1}{2} v_p + y \cos(3\omega t) \quad (3.24)$$

The equations (3.23) and (3.24) can be illustrated in Fig. 3. 23, where the voltage gain $M > 1$ with Hsieh's method.

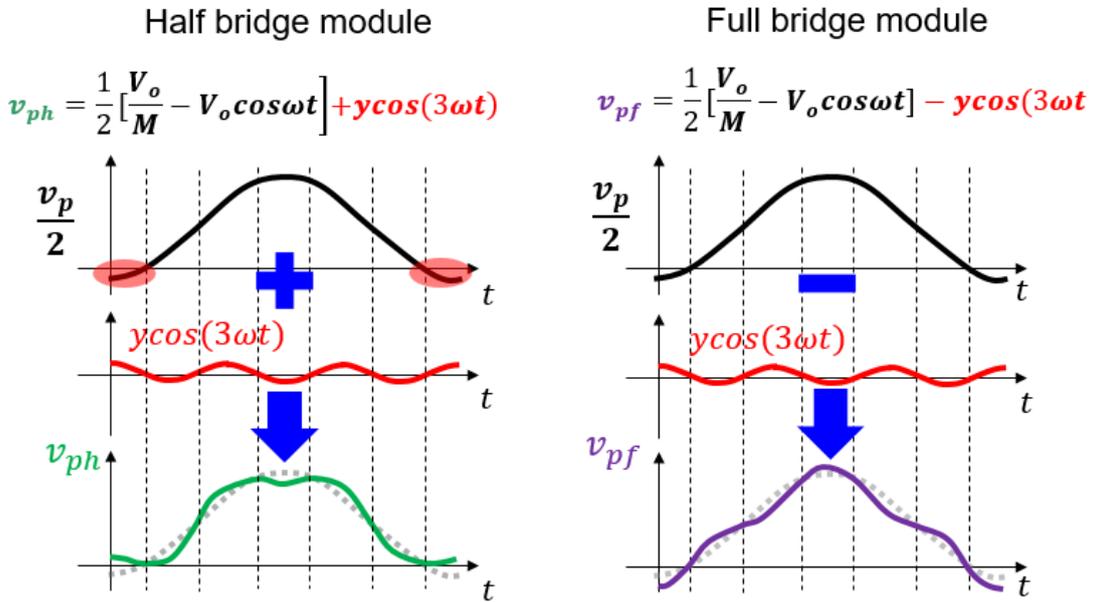


Fig. 3. 23 Concept of injecting 3rd order voltage in hybrid MMC, $M > 1$

In Fig. 3. 23, the black waveforms are $\frac{1}{2} v_p$. When $M > 1$, the waveform of $\frac{1}{2} v_p$ will be negative during some time (shown in the red area), which cannot be realized

by the half bridge module. To avoid a negative output voltage of the half bridge module, a third-order voltage (red waveform) is injected into the half bridge module. As a result, the total output voltage v_{ph} (green waveform) is always positive. This injected voltage should not affect the output of the arm voltage (v_p). An opposite third-order voltage is also injected into the full bridge module. As a result, a higher voltage gain ($M > 1$) can be realized in the hybrid MMC. This control method can be realized by the control diagram shown in Fig. 3. 24.

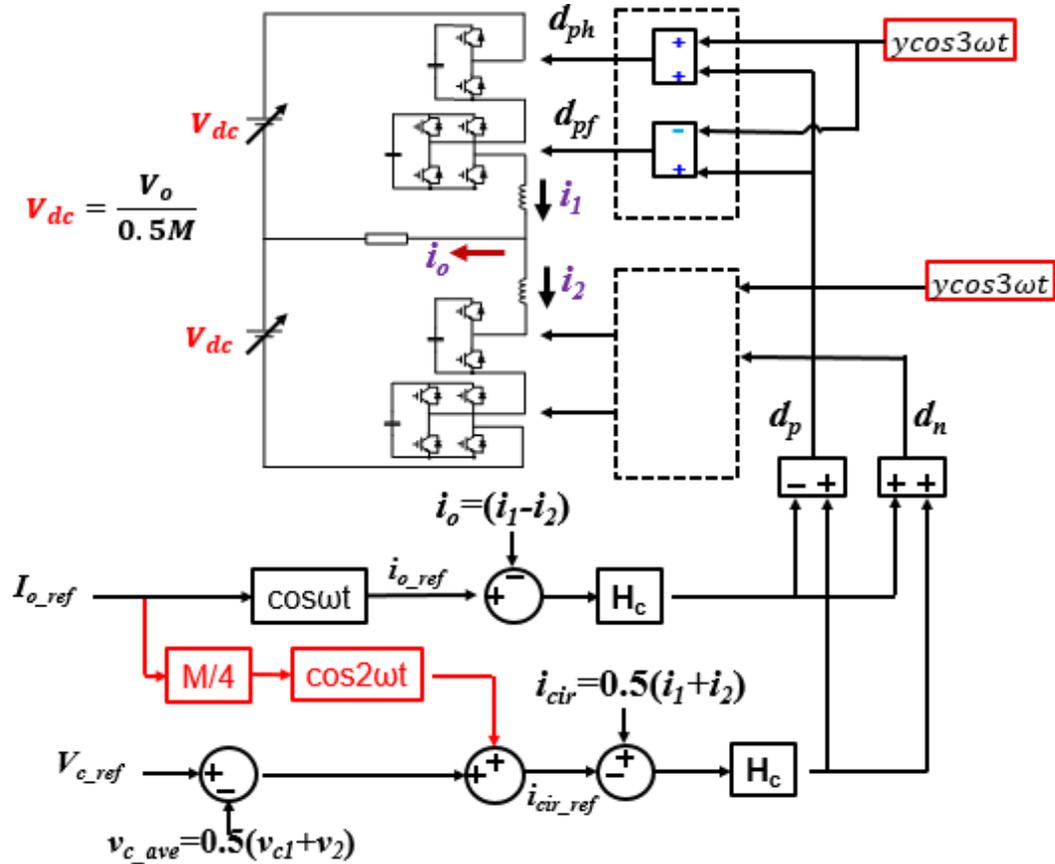


Fig. 3. 24 Control diagram of the hybrid MMC

In Hsieh's method, the duty cycle of the half bridge module can be expressed as:

$$d_{ph} = v_{ph}/V_c = 0.5[1 - M\cos\omega t + yM\cos 3\omega t] \quad (3.25)$$

Ideally, the upper limit of the duty cycle is one, and the lower limit of the duty cycle is zero, so the extreme voltage gain is one in a traditional half bridge MMC (without the third-order voltage injection), shown in Fig. 3. 25.

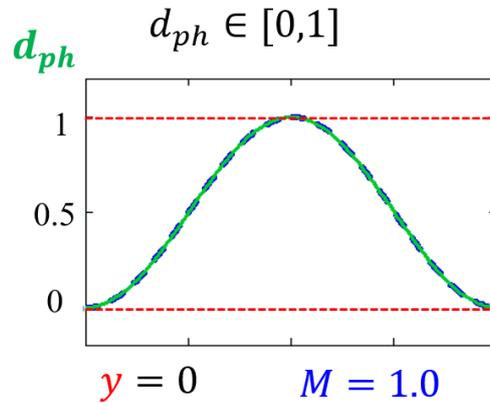


Fig. 3. 25 The duty cycle when $y=0$

With the increasing of y , the voltage gain can be increased, but the duty cycle is still in the range of $[0,1]$. The largest voltage gain happens at the point of $y=0.17$, as shown in Fig. 3. 26. The blue dot curve is the duty cycle without injection, $0.5(1-M\cos\omega t)$, showing that $M>1$ with the injection.

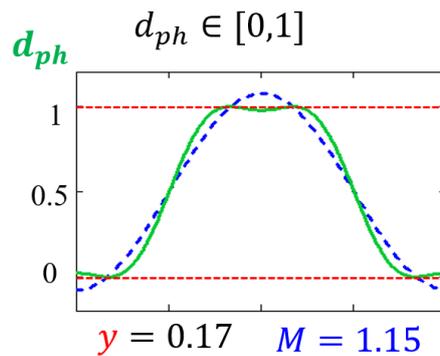


Fig. 3. 26 The largest voltage gain when $y=0.17$

If the injection (y) keeps increasing, the voltage gain will decrease adversely, as shown in Fig. 3. 27. Too much injection will also make the duty cycle exceed the limits.

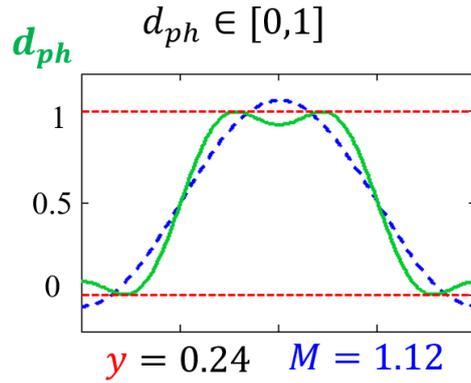


Fig. 3. 27 The duty cycle when $y=0.24$

With plenty of simulation points, a curve of voltage gain (M) vs. injection (y) can be drawn, as shown in Fig. 3. 28.

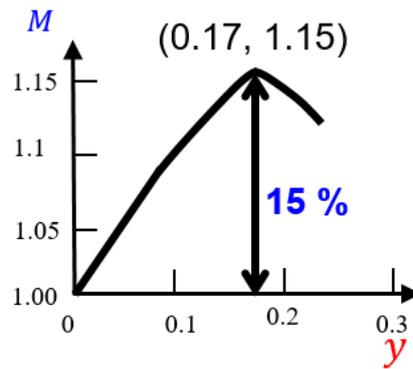


Fig. 3. 28 The voltage gain vs. the injected voltage

A curve of the capacitor voltage ripple vs. the voltage gain in hybrid MMC can be drawn, as shown in Fig. 3. 29. The green curve represents Hsieh's method for the hybrid MMC. With the increasing of the injection (y), the voltage gain can be increased to be as high as 1.15. But, an over injected voltage will adversely decrease the voltage gain, as the green dot line.

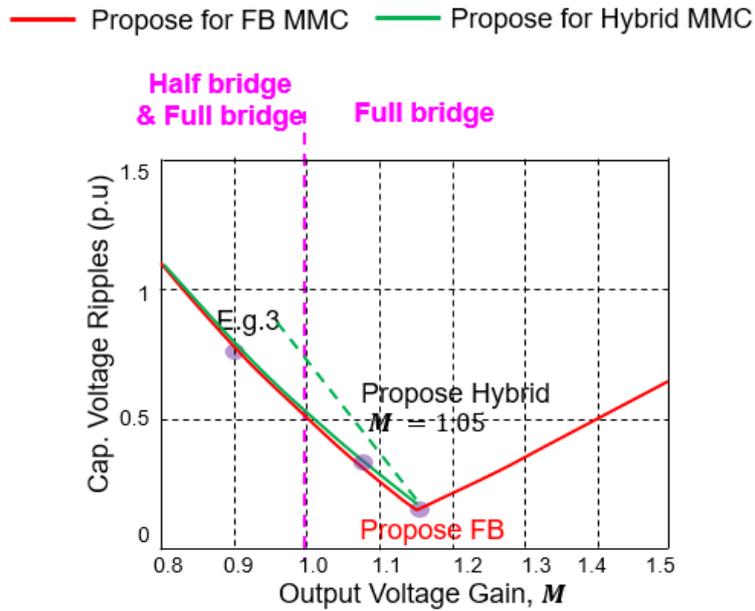


Fig. 3. 29 The effect of proposed method for hybrid MMC

In practice, some margin has to be preserved for control in the duty cycle. A typical value of margin is 10%. In Fig. 3. 29, the indicated voltage gain for the half bridge MMC is 0.9. Similarly, the indicated voltage gain for the hybrid MMC is 1.05. At the point of $M=1.05$ in the hybrid MMC, the duty cycle of one half bridge module is shown in Fig. 3. 30. The upper limit is changed to be 0.95, and the lower limit is changed to be 0.05.

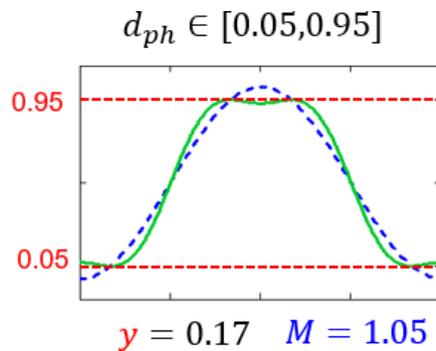


Fig. 3. 30 The duty cycle when 10% margin is saved in duty cycle

A simulation model is built to verify this concept for the hybrid MMC. The simulation model and waveforms are shown in Fig. 3. 31. It shows that this method can reduce the capacitor voltage ripple significantly while maintaining a sinusoidal output voltage.

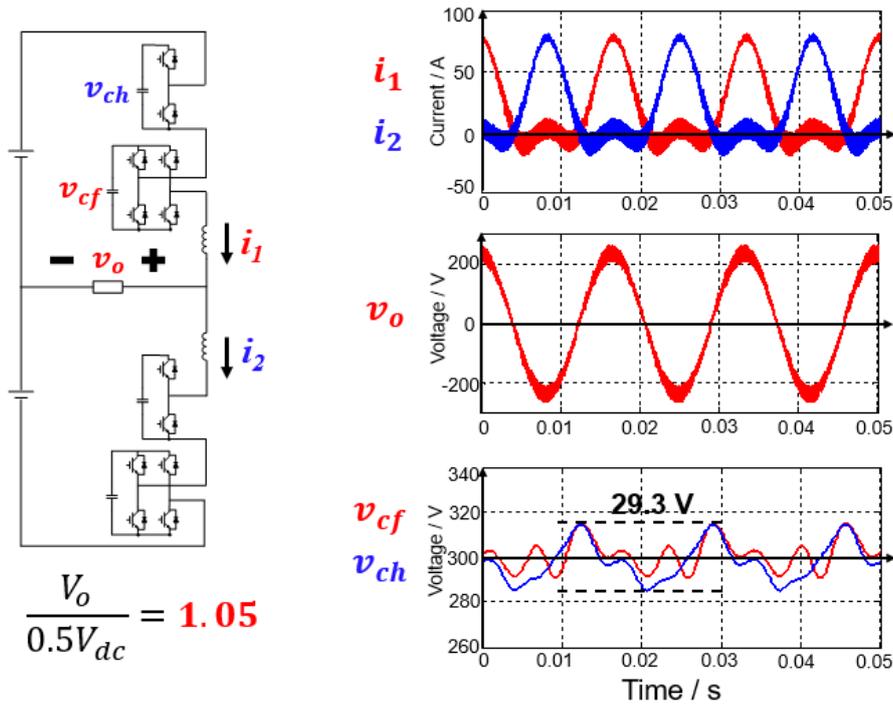


Fig. 3. 31 The simulation for the proposed method in hybrid MMC

To compare the losses of the half bridge MMC, the full bridge MMC and the hybrid MMC, the loss model shown Fig. 3. 6 is utilized.

The half bridge MMC is controlled as example 3, where the voltage gain is 0.9. The hybrid MMC is controlled with the Hsieh's method, where the voltage gain is 1.05. The full bridge MMC is controlled with the proposed method, where the voltage gain is 1.15. Based on the criterion of the same voltage ripple, the capacitance of one module in each case is shown in Fig. 3. 32. The full bridge MMC has the smallest

required capacitance. The hybrid MMC is the middle one between the full bridge MMC and the half bridge MMC.

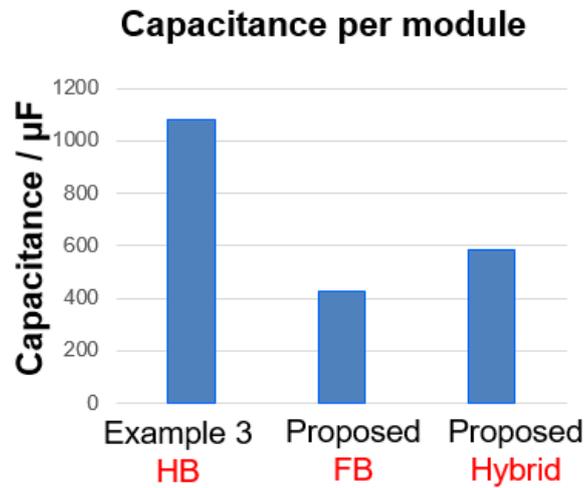


Fig. 3. 32 Capacitors per module under the same voltage ripple

Fig. 3. 33 gives the loss comparison. The full bridge MMC has the largest loss, because of the doubled conduction loss when compared with the half bridge MMC. A hybrid MMC is also at a middle position between the half bridge MMC and the full bridge MMC. It is worth of mentioning that only the full bridge MMC and the hybrid MMC have the capability of fault protection.

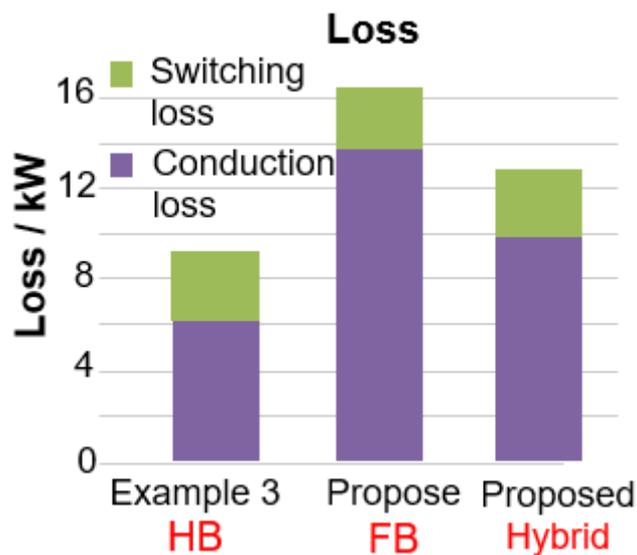


Fig. 3. 33 Loss comparison

3.8 Discussion and Conclusion

A novel control strategy for capacitor reduction was proposed in this chapter. The strategy can eliminate completely both the fundamental component and the second-order component of the capacitor voltage, by means of the second-order harmonic current injections in conjunction with voltage gain control ($M=1.15$). Ideally, the proposed strategy works with full bridge topology. Furthermore, the concept can be extended to the hybrid MMC, by injecting a third-order voltage in both the half bridge modules and the full bridge modules. Combined with the gain control ($M=1.05$) in the hybrid MMC, the capacitors can be reduced by 50% compared with half bridge MMC, but the loss is increased by 45%.

Chapter 4 Hardware Experiments

A scaled down hardware of the three phase MMC system is built to verify the concept. The hardware structure and the software structure will be explained in this chapter. Finally, the experimental results are shown to verify the concepts.

This prototype of a scale down MMC is the result of a team efforts, including Wei Zhang, Kai Li, Chen Li, Dr. Rong Xu and Yadong Lyu.

4.1 Introduction of Scaled Down Hardware

The scaled down MMC architecture is shown in Fig.4. 1. The three phase scaled down hardware has 24 modules in total, 4 modules per arm. Each module is implemented with a full bridge. However, this module can operate as a full bridge module or a half bridge module. The master DSP synchronizes three phase DSP boards. Each DSP board has one DSP chip and one CPLD chip. The DSP board communicates with the module boards through the interface board. Table 4. 1 gives the parameters of the scaled down hardware.

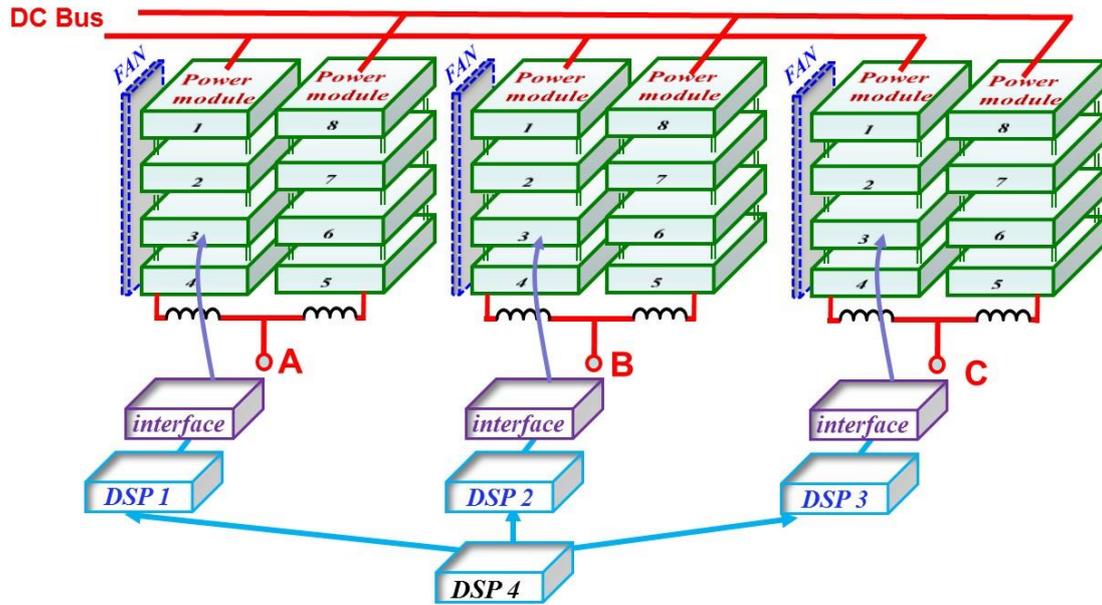


Fig.4. 1 The scaled down MMC architecture

Table 4. 1 the parameters of the scaled down MMC

DC bus voltage	600V
DC current	3 A
Power rating	5.4 kW
Arm inductor (L)	0.3mH
Module capacitance	1200 μ F
Switching frequency	Up to 10kHz
Modules per arm	4

Fig.4. 2 shows the structure of one phase. All module boards of one phase are plugged into the interface board. The interface board offers the PWM signal connection and A/D signal connection between the module boards and the control board.

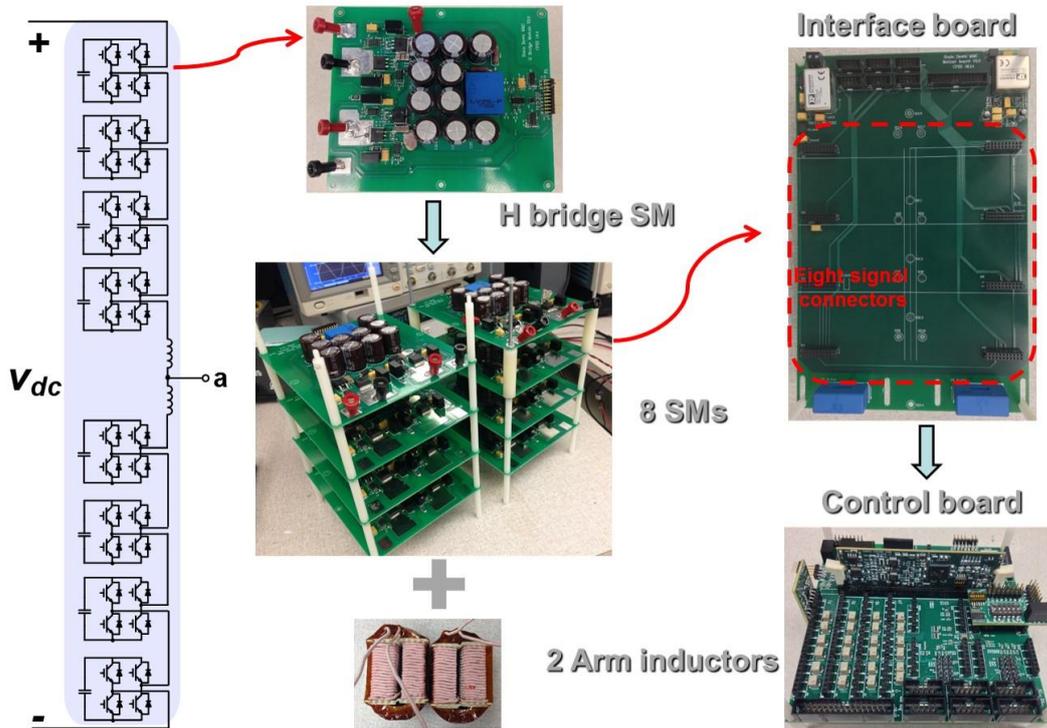


Fig.4. 2 the contracture of one phase

The picture of the interface board is shown in Fig.4. 3.

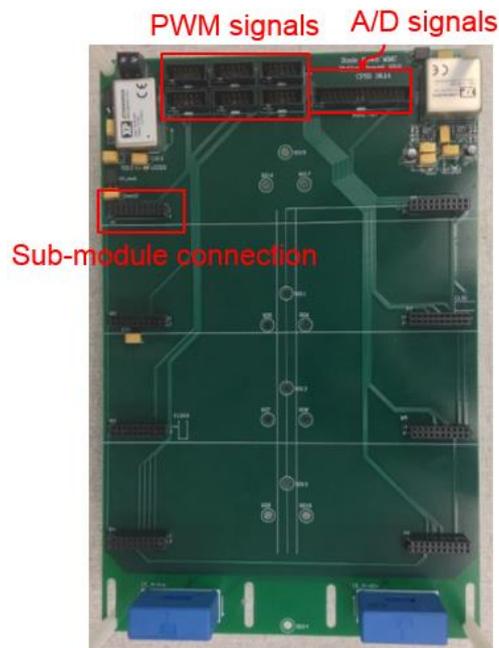


Fig.4. 3 The interface board

The picture of module board is shown in Fig.4. 4.

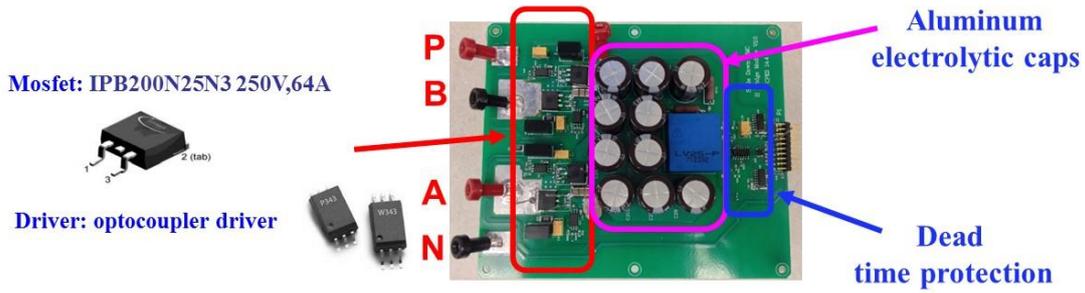


Fig.4. 4 The picture of module board

4.2 Control Loops

The control loops of the hardware are more complicated since the capacitor balance control must be considered. The completed control loops are shown in Fig.4. 5. The output current loop and the circulating current loop have been introduced in Fig. 3. 1, Chapter 3. Besides the current loops, Fig.4. 5 also includes the capacitor voltage balance control [12].

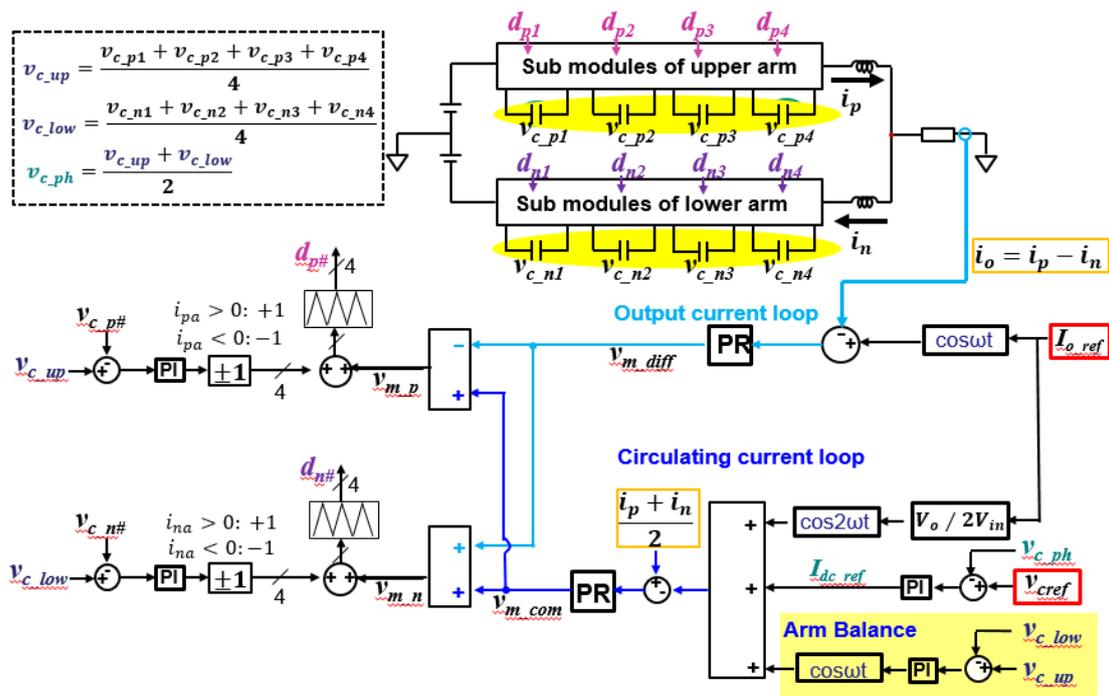


Fig.4. 5 The control loops

There are three different frequency components that refer to circulating current. The first component is the injected second-order circulating current. The second component is the DC current reference for controlling the capacitor voltage and the third component is at the line frequency, for the balance control between the upper arm and the lower arm. To explain the arm balance control, the arm currents and the arm voltages are assumed to be:

$$\begin{cases} i_p = I_{dc} + I_h \cos 2\omega t + \frac{I_o}{2} \cos \omega t \\ i_n = I_{dc} + I_h \cos 2\omega t - \frac{I_o}{2} \cos \omega t \end{cases} \quad (4.1)$$

$$\begin{cases} v_p = \frac{V_{dc}}{2} - V_o \cos \omega t \\ v_n = \frac{V_{dc}}{2} + V_o \cos \omega t \end{cases} \quad (4.2)$$

In this case the circulating current is:

$$i_{cir} = \frac{i_p + i_n}{2} = I_{dc} + I_h \cos 2\omega t \quad (4.3)$$

The upper arm power and lower arm power can be expressed as:

$$\begin{cases} p_p = v_p i_p = \frac{1}{2} V_{dc} I_{dc} - \frac{1}{4} V_o I_o + p_p(\omega t) + p_p(2\omega t) + p_p(3\omega t) \\ p_n = v_n i_n = \frac{1}{2} V_{dc} I_{dc} - \frac{1}{4} V_o I_o + p_n(\omega t) + p_n(2\omega t) + p_n(3\omega t) \end{cases} \quad (4.4)$$

This energy balance is only considering the low frequency component, so only the DC component of the arm power is measured here. If the summation of the capacitor voltages in the upper arm is larger than the lower arm, it means that the DC power of the upper arm should be decreased while the DC power of the lower arm should be increased. The DC power for each arm should be changed to be:

$$\begin{cases} p_p(DC) = \frac{1}{2} V_{dc} I_{dc} - \frac{1}{4} V_o (I_o + \Delta I) \\ p_n(DC) = \frac{1}{2} V_{dc} I_{dc} - \frac{1}{4} V_o (I_o - \Delta I) \end{cases} \quad (4.5)$$

The arm currents should be changed to:

$$\begin{cases} i_p = I_{dc} + I_h \cos 2\omega t + \left(\frac{I_o}{2} + \Delta I\right) \cos \omega t \\ i_n = I_{dc} + I_h \cos 2\omega t - \left(\frac{I_o}{2} - \Delta I\right) \cos \omega t \end{cases} \quad (4.6)$$

The circulating current should be changed to:

$$i_{cir} = I_{dc} + I_h \cos 2\omega t + \Delta I \cos \omega t \quad (4.7)$$

As seen in equation (4.7), a small fundamental component is required in the circulating current when the upper arm and the lower arm are not balanced.

Another balance control is the module balance control. Each module's capacitor voltage is compared with the average voltage of all capacitors in this arm. If one module's capacitor voltage is smaller than the average voltage, this module should be charged more energy. So, if the direction of the arm current is flowing into the module, the voltage command of this module should be a bit larger, or vice versa. Finally, each module will get its own voltage command. The voltage command will be compared with a phase shifted carrier wave to generate the driving signal.

4.3 Software of Scaled Down MMC

The master DSP4 has a peripheral switch to turn on or shut down the system. The master DSP4 and the phase DSP1, DSP2 and DSP3 are connected with I/O pins, as shown in Fig.4. 6. The master DSP sends the phase signals to the phase DSP through the I/O connection. Each phase signal has a $2/3 \pi$ phase shift. The phase DSP generates the output current reference based on its phase signal. The phase signal is shown in Fig.4. 7.

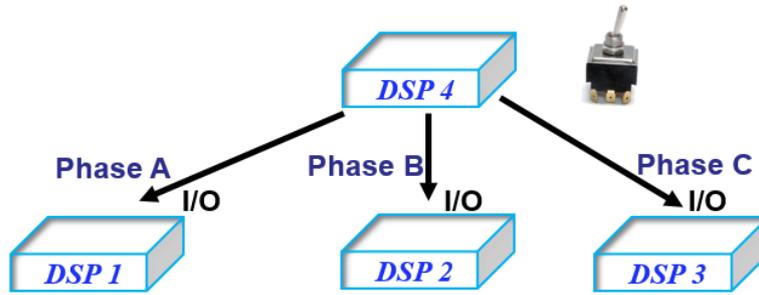


Fig.4. 6 The structure of connection between master DSP and phase DSP

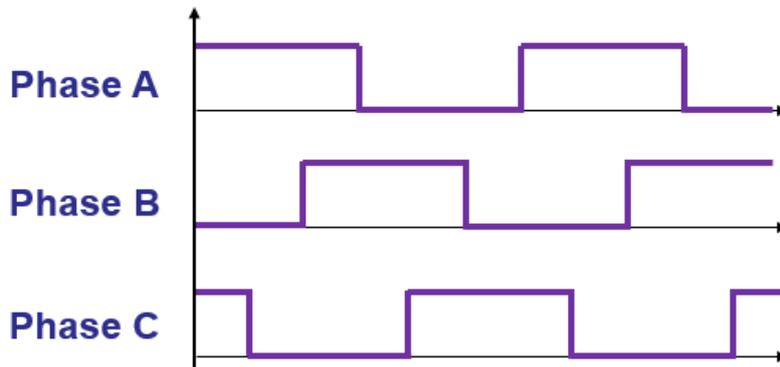


Fig.4. 7 Phase signals to three phase DSP

Each phase DSP is working as a controller of a single phase MMC, just with different current references, as shown in Fig.4. 8.

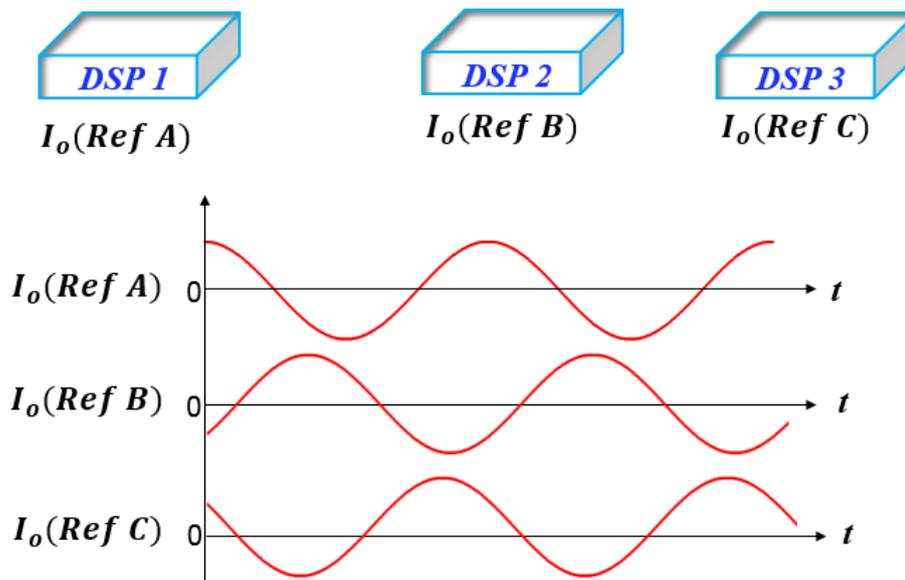


Fig.4. 8 Current references for each phase DSP

Fig.4. 9 shows the digital board. The CPLD is on the bottom side and most control programs are operated in the DSP.

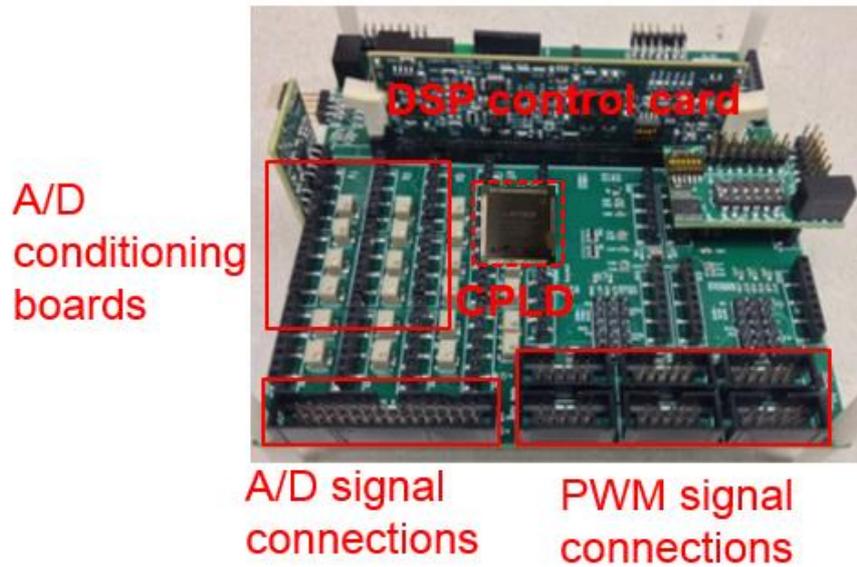


Fig.4. 9 Digital control board

The program flow chart is shown in Fig.4. 10. The CPLD is also responsible for the hardware protection. The control loops have been illustrated in Fig.4. 5. The following part will explain the process of the soft start.

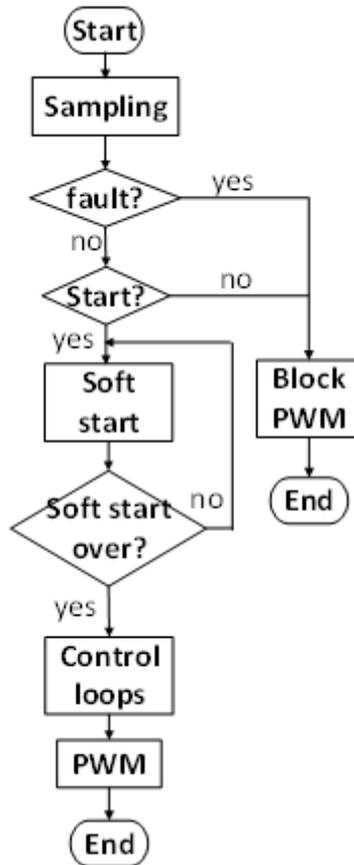


Fig.4. 10 program flow chart

The soft start program starts at the moment when the DC source has already been connected to the DC bus. The converter is in the idle state, as shown in Fig.4. 11. At this time all devices are blocked, so the capacitor voltage is:

$$v_{cp1} = \frac{V_{dc}}{8} \quad (4.8)$$

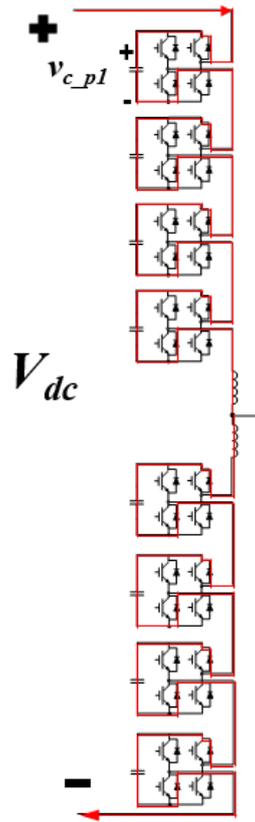


Fig.4. 11 idle state of MMC

However, in the steady state the capacitor voltage is $V_{dc}/4$. The soft start program is responsible for increasing the capacitor voltage slowly from the idle state ($V_{dc}/8$) to the steady state ($V_{dc}/4$). During the period of soft start, both the upper arm and the lower arm have the same voltage command, which will decrease from 1 to 0.5 on a programmed slope, to increase the capacitor voltage slowly. This process is shown in the Fig.4. 12.

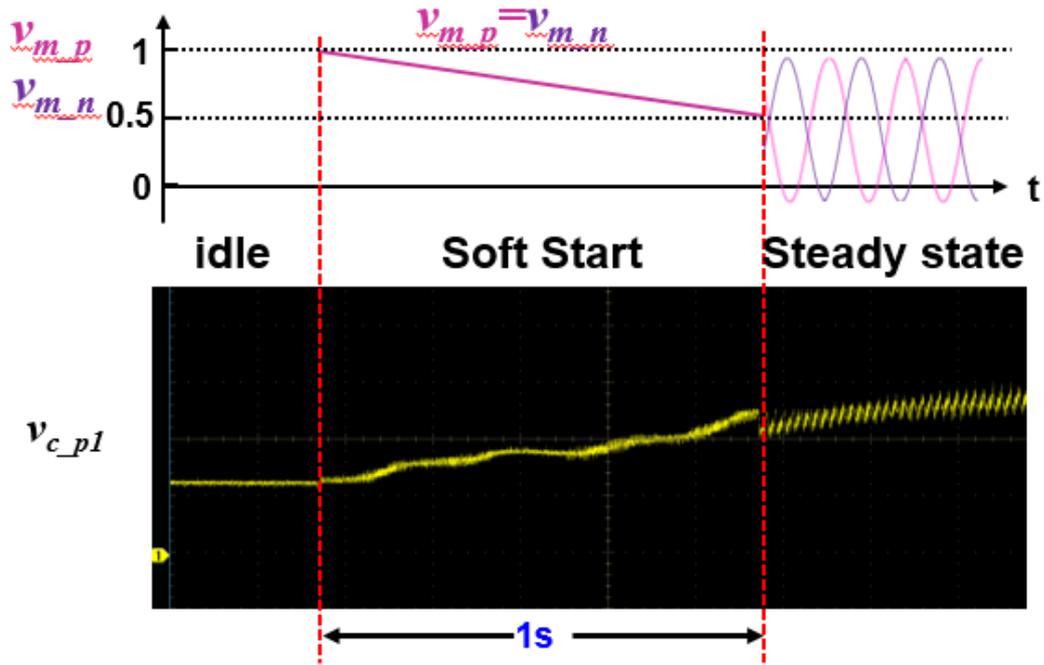


Fig.4. 12 The period of soft start

4.4 Experiment Results

The experiments were conducted to verify the proposed control concept. Fig.4. 13 shows the output current of three phase MMC hardware.

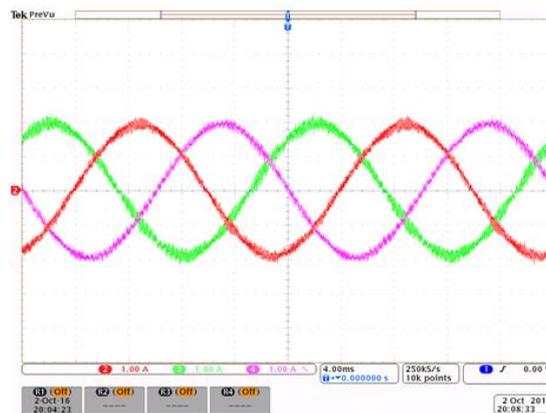


Fig.4. 13 Output current of three phase MMC hardware

The waveforms of the experiments of example 2 are shown in Fig.4. 14. The voltage gain is: $M = 0.9$ and the arm current is: $i_p = \frac{I_o}{4} M + \frac{I_o}{2} \cos\omega t$. Fig.4. 15 gives the state planes from the experiments of example 2.

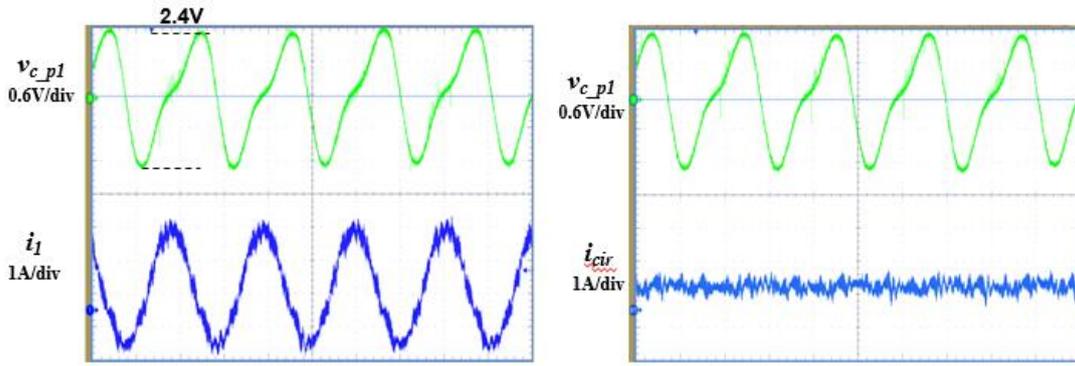


Fig.4. 14 The experimental waveforms of example 2

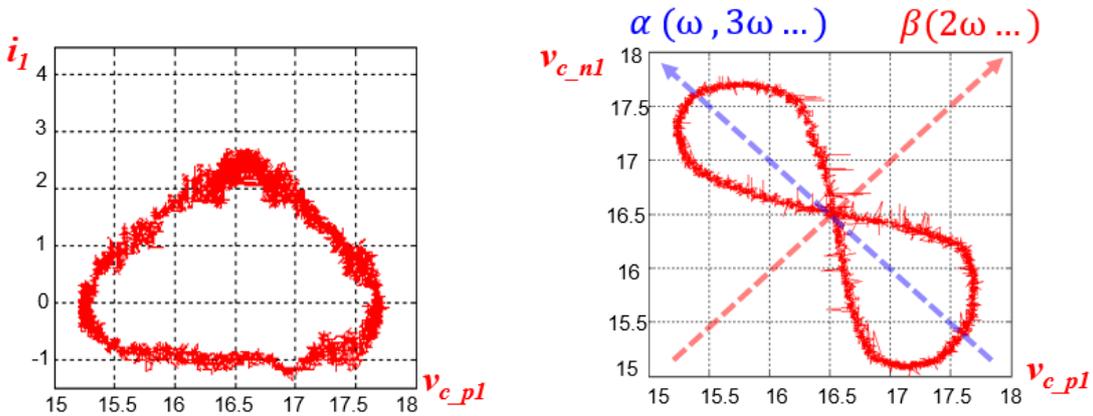


Fig.4. 15 The experimental state planes of example 2

The waveforms of the experiments of example 3 are shown in Fig.4. 16. The voltage gain is $M = 0.9$ and the arm current is: $i_p = \frac{I_o}{4} M + \frac{I_o}{4} M \cos 2\omega t + \frac{I_o}{2} \cos \omega t$. Fig.4. 17 gives the state planes from the experiments of example 3.

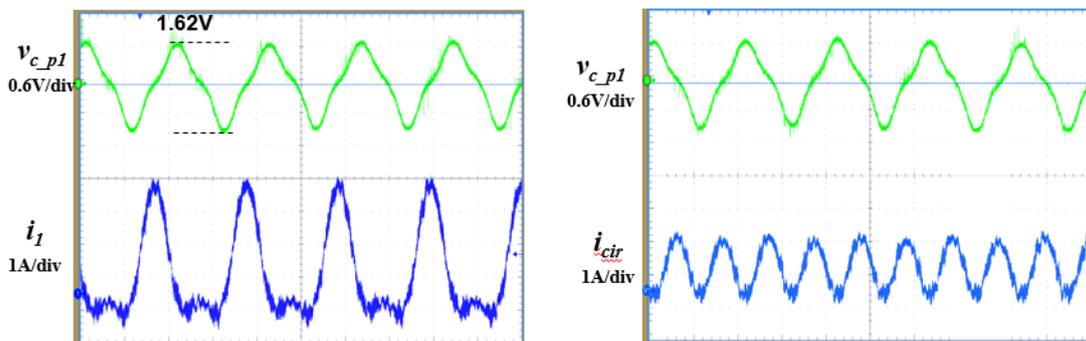


Fig.4. 16 The experimental waveforms of example 3

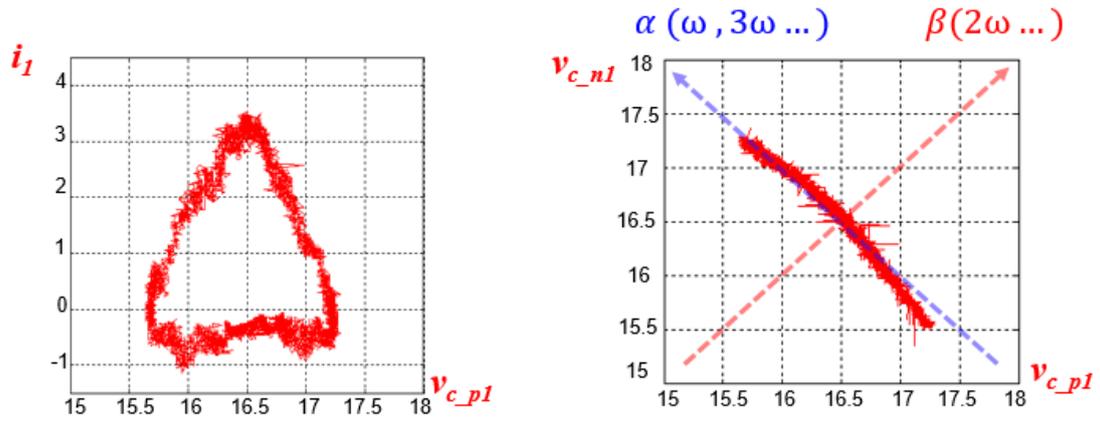


Fig.4. 17 The experimental state planes of example 3

The waveforms of the experiments of example 4 are shown Fig.4. 18. The voltage gain is: $M = 1.4$ and the arm current is: $i_p = \frac{I_o}{4} M + \frac{I_o}{2} \cos\omega t$. Fig.4. 19 gives the state planes from the experiments of example 4.

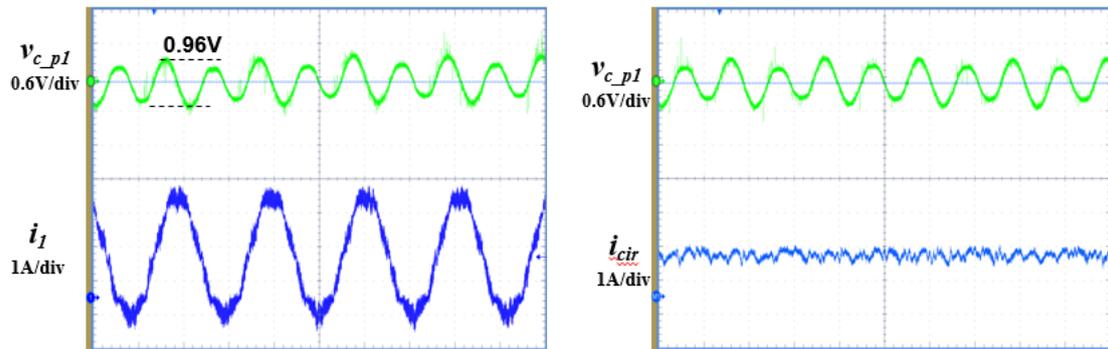


Fig.4. 18 The experimental waveforms of example 4

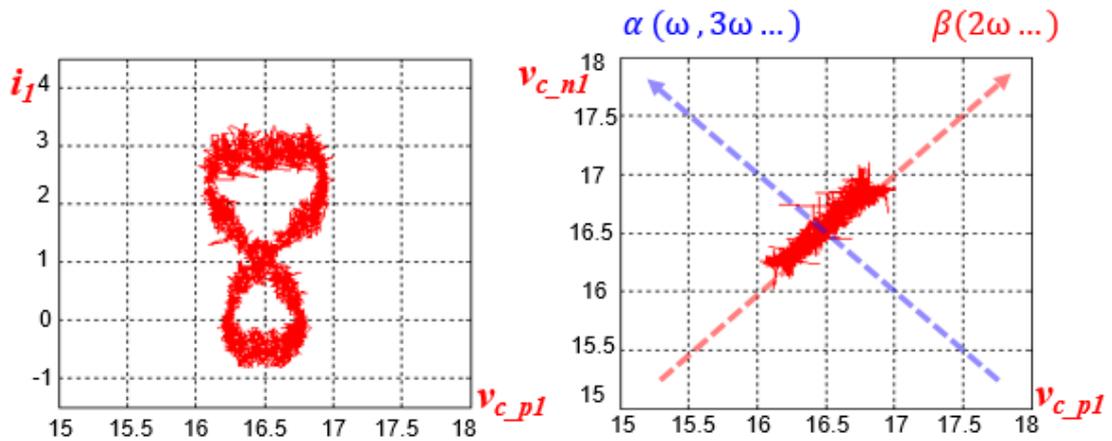


Fig.4. 19 The experimental state planes of example 4

The waveforms of the experiments of the proposed control with the full bridge MMC are shown Fig.4. 20. The voltage gain is $M = 1.15$ and the arm current is $i_p = \frac{I_o}{4} M + \frac{I_o}{4} M \cos 2\omega t + \frac{I_o}{2} \cos \omega t$. Fig.4. 21 gives the state planes from the experiments of the proposed control.

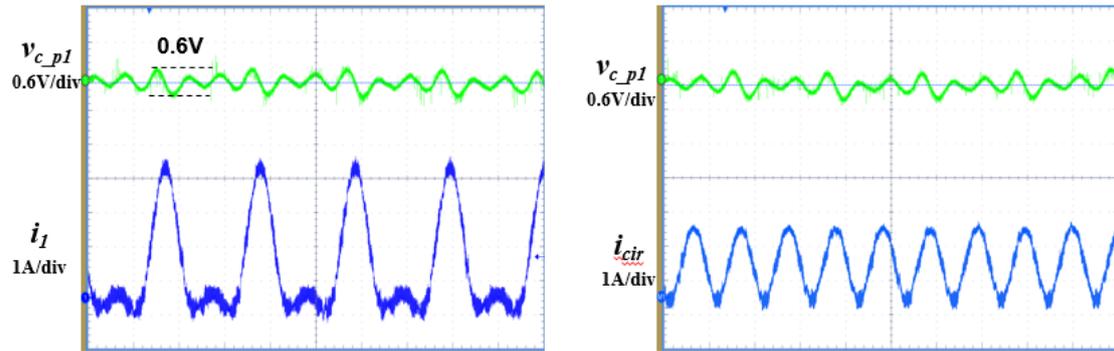


Fig.4. 20 The experimental waveforms of the proposed control

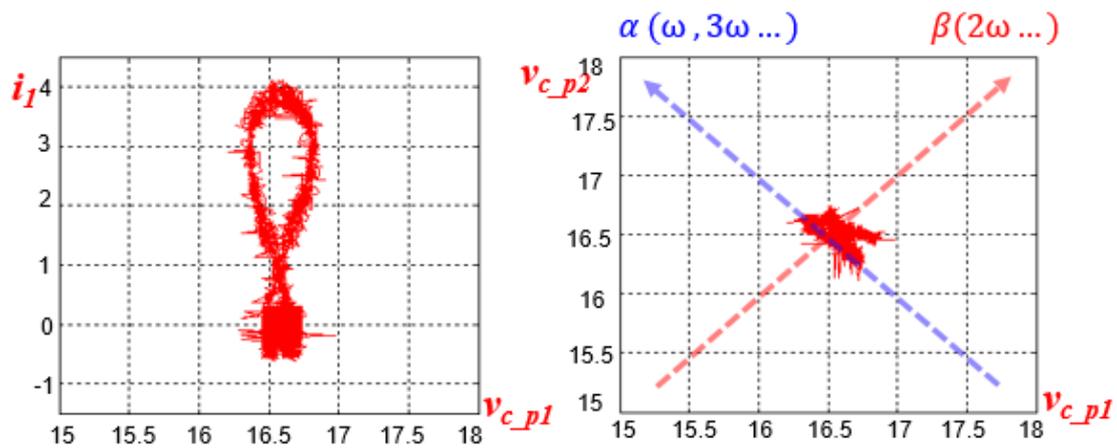


Fig.4. 21 The experimental state planes of the proposed control

The hybrid MMC experiments are also conducted. The voltage gain is: $M = 1.05$ and the arm current is: $i_p = \frac{I_o}{4} M + \frac{I_o}{4} M \cos 2\omega t + \frac{I_o}{2} \cos \omega t$. Two modules in one arm are working as half bridge modules, while the other two modules are working as full bridge modules. A third-order voltage command is injected in both the half bridge modules and the full bridge modules. The injection voltage is: $y = \frac{1}{6} \frac{V_o}{4} \cos 3\omega t$.

The output current waveform of the hybrid MMC under the third-order voltage injection is shown in Fig.4. 22. It shows that this injection does not influence the output current.

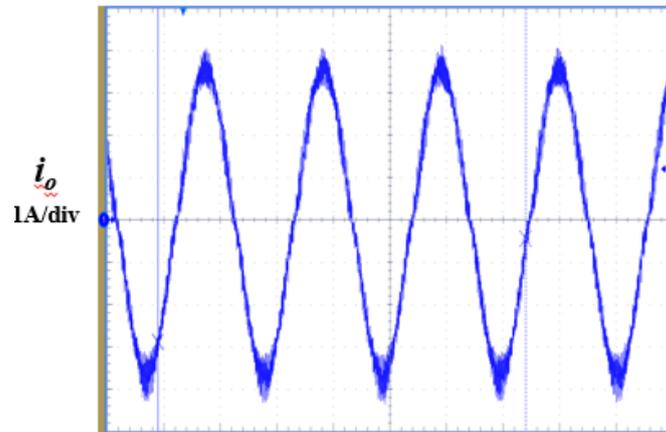


Fig.4. 22 The output current in hybrid MMC

The upper arm current and the circulating current are shown in Fig.4. 23. A second-order current is injected in the circulating current.

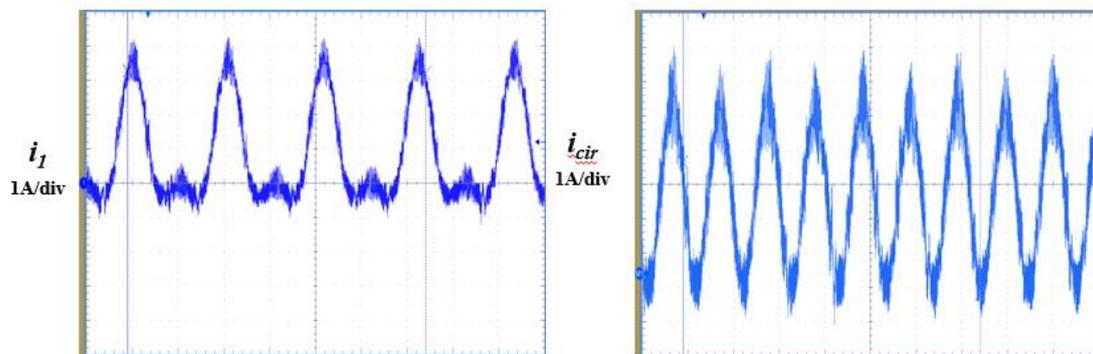


Fig.4. 23 The arm current and circulating current in Hybrid MMC

The output voltage of the output voltage of a half bridge module, v_{m_h} , and a full bridge module, v_{m_f} , are shown in Fig.4. 24. The half bridge module outputs only positive voltage, while the full bridge module outputs both positive and negative voltage.

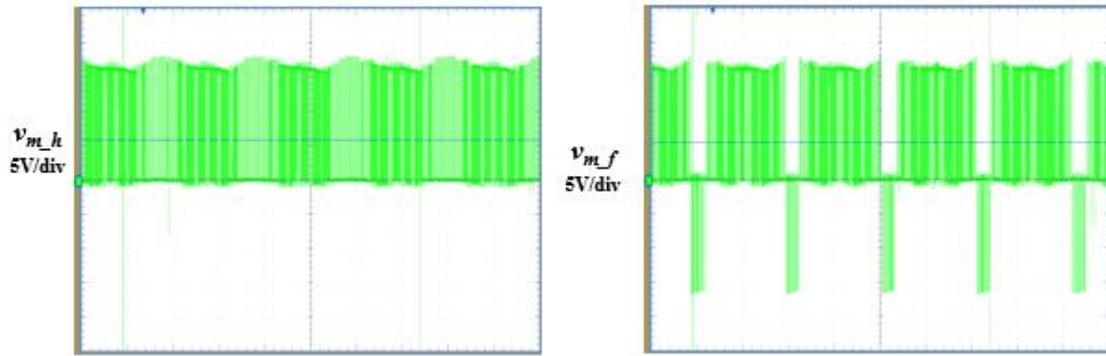


Fig.4. 24 The output voltages of a half bridge module and a full bridge module

The capacitor voltage of a full bridge module, v_{c_f} , and the capacitor voltage of a half bridge module, v_{c_h} , are shown in Fig.4. 24.

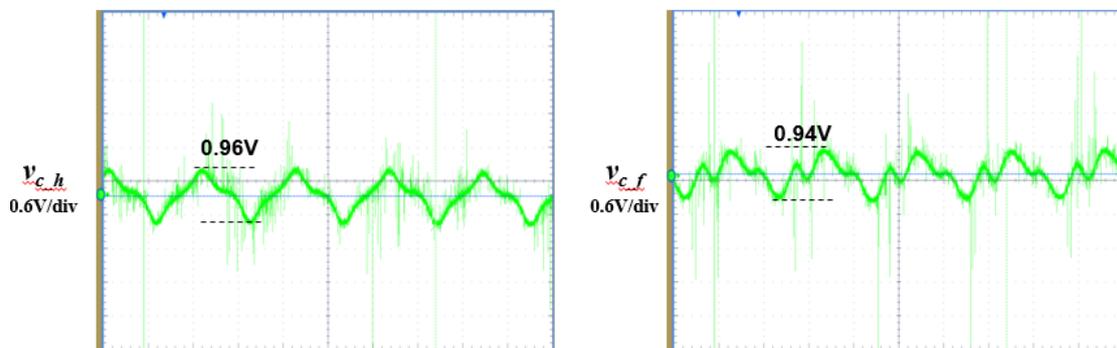


Fig.4. 25 The capacitor voltages of a full bridge module and a half bridge module

With Hsieh's control, the hybrid MMC can enjoy a lower capacitor voltage ripple than the half bridge MMC. In the experiments, the capacitor voltage ripple (0.96V) in the hybrid MMC is at the middle position between the half bridge MMC (1.62V) and the full bridge MMC (0.6V).

Chapter 5 Conclusion and Future Work

5.1 Summary and Conclusion

State-trajectory technique together with power flow analysis are employed to analyze the MMC system and the proposed method provides visual illustrations of the complex energy storage and transfer concept and means to reduce the circulating energy.

Furthermore, the analytical approach facilitates the development of a new control strategy, leading to a significant reduction of the bulky capacitor bank in each module of the MMC systems. This is achieved by the ideal of injecting a circulating current in conjunction with voltage gain control. With the proposed control strategy, the circulating energy associated with both the fundamental and second-order harmonic of the line frequency are eliminated for the first time. Consequently, the capacitor banks are greatly reduced and are only required to store the circulating energy associated with the third-order harmonic.

The proposed control strategy can only be realized in the full bridge module. It is demonstrated that a 61% voltage ripple reduction is achieved when compared to half bridge modules of the best practice and a 36% reduction is achieved when compared to full bridge modules with the previous control method. Although the full bridge MMC increases the loss by 85% compared to half bridge MMC, the short circuit protect can be realized by full bridge MMC.

The proposed method can be extended to the hybrid MMC. In addition to the reduction of capacitor banks, it also offers short circuit protection. In this special control, a third-order harmonic voltage is injected together with gain control. The capacitors can be reduced by 50% compared with half bridge MMC, but the loss is increased by 45%.

5.2 Future Work

The analysis in this thesis ignores the effect of the inductors. The proposed method requires a negative output voltage of the module. It would be interesting to explore other topologies, which can generate negative voltage with reduced loss. There is no accurate small signal model of MMC yet. Currently, the compensators are tuned to meet the requirement of stability and accuracy. An accurate small signal model would be helpful to instruct engineers in designing the compensators.

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