

An Improved Controller for the Rhino Robot Arm/

by

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(ABSTRACT)

content

The study of robotics cannot be satisfactorily pursued without access to working robots. The inexpensive Rhino robot arm is one that academic institutions can easily obtain for educational purposes. This thesis presents a new controller that replaces the original Rhino controller, which in many ways was not suited, or was too limited, for experimentation.

A comparison of the old and new controllers is given, but the primary purpose of this thesis is to provide complete details of the new controller, and its use.

The conclusion discusses the performance of the new controller and areas of experimentation to which it might be applied.

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CHAPTER 1. INTRODUCTION

ROBOTS AS RESEARCH TOOLS

The study of robotics is not complete without some practical experience in making robots move. Indeed, there is a wealth of research problems involving precisely that task in such areas as trajectory planning, collision avoidance, and sensory feedback. Powerful and flexible tools are necessary to enhance the research possibilities.

Few robots are designed specifically to be research tools. In the case of an industrial robot, information that would greatly aid in using it for experimentation is often proprietary, unavailable even to academic institutions. Thus, a robot in the research lab is often just a large 'black box' designed to move through a series of widely separated points specified by the user. The path that is followed from point to point is determined by computations over which the user has no control.

However, a researcher may want the robot to follow a path determined by computations being made on an entirely separate machine, but may be unable to circumvent the control circuitry

and software of the robot in his laboratory.

The Rhino¹ robot thus finds its place in the laboratory, since it was designed specifically for research. The details of its circuitry and software are provided by the manufacturer. But, as a research tool, it has some severe limitations.

COMPARISON OF THE OLD AND NEW CONTROLLERS

There are several problems with the design of the original controller for the Rhino robot. Because the controller implements what is generally called 'bang-bang' control, the robot cannot make velocity-controlled moves. Under that type of control, every move is made at top speed, often resulting in large, undesirable oscillation of the end effector (gripper). This limited capacity is not surprising, with only one microprocessor controlling all six motors.

The primary reason for designing a new controller was to implement velocity control during execution of move commands. Among the benefits expected under velocity control was the reduction

¹ The name Rhino is a registered trademark of Rhino Robots, Inc., 308 S. State, Champaign, IL, 61820.

of unwanted oscillations to a tolerable level. The major obstacle to achieving velocity control was the lack of tachometers on the motors of the robot. Velocity control had to be implemented using only position feedback.

The position feedback from each motor consists of two bits from a quadrature-encoded shaft encoder disk. The disk, itself, compounds the problem of obtaining velocity control from position feedback because it has very poor angular resolution (15 to 45 degrees).

The velocity control problem was solved, however, to the extent that the new controller can maintain a specified velocity to a reasonable degree of accuracy (about 8% in most cases) and can execute moves with no overshoot and a tolerably small amount of oscillation of the end effector.

One measure of the quality of a robot is the repeatability of a position (that is, how close can the robot come to assuming a specified previous position). Under the new controller, repeatability (typically on the order of 1 millimeter) has been improved by a factor of four. That is because the original controller senses angular error with only one-fourth the resolution of the new controller.

A further significant limitation of the original controller is the small angular distance that can be specified by a single move command. It is restricted to a signed one-byte number (± 127), corresponding to about ten degrees of motion at most joints. Thus, to implement a long move it is necessary to break the move up into several short, consecutive moves. That problem is compounded by the lack of a buffer for a follow-up move, causing the motors to pause slightly at the end of each short move while the follow-up move is communicated.

That communication, itself, is somewhat tedious since commands and data are passed using ASCII coding. For example, passing a number such as '-120' requires four bytes of data, one for each character.

In recognition of those limitations, the new controller accepts signed 16-bit moves (± 32767), as two 8-bit (serial) data bytes, allowing even very large moves (± 2500 degrees) to be communicated by just two bytes of data. Furthermore, it has the capability to receive data for a following move during current move execution, and the transition from one move to the next is smooth.

The new controller has an extensive communication language. It

allows the user (under dynamic computer control) to easily monitor and alter the internal states and control parameters of the system, thus providing additional research capability. That contrasts with the old controller, which has only four marginally useful (and somewhat clumsy) commands.

The improvements in communication and control capability were not cheap. Large amounts of processing and computational power are used. The final design is a three-level communications network consisting of a host computer (highest level), a communications facilitator (middle level computer), and up to seven computers that implement control on individual motors (lowest level).

The communications network problem was considerably reduced because communications originating at the lowest level can be serviced by polling, rather than by interrupt. That is due to the high speed at which the middle level computer (Intel 8751) is capable of polling and the relatively low priority of communications originating at the lowest level.

The solution of the velocity control problem is somewhat ad hoc. However, the control algorithm has been greatly generalized, allowing the user to specify twelve parameters for each

motor, and to change them at any time, even during the execution of move commands.

The software and hardware that were developed to implement the control are specified in detail in this document. However, theoretical details supporting the effectiveness of the control algorithm are not elaborated. The lack of theoretical details is mainly due to the lack of a well-developed and computationally tractable model for the system.

Sampled-data system modelling is generally simplified by making the initial assumption that the sample rate is constant. The poor resolution of the Rhino robot position encoders led to the use of an interrupt-driven control algorithm, where an interrupt is generated each time the position encoder output changes. Clearly, the faster a motor is turning, the faster is the rate of interrupt generation. Thus the simplifying assumption of a constant sample rate cannot be made for this system.

The theoretical implications of a variable-rate sampled-data system are not trivial. In fact, they could easily be the basis of another thesis. For that reason it was impossible, under the various constraints (particularly, the time constraint), to give that topic a just treatment here.

This document primarily explains how the new controller works and presents the communication format for running it from a host computer. During its development, the controller was run from a VAX/VMS 11/780, so all references to communication assume the VAX as host. However, any computer capable of unformatted 8-bit communication over an RS/232 interface, at either 4800 or 9600 baud, can be used as the host.

POSSIBLE IMPROVEMENTS ON THE NEW CONTROLLER

While the control exercised through the new controller is far better than what was available using the original controller, it is also far from perfect. That fact suggests that work could be done on the new system to improve it further.

In particular, the microprocessor used at the lowest level for motor control is very limited in computational power and speed, and in program length. If a more sophisticated microprocessor were used, then the velocity measurement could be made with greater resolution. Similarly, the pulsewidth power to the motor could be computed with greater resolution. Those two factors together would result in tighter control of the velocity.

It would be difficult to use the existing program to control motors having much finer or much coarser angular position resolution. In the latter case, sparseness of feedback would tend to destabilize the control at low speeds. In the former case, the long computation time would tend to destabilize the control at high speeds (although that could be remedied by using a faster microprocessor or fewer of the samples).

The program running at the lowest level was written in modules, primarily to facilitate debugging the control algorithm. It would therefore be relatively easy to make changes in, or even completely rewrite the control algorithm, not having to alter the communication and bookkeeping routines.

The program running at the middle level is primarily a collection of routines that handle special cases. It would be a simple matter to expand the communication codes if the need arose; for example, the seventh lower-level computer (the Rhino has only six motors), could have special functions.

The middle-level computer could also be incorporated into the control scheme. For example, it could provide feedback paths among the low-level computers. That suggests many interesting research topics in the area of large-scale systems.

CHAPTER 2. SYSTEM OVERVIEW OF THE CONTROLLER

COMMUNICATIONS

The system can be considered as a distributed network of computers, where the host computer (hereafter, assumed to be the VAX) communicates, over an RS/232 serial link, with the Intel 8751 microprocessor; and the 8751 communicates with up to seven Intel 8748 microprocessors, each of which controls one motor of the Rhino robot. A block diagram of the entire system is given in Figure 1 on page 20.

An overview of the system must include the program running on the VAX, which communicates various commands to the Rhino robot. For example, the program might be designed to compute the sequence of move commands that will cause the Rhino robot to move along some desired trajectory. Whatever its purpose, the program must use the communication protocol and data format expected by the Intel 8751, the details of which are given in "Appendix A. Protocol and Data Format in VAX/8751 Communications" on page 26. The VAX program must also respond to the condition of a motor stalling; and it must wait to send move data until the 8751 indicates that the Rhino is ready for

another move. A sample program for the VAX is given in "Appendix S. Sample VAX Program (PASCAL)" on page 118.

The Intel 8751 can be considered as a simple communication link between the VAX and the six Intel 8748's. However, it also serves:

- to format certain data passed between the VAX and the 8748's,
- to react swiftly to emergency conditions reported by the 8748's,
- to concatenate certain communications from the various 8748's before passing them on to the VAX,
- to report system states (such as positions and velocities of the motors) when requested by the VAX.
- to read data ('peek') from any system random access memory (RAM), and write data ('poke') to locations in individual 8748 internal RAM.

Each Intel 8748 serves primarily to control the position and velocity of one motor on the Rhino robot and to sense if that motor is stalled. Its secondary, but no less important, function is to communicate with the Intel 8751. The communication protocol and data formatting are discussed in "Appendix C. Pro-

tocol and Data Format in 8751/8748 Communications" on page 39.

Immediate commands between the 8751 and 8748's, also called codes (as distinct from data), are communicated through two 'mailboxes.' The 8748 writes commands to the 8751 through one mailbox and reads commands from the 8751 through the other.

Each mailbox is equipped with a flag that is set when a command is written by one microprocessor, and cleared when it is read by the other. Details of the mailboxes are given in "Appendix D. The Mailboxes" on page 44.

Data are passed through an external random access memory to which both the 8751 and the 8748 have read- and write-privilege (called the shared RAM). Details of the shared RAM are given in "Appendix E. The Shared Random Access Memory" on page 52.

While each 8748 must communicate with only one pair of mailboxes, and gain access to only one shared RAM, the 8751 has up to seven pairs of mailboxes and seven shared RAM's to service. It was therefore necessary to devise a straightforward addressing scheme that would:

- access the read-mailbox flags (to test for the presence of

commands from the various 8748's),

- access the read-mailboxes individually (to read in a command from an individual 8748),
- access the write-mailbox flags (to check that the old command has been read before writing the new one),
- access the write-mailboxes, either individually or globally,
- access an individual shared RAM, and
- access the shared-RAM-lockout flags.

The scheme used for mailbox addressing is detailed in "Appendix D. The Mailboxes" on page 44; the scheme for shared RAM addressing is detailed in "Appendix E. The Shared Random Access Memory" on page 52.

BOOKKEEPING TASKS IN THE INTEL 8751

The 8751 must keep track of several significant conditions in each 8748. At all times it must monitor:

- which 8748s are 'in service' (that is, expected to function);
- which 8748s' motors (if any) are stalled;
- which 8748s have lost power temporarily (causing an ini-

tializing 'hardware reset' to occur);

- which 8748s are ready for another move command.

The 'in-service' status of a particular 8748 determines if the 8751 will attempt to communicate with it.

In the cases of hardware reset and motor stall, the 8751 notifies the VAX immediately if the condition is reported from any 8748. However, the 8751 waits for all in-service 8748s to report being ready for another move before notifying the VAX.

Those bookkeeping details are given in "Appendix L. Bookkeeping Tasks in the Intel 8751" on page 86.

BOOKKEEPING TASKS IN THE 8748

Keeping Track of Velocity

It is evident that the direction as well as the speed of the motion must be determined to know the velocity. Not so evident, perhaps, is that it is also important to know the recent history of the velocity in order to perform the control task properly.

Of particular interest are the cases when

- motion is just beginning
- the direction of motion reverses
- the velocity is approaching the velocity set point
- the velocity is diverging from the velocity set point

Each of those cases requires special handling, so one of the bookkeeping tasks is to determine when they occur. The details of that task are given in "Appendix K. Velocity Bookkeeping in the 8748" on page 79.

Keeping Track of Position

There are several locations in 8748 RAM and shared RAM that keep track of position. Each of those locations serves a specific function in the overall task of position control. After each motion interrupt, the various position data must be updated. The details of that task are somewhat complicated; the interested reader is directed to "Appendix J. Position Bookkeeping in the 8748" on page 73.

CONTROL CONSIDERATIONS

Stability and Variable-Rate Sampling

In a system where position data are used to generate velocity feedback, it is a significant event when the position remains constant if it should be changing. Similarly, it is a significant event when the position changes if it should be constant. Therefore, it is important to report either case to the controller.

This argues for interrupt-driven control, where an interrupt is generated

- if the position has not changed after some standard period of time, T , or
- when a change in position occurs,

The controller must distinguish the cause of the interrupt in order to take the proper action. (The details of the interrupt generation are presented in "Appendix H. 8748 Interrupt Generation" on page 67.)

The result of this scheme is variable-rate sampling. When the

motor is stopped, samples occur at a fixed rate, $1/T$. When the motor is moving, however, samples occur whenever a change of position is detected, which depends on the angular velocity and on the resolution of the shaft encoder disk that provides the position feedback (details of the shaft encoder disk and the position feedback are given in "Appendix G. Shaft Position Encoding" on page 61).

So there is a threshold of velocity detection established by picking the value of T (seconds). That is, velocities resulting in detection of fewer than $1/T$ position changes per second cannot be discriminated as uninterrupted motion.

That may not be a problem when the encoder disk is densely encoded, but those on the Rhino motors have a resolution of between 15 and 45 degrees of a motor shaft revolution, depending on the particular motor. So picking, for example, $T = 1/16$ second, the minimum velocity that can be discriminated is between 40 and 120 r/min.

Thus, it is not surprising that using this type of feedback for velocity control can result in unstable performance at set points below about 200 r/min. On the other hand, one might expect that choosing larger values of T would result in sparse

feedback, which can lead to sluggish response and to instability. That result was obtained experimentally.

During motor motion, the rate of interrupt generation is clearly dependent on the velocity, so there is no fixed sample rate. That fact makes the system difficult to model, since the simplifying assumption of a fixed sample rate cannot be made.

One way to model the system is to linearize it about some fixed velocity equilibrium points (system poles thus vary with the velocities). Representing each motor by a one-pole model, each pole can be imagined to vary (dependent on the associated velocity) in the z-plane along the real line from a point near the origin (good stability) to a point near the unit circle (marginal stability). Experimental results indicate tightest velocity control occurs at speeds above 20% of full speed, with actual instability occurring under certain types of loading at speeds below 15% of full speed. This is discussed in more detail in the section titled "Performance" on page 21.

Velocity Determination from Position Feedback

Since velocity is the derivative of position, obtaining velocity data from position feedback gives rise to derivative control. The simplest method, given that Intel 8748 microprocessors were to be used, was to measure the time period, t , between motion interrupts and to determine the reciprocal, $1/t$, which is the instantaneous velocity in detected position changes per second. The angular velocity is directly proportional to that result, according to the angular resolution of the encoder disk.

That scheme is not without faults. It implicitly assumes perfect spacing and detection of the transition points on the shaft encoder disk. That is, of course, not possible; the result is measurement error, which can be considered as noise due to the differentiation.

Another problem is the reciprocal operation, itself. In order to obtain good timing resolution over the full range of motor speeds it is necessary to use a two-byte clock. The Intel 8748 has neither a divide nor a multiply command, so computing a two-byte reciprocal would be an extremely time-consuming operation. For that reason, a method of taking the reciprocal was

devised using a clock frequency that is a power of 2 and a reciprocal look-up table. The method is described in detail in "Appendix K. Velocity Bookkeeping in the 8748" on page 79.

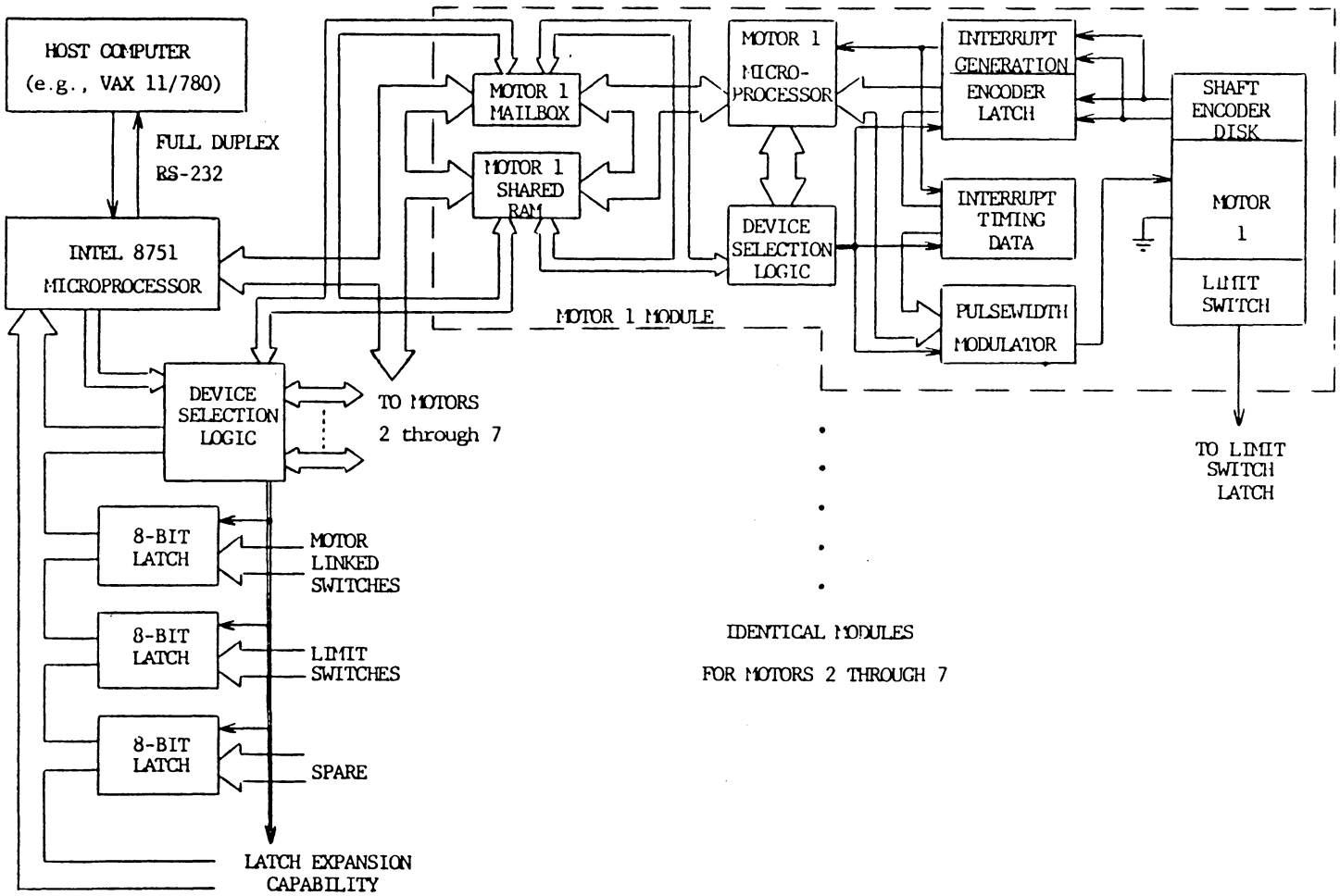
Velocity Control by Pulsewidth Modulation

The 8748 functions as a velocity controller, and can be viewed as closing a feedback loop where input is a velocity set point and output is the motor velocity. The flexibility of software allows easy definition of special situations and corresponding linear or non-linear responses.

The system state is broken down into various special cases for which different control algorithms are used, as discussed in "Appendix M. Control by Non-Linear Feedback" on page 90.

In any case, the result of the algorithm is a new value for the level of power that is sent to the DC motor. Power to the motor is varied by a pulsewidth modulator (see "Appendix O. The Pulsewidth Modulator" on page 98). The pulsewidth (duty cycle) is directly proportional to a seven-bit number received from the 8748. The polarity of the voltage applied to the motor is determined by an associated sign bit.

Figure 1. System block diagram.



CHAPTER 3. CONCLUSION

PERFORMANCE

Maximum motor angular speed is about 240 holes per second. Since that is slightly less than an exact power of two, representation of the velocity in binary form is optimized. (The maximum angular speed corresponds to about 5000 r/min; see "Appendix G. Shaft Position Encoding" on page 61 for details of the angular measurement in holes per second.)

Velocity measurements were made on all the motors under various loading conditions, and over the full range of velocity set points. Differences in motor loading affect performance significantly. Such differences involve changing torque, changing friction, changing load, and centrifugal forces. ;p. Some of the motors see a relatively constant load. In that category are the gripper motor, the roll and pitch motors, and the 'waist' motor. The others (the 'shoulder' and 'elbow' motors) are subject to widely varying loading, especially during maneuvers which extend or retract the robot arm.

The best results, of course, were for the four motors whose

loads are not greatly affected by configuration. In that case, for set points above 10% of maximum speed, speed was stable, fluctuating up to 8% about the set point, and exhibiting good recovery from sudden load changes and step changes of the set point. At the end of a move, regardless of the speed, position overshoot is less than thirty degrees of one motor shaft revolution (about 0.05 degrees at the joint), and velocity ramps down so smoothly that very little oscillation occurs.

For set points below 10% of maximum speed, stability was marginal, and was the worst at the slowest set point possible, which is 2% of maximum. At speeds below about 5% of maximum, many loading conditions caused instability, which manifests as starting and stopping the motor in brief bursts of motion.

The worst case was the shoulder motor at full extension under rated loading (four pounds) where instability occurred at set points below 15% of maximum when the load was being lowered, and the same move was only marginally stable at set points between 15% and 25% of maximum (marginally stable meaning the velocity fluctuates around 50% of the set point value, about the set point).

The performance results mean that for all motors the minimum

specified speed for a move will have to be greater than 5% of maximum speed (and, for the shoulder and elbow motors, greater than 15% of maximum speed) to ensure smooth motion of the robot arm. While that is somewhat restrictive, it still provides a good range of speeds for experimentation.

AREAS OF EXPERIMENTATION

Every stage of the design was carried out with the main consideration of creating a tool for experimentation. The internal workings of the system were intended to be as accessible as possible to the user.

The control algorithms of the 8748 programs were written to allow the user to change almost every significant parameter. In particular, the following are specified by the user for each motor:

- the coefficients (zero to $63/16$ in increments of $1/16$) multiplying the velocity error, for each of four different speed ranges;
- magnitude limits (0 to 127) on the velocity error for each of four different speed ranges, allowing non-linearities in the algorithm;

- a hysteresis (0 to 63), or minimum non-zero value of the pulsewidth (another non-linearity);
- the minimum overshoot correction power, (0 to 127) specified for overshoot less than one hole, and for overshoot greater than one hole (the same values are used for undershoot correction).

All system RAM can be read by the user. Furthermore, the user can write to the 8748 internal RAM, which is the significant area in terms of control.

The system can be run with zero to seven motors operational. Since the Rhino robot has only six motors, there is a spare axis available. It could be used for another axis of motion, or for something else entirely, such as a sensory-data processing microcomputer.

There is capability for up to six additional 8-bit-latch inputs, directly addressable from the host computer, similar to the latches used for the motor-linked switches and the limit switches.

The foregoing capabilities were designed into the system to make the research possibilities as wide-ranging as possible.

For instance, the Rhino robot with this controller could certainly be used in motion studies of trajectory control or of dynamics under load. The addressing and input capabilities make its use with sensory-feedback devices feasible. Adaptive control could be studied using a program that makes changes in the various control parameters and set points based on velocity and/or position feedback.

The user could obtain other 8748 and 8751 microprocessors and rewrite some or all of the software, to test entirely different algorithms or to expand capabilities, and plug them into the existing hardware.

In short, the system is a functional experimental tool with far more capability than existed with the old controller.

APPENDIX A. PROTOCOL AND DATA FORMAT IN VAX/8751 COMMUNICATIONS

COMMUNICATING COMMAND CODES

All command codes have a common format which promotes quick code validation. The format is easily seen if the codes are written as hexadecimal (hex) numbers. In all cases, the upper and lower hex digits are identical. In other words, from each hex code, the hex number 11 (decimal 17) can be factored. A complete list of the codes which the VAX can send to the 8751 is given in Figure 2 on page 30.

The communication originating from VAX initiates a predictable sequence of events in the 8751. For some commands, the 8751 will request data to be transmitted. For others, the 8751 sends a simple response or prepares data for transmission to VAX. This is called the communication protocol for VAX-originated commands, and is tabulated in Figure 3 on page 31.

The 8751 has a set of command codes which it can send to VAX.

Some of them are sent only in response to VAX commands, but there are some which can originate from the 8751. The code format is the same as that described above for the VAX codes. A complete list of the codes which the 8751 can send to VAX is given in Figure 4 on page 32.

Communication originating from the 8751 must elicit certain expected responses from VAX, in the cases where a response is required. In most cases, no response is expected from VAX, so the program running on the VAX has a bit of latitude in that area. The communication protocol for 8751-originated command codes is tabulated in Figure 5 on page 33.

COMMUNICATING DATA

Data are serially communicated between VAX and the 8751 only after a 'send data' code has been transmitted and received successfully. Data for each command have a unique format, as enumerated here.

Data from VAX to the 8751:

1. The data for a move command are transmitted in two groups, each group containing data for seven motors.
 - a. The angular distance for each motor is formatted as a sixteen-bit number, high byte transmitted before low byte; motor seven data are transmitted first, motor 1 data last; the lower 15 bits are the (unsigned) magnitude of the move, in encoder holes; the highest, or sixteenth, bit is the direction of the move, where a zero indicates clockwise.
 - b. The velocity for each motor is a number from 0 to 127, and represents one-half of the velocity set point in holes per second, rounded up; motor seven data are transmitted first, motor one data last.
2. A motor number is sent for several of the commands; it is essential that it not exceed seven (that is, the upper five bits of the byte must be clear).
3. Coefficients are from 0 to 63.
4. Addresses for 8751 peek and shared RAM peek are from 0 to 255.
5. Addresses for the 8748 peek/poke are between 0 and 63; the eighth bit of the address byte is also used, indicating 'peek' if it is clear and 'poke' if it is set.

Data from the 8751 to VAX:

1. Format for data in response to 48PK or SHRPK: first, the command code that elicited the data; next, the Rhino Clock count, a sixteen bit positive number, high byte first; the address of the peek comes next; finally, the data read at that address from each motor, with motor seven data first, motor one data last.
2. Format for data in response to 51PK: first, the 8751 peek code; next, the Rhino Clock count, a sixteen bit positive number, high byte first; the address of the peek comes next; finally, the data read from that address (from internal 8751 RAM if the address is 0-127; from the latch that is enabled by the address if the address is 128-255).
3. Format for data in response to VRQ: first, the Rhino Clock count, a sixteen bit positive number, high byte first; followed by the velocity of each motor, a one-byte number in two's-complement, representing one-half the velocity; motor seven's velocity first, motor one's last.
4. Format for data in response to PRQ: first, the Rhino Clock count, a sixteen bit positive number, high byte first; followed by the position of each motor, a two-byte number in two's-complement form, high byte first, with motor seven data first and motor one data last.

COMMAND CODES FROM VAX 11/780 TO INTEL 8751		
CODE	mnemonic	COMMAND
0	NOP	No operation
17	ECI	Enable 'command-on-interrupt'
34	DCI	Disable 'command-on-interrupt'
51	48PK	'Peek' into 8748 internal RAM
	WR48	'Poke' into 8748 internal RAM
68	51PK	'Peek' into 8751 internal RAM
85	VRQ	Velocity data request
102	PRQ	Position data request
119	SNDVX	Send data to VAX (from 8751)
136	OVR	Send previous code over again
153	CRM	Clear remaining moves
170	MOV	Move
187	HLT	Halt
204	AGO	All motors Go
221	SHRPK	'Peek' into shared RAM
238	RAP	Reset absolute position
255	KFF	Coefficients

Figure 2. Command codes from VAX to 8751.

VAX ORIGINATED CODE	8751 RESPONSE	VAX RESPONSE	8751 RESPONSE	VAX RESPONSE	8751 RESPONSE
NOP (0)					
DCI (34)	DCI (34)				
CRM (153)	CRM (153)				
HLT (187)	HLT (187)				
AGO (204)	AGO (204)				
RAP (238)	RAP (238)				
OVR (136)	1 byte data	depends on data			
VRQ (85)	VDT (85)	SNDVX (119)	9 bytes data		
PRQ (102)	PDT (102)	SNDVX (119)	16 bytes data		
ECI (17)	SND51 (17)	1 byte data	RCVD (119)		
			INV (255)		
KFF (255)	SND51 (17)	15 bytes data	RCVD (119)		
51PK (68)	SND51 (17)	1 byte data	DAT (68)	SNDVX(119)	5 bytes data
SHRPK (221)	SND51 (17)	1 byte data	DAT (68)	SNDVX(119)	11 bytes data
48PK (51)	SND51 (17)	1 byte data (high bit clear)	DAT (68)	SNDVX(119)	11 bytes data
WR48 (51)	SND51 (17)	1 byte data (high bit set)	SND51 (17)	2 bytes data	RCVD (119)
MOV (170)	SND51 (17)	14 bytes data	SND51 (17)	7 bytes data	RCVD (119)

Figure 3. Communication protocol for VAX-originated codes to 8751.

COMMAND CODES FROM INTEL 8751 TO VAX 11/780		
CODE	mnemonic	COMMAND
0	NOP	No operation
17	SND51	Send data to 8751 (from VAX)
34	DCI	Disabled command-on-interrupt
51	RDYNXT	Ready for next move
68	DAT	'Peek' data ready to transmit
85	VDT	Velocity data ready to transmit
102	PDT	Position data ready to transmit
119	RCVD	Data received
136	OVR	Send previous data over again
153	CRM	Clear remaining moves
170	HDWRST	Hardware reset
187	HLT	Halted
204	AGO	All motors in 'go' state
221	MTRSTL	At least one motor is stalled
238	RAP	Reset absolute position
255	INV	Invalid data

Figure 4. Command codes from 8751 to VAX.

INTEL 8751 ORIGINATED CODE	VAX 11/780 RESPONSE	INTEL 8751 RESPONSE
NOP (0)		
RDYNXT (51)		
HDWRST (170)		
HLT (187)		
MIRSTL (221)		
OVR (136)	1 byte data	depends on data
VDT (85)	SNDVX (119)	9 bytes data
PDT (102)	SNDVX (119)	16 bytes data
DAT (68)	SNDVX (119)	either 5 or 11 bytes data

Figure 5. Communication protocol for 8751-originated codes to VAX.

APPENDIX B. 8751 SOFTWARE FOR VAX COMMUNICATION

SCHEME FOR VAX COMMUNICATIONS

All communication with the host computer occurs over RS/232 serial link. The highest priority of the 8751 program is servicing the asynchronous receiver/transmitter. This is accomplished by setting the serial port interrupt to the highest priority and always having that interrupt enabled.

The 8751 distinguishes between 'code' and 'data' from the VAX. Command code is expected to be received in the symmetric format described in "Appendix A. Protocol and Data Format in VAX/8751 Communications" on page 26, while data is unformatted. The two different classes of communication are treated completely differently from the moment they are received.

The following discussion refers to various locations in 8751 internal RAM, the allocation of which is shown in Figure 18 on page 104.

Processing Commands in the Interrupt Routine

The serial-port-interrupt-service subroutine only distinguishes between the two classes of communication by the value found in the location denoted NR, which is short for 'Number of data bytes to Receive'. If NR is zero, then the communication from VAX is taken to be a command code.

Command codes received from the VAX are immediately moved into a holding location, called the Serial Port Read Buffer. The code is held there until all data associated with it have also been received, after which the code is moved to the VAX Command Buffer, where it will be detected by the main program and decoded.

The foregoing process may take several iterations of the serial-port-interrupt-service subroutine, depending on the amount of data expected with the particular command.

Processing Data in the Interrupt Routine

If the number NR is not zero, then the communication from VAX is taken to be data. There is a 15-byte receive-data buffer in 8751 internal RAM. Data associated with a command code is held there until all of it is received, after which the main program is allowed to process it.

The data arriving over the serial port is put in the location computed by adding the number (NR - 1) to the lowest address of the receive-data buffer. After a data byte is received the number NR is decremented by one. Thus, the last byte of data received will always be at the bottom of the receive-data buffer.

Processing Communications in the Main Routine

If the main routine is not currently processing a command, then it will look for the arrival of a new command code in the VAX Command Buffer. When a code appears there, it is moved to the

VAX Command location, and the decode-VAX-command subroutine is called to take the appropriate action.

That subroutine will generate a response, and may also generate data, that must be transmitted to VAX. The response appears in the Response Code location, and the data appears in the 16-byte write-data buffer.

The number of data bytes generated appears in NTBUFF, where it is 'invisible' to the various transmit routines until the VAX has sent a request for data. At that time, it will be moved to the NT location, where NT is short for Number of data bytes to Transmit.

After a response to a command is generated, the Write-to-VAX subroutine is invoked. If the transmitter is idle, the code is sent immediately; otherwise, it is queued for transmission.

Transmitting Responses

The priority of transmission is this:

1. Data for transmission (determined by NT not zero, where NT denotes the Number of data bytes to Transmit).
2. Contents of the Serial Write Buffer
3. Contents of the Response Code location.
4. A request for data, if VAX has indicated it has data to transmit.

If the transmitter is not idle, but the Serial Write Buffer is empty, then the contents of the Response Code location are moved to the Serial Write Buffer (queued for transmission).

After a byte of data is transmitted, the number NT is decremented by one. Thus, the value of NT indicates not only how much data is left to transmit, but also points to the location of the next byte to transmit, in the same manner as NR, above.

For details, see "The Serial Output Subroutine" on page 132 and "The Serial Port Interrupt Service Subroutine" on page 144.

APPENDIX C. PROTOCOL AND DATA FORMAT IN 8751/8748 COMMUNICATIONS

COMMUNICATING COMMAND CODES

All command codes have a common format which promotes quick code validation. The format is easily seen if the codes are written as hexadecimal (hex) numbers. In all cases, the upper and lower hex digits are identical. In other words, from each hex code, the hex number 11 (decimal 17) can be factored.

Complete lists of the codes which the 8751 and the 8748 can send each other are given in Figure 6 on page 42.

The command codes sent between the 8751 and 8748 result in the completely predictable responses written into software. These are called the communication protocol, and are tabulated in Figure 7 on page 43.

COMMUNICATING DATA

All data passed between the 8751 and the 8748s is passed through the shared RAM. There is only one set of data for which the 8748 requires a different format from the 8751 than the 8751 requires from the VAX. That is, the 8751 passes on all other data to the 8748's in exactly the same form they were received from VAX.

The data that are reformatted are the move distance data. The main reason is to remove a considerable computational burden from the 8748 and put it on the 8751. Since the 8751 is a more powerful microprocessor, the same tasks are not as difficult to perform.

The reformatting of the move distance data is outlined here.

- The sign bit is stripped off of the high byte of the distance, leaving only a 15-bit magnitude, which is moved to the low and high byte 'next move' locations in shared RAM.
- The sign bit is loaded into the 'next move sign' location in shared RAM, where it is in the eighth bit position, with all other bits cleared.

- If the 15-bit move is not zero, the 'next move received' flag in shared RAM is set to a non-zero value; otherwise, it is set to zero.
- If the 15-bit move exceeds the number 31, then the 'next move infinite' flag in shared RAM is set to a non-zero value; otherwise, it is set to zero.

Data passed from the 8748 to the 8751 are forwarded to VAX in unchanged format, with the exception of velocity data. The velocity data come from the 8748's as seven bit magnitudes with the direction sign in the eighth bit positions. The 8751 reformats that data into 8-bit, two's complement numbers before sending them to VAX.

COMMAND CODES FROM INTEL 8751 TO INTEL 8748's		
CODE	MNEMONIC	COMMAND
0	NOP	no operation
136	OVR	Send previous code over again
153	CRM	Clear remaining moves
170	MOV	Move
187	HLT	Halt
204	AGO	Go
221	48PK	'Peek' into internal 8748 RAM
	WR48	'Poke' into internal 8748 RAM
238	RAP	Reset absolute position
255	KFF	Coefficients

COMMAND CODES FROM INTEL 8748 TO INTEL 8751		
CODE	MNEMONIC	COMMAND
0	NOP	no operation
136	OVR	Send previous code over again
153	MTRSTL	Motor is stalled
170	HDWRST	Hardware reset
187	RDYNXT	Ready for next move
204	DAT	'Peek' data ready

Figure 6. Command codes between 8751 and 8748.

8751 ORIGINATED CODE	8748 RESPONSE	8748 ACTION
NOP (0)	none	none
OVR (136)	1 byte data	clear previous code location
CRM (153)	none	clear all present move, next move, pulsewidth magnitude and velocity data
MOV (170)	none	read next move data in from shared RAM to internal RAM next move locations
HLT (187)	none	clear the 'go' flag
AGO (204)	none	set the 'go' flag
RAP (238)	none	clear the absolute position locations in shared RAM
KFF (255)	none	read coefficients in from shared RAM to the internal RAM coefficient locations
WR48 (221)	none	read in 'poke' data from shared RAM into the specified internal RAM location
48PK (221)	DAT (204)	read in 'peek' address from shared RAM and put data from that address in internal RAM in data passing location of shared RAM

8748 ORIGINATED CODE	8751 RESPONSE	8751 ACTION
NOP (0)	none	none
OVR (136)	1 byte data	clear previous code location
MTRSTL (153)	HLT (187)	set the motor's stall flag, halt all motors, and send 'motor stalled' code to VAX
HDWRST (170)	none	set the motor's 'hardware reset' flag, halt all motors, and send 'hardware reset' code to VAX
RDYNXT (187)	none	clear the motor's 'not ready for next move' flag

Figure 7. 8751/8748 Communications protocol and resulting actions.

APPENDIX D. THE MAILBOXES

8748 ACCESS TO THE MAILBOXES

There are two mailboxes associated with each 8748. The 8748 can read command codes from its read mailbox that were put there by the 8751; the 8748 can write command codes to its write-mailbox for the 8751 to read.

Some confusion may arise over the fact that the 8748-read-mailbox is one of the seven 8751-write-mailboxes; and the 8748-write-mailbox is one of the seven 8751-read-mailboxes. However, it need only be remembered that each microprocessor reads from its own read mailbox and writes to its own write mailbox.

The mailboxes are shown in functional block diagram form in Figure 8 on page 49. The diagram also shows the method by which the 8748 addresses its mailboxes. The same diagram is shown in schematic form in Figure 23 on page 110.

For the 8748, the binary address 100xxxxx (where x indicates

either a zero or a one), when written on Port 2, will cause the mailbox-enable line to become active (low). That line serves a dual purpose.

When it is active, the mailbox-enable gates the read- and write-pulses from the 8748 through to the read- and write-mailboxes. Notice that it also gates the write-mailbox-flag through to Test Input 1 of the 8748; when it is not enabled, the read-mailbox-flag is gated through to that same test input. So the read-mailbox-flag is tested when the mailboxes are not enabled, and the write-mailbox-flag is tested when they are enabled.

Thus, putting the mailbox-enable address on Port 2 is a device select operation. When they are enabled, the mailboxes act very much like random access memory (except, of course, no address need be multiplexed on the bus lines to read or write). The 8748 software access the mailbox only from the main routine, which is given in detail in the appendix, "Listing of the 8748 Assembly Language Program."

8751 ACCESS TO THE MAILBOXES

The 8751 has up to fourteen mailboxes to which it must gain access, two for each motor. The access scheme is similar to that of the 8748s, only on a larger scale. The details of addressing the mailboxes can be found in the Respond-to-8748, Decode-8748-Command, and Global-Write subroutines in the appendix, "Listing of the 8751 Assembly Language Program."

The hardware which implements the access scheme is shown in block diagram form in Figure 10 on page 51 and Figure 9 on page 50, and in schematic form in Figure 22 on page 109.

Two 74LS138 decoders are used to gate the 8751 read- and write-pulses through to the proper mailboxes. Note that 8751 Port 2 is used to output the device address.

The read-mailboxes are addressed by a binary number `xaaa0xxx`, where 'aaa' is the (binary) motor number assigned to the mailbox being addressed, and x indicates either a zero or a one.

The write-mailboxes are addressed by a binary number `laaa0xxx`, where 'aaa' is the (binary) motor number assigned to the mail-

box being addressed, and x indicates either a zero or a one. Note that if 'aaa' = '000', then all seven write-mailboxes are addressed simultaneously; thus, the write-mailboxes can be addressed either globally or locally.

The mailboxes behave like random access memory from the point of view of the 8751, except no address need be multiplexed on Port 0 to perform a read or write. However, the 8751 (unlike the 8748) cannot perform a read or write on Port 0 without multiplexing some address; so whenever a mailbox is read from or written to, a dummy address is specified.

The 8751 checks the mailbox flags, just as the 8748 does. With reference to Figure 10 on page 51, it can be seen that the same addresses that access the read-mailboxes on Port 0 also enable the output of the read-mailbox-flag latch onto Port 1. (Note that the address 00000000 on Port 2 also enables the read-mailbox-flag latch output.)

Similarly, the same addresses that access the write-mailboxes on Port 0 also enable the output of the write-mailbox-flag latch onto Port 1.

The system was designed that way to allow a mailbox's flag to be

checked using the same address that accesses the mailbox, where the state of the flag appears at Port 1 and the mailbox is accessed through Port 0.

The mailbox flags from motor 1 appear in the bit 1 position of Port 1 input, those from motor 2 appear in the bit 2 position, etc. This scheme allows quick isolation of the flag of interest within the 8751 software.

The schematic of the hardware for addressing the mailboxes and accessing the flags is given in Figure 22 on page 109.

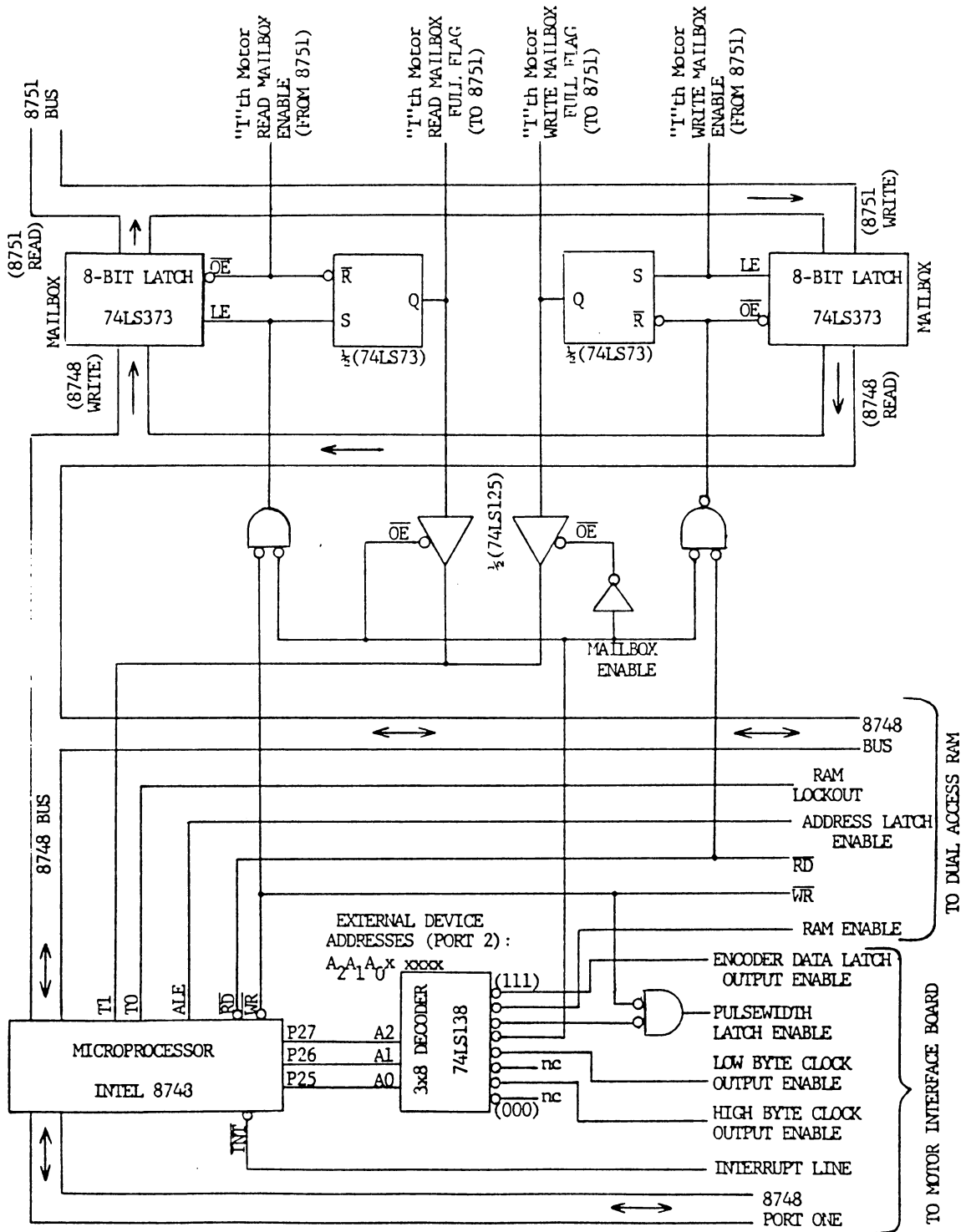


Figure 8. The mailboxes and the 8748 device addressing scheme.

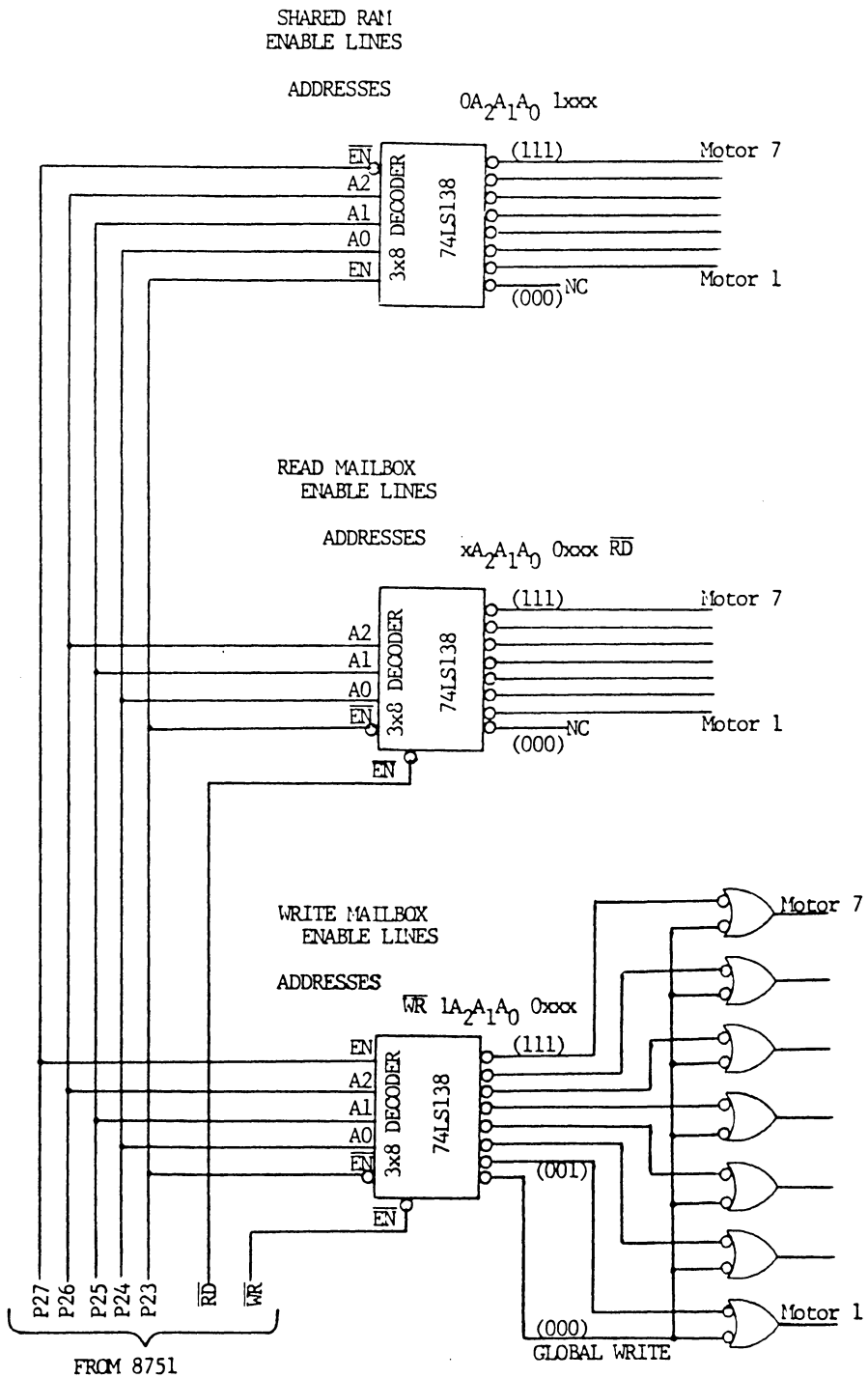


Figure 9. 8751 Port 0 Input Device Addressing Scheme.

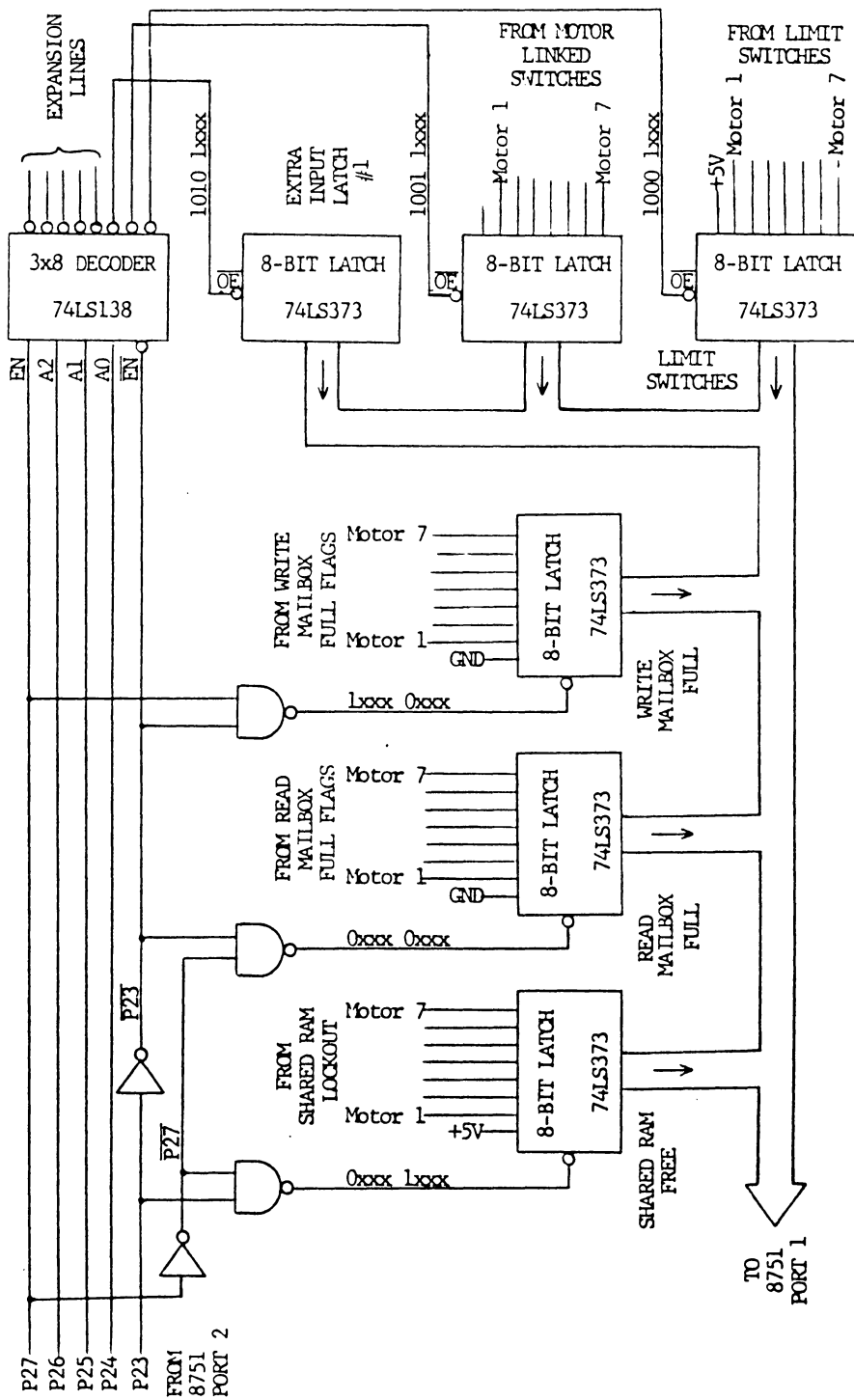


Figure 10. 8751 Port 1 Input Device Addressing Scheme.

APPENDIX E. THE SHARED RANDOM ACCESS MEMORY

The shared random access memory (RAM) appears to both the 8748 and 8751 as a normal external RAM. In practice, the only difference is that it must be ascertained that the other device with access is not using it before proceeding to read or write.

For the purpose of protecting the various hardware devices, the system was designed with an absolute 'hardware lockout'. That is, if one of the microprocessors is using the shared RAM, it is impossible for the other one to do so. So it is that the one which is locked out could go through the motions of reading or writing, but the result would be the same as if there were no RAM connected to it. That design was achieved by the use of tri-state buffers on every line that is needed to read and write to the RAM.

With reference to Figure 11 on page 55, it can be seen that the data bus lines from each microprocessor must be enabled through the 74LS245 tri-state bus transceiver before any address or data can be passed to or from the shared RAM. The control lines, consisting of the address latch enable and the read- and write-pulse lines, must also be enabled through tri-state buf-

fers, before a read or write can be performed.

The heart of the lockout system is the 74LS74 dual delay-type flip-flop with overriding presets. The sequence of events is as follows:

1. The microprocessor program puts the address on Port 2 which selects the shared RAM.
2. The device select logic decodes the Port 2 address and activates the (low active) shared RAM enable line.
3. The microprocessor attempting to gain access tests its lockout line: if it is high, then the other microprocessor is locked out, and the read or write can be performed; if it is low, then the other microprocessor is using the shared RAM, so a waiting loop is performed until the lockout line goes high.
4. When the lockout line is high, the delay flip-flop, which is being clocked at 6 MHz, gates the low enable through to the various tri-stated buffers, connecting the address/data bus to the address latch and to the shared RAM, and connecting the control lines to their appropriate points.
5. The active low output of the the delay flip-flop is also connected to the overriding preset of the other half of the

dual flip-flop, causing it to remain in the set (inactive) condition, regardless of the input, thus locking out the other microprocessor.

6. After the read or write is performed, the enable address is removed from Port 2 to allow the other microprocessor to have access to the shared RAM.

Note the necessity for the pull-up resistors at the tri-state outputs. This prevents spurious chip selecting and address latching, thus conserving power and extending the life of the memory chips.

A detailed schematic of the shared RAM can be seen in Figure 21 on page 108.

The scheme for 8748 access to the shared RAM is shown in block diagram form in Figure 8 on page 49 and in schematic form in Figure 23 on page 110.

The scheme for 8751 access to the shared RAM is shown in schematic form in Figure 20 on page 107, which corresponds to parts of the two block diagrams, Figure 9 on page 50 and Figure 10 on page 51.

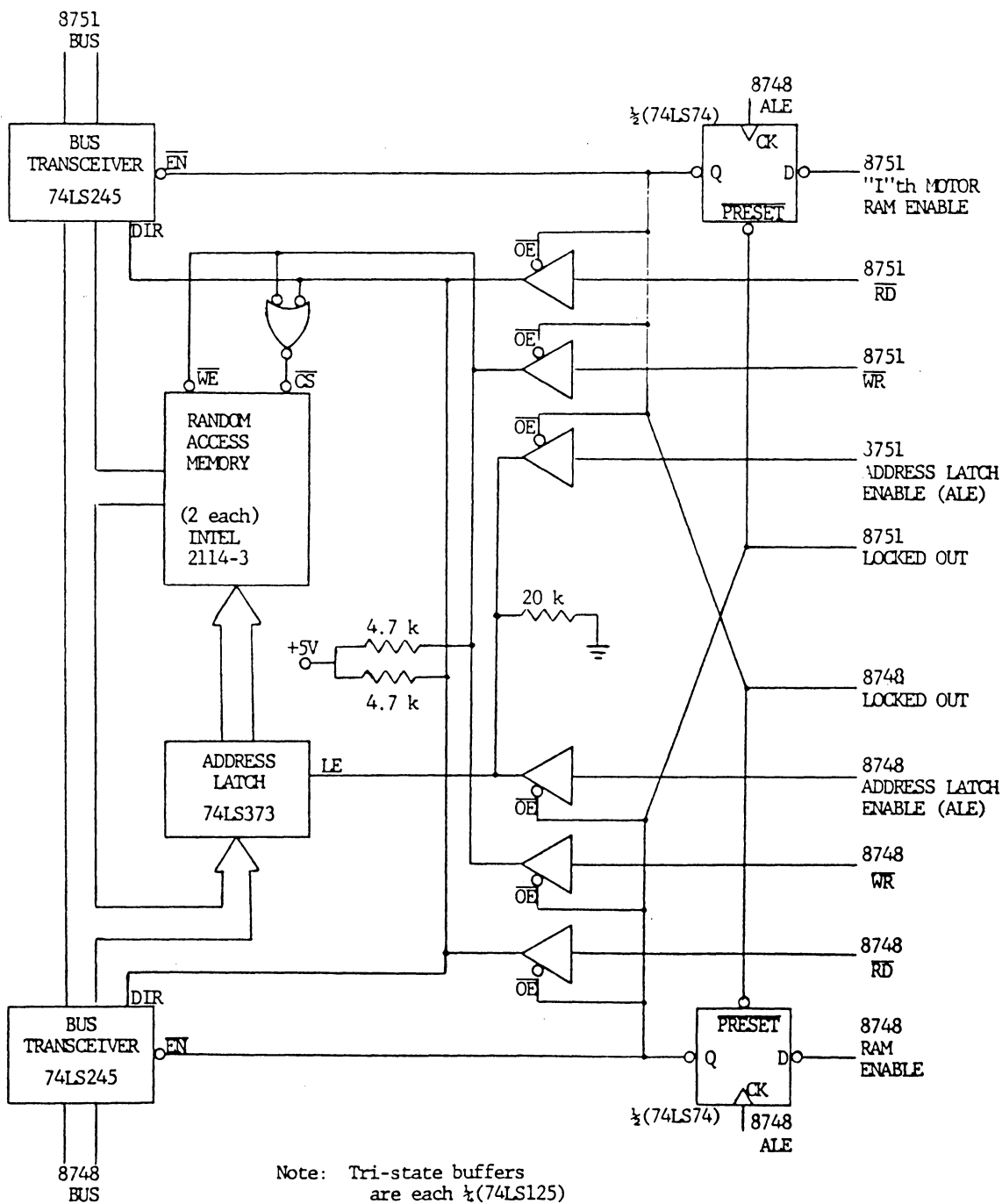


Figure 11. Block diagram of the shared RAM.

APPENDIX F. THE COMMANDS FROM VAX

The various commands which can be sent from the VAX are listed in Figure 2 on page 30. Those which can be considered to originate from the VAX, as opposed to being used only in response to 8751 codes, are shown along with their protocol in Figure 3 on page 31.

COMMANDS CONTROLLING THE STATE

Commands which change some state of the 8748's or the shared RAM are said to control the state. Commands in this category are somewhat self-explanatory. They are listed here:

- HALT (HLT) : This command clears the 'go' flags in all the 8748's, and can be considered to put the robot in the halt state; in that state no power is applied to any of the motors, but the 8748's keep track of changes in position.
- GO (AGO) : This command sets the 'go' flags in all the 8748's, and can be considered to put the robot in the go

state; in that state the 8748's attempt to reduce position error to zero, using the current value of the velocity set point for velocity control.

- RESET ABSOLUTE POSITION (RAP) : This command causes all 8748's to set their absolute position counters to zero.
- WRITE TO 8748 (WR48) : This command has data associated with it which will be written into the internal RAM of the specified 8748; it is referred to elsewhere in this document as the 'poke' command.
- COEFFICIENTS (KFF) : This command allows the user to write the various position error coefficients and magnitude limits, the gripper closed pulsewidth (ignored by all but the gripper controller), the starting pulsewidth, pulsewidth hysteresis value, and long and short overshoot pulsewidths to a specified 8748 internal RAM.
- MOVE (MOV) : this command allows the user to alter the values of the position error and velocity set point in all of the 8748's at one time.
- CLEAR REMAINING MOVES (CRM) : this command causes all 8748's to set their internal position error, next move data, and velocity data locations to zero; note that if the motors are in motion, the configuration when this command is received becomes the point of zero position error.

COMMANDS MONITORING THE STATE

Commands which are used to determine the state of the system are said to monitor the state. They are listed here:

- VELOCITY DATA REQUEST (VRQ) : This command results in a stream of data from the 8751 representing the current motor velocities and the internal time (Rhino Clock) of the system.
- POSITION DATA REQUEST (PRQ) : This command results in a stream of data from the 8751 representing the current configuration of the motors with respect to some calibration point, and the internal time (Rhino Clock) of the system.
- SEND LAST CODE OVER AGAIN (OVR) : This command causes the 8751 to repeat the most recent command code sent to VAX.
- PEEK 8748 (48PK) : This command results in a stream of data from the 8751 representing the data found at the specified location in each 8748, and the internal time (Rhino Clock) of the system.
- PEEK 8751 (51PK) : This command results in a stream of data from the 8751 representing the data found at the specified location in the 8751, and the internal time (Rhino Clock) of the system.

- PEEK SHARED RAM (SHRPK) : This command results in a stream of data from the 8751 representing the data found at the specified location in all of the shared RAM's, and the internal time (Rhino Clock) of the system.

REPETITIVE COMMAND FUNCTION (COMMAND-ON-INTERRUPT)

There is one pair of commands that does not fit into either of the preceding categories. The function of this command pair is to allow a state-monitoring command to be repeated quickly without actually sending it from the VAX.

When this function is invoked, it is accompanied by the code of the command that is to be repeated. Execution of the accompanying code then occurs whenever the state of 8751 Interrupt 0 falls from high to low. Whenever that interrupt condition occurs, the Rhino Clock is incremented as well (it is not incremented at any other time).

The intent of this design is that the Interrupt 0 line should be connected to a constant frequency square-wave generator. That

causes the Rhino Clock to be an accurate measure of the passage of time relative to the system. Then, whenever one of the monitor commands is repeated, there is a time-identifier along with the system data. Thus the Rhino Clock provides data for accurate time graphing of system states.

ENABLE COMMAND-ON-INTERRUPT (ECI) : This command is accompanied by one of the commands, VRQ, PRQ, PK48, PK51. The accompanying command will be queued for execution each time the Interrupt 0 line falls from high to low. In the case of the peek commands, the last address specified for a peek before the ECI command is used for the repetitive peek.

DISABLE COMMAND-ON-INTERRUPT (DCI) : This command causes the interrupt command buffer to be cleared (effectively loading the no-operation command). Thus, when Interrupt 0 transits high to low, the Rhino Clock is still incremented, but no command is queued for execution.

APPENDIX G. SHAFT POSITION ENCODING

THE SHAFT ENCODER DISK AND ANGULAR MEASURE

The shaft encoder disk is a disk that is attached to the motor shaft to provide position feedback. It has two perforated annular regions which allow light from light-emitting diodes to reach photo-sensitive transistors when the disk is in certain positions, and which block the light in other positions. A typical disk is shown in Figure 12 on page 65, where the perforations are arranged in what is called quadrature encoding.

The reason for quadrature encoding is that the succession of two-bit 'words' from the collectors of the photo-sensitive transistors when the motor is rotating clockwise is the opposite of the succession generated by counterclockwise motion. Thus the direction of motor motion can be deduced by inspection of the two-bit encoder output sequence.

It seems natural to use the encoder shaft to measure angular distance. In this document, the distance of motor shaft angular motion is discussed in terms of 'holes'. One hole is

defined as the angular distance from the center of a position where the encoder bits are (0,0) to the center of the next position where the encoder bits are (0,0). The three intermediate positions will be referred to as 'quarter-hole' positions, and the angular distance from one to the next is called one quarter-hole.

Note that the resolution of the encoder disk attached to a particular motor determines the constant of proportionality between velocity in holes per second and velocity in revolutions per minute (r/min) for that motor.

ENCODER OUTPUT

The output of the encoder comes from photo-sensitive transistors. Thus, when a void area of the encoder disk falls between the light source and the transistor, the transistor is switched on; when a solid area of the disk falls between them, the transistor is switched off.

Consider what happens when the transistor is switched on, but a

solid part of the disk is rotating into position between the light source and the photo-sensitive transistor. As the shadow of the solid area falls onto the transistor, the amount of light falling onto it decreases. However, the decrease in light is not abrupt, especially at slow speeds, so the transistor operates over its linear region for the period during which transition from light to dark is occurring.

Linear operation is not desirable in a digital system. It is therefore necessary to condition the data from the position encoder. In particular, the transitions between low and high levels should be quite abrupt; that is, the encoder output should be two square waves, regardless of motor speed. That is the function of the bit-shaping circuitry, shown in block form in Figure 13 on page 66 and in complete detail in Figure 24 on page 111.

Referring to the block diagram, it can be seen that each photo-sensitive transistor's output is compared to a +2.5-volt reference by an LM339 comparator. This causes the transitions between low (0 volts) and high (5 volts) levels to occur in only a few nanoseconds.

The 220 kilohm and 1 megohm resistors provide hysteresis in the

comparison process. A simple analysis shows that they cause the low-to-high transition to occur at 3.05 volts, while the high-to-low transition occurs at 1.95 volts. The point of introducing hysteresis is to prevent the comparator from oscillating when the input voltage from the photo-sensitive transistor is changing slowly and is close to the transition voltage.

Notice that 4.7 kilohm pull-up resistors are needed for both the open-collector photosensitive-transistors and the comparator outputs.

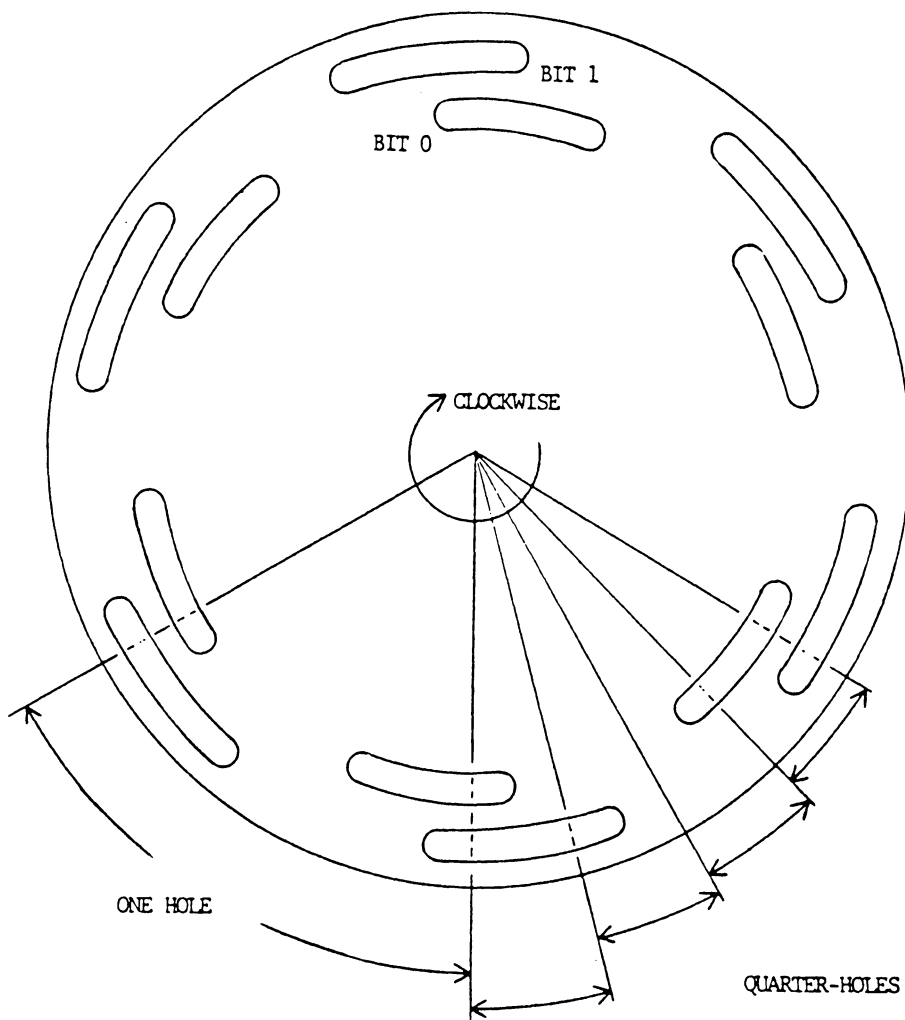


Figure 12. Typical shaft encoder disk and its natural angular measurement.

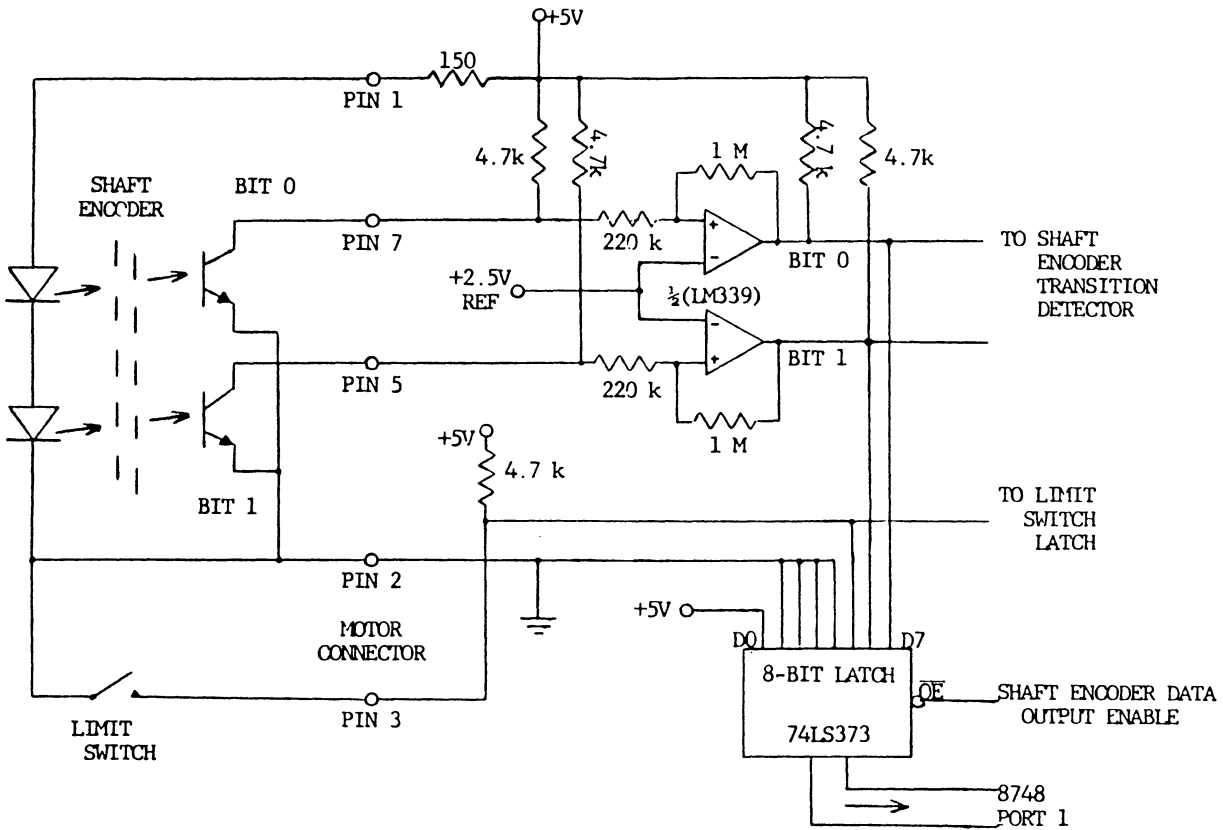


Figure 13. Block diagram of the shaft encoder and output conditioning.

APPENDIX H. 8748 INTERRUPT GENERATION

MOTOR MOTION INTERRUPT GENERATION

The position encoder output is used to detect motor motion. Referring to Figure 14 on page 70, it can be seen that any transition of either of the encoder bits will trigger one of the four edge-triggered, one-shot multivibrators. Once triggered, a multivibrator remains high for 700 microseconds (timing circuitry is shown in detail in Figure 25 on page 112), during all of which time it holds the 8748 interrupt line in the active condition.

For that reason, when the interrupt service routine in the 8748 finishes servicing a motion interrupt, it must wait until the interrupt line becomes inactive before returning from the routine. Otherwise, it could respond to the same interrupt more than once.

The point of that arrangement is to provide an easy distinction between an interrupt that is generated by motor motion, and one that is generated by lack of motor motion. In the latter case,

the interrupt line is held active only until an interrupt acknowledge signal is sent from the 8748; in the former case, the acknowledge signal has no effect on the state of the interrupt line.

MOTOR STOPPED INTERRUPT GENERATION

As shown in Figure 14 on page 70, the time elapsed since the last interrupt is measured by a two-byte clock. (For more details on interrupt clocking, see "Appendix K. Velocity Bookkeeping in the 8748" on page 79.) If the time since the last interrupt exceeds 1/16 second, then motion, if any, is so slow that the motor is assumed stopped. An interrupt must therefore be generated to notify the 8748 of the stopped condition.

That task is performed by the motor-stopped flip-flop, shown in the same figure. If the clock counts up to 1/16 second before a motion interrupt, then the motor stopped flip-flop is set, which holds the interrupt line active. That flip-flop is only cleared when an interrupt-acknowledge signal is sent from the 8748. Note that the interrupt-acknowledge signal also per-

forms the task of enabling the encoder-data-latch output onto the 8748 Port 1.

If a motion interrupt occurs during the time that the motor-stopped flip-flop is set, or while the motor-stopped interrupt is being serviced, that interrupt is not lost. It lasts for 700 microseconds, so it is detected when the motor-stopped subroutine finishes (unlike motion interrupt servicing, motor-stopped servicing does not wait for the interrupt line to become inactive before returning).

For details of those routines, see "The Motor Stopped Subroutine" on page 160 and "The Interrupt Service Subroutine" on page 153.

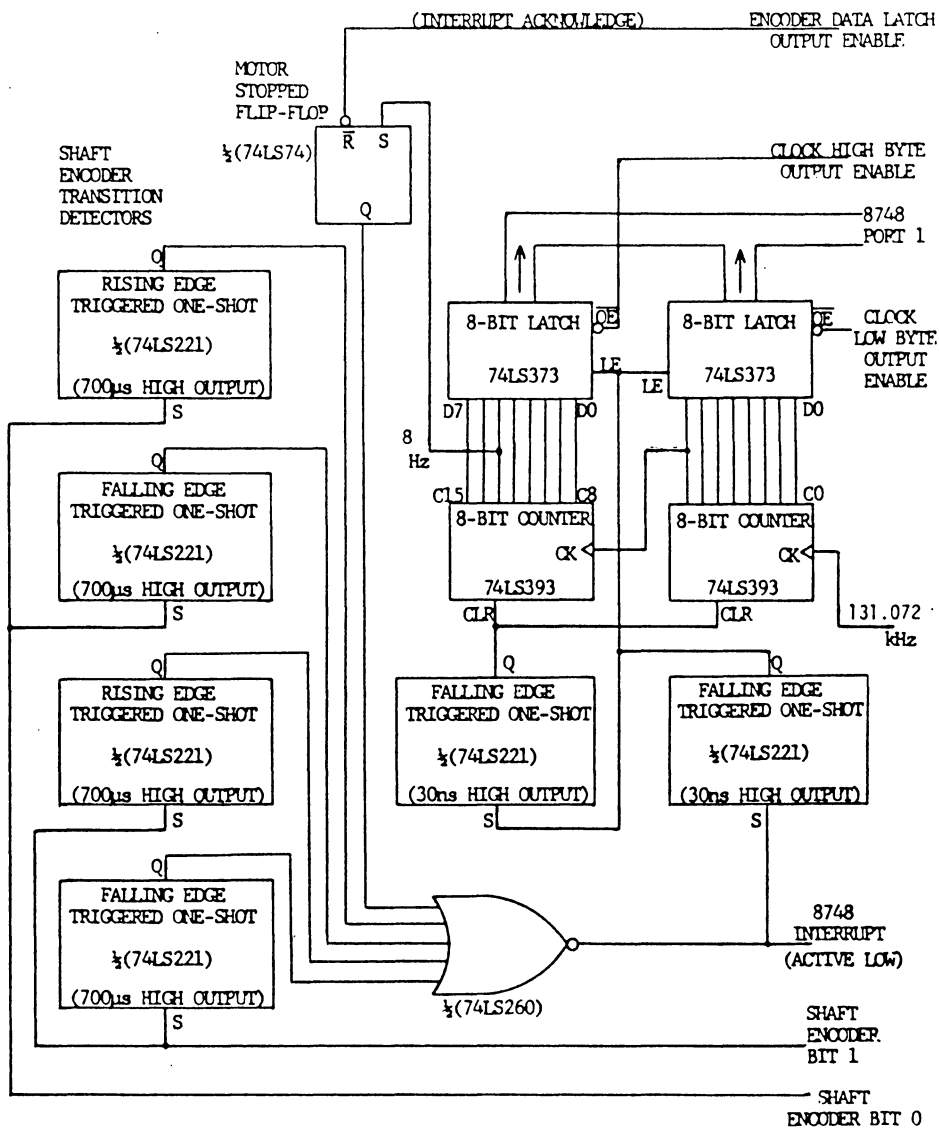


Figure 14. 8748 interrupt generation and clocking.

APPENDIX I. KEEPING TRACK OF DIRECTION

It is quite important to know the current direction of motion, but equally important is to know the direction of motion during the previous interrupt, and how the direction of motion relates to the commanded direction of motion.

As for the direction of motion, quadrature encoding allows a very simple detection scheme. The value of encoder bit 1 is taken 'exclusive-or' with the previous value of encoder bit 0. The result of that operation is zero if the direction is clockwise, and one if the direction is counter-clockwise, and can thus be used as the value for the absolute-direction flag.

At this point in the interrupt-service subroutine the value of the previous absolute-direction flag is still available. The 'exclusive-or' of the present and previous absolute-direction flags yields a one if a reversal has just occurred.

If reversal has just occurred, then the new-motion flag must be set. The reason is, of course, that the motor had to come to a full stop before reversing direction. Also, if the previous-position-(0,0) flag is clear, then the

reversal-since-last-update flag must be complemented. (For more details on the reversal-since-last-update flag, see "The Absolute Position Counter" on page 73.)

The absolute-position flag can now be taken 'exclusive-or' with the sign of the present move command (position error) to yield a value for the relative-direction flag. The relative-direction flag will thus be zero if motion is in the commanded direction, and will be one if motion is opposite the commanded direction.

All the flags mentioned in the foregoing are located in Registers 6 and 7 of 8748 Register Bank 1. For complete details on how the updating is accomplished, refer to "The Interrupt Service Subroutine" on page 153, step 4, and the associated section of the program listing, in the appendix "Listing of the 8748 Assembly Language Program".

APPENDIX J. POSITION BOOKKEEPING IN THE 8748

There are several locations in RAM that keep track of position. Each position data location serves a specific function in the overall task of position control. After each interrupt due to motor motion, the various position data locations must be updated.

THE ABSOLUTE POSITION COUNTER

The absolute position counter in shared RAM holds a signed, two-byte number representing the sum of all moves since the absolute position counter was last set to zero. (Note that the command 'reset absolute position' will set the absolute position counter to zero, as will a hardware reset.)

The number is in the angular measure of encoder disk holes, so it must be updated only when the encoder is in the (0,0) position. That is, on those interrupts occurring at quarter-hole positions that are not (0,0), the absolute position counter is

not updated. It is arbitrary which of the four quarter-hole positions is chosen as the one on which to update the counter; (0,0) was chosen because it is easy to detect. (For a discussion of angular measurement in 'holes', see "Appendix G. Shaft Position Encoding" on page 61.)

Notice that if the direction of motion reverses while the encoder disk is not in the (0,0) position, then the next time the encoder reaches the (0,0) position it would be a mistake to change the number in the absolute position counter, since the encoder disk has merely backtracked to its previous position. For that reason, it is necessary to keep track of reversals which occur when the motor is not in the (0,0) position.

That is the function of the reversal-since-last-update flag. For every reversal occurring in a position other than (0,0), that flag is complemented. That requires knowledge of the previous position, since a reversal is not detected until the position has changed.

That is the function of the present-position-(0,0) and the previous-position-(0,0) flags. When a motion interrupt occurs, the value of the former must be moved to the latter to update it. (Later, during the position-update subroutine, the pres-

ent-position-is-(0,0) flag is updated). So, if a reversal is detected and if the previous-position-(0,0) flag is clear, the reversal-since-last-update flag is complemented.

During the position-update subroutine, the absolute position counter is only updated if the present position is (0,0) and the reversal-since-last-update flag is clear. The updating depends on the absolute direction of motor motion. If the absolute-direction flag is set, then motor motion is counter-clockwise, and the absolute position is decremented. Otherwise, the absolute position is incremented.

THE PRESENT MOVE COMMAND (POSITION ERROR)

The present move data is a signed, two-byte number in internal RAM. For the purpose of the following discussion, it will be called the position error. It is measured in angular units of encoder holes, so (like the absolute position counter) it is only updated when the encoder position is (0,0) and the reversal-since-last-update flag is clear.

Unlike the absolute-position, however, the updating of the position error is dependent upon the direction of motion relative to the commanded direction. If the relative-direction flag is clear, then the motor is moving in the commanded direction, so the position error is decremented (since position error is being reduced). Otherwise, position error is incremented.

The position error can also be altered by issuing a new move command. When the position error is small and there is a new move command in the same direction waiting to execute, the new move command and the position error will be summed to yield a new value for the position error. If the position error is zero, then any new move is brought in immediately upon detection.

It should be added that new move commands are detected only during the interrupt service subroutine, to ensure that a standard measure of time is allowed for the motor to start moving after initial power is applied to it.

THE QUARTER-HOLE TAIL

It was considered desirable to control the position with quarter-hole resolution rather than, as the original controller did, with only full hole resolution. So, while the position counters only register full hole changes in position, the controller is operating at the quarter-hole level.

To reduce storage requirements, the quarter-hole tail was designed to represent only the number of quarter-holes moved since the last interrupt, relative to the commanded direction of motion. So it is, effectively, the low order two bits of the position error.

The quarter-hole tail, unlike the other position data locations, must be updated after every motion interrupt, regardless of reversals, etc. If the relative-direction flag is clear, the quarter-hole tail is decremented since the number of quarter-holes of position error is decreasing. Otherwise, it is incremented. However, every time the position is (0,0), the quarter-hole tail is cleared, forcing its magnitude to be modulo four, as it was designed to be.

The quarter-hole tail serves only one purpose. The Move-Yet? subroutine (see "The Move Yet? Subroutine" on page 162) uses it to detect small position errors whenever there is no large position error.

APPENDIX K. VELOCITY BOOKKEEPING IN THE 8748

MEASURING THE MOTOR SPEED

The motor speed is determined by measuring the time between motion interrupts, and finding the reciprocal of that time. The timing is done by two 8-bit dividers (74LS393s), as shown in Figure 14 on page 70.

Clocking the Interrupt Interval

When the interrupt line becomes active, its transition from high to low triggers a 30-nanosecond pulse from the one-shot multivibrator that latches the value of the clock bytes onto their respective (tri-state) bus buffer latches. As that 30-nanosecond pulse finishes, its falling edge triggers another 30-nanosecond pulse that clears the clock value to zero. In that way, the clock counts only the elapsed time between interrupts.

A detailed schematic of the timing and interrupt circuitry is given in Figure 25 on page 112.

Taking the Reciprocal

The following scheme was devised to simplify the task of determining the reciprocal of the clock time.

The most significant eight bits of the clock count can always be expressed in the form

$$(1.xxxxxxx) \times 2^{**m}$$

where m is equal to the bit position of the most significant bit, from 0 to 15, and each 'x' can be either one or zero.

The elapsed time is simply the clock count divided by the clock input frequency. There is a distinct advantage to be gained by making the clock input frequency an exact power of 2. The advantage is that the quotient which yields the elapsed time can then be written (in terms of the eight most significant

bits) as

$$(1.\text{xxxxxxxx}) \times 2^{(m-n)}$$

where n is the base 2 logarithm of the clock input frequency, $2^{**} n$, and $(m-n)$ is an integer.

The reciprocal is thus

$$(1/(1.\text{xxxxxxxx})) \times 2^{(n-m)}$$

Finding the reciprocal of any elapsed time is therefore reduced to finding the binary reciprocal of $1.\text{xxxxxxxx}$ and shifting the result $n-m$ times. Since there are only 128 different values of the form $1.\text{xxxxxxxx}$, a 128-byte look-up table is used to determine the reciprocal.

Note that the reciprocal satisfies the binary inequality

$$0.1000000 < 1/1.\text{xxxxxxxx} \leq 1.0000000$$

However, the numbers in the look-up table are between 128 and 255, to maximize the resolution of the table. Therefore, the reciprocal from the look-up table has been pre-multiplied by

256, or $2^{**} 8$.

Thus, the equation for velocity, denoting the returned value from the look-up table by LTV, is

$$\begin{aligned} & ((LTV) \times 2^{**} -8) \times 2^{**} (n-m) \\ & = LTV \times 2^{**} (n-m-8) \end{aligned}$$

Therefore, the value returned from the look-up table is shifted $(n-m-8)$ times to obtain the velocity value.

It remains to determine a suitable value of $2^{**} n$, the input clock frequency. The frequency $2^{**} 17$ was chosen for several reasons. First and foremost, it is fast enough to allow discrimination between speeds of 254 and 255 holes per second, which is slightly faster than any of the motors can move. However, another consideration was that it also produces subharmonics as slow as 2 Hz in the interrupt clock. Initially it was not known what the rate of motor stop interrupt generation should be, so it was deemed useful to have such slow frequencies available.

The value of input clock frequency chosen, then the velocity equation is

$$\text{LTV} \times 2^{**} (9 - m)$$

Note, however that the result is in interrupts per second, which is the same as quarter-holes per second. To get the velocity in holes per second, that result must be divided by four; or, equivalently, multiplied by $2^{**} -2$. Furthermore, the result is formatted for only seven bits, rather than eight, so the result must be divided once more, by two. Finally, then velocity is found by shifting the look-up table value, LTV, according to

$$\text{LTV} \times 2^{**} (6-m)$$

where m is the bit position of the most significant digit of the clock count, from 0 to 15. Implementation of this scheme is outlined in "The Interrupt Service Subroutine" on page 153, step 5, with assembly language details in the associated section of the appendix "Listing of the 8748 Assembly Language Program".

DETERMINING VELOCITY ERROR

Velocity error is determined very simply by subtracting the current velocity error from the velocity set point. While this actually gives the negative of the velocity error, that number indicates the direction in which power to the motor should be changed. That is, if velocity is larger than the set point, power to the motor should be reduced.

Before subtraction is performed, however, it is necessary to check the sign of the velocity relative to the set point. If the motor is moving in the wrong direction, then velocity is actually negative, relative to the set point. In that case, the magnitude of the velocity is added to the set point to obtain the velocity error.

DETERMINING THE DIRECTION OF ACCELERATION.

The direction of acceleration is determined simply by subtracting the previous velocity from the present velocity. The result is used to determine when to stop integrating the velocity error.

For example, if the velocity exceeds the set point, then the motor power is decreased by subtracting the product of the velocity error and a coefficient specified from VAX, from the present pulsewidth. That effectively integrates the velocity error, over a period of many motion interrupts. However, when the motor velocity begins to decrease towards the set point, there is no need to decrease the power to the motor any further, since the desired change has already begun to occur. (An analogous test is made if the velocity is below the set point.)

That scheme was found to have a stabilizing effect on the motor velocity at all set points.

APPENDIX L. BOOKKEEPING TASKS IN THE INTEL 8751

(HARDWARE) THE MOTOR LINKED LATCH

Occasions may arise when it is not desired (or not possible) to connect all motors to the system. Indeed, the 8751 is capable of facilitating seven motors, while the Rhino has only six. (The additional capability was provided in anticipation of sensor experimentation.) There must be a method for the 8751 to determine which motors are in service.

The function of the motor-linked switches is to provide that information to the 8751 through one of the spare latch inputs. The motor linked information is used in every communication with the 8748's to prevent the 8751 from waiting indefinitely for responses from 8748's that are not operational.

It should be noted that the motor linked latch is read only once, during the initialization routine executed on power-up. So if motors are to be connected or disconnected, the system power must be shut off.

The motor linked latch is shown in block form in Figure 10 on page 51, and detailed connections are shown in Figure 20 on page 107.

(HARDWARE) THE BAUD RATE

The baud rate can be set to either 4800 or 9600. That is done simply by wiring bit zero of the motor-linked latch to +5-volts for 4800 baud, or to ground for 9600 baud. In order to change the baud rate, system power must be turned off and back on again, since the baud rate is set during the initialization routine.

(SOFTWARE) THE 8748 STATUS FLAGS

Several flags are used by the 8751 to keep track of the status of the various linked 8748's and their motors.

Not Ready for Next Move Flags

In normal operation, the not-ready-for-next-move flags of all linked (operational) motors are set. However, if the 8751 receives code from an 8748 indicating that it is ready for the next move, the flag corresponding to that 8748 is cleared. When the condition occurs that all of the flags are clear, the VAX is notified that the system is ready for the next move, and the flags of all linked motors are reset.

Nothing prevents the 8751 from accepting another move command from the VAX when those flags are set, so the program running on the VAX must also keep track of this status to prevent it overwriting prior move commands before they are executed.

Motor Stalled Flags

A stall occurs when a motor has not moved for one second under at least 50% power. In normal operation, the motor-stalled flags are all clear. However, if the 8751 receives code from an 8748 indicating that its motor is stalled, the flag corresponding to that 8748 is set until the VAX clears the stall condition. The stall condition is cleared by VAX with the Clear Remaining Moves (CRM) command.

Hardware Reset Flags

Hardware reset occurs whenever power is turned off and back on. The significance of a hardware reset is that all data in the internal and shared RAMs of the 8748 are lost. In normal operation, the hardware-reset flags are all clear. However, if the 8751 receives code from an 8748 indicating that it has undergone hardware reset, the flag corresponding to that 8748 is set until the VAX is notified of the hardware reset condition.

APPENDIX M. CONTROL BY NON-LINEAR FEEDBACK

While the motor is in motion, the 8748 functions as a velocity controller, and can be viewed as closing a feedback loop where system input is a velocity set point and system output is the motor velocity. Unlike an ordinary feedback loop, however, it can respond to special situations in a most non-linear manner.

The situation is broken down into various cases, or system states, under which different control algorithms are applied.

1. the motor is not moving and the position error is zero
2. the motor is not moving and the position error is not zero
 - a. initial power has not yet been applied
 - b. the motor did not move under the initial application of power
 - c. the motor did not move under further application of power
3. the motor is moving
 - a. a move command is being executed
 - 1) position error is large
 - 2) position error is small
 - b. all move commands completed

- 1) position error is large
- 2) position error is small
- 3) the position error is zero

Each of these states has significance in terms of velocity and position control, and the 8748 software is designed to recognize them and take the appropriate control action.

Note that state 1 is an equilibrium point, and does not require any action.

State 2 is typical of a start-up situation, and is handled by the motor-stopped subroutine, which is outlined in "The Motor Stopped Subroutine" on page 160.

In state 2a, the position error has just been detected. In that case, the starting pulsewidth, specified from the VAX, is applied.

In state 2b, the motor failed to respond to the initial pulsewidth, indicating that the motor is probably working against a load. In that case, the pulsewidth is increased in direct proportion to the velocity set point.

In state 2c, the motor is not moving even under larger amounts of power. Power is increased again, unless the pulsewidth is over 50% and the motor has not moved for one second, when the stall condition is assumed.

The system is in state 3 whenever there is a motion interrupt. The actions taken are outlined in "The Interrupt Service Subroutine" on page 153. Initially (assuming the system is not halted or stalled), the change in pulsewidth is determined strictly by the coefficient and maximum velocity error specified from VAX for the range in which the velocity set point falls, and by the direction of the acceleration, as described in "Appendix N. Determining the Pulsewidth" on page 94. Afterwards, the substate is determined and other changes are made, if necessary.

In state 3a1, the pulsewidth is not changed any further, since the state should be under velocity control only. In state 3a2, if no further move in the same direction follows the move being executed, then the velocity set point is simply ramped down as the position approaches the position set point. If a further move does follow, the state is treated as state 3a1.

In state 3b1, the long overshoot pulsewidth, specified from the

VAX, is applied in the direction that will correct the error. In addition to that, if the motor motion is in the direction of worsening position error, the corrective pulsewidth is increased in direct proportion to the motor speed. This is a very non-linear response, and it is one reason that overshoot is kept so low.

In state 3b2, the response is the same as for state 3b1, except that the short overshoot pulsewidth is applied, rather than the long overshoot pulsewidth. It, too, is specified from the VAX.

In state 3b3, the response should be a braking pulsewidth. However, in the case where the motor is moving relatively slowly, no response is required. The scheme chosen, and it works well, is to subtract one from the motor speed and use the result as the braking pulsewidth. This works particularly well in avoiding 'jitter' at the final position, since the value of speed assigned just after direction reverses is one; after subtracting one from that speed, zero pulsewidth is applied as braking.

APPENDIX N. DETERMINING THE PULSEWIDTH

The duty cycle of the rectangular pulse train supplying power to the motor is directly proportional to the pulsewidth written to the pulsewidth modulator. (For details of the pulsewidth modulator, see "Appendix O. The Pulsewidth Modulator" on page 98.) This appendix explains how the value of the pulsewidth is obtained under normal velocity feedback control.

When a position error is initially detected, the value which the user has specified as the 'starting pulsewidth' is used as the pulsewidth, and the sign of the position error is used as the pulsewidth sign. After this initial value of pulsewidth is applied to the motor, one of two things will occur: either the motor will move or it will not.

If the motor does not move, then the motor stopped subroutine will detect that exactly one-sixteenth of a second has passed since initial power was applied, and will increment the pulsewidth by the amount of the velocity set point, under the assumption that the lack of response indicates the motor is working against a heavy load. If the motor fails to move after that, then on each successive motor-stopped interrupt, the pulse-

idth is incremented by the amount of the starting pulsewidth, plus the number of interrupts since power was first applied. That process will continue until either the motor moves or the pulsewidth exceeds 50% and the motor has not moved for more than one second under applied power. (The latter case is considered as the stall condition.)

If the motor does move, then on the first motion interrupt after power is applied, there is no way to determine the speed because the clock value is meaningless. The velocity error is set to be zero, since there is no way to determine a good value for it until another move interrupt yields a valid clock count.

On successive motion interrupts, the velocity is determined using the scheme given in "Appendix K. Velocity Bookkeeping in the 8748" on page 79. The velocity error is the velocity minus the velocity set point. The negative of the velocity error is used in the following way to obtain the pulsewidth increment:

1. The error is compared to the user-specified maximum error for the range in which the velocity set point falls, and is set equal to the maximum if it exceeds it (sign is preserved).
2. If the sign of the acceleration indicates that the velocity

is approaching the set point, the velocity error is set to zero.

3. The velocity error is multiplied by the user-specified coefficient for the range in which the velocity set point falls, yielding the pulsewidth increment.
4. If the increment exceeds a magnitude of 127, it is set equal to 127.
5. The increment is added to the pulsewidth.
6. If the new pulsewidth is negative, it is two's complemented and the pulsewidth sign is also complemented.
7. If the new pulsewidth is greater than 127, it is set equal to 127.
8. The user-specified hysteresis value is added to the magnitude of the pulsewidth.
9. If the result exceeds 127, it is set equal to 127.
10. The new pulsewidth and sign are written to the pulsewidth modulator, and to their internal 8748 RAM locations.

Note that when the pulsewidth sign changes, a pulsewidth of zero must be written to the pulsewidth modulator for about 30 microseconds to allow the excited optical isolator and power transistor pair to turn off before exciting the other pair. If both transistors were on at the same time, they would provide a low resistance path from the +12-volt supply to the -12-volt

supply, and would be burned out very quickly by excessive current (refer to Figure 26 on page 113).

The foregoing scheme for updating the pulsewidth does not hold for the special cases, such as overshoot and undershoot. They are explained in "Appendix M. Control by Non-Linear Feedback" on page 90.

APPENDIX O. THE PULSEWIDTH MODULATOR

The pulsewidth modulator is based on a very simple scheme. Referring to Figure 15 on page 100, the pulsewidth (duty cycle) is specified by a number from 0 to 127, which is latched into the pulsewidth latch from the 8748.

That magnitude is constantly compared to the magnitude of a counter which counts repetitively from 0 to 127. As long as the value in the latch exceeds the increasing number in the counter, power is applied to the motor. When the counter value equals or exceeds the pulsewidth latch value, power to the motor is cutoff.

The result is a rectangular wave, or pulse train, of power to the motor with constant period, P , which is the time it takes the counter to count from 0 to 127 (about 2^{-8} second).

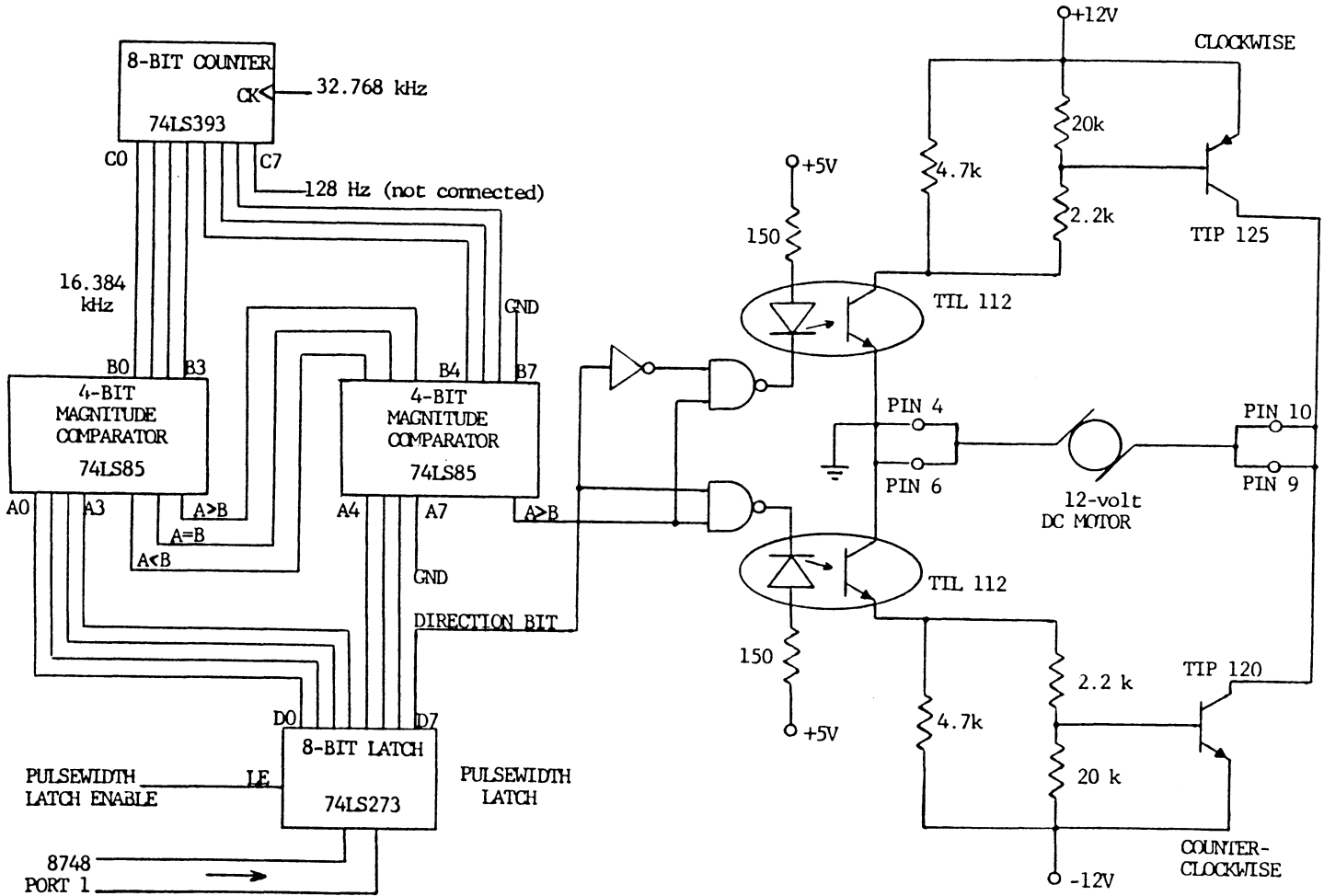
The rectangular output of the 7-bit comparison circuit is gated to one of two optical isolators by the pulsewidth sign bit, which is the eighth bit of the pulsewidth data, latched from the 8748. Each optical isolator is connected so that when it is turned on, biasing is applied to the base of the associated

power transistor, driving that transistor into saturation.

The power transistors are a complementary pair, with the PNP TIP-125 providing power for clockwise motor motion and the NPN TIP-120 providing power for counterclockwise motion.

Complete details of the pulsewidth modulator are presented in the schematic diagram, Figure 26 on page 113.

Figure 15. Block diagram of the pulswidth modulator.



APPENDIX P. ALLOCATION OF RANDOM ACCESS MEMORY

The 8748 RAM, aside from being somewhat small, has a fairly difficult access scheme. Most of it can only be addressed indirectly, which quickly increases the number of program steps in even the simplest procedures. The 8748 program was written 'around' the RAM access problem. That accounts for the peculiar arrangement of the RAM allocation in the 8748, which is shown in Figure 16 on page 102.

The shared RAM allocations were made based on the same considerations, namely, how to allow access by the 8748 from its various routines in the smallest number of program steps (and, thus, the shortest amount of time as well). The result is that the shared RAM allocation is nearly identical to that of the 8748 internal RAM. Allocation of the shared RAM is shown in Figure 17 on page 103.

The 8751, having far more flexible addressing capability than the 8748, was open to a more logical allocation of internal RAM. That allocation is shown in Figure 18 on page 104.

CHANGE IN VELOCITY	(63)	
USER-SPECIFIED CONTROL VARIABLES	(56-61)	
PULSEWIDTH MAGNITUDE AND SIGN	(54-55)	
PRESENT MOVE VELOCITY, MAGINTUDE AND SIGN	(50-53)	
NEXT MOVE FLAGS AND NEXT MOVE VELOCITY, MAGNITUDE, AND SIGN	(44-49)	
FRACTIONAL (QUARTER-HOLE) POSITION ERROR	(43)	
SPEED	(42)	
PEEK/POKE ADDRESS	(41)	
MOTOR STOPPED INTERRUPT COUNT	(40)	
COEFFICIENTS AND MAXIMUM MAGNITUDES	(32-39)	
ENCODER BIT DATA AND MOTION FLAGS (R6, R7)	(30-31)	REGISTER BANK 1
VELOCITY SET POINT (R5)	(29)	
WORK REGISTERS (R3, R4)	(27-28)	
QUARTER-HOLE POSITION ERROR (R2)	(26)	
ADDRESS POINTERS (R0, R1)	(24-25)	
STACK	(8-23)	
WRITE BUFFER (R7)	(7)	
PREVIOUS WRITE DATA (R6)	(6)	
WORK REGISTERS (R0-R5)	(0-5)	

Figure 16. Allocation of 8748 internal RAM.

UNASSIGNED	(62-1023)
USER-SPECIFIED VALUES FOR CONTROL VARIABLES	(56-61)
UNASSIGNED	(53-55)
PRESENT ABSOLUTE POSITION OF MOTOR	(51-52)
UNASSIGNED	(50)
NEXT MOVE FLAGS AND NEXT MOVE VELOCITY, MAGNITUDE, AND SIGN	(44-49)
UNASSIGNED	(43)
PRESENT MOTOR VELOCITY	(42)
8748 ADDRESS TO BE PEEKED OR POKED	(41)
DATA PASSING LOCATION FOR 8748 PEEK/POKE	(40)
COEFFICIENTS AND MAXIMUM MAGNITUDES	(32-39)
UNASSIGNED	(0-31)

Figure 17. Allocation of shared RAM.

STACK	(80-127)
WRITE DATA BUFFER (TO VAX)	(64-79)
VAX COMMUNICATION FLAGS AND DATA	(56-63)
PREVIOUS COMMAND DATA	(48-55)
COMMAND DATA	(44-47)
RHINO CLOCK	(42-43)
8748 ADDRESSING DATA	(36-41)
8748 STATUS FLAGS	(32-35)
READ DATA BUFFER (FROM VAX)	(16-31)
REGISTER BANK 1	(8-15)
REGISTER BANK 0	(0-7)

Figure 18. Allocation of 8751 internal RAM.

APPENDIX Q. SYSTEM SCHEMATIC DIAGRAMS.

The complete system schematics are given in this appendix. An attempt was made to have the schematics correspond one-to-one with the block diagrams in the other appendices. This was managed for the most part, but the major exceptions are the schematics in Figure 20 on page 107 and Figure 22 on page 109, which, taken together, correspond to Figure 9 on page 50 and Figure 10 on page 51.

Also, there is no block diagram corresponding to Figure 19 on page 106, or Figure 27 on page 114.

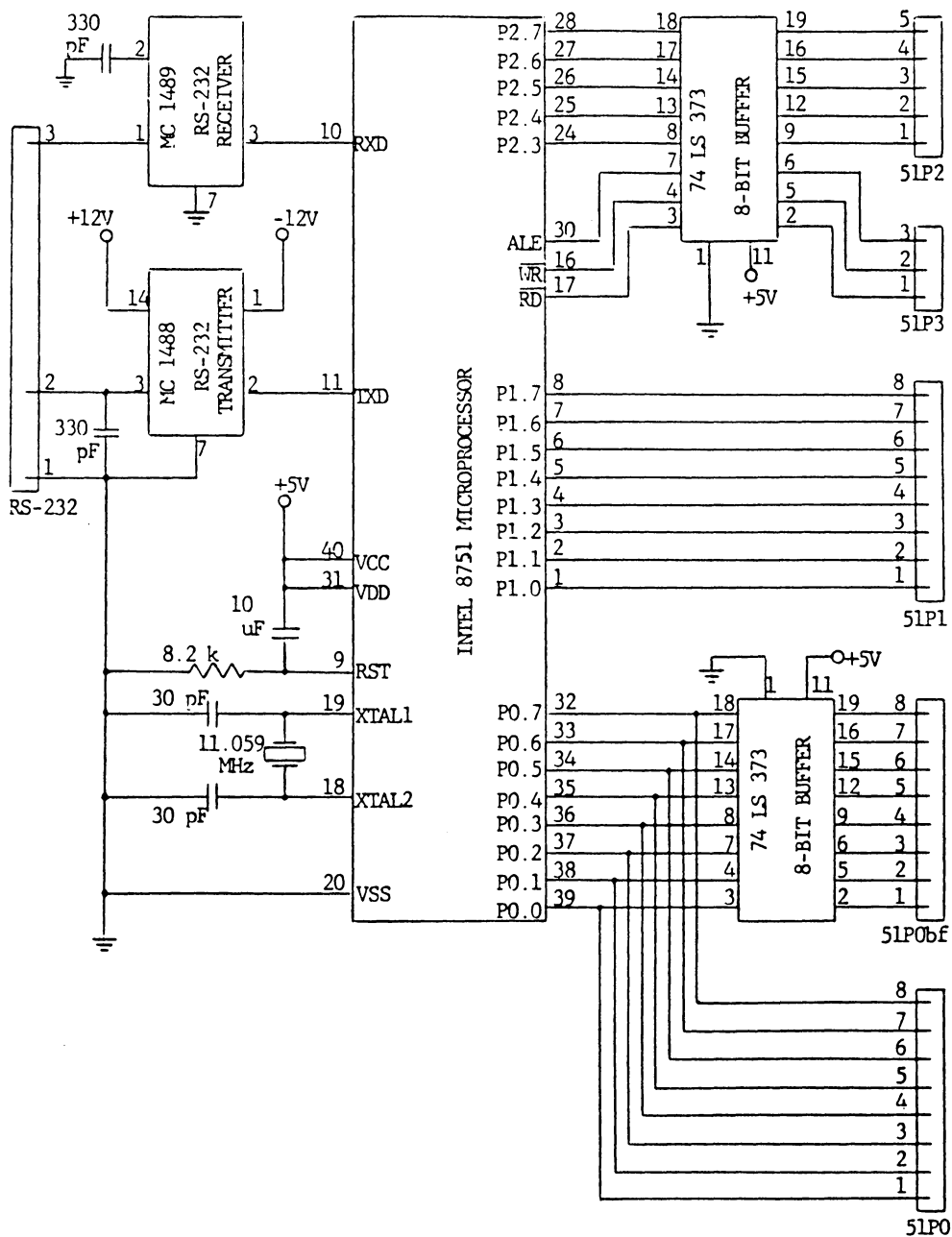


Figure 19. Connections to the Intel 8751 microprocessor.

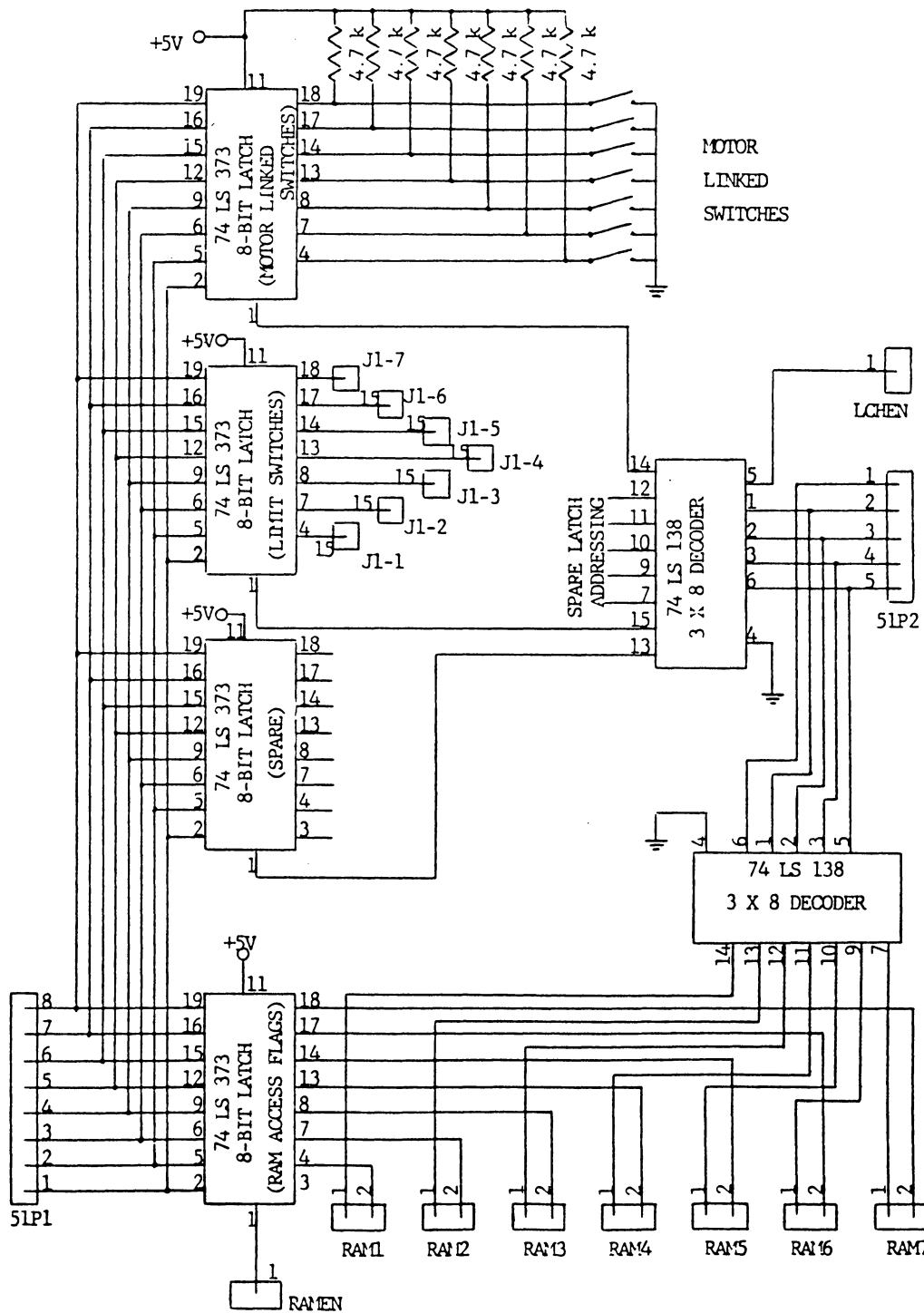


Figure 20. Connections for 8751 shared RAM enables, flag latches, and extra latches.

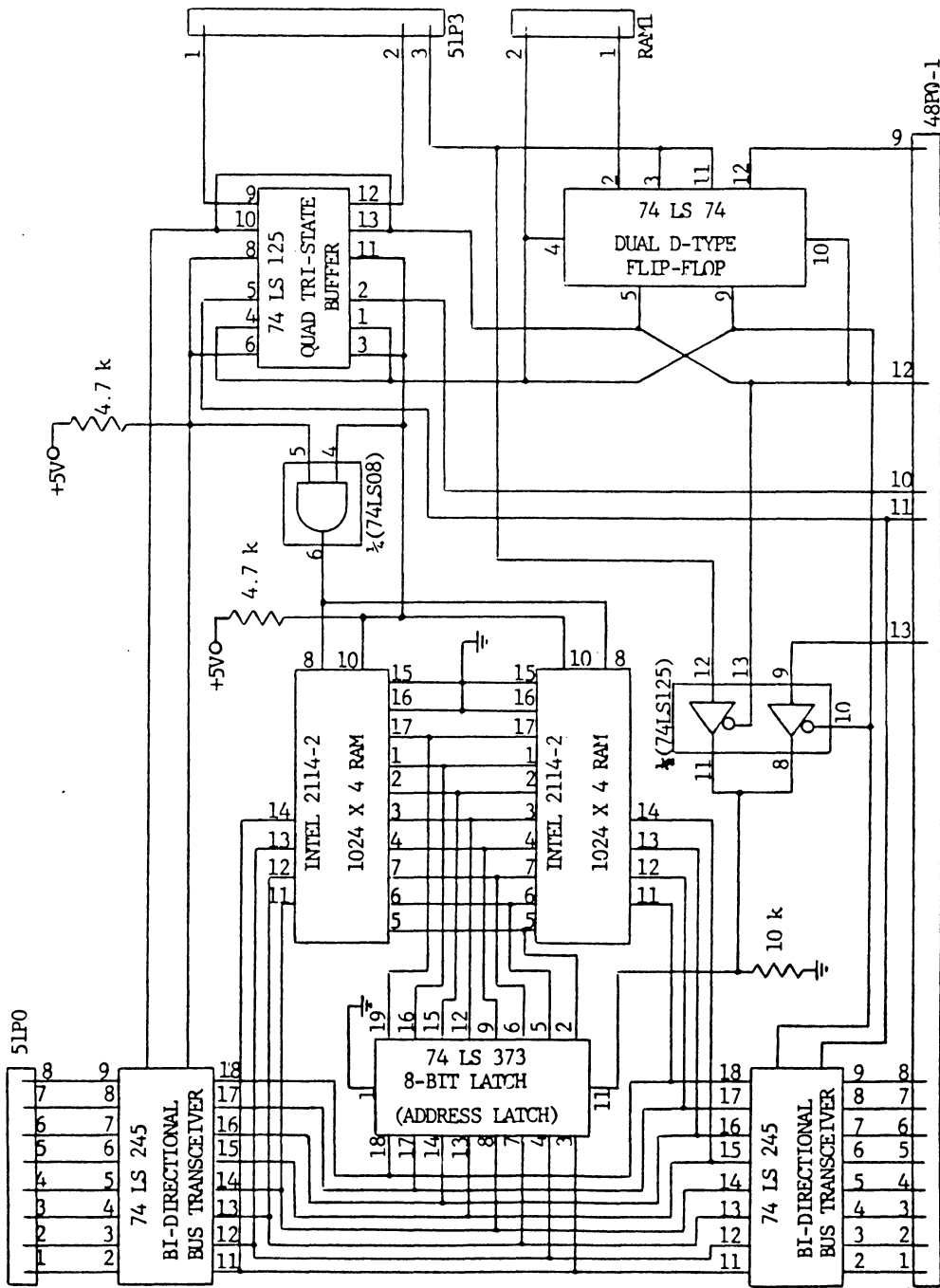


Figure 21. Connections to the shared RAM.

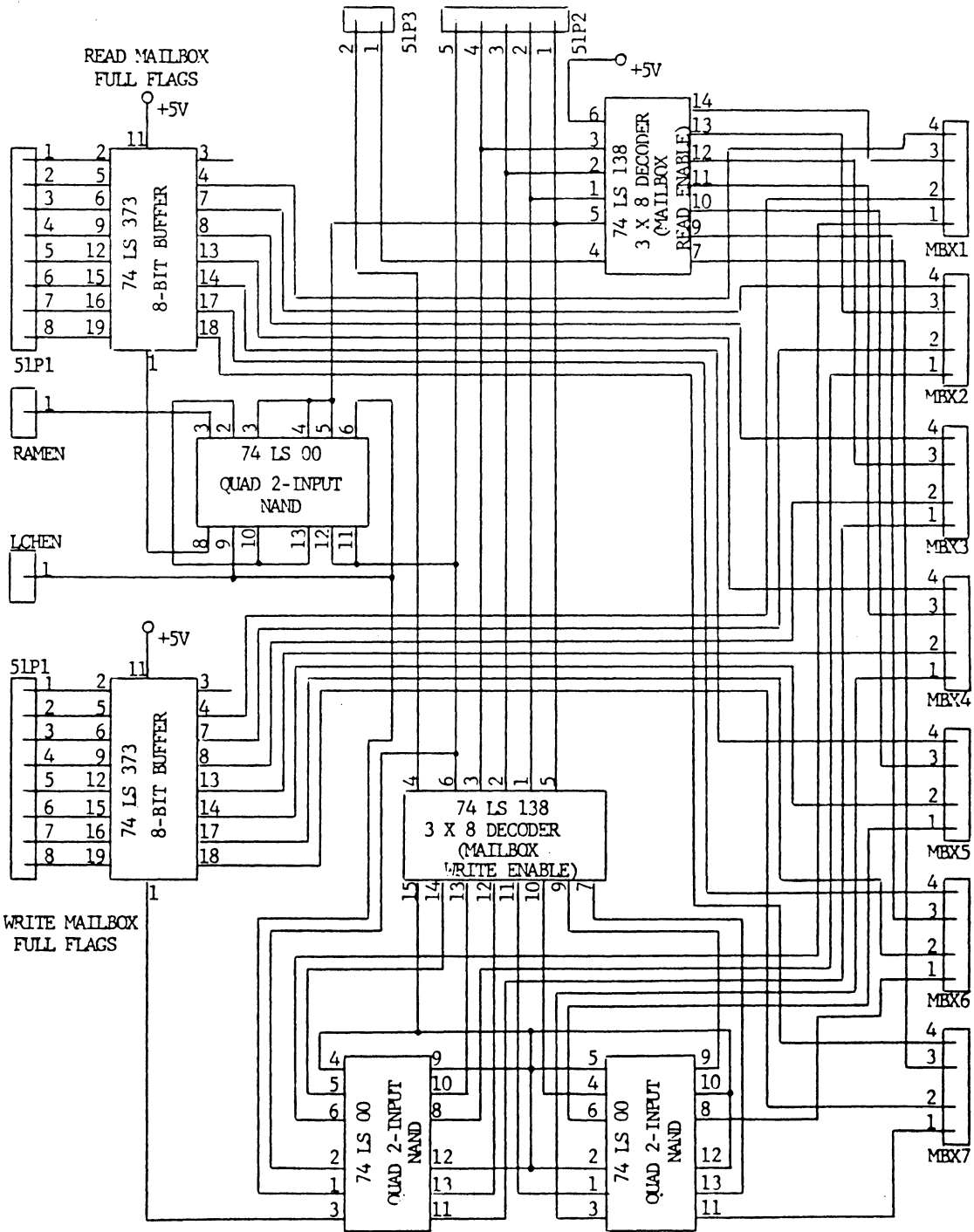


Figure 22. Connections for the 8751 mailbox enables and flag latches.

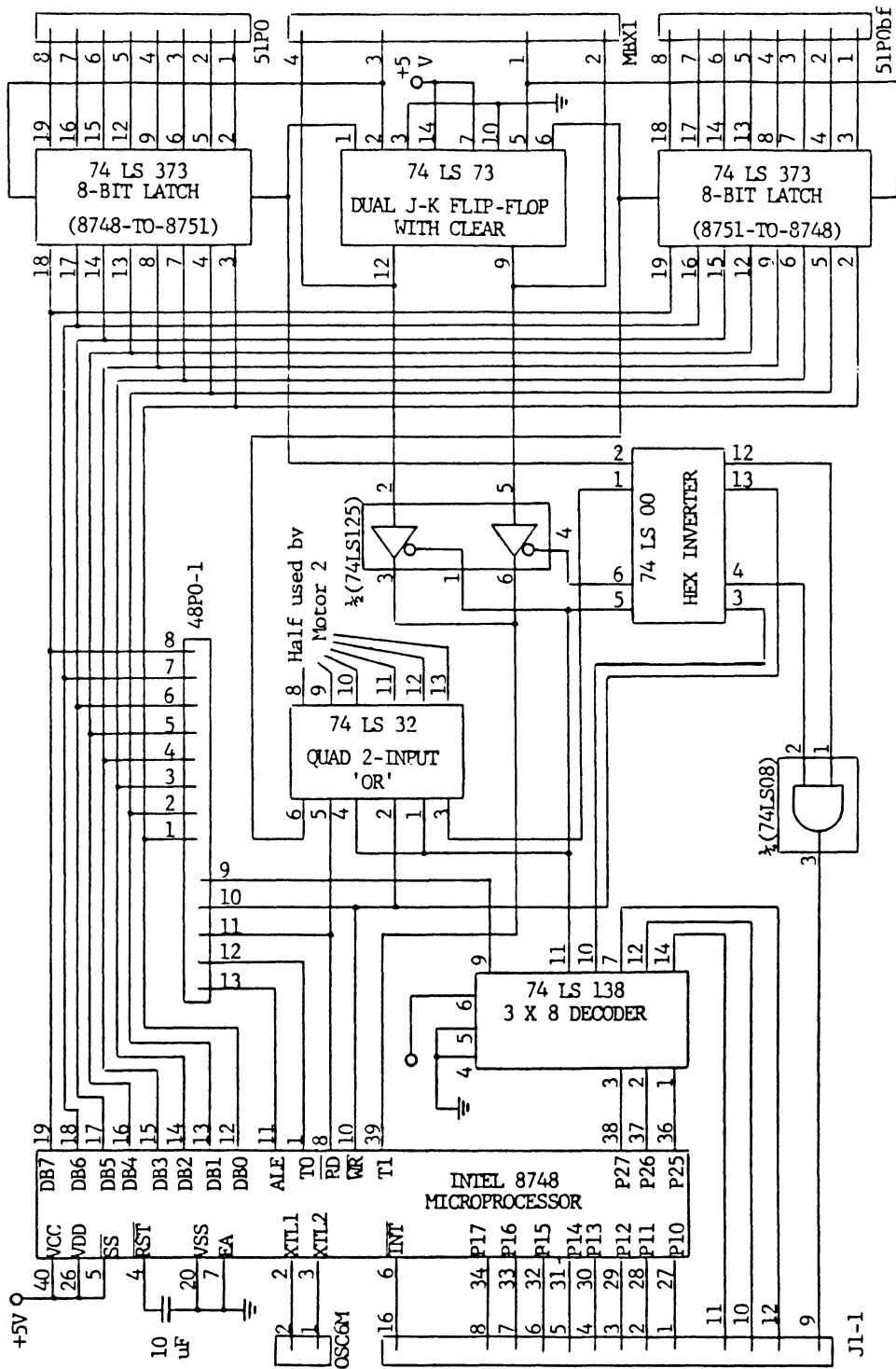


Figure 23. Connections to the Intel 8748, its mailbox, and device selection.

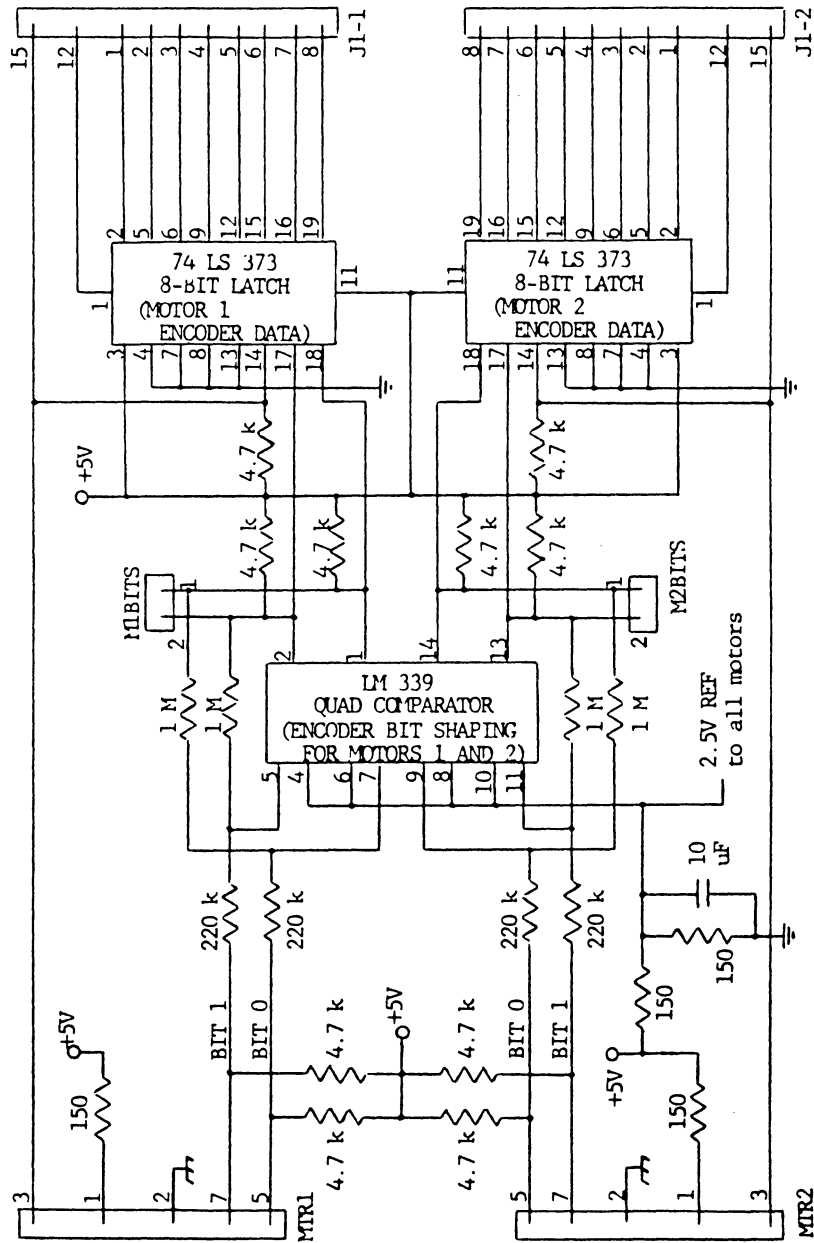


Figure 24. Connections for encoder bit shaping and data latching.

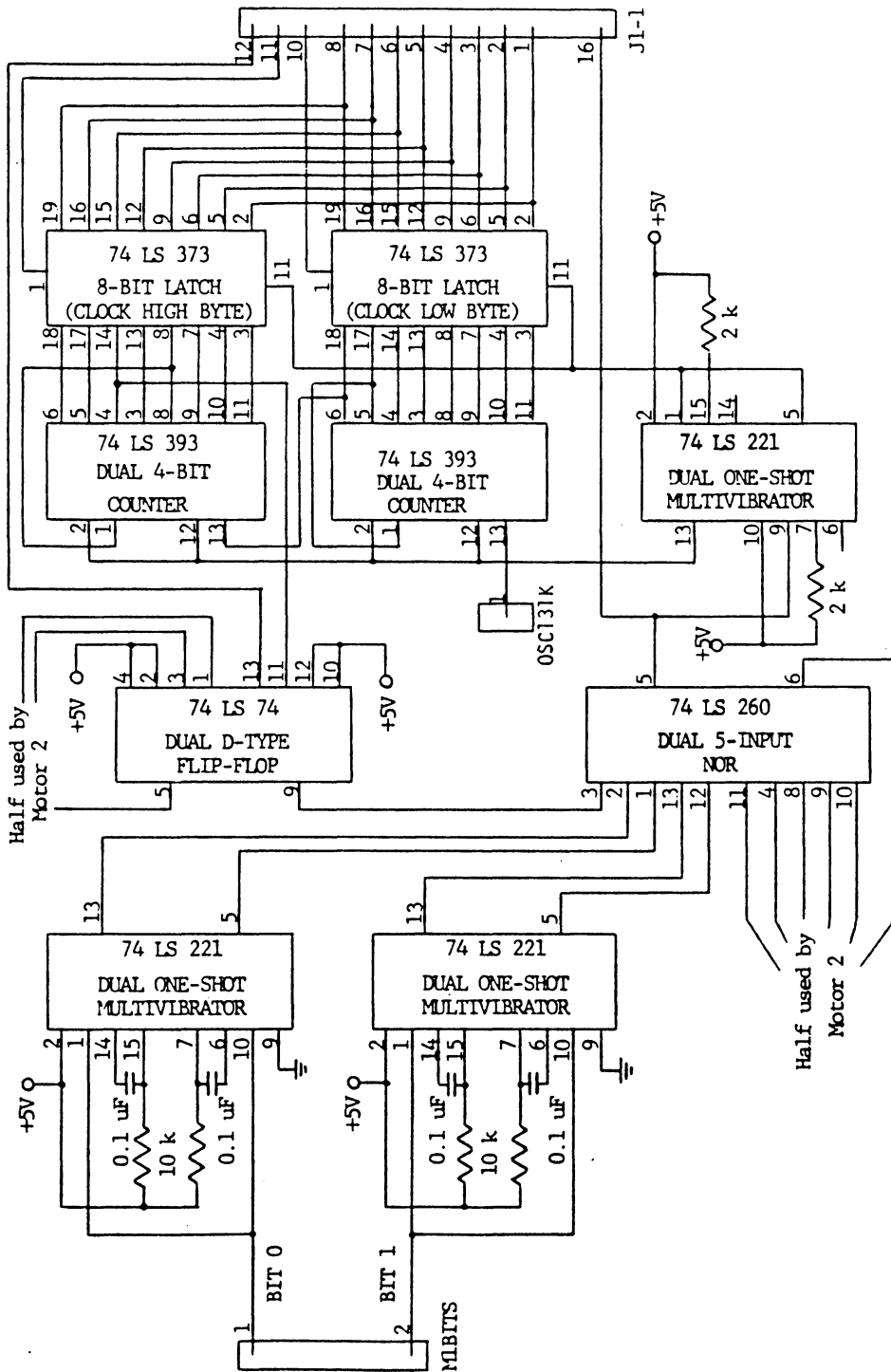


Figure 25. Connections for interrupt generation and interrupt clocking.

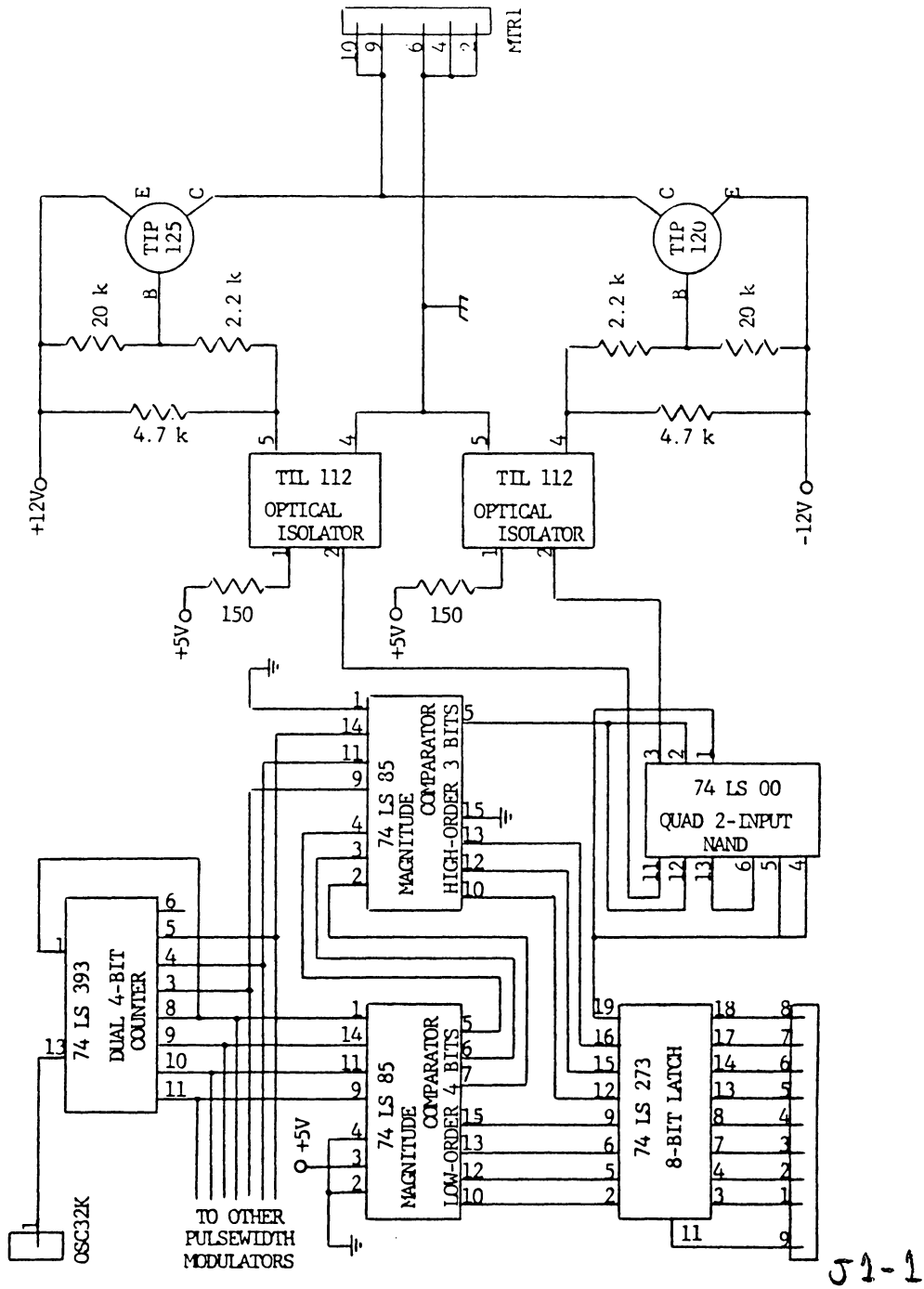


Figure 26. Connections for the Motor 1 pulswidth modulator.

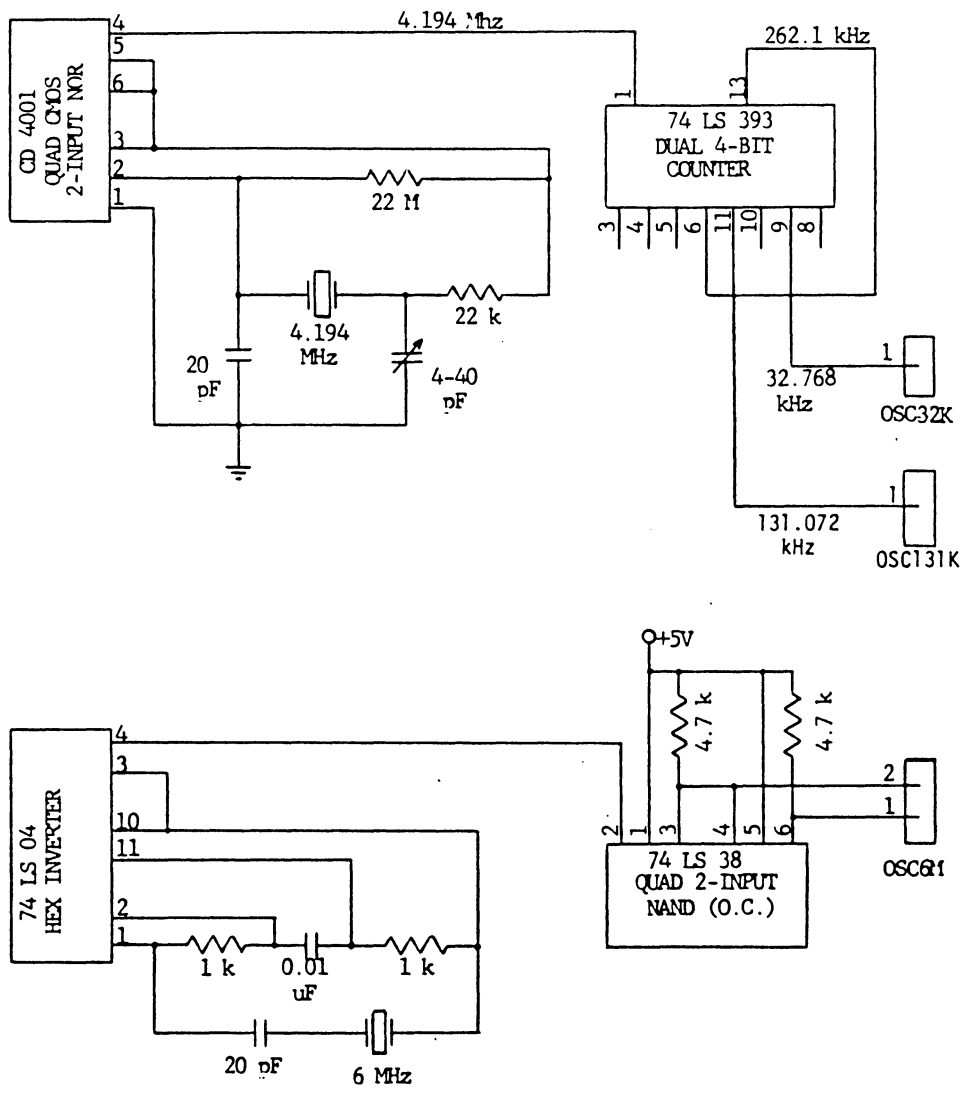


Figure 27. Oscillators for the 8748's (6 MHz) and interrupt clock (32 kHz).

APPENDIX R. A SPECIAL CASE: THE GRIPPER MOTOR

The program for gripper motor control differs somewhat from the program for the other motors. The main difference is that velocity control is disabled. Velocity control is both unnecessary and undesirable for the gripper.

If the gripper motor had velocity control, then when it closed on an object more and more power would be applied in an attempt to maintain the set point velocity. That might damage the object. A more appropriate program would be set up to sense the moment of contact and apply some designated amount of gripping power to the motor.

The point of contact is sensed by a method similar to that used to sense motor stalling in the other program. If the motor does not move for more than 1/8 second under application of the specified closing power, then it is assumed that the jaws are closed on some object (or completely closed). In that case, the user-specified gripping power is applied to the motor.

If the motor moves beyond a small amount after contact is made, power is discontinued. It is assumed that the motor moves

after making contact only if the object is deforming or slipping, or if contact has been lost. The discontinuation of power is designed to prevent damage.

In the program for the gripper, the user specifies several parameters.

- the power to be applied during the opening or closing of the gripper 'jaw' (0 to 63),
- the hysteresis (minimum non-zero) power during opening or closing,
- the gripping power (applied after contact is made) (0 to 63), and
- the overshoot (undershoot) correction power.

Another difference is that all position data locations are kept in terms of quarter-holes. That simplifies the bookkeeping tasks and maximizes position resolution and repeatability.

When a move is commanded, the gripper motor will move all the way to the new position or to a point of contact, whichever occurs first. In either case, the position error is set to zero where motion stops. Thus, a very long move can be specified if it is desired to have the jaws close on an object, and the part

of the move left after contact is made is simply deleted.

The program used is not specified in detail due to the fact that it is identical in most respects to the other program, and due to space limitations.

APPENDIX S. SAMPLE VAX PROGRAM (PASCAL)

This program was created specifically to aid in the development and debugging of the new controller. It is useful in making the robot run, and for helping anyone interested to see one way the bookkeeping and communication tasks can be accomplished. It is written in PASCAL primarily because of the availability of the 'case' statement in that language.

Some people claim that PASCAL is self-documenting. Indeed, the freedom of choice in naming procedures, and the unrestricted use of indentation are tremendous aids in making a program understandable. For that reason, a detailed outline was not considered necessary. A brief outline is given at the end of this appendix, and the complete program listing is given in "Appendix V. Listing of the Sample Program on VAX" on page 170.

In order to fully understand this program, one must study the communication protocol and the communication subroutines in the 8751 assembly language program thoroughly. In fact, the sole function of this program is to translate the user's commands into a format that fits the protocol, and to provide the inverse operation on communication and data from the 8751.

Some would say it makes the Rhino robot user-friendly.

Before using this program, one would do well to understand the function of the following command entries:

- '?' : This command causes the menu of valid commands to be displayed to the user, so it acts like a help command.
- 'x' : This command acts like an escape character. It is followed immediately on the command line by a number from 0 to 255 that will be sent directly to the Intel 8751. Essentially, 'x' disables all the prompting and formatting procedures of the program and allows the user to send codes directly to the 8751.
- 'f' : This command allows the user to change the value of three Boolean flags used in the program:
 - The auto-respond flag is the complement of the 'x' command. If it is cleared, all of the automatic response features of the program are disabled so codes and data from the 8751 are displayed exactly as they are received, with no translation or formatting, and no prompting of the 8751.
 - The ready flag is set whenever a 'ready for next move' code (RDYNXT) is received, and is cleared whenever a 'move' command (MOV) is transmitted. A move command

will not be processed if this flag is not set. It is initially set.

- The go flag is set whenever the 'go' command (AGO) is transmitted, and is cleared whenever the 'halt' command (HLT) or the 'motor stalled' command (MTRSTL) is received. It is initially cleared.
- 'z' : This command causes program execution to end.

When a command mnemonic is entered (only the first letter is required), the program will prompt the user for all the data that must accompany the command. The entire communication sequence, including formatting of the data, is then carried out according to the protocol for the particular command, with no further effort on the part of the user.

If the 'auto-respond' flag is set, then all communications originating in the 8751 are also handled automatically. Notice of the communication (and its meaning) is displayed to the user.

Thus, the program allows the user to control the Rhino robot from a keyboard with simple command mnemonics and data entries.

A brief outline of the sample VAX program follows.

Variables and Constants

1. Define the nonstandard types for variables.
2. Declare the program variables and their types.
3. Declare the program constants.

External Procedures

1. The Rhino Read procedure looks for 8-bit input from both the Rhino (Intel 8751) and the keyboard.
2. The Rhino Write procedure writes 8-bit codes to the Rhino (Intel 8751).

Internal Procedures

1. The Read Two RS/232 Devices procedure assigns the correct device address to the Rhino and calls the external 'rhino read' procedure.
2. The Get Response procedure waits for an expected code from the Rhino, and interprets any code arriving before the

expected code.

3. The Get Data procedure prompts the Rhino for data and waits for the appropriate number of data bytes to be received (it also formats the received data).
4. The Get Screen Data procedure prompts the user for the appropriate data to accompany to command entered by the user, and formats them for transmission to the Intel 8751.
5. The Get All Data procedure sends a command to the Rhino which will elicit data, then uses the Get Data procedure to properly handle the data when the Rhino has it ready to transmit.
6. The Display 8751 Data procedure is used to display data returned from an 8751 peek command.
7. The Display 8748 Data procedure is used to display data returned from an 8748 peek command.
8. The Display Shared RAM Data procedure is used to display data returned from a shared ram peek command.

9. The Display Velocities procedure is used to display data returned from a velocity request.
10. The Display Positions procedure is used to display data returned from a position request.
11. The Send Command Get Echo procedure is used to send commands to the 8751 when the only expected response is an 'echo' of the same code (for example, the 'halt' command).
12. The Send 8748 Data procedure is used to send the last two bytes of data for an 8748 'poke' command.
13. The Send Moves procedure is used to send the move and velocity data to the 8751 for a 'move' command.
14. The Load Coefficients procedure is used to send the data accompanying a 'coefficient' command to the 8751.
15. The Enable C-O-I procedure is used to send the command code and data for the 'enable command-on-interrupt' command.
16. The Code From 8751 procedure is used to decode and respond to incoming code from the Intel 8751.

17. The Keyboard Command procedure is used to interpret the command entered by the user from the keyboard, and to take appropriate action to implement that command.
18. The User Help procedure is used to display to the user the menu of valid commands that can be entered from the keyboard.
19. The Change Flags procedure allows the user to alter the values (TRUE or FALSE) of the three Boolean flags in the VAX program from the keyboard.

The Main Program

1. Prompt for command and data input from the user, and call the appropriate procedures based on the input.
2. Monitor input from the Rhino (Intel 8751 serial port), indicating to the user when it occurs, what it means, and what actions have been or should be taken in response.

APPENDIX T. 8751 ASSEMBLY LANGUAGE PROGRAM OUTLINE

THE INITIALIZATION ROUTINE

The initialization routine is executed on power up.

1. Put the 'no operation' code in all mailboxes.
2. Clear internal RAM locations zero through 127.
3. Put the data byte from the 'motor linked' latch in the motor link location in internal RAM.
4. Wait for a 'hardware reset' code from every linked motor.
5. Initialize the stack pointer to just below the bottom of the stack area of internal RAM.
6. Set up the serial port for communication with VAX.
 - a. Set the serial port mode for a ten-bit frame with no parity bit (this is called Mode 1).
 - b. Set up Timer 1 to generate 9600 baud.
 - c. Clear the serial port transmit and receive interrupt flags.
 - d. Set the serial port interrupt priority to the highest level.
7. Put the 'hardware reset' code into the serial port write buffer.

8. Initialize the Rhino Clock to unity (this clock counts the number of times external interrupt zero occurs).
9. Set interrupt zero to the positive-edge-triggered mode (this interrupt increments the Rhino Clock and causes execution of the command-on-interrupt code).
10. Enable the serial port interrupt and interrupt zero.
11. Start the main routine.

8751 MAIN PROGRAM

The main routine monitors communication from the 8748 mailboxes and the VAX, and responds appropriately to commands from any of them.

1. If any 'read mailbox full' flag is set, call the respond-to-8748 subroutine.
2. Check the various **8748 status flags**.
 - a. If the peek data ready flag of every linked motor is set, then all the peek data is ready to send to the VAX.
 - 1) Clear the peek data ready flags.
 - 2) Read 1 byte of peek data in from each of the seven shared RAM's to the write buffer, with the Motor 1

data at the bottom of the buffer.

- 3) Above the peek data in the write buffer put the address from which the data was obtained in the 8748's.
 - 4) Above the address put the low and high byte of the Rhino Clock.
 - 5) Finally, above the clock data, put the '8748 peek' code to indicate to VAX which peek command is being answered.
 - 6) Put the 'peek data ready' code in the response code buffer.
 - 7) Load the number 11 as the pending number of data bytes to transmit (i.e., into NTBUFF).
 - 8) Call the write-to-VAX subroutine.
 - 9) Restart the main routine.
- b. If any 8748 hardware reset flag is set, then several steps are taken.
- 1) Clear the 8748 hardware reset flags.
 - 2) Put the 'hardware reset' code in the response code buffer.
 - 3) Call the write-to-VAX subroutine.
 - 4) Restart the main routine.
- c. If any 8748 motor stalled flag is set, then several steps are taken.

- 1) If the 'new stall' flag is set, then a stall has just occurred.
 - a) Reset the 'new stall' flag.
 - b) Put the 'motor stalled' code in the response code buffer.
 - c) Call the write-to-VAX subroutine.
- 2) If the VAX command is 'no operation' (i.e., cleared), then move in the contents of the read command buffer to the VAX command location, and clear the buffer.
- 3) The VAX command must be executable during a stall.
 - a) If the command is either 'go' or 'move', then it must not be executed, since at least one motor is stalled.
 - i. Replace the VAX command by the 'halt' command.
 - ii. Put the 'motor stalled' code in the response code buffer.
 - iii. Call the write-to-VAX subroutine.
 - b) Call the decode-VAX-command subroutine.
- 4) If no data is to be transmitted or received (that is, if NT, NTBUFF, NR, and NRBUFF are zero), then check for an interrupt command.
 - a) Move the contents of the interrupt command

buffer to the VAX command location, and clear the buffer.

b) Call the decode-VAX-command subroutine.

5) Restart the main routine.

d. If the not ready for next move flags are all clear, then the system is ready for the next move.

1) Reset the 'not ready for next move' flags of all linked motors.

2) Put the 'ready for next move' code in the serial port write buffer.

3) Call the write-to-VAX subroutine.

3. If no transmit data remains in the write buffer (that is, if NT is zero) then check for a VAX command.

a. If the VAX command is 'no operation', then move the contents of the read command buffer to the VAX command location, and clear the buffer.

b. Call the decode-VAX-command subroutine.

4. If there is no data to be transmitted or received (that is, if NT, NTBUFF, NR, and NRBUFF are zero), then check for an interrupt command.

a. Move the contents of the interrupt command buffer into the VAX command location, and clear the buffer.

b. Call the decode-VAX-command subroutine.

5. Restart the main routine.

THE RESPOND TO 8748 SUBROUTINE

The respond-to-8748-mailbox subroutine checks each motor's read mailbox individually, starting with motor seven.

1. If the motor's 'read mailbox full' flag is set, then enable the motor's read mailbox.
 - a. Read in the command code from the 8748 read mailbox.
 - b. Call the decode-8748-command subroutine.
2. Return from the respond-to-8748-mailbox subroutine.

THE DECODE 8748 COMMAND SUBROUTINE

The decode-8748-command subroutine determines the appropriate response to a command from an Intel 8748.

1. If the command is not 'no operation', then several steps are taken.
 - a. Enable the motor's write mailbox.
 - b. If the code is not valid, request a resend of the command.
 - c. If the code is valid, then decode the command.

- 1) If the command is send previous code over again, then put the contents of the motor's previous code location into the motor's write mailbox, and clear the previous code location.
 - 2) If the command is motor stalled, then several steps are taken.
 - a) Set the motor's 'stall' flag.
 - b) Set the 'new stall' flag.
 - c) Put the 'halt' code in all motors' write mailboxes.
 - 3) If the command is hardware reset, then several steps are taken.
 - a) Set the motor's 'hardware reset' flag.
 - b) Put the 'halt' code in all motors' write mailboxes.
 - 4) If the command is ready for next move, then clear the motor's 'not ready for next move' flag.
 - 5) If command is peek data ready, then set the motor's 'peek data ready' flag.
2. Return from the decode-8748-command subroutine.

THE WRITE TO VAX SUBROUTINE

The write-to-VAX subroutine transmits the command in the response code buffer.

1. If the 'transmitter idle' flag is set, then call the serial-output subroutine.
2. If the 'transmitter idle' flag is clear, wait for one of the following two occurrences.
 - a. If the 'transmitter idle' flag becomes set, then call the serial-output subroutine.
 - b. If the response code buffer is cleared, then the response code was transmitted from the serial-port-interrupt-service subroutine.
3. Return from the write-to-VAX subroutine.

THE SERIAL OUTPUT SUBROUTINE

The serial-output subroutine puts the appropriate data byte into the transmit serial port buffer.

1. Clear the 'transmitter idle' flag.

2. If there is data to transmit (that is, if NT is not zero), then several steps are taken.
 - a. Compute the location of the data byte to transmit.
 - b. Move the byte from that location to the serial port transmit buffer.
 - c. Decrement the data byte counter, NT.
 - d. Set the previous write to VAX location equal to one to indicate 'no operation'.
 - e. Return from the serial-output subroutine.
3. If there is no data to transmit, then check for a command to transmit.
 - a. If the write code buffer is not zero, then its contents must be transmitted.
 - b. If the write code buffer is zero, then check the response code location.
 - 1) If the code is not equal to zero, then put it directly into the write code buffer.
 - 2) If the code is equal to zero, and the 'request data from VAX' flag is set, then several steps are taken.
 - a) Put the 'send data to 8751' code into the write code buffer.
 - b) Move the contents of NRBUFF to NR (update the current number of data bytes to transmit).

- c) Put the 'send data to 8751' code in the previous write to VAX location.
- 3) Clear the response code buffer.
- c. If the write code buffer is not zero, then its contents must be transmitted.
 - 1) If the code equals one, then put the 'no operation' code into the seial port transmitter buffer.
 - 2) If the code is not equal to one or to zero, then put it directly into the serial port transmitter buffer.
 - 3) If the code is zero, do not transmit it, and reset the 'transmitter idle' flag.
 - 4) Clear the write code buffer location.
- d. Return from the serial-output subroutine.

THE DECODE VAX COMMAND SUBROUTINE

The decode-VAX-command subroutine executes the appropriate response to a command from the VAX.

- 1. If the command is no operation, no action is taken.
- 2. If the code is not valid, then several steps are taken.

- a. If the previous code to VAX was one which required the 'send data' response from VAX, then the VAX may be expecting data to be sent, so that a resend request would be seen as data.
 - 1) Send a string of 16 zero bytes to VAX to indicate a data communication fault.
 - 2) Put unity in the response code buffer to indicate 'no operation' should be sent to VAX.
 - b. If the previous code to VAX did not require the 'send data' response from VAX, then put the 'send previous command over again' code in the response buffer.
3. If the command is enable command-on-interrupt, then several steps are taken.
- a. If the command to be executed on interrupt zero is not one of the four commands allowed for that purpose, then put the 'invalid data' code into the response code buffer.
 - b. If the command is allowable on interrupt, then move it to the interrupt command location and put the 'received data' code in the response code buffer.
4. If the command is disable command-on-interrupt, clear the interrupt command location.
5. If the command is 8748 peek/poke then several steps are taken.

- a. If the high bit of the address to peek/poke is set, then the desired operation is a poke.
 - 1) Request more data from the VAX (the motor number for the poke operation and the data byte to be poked).
 - 2) Wait for the data to be received from the VAX.
 - 3) Obtain access to the shared RAM of the 8748 to be poked.
 - 4) Put the address and the data byte in their locations there.
 - 5) Enable that motor's write mailbox.
 - 6) Wait for the write mailbox full flag to be clear.
 - a) If the write mailbox is full, check that motor's read mailbox.
 - b) If the read mailbox is full, call the decode-8748-command subroutine.
 - 7) Put the '8748 peek/poke' command code into the write mailbox.
 - 8) Put the 'received data' code into the response code buffer.
- b. If the high bit of the peek/poke address is clear, then the desired operation is a peek.
 - 1) Gain access to each shared RAM individually, and write the address of the peek in its location in

shared RAM.

- 2) After all shared RAM's have the peek address loaded, set the '8748 peek in progress' flag (bit zero of the byte containing the 'peek data ready' flags).
 - 3) Call the global-write subroutine to write the '8748 peek/poke' command into all write mailboxes.
 - 4) Clear the response code buffer (the main routine concatenates the 8748 peek data when it is ready).
 - 5) Return from the decode-VAX-command subroutine.
6. If the command is 8751 peek then several steps are taken.
- a. If the high bit of the address of the peek is set, then one of the external latches is to be read.
 - 1) Put the address out on Port 2 to enable the appropriate latch output.
 - 2) Read the latch output in from Port 1 to the bottom of the write buffer.
 - b. If the high bit of the address of the peek is clear, then one of the internal RAM addresses is to be read.
 - 1) Put the address into an address pointer.
 - 2) Read the internal RAM address by indirect addressing and put the data in the bottom of the write buffer.
 - c. Above the data in the write buffer, put the address

from which it was read, the low and high bytes of the Rhino Clock, and the '8751 peek' code.

- d. Set the pending number of data bytes for transmission to five.
 - e. Put the 'peek data ready' code in the response code buffer.
7. If the command is velocity request, then several steps are taken.
- a. Gain access to the shared RAM of each motor, individually, and move in the velocity data to the write buffer (Motor 1 data at the bottom of the buffer).
 - b. Above the data in the write buffer, put the low and high bytes of the Rhino Clock.
 - c. Set the pending number of data bytes to transmit (NTBUFF) to nine.
 - d. Put the 'velocity data ready' code in the response code buffer.
8. If the command is absolute position request, then several steps are taken.
- a. Gain access to the shared RAM of each motor, individually, and move in the low and high bytes of position data to the write buffer (Motor 1 data at the bottom of the buffer).
 - b. Above the data in the write buffer, put the low and

high bytes of the Rhino Clock.

- c. Set the pending number of data bytes to transmit (NTBUFF) to sixteen.
 - d. Put the 'position data ready' code in the response code buffer.
9. If the command is send data to VAX, then just return, since that should never reach this level in the program (it should be intercepted by the serial-port-interrupt-service subroutine).
10. If the command is send previous code over again, then two steps are taken.
- a. Move the contents of the previous write to VAX location to the response code buffer.
 - b. Set the previous write to VAX location to unity, indicating a 'no operation' code.
11. If the command is clear remaining moves, then several steps are taken.
- a. Clear the '8748 motor stalled' flags.
 - b. Call the global-write subroutine to put the 'clear remaining moves' code in all write mailboxes.
 - c. Put the 'cleared remaining moves' code in the response code buffer.
12. If the command is move, then several steps are taken.
- a. If no motors are linked, then put 'ready for next move'

- code in the response code buffer.
- b. If at least one motor is linked, then gain access to each shared RAM, individually.
 - 1) For the particular motor, if the move is zero, clear the 'next move received' flag in shared RAM, and clear the motor's 'not ready for next move' flag in 8751 internal RAM.
 - 2) Strip off the sign bit (bit 15) of the move and write it to the 'move sign' location in shared RAM.
 - 3) For the particular motor, if the move exceeds 31, then set the 'infinite move' flag in shared RAM.
 - 4) Put the unsigned two byte move in its locations in shared RAM.
 - c. Set the receive data pending buffer to seven (for seven bytes of velocity data).
 - d. Set the 'request data' flag.
 - e. Call the write-to-VAX subroutine to transmit the 'send data to 8751' code to the VAX.
 - f. Wait until all seven bytes of velocity data have been received from the VAX.
 - g. Move the velocity data from the read buffer to the shared RAM velocity location for each motor.
 - h. Call the global-write subroutine to put the 'move' command in all of the write mailboxes.

- i. Put the 'received data' code into the response code location.
13. If the command is halt, then two steps are taken.
 - a. Call the global-write subroutine to pass the 'halt' command on to all the write mailboxes.
 - b. Put the 'motors halted' code in the response code location.
14. If the command is all motors go, then two steps are taken.
 - a. Call the global-write subroutine to pass the 'go' command on to all the write mailboxes.
 - b. Put the 'motors in go state' code in the response code location.
15. If the command is shared RAM peek, then several steps are taken.
 - a. Gain access to each motor's shared RAM, individually.
 - b. Move the data from the indicated address into the write buffer, with Motor 1 data at the bottom of the buffer.
 - c. Above the data in the write buffer, put the address from which the data came, the low and high bytes of the Rhino Clock, and the command to which the data is the response.
 - d. Set the pending transmit data byte counter to eleven.
 - e. Put the 'peek data ready' code in the response code buffer.

16. If the command is reset absolute position counters, then two steps are taken.
 - a. Call the global-write subroutine to pass the 'reset absolute position' command on to all the write mailboxes.
 - b. Put the 'absolute positions reset' code in the response code location.
17. If the command is coefficients, then several steps are taken.
 - a. Gain access to the shared RAM for the motor number indicated.
 - b. Move the coefficients from the read buffer to the corresponding shared RAM locations.
 - c. Check that the motor's write mailbox is not full.
 - 1) If it is full, and if the read mailbox is full, call the respond-to-8748 subroutine.
 - 2) Wait until the write mailbox is not full.
 - d. Put the 'coefficients' command code into the write mailbox.
 - e. Put the 'received data' code in the response code buffer.
18. Clear the VAX command location.
19. Jump to the write-to-VAX subroutine (that is, return from this subroutine by way of the write-to-VAX subroutine).

THE GLOBAL WRITE SUBROUTINE

The global-write subroutine writes a specified command code to all write mailboxes simultaneously.

1. Enable all write mailboxes.
2. If any write mailbox is full, then several steps are taken.
 - a. If any read mailbox is full, call the respond-to-8748 subroutine.
 - b. Keep checking the write and read mailboxes until all of the write mailboxes are empty.
3. Write the code from the 'global' location to all the mailboxes simultaneously.
4. Put the same code in each of the 'previous write to 8748' locations.
5. Return from the global-write subroutine.

THE SERIAL PORT INTERRUPT SERVICE SUBROUTINE

The serial-port-interrupt-service subroutine is called whenever the serial port finishes transmitting or receiving a byte of communication data.

1. Save the processor status word and the accumulator contents on the stack.
2. Select register bank 1.
3. If the receive interrupt flag is set, then a byte of communication data has just been received from the VAX.
 - a. Clear the receive interrupt flag.
 - b. If any receive data is pending (that is, if NR is not zero), then the byte just received is unformatted data.
 - 1) Compute the read buffer location in which to put the incoming data.
 - 2) Decrement the receive data pending counter (NR).
 - a) If the result is NR equals zero, then all data associated with the command in the input code buffer has been received.
 - i. Move the command from the input code buffer to the read code buffer, so it will be processed by the main routine.

- ii. Clear the input code buffer.
- iii. If the command is always followed by an address (for example, the peek commands), then the lowest byte in the read buffer is an address to be moved to the 'latch address' location.
 - b) If the result is NR not equal zero, then more data is yet to be received.
- c. If no receive data is pending (that is, if NR equals zero), then the incoming communication byte is a command code.
 - 1) Move the code from the serial port receiver buffer to the input code buffer.
 - 2) If the number of data bytes which are associated with the incoming command code is not zero, then several steps are taken.
 - a) Set the number of receive data bytes pending (NRBUFF) to the correct value for the particular command.
 - b) Set the 'request data from VAX' flag.
 - c) Call the serial-output subroutine.
- d. Recover the processor status word and accumulator contents from the stack.
- e. Return from the serial-port-interrupt-service subrou-

tine.

4. If the transmit interrupt flag is set, then several steps are taken.
 - a. Clear the transmit interrupt flag.
 - b. Call the serial-output subroutine.
 - c. Recover the processor status word and the accumulator contents from the stack.
 - d. Return from the serial-port-interrupt-service subroutine.

THE INTERRUPT ZERO SERVICE SUBROUTINE

The interrupt-zero-service subroutine is called whenever there is a low-to-high transition of the interrupt zero line of the Intel 8751.

1. Save the processor status word and accumulator contents on the stack.
2. Increment the two-byte Rhino Clock.
3. If the '8748 RAM peek in progress' flag is clear, move the interrupt command into the interrupt command buffer for processing by the main routine.
4. Recover the processor status word and accumulator contents from the stack.
5. Return from the interrupt-zero-service subroutine.

APPENDIX U. 8748 ASSEMBLY LANGUAGE PROGRAM OUTLINE

THE INITIALIZATION ROUTINE

The initialization routine is executed on power up.

1. Obtain the present shaft encoder disk position.
2. Set the 'motor stopped' flag.
3. Gain access to the shared RAM.
4. Clear shared RAM locations zero through 63.
5. Clear internal RAM locations zero through 63.
6. Test the shared RAM by a write and read of location zero.
7. Put the 'hardware reset' code in the write mailbox.
8. Write a zero pulsewidth to the pulsewidth latch.
9. Jump to the main program.

THE MAIN PROGRAM

The main routine services the mailboxes and responds to commands from the 8751.

1. Strobe the interrupt enable to pick up the interrupt condition.
2. If the write buffer is full, jump to the write routine.
3. If the read mailbox is full, read in the command and interpret it.
 - a. If the command is the no operation, then restart the main routine.
 - b. If the command code is not in valid format, put the 'resend request' code in the write buffer and go to the write routine.
 - c. If the command is resend request then several steps are taken.
 - 1) Put the code from the 'previous write' buffer in the write mailbox.
 - 2) Put the 'no operation' code in the 'previous write' buffer, in case the previously saved code was garbled before transmission (this avoids an infinite loop of resend requests and retransmissions of garbage).

- 3) Restart the main routine.
- d. If the command is clear remaining moves, then several steps are taken.
- 1) Clear the 'motor stalled' flag.
 - 2) Clear all next move locations, all present move locations, the present pulsewidth location, and the velocity set point location.
 - 3) Put the 'ready for next move' code into the write buffer.
 - 4) Restart the main routine.
- e. If the command is move, then several steps are taken.
- 1) Gain access to the shared RAM.
 - 2) Move in the 'next move infinite' and 'received next move' flags, the velocity, the low and high bytes of the next move, and the sign of the next move from the shared RAM.
 - 3) Restart the main routine.
- f. If the command is halt, clear the 'go' flag, and restart the main routine.
- g. If the command is go, set the 'go' flag and restart the main routine.
- h. If the command is 8748 peek/poke, then several steps are taken.
- 1) Gain access to the shared RAM.

- 2) Read in the 1-byte address to be 'peeked' or 'poked'.
 - 3) If the high bit of the address is set, then a 'poke' is to be executed (only the low six bits of the address are significant in internal RAM addresses).
 - a) Read in the data to be 'poked' from the data passing location in shared RAM.
 - b) Put that data into the location specified by the low six bits of the address byte.
 - c) Restart the main routine.
 - 4) If the high bit of the address is clear, then a 'peek' is to be executed.
 - a) Read data from the location specified by the low six bits of the address byte.
 - b) Move that data to the data passing location in shared RAM.
 - c) Put the 'peek complete' code into the write buffer.
 - d) Go to the write routine.
- i. If the command is reset absolute positions, then several steps are taken.
- 1) Gain access to the shared RAM.
 - 2) Clear the low and high bytes of the absolute posi-

tion.

3) Restart the main routine.

j. If the command is none of the above, then it must be coefficients.

1) Gain access to the shared RAM.

2) Move the six coefficients from their locations in shared RAM to the corresponding locations in internal RAM.

3) Restart the main routine.

4. The write routine is part of the main routine.

a. Move the code from the write buffer to the previous write buffer.

b. Clear the write buffer.

c. Strobe the interrupt enable line while waiting for the write mailbox to become empty (without this step, response to an interrupt might be delayed unduly).

d. Once the write mailbox is empty, put the code from the previous write buffer into the write mailbox.

e. Restart the main routine.

THE INTERRUPT SERVICE SUBROUTINE

The interrupt-service subroutine is executed whenever the interrupt line is active and the interrupt is enabled.

1. Put the 'interrupt acknowledge' address on Port 2 (this is also the address that enables the shaft encoder data latch output).
2. Read in the shaft encoder data.
3. If the position is unchanged since the last interrupt, call the motor-stopped subroutine, then return from the interrupt service routine.
4. Update the register 6 and 7 flags and data.
 - a. Exchange the present shaft encoder data for the contents of register 7.
 - b. Restore the previous state of the 'reversal since last update' flag (register 7, bit 0).
 - c. Exclusive-or the present encoder bit 0 with the previous encoder encoder bit 1 to obtain the absolute direction bit.
 - d. Update the 'absolute direction' flag by exchanging the new direction bit for the old flag value.
 - e. Exclusive-or the new and old values of the 'absolute direction' flag to see if the direction has just

changed.

f. If the direction has just changed, then two steps are taken.

1) Set the 'new motion' flag, since motor had to come to a stop before reversing.

2) Complement the 'reversal since last update' flag, unless the 'previous position 0,0' flag is set (since, in that case, the last update occurred just as the new direction began).

g. Exclusive-or the 'absolute direction' flag with the present move sign to obtain the new value for the 'relative direction' flag.

5. Determine the velocity of the motor.

a. If the 'new motion' flag is set, then the velocity is taken to be 1, since the interrupt clock value is meaningless, but there is motion.

b. If the 'new motion' flag is clear, then use the interrupt clock value to determine the velocity.

1) Effectively shift the 16-bit clock value left until it is left-adjusted, keeping track of the number of shifts required.

2) The high byte of this left-adjusted number is used to obtain a value from the velocity look-up table.

3) The look-up table value is shifted right a number

of times equal to eleven minus the number of left shifts required to left-adjust the clock value (note that this is based on the fact that the relationship between the clock value and the look-up table value is reciprocal and logarithmic base 2).

- 4) If a set bit is shifted out on the last right shift, round the result upward.
 - 5) If the result of the right-shifting is zero, set it to one to indicate that the motor is not stopped.
6. Copy the velocity value into the 'speed' location in internal RAM.
 7. Determine the velocity error.
 - a. If the 'relative motion' flag is set, then the speed is negative with respect to the velocity set point.
 - b. Subtract the speed from the velocity set point to obtain the velocity error.
 - c. Determine which maximum velocity error magnitude applies for the present velocity set point.
 - d. Limit the velocity error by the relationship: $-1 * (\text{maximum velocity error}) \leq \text{velocity error} \leq (\text{maximum velocity error})$.
 - e. If velocity change is towards the set point, then set the velocity error to zero.

8. If the 'go' flag is not set or if the 'stall' flag is set, then the motor is either halted or stalled.
 - a. Call the position-update subroutine.
 - b. Write zero pulsewidth to the pulsewidth modulator latch and to the internal 'pulsewidth' location.
 - c. Wait for the interrupt line to become inactive before returning from the interrupt.
9. If the 'go' flag is set and the 'stall' flag is clear, then several steps are taken.
 - a. Determine which velocity coefficient to use, based on the current velocity set point.
 - b. Call the pulsewidth-update subroutine.
 - c. Call the position-update subroutine.
 - d. Handle special cases of the state.
 - 1) If the position error is negative, then overshoot is occurring.
 - a) If the overshoot is at least one full hole, load the user-specified pulsewidth for a 'long' overshoot as the base pulsewidth.
 - b) If the overshoot is less than one full hole, load the user-specified pulsewidth for a 'short' overshoot as the base pulsewidth.
 - c) If motor motion is in the direction of worse overshoot, add the value of the 'speed'

location to the base pulsewidth to give additional braking that is proportional to the overshoot speed.

- d) Write the computed pulsewidth to the pulsewidth modulator latch with the pulsewidth sign opposite to the commanded move sign.
 - e) Wait for the interrupt line to become inactive before returning from the interrupt-service routine.
- 2) If the position error is zero, then several steps are taken.
- a) Clear the velocity set point, since move is finished.
 - b) If the speed equals one, then set pulsewidth to zero to avoid end position jitter.
 - c) If the speed is greater than one, then set the pulsewidth equal to the speed, thus applying braking power proportional to the speed.
 - d) Write the computed pulsewidth to the pulsewidth modulator latch with the pulsewidth sign opposite to the 'absolute direction' sign.
 - e) Wait for the interrupt line to become inactive before returning from the interrupt-service routine.

- 3) If the move error is positive and the velocity set point equals zero, then the motor is undershooting (that is, it has completed the last move command but is out of position in the undershoot direction).
 - a) If the undershoot is at least one full hole, load the user-specified pulsewidth for a 'long' overshoot as the pulsewidth.
 - b) If the undershoot is less than one full hole, load the user-specified pulsewidth for a 'short' overshoot as the pulsewidth.
 - c) Write the computed pulsewidth to the pulsewidth modulator latch with the pulsewidth sign the same as the 'absolute direction' sign.
 - d) Wait for the interrupt line to become inactive before returning from the interrupt-service routine.
- 4) If none of the cases above is true (that is, the move error is positive and the velocity set point is non-zero), then several cases must be considered.
 - a) If the position error greater than 127 holes then the state should be under ordinary velocity control (already determined); so just wait

for the interrupt line to become inactive and return from the interrupt service routine.

b) If the error is less than 128 holes, then several flags must be tested.

i. If the 'next move received' flag is set and the next move sign is the same as the present move sign, then the next move is like an extension of the present move.

i) If the 'next move infinite' flag is set, then the extension of the present move is long (at least 32 holes), so no preparation for stopping is required; just wait for the interrupt line to become inactive and return from the interrupt service routine.

ii) If the 'next move infinite' flag is clear, then the extension of the present move is short (less than 32 holes); if the present move (position error) is also small, then add the next move to the present move.

ii. Decelerate by ramping down the velocity set point: if the velocity set point exceeds the position error plus fifteen,

then the set point is replaced by the the position error plus fifteen.

- iii. Wait until the interrupt line is inactive, then return from the interrupt service routine.

THE MOTOR STOPPED SUBROUTINE

The motor-stopped subroutine is called from the interrupt-service subroutine whenever there is an interrupt with no motor motion.

1. If the interrupt line is still active, then motor motion has occurred (since the flip-flop that is set after 1/16 second of time passes without an interrupt should have been reset by the interrupt acknowledge), so return from the motor-stopped subroutine.
2. If the interrupt line is no longer active then the motor has not moved in the past 1/16 second.
 - a. Increment the 'motor stopped interrupt count', which keeps track of the number of times the motor stop interrupt has occurred since the last motion.

- b. Set the 'motor stopped' flag.
- c. Put zero in the 'speed' location.
- d. Call the position-update subroutine.
- e. If the 'stall' flag is set or the 'go' flag is clear, write zero to the pulsewidth modulator latch and the pulsewidth location in internal RAM, and return from the motor-stopped subroutine.
- f. If the 'stall' flag is clear and the 'go' flag is set, check to see if the motor is stalled.
 - 1) If the pulsewidth is at least 50% and the 'motor stopped interrupt count' is at least 8 (that is, motor has been stopped for at least one second), then the motor is stalled.
 - a) Set the 'stall' flag.
 - b) Write zero to the pulsewidth modulator latch and to the internal pulsewidth location.
 - c) Return from the motor-stopped subroutine.
 - 2) If the pulsewidth is less than 50% or the 'motor stopped interrupt count' is less than 8, then the motor is not stalled.
 - a) Call the move-yet? subroutine to determine the appropriate pulsewidth (which depends on the position error).
 - b) Write the pulsewidth to the pulsewidth modula-

- tor latch.
- c) Return from the motor-stopped subroutine.

THE MOVE YET? SUBROUTINE

The move-yet? subroutine checks the remaining position error and determines the appropriate pulsewidth.

1. If the position error is non-zero or if the 'quarter-hole tail' is non-zero, then the pulsewidth will be non-zero.
 - a. If the motor stopped interrupt count is exactly one, then add the velocity set point to the starting pulsewidth.
 - b. Add the user-specified starting pulsewidth to the current pulsewidth.
 - c. Obtain the pulsewidth sign by exclusive-or of the present move sign with the sign of the position error.
 - d. Return from the move-yet? subroutine with the accumulator cleared.
2. If the present position error is zero, then call the new-move subroutine.
 - a. If a non-zero new move is returned, determine the

starting pulsewidth.

- 1) Set the pulsewidth equal to the user-specified starting pulsewidth.
 - 2) Set the pulsewidth sign equal to the sign of the new move (position error).
 - 3) Return from the move-yet? subroutine with the accumulator cleared.
- b. If a zero new move is returned, do not change the pulsewidth, and return from the move-yet? subroutine with a non-zero value in the accumulator.

THE NEW MOVE SUBROUTINE

The new-move subroutine moves the data for a non-zero next move into the present move locations.

1. If the 'next move received' flag is not set, then return from the new-move subroutine with a non-zero value in the accumulator.
2. If the 'next move received' flag is set, then several steps are taken.
 - a. Clear the 'next move received' flag.

- b. Move the velocity command into the velocity set point location.
- c. Move the velocity, distance, and sign data from the next move locations to the present move locations.
- d. Put the 'ready for next move' code into the write buffer.
- e. Return from the new-move subroutine with the accumulator cleared.

THE POSITION UPDATE SUBROUTINE

The position-update subroutine updates the position error and quarter-hole error locations in internal RAM and the velocity and absolute position locations in shared RAM.

1. Gain access to the shared RAM.
2. Concatenate the sign bit from the 'absolute direction' flag and the present speed, storing the result in the velocity location of the shared RAM.
3. If the speed is zero, then the motor has not moved and no position updating is required, so just return from the position-update subroutine.

4. If the speed is not zero, then update the quarter-hole position error, the position error, and the absolute position.
 - a. If the 'relative direction' flag is set, then motion is in the direction opposite that specified by the move sign, so increment the quarter-hole position error.
 - b. If the 'relative direction' flag is clear, then motion is in the same direction as that specified by the move sign, so decrement the quarter-hole position error.
 - c. If the 'present position 0,0' flag is clear, then no further position updating is required, so return from the position-update subroutine.
 - d. If the 'present position 0,0' flag is set, then all position data locations are updated.
 - 1) Clear the quarter-hole position error location.
 - 2) If 'relative direction' flag is set, then increment the position error (present move) in internal RAM.
 - 3) If 'relative direction' flag is clear, then decrement the position error (present move) in internal RAM.
 - 4) If 'absolute direction' flag is set, then decrement the absolute position in shared RAM.
 - 5) If 'absolute direction' flag is clear, then incre-

ment the absolute position in shared RAM.

- 6) Return from the position-update subroutine.

THE PULSEWIDTH UPDATE SUBROUTINE

1. The pulsewidth-update subroutine determines the appropriate new pulsewidth (based on the present pulsewidth, the velocity error, and the velocity error coefficient), and writes the new pulsewidth to the pulsewidth modulator and to the internal RAM locations for the pulsewidth.
2. Call the multiply subroutine to multiply the velocity error and the velocity error coefficient (the returned quotient is therefore the pulsewidth increment).
3. If present pulsewidth (power) is in the direction opposite the commanded direction of motion, then it is negative with respect to the pulsewidth increment, so two's complement the pulsewidth increment before adding it to the pulsewidth.
4. Add the pulsewidth increment to the pulsewidth.
5. If the new pulsewidth exceeds 127, then it has overflowed.
 - a. If the pulsewidth increment was positive, then the

overflow is due to the magnitude exceeding the maximum allowed (127).

- 1) Set the pulsewidth equal to the maximum, 127.
 - 2) Concatenate the pulsewidth sign.
 - 3) Write the signed pulsewidth to the pulsewidth modulator.
 - 4) Return from the pulsewidth-update subroutine.
- b. If the pulsewidth increment was negative, then the overflow is due to the value of the pulsewidth going negative.
- 1) Two's complement the pulsewidth value.
 - 2) Complement the pulsewidth sign.
 - 3) Write zero to the pulsewidth modulator.
 - 4) Enter a delay loop to allow time for the power transistor that was turned on to reach the cutoff state before the other power transistor is turned on.
 - 5) Add the user-specified hysteresis value to the pulsewidth.
 - 6) If the pulsewidth now exceeds 127, set the it to the maximum value, 127.
 - 7) Concatenate the pulsewidth sign.
 - 8) Write the signed pulsewidth to the pulsewidth modulator.

- 9) Return from the pulsewidth-update subroutine.
6. If the new pulsewidth does not exceed 127, and if it is not zero, then add the user-specified hysteresis value to it.
7. If the pulsewidth now exceeds 127, set it to the maximum value, 127.
8. Concatenate the pulsewidth sign.
9. Write the signed pulsewidth to the pulsewidth modulator.
10. Return from the pulsewidth-update subroutine.

THE MULTIPLY SUBROUTINE

1. The multiply subroutine is a fast subroutine for multiplying the argument passed to it in the accumulator by the number in the location passed to it in address pointer RB1 R0 (where the number at RB1 R0 is taken to have only six significant digits, and taken to be divided by 16).
2. Save the original argument in RB1 R3, to preserve the sign data.
3. If the argument is negative (high bit set) then two's complement it.
4. Use RB0 R0 through RB0 R5 to store the argument multiplied

- by powers of 2, from 2^{+1} through 2^{-4} , respectively.
5. Obtain the coefficient from the location specified by the address pointer RB1 R0.
 6. For each bit of the coefficient that is not set, clear the corresponding register in RBO (for example, if bit 0 is not set, clear RBO R5 and if bit 3 is not set, clear RBO R2), for bits zero through five of the coefficient.
 7. Add the resulting contents of RBO R0 through RBO R5 to obtain the product.
 8. If the original argument was negative, two's complement the product.
 9. Return from the multiply subroutine.

APPENDIX V. LISTING OF THE SAMPLE PROGRAM ON VAX

This program was compiled by the VAX/VMS 11/780 resident PASCAL compiler. Page headings have been deleted for the sake of brevity.

```

0001 program rhinocom (input,output);
0002
0003
0004
0005
0006
0007
0008 {***** define the variable types ****}
0009 {*****}
0010
0011 TYPE
0012     smallint = 0..255;
0013     bvt1     = [byte] smallint;
0014
0015     code set type = set of smallint;
0016     mnemonic set type = set of char;
0017
0018     string5 = packed array [1..5] of char;
0019     string80 = varying [80] of char;
0020
0021
0022 {***** define the variables ****}
0023 {*****}
0024
0025
0026 var
0027     command, prevcommand, coi command : bvt1;
0028     code, termcode, expected code     : bvt1;
0029     pkaddress, dest                    : bvt1;
0030     termflag                            : bvt1;
0031     junkcode                            : bvt1;
0032     movesiqn                            : bvt1;
0033
0034     datatype : integer;
0035     movetime  : integer;
0036     modulomove : integer;
0037     length    : integer;
0038     loopcount : integer;
0039     status, delaystatus : integer;
0040     test1, test2 : integer;
0041     et1, chan1 : integer;
0042
0043     poke48data : array [0..2] of bvt1;
0044     latch51    : array [0..4] of bvt1;
0045     latch48    : array [0..10] of bvt1;
0046     latchex    : array [0..10] of bvt1;
0047     velocities : array [0..8] of bvt1;
0048     veloc cmd  : array [0..6] of bvt1;
0049     coefficients : array [0..14] of bvt1;
0050     movedata   : array [0..13] of bvt1;
0051     positiondata : array [0..15] of bvt1;
0052
0053     moves : array [0..6] of integer;
0054     positions : array [0..7] of integer;
0055     velocity : array [0..6] of integer;
0056
0057     autorespond : boolean;
0058     go flag     : boolean;
0059     readyflag  : boolean;
0060
0061     code set : code set type;
0062     mnemonic set : mnemonic set type;
0063
0064     source, rhino, keyboard : string5;
0065     junkinput : string80;
0066
0067     chrc : char;
0068
0069
0070 {***** define the communication codes ****}
0071 {***** between VAX and the 8751 ****}
0072 {*****}
0073
0074
0075 const
0076
0077     nop = 0; {no operation}
0078     ec1 = 17; {enable command-on-interrupt}
0079     dc1 = 34; {disable command-on-interrupt}
0080     pk48 = 51; {peek/poke 8748 internal ram}
0081     pk51 = 68; {peek 8751 internal ram or latch}
0082     vrg = 85; {velocity request}
0083     prq = 102; {position request}
0084     sndvx = 119; {send to VAX}
0085     crm = 153; {clear remaining moves}
0086     mov = 170; {move}
0087     hlt = 187; {halt}
0088     ago = 204; {all motors go}
0089     shrp = 221; {shared RAM peek}
0090     rap = 238; {reset absolute position}
0091     kif = 255; {coefficients}
0092
0093     ovr = 136; {send over (resend request)}
0094
0095     snd51 = 17; {send to 8751}
0096     rdynxt = 51; {ready for next move}
0097     dat = 68; {peek data ready}
0098     vdt = 85; {velocity data ready}
0099

```

```

0100      pdt      = 102;    {position data ready}
0101      rcvdat  = 119;    {received data}
0102      hwrst   = 170;    {hardware reset of Rhino}
0103      mtrstl  = 221;    {motor stall}
0104      inv     = 255;    {invalid data}
0105
0106
0107      {*****}
0108      {**      define external procedures:      **}
0109      {*****}
0110
0111  procedure rhinord
0112      (%stdescr tline:string5;
0113       %ref keybuff:byt1;
0114       %ref rhinobuff:byt1;
0115       %ref termflaq:byt1;
0116       %ref rhinoflaq:integer;
0117       %ref rhinochanal:integer); extern;
0118
0119
0120
0121  procedure rhinowr
0122      (%ref rhinoflaq:integer;
0123       %ref rhinochanal:integer;
0124       %ref buffer:byt1); extern;
0125
0126
0127      {*****}
0128      {**      define internal procedures :      **}
0129      {*****}
0130
0131  procedure tthead2(var dest:byt1);          {This procedure calls}
0132                                          {the rhinord external}
0133                                          {procedure, with the }
0134                                          {correct device name.}
0135
0136      begin
0137          status:=0;
0138
0139          if (rhino='ttb0:') or (rhino='TTB0:') then
0140              rhinord('ttb0:',termcode,dest,termflaq,e1,chan1);
0141          if (rhino='ttb1:') or (rhino='TTB1:') then
0142              rhinord('ttb1:',termcode,dest,termflaq,e1,chan1);
0143          if (rhino='ttb2:') or (rhino='TTB2:') then
0144              rhinord('ttb2:',termcode,dest,termflaq,e1,chan1);
0145          if (rhino='ttb7:') or (rhino='TTB7:') then
0146              rhinord('ttb7:',termcode,dest,termflaq,e1,chan1);
0147          if (rhino='tte7:') or (rhino='TTE7:') then
0148              rhinord('tte7:',termcode,dest,termflaq,e1,chan1);
0149
0150          if termflaq=0 then status:=10;
0151
0152      end;
0153
0154      {*****}
0155
0156  procedure get response(expected code:byt1);
0157                                          {this procedure looks for code}
0158                                          {from the rhino, then tests to}
0159                                          {see if it matches the code }
0160                                          {expected. A status code is }
0161                                          {returned indicating what code}
0162                                          {was actually received, if any}
0163
0164      begin
0165          code set:=(nop,hwrst,rdynxt,dat,
0166                   rcvdat,vdt,pdt,mtrstl,inv,ovr);
0167
0168          tthead2(code);
0169
0170          if status=10 then                { status = 10 only if a byte }
0171              writeln('No response...');  { is received from the Keyboard }
0172                                          { before a byte from the Rhino }
0173
0174          if status<10 then
0175              if code = expected code then status:=0
0176              else if code in code set then
0177                  case code of
0178                      nop      : begin
0179                                  writeln(' NO OPERATION code      ');
0180                                  writeln(' received from Rhino ');
0181                                  writeln(' before expected response ');
0182                                  writeln(' ..... ');
0183
0184                                  get response(expected code);
0185                                  end;
0186
0187                      hwrst    : begin
0188                                  status:=8;          {hardware reset}
0189                                  go flaq:=false;
0190                                  readyflaq:=true;
0191                                  end;
0192
0193                      mtrstl   : begin
0194                                  status:=7;          {motor stalled}
0195                                  go flaq:=false;
0196                                  readyflaq:=false;
0197                                  end;
0198
0199

```

```

0199      inv      : begin
0200                writeln('   INVALID DATA code      ');
0201                writeln('   received from Rhino      ');
0202                writeln('   before expected response  ');
0203                writeln('   .....');
0204
0205                get response(expected code);
0206                end;
0207
0208      rcvdat   : begin
0209                writeln('   RECEIVED DATA code    ');
0210                writeln('   received from Rhino    ');
0211                writeln('   .....');
0212
0213                get response(expected code);
0214                end;
0215
0216      ovr      : begin
0217                writeln('   RESEND REQUEST code    ');
0218                writeln('   received from Rhino    ');
0219                writeln('   .....');
0220                writeln('   . . resending: ',prevcommand);
0221                writeln('   .....');
0222
0223                rhinowr(efl,chanl,prevcommand);
0224                get response(expected code);
0225                end;
0226
0227      rdynxt   : begin
0228                writeln('   READY FOR NEXT MOVE code ');
0229                writeln('   received from Rhino      ');
0230                writeln('   before expected response ');
0231                writeln('   .....');
0232
0233                readyflag:=true;
0234                get response(expected code);
0235                end;
0236
0237      dat      : status:=-4;          {peek data ready}
0238
0239      vdt      : status:=-9;          {velocity data ready}
0240
0241      pdt      : status:=-16;         {position data ready}
0242
0243      end {various cases of code}
0244
0245      else status:=2;
0246
0247      if status<0 then {in this case, the 8751 has data to transmit}
0248      begin
0249          delaystatus:=status;          {delay asking for data}
0250          status:=0;                    {and go look again for}
0251          get response(expected code);   { the expected code }
0252          end;
0253
0254      if (status=2) and (expected code=snd51) then
0255      begin
0256          command:=nop;                 {in this case, 8748 mav}
0257          for loopcount:=1 to 17 do    {be expecting data, so }
0258              rhinowr(efl,chanl,command); {send 17 zero bytes to }
0259          status:=6;                    {clear communication and}
0260          {set status to data fault}
0261          end;
0262      end;
0263
0264      (*****)
0265
0266      procedure get data;
0267
0268      {this procedure gets a data}
0269      { stream from the rhino }
0270
0271      begin
0272          code:=sndvx; {send data to vax}
0273          rhinowr(efl,chanl,code);
0274          test1:=0;
0275          test2:=0;
0276          length:=0;
0277
0278          case datatype of
0279
0280          1 : begin {Datatype of 1 means that the data}
0281                  { from the 8751 are 'peck' data. }
0282                  case code of {Peck data are always preceded by }
0283                  { the original peck request code. }
0284
0285                  pk51 : begin
0286                      for loopcount:=3 downto 0 do
0287                          begin
0288                              length:=length+1;
0289                              tthread2(latch51[loopcount]);
0290                              if status<10 then test1:=
0291                                  test1 + latch51[loopcount];
0292                              if status=10 then test2:=10;
0293                          end;
0294                      end;
0295
0296
0297

```

```

0298         latch51(4):=code;
0299     end;
0300
0301     pk48 : begin
0302         for loopcount:=9 downto 0 do
0303             begin
0304                 length:=length+1;
0305                 ttread2(latch48(loopcount));
0306                 if status<10 then test1:=
0307                     test1 + latch48(loopcount);
0308                 if status=10 then test2:=10;
0309             end;
0310             latch48(10):=code;
0311         end;
0312
0313     shrpK : begin
0314         for loopcount:=9 downto 0 do
0315             begin
0316                 length:=length+1;
0317                 ttread2(latchex(loopcount));
0318                 if status<10 then test1:=
0319                     test1 + latchex(loopcount);
0320                 if status=10 then test2:=10;
0321             end;
0322             latchex(10):=code;
0323         end;
0324
0325     end; (various cases of original peek code)
0326
0327 end; (case of datatype = 1)
0328
0329 2 : begin
0330     for loopcount:=8 downto 0 do (datatype of 2 means that)
0331         begin (the data from 8751 are )
0332             begin { velocities
0333                 length:=length+1;
0334                 ttread2(velocities(loopcount));
0335                 if status<10 then
0336                     begin
0337                         test1:=test1 + velocities(loopcount);
0338                         if loopcount<7 then
0339                             if velocities(loopcount)>127 then
0340                                 velocity(loopcount):=
0341                                     -2 * ( 256 - velocities(loopcount) )
0342                                 else velocity(loopcount):=
0343                                     2 * velocities(loopcount);
0344                             end;
0345                         if status=10 then test2:=10;
0346                     end;
0347                 end;
0348             end; (case of datatype = 2)
0349
0350 3: begin
0351     for loopcount:=15 downto 0 do (Datatype of 3 means that the)
0352         begin { data from the 8751 are }
0353             begin { positions.
0354                 length:=length+1;
0355                 ttread2(positiondata(loopcount));
0356                 if status<10 then test1:=test1 + positiondata(loopcount);
0357                 if status=10 then test2:=10;
0358             end;
0359             if (not(status=10)) then
0360                 for loopcount:=0 to 7 do
0361                     begin
0362                         positions(loopcount):=positiondata[2*loopcount]
0363                             + 256*positiondata[2*loopcount+1];
0364                         if (positions(loopcount)>32767)
0365                             and (loopcount<>7) then
0366                             positions(loopcount):=
0367                                 -1 * (65536-positions(loopcount));
0368                     end;
0369                 end; (case of datatype = 3)
0370
0371 end; (various cases of datatype)
0372
0373 if (status<10) and (test1=0) then {8751 sent all zeros, a data fault}
0374     begin
0375         length:=17-length;
0376         writeln('reading', length, 'data to dummy location');
0377         for loopcount:=1 to length do
0378             ttread2(coda);
0379         if status<10 then status:=6; (data communication fault)
0380     end;
0381 if test2=10 then
0382     begin
0383         status:=10;
0384         writeln(' ');
0385         writeln('Data stream from Rhino contaminated ');
0386         writeln('before completion by entries from keyboard ');
0387         writeln('..... resulting data field is invalid. ');
0388     end;
0389
0390 end;
0391
0392 (*****
0393
0394
0395 procedure get screendata;
0396     begin (this procedure prompts the)

```

```

0397 if status=0 then { user for data to send to }
0398 case command of { the 8751 }
0399
0400 eci : begin
0401   writeln('Interrupt commands are executed by Rhino whenever ');
0402   writeln('the Interrupt Zero line has a low-high transition. ');
0403   writeln('Valid interrupt commands are: ');
0404   writeln;
0405   writeln('          51PK, 48PK, VRQ, and PRQ ');
0406   writeln;
0407   write ('          Interrupt command: ');
0408
0409   read(chrc);
0410
0411   if (not(chrc='4') and (not(chrc='5'))
0412       and (not(chrc='v') and (not(chrc='V'))
0413           and (not(chrc='p') and (not(chrc='P')))) then
0414     coi command:=nop;
0415
0416   if chrc='4' then coi command:=pk48;
0417   if chrc='5' then coi command:=pk51;
0418   if (chrc='v') or (chrc='V') then coi command:=vrq;
0419   if (chrc='p') or (chrc='P') then coi command:=prq;
0420
0421   readln(junkinput);
0422
0423 end;
0424
0425 Kff : begin
0426   writeln;
0427   write('          Enter MOTOR NUMBER (1 to 7) : ');
0428   readln(coefficients[0]);
0429   coefficients[0]:=coefficients[0] mod 8;
0430
0431   writeln('For velocity set point from 1 to 31,');
0432   write('          velocity error coefficient: ');
0433   readln(coefficients[1]);
0434   write('          maximum magnitude of error: ');
0435   readln(coefficients[5]);
0436   writeln('For velocity set point from 32 to 63,');
0437   write('          velocity error coefficient: ');
0438   readln(coefficients[2]);
0439   write('          maximum magnitude of error: ');
0440   readln(coefficients[6]);
0441   writeln('For velocity set point from 64 to 127,');
0442   write('          velocity error coefficient: ');
0443   readln(coefficients[3]);
0444   write('          maximum magnitude of error: ');
0445   readln(coefficients[7]);
0446   writeln('For velocity set points above 127,');
0447   write('          velocity error coefficient: ');
0448   readln(coefficients[4]);
0449   write('          maximum magnitude of error: ');
0450   readln(coefficients[8]);
0451   writeln(' ');
0452   write('          Enter gripper pulsewidth: ');
0453   readln(coefficients[9]);
0454   write('          Enter hysteresis pulsewidth: ');
0455   readln(coefficients[10]);
0456
0457   write('          Enter starting pulsewidth: ');
0458   readln(coefficients[11]);
0459
0460   write('          Enter long overshoot pulsewidth: ');
0461   readln(coefficients[12]);
0462
0463   write('          Enter short overshoot pulsewidth: ');
0464   readln(coefficients[13]);
0465
0466 end;
0467
0468 pk51 : begin {peek into 8751 ram or latch}
0469   writeln(' ');
0470   writeln('Data can be read from the following locations: ');
0471   writeln;
0472   writeln(' - 8751 internal RAM, addresses 0 to 127 ');
0473   writeln(' - limit switch latch, address 136 ');
0474   writeln(' - motors linked latch, address 152 ');
0475   writeln;
0476   write('          Enter address to be read from 8751: ');
0477
0478   readln(pkaddress);
0479 end;
0480
0481 pk48 : begin
0482   if chrc='4' then begin
0483     writeln(' ');
0484     writeln('8748 RAM addresses are 0 - 63. ');
0485     writeln(' ');
0486     write ('          Enter peek address: ');
0487
0488     readln(pkaddress);
0489     pkaddress:=pkaddress mod 128;
0490   end;
0491
0492   if chrc='W' then begin
0493     writeln;
0494     write('Motor number for the poke (1 to 7): ');
0495

```

```

0496         readln(poke48data1));
0497         poke48data[1]:=poke48data[1] mod 8;
0498
0499         writeln(' ');
0500         write(' Enter poke address (0 to 63): ');
0501         readln(poke48data2));
0502         poke48data[2]:=poke48data[2] mod 128;
0503         poke48data[2]:=poke48data[2] + 128;
0504
0505         writeln(' ');
0506         write(' Enter data to be written (0 to 255): ');
0507         readln(poke48data0));
0508         end;
0509
0510     end;
0511
0512
0513 shrpK : begin
0514         writeln(' ');
0515         writeln('Enter the location');
0516         write ('          to be read (0-255): ');
0517
0518         readln(pkaddress);
0519         pkaddress:=pkaddress mod 128;
0520         end;
0521
0522
0523 mov    : begin
0524         writeln(' ');
0525         writeln('Enter TIME move should take          ');
0526         write ('          (1 to 127 seconds): ');
0527
0528         readln(movetime);
0529
0530         writeln(' ');
0531         writeln('Enter the MOVES: ');
0532         writeln;
0533
0534         for loopcount:=0 to 6 do
0535             begin
0536                 write('          Motor', loopcount+1, ' : ');
0537
0538                 readln(moves[loopcount]);
0539
0540                 if moves[loopcount]<0 then
0541                     begin
0542                         movesign:=128;
0543                         moves[loopcount]:= -1 * moves[loopcount];
0544                     end
0545                 else movesign:=0;
0546
0547                 if (movetime<>0) then
0548                     veloc cmd[loopcount]:=
0549                         moves[loopcount] div movetime
0550                 else veloc cmd[loopcount]:=200;
0551
0552                 veloc cmd[loopcount]:=veloc cmd[loopcount] div 2;
0553                 veloc cmd[loopcount]:=veloc cmd[loopcount] mod 128;
0554
0555                 if (veloc cmd[loopcount]<=0)
0556                     and (moves[loopcount]>0) then
0557                     veloc cmd[loopcount]:=1;
0558
0559                 if veloc cmd[loopcount]>100 then
0560                     veloc cmd[loopcount]:=100;
0561
0562                 movedata[2*loopcount]:=moves[loopcount] mod 256;
0563                 movedata[2*loopcount+1]:=
0564                     (moves[loopcount] div 256) + movesign;
0565
0566                 if movesign=128 then
0567                     moves[loopcount]:= -1 * moves[loopcount];
0568
0569             end;
0570         end;
0571     end (case of command = mov)
0572
0573     end; . {various cases of command mnemonic}
0574
0575     writeln(' ');
0576
0577 end;
0578
0579 {*****}
0580
0581 procedure get alldata;          { this procedure obtains }
0582                                { data from the rhino }
0583
0584     begin
0585         rhinowr(efl,chan1,command);
0586         prevcommand:=command;
0587         if status=0 then
0588             begin
0589                 case command of
0590                     pk48: datatype:=1;      {set the datatype for use }
0591                     pk51: datatype:=1;      {in the get data procedure}
0592                     shrpK: datatype:=1;
0593                     vrq: datatype:=2;
0594

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0595         prq: datatype:=3;
0596     end;
0597     if datatype=1 then          {a peek command must be}
0598     begin                      {followed by an address}
0599         get response(snd51);
0600         if status=0 then rhinowr(ef1,chan1,pkaddress);
0601         if status=0 then get response(dat); {expect 'data ready'}
0602     end;
0603     else get response(command);
0604     if status=0 then get data;
0605     end;
0606 end;
0607
0608 {*****}
0609 procedure display 51data;      { this procedure displays the }
0610                               {data obtained from an 8751 peek}
0611 begin
0612     writeln(' 8751 PEEK:');
0613     writeln(' ');
0614     writeln('rhino time address data');
0615     writeln(latch51[3]*256+latch51[2],latch51[1],latch51[0]);
0616     writeln(' ');
0617 end;
0618
0619 {*****}
0620
0621 procedure display 48data;     { this procedure displays the }
0622                               {data obtained from an 8748 peek}
0623 begin
0624     writeln(' 8748 PEEK:');
0625     writeln(' ');
0626     writeln('rhino time address');
0627     writeln(latch48[9]*256+latch48[8],latch48[7]);
0628     writeln(' ');
0629     writeln(' motor 1 motor 2 motor 3 motor 4',
0630            ' motor 5 motor 6 motor 7');
0631     writeln(latch48[0],latch48[1],latch48[2],latch48[3],
0632            latch48[4],latch48[5],latch48[6]);
0633     writeln(' ');
0634 end;
0635
0636 {*****}
0637
0638 procedure display shrdata;    {this procedure displays the data}
0639                               {obtained from a shared RAM peek.}
0640 begin
0641     writeln(' SHARED RAM PEEK:');
0642     writeln(' ');
0643     writeln('rhino time address');
0644     writeln(latchex[9]*256+latchex[8],latchex[7]);
0645     writeln(' ');
0646     writeln(' motor 1 motor 2 motor 3 motor 4',
0647            ' motor 5 motor 6 motor 7');
0648     writeln(latchex[0],latchex[1],latchex[2],latchex[3],
0649            latchex[4],latchex[5],latchex[6]);
0650     writeln(' ');
0651 end;
0652
0653 {*****}
0654
0655 procedure display velocities; { this procedure displays }
0656                               {the velocity data from rhino}
0657 begin
0658     writeln(' VELOCITIES:');
0659     writeln(' ');
0660     writeln('rhino time motor 1 motor 2 motor 3 motor 4',
0661            ' motor 5 motor 6 motor 7');
0662     writeln(velocities[8]*256+velocities[7],velocity[0],
0663            velocity[1],velocity[2],velocity[3],
0664            velocity[4],velocity[5],velocity[6]);
0665     writeln(' ');
0666 end;
0667
0668 {*****}
0669
0670 procedure display positions;  { this procedure displays }
0671                               {the position data from rhino}
0672 begin
0673     writeln(' POSITIONS:');
0674     writeln(' ');
0675     writeln('rhino time motor 1 motor 2 motor 3',
0676            ' motor 4 motor 5 motor 6 motor 7');
0677     writeln(positions[7],positions[0],positions[1],positions[2],
0678            positions[3],positions[4],positions[5],positions[6]);
0679     writeln(' ');
0680 end;
0681
0682 {*****}
0683
0684 procedure send command get echo; {this procedure transmits the}
0685                               {command code and obtains the}
0686                               {resulting 8751 response if}
0687                               {an echo of the command is}
0688                               {the expected response.}
0689 begin
0690     rhinowr(ef1,chan1,command);
0691     prevcommand:=command;
0692     get response(command);
0693 end;

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```

0694      {*****}
0695
0696 procedure send 48data;          {this procedure sends the}
0697                               { appropriate data for an}
0698                               {8748 poke command (HR48)}
0699                               { to the 8751 }
0700     begin
0701       rhinowr(ef1,chan1,command);
0702       prevcommand:=command;
0703       get response(snd51);
0704       if status=0 then
0705         begin
0706           rhinowr(ef1,chan1,poKe48data[2]);
0707           get response(snd51);
0708           if status=0 then
0709             begin
0710               for loopcount:=1 downto 0 do
0711                 rhinowr(ef1,chan1,poKe48data[loopcount]);
0712                 get response(rcvdat);
0713             end
0714           end
0715         end;
0716     end;
0717      {*****}
0718
0719 procedure send moves;          {this procedure sends the data}
0720                               {in the MOVES array to the 8751}
0721     begin
0722       rhinowr(ef1,chan1,command); {move command to 8751}
0723       prevcommand:=command;
0724       get response(snd51); {should be 'send data'}
0725       if status=0 then
0726         begin
0727           for loopcount:=13 downto 0 do
0728             rhinowr(ef1,chan1,movedata[loopcount]);
0729             get response(snd51); {should be 'send data to 8751'}
0730             if status=0 then
0731               begin
0732                 for loopcount:=6 downto 0 do
0733                   rhinowr(ef1,chan1,veloc cmd[loopcount]);
0734                   get response(rcvdat);
0735                 end;
0736             end;
0737           if status=0 then readyflag:=false;
0738         end;
0739     end;
0740      {*****}
0741
0742 procedure load coefficients;   {this procedure sends the data}
0743                               {from the COEFFICIENTS array }
0744                               { to the 8751 }
0745     begin
0746       rhinowr(ef1,chan1,command); {coefficient command to 8751}
0747       prevcommand:=command;
0748       get response(snd51); {should be 'send data'}
0749       if status=0 then
0750         begin
0751           for loopcount:=14 downto 0 do
0752             rhinowr(ef1,chan1,coefficients[loopcount]);
0753             get response(rcvdat); {should be 'data received'}
0754           end;
0755         end;
0756     end;
0757      {*****}
0758
0759 procedure enable coi;         { this procedure sends the }
0760                               { interrupt command to rhino }
0761     begin
0762       rhinowr(ef1,chan1,command); {send 'enable command on interrupt'}
0763       prevcommand:=command;
0764       get response(snd51); {expected response is 'send data'}
0765       if status=0 then
0766         begin
0767           rhinowr(ef1,chan1,coi command); {send the interrupt command}
0768           get response(rcvdat); {expected response is 'data received'}
0769         end;
0770     end;
0771      {*****}
0772
0773 procedure code from 8751;     {this procedure tests the code }
0774                               { received from the 8751 }
0775     begin
0776       status:=0;
0777       code set:=lnop,rdynxt,hdwrst,mtrstl,ovr,dat,vdt,pdt,
0778               rap,dci,hl1,aqo,crm,rcvdat,snd51,inv);
0779       if code in code set then
0780         case code of
0781           nop      : writeln('          NO OPERATION');
0782           rdynxt   : begin
0783                       writeln('          READY FOR NEXT MOVE');
0784                       readyflag:=true;
0785                     end;
0786           hdwrst   : begin
0787                       readyflag:=true;
0788                     end;
0789         end;
0790     end;
0791
0792

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0793         writeln('          RHINO HARDWARE RESET      ');
0794         writeln('          System halted.          ');
0795         writeln('          Reload control coefficients. ');
0796         go flag:=false;
0797         readyflag:=true;
0798     end;
0799
0800 mtrstl : begin
0801         writeln('          RHINO STALLED          ');
0802         writeln('          System halted.          ');
0803         writeln('          Send CRM to clear stall condition. ');
0804         go flag:=false;
0805     end;
0806
0807 ovr      : begin
0808         writeln('          RESEND LAST COMMAND    ');
0809         writeln('          Previous command code : ',prevcommand);
0810     end;
0811
0812 dat      : begin
0813         if autorespond=true then
0814             begin
0815                 datatype:=1;
0816                 get data;
0817                 if status=0 then
0818                     case code of
0819                         pk48 : display 48data;
0820                         pk51 : display 51data;
0821                         shrpK : display shrdata;
0822                     end
0823                 end
0824                 else writeln('Peek data is ready');
0825             end;
0826
0827 vdt      : begin
0828         if autorespond=true then
0829             begin
0830                 datatype:=2;
0831                 get data;
0832                 if status=0 then display velocities;
0833             end
0834             else writeln('Velocity data ready');
0835         end;
0836
0837 pdt      : begin
0838         if autorespond=true then
0839             begin
0840                 datatype:=3;
0841                 get data;
0842                 if status=0 then display positions;
0843             end
0844             else writeln('Position data ready');
0845         end;
0846
0847 rap      : writeln(' ABSOLUTE POSITION COUNTER RESET');
0848
0849 aqo      : begin
0850         go flag:=true;
0851         writeln('          RHINO IN GO MODE');
0852     end;
0853
0854 hlt      : begin
0855         go flag:=false;
0856         writeln('          RHINO IN HALT MODE');
0857     end;
0858
0859 crm      : begin
0860         readyflag:=true;
0861         writeln('          REMAINING MOVES CLEARED');
0862     end;
0863
0864 rcvdat   : begin
0865         writeln('          RECEIVED ALL DATA      ');
0866         writeln('          ');
0867         writeln('          previous code = ',prevcommand );
0868     end;
0869
0870 dci      : writeln(' DISABLED COMMAND-ON-INTERRUPT');
0871
0872 snd51    : writeln(' READY TO RECEIVE DATA          ');
0873
0874 inv      : writeln(' INVALID DATA                    ');
0875
0876
0877     end (cases of command code from 8751)
0878
0879 else (if the code is not one of the known commands)
0880     begin
0881         if autorespond=true then
0882             writeln(' Unknown code from Rhino:', code );
0883         if autorespond=false then
0884             writeln('Data:', code );
0885         end;
0886     end;
0887
0888     writeln(' ');
0889 end;
0890
0891 (*****

```

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0892 procedure Rhino command(mnemonic:char); (this procedure tests the mnemonic)
0893                                     (received from the user's keyboard)
0894
0895 begin
0896
0897   status:=0;
0898   mnemonic set:=['G','N','D','C','K','H',
0899                'S','X','I','A','R','E','V','P','5','4','M'];
0900
0901   if mnemonic in mnemonic set then
0902     begin
0903       case mnemonic of
0904
0905         'G' : begin
0906                 writeln('unassigned command');
0907               end;
0908
0909         'N' : begin
0910                 command:=nop;
0911                 writeln('          NOP          ');
0912                 rhinowr(efl,chan1,command);
0913                 prevcommand:=command;
0914               end;
0915
0916         'D' : begin
0917                 command:=dci;
0918                 writeln('          DCI          ');
0919                 send command get echo;
0920               end;
0921
0922         'C' : begin
0923                 command:=crm;
0924                 writeln('          CRM          ');
0925                 send command get echo;
0926                 if status=0 then readyflag:=true;
0927               end;
0928
0929         'K' : begin
0930                 command:=kff;
0931                 get screendata;
0932                 if status=0 then writeln('          KFF          ');
0933                 if status=0 then load coefficients;
0934               end;
0935
0936         'S' : begin
0937                 command:=shrp;
0938                 get screendata;
0939                 if status=0 then writeln('          SHRP          ');
0940                 if status=0 then get alldata;
0941                 if status=0 then display shrdata;
0942               end;
0943
0944         'H' : begin
0945                 command:=hlt;
0946                 writeln('          HLT          ');
0947                 send command get echo;
0948                 if status=0 then go flag:=false;
0949               end;
0950
0951         'A' : begin
0952                 command:=aqo;
0953                 writeln('          AQO          ');
0954                 send command get echo;
0955                 if status=0 then go flag:=true;
0956               end;
0957
0958         'X' : begin
0959                 readln(command);
0960                 rhinowr(efl,chan1,command);
0961                 status:=11;
0962               end;
0963
0964         'R' : begin
0965                 command:=rap;
0966                 writeln('          RAP          ');
0967                 send command get echo;
0968               end;
0969
0970         'E' : begin
0971                 command:=eci;
0972                 get screendata;
0973                 if status=0 then writeln('          ECI          ');
0974                 if status=0 then enable coi;
0975               end;
0976
0977         'V' : begin
0978                 command:=vrq;
0979                 writeln('          VRQ          ');
0980                 get alldata;
0981                 if status=0 then display velocities;
0982               end;
0983
0984         'P' : begin
0985                 command:=prq;
0986                 writeln('          PRQ          ');
0987                 get alldata;
0988                 if status=0 then display positions;
0989               end;
0990

```

```

0991      '5' : begin
0992          command:=pk51;
0993          get screendata;
0994          if status=0 then writeln ('          51PK      ');
0995          if status=0 then get alldata;
0996          if status=0 then display 51data;
0997          end;
0998
0999      '4' : begin
1000          command:=pk48;
1001          get screendata;
1002          if status=0 then writeln ('          48PK      ');
1003          if status=0 then get alldata;
1004          if status=0 then display 48data;
1005          end;
1006
1007      'W' : begin
1008          command:=pk48;
1009          get screendata;
1010          if status=0 then writeln ('          WR48      ');
1011          if status=0 then send 48data;
1012          end;
1013
1014      'M' : begin
1015          if readyflag=false then status:=3
1016          else
1017              begin
1018                  command:=mov;
1019                  get screendata;
1020                  if status=0 then writeln('          MOV      ');
1021                  if status=0 then send moves;
1022                  if status=0 then
1023                      begin
1024                          writeln(' COMPUTED SPEEDS:');
1025                          writeln
1026                          (' motor 1 motor 2 motor 3 motor 4 motor 5 motor 6 motor 7');
1027                          writeln(2*veloc cmd[0],
1028                                  2*veloc cmd[1],2*veloc cmd[2],2*veloc cmd[3],
1029                                  2*veloc cmd[4],2*veloc cmd[5],2*veloc cmd[6]);
1030                          writeln(' ');
1031                          writeln('GO FLAG=',go flag);
1032                          end
1033                      end
1034                  end; {the case of mnemonic = 'M'}
1035          end; {the various cases of mnemonic}
1036
1037      writeln(' ');
1038
1039      case status of
1040
1041      0 : writeln('communication sequence completed');
1042
1043      1 : begin
1044          writeln('Rhino requests resend. ');
1045          writeln(' Previous command was: ',prevcommand);
1046          end;
1047
1048      2 : writeln('Rhino response unrecognized:',code);
1049
1050      3 : writeln('System not ready for next move. ');
1051
1052      4 : writeln('Command-on-interrupt enabled. ');
1053
1054      5 : writeln('Invalid data. ');
1055
1056      6 : writeln('Data communication fault. ');
1057
1058      7 : begin
1059          writeln('At least one motor is STALLED ...Rhino halted. ');
1060          writeln(' Issue CRM to clear stall condition. ');
1061          go flag:=false;
1062          end;
1063
1064      8 : begin
1065          writeln('HARDWARE RESET occurred ...Rhino halted. ');
1066          writeln(' Reload control coefficients. ');
1067          go flag:=false;
1068          end;
1069
1070      9 : writeln('8748 RAM PEEK in progress... ');
1071
1072      10 : writeln('Rhino communication interrupted from keyboard. ');
1073
1074      11 : writeln(' ');
1075
1076      end; {various cases of status}
1077
1078      end {close the if statement for mnemonic in mnemonic set}
1079
1080      else {mnemonic not in mnemonic set}
1081          writeln('UNKNOWN RHINO COMMAND. RETRY. ');
1082
1083      writeln(' ');
1084
1085      if delaystatus<0 then {Rhino has data to transmit}
1086          begin
1087
1088
1089

```

```

1090      writeln('..Rhino originated communication...');
1091      if delaystatus=-4 then
1092          begin
1093              datatype:=1;
1094              get data;
1095              if status=0 then
1096                  case code of
1097                      pk48 : displav 48data;
1098                      pk51 : displav 51data;
1099                      shrpk : displav shrdata;
1100                  end;
1101          end;
1102      if delaystatus=-9 then
1103          begin
1104              datatype:=2;
1105              get data;
1106              if status=0 then display velocities;
1107          end;
1108      if delaystatus=-16 then
1109          begin
1110              datatype:=3;
1111              get data;
1112              if status=0 then display positions;
1113          end;
1114      delaystatus:=1;
1115  end;
1116  end;
1117  end;
1118  end;
1119  end;
1120  end;
1121  end;
1122  (*****);
1123  procedure user help;
1124      begin
1125          {this procedure displays the}
1126          { meanings of the various }
1127          { command mnemonics }
1128          writeln('The following MNEMONICS represent valid commands: ');
1129          writeln('');
1130          writeln(' ECI = enable command-on-interrupt ');
1131          writeln(' DCI = disable command-on-interrupt ');
1132          writeln('');
1133          writeln(' AGO = all motors go ');
1134          writeln(' HLT = halt all motors ');
1135          writeln(' RAP = reset absolute position counters ');
1136          writeln('');
1137          writeln(' KFF = coefficients for control algorithm ');
1138          writeln(' CRM = clear remaining moves ');
1139          writeln(' MOV = move ');
1140          writeln('');
1141          writeln(' WR48 = write to 8748 internal ram (poke) ');
1142          writeln(' 48PK = 8748 internal ram peck ');
1143          writeln(' 51PK = 8751 internal ram peck ');
1144          writeln(' SHRPK = shared RAM peck ');
1145          writeln('');
1146          writeln(' VRQ = velocity data request ');
1147          writeln(' PRQ = position data request ');
1148          writeln('');
1149          writeln(' X = escape character: send numeric code directly ');
1150      end;
1151  (*****);
1152  procedure change flags;
1153  begin
1154      writeln('The following flags can be altered:');
1155      writeln('');
1156      writeln(' 1 = READYFLAG ');
1157      writeln(' 2 = GO FLAG ');
1158      writeln(' 3 = AUTORESPOND ');
1159      write ('Enter number of flag to change: ');
1160      read(chrc);
1161      readln(junkinput);
1162      case chrc of
1163          '1' : begin
1164              writeln('READYFLAG = ',readyflag);
1165              write ('Do you want to change it? (Y/N) ');
1166              read(chrc);
1167              readln(junkinput);
1168              if (chrc='v') or (chrc='Y') then
1169                  if readyflag=true then readyflag:=false
1170                  else readyflag:=true;
1171          end;
1172          '2' : begin
1173              writeln('GO FLAG = ',go flag);
1174              write ('Do you want to change it? (Y/N) ');
1175              read(chrc);
1176              readln(junkinput);
1177              if (chrc='v') or (chrc='Y') then
1178                  if go flag=true then go flag:=false
1179                  else go flag:=true;
1180          end;
1181          '3' : begin
1182              writeln('AUTORESPOND = ',autorepond);
1183              write ('Do you want to change it? (Y/N) ');
1184              read(chrc);
1185              readln(junkinput);
1186              if (chrc='v') or (chrc='Y') then
1187                  if autorepond=true then autorepond:=false
1188                  else autorepond:=true;
1189          end;
1190      end;

```

```

1189         end;
1190
1191
1192     '3' : begin
1193         writeln('AUTORESPOND = ',autorespond);
1194         write ('Do you want to change it? (Y/N) ');
1195         read(chrc);
1196         readln(junkinput);
1197         if (chrc='Y') or (chrc='y') then
1198             if autorespond=true then autorespond:=false
1199             else autorespond:=true;
1200         end;
1201     end; (case statement)
1202
1203 end; (change flags procedure)
1204
1205
1206
1207
1208
1209
1210     (*****
1211     (**      THE MAIN PROGRAM BEGINS HERE      **)
1212     (**      **)
1213     (*****
1214
1215     (INITIALIZE THE VARIABLES AND FLAGS)
1216
1217 begin
1218
1219     writeln('Enter device name');
1220     write(' for the RHINO port (TTBn:) .. '); {get the name of the terminal}
1221     {line that the Rhino is con- }
1222     { nected to. }
1223     readln(rhino);
1224
1225     modulomove:=32768; {Maximum allowable move command is +/- 32767.}
1226
1227     status:=0; {Initially, status indicates no errors}
1228     delaystatus:=1; { and no data waiting for transmission}
1229
1230     readyflag:=true; {Initially, system is ready for a move.}
1231     go flag:=false; {Initially, motors are all halted.}
1232     autorespond:=true; {Start program in automatic response mode.}
1233
1234
1235     (INITIALIZE THE COMMUNICATION LINK)
1236
1237
1238     writeln(' To initialize communication, ');
1239     writeln(' press any key ... ');
1240     writeln(' ');
1241
1242     tthread2(code); {When first called, channels and event flags}
1243     {are assigned for the Rhino and the keyboard}
1244
1245     writeln('Rhino assigned channel number = ',chan1);
1246     writeln;
1247
1248     if status=0 then (a code from Rhino was received first)
1249     begin
1250         writeln('Code from Rhino = ',code );
1251         writeln(' ');
1252         code from 8751;
1253     end
1254
1255     else (input from the keyboard was received first)
1256     begin
1257         writeln(' Sending HALT command to Rhino ');
1258         writeln(' ');
1259         command:=hlt;
1260         send command get echo;
1261         if status<10 then
1262         begin
1263             writeln('Rhino communication established. ');
1264             writeln(' ');
1265             writeln(' Code from Rhino = ', code );
1266             writeln(' ');
1267         end;
1268     end;
1269
1270     (INITIALIZATION IS COMPLETE)
1271
1272
1273
1274     (The next part of the main program monitors input from both the)
1275     ( user's keyboard and the Intel 8751 serial port. )
1276
1277
1278     repeat
1279     begin { Prompt the user for a command }
1280         writeln('COMMAND:'); {and call the procedure to await}
1281         tthread2(code); { code from either source. }
1282         { Upon return from tthread2, one }
1283         { of them has transmitted code.}
1284
1285     if termflag=0 then {code is from the keyboard rather than the Rhino}
1286     begin
1287         if (termcode>96) and (termcode<123) then (change characters)

```

```

1288          termcode:=termcode-32;          ( to upper case )
1289
1290      chrc:=chr(termcode);          {convert the 8-bit number }
1291          { to ASCII code. }
1292
1293          {Normally, the first character of }
1294          { the keyboard entry uniquely }
1295          { identifies the command, but }
1296          { if the entry is 'X', the escape }
1297          { character, what follows is the }
1298          { numerical command code to send.}
1299
1300      mnemonic set:=['?', 'Z', 'F'];      {see if entry is from the set of }
1301      if chrc in mnemonic set then      { internal program commands. }
1302          case chrc of
1303              '?' : user help;
1304              'F' : change flags;
1305              'Z' : writeln('MAIN PROGRAM EXECUTION ENDS');
1306          end {cases of internal program commands}
1307
1308      else Rhino command(chrc);          {if command is not from the set of }
1309          {internal program commands, then do}
1310          { see if it is a Rhino command. }
1311      end {the if..begin statement for input from the user's keyboard}
1312
1313      else {input is from the Rhino rather than the keyboard}
1314      begin
1315          if autorespond=true then {Rhino input is command code}
1316          begin
1317              writeln(' Rhino originated code ... ');
1318              writeln(' ');
1319              code from 8751; {go interpret the Rhino }
1320              { communication code }
1321          end;
1322          if autorespond=false then {Rhino input may be command or data}
1323          writeln(' code from rhino: ', code );
1324          writeln;
1325          end;
1326      end; {the repeat loop}
1327
1328      until chrc='Z'; {return to start of repeat loop}
1329          {unless Keyboard entry was 'Z'}
1330
1331      end.

```

COMMAND QUALIFIERS

```

PAS/LIS RHINOCOM
/CHECK=(BOUNDS, NOCASE SELECTORS, NOOVERFLOW, NOPOINTERS, NOSUBRANGE)
/DEBUG=(NOSYMBOLS, TRACEBACK)
/NOENVIRONMENT
/LIST=CS:(HOPKINS JRHINOCOM.LIS;81
/OBJECT=CS:(HOPKINS JRHINOCOM.OBJ;89
/NOCROSS REFERENCE /ERROR LIMIT=30 /NOG FLOATING /NOMACHINE CODE
/NOOLD VERSION /OPTIMIZE /NOSTANDARD /WARNINGS

```

COMPILER INTERNAL TIMING

Phase	Faults	CPU Time	Elapsed Time
Initialization	97	00:00.2	00:00.7
Source Analysis	344	00:04.3	00:05.3
Source Listing	25	00:01.8	00:02.8
Tree Construction	397	00:02.2	00:04.8
Flow Analysis	69	00:01.1	00:02.6
Profit Analysis	75	00:01.2	00:02.0
Context Analysis	454	00:13.0	00:23.9
Name Packing	11	00:00.6	00:00.9
Code Selection	109	00:03.0	00:05.4
Final	170	00:06.3	00:08.6
TOTAL	1759	00:33.7	00:57.2

COMPILATION STATISTICS

```

CPU Time: 00:33.7 (2390 Lines/Minute)
Elapsed Time: 00:57.2
Page Faults: 1759
Compilation Complete

```

APPENDIX W. LISTING OF THE 8751 ASSEMBLY LANGUAGE PROGRAM

This program was assembled on the Intel MDS-80 Development System, using the MCS-51 Macro Assembler, Version 2.0. The cross-reference and no-page-numbering options were specified.

ISIS-II MCS-51 MACRO ASSEMBLER V2.0
 OBJECT MODULE PLACED IN F1.P51V17.OBJ
 ASSEMBLER INVOKED BY ASM51.F1.P51V17.ASM XREF NOPAGING

LOC	OBJ	LINE	SOURCE	
		1		COMMUNICATION CODES FROM 8751 TO VAX

			;} NOP EQU 0H	;} NO OPERATION.
0011			;} SND51 EQU 11H	;} SEND DATA TO 8751.
0022			;} DCI EQU 22H	;} COMMAND ON INTERRUPT DISABLED.
0033			;} RDYNXT EQU 33H	;} RHINO READY FOR NEXT MOVE.
0044			;} DAT EQU 44H	;} DATA FROM 8751 RAM, 8748 RAM, SHARED RAM, ;} OR EXTERNAL LATCH FOLLOWS.
0055			;} VDT EQU 55H	;} VELOCITY DATA READY.
0066			;} PDT EQU 66H	;} POSITION DATA READY.
0077			;} RCVDAT EQU 77H	;} DATA RECEIVED.
0088			;} OVR EQU 88H	;} SEND PREVIOUS CODE OVER AGAIN.
0099			;} CRM EQU 99H	;} CLEARED REMAINING MOVES.
00AA			;} HDWRST EQU 0AAH	;} HARDWARE RESET.
00BB			;} HLT EQU 0BBH	;} INSTRUCTED ALL MOTORS TO HALT.
00CC			;} AGO EQU 0CCH	;} INSTRUCTED ALL MOTORS TO GO.
00DD			;} MTRSTL EQU 0DDH	;} RHINO MOTOR(S) STALLED.
00EE			;} RAP EQU 0EEH	;} ABSOLUTE POSITIONS RESET.
00FF			;} INV EQU 0FFH	;} INVALID DATA.
			;}	
				COMMUNICATION CODES FROM VAX TO 8751

			;} NOP EQU 00H	;} NO OPERATION.
0011			;} ECI EQU 11H	;} ENABLE COMMAND ON INTERRUPT.
			;} DCI EQU 22H	;} DISABLE COMMAND ON INTERRUPT.
0033			;} PK48 EQU 33H	;} 8748 INTERNAL RAM PEEK.
0044			;} PK51 EQU 44H	;} 8751 INTERNAL RAM (OR EXT LATCH) PEEK.
0055			;} VRQ EQU 55H	;} REQUEST VELOCITY DATA.
0066			;} PRQ EQU 66H	;} REQUEST POSITION DATA.
0077			;} SNDVX EQU 77H	;} SEND DATA FROM I/O BUFFER TO VAX.
			;} OVR EQU 88H	;} SEND PREVIOUS CODE OVER AGAIN.
00AA			;} CRM EQU 99H	;} CLEAR REMAINING MOVES IN ALL MOTORS.
			;} MOVE EQU 0AAH	;} MOVE DATA FOLLOWS.
			;} HLT EQU 0BBH	;} HALT ALL MOTORS.
			;} AGO EQU 0CCH	;} INSTRUCT ALL MOTORS TO GO.
00DD			;} SHRPK EQU 0DDH	;} RAM PEEK (TO SHARED RAMS).
			;} RAP EQU 0EEH	;} RESET ABSOLUTE POSITIONS OF ALL MOTORS.

```

00FF      63      KFF      EQU      OFFH      ; COEFFICIENTS FOLLOW.
          64      }
          65      }
          66      }
          67      }
          68      }
          69      }
          70      }
          71      }
          72      }
          73      }
          74      }
          75      }
          76      }
          77      }
          78      }
          79      }
00DD      80      PK48RM EQU      ODDH      ; READ 8748 INTERNAL RAM ADDRESS.
          81      }
          82      }
          83      }
          84      }
          85      }
          86      }
          87      }
          88      }
          89      }
          90      }
          91      }
          92      }
          93      }
          94      }
          95      }
          96      }
          97      }
          98      }
          99      }
          100     }
          101     }
          102     }
          103     }
          104     }
          105     }
          106     }
          107     }
          108     }
          109     }
          110     }
          111     }
          112     }
          113     }
          114     }
          115     }
          116     }
          117     }
          118     }
          119     }
          120     }
          121     }
          122     }
          123     }
          124     }
          125     }
          126     }
          127     }
          128     }
          129     }
          130     }
          131     }
          132     }
          133     }
          134     }
0010      103     SRRDBF      EQU      10H      ; (16) INPUT BUFFER FOR CODE FROM VAX.
0011      104     RDBOT      EQU      11H      ; (17) RAM LOCATION 9H TO 17H ARE THE INPUT
001F      105     RDTOP      EQU      1FH      ; (31) DATA BUFFERS FOR VAX/8751 DATA.
          106     }
0020      107     RSET48      EQU      20H      ; (32) 8748 HARDWARE RESET STATUS BYTE.
0021      108     RDY48      EQU      21H      ; (33) 8748 READY (FOR NEXT MOVE) STATUS BYTE.
0022      109     STLL48      EQU      22H      ; (34) 8748 STALL STATUS BYTE.
          110     }
0023      111     NEWSTL      EQU      23H      ; (35) 'NEW STALL HAS OCCURED' FLAG.
          112     }
0024      113     MTRLNK      EQU      24H      ; (36) EACH MOTOR LINKED HAS CORRESP BIT SET.
0025      114     MTRNMR      EQU      25H      ; (37) MOTOR NUMBER.
0026      115     BITLOC      EQU      26H      ; (38) BIT LOCATION.
          116     }
0028      117     RAMRDY      EQU      28H      ; (40) '8748 PEEK DATA READY' FLAGS.
0029      118     RAMADR      EQU      29H      ; (41) ADDRESS TO BE READ FOR PEEK COMMANDS.
          119     }
002A      120     RNOCKL      EQU      2AH      ; (42) RHINO CLOCK LOW BYTE.
002B      121     RNOCKH      EQU      2BH      ; (43) RHINO CLOCK HIGH BYTE.
          122     }
002C      123     INTCMD      EQU      2CH      ; (44) INTERRUPT COMMAND LOCATION.
002D      124     INTCDB      EQU      2DH      ; (45) INTERRUPT COMMAND BUFFER LOCATION.
          125     }
002E      126     VAXBUF      EQU      2EH      ; (46) VAX COMMAND BUFFER LOCATION.
002F      127     VAXCMD      EQU      2FH      ; (47) VAX COMMAND LOCATION.
          128     }
0030      129     GLOBL      EQU      30H      ; (48) GLOBAL 8748 WRITE BUFFER.
0030      130     PRVMTX      EQU      30H      ; (LOCATIONS 31H-37H HOLD PREVIOUS
          131     }
          132     }
          133     }
          134     }
0038      133     XMTFLG      EQU      38H      ; (56) THIS LOCATION HOLDS THE TRANSMIT FLAGS.
          134     }

```

0039	135	NTBUFF	EQU	39H	; (57) 'NT' BUFFER (SEE NEXT LOCATION).
003A	136	NT	EQU	3AH	; (58) NUMBER REMAINING DATA BYTES TO TRANSMIT.
003B	137	NRBUFF	EQU	3BH	; (59) 'NR' BUFFER (SEE NEXT LOCATION).
003C	138	NR	EQU	3CH	; (60) NUMBER REMAINING DATA BYTES TO RECEIVE.
	139				
003D	140	PRVXWR	EQU	3DH	; (61) PREVIOUS WRITE TO VAX.
003E	141	RESPCD	EQU	3EH	; (62) RESPONSE CODE LOCATION.
003F	142	SRWRBF	EQU	3FH	; (63) WRITE BUFFER LOCATION.
	143				
0040	144	WRBOT	EQU	40H	; (64) LOCATIONS 40H-4FH ARE THE DATA OUTPUT
004F	145	WRTOP	EQU	4FH	; BUFFERS FOR 8751/VAX COMMUNICATIONS.
	146				
004F	147	STKBAS	EQU	4FH	; (79) LOCATION BELOW START OF STACK.
	148				
	149				
	150				
	151				
	152				
	153				
	154				
0000	155	IDLE	EQU	00H	; DURING 'IDLE', READ MAILBOX FULL FLAGS ENABLED.
	156				
0018	157	MTRAM1	EQU	18H	; ADDRESS TO ENABLE RAM OF MOTOR ONE.
	158				
0080	159	GLBLWR	EQU	80H	; ADDRESS TO WRITE GLOBALLY TO PIGEON-HOLES.
	160				
0088	161	LIMLCH	EQU	88H	; ADDRESS TO ENABLE LIMIT SWITCH LATCH.
0098	162	LNKLCH	EQU	98H	; ADDRESS OF MOTORS LINKED LATCH.
	163				
	164	;XTLCH1	EQU	10101XXXB	; ADDRESS OF EXTRA LATCH 1.
	165	;XTLCH2	EQU	10111XXXB	; ADDRESS OF EXTRA LATCH 2.
	166	;XTLCH3	EQU	11001XXXB	; ADDRESS OF EXTRA LATCH 3.
	167	;XTLCH4	EQU	11011XXXB	; ADDRESS OF EXTRA LATCH 4.
	168	;XTLCH5	EQU	11101XXXB	; ADDRESS OF EXTRA LATCH 5.
	169	;XTLCH6	EQU	11111XXXB	; ADDRESS OF EXTRA LATCH 6.
	170				
	171				
	172				
	173				
	174				
00FD	175	BAUD96	EQU	0FDH	; THIS RELOAD VALUE COMPUTED FOR
	176				; TIMER ONE BAUD RATE GENERATION OF 9600.
	177				
00FA	178	BAUD48	EQU	0FAH	; THIS RELOAD VALUE COMPUTED FOR
	179				; TIMER ONE BAUD RATE GENERATION OF 4800.
	180				
0002	181	MTR1BT	EQU	2H	; MOTOR 1 BIT LOCATION IS BIT ONE.
	182				
	183				
	184				
	185				
	186				
	187				
	188				
0020	189	CF1	EQU	20H	; VELOCITY ERROR COEFFICIENT 1 (1-31 HPS)
0021	190	CF2	EQU	21H	; VELOCITY ERROR COEFFICIENT 2 (32-63 HPS)
0022	191	CF3	EQU	22H	; VELOCITY ERROR COEFFICIENT 3 (64-127 HPS)
0023	192	CF4	EQU	23H	; VELOCITY ERROR COEFFICIENT 4 (128+ HPS)
	193				
0024	194	MG1	EQU	24H	; MAX ERROR MAGNITUDE (1-31 HPS).
0025	195	MG2	EQU	25H	; MAX ERROR MAGNITUDE (32-63 HPS)
0026	196	MG3	EQU	26H	; MAX ERROR MAGNITUDE (64-127 HPS)
0027	197	MG4	EQU	27H	; MAX ERROR MAGNITUDE (128+ HPS)
	198				
0028	199	RAMDAT	EQU	28H	; DATA FOR 8748 POKE OR FROM 8748 PEEK.
	200	;RAMADR	EQU	29H	; 8748 RAM ADDRESS TO BE PEEKED OR POKED.
	201				
002A	202	SPEED	EQU	2AH	; MOTOR VELOCITY.
	203				
002C	204	NXVMNF	EQU	2CH	; 'NEXT MOVE INFINITE' FLAG.
002D	205	RCVDNM	EQU	2DH	; 'RECEIVED NEXT MOVE' FLAG.
002E	206	RAMVEL	EQU	2EH	; VELOCITY COMMAND LOCATION.
002F		LOBTMV	EQU	2FH	; LOW BYTE MOVE LOCATION.

```

0030      207      HIBTMV EQU 30H      ; HIGH BYTE MOVE LOCATION.
0031      208      NXMVSX EQU 31H      ; NEXT MOVE SIGN LOCATION.
                                209      ;
0033      210      LOBTPS EQU 33H      ; LOW BYTE ABSOLUTE POSITION.
0034      211      HIBTPS EQU 34H      ; HIGH BYTE ABSOLUTE POSITION.
                                212      ;
0038      213      GRIPPR EQU 38H      ; GRIPPER PULSEWIDTH.
                                214      ;
0039      215      HYSTPW EQU 39H      ; HYSTERESIS VALUE FOR MOTOR PULSEWIDTH.
003A      216      STRTPW EQU 3AH      ; STARTING PULSEWIDTH.
003B      217      LONGOV EQU 3BH      ; PULSEWIDTH VALUE FOR LONG OVERSHOOT.
003C      218      SHRTOV EQU 3CH      ; PULSEWIDTH VALUE FOR SHORT OVERSHOOT.
                                219      ;
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                                221      ; .....
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0000      225      ORG 0H              ; VECTOR LOCATION FOR HARDWARE RESET.
0000 012C 226      AJMP BEGIN0         ; JUMP TO INITIALIZATION ROUTINE.
                                227      ;
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0003      229      ORG 3H              ; VECTOR LOCATION FOR INTERRUPT ZERO.
0003 C136 230      AJMP INTRP0         ; JUMP TO INTERRUPT 0 SERVICE ROUTINE.
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0008      232      ORG 8H              ; UNUSED INTERRUPT VECTOR (TIMER 0).
0008 32   233      RETI
                                234      ;
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0013      235      ORG 13H             ; UNUSED INTERRUPT VECTOR (INTERRUPT 1).
0013 32   236      RETI
                                237      ;
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001B      238      ORG 1BH             ; UNUSED INTERRUPT VECTOR (TIMER 1).
001B 32   239      RETI
                                240      ;
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0023      242      ORG 23H             ; VECTOR LOCATION FOR SERIAL PORT INTERRUPT.
0023 A194 243      AJMP SRLISR         ; JUMP TO INTERRUPT SERVICE ROUTINE.
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002B      246      ORG 2BH             ; UNUSED INTERRUPT VECTOR (ON 8752).
002B 32   247      RETI
                                248      ;
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002C 75A080 254      BEGIN0: MOV P2,#GLBLNR ; WRITE
002F E4     255      CLR A ; 'NO OPERATION' CODE
0030 F2     256      MOVX @R0,A ; GLOBALLY (I.E., TO ALL MAILBOXES)
                                257      ;
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0031 F8     258      BEGLP1: MOV R0,A ; CLEAR INTERNAL RAM
0032 F6     259      MOV @R0,A ; LOCATIONS 0 THROUGH 127
0033 D8FD   260      DJNZ R0,BEGLP1
                                261      ;
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                                278      ;

0035 75A098 262      MOV P2,#LNKLCH ; READ IN 'MOTORS LINKED' DATA
0038 E590   263      MOV A,#1
003A 7FFA   264      MOV R7,#BAUD48
003C 20E002 265      JB ACC.0,BEG48 ; IF BIT ZERO IS SET, BAUD RATE IS 4800.
003F 7FFD   266      MOV R7,#BAUD96 ; OTHERWISE, IT IS 9600.
0041 54FE   267      MOV A,#0FEH
0043 F524   268      ANL MTRLNK,A ; STORE MOTOR LINKED DATA.
0045 75A000 269      MOV P2,#IDLE
                                270      ;
                                271      ;
                                272      ;
                                273      ;
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0048 852420 271      MOV RSET48,MTRLNK ; INITIALIZE THE HARDWARE RESET BYTE.
                                272      ;
                                273      ;
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                                278      ;

004B 752507 276      BEGLP2: MOV MTRNMR,#7H ; START WITH MOTOR NUMBER SEVEN,
004E 752680 277      MOV BITLOC,#80H ; WHICH CORRESPONDS TO BIT LOCATION 7.
                                278      ;
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                                300      ;

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0051 E590
0052 E524
0053 E526
0057 6011

0059 E525
005B C2
005C E5A0
005E E520
005F 64AA
0061 7007

0063 E526
0065 F4
0066 E520
0068 F520

006A E520
006C 600C
006E D52502
0071 8008

0073 E526
0075 03
0076 E526
0078 0151

007A 75814F

007D D29E

007F 438920
0082 8F80
0084 D28E

0086 C299

0088 C298
008A D29C

008C D2BC
008E D2AC

0090 7599AA
0093 753DAA

0096 852421
0099 052A

009B D288
009D D2A8

009F D2AF

00A1 75A000
00A4 E590
00A6 E524
00A8 6002
00AA 3180
00AC E524

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BEGLP3: MOV A,P1 ; ISOLATE THE
        ANL A,MTRLNK ; 'READ MAILBOX FULL' FLAG
        ANL A,BITLOC ; OF THE 'N'TH MOTOR, IF IT IS LINKED.
        JZ NXMTR1 ; IF NOT FULL, GO ON TO NEXT MOTOR.

        MOV A,MTRNMR ; BUT IF FULL,
        SHAP A ; READ IN THE CODE FROM THE
        MOV D2,A ; 'N'TH MOTOR'S MAILBOX.
        MOVX A,#R0 ;
        XRL A,#HDWRST ; IF CODE IS NOT 'HARDWARE RESET',
        JNZ NXMTR1 ; GO ON TO NEXT MOTOR.

        MOV A,BITLOC ; IF CODE IS 'HARDWARE RESET',
        CPL A ; CLEAR THE 'N'TH MOTOR'S
        ANL A,RSET48 ; RESET FLAG.
        MOV RSET48,A ;

NXMTR1: MOV A,RSET48 ; CHECK IF ALL MOTORS HAVE SENT RESET CODE.
        JZ BEGFIN ; IF SO, CONTINUE THE INITIALIZATION PROCEDURE.
        DJNZ MTRNMR,NXMTR2 ; IF NOT, GO CHECK THE NEXT MOTOR'S MAILBOX.
        JMP BEGLP2 ; IF RESULT IS ZERO, GO START WITH MOTOR 7 AGAIN.

NXMTR2: MOV A,BITLOC ; DETERMINE THE BIT WHICH CORRESPONDS
        RR A ; TO THE PARTICULAR MOTOR NUMBER
        MOV BITLOC,A ; WHICH IS TO BE CHECKED NEXT.
        AJMP BEGLP3 ;

BEGFIN: MOV SP,#STKBAS ; INITIALIZE THE STACK POINTER AT 79.
;.....
;-----
; INITIALIZE THE SERIAL PORT:
;-----
;.....
        SETB SCON.6 ; SET SERIAL PORT TO MODE 1.
        ORL TMOD,#20H ; SET TIMER 1 MODE TO 8-BIT, AUTO-RELOAD.
        MOV TH1,#7 ; PUT THE RELOAD VALUE INTO TIMER 1 HIGH BYTE.
        SETB TCON.6 ; START TIMER 1 (STARTS BAUD RATE GENERATION).

        CLR SCON.1 ; CLEAR TRANSMIT INTERRUPT FLAG.

        CLR SCON.0 ; CLEAR RECEIVE INTERRUPT FLAG.
        SETB SCON.4 ; ENABLE SERIAL PORT RECEIVER (REN).

        SETB IP.4 ; SET SERIAL PORT INTERRUPT TO HIGHEST PRIORITY.
        SETB IE.4 ; ENABLE THE SERIAL PORT INTERRUPT.
;.....
;-----
        MOV SBUF,#HDWRST ; PUT HARDWARE RESET CODE IN SERIAL BUFFER.
        MOV PRVXMR,#HDWRST ; ALSO PUT IT INTO PREVIOUS VAX WRITE.

        MOV R0Y48,MTRLNK ; INITIALIZE MOTOR READY FLAGS (NOT READY).
        INC RNOCKL ; INCREMENT RHINO CLOCK TO 1.

        SETB TCON.0 ; SET INTERRUPT ZERO TO EDGE-TRIGGERED MODE.
        SETB IE.0 ; ENABLE INTERRUPT ZERO.

        SETB IE.7 ; ENABLE ALL INTERRUPTS.
;.....
;-----
; MAIN ROUTINE POLLS 'READ MAILBOX FULL'
; FLAGS, AND EXECUTES ANY VAX COMMANDS
; INTERRUPTED BY SERIAL PORT OR INTERRUPT ZERO.
;-----
;.....
MAIN: MOV P2,#IDLE ; CHECK THE
      MOV A,P1 ; 'READ MAILBOX FULL' FLAGS
      ANL A,MTRLNK ; OF ALL LINKED MOTORS.
      JZ NOCOMM ;
      ACALL RESPND ; IF ANY MAILBOX IS FULL, CALL 'RESPOND'.
NOCOMM: MOV A,MTRLNK ; IF NO MOTORS ARE LINKED,

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00AE 6023
00B0 E528
00B2 6524
00B4 54FE
00B6 6047

00B8 E520
00BA 6002
00BC 2140

00BE E522
00C0 6002
00C2 2140

00C4 E521
00C6 700B
00C8 753E33
00CB 853E30
00CE 852421
00D1 31F4

00D3 E53A
00D5 70CA

00D7 E52F
00D9 7006
00DB 852E2F
00DE 752E00

00E1 E52F
00E3 6002
00E5 5144

00E7 E53A
00E9 453C
00EB 4539
00ED 4538
00EF 70B0

00F1 E52D
00F3 60AC
00F5 852D2F
00F8 752D00
00FB 5144
00FD 01A1

00FF 75A018
0102 752602
0105 7A07
0107 7840
0109 7928

010B E590
010D F4
010E 5524
0110 5526
0112 70F7

0114 E3
0115 F6

0116 E526
0118 23
0119 F526

011B E5A0
011D 2410
011F F5A0

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JZ INCODE
MOV A,RAMRDY
XRL A,MTRLNK
ANL A,#0FEH
JZ GETRAM

MOV A,RSET48
JZ STLCHK
AJMP NEWRST

STLCHK: MOV A,STLL48
JZ RDYCHK
AJMP STAL48

RDYCHK: MOV A,RDY48
JNZ INCODE
MOV RESPDC,#RDYNXT
MOV PRVXWR,RESPDC
MOV RDY48,MTRLNK
ACALL WRITVX

INCODE: MOV A,NT
JNZ MAIN

MOV A,VAXCMD
JNZ DECODE
MOV VAXCMD,VAXBUF
MOV VAXBUF,#0H

DECODE: MOV A,VAXCMD
JZ BKCOM1
ACALL DCDVAX

BKCOM1: MOV A,NT
ORL A,NR
ORL A,NTBUFF
ORL A,NRBUFF
JNZ MAIN

MOV A,INTCDB
JZ MAIN
MOV VAXCMD,INTCDB
MOV INTCDB,#0H
ACALL DCDVAX
AJMP MAIN

}.....
GETRAM: MOV P2,#MTRAM1
MOV BITLOC,#MTR1BT
MOV R2,#7H
MOV R0,#WRBOT
MOV R1,#RAMDAT

GETLP1: MOV A,P1
CPL A
ANL A,MTRLNK
ANL A,BITLOC
JNZ GETLP1

MOVX A,R1
MOV @R0,A

MOV A,BITLOC
RL A
MOV BITLOC,A

MOV A,P2
ADD A,#10H
MOV P2,A

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```

} THEN SYSTEM IS IN DEBUG MODE,
} SO SKIP THE FOLLOWING TESTS.
} CHECK 'PEEK DATA READY' FLAGS.
} IF ALL LINKED MOTORS HAVE PEEK
} DATA READY, THEN GO SEND
} PEEK DATA TO THE VAX.

} IF ANY LINKED MOTOR HAS
} RESET, GO NOTIFY THE VAX.

} IF ANY MOTOR HAS STALLED,
} SPECIAL HANDLING IS REQUIRED.

} IF ALL MOTORS
} ARE READY FOR
} NEXT MOVE, THEN
} NOTIFY THE VAX.

} IF ANY DATA REMAINS TO TRANSMIT TO VAX,
} DO NOT DECODE NEXT COMMAND.

} IF A VAX COMMAND IS WAITING
} TO EXECUTE, GO DECODE IT.
} ELSE, MOVE IN ANY NEW COMMAND FROM VAX BUFFER,
} AND CLEAR THE READ BUFFER.

} CHECK THE VAX COMMAND LOCATION.
} IF ZERO, THERE IS NO COMMAND TO EXECUTE.
} IF NOT ZERO, CALL DECODE VAX COMMAND.

} BEFORE EXECUTING THE 'INTERRUPT COMMAND',
} ALL PRESENT AND PENDING
} DATA COMMUNICATIONS MUST BE
} COMPLETED.

} LOAD ANY NON-ZERO INTERRUPT COMMAND
} INTO THE VAX COMMAND LOCATION,
} AND GO DECODE IT.

} LOAD THE 8748 PEEK DATA INTO THE WRITE
} BUFFER AREA, WITH MOTOR 1 DATA AT THE
} BOTTOM OF THE BUFFER.

} THE DATA FROM EACH 8748 IS AT
} THE SAME ADDRESS IN EACH SHARED RAM.

} GET THE DATA FROM ONE SHARED RAM
} AT A TIME. THIS INVOLVES POLLING
} AN INDIVIDUAL SHARED RAM LOCKOUT FLAG
} UNTIL ACCESS IS GAINED.

} ONCE ACCESS IS GAINED, MOVE IN THE PEEK
} DATA TO THE SPECIFIED WRITE BUFFER LOCATION.

} COMPUTE THE BIT CORRESPONDING TO THE NEXT
} MOTOR NUMBER OF THE NEXT SHARED RAM TO BE READ.

} COMPUTE THE ADDRESS OF THE
} SHARED RAM ENABLE FOR THE NEXT
} MOTOR TO BE READ.

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0121 08          423          INC R0          ; INCREMENT R0 TO NEXT WRITE BUFFER ADDRESS.
0122 DAE7        424          ;
0124 A629        425          DJNZ R2,GETLP1 ; SEE IF ALL SEVEN RAMS HAVE BEEN READ.
0126 08          426          ;
0127 A62A        427          MOV @R0,RAMADR ; ABOVE THE RAM PEEK DATA IN THE WRITE
0129 08          428          INC R0          ; BUFFER, PUT THE ADDRESS THAT WAS READ,
012A A62B        429          MOV @R0,RNOCKL ; THE LOW AND HIGH BYTES OF THE
012C 08          430          INC R0          ; 'RHINO CLOCK', AND THE COMMAND
012D 7633        431          MOV @R0,RNOCKH ; WHICH INITIATED THE PEEK (PK48).
012F 75390B      432          INC R0          ;
0132 752800      433          MOV @R0,#PK48 ;
0135 753E44      434          ;
0138 853E3D      435          MOV NTBUFF,#0BH ; SET NUMBER OF BYTES TO TRANSMIT TO 11.
013B 1201F4      436          MOV RAMRDY,#0 ; CLEAR THE RAM READY FLAGS.
013E 01A1        437          ;
0140 753EAA      438          MOV RESPDC,#DAT ; LOAD PEEK DATA READY AS RESPONSE.
0143 853E3D      439          MOV PRVXWR,RESPDC ; ALSO SAVE IT IN PREVIOUS WRITE TO VAX.
0146 752000      440          ;
0149 31F4        441          CALL WRITVX    ; GO WRITE THE CODE TO VAX.
014B 01A1        442          ;
014D E523        443          AJMP MAIN     ;
014F 600B        444          ;
0151 752300      445          ;
0154 753EDD      446          ;
0157 853E3D      447          ;
015A 31F4        448          ;
0160 852E2F      449          NEWRST: MOV RESPDC,#HDWRST ; IN CASE SOME 8748 HAS UNDERGONE A HARDWARE
0163 752E00      450          MOV PRVXWR,RESPDC ; RESET, SEND THE 'HARDWARE RESET' CODE
0166 E52F        451          MOV RSET48,#0H ; TO THE VAX, AND CLEAR THE RESET FLAGS.
0168 7002        452          ACALL WRITVX ;
016A 01E7        453          AJMP MAIN     ;
016C 64CC        454          ;
016E 6006        455          ;
0170 E52F        456          ;
0172 64AA        457          STAL48: MOV A,NEWSTL ; INSPECT THE 'NEW STALL' FLAG.
0174 7008        458          JZ STLRSP     ; IF NOT SET, GO CHECK VAX STALL RESPONSE.
0176 752FBB      459          ;
0179 753EDD      460          MOV NEWSTL,#0H ; IF 'NEW STALL' FLAG IS SET, THEN
017C 31F4        461          MOV RESPDC,#MTRSTL ; NOTIFY THE VAX OF THE STALL.
017E 01E1        462          MOV PRVXWR,RESPDC ;
0180          463          ACALL WRITVX ;
0182          464          ;
0184          465          STLRSP: MOV A,VAXCMD ; GET VAX STALL RESPONSE COMMAND,
0186          466          JNZ CHKCMD  ; EITHER FROM THE VAX COMMAND LOCATION
0188          467          MOV VAXCMD,VAXBUF ; OR FROM THE VAX COMMAND BUFFER.
018A          468          MOV VAXBUF,#0H ;
018C          469          ;
018E          470          CHKCMD: MOV A,VAXCMD ; DURING A STALL, THE 'MOVE' AND
0190          471          JNZ ISITGO ; THE 'GO' COMMANDS ARE NOT ALLOWED.
0192          472          AJMP BKCOMI ;
0194          473          ;
0196          474          ISITGO: XRL A,#AGO ; IF EITHER OF THOSE
0198          475          JZ NOTALW ; COMMANDS IS RECEIVED
019A          476          ; FROM THE VAX, THEN
019C          477          MOV A,VAXCMD ; RESEND THE 'MOTOR STALLED' CODE
019E          478          XRL A,#MOVE ; AND SUBSTITUTE THE 'HALT'
01A0          479          JNZ CODEOK ; FOR THE ONE SENT FROM VAX.
01A2          480          ; IF CODE IS NEITHER 'MOVE' NOR 'GO',
01A4          481          NOTALW: MOV VAXCMD,#HLT ; THEN DECODE IT AS USUAL.
01A6          482          MOV RESPDC,#MTRSTL ;
01A8          483          ACALL WRITVX ;
01AA          484          CODEOK: AJMP DECODE ;
01AC          485          ;
01AE          486          ;
01B0          487          ;
01B2          488          ;
01B4          489          ; 'RESPOND TO 8748 MAILBOX CODE' SUBROUTINE:
01B6          490          ;
01B8          491          ; PROVIDE: NOTHING
01BA          492          ;
01BC          493          ; RETURNS: APPROPRIATE CHANGES TO 8748
01BE          494          ; STATUS FLAGS (RSET48, STLL48, AND

```

0180 752507
 0183 752680
 0186 E590
 0188 E524
 018A E526
 018C 600B
 018E E525
 0190 C4
 0191 F5A0
 0193 E3
 0194 31A2
 0196 75A000
 0199 E526
 019B 03
 019C F526
 019E D525E5
 01A1 22

01A2 601F
 01A4 43A080
 01A7 FB
 01A8 7430
 01AA 2525
 01AC FB
 01AD EB
 01AE C4
 01AF 6B

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RESPND: MOV MTRNMR,#7H
 MOV BITLOC,#80H
 RESLP1: MOV A,P1
 ANL A,MTRLNK
 ANL A,BITLOC
 JZ NXMTR3
 MOV A,MTRNMR
 SWAP A
 MOV P2,A
 MOVX A,R01
 ACALL DCD48
 MOV P2,#IDLE
 NXMTR3: MOV A,BITLOC
 RR A
 MOV BITLOC,A
 DJNZ MTRNMR,RESLP1
 RET

DCD48: JZ DCDFIN
 ORL P2,#80H
 MOV R3,A
 MOV A,#PRVMTR
 ADD A,MTRNMR
 MOV R0,A
 MOV A,R3
 SWAP A
 XRL A,R3

RDY48). HALTS ALL MOTORS IF ONE OF
 THEM IS STALLED, AND SETS STALL
 FLAG TO INDICATE A NEW STALL
 RESENDS PREVIOUS CODE TO 8748 IF
 REQUESTED.
 CHANGES: ACCUM, P2, PSW, BITLOC, MTRNMR
 CALLS: 'DECODE 8748 CODE' ('DCD48')
 CALLED BY: MAIN ROUTINE ('GLOBAL WRITE') ('GLOBAL')
 START WITH MOTOR NUMBER SEVEN MAILBOX.
 LOAD IN CORRESPONDING BIT LOCATION.
 CHECK IF THE 'N'TH MOTOR'S
 'READ MAILBOX FULL' FLAG IS SET.
 IF NOT FULL, GO CHECK NEXT MOTOR'S MAILBOX.
 IF FULL, COMPUTE THE
 ADDRESS TO ENABLE THIS
 MOTOR'S READ MAILBOX, AND
 READ IN THE CODE FROM IT.
 CALL THE DECODE 8748 SUBROUTINE.
 CLEAR THE ENABLE ADDRESS FROM PORT 2.
 COMPUTE THE BIT LOCATION
 CORRESPONDING TO THE NEXT MOTOR.
 DECREMENT MOTOR NUMBER
 UNTIL ALL READ MAILBOXES HAVE BEEN CHECKED.

 'DECODE 8748 CODE' SUBROUTINE:
 PROVIDE: BYTE TO BE DECODED IN ACCUM,
 CORRECT MOTOR NUMBER IN MTRNMR,
 CORRECT MOTOR BIT LOCATION IN BITLOC,
 CORRECT 'READ MBX' ENABLED ON P2.
 RETURNS: APPROPRIATE ACTION TO CODE.
 CHANGES: P2, R0, R3, A, PSW,
 NEWSTL, GLOBL, RSET48, STLL48
 RDY48
 CALLS: 'GLOBAL WRITE' ('GLOBAL')
 (VECTORS TO 'CLRVRT')
 CALLED BY: 'RESPOND TO 8748' ('RESPND')
 IF CODE IS NON-ZERO,
 ENABLE THE MOTOR'S WRITE MAILBOX.
 SAVE ASIDE A COPY OF 8748 CODE.
 COMPUTE ADDRESS OF LOCATION
 WHERE CODE PREVIOUSLY SENT
 TO THIS MOTOR IS STORED.
 VALIDATE 8748 CODE BY
 CHECKING THAT BOTH
 NIBBLES ARE THE SAME.


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01B0 7012
01B2 EB
01B3 5407
01B5 601A
01B7 14
01B8 601A
01BA 14
01BB 6026
01BD 14
01BE 6029
01CO 14
01C1 602C
01C3 22
01C4 E590
01C6 E524
01C8 E526
01CA 70F8
01CC 7488
01CE F6
01CF F2
01D0 22
01D1 C6
01D2 F2
01D3 22
01D4 E526
01D6 4222
01D8 7523FF
01DB 75A080
01DE 748B
01EO B187
01E2 22
01E3 E526
01E5 4220
01E7 21DB
01E9 E526
01EB F4
01EC 5221
01EE 22
01EF E526
01F1 4228
01F3 22
01F4 E538

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JNZ RSNRQ1
MOV A,R3
ANL A,#7H
JZ RSND48
DEC A
JZ STL48
DEC A
JZ HWRST
DEC A
JZ RDYNX
DEC A
JZ PKRDY
DCDFIN: RET
RSNRQ1: MOV A,P1
ANL A,MTRLNK
ANL A,BITLOC
JNZ RSNRQ1
MOV A,#OVR
MOV @R0,A
MOVX @R0,A
RET
RSND48: XCH A,@R0
MOVX @R0,A
RET
STL48: MOV A,BITLOC
ORL STILL48,A
ORL NEWSTL,#OFFH
MOV NEWSTL,#OFFH
SNDHLT: MOV P2,#GLBLWR
MOV A,#HLT
MOVX @R0,A
ACALL CLRWR2
RET
HWRST: MOV A,BITLOC
ORL RSET48,A
AJMP SNDHLT
RDYNX: MOV A,BITLOC
CPL A
ANL A,RDY48,A
RET
PKRDY: MOV A,BITLOC
ORL RAMRDY,A
RET
WRITVX: MOV A,XMTFLG

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; IF NOT VALID, GO ASK FOR RESEND.
;
; IF VALID, DECODING DEPENDS ONLY
; ON THE LOWEST THREE BITS.
; IF CODE WAS 88H, GO RESEND LAST CODE.
;
; IF CODE WAS 99H, MOTOR IS STALLED.
;
; IF CODE WAS 0AAH, 8748 HAS RESET.
;
; IF CODE WAS 0BBH, READY FOR NEXT MOVE.
;
; IF CODE WAS 0CCH, RAM PEEK IS COMPLETE.
;
; IF NONE OF ABOVE, CODE HAS NO MEANING.
;
; OBTAIN 'WRITE MAILBOX FULL' FLAG
; FOR THIS MOTOR. IF IT IS FULL,
; WAIT FOR IT TO BE READ BY THE 8748.
;
; IF IT IS EMPTY,
; PUT 'RESEND REQUEST' CODE INTO MAILBOX,
; AND INTO 'PREVIOUS WRITE' LOCATION.
;
; IF A RESEND WAS REQUESTED BY THE 8748,
; WRITE PREVIOUS CODE TO MAILBOX, AND CLEAR
; PREVIOUS WRITE LOC TO AVOID INFINITE LOOP.
;
; IF THE MOTOR IS STALLED,
; SET THE MOTOR'S STALL FLAG,
; SET THE 'NEW STALL' FLAG,
; AND WRITE 'HALT' TO ALL MOTORS.
;
; IF THE 8748 HAS UNDERGONE HARDWARE RESET,
; SET THE MOTOR'S RESET FLAG,
; AND GO WRITE 'HALT' TO ALL MOTORS.
;
; IF THE 8748 IS READY FOR ANOTHER MOVE,
; CLEAR THE MOTOR'S 'NOT READY' FLAG.
;
; IF THE 8748 HAS JUST COMPLETED A PEEK,
; SET THE MOTOR'S 'PEEK COMPLETE' FLAG.
;
; .....
;
; WRITE TO VAX SUBROUTINE:
;
; PROVIDE: CODE FOR TRANSMISSION IN 'RESPCD'.
; RETURNS: IF TRANSMITTER IS IDLE, SENDS
; CODE DIRECTLY. IF NOT IDLE, CODE
; IS LEFT IN THE WRITE BUFFER FOR
; TRANSMISSION.
;
; CHANGES: RESPDC, WRBUF, ACCUM, PSM
; CALLS: 'SERIAL OUTPUT' ('SEROUT')
; CALLED BY: MAIN ROUTINE
; (NOTE, ALSO USED AS TAIL END
; OF DECODE VAX SUBROUTINE.)
;
; IF 'TRANSMITTER IDLE' FLAG IS SET,

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01F6 20E005	639	JB ACC.0,WRIRDY	GO CALL THE SERIAL OUTPUT SUBROUTINE.
	640		
01F9 E53E	641	MOV A,RESPCD	IF TRANSMITTER IS NOT IDLE, AND IF CODE
01FB 70F7	642	JNZ WRITVX	IS WAITING TO BE SENT, STAY IN THIS LOOP.
	643		(THIS PREVENTS OVERWRITING THE RESPONSE CODE)
	644		
01FD 22	645	RET	RETURN AFTER RESPONSE CODE IS WRITTEN.
	646		
01FE 5101	647	WRIRDY: ACALL SEROUT	
0200 22	648	RET	
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0201 5338FE	681	SEROUT: ANL XMTFLG,#0FEH	CLEAR THE 'TRANSMITTER IDLE' FLAG (BIT 0).
	682		
0204 E53A	683	MOV A,NT	IF THE 'DATA BYTES REMAINING' COUNTER
0206 702B	684	JNZ MRDATA	IS NOT ZERO, THERE IS MORE DATA TO TRANSMIT.
	685		
0208 E53F	686	MOV A,SRWRBF	IF CODE IS TO BE TRANSMITTED, THEN
020A 7019	687	JNZ PROCSS	CODE IN THE WRITE BUFFER HAS PRIORITY.
020C E53E	688	MOV A,RESPCD	IF WRITE BUFFER IS EMPTY, CODE IN THE
020E 753E00	689	MOV RESPCD,#0H	'RESPONSE CODE' LOCATION IS TRANSMITTED.
0211 7012	690	JNZ PROCSS	
0213 E538	691	MOV A,XMTFLG	IF BOTH THE ABOVE LOCATIONS ARE EMPTY, THEN
0215 30E128	692	JNB ACC.1,SETFLG	CHECK THE 'EXPECTING DATA' FLAG.
0218 5338FD	693	ANL XMTFLG,#0FDH	IF IT IS SET, THEN LOAD THE
021B 7411	694	MOV A,#SND51	'READY TO RECEIVE' CODE FOR TRANSMISSION.
021D 85383C	695	MOV NR,NRBUF	MOVE PENDING NUMBER OF RECEIVE DATA BYTES
0220 753B00	696	MOV NRBUF,#0H	INTO NUMBER OF RECEIVE DATA BYTES LOCATION.
0223 F53D	697	MOV PRVXWR,A	
	698		
0225 F53F	699	PROCSS: MOV SRWRBF,A	MOVE TRANSMIT CODE INTO WRITE BUFFER.
0227 14	700	DEC	IF NO-OP CODE IS TO BE TRANSMITTED, THEN THE
0228 7002	701	JNZ NOTNOP	NUMBER LOADED WILL BE THE NUMBER ONE.
022A F53F	702	MOV SRWRBF,A	IF IT IS 1, PUT NO-OP CODE IN WRITE BUFFER.
	703		
022C 853F99	704	NOTNOP: MOV SBUF,SRWRBF	MOVE CODE TO SERIAL PORT OUTPUT BUFFER,
022F 753F00	705	MOV SRWRBF,#0H	AND CLEAR WRITE BUFFER.
0232 22	706	RET	
	707		
0233 743F	708	MRDATA: MOV A,#SRWRBF	IF DATA IS TO BE SENT,
0235 253A	709	ADD A,NT	COMPUTE THE DATA BUFFER LOCATION
0237 F8	710	MOV R0,A	WHERE THE BYTE TO TRANSMIT IS FOUND.

0238 8699
023A 153A
023C 753D01
023F 22

0240 433801
0243 22

0244 E52F
0246 6053

0248 C4
0249 652F
024B 6002
024D 419F

024F E52F
0251 540F

0253 14
0254 7002
0256 41C4
0258 14
0259 7002
025B 41F0
025D 14
025E 7002
0260 41FB
0262 14
0263 7002
0265 618E
0267 14
0268 7002
026A 61B5
026C 14
026D 7002
026F 61F1
0271 14
0272 7002
0274 812B
0276 14
0277 7002
0279 812C
027B 14
027C 7002
027E 8137

711 MOV SBUF, @RO
712 DEC NT
713 MOV PRVXWR, #1
714 RET
715
716 SETFLG: ORL XMTFLG, #1H
717 RET
718
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745 DCDVAX: MOV A, VAXCMD
746 JZ DCVFIN
747
748 SWAP A
749 XRL A, VAXCMD
750 JZ DCOK
751 AJMP RSNRQ2
752
753 DCDOK: MOV A, VAXCMD
754 ANL A, #0FH
755
756 DEC A
757 JNZ DCNXT0
758 AJMP ENINT
759
760 DCNXT0: DEC A
761 JNZ DCNXT1
762 AJMP DISINT
763
764 DCNXT1: DEC A
765 JNZ DCNXT2
766 AJMP RAM48
767
768 DCNXT2: DEC A
769 JNZ DCNXT3
770 AJMP RAM51
771
772 DCNXT3: DEC A
773 JNZ DCNXT4
774 AJMP VLCREQ
775
776 DCNXT4: DEC A
777 JNZ DCNXT5
778 AJMP ABSREQ
779
780 DCNXT5: DEC A
781 JNZ DCNXT6
782 AJMP S1DDAT
783
784 DCNXT6: DEC A
785 JNZ DCNXT7
786 AJMP RSNDVX
787
788 DCNXT7: DEC A
789 JNZ DCNXT8
790 AJMP CR48MV

LOAD THE DATA BYTE TO THE SERIAL
PORT TRANSMIT BUFFER.
DATA TRANSMISSION DOES NOT BEGIN UNLESS
PREVIOUS CODE HAS BEEN RECEIVED BY VAX.

IN THE CASE OF NO TRANSMISSION,
SET THE 'TRANSMITTER IDLE' FLAG.

'DECODE VAX COMMAND' SUBROUTINE:

PROVIDE: VAX COMMAND IN 'VAX COMMAND'
('VAXCMD') LOCATION.

RETURNS: APPROPRIATE ACTION BASED ON
VAX COMMAND. RETURN CODE FOR
TRANSMISSION TO VAX, CORRECT VALUE
ENTERED INTO 'PREVIOUS WRITE TO VAX'
LOCATION ('PRVXWR').
LAST PART OF SUBROUTINE IS ALWAYS A
JUMP TO 'WRITE TO VAX'.

CHANGES: R0, R1, R2, R3, R4, IE, 0, ACCUM, PSW,
GLOBL, VAXCMD, INTCMD, INTCDB,
BITLOC, NTBUFF, NT, PRVXWR, WRBUF

CALLS: 'LOAD 8748 RAMS' ('LOAD48')
'GLOBAL WRITE' ('GLOBAL')
'COMPUTE VELOCITIES' ('VELOCS')

CALLED BY: MAIN ROUTINE

IF THE CODE IS ZERO,
NO OPERATION.

TEST CODE FOR VALIDITY
('NIBBLE'-WISE SYMMETRY)
IF CODE IS NOT VALID,
GO REQUEST A RESEND.

DECODE THE CODE BY TESTING
ONLY THE FOUR LOWER BITS.

IF CODE WAS 11H, INTERRUPT COMMAND FOLLOWS.

IF 22H, DISABLE EXTERNAL INTERRUPT ZERO.

IF 33H, PERFORM 8748 RAM PEEK/POKE.

IF 44H, PERFORM 8751 RAM OR LATCH PEEK.

IF 55H, SEND VELOCITY DATA.

IF 66H, SEND ABSOLUTE POSITION DATA.

IF 77H, SEND DATA FROM I/O BUFFER.

IF 88H, RESEND CODE PREVIOUSLY SENT TO VAX.

IF 99H, PASS 'CLEAR MOVES' CODE TO 8748'S.

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0280 14          783      DCNXT8: DEC      A          ;
0281 7002       784      JNZ      DCNXT9   ;
0283 813C       785      AJMP     MOVE48   ; IF 0AAH, MOVE DATA IS IN THE READ BUFFER.
0285 14         786      DCNXT9: DEC      A          ;
0286 7002       787      JNZ      DCNXT10  ;
0288 8100       788      AJMP     PASSON   ; IF 0BBH, PASS 'HALT' CODE TO 8748'S.
028A 14         789      DCNXT10: DEC     A          ;
028B 7002       790      JNZ      DCNXT11  ;
028D 8100       791      AJMP     PASSON   ; IF 0CCH, PASS 'GO' CODE TO 8748'S.
028F 14         792      DCNXT11: DEC     A          ;
0290 7002       793      JNZ      DCNXT12  ;
0292 81DA       794      AJMP     SHDRM   ; IF 0DDH, PERFORM SHARED RAM PEEK.
0294 14         795      DCNXT12: DEC     A          ;
0295 7002       796      JNZ      DCNXT13  ;
0297 8100       797      AJMP     PASSON   ; IF 0EEH, PASS 'RESET ABSOLUTE POSITION'
                                           ; CODE TO 8748'S.
0299 A115       800      DCNXT13: AJMP    COEF48   ; IF NONE OF ABOVE,
                                           ; THEN CONTROL COEFFICIENTS ARE IN READ BUFFER.
029B 752F00     801      DCVFIN: MOV     VAXCMD,#0H ; CLEAR THE VAX COMMAND LOCATION.
029E 22         802      RET
                                           ;
                                           ;
                                           ;
                                           ;
029F E53D       803      }.....
02A1 6444       804      }.....
02A3 6011       805      }.....
02A5 E53D       806      }.....
02A7 6455       807      }.....
02A9 600B       808      RSNRQ2: MOV     A,PRVXWR ; IF CODE PREVIOUSLY SENT TO VAX
02AB E53D       809      XRL     A,#DAT   ; IS ONE OF THE THREE CODES THAT
02AD 6466       810      JZ      FAULT    ; REQUIRE 'SEND DATA' AS A RESPONSE,
02AF 6005       811      MOV     A,PRVXWR ; THEN DO NOT REQUEST A RESEND FROM VAX,
02B1 753E88     812      XRL     A,#VDT   ; SINCE THE 'RESEND REQUEST' CODE MIGHT
02B4 41E8       813      JZ      FAULT    ; BE TREATED AS UNFORMATTED DATA BY VAX.
                                           ; INSTEAD, JUMP TO THE 'FAULT' LOCATION
                                           ; WHERE A STRING OF ZEROS IS SENT TO VAX
                                           ; TO RESTART THE COMMUNICATION SEQUENCE.
02B6 7A10       814      MOV     RESPDC,#OVR ; OTHERWISE, DO SEND
02B8 753E01     815      AJMP    PREWRI   ; 'RESEND REQUEST' CODE TO VAX.
02BB 31F4       816      }.....
02BD DAF9       817      }.....
                                           ;
02BF 853D3E     818      MOV     R2,#10H   ; SEND SIXTEEN ZEROS TO INDICATE
02C2 41E8       819      AJMP    PREWRI   ; A COMMUNICATION FAULT AND TO RESTART
                                           ; THE COMMUNICATION SEQUENCE.
                                           ;
                                           ;
02C4 E511       820      }.....
02C6 6433       821      }.....
02C8 6018       822      }.....
02CA E511       823      }.....
02CC 6444       824      }.....
02CE 6012       825      }.....
02D0 E511       826      }.....
02D2 6455       827      }.....
02D4 600C       828      }.....
02D6 E511       829      }.....
02D8 6466       830      }.....
02DA 6006       831      }.....
02DC 753EFF     832      }.....
02DF 0202E8     833      }.....
                                           ;
02E2 85112C     834      ENINT: MOV     A,RDBOT ; GET THE COMMAND TO EXECUTE ON INTERRUPT.
02E5 753E77     835      XRL     A,#PK48  ; TEST WHETHER IT IS ONE OF THE FOUR
02E8 752F00     836      JZ      VALCMD   ; COMMANDS THAT ARE ALLOWED TO BE
02EB 853E3D     837      MOV     A,RDBOT  ; EXECUTED ON INTERRUPT 1.
02EE 21F4       838      XRL     A,#PK51  ;
0290 7002       839      JZ      VALCMD   ;
0292 81DA       840      MOV     A,RDBOT  ;
0294 14         841      XRL     A,#PRQ   ;
0295 7002       842      JZ      VALCMD   ;
0297 8100       843      MOV     RESPDC,#INV ; IF IT IS NOT ONE OF THE FOUR, RETURN AN
0299 A115       844      AJMP    PREWRI   ; 'INVALID DATA' CODE AS RESPONSE.
029B 752F00     845      }.....
029E 22         846      }.....
029F E53D       847      }.....
02A1 6444       848      }.....
02A3 6011       849      }.....
02A5 E53D       850      }.....
02A7 6455       851      }.....
02A9 600B       852      }.....
02AB E53D       853      }.....
02AD 6466       854      }.....
02AF 6005       855      }.....
                                           ;
02B1 753E88     856      VALCMD: MOV     INTCMD,RDBOT ; OTHERWISE, STORE IT IN THE INTERRUPT
02B4 41E8       857      MOV     RESPDC,#RCVDAT ; COMMAND LOCATION, AND SEND
                                           ; 'RECEIVED DATA' CODE AS RESPONSE.
02B6 7A10       858      }.....
02B8 753E01     859      }.....
02BB 31F4       860      }.....
02BD DAF9       861      }.....
02BF 853D3E     862      }.....
02C2 41E8       863      }.....
02C4 E511       864      }.....
02C6 6433       865      }.....
02C8 6018       866      }.....
02CA E511       867      }.....
02CC 6444       868      }.....
02CE 6012       869      }.....
02D0 E511       870      }.....
02D2 6455       871      }.....
02D4 600C       872      }.....
02D6 E511       873      }.....
02D8 6466       874      }.....
02DA 6006       875      }.....
02DC 753EFF     876      }.....
02DF 0202E8     877      }.....
02E2 85112C     878      }.....
02E5 753E77     879      }.....
02E8 752F00     880      }.....
02EB 853E3D     881      }.....
02EE 21F4       882      }.....
0290 7002       883      }.....
0292 81DA       884      }.....
0294 14         885      }.....
0295 7002       886      }.....
0297 8100       887      }.....
0299 A115       888      }.....
029B 752F00     889      }.....
029E 22         890      }.....
029F E53D       891      }.....
02A1 6444       892      }.....
02A3 6011       893      }.....
02A5 E53D       894      }.....
02A7 6455       895      }.....
02A9 600B       896      }.....
02AB E53D       897      }.....
02AD 6466       898      }.....
02AF 6005       899      }.....
02B1 753E88     900      }.....
02B4 41E8       901      }.....
02B6 7A10       902      }.....
02B8 753E01     903      }.....
02BB 31F4       904      }.....
02BD DAF9       905      }.....
02BF 853D3E     906      }.....
02C2 41E8       907      }.....
02C4 E511       908      }.....
02C6 6433       909      }.....
02C8 6018       910      }.....
02CA E511       911      }.....
02CC 6444       912      }.....
02CE 6012       913      }.....
02D0 E511       914      }.....
02D2 6455       915      }.....
02D4 600C       916      }.....
02D6 E511       917      }.....
02D8 6466       918      }.....
02DA 6006       919      }.....
02DC 753EFF     920      }.....
02DF 0202E8     921      }.....
02E2 85112C     922      }.....
02E5 753E77     923      }.....
02E8 752F00     924      }.....
02EB 853E3D     925      }.....
02EE 21F4       926      }.....
0290 7002       927      }.....
0292 81DA       928      }.....
0294 14         929      }.....
0295 7002       930      }.....
0297 8100       931      }.....
0299 A115       932      }.....
029B 752F00     933      }.....
029E 22         934      }.....
029F E53D       935      }.....
02A1 6444       936      }.....
02A3 6011       937      }.....
02A5 E53D       938      }.....
02A7 6455       939      }.....
02A9 600B       940      }.....
02AB E53D       941      }.....
02AD 6466       942      }.....
02AF 6005       943      }.....
02B1 753E88     944      }.....
02B4 41E8       945      }.....
02B6 7A10       946      }.....
02B8 753E01     947      }.....
02BB 31F4       948      }.....
02BD DAF9       949      }.....
02BF 853D3E     950      }.....
02C2 41E8       951      }.....
02C4 E511       952      }.....
02C6 6433       953      }.....
02C8 6018       954      }.....
02CA E511       955      }.....
02CC 6444       956      }.....
02CE 6012       957      }.....
02D0 E511       958      }.....
02D2 6455       959      }.....
02D4 600C       960      }.....
02D6 E511       961      }.....
02D8 6466       962      }.....
02DA 6006       963      }.....
02DC 753EFF     964      }.....
02DF 0202E8     965      }.....
02E2 85112C     966      }.....
02E5 753E77     967      }.....
02E8 752F00     968      }.....
02EB 853E3D     969      }.....
02EE 21F4       970      }.....
0290 7002       971      }.....
0292 81DA       972      }.....
0294 14         973      }.....
0295 7002       974      }.....
0297 8100       975      }.....
0299 A115       976      }.....
029B 752F00     977      }.....
029E 22         978      }.....
029F E53D       979      }.....
02A1 6444       980      }.....
02A3 6011       981      }.....
02A5 E53D       982      }.....
02A7 6455       983      }.....
02A9 600B       984      }.....
02AB E53D       985      }.....
02AD 6466       986      }.....
02AF 6005       987      }.....
02B1 753E88     988      }.....
02B4 41E8       989      }.....
02B6 7A10       990      }.....
02B8 753E01     991      }.....
02BB 31F4       992      }.....
02BD DAF9       993      }.....
02BF 853D3E     994      }.....
02C2 41E8       995      }.....
02C4 E511       996      }.....
02C6 6433       997      }.....
02C8 6018       998      }.....
02CA E511       999      }.....
02CC 6444       1000     }.....

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02F0	752C00	855	DISINT:	MOV	INTCMD,#0H	DISABLE THE INTERRUPT-ON-COMMAND BY
02F3	752D00	856		MOV	INTCDB,#0H	PUTTING NO-OP CODE INTO INTERRUPT COMMAND
		857				LOCATIONS
02F6	852F3E	858		MOV	RESPCD,VAXCMD	ECHO 'INTERRUPT DISABLED' CODE AS RESPONSE.
02F9	41E8	859		AJMP	PREWRI	
		860				
		861				
		862				
		863				
		864				
		865				
		866				
		867				
02FB	E529	868	RAM48:	MOV	A,RAMADR	GET THE 8748 ADDRESS OF INTEREST.
02FD	20E72F	869		JB	ACC.7,POKE	IF THE HIGH BIT IS SET, COMMAND IS A POKE.
		870				
		871				
		872				
		873				
		874				
0300	75A018	875		MOV	P2,#MTRAMI	OTHERWISE, COMMAND IS A PEEK, SO
0303	752602	876		MOV	BITLOC,#MTR1BT	IT IS NECESSARY TO WRITE THE
0306	7A07	877		MOV	R2,#7H	ADDRESS TO EACH SHARED RAM INDIVIDUALLY.
0308	7829	878		MOV	R0,#RAMADR	START WITH MOTOR SEVEN.
		879				SET R1 TO ADDRESS OF 'RAM ADDRESS'.
030A	E590	880	RAMLP1:	MOV	A,P1	TEST THE PARTICULAR MOTOR'S
030C	F4	881		CPL	A	'SHARED RAM LOCKOUT' FLAG.
030D	F524	882		ANL	A,MTRLNK	WAIT IN THIS LOOP UNTIL
030F	F526	883		ANL	A,BITLOC	TO THIS MOTOR'S SHARED RAM.
0311	70F9	884		JNZ	RAMLP1	
		885				
0313	E529	886		MOV	A,RAMADR	MOVE THE ADDRESS OF INTEREST
0315	F2	887		MOVX	@R0,A	INTO THE PROPER LOCATION IN SHARED RAM.
		888				
0316	E526	889		MOV	A,BITLOC	COMPUTE THE BIT LOCATION
0318	F2	890		RL	A	CORRESPONDING TO
0319	F526	891		MOV	BITLOC,A	THE NEXT MOTOR NUMBER.
		892				
031B	E5A0	893		MOV	A,P2	COMPUTE THE SHARED RAM ENABLE ADDRESS
031D	F410	894		ADD	A,#10H	FOR THE NEXT MOTOR.
031F	F5A0	895		MOV	P2,A	
		896				
0321	DAE7	897		DJNZ	R2,RAMLP1	CONTINUE UNTIL SHARED RAMS OF ALL LINKED
0323	752801	898		MOV	RAMRDY,#1	MOTORS HAVE BEEN WRITTEN TO.
		899				SET '8748 PEEK IN PROGRESS' FLAG.
0326	7530DD	900		MOV	GLOBL,#PK48RM	WRITE 'READ RAM' TO ALL MAILBOXES.
0329	B16F	901		ACALL	GLOBAL	
		902				
032B	752F00	903		MOV	VAXCMD,#0H	CLEAR VAX COMMAND LOCATION. THERE IS
032E	22	904		RET		NO IMMEDIATE RESPONSE TO THIS COMMAND.
		905				(RESPONSE IS SENT AFTER 8748'S HAVE ALL
		906				PERFORMED THEIR INDIVIDUAL RAM PEEKS)
		907				
032F	753B02	908	POKE:	MOV	NRBUFF,#2H	FOR POKE COMMAND, ANOTHER TWO BYTES OF DATA
0330	433802	909		ORL	XMTFLG,#2H	MUST BE OBTAINED FROM THE VAX.
0332	753E00	910		MOV	RESPCD,#0H	GO ASK FOR THEM.
0338	31F4	911		ACALL	WRITVX	
		912				
033A	E53C	913	RAMLP2:	MOV	A,NR	WAIT UNTIL BOTH BYTES OF
033D	4538	914		ORL	A,NRBUFF	DATA HAVE BEEN RECEIVED.
033E	70FA	915		JNZ	RAMLP2	
		916				
0340	E512	917		MOV	A,RDBOT+1	GET MOTOR NUMBER OF 8748 TO BE POKED.
0342	F525	918		MOV	MTRNMR,A	THIS NUMBER IS USED BELOW IN A LOOP TO
0344	FA	919		MOV	R2,A	GENERATE THE CORRESPONDING BIT LOCATION.
0345	C4	920		SWAP	A	COMPUTE THE SHARED RAM ENABLE ADDRESS
0346	4408	921		ORL	A,#8H	FOR THIS MOTOR, AND ENABLE IT.
0348	F5A0	922		MOV	P2,A	
		923				
034A	7401	924	RAMLP3:	MOV	A,#1H	COMPUTE THE CORRESPONDING BIT LOCATION.
034C	F2	925		RL	A	
034E	DAFD	926		DJNZ	R2,RAMLP3	
034F	F526	927		MOV	BITLOC,A	
		928				
0351	E590	929	RAMLP4:	MOV	A,P1	GET 'SHARED RAM LOCKOUT' FLAG
0353	F4	930		CPL	A	FOR THE PARTICULAR MOTOR.
0355	F524	931		ANL	A,MTRLNK	STAY IN THIS LOOP UNTIL
0356	5526	932		ANL	A,BITLOC	ACCESS IS GAINED TO THE SHARED RAM.

0358	70F7	927	JNZ	RAMLP4	}	
		928			}	
035A	7929	929	MOV	R1,#RAMADR	}	PUT THE ADDRESS OF INTEREST
035B	7930	930	MOV	A,#R1	}	AND THE DATA BYTE TO BE POKED TO THAT ADDRESS
035C	7931	931	MOVX	@R1,A	}	IN THEIR PROPER LOCATIONS IN SHARED RAM.
035D	7932	932	DEC	R1	}	
035E	7933	933	MOV	A,#RDBOT	}	
0361	F3	934	MOVX	@R1,A	}	
		935			}	
0362	F5A0	936	MOV	A,P2	}	COMPUTE THE WRITE MAILBOX ENABLE ADDRESS
0364	6488	937	XRL	A,#88H	}	FOR THIS MOTOR, AND ENABLE IT.
0366	F5A0	938	MOV	P2,A	}	
		939			}	
0368	F590	940			}	
0369A	F524	941	RAMLP5:	MOV	A,P1	CHECK THAT THIS MOTOR'S
0369B	F524	942		ANL	A,#MTRLNK	WRITE MAILBOX IS NOT FULL.
0369C	F526	943		ANL	A,#BITLOC	
0369E	6013	944		JZ	RAMWRT	IF IT IS NOT FULL, GO WRITE TO THE MAILBOX.
		945				
0370	53A070	946		ANL	P2,#70H	BUT IF IT IS FULL, THEN
0371	F590	947		MOV	A,P1	CHECK IF THIS MOTOR'S
0372	F524	948		ANL	A,#MTRLNK	READ MAILBOX IS FULL, SINCE IF IT IS FULL,
0373	F526	949		ANL	A,#BITLOC	THE 8748 MAY BE WAITING TO WRITE TO IT,
0379	6003	950		JZ	NOTFLL	IN THAT CASE, BOTH MICROPROCESSORS WOULD
037B	F590	951		MOVX	A,#R0	GET STUCK WAITING TO WRITE FOREVER.
037C	31A2	952		ACALL	DCD48	SO, IF IT IS FULL, READ IT AND GO DECODE IT.
		953				
037E	43A080	954	NOTFLL:	ORL	P2,#80H	IF READ MAILBOX IS NOT FULL, GO BACK AND
0381	6168	955		AJMP	RAMLP5	SEE IF THE WRITE MAILBOX IS STILL FULL.
		956				
0383	74DD	957	RAMWRT:	MOV	A,#PK48RM	WHEN WRITE MAILBOX IS EMPTY,
0385	F2	958		MOVX	@R0,A	GO AHEAD AND WRITE THE 'PEEK RAM' CODE TO IT.
0386	75A000	959		MOV	P2,#IDLE	CLEAR ENABLE ADDRESS FROM PORT 2.
		960				
0389	753E77	961		MOV	RESPCD,#RCVDAT	LOAD 'RECEIVED DATA' AS RESPONSE TO VAX.
038C	41E8	962		AJMP	PREWRI	
		963				
		964	}			
		965	}			
038E	E529	966	RAM51:	MOV	A,RAMADR	TEST THE 8751 ADDRESS TO BE PEEKED.
0390	20E705	967		JB	ACC.7,LCHEXT	IF IT EXCEEDS 128, IT IS A LATCH ADDRESS.
		968				OTHERWISE, IT IS AN INTERNAL RAM ADDRESS.
0393	F8	969	RAMINT:	MOV	R0,A	PUT DATA FROM INTERNAL RAM LOCATION
0394	8640	970		MOV	WRBOT,@R0	IN LOWEST WRITE BUFFER LOCATION.
0396	61A0	971		AJMP	RAMFIN	
		972				
0398	F5A0	973	LCHEXT:	MOV	P2,A	PUT DATA FROM EXTERNAL LATCH
039A	8E9040	974		MOV	WRBOT,P1	IN LOWEST WRITE BUFFER LOCATION.
039D	75A000	975		MOV	P2,#IDLE	
		976				
03A0	7941	977	RAMFIN:	MOV	R1,#WRBOT+1	ABOVE THE PEEK DATA, IN THE WRITE BUFFER,
03A2	A729	978		MOV	@R1,RAMADR	PUT THE ADDRESS WHERE DATA WAS OBTAINED,
03A4	05	979		INC	R1	THE LOW AND HIGH BYTES OF 'RHINO CLOCK',
03A5	A72A	980		MOV	@R1,RNOCKL	AND THE COMMAND TO WHICH THIS DATA
03A7	05	981		INC	R1	IS THE RESPONSE.
03A8	A72B	982		MOV	@R1,RNOCKH	
03AA	05	983		INC	R1	
03AB	7744	984		MOV	@R1,#PK51	
		985				
03AD	753905	986		MOV	NTBUFF,#5H	SET 'NT BUFFER' FOR FIVE BYTES OF DATA.
		987				
03B0	852F3E	988		MOV	RESPCD,VAXCMD	ECHO '51RQ' CODE AS RESPONSE.
03B3	41E8	989		AJMP	PREWRI	
		990				
		991	}			
		992	}			
03B5	75A018	993	VLCREQ:	MOV	P2,#MTRAM1	TO SEND VELOCITIES OF ALL MOTORS, IT IS
03B8	752602	994		MOV	BITLOC,#MTR1BT	NECESSARY TO GAIN ACCESS TO EACH MOTOR'S
03BB	7820	995		MOV	R0,#WRBOT	SHARED RAM, INDIVIDUALLY, TO READ ITS
03BD	72A	996		MOV	R1,#SPEED	VELOCITY LOCATION. START WITH MOTOR 1.
03BF	7A07	997		MOV	R2,#7H	
		998				
03C1	E590	999	VLCLP1:	MOV	A,P1	CHECK THIS MOTOR'S

03C3	F4	999	CPL	A	;	'SHARED RAM LOCKOUT' FLAG.
03C4	5524	1000	ANL	A,MTRLNK	;	WAIT IN THIS LOOP UNTIL
03C6	5526	1001	ANL	A,BITLOC	;	ACCESS IS GAINED TO
03C8	70F7	1002	JNZ	VLCLP1	;	THIS MOTOR'S SHARED RAM.
		1003			;	
03CA	F3	1004	MOVX	A,R1	;	ONCE ACCESS IS GAINED,
03CB	30E704	1005	MOV	ACC,7,VLC2S	;	READ THE 'VELOCITY' LOCATION.
03CE	5480	1006	XRL	A,#80H	;	IF BIT 7 IS SET, DIRECTION OF MOTION IS
03D0	F4	1007	CPL	A	;	COUNTERCLOCKWISE, SO PUT VELOCITY IN
03D1	04	1008	INC	A	;	2'S COMPLEMENT FORM.
		1009			;	
03D2	F6	1010	VLC2S: MOV	R0,A	;	MOVE VELOCITY TO ITS LOCATION IN THE WRITE
03D3	08	1011	INC	R0	;	BUFFER, MOTOR 1 AT THE BOTTOM.
		1012			;	
03D4	F5A0	1013	MOV	A,P2	;	COMPUTE SHARED RAM ENABLE ADDRESS
03D6	2410	1014	ADD	A,#10H	;	FOR THE NEXT MOTOR'S SHARED RAM,
03D8	F5A0	1015	MOV	P2,A	;	AND ENABLE IT.
		1016			;	
03DA	F526	1017	MOV	A,BITLOC	;	COMPUTE THE BIT LOCATION CORRESPONDING
03DC	23	1018	RL	A	;	TO THE NEXT MOTOR'S MOTOR NUMBER.
03DD	F526	1019	MOV	BITLOC,A	;	
		1020			;	
03DF	DAE0	1021	DJNZ	R2,VLCLP1	;	LOOP UNTIL ALL RAMS HAVE BEEN READ.
		1022			;	
03E1	A62A	1023	MOV	R0,RNOCKL	;	ABOVE ALL THE VELOCITY DATA
03E2	08	1024	INC	R0	;	IN THE WRITE BUFFER,
03E4	A62B	1025	MOV	R0,RNOCKH	;	PUT THE LOW AND HIGH 'RHINO CLOCK' BYTES.
		1026			;	
03E6	753909	1027	MOV	NTBUFF,#9H	;	SET 'NT BUFFER' FOR 9 BYTES OF DATA.
		1028			;	
03E9	75A000	1029	MOV	P2,#IDLE	;	CLEAR LAST ENABLE ADDRESS FROM PORT 2.
		1030			;	
03EC	852F3E	1031	MOV	RESPCD,VAXCMD	;	ECHO 'VRQ' CODE AS RESPONSE TO VAX.
03EF	41E8	1032	AJMP	PREWRI	;	
		1033			;	
		1034			;	
		1035			;	
		1036			;	
		1037			;	
		1038			;	
		1039			;	
		1040			;	
		1041			;	
		1042			;	
		1043			;	
		1044			;	
		1045			;	
		1046			;	
		1047			;	
		1048			;	
		1049			;	
		1050			;	
		1051			;	
		1052			;	
		1053			;	
		1054			;	
		1055			;	
		1056			;	
		1057			;	
		1058			;	
		1059			;	
		1060			;	
		1061			;	
		1062			;	
		1063			;	
		1064			;	
		1065			;	
		1066			;	
		1067			;	
		1068			;	
		1069			;	
		1070			;	
03F1	75A018	1071	ABSREQ: MOV	P2,#MTRAM1	;	TO SEND ABSOLUTE POSITION DATA FROM ALL MOTORS,
03F4	752602	1072	MOV	BITLOC,#MTR1BT	;	IT IS NECESSARY TO READ THE SHARED RAM OF EACH
		1073			;	MOTOR INDIVIDUALLY. START WITH MOTOR 1,
		1074			;	WHOSE DATA GOES AT THE BOTTOM OF THE WRITE
		1075			;	BUFFER.
		1076			;	
		1077			;	
		1078			;	
		1079			;	
		1080			;	
		1081			;	
		1082			;	
		1083			;	
		1084			;	
		1085			;	
		1086			;	
		1087			;	
		1088			;	
		1089			;	
		1090			;	
		1091			;	
		1092			;	
		1093			;	
		1094			;	
		1095			;	
		1096			;	
		1097			;	
		1098			;	
		1099			;	
		1100			;	

0420	753910	1071			
		1072	MOV	NTBUFF,#10H	SET 'NT BUFFER' FOR 16 BYTES OF DATA.
		1073			
0423	75A000	1074	MOV	P2,#IDLE	CLEAR LAST ENABLE ADDRESS FROM PORT 2.
		1075			
0426	852F3E	1076	MOV	RESPCD,VAXCMD	ECHO 'PRQ' CODE AS RESPONSE TO VAX.
0429	41E8	1077	AJMP	PREWRI	
		1078			
		1079	}	
042B	22	1080	SND DAT: RET		THE NT BUFFER SHOULD HAVE BEEN LOADED TO 'NT' IN THE SERIAL PORT ISR.
		1081			
		1082	}	
		1083			
042C	853D3E	1084	RSNDVX: MOV	RESPCD,PRVXWR	OBTAIN CODE PREVIOUSLY WRITTEN TO VAX.
042E	753D01	1085	MOV	PRVXWR,#1H	SET THE 'PREVIOUS WRITE' LOCATION FOR
042F	752F00	1086	MOV	VAXCMD,#0H	NO-OPERATION, TO AVOID INFINITE LOOP.
0435	21F4	1087	AJMP	WRITVX	GO WRITE PREVIOUS CODE.
		1088			
		1089	}	
		1090			
0437	752200	1091			
043A	81D0	1092	CR48MV: MOV	STLL48,#0H	CLEAR THE 'MOTOR STALLED' FLAGS.
		1093	AJMP	PASSON	
		1094			
		1095	}	
		1096			
043C	E524	1097	MOVE48: MOV	A,MTRLNK	IF NO MOTORS ARE CONNECTED, SYSTEM IS IN
043E	7095	1098	JNZ	LDMOVS	DEBUG MODE, SO RESPOND TO EACH MOVE CODE
0440	753E33	1099	MOV	RESPCD,#RDYNXT	WITH A READY FOR NEXT MOVE CODE.
0443	31F4	1100	ACALL	WRITVX	
		1101			
		1102	}	
		1103			
0445	7811	1104	LDMOVS: MOV	R0,#RDBOT	THE MOVE FOR EACH MOTOR MUST BE WRITTEN
0447	75A018	1105	MOV	P2,#MTRAM1	INDIVIDUALLY TO THAT MOTOR'S SHARED RAM.
044A	752602	1106	MOV	BITLOC,#MTR1BT	START WITH MOTOR 1.
044D	7A07	1107	MOV	R2,#7H	
		1108			
044F	E590	1109	MOVLPO: MOV	A,P1	CHECK THIS MOTOR'S
0451	F4	1110	CPL	A	'SHARED RAM LOCKOUT' FLAG.
0452	5524	1111	ANL	A,MTRLNK	STAY IN THIS LOOP UNTIL ACCESS
0453	5524	1112	ANL	A,BITLOC	TO THE SHARED RAM IS GAINED.
0454	5526	1113	JNZ	MOVLPO	
0456	70F7	1114			
		1115	}	
		1116			
0458	7931	1117	MOV	R1,#NMMVSN	ONCE ACCESS IS GAINED, VARIOUS QUANTITIES
045A	08	1118	INC	R0	MUST BE DETERMINED. FIRST, PICK OFF THE
045B	E6	1119	MOV	A,@R0	SIGN OF THE MOVE FROM THE HIGH BYTE. (NOTE
045C	47F	1120	ANL	A,@7FH	THAT THE MOVE DISTANCE IS POSITIVE, WITH A
045E	C4	1121	XCH	A,@R0	SIGN BIT APPENDED AS THE HIGHEST BIT.)
045F	5480	1122	ANL	A,@80H	WRITE THE SIGN BIT TO THE 'NEXT MOVE SIGN'
0461	F3	1123	MOVX	@R1,A	LOCATION.
		1124			
0462	19	1125	DEC	R1	NEXT, WRITE THE HIGH BYTE OF THE MOVE
0463	E6	1126	MOV	A,@R0	WITH THE SIGN BIT REMOVED, TO THE 'NEXT MOVE
0464	F3	1127	MOVX	@R1,A	HIGH BYTE' LOCATION.
		1128			
0465	18	1129	DEC	R0	WRITE THE LOW BYTE OF THE MOVE
0466	19	1130	DEC	R1	TO THE 'NEXT MOVE LOW BYTE' LOCATION.
0467	E6	1131	MOV	A,@R0	
0468	F3	1132	MOVX	@R1,A	
		1133			
		1134	}	
		1135			
0469	792C	1136	MOV	R1,#NMMVNF	'OR' TOGETHER THE HIGHEST THREE BITS OF THE
046B	54E0	1137	ANL	A,@E0H	LOW BYTE AND ALL THE BITS OF THE HIGH BYTE
046D	08	1138	INC	R0	TO OBTAIN THE 'NEXT MOVE INFINITE' FLAG.
046E	48	1139	ORL	A,@R0	BY 'INFINITE' IS MEANT THAT THE MOVE IS
046F	F3	1140	MOVX	@R1,A	GREATER THAN 31 HOLES.
		1141			
		1142	}	
		1143			
0470	09	1144	INC	R1	'OR' TOGETHER BOTH BYTES OF THE MOVE
0471	18	1145	DEC	R0	TO OBTAIN THE 'NEXT MOVE RECEIVED' FLAG.
0472	46	1146	ORL	A,@R0	SO IF THE MOVE IS ZERO, NO MOVE APPEARS
0473	F3	1147	MOVX	@R1,A	TO BE RECEIVED TO THE 8748 SOFTWARE
0474	7005	1148	JNZ	NOTRDY	IF THE MOVE IS ZERO, THEN CLEARLY THIS MOTOR
0476	E526	1149	MOV	A,BITLOC	IS READY FOR THE NEXT MOVE, SO

0478 F4	1143	CPL A	CLEAR THE 'NOT READY' FLAG FOR THIS MOTOR.
0479 5221	1144	ANL R0Y48,A	
047B 08	1145		
047C 08	1146	NOTRDY: INC R0	INCREMENT POINTER R0 TWICE,
	1147	INC R0	TO LOW BYTE OF NEXT MOTOR'S MOVE.
047D E5A0	1148		
047F 2410	1149	MOV A,P2	COMPUTE SHARED RAM ENABLE ADDRESS FOR
0481 F5A0	1150	ADD A,#10H	THE NEXT MOTOR, AND ENABLE IT.
	1151	MOV P2,A	
0483 E526	1152	MOV A,BITLOC	COMPUTE THE BIT LOCATION CORRESPONDING TO
0485 F3	1153	RL A	THE NEXT MOTOR'S MOTOR NUMBER.
0486 F526	1154	MOV BITLOC,A	
	1155		
0488 DAC5	1156	DJNZ R2,MOVLPO	CONTINUE LOOPING UNTIL MOVES HAVE BEEN
	1157		WRITTEN TO ALL LINKED MOTORS.
	1158		
048A 75A000	1159		
	1160	MOV P2,#IDLE	CLEAR LAST ENABLE ADDRESS FROM PORT 2.
048D 753B07	1161		
0490 433B02	1162	MOV NRBUF,#7H	NOW REQUEST TO RECEIVE THE VELOCITY DATA,
0493 753B00	1163	ORL XMTFLG,#2H	AMOUNTING TO 7 BYTES.
0496 31F4	1164	MOV RESPD,#0H	
	1165	ACALL WRITVX	
	1166		
0498 E53C	1167	MOVLPI: MOV A,NR	WAIT IN THIS LOOP UNTIL
049A 453B	1168	ORL A,NRBUF	ALL 7 DATA BYTES
049C 70FA	1169	JNZ MOVLPI	HAVE BEEN RECEIVED.
	1170		
049E 7811	1171	MOV R0,#RDBOT	IT IS NECESSARY TO WRITE THE VELOCITY DATA
04A0 792E	1172	MOV R1,#RAMVEL	TO EACH MOTOR'S SHARED RAM, INDIVIDUALLY.
04A2 7A07	1173	MOV R2,#7H	START WITH MOTOR 1.
04A4 75A018	1174	MOV P2,#MTRAM1	
04A7 752602	1175	MOV BITLOC,#MTR1BT	
	1176		
04AA E590	1177	MOVLPI: MOV A,P1	CHECK THIS MOTOR'S
04AC F4	1178	CPL A	'SHARED RAM LOCKOUT' FLAG.
04AD 5524	1179	ANL A,MTRLNK	STAY IN THIS LOOP UNTIL ACCESS
04AF 5526	1180	ANL A,BITLOC	TO THIS MOTOR'S SHARED RAM IS GAINED.
04B1 70F7	1181	JNZ MOVLPI2	
	1182		
04B3 F6	1183	MOV A,R0	ONCE ACCESS IS GAINED, WRITE THE VELOCITY
04B4 F3	1184	ORL A	COMMAND TO ITS LOCATION IN SHARED RAM.
	1185		
04B5 E5A0	1186	MOV A,P2	COMPUTE THE NEXT MOTOR'S
04B7 2410	1187	ADD A,#10H	SHARED RAM ENABEL ADDRESS,
04B9 F5A0	1188	MOV P2,A	AND ENABLE IT.
	1189		
04BB E526	1190	MOV A,BITLOC	COMPUTE THE BIT LOCATION CORRESPONDING
04BD F3	1191	RL A	TO THE NEXT MOTOR'S MOTOR NUMBER.
04BE F526	1192	MOV BITLOC,A	
	1193		
04C0 08	1194	INC R0	INCREMENT R0 TO NEXT READ BUFFER LOCATION.
04C1 DAE7	1195	DJNZ R2,MOVLPI2	LOOP UNTIL ALL VELOCITY DATA HAS BEEN WRITTEN.
	1196		
04C3 75A000	1197	MOV P2,#IDLE	CLEAR LAST ENABLE ADDRESS FROM PORT 2.
04C6 852F30	1198	MOV GLOBL,VAXCMD	PASS 'MOVE' COMMAND ON TO THE 8748'S
04C9 B16F	1199	ACALL GLOBAL	USING THE 'GLOBAL WRITE' SUBROUTINE.
	1200		
04CB 753E77	1201	MOV RESPD,#RCVDAT	LOAD 'RECEIVED DATA' AS RESPONSE TO VAX.
04CE 41E8	1202	MOV PREWRI	
	1203		
	1204		
	1205		
	1206		
04D0 852F30	1207	PASSON: MOV GLOBL,VAXCMD	PASS ON THE HALT/GO/RESET/CLEAR CODE
04D3 B16F	1208	ACALL GLOBAL	TO 8748'S USING THE GLOBAL WRITE SUBROUTINE.
	1209		
04D5 852F3E	1210	MOV RESPD,VAXCMD	ECHO ORIGINAL VAX COMMAND AS RESPONSE CODE.
04D8 41E8	1211	MOV PREWRI	
	1212		
	1213		
04DA 75A018	1214	SHDRM: MOV P2,#MTRAM1	TO DO A 'SHARED RAM PEEK', IT IS NECESSARY

04DD	752602	1215	MOV	BITLOC,#MTR1BT	TO READ EACH MOTOR'S SHARED RAM INDIVIDUALLY.
04ED	7840	1216	MOV	R0,#RDBOT	START WITH MOTOR 1, WHOSE DATA WILL BE AT
04EE	A929	1217	MOV	R1,RAMADR	THE BOTTOM OF THE WRITE BUFFER.
04E4	7A07	1218	MOV	R2,#7	NOTE THAT ADDRESS TO BE READ IS IN R1.
04E6	E590	1219			
04E8	F4	1220	RMPLP1: MOV	A,P1	CHECK THIS MOTOR'S
04E9	5524	1221	CPL	A	'SHARED RAM LOCKOUT' FLAG.
04EB	5526	1222	ANL	A,MTRLNK	STAY IN THIS LOOP UNTIL ACCESS
04ED	70F7	1223	ANL	A,BITLOC	TO THE SHARED RAM IS GAINED.
		1224	JNZ	RMPLP1	
04EF	E3	1225	MOVX	A,R1	READ DATA FROM APPROPRIATE ADDRESS IN SHARED
04F0	F6	1226	MOV	R0,A	RAM INTO THIS MOTOR'S WRITE BUFFER LOCATION.
04F1	E526	1227	MOV	A,BITLOC	COMPUTE BIT LOCATION CORRESPONDING TO
04F3	23	1228	RL	A	NEXT MOTOR'S MOTOR NUMBER.
04F4	F526	1229	MOV	BITLOC,A	
04F6	E5A0	1230	MOV	A,P2	COMPUTE NEXT MOTOR'S
04F8	2410	1231	ADD	A,#10H	SHARED RAM ENABLE ADDRESS,
04FA	F5A0	1232	MOV	P2,A	AND ENABLE IT.
04FC	08	1233	INC	R0	INCREMENT WRITE BUFFER POINTER.
04FD	DAE7	1234	DJNZ	R2,RMPLP1	LOOP UNTIL ALL SHARED RAMS HAVE BEEN 'PEEKED'.
04FF	75A000	1235	MOV	P2,#IDLE	CLEAR LAST ENABLE ADDRESS FROM PORT 2.
0502	A629	1236	MOV	R0,RAMADR	ABOVE THE PEEK DATA IN THE WRITE BUFFER,
0504	08	1237	INC	R0	PUT THE ADDRESS THAT WAS PEEKED INTO,
0505	A62A	1238	MOV	R0,RNOCKL	THE LOW AND HIGH BYTES OF 'RHINO CLOCK',
0507	08	1239	INC	R0	AND THE COMMAND TO WHICH THIS DATA
0508	A62B	1240	MOV	R0,RNOCKH	IS THE RESPONSE.
050A	08	1241	INC	R0	
050B	76DD	1242	MOV	R0,#SHRPK	
050D	75390B	1243	MOV	NTBUFF,#0BH	LOAD 'NT BUFFER' FOR 11 BYTES.
0510	753E44	1244	MOV	RESPCD,#DAT	LOAD 'PEEK DATA READY' CODE AS RESPONSE TO VAX.
0513	41E8	1245	AJMP	PREHRI	
0515	E511	1246			
0517	F525	1247	COEF48: MOV	A,RDBOT	COEFFICIENTS ARE SENT FOR A PARTICULAR MOTOR.
0519	FA	1248	MOV	M1,RNMR,A	GET THE MOTOR NUMBER OF INTEREST
		1249	MOV	R2,A	IT IS ALSO USED IN COMPUTING BIT LOCATION.
051A	C4	1250	SWAP	A	COMPUTE SHARED RAM ENABLE ADDRESS
051B	4408	1251	ORL	A,#8H	OF THE MOTOR TO RECEIVE THE COEFFICIENTS.
051D	F5A0	1252	MOV	P2,A	
051F	7401	1253	MOV	A,#1H	COMPUTE THE BIT LOCATION CORRESPONDING
0521	23	1254	RL	A	TO THE MOTOR'S MOTOR NUMBER.
0522	DAFD	1255	DJNZ	R2,COELP1	
0524	F526	1256	MOV	BITLOC,A	
0526	E590	1257	COELP2: MOV	A,P1	CHECK THE MOTOR'S
0528	F4	1258	CPL	A	'SHARED RAM LOCKOUT' FLAG.
0529	5524	1259	ANL	A,MTRLNK	STAY IN THIS LOOP UNTIL ACCESS
052B	5526	1260	ANL	A,BITLOC	IS GAINED TO THE SHARED RAM.
052D	70F7	1261	JNZ	COELP2	
052F	7812	1262	MOV	R0,#RDBOT+1	ONCE ACCESS IS GAINED,
0531	7920	1263	MOV	R1,#CF1	WRITE EACH COEFFICIENT DATA BYTE
0533	7A02	1264	MOV	R2,#2	FROM THE READ BUFFER TO ITS
0535	7B08	1265	MOV	R3,#8	PROPER LOCATION IN SHARED RAM.
0537	F6	1266	MOV	A,R0	
0539	08	1267	MOVX	R0,A	
053B	08	1268	INC	R0	
053D	08	1269	INC	R0	
053F	DBFA	1270	DJNZ	R2,COELP3	
0541	7806	1271	MOV	R3,#8H	
0543	7920	1272	MOV	R1,#RIPPR	
0545	7C08	1273	MOV	R1,#8	
0547	DAF4	1274	DJNZ	R2,COELP3	

0543	E5A0	1287		
0545	6488	1288	MOV	A,P2
0547	F5A0	1289	XRL	A,#88H
		1290	MOV	P2,A
		1291		COMPUTE THE MOTOR'S
		1292		WRITE MAILBOX ENABLE ADDRESS,
		1293		AND ENABLE IT.
0549	E590	1294	COELP4: MOV	A,P1
054B	5524	1295	ANL	A,MTRLNK
054D	5526	1296	ANL	A,BITLOC
054F	6013	1297	JZ	COEWRT
		1298		CHECK THAT THE MOTOR'S WRITE MAILBOX
		1299		IS NOT FULL.
0551	53A070	1299		
0554	E590	1300	ANL	P2,#70H
0556	5524	1301	MOV	A,P1
0558	5526	1302	ANL	A,MTRLNK
055A	6003	1303	ANL	A,BITLOC
055C	E2	1304	JZ	NOREAD
055D	31A2	1305	MOVX	A,@R0
		1306	ACALL	DCD48
		1307		IF IT IS FULL, ENABLE THE MOTOR'S
		1308		READ MAILBOX, AND SEE IF IT IS FULL.
055F	43A080	1309	NOREAD: ORL	P2,#80H
0562	A149	1310	AJMP	COELP4
		1311		ENABLE THE MOTOR'S WRITE MAILBOX AGAIN.
		1312		GO TRY WRITING AGAIN.
0564	74FF	1313	COEWRT: MOV	A,#KFF
0566	F2	1314	MOVX	@R0,A
		1315		IF WRITE MAILBOX IS NOT FULL, THEN PUT
		1316		'COEFFICIENTS' CODE INTO IT.
0567	75A000	1317	MOV	P2,#IDLE
056A	753E77	1318	MOV	RESPCD,#RCV DAT
056D	41E8	1319	AJMP	PREWR1
		1320		CLEAR ENABLE ADDRESS FROM PORT 2.
		1321		LOAD 'RECEIVED DATA' AS RESPONSE TO VAX.
		1322		
		1323	
		1324		GLOBAL WRITE SUBROUTINE:
		1325		
		1326		PROVIDE: CODE DESTINED FOR ALL 8748'S IN
		1327		LOCATION 'GLOBL'.
		1328		RETURNS: CODE IS WRITTEN TO ALL 8748
		1329		WRITE MAILBOXES.
		1330		CHANGES: P2,R0,R4,ACCUM,PSW
		1331		CALLS: 'RESPOND TO 8748S' ('RESPND')
		1332		CALLED BY: 'DECODE 8748' ('DCD48')
		1333		(VECTORS INTO CLRWR2)
		1334		'DECODE VAX COMMAND' ('DCOVAX')
		1335		'COMPUTE VELOCITIES' ('VELOCS')
056F	75A080	1336	GLOBAL: MOV	P2,#GLOBLWR
0572	E590	1337	MOV	A,P1
0574	5524	1338	ANL	A,MTRLNK
0576	600D	1339	JZ	CLRWR2
		1340		IF ALL WRITE MAILBOXES ARE EMPTY,
		1341		THEN GO DO THE GLOBAL MAILBOX WRITE.
0578	75A000	1342	MOV	P2,#IDLE
057B	E590	1343	MOV	A,P1
057D	5524	1344	ANL	A,MTRLNK
057F	60EE	1345	JZ	GLOBAL
0581	3180	1346	GLOBAL	RESPND
0583	A16F	1347	AJMP	GLOBAL
		1348		OTHERWISE, SINCE AT LEAST ONE OF THE WRITE
		1349		MAILBOXES IS FULL, SEE IF ANY OF THE READ
		1350		MAILBOXES ARE FULL. IF SO, IT COULD BE THAT
		1351		SOME 8748 IS WAITING TO WRITE, AND BOTH IT
		1352		AND THE 8751 WOULD WAIT FOREVER IF ONE OF
		1353		THE MAILBOXES DOES NOT GET READ.
0585	E530	1354	CLRWR2: MOV	A,GLOBL
0587	F2	1355	MOVX	@R0,A
0588	75A000	1356	MOV	P2,#IDLE
		1357		IF ALL THE WRITE MAILBOXES ARE EMPTY,
		1358		WRITE THE CODE TO ALL MAILBOXES.
		1359		CLEAR THE ENABLE ADDRESS FROM PORT 2.
058B	7830	1360	MOV	R0,#PRVMTR
058D	7C07	1361	MOV	R4,#7H
058F	08	1362	INC	R0
0590	F6	1363	MOV	@R0,A
0591	DCFC	1364	DJNZ	R4,GLOBLP1
0593	22	1365	RET	

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SERIAL PORT INTERRUPT SERVICE SUBROUTINE:

```

0594 C0D0
0596 C0F0
0598 D2D3
059A 209809
059D 30992F
05A0 C299
05A2 5101
05A4 C131
05A6 C298
05A8 F83C
05AA 6025
05AC 2410
05AE F8
05AF A699
05B1 D53C1B
05B4 85102E
05B7 751000
05BA E52E
05BC 64DD
05BE 600C
05C0 E52E
05C2 6444
05C4 6006
05C6 E52E
05C8 6433
05CA 7065
05CC 851129
05CF C131
05D1 859910
05D4 E510
05D6 60F7
05D8 6477
05DA 700B
05DC 85293A
05DF 752900
05E2 751000
05E5 C12A

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```

SRLISR: PUSH PSW
        PUSH ACC
        SETB PSW.3
        JB SCON.0,RCVR
        JNB SCON.1,SRLJMP
        CLR SCON.1
        ACALL SEROUT
        AJMP SRLFIN
RCVR: CLR SCON.0
      MOV A,NR
      JZ SRLCOD
SRLDAT: ADD A,#SRRDBF
        MOV R0,A
        MOV @R0,SBUF
NODATA: DJNZ NR,SRLJMP
        MOV VAXBUF,SRRDBF
        MOV SRRDBF,#0
        MOV A,VAXBUF
        XRL A,#SHRPK
        JZ ADRLCH
        MOV A,VAXBUF
        XRL A,#PK51
        JZ ADRLCH
        MOV A,VAXBUF
        XRL A,#PK48
        JNZ SRLFIN
ADRLCH: MOV RAMADR,RDBOT
SRLJMP: AJMP SRLFIN
SRLCOD: MOV SRRDBF,SBUF
        MOV A,SRRDBF
        JZ SRLJMP
        XRL A,#SNDVX
        JNZ NOTVAX
        MOV NT,NTBUFF
        MOV NT@,NTBUFF
        MOV SRRDBF,#0H
        AJMP SRLOUT

```

```

}
} .....
}
} SERIAL PORT INTERRUPT SERVICE SUBROUTINE:
}
} PROVIDE: NONE
}
} RETURNS: PROCESSES SERIAL INPUT BYTE, OR
} SERVICES SERIAL OUTPUT BUFFER.
} USES VALUE OF NT (NR) TO DETERMINE
} IF OUTPUT (INPUT) BYTE IS CODE OR
} DATA. RESPONDS DIRECTLY TO INPUT
} CODES THAT WILL BE FOLLOWED BY DATA.
}
} CHANGES: SCON.0, SCON.1, WRBUF, NT, NR,
} TRFLAG, VAXCMD
}
} CALLS: 'SERIAL OUTPUT' ('SEROUT')
}
} CALLED BY: INTERRUPT ZERO FALLING EDGE
}
} SAVE PROGRAM STATUS WORD ON STACK.
} SAVE ACCUMULATOR CONTENTS ON STACK.
} SELECT REGISTER BANK 1.
}
} IF SERIAL PORT RECEIVE FLAG IS SET,
} GO SERVICE THE SERIAL PORT RECEIVER.
}
} IF NEITHER FLAG IS SET, SPURIOUS INTERRUPT.
} ELSE, THE SERIAL PORT TRANSMIT FLAG IS SET,
} SO GO SERVICE THE SERIAL PORT TRANSMITTER.
}
} CLEAR 'RECEIVER INTERRUPT' BIT.
} CHECK NUMBER OF DATA BYTES LEFT TO RECEIVE.
} IF ZERO, INCOMING BYTE IS CODE, NOT DATA.
}
} COMPUTE CURRENT READ BUFFER LOCATION,
} AND MOVE THE INCOMING DATA INTO IT.
}
} DECREMENT RECEIVE DATA BYTE COUNT, AND IF
} NO DATA IS LEFT TO RECEIVE, PUT THE ORIGINAL
} CODE INTO THE VAX BUFFER FOR PROCESSING.
}
} SOME OF THE CODES FROM VAX ARE ACCOMPANIED
} BY AN ADDRESS TO BE PEEKED OR POKED.
} IF THE CODE IS ONE OF THOSE, GO MOVE THAT
} ADDRESS FROM THE BOTTOM OF THE READ BUFFER
} TO A SPECIAL LOCATION (LCHADR).
} IF IT IS NOT ONE OF THOSE CODES, THEN THE
} ROUTINE IS FINISHED.
}
} MOVE INCOMING CODE FROM SERIAL PORT RECEIVER
} BUFFER INTO THE 'INCOMING CODE' BUFFER.
} IF CODE IS NO-OP, PROCESSING IS COMPLETE.
}
} IF INCOMING CODE IS THE 'SEND TO VAX' CODE,
} THEN LOAD THE PENDING NUMBER OF DATA BYTES
} TO BE TRANSMITTED (NTBUFF) INTO 'NT'. THE
} NUMBER TO BE TRANSMITTED IMMEDIATELY
} 'SEND TO VAX' CODE IS FULLY ANSWERED BY
} DATA TRANSMISSION, SO CLEAR COMMAND.
}
} IF INCOMING CODE IS NOT 'SEND TO VAX':

```

```

05E7 740D
05E9 6510
05EB 7005
05ED 753B01
05F0 C127

05F2 74AA
05F4 6510
05F6 7005
05F8 753B0E
05FB C127

05FD 74FF
05FF 6510
0601 7005
0603 753B0F
0606 C127

0608 7444
060A 6510
060C 7005
060E 753B01
0611 C127

0613 7433
0615 6510
0617 7005
0619 753B01
061C C127

061E 7411
0620 6510
0622 7090
0624 753B01

0627 433802
062A E538
062C 30E002
062F 5101

0631 D0D0
0633 D0D0
0635 32

0636 C0D0
0638 C0E0

063A 052A
063C E52A
063E 7002
0640 052B

0642 E528
0644 7003

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NOTVAX: MOV A,#SHRPK
XRL A,SRRDBF
JNZ NOTRMP
MOV NRBUFF,#1H
AJMP SRLXMT

NOTRMP: MOV A,#MOVE
XRL A,SRRDBF
JNZ NOTMOV
MOV NRBUFF,#0EH
AJMP SRLXMT

NOTMOV: MOV A,#KFF
XRL A,SRRDBF
JNZ NOTKFF
MOV NRBUFF,#0FH
AJMP SRLXMT

NOTKFF: MOV A,#PK51
XRL A,SRRDBF
JNZ NOT5PK
MOV NRBUFF,#1H
AJMP SRLXMT

NOT5PK: MOV A,#PK48
XRL A,SRRDBF
JNZ NOT4PK
MOV NRBUFF,#1H
AJMP SRLXMT

NOT4PK: MOV A,#ECI
XRL A,SRRDBF
JNZ NODATA
MOV NRBUFF,#1H

SRLXMT: ORL XMTFLG,#2H
SRLOUT: MOV A,XMTFLG
JNB ACC.0,SRLFIN
ACALL SEROUT

SRLFIN: POP ACC
POP PSW
RETI

```

```

} SOME OF THE INCOMING CODES WILL BE FOLLOWED
} BY DATA. DETERMINE IF IT THE CODE IS GOING
} TO BE FOLLOWED BY DATA, AND IF SO, LOAD THE
} NUMBER OF EXPECTED BYTES OF DATA INTO 'NR'.
} THE 'SHARED RAM PEEK' CODE
} IS FOLLOWED BY A 1-BYTE ADDRESS.
}
} THE 'MOVE' CODE IS FOLLOWED BY
} 14 BYTES OF DATA.
}
} THE 'COEFFICIENTS' CODE IS
} FOLLOWED BY 15 BYTES OF DATA.
}
} THE '8751 PEEK' CODE
} IS FOLLOWED BY A 1-BYTE ADDRESS.
}
} THE '8748 PEEK/POKE' CODE
} IS FOLLOWED BY A 1-BYTE ADDRESS.
}
} THE 'INTERRUPT COMMAND ENABLE'
} IS FOLLOWED BY A 1-BYTE COMMAND CODE.
}
} IN CASE THE CODE IS FOLLOWED BY DATA,
} SET THE 'ASK FOR DATA' FLAG.
} IF 'TRANSMITTER IDLE' FLAG IS SET,
} CALL THE 'SERIAL OUTPUT' SUBROUTINE.
}
} RESTORE ACCUMULATOR.
} RESTORE PROGRAM STATUS WORD.
} RETURN FROM INTERRUPT.
}
}.....
}.....
} INTERRUPT ZERO SERVICE SUBROUTINE:
} PROVIDE: NOTHING.
} RETURNS: RHINO CLOCK IS INCREMENTED BY 1.
} INTERRUPT COMMAND IS PLACED IN
} INTERRUPT COMMAND BUFFER.
} CHANGES: RNOCKL,RNOCKH,INTCDB
} CALLS: NONE
} CALLED BY: INTERRUPT ZERO ACTIVE
}
} SAVE PROCESSOR STATUS WORD ON STACK.
} SAVE ACCUMULATOR CONTENTS ON STACK.
} INCREMENT THE TWO-BYTE RHINO CLOCK.
} NOTE THAT THE HIGH BYTE IS INCREMENTED
} ONLY IF THE LOW BYTE INCREMENTS TO ZERO,
} THUS GENERATING A CARRY TO THE HIGH BYTE.
}
} IF AN 8748 RAM PEEK IS IN PROGRESS,
} DO NOT MOVE THE INTERRUPT COMMAND

```

0646 852C2D
 0649 D0E0
 064B D0D0
 064D 32

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```

MOV   INTCDB,INTCMD ; INTO THE INTERRUPT COMMAND BUFFER.
INTFIN: POP ACC ; RECOVER ACCUMULATOR CONTENTS FROM STACK.
      POP PSW ; RECOVER PROCESSOR STATUS WORD FROM STACK.
      RETI ;
;.....
;.....
      END ;
  
```

XREF SYMBOL TABLE LISTING

NAME	TYPE	VALUE	ATTRIBUTES AND REFERENCES
ABS L P1	C ADDR	03FDH	A 1043# 1047 1066
ABS REG	C ADDR	03F1H	A 773 1036#
ACC	D ADDR	00E0H	A 265 639 692 865 966 1005 1383 1468 1471
ADRLCH	C ADDR	05CCH	A 1408 1411 1415#
AGO	NUMB	00CCH	A 27# 474
BAUD 48	NUMB	00FAH	A 178# 264
BAUD 96	NUMB	00FDH	A 175# 266
BFC 48	C ADDR	0041H	A 265# 267#
BFC F IN	C ADDR	007AH	A 297# 306#
BFC IN 0	C ADDR	002CH	A 226 254#
BFC L P1	C ADDR	0032H	A 259# 260
BFC L P2	C ADDR	0048H	A 276# 299
BFC L P3	C ADDR	0051H	A 279# 304
BIT LOC	NUMB	0026H	A 115# 277 281 291 301 303 401 409 415 417
BK COM 1	C ADDR	00E7H	A 510 514 526 528 585 597 605 609 614
CF 1	NUMB	0020H	A 869 876 882 884 921 926 942 948 993 1001
CF 2	NUMB	0021H	A 1017 1019 1037 1046 1060 1062 1105
CF 3	NUMB	0022H	A 1111 1142 1153 1155 1175 1180 1190 1192
CF 4	NUMB	0023H	A 1215 1223 1229 1231 1267 1272 1294 1300
CHK CMD	C ADDR	0166H	A 382 385# 472
CLR R 2	C ADDR	0569H	A 188# 1276
CLR R 3	C ADDR	0580H	A 189#
CLR R 4	C ADDR	0581H	A 190#
CLR R 5	C ADDR	0582H	A 191#
CLR R 6	C ADDR	0583H	A 464#
CLR R 7	C ADDR	0584H	A 470#
CLR R 8	C ADDR	0585H	A 606# 1349#
CLR R 9	C ADDR	0586H	A 607# 1349#
CLR R 10	C ADDR	0587H	A 608# 1349#
CLR R 11	C ADDR	0588H	A 609# 1349#
CLR R 12	C ADDR	0589H	A 610# 1349#
CLR R 13	C ADDR	058AH	A 611# 1349#
CLR R 14	C ADDR	058BH	A 612# 1349#
CLR R 15	C ADDR	058CH	A 613# 1349#
CLR R 16	C ADDR	058DH	A 614# 1349#
CLR R 17	C ADDR	058EH	A 615# 1349#
CLR R 18	C ADDR	058FH	A 616# 1349#
CLR R 19	C ADDR	0590H	A 617# 1349#
CLR R 20	C ADDR	0591H	A 618# 1349#
CLR R 21	C ADDR	0592H	A 619# 1349#
CLR R 22	C ADDR	0593H	A 620# 1349#
CLR R 23	C ADDR	0594H	A 621# 1349#
CLR R 24	C ADDR	0595H	A 622# 1349#
CLR R 25	C ADDR	0596H	A 623# 1349#
CLR R 26	C ADDR	0597H	A 624# 1349#
CLR R 27	C ADDR	0598H	A 625# 1349#
CLR R 28	C ADDR	0599H	A 626# 1349#
CLR R 29	C ADDR	059AH	A 627# 1349#
CLR R 30	C ADDR	059BH	A 628# 1349#
CLR R 31	C ADDR	059CH	A 629# 1349#
CLR R 32	C ADDR	059DH	A 630# 1349#
CLR R 33	C ADDR	059EH	A 631# 1349#
CLR R 34	C ADDR	059FH	A 632# 1349#
CLR R 35	C ADDR	05A0H	A 633# 1349#
CLR R 36	C ADDR	05A1H	A 634# 1349#
CLR R 37	C ADDR	05A2H	A 635# 1349#
CLR R 38	C ADDR	05A3H	A 636# 1349#
CLR R 39	C ADDR	05A4H	A 637# 1349#
CLR R 40	C ADDR	05A5H	A 638# 809 1251
CLR R 41	C ADDR	05A6H	A 639# 809 1251
CLR R 42	C ADDR	05A7H	A 640# 809 1251
CLR R 43	C ADDR	05A8H	A 641# 809 1251
CLR R 44	C ADDR	05A9H	A 642# 809 1251
CLR R 45	C ADDR	05AAH	A 643# 809 1251
CLR R 46	C ADDR	05ABH	A 644# 809 1251
CLR R 47	C ADDR	05ACH	A 645# 809 1251
CLR R 48	C ADDR	05ADH	A 646# 809 1251
CLR R 49	C ADDR	05AEH	A 647# 809 1251
CLR R 50	C ADDR	05AFH	A 648# 809 1251
CLR R 51	C ADDR	05B0H	A 649# 809 1251
CLR R 52	C ADDR	05B1H	A 650# 809 1251
CLR R 53	C ADDR	05B2H	A 651# 809 1251
CLR R 54	C ADDR	05B3H	A 652# 809 1251
CLR R 55	C ADDR	05B4H	A 653# 809 1251
CLR R 56	C ADDR	05B5H	A 654# 809 1251
CLR R 57	C ADDR	05B6H	A 655# 809 1251
CLR R 58	C ADDR	05B7H	A 656# 809 1251
CLR R 59	C ADDR	05B8H	A 657# 809 1251
CLR R 60	C ADDR	05B9H	A 658# 809 1251
CLR R 61	C ADDR	05BAH	A 659# 809 1251
CLR R 62	C ADDR	05BBH	A 660# 809 1251
CLR R 63	C ADDR	05BCH	A 661# 809 1251
CLR R 64	C ADDR	05BDH	A 662# 809 1251
CLR R 65	C ADDR	05BEH	A 663# 809 1251
CLR R 66	C ADDR	05BFH	A 664# 809 1251
CLR R 67	C ADDR	05C0H	A 665# 809 1251
CLR R 68	C ADDR	05C1H	A 666# 809 1251
CLR R 69	C ADDR	05C2H	A 667# 809 1251
CLR R 70	C ADDR	05C3H	A 668# 809 1251
CLR R 71	C ADDR	05C4H	A 669# 809 1251
CLR R 72	C ADDR	05C5H	A 670# 809 1251
CLR R 73	C ADDR	05C6H	A 671# 809 1251
CLR R 74	C ADDR	05C7H	A 672# 809 1251
CLR R 75	C ADDR	05C8H	A 673# 809 1251
CLR R 76	C ADDR	05C9H	A 674# 809 1251
CLR R 77	C ADDR	05CAH	A 675# 809 1251
CLR R 78	C ADDR	05CBH	A 676# 809 1251
CLR R 79	C ADDR	05CAH	A 677# 809 1251
CLR R 80	C ADDR	05CCH	A 678# 809 1251

RESPND	. . .	C	ADDR	0180H	A	1201	1209	1251	1312	
RNPLP1	. . .	C	ADDR	04E6H	A	348	509#	1345		
RNCKKH	. . .		NUMB	002BH	A	1220#	1224	1238		
RNOCKL	. . .		NUMB	002AH	A	121#	431	981	1025	1070
RSET48	. . .		NUMB	0020H	A	120#	330	429	979	1023
RSND48	. . .	C	ADDR	01D1H	A	107#	271	293	294	296
RSNDVX	. . .	C	ADDR	042CH	A	571	593#		358	451
RSNRQ1	. . .	C	ADDR	01C4H	A	779	1086#			606
RSNRQ2	. . .	C	ADDR	029FH	A	567	583#	586		
SBUF	. . .	D	ADDR	0099H	A	751	808#			
SCON	. . .	D	ADDR	0098H	A	326	704	711	1400	1419
SEROUT	. . .	C	ADDR	0201H	A	311	317	319	320	1386
SETFLG	. . .	C	ADDR	0240H	A	647	681#	1391	1469	1389
SHRDRM	. . .	C	ADDR	04DAH	A	692	716#			1390
SHRPK	. . .		NUMB	00DDH	A	794	1214#			1394
SHRTOV	. . .		NUMB	003CH	A	59#	1248	1407	1431	
SND51	. . .		NUMB	0011H	A	218#				
SNDAT	. . .	C	ADDR	042BH	A	6#	694			
SNDHLT	. . .	C	ADDR	01DBH	A	776	1081#			
SNDVX	. . .		NUMB	0077H	A	600#	607			
S	. . .	D	ADDR	0081H	A	49#	1423			
SEED	. . .		NUMB	002AH	A	306				
SRLCOD	. . .	C	ADDR	05D1H	A	201#	995			
SRLDAT	. . .	C	ADDR	05ACH	A	1396	1419#			
SRLFIN	. . .	C	ADDR	0631H	A	1398#				
SRLISR	. . .	C	ADDR	0594H	A	1392	1414	1416	1468	1471#
SRLJMP	. . .	C	ADDR	05CFH	A	243	1582#			
SRLOUT	. . .	C	ADDR	062AH	A	1389	1402	1416#	1421	
SRLXMT	. . .	C	ADDR	0627H	A	1428	1467#			
SRRDBF	. . .		NUMB	0010H	A	1435	1441	1447	1453	1459
						103#	1398	1403	1404	1419
						1438	1444	1450	1456	1462
						142#	686	699	702	704
						364	457#	705	708	
SRHRBF	. . .		NUMB	003FH	A	147#	306			
STAL48	. . .	C	ADDR	014DH	A	573	597#			
STKBAS	. . .		NUMB	004FH	A	359	362#			
STL48	. . .	C	ADDR	01D4H	A	359	362#			
STLCHK	. . .	C	ADDR	00BEH	A	109#	362	598	1093	
STLL48	. . .		NUMB	0022H	A	458	465#			
STLRSP	. . .	C	ADDR	015CH	A	216#				
STRTPW	. . .		NUMB	003AH	A	315	332			
TCON	. . .	D	ADDR	0088H	A	314				
TH1	. . .	D	ADDR	008DH	A	313				
TMOD	. . .	D	ADDR	0089H	A	833	836	839	842	846#
VALCMD	. . .	C	ADDR	02F2H	A	126#	378	379	467	468
VAXBUF	. . .		NUMB	002EH	A	127#	376	378	381	393
VAXCMD	. . .		NUMB	002FH	A	745	749	753	802	850
						1076	1088	1198	1206	1209
						15#	812			
VDT	. . .		NUMB	0055H	A	1005	1010#			
VLC2S	. . .	C	ADDR	03D2H	A	998#	1002	1021		
VLCPL1	. . .	C	ADDR	03C1H	A	770	992#			
VLCREQ	. . .	C	ADDR	03B5H	A	46#	838			
VRG	. . .		NUMB	0055H	A	144#	403	969	973	976
WRB0T	. . .		NUMB	0040H	A	639	647#			994
WRTRDY	. . .	C	ADDR	01FEH	A	371	441	452	463	483
WRITVX	. . .	C	ADDR	01F4H	A	1089	1101	1165	638#	642
						145#			823	852
						133#	638	681	691	693
WRTOP	. . .		NUMB	004FH	A	716	903	1163	1466	1467
XMTFLG	. . .		NUMB	0038H	A					

REGISTER BANK(S) USED: 0, TARGET MACHINE(S): 8051

ASSEMBLY COMPLETE, NO ERRORS FOUND

APPENDIX X. LISTING OF THE 8748 ASSEMBLY LANGUAGE PROGRAM

This program was assembled on the Intel MDS-80 Development System, using the MCS-48/UPI-41 Macro Assembler, Version 3.0. The cross-reference and no-page-numbering options were specified.

LOC	OBJ	LINE	SOURCE	STATEMENT	
		1		COMMUNICATION CODES FROM 8748 TO 8751:	
		2		-----	
		3			
		4	NOP	EQU 00H	NO OPERATION CODE.
		5			
0088		6	OVR	EQU 088H	RESEND REQUEST CODE.
0099		7	MTRSTL	EQU 099H	MOTOR STALLED CODE.
00AA		8	HDWRST	EQU 0AAH	HARDWARE RESET UNDERWAY CODE.
00BB		9	RDYNT	EQU 0BBH	READY FOR NEXT MOVE CODE.
00CC		10	RAMPK	EQU 0CCH	INTERNAL RAM PEEK COMPLETE.
		11			
		12			
		13		
		14		COMMUNICATION CODES FROM 8751 TO 8748:	
		15		-----	
		16			
		17	NOP	EQU 00H	NO OPERATION
		18	OVR	EQU 088H	REQUEST TO SEND PREVIOUS CODE
		19	CRM	EQU 099H	CLEAR UNEXECUTED MOVES
		20	MOV	EQU 0AAH	GET NEXT MOVE AND VELOCITY FROM RAM
		21	HLT	EQU 0BBH	HALT MOTOR
		22	AGO	EQU 0CCH	GO (EXECUTE MOVES)
		23	PK48	EQU 0DDH	INTERNAL RAM PEEK/POKE.
		24	RAP	EQU 0EEH	RESET ABSOLUTE POSITION
		25	KFF	EQU 0FFH	GET CONTROL COEFFICIENTS FROM RAM
		26			
		27		
		28			
		29		DEVICE ADDRESSES:	
		30		-----	
		31		UPPER 3 BITS TO 3 X 8 DECODER, THROUGH PORT 2)	
		32			
0000		33	IDLE	EQU 0H	IDLE (NO DEVICE ADDRESSED).
		34			
0020		35	CLCKHI	EQU 20H	CLOCK HIGH BYTE ADDRESS.
0060		36	CLCKLO	EQU 60H	CLOCK LOW BYTE ADDRESS.
		37			
0080		38	MLBXEN	EQU 80H	MAILBOX ENABLE ADDRESS.
00A0		39	PWLTEN	EQU 0A0H	PULSEWIDTH LATCH ENABLE ADDRESS.
		40			
00C0		41	XRAMEN	EQU 0C0H	EXTERNAL RAM ENABLE.
00E0		42	BITDAT	EQU 0E0H	BIT DATA LATCH OUTPUT ENABLE ADDRESS.
		43			
		44		
		45			
		46		INTERNAL (INT) AND EXTERNAL (EXT) LOCATION SYMBOLS:	
		47		-----	
		48			
0020		49	CF1	EQU 20H	(#32) INT/EXT COEFFICIENT FOR
		50			2-31 HOLES/SECOND (HPS).
0021		51	CF2	EQU 21H	(#33) INT/EXT COEFFICIENT FOR 32-63 HPS.
0022		52	CF3	EQU 22H	(#34) INT/EXT COEFFICIENT FOR 64-127 HPS.
0023		53	CF4	EQU 23H	(#35) INT/EXT COEFFICIENT FOR 128+ HPS.
		54			
0024		55	MG1	EQU 24H	(#36) INT/EXT MAX VELOCITY ERROR FOR 2-31 HPS.
0025		56	MG2	EQU 25H	(#37) INT/EXT MAX VELOCITY ERROR FOR 32-63 HPS.
0026		57	MG3	EQU 26H	(#38) INT/EXT MAX VELOCITY ERROR FOR 64-127 HPS.
0027		58	MG4	EQU 27H	(#39) INT/EXT MAX VELOCITY ERROR FOR 128+ HPS.
		59			
0028		60	STPCNT	EQU 28H	(#40) INT NUMBER OF MOTOR STOP INTERRUPTS
		61			SINCE LAST MOTION OF MOTOR.
		62			
0028		63	RAMDAT	EQU 28H	(#40) EXT LOCATION OF DATA FOR PEEK/POKE.
0029		64	RAMADR	EQU 29H	(#41) INT/EXT LOC OF ADDRESS FOR PEEK/POKE.
		65			
002A		66	SPEED	EQU 2AH	(#42) INT SPEED.
		67			EXT VELOCITY (SIGNED).

```

002B      68 QHTAIL      EQU    2BH      ; (#43) INT QUARTER-HOLE TAIL LOCATION.
          69           ;              (NUMBER OF QUARTER-HOLES
          70           ;              SINCE LAST POSITION UPDATE,
          71           ;              RELATIVE TO COMMAND DIRECTION)
          72           ;
          73           ;
002C      74 NXMVNF     EQU    2CH      ; (#44) INT/EXT 'NEXT MOVE INFINITE' FLAG.
002D      75 RCVDNM     EQU    2DH      ; (#45) INT/EXT 'RECEIVED NEXT MOVE' FLAG.
          76           ;
002E      77 NXTVEL     EQU    2EH      ; (#46) INT/EXT NEXT VELOCITY LOCATION.
002F      78 NXMVLO     EQU    2FH      ; (#47) INT/EXT NEXT MOVE LOW BYTE LOCATION.
0030      79 NXMVHI     EQU    30H      ; (#48) INT/EXT NEXT MOVE HIGH BYTE LOCATION.
0031      80 NXMVSN     EQU    31H      ; (#49) INT/EXT NEXT MOVE SIGN LOCATION.
          81           ;
0032      82 PRSVEL     EQU    32H      ; (#50) INT PRESENT VELOCITY LOCATION.
0033      83 PRMVLO     EQU    33H      ; (#51) INT PRESENT MOVE LOW BYTE LOCATION.
          84           ; EXT PRESENT ABSOLUTE POSITION LOW BYTE.
0034      85 PRMVHI     EQU    34H      ; (#52) INT PRESENT MOVE HIGH BYTE LOCATION.
          86           ; EXT PRESENT ABSOLUTE POSITION HIGH BYTE.
0035      87 PRMVSN     EQU    35H      ; (#53) INT PRESENT MOVE SIGN LOCATION.
          88           ;
0036      89 PLSMTH     EQU    36H      ; (#54) INT PULSEWIDTH LOCATION.
0037      90 SIGNPW     EQU    37H      ; (#55) INT PULSEWIDTH SIGN.
          91           ;
0038      92 GRIPPR     EQU    38H      ; (#56) INT/EXT GRIPPER (CLOSED) PULSEWIDTH
          93           ;
0039      94 HYSTPW     EQU    39H      ; (#57) INT/EXT HYSTERESIS PULSEWIDTH.
003A      95 STRTPW     EQU    3AH      ; (#58) INT/EXT STARTING PULSEWIDTH.
          96           ;
003B      97 LONGOV     EQU    3BH      ; (#59) INT/EXT LONG OVERSHOOT PULSEWIDTH.
003C      98 SHRTOV     EQU    3CH      ; (#60) INT/EXT SHORT OVERSHOOT PULSEWIDTH.
          99           ;
003F      100 DELTAV    EQU    3FH      ; (#63) INT CHANGE IN VELOCITY SINCE LAST INTERRUPT.
          101           ;
          102           ;
          103           ;
          104           ;
          105           ;
          106           ;
          107           ;
          108           ;
          109           ;
          110           ;
          111           ;
          112           ;
          113           ;
          114           ;
          115           ;
          116           ;
          117           ;
          118           ;
          119           ;
          120           ;
          121           ;
          122           ;
          123           ;
          124           ;
          125           ;
          126           ;
          127           ;
          128           ;
          129           ;
          130           ;
          131           ;
          132           ;
          133           ;
          134           ;
          135           ;
          136           ;
          137           ;
          138           ;
          139           ;

```

REGISTER BANK ZERO ASSIGNMENTS

R0 - R5 ARE WORKING REGISTERS.
R6 HOLDS PREVIOUS CODE WRITTEN TO 8751.
('PREVIOUS WRITE BUFFER')
R7 HOLDS CODE TO BE WRITTEN TO 8751 ('WRITE BUFFER').

REGISTER BANK ONE ASSIGNMENTS

R0 - R1 ARE WORKING REGISTERS.
R2 HOLDS CURRENT QUARTER-HOLE MOVE.
R3-R4 ARE WORKING REGISTERS.
R5 HOLDS CURRENT VELOCITY SET POINT.
R6 HOLDS VARIOUS FLAGS:
BIT ZERO = 'RELATIVE DIRECTION' FLAG
(DIRECTION RELATIVE TO COMMAND)
BIT TWO = 'NEW MOTION' FLAG
(MOTOR STOPPED JUST PRIOR TO THIS INTERRUPT)
BIT FOUR = 'PREVIOUS ENCODER POSITION 0,0' FLAG
(MOTOR JUST LEFT 0,0 POSITION)
BIT SEVEN = 'ABSOLUTE DIRECTION' FLAG
(ABSOLUTE DIRECTION OF MOTOR MOTION)

```

140 }
141 } R7 HOLDS VARIOUS FLAGS:
142 } BIT ZERO = 'REVERSAL SINCE LAST UPDATE' FLAG
143 } (DIRECTION REVERSED AFTER LAST POSITION UPDATE)
144 }
145 } BIT ONE = 'MOTOR STOPPED' FLAG
146 } (MOTOR CURRENTLY STOPPED)
147 }
148 } BIT TWO = RESERVED (MUST BE ZERO).
149 }
150 } BIT THREE = 'PRESENT ENCODER POSITION 0,0' FLAG
151 } (VALID ONLY AFTER EXECUTION OF
152 } POSITION UPDATE SUBROUTINE)
153 }
154 } BIT FIVE = LIMIT SWITCH STATE.
155 } BIT SIX = PRESENT STATE OF ENCODER BIT ONE.
156 } BIT SEVEN = PRESENT STATE OF ENCODER BIT ZERO.
157 }
158 }
159 } .....
160 } ASSIGNMENT OF MICROPROCESSOR FLAGS:
161 } -----
162 }
163 } FLAG ZERO (F0) = 'GO' FLAG
164 } (CLEAR INDICATES MOTOR IS HALTED)
165 }
166 } FLAG ONE (F1) = 'STALL' FLAG
167 } (SET INDICATES MOTOR IS STALLED)
168 }
169 } .....
170 } MISCELLANEOUS BIT MASKS AND VALUES:
171 } -----
172 }
173 }
174 } 0080 SGNMSK EQU 80H ; BIT MASK TO ISOLATE SIGN BIT.
175 } 00E0 MASK32 EQU 0E0H ; BIT MASK TO ISOLATE TOP 3 BITS.
176 } 00FF ALL1S EQU 0FFH ; BIT MASK COMPOSED OF ALL ONES.
177 } 00FE UPPER7 EQU 0FEH ; BIT MASK WITH UPPER SEVEN BITS SET.
178 } 007F LOWER7 EQU 7FH ; BIT MASK WITH LOWER SEVEN BITS SET.
179 }
180 }
181 } .....
182 } INTERRUPT VECTURING:
183 } -----
184 }
185 }
186 } 0000 ORG 0 ; VECTOR LOCATION FOR HARDWARE RESET (POWER-UP).
187 }
188 } 0000 0408 BEGIN: JMP BEGIN0 ; GO TO INITIALIZATION PROCEDURE.
189 } 0002 00 NOP ;
190 }
191 }
192 } ; VECTOR LOCATION FOR EXTERNAL INTERRUPT.
193 }
194 } 0003 8AE0 ORL P2,#BITDAT ; WRITE INTERRUPT ACKNOWLEDGE TO PORT 2
195 } ; (NOTE THIS IS ALSO ENCODER DATA OUTPUT ENABLE.)
196 }
197 } 0005 248B JMP ISR ; GO TO INTERRUPT SERVICE ROUTINE.
198 }
199 }
200 } ; VECTOR LOCATION FOR TIMER INTERRUPT
201 }
202 } 0007 93 RETR ; NO USE FOR THIS INTERRUPT. IF IT OCCURS,
203 } ; JUST RETURN TO THE POINT OF INTERRUPT.
204 }
205 } .....
206 } INITIALIZATION PROCEDURE:
207 } -----
208 } (EXECUTED ONLY ON HARDWARE RESET)
209 }
210 }
211 } 0008 9AE0 BEGIN0: ANL P2,#BITDAT ; ENABLE ENCODER DATA LATCH OUTPUT (#0E0H).

```

```

000A 09          212          IN      A,P1          ; OBTAIN THE ENCODER DATA.
000B D303        213          XRL    A,#3H        ; SET 'MOTOR STOPPED' FLAG, AND
000D AF          214          MOV    R7,A         ; CLEAR 'REVERSAL SINCE LAST UPDATE' FLAG.

000E 9AC0        215          ; LEAVE ADDRS OF RAM-ENABLE ON PORT 2 (#0C0H)
0010 2610        216          BEGLP1: JNTO        ; POLL RAM LOCKOUT UNTIL ACCESS
                                ; TO SHARED RAM IS GAINED.

0012 27          217          CLR    A            ; CLEAR
0013 B83F        218          MOV    R0,#3FH     ; EXTERNAL RAM LOCATIONS #1 - #63 AND
0015 90          219          BEGLP2: MOVX   @R0,A  ; INTERNAL RAM LOCATIONS #1 - #63.
0016 A0          220          MOV    R0,A        ;
0017 E815        221          DJNZ  R0,BEGLP2   ;

0019 23AA        222          MOV    A,#HDWRST   ; LOAD CODE FOR 'HARDWARE RESET'.
001B 90          223          MOVX   @R0,A       ; TEST THE EXTERNAL RAM
001C 80          224          MOVX   A,@R0       ; BY A WRITE/READ OF LOCATION ZERO.

001D 9A80        225          ANL    P2,#MLBXEN  ; ENABLE THE MAILBOX.
001F 02          226          OUTL  BUS,A        ; WRITE THE 'HARDWARE RESET' CODE TO MAILBOX.
0020 AE          227          MOV    R6,A        ; SAVE COPY OF CODE IN 'PREVIOUS WRITE' BUFFER.

0021 27          228          CLR    A            ;
0022 342C        229          CALL  PWHRT        ; GO WRITE ZERO PULSEWIDTH TO PW LATCH.

; .....
; .....
; THIS BEGINS THE MAIN ROUTINE. ESSENTIALLY, IT COMMUNICATES WITH
; THE 8751 RESPONDING APPROPRIATELY TO COMMANDS, AND SENDING THE
; NECESSARY MESSAGES DEPENDING ON INTERNAL STATES.

0024 05          240          MAIN48: EN      I    ; STROBE INTERRUPT ENABLE TO PICK UP
0025 15          241          DIS      I          ; THE INTERRUPT CONDITION.

0026 C5          242          SEL     RBO        ; SELECT REGISTER BANK ZERO.

0027 FF          243          MOV     A,R7       ; GET CONTENTS OF WRITE BUFFER.
0028 F269        244          JB7     WRITE      ; IF BIT 7 IS SET, GO WRITE CODE TO MAILBOX.

002A 9A00        245          RDMBX: ANL    P2,#IDLE ; IF WRITE MAILBOX IS EMPTY, RESTART MAIN.
002C 4624        246          JNT1   MAIN48      ;

002E 8A80        247          ORL    P2,#MLBXEN  ; IF FULL, PUT MAILBOX ENABLE ON PORT 2.
0030 08          248          INS    A,BUS       ; INPUT CODE FROM MAILBOX.
0031 C624        249          JZ     MAIN48      ; IF CODE IS ZERO, NO OPERATION.

0033 A9          250          MOV     R1,A       ; STORE INPUT CODE IN R1.
0034 47          251          SHAP  A            ; VALIDATE INPUT CODE BY
0035 09          252          XRL   A,R1         ; TESTING FOR NIBBLE-WISE SYMMETRY.
0036 9667        253          JNZ   R5NDRQ      ; IF CODE IS NOT VALID, GO REQUEST RESEND.

0038 F9          254          MOV     A,R1       ; OBTAIN ORIGINAL CODE AGAIN.
0039 5307        255          ANL    A,#7H       ; ISOLATE LOWEST THREE BITS.
003B C678        256          JZ     RESEND      ; IF CODE WAS 88H, WRITE PREVIOUS CODE TO MAILBOX.

003D D5          257          SEL     RB1        ; SELECT REGISTER BANK ONE.

003E 07          258          DEC    A           ;
003F C67B        259          JZ     CLRMYVS     ; IF CODE WAS 99H, GO CLEAR ALL MOVE COMMANDS.

0041 07          260          DEC    A           ;
0042 C6B3        261          JZ     MOVE        ; IF CODE WAS 0AAH, A NEW MOVE IS IN SHARED RAM.
0044 07          262          DEC    A           ;
0045 C689        263          JZ     HALT        ; IF CODE WAS 0BBH, GO HALT THE MOTOR.
0047 07          264          DEC    A           ;
0048 C6AD        265          JZ     GO          ; IF CODE WAS 0CCH, BEGIN (CONTINUE) MOTION.
004A 07          266          DEC    A           ;
004B C697        267          JZ     INTRAM      ; IF CODE WAS 0DDH, GO PEEK OR POKE INTERNAL RAM.
004D 07          268          DEC    A           ;
004E C68C        269          JZ     RESET       ; IF CODE WAS 0EEH, GO RESET ABSOLUTE POSITION.

; .....
; .....
; OTHERWISE CODE WAS 0FFH, SO GET COEFFICIENTS.

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284                                     } (FALL THROUGH TO THAT ROUTINE.)
285 } .....
286
287           } GET NEW SET OF COEFFICIENTS FOR CONTROL ALGORITHM:
288
0050 8AC0          COEFS: ORL   P2,#XRAMEN  } PUT RAM ENABLE ON PORT 2.
0052 2652          JNTO  COEFS           } IF RAM IS BUSY, KEEP WAITING FOR ACCESS.
290
291          MOV   R0,#CF1                } LOAD FIRST COEFFICIENT ADDRESS.
0054 B820          MOV   R3,#2H          } USE R3 AS OUTER LOOP COUNTER.
0056 B802          MOV   R4,#8H          } USE R4 AS INNER LOOP COUNTER.
0058 BC08          COELP1: MOVX  A,@R0    } MOVE IN THE COEFFICIENTS
296          MOV   @R0,A                } FROM EXTERNAL RAM TO
297          INC   R0                    } CORRESPONDING LOCATIONS IN INTERNAL RAM.
298          DJNZ  R4,COELP1
005D EC5A          MOV   R0,#GRIPPR     } LOAD FIRST PARAMETER ADDRESS.
005F B838          MOV   R4,#6H          } USE R4 AS INNER LOOP COUNTER AGAIN.
0061 BC06          DJNZ  R3,COELP1     } RUN INNER LOOP A SECOND TIME FOR PARAMETERS.
0063 EB5A          JMP   MAIN48
299
300 } .....
301           } REQUEST A RESEND OF LAST CODE:
302
0067 BF88          RSNDRQ: MOV  R7,#OVR   } MOVE RESEND REQUEST INTO R7.
310                                     } (FALL THROUGH TO WRITE ROUTINE.)
311 } .....
312           } WRITE CODE IN WRITE BUFFER (R7) TO MAILBOX:
313
0069 27           WRITE:  CLR   A         } CLEAR WRITE BUFFER AND
006A 2F           XCH   A,R7            } PUT CODE INTO PREVIOUS WRITE BUFFER.
006B AE           MOV   R6,A
316
317          WRILP1: EN   I               } STROBE INTERRUPT LINE IN CASE AN INTERRUPT
006D 05           DIS   I               } OCCURS WHILE WAITING TO WRITE TO MAILBOX.
006E 15           ANL   P2,#IDLE
006F 9A00          ORL   P2,#MLBXEN     } PUT MAILBOX ADDRESS ON PORT 2.
0070 8A80          ORL   P2,#MLBXEN     } IF WRITE MAILBOX IS FULL, PREVIOUS CODE HAS NOT
0072 566C          JTI   WRILP1        } YET BEEN READ BY 8751, SO KEEP WAITING.
320
321          NOPOLL: MOV   A,R6           } OBTAIN CODE TO BE WRITTEN.
0074 FE           OUTL  BUS,A           } WRITE IT TO MAILBOX.
0075 02           JMP   RDMBX
0076 042A
324 } .....
325           } OBTAIN PREVIOUS CODE TO EXECUTE A RESEND TO 8751:
326
0078 2E           RESEND: XCH  A,R6      } EXCHANGE NOP CODE FOR PREVIOUS CODE.
0079 0475          JMP   NOPOLL         } WRITE TO MAILBOX WITHOUT POLLING.
330 } .....
331           } CLEAR ALL REMAINING MOVES AND RELATED INFORMATION:
332
007B A5           CLRMVS: CLR  F1         } CLEAR THE STALL FLAG.
334
335          CLRRLP1: MOV   R1,#NMMVNF    } LOAD ADRS OF FIRST MOVE DATA LOCATION.
007C B92C          MOV   R0,#11D         } USE R0 AS A LOOP COUNTER.
007E B80B          MOV   @R1,A           } CLEAR ALL THE MOVE INFORMATION LOCATIONS,
0080 A1           INC   R1              } EXCEPT PULSEWIDTH SIGN.
0081 19           DJNZ  R0,CLRRLP1
0082 E880          MOV   R5,A           } CLEAR VELOCITY SET POINT.
340
0084 AD           CALL  RDMMSG          } GO PUT 'READY' MESSAGE IN BUFFER.
342
0085 340C          JMP   MAIN48
0087 0424
348
349

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356 }.....
357
358           ; ENTER THE 'HALT' CONDITION:
359
0089 85     HALT:  CLR  F0           CLEAR FLAG 0 TO INDICATE HALT CONDITION.
008A 0424   JMP    MAIN48
360
361
362           ;.....
363
364           ; ZERO THE ABSOLUTE POSITION LOCATIONS IN EXTERNAL RAM:
365
008C 8AC0   RESET:  ORL  P2,#XRAMEN    PUT RAM ENABLE ON PORT 2.
008E B933   MOV    R1,#PRMVLO    LOAD ADRS OF ABSOLUTE POSITION LOW BYTE.
366                                     (SAME AS ADRS OF PRESENT MOVE LOW BYTE.)
0090 2690   RESLP1: JNT0  RESLP1    IF RAM IS BUSY, KEEP WAITING FOR ACCESS.
367
0092 91     MOVX  @R1,A           CLEAR BOTH BYTES
0093 19     INC   R1           OF ABSOLUTE POSITION.
0094 91     MOVX  @R1,A
0095 0424   JMP    MAIN48
368
369           ;.....
370
0097 8AC0   INTRAM: ORL  P2,#XRAMEN    ENABLE EXTERNAL RAM.
0099 2699   INTLP1: JNT0  INTLP1    IF LOCKED OUT, KEEP WAITING.
371
372
009B B829   MOV    R0,#RAMADR    LOAD LOCATION OF ADDRESS TO PEEK/POKE.
009D 80     MOVX  A,@R0           READ IN ADDRESS.
009E A9     MOV    R1,A           AND PUT IT IN ADDRESS POINTER 1.
009F C8     DEC   R0           DECR R0 TO DATA PASSING ADDRESS.
00A0 F2A9   JB7   POKE           IF BIT 7 OF ADDR IS SET, COMMAND IS A POKE.
373                                     ELSE, COMMAND IS A PEEK.
374
00A2 F1     PEEK:  MOV    A,@R1    GET DATA FROM PEEK ADDRESS (R1).
00A3 90     MOVX  @R0,A    WRITE THE DATA TO DATA PASSING LOCATION.
375
00A4 C5     SEL   RBO           SELECT REGISTER BANK 0.
00A5 BFCC   MOV    R7,#RAMPK    PUT 'RAM PEEK COMPLETE' CODE IN WRITE BUFFER.
00A7 0469   JMP    WRITE        GO WRITE CODE TO MAILBOX.
376
00A9 80     POKE:  MOVX  A,@R0    OBTAIN DATA TO BE 'POKED'.
00AA A1     MOV    @R1,A    PUT IT IN PROPER INTERNAL RAM LOCATION.
00AB 0424   JMP    MAIN48
377
378           ;.....
379
00AD 7624   GO:    JF1   MAIN48    IF STALLED, DO NOT START GOING.
380
00AF 85     CLR   F0           CLEAR 'GO' FLAG
00B0 95     CPL   F0           IN ORDER TO SET IT.
00B1 0424   JMP    MAIN48
381
382           ;.....
383
00B3 8AC0   MOVE:  ORL  P2,#XRAMEN    PUT EXTERNAL RAM ENABLE ON PORT 2.
00B5 B82C   MOV    R0,#NXMVNF    LOAD ADDRESS OF 'NEXT MOVE INFINITE' FLAG.
00B7 B906   MOV    R1,#6H        LOAD LOOP COUNTER FOR SIX BYTES OF DATA.
384
00B9 26B9   MOVLP1: JNT0  MOVLP1    IF 8748 IS LOCKED OUT OF SHARED RAM,
385                                     KEEP WAITING.
00BB 80     MOVLP2: MOVX  A,@R0    TRANSFER NEXT MOVE DATA FROM
00BC AD     MOV    @R0,A    EXTERNAL RAM LOCATIONS TO
00BD 18     INC   R0           CORRESPONDING INTERNAL LOCATIONS.
00BE E9BB   DJNZ  R1,MOVLP2
386
00C0 0424   JMP    MAIN48
387
388           ;.....
389
426 }.....
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			; MOVE YET SUBROUTINE:	PROVIDE: REGISTER BANK 1 SELECTED.
				RETURNS: ACCUMULATOR IS ZERO IF THE
				MOTOR POSITION IS INCORRECT, AND
				NON-ZERO IF MOTOR POSITION IS
				CORRECT. IF MOTOR POSITION IS
				INCORRECT, USABLE VALUES ARE RETURNED
				IN PULSEWIDTH AND PULSEWIDTH SIGN
				LOCATIONS, AND, IN THAT CASE, ON RETURN
				RO = #SIGNPW AND R1 = #PLSWTH.
				CHANGES: RB1: RO, R1, ACC, PSM, PLSWTH, SIGNPW
				CALLS: NEW MOVE (NEWMOV)
				CALLED BY: MOTOR STOPPED (MTRSTP)
00C2	B934	MOVYET: MOV	R1,#PRMVHI	LOAD ADDR OF PRESENT MOVE HIGH BYTE.
00C4	F1	MOV	A,#R1	OBTAIN IT FOR INSPECTION.
00C5	96CC	JNZ	DETSGN	IF NOT ZERO, MORE TO MOVE. GO DETERMINE SIGN.
				IF ZERO, DECR R1 TO ADDR LOW BYTE PRESENT MOVE.
00C7	C9	DEC	R1	OBTAIN LOW BYTE FOR INSPECTION.
00C8	F1	MOV	A,#R1	IF IT IS ALSO ZERO, GO CHECK FOR Q-H TAIL.
00C9	C6E5	JZ	CKQHTL	ELSE, MOVE IS POSITIVE NUMBER, SO CLEAR SIGN BIT.
00CB	27	CLR	A	
				MASK OFF ALL BUT SIGN BIT OF MOVE.
00CC	5380	DETSGN: ANL	A,#SGNMSK	OBTAIN CORRECT PULSEWIDTH SIGN
00CE	B835	MOV	RO,#PRMVSN	BY EXCLUSIVE OF WITH PRESENT MOVE SIGN,
00D0	D0	XRL	A,#RO	AND STORE IT IN INTERNAL RAM LOCATION.
00D1	B837	MOV	RO,#SIGNPW	
00D3	A0	MOV	OR0,A	
				IF THE MOTOR STOP INTERRUPT COUNT
00D4	B928	MOV	R1,#STPCNT	IS EXACTLY THREE, THEN ADD IN THE VELOCITY
00D6	F1	MOV	A,#R1	SET POINT TO THE PULSEWIDTH. OTHERWISE,
00D7	D303	XRL	A,#3H	JUST ADD IN THE STOP COUNT, ITSELF.
00D9	96DC	JNZ	ADDGO	
00DB	FD	MOV	A,R5	
				ADD IN THE VALUE OF THE STARTING
00DC	B93A	ADDGO: MOV	R1,#STRTPW	PULSEWIDTH TO THE PRESENT
00DE	61	ADD	A,#R1	PULSEWIDTH.
00DF	B936	MOV	R1,#PLSWTH	
00E1	61	ADD	A,#R1	
00E2	A1	MOV	OR1,A	STORE NEW PULSEWIDTH.
00E3	27	CLR	A	CLEAR ACC TO INDICATE MORE TO MOVE.
00E4	83	RET		
				LOAD ADDR OF QUARTER-HOLE TAIL.
00E5	B92B	CKQHTL: MOV	R1,#QHTAIL	OBTAIN IT FOR INSPECTION.
00E7	F1	MOV	A,#R1	IF NOT ZERO, GO DETERMINE SIGN OF MOVE.
00E8	96CC	JNZ	DETSGN	
				ELSE, SEE IF NEW MOVE AWAITS EXECUTION.
00EA	14F2	CALL	NEWMOV	IF NEW MOVE AWAITS, CLEAR PULSEWIDTH
00EC	B936	MOV	R1,#PLSWTH	AND
00EE	A1	MOV	OR1,A	GO DETERMINE NEW SIGN AND PW.
00EF	C6CC	JZ	DETSGN	IF NOT, RETURN WITH 'NO MOVE' INDICATED.
00F1	83	RET		
			
			
			; NEW MOVE SUBROUTINE:	PROVIDE: REGISTER BANK 1 SELECTED.
				RETURNS: IF NEXT MOVE HAS BEEN RECEIVED;
				MOVES NEXT MOVE DATA TO PRESENT
				MOVE DATA. PUTS 'READY FOR NEXT
				MOVE' CODE (#0DDH) IN WRITE BUFFER, AND
				RESETS THE 'NEXT MOVE RECEIVED' FLAG.
				ALSO, ACC IS RETURNED ZERO ONLY IF NEXT
				MOVE HAS BEEN RECEIVED.

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507
508 NEWMOV: MOV R3,#4
509
510 MOV RO,#RCVDNM
511 MOV A,@RO
512 JNZ GETMOV
513 JMP NEWFIN
514
515 GETMOV: MOV @RO,#0
516 INC RO
517 MOV A,@RO
518 MOV R5,A
519 MOV R1,#PRSVEL
520 NEWLP1: MOV A,@RO
521 MOV @R1,A
522 INC RO
523 INC R1
524 DJNZ R3,NEWLP1
525
526 MOV RO,#STPCNT
527 MOV @RO,#0H
528
529 RDYMSG: MOV RO,#7H
530 MOV @RO,#RDYNXT
531
532 NEWFIN: MOV A,R3
533 RET
534
535 ; .....
536 ; .....
537 ; .....
538 ; UPDATE PULSEWIDTH SUBROUTINE:
539
540 PROVIDE: SELECT RB1, VELOCITY ERROR IN ACC,
541 COEFFICIENTS ADDRESS IN RO, CORRECT VALUES
542 FOR PARTICULAR ENTRY POINT.
543
544 RETURNS: PROPER PULSEWIDTH (BASED ON COEF-
545 FICIENTS SUPPLIED) WRITTEN TO
546 INTERNAL LOCATIONS AND TO
547 PULSEWIDTH LATCH.
548
549 CHANGES: RB1: RO,R1,R3,ACC,PSW,PLSWTH,SIGNPW,
550 PW LATCH IN PW MODULATOR.
551
552 CALLS: MULT
553
554 CALLED BY: INITIALIZATION ROUTINE
555 (VECTORS TO PWRIT)
556 INTERRUPT SERVICE ROUTINE
557 (VARIOUS ENTRY POINTS)
558
559 PHUPDT: CALL MULT
560 MOV R3,A
561
562 MOV RO,#SIGNPW
563 MOV A,@RO
564 MOV R1,#PRMYSN
565 MOV A,@R1
566 XRL @R1,PWRVRS
567 JB7 R1
568 JMPBK3: MOV R1
569 MOV A,@R1
570 ADD A,R3
571 MOV @R1,A

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0121 F23B      572      JB7      OVFLOW      ; IF BIT 7 IS SET, GO SEE WHY SUM OVERFLOWED.
                573
0123 F1        574      PWHYST: MOV   A,#R1      ; GET PRESENT PULSEWIDTH.
0124 C62B      575      JZ      PWSIGN      ; IF PW IS ZERO, DON'T ADD HYSTERESIS OFFSET.
0126 B939      576      MOV   R1,#HYSTPM    ; ELSE, ADD USER-SPECIFIED
0128 61        577      ADD   A,R1          ; HYSTERESIS OFFSET TO PW.
0129 F240      578      JB7      MAXOUT     ; IF THAT OVERFLOWS PW, GO SET PW TO MAXIMUM.
                579
012B 40        580      PWSIGN: ORL   A,#R0      ; CONCATENATE PW SIGN FOR WRITE TO PW LATCH.
                581
012C 39        582      PHWRT: OUTL  P1,A      ; PUT NEW PULSEWIDTH ON PORT 1.
012D 8AA0      583      ORL   P2,#PWLTEN    ; PUT PULSEWIDTH LATCH ENABLE ON PORT 2.
012F 90        584      MOVX  @R0,A         ; GENERATE LATCH PULSE WITH WRITE TO DUMMY ADDRESS.
0130 9A00      585      ANL  P2,#IDLE      ; CLEAR ENABLE ADDRESS FROM PORT 2.
0132 89FF      586      ORL  P1,#ALLIS     ; RESTORE PORT 1 TO THE INPUT STATE.
0134 83        587      RET
                588
0135 FB        589      PWRVRS: MOV  A,R3      ;
0136 37        590      CPL  A             ; REVERSE THE SIGN OF THE
0137 17        591      INC  A             ; PULSEWIDTH INCREMENT.
0138 AB        592      MOV  R3,A         ;
0139 241D      593      JMP  JMPBK3       ;
                594
                595      ; DETERMINE REASON FOR OVERFLOWED SUM:
                596
013B FB        597      OVFLOW: MOV  A,R3      ; GET THE PULSEWIDTH INCREMENT FOR TESTING.
013C F244      598      JB7      CHGSN     ; IF NEGATIVE, THEN PULSEWIDTH SIGN CHANGED.
013E B17F      599      MOV  @R1,#LOWER7  ; IF POSITIVE, THEN PULSEWIDTH SATURATED.
                600
0140 237F      601      MAXOUT: MOV  A,#LOWER7 ; LOAD MAXIMUM PW VALUE (127) INTO ACC.
0142 242B      602      JMP  PWSIGN
                603
0144 F1        604      CHGSN: MOV  A,#R1      ; OBTAIN THE
0145 37        605      CPL  A             ; NEGATIVE PULSEWIDTH,
0146 17        606      INC  A             ; 2'S COMPLEMENT IT,
0147 A1        607      MOV  @R1,A        ; AND REPLACE IT.
                608
0148 F0        609      MOV  A,#R0        ; OBTAIN PW SIGN,
0149 D380      610      PWDLRV: XRL  A,#SGNMSK ; REVERSE IT,
014B A0        611      PWDLAY: MOV  @R0,A    ; AND REPLACE IT.
014C 39        612      ORL  P1,A         ; PUT PW SIGN BIT (WITH ZERO PW) ON PORT 1.
014D 8AA0      613      ORL  P2,#PWLTEN    ; PUT PULSEWIDTH LATCH ENABLE ADDRESS ON PORT 2.
014F 90        614      MOVX  @R0,A        ; GENERATE LATCH PULSE WITH WRITE TO DUMMY ADDRESS.
                615
0150 BB30      616      MOV  R3,#30H      ; ALLOW TIME FOR POWER TRANSISTOR TO CUTOFF
0152 EB52      617      PWULP1: DJNZ R3,PWULP1 ; BEFORE APPLYING REVERSE POWER.
                618
0154 2423      619      JMP  PWHYST       ; GO PROCESS THE NEW PULSEWIDTH.
                620
                621      ; .....
                622      ; .....
                623      ; .....
                624      ; MOTOR STOPPED SUBROUTINE:
                625
                626      ;
                627      ; PROVIDE: RB1 SELECTED, CORRECT VALUES
                628      ; FOR PARTICULAR ENTRY POINT.
                629
                630      ; RETURNS: STALL FLAG SET IF MOTOR STALLED.
                631      ; IF MOTOR IS RECEIVING LESS THAN 50%
                632      ; PULSEWIDTH BUT IS NOT YET MOVING,
                633      ; PULSEWIDTH WILL BE INCREASED
                634      ; ENTRY AT 'WRPWO' SETS PULSEWIDTH
                635      ; AND ASSOCIATED LOCATIONS TO ZERO.
                636
                637      ; CHANGES: RB1: R0,R1,R7,ACCUM,PSW,F1,
                638      ; P2,SIGNPW,PLSWTH,STPCNT,WRITE BUFFER
                639
                640      ; CALLS: POSITION UPDATE (PSNUPD)
                641      ; PULSEWIDTH UPDATE (PWUPDT)
                642      ; (ENTRY AT 'PWRIT' OR 'PWLAY')
                643      ; MOVE YET (MOVYET)

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644      } CALLED BY: INTERRUPT SERVICE ROUTINE
645      } (FROM 'MOTION', 'NOPMUD',
646      } AND 'OVRSH')
647
0156 B928 648 STALL1: MOV R1,#STPCNT } OBTAIN THE NUMBER OF
0158 F1      649      MOV A,#R1      } MOTOR STOP INTERRUPTS.
0159 03EF    650      ADD A,#11H     } SEE IF IT EXCEEDS SIXTEEN.
015B F283    651      JB7          } IF NOT, MOTOR IS NOT REALLY STALLED.
652
015D B5      653      CPL F1         } IF SO, SET THE STALL FLAG.
015E B807    654      MOV R0,#7H     } PUT 'MOTOR STALLED' CODE
0160 B099    655      MOV @R0,#MTRSTL } INTO WRITE BUFFER.
656
0162 9A00    657 MTRSTP: ANL P2,#IDLE } CLEAR ENABLE ADDRESS FROM PORT 2.
658
0164 868A    659      JNI TRNSIT     } IF INTERRUPT STILL ACTIVE, MOTOR IS MOVING.
0166 11      660      INC @R1       } ELSE, INCREMENT 'MOTOR STOPPED INTERRUPT' COUNT.
661
0167 FF      662      MOV A,R7        } MOTOR IS NOT IN MOTION,
0168 4302    663      ORL A,#2H     } SO SET 'MOTOR STOPPED' FLAG.
016A AF      664      MOV R7,A        }
665
016B B92A    666      MOV R1,#SPEED   } WRITE ZERO TO
016D B100    667      MOV @R1,#0H     } SPEED LOCATION.
668
016F 7429    669 PMO: CALL PSNUPD  } CALL 'POSITION UPDATE' SUBROUTINE.
0171 B837    670      MOV RO,#SIGNPM } LOAD ADDR OF PULSEWIDTH SIGN.
671
0173 7677    672      JF1 WRPWO     } IF MOTOR IS STALLED, WRITE ZERO PULSEWIDTH.
0175 B67E    673      JF0 STLLCK    } IF 'GO' FLAG SET, GO CHECK FOR STALL.
674
0177 27      675 WRPWO: CLR A       } WRITE ZERO
0178 B936    676      MOV R1,#PLSWTH } TO THE
017A A1      677      MOV @R1,A      } PULSEWIDTH LOCATION.
017B 342C    678      CALL PWRWRT    } GO WRITE THE ZERO PW TO THE PW LATCH.
017D 83      679      RET          }
680
017E B936    681 STLLCK: MOV R1,#PLSWTH } INSPECT
0180 F1      682      MOV A,@R1     } PRESENT PULSEWIDTH.
0181 D256    683      JB6 STALL1    } IF PW EXCEEDS 63, THERE MAY BE A STALL.
684
0183 14C2    685 NOSTAL: CALL MOVYET } SEE IF A MOVE REMAINS TO EXECUTE.
0185 9677    686      JNZ WRPWO     } IF NO MOVE IS INDICATED, GO WRITE ZERO PW.
687
0187 F0      688      MOV A,@R0     } IF THERE IS A MOVE, RECALL PULSEWIDTH SIGN.
0188 344B    689      CALL PWDLAY    } GO WRITE PULSEWIDTH WITH DELAY.
018A 83      690 TRNSIT: RET     }
691
692 } .....
693 } .....
694
695 } THIS IS THE INTERRUPT SERVICE ROUTINE. IT WILL BE ENTERED
696 } WHENEVER THERE IS AN ENCODER BIT TRANSITION, OR IF 1/8 SECOND OF
697 } TIME PASSES WITHOUT AN ENCODER BIT TRANSITION. THE TRANSITION
698 } INTERRUPT REMAINS ACTIVE FOR 700 MICROSECONDS.
699 } THE ONE-SECOND INTERRUPT REMAINS ACTIVE UNTIL ACKNOWLEDGED.
700
701 } NOTE THAT THE INTERRUPT ACKNOWLEDGE SENT AT THE
702 } INTERRUPT VECTOR POINT (PC=3) IS ALSO THE
703 } ENCODER DATA LATCH OUTPUT ENABLE.
704
018B D5      705 ISR: SEL RB1      } SELECT REGISTER BANK ONE FOR THE ISR.
018C B928    706      MOV R1,#STPCNT } LOAD ADDR OF MOTOR STOP INTERRUPT COUNT.
018E 09      707      IN A,#R1      } INPUT THE ENCODER DATA.
018F DF      708      XRL A,R7       } SEE IF PRESENT POSITION AND PREVIOUS POSITION
0190 33C0    709      ANL A,#0COH   } ARE THE SAME (BY EXCLUSIVE OR OF THE TWO BITS).
0192 3497    710      JNZ MOTION    } IF NOT ZERO, THE MOTOR IS IN MOTION.
0194 3462    711      CALL MTRSTP   } IF SO, THEN CALL THE MOTOR STOPPED SUBROUTINE.
0196 93      712      RETR        } RETURN TO MAIN PROGRAM, RESTORING PSW.
713
714 } IF MOTOR IS MOVING, ISR BRANCHES TO HERE:
715

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0197 B100 2716 MOTION: MOV   Q,R1,#0H      ; CLEAR MOTOR STOPPED INTERRUPT COUNT.
0199 09   2717         IN     A,P1          ; INPUT THE ENCODER DATA AGAIN
019A 9A20 2718         ANL   P2,#CLCKHI     ; PUT ADDRESS OF HIGH CLOCK BYTE ON PORT 2.
019C 2F   2719         XCH  A,R7          ; EXCHANGE FOR PREVIOUS ENCODER BITS.
019D 12A0 2720         JBO  DIRDET       ; PRESERVE STATE OF
019F CF   2721         DEC   R7          ; 'REVERSAL SINCE LAST UPDATE' FLAG.
                                           ; (NOTE ENCODER DATA BIT 0 IS HARDWARE SET HIGH)
                                           ; .....
                                           ; DIRECTION DETERMINATION: BOTH ABSOLUTE AND RELATIVE-TO-MOVE-
                                           ; SIGN. ALSO POS ERROR IS INCREMENTED/DECREMENTED ACCORDINGLY.
01A0 F7   2728 DIRDET: RLC   A              ; MOVE B1(K-1) TO THE B0 POSITION (BIT 7).
01A1 DF   2729         XRL   A,R7          ; XCLSV-OR B1(K-1) WITH B0(K)
                                           ; TO GET 'ABSOLUTE DIRECTION' FLAG.
01A2 53FE 2730         ANL   A,#UPPER7      ; CLEAR THE 'RELATIVE DIRECTION' FLAG.
01A4 2E   2731         XCH  A,R6          ; EXCHANGE FOR PREVIOUS FLAG VALUES OF R6.
01A5 DE   2732         XRL   A,R6          ; EXCLUSIVE-OR PREVIOUS 'ABSOLUTE DIRECTION'
                                           ; AND PRESENT 'ABSOLUTE DIRECTION' FLAGS
                                           ; TO SEE IF DIRECTION HAS REVERSED.
01A6 F2AA 2733         JB7   DIRRVS      ; IF THEY ARE DIFFERENT, DIRECTION HAS REVERSED.
01A8 24B4 2734         JMP   DIRCMP     ; OTHERWISE GO COMPARE ABSOLUTE DIRECTION
                                           ; TO COMMANDED DIRECTION.
01AA FE   2740 DIRRVS: MOV   A,R6          ; SINCE MOTION JUST REVERSED MOTION IS JUST
01AB 4304 2741         ORL   A,#4H      ; STARTING, SO SET, 'NEW MOTION' FLAG.
01AD AE   2742         MOV   R6,A
01AE 92B4 2743         JB4   DIRCMP     ; IF 'PREVIOUS POSITION 0,0' FLAG IS SET,
                                           ; THEN REVERSAL DOES NOT AFFECT 'POSITION UPDATE.
01B0 FF   2744         MOV   A,R7          ; OTHERWISE IT DOES AFFECT IT, SO SET
01B1 D301 2745         XRL   A,#1H      ; THE 'REVERSAL SINCE LAST UPDATE' FLAG.
01B3 AF   2746         MOV   R7,A
01B4 B835 2750 DIRCMP: MOV   R0,#PRMVSN   ; COMPARE THE PRESENT MOVE SIGN
01B6 F0   2751         MOV   A,R0          ; TO THE 'ABSOLUTE DIRECTION' OF MOTION
01B7 DE   2752         XRL   A,R6          ; BY EXCLUSIVE OR'ING THEM
01B8 F2BC 2753         JB7   DIROPP     ; IF DIRRVERS, GO SET 'RELATIVE DIRECTION' FLAG.
01BA 24BD 2754         JMP   VELDET     ; OTHERWISE, LEAVE IT CLEARED (DONE ABOVE).
01BC 1E   2755 DIROPP: INC   R6              ; SET 'RELATIVE DIRECTION' FLAG.
                                           ; .....
                                           ; VELOCITY DETERMINATION
01BD B901 2760 VELDET: MOV   R1,#1H      ; LOAD LEAST SHIFT.
01BF 52CD 2761         JB2   VELNEW     ; IF 'NEW MOTION' FLAG IS SET, GO SET SPEED
                                           ; TO ITS SMALLEST NON-ZERO VALUE (1).
01C1 09   2762         IN     A,P1          ; INPUT THE HIGH BYTE OF THE CLOCK.
01C2 8A60 2763         ORL   P2,#CLCKLO     ; PUT ADDRESS OF LOW CLOCK BYTE ON PORT 2.
01C4 96D0 2764         JNZ   VELSL0     ; IF HIGH BYTE IS NOT ZERO, VEL < 128.
                                           ; ELSE VEL >= 128.
01C6 09   2765         IN     A,P1          ; INPUT THE LOW CLOCK BYTE.
01C7 F2E3 2766         JB7   LOOKUP     ; IF HIGH BIT IS SET, 128 <= VEL < 256
01C9 23FE 2767         MOV   A,#0FEH      ; VELOCITY IS MAXIMUM. SET IT TO 254.
01CB 24E4 2768         JMP   SHIFT
01CD F9   2769 VELNEW: MOV   A,R1          ; NEW MOTION, SO SET VEL TO 1 HOLE PER SECOND
01CE 24E4 2770         JMP   SHIFT     ; (THE MINIMUM).
01D0 AB   2771 VELSL0: MOV   R3,A          ; STORE HIGH CLOCK BYTE TEMPORARILY.
01D1 09   2772         IN     A,P1          ; OBTAIN LOW CLOCK BYTE.
01D2 19   2773         INC   R1          ; LOOK-UP TABLE SHIFT COUNT IS AT LEAST 2
                                           ; FOR QUARTER-HOLE VELOCITY LESS THAN 128.
01D3 2B   2784 VELLP1: XCH  A,R3          ; EXCHANGE LOW CLOCK BYTE, RECOVERING THE HIGH.
01D4 97   2785         CLR   C              ; CLEAR THE CARRY BIT.
01D5 67   2786         RRC   A              ; ROTATE THE HIGH CLOCK BYTE RIGHT.

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01D6 C6E1	788	JZ	VELSHF	IF BITS LEFT ARE ALL ZERO, GO GET TABLE VALUE.
01D8 2B	789	XCH	A,R3	EXCHANGE HIGH CLOCK BYTE, RECOVERING THE LOW.
01D9 67	790	RRC	A	ROTATE IN THE BIT FROM THE HIGH CLOCK BYTE.
01DA 19	791	INC	R1	INCREMENT THE LOOK-UP TABLE SHIFT COUNT.
01DB 24D3	792	JMP	VELLP1	
	793			
01DD 97	794	SHFRT: CLR	C	DIVIDE THE VELOCITY BY TWO AGAIN.
01DE 67	795	RRC	A	
01DF 24E4	796	JMP	SHIFT	
	797			
01E1 2B	798	VELSHF: XCH	A,R3	RECOVER THE 7 BITS IN THE LOW CLOCK BYTE.
01E2 67	799	RRC	A	ROTATE IN THE EIGHTH BIT FROM CARRY.
01E3 E3	800	LOOKUP: MOV	P3,A	OBTAIN LOOK-UP TABLE VELOCITY VALUE.
	801			
01E4 E9DD	802	SHIFT: DJNZ	R1,SHFRT	KEEP SHIFTING UNTIL COUNTER IS ZERO,
01E6 AA	803	MOV	R2,A	TO OBTAIN THE VELOCITY.
01E7 97	804	CLR	C	SHIFT A FINAL TIME TO FIT INTO SEVEN BITS.
01E8 67	805	RRC	A	
	806			
01E9 1300	807	ADDC	A,#0	ROUND UPWARD, USING THE BIT LAST SHIFTED OUT.
	808			
	809			
	810			
	811			
	812			
	813			
01EB 9A00	814	VELCTY: ANL	P2,#IDLE	CLEAR ENABLE ADDRESS FROM PORT 2.
01ED B82A	815	MOV	R0,#SPEED	DETERMINE THE VALUE
01EF 20	816	XCH	A,R0	OF THE CHANGE IN SPEED SINCE LAST
01F0 37	817	CPL	A	INTERRUPT, AND STORE IT IN
01F1 17	818	INC	A	THE LOCATION CALLED 'DELTA V'.
01F2 60	819	ADD	A,R0	
01F3 B93F	820	MOV	R1,#DELTA V	
01F5 A1	821	MOV	R1,A	
	822			
01F6 FA	823	MOV	A,R2	ISOLATE THE LOW BIT ONLY OF THE
01F7 5301	824	ANL	A,#1H	FULL VELOCITY MEASURE.
01F9 AA	825	MOV	R2,A	
01FA 00	826	NOP		ADJUST FOR PAGE BOUNDARY.
01FB 00	827	NOP		
	828			
01FC B927	829	MOV	R1,#MG4	DETERMINE THE ADDRESS OF THE
01FE FD	830	MOV	A,R5	MAXIMUM MAGNITUDE FOR
01FF D208	831	JB6	LIMIT	THE RANGE IN WHICH THE
0201 C9	832	DEC	R1	VELOCITY SET POINT
0202 B208	833	JB5	LIMIT	FALLS.
0204 C9	834	DEC	R1	
0205 9208	835	JB4	LIMIT	
0207 C9	836	DEC	R1	
	837			
0208 FE	838	LIMIT: MOV	A,R6	GET REGISTER 6 FLAGS.
0209 67	839	RRC	A	ROTATE 'RELATIVE DIRECTION' FLAG INTO CARRY.
020A F0	840	MOV	A,R0	RECOVER PRESENT VELOCITY.
020B F60F	841	JC	MTNWRG	IF CARRY IS SET, MOTION IS IN WRONG DIRECTION.
	842			
020D 37	843	CPL	A	OTHERWISE, PRESENT VELOCITY MUST BE
020E 17	844	INC	A	SUBTRACTED FROM THE VELOCITY SET POINT.
	845			
020F 6D	846	MTNWRG: ADD	A,R5	ADD VELOCITY SET PNT TO GET VELOCITY ERROR.
0210 AC	847	MOV	R4,A	STORE PRESENT VELOCITY ERROR IN REGISTER 4.
	848			
0211 97	849	CLR	C	RESTORE FULL VELOCITY ERROR.
0212 67	850	RRC	A	
0213 6A	851	ADD	A,R2	
	852			
0214 2C	853	XCH	A,R4	SEE THAT ERROR DID NOT OVERFLOW.
0215 DC	854	XRL	A,R4	
0216 F223	855	JB7	MAXERR	
	856			
0218 FC	857	MOV	A,R4	OBTAIN VELOCITY ERROR FOR
0219 F21D	858	JB7	NEGERR	COMPARISON TO MAXIMUM ALLOWABLE ERROR.
021B 37	859	CPL	A	

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021C 17      860      INC      A      ;
861      ;
021D 61      862      NEGERR: ADD  A,ØR1      ; GET DIFFERENCE: (MAXMAG) - (VEL ERROR).
021E F222    863      JB7      A,PREMAX  ; IF NEGATIVE THEN ERROR EXCEEDS MAXIMUM.
0220 442B    864      JMP      A,CHKDLV ;
865      ;
0222 37      866      PREMAX: CPL  A      ; DETERMINE SIGN OF MAXIMUM ERROR.
0223 DC      867      MAXERR: XRL  A,R4    ; AND PUT SIGN IN CARRY.
0224 F7      868      RLC      A      ;
0225 F1      869      MOV      A,ØR1    ; MOVE MAXIMUM MAGNITUDE INTO ACCUMULATOR,
0226 E62A    870      JNC      MAXPOS  ; AND DETERMINE PROPER SIGN FOR IT.
0228 37      871      CPL      A      ;
0229 17      872      INC      A      ;
022A AC      873      MAXPOS: MOV  R4,A    ;
874      ;
022B FC      875      CHKDLV: MOV  A,R4    ; IF THE SIGN OF DELTA V IS
022C C635    876      JZ      UPDATE ; THE SAME AS THE SIGN OF THE VELOCITY ERROR
022E B83F    877      MOV      R0,#DELTA ; THE PRESENT PULSEWIDTH IS ALREADY
0230 D0      878      XRL  A,ØR0    ; BRINGING THE VELOCITY CLOSER TO THE SET
0231 F235    879      JB7      UPDATE ; POINT, SO LOAD ZERO AS THE VELOCITY
0233 BC00    880      MOV      R4,#0H  ; ERROR (NO PULSEWIDTH INCREMENT).
881      ;
0235 B63B    882      UPDATE: JFO  UPDPW  ; IF 'GO' FLAG SET, GO CHECK 'STALL' FLAG.
0237 346F    883      NOPWUD: CALL PWO    ; ELSE, SET PULSEWIDTH TO ZERO.
0239 44D3    884      JMP      FNPLP1 ;
885      ;
023B 7637    886      UPDPW: JF1  NOPWUD ; IF MOTOR IS STALLED, NO PULSEWIDTH UPDATE.
887      ;
023D F9      888      MOV      A,R1    ; OBTAIN THE ADDRESS OF THE VELOCITY ERROR
023E 03FC    889      ADD     A,#-4H   ; COEFFICIENT BY SUBTRACTING FOUR FROM
0240 A8      890      MOV      R0,A    ; THE ADDRESS OF THE MAXIMUM MAGNITUDE.
891      ;
0241 FC      892      MOV      A,R4    ; RECALL THE VELOCITY ERROR,
0242 3412    893      CALL   PWUPDT  ; AND CALL PULSEWIDTH UPDATE SUBROUTINE.
894      ;
0244 7429    895      CALL   PSNUPD  ; CALL THE POSITION UPDATE SUBROUTINE.
896      ;
897      ;
898      ;
899      ;
900      ;
901      ;
          ; PREPARE FOR NEXT INTERRUPT BY ADJUSTING VELOCITY SET POINT
          ; AND ADJUSTING PRESENT PULSEWIDTH, IF NECESSARY.
0246 B934    902      PREPAR: MOV  R1,#PRMVI ; CONSIDER HIGH BYTE OF PRESENT MOVE
0248 F1      903      MOV      A,ØR1    ;
0249 F2A0    904      JB7      OVRSH1  ; IF IT IS NEGATIVE, OVERSHOOT IS OCCURRING.
024B 96BC    905      JNZ     INFMOV  ; IF IT NOT ZERO, LONG MOVE REMAINS.
906      ;
024D C9      907      DEC      R1      ; INSPECT THE LOW BYTE
024E F1      908      MOV      A,ØR1    ; OF REMAINING PRESENT MOVE.
024F F2BC    909      JB7      INFMOV  ; IF IT EXCEEDS 127, THEN MOVE IS VERY LONG.
0251 AA      910      MOV      R2,A    ;
0252 D27B    911      JB6      DCLSTP  ; IF REMAINING MOVE EXCEEDS 32, DONT LOOK
0254 B27B    912      JB5      DCLSTP  ; FOR NEXT MOVE, JUST GO DECELERATE.
0256 965F    913      JNZ     PREDCL  ; IF IT IS NOT ZERO, GO CHECK THE NEXT MOVE.
914      ;
0258 B92B    915      MOV      R1,#QTAIL ; IF IT IS ZERO, CHECK THE QUARTER-HOLE
025A F1      916      MOV      A,ØR1    ; POSITION ERROR.
025B F2A5    917      JB7      OVRSH2  ; IF IT IS NEGATIVE, SHORT OVERSHOOT IS OCCURRING.
025D C68C    918      JZ      NOMOVE  ; IF IT IS ZERO, THEN MOVE IS COMPLETE.
919      ;
920      ;
921      ;
          ; SMALL MOVE REMAINING.
922      ;
923      ;
025F B82D    924      PREDCL: MOV  R0,#RCVDNM ; INSPECT THE
0261 F0      925      MOV      A,ØR0    ; 'NEXT MOVE RECEIVED' FLAG.
0262 C67B    926      JZ      DCLSTP  ; IF IT IS NOT SET, GO DECELERATE TO STOP.
927      ;
0264 B931    928      MOV      R1,#ØMVSN ; IF IT IS SET, THERE IS A NEXT MOVE TO EXECUTE.
0266 F1      929      MOV      A,ØR1    ; INSPECT THE SIGN OF THE NEXT MOVE
0267 B935    930      MOV      R1,#PRMVSN ; TO SEE IF IT IS IN THE SAME DIRECTION
0269 D1      931      XRL  A,ØR1    ; AS THE PRESENT MOVE.

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026A 967B	932	JNZ	DCLSTP	IF NOT, GO DECELERATE TO STOP.
026C C8	933			
026D FO	934	DEC	R0	IF NEXT MOVE IS IN SAME DIRECTION, THEN
026E 96BC	935	MOV	A,@R0	INSPECT THE 'INFINITE MOVE' FLAG.
	936	JNZ	INFMOV	IF SET, THEN NEXT MOVE IS A VIRTUAL
	937			'INFINITE EXTENSION' OF PRESENT MOVE.
	938			
	939			OTHERWISE, NEXT MOVE IS A
	940			SMALL EXTENSION OF THE PRESENT MOVE:
	941			
0270 B833	942	MOV	R0,#PRMVLO	ADD THE SMALL EXTENSION (I.E., SMALL NEXT MOVE)
0272 FO	943	MOV	A,@R0	TO THE PRESENT MOVE,
0273 B82F	944	MOV	R0,#NMMVLO	STORING THE SUM AS THE
0275 60	945	ADD	A,@R0	NEW NEXT MOVE.
0276 B2BC	946	JB5	INFMOV	
0278 A0	947	MOV	@R0,A	
0279 14F2	948	CALL	NEWMOV	CALL 'NEW MOVE' TO LOAD SUM AS PRESENT MOVE.
	949			
	950			
	951			
	952			DECELERATE TO A STOP.
	953			
027B FD	954	DCLSTP: MOV	A,R5	INSPECT VELOCITY SET POINT.
027C C6BF	955	JZ	UDRSHT	IF IT IS ZERO, THEN UNDERSHOOT IS OCCURRING.
027E FA	956	MOV	A,R2	OTHERWISE,
027F 0310	957	ADD	A,#10H	THE VELOCITY SHOULD NOT EXCEED THE
0281 F2D3	958	JB7	FNPLP1	POSITION ERROR PLUS SIXTEEN.
0283 AA	959	MOV	R2,A	
0284 37	960	CPL	A	
0285 6D	961	ADD	A,R5	
	962			
0286 F2D3	963	JB7	FNPLP1	(VELOCITY SET POINT) < (MOVE + 10) IS OK,
0288 FA	964	MOV	A,R2	OTHERWISE, REPLACE THE VELOCITY SET POINT
0289 AD	965	MOV	R5,A	BY THE AMOUNT OF THE MOVE.
028A 44D3	966	JMP	FNPLP1	
	967			
	968			
	969			
	970			NO MOVE REMAINS, BUT MOTOR IS IN MOTION.
	971			
028C B832	972	NOMOVE: MOV	R0,#PRSVL	CLEAR THE PRESENT VELOCITY LOCATION
028E A0	973	MOV	@R0,A	IN INTERNAL RAM AND ALSO
028F AD	974	MOV	R5,A	CLEAR THE VELOCITY SET POINT.
0290 14F2	975	CALL	NEWMOV	SEE IF A NEW MOVE IS WAITING TO EXECUTE.
0292 C646	976	JZ	PREPAR	IF THERE IS A NEW MOVE, RESTART PREPARATIONS.
	977			
0294 B92A	978	MOV	R1,#SPEED	OTHERWISE, USE PRESENT MOTOR SPEED
0296 F1	979	MOV	A,@R1	TO DETERMINE THE PROPER
0297 07	980	DEC	A	BRAKING PULSEWIDTH. NOTE THAT IF
0298 B936	981	MOV	R1,#PLSWTH	SPEED = 1, THEN NO BRAKING PW IS
029A A1	982	MOV	@R1,A	APPLIED (PREVENTS JITTER ON STOP).
	983			
029B FE	984	MOV	A,R6	GET REGISTER 6 FLAGS.
029C 5380	985	ANL	A,#SGNMSK	ISOLATE 'ABSOLUTE DIRECTION' FLAG.
029E 44B6	986	JMP	WRPW02	(JUMP TO LOCATION IN OVERSHOOT ROUTINE, BELOW)
	987			
	988			
	989			
	990			OVERSHOOT IS OCCURRING.
	991			
02A0 B83B	992	OVRSH1: MOV	R0,#LONGOV	LOAD THE 'LONG OVERSHOOT'
02A2 FO	993	MOV	A,@R0	PULSEWIDTH INTO ACCUMULATOR.
02A3 44A8	994	JMP	WRPW01	
	995			
02A5 B83C	996	OVRSH2: MOV	R0,#SHRTOV	LOAD THE 'SHORT OVERSHOOT'
02A7 FO	997	MOV	A,@R0	PULSEWIDTH INTO ACCUMULATOR.
	998			
02A8 B936	999	WRPW01: MOV	R1,#PLSWTH	WRITE THE PULSEWIDTH
02AA A1	1000	MOV	@R1,A	TO ITS INTERNAL RAM LOCATION.
	1001			
02AB FE	1002	MOV	A,R6	GET REGISTER 6 FLAGS.
02AC 12B3	1003	JBO	RITDIR	MOTION SHOULD BE OPPOSITE COMMANDED.


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02AE B82A      1004      MOV      RO,#SPEED      ; IF NOT, THEN ADD THE
02B0 F0        1005      MOV      A,@RO          ; PRESENT SPEED TO THE OVERSHOOT
02B1 61        1006      ADD      A,@R1         ; PULSEWIDTH FOR ADDITIONAL BRAKING.
02B2 A1        1007      MOV      @R1,A         ;
02B3 B835      1008      ;
02B5 F0        1009      RITDIR: MOV      RO,#PRMVSN ; LOAD PRESENT MOVE SIGN
02B6 B837      1010      MOV      A,@RO          ; INTO THE ACCUMULATOR.
02B8 3449      1011      ;
02BA 44D3      1012      WRPW02: MOV      RO,#SIGNPW ; LOAD ADDR OF PULSEWIDTH SIGN.
02B9 44D3      1013      CALL     PWDLRV        ; GO WRITE PULSEWIDTH WITH REVERSAL OF SIGN.
02BA 44D3      1014      JMP      FNPLP1        ; PREPARATIONS ARE FINISHED.
02B9 44D3      1015      ;
02B9 44D3      1016      ;.....
02B9 44D3      1017      ;
02B9 44D3      1018      ; INFINITE MOVE (I.E., >31) REMAINING.
02B9 44D3      1019      ;
02BC FD        1020      INFMOV: MOV      A,R5     ; INSPECT VELOCITY SET POINT,
02BD 96D3      1021      JNZ     FNPLP1        ; IF NOT ZERO, THEN MOVE IS BEING EXECUTED.
02BD 96D3      1022      ;
02BD 96D3      1023      ; ELSE, MOTOR IS OUT OF POSITION
02BD 96D3      1024      ; IN UNDERSHOOT DIRECTION.
02BF B933      1025      UDRSHT: MOV      R1,#PRMVLO ; INSPECT THE LOW BYTE
02C1 F1        1026      MOV      A,@R1         ; OF THE UNDERSHOOT.
02C2 B93B      1027      MOV      R1,#LONGOV   ; IF IT IS ZERO, ASSUME
02C4 96C7      1028      JNZ     LNGUND        ; SHORT AMOUNT OF UNDERSHOOT,
02C6 19        1029      INC      R1           ; ELSE, ASSUME LONG AMOUNT OF
02C7 F1        1030      LNGUND: MOV      A,@R1         ; UNDERSHOOT. LOAD PULSEWIDTH
02C8 B936      1031      MOV      R1,#PLSWTH   ; ACCORDINGLY.
02CA A1        1032      MOV      @R1,A         ;
02CB B835      1033      ;
02CD F0        1034      MOV      RO,#PRMVSN   ; LOAD PRESENT MOVE SIGN
02CE B837      1035      MOV      A,@RO          ; AS THE PROPER SIGN FOR
02D0 A0        1036      MOV      RO,#SIGNPW   ; THE PULSEWIDTH.
02D1 344B      1037      MOV      @RO,A         ;
02D1 344B      1038      ;
02D1 344B      1039      CALL     PWDLAY        ; GO WRITE TO PW LATCH, WITH A DELAY.
02D3 86D3      1040      ;
02D5 93        1041      FNPLP1: JNT     FNPLP1   ; WAIT UNTIL INTERRUPT IS NO LONGER ACTIVE.
02D5 93        1042      RETR     ; RETURN, RESTORING PSM.
02D5 93        1043      ;
02D5 93        1044      ;.....
02D5 93        1045      ;.....
02D5 93        1046      ;
02D5 93        1047      ; MULTIPLY SUBROUTINE:
02D5 93        1048      ;
02D5 93        1049      ; PROVIDE: COEFFICIENT ADDRESS IN RO,
02D5 93        1050      ; MULTIPLICAND IN ACCUMULATOR.
02D5 93        1051      ;
02D5 93        1052      ; RETURNS: PRODUCT OF COEFFICIENT AND
02D5 93        1053      ; MULTIPLICAND, DIVIDED BY SIXTEEN,
02D5 93        1054      ; IN ACCUMULATOR.
02D5 93        1055      ;
02D5 93        1056      ; CHANGES: ACCUM, FLAGS,
02D5 93        1057      ; R0: RO,R1,R2,R3,R4
02D5 93        1058      ; RB1: RO,R3
02D5 93        1059      ;
02D5 93        1060      ; CALLS: NONE
02D5 93        1061      ;
02D5 93        1062      ; CALLED BY: UPDATE PULSEWIDTH (UPDTPM)
02DF          1063      ORG      2DFH         ; START SUBROUTINES SO PAGE BOUNDARY IS GOOD.
02DF          1064      ;
02DF 37        1065      MLTNEG: CPL      A         ; TWO'S COMPLEMENT
02E0 17        1066      INC      A             ; THE MULTIPLICAND.
02E1 44E6      1067      JMP      MULT2         ; JUMP BACK INTO MULTIPLY ROUTINE.
02E1 44E6      1068      ;
02E3 AB        1069      MULT:   MOV      R3,A     ; STORE ORIGINAL MULTIPLICAND.
02E4 F2DF      1070      JNB     MLTNEG        ; IF MULTIPLICAND IS NEGATIVE, SPECIAL CASE.
02E6 C5        1071      MULT2:  SEL      R0       ; SELECT REGISTER BANK ZERO.
02E7 A9        1072      ;
02E7 A9        1073      MOV      R1,A         ; STORE MULTIPLICAND TIMES 1.00 IN R1.
02E8 E7        1074      ;
02E8 E7        1075      RL      A             ; MULTIPLY THE MULTIPLICAND BY TWO.

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02E9 A8	1076	MOV	R0,A	STORE MULTIPLICAND TIMES 2.00 IN R0.
	1077			
02EA F9	1078	MOV	A,R1	RECOVER MULTIPLICAND.
02EB 17	1079	INC	A	INCREMENT IT TO EFFECT ROUNDING UPWARD.
02EC 97	1080	CLR	C	CLEAR CARRY FOR NEXT DIVIDE BY TWO.
02ED 67	1081	RRC	A	DIVIDE IT BY TWO.
02EE AA	1082	MOV	R2,A	STORE MULTIPLICAND TIMES 1/2 IN R2.
	1083			(NOTE ROUNDING UPWARD)
02EF 97	1084	CLR	C	
02F0 67	1085	RRC	A	
02F1 AB	1086	MOV	R3,A	STORE MULTIPLICAND TIMES 1/4 IN R3.
	1087			
02F2 97	1088	CLR	C	
02F3 67	1089	RRC	A	
02F4 AC	1090	MOV	R4,A	MOVE MULTIPLICAND TIMES 1/8 INTO R4.
	1091			
02F5 97	1092	CLR	C	
02F6 67	1093	RRC	A	
02F7 AD	1094	MOV	R5,A	MOVE MULTIPLICAND TIMES 1/16 INTO R5.
	1095			
02F8 D5	1096	SEL	RB1	
02F9 F0	1097	MOV	A,@R0	OBTAIN COEFFICIENT TO USE AS MULTIPLIER.
02FA C5	1098	SEL	RB0	
	1099			
02FB B2FF	1100	JB5	ADDX2	IF BIT 5 IS SET, MLPLCD TIMES 2 IS ADDED IN.
02FD B800	1101	MOV	R0,*0H	OTHERWISE CLEAR THAT REGISTER.
	1102			
02FF 9203	1103	ADDX2: JB4	ADDX1	IF BIT 4 IS SET, MLPLCD TIMES 1 IS ADDED IN.
0301 B900	1104	MOV	R1,*0H	OTHERWISE CLEAR THAT REGISTER.
	1105			
0303 7207	1106	ADDX1: JB3	ADDHLF	IF BIT 3 IS SET, MLPLCD TIMES 1/2 IS ADDED IN.
0305 BA00	1107	MOV	R2,*0H	OTHERWISE CLEAR THAT REGISTER.
	1108			
0307 520B	1109	ADDHLF: JB2	ADD4TH	IF BIT 2 IS SET, MLPLCD TIMES 1/4 IS ADDED IN.
0309 B800	1110	MOV	R3,*0H	OTHERWISE CLEAR THAT REGISTER.
	1111			
030B 320F	1112	ADD4TH: JB1	ADD8TH	IF BIT 1 IS SET, MLPLCD TIMES 1/8 IS ADDED IN.
030D BC00	1113	MOV	R4,*0H	OTHERWISE CLEAR THAT REGISTER.
	1114			
030F 1213	1115	ADD8TH: JB0	ADDUP	IF BIT 0 IS SET, MLPLCD TIMES 1/16 IS ADDED IN.
0311 B000	1116	MOV	R5,*0H	OTHERWISE CLEAR THAT REGISTER.
	1117			
0313 FD	1118	ADDUP: MOV	A,R5	OBTAIN FIRST PARTIAL SUM (TIMES 1/16).
0314 6C	1119	ADD	A,R4	ADD IN NEXT PARTIAL SUM (TIMES 1/8).
0315 68	1120	ADD	A,R3	ADD IN NEXT PARTIAL SUM (TIMES 1/4).
0316 6A	1121	ADD	A,R2	ADD IN NEXT PARTIAL SUM (TIMES 1/2).
0317 69	1122	ADD	A,R1	ADD IN NEXT PARTIAL SUM (TIMES 1).
0318 68	1123	ADD	A,R0	ADD IN NEXT PARTIAL SUM (TIMES 2).
	1124			
0319 D5	1125	SEL	RB1	SELECT REGISTER BANK ONE.
	1126			
031A F221	1127	JB7	MAXPRD	IF BIT 7 IS SET, PRODUCT HAS OVERFLOWED.
031C 2B	1128	XCH	A,R3	RECOVER ORIGINAL MULTIPLICAND.
031D F225	1129	JB7	NEGPRD	IF IT IS NEGATIVE, GO NEGATE THE PRODUCT.
031F FB	1130	MOV	A,R3	OTHERWISE, RECOVER THE POSITIVE PRODUCT.
0320 83	1131	RET		
	1132			
0321 237F	1133	MAXPRD: MOV	A,*7FH	OBTAIN SIGN OF PRODUCT.
0323 641C	1134	JMP	MULT3	IF POSITIVE GO LOAD MAXIMUM POSITIVE VALUE.
	1135			
0325 FB	1136	NEGPRD: MOV	A,R3	RECOVER PRODUCT.
0326 37	1137	CPL	A	TWO'S COMPLEMENT
0327 17	1138	INC	A	THE PRODUCT.
0328 83	1139	RET		
	1140			
	1141			
	1142			
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0329 FE
032A 5380
032C B82A
032E 40
032F 8AC0
0331 2631
0333 90

0334 F0
0335 C67C

0337 18
0338 FE
0339 123F
033B F0
033C 07
033D 07
033F A0

0340 FF
0341 F27C
0343 D27C
0345 B000

0347 B833
0349 B934

034B 4308
034D AF

034E 125E

0350 FE
0351 1261

0353 F0
0354 07
0355 A0
0356 17
0357 9666
0359 F1
035A 07
035B A1
035C 6466

035E CF
035F 647C

0361 10
0362 F0
0363 9666
0365 11

PSNUPD: MOV A,R6
          ANL A,#SGNMSK
          MOV R0,#SPEED
          ORL A,@R0
          ORL D2,#XRAMEN
PSNLP1: JNT0 PSNLP1
          MOVX @R0,A

          MOV A,@R0
          JZ PSNFIN

          INC R0
          MOV A,R6
          JBO MTNOP1
          MOV A,@R0
          DEC A
          DEC A
          MOV @R0,A
          INC @R0

          MOV A,R7
          PSNFIN
          JBO PSNFIN
          MOV @R0,#0

          MOV R0,#PRMVLO
          MOV R1,#PRMVHI

          ORL A,#8H
          MOV R7,A

          JBO PSNSAM

          MOV A,R6
          JBO MTNOP2

          MOV A,@R0
          DEC A
          MOV @R0,A
          INC A
          JNZ PSNSSET
          MOV A,@R1
          DEC A
          MOV @R1,A
          PSNSSET

PSNSAM: DEC R7
          JMP PSNFIN

MTNOP2: INC @R0
          MOV A,@R0
          JNZ PSNSSET
          INC @R1

```

```

} RETURNS: UPDATED VELOCITY IN EXTERNAL RAM.
} IF ENCODER POSITION IS 0,0 THE VALUES
} OF REMAINING MOVE, ABSOLUTE POSITION, AND
} 'ENCODER POSITION 0,0' FLAG ARE UPDATED.
}
} CHANGES: R0,R1,R3,R7,QTAIL,LO&HI PRSMOV
} EXTERNAL RAM LOCS LO&HI ABS POS.
}
} CALLS: NONE
}
} CALLED BY: INTERRUPT SERVICE ROUTINE
}
} OBTAIN REGISTER 6 FLAGS.
} ISOLATE THE 'ABSOLUTE DIRECTION' FLAG.
} CONCATENATE THE DIRECTION BIT
} WITH THE SPEED AND WRITE IT
} TO THE VELOCITY LOCATION IN EXTERNAL RAM.
}
} INSPECT THE SPEED.
} IF SPEED IS ZERO, POSITION HAS NOT CHANGED.
}
} INCR TO ADDR OF QUARTER-HOLE TAIL.
} INSPECT THE 'RELATIVE DIRECTION' FLAG.
} IF MOTION IS OPPOSITE COMMANDED,
} THEN QUARTER-HOLE TAIL MUST BE INCREMENTED.
} IF MOTION IS IN THE COMMANDED DIRECTION,
} THEN QUARTER-HOLE TAIL MUST BE
} DECREMENTED.
}
} OBTAIN REGISTER 7 FLAGS AND ENCODER BIT DATA.
} IF BIT 7 SET, ENCODER NOT ON 0,0.
} IF BIT 6 SET, ENCODER NOT ON 0,0.
} OTHERWISE, POSITION IS 0,0 SO CLEAR Q-H TAIL.
} AND UPDATE PRESENT MOVE AND ABSOLUTE POSITION:
}
} SET ADDRESS POINTERS TO
} LOW AND HIGH BYTES OF MOVE COMMAND.
} (SAME ADDRESSES FOR ABSOLUTE POSITION BYTES.)
}
} SET THE 'ENCODER POSITION 0,0' FLAG.
}
} IF 'REVERSAL SINCE LAST UPDATE' FLAG IS SET,
} POSITION IS THE SAME AS IT WAS AT LAST UPDATE.
}
} OBTAIN REGISTER 6 FLAGS.
} IF 'RELATIVE DIRECTION' FLAG IS SET, MOTION
} IS OPPOSITE COMMANDED, SO MOVE IS INCREMENTED.
}
} OTHERWISE, MOTION IS IN COMMANDED DIRECTION,
} SO MOVE IS DECREMENTED.
}
} (NOTE THAT HIGH BYTE MUST BE DECREMENTED
} ONLY IF LOW BYTE WAS EQUAL TO ZERO)
}
} PC BRANCES HERE WHEN 'REVERSAL SINCE LAST
} UPDATE FLAG IS SET. CLEAR THAT FLAG.
} (POSITION IS THE SAME AS AT LAST UPDATE.)
}
} SINCE MOTION IN OPPOSITE COMMANDED,
} MOVE MUST BE INCREMENTED.
} (NOTE HIGH BYTE IS ONLY INCREMENTED IN
} CASE LOW BYTE BECOMES ZERO ON INCREMENT.)

```

```

0366 FE      1220
1221 PSNSET: MOV    A,R6      } OBTAIN REGISTER 6 FLAGS.
1222          }
0367 F273    1223          JB7  MTNOP3      } IF 'ABSOLUTE DIRECTION' FLAG IS SET, THEN ABSOLUTE
0369 80      1224          MOVX  A,@R0      } POSITION IS DECREMENTED (BELOW) SINCE MOVE IS
036A 17      1225          INC   A          } COUNTERCLOCKWISE. OTHERWISE, IF 'ABSOLUTE POS-
036B 90      1226          MOVX  @R0,A      } ITION' FLAG IS CLEAR, THEN ABSOLUTE POSITION
036C 967C    1227          JNZ  PSNFIN    } MUST BE INCREMENTED, SINCE MOVE IS CLOCKWISE.
036E 81      1228          MOVX  A,@R1      }
036F 17      1229          INC   A          } (NOTE HIGH BYTE IS ONLY INCREMENTED
0370 91      1230          MOVX  @R1,A      } IF LOW BYTE INCREMENTS TO ZERO.)
0371 647C    1231          JMP   PSNFIN    }
1232          }
0373 80      1233 MTNOP3: MOVX  A,@R0      } MOVE IS COUNTER-CLOCKWISE,
0374 07      1234          DEC   A          } SO DECREMENT ABSOLUTE POSITION.
0375 90      1235          MOVX  @R0,A      }
0376 17      1236          INC   A          } (NOTE HIGH BYTE IS ONLY DECREMENTED IF
0377 967C    1237          JNZ  PSNFIN    } LOW BYTE WAS PREVIOUSLY ZERO.)
0379 81      1238          MOVX  A,@R1      }
037A 07      1239          DEC   A          }
037B 91      1240          MOVX  @R1,A      }
1241          }
037C 9A00    1242 PSNFIN: ANL   P2,#IDLE } CLEAR ENABLE ADDRESS FROM PORT 2.
037E 83      1243          RET          }
1244          }
1245          } .....
1246          } .....
1247          }
1248          }
0380          1249          ORG   380H      } START VELOCITY LOOKUP TABLE HERE
1250          } (SECOND HALF OF PAGE THREE).
1251          }
1252          }
1253          }
0380 FE      1254          DB    OFEH, OFEH, OFCH, OFAH, OF8H, OF6H, OF5H, OF3H }
0381 FE      }
0382 FC      }
0383 FA      }
0384 F8      }
0385 F6      }
0386 F5      }
0387 F3      }
1254          }
0388 F1      1255          DB    OF1H, OFFH, OEDH, OECH, OEAH, OE8H, OE7H, OE5H }
0389 FF      }
038A ED      }
038B EC      }
038C EA      }
038D E8      }
038E E7      }
038F E5      }
1256          }
0390 E4      1257          DB    OE4H, OE2H, OE0H, ODFH, ODDH, ODCH, ODAH, OD9H }
0391 E2      }
0392 E0      }
0393 DF      }
0394 DD      }
0395 DC      }
0396 DA      }
0397 D9      }
1258          }
0398 D8      1259          DB    OD8H, OD6H, OD5H, OD3H, OD2H, OD1H, OCFH, OCEH }
0399 D6      }
039A D5      }
039B D3      }
039C D2      }
039D D1      }
039E CF      }
039F CE      }
1260          }
03A0 CD      1261          DB    OCDH, OCCH, OCAH, OC9H, OC8H, OC7H, OC5H, OC4H }
03A1 CC      }
03A2 CA      }

```

03A3	C9					
03A4	C8					
03A5	C7					
03A6	C5					
03A7	C4					
		1262				
03A8	C3	1263	DB	0C3H, 0C2H, 0C1H, 0C0H, 0BFH, 0BDH, 0BCH, 0BBH		}
03A9	C2					
03AA	C1					
03AB	C0					
03AC	BF					
03AD	BD					
03AE	BC					
03AF	BB					
		1264				
03B0	BA	1265	DB	0BAH, 0B9H, 0B8H, 0B7H, 0B6H, 0B5H, 0B4H, 0B3H		}
03B1	B9					
03B2	B8					
03B3	B7					
03B4	B6					
03B5	B5					
03B6	B4					
03B7	B3					
		1266				
03B8	B2	1267	DB	0B2H, 0B1H, 0B0H, 0AFH, 0AEH, 0ADH, 0ACH, 0ACH		}
03B9	B1					
03BA	B0					
03BB	AF					
03BC	AE					
03BD	AD					
03BE	AC					
03BF	AC					
		1268				
03C0	AB	1269	DB	0ABH, 0AAH, 0A9H, 0A8H, 0A7H, 0A6H, 0A5H, 0A5H		}
03C1	AA					
03C2	A9					
03C3	A8					
03C4	A7					
03C5	A6					
03C6	A5					
03C7	A5					
		1270				
03C8	A4	1271	DB	0A4H, 0A3H, 0A2H, 0A1H, 0A1H, 0A0H, 9FH, 9EH		}
03C9	A3					
03CA	A2					
03CB	A1					
03CC	A1					
03CD	A0					
03CE	9F					
03CF	9E					
		1272				
03D0	9E	1273	DB	9EH, 9DH, 9CH, 9BH, 9BH, 9AH, 99H, 98H		}
03D1	9D					
03D2	9C					
03D3	9B					
03D4	9B					
03D5	9A					
03D6	99					
03D7	98					
		1274				
03D8	98	1275	DB	98H, 97H, 96H, 96H, 95H, 94H, 94H, 93H		}
03D9	97					
03DA	96					
03DB	96					
03DC	95					
03DD	94					
03DE	94					
03DF	93					
		1276				
03E0	92	1277	DB	92H, 92H, 91H, 90H, 90H, 8FH, 8EH, 8EH		}
03E1	92					
03E2	91					

NEGPRD	1129	1136*							
NEWFIN	514	532*							
NEWLP1	520*	524							
NEWMOV	480	508*	948	975					
NOMOVE	918	972*							
NOPLL	328*	336							
NOPLUD	883*	886							
NOSTAL	651	685*							
NXMHVHI	79*								
NXMHVLO	78*	944							
NXMHVNF	74*	444	414						
NXMHVSN	80*	928							
NXTVEL	77*								
OVFLW	572	597*							
OVR	6*	310							
OVRSH1	904	992*							
OVRSH2	917	996*							
PEEK	390*								
PLSMTH	89*	470	481	676	681	981	999	1031	
POKE	387	397*							
PREDCL	913	924*							
PREMAX	863	866*							
PREPAR	902*	976							
PRMVHI	85*	447	902	1188					
PRMVLO	83*	369	942	1025	1187				
PRMVSN	87*	457	564	750	930	1009	1034		
PRSVEL	82*	519	972						
PSNFIN	1170	1182	1183	1213	1227	1231	1237	1242*	
PSNLP1	1166*	1166							
PSNSAM	1194	1212*							
PSNSET	1205	1209	1218	1221*					
PSNUPD	669	895	1161*						
PWO	669*	883							
PWDLAY	611*	689	1039						
PWDLRV	610*	1013							
PWHYST	574*	619							
PWLTEN	39*	583	613						
PWRVRS	566	589*							
PWSIGN	575	580*	602						
PWULP1	617*	617							
PWUPDT	559*	893							
PWWRIT	234	582*	678						
QHTAIL	69*	476	915						
RAMADR	64*	383							
RAMDAT	63*								
RAMPK	10*	394							
RCVDNM	75*	510	924						
RDMBX	251*	529							
RDYMSG	352	529*							
RDYNXT	9*	520							
RESEND	265	335*							
RESET	281	68*							
RESLP1	371*	371							
RITDIR	1003	1009*							
RSNDRQ	261	310*							
SGNMSK	174*	456	610	985	1162				
SHFRT	794*	802							
SHIFT	775	778	796	802*					
SHRTOV	98*	996							
SIGNPM	90*	459	562	670	1012	1036			
SPEED	66*	666	815	978	1004	1163			
STALL1	648*	683							
STLLCK	673	681*							
STPCNT	60*	462	526	648	706				
STRTPM	95*	468							
TRNSIT	659	690*							
UDRSHT	955	1025*							
UPDATE	876	879	882*						
UPDPW	882	886*							
UPPER7	177*	731							
VELCTY	814*								
VELDET	754	762*							

VELLP1	785*	792					
VELNEW	763	777*					
VELSHF	788	798*					
VELSLO	768	780*					
WRILP1	320*	324					
WRITE	249	316*	395				
WRPWO	672	675*	686				
WRPWO1	994	999*					
WRPWO2	986	1012*					
XRAMEN	41*	216	289	368	380	413	1165

CROSS REFERENCE COMPLETE

APPENDIX Y. LISTINGS OF THE INPUT/OUTPUT PROCEDURES ON VAX

The VAX program calls these external procedures to communicate in 8-bit format with the 8751 serial port. They are external to the main program because they are written in FORTRAN, while the main program is in PASCAL.

At this writing, the main VAX input/output system call was SYS\$QIO. These programs call that routine, and make use of some other system calls and constants. It seems at this point that there is not much reason to explain the functioning of these routines because they will all be defunct within two months of this writing, when a new operating system is to be installed on VAX. However, the routines are included here for the sake of completeness.

```

0001
0002 c      This subroutine derives from the READ_TWO subroutine
0003 c      written by Dr. Roger Ehrich of the Virginia Tech Computer
0004 c      Science Department.
0005
0006 c
0007 c      RHINORD (device,keybuff,rhinobuff,term,flag1,chan1)
0008 c
0009 c      RHINORD attempts to read a character from two terminals
0010 c      simultaneously and returns the character that is read first.
0011 c      device character*(*), the name of the rhino communication line.
0012 c      keybuff byte, code from the keyboard is returned in this buffer.
0013 c      rhinobuff byte, code from the rhino is returned in this buffer.
0014 c      term byte, identifies the source of the character:
0015 c      0 means the login terminal and 1 means the rhino.
0016 c      flag1 the event flag used for communication with the rhino
0017 c      chan1 the channel used for communication with the rhino
0018 c
0019 c      The logical device can be given in upper or lower case, with or without
0020 c      trailing blanks
0021 c
0022 c      subroutine rhinord (device,keybuff,rhinobuff,term,flag1,chan1)
0023
0024 CHARACTER*(*) device
0025 CHARACTER*63 updevice
0026 BYTE keybuff,rhinobuff,term,call_flag /0/
0027 INTEGER*4 chan0,chan1,terminators(2) /0,0/
0028 INTEGER*4 flag0,flag1,mask,op0,op1,state
0029 EXTERNAL io$_readvblk,io$_noecho,io$_nofiltr
0030 EXTERNAL io$_ttyreadall
0031
0032 c      The first time this subroutine is called from the rhinocom
0033 c      program, this part of it gets event flags and channels
0034 c      assigned for the rhino line and the login terminal. After
0035 c      the first call, the call_flag is never zero again, so this
0036 c      part of the subroutine is skipped over.
0037
0038 if (call_flag.eq.0) then
0039     j=index (device/' ',' ')-1
0040     call str$upcase (updevice,device)
0041     call sys$assign ('TT',chan0,,)
0042     call sys$assign (updevice(1:j),chan1,,)
0043
0044     n=62
0045     do while (lib$reserve_ef(n).ne.1)
0046         n=n-1
0047     end do
0048     flag0=n
0049     do while (lib$reserve_ef(n).ne.1)
0050         n=n-1
0051     end do

```

```

0052         flag1=n
0053
0054         mask=2**(flag0-32)+2**(flag1-32)
0055
0056         op0=ior (%loc (io$_readvblk),%loc (io$_nofiltr))
0057
0058         op1=ior (%loc (io$_ttyreadall),%loc (io$_noecho))
0059
0060         call_flag=1
0061     end if
0062
0063 c     Makes two simultaneous read requests
0064 c     using the system i/o routine:
0065
0066         call sys$qio (%val (flag0),%val (chan0),%val (op0),,,,keybuff,%val(1)
0067         1,,terminators,,)
0068         call sys$qio (%val (flag1),%val (chan1),%val (op1),,,,rhinobuff,%val(1)
0069         1,,terminators,,)
0070
0071
0072 c     Wait for the logical or of the event flags to become set,
0073 c     indicating that one of the read requests has been filled:
0074
0075 10     call sys$wflor (%val (flag0),%val (mask))
0076
0077
0078 c     Get the system event flags:
0079
0080         call sys$readef (%val (flag0),state)
0081
0082
0083 c     If the flag assigned to the login terminal is set,
0084 c     then clear the 'term' flag and cancel the read request
0085 c     of the rhino channel:
0086
0087         if (iand (state,2**(flag0-32)).ne.0) then
0088             term=0
0089             call sys$cancel (%val (chan1))
0090             go to 20
0091         end if
0092
0093
0094 c     If the flag assigned to the rhino is set, then set
0095 c     the 'term' flag and cancel the read request
0096 c     of the login terminal channel:
0097
0098         if (iand (state,2**(flag1-32)).ne.0) then
0099             term=1
0100             call sys$cancel (%val (chan0))
0101             go to 20
0102         end if

```

```

0103
0104   c   If neither event flag is set, go wait for the
0105   c   logical-or of them to be high:
0106
0107           go to 10
0108
0109   20   return
0110
0111           end

```

PROGRAM SECTIONS

Name	Bytes	Attributes
0 \$CODE	418	PIC CON REL LCL SHR EXE RD NOWRT LONG
1 \$PDATA	5	PIC CON REL LCL SHR NOEXE RD NOWRT LONG
2 \$LOCAL	300	PIC CON REL LCL NOSHR NOEXE RD WRT LONG
Total Space Allocated	723	

ENTRY POINTS

Address	Type	Name
0-00000000		RHINORD

VARIABLES

Name	Address	Type	Name	Address	Type	Name	Address	Type	Name
2-00000047	L*1	CALL_FLAG	2-00000048	I*4	CHAN0	AP-00000018@	I*4	CHAN1	
2-0000004C	I*4	FLAG0	AP-00000014@	I*4	FLAG1	2-00000060	I*4	J	
2-00000050	I*4	MASK	2-00000064	I*4	N	2-00000054	I*4	OPO	
AP-0000000C@	L*1	RHINOBUF	2-0000005C	I*4	STATE	AP-00000010@	L*1	TERM	

UPDEVICE

ARRAYS

Address	Type	Name	Bytes	Dimensions
2-00000000	I*4	TERMINATORS	8	(2)

LABELS

Address	Label	Address	Label
0-0000012E	10	0-000001A1	20

FUNCTIONS AND SUBROUTINES REFERENCED

Type	Name	Type	Name
	IOSM_NOECHO		IOSM_NOFILTR
	IOS_TTYREADALL	I*4	LIB\$INDEX
	STR\$UPCASE		SYSS\$ASSIGN
	SYSS\$QIO		SYSS\$READEF
			IOS_READVBLK
		I*4	LIB\$RESERVE_EF
			SYSS\$CANCEL
			SYSS\$WFLOP

COMMAND QUALIFIERS

```

FORTRAN /LIS RHINORD
/CHECK=(NOBOUNDS,OVERFLOW,NOUNDERFLOW)
/DEBUG=(NOSYMBOLS,TRACEBACK)
/STANDARD=(NOSYNTAX,NOSOURCE_FORM)
/SHOW=(NOPREPROCESSOR,NOINCLUDE,MAP)

```

/F77 /NOG_FLOATING /I4 /OPTIMIZE /WARNINGS /NOD_LINES /NOCROSS_REFERENCE /NOMACHINE_CODE
COMPILATION STATISTICS

Run Time: 1.70 seconds
Elapsed Time: 2.92 seconds
Page Faults: 385
Dynamic Memory: 122 pages

```

0001 c This subroutine derives from the TT_WRITE subroutine, written by
0002 c Dr. Roger Ehrich of the Virginia Tech Computer Science Department.
0003
0004
0005 c RHINOWR (efn,channel,buffer)
0006 c
0007 c RHINOWR writes one byte to the specified channel and returns
0008 c when the information transfer is complete.
0009 c RHINOWR is designed to write 8-bit bytes to any
0010 c allocated terminal without physical I/O privileges.
0011 c efn integer*4, the event flag to be used
0012 c channel integer*4, the channel assigned to the communication
0013 c buffer byte, the data to be sent
0014 c
0015 c All 256 8 bit bytes can be written
0016 c
0017
0018 c subroutine rhinowr (efn,channel,buffer)
0019
0020 c BYTE buffer
0021 c INTEGER*4 efn,channel,status,msgvec(3)
0022 c INTEGER*4 sys$qiow,sys$qiow,operation
0023 c DATA msgvec /'F0001',x,0,0/
0024 c EXTERNAL io$writevblk,ss$_normal,io$m_noformat
0025
0026
0027 c Define the particular output operation to be performed
0028 c by the vax i/o system call:
0029
0030 c operation=ior (%loc (io$writevblk),%loc (io$m_noformat))
0031
0032
0033 c Make the system output call with a wait for execution
0034 c and with a status code returned indicating whether
0035 c execution was normal:
0036
0037 c status=sys$qiow (%val (efn),%val (channel),%val (operation),
0038 c 1 ,,,buffer,%val (1),,,)
0039
0040
0041 c If the status code indicates abnormal execution,
0042 c stop program execution and print a message:
0043
0044 c if (status.ne.%loc (ss$_normal)) then
0045 c msgvec(2)=status
0046 c call sys$putmsg (msgvec,,'SS')
0047 c stop 'STOP from RHINOWR'
0048 c end if
0049
0050 c return
0051 c end

```

PROGRAM SECTIONS

Name	Bytes	Attributes
0 \$CODE	94	PIC CON REL LCL SHR EXE RD NOWRT LONG
1 \$PDATA	20	PIC CON REL LCL SHR NOEXE RD NOWRT LONG
2 \$LOCAL	108	PIC CON REL LCL NOSHR NOEXE RD WRT LONG
Total Space Allocated	222	

ENTRY POINTS

Address	Type	Name
0-00000000		RHINOWR

VARIABLES

Name	Address	Type	Name	Address	Type	Name
AP-0000000C@ L*1	AP-00000008@	I*4	CHANNEL	AP-00000004@	I*4	EFN
OPERATION	2-0000000C	I*4	STATUS	2-00000010	I*4	SYSSQIO

ARRAYS

Address	Type	Name	Bytes	Dimensions
2-00000000	I*4	MSGVEC	12	(3)

FUNCTIONS AND SUBROUTINES REFERENCED

Type	Name	Type	Name	Type	Name	Type	Name
	IOSM_NOFORMAT		IOS_WRITEVBLK		SS\$_NORMAL		SYSSPUTMSG

COMMAND QUALIFIERS

FORTRAN /LIS RHINOWR
 /CHECK=(NOBOUNDS,OVERFLOW,NOUNDERFLOW)
 /DEBUG=(NOSYMBOLS,TRACEBACK)
 /STANDARD=(NOSYNTAX,NOSOURCE_FORM)
 /SHOW=(NOPREPROCESSOR,NOINCLUDE,MAP)
 /F77 /NOG_FLOATING /I4 /OPTIMIZE /WARNINGS /NOD_LINES /NOCROSS_REFERENCE /NOMACHINE_CODE

COMPILATION STATISTICS

Run Time: 0.71 seconds
 Elapsed Time: 1.71 seconds
 Page faults: 354
 Dynamic Memory: 117 pages

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