Active Source Management to Maintain High Efficiency in Resonant Conversion over Wide Load Range

by

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Abstract

High-frequency and large amplitude current is a driving requirement for applications such as induction heating, wireless power transfer, power amplifier for magnetic resonant imaging, electronic ballasts, and ozone generators. Voltage-fed resonant inverters are normally employed, however, current-fed (CF) resonant inverters are a competitive alternative when the quality factor of the load is significantly high. The input current of a CF resonant inverter is considerably smaller than the output current, which benefits efficiency. A simple, parallel resonant tank is sufficient to create a high-power sinusoidal signal at the output. Additionally, input current is limited at the no-load condition, providing safe operation of the system. Drawbacks of the CF resonant inverter are associated with the implementation of the equivalent current source. A large input inductor is required to create an equivalent dc current source, to reduce power density and the bandwidth of the system. For safety, a switching stage is implemented using bidirectional voltage-blocking switches, which consist of a series connection of a diode and a transistor. The series diode experiences significant conduction loss because of large on-state voltage. The control of the output current amplitude for constant-frequency inverters requires a pre-regulation stage, typically implemented as a cascaded hard-switched dc/dc buck converter. The pre-regulation also reduces the efficiency.

In this dissertation, a variety of CF resonant inverters with two input inductors and two grounded switches are investigated for an inductive-load driver with loaded quality factor larger than ten, constant and high-frequency (~500 kHz) operation, high reactive output power (~14 kVA), high bandwidth (~100 kHz), and high efficiency (over 95 %). The implementation of such system required to question the fundamental operation of the CF resonant inverter. The input inductance is reduced by around an order of magnitude, ensuring sufficient bandwidth, and allowing rich harmonic content in the input current. Of particular importance are fundamental and second harmonic components

since they influence synchronization of the zero-crossing of the output voltage and the turn-on of the switches. The synchronization occurs at a particular frequency, termed synchronous frequency, and it allows for zero switching loss in the switches, which greatly boosts efficiency. The synchronous conditions were not know prior this work, and the dependence among circuit parameters, input current harmonics, and synchronous frequency are derived for the first time. The series diode of the bidirectional switch can reduce the efficiency of the system to below 90 %, and has to be removed from the system. The detrimental current-spikes can occur if the inverter is not operated in synchronous condition, such as in transients, or during parametric variations of the load coil. The resistance of the load coil has a wide variance, five times or more, while the inductance changes as well by a few percent. To accommodate for non-synchronous conditions, a low-loss current snubber is proposed as a safety measure to replace lossy diodes. The center-piece of the dissertation is the proposal of a two-phase zero-voltage switching buck pre-regulator, as it enables fixed frequency and synchronous operation of the inverter under wide parametric variations of the load. The synchronous operation is controlled by phase-shifting the switching functions of the pre-regulator and inverter. The pre-regulator reduces the dc current in the input inductors, which is a main contributor to current stress and conduction losses in the inverter switches. Total loss of the inverter switches is minimized since no switching loss is present and minimal conduction losses are allowed. The dc current in the input inductors, once seen as a means to transfer power to load, is now contradictory perceived as parasitic, and the power is transferred to the load using a fundamental frequency harmonic! The input current to the resonant tank, previously designed to be a square-wave, now resembles a sine-wave with very rich harmonic content. Additionally, the efficiency of the pre-regulator at heavy-load condition is improved by ensuring ZVS for with an additional inductive tank.

The dissertation includes five chapters. The first chapter is an introduction to current-fed resonant inverters, applications, and state-of-the-art means to ensure constant frequency operation under load's parametric variations. The second chapter is dedicated to the optimization of the CF resonant inverter topology with a dc input voltage, two input inductors, and two MOSFETs. The topology is termed as a boost amplifier. If the amplifier operates away from the synchronous frequency, detrimental current spikes will flow though the switches since the series diodes are eliminated. Current spikes reduce the efficiency up to few percent and can create false functioning of the system. Operation at the synchronous frequency is achieved with large, bulky, input inductors, typically around 1-2 mH or higher, when the synchronous frequency follows the resonant frequency of the tank at 500 kHz. The input inductance cannot be reduced arbitrarily to meet the system bandwidth requirement, since the synchronous frequency is increased

based on the inductance value. The relationship between the two (input inductance and the synchronous frequency) was unknown prior this work. The synchronous frequency is determined to be a complicated mathematical function of harmonic currents through the input inductors, and it is found using the harmonic decomposition method. As a safety feature, a current snubber is implemented in series with the resonant tank. Snubber utilizes a series inductance of cable connection between the tank and the switching stage, and it is more efficient than the previously employed series diodes. Topology optimization and detailed design procedure are provided with respect to efficiency and system dynamics. The mathematics is verified by a prototype rated at 14 kVA and 1.25 kW. The input inductance is reduced by around an order of magnitude, with the synchronous frequency increase of 2 %. The efficiency of the power amplifier reached 98.5 % and might be improved further with additional optimization. Silicon carbide MOSFETs are employed for their capability to operate efficiently at high frequency, and high temperature.

The third chapter is dedicated to the development of the boost amplifier's large signal model using the Generalized State-space Averaging (GSSA) method. The model accurately predicts amplifier's transient and steady-state operation for any type of input voltage source (dc, dc with sinusoidal ripple, pulse-width modulated), and for either synchronous or non-synchronous operating frequency. It overcomes the limitation of the low-frequency model, which works well only for dc voltage-source input and at synchronous frequency. As the measure of accuracy, the zero-crossing of the resonant voltage is predicted with an error less than 2° over a period of synchronous operation, and for a range of interest for input inductance (25 μH – 1000 μH) and loaded-quality factor (10 – 50). The model is validated both in simulation and hardware for start-up transient and steady-state operation. It is then used in the synthesis of modulated output waveforms, including Hann-function and trapezoidal-function envelopes of the output voltage/current.

In the fourth chapter, the GSSA model is employed in development of the PWM compensation method that ensures synchronous operation at constant frequency for the wide variation of the load. The boost amplifier is extended with a cascaded pre-regulator whose main purpose is to control the output resonant voltage. The pre-regulator is implemented as two switching half-bridges with same duty-cycle and phase-shift of 180°. The behavior of the cascaded structure is the same as of the buck converter, so the half-bridges are named buck pre-regulators. ZVS operation is ensured by putting an inductive tank between the half-bridges. Each output of half-bridges is connected to each of input inductors of the boost to provide the PWM excitation. Using the GSSA model, the synchronous condition and control laws are derived for the amplifier. Properties of the current harmonics in the input inductors are

well examined. It is discovered that the dc harmonic, once used to transfer power, is unwanted (parasitic) since it increases conduction loss in switches of the boost. A better idea is to use the fundamental harmonic for power transfer, since it does not create loss in the switches. Complete elimination of the dc current is not feasible for constant frequency operation of the amplifier since the dc current depends on the load coil's resistance. However, significant mitigation of around 55 % is easily achievable. The proposed method improves significantly the efficiency of both the buck pre-regulator and the boost. Synchronous operation is demonstrated in hardware for fixed switching frequency of 480 kHz, power level up to 750 W, input voltage change from 300 V to 600 V, load coil's resistance change of three times, and load coil's inductance change of 3.5 %. Measured efficiency is around 95 %, with a great room for improvements. Chapter five summarizes key contributions and concludes the dissertation.

To my late and beloved mother Olga

My source of inspiration and dedication

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Chapter 1. Introduction

1.1. Resonant Inverters for Inductive Loads

High-frequency current is an excitation requirement for a large number of applications including wireless power transfer (WPT), fluorescent lighting, magnetic resonance imaging, ozone generation, ultrasonic generators, antenna drivers, induction heating, welding, and cooking. In recent years, rapid development have been made in the areas of WPT, induction cookers, and fluorescent lighting, while induction heaters are improving more slowly since it is mature area. Resonant power inverter topologies are normally used to create high-frequency currents for their superior efficiency at high switching frequency, thanks to soft-switching techniques that minimize switching losses [1]. For inductive loads, high-frequency current is converted to magnetic field in order to transfer power, heat-up surrounding objects by inducing eddy currents, or send information. The inductive load presents itself as a low impedance at the resonant frequency, necessitating large excitation current for high output power. The load current has to be scaled down so the switching stage of the resonant inverter has low conduction loss and good efficiency.

1.1.1. Voltage-fed Resonant LCL Inverter

A voltage-fed LCL resonant inverter is the standard topology where isolation of the load is not required (Figure 1-1) [2], [3]. The switching stage inverts the input voltage source, and the resonant tank has a square-wave or a pulse-width modulated voltage at its input. At the resonant frequency defined with L_r and C_r, a high current gain exists between the inductors L_1 and L_r. The current gain equals to the ratio of L_1 and L_r. Input impedance to the resonant tank is slightly inductive, and zero-voltage switching is maintained for all switches in the full-bridge configuration.

Many control methods exist to control the amplitude of the output, and the power level. The output voltage/current is proportional to the input voltage, so the basic method is to control the input voltage using a pre-regulation stage [3]. Complexity, cost, and efficiency reduction are associated with the pre-regulator, so frequency control [4] or various pulse-width modulated methods are usually implemented as an inexpensive alternative.

Power level is scaled up using a multi-phase design [5], [6]. The switching functions of each phase are interleaved, so fixed frequency, high-power operation is possible with ensured ZVS for all switches. The voltage-fed topology is characterized with excellent efficiency because of ZVS and load current matching.

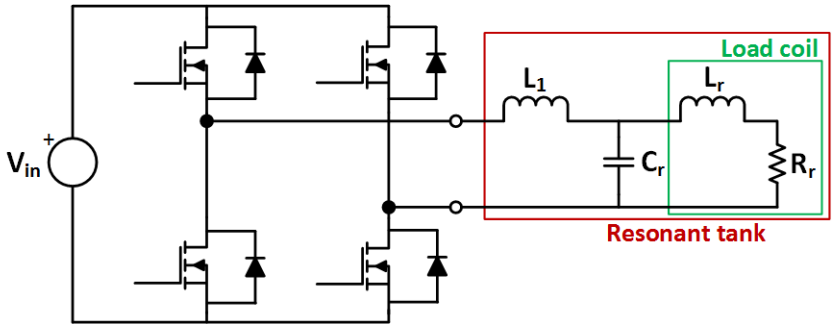


Figure 1-1. Voltage-fed LCL resonant inverter.

1.1.2. Current-fed Parallel Resonant Inverter

Dual topology to the voltage-fed inverter is a current-fed parallel resonant inverter [3], [7] in Figure 1-2. It uses a combination of the voltage source and the series inductor to create dc current source. The switching stage inverts the input current and delivers a square-wave current waveform to the resonant tank. The parallel resonant tank boosts the input current to the tank and the load has Q-times larger current where Q is the quality-factor of the load coil. Output voltage/current amplitude is controlled by varying input voltage using a pre-regulator or by controlling switching frequency. Scaling the power up is done by paralleling transistors, since the output capacitance is in parallel with the output capacitor. The current-fed inverter has limitations in power density and system bandwidth due to large input inductor, efficiency due to loss of series diodes, and a number of applicable control methods. However, the current-fed topology is attractive alternative to the voltage-fed topology when the loaded quality-factor is high [8].

1.1.3. Current-fed Parallel Resonant Inverter with Two Input Inductors

When power level or frequency is particularly high, top switches can be eliminated from the topology as shown in Figure 1-2. Further, series diodes can be eliminated if the turn-on of the switches is synchronized with the

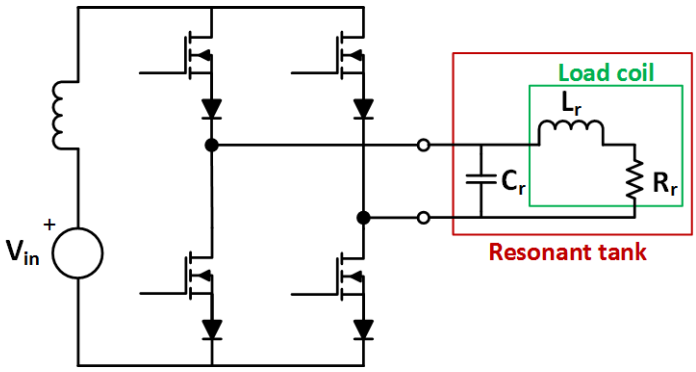


Figure 1-2. Current-fed parallel resonant inverter with single input inductor.

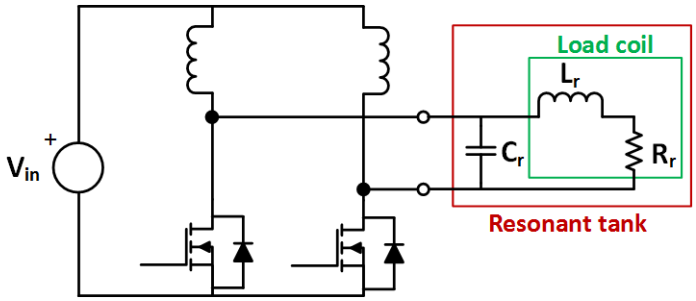


Figure 1-3. Current-fed parallel resonant inverter with two input inductors. Series diodes in switch configuration can be eliminated if voltage of the resonant tank is synchronized with the switching of MOSFETs. If synchronization is not achieved, current spikes appear in MOSFETs which may cause failure.

zero-crossing of the output voltage. The resultant topology has only grounded switches and it is shown in Figure 1-3. The reliability may not be great due to absence of series diodes [9]. Low power density, bandwidth, and limited control options characterize this topology, the same as in previous case.

1.1.4. Current-fed Parallel Resonant Inverter with Two Input Inductors under Parametric Variations of the Load at Constant Switching Frequency

The resonant inverter in Figure 1-3 will suffer from cross-conduction of the switches when operating at constant switching frequency due to parametric variations of the load. At particular frequency, termed synchronous frequency, the turn-on of the switches will be synchronized with the zero-crossing of the resonant tank's voltage. This frequency is the same as the resonant frequency of the parallel resonant tank in Figure 1-3, driven with sinusoidal excitation. For non-sinusoidal excitations, the synchronous frequency is close to but different than the resonant frequency. The load coil changes its equivalent parameters during start-up operation, due to variance in operating temperature or external conditions [10], [11]. While the load resistance changes in the wide range (this work considers change of five times: Q = 10-50), the load coil's inductance changes by only a few percent. Synchronous frequency will also change by several percent. For operation at the constant switching frequency, the cross-conduction of the switches happens when the switching and synchronous frequency are not equal. One of the switches and a diode in the other switch provide a low impedance in parallel with the non-zero resonant capacitor voltage. A large current spike occurs, and it can damage transistors [12] or at best significantly degrade efficiency. Thus, in absence of the series diodes in the switch configuration, additional circuitry is required to synchronize the amplifier's operation at constant switching frequency.

1.1.5. Comparison of Basic Driving Topologies for an Inductive Load

Abovementioned positive (marked with a green plus sign) and negative (marked with a negative red sign) characteristics of the voltage-fed and current-fed resonant inverter topologies are summarized in Table 1-1. The table shows that voltage-fed topology has many advantages, and for most cases is the better choice than its current-fed counterpart. Current-fed topologies have the advantage of higher current gain, since the quality-factor reaches up to fifty. The input current scales with the output current, reducing light load losses. However, current-fed topologies possess a large number of drawbacks, associated with construction of the current source. The current-fed topologies have to be considerably improved to be more competitive with voltage-fed counterparts.

Table 1-1. Summary of characteristics for voltage-fed resonant LCL inverter and two current-fed resonant inverter topologies shown in Figure 1-1, Figure 1-2 (Current-fed 1I), and Figure 1-3 (Current-fed 2I).

Voltage-fed LCL	Current-fed 1I	Current-fed 2I
(+) Typically high efficiency and power density	(+) No cross-conduction	(+) Ground referenced switches
(+) Safe operation at no-load condition	(+) Safe operation at no-load condition	(+) Safe operation at no-load condition
(+) Boosts current L_1/L_r times	(+) Boosts current Q times	(+) Boosts current Q times
(+) Many options for control	(+) Simple tank structure	(+) Simple tank structure
(+) Multi-phase/interleaved design to scale up power	(+) Output is clean sine-wave	(+) Output is clean sine-wave
(+) Multi-phase/interleaved design for constant frequency operation	(-) Low efficiency due to series diodes	(-) Cross-conduction between switches for non-synchronous operation
(-) Cross-conduction of switches	(-) Low power density and bandwidth due to input inductor size	(-) Low power density and bandwidth due to input inductor size
(-) Design of dc link	(-) Limited control options	(-) Limited control options
	(-) Efficiency reduction due to pre-regulator	(-) Efficiency reduction due to pre-regulator
	(-) Fixed frequency operation requires additional hardware compensation	(-) Fixed frequency operation requires additional hardware compensation

1.2. Motivation

This dissertation considers implementation a high-frequency (~500 kHz) resonant driver, with a large bandwidth (~80 kHz), and a highly inductive load with the quality factor larger than ten. Constant frequency operation and spectral clarity of the output current are required to reduce electromagnetic interference. The current-fed parallel resonant inverter with two input inductors has the desired characteristics of current gain and ground referenced switches. However, limitations in bandwidth, low efficiency, and changing synchronous frequency have to be solved for successful application of the topology. Also, in further text, current-fed parallel resonant inverter will be replaced by "*boost amplifier*" term since it is easier to use and the topology resembles of a boost inverter.

1.3. Literature Overview

Load variation is major issue that prevents reliable and efficient operation of the boost amplifier at constant switching frequency. A large number of methods or strategies exist, and for the purpose of a literature review they are divided into two groups. The first group, consists of source management strategies that focus on adapting the source to compensate for the changes in the resonant tank. The "source" typically consists of an input voltage source and a switching stage, but can be extended to any circuit topology that drives the resonant tank. The second group, consists of load management strategies that use a specially designed resonant tank to mitigate the effects of load variations, or have an adaptive circuit that provides the necessary compensation of the resonant tank.

1.3.1. Source Management Strategies

Source management strategies adapt to load variation by changing the load's or resonant tank's excitation. Inexpensive, most simple, and mostly used strategy is to vary the switching frequency. Implementations using phase-locked loops [13] and self-oscillating circuits [14]-[17] are implemented for the boost amplifier already. Frequency varies only a few percent as in the case of the boost amplifier, however, the goal is to make the switching frequency constant.

The PWM-based strategies provide a simple solution for constant frequency operation in voltage-fed resonant topologies. Clamped-mode control [18] adapts to the load variation by changing a phase-shift between PWM functions for each phase-leg of the voltage full-bridge. The complexity and the implementation cost of the method is low. The loss of soft switching is a common issue, especially for large variations of the input voltage. Asymmetric PWM control [19] method applies uneven positive and negative voltage pulses in time to drive the resonant tank, thereby creating an advantage in achieving ZVS. Asymmetric voltage cancellation control method [20] clamps the output voltage of the full-bridge to zero only during one half-cycle of the period. It has a wider ZVS range than the previous two methods. In Pulse-density modulation [21], the resonant system is kept turned-on for a number of cycles, and then turned-off for one cycle or more. By varying the duration of on and off cycles the power delivery to the output can be controlled. All abovementioned PWM methods are not applicable in the case of the boost amplifier. Making both switches off at the same time destroys them. Making both switches on at the same time shorts the resonant capacitor. Any asymmetry leads to shorting resonant capacitor as well.

Active compensation strategy uses a master converter to deliver most of the power, and a slave converter to compensate for a desired variable and deliver some of the power to the load [22]. Parallel processing method is applied to a current-fed resonant inverter in [23], where a slave converter is used to control the output voltage level. Increased hardware complexity for compensation circuit and inability to control the output from zero to the specified maximum are main issues.

Multi-phase or interleaving strategy [5], [6], [24] is a very powerful method to compensate for a desired variable. Multiple phases of the base converter/inverter are put in parallel to scale up power or frequency. The total power is shared between phases. If the phases operate with the relative phase-shift between them, a variable in the system can be compensated. The properties of the multi-phase/interleaving strategy is exactly what the boost amplifier requires. Distributing power between phases improves efficiency, while the phase-shift can possibly bring compensation of the synchronous frequency. It is unknown how the multi-phase would look like for the case of the boost amplifier. Table 1-2 summarizes the source management strategies.

Table 1-2. Summary on source management strategies.

Strategies	Benefits	Limitations
Frequency change [13]-[17]	Inexpensive & simple; keeps ZVS/ZCS	Wide variation of switching frequency; EMI/EMC; passive components oversized
PWM based [18]-[21]	Inexpensive & simple; ZVS/ZCS	Loss of ZVS/ZCS; duty cycle loss
Active compensation [22], [23]	Compensation of desired variable	Increase hardware, cost & control complexity; Insufficient
Multiphase/ interleaved [5], [6], [24]	Compensation of desired variable; Shares power	Increase hardware & control complexity

1.3.2. Load Management Strategies

In load management strategies, the source (either voltage or current) is kept unchanged. The compensation for the load variations is done on the side of the resonant tank. The most commonly used method is to design a resonant tank for soft-switching of the power circuit's transistors. A boost amplifier can be designed for ZCS if an inductance is placed in series with the resonant tank [25]-[28]. The switches operate with a slight overlap between gating signals. The series inductance resonate with the resonant capacitor to help commutate the current of the resonant tank. The switches turn-off with ZCS. Although the strategy helps to ensure soft-switching for a wide variation of the load, the method only alleviates the problem. The power factor at the output of the switching stage will be poor at the light load, with a large reactive current flowing though the switches. The light load efficiency would be then reduced. Often to mitigate the reactive current, the operating frequency has to be changed too. The commutation process lasts for a significant amount of the switching cycle, and during that time power is not transferred to the load. The input current has to be increased to compensate for the time not used in power delivery. Finally, for high-voltage applications the series inductance "rings" with the output capacitance of transistor. The ringing oscillations can be severe and require attenuation using damping resistor [29].

Reconfigurable matching circuit uses an array of individual inductors, capacitors, and switches/circuit breakers that can tune/detune resonant converters [30], [31], [32], [33]. Converter operation is tuned for discrete frequency points. For a good resolution, or a wide compensation range, a large number of components are required. The cost and complexity rises quickly. The approach is unfavorable for the boost amplifier implementation.

Reactive energy compensation with a tunable impedance is an effective strategy to compensate for load variations. A variable inductor using core saturation is already implemented for a current-fed push-pull resonant inverter, and other resonant topologies [34]-[37]. However, losses, control complexity, and reduced bandwidth limit the use [38]. Phase-controlled reactance [39]-[44] produces a large compensation range. An inductor or capacitor is paired with a bidirectional voltage-blocking switch to implement the controlled reactance. A capacitor/switch combination is preferable since the switch operates at ZVS. Phase-controlled reactance produces a rich harmonic content because its switching frequency is the same as the main power converter, and additional reactive components are required to filter out unwanted harmonic. More importantly, employment of phase-controlled reactance can take care of only a load variation issue. A separate circuit is required for amplitude control of the boost amplifier, thus the hardware complexity increases with implementation of a phase-controlled reactance.

Resistance compression networks suppress variations of the load resistance. The method is presented in [45], [46] for dc/dc converters. The extension to dc/ac applications is shown in [47], where a phase-controlled reactance is used. Although the method is effective, it increases the hardware complexity as well. The summary on load management strategies is given in Table 1-3.

Table 1-3. Summary on load management strategies.

Strategies	**Benefits**	**Limitations**
Design for ZVS/ZCS [25]-[29]	Improves efficiency	Only alleviates the problem, often in connection with frequency change
Reconfigurable matching circuit [30]-[33]	Impedance scaling; improves power transfer;	Complicated & costly, matching at discrete points only
Reactive energy compensation w/ tunable impedance [34]-[44]	Continuous tuning; improves power transfer	Increase hardware complexity, lossy
Resistance compression networks [45]-[47]	Reduces load variations	Increase hardware & control complexity, lossy

1.4. Objectives and Challenges

The objectives and challenges of this dissertation are summarized in the following points:

1. Dynamic Performance: The large input inductance of the inverter limits the bandwidth of the system. Reducing the inductance leads to improved bandwidth, however, the ripple of the current in input current is significant. The tank current is not a pure square-wave anymore. A strong fundamental frequency current is circulating through input inductors and the resonant tank, changing the resonance point. Current-fed parallel resonant inverter with a current splitting transformer [48] is a common means to solve this problem, as the splitting transformer attenuates the fundamental frequency current. The topology is presented in Figure 1-4. This approach, although effective, was not pursued. The fundamental frequency current has the impact on the synchronous operation, and should be used to keep the inverter in synchronization for the parametric variations of the load. The challenge is to find a mathematical relationship between the input inductor harmonic currents and the synchronous conditions. For this purpose, frequency decomposition and balancing method is used.
2. Size Reduction: Current-fed resonant inverters suffer from large input inductors required to mitigate the ripple of the input current. Reduction of the inductance for the enhanced bandwidth would lead to the reduced size of the inductor as well. Thus, by following the original goal the reduced inductor size will come as a "free" reward.

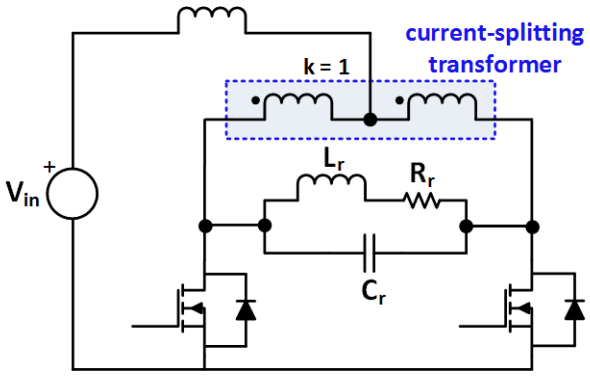
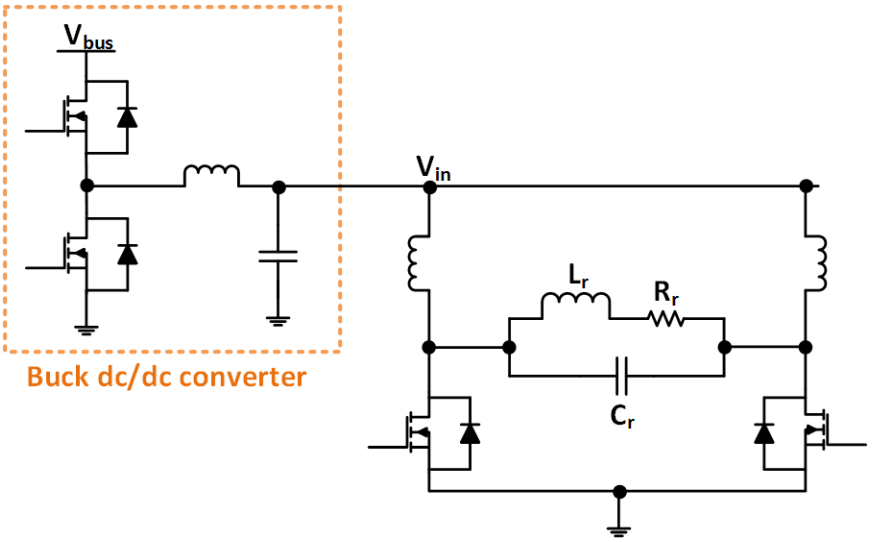
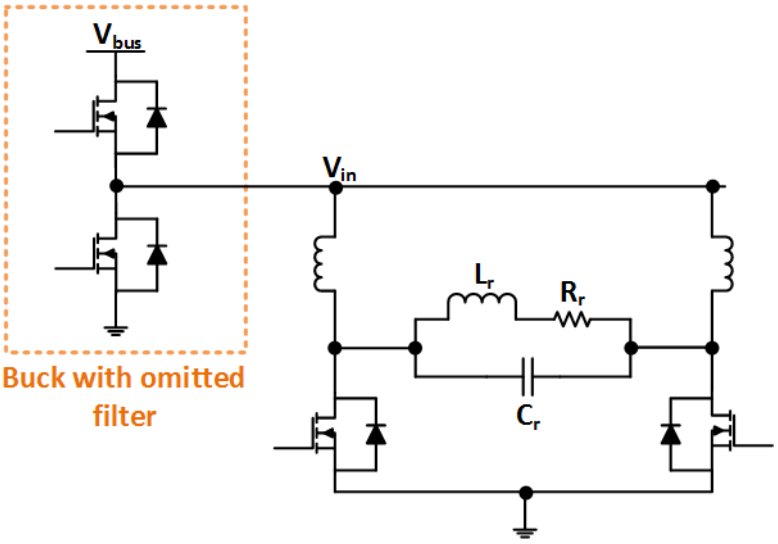


Figure 1-4. Current-fed parallel resonant inverter with current-splitting transformer [48]. Coupling coefficient of the transformer is labeled with k. Coupling is normally set to one.

3. Loss Reduction: If the inverter switches operate under the synchronous condition, no switching loss would be applied to them. Thus, reducing conduction losses is a key to high efficiency, and the series diodes with transistors have to be taken out from the inverter circuit. The challenge is how to improve the reliability of the inverter when the synchronization fails, but without putting diodes back in the circuit.
4. Control of Output Amplitude: The amplitude of the output voltage/current is typically controlled by the input voltage to the inverter. The buck dc/dc converter in Figure 1-5 a) can be used, but more often the output filter of the buck is omitted since the inverter behaves as the equivalent buck filter. The topology is shown in Figure 1-5 b). Both buck topologies are employing hard-switching, and therefore experience large switching loss. Since high efficiency is an important goal, the ZVS topology with reduced hardware complexity is to be found.
5. Synthesis of Output Waveform Containing an Envelope: Power amplifier for an antenna is required to produce the output waveform that contains an envelope in which data is coded. The envelope is synthesized using the amplitude control converter. The bandwidth of the inverter has to be high enough to pass the enveloped signal to the output.
6. Constant Frequency Operation: There are several solutions to maintain operating frequency constant, as discussed in the literature overview. However, the additional hardware complexity and cost is associated with implementation of a solution. If a buck is required for amplitude control, and an additional hardware is needed for compensation, the resultant system would be too complicated and costly. The desired solution is produced if the amplitude control and constant frequency control circuit can be embedded in one electrical circuit. Such functionality is often seen in multi-phase/interleaved converters, so a multi-phased solution will be pursued to solve the load variation issue.
7. Integration of Circuit Parasitic Elements: The integration of the circuit parasitic elements simplifies the complexity, operation, and cost of power electronics systems, and the opportunity will be search to integrate as many parasitic elements as possible into inverter operation.



(a)



(b)

Figure 1-5. Boost amplifier with a dc/dc converter for control of the output amplitude: (a) buck dc/dc converter drives the amplifier; (b) output filter in the buck can be omitted, since inverter itself behaves as a buck filter.

1.5. Organization of the Dissertation

The dissertation has five chapters. The analysis of the boost amplifier under reduced input inductance is carried out in Chapter 2. Synchronous conditions are found as a function of the circuit parameters and the harmonic currents in the input inductors. A current snubber structure is proposed to replace series diodes in switch configuration. The snubber integrates parasitic inductance of a cable that connects load with the switching stage. The bandwidth is extended to 80 kHz for the reduction of the input inductance by an order of magnitude. The hardware prototype is built to validate the theory. A 98.5 % efficient boost amplifier is tested for output reactive power of 14 kVA and active power of 1.25 kW.

Chapter 3 uses Generalized State-Space Averaging (GSSA) to create a large signal model of the boost amplifier. The model is validated in simulation and hardware, and it is used in the synthesis of signals with an envelope. Hann-function, and trapezoidal-function examples are given. In Chapter 4, a two-phase buck with ZVS capability is proposed to drive the boost amplifier. The resultant topology is termed as buck-boost amplifier. The switching function of the buck is phase-shifted to the switching function of the boost. The power transfer is controlled with the duty-cycle of the buck, and the synchronous operation of the boost is controlled by adjusting the relative phase-shift between switching functions of the buck and the boost. The mathematical control laws are derived from the GSSA model which was developed in the previous chapter. The theory is validated with a prototype operated at 480 kHz, reactive power up to 11.3 kVA, active power of 0.7 kW, and efficiency of around 95 %. Chapter 5 concludes the dissertation, summarizes major contributions, discusses the intellectual merit, and proposes directions for future work.

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Chapter 2. Boost Amplifier with Small Input Inductance and Operation at Synchronous Frequency

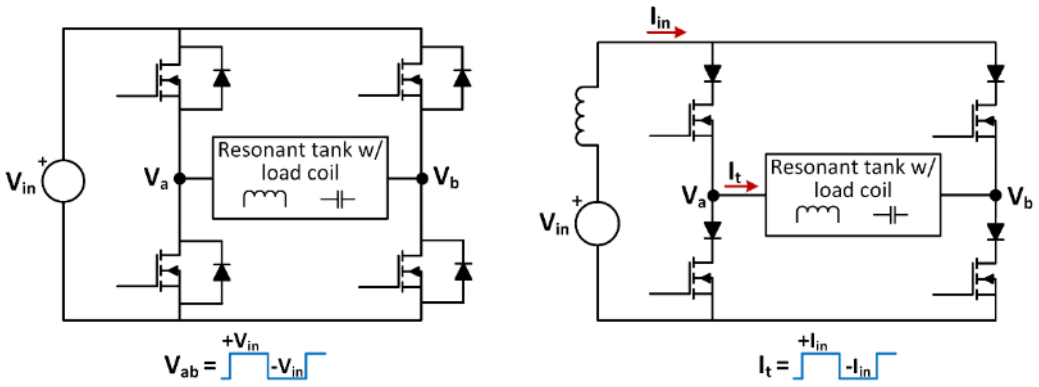
Resonant inverter is operated at the "synchronous" frequency when zero-crossings of the input voltage and current for the resonant tank are synchronized. The efficiency is maximized since no reactive power circulates through the tank and switches. The synchronous frequency defers from the resonant frequency of the tank. The resonant frequency is defined for the sinusoidal inputs and depends only on the value of consisting passive elements. However, the resonant tank is excited with the abundance of the harmonics for a typical resonant converter. Harmonics depend on many converter parameters and they impact the synchronization of the tank's input voltage and current. Thus, the inverter should be operated at the "synchronous" frequency for the optimal operation.

One drawback with current-fed resonant topologies, such is the boost amplifier, is the bulky, bandwidth-limiting input inductor(s) required to make the input current constant. A few millineries might be required at the switching frequency of 500 kHz. The design of resonant tank is simple since the resonant frequency is equal to the synchronous frequency. Reduction of the input inductance leads to significant harmonic currents in the input inductors. The harmonic currents propagate to the resonant tank and impact the synchronous frequency. The relationship between the input inductance, harmonic currents, and synchronous frequency has been unknown, preventing the reduction of the input inductance. Harmonic decomposition for the steady-state operation is used to determine the complex relationship between the three. The synchronous frequency is computed as a mathematical function of the input inductance and resonant tank elements. The boost amplifier can now be designed using the inductance reduced by an order of magnitude, and can operate at the desired frequency without detrimental current spikes and with high efficiency. A 500-kHz amplifier driving 14-kVA load at maximal efficiency of 98.5% has been tested to verify the theory.

2.1. Introduction

2.1.1. Overview of Current-fed Resonant Inverter Topologies

Resonant power conversion is a logical choice of driving high Q-factor coils for the ability to minimize switching energy losses by implementing zero-voltage or zero-current switching (ZVS or ZCS, respectively) [1]. Voltage-fed (VF) inverter consists of a resonant tank driven by a switching stage – input voltage source feeding a half-bridge (2 switches) [50] or full-bridge (4 switches) configuration (Figure 1-1 a)). The switching stage inverts the input voltage and creates a square-wave voltage waveform at the input of the resonant tank, as indicated by Figure 1-1 a). Current-fed (CF) inverter consists of the switching stage feeding the output resonant tank as well. The switching stage consists of the input voltage source, large input inductor, and full-bridge configuration of the switches, as shown in Figure 1-1 b), [52]-[56]. The input inductor is in series with the voltage source, having the inductance significantly large to make the input current constant. The diodes in series with transistors are necessary to prevent high circulating current from the resonant tank. The switching bridge inverts the input current and creates an equivalent square-wave current source. VF inverter is typically more efficient (for the lack of series diodes) and achieve higher power density (for the lack of large input inductor) than the current-fed one [56].



(a) **(b)**

Figure 2-1. (a) Voltage-fed inverter driving a resonant tank comprising load coil. Voltage V_{ab} is the output voltage of the switching stage, having a square-wave waveform. (b) Current-fed inverter driving a resonant tank comprising load coil. Current I_t is the output current of the switching stage, having a square-wave waveform. Drawbacks: large input inductor and diode in series with switch.

The current-fed (CF) based topologies are attractive alternative (to voltage-fed topologies) for their natural characteristic to boost (amplify) small input current and deliver it to the load [57]. The CF topologies with ground referenced switches are preferred when the load coil current, power, and the frequency are high. Such topology is boost amplifier/inverter, having two equal input inductors instead of top switches (Figure 2-2 a) [58]-[61]. The series diodes can be eliminated (Figure 2-2 b)) if the reactive energy that may circulate through the switching stage and resonant tank does not degrade significantly the operation of the inverter [62]-[67]. Figure 2-3 a) shows a variation of topology in Figure 2-2 b), where a single input inductor and a current-splitting transformer is used [68]-[74]. The current-splitting transformer mitigates the circulation of the fundamental frequency current through the input inductors and resonant tank. The tank's input current resembles more a square-wave shape, even for very low input inductance. Resonant inverter operation is similar to one in Figure 1-1 b), and it is typically designed to operate at resonant frequency of the tank. The inductor in series with voltage source can be integrated with the transformer when transformer windings are loosely coupled, benefiting the power density [75], [76]. Further, splitting transformer can be integrated with the load coils, which is attractive approach for induction cooking/heating application [77], [78]. Classic current-fed push-pull is used when an isolation is required between input and the output [79]-[89]. Topologies with or without series diodes are both used. This work is concentrated on analysis and optimization of the boost amplifier topology Figure 2-2 b), for its simple structure and opportunity to harness the ac currents in the input inductors. The boost amplifier topology is also known as Current- fed parallel resonant inverter [64],

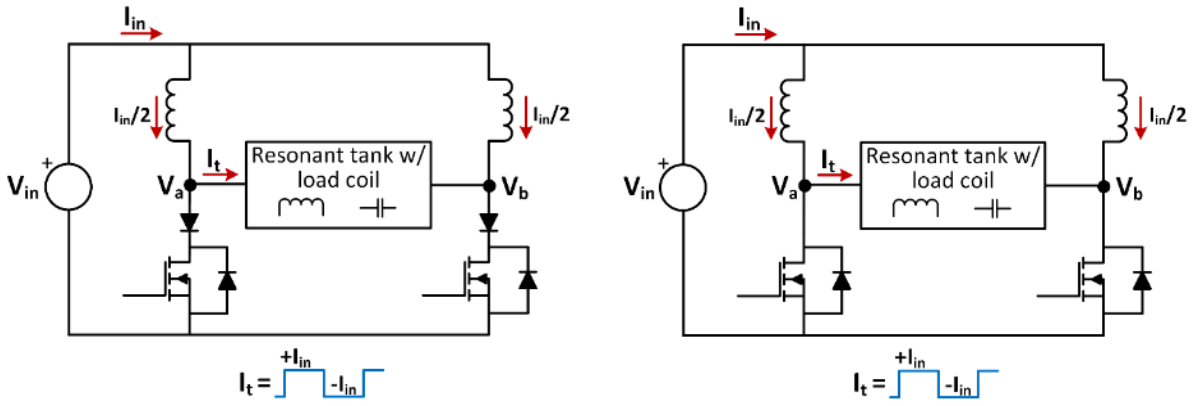


Figure 2-2. (a) Boost amplifier having the series diode with the switch. (b) Boost amplifier having no series diode with the switch. Both configurations produce the square-wave current in the resonant tank.

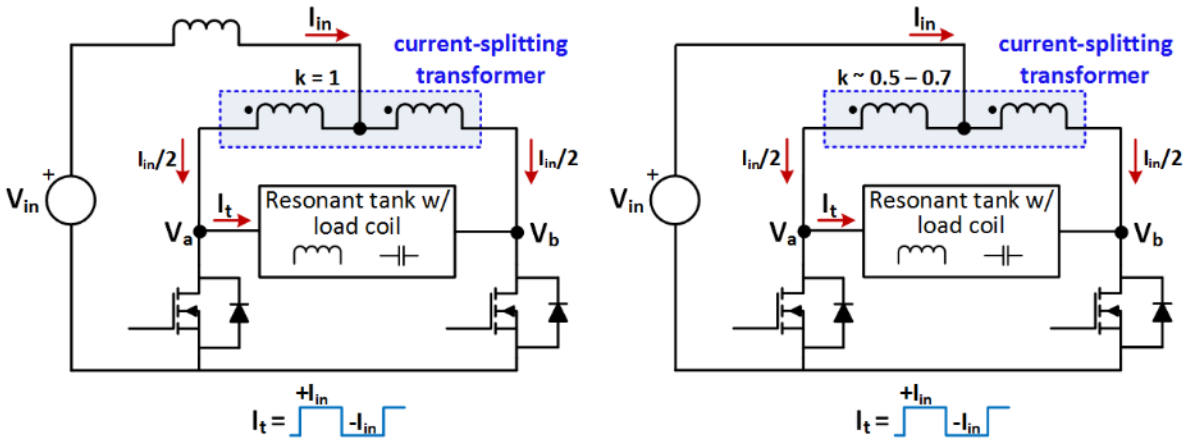


Figure 2-3. (a) Boost amplifier having a single input inductor and a current-splitting transformer with completely coupled windings. (b) Boost amplifier having a loosely coupled current-splitting transformer. The input inductor is integrated into the current-splitting transformer.

Current-fed parallel resonant push-pull inverter [59], Two current-source inverter [65], or Current-fed half-bridge [90] resonant converter.

Another benefit of the boost amplifier topology is a simple structure of the resonant tank. Except of the load coil, one compensating, parallel capacitor is sufficient to form functional resonant tank (Figure 2-4). The capacitor provides for the large current in the load coil. Small current flows from the switching stage into the resonant tank to compensate for the active power spent in the load. Additionally, parallel resonant tank has strong filtering capability at the resonant frequency of the tank [91], and therefore the load's current and voltage can be considered sinusoidal.

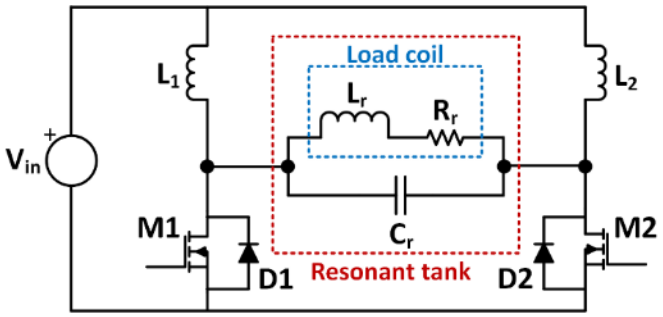


Figure 2-4. Investigated topology of the boost amplifier with a simple parallel resonant tank comprising of the load coil and the compensating capacitor. Load coil comprises of the load inductance L_r and load resistance R_r which substitutes for all losses in the coil. The input inductors are equal in value.

2.1.2. Definitions of Important Frequencies for a Current-fed Parallel Resonant Tank

The resonant tank is fed by an equivalent current source. The natural and resonant frequency can be defined for the sinusoidal excitation (Figure 2-5 a)). The undamped natural frequency, or just natural frequency (f_n) is defined as

$$f_n = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r}} \tag{2-1}$$

and this is the resonant frequency of the tank when no loading (damping) is present. The input impedance of the tank (z_t) at the natural frequency is

$$z_t(j\omega_n) = \frac{L_r / C_r}{R_r} + \frac{1}{j\omega_n C_r} \tag{2-2}$$

where $\omega_n = 2\pi f_n$. The existence of the imaginary part will force the input voltage and current of the tank to be out of synchronization. The synchronization is reached when the tank is excited at the resonant frequency f_r,

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r} - \left(\frac{R_r}{L_r}\right)^2} \tag{2-3}$$

The input impedance is purely resistive,

$$z_t(j\omega_r) = R_t = R_r(1+Q^2) \tag{2-4}$$

with $\omega_r = 2\pi f_r$ and Q being the Q-factor of the inductive load,

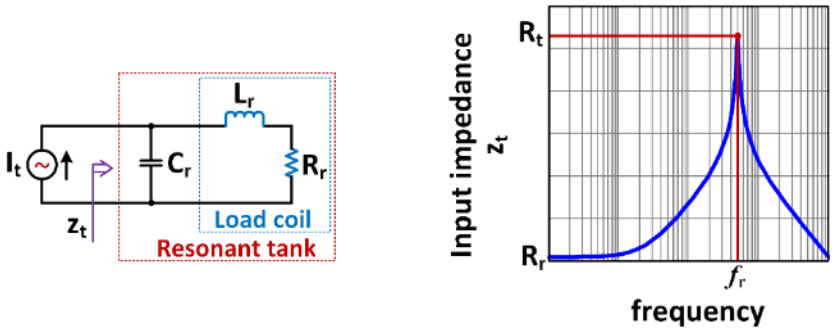
$$Q = 2\pi f_r \cdot L_r / R_r \tag{2-5}$$

The Q-factor in this work is assumed be high, $Q > 10$. The load coil resistance R_r is scaled up to R_t, as shown in Figure 2-5 b). Thus, if the active power of the source is the same as the load power, then the small input current will cause large output current. The ratio between the amplitudes of the load current I_{rm} and the tank's input current I_{tm} is:

$$\frac{I_{rm}}{I_{tm}} = Q \tag{2-6}$$

In addition, the input current is equal to zero when no loading is present ($R_r = 0\ \Omega$). This property of the resonant tank is important safety feature for the boost amplifier.

The meaning of the resonant frequency is lost when the source excitation is not sinusoidal. In general case the tank's input voltage and current are not synchronized at the resonant frequency. Good example is [71], where the parallel resonant tank driven by ideal square-wave current source is analyzed (Figure 2-6). Reference [71] determines that the synchronization of the tank's input voltage and current depends on the quality factor of the load. If the loaded quality factor is smaller than ten the synchronization will not occur. The synchronization frequency is determined by numerical means and it is termed "ZVS frequency". Other authors, [79], and [81], term it simply as the resonant frequency of the system (converter). The first name is problematic since there is infinite number of ZVS frequencies for a resonant converter. The latter name is confusing since "the resonance" can be dependent on circuit parameters as amplitude, duty-cycle, or phase-shift between gating signals. This is in contrary to the conventional definition of the resonant frequency of the passive resonant tank that depends only on the values of its elements, as indicated by (2-3). Thus, *the synchronous frequency* with the associated label f_{sy} will be used in this work. In the following section, it will be derived for the boost amplifier in Figure 2-4.



(a) **(b)**

Figure 2-5. (a) Sinusoidal current source (I_t) feeding parallel resonant tank; (b) Magnitude of the input impedance z_t of the resonant tank. The R_t follows (2-4).

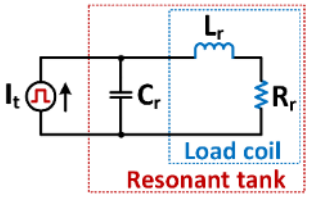


Figure 2-6. Square-wave current source (I_t) feeding parallel resonant tank. Tank's input voltage and current are not synchronized at the resonant frequency for low value of loaded Q-factor.

2.1.3. Input Inductance Problem and Prior Work

When loaded quality factor is sufficiently high as it is in this work, the synchronous frequency equals the resonant frequency of the tank as long as the tank's input current I_t is clean square-wave [71]. A square-wave current source I_t in Figure 2-6 can be created from the switching stage of the boost amplifier in Figure 2-4 when inductances L_1 and L_2 are equal ($L_1 = L_2 = L_{in}$) and sufficiently large to make I_{L1} and I_{L2} constant. Prior work, [59]-[61], [63]-[67], follows this approach for the simplicity of system design and operation. As result, input inductors are large and bulky, and dynamic response of the system is low. Reduction of the input inductance is not straightforward since it is in mathematical relationship with the synchronous frequency, as it is indicated in the work on push-pull topology [79]. Additionally, if the system is not operated at the synchronous frequency the switches may fail due to current spikes since the two switches may short the resonant tank [72].

2.1.4. Methodology and Chapter Organization

Section two explains in detail the operation of the boost amplifier at the steady-state. The penalties for operation at off-synchronous frequencies are outlined with the help of LT-spice circuit simulator. It will be shown that spurious current spikes occur which induce loss and degrade the reliability of the MOSFET's gate driver circuit. The impact of boost inductance L_{in} on synchronous frequency of the inverter is investigated in section three, by using harmonic decomposition of the currents in the input inductors. Harmonic balance principle is applied to the computation of the load coil's voltage to find the impact of the harmonic currents. Section four examines amplifier's performance at synchronous frequency for a range of input inductances, and finds trade-offs between input inductor size, amplifier's bandwidth and efficiency. Section five describes the implementation of a snubber circuit, the safety feature that prevents excessive current spikes in the case of faults. Section six describes amplifier's design and implementation for the boost inductance reduced by an order of magnitude. A demonstration circuit is built for the power level of 14 kVA in the output coil, nominal real power of 0.7 kW, and operating frequency of around 500 kHz. The hardware tests are given in section seven. Section eight concludes the chapter.

2.2. Operation of the Boost Amplifier

2.2.1. Operation of the Idealized Boost Amplifier at the Resonant Frequency

The theoretical operation of the boost amplifier in Figure 2-4 is easily explained with the help of a simplified and idealized topology in Figure 2-7. The current in the input inductors is assumed to be dc for their large inductance, and

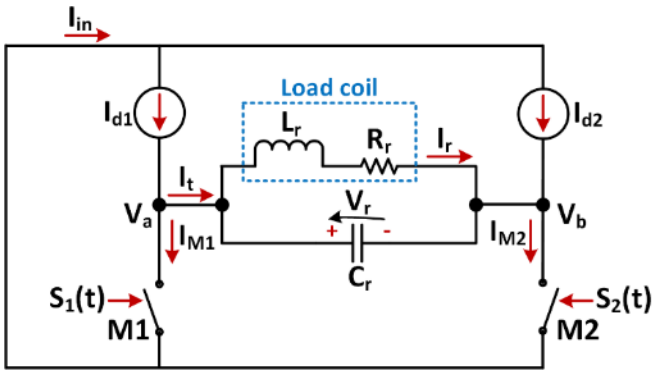


Figure 2-7. Idealized boost amplifier. It is the simplification of amplifier in Figure 2-4 containing dc current sources and ideal switches instead of input inductors and MOSFETs.

therefore is replaced with ideal dc current sources in the idealized topology in Figure 2-7. Since the both circuits are designed to be symmetrical, the current sources have the same magnitude and are equal to the half of the input current I_{in}:

$$I_{L1} = I_{L2} = \frac{I_{in}}{2} \tag{2-7}$$

Ideal switches are used instead of MOSFETs to avoid the complications with non-linear output capacitance and the gate driver circuit. The diodes are eliminated since at the resonant frequency they do not conduct current. Simple switching functions $S_1(t)$ and $S_2(t)$ are used to turn the switches on and off. The ideal switch is turned on when the switching function is equal to one. Analogously, the ideal switch is off when the switching function is equal to zero. The $S_1(t)$ and $S_2(t)$ are modulated in order to create the square-wave current waveform through the resonant tank. The period of the modulation equals to the period of the resonant frequency of the tank ($T = 1/f_{sw} = T_r = 1/f_r$). It is assumed that $S_1(t)$ and $S_2(t)$ are complementary and defined as

$$S_1(t) = \begin{cases} 0, & 0 \le t < \dfrac{T}{2} \\ 1, & \dfrac{T}{2} \le t < T \end{cases} \tag{2-8}$$

and

$$S_2(t) = 1 - S_1(t) = \begin{cases} 1, & 0 \le t < \dfrac{T}{2} \\ 0, & \dfrac{T}{2} \le t < T \end{cases} \tag{2-9}$$

Switching functions $S_1(t)$ and $S_2(t)$ are shown in Figure 2-8 together with the main voltage and current waveforms in the amplifier. The resonant tank's input current is then the square-wave with the period *T*, high-level of the half of the input current, and the low-level of the minus of the half of the input current:

$$I_t(t) = \begin{cases} +I_{in}/2, & S_1(t) = 0, \quad 0 \le t < \dfrac{T}{2} \\ -I_{in}/2, & S_1(t) = 1, \quad \dfrac{T}{2} \le t < T \end{cases} \tag{2-10}$$

The current in the switch M1 during the on-time is the summation of the currents in both current sources I_{L1} and I_{L2}, equaling to I_{in}:

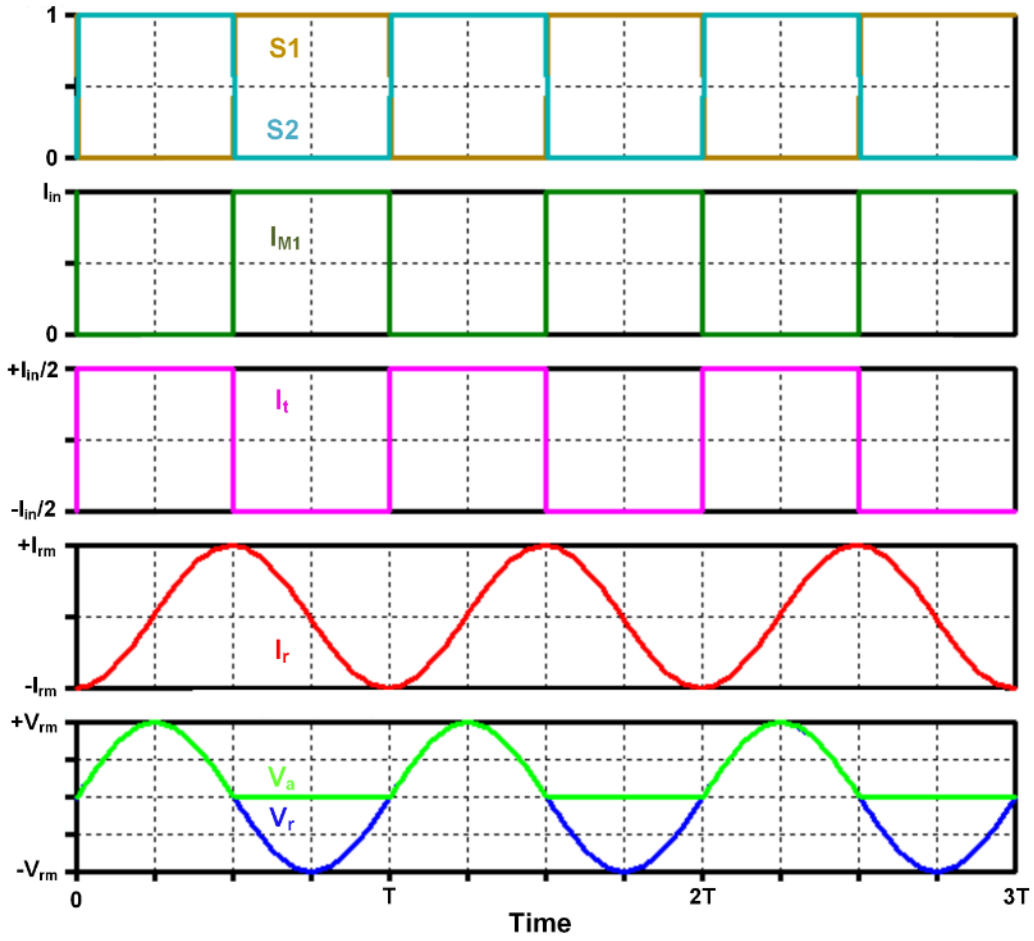


Figure 2-8. Theoretical waveforms of main voltages and currents in the boost amplifier from Figure 2-7. Synthesis of the square-wave tank current I_t is shown in magenta color.

$$I_{M1}(t)=\begin{cases}0, & S_1(t)=0, \quad 0\le t<\dfrac{T}{2}\\ I_{in}, & S_1(t)=1, \quad \dfrac{T}{2}\le t<T\end{cases} \tag{2-11}$$

Similarly, the current through the switch M2 is:

$$I_{M2}(t)=\begin{cases}I_{in}, & S_2(t)=1, \quad 0\le t<\dfrac{T}{2}\\ 0, & S_2(t)=0, \quad \dfrac{T}{2}\le t<T\end{cases} \tag{2-12}$$

The tank has strong filtering property since the quality factor of the load is high. Thus, the current I_t from (2-10) can be represented only with its first harmonic in the analysis of the resonant tank operation

$$I_t(t)\approx I_{tm}\sin(2\pi f_{sw}t) \tag{2-13}$$

where

$$I_{tm}=\frac{4}{\pi}\frac{I_{in}}{2}=\frac{2I_{in}}{\pi} \tag{2-14}$$

Resonant tank's voltage is sinusoidal as well,

$$V_r(t)=V_{rm}\sin(2\pi f_{sw}t) \tag{2-15}$$

where the amplitude V_{rm} is

$$V_{rm}=I_{tm}R_t=\frac{2I_{in}}{\pi}R_r(1+Q^2) \tag{2-16}$$

According to (2-6), the amplitude of the load coil's current is

$$I_{rm}=QI_{tm}=\frac{2QI_{in}}{\pi} \tag{2-17}$$

Voltage over switch M1 (V_a) equals to the voltage $V_r(t)$ when the switch is off. During the on-time the voltage V_a depends on the on-resistance of the switch R_{on} and the current that flows though the switch:

$$V_a(t)=\begin{cases}V_r(t), & S_1(t)=0, \quad 0\le t<\dfrac{T}{2}\\ R_{on}I_{in}, & S_1(t)=1, \quad \dfrac{T}{2}\le t<T\end{cases} \tag{2-18}$$

Similarly, the voltage of the switch M2 is defined as

$$V_b(t) = \begin{cases} R_{on} I_{in}, & S_2(t) = 1, \quad 0 \le t < \dfrac{T}{2} \\ V_r(t), & S_2(t) = 0, \quad \dfrac{T}{2} \le t < T \end{cases} \tag{2-19}$$

The relationship between main variables were derived in this section. The following section shows the computation of the circuit parameters based on a given set of specifications.

2.2.2. Computation of Circuit Parameters of an Idealized Boost Amplifier

Calculation of the amplifier's parameters is fast once initial set of specifications is established. The example is given for the switching frequency f_{sw} = 500 kHz, maximum amplitude of the resonant tank voltage V_{rm} = 800 V, nominal loaded quality-factor Q = 20, and apparent power in the load of PQ = 14 kVA. The active power in the load is simply

$$PA = \frac{PQ}{Q} = 700\,W \tag{2-20}$$

The apparent power is a function of load's voltage and current amplitude,

$$PQ = \frac{1}{2} V_{rm} I_{rm} \tag{2-21}$$

from which the load's current amplitude is calculated to be I_{rm} = 35 A. The load coil's resistance is obtained from

$$PA = \frac{1}{2} I_{rm}^2 R_r \tag{2-22}$$

The calculated value is R_r = 1.14 Ω. The load coil's inductance is calculated from (2-5) to be L_r = 7.27 μH. The resonant capacitor value is obtained from (2-3) to be C_r = 13.9 nF. Using (2-17), the input current is computed as I_{in} = 2.75 A. Current sources I_{L1} and I_{L2} are calculated from (2-7), $I_{L1} = I_{L2}$ = 1.375 A. The boost amplifier's parameters are summarized in the Table 2-1. Circuit simulation in LT spice is performed. The Appendix A contains the list of schematics for all simulated cases in this Chapter 2. The schematics are described in detail and the locations of the simulation files are given. The circuit parameters are tabulated in Table 2-1. Simulation waveforms are presented in Figure 2-9. The waveforms are the same as in the Figure 2-8 where the symbols for magnitudes are replaced by the real numbers.

Table 2-1. Summary of the parameters for the idealized boost amplifier in Figure 2-7.

f_{sw} (kHz)	PQ (kVA)	PA (W)	V_{rm} (V)	I_{rm} (A)
500	14	700	800	35
I_{in} (A)	I_{L1}/I_{L2} (A)	R_r (Ω)	L_r (μH)	C_r (nF)
2.75	1.375	1.14	7.27	13.9

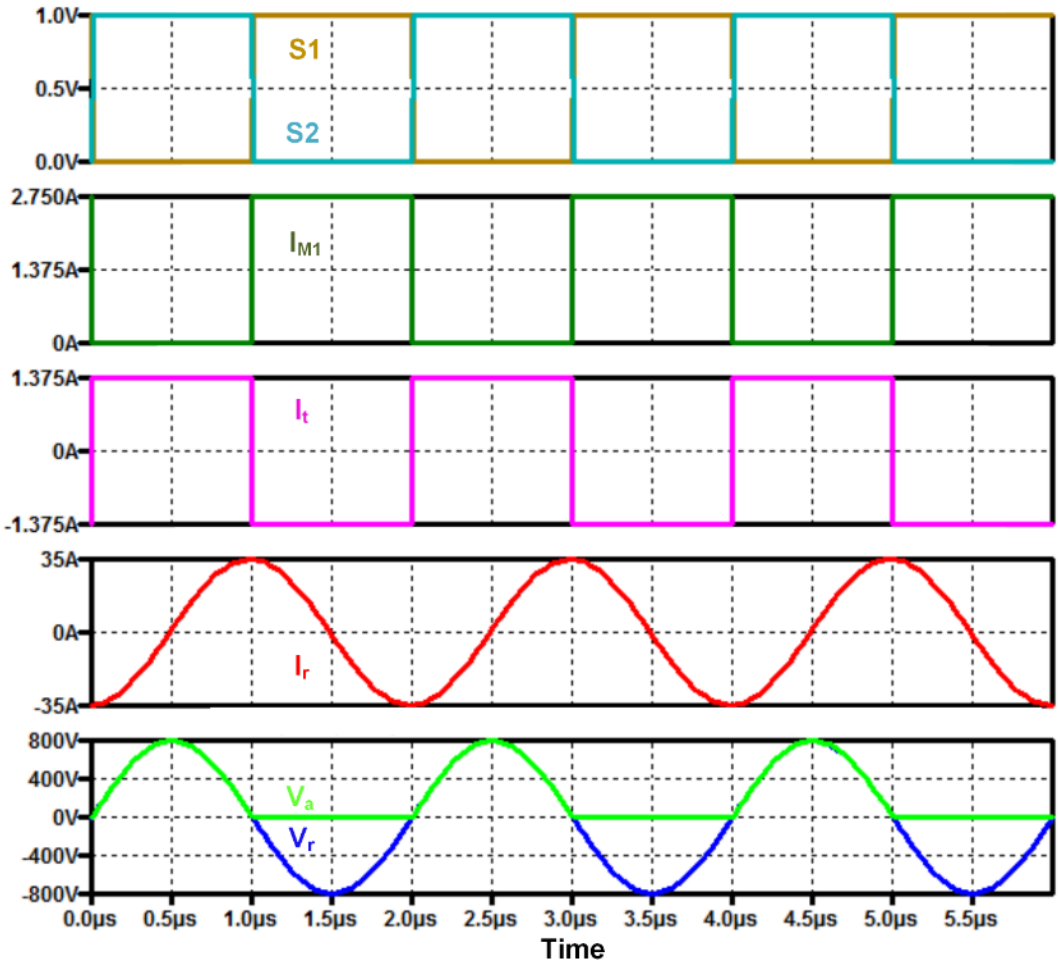


Figure 2-9. Idealized boost amplifier operation at the resonant frequency for the circuit parameters from Table 2-1. Tank is fed by square-wave current I_t (in magenta color).

2.2.3. Operation at the Resonant Frequency and with Large Input Inductance

The resonant tank has large quality-factor, making the resonant/synchronous frequency sensitive to circuit parameters such as parasitic elements in the components or printed circuit board. The idealized boost amplifier in Figure 2-7 helped to explain basic operation of the actual topology in Figure 2-4. The amplifier's circuit in Figure 2-4 with added parasitic elements is shown in Figure 2-10. The circuit in Figure 2-10 will be used to analyze the amplifier's operation. Parasitics are colored in gray. The input inductors contain parasitic parallel capacitance from the wire winding. Printed circuit board (PCB) parasitics adds too, producing total inductor parasitic capacitances C_{pL1} and C_{pL2}.

The stray inductance L_s is in series with the resonant tank. It comes from the trace parasitics or cable connection, and is a lumped value that accounts for the MOSFET package, the distance of the resonant capacitor from the switches, and ground connection between the switches. The inductive load is often placed afar from the switching stage [56] and require the resonant capacitor to be close to the load to minimize the conduction losses in the cable connection. Thus, the stray inductance from the cable connection of the resonant capacitor and the switches can be significant, and dominate total stray inductance L_s. For simplicity, it is assumed for now that the inductance L_s comes from the MOSFET package only. It will be shown later that some inductance is actually beneficial for the amplifier's reliable operation during faults or during non-synchronous operation.

The steady-state maximum voltage on the switches is $V_{max} = V_{rm} = 800$ V. The CMF20120D silicon-carbide (SiC) MOSFET transistor [92] is used for the system implementation since SiC MOSFETs offer excellent performance

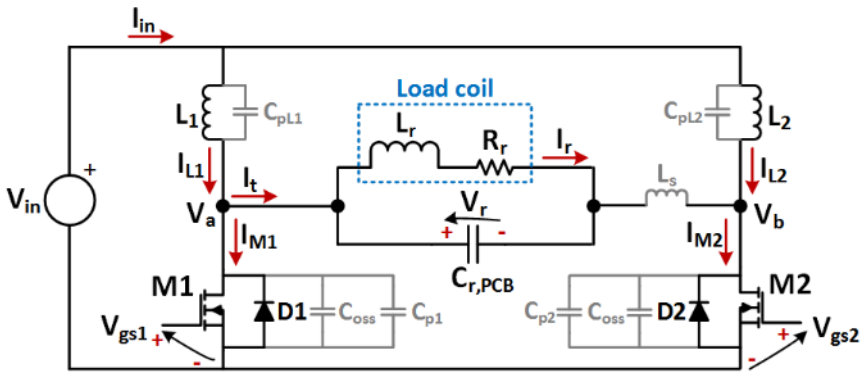


Figure 2-10. Investigated topology of the boost amplifier with the major variables labeled. Resonant capacitance C_r is a sum of MOSFET's non-linear output capacitor C_{oss} and physical on-board capacitor $C_{r,PCB}$.

for the 1200 V rated switches [93]. The parasitic inductance of the package is 7 nH according to the spice model obtained from the manufacturer, and for two MOSFETs the stray inductance is L_s = 14 nH.

MOSFET's non-linear output capacitance C_{oss} impacts the resonant frequency of the tank [94] since it forms the resonant capacitance C_r together with the physical on-board $C_{r,PCB}$ capacitor (Figure 2-10). The switch M1 is off and the M2 is on during the first half-cycle of the amplifier operation, and therefore The C_{oss} capacitor from MOSFET M1 is in the parallel configuration with the $C_{r,PCB}$ since the M2's capacitor is shorted. During the second half-cycle the M1 conducts and shorts its capacitor, while M2's C_{oss} capacitor is in the parallel configuration with the $C_{r,PCB}$ capacitor since M2 is off. Thus, at all times one C_{oss} capacitor is in parallel with the $C_{r,PCB}$ capacitor, and the two comprise the resonant capacitance C_r. The same argument can be made for parasitic capacitances of input inductors, CpL1 and CpL2, and parasitic capacitances of nodes A and B to the ground, Cp1 and Cp2. If the amplifier's circuit is symmetric, $C_{pL1} = C_{pL2} = C_{pL}$, and $C_{p1} = C_{p2} = C_p$.

The C_{oss} is non-linear capacitor whose value depends on the applied voltage, and it is often substituted with a linear capacitor $C_{oss,eq}$ for design purpose. The required capacitance of physical on-board capacitor $C_{r,PCB}$ that needs to be placed in parallel with the load coil is

$$C_{r,PCB} = C_r - C_{oss,eq} - C_{pL} - C_p \tag{2-23}$$

where C_r is the resonant capacitance from (2-3). The $C_{oss,eq}$ capacitor is computed as time-related or charge-related (energy-related) equivalent [95]. The latter one will be used in this work, and it is an equivalent linear capacitor that stores the same charge as the non-linear capacitor for the same applied voltage. The calculation of $C_{oss,eq}$ is presented in the Appendix B. Value of $C_{oss,eq}$= 195 pF is computed for the voltage of V_{rm} = 800 V. The use of (2-23) to design the resonant tank does not give the best results. The equivalent linear capacitor cannot represent truly the non-linear nature of C_{oss} [95], leading to small error in the time-domain simulation. Additionally, the resonant capacitance is computed from the formula for the resonant frequency, (2-3), which introduces additional error into derivation of the capacitor $C_{r,PCB}$. Thus, the value of $C_{r,PCB}$ needs to be tuned for best results. The $C_{r,PCB}$ = 13.74 nF is adopted for the circuit simulation in this section, while C_{pL} and C_p are assumed to be zero for simplicity. The input voltage V_{in} is computed as

$$V_{in} = \frac{V_{rm}}{\pi} \tag{2-24}$$

when (2-17), (2-20), (2-21) are combined. The value V_{in} = 254.65 V is obtained. The input inductance is conventionally computed based on the current ripple criteria. Typically 10 % or 20 % ripple is assumed. Approximate formula is used [60]

$$L_{in} = \frac{T}{2}\frac{V_{in}}{ripple \cdot I_{L1}} = \frac{QV_{in}^2}{ripple \cdot f_{sw} \cdot PQ} \tag{2-25}$$

The input inductance L_{in} = 1.9 mH is computed for *ripple* = 0.1. The remaining circuit parameters are the same as in section 2.2.2. The amplifier's parameters are summarized in the Table 2-2.

The power losses are added to the amplifier LT spice simulation. Transistor loss model is included in its spice model. Parasitic resistances are associated with the loss of inductors and capacitors, and they are assumed to be same for all simulation cases covered in this section for easy comparison. Resonant capacitor C_r is assumed to have the series parasitic resistance of 6.5 mΩ. Total inductor loss is lumped into the parallel parasitic resistance and which is assumed to be equal to 40 kΩ.

A piece-wise-modulated (PWM) voltage source at the switching frequency with +20 V/-5 V voltage levels is used to drive CMF20120 MOSFETs. The PWM waveforms are nearly square-waves with small 20 ns dead-time to account for different turn-on and turn-off times. Series 5 Ω gate resistor is placed between the square-wave source and the gate terminal of the MOSFET. Simulation is performed and corresponding waveforms are plotted in Figure 2-11. Gate-source voltages have typical curves of rising and falling exponential functions when transitioning from one voltage

Table 2-2. Summary of the parameters for the design and simulation of the boost amplifier in Figure 2-10. Large boost inductance of 1.9 mH is designed to limit the current ripple in the input inductors to 10 % only. The operation at the resonant frequency given with (2-3) is assumed.

f_{sw} (kHz)	PQ (kVA)	PA (W)	V_{rm} (V)	I_{rm} (A)	V_{in} (V)
500	14	700	800	35	254.65
R_r (Ω)	L_r (μH)	C_r (nF)	$C_{r,PCB}$ (nF)	$C_{oss,eq}$ (pF)	L_{in} (mH)
1.14	7.27	13.9	13.74	195	1.9

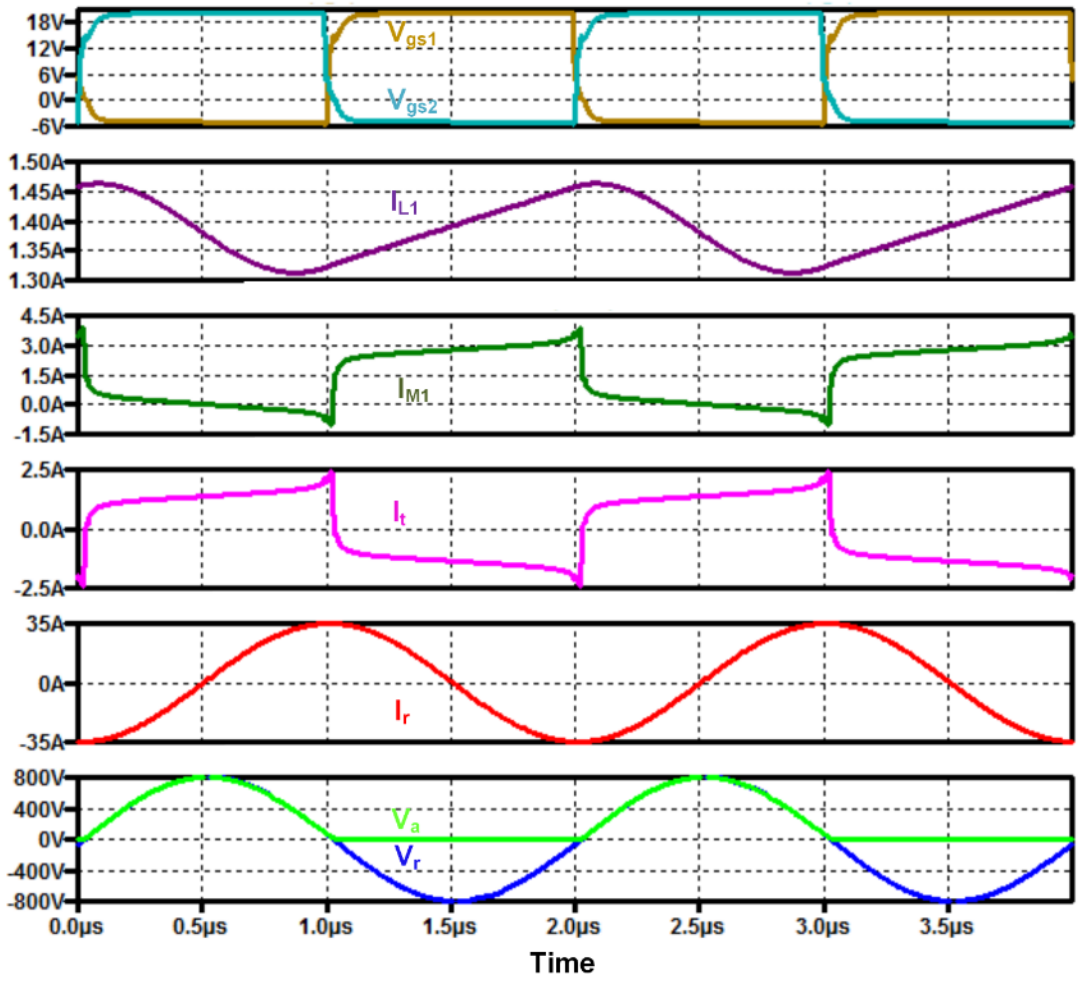


Figure 2-11. Simulation waveforms for the boost amplifier's operation at the resonant frequency and L_{in} = 1.9 mH. The waveforms correspond to the circuit from Figure 2-10 with parameters in Table 2-2.

level to another. The examined current ripple approximates the designed 10 % value. The switch and the tank currents are not square-wave anymore because C_{oss} capacitor charging/discharging current is added to the square-waves. However, resonant voltage and current are not changed when compared to results in Figure 2-9.

2.2.4. Operation below the Resonant Frequency and with Large Input Inductance

The switching frequency normally tracks the load-dependent resonant frequency (equation (2-3)) in order to maximize the efficiency. The change of the switching frequency is not desirable due to decreased spectral clarity of the output variables, increased complexity in control, electromagnetic interference (EMI), and electromagnetic compatibility (EMC) design. Thus, the boost amplifier operation will be examined for fixed switching frequency of

f_{sw} = 500 kHz and loaded quality-factor in the range $10 \leq Q \leq 50$. Nominal quality factor was set to Q = 20, and the resonant frequency is equal to the switching frequency at Q = 20. For Q >20, the switching frequency is smaller than the resonant frequency, and the input impedance of the resonant tank is inductive.

In the first half-cycle ($0 \leq t < T/2$) the switch M2 is on while the switch M1 is off. The resonant voltage V_r will fall to zero before the commutation of the switches occurs. The diode D1 will start to conduct, and short the resonant capacitor since the M2 is on. A transient current is created and it circulates through capacitor $C_{r,PCB}$, the transistor M2, and diode D1. The transient current will increase positive currents I_t and I_{M2}, and create a current spike. If the duration of the transient current is sufficiently long, the switch M2 and diode D1 would circulate the whole load coil current I_r. At the moment of switching the coil current is equal to its maximum I_{rm}. In conventional boost amplifiers for induction heaters, [78], [81], the spike is low because the loaded q-factor is low as well. However, in the boost amplifier analyzed in this work the Q-factor is high and the current spike may be detrimental. It creates significant loss that may reduce the efficiency by few percent and if excessive, it can lead to erroneous gate drive operation or even damage the gate terminal of the MOSFET because of overvoltage. The spike is naturally attenuated with the stray series inductance L_s. Larger series inductance can be designed to provide for higher attenuation. Figure 2-12 shows the amplifier's simulation waveforms for the loaded quality-factor of Q = 50. The current spike is noticeable, and is around three times larger than the value prior it. It is attenuated with parasitic inductance L_s = 14 nH and series on-state resistance of R_{on} = 80 mΩ from the model of the MOSFET. However, tolerances in circuit parameters and the gate driver timing can produce much more significant spikes. Thus, additional snubbing series inductance is will be implemented.

2.2.5. Operation above the Resonant Frequency and with Large Inductance

The boost amplifier operates above the resonant frequency when the loaded quality-factor falls below the nominal value of Q = 20. The input impedance of the tank is capacitive, and the current transition of the tank's input current starts before the resonant tank's voltage reaches zero. At the end of the first half-cycle ($0 < t < T/2$) the switch M1 is off while the switch M2 is on. Resonant tank voltage V_r is positive while the M1 turns on and M2 turns off. In absence of the parasitic trace inductances in the circuit the resonant capacitor would be shorted via transistor M1 and diode D2, leading to another detrimental current spike. However, some parasitic inductance L_s is present (Figure 2-10) and can influence the switching process in desirable way as it prevents sudden current increase in transistor M1.

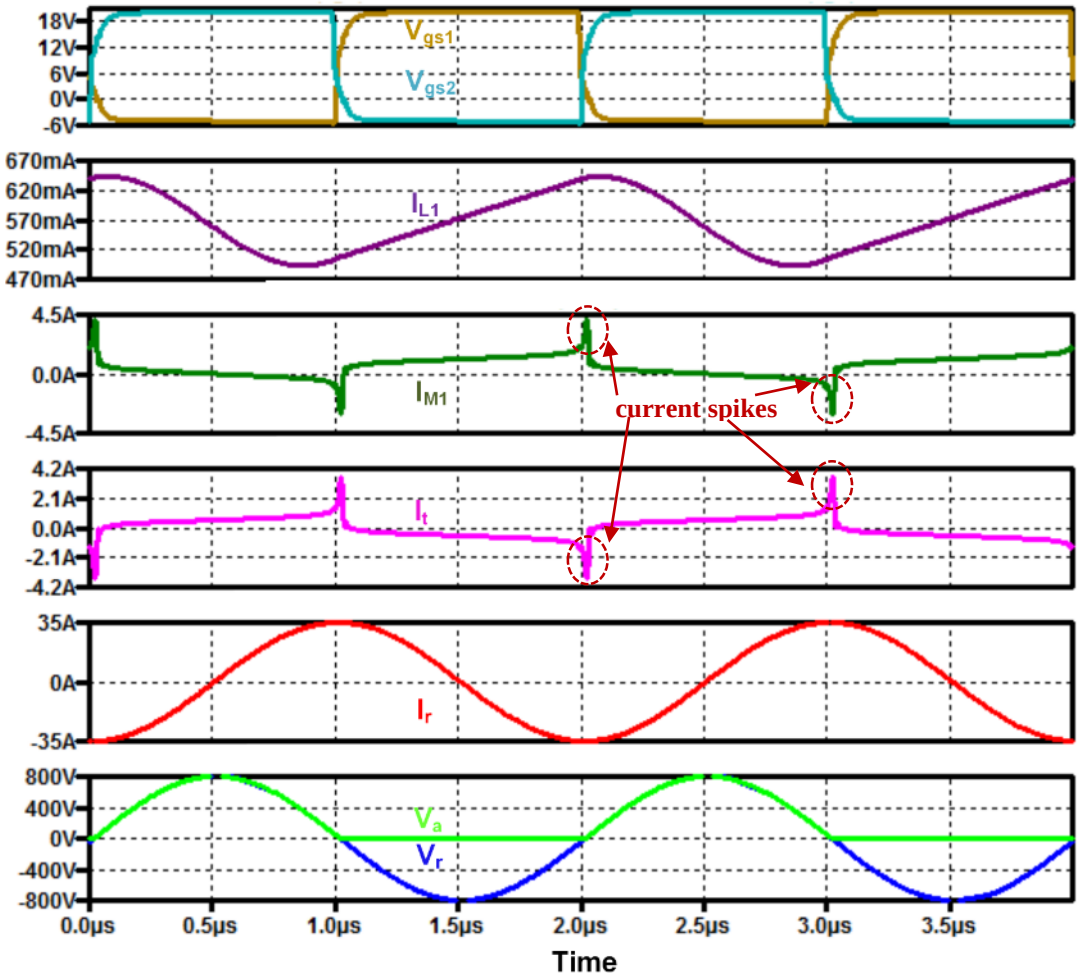


Figure 2-12. Simulation waveforms for the boost amplifier's operation below the resonant frequency and L_{in} = 1.9 mH. The loaded quality-factor is Q = 50. The current spikes are noticeable.

Additionally, L_s will resonate with capacitance C_r and the tank's input current I_t will be stirred from its positive value to its negative value in sinusoidal fashion. Thus, L_s assist the switching transition and it can be design parameter of the boost amplifier. In low input voltage applications such as the solar panels this property is significant as it leads to an efficient system (95 % reported in [67]). In high input voltage applications the MOSFET's output capacitance is significantly larger, and it rings with the L_s creating additional loss and degrading the reliability of the gate driver. Additional snubber circuit may be required to damp the oscillations. Additionally, the turn-on voltage on the transistors in not zero, and additional switching loss is created. Thus, the attractiveness of this approach is reduced for the analyzed boost amplifier.

Figure 2-13 shows the simulation waveforms of the boost amplifier operated at the resonant frequency and with the quality-factor of Q = 10. The voltage and current in the load are unchanged from the previous cases. The switching transient of the transistor's current is noticeable. The current overshoot is 100 % larger than the normal on-state current level. Similar conclusion can be drawn for the tank's input current. The gate-source voltage of the transistors rings at the end of the current transition interval. The maximum voltage on the transistor's gate exceeds twenty five volts. The minimum voltage on the gate reaches minus twelve. Both minimum and maximum voltages are dangerously excessive and can damage the transistor.

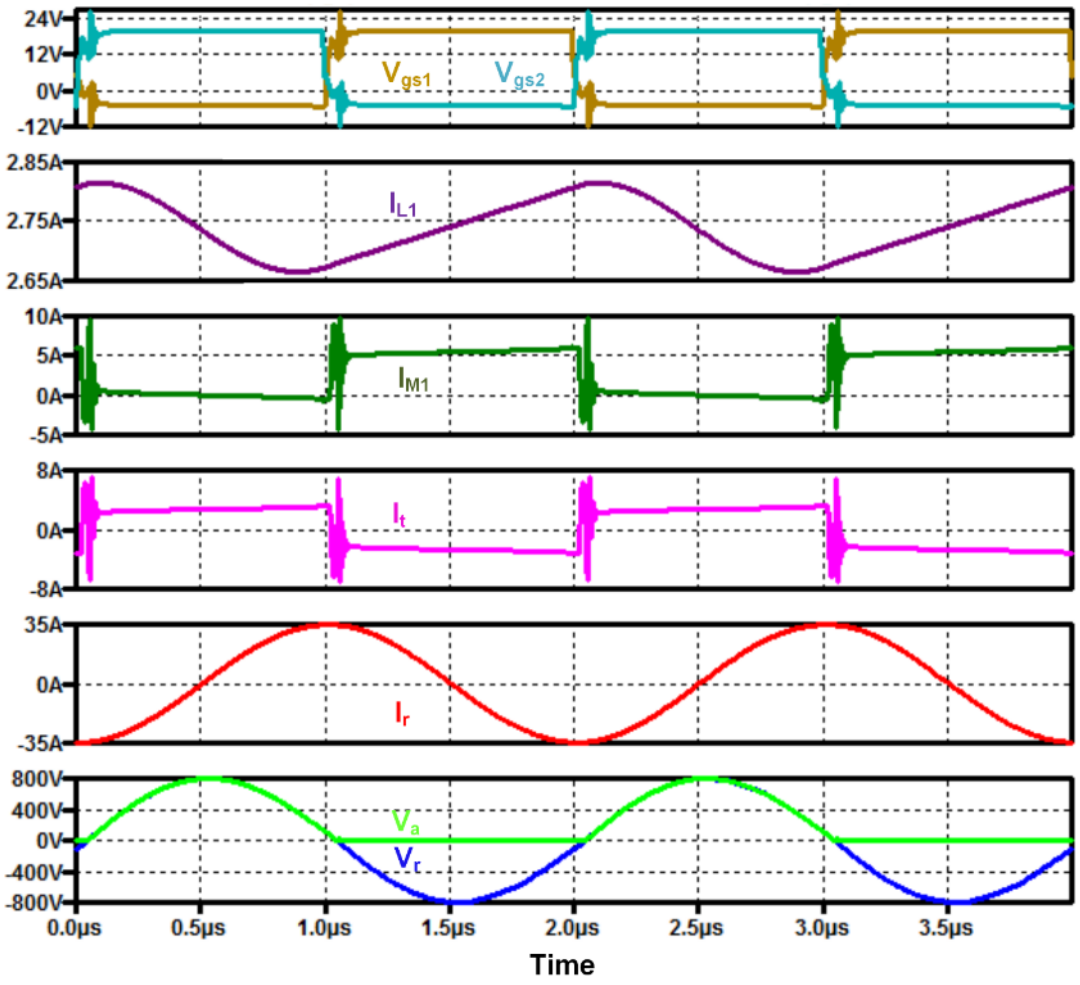


Figure 2-13. Simulation waveforms for the boost amplifier's operation above the resonant frequency and L_{in} = 1.9 mH. The Q-factor is set to Q = 10, while the switching frequency is unchanged – f_{sw} = 500 kHz.

2.2.6. Operation at the Resonant Frequency and with Reduced Input Inductance

Reduction of the input inductance is desirable to increase power density and improve dynamics of the boost amplifier. In the previous analysis, it was assumed that the inductors' current is dc value. As the inductance value is decreased, the current ripple in the inductors is higher. At some point, the ripple current cannot be neglected since the resonant frequency of the tank will not be close enough to the synchronous frequency any more.

Figure 2-14 shows the simulation example where the input inductance is reduced to L_{in} = 125 µH. The rest of the

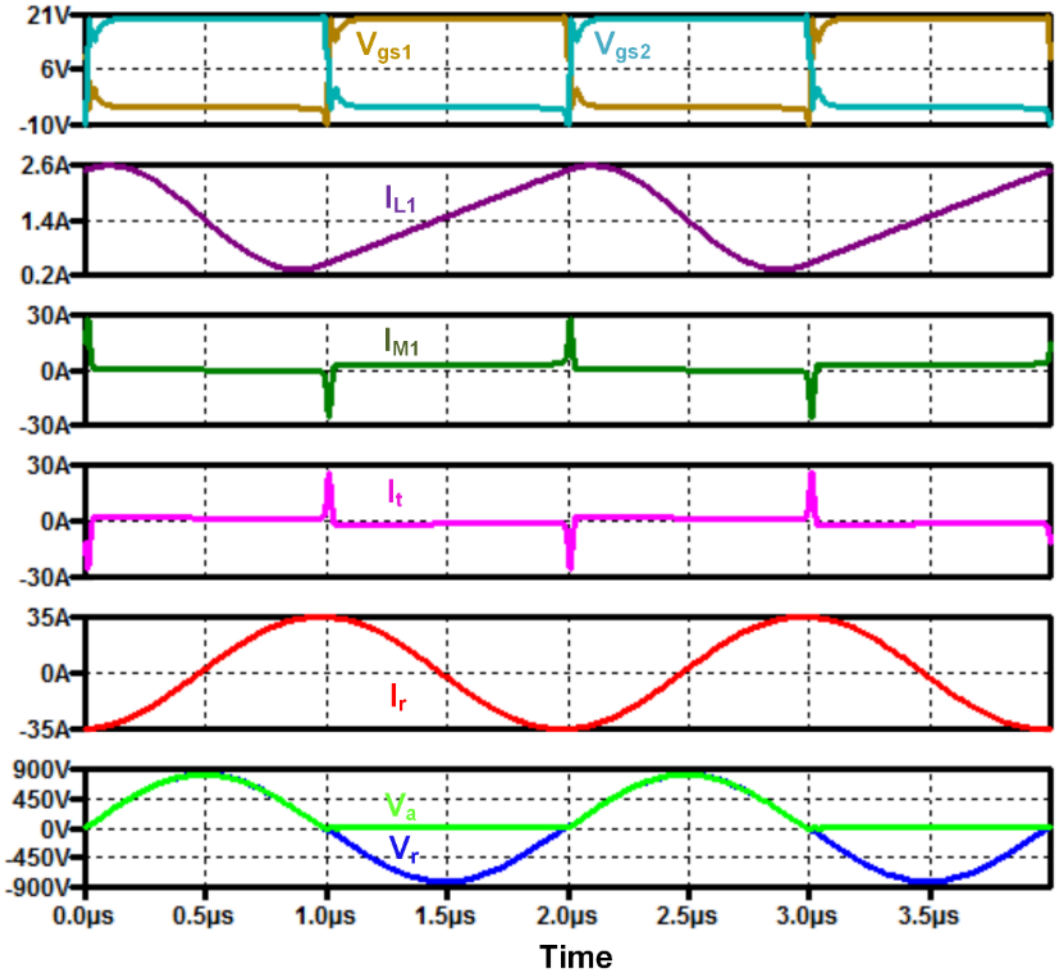


Figure 2-14. Simulation waveforms for the boost amplifier operation's at the resonant frequency of the tank and L_{in} = 125 µH. The loaded Q-factor is Q = 20, and the switching frequency is f_{sw} = 500 kHz.

amplifier is the same as in section 2.2.3., with parameters specified in Table 2-2. The current ripple is nearly two times larger than the average. Enormous current spike is flowing through the switches and the resonant tank, with the maximum value of almost thirty amps. The shape and the size of the spike indicates that the resonant frequency is well below the synchronous frequency. Additionally, the gate-source voltage reaches -10 V, which may produce the failure of the gate terminal of the transistors.

2.2.7. Operation at the Synchronous Frequency and Reduced Input Inductance

The operation at the synchronous frequency with reduced input inductance can be achieved by either changing the switching frequency or by retuning the resonant tank. The latter is chosen since the simulation examples will be compared and it is easier to do so when the switching frequency is fixed for all cases. The resonant capacitance is increased from C_r = 13.9 nF to C_r = 14.37 nF for the reduction of the input inductance from L_{in} = 1.9 mH to L_{in} = 125 μH. The LT spice simulation is performed for the parameters in Table 2-3. The simulation waveforms are shown in Figure 2-15. The amplifier works at the synchronous frequency, as seen from the examination of the tank's input current and voltages V_a and V_r.. The gating waveforms contain no overshoots or undershoots, providing safe switching pattern for transistors. The current ripple is the same as in previous case and it is around two times larger than the average value.

Switch current, or the tank's input current contain no spikes. Compared to the waveforms in Figure 2-11, the two currents do not resemble a clean, square-wave shape. Instead, they resemble a sinusoidal current imposed upon the square-wave. The RMS value of the tank's input current is almost 6 % larger than for the case in section 2.2.3. This suggests that some of the input inductor's current flows though the resonant tank and increases its RMS value while impacting the synchronous frequency.

The load coil's voltage and current waveforms correspond to ones in Figure 2-11. Thus, the load coil can experience the same driving conditions regardless of the choice for the input inductance. The only difference is how currents propagate in the rest of boost amplifier.

Table 2-3. Summarized parameters of the boost amplifier for the operation at the synchronous frequency and reduced boost inductance from L_{in} = 1.9 µH to L_{in} = 125 µH. All parameters are the same as in Table 2-2 except for resonant capacitor increases from C_r = 13.9 nF to C_r = 14.37 nF.

f_{sw} (kHz)	PQ (kVA)	PA (W)	V_{rm} (V)	I_{rm} (A)	V_{in} (V)
500	14	700	800	35	254.65
R_r (Ω)	L_r (µH)	C_r (nF)	$C_{r,PCB}$ (nF)	$C_{oss,eq}$ (pF)	L_{in} (µH)
1.14	7.27	14.37	14.19	195	125

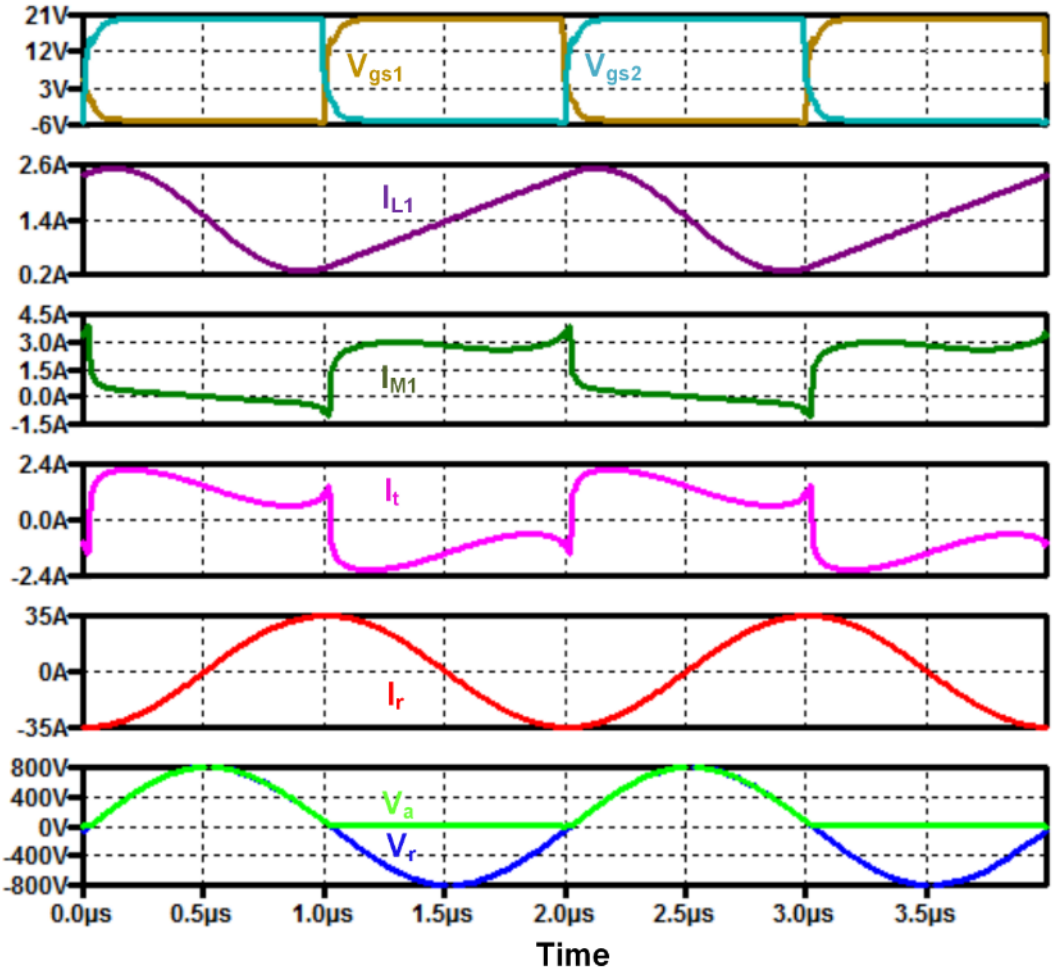


Figure 2-15. Simulation waveforms for the boost amplifier's operation at the synchronous frequency and L_{in} = 125 µH. The amplifier's circuit parameters are summarized in Table 2-3.

2.2.8. Power Loss and Efficiency Consideration

The choice of the constant switching frequency in simulation examples in previous sections is intentional since it is easier to compare the simulation cases for the transistor power loss. The transistor power loss is of particular interest since the current spikes affect transistors while the impact on other components is negligible. Also, power transistors are thermal hotspots in power electronic systems. The power loss elements (parasitic parallel resistance of the input inductors and parasitic series resistance of resonant capacitor) are also fixed for the same reason as the switching frequency, although the inductor design and its parasitic parameters vary greatly for the inductance having a difference by an order of magnitude.

The simulated boost amplifier efficiency is plotted in Figure 2-16. The blue curve represents the conventional design where the input inductance is large and the amplifier is operated at the resonant frequency of the tank. The efficiency drops few percent as the Q-factor increases since the loss in the input inductors and resonant capacitor does not change significantly with load. When the amplifier is operated at the resonant frequency with reduced input inductance the current spikes will deteriorate the efficiency due to increased transistor loss. The transistor loss in quantified in the Figure 2-17. At the light load condition (Q-factor is high), the power transistor loss is more than ten times larger for the reduced inductance case. If the amplifier is operated at the synchronous frequency and with reduced input inductance, the efficiency nor the power loss of the transistors will not change significantly from the case when the boost inductance is large.

From the previous discussion it is concluded that:

- The reduction of the input inductance will not impact the power loss of power transistors if the amplifier is operated at the synchronous frequency.
- The resonant capacitor loss is independent from the loading conditions and depends only on the current in the load coil due to the high quality-factor of the load.
- The efficiency of the amplifier depends on the implementation of the input inductors. Current simulations do not include different core and conduction losses. The known trade-off for inductor of the open-loop buck converter also applies here: larger inductance reduces core losses and improves the efficiency at the expense of the inductor size and dynamic performance [96].

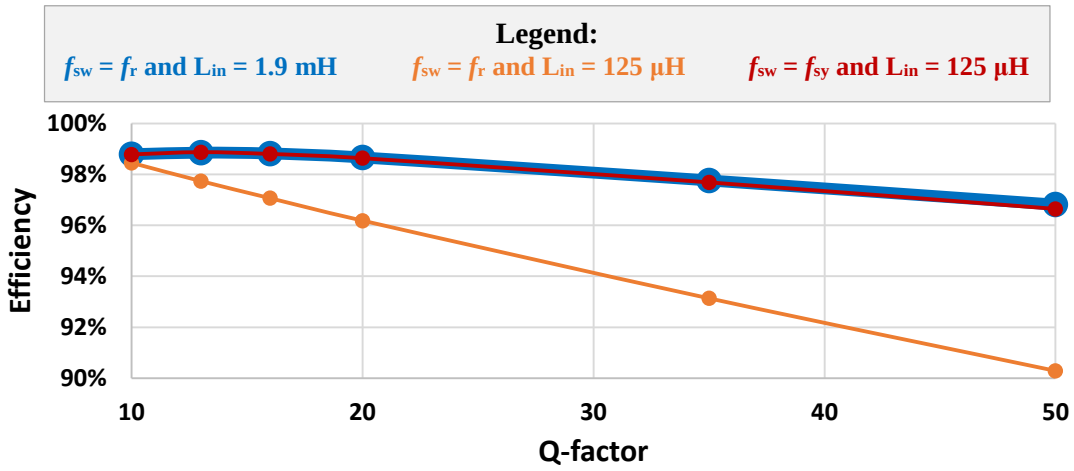


Figure 2-16. The efficiency versus the loaded quality-factor for the boost amplifier in different simulated cases. Blue curve represents the operation at resonant frequency with large input inductance that are covered in sections 2.2.3., 2.2.4., and 2.2.5. Orange curve represents the operation at the resonant frequency with small input inductance that is covered in section 2.2.6. Red curve represents the operation at the synchronous frequency and small input inductance that is covered in section 2.2.7.

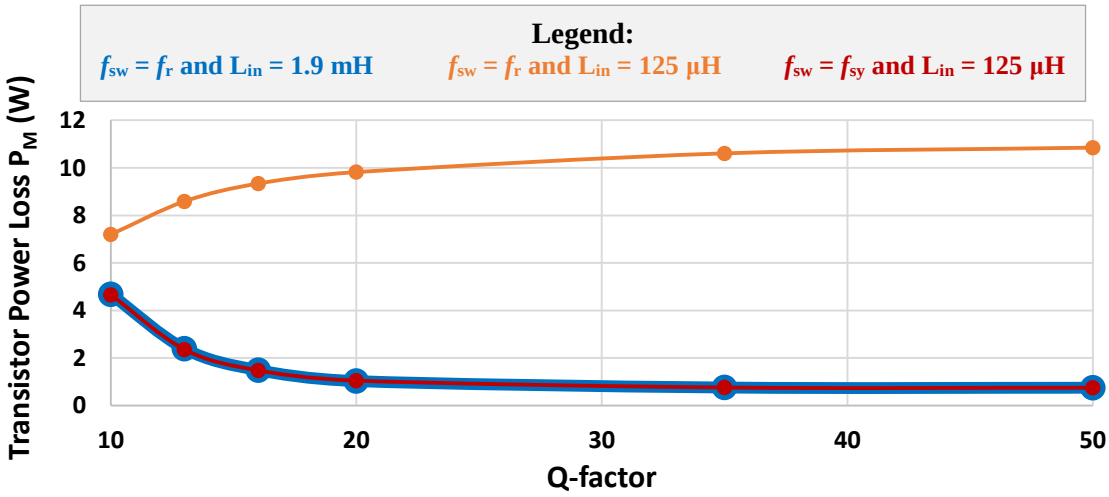


Figure 2-17. The transistor power loss P_M versus the loaded quality-factor for the boost amplifier in different simulated cases. Blue curve represents the operation at resonant frequency with large input inductance that are covered in sections 2.2.3., 2.2.4., and 2.2.5. Orange curve represents the operation at the resonant frequency with small input inductance that is covered in section 2.2.6. Red curve represents the operation at the synchronous frequency and small input inductance that is covered in section 2.2.7.

2.3. Impact of Input Inductance on Synchronous Frequency

2.3.1. Significance of Current Harmonics in the Input Inductors

The behavior of the boost amplifier at the synchronous frequency is performed using a simplified circuit in Figure 2-18 a), where the MOSFETs are replaced with ideal switches. The amplifier's circuit parameters are the same as in Table 2-3. The input inductance is small, L_{in} = 125 μH, allowing abundance of harmonics in the input inductor's current. For the steady-state operation of the boost amplifier, the inductors can be replaced by the current sources that represent each harmonic current in the input inductor. Not all harmonics are significant for the analysis, and the circuit simulations are iterated to determine the minimum number of significant harmonics in the input inductor's current. Two simulation cases are analyzed and compared: idealized amplifier in Figure 2-18 a) with input inductors and voltage source (case 1), and idealized amplifier with equivalent current sources (case 2). The dc, first and second harmonic currents are found significant and their sum approximates well the input inductor's current:

$$\begin{aligned} I_{L1}(t) &= I_{L1}^{(0)}(t) + I_{L1}^{(1)}(t) + I_{L1}^{(2)}(t) \\ I_{L2}(t) &= I_{L2}^{(0)}(t) + I_{L2}^{(1)}(t) + I_{L2}^{(2)}(t) \end{aligned} \tag{2-26}$$

where $I_{L1}^{(n)}(t) / I_{L1}^{(n)}(t)$ represents the nth harmonic component of I_{L1}/I_{L2} current. Due asymmetry of the S_1/S_2 switching functions it is true that

$$\begin{aligned} I_{L1}^{(0)}(t) &= I_{L2}^{(0)}(t) = I_L^{(0)}(t) \\ I_{L1}^{(1)}(t) &= -I_{L2}^{(1)}(t) = I_L^{(1)}(t) \\ I_{L1}^{(2)}(t) &= I_{L2}^{(2)}(t) = I_L^{(2)}(t) \end{aligned} \tag{2-27}$$

Harmonic components contain amplitude and phase information

$$\begin{aligned} I_L^{(0)}(t) &= I_{Lm0} \\ I_L^{(1)}(t) &= I_{Lm1}\sin(\omega t + \gamma_1) \\ I_L^{(2)}(t) &= I_{Lm2}\sin(2\omega t + \gamma_2) \end{aligned} \tag{2-28}$$

where I_{Lmn} is the nth harmonic magnitude and γ_n is the nth harmonic phase angle. The phase angles are referenced to the rising edge of the switching function $S_2(t)$, defined with (2-9). Three current sources are sufficient to completely replace each of input inductors as shown in Figure 2-18 b). The amplitude and the phase of the current sources is given in the Table 2-4.

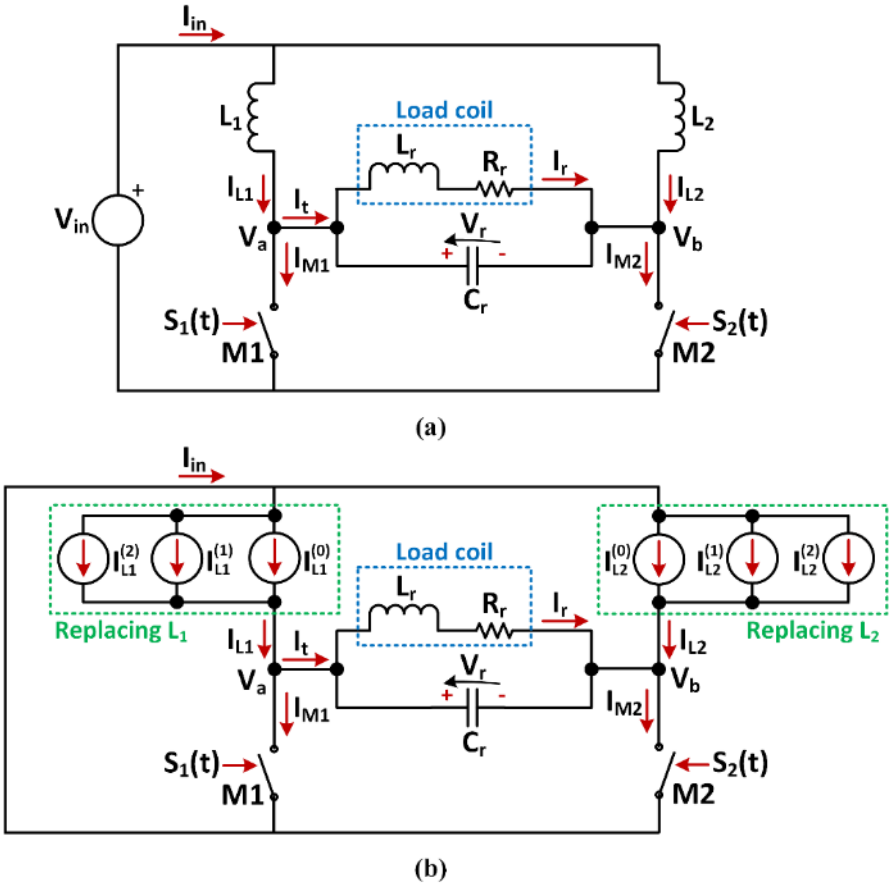


Figure 2-18. (a) Idealized boost amplifier with ideal switches replacing MOSFETs. Simpler topology is used to analyze the operation at the synchronous frequency. (b) Boost amplifier with input inductors and voltage power supply replaced by current sources. Each significant harmonic is replaced by a current source of amplitude and phase as noted in Table 2-4. The amplifier's steady-state operation is equivalent for both cases, and it is shown in Figure 2-19.

Table 2-4. Parameters of Current Sources in Figure 2-18 b) that Replace Input Inductors in Figure 2-18 a). The values are obtained from LT spice simulation.

Current harmonic	$I_{L1}^{(0)}$	$I_{L1}^{(1)}$	$I_{L1}^{(2)}$	$I_{L2}^{(0)}$	$I_{L2}^{(1)}$	$I_{L2}^{(2)}$
Amplitude (A)	1.372	1.019	0.212	1.372	1.019	0.212
Phase (°)	-	90.3	1.1	-	-89.7	1.1

The amplifier operation at the steady state is given in Figure 2-19 for both simulation cases. The agreement between time-domain waveforms is good for both simulations. The removal of the second harmonic current would lead to significant error since the amplitude of the second harmonic is around 15 % of the dc current.

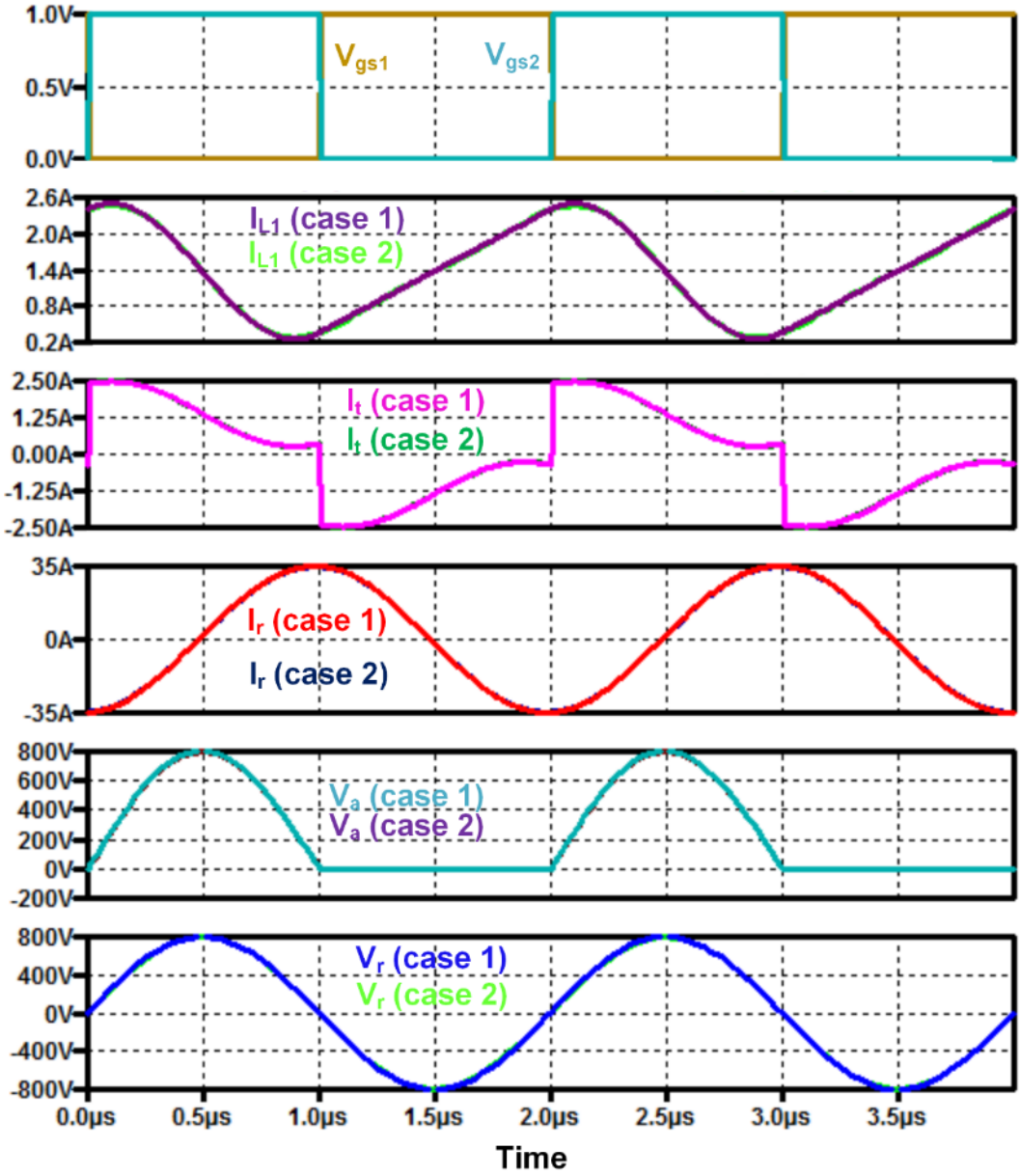


Figure 2-19. The Comparison of Boost inverter's simulation waveforms for circuits in Figure 2-18 a) and Figure 2-18 b). The circuit parameters are given with Table 2-3 and Table 2-4. The results show excellent agreement between simulation cases and confirm that the input inductor's current can be approximated with its dc, first, and second harmonic.

The approximation given with (4-4) is valid even if the input inductance is further decreased to the value comparable with the load coil's inductance. However, the amplifier's operation would be very lossy because of large circulating currents.

The tank's input current is derived from (4-3), (2-9), (4-4), and (4-5):

$$I_t(t) = \begin{cases} I_L^{(0)}(t) + I_L^{(1)}(t) + I_L^{(2)}(t), & S_1(t) = 0, \quad 0 \le t < \dfrac{T}{2} \\ -I_L^{(0)}(t) + I_L^{(1)}(t) - I_L^{(2)}(t), & S_1(t) = 1, \quad \dfrac{T}{2} \le t < T \end{cases} \tag{2-29}$$

The (2-29) can be rewritten as a sum of currents that are generated from different harmonics in the input inductor's current

$$I_t(t) = I_{t0}(t) + I_{t1}(t) + I_{t2}(t) \tag{2-30}$$

where

$$\begin{aligned} I_{t0}(t) &= I_{Lm0} \cdot \left(S_2(t) - S_1(t)\right) \\ I_{t1}(t) &= I_L^{(1)}(t) \approx I_{Lm1} \cos(\omega t) \\ I_{t2}(t) &= I_L^{(2)}(t) \cdot \left(S_2(t) - S_1(t)\right) \end{aligned} \tag{2-31}$$

The result is shown graphically in Figure 2-20, where the equivalent circuit model of the boost amplifier's switching stage is presented. The tank's input current is a sum of three elements: a square-wave source $I_{t0}(t)$, a cosine source $I_{t1}(t)$, and modulated sine-source $I_{t2}(t)$ whose frequency is twice the switching frequency. The square-wave source is the same as for the case when input inductance is large, given with (2-10) and Figure 2-6. The cosine source represents a circulating current that flows through both input inductors L_1 and L_2, and the resonant tank. Its conduction path completely avoids the switches, so the current in switch M1 is

$$I_{M1}(t) = \begin{cases} 0, & S_1(t) = 0, \quad 0 \le t < \dfrac{T}{2} \\ 2 \cdot \left(I_L^{(0)}(t) + I_L^{(2)}(t)\right), & S_1(t) = 1, \quad \dfrac{T}{2} \le t < T \end{cases} \tag{2-32}$$

The $I_{t2}(t)$ source contribution to conduction loss of the switch is minor since the RMS current is dominated with dc component. The only significant influence it makes is on the synchronous frequency. The active power transfer to the load is obtained just with the square-wave source $I_{t0}(t)$. The instantaneous power at the input of the resonant tank is

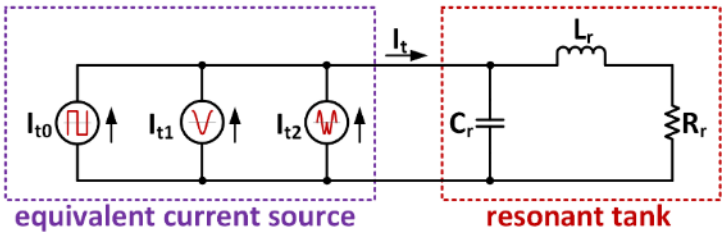


Figure 2-20. Boost inverter's switching stage reflected to the load side. Three current sources are present when input inductance L_{in} is small: a square-wave source $I_{t0}(t)$, cosine source $I_{t1}(t)$, and modulated sine-source $I_{t2}(t)$ whose frequency is two times the switching frequency. Only the square-wave source is present when inductance L_{in} is large, as indicated in Figure 2-6.

$$p_t(t) = V_r(t)I_t(t) = V_r(t)I_{t0}(t) + V_r(t)I_{t1}(t) + V_r(t)I_{t2}(t) = p_{t0}(t) + p_{t1}(t) + p_{t2}(t) \tag{2-33}$$

The average power is

$$P_t = P_{t0} \tag{2-34}$$

since it is easily shown from (2-15) and (2-31) that $P_{t1} = P_{t2} = 0$. The analysis in this section agrees with conclusions from section 2.2.8. In addition, it is confirmed that

- The synchronous frequency is a math function of the harmonic currents in the input inductors.
- Since the current harmonics are a function of the input inductance L_{in}, the synchronous frequency is a function of the input inductance.
- The current harmonics do not create significant loss in the resonant tank or in the switches. The reduction of the input inductance may influence only the loss in the inductor itself.
- The active power is transferred though the dc component in the input inductor's current. Harmonics circulate through the resonant tank and input inductors as reactive energy, influencing the synchronous frequency. Smaller the input inductance is, the reactive energy is larger.
- Choosing large or small input inductance is a trade-off between larger, more efficient system and smaller, more dynamic system.

2.3.2. Harmonic Decomposition and Balancing

Fourier analysis can be applied to periodic waveforms to obtain harmonic decomposition of the electric signals. A decomposed signal contains an infinite number of harmonics, however, it can be represented as the sum of finite

number of harmonics for given accuracy. The input inductor's current is decomposed with (4-4), (4-5), and (2-28). The accuracy of the decomposition is validated with the circuit simulation whose results are given in Figure 2-19. Circuit variables such as input inductor's voltage and resonant tank's input current will be decomposed later in the text. After the decomposition, a principle of harmonic balancing [97] is applied to determine dependencies between the magnitudes and phases of circuit variables. In harmonic balancing, two expressions are equal if both amplitude and phase are equal for any particular frequency in each expression.

The analysis of steady-state for the boost amplifier in Figure 2-18 a) starts with power equations and calculation of dc components. From (2-22), (2-24), and current-voltage relationship of the resonant coil including the coil resistance, the output active power can be expressed as

$$PA = \frac{1}{2} V_{rm}^2 \frac{R_r}{(\omega L_r)^2 + R_r^2} = \frac{\pi^2}{2} \frac{V_{in}^2}{R_r (1+Q^2)} \tag{2-35}$$

Efficiency is assumed to be very high, so PA = P_{in}. Then

$$I_{Lm0} = \frac{\pi^2}{4} \frac{V_{in}}{R_r (1+Q^2)} \tag{2-36}$$

The relationship between the input voltage and current of the resonant tank is derived to be

$$L_r C_r \frac{d^2 V_r}{dt^2} + R_r C_r \frac{dV_r}{dt} + V_r = L_r \frac{dI_t}{dt} + R_r I_t \tag{2-37}$$

The synchronous frequency will be derived from the harmonic balancing of the left-hand and right-hand side of (2-37). After combining (2-15) with (2-37), the left-hand side can be rewritten as

$$left = L_r C_r \frac{d^2 V_r}{dt^2} + R_r C_r \frac{dV_r}{dt} + V_r = V_{rm} \sqrt{\left(1 - \frac{\omega^2}{\omega_n^2}\right)^2 + \left(\frac{1}{Q} \frac{\omega^2}{\omega_n^2}\right)^2} \sin(\omega t + \theta) \tag{2-38}$$

where $\omega_n = 2\pi f_n$, with f_n being the natural frequency of the resonant tank defined with (4-1), and

$$\theta = \tan^{-1} \left(\frac{\frac{1}{Q} \frac{\omega^2}{\omega_n^2}}{1 - \frac{\omega^2}{\omega_n^2}} \right) \tag{2-39}$$

The tank's input current is given with (2-29). Harmonic decomposition of the current gives

$$I_t(t) = I_{\sin}\sin\omega t + I_{\cos}\cos\omega t \tag{2-40}$$

since high Q-factor filters out the high-frequency content and only the first harmonic will be significant. Sine component is dominated by the DC-component magnitude of the input inductor's current,

$$I_{\sin} = \frac{4}{\pi}I_{Lm0} + I_{Lm1}\cos\gamma_1 - \frac{4}{3\pi}I_{Lm2}\sin\gamma_2 \approx \frac{4}{\pi}I_{Lm0} \tag{2-41}$$

since $\gamma_1 \approx \pi/2$ and $\gamma_2 \approx 0$ from the Table 2-4. The cosine component is dependent on the first and the second harmonic current magnitude of the I_{L1} or I_{L2}:

$$I_{\cos} = I_{Lm1}\sin\gamma_1 + \frac{8}{3\pi}I_{Lm2}\cos\gamma_2 \tag{2-42}$$

The equation (2-40) can be rewritten as

$$I_t(t) = I_{tm}\sin(\omega t + \alpha) \tag{2-43}$$

where $\alpha = \tan^{-1}\frac{I_{\cos}}{I_{\sin}}$ and $I_{tm} = \sqrt{I_{\sin}^2 + I_{\cos}^2}$. The right-hand side of (2-37) is:

$$right = L_r\frac{dI_t}{dt} + R_r I_t = I_{tm}R_r\sqrt{1+Q^2}\sin(\omega t + \alpha + \beta) \tag{2-44}$$

where $\beta = \tan^{-1}Q$. The application of harmonic balance method on (2-37) produces

$$V_{rm}\sqrt{\left(1-\frac{\omega^2}{\omega_n^2}\right)^2 + \left(\frac{1}{Q}\frac{\omega^2}{\omega_n^2}\right)^2} = I_{tm}R_r\sqrt{1+Q^2}$$
$$\theta = \alpha + \beta \tag{2-45}$$

Current-voltage relationship on input inductor L_1 gives

$$V_{L1}(t) = L_{in}\frac{dI_{L1}}{dt} \tag{2-46}$$

The inductor's voltage can also be written as the difference between the input voltage V_{in} and the voltage on the transistor M1, V_a. Due to switching, it is written as

$$V_{L1}(t) = \begin{cases} V_{in} - V_{rm}\sin(\omega t), & S_1(t) = 0,\ 0 \le t < T/2 \\ V_{in}, & S_1(t) = 1,\ T/2 \le t < T \end{cases} \tag{2-47}$$

Harmonic decomposition is applied on (2-47), and then the harmonic balancing with (2-46) produces amplitude and phase information for the current harmonics in the L_1:

$$I_{Lm1} = \frac{1}{2\omega L_{in}} V_{rm}$$
$$\gamma_1 = \frac{\pi}{2} \tag{2-48}$$

and

$$I_{Lm2} \approx \frac{2}{3\pi} I_{Lm1}$$
$$\gamma_2 \approx 0 \tag{2-49}$$

The phase-angle α from (2-43) can be calculated now as:

$$\alpha = \tan^{-1} \frac{I_{\cos}}{I_{\sin}} \approx \tan^{-1} \left(\frac{R_r \left(1+Q^2\right)}{2\omega L_{in}} \left(1 + \frac{16}{9\pi^2}\right) \right) \tag{2-50}$$

As the input inductance L_{in} is reduced, the sine-component I_{sin} stays mostly constant while the cosine-component I_{cos} changes greatly. The equivalent tank current is a quadrature source where sine component depends on the active power that is delivered to the load, while the cosine-component serves to synchronize the switching function with the resonant voltage V_r. Figure 2-21 shows the phasor diagram of the tank's input current and voltage. The synchronization occurs when the phasor of the voltage V_r aligns with the sine-component of the tank's input current. In another words, the phase-difference between V_r phasor and I_t phasor has to be α given with (2-50). The existence of the sine and cosine components indicate that the switching stage of the amplifier behaves as the quadrature current source. This is shown in Figure 2-22. It should be noted that the harmonic decomposition has linearization effect upon the amplifier circuit.

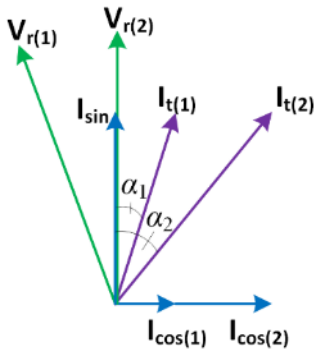


Figure 2-21. Phasor representation of the tank's input current and voltage. Current $I_{t(1)}$ creates insignificant cosine-component $I_{cos(1)}$ in order to align $V_{r(1)}$ with I_{sin}. Current $I_{t(2)}$ creates the right amount of the cosine-component and $V_{r(2)}$ is then aligned with I_{sin}. Phase-angle α_2 corresponds to the α computed in (2-50).

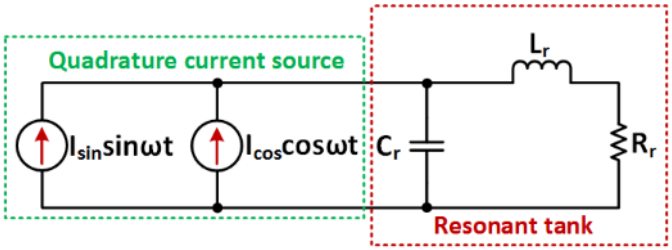


Figure 2-22. The boost amplifier represented as linear circuit. It consists of the quadrature current source and the resonant tank. The quadrature current source has a sine-component, dependent on power transfer conditions in (2-34) and given with (2-41); and a cosine component, dependent on applied voltage and the input inductance, given with (2-42), (2-48), and (2-49).

2.3.3. Relationship between the Input Inductance and the Synchronous Frequency

Combining (2-39), (2-44), and (2-45) gives the term for the synchronous angular frequency:

$$\omega_{sy} = \frac{1}{\sqrt{L_r C_r}} \frac{1}{\sqrt{1+\frac{1}{Q\tan\theta}}} \tag{2-51}$$

The synchronous frequency is simply $f_{sy} = \frac{\omega_{sy}}{2\pi}$. Using (2-44), (2-45), and (2-50), phase-angle θ is connected with α and β as

$$\theta = \alpha + \beta \tag{2-52}$$

If the amplifier's circuit parameters are already set, then the switching frequency is computed for the best efficiency to equal the synchronous frequency using (2-51). The comparison between formulas for natural, resonant, and synchronous angular frequencies is given in Table 2-5, as well as the comparison between computed values for the resonant capacitor C_r. When the input inductance has the infinite value, the formula for the synchronous frequency reduces to one for the resonant frequency since $\alpha \approx 0$ and $\tan\theta = Q$. Further, the resonant frequency formula reduces to one for natural frequency when no loading is present, and therefore Table 2-5 serves as means to compute the switching frequency when different non-idealities are included.

Figure 2-23 shows the comparison between natural, resonant, and synchronous frequency for different values of the input inductance. Other amplifier's parameters are kept constant and equal to ones in Table 2-3. The difference between the resonant and synchronous frequency when L_{in} = 1.9 mH is only few hundred Hertz, making designs with large input inductance successful. As the input inductance is further reduced the synchronous frequency moves away from the resonant frequency. At L_{in} = 125 μH the difference is around 8 kHz.

The (2-51) shows usefulness in different design scenarios for the boost amplifier. When the switching frequency and the resonant tank parameters are known, the (2-51) is used to determine the boost inductance value. Or, if switching frequency, power level, and input inductance are known, the resonant capacitance is computed with (2-51). Figure 2-24 shows the dependence of the resonant capacitance on the input inductance for the switching frequency of 500 kHz and loaded quality-factor of 20.

Table 2-5. Summary on the Computation of Natural, Resonant, and Synchronous Angular Frequency; Summary on the Computation of the Resonant Capacitor C_r.

Natural angular frequency	Resonant angular frequency	Synchronous angular frequency
$\omega = \frac{1}{\sqrt{L_r C_r}}$	$\omega = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_r}{L_r}\right)^2}$	$\omega = \frac{1}{\sqrt{L_r C_r}} \frac{1}{\sqrt{1 + \frac{1}{Q \tan\theta}}}$
$C_r = \frac{1}{\omega^2 L_r}$	$C_r = \frac{1}{\omega^2 L_r} \frac{1}{1 + \frac{1}{Q^2}}$	$C_r = \frac{1}{\omega^2 L_r} \frac{1}{1 + \frac{1}{Q \tan\theta}}$

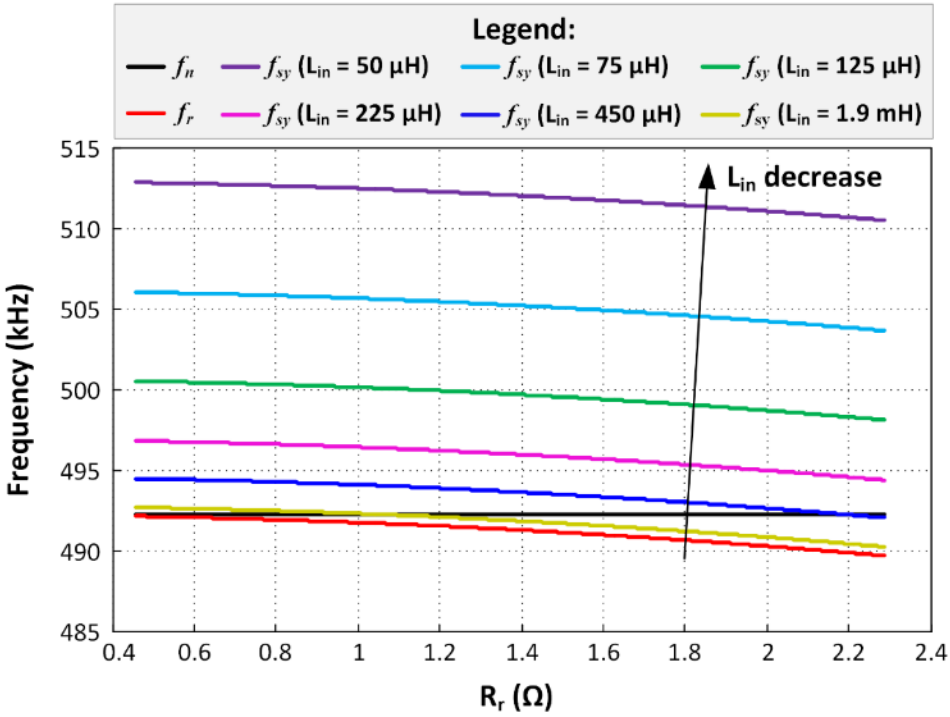


Figure 2-23. Dependence of synchronous frequency on R_r for different cases of input inductance. The graph is generated using formulas in Table 2-5 for amplifier's parameters in Table 2-3. Synchronous frequency increases with decrease of input inductance.

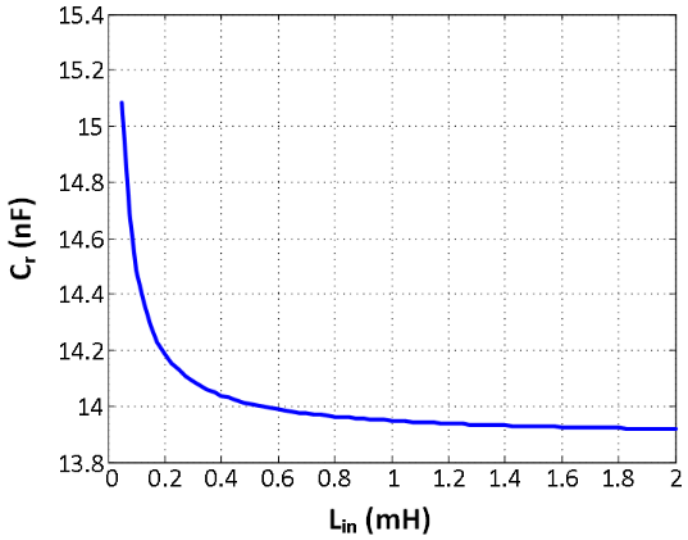


Figure 2-24. The dependence of the resonant capacitor C_r on the input inductance for the switching frequency of 500 kHz, loaded quality-factor of 20 and amplifier's circuit parameters in Table 2-3.

2.3.4. Switching Stage Model of the Boost Amplifier

The input impedance of the resonant tank can be computed from Figure 2-5 a), and it is equal to:

$$z_t(s) = \frac{1}{sC_r} \| \left(sL_r + R_r \right) \tag{2-53}$$

In Figure 2-22 it was shown that the switching stage of the amplifier behaves as the equivalent quadrature current source. When the input voltage of the amplifier V_{in} is dc value, the cosine-component can be replaced with the equivalent impedance since it dependent on the resonant tank's voltage V_r. The cosine-component is computed from (2-42) as

$$I_{\cos} \cos\omega t = \frac{V_{rm}}{2\omega L_{in}} \left(1 + \frac{16}{9\pi^2} \right) \cos\omega t \tag{2-54}$$

The cosine-source can be replaced with the equivalent inductor since:

$$V_{rm} \sin\omega t = -L_{in-eq} \frac{d}{dt} \left(I_{\cos} \cos\omega t \right) = L_{in-eq} \frac{V_{rm}}{2L_{in}} \left(1 + \frac{16}{9\pi^2} \right) \sin\omega t \tag{2-55}$$

The equivalent inductance is then equal to:

$$L_{in-eq} = \frac{2L_{in}}{1 + \frac{16}{9\pi^2}} \tag{2-56}$$

The equivalent model of the switching stage is shown in Figure 2-25. It is represented as a square-wave current source with the source inductance defined with (2-55). The result resembles the well-known Norton theorem. However, Norton theorem is valid for linear circuits only, and its use in the explanations would be erroneous.

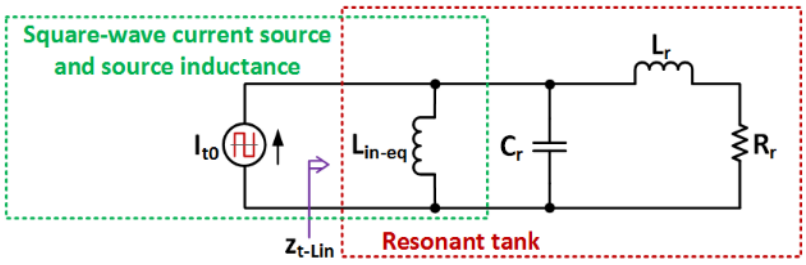


Figure 2-25. Model of the switching stage, consisting of a square-wave current source defined with (2-30) and a source inductance. The source inductance interacts with other passive elements and can be regarded as the part of the resonant tank.

The input impedance when looking from the current source side is equal to

$$z_{t-Lin}(s) = sL_{in-eq} \,||\, \frac{1}{sC_r} \,||\, (sL_r + R_r) \tag{2-57}$$

Impedances $z_t(s)$ and $z_{t\text{-}Lin}(s)$ are plotted in Figure 2-26 for the amplifier's parameters given in Table 2-3. The resonance of the impedance $z_t(s)$ is at the resonant frequency of the tank defined with (2-3). The resonance of the impedance $z_{t\text{-}Lin}(s)$ is at the synchronous (angular) frequency, and it can be rewritten as

$$\omega_{sy} = \sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2} \tag{2-58}$$

where $L_q = L_r \,||\, L_{in-eq}$. Equation (4-2) is more convenient representation of the synchronous angular frequency than (2-51), and makes the computation of the amplifier's parameters easier.

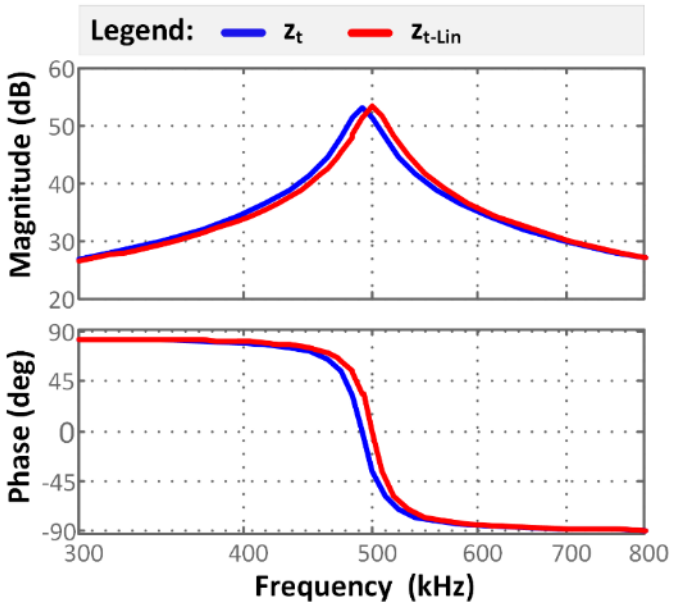


Figure 2-26. Input impedance of the resonant tank. Blue: input impedance defined with Figure 2-5 and (2-57). Resonance determines the resonant frequency. Red: input impedance defined with Figure 2-25 and (2-58) – the input inductors are included in the resonant tank. Resonance determines the synchronous frequency.

2.3.5. Power Factor and Synchronization Factor

The concept of power factor is often used as a measure of synchronization between the tank's input voltage and current. The approach is valid only if both voltage and current are sinusoidal, or one of the two is a sinusoidal and the other is a square-wave waveform. For many power converters this condition is fulfilled, however in the case of the boost amplifier it is not. Power factor is defined as [1]

$$PF = \frac{P_{av}}{V_{rms} I_{rms}} \tag{2-59}$$

For sinusoidal voltage and current waveforms, power factor is equal to

$$PF = \cos\varphi \tag{2-60}$$

where φ is the phase difference between the sine voltage and the sine current. The power factor at the output of the switching stage is computed using (2-59) and it is equal to

$$PF = \frac{1}{\sqrt{1 + \left(\frac{R_r \left(1 + Q^2\right)}{\omega L_{in-eq}} \right)^2}} \tag{2-61}$$

The value of L_{in} = 1.9 mH produces power factor of PF = 99.97 %. Reduced input inductance of L_{in} = 125 μH produces PF = 94.58 % at the synchronous frequency. Both cases for the input inductance operate at the synchronous frequency, and minimize the loss of switches. However, they have different power factor values. For that reason it is more meaningful to use the synchronous factor (SF), defined as

$$SF = \cos\varphi \tag{2-62}$$

where φ is defined as the phase angle between the zero-crossings of the tank's input current (a square wave) and voltage (a sine):

$$V_r = V_{rm} \sin(\omega t + \varphi) \tag{2-63}$$

In both cases for L_{in} the synchronous factor SF is equal to one. The issue of power factor definition and terminology is produced by the dual nature of the input inductors. They form a constant current source and are a part of the resonant tank. Alternatively, the boost amplifier can be seen as the decoupled system of ideal square-wave source and the resonant tank, as in Figure 2-25. The conventional interpretation of the power factor can be then used.

2.4. Impact of Input Inductance on Inductor Size, Amplifier Efficiency, and Dynamic Performance

The qualitative analysis of the boost amplifier performance for different values of the input inductance was performed in the previous sections. Larger inductance will lead to a larger physical inductor that is more efficient. The dynamic performance of the amplifier will be limited, preventing its use in the applications such as antenna drivers. Smaller inductance will lead to a smaller physical inductor that is less efficient, and good dynamic performance. However, quantitative analysis of the boost amplifier performance under different input inductances is required to better understand the design trade-offs between inductor size, system efficiency, and dynamic performance.

Five representative design-cases are analyzed in this section to quantify the trade-offs. For each design-case, the input inductor is designed with regard to its inductance, electrical excitation, and energy requirement. The implementation technology is kept same in all cases. The details on design considerations and constraints are given in section 2.4.1. The size of an inductor is estimated using area product method, with results presented in section 2.4.2. Major power losses in the boost amplifier are modeled and presented in section 2.4.3. Modeled losses include: transistor conduction loss, gate driver loss, input inductor dc and ac conduction losses, input inductor core loss, resonant capacitor conduction loss, and loss due to series inductance with the resonant tank (L_s). The switching loss of the transistor is assumed to be zero because the amplifier is operated at the synchronous frequency. The computation of the power losses is used to evaluate and compare the efficiency of each design-case. Detailed design procedure for input inductors is given in section 2.4.4. The computer program is written to generate large number of possible designs for different input inductance, core size, and change of magnetic flux density. The inductor designs are evaluated using the power loss model given in 2.4.3. Dynamic performance of the boost amplifier is evaluated using low-frequency equivalent model, as presented in section 2.4.5. The input inductance is varied from 75 – 9000 μH to achieve the bandwidths from few kH to 100 kHz.

The quantitative comparison between performances of five design-cases is given in section 2.4.6. Computations show that the amplifier efficiency reaches 99 % mark when input inductance is larger than 750 μH, with low bandwidth of only up to 30 kHz. Bandwidth of 100 kHz can be reached with input inductance 75 μH, but the light-load efficiency will drop to only 95 %. The balance between efficiency, bandwidth, and inductor core-size is found for the minimum value of the input inductance that keeps input power to the resonant tank positive for all load conditions.

2.4.1. Design Considerations

The power amplifier for any given input inductance is designed to operate at the synchronous frequency for the nominal value of quality-factor of $Q_{nom} = 20$. However, to examine the efficiency at any load condition the Q-factor is varied between 10 and 50. The varying quality-factor will impact the coil's resistance R_r and the active power PA at the output. The switching frequency is kept to 500 kHz, and it is equal to the synchronous frequency. The resonant capacitor is computed from the formula for the synchronous frequency. Thus, (2-58) is used for each input inductance value. The amplifier's parameters are taken as the starting point to design the input inductors, and they are summarized in Table 2-6.

The choice of available core shapes and materials from different manufacturers is large, and the analysis for all possible options is impractical. Thus, low-profile PQ-type core shape is selected [1]. The N49 ferrite magnetic material [98] is selected for the frequency range around 500 kHz. The wire winding is implemented using litz wire, which is normal practice for high-frequency magnetic components to avoid skin-effect issues [1]. The use of bobbin is assumed in the design calculations, however, in the actual implementation the bobbin is not used because of availability. The air-gap is assumed to be in the central leg, although in the actual implementation equally long air-gaps are implemented on all legs using a ceramic spacer.

The losses in the inductor's winding are modeled and computed for dc and ac current conduction. The skin effect is considered in order to obtain proper size of the litz wire. The losses due to proximity effect in litz wire are modeled using [99], which is the extension of method applied to solid wire [100]. The ac resistance and the ac conduction loss are then computed. The losses due fringing effect [101] are not included, however, the attention was put not to allow the air-gap to be excessively large.

Table 2-6. The summary of amplifier's parameters used in design of the input inductors.

f_{sw} (kHz)	PQ (kVA)	V_{rm} (V)	V_{in} (V)	I_{rm} (A)	Q_{nom}
500	14	800	254.64	35	20
Q	PA_{nom} (kW)	PA (kW)	$R_{r,nom}$ (Ω)	R_r (Ω)	L_r (μH)
10 - 50	0.7	0.28 – 1.4	1.14	0.46 – 2.27	7.28

The limitation of the core saturation is included in the design procedure. Sinusoidal excitation at the fundamental frequency is assumed to compute the core losses. Although dc and higher harmonics than the fundamental contribute to the core loss as well [102], [103], the sinusoidal approximation allows to use core-loss density data from the core manufacturer [104]. The area-product (AP) method [105] is used to estimate the inductor size. This method is not intended for inductors with large ac excitations [106], and therefore a computer aided design procedure is established. The design procedure varies the input inductance from several tens of μH to few mH, core size, and the allowed maximum of the magnetic flux density change to assess large number of possible designs. The performance limitations are examined. The design procedure will be explained more in the detail in section 2.4.3.

The inductor design is limited with various technological and practical limitations. The core saturation occurs at few hundred of mili-Tesla for ferrites [98]. The conservative value B_{sat} = 200 mT is assumed. The litz wire poorly utilizes the available winding area of an inductor. In practical designs the fill factor K_u is typically limited to $K_u < 0.32$ [101]. The operating temperature of the inductor can change the performance to small extent, and therefore it is assumed to be $T_{ind} \approx 70$ °C. The maximum current density in the winding is often taken as a limitation in the inductor design. Typically values of 2 A/mm^2 < J_{max} < 6 A/mm^2 are assumed to avoid excessive self-heating. For pulsed-power applications it can take larger values, although finite element analysis is required to estimate the operating temperature more precisely. In this work, more aggressive J_{max} = 9 A/mm^2 is assumed. The saturation current density is taken to be $J_{sat} = 1.5\ J_{max}$. In order to minimize the impact of the fringing effect, the air-gap l_g is limited to the tenth of the magnetic core's cross-section diameter D, $l_g < D/10$. The design limitation parameters are tabulated in Table 2-7.

The input inductors are designed for the worst-case of maximum input current which occurs at the maximum power condition in the amplifier. However, inductors' and amplifier's performance are examined for large variation of the load, $10 \leq Q \leq 50$. The design trade-offs are discussed in section 2.4.5.

Table 2-7. Summary of the parameters used for the input inductor design.

B_{sat} (mT)	200	J_{max} (A/mm^2)	9
$K_{u(max)}$	0.32	J_{sat} (A/mm^2)	13.5
T_{ind} (°C)	70	$l_{g(max)}$	D/10

2.4.2. Estimation of the Inductor's Size

The saturation limit depends on the maximum current in the inductor's windings. The inductor current consists of the dc and the ripple part. The dc part is calculated with (2-36), with its maximum value given with:

$$I_{Lm0,\max} = \frac{\pi^2}{4} \frac{V_{in}}{R_{r,\max}(1+Q_{\min}^2)} \tag{2-64}$$

The ripple of the inductor current was approximated with (2-25). However, it can be accurately calculated with

$$ripple = \frac{4}{\pi} \frac{R_{r,\max}\left(1+Q_{\min}^2\right)}{\omega L_{in}} \left(-1 + \frac{2}{\pi} \sin^{-1}\left(\frac{1}{\pi}\right) + 2\cos\left(\sin^{-1}\left(\frac{1}{\pi}\right)\right)\right) \tag{2-65}$$

The ripple is plotted against input inductance value in Figure 2-27. The ripple is very small for input inductances larger than 1 mH so the x-axis is given in the logarithmic scale. For small values of the input inductance the ripple is around two, resulting that inductor current will change from zero to up to two times its mean value given with (2-64). The maximum and minimum values of the input inductor current is given with

$$\begin{aligned} I_{L\max} &= \left(1+\frac{ripple}{2}\right)\cdot I_{Lm0,\max} \\ I_{L\min} &= \left(1-\frac{ripple}{2}\right)\cdot I_{Lm0,\max} \end{aligned} \tag{2-66}$$

The absolute value of the ripple current is

$$\Delta I_L = ripple \cdot I_{Lm0,\max} \tag{2-67}$$

The saturation of the inductor's core occurs when the inductor's current reach saturation level, noted as I_{sat}. In the inductor design procedure, the saturation current I_{sat} is usually assumed to be somewhat larger than the maximum expected current (I_{Lmax}) in the inductor's winding. The 50 % is assumed in this work, thus it can be written:

$$I_{sat} = 1.5 I_{L\max} \tag{2-68}$$

The dependences of maximum inductor current, saturation current, and ripple current on the input inductance are given in Figure 2-28.

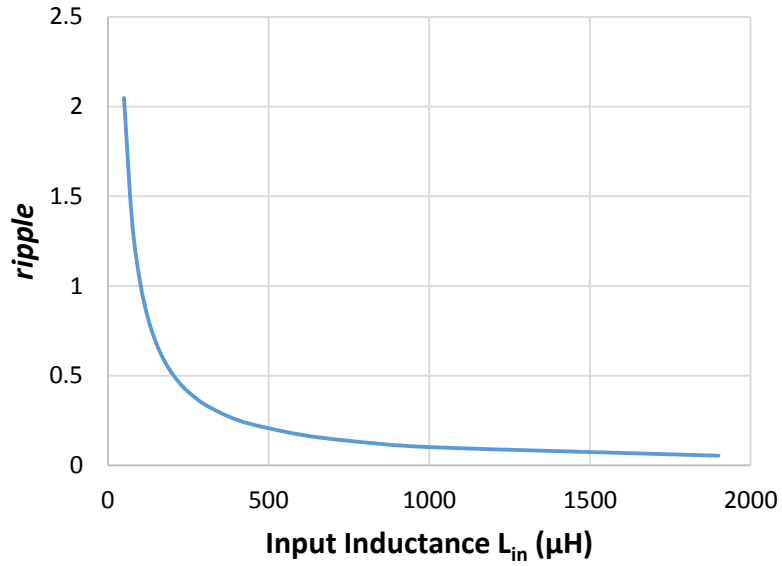


Figure 2-27. Dependence of input inductor's current ripple on the input inductance. The graph is plotted based on (2-65).

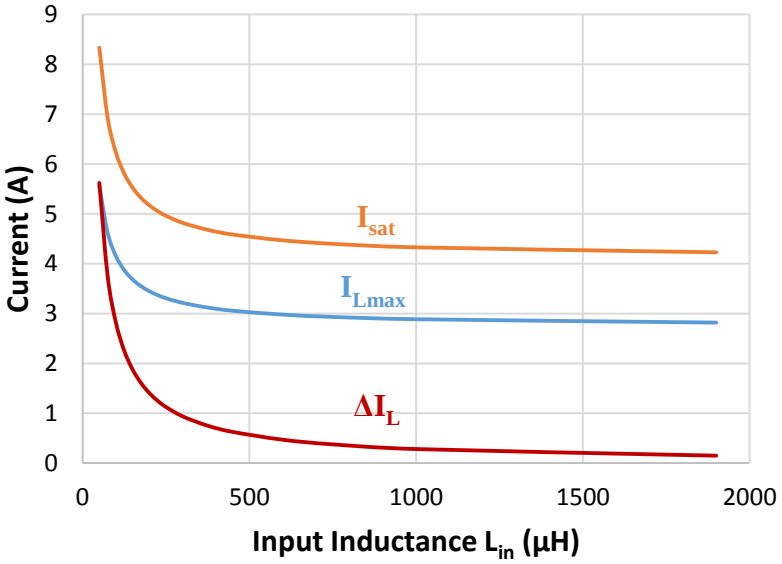


Figure 2-28. Dependence of ripple on the input inductance. The graph is plotted based on (2-66), (2-67), and (2-68).

When the inductor's current reaches the saturation limit I_{sat}, the energy of the inductor is equal to:

$$E_{sat} = \frac{1}{2} L_{in} I_{sat}^2 \tag{2-69}$$

The dependence of the saturation energy on the input inductance is given in Figure 2-29. The saturation energy E_{sat} is the important variable to determine the size of the inductor. The inductor area product (AP) is the multiplication of the window area of the core, W_a, and the cross section of the magnetic path, A_c. The AP [105], as a geometric constant, relates to the energy handling capability of the inductor with

$$AP = W_a A_c \geq \frac{E_{sat}}{\frac{1}{2} K_u B_{sat} J_{sat}} \tag{2-70}$$

where K_u is the fill-factor of the inductor's window area, B_{sat} is the saturation limit, and J_{sat} is the saturation current density given in Table 2-7. The (2-70) refers that the core size (described with it AP) has to be large enough to store required amount of energy. Figure 2-30 shows the dependence of a value of the right-hand side of (2-70) on the input inductance (blue curve). As the value increases, the larger core should be selected for inductor's implementation. For example, the inductor core PQ4040 should be used for design when L_{in} = 1.9 mH. Also, core PQ2625 should be used when L_{in} = 125 µH. However, it is possible to use larger core size to improve the efficiency.

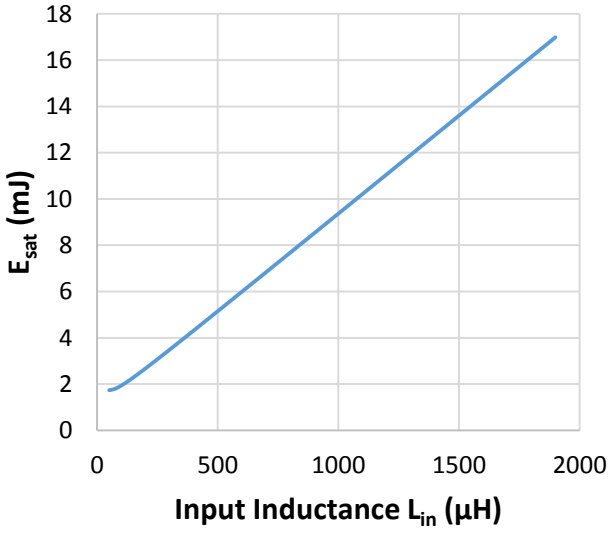


Figure 2-29. Saturation energy dependence on the input inductance.

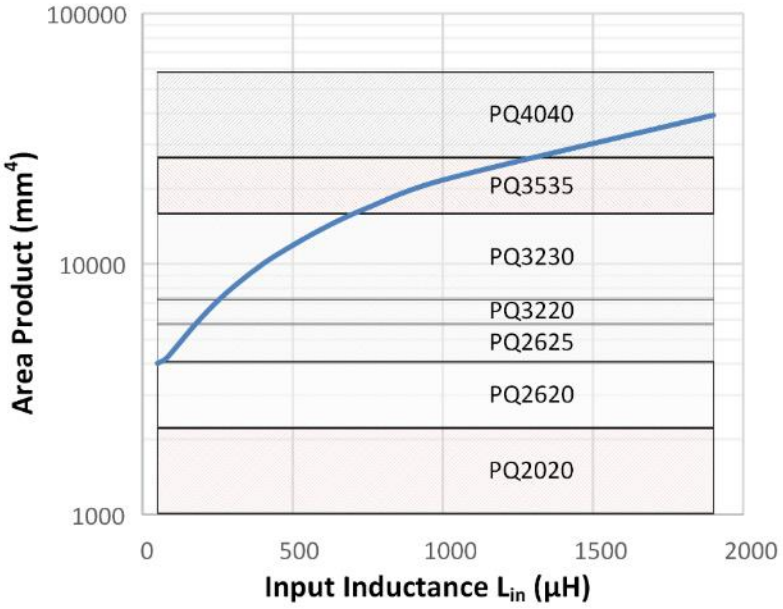


Figure 2-30. Inductor core size selection based on area product method. For L_{in} = 1.9 mH, PQ4040 core is selected. For L_{in} = 1 mH the PQ3535 core is selected. For L_{in} = 225 µH, PQ3220 core is selected. AP method examines saturation limitations for an inductor. Actual high-frequency inductor with large ripple currents requires more detailed computation to determine the size, however, AP method gives good estimates.

2.4.3. Amplifier Losses

The power losses in the amplifier's circuit are modeled for all major components in Figure 2-10: power transistors, gate drivers, resonant capacitor, input inductors, and (parasitic) inductor in series with the resonant tank. Power transistor loss is assumed to have the conduction loss only because the amplifier is operated at the synchronous frequency. The conduction loss is dominated with the dc component of the input inductor current. At any time instance, one transistor is conducting and the other is turned off. Thus, power loss in the channel for a single transistor is:

$$P_{M-ch} = \frac{1}{2} R_{ds} \left(2 I_{Lm0}\right)^2 = 2 R_{ds} I_{Lm0}^2 \tag{2-71}$$

The gate driving circuit for a MOSFET shown in Figure 2-31. It is a basic driving structure that consists of a gate driver component, external gate resistor R_{egr}, and MOSFET itself. The MOSFET contains internal parasitic components, and Figure 2-31 shows its internal gate resistance R_{igr} and internal parasitic capacitances C_{gd}, C_{gs}, and

C_{ds}. The gate driver receives a logic-level (+5 V for high level and 0 V for low level) PWM signal. It outputs level-shifted signal (+20 V for high level and -5 V for low level) to drive a CMF20120 MOSFET with the help of +25 V power supply V_{gd}. The external gate resistance controls the switching speed of the MOSFET, and it is usually set between zero and ten Ohms. The gate driver circuit creates loss since in each switching cycle the electric charge is stored in the gate-source MOSFET capacitor to keep the MOSFET on, and later it dissipated in the resistors R_{egr} and R_{igr} to keep the MOSFET off. If the internal losses of the gate driver circuit are neglected, the gate driver loss is the function of the gate charge of the power MOSFET, Q_g, applied gate driver voltage, V_{gd}, and switching frequency, f_{sw}:

$$P_{gd} = Q_g V_{gd} f_{sw} \tag{2-72}$$

The gate driver loss is split between the rate resistors R_{egr} and R_{igr}, and therefore it can be written:

$$P_{egr} = \frac{R_{egr}}{R_{egr} + R_{igr}} P_{gd} \text{ and } P_{igr} = \frac{R_{igr}}{R_{egr} + R_{igr}} P_{gd} \tag{2-73}$$

The power loss that is dissipated in the MOSFET (at synchronous frequency) is

$$P_M = P_{M-ch} + P_{igr} \tag{2-74}$$

The resonant capacitor loss is

$$P_{cap} = \frac{1}{2} ESR_{Cr} I_{rm}^2 \tag{2-75}$$

where ESR_{Cr} is the equivalent series resistance of the capacitor. Significant loss may come from the series inductance with the resonant tank, L_s (Figure 2-10), since the resonant tank may be placed further away from the switching stage. During the switching instance, the energy in the inductor L_s changes approximately by:

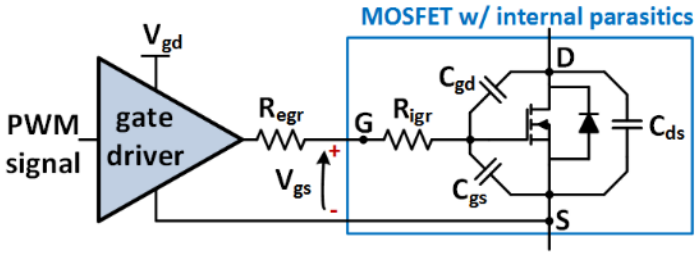


Figure 2-31. Gate driving circuit of a MOSFET. MOSFET is shown with internal parasitic components: capacitances C_{gd}, C_{gs}, and C_{ds}; internal gate resistance R_{igr}. For CMF20120 MOSFET, the internal gate resistance is R_{igr} = 5 Ω [92].

$$E_s = \frac{1}{2} L_s \left(2 I_{Lm0}\right)^2 \tag{2-76}$$

However, it must be noted that this approximation is valid if the amplifier is operated at the synchronous frequency. The stored energy is released at the moment of switching, and it will resonate between L_s and C_{oss} capacitor of the MOSFET. Eventually, the energy will be damped and lost. The inductor L_s changes its energy levels two times in one period of amplifier's operation, and therefore the associated loss with the series inductor is

$$P_s = 2 f_{sw} E_s \tag{2-77}$$

Both conduction loss and the core loss are included in the input inductors loss computation. The conduction loss is the sum of the dc current and ac current losses in the copper windings:

$$P_{Lin-cond} = P_{Lin-dc} + P_{Lin-ac} \tag{2-78}$$

The dc loss is simply

$$P_{Lin-dc} = R_{dc} I_{Lm0}^2 \tag{2-79}$$

where R_{dc} is the dc winding resistance of the inductor given with

$$R_{dc} = \frac{\rho n_M MLT}{A_{w(litz)}} \tag{2-80}$$

The ρ is copper resistivity, n_M is number of inductor turns, MLT is the mean length of a turn, and $A_{w(litz)}$ is the cross-section of the copper area of the used litz wire. The ac conduction loss can be approximated with

$$P_{Lin-ac} = \frac{1}{2} R_{ac} I_{Lm1}^2 \tag{2-81}$$

since the contribution of the second harmonic current are neglected due to relatively small amplitude. The ac resistance of the winding is computed as

$$R_{ac} = R_{dc} F \tag{2-82}$$

where F is the winding resistance ratio of the litz wire [99]. The detailed derivations are given in Appendix C. The fringing effect related losses in the windings are neglected. The inductor core losses depend on the core volume, V_c, and the core-loss density ($P_{v\sin}$) for given excitation. For simplicity, the core-loss data for sinusoidal excitation is used in the computation. Thus, it can be written

$$P_{Lin-core} = V_c P_{v\sin} \tag{2-83}$$

The total inductor loss is the sum of the conduction and core loss:

$$P_{Lin-tot} = P_{Lin-cond} + P_{Lin-core} \tag{2-84}$$

The total amplifier loss is the sum of all modeled losses:

$$P_{tot} = 2P_{M-ch} + 2P_{gd} + P_{cap} + P_s + 2P_{Lin-tot} \tag{2-85}$$

The losses may be divided into groups based on their origin and dependence. The first group are fixed losses, P_{fx}, since they are same for any boost amplifier design with parameters in Table 2-6. These include resonant capacitor losses and total gate driver losses:

$$P_{fx} = 2P_{gd} + P_{cap} \tag{2-86}$$

The second group of losses depend on the current ripple in the input inductor, ΔI_L. Core loss and the ac conduction loss in the input inductors belong to this group:

$$P_{\Delta I} = 2P_{Lin-core} + 2P_{Lin-ac} \tag{2-87}$$

The third group of losses are load-dependent. MOSFET conduction loss and input inductor dc conduction loss are in this group:

$$P_Q = 2P_{M-ch} + 2P_{Lin-dc} \tag{2-88}$$

Taking into account all losses in (2-85), and from (2-20), the amplifier efficiency is derived as

$$\eta = \frac{1}{1 + \frac{P_{tot}}{PA}} \tag{2-89}$$

The efficiency formula will be used in the next section to assess the amplifier performance for different input inductance values and input inductor designs.

2.4.4. Design Procedure for the Input Inductors

The performance of the boost amplifier is largely impacted by the input inductor design. The input inductance influences power losses, size, and dynamic response. The choice of the core size and operating flux density further increase the complexity of the performance optimization for the amplifier. Large number of possible design scenarios exist and they have to be evaluated in fast and systematic manner. The custom computer program is made in *Mathcad Prime* for this purpose.

The algorithm of the program is given in Figure 2-32. The computer program takes the parameters from the electric circuit as inputs. These are the power requirements, operating frequency, input voltage, and the range for possible values of the input inductance. The circuit parameters are given in Table 2-6, while the input inductance range is from 50 μH to 1900 μH. The inputs are processed to create a range of possible excitations for the input inductor. The maximum current, saturation current, and the current are computed using (2-64) - (2-68). The electric inputs are

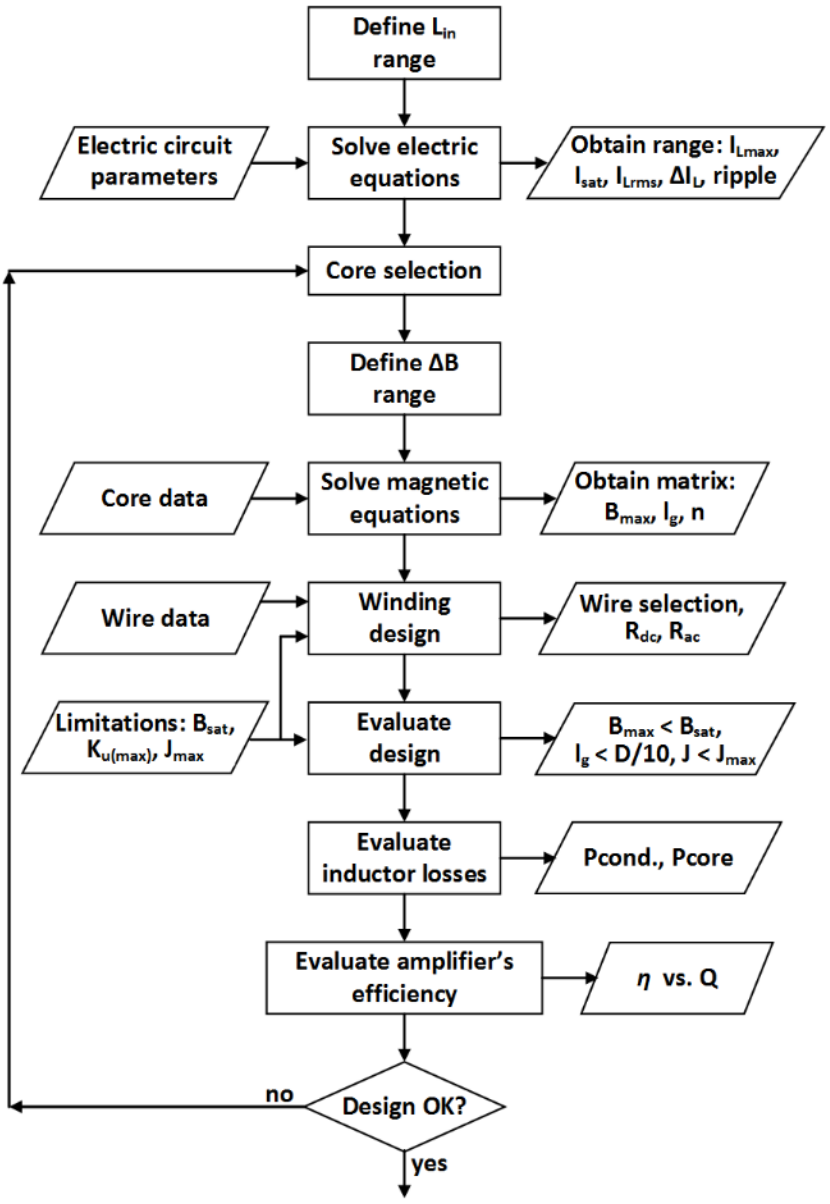


Figure 2-32. The Algorithm of inductor design program in Mathcad Prime.

then used in magnetic design. The inductor cores are evaluated one by one. The PQ-core geometrical data is found in the corresponding datasheets for each part. The core-loss density data is extracted from the manufacturer's *MDT* computer program that contains data for the N49 PQ-cores. Six core sizes are evaluated, from PQ2020 to PQ4040. The magnetic flux density ΔB range is defined to be from 10 mT to 100 mT. The number of turns in the winding are computed with:

$$n = ceil\left(\frac{L_{in}\Delta I_L}{A_c \Delta B}\right) \tag{2-90}$$

where ΔI_L is computed with (2-67), A_c is cross-section of the magnetic core, and *ceil*() is mathematical function that rounds the real number to the first higher integer value. The air-gap is computed with:

$$l_g = \frac{\mu_0 n^2 A_c}{L_{in}} \tag{2-91}$$

where μ_0 is permeability of free space. Maximum magnetic flux density is obtained with:

$$B_{\max} = \frac{L_{in} I_{\max}}{n A_c} \tag{2-92}$$

Next step in algorithm is the winding design. The database is created with litz wire with AWG equivalent sizes from 9 to 30. In order to minimize conduction loss, the largest possible wire size is used to fill the window area completely for any given number of turns. The fill factor K_u is evaluated not to cross the maximum value of $K_{u(max)} = 0.32$. The winding dc and ac resistances are computed with (2-80) and (2-82).

The program has computed large number of possible designs by now. However, not all designs are valid. Some will have operating flux density or air-gap larger than the specified limit. Excessive current density in the windings may be tolerated in many cases if the inductor does not operate outside of thermal limitations. Figure 2-33 show the matrix of all computed inductor designs for the core PQ3220. Red region represent design that has the current density larger than the saturation limit. Orange regions represent design cases with excessive air-gap length. Light-green are the regions with excessive current density. Green regions are valid designs. The inductor experiences the lowest loss if the conduction and core losses are balanced [1]. This is the case for 50 mT ≤ ΔB ≤ 70 mT and 150 μH ≤ L_{in} ≤350 μH.

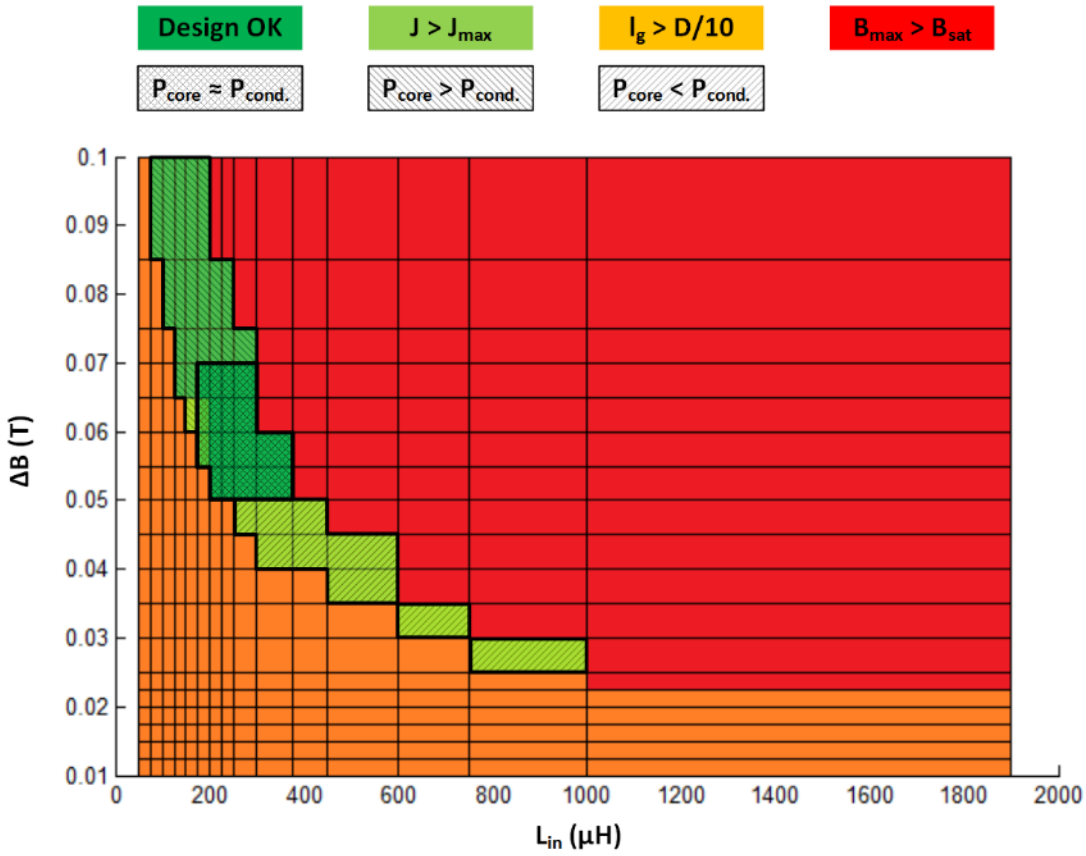


Figure 2-33. Matrix of input inductor designs for PQ3220 core. Red regions represent invalid designs when maximum flux density is larger than the saturation limits. Orange regions represent designs when air-gap is excessive – larger than 1/10 of the core cross-section diameter. Light green regions represent designs with excessive current density that may cause thermal problems. In pulsed-power operation this can be tolerated. Green regions represent valid designs. The power loss in the inductor is minimized when $P_{core} \approx P_{cond}$.

Figure 2-34 shows the matrix of the designs for the PQ4040 core. The number of possible designs is larger, however, the optimal design region characterized with $P_{core} \approx P_{cond}$ shift to the higher values of the input inductance. The optimal design occurs for 25 mT $\leq \Delta B \leq$ 35 mT and 600 μH $\leq L_{in} \leq$750 μH. The region where L_{in} < 600 μH has large core losses and elevated overall inductor losses. The region where 750 μH < L_{in} < 1000 μH is large conduction losses and elevated overall inductor losses. The designs where 1000 μH < L_{in} are not feasible mainly due to excessive air-gap. Special winding designs would be required for this case to minimize fringing effect losses. The conductors would have to be placed away from the gap and the lines of magnetic flux. Otherwise, the multi-core inductor design would be required.

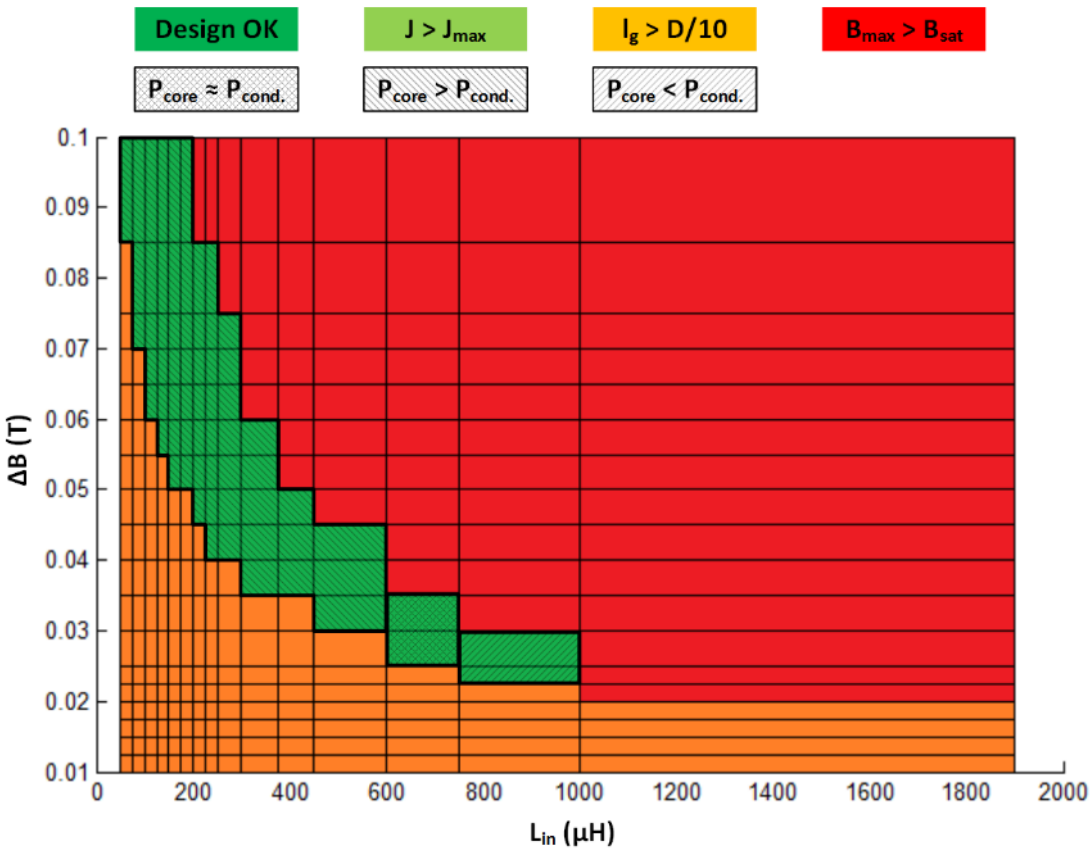


Figure 2-34. Matrix of input inductor designs for PQ4040 core. Red regions represent invalid designs when maximum flux density is larger than the saturation limits. Orange regions represent designs when air-gap is excessive – larger than 1/10 of the core cross-section diameter. Light green regions represent designs with excessive current density that may cause thermal problems. In pulsed-power operation this can be tolerated. Green regions represent valid designs. The power loss in the inductor is minimized when $P_{core} \approx P_{cond}$.

Final step in the algorithm is the evaluation of the amplifier's performance. The inductor's conduction and core losses are computed with (2-78) - (2-84). The total losses of the amplifier are calculated with (2-85), and the efficiency is evaluated with (2-89) for all loaded quality factors in the range of $10 \leq Q \leq 50$. The core size can be changed for trade-offs between efficiency, size, and dynamic performance. The broader discussion is given in section 2.4.6. Table 2-8 summarizes all parametric ranges that are used in evaluating inductor and amplifier performance.

Table 2-8. Summary of the parameters that influence the input inductor design and amplifier's efficiency.

L_{in} (μH)	50 - 1900	ΔB (mT)	10 - 100
Core size	PQ2020 – PQ4040	Wire size (AWG number)	9 - 30
Q	10 - 50		

2.4.5. Dynamic Performance of Boost Amplifier

Low-frequency equivalent model [**68**] is commonly used to investigate dynamic performance of the boost amplifier. The model derived from energy-power relationship at the input side of the inverter (derivation is given in Appendix D), and it is represented as equivalent buck-type filter (Figure 2-35). The model parameters are calculated as

$$\begin{aligned} L_{eq} &= \frac{L_{dd}}{2} \\ C_{eq} &= \pi^2 C_r \\ R_{eq} &= \frac{2}{\pi^2} R_r \left(1+Q^2\right) \end{aligned} \tag{2-93}$$

The output voltage of the equivalent model is π times smaller than the amplitude of the resonant tank voltage:

$$V_{rm} = \pi \cdot V_{req} \tag{2-94}$$

The input-output voltage transfer function is then expressed as

$$G_{io}(s) = \frac{V_r(s)}{V_{in}(s)} = \frac{\pi \cdot V_{req}(s)}{V_{in}(s)} = \frac{\pi}{1 + s\frac{L_{eq}}{R_{eq}} + s^2 L_{eq} C_{eq}} \tag{2-95}$$

The equivalent inductance L_{eq} is a half of the input inductance. As the input inductance L_{in} is reduced, the dynamic response of the amplifier is increased since the L_{in} is in series with the input voltage source. This property is shown in Figure 2-36, where the magnitude of the input-output voltage transfer function is plotted for wide-range of the input inductance and the parameters of the resonant tank in Table 2-1. When the input inductance is in the mili-Henry range, the bandwidth of the amplifier is limited to few tens of kilohertz. However, for input inductance of L_{in} = 125 uH, the bandwidth is around 80 kHz. The large bandwidth of the amplifier is desirable in order to provide fast-changing magnitude of the output waveforms, or to accommodate for the fast changing load conditions.

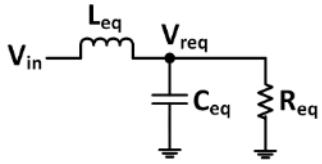


Figure 2-35. Low-frequency equivalent model of the inverter.

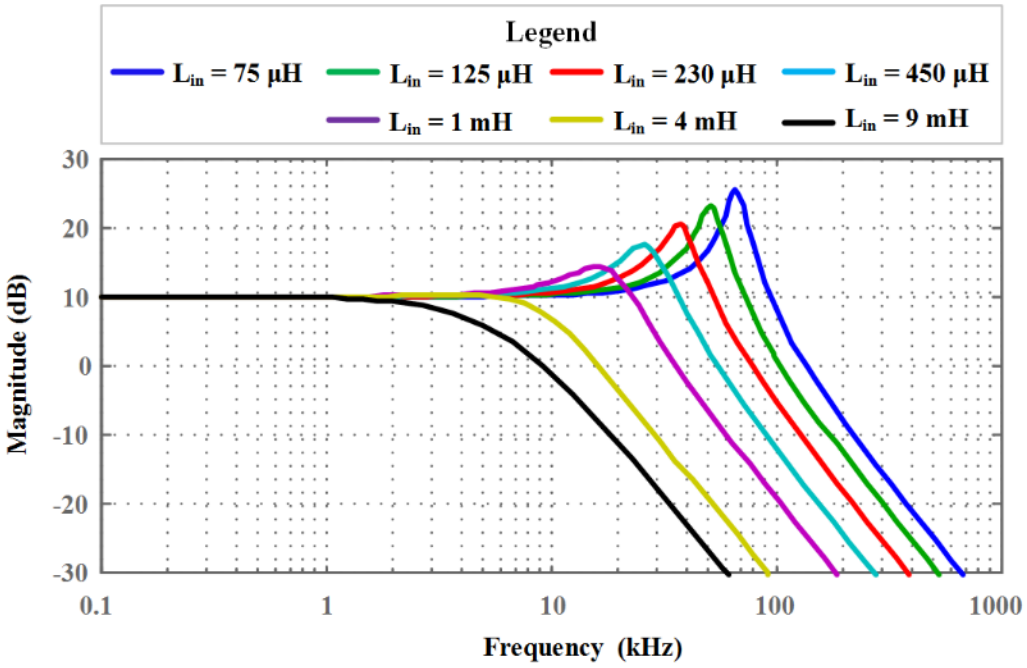


Figure 2-36. Input-output voltage transfer function for the Low-frequency model in Figure 2-35. The parameters of the resonant tank are given in Table 2-6, while the input inductance is varied from 75 µH to 9 mH.

2.4.6. Discussion

Five different cases of the input inductor and power amplifier designs are examined to quantify the trade-offs between the system efficiency, bandwidth, and the input inductor's size. Each design-case uses inductor design procedure in 2.4.4 to optimize performance by varying core size, inductance, and magnetic flux density, as summarized in Table 2-8. Other parameters, such as maximum magnetic flux density, air gap length, number of turns, and the winding design (including winding resistances for dc and ac currents, R_{dc} and R_{ac}) are computed from the design procedure. Design-cases are evaluated with the help of amplifier loss analysis in section 2.4.3, and system bandwidth in section 2.4.5.

Design-cases for the input inductors are given in Table 2-9, and they are labeled as "Inductor 1", "Inductor 2", … "Inductor 5". The Inductor 1 design case favors high bandwidth, regardless of efficiency. Small value of the input inductance is chosen, L_{in} = 75 μH, which resulted in small core size and large variation of the magnetic flux density. Inductor 2-3 design cases aim for both moderate core size, good bandwidth, and reasonably high efficiency. Inductor 4-5 design cases aim for good amplifier efficiency only. Following text describes the power losses and efficiency evaluation for all five design-cases.

The gate driver circuit scheme is given with Figure 2-31. The driver circuit parameters correspond to the actual hardware implementation. The driving voltage is V_{gd} = 25 V since the MOSFET is driven with +20 V/-5 V voltage level signal. The gate charge of MOSFET is taken from CMF20120 datasheet, Q_g = 90.8 nC, as well as the internal gate resistance, R_{igr} = 5 Ω. The external gate resistance is also equal to R_{egr} = 5 Ω. The gate driver power losses are calculated from (2-72), and (2-73) to be $P_{igr} = P_{egr}$ = 0.57 W.

Table 2-9. Different design examples for the input inductors. The amplifier's efficiency is compared for the designs in Figure 2-40.

Design Case	Inductor 1	Inductor 2	Inductor 3	Inductor 4	Inductor 5
Core Size	PQ2625	PQ3220	PQ3220	PQ3220	PQ4040
L_{in} (μH)	75	125	225	750	750
ΔB (mT)	100	75	50	25	25
B_{max} (mT)	142	125	133	195	195
l_g (mm)	0.7	0.97	1.18	1.38	1.14
n (turns)	19	25	37	73	60
Equivalent AWG	18.5	19.5	21	24	15
Strands No./Strand AWG	150/40	125/40	120/42	100/44	125/36
R_{dc} (mΩ)	47	64	135	503	70
R_{ac} (mΩ)	263	424	871	2.335	9532
System Bandwidth (kHz)	100	80	55	30	30

The value parasitic series resistance of the resonant capacitor, ESR_{Cr}, is obtained from capacitor characterization measurement. The designed amplifier utilizes 1 nF, 2000 V rated, NPO surface mounted capacitors with part number C1825C102JGGACTU. The NPO capacitors have stable capacitance value for wide-range of applied voltages and temperatures. Thus, ten capacitors from the same batch were characterized using Agilent 4294A impedance analyzer with 16047E adapter. The average of ten measurements gives capacitance of 970 pF and ESR_{Cr} = 6.4 m Ω. The power loss in the resonant capacitor is computed from (2-75) to be P_{cap} = 3.96 W. The fixed power losses for any amplifier with parameters as in Table 2-6 are P_{fx} = 6.24 W.

The series inductance with resonant tank is designed to emulate the cable connection of the resonant tank to the switching stage. The value of L_s = 250 nH is taken. The on-state resistance of CMF20120 MOSFET is $R_{ds\text{-}on}$ = 100 mΩ, as specified by component datasheet. The above mentioned parameters, and power losses are tabulated in Table 2-10. The amplifier's circuit parameters in Table 2-6, inductor parameters in Table 2-9, and parameters from Table 2-10 are used to compute rest of modeled power losses in section 2.4.3. The ripple current ΔI_L-related losses will be discussed next for any of the examined design-cases.

The core-losses strongly depend on the excitation magnitude, as shown in Figure 2-37. Also, the core-loss depends linearly on the volume of the core. For example, PQ4040 is about two times larger than PQ3220 core, and therefore it will experience about two times larger core loss for the same excitation level. Figure 2-38 presents ΔI_L-related losses for each of the five inductor implementations. Large magnetic flux density lead to high core-losses for Inductor 1 and 2, as shown in Figure 2-38 a). The balanced value for core losses is obtained for Inductor 3 design. The Inductor 4 and 5 designs experience very small core-losses, however, the conduction losses are expected to be high.

Table 2-10. Summary of parameters used in amplifiers loss calculation. Resonant capacitor and gate driver loss are computed from the parameters. These losses are present for any design that utilizes NPO capacitors and SiC CMF20120 transistors.

V_{gd} (V)	Q_g (nC)	R_{egr} (Ω)	R_{igr} (Ω)	P_{egr} (W)	P_{igr} (W)
25	90.8	5	5	0.57	0.57
ESR_{Cr} (mΩ)	P_{cap} (W)	P_{fx} (W)	L_s (nH)	$R_{ds\text{-}on}$ (mΩ)	
6.4	3.96	6.24	250	100	

Figure 2-38 b) shows the conduction losses due to ac-resistance of the winding. Since litz wire with significant number of strands is used for each inductor implementation, as indicated by Table 2-9, the ac-resistance related losses are expected to be small.

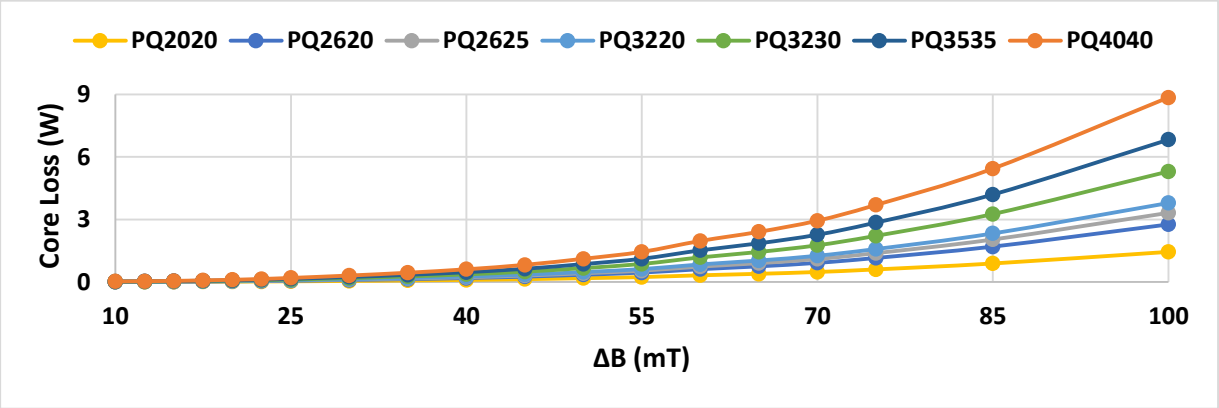


Figure 2-37. Core losses dependence on the change of the magnetic flux density for each PQ core size. The data is computed from the core-loss density data given by manufacturer. The core-loss density data is obtained for the sinusoidal excitation.

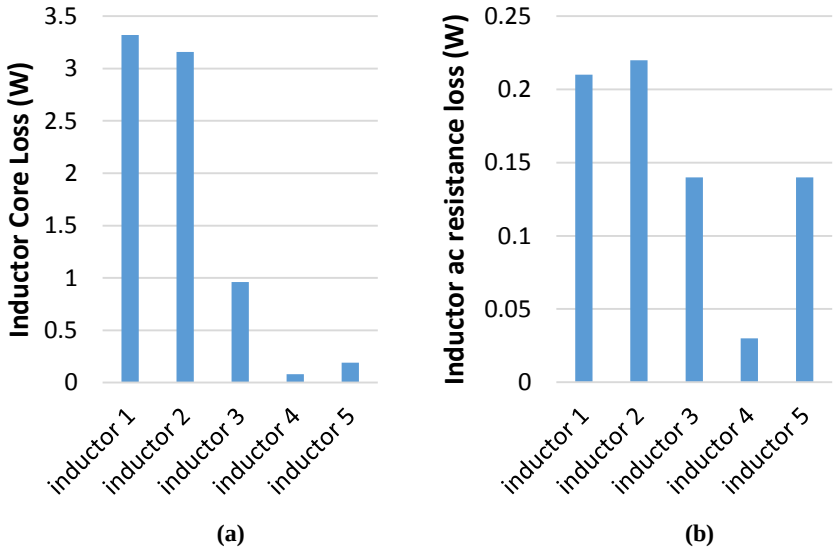
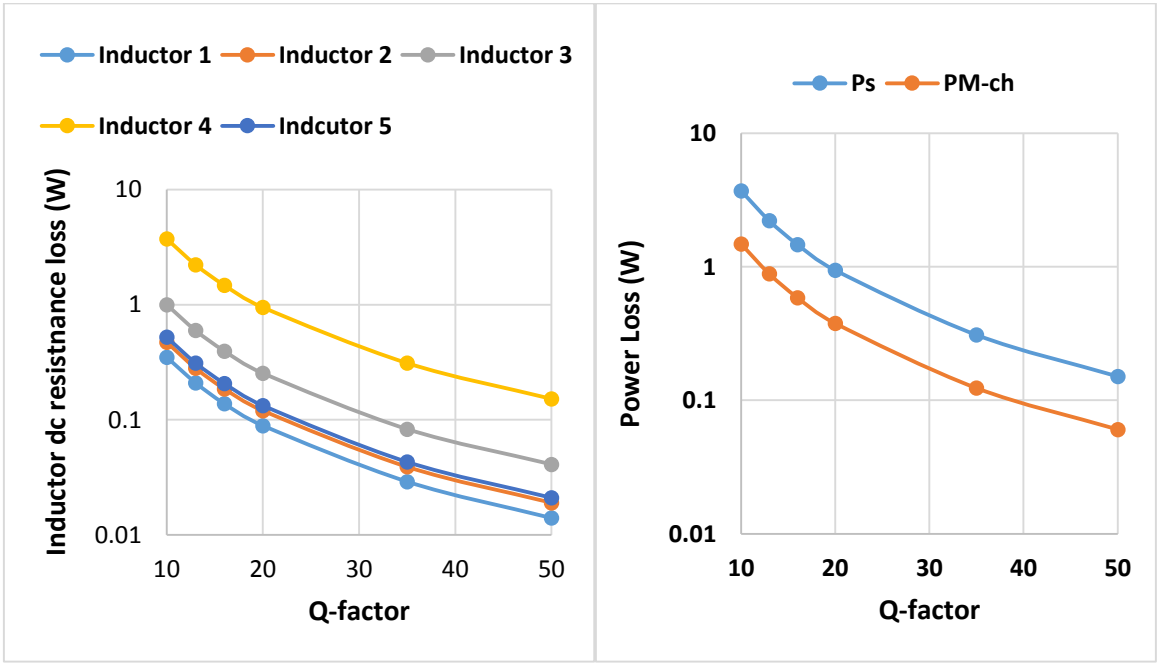


Figure 2-38. Power losses that depend on the ripple of input inductor current: (a) Inductor core-loss; (b) Inductor ac resistance loss.

The load-related losses include the input inductor's dc-resistance loss, L_s-inductor related loss, and on-state MOSFET conduction loss. The input inductor's dc resistance loss is shown in Figure 2-39 a) for each inductor implementation. Inductor 1 design shows the smallest loss due to small number of turns. The loss is increased in Inductors 2-4 because the number of turns is increased for each inductor design, while the inductor's window area is small. Inductor 5 is able to reduce the dc-resistance related losses thanks to its much larger window area, which allows for much thicker and less resistive wire to be used in conducting the inductor's current. The MOSFET's conduction loss ($P_{M\text{-}ch}$) and L_s-inductor related loss (P_s) are plotted in Figure 2-39 b). The $P_{M\text{-}ch}$ loss could be reduced if switch with smaller on-state resistance is used or more MOSFETs are paralleled. The change of MOSFET easily feasible since the output capacitance of a MOSFET is used in computation of the synchronous frequency. The P_s loss is strong function of the series resistance with resonant tank, L_s. Smaller L_s would decrease the loss, however, small L_s is not advisable for non-synchronous or transient operation where current spikes (sections 2.2.4, and 2.2.5) can occur. The amplifier's power losses are quantified for each of the five implementations at this point. In the following, the power losses and the efficiency will be compared for all five implementations.



(a) **(b)**

Figure 2-39. Load-dependent losses: (a) Inductor dc-resistance losses; (b) MOSFET on-state and L_s-related losses.

The design strategy for Inductor 1 is to achieve maximum bandwidth of the system, and therefore small inductance value L_{in} = 75 μH is chosen. The PQ2625 core is selected, as it balances conduction and core losses, and fits with boundary given with area product method in Figure 2-30. The penalty for low inductance and high bandwidth is poor efficiency, as it shown in Figure 2-40 a) where expected efficiencies are plotted for different design scenarios.

Inductor 2 design gives decreased bandwidth since L_{in} = 125 μH. The core size is PQ3220 rather than PQ2625 that is suggested by AP method, since slightly more efficient system is expected. The overall system efficiency is expected to improve (Figure 2-40a) from the previous design case due to smaller inductor losses. The bandwidth of the amplifier reduces to 80 kHz due to larger input inductance.

The trend of increased efficiency is continued with Inductor 3 design, where the inductance is increased to L_{in} = 225 μH and the corresponding core losses are decreased. The benefit is particularly useful at the light load, where approximately 2 % efficiency increase is expected when compared to Inductor 1 case. However, the bandwidth of the amplifier is further decreased to 55 kHz, around the half of the value for the Inductor 1 design-case.

The core losses can be traded-off for the conduction losses for the same core size in order to improve the light-load efficiency. The example is given with Inductor 4 design, where the input inductance is increased to L_{in} = 750 μH. The flux density ΔB is reduced because of the larger input inductance, leading to smaller core losses. Although the benefit of such design is higher light-load efficiency, at heavy-load the efficiency is slightly worse. In practice, this may be more preferable since the light-load condition occurs more often than the heavy-load condition.

Overall efficiency can be slightly increased again with the selection of the larger core size (Figure 2-40b). Inductor 5 utilizes the same inductance value as Inductor 4, but the core size brings larger window area where thicker conductor can decrease conduction losses. The light load efficiency will be same in the two cases, however, the heavy load efficiency will be better for Inductor 5 based system. Also, overall efficiency is larger for Inductor 5 based system than for Inductor 3. However, the penalty of highly efficient system is poor bandwidth, only 30 kHz for L_{in} = 750 μH.

The Inductor 1 based design has superior system bandwidth (2-3 better) than the other design-cases at the expense of the efficiency (1 % - 2 % worse efficiency). Also, the input inductors are much smaller in size – Inductor 1 is 2.67 times smaller than Inductor 5. Inductor 4-5 design-cases have superior efficiency among analyzed design cases. Inductor 2-3 based design try to balance the input inductor size, system bandwidth, and efficiency.

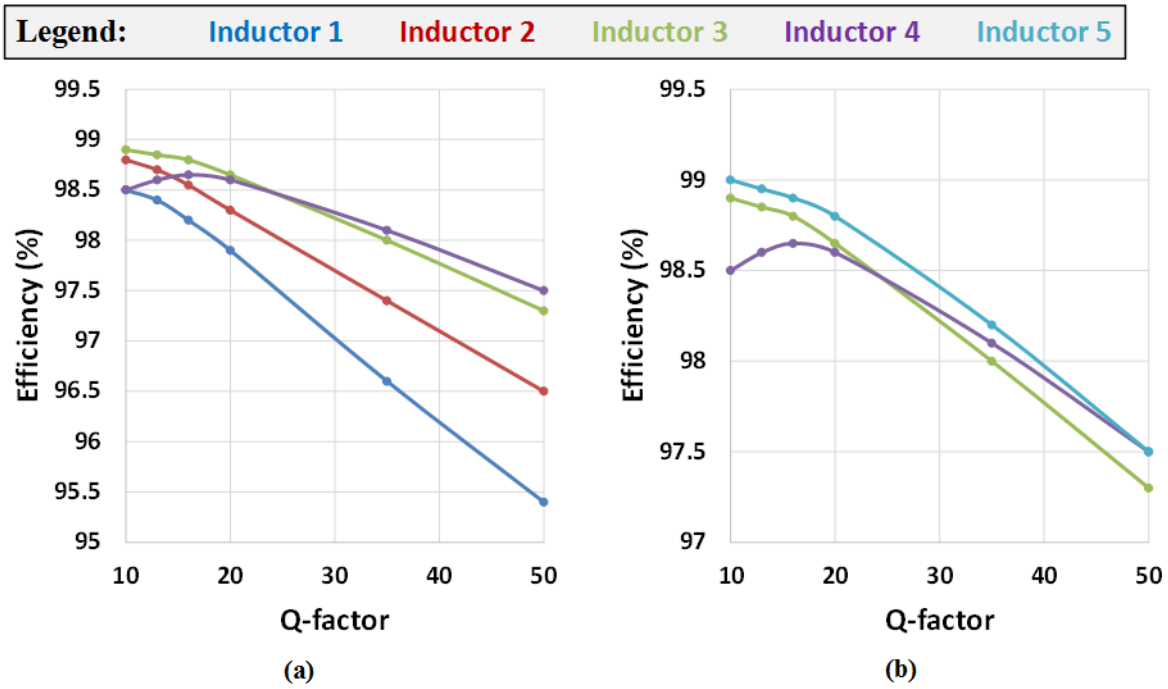


Figure 2-40. Expected efficiency vs. Q-factor for inductor designs in Table 2-9: (a) Increase of the input inductance for core PQ3220 brings more efficient design (Inductors 2-4). If the inductance is further increased the inductor's conduction losses are greater than the core losses, reducing the efficiency at the heavy load (inductor 4). However, light load efficiency is improved since core loss is the major contributor to the total loss. (b) Larger core size (PQ4040) selected for L_{in} = 750 µH (Inductor 5). Light load efficiency is as good as in Inductor 4 case. Heavy load efficiency is improved since winding loss is lower because of larger window area and larger cross section of the winding.

The inductance value to achieve the compromise between the size, efficiency, and bandwidth can be found with the help of instantaneous power $p_t(t)$ that flows to the resonant tank. Based on discussion in section 2.3.1, lower input inductance leads to more reactive power circulation through the resonant tank. Figure 2-41 shows the simulation cases when L_{in} = 125 µH and L_{in} = 232 µH, and the amplifier is operated at the light load (Q = 50). When L_{in} = 125 µH, there are regions with very high and very low (even negative) instantaneous power. During the time with low or negative instantaneous power the amplifier circuit is not utilized – it does not do its purpose to transmit power. Thus, this operation mode should be avoided for best performance. When L_{in} = 232 µH, the instantaneous power is positive, even with significant reactive power circulating through the resonant tank. Thus, for best (optimum) performance, the instantaneous power $p_t(t)$ should always be positive:

$$p_t(t) = V_r I_t(t) > 0 \tag{2-96}$$

Since the resonant capacitor voltage $V_r(t)$ is sinusoidal, the previous condition is equivalent to

$$I_t(t) = I_{L1}(t) - I_{M1}(t) = I_{L1}^{(0)}(t) + I_{L1}^{(1)}(t) + I_{L1}^{(2)}(t) - \frac{1}{2} C_{oss} \frac{dV_{Cr}}{dt} > 0 \tag{2-97}$$

The second harmonic current in the input inductors and the MOSFET's output capacitance current can be neglected for simplicity. Rewriting the previous equation gives:

$$I_t(t) = I_{L1}^{(0)}(t) + I_{L1}^{(1)} > 0 \tag{2-98}$$

From (2-24), (2-28), (2-36), (2-48), and (2-98), the value for optimum input inductance is obtained as:

$$L_{in,opt} = \frac{2}{\pi} \frac{R_{r,\min}\left(1 + Q_{\max}^2\right)}{\omega} \tag{2-99}$$

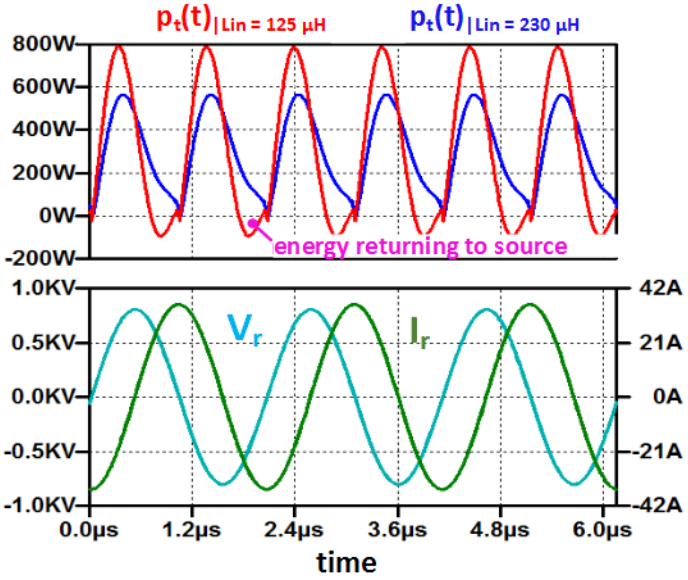


Figure 2-41. Instantaneous power of the resonant tank, $p_t(t)$, for two cases of the input inductance and Q = 50. Red: L_{in} = 125 µH; instantaneous power is negative in marked area, $p_t(t) < 0$, and energy is flowing from the resonant tank back to the source. Blue: L_{in} = 232 µH; instantaneous power is positive, $p_t(t) > 0$, which leads to improved efficiency.

For Amplifier's parameters in Table 2-6, the optimum input inductance value is computed to be $L_{in,opt}$ = 232 μH which is very close to the previously examined L_{in} = 225 μH. Useful is the power loss comparison for amplifiers with L_{in} = 125 μH (Inductor 2 design), and L_{in} = 225 μH (Inductor 3 design). The power loss breakdown is computed with the help of section 2.4.3, and it is shown in Figure 2-42. The power losses are plotted for heavy-load condition where Q = 10, and for light load condition where Q = 50. The heavy-load efficiency (Figure 2-40 a)) and power losses (Figure 2-42) are very close for both Inductor 2 and 3 design-cases. Significant (~1 %) light-load efficiency improvement for the Inductor 3 design is achieved with decrease of $P_{\Delta I}$ related losses (primarily core losses). The efficiency at the light-load cannot be additionally improved much with the increase of either input inductance or core size since for Inductor 3 the fixed losses (P_{fx}) already comprise the most of the total power loss. Thus, (2-99) provides good estimation for maximum input inductance that should be used to design the boost power amplifier since no major improvement can be obtained if the input inductance is increased.

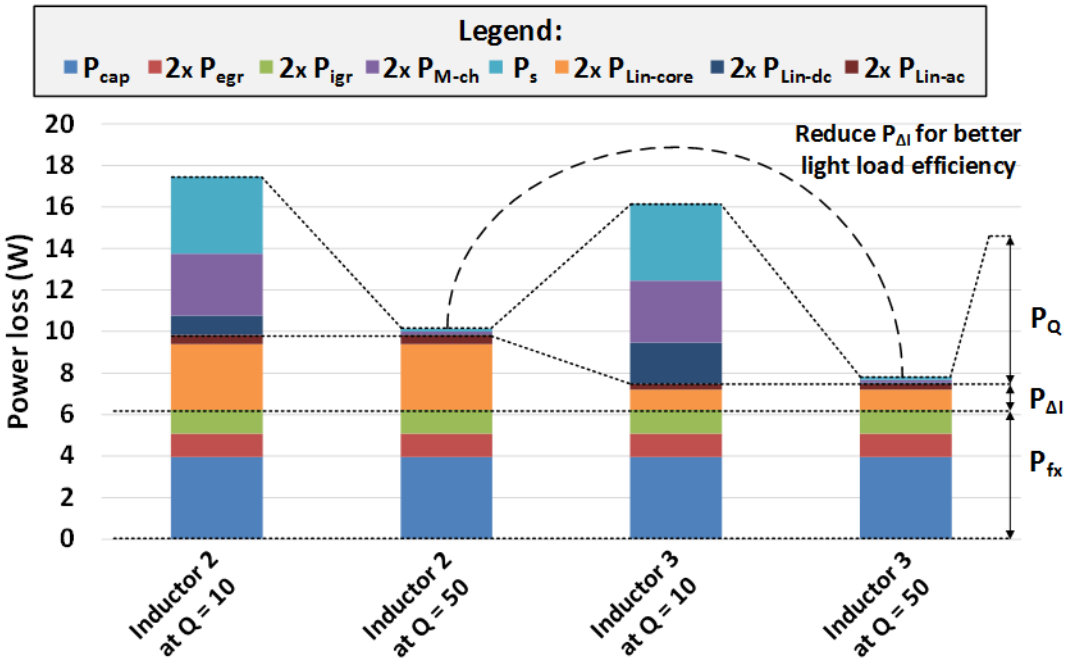
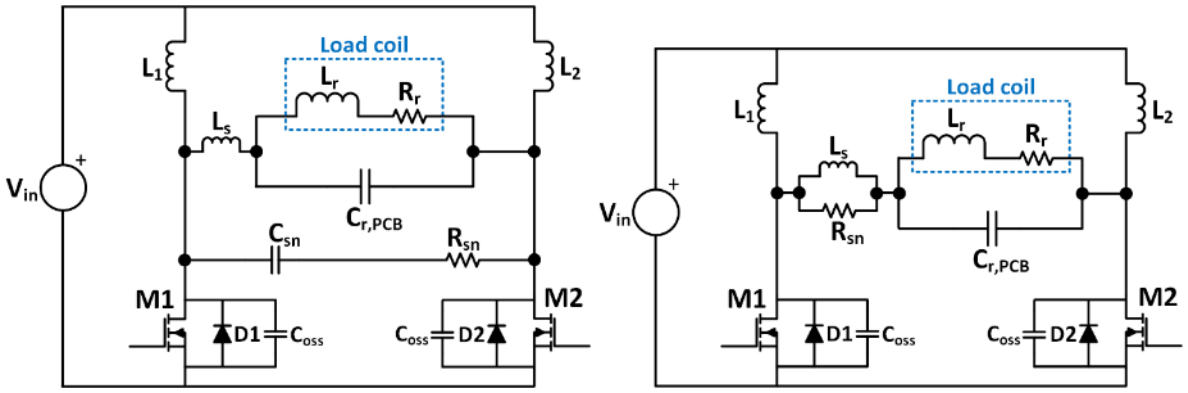


Figure 2-42. Loss breakdown for design-cases: Inductor 2 and Inductor 3. The heavy load represents condition when Q = 10. Light load represents condition when Q = 50. The loss is calculated based on analysis in section 2.4.3.

2.5. Design of Snubber Circuit

Boost amplifier circuit scheme in Figure 2-10 may not be complete if the series inductance with the resonant tank (L_s) takes significantly large values. The inductance L_s may originate from parasitic inductance of the cable that connects the resonant load (tank) and the switching stage. Physical separation of the load and the switching stage that leads to large L_s inductance is not uncommon in applications such as induction heaters [56]. Additionally, inductance L_s may be purposely made large in order to suppress current spikes in the switches during faults. Regardless of the inductance origin, couple hundred of nano-Henries may present between the resonant tank and the switching stage.

The energy stored in the L_s inductor would create oscillatory circuit with the parasitic output capacitor of the switch, C_{oss}. The ringing may be severe, and unlike in the low-voltage applications [67], requires attenuation by implementing a snubber circuit. Two basic configurations are possible [107]: LCR-snubber (Figure 2-43 a)), and LR-snubber (Figure 2-43 b)). The LCR-snubber circuit provides additional degree of freedom since both C_{sn} and R_{sn} are involved in the snubbing process. The LR-snubber may be difficult to implement when L_s originates from the cable connection between load and switching stage. The snubber resistor R_{sn} would then have long leads that can complicate the physical design and create additional design considerations. Additionally, the value of R_{sn} may be too low and comparable to L_s when switches with large C_{oss} is used. Both structures will be considered in implementing the boost amplifier.



(a) **(b)**

Figure 2-43. Common snubber circuits applicable to the boost amplifier: (a) Current LCR-snubber, consisted of L_s, C_{sn} and R_{sn}; (b) Current LR-snubber, consisted of L_s and R_{sn}. Snubber circuit decrease the ringing between L_s and C_{oss} after the switching instance.

The value of inductance L_s can be computed in order to mitigate severe fault conditions. A simple example illustrates the computation: it is assumed that the voltage on the resonant capacitor is 75 V when the fault happens, and the transistor current should not increase more than 6 A for the fault duration of 20 ns. Easy calculation gives:

$$L_s = \frac{V_r}{dI_{M1}/dt} = \frac{75V}{6A/20ns} = 250\,nH \tag{2-100}$$

There are other possibilities to form the design criteria for the inductance L_s calculation, however, in this work the (2-100) and value of 250 nH will be used.

During each switching cycle the L_s inductor would changes its energy approximately by

$$E_{sn-Ls} = \frac{1}{2} L_s \left(2I_{Lm0}\right)^2 = 2L_s I_{Lm0}^2 \tag{2-101}$$

This energy is dissipated on the snubber resistor R_{sn} during each half-cycle of the period. The total power loss due to the inductor-stored energy is then:

$$P_{sn-Ls} = 2E_{sn-Ls} f_{sw} = 4L_s I_{Lm0}^2 f_{sw} \tag{2-102}$$

For the power amplifier with parameters given in Table 2-3, the L_s-related loss is $P_{sn\text{-}Ls}$ = 1 W.

2.5.1. LCR Snubber Structure

The performance LCR snubbber will be investigated first. The snubber capacitor C_{sn} is typically computed to be two or four times larger than the equivalent output capacitance of the transistor, $C_{oss,eq}$ [107]. In the case of circuit in Figure 2-43 a), however, large C_{sn} capacitor would lead to excessive loss. Since inductance L_s and resistor R_{sn} have small impedances, the C_{sn} capacitor will experience full $V_r(t)$ imposed on it. The voltage would impose a large circulating current though C_{sn} and R_{sn}, creating a loss on snubber resistor:

$$P_{sn-c} = \frac{1}{2} R_{sn} \left(\omega C_{sn} V_{rm}\right)^2 \tag{2-103}$$

The total power loss of the snubber is

$$P_{sn} = P_{sn-Ls} + P_{sn-c} \tag{2-104}$$

and it is largely dominated by the circulating current induced loss, $P_{sn\text{-}c}$. Figure 2-44 plots the dependence of the $P_{sn\text{-}c}$ on the snubber resistance for different snubber capacitances. Both C_{sn} and R_{sn} take reasonable values that may be used

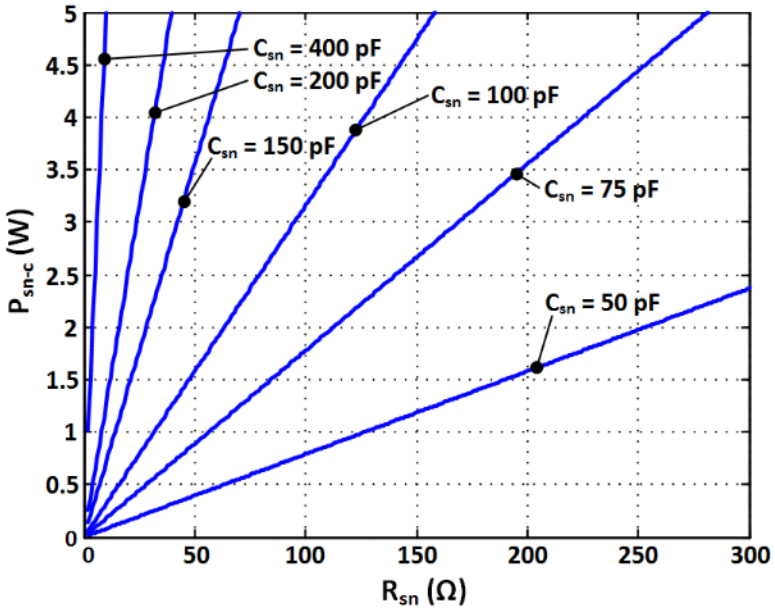


Figure 2-44. Power losses in the snubber resistor as consequence of the circulation current though the C_{sn}-R_{sn} branch at fundamental frequency. The amplitude of the resonant voltage is V_{rm} = 800 V. The power losses P_{sn-c} follow equation (2-103), and they increase rapidly with the increase of snubber resistance R_{sn} for large value of snubber capacitance C_{sn}. Lower values of C_{sn} preferred.

in the actual system. The small values of C_{sn} are preferred, since larger range The output capacitance of the transistor is approximately $C_{oss,eq}$ = 200 pF. The snubber capacitance impacts the computation of the synchronous frequency, thus, the value of the physical capacitor that is put in parallel with the load coil is:

$$C_{r,PCB} = C_r - C_{oss,eq} - C_{sn} \tag{2-105}$$

where C_r is the value of the resonant capacitor, as computed with (2-58).

The equivalent circuit of the snubber (Figure 2-45) is used to study the damping of the oscillations between L_s and C_{oss}. The circuit is derived from Figure 2-10, where transistor M1 is off (substituted with its output capacitance), transistor M2 is on (providing a short circuit connection), capacitor $C_{r,PCB}$ is a negligibly low-impedance at the frequencies where snubber operates (an effective short circuit), and both L1 and L2 are significantly high impedance at the frequencies where snubber operates (an effective open circuit). The circuit does not have sources, but it is energized since at the beginning of the switching cycle the current in the L_s inductor is approximately I_{Lm0}. The snubber

capacitor voltage and the C_{oss} voltage are zero since the switching instance occurs at the zero-crossing of the resonant voltage $V_r(t)$. It should be noted that performance of the C_{sn}-R_{sn} branch is evaluated for the normal operation only (at steady-state and synchronous frequency). At faults the L_s inductance is the main parameter for examination, and for this work it is defined with (2-100).

The circuit in Figure 2-45 is the third order circuit for which is difficult to define a damping ratio. Instead, the frequency characteristic of the equivalent impedance between nodes 1 and 2 ($z_{12}(j\omega)$) is examined. The impedance is equal to

$$z_{12}(j\omega) = (j\omega L_s) \| \left(\frac{1}{j\omega C_{oss}} \right) \| \left(R_{sn} + \frac{1}{j\omega C_{sn}} \right) \tag{2-106}$$

The magnitude of the input impedance $\|z_{12}(j\omega)\|$ is plotted in Figure 2-46 for four different values of the snubber capacitor C_{sn}. Each plot contains a family of five $\|z_{12}(j\omega)\|$ curves (blue and green lines) for different values of snubber resistance. The resonant points for each curve approximate the free-ringing frequency of the snubber circuit, and they are marked as red dots. The dashed U-shaped red line connects the red dots to emphasize a trend: for each C_{sn} there is an optimum snubber resistance R_{sn} for which maximum damping occurs. For the maximum damping case the $\|z_{12}(j\omega)\|$ will have the smallest impedance, and the $\|z_{12}(j\omega)\|$ curve is colored in green.

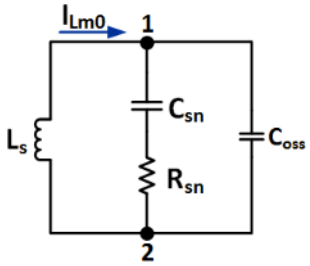


Figure 2-45. Equivalent LCR snubber circuit for the boost amplifier under steady-state and synchronous frequency.

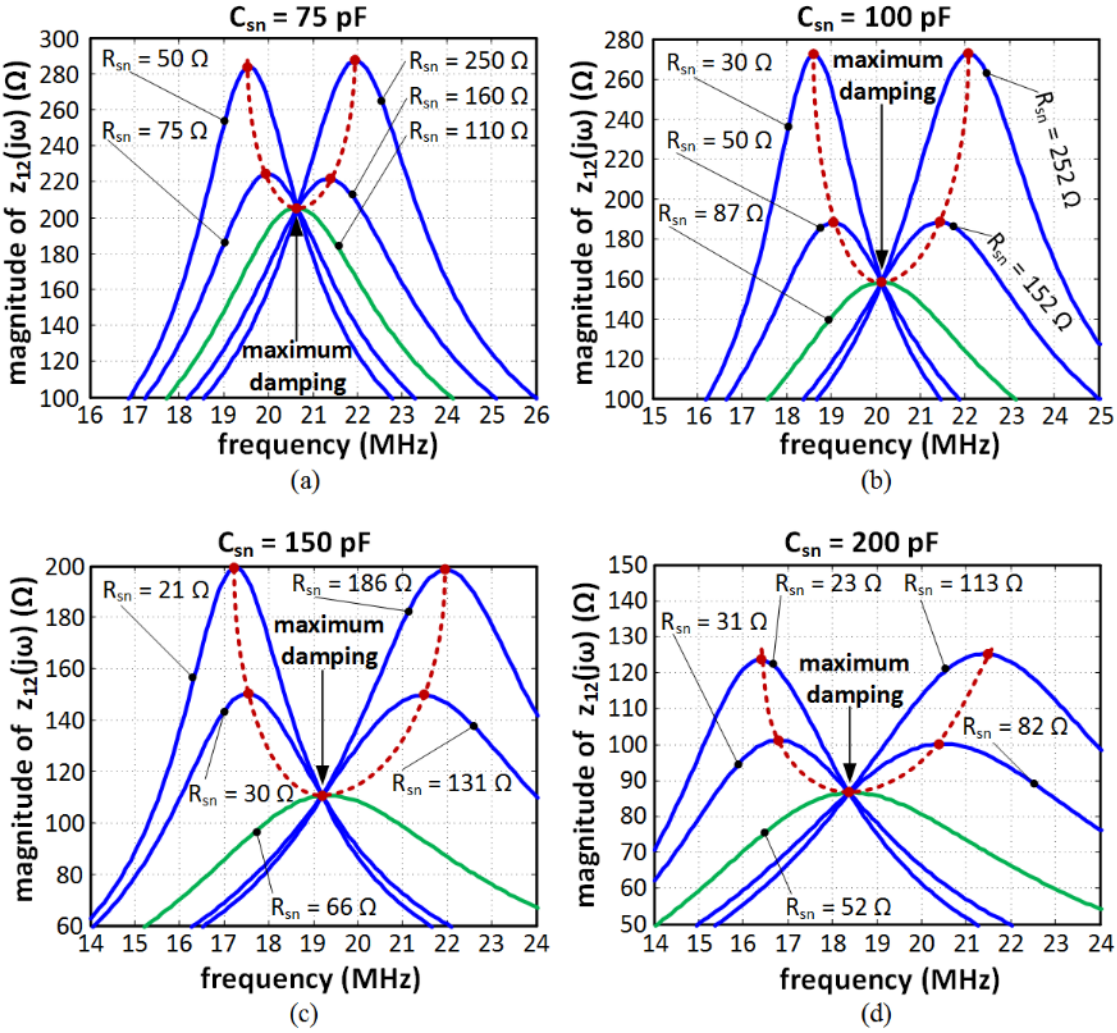


Figure 2-46. The magnitude of snubber impedance $z_{12}(j\omega)$ for four different values of snubber capacitance C_{sn}. Snubber resistance R_{sn} is varied for each of the C_{sn} capacitances. Each $||z_{12}(j\omega)||$ curves (blue or green lines) will have a resonant point (peak) that occurs near the frequency of free oscillation for the snubber circuit in Figure 2-45. These resonant points are marked with red dots, and connected with a red line that forms a U-shaped curve. Maximum damping of the snubber circuit of the occurs for $||z_{12}(j\omega)||$ curve with the smallest resonant peak, which is the curve that crosses the valley point of the red U-shaped curve. This $||z_{12}(j\omega)||$ curve is colored in green. (a) C_{sn} = 75 pF; maximum damping occurs at R_{sn} = 110 Ω. (b) C_{sn} = 100 pF; maximum damping occurs at R_{sn} = 87 Ω. (c) C_{sn} = 150 pF; maximum damping occurs at R_{sn} = 66 Ω. (d) C_{sn} = 200 pF; maximum damping occurs at R_{sn} = 52 Ω.

Few important points can be concluded from Figure 2-46:

- The frequency of free-oscillations decreases with the increase of C_{sn}.
- More damping is possible for larger values of C_{sn}.
- The optimal R_{sn} for maximal damping reduces with the increase of C_{sn}.
- The snubber loss tend to increase with C_{sn}, as indicated by (2-103), (2-104), and Figure 2-46.

Figure 2-47 is generated in order to properly access the trade-offs between the snubber power loss (Figure 2-44) and snubber damping performance (Figure 2-46). A family of blue curves represent a dependence of snubber's impedance $||z_{12}||$ on snubber resistance R_{sn} for fixed snubber capacitor C_{sn}. Six curves are presented: from C_{sn} = 50 pF where damping potential is limited to C_{sn} = 400 pF where damping can be large, but too lossy. Orange dots are points with maximum damping for given C_{sn}.

The red lines represent the dependence of snubber's impedance on snubber resistance for given $P_{sn\text{-}c}$ loss. Four curves are given. The damping potential increases two-fold when $P_{sn\text{-}c}$ is increased from 1.5 W to 4 W Green dots represent points where maximum damping can be achieved for given $P_{sn\text{-}c}$ loss.

It is not good idea to design C_{sn} and R_{sn} to match an orange point in Figure 2-47, since for given power loss there is another solution that can provide more damping. For example, there is an orange point on the C_{sn} = 75 pF curve. The snubber resistance is R_{sn} = 110 Ω. The power loss due to fundamental frequency circulating current is $P_{sn\text{-}c}$ = 2 W. There is a green point on the $P_{sn\text{-}c}$ = 2 W curve, near its intersection with C_{sn} = 150 pF. The snubber resistance is R_{sn} = 28 Ω. The snubber impedance is lower for the green than for the orange point, and therefore the damping of the oscillations will be higher.

Also, the examination of C_{sn} = 150 pF curve leads to a similar conclusion. The orange point at R_{sn} = 66 Ω will have slightly larger damping performance than two green points at R_{sn} = 28 Ω and R_{sn} = 34 Ω. The power losses are, however, doubled.

Thus, the C_{sn} and R_{sn} should be designed using green points on red $P_{sn\text{-}c}$ curve. For example, when $P_{sn\text{-}c}$ = 2 W the optimum snubber capacitance and resistance are C_{sn} = 150 pF and R_{sn} = 28 Ω. When $P_{sn\text{-}c}$ = 2.5 W, the optimum snubber capacitance and resistance are C_{sn} = 150 pF and R_{sn} = 34 Ω.

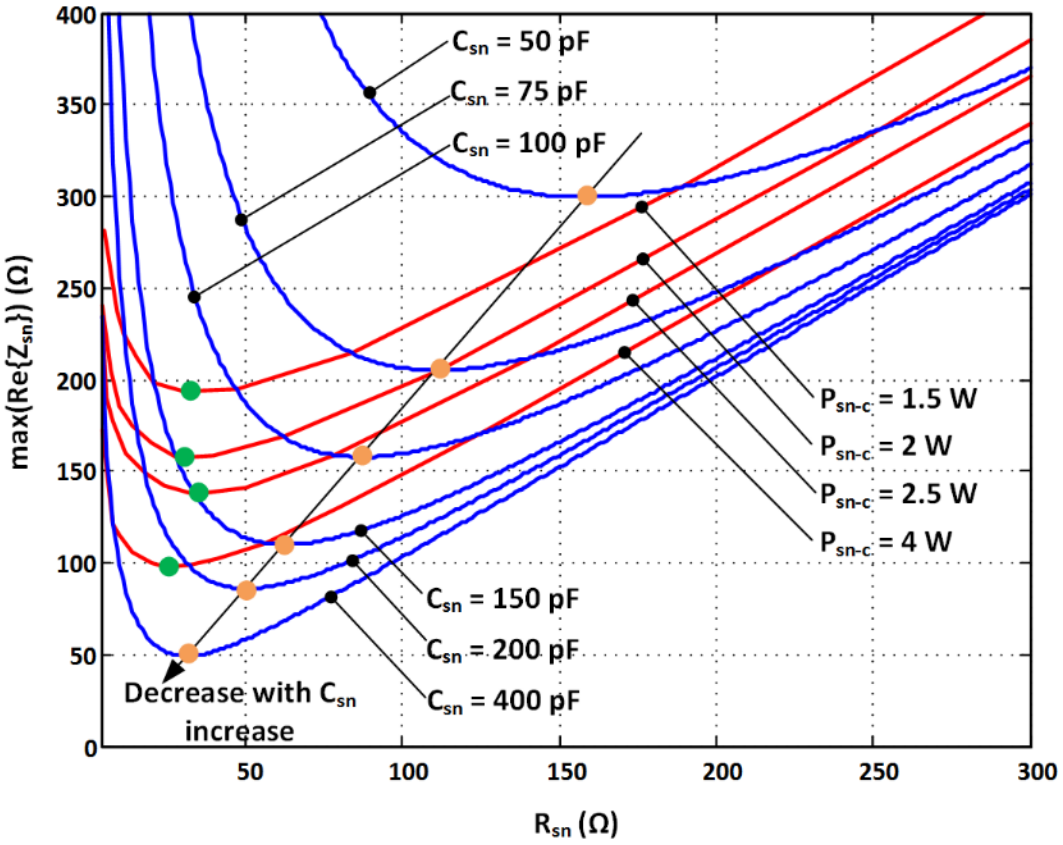


Figure 2-47. Dependence of snubber circuit's impedance on snubber resistance. Blue lines represent fixed snubber capacitance C_{sn} case. Orange dots represent points of maximum damping for given C_{sn}. Red lines represent fixed $P_{sn\text{-}c}$ loss. Green dots represent points of maximum damping for given $P_{sn\text{-}c}$ loss.

A set of six simulation examples is run to illustrate the performance of snubber circuits. The examples are based on the boost amplifier in Figure 2-43 a), with circuit parameters given in Table 2-3.The inductance in series with the resonant tank is L_s = 250 nH, except for the first simulation example where L_s is zero (no snubber implemented). The C_{sn}, and R_{sn} are taking different values to show their influence on oscillation's damping. The on-board resonant capacitor $C_{r,PCB}$ is computed using (2-105) for each simulation example in order to ensure synchronous operation at f_{sw} = 500 kHz.

First simulation example demonstrates the steady-state operation of boost amplifier with no snubber implemented. The simulation waveforms of the selected variables is shown in Figure 2-48 a). The waveforms are clear from current spikes and ringing oscillations due to synchronous frequency operation. However, as discussed before, in the case of faults the amplifier may be damaged due to current spikes.

Second simulation example utilizes L_{sn} = 250 nH in series with the resonant tank. No C_{sn} and R_{sn} are placed in the system. Heavy ringing is present in all simulated waveforms shown in Figure 2-48 b) due to energy oscillation between L_{sn} and C_{oss}. Such ringing is unacceptable in practical systems, and it has to be attenuated with proper snubber circuit.

Third simulation example utilizes L_{sn} = 250 nH, with snubber design using $P_{sn\text{-}c}$ = 2 W curve in Figure 2-47. Values of C_{sn} = 75 pF and R_{sn} = 110 Ω are selected. The simulation waveforms of selected variables are shown in Figure 2-49 a). The oscillations are well controlled, and the resonant tank's current does not see excessive overshoot.

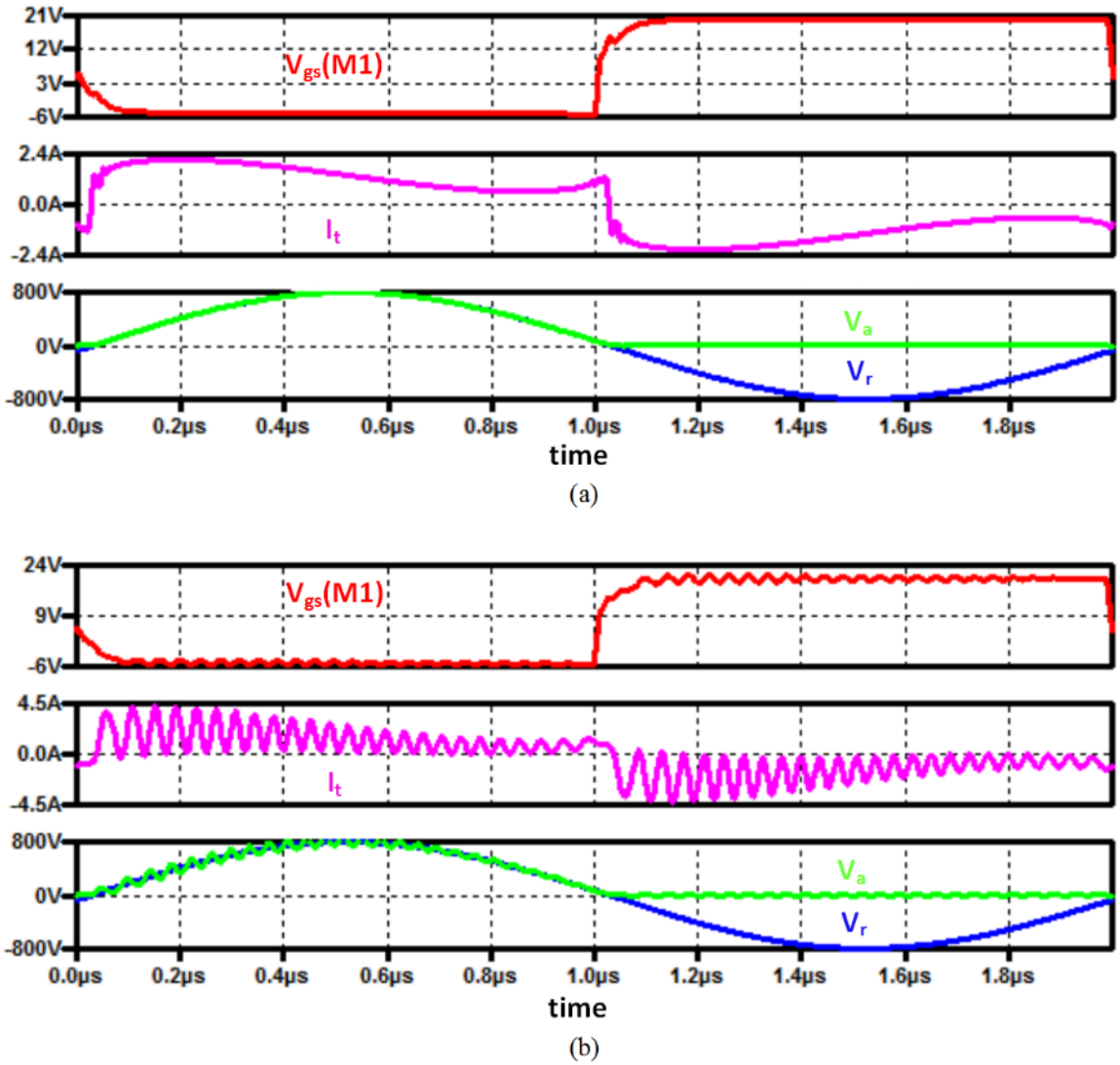


Figure 2-48. Simulated boost amplifier: (a) no snubber implemented (b) L_s = 250 nH and no C_{sn} and R_{sn} placed in the system.

In fourth simulation example the parameters of the snubber are slightly changed. The $P_{sn\text{-}c}$-loss is kept to 2 W, while more damping is obtained by selecting C_{sn} = 150 pF and R_{sn} = 28 Ω. The simulation waveforms are given with Figure 2-49 b). When compared with Figure 2-49 a), the oscillations are somewhat more damped. The peak tank's current is reduced as well.

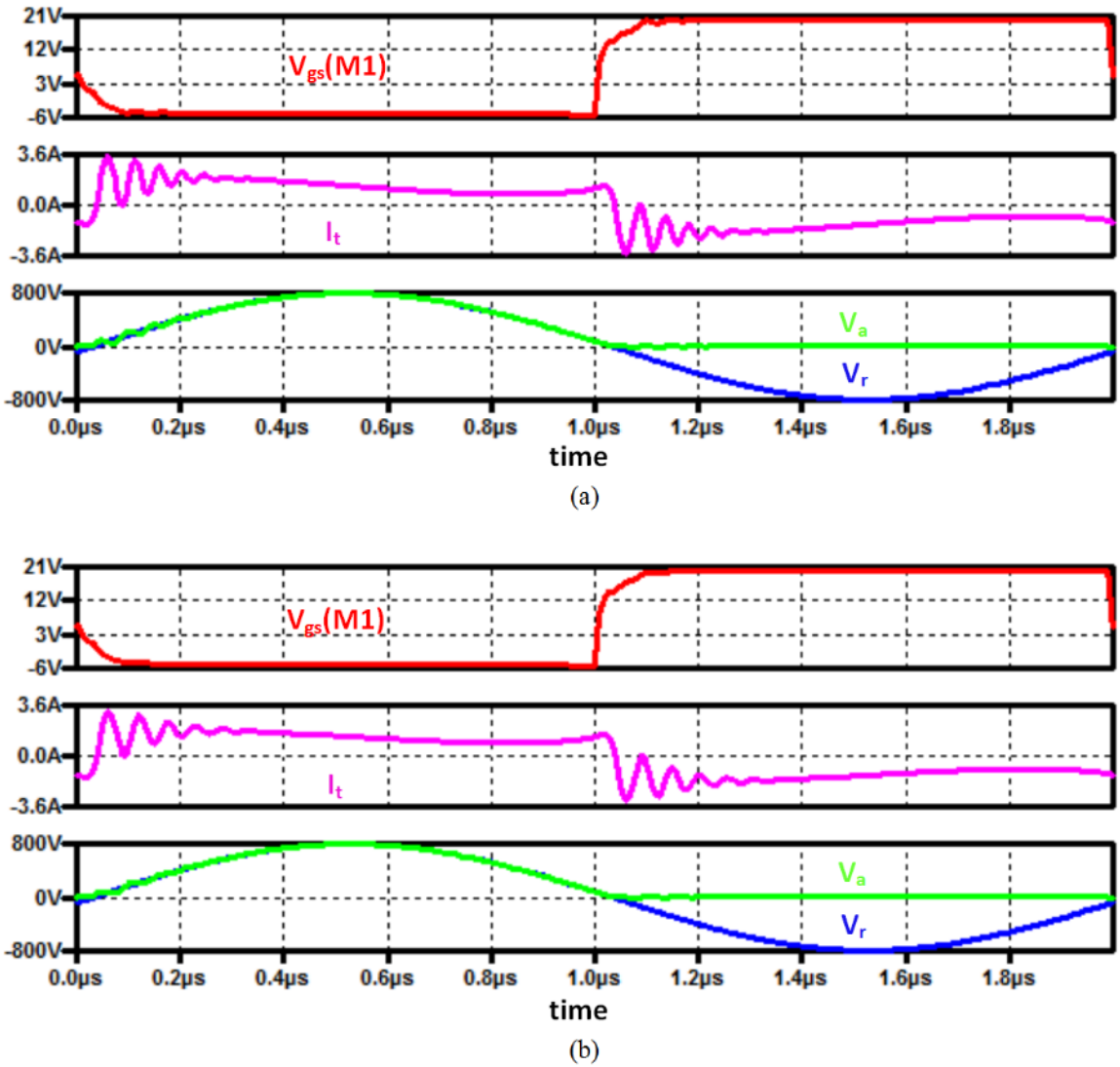


Figure 2-49. Simulated boost amplifier with a LCR snubber circuit with fixed loss of $P_{sn\text{-}c}$ = 2 W. (a) L_s = 250 nH, C_{sn} = 75 pF and R_{sn} = 110 Ω. (b) L_s = 250 nH, C_{sn} = 150 pF and R_{sn} = 28 Ω.

Fifth simulation example bring more damping performance at the expense of the snubber loss. The P_{sn-c} is set to 2.5 W, while R_{sn} = 34 Ω for C_{sn} = 150 pF. The simulation waveforms are given in Figure 2-50 a). The oscillations are reduced when compared with the case in Figure 2-49 b).

Final, and sixth simulation example further damps oscillations at the expense of snubber loss. Fixed snuber loss is P_{sn-c} = 4 W now, the C_{sn} = 150 pF and R_{sn} = 66 Ω. If it is necessary to meet EMI/EMC requirements, the snubber circuit with more damping can be implemented, as indicated by Figure 2-47. Additional loss would have to be sacrificed.

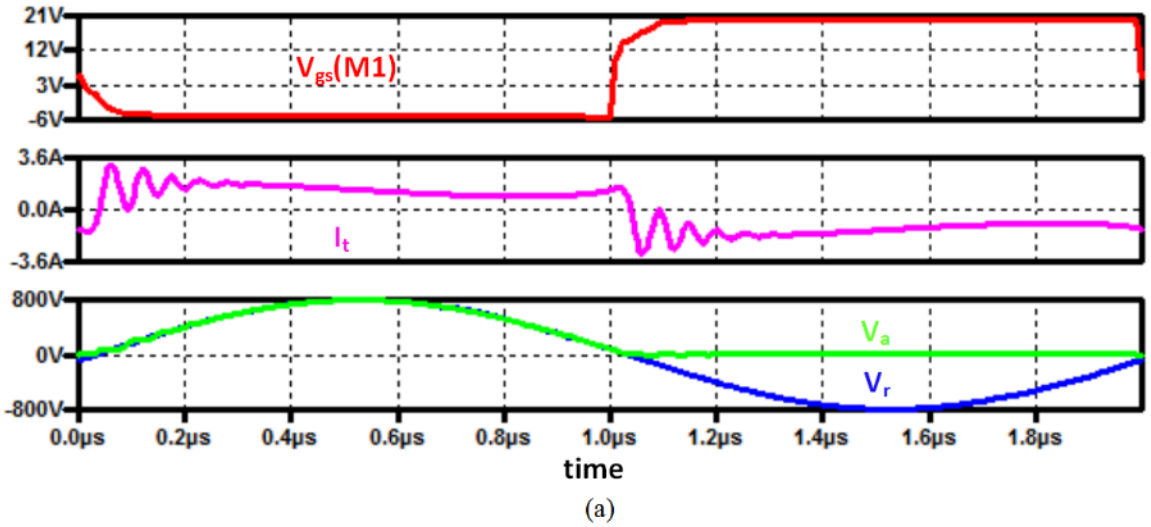


Figure 2-50. Simulated boost amplifier with a LCR snubber circuit for: (a) L_s = 250 nH, C_{sn} = 150 pF and R_{sn} = 34 Ω. (b) L_s = 250 nH, C_{sn} = 150 pF and R_{sn} = 66 Ω.

2.5.2. LR Snubber Structure

Equivalent circuit of LR snubber structure is simple parallel LCR tank consisted of series inductor Ls, transistor's output capacitor $C_{oss,eq}$, and snubber resistor R_{sn}, as shown in Figure 2-51. The ringing oscillation frequency is approximately

$$f_{osc} = \frac{1}{2\pi\sqrt{L_s C_{oss}}} \tag{2-107}$$

The quality factor of snubber circuit is

$$Q_{sn} = R_{sn}\sqrt{\frac{C_{oss,eq}}{L_s}} \tag{2-108}$$

In designing the snubber circuit the impedance of series inductor should be much smaller than the snubber resistance

$$\omega L_s << R_{sn} \tag{2-109}$$

so the resonant tank's input current flows majorly though the inductor. LR snubber structure is advantageous over the LCR structure since it does not have additional loss components except for one in (2-102). Additionally, resistance R_{sn} can be chosen with larger degree of freedom.

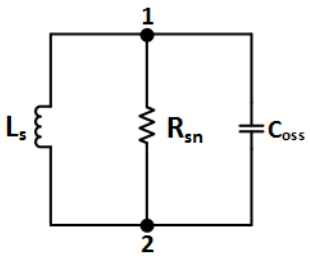


Figure 2-51. Equivalent LR snubber circuit for the boost amplifier at the steady-state and synchronous frequency.

2.5.3. Snubber Loss vs. Series Diode Loss

The comparison of the loss performance for the current snubber and the series diode in the switch configuration are important when both are an option for the implementation of the boost amplifier. The diode loss P_D is equal to

$$P_D = 2I_{Lm0}V_F \tag{2-110}$$

where V_F is the forward voltage drop of the series diode. For comparisons, the SiC C4D20120A diode is considered since it has the same current rating as CMF20120 SiC MOSFET. Figure 2-52 shows comparison of the snubber losses. Series diode has high loss when the current is small in the system. As the current and power increases, the snubber loss becomes higher since both operating frequency and power are high. If the operating frequency is low (reduced to 100 kHz in this example), the snubber loss is considerably lower than the series diode loss. Thus, the series diode is advantageous when the safety must be guaranteed at all times, and for high power, high frequency systems. Snubber structure is cheaper, does not need passive cooling as in the diode case, and may have better loss performance. However, snubber does not provide inherently safe operation and should be seen as the safety feature when the diode is not present rather as the direct replacement of the diode. For the specifications that are used in this work, it is computed that snubber creates approximately 1.5-3 times less loss than the series diode.

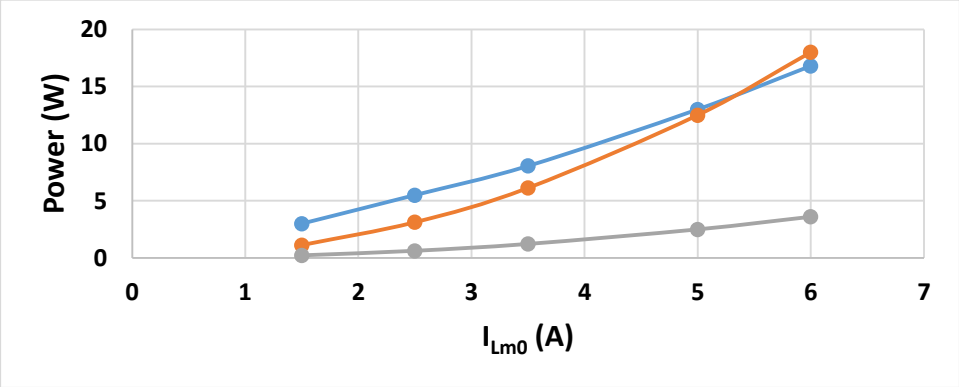


Figure 2-52. Comparison between calculated losses for the series diode in the switch configuration (blue), LR snubber at f_{sw} = 500 kHz (orange), and LR snubber at f_{sw} = 100 kHz (gray).

2.6. Design & Implementation of Boost Amplifier

2.6.1. Design Goals & Specifications

The theoretical operation of the boost amplifier was derived in the previous sections. The design equations are systematized in this section, forming a procedure to make an amplifier design easier. A design example for the boost amplifier circuit in Figure 2-43 a) is given to demonstrate its performance.

The amplifier's is designed for frequency of operation not larger than f_{sw} = 500 kHz, with reactive power of PQ ≥ 14 kVA in the load, and loaded quality-factor in the range $10 \leq Q \leq 50$. The input voltage V_{in} should be limited less than 300 V, with preferred voltage level of V_{in} = 254.64 V. The motivation to make the input voltage higher is to push the power transistors to their maximum voltage-blocking limits, which gives larger output power. The amplifier will be designed for nominal input voltage V_{in} = 254.64 V, loaded quality-factor of Q_{nom} = 20, and load's reactive power of PQ = 14 kVA. If possible, it will be attempted in the hardware tests to increase the input voltage up to V_{in} = 300 V with the reactive power increase to PQ = 20 kVA.

The amplifier is designed for input inductance of $L_{in} = L_{in,opt}$ = 232 μH (see section 2.4.6 for computation) for the optimum performance. The design is repeated and additional test are done for low value of input inductance (L_{in} = 125 μH) for improved bandwidth. The specifications are similar to the ones in section 2.2., and are summarized in the Table 2-11. The columns on left give the ranges of variables, so there is some liberty to adjust parameters for easiness of practical implementation. The columns on the right give nominal values of variables that are used to initiate the design procedure.

Table 2-11. Boost inverter specifications for the circuit in Figure 2-43 a).

Ranges of variables		Nominal values of variables	
V_{in} (V)	< 300	V_{in} (V)	254.64 V
f_{sw} (kHz) @ Q_{nom}	< 500	f_{sw} (kHz)	500 kHz
PQ (kVA)	≥ 14	PQ (kVA)	14
Q @ f_{sw}	10 - 50	Q_{nom} @ f_{sw}	20
L_{in} (μH)	125 - 232	L_{in} (μH)	232

2.6.2. Design Procedure for Boost Amplifier

Orderly and step-by step procedure is made to assist circuit design. A design example is given for the boost amplifier specifications in Table 2-11. Nominal values of PQ = 14 kVA and Q_{nom} = 20 for the switching frequency of 500 kHz and input voltage V_{in} = 254.64 V are used to initiate design.

The Step 1 of the design procedure is the computation of the load parameters. From (2-20), the nominal active power (PA_{nom}) is computed, as shown in Table 2-12. The load inductance, nominal, maximum, and minimum load resistance are computed using (2-5), and (2-35). The reconfigurable inductor-resistor network is constructed to emulate the inductive and resistive behavior of the load coil. Four different reconfigurations are possible, and they are described in Section 2.6.3.1 in detail. Depending on the used reconfiguration, the load inductance varies from L_r = 7.22 μH to L_r = 7.34 μH with the loaded Q-factor in the range Q = 13-40.

Once the load parameters are known, the input inductance is computed or selected in Step 2. The optimal inductance is obtained by using (2-99). Two physical inductors are built using PQ3220 high-frequency N49 material with the inductance of L_{in} = 229 μH. The detailed inductor design procedure is given in section 2.4.4, while inductor implementation is presented in section 2.6.3.2.

In Step 3, the resonant capacitance is computed by using (4-2) and (2-58). Resonant capacitance comprises of physical capacitor placed in parallel with the resonant tank, $C_{r,PCB}$, equivalent, linear, output capacitance of the power transistor, $C_{oss,eq}$, and the snubber capacitor, C_{sn}, as indicated by (2-105). Thus, before computing $C_{r,PCB}$ the power transistor should be selected and snubber circuit designed.

The power transistor is selected in Step 4. The silicon-carbide MOSFET (Cree's CMF20120D) is selected for its excellent performance at high operating frequencies over silicon transistors [93]. The maximum voltage and current stress are computed and tabulated in Table 2-12. The CMF20120D satisfies maximum voltage/current requirements.

Snubber circuit is designed in Step 5. The power dissipation of the snubber is chosen to be small in order to keep efficiency high, so the P_{sn-c} = 2 W is selected. The inductance in series with the resonant tank (L_s) is computed using (2-100). Snubber capacitor and resistor are chosen to confirm the discussion in section 2.5. The snubber resistor is implemented as a parallel connection of 20 identical surface mount resistors to limit the temperature increase.

Table 2-12. Step-by-step procedure to design boost amplifier.

Step 1: Calculation of load parameters	$PA_{nom} = \frac{PQ}{Q_{nom}} = 700\,W$ $R_{r,nom} = \frac{\pi^2}{2}\frac{V_{in}^2}{PA_{nom}\left(1+Q_{nom}^2\right)} = 1.14\Omega$ $L_r = \frac{Q_{nom}R_{r,nom}}{\omega} = 7.28\mu H$ where $\omega = 2\pi \cdot 500kHz$ $R_{r,\max} = \frac{\omega L_r}{Q_{\min}} = 2.28\Omega$ and $R_{r,\min} = \frac{\omega L_r}{Q_{\max}} = 0.46\Omega$ Reconfigurable load constructed with L_r = 7.22-7.34 μH and Q = 13-40
Step 2: Input Inductance calculation	$L_{in,opt} = \frac{2}{\pi}\frac{R_{r,\min}\left(1+Q_{\max}^2\right)}{\omega} = 232\mu H$ Two inductors of L_{in} = 229 μH constructed using N49, PQ3220 cores
Step 3: Resonant capacitor calculation	$C_r = \frac{1}{\omega^2 L_r}\frac{1}{1+\frac{1}{Q^2}} + \frac{1}{\omega^2 L_{in-eq}} = 14.15nF$, where $L_{in-eq} = \frac{2L_{in}}{1+\frac{16}{9\pi^2}}$
Step 4: Switch selection	SiC MOSFET CMF20120D selected $V_{\max} = V_{rm} = \pi V_{in} = 800V$ $I_{\max} = 2I_{Lm0} + \omega C_{oss,eq}V_{rm} = 6.2A$ $C_{oss,eq} = 195pF$
Step 5: Snubber computation	$P_{sn-c} = 2W$ is selected for low loss. $L_s = 250nH$, $C_{sn} = 75pF$, and $R_{sn} = 100\Omega$. L_s is air-core inductor, implemented using 20 AWG magnet wire. C_{sn} consists of two ceramic capacitors F151K25Y5RN63J5R in series. Twenty 2 kΩ RCL12252K00FKEG resistors in parallel selected for R_{sn} implementation.
Step 6: On-board capacitor calculation	$C_{r,PCB} = C_r - C_{oss,eq} - C_{sn} = 13.88nF$ $C_{r,PCB}$ implemented as fifteen C1825C102JGGACTU 0.97 nF capacitors for total $C_{r,PCB}$ = 14.55 nF.
Step 7: Re-calculate switching frequency	$f_{sw} = \frac{1}{2\pi}\sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2}$ where $L_q = L_r \parallel L_{in-eq}$ f_{sw} = 483-490 kHz for different loads

The on-board resonant capacitor $C_{r,PCB}$ is computed in Step 6. The $C_{r,PCB}$ = 13.88 nF is obtained. A parallel configuration of identical ceramic COG/NPO capacitors is used in order to make the implementation simpler. The COG/NPO technology is used for the capacitance stability with applied voltage and temperature. The C1825C102JGGACTU, 1 nF capacitor, is selected. The actual capacitance of each capacitor has to be measured due to component tolerances. The mean measured value is C_{mean} = 0.97 nF per capacitor. Fifteen parallel capacitors for total capacitance of $C_{r,PCB}$ = 14.55 nF is chosen to keep the switching frequency of the amplifier below 500 kHz.

In Step 7, the switching frequency is recomputed using (2-58) to adjust for the component selections in Steps 1-6. The range of frequencies is obtained since for each load configuration there is specific synchronous frequency that the switching frequency follows.

Similarly, the designed procedure in Table 2-11 is followed for the boost amplifier design with reduced value of input inductance. The difference is that in Step 4 the computation of L_{in} is simply substituted with desired input inductance L_{in} = 125 µH. The obtained circuit parameters for the boost amplifier implementation are summarized in Table 2-13.

Table 2-13. Summarized parameters for implementation of boost amplifier.

V_{in} (V)	L_r (µH)	R_r (Ω)	L_{in} (µH)	Transistor
254.64 V	7.22-7.34	0.57-1.96	125-229	CMF20120D MOSFET
L_s (nH)	C_{sn} (pF)	R_{sn} (Ω)	C_{PCB} (nF)	f_{sw}(kHz)
250	75	100	14.55	483.5-489.5

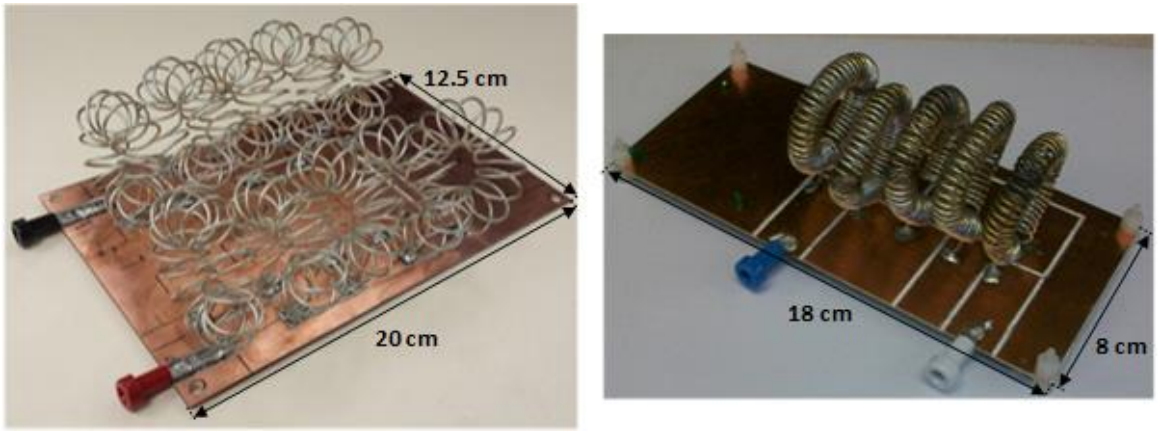
2.6.3. Implementation of Boost Amplifier

The details on implementation of the boost amplifier are described in this section. The design and construction of the load, input inductors, and the gate driver are explained with greater detail. The printed-circuit-board layout and the thermal are described in sufficient detail to ensure the reconstruction of the implemented amplifier. Finally, component list and the photo of the amplifier are given.

2.6.3.1. Implementation of the Inductive Load Coil

The boost amplifier can drive a set of different inductive loads: induction heating/welding/cooking coil, antenna, or primary coil of wireless-power-transfer system. In order to emulate behavior of the inductive load during power

tests, a pair of wire-wound set of coils is designed. The first load, labeled as Load-1, contains a set of ten individual coils placed in series. Each coil contains 14 turns with 1.6 cm diameter. The spacing between the turns is sparse, leading to coil's quality-factor of Q = 40 at frequencies around 500 kHz. The inductance of the coil is L_{r-1} = 7.22 μH. Second load coil, labeled as Load-2, contains a set of five individual placed in series. Each coil contains 48 turns with 0.8 cm diameter. The spacing between the coils is dense, increasing proximity effect losses. The resultant quality-factor is Q = 28 at around 500 kHz, with inductance of L_{r-2} = 7.28 μH. The two constructed load coils are presented in Figure 2-53. To increase the number of possible load configurations to four, a 1 Ω, low inductance, high power resistor (TA2K0PH1R00KE) can be placed in series with each of the load coils. Table 2-14 lists all possible load configurations that are used in amplifier power tests.



(a) **(b)**

Figure 2-53. Inductive load emulators: (a) Load 1 with Q = 40; (b) Load 2 with Q = 28. Inductive loads can be placed in series with 1 Ω resistor to obtain Q = 12 and Q = 14 loads.

Table 2-14. Possible load configuration. Individual coils are labeled as Load-1 and Load-2. Two new load configurations are created, labeled as Load-3 and Load-4, when 1 Ω resistor is placed in series with each of individual coils.

	Q-factor	Inductance (μH)	Resistance (Ω)
Load-1	40	7.22	0.57
Load-2	28	7.28	0.78
Load-3 = Load-1 + 1 Ω	14	7.3	1.59
Load-4 = Load-2 + 1 Ω	12	7.34	1.86

2.6.3.2. Implementation of Input Inductors

A pair of Inductors 2 are built to test the boost amplifier for large bandwidth and high efficiency. Also, a pair of Inductors 3 are built to test boost amplifier for high light load efficiency. The inductors are designed with the help of section 2.4.4 with some modifications: the bobbin is not used due availability, and the air gap is present on all three legs of magnetic PQ core for fast prototyping (gapped cores were not available). For both Inductor 2 and 3 the PQ3220 cores with N49 material are used. The air-gap in both designs is 0.675 mm, which is the thickness of ceramic spacer. Kapton tape and metal clip are used to ensure mechanical stability of the inductor structures. Inductor 2's wire winding has 25, while Inductor 3's has 34 turns. The winding is split into two halves, and each half is wound around corresponding half of the PQ3220 core. The pair of Inductors 3 is shown in Figure 2-54.

Inductors 2 and 3 are implemented and characterized using Agilent 4294A impedance analyzer with 16047e adapter. Inductance, dc and ac series resistance, and parallel capacitance are extracted from characterization. They are tabulated in Table 2-15 and Table 2-16 for Inductor 2 and Inductor 3 respectively. Section 2.7 examines boost amplifier's performance for both Inductor 2 and 3 implementations.

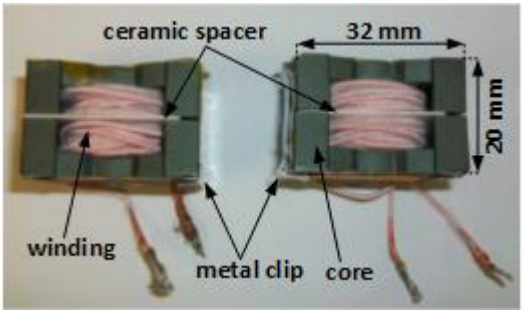


Figure 2-54. A pair of Inductors 3.

Table 2-15. Summary of Inductor 2 implementation parameters.

Core Material	N49	Wire Size (AWG)	18
Core Size	PQ 3220	Litz/stranded wire	100/38
Number of Turns	25	Air gap	0.675 mm
Total Inductance	125 µH	R_{dc}	60 mΩ
Parallel capacitance	4 pF	R_{ac}	2 Ω

Table 2-16. Summary of Inductor 3 implementation parameters.

Core Material	N49	Wire Size (AWG)	22
Core Size	PQ 3220	Litz/stranded wire	160/44
Number of Turns	34	Air gap	0.675 mm
Total Inductance	229 μH	R_{dc}	80 mΩ
Parallel capacitance	6 pF	R_{ac}	4 Ω

2.6.3.3. Gate driver circuit implementation

The design of gate driver circuit is very important to successfully run power electronic systems since high dv/dt or di/dt can inject noise to the driver and produce spurious switching of MOSFETs. In the case of boost amplifier, high di/dt the noise can be injected due to current spikes to the gate driver via parasitic inductor of the source terminal of MOSFET (see sections 2.2.4 and 2.2.5). The gate-source voltage may rise to the levels outside safe operating area of the MOSFET. Additionally, the spurious switching can occur. For that reason a gate driver topology with negative turn-off voltage is selected. Negative voltage is created with the help of isolated power supply and simple voltage reference circuit utilizing a zener diode (Figure 2-55 a)). The power for the gate driver is generated with bench power supply (HP E3631A) that outputs 24 V. The floating 24 V is obtained with the use of isolated power supply (XP IU2424SA). Bulk capacitor C1 provides energy storage if the power amplifier is run in the pulsed (burst) mode. Common mode choke CH1 is part of standard drivers for MOSFETs, however, it is not essential in case of boost amplifier since both MOSFETs are ground referenced. Resistor R1 provides damping (minimum loading) for isolated power supply. The series combination of resistor R2 and zener diode D1 splits the 24 V output of the power supply to positive +19.3 V and negative -4.7 V voltage levels that are used to drive power MOSFETs.

Another important feature for the gate driver circuit topology is simplicity. Figure 2-55 b) shows the propagation of the driving PWM signal from the waveform generator, through the standard signal isolator to the gate driver chip (IXDN630YI). The gate driver chip converts logic-level to the +19.3 V/-4.7 V level signal. The series 5 Ω gate resistor R_{egr} is placed between the MOSFET and gate driver chip to provide damping. More importantly, low impedance connection between the gate terminal of MOSFET and the gate driver chip helps to suppress the spiking of the gate-source voltage (V_{gs}) due to current spikes. Resistor R3 is placed between gate and source terminals of MOSFET for

protection. It will clamp the V_{gs} voltage to zero if the gate-driver's output is at high-impedance state. The major components in the gate driver circuit design are listed in Table 2-17.

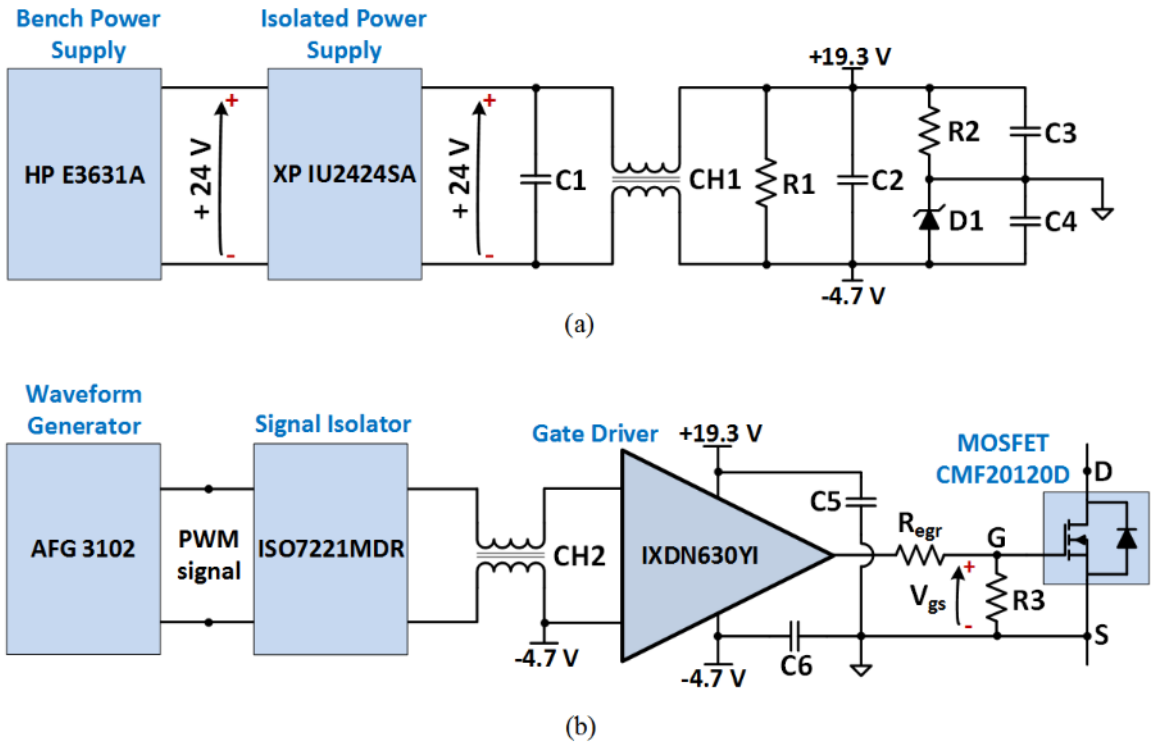


Figure 2-55. (a) Gate driver power supply with +19.3 V for MOSFET turn-on and -4.7 V negative voltage for MOSFET turn-off. Negative voltage generation is obtain using a 4.7 V Zener diode D1. Bench power supply generates power for the gate driver, while isolated power supply provides good isolation of the gate driver; (b) PWM signal to control power MOSFETs is created using a waveform generator. The signal isolation is obtain with digital isolator ISO7221MDR. High-speed gate driver chip IXDN630YI is supplied with +19.3 V/-4.7 V in order to drive the MOSFET with ~ +20 V turn-on pulse and ~ -5V negative turn-off pulse. Both ground pins for signal isolator and gate driver chips is connected to -4.7 V node. Signal isolator is powered with common ground node and -4.7 V node.

Table 2-17. List of components in the gate driver circuit implementation. Components correspond to the gate driver circuit schematics in Figure 2-55.

Symbol	Description	Value	Part Number
M1-M2	Power MOSFETs	1200 V/20 A	CMF20120D
-	Gate driver chip	30 A max current	IXDN630YI
	Signal isolator chip	2 channel	ISO7221MDR
-	Isolated power supply for gate driver	+24 V input/+ 24 V output	XP IU2424SA
CH1	Common mode choke	900 Ω/2 A	ACM4520-901-2P-T000
CH2	Common mode choke	600 Ω/0.2 A	EXC-24CN601X
D1	Zener diode	4.7 V	BZT52C4V7-13-F
R1, R3	Chip resistor	20 kΩ	ERJ-6GEYJ203V
R2	Chip resistor	1 kΩ	RNCP1206FTD1K00
R_{egr}	Chip resistor	5 Ω	RHC2512FT4R99

2.6.3.4. Other Considerations and List of Major Components in the Amplifier's Implementation

The PCB for the boost amplifier is 16 cm long and 6.35 cm wide. The gate driver circuit, power switching MOSFETs, input inductors, snubber circuit, series inductor with the resonant tank, and the on-board resonant capacitors are placed on the PCB. The load coil is placed away from the PCB, with the impedance of connection cables considered as a part of the load for easiness of implementation. The component layout and conductor routing are extremely important in the successful power amplifier design. For that reason, the PCB is sectioned for placement of above-mentioned components. The amplifier's switching stage is placed in the middle of the PCB and has the gate driver circuit on one side and the power processing section (input inductors, snubber circuit, and resonant tank) on the oposite side. With such placement the logic inputs gating signals, and gate drivers are separated from the power processing section, which reduces the noise injection to the gate driver and spurious switching. Kelvin connection [108] is used to interface the gate driver circuit and the power MOSFETs to reduce the common-source parasitic inductance of the MOSFET and related issues. The power processing section is routed so each of input inductors, snubber circuit, and the resonant tank has unique conduction paths leading to the MOSFET nodes, minimizing noise generation.

The power transistors are cooled using an 11 cm x 5.6 cm x 2 cm aluminum heat sink attached to two 10.3 W fans. The heat sink has 11 fins, which are 0.2 cm wide and 1.5 cm long. The thermal system is sufficient to keep temperature increase of transistor junctions is low since only few to several watts of loss on the power devices is expected. The component list used in the boost amplifier design and implementation is given the Table 2-18. The implemented amplifier is shown in Figure 2-56.

Table 2-18. List of major components in the implementation of the power stage of the boost amplifier.

Symbol	Description	Value	Part Number
M1-M2	Power MOSFETs	1200 V/20 A	CMF20120D
L1, L2	Input inductor ferrite cores	PQ3220/N49	B65879A0000R049
$C_{r,PCB}$	COG/NPO ceramic capacitor	1 nF, 2 kV	C1825C102JGGACTU
C_{sn}	Through hole ceramic capacitor (two in series to form C_{sn})	150 pF, 1 kV	F151K25Y5RN63J5R
R_{sn}	SMD resistor	2 kΩ	RCL12252K00FKEG
R_r	Damping resistor for inductive load	1 Ω	TA2K0PH1R00KE
Fans	Fans to cool heat sink	24 V, 10.3 W	1939K17

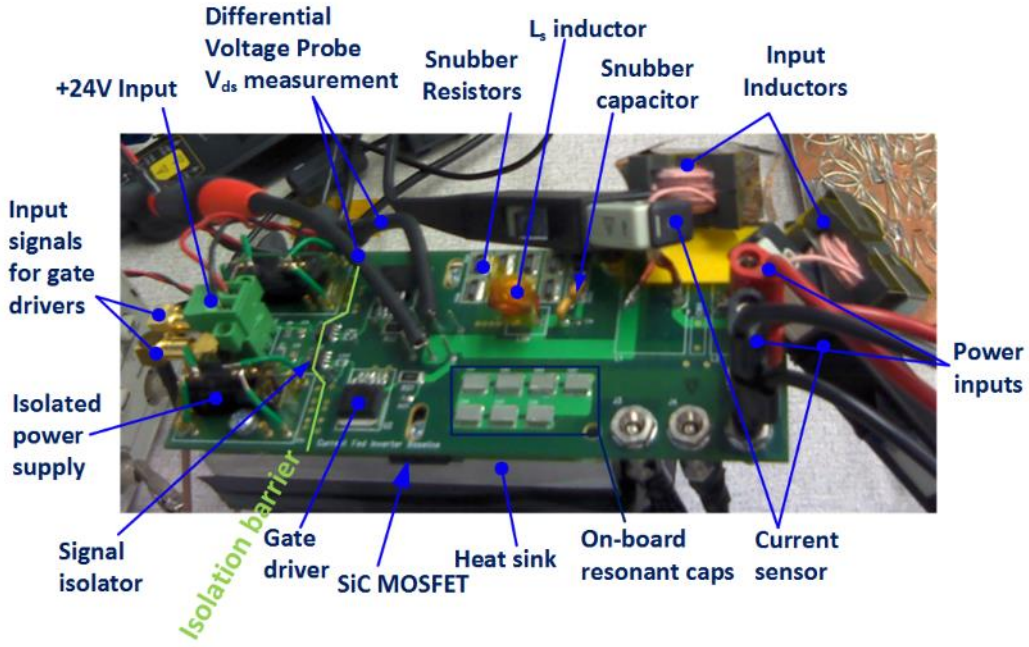


Figure 2-56. Boost amplifier implementation with major components being labeled.

2.7. Experiments

2.7.1. Description of the Test Setup, Measurement Strategy, and Measurement Accuracy

The boost amplifier is powered from the Sorensen DCR 600-4.5A power supply. The switching signal for the gate driver is created with AFG 3102 dual channel waveform generator. The gate drivers are supplied from HP 36631A bench power supply set for 24 V output. The fans for cooling of heat sink and load coils are powered from UP60-14 power supply. Thermal camera FLIR E40 is used to find possible hotspots in the system.

The capturing of the amplifier's waveforms is done using TDS7054 and MSO4054B oscilloscopes. Voltage sensing is achieved with Tektronix P5205 and THDP0200 voltage probes. Current sensing is achieved with TCP0030 and A6303 current probes. The A6303 probe is connected to the AM503B amplifier before connecting to the oscilloscope. The test setup is shown in Figure 2-57.

The boost amplifier is at first tested at continuous operation to determine the hotspots in the system. Afterwards the amplifier is tested at pulsed-power mode to keep the temperature of the load coil low, and its equivalent circuit parameters constant during the amplifier operation. The power pulse is set for duration of 500 μs with 3 ms period (the duty cycle of the pulse is 1/6).

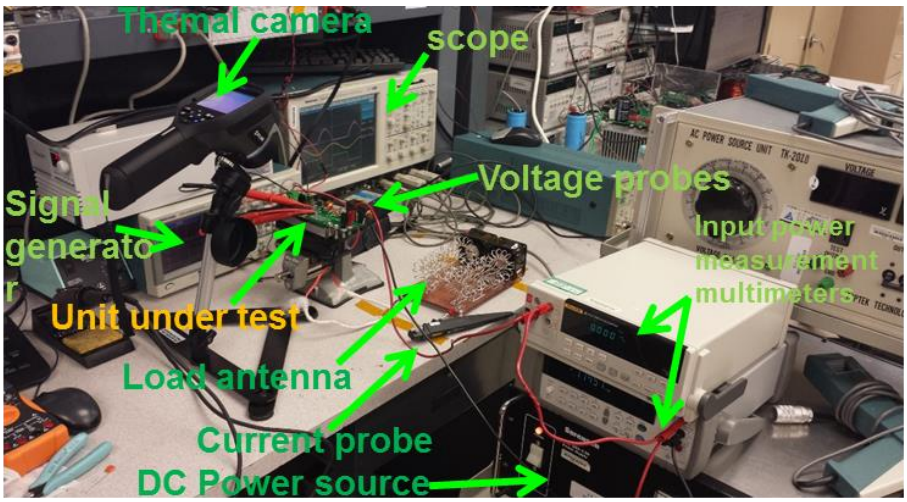


Figure 2-57. Test setup of the boost amplifier from Figure 2-43 a) and with parameters from Table 2-13. Most important equipment used in testing is labeled.

The voltage and current probes measure main circuit variables such as input voltage (V_{in}), input current (I_{in}), input inductor current (I_{L1}), resonant tank voltage (V_r), output voltage of the switching stage (V_{AB}), input current to the resonant tank (I_t), and the resonant tank current (I_r). Since oscilloscope has only four channels, at first the amplifier is tuned to the resonant frequency while measuring V_{AB}, I_t, I_r, and V_{in}. The tuning process involves varying the switching frequency until synchronous operation described in section 2.2.7 is achieved. After the synchronous operation is verified, the probes are moved to measure V_{in}, I_{in}, I_t, and V_r in order to access the efficiency of the amplifier.

The input power (P_{in}) is computed as the average of V_{in} and I_{in} product over 50 measured cycles in the steady-state. Similarly, the output power of the resonant tank (P_t) is computed as the average of V_r and I_t product over 50 cycles in the steady state. The power that is given to the load coil (output power) is

$$PA = P_t - P_{cap} \tag{2-111}$$

where P_{cap} is power loss of the resonant capacitor that is generated due to its parasitic resistance (ESR_{Cr}), as described with (2-75). The amplitude of the resonant current can be measured with secondary scope, and P_{cap} can be computed using (2-75). The amplifier efficiency is simply the ratio of the output and the input power.

The proposed measurement method of the output power is not significantly susceptible to the error from the measurement delay mismatch between probes. The zero-crossings of V_r and I_t tend to be synchronized, and therefore the measurement error depends on the cosine of the phase angle between the zero-crossings of the measured signals ($\Delta\varphi_c$). Since the phase angle $\Delta\varphi_c$ is small, the value of the cosine will be close to one and the measurement error is not significant. If the output power is computed from V_r and I_r measurements, the error would be significant. The output power depends on the cosine of the phase angle between V_r and I_r zero-crossings (φ_s). Since V_r and I_r are voltage and current of an inductor, the φ_s is close to $\pi/2$. The $\cos(\varphi_s)$ vary significantly around $\pi/2$ value in case of the measurement delay mismatch, making the measurement error unacceptable.

The sampling rate of the oscilloscope is set to 500 MS/s for the total recording time of 2 ms. Total number of samples is 1 million for total 1000 cycles, or 1000 samples per cycle. The samples are recorded and sent to MATLAB for post-processing in order to compute the efficiency. Since the oscilloscope is used to record measurements, the measurement error will be significant when computing the efficiency of the amplifier. The waveform averaging, offset and gain compensation is done in the post-processing in order to increase the accuracy. Offset is relatively easy to

adjust (nullify) in the examination of the measured signal. Gain compensation is typically not necessary to be applied, however, if necessary (2-24) can be applied to correct the ratio of the input and the output voltage.

Since the measurement error due to signal propagation mismatch in the probes is minimized, the main source of measurement error is the due to sampling of the signals. The oscilloscope has 8 bit sampling, giving 256 quantization levels. The averaging increases effective number of bits in the quantization process by

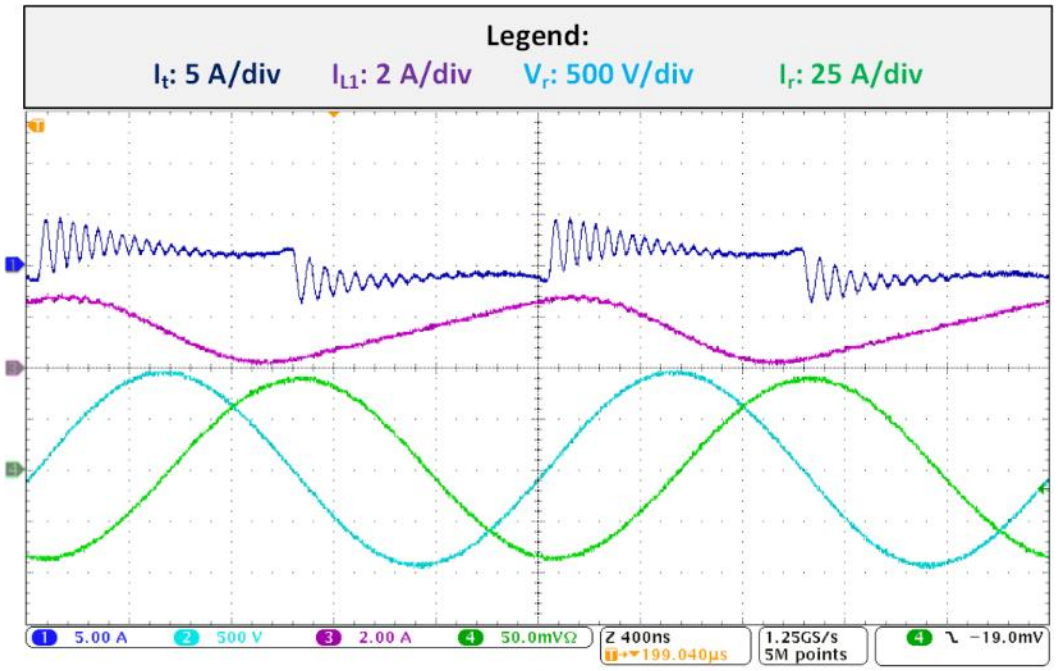
$$0.5 \cdot \log_2(N) \tag{2-112}$$

where N is the number of averages. Since the number of averages is 50, the increase in resolution is 2.822 bits, and the effective number of bits is ENOB = 10.822. Such ENOB ensures the measurement error of the efficiency to be less than few percent.

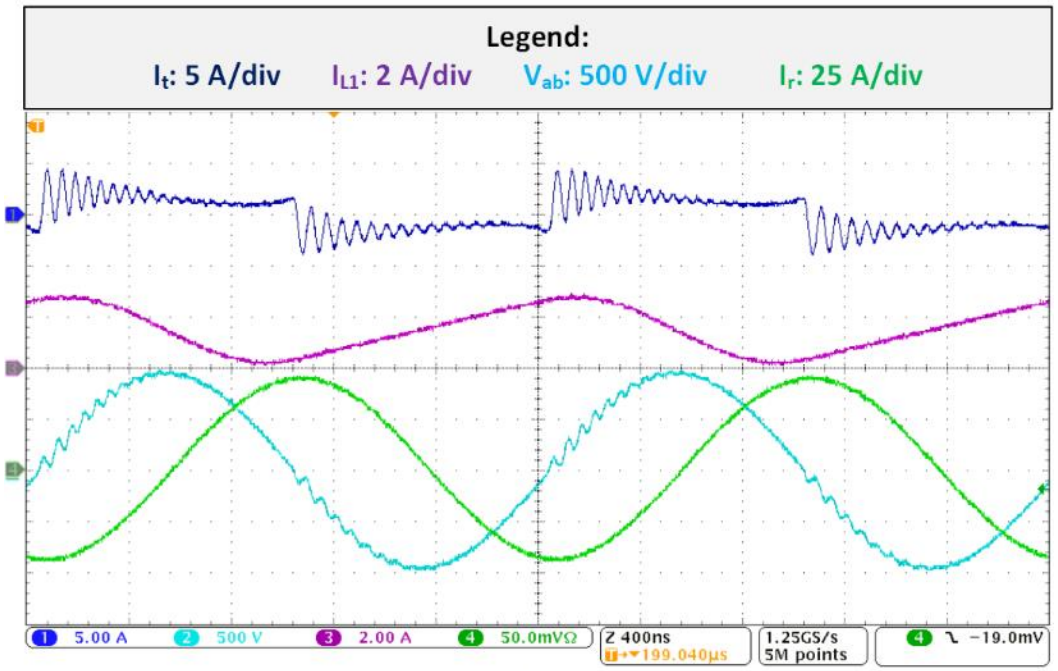
2.7.2. Continuous Operation at Synchronous Frequency & Thermal Performance

The boost amplifier from Figure 2-56 and Table 2-13 is tested for the input voltage of V_{in} = 300 V to maximize the output power and verify the thermal performance of the amplifier's power stage. The input inductor has value of L_{in} = 125 uH, which corresponds to the Inductor 2 design. The load configuration is set to Load-2 (from Table 2-14). The inductance of the Load-2 takes values at the lower end of the specified range since the coils were stiff after the construction and the cross-section of the coil's turn is smaller. The synchronous frequency is thus increased from the expected value in Table 2-13, and it is equal to 500 kHz. The switching frequency is tuned to the synchronous frequency.

Figure 2-58 a) shows the recorded waveforms of V_r, I_r, I_{L1}, and I_t variables. Tested reactive power is 20 kVA. The active power in the load is measured as PA = 854 W. The loaded quality factor is Q = 24. The magnitudes of the resonant voltage and current are V_{rm} = 942 V and I_{rm} = 44 A. The high-frequency ringing of the It current is larger than it is expected from the analysis in section 2.5. The snubber performance will be examined more in detail in section 2.7.5. The left-hand side of the boost amplifier is not completely symmetrical with right-hand side (parasitic PCB capacitances differs, as well as output capacitances of transistors), and therefore the current ringing is not symmetrical against x-axis. It is difficult to balance the both sides since the output capacitors of transistors are non-linear, and the balancing would require to have two transistors with almost equal output capacitance dependence on voltage. Figure 2-58 b) shows the recorded waveform of V_{AB} variable, while I_R, I_{L1} and I_t are same as in Figure 2-58 a).



(a)



(b)

Figure 2-58. Measured waveforms for the boost amplifier with L_{in} = 125 µH, V_{in} = 300 V and PQ = 20 kVA and Q = 24. (a) $V_r(t)$ measured; (b) $V_{AB}(t)$ measured.

The thermal performance of the power stage is examined using FLIR E40 thermal camera and the steady-state of the amplifier's operation. The amplifier reached thermal equilibrium. Figure 2-59 a) shows the normal picture of the amplifier's power stage. Figure 2-59 b) shows the infrared picture, where the thermal hotspots are detected to be the On-board resonant capacitors, gate driver chip, and the gate resistors. The resonant capacitors operate at the limit of their specified temperature range, around 125 °C. The gate driver operates at around 90 °C. The gate resistors' temperature is close to 100 °C. The input inductors, heat sink, power transistors, and snubber resistors do not show significant increases in temperature. The load coil starts overheating after 700 W of output power, with temperatures going over 150 °C. The load coil is a piece of wire, and thus it does not have a difficulty to sustain high temperature. However, the testing is more difficult since the load coil changes its circuit parameters with temperature [109]. The load resistance would normally increase. The inductance also increases, as the wire is expanded and forms larger winding turn. The synchronous frequency would change as well, and the switching frequency would have had to be changed dynamically. For this reason, for the efficiency measurement the amplifier is tested in the pulsed mode. The input voltage is reduced to V_{in} = 800 V for safety of power transistors. The value of V_{in} = 942 V showed to be too aggressive. The initial start-up transient reaches around 1200 V, which is the maximum rated voltage of transistors and can lead to their failure.

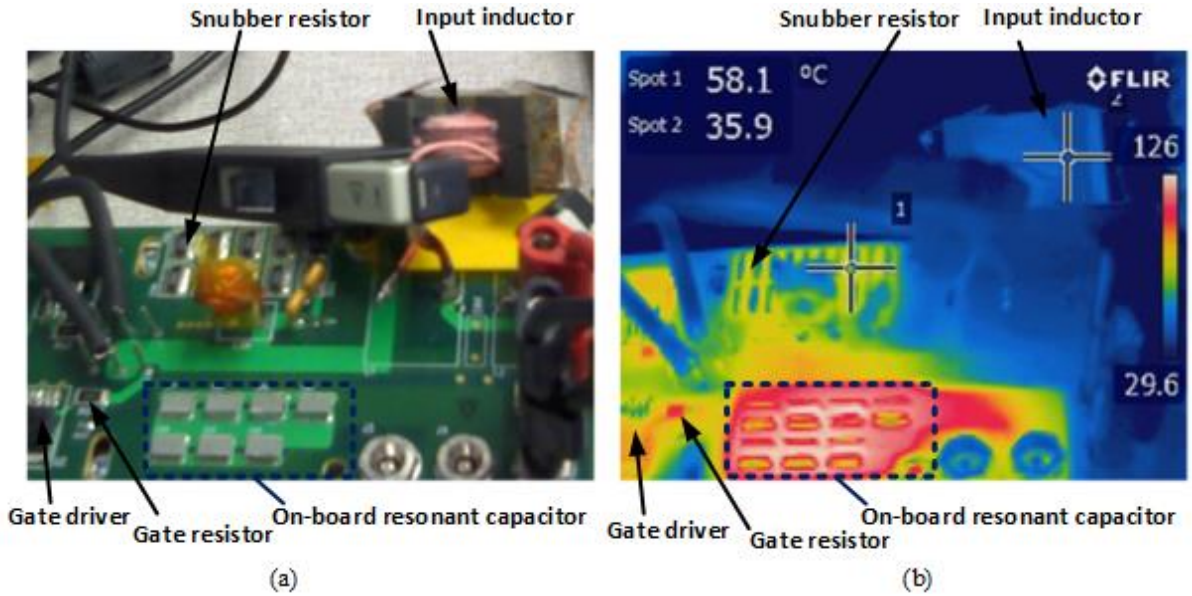


Figure 2-59. Thermal image of the amplifier's power stage: (a) power stage; (b) thermal image. On-board capacitor operates at the temperature limit ~ 125 °C. The gate driver chip and the gate resistor heat up to ~ 90 °C.

2.7.3. Synchronous Operation for Inductor 3 Design-Case

The boost amplifier is tested for Inductor-3 design-case. From the analysis in section 2.4, it is expected that Inductor-3 design-case has good light and heavy load efficiency, while keeping the input inductance (L_{in} = 232 μH) and bandwidth of the system relatively low. The amplifier is tested for input voltage of V_{in} = 255 V, and in pulsed power mode. The pulse is 500 us long, with 3 ms period between pulses. The load is varied for all four configurations that are indicated in Table 2-14. For each load, the amplifier is operated at the synchronous frequency. The recorded waveforms include input voltage (V_{in}) and current (I_{in}), resonant tank's voltage (V_r) and input current (I_t). Separate scope is used to record the amplitude of the resonant tank's current (I_r). The recordings of the five variables are transferred to MATLAB, where the post-processing is done to extract 50 cycles of the steady-state operation, and eliminate possible offset and gain errors of the probes. The efficiency of the amplifier is computed for 50 cycles, as noted in section 2.7.1.

Figure 2-60, Figure 2-61, Figure 2-62, and Figure 2-63 show the recorded waveforms for each load configuration. For all tested cases the output reactive power is around PQ = 14 kVA. In Figure 2-60, the Load-1 is tested. The loaded quality factor of the load is Q = 40 at the switching frequency of f_{sw} = 486.5 kHz. The amplitudes of the resonant voltage and current are V_{rm} = 800 V and I_{rm} = 34.5 A. The measured input voltage and current are V_{in} = 249.5 V and I_{in} = 1.3788 A. The input power is P_{in} = 344 W. The measured power given to the resonant tank is P_t = 340.4 W. The output power is computed as in (2-111), and it is equal to PA = 336.4 W. The measured efficiency is computed to be η = 97.8 %. The error from the quantization process is assessed, and the worst-case efficiency due to error is computed to be η_{min} = 95.5 %.

The tests of the Load-2 configuration are given in Figure 2-61. The switching frequency is set to f_{sw} = 481.5 kHz. The Q-factor of the load is Q = 28. The amplitudes of the resonant voltage and current are V_{rm} = 800 V and I_{rm} = 35 A. The input voltage and current are measured to V_{in} = 257 V and I_{in} = 2.031 A. The input power is computed to be P_{in} = 522 W. The resonant tank's power is measured to be P_t = 515.1 W. The output power is PA = 511.1 W, with the efficiency of η = 97.9 %. The worst-case efficiency due to quantization process is η_{min} = 96 %.

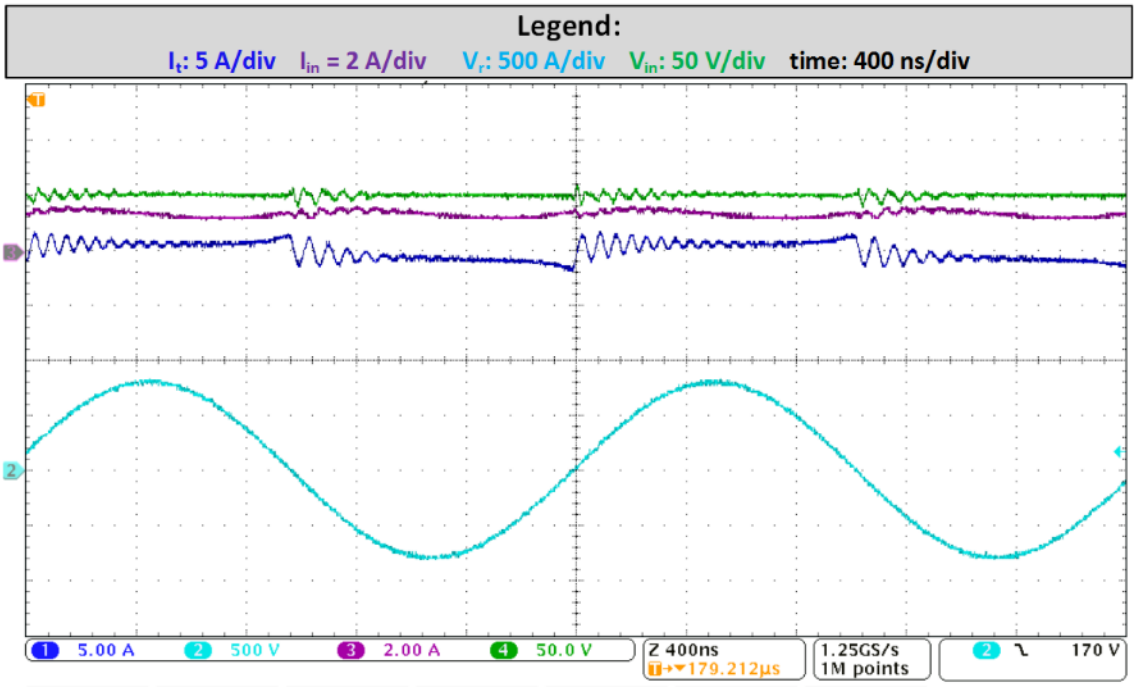


Figure 2-60. Recoded waveforms of the boost amplifier test for L_{in} = 229 µH, V_{in} = 249.5 V, I_{in} = 1.3788 A f_{sw} = 486.5 kHz, V_{rm} = 800 V, and Q = 40.

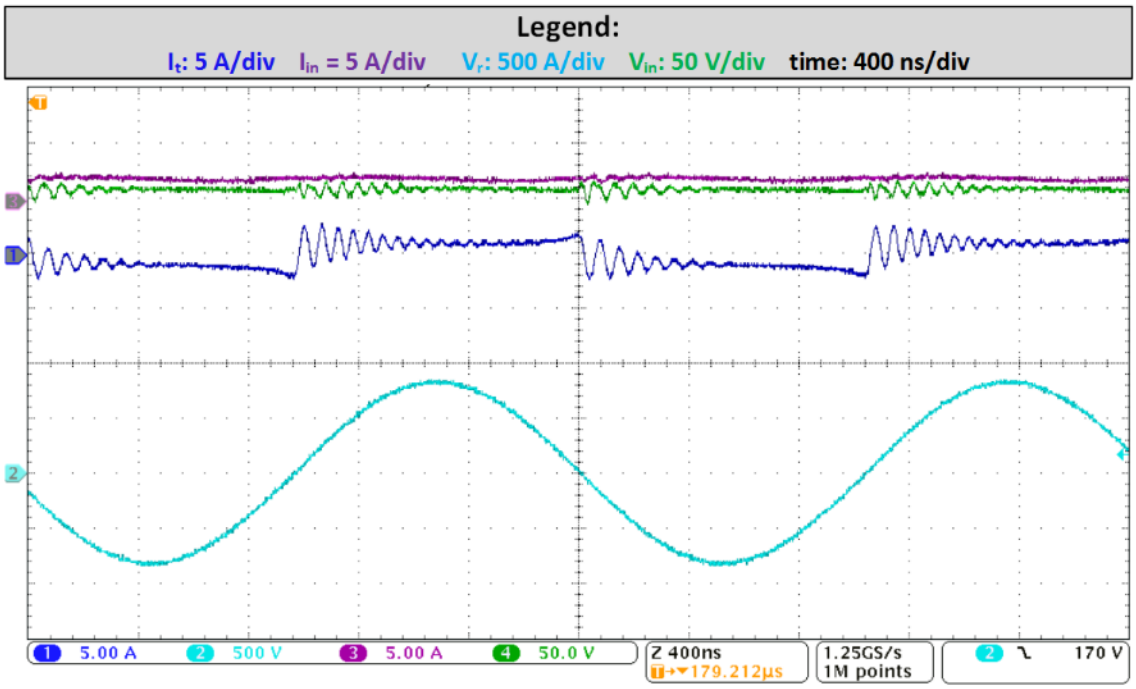


Figure 2-61. Recoded waveforms of the boost amplifier test for L_{in} = 229 µH, V_{in} = 257 V, I_{in} = 2.031 A, f_{sw} = 481.5 kHz, V_{rm} = 800 V, and Q = 28.

The waveforms of the Load-3 tests are given in Figure 2-62. The switching frequency is f_{sw} = 481.5 kHz, with the Q-factor of Q = 14. The amplitudes of the resonant voltage and current are V_{rm} = 800 V and I_{rm} = 35 A. The input voltage is V_{in} = 253 V, and the input current is I_{in} = 3.915 A. The input power is P_{in} = 990 W. The tank's input power is P_t = 975 W, and the output power is PA = 971 W. The efficiency is η = 98.1 %. The worst-case efficiency due to quantization process is η_{min} = 97.2 %.

The test waveforms for the Load-4 are given in Figure 2-63. The switching frequency is f_{sw} = 477 kHz. The loaded quality-factor is Q = 12.8. The amplitudes of the resonant voltage and current are V_{rm} = 820 V and I_{rm} = 37 A. The input voltage and current are V_{in} = 257.3 V and I_{in} = 4.5364 A, and the input power is computed as P_{in} = 1165 W. The resonant tank's input power is measured as P_t = 1149 W. The output power is PA = 1145 W, and the efficiency is computed to be η = 98.3 %. The worst-case efficiency due to quantization process is computed to be η_{min} = 97.5 %.

The ringing is present in V_{in} and I_{in} waveforms. The cause of observed ringing is the parasitic capacitance of the input inductors that makes a propagation path for the high frequency currents from the V_A and V_B nodes to V_{in} node. The ringing on V_{in} node is observed because no additional capacitor is put in between the power source and the amplifier to filter out the high frequency content.

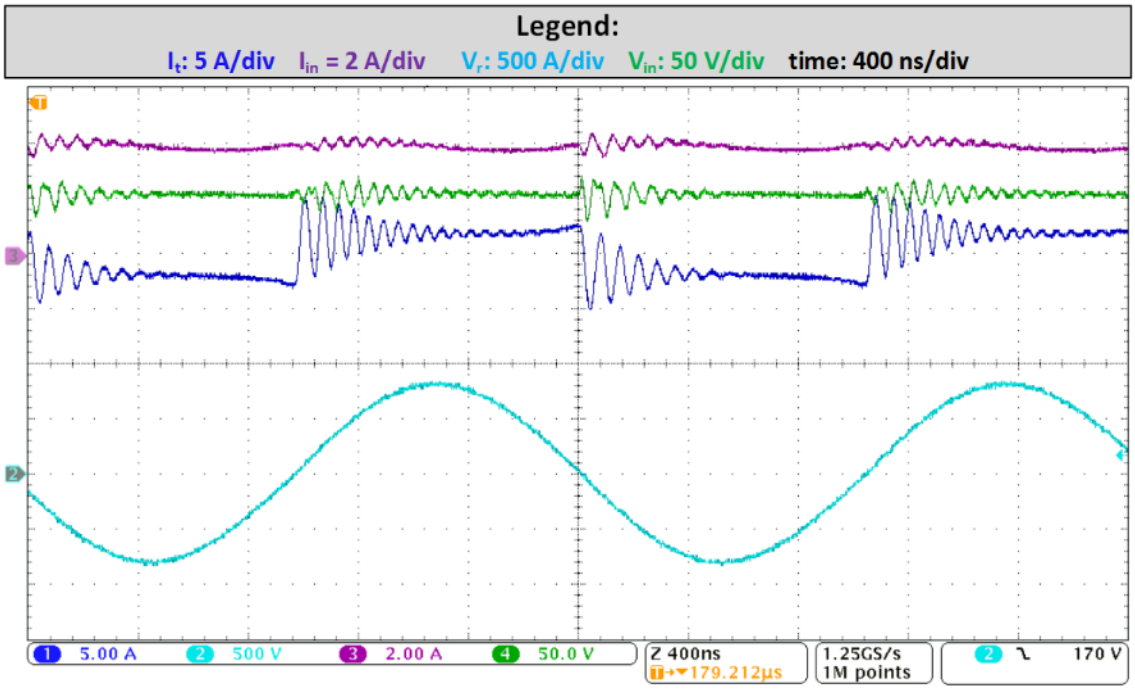


Figure 2-62. Recoded waveforms of the boost amplifier test for L_{in} = 229 µH, V_{in} = 253 V, I_{in} = 3.915 A, f_{sw} = 481.5 kHz, V_{rm} = 800 V, and Q = 14.2.

Figure 2-64 shows the efficiency and output power versus the loaded-quality factor Q. The efficiency curve is reasonably flat with the change of Q-factor, which is expected from the discussion in section 2.4.6. The sudden increase of the efficiency and output power for Q = 12.8 indicate some larger error value in the measurements, as more flat efficiency characteristics is expected. The maximum measured output power is PA_{max} = 1145 W, and the minimum output power is PA_{min} = 336.4 W.

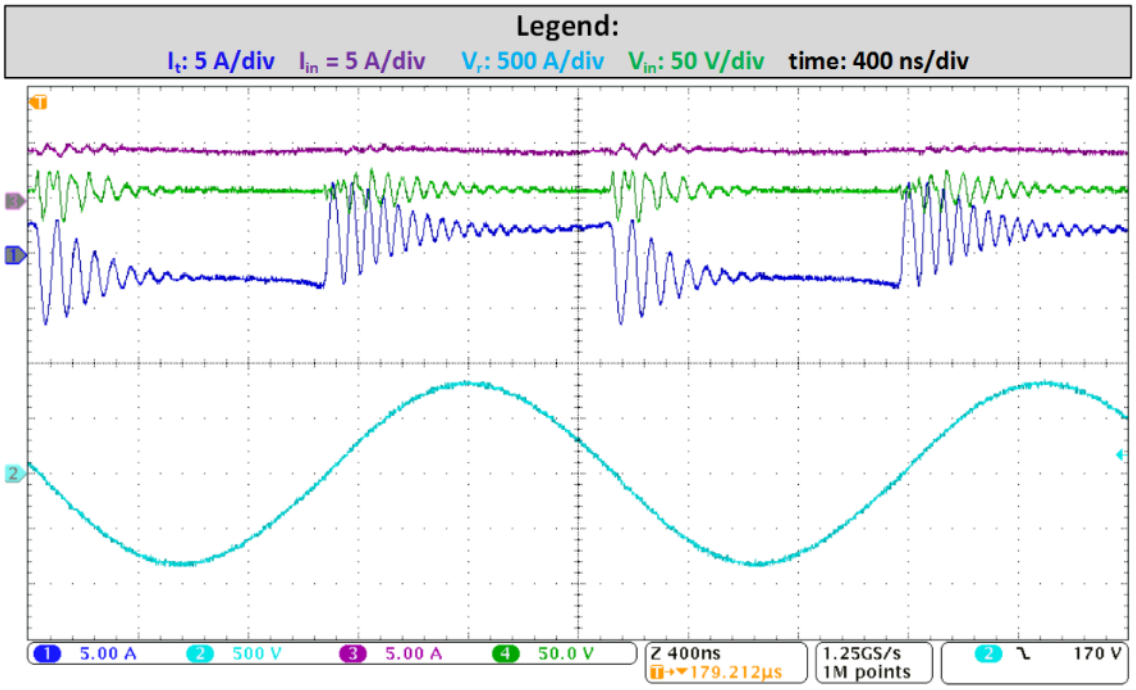


Figure 2-63. Recoded waveforms of the boost amplifier test for L_{in} = 229 µH, V_{in} = 257.3 V, I_{in} = 4.5264 A, f_{sw} = 477 kHz, V_{rm} = 820 V, and Q = 12.8.

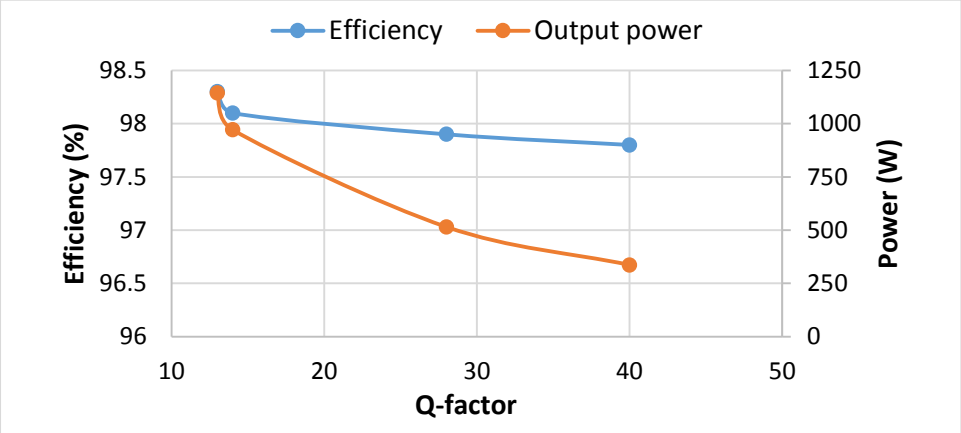


Figure 2-64. System efficiency and output power for Inductor-3 case, L_{in} = 229 µH.

2.7.4. Synchronous Operation for Inductor 2 Design-Case

The hardware tests of the boost amplifier are done for the Inductor-2 design-case in order to confirm the trade-off between large bandwidth and light-load efficiency. The recorded waveforms from the maximum power case (loaded quality factor is Q = 12) is shown in Figure 2-65. The input voltage was set to V_{in} = 255 V. The amplitudes of resonant voltage and current are V_{rm} = 800 V and I_{rm} = 35 A. The switching frequency is f_{sw} = 483.5 kHz. The input current is I_{in} = 4.48 A. Recoded power at the input of the resonant tank is P_t = 1128 W. The output power is PA = 1124 W. The efficiency is calculated to be η = 98.5 %. The worst-case efficiency is computed to be η_{min} = 98 %. Noticeable, the input current ripple is much higher for Inductor-2 than for Inductor-3 design-case.

The measurement procedure is repeated as it is in previous section for the rest of load configurations. The measured efficiency and output power are plotted in Figure 2-66. Minimum efficiency is measured for the Q = 40 case, and it equals to η = 96.5 %. The drop of around 2 % in efficiency is measured from heavy load (Q = 12) to light load (Q = 40) case. This is in accordance with predictions in section 2.4.6, where slightly higher efficiency is predicted since fixed snubber losses were not included. Figure 2-67 shows the difference between the prediction and measurement. The maximum of the measured output power is PA_{max} = 1124 W. The minimum of the measured output power is PA_{min} = 364.4 W

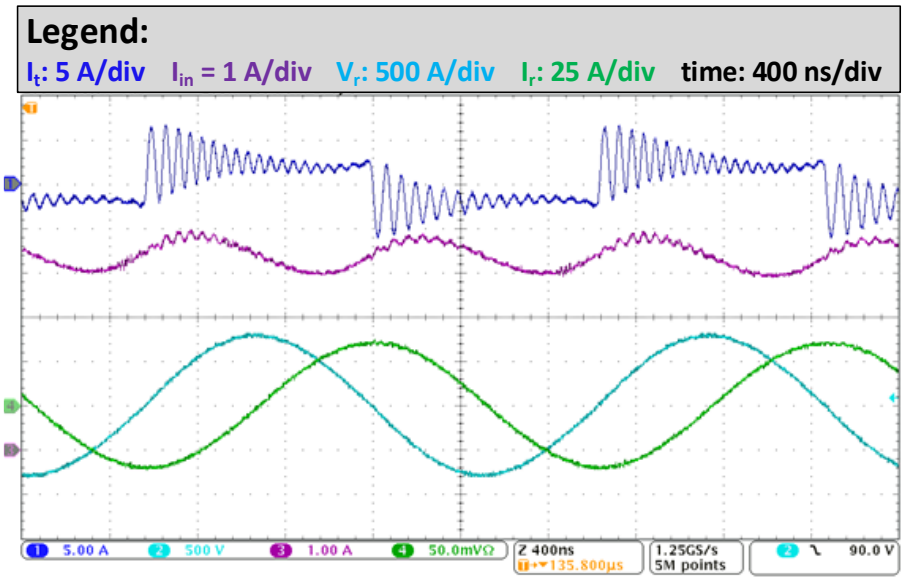


Figure 2-65. Recoded waveforms of the boost amplifier test for L_{in} = 125 µH, V_{in} = 255 V, I_{in} = 4.48 A, f_{sw} = 483.5 kHz, V_{rm} = 800 V, and Q = 12.

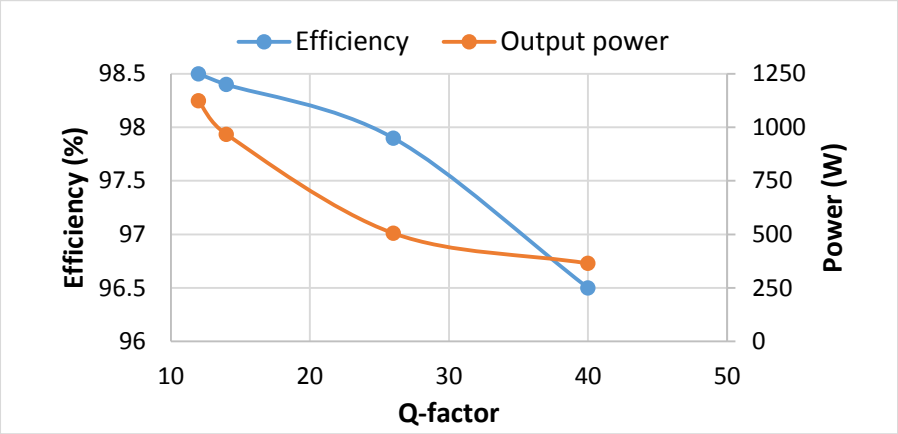


Figure 2-66. System efficiency and output power for Inductor-2 case, L_{in} = 125 µH.

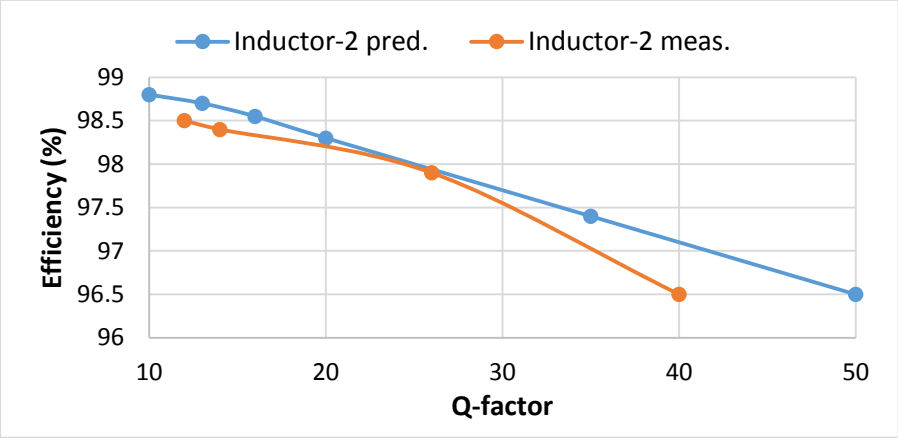


Figure 2-67. System efficiency for Inductor-2 case (L_{in} = 125 µH), prediction versus measurement. The chart is based on curves in Figure 2-40 and Figure 2-66.

The comparison between measured efficiency of Inductor-2 and Inductor-3 design-cases is shown in Figure 2-68. The measurement is not completely fair since the measurements are obtained for somewhat different input voltages, operating frequencies, and power levels. However, the results still depict the major difference between the cases: the light-load efficiency is considerably better (1.3 % higher for Q = 40) for the Inductor-3 than for Inductor-2 case. The heavy-load efficiency does not differ much (both in prediction and in measurement), thus the error in measurement or differences in the implementation may impact the obtained result.

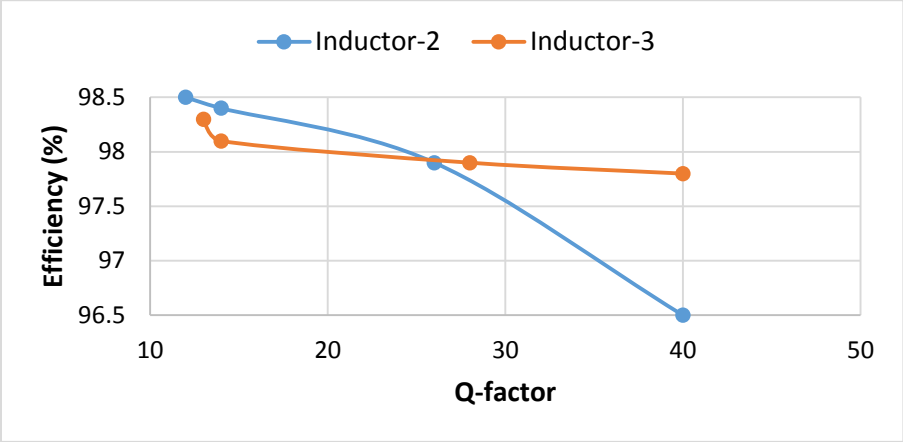


Figure 2-68. Comparison between efficiencies for Inductor-2 case (L_{in} = 125 µH) and Inductor-3 case (L_{in} = 229 µH).

2.7.5. Snubber Performance

The ringing in any of the measured waveforms of tank's input current (I_t) is more pronounced than what is expected from theoretical analysis and simulations in section 2.5. Figure 2-49 a) is a good representative of the expected and Figure 2-62 of the measured performance. Additionally, the ringing in the measured waveforms is not symmetrical with the x-axis. The reason is poor performance of implemented LCR snubber structure.

The circuit parasitics are investigated to find possible reasons for excessive ringing of I_t current. It has been found that two parasitic capacitances in the snubber circuit are culprits. The capacitances are labeled as C_{p3} and C_{p4} in Figure 2-69, where a detailed circuit schematics of the boost amplifier that includes circuit parasitics is given. Impedance analyzer Agilent 4294A with 16047e adapter is used to measure C_{p3} and C_{p4} capacitances of the amplifier's PCB. Few to several tens of pico-farads were measured, however, the exact values of the capacitances are found using a parametric study of the boost amplifier's circuit model. Additionally, capacitances C_{p1} and C_{p2} are measured for non-equal values, in the range of tens of pico-farads.

For the purposes of the parametric study, the circuit in Figure 2-69 is built in LT spice. After series of parametric variations, the circuit parameters of the boost amplifier are determined to simulate the amplifier's behavior from Figure 2-62. The parameters are tabulated in Table 2-19. The simulated waveforms (red) of the amplifier are compared with measurements (blue) in Figure 2-70. The steady-state operation is matched very closely for dc values of input voltage (V_{in}) and current (I_{in}), and also for ac value of resonant voltage (V_r) at the fundamental frequency. The harmonic

contents of tank's input current (I_t) is modeled precisely as well, thanking to close estimation of C_{p3} and C_{p4} capacitances. The ringing behavior in I_t current is also function of C_{p1} and C_{p2}. Since these capacitances are estimated closely to exact values, the simulated I_t resembles well measured waveform. The ringing behavior of I_{in} and V_{in} could be more precisely match by increasing capacitances C_{pL1} and C_{pL2}, however, the performance of the snubber circuit would not be changed.

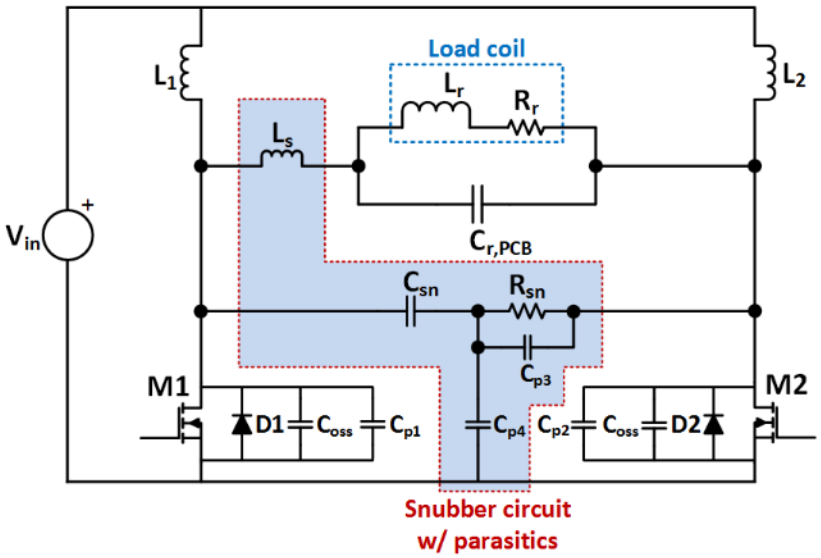


Figure 2-69. Snubber circuit w/ parasitics that degrade the performance.

Table 2-19. Simulation parameters of the boost amplifier used to match measured results.

V_{in} (V)	253 V	f_{sw}(kHz)	481.5	$L_1/L_2/L_{in}$ (µH)	229
L_r (µH)	7.28	R_r (Ω)	1.54	L_s (nH)	280
C_{sn} (pF)	75	R_{sn} (Ω)	100	C_{pL1} (pF)	5
C_{pL2}(pF)	10	C_{p1} (pF)	80	C_{p2} (pF)	140
C_{p3} (pF)	40	C_{p4} (pF)	20		

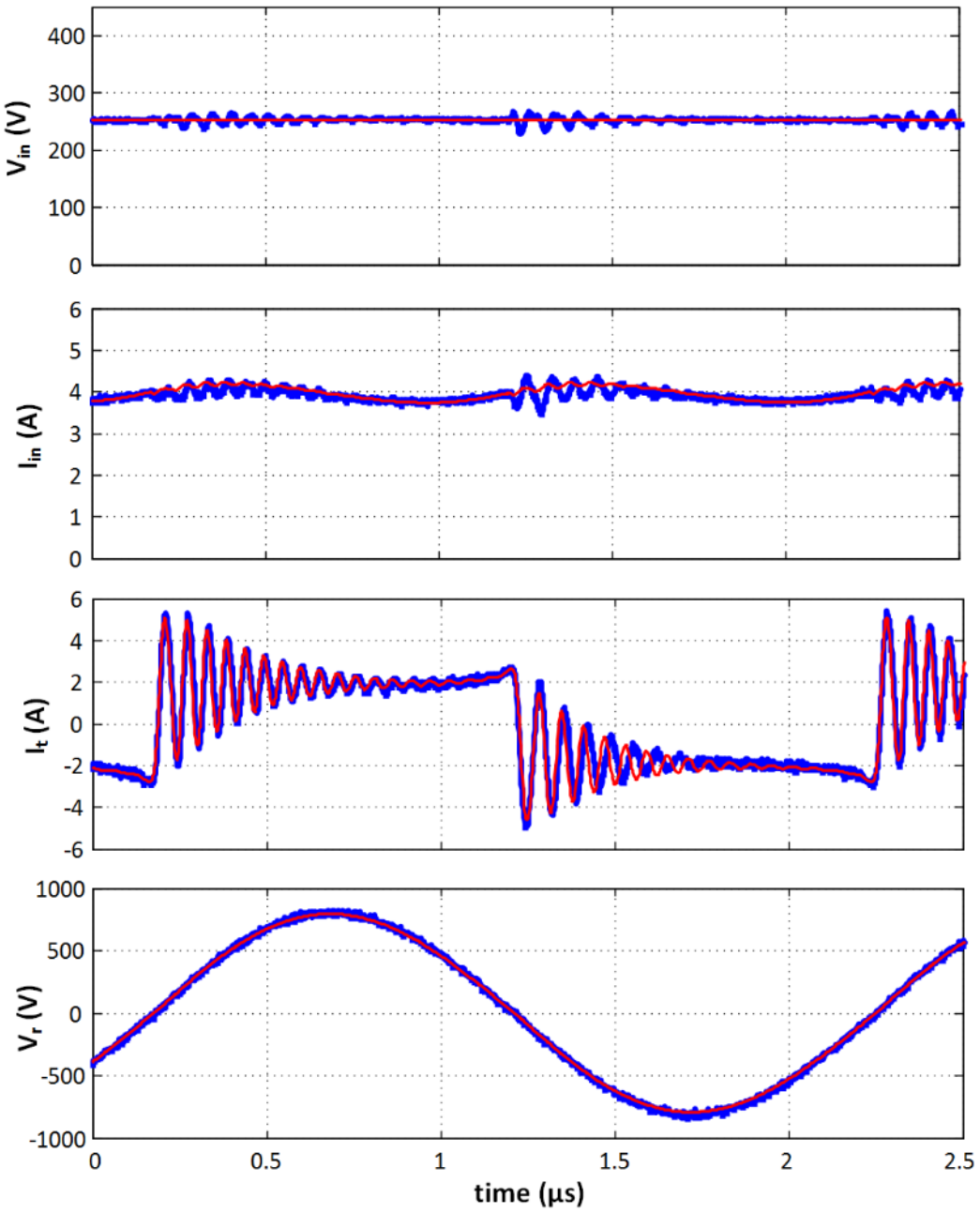


Figure 2-70. LCR snubber performance for L_s = 250 nH, C_{sn} = 75 pF, and R_{sn} = 100 Ω: Measurements vs. simulated model. Blue: measurements; Red: Simulation model.

Although the C_{p4} capacitance could be eliminated though the careful layout, the C_{p3} capacitance is difficult to tackle. The R_{sn} resistance is a parallel configuration of large number of individual components so the required power level is reached. As a consequence there will be some significantly enough parasitic capacitance (C_{p3}). Having also large power dissipation, it is concluded that LCR is not a convenient snubber structure unless the parasitic components are not extremely well controlled.

Performance of LR snubber structure is examined is well, and it is presented in Figure 2-71. The figure shows that snubber is doing excellent work. Small ringing is still present since the quality-factor of snubber circuit is Q_{sn} = 2.8. Comparing the obtained measurements and theoretical investigation in section 2.5 it is seen that LR snubber offer superior performance, both in terms of power loss and available damping of oscillations.

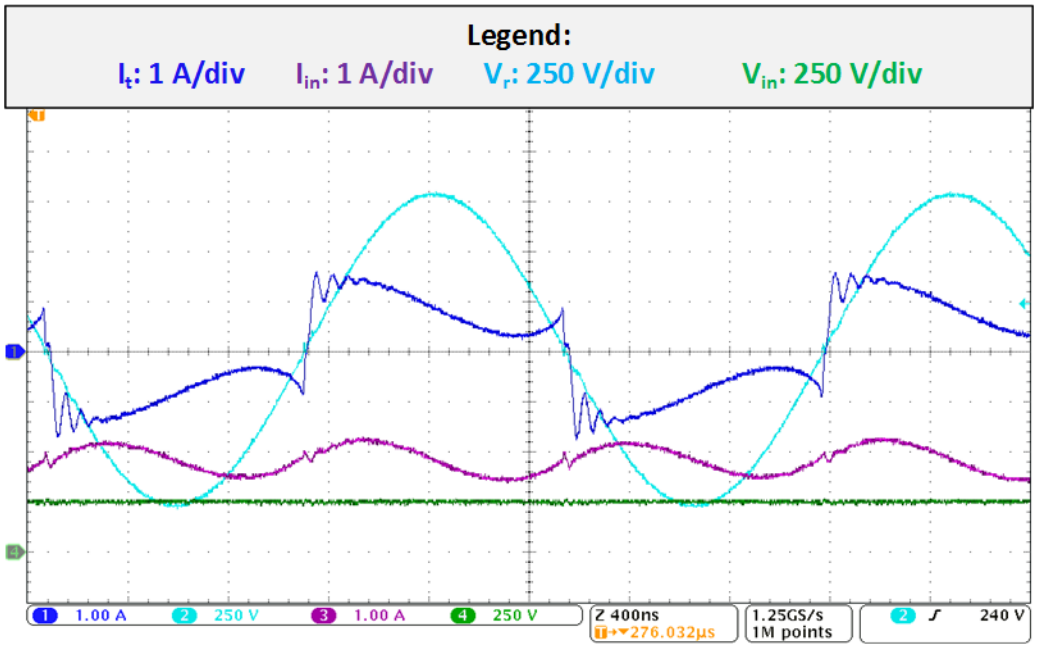


Figure 2-71. LR snubber performance for L_s = 250 nH, and R_{sn} = 100 Ω. Ringing is limited but observable since quality-factor of the snubber circuit is Q_{sn} = 2.8.

2.7.6. Unsolved Issues

The boost amplifier has been tested for two different input inductance values. High efficiency has been reported, over 95 % for wide range of the load change. However, further improvements can be made that can improve the amplifier's performance, or the accuracy of measurements.

One of the largest issues in testing the boost amplifier was the high quality-factor of the load. Power and temperature cycling changes the circuit parameters, changing the operating point of the amplifier. The circuit for continuous tuning of the switching frequency to the synchronous frequency would make the testing significantly easier. Such circuits are reported in [110].

The load inductor is prone to overheat when the output power is higher than 700 W. More advanced cooling system using an enclosure full of oil would prevent the overheating, and additionally would enable more precise efficiency measurement. The input power would then be measured using a set of high resolution digital multi-meters, while the output power would be estimated with the temperature characterization of the oil enclosure for given power loss in the enclosure.

The estimation of the amplifier's performance can be improved if better prediction of the AC conduction losses is achieved. Method proposed in [99] did not predict the proximity effects very accurately due to irregular structure of the winding. The order in the structure of the winding can be improved by utilizing a bobbin. The bobbin can be created using 3D printing technology. The inclusion of fringing effects on the inductance and losses in the analysis of input inductor performance would increase the predictability of boost amplifier operation.

The section 2.7.5 describes the issues with circuit parasitics on the operation and performance of the boost amplifier. The parasitics can be modeled and estimated using finite element analysis (FEA) tools, such as ANSYS Q3D. Left-hand and right-hand side of the boost amplifier's schematic can be made more symmetrical, which would make the waveforms of the circuit variables more symmetrical with x-axis (time) as well.

Snubber circuit was analyzed in detail. The pitfalls in snubber implementation were presented, however, a redesign is required to achieve optimum performance. This will be the part of the future work.

2.8. Conclusion

The boost amplifier operation is predicted and modeled for wide range of input inductance values, L_{in}. Of particular interest is design for low values of L_{in} (L_{in} ~ 100 μH), where the amplifier's bandwidth is significantly high, around 100 kHz. The trade-offs in selection of the input inductance value are well examined, both qualitatively and quantitatively. The design guidelines are given. The amplifier is constructed for 14 kVA at the output, and tested for very high efficiency, well over 95 %, with maximum of 98.5 %.

The term "synchronous frequency" is established to replace imprecise "resonant frequency" and "ZVS frequency" for general resonant power converter system. It will be shown in section 4 that "synchronous frequency" depends on circuit parameters such as input voltage magnitude or duty cycle.

The boost amplifier topology presented in this chapter overcomes two traditional drawbacks of the current-fed resonant converters. The input inductor(s) can be arbitrarily designed for small size or large bandwidth while keeping the efficient operation at the synchronous frequency. A series diode associated with the bidirectional voltage blocking switch can be completely eliminated or replaced by approximately 1.5–3 times less lossy current snubber.

The obtained results are valid for highly inductive loads with quality-factors larger than ten. However, the methodology is still applicable for low Q-factor loaded system if more harmonic content is assumed for input inductor's current, resonant tank's voltage and current.

Minimum input inductance for which derived equations in section 1.3 are correct is around three to four times larger than the resonant coil's inductance. This limitation is not very significant since the currents in input inductors and the power transistors are comparable to the coil's current, making the boost amplifier very inefficient.

The boost amplifier was analyzed in this chapter for the constant input voltage. In practice, the output amplitude is controlled with front converter. Chapter 3 examines the amplitude control of amplifier's output with slowly changing input voltage. In chapter 4, the boost amplifier is driven with PWM excitation at the switching frequency. Important drawback of the boost amplifier is the inability to keep switching frequency tied to synchronous frequency under parametric variations. For example, the tests in section 2.7.3 and 2.7.4 are done at different switching frequencies. However, in chapter 4 it will be shown that the synchronous frequency can be controlled and tied to the fixed switching frequency even under severe parametric variations.

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Chapter 3. Modeling of Boost Amplifier with High Q-factor Inductive Load

Average model for current-fed parallel resonant boost inverter has been developed based on Generalized State-Space Averaging method. The model includes impact of input inductance on the resonant/synchronous frequency. Compared with known low-frequency model, the new average model gives the complete insight to the complex high frequency operation of the inverter and improved accuracy when the inverter is operated away from the synchronous frequency. The model is validated with switching simulations and experimentation for various cases of inverter excitations. In addition, model is used in synthesis of output waveforms with slowly changing envelope. Hann-function and trapezoidal-function envelopes are created.

3.1. Introduction

Resonant power conversion is the preferred method of power transfer in high-frequency, high power applications due to small switching losses [1]. When operated at the resonant frequency, the switching losses are close to zero. However, design and operation at the resonant frequency is not always a trivial task and such is the case of Current-fed Parallel Resonant Inverter with two input inductor (boost inverter) given in Figure 3-1. Commonly, the boost inverter is represented with the equivalent circuit in Figure 3-2 a), and the resonant frequency is given with

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r} - \left(\frac{R_r}{L_r}\right)^2} \tag{3-1}$$

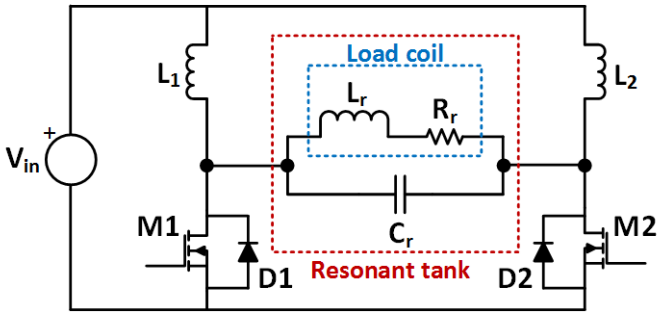
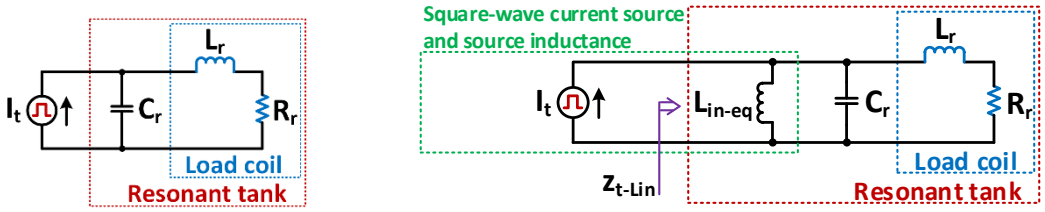


Figure 3-1. Current-fed parallel resonant boost inverter with two input inductors.

In the previous chapter, it has been shown that (4-1) holds only when the input inductance (L_{in}) is very large (mili-Henry range). When the input inductance takes much smaller values and the input voltage to the amplifier is the dc value, it was concluded that the resonant frequency is a function of the input inductance as well. New equivalent model of the inverter is found (Figure 3-2 b)), where the switching stage of the inverter is substituted with an equivalent square-wave current source and a parallel output inductance. The resonant frequency of the circuit in new equivalent model is termed synchronous frequency, since at the synchronous frequency the zero-crossing of the voltage over the resonant tank coincides with the zero-crossing of the current flowing towards the resonant tank. The comparison between equations for natural, resonant, and synchronous frequencies is given in Table 3-1.



(a) (b)

Figure 3-2. (a) Equivalent inverter model when L_{in} is very large (b) Equivalent circuit model when L_{in} is relatively small. The value of $L_{in\text{-}eq}$ is given in Table 3-1.

Table 3-1. Summary on natural, resonant, and synchronous angular frequency computation.

Natural angular frequency	Resonant angular frequency	Synchronous angular frequency
$\omega_n = \frac{1}{\sqrt{L_r C_r}}$	$\omega_r = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_r}{L_r}\right)^2}$	$\omega_{sy} = \sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2}$ $L_q = L_r \,\|\| L_{in-eq}$ and $L_{in-eq} = \frac{2L_{in}}{1+\frac{16}{9\pi^2}}$

System model is a very useful tool in the design procedure since it helps to determine harmonic contents of important variables. With the precise model, selected harmonics can be minimized or optimized for desirable performance. Frequency characteristics can be obtained as well, assisting the controls design. The boost inverter from Figure 3-1 traditionally has very large inductance [2]-[120], thus for its modeling commonly two approaches are used. First is a harmonic analysis, typically with the First-Harmonic-Approximation (FHA). FHA is used to determine the steady-state behavior at particular operating frequency. In [8], the third harmonic is used to extend the modeling approach to cases where the loaded Q-factor is small (around 2). The start-up behavior of the inverter can be used with the well-known low-frequency model [120]. The model is derived from power-energy relations when looking at the circuit from the input side. Although the model is accurate, it suffers from the reduced precision when the inverter is operating away from the system synchronous frequency (Table 3-1). Also, the low-frequency model does not give the insight to the harmonic contents thus making it not useful in circuit optimization process.

When the L_{in} is low, use of circuit simulators is an option to linearize the system [11]. However, this method is complicated, time-consuming, and with questionable accuracy. In [122], the Generalized State-Space Averaging [13] (GSSA) method is applied to model a similar topology that uses a current-splitting transformer. GSSA method is a powerful tool that works well to make a resonant converter system to be time-invariant, and it accurate when all important harmonics are considered. For example, [122] does not take into the account the first harmonic current circulation through the resonant tank, loosing precision. Thus, in this work the GSSA method is applied to obtain the system model.

The chapter is organized in seven section. Section two considers taken assumptions for inverter model derivation. Section three presents the derived model. In section four, the model is compared to the switching model made in LT-spice. From it, model accuracy is assessed and model limitations are provided. In section five the model is compared to the low-frequency model. In section six the actual boost inverter system is built and tested. The GSSA model is matched against measured waveforms for different cases of excitations: step, sinusoidal and trapezoidal. Section seven concludes the work.

3.2. Modeling Approach and Assumptions

Resonant converters and especially inverters are very difficult to model since the perturbation & linearization approach that is common for PWM converters does not work. The problem lays in the fact that the state variables are

not varying around a certain steady-state point. Rather, state variables oscillate at particular frequency. For many systems FHA is sufficient, but in this case in insufficient. State plane analysis is widely used, however it is limited for systems with two elements. Different averaging methods has been derived for slowly changing amplitudes or phases. GSSA belongs into this category. It is very accurate tool to make the time-variant system such is resonant inverter into a time-invariant. Basic principle is the extension of the Fourier series for slowly varying signals. This is done by making Fourier coefficient time-variant by computing the average value of it on a period of time for every time instance t. The (3-2) gives the forward and inverse transformation:

$$\begin{aligned} \langle x \rangle_n(t) &= \frac{1}{T}\int_{t_0}^{t_0+T} x(t-T+s)\cdot e^{-jn\omega(t-T+s)}ds \\ x(t-T+s) &= \sum_n \langle x \rangle_n(t)\cdot e^{jn\omega(t-T+s)} \end{aligned} \tag{3-2}$$

In modeling the converter, the key assumption is that the Q-factor of the load is high, Q > 10. With this assumption the output voltage V_r and output current I_r can be assumed to be purely sinusoidal (contain 1st harmonic only). Another assumption is that the current though the input inductor contains the dc component, first and second harmonics. The modeling begins by writing the state-space model with time-dependent transition matrix A. The obtained model for the circuit in Figure 3-3 is given with

$$\dot{X}(t) = A(t)X(t) + B(t)U(t) \tag{3-3}$$

where state variables are given with $X(t) = \begin{bmatrix} V_r & I_r & I_{L1} & I_{L2} \end{bmatrix}^T$, $V_r = V_a - V_b$, source matrix with $U(t) = V_{in}$, input matrix $B(t) = \begin{bmatrix} 0 & 0 & 1/L_1 & 1/L_2 \end{bmatrix}^T$, and $L_1 = L_2 = L_{in}$. The transition matrix A(t) is given with

$$A(t) = \begin{bmatrix} 0 & -\frac{1}{C_r} & \frac{1}{C_r}s_2(t) & -\frac{1}{C_r}(1-s_2(t)) \\ \frac{1}{L_r} & -\frac{R_r}{L_r} & 0 & 0 \\ -\frac{1}{L_1}s_2(t) & 0 & 0 & 0 \\ \frac{1}{L_2}(1-s_2(t)) & 0 & 0 & 0 \end{bmatrix} \tag{3-4}$$

where $S_2(t)$ is the switching function defined (for the period of operation T) with

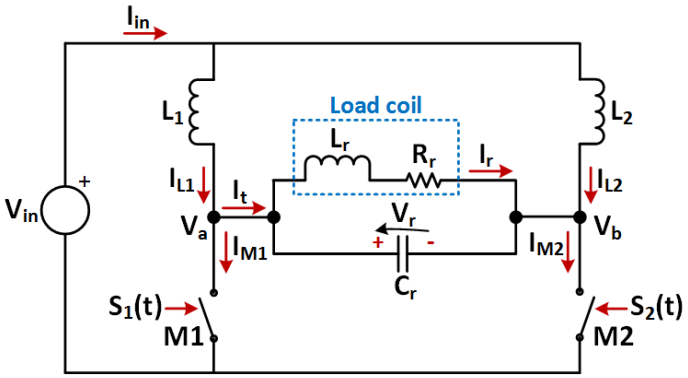


Figure 3-3. Current-fed parallel resonant boost inverter with two input inductors.

$$S_2(t) = 1 - S_1(t) = \begin{cases} 1, & 0 \le t < \dfrac{T}{2} \\ 0, & \dfrac{T}{2} \le t < T \end{cases} \tag{3-5}$$

Next section applies the (3-2) and (3-3) to make the time-invariant, average model.

3.3. Detailed Model

Following the GSSA method, the time-variant system (3-3) is transformed to the time-invariant:

$$\frac{d}{dt}\langle X_{14\times1}\rangle(t) = A_{14\times14}\cdot\langle X_{14\times1}\rangle(t) + B_{14\times2}\cdot\langle U_{2\times1}\rangle(t) \tag{3-6}$$

where state variables are given with

$$\langle X_{14\times1}\rangle(t) = \left[\langle \mathrm{V_r}\rangle_{-1} \;\; \langle \mathrm{V_r}\rangle_{1} \;\; \langle \mathrm{I_r}\rangle_{-1} \;\; \langle \mathrm{I_r}\rangle_{1} \;\; \langle \mathrm{I_{L1}}\rangle_{-2} \;\; \langle \mathrm{I_{L1}}\rangle_{-1} \;\; \langle \mathrm{I_{L1}}\rangle_{0} \;\; \langle \mathrm{I_{L1}}\rangle_{1} \;\; \langle \mathrm{I_{L1}}\rangle_{2} \;\; \langle \mathrm{I_{L2}}\rangle_{-2} \;\; \langle \mathrm{I_{L2}}\rangle_{-1} \;\; \langle \mathrm{I_{L2}}\rangle_{0} \;\; \langle \mathrm{I_{L2}}\rangle_{1} \;\; \langle \mathrm{I_{L2}}\rangle_{2}\right]^T \tag{3-7}$$

The index number for a variable represents given harmonic. Since the GSSA relies on bilateral transformation the index numbers can be both positive and negative. The input is simply $\langle U_{2\times1}\rangle(t) = [\langle V_{in}\rangle_0 \;\; \langle V_{in}\rangle_0] = [V_{in} \;\; V_{in}]$ since it is assumed that V_{in} is slowly changing variable. The input matrix is

$$B_{14\times1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \dfrac{1}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \dfrac{1}{L_2} & 0 & 0 \end{bmatrix}^T \tag{3-8}$$

while the transition matrix A_{14x14} is

$$A_{14\times14}=\begin{bmatrix}
j\omega & 0 & -\frac{1}{C_r} & 0 & \frac{1}{j\pi C_r} & \frac{1}{2C_r} & -\frac{1}{j\pi C_r} & 0 & -\frac{1}{j3\pi C_r} & \frac{1}{j\pi C_r} & -\frac{1}{2C_r} & -\frac{1}{j\pi C_r} & 0 & -\frac{1}{j3\pi C_r} \\
0 & -j\omega & 0 & -\frac{1}{C_r} & \frac{1}{j3\pi C_r} & 0 & \frac{1}{j\pi C_r} & \frac{1}{2C_r} & -\frac{1}{j\pi C_r} & \frac{1}{j3\pi C_r} & 0 & \frac{1}{j\pi C_r} & -\frac{1}{2C_r} & -\frac{1}{j\pi C_r} \\
\frac{1}{L_r} & 0 & j\omega-\frac{R_r}{L_r} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{L_r} & 0 & -j\omega-\frac{R_r}{L_r} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{j\pi L_1} & \frac{1}{j3\pi L_1} & 0 & 0 & j2\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{1}{2L_1} & 0 & 0 & 0 & 0 & j\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{1}{j\pi L_1} & \frac{1}{j\pi L_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{2L_1} & 0 & 0 & 0 & 0 & 0 & -j\omega & 0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{1}{j3\pi L_1} & -\frac{1}{j\pi L_1} & 0 & 0 & 0 & 0 & 0 & 0 & -j2\omega & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{j\pi L_2} & \frac{1}{j3\pi L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & j2\omega & 0 & 0 & 0 & 0 \\
\frac{1}{2L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & j\omega & 0 & 0 & 0 \\
-\frac{1}{j\pi L_2} & \frac{1}{j\pi L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{2L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -j\omega & 0 \\
-\frac{1}{j3\pi L_2} & -\frac{1}{j\pi L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -j2\omega
\end{bmatrix} \tag{3-9}$$

The system is 14th-order. However, most of the elements are equal to zero thus the system is still useful and manageable.

3.4. Model Accuracy and Limitations

The derived model is validated with the switching model that is constructed using LT-spice software. The ideal model for a switch is used, thus the switching model is named an ideal switching model. Since the derived model is an average model, the obtained state variable's waveform will follow the envelope of the corresponding signal in the switching simulation. Also, the high frequency behavior of the system can be reconstructed from the model. The output voltage/current can be obtained with

$$\begin{aligned} V_r &= \langle \mathrm{V_r} \rangle_{-1} \cdot e^{-j\omega t} + \langle \mathrm{V_r} \rangle_{1} \cdot e^{j\omega t} \\ I_r &= \langle \mathrm{I_r} \rangle_{-1} \cdot e^{-j\omega t} + \langle \mathrm{I_r} \rangle_{1} \cdot e^{j\omega t} \end{aligned} \tag{3-10}$$

while boost inductor currents I_{L1}/I_{L2} can be calculated with

$$I_{L1} = \langle \mathrm{I_{L1}} \rangle_{-2} e^{-j2\omega t} + \langle \mathrm{I_{L1}} \rangle_{-1} \cdot e^{-j\omega t} + \langle \mathrm{I_{L1}} \rangle_{0} + \langle \mathrm{I_{L1}} \rangle_{1} \cdot e^{j\omega t} + \langle \mathrm{I_{L1}} \rangle_{2} \cdot e^{j2\omega t}$$
$$I_{L2} = \langle \mathrm{I_{L2}} \rangle_{-2} e^{-j2\omega t} + \langle \mathrm{I_{L2}} \rangle_{-1} \cdot e^{-j\omega t} + \langle \mathrm{I_{L2}} \rangle_{0} + \langle \mathrm{I_{L2}} \rangle_{1} \cdot e^{j\omega t} + \langle \mathrm{I_{L2}} \rangle_{2} \cdot e^{j2\omega t} \quad (3\text{-}11)$$

Validation of the model is examined in two cases. First case is the start-up transient when V_{in} = const. Here, the state variable waveforms will show ringing behavior before settling in the steady state. Parameters of the system are summarized in the Table 3-2. Figure 3-4 shows the relation of the V_r waveforms between the derived average model and ideal switching model at the start-up. As predicted by the theory, the V_r from the average model is indeed an envelope for the waveform in the switching model. Figure 3-5 shows the V_r voltage at the steady state. Clearly, the average model precisely follows the switching model. Conclusion is the same if the I_r current is observed in Figure 3-6 and Figure 3-7. Interesting waveforms are seen when the dynamics of the tank input current (I_t) are checked (Figure 3-8 and Figure 3-9). Green waveform represent the I_t from the switching model. Red waveform is the $\langle \mathrm{I_{L1}} \rangle_0$ current in the average model, while blue represent the total I_{L1} current in the average model. It can be seen that $\langle \mathrm{I_{L1}} \rangle_0$ accurately follows the envelope of the I_t current in the switching simulation. Examining the current ripple, it is clear that there is negligible discrepancy between average and the switching model. This confirms the assumption that the input inductor current should be modeled up to the second harmonic.

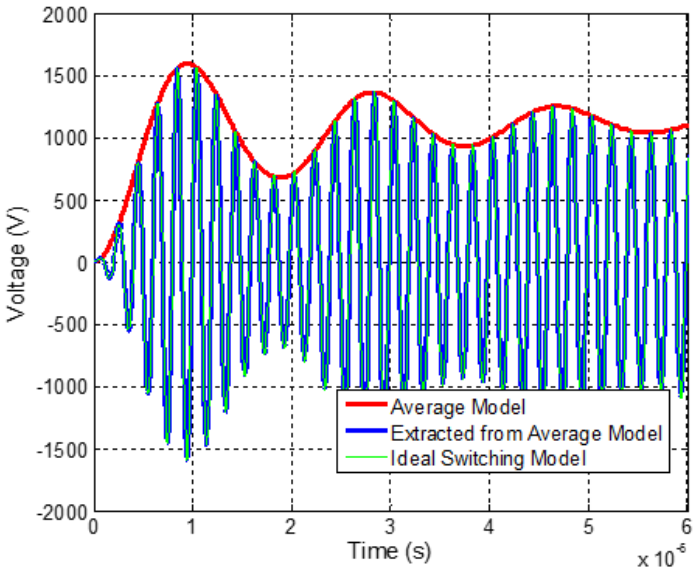


Figure 3-4. V_r at start-up.

Table 3-2. Simulation parameters for model validation.

V_{in} (V)	f_{sw}(kHz)	L_r (µH)	Q	C_r (nF)	L_{in} (µH)
350	507.66	7.05	20	14.37	125

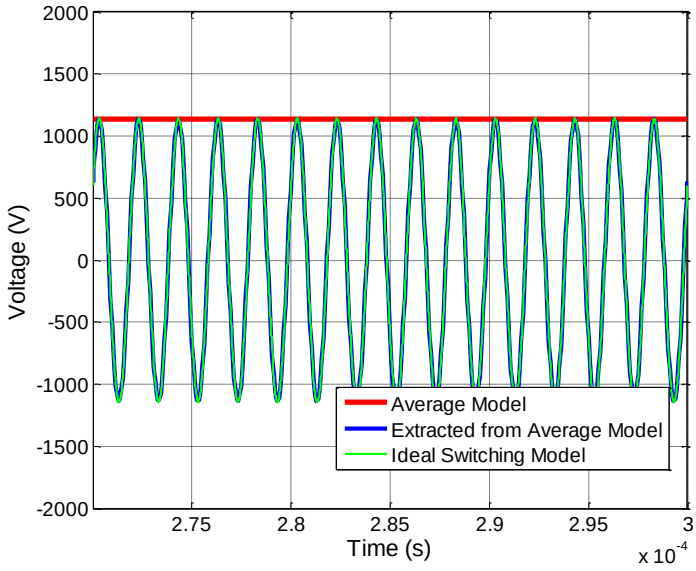


Figure 3-5. V_r at steady-state.

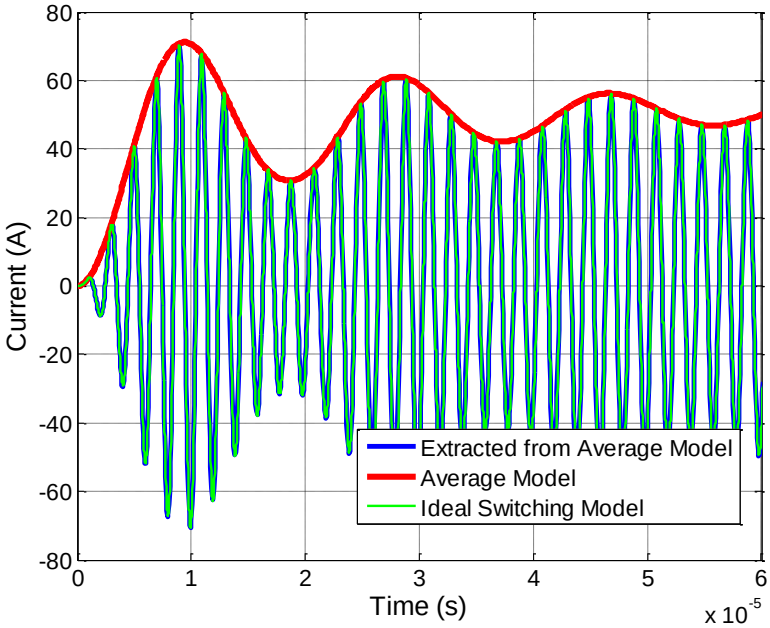


Figure 3-6. I_r at start-up.

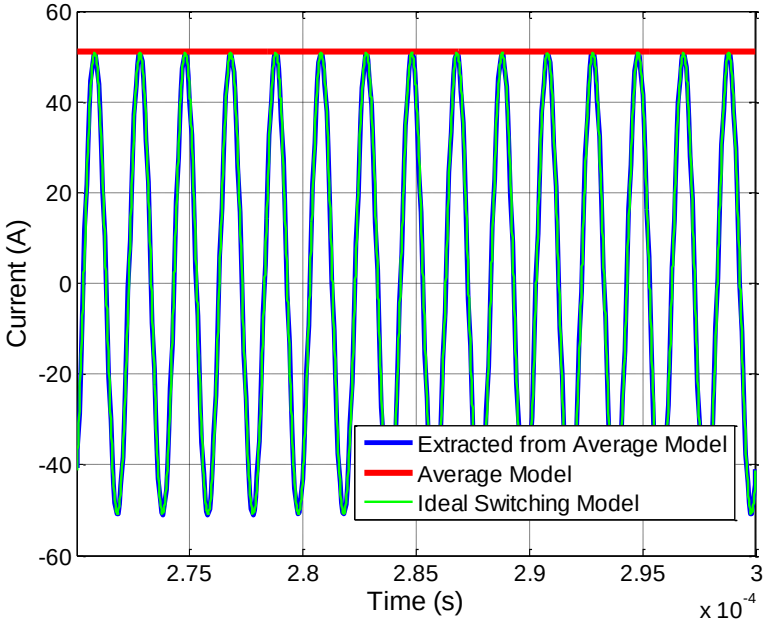


Figure 3-7. I_r at steady-state.

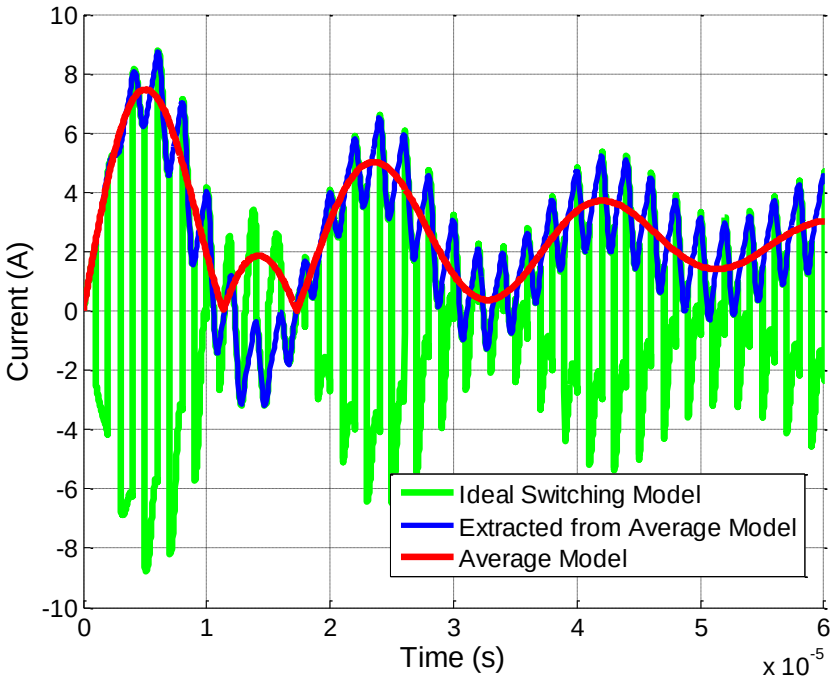


Figure 3-8. I_t(green, switching model)/I_{L1}(blue, average model) at start-up transient.

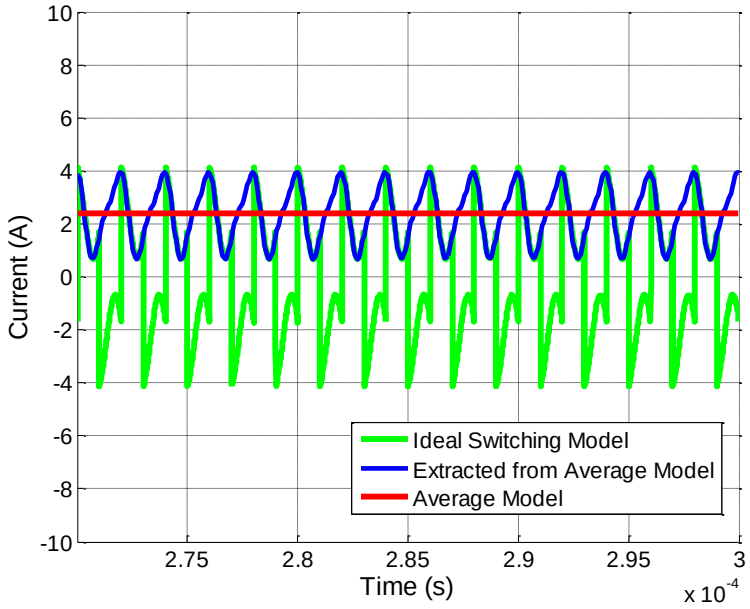


Figure 3-9. I_t(green, switching model)/I_{L1}(blue, average model) at steady-state.

Second validation example is the case when input voltage is a Hann function $V_{in} = 300V \cdot \sin^2(2\pi \cdot 10kHz \cdot t)$. In this example the Q-factor of the load is changed to 50. Figure 3-10 shows the performance of the average model for the V_r state variable. It is seen that the model is accurately predicting the switching simulation. Figure 3-11 examines the I_{L1} current. Again, the model works well.

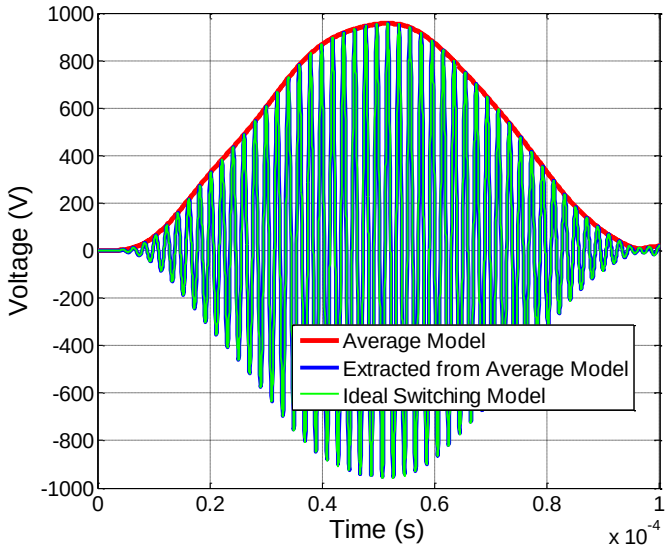


Figure 3-10. V_r waveform with low-frequency distorted envelope.

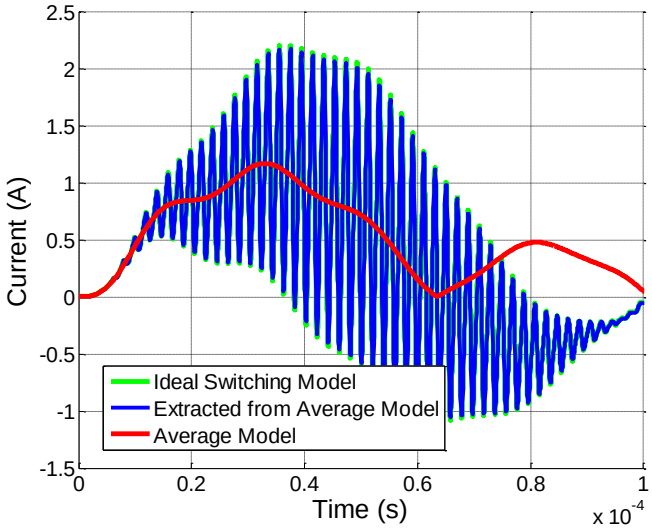


Figure 3-11. I_{L1} waveform with low-frequency distorted envelope.

Next example shows some limitations of the average model. In this example the L_{in} is reduced to L_{in} = 25 µH, while the Q-factor is kept to Q = 50. V_r waveforms are shown in Figure 3-12 for the Hann excitation. It can be noticed that at the end of the Hann cycle the average model does not predict the ringing behavior of the waveform in the switching model.

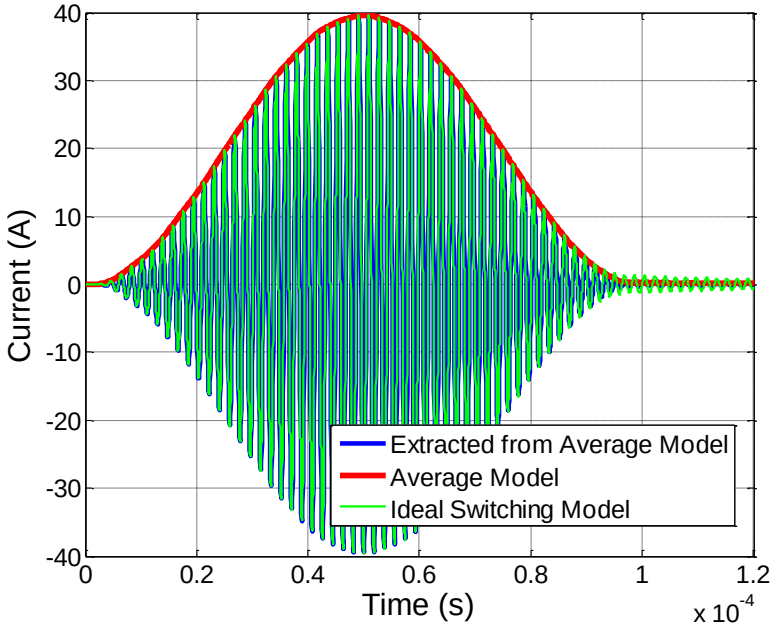


Figure 3-12. V_r waveform – model inaccuracy at the end of the cycle for L_{in} = 25 µH.

From this, the question rises how to inspect the model accuracy with some tangible parameter. Previously, the model accuracy has been inspected visually by comparing switching and average models. It is an imperative for the inverter to operate at the synchronous frequency, since the switching losses are virtually zero. Previous chapter derives the synchronous frequency, but it can also be derived from the average model, getting the same result that is given in Table 3-1, and given here as

$$\omega = \sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2} \tag{3-12}$$

where $L_q = L_r \,||\, L_{in-eq}$ and $L_{in-eq} = \frac{2L_{in}}{1+\frac{16}{9\pi^2}}$. Analogously, the resonant capacitor value C_r can be computed from the synchronous frequency,

$$C_r = \frac{1}{\omega^2 L_r}\frac{1}{1+\frac{1}{Q^2}} + \frac{1}{\omega^2 L_{in-eq}} \tag{3-13}$$

The switching simulation is set to operate at the synchronous frequency using the equation (3-12). The simulation is then checked if it indeed works at the synchronous frequency. For that purpose the phase angle φ between the switching instance $S_2(t)$ and zero-crossing of the V_r voltage is monitored. Mathematically, it can be written

$$V_r = V_{rm}\sin(\omega t + \varphi) \tag{3-14}$$

Ideally, the φ = 0 when operating at the synchronous frequency. However, synchronous frequency calculation neglects the influence of higher harmonics in the boost inductor current and output/voltage waveforms, so there will be some deviation between synchronous frequency and the computation based on the model. In terms of the phase angle φ, it will not be equal to zero but it will have some value close to zero. This non-zero value expresses the error of the model. As a quality parameter, for |φ| < 1° it will be considered that the model is very accurate. The voltage on the switch prior to the turn-on can be estimated to be $V_r = V_{rm}\sin(\varphi) \approx V_{rm}\cdot\varphi = V_{rm}\cdot\frac{1°}{360°}2\pi \approx 0.0175V_{rm}$. Thus, the switch will experience only 1.75 % of its peak voltage at the turn on. Next, when 1° < |φ| < 2° the switch model is considered to be accurate. The switch will turn on at up to 3.5 % of its peak voltage. Between 2° < |φ| < 3° the model is considered to be relatively inaccurate, with switching the voltage up to 5.25 % of its peak. The model is considered to be inaccurate when 3° < |φ|. The metrics for the evaluation of the model precision are now defined.

Most important circuit parameters that determine the distribution of harmonic currents are the loaded Q-factor and the input inductance L_{in}. Phase angle φ will be extracted from the switching simulation for various values of Q and L_{in}. The input voltage V_{in}, switching frequency and resonant inductance L_r are considered constant. Resonant capacitor C_r is changed to follow (3-12). The summary of parameters used in the simulations are given with the Table 3-3.

Figure 3-13 plots the phase angle φ against the input inductance L_{in} for various values of the Q-factor. It is seen that the model is largely accurate for high Q-factors and large inductances. The φ is increased with the increase of the Q-factor, but it decreases with the increase of the L_{in}. Also, the φ is varying less for low Q-factors. Accuracy regions are plotted in Figure 3-14. Note that y-axis is given in logarithmic scale. The desired region of operation, $10 < Q < 50$ and $50\ \mu H < L_{in} < 1000\ \mu H$ is exemplified in the figure.

Table 3-3. Parameters for a series of simulations to determine the accuracy of the model.

V_{in} (V)	f_{sw}(kHz)	L_r (µH)	Q	C_r (nF)	L_{in} (µH)
255	500	7.05	2-200	(3-12)	25 - 1000

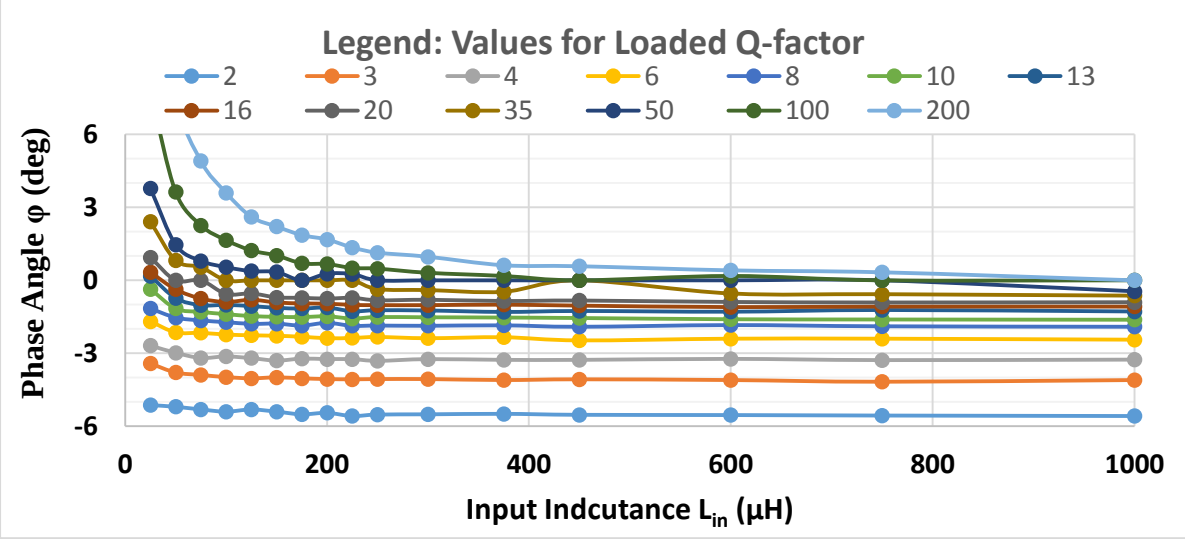


Figure 3-13. φ vs. L_{in} for various Q.

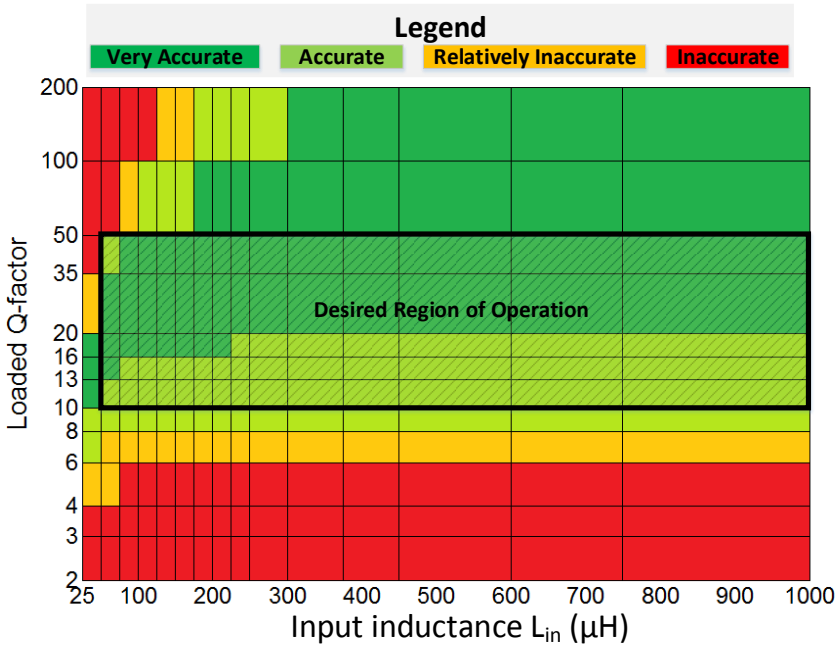


Figure 3-14. φ vs. L_{in} and Q (based on comparison of the average and the switching model).

3.5. Comparison with Low-frequency Model

Low frequency model is shown in Figure 3-15. It is derived from energy-power relationship at the input side of the inverter. The parameters of the model can be calculated from

$$\begin{aligned} L_{eq} &= \frac{L_{in}}{2} \\ C_{eq} &= \pi^2 C_r \\ R_{eq} &= \frac{2}{\pi^2} R_r \left(1+Q^2\right) \end{aligned} \tag{3-15}$$

The model works well when operated at the synchronous frequency. One should be careful when using (3-13) since the Q-factor is frequency dependent. Q-factors for natural frequency, resonant frequency and synchronous frequency are tabulated in the Table 3-4. Putting the term for the system Q-factor to (3-13), R_{eq} can be rewritten as

$$R_{eq} = \frac{2}{\pi^2}\frac{L_r}{C_r}\frac{1}{R_r}\left(1+\frac{L_r}{L_{in}}\frac{16+9\pi^2}{18\pi^2}\right) \tag{3-16}$$

Thus, (3-14) in computing the low-frequency model. When the inverter is operating away from the synchronous frequency, low-frequency model should not be used. The comparison of low-frequency model and average model is shown in Figure 3-16 for the parameters given in Table 3-5. The matching of the two models is excellent, however, the low-frequency model is unable to reconstruct the high frequency behavior of the system.

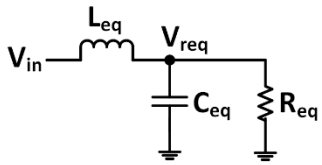


Figure 3-15. Low-frequency equivalent model of the inverter.

Table 3-4. Natural, resonant, and synchronous frequency with Corresponding Q-factors.

Natural frequency	Resonant frequency	Synchronous frequency
$\omega_n = \frac{1}{\sqrt{L_r C_r}}$	$\omega_r = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_r}{L_r}\right)^2}$	$\omega_{sy} = \sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2}$
$Q_n = \frac{\omega_n L_r}{R_r}$	$Q_r = \frac{\omega_r L_r}{R_r}$	$Q_{sy} = \frac{\omega_{sr} L_r}{R_r}$
$Q_n = \frac{1}{R_r}\sqrt{\frac{L_r}{C_r}}$	$Q_r = \frac{1}{R_r}\sqrt{\frac{L_r}{C_r} - R_r^2}$	$Q_{sy} = \frac{1}{R_r}\sqrt{\frac{L_r^2}{L_q C_r} - R_r^2}$

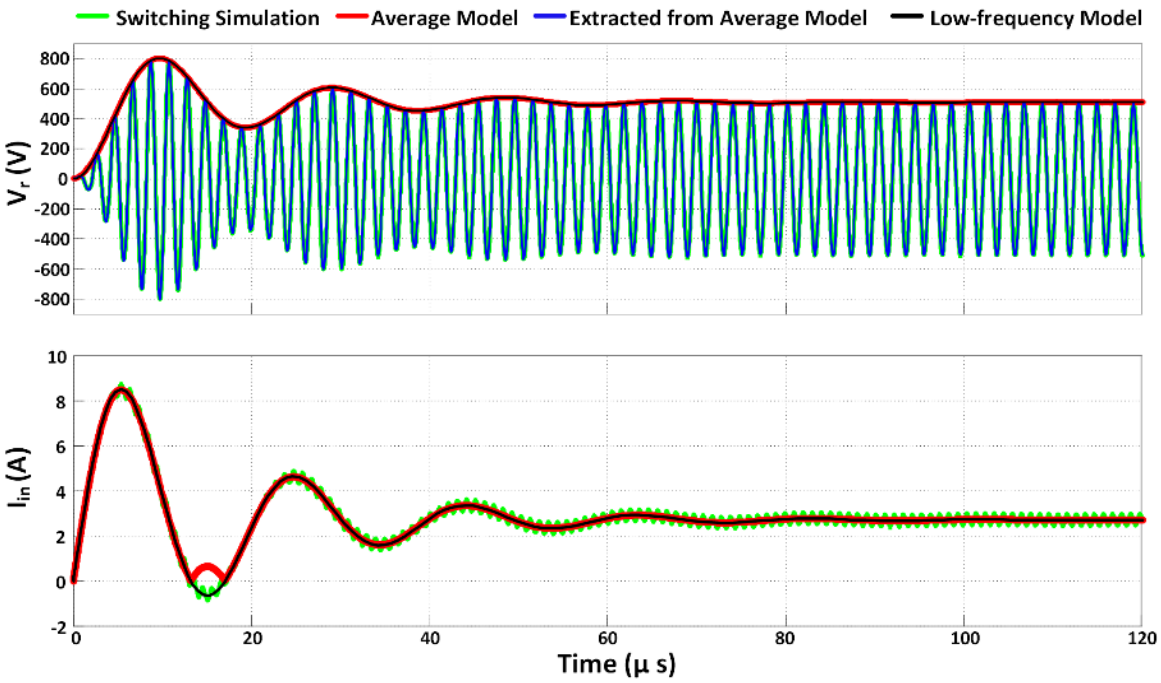


Figure 3-16. Average vs. Low-frequency model comparison for the parameters given in Table 3-5.

Table 3-5. System parameters for comparison of average and low-frequency models.

V_{in} (V)	f_{sw}(kHz)	L_r (µH)	Q	C_r (nF)	L_{in} (µH)
162	489.2	7.28	13.16	14.95	125

3.6. Validation Experiments

The developed average model was validated using switching simulation model in the section four. In this section, a boost inverter fed with the buck converter is built in order to perform model validation experiments (Figure 3-17). The buck converter is required in order to create different excitations for the inverter using a negative feedback mechanism. The feedback mechanism is forcing the input voltage of the inverter V_{in} to follow the desired reference waveform. The implementation of the buck converter is given in detail in [124]. The experiments are run for three types of input voltage waveforms. First type is a constant voltage, where the inverter is subdued to the step start-up condition. The model is validated both at the start-up and at the steady-state. Second type of input excitation is a Hann function. Two cases are examined for different carrier frequency and Hann pulse duration. The third type of excitation is the trapezoidal waveform.

In the validation process, the hardware is probed for a given excitation. From the measured waveforms the model parameters are calculated and the model is built. Finally, model is verified whether it can represent truly the real world behavior.

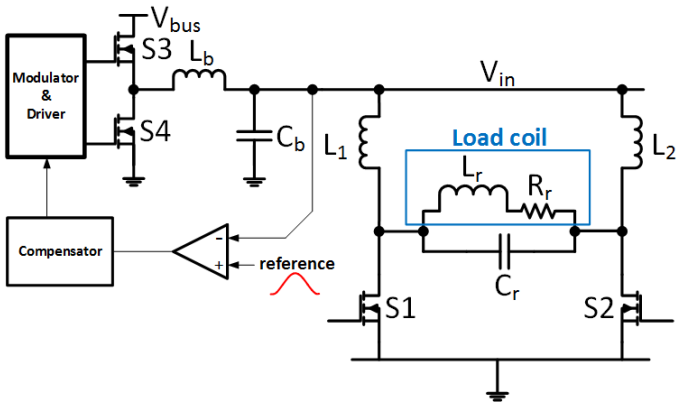


Figure 3-17. Low-frequency equivalent model of the inverter.

3.6.1. Constant Voltage Excitation: Step-up Transient Response & Steady-state

At the start-up transient the inverter starts operating with its full input voltage. The overshoot and ringing of the state variable waveforms is expected. Thus, low value of the input voltage is taken. The inverter is tuned manually to operate at synchronous frequency at 483.5 kHz for the input inductance of L_{in} = 125 μH and C_r = 14.85 nF. Parameters of the load usually vary 5-10 % with the excitation levels due to self-heating, thus they are determined in the process of model parameters calculation. The model parameters are tabulated in the Table 3-6. The model is built and compared with the measured waveforms in Figure 3-18. It is seen that the resonant voltage and current are faithfully mapped with the model. The input current I_{in} has slightly less ringing in the real circuit rather than in the model, but the difference is essentially non-important. The steady-state behavior of inverter is modeled very precisely, as shown in Figure 3-19.

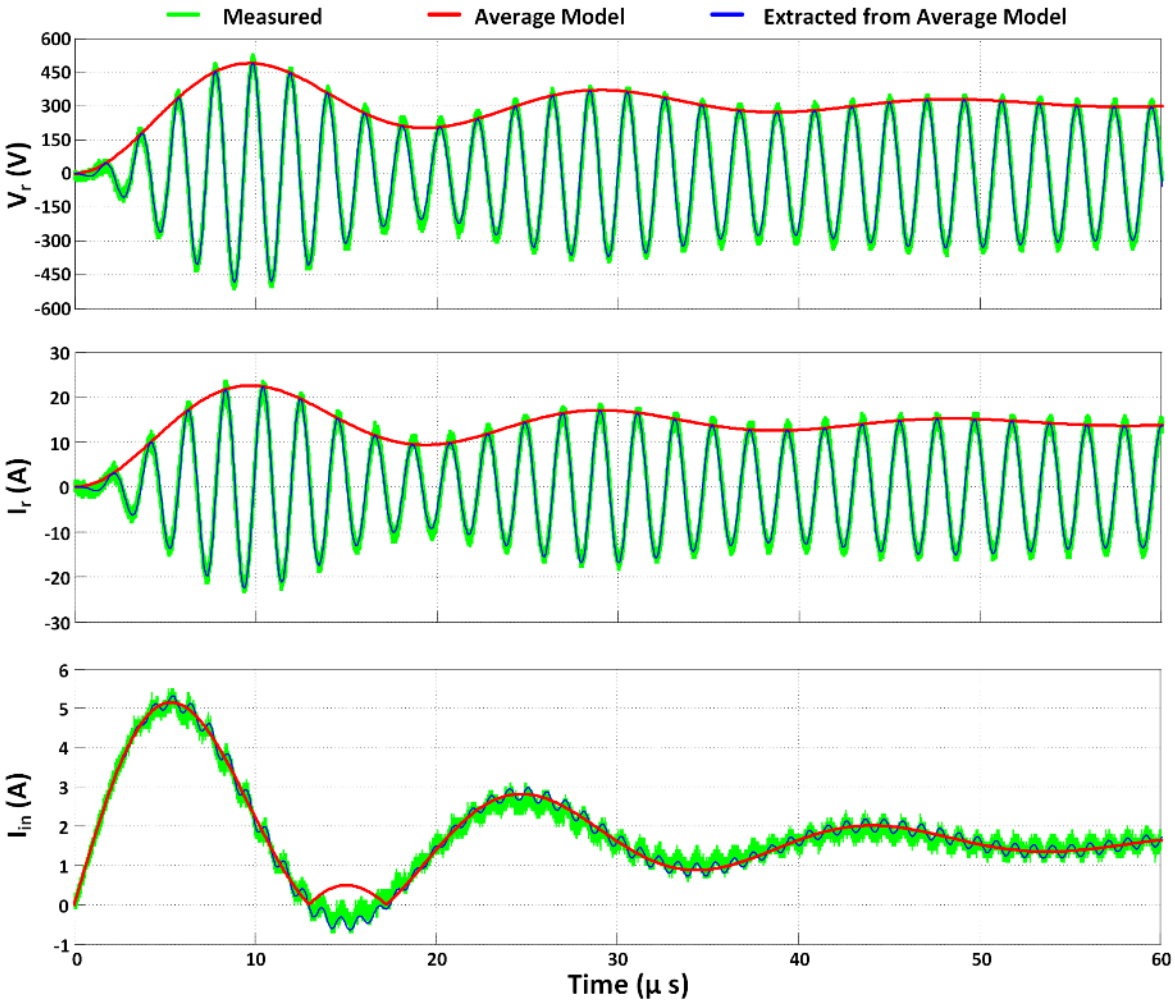


Figure 3-18. Start-up transient waveforms with V_{in} = const.

Table 3-6. The parameters of the model for the constant input voltage excitation.

V_{in} (V)	f_{sw}(kHz)	L_r (µH)	R_r (Ω)	C_r (nF)	C_{PCB} (nF)	L_{in} (µH)
99 V	483.5	6.9	1.56	14.85	14.55	125

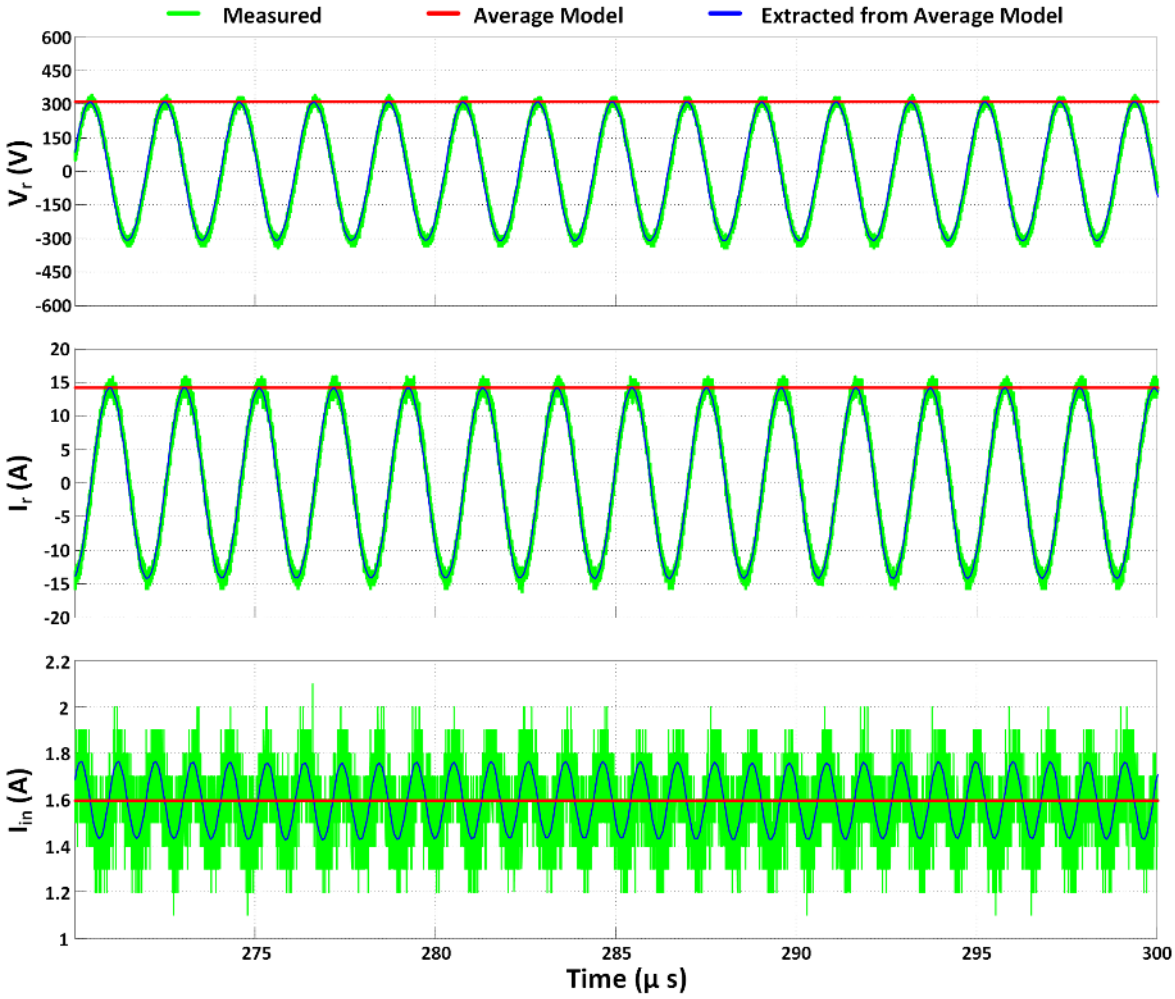


Figure 3-19. Steady-state waveforms when V_{in} constant.

3.6.2. Hann-function Excitation

Second test validation example is the Hann function, with the 100 µs pulse width and oscillation frequency of 380 kHz. The maximum input voltage is $V_{in\text{-}max}$ = 150 V with input inductance of 125 µH. All model parameters are summarized in the Table 3-7. Figure 3-20 shows the performance of the model. The mapping of the resonant voltage and current is excellent, while the input current waveform has some errors at the start and at the end of the interval.

The error occurs because the dead-time effect of the buck switches, so the Hann-shaped waveform at the input is distorted in the actual measurement.

Table 3-7. Model parameters for the Hann-function excitation of oscillation frequency of 380 kHz.

$V_{in\text{-}max}$ (V)	f_{sw}(kHz)	L_r (µH)	R_r (Ω)	C_r (nF)	C_{PCB} (nF)	L_{in} (µH)
150 V	380	7.28	0.57-1.96	24.55	24.25	125

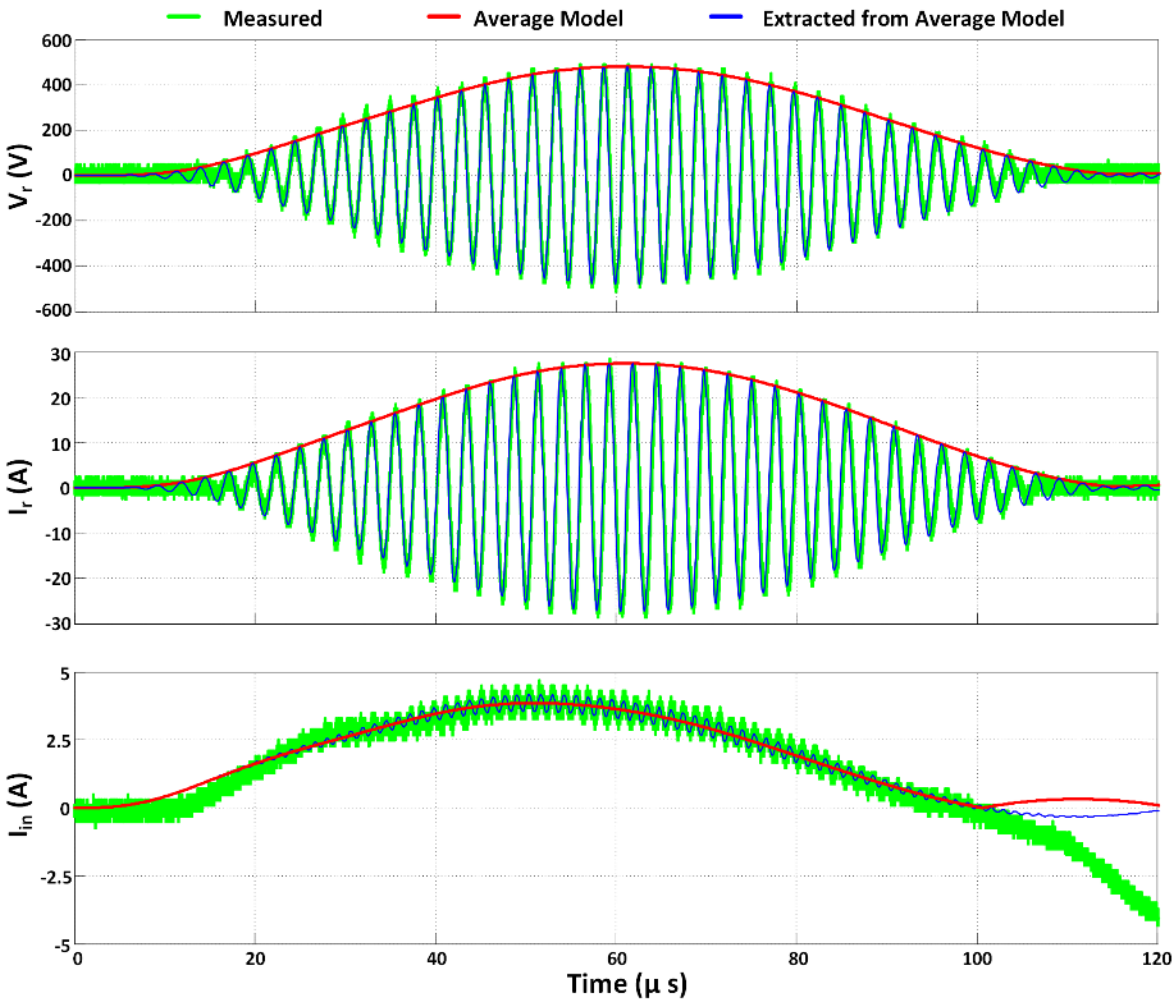


Figure 3-20. Hann-function at 380 kHz.

Following example shows the shaping of the resonant voltage and current for the Hann pulse of shorter length, 50 μs, and higher frequency of oscillation, 483.5 kHz. The parameters of the model are given in the Table 3-8. Figure 3-21 shows the mapping of the resonant voltage and current. The mapping is precise with some discrepancy at the end of the cycle. The discrepancy comes from the difference in excitations in the hardware and in the model. V_{in} in the hardware actually goes negative to deplete fast the energy stored in the inverter. The model actually uses the mathematical Hann function for the excitation.

Table 3-8. Model parameters for the Hann-function excitation of oscillation frequency of 483.5 kHz.

$V_{in\text{-}max}$ (V)	f_{sw}(kHz)	L_r (μH)	R_r (Ω)	C_r (nF)	C_{PCB} (nF)	L_{in} (μH)
93 V	483.5	7.28	1.7	14.85	14.55	125

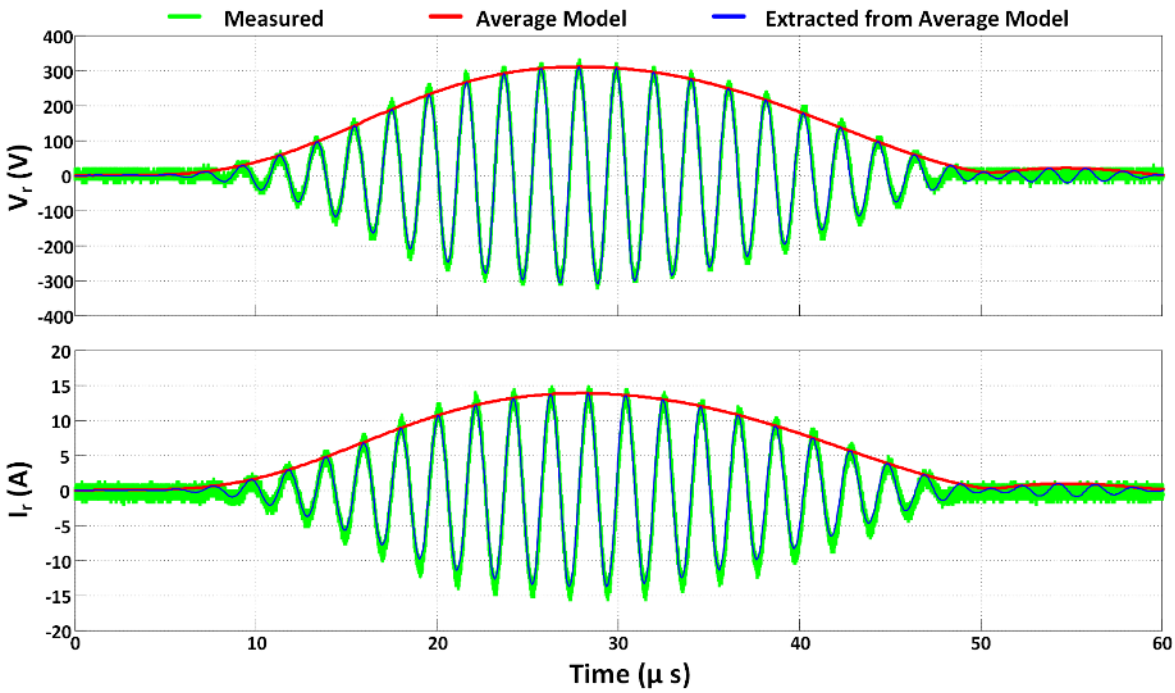


Figure 3-21. Han-function at 483.5 kHz.

3.6.3. Trapezoidal-function Excitation

The last example is the trapezoidal excitation of the inverter. The parameters of the model are given in the Table 3-9. The model precision can be seen from Figure 3-22 and Figure 3-23. If the noise in current measurements is disregarded, the waveforms mapping is excellent. Some discrepancy in the input current waveform can be attributed to the dead-time effect as noted before.

Table 3-9. Model parameters for the trapezoidal-function excitation.

V_{in} (V)	f_{sw}(kHz)	L_r (µH)	R_r (Ω)	C_r (nF)	C_{PCB} (nF)	L_{in} (µH)
155 V	483.5	7.28	1.7	14.85	14.55	125

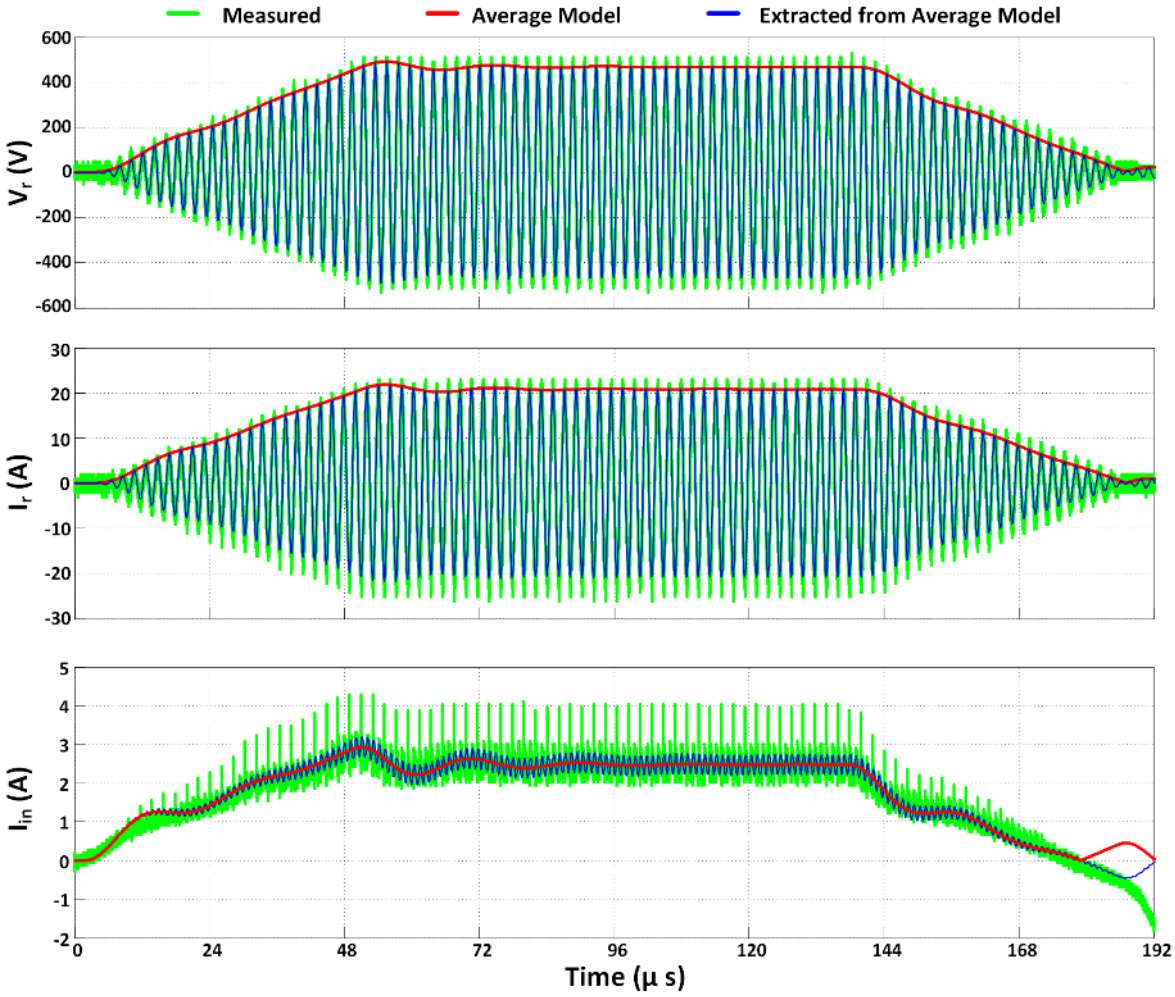


Figure 3-22. Transient waveforms when V_{in} is trapezoidal.

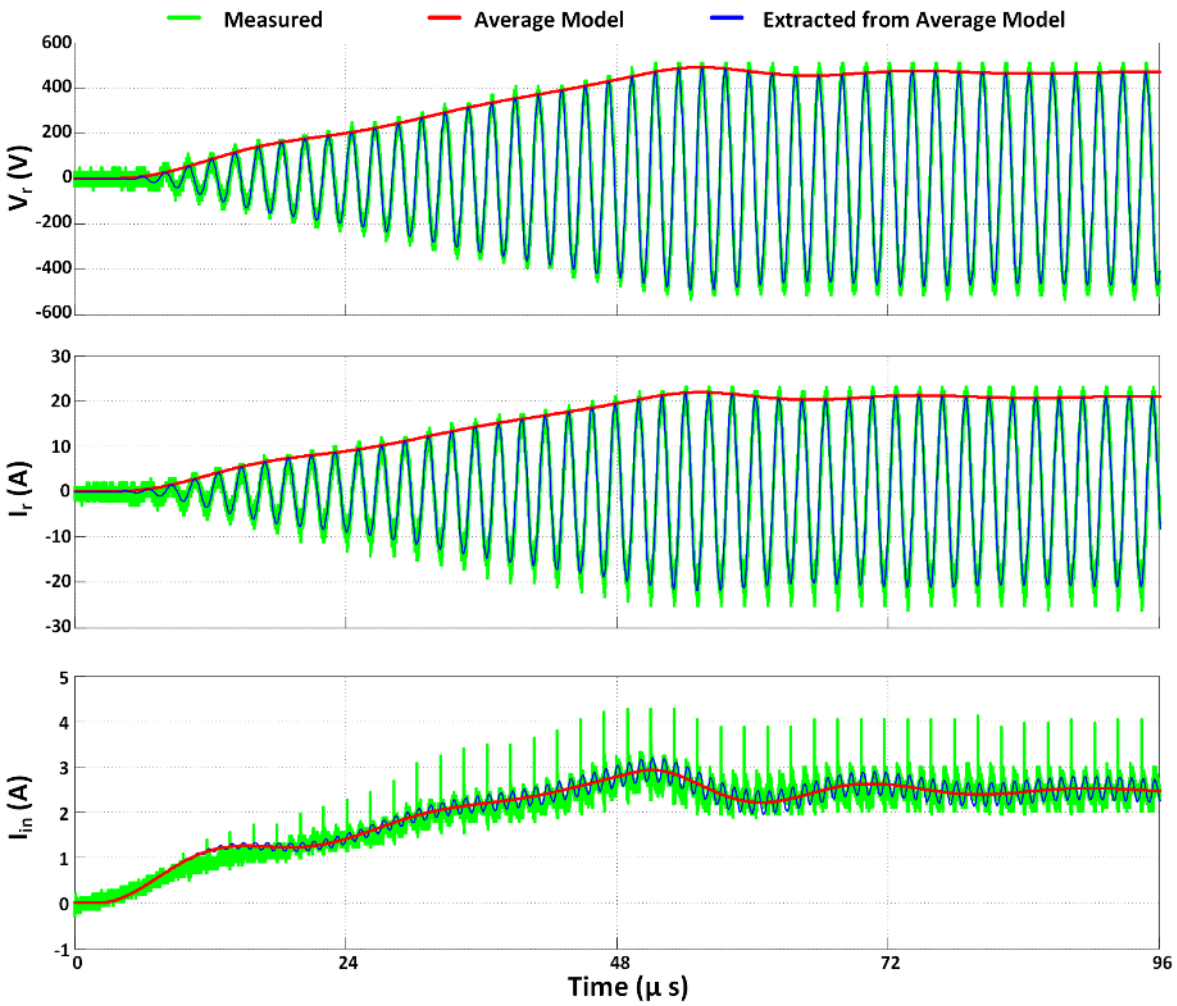


Figure 3-23. Transient waveforms when V_{in} is trapezoidal.

3.7. Conclusion

Low-frequency model of the boost inverter is unable to predict the high-frequency behavior of the inverter. In addition, the precision of the model at low frequencies is reduced when operated away from the synchronous frequency. Usefulness of frequency domain analysis is limited only for the cases when the inductance of the input inductor is very large so the current though it can be considered to be dc. GSSA model developed in this work surpasses limitations of both approaches. The model accuracy is extensively validated both with simulations and hardware measurements. It is concluded that higher frequency harmonics has to be included when either Q-factor of the load or the input inductance become sufficiently low. For example, for the load Q-factor smaller than 8, the third harmonic of the output current/voltage has to be included in the model to ensure accuracy. The derived model helps harmonic and transient analysis of the inverter, and establishes a tool to optimize the inverter design.

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Chapter 4. Active Compensation of Buck-boost Power Amplifier for Constant Frequency Operation Under Wide-load Variation

Current-fed resonant inverters are normally operated with 50 % duty-cycle, while the amplitude of the oscillations at the output is adjusted by changing the switching frequency of the inverter. The change of the switching frequency large, and can go easily around 50 %. For systems where the switching frequency is required to be constant, the additional dc/dc converter needs to be placed in front of the inverter stage to manage the amplitude of the output variable. The dc/dc stage is typically hard-switched buck converter whose efficiency is not great if operated at high switching frequency. The inverter stage is ideally tuned to the synchronous frequency for the best efficiency. Parametric variations of the load, or other circuit parameter can de-tune the inverter from the synchronization since the switching frequency is fixed. Common penalty is loss of the efficiency. Destruction of the switches is possible for cases where inverters are implemented with unidirectional voltage-blocking switches. The problem is normally solved with additional investment in hardware to construct either a compensating reactance or compensating source at the inverter's ac side that can tune inverter back to synchronization. The proposed solution in this chapter focuses on the overall efficiency, and improves both buck dc/dc stage and the inverter stage. The buck stage is extended from single-phase to two-phase buck with an inductive tank between the phases to ensure zero-voltage switching (ZVS) for all switches in the configuration. Buck phases share the total input current, resulting in improved efficiency of the buck stage. In addition, the buck stage do not utilize any output filter, since the inverter stage behaves as an equivalent buck (low-pass) filter. The boost amplifier (current-fed inverter with two input inductors) with small input inductance is selected for the inverter stage. Each of the buck phases is connected to the one of the input inductors in the boost stage. The relative phase-shift between the switching functions of the buck and the boost stages can be used to control a circulating current through one buck-phase, one input inductor, resonant tank, other input inductor, and other buck-phase. The circulating current is used to control the synchronous operation of the boost amplifier, maximizing its efficiency even for significant parametric variations of the load. All switches in the system enjoy ZVS. A prototype is constructed to verify the operation principle, and it is tested up to 750 W with efficiency of around 95 % for inductive loads with quality factor larger than ten.

4.1. Introduction

4.1.1. Current-fed Resonant Inverters with Capability to Control the Output Voltage/Current Amplitude

Common resonant inverters control the amplitude of the output variable (either voltage or current) with the change of the switching frequency [1]. The switching frequency has to be varied in the wide-range in order to adjust for different conditions at the input or output side [126]. For current-fed resonant inverters at fixed frequency, the output's amplitude is controlled by varying the input voltage. Normally, a dc/dc buck converter is put in the front of the resonant inverter for this purpose. Figure 4-1 shows the buck converter driving a boost amplifier, an inverter topology devolved in detail in Chapter 2. The topology is referred to as "cascaded buck-boost amplifier". Based on the voltage available from the bus (V_{bus}), the buck converter controls its output with the duty-cycle. Buck's output is the input to the boost amplifier (V_{in}). The output's amplitude is controlled by selecting the duty-cycle and V_{in},. Output filter of the buck, consisted of L_b and C_b, decreases the ripple of output voltage. Thus, the switching frequency of the buck can be lower than the frequency of the resonant inverter. The input inductors L_1 and L_2 of the boost amplifier are equal, $L_1 = L_2 = L_{in}$.

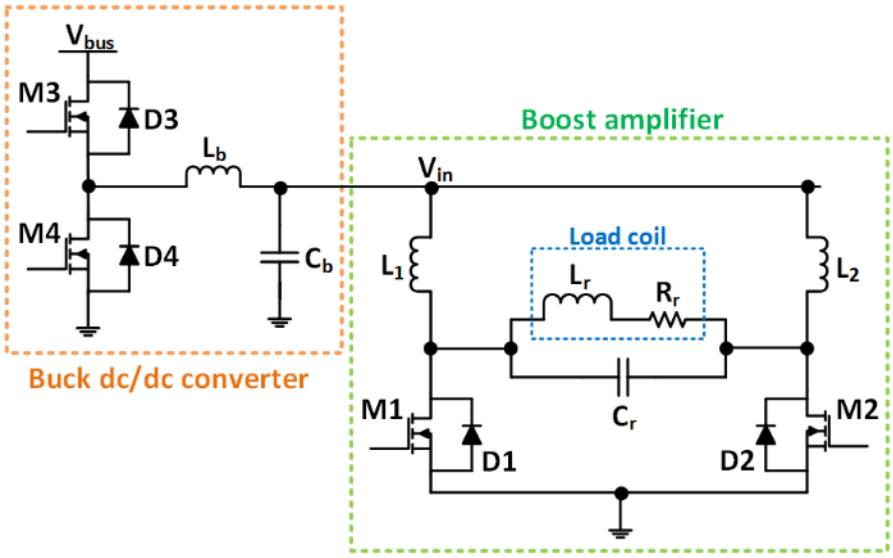


Figure 4-1. Cascaded Buck-Boost amplifier. Duty-cycle of the boost amplifier is fixed to 0.5, and boost amplifier serves to invert input dc voltage (V_{in}) to high-frequency, high-power signal at the load side. Duty-cycle of the buck converter is controlled to produce desired V_{in} voltage. By changing V_{in}, amplitude of the output is controlled. Switching frequency of buck converter does not need to equal that of the boost amplifier.

Figure 4-2 shows buck converter where the output filter is omitted [127]-[131]. The reduction of the filter is possible since the resonant inverter (boost amplifier) behaves as an equivalent buck filter (low-pass filter) at low frequency [132]. Note that now the input voltage of the boost amplifier/stage is a pulse-width modulated (PWM) signal. The switching frequency of the buck stage is close to or equal to the frequency of the amplifier in order to minimize the ripple current in the input inductors. The topology is referred to as "buck-boost amplifier", as buck and boost are merged to form a unified topology.

Circuits in Figure 4-1 and Figure 4-2 are capable to control the output's amplitude from zero to a required maximum level, since the buck processes full input power. If the input bus voltage varies, the duty-cycle can be changed to produce a constant amplitude at the output. A parallel power regulation technique [133]-[136] is an option when the output's amplitude is constrained in a narrow range around an operating point. Only a fraction of the input power is used to regulate the output, leading to a more efficient system. Drawback is the inability to regulate the output for large fluctuations of the input bus voltage [134].

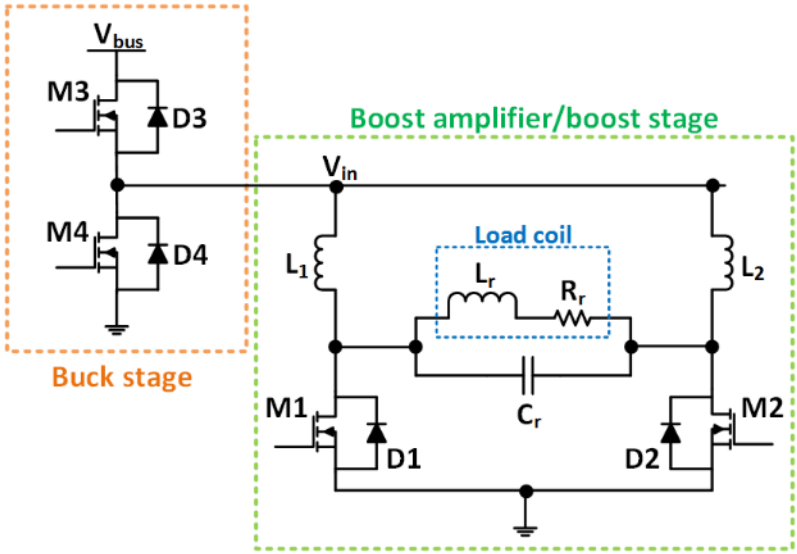


Figure 4-2. Buck-boost amplifier. Switches M1 and M2 are operated as in the cascaded buck-boost case. Switches M3 and M4 are required to operate at the frequency of the boost stage to minimize current ripple of inductors L_1 and L_2. Voltage V_{in} is a PWM signal, but the output's amplitude depends only on the average value of the V_{in} voltage.

4.1.2. Synchronous Operation of the Boost Amplifier

The synchronous frequency of the boost amplifier in Figure 4-1 is given by (2-58):

$$f_{sy} = \frac{1}{2\pi}\sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2} \tag{4-1}$$

where $L_q = L_r \,||\, L_{in-eq}$, $L_1 = L_2 = L_{in}$, and

$$L_{in-eq} = \frac{2L_{in}}{1+\frac{16}{9\pi^2}} \tag{4-2}$$

Equations (4-1) and (4-2) are valid under assumption that the load coil is highly inductive with quality-factor (Q) larger than ten. The important feature of boost amplifier topology in Figure 4-1 is that switches M1 and M2 experience small current compared to the load's one. The load's current is approximately Q times larger in magnitude.

The parameters of the synchronous frequency normally vary in a physically implemented system. The quality-factor of the load coil depends on the loading (external) conditions, temperature, and coil's current amplitude [137]. Input inductance and resonant capacitor may also vary for the same reasons. Thus, the synchronous frequency is not constant, and varies up to several percent. When the switching frequency of the boost amplifier is constant, the non-synchronous operation is eminent due to parametric variations. Lossy current spikes may occur in the switches (section 2.2). The magnitude of the spikes is clamped by the magnitude of the current in the load coil. When the load's quality-factor is small, the spikes can be tolerated since the current in the coil is only few times larger than the current present in the switches. The system efficiency is penalized, however, the benefit is employment of ZVS on switches M1/M2 [138], [139]. For highly inductive loads as in this work, the spikes are excessive and may even damage the switches [140], ruling out design for ZVS.

Most simple alternative to prevent the spikes is to put diodes in series with MOSFETs in boost amplifier topology in Figure 4-1. The diodes would have large conduction loss, while MOSFETs would be affected by the switching loss, penalizing efficiency. Snubber structure, developed in section 2.5, is helpful to mitigate the spikes and it is more efficient solution than putting the series diodes. However, it only mitigates the problem, it does not solves it. The boost amplifier can be designed to operate at zero-current switching (ZCS) [141], which also employs the series inductance with the resonant tank as the snubber structure. The method is beneficial for low input voltage applications with an

isolation transformer such as photovoltaic, where the turn-off switching losses are larger than ZVS losses due to large leakage inductance of transformer [142]. The maintenance of desired ZCS condition requires a change of the switching frequency. The series inductance oscillates with the output capacitance of the M1/M2 transistors, requiring snubbing that relates to increased loss. This work considers input voltage of 200 V- 300 V to the boost amplifier, and does not utilize isolation transformer. The ZCS method is thus unsuitable even if the switching frequency is made constant and snubbing loss kept low.

The boost amplifier is commonly designed so the switching frequency is dynamically tuned to lock to the synchronous frequency. The versions using a phase-locked loop [130] or self-tuning circuits [143]-[146] are developed. Still, buck stage is required to control the amplitude of the output. Variable switching frequency is not desirable as it complicates design, and it is forbidden by system specifications.

Controllable reactance can be added to the resonant tank to compensate the synchronous frequency in (4-1), so it equals to the switching frequency. Reconfigurable matching circuit method uses an array of discrete inductors, capacitors, and switches/circuit breakers to tune/detune resonant converters [147]-[150]. Large number of components is added, increasing size, cost, and complexity. The tuning is obtained at discrete points, making unfavorable solution to the problem. Variable inductor can be implemented by saturating the magnetic core [151]-[154], but losses, control complexity, and reduced bandwidth limit the use of this approach [155]. Phase-controlled reactance, a variety invented to compensate the reactive energy on the power grid [156]-[157], is gaining popularity in resonant converters [158]-[159], particularly in wireless power transfer [160]-[164]. To implement the phase-controlled reactance, an inductor or capacitor is paired with a bidirectional voltage-blocking switch whose switching pattern controls the equivalent impedance of the reactance. Both inductive and capacitive controlled reactance versions can compensate the resonant tank, with the latter being preferable due to ZVS turn-on condition on the switch. Resistance compressors are able to suppress variations of the load resistance, and [165]-[166] reports solution for dc/dc converters. The concept is extended to dc/ac conversion in [167], using phase-controlled reactance. Controllable reactance methods, although effective, add complexity and cost to the system.

Active compensation method requires a master converter for power processing and auxiliary converter for compensation of required variable, which is in most cases (for dc/dc conversion) ripple of an inductor or capacitor [168]. The parallel processing technique in [134] is an example applicable to boost amplifier. Similarly as for controllable reactance methods, added complexity and cost are associated with active compensation method.

In voltage-fed resonant inverters, multi-phase/interleaved topologies are used to scale up the output power while using phase-shift control and fixed frequency operation [169], [170]. Phases share the total power so the interleaving method is convenient for systems with high output power [171]. The difficulty is how to apply the method to current-fed resonant inverter without using inter-phase coupling transformer as in [172]. Moreover, boost transistors have to synchronize switching with zero-crossing of the output voltage, having the applicability of the concept unclear.

The difficulty with buck-boost topology is that buck-stage is required to control the output voltage magnitude, while additional circuitry is required to compensate load variations if the series diodes with M1/M2 are absent. Chapter 2 describes the behavior of boost amplifier at the steady-state when input inductance is low. It was shown that a circulating current at the fundamental frequency flows through input inductors and the resonant tank. This circulating current has strong effect on the synchronization, and can be harnessed for synchronous operation of the boost amplifier under parametric variations of the load.

Multi-phased/interleaved approach for the buck-stage is proposed in the next section to harness and control the circulating current. The relative phase-shift between the switching functions of the buck and the boost stage is used control the synchronous operation. The buck has now two-fold function, it controls the output voltage amplitude and ensures the synchronous operation of the boost amplifier under parametric variations of the load. The proposed circuit is an extension of topology in Figure 4-2, consisting of two-phase buck and an inductive tank between the phases to allow ZVS on all switches in the buck stage [173]-[175]. The efficiency of the buck-stage greatly benefits from multi-phase implementation, since switching losses are decreased with ZVS. Power loss is further reduced since the phases share the processed power. The result is an efficient, and adaptable topology to both bus voltage and load variations.

4.1.3. Two-phase Buck-Boost Amplifier Topology

The buck-boost topology in Figure 4-2 can be extended to the two-phase buck stage (Figure 4-3). Each phase operates with the same duty-cycle, but with adjustable relative phase delay of the gating PWM functions. As result, boost stage sees PWM voltages V_{in1} and V_{in2} at its inputs. The average voltage of V_{in1} equals the one of V_{in2}. Between the two phases an inductive tank can be placed so the ZVS can be reached for all buck switches. The phase-shift between the two buck phases control the amount of reactive current in the inductive tank, so sufficient current exist to spur ZVS condition in all switches [173]. The buck phases share the input current, reducing the conduction loss. More phases than two could be implemented, which would further reduce the conduction loss, and more importantly, the switching frequency of the buck stage can be reduced.

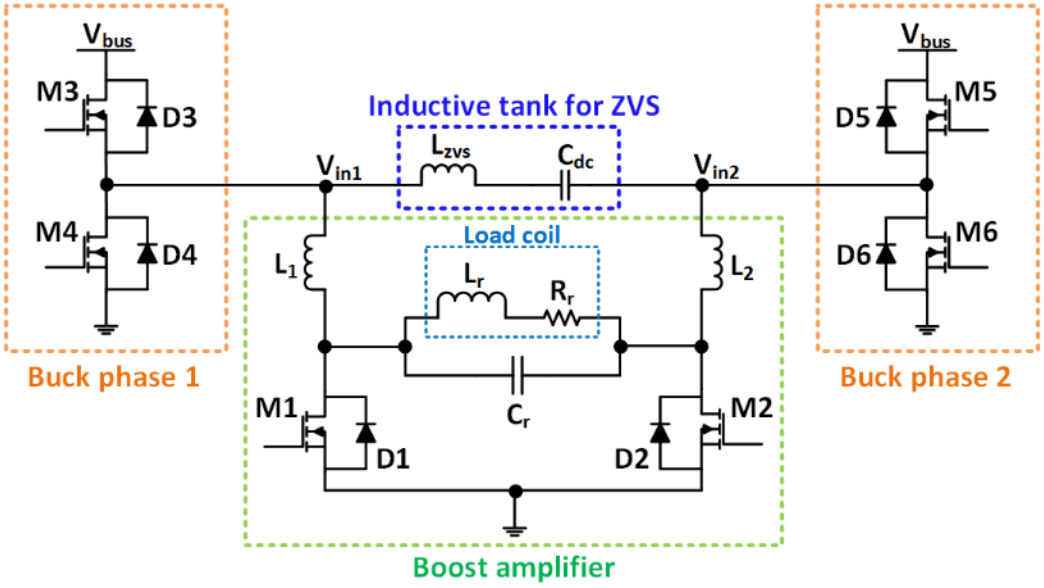


Figure 4-3. Two-phase buck-boost amplifier. Switches M1 and M2 are operated as in the cascaded buck-boost case. Switches M3, M4, M5, and M6 are operated at the frequency of the boost stage. Relative phase-shift between switching functions of buck phases 1 and 2 controls ZVS condition on buck switches. Relative phase-shift between switching functions of buck phases and the boost amplifier control the synchronous operation of the boost amplifier. Voltages V_{in1} and V_{in2} are PWM signals with the same duty-cycle. The average voltage of V_{in1} and V_{in2} correlates with the output voltage magnitude.

In order to demonstrate the capability of the multi-phase buck-boost topology, the two-phase buck-boost in Figure 4-3 is examined in this chapter. The extension of the buck-stage is an obvious improvement of the existing topology. However, when the buck-stage is operated at the same switching frequency as the boost-stage, a compensating current can be injected to the resonant tank in order to control the zero-crossing of the resonant tank's voltage. The compensating current is controlled with the relative phase-shift between the switching functions of the buck and the boost stage, and it flows through the buck phase 1, inductor L_1, resonant tank, inductor L_2, and buck phase 2 The synchronization of the boost amplifier can be achieved even for few percent change of the synchronous frequency due to parametric variations of the circuit.

A capability for compensation is a strong function of the boost amplifier's input inductance L_{in}. It limits the amount of the compensating current, which has dominant fundamental frequency component. The compensation method was not explored before since the input inductance is typically designed to be very large, often in mili-Henry range. Thus, a theory how to reduce the input inductance by the order of magnitude and operate at the synchronous frequency (presented in Chapter 2) had to precede in order for the compensation method to be explored. A topology with inversely-coupled current-splitting transformer [132] is often preferred instead of one in Figure 4-2 for simpler design in case of small input inductance. However, the splitting transformer would suppress the circulation of the compensating current at the fundamental frequency, and preventing use of the compensation strategy.

The compensation is complex mathematical problem that has to include harmonics generated by the switching function of the buck stage and their propagation to the resonant tank. The generalized state-space averaging (GSSA) [176] model of the boost amplifier, developed in Chapter 3, is used as a tool in the analysis. The proposed solution is non-obvious but simple and effective hardware solution to the boost amplifier's fixed-frequency, synchronous-operation problem.

The proposed compensation of the boost amplifier has significant advantages:

- Enables constant frequency operation.
- Boost amplifier operates at synchronous condition even for significant parametric variations.
- All buck switches enjoy ZVS. Transistors in the boost stage does not experience switching loss.
- The output power is controlled with the input voltage to the system and duty-cycle of the buck.
- Current stress may be reduced, improving efficiency.

- The compensation of the boost amplifier is “for free” since multi-phase buck should be pursued for efficiency improvement of the buck-stage alone.

4.1.4. Methodology and Chapter Organization

The buck stages produce PWM voltage signals at the inputs of boost amplifier. PWM signals for an arbitrary duty-cycle can be represented as a sum of infinite number of harmonic components. In order to show that a compensation conditions exist for the boost amplifier, the compensation problem is solved first for the simplified case where input voltages have only dc and fundamental components. The solution is found afterwards for the proposed circuit in Figure 4-3.

This chapter is divided into eight sections. Second section describes in detail the operation of the boost amplifier at synchronous and non-synchronous condition. Ideal switches are used. Simulation waveforms are given and the two conditions are compared. Third section explores a simplification of the compensation circuit in Figure 4-3, where the each of the buck phases is modeled as a sum of dc and fundamental frequency voltage sources. This compensation case is named as “sinusoidal compensation”, since two phase-shifted sinusoidal voltage sources are utilized. In computation of the synchronous condition for the boost amplifier, a topology with ideal switches is assumed so the GSSA model from Chapter 3 can be used.

Fourth section analyses the idealized representation of the circuit in Figure 4-3, where switches are ideal and the buck phases are replaced with equivalent PWM voltage sources with corresponding on-level, duty-cycle, and phase-shift for given frequency. Mathematical dependence connecting the PWM parameters and synchronous operation is derived, and validated in simulation.

Section five describes the design and implementation of the buck-boost amplifier. Buck and boost stages are implemented on independent printed circuit boards (PCBs), and they are connected with a cable. Buck stage may experience hard-switching, and therefore attention is put to minimize switching power and gate driver loop and associated parasitic inductances. The hardware tests of the amplifier are given in section six. Constant frequency operation is confirmed for load parametric variations. Constant output magnitude operation is confirmed for varying bus voltage and adjusting the duty-cycle. The amplifier for power level of 750 W and efficacy of 95 % for switching frequency of 480 kHz, input voltage in 450 V- 600 V range, and output voltage magnitude of 700 V.

4.2. Synchronous and Non-Synchronous Operation of Idealized Boost Amplifier

The operation of boost amplifier is demonstrated with an equivalent circuit employing ideal bidirectional voltage-blocking switches (Figure 4-4, major circuit variables are labeled). The complexity of the analysis is greatly reduced, and utilization of the GSSA circuit model developed in Chapter 3 is allowed. The circuit in Figure 4-4 is simulated in LT spice to show waveforms of the main variables for both synchronous and non-synchronous operation of the boost amplifier. Input voltage of the amplifier is dc value, and it is set to V_{in} = 255 V. Switching frequency is f_{sw} = 500 kHz, and it equals to the synchronous frequency for parameters $L_1 = L_2$ = 125 μH, L_r = 7.27 μH, C_r = 14.38 nF, and R_r = 1.14 Ω. The parameters of the amplifier are summarized in Table 4-1. The switching functions $S_1(t)$ and $S_2(t)$ are defined as:

$$S_1(t) = \begin{cases} 0, & 0 \le t < \dfrac{T}{2} \\ 1, & \dfrac{T}{2} \le t < T \end{cases} \text{ and } S_2(t) = 1 - S_1(t) = \begin{cases} 0, & 0 \le t < \dfrac{T}{2} \\ 1, & \dfrac{T}{2} \le t < T \end{cases} \tag{4-3}$$

Figure 4-5 shows simulation waveforms of the circuit from Figure 4-4 for both synchronous and non-synchronous operation. Synchronous operation is set by selecting the load resistance R_r to $R_{r\text{-}1}$ = 1.14 Ω. Corresponding simulation waveforms are colored in blue. Switching functions are same for both cases. Non-synchronous operation is set by setting load resistance R_r to $R_{r\text{-}2}$ = 2.28 Ω. Corresponding simulation waveforms are colored in red. Non-synchronous operation is observed as the M1 switch's voltage waveform (V_a) will have negative values, and the switch turn-on does not happen at zero Volts. The switch M1 is turned-on at 90 V. Resonant voltage V_r and current I_r are sine-waves with amplitudes of V_{rm} = 800 V and I_{rm} = 35 A for both simulation cases.

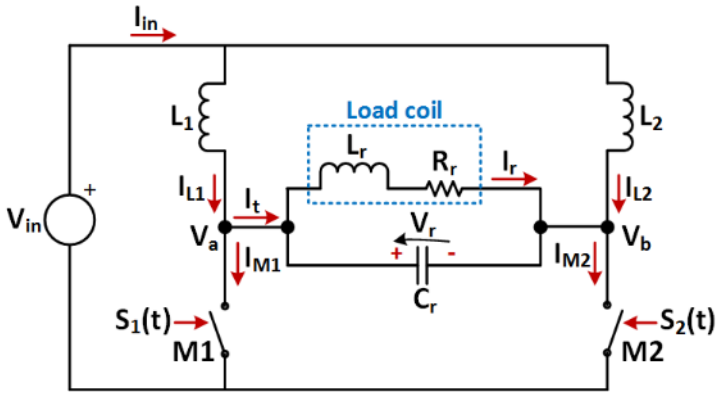


Figure 4-4. Boost amplifier with ideal bidirectional voltage-blocking switch. Input inductors have equal value, $L_1 = L_2 = L_{in}$.

Table 4-1. Circuit parameters of idealized boost amplifier from Figure 4-4. Switching functions are given with (4-3).

f_{sw} (kHz)	V_{in} (V)	L_1 (μH)	L_2 (μH)
500	255	125	125
L_r (μH)	C_r (nF)	R_{r-1} (Ω)	R_{r-2} (Ω)
7.27	14.38	1.14	2.28

The synchronous frequency depends on the current harmonics of the input inductors. It has been shown in Chapter 2 that harmonics higher than second can be neglected, and that input inductors currents can be written as:

$$\begin{aligned} I_{L1}(t) &= I_{L1}^{(0)}(t) + I_{L1}^{(1)}(t) + I_{L1}^{(2)}(t) \\ I_{L2}(t) &= I_{L2}^{(0)}(t) + I_{L2}^{(1)}(t) + I_{L2}^{(2)}(t) \end{aligned} \tag{4-4}$$

where $I_{L1}^{(n)}(t) / I_{L2}^{(n)}(t)$ are the nth harmonic component of I_{L1}/I_{L2} currents. Since switching functions $S_1(t)$ and $S_2(t)$ are complementary, the harmonics in inductors L_1 and L_2 relate as:

$$\begin{aligned} I_{L1}^{(0)}(t) &= I_{L2}^{(0)}(t) = I_L^{(0)}(t) \\ I_{L1}^{(1)}(t) &= -I_{L2}^{(1)}(t) = I_L^{(1)}(t) \\ I_{L1}^{(2)}(t) &= I_{L2}^{(2)}(t) = I_L^{(2)}(t) \end{aligned} \tag{4-5}$$

The current flowing though switch M1 is then:

$$I_{M1}(t) = \begin{cases} 0, & S_1(t) = 0, \quad 0 \le t < \dfrac{T}{2} \\ 2 \cdot \left(I_L^{(0)}(t) + I_L^{(2)}(t) \right), & S_1(t) = 1, \quad \dfrac{T}{2} \le t < T \end{cases} \tag{4-6}$$

It is seen that the fundamental frequency current of the input inductors, $I_L^{(1)}(t)$, does not flow though the switches. Instead, the $I_L^{(1)}(t)$ circulates between inductors L_1, L_2, and the resonant tank. The prominent influence on synchronous frequency comes from the fundamental harmonic component $I_L^{(1)}(t)$. The control of $I_L^{(1)}(t)$ is beneficiary, since it does not add to the conduction loss of M1/M2 switches while synchronous operation of the amplifier can be achieved for load's parametric variation. The output voltage of the resonant tank has different mathematical representation, given with

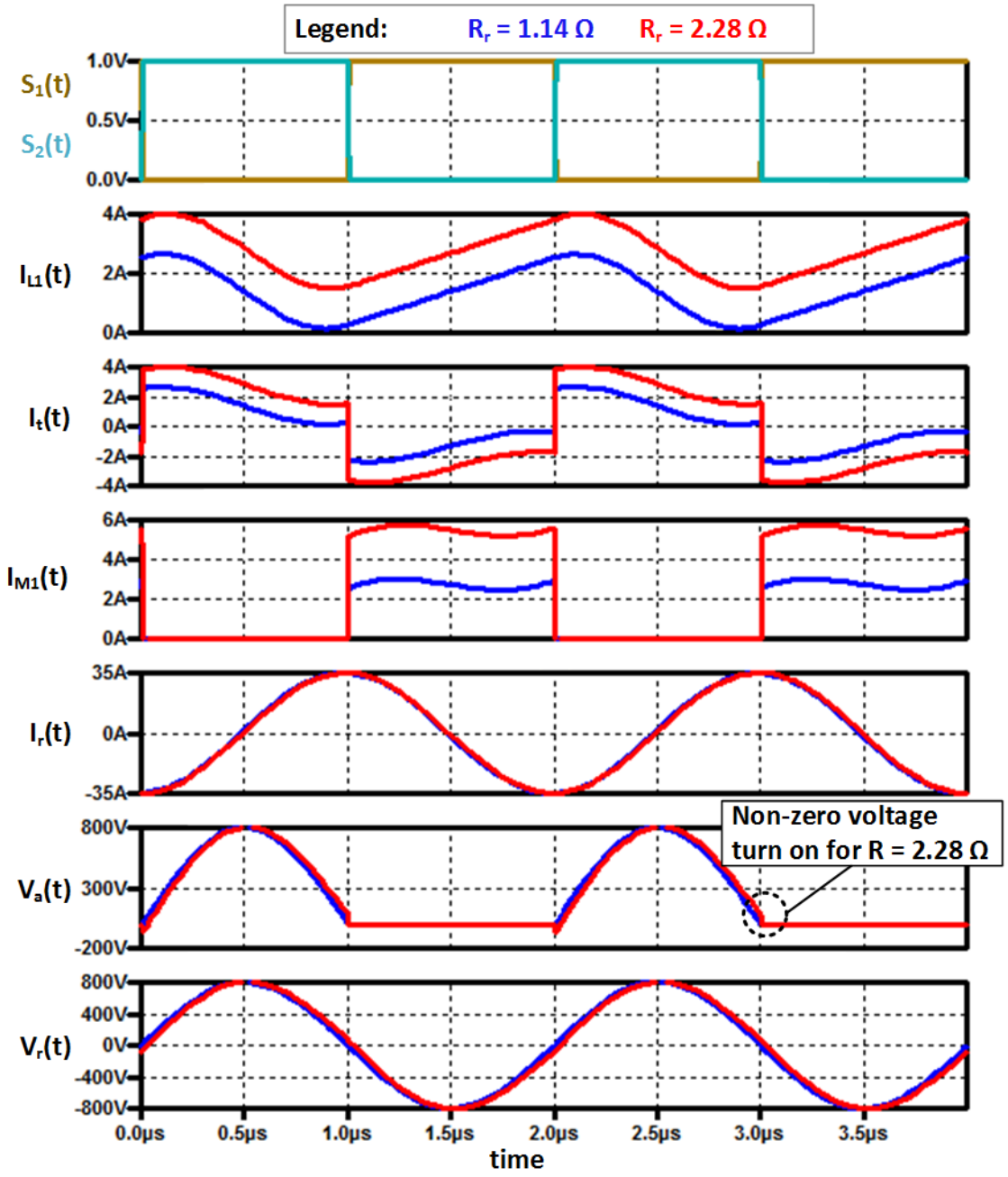


Figure 4-5. Simulation waveforms of the idealized boost amplifier from Figure 4-4. Load resistance is varied to show synchronous operation (in blue) for R_r = 1.14 Ω, non-synchronous operation (in red) for R_r = 2.28 Ω. Non-synchronous operation is observed when a switch is turned on while having non-zero voltage applied on it.

$$V_r(t) = V_a(t) - V_b(t) = V_{rm}\sin(\omega t + \varphi) = V_{rs}\sin\omega t + V_{rc}\cos\omega t \quad (4\text{-}7)$$

where V_{rm} is the amplitude of oscillations, φ is relative phase delay from the switching function $S_2(t)$, V_{rs} and V_{rc} are the sine and cosine component amplitudes. The synchronous operation of the boost amplifier is described with either

$$\varphi = 0 \text{ or } V_{rc} = 0 \quad (4\text{-}8)$$

The latter condition will be used to represent synchronous operation since it simplifies the math computations.

4.3. Sinusoidal Compensation

4.3.1. Proposed Topology for Sinusoidal Compensation

The additional sinusoidal voltage sources V_1 and V_2 are proposed (Figure 4-6) in order to control the fundamental frequency harmonic currents in inductors L_1 and L_2, and consequently the synchronous operation. The dc source V_{in} sets the amplitude of the output voltage, same as for the circuit in Figure 4-4. The active power to the load is supplied by the source V_{in}. Sources V_1 and V_2 only control the synchronous operation of the amplifier and they process insignificant amount of the active power.

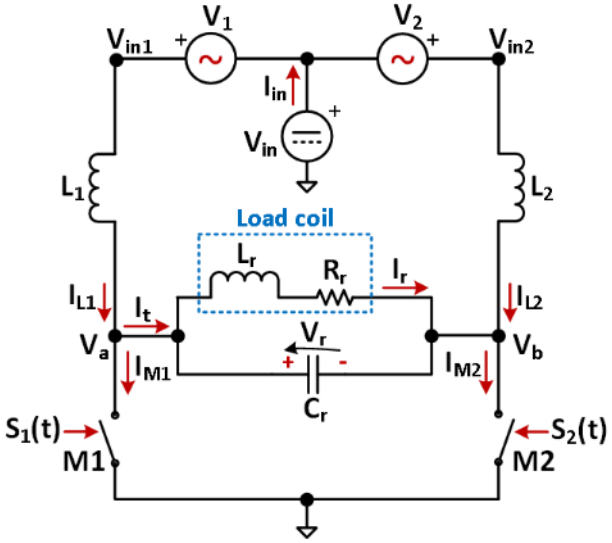


Figure 4-6. Circuit schematics for sinusoidal compensation of the boost amplifier. Sources V_1 and V_2 control a circulating current at the fundamental frequency through L_1, L_2, and the resonant tank. The circulating current is used to control the zero-crossing of the resonant tank's voltage, $V_r(t)$.

The sources V_1 and V_2 are described as

$$V_1 = V_{1m}\sin(\omega t + \Psi_1) \text{ and } V_2 = V_{2m}\sin(\omega t + \Psi_2) \tag{4-9}$$

where the amplitudes are equal $V_{1m} = V_{2m} = V_{cm}$, and relative phase delays are shifted by $\Psi_2 - \Psi_1 = \pi$ for purpose of balancing the circuit.

4.3.2. GSSA Model of Boost Amplifier with Sinusoidal Compensation

The circuit in Figure 4-6 is represented with fourteenth order GSSA model described with:

$$\frac{d}{dt}\langle X_{14\times1}\rangle(t) = A_{14\times14}\cdot\langle X_{14\times1}\rangle(t) + B_{14\times6}\cdot\langle U_{6\times1}\rangle(t) \tag{4-10}$$

The states, as in Chapter 3, are given with

$$\langle X_{14\times1}\rangle(t) = \left[\langle \mathrm{V_r}\rangle_{-1} \;\; \langle \mathrm{V_r}\rangle_{1} \;\; \langle \mathrm{I_r}\rangle_{-1} \;\; \langle \mathrm{I_r}\rangle_{1} \;\; \langle \mathrm{I_{L1}}\rangle_{-2} \;\; \langle \mathrm{I_{L1}}\rangle_{-1} \;\; \langle \mathrm{I_{L1}}\rangle_{0} \;\; \langle \mathrm{I_{L1}}\rangle_{1} \;\; \langle \mathrm{I_{L1}}\rangle_{2} \;\; \langle \mathrm{I_{L2}}\rangle_{-2} \;\; \langle \mathrm{I_{L2}}\rangle_{-1} \;\; \langle \mathrm{I_{L2}}\rangle_{0} \;\; \langle \mathrm{I_{L2}}\rangle_{1} \;\; \langle \mathrm{I_{L2}}\rangle_{2}\right]^T \tag{4-11}$$

where the symbol in the bracket represent a variable, and the index number represent a harmonic component. The transition matrix A_{14x14} is unchanged, and it is given with (3-9). The inputs to the system include all harmonic components present in the nodes V_{in1} and V_{in2} in Figure 4-6. The input matrix $\langle U_{6\times1}\rangle(t)$ is:

$$\langle U_{6\times1}\rangle(t) = \left[\langle V_{in1}\rangle_{-1} \;\; \langle V_{in1}\rangle_{0} \;\; \langle V_{in1}\rangle_{1} \;\; \langle V_{in2}\rangle_{-1} \;\; \langle V_{in2}\rangle_{0} \;\; \langle V_{in2}\rangle_{1}\right]^T \tag{4-12}$$

where the matrix components are equal to

$$\langle V_{in1}\rangle_0 = \langle V_{in2}\rangle_0 = V_{in},\ \langle V_{in1}\rangle_{-1} = \langle V_1\rangle_{-1},\ \langle V_{in1}\rangle_1 = \langle V_1\rangle_1,\ \langle V_{in2}\rangle_{-1} = \langle V_2\rangle_{-1}, \text{ and } \langle V_{in2}\rangle_1 = \langle V_2\rangle_1 \tag{4-13}$$

The $\langle V_1\rangle_{-1}$, $\langle V_1\rangle_1$, $\langle V_2\rangle_{-1}$, and $\langle V_2\rangle_1$ are harmonic components of sources V_1 and V_2. Based on xx and xx, they are equal to

$$\langle V_1\rangle_{-1} = -\frac{V_{cm}}{2j}e^{-j\Psi_1},\ \langle V_1\rangle_1 = \frac{V_{cm}}{2j}e^{j\Psi_1},\ \langle V_2\rangle_1 = \frac{V_{cm}}{2j}e^{j\Psi_2}, \text{ and } \langle V_2\rangle_{-1} = -\frac{V_{cm}}{2j}e^{-j\Psi_2} \tag{4-14}$$

The input matrix B_{14x6} is computed as:

$$B_{14\times 6}=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1/L_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1/L_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/L_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/L_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/L_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/L_2 & 0 \end{bmatrix}^T \tag{4-15}$$

The GSSA model is now fully described and the synchronous condition characterized with (4-8) can be computed for the steady state operation. The equation connecting Fourier coefficients and time-domain waveforms for the output voltage V_r is given with

$$\langle V_r \rangle_{-1}=\frac{1}{2}\left(V_{rs}\sin\omega t+V_{rc}\cos\omega t\right),\ \text{and}\ \langle V_r \rangle_{1}=\frac{1}{2}\left(-V_{rs}\sin\omega t+V_{rc}\cos\omega t\right) \tag{4-16}$$

After some computation, the cosine component of the output voltage is computed as:

$$V_{rc}=R_rY_1\left(\left(1+\frac{\pi Q}{R_rY_1}+Q^2\right)V_{in}-\frac{1+Q^2}{\omega L_{in}Y_1}V_{cm}\cos\Psi_1\right) \tag{4-17}$$

where Q is quality-factor of the load,

$$Q=\frac{\omega L_r}{R_r} \tag{4-18}$$

and Y_1 is conductance equal to

$$Y_1=-\pi\omega C_r+\frac{1}{\omega L_{in}}\frac{16+9\pi^2}{18\pi} \tag{4-19}$$

Based on (4-8) and (4-17), the synchronization of the boost amplifier can be controlled with the amplitude or phase-delay of the compensating sources. Next sections cover the use of either control strategies. Also, it is possible to combine the two strategies but that discussion will not be outlined in this work.

4.3.3. Amplitude Control

The amplitude of the compensating sources is utilized to control the synchronous operation of the boost amplifier. The phase-delay Ψ_1 is fixed, and it is beneficiary to make it zero since the circulating current $I_L^{(1)}(t)$ is maximized. Equating (4-17) to zero for synchronous operation allows to find the dependence of the amplitude V_{cm} on the circuit parameters as:

$$V_{cm} = \frac{1+\frac{\pi Q}{R_r Y_1}+Q^2}{1+Q^2}\omega L_{in} Y_1 V_{in} \tag{4-20}$$

Figure 4-7 shows dependence of V_{cm} on the load coil's resistance while other parameters are fixed and equal to ones in Table 4-1. The dependence is uniform, which is good for the practical implementation of the control block. The negative value of the amplitude is interpreted as the phase-delay Ψ_1 changes its value to $\Psi_1 = \pi$. Equation (4-20) is confirmed by series of simulations. Boost amplifier with ideal switches is simulated for the parameters in Table 4-1, and for five different values of the load coil's resistance. The matching between the theoretical curve and simulated results confirm the validity of (4-20).

The simulation waveforms of the boost amplifier in the steady-state are shown in Figure 4-8. Cases for three different load coil's resistances are given. The switching functions are kept same for all simulation cases. The light-load case is obtained by setting $R_r = 0.5\ \Omega$. The main variables are colored in green. The amplitude of the compensating source is close to 40 V. For the nominal-load case the load resistance is $R_r = 1.1\ \Omega$. The main variables are colored in blue, and the amplitude of the compensating source is 12 V. The heavy-load case is obtained with $R_r = 2.2\ \Omega$. The main variables are colored in red, and the amplitude of the compensating source is equal to 82 V. The phase-delay is

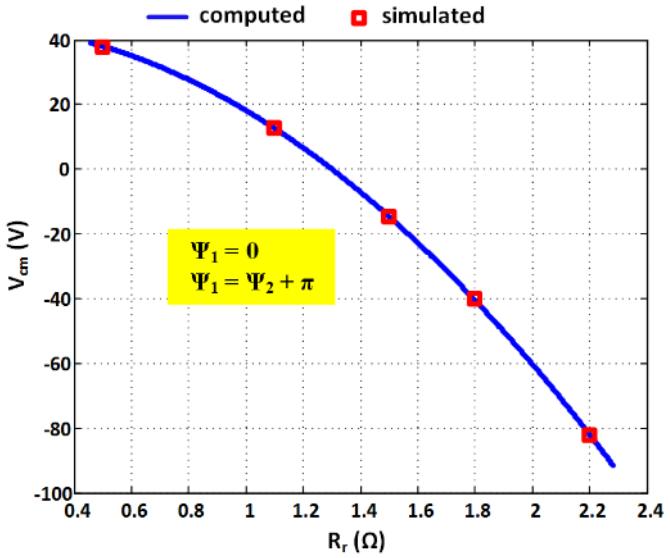


Figure 4-7. Dependence of V_{cm} on the load resistance R_r to keep the boost amplifier under synchronization. Blue curve is plotted based on (4-20). Red markers confirm (4-20) using switching simulation of idealized boost amplifier in LT spice. The amplifier's parameters are given in Table 4-1.

shifted by 180° to adjust for "negative amplitude" value that is required by (4-20). For all simulation cases the output voltage and current are same: V_{rm} = 800 V and I_{rm} = 35 A.

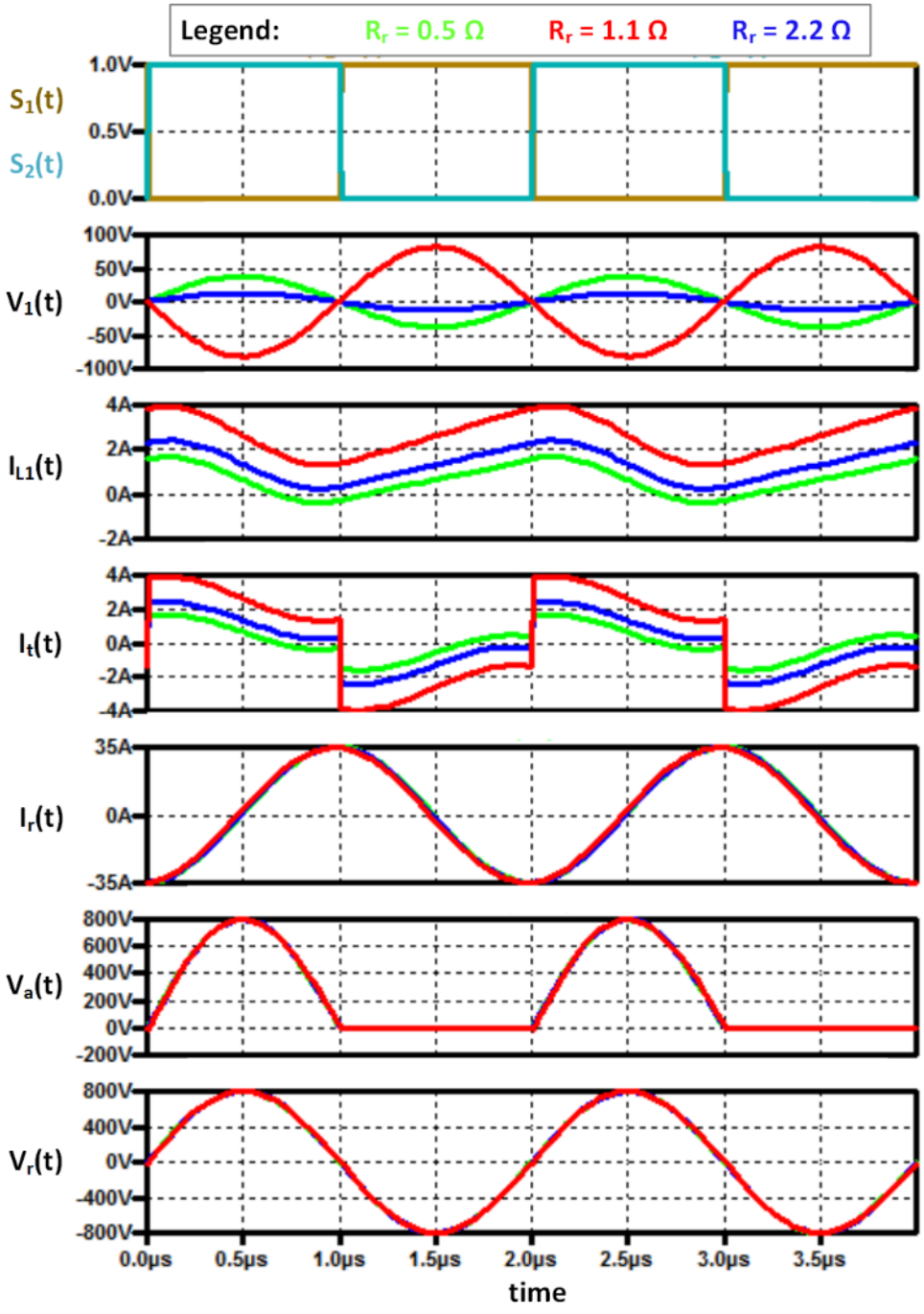


Figure 4-8. Simulation waveforms of the boost amplifier for the load resistance taking values of R_r = 0.5 Ω, R_r = 1.1 Ω, and R_r = 2.2 Ω. The V_{cm} follows equation (4-20) to keep the amplifier in synchronization.

4.3.4. Phase Control

The compensator's phase-delay can be used as a control variable in order to achieve synchronous operation of the boost amplifier. The compensator's amplitude is fixed. Equation (4-17) is set to zero to achieve synchronization, and the phase-angle Ψ_1 is expressed as a function of the amplifier's circuit parameters, given with:

$$\Psi_1 = \cos^{-1}\left(\frac{1+\frac{\pi Q}{R_r Y_1}+Q^2}{1+Q^2} \omega L_{in} Y_1 \frac{V_{in}}{V_{cm}} \right) \tag{4-21}$$

The (4-21) is plotted in Figure 4-9, where a blue line indicated a theoretical curve computed for circuit parameters in Table 4-1. The amplitude of the compensating source is fixed to V_{cm} = 180 V. The theoretical curve is monotonous, indicating that a control system can be easily built. Circuit simulations are performed for the parameters in Table 4-1 so the (4-21) is validated. Red markers in Figure 4-9 represent values obtained from simulations, and they lay on the computed theoretical curve, validating the equation.

Simulation waveforms are plotted in Figure 4-10 for three different values of load resistance. The resistance change varies the synchronous frequency of the amplifier by 2.5 kHz. The compensation, as indicated by the Figure 4-10 is able to keep the amplifier in synchronization.

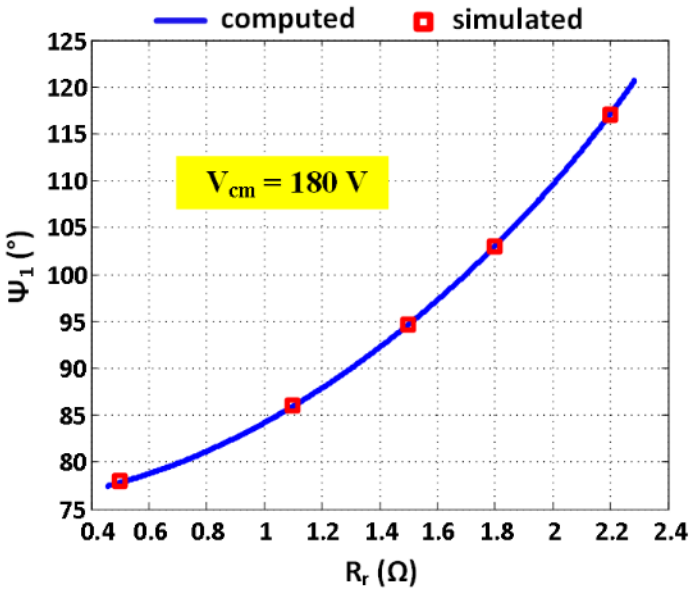


Figure 4-9. Dependence of the phase-delay of the source V_1 on the load resistance when the amplifier operates at synchronization. The graph follows equation (4-21). The amplifier's parameters are given in Table 4-1.

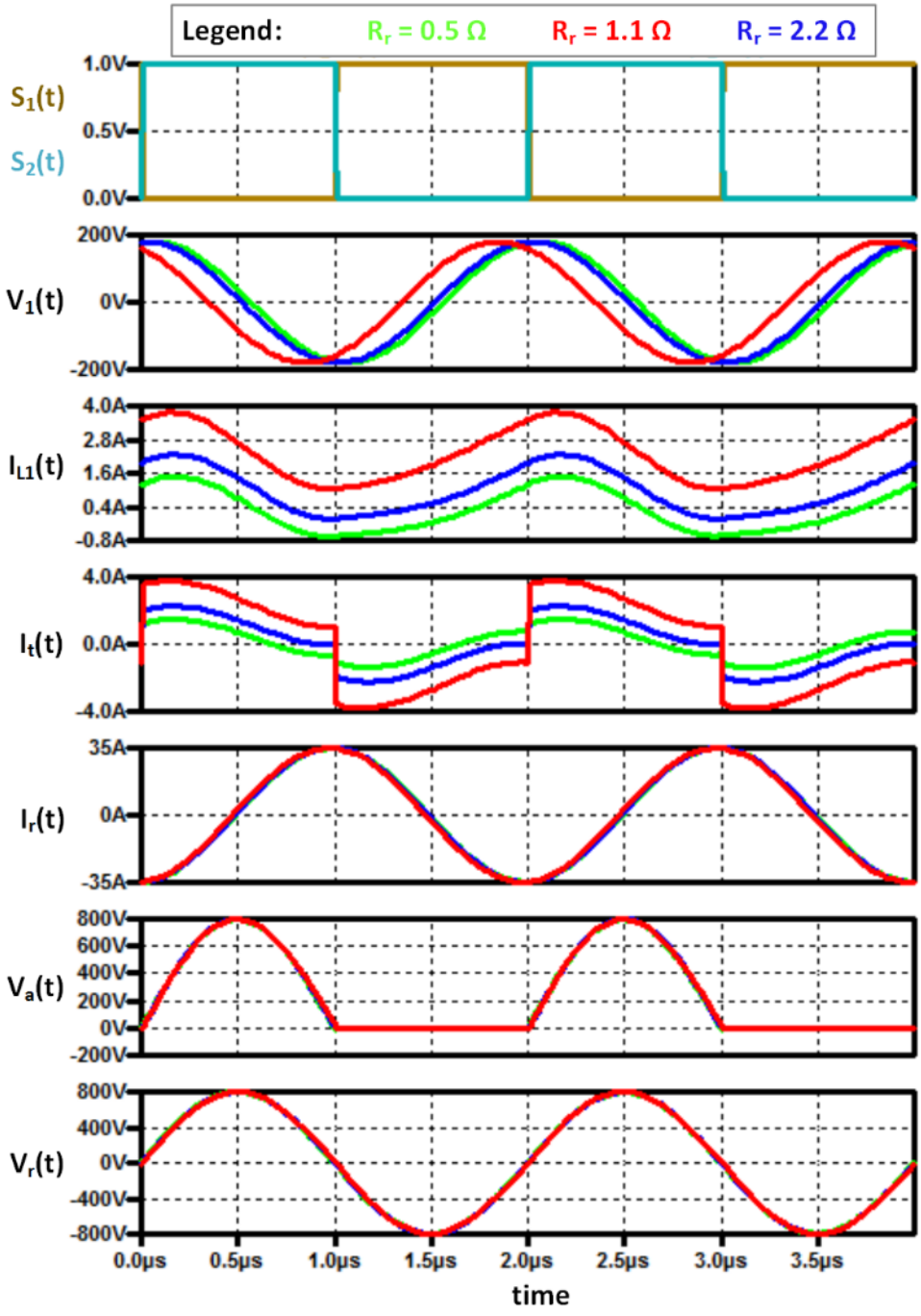


Figure 4-10. Simulation waveforms of the boost amplifier for the load resistance taking values of R_r = 0.5 Ω, R_r = 1.1 Ω, and R_r = 2.2 Ω. The Ψ_1 follows equation (4-21) to keep the amplifier in synchronization. The V_{cm} is set to 180 V.

4.3.5. Synchronous Frequency as Controlled Variable

Previous sections showed the compensation strategy to keep the synchronous frequency of the boost amplifier constant under parametric variations of the load. The order of thinking can be reversed: the synchronous frequency is a controlled variable. For $V_{rc} = 0$, rearrangement of the (4-17) produces the fourth-order equation:

$$\omega^4 - \omega^2\left(\omega_{sy}^2 - \frac{1}{\pi L_{in} C_r}\frac{V_{cm}\cos\Psi_1}{V_{in}}\right) + \frac{R_r^2}{L_r^2}\left(\frac{1}{\pi L_{in} C_r}\frac{V_{cm}\cos\Psi_1}{V_{in}} - \frac{1}{L_{in-eq} C_r}\right) = 0 \qquad (4\text{-}22)$$

where one of the four solutions gives the dependence of synchronous frequency $\omega_{sync}(V_{cm}, \Psi_1)$ on control variables. The $\omega_{sy} = 2\pi f_{sy}$ is uncompensated synchronous angular frequency given obtained from (4-1).

The $\omega_{sync}(V_{cm}, \Psi_1)$ is computed numerically. Figure 4-11 shows the $\omega_{sync}(V_{cm}, 0)$ for boost amplifier's parameters in Table 4-1, and load coil's resistance of $R_r = 1.14$ .The computation is shown with the curve in blue. Red markers show the validation of the (4-22) using a circuit simulation in LT spice. Figure 4-12 shows the control of the synchronous frequency with the phase-delay of the compensation source. The $\omega_{sync}(180\text{ V}, \Psi_1)$ is plotted in blue. Red markers show matching with the circuit simulation. The obtained results in Figure 4-11 and Figure 4-12 show that the synchronous frequency can be controlled in a narrow range, few percent around the target operating frequency.

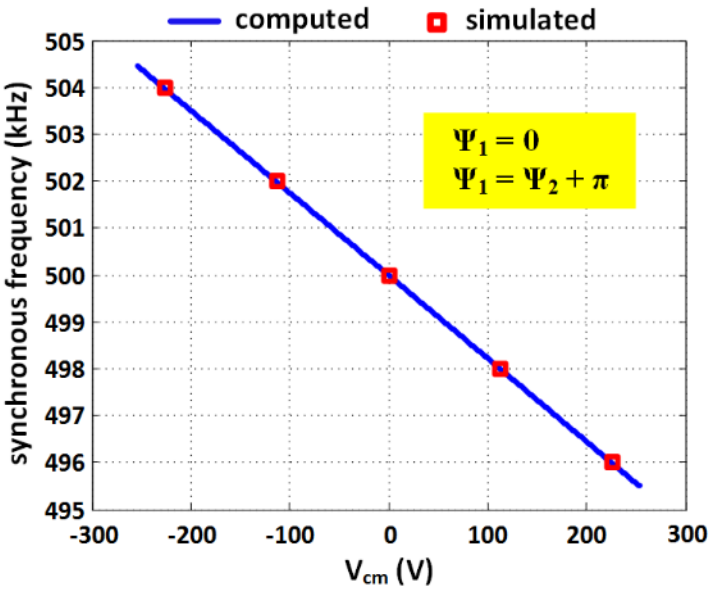


Figure 4-11. Mathematical dependence of the synchronous frequency on the amplitude of the compensating source. The computed curve follows a solution of equation in (4-22).

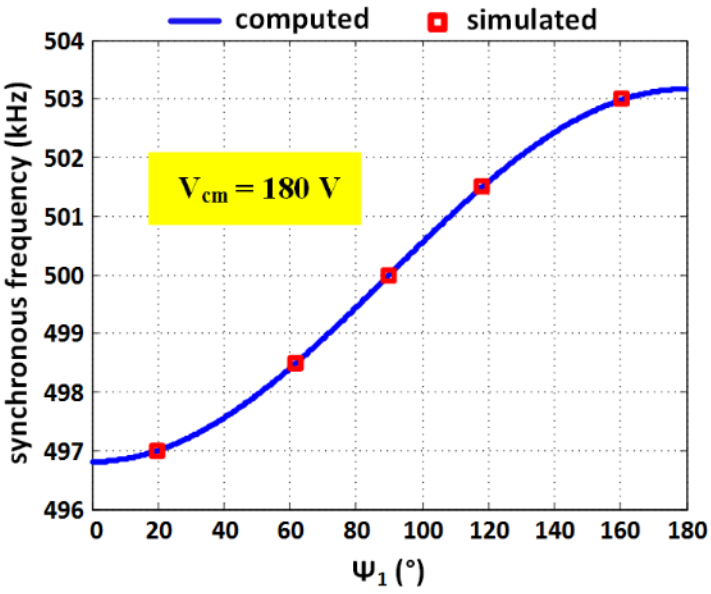


Figure 4-12. Mathematical dependence of the synchronous frequency on the amplitude of the compensating source. The computed curve follows a solution of equation in (4-22).

4.3.6. Discussion on Possible Hardware Implementation

The sinusoidal compensation was derived as simpler step in exploring compensation mechanism using a fundamental frequency current in the input inductor. It can be implemented using parallel power regulation method described in [133]. This direction was not pursued since additional circuitry would be needed for amplitude control. As discussed before, circuit in Figure 4-3 is the desired topology that can both control the output's amplitude and provide compensation of the synchronous frequency. The key contribution of this section is the demonstration of synchronous frequency being a controlled variable.

4.4. PWM Compensation

4.4.1. Circuit Model of the Proposed Two-phase Buck-boost Amplifier

The buck-boost amplifier topology in Figure 4-3 is proposed to compensate for the parametric variation of the load, so the synchronous operation is ensured. Each phase of the amplifier's buck-stage produces a PWM voltage at inputs of the boost stage. The two PWM voltages can replaced with ideal PWM sources for the purpose of synchronous operation analysis. MOSFETs are replaced with ideal switches, and an idealized circuit model for the buck-boost

amplifier is obtained and shown in Figure 4-13. The circuit model will be used for the analysis of the synchronous operation. The two equivalent voltage sources are mathematically defined as:

$$V_1 = V_{bus} PWM(t,T,d,\psi_1) \text{ , and } V_2 = V_{bus} PWM(t,T,d,\psi_2) \tag{4-23}$$

where V_{bus} is input bus voltage (Figure 4-3), and PWM is a function of time, period T, duty-cycle d, and relative phase-shift ΨT from the switching function $S_2(t)$, as shown in Figure 4-14. It is mathematically defined as

$$PWM(t,T,d,\Psi) = \begin{cases} 0, & (0 \le t < \Psi T) \cup ((\Psi + d)T \le t < T) \\ 1, & \Psi T \le t < (\Psi + d)T \end{cases} \tag{4-24}$$

for condition d + Ψ ≤1. When d + Ψ >1, the PWM can be written as:

$$PWM(t,T,d,\Psi) = \begin{cases} 0, & (\Psi + d - 1)T \le t < \Psi T \\ 1, & (0 \le t < (\Psi + d - 1)T) \cup (\Psi T \le t < T) \end{cases} \tag{4-25}$$

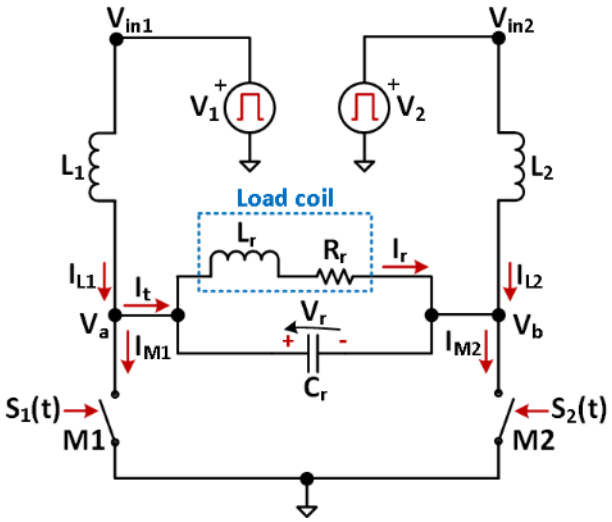


Figure 4-13. Circuit schematics for PWM compensation of the boost amplifier. Sources V_1 and V_2 create a circulating current through L_1, L_2, and the resonant tank. The circulating current is used to control the zero-crossing of the resonant tank's voltage, $V_r(t)$. The PWM sources inject infinite number of harmonic to the boost amplifier. Selectivity (high Q-factor) of the resonant tank filters out all harmonic components except of dc, first, and second.

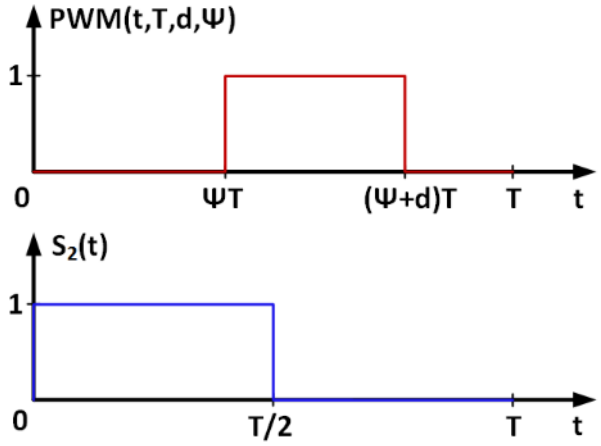


Figure 4-14. Graphic representation of the PWM function. It is characterized by the relative phase-shift ΨT from the switching function $S_2(t)$ and duty-cycle d. The graph shows the representation for d + Ψ ≤ 1, mathematically defined with (4-24).

The values of the phase-shift parameter Ψ are bounded,

$$0 \le \Psi < 1 \tag{4-26}$$

so phase-shift ΨT fits into one period T of the amplifier operation. The duty-cycle is limited as

$$0 \le d \le 0.5 \tag{4-27}$$

because of over-voltage condition on transistors M1/M2 in Figure 4-3. More discussion will be given in section 4.5 . For the asymmetry of the left-hand and right-hand side of the circuit it is assumed that

$$\Psi_2 = \Psi_1 \pm 0.5 \tag{4-28}$$

and duty-cycles are same for both V_1 and V_2 (as shown in (4-23)). The amplitude of the output voltage is controlled with the duty-cycle:

$$V_{rm} = \pi \cdot average\left(V_1(t)\right) = \pi d V_{bus} \tag{4-29}$$

where average() is a function that computes an average value of a variable on period of repetition. The synchronous operation is control with a relative phase-shift variable, Ψ_1. Figure 4-15 shows the theoretical waveforms for voltage inputs, switch M1 voltage, and the output voltage at synchronous condition for the amplifier parameters summarized in Table 4-2. The waveforms are obtained using LT-spice simulation of idealized buck-boost amplifier.

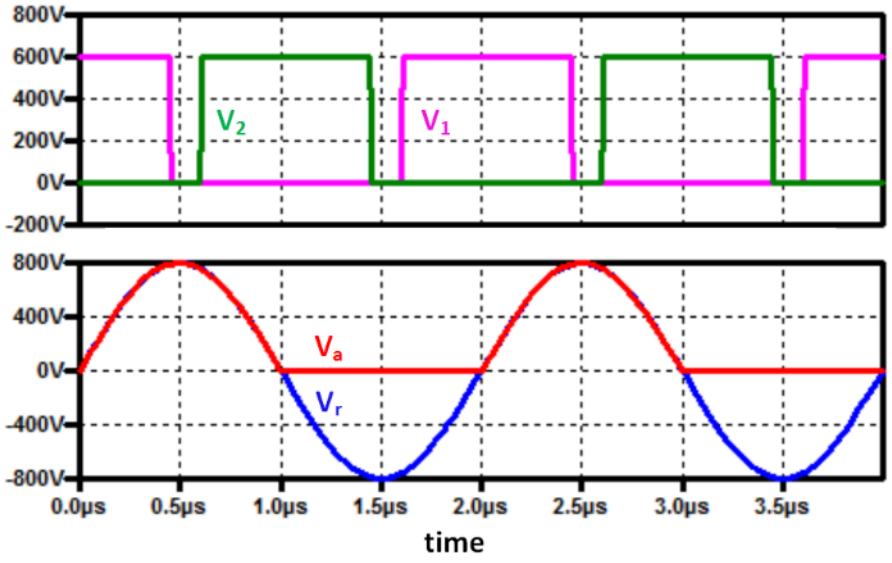


Figure 4-15. Simulation waveforms of the boost amplifier with PWM compensation operated in synchronous condition.

Table 4-2. Simulation parameters of idealized buck-boost amplifier in Figure 4-13.

f_{sw} (kHz)	V_{bus} (V)	d	Ψ_1	Ψ_2
500	600	0.424	0.8	0.3
L_1 (µH)	L_2 (µH)	L_r (µH)	C_r (nF)	R_r (Ω)
125	125	7.27	14.38	1.14

4.4.2. GSSA Model of the Boost Amplifier for PWM Compensation

The time-variant inputs $V_1(t)$ and $V_2(t)$ in (4-23) are transformed into time-invariant coefficients using GSSA method. The coefficients are same for both PWM(t,T,d,Ψ) mathematical representations in (4-24) and (4-25), and depend on the harmonic number n ($n \neq 0$) as:

$$\langle V_1 \rangle_n = -\frac{V_{bus}}{j2\pi n} e^{-j2\pi n\Psi_1}\left(e^{-j2\pi nd} - 1\right), \text{ and } \langle V_2 \rangle_n = -\frac{V_{bus}}{j2\pi n} e^{-j2\pi n\Psi_2}\left(e^{-j2\pi nd} - 1\right) \quad (4\text{-}30)$$

For n = 0,

$$\langle V_1 \rangle_0 = \langle V_2 \rangle_0 = dV_{bus} \quad (4\text{-}31)$$

The previous assumption, that only dc, first, and second harmonic in $I_{L1}(t)/I_{L2}(t)$ currents are important and others can be neglected, is still valid. Thus, only dc, first, and second harmonics of $V_1(t)$ and $V_2(t)$ are important as well. The input vector to the GSSA model will than have ten elements, defined as:

$$\langle U_{10\times1}\rangle(t)=\left[\langle V_1\rangle_{-2}\quad\langle V_1\rangle_{-1}\quad\langle V_1\rangle_{0}\quad\langle V_1\rangle_{1}\quad\langle V_1\rangle_{2}\quad\langle V_2\rangle_{-2}\quad\langle V_2\rangle_{-1}\quad\langle V_2\rangle_{0}\quad\langle V_2\rangle_{1}\quad\langle V_2\rangle_{2}\right]^T \tag{4-32}$$

where the matrix elements are computed based on (4-30) and (4-31). The input matrix B_{14x10} is computed as:

$$B_{14\times10}=\begin{bmatrix}0&0&0&0&1/L_1&0&0&0&0&0&0&0&0&0\\0&0&0&0&0&1/L_1&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&1/L_1&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&1/L_1&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&1/L_1&0&0&0&0&0\\0&0&0&0&0&0&0&0&0&1/L_2&0&0&0&0\\0&0&0&0&0&0&0&0&0&0&1/L_2&0&0&0\\0&0&0&0&0&0&0&0&0&0&0&1/L_2&0&0\\0&0&0&0&0&0&0&0&0&0&0&0&1/L_2&0\\0&0&0&0&0&0&0&0&0&0&0&0&0&1/L_2\end{bmatrix}^T \tag{4-33}$$

The states and the transition matrix A_{14x14} of the GSSA model remain the same as in (4-10), which is rewritten as:

$$\frac{d}{dt}\langle X_{14\times1}\rangle(t)=A_{14\times14}\cdot\langle X_{14\times1}\rangle(t)+B_{14\times10}\cdot\langle U_{10\times1}\rangle(t) \tag{4-34}$$

4.4.3. Solution to the Synchronization Problem

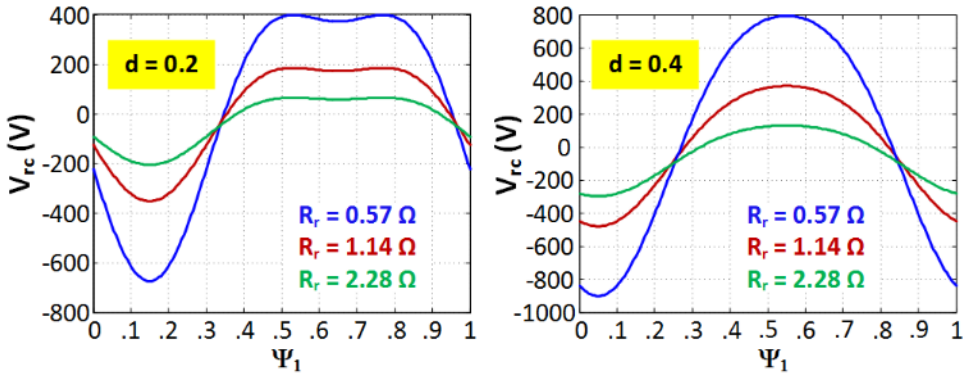
The (4-34) is solved at the steady-state to find a solution to the synchronization problem. The cosine component of the resonant voltage is computed as

$$V_{rc}=R_rY_1V_{bus}\left(\left(1+\frac{\pi Q}{R_rY_1}+Q^2\right)d+\frac{1+Q^2}{\pi Y_1\omega L_{in}}f_{eR}(\Psi_1,d)\right) \tag{4-35}$$

where Q is given with (4-18), and

$$f_{eR}(\Psi_1,d)=-2\sin(\pi d)\sin\left(2\pi\left(\Psi_1+\frac{d}{2}\right)\right)+\frac{4}{3\pi}\sin(2\pi d)\cos\left(4\pi\left(\Psi_1+\frac{d}{2}\right)\right) \tag{4-36}$$

The first term in brackets of (4-35) represent a contribution of dc harmonic of input sources to the cosine component of the resonant voltage. The first term in (4-36) represent a contribution of first harmonic, and the second term in (4-36) represent a contribution of the second harmonic of the input sources to the cosine component of the



(a) **(b)**

Figure 4-16. Graphical method to solve equation (4-35) for amplifier's parameters in Table 4-2 and different values of load resistance. (a) d = 0.4; (b) d = 0.2.

resonant voltage. The (4-35) is too complicated to find analytical solution for $V_{rc} = 0$. Rather, the equation is solved using computer software, or graphical method as shown in Figure 4-16. The results are given for amplifier's parameters in Table 4-2, and three values of the load resistance. There are two of (4-35). The characteristics of both solutions will be discussed in section 4.4.5.

4.4.4. Equivalent Circuit Model at the Load Side

The resonant voltage and current are connected with

$$V_r = L_r \frac{dI_r}{dt} + R_r I_r \tag{4-37}$$

The resonant current can be represented with sine and cosine components as:

$$I_r = I_{rs} \sin(\omega t) + I_{cs} \cos(\omega t) \tag{4-38}$$

Taking into account (4-7), (4-37), and (4-38), the resonant tank's voltage and current components are connected with

$$\begin{aligned} V_{rs} &= R_r I_{rs} - \omega L_r I_{rc} \\ V_{rc} &= R_r I_{rc} + \omega L_r I_{rs} \end{aligned} \tag{4-39}$$

Synchronous condition greatly simplifies the equations that describe the resonant tank. From (4-7), (4-8), (4-29), and (4-39), resonant tank's current components are

$$I_{rs} = \frac{\pi d V_{bus}}{R_r\left(1+Q^2\right)}, \text{ and } I_{rc} = -Q\frac{\pi d V_{bus}}{R_r\left(1+Q^2\right)} \tag{4-40}$$

The output power is calculated as:

$$PA = \frac{1}{2}\frac{\left(\pi d V_{bus}\right)^2}{R_r\left(1+Q^2\right)} \tag{4-41}$$

Figure 17 a) shows an equivalent circuit model reflected to the load side. Currents I_{sin} and I_{cos} are harmonic components of tank's input current $I_t(t)$, and they are computed from (4-29), and (4-40) as

$$I_{\sin} = \frac{\pi d V_{bus}}{R_r\left(1+Q^2\right)}, \text{ and } I_{\cos} = \pi d V_{bus}\left(\omega C_r - \frac{Q}{R_r\left(1+Q^2\right)}\right) \tag{4-42}$$

The input admittance to the resonant tank $y_t(j\omega)$ is equal to

$$y_t(j\omega) = j\omega C_r + \frac{1}{R_r(1+jQ)} = \frac{1}{R_r\left(1+Q^2\right)} + j\omega C_r - \frac{jQ}{R_r\left(1+Q^2\right)} \tag{4-43}$$

where Q is defined with (4-18). At the synchronous condition, the circuit model in Fig 17 a) can be simplified with the circuit in Fig 17 b) where cosine current source component is substituted with an equivalent, controllable admittance $y_c(j\omega)$. The admittance is computed from (4-29) and (4-42) as

$$y_c(j\omega) = -j\frac{I_{\cos}}{V_{rm}} = \frac{jQ}{R_r\left(1+Q^2\right)} - j\omega C_r \tag{4-44}$$

The resonant tank and controllable admittance are summed up together to form a load to the source current I_{sin} as:

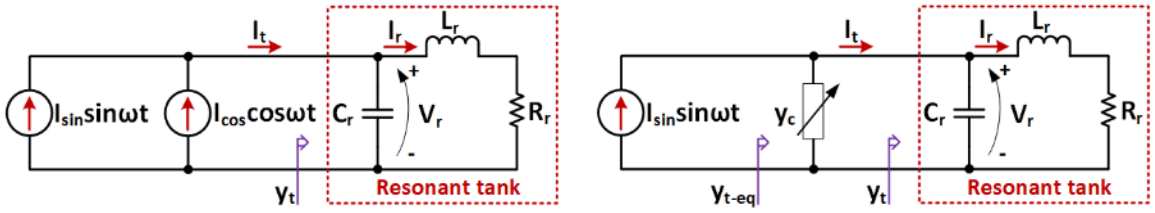


Figure 4-17. Equivalent circuit model at the load side: (a) quadrature source implementation; (b) simplified circuit at the synchronous condition.

$$y_{t-eq}(j\omega) = y_c(j\omega) + y_t(j\omega) = \frac{1}{R_r\left(1+Q^2\right)} \tag{4-45}$$

Important conclusions are formed from (4-43), (4-44), and (4-45):

- Buck-boost amplifier presents an ideal sinusoidal current source to the load, and it is described with (4-42). The source equation is same as for ideal boost amplifier with dc input voltage source and infinite input inductance operated at resonant frequency.
- The buck-boost compensation mechanism behaves as variable matching circuit, which at synchronous frequency compensates for the input reactance of the resonant tank.
- The load to the ideal current source is described with (4-45), and it is purely resistive thanking to the buck-boost compensation mechanism. The (4-45) represents an input admittance of the resonant tank at the resonant frequency.

4.4.5. Current Harmonics in Input Inductors to the Boost Stage

The PWM voltage source $V_1(t)$ is represented with its dc, first, and second harmonic as:

$$\begin{aligned} V_1^{(0)}(t) &= dV_{bus} \\ V_1^{(1)}(t) &= \frac{2V_{bus}}{\pi}\sin(\pi d)\cdot\cos\left(\omega t - 2\pi\left(\psi_1 + \frac{d}{2}\right)\right) \\ V_1^{(2)}(t) &= \frac{V_{bus}}{\pi}\sin(2\pi d)\cdot\cos\left(2\omega t - 4\pi\left(\psi_1 + \frac{d}{2}\right)\right) \end{aligned} \tag{4-46}$$

$V_1^{(n)}(t)$ represent n-th harmonic of the source. Harmonic components higher than second can be ignored for the practical circuit since they do not impact significantly synchronous operation or the power delivery.

The currents in inductors L_1 and L_2 are described with (4-4). In Chapter 2, it was determined that the inductors and input voltage source can be replaced with an array of equivalent current sources of the same amplitudes and phase-angles. The same modeling approach is repeated in this section. After some computation, the dc component of the current in L_1 is equal to:

$$I_{L1}^{(0)}(t) = \frac{\pi^2}{4}\frac{dV_{bus}}{R_r\left(1+Q^2\right)} - \frac{V_{bus}}{4\omega L_{in}} f_{el}\left(\Psi_1, d\right) \tag{4-47}$$

where

$$f_{el}(\Psi_1, d) = 2\sin(\pi d)\cos\left(2\pi\left(\Psi_1 + \frac{d}{2}\right)\right) + \frac{2}{3\pi}\sin(2\pi d)\sin\left(4\pi\left(\Psi_1 + \frac{d}{2}\right)\right) \tag{4-48}$$

The first term in (4-47) correspond to the active power delivery to the load, and originates for the dc component of the source V1. The second term in (4-47) originates from first and second harmonic component of the V_1 source. The $I_{L1}^{(0)}(t)$ impacts strongly the current stress of switches M1/M2, as shown in (4-6). Making $f_{el}(\Psi_1, d)$ positive is beneficial since $I_{L1}^{(0)}(t)$ is reduced, and the current stress is reduced as well. It was shown that (4-35) has two solutions when $V_{rc} = 0$. From (4-47), (4-48), and Figure 4-18, it is seen that one solution produces $f_{el}(\Psi_1, d) < 0$ (red point in Figure 4-18), and second solution produces $f_{el}(\Psi_1, d) > 0$ (green point in Figure 4-18). The second solution reduces the current stress, and it should be used in amplifier designs.

The first harmonic component in inductor L_1 current is equal to:

$$I_{L1}^{(1)}(t) = \frac{\pi d V_{bus}}{2\omega L_{in}}\cos(\omega t) + \frac{2V_{bus}}{\pi\omega L_{in}}\sin(\pi d)\cdot\sin\left(\omega t - 2\pi\left(\psi_1 + \frac{d}{2}\right)\right) \tag{4-49}$$

The first term in (4-49) originates from the dc component, whereas the second term originates from the first and second components of the of the V1 source. The amplitude of the current $I_{L1}^{(1)}(t)$ is controlled by choice of Ψ_1 for given duty-cycle. The second harmonic component in inductor L_1 current is:

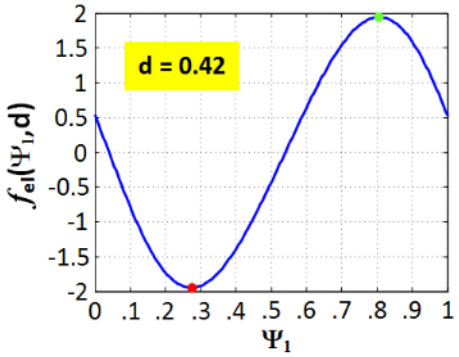


Figure 4-18. Dependence of function $f_{el}(\Psi_1, d)$ on Ψ_1 for d = 0.42. The $I_{L1}^{(0)}(t)$ value in (4-47) is reduced for $f_{el}(\Psi_1, d) > 0$. Current stress in switches M1/M2 is also reduced since $I_{L1}^{(0)}(t)$ is main contributor to the switch current, as shown in (4-6). Conduction losses in transistors M1/M2 are reduced as well. Synchronization occurs when $\Psi_1 = 0.805$ (green point on $f_{el}(\Psi_1, d)$ curve) or $\Psi_1 = 0.275$ (red point on $f_{el}(\Psi_1, d)$ curve). The green point represent desirable operating condition.

$$I_{L1}^{(2)}(t)=\frac{dV_{bus}}{3\omega L_{in}}\sin(2\omega t)+\frac{V_{bus}}{2\pi\omega L_{in}}\sin(2\pi d)\cdot\sin\left(2\omega t-4\pi\left(\psi_1+\frac{d}{2}\right)\right) \tag{4-50}$$

Similarly as before, the first term in (4-50) originates from the dc component, whereas the second term originates from the first and second harmonic components of the of the V1 source. The input power of the ideal, lossless buck-boost amplifier is computed as:

$$P_{bus}=2\left(P_1^{(0)}+P_1^{(1)}+P_1^{(2)}\right) \tag{4-51}$$

where $P_1^{(n)}$ is the average power of the n-th harmonic component that is used to transfer power, given with:

$$P_1^{(n)}=\frac{1}{T}\int_0^T V_1^{(n)}(t)\cdot I_{L1}^{(n)}(t)dt \tag{4-52}$$

From (4-46), (4-47), (4-49), and (4-50), the $P_1^{(0)}$, $P_1^{(1)}$, and $P_1^{(2)}$ are computed as

$$\begin{aligned}
P_1^{(0)}&=\frac{\pi^2}{4}\frac{d^2V_{bus}^2}{R_r\left(1+Q^2\right)}-P_1^{(1)}-P_1^{(2)}\\
P_1^{(1)}&=\frac{dV_{bus}^2}{2\omega L_{in}}\sin(\pi d)\cos\left(2\pi\left(\Psi_1+\frac{d}{2}\right)\right)\\
P_1^{(2)}&=\frac{dV_{bus}^2}{6\pi\omega L_{in}}\sin(2\pi d)\sin\left(4\pi\left(\Psi_1+\frac{d}{2}\right)\right)
\end{aligned} \tag{4-53}$$

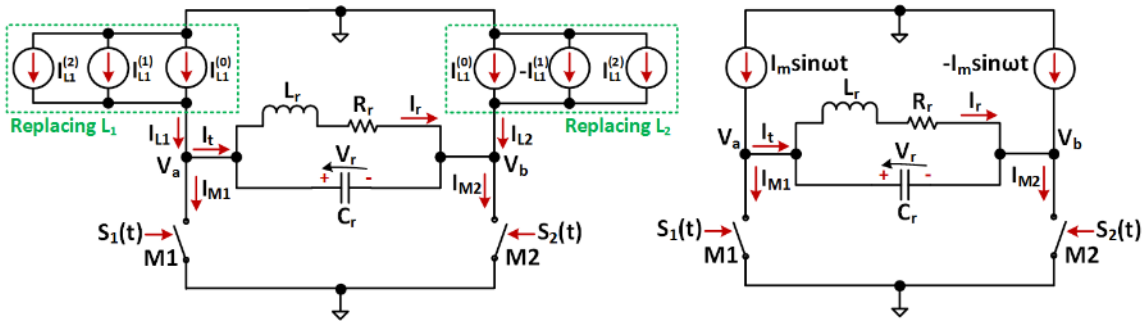
and

$$P_{bus}=PA=\frac{\pi^2}{2}\frac{d^2V_{bus}^2}{R_r\left(1+Q^2\right)} \tag{4-54}$$

Power level in the system is always the same as long as the system operates in synchronous condition, it is function of the average voltage at the input of boost amplifier and the load coil's parameters, and it is given with (4-54). However, the transferred power distributes differently among harmonic. The power of the second harmonic, $P_1^{(2)}$, is typically much smaller than the other two components, and account for around 5 % of the total transferred power. The power is thus split majorly between first and second harmonic. For negative values of $f_{el}(\Psi_1, d)$, $P_1^{(1)}$ is negative, and V_1 source supplies larger dc current to make $P_1^{(0)}$ larger and keep P_{bus} constant. Larger dc current means more current flowing through switches and larger conduction loss. When $f_{el}(\Psi_1, d) > 0$, $P_1^{(1)}$ is positive and total power is shared with $P_1^{(0)}$. The source V_1 supplies less dc current, and the conduction loss is lowered. The minimum switch loss

occurs when $I_{L1}^{(0)}(t)=0$. The power is transferred to the load majorly by the fundamental frequency, while small portion is transferred with the second harmonic. Figure 4-19 a) shows equivalent current-source model of the amplifier where each significant harmonic component of the input inductors is replaced with a current source of the same amplitude and phase. The circuit in Figure 4-19 b) shows a simplification where dc component is nullified and second harmonic component is neglected. Table 4-3 shows different scenarios for the boost amplifier with the same output voltage (V_{rm} = 800 V) and current (I_{rm} = 35 A). The synchronous conditions are calculated based on (4-35) and are also given in the table. The goal is to compare the scenarios with respect to the switch current in the boost stage.

Case-1 is the worst design case for which switch current level is 65 % higher than the nominal (Case-2), as shown in Figure 4-20. Case-3 current level is 55 % lower than the nominal. The current level decrease depends on the amplifier's parameters, such as quality-factor. The Case-3 does not possess capability to control switch's dc current since duty-cycle is used to control output power, Ψ_1 is used in synchronization, and switching frequency is fixed. If the switching frequency or input inductance can be varied, Case-4 is viable. The dc component is nullified and minimum current stress is observed. Case-5 correspond to the ideal circuit in Figure 4-19 b), where dc component is nullified and second (and higher harmonics) are neglected. Switches do not conduct any current and have zero power loss. The analysis of properties and possible implementations of the Case-4 and the Case-5 circuits are out of the scope of this work, and they will be briefly discussed as the future work.



(a) (b)

Figure 4-19. Equivalent current-source model: (a) dc, first, and second harmonic components are present. This is the general case. (b) the dc component is nullified, and second harmonic component is neglected.

Table 4-3. Five design cases for boost amplifier. All cases has same output conditions, and operate at synchronous condition. The design cases are compared for the current harmonics in the input inductor, used harmonic components to transfer power, and current stress and conduction loss in the switches.

Case-1	PWM source with active compensation for fixed frequency operation, $f_{el}(\Psi_1, d) < 0$, $P_1^{(1)}$ negative, current stress increases					
	f_{sw} (kHz)	500	L_{in} (μH)	125	R_{on} (mΩ)	80
	V_{bus} (V)	600	d	0.42	Ψ_1	0.278
	L_r (μH)	7.27	C_r (nF)	14.38	R_r (Ω)	1.14
Case-2	dc source, at synchronous frequency, no active power transferred with first harmonic, nominal current stress					
	f_{sw} (kHz)	500	L_{in} (μH)	125	R_{on} (mΩ)	80
	V_{bus} (V)	600	d	1		
	L_r (μH)	7.27	C_r (nF)	14.38	R_r (Ω)	1.14
Case-3	PWM source with active compensation for fixed frequency operation, $f_{el}(\Psi_1, d) > 0$, $P_1^{(1)}$ positive and partially carries power					
	f_{sw} (kHz)	500	L_{in} (μH)	125	R_{on} (mΩ)	80
	V_{bus} (V)	600	d	0.42	Ψ_1	0.805
	L_r (μH)	7.27	C_r (nF)	14.38	R_r (Ω)	1.14
Case-4	PWM source with active compensation, dc component nullified by setting either switching frequency or input inductance, $P_1^{(1)}$ carry most of the power					
	f_{sw} (kHz)	500	L_{in} (μH)	40	R_{on} (mΩ)	80
	V_{bus} (V)	600	d	0.42	Ψ_1	0.95
	L_r (μH)	7.27	C_r (nF)	14.38	R_r (Ω)	1.14
Case-5	Idealization for which all power is transferred with fundamental component					
	f_{sw} (kHz)	500			R_{on} (mΩ)	80
	I_m (A)	1.72				
	L_r (μH)	7.27	C_r (nF)	14.38	R_r (Ω)	1.14

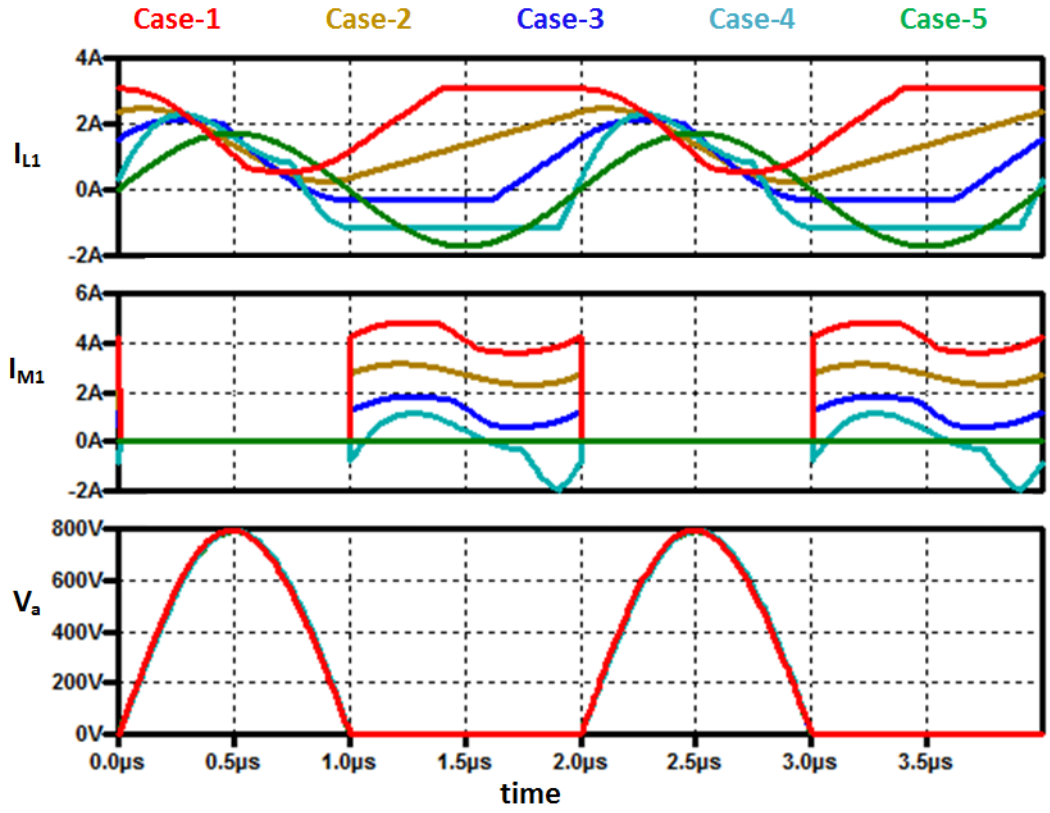


Figure 4-20. Comparison between five design cases with a goal to minimize conduction losses in the boost switches. The switch current is minimized as the input inductor current becomes more sinusoidal, while $f_{el}(\Psi_1, d) > 0$.

Figure 4-21 shows the amplitudes of harmonic components in input inductor current for each of five cases in Table 4-3. Comparison between Case-1 and Case-3 shows that the amplitudes of first and second harmonics are the same, with opposing phases. Case-1 has much larger the dc component than Case-3 since it has negative value for $P_1^{(1)}$ and more power needs to be transferred with $P_1^{(0)}$ component, as shown in Figure 4-22. Case-2 has significant the dc, first, and second harmonics of the I_{L1} current, however, it transfers power only using the dc harmonic (Figure 4-22). Case-3 transfers power using all harmonic components, where the dc and the first components dominate the total power transfer. Case-4 does not use the dc component to transfer power at all. Case-5 is the idealization that transfers power only using the fundamental component. Total transferred power is the same for all cases.

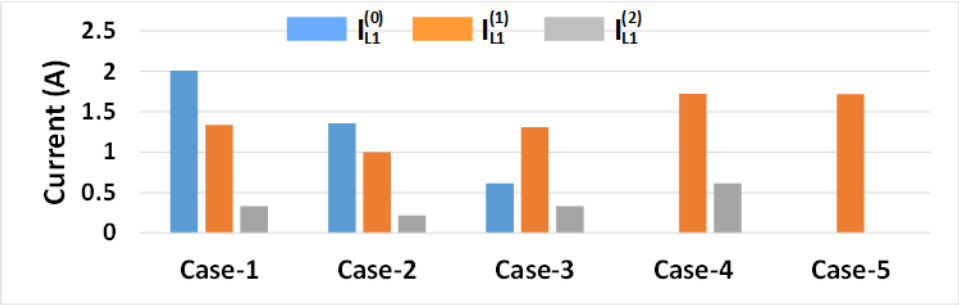


Figure 4-21. Harmonic components of the input inductor current for five design cases that are described in Table 4-3. Case-1 and Case-3 have the same first and second harmonic amplitude but opposing phases. Case-4 has dominant first harmonic. Case-5 is the idealization with first harmonic only.

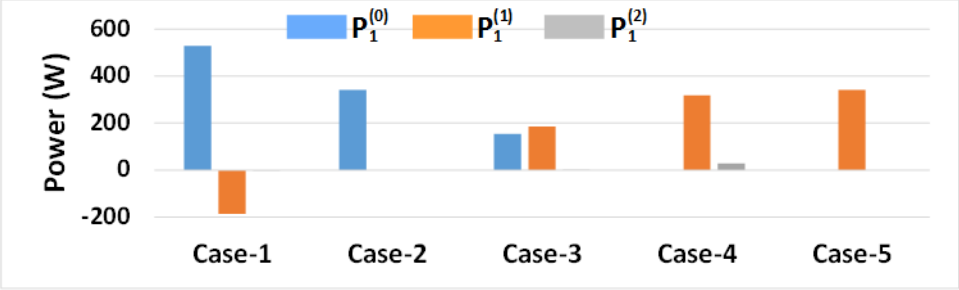


Figure 4-22. Amount of power that source V_1 transfers using the dc, first, and second harmonic component for each of the cases. Total power of V_1 source is the same for all cases. Case-1 has negative first and second power components so the dc component is enlarged. Case-2 uses only the dc harmonic component to transfer power. Case-3 uses all harmonic components with first and second components helping in power transfer so the dc component is reduced. Case-4 does not use dc component for power transfer, and the first harmonic component dominates power transfer. Case-5 is the idealization where whole power is transferred using fundamental frequency component.

Figure 4-23 shows how the switch conduction loss is impacted by selecting each of the cases to transfer power. The loss is normalized to the value of the Case-1. On-state resistance of the switch is the same for all cases and it equals R_{on} = 80 mΩ. It is seen that choosing to include first harmonic component into transferring power is quite beneficial in reducing the conduction losses of the switches, as Case-3 and Case-4 losses are five to ten times lower that Case-2. Obviously Case-1 produces the worst result. Case-5 is the idealization in which no loss is incurred since no current flows through the switch.

PWM source V_1 is the idealization of the buck stage that contains two switches that turn-on and turn-off alternatively. At any instance of time, either top or bottom switch is conducting. Thus, of interest is if implementation of the active compensation increases RMS current and conduction loss of buck switches. Figure 4-24 shows that RMS current is similar for Case-2, Case-3, and Case-4, leading to almost equal conduction losses of buck switches for any of these cases. Also, active compensation assist in reaching ZVS on buck switches since in Case-3 and Case-4 the dc component of input inductor is reduced (this can also be seen from Figure 4-20).

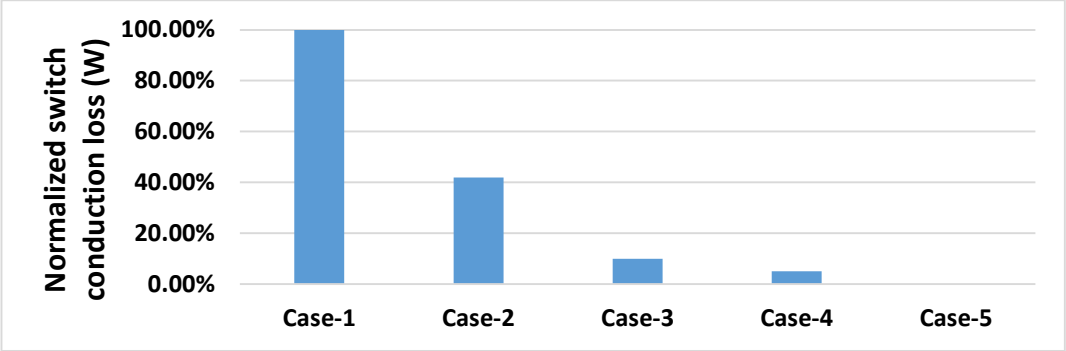


Figure 4-23. Switch conduction loss normalized for the loss of the switch in Case-1. By properly applying the active compensation the switch conduction loss is considerably minimized. Utilization of the first harmonic to transfer power can reduce the switch conduction loss to only a fraction from the case when only dc harmonic is used.

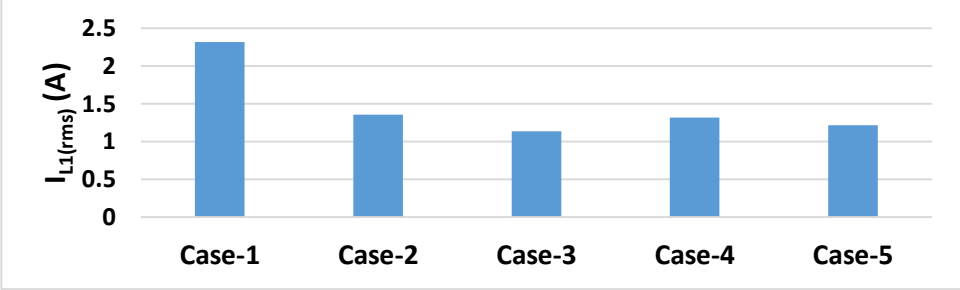


Figure 4-24. RMS current of the input inductor for different design cases obtained from switching simulation model. This current flows through buck stage switches and creates conduction loss. Case-2, Case-3, Case-4, and Case-5 have small difference in obtained RMS currents. Case-1 roughly doubles the current though buck switches when compared to other design cases. Buck switches are thus not penalized if the active compensation is applied as in Case-3 and Case-4 as no RMS current increase is observed.

Important conclusions are made:

- dc voltage source at the input of boost amplifier increase conduction loss of switches.
- The current in input inductors should resemble a sine-wave for smallest loss in boost switches.
- dc and other even harmonics can be considered "parasitic" as they create loss in switches while delivering power. Even harmonics are "common-mode" currents that are shunted to the ground with switches.
- Fundamental and other even harmonics are "differential-mode" currents that deliver power to the load directly, or impact zero-crossing of the resonant voltage.
- Input inductor limits the fundamental current circulation and can be reduced significantly, allowing high current gain from input to output current without penalty of large input inductor. For example, the Case-4 is derived for L_{in} = 40 μH. The ripple or the peak of the input inductor current may not be high if Ψ_1 is far away from 0.5 value. In the example above the Ψ_1 = 0.95 and the maximum input current is less than for the nominal Case-2.

The minimum current ripple in the input inductors occurs at:

$$\Psi_1 = \frac{1}{4} - \frac{d}{2} \tag{4-55}$$

which can be easily validated using formulas for harmonic currents in (4-49) and (4-50). Although this case is not significant for the Case-3 developed in this work, it may have uses if the switching frequency can be controlled. The control mode that for heavy load the dc current is nullified, and for light load the current ripple in input inductors is minimized gives the opportunity to optimize losses for wide range of loads.

4.4.6. Limitations

Equating (4-35) to zero produces two solutions, as indicated by Figure 4-16. The solution for which the function $f_{el}(\Psi_1, d)$ (given with (4-48)) is positive ($f_{el}(\Psi_1, d) > 0$) is desired solution since the current stress in switches is reduced (Figure 4-20). The solution for which $f_{el}(\Psi_1, d) < 0$ is undesired solution for which the current stress in switches increases.

The goal of the active compensation is to achieve synchronous condition (by equating (4-35) to zero) for a range of load's parametric variations. It assumed that the loaded quality-factor changes by around five times, as well as load coil's resistance. The load coil's inductance changes by few percent (~3.2 %), around its base value of $L_r = 7.27$ μH. The parameters of the resonant tank are summarized in Table 4-4. The compensation has to be achieved for wide range of amplitudes of the output voltage. The duty-cycle range from d = 0 to d = 0.5 is examined. The upper limitation comes from the overvoltage condition of the transistors in the boost stage.

Figure 4-25 shows the dependence of the compensation variable Ψ_1 on duty-cycle for the parameters of the resonant tank given in Table 4-4 and for synchronous operation of the boost switches. The dependence is numerically computed using computer program from equating (4-35) to zero. The load parameters take range of values from Table 4-4. Blue curves represent desirable solution for Ψ_1 for which $f_{el}(\Psi_1, d) > 0$ and the switch stress is reduced. Red curves represent undesirable solution for Ψ_1 for which current stress of the switches is increased. The range of load's parameters for which compensation is possible is actually wider than what was declared in Table 4-4, however, the Ψ_1 is not then a monotonous function of duty-cycle d. The monotonicity is important to make implementation of the control system simpler.

Table 4-4. Parameters of the resonant tank for which active compensation is able to ensure synchronous operation of the amplifier.

f_{sw} (kHz)	500	L_r (μH)	7.15 - 7.38
L_{in} (μH)	125	Q	10 - 50
C_r (nF)	14.38	R_r (Ω)	0.46 - 2.2

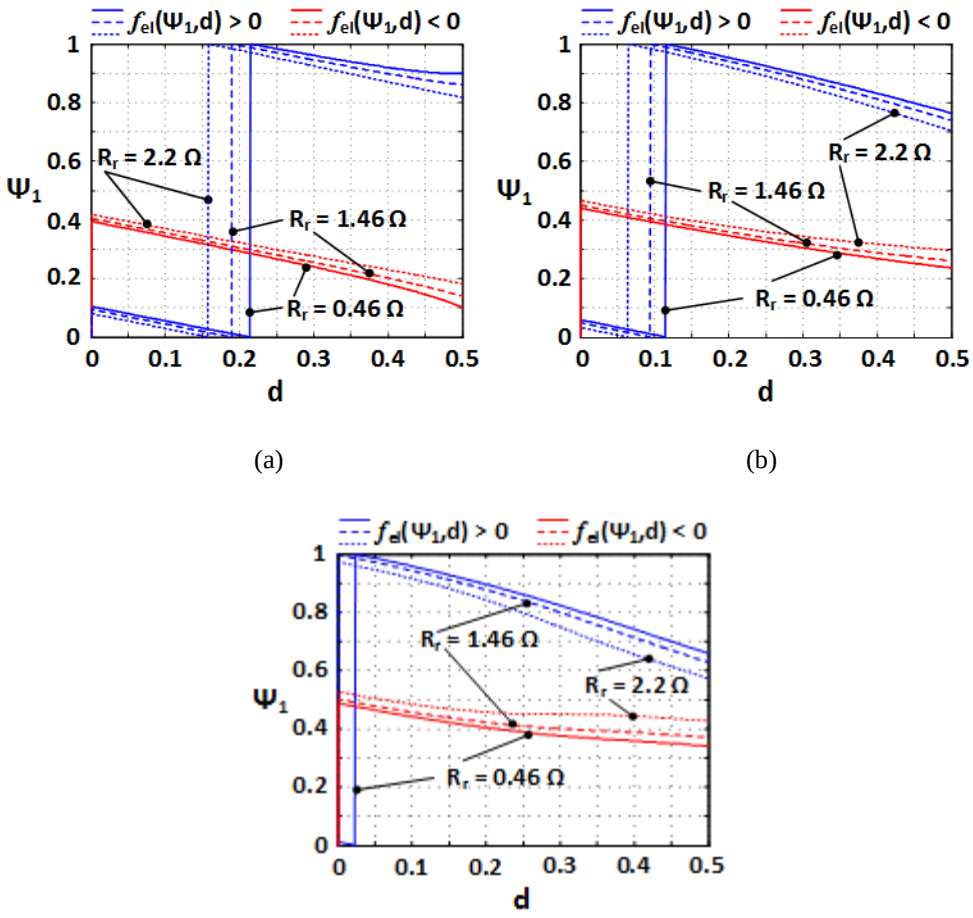


Figure 4-25. Dependence of control variable Ψ_1 on duty-cycle d for the resonant tank's parameters in Table 4-4 and range of load inductance and resistance parameters: a) L_r = 7.15 µH; b) L_r = 7.27 µH; c) L_r = 7.38 µH. The dependence is numerically computed using computer program from the equating (4-35) to zero. Blue curve represent desirable solution for Ψ_1 for which current stress in transistors of the boost stage is reduced ($f_{el}(\Psi_1, d) > 0$). Blue curve unwraps around $\Psi_1 = 0$ and $\Psi_1 = 1$. Red curve represent undesirable solution for which current stress is increased ($f_{el}(\Psi_1, d) < 0$). The parameter Ψ_1 is monotonous function of duty-cycle d, which helps to make implementation of the control system simpler.

4.5. Design & Implementation

The detailed schematic of the two-phase buck-boost amplifier is given in Figure 4-26. The boost stage employs a snubber circuit, consisted of L_s and R_{sn}, in order to attenuate current spikes during start and stop transients. Each MOSFET in Figure 4-26 is driven by an isolated gate driver circuit whose implementation is explained in detail in Chapter 2. Gate drivers are excited with switching functions generated by waveform generators. Switching functions of the boost stage, $S_1(t)$ and $S_2(t)$, are defined with (4-3). Switching functions of buck stage switches ($S_3(t)$, $S_4(t)$, $S_5(t)$, and $S_6(t)$) are defined with help of PWM functions that are given with (4-24) or (4-25). The switching functions are mathematically defined as:

$$\begin{matrix} S_3(t) = PWM\left(t, T, d_3, \Psi_3\right) \\ S_4(t) = PWM\left(t, T, d_4, \Psi_4\right) \end{matrix} \text{ and } \begin{matrix} S_5(t) = PWM\left(t, T, d_5, \Psi_5\right) \\ S_6(t) = PWM\left(t, T, d_6, \Psi_6\right) \end{matrix} \tag{4-56}$$

The computation of the duty-cycles and phase-delays of the switching functions will be shown in the next section.

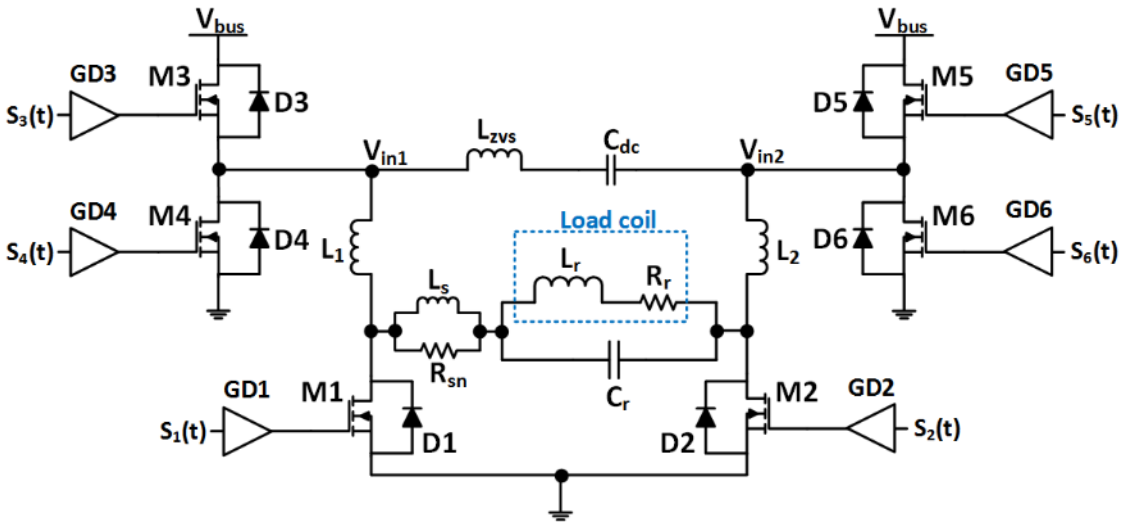


Figure 4-26. The circuit schematic of the implemented Buck-boost amplifier. The specifications, parameters, and component description are given in Table 4-5. Design of ZVS inductor is given in Table 4-6. Gate driver is described in Chapter 2. PWM signals for the gate driver are given with (4-64), (4-65), and they are generated using dual channel waveform generator. Four different load configurations are available for testing, as reported in Chapter 2. Snuber circuit consists of L_s and R_{sn}, and prevents a current spike in M1 and M2 switches during transients. The snubber circuit's power loss is just few watts, and it is less lossy than series diodes that would typically be in series with switches M1 and M2. Design of the snubber circuit is described in Chapter 2.

4.5.1. Design Guidelines

The buck-boost design procedure follows closely the boost amplifier's design procedure in Chapter 2. So, the first step is to design a boost amplifier for the desired synchronous condition for a nominal loaded quality-factor. Next, the switching frequency is set to be equal or close to the synchronous frequency. This allows the active compensation to synchronize the boost for both high and lower values of loaded quality-factor than nominal. Final step is to design the two-phase buck stage. Switch selection is the same as for the boost stage, and C2M0080120D SiC MOSFETs are selected for the bus voltage of V_{bus} = 600 V. To form a phase-leg, C4D02120A SiC diodes are paired to MOSFETs.

The inductive tank is designed so the buck switches achieve ZVS. The design presented here is the simplification of the method presented in [174]. Capacitance C_{dc} of 470 nF is chosen to block dc current flowing though the inductive tank. During dead-time, both switches in one buck phase are turned off. The current in L_{zvs} helps for all switches to achieve ZVS. The input inductor current helps to low-side switches, while it obstructs high-side switches. The ZVS condition of the high-side switch will determine the design of L_{zvs} inductor and the dead-time. At the time-instance of turning-on the high-side switch, the input inductor current is at its minimum value (at the valley). The worst-case to achieve ZVS is when the ripple of input inductor current $I_{L1}(t)$ is minimal, so $I_{L1}(t)$ can be approximated with its dc harmonic. Thus, the worst-case current I_{off} that has to deplete output capacitances of all switches and diodes is approximated with:

$$I_{off} = I_{Lzvs} - I_{L1}^{(0)} \tag{4-57}$$

where I_{Lzvs} is current in the L_{zvs} at the moment of switching, defined with:

$$I_{Lzvs} = \frac{dTV_{bus}}{2L_{zvs}} \tag{4-58}$$

and $I_{L1}^{(0)}$ is average current in the input inductor. The existence of ZVS condition is computed as

$$\frac{1}{2}L_{zvs}I_{Lzvs}^2 \geq C_{eq}V_{bus}^2 + \frac{1}{2}L_1\left(I_{L1}^{(0)}\right)^2 \tag{4-59}$$

where C_{eq} is the equivalent capacitance seen at the midpoint of the phase-leg. The capacitance C_{eq} is consisted of two MOSFET and two diode equivalent output capacitors ($C_{oss,eq}$ and $C_{j,eq}$):

$$C_{eq} = C_{oss,eq} + C_{j,eq} \tag{4-60}$$

Using, (4-59), inductor L_{zvs} is computed as

$$L_{zvs} \le \frac{(dTV_{bus})^2}{8 \cdot \left(C_{eq} V_{bus}^2 + \frac{1}{2} L_1 \left(I_{L1}^{(0)} \right)^2 \right)} \tag{4-61}$$

Dead time is computed as

$$t_{dead} \approx \frac{2C_{eq}V_{bus}}{I_{off}} + t_d \tag{4-62}$$

and

$$t_d = t_{d-off} - t_{d-on} \tag{4-63}$$

where $t_{d\text{-}off}$ and $t_{d\text{-}on}$ are turn-on and turn-off delay times of selected MOSFET. Parameters Ψ_1 and d define the PWM function of compensating source V_1 Figure 4-13. For a practical circuit they need to be translated to phase-shift and duty-cycle of each individual MOSFET. With regard to the dead-time, phase-shift parameters for each switch are defined as

$$\begin{aligned} \Psi_{M3} &= \Psi_1 + \frac{T_{dead}}{T} \\ \Psi_{M4} &= \Psi_1 + d + \frac{T_{dead}}{T} \\ \Psi_{M5} &= \Psi_2 + \frac{T_{dead}}{T} \\ \Psi_{M6} &= \Psi_2 + d + \frac{T_{dead}}{T} \end{aligned} \tag{4-64}$$

The duty-cycle for each MOSFET is defined as

$$\begin{aligned} d_{M3} &= d - \frac{T_{dead}}{T} + t_d \\ d_{M4} &= 1 - d - \frac{T_{dead}}{T} - t_d \\ d_{M5} &= d - \frac{T_{dead}}{T} + t_d \\ d_{M6} &= 1 - d - \frac{T_{dead}}{T} - t_d \end{aligned} \tag{4-65}$$

The buck-stage can be designed using (4-57) - (4-65). The system implementation is shown in the next section.

4.5.2. System Implementation

The buck-boost amplifier is implemented using design guidelines from the previous section and the compensation law derived in section 4.4. For the implemented circuit schematic given Figure 4-26, the system specifications, main circuit parameters, and most important components of the implemented system are given in Table 4-5. Details on the design of the ZVS inductor are given in Table 4-6. The design of gate driver circuit is shown in Chapter 2. Driving PWM signals for MOSFETs, defined with (4-56), (4-64), and (4-65), are generated using AFG 3102 dual channel waveform generator. The amplifier is operated in the open-loop mode.

Table 4-5. Specifications of the buck-boost amplifier in Figure 4-26, list of major circuit parameters and components.

Symbol	Description	Value	Part Number
f_{sw}	Switching frequency	480 kHz	
V_{bus}	Bus voltage	300 V- 600 V	Sorensen DCR 600-4.5B
M1-M6	SiC Power MOSFETs	1200 V/20 A	C2M0080120D
D1-D6	SiC Power Diode	1200 V/2 A	C4D02120A
C_{bus}	Bus capacitor (10 in parallel, 4.7 μF total)	470 nF	SV09AC474KAR
L1, L2	Input inductor, PQ3220/N49 ferrite cores	125 μH	B65879A0000R049
L_{zvs}	ZVS inductor PQ3220/N49 ferrite cores	80 μH	B65879A0000R049
C_{dc}	dc current elimination cap in L_{zvs} branch	470 nF	SV09AC474KAR
$C_{r,PCB}$	COG/NPO ceramic capacitor (fifteen in parallel to form ~15 nF capacitor)	1 nF, 2 kV	C1825C102JGGACTU
L_r	Inductance of inductive load	7.4 μH – 7.7 μH	Air-core, custom made
R_r	Damping resistor for inductive load (optional)	1 Ω	TA2K0PH1R00KE
L_s	Snubber inductor	250 nH	Air-core, custom made
R_{sn}	SMD resistor	2 kΩ	RCL12252K00FKEG
Fans	Fans to cool heat sink	24 V, 10.3 W	1939K17

Table 4-6. Details on implementation of ZVS inductor, L_{zvs}.

Core Material	N49	Wire Size (AWG)	17
Core Size	PQ 3220	Litz/stranded wire	550/44
Number of Turns	20	Air gap	0.675 mm
Total Inductance	80 μH	R_{dc}	0.232
Parallel capacitance	9 pF	R_{ac}	1

Implemented buck-boost amplifier is shown in Figure 4-27. The boost stage is implemented on the separate board, and it is improved version of circuit developed in Chapter 2. Buck stage is designed to have separate sections on PCB board for signal input, signal isolation, gate drivers, switching stage, and power processing (dc capacitors, ZVS inductor, and power interconnection with boost stage). Switching noise immunity is improved by having separate sections. Special care is put to minimize power switching loops by placing a MOSFET, its commutating pair diode, and dedicated decoupling capacitor close together on the PCB board. The circuit parasitics are reduced, increasing reliability of the system.

The test setup is shown in Figure 4-28. Short-circuit protection circuit is placed between voltage source and the test circuit aid tests, and prevent failure of the system in case of faults. Inductive load design, measurement setup, and measurement procedure are the same as in Chapter 2. Three synchronized waveform generators are used to generate PWM signals for the system. The distance between generators and the amplifier is minimized for best noise immunity. The propagation delays of PWM signals are calibrated before measurements.

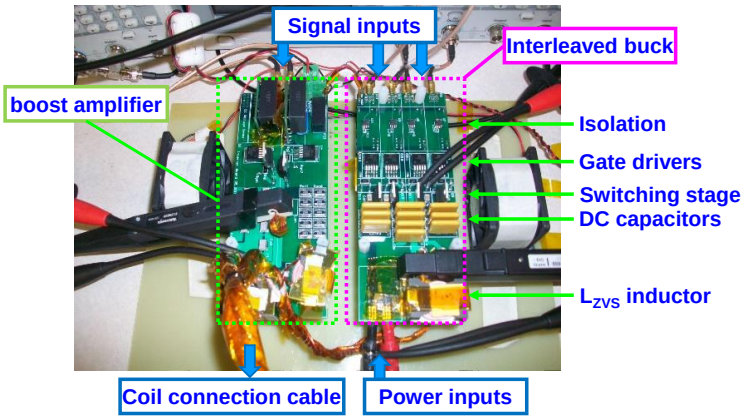


Figure 4-27. Buck-boost amplifier constructed as two separate PCB boards. Left: boost stage; right: two-phase buck stage. Boards are 6.35 cm wide and 16 cm long.

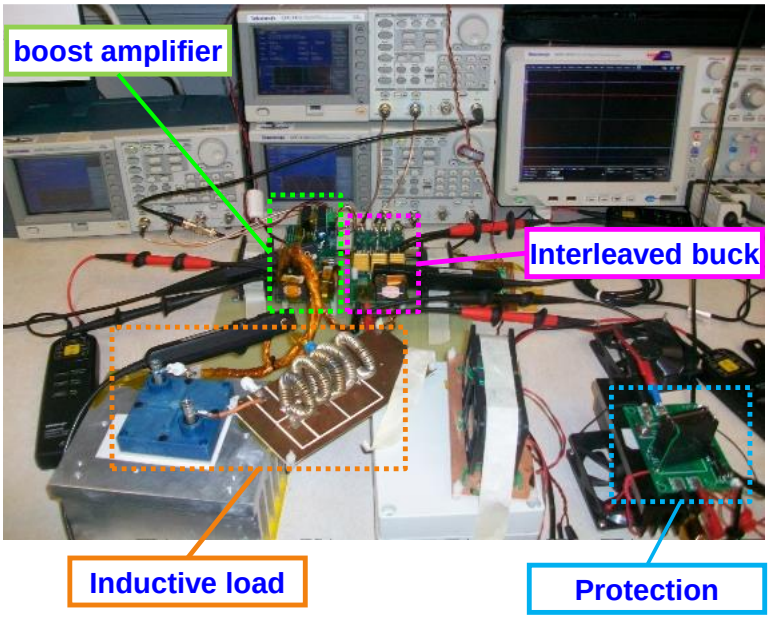


Figure 4-28. The test setup showing most important hardware components.

4.6. Experiments

4.6.1. Objectives, Instrumentation, and Measurement Procedure

The implemented buck-boost amplifier is tested to validate the theory developed in the section 4.4. Two test cases will be examined: 1) Constant frequency operation under load variations; 2) Constant frequency and constant output amplitude under input voltage variations.

The load configurations are described in Chapter 2, and Load-2, Load-3, and Load-4 configurations are tested to validate constant frequency operation of buck-boost amplifier under load variations. For all tests, input bus voltage is fixed to V_{bus} = 300 V, switching frequency is f_{sw} = 480 kHz, and duty-cycle is varied in the range d = 0.35 – 0.5. The bus voltage is supplied by Sorensen DCR 600-4.5A power supply. The amplifier is operated in the burst-mode, to prevent the dynamic change of load coil's parameters due to self-heating. The gating signals for each transistor are created with AFG 3102 dual channel waveform generators. Three synchronized waveform generators are used for six transistors in buck-boost amplifier circuit. Number of cycles for the burst mode of boost stage switches is five hundred, and for buck stage is two hundred. Boost stage operates for longer number of cycles to deplete input inductor current prior the quite interval. The period of the burst mode is 3 ms. Given number of cycles is sufficient to bring the amplifier to the steady-state condition so waveforms can be recoded and efficiency estimated. Two scopes are used in

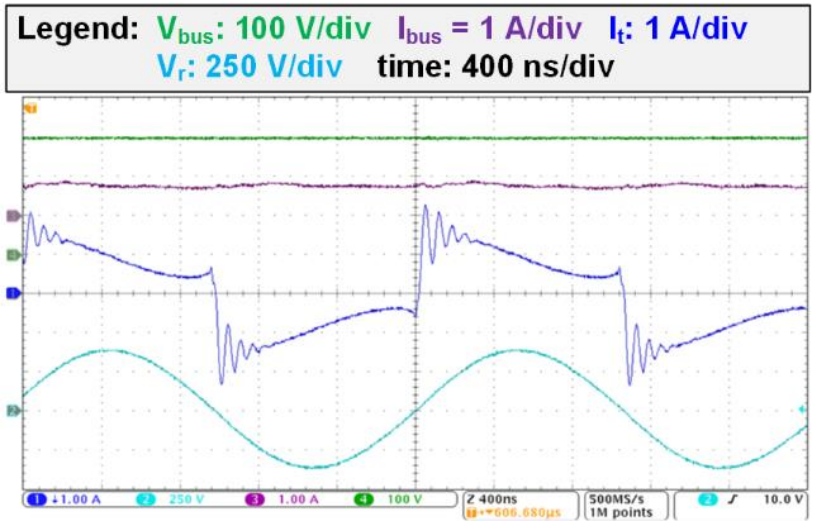
measurements. One scope (Tektronix MSO 4054B) records waveforms relevant to efficiency estimation: input bus voltage (V_{bus}), input bus current (I_{bus}), resonant tank's voltage (V_r), and resonant tank's input current (I_t). Second scope (Tektronix MSO 5104) measures output current (I_r), current in the ZVS inductor (I_{Lzvs}), input inductor current (I_{L1}), and voltage at the input voltage to the boost stage (V_{in1}). Voltage is measured using THDP0200 high-voltage differential probes. Current is measured using TCP0030A probes from Tektronix.

Before testing the amplifier, gating signals of MOSFETs are generated based on (4-64) and (4-65), and by using waveform generators. All delays are compensated and proper driving of MOSFETs is validated prior applying bus voltage to the amplifier. Few iterations are usually required to adjust Ψ_1 value so the boost switches work in synchronous condition. The iterative process can be quite lengthy for high values of loaded quality-factor.

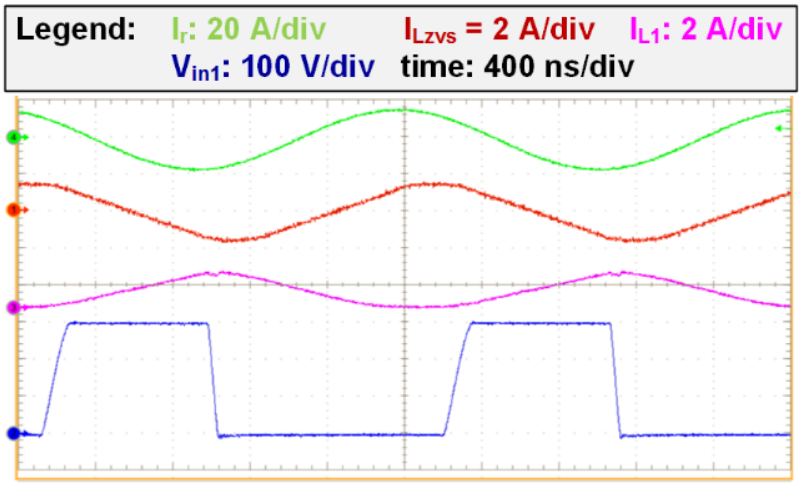
4.6.2. Validation of Constant Frequency Operation under Load Variations

First test is done for the heavy-load condition, which corresponds to the Load-4 configuration. Heavy-load is easiest to measure since low quality-factor of the load makes the tuning process less difficult. Measured waveforms for d = 0.4, and for amplifier at the steady-state are given in Figure 4-29 a) and Figure 4-29 b). It is seen that boost switches are operated at the synchronous condition, and ZVS operation is ensured for buck switches. Measurements for other duty-cycle values are done, and efficiency is computed and shown in Figure 4-30. Peak efficiency is 96.3 %, and the output power reached 362 W for d = 0.5.

Second test is done for Load-2 configuration. Measured waveforms are shown in Figure 4-31 a) and Figure 4-31 b) for d = 0.4. Loaded quality factor is Q = 35, which corresponds to reduction of load coil's resistance by factor of three. The coil's inductance reduced slightly. Boost switches operate at synchronization, while buck switches have ZVS. The current in the input inductor L_1 has negative values, making ZVS condition on buck switches easier. Efficiency and the output power dependence on duty-cycle is given in Figure 4-32. The efficiency drops below 90 % because of large gate driver loss. There are six transistors with 4.5 W of total gate driver loss.



(a)



(b)

Figure 4-29. Test waveforms for V_{bus} = 300 V, f_{sw} = 480 kHz, d = 0.4, Q = 14, and L_r = 7.7 µH. Boost switches are operated in synchronization with the resonant voltage. Buck switches operate at ZVS.

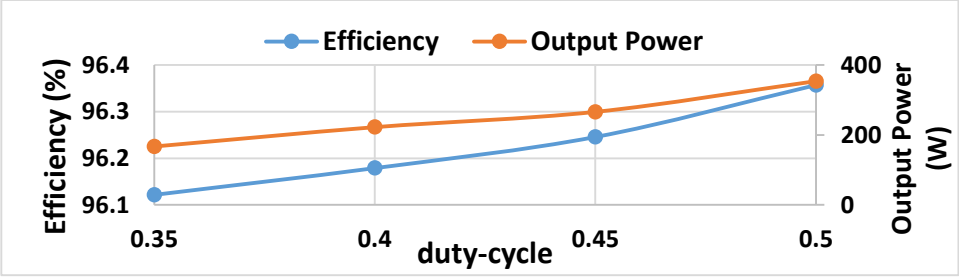
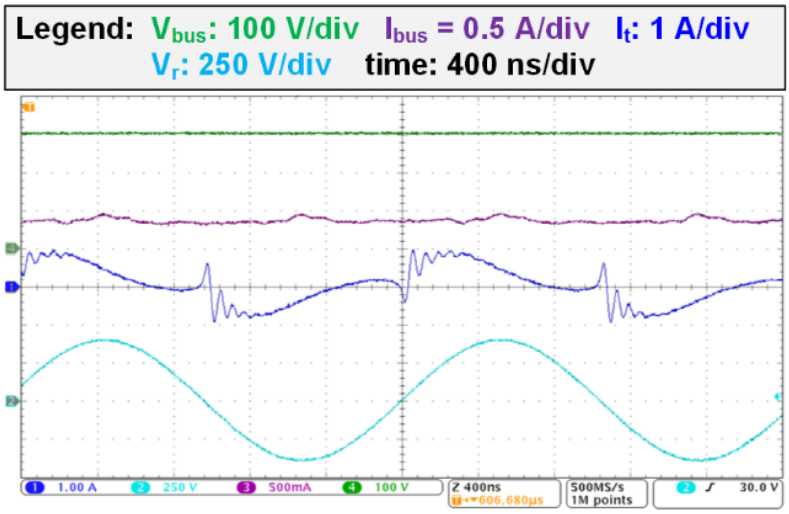
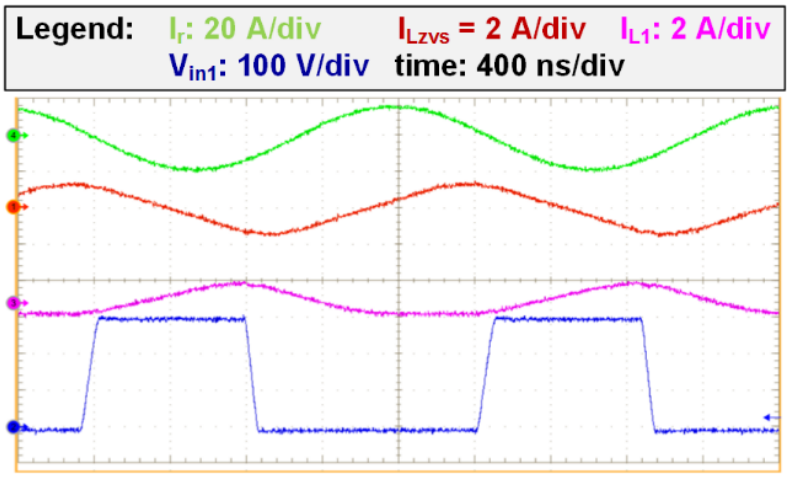


Figure 4-30. Efficiency and output power measurement for Load-4 configuration and different values of duty-cycle. Boost switches operate at synchronous condition, and buck switches operate at ZVS for the whole range.



(a)



(b)

Figure 4-31. Test waveforms for V_{bus} = 300 V, f_{sw} = 480 kHz, d = 0.4, Q = 35, and L_r = 7.65 µH. Boost switches are operated in synchronization with the resonant voltage. Buck switches operate at ZVS.

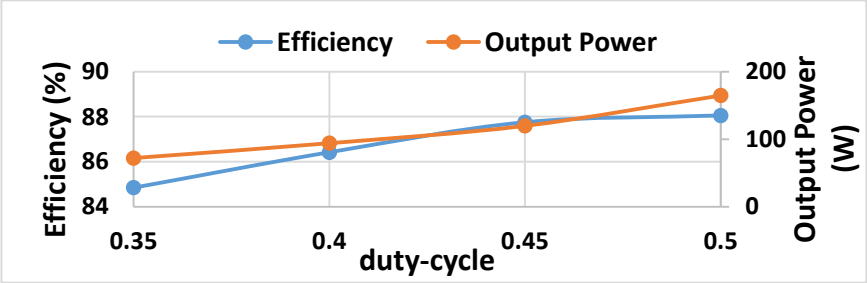
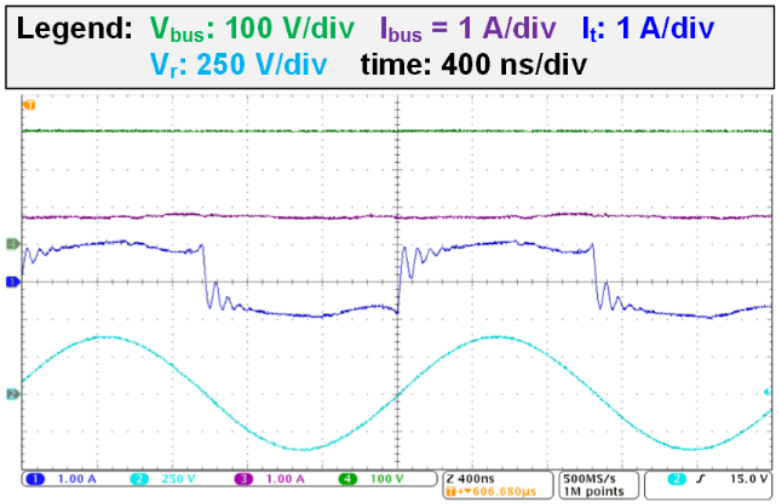
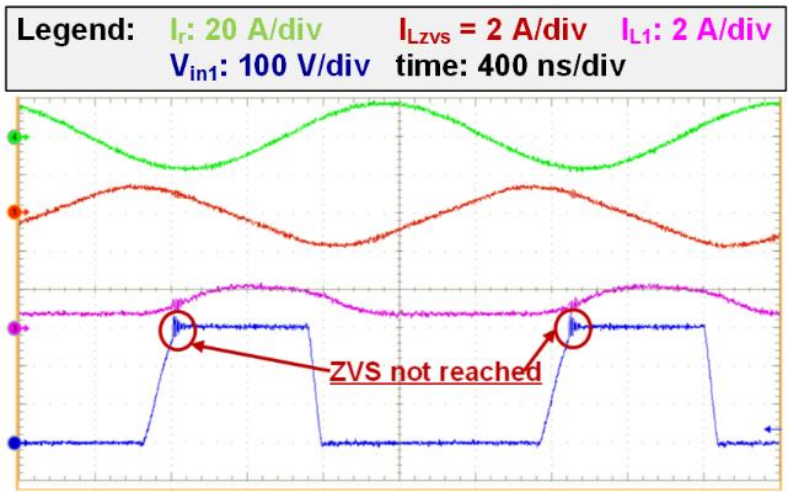


Figure 4-32. Efficiency and output power measurement for Load-2 configuration and different values of duty-cycle. Boost switches operate at synchronous condition, and buck switches operate at ZVS for the whole range.

Third test is done for Load-3 configuration, where load coil's inductance is reduced by 3.5 % while the quality factor of the load is Q = 15. The boost switches operate at synchronous condition, as seen in Figure 4-33 a). Buck switches fail to reach ZVS for d = 0.35 and d = 0.4 since the current in L_1 is more positive at the rising edge of V_{in1} voltage. For d = 0.45 and d = 0.5, buck switches reach ZVS. Efficiency and the output power measurement are given in Figure 4-34. The efficiency drops more steeply when ZVS in buck switches is not achieved. ZVS range for buck switches can be extended by reducing the L_{zvs} inductor, or by increasing the bus voltage, so current in L_{zvs} inductor is larger.



(a)



(b)

Figure 4-33. Test waveforms for V_{bus} = 300 V, f_{sw} = 480 kHz, d = 0.4, Q = 15, and L_r = 7.43 µH. Boost switches are operated in synchronization with the resonant voltage. Buck switches operate at ZVS for d = 0.45 and d = 0.5. Buck switches fail to reach ZVS for d = 0.35 and d = 0.4.

All three tests were successful in keeping boost switches in synchronization with the resonant voltage. The circuit parameters for each load are extracted from measurements, and they are summarized in Table 4-7. The uncompensated synchronous frequency is computed and presented in Table 4-7 for comparison. Around 6 kHz is between synchronous frequency of Load-4 (474.28 kHz) and switching frequency (480 kHz), and around 8 kHz between synchronous frequency of Load-4 and Load-3 (482.41 kHz). Thus, test examples demonstrate compensation of the synchronous frequency for 1-2 %.

The dependence of control variable Ψ_1 on duty-cycle is plotted in Figure 4-35 for theoretical curves based on parameters in Table 4-7 and for actual values used in hardware tests. The theoretical curves are plotted with lines, while values used in hardware tests are represented with diamond markers. The practice matches well the theory. Small deviations are noticeable, and they are expected since it is difficult to make perfect synchronous condition for large values of quality factor. Additionally, the dependence between the control variable and duty-cycle is monotonous, making implementation of the control system easier.

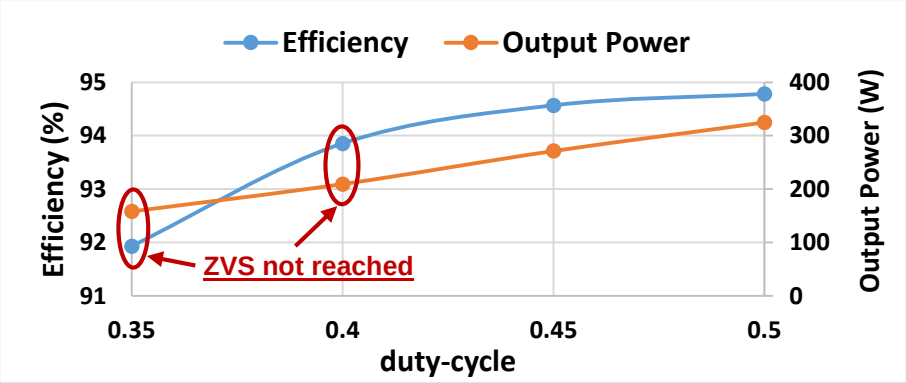


Figure 4-34. Efficiency and output power measurement for Load-3 configuration and different values of duty-cycle. Boost switches operate at synchronous condition, and buck switches operate at ZVS for the whole range.

Table 4-7. Extracted parameters of the resonant tank for each load configuration. Switching frequency is f_{sw} = 480 kHz. Synchronous frequency is compensated for 1-2 % around the base switching frequency.

	Load 2	Load 3	Load 4
L_r (µH)	7.65	7.43	7.7
R_r (Ω)	0.63	1.46	1.63
C_r (nF)	15.12	15.1	15.08
f_{sy} (kHz)	476.16	482.41	474.28

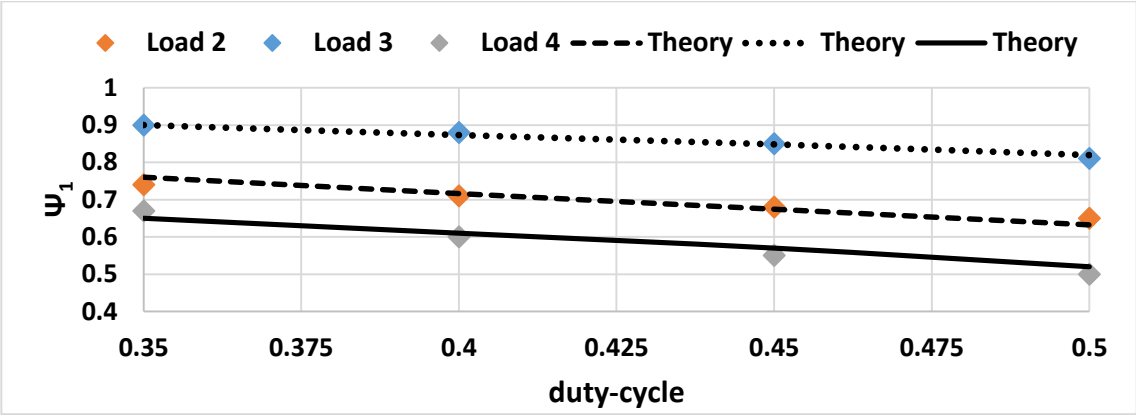
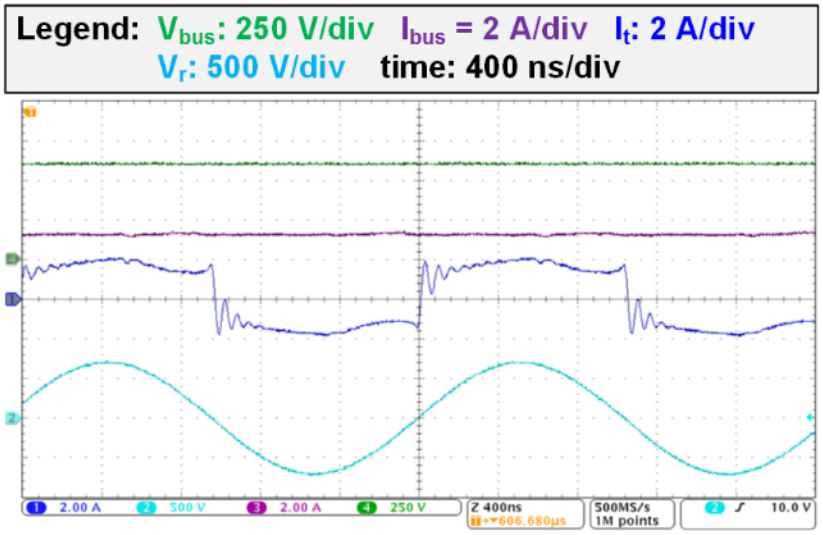


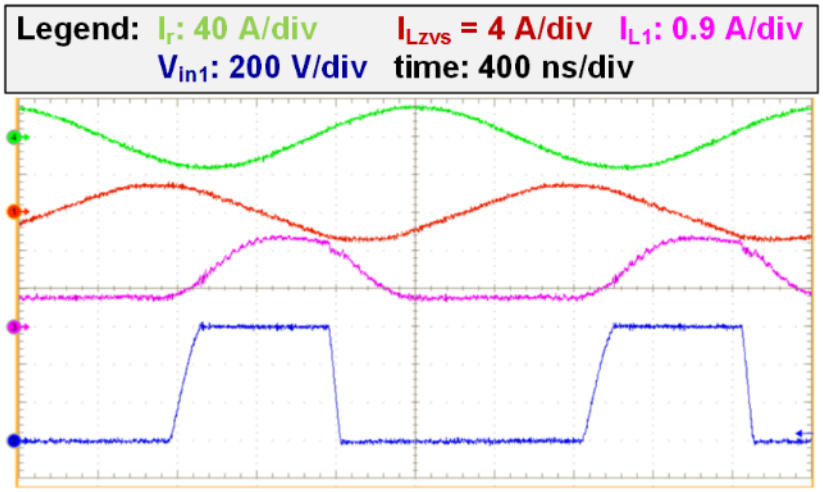
Figure 4-35. Validation of theory on synchronous operation. Markers represent values of control variable Ψ_1 used in hardware tests. Lines represent theoretical curves. Matching is good, validating theory.

4.6.3. Validation of Constant Frequency and Constant Output Amplitude Operation

In this series of test, the switching frequency is kept constant to f_{sw} = 480 kHz, and the bus voltage is varied from V_{bus} = 450 V to V_{bus} = 600 V. Duty-cycle is adjusted so the amplitude of the output voltage is kept to V_{rm} = 700 V. Load-3 is used for demonstration of the constant amplitude operation. Generation of gate driver's PWM signals, and measurement setup is the same as for previous series of tests. Measurements for V_{bus} = 600 V are shown in Figure 4-36 a) and Figure 4-36 b). The boost switches operate at synchronous condition. The buck switches are operating under ZVS.



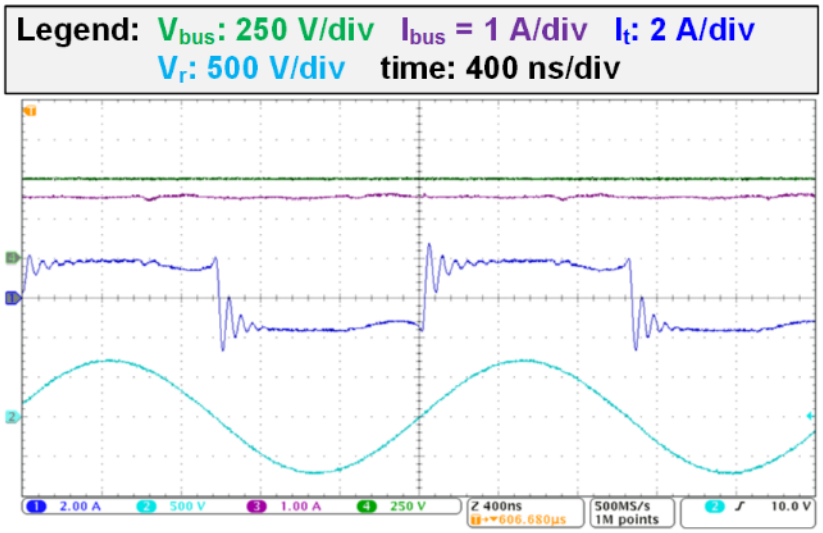
(a)



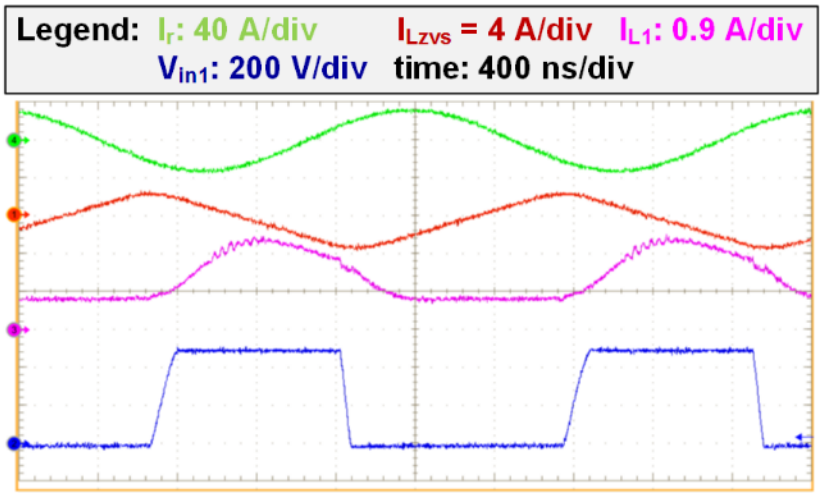
(b)

Figure 4-36. Measured waveforms for V_{bus} = 600 V, f_{sw} = 480 kHz, d = 0.37, and Ψ_1 = 0.89. Amplitude of the output (resonant) voltage is V_{rm} = 700 V. Amplitude of the load current is I_{rm} = 32 A.

Figure 4-37 a) and Figure 4-37 b) show measured waveforms for V_{bus} = 500 V and d = 0.44. The amplitude of the output voltage is kept to V_{rm} =700 V. Boost switches operate at synchronous condition, while buck switches operate at ZVS. Figure 4-38 shows the efficiency and output power of the buck-boost amplifier. Efficiency is 95 % flat, since boost amplifier is driven basically for almost the same driving conditions (input current to the boost does not change significantly). There is slight variation of the output power, which occurred due to inability to set V_{rm} precisely to 700 V.



(a)



(b)

Figure 4-37. Measured waveforms for V_{bus} = 500 V, f_{sw} = 480 kHz, d = 0.44, and Ψ_1 = 0.85. Amplitude of the output (resonant) voltage is V_{rm} = 700 V. Amplitude of the load current is I_{rm} = 32 A.

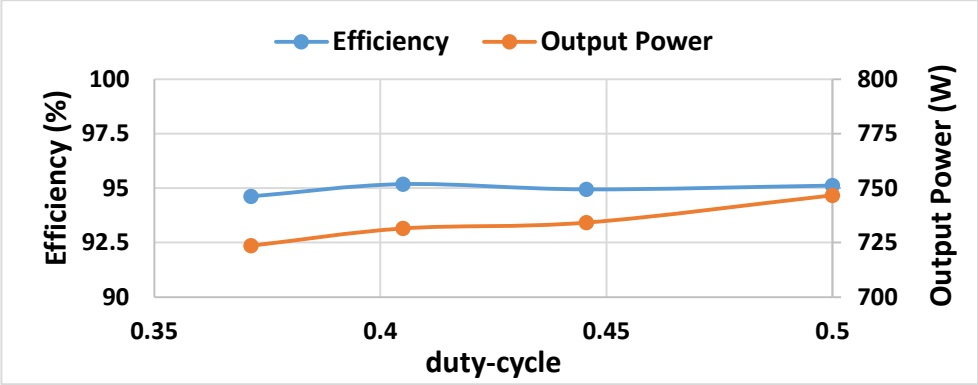


Figure 4-38. Efficiency and output power for the buck-boost amplifier operated at f_{sw} = 480 kHz, V_{rm} = 700 V, and I_{rm} = 32 A.

4.7. Conclusions

Two-phase buck-boost amplifier is proposed to improve overall performance of current-fed resonant inverters. Common drawbacks of current-fed topology are solved, such as series diode in switch configuration, large input inductor, and sensitivity load variations. Efficiency of the buck pre-regulator is improved by employing ZVS using two-phase configuration with an inductive tank between the phases. Efficiency of the boost stage is further improved by reducing current stress in the switches. Fixed frequency operation is confirmed, where either load (1-2 % change of synchronous frequency), or input voltage is varied (25 % change). A demonstration amplifier is built and tested for the power level of 11.3 kVA of reactive and 0.7 kW of active power. The efficiency is around 95 %.

Immunity to load variations is accomplished by phase-shifting the switching function of the buck stage with respect to boost stage. The circulating current between one buck phase, resonant tank, and another buck stage is controlled by this phase-shift. When reflected to the side of the resonant tank, buck-boost amplifier behaves as a current source with controllable output admittance. The admittance is in fact an adaptable matching circuit that is able to compensate for the reactive part of the resonant tank's impedance.

The power to the load is transferred via dc, first, and second harmonic of the equivalent current source that replaces input inductors to the boost. In conventional boost amplifier (current-fed resonant inverter), the current in the input inductors is designed to be dc, and whole power is transferred using dc component. It is determined that power transfer using dc component increases stress of the switches in the boost stage, and that better idea is to transfer power using fundamental component of the input inductor's current.

The developed theory in this chapter is also applicable to the case of boost amplifier with bidirectional voltage-blocking switches, consisted of series configuration of transistor and diode. The GSSA model (used in derivation of the active compensation) is created around an equivalent buck-boost amplifier employing ideal switches that are able to block both positive and negative voltages. The only difference is that ideal switch conducts current in both directions, whereas the switch consisted of series configuration of diode and transistor can conduct current only in one direction. Thus, the theory presented here can be employed for topologies with series diodes only if the switch current is strictly positive.

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Chapter 5. Conclusion and Future Work

5.1. Conclusion

This dissertation examines the applicability of current-fed resonant inverter topology for a driver of an inductive coil with high quality-factor. The main issues are low bandwidth due to large input inductance, large conduction loss of series diodes in the switching stage, low efficiency of the buck pre-regulator, and sensitivity to load variations.

The introduction to the dissertation is given in Chapter 1. It describes characteristics of resonant inverters, and methods of suppressing load variation in a power electronics converter. Boost amplifier topology, a resonant inverter with two input inductors, is recognized as a potential topology to overcome all of the issues associated with the current-fed resonant topology. In Chapter 2, the boost amplifier is analyzed for reduced value of the input inductance and high quality-factor of the load. Series diodes in switch configuration are eliminated since the transistors can be turned on at zero voltage and without degrading current spike. A current snubber structure is introduced in absence of series diodes to improve reliability during transients and faults. The snubber utilizes parasitic series inductance between the resonant tank and the switching stage, and it is more efficient than diodes. The synchronous frequency, at which transistors are turned on at zero voltage, is found to be a mathematical function of the input inductance and the parameters of the resonant tank. Efficient operation without switching loss is obtained for reduced value of the input inductance. As consequence of the reduced input inductance, the input current is not strictly dc anymore.

Chapter 3 develops a mathematical large-signal model of the amplifier that is used in synthesis of the output waveforms for transient and steady-state modes, Hann-function, and trapezoidal-function envelopes. In Chapter 4, a two-phase buck with zero-voltage switching (ZVS) is proposed to improve the efficiency of the buck pre-regulator. The mathematical model is used for optimization of the two-phase buck. It was found that the buck pre-regulator operation can be phase-shifted relative to the operation of the boost amplifier in order to control the zero-crossing of the output voltage. The boost switches can now turn-on at zero voltage, even in the presence of wide load variations. In addition, current stress in all components can be reduced. As a consequence, the current in the input inductors has multiple harmonics with dominant fundamental harmonic. The dc component is minimized as it creates conduction loss in boost switches.

The proposed two-phase buck-boost solution overcomes all of abovementioned limitations of the current-fed resonant inverters. The developed theory is covered with a large number of circuit simulations and hardware tests. Up to 98.5 % efficient boost amplifier with power levels of 14 kVA for reactive and 1.25 kW for active output power is presented. Also, around 95 % efficient buck-boost amplifier is presented for power levels of 11.3 kVA for reactive and 0.7 kW for active output power.

5.1.1. List of Contributions

The major contributions of the dissertation are summarized in this section. In Chapter 2, the operation of the boost amplifier is analyzed. The major contributions include:

1. The impact of input inductance on synchronous frequency is found (2-58), which allowed the reduction of the input inductance by an order of magnitude. The bandwidth of the system is increased approximately four times Table 2-9.
2. The lossy series diodes in switch configuration are replaced with current-spike limiting snubber of up to 3 times less loss (Figure 2-52).
3. The loss model of the amplifier is developed (section 2.4.3).
4. The loss model is used to minimize the input inductance value without significantly sacrificing efficiency. The input inductor's size is reduced 2.34 times. Trade-offs between size of the input inductor, system bandwidth, and efficiency are well studied (section 2.4.6).
5. A detailed step-by-step design procedure is given (section 2.6.2).
6. A highly efficient system is developed, with efficiency in the range from 96.5 % to 98.5 % for 14kVA of output reactive power. The active power peaked at 1.25 kW (section 2.7).

In Chapter 3, the major contribution include:

1. The mathematical large signal model of the boost amplifier is developed (section 3.3).
2. The model is used to synthesize output waveforms with an envelope. Hann-function and trapezoidal-function envelopes are reported (section 3.6).
3. The model is used later in Chapter 4 to optimize the operation of the buck-boost amplifier.

In Chapter 4, a two-phase buck-boost amplifier is proposed for amplitude control of the high-frequency output. The major contributions include:

1. Efficiency improvement in the buck pre-regulator stage thanks to implemented zero-voltage switching (section 4.5.1).
2. Efficient and reliable operation of the boost stage at fixed frequency by implementing a compensation method that functions as an adaptable matching circuit to the resonant tank (section 4.4.4).
3. Reduction of the current stress in switches of the boost stage (section 4.4.5).
4. A highly efficient system is demonstrated, with efficiency of around 95 % for 11.3 kVA output reactive power and 0.7 kW output active power under the steady-state (section 4.6).

5.1.2. Intellectual Merit

Standard implementation of a current-fed inverter requires a large input inductor to make input current constant. The series diodes in switch configuration are typically present, however, if the synchronization of the switches turn-on and zero-crossing of the output voltage is achieved, the diodes can be left out. Conceiving a two-phase buck-boost topology had to break up with standard practice and sometimes even required counter-intuitive measures. In Chapter 2, the following intellectual barriers had to be crossed:

1. In order to achieve large bandwidth in the system, input inductance needs to be reduced by an order of magnitude. Reduction of the input inductance introduced appreciable first harmonic component of the input inductor current. A group from Auckland University proposed a current-splitting transformer to mitigate influence of the first harmonic, however, that approach has not been pursued since the fundamental current can be very useful for system with amplitude control.
2. Synchronization of the switches turn-on and the zero-crossing of the output voltage depends on the current harmonics in the input inductors, and occurs for a particular frequency, termed *synchronous frequency*. It has been concluded that this name is more appropriate than *resonant frequency* which is defined for sinusoidal excitation, or *ZVS frequency* which can correlate to a band of frequencies. Furthermore, it is concluded that *synchronous frequency* is controllable and does not depend on circuit parameters only.
3. A snubber structure adds a safety measure to the current-fed resonant inverter with no series diodes in switch configuration. It is a fail-safe mechanism for instances where the amplifier is not kept in perfect synchronization. The series inductance between resonant tank and the switching stage, once seen as a

parasitic and degrading element, can be used in the snubber structure. In this particular case, the snubber consumes around three times less loss than the series diodes.

In Chapter 3, a modeling methodology includes the non-linearity of the boost amplifier, while converting circuit from time-variant to time-invariant system. In this way, the behavior of the boost amplifier in non-optimal condition is preserved. The model is then used in Chapter 4 to design a compensation system for the variations of the input voltage and load's parameters. From analyzing the proposed buck-boost topology, it was recognized that:

1. Fundamental frequency current in the input inductors can be utilized and controlled to provide the synchronous frequency compensation, and ensure fixed frequency operation even in the presence of variations from input voltage and load's parameters.
2. The proposed system has benefits to transfer the power to the load by using a fundamental frequency component. The dc component, normally used to transfer power, increases conduction loss in the boost switches. The fundamental frequency current does not flow though switches and thus does not create loss. Thus, current stress in switches is reduced when fundamental frequency component is used in power transfer.

After the changes proposed in this dissertation, very little survived from the traditional current-fed resonant inverter. There are no series diodes in the switch configuration. Input inductance is small with the tendency to become comparable to the inductance of the load coil. The current in the input inductors, while once pure dc, now is largely sinusoidal. However, the resultant topology is still a current-fed resonant inverter, except for the input current source is comprised of the dc, first, and second harmonics. The buck boost amplifier represents an equivalent current source with a controllable output admittance (matching circuit) driving a resonant tank.

5.1.3. Limitations

All conclusions developed in this work are limited to the analyzed case of loaded quality-factor larger than ten. The high-Q makes the resonant tank behave as a very selective filter, and the output variables (voltage and current) can be considered as purely sinusoidal signals. This assumption makes the analysis easier. In the case of a low-Q load, the third and other odd harmonics may be present in the spectra of the output variables. Finding the analytical solution of the synchronization problem becomes complicated, and a reported work presents the numerical solution to the problem. The search for an analytical solution can be attempted by extending the circuit model presented in Chapter 3.

Another limitation case is for extremely high Q-factor, around 200, where modeling the method has a significant error. This fact was reported in Chapter 3. The model of the boost amplifier works well for all reasonable input inductance values, with limitation on inductance's minimum value to about four times higher than the load's coil inductance.

5.1.4. Impact on Applications

The buck-boost amplifier has been developed for applications with highly inductive and varying loads such as induction heating, wireless power transfer, and magnetic resonance imaging. The proposed topology enables fixed frequency operation with excellent efficiency, high bandwidth, safe operation at no-load condition, and reduced size of magnetic components. It is a versatile topology that can be designed for higher power, frequency, and ambient temperature. If required, a topology with galvanic isolation or dc output is easily derived.

The topology uses unidirectional voltage-blocking switches, so bidirectional power flow is allowed. Thus, the topology is suitable for wireless power chargers for electric vehicles that require bidirectional operation for both vehicle-to-grid and grid-to-vehicle power delivery.

Power scaling is easily achieved in the boost stage by paralleling more transistors. Output capacitance comprises the resonant capacitor, so a large number of parallel transistors can be placed. The buck stage can parallel limited number of transistors because their output capacitance limits the ZVS range. Instead, more parallel phases can be introduced, comprising of a phase-leg and an inductor connecting the mid-point of the phase-leg and one terminal of the resonant tank. With a larger number of phases the switching frequency of each phase can be reduced, while having the same ripple current flowing through the switches and the resonant tank.

Silicon carbide MOSFETs and diodes are chosen for amplifier implementation for their low-loss operation at high frequency. All switches exhibit low loss, so the temperature rise of the transistor's junction is not significant. The passives such as the gate resistor and resonant capacitors are recognized as thermal hotspots of the system. Paralleling devices on a larger area solves this issue. Thus, the topology can be translated for high ambient temperature environments, such as induction melting furnace.

Scaling the frequency up is possible. The boost stage requires adaptation of the resonant tank, typically achieved with subtracting a resonant capacitor. In practical applications, a bank of capacitors and switches exist so the operation

of the amplifier can be tuned for a particular frequency band. The buck stage relies on a ZVS mechanism that requires significant dead time. Considering practical limitations, such as output capacitance of the MOSFET, some redesign of the buck stage should be considered for switching frequencies in the megahertz range. Another option is the use of the multi-phase design, as explained for power scaling.

An isolated variation of the buck-boost topology is feasible. Two different approaches can be found in the literature. A transformer is placed between the load and the resonant capacitor, as in wireless power transfer or induction heating. It is also possible to couple input inductors with the output.

The proposed topology can also be used in dc/dc applications. A rectifier can be added to the output, with or without an isolation transformer. Similar topologies were reported before for converters interfacing solar panels. Voltage gain of around ten is possible if a transformer with 3:1 turn ratio is added.

5.2. Future Work

The research on buck-boost topology is opened in this dissertation. The principles of operation are shown, and basic properties are derived. However, there is a great room for improvements and many directions for this research to branch out. In the sections below, some directions for the continuation of the research on buck-boost topology are given.

5.2.1. Implementation of Control Loop

Power amplifiers developed in this dissertation are implemented with no control loop in the inverter stage. Chapter four demonstrated monotonous dependence of control variable Ψ_1 (relative phase-shift between buck and boost stages) on the duty-cycle, making control easier for slowly changing the duty-cycle due to variations of the input voltage. The synchronization can be controlled using phase-locked loops (PLLs) or self-oscillating switching (SOS) methods, by accommodating the Ψ_1 value. State-of-the-art current-fed resonant inverters already employ PLLs and SOS whose synchronization is controlled by varying frequency. Thus, the design of PLL or SOS-based control mechanism is the next step of development for buck-boost amplifier.

5.2.2. Continuous Operation and High-precision Efficiency Measurement

Implementation of the control loop will enable continuous tuning of the buck-boost amplifier. The testing will be significantly easier for cases of large quality-factor loads, since the control loop will keep the amplifier in

synchronization for variations of the circuit parameters. The amplifier can then be operated in the continuous mode, where parametric variations due to temperature change are not detuning the amplifier from synchronization. Next, a more precise measurement system can be employed. On the input side, a pair of multi-meters is sufficient to measure mostly dc signals. On the AC side, load coils can be placed in the enclosure filled with oil. The enclosed system can be temperature-calibrated for a given power loss. The data can be used in the actual power test to determine the temperature increase of the enclosure and related power loss.

5.2.3. Optimization of Magnetic Components for Improved Efficiency

Implemented inductors in Chapters 2-4 suffer from excessive conduction power loss in the windings because of proximity effect. The efficiency at the heavy load can be improved by around 1 % if the proximity effect is controlled.

5.2.4. Extension to Low Quality-factor Loads

The proposed topology in this dissertation assumes that the loaded quality-factor is high (larger than ten). The modeling approach can be extended for a low quality-factor case, where higher harmonic components are considered for the output voltage and current, and for input inductors.

5.2.5. Synthesis of Output Waveforms with Envelope Using Buck-Boost Amplifier

Operation of the buck-boost amplifier is demonstrated for the steady-state operation only. The synthesis of output waveforms with envelopes has not been tried yet. The comparison with cascaded buck-boost is required to evaluate the performance.

5.2.6. Investigation on Properties of Buck-boost Amplifier with Near-zero Transistor Loss in the Boost Stage

Chapter four demonstrated that the buck-boost can transfer almost whole power to the load at the fundamental frequency component. The current flowing though the transistors in the boost stage would be minimized, as well as the power losses. The properties of the amplifier for such mode of operation are yet to be explored.

5.2.7. Efficiency Optimization Using Frequency Control

Frequency, duty-cycle, and control variable Ψ can be controlled for optimization of the efficiency for buck-boost amplifier. At light-load, the amplifier can be operated for minimum ripple current in the input inductors, minimizing

core losses in inductors. At heavy-load, the current in the boost transistors can be minimized as described in the previous section. With such control mechanism, overall efficiency from light-load to heavy-load can be optimized.

5.2.8. Design of Multi-phase Buck Converter

A multi-phase buck design is possible if either frequency or power have to be scaled up. Each buck can be connected to the either side of the resonant tank via an input inductor. The buck transistors would operate at a lower frequency than the ones from boost, however, the fundamental frequency of the current flowing to switches and resonant tank should match the switching frequency of the switches.

Appendix A. Simulation Models for Section 2.2

This appendix contains screenshots of LT spice simulation models that used to plot boost amplifier's waveforms in section 2.2.

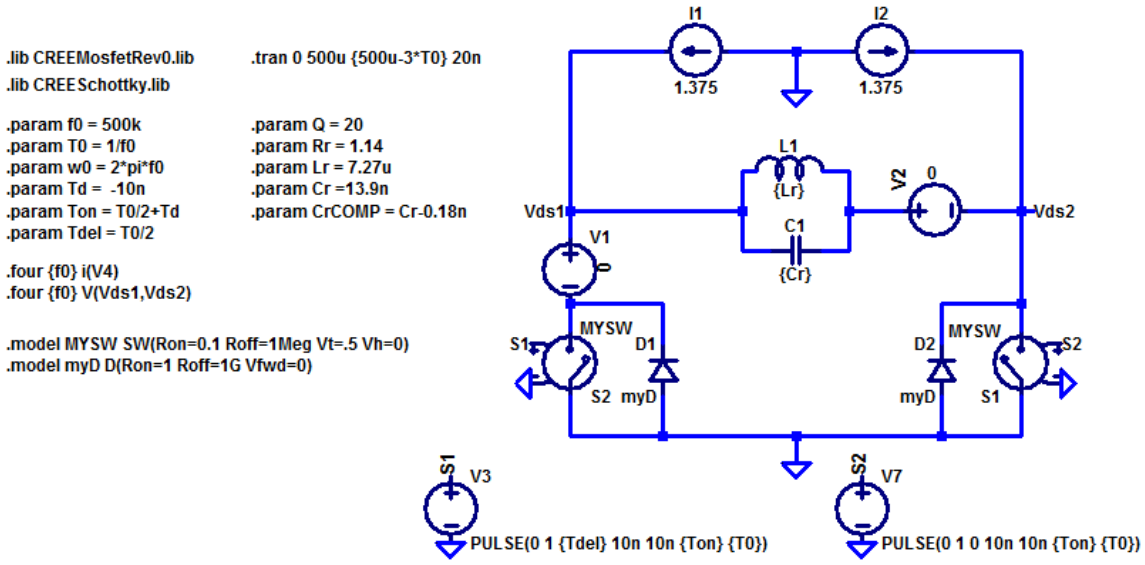


Figure A-1. Simulation model that was used to generate Figure 2-9.

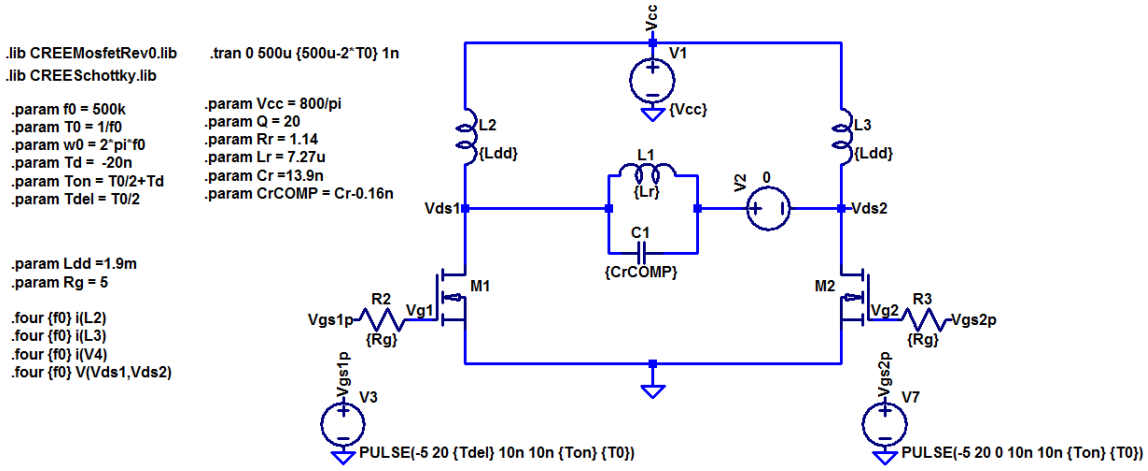


Figure A-2. Simulation model that was used to generate Figure 2-11.

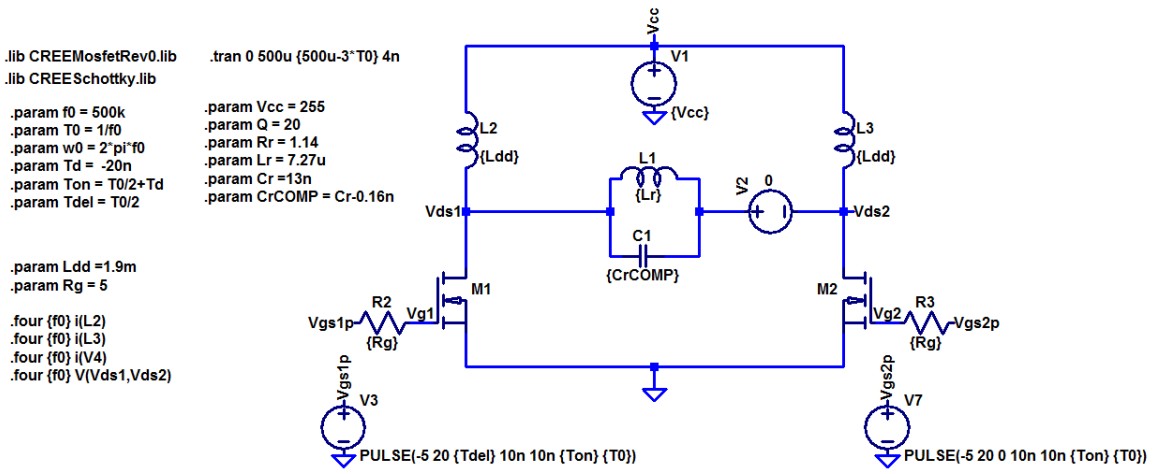


Figure A-3. Simulation model that was used to generate Figure 2-12.

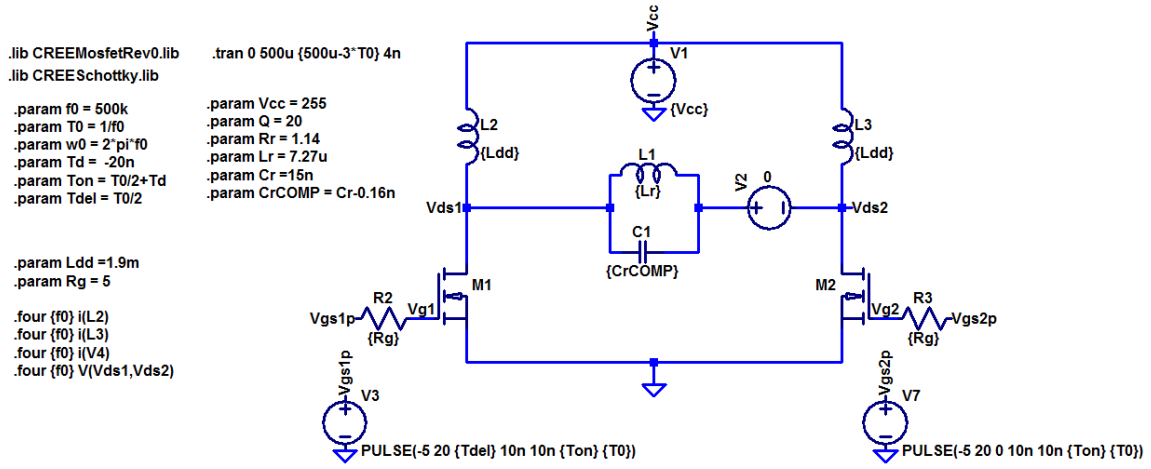


Figure A-4. Simulation model that was used to generate Figure 2-13.

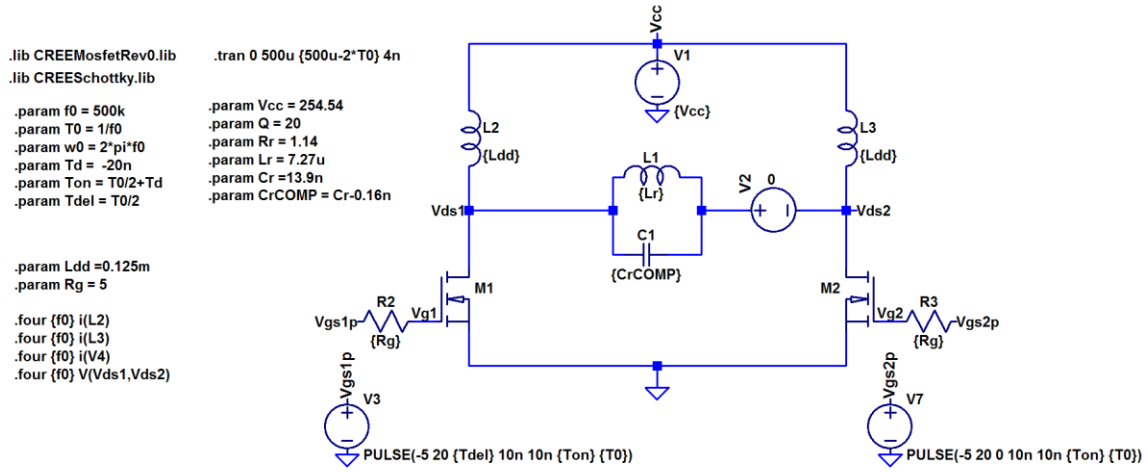


Figure A-5. Simulation model that was used to generate Figure 2-14.

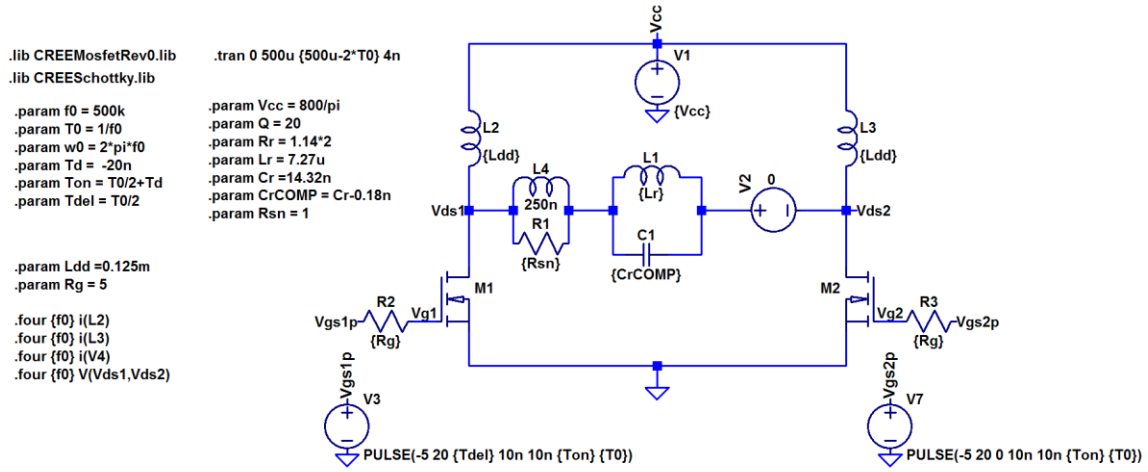


Figure A-6. Simulation model that was used to generate Figure 2-15.

Appendix B. The Computation of $C_{oss,eq}$ Using Saber

The non-linear output capacitance (C_{oss}) of a transistor switch impacts the time-domain behavior of high frequency converters [1-4]. In case of the boost amplifier, the C_{oss} capacitor is comparable to the linear capacitor $C_{r,PCB}$ that is in parallel configuration with it (Figure 2-10). The C_{oss} and $C_{r,PCB}$ comprise the resonant capacitor C_r. For the convenience of the circuit design, the C_{oss} is often substituted with a linear capacitor $C_{oss,eq}$ that stores the same charge for given voltage [4]. Then the resonant capacitance is computed as the sum of $C_{oss,eq}$ and $C_{r,PCB}$:

$$C_r = C_{oss,eq} + C_{r,PCB} \tag{B-1}$$

The value of capacitance $C_{oss,eq}$ is good starting point since it does not reflect the behavior of the non-linear capacitance [2, 4]. Thus, for best performance either capacitance $C_{oss,eq}$ or switching frequency require some tuning. The computation of $C_{oss,eq}$ is done based on the data specified in the transistor's datasheet. In the case of used CREE CMF20120 MOSFET, manufacturer specifies the stored energy (E_{oss} = 62 uJ) in the output capacitor for an applied voltage (V_{ds} = 800 V). The relationship between the two is simple

$$E_{oss} = \frac{1}{2} C_{oss,eq} V_{ds}^2 \tag{B-2}$$

The equivalent output capacitance is then computed as $C_{oss,eq}$ = 194 pF. This approach is the most simplistic, but it is applicable only if applied voltage is indeed 800 V. For V_{ds} < 800 V, the graph with E_{oss} dependence on the applied voltage V_{ds} can be used. The data from the graph can be extracted with the help of dedicated software and then the equation $E_{oss} = \frac{1}{2} C_{oss,eq} V_{ds}^2$ (B-2(B-2) is applied to calculate $C_{oss,eq}$. When V_{ds} > 800 V, the graph with the C_{oss} capacitance's dependence on the applied voltage should be used Figure B-1. The following text contains set of instructions to compute the $C_{oss,eq}$.

Extraction of the data and conversion to the numeric format is done with tools incorporated in Saber Sketch program. After opening the program, click *Model Architect* icon at the bottom of the screen. Among a set of supported tools, *Scanned Data Utility* should be opened. Click on *File*, then *Import Image*, and then select the print-screen from the page of datasheet where the C_{oss} graph is given. The blue frame has to be placed directly over the borders of the graph. Click on *Edit*, then *Axis definition*. Set the both x-axis and y-axis as it is in the datasheet graph. The x-axis

starts from zero and its maximum is at eight hundred. The scale is linear. The y-axis is in logarithmic scale, with the start at ten and maximum at ten thousand. The screen should look like in Figure B-2.

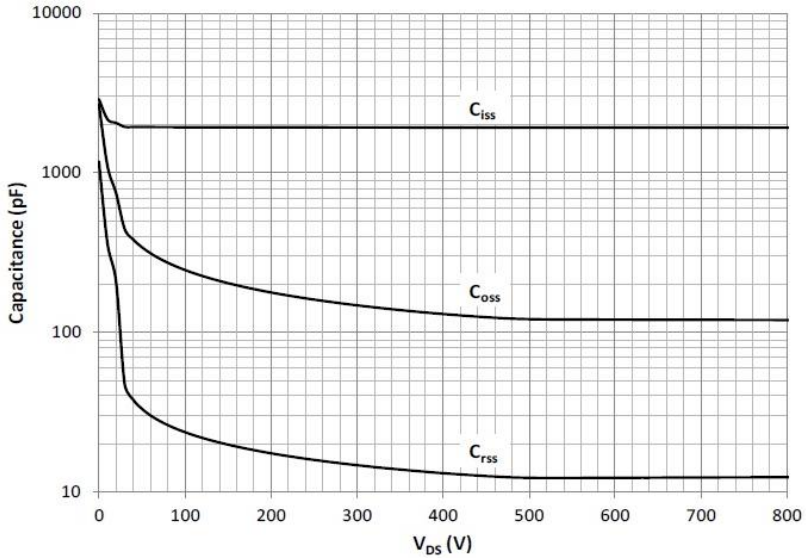


Figure B-1. The non-linear capacitance C_{oss} dependence on drain-source voltage of the MOSFET. The graph is taken from CREE's CMF20120 MOSFET datasheet.

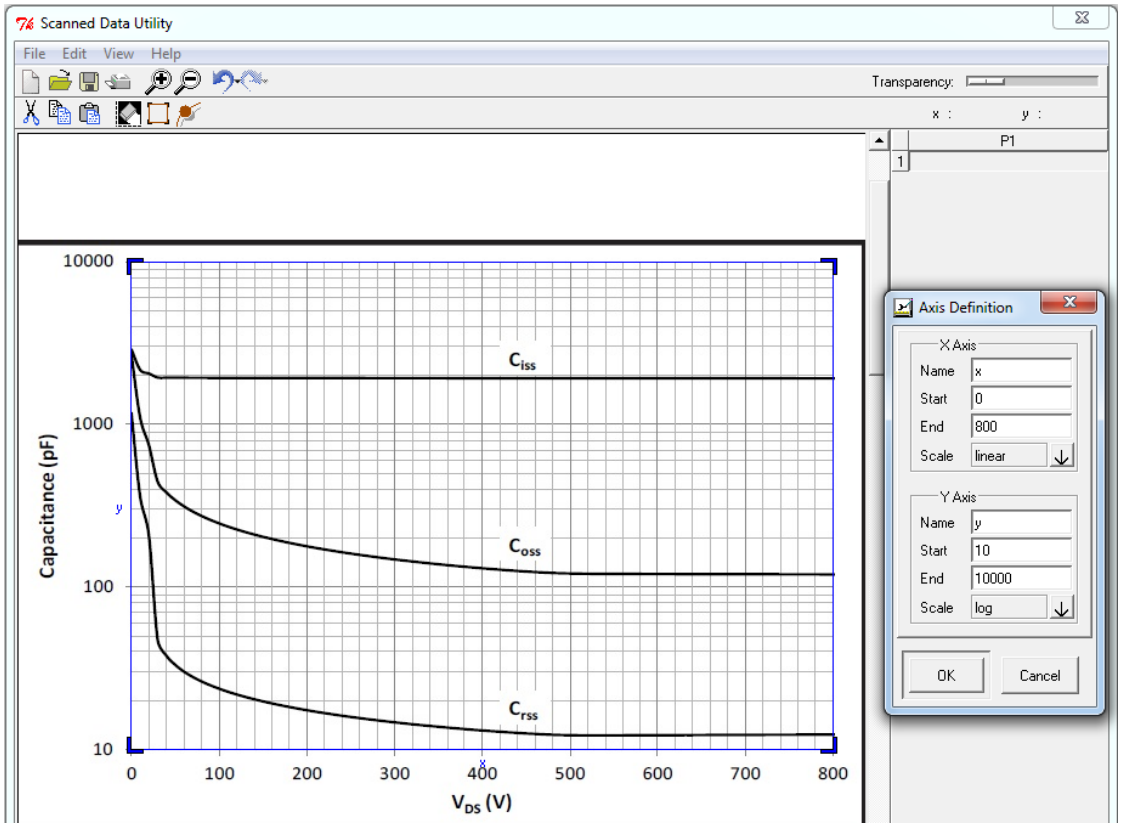


Figure B-2. Setting the blue frame over the borders of the C_{oss} graph. The x-axis and y-axis definition is set as it is in the graph. The C_{oss} curve data points can be mapped now.

Next, the data points are to be inserted. Click on *Edit*, then *New Curve*. Insert a point-by-point, until the C_{oss} curve is mapped (interpolated). At first the dots and connecting lines will be in red, but they will convert to blue color when the insertion is completed. Both the dots and the lines should follow the C_{oss} curve. The screen will look like on in Figure B-3.

The C_{oss} curve can be exported under the *File* menu. *Scope plotfile* is convenient since the data can be manipulated using CosmosScope™ tool. The tool is very convenient for data manipulation and graphic representation. Now the C_{oss} information is entered and ready for manipulation. Under CosmosScope™ the calculator option should be selected. The calculator is able to perform mathematical operation on the waveforms and graphs. The C_{oss} curve should be integrated and plotted by first entering the curve's name into the calculator and then clicking *integ* button. The *integ* function performs the integration operation and calculates the stored charge Q_{oss} for applied voltage:

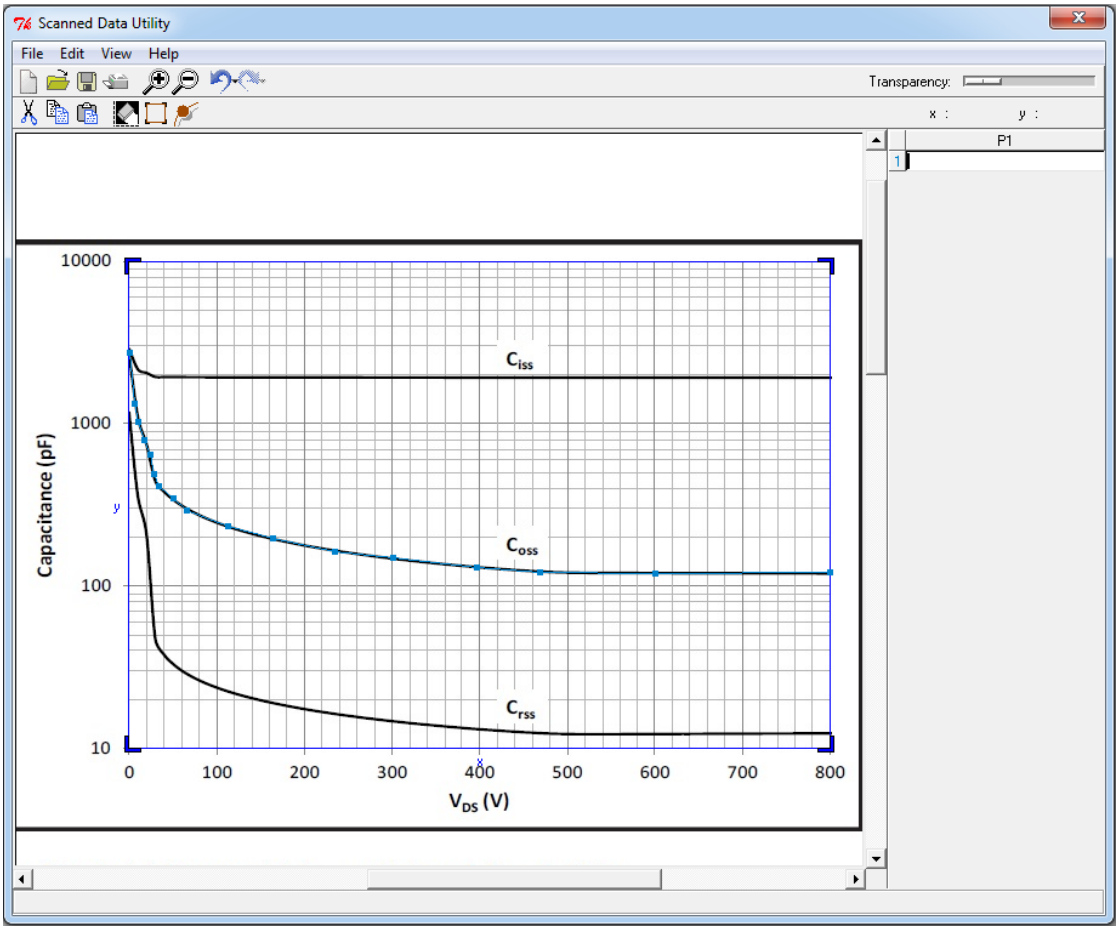


Figure B-3. The non-linear capacitance C_{oss} is interpolated by entering the dots on the C_{oss} curve.

$$Q_{oss} = \int_0^{V_{rm}} C_{oss}(V)dV \tag{B-3}$$

where V_{rm} is the amplitude of the resonant tank's voltage (2-16). The result is plotted and the markers are entered to read the values from the plots. The screen should look like in Figure B-4. For the simplicity, the Q_{oss} is rounded to Q_{oss} = 157 nC at V_{rm} = 800 V. The Q_{oss} calculation can be easily extended for voltages larger than 800 V since the capacitance C_{oss} does not change significantly after 600 V and it equals to C_{oss} = 121 pF as indicated by the plot in Figure B-4. It can be written

$$Q_{oss} = 157nC + \int_{800V}^{V_{rm}} 121pF \cdot dV \tag{B-4}$$

For V_{rm} = 1000 V, the stored charge is Q_{oss} = 181 nC. The equivalent output capacitance $C_{oss,eq}$ is then computed as

$$C_{oss,eq} = \frac{Q_{oss}}{V_{rm}} \tag{B-5}$$

The V_{rm} = 800 V gives $C_{oss,eq}$ = 196 pF, while V_{rm} = 1000 V gives 181 pF.

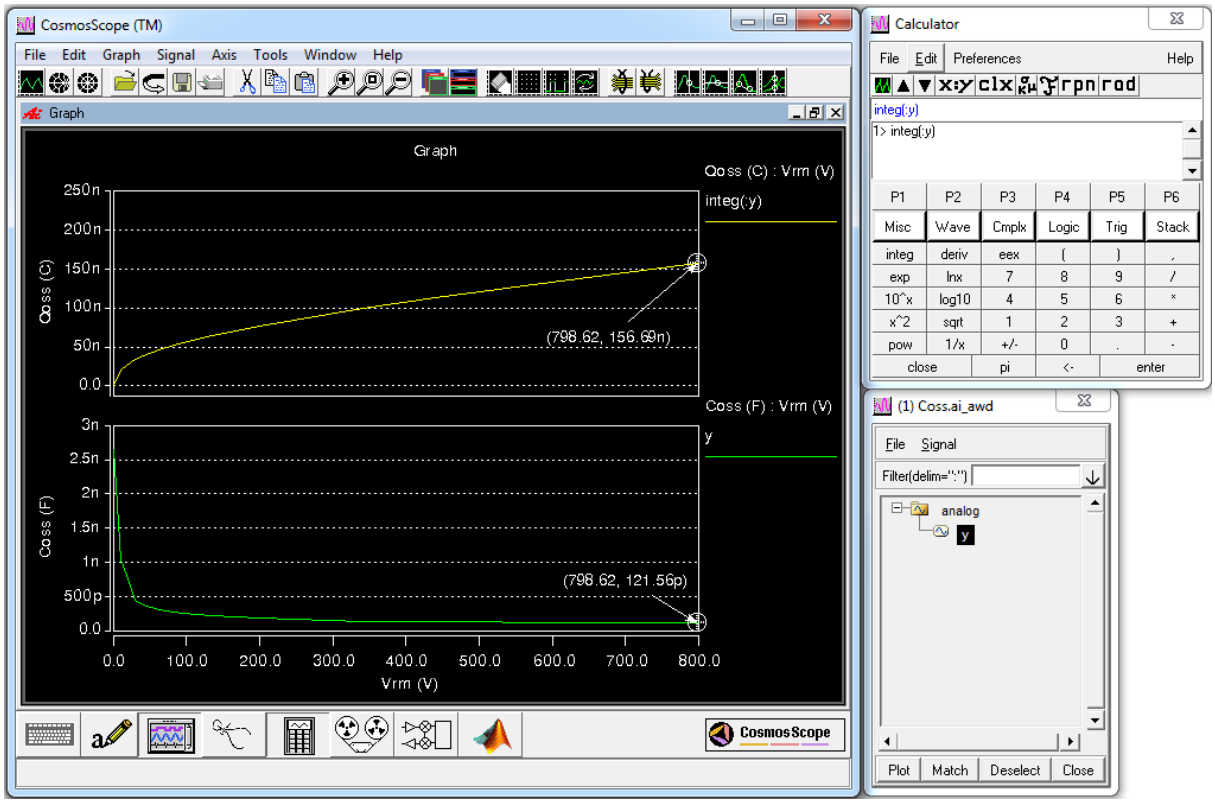


Figure B-4. Calculation of the stored charge of the non-linear MOSFET output capacitance using Saber's CosmosScope™.

References

[1] Gauen, K.: 'The effects of MOSFET output capacitance in high frequency applications', in Editor (Ed.)^(Eds.): 'Book The effects of MOSFET output capacitance in high frequency applications' (1989, edn.), pp. 1227-1234 vol.1222

[2] Franz, G.A., Walden, J.P., Scott, R.S., Bicknell, W.H., and Steigerwald, R.L.: 'Use of accurate MOS models for optimizing resonant converter designs', in Editor (Ed.)^(Eds.): 'Book Use of accurate MOS models for optimizing resonant converter designs' (1990, edn.), pp. 1564-1568 vol.1562

[3] Sekiya, H., Watanabe, T., Suetsugu, T., and Kazimierczuk, M.K.: 'Analysis and Design of Class DE Amplifier With Nonlinear Shunt Capacitances', Circuits and Systems I: Regular Papers, IEEE Transactions on, 2009, 56, (10), pp. 2362-2371

[4] Drofenik, U., Musing, A., and Kolar, J.W.: 'Voltage-dependent capacitors in power electronic multi-domain simulations', in Editor (Ed.)^(Eds.): 'Book Voltage-dependent capacitors in power electronic multi-domain simulations' (2010, edn.), pp. 643-650

Appendix C. Simulation Models for Section 2.2

This appendix contains screenshots of Mathcad Prime program used in design calculations of the input inductor, described in section 2.4. Each page of the program is given as a separate figure.

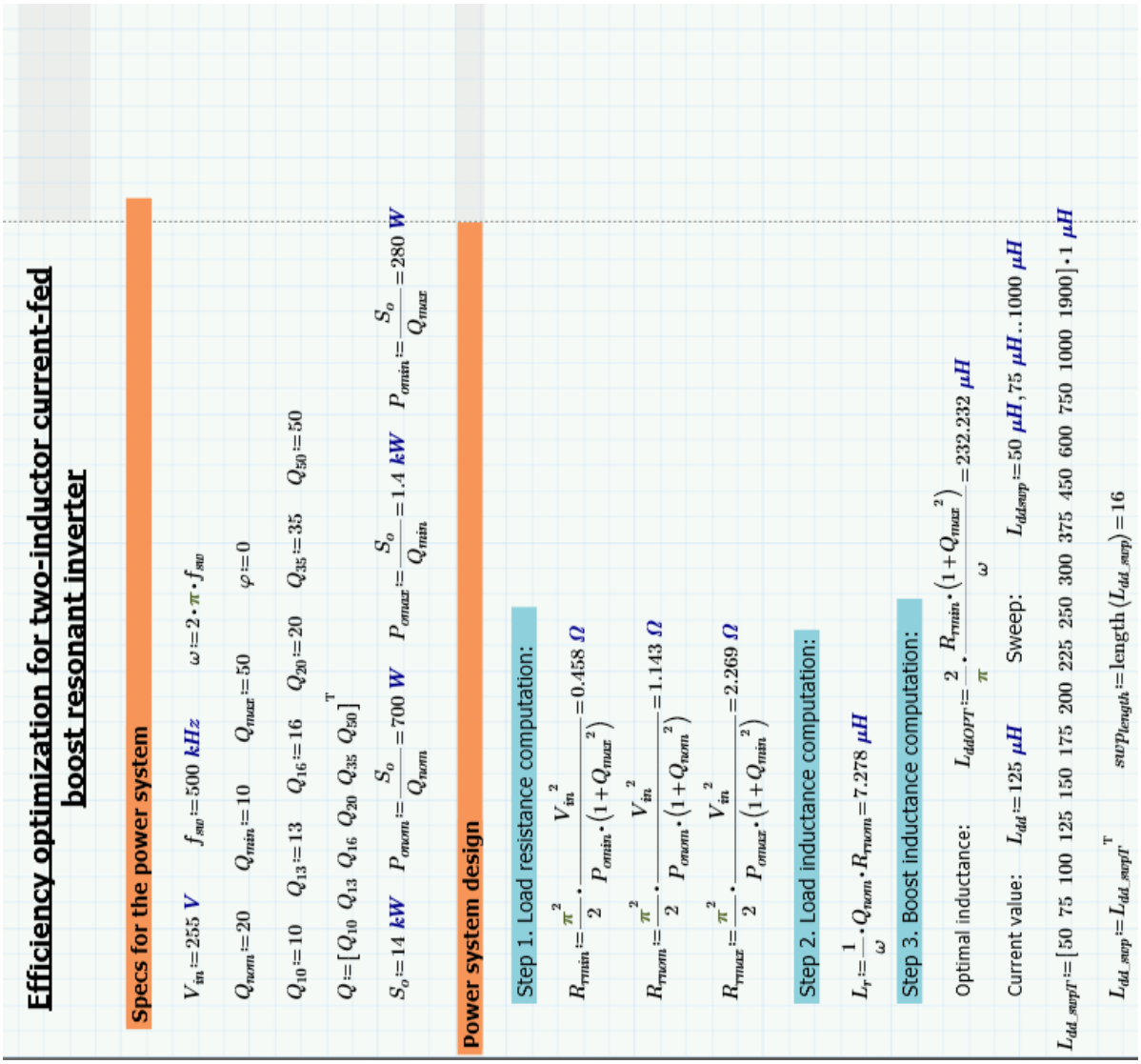


Figure C-1. Page 1.

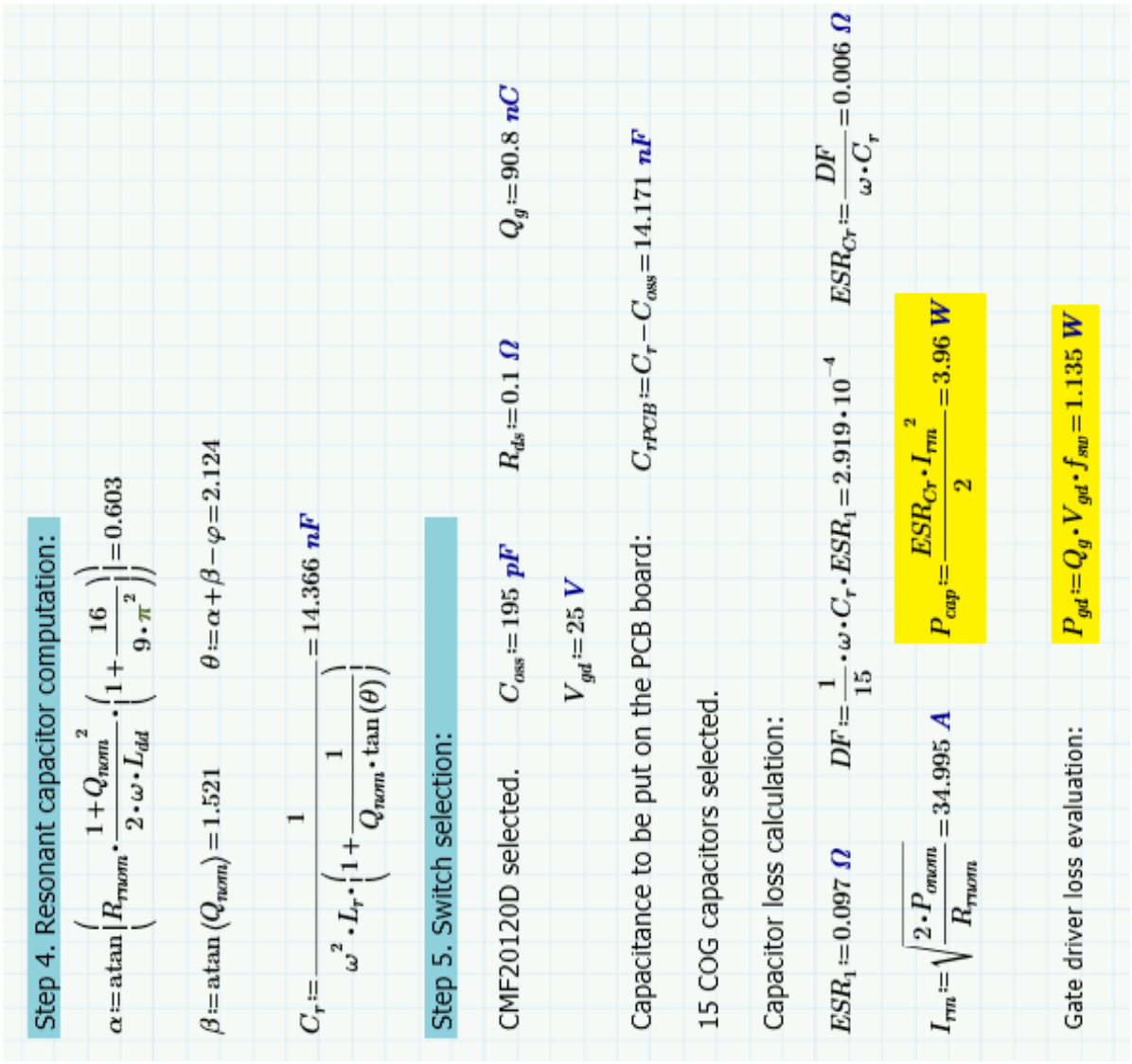


Figure C-2. Page 2.

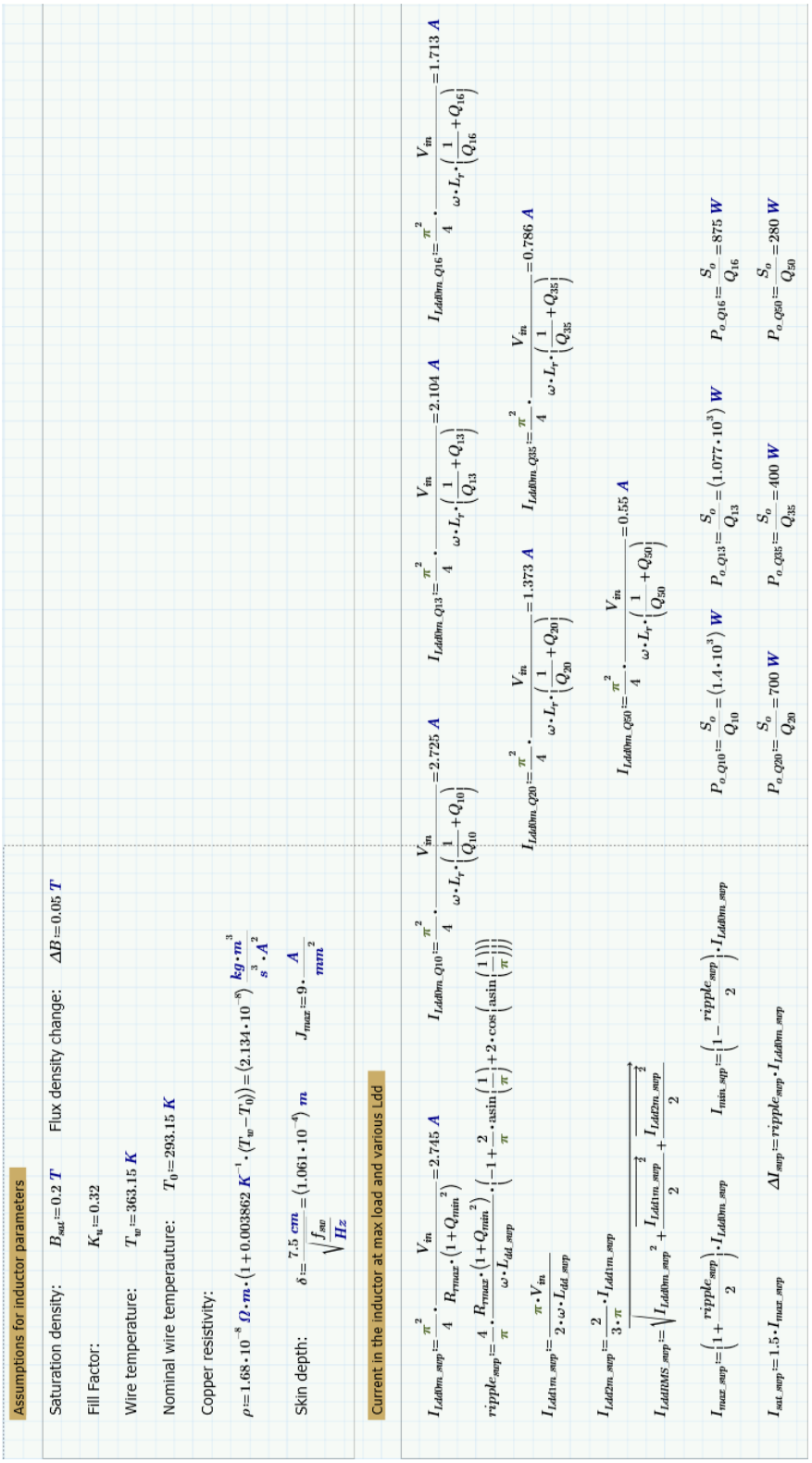


Figure C-3. Page 3.

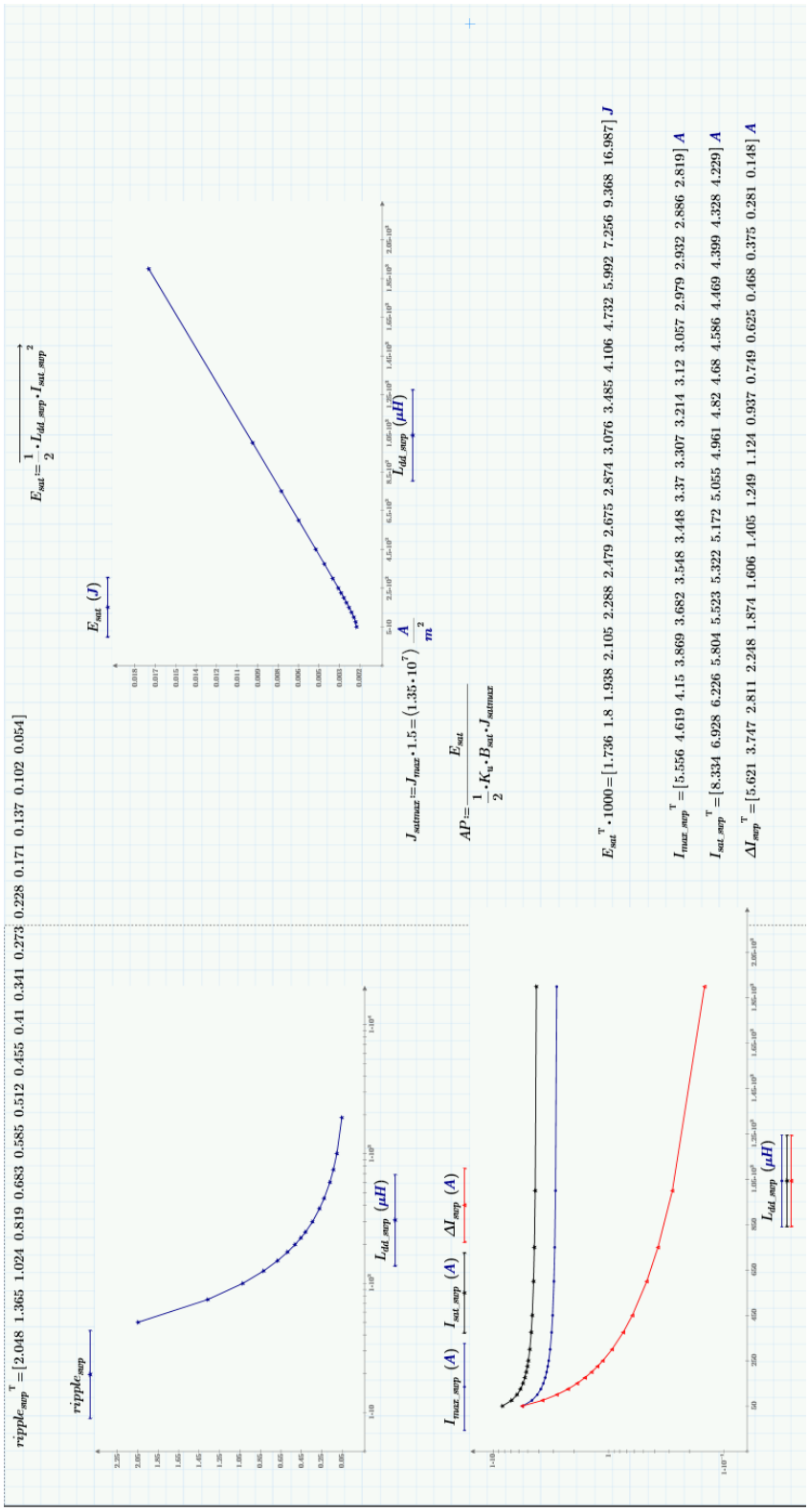


Figure C-4. Page 4.

Magnetic core size table

Core	A_c	W_a	$AcWa$	b	D	MLT	l_m	V_e
	(mm^2)	(mm^2)	(mm^4)	(mm)	(mm)	(mm)	(mm)	(mm^3)
"PQ2020"	62.9	35	2201.5	11.7	9	44	45.2	2843
"PQ2620"	112.3	33	4035.9	9	12	56	44.4	5435
"PQ2625"	122	47	5734	12.7	12.5	56	53.6	6530
"PQ3220"	154.2	47	7247.4	9.1	14	66	48.4	7460
"PQ3230"	153.8	104	15995.2	18.5	14	62	67.8	10440
"PQ3535"	169.7	158	26812.6	21.8	14.7	76	79.2	13440
"PQ4040"	188.3	309	58184.7	25.4	15.5	87	92.5	17430

b is bobbin height
D is core cross section diameter

$$\Delta B_{Bastpl^T} := [0.01 \;\; 0.0125 \;\; 0.015 \;\; 0.0175 \;\; 0.02 \;\; 0.0225 \;\; 0.025 \;\; 0.03 \;\; 0.035 \;\; 0.04 \;\; 0.045 \;\; 0.05 \;\; 0.055 \;\; 0.06 \;\; 0.065 \;\; 0.07 \;\; 0.075 \;\; 0.085 \;\; 0.1]\ T$$

$$\Delta B_{Bastp} := \Delta B_{Bastpl^T} \qquad sup_{\Delta B} := \text{length}(\Delta B_{Bastp}) = 19$$

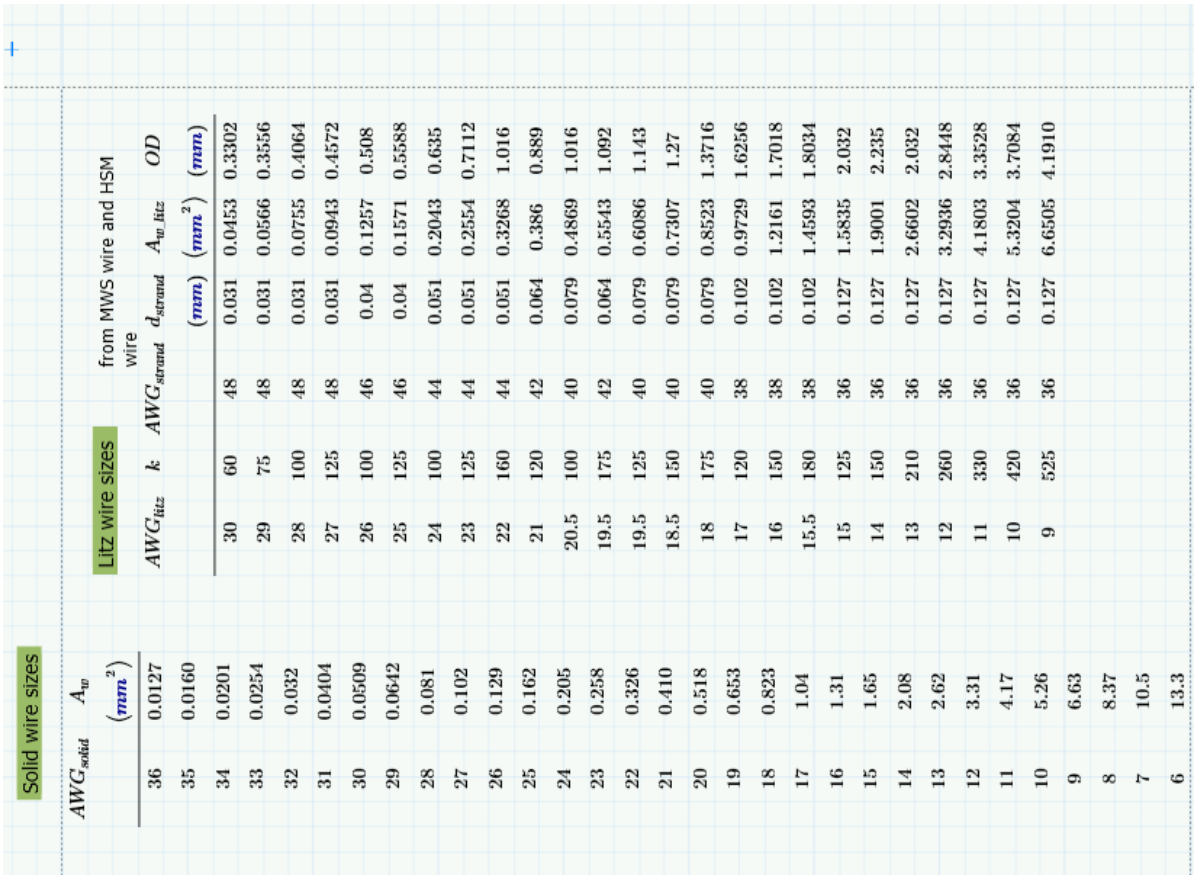
$$P_{vstrT} := [1.5 \;\; 2.2 \;\; 2.98 \;\; 4.54 \;\; 6 \;\; 8.4 \;\; 11.11 \;\; 17.81 \;\; 25.48 \;\; 34.92 \;\; 47.16 \;\; 63.88 \;\; 82.88 \;\; 112.96 \;\; 138.03 \;\; 168.66 \;\; 212.08 \;\; 312.17 \;\; 507.94]\ \frac{kW}{m^3}$$

$$P_{vstn} := P_{vstrT^T} \qquad \alpha_c := 1.3365 \qquad \beta_c := 2.6715$$

$$L_{dd\_sup^T} = [5 \cdot 10^{-5} \;\; 7.5 \cdot 10^{-5} \;\; 1 \cdot 10^{-4} \;\; 1.25 \cdot 10^{-4} \;\; 1.5 \cdot 10^{-4} \;\; 1.75 \cdot 10^{-4} \;\; 2 \cdot 10^{-4} \;\; 2.25 \cdot 10^{-4} \;\; 2.5 \cdot 10^{-4} \;\; 3 \cdot 10^{-4} \;\; 3.75 \cdot 10^{-4} \;\; 4.5 \cdot 10^{-4} \;\; 6 \cdot 10^{-4} \;\; 7.5 \cdot 10^{-4} \;\; 0.001 \;\; 0.002]\ H$$

$$AP^T = [4.019 \cdot 10^3 \;\; 4.167 \cdot 10^3 \;\; 4.486 \cdot 10^3 \;\; 4.874 \cdot 10^3 \;\; 5.296 \cdot 10^3 \;\; 5.737 \cdot 10^3 \;\; 6.191 \cdot 10^3 \;\; 6.653 \cdot 10^3 \;\; 7.121 \cdot 10^3 \;\; 8.068 \cdot 10^3 \;\; 9.505 \cdot 10^3 \;\; 1.095 \cdot 10^4 \;\; 1.387 \cdot 10^4 \;\; 1.68 \cdot 10^4 \;\; 2.168 \cdot 10^4 \;\; 3.932 \cdot 10^4]\ mm^4$$

Figure C-5. Page 5.



Solid wire sizes

AWG_{solid}	A_w (mm^2)
36	0.0127
35	0.0160
34	0.0201
33	0.0254
32	0.032
31	0.0404
30	0.0509
29	0.0642
28	0.081
27	0.102
26	0.129
25	0.162
24	0.205
23	0.258
22	0.326
21	0.410
20	0.518
19	0.653
18	0.823
17	1.04
16	1.31
15	1.65
14	2.08
13	2.62
12	3.31
11	4.17
10	5.26
9	6.63
8	8.37
7	10.5
6	13.3

Litz wire sizes

AWG_{litz}	k	AWG_{strand}	from MWS wire and HSM wire d_{strand} (mm)	A_{w_litz} (mm^2)	OD (mm)
30	60	48	0.031	0.0453	0.3302
29	75	48	0.031	0.0566	0.3556
28	100	48	0.031	0.0755	0.4064
27	125	48	0.031	0.0943	0.4572
26	100	46	0.04	0.1257	0.508
25	125	46	0.04	0.1571	0.5588
24	100	44	0.051	0.2043	0.635
23	125	44	0.051	0.2554	0.7112
22	160	44	0.051	0.3268	1.016
21	120	42	0.064	0.386	0.889
20.5	100	40	0.079	0.4869	1.016
19.5	175	42	0.064	0.5543	1.092
19.5	125	40	0.079	0.6086	1.143
18.5	150	40	0.079	0.7307	1.27
18	175	40	0.079	0.8523	1.3716
17	120	38	0.102	0.9729	1.6256
16	150	38	0.102	1.2161	1.7018
15.5	180	38	0.102	1.4593	1.8034
15	125	36	0.127	1.5835	2.032
14	150	36	0.127	1.9001	2.235
13	210	36	0.127	2.6602	2.032
12	260	36	0.127	3.2936	2.8448
11	330	36	0.127	4.1803	3.3528
10	420	36	0.127	5.3204	3.7084
9	525	36	0.127	6.6505	4.1910

Figure C-6. Page 6.

Figure C-7. Page 7.

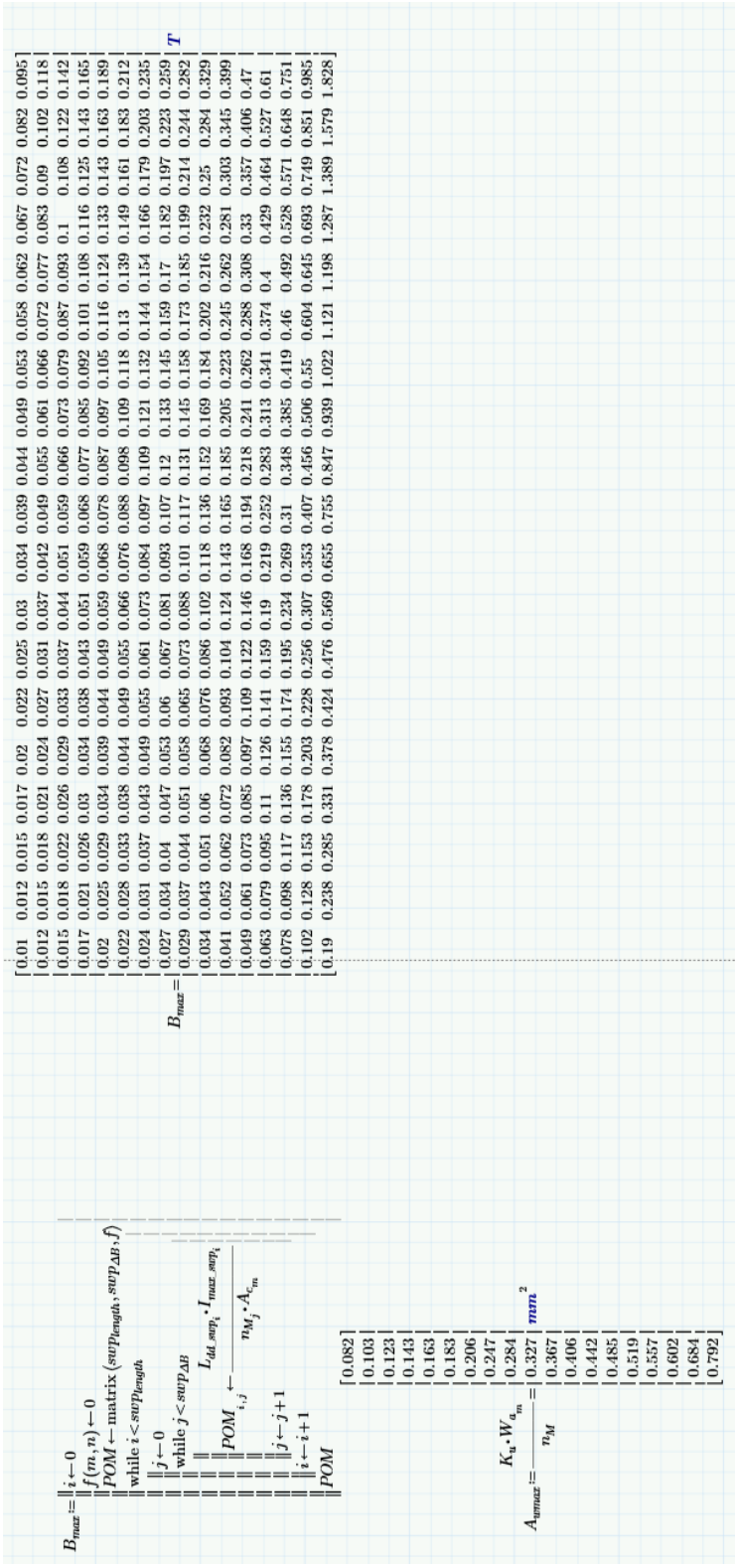


Figure C-8. Page 8.

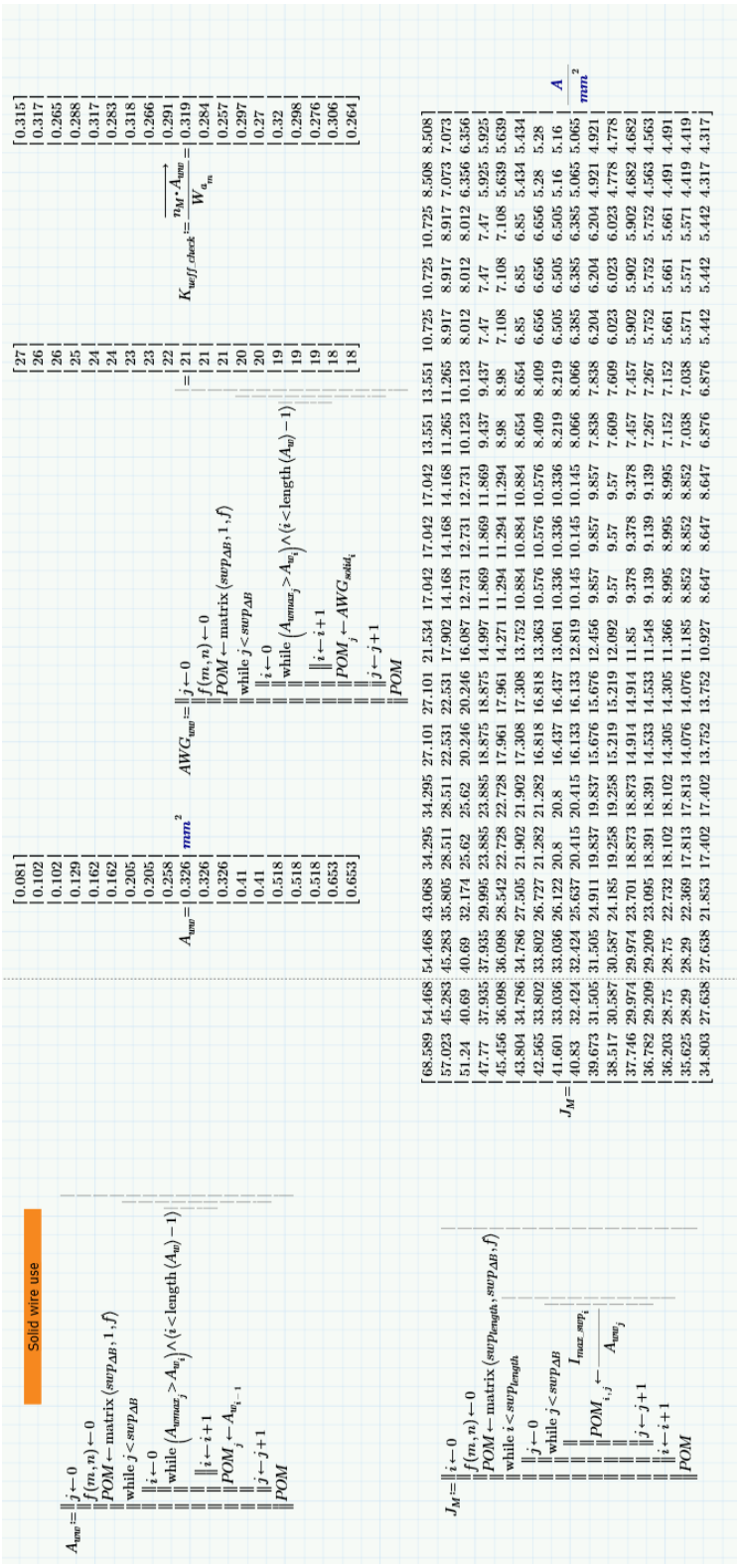


Figure C-9. Page 9.

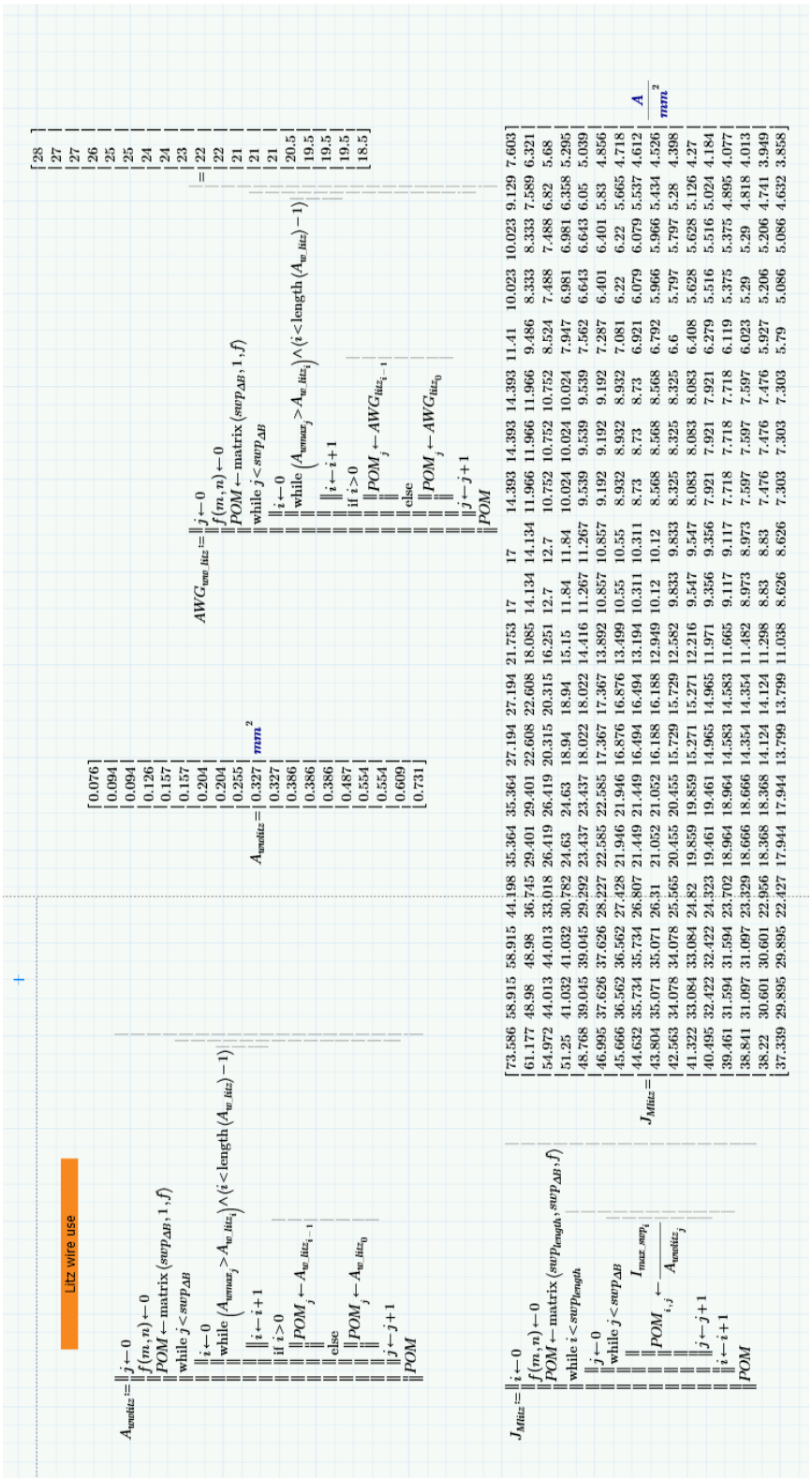


Figure C-10. Page 10.

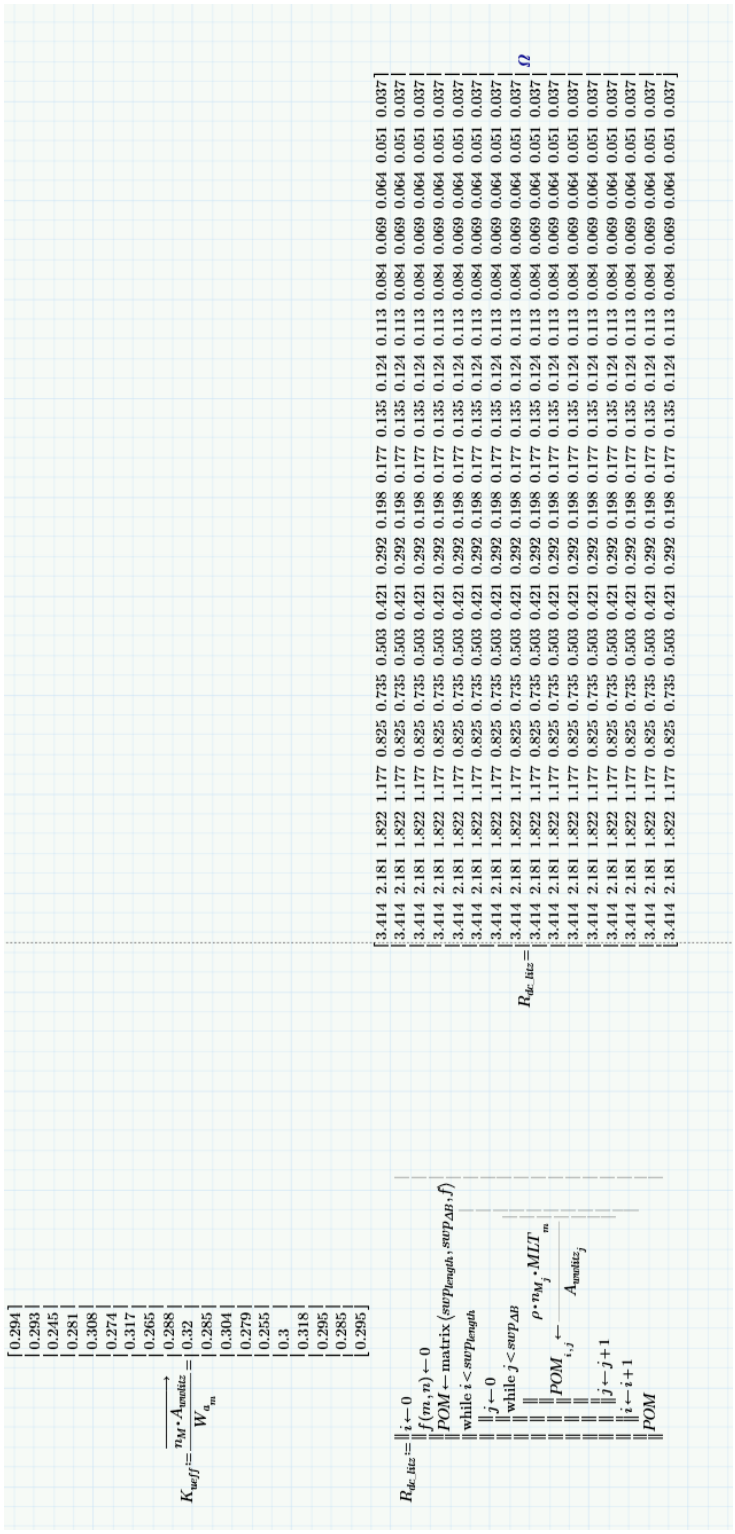


Figure C-11. Page 11.

Figure C-12. Page 12.

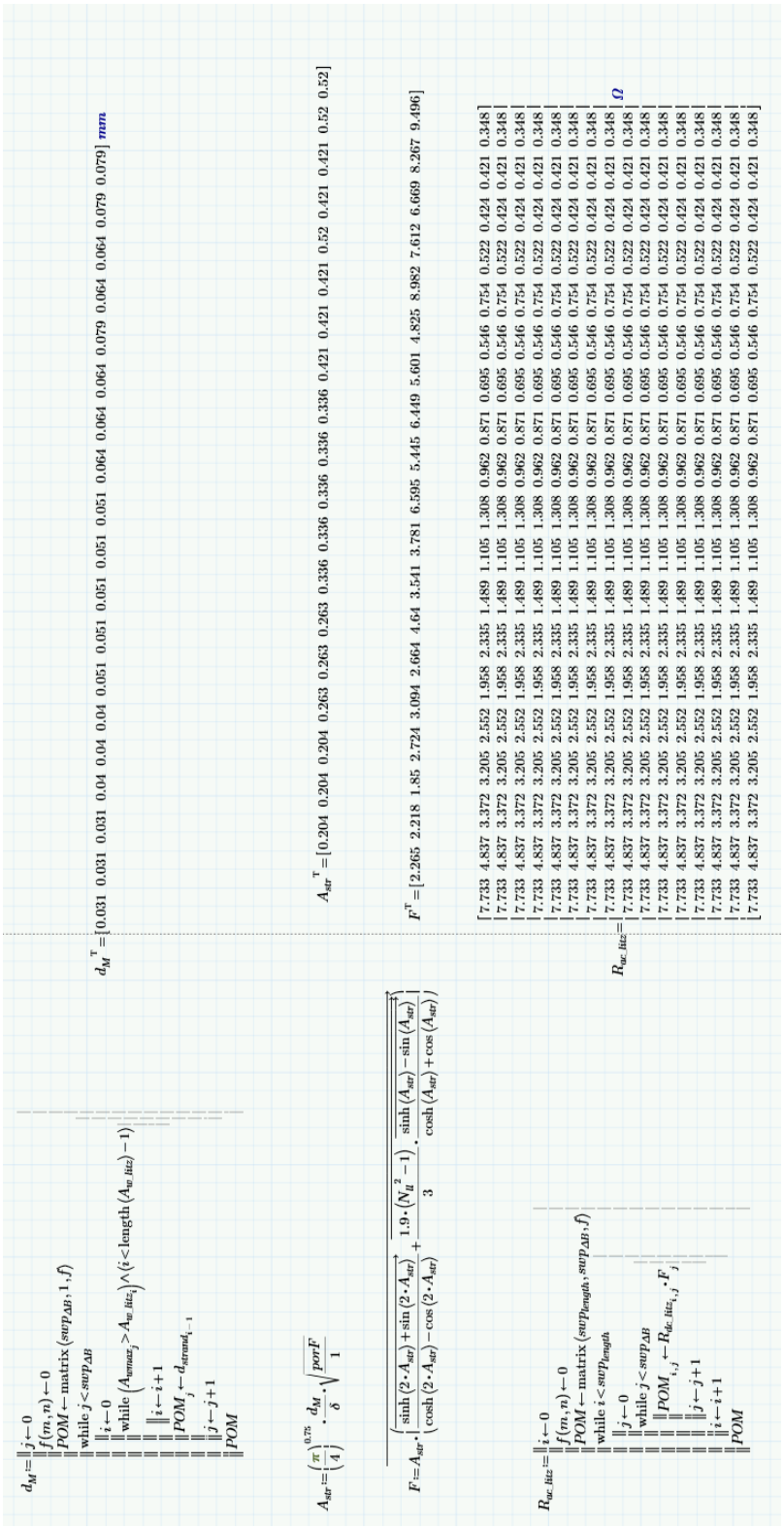


Figure C-13. Page 13.

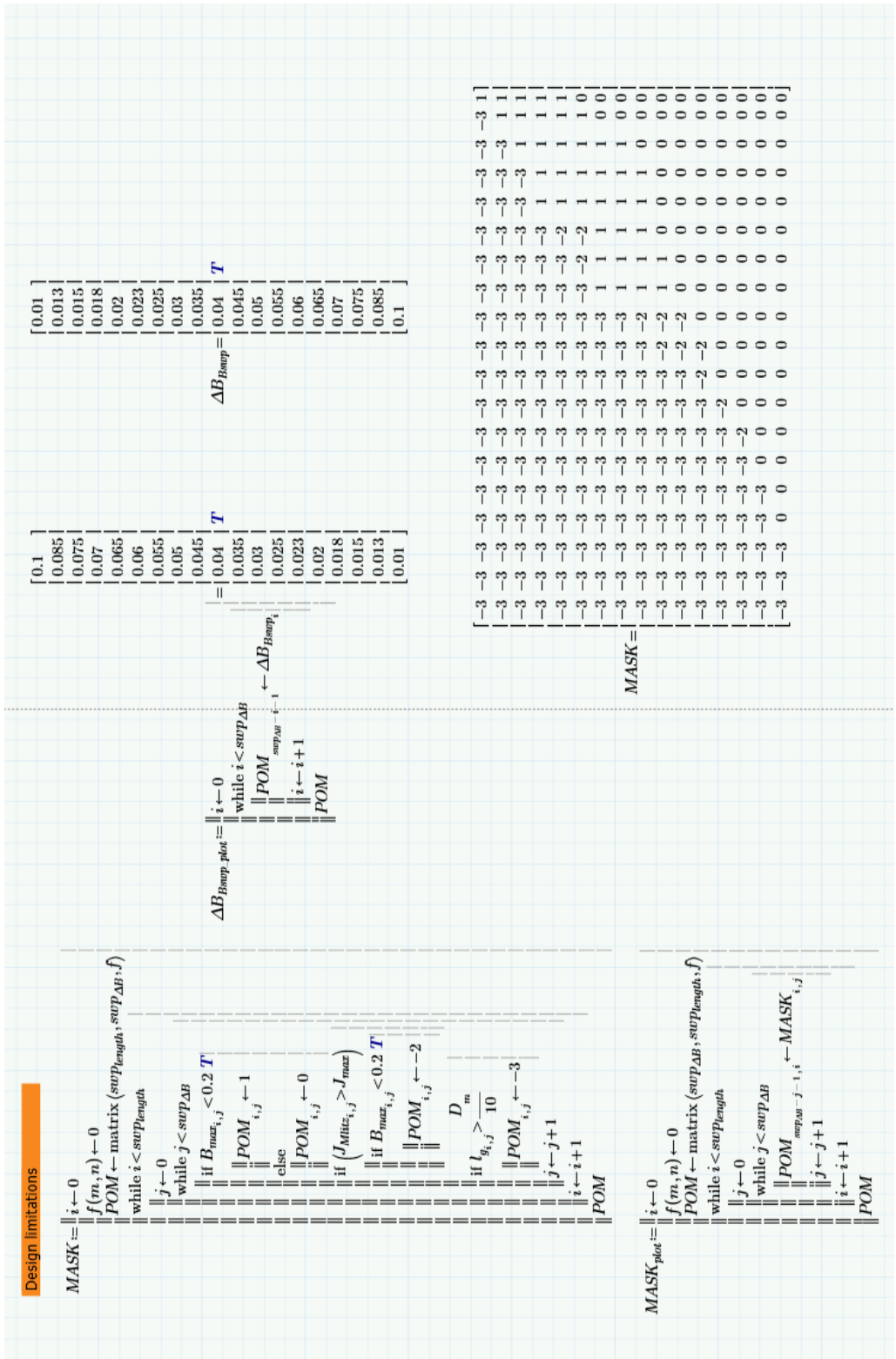


Figure C-14. Page 14.

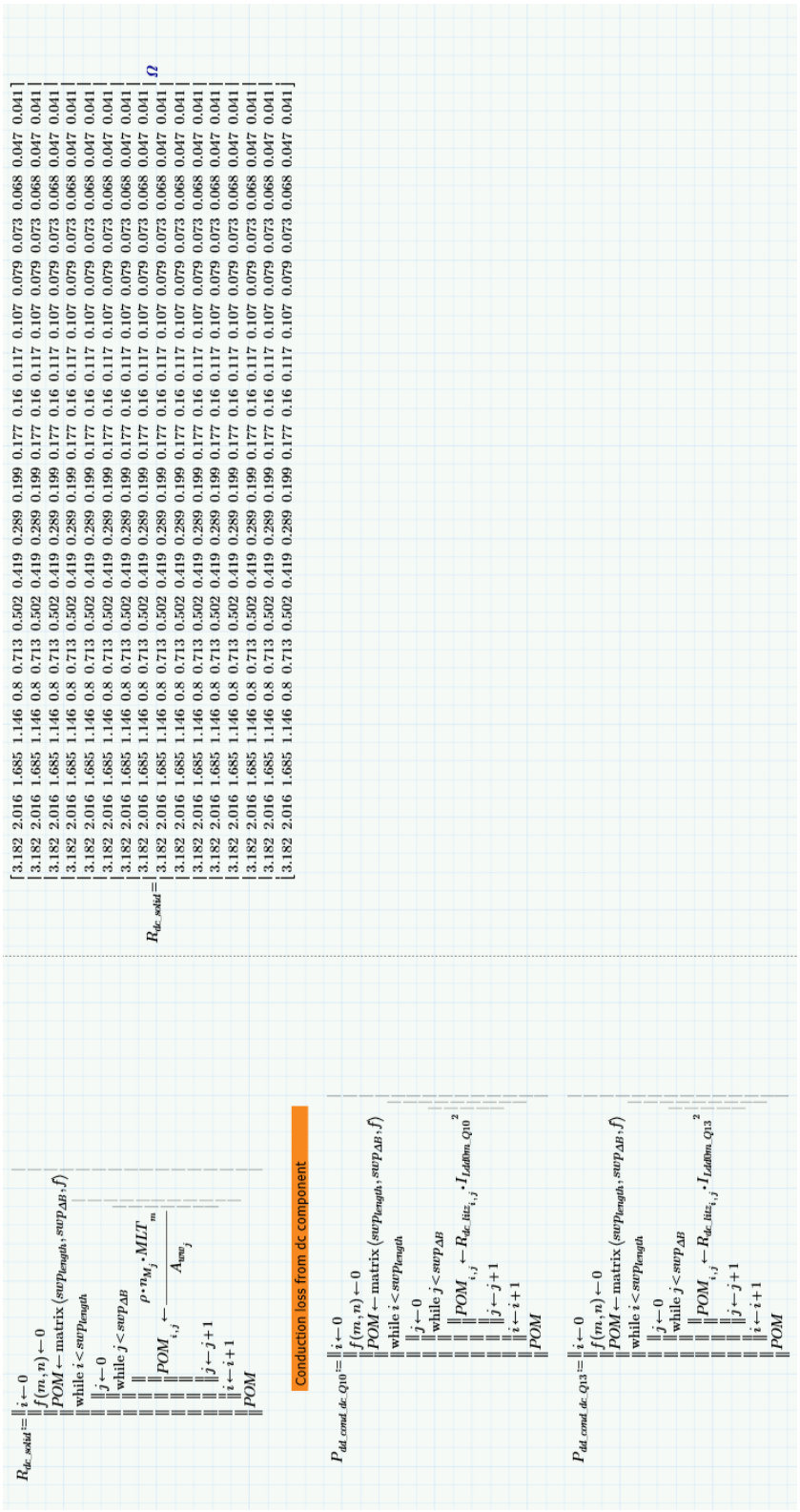


Figure C-15. Page 15.

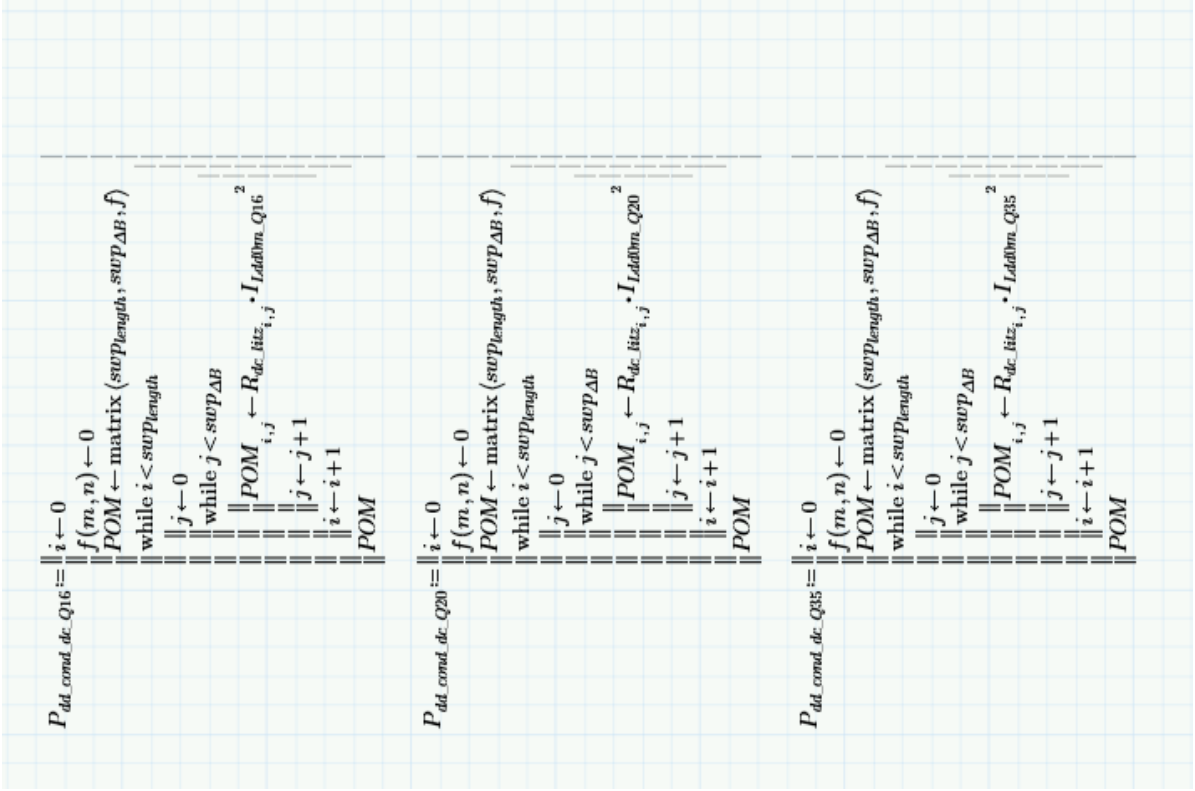


Figure C-16. Page 16.

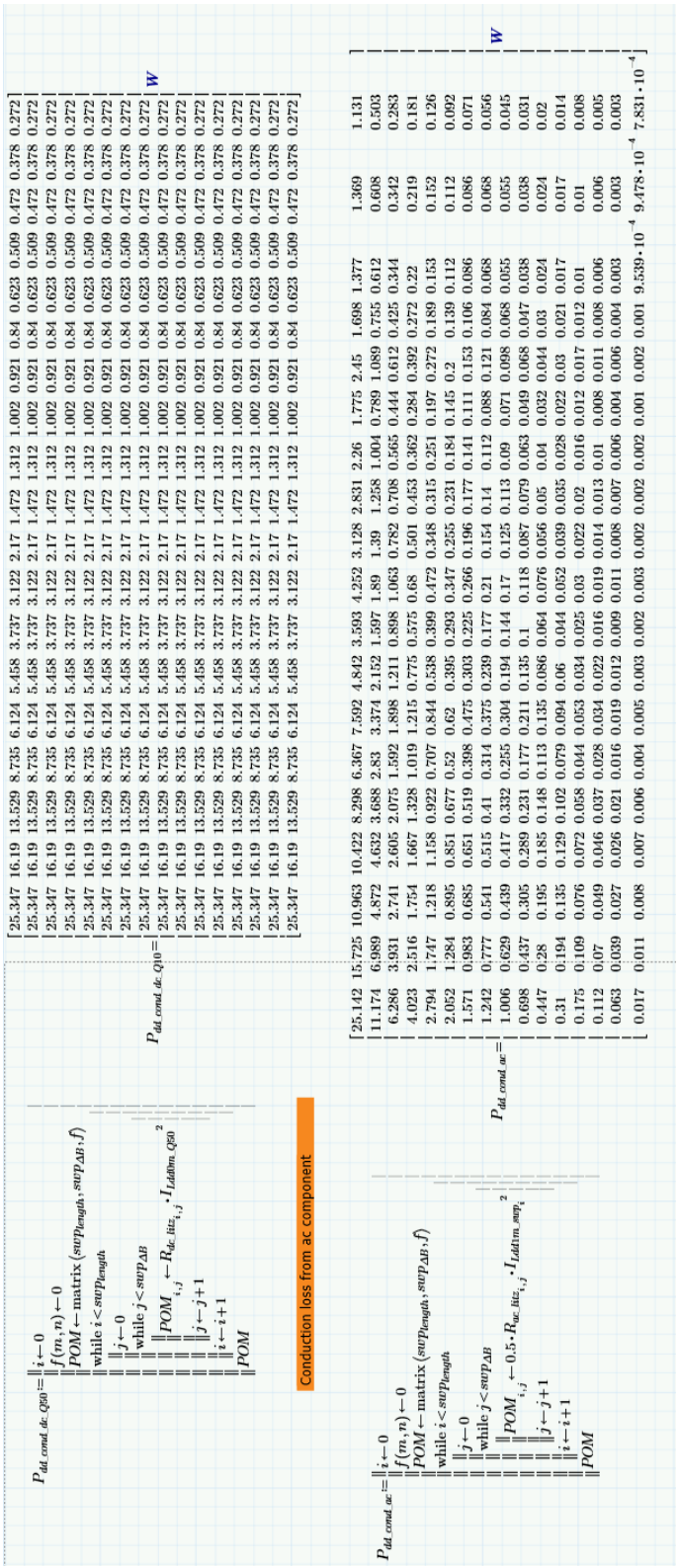


Figure C-17. Page 17.

$$P_{dd\_cond\_Q10} := P_{dd\_cond\_dc\_Q10} + P_{dd\_cond\_ac}$$

$$P_{dd\_cond\_Q13} := P_{dd\_cond\_dc\_Q13} + P_{dd\_cond\_ac}$$

$$P_{dd\_cond\_Q16} := P_{dd\_cond\_dc\_Q16} + P_{dd\_cond\_ac}$$

$$P_{dd\_cond\_Q20} := P_{dd\_cond\_dc\_Q20} + P_{dd\_cond\_ac}$$

$$P_{dd\_cond\_Q35} := P_{dd\_cond\_dc\_Q35} + P_{dd\_cond\_ac}$$

$$P_{dd\_cond\_Q50} := P_{dd\_cond\_dc\_Q50} + P_{dd\_cond\_ac}$$

$$P_{dd\_core} := V_{c_m} \cdot P_{vsin}$$

$$P_{dd\_cond\_Q10} = \begin{bmatrix} 50.489 & 31.916 & 24.492 & 19.157 & 14.422 & 11.825 & 11.329 & 7.965 & 5.764 & 5.723 & 4.44 & 3.834 & 3.181 & 2.614 & 3.073 & 2.207 & 1.849 & 1.747 & 1.403 \\ 36.521 & 23.179 & 18.401 & 13.367 & 9.812 & 8.288 & 7.111 & 5.274 & 3.767 & 3.361 & 2.702 & 2.261 & 1.925 & 1.629 & 1.712 & 1.264 & 1.084 & 0.986 & 0.774 \\ 31.632 & 20.122 & 16.27 & 11.341 & 8.198 & 7.05 & 5.635 & 4.333 & 3.068 & 2.535 & 2.094 & 1.71 & 1.486 & 1.283 & 1.235 & 0.934 & 0.816 & 0.72 & 0.555 \\ 29.369 & 18.706 & 15.283 & 10.403 & 7.452 & 6.477 & 4.951 & 3.897 & 2.745 & 2.152 & 1.813 & 1.455 & 1.283 & 1.124 & 1.015 & 0.781 & 0.692 & 0.597 & 0.453 \\ 28.14 & 17.938 & 14.747 & 9.893 & 7.046 & 6.166 & 4.58 & 3.66 & 2.569 & 1.944 & 1.66 & 1.317 & 1.172 & 1.037 & 0.895 & 0.698 & 0.625 & 0.53 & 0.398 \\ 27.399 & 17.474 & 14.424 & 9.586 & 6.801 & 5.978 & 4.356 & 3.518 & 2.463 & 1.819 & 1.567 & 1.233 & 1.106 & 0.985 & 0.823 & 0.648 & 0.584 & 0.49 & 0.364 \\ 26.918 & 17.173 & 14.214 & 9.386 & 6.643 & 5.856 & 4.211 & 3.425 & 2.395 & 1.738 & 1.507 & 1.179 & 1.062 & 0.951 & 0.776 & 0.616 & 0.558 & 0.464 & 0.343 \\ 26.588 & 16.967 & 14.07 & 9.25 & 6.534 & 5.773 & 4.111 & 3.361 & 2.348 & 1.682 & 1.466 & 1.142 & 1.033 & 0.927 & 0.744 & 0.593 & 0.54 & 0.446 & 0.328 \\ 26.352 & 16.819 & 13.967 & 9.152 & 6.456 & 5.713 & 4.04 & 3.316 & 2.314 & 1.642 & 1.437 & 1.116 & 1.011 & 0.911 & 0.721 & 0.577 & 0.527 & 0.433 & 0.317 \\ 26.045 & 16.627 & 13.833 & 9.025 & 6.354 & 5.635 & 3.947 & 3.257 & 2.27 & 1.59 & 1.399 & 1.081 & 0.984 & 0.889 & 0.691 & 0.557 & 0.51 & 0.416 & 0.303 \\ 25.794 & 16.47 & 13.724 & 8.92 & 6.271 & 5.571 & 3.872 & 3.208 & 2.234 & 1.548 & 1.368 & 1.053 & 0.961 & 0.871 & 0.666 & 0.54 & 0.496 & 0.402 & 0.292 \\ 25.657 & 16.384 & 13.664 & 8.864 & 6.226 & 5.537 & 3.83 & 3.182 & 2.214 & 1.524 & 1.351 & 1.037 & 0.949 & 0.862 & 0.653 & 0.53 & 0.489 & 0.395 & 0.286 \\ 25.521 & 16.3 & 13.605 & 8.807 & 6.182 & 5.502 & 3.789 & 3.156 & 2.195 & 1.501 & 1.334 & 1.022 & 0.937 & 0.852 & 0.64 & 0.521 & 0.481 & 0.388 & 0.28 \\ 25.458 & 16.26 & 13.578 & 8.781 & 6.161 & 5.487 & 3.77 & 3.144 & 2.186 & 1.491 & 1.326 & 1.015 & 0.931 & 0.848 & 0.634 & 0.517 & 0.478 & 0.384 & 0.277 \\ 25.409 & 16.23 & 13.556 & 8.761 & 6.145 & 5.474 & 3.756 & 3.134 & 2.179 & 1.483 & 1.32 & 1.009 & 0.927 & 0.844 & 0.629 & 0.514 & 0.475 & 0.381 & 0.275 \\ 25.364 & 16.201 & 13.537 & 8.742 & 6.13 & 5.463 & 3.742 & 3.126 & 2.173 & 1.475 & 1.314 & 1.004 & 0.923 & 0.841 & 0.625 & 0.511 & 0.473 & 0.379 & 0.273 \end{bmatrix} W$$

$$P_{dd\_core}{}^{T} = [0.011 \quad 0.016 \quad 0.022 \quad 0.034 \quad 0.045 \quad 0.063 \quad 0.083 \quad 0.133 \quad 0.19 \quad 0.261 \quad 0.352 \quad 0.477 \quad 0.618 \quad 0.843 \quad 1.03 \quad 1.258 \quad 1.582 \quad 2.329 \quad 3.789] \; W$$

Figure C-18. Page 18.

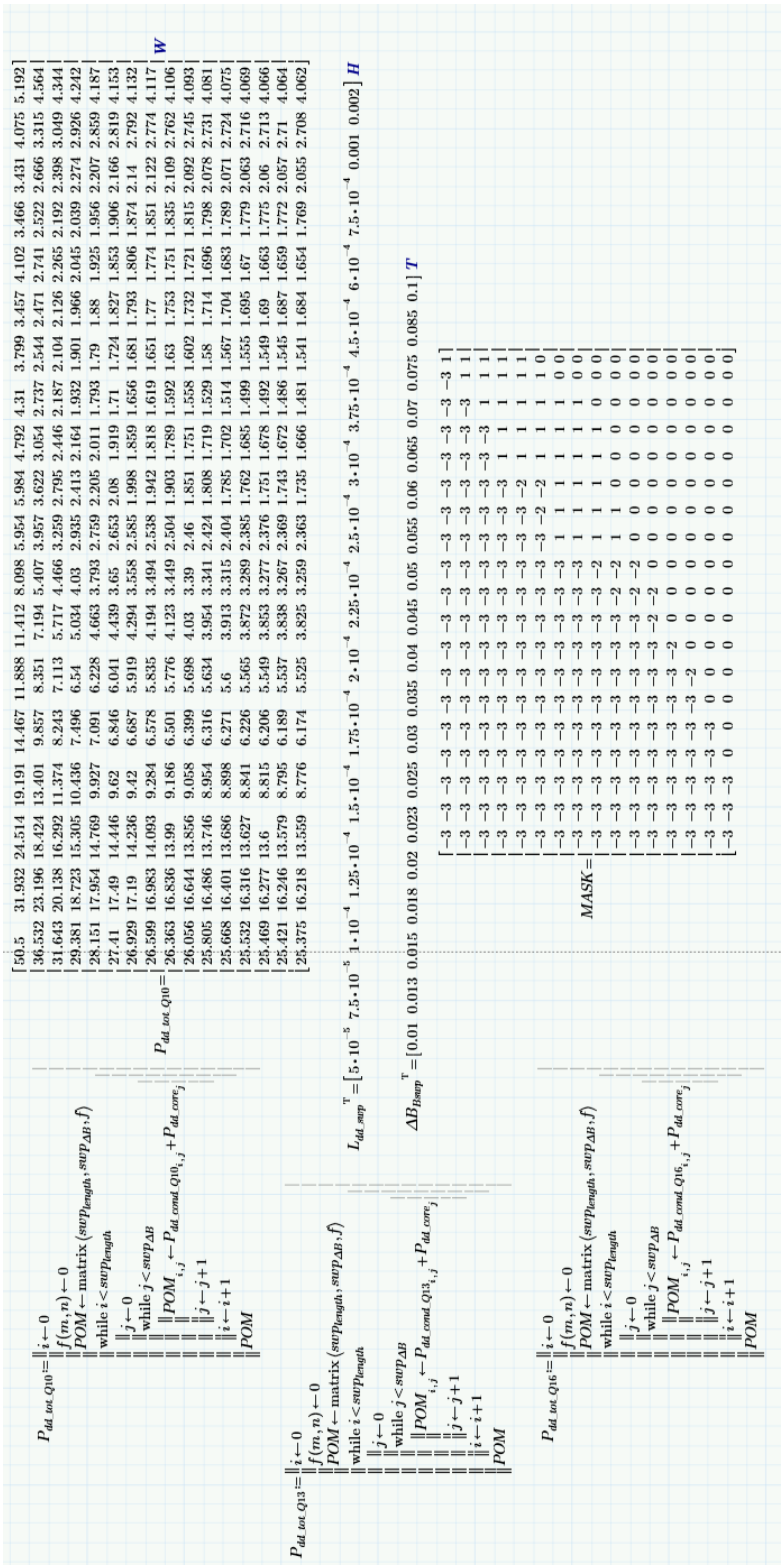


Figure C-19. Page 19.

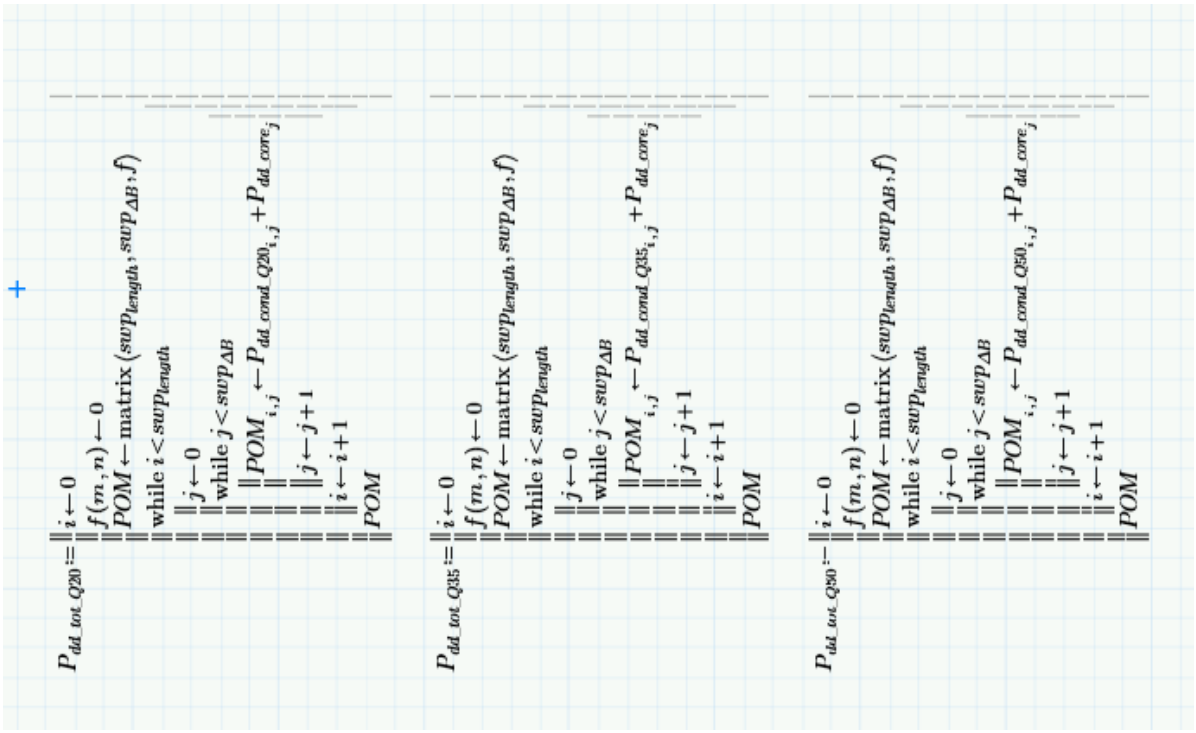


Figure C-20. Page 20.

Figure C-21. Page 21.

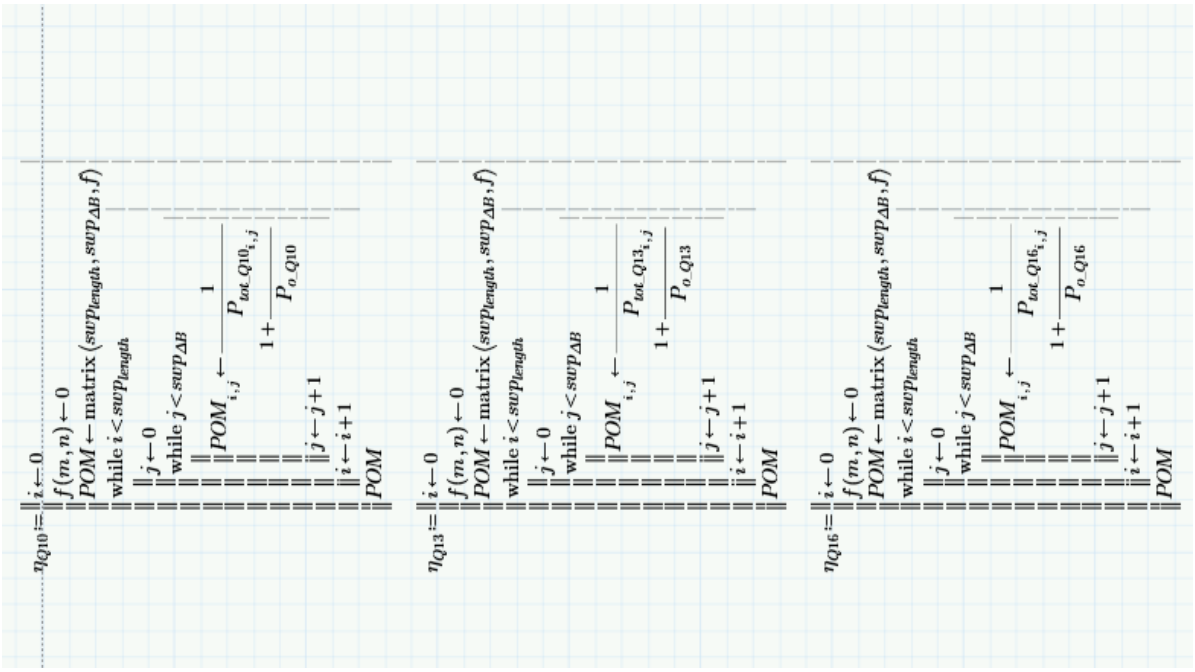


Figure C-22. Page 22.

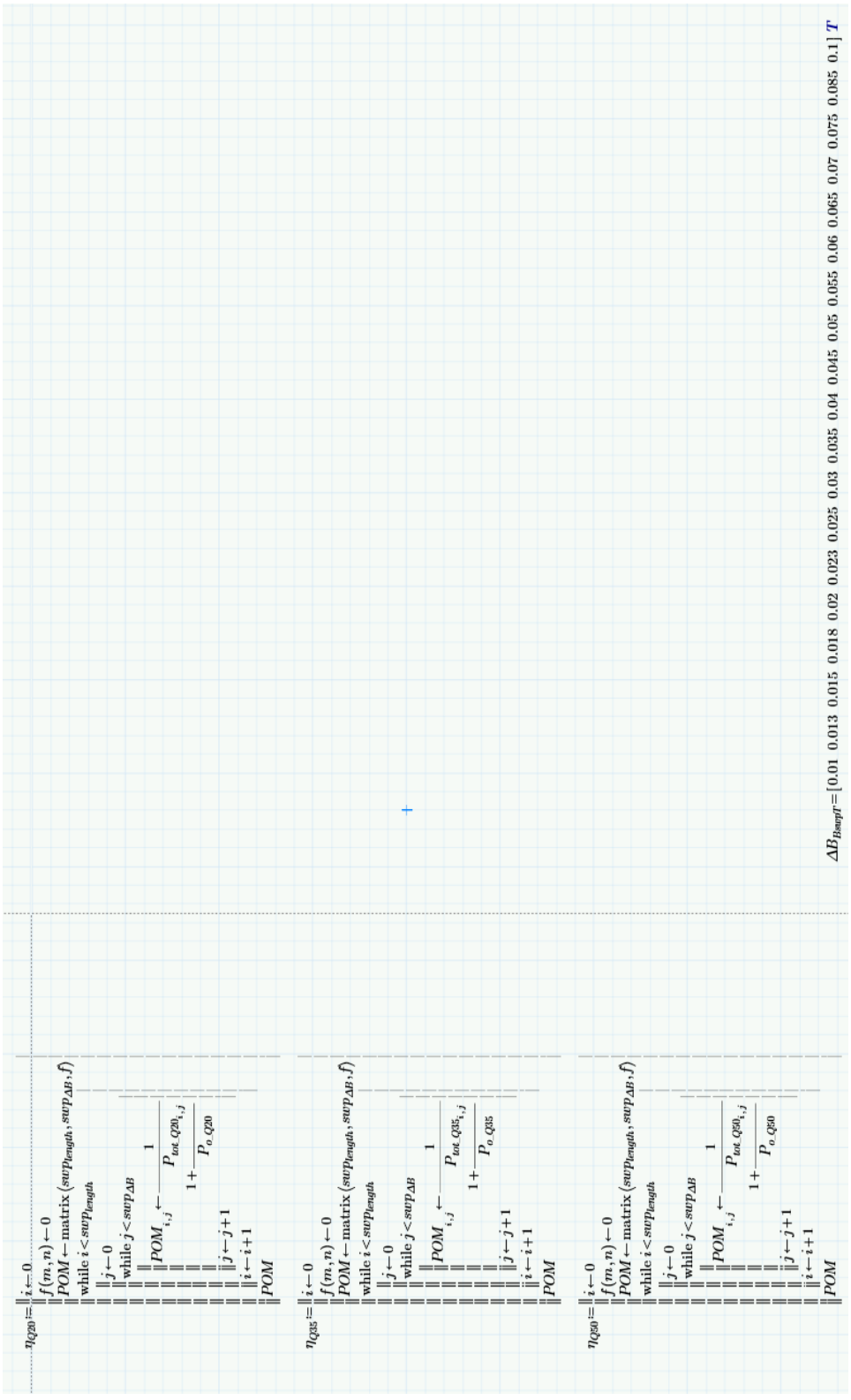


Figure C-23. Page 23.

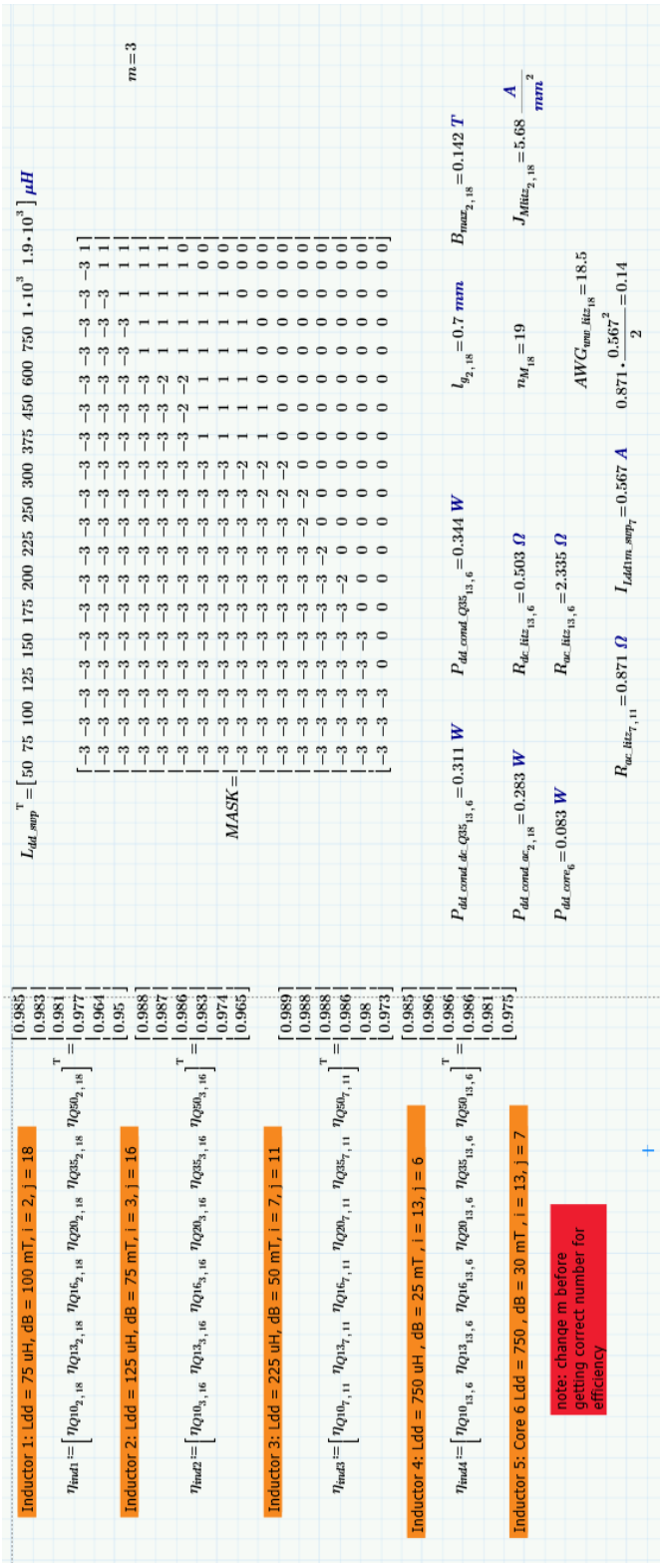


Figure C-24. Page 24.

Appendix D. Derivation of the Low-frequency model

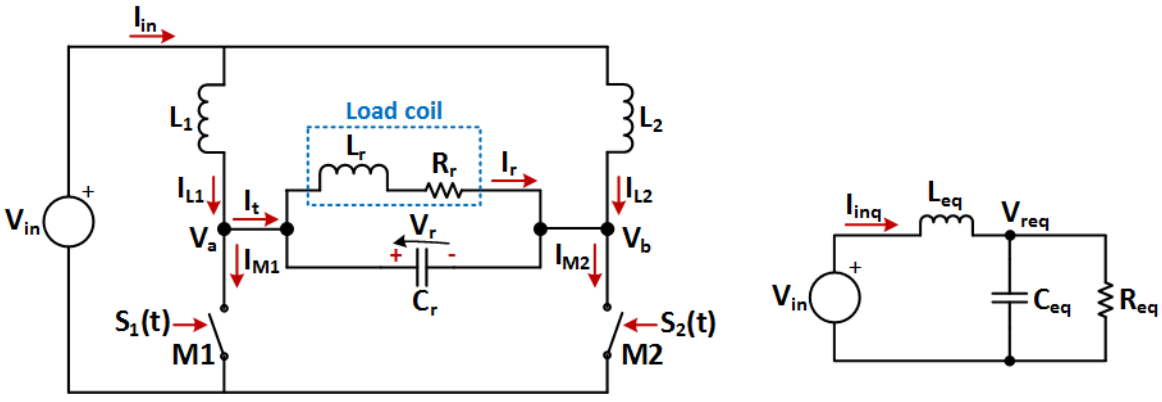
D.1. Model Derivation

The boost amplifier is shown in Figure D-1 a). An equivalent model that is able to predict transient behavior at low frequencies (low frequency oscillations or envelopes) is introduced in [1], and it is shown in Figure D-1 b). In this Appendix, the derivation of the model will be shown, and its applicability to the boost amplifier with reduced input inductance (50 μH ≤ L_{in}) and high loaded quality-factor (10 < Q <50). The model is termed Low-frequency model, and it is derived from the energy and power equations for the boost amplifier and the model itself. The energy conservation principle is applied, and thus the two models have:

- Equal input voltage and current.
- Equal power dissipation.
- Inductors and capacitors store equal energy.

Low-frequency model is valid only if boost amplifier is operated at (angular) synchronous frequency defined with

$$\omega_{sy} = \sqrt{\frac{1}{L_q C_r} - \left(\frac{R_r}{L_r}\right)^2} \tag{D-1}$$



(a) (b)

Figure D-1. (a) Boost amplifier with ideal switches. Input inductances L_1 and L_2 have equal value $L_1 = L_2 = L_{in}$. (b) Low-frequency equivalent model of the boost amplifier. Equivalent model replicates transient performance of the boost amplifier.

where

$$L_q = L_r \parallel L_{in-eq} \tag{D-2}$$

and

$$L_{in-eq} = \frac{2L_{in}}{1+\frac{16}{9\pi^2}} \tag{D-3}$$

First, the equivalent input inductor L_{eq} of the Low-frequency model is derived. If input inductors of the boost amplifier have equal value ($L_1 = L_2 = L_{in}$), than the input current of the boost amplifier splits into two, so currents in L_1 and L_2 are equal as well. Total energy of inductors L_1 and L_2 can be written as

$$E_{Lin} = 2 \cdot \left(\frac{1}{2} L_{in} \left(\frac{I_{in}}{2} \right)^2 \right) = \frac{L_{in} I_{in}^2}{4} \tag{D-4}$$

where I_{in} is the input current of the boost amplifier. For the Low-frequency model, the same input current should flow to the circuit, so:

$$I_{in} = I_{inq} \tag{D-5}$$

The energy of the input inductor L_{eq} of Low-frequency model is

$$E_{Leq} = \frac{1}{2} L_{eq} I_{in}^2 \tag{D-6}$$

Thanks to energy conservation principle, the equations (D-4) and (D-6) are equal. The input inductance of the Low-frequency model is then computed as:

$$L_{eq} = \frac{L_{in}}{2} \tag{D-7}$$

Next, equivalent capacitor C_{eq} of Low-frequency model is derived. The maximum energy of the resonant capacitor C_r is equal to

$$E_{Cr} = \frac{1}{2} C_r V_{rm}^2 = \frac{\pi^2}{2} C_r V_{in}^2 \tag{D-8}$$

where V_{rm} is the amplitude of the oscillations of V_r voltage, and at synchronous frequency the relationship

$$V_{rm} = \pi V_{in} \tag{D-9}$$

is valid. The low-frequency behavior of the boost amplifier originates from interaction between the input inductors (L_1 and L_2) and resonant capacitor C_r. In the Low-frequency model, this interaction is represented by equivalent input inductor L_{eq} and equivalent capacitor C_{eq}. Thus, the energy of C_{eq} capacitor equivalents the maximum energy of C_r capacitor, producing:

$$E_{Ceq} = E_{Cr} = \frac{1}{2} C_{eq} V_{in}^2 \tag{D-10}$$

The equivalent capacitor C_{eq} is then computed as:

$$C_{eq} = \pi^2 C_r \tag{D-11}$$

It should be kept in mind that the amplitude of the resonant voltage V_r and the output voltage of Low-frequency model are connected as:

$$V_{rm} = \pi V_{req} \tag{D-12}$$

Finally, the equivalent resistance R_{eq} of Low-frequency model is derived. Circuits in Figure D-1 a) and Figure D-2 b) transfer the same amount of power to the load. The power given to the load for circuit in Figure D-1 a) is equal to:

$$PA = \frac{(\pi V_{in})^2}{2R_t} \tag{D-13}$$

where R_t is the resistance of the resonant tank described with

$$R_t = R_r \left(1 + Q^2\right) \tag{D-14}$$

and Q is the quality-factor of the load given with

$$Q = \frac{\omega L_r}{R_r} \tag{D-15}$$

At synchronous frequency the Q-factor equates to

$$Q = \frac{1}{R_r}\sqrt{\frac{L_r^2}{L_q C_r} - R_r^2} \tag{D-16}$$

The power dissipation of the equivalent resistor R_{eq} in the Low-frequency model is:

$$P_{inq} = \frac{V_{in}^2}{R_{eq}} \tag{D-17}$$

From PA = P_{inq}, the resistor R_{eq} is:

$$R_{eq} = \frac{2}{\pi^2} R_t = \frac{2}{\pi^2}\frac{L_r}{C_r}\frac{1}{R_r}\left(1 + \frac{L_r}{L_{in}}\frac{16+9\pi^2}{18\pi^2}\right) \tag{D-18}$$

D.2. Model Validation using Switching Simulation

Low-frequency model is valid at the synchronous frequency only. In this section, the model is validated using switching simulation model in LT-spice for the range of input inductance and Q-factor values of interest (50 μH ≤ L_{in} ≤ 4000 μH and 10 ≤ Q ≤ 50). The switching frequency is kept to f_{sw} = 500 kHz for simplicity, and the resonant capacitor is computed for each simulation as:

$$C_r = \frac{1}{\omega^2 L_r}\frac{1}{1+\frac{1}{Q^2}} + \frac{1}{\omega^2 L_{in-eq}} \tag{D-19}$$

The amplitude of the resonant voltage is set to V_{rm} = 800 V, and reactive energy of the tank is PQ = 14 kVA. The parameters of the simulation are summarized in Table D-1. Figures D-1, D-2, and D-3 show the simulations and comparison between the Low-frequency model and the switching model for the first 100 μs of the start-up transient. It is seen that for the ranges of interest for input inductance and the quality-factor the two models match very well, and the Low-frequency model predicts well the envelopes of the signals in the switching model.

Table D-1. Summary on simulation parameters for validation of Low-frequency model.

f_{sw} (kHz)	500	PQ (kVA)	14
V_{rm} (V)	800	Q	10-50
V_{in} (V)	254.65	L_{in} (μH)	50-4000
L_r (μH)	7.27	C_r (nF)	Calculated from (D-19) for synchronous operation

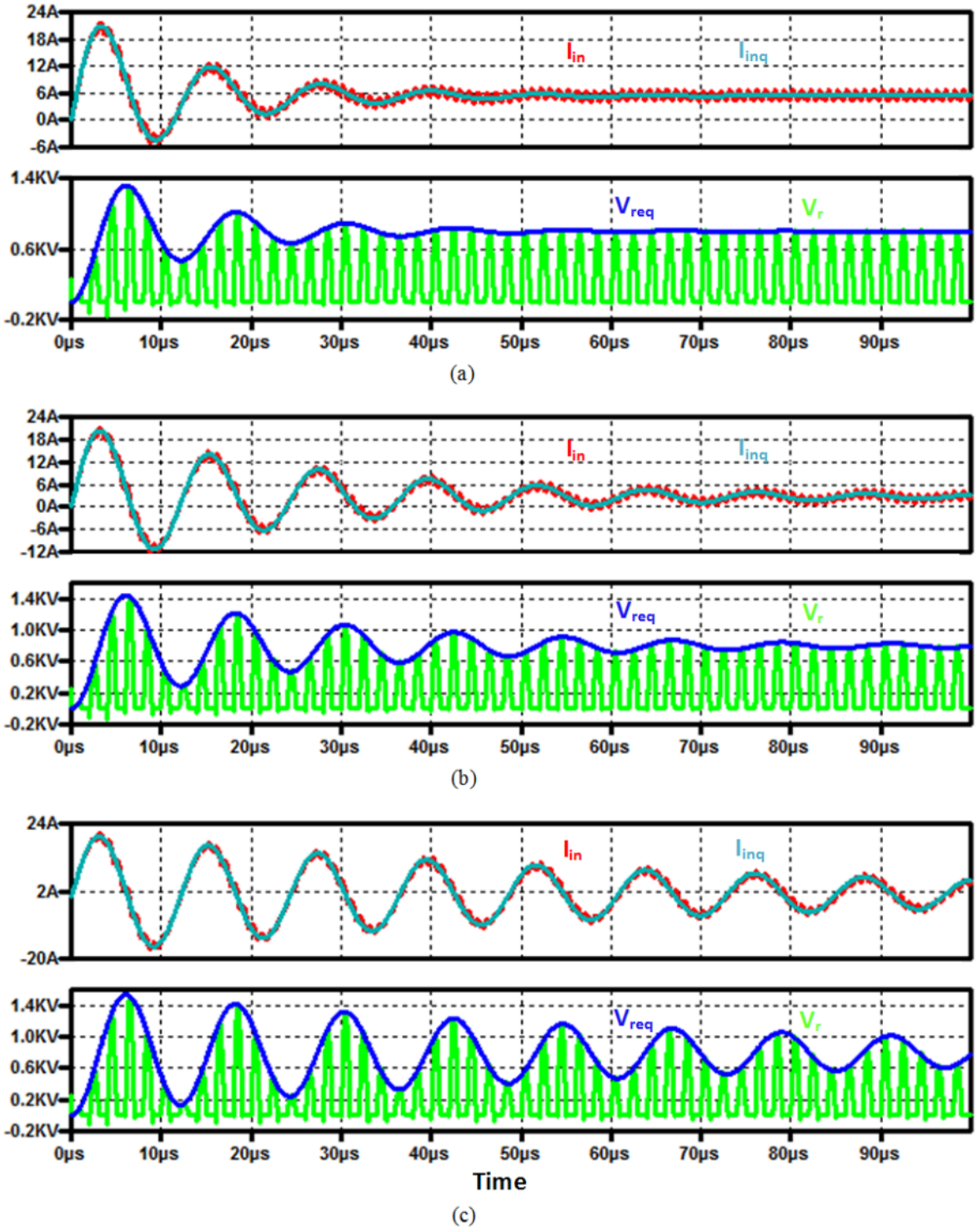


Figure D-2. Comparison between switching simulation model and Low-frequency model of the boost amplifier for the circuit variables given in Figure D-1 and simulation parameters given in Table D-1. The input inductance is L_{in} = 50 µH, and the loaded quality-factor is (a) Q = 10; (b) Q = 20; (c) Q = 50.

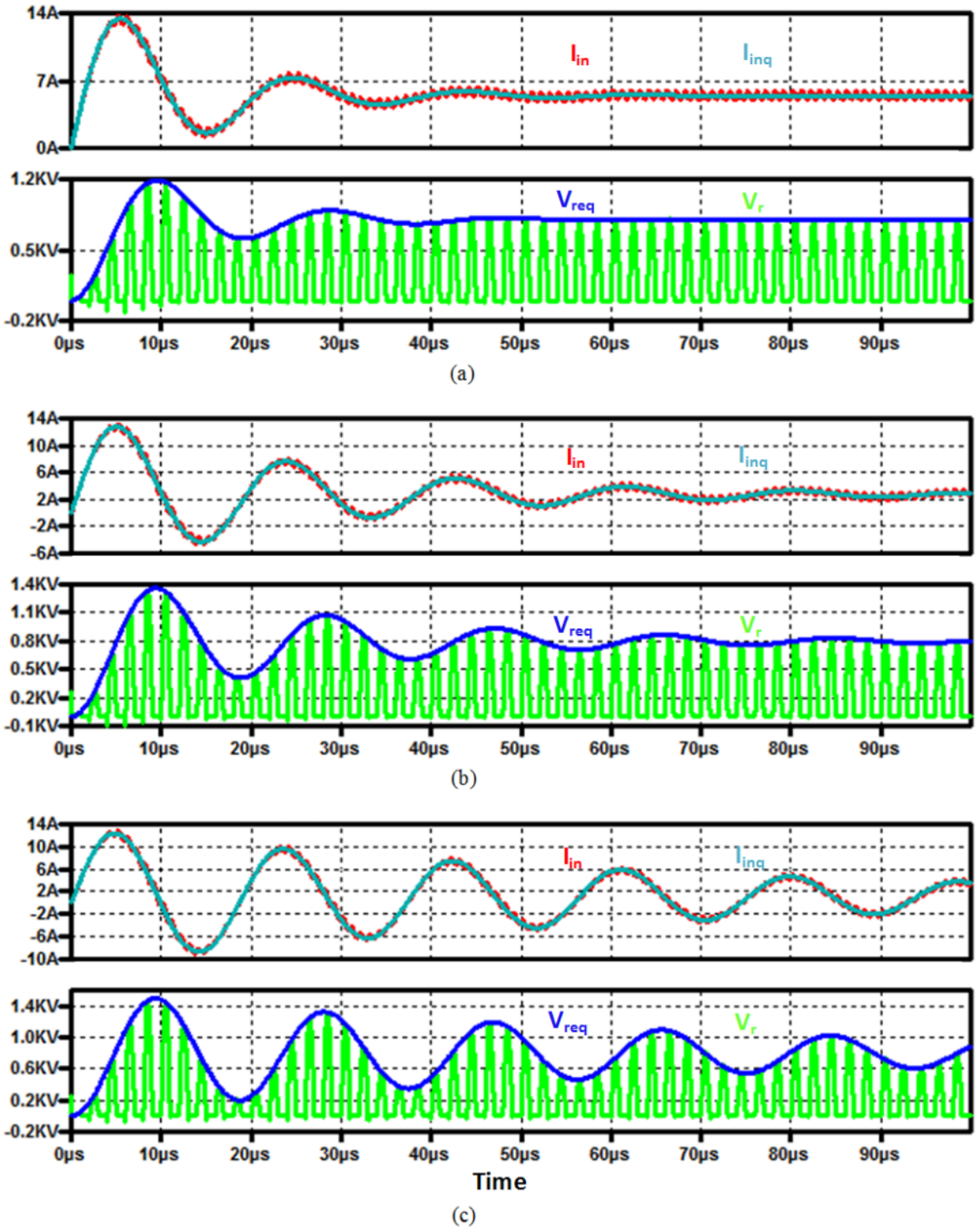


Figure D-3. Comparison between switching simulation model and Low-frequency model of the boost amplifier for the circuit variables given in Figure D-1 and simulation parameters given in Table D-1. The input inductance is L_{in} = 125 µH, and the loaded quality-factor is (a) Q = 10; (b) Q = 20; (c) Q = 50.

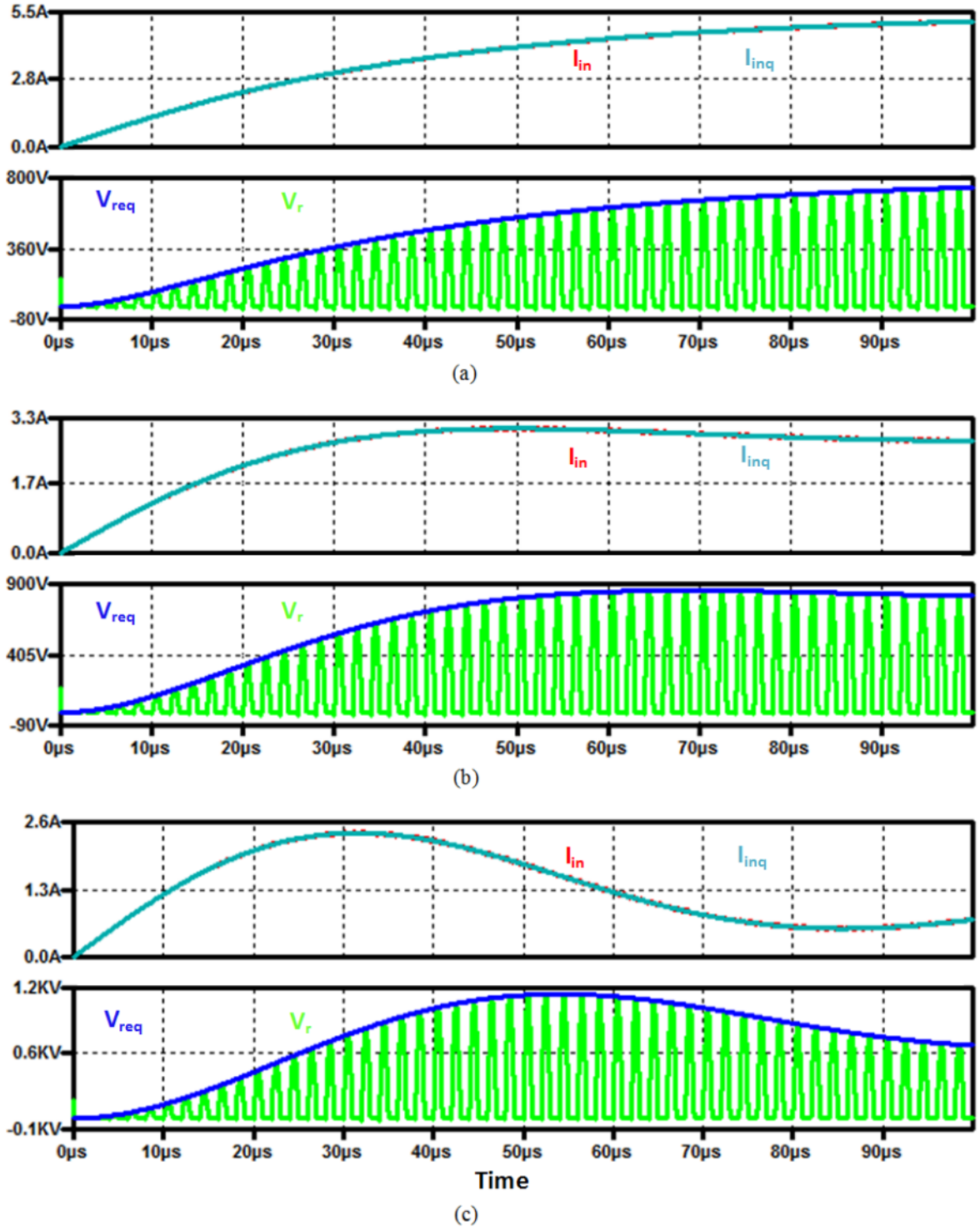


Figure D-4. Comparison between switching simulation model and Low-frequency model of the boost amplifier for the circuit variables given in Figure D-1 and simulation parameters given in Table D-1. The input inductance is L_{in} = 4 mH, and the loaded quality-factor is (a) Q = 10; (b) Q = 20; (c) Q = 50.

References

[1] A. W. Green, "Modelling a push-pull parallel resonant convertor using generalised state-space averaging," *Electric Power Applications, IEE Proceedings B,* vol. 140, pp. 350-356, 1993.

Appendix E. Validation of the PWM Compensation Model

E.1. Model Validation using Switching Simulation

Simplified circuit of the two-phase buck-boost amplifier is shown in Figure E-1. The Generalized state-space averaged (GSSA) model was developed in Chapter 4 for the circuit in Figure E-1. The synchronous condition was computed from the GSSA model by setting cosine component of the resonant voltage to be zero, as given with

$$
\begin{aligned}
&V_r(t) = V_a(t) - V_b(t) = V_{rs}\sin\omega t + V_{rc}\cos\omega t \\
&V_{rc} = R_r Y_1 V_{bus}\left(\left(1+\frac{\pi Q}{R_r Y_1}+Q^2\right)d + \frac{1+Q^2}{\pi Y_1 \omega L_{in}} f_{eR}(\Psi_1, d)\right) = 0 \\
&f_{eR}(\Psi_1, d) = -2\sin(\pi d)\sin\left(2\pi\left(\Psi_1+\frac{d}{2}\right)\right) + \frac{4}{3\pi}\sin(2\pi d)\cos\left(4\pi\left(\Psi_1+\frac{d}{2}\right)\right)
\end{aligned}
\qquad \text{(E-1)}
$$

where V_{bus} is the input voltage to the buck-boost, Y_1 is defined with (4-19), d is the duty-cycle of the PWM sources $V_1(t)$ and $V_2(t)$, and Ψ_1 is the phase-shift of the rising edge of $V_1(t)$ to the rising edge of $S_2(t)$. The Ψ_1 is the control variable since its value can be adjusted so the amplifier is kept in synchronization.

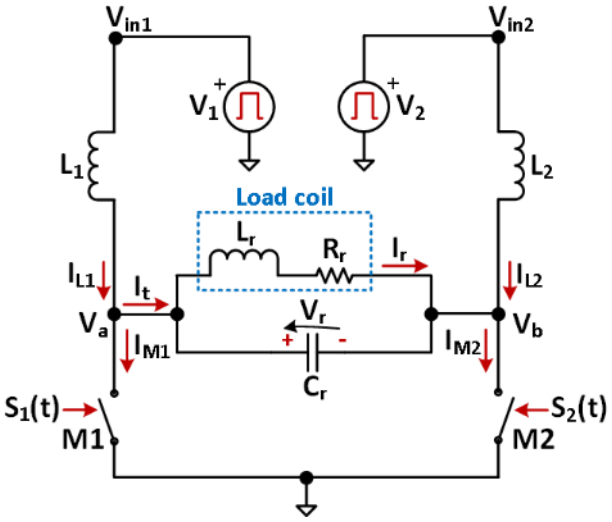


Figure E-1. Simplified model of the two-phase buck-boost amplifier for which GSSA was developed in Chapter 4. For definitions of $S_1(t)$ and $S_2(t)$ see equation . For definitions of V1 and V2 see (4-23), (4-24), (4-25), and Figure 4-14)

The validity of the GSSA model for dc excitation (d = 1) was done in Chapter 3 by checking if the model predicts synchronous condition right. Similar approach is taken here, where GSSA model with PWM excitation is compared with equivalent switching simulation model in LT-spice (Figure E-2). Both models are set for synchronous condition. In GSSA model the synchronization is maintained by numerically computing Ψ_1 so the (E-1) is satisfied ($V_{rc} = 0$). In switching simulation model the Ψ_1 is manually adjusted for synchronization. The switching model is more accurate, since it considers all harmonics that are generated by sources and are propagated to the resonant tank. The GSSA model is simpler since it only considers harmonics up to the second. Also, switching simulation model contain lossy elements in its reactive components so the convergence is not an issue. The control variable Ψ_1 is compared for both models for the case of the switching frequency of f_{sw} = 500 kHz, bus voltage of V_{bus} = 600 V and output's reactive power of around PQ = 14 kVA. The quality factor of the load for both models is varied between ten and fifty. A range of input inductance values is considered, from 50 μH to 230 μH. The range covers very small inductance (50 μH), up to the moderate value (230 μH). Higher values are not considered since the input current is becoming more and more the dc value and the capability for compensation is lost. The duty-cycle is varied between d = 0.1 to d = 0.5.

First validation example is done for L_{in} = 50 μH. The parameters for the GSSA and switching models are given in Table E-1. Figure E-3 plots the dependence of the control variable Ψ_1 on the duty-cycle for both models and range of duty-cycles. Different loaded quality-factors are considered. The Figure E-3 shows that the two models are performing very similarly.

Table E-1. Parameters of the two-phase buck-boost amplifier used to compute synchronous condition from (E-1), and for the switching model simulated in LT-spice.

f_{sw} (kHz)	500	V_{bus} (V)	600
$L_1 = L_2 = L_{in}$ (μH)	50	C_r (nF)	14.38
L_r (μH)	7.27	Q	10-50
d	0.1-0.5	Ψ_1	Computed using (E-1) or adjusted in simulations for synchronous condition

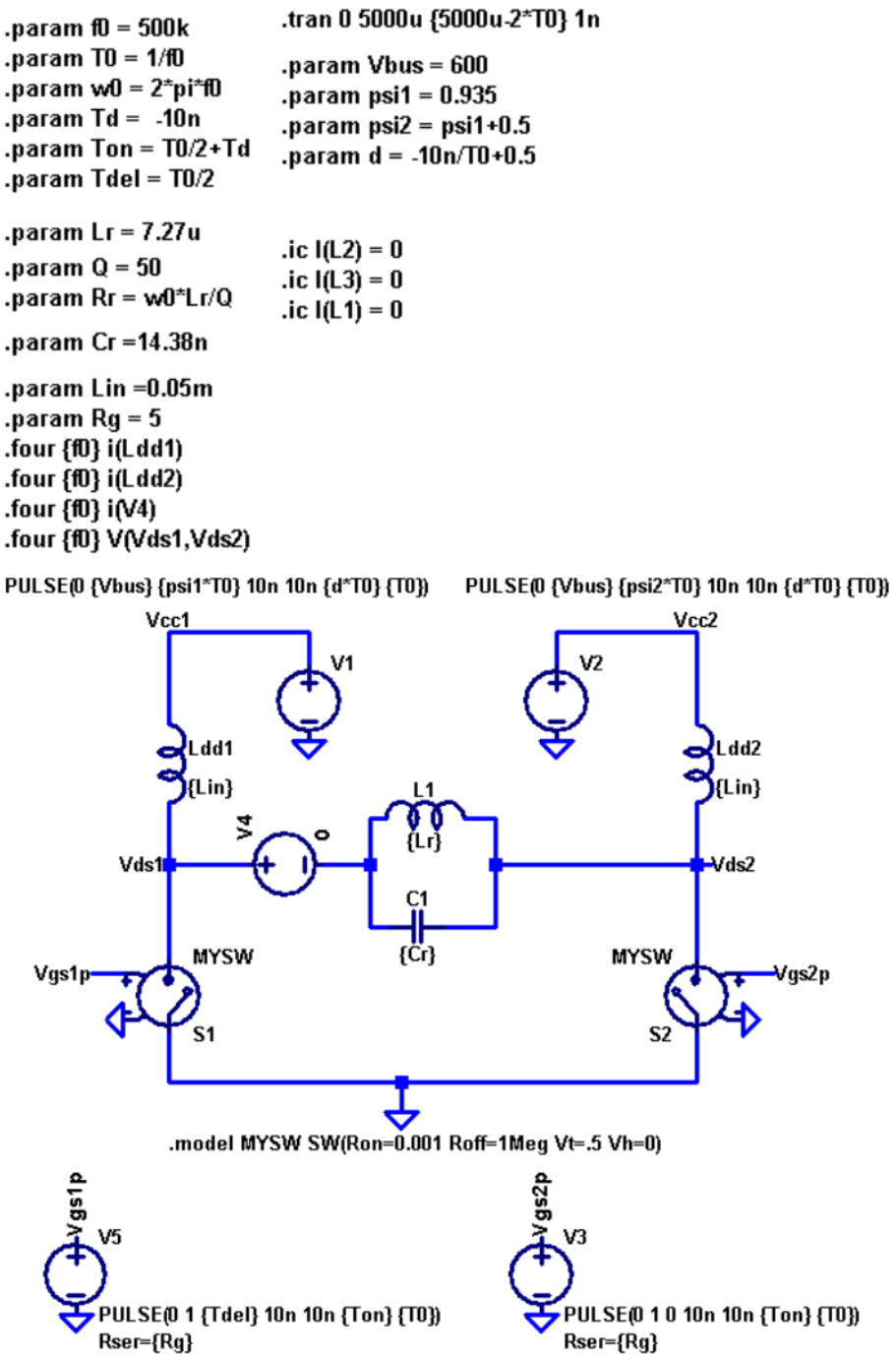
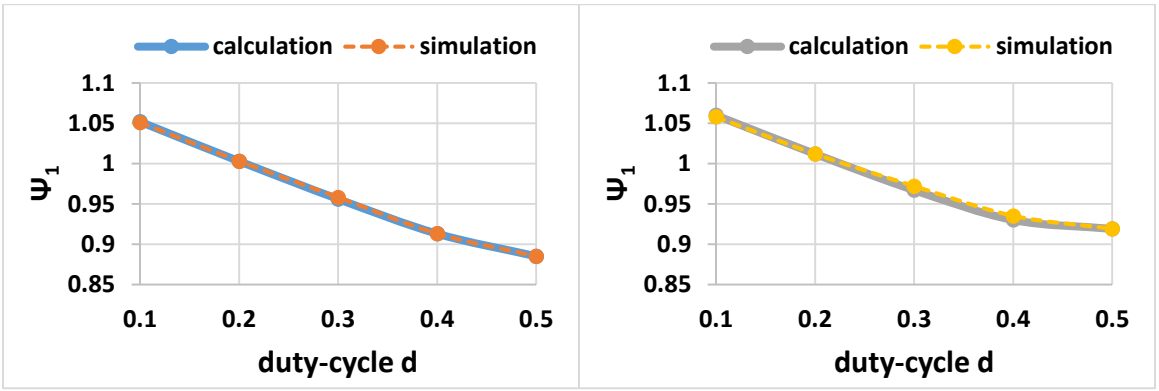
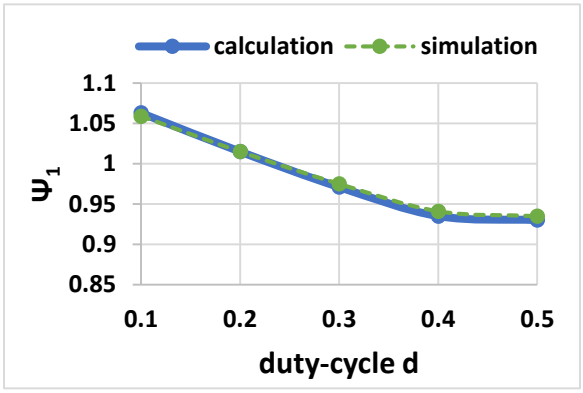


Figure E-2. Switching simulation model of the circuit in Figure E-1 made in LT-spice. Circuit components have parasitic resistances in order to help convergence of the model. Inductors and switches have parasitic series resistance of 1 mΩ, while resonant capacitor has 22 mΩ.



(b) (b)



(c)

Figure E-3. Dependence of controlled variable Ψ_1 on the duty-cycle d for two-phase buck-boost amplifier operated at synchronous condition. Solid lines represent numerically calculated values from (E-1) and dashed lines represent values of Ψ_1 obtained from the switching model using ideal switches presented in Figure E-2. Parameters of the buck-boost amplifier are given in Table E-1, input inductance is L_{in} = 50 µH, and (a) Q = 10; (b) Q = 20; (c) Q = 50. Numerically computed values show close match with the results obtained from switching simulations.

Figure E-4 shows the difference between the obtained variables for the control variable Ψ_1 in both models. At f_{sw} = 500 kHz, the difference of $\Delta\Psi_1$ = 0.01 corresponds to time delay of only 20 ns, so the GSSA model can be considered quite accurate.

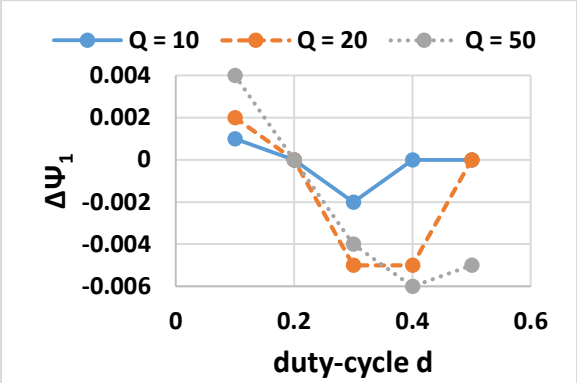
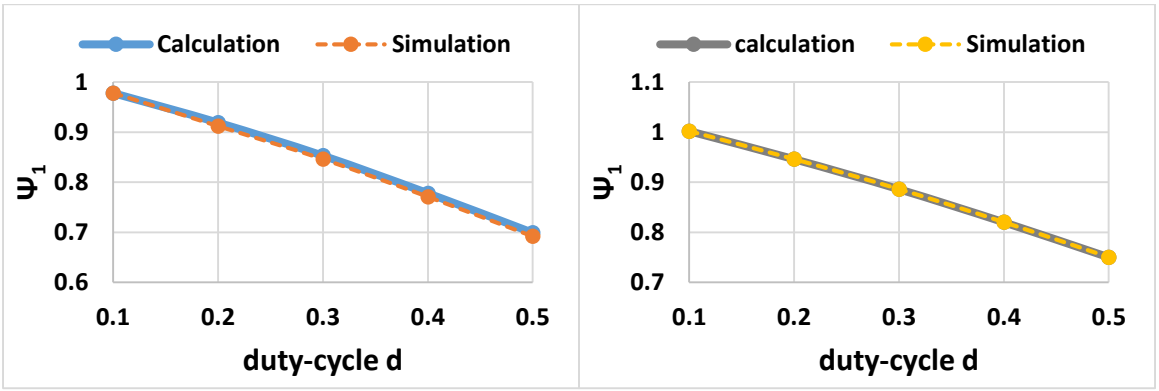


Figure E-4. The difference between obtained values for the control variable Ψ_1 from numerical computation of the mathematical model and switching simulation model. The input inductance value is L_{in} = 50 µH. The difference exist since the switching simulation model includes effects of higher harmonics in circuit's state variables, and introduces limited but still significant loss that is required to provide convergence of the simulation.

Next validation example is shown for L_{in} = 125 µH. The parameters for the GSSA and switching models are given in Table E-2. Figure E-5 plots the dependence of the control variable Ψ_1 on the duty-cycle for both models and range of duty-cycles. Different loaded quality-factors are considered (Q = 10-50). The Figure E-5 shows that the two models are performing very similarly.

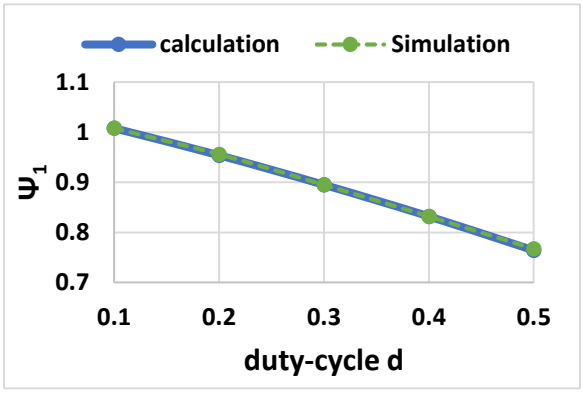
Table E-2. Parameters of the two-phase buck-boost amplifier used to compute synchronous condition from (E-1), and for the switching model simulated in LT-spice. The input inductance is set to L_{in} = 125 µH.

f_{sw} (kHz)	500	V_{bus} (V)	600
$L_1 = L_2 = L_{in}$ (µH)	125	C_r (nF)	14.38
L_r (µH)	7.27	Q	10-50
d	0.1-0.5	Ψ_1	Computed using (E-1) or adjusted in simulations for synchronous condition



(a)

(b)



(c)

Figure E-5. Dependence of controlled variable Ψ_1 on the duty-cycle d for two-phase buck-boost amplifier operated at synchronous condition. Solid lines represent numerically calculated values from (E-1) and dashed lines represent values of Ψ_1 obtained from the switching model using ideal switches presented in Figure E-2. Parameters of the buck-boost amplifier are given in Table E-2, input inductance is L_{in} = 125 µH, and (a) Q = 10; (b) Q = 20; (c) Q = 50. Numerically computed values show close match with the results obtained from switching simulations.

Figure E-6 shows the difference between the obtained variables for the control variable Ψ_1 in both models. The difference is slightly higher than in the previous case but it is still limited and the GSSA model can be considered to be very accurate.

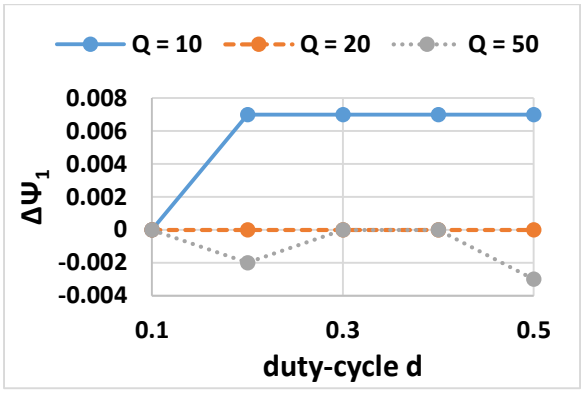
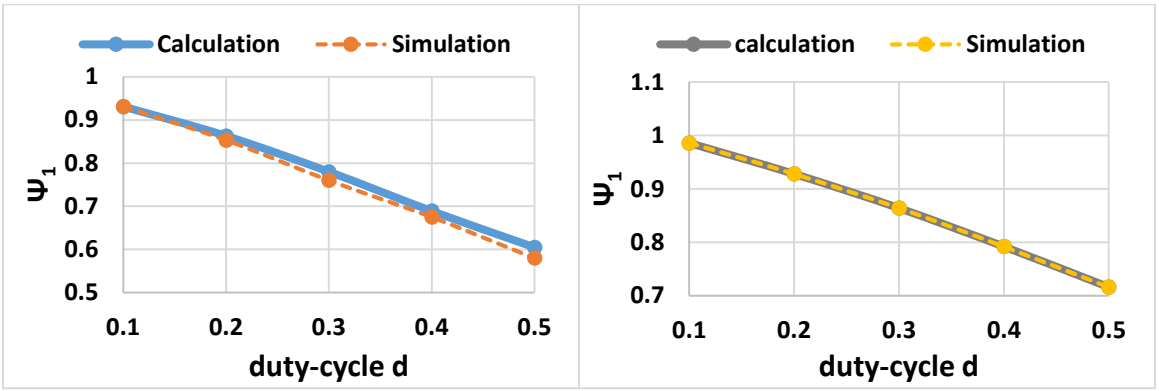


Figure E-6. The difference between obtained values for the control variable Ψ_1 from numerical computation of the mathematical model and switching simulation model. The input inductance value is L_{in} = 125 µH. The difference exist since the switching simulation model includes effects of higher harmonics in circuit's state variables, and introduces limited but still significant loss that is required to provide convergence of the simulation.

Final validation example is shown for L_{in} = 230 µH. The parameters for the GSSA and switching models are given in Table E-3. Figure E-7 plots the dependence of the control variable Ψ_1 on the duty-cycle for both models and range of duty-cycles. Different loaded quality-factors are considered (Q = 10-50). The Figure E-7 shows that the two models are performing very similarly for high values of the quality factor, and are having some difference when quality factor is low (Q = 10). However, the difference is not excessive.

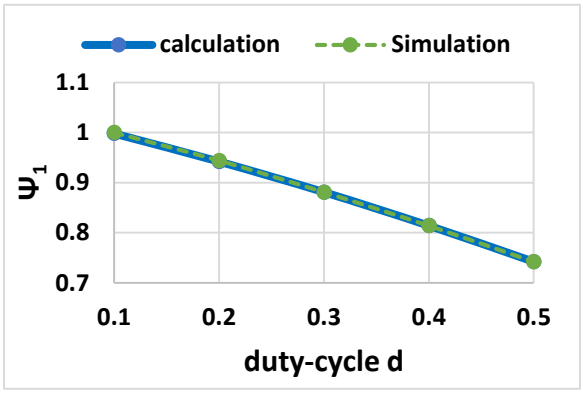
Table E-3. Parameters of the two-phase buck-boost amplifier used to compute synchronous condition from (E-1), and for the switching model simulated in LT-spice. The input inductance is set to L_{in} = 230 µH, and resonant capacitor to C_r = 14.2 nF.

f_{sw} (kHz)	500	V_{bus} (V)	600
$L_1 = L_2 = L_{in}$ (µH)	230	C_r (nF)	14.2
L_r (µH)	7.27	Q	10-50
d	0.1-0.5	Ψ_1	Computed using (E-1) or adjusted in simulations for synchronous condition



(a)

(b)



(c)

Figure E-7. Dependence of controlled variable Ψ_1 on the duty-cycle d for two-phase buck-boost amplifier operated at synchronous condition. Solid lines represent numerically calculated values from (E-1) and dashed lines represent values of Ψ_1 obtained from the switching model using ideal switches presented in Figure E-2. Parameters of the buck-boost amplifier are given in Table E-3, input inductance is L_{in} = 230 µH, and (a) Q = 10; (b) Q = 20; (c) Q = 50. Numerically computed values show close match with the results obtained from switching simulations.

Figure E-8 shows the difference between the obtained variables for the control variable Ψ_1 in both models. Notable is the difference for the low value of the quality factor (Q = 10). This is due to reduced capability to produce significant amplitude of fundamental frequency current since the input inductance is doubled. Still, $\Delta\Psi_1$ produces the delay of V1 function by 50 ns, which is not too excessive. Thus, the GSSA modeling method and correlating set of modeling assumptions produce a sufficiently accurate model that can be used to describe the buck-boost amplifier.

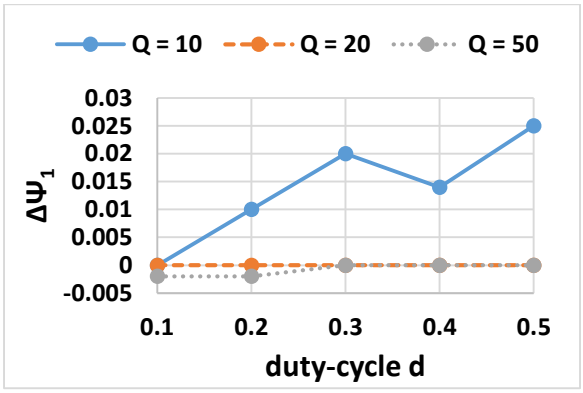


Figure E-8. The difference between obtained values for the control variable Ψ_1 from numerical computation of the mathematical model and switching simulation model. The input inductance value is L_{in} = 230 µH. The difference exist since the switching simulation model includes effects of higher harmonics in circuit's state variables, and introduces limited but still significant loss that is required to provide convergence of the simulation.

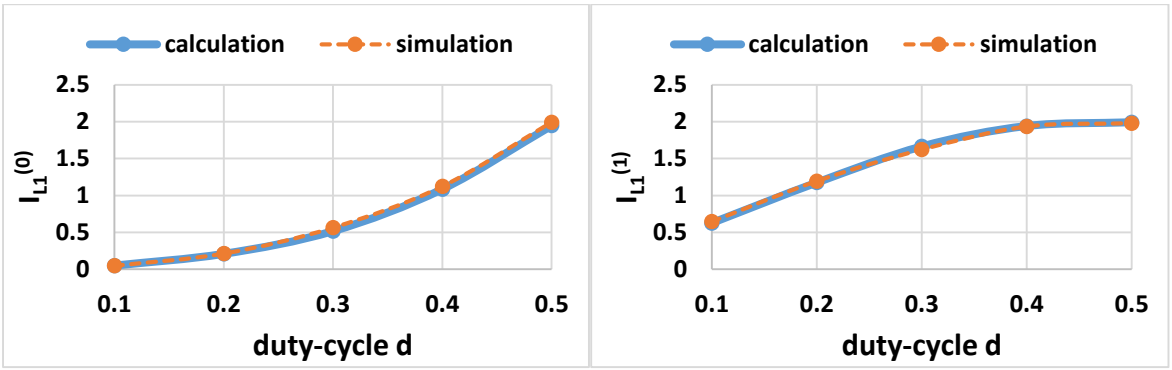
E.2. Validation of Formulas used to Compute Input Inductor's Current

Key formulas for analyzing the buck-boost amplifier are the ones for current of the input inductors. Input inductor current defines the loss of transistors in the boost stage, impacts ZVS condition of buck switches, and is used in input power computation. The input inductor current harmonics equations are written as

$$
\begin{aligned}
I_{L1}^{(0)}(t) &= \frac{\pi^2}{4}\frac{dV_{bus}}{R_r\left(1+Q^2\right)} - \frac{V_{bus}}{4\omega L_{in}} f_{el}\left(\Psi_1, d\right) \\
f_{el}\left(\Psi_1, d\right) &= 2\sin(\pi d)\cos\left(2\pi\left(\Psi_1 + \frac{d}{2}\right)\right) + \frac{2}{3\pi}\sin(2\pi d)\sin\left(4\pi\left(\Psi_1 + \frac{d}{2}\right)\right) \\
I_{L1}^{(1)}(t) &= \frac{\pi d V_{bus}}{2\omega L_{in}}\cos(\omega t) + \frac{2V_{bus}}{\pi\omega L_{in}}\sin(\pi d)\cdot\sin\left(\omega t - 2\pi\left(\psi_1 + \frac{d}{2}\right)\right) \\
I_{L1}^{(2)}(t) &= \frac{dV_{bus}}{3\omega L_{in}}\sin(2\omega t) + \frac{V_{bus}}{2\pi\omega L_{in}}\sin(2\pi d)\cdot\sin\left(2\omega t - 4\pi\left(\psi_1 + \frac{d}{2}\right)\right)
\end{aligned}
\qquad \text{(E-2)}
$$

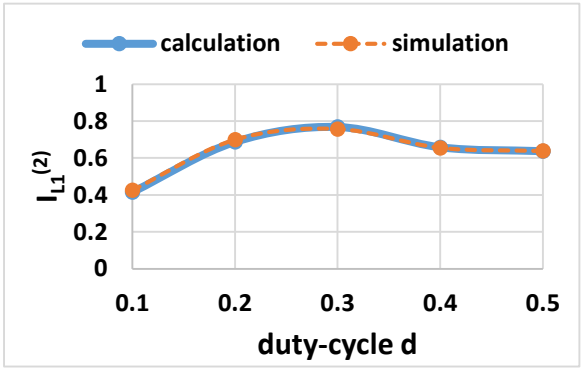
The validation of (E-2) is performed it the same fashion as in previous section of this appendix, where the values obtained from GSSA model are compared to compared to ones from switching simulation model. The buck-boost amplifier's parameters are also same is in previous condition. From the following set of figures it is seen that (E-2)

are accurate descriptions of input inductor's currents, and that (G-2) can be used for predicting the behavior of the amplifier.



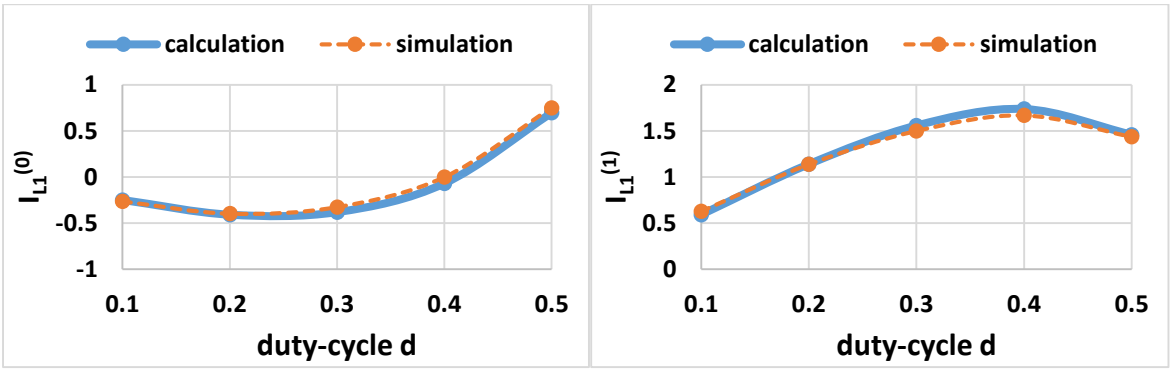
(a)

(b)



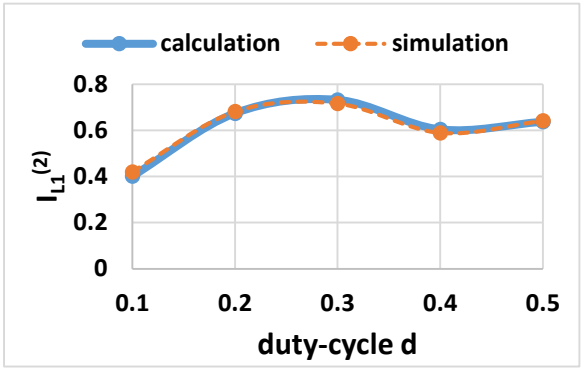
(c)

Figure E-9. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 50 µH, and the quality factor is Q = 10. The rest of the parameters is the same as in Table E-1. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**



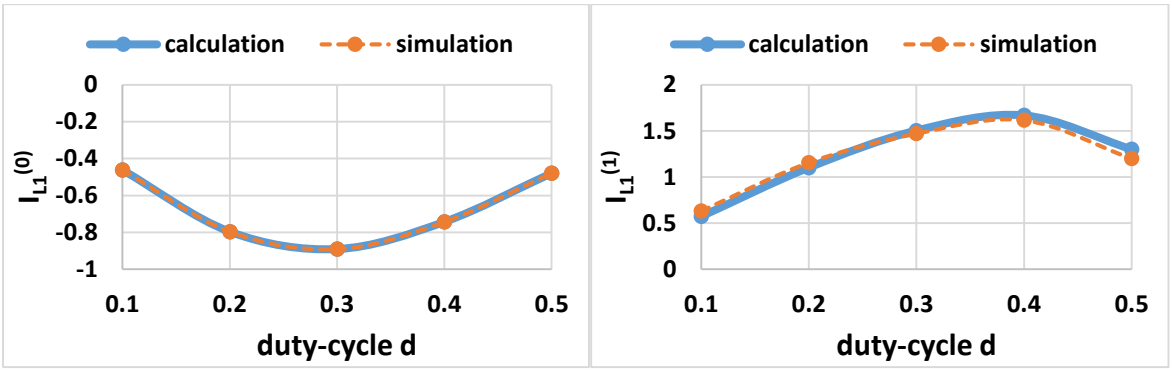
(a)

(b)



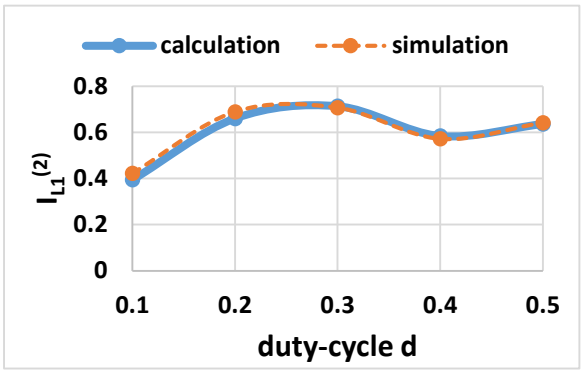
(c)

Figure E-10. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 50 µH, and the quality factor is Q = 20. The rest of the parameters is the same as in Table E-1. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**



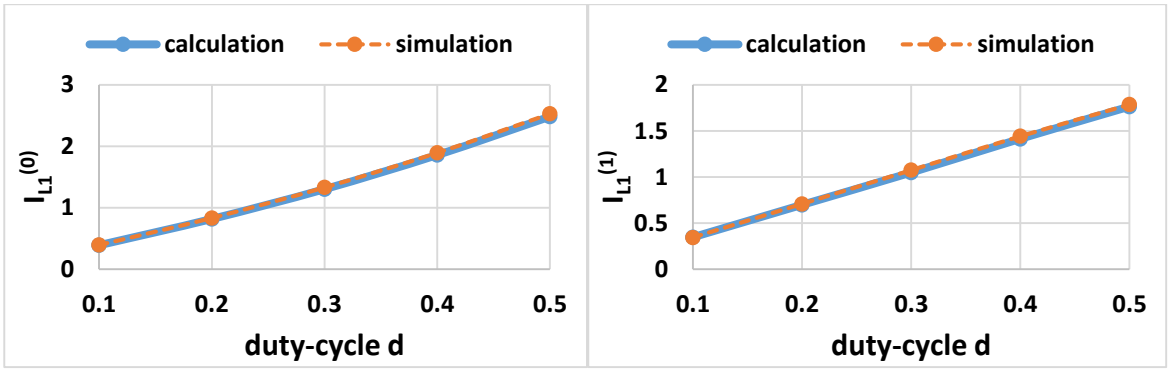
(a)

(b)



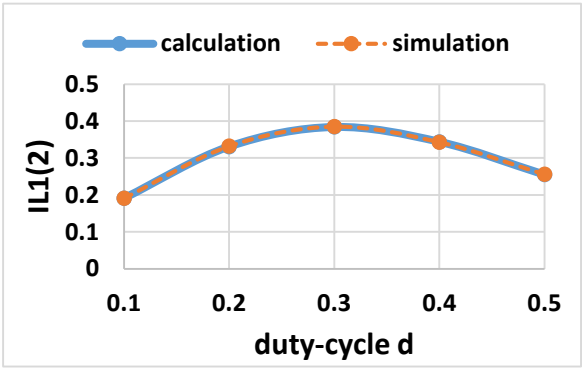
(c)

Figure E-11. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 50 µH, and the quality factor is Q = 50. The rest of the parameters is the same as in Table E-1. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**



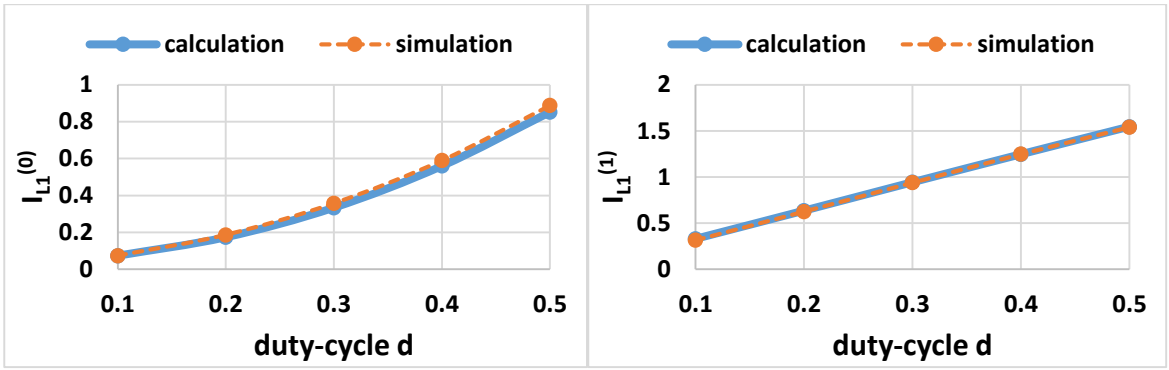
(a)

(b)



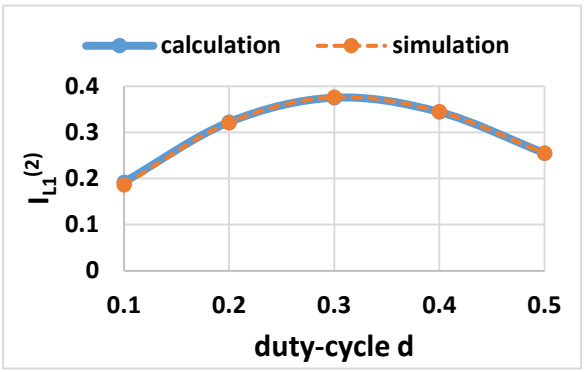
(c)

Figure E-12. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 125 µH, and the quality factor is Q = 10. The rest of the parameters is the same as in Table E-2. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**



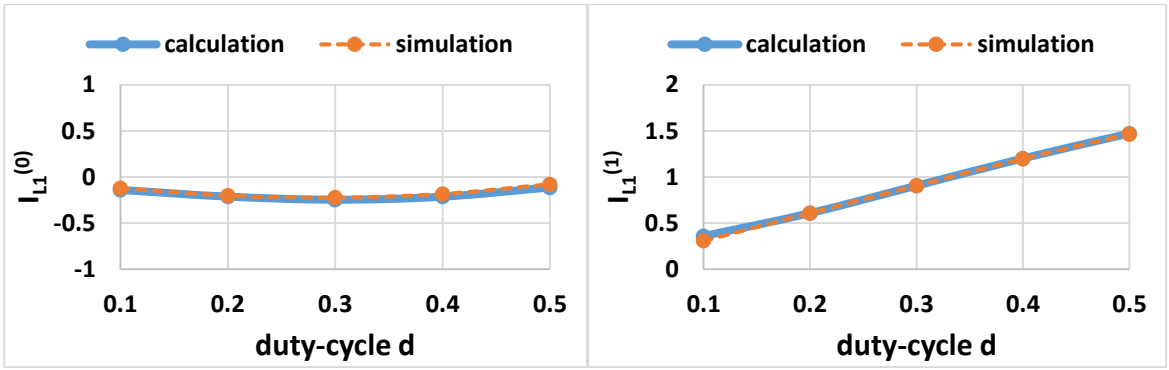
(a)

(b)

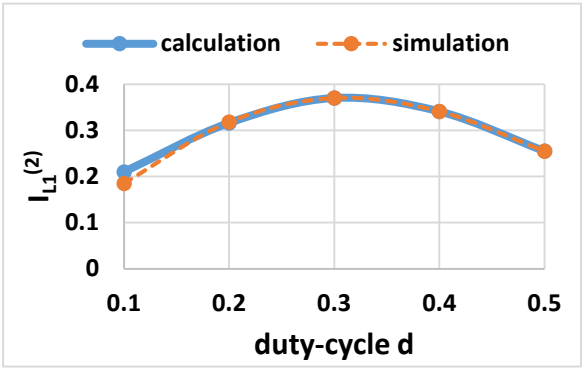


(c)

Figure E-13. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 125 µH, and the quality factor is Q = 20. The rest of the parameters is the same as in Table E-2. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**

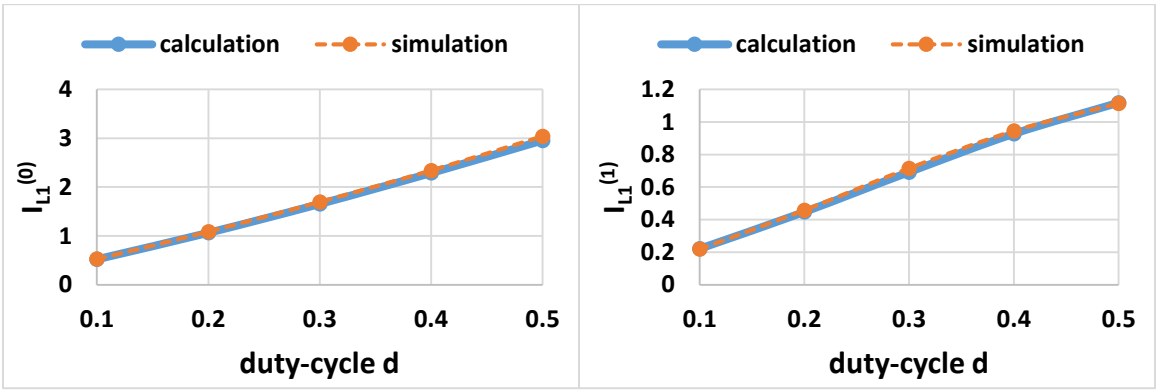


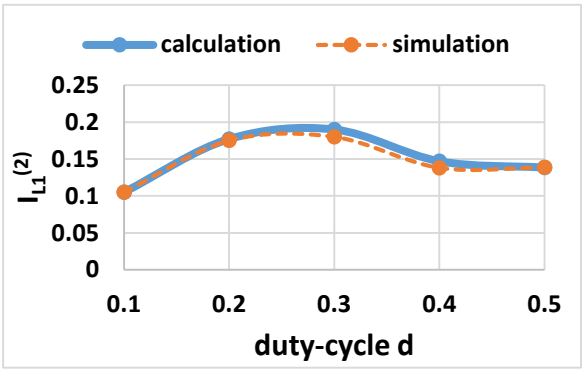
(a) (b)



(c)

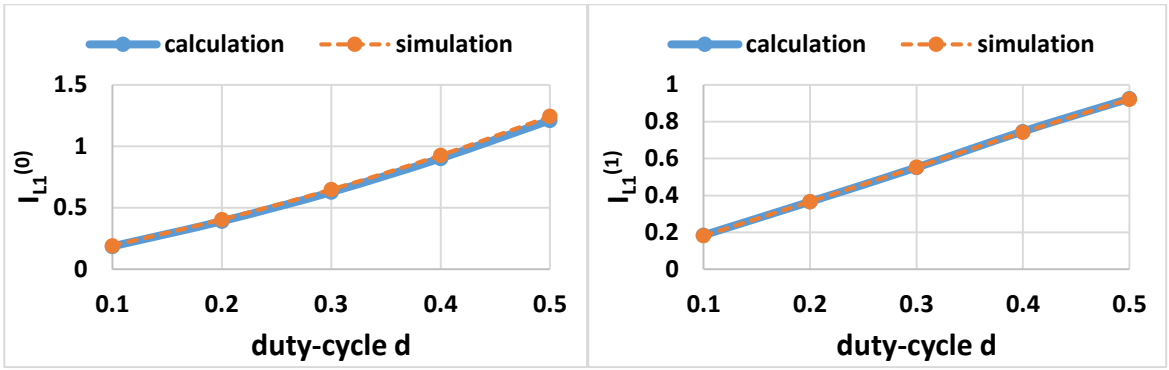
Figure E-14. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 125 µH, and the quality factor is Q = 50. The rest of the parameters is the same as in Table E-1. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**





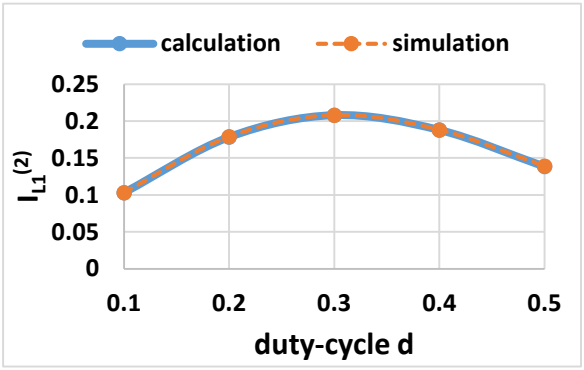
(c)

Figure E-15. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 230 µH, and the quality factor is Q = 10. The rest of the parameters is the same as in Table E-3. (a) $I_{L1}^{(0)}(t)$; (b) $I_{L1}^{(1)}(t)$; (c) $I_{L1}^{(2)}(t)$.



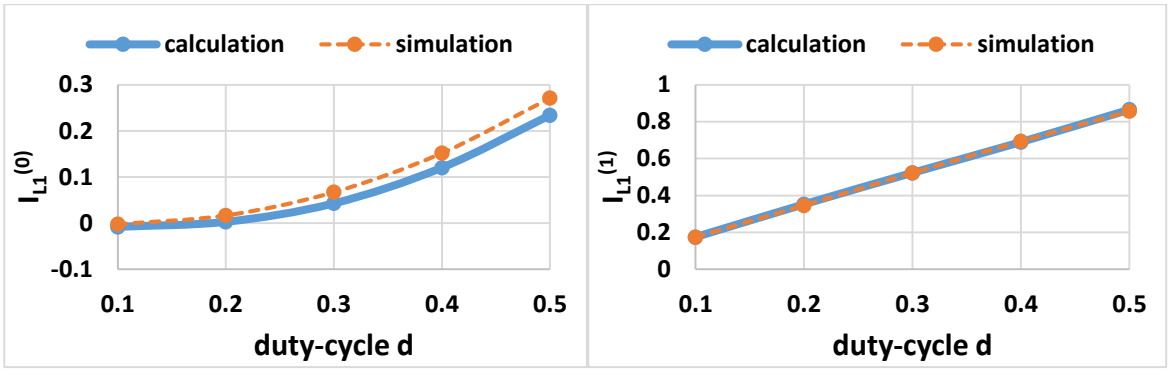
(a)

(b)



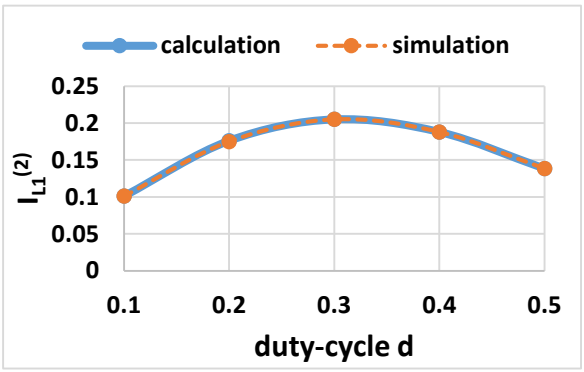
(c)

Figure E-16. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 230 µH, and the quality factor is Q = 20. The rest of the parameters is the same as in Table E-3. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**



(a)

(b)



(c)

Figure E-17. Difference of calculated and simulated values of input inductor current harmonics. The input inductance is L_{in} = 230 µH, and the quality factor is Q = 50. The rest of the parameters is the same as in Table E-3. (a) $I_{L1}^{(0)}(t)$ **; (b)** $I_{L1}^{(1)}(t)$ **; (c)** $I_{L1}^{(2)}(t)$ **.**

References

[1] A. W. Green, "Modelling a push-pull parallel resonant convertor using generalised state-space averaging," *Electric Power Applications, IEE Proceedings B,* vol. 140, pp. 350-356, 1993.