Optimization of Bonding Geometry for a Planar Power Module to Minimize Thermal Impedance and Thermo-Mechanical Stress

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Abstract

This study focuses on development a planar power module with low thermal impedance and thermo-mechanical stress for high density integration of power electronics systems. With the development semiconductor technology, the heat flux generated in power device keeps increasing. As a result, more and more stringent requirements were imposed on the thermal and reliability design of power electronics packaging.

In this dissertation, a boundary-dependent RC transient thermal model was developed to predict the peak transient temperature of semiconductor device in the power module. Compared to conventional RC thermal models, the RC values in the proposed model are functions of boundary conditions, geometries, and the material properties of the power module. Thus, the proposed model can provide more accurate prediction for the junction temperature of power devices under variable conditions. In addition, the transient thermal model can be extracted based on only steady-state thermal simulation, which significantly reduced the computing time.

To detect the peak transient temperature in a fully packaged power module, a method for thermal impedance measurement was proposed. In the proposed method, the gate-emitter voltage of an IGBT which is much more sensitive to the temperature change than the widely used forward voltage drop of a pn junction was monitored and used as temperature sensitive parameter. A completed test circuit was designed to measure the thermal impedance of the power module using the gate-emitter voltage. With the designed test set-up, in spite of the temperature dependency of the IGBT electrical characteristics, the power dissipation in the IGBT can be regulated to be constant by

adjusting the gate voltage via feedback control during the heating phase. The developed measurement system was used to evaluate thermal performance and reliability of three different die-attach materials.

From the prediction of the proposed thermal model, it was found that the conventional single-sided power module with wirebond connection cannot achieve both good steady-state and transient thermal performance under high heat transfer coefficient conditions. As a result, a plate-bonded planar power module was designed to resolve the issue. The comparison of thermal performance for conventional power module and the plate-bonded power module shows that the plate-bonded power module has both better steady-state and transient thermal performance than the wirebonded power module. However, due to CTE mismatch between the copper plate and the silicon device, large thermo-mechanical stress is induced in the bonding layer of the power module. To reduce the stress in the plate-bonded power module, an improved structure called trenched copper plate structure was proposed. In the proposed structure, the large copper plate on top of the semiconductor can be partitioned into several smaller pieces that are connected together using a thin layer copper foil. The FEM simulation shows that, with the improved structure, the maximum von Mises stress and plastic strain in the solder layer were reduced by 18.7% and 67.8%, respectively. However, the thermal impedance of the power module increases with reduction of the stress. Therefore, the trade-off between these two factors was discussed. To verify better reliability brought by the trenched copper plate structure, twenty-four samples with three different copper plate structures were fabricated and thermally cycled from -40˚C to 105˚C. To detect the failure at the bonding layer, the curvature of these samples were measured using laser scanning before and after cycling. By monitoring the change of curvature, the degradation of bonding layer can be detected. Experimental results showed that the samples with different copper plate structure had similar curvature before thermal cycle. The curvatures of the samples with single copper plate decreased more than 80% after only 100 cycles. For the samples

with 2 × 2 copper plate and the samples with 3 × 3 copper plate, the curvatures became 75.8% and 77.5% of the original values, respectively, indicating better reliability than the samples with single copper plate. The x-ray pictures of cross-sectioned samples confirmed that after 300 cycles, the bonding layer for the sample with single copper plate has many cracks and delaminations starting from the edge.

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Chapter 1. INTRODUCTION

1.1. Motivation and Objective

In recent years, there is a growing demand to increase the power density in power module. As shown in Figure 1-1, the heat flux generated by power semiconductor devices keeps increasing [1]. In some motor drive applications, the heat flux can be higher than 200 W/cm^2 in steady-state and the peak heat flux can be as high as 400 W/cm^2 under transient conditions [2]-[3]. In spite of the more stringent transient requirements, most publications in power electronics tend to focus on steady-state thermal management

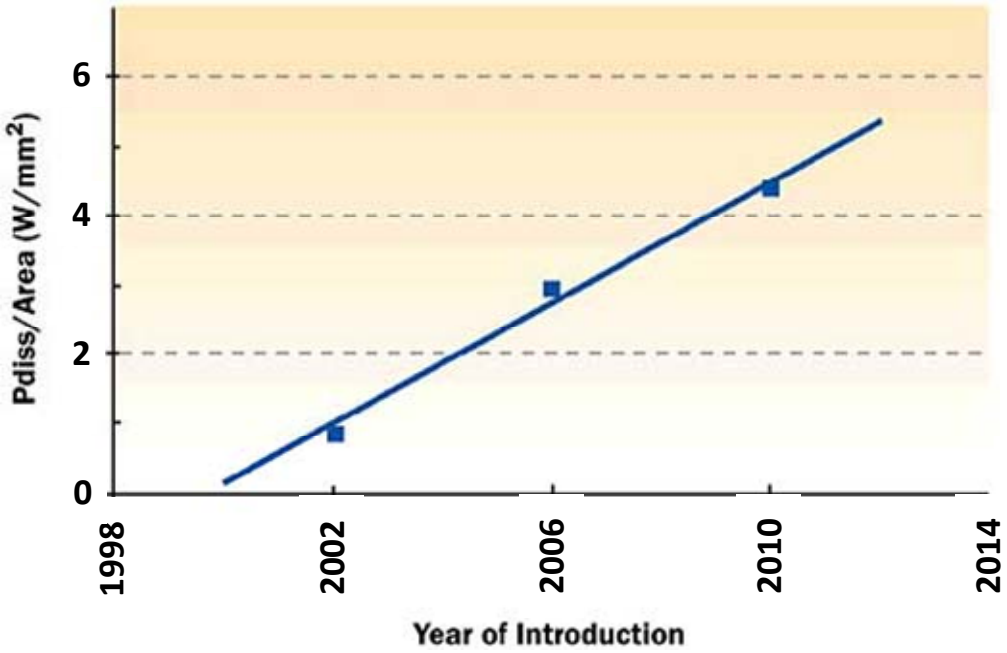


Figure 1-1. Trend in dissipated power per effective die area of the die with the highest dissipation in the power module [1] (Used under fair use guidelines, 2011).

[4]-[5]. In this dissertation, attention is paid to both steady-state thermal resistance and transient thermal impedance of the power module. To keep the peak transient temperature of semiconductor device low, a large amount of thermal mass is required in the power module. Due to large thermal capacitance, copper plate is widely used in the power module to improve transient thermal performance [6]. However, the large mismatch of

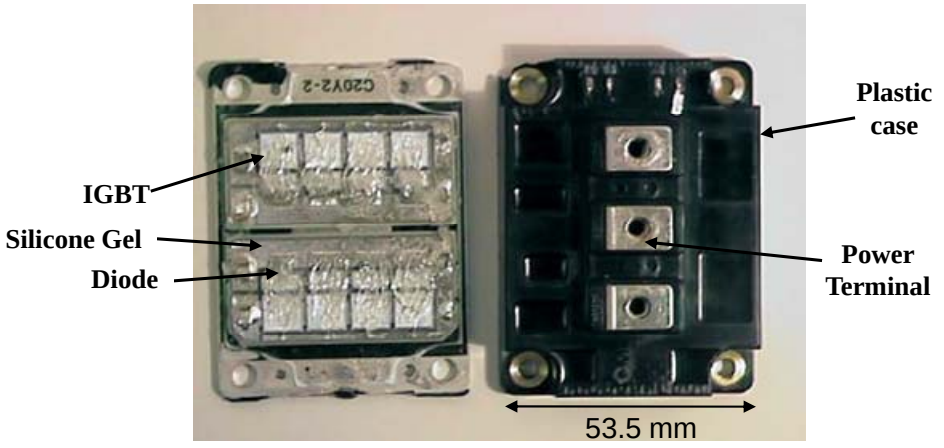
coefficient of temperature expansion (CTE) between copper and other components in the power module such as silicon die and ceramic substrates could cause severe reliability issue. Therefore, how to achieve both good thermal performance and thermo-mechanical performance is a challenge for power module design.

Before the investigation of the thermal performance of the power module, an accurate thermal model is required to predict the junction temperature of the semiconductor devices. Based on the thermal model, the geometries of the power module can be optimized and the heat transfer coefficient of the heat-exchanger can be selected. The transient thermal model also can be used for coupled electro-thermal simulation to provide more accurate predictions on the losses and the junction temperatures of the power devices.

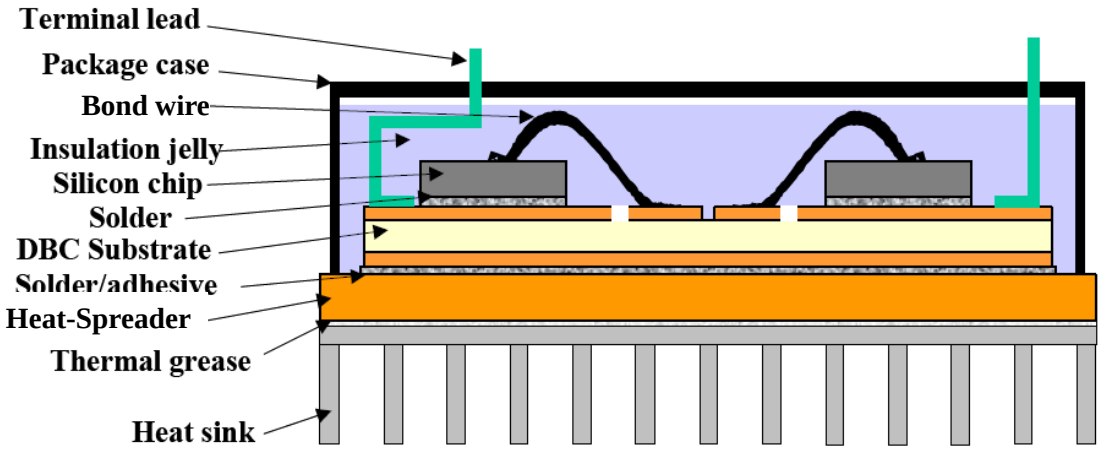
Based on previous research work [7]-[8], it can be seen that the conventional wirebonded power module (shown in Figure 1-2) cannot meet critical thermal requirements in high power density application because of its incapability of implementing double-sided cooling and lack of thermal mass. Therefore, a planar structure is desired for high density power modules. It has been reported in [9] that compared to the conventional wirebonded power module, planar power modules have several advantages, such as better thermal performance, smaller footprint area, and lower parasitic impedances.

1.2. Review of Existing Planar Packaging Technologies

In the past decade, many research works have been done to explore new planar packaging structures for the power module to achieve better thermal, electrical, and mechanical performances. In this section, several planar packaging techniques that can be applied to automotive applications (power range: 10 kW - 50 kW; voltage: 400 V - 1200 V) are reviewed. The thermal performance and mechanical performance of different packaging structures are discussed.



(a)



(b)

Figure 1-2. (a) Outside and inside of a commercial wire-bond module [7]; (b) the cross-sectional view of the IGBT module on a heatsink (Used under fair use guidelines, 2011).

1.2.1. Dimple Array Interconnection

Dimple array interconnect [11]-[12] was introduced by CPES at Virginia Tech in 2001 for motor drive application in the 600 V voltage range and up to 30 kW power range (shown in Figure 1-3). A single solid metal sheet with dimple structure is solder-attached to the source pads of the power devices as the interconnection. The gate bond wires are replaced by dimpled metal tabs. Before soldering the metal sheet to the device pads, nickel and silver have to be deposited onto the aluminum pads of the

semiconductor devices. The dimple array interconnects allow flexible layout design to populate the solder bumps across a solderable die surface. The dimple structure on the metal foil also helps form hourglass-shaped solder joint to improve compliance, easier alignment, and extra standoff height. However, it is difficult to realize double-sided cooling for the dimple array structure due to high thermal resistance of flex layer and limited solder area on the top surface of the devices.

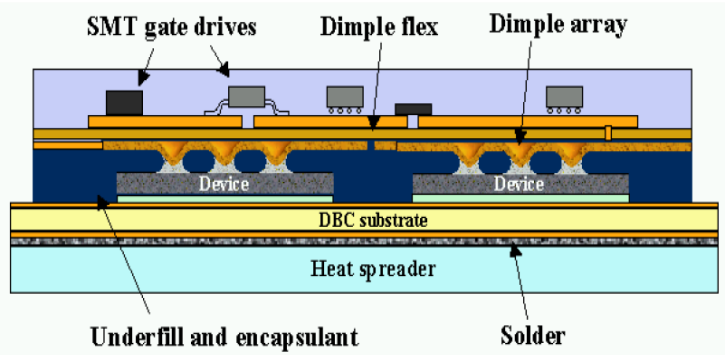


Figure 1-3. Dimple array interconnection [11] (Used under fair use guidelines, 2011).

1.2.2. Flip-Chip-on-Flex Interconnection

Flip-chip-on-flex (FCOF) as shown in Figure 1-4 was introduced by CPES for motor drive application in the 40 V – 400 V voltage range and up to 10 kW power range [13]-[19]. The package consists of three interconnection layers. The direct bond copper (DBC) substrate provides the mechanical support and power interconnections for the bottom terminals of the devices. The top power interconnection of the devices is implemented by using an insulated metal substrate called Pyralux from DuPont Corporation [20]. In Pyralux, one layer of polyimide film (Kapton tape) is bonded between two copper sheets so that the IMS is ready to be soldered. The bottom copper layer of the Pyralux provides interconnections for source and gate of the power devices. The top flex layer is utilized for driving and control circuits.

In the FCOF package, thanks to flexibility of the Pyralux material, the thermo-mechanical stress induced by CTE mismatch can be absorbed. As a result, the reliability of the power module can be improved. However, due to the limitation on the copper thickness of Pyralux, the power rating of power module is constrained to be less than 10 kW. In terms of thermal performance of the power module, the DBC substrate is the only thermal path due to high thermal resistance of Kapton layer in the Pyralux. Therefore, it is difficult to implement double-sided cooling technique for FCOF package.

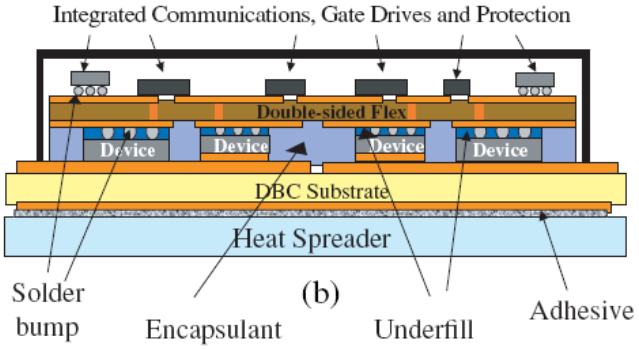


Figure 1-4. Flip-chip on flex interconnection [13] (Used under fair use guidelines, 2011).

1.2.3. Sandwich Structure

Sandwich structure was introduced by Denso, Universities of Nottingham, and Cambridge in 2007 for motor drive application up to 600 V voltage range and 10 kW power range [23]-[25]. In this structure, the power semiconductor devices are sandwiched between two DBC substrates as shown in Figure 1-5. The non-standard two-step etching process is used to pattern the top and bottom interconnects. The assembly of the power modules requires two reflow steps. The first step is to solder the dies to the bottom DBC tile using a high-temperature alloy. Then a lower temperature solder paste is applied onto the bottom substrate and dies by stencil printing. In the second reflow step, the top DBC substrate is soldered to the gate and source pads.

Thanks to large solder area on the top of the devices and high thermal conductivity of the top DBC substrate, the heat generate from semiconductor devices can be quickly removed from both sides of the power module. Therefore, the double-sided cooling technique can be easily applied, leading to superior thermal performance. However, due to less compliance and large CTE mismatch between the DBC substrate and silicon devices, large thermo-mechanical stress could be induced in the power module during the thermal cycling.

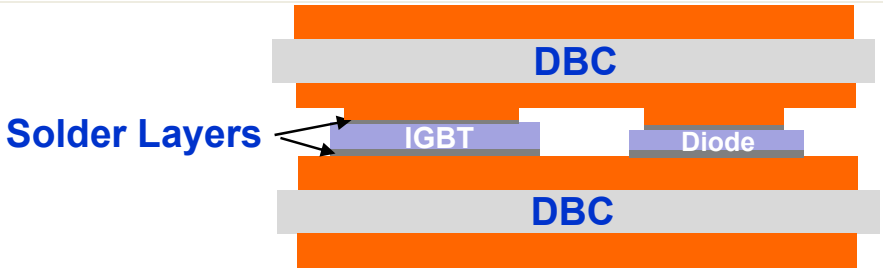


Figure 1-5. Sandwich structure of power module [23] (Used under fair use guidelines, 2011).

1.2.4. Power Post/Bump Interconnection

A power post interconnection called Metal-Post-Interconnected-Parallel-Plate Structure (MPIPPS) was firstly proposed by CPES in [32]. In 2006, Alstom proposed a similar structure called power bump for traction application in the 1500 V – 3300 V voltage range and 1200 A – 2400 A current range [26]-[29]. In power bump structure, copper cylinders or balls are soldered between the chip and substrate (shown in Figure 1-6). The bumps provide high current and thermal path for the power module and standoff between substrates for electrical isolation after encapsulation. Compared to the sandwich structure, the power bumps between the top substrate and the devices provide better compliance, resulting in better reliability. This structure is designed to allow the double-sided liquid cooling. A comparison with an equivalent water-cooled three-phase

inverter shows the following gains: 55% in weight, 45% in volume, and 30% in cost assuming the same volume of production.

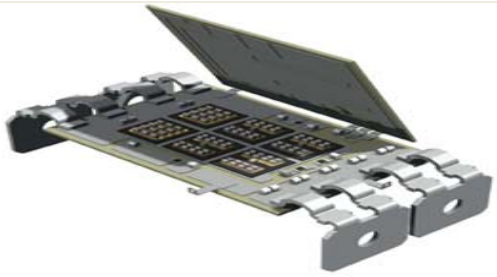


Figure 1-6. Power bump packaging for power module [26] (Used under fair use guidelines, 2011).

1.2.5. SKiN Power Module

SKiN was developed by Semikron for three phase inverter in the power rating of 600 V – 1200 V voltage and up to 100 A current [30]. Having the similar idea with dimple array interconnection, the power semiconductor devices are welded with the aluminum emitter and gate surface on aluminum punched dimple array structures of a flex board (shown in Figure 1-7). A packaging concept is to attach the power chips to a flexible printed circuit board by ultrasonic welding. The key material is a specially developed isolated flex board having a bottom layer made of thick aluminum and a copper layer on the top. The dies can be welded to a punched dimple structure on the aluminum layer by the ultrasonic bonder. The thick aluminum layer can be used to carry high current in the power module while the copper layer is used for low power circuits. Thanks to the thick aluminum layer, the SKiN power module is able to handle higher power than the flip-chip on flex circuit. In addition, the welding of the aluminum layer on the flex board to the aluminum pads of the devices has better reliability than the soldering. However, the implementation of the double-sided cooling in the SKiN power module is still difficult due to the high thermal resistance of the flex board.

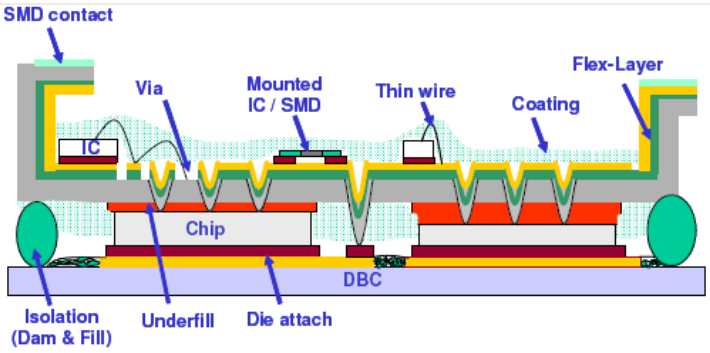


Figure 1-7. SKiN power module from Semikron [30] (Used under fair use guidelines, 2011).

1.2.6. Pressure Contact Techniques from Semikron

In recent years, several techniques were proposed by Semikron to replace the solder layers in the power module with silver sintering and pressure contact. MiniSKiiP was introduced by Semikron for motor drive applications in the range of 600 V – 1200 V and up to 15 kW voltage [35]. In order to make mounting and removal of the power module easy, spring contact systems was used (shown in Figure 1-8). The power module is clamped between the cooler and the PCB with one or two screws, enabling electrical and thermal contact at the same time. In case of a defect, the system can be un-screwed to replace the defect components.

SKiM is another technique introduced by Semikron for automotive applications in the range of 600 V – 1200 V and 22 kW – 150 kW [31]-[34]. As shown in Figure 1-9, similar with MiniSKiiP, this technology eliminates the solder from power modules using silver sintering that is more reliable and has better electrical and thermal performance. This package is based on the SKiiP package. SKiM is a 100% solder-free packaging technology. Pressure contact is used to form the interconnection for the terminals on the top of the devices and among devices. The DBC substrate carrying semiconductor chips is located in a frame. This frame aligns a bridge element that transfers vertical pressure to the substrate through its distributed pressure columns. The pressure is generated by screwing a pressure plate onto the heat sink, with a spring pad inserted between pressure

plate and bridge element in order to ensure even pressure distribution. The electrical interface from gate driver PCB to DBC substrate is realized by spring contacts, which are integrated in the bridge element, while the power terminals are bolt connections soldered to the substrate.

Figure 1-8. MiniSKiiP power module from Semikron [35] (Used under fair use guidelines, 2011).

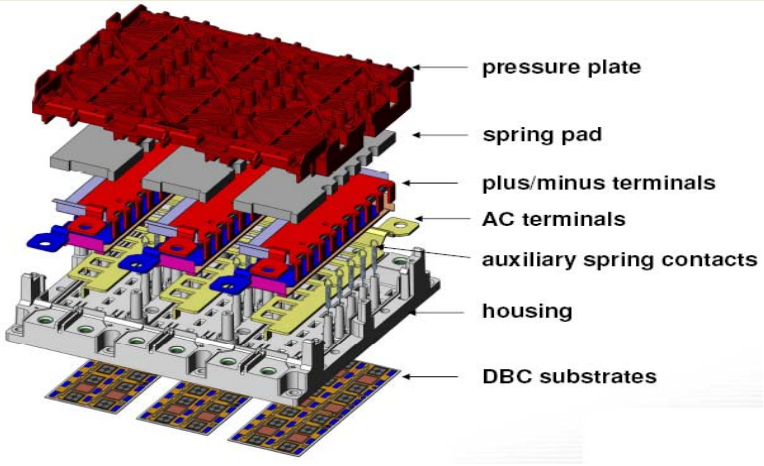


Figure 1-9. SKiM power module from Semikron [31] (Used under fair use guidelines, 2011).

In these modules, the sintering technique for the die-attach layer and the pressure contact for the interconnection of the top terminals of the power devices can significantly improve reliability of the power modules. However, the pressure contact technique requires delicate mechanical design and process, which may increase the cost of the

power module and complexity of the process. In addition, the double-sided cooling cannot be applied for these power modules.

1.2.7. Copper Plate-Bonded Power Module

Copper plate-bonded power module has similar structure with the Metal Post Interconnected-Parallel Plate Structure (MPIPPS) proposed by CPES in [32]. As shown in Figure 1-10, this structure was used in the power module for Lexus hybrid electric vehicle [6]. Instead of using multiple copper posts, a copper plate is inserted between the dice and the substrate to achieve better thermal and electrical performances. The power semiconductor dice are die-attached to the bottom substrate and then bonded to the top substrate via copper plates. In Lexus, the copper plates are used to improve the dielectric performance of the power module and also to compensate the height different of the IGBT dice and the diode dice. There are three bonding layers existing in the power module and labeled as solder layers in Figure 1-10. With large thickness, the copper plate also serves as thermal mass to reduce the peak transient temperature. The double-sided cooling technique can be implemented since the heat is dissipated almost equally from both sides of the power module. Thanks to the large bonding area of the copper plate, the plate-bonded power module also can carry high current.

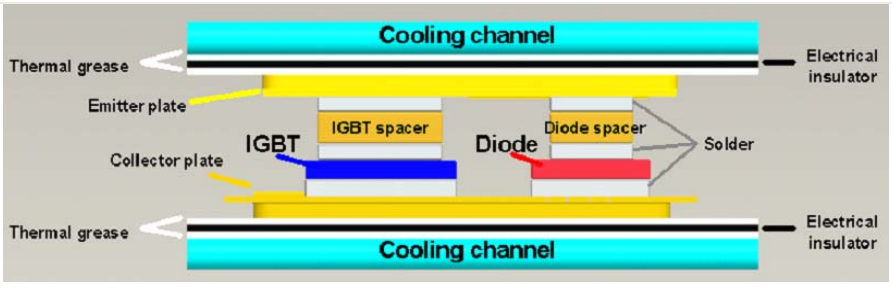


Figure 1-10. Plate-bonded module in Lexus [6] (Used under fair use guidelines, 2011).

Although the copper plate in the power module can significantly improve the transient thermal performance of the power module, it also induces large

thermo-mechanical stress due to large CTE mismatch between copper and silicon dice [10]. Therefore, the means that can reduce the thermo-mechanical stress in the power module have to be studied.

TABLE 1-1. COMPARISON OF THERMAL AND MECHANICAL PERFORMANCES FOR DIFFERENT PLANAR STRUCTURES

Structure	Double-Sided Cooling Capability	Transient Thermal Performance	Reliability
Dimple Array Interconnection (CPES)	No	Fair	Good
Flip-Chip on Flex Interconnection (CPES)	No	Poor	Good
Sandwich Structure (Denso)	Yes	Fair	Fair
Power Post/Bump Interconnection (CPES&Alstom)	Yes	Fair	Fair
SKiN Power Module (Semikron)	No	Poor	Good
Pressure Contact Techniques (Semikron)	No	Poor	Good
Plate-Bonded Power Module (Toyota)	Yes	Good	Poor

TABLE 1-1 compares the thermal and thermo-mechanical performances of different planar structures. In this table, the transient thermal performances of the planar structures are also discussed. The transient thermal performance of the power module is determined by amount of thermal mass. Since copper and aluminum have large thermal capacitance, the structures that have thick copper or aluminum layers such as plate-bonded module, and power bump structure will have better transient thermal performance than other structures. The plate-bonded module has the best thermal performance since there is a thick copper plate inserted to add thermal mass and bonding area. In addition, unlike the power bump module that requires many copper cylinders to connect dice and the top substrate, the plate-bonded module requires only one copper plate, which can significantly simplify the process. However, the reliability of the plate-bonded power module is poor due to the large thermo-mechanical stress induced by the CTE mismatch.

1.3. Significance and Objectives of This Study

Thermal design of the power module becomes more and more critical for high density integration. Therefore, in this dissertation, several issues related to thermal design are addressed. In [36]-[37], it is found that the conventional compact thermal model are usually independent of boundary conditions, rendering these models ineffective in predicting the transient temperature of the thermal stacks as a function of heat-transfer coefficients. In this dissertation, a boundary-dependent circuit model for transient thermal behavior of a power module is proposed. In the proposed model, the thermal resistances and capacitances depend on the material properties and dimensions of the thermal layers, as well as the heat-transfer coefficient of the boundary. Only steady-state FEM simulation is needed to extract the model parameters, which can significantly reduce the computing time for model extraction.

This dissertation also presents a method to measure thermal impedance of the power module using the gate-emitter voltage of an IGBT as the temperature sensitive parameter. Compared to the forward voltage drop of a pn junction, the gate-emitter voltage of an

IGBT is more sensitive to temperature change, leading to more accurate measurement results. The bonding quality of three different die-attach materials were compared using the thermal impedance measurement results. Results show that the nano-silver bonding has lower thermal impedance and better reliability than SAC305 and SN100C solders.

As discussed in Section 1.2, the structure shown in Figure 1-10 has superior thermal performance, especially for transient thermal performance. This makes it a good candidate for high density power module. However, the copper plate also induces large thermo-mechanical stress in the power module due to large coefficient of temperature expansion (CTE) mismatch between copper and silicon, leading to poor reliability [10][38].

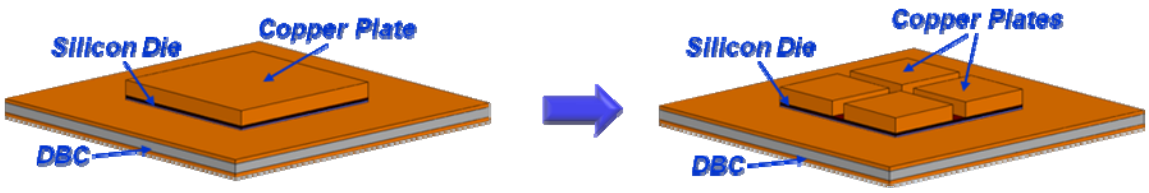


Figure 1-11. Reduce thermo-mechanical stress by partitioning the copper plate to smaller pieces.

In this dissertation, one effective way to reduce the thermo-mechanical stress was proposed. In the proposed method, the large piece of copper plate has to be partitioned into several smaller pieces so that the footprint area of a single copper plate is reduced as shown in Figure 1-11. However, due to the gaps among the smaller plates, the total thermal mass and the thermal conduction area of the power module will be slightly reduced, resulting in minor degradation in the thermal performance. Increasing the number of copper plates and reducing the footprint area for single copper plate decreases the maximum thermo-mechanical stress, but increase junction temperature of the silicon dice as shown in Figure 1-12. Thus, a trade-off between the thermo-mechanical reliability and the thermal performance has to be made.

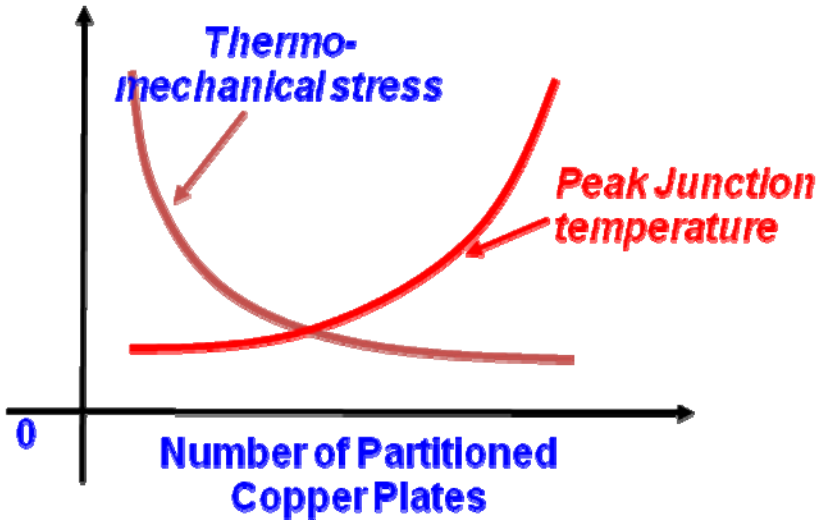


Figure 1-12. Trade-off between the thermo-mechanical performance and thermal performance of the power module.

1.4. Outline of Dissertation

This dissertation focuses on solving thermal-related issues in the power module and target to design a planar power module with low thermal impedance and low thermo-mechanical stress.

In Chapter 2, a boundary-dependent steady-state thermal model is proposed. In the proposed model, each layer in the power module is modeled as a thermal resistor. The resistance value is determined by the material properties of the layer and the effective heat spreading area that is a function of the footprint area of the power module, thickness of the heat-spreader, and the heat transfer coefficient of the heat-exchanger. Thus, it can be seen that different from the conventional compact thermal models, the boundary conditions and geometries of the power module are taken into account for calculating thermal resistance in the proposed model. The relation between the effective spreading area of the heat and the parameters mentioned above are established using response surface method. The proposed model is verified using finite element simulation. It shows that compared to the conventional thermal model based on 45˚ heat spreading angle, the

proposed model can provide more accurate prediction of the thermal resistance of the power module.

In Chapter 3, the effective spreading area of the heat derived in Chapter 2 is used to calculate the thermal capacitance in the power module so that the transient thermal model can be built. The transient thermal model derived can achieve better fitting with the results from finite element simulation than the thermal model based on 45˚ heat spreading angle. Therefore, the derived transient thermal model is used in coupled electro-thermal simulation for a buck converter to estimate the peak junction temperature during load change. The detailed steps to perform the coupled electro-thermal simulation are also described in this chapter. It can be seen that without the coupled electro-thermal simulation, the peak junction temperature of the silicon IGBT is under-estimated or over-estimated by more than 15˚C.

In Chapter 4, a measurement system for thermal impedance is developed. Thanks to its high temperature sensitivity (10mV/˚C), the gate-emitter voltage of an IGBT is used as the temperature-sensitive parameter. The power dissipation in the IGBT remains constant by a feedback loop, regardless of the junction temperature. Since a die-attach layer has significant impact on the thermal performance of a power module, its quality can be characterized using the developed thermal impedance measurement system. Experimental results show that the thermal impedance of the samples using different die-attach materials can be differentiated by the measurement system. The sample using sintered nano-silver for the die-attach has a 12.1% lower thermal impedance than the samples using SAC305 and SN100C solders. To check the degradation of the die-attachment, three samples using three die-attach materials were thermally cycled from -40˚C to 125˚C. The experimental results showed that after 500 cycles, the thermal impedance of SAC305 samples and SN100C samples is increased by 12.8% and 15%, respectively, which is much higher than the sample using the sintered nano-silver for the die-attach (increased by 4.1%).

In Chapter 5, the steady-state and transient thermal performance of a conventional wirebonded power module are analyzed. It is found that with a heat-exchanger having high heat transfer coefficient, the heat-spreader cannot effectively spread the heat to a larger area. Instead, it increases the thermal resistance and adds one interface layer in the vertical direction. Thus, from steady-state thermal performance point of view, the heat-spreader should be eliminated. However, the heat-spreader also serves as thermal mass for thermal transient. Removal of the heat-spreader results in degradation of the transient thermal performance. This shows that the conventional wirebonded power module cannot meet both steady-state and transient thermal requirements. To resolve this issue, a planar plate-bonded power module was proposed. In the proposed structure, the heat-spreader is eliminated to reduce the thermal resistance. However, a copper plate is attached on the top of the semiconductor device serving as thermal mass.

The plate-bonded power module can achieve both better steady-state and transient thermal performance than the wirebonded power module. However, the thick copper plate could induce large thermo-mechanical stress in the power module. The thermo-mechanical performance of the plate-bonded power module is investigated using ANSYS simulation in Chapter 6. To minimize the stress in the plate-bonded power module, the large piece of copper plate is replaced by trenched copper plate with 2 × 2 array or 3 × 3 array. By replacing the single copper plate with trenched copper plate, the maximum stress can be reduced by 18.7%. However, due to loss of thermal mass in the power module, the transient thermal performance of the copper plate-array power module degrades. The trade-off between the transient thermal performance and thermo-mechanical performance is also discussed in this chapter.

To verify the benefit brought by using trenched copper plate structure, twenty-four samples with three different structures were built and thermally cycled. The detailed experiment procedures are reported in Chapter 7. To detect the failure at the bonding layer, the curvatures of these samples are measured using laser scanning before and after

cycling. When cracks and delaminations occur at the bonding layer, the residual stress induced during thermal process can be released. As a result, the curvatures of the samples decrease. By monitoring the change of curvature, the degradation of bonding layer can be detected. Experimental results show that the samples with different copper plate structure have similar curvature before thermal cycle. The curvatures of the samples with single copper plate are reduced by more than 80% after only 100 cycles. For the samples with 2 × 2 trenched copper plates and 3 × 3 trenched copper plates, the curvatures are only reduced by 24.2% and 22.5%, respectively, indicating better reliability than the samples with single copper plate. The x-ray pictures of cross-sectioned samples further confirms the better reliability of trenched copper plate samples.

Chapter 2. A BOUNDARY-DEPENDENT STEADY-STATE THERMAL EQUIVALENT CIRCUIT FOR POWER MODULE

This chapter presents a complete analysis of steady-state thermal equivalent circuit of the power module. Several widely-used thermal equivalent circuits for the power module are reviewed and compared in this chapter. A boundary-dependent model based on finite difference method and response surface method was proposed. Figure 2-1 shows the stack structure for thermal management of a typical power module. The IGBT is attached to a direct-bonded-copper (DBC) substrate via solder. The heat-spreader underneath the DBC substrate can reduce the thermal resistance by spreading the heat over a larger cross-section. The whole power module is attached to the heat-exchanger via thermal interface materials (TIM), such as thermally conductive epoxy, solder, or thermal grease. As shown in Figure 2-2, the heat transfer coefficient of the heat-exchanger can vary from 10 $W/m^2/°C$ to 10^5 $W/m^2/°C$, depending on the convection mechanisms [1].

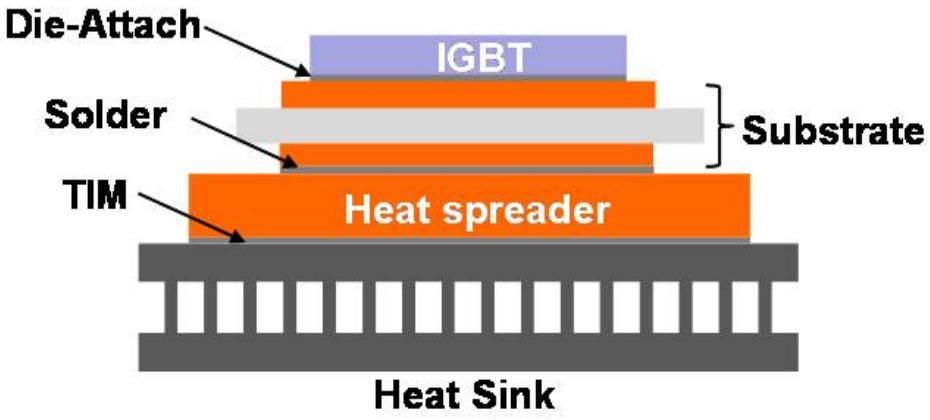


Figure 2-1. Structure for conventional power module with heat exchanger.

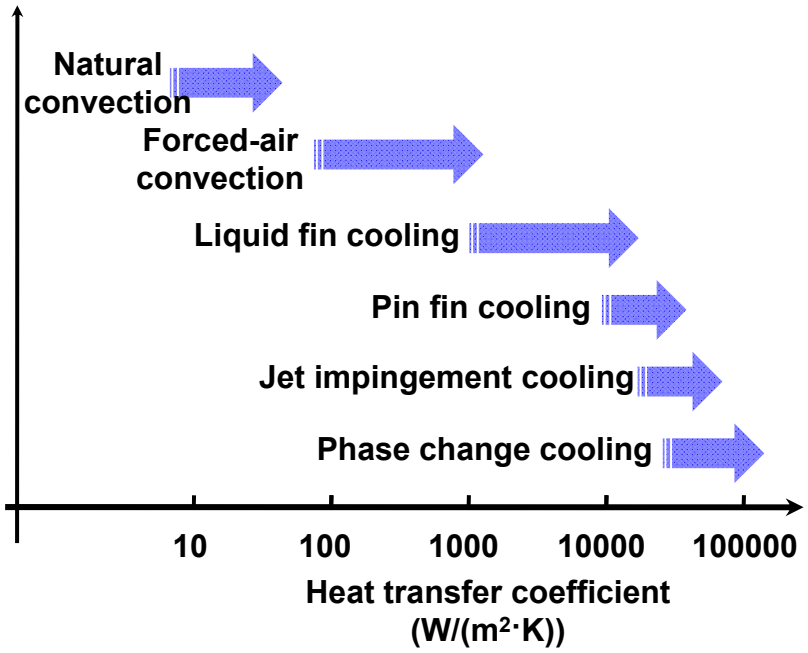


Figure 2-2. Heat transfer coefficients for different cooling mechanisms.

2.1. Review of Literature

2.1.1. Thermal Models Independent of Boundary Condition

Many compact thermal models have been proposed in literatures to describe the power module shown in Figure 2-2 [40]-[47]. In most compact thermal models, each layer in the power module is modeled as the combination of resistor and capacitor. Foster RC network and Cauer RC network shown in Figure 2-3 are most widely used thermal models. The

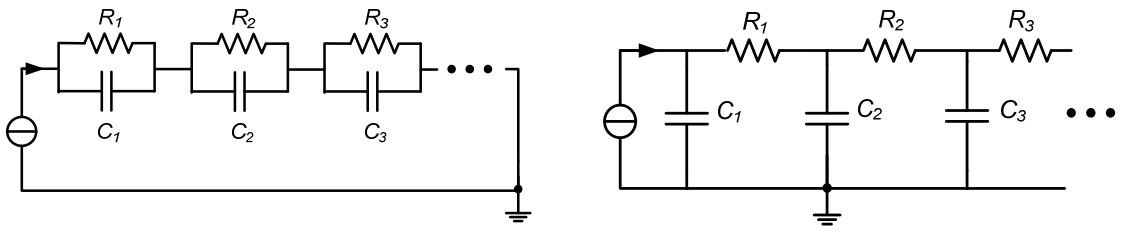
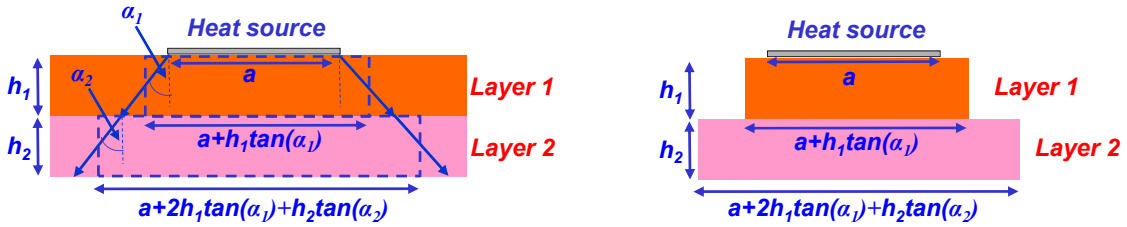


Figure 2-3. Foster (a) and Cauer (b) thermal networks.

values for RC can be extracted from the dimensions of the power module and the properties of the materials used [40]-[43].

Some compact thermal models were proposed based on solving partial differential equations of heat transfer. In [41]-[47], a thermal model was proposed based on a finite difference discretization of the heat transfer equation. In this type of models, the heat spreading effect in the power module is described by a heat spreading angle (as shown in Figure 2-4). In [1], an empirical heat spreading angle of 45˚ is employed. Figure 2-5 shows the comparison of thermal resistances obtained from the FEM simulation and obtained from the thermal model based on 45˚ heat spreading angle. It can be seen that a large discrepancy exists, especially for the cases with low heat transfer coefficient. In [41]-[43], the heat is assumed to cylindrically spread along the edges of the heat source and spherically spread at the corners of the heat source. In [45][47], the heat spreading angle is not constant and it depends on the material properties of different layers. In the layer with higher thermal conductivity, the heat can spread more. However, for all these models, the heat conduction within the power module is independent of the heat transfer coefficient of the power module. In [46], the heat-spreading angle of a single layer structure (shown in Figure 2-7(a)) was calculated and shown in Figure 2-7(b). It can be seen that the heat spreading angle increases when the thickness of the substrate increases. The heat spreading angle of 45˚ is only valid with thick substrate ($t_s/a > 2$).

Figure 2-8 shows the distribution of the heat flux in a power module under different heat transfer coefficients. It can be seen that with higher heat transfer coefficient, the heat tends to dissipate into the ambient via the vertical path, leading to smaller spreading effect. This shows that the heat spreading effect of the power module is not constant. Instead, it varies with the geometries of the power module and the boundary conditions. Thus, the heat transfer coefficient should be taken into account in the modeling of the power module.



(a) (b)

Figure 2-4. Heat spreading angle in the power module is shown in (a); the calculation of the effective area for heat spreading based on the heat spreading angle is shown in (b).

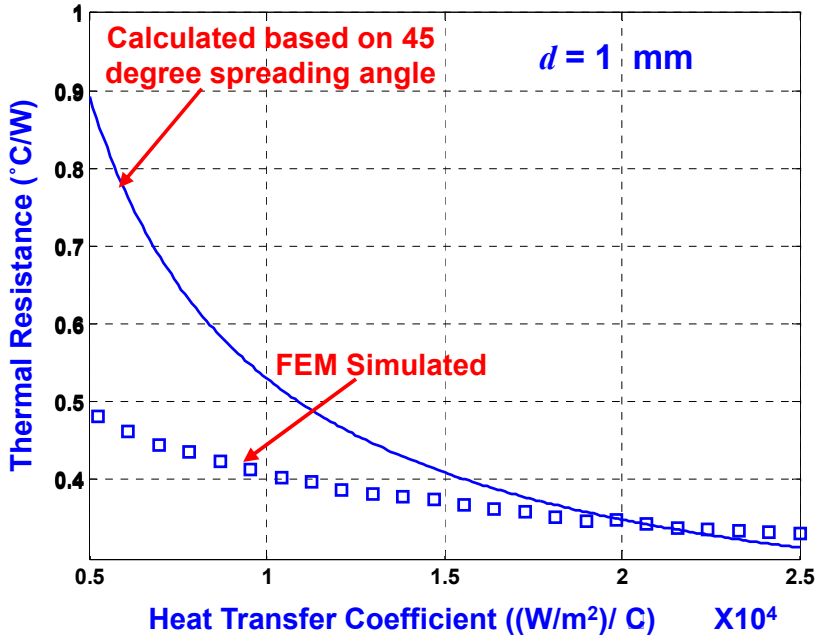


Figure 2-5. Comparison of thermal resistances obtained from FEM simulation and 45° spreading thermal model (structure used in simulation shown in Figure 2-6; material properties and boundary conditions used in simulation shown in TABLE 2-1 and TABLE 2-2).

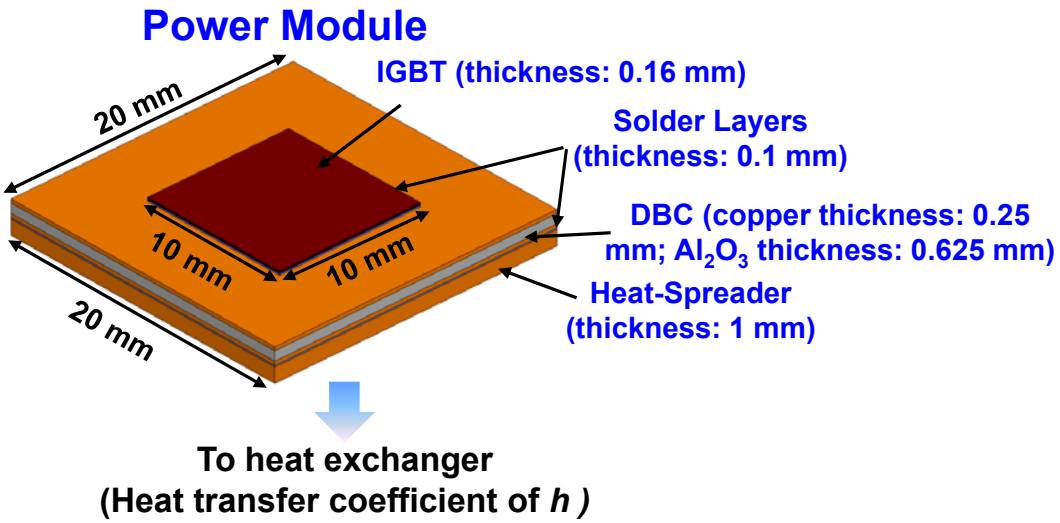


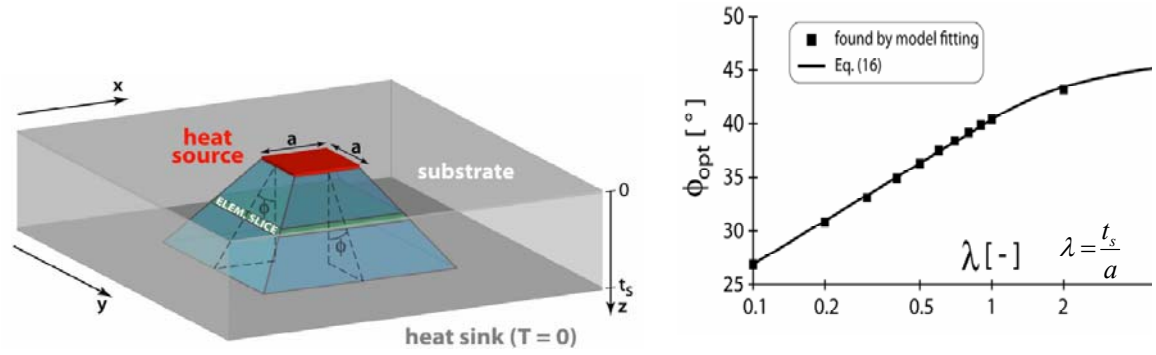
Figure 2-6. Structure used for finite element simulation in Figure 2-5.

TABLE 2-1. MATERIAL PROPERTIES USED IN THE SIMULATION

	Thermal Conductivity k	Specific Heat Capacity c	Mass Density ρ
Copper	400 $W/(m \cdot C)$	385 $J/(kg \cdot C)$	8933 kg/m^3
Alumina in DBC	35 $W/(m \cdot C)$	850 $J/(kg \cdot C)$	3960 kg/m^3
IGBT	148 $W/(m \cdot C)$	712 $J/(kg \cdot C)$	2330 kg/m^3
Solder	48 $W/(m \cdot C)$	167 $J/(kg \cdot C)$	8000 kg/m^3

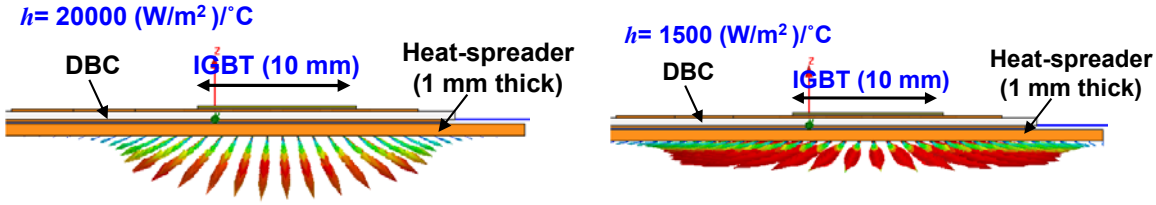
TABLE 2-2. BOUNDARY CONDITIONS AND DIMENSIONS USED IN SIMULATION SHOWN IN FIGURE 2-5

	Value
Ambient Temperature (°C)	25
Heat Transfer Coefficient ($(W/m^2)/ °C$)	From 5000 to 25000
Power Loss in IGBT	200 W



(a) (b)

Figure 2-7. Heat spreading effect in single layer structure [46] (a) structure used in the study; (b) heat-spreading angle vs normalized thickness of substrate.



(a) (b)

Figure 2-8. Heat flux distribution in a power module (a) with heat transfer coefficient of 20000 W/m^2/°C and (b) with heat transfer coefficient of 1500 W/m^2/°C (material properties and boundary conditions used in simulation shown in TABLE 2-1 and TABLE 2-3).

TABLE 2-3. BOUNDARY CONDITIONS AND DIMENSIONS USED IN SIMULATION SHOWN IN FIGURE 2-8

	Value
Ambient Temperature (°C)	25
Heat Transfer Coefficient ((W/m^2)/ °C)	20000 or 1500
Power Loss in IGBT	200 W

2.1.2. Thermal Models Dependent on Boundary Conditions

Another type of thermal models was proposed based on the solution of the heat conduction equations [49]-[52]. In [49], the exact solution of steady-state temperature distribution for a multilayer power module was derived. However, in this model, the temperature at the bottom surface of the power module is considered to equal to the ambient temperature. In other words, the heat transfer coefficient is assumed to be infinite, which is not true for most power electronics systems. Finite element method (FEM) is widely used to solve the heat conduction equations in a numerical way. As a result, a thermal model was developed based on solving the heat conduction equations using FEM [50]-[51]. In this model, the entire power module is divided into many small "elements". Each element can be modeled as the combination of the thermal resistance and capacitance networks. This model can be applied to all kinds of boundary conditions and provide accurate results. However, due to the large number of elements, it is very difficult to use for geometry design and optimization of the power module. A simple closed-form solution for the steady-state temperature distribution of a stacked structure was proposed in [52]. However, this solution can only be applied to a simple structure in which a heat source is placed on the top of a substrate. The vertical lay-up of the power module is much more complicated, and many layers such as substrates, heat-spreaders, and die-attach layers may have significantly impact on the thermal performance of the power module.

2.2. Steady-State Boundary-Dependent Model of Power Module

2.2.1. Selection of Input Variables for Thermal Model

The compact thermal model shown in Figure 2-13 has many advantages such as easy to use, have clear physical meaning, and can be extracted directly from the geometries and material properties of the power module. Thanks to these properties, the thermal model is suitable for optimization of the thermal design and coupled electro-thermal

simulation. In this section, several very important parameters of the power module were selected as input variables for the thermal model.

The thermal performance of a typical power module shown in Figure 2-9 (the cross-section was shown in Figure 2-1) can be impacted by many factors:

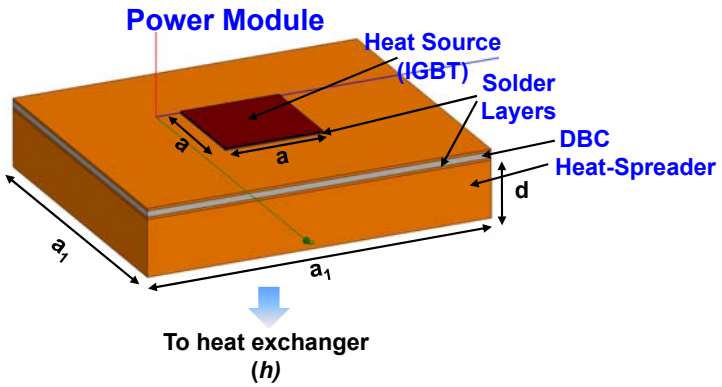


Figure 2-9. The parameters used for optimization of the power module (*d*: 1 - 5 mm; a_1: 12 – 28 mm; h: 10000 – 50000 W/(m^2·C)).

1. Materials

The heat generated in the power module has to pass through many layers before it dissipates in the ambient. As a result, the material properties of these layers have significant impact on the thermal performance. For substrates in the power module, direct-bonded-copper (DBC) substrate and direct-bonded-aluminum (DBA) substrate are widely used. Generally speaking, DBC substrate has better thermal performance than DBA substrate due to high thermal conductivity of copper. The ceramics used in the substrate contribute a large portion in the total thermal resistance of the substrate. As a results, the substrate employed ceramic with higher thermal conductivity such as AlN (150 W/(m·K)) and BeO (230 W/(m·K)) can achieve better thermal performance. However, this could result in higher cost and more complicated process (BeO is a toxic material) [55]. The most common materials for the heat-spreader are copper and aluminum. Copper has high thermal conductivity and large thermal mass that makes it perfect for heat-spreader. Compared to copper, aluminum has lower thermal conductivity and less thermal mass. However, it is much lighter than copper which makes it suitable for weight sensitive

applications such as power modules for aircrafts. The selection of die-attach material and thermal interface material also can impact the thermal performance of the power module [55][56]. To reduce the thermal resistance in the power module, die-attach and thermal interface materials with higher thermal conductivity and better reliability are desired.

2. Geometries

The structures of the power module such as footprint area and thickness of the heat-spreader also play a very important role in thermal performance. In general, larger footprint area helps to increase area for heat spreading, leading to lower thermal resistance. However, the large footprint area also reduces the power density and increases the cost of the power module. Therefore, a trade-off has to be made between the thermal performance and the power density when the footprint area of the power module is designed. The thickness of the heat-spreader also shows two opposite impacts on the thermal performance of the power module. On one hand, thicker heat-spreader can reduce the thermal resistance of the power module by spreading the heat to a larger area. On the other hand, thicker heat-spreader indeed increases the thermal resistance in the vertical direction. Thus, the thickness of the heat-spreader has to be optimized to minimize the overall thermal resistance of the power module.

3. Performance of the heat-exchanger

The cooler with higher heat transfer coefficient can help to improve thermal performance of the power module. However, it usually requires complicated cooling mechanism and leads to higher manufacturing cost and more complicated fabrication process. Therefore, based on the thermal requirement of the power module, selecting the cooler with proper transfer coefficient to avoid overdesign is critical.

From the above discussion, it can be seen that the selection of materials are often constrained by factors such as cost, reliability, process, weight, etc. Within these constraints, the materials that have high thermal conductivity are preferred in the power module. Thus, this study focus on the geometry of the power module (the footprint area of

the power module, the thickness of the heat-spreader) and the selection of the heat transfer coefficient.

Three parameters under investigation can be normalized as follows:

$$r' = \frac{a_1}{a} \tag{2-1}$$

$$d' = \frac{d}{a} \tag{2-2}$$

$$h' = \frac{hT_a}{\Phi} \tag{2-3}$$

The sizes of the heat source (IGBT die) and the footprint area are described by a^2 and a_1^2, respectively (shown in Figure 2-9). In this study, the size of the IGBT is assumed to be 1 cm^2 which is typical for medium power application. The thickness of the heat-spreader is d. The heat transfer coefficient at the bottom of the power module is h that can be normalized using heat flux (Φ) and ambient temperature (T_a). In this study, the ambient temperature is set to be 25˚C. It should be noticed that the ambient temperature could be higher than 25˚C for some applications. However, the ambient temperature will not impact the thermal resistance/impedance and temperature rise of the power module. Therefore, the methodology of modeling and the results derived based on 25˚C are also valid for the cases with other ambient temperatures. For the power module in the power level from 10 kW to 100 kW, the ranges of the parameters used in the study are shown in TABLE 2-4.

TABLE 2-4. PARAMETERS AND THEIR RANGES USED IN THE STUDY

(T_a = 25˚C; Φ = 200 W/cm^2; a = 1 cm)

	a_1 (cm)	d (mm)	h (W/(m^2·C))	r'	d'	h'
Minimum	1.2	1	10000	1.2	0.1	1250
Maximum	2.8	5	50000	2.8	0.5	6250

2.2.2. Set-Up for Thermal Simulation

To build and verify the boundary-dependent thermal model for the power module, thermal simulation is required. Thus, finite-element ePhysics from Ansoft [53] is used herein to study how the heat propagates from the junction to the heat exchanger under steady state and transient conditions. EPhysics' ability to refine the mesh adaptively allows trade-off between numerical accuracy and computation time. The detailed steps for thermal simulation using ePhysics are presented in Appendix A.

Before a simulation, a three-dimensional (3D) model of the power module is built in ePhysics as shown in Figure 2-9. To avoid hot spots, sufficient distance should be allocated among neighboring dice to minimize thermal interaction. The minimal distance should be larger than $2d\cdot\tan(\alpha)$, where α is the heat spreading angle and d is the thickness of the heat spreader d. As discussed in Section 2.1, for the power modules with high heat transfer coefficient, the heat spreading angle is small, leading to smaller distance among dice. Without thermal interaction among neighboring dice, it suffices to consider a module with one die herein. The methodology is still applicable to a module with multiple dice.

The DBC substrate used in Figure 2-9 has an alumina layer with a thickness of 0.625 mm sandwiched between copper layers with a thickness of 0.25 mm. The solder layer has a thickness of 0.1 mm. The IGBT area is 1 cm^2 and is modeled with the thermal properties of silicon. The material properties used in the simulation are listed in Table 2-1.

For the medium-voltage power module considered herein, heat is convected away primarily by a heat-exchanger mounted to the bottom of the power module. Therefore, the major part of the heat generated in the IGBT is transported via conduction to the bottom of the power module, and is then dissipated with a heat transfer coefficient h. The top and lateral surfaces of the power module can be considered adiabatic.

In the power module shown in Figure 2-9, the shapes of the IGBT as well as the whole module are assumed to be square, which is not the case for the many power modules. However, the study shows that the thermal impedance of the power module is a

weak function of its shape [57]-[58]. Figure 2-10 shows the power modules with three different footprint shapes for the heat sources: square, rectangular with aspect ratio of 2, and round. For these three cases, the ratios of the footprint areas of the heat source and the power module are maintained to be same. The thermal resistances of the power modules with different shapes for the heat sources under various conditions are shown in Figure 2-11. It can be seen that the thermal resistance of the power module changes less than 2% when the shape of the heat source changes from square to round. Thus, the study results based on the square heat source can be applied to the heat sources that have different shapes but same footprint area.

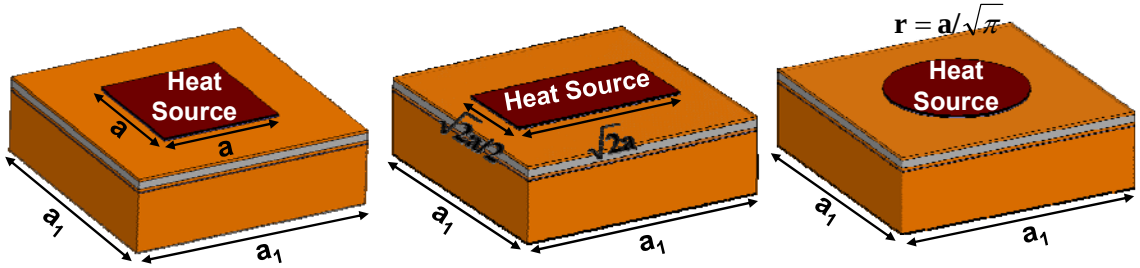


Figure 2-10. The power modules with different shapes for the heat sources.

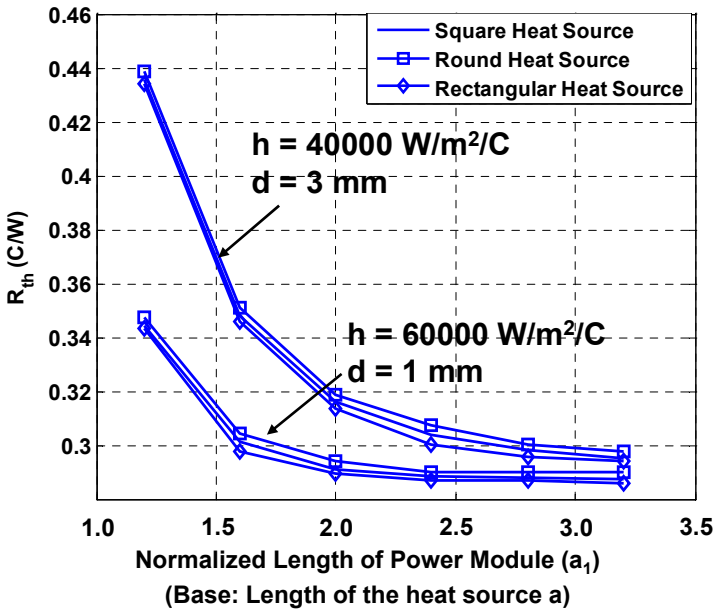


Figure 2-11. Simulated R_{th} of the power module with different shapes for the heat sources (a = 10 mm; material properties and boundary conditions used in simulation shown in TABLE 2-1 and TABLE 2-5).

TABLE 2-5. BOUNDARY CONDITIONS IN SIMULATION SHOWN IN FIGURE 2-11

	Value
Ambient Temperature (°C)	25
Heat Transfer Coefficient ((W/m^2)/ °C)	40000 or 60000
Power Loss in IGBT	200 W

2.2.3. Thermal Model Based on Finite Difference Method

For vertical power device, the semiconductor pn junction region, where the most of the heat is generated, is close to the top surface of the silicon chip. Thus, it can be assumed that the electrical power loss is imported from the top surface of the chip. The electrical power loss is treated as the first boundary condition in the thermal problem. The lower surface of the power module, where the heat-exchanger system is installed, is treated as the second boundary condition. The thermal system then can be described by the partial differential equation [44]

$$k \cdot \nabla^2 T + g = \rho \cdot c_p \frac{\partial T}{\partial t} \tag{2-4}$$

with the boundary conditions

$$k \frac{\partial T}{\partial n} = \frac{P}{A} \tag{2-5}$$

on the top surface of the power device and

$$k \frac{\partial T}{\partial n} = h(T - T_a) \tag{2-6}$$

at the bottom surface of the power module. In the above equations, the nomenclature definition is shown as follows:

k: Thermal conductivity (W/(°C·m))

c_p: Specific heat (J/(kg·°C))

h: Heat transfer coefficient (W/m^2)

ρ: Mass density (kg/m^3)

T: Temperature (°C)

P: Power dissipation (W)

T_a: Ambient temperature (°C)

x: Length in heat transfer direction (m)

n: Outward normal vector to the boundary *A:* Effective area of heat transfer (m^2)

g: Generating heat (W/m^3)

Considering the thermal system in Figure 2-12(a), the internal generating heat is zero ($g = 0$). At node i, the discretization of equation (2-4) with a constant step Δx gives the following equation:

$$\frac{T_{i+1}(t)+T_{i-1}(t)-2T_i(t)}{\Delta x^2}=\frac{\rho\cdot c_p}{k}\frac{dT_i(t)}{dt} \tag{2-7}$$

where T_i is the temperature at node i.

With the discretization, the boundary condition in equation (2-5) can be obtained:

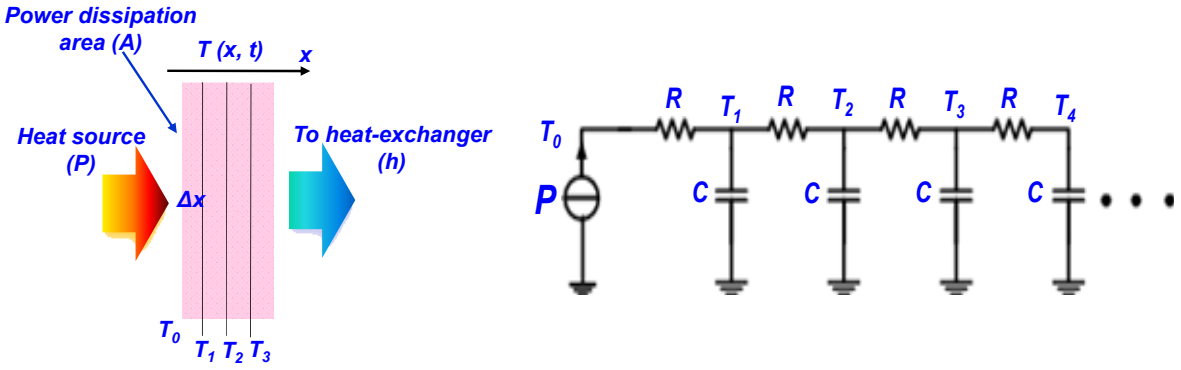
$$\frac{T_1(t)-T_0(t)}{\Delta x}=\frac{P}{k\cdot A} \tag{2-8}$$

From equations (2-7) and (2-8), the thermal model of can be derived as shown in Figure 2-12(b). It should be noted that in Figure 2-12(b), T_i refers to the voltage at node i and P is the current source. From Figure 2-12(b), the nodal equation can be written as:

$$\frac{T_{i+1}(t)+T_{i-1}(t)-2T_i(t)}{R}=C\frac{dT_i(t)}{dt} \tag{2-9}$$

At node 0, the following equation can be obtained:

$$\frac{T_1(t)-T_0(t)}{R}=P \tag{2-10}$$



(a) (b)

Figure 2-12. Heat transfer in a multi-layer structure (a) and the FDM model for the structure (b).

Comparing the equations (2-7), (2-8) and (2-9), (2-10), the parameters R and C in Figure 2-12(b) can be calculated:

$$R = \frac{\Delta x}{k \cdot A} \quad \text{and} \quad C = \rho \cdot c_p \cdot \Delta x \cdot A \tag{2-11}$$

Since the components in the power module are thin layers, each component (layer) can be considered as a "discretizd element" in Figure 2-12(a). Therefore, the thermal model of a typical power module shown in Figure 2-1 can be described as in Figure 2-13. The values of the resistor and the capacitor can be calculated as

$$R_i = \frac{d_i}{k_i A_i} \tag{2-12}$$

$$C_i = \rho_i \cdot c_{pi} \cdot d_i \cdot A_i \tag{2-13}$$

where ρ_i, c_{pi}, and d_i are the density, specific heat capacity, and thickness of the i^{th} layer. A_i is the effective heat spreading area in the layer. The heat-exchanger with the heat transfer coefficient of h is also considered to be a resistor (R_9 in Figure 2-13). The resistance can be calculated based on the definition of the heat transfer coefficient.

$$R_9 = \frac{1}{hA_9} \tag{2-14}$$

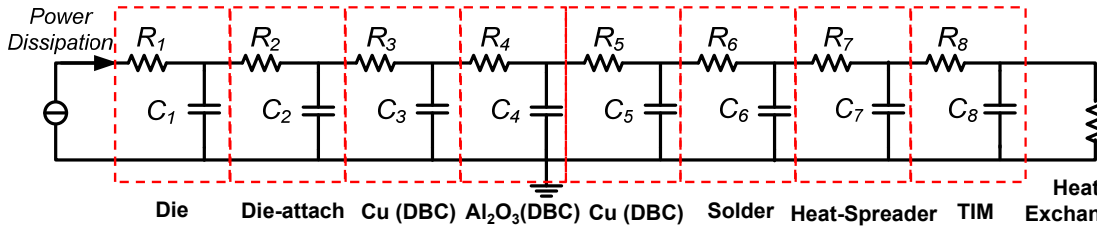


Figure 2-13. The thermal model based on finite difference method (FDM) of the power module shown in Figure 2-1.

2.2.4. Boundary-Dependent Steady-State Thermal Model for the Power Module

Under steady-state situation, the thermal model of the power module can be obtained by eliminating the thermal capacitors in the model shown in Figure 2-13. As shown in Figure 2-14, each layer in the power module can be modeled as one thermal resistor and

all the resistors are in series. As discussed before, the resistance for each layer is dependent on thermal conductivity of the material, the thickness of the heat-spreader, heat transfer coefficient of the heat-exchanger, and the effective heat spreading area of the layer.

However, the contribution from each layer to the total thermal resistance is different. For instant, the copper layers of DBC are very thin and also have very good thermal conductivity. As a result, the thermal resistance from DBC is dominant by the ceramic layer and the copper layers of DBC can be ignored when calculating the thermal resistance of the power module. Figure 2-15 and TABLE 2-6 show the breakdown of thermal resistance from each layer in the power module which further confirms that the copper layers from the DBC only contribute less than 2% to the total thermal resistance of the power module. Therefore, the thermal model shown in Figure 2-14 can be further simplified to be as shown in Figure 2-16.

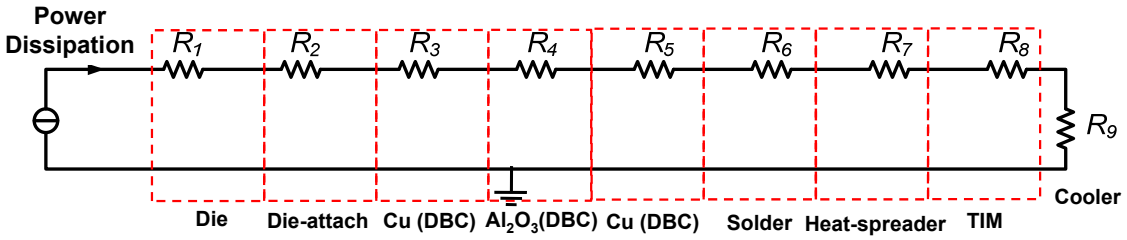


Figure 2-14. The steady-state thermal model for the power module.

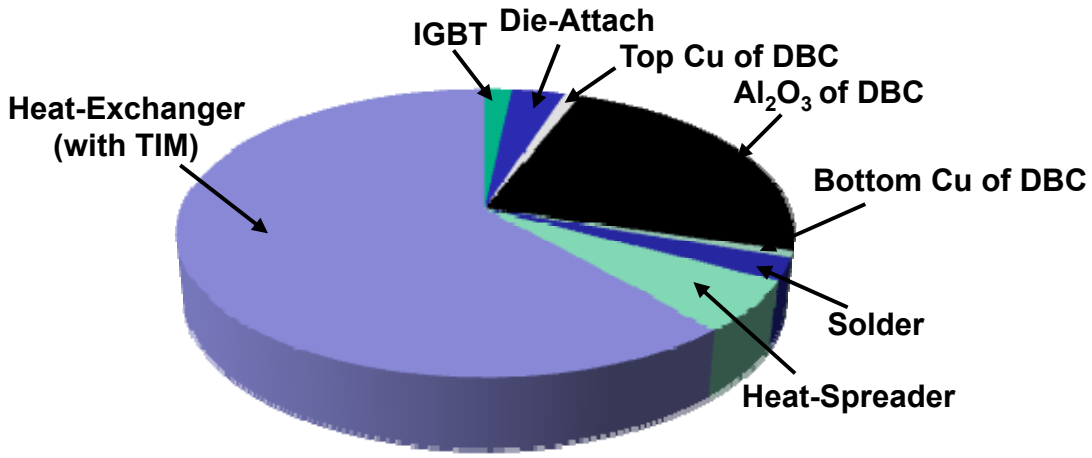


Figure 2-15. The breakdown of thermal resistance from each layer in the power module.

TABLE 2-6. CONTRIBUTION TO R_{TH} FROM EACH LAYER

Layer	R_{th} (˚C/W)	Percentage
IGBT	**0.0109**	**1.7%**
Die-attach	**0.0203**	**3.2%**
Top Cu of DBC	**0.0062**	**1.0%**
Al_2O_3 of DBC	**0.1499**	**23.7%**
Bottom Cu of DBC	**0.0045**	**0.7%**
Solder	**0.0159**	**2.5%**
Heat Spreader	**0.0361**	**5.7%**
Cooler (with TIM)	**0.3893**	**61.5%**
Total:	**0.6332**	**-**

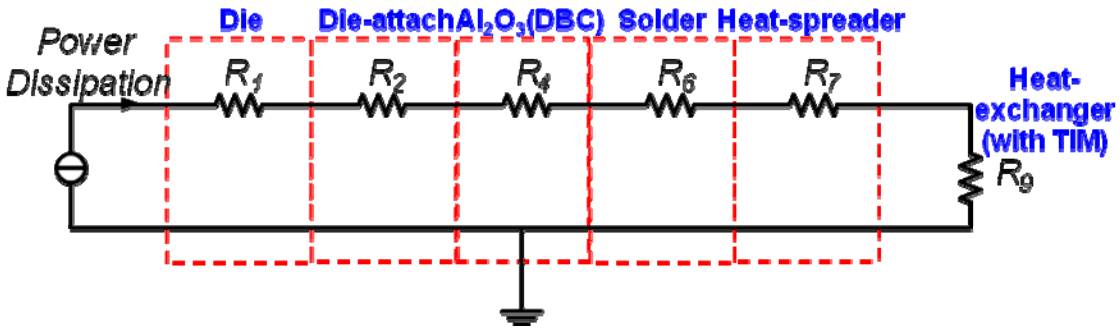


Figure 2-16. The simplified steady-state thermal model for the power module.

$$R_i = \frac{d_i}{k_i A_i} \qquad i = 1,\quad 2,\quad 4,\quad 6,\quad 7 \tag{2-15}$$

$$R_9 = \frac{1}{h \cdot A_9} \tag{2-16}$$

$$R_{th} = \sum_{i=1}^{9} R_i \tag{2-17}$$

As discussed in Section 2.1.1, the heat spreading area in the power module is the function of heat transfer coefficient, the thickness of the heat-spreader, and the footprint area of the power module. However, due to the complicated structure, it is difficult to derive the closed-form equation of the spreading effect in the power module. Therefore, in this study, a numerical method called response surface method is employed to explore the relation between the heat spreading area and the important parameters shown in TABLE 2-4. The diagram in Figure 2-17 shows the procedure to build the boundary-dependent thermal model for the power module. Firstly, a set of r_i', d_i', and h_i' are selected based on the range set in TABLE 2-4 and the principles of design for experiment. The steady-state thermal performance of the power module will be simulated using the selected data set. From the simulation, the thermal resistance of each layer in the power module (R_{i1}, R_{i2},…, R_{i5}) can be obtained. After that, a numerical thermal model can be built using response surface method based on the simulation results of each layer in the power module. The model is used to describe the relation between the effective heat spreading area and the important design variables (r', d', and h'). With the effective heat spreading area of each layer, the thermal resistance of each layer as well as the total thermal resistance of the power module can be calculated using equations (2-15), (2-16), and (2-17).

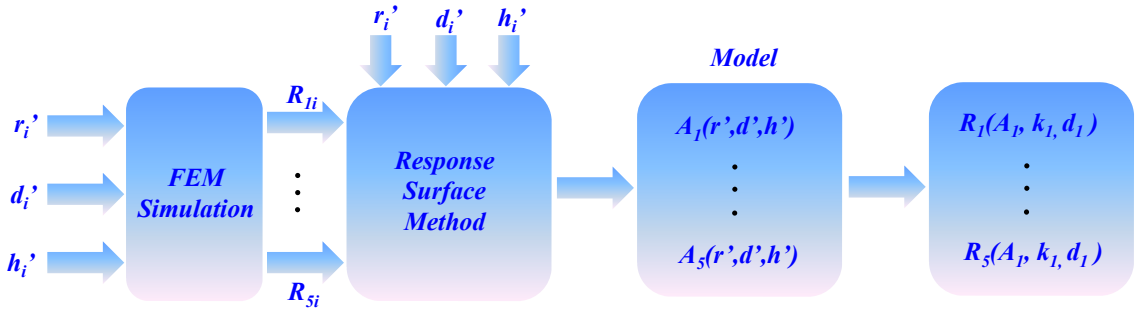


Figure 2-17. Build the thermal model for the power module using response surface method.

Response surface method (RSM) is a collection of statistical and mathematical techniques useful for developing model and optimizing design [59]. The performance measured or simulated is called the response. The important design variables (r', d', and h') are considered to be inputs for the model. In this case, the response is the simulated thermal

resistance (R_i) or effective heat spreading area (A_i) for the ith layer in the power module. The relation between the inputs and the response is

$$A_i = f_i(r_i^{'}, d_i^{'}, h_i^{'}) + \varepsilon \tag{2-18}$$

where the form of the true response function f_i is unknown and perhaps very complicated, and ε is a term that represents other sources of variability not accounted for in f_i. Since the true response function f is unknown, we must approximate it. Usually, a low-order polynomial in some relatively small region of the independent variable space is appropriate. Here, to model the curvature in the response, a second-order approximation as shown in (2-19) can be adopted.

$$\begin{aligned} A_i = A_0(&\alpha_{i0} + \alpha_{i1}r' + \alpha_{i2}d' + \alpha_{i3}h' + \alpha_{i4}r'^2 + \alpha_{i5}d'^2 + \alpha_{i6}h'^2 \\ &+ a_{i7}r'd' + a_{i8}r'h' + a_{i9}d'h') \end{aligned} \tag{2-19}$$

where A_0 is the footprint area of the heat source. The second-order model shown in (2-19) is very flexible. It contains not only the second-order effects from each input variable (main effects), but also the interactions among the input variables (the α_{i7}, α_{i8}, and α_{i9} terms).

To obtain the ten parameters (the α's in equation (2-19)) in the model, a series of simulation runs has to be designed. Factorial designs are widely used in model involving several factors where it is necessary to investigate the joint effects of the factors on a response variable. A common design is one with all input factors set at two levels each. These levels are called 'high' and 'low' or '+1' and '-1', respectively. A design with all possible high/low combinations of all the input factors is called a full factorial design in two levels. Therefore, for a system with three inputs, only eight runs ($2^3 = 8$) of simulation need to be performed. However, there are ten unknown parameters in equation (2-19). Thus, to obtain the accurate second-order model, the number of levels for each input can be increased to three. As a result, total 27 runs of simulations are required for three-input system. The three levels for each input are usually referred to as low, intermediate and high levels or numerically expressed as -1, 0, and 1. Based on the range of the inputs shown in

TABLE 2-4, the three levels can be set as TABLE 2-7. The matrix for three-level full factorial design is listed in TABLE 2-8.

TABLE 2-7. THREE LEVELS FOR THE INPUTS

	r′	*d′*	*h′*
Low (-1)	1.2	0.1	1250
Intermediate (0)	2.0	0.3	3750
High (+1)	2.8	0.5	6250

TABLE 2-8. DESIGN MATRIX FOR SIMULATION (THREE LEVEL FULL FACTORIAL)

Run	*r′*	*d′*	*h′*
1	-1	-1	-1
2	-1	-1	0
3	-1	-1	1
4	0	-1	-1
5	0	-1	0
6	0	-1	1
7	1	-1	-1
8	1	-1	0
9	1	-1	1
10	-1	0	-1
11	-1	0	0

12	-1	0	1
13	0	0	-1
14	0	0	0
15	0	0	1
16	1	0	-1
17	1	0	0
18	1	0	1
19	-1	1	-1
20	-1	1	0
21	-1	1	1
22	0	1	-1
23	0	1	0
24	0	1	1
25	1	1	-1
26	1	1	0
27	1	1	1

Before building the thermal model for the power module, the sensitivities of each factor in equation (2-19) to the thermal resistances were analyzed using JMP software from SAS [60]. Based on the results of sensitivity analysis, some terms in equation (2-19) that have minor contribution to the thermal resistance can be neglected so that the complexity

of the model can be reduced. The contrasts of the factors are widely used to identify which factors are likely to be important to the thermal resistance.

Figure 2-18 shows the sensitivity analysis results for thermal resistance of each layer. Since the silicon die has good thermal conductivity, the whole IGBT can be considered as heat source. The die-attach layer has the same footprint area as the IGBT. Therefore, for the IGBT and the die-attach layer, there is no heat spreading effect and the effective area is the same as the footprint area of the IGBT (equation (2-20)). For the rest of layers, the factors that have significant impact on the effective areas are highlighted. Based on the analysis result, the second-order approximation for each layer can be written in equations (2-21)-(2-24).

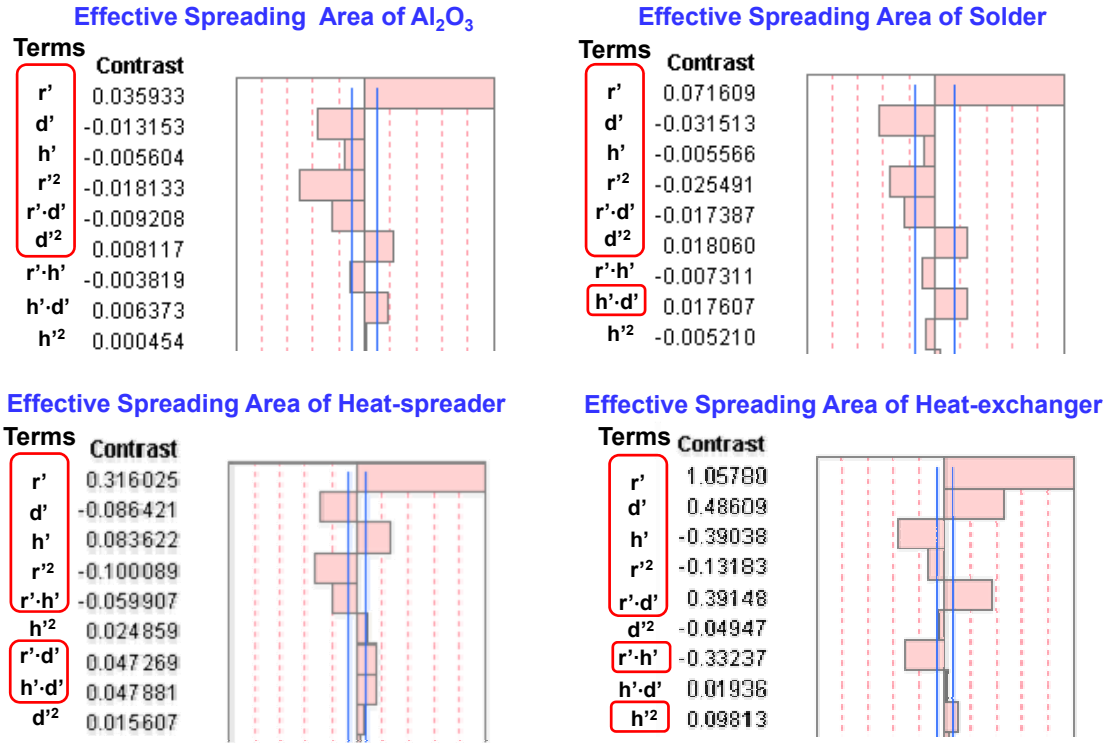


Figure 2-18. Sensitivity analysis on the optimization parameters ($1.2 \le r' \le 2.8$; $0.1 \le d' \le 0.5$; $1250 \le h' \le 6250$).

$$A_i = A_0 \ when \quad i = 1, \quad 2 \tag{2-20}$$

$$A_4 = A_0(\alpha_{40} + \alpha_{41}r' + \alpha_{42}h' + \alpha_{43}h_1' + \alpha_{44}r'^2 + \alpha_{45}r'h' + \alpha_{46}h'^2) \quad (2\text{-}21)$$

$$A_6 = A_0(\alpha_{60} + \alpha_{61}r' + \alpha_{62}h' + \alpha_{63}h_1' + \alpha_{64}r'^2 + \alpha_{65}r'h' + \alpha_{66}h'^2 + \alpha_{67}h'h_1') \quad (2\text{-}22)$$

$$A_7 = A_0(\alpha_{70} + \alpha_{71}r' + \alpha_{72}h' + \alpha_{73}h_1' + \alpha_{74}r'^2 + \alpha_{75}r'h' + \alpha_{76}r'h_1' + \alpha_{77}h'h_1') \quad (2\text{-}23)$$

$$A_9 = A_0(\alpha_{90} + \alpha_{91}r' + \alpha_{92}h' + \alpha_{93}h_1' + \alpha_{94}r'^2 + \alpha_{95}r'h' + \alpha_{96}r'h_1' + \alpha_{97}h_1'^2) \quad (2\text{-}24)$$

As shown in Figure 2-17, based on the steady-state simulation results of 27 runs, the coefficient of estimates in equations (2-21)-(2-24) can be obtained. The estimation of the coefficient is derived based on the least squares fitting. The method of least squares is a standard approach to obtain the approximated solution of overdetermined systems, in which the sets of equations are more than unknowns. "Least squares" means that the overall solution minimizes the sum of the squares of the errors made in solving every single equation [61]. TABLE 2-9 shows the thermal resistance obtained using the boundary-dependent thermal model. It can be seen that the maximum error between the thermal model and the FEM simulation is only 6.31%, which indicates that the proposed boundary-dependent model can be used to predict the thermal resistance of the power module.

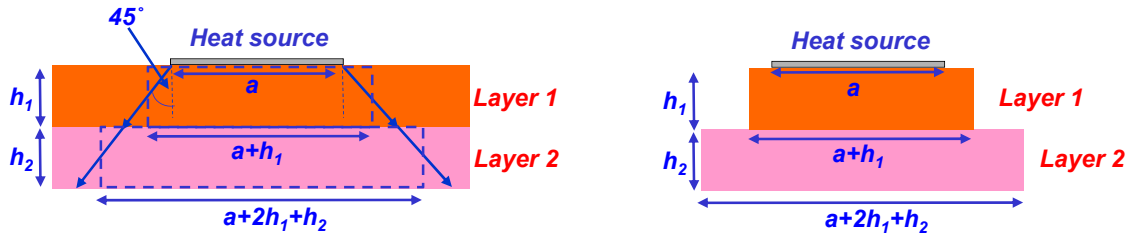
Another widely used thermal model is to assume that the heat spreads in the power module with the spreading angle of 45˚. As shown in Figure 2-19 (a), the heat transfer from the heat source with the length of *a* to the underneath layer with a fixed spreading angle of 45˚. As a result, the length of the effective spreading area of the underneath layer is increased to $a + h_1$ (shown in Figure 2-19 (b)). Similar spreading effect occurs for the rest of the layers. Based on this assumption, the thermal resistance of the power module was also calculated and listed in TABLE 2-9.

TABLE 2-9. COMPARISON OF R_{TH} VALUES OBTAINED FROM FEM SIMULATION AND TWO DIFFERENT THERMAL MODELS

Run	Simulated R_{th} (˚C/W)	R_{th} from Boundary-dependent Model (˚C/W)	Error from Boundary-dependent Model	R_{th} from 45˚ Model (˚C/W)	Error from 45˚ Model
1	0.95	0.916	-3.54%	0.922	-2.95%
2	0.486	0.491	0.95%	0.459	-5.56%
3	0.399	0.376	-5.84%	0.372	-6.77%
4	0.548	0.546	-0.33%	0.799	45.80%
5	0.369	0.359	-2.84%	0.417	13.01%
6	0.331	0.32	-3.26%	0.346	4.53%
7	0.471	0.464	-1.38%	0.799	69.64%
8	0.356	0.335	-5.80%	0.417	17.13%
9	0.325	0.326	0.13%	0.346	6.46%
10	0.982	0.94	-4.20%	0.957	-2.55%
11	0.518	0.516	-0.57%	0.494	-4.63%
12	0.432	0.404	-6.31%	0.407	-5.79%
13	0.532	0.515	-3.20%	0.584	9.77%
14	0.363	0.354	-2.65%	0.36	-0.83%
15	0.331	0.321	-2.91%	0.317	-4.23%
16	0.428	0.428	-0.02%	0.584	36.45%

17	0.336	0.322	-4.42%	0.36	7.14%
18	0.317	0.307	-3.13%	0.317	0.00%
19	1.016	1.074	5.70%	0.991	-2.46%
20	0.553	0.576	4.02%	0.528	-4.52%
21	0.466	0.441	-5.47%	0.442	-5.15%
22	0.54	0.51	-5.43%	0.508	-5.93%
23	0.372	0.361	-3.07%	0.341	-8.33%
24	0.341	0.33	-3.18%	0.31	-9.09%
25	0.423	0.417	-1.45%	0.48	13.48%
26	0.336	0.324	-3.45%	0.332	-1.19%
27	0.319	0.31	-2.79%	0.304	-4.70%

As it can be observed from TABLE 2-9, the maximum error of thermal resistance can be as high as 69.64%, which is much higher than that of the proposed boundary-dependent model (6.31%).



(a) (b)

Figure 2-19. Assumption of 45° heat spreading angle in the power module (a) and calculation of the effective spreading area (b).

The coefficient of determination, R^2, can be used to evaluate these two models [62]. It provides a measure of how well future outcomes are likely to be predicted by the model. The value of R^2 is the range from 0 to 1. The higher R^2 value indicates that the model can fit the data very well. From the data in TABLE 2-9, the sum of the squares of the errors is given by:

$$SS_{tot} = \sum_{i=1}^{27} (R_{th\_sim\_i} - \overline{R}_{th\_sim})^2 \tag{2-25}$$

where $R_{th\_sim\_i}$ is the simulated thermal resistance and i represents the observed data point. $\overline{R}_{th\_sim}$ is the mean of the data points and is defined by:

$$\overline{R}_{th\_sim} = \frac{1}{27} \sum_{i=1}^{27} R_{th\_sim\_i} \tag{2-26}$$

The sum of squares of errors between simulated values and modeled values is calculated using:

$$SS_{err} = \sum_{i=1}^{27} (R_{th\_sim\_i} - R_{th\_model\_i})^2 \tag{2-27}$$

$R_{th\_model\_i}$ in equation (2-27) is the thermal resistance predicted by model. From equations (2-25) and (2-27), the coefficients of determination of these two models can be obtained using equation (2-28) and listed in TABLE 2-10.

$$R^2 = 1 - \frac{SS_{err}}{SS_{tot}} \tag{2-28}$$

The coefficient of determination of the proposed boundary-dependent model is nearly 1 which indicates a good fitting between the model and the data. However, the coefficient of determination of the thermal model based on 45° heat spreading angle is only 0.791.

To further check the accuracy of the boundary-dependent thermal model, the thermal resistances at some data points that were not used for the curve fitting were calculated using two thermal models as shown in TABLE 2-11. It can be seen that the maximum error of the thermal resistance obtained from the boundary-dependent thermal model is only

8.15% which is much lower than that from the thermal model based on 45° spreading angle.

Figure 2-20 shows comparison of the thermal resistances obtained from FEM simulation, the proposed boundary-dependent thermal model, and the thermal model based on 45° spreading angle with d = 4 mm and a = 26 mm. It indicates thermal resistance is significantly overestimated by using the thermal model based on 45° heat spreading angle when the heat transfer coefficient is low. In other words, the heat tends to spread to a large area (spreading angle is larger than 45°) with low heat transfer coefficient. Only under high heat transfer coefficient condition, the 45° spreading angle can be used to approximate the heat transfer in the power module. However, the results from the proposed boundary-dependent thermal model agree with the results of the FEM simulation very well.

TABLE 2-10. EVALUATION OF TWO DIFFERENT THERMAL MODELS

	Maximum Error	**Coefficient of Determination**
45˚ Heat Spreading Thermal Model	69.64%	0.791
Boundary-dependent Thermal Model	6.31%	0.988

TABLE 2-11. ERRORS FROM TWO DIFFERENT THERMAL MODELS FOR THE NON-FITTING DATA POINTS

a_1 **(cm)**	d **(mm)**	h **(W/(m^2·C)**	**Simulated R_{th} (˚C/W)**	**Error from Boundary-dependent Model**	**Error from 45˚ Model**
1.6	2	22000	0.446994	6.04%	-5.91%

1.6	2	34000	0.383438	7.76%	-8.37%
1.6	2	40000	0.365819	7.73%	-9.16%
1.8	2	22000	0.415105	4.67%	1.31%
1.8	2	34000	0.363951	5.87%	-3.46%
1.8	2	40000	0.349723	5.91%	-4.98%
2.4	2	22000	0.371975	-1.34%	13.06%
2.4	2	34000	0.339903	-1.15%	3.37%
2.4	2	40000	0.330467	-0.78%	0.56%
2.6	2	22000	0.365821	-3.34%	14.96%
2.6	2	34000	0.336814	-3.12%	4.31%
2.6	2	40000	0.328124	-2.57%	1.28%
1.6	4	22000	0.461904	5.87%	-13.72%
1.6	4	34000	0.399083	8.00%	-15.85%
1.6	4	40000	0.381796	8.15%	-16.55%
1.8	4	22000	0.423575	4.56%	-14.72%
1.8	4	34000	0.37375	6.33%	-16.59%
1.8	4	40000	0.360054	6.57%	-17.20%
2.4	4	22000	0.367694	-0.32%	-6.46%
2.4	4	34000	0.338708	0.06%	-11.27%
2.4	4	40000	0.330555	0.29%	-12.69%

2.6	4	22000	0.35867	-2.05%	-4.11%
2.6	4	34000	0.33345	-1.93%	-9.87%
2.6	4	40000	0.326277	-1.68%	-11.55%

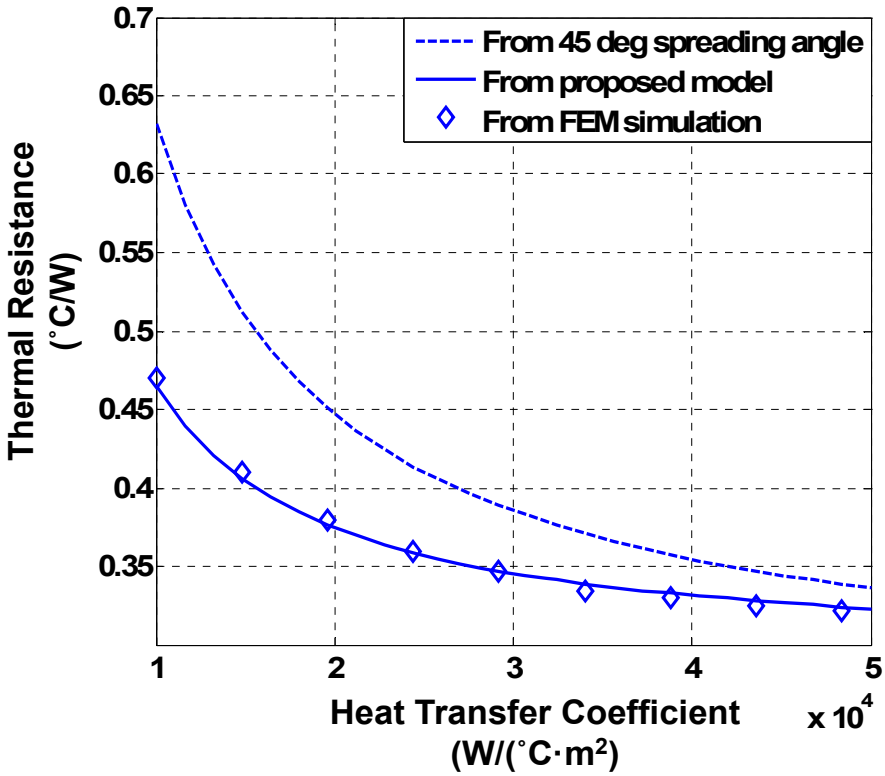


Figure 2-20. Comparison of thermal resistances obtained from FEM simulation, proposed boundary-dependent thermal model, and 45° spreading thermal model (d = 4 mm and a = 26 mm).

2.3. Conclusion

In this chapter, a boundary-dependent steady-state thermal model based on finite difference method was developed. Each layer in the power module was modeled as a thermal resistance in the proposed model. The resistance value is determined by the material properties of the layer and the effective heat spreading area. The spreading area is dependent on the footprint area of the power module, thickness of the heat-spreader, and the heat transfer coefficient of the heat-exchanger. The relation between the effective

spreading area of the heat and the parameters mentioned above were established using response surface method. The proposed model was verified using finite element simulation. It shows that compared to the conventional thermal model based on 45° heat spreading angle, the proposed model can provide more accurate prediction on the thermal resistance of the power module. The maximum error from the proposed thermal equivalent circuit is only 8.15% (vs 69.64% from the 45° heat spreading model). In addition, the coefficient of determination of the proposed model is much higher than the thermal model based on 45° heat spreading angle (0.988 vs 0.781). The assumption of 45° heat spreading angle is only valid for cases with high heat transfer coefficient and thick substrate.

Chapter 3. A TRANSIENT THERMAL MODEL TO PREDICT PEAK TRANSIENT TEMPERATURE

An accurate transient thermal model is necessary for transient thermal design and coupled electro-thermal simulation of complete power electronics system including semiconductor devices, thermal packages, and heat-exchangers [63]-[64]. In this chapter, a transient thermal model is proposed for the power module based on the effective heat spreading area calculated in Chapter 2. The FEM simulation results also show that the proposed transient thermal model can predict the transient thermal performance of the power module accurately. With the proposed thermal model, coupled electro-thermal simulation of the power module is conducted to predict the peak transient temperature.

3.1. Thermo-Electrical Coupled Simulation Using Transient Thermal Model

As shown in Figure 3-1, the power electronics system is an coupled electro-thermal system. Under critical transient thermal situation, the self-heating effects of the semiconductor devices play an important role [65]-[66]. The characteristics of power device such as threshold voltage and on-resistance are significantly affected by the junction temperature. As a result, the changed device characteristics will cause the change of the power dissipation, which again leads to change of the junction temperature. This coupling effect imposes challenge in predicting the system behaviors. Thus, the coupled electro-thermal simulation is required to predict the following system behaviors:

1. Predict thermal runaway

For those devices that have positive temperature coefficient, the on-resistance of the device increases with junction temperature. The increase of the on-resistance will further increase the power dissipation, leading to even higher junction temperature. This may cause thermal instability in the system [67]-[68]. The coupled electro-thermal simulation can be used to verify the stability of the thermal design.

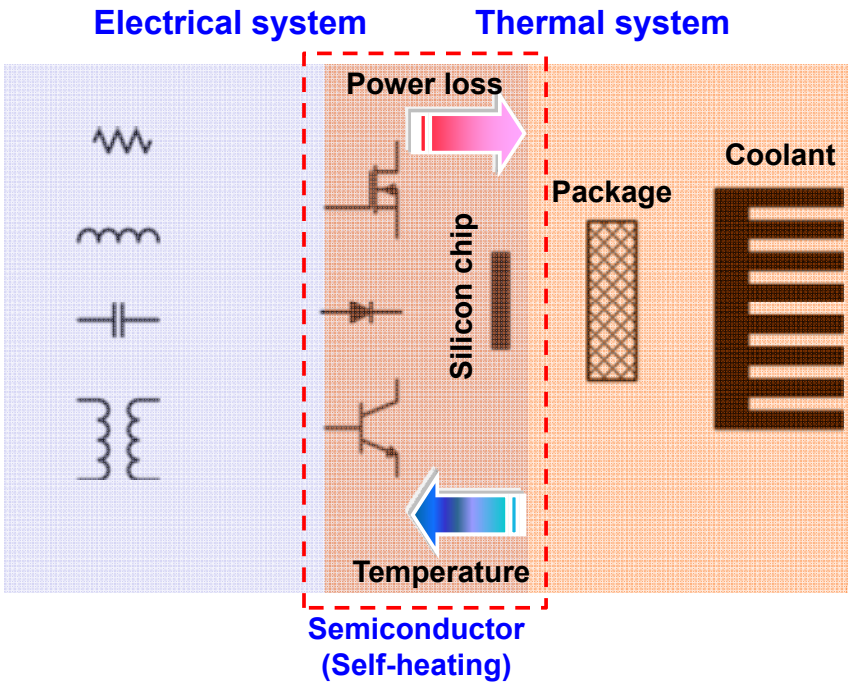


Figure 3-1. Self-heating effect in power electronics system.

2. Predict device overheat during transient

In the coupled electro-thermal simulation, the device junction temperature, device characteristics, and device power dissipation changes instantaneously. Therefore, the simulation can predict junction temperature of complicated components very accurately even under transient condition [69].

3. Simulate current sharing in parallel devices

For power devices in parallel, the thermal performance difference in the package can cause different junction temperature for each device, resulting in unbalance current sharing [70]. The electro-thermal simulation can be used to predict this behavior and improve the thermal design.

4. Simulate power cycling

The electro-thermal simulation can provide the temperature information of the power module under power cycling, which can be used as input for the stress simulation [71].

Figure 3-2 shows the key steps for electro-thermal simulation. Based on packaging structure and material properties, the thermal model is firstly extracted. Then the thermal

model can be implemented in circuit simulator. With the temperature-dependent device model, the whole system with the coupling between electrical and thermal can be simulated.

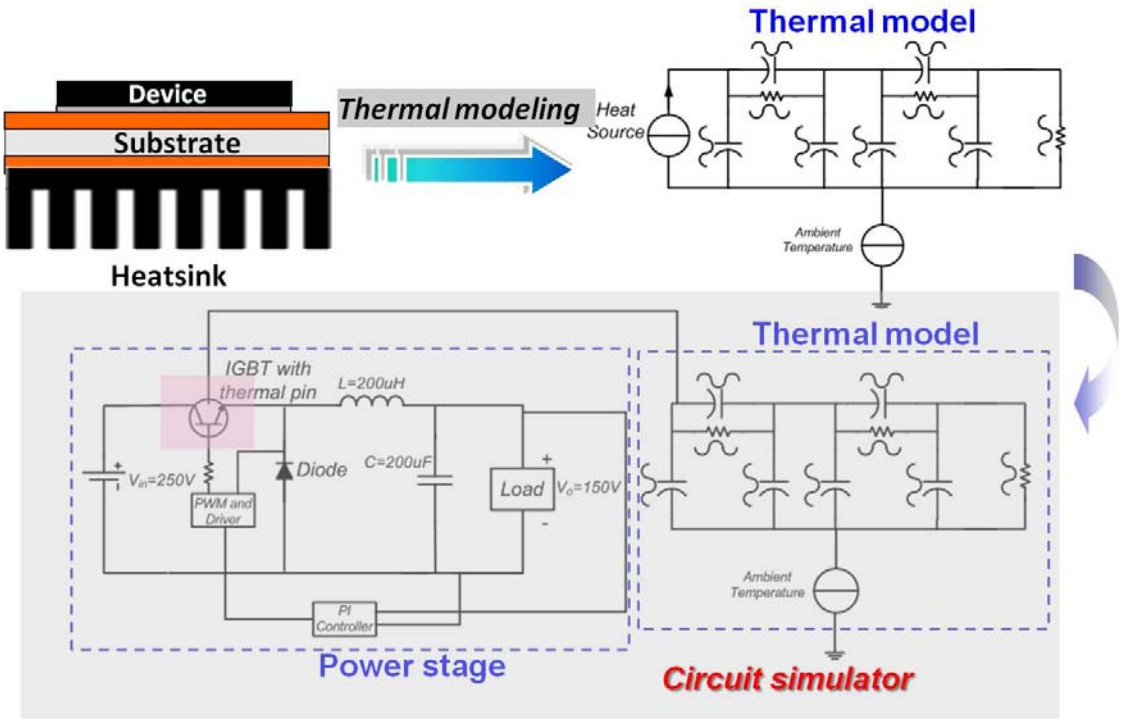


Figure 3-2. Key steps for coupled electro-thermal simulation.

3.2. Transient Thermal Model Based On Effective Heat Spreading Area

There were many methods proposed by researchers to extract the transient thermal model for power electronics systems. In [72]-[73], the heat transfer equations were analytically solved using eigenfunctions or Green's function. However, the analytical solutions are described using complicated integrals which do not show the physical meaning of the thermal model. In addition, these integrals still need to be solved using numerical algorithm, which makes the results difficult to be used in thermo-electrical coupled simulation. In [74]-[75], transient thermal models constructed by RC networks can be extracted from finite element simulation results. However, these models are built based on pure numerical simulations. To describe the transient response of the power module, a large number of transient FEM simulations have to be performed. This

significantly increases the calculating times. Also, since there is no geometry information or boundary conditions contained in the model, all the tedious numerical extraction processes have to be repeated once the geometry of the power module changes.

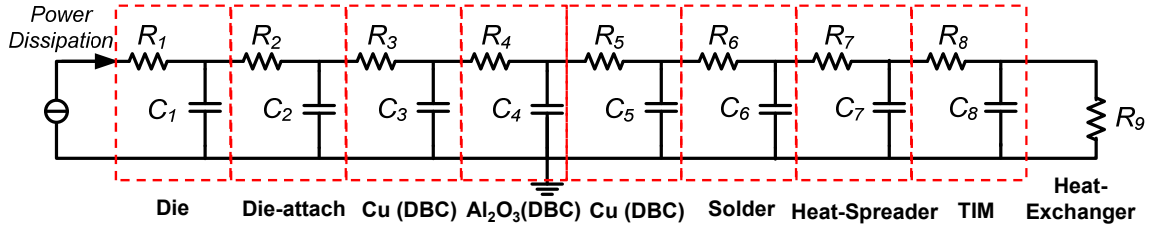


Figure 3-3. The transient thermal model based on finite difference method (FDM) of the power module shown in Figure 2-1.

In Chapter 2, a thermal model based on finite difference method was proposed as shown in Figure 3-3. To calculate the thermal resistance, the effective area of each layer was extracted based on steady-state thermal simulations. The results clearly show good matching between the thermal model and FEM simulation results. The effective area obtained also can be used to calculate the thermal capacitance of i^{th} layer in power module as shown in equation:

$$C_i = \rho_i \cdot c_{pi} \cdot d_i \cdot A_i \tag{3-1}$$

where ρ_i, c_{pi}, and d_i are the density, specific heat capacity, and thickness of the i^{th} layer. A_i is the effective heat spreading area in the layer calculated in Chapter 2.2. The detailed

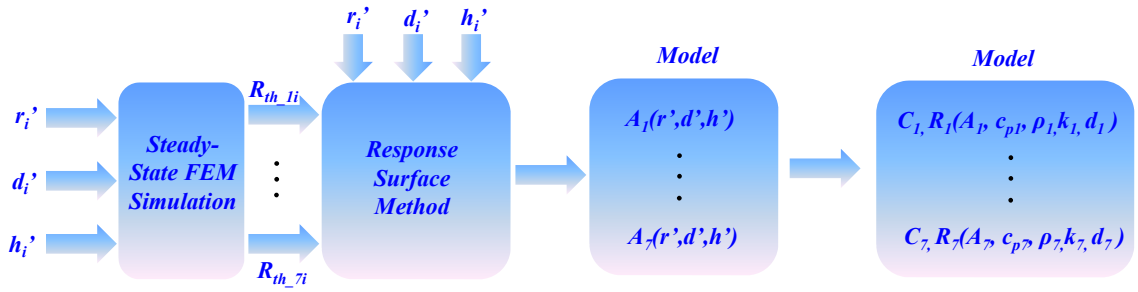


Figure 3-4. Procedure to build transient thermal model for the power module.

procedure to build the transient thermal model is shown in Figure 3-4. Thus, the power module in Figure 2-1 can be modeled as the thermal circuit shown in Figure 3-3.

3.3. Verification of Transient Thermal Model Using FEM Simulation

The transient thermal model shown in Figure 3-3 is used to predict the transient responses of the power module to step thermal load. As discussed in Chapter 2, the effective heat spreading area of each layer also can be obtained based on 45° heat spreading angle. Thus, the comparisons of the results obtained from the two different transient thermal models and the results from FEM simulation are plotted in Figure 3-5 and Figure 3-6. Figure 3-5 shows the comparison under eight extreme conditions of the range investigated. It can be seen when the footprint area of the power module is small (a = 12 mm), both thermal models can predict the transient response of the power module very well. This is because for power modules having small footprint area, the limitation of the heat spreading effect is the boundary of the module instead of the heat spreading angle. However, the results from 45° heat spreading angle still have larger error. For the power modules that have large footprint area (a = 28 mm) and low heat transfer coefficient (h = 10000 W/(m^2·K)), significantly discrepancies between the results from 45° heat spreading model and FEM simulation results (maximum error is 65%). This can be further confirmed by the comparison results in Figure 3-6. The thermal model based on 45° heat spreading angle also fails to predict transient responses of the power module for other two low heat transfer coefficient cases. However, similar with the steady-state thermal resistance, when the heat transfer coefficient goes to high value (h = 50000 W/(m^2·K)), 45° heat spreading model is able to provide fairly accurate prediction for transient thermal response even if the footprint area of the power module is large. In conclusion, 45° heat spreading model is only valid for power modules with small footprint area and high heat transfer coefficient (h > 50000 W/(m^2·K)). On the contrary, the proposed boundary-dependent model can predict the transient thermal response of the power module accurately under all conditions.

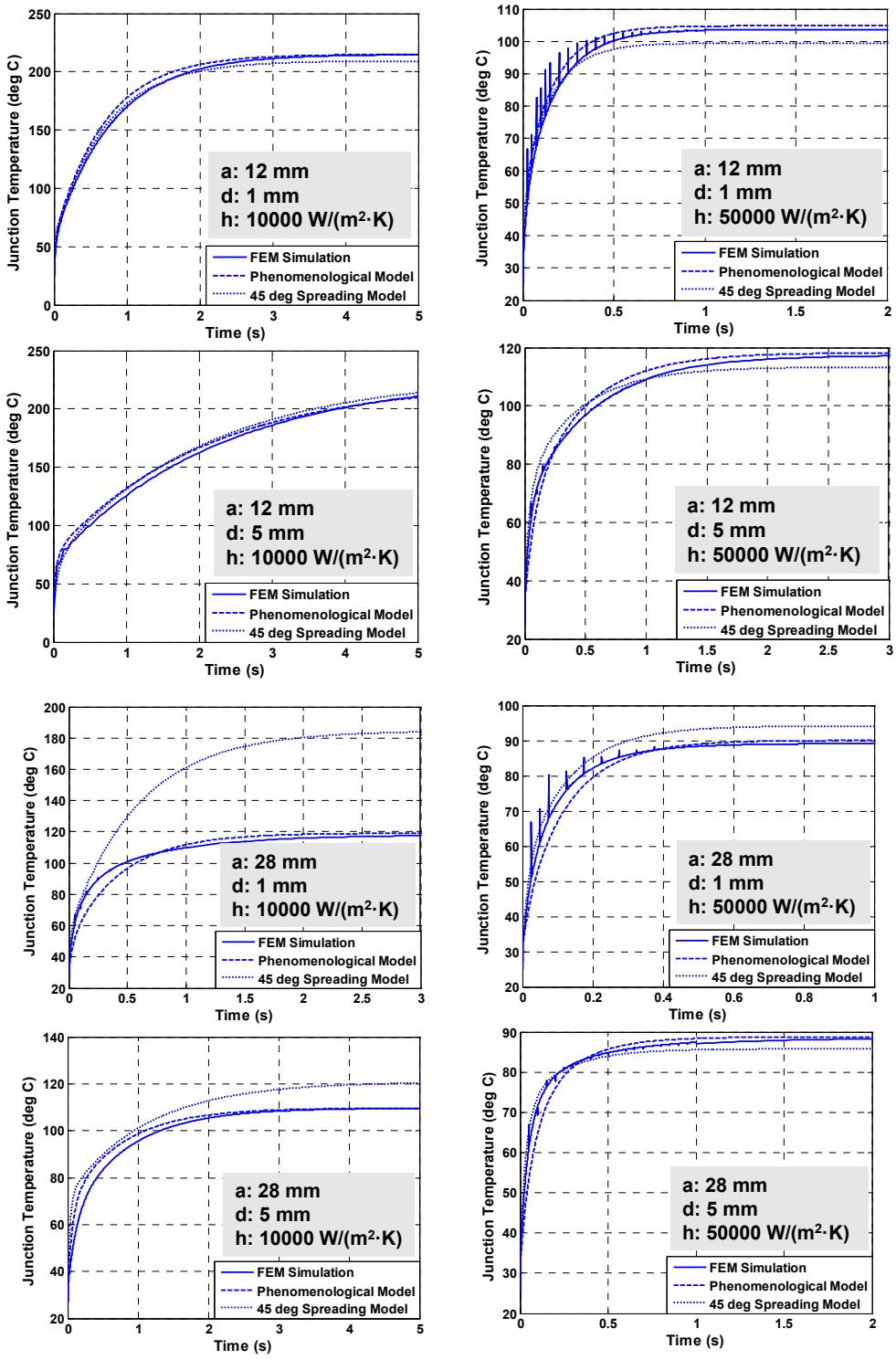


Figure 3-5. Comparison of transient thermal responses of the power module obtained from FEM simulation, boundary-dependent thermal model, and 45° spreading thermal model (Φ = 200 W/cm^2)(structure used for simulation shown in Figure 3-7).

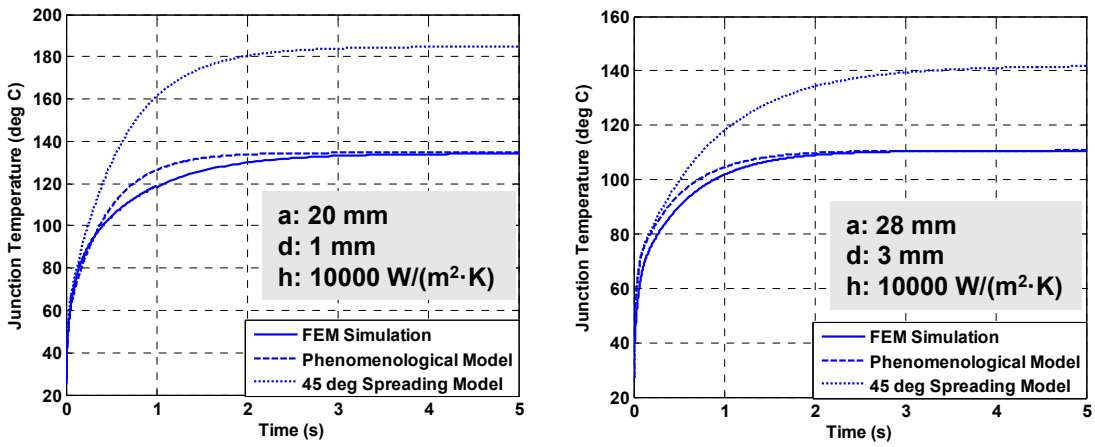


Figure 3-6. Comparison of transient thermal responses of the power module with low heat transfer coefficient and large footprint area obtained from FEM simulation, boundary-dependent thermal model, and 45° spreading thermal model (Φ = 200 W/cm^2) (structure used for simulation shown in Figure 3-7).

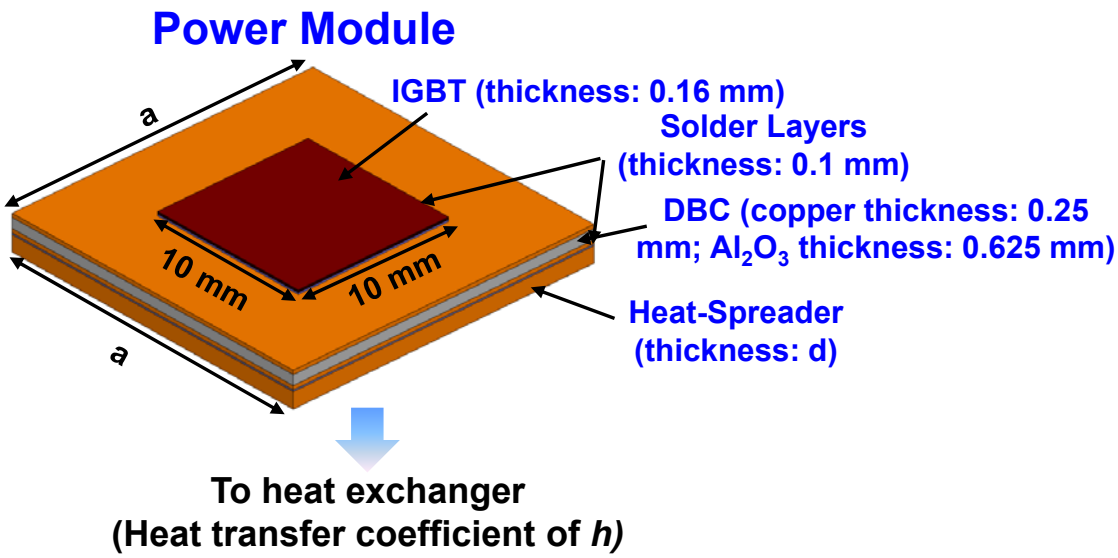


Figure 3-7. Structure used in the simulations for Figure 3-5 and Figure 3-6.

3.4. Prediction of Peak Transient Temperature of Power Module Using Coupled Electro-thermal Simulation

3.4.1. Design Specification

In this section, a design case will be presented to show the steps to perform coupled electro-thermal simulation to estimate the peak junction temperature of the IGBT. The power module is a buck converter with one IGBT and one diode as shown in Figure 3-8. The key parameters and load profile for the buck converter are shown in Figure 3-9. During the load transient period (0.3 second), the load current will increase from 20 A to 40 A at slew rate of 0.2 A/μs (for both step up and step down load changes), leading to significant increasing of power dissipation in IGBT. This could cause overheating of the IGBT. In this application, the maximum junction temperature of IGBT is 125°C. Thus, the proper heat transfer coefficient of the heat-exchanger has to be selected based on coupled electro-thermal simulation to prevent IGBT from overheating.

3.4.2. Extraction of Transient Thermal Model

Since the power module includes many layers, each layer can be treated as one element and modeled as one RC network shown in Figure 3-3. In the power module, the distance between the IGBT and the diode is designed in such a way that the thermal interference should be avoided. Since the IGBT has higher heat flux than the diode, in this study, only the IGBT is considered. The power module and its dimensions are shown in Figure 3-10. The IGBT is soldered on the DBC substrate. The heat-spreader is attached to the substrate to spread the heat to a larger area. A liquid heat-exchanger with the heat transfer coefficient of h is installed underneath of the power module. The parameters in the thermal model shown in Figure 3-3 can be derived using the method mentioned in Chapter 2. To verify the proposed model, ePhysics software is used to simulate the junction temperature under thermal transient situation (power dissipation is 200 W and h

is 10000 W/(m^2·°C) and 50000 W/(m^2·°C)). The properties of materials used in simulation are shown in TABLE 3-1. Figure 3-11(b) shows the comparison of junction temperature-versus-time curves obtained from FEM thermal model and ePhysics simulation. It can be found that the two curves match very well. Therefore, this FEM thermal model can be imported into Saber circuit simulator for coupled electro-thermal simulation.

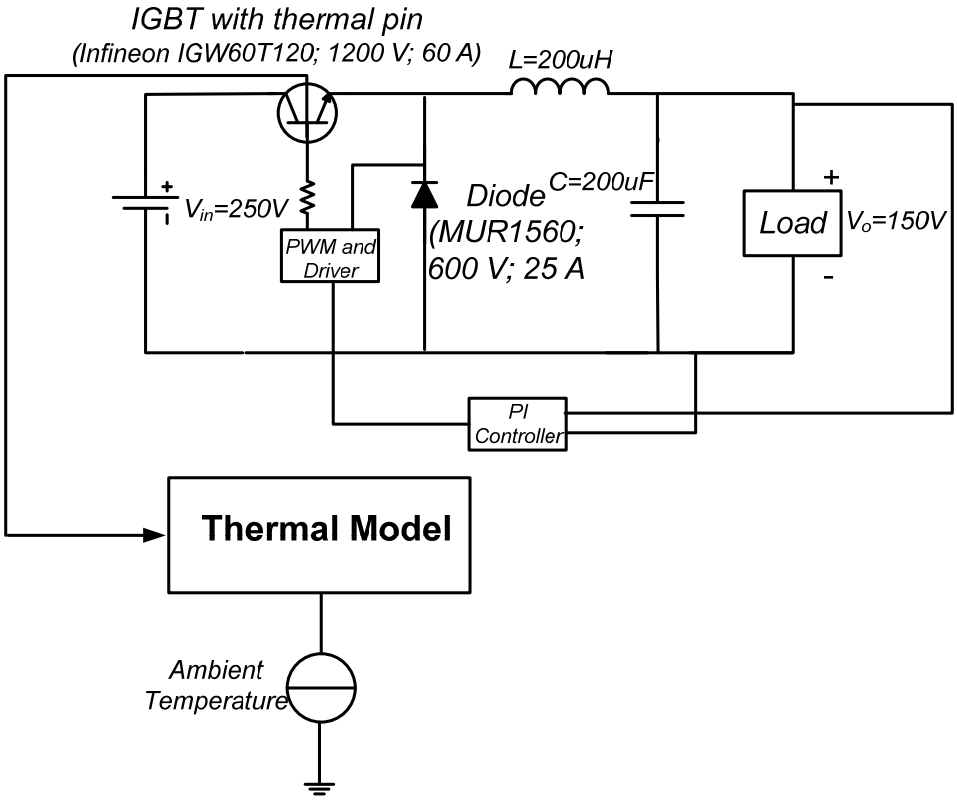


Figure 3-8. Buck converter used for coupled electro-thermal simulation.

Specifications for DC-DC Buck Converter	
Input voltage	250 V
Output voltage	150 V
Steady-state load current	20 A
Transient load current	40 A
Maximum Junction Temperature of IGBT	150°C

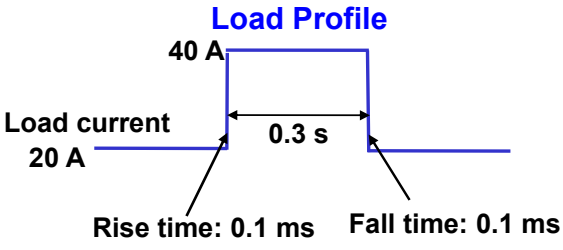
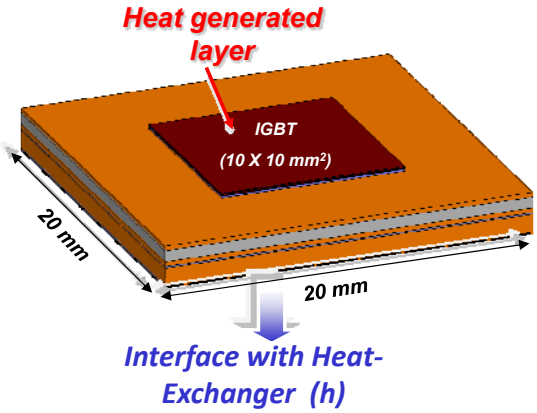
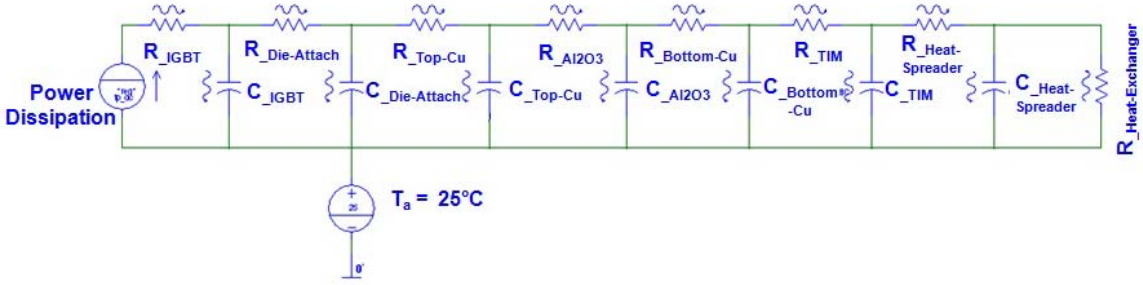


Figure 3-9. Key parameters and load profile for buck converter.

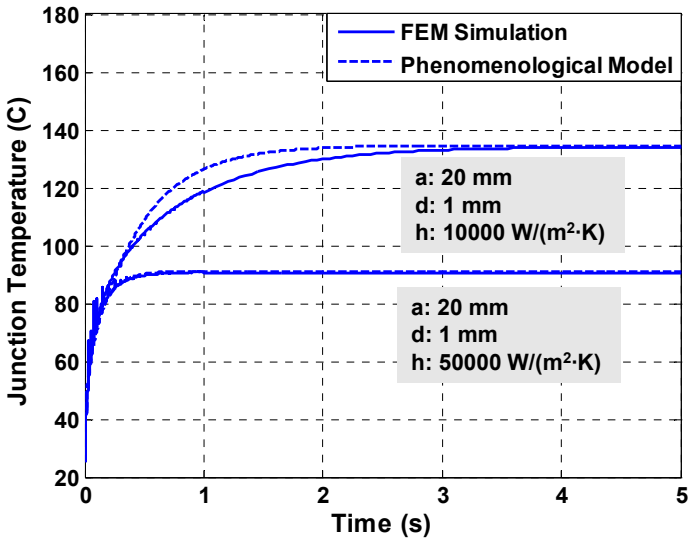


Layer		Thickness
DBC	Cu	0.25 mm
	Al_2O_3	0.625 mm
IGBT		0.16 mm
Solder		0.1 mm
Heat-Spreader		1 mm

Figure 3-10. The power module and its dimensions.



(a)



(b)

Figure 3-11. Boundary-dependent model of the power module in Saber (a) and the verification of the thermal model using finite element simulation (b).

TABLE 3-1. MATERIAL PROPERTIES USED IN SIMULATION

	Thermal Conductivity *k*	Specific Heat Capacity *c*	Mass Density ρ
Copper	400 *W/(m·C)*	385 *J/(kg·C)*	8933 kg/m^3
Alumina in DBC	35 *W/(m·C)*	850 *J/(kg·C)*	3960 kg/m^3
IGBT	148 *W/(m·C)*	712 *J/(kg·C)*	2330 kg/m^3
Solder	48 *W/(m·C)*	167 *J/(kg·C)*	8000 kg/m^3

3.4.3. Prediction of Peak Junction Temperature Using Coupled Electro-thermal Simulation

Figure 3-12 shows the diagram of coupled electro-thermal simulation for the power module in Saber software. IGBT model used in this simulation is physic-based model which has temperature-dependent characteristics [76]-[77]. The temperature information is fed into the device model through the thermal pin of the IGBT shown in Figure 3-12. Meanwhile, this pin also provides the power loss information of the IGBT as the input of the thermal model simultaneously. This enables the coupling effect between the thermal system and the electrical system.

With the diagram shown in Figure 3-12, the whole system can be simulated with different heat transfer coefficients of the heat-exchanger. Figure 3-13 illustrates the junction temperature waveforms of the IGBT and the output voltage waveforms under load transient with different heat transfer coefficients. It clearly shows that the peak junction temperature of the IGBT can be as high as 175°C during transient when h= 10000 W/(m^2·°C) (case 2 in Figure 3-13). This could cause damage of the IGBT. Also, it can be observed that the power losses in the IGBT increase during the transient. This is caused by the positive temperature coefficient of the IGBT on-resistance. If the transient period increases, the junction temperature of the IGBT could go to extremely high value and thermal runaway will occurs. When the heat transfer coefficient of the heat-exchanger is increased to 50000 W/m^2 (case 1 in Figure 3-13), the maximum

junction temperature of the IGBT is reduced to 125˚C, which is lower than the allowed the maximum junction temperature for IGBT (150˚C). Figure 3-14 shows the collector-emitter current and voltage of IGBT under heavy load for two different cases. It can be seen that the voltage waveforms of these two cases are very similar. However, due to different junction temperature the turn-off current for two cases are different. In case 1, the lower junction temperature leads to lower tail current. The lower tail current again helps reduce the loss in the IGBT.

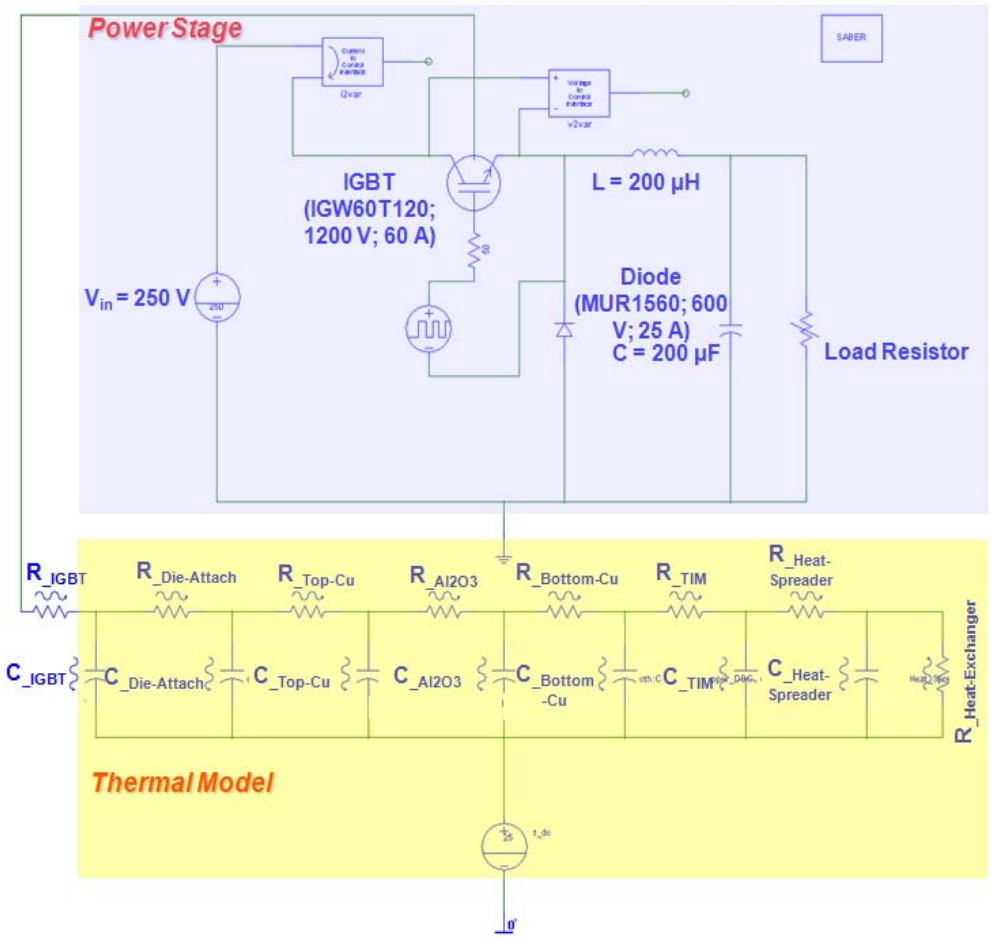


Figure 3-12. Coupled electro-thermal simulation of buck converter in Saber.

In the conventional method used to estimate the peak junction temperature, the power losses in the IGBT at certain junction temperature are firstly estimated using the

datasheet provided by the manufacturer. Since the actual junction temperature of the IGBT is unknown, the junction temperature of the IGBT is assumed to be 25˚C or 150˚C. After calculating the power losses, the junction temperature of the IGBT can be derived by multiplying the power losses and the thermal resistance of the power module and the results are shown in TABLE 3-2. It can be seen that large discrepancy occurs between the junction temperature calculated and the junction temperature obtained from the coupled electro-thermal simulation. This shows that without considering the coupled electro-thermal effect in the IGBT, the thermal system of the power module can be either underdesigned or overdesigned.

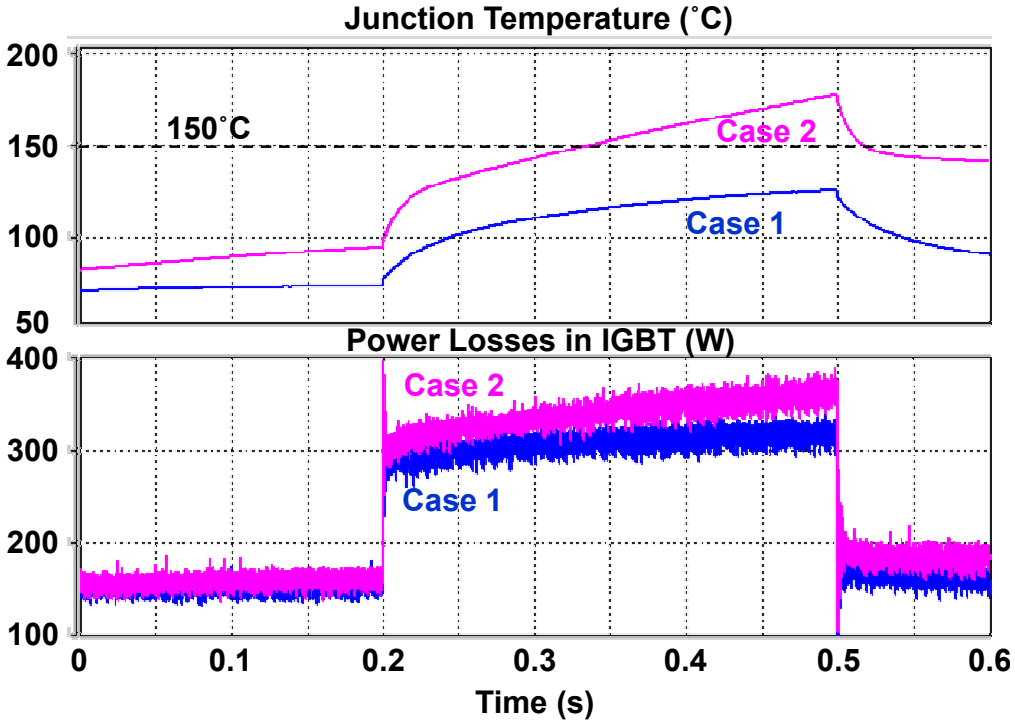


Figure 3-13. Junction temperatures and power losses in IGBT for two cases (case 1: h = 50000 W/(m^2·˚C); case 2: h = 10000 W/(m^2·˚C)).

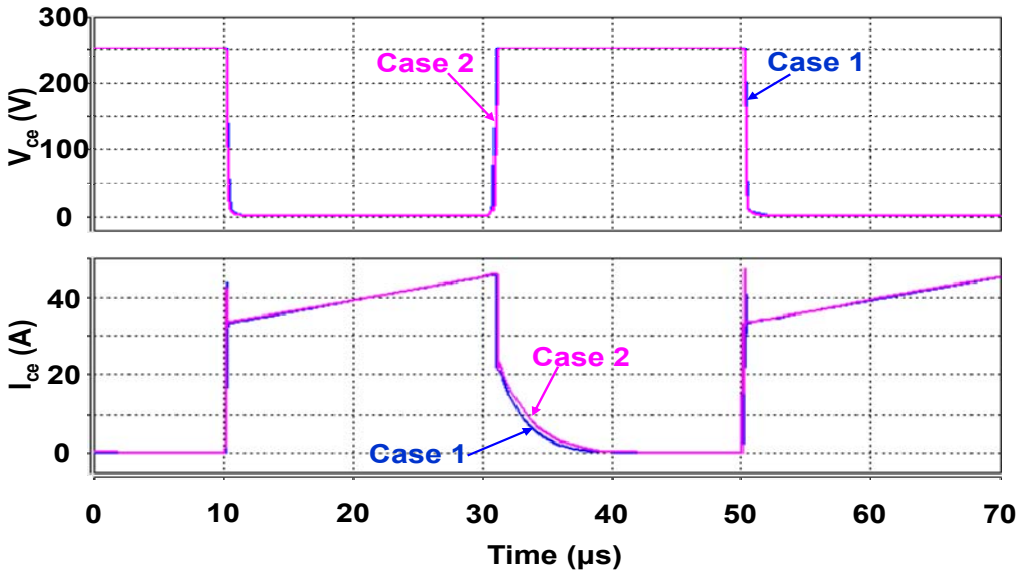


Figure 3-14. Collector-emitter current and voltage of IGBT for two different cases (case 1: h = 50000 W/(m^2·°C); case 2: h = 10000 W/(m^2·°C)).

TABLE 3-2. COMPARISON OF CALCULATED AND SIMULATED PEAK JUNCTION TEMPERATURE OF IGBT

P_{l1}(T_j = 25°C)	**237.46 W**
P_{l2}(T_j = 150°C)	309.23 W
Peak T_j Using P_{l1}	155.15°C
Peak T_j Using P_{l2}	194.49°C
Peak T_j using coupled electro-thermal simulation	175.23°C

3.5. Conclusion

The accurate transient thermal model is essential for coupled electro-thermal simulation. In this chapter, a transient thermal model for the power module was developed based on the effective heat spreading area. The transient thermal responses of the power module obtained from the proposed model agree with the results from finite element simulation. A case study was presented to show how to use coupled

electro-thermal simulation to select the heat transfer coefficient of the heat-exchanger. The coupled electro-thermal simulation can provide more accurate information on the peak junction temperature of the IGBT than the conventional method.

Chapter 4. MEASUREMENT OF TRANSIENT THERMAL IMPEDANCE OF POWER MODULE AND ITS APPLICATION IN CHARACTERIZATION OF DIE-ATTACH MATERIALS

In recent years, there is a growing demand to increase the power density of power modules. As a result, the heat flux generated by power semiconductor devices keeps on increasing. In some motor drive applications, the heat flux can be higher than 100 W/cm^2 in steady state, and the peak heat flux can be as high as 300 W/cm^2 under transient conditions [3]. Figure 4-1 shows the cross-section of a conventional power module. The heat generated from the IGBT has to travel through all the layers before it dissipates into the ambient. To evaluate the transient thermal performance of a power module, a thermal impedance measurement method that can be applied to fully packaged power electronics system has to be proposed.

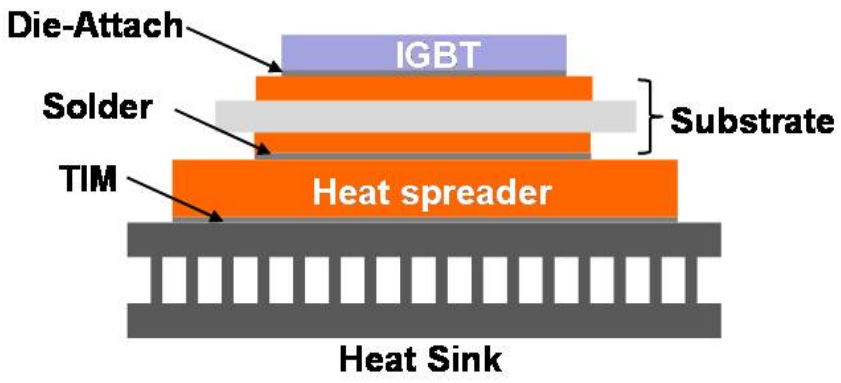


Figure 4-1. Cross-section of a power module with heat sink.

In this chapter, a measurement system for thermal impedance is developed. The gate-emitter voltage (V_{ge}) of an Insulated Gate Bipolar Transistor (IGBT) is employed as the temperature-sensitive parameter. Compared to the forward voltage drop of a pn

junction, V_{ge} is more sensitive to temperature change, resulting in more accurate measurements. In spite of the temperature dependency of the IGBT electrical characteristics, the power dissipation in the IGBT is regulated to be constant by adjusting the gate voltage via feedback control during the heating phase.

Thermal properties of the die-attach layer play a vital role in the thermal management of the system. The conventional method for evaluating the thermal properties of the die-attach is to use the thermal resistance of the power module. However, it can yield only the total value for the whole structure without any information about the contributions of the layers along the heat path. In addition, the variables induced in the measurement such as the thickness of the thermal interface materials and the ambient temperature could affect measurement results. With the developed measurement setup, the thermal impedances of samples with three die-attach materials are measured to evaluate thermal performance and reliability of die-attach materials. By controlling the width of the heating pulse, the depth to which the heat diffuses can be controlled to minimize the interference of the other layers in the measurement of the thermal impedance of the die-attach layer.

4.1. Selection of Temperature-Sensitive Parameter

There are several methods proposed in literature to measure the thermal impedances of packaged power modules [78]. Thermal impedance measurement using the electrical parameters of semiconductor devices is widely used thanks to such advantages as fast response and non-destructive measurement, which can be applied to a fully packaged power module. Several electrical properties of semiconductor, such as the forward-voltage of a pn junction and the gate-emitter voltage of an IGBT, are strong functions of temperature [79]-[83]. In [82], the turn-on delay and di_{ds}/dt were used to monitor the average junction temperature of MOSFET under operating condition. The change of these parameters can be used to infer the junction temperature of the semiconductor die.

4.1.1. Characterization of the K-Factor for PN Junction

The forward-voltage of a pn junction is the most commonly used temperature sensitive parameter for thermal impedance measurement. The variation of the junction voltage with temperature at a constant current I_{pn} is found to be [81]:

$$\frac{dV_{pn}}{dT} = -\gamma \frac{k}{q} + \frac{(V_{pn} - E_g / q)}{T} \tag{4-1}$$

where q is the electron charge (1.6×10^{-19} C); k is Boltzmann's constant (1.381×10^{23} J/K); V_{pn} is the voltage across the junction; T is the temperature; γ is a constant equal to about 3; and E_g is the bandgap of silicon (1.12 eV at 275 K). Restricted by the properties of silicon material, the K-factor of a pn junction is around 2 mV/°C. Figure 4-2 plots the

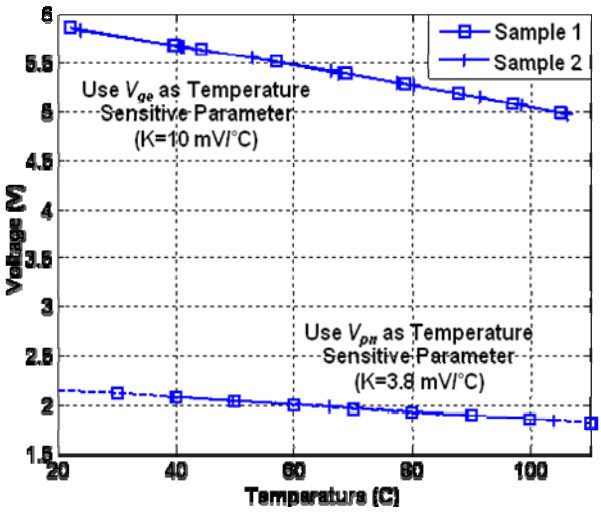


Figure 4-2. Measured K-factor for the forward voltage of two power diodes in series and the gate-emitter voltage for an IGBT. (Drive current for the power diodes: 0.4 mA; drive current for the IGBT: 1.5 mA; the collector-emitter voltage for the IGBT: 5 V.)

relationship between the forward-voltage and the junction temperature of two diodes in series (bottom curves). During the characterization, the temperature of the diodes is controlled by a hot plate installed underneath. To avoid the self-heating effect, a very small current (0.4 mA) is injected into the temperature sensing diodes. The forward-voltage drop of the diodes is linear versus the junction temperature between

25˚C and 130˚C. However, even with two sensing diode in series, the value of the K-factor is only 3.8 mV/˚C.

4.1.2. Characterization of the K-Factor for Gate-Emitter Voltage of an IGBT

For a given collector current and collector-emitter voltage across an IGBT, the gate voltage can be used as the temperature sensitive parameter for thermal impedance measurement [82]-[83]. When the IGBT is heated up, the gate-emitter voltage decreases to maintain the same collector current. The temperature coefficient is around 10 mV/˚C for most power IGBTs. Figure 4-3 shows the test set-up for the K-factor characterization of an IGBT. The IGBT (IRG4CH30K from International Rectifier) was attached on a silver-plated DBC substrate. A chip thermistor was attached on the same substrate to measure the temperature of the substrate, controlled by a hot plate installed underneath. A

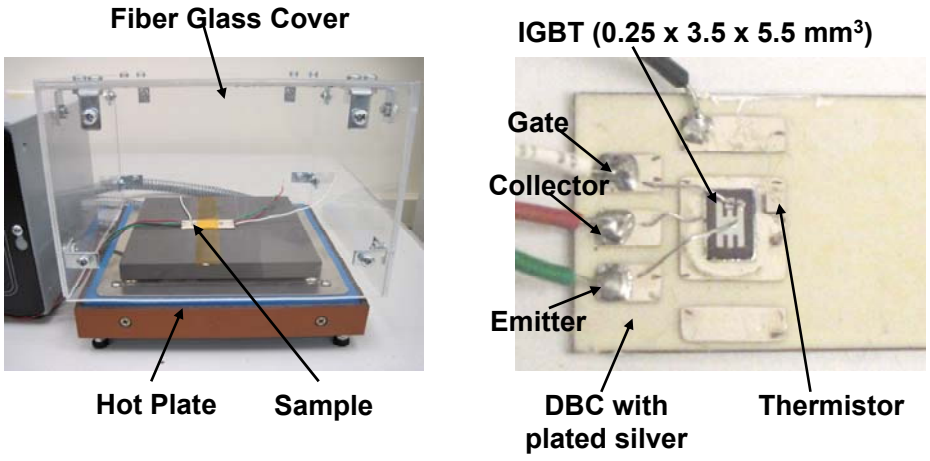
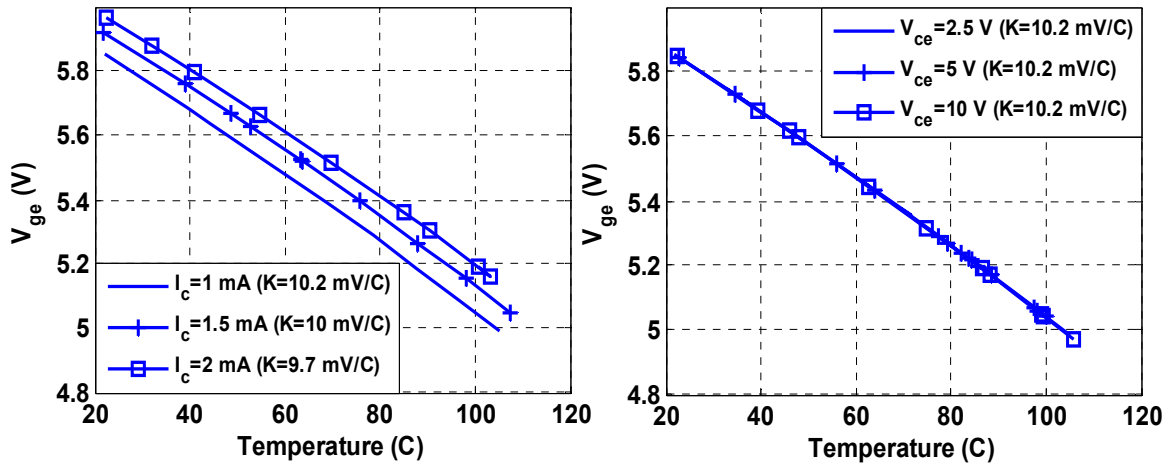


Figure 4-3. Set-up for the K-factor measurement of IGBT IRG4CH30K from International Rectifier (a) and the sample used for measurement (b).

cover made of fiberglass was employed to minimize the temperature disturbance from the environment. The K-factors of two samples were measured and shown in Figure 4-2. It can be seen that with a 1.5 mA collector current and a 5 V collector-to-emitter voltage, the K-factor of the IGBT is 10 mV/°C, which shows V_{ge} is much more sensitive than the pn

junction voltage. The variation of the K-factor between the two samples is less than 0.5%. The sensitivity of the K-factor for V_{ge} was also investigated. The collector current of the IGBT during the measurement period was changed from 1 mA to 2 mA and the curves of junction temperature vs V_{ge} were plotted in Figure 4-4(a). It clearly shows that there is only a 5% change when the emitter current changes from 1 mA to 2 mA. Figure 4-4(b) shows the impact of V_{ce} on the K-factor of the IBGT. It can be seen that the K-factor keeps constant even if V_{ce} changes from 2.5 V to 10 V. These results show that V_{ge} is a robust temperature sensitive parameter.



(a) (b)

Figure 4-4. Sensitivity analysis of the K-factor for IGBT IRG4CH30K: (a) K values with different collector current (V_{ce}=5 V); (b) K values with different collector-to-emitter voltage (I_c = 1 mA).

4.2. Design of Measurement System for Thermal Impedance

A circuit is designed to measure the junction temperature of the IGBT using gate-emitter voltage as a temperature sensitive parameter. The schematic diagram of the testing circuit is shown in Figure 4-5. The current flowing through the IGBT is sensed by a current sensing network, which comprises of a switch S_1, and two resistors (R_{s1} and R_{s2}). The resistor R_{s1} is in series with the switch S_1. The resistance of R_{s2} is set to be around 1000 times larger than the total resistance of R_{s1} and on-resistance of S_1. The feedback loop

shown in Figure 4-5 can regulate the voltage across the sensing network V_s to be equal to $V_{ref}R_2/R_1$ by adjusting V_{ge}. As a result, the voltage across the IGBT V_{ce} is also kept constant during the measurement.

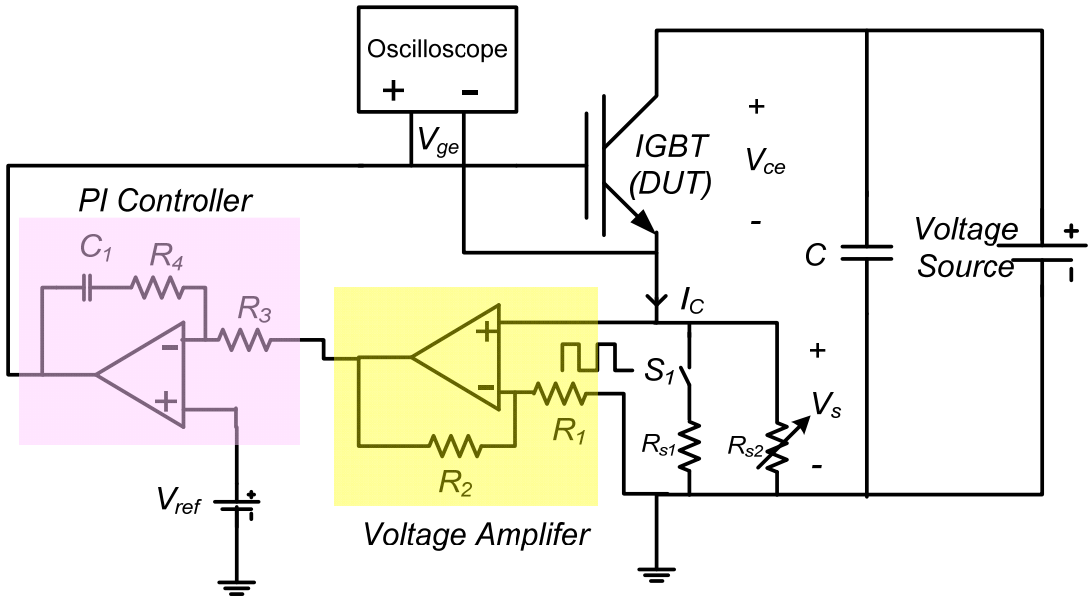


Figure 4-5. Schematic diagram of the circuit to generate regulated high-power and low-power pulses for measuring thermal impedance (part numbers and manufactures are shown in TABLE 4-1).

TABLE 4-1. COMPONENTS USED IN THE MEASUREMENT CIRCUIT

	Part Number	Manufacturer
IGBT	IRG4CH30K	IR
S_1(MOSFET)	CSD16413(R_{ds}=4.1 mΩ)	Ciclon
R_{s1}	FCSL (25 mΩ)	Ohmite
R_{s2}	43 Series Trimmer (100 Ω)	Vishay
R_3	10 kΩ	NA
R_4	47 kΩ	NA
C_1	2.2 nF	NA
Op-Amp	AD825	Analog Device

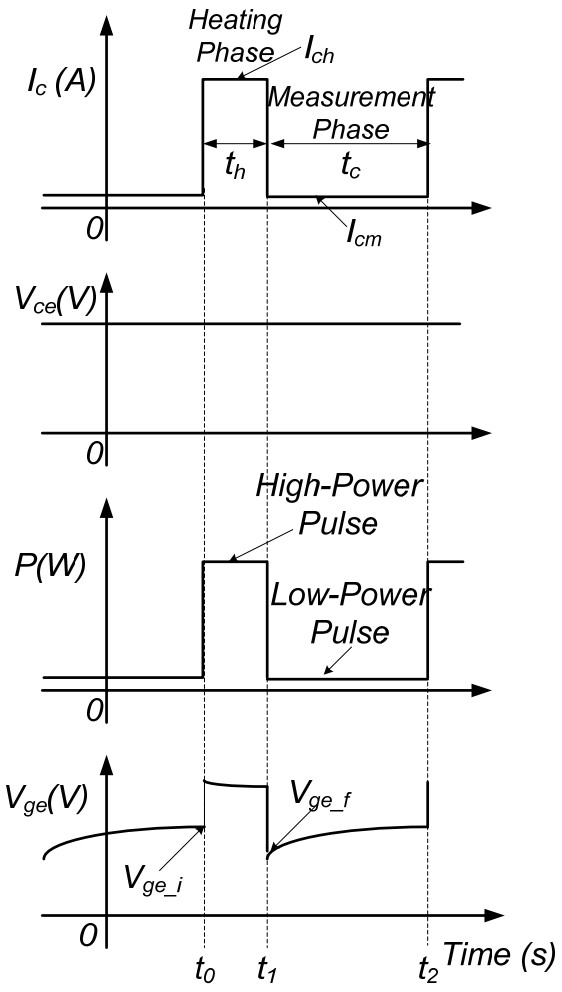


Figure 4-6. The waveforms from the thermal impedance measurement.

The waveforms for thermal impedance measurement are shown in Figure 4-6. In the heating phase (0 - t_0), S_1 in the sensing network is turned on so that the total sensing resistance of the network is approximately equal to R_{s1}. Thanks to the small value of R_{s1}, a large collector current $I_{ch} = V_s/R_{s1}$ flows through the IGBT to heat it up. The power dissipation in the IBGT is

$$P = I_{ch} \cdot V_{ce} = \frac{V_s \cdot V_{ce}}{R_{s1}} \tag{4-2}$$

Under the control of the feedback loop, both the collector current I_{ch} and the voltage across

the IGBT V_{ce} can be regulated to be constant in spite of the temperature dependency of the IGBT characteristics. As a result, the power dissipation in the IGBT during the heating period is constant. This can eliminate measurement error brought by variation of power dissipation of IGBT, which could be induced by the characteristic difference of samples and different junction temperatures.

During the cooling phase (t_0 - t_1), S_1 is turned off. Therefore, the sensing resistance of the network drastically increases from R_{s1} to R_{s2}. Since the voltage reference in the feedback loop does not change, the current flowing through the IGBT is reduced to measurement current I_{cm}, which is equal to V_s/R_{s2}. The junction temperature of the IGBT can then be measured during this period by measuring the change of V_{ge}. The measurement current I_{cm} must be large enough to ensure that the device is turned on but not so large as to cause significant self-heating.

In the waveform of V_{ge} shown in Figure 4-6, V_{ge_i} is the gate voltage before the heating pulse and V_{ge_f} represents the gate voltage after the heating pulse with the width of t_h. Thus, the thermal impedance of the sample at time t_h can be calculated

$$Z_{th}(t_h) = \frac{V_{ge\_i} - V_{ge\_f}(t_h)}{K \cdot P} \tag{4-3}$$

By changing the width of the heating pulse t_h, the curve of thermal impedance vs time can be plotted.

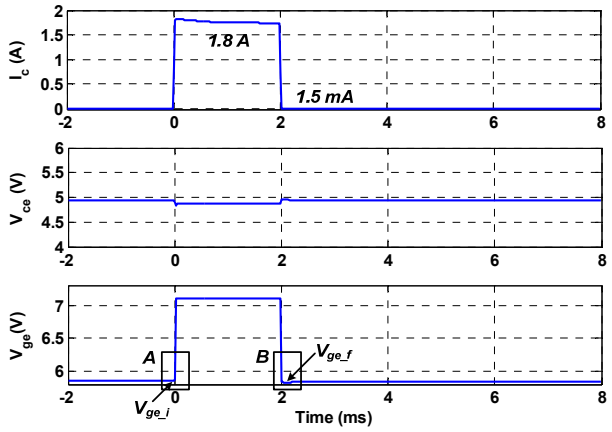
4.3. Experimental Results of Thermal Impedance Measurement

Based on the schematic diagram in Figure 4-5, a control board was made for thermal impedance measurement. The components used on the board are listed in TABLE II. MOSFET CSD16413 with on-resistance of 4.1 mΩ from Ciclon Semiconductor was employed for the switch S_1. The two resistors R_{s1} and R_{s2} (shown in Figure 4-5) were set to be 25 mΩ and 36 Ω, respectively, which set the heating current and the measurement current to be 1.8 A and 1.5 mA. Figure 4-7(a) shows the measurement waveforms of the IGBT with 2 ms heating pulse. It can be seen that the power dissipation in the IGBT was

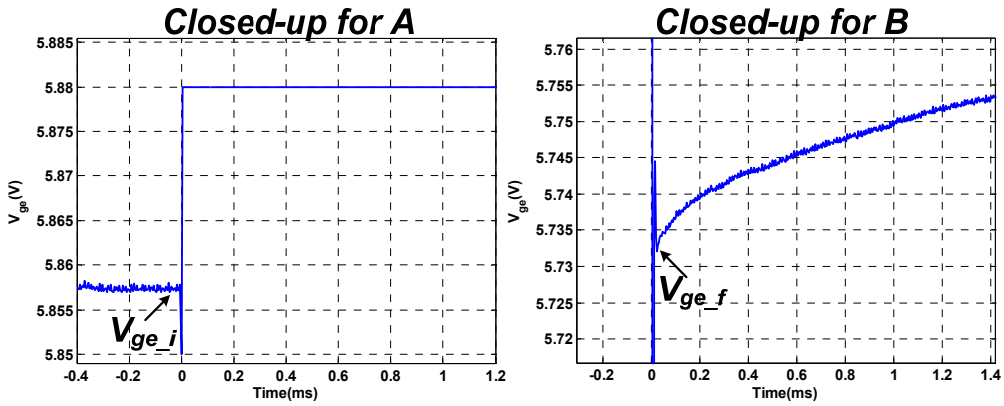
regulated to be around 9 W during the heating phase. V_{ge_i} and V_{ge_f} can be read from Figure 4-7(b) so that the thermal impedance with 2 ms heating pulse can be calculated.

To check whether the measurement set-up can discriminate thermal performance difference in the die-attach layer, a sample was fabricated with a small piece of Kapton tape (1.5 mm×1.5 mm) embedded in the die-attach layer (shown in Figure 4-8). The Kapton tape covers around 11.7% of the total bonding area (3.5 mm×5.5 mm). Compared to the SAC305 solder paste used for die-attach, the thermal conductivity of the Kapton tape is much lower (0.12 W/(m·˚C)), resulting in an increase of the thermal resistance in the die-attach layer.

In the test set-up, the sample is mounted on a heat-sink via thermal grease, which may induce variations from sample to sample. Based on the heat propagation rate in different materials reported in [84], the heat propagation times in silicon die and in DBC substrate are around 2 ms and 40 ms, respectively. Therefore, the maximum width of the heating pulse should be less than 42 ms to minimize the interference from the attachment between the sample and the heat-sink. In this experiment, thermal impedances of the samples were measured with 500 us, 2 ms, 5ms, 10 ms, and 20 ms heating pulse and the results are shown in Figure 4-9.It clearly shows that for 20 ms heating pulse, the thermal impedance of the sample with Kapton tape embedded is around 8% higher than that of the sample without Kapton tape. This indicates that the thermal impedance measurement results obtained from the test set-up can be used to evaluate the bonding quality of die-attach layer. For a heating pulse shorter than 2 ms, as expected, the thermal impedances for these two samples are the same, which agrees with the propagation time in the IGBT.



(a)



(b)

Figure 4-7. Experimental waveforms for thermal impedance measurement of the sample in Figure 4-3: (a) waveforms of the IGBT; (b) closed-up waveforms of V_{ge} .

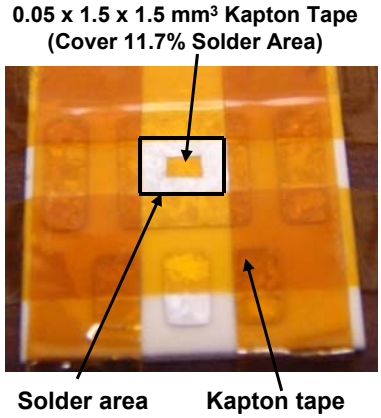


Figure 4-8. Sample with Kapton tape embedded in the die-attach layer.

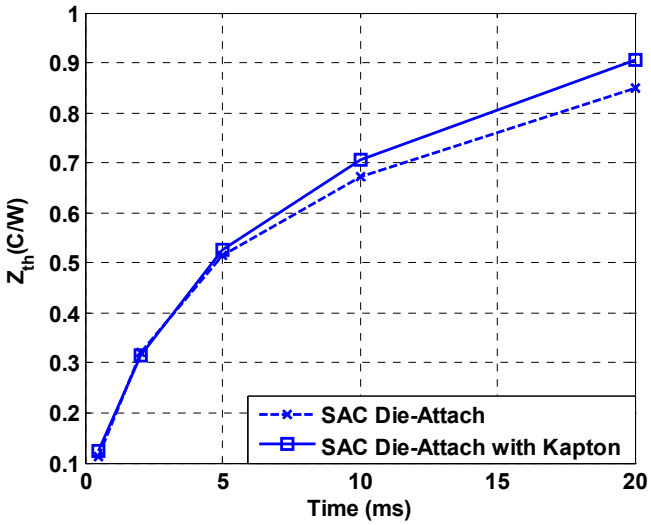


Figure 4-9. Thermal impedance of SAC die-attach samples

Since there are some noises in the experimental waveforms when obtaining gate-emitter voltage, the raw waveforms of V_{ge} need to be processed to get $Z_{th}(t_h)$. V_{ge_i} was acquired by averaging the gate-emitter voltage before the heating pulse in 0.2 ms. The influence of the noises on the obtained V_{ge_i} can be eliminated with this method. After the heating pulse is applied on the IGBT, there are some noises caused by the large change of the collector current (from 1.8 A to 1.5 mA) as shown in Figure 4-10(a). Thus, V_{ge_f} cannot be acquired directly from the experimental data. Based on the ideal transient thermal dissipation, the junction temperature of the IGBT, which corresponds to V_{ge} is linear with respect to the square root of the cooling time after the heating pulse [85]. Therefore, V_{ge} is also linear with respect to the cooling time. From the linear regression between V_{ge} and the square root of the cooling time after the heating pulse, V_{ge_f} can be found by extrapolating the line to 0 ms as shown in Figure 4-10(b).

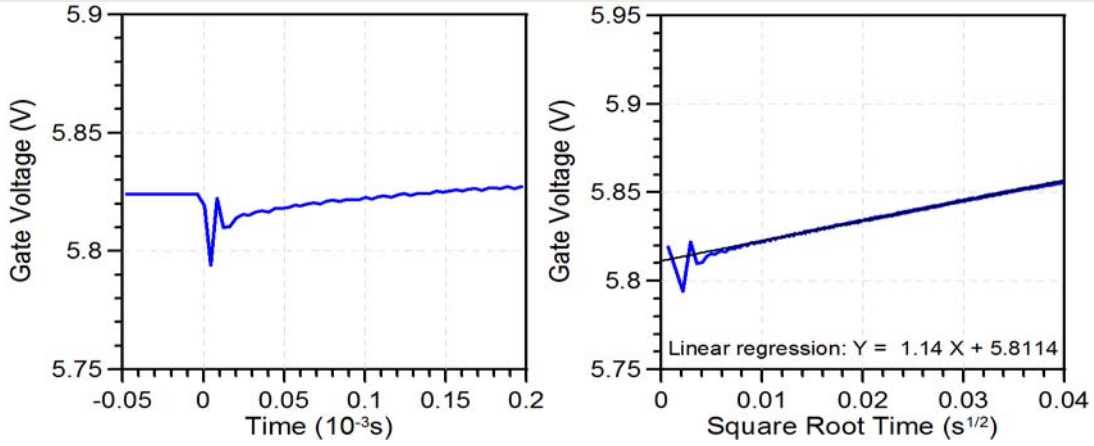


Figure 4-10. Extrapolation of V_{ge_f} from the raw data: (a) raw data of V_{ge_f}; (b) linear regression of V_{ge_f} vs square root of the time.

4.4. Evaluating Degradation of Die-Attach Materials Using Thermal Impedance

Design of Measurement System for Thermal Impedance

Die-attach integrity is highly dependent on the quality of the die-attach material, interfaces, and surfaces. Reliability tests, such as thermal cycling can cause degradation such as crack, delamination, and growth of the voids at the die-attach layer, resulting in an increase of the thermal impedance. Therefore, the test set-up developed in this chapter can be employed to evaluate the bonding quality of different die-attach materials.

Three samples were made using different die-attach materials: SAC305 solder paste, SN100C solder preform processed with vacuum reflow, and sintered nano-silver paste. The properties of these three materials are listed in TABLE 4-2. For each sample, an IGBT die is attached on a silver-plated copper block with a thickness of 6 mm, as shown in Figure 4-11. The coefficient of thermal expansion (CTE) mismatch between the thick copper substrate and the silicon die can induce large thermo-mechanical stress during the thermal cycling, which accelerates the degradation of the die-attach layer.

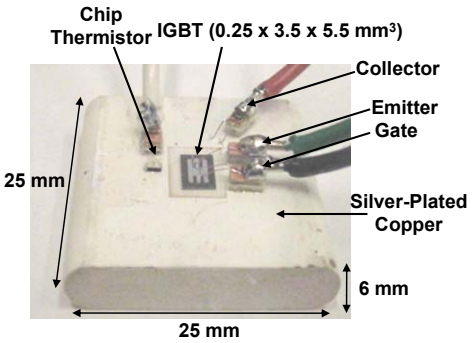


Figure 4-11. Sample used for thermal cycling test.

TABLE 4-2. PROPERTIES OF DIFFERENT DIE-ATTACH MATERIALS

Material	Thermal Conductivity (W/(m·˚C))	Melting Points (˚C)
SAC305 Solder	57.8	217
SN100C Solder	64.0	227
Nano-silver Paste	100	960

The thicknesses of the bonding line for these samples were measured to be 50 μm. The measurement results of thermal impedance for these three samples before thermal cycling are shown in Figure 4-14. Thanks to the high thermal conductivity of the bulk material and the low interfacial thermal resistance, the sample with sintered nano-silver has the lowest thermal impedance (12.1% lower than SAC305 sample and SN100C sample with 40 ms heating pulse). The sample with the SAC305 solder has a similar thermal impedance to the sample with the SN100C solder.

Three samples with different die-attach materials have been thermally cycled using the profile recommended by the JEDEC standard (shown in Figure 4-15) [86]. The temperature range of the cycling is from -40˚C to 125˚C. The dwelling time at extreme temperatures is 10 minutes. It takes 100 minutes to finish one cycle. The thermal impedances of the samples were measured after every 100 cycles.

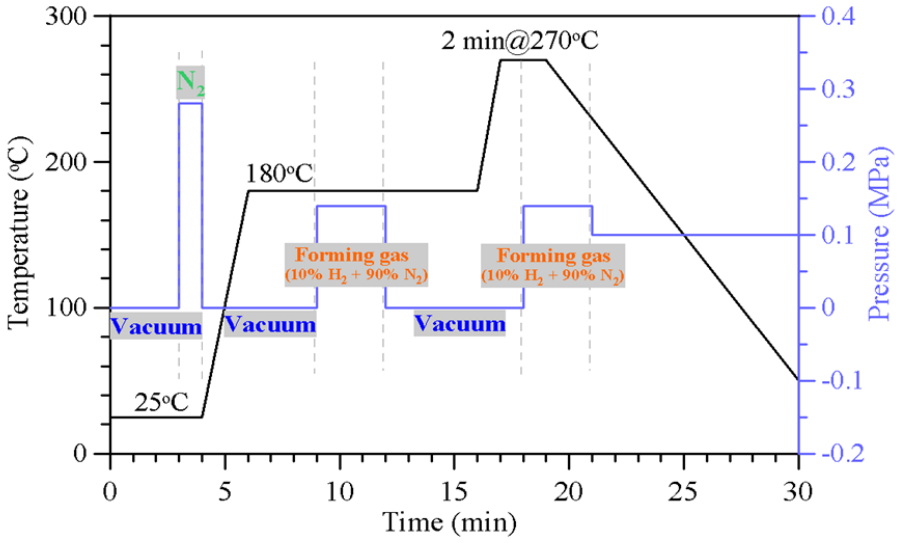
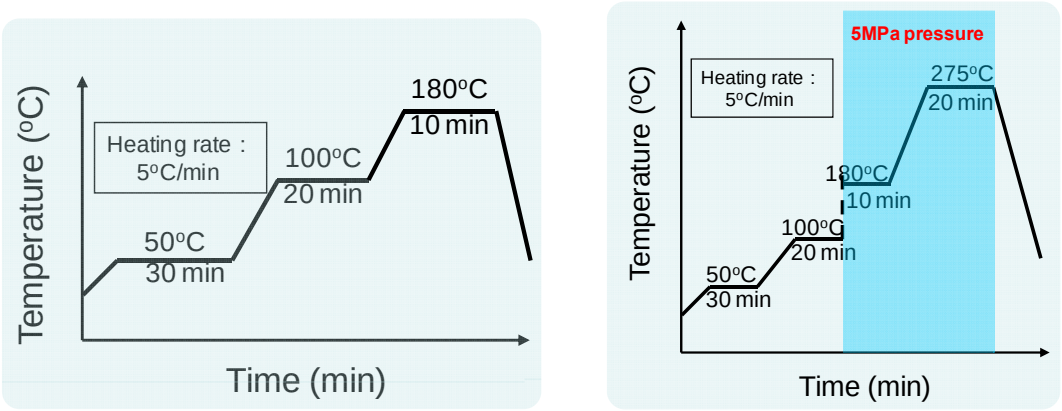


Figure 4-12. Temperature profile for reflow of lead-free solders.



(a) (b)

Figure 4-13. Heating profile of nanosilver attached IGBT devices: (a) drying profile and (b) sintering profile.

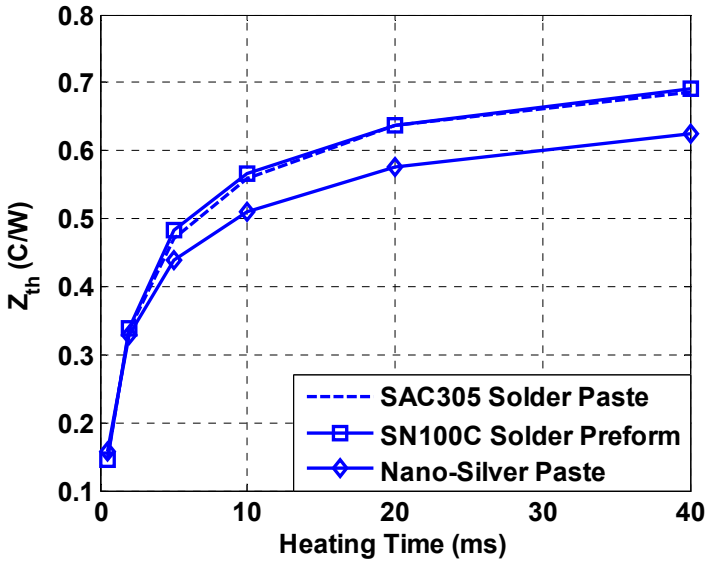


Figure 4-14. Thermal impedance of samples with different die-attach materials before cycling (dimensions of the joint: 3.5 mm × 5 mm × 0.05 mm; reflow profile for solders shown in Figure 4-12 and sintering profile for nano-silver paste shown in Figure 4-13).

Thermal impedances of the samples after thermal cycling are shown in Figure 4-16. It can be seen that for the samples using solder, thermal impedances have a noticeable increase after 200 cycles, which keeps increasing with acceleration after that. For the sample using sintered nano-silver, thermal impedance only increased by 4% after 400 cycles. The changes of the thermal impedance are described in Figure 4-17. For the sintered nano-silver sample, the thermal impedance increases as the cycling number increases. However, after 400 cycles, the thermal impedance of the sample tends to be stable without further increasing. As a result, the thermal impedance of the sintered nano-silver sample only increased by 4.1% after 500 cycles. For the two samples using solder as the die-attach material, the thermal impedance of the samples increase dramatically after thermal cycling. The thermal impedance of the samples using the SAC305 solder paste and using the SN100C solder preform increased 7.8% and 15% after 400 cycles, respectively. From Figure 4-17, it also can be seen that the thermal impedance of the solder samples still keeps increasing along the number of thermal cycling. Similar observations were reported in [87] after the samples were stressed using

power cycling. After 500 cycles, the thermal impedance of the SAC305 sample further increased by 5% to 12.8%. For the SN100C sample, the large thermo-mechanical stress caused by thermal cycling damaged the IGBT die after 400 cycles. The measurement shows that the resistance between the gate and the emitter of the sample dropped to 1.5 Ω after 500 cycles.

The experiment results show a lower thermal impedance and less degradation after thermal cycling using the nano-silver paste, which is brought by its high thermal conductivity and porous structure. The two samples using the solder as the die-attachment have a similar thermal impedance before thermal cycling. However, after 200 cycles, the thermal impedance of the SN100C sample increases dramatically compared to the SAC305 sample, which implies that the joint of SN100C solder preform has more cracks or delaminations induced by thermal cycling. This could be caused by the oxidation of the sample surface before the solder reflow. In the SAC305 solder paste, the flux can help remove the oxidation layer to improve the wettability of the bonding surface. However, due to the lack of flux in the SN100C solder preform, the oxidation of the bonding surface can lead to poor wettability. As a result, the die-attach of the SN100C sample degrades faster than that of the SAC305 sample.

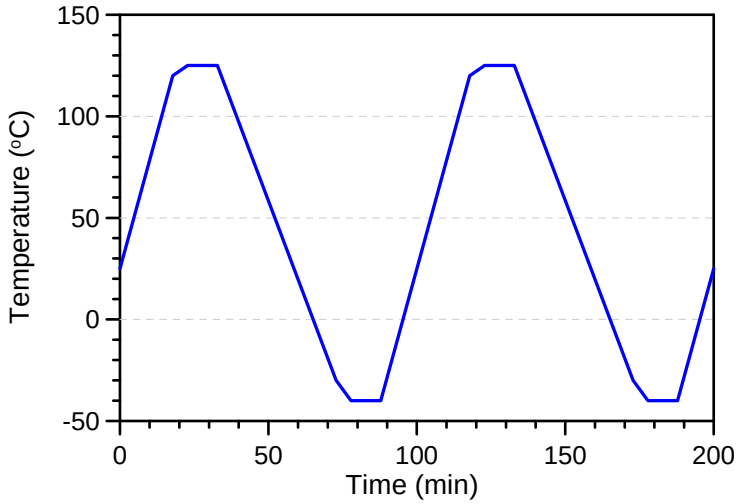


Figure 4-15. Thermal cycling profile used for reliability test.

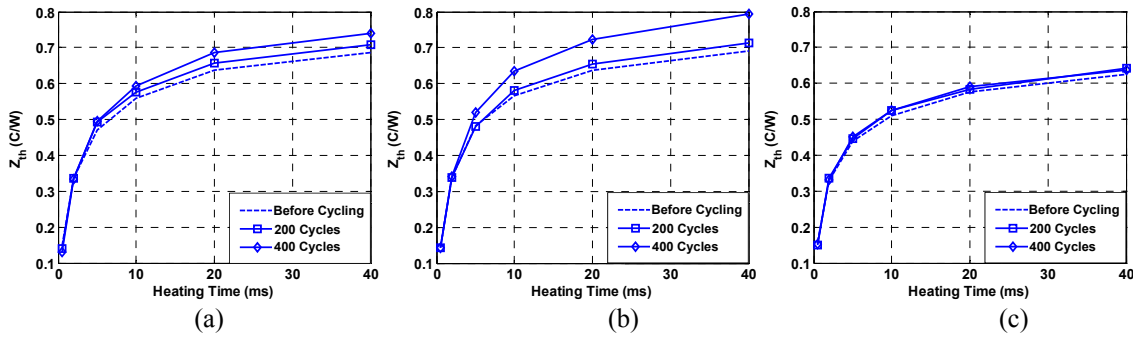


Figure 4-16. Thermal impedance of sample using different die-attach materials after 400 cycles: (a) SAC305 solder paste; (b) SN100C Solder preform; (c) Nano-silver paste (dimensions of the joint: 3.5 mm × 5 mm × 0.05 mm; reflow profile for solders shown in Figure 4-12 and sintering profile for nano-silver paste shown in Figure 4-13).

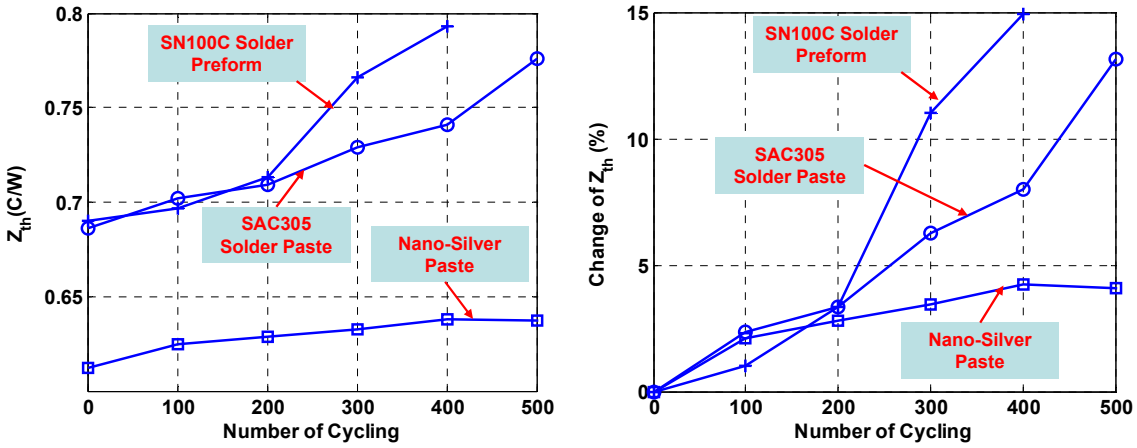


Figure 4-17. The change of thermal impedance (a) and the percentage change of thermal impedance (b) for the samples with different die-attach materials after 500 cycles (dimensions of the joint: 3.5 mm × 5 mm × 0.05 mm; reflow profile for solders shown in Figure 4-12 and sintering profile for nano-silver paste shown in Figure 4-13; thermal cycling profile shown in Figure 4-15).

4.5. Conclusions

In this chapter, a thermal impedance measurement system is developed to characterize the thermal performance of three die-attach materials. The gate-emitter voltage of IGBT with the K-factor of 10 mV/˚C is employed as a temperature sensitive parameter for thermal impedance measurement, which is much more sensitive to

temperature than the forward voltage of the pn junction. In addition, the power dissipation in the IGBT is regulated by the feedback control loop in the test set-up regardless of the junction temperature. This can significantly improve the measurement accuracy.

With the developed measurement system, the thermal impedance of the three samples with different die-attach materials are measured and compared. Results show that the sample using the nano-silver paste as the die-attach has the lowest thermal impedance (12.1% lower than SAC305 sample and SN100C sample for 40 ms heating pulse).

Samples with different die-attach materials have been thermally cycled from -40˚C to 125˚C and the degradation of the die-attach layer was evaluated using thermal impedance measurement. The results show that after 500 cycles, the thermal impedance of the sintered-silver sample only increased by 4.1%, which is more than 10% lower than that of the soldered samples.

Chapter 5. A PLANAR POWER MODULE WITH LOW THERMAL IMPEDANCE

In this chapter, it was found that the conventional single-sided power module with wirebond connection cannot achieve both good steady-state and transient thermal performance under high heat transfer coefficient conditions. As a result, a planar power module with plate bonding is designed to resolve the issue. In the proposed planar power module, the semiconductor device is sandwiched between two substrates and a copper plate is inserted on the top of the semiconductor to serve as thermal mass. The comparison of thermal performance for conventional power module and planar power module is presented. The results clearly show that the proposed planar power module has both better steady-state and transient thermal performance than the wirebonded power module.

However, due to CTE mismatch between the copper plate and the silicon device, large thermo-mechanical stress could be induced in the bonding layer of the power module. The stress distribution in a three-layer structure was analytically analyzed. It is found that the stress concentrates at the edge of the bonding layer and with increasing of thickness or footprint area of the copper plate, the maximum stress in the bonding layer increases. The detailed analysis of the thermo-mechanical stress distribution in the power module is presented in Chapter 6.

5.1. Thermal Performance Limitation of Conventional Wirebonded Power Module

Figure 5-1 shows the typical structure for a wirebonded power module. The heat-spreader is attached underneath the power module to spread the heat to a large area, leading to smaller thermal resistance. However, the heat-spreader also increases the

thermal resistance in the vertical direction as shown in Figure 5-1. These two contradictory effects work on the power module simultaneously. The overall impact of the heat-spreader depends on which effect dominates. For the cases with low heat transfer coefficient, the heat-spreading area can be significantly increased by using heat-spreader. Therefore, the spreading effect will be dominant. Figure 5-2 shows the changing of the thermal resistance when the thickness of the heat-spreader varies. It can be found when the thickness of the heat-spreader increases from 1 mm to 5 mm, the total thermal resistance of the power module with heat transfer coefficient of 10000 W/(m^2·°C) reduces by 12% (dash-line in Figure 5-2). However, for the power module with high heat transfer

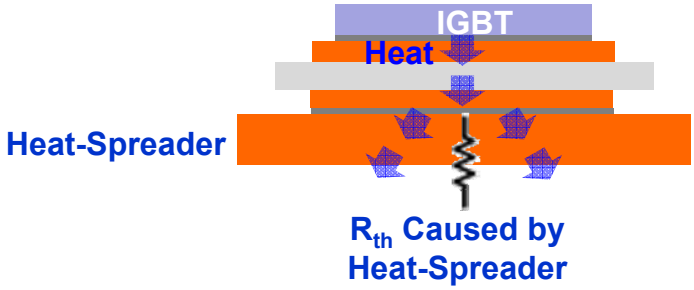


Figure 5-1. Impacts of the heat-spreader in the power module.

coefficient (50000 W/(m^2·°C)), increasing the thickness of the heat-spreader does not necessarily result in reduction of the thermal resistance. As described by the solid line in Figure 5-2, the thermal resistance of the power module with 5 mm thick heat-spreader is actually slightly higher than that with 1 mm thick heat-spreader. This shows that under high heat transfer coefficient, the benefit brought by the spreading effect has been outweighed by the increase of the thermal resistance in vertical direction. Therefore, when high performance heat-exchanger is installed under the power module, from the steady-state point of view, the heat-spreader should be eliminated. In addition, removal of the heat-spreader also can eliminate one interface layer that is used to attach the heat-spreader to the heat-exchanger and simplify the process. This interface layer involves large-area bonding that usually causes reliability issue in thermal cycling test.

Therefore, removal of the interface layer also helps improve reliability of the power module.

However, another very important function of the heat-spreader is to absorb the thermal energy during the transient. Although removal of the heat-spreader can benefit the steady-state performance of the power module for high heat transfer coefficient case, it will degrade the transient thermal performance of the power module as shown in Figure 5-3. Without the heat-spreader, due to lack of sufficient thermal mass, the junction temperature of the power module could be 10˚C higher for power dissipation of 200 W in the IGBT.

From above analysis, it can be seen that conventional wirebonded power module cannot achieve both good steady-state and transient thermal performances. Thus, a new structure is desired for the power module.

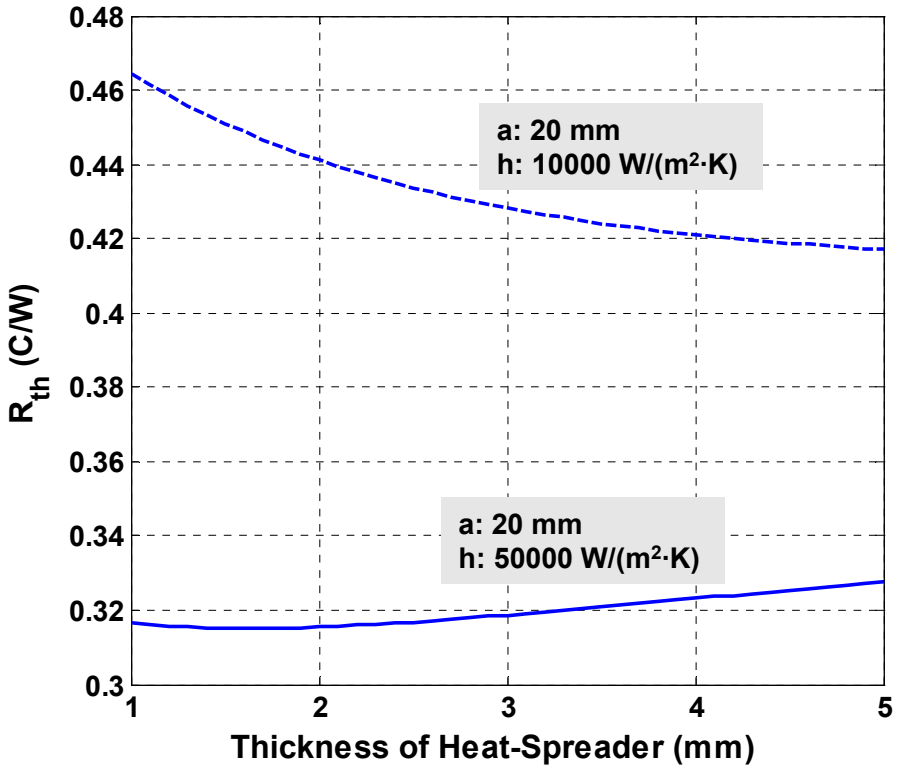


Figure 5-2. Finite element analysis of impacts of the heat-spreader on thermal resistance under different heat transfer coefficient (the structure used in the simulation shown in Figure 5-4).

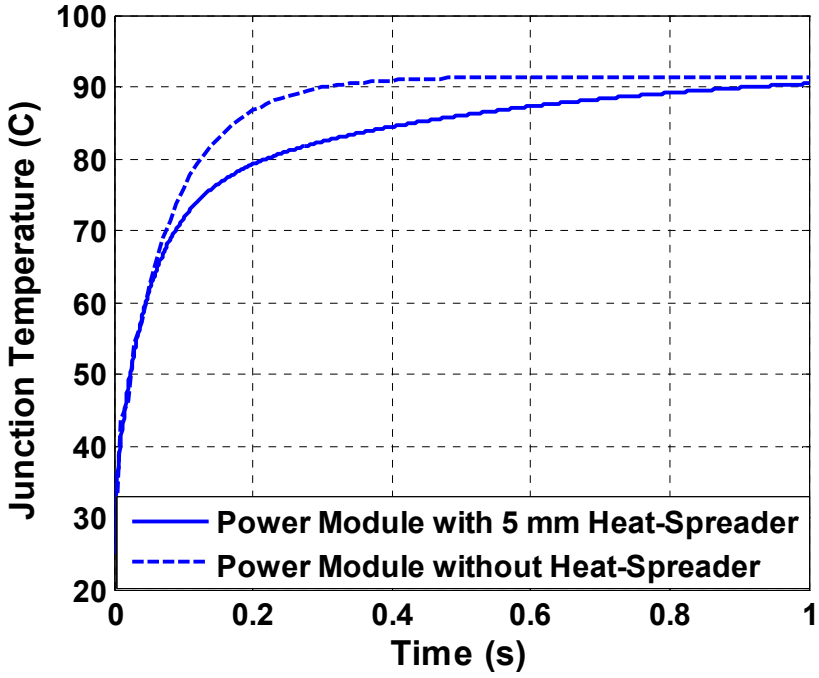


Figure 5-3. Finite element analysis of impacts of the heat-spreader on transient thermal performance of the power module (h = 50000 W/(m^2·°C) and power dissipation: 200 W; the structure used in the simulation shown in Figure 5-4).

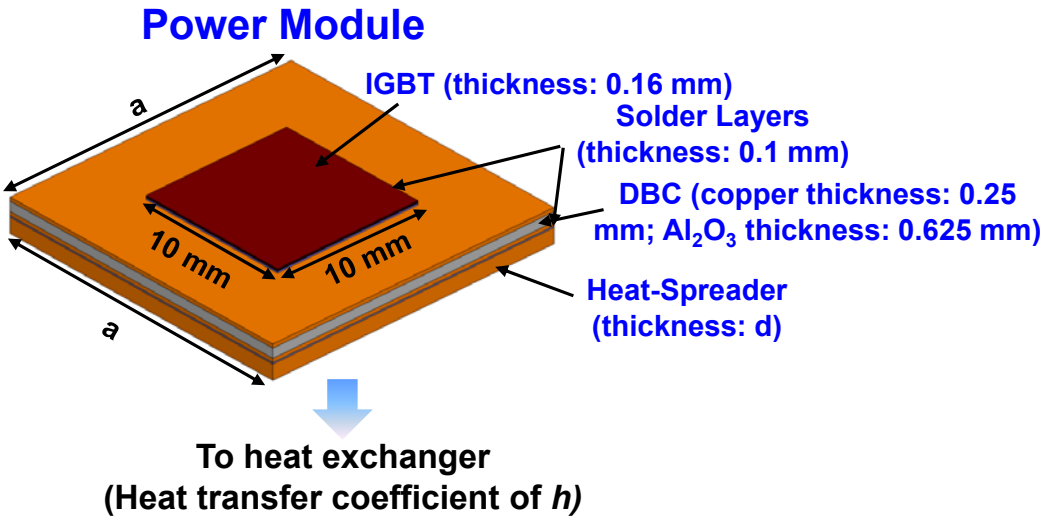


Figure 5-4. Structure used in the simulations for Figure 5-2 and Figure 5-3.

5.2. A Planar Power Module with Improved Thermal Performance

In recent years, much progress has been made in the design of planar packaging techniques for power modules. This is due to the planar packaging's potential for achieving higher power density and better thermal and electrical performance than conventional wirebond packaging [88]-[91]. Among the planar structures, the plate-bonded power module as shown in Figure 5-5 has the potential to achieve both good steady-state and transient thermal performances [10]. In plate-bonded power module, semiconductor dice are sandwiched between two DBC substrates and copper plates are employed for interconnecting dice and the top substrate. Thanks to large thermal mass provided by the copper plates, the transient thermal performance of the power module can be significantly improved. Since the top DBC substrate also serves as thermal mass, the thickness of the copper plate can be reduced compared to the thickness of the heat-spreader in the single-sided power module. In addition, thanks to absence of heat-spreader and extra thermal interface layer in the bottom thermal path of the module, the steady-state thermal resistance will not be degraded.

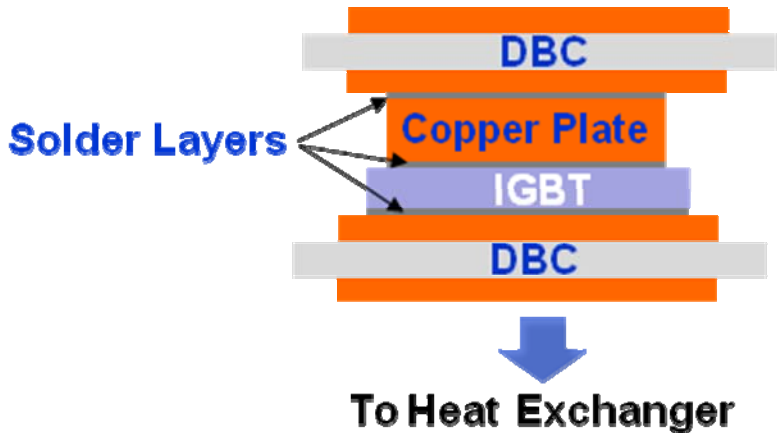


Figure 5-5. Plate-bonded power module to achieve better thermal performance.

Figure 5-6 shows the transient thermal performance of the plate-bonded module with only 1 mm thick copper plate on the dice. It can be seen that for 0.2 s transient, the junction temperature of the IGBT in the plate-bonded module can be 28°C lower than that of the conventional power module with 5 mm heat-spreader. The latest power module from Semikron, SKiiP 38NAB12T4V1, which employs the state-of-art SKiiP packaging technology [31] has thermal impedance of 0.31°C/W for 0.2 s transient [92]. It can be seen that with the proposed structure, the thermal impedance of the power module can be reduced to 0.14°C/W. This is because of sufficient thermal mass in the power module and low thermal resistance from the heat dissipation path.

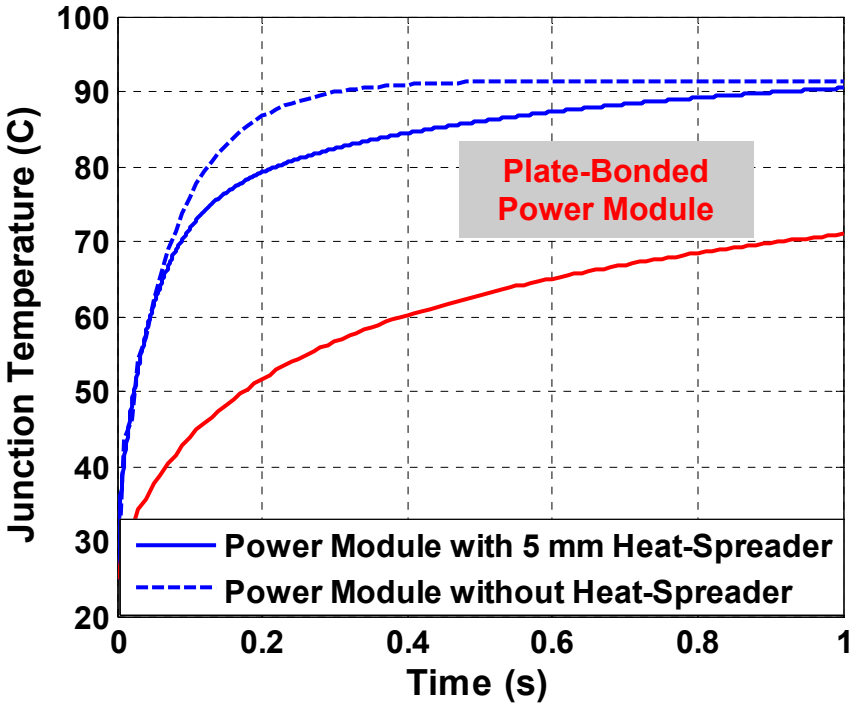


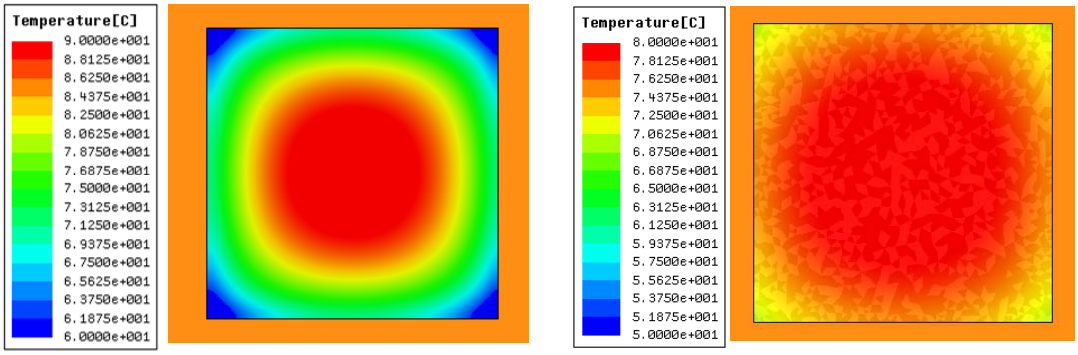
Figure 5-6. Better transient thermal performance achieved by the plate-bonded power module shown in finite element simulation (h = 50000 W/(m^2·°C) and power dissipation: 200 W).

For the thermal resistance, the comparison of three different power modules is shown in TABLE 5-1. The difference between the thermal resistances of two single-sided power modules is negligible, which clearly shows that there is no benefit on the thermal

resistance brought by the heat-spreader. However, compared to the single-sided power modules, the plate-bonded module shows remarkable advantage even in steady-state thermal performance. This is because the copper plate can help to make the heat flux distribution in the IGBT more evenly so that the hot-spot can be eliminated. This can be found in the comparison of the temperature contour on the top surface of the IGBT for two different power modules (shown in Figure 5-7). It can be seen that the plate-bonded module can achieve both better steady-state and transient thermal performance compared to the single-sided power module.

TABLE 5-1. COMPARISON OF THERMAL RESISTANCE FOR SINGLE-SIDED POWER MODULE AND PLATE-BONDED MODULE

	Single-Sided Power Module with 5 mm Heat-Spreader	**Single-Sided Power Module without Heat-Spreader**	**Plate-Bonded Power Module**
Thermal Resistance (°C/W)	0.330	0.333	0.280



(a) (b)

Figure 5-7. Temperature contour on the IGBT in finite element simulation for (a) single-sided power module with heat-spreader and (b) plate-bonded module.

5.3. *Analytical Analysis of Thermo-mechanical Stress in Plate-Bonded Power Module*

Due to the large CTE (coefficient of thermal expansion) mismatch among materials in the plate-bonded module, different layers tend to have different deformations under thermal cycling. The thick copper plate on the top of the semiconductor device could induce high thermo-mechanical strain and stress in the bonding layers. The CTE values of materials used in the plate-bonded module are listed in TABLE 5-2. Thermal stresses have significant impact on the reliability and lifetime of the power module [93]. The bonding interfaces of the layered structures suffer from high stress concentrations, which eventually lead to the cracking of the bonding layer or interfacial delamination.

TABLE 5-2 CTE OF MATERIALS USED IN THE POWER MODULE

Materials	*Copper*	*AlN*	*Solder*	*Silicon*
CTE (ppm/°C)	16.7	4.5	20.5	2.5

Since the plate-bonded power module has a multi-layered structure, to understand the thermo-mechanical stress distribution in the power module, it is necessary to study the stress distribution in a three-layer structure as shown in Figure 5-8(a). In Figure 5-8(a), a copper layer with the thickness of t_1 is attached to a silicon layer with the thickness of t_2 via the solder layer, which has thickness of t_0. To simplify the analysis, the cross-section of the three-dimensional structure in Figure 5-8(b) can be used. For the structure in Figure 5-8(b), if the elastic deformation and bending effect are considered, based on the equilibrium of force and moment, the shear stress at the interfacial layer can be derived as [94]:

$$\tau = \frac{k(\alpha_1 - \alpha_2)\Delta T}{\lambda \cosh(kl)} \sinh(kx) \tag{5-1}$$

where $k = \sqrt{\frac{\lambda}{\kappa}}$, $\lambda = \frac{1-\nu_1}{E_1 t_1} + \frac{1-\nu_2}{E_2 t_2} + \frac{(t_1 + t_2 + t_0)^2}{4D}$, $\kappa = \frac{t_1}{3G_1} + \frac{2t_0}{3G_0} + \frac{t_2}{3G_2}$,

and $D = \sum_{i=0}^{2} \frac{E_i t_i^3}{12(1-\nu_i)}$.

In the above equations:

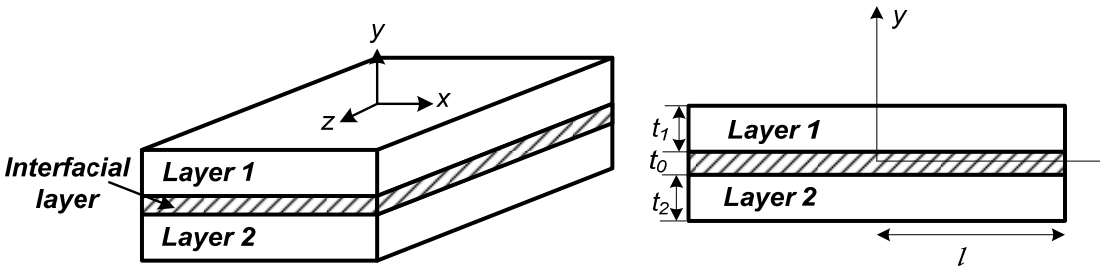
α_i: Coefficient of Temperature Expansion (CTE);

ν_i: Poisson's ratio;

E_i: Young's modulus;

G_i: shear modulus; and

ΔT: temperature change.

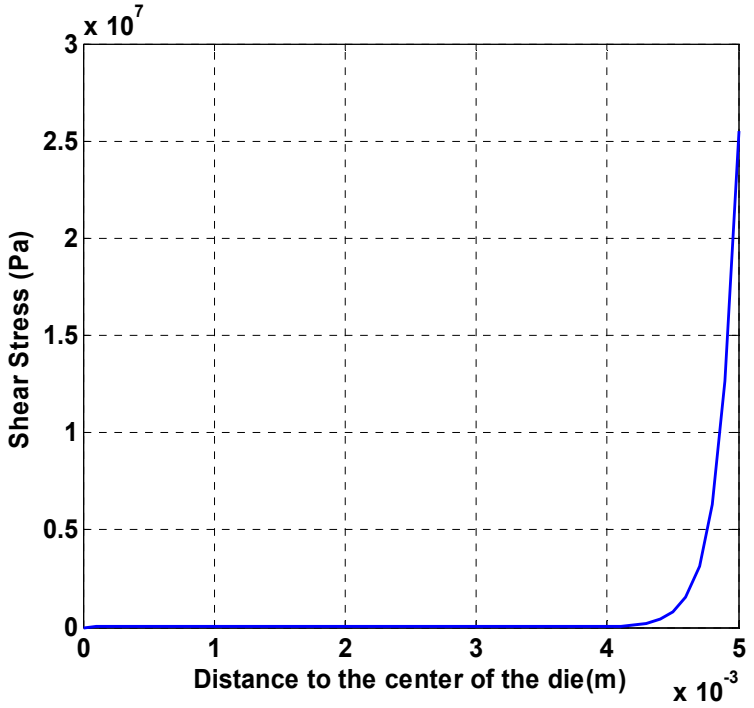


(a) (b)

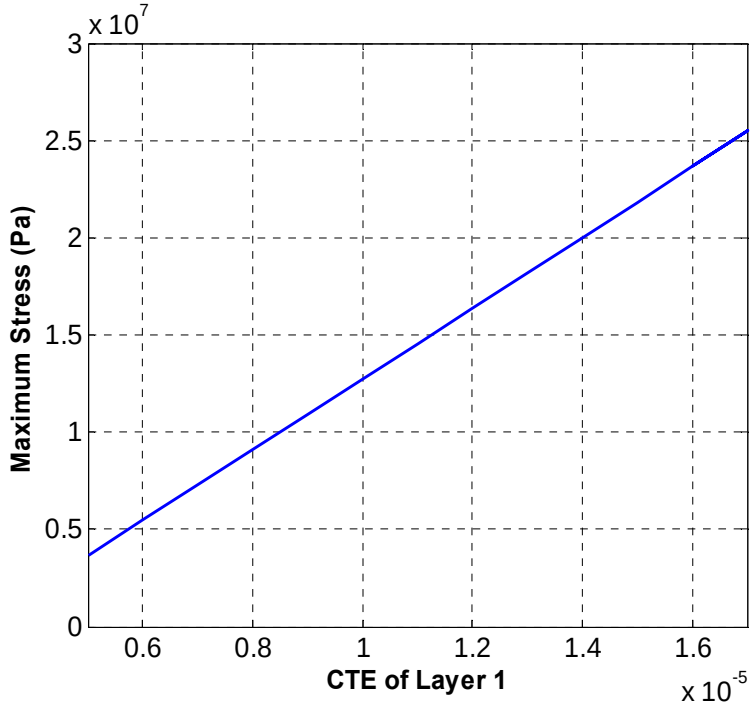
Figure 5-8. Structure used for analytical thermal stress analysis (a) Three-layer structure; (b) Cross-section of three-layer structure.

The shear stress in the solder layer can be calculated based on equation (5-1). Figure 5-9(a) shows the shear stress distribution at different locations in the interfacial layer. It can be seen that the edge of the solder layer suffers higher stress than the center of the solder layer. This indicates that the weak point of the interfacial layer is at the edge near the corner of the structure. Figure 5-9(b) shows the maximum stress vs the CTE of layer 1. Higher CTE mismatch between layer 1 and layer 2 results in high stress in the solder layer. Figure 5-9(c) describes the maximum stress in the solder layer with different thicknesses of copper plate. The figure indicates that with the increase of the copper plate thickness, the stress in the solder layer increases correspondingly. However, the structure used in Figure

5-8 is much simpler than a real power module. In addition, only elastic deformation is considered in (5-1). Therefore, Figure 5-9 can only provide a qualitative analysis of the thermo-mechanical stress in the power module. To obtain an accurate thermo-mechanical stress distribution in the power module, finite element method (FEM) simulation must be used.



(a)



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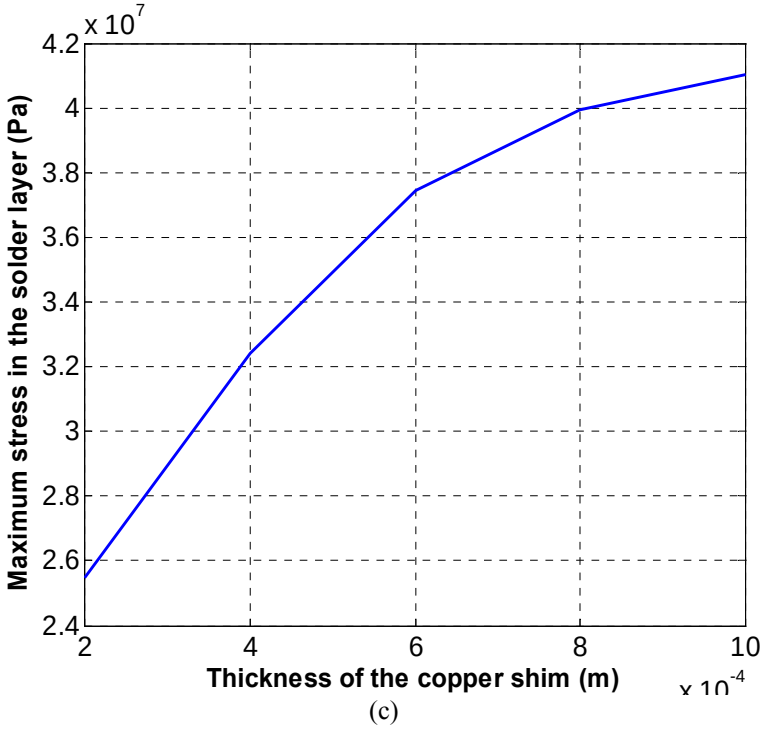


(c)

Figure 5-9. Shear stress distribution in the layered structure: (a) Stress vs distance to the center of the device (t_0=0.1 mm *;* t_1=t_2=0.2 mm); (b) Stress vs CTE of layer 1; (c) Stress vs thickness of the copper plate (t_0=0.1 mm ; t_2=0.2 mm).

5.4. Conclusion

In this chapter, the steady-state and transient thermal performances of a single-sided wirebonded power module were analyzed. It was found that the conventional single-sided wirebonded power cannot achieve both good steady-state and transient thermal performance under high heat transfer coefficient condition. Therefore, a planar plate-bonded power module was proposed to improve both steady-state and transient thermal performance. Compared to conventional single-sided power module, the plate-bonded module has more thermal mass provided by the top substrate and the copper posts on the silicon dice, resulting in 28°C lower in junction temperature for 0.2 s transient. In addition, the copper plates also eliminate the hotspot on the silicon dice, which helps to improve the steady-state thermal performance as well. Although plate-bonded power module achieves better thermal performance than the conventional wirebonded power module, the high thermo-mechanical stress in the power module can cause reliability issue. The thicker and larger copper plate results in higher stress. Therefore, a means to reduce the stress of the plate-bonded power module is required.

Chapter 6. POWER MODULE USING TRENCHED PLATE TO LOWER THERMO-MECHANICAL STRESS

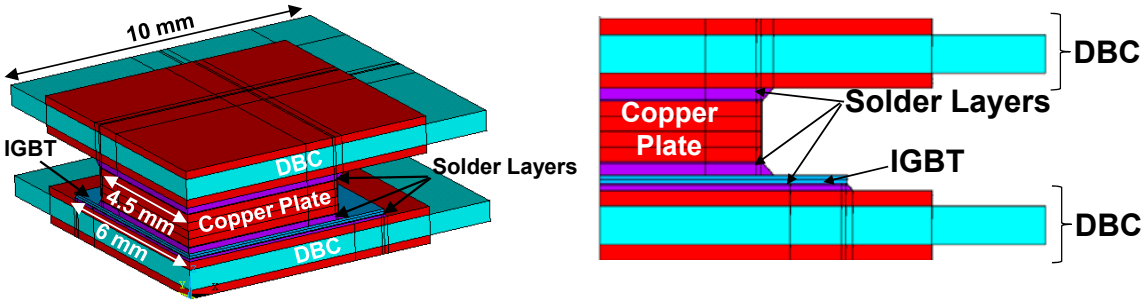
In the last chapter, the analysis shows that the plate-bonded power module has better steady-state and transient thermal performance than the conventional wirebonded power module. However, the copper plate could induce high thermo-mechanical stress in the power module, leading to poor reliability. In this chapter, finite element simulation using ANSYS software is performed to study the stress distribution in the plate-bonded power module. The detailed settings for stress simulation such as meshing, material properties, and boundary conditions are presented. From the FEM simulation results, it is observed that the maximum stress in the plate-bonded power module is much higher than that of the conventional wirebonded power module.

Analytical analysis of stress distribution in layered structures suggests that smaller footprint area for copper plates yields lower stress. Therefore, to reduce the stress in the plate-bonded power module, the large copper plate on top of the semiconductor can be partitioned into several smaller pieces which are connected using a thin layer of copper foil. The new structure is called trenched copper plate structure. The parametric study shows that the maximum von Mises stress and plastic strain in the solder layer can be reduced by 18.7% and 67.8%, respectively if the single piece of copper plate is replaced by a 3 × 3 trenched copper plate. However, the thermal mass of the copper plate-array structure is reduced, leading to higher transient peak temperature. The trade-off between transient thermal performance and thermo-electrical performance is also discussed in this chapter.

6.1. Simulation Setting of Thermo-Mechanical Stress

6.1.1. Modeling of Power Module

ANSYS is a powerful tool for thermal, electrical, and thermo-mechanical simulation. In this study, the stress and strain distribution of the plate-bonded power module shown in Figure 5-5 is simulated using ANSYS. In the plate-bonded power module, the IGBT and the copper plate are sandwiched between two DBC substrates. There are three solder layers used in the assembling of the power module. Thanks to the symmetric structure, only one quarter of the power module is used for simulation to save computing time as shown in Figure 6-1. The dimensions of the plate-bonded power module are also shown in Figure 6-1 and TABLE 6-1. The cross-section of the plate-bonded module is shown in Figure 6-1(b). It should be noted that, in practice, the edge of the solder layer is not perpendicular to the substrates. Thus, in this simulation, a 45˚ angle is introduced in the edge of the solder layer (shown in Figure 6-1(b)).



(a) (b)

Figure 6-1. The power module used for thermo-mechanical simulation (a) and the cross-section view (b).

6.1.2. Boundary Conditions

Since the thermal cycling temperature range is from -40˚C to 105˚C [95], the distribution of the mechanical stresses in the power module at the maximum temperature (105˚C) is simulated using ANSYS software. The maximum stress under this condition is an indicator of failure of solder material. Based on Coffin-Manson law, the strain in the

solder layer is directly related to the reliability. Therefore, the stress and strain distributions in the solder layers will be simulated.

TABLE 6-1. THICKNESS OF DIFFERENT LAYERS IN PLATE-BONDED POWER MODULE

Layer		Thickness
DBC thickness	Cu	0.25 mm
	Al_2O_3	0.625 mm
IGBT		0.16 mm
Bottom Solder Layer		0.1 mm
Middle Solder Layer		0.2 mm
Top Solder Layer		0.2 mm

To simulate the thermal-mechanical stress/strain in the power module, a temperature at which the solder layers achieve stress-free state has to be set. The stress-free temperature is generally understood to be lower than the solidus temperature of solder. The stress-free temperature can be further reduced significantly at the assembly stage by controlling the cool-down profile, or after assembly by such processes as thermal cycling, annealing, and so on [96]-[97]. For the purpose of correlating the trend of the maximum stress with the height of the copper plate, 25^{o}C and 85^{o}C were set as stress-free temperatures, and were found lead to the same conclusions. Since the other authors had set their stress-free states at 25^{o}C [98]-[99], this temperature was used in the simulation to facilitate comparison of results.

The boundary conditions of the simulation are also critical for the result. Figure 6-2 shows one quarter of the entire structure. To simulate the case that the sample is placed in the thermal cycling chamber, the two surfaces A and B (shown in Figure 6-2) are set to be constrained in x and y directions, respectively. In addition, the origin point O is set to be fixed in all directions.

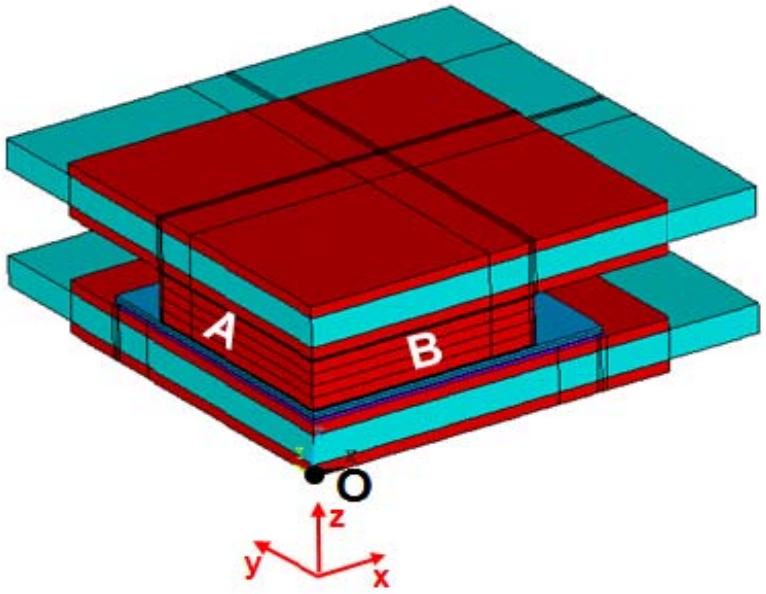


Figure 6-2. Boundary conditions used in thermo-mechanical stress simulation.

6.1.3. Material Properties

In the simulation, the ductile materials in the module have plastic deformation under thermal loading. Thus, the plastic constitutive laws are used for the ductile materials, such as solder and copper. Due to its good wettability and reliability, SAC305 lead-free solder (96.5% tin, 3% silver, and 0.5% copper) are widely used in the industry [100]. Therefore, in this study, SAC305 lead-free solder is used as a bonding material. For the solder layers, Anand model is employed, which has been added to the ANSYS software. Anand model is widely used in thermo-mechanical analysis of electronic packaging. This model is a single-scalar internal variable model for large, isotropic, viscoplastic deformations proposed by Anand [101] and Brown et al. [102]. The Anand constitutive law is described by a flow equation (6-1) and the three evolution equations shown in (6-2), (6-3), and (6-4), which reflect the physical phenomena of strain rate, temperature sensitivity, strain rate history effects, strain hardening, and dynamic recovery during the deformation of the material. The definitions of the parameters and the values used in the ANSYS simulation are shown in TABLE 6-2.

$$\frac{d\varepsilon_{in}}{dt} = Ae^{-\frac{Q}{RT}} \cdot \left[\sinh(\xi \frac{\sigma}{s})\right]^{1/m} \tag{6-1}$$

$$\frac{ds}{dt} = \left\{h_0(|B|)^a \frac{B}{|B|}\right\} \frac{d\varepsilon_{in}}{dt} \tag{6-2}$$

$$B = 1 - \frac{s}{s^*} \tag{6-3}$$

$$s^* = \hat{s}[\frac{1}{A}\frac{d\varepsilon_{in}}{dt}e^{(-\frac{Q}{RT})}]^n \tag{6-4}$$

TABLE 6-2. PARAMETERS USED IN ANSYS SIMULATION [103]

Parameters	Definition	Value
ε_{in}	Plastic strain	-
T	Temperature	-
s	Deformation resistance	-
σ	Stress	-
S_o	Initial value of deformation resistance	2.45 MPa
Q/R	R: universal gas content	6067.3
	Q: activation energy	
A	Pre-exponential factor	717.260 /sec
ζ	Multiplier of the stress	2
m	Strain rate sensitivity of stress	0.13
h_o	Hardening constant	14560 MPa
$\hat{S}$	Coefficient for deformation resistance saturation value	29 MPa
n	Strain rate sensitivity of saturation value	0.0436
a	Strain rate sensitivity of hardening	2.22

For the copper layers, experimental results show that the constitutive law described in (6-5) matches well with the properties of copper [107]. The parameters k and n are dependent on material properties. The values of k and n for copper are shown in TABLE 6-3.

$$\sigma = k\varepsilon^n \tag{6-5}$$

TABLE 6-3. PARAMETERS FOR COPPER CONSTITUTIVE LAW [107]

Symbol	k	n
Value	335	0.256

For brittle materials such as alumina and silicon in the power module, the thermo-mechanical stress induced by thermal cycling is lower than the yield stress. Therefore, only elastic stress and strain are considered for alumina and silicon in the power module. The properties of the brittle materials are summarized in TABLE 6-4.

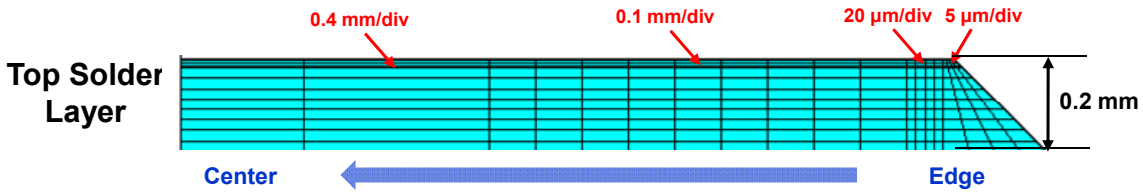
TABLE 6-4. PARAMETERS FOR BRITTLE MATERIALS

Material	CTE	Young's Modulus	Poisson Ratio
Alumina	8.1 ppm	300 GPa	0.21
Silicon	2.6 ppm	185 GPa	0.28

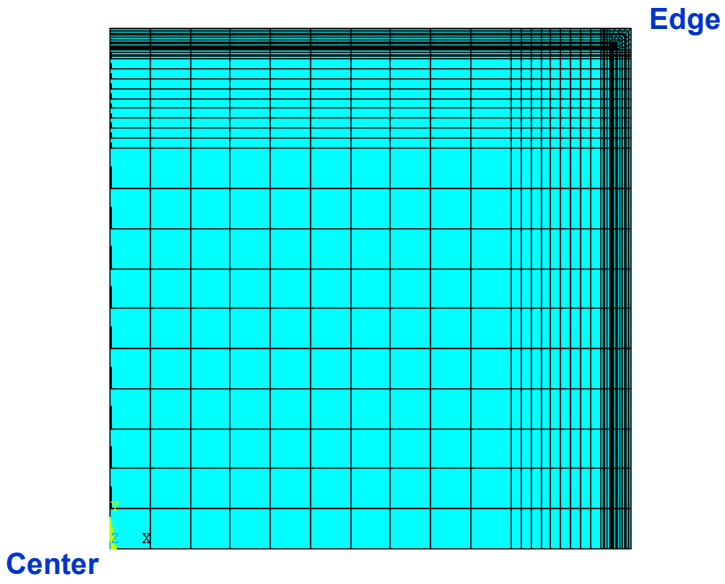
6.1.4. Meshing

The meshing density has significant impact on the accuracy of the result in FEM simulation. Dense mesh results in more accurate simulation results. However, it requires more computing time. In order to achieve better trade-off between computing time and mesh density, fine mesh are only used for critical layers such as solder layers. From the analytical analysis from the last chapter, it can be seen that the edge of the solder layer has the highest stress. Therefore, to obtain the accurate maximum stress in the power module, denser mesh is used at the edge than the center part of solder layers. As shown in

Figure 6-3, from the edge to center of the solder layer, the mesh density gradually decreases from 20 μm/div to 400 μm/div. The hextetrahedral mesh shown in Figure 6-3 makes the simulation easy for convergence. The detailed steps for thermo-mechanical performance simulation using ANSYS are shown in Appendix B.



(a)



(b)

Figure 6-3. Meshing in the solder layers of the power module: (a) cross-section view of the mesh in solder layer; (b) top view of the mesh in solder layer.

6.2. Thermo-Mechanical Stress/Strain Distribution of Plate-Bonded Module

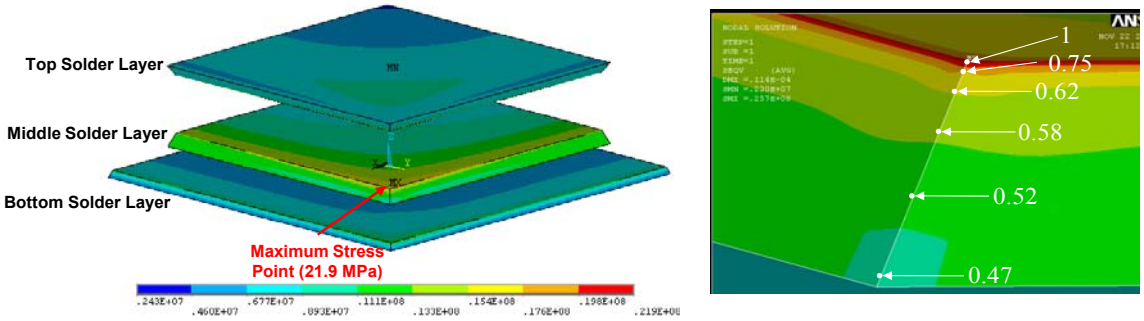
Since the solder layers in the plate-bonded structure are weak points according to the reliability test, the stress distribution in the solder layers is analyzed. For ductile materials

such as solder, a ductile rupture can occur when plastic deformation in the material results in a progressive local reduction in cross-sectional area. Von Mises' theory states that a given material fails by yielding at a critical level of distortional energy [108]. Thus, the distribution of von Mises stress can be used to predict a ductile rupture in the power module. Another critical parameter that has significant impact on the reliability of the power module is plastic strain. According to the widely used Coffin-Manson law, the number cycles to failure (N_f) or fatigue life can be predicted using the following equation [109]-[110]:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon'_f (2N_f)^c \tag{6-6}$$

where $\Delta\varepsilon_p$ is the plastic strain amplitude; ε_f' is the fatigue ductility coefficient; and c is the fatigue ductility exponent that varies between -0.5 and -0.7 [111]. As a result, the distribution of plastic strain in the power module also needs to be simulated.

Figure 6-4(a) shows the von Mises stress distribution in the solder layers. Since the CTE mismatch between the copper plate and the silicon device is larger than both the mismatch between the device and the DBC and the mismatch between the copper plate and the DBC, the maximum stress (21.9 MPa) occurs at the corner of the middle solder layer, which is the solder layer between the copper plate and the silicon device. This result agrees with the trend shown in Figure 5-9(a). Figure 6-4(b) shows the stress distribution in the corner of the middle layer. The labeled values are the normalized stresses at different locations (the normalization base is the maximum stress of 21.9 MPa). Figure 6-5 shows the plastic strain distribution in the solder layer. It can be seen that the stress and strain distribution patterns are very similar. The maximum strain point also occurs at the middle solder layer.



(a) (b)

Figure 6-4. Simulated Von Mises stress distribution in (a) Solder layers and (b) Middle solder layer (Base for normalization: 21.9 MPa) of the plate-bonded power module.

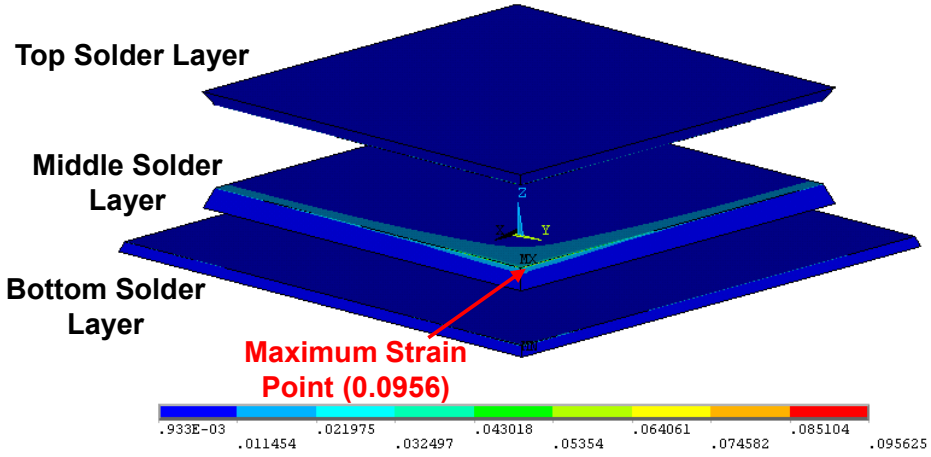
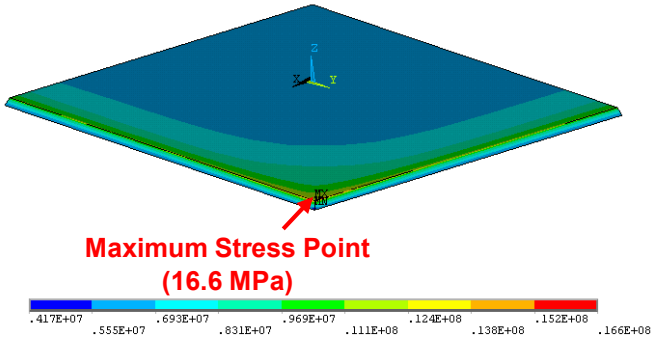
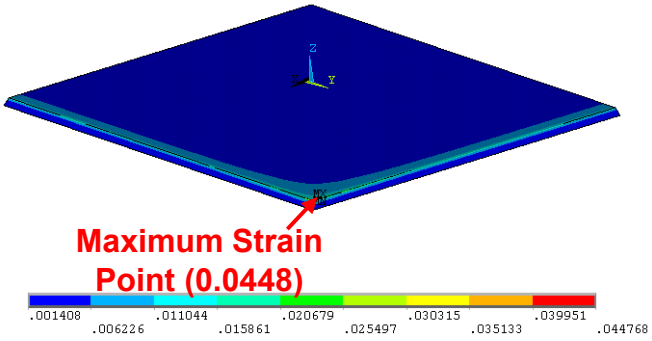


Figure 6-5. Simulated plastic strain distribution in solder layers of the plate-bonded power module.

The stress and strain distributions of a conventional wire-bonded power module are also simulated and results are shown in Figure 6-6. TABLE 6-5 compares the maximum stress and strain in plate-bonded power module and in conventional wire-bonded power module. It clearly shows that due to large CTE mismatch between copper plate and silicon device, the plate-bonded power module suffers 31.9% higher in stress and 113.4% higher in strain, resulting in significant degradation of reliability. Therefore, the structure of plate-bonded power module has to be modified to reduce the thermo-mechanical stress and strain.



(a)



(b)

Figure 6-6. Simulated Von Mises stress distribution (a) and plastic strain distribution (b) of solder layer in a wirebonded power module.

TABLE 6-5. COMPARISON OF MAXIMUM STRESS AND STRAIN IN DIFFERENT POWER MODULES

	Plate-Bonded Power Module	*Wire-bonded Power Module*
Maximum Von Mises Stress (MPa)	21.9	16.6
Maximum Plastic Strain	0.0956	0.0448

6.3. Plate-Array Power Module with Lower Thermo-Mechanical Stress

The Plate-bonded power module can achieve better thermal performance than the conventional wire-bonded power module. As shown in Figure 6-7, the plate-bonded

power module was firstly used by Toyota Lexus hybrid electric vehicle [6]. In the Lexus power module, the copper plates inserted between the top substrate and the semiconductor dice to improve dielectric performance and compensate the height different between the IGBT and the diode [104]. The power module with thick copper plates suffers from high thermo-mechanical stress. The analytical analysis in Section 5.3 shows that larger bonding area results in higher stress. Therefore, to reduce the thermo-mechanical stress, the large copper plate on top of the device can be divided into several smaller pieces as shown in Figure 6-8. A similar method called metal-post-interconnect-parallel-plate structure was used by researchers from CPES [32] and Alstom [28] as shown in Figure 6-9.

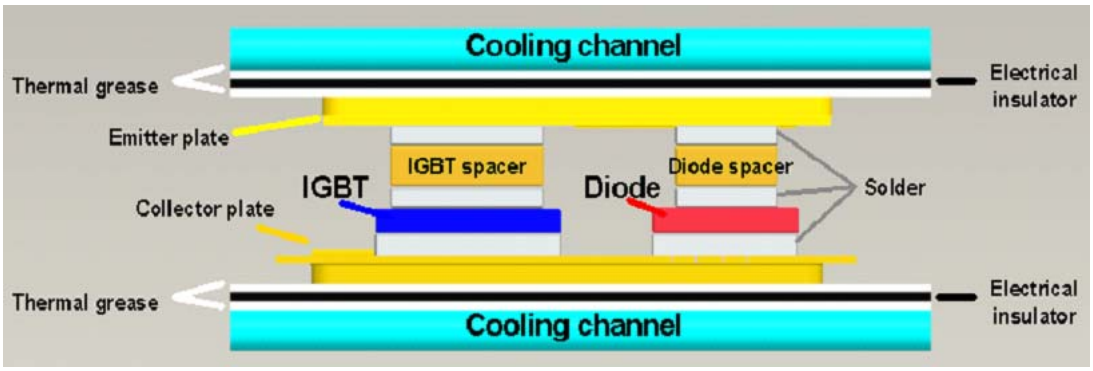


Figure 6-7. Plate-bonded power module from Toyota [6] (Used under fair use guidelines, 2011).

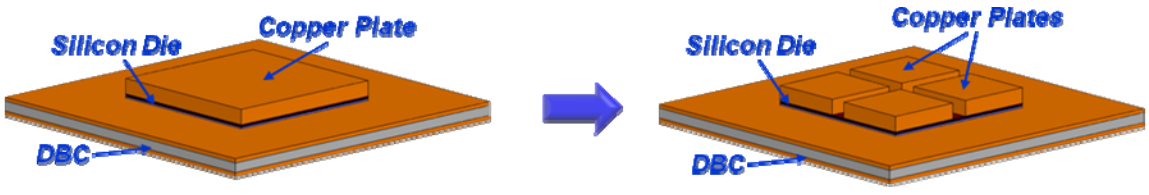


Figure 6-8. Reduce thermo-mechanical stress by partitioning the copper plate to smaller pieces.

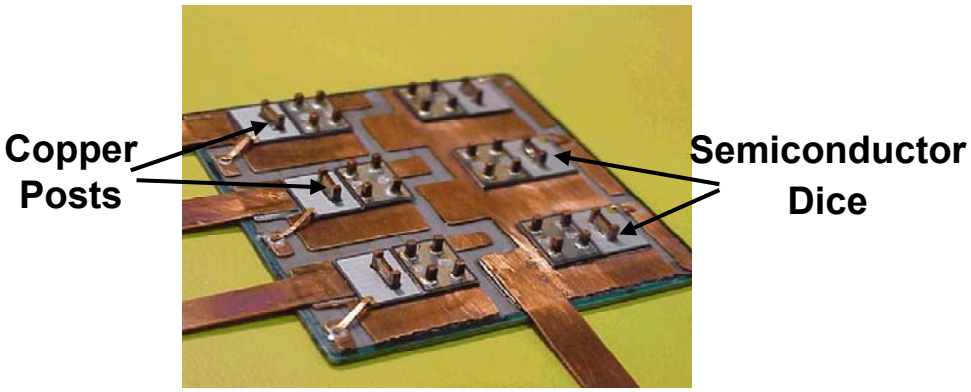


Figure 6-9. Metal-Post-Interconnect-Parallel-Plate Structure (MPIPPS) proposed by CPES [32] (Used under fair use guidelines, 2011).

The width of the spacing among neighboring copper plates affects the thermal performance, thermo-mechanical performance and processability of the power module. Smaller spacing results in better thermal performance. Figure 6-10 shows the thermal performance of the power module vs the spacing between plates. The spacing does not have significant impact on the thermal resistance of the power module. However, the thermal impedance is affected by the thermal mass near the heat source. From Figure 6-10, it can be seen that the thermal impedance of the power module is increased by 13.4% when the spacing increases from 0.4 mm to 1 mm. Smaller spacing also results in more difficulties in process and higher stress/strain in the solder layer. Figure 6-11 shows the change of the maximum stress/strain in the solder layers with the spacing. It clearly indicates that higher stress and strain in the solder layer with smaller spacing. However, with increasing of the spacing, the reductions of stress and strain decrease. In this study, the spacing is set to be 0.8 mm which is mainly limited by the process. The trenched copper plate was fabricated using wet etching. Due to isotropic etching, the spacing among copper plates has to be equal or larger than 0.8 mm to etch away 0.4 mm thick copper.

Due to the limited surface area on the semiconductor device, too many partitions lead to significant loss of thermal mass and increasing of process complexity. As a result, in this study, the number of copper plates varies among one (1 × 1 matrix), four (2 × 2 matrix), and nine (3 × 3 matrix).

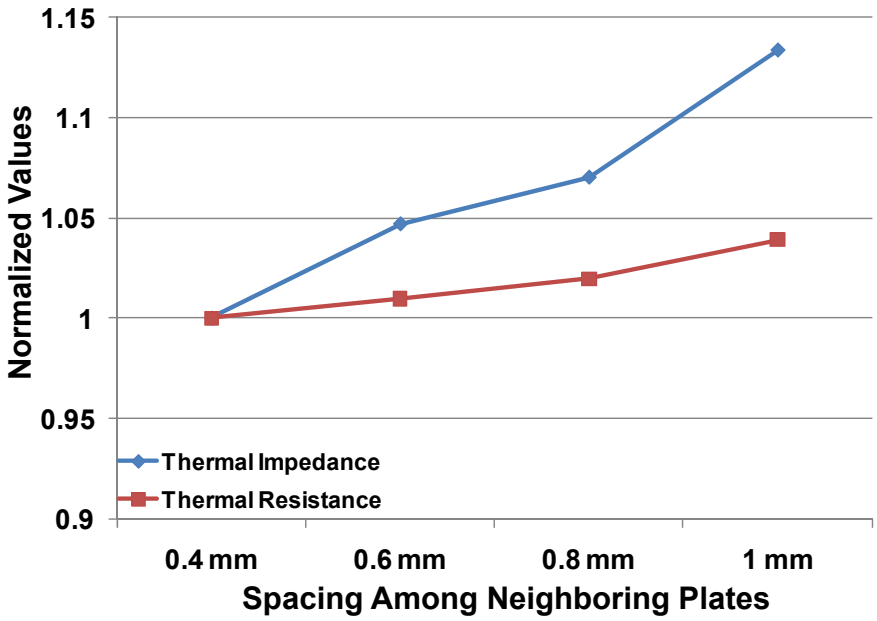


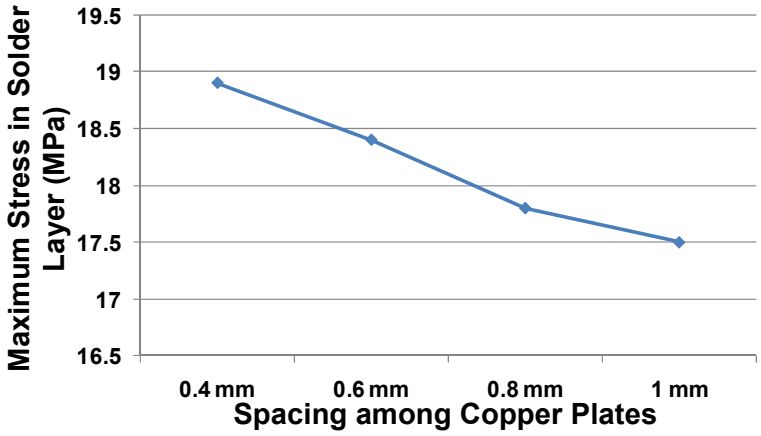
Figure 6-10. Spacing between neighboring plates vs thermal performance based on finite element simulation (thermal resistance and thermal impedance normalized based on the values of 0.4 mm spacing).

6.4. Thermo-Mechanical Stress Distribution of Plate-Array Power Module

The thermo-mechanical stress distribution of plate-array power module were simulated and compared with single-plate power module. The structures used in the simulation are shown in Figure 6-13. Thanks to symmetric structure, only one quarter of the structure is simulated. The simulation set-up described in Section 6.1 is used in this study.

The simulation results for plate-array power module are shown in Figure 6-12. It can be seen that with increasing of number of copper plates, the maximum stress and strain in

the middle and top solder layers decreases significantly. However, the stress and strain in the bottom solder layer increases slightly. As a result, compared to single-post structure, the maximum stress and strain in the structure with 3 × 3 plate-array can be reduced by 18.7% and 67.8%, respectively.



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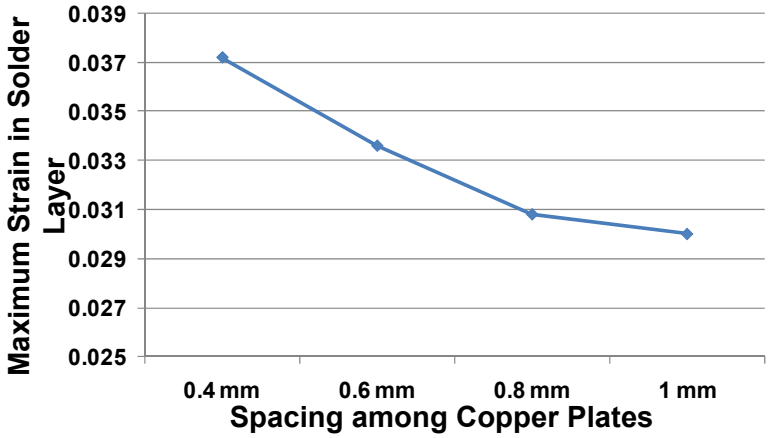
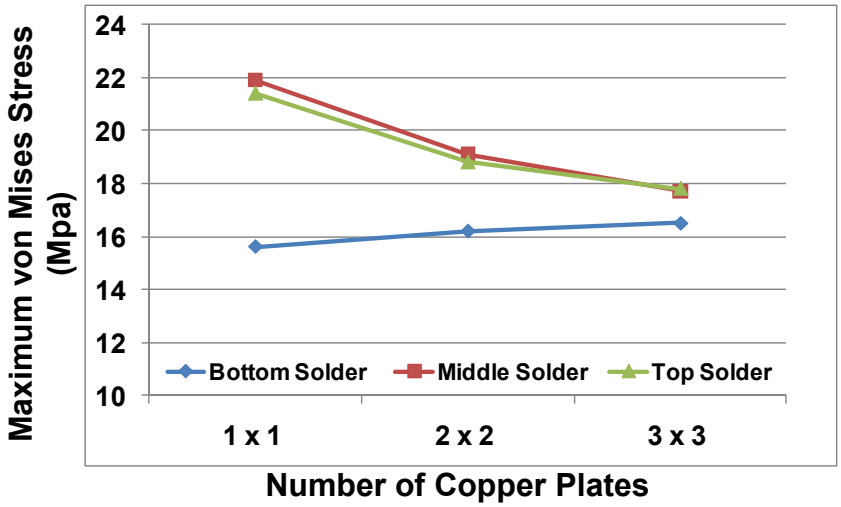
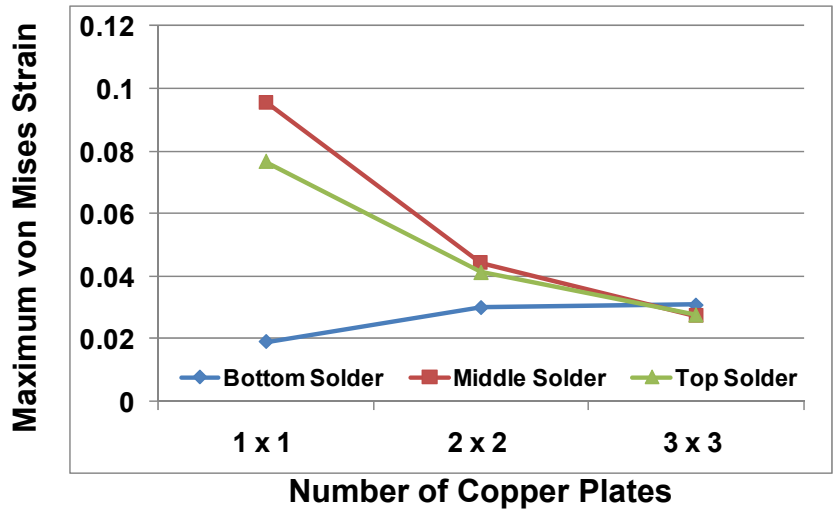


(b)

Figure 6-11. Stress (a) and strain (b) vs the spacing among copper plates for 3 × 3 trenched copper plate.



(a)



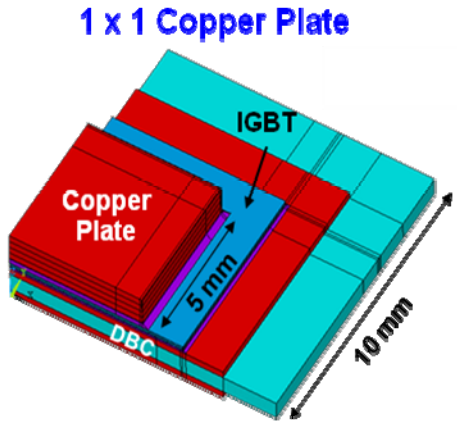
(b)

Figure 6-12. Simulated stress (a) and strain (b) distributions for plate-array power module.

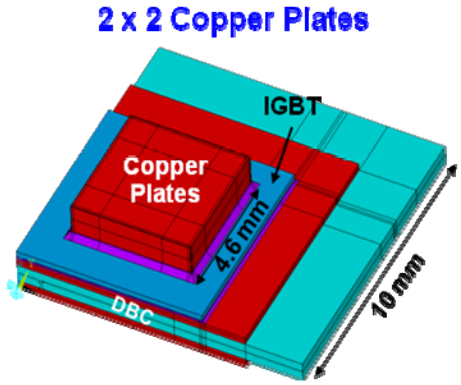
In [32], the thermo-mechanical stresses in wirebonded power module and the planar power module are compared. It concludes that the stress in the bond wire is much smaller than that in the solder layers of the planar power module. As a result, the wirebonded power module has better reliability. This statement is correct if the weak point of thermo-mechanical performance of the wirebonded power module is the interface between bond wire and silicon device. However, with increasing of die-size of power semiconductor device (> 1 cm^2), the thermo-mechanical stress in the die-attach layer

keeps increasing. As a result, die-attach layer becomes more vulnerable to temperature cycling than bond wire [105]-[106]. In this study, die-attach layer is considered to be the weak point in the wirebonded power module. Therefore, the maximum stress/strain in the die-attach layer of the wirebonded power module is compared with the maximum stress/strain in the solder layers of the post-array power module. From Figure 6-12, it can be seen that by using 3 × 3 array, the maximum stress and strain in the post array power module can be limited to the similar values as the wirebonded power module has.

From the simulation results, it also can be seen that the plate-array structure can help make the stress more evenly distributed among three solder layers. This can be explained in Figure 6-14. When the temperature of the power module increases, all the layers tend to expand. However, due to larger CTE, the copper plate and the bottom DBC layers tend to expand more than the silicon layer does. The expansion of the copper plate and the DBC will be limited by the middle solder layer and the bottom solder layer. As a result, the silicon is subject to tensile stress which is balanced by the compression stresses from the copper plate and the DBC. For single plate case, the large stress in the middle solder layer indicates that large tensile stress is imposed from the copper plate, which helps reduce the stress in the bottom solder layer. When the stress at the middle solder layer is reduced in the case with copper plate-array, to balance the tensile stress in the silicon layer, higher compression stress from the bottom DBC is required, leading to increasing stress in the bottom solder layer.



(a)



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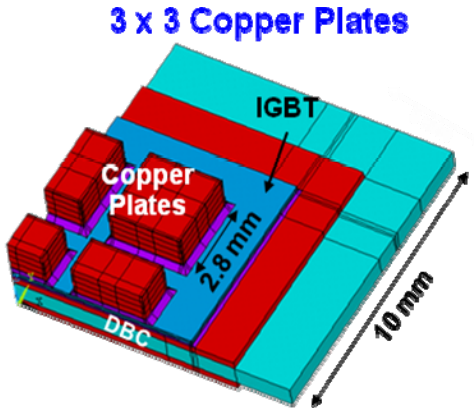


(c)

Figure 6-13. Structures used in ANSYS simulation: plate-bonded power module with single-copper plate (a), 2 × 2 copper plates (b), and 3 × 3 copper plates (c) (top DBC is not shown in the pictures).

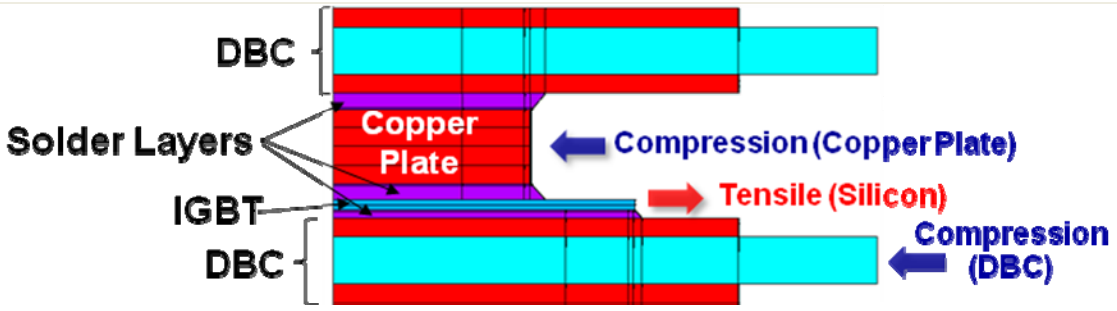
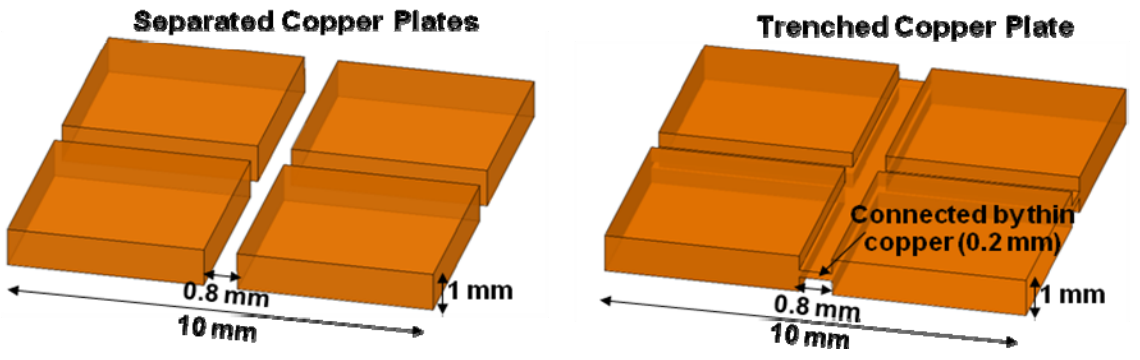


Figure 6-14. Stress distribution in the power module when the temperature increases.

6.5. Trenched Copper Plate Power Module

Simulation results suggest that with nine pieces small copper plates instead of one large piece copper plate, the maximum stress and strain can be significantly reduced. However, the large number of copper plates increases the process complexity such as alignment and handling of copper plates during sample preparation. Therefore, a trenched copper plate can be used to replace several separated small copper plates as shown in Figure 6-15. In Figure 6-15(b), four smaller pieces of copper plates are joined together using a thin layer of copper (0.2 mm thick). The thin joint layer can help keep copper plate in position without inducing large stress in the bonding layers. Since the expansion or contraction of the small copper plates could be constrained by the connection, with increasing of the thickness for the connection, the stress and the strain at the solder layers increase. As shown in Figure 6-16, using the connection with 0.2 mm only increases the stress and strain in the solder layer by 1.4% and 3.4%, respectively. Therefore, the thickness of the connection can be set to be 0.2 mm to minimize its impact on the stress and strain in solder layers. The trenched copper plate structure has slightly more thermal mass inserted in the power module compared to the separated copper plates which has potential to achieve better transient thermal performance. However, with 0.2 mm connection, the improvement of the thermal performance is negligible (shown in TABLE 6-6).



(a) (b)

Figure 6-15. Separated copper plates (a) and trenched copper plate (b).

TABLE 6-6. NORMALIZED THERMAL PERFORMANCES OF THE TRENCHED COPPER PLATE STRUCTURES (BASE: PLATE-ARRAY STRUCTURE).

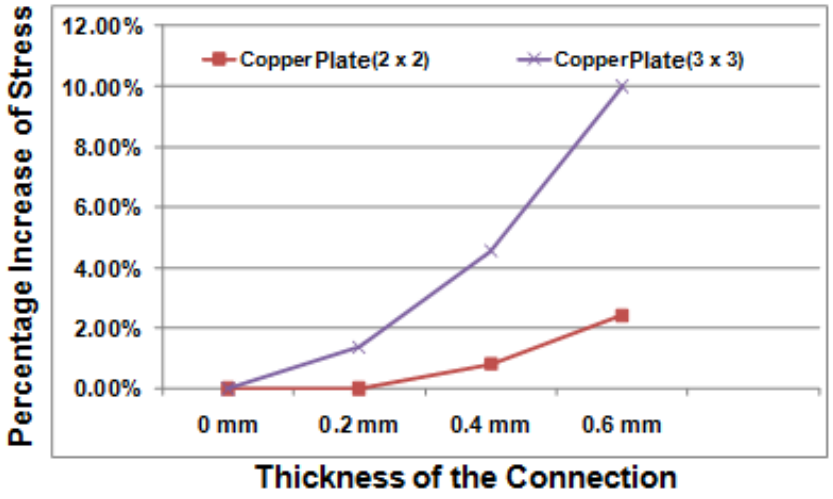
	Thermal Impedance for 0.34 s transient (°C/W)
Trenched Copper Plate (2 × 2)	0.983
Trenched Copper Plate (3 × 3)	0.992

6.6. Trade-off between Thermal Performance and Thermo-Mechanical Stress

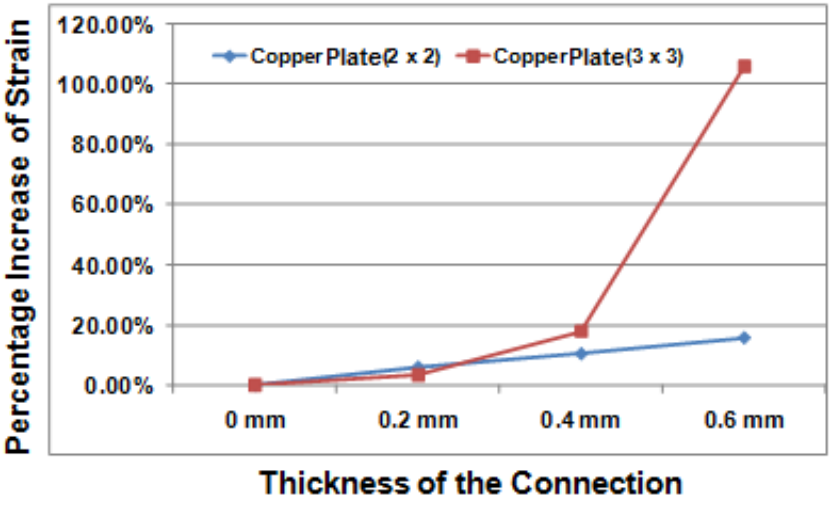
To reduce the thermo-mechanical stress in the power module, some clearances have to be left to divide the large piece of copper plate into several small ones. The clearance reduces the thermal mass and contact area for thermal path. With 1 mm thick copper plate, the spacing between two neighboring copper plates is set to be 0.8 mm.

Figure 6-17 presents the thermal performance and the maximum stress/strain in the power module when different copper plate structures are used. The trade-off between thermal performance and reduction of thermo-mechanical stress/strain is clearly shown in Figure 6-17. With increasing of number of plates, the maximum stress and strain in the power module are reduced significantly. However, when the number of copper plates increases from 3 × 3 to 4 × 4, the stress and strain in the power module only decreases by less than 5%, which shows that the benefit of using 4 × 4 trenched copper plate is not noticeable. Therefore, in this study, the maximum number of plates is limited to be 3 × 3.

Different with the stress and strain, the thermal impedance of the power module at 0.34 s increases by 9.04% when 3 × 3 trenched copper plate is employed due to less thermal mass. Since the heat dissipates from the bottom side via heat-exchanger, partitioning the copper plate on the top of the device would not impact the thermal resistance. The variation of the thermal resistance is less than 3% when the copper plate structure changes. From the above discussion, it can be seen that the section of the copper plate structure should focus on the trade-off between the transient thermal performance and the thermo-mechanical stress/strain.

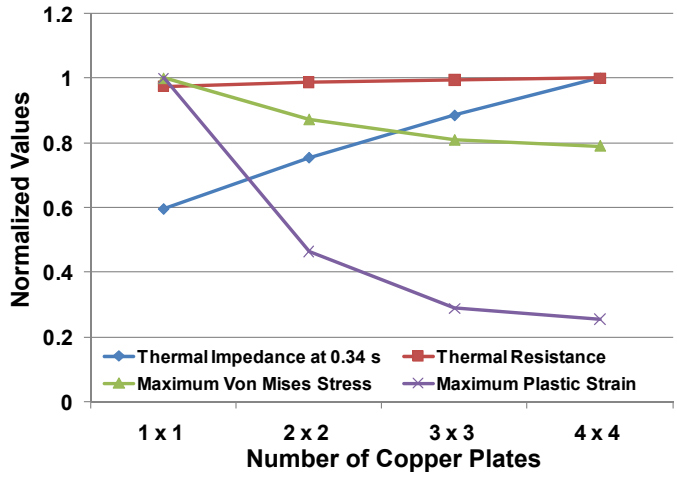


(a)

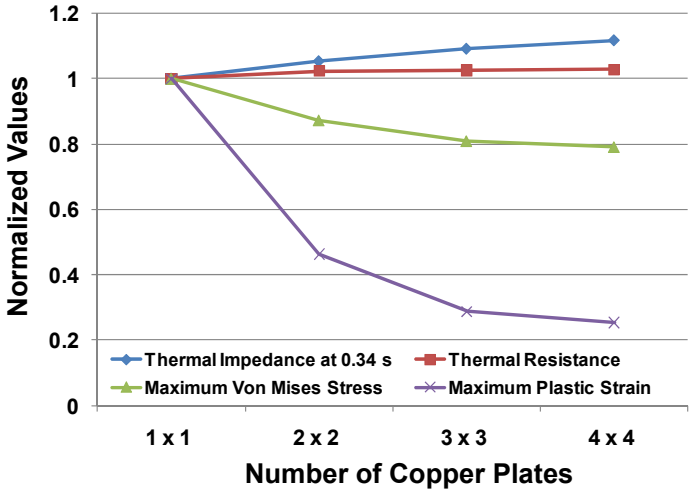


(b)

Figure 6-16. Stress (a) and strain (b) vs the thickness of the connection among copper plate array.



(a)



(b)

Figure 6-17. Trade-off between thermal performance and thermo-mechanical performance for power module with heat transfer coefficient of 50000 W/(m^2·˚C): (a) normalized based on the maximum value; (normalized base: 0.168 ˚C/W for thermal impedance; 0.2523 ˚C/W for thermal resistance; 21.9 MPa for von Mises stress; 0.0956 for plastic strain); (b) normalized based on the case with single copper plate (normalized base: 0.151 ˚C/W for thermal impedance; 0.246 ˚C/W for thermal resistance; 21.9 MPa for von Mises stress; 0.0956 for plastic strain);

6.7. Conclusions

In the last chapter, a power module with both good transient and steady-state thermal performance was proposed. However, due to thick copper plate required on the top of

silicon device, large thermal stress could be induced during thermal cycling, leading to poor reliability.

In this chapter, a trenched copper plate structure was used to replace the single copper plate in the power module to reduce the thermo-mechanical stress. To verify the reduction brought by the structure change, finite element simulation was used to find the maximum stress and strain in the power module with different structures. To obtain accurate simulation results, material properties, meshing rules, and boundary conditions were discussed. Due to high yield stress and young's modulus, only elastic properties were considered for brittle materials such as ceramic and silicon. For copper and solder which could yield during thermal cycling, plastic constitutive laws should be applied. In this study, Anand model was used for SAC305 lead-free solder and an empirical model in [107] was employed for copper. Meshing density is another critical parameter for FEM simulation. The fine mesh was used at stress/strain concentration region to get accurate results. For those regions that have lower stress/strain, the coarse mesh was applied to save computing time. The boundary conditions of thermo-mechanical stress simulation were set to simulate the case that the sample is thermally cycled.

The FEM simulation results clearly show the advantages of using trenched copper plate to replace the single copper plate in terms of thermo-mechanical stress. There were three structures that were simulated using ANSYS. Compared to the single copper plate structure, dividing the copper plate into four smaller pieces (2 × 2 array) can reduce the maximum von mises stress by 13.6% and the maximum plastic strain by 53.7%. If a 3 × 3 trenched copper plate is used, the maximum von mises stress and the maximum plastic strain can be further reduced to 81.3% and 32.2% of the original values.

The thermal performance of the trenched copper plate module was also investigated. With increasing of number of copper plates, the transient thermal performance would degrade by 9.04% while the steady-state thermal performance keeps stable. Therefore,

the design of copper plate structure should depend on the trade-off between transient thermal performance and thermo-mechanical stress.

Chapter 7. RELIABILITY TEST FOR TRENCHED COPPER PLATE POWER MODULE

In previous chapter, a trenched copper plate structure was proposed to reduce the thermo-mechanical stress in the power module at the price of less thermal mass. In this chapter, twenty-four samples with three different structures were fabricated. The numbers of copper plates in the trenched plate are set to be 1 × 1, 2 × 2, and 3 × 3. The detailed process step for sample fabrication is discussed.

These samples were thermally cycled from -40˚C to 105˚C. To detect the failure at the bonding layer, the curvature of these samples were measured using laser scanning before and after cycling. Figure 7-1 shows the curvature caused by the bending of the substrate. The curvature of a point is a measure of how sensitive its tangent line is when the point moves to other nearby points. It is natural to define the curvature of a straight line to be zero. The curvature of an arc of circle with the radius R should be large if R is small and small if R is large. Thus the curvature of a circle is defined to be the reciprocal of the radius [112]:

$$\kappa = \frac{1}{R} \tag{7-1}$$

As shown in Figure 7-1, more bending of the substrate results in smaller radius R and higher curvature. When cracks and delaminations occur at the bonding layer, the residual stress induced during thermal process is released. As a result, the curvature of the samples becomes zero. By monitoring the change of curvature, the degradation of bonding layer can be detected. Experimental results showed that the samples with different copper plate structure had similar curvature before thermal cycle. The curvatures of the samples with single copper plate decreased more than 80% after only 100 cycles. For the samples with 2 × 2 trenched copper plates and the samples with 3 × 3

trenched copper plates, the curvatures were only reduced by 24.2% and 22.5% after 100 cycles, respectively, indicating better reliability than the samples with single copper plate. The x-ray pictures of cross-sectioned samples confirmed that after 300 cycles, the bonding layer for the sample with single copper plate has many cracks and delaminations starting from the edge. However, no noticeable cracks were observed in the bonding layer of the sample with 3 × 3 trenched copper plate.

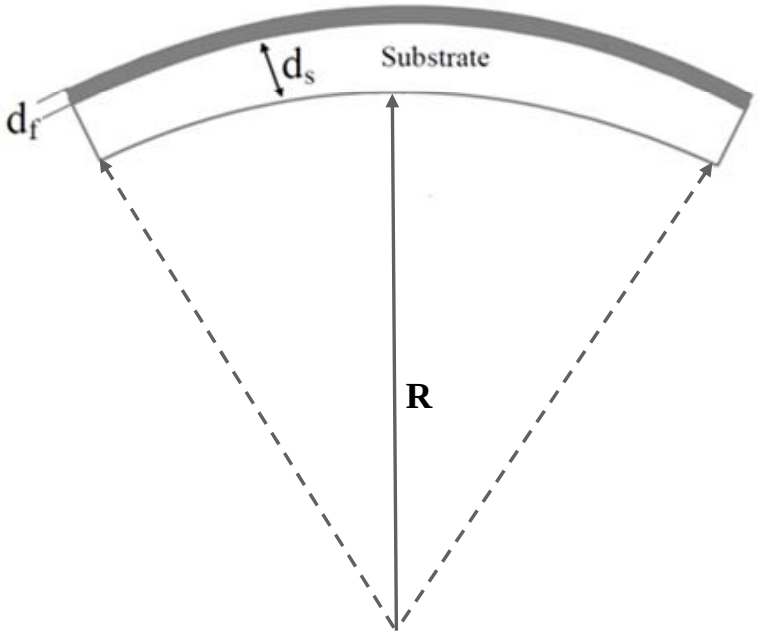


Figure 7-1. Curvature caused by the bending of substrate.

7.1. Design of Experiment

In order to confirm the benefit brought by the trenched copper plate power module, three types of power modules that have different number of copper plates will be thermally cycled. However, the completed power modules shown in Figure 6-13 have complicated structure and multiple solder layers. This imposes difficulties in sample fabrication and failure detection. Since the maximum stress and strain occurs at the middle solder layer that joins the silicon device and the copper plate, a simplified

structure as shown in Figure 7-2 is employed for reliability test. In the simplified structure, the silicon device is bonded to 1 mm thickness copper plate via solder layer. The comparisons of the maximum stress and strain in the completed power module and simplified power module are shown in Figure 7-3. Due to more symmetric structure, the maximum stress and strain in the completed power module is much lower than that in the simplified module. However, for both cases, with increasing of number of copper plates, the maximum stress and strain decrease. Therefore, to verify the benefit brought by multiple copper plates, the simplified structure as shown in Figure 7-2(b) can be used.

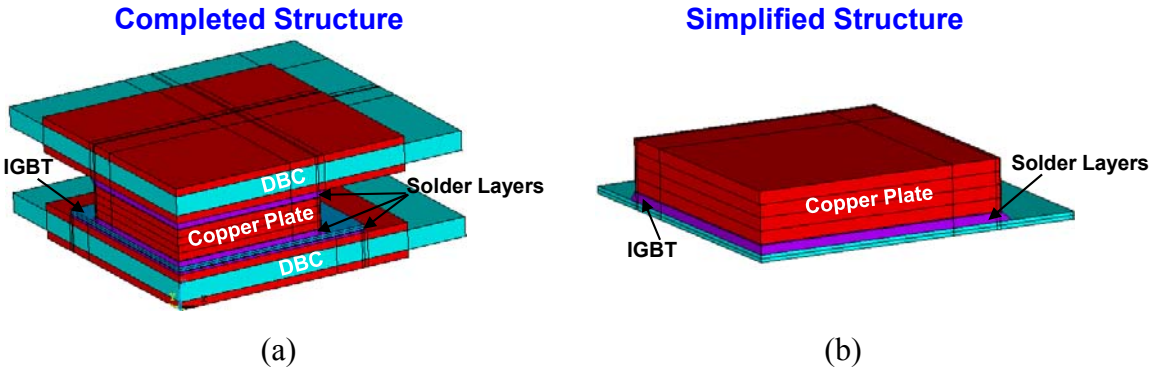
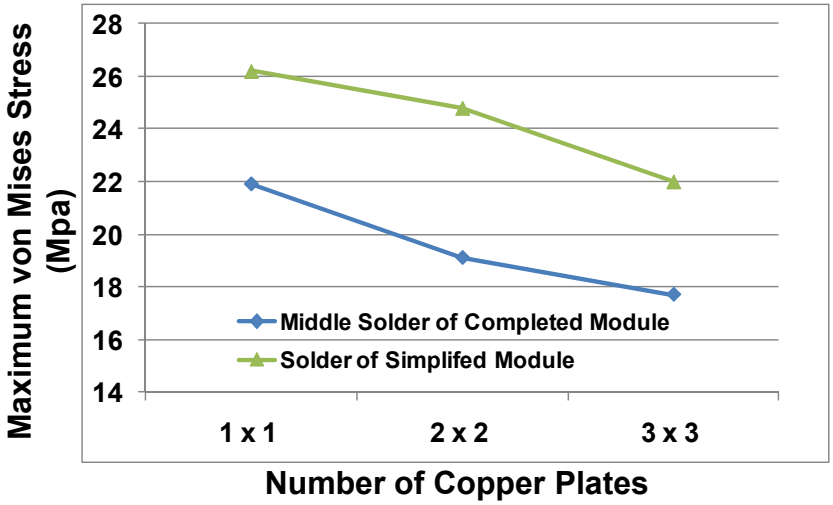


Figure 7-2. Comparison of completed structure for power module (a) and simplified structure for reliability test (b).

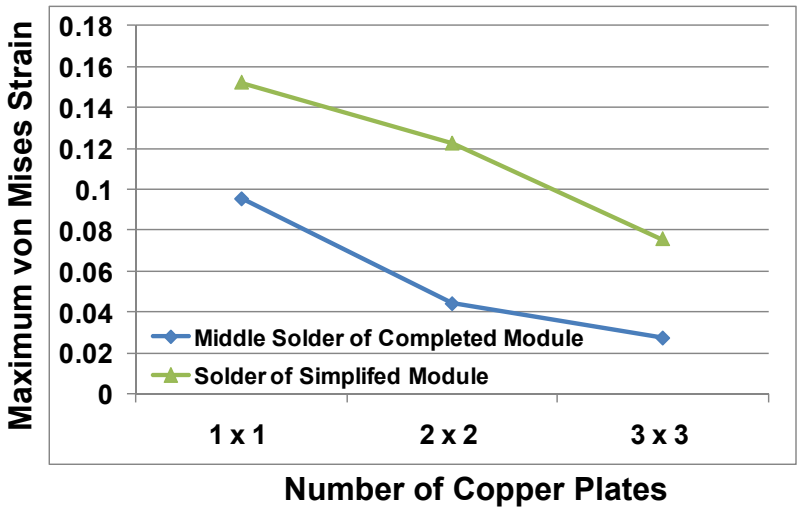
7.2. Preparation of Samples

To experimentally verify the better reliability brought by trenched copper plate structure, totally twenty-four samples with three different structures (eight samples for each structure) were fabricated. The cross-section view of reflow is shown in Figure 7-4. A Cirlex fixture is used to align copper plate, solder preform, and silicon die. The thickness of the fixture is designed to be 1.55 mm. A weight of seven grams is placed on the top of the silicon die to improve the wettability. Since the thick solder layer (0.2 mm) is employed in this application to reduce the maximum stress, the die could be tilted

during the reflow process. Therefore, four Circlex spacers were embedded in the solder layer to control the uniformity of solder thickness.



(a)



(b)

Figure 7-3. Comparison of the maximum stress (a) and the maximum strain (b) in the completed structure and the simplified structure （based on finite element simulation）.

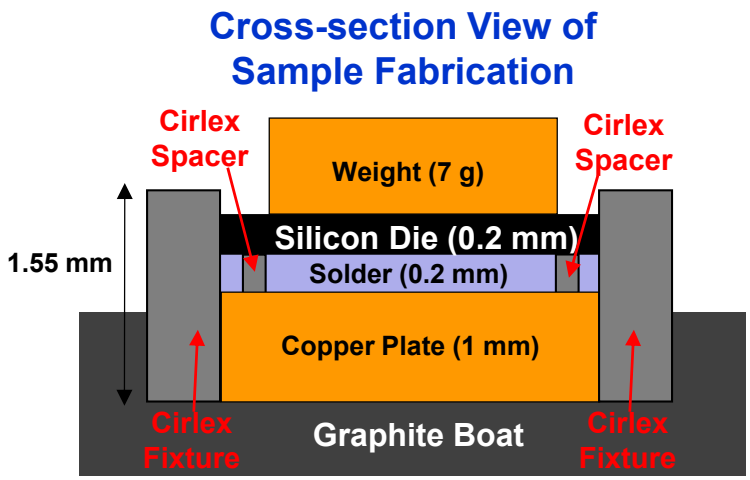


Figure 7-4. Cross-section view of reflow assembling for sample.

Figure 7-5. The 2112-1 hydraulic press from Carver to flatten the copper plate.

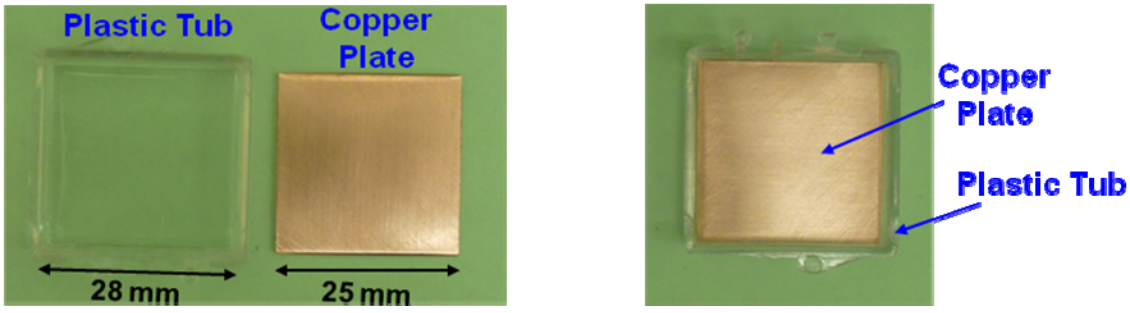
The trenched copper plate shown in Figure 6-15(b) can be fabricated using wet etching process. A copper plate with 1 mm thickness is firstly flattened by hydraulic press (Carver, Model 2112-1) under 1.4 MPa for 1 hour at room temperature as shown in Figure 7-5. The flat copper plate is then masked by Kapton tape. The laser cutting on Kapton tape forms the desired patterns.

After patterning, the copper plate can be etched using ferric chloride ($FeCl_3$) solution in a spray etching machine as shown in Figure 7-6. The etching rate of the process is highly dependent on the flow rate [113]. The flow rate at the edge of the copper plate is much higher than that at the center because of more opening space at the edge. Therefore, the etching rate at the edge of the copper plate is higher than that at the center. To achieve uniform etching rate across the copper plate, the copper plate is placed in a plastic tub as shown in Figure 7-7. During the etching process, the tub is filled with etching solution. The etching solution sprayed in the tub causes the moving of all the liquid in it. Therefore, the flow rate of etching solution in the tub is uniform, leading to uniform etching rate across the copper plate. Since the wet etching is an isotropic process, to achieve symmetric cross-section view, both sides of the copper plate have to be patterned and etched. During the etching process, the copper plate is rotated and flipped periodically to ensure the etching uniformity.

Figure 7-6. Spray etching machine.

After etching and proper cleaning processes, the copper plate is coated with silver to improve wettability and prevent surface oxidization. The detailed process flow and the critical process parameters for copper plate fabrication are shown in Figure 7-8(a). From Figure 7-8(b), it can be seen that to simplify the process, four samples with different numbers of copper plates are made in one large piece of copper plate. This arrangement also can make sure that the process conditions such as reflow temperature and plating

quality of silver are exactly same for different types of samples that are integrated in the same copper plate. Therefore, the difference in the reliability test for trenched copper



(a) (b)

Figure 7-7. The plastic tub and copper plate used in the etching process (a) and the copper plate placed in the plastic tub (b).

plate samples and single-plate samples are brought by structure instead of other process conditions.

After the fabrication of the copper plates, the copper plates are soldered to the silicon dummy chip using SAC305 lead-free solder in the vacuum reflow chamber (MV2200 from SST technology as shown in Figure 7-9). In the reflow chamber, the sample is placed in a graphite boat that works as heat source when current flows through it (shown in Figure 7-9). A thermocouple is inserted into the graphite boat to monitor the temperature of the reflow process. Compared to soldering in the air, the advantages of this solder vacuum reflow is able to achieve lower void percentage in solder layer and is cleaner process since no flux is required in vacuum reflow. The voids in the solder layer could degrade the electrical, thermal, and mechanical performance of the electronics system. More importantly, high void percentage could impair the reliability of the solder joint, leading to early failure of electronic system. One main reason of voids formed in the solder layer is that the outgas of flux is entrapped during reflow process as shown in the x-ray picture in Figure 7-10(a). In the x-ray image, the darker region represents the

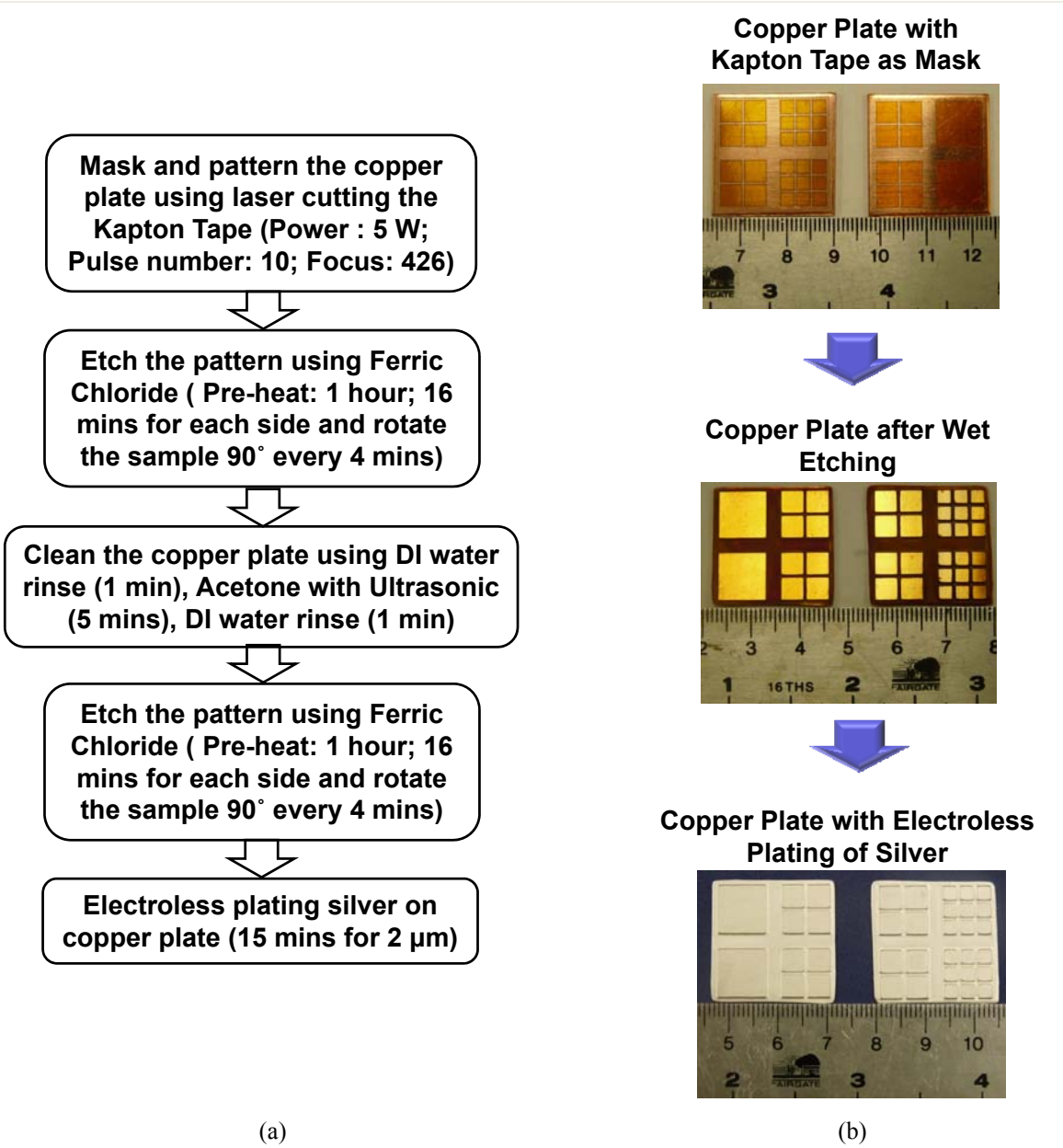
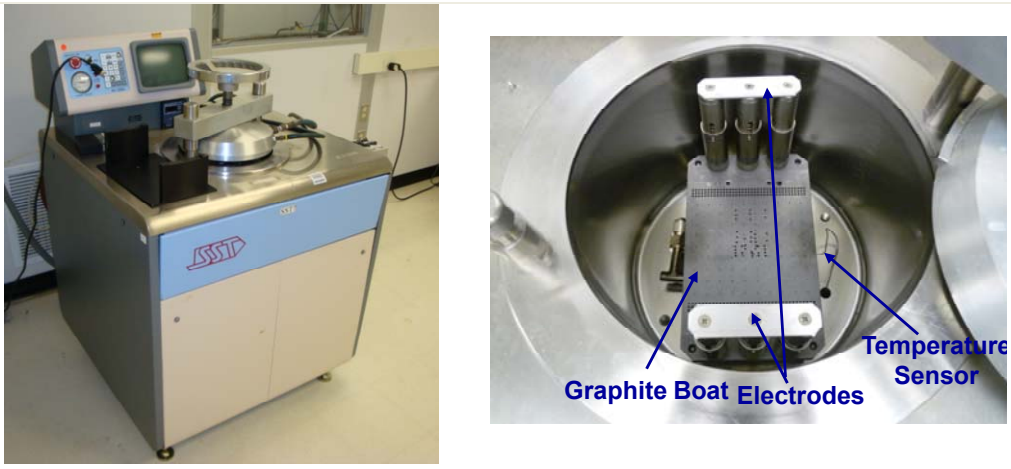


Figure 7-8. Process flow and key process parameters (a) and hardware (b) for fabrication of copper plate.

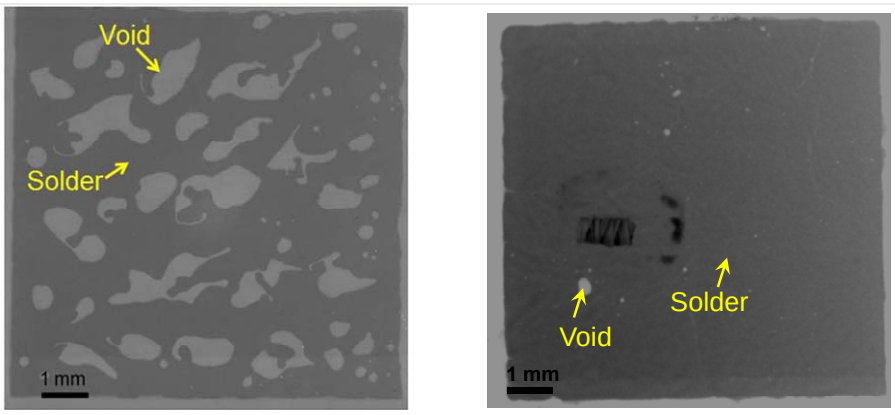
good bonding area without voids, the lighter region represents the voids trapped in the solder layer. Notice that the gas formation during the solder reflow is a random process, the trapped voids are found randomly distributed under the device. For this specific sample, the void area is calculated to be close to 23%. However, flux is widely used in solder reflow process to remove oxidation and improve wettability of the surface. Using

vacuum reflow and protective atmosphere can prevent the bonding surface from oxidization. Therefore, no flux is required in vacuum reflow process, resulting in lower voids percentage [114]. Figure 7-10(b) shows the x-ray image of solder joint formed using vacuum reflow. From the image, it is estimated that the void percentage is less than 1%, which is much lower than that of the solder joint formed using reflow process with flux. The black area in Figure 7-10(b) is caused by the solder area on the top surface of the device.



(a) (b)

Figure 7-9. Vacuum reflow chamber MV2200 from SST (a) and inside view of the chamber (b).



(a) (b)

Figure 7-10. X-ray images of solder layers formed using different processes: (a) reflow in the air (void percentage: 23%); (b) reflow in vacuum chamber (void percentage: <1%).

Figure 7-11 shows the solder reflow profile used for reliability test. The peak temperature used to reflow SAC305 lead-free solder is set to be 270˚C for two minutes. The forming gas during reflow can be used to remove oxidation and the nitrogen gas helps create vacuum environment inside the chamber.

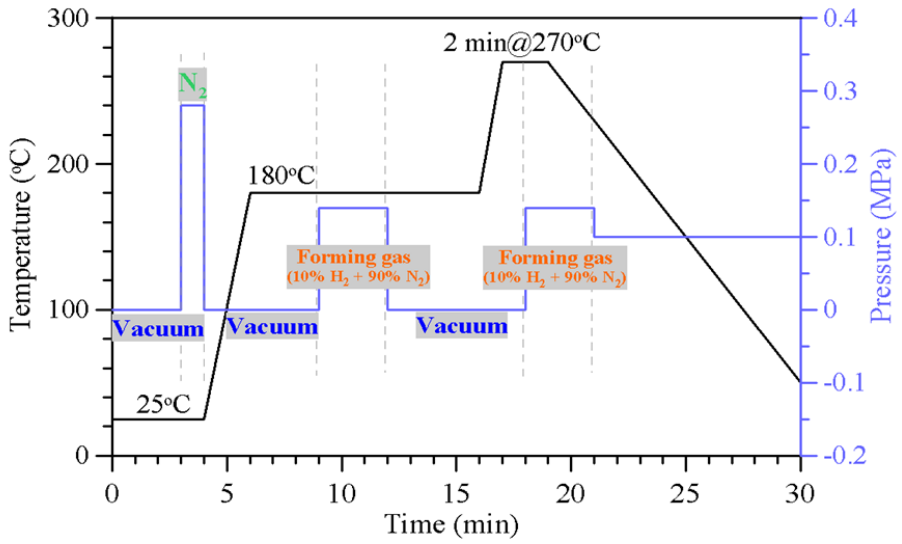


Figure 7-11. Temperature profile for vacuum solder reflow.

The components used in the reflow process are shown in Figure 7-12. Figure 7-13 describes the main steps for assembly of samples. Firstly, the two pieces of copper plates that can be used to make eight samples are placed in the graphite boat (Figure 7-13(a)). A fixture made of Cirlex from Dupont is used for alignment of copper plates, solder preform, and silicon chips. Cirlex is an all-polyimide sheet material that shows good mechanical stability across wide temperature (-269°C to as high as 351°C). It is also readily modified/machined by laser cutting, drilling, machining and chemical etching. With the help of Cirlex fixture, the SAC305 solder preforms are aligned with the copper plates as shown in Figure 7-13(c). After that, four small Cirlex spacers are dropped on each preform to resolve die tilting issue. The silicon devices are then placed on the top. To improve the soldering quality, a weight of seven grams is applied for each sample in the reflow process. The completed samples are shown in Figure 7-13(f).

It should be noted that in the experiment, one large piece of solder preform without partitioning is used for every trenched copper plate sample to simplify the process. Thanks to the surface tension, the melting solder tends to shrink underneath of the trenched copper plate and automatically forms gaps between neighboring copper plates. Figure 7-14 shows the x-ray images of solder joints for different samples. It can be seen that for the samples with 2 × 2 or 3 × 3 trenched copper plates, there is only a small amount of solder in the gaps. In addition, thanks to vacuum reflow, the void percentages in the solder layers are very small (< 5%) for all the samples.

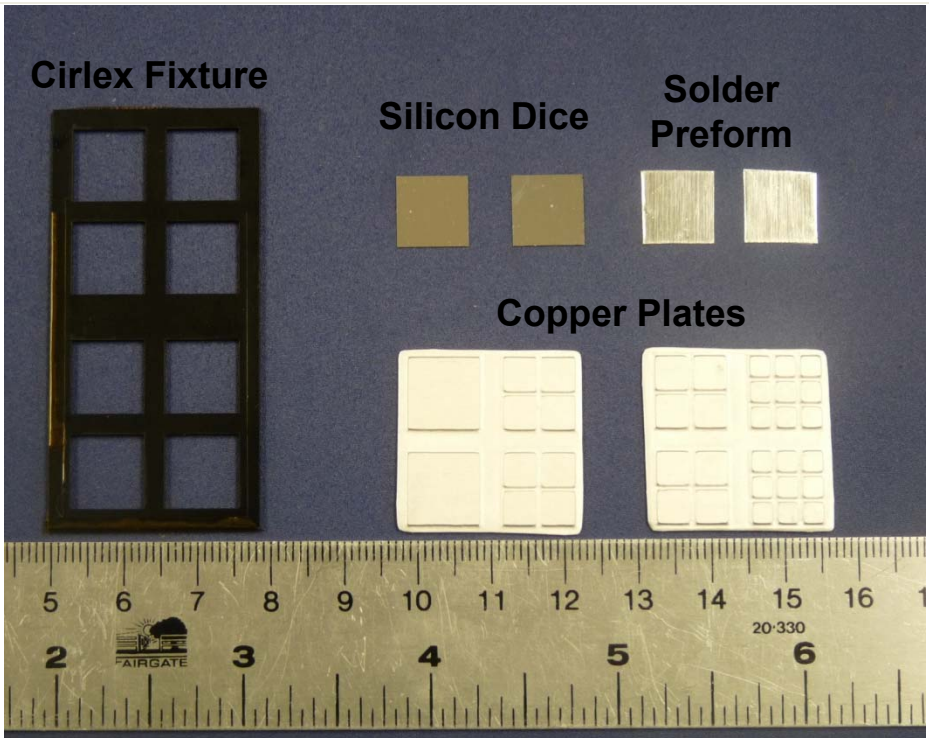


Figure 7-12. Components used for fabrication of samples.

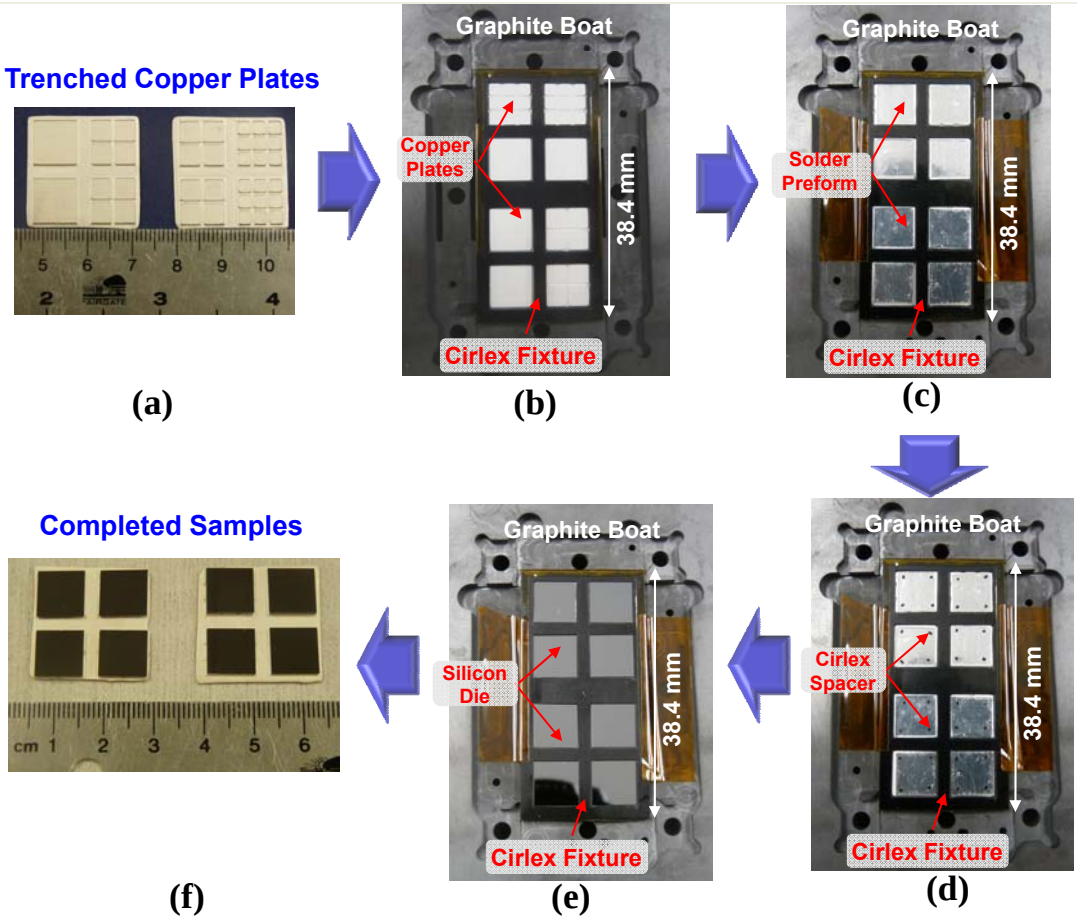


Figure 7-13. Procedure for assembly of samples.

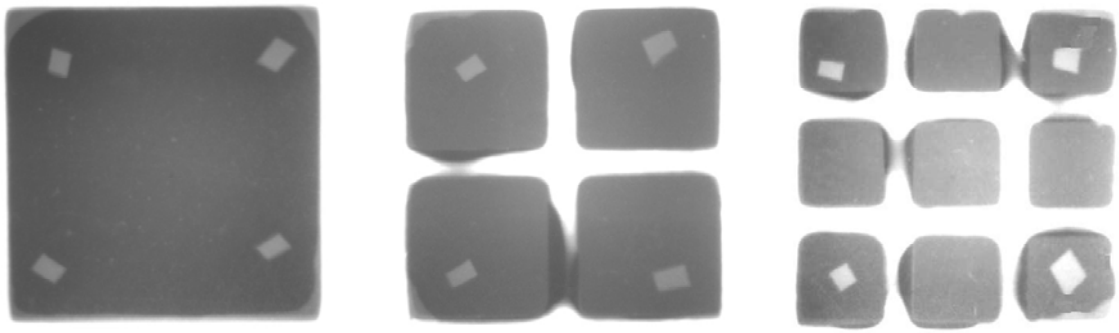


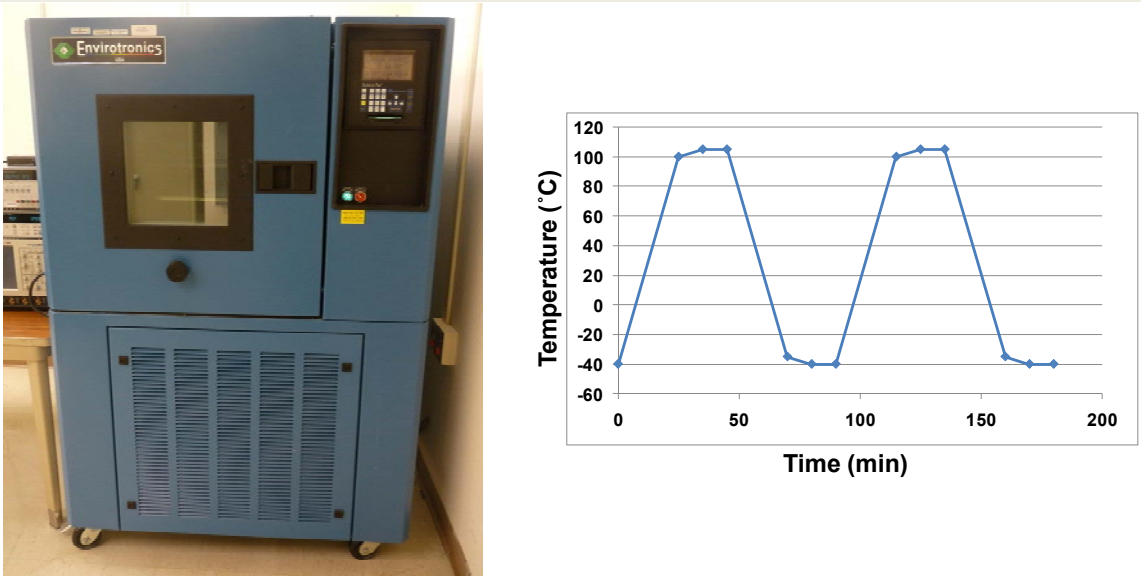
Figure 7-14. X-ray images of solder joints for different types of samples.

7.3. Reliability Test of Trenched Copper Plate Samples

7.3.1. Set-up of Thermal Cycling Test

To test the reliability of different structures, the samples were thermally cycled using thermal cycling chamber from Envirotronics as shown in Figure 7-15(a). Thermal cycling test identifies the ability of assembly to resist extremely low and high temperatures, as well as their ability to withstand cyclical exposures to these temperature extremes. During this testing, the environment temperature of packaging was alternated between hot and cold extremes at a predetermined rate for a specified number of cycles using temperature cycle chamber. Due to CTE mismatch of different materials, the change of temperature will induce thermo-mechanical stress and strain inside the electronic packaging, eventually leading to failure of electronic system. Therefore, thermal cycling is an effective method for stressing wire bonds, solder joints, die bonds, and hermetic seals. Usually, failure mechanisms accelerated by temperature cycling include die cracking and joint failure. The alternating hot and cold temperatures act to flex the junctions, promoting the propagation of micro-cracks or voids which occur as a result of intermetallic compound formation, mismatched CTEs, improper wire-bonding parameters, and similar phenomena. Temperature cycling is becoming more prevalent, particularly in the automotive industry.

There are three factors identify a temperature profile for cycling: the temperature range, the rate of temperature change, and the soaking time at the extreme temperatures. Based on standard from automotive industry, the cycling profile used in this study is shown in Figure 7-15(b). The temperature inside the thermal cycling chamber was controlled to periodically change from -40˚C to 105˚C. The soaking time at extreme temperatures was set to be 10 minutes. The total time for a completed cycle is 90 minutes.



(a) (b)

Figure 7-15. Thermal cycling chamber from Envirotronics (a) and thermal cycling profile (b).

7.3.2. Review on Failure Detection of Thermal Cycling Test

The thermal cycling could cause failure of solder joint in the power module, leading to degradation on mechanical, electrical, and thermal performance. By monitoring the change of the performance, the developing of the cracks and voids can be estimated. There are many methods proposed in previous literatures to detect the failure in solder joints after thermal cycling. These methods generally can be categorized into two types: destructive methods and non-destructive methods.

1. Destructive Methods for Failure Detection

For the methods fell into this category, a series of destructive experiments will be conducted on the thermally cycled samples to identify the impact from reliability test. After the destructive test, the samples cannot be re-used for thermal cycling, which implies a large amount of samples required. One widely used destructive method for failure detection is to observe the cross-section of the joint layer using optical microscope or scanning electron microscopy technique. However, only very small portion of the sample can be examined using this method. Other destructive methods usually involve

monitoring of the mechanical performance change of samples along the thermal cycling. In [115][116], the die-shear strength test were used to qualify the bonding quality before and after thermal cycling. The temperature cycling could cause growth of the void, crack, and delamination in the solder layer. As a result, the die-shear strength of the samples could become weak with increasing of number of thermal cycling. By testing the change of the die-shear strength for cycled samples, the failure can be detected.

2. Non-Destructive Methods for Failure Detection

Visual inspection is the common used non-destructive failure detection method. The bonding layer can be examined using x-ray and scanning acoustic microscopy. The impact of finely focused electrons onto an appropriate target generates a high flux x-ray beam. The x-ray is then allowed to impinge on the sample to be analyzed. The transmitted x-rays strike a fluorescent screen, producing an image. The percentage of transmission of x-rays through the sample of interest is a function of the material content and density [117]. Porous regions allow greater penetration of x-rays. Therefore, the x-ray is a powerful tool to detect the void in bonding layer. However, it is inadequate to find the early stage cracks and delaminations since only small gaps are formed in the bonding layer in these cases. Another powerful tool used in packaging industry to detect cracks, dealaminations, etc is scanning acoustic microscopy. Two modes of acoustic imaging are used. One is called scanning laser acoustic microscopy (SLAM) and the other is called C-SAM or pulse mode acoustic imaging. In these methods, acoustic waves travel through (for SLAM) or reflect from (C-SAM) the sample. The acoustic wave undergoes changes, depending on the internal features of the sample. Based on the changes of the waves, the images of the scanned areas can be generated. The detailed description of these techniques can be found in [121]-[123].

Visual inspection usually requires delicate and expensive equipments. In addition, the explanation of the images is also highly dependent on the experience of the operator and it is subjective. Therefore, some other non-destructive methods that can provide

quantitive results are desired. As mentioned before, the failure in the solder layer also impairs electrical and thermal performance of the sample. Therefore, some electrical or thermal parameters of the sample can be used to detect the failure in the solder layer. In [118][120], electrical resistances of solder joints were measured and set as reference. After thermal cycling, the electrical resistances of samples were measured again and compared to the reference values. Once the resistance increased more than 20%, the sample was considered to fail. This method has advantages such as easy to implement and less samples required compared to destructive methods. However, the electrical resistance of the joint layer could be very small, especially for large bonding area. This imposes critical requirements on the measurement accuracy. The change of the electrical resistance can be overwhelmed by the measurement error. In [119], another accurate way to detect the degradation of solder layer was proposed. In that method, the thermal impedance of the power module was measured as criterion to detect the failure of the die-attach layer. However, to use thermal impedance for failure detection, an active device is required, which increases the cost for sample fabrication.

7.3.3. Using Curvature for Failure Detection

Residual stress during the solder process could cause the curvature on the samples. Residual stress is a tension or compression stress that exists in a material without application of an external load. There are essentially two types of residual stresses. One type of stress is intrinsic. It is related to film growth, and will generally be temperature independent [124]. Factors that impact this type of stress include deposition conditions, the growth morphology, and the possible lattice mismatch between layers. These additional stresses called “intrinsic stresses” being produced by non-equilibrium growth processes. These non-equilibrium microstructures lead to additional stresses caused by the tendency of the film to shrink or expand once it has been deposited onto its substrate. When the film initially shrinks relative to the substrate, the film is under residual tensile stress. When the film expands relative to the substrate, there is compressive stress on the

film. These results are regardless of the specific mechanisms that cause films to stretch or shrink relative to substrates. Sometimes the tensile stresses are sufficiently large to cause a film fracture. Similarly, excessively high compressive stresses can cause film wrinkling and local loss of adhesion to the substrate [125].

Another type of residual stresses is related to the temperature processes such as solder reflow, sintering, and welding. For instance, in solder reflow process, when the solder melts, all the layers can expand without constrains. However, once the process temperature decreases to the solidus temperature of the solder, contraction of different layers is limited by the solder layer. Due to different thermal expansion coefficients (CTE) among layers, the layer that has higher CTE tends to contract more than that having lower CTE. As a result, the layer with higher CTE will be under tension stress and the layer with lower CTE will be under compression stress as shown in Figure 7-16 [126]. In Figure 7-16, the CTE of silicon chip is only around 2.6 - 3 ppm/^{o}C at room temperature, which is much lower than that of DBC (7.4 ppm/^{o}C). The curvature is formed in the layered structure because of the residual stress brought by the process.

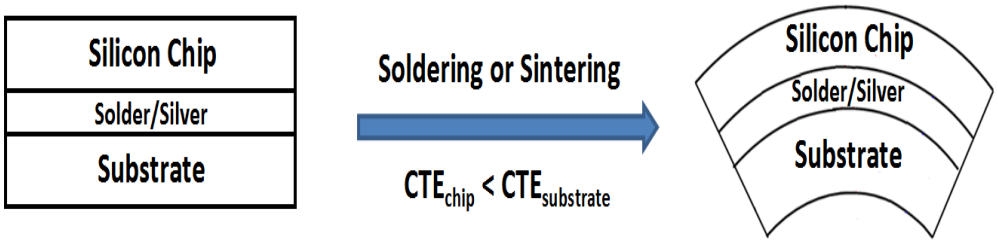


Figure 7-16. Formation of curvature in die-attachment [126] (Used under fair use guidelines, 2011).

Figure 7-17 shows the experimental results of the attachment of power module to aluminum heatsink using SAC305 lead free solder. The equivalent CTE of power module (10.3 ppm/^{o}C) is much less than that of the aluminum heatsink (23.1 ppm/^{o}C). As a result, after reflow process (peak temperature of 270^{o}C), the DBA substrates suffers from high tension stress and the aluminum heatsink is under compression stress. The whole structure is bent as shown in Figure 7-17.

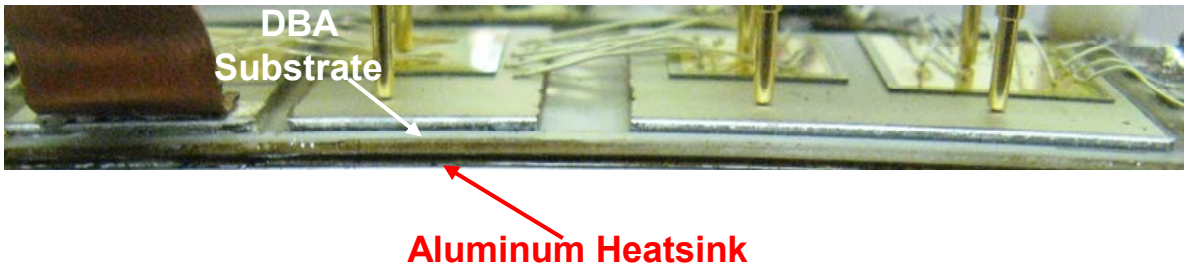


Figure 7-17. Bending of DBA after reflow process.

This thermal mismatch induced residual stresses are identified as one of the major causes of voiding and failure of bonding layers in electronic packaging. The thermal cycling will cause growth of the microcracks and voids, resulting in redistribution of the residual stress in the bonding layers [127] [128]. Therefore, the curvature will be reduced with releasing of the residual stress along the thermal cycling via increasing of the cracks and voids. In [126] and [129], the experimental results show that the decreasing of the curvature along thermal cycling indicates growth of the cracks and delaminations. In the thermally cycled samples with zero curvature, the images of scanning electron microscopy illustrate large cracks and delaminations in bonding layer. For this reason, the curvature of the samples can be monitored and used for failure detection.

7.3.4. Curvature Measurement using Laser Scanning

The next step in this work is to find a reliable method to detect the curvature of samples before and after thermal cycling. Curvatures could be measured without direct contact methods (video, laser scanning, grids, and double crystal diffraction topology). In this study, an optical method was used for the curvature measurement. The measurement set-up is shown in Figure 7-18 and its schematic is shown in Figure 7-19.

Figure 7-18. The optical setup for the curvature measurement [129] (Used under fair use guidelines, 2011).

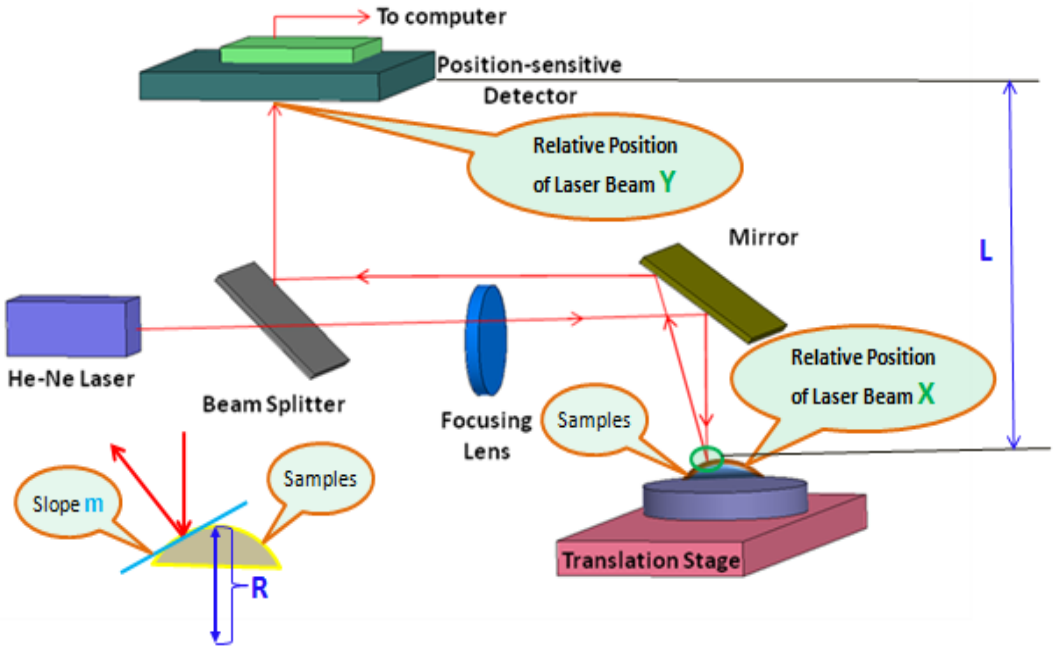


Figure 7-19. Schematic of the optical setup for the curvature measurement.

The optical setup mainly consisted of two parts: the optical scanning component and the hot stage mounted on the translation stage. Specifically, it consisted of a low-power HeNe laser (4 mW), beam splitter, mirror, focusing lenses, and a position-sensitive detector. During the curvature measurement, a bi-layer composite specimen was placed on the setter in the hot stage with the coated surface facing down. Then the smooth substrate surface (typically silicon) would reflect the incoming laser beam. The translation stage could carry the specimen to move so that the laser beam scanned a certain distance d on the curved composite specimens as shown in Figure 7-20. During the scanning, the reflected laser beam would be projected onto a position-sensitive photo-detector so that the distance changes d' due to the curvature could be recorded.

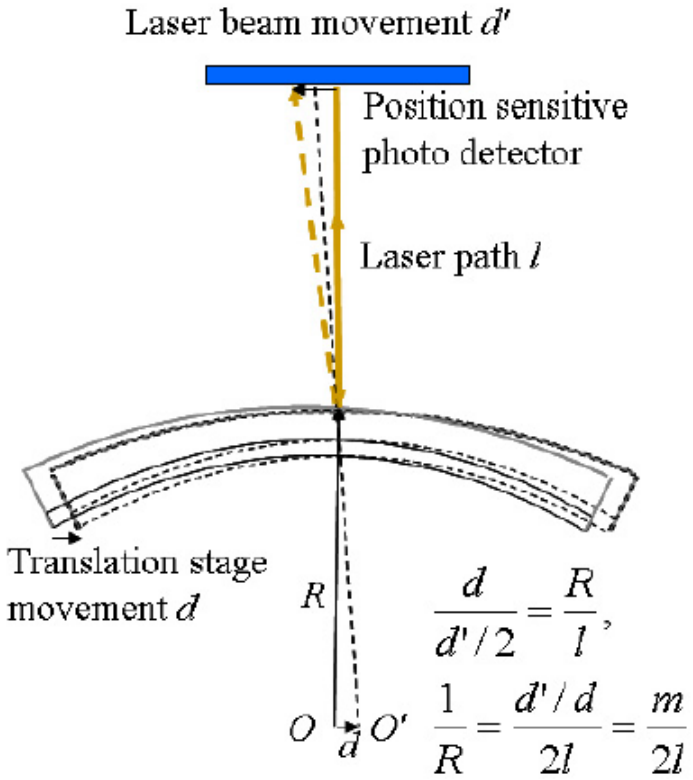


Figure 7-20. Mechanism of curvature measurement by optical set-up [130] (Used under fair use guidelines, 2011).

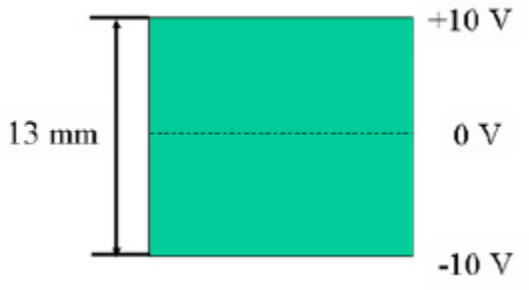


Figure 7-21. Schematic of the position-sensitive photo-detector [131] (Used under fair use guidelines, 2011).

The position-sensitive photo-detector (Hamamatsu Corporation) could linearly change the perpendicular positions of an incoming laser beam into the output voltage values as shown in Figure 7-21. With the assistance of the photo-detector, the translate relationships in the optical setup during the measurement were shown in Figure 7-20. In the relationships, m=d'/d is the slope during the curvature scan and it could be determined by the experiment. So once the length of the optical path length L is measured, we can get the value of curvature, which equaled to 1/R.

Simply speaking, the curvature of the tested sample would calculated by using equation (7-2),where m was obtained by scanned data and L was constant. In this study, L is 0.85, the distance between the substrate and detector.

$$\kappa = \frac{1}{R} \approx \left(\frac{m}{2L} \right) \tag{7-2}$$

The original results from the scanning were two columns of data. They, respectively, represented the relatively detector position and relative position of the laser beam. The data of detector position from scanning was record by the electrical signal, that is, the voltage. Thus it needs to multiply a factor 0.65 to be converted into data in length. Figure 7-22 shows the measurement data for one sample with 3 × 3 trenched copper plate before thermal cycling and after 300 thermal cycles. The linear curve fitting is used to obtain the slope (m) for different cases. It can be seen that the measured data can match with the

fitting lines very well. As expected, the measured slope decreases from 3. 292 to 2.1429 after 300 cycles, indicating the reduction of curvature.

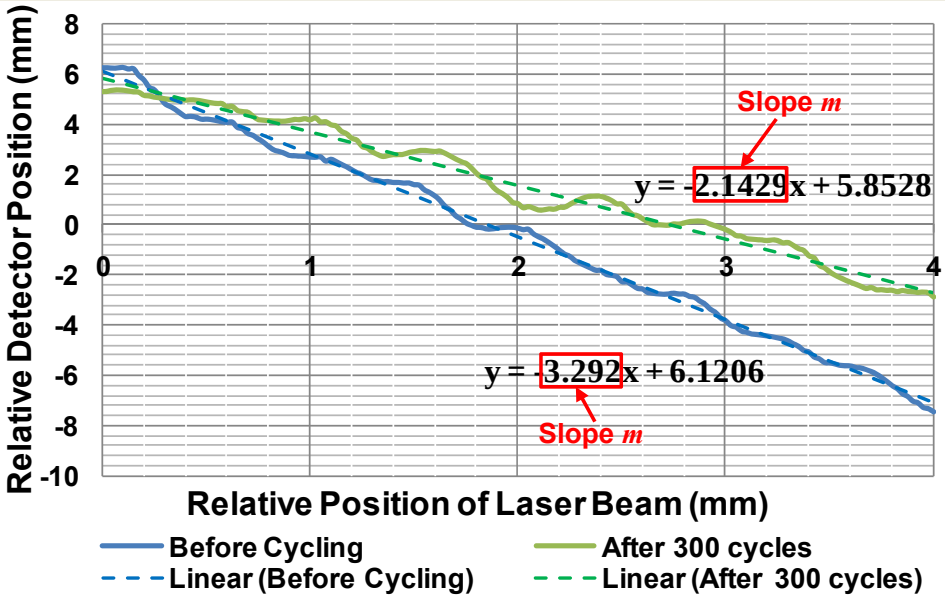


Figure 7-22. Measurement data of one sample with 3 × 3 copper plates from laser system (solid line: measurement data; dash line: linear curve fitting).

7.4. Experimental Results and Discussions

7.4.1. Curvature Change of Thermally Cycled Samples

The twenty-four samples (eight samples for each type) were thermally cycled. The curvature of each sample measured before thermal cycling was used as reference. After thermal cycling, the curvature was re-measured and compared with the reference. Figure 7-23 plots the sample curvatures of different types copper plates with error bars. It can be seen that the curvatures for the samples with the same type of copper plate are very consistent and the variation among the samples is within the range of ±15%. In addition, the initial curvatures for different samples are similar. For the samples with conventional copper plate, the curvatures decrease dramatically at the beginning of the thermal cycling test. After 100 cycles, the curvatures of those samples were reduced by more than 80%

(shown in Figure 7-24). The curvatures of six out of eight samples with 1 × 1 copper plate became zero after 300 cycles, which indicates cracks and delaminations emerged in those samples. The curvatures of samples with 2 × 2 trenched copper plates and 3 × 3 trenched copper plates also decreases with the thermal cycling. After the first 100 cycles, the average curvatures for samples with 2 × 2 copper plates and 3 × 3 copper plates reduced to 68.5% and 75.3% of their original curvatures. However, after 150 cycles, the curvatures of these samples tend to be stable. From 150 cycles to 400 cycles, the curvatures of 2 × 2 samples and 3 × 3 samples were only reduced by 7.3% and 2.2%, respectively. This indicates that there are no large number of cracks and delaminations in the solder layers of samples with trenched copper plate that can help release residual stress. From Figure 7-23 and Figure 7-24, it also can be seen that the samples with 3 × 3 trenched copper plates have slightly smaller initial curvature and lower rate of curvature reduction than the samples with 2 × 2 copper plates. However, up to 400 cycles, the difference between these samples are not pronounced. The thermal cycling of the samples is still on-going.

7.4.2. SEM Inspection on Thermally Cycled Samples

In order to confirm less cracks and delaminations in the bonding layers for samples with trenched copper plate structure, two samples (one sample with 3 × 3 trenched copper plate and one with single copper plate) were cross-sectioned and examined using scanning electron microscopy (SEM). SEM is a powerful tool in inspecting the microstructure of electronic components and material interfaces. Major steps include sectioning and cutting, mounting, planar grinding, polishing and etching [129].

The first step to prepare samples for SEM is to cross-section the sample at the area of interest using abrasive cutting or diamond wafer cutting. Next, the specimen is encapsulated using mounting resins (acrylic resins, epoxy resins, and polyester resins) to protect the specimen edge and maintain the integrity of surface features. The encapsulated specimen is shown in Figure 7-25(a). A subsequent planar grinding

planarizes the sample cross-sections and exposes the exact area of interest. A sequentially decreasing grit/particle size of the silicon carbide abrasive paper is normally used. For electronic components that have multiple materials with different hardness, it is recommended that fine abrasives such as 800 or 1200 grit SiC be used after sectioning to prevent brittle devices such as silicon from cracking. A coarser grit abrasive might produce more damage to the specimen that sectioning. Hard ceramic substrates, such as alumina, should be rough polished with diamond lapping films to minimize edge rounding. For SEM analysis, polishing of the specimen using diamond or alumina fine powder is usually required. The particle size starts from 5 µm, 1 µm, and can be as fine as 0.05 µm. Ultrasonic cleaning is recommended after every particle size polishing to thoroughly clean the surface because residual powder from last polishing step may contaminate the next level polishing mixtures and cause scratches on the sample surfaces.

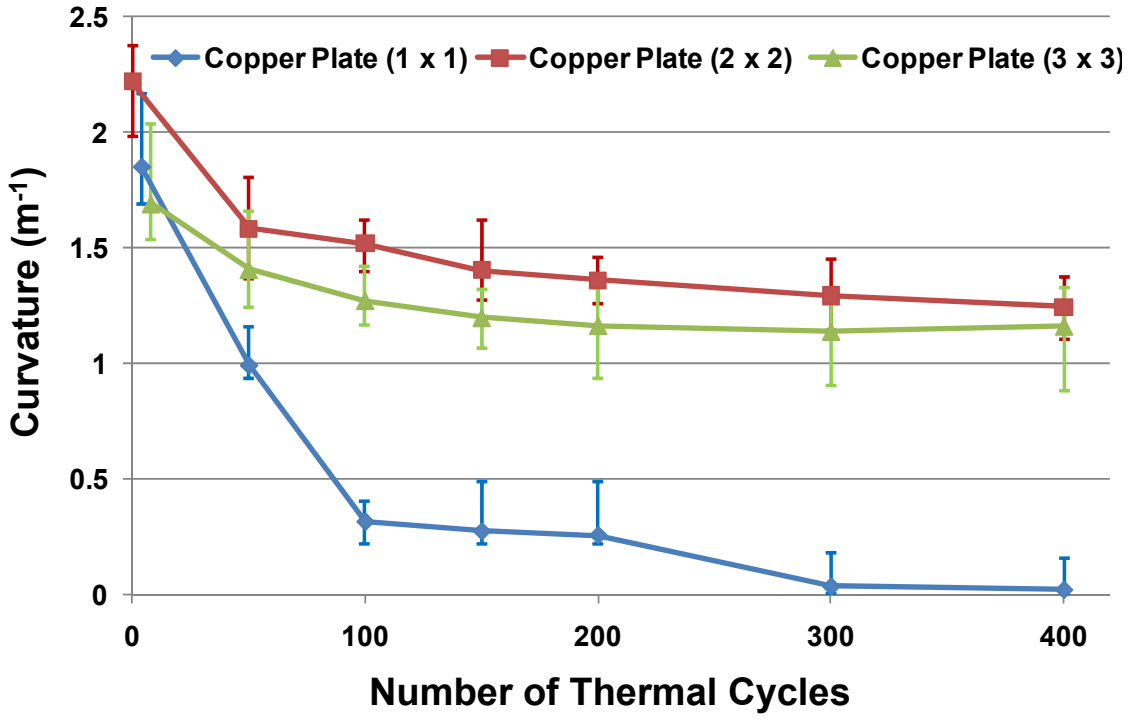


Figure 7-23. Curvature vs number of thermal cycles for different types of samples.

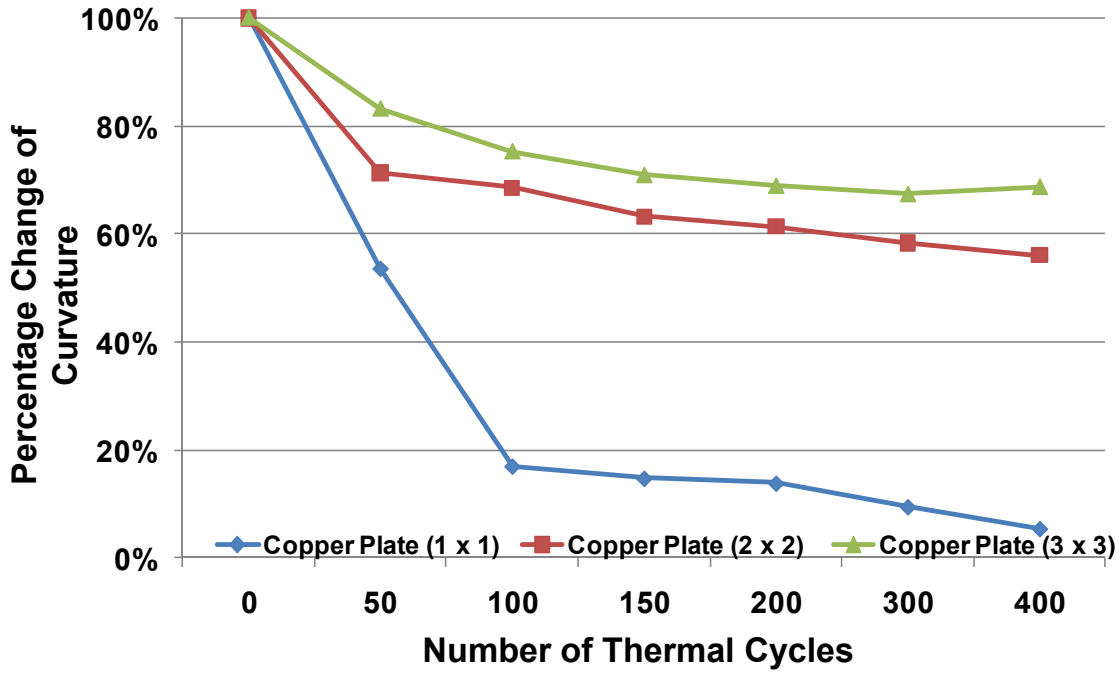


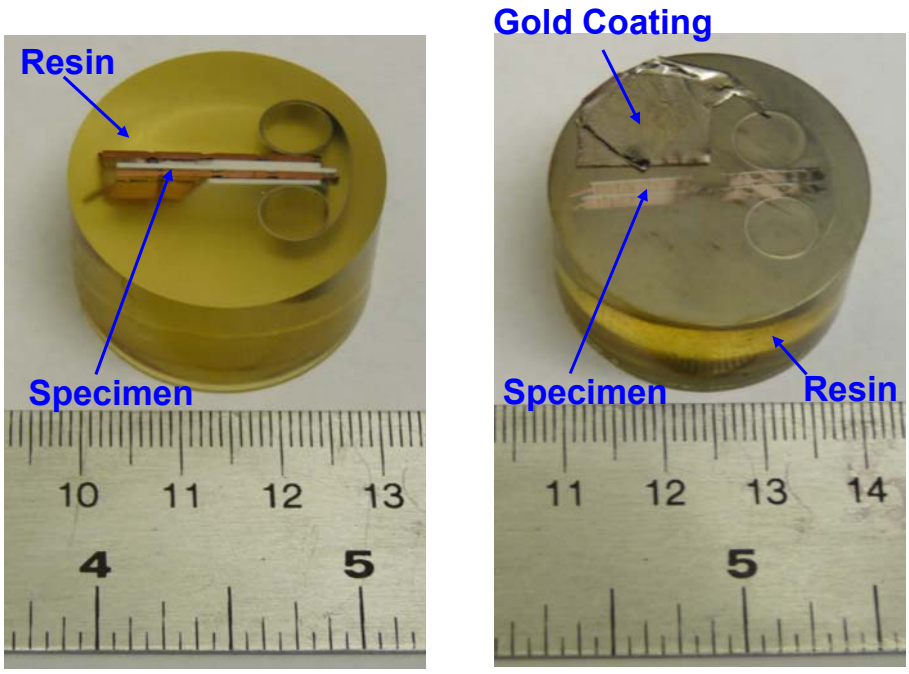
Figure 7-24. Percentage change of curvature vs number of thermal cycles for different types of samples.

After polishing, an ultrathin coating of gold was deposited on the surface of the sample using low vacuum sputtering coating to improve the conductivity of sample surface. Figure 7-25(b) shows the sample coated with gold.

Figure 7-26 and Figure 7-27 show the SEM images of one sample with 3 × 3 trenched copper plate and one sample with single copper plate after 300 cycles. The curvature of the sample with 3 × 3 copper plates was reduced to 72% of its original value after 300 cycles. However, for the sample with single copper plate, the curvature already dropped to zero after 300 cycles, indicating that there were cracks and delaminations in the solder layer to release the residual stress. From the stress simulation, it can be seen that the maximum stress occurs at the edge of the solder layer. Therefore, the examination focuses on the edges and corners of the solder layers. Figure 7-26(a) gives the image at the edge of solder for the sample with 3 × 3 trenched copper plate. From SEM image, there are no noticeable cracks or delaminations observed. Figure 7-26(b) shows the close-up view of the corner of the solder layer, which further confirms the

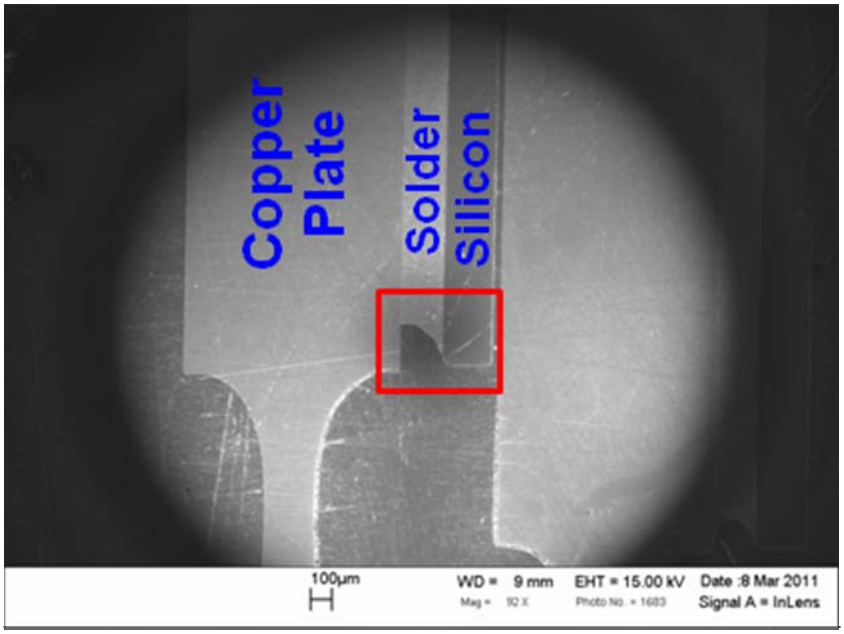
solder integrity. Figure 7-27 shows the SEM images for the sample with single copper plate. After 300 cycles, obvious cracks starting from the edge of the solder layer can be found in this sample. The length of the cracks is as long as 1.8 mm, which could cause severe degradation in electrical, thermal, and mechanical performances of the power module. The close-up view of the highlighted region in Figure 7-27(a) is shown in Figure 7-27(b). The cracks and delaminations are even more noticeable in this figure.

The SEM images verified the correlation between the curvature and the growth of cracks in the solder layer. In addition, the results also prove that the sample with 3 × 3 trenched copper plate has better reliability than the sample with single copper plate.

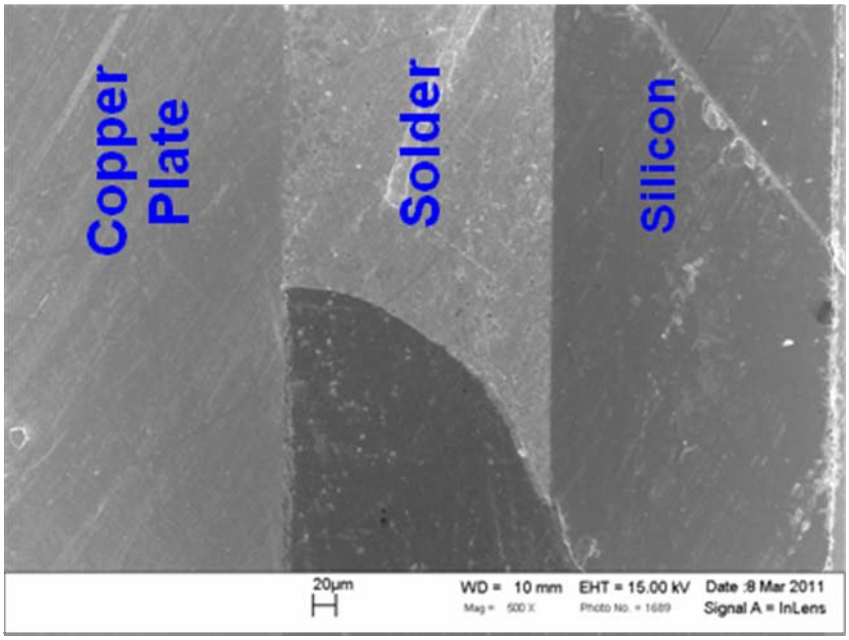


(a) (b)

Figure 7-25. Sample prepared for SEM inspection: (a) after encapsulation; (b) after gold coating.

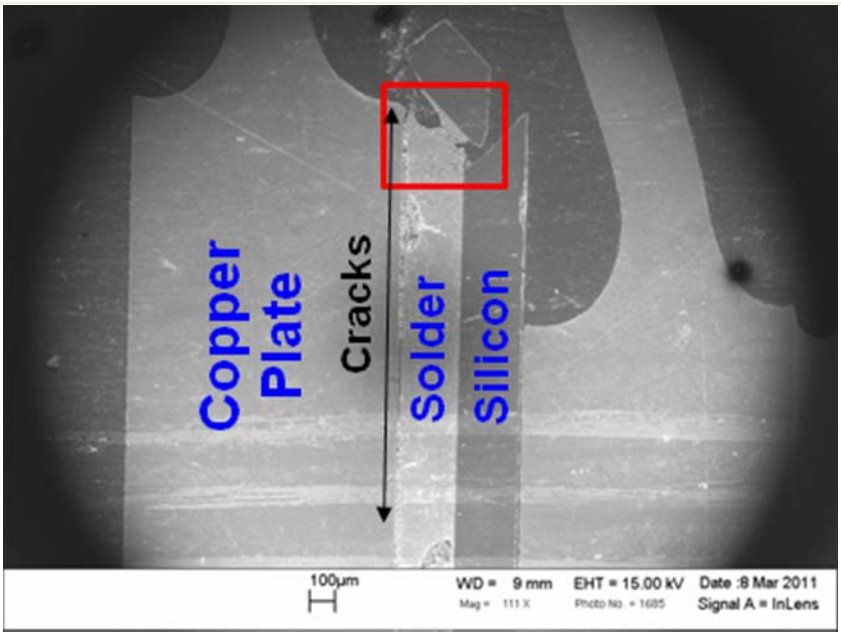


(a)

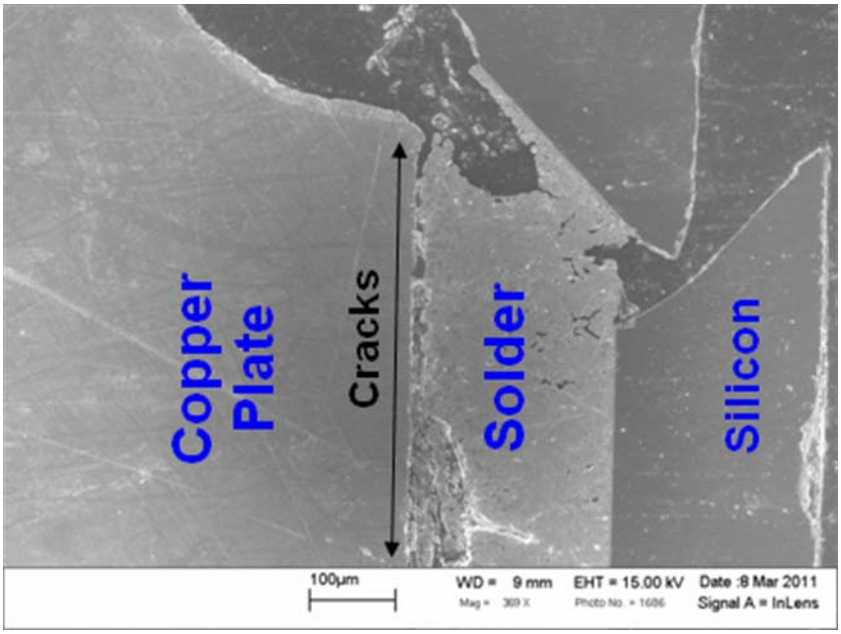


(b)

Figure 7-26. SEM images of the sample with 3 × 3 copper plate (a) and the close-up view of the edge of solder (b).



(a)



(b)

Figure 7-27. SEM images of the sample with single copper plate (a) and the close-up view of the edge of solder (b).

7.5. Conclusions

In this chapter, twenty-four samples with different shapes of copper plates were fabricated to demonstrate the better reliability brought by trenched copper plate structure. All the samples were thermally cycled from -40˚C to 105˚C. It is reported that the thermal cycling induced cracks and delaminations would cause release and redistribution of residual stress in the samples, resulting in the decreasing of the curvatures. Therefore, the curvatures of the samples were measured and used as indicator for failure of solder joints. Experimental results show that the curvatures of six out of eight samples with single copper plate became zero after 300 cycles. However, the curvatures of the samples with 2 × 2 trenched copper plates and the samples with 3 × 3 trenched copper plates still remained 68.5% and 75.3% of their original values. This shows better reliability of the samples with trenched copper plate structure. To further confirm the reliability test results, one sample with single copper plate and one sample with 3 × 3 trenched copper plate were cross-sectioned and scanned using SEM after 300 cycles. The SEM images indicate that the obvious cracks occur from the edge of the solder layer for the single copper plate sample. However, for the sample with 3 × 3 trenched copper plate, there is no noticeable crack or delamination observed from the SEM images. The inspection results further verified the benefit of trenched copper plate structure.

Chapter 8. CONCLUSIONS AND FUTURE WORK

8.1. Introduction

This dissertation focuses on the development of a power module with low thermal impedance and low thermo-mechanical stress for medium-power application. The thermal modeling, thermal impedance measurement, thermo-mechanical stress simulation, and structure design to reduce the thermo-mechanical stress in the power module were discussed in the dissertation.

With increasing of power density, more and more critical thermal requirements that include both steady-state and transient thermal requirements are imposed on the power module design. Therefore, a transient thermal model is necessary for thermal design and thermo-electrical coupling simulation. Conventional compact thermal models are derived from material properties and geometries of the power module and independent on boundary conditions. This assumption was proved to be inaccurate, especially for cases with high heat transfer coefficient as boundary conditions. In this dissertation, a boundary-dependent compact thermal model was proposed. Compared to conventional boundary-independent thermal model, the proposed model can predict the transient thermal response of power module more accurately. Since the transient thermal performance has to be investigated, this dissertation also discussed the method for thermal impedance measurement. A measurement method using the gate-emitter voltage of an IGBT as temperature sensitive parameter was proposed. The measurement results were used to characterize three different die-attach materials.

Thermal analysis showed that the conventional wirebonded power module was not able to meet both steady-state and transient thermal performances. The plate-bonded power module can improve the transient thermal performance without degrading the steady-state performance. However, the copper plate causes large thermo-mechanical

stress. In this dissertation, a trenched copper plate power module was proposed to achieve both good thermal performance and thermo-mechanical performance. The dissertation discussed the design trade-off between the thermal performance and thermo-mechanical performance. The results were verified using both simulation and experiment.

8.2. Main Contributions and Conclusions

1. A boundary-dependent transient thermal model was proposed. In the proposed model, each layer in the power module is represented by a thermal resistor. The resistances can be calculated using the material properties of the layer and the effective heat spreading area. The conventional way to estimate the effective heat spreading area is based on the assumption that the heat spreads in the power module with a fixed spreading angle of 45^{o}. However, the results from finite element simulation show that the effective heat spreading area is a function of heat transfer coefficient and geometries of the power module. In the proposed model, the relation between the heat transfer coefficient, the geometries of the module, and the effective heat spreading area is established using response surface method. The thermal model was verified using finite element simulation. The maximum error from the boundary-dependent thermal model is only 6.31% which is much lower than the error from the model based on heat spreading angle of 45˚ (69. 34%). In addition, the transient thermal model was extracted from only steady-state thermal simulation, which significantly saved computing time.
2. A means to measure the thermal impedance of a fully-packaged power module was proposed. Experimental results show that the gate-emitter voltage of the power IGBT is five times more sensitive than the forward voltage drops of the diode. Therefore, a measurement system based on monitoring gate-emitter voltage change to measure the junction temperature of the IGBT was designed.
3. The designed thermal impedance measurement system was used to evaluate the quality of two lead-free solders and sintered nano-silver. Experimental results

show that the sample using sintered nano-silver for the die-attach has a 12.1% lower thermal impedance than the samples using SAC305 and SN100C solders. To check the degradation of the die-attachment, three samples using three die-attach materials were thermally cycled from -40˚C to 125˚C. The experimental results show that after 500 cycles, the thermal impedance of SAC305 samples and SN100C samples is increased by 12.8% and 15%, respectively, which is much higher than the sample using the sintered nano-silver for the die-attach (increased by 4.1%).

4. The thermal performance of the conventional wirebonded power module was evaluated. Under high heat transfer coefficient condition, the heat-spreader of the wirebonded power module cannot effectively reduce the thermal resistance by enhancing the heat spreading effect. Thus, the heat-spreader should be eliminated. However, removal of the heat-spreader will lead to lack of the thermal mass during thermal transient, which increases transient peak temperature in the module. Due to the limitation of heat-spreader, the wirebonded power module cannot achieve both good steady-state and transient thermal performance.
5. A plate-bonded power module was proposed to improve the thermal performance of the power module. In the plate-bonded power module, the dice were sandwiched between two substrates. The heat-spreader was removed to reduce thermal resistance and a copper plate was inserted between the top surface of silicon dice and the top substrate to add thermal mass so that the peak transient temperature can be reduced. From simulation, it can be seen that compared to the wirebonded power module, the plate-bonded power module can reduce the thermal resistance by 16% and thermal impedance by 0.28^{o}C/W for 0.2 s transient.
6. The thermo-mechanical stress distribution in the plate-bonded power module was simulated using ANSYS. The results showed that due to large CTE mismatch

between copper plate and silicon dice, the maximum stress in the plate-bonded power module is 31.9% higher than the wirebonded power module, resulting in poor reliability.

7. A trenched copper plate structure was proposed to reduce the stress in the power module by slightly degradation of thermal performance. In the proposed, the large copper plate was divided into several smaller pieces and connected together via a thin layer of copper to reduce the bonding area for each copper plate. Smaller footprint area for each piece of copper plate can reduce the maximum stress in the bonding layer. However, the clearance in the copper plate-array results in less thermal mass to minimize the peak transient temperature in the power module. Therefore, the trade-off between the thermal performance and the thermo-mechanical performance was also discussed.
8. It was experimentally verified that copper plate-array structure can reduce the thermo-mechanical stress in the power module, leading to better reliability. Twenty-four samples with three different structures were fabricated and thermally cycled from -40˚C to 105˚C. The curvature of the samples was measured using laser system and the measurement results were used as failure criterion. Curvature is a reflection of residual stress induced by thermal process. Large curvature means high residual stress in the bonding layer. For samples using single copper plate, the curvature became almost zero after only 100 cycles, indicating cracks and delaminations occur at the bonding layer and help release the residual stress. However, for samples with trenched copper plate structure, the change of the curvature was less than 40% after 400 cycles. The x-ray pictures of cross-sectioned samples confirmed that after 300 cycles, the bonding layer for the sample with single copper plate has many cracks and delaminations starting from the edge. However, no noticeable cracks were observed in the bonding layer of the sample with 3 × 3 trenched copper plate structure.

8.3. Future Work

The work presented in this dissertation can be further extended. This can make the work on design of the power module more comprehensive and valuable. The following subjects have not been studied in this dissertation and are suggested to be the topics of future work:

- Thermal modeling and design for multichip power modules
- Thermo-mechanical stress analysis for multichip power modules
- Evaluation of thermal and thermo-mechanical performances of plate-bonded power modules with different materials for plates
- Investigation of impacts from solder joint shape on thermo-mechanical performance of power modules
- Improvement of process for fabrication of trenched copper plate power modules

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APPENDIX A: Simulation of Thermal Performance of Power Module

In this dissertation, both steady-state and transient thermal simulation of power module are simulated using Ansoft ePhysics software. EPhysics' ability to refine the mesh adaptively allows trade-off between numerical accuracy and computation time. The steps for thermal simulation are shown as follows:

1. Build model in ePhysics

   The interface of ePhysics is shown in Figure A-1. The model can be built by using the 1D, 2D, and 3D shapes in the toolbar.

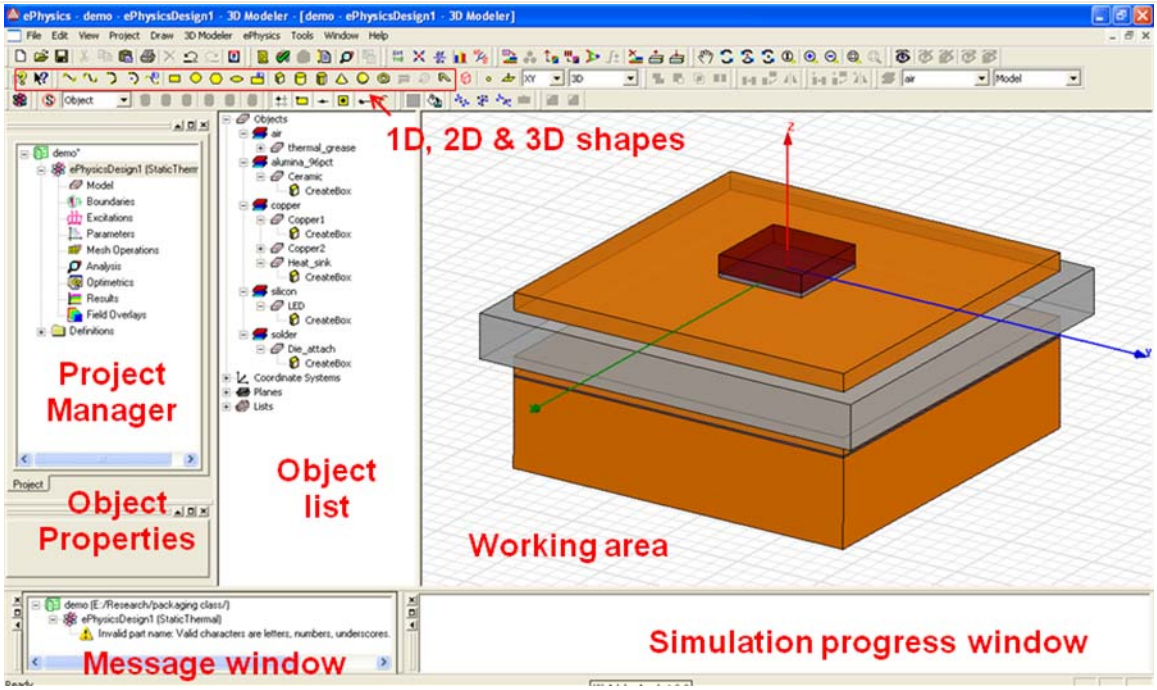


Figure A-1. Interface of ePhysics thermal simulation.

2. Select solution type

   After building the physical model in ePhysics, the solution type can be selected as shown in Figure A-2. Based on different application, the "Static Thermal" or "Transient Thermal" simulation will be performed.

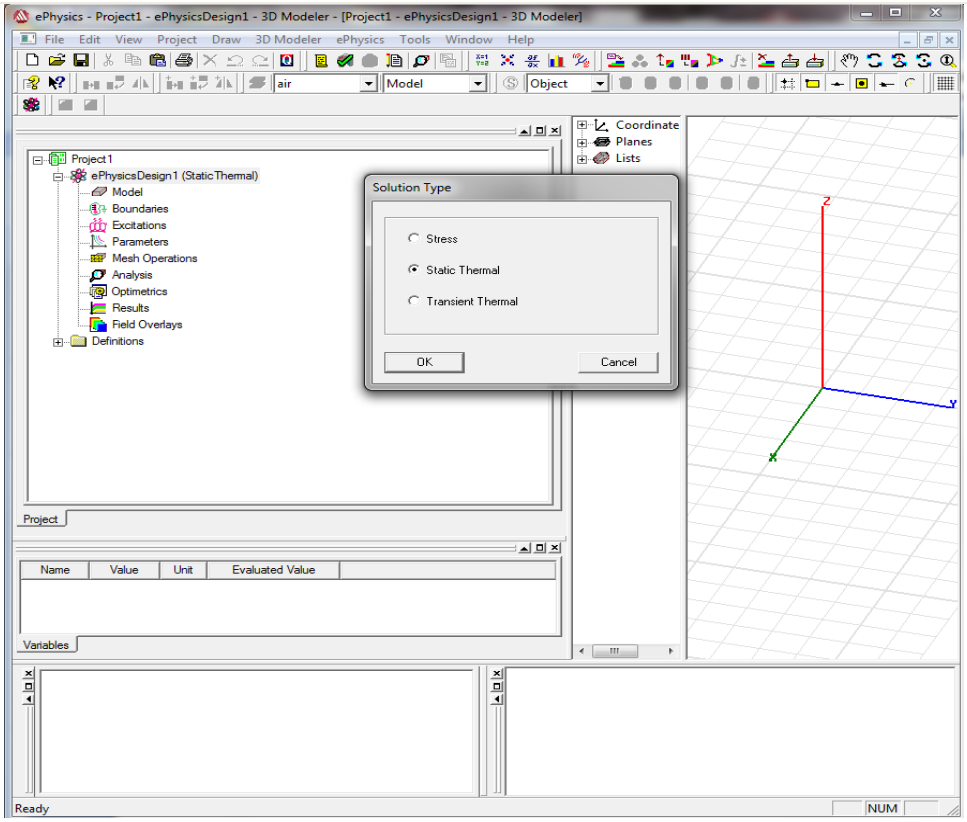


Figure A-2. Selection of simulation type.

3. Assign material properties for the model

   The ePhysics has its own material library that includes the most widely-used materials in electronic packaging. To assign material properties to an object, the object is firstly selected and then right click to select the "material properties" tag. The material can be selected from the material property table.

4. Assign excitations

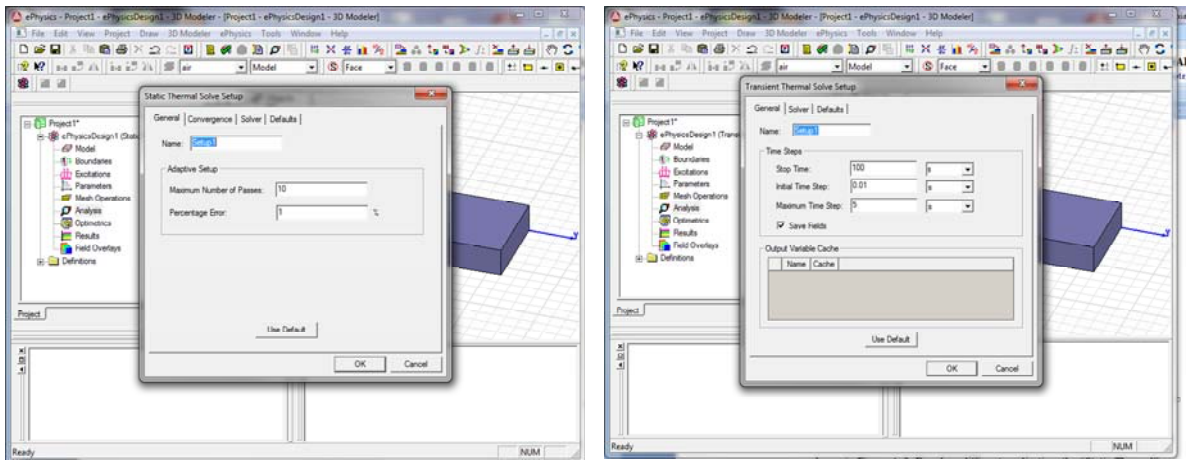
   Excitation of the thermal simulation is the heat source in the power module. In this application, since the junction of the power semiconductor is very shallow, the top surface of the IGBT can be considered to be the heat source. Thus, select the top surface of the IGBT and right click to select "assign excitation" tag to input the total power loss in the IGBT.

5. Assign boundary conditions

In this application, the heat-exchanger is installed underneath of the power module and majority of the heat is dissipated from the bottom surface of the power module. Therefore, a uniform heat transfer coefficient is applied to the bottom surface of the power module. Select the bottom surface and assign “heat transfer” boundary condition to it. The rest of surfaces of the power modules are adiabatic.

6. Setup analysis

   After setting the boundary conditions, the analysis can be set up as shown in Figure A-3. For static thermal analysis, the default values can be used. However, for transient thermal analysis, the stop time, initial time step, and maximum time step have to be assigned.



(a) (b)

Figure A-3. Analysis setup for static thermal simulation (a) and transient thermal simulation (b).

7. Post processing

   After simulation, the temperature contour can be plotted by selecting the interested objects and clicking Fields Overlays -> Fields-> Temperature as shown in Figure A-4.

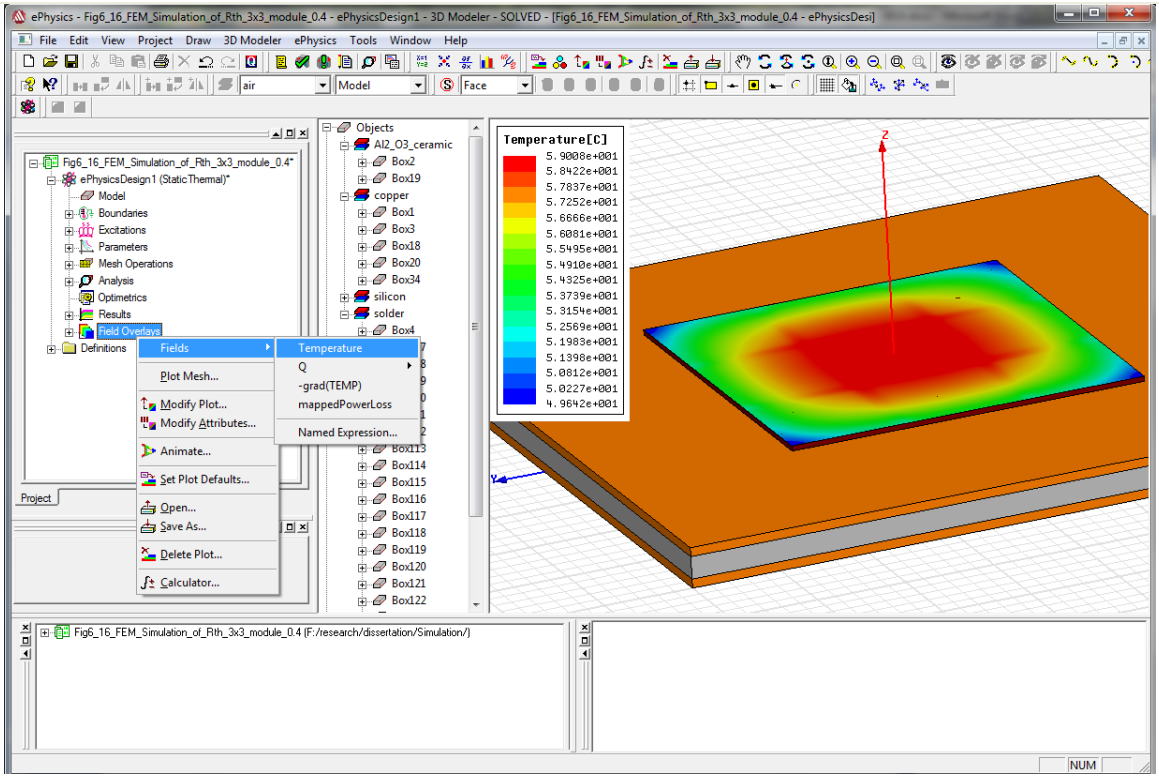


Figure A-4. Post processing to plot temperature contour.

APPENDIX B: SIMULATION OF THERMO-MECHANICAL PERFORMANCE OF POWER MODULE

In this dissertation, the thermo-mechanical stress and strain distributions in the power module are simulated using ANSYS software. The based steps for thermo-mechanical simulation of the power module are shown as follows:

1. Build model in ANSYS

   The interface of ANSYS is shown in Figure B-1. The model can be built by using the commands in modeling section under ANSYS Main Menu-> Preprocessor (highlighted part in Figure B-1). After build the model, the entire model should be portioned into many small parts so that different meshing density can be applied to different parts. By doing this, better trade-off between simulation time and accuracy can be achieved. After partition, all parts have to be glued together by using “Glue” command. Therefore, the volumes can be redefined so that they share areas along their common boundaries.

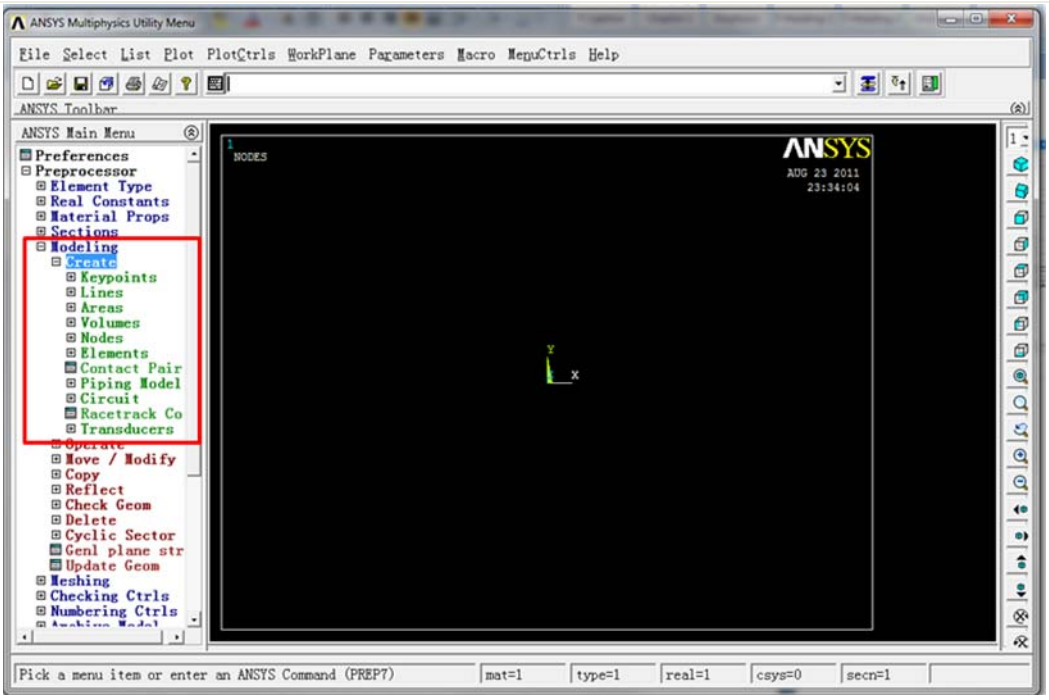


Figure B-1. Interface of ANSYS thermo-mechanical simulation.

2. Assign material properties and element type

The material properties used in the simulation can be set up using the commands under Preprocessor ->Material props under ANSYS Main Menu as shown in Figure B-2. The detailed material properties were discussed in Section 6.1.3 in the dissertation.

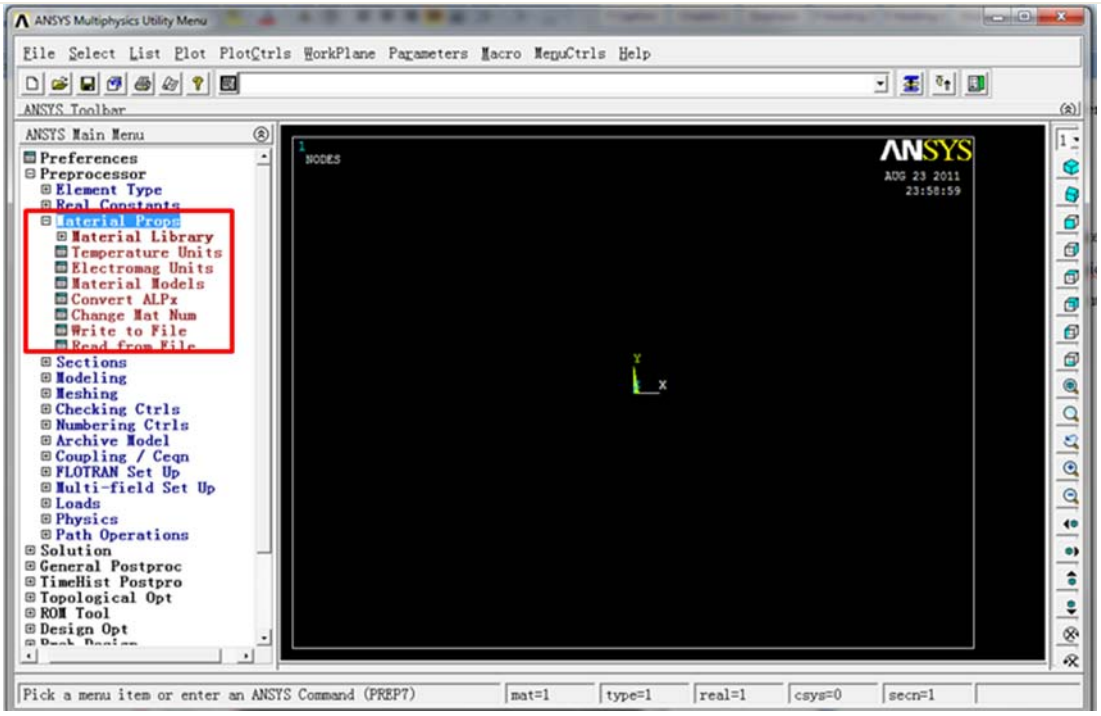
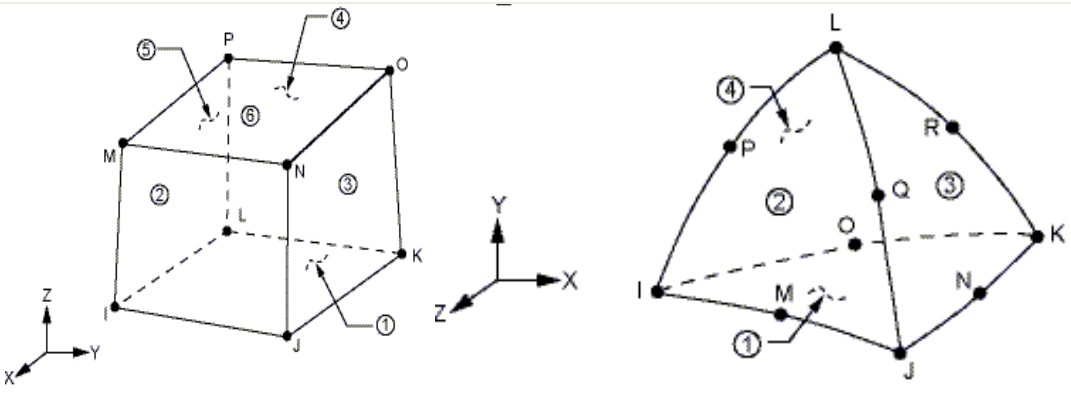


Figure B-2. Assign material properties in the simulation.

Two element types are used in the simulation. For SAC305 solder, element SOLID185 (Hexahedral element) is used as shown in Figure B-3(a). The element is defined by eight nodes and the orthotropic material properties. For rest of materials, SOLID187 element is used. SOLID187 element is a higher order 3-D, 10-node element. SOLID187 has a quadratic displacement behavior and is well suited to modeling irregular meshes (such as those produced from various CAD/CAM systems). The element is defined by 10 nodes having three degrees of freedom at each node: translations in the nodal x, y, and z directions.



(a) (b)

Figure B-3. Element types used in thermo-mechanical simulation (a) element SOLID185 and (b) element SOLID187.

3. Mesh the model

The detailed meshing rules have been discussed in Section 6.1.4. Since the focus of the study is the stress/strain distribution in the bonding layers, fine mesh is used for all solder layers. Also, the edge of the bonding layer suffers from higher stress. Therefore, the mesh is denser at the edge and corner area. The mesh in the bonding layers is shown in Figure B-4. The rest components can be meshed by using automatic mesh function in ANSYS.

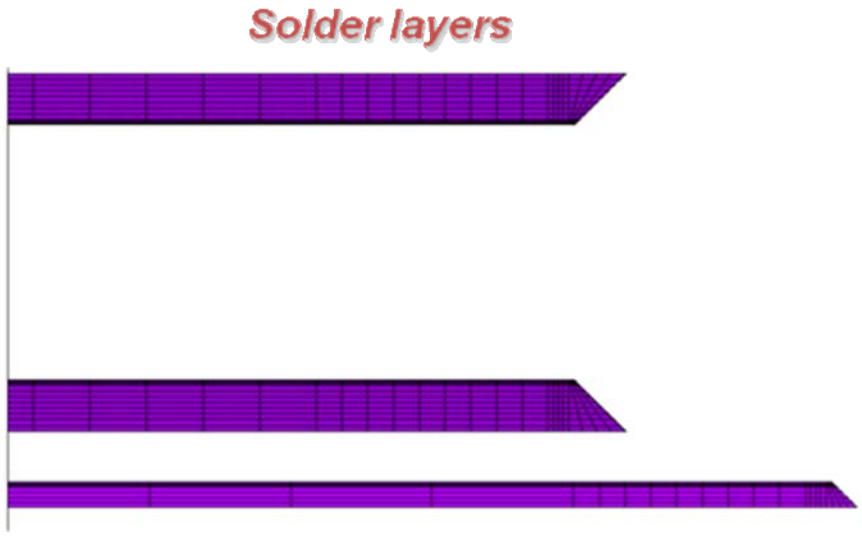


Figure B-4. Mesh in the bonding layers.

4. Apply the boundary conditions and loads

In thermo-mechanical simulation, the displacements of several key points have to be fixed to simulate boundary conditions of thermal cycling. Thanks to sysmetric structure of the power module, only one quarter of the power module needs to be simulated. The boundary conditions applied are shown in Figure B-5.

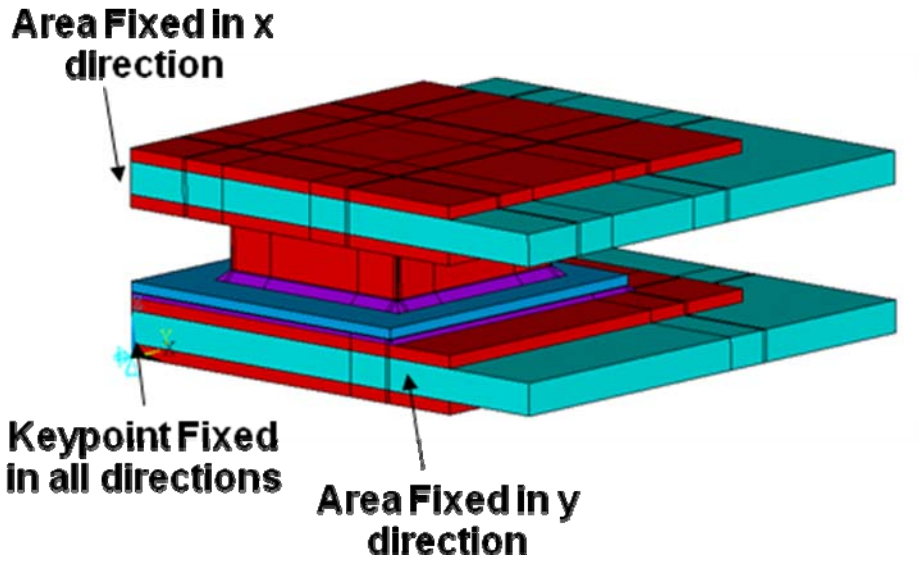


Figure B-5. Boundary conditions for power module.

The stress-free temperature can be set from Solution-> Define Loads -> Settings -> Reference Temp. In this simulation, the stress-free temperature is set to be 25°C and the stress/strain distribution at 125°C is simulated. Therefore, the temperature load can be set through Solution -> Define Loads -> Apply -> Structural -> Temperature -> Uniform Temp.

5. Simulate the thermo-mechanical performance of the power module

After the boundary conditions and the thermal load have been applied, the simulation can be started by selecting Solve -> Current LS as shown in Figure B-6.

6. Plot stress/strain distribution in the bonding layers

After finishing the simulation, the stress and strain distribution in the power module can be plotted. Go to General Postproc -> Read Results -> Last Set to load the simulation results. After loading simulation results, go to General Postproc -> Plot

Results -> Contour Plot -> Nodal Solu. The following dialog box occurs (shown in Figure B-7). In the dialog box, select von Mises stress and strain to plot it.

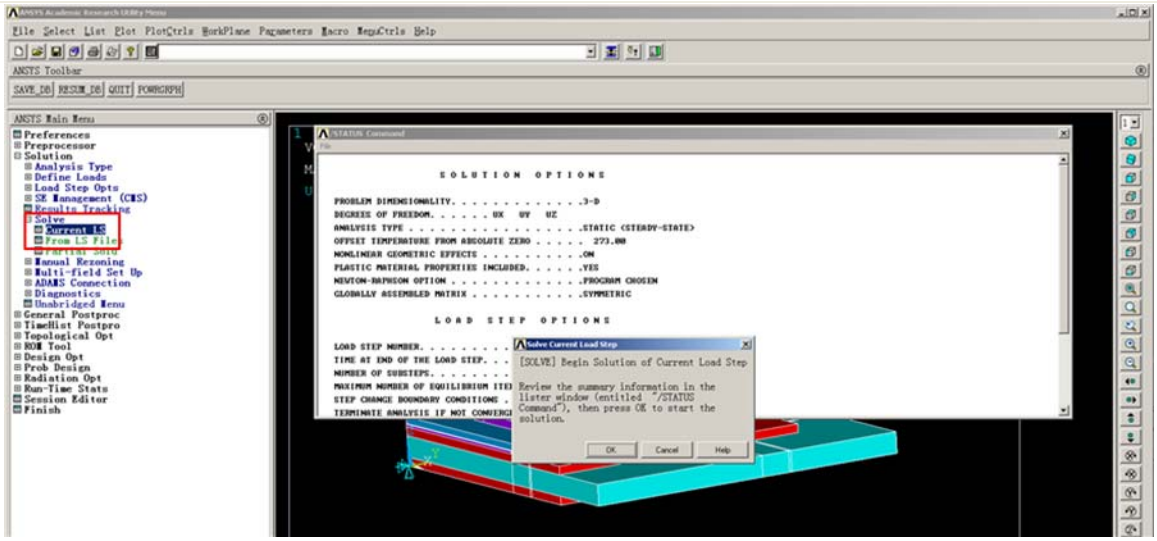


Figure B-6. Start to simulate the thermo-mechanical performance of the power module.

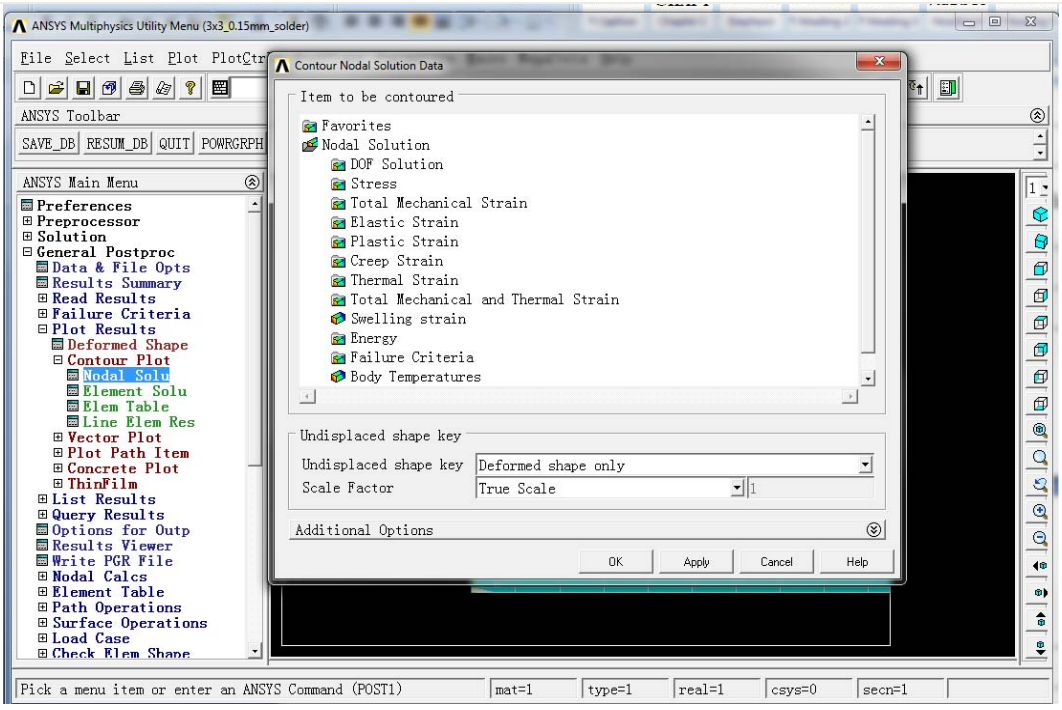


Figure B-7. Plot the stress and strain distributions in the power module.

LIST OF PUBLICATIONS

JOURNAL PAPERS

[1] X. Cao, T. Wang, K.D.T. Ngo, and G-Q. Lu, "Parametric Study of Joint Height for a Medium-Voltage Planar Package," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, No. 3, September, 2010, pp. 553-562.

[2] X. Cao, T. Wang, G-Q. Lu, and K.D.T. Ngo, "Characterization of Lead-Free Solder and Sintered Nano-Silver Die-Attach Layers Using Thermal Impedance," *IEEE Transactions on Components, Packaging and Manufacturing Technologies,* vol. 1, No. 4, April, 2011, pp. 495-501.

CONFERENCE PAPERS

[1] X. Cao, T. Wang, K.D.T. Ngo, and G-Q. Lu, "Height Optimization for a Medium-Voltage Planar Package," *Proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 479-484, February 14-19, 2009, Washington DC, USA.

[2] X. Cao, K.D.T. Ngo, and G-Q. Lu, "Thermal Design of Power Module to Minimize Peak Transient Temperature," *Proceedings of 2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, pp. 248- 254, August 10 -13, 2009, Beijing, China (will be submitted to *IEEE Transactions on Components and Packaging Technologies*).

[3] X. Cao, T. Wang, Z. Tan, K. Ngo, S. Luo, and G-Q. Lu, "Development of a Double-side Cooled Power Modules Joined by Low-temperature Sintering of Nanosilver Paste for Electric Vehicles," in proceedings of IMAPS 2nd ATW on Automotive Microelectronics and Packaging**,** April 27-28, 2010**,** Dearborn, Michigan.

[4] X. Cao, T. Wang, G-Q. Lu, and K.D.T. Ngo, "Characterization of Lead-Free Solder and Sintered Nano-Silver Die-Attach Layers Using Thermal Impedance," *Proceedings of IEEE International Power Electronics Conference (IPEC),* pp.546-552, June 21-24, 2010, Sapporo, Japan.

PAPERS UNDER REVIEW

[1] X. Cao, G-Q. Lu, and K.D.T. Ngo, “Boundary-Dependent Circuit Model for the Transient Behavior of a Thermal Stack in Power Modules,” Accepted by IEEE Energy Conversion Congress and Exposition, 2011.

PAPERS WILL BE SUBMITTED

[1] X. Cao, G-Q. Lu, and K. D. T. Ngo, “Thermal Design of Power Module Based on A Phenomenological Transient Thermal Model”.

[2] X. Cao, G-Q. Lu, and K. D. T. Ngo, “A Planar Power Module with Low Thermal Impedance and Thermo-Mechanical Stress".

DISCLOSURES FILED

[1] K.D.T. Ngo, X. Cao, S. Sasaki, and G-Q. Lu, “Hourglass-Shaped Joint for Large Bonding Area to Improve Reliability”.

[2] K.D.T. Ngo, X. Cao, and S. Sasaki, “One-Step Reflow Process to Form Multiple Solder Layers with Desirable Shapes”.

[3] K.D.T. Ngo, X. Cao, and T. Suzuki, “Pulsewidth-Modulated Resonant Power Conversion”.