High-frequency Quasi-square-wave Flyback Regulator

Zhemin Zhang

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Khai D. T. Ngo, Chair
Jih-Sheng (Jason) Lai
Qiang Li
Dong Ha
Guo-Quan Lu

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Abstract

Motivated by the recent commercialization of gallium-nitride (GaN) switches, this paper examines the feasibility of switching the flyback converter at 5 MHz in order to improve the power density of this versatile isolated topology. Soft switching techniques have to be utilized to eliminate the switching loss to maintain high efficiency at multi-megahertz. A numerical methodology of parameters design is proposed based on the steady-state model of zero-voltage switching quasi-square-wave flyback converter to improve the traditional modeling. The magnetizing inductance is selected to guarantee zero-voltage switching for the entire input and load range with the trade-off design for conduction loss and turn-off loss.

A design methodology is introduced to select a minimum core volume for an inductor or coupled inductors experiencing appreciable core loss. The geometric constant $K_{gac} = MLT/(A_c^2 W_A)$ is shown to be a power function of the core volume V_e, where A_c is the effective core area, W_A is the area of the winding window, and MLT is the mean length per turn for commercial toroidal, ER, and PQ cores, permitting the total loss to be expressed as a direct function of the core volume. The inductor is designed to meet specific loss or thermal constraints. An iterative procedure is described in which two- or three-dimensional proximity effects are first neglected and then subsequently incorporated via finite-element simulation. Interleaved and non-

interleaved planar PCB winding structures were also evaluated to minimize leakage inductance, self-capacitance and winding loss. The analysis on the trade-off between magnetic size, frequency, loss and temperature indicated the potential for a higher density flyback converter.

A small-signal equivalent circuit of QSW converter is proposed to design the control loop and to understand the small-signal behavior. By adding a simple damping resistor on the traditional small-signal CCM model, the pole splitting phenomenon observed in QSW converter can be predicted. With the analytical expressions of the transfer functions of QSW converters, the impact of key parameters including magnetizing inductance, dead time, input voltage and output power on the small-signal behavior can be analyzed. The closed-loop bandwidth can be pushed much higher with this modified model, and the transient performance is significantly improved.

With the traditional fix dead-time control, a large amount of loss during dead time occurred, especially for the eGaN FETs with high reverse voltage drop. An adaptive dead time control scheme is implemented with simple combinational logic circuitries to adjust the turn on time of the power switches. A variable deadtime control is proposed to further improve the performance of adaptive dead-time control with simplified sensing circuit, and the extra conduction loss caused by propagation delay in adaptive dead-time control can be minimized at multi-megahertz frequency.

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General Audience Abstract

With the fast development of telecom, computer and network systems, high efficient and small volume power supplies are highly desired. A typical method for achieving high power density involves increasing the frequency and implement soft-switching techniques to minimize loss. Thanks to the recent commercialization of the advanced semiconductor gallium-nitride (GaN) switches, it is feasible to design high density power supplies and cost effective power system.

Several challenges including optimization of power converter, high frequency magnetics and implementation of control architecture have been addressed in this dissertation which helps to realize this compact power system. With the implementation of proposed circuit model and semi-numerical design procedures for magnetics, a 30W high-frequency isolated DC/DC converter with planar inductor is fabricated to verify the theoretical analysis, which also demonstrates much improved performances.

To my Parents

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Chapter 1 Introduction

This chapter presents the background, motivation, and overview of this dissertation. The existing research activities including high-frequency magnetic design methodologies, advantages and challenges of gallium nitride (GaN) devices, and dead-time control are reviewed. The structure of this dissertation is explained, and a brief summary of the main contributions is given.

1.1 Background and Motivation

Enterprise networks continue to expand, growing more versatile and complex. Devices once considered peripherals—wireless accesses points (WAPs), security network cameras, building automation and control systems, and voice-over-IP (VoIP) phones—are now important network assets. The cabling infrastructure needs to support the growing devices, and the option to power them over structured cabling becomes more attractive. [1].

Figure 1.1. Power over Ethernet (PoE) system.

Power over Ethernet (PoE) (see in Figure 1.1) has emerged as a key powering strategy over the past decade, allowing network managers, installers, and integrators to use structured cabling to provide both power and data to many of their network devices. Power over Ethernet was first adopted in 2003 with the original 802.3af standard, providing up to 15 W of DC power with a minimum availability of 12.95 W to the powered device. The ability to power IP devices, primarily VoIP phones at that time, proved to be very cost effective for customers. As years went by and advanced VoIP phones began to require more power, the IEEE ratified 802.3at in 2009 allows up to 30 W of DC power with 25.5 W available to the powered device. This accommodated VoIP phones with larger full-color displays, as well as some of the early IP security cameras and other IP devices. PoE remains very cost effective, and therefore becomes a very popular technology. The need for more power continues to grow, and the new standard, IEEE P802.3bt, is designed to deliver up to 74.55 watts of power to PoE enabled devices, assuming a 100m channel. The evolution of remote powering is illustrated in Figure 1.2 [1].

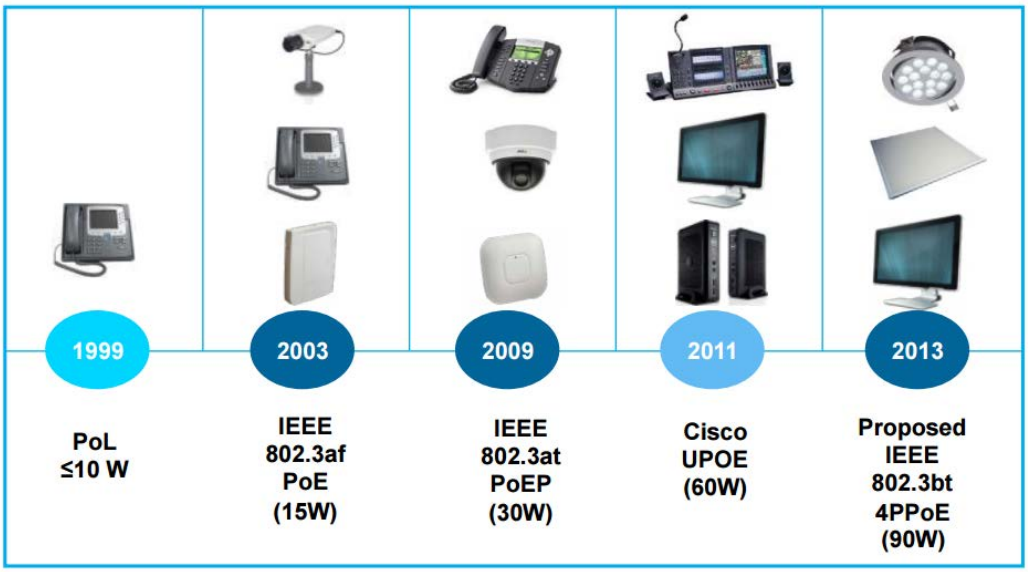


Figure 1.2. The evolution of remote powering technology.

The global power over Ethernet solutions market is expected to grow at a CAGR of 12.56% between 2016 and 2022, increasing from 451.1 million USD to 1,048.3 million USD. Increasing demand for PoE-based products, especially in the commercial vertical, is one of the major factors fueling the growth of this market. The growing IoT industry is also expected to generate demand for networking devices. The key restraining factor for the growth of this market is the limitation on the amount of power delivered to the end devices by the use of PoE-based power sourcing equipment.

1.2 Application of GaN FETs at High Frequency

It is highly desired to reduce both power consumption and volume as more devices are added and more power is required. A bus converter transfers the intermediate bus voltage into the voltages required by the different loads in this system. The two most important desiderata for a PoE topology are low cost and high efficiency. Low cost, which is a must for any product of mass usage, implies a simple topology [3]. Thanks to the simplicity of power stage, flyback-type converters are widely adopted as cost-effective isolated power converters for low-power applications [4]-[7]. In the earliest days of PoE power supplies, their compliance to the specification was effected by the discrete circuitry added at the frontend. The obvious shortcoming of this approach is that of complexity and component count coupled with greater demands on the design skills of the power supply designer. A refinement of this approach which some IC vendors have followed, is to build just the powered device interface (PDI) to ensure its compliance with the specification and follow this with a power supply designed around a separate PWM controller. This is an improvement to the previous approach, but still requires two complex ICs for a complete solution. Another better approach is to integrate the PDI and PWM

controller into a single IC and build the entire power supply solution around it. The commercial brick flyback converter for low power application is surveyed [8]-[15] and shown in Figure 1.3.

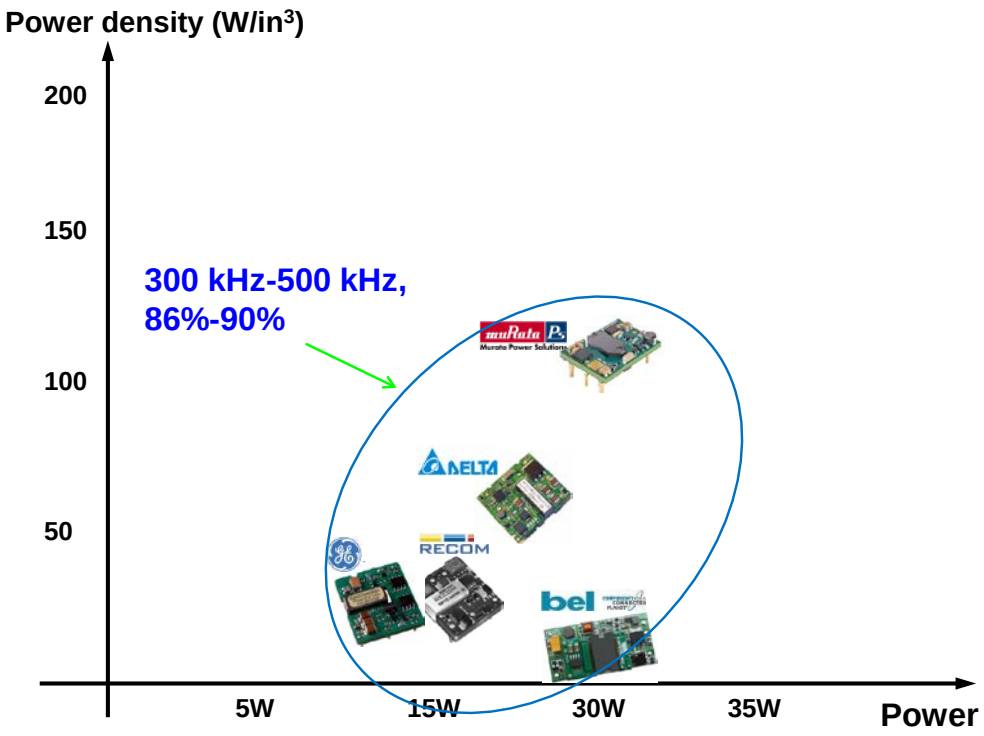


Figure 1.3. The state-of-the-art commercial flyback converter at low power application based on the datasheet from different manufactures [10]-[15].

The discrete solution operates at the frequency ranging from 300 kHz to 500 kHz, and offers the power density in the 30-100W/in^3 range with the efficiency of 86% -90%. While flyback's coupled inductors provide a convenient means for isolation, their stored energy results in the converter's low power density, and their leakage inductances for the high voltage stress on the semiconductor switches. Thus, attempting to reduce the size of the inductors by increasing the switching frequency might have limited success unless the switching frequency is increased significantly, and unless the leakage inductance could be scaled down, at least proportionally to the rate at which commutation speed increases.

It is difficult to further push the switching frequency of POL converter to increase the power density with the state-of-art silicon-based power transistor. The emerging gallium nitride (GaN) power device technology promises to have better performance in the figure of merits than the existing silicon devices as shown in Figure 1.4. The theoretical limit of GaN is at least three orders of magnitude lower than that of Si.

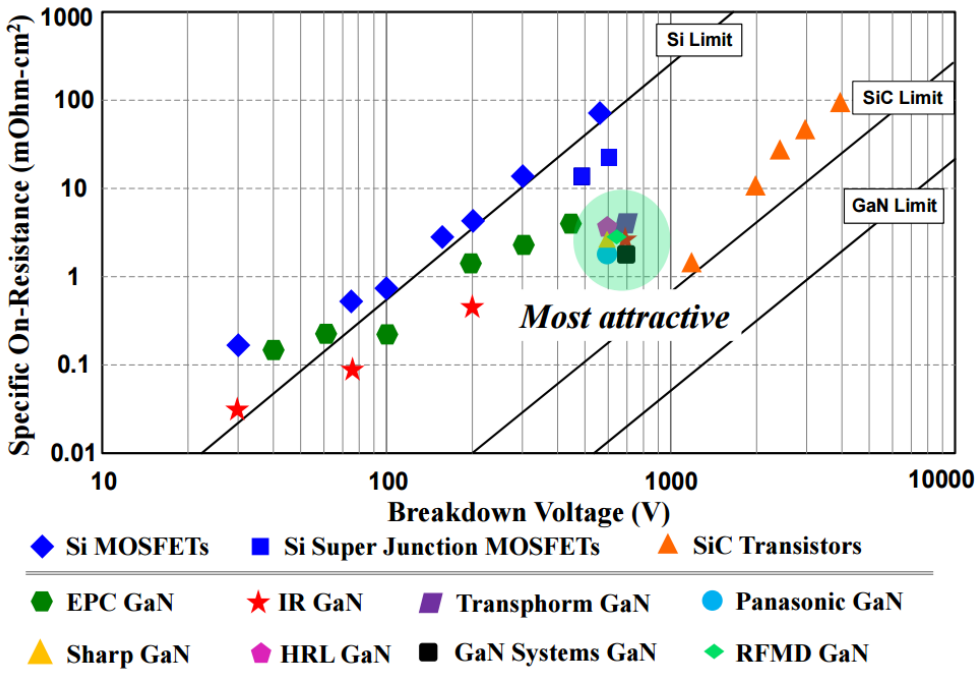


Figure 1.4. Specific on-resistance vs breakdown voltage for Si, SiC, and GaN [16]-[18].

Nonetheless, the introduction of GaN transistors on the market in the last few years [19]-[26] has renewed the interest in investigating the correlation between multi-megahertz switching frequency and the power density of flyback topology. The baseline for the research is the class of converters for PoE application with the specification of 36 -72 V down to 12 V at 0 - 30 W. Soft-switching techniques have to be used to mitigate switching loss at multi-megahertz range. The multi-resonant converter [27]-[29], Class E [30]-[32] and Class Φ [33]-[34] converter can operate at very high switching frequency, but the voltage stress and current stress are normally 3-

5 times larger than the input voltage, which is shown in Table 1.1. These converters are variable frequency which is also not preferred. Quasi-square-wave converter with synchronous rectifier [4], [35], [10] is an option. In addition to zero-voltage switching, the output can be regulated at constant switching frequency while maintaining low voltage stress and relatively low current stress on the switches.

Table 1.1. Specification and performance of high-frequency resonant converters [27]-[34]

	MRC	Class E	Class Φ
Topology	Forward	Class E_M	Class Φ_2
Output power	50 W	13.9 W	200 W
Frequency	3 MHz	3.5 MHz	30 MHz
Device	MOSFET	MOSFET	RF MOSFET
Power density	50 W/in^3	N/A	N/A
Efficiency	83%	94.8%	84%
Application	SMPS	Power amplifier	RF amplifier

1.3 Overview of Conventional Design Method for Magnetics

Magnetic components usually occupy a significant percent of the volume within a power converter. A typical method for reducing the volume involves increasing the switching frequency and operating the converter in critical conduction mode or resonant mode to minimize switching loss and noise. This method also significantly increases the core loss and ac winding loss, rendering standard design methods less effective. Core loss is difficult to model accurately owing to the effects of shape, bias, and temperature. Proximity fields are often two- or three-dimensional in a practical winding window of a high-density inductor, whereas analytical models of ac winding loss rely on one- or quasi-two-dimensional assumptions [37], [38]. The finite-

element simulation has proven to be an effective tool in dealing with complex magnetic loss effects [39], [40].

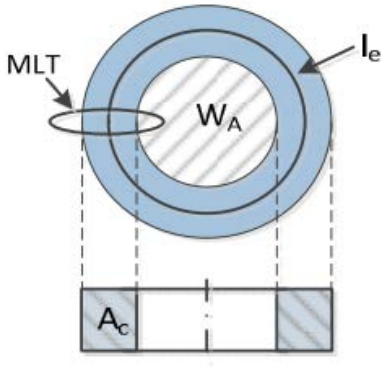


Figure 1.5. Definition of W_A, A_c, l_e and MLT for magnetic core used in the analysis.

Conventional inductor design methodology is based on area product (A_p) [41]–[44]. The analytic formulation of A_p method is

$$A_p = A_c W_A = \frac{L_m I_{Lmmax} I_{total}}{K_u B_{max} J} \tag{1.1}$$

where the definition of window area W_A, effective cross-sectional area of magnetic circuit A_c, effective length l_e, and mean length of a turn MLT for magnetic core used in the analysis is shown in Figure 1.5. Ku is the fill factor of the window area, I_{Lmmax} is the peak magnetizing current, B_{max} is the peak flux density, and J is the current density that equals to rms current I_{total} divided by cross-sectional area of the windings [45]. Another method is geometric constant (K_g) [46], [9] and its analytic formulation is found from [9]

$$K_g = \frac{A_c^2 W_A}{MLT} = \frac{\rho L_m^2 I_{Lmmax}^2 I_{total}^2}{K_u B_{max}^2 P_t} \tag{1.2}$$

where total loss P_t is estimated and given in advance. The appropriate core size can be selected from the A_p or K_g chart (see in Appendix B) using the equations shown above to calculate the area product A_p or geometric constant K_g.

The design variables, such as the current density J and maximum flux density B_{max}, are usually established arbitrarily in advance; consequently, many iterations may be required to reach a feasible design. De Nardo *et al.* [49] recently demonstrated an approach based on the geometric form factors (GFFs) of magnetic cores, the shape of which strongly influences the design problem, and revealed the limitations of the previous geometric constant method. However, the high-frequency eddy effects of the winding loss are not considered in their design approach [49]. Amoiralis *et al.* [50] Shuai and Biela [51] introduced iterative methods to derive the optimal transformer in terms of the loss, size, and thermal constraints. These methods are complex and usually cover specific ranges of several design variables until a feasible design is obtained [48].

The accurate modeling of core loss and copper loss are usually the big challenges for all the conventional design methods described above, especially when the switching frequency is multi-megahertz. The Steinmetz equation has been widely used to predict the core loss under sinusoidal excitation. The modified Steinmetz equation (MSE) [53] and improved generalized Steinmetz equation (iGSE) [54] have been proposed for non-sinusoidal excitation. The rectangular extension of the Steinmetz equation (RESE) was proposed by Mu and Lee [6] as an alternative to improve the accuracy on the basis of measurements.

The effect of high-frequency operation on windings and cores has been analyzed in many papers [56]–[66]. An increase in the winding ac resistance due to skin and proximity effects was

discussed in Dowell's study [37], which assumed the presence of a one-dimensional field on the winding surfaces. Wang *et al.* [38] developed a quasi-two-dimensional field solution for a micro-inductor in which the one-dimensional assumption was found to be inapplicable even in the absence of air gaps. Roshen [56], [57] derived formulas for the winding loss due to the fringing flux near the air gap for core structures in which the core reluctance is much smaller than the gap reluctance. The finite element method would be more advantageous for quantifying the winding loss when the flux field is irregular around the conductors. To predict the temperature rise of magnetic components, several thermal models are discussed in [67]–[68]. The usefulness of these models depends on the accurate representation of heat-transfer coefficient, which is nonlinear and depends on the geometry and cooling conditions.

Since switching frequency can be pushed to multi-megahertz or higher with the fast development of GaN device, passive components such as magnetics become the bottom neck to further shrink the total size. It is highly required to develop a systematic design procedure for high-frequency magnetics to meet the following conditions: 1) the magnetic core does not saturate; 2) the total core and copper losses do not exceed the allowed loss budget; 3) the core temperature is limited to avoid thermal runaway.

1.4 Overview of Dead-time Control

GaN devices have the bi-directional current flow capability in nature due to their physical structure. E-mode GaN can conduct in the reverse direction when the drain voltage is lower than the gate by at least V_{TH}, as shown in Figure 1.6. The voltage drop V_{SD} is determined by the reverse current I_{SD}, transconduction g_m, threshold voltage V_{TH}, and applied gate-source voltage V_{GS}, as given by (1.2). It is obvious that V_{SD} increases with I_{SD} and the first term is considerable

even at low current due to the non-linearity of gm. It should be pointed out that V_{SD} increases significantly if $V_{GS(off)}$ has initial negative bias in off state [16], [18].

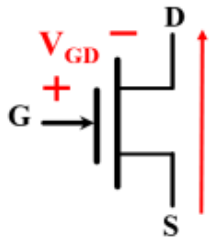
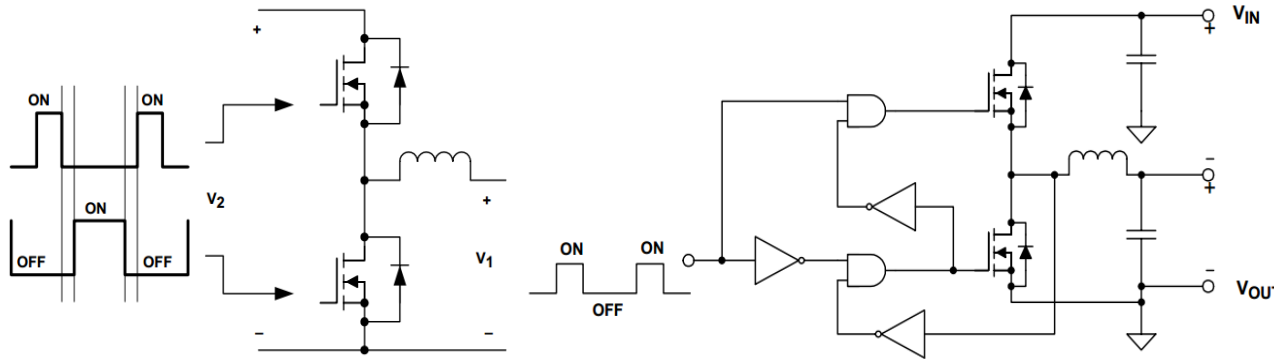


Figure 1.6. Reverse conduction of e-mode GaN devices.

$$V_{SD} = \frac{I_{SD}}{g_m} + V_{TH} - V_{GS(off)} \tag{1.3}$$

The reverse voltage drop of GaN device is much higher than Si MOSFET and may lead a higher conduction loss without proper deadtime. Optimizing dead-time can partially solve this problem [26], [81]-[83], but only at relatively low frequency. No commercial control chip for this application can operate above 1 MHz. The propagation delay of the gate driver and other control logic circuit can cause a lot of issues. The popular dead-time control techniques mainly include fixed dead-time control and adaptive dead-time control [84].

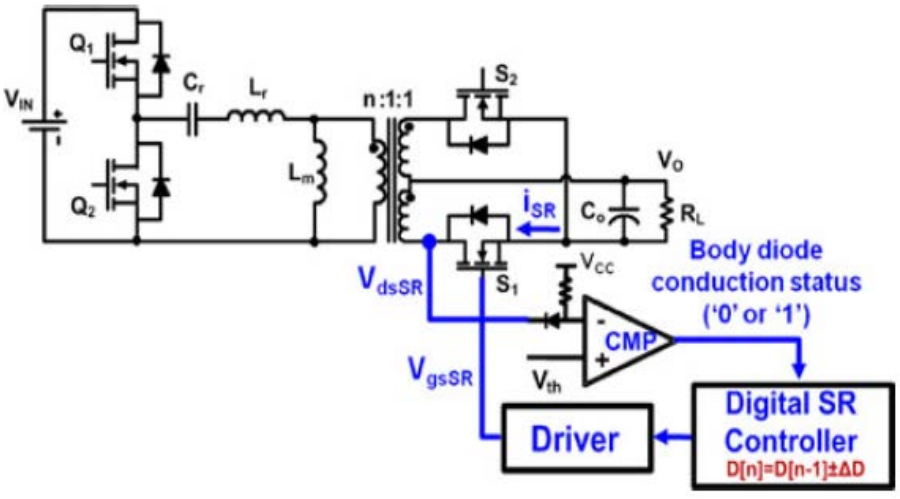


(a) (b)

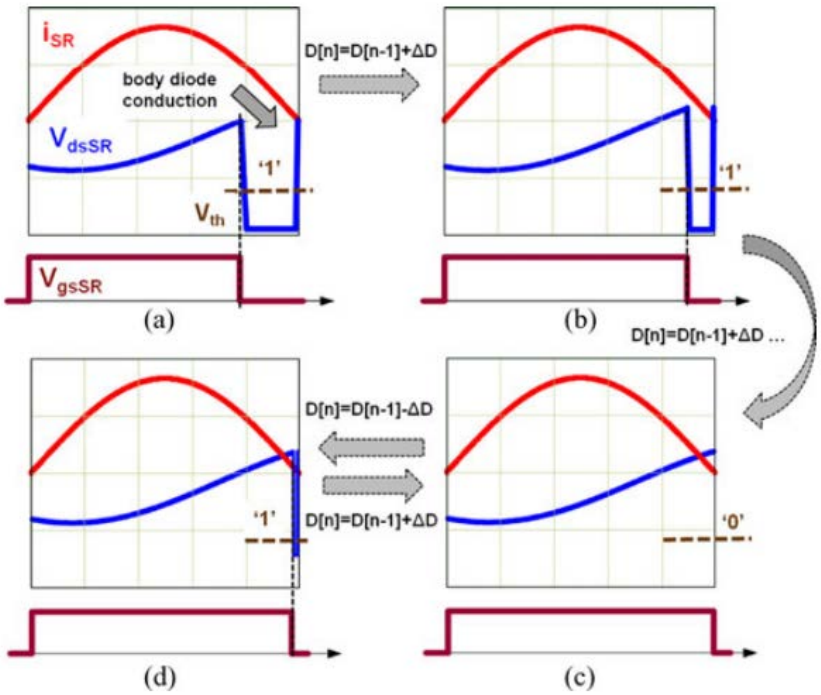
Figure 1.7. (a) Fix dead-time and (b) Adaptive dead-time control.

With fixed dead-time, a constant uncontrolled dead-time is added to the gate signal for the synchronous MOSFET. A simple RC network is the usual implementation to set the proper deadtime. The fixed dead-time must be long enough to avoid over shoot in any conditions, regardless of changes in temperature, load, and the type of MOSFET device. To avoid any chance of shoot through, the dead-time is usually much longer than needed in most situations, resulting in excessive body diode conduction.

Adaptive dead-time control is able to adjust the dead-time according to the current conditions in the circuit. An example of an adaptive dead-time control circuit is shown in Figure 1.7(b). Due to the inevitable package inductance, the sensed terminal drain to source voltage of the SR is actually the sum of the MOSFET's ON-status resistive voltage drop and the package inductive voltage drop, which deviates greatly from the purely resistive voltage drop of the MOSFET as the switching frequency increases. The feedback loop acts to detect body diode conduction. As a result, this method can only decrease body diode conduction rather than eliminate it.



(a)



(b)

Figure 1.8. (a) Control blocks of the proposed universal adaptive SR driving scheme and (b) SR turn-OFF tuning process to eliminate the body diode conduction [85].

The SR control in LLC converter proposed in [85] is another application of adaptive deadtime control. The intelligent digital control is implemented to tune the SR gate driving signals more precisely as shown in Figure 1.8(a) and the main waveforms are reported in Figure 1.8(b).

Another type of dead-time control is predictive dead-time control, which uses the information of the previous switching cycle to determine the dead-time needed in the current cycle. Depending on the numbers of cycles needed for the buck converter to reach steady state, predictive dead-time control can be further categorized into unit bit delay adjustment and one step adjustment. A simplified predictive dead-time control using analog circuitry can be a good

solution for megahertz switching frequency. The large propagation delay of control circuits can be overcome, since the off time of SW and on time of SR can be decoupled.

1.5 Dissertation Outline

Following this introductory chapter, Chapter 2 demonstrates the steady-state model of quasi-square-wave flyback converter. A numerical methodology of parameters design is proposed based on the steady-state model of zero-voltage switching quasi-square-wave flyback converter to improve the traditional modeling. The magnetizing inductance is selected to guarantee zero-voltage switching for the entire input and load range. Meanwhile, the ripple of magnetizing current should be relatively small to reduce the conduction loss of winding and switches.

Chapter 3 introduces the methodology named Kgac for the coupled inductors in the flyback topology with large ac flux. A designer can select magnetic flux density based on thermal constraint with this method. An empirical relationship among effective area (Ac), mean length per turn (MLT), window area (WA), and volume (Ve) is suggested for the derivation of the core volume that minimizes the total loss. An optimal core volume can be calculated with the given specifications when the ac winding loss is taken into consideration in the design procedures. Interleaved and non-interleaved planar PCB winding structures are also evaluated to minimize leakage inductance, self-capacitance, and winding loss using finite element simulation tool Ansys/Maxwell.

Chapter 4 demonstrates a modified small-signal model of QSW converter to explain the double-pole splitting phenomenon and to analytically quantify the damping effect. The impacts of deadtime, input voltage, and output power on control-to-output transfer function are also investigated in detail. The closed-loop bandwidth can be pushed much higher with this modified

model, and the transient performance is significantly improved compared to the state-of-the-art commercial product.

Chapter 5 describes the prototypes of the power stage and control system for QSW converter to verify the analysis of QSW flyback converter and evaluate its efficiency. In order to reduce the large amount of loss during dead time from traditional fixed dead-time control, especially for the eGaN FETs with high reverse voltage drop, an adaptive dead time control scheme with simple combinational logic circuitries is implemented to adjust the turn on time of the power switches. A variable deadtime control is further proposed and thoroughly illustrated to overcome several limitations of adaptive dead-time control at multi-megahertz frequency.

Chapter 6 summarizes the main conclusions of this dissertation and proposes potential future work.

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Chapter 2 Steady-State Circuit Model of Quasi-Square-Wave Flyback Converter

A typical method for reducing the size of the power converter involves increasing switching frequency and operating the converter in critical conduction mode or resonant mode to minimize switching loss and noise. Quasi-square-wave (QSW) mode is the most simple and effective way to achieve zero-voltage-switching and is widely used in medium-low application.

Within multi-megahertz switching frequency range, the traditional function between duty cycles to conversion ratio does not hold any more. The resonant period between inductance and parasitic capacitances cannot be negligible. A steady-state model of zero-voltage-switching (ZVS) quasi-square-wave flyback converter is used to design parameters and derive the duty cycle and dead time including the resonant intervals. A charge conservation method including capacitor nonlinearity is applied, and a numerical methodology of parameters design for the flyback converter with wide input and load range is proposed to improve the traditional model. The magnetizing inductance is selected to guarantee zero-voltage switching for the entire input and load range. The timing of the converter can also be derived from the charge based model.

2.1 Introduction

The industry's requirement for highly efficient, high density power supplies has made it necessary for designers to adopt resonant techniques that enable both high frequency as well as high efficiency operation. Flyback converters are widely used as cost-effective isolated power converters for low-power applications due to the simplicity of power stage [1]-[8]. Synchronous rectifier (SR) i.e., a low-on-resistance switch can also be used to further reduce the conduction

loss of diode on the secondary side. With proper control of gate driving signal, the operation of the circuit shown in Figure 2.1 is identical to that of a conventional diode rectifier. Namely, during the time switch SW is turned on, energy is stored in the transformer magnetizing inductance and transferred to the output after SW is turned off.

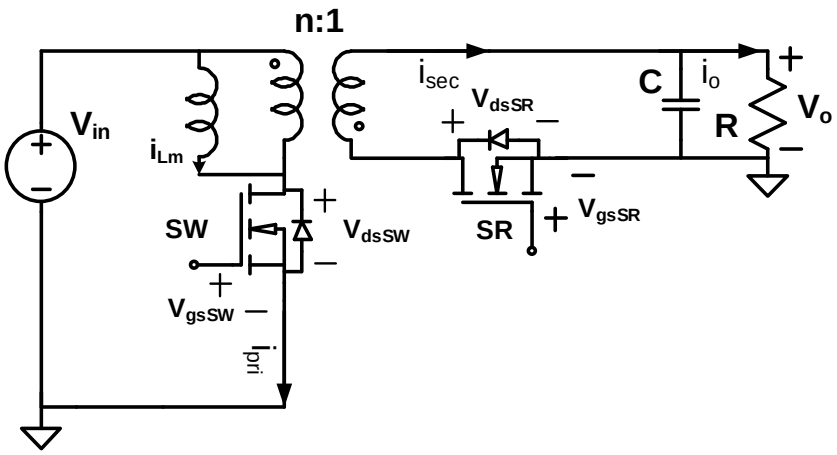


Figure 2.1. Flyback converter with synchronous rectifier on the secondary side.

The conduction periods of the primary switch SW and the secondary-side switch SR must not overlap for the proper operation of converter. To avoid the simultaneous conduction of SW and SR, a delay between the turn-off instant of the switch SW and the turn-on instant of SR as well as between the turn-off instant of SR and the turn-on instant of SW must be introduced in the gate-drive waveforms of the switches. In order to achieve soft switching, especially for multi-megahertz range, the converter can be operated at critical current (CRM) mode or quasi-square wave (QSW) mode either with a variable or constant switching frequency pulse-width-modulation (PWM) control during the dead time interval.

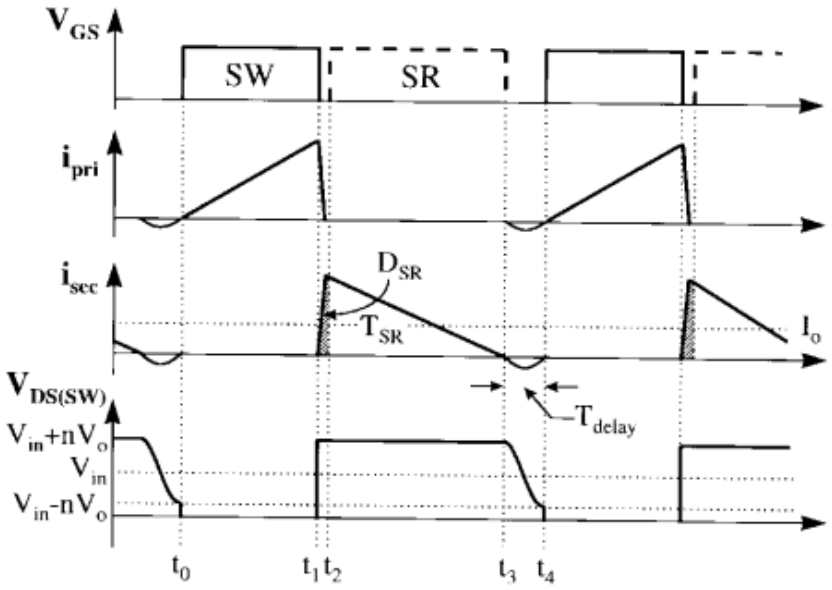


Figure 2.2. Key waveforms of variable frequency CRM flyback converter with SR.

The key waveforms of the flyback converter with the SR operating in variable-frequency CRM are given in Figure 2.2. The amplitude of the oscillation after the turn off of SR is larger than the input voltage, i.e., if

$$V_{in} < nV_o \tag{2.1}$$

Primary-switch voltage $V_{DS(SW)}$ will fall to zero before the switch is turned on. ZVS condition in (2.1) may be achieved in certain designs for low input-voltages, but not at higher input voltages as shown in Figure 2.2. The key waveforms of the flyback converter with the SR operating in QSW are shown in Figure 2.3.

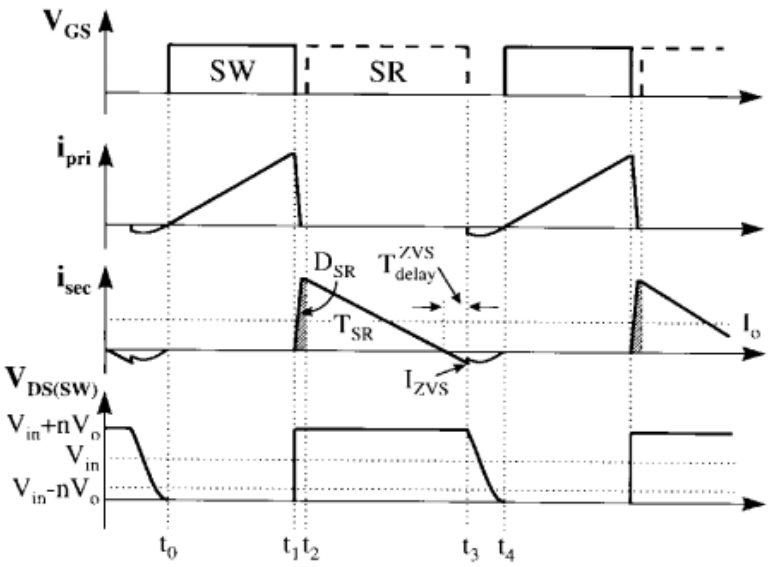


Figure 2.3. Key waveforms of constant frequency QSW flyback converter.

The parasitic capacitances in flyback converter are shown in Figure 2.4. The output capacitance C_{oss_SW} and C_{oss_SR} of SW and SR are assumed to be linear. The self-winding capacitance of coupled inductors C_p is lumped on the primary side. The equivalent capacitance C_{eq} which resonates with parasitic inductance can be expressed as

$$C_{eq} = C_{oss\_SW} + \frac{C_{oss\_SR}}{n^2} + C_p \tag{2.2}$$

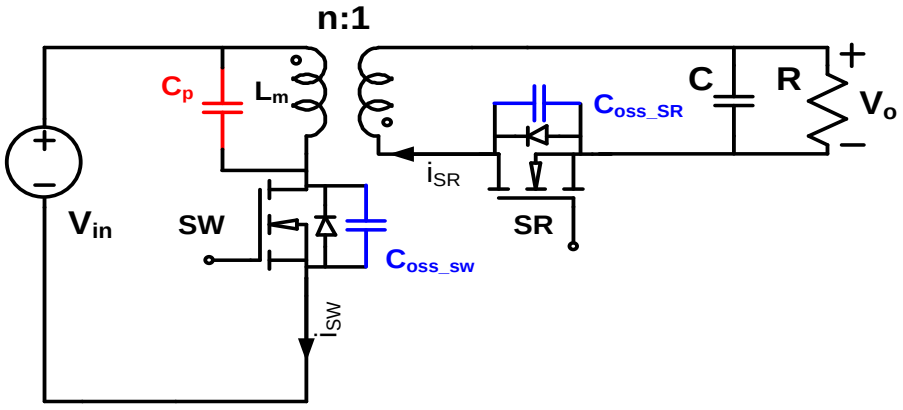


Figure 2.4. Parasitic capacitances of switches and inductors in flyback converter.

The complete ZVS of the primary switch in the flyback converter with SR can be achieved in the entire input-voltage range if the turn-off instant of SR after the secondary current zero crossing is delayed enough to allow a negative secondary current to build up. To achieve ZVS in the entire input-voltage range, the energy stored in magnetizing inductance by the negative secondary current i_{ZVS} must be large enough to discharge primary switch capacitance from voltage $V_{in}+nV_o$ down to zero, i.e.,

$$\frac{1}{2}L_m\frac{{i_{zvs}}^2}{n^2}+\frac{1}{2}C_{eq}n^2{V_o}^2\geq\frac{1}{2}C_{eq}{V_{in(max)}}^2 \tag{2.3}$$

Rearranging the equation (2.3), the negative secondary current should be

$$i_{zvs}\geq n\sqrt{\frac{C_{eq}}{L_m}({V_{in(max)}}^2-n^2{V_o}^2)} \tag{2.4}$$

Quasi-square-wave soft-switching technique is a solution to eliminate the limitations of partial ZVS in CRM operation. Compared to the wide switching frequency range of CRM operation, the switching frequency of QSW mode is constant, which may simplify the design of EMI filter. In the meantime, the loss and volume of magnetics will be optimized at one fixed frequency. The ripple current becomes larger at light load condition which may deteriorate the converter efficiency. However, the large circulation energy can be mitigated by switching the converter to burst mode or pulse skip mode at light load.

2.2 Traditional Steady-State Model of Quasi-Square-Wave Flyback Converter

2.2.1 Development of linear equivalent capacitances

In order to develop equivalent linear capacitors, analysis must focus on the parameters of interest on which to base the equivalence. Because of their fundamental nonlinearity, a constant-valued, linear capacitance will only be able to correctly model a single parameter for a given voltage transition in general. Because both are conservative, only the defining curve of the nonlinear capacitor voltage dependence is needed to obtain the storage at a given voltage. Linear equivalent capacitors which store the same amount of charge or energy at a given voltage can be developed for the nonlinear capacitor, which are independent of application circuit.

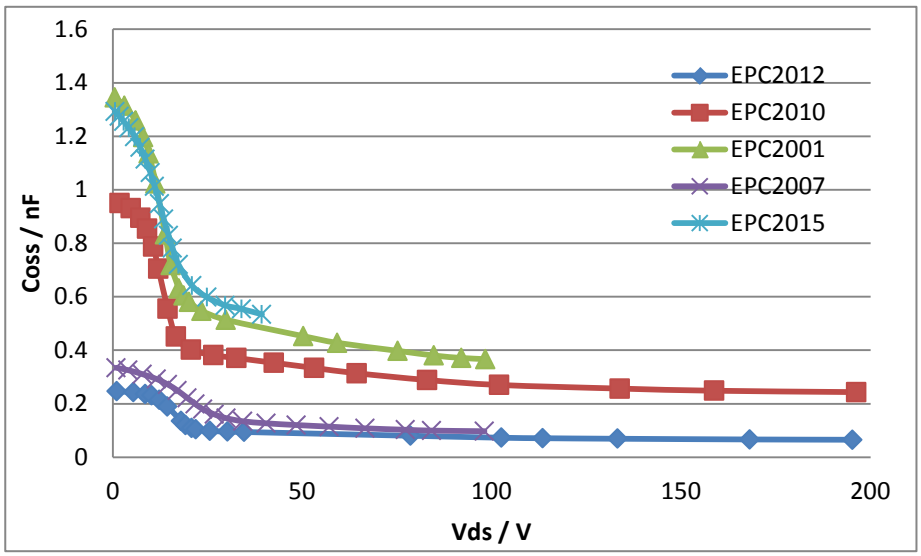


Figure 2.5. Output capacitance of GaN devices with respect to V_{ds}.

The output capacitance versus device voltage V_{ds} of different eGaN FETs can be found from the datasheet shown in Figure 2.5 [9]. The charge can then be used to find a linear capacitance

value that contains the same amount of charge at a certain V_{ds} by considering the charge stored in the equivalent capacitor $C_{eq,Q}$, which is linear, constant-valued

$$Q_{oss}(V_{ds}) = \int_0^{V_{ds}} C_{oss} dv. \tag{2.5}$$

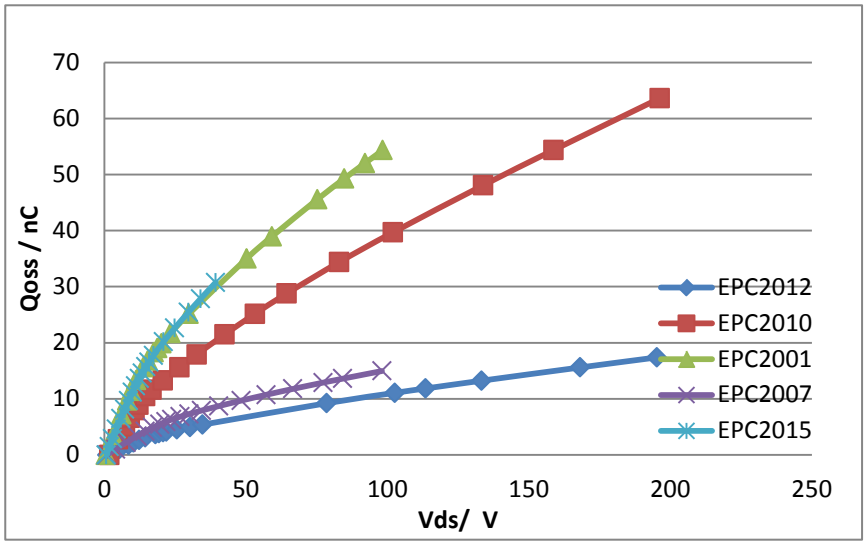


Figure 2.6. Output charges of GaN devices with respect to V_{ds}.

The curves of charge versus V_{ds} are shown in Figure 2.6, and the linear capacitance which is charge-equivalent is

$$C_{eq,Q}(V_{ds}) = \frac{1}{V_{ds}} \int_0^{V_{ds}} C_{oss}(V_{ds}) dv. \tag{2.6}$$

A similar process may be used to find the total energy. The curves of energy voltage dependences show in Figure 2.7 are obtained by integrating the product of C_{oss} and V_{ds} over the voltage range.

$$E_{oss}(V_{ds}) = \int_0^{V_{ds}} C_{oss} \cdot V_{ds} dv, \tag{2.7}$$

and energy-equivalent linear capacitance is equal to

$$C_{eq,E}(V_{ds}) = \frac{2}{V_{ds}^2}\int_0^{V_{ds}} C_{oss} \cdot V_{ds} dv. \tag{2.8}$$

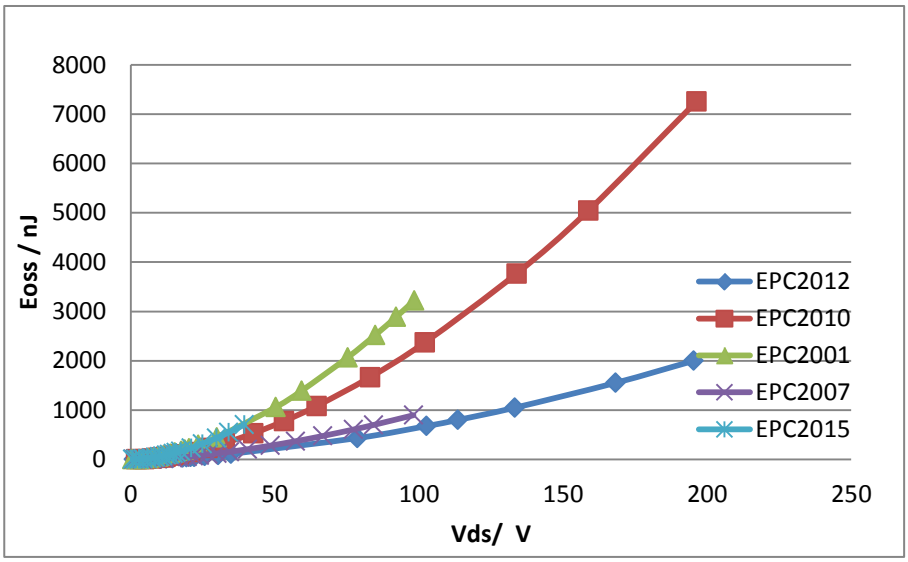
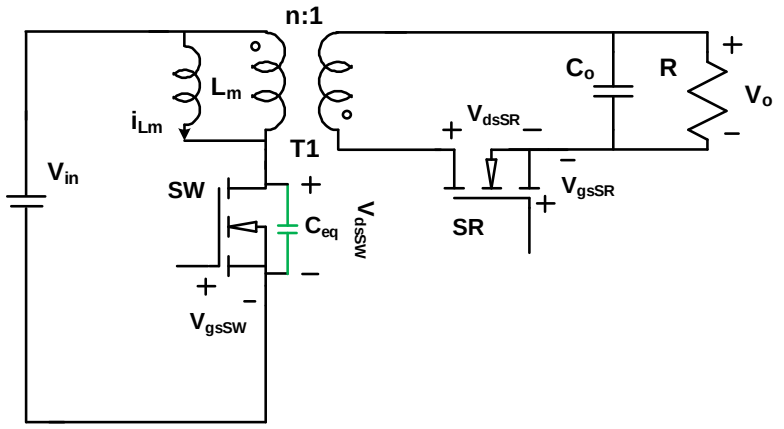


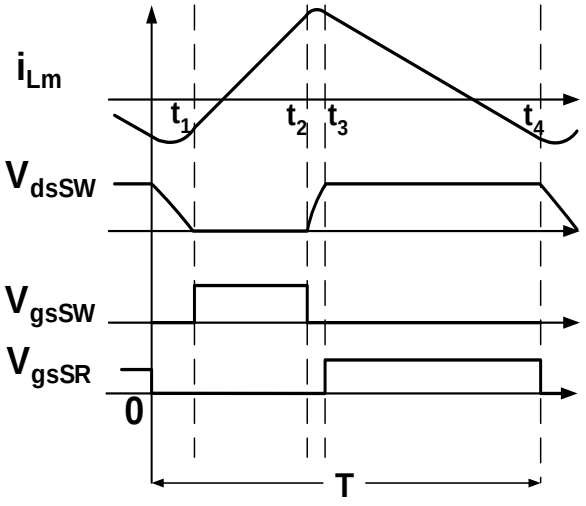
Figure 2.7. Output capacitive energy of GaN devices with respect to V_{ds}.

2.2.2 Steady state model of ZVS QSW flyback converter

An equivalent linear capacitor is normally used to represent the output capacitor of the power transistor in the traditional model of QSW converter [10]. The Zero-voltage-switching quasi-square-wave flyback converter with the equivalent capacitor and its typical steady-state waveforms are shown in Figure 2.8. The C_{eq} is the sum of all the parasitic capacitances in the converter including output capacitance of transistor and the self-winding capacitance of coupled inductors whose value is given in (2.2).



(a)



(b)

Figure 2.8. (a) Flyback converter with equivalent capacitor in parallel and (b) Typical steady-state waveforms for ZVS QSW flyback converter.

The operation of QSW flyback converter is divided into four stages during one switching period including two resonance intervals. Unlike the traditional flyback converter, the transition intervals ([0, t_1] and [t_2, t_3]) which are the resonance between coupled inductors and output capacitors of switches cannot be negligible at multi-megahertz or even at higher frequency. The equivalent circuits for each stage are shown in Figure 2.9 to illustrate the steady-state operation of

QSW flyback converter in one switching cycle. The V_{in} is the input voltage, V_o is the output voltage, and n is the turns ratio of coupled inductors. The magnetizing current i_{Lm} and the voltage V_{dsSW} across equivalent capacitance C_{eq} are the state variables.

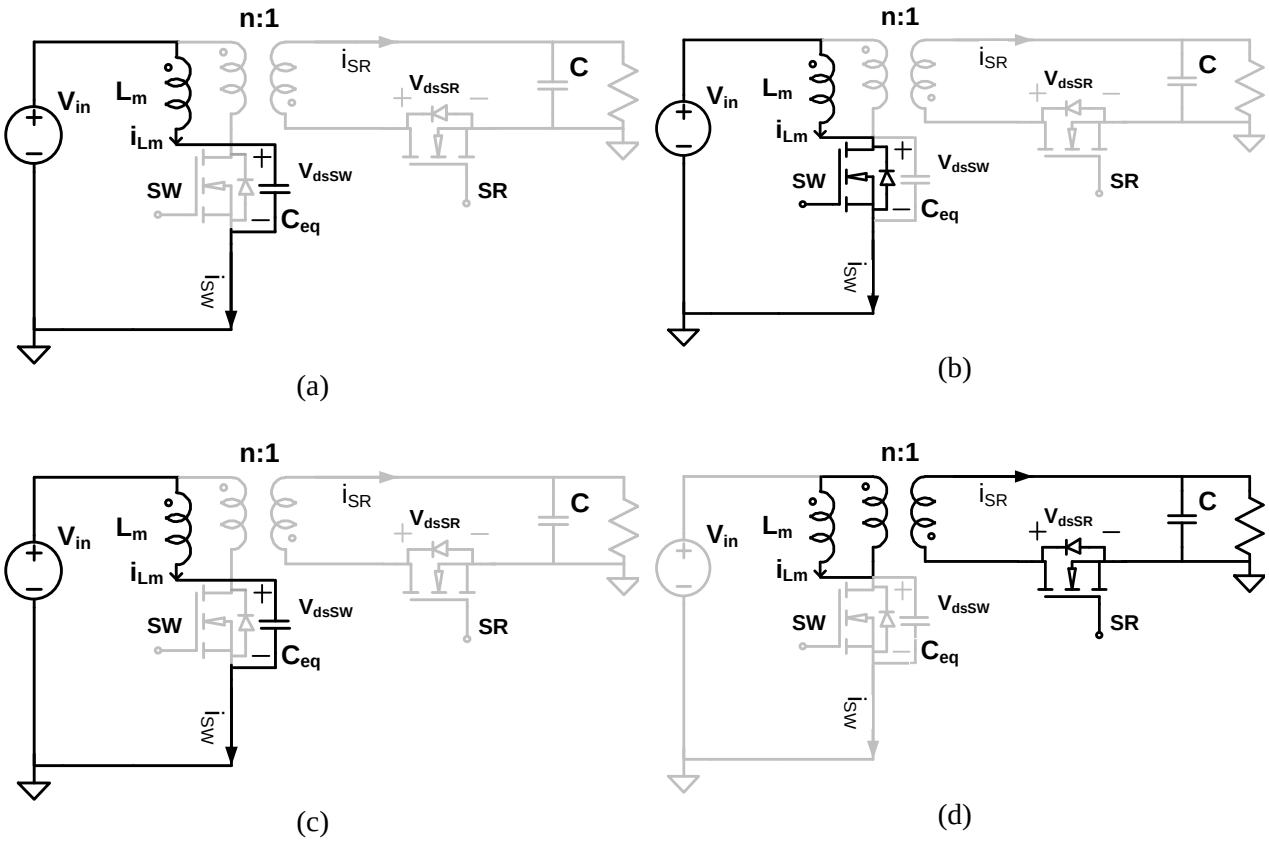


Figure 2.9. Equivalent circuits of QSW flyback converter for each stage: (a) stage 1 [0, t_1], (b) stage 2 [t_1, t_2], (c) stage 3 [t_2, t_3], (d) stage 4 [t_3, t_4].

1) Stage 1 [0, t_1]

At t = 0, the switch SW is off, and the synchronous rectifier is turned off. With the negative initial current $i_{Lm}(0)$, the magnetizing inductance L_m starts to resonate with the parasitic capacitance C_{eq} to discharge the $V_{dsSW}(0)$ from $V_{in}+nV_o$ to zero. ZVS is achieved for the switch SW. The voltage V_{dsSW} across the input switch and the inductor current are expressed as

$$V_{dsSW}(t) = nV_o \cos \omega t + Zi_{Lm}(0) \sin \omega t + V_{in} \tag{2.9}$$

$$i_{Lm}(t) = -\frac{nV_o}{Z} \sin \omega t + i_{Lm}(0) \cos \omega t \tag{2.10}$$

where $\omega = 1/\sqrt{L_m C_{eq}}$ and $Z = \sqrt{L_m / C_{eq}}$. This stage ends at t = t_1 when V_{dsSW} reaches zero, and the inductor current is $i_{Lm}(t_1)$.

2) Stage 2 [t_1, t_2]

Synchronous rectifier is off, and SW is turned on softly during this stage. The inductor current is charged linearly from $i_{Lm}(t_1)$ and is given by

$$i_{Lm}(t) = \frac{V_{in}}{Z} \omega (t - t_1) + i_{Lm}(t_1) \tag{2.11}$$

The energy is stored in the magnetizing inductance from the input. This stage ends at t = t_2 when the switch SW is turned off, and the inductor current becomes $i_{Lm}(t_2)$.

3) Stage 3 [t_2, t_3]

Synchronous rectifier is still off, and the switch SW is turned off at t = t_2. It is another resonant commutation stage similar to the first interval. The junction capacitance of SR is discharged by the resonant inductor current to achieve soft switching for SR. This commutation interval is much shorter because the turn-off current here is several times larger those in the first stage. The voltage V_{dsSW} and the inductor current are given by

$$V_{dsSW}(t) = -V_{in} \cos \omega (t - t_2) + Zi_{Lm}(t_2) \sin \omega (t - t_2) + V_{in} \tag{2.12}$$

$$i_{Lm}(t) = \frac{V_{in}}{Z} \sin \omega (t - t_2) + i_{Lm}(t_2) \cos \omega (t - t_2) \tag{2.13}$$

This stage ends at $t = t_3$ when V_{dsSW} reaches $V_{in}+nV_o$. SR is ready to be softly turned on, and the inductor current becomes $i_{Lm}(t_3)$.

4) Stage 4 [t_3, t_4]

The switch SW is off, and SR is on. The energy stored in the inductor is transferred to the output. Negative i_{SR} at the end of the stage makes the input switch turn on softly. The inductor current is discharged linearly from $i_{Lm}(t_3)$ and is given by

$$i_{Lm}(t) = -\frac{nV_o}{Z}\omega(t-t_3) + i_{Lm}(t_3) \tag{2.14}$$

This stage ends at $t = t_4$ when SR is turned off, and the inductor current is $i_{Lm}(t_4)$ which is equal to $i_{Lm}(0)$. To sum up, the steady state model of QSW flyback converter with an equivalent capacitor is listed in Table 2.1.

Table 2.1. Steady-state model of QSW flyback converter

$V_{dsSW}(t) = \begin{cases} nV_o \cos\omega t + Zi_{Lm}(0)\sin\omega t + V_{in} \\ 0 \\ -V_{in}\cos\omega(t-t_2) + Zi_{Lm}(t_2)\sin\omega(t-t_2) + V_{in} \\ V_{in} + nV_o \end{cases}$	$\begin{array}{l} 0 < t \le t_1 \\ t_1 < t \le t_2 \\ t_2 < t \le t_3 \\ t_3 < t \le t_4 \end{array}$
$i_{Lm}(t) = \begin{cases} -\frac{nV_o}{Z}\sin\omega t + i_{Lm}(0)\cos\omega t \\ \frac{V_{in}}{Z}\omega(t-t_1) + i_{Lm}(t_1) \\ \frac{V_{in}}{Z}\sin\omega(t-t_2) + i_{Lm}(t_2)\cos\omega(t-t_2) \\ -\frac{nV_o}{Z}\omega(t-t_3) + i_{Lm}(t_3) \end{cases}$	$\begin{array}{l} 0 < t \le t_1 \\ t_1 < t \le t_2 \\ t_2 < t \le t_3 \\ t_3 < t \le t_4 \end{array}$

2.2.3 State plane diagram of ZVS QSW flyback converter

The timing of the converter can be extracted intuitively in the state plane diagram with regard to the boundary condition of zero voltage switching [10]. All the variables of converter are normalized and displayed in Table 2.2. Voltages are normalized to input voltage V_{in}, while currents are normalized to V_{in}/Z, where $Z = \sqrt{L_m / C_{eq}}$. The time normalized to $1/\omega$ becomes angle variable $\theta = \omega t$. The normalized steady-state model of QSW flyback converter is summarized in Table 2.3

Table 2.2. Normalization and notation of all the variables in QSW flyback converter

Parameters	Notation	Normalized
Input voltage	V_{in}	1
Output voltage	V_o	M
Capacitor voltage	V_{dssw}	V_{cn}
Magnetizing current	i_{Lm}	i_{Lmn}
Output current	i_o	i_{on}
Time	t	θ
Switching period	T_s	θ_s

Table 2.3. Normalized steady-state model of QSW flyback converter

$V_{cn}(\theta)=\begin{cases} nM\cos\theta+\mathrm{i}_{Lmn}(0)\sin\theta+1 \\ 0 \\ -\cos(\theta-\theta_2)+\mathrm{i}_{Lmn}(\theta_2)\sin(\theta-\theta_2)+1 \\ 1+nM \end{cases}$	$\begin{matrix} 0<\theta\le\theta_1 \\ \theta_1<\theta\le\theta_2 \\ \theta_2<\theta\le\theta_3 \\ \theta_3<\theta\le\theta_4 \end{matrix}$
$i_{Lmn}(\theta)=\begin{cases} -nM\sin\theta+\mathrm{i}_{Lmn}(0)\cos\theta \\ (\theta-\theta_1)+\mathrm{i}_{Lmn}(\theta_1) \\ \sin(\theta-\theta_2)+\mathrm{i}_{Lmn}(\theta_2)\cos(\theta-\theta_2) \\ -\mathrm{nM}(\theta-\theta_3)+\mathrm{i}_{Lmn}(\theta_3) \end{cases}$	$\begin{matrix} 0<\theta\le\theta_1 \\ \theta_1<\theta\le\theta_2 \\ \theta_2<\theta\le\theta_3 \\ \theta_3<\theta\le\theta_4 \end{matrix}$

Based on the typical steady-state waveforms of the resonant tank current and voltage shown in Figure 2.8, the corresponding state-plane diagram is shown in Figure 2.10.

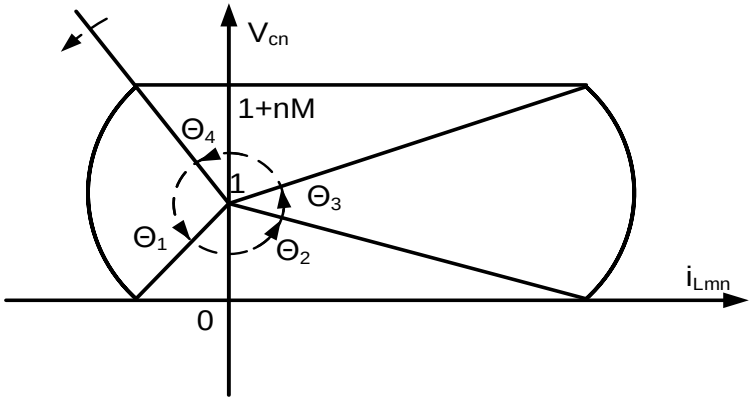


Figure 2.10. State-plane diagram for the waveforms shown in Figure 2.8.

For a QSW flyback converter, zero-voltage switching can be realized when the input/output voltages, switching frequency and power level are operating at certain conditions. The on time of SW and SR, the dead time for the resonant intervals can be calculated using the normalized state-plane diagram shown in Figure 2.10.

2.3 Steady-State Model of Quasi-Square-Wave Flyback Converter Considering Nonlinear Capacitances

The value of the magnetizing inductance and the timing of the converter are highly dependent on the nonlinear capacitance at multi-megahertz. The output capacitance C_{oss}, which is the sum of C_{ds} and C_{gd}, is the major concern for power converter design, since it must be charged or discharged by the converter power stage with each switching action. The traditional equivalent linear capacitance models introduce errors on the timing of the converter, which can be seen in Figure 2.25. An accurate steady-state model of the converter considering capacitance nonlinearity is highly demanded in the design process.

2.3.1 Nonlinear capacitances

The nonlinear effect of device capacitances on circuit operation is often ignored since the nonlinear behavior of the output device capacitance is not as important at low frequencies. As the switching frequency increases to megahertz, the nonlinear capacitance will lead to a significant discrepancy where the time required to discharge the capacitor may be significant in one switching period.

To further demonstrate the variation in C_{oss} among a variety of devices, a number of example curves are shown in Figure 2.5. In order to quantify the nonlinearity of output capacitance, a simplified empirical fit to the nonlinear capacitance C_{oss} can be expressed as

$$C_{oss}(V_{ds}) = \frac{C_0}{\left(1 + \frac{V_{ds}}{\Phi_B}\right)^m}, \tag{2.15}$$

where C_0 is the junction capacitance at zero bias and is highly process dependent; m is the junction grading coefficient, typically between 0.33 and 0.5, depending on the abruptness of the

diffusion junction; and Φ_B is the built-in potential that is determined by doping levels. Equation (2.15) is sufficiently accurate for simple devices, but inadequate for more complex, modern devices, including super junction devices as well as wide-bandgap devices [11].

The lookup table is another approach to supply the nonlinear capacitance. To achieve high accuracy of the device model, a huge dataset needs to be stored in the table. The database will be scaled exponentially if temperature coefficient or other factors need to be considered.

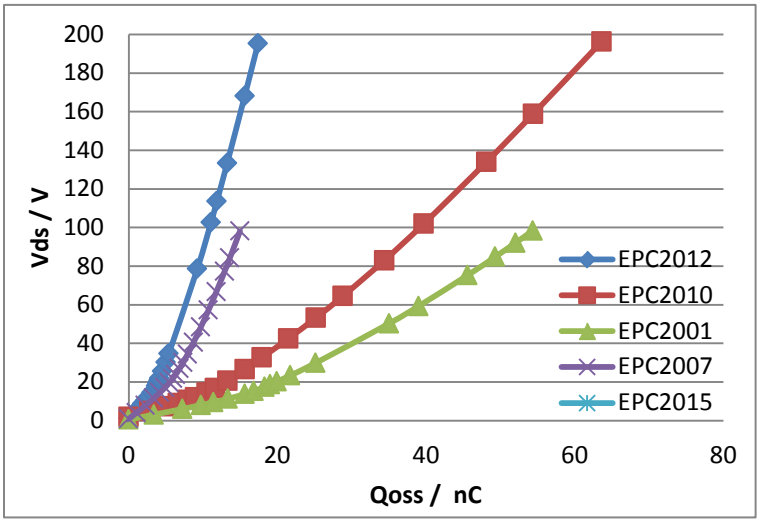


Figure 2.11. Charge versus drain-source voltage of eGaN FETs.

Because the curves in Figure 2.5 vary widely for different devices, developing methods that remain valid for the nonlinearity of capacitance is better than applying empirical fit formulas such as that of (2.15). Given a CV curve, the total charge in a nonlinear capacitance can be derived by integrating C_{oss} over the voltage range. A quadratic equation provides an adequate fit to the curves shown in Figure 2.11. Therefore the voltage across the capacitance as a function of the charge can be obtained as

$$V_{ds} = aQ_{oss}^2 + bQ_{oss} \tag{2.16}$$

where a and b are constants depending on the varying structures of the devices. The theory of charge conservation across the nonlinear capacitance could be employed in the converter design.

2.3.2 Charge based model of QSW flyback converter

A QSW flyback converter can be divided into resonant stages and linear stages during one switching period as discussed above. The steady state charge waveforms are shown in Figure 2.12. The charge on the capacitors during the linear charging or discharging of the magnetizing inductor is constant, while the nonlinear capacitances have significant influence on the timing at resonant interval. This section focuses on the analysis for resonant interval. The self-capacitance of the flyback transformer is much smaller than the output capacitance of the power switches, which could be neglected to simplify the analysis.

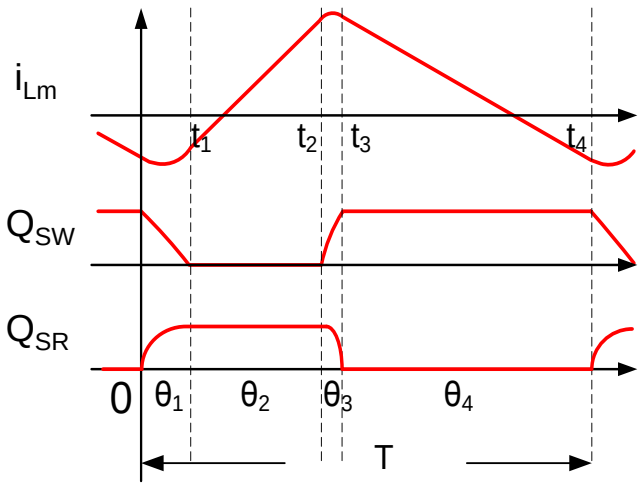


Figure 2.12. Typical charge based steady-state waveforms for ZVS QSW flyback converter.

During the resonant interval, the magnetizing inductance L_m resonates with the parasitic capacitors of SW and SR. As shown in Figure 2.4, the magnetizing current divides itself between the two devices during the transition period, charging one capacitor and discharging the other:

$$i_{Lm}(t) = i_{SW}(t) + \frac{i_{SR}(t)}{n}. \tag{2.17}$$

The amount of charge removed or stored in each capacitor is

$$Q_{SW}(t) = \int_0^t i_{SW}(t)dt + Q_{SW}(0), \tag{2.18}$$

$$Q_{SR}(t) = -\int_0^t i_{SR}(t)dt + Q_{SR}(0). \tag{2.19}$$

According to the law of total charge conservation, (2.17)-(2.19) are solved to eliminate i_{sw} and i_{sr}:

$$Q_{SW}(t) - Q_{SW}(0) - \frac{Q_{SR}(t) - Q_{SR}(0)}{n} = \int_0^t i_{Lm}(t)dt. \tag{2.20}$$

From Kirchoff's voltage law, the voltages across the capacitors of SW and SR satisfy the relation:

$$V_{dsSW}(t) = V_{in} - L_m \frac{di_{Lm}(t)}{dt}, \tag{2.21}$$

$$V_{dsSR}(t) = V_o + \frac{L_m}{n}\frac{di_{Lm}(t)}{dt}, \tag{2.22}$$

By plugging (2.16) into (2.21) and (2.22), it becomes

$$a_{SW}Q_{SW}^2(t) + b_{SW}Q_{SW}(t) = V_{\text{in}} - L_m \frac{di_{Lm}(t)}{dt}, \tag{2.23}$$

$$a_{SR}Q_{SR}^2(t) + b_{SR}Q_{SR}(t) = V_o + \frac{L_m}{n}\frac{di_{Lm}(t)}{dt}, \tag{2.24}$$

where the charging constants of eGaN FETs could be extracted from the CV curve in the device datasheets. At the end of the resonant stage, Q_{SW} reaches zero at $t = t_1$ and Q_{SR} is equal to zero at $t = t_3$. Zero voltage switching is achieved for both switches if all charges across the capacitance can be removed by the sufficient inductor current.

The linear interval is identical to those in the traditional model where the inductor is charged from t_1 to t_2, and the energy is transferred to output during t_3 and t_4. By averaging the current of SR over one switching period, the output current can be obtained by

$$i_o = \frac{1}{T_s}\int_{t3}^{t4} n \cdot i_{Lm} dt \tag{2.25}$$

where T_s is the switching period.

2.3.3 Iterative design algorithm

By considering all the specifications including input/output voltages, output power and operating frequency, a numerical iterative algorithm can be applied to find the maximum inductance to fulfill the ZVS conditions of both switches for the entire range. Meanwhile, the timing of the converter can be obtained. Figure 2.13 exhibits the step-by-step procedure of the numerical calculation algorithm.

The initial inductor current $i_{Lm}(0)$ is estimated to be a negative value close to zero. Since the nV_o is larger than V_{in}, the converter can achieve ZVS by natural resonant as critical mode if the inductance is small enough. The FET on-times (θ_2 and θ_4), resonant intervals (θ_1 and θ_3) can be derived subsequently. The iterative routine exits when the sum of time intervals is equal or close to switching period.

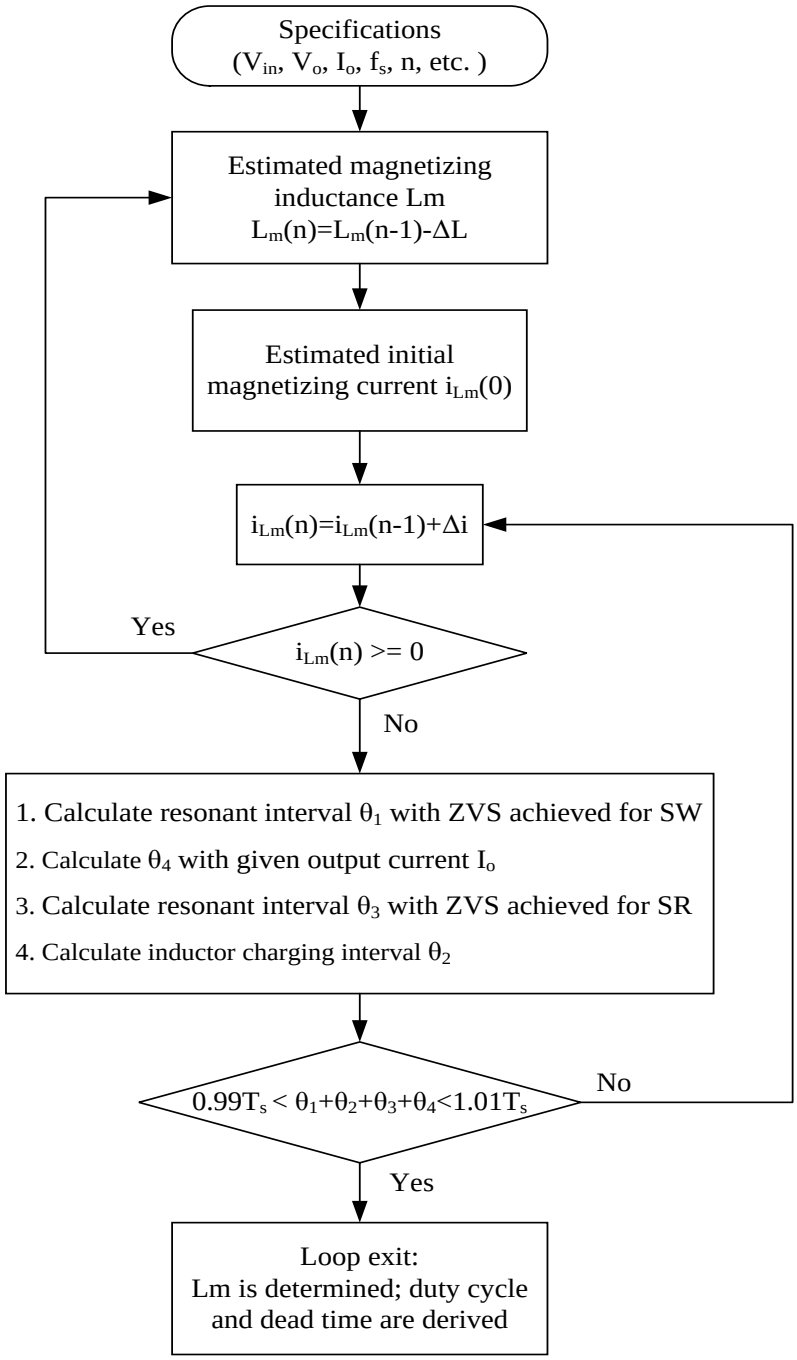


Figure 2.13. Flowchart of the numerical iterative algorithm with regard to charge based model.

2.4 Design Example of QSW Flyback Converter Using Charge Based Model

Based on the steady state model of QSW flyback converter including nonlinear capacitance, the magnetizing inductance L_m can be derived numerically with the ZVS condition of $Q_{SW}(t_1)$ =

0 and $Q_{SR}(t_3) = 0$ shown in Figure 2.12. The largest inductance should be selected to reduce the conduction loss and turn-off loss under ZVS conditions. The L_m is designed to achieve ZVS for both switches at the worst case, and thus can be applied in the entire input and load range. The timing of the QSW flyback converter can be obtained next to set the proper dead time in control loop. A high-frequency flyback converter with wide input and load range is exemplified to illustrate how to utilize the charge based steady-state model whose specifications are shown in Table 2.4.

Table 2.4 Specifications of QSW flyback converter

Line voltage	Switching frequency	Output voltage	Output power
36 V-72 V	5 MHz	12 V	30 W

2.4.1 Determination of magnetizing inductance

The magnetizing inductance needs to be designed at the worst case to achieve zero-voltage-switching for the entire input and load range. The worst case is the smallest magnetizing current condition which is employed to discharge the energy stored in the equivalent capacitor, which is low input voltage (V_{in} =36V) and full load (P_o = 30W) condition. Figure 2.14 shows the results of magnetizing current at different load and input voltage conditions. Figure 2.14 (a) and (b) indicate that if the input voltage is constant, input switch SW is harder to achieve ZVS at heavy load. Figure 2.14 (c) and (d) show that the switch SW is harder to achieve softs switching at low input voltage with the same load condition.

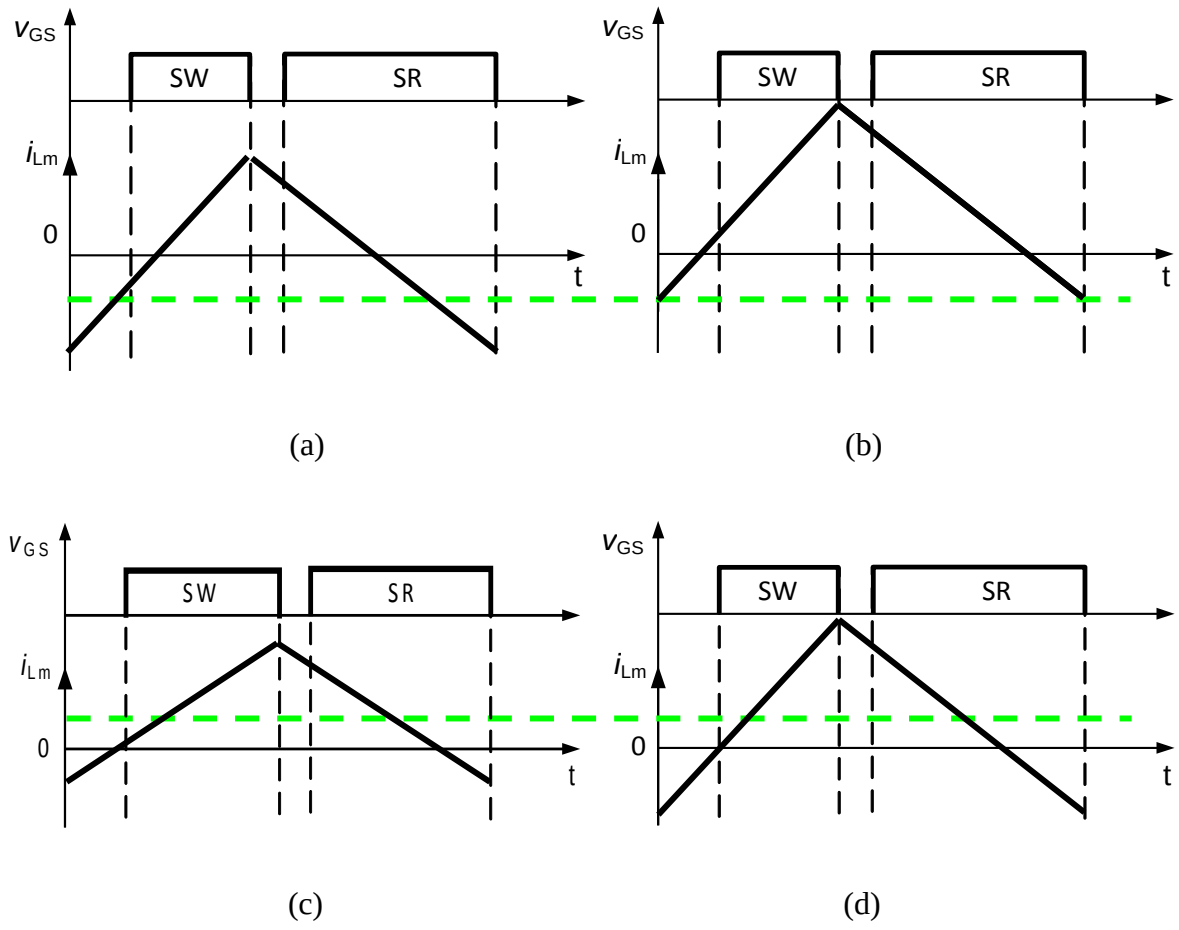


Figure 2.14. Magnetizing current waveforms at (a)V_{in} = 72 V, no load, (b) V_{in} = 72 V, full load (30 W), (c) P_o = 30 W, V_{in} = 36 V (d) P_o = 30 W, V_{in} = 72 V.

The step-by-step numerical procedure is exhibited in Figure 2.13, and the Matlab file attached in the Appendix A illustrates the detailed calculation process. EPC2012 (200 V) is the input side switch; and EPC2001 (100 V) is used as the SR on the output side. The magnetizing inductance is designed to be 0.85uH to enable ZVS over entire input and load range, and the calculated waveforms of magnetizing current i_{Lm}, switch voltage V_{dsSW}/V_{dsSR} are shown in Figure 2.15.

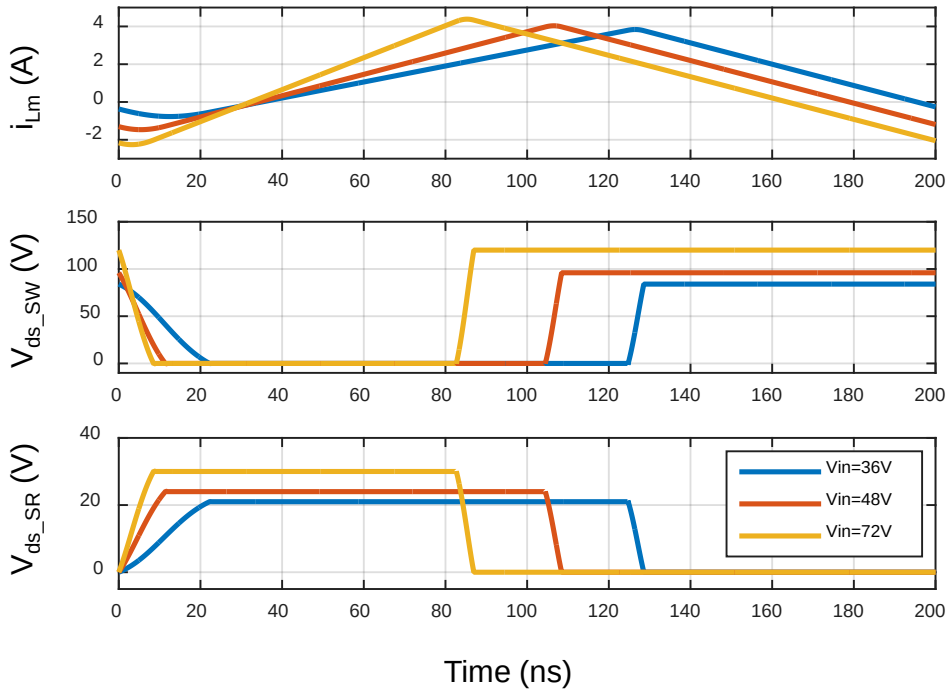
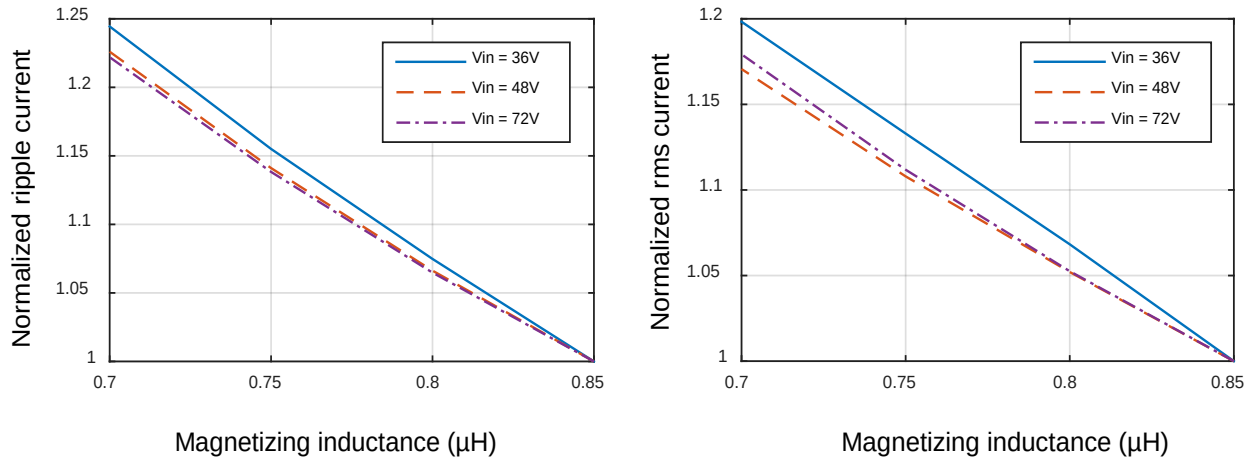


Figure 2.15. Calculated magnetizing current i_{Lm} and switch voltage V_{dsSW}/V_{dsSR} at f_s = 5 MHz, P_o = 30 W and input voltage of 36V, 48V and 72V.

The largest magnetizing inductance is preferred among all the possible solutions to achieve ZVS. If magnetizing inductance is smaller, the resonant period is shorter and the ripple current of magnetizing inductance is larger, which means that turn-off loss and conduction loss are higher. When Lm is greater than 0.85 μH, zero-voltage switching is lost for primary SW at low input voltage and the turn-on loss starts to increase. Figure 2.16 shows the magnetizing inductance versus normalized ripple and rms current of i_{Lm} at a full load of 30W and different input voltage conditions. Compared to the conduction loss and winding loss designed at magnetizing inductance of 0.85-μH, the losses will be 40% larger when the rms current increases by 20% with an inductance of 0.7-μH.



(a) (b)

Figure 2.16. (a) Magnetizing inductance versus ripple current of i_{Lm} at V_{in} = 48V, P_o = 30W and (b) Magnetizing inductance versus rms current of i_{Lm} at V_{in} = 48V, P_o = 30W.

2.4.2 Device selection

Considering the balance of voltage stress on eGaN FETs between input side and output side, the turns ratio n of coupled inductors was chosen to be 4:1. To leave adequate voltage margins for the ringing generated by the parasitic and leakage inductances, 200-V eGaN FETs was selected as input side switch; and a 100-V GaN FET was used as the SR on the output side. The available devices including the properties of R_{dson}, total gate charge Q_g, internal gate resistance R_g, thermal resistance $R_{\theta JA}$ and charging constants a, b of eGaN FETs are listed in Table 2.5.

Table 2.5 The properties of R_{dson}, total gate charge Q_g, internal gate resistance R_g, thermal resistance $R_{\theta JA}$ and charging constants a, b of eGaN FETs

	V_{ds} (V)	R_{dson} (mΩ)	Q_g (nC)	R_{gi} (Ω)	$R_{\theta JA}$ (°C/W)	a	b
EPC2010	200	25	5.3	0.4	56	$2.54 \cdot 10^{16}$	$1.56 \cdot 10^{9}$
EPC2019	200	50	1.8	0.4	72	$2.04 \cdot 10^{17}$	$2.01 \cdot 10^{9}$
EPC2012	200	100	1	0.6	85	$3.75 \cdot 10^{17}$	$5.16 \cdot 10^{9}$
EPC2022	100	3.2	13.2	0.3	42	$3.95 \cdot 10^{15}$	$5.92 \cdot 10^{8}$
EPC2001	100	7	7.5	0.3	54	$2.30 \cdot 10^{16}$	$5.86 \cdot 10^{8}$
EPC2016	100	16	3.4	0.4	69	$9.32 \cdot 10^{16}$	$8.36 \cdot 10^{8}$
EPC2007	100	30	1.6	0.4	80	$3.32 \cdot 10^{17}$	$1.54 \cdot 10^{9}$

The devices are selected to achieve the lowest total loss within the thermal constraint. The total device losses include conduction loss, turn-off loss, and gate driving loss. The conduction loss of switches is

$$P_{con} = i_{rms}^2 R_{dson} \tag{2.26}$$

The gate drive currents are

$$i_{gsw} = (V_{plsw} - V_{gsN})/R_{gsw} \tag{2.27}$$

$$i_{gsr} = (V_{plsr} - V_{gsN})/R_{gsr} \tag{2.28}$$

The turn-off loss of each switch can be derived as

$$P_{offsw} = 0.5(nV_o + V_{in}) i_{offsw} f \frac{Q_{gsw}}{i_{gsw}} \tag{2.29}$$

$$P_{offsr} = 0.5 \left(V_o + \frac{V_{in}}{n}\right) i_{offsr} f \frac{Q_{gsr}}{i_{gsr}} \tag{2.30}$$

The total driving loss is

$$P_{driving} = (Q_{sw} + Q_{sr})V_{drive}f \tag{2.31}$$

By following the design procedure shown in Figure 2.13, the maximum magnetizing inductance is obtained for various device sizes and shown in Figure 2.17.

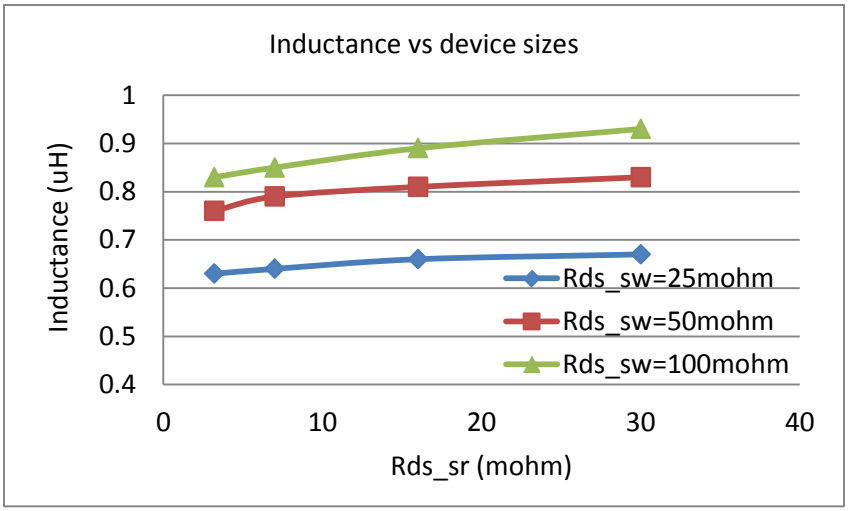
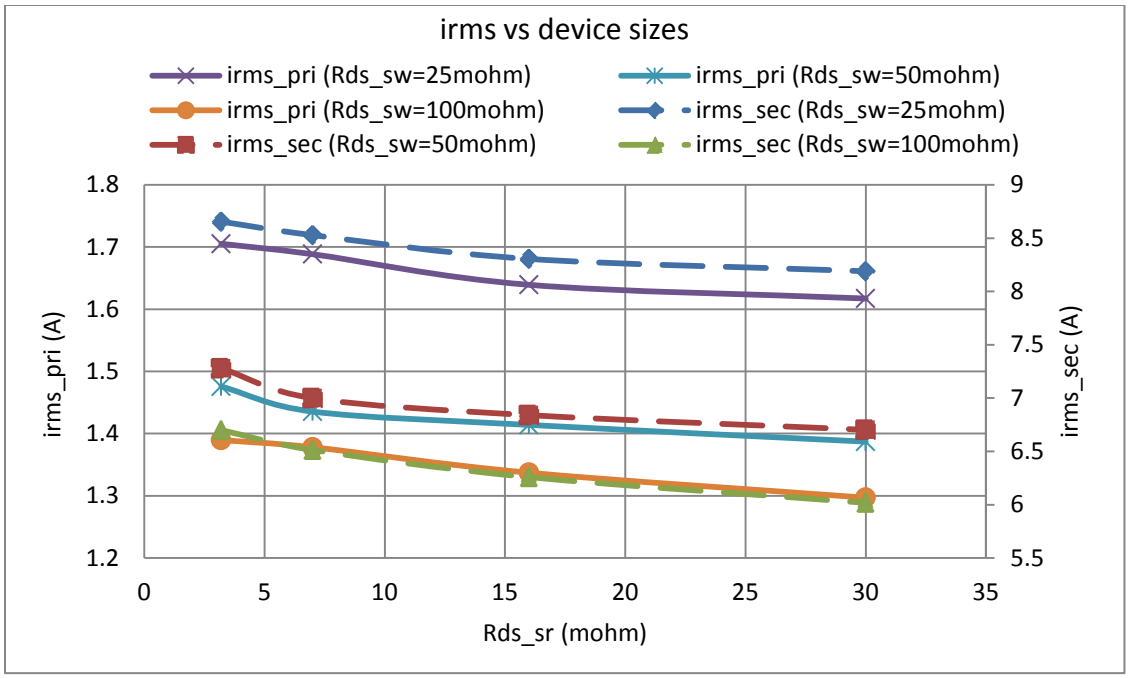
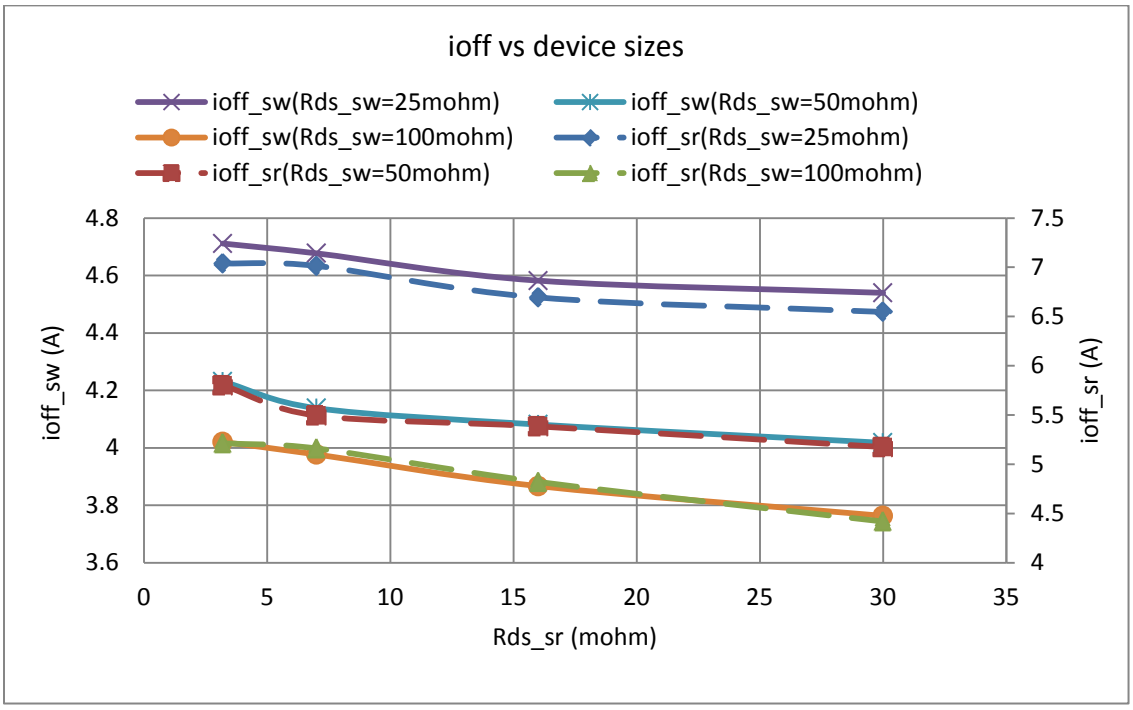


Figure 2.17. Designed magnetizing inductance for various device sizes.

The figure-of-merit (R_{ds}*Q_g) is approximate 50mΩ·nC for 100V eGaN FETs and 100 mΩ·nC for 200V eGaN FETs. Larger devices have more dies in parallel and smaller R_{ds}, so that the smaller magnetizing inductance is required to provide more energy to discharge the output capacitance. The turn-off current of input switch is the magnetizing current at t_2 shown in Figure 2.12, and the turn-off of output switch equals to the product of magnetizing current at t_4 and turns ratio. The rms current can also be calculated from the numerical model. Figure 2.18 shows rms current and turn-off current of SW and SR with different device sizes.



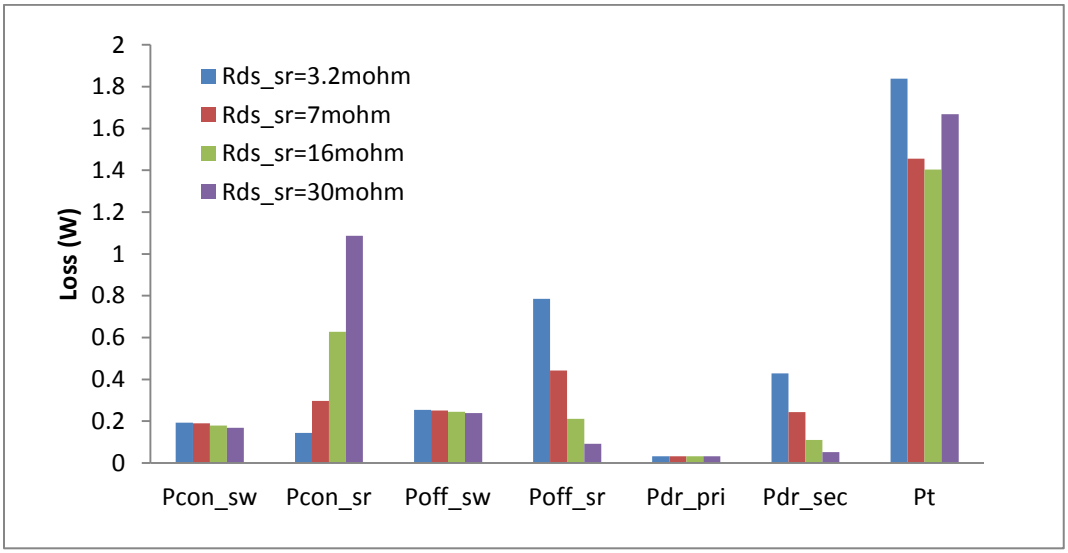
(a)



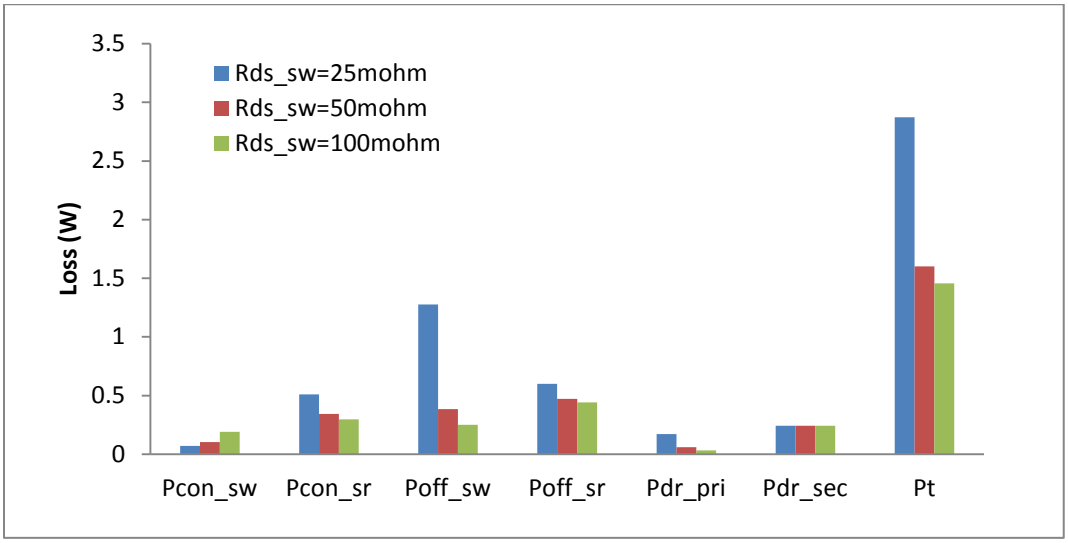
(b)

Figure 2.18. (a) Rms current and (b) Turn-off current of SW and SR for various device sizes.

Based on (2.26) to (2.31), the conduction loss, turn-off loss and gate drive loss are calculated. Figure 2.19 shows two cases of loss breakdown for SW and SR with different device sizes.



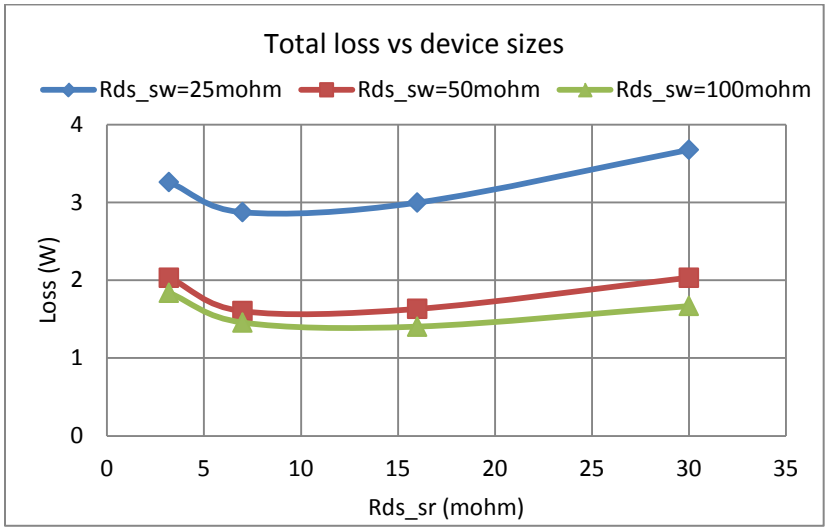
(a)



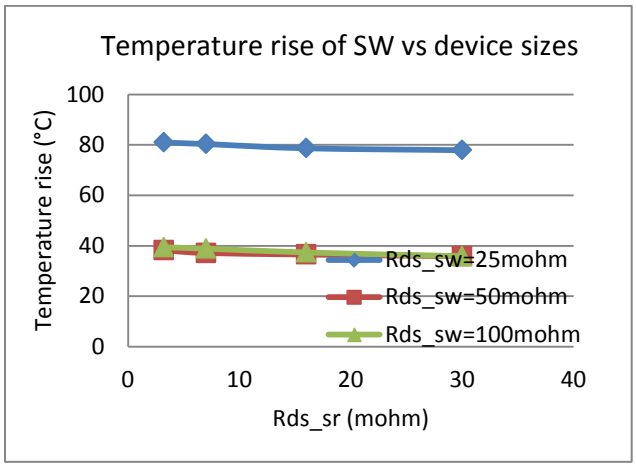
(b)

Figure 2.19. (a) Loss breakdown of different device size for SR when R_{ds_sw} = 100 mΩ and (b) Loss breakdown of different device size for SW when R_{ds_sr} = 7 mΩ.

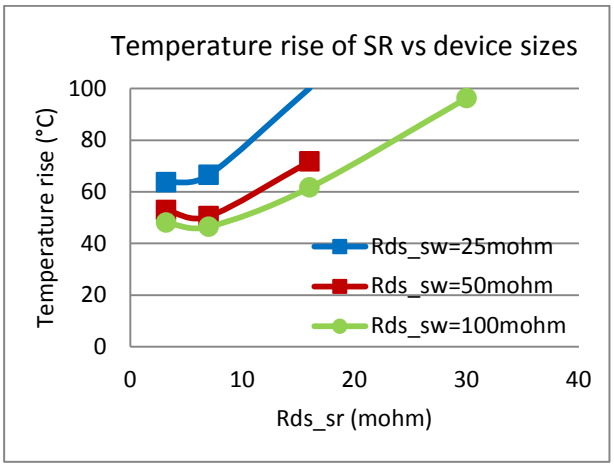
Small device with a R_{dson} of 100 mΩ was selected for SW to reduce the Q_g and the turn-off loss on the input side. On the output side, R_{dson} should be designed around 10 mΩ to achieve low conduction loss. The total losses can be derived and is shown in Figure 2.20(a).



(a)



(b)



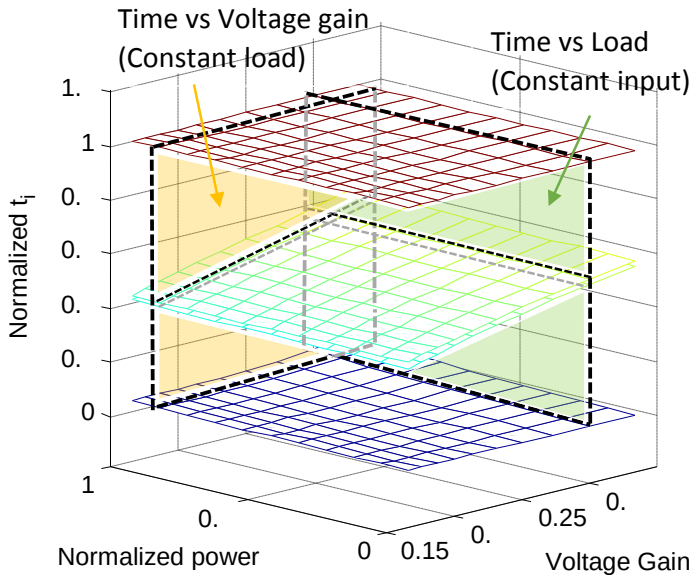
(c)

Figure 2.20. (a) Total loss for various device sizes, (b) Temperature rise of SW vs device sizes and (c) Temperature rise of SR vs device sizes.

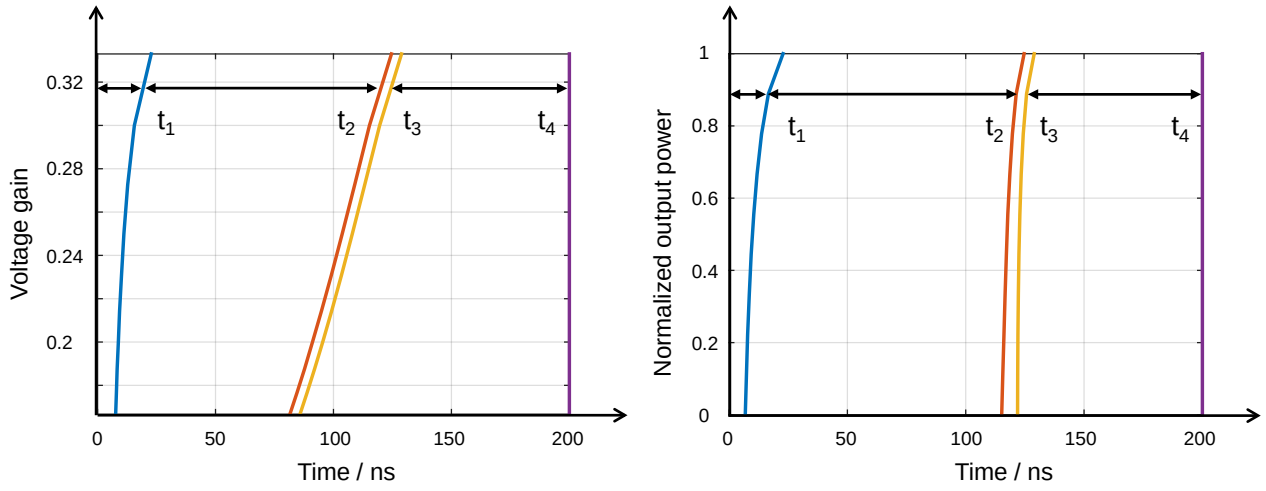
According to Table 2.5, EPC2012 was selected as input side switch; EPC2001 was used as the synchronous rectifier; and the total losses of eGaN FETs were 1.45W. With the LGA package, the thermal resistance (see in Table 2.5) is given by the manufacture. The temperature rise of SW and SR are shown in Figure 2.20(b) and Figure 2.20(c). The estimated temperature rise of SW is 39°C and temperature rise of SR is 46°C.

2.4.3 Calculation of duty cycle and dead time

After the magnetizing inductance and devices are determined, the timing (t_1, t_2, t_3, t_4) of the converter can be obtained from the charge based model, and the 3D plot of normalized time interval with different input and load in one switching period is shown in Figure 2.21(a). The time is normalized to the switching period, the power is normalized to the maximum output power, and the input voltage is represented by voltage gain. Figure 2.21(b) exhibits the time interval with different loads when V_{in} = 36 V. Figure 2.21(c) also shows how the timing (t_1, t_2, t_3, t_4) changes with variable input voltage at full load.



(a)



(b) (c)

Figure 2.21. (a) 3D plot of normalized time interval defined in Figure 2.8 with different input and load in one switching period; (b) time interval with different loads when V_{in} = 36 V; (c) time interval with different voltage gain when P_o = 30 W for the specifications shown in Table 2.4.

2.4.4 Simulation verifications

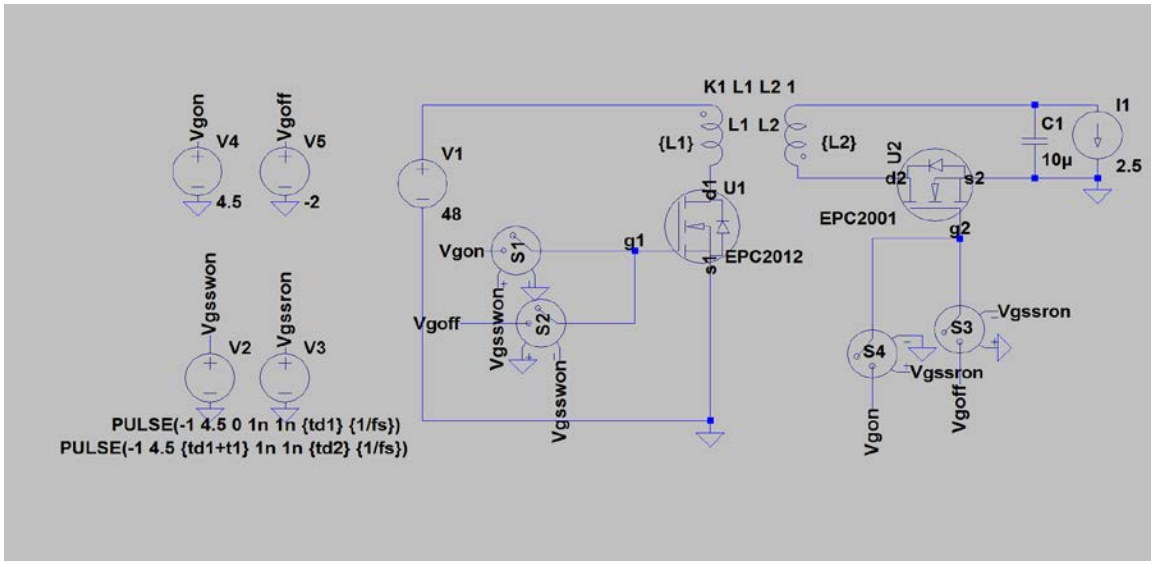


Figure 2.22. Simulation schematics of flyback converter using the specifications shown in Table 2.4.

A flyback converter was simulated in LTSpice to validate the charge based model. The simulation schematic is shown in Figure 2.22 with a rated input voltage of 48 V, an output power of 30 W, a switching frequency of 5 MHz. The magnetizing inductance is 0.87 µH which is obtained from a real prototype. To regulate the output voltage as 12 V and maintain soft switching, the duty cycle and dead-time is calculated from the charge based model as shown in Table 2.6. The steady-state waveforms of V_{dsSW}, V_{dsSR}, V_{gsSW}, V_{gsSR} and V_o are shown in Figure 2.23, and both switches are turning on softly.

Table 2.6 Calculated time interval of θ_1, θ_2, θ_3 and θ_4 at V_{in} = 48V, V_o = 12V, P_o = 30W

θ_1	θ_2	θ_3	θ_4
16 ns	90 ns	4.96 ns	89.04 ns

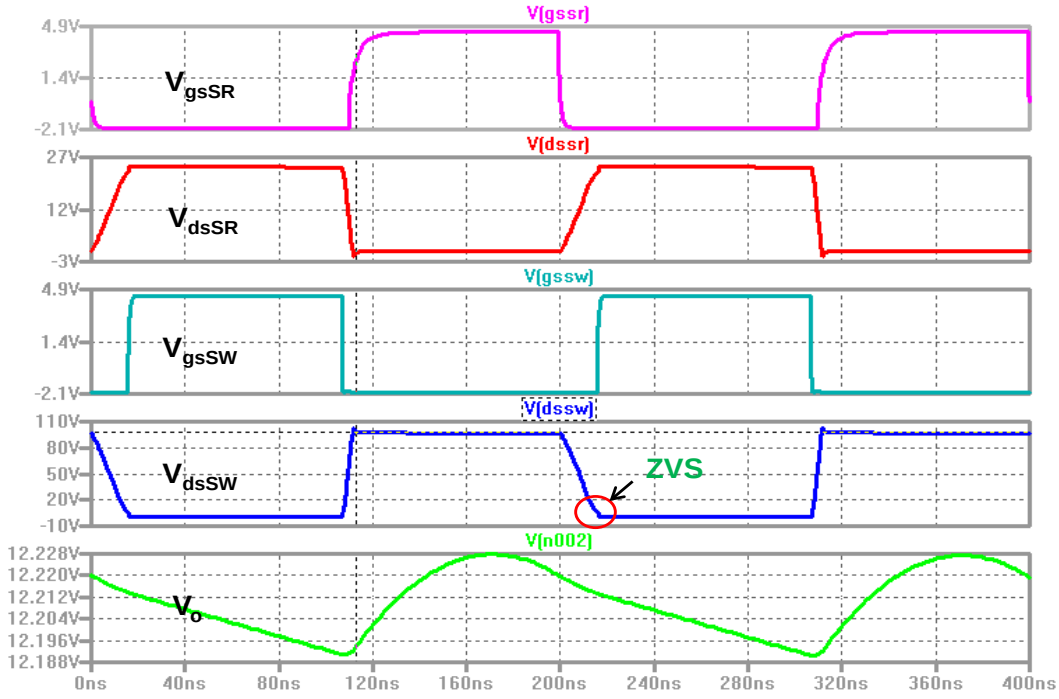


Figure 2.23. Steady-state waveforms of QSW flyback converter simulated based on the schematics shown in Figure 2.22 with the duty cycle and dead time listed in Table 2.6.

Figure 2.24 provides the comparison of V_{dssw} and V_{dssr} between the simulation and calculations from the charge based model using nonlinear capacitance and the other linear equivalents. The waveforms calculated by charge based model with nonlinear capacitance are greatly consistent with the simulation results. The value of energy-equivalent linear capacitance $C_{eq,E}$ derived from (2.8) is relatively large which introduces more error, while the linear charge equivalent $C_{eq,Q}$ can be a good approximation to derive each time intervals.

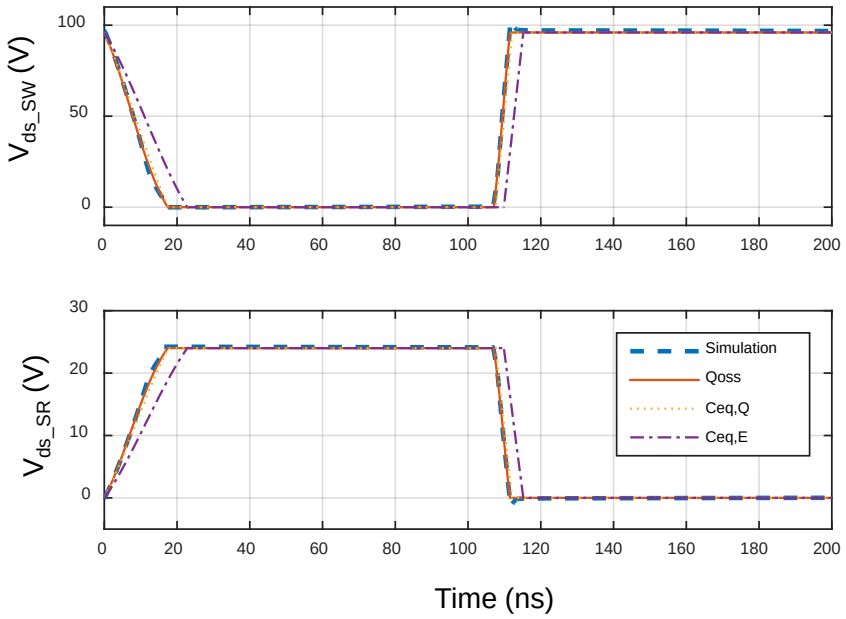
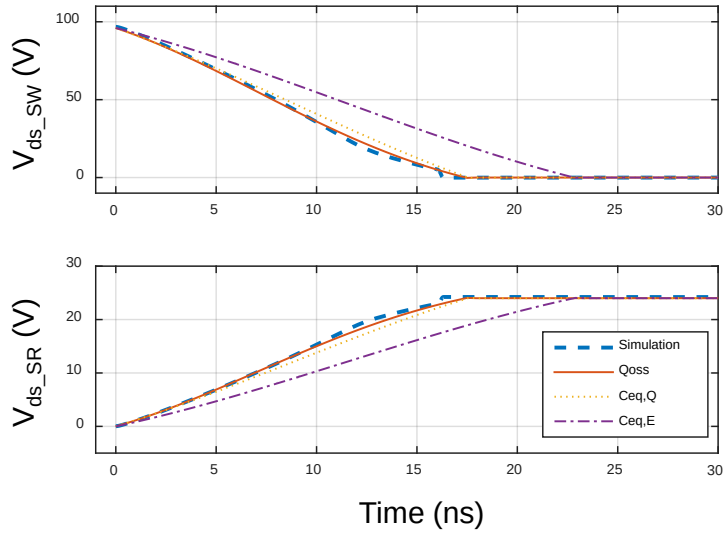


Figure 2.24. Waveforms of V_{dssw} and V_{dssr} from the simulation and calculations with nonlinear and linear equivalent capacitances in the model.

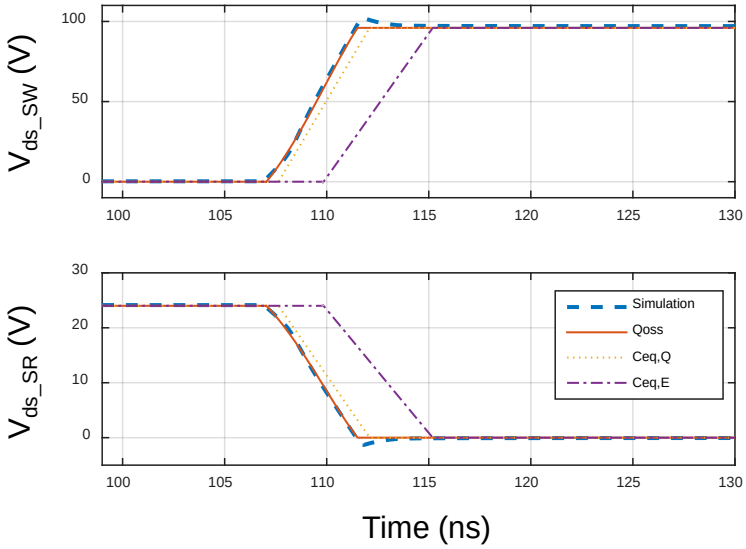
The detailed turn-on and turn-off transition period when V_{in} = 48 V, P_o =30 W and f = 5 MHz are shown in Figure 2.25. The time of resonant interval θ_1 and θ_3 are listed in Table 2.7. Approximate 40% error is introduced by energy equivalent model in the interval θ_1 with respect to the others. Since the turn-off current of SW is much larger compared to turn-on transient, the resonant time of θ_3 are only 5 ns which are almost the same for different models.

Table 2.7 Calculated time interval of θ_1, θ_3 from nonlinear and equivalent linear capacitance

	Simulation	Nonlinear capacitance Q_{oss}	Charge equivalent capacitance $C_{eq,Q}$	Energy equivalent capacitance $C_{eq,E}$
Turn-on resonant θ_1 (ns)	16	16	16	22.5
Turn-off resonant θ_3 (ns)	4.96	5	4.85	5



(a)



(b)

Figure 2.25. V_{dssw} and V_{dssr} during turn-on and -off transition period when V_{in} = 48 V, P_o =30 W and f = 5 MHz. (a) V_{dssw} and V_{dssr} with the simulation and calculations of the nonlinear capacitance, C_{oss} and the other linear equivalents developed here during period [0, t_1]; (b) V_{dssw} and V_{dssr} with the simulation and calculations of the nonlinear capacitance, C_{oss} and the other linear equivalents developed here during period [t_2, t_3].

2.5 Summary

A charge based steady-state model with the nonlinear capacitor of zero-voltage-switching (ZVS) quasi-square-wave flyback converter is proposed to improve the traditional model. It can be used to design magnetizing inductance to guarantee zero-voltage switching for the entire input and load range, and select devices to optimize the total efficiency. The timing of the converter can also be derived from the charge based model, which shows great agreements to the simulation results.

2.6 Reference

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Chapter 3 High-Frequency Magnetic Design of QSW Flyback Converter

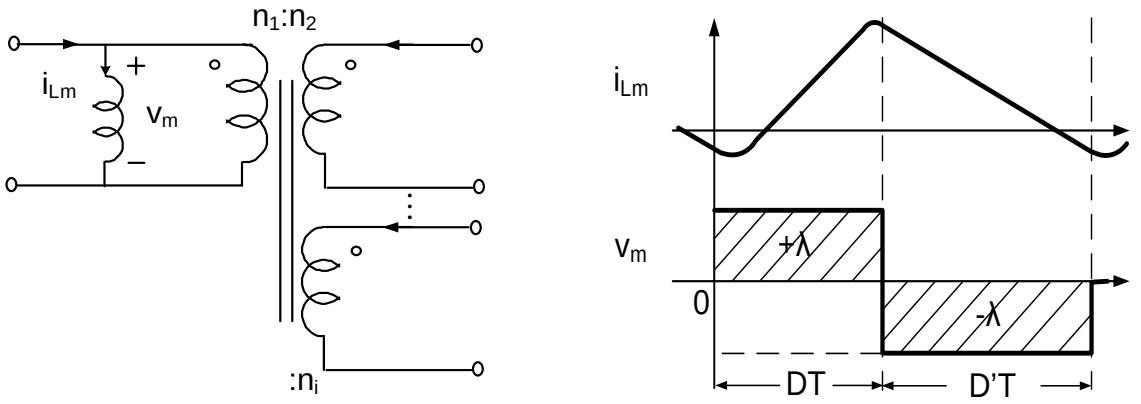
The previous section presents the derivation of the steady-state model of the quasi-square-wave (QSW) converter. The value of the magnetizing inductance can be determined based on the model to realize ZVS for both switches for the entire input and load range. This chapter addresses the physical design to select the core size of the coupled inductors.

A design procedure is introduced to select the minimal core size for an inductor that will be subjected to a significant ac flux swing. At the same time, the system must stay within the loss or thermal constraints. The geometric constant $K_{gac} = MLT/(A_c^2 W_A)$ is shown to be a power function of the core volume V_e, where A_c is the effective core area, W_A is the area of the winding window, and MLT is the mean length per turn. An iterative procedure is then described in which two- or three-dimensional proximity effects are first neglected and subsequently incorporated in the design via finite-element simulation.

3.1 Design Methodology of Geometric Constant K_{gac}

The design methodology presented here is applicable to a one-winding inductor and coupled inductors under a significant ac flux swing. The coupled inductors in Figure 3.1(a) are modeled using the magnetizing inductance L_m, the ideal transformer with a turns ratio $n_1:n_i$ for the i-th winding, and a coupling coefficient that is assumed to be one. The associated waveforms in Figure 3.1(b) facilitate the explanation of this methodology. The voltage waveform $v_m(t)$ for the inductor generally consists of a positive volt-second (flux linkage) $+\lambda$ and a negative volt-second $-\lambda$ under the steady state, as illustrated in Figure 3.1(b). For the inductor in a buck converter, $\lambda =$

($V_{in} - V_{out}$)DT, whereas $\lambda = V_{in}$DT for the inductor or coupled inductors in a boost converter, buck-boost converter, or flyback converter. The ripple current of the magnetizing inductance i_{Lm} is much larger than the dc current, which results in significant ac flux and core loss.



(a) (b)

Figure 3.1. (a) Coupled inductor model and (b) Pertinent current and voltage waveforms.

The overall design methodology is summarized in the flowchart in Figure 3.2. The single-pass basic design procedure is a useful method to apply in low-frequency inductors with negligible core loss. An improved iterative design procedure is developed to be used when the proximity effect in the winding is significant at high frequencies, and the waveform factor, dc bias and temperature effect of the core loss need to be modeled.

The specific design curves of P_{total} versus volume V_e are shaped by the critical parameters of the ac to dc resistance ratio F_{Ri} and the ac flux density B_{ac}, which are elaborated in detail in the later section. The two-dimensional curve of P_{total} versus V_e can be plotted by sweeping the intermediate variable B_{ac}. Volume (V_e) can be obtained subsequently by solving the curve function under a given value of P_{total}. The calculated core volume serves as a baseline for

selecting the commercial core. The geometrical parameters A_c, W_A, and MLT would be known; the ac flux density B_{ac} is derived.

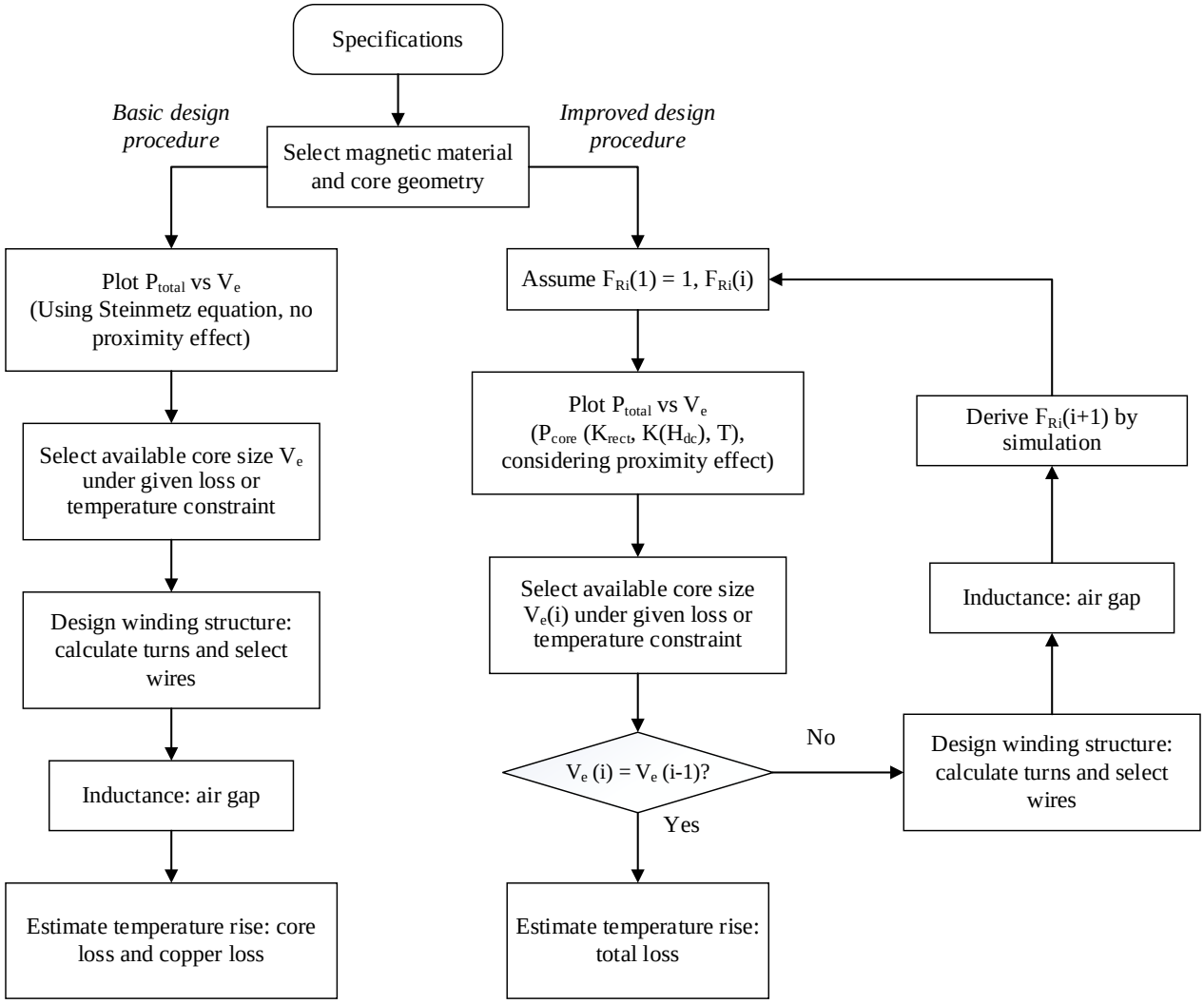


Figure 3.2. Flowchart of the design procedure for the K_{gac} method.

The number of turns (n_1) for the primary winding can be obtained; its value should be rounded to an integer. The number of turns n_i for the i-th winding can be computed on the basis of a set turns ratio. The wire size is generally selected from standard wire tables. For a printed circuit board (PCB) winding structure, the winding area may not exactly correspond to the

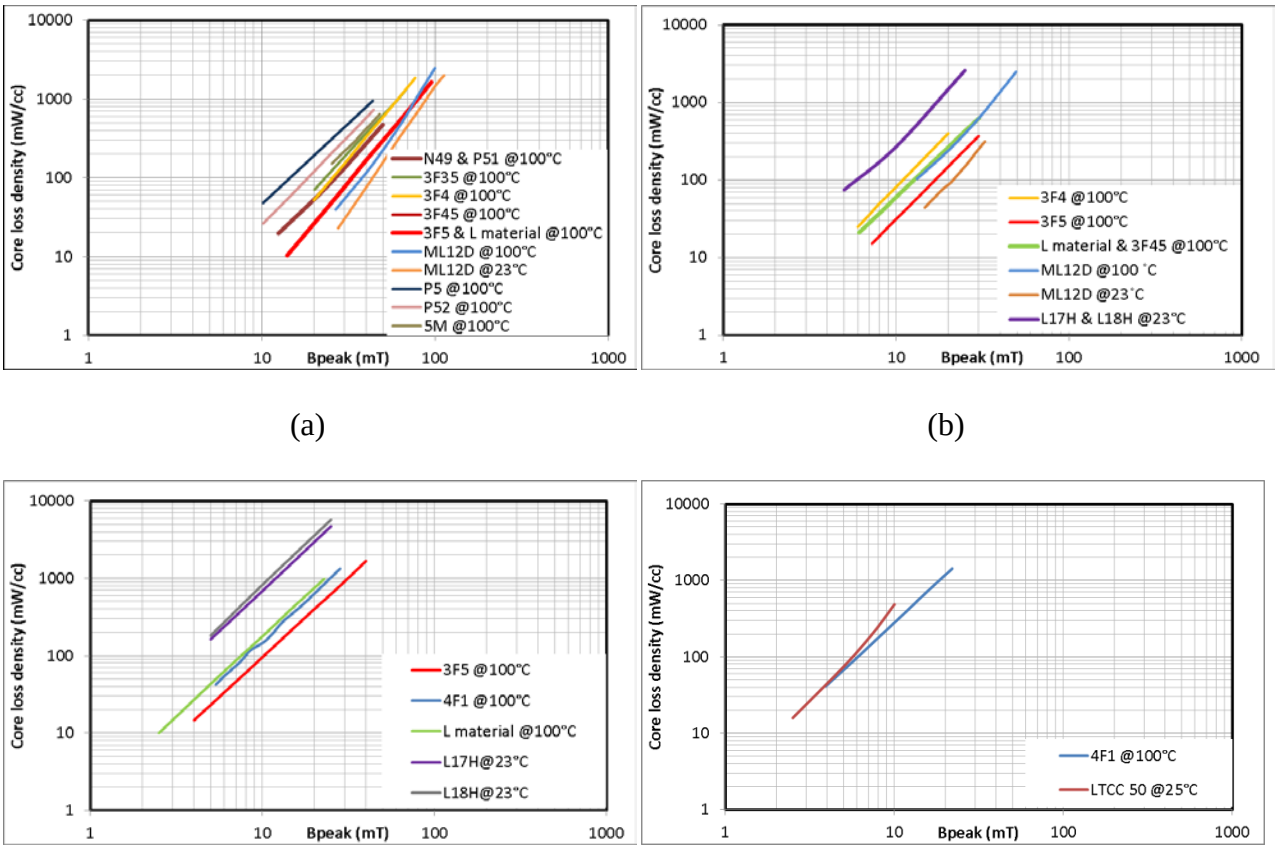
optimum selection, which is limited by the arbitrary selection of the fill factor K_u. This discrepancy results from an additional area of insulation and dielectric material. The air gap length l_g is found for the given inductance.

For an improved design procedure, the iterative process derives the accurate copper loss. Finite-element analysis (FEA) simulation is conducted, and $F_{Ri}(i+1)$ can be obtained to replace the initial arbitrary $F_{Ri}(1)$. The volume of the core will be redesigned for comparison with the previous core by repeating the design steps. The iteration will run continuously until the volumes derived by different loops are identical. The core loss and copper loss of the minimized inductor or coupled inductors can be subsequently predicted, and the temperature rise of the coupled inductors can be estimated.

3.2 Survey of High-Frequency Magnetic Materials

The combinations of manganese and zinc (MnZn) or nickel and zinc (NiZn) are the most popular ferrites that exhibit good magnetic properties in the megahertz range. In order to select a suitable magnetic material, we surveyed commercial soft ferrite products [1]-[4] that can operate from 1 MHz to 5 MHz.

Core loss density is a strong function of temperature, and can vary by a factor of three. A minimum loss point generally exists between 23°C and 100°C in the U-shaped loss curve. Most data are measured at 100 °C in the datasheet, which is close to practical circumstances.



(a) (b)

(c) (d)

Figure 3.3. Core loss density at (a) 1 MHz, (b) 2 MHz, (c) 3 MHz and (d) 5 MHz.

Ferroxcube and Magnetics, Inc. are popular manufacturers of ferrite materials. FINEMET (Hitachi), TDK-EPC, ACME, and Nicera also have some competitive products for using at high frequencies. Figure 3.3(a) shows the core loss density as a function of peak flux density at 1 MHz. The ML12D (Hitachi) material has the smallest core loss. The core loss density is only 30 mW/cm^3 at 23°C when B_{peak} equals to 30 mT. Among the other materials from Ferroxcube, 3F5 has the lowest loss. L material from Magnetics, Inc. stands at the same level as 3F5.

Figure 3.3(b) shows the core loss densities as a function of peak flux density at 2 MHz. Materials ML12D and 3F5 perform the best. The core loss density is 150 mW/cm^3 when B_{peak}

equals 30 mT. The eddy-current loss in the core also becomes significant as the frequency increases.

Figure 3.3(c) shows the core loss density as a function of peak flux density at 3 MHz. The better choices are 3F5 and 4F1 from Ferroxcube. NiZn ferrite (4F1) is more suitable when the frequency is greater than 3 MHz. LTCC 50 is another option in the 3-5 MHz range. The core loss curve is measured and shown in Figure 3.3(d).

3.3 Derivation of Design Curves

The design curves of P_{total} versus volume V_e are shaped by the critical parameters of F_{Ri} and $B_{ac.}$ The basic design equations for the inductance, losses, and other parameters are required to plot the design curves, and are derived below.

3.3.1 Inductance

Based on Ampere's law and the characteristics of magnetic materials, the inductance with an air gap is

$$L_m = \frac{\mu_0 n_1^2 A_g}{\frac{l_e}{\mu_r} + l_g}, \tag{3.1}$$

where μ_0 is the permeability of free space, which is equal to $4\pi \cdot 10^{-7}$ (H/m); μ_r is the relative permeability; l_e is the effective length of the magnetic circuit; l_g is the gap length; and A_g is the effective cross-sectional area of the magnetic circuit, considering the fringing effect. The total flux in the air gap must be identical to the total flux in the core, but must spread over a larger cross-sectional area. A well-known approach to model the fringing effect caused by the air gap is illustrated in [5]. The effective cross-sectional areas of a magnetic circuit with an air gap are

$$\begin{cases} A_g = (a + l_g)(d + l_g), & \text{if } A_g \text{ is rectangular,} \\ A_g = \pi\left(r + \frac{l_g}{2}\right)^2, & \text{if } A_g \text{ is circular,} \end{cases} \tag{3.2}$$

where a is the core width, d is the length of the rectangular cross-sectional area, and r is the radius of the circular cross-section.

3.3.2 Core Loss

Despite the bias effect and temperature effect, the most classical core loss model is the Steinmetz Equation, which can be expressed analytically as

$$P_{core} = K_{fe} f^{\alpha} B_{ac}^{\beta} \cdot V_e = P_v \cdot V_e \tag{3.3}$$

where P_v is the core loss density, and K_{fe}, α, and β are Steinmetz coefficients. This model is defined for sinusoidal waveforms. For triangular field shapes such as those shown in Figure 3.1(b), the peak of the ac flux density B_{ac} can be derived as

$$B_{ac} = \frac{\lambda}{2n_1 A_c} = \frac{L_m I_{Lmac}}{2n_1 A_c}. \tag{3.4}$$

where A_c is the effective cross-sectional area of magnetic circuit, and I_{Lmac} is the peak-to-peak magnetizing current. The value of the flux density is chosen to be less than the worst-case saturation flux density B_{sat} of the core material. If the ripple current is significant compared to the dc current, the core loss will be significant because of the large ac flux. The flux density is not limited by the saturation flux density B_{sat}, but is restricted by the large core loss.

A model called the RESE [6] is employed to calculate the core loss under rectangular ac voltages. The core loss P_{core} can be calculated as

$$P_{core} = P_v \cdot V_e = \frac{8}{\pi^2[4D(1-D)]^{\gamma+1}} K_{fe} f^{\alpha} B_{ac}^{\beta} \cdot V_e, \tag{3.5}$$

where the value of γ is a function of the frequency, flux density, and temperature. The core loss model with a pre-magnetization can be modeled as the product of the zero-bias core loss density and the bias factor

$$P_{core} = P_v \cdot V_e \cdot K(H_{dc}), \tag{3.6}$$

where $K(H_{dc})$ is the bias factor whose value is curve-fitted by the measurement data. The ferrite material (LTCC40011) is characterized under the dc bias condition [7] shown in Figure 3.4. The spacing between the three measurement points of 5, 7.5, and 10 mT are almost constant for different dc biases, which means we can assume that the factor $K(H_{dc})$ is only affected by H_{dc}. The hysteresis loss is caused by the movement of the domain wall, which is affected by dc offset, while eddy current loss is independent of dc bias, which has no impact on the electrical resistance of magnetic material. The impact of the ac and dc components on the core loss can be decoupled.

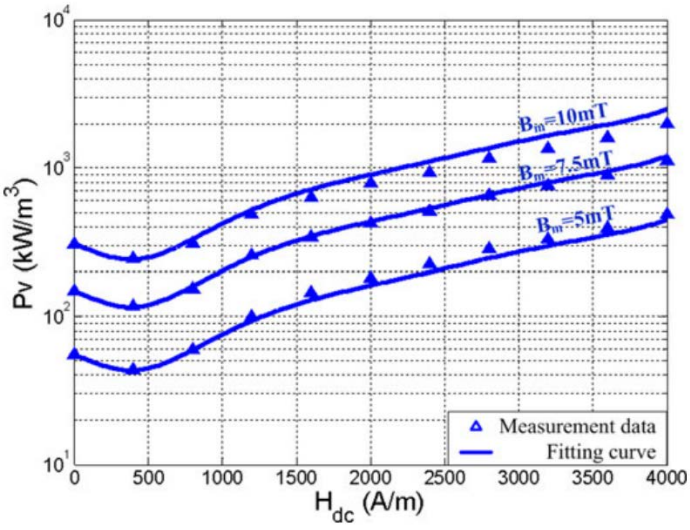


Figure 3.4. Core loss of ferrite material under the dc bias conditions [7].

Core loss density P_v is limited by the maximum temperature that can be allowed in the material. A commonly used maximum temperature for many applications is 100 °C. At this temperature, the maximum P_v is in hundreds of kilowatts per meter cubed [5]. The exact value of P_v depends on how efficiently the heat is removed; that is, on the thermal resistance between the core and the ambient. The impact of temperature can also be modeled as a factor multiplied by the Steinmetz equation [8]. It may be reasonable to multiply the temperature factor by the dc bias factor to describe the core-loss change at a certain bias and temperature, but whether the dc bias factor can be decoupled from the temperature factor needs to be investigated.

3.3.3 Winding Loss

The winding loss ($P_{winding}$) of an inductor and coupled inductors is the sum of the dc winding loss and ac winding loss,

$$P_{winding} = \sum_{i=j} I_{irms}^2 R_i = \sum_{i=j} (I_{idc}^2 R_{idc} + I_{iac}^2 R_{iac}), \tag{3.7}$$

where j is 1 for a single inductor, R_{idc} is the dc resistance of the i-th winding, R_{iac} is the ac resistance of the i-th winding, I_{idc} is the dc current in the windings, and I_{iac} is the root mean square (rms) current of the ac components, which is equal to

$$I_{iac}^2 = I_{irms}^2 - I_{idc}^2. \tag{3.8}$$

The dc winding resistance R_{idc} is

$$R_{idc} = \frac{\rho n_i MLT}{A_{wi}}. \tag{3.9}$$

where A_{wi} is the cross-sectional area of the i-th winding. The mean length per turn MLT of the ER-shaped core equals the equivalent circumference, which is the average of the inner circumference and outer circumference for the winding window. The fill factor K_u is a fraction of

the core window area that is filled with wire and must lie between zero and one, which is determined by the type and size of the wire, insulation, bobbin, and other components. For PCB windings, the fill factor is determined by the copper thickness and the number of winding layers, and the value of Ku is relatively low, as it is limited by insulation and dielectric material. Therefore,

$$\alpha_i K_u W_A = n_i A_{wi}. \tag{3.10}$$

where α_i is ratio of the *i*-th winding to the total winding area, and W_A is window area. By solving (3.4), (3.9) and (3.10) to eliminate A_{wi}, the dc resistances become

$$R_{idc} = \frac{\rho MLT n_i^2}{\alpha_i K_u W_A} = \frac{\rho}{\alpha_i K_u}\left(\frac{\lambda}{2B_{ac}}\frac{n_i}{n_1}\right)^2 \frac{MLT}{W_A A_c^2}, \tag{3.11}$$

where the turns ratio n_i:n_1 is often given. It is desirable to choose α_i to minimize the total winding loss. The optimal choice for α_i is found from [9]:

$$\alpha_i = \frac{n_i I_{irms}}{\sum_{i=j} n_i I_{irms}}, \tag{3.12}$$

$$\sum_{i=j} \alpha_i = 1, \tag{3.13}$$

where α_1 is 1 for a single-winding inductor when j = 1, and α_i is often the function of the duty cycle *D*, depending on the operation of the topology for the coupled inductors. Considering the increasing winding loss caused by high-frequency skin and proximity effects, the ac resistance is assumed to be F_{Ri} times the dc resistance:

$$R_{iac} = \mathrm{F}_{Ri} R_{idc}. \tag{3.14}$$

The proximity fields are often two- or three-dimensional in the practical winding window for a high-density inductor, whereas analytical models of the ac winding loss that rely on one- or quasi-two-dimensional assumptions are invalid (Figure 3.5).

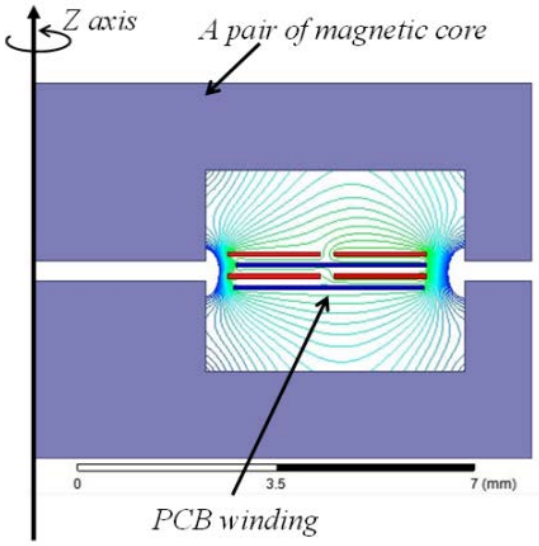


Figure 3.5. Irregular flux lines around the conductor with an air gap.

The parameter F_{Ri} is quantified by finite-element simulation. An iterative design procedure is performed to initially set F_{Ri} to one and update its value after each iteration. By solving (3.7), (3.8), (3.11), and (3.12), the winding loss can be expressed as

$$P_{winding} = \sum_{i=j} (I_{idc}^2 + I_{iac}^2 \mathrm{F}_{Ri}) R_{idc} = \sum_{i=j} [I_{idc}^2 + (I_{irms}^2 - I_{idc}^2)\mathrm{F}_{Ri}] \frac{\rho}{\alpha_i K_u} \left(\frac{\lambda}{2B_{ac}} \frac{n_i}{n_1}\right)^2 \frac{MLT}{W_A A_c^2}, \quad (3.15)$$

where the rms winding current and flux linkage can be derived according to the operation of the converters under a large ac flux swing.

3.3.4 Core Geometric Constant K_{gac}

The shape of the magnetic core is selected based on the application. It is convenient to define a geometric constant K_{gac}, which can be used to generally quantify all the core shapes. The geometric constant K_{gac} is defined to MLT/($A_c^2W_A$) based on the analytical equation of winding loss.

The physical quantities MLT, W_A, and A_c are related to the core size V_e by dimensional analysis for various core shapes. The results of regression analysis (Figure 3.6(a)) based on a series of data from commercial ER cores supplied by the core manufacturers [10] show an excellent correlation (y = 19.405x$^{-1.783}$, R^2 = 0.9948) between the geometrical parameters MLT/($W_A \cdot A_c^2$) and the core volume V_e. The regression analysis between MLT/($W_A \cdot A_c^2$) and core volume V_e for other core shapes are shown in Figure 3.6. To eliminate the term MLT/($W_A \cdot A_c^2$) in (3.15), it becomes

$$P_{winding} = \sum_{i=j} [I_{idc}^2 + (I_{irms}^2 - I_{idc}^2)F_{Ri}] \frac{\rho}{\alpha_i K_u} \left(\frac{\lambda}{2B_{ac}} \frac{n_i}{n_1}\right)^2 a_1 V_e^{-a_2}, \qquad (3.16)$$

where a_1 and a_2 are constants depending on the core shape (e.g., E core, toroid). Table 3.1 lists a_1 and a_2 for commercial ER, EI, toroidal, and PQ cores [10]–[12].

Table 3.1 Values of a_1 and a_2 for different core shapes

	a_1	a_2
EI cores	1.533	2.02
ER cores	19.41	1.78
Toroidal cores	13.25	1.79
PQ cores	5.84	1.82

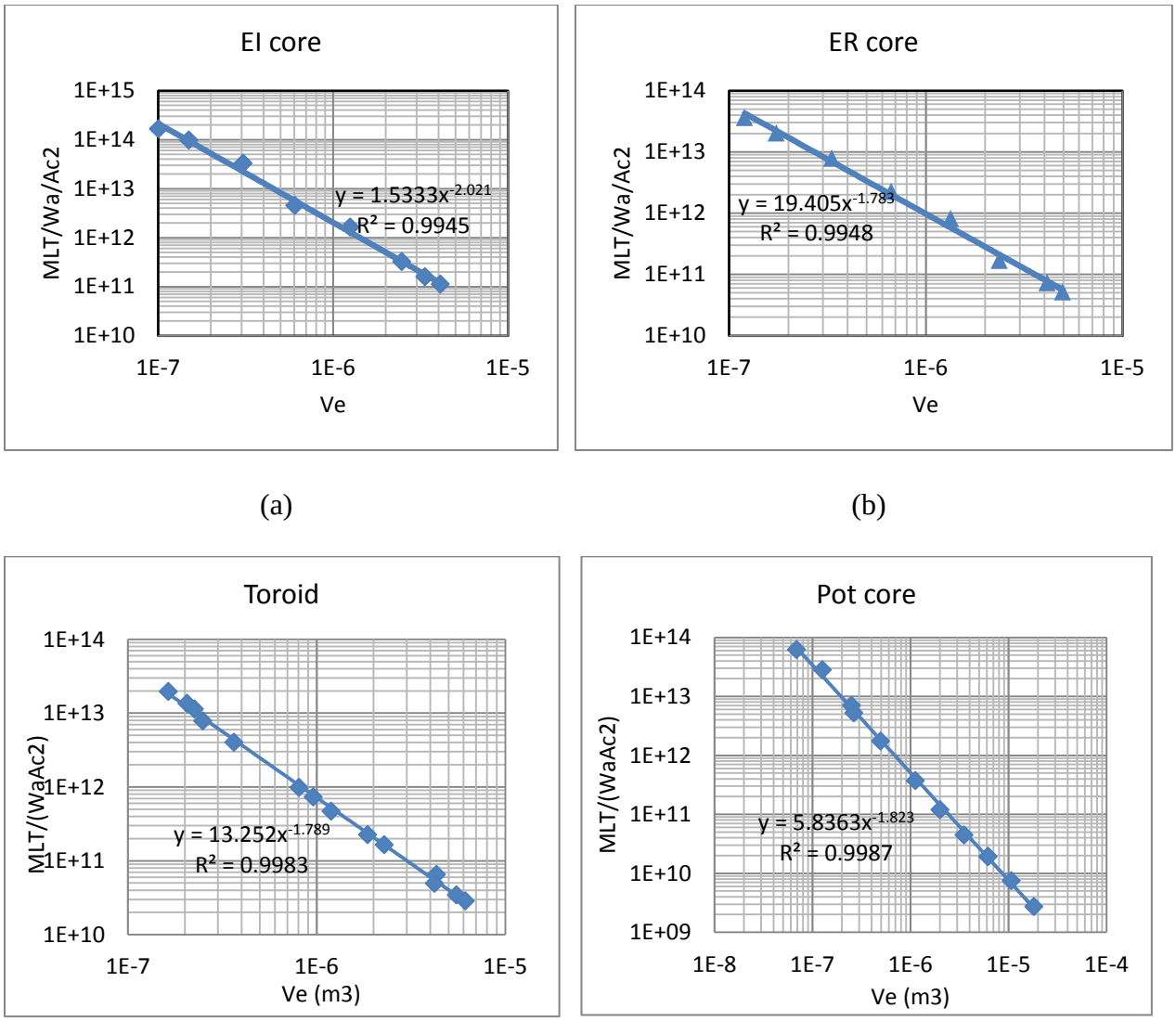


Figure 3.6. Regression analysis between MLT/($W_A \cdot A_c^2$) and core volume V_e (a) EI core, (b) ER core, (c) Toroidal core and (d) Pot core.

By adding (3.6) and (3.16), the total loss P_{total} is obtained as

$$P_{total}(V_e, B_{ac}) = P_{winding} + P_{core} = K_w a_1 V_e^{-a_2} + P_v V_e, \tag{3.17}$$

where $K_w = \sum_{i=j}[I_{idc}^2 + (I_{irms}^2 - I_{idc}^2)\mathrm{F}_{Ri}]\frac{\rho}{\alpha_i K_u}\left(\frac{\lambda}{2B_{ac}}\frac{n_i}{n_1}\right)^2$.

The derivative of the total loss (3.17) with respect to the volume, dP_{total}/dV_e, is set to zero to choose the core volume that minimizes the total loss. Then, the minimum volume of the core is calculated as

$$V_e(B_{ac}) = \left(\frac{K_w a_1 a_2}{P_v}\right)^{\frac{1}{a_2+1}}. \tag{3.18}$$

The specific design curves of P_{total} versus the volume V_e are shaped by the critical parameters of B_{ac} according to (3.17) and (3.18). The value for V_e can be obtained by solving the curve function under a given total loss P_{total} and by taking the most approximated value, from which the commercial core's volume can be selected.

3.3.5 Temperature Rise of Coupled Inductors

The temperature rise of a single inductor or coupled inductors occurs because the loss is dissipated by the inductors in the form of heat. The heat is divided into conduction, convection, and radiation. Linear thermal resistances are frequently used for conductive heat transfer. Convective and radiant heat transfer are nonlinear and depend on the instantaneous temperature difference between the object and the ambient. It is difficult to derive an accurate thermal model without statistical experimental data.

An empirical formula that lumps the winding loss and core loss together is used to estimate the temperature rise of the inductor with the assumption of an uniform dissipation of thermal energy throughout the surface area of the assembly at all ambient temperatures under natural air cooling:

$$\Delta T = \left(\frac{P_{total}}{A_T}\right)^{0.833}, \tag{3.19}$$

where P_{total} is the total loss in milliwatts, and A_T is the surface area of the coupled inductors in centimeters squared. The exponent (0.833) used in the above formula to estimate the temperature rise was derived from empirical data [13].

According to a series of data for commercial EI cores supplied by the core manufacturer [10], the total surface area A_T of the EI core and PCB winding is a power function of the core volume V_e as shown in Figure 3.7.

$$A_T = a_3 V_e^{a_4}, \tag{3.20}$$

where a_3 is 20.08 and a_4 is 0.671 for an EI-shaped core.

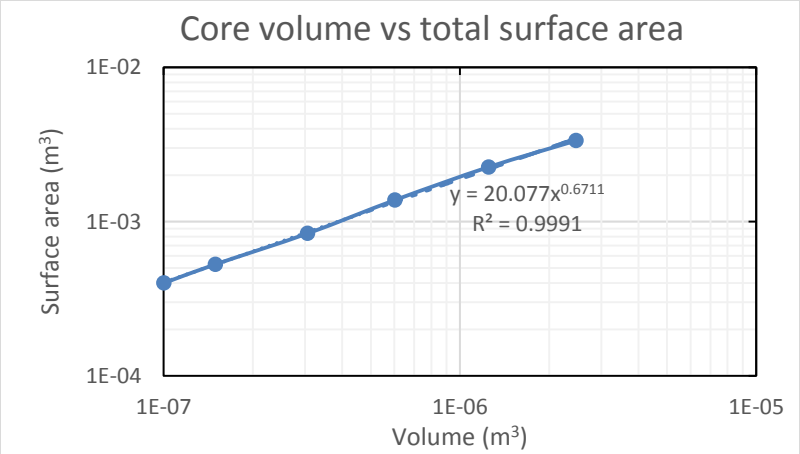


Figure 3.7. Regression analysis between total surface area A_T and the volume of core V_e.

To eliminate the A_T in (3.19) using (3.20) yields

$$\Delta T = \left(\frac{P_{total}}{a_3 V_e^{a_4}}\right)^{0.833} \tag{3.21}$$

where V_e is the core volume in cubic meters, a_3 and a_4 vary with different core shapes.

3.4 Design Example of Coupled Inductors

The two-winding coupled inductors in a flyback converter are used as an example to illustrate the iterative design procedure. The value of the ac resistance is not significantly affected by skin and proximity effects in low-frequency design. A single-pass design process may be sufficient to find the right volume of the core. It is difficult to calculate the ac resistance accurately using a mathematical model because of the effects of fringing and proximity at high frequencies. An iterative procedure to select the core and update the value of F_{Ri} is demonstrated on the basis of the FEA simulation.

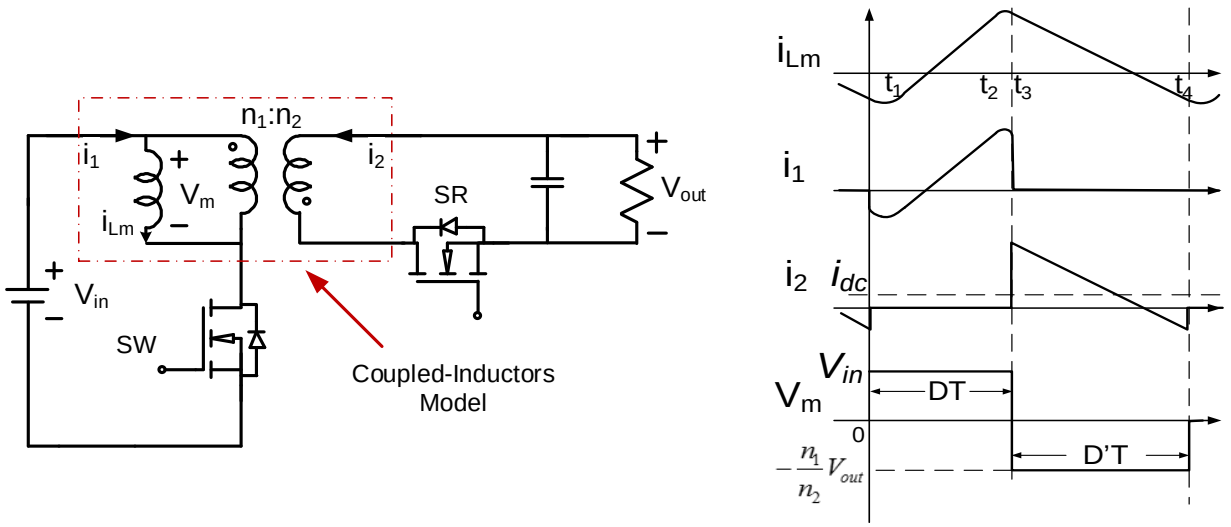


Figure 3.8. (a) Coupled inductors embedded in flyback converter and (b) Typical current and voltage waveforms.

The design specifications of a power converter operating at 5 MHz are shown in Table 3.2. The total efficiency of the converter is required to be above 90%. The estimation of magnetic loss is 0.8 W, which ensures that the temperature of the flyback transformer remains in the safe region.

Table 3.2 Specifications of power converter operating at 5 MHz

Input voltage	48 V
Output voltage	12 V
Magnetizing inductance	0.85μH
Duty cycle	0.45
DC current on the secondary side (I2dc)	2.5 A
Turns ratio n = n1/n2	4

3.4.1 Selecting Material and Core Geometry

Commercial NiZn ferrite (4F1) is the most suitable material for use at 5 MHz. The specifications for 4F1 are listed in TABLE 3.3. To limit the core loss density to less than 4000 kW/m^3 at 5 MHz, the maximum ac flux density is restricted to 50 mT based on the P_v–B_{ac} graph provided by the magnetic core manufacturer.

Table 3.3 Specifications for NiZn ferrite 4F1

Parameter	Value
K_{fe}	0.327 kW/(m^{3}MHz$^{\alpha}$mT$^{\beta}$)
α	1.24
β	2.07
B_{acmax}	50 mT
B_{sat}	0.3 T
μ_r	80

A planar EI-shaped core (Figure 3.9) is selected; its geometric coefficients are $a_1 = 2.49$ and $a_2 = 1.93$ (Table 3.1).

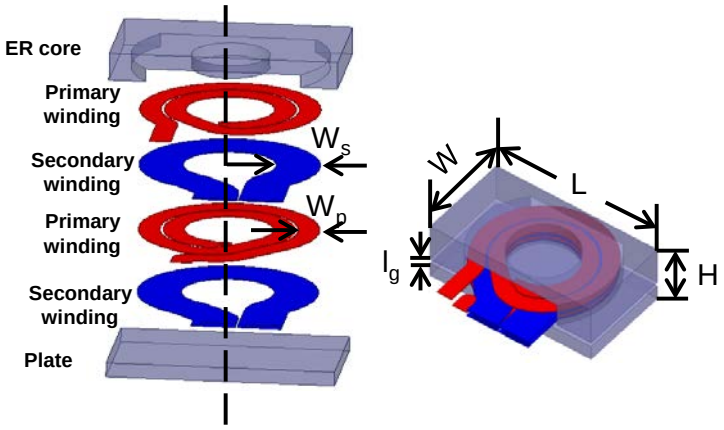


Figure 3.9. Exploded view of planar coupled inductors with four-layer winding structure.

3.4.2 Selecting Magnetic Core Size

The current ripple is relatively high compared to the dc current, and the value of H_{dc} is less than 5% of the saturated field strength in this application. According to the measurements of the core loss for various magnetic materials [7], [14]–[16], the change in the core loss is within 10% with a small H_{dc}. It is reasonable to assume that $K(H_{dc})$ is one. The coupled inductors were designed at full load, and the duty cycle range for the converter is near 50% in this application. Equation (3.5) can be further simplified to calculate the core loss by eliminating the core loss factor γ:

$$P_{core} = \frac{8}{\pi^2} K_{fe} f^{\alpha} B_{ac}^{\beta} \cdot V_e = P_v \cdot V_e. \tag{3.22}$$

The currents of the coupled inductors are shown in Figure 3.8(b). For a triangular magnetizing current with a dc offset, the rms value of the current waveforms can be given by

$$I_{Lmrms} = \sqrt{\left(\frac{nI_{2dc}}{D'}\right)^2 + \frac{1}{12}\left(\frac{V_{in}D}{L_m f}\right)^2}, \tag{3.23}$$

$$I_{1rms} = \sqrt{D} I_{Lmrms}, \tag{3.24}$$

$$I_{2rms} = n\sqrt{D'} I_{Lmrms} \tag{3.25}$$

where V_{in}, I_{2dc}, and D are defined in Figure 3.8(b), $n = n_1/n_2$, and $D' = 1 - D$. By combining (3.12) and (3.13), α_1 and α_2 can be expressed as

$$\alpha_1 = \frac{\sqrt{D}}{\sqrt{D} + \sqrt{D'}}, \tag{3.26}$$

$$\alpha_2 = \frac{\sqrt{D'}}{\sqrt{D} + \sqrt{D'}}. \tag{3.27}$$

By plugging (3.22) - (3.27) into (3.17), the coefficient of total loss K_w is found to be equal to

$$K_w = \left\{ \left[\sqrt{D}\left(D + F_{R1}D'\right) + \sqrt{D'}\left(D' + F_{R2}D\right)\right]\left(\frac{I_{2dc}}{nD'}\right)^2 + \frac{F_{R1}\sqrt{D} + F_{R2}\sqrt{D'}}{12}\left(\frac{V_{in}D}{L_m f}\right)^2 \right\} \cdot \frac{\rho}{K_\mu}\left(\frac{V_{in}D}{2B_{ac} f}\right)^2 \left(\sqrt{D} + \sqrt{D'}\right), \tag{3.28}$$

The fill factor K_u of the planar inductor is set to 0.11, and $F_{Ri}(1)$ is initially assumed to be one. Equation (3.17) and (3.18) are solved by sweeping the flux density B_{ac} within the range of 10 to 50 mT. The first line in Figure 3.10 represents the relationship between the total magnetic loss and the core volume after the first pass.

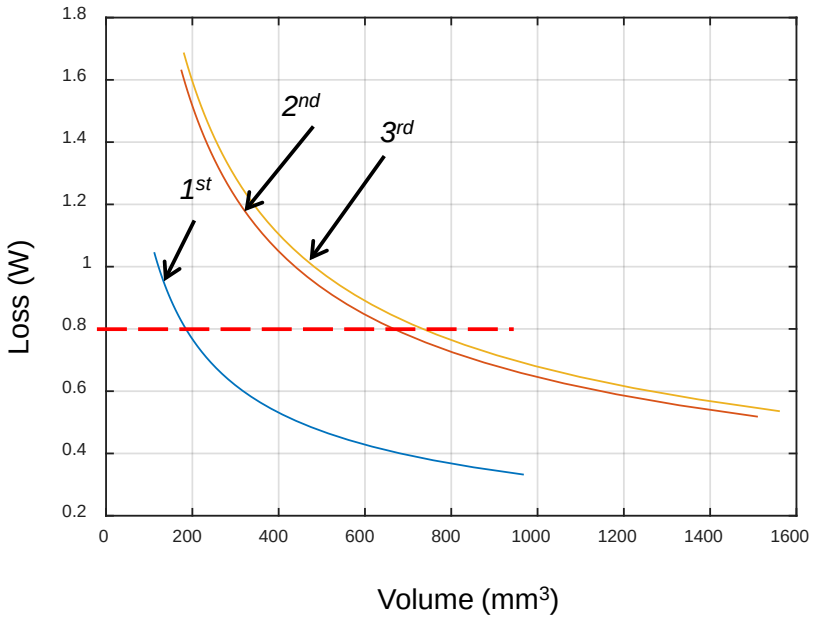


Figure 3.10. Total loss P_{total} as a function of volume V_e using the specifications shown in Table 3.2 for $F_{Ri}(1)$, $F_{Ri}(2)$, and $F_{Ri}(3)$.

With the total loss limitation of 0.8-*W*, the volume V_e was calculated as 180 mm^3. After referring to the table of available EI cores, EI11 ($V_e(1)$ = 180 mm^3) was selected, with the parameters L = 11 mm, W = 6 mm, A_c = 11.9 mm^2, W_A = 1.4 mm^2, and MLT = 13.35 mm[10]. The ac flux density is calculated as 45mT. The number of turns on the primary side can be obtained as

$$n_1 = \frac{\lambda}{2B_{ac}A_c} = \frac{V_{in}D}{2B_{ac}A_c f} = \frac{48 \times 0.45}{2 \times 0.045 \times 11.9 \times 10^{-6} \times 5 \times 10^6} \approx 4. \qquad (3.29)$$

As the turns ratios is four, the number of turns on the secondary side n_2 is one. The air gap is determined to be 0.18 mm by equations (3.1) and (3.2) to achieve a 0.85μH inductance with a relative permeability of 80. To fully use the window area to reduce the winding loss, an interleaved four-layer PCB winding is used with 2 oz. copper having a width of 0.8 mm on the primary winding and 1.725 mm on the secondary-side winding. The dc resistance is determined

to be 28.5mΩ on the primary side and 1.8mΩ for the secondary winding by simulating the system in ANSYS Maxwell with the winding structure shown in Figure 3.9. Excited by the triangular-shaped winding current shown in Figure 3.8(b), with I_{1rms} = 1.55 A, I_{2rms} = 6.22 A, I_{1dc} = 0.61 A, and I_{2dc} = 2.53 A, the winding loss can be obtained as 0.211W on the primary side and 0.232 W on the secondary side (see Figure 3.11).

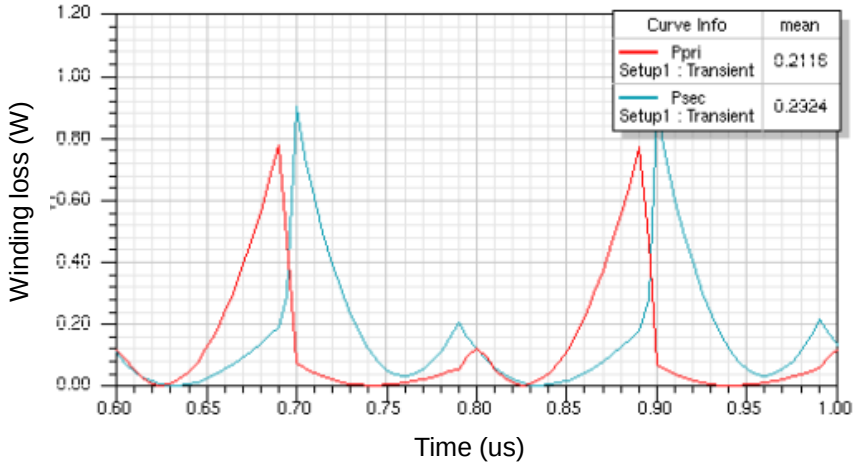


Figure 3.11. Instantaneous winding loss of the coupled inductors with the EI11 core shown in Figure 3.9 and the parameters listed in the second column of Table 3.4.

Solving (3.7) and (3.8) yields the ac resistances:

$$R_{1ac} = \frac{P_{1winding} - P_{1winding\_dc}}{I_{1rms}^2 - I_{1dc}^2} = \frac{0.211 - 0.61^2 \times 0.028}{1.55^2 - 0.61^2} = 120.7\ m\Omega, \tag{3.30}$$

$$R_{2ac} = \frac{P_{2winding} - P_{2winding\_dc}}{I_{2rms}^2 - I_{2dc}^2} = \frac{0.232 - 2.53^2 \times 0.0018}{6.22^2 - 2.53^2} = 8.5\ m\Omega. \tag{3.31}$$

The ratio of the ac resistance to the dc resistance, $F_{Ri}(2)$, can be calculated as

$$\mathrm{F}_{R1}(2) = \frac{R_{1ac}}{R_{1dc}} = \frac{120.7}{28.5} = 4.23, \tag{3.32}$$

$$\mathrm{F}_{R2}(2) = \frac{R_{2ac}}{R_{2dc}} = \frac{8.5}{1.8} = 4.74. \tag{3.33}$$

The results of the first pass with the initial $F_{Ri}(1)$ are given in the second column of Table 3.4. By repeating the design procedure with the updated $F_{Ri}(2)$, another curve of P_{total} versus $\mathrm{V_e}$ is plottedas shown in Figure 3.10. Similarly, volume V_e is calculated as 638 mm^3, which is within the total loss requirements. After checking the family of available EI cores, a larger size of EI 18 is selected as F_{Ri} increases. Additional iterations are required until the volumes derived by different loops are identical. The loop is ended when the $V_e(3)$ value selected from the third pass is equal to the value of $V_e(2)$, as shown in the 2nd Pass and 3rd Pass columns of Table 3.4.

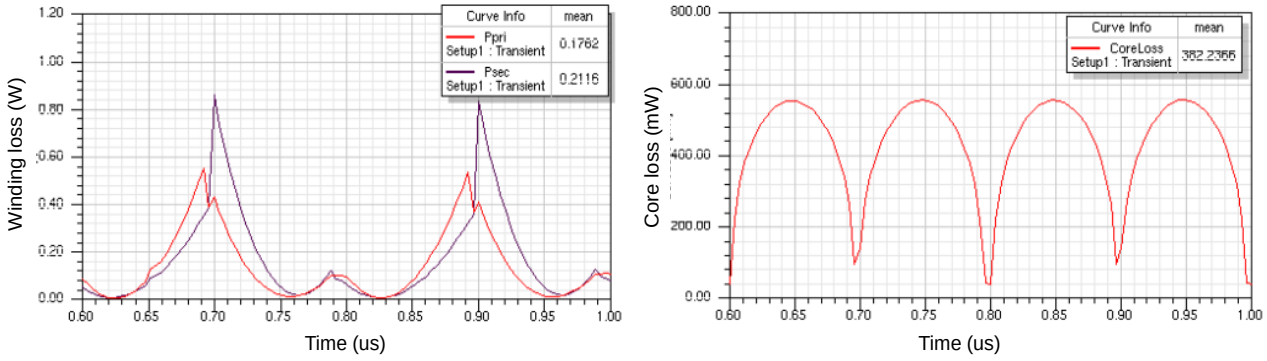
Table 3.4 Design procedure for coupled inductors at 5 MHz

Parameter	**1st pass**	**2nd pass**	**3rd pass**
$F_{R1}(i)$	1	4.2	4.8
$F_{R2}(i)$	1	4.7	5.2
V_e (mm^3)	180	638	709
Core size $V_e(i)$ (mm^3)	150 (EI11)	604 (EI 18)	604 (EI 18)
L (mm)	11	18	18
W (mm)	6	9.7	9.7
A_c (mm^2)	11.9	30.2	30.2
B_{ac} (mT)	45	18	18
n_1	4	4	4
n_2	1	1	1
W_p (mm)	1.36	1.7	1.7
W_s (mm)	2.8	3.5	3.5
l_g(mm)	0.12	0.51	0.51

Parameter	1st pass	2nd pass	3rd pass
R_{1dc} (mΩ)	28.5	21	21
R_{2dc} (mΩ)	1.8	1.5	1.5
R_{1ac} (mΩ)	120.7	101	101
R_{2ac} (mΩ)	8.5	7.8	7.8
$F_{R1}(i+1)$	4.2	4.8	4.8
$F_{R2}(i+1)$	4.7	5.2	5.2

Note: W_p and W_s are the widths of the windings defined in Figure 3.9.

Compared to the A_p and K_g methods, the K_{gac} method is more straightforward, as it does not need to consider the arbitrary variables J and B_{max} in the first pass. The temperature rise of the coupled inductors is checked in the end. The simulation results provide a winding loss of the finalized core structure of 0.39 W, as shown in Figure 3.12(a). As the characteristic curve of the core loss density for the 4F1 material is imported into ANSYS Maxwell, the total core loss is found to be 0.38 W by taking the average of the instantaneous core loss in one cycle, as shown in Figure 3.12(b). The total loss is 0.77 W, which is around 2.6% of the maximum output power.



(a) (b)

Figure 3.12. (a) Instantaneous winding loss and (b) Instantaneous core loss of the coupled inductors with the EI 18 core and the parameters listed in the 3rd Pass column of Table 3.4.

3.4.3 Optimization of Winding Structure

Two-layer and four-layer winding structures are evaluated by simulating in ANSYS Maxwell and HFSS to optimize the leakage inductance, winding loss, and parasitic capacitance.

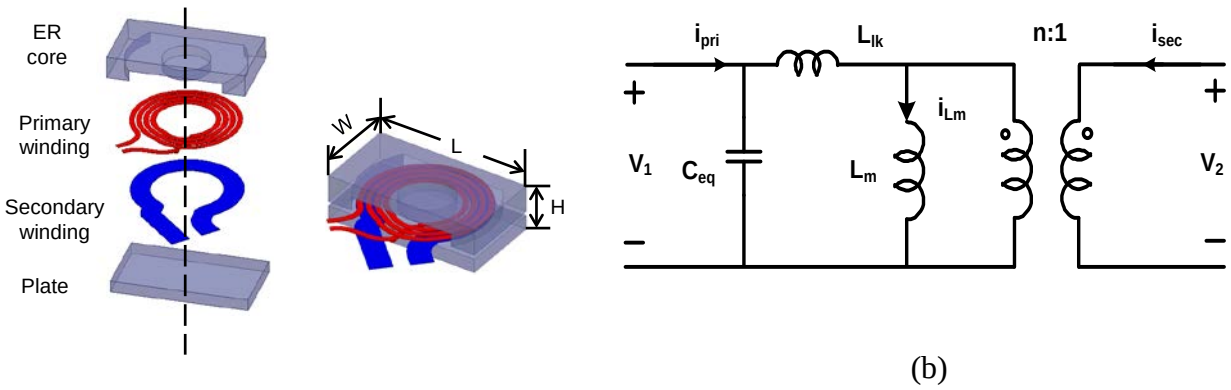


Figure 3.13. Coupled inductors with (a) Exploded view of two-layer winding and (b) The inductors' equivalent circuit.

Figure 3.13(a) shows the two-layer winding structure. The copper width is 0.635 mm on the primary side and 2.54 mm on the secondary. Figure 3.13(b) shows the equivalent circuit model of the coupled inductor. The magnetizing inductance L_m is obtained by

$$L_m = nL_{12}, \tag{3.34}$$

where L_{12} is the mutual inductance. The leakage inductance can be calculated by

$$L_{lk} = L_{11} + n^2 L_{22} - 2nL_{12}, \tag{3.35}$$

where L_{11} is the self-inductance on the primary side and L_{22} is the self-inductance on the secondary side. The coupling coefficient could be derived as

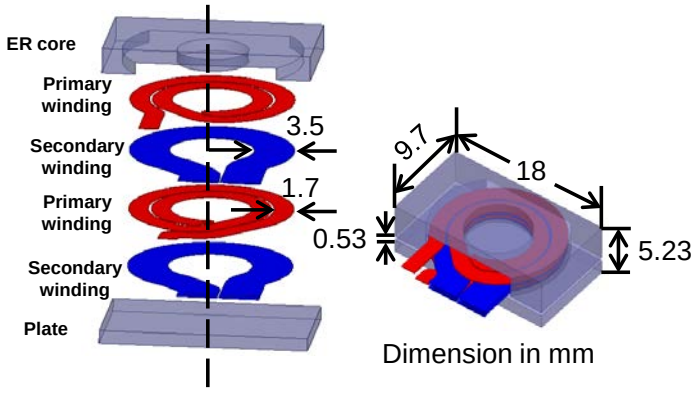
$$k = \frac{L_{12}}{\sqrt{L_{11}L_{22}}}. \tag{3.36}$$

From finite-element simulation, the impedance matrix can be derived as

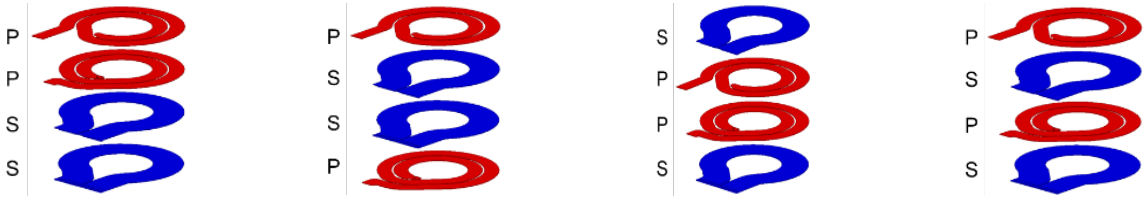
$$\begin{bmatrix} L_{11} & L_{21} \\ L_{12} & L_{22} \end{bmatrix} = \begin{bmatrix} 876.1\,nH & 211.3\,nH \\ 211.3\,nH & 60.38\,nH \end{bmatrix}. \tag{3.37}$$

The self-inductance is L_{11} = 876.1nH on the primary side and L_{22} = 60.38nH on the secondary side. The total leakage inductance is calculated as 151.8nH, and the coupling coefficient is 91.9%.

In order to further decrease the leakage inductance, the four-layer winding structures shown in Figure 3.14 are evaluated. Using P to stand for the primary winding and S to stand for the secondary winding, the interleaving arrangements are PPSS, PSSP, SPPS, and PSPS.



(a)



(b) (c) (d) (e)

Figure 3.14. Four-layer planar coupled inductors with different winding arrangements (a) Exploded view of four-layer coupled inductors (b) PPSS (c) PSSP (d) SPPS(e) PSPS.

The leakage inductance of the four-layer structures can also be obtained from (3.35). To evaluate the winding loss by finite-element simulation in ANSYS Maxwell, the primary winding was excited by current i_{SW} with 0.73-A dc and 1.65-A RMS current, and the secondary winding

was excited by the current i_{SR} with 2.52-A dc and 6-A RMS current. The winding loss of the PSPS structure was derived as 0.4 W. The winding loss of the other structures can be also obtained this way, and are shown in Table 3.5.

The fact that there is self-capacitance means the lumped capacitance is paralleled on the primary winding, while the secondary side is an open circuit. The values of the capacitances can be simulated by ANSYS HFSS, and are shown in Table 3.5.

Table 3.5 Comparison of different winding arrangements

	Two-layer	**PPSS**	**PSSP**	**SPPS**	**PSPS**
Leakage inductance (nH)	151.80	73.00	49.74	45.83	41.61
Coupling coefficient	0.92	0.96	0.97	0.97	0.98
Self-capacitance (pF)	3.83	16.39	10.35	20.78	12.95
Total winding losses (W)	0.68	0.43	0.39	0.39	0.38

The interleaved PSPS, PSSP and SPPS coupled inductors are much better than the non-interleaved structures for the leakage inductance and winding losses. The coupling coefficient for these interleaved structures is up to 98%, which is 6% larger than the two-layer geometry. The winding losses are also reduced by 41% compared to the two-layer structure. The primary self-capacitance of the four-layer structure is three times larger than that of the two-layer structure because its value mainly depends on the area and distance between two coils. The value of the inductance is only 10% of the output capacitance of the switches, which has a relatively minor influence on soft-switching operation. Considering the better coupling and low winding loss, the PSPS structure shown in Figure 3.14(a) is selected for the coupled inductors.

3.5 Experimental Verification

3.5.1 Core Loss Measurement Under Rectangular Voltage Excitation

An inductive cancellation method [17] is used to evaluate the core loss of the inductor or coupled inductors under a real rectangular waveform. Figure 3.15 shows the equivalent circuit of the inductive cancellation method, which includes a power amplifier driven by an arbitrary signal from the function generator, a sensing resistor, a tested magnetic core, and a reference air core transformer with a 1:1 turns ratio.

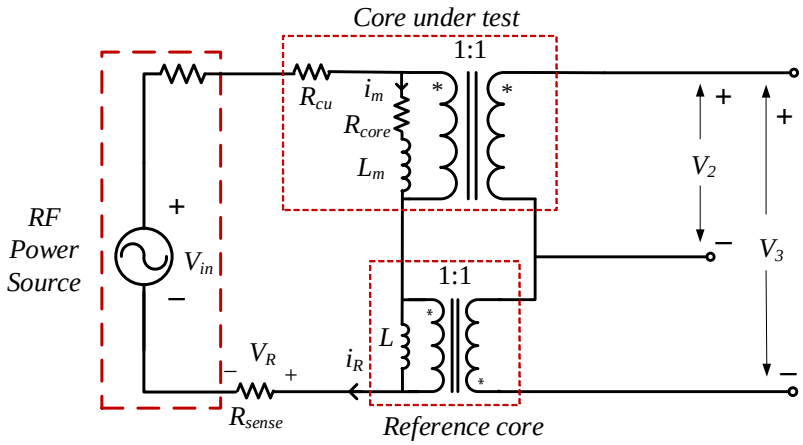


Figure 3.15. Equivalent circuit of inductive cancellation method for core loss measurement.

The inductor is modeled as nonlinear core loss resistor R_{core} in series with magnetizing inductor L_{m}. The polarity of the reference transformer is changed, so V_3 is equal to

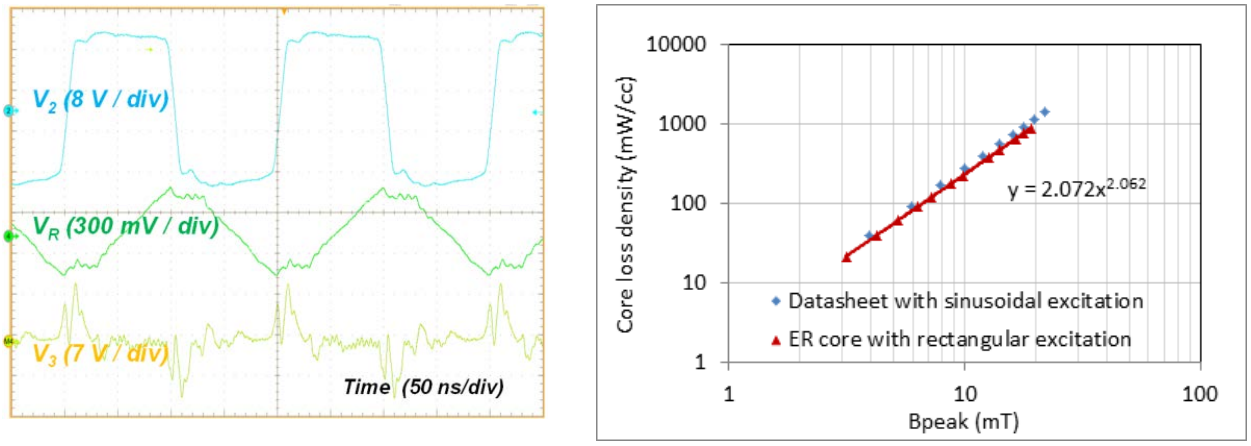
$$V_3 = (R_{core} + j\omega L_m - j\omega L) i_m. \tag{3.38}$$

If L and L_{m} are identical, the voltage on the magnetizing inductor will be cancelled out for any frequency, and V_3 will be equal to the voltage on the equivalent core loss resistor, which is in phase with V_{R}. The core loss can be calculated by integrating the product of V_3 and V_{R},

$$P_{core} = \frac{1}{TR_{sense}} \int_0^T V_3 V_R dt, \tag{3.39}$$

where T is the excitation period, and R_{sense} is the sensing resistance.

The core loss of NiZn ferrite 4F1 was measured under rectangular voltage excitation using an ER 18 core at room temperature. An air core transformer with an inductance of 1.2 μH, which is identical to the magnetizing inductance of the core under test, was wound to cancel the reactive power. A 0.5 Ω resistance was selected to sense the transformer current.



(a) (b)

Figure 3.16. (a) Measurement waveforms with ER-shaped core under rectangular voltage excitation and (b) Core loss density of NiZn 4F1 material at 5 MHz and a 50% duty cycle.

The measured waveforms of V_2, V_3, and V_R are shown in Figure 3.16(a) with a 50% duty cycle and 5-mT peak flux density. The loss of the ER-shaped core at 5 MHz and a 50% duty cycle is approximately 85.5% of the value on the datasheet for a sinusoidal excitation, as shown in Figure 3.16(b), which can be calculated as

$$P_{core} = 2.07 \times B_{ac}^{2.06} V_e. \tag{3.40}$$

3.5.2 Test Results of Coupled Inductors in 5-MHz Converter

A 5-MHz power converter was built with the dimensions of 25 mm × 24 mm × 5.2 mm for the power stage shown in Figure 3.17(a). The ER core, with an area of 18 mm × 10 mm, occupies 30% of the power stage. An EPC 2012 eGaN FET (200 V) was selected to be the input switch, an EPC 2001 eGaN FET (100 V) was the synchronous rectifier, and the LM5114 was used to drive the eGaN FETs.

The peak efficiency was 90.6% with an input voltage of 48 V and output voltage regulated as 12 V constantly at 5 MHz. The temperature was 50 °C in the core and 53 °C in the windings under full load with natural air cooling conditions, as shown in Figure 3.17(b).

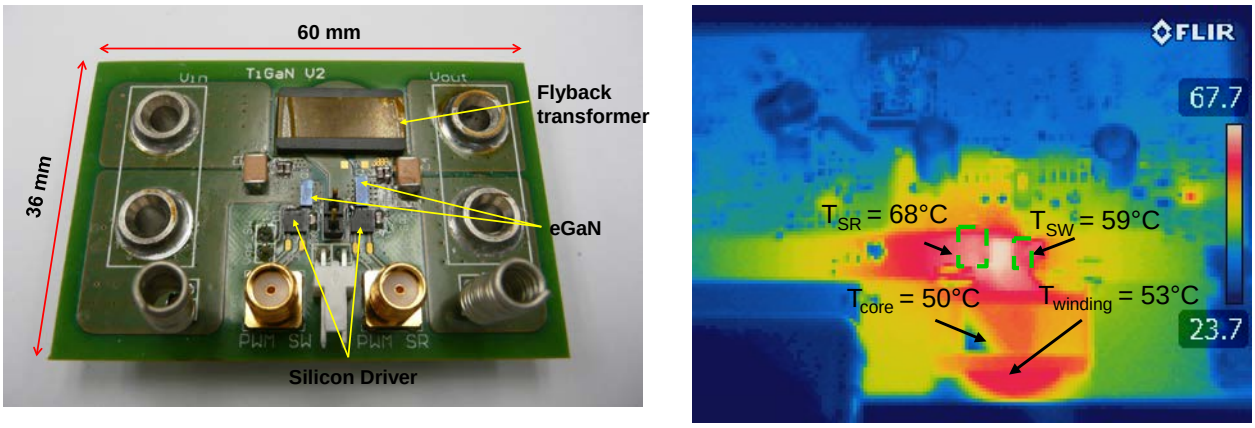
The total loss of the coupled inductors can be estimated from (3.19) as

$$P_{total} = 13.8 \times e^{\frac{ln(53-24)}{0.833}} = 0.786\, W, \tag{3.41}$$

where the area for heat dissipation is 13.8 cm^2, including the surface area of the ER core and PCB winding. Because of the abundant thermal vias and grounding copper on the PCB, the estimated area for heat dissipation is lower than the actual area. The core loss can be derived using (3.40) as

$$P_{core} = 2.07 \cdot 16.7^{2.06} \times 6.04 \times 10^{-4} = 0.41\, W \tag{3.42}$$

where B_{ac} is calculated as 16.7 mT and the core volume of EI 18 is 604 mm^3. The winding loss is approximately 0.37 W, which is consistent with the simulation results presented in Figure 3.12.



(a) (b)

Figure 3.17. (a) Test board of power converter with the specifications shown in Table 3.2 and (b) Temperature distribution at V_{in} = 48 V, P_o = 30 W, and f = 5 MHz with natural air cooling.

3.6 Investigation of Power Density for Flyback Converter

Since the coupled inductor occupies approximately 30% of the printed circuit board, it is critical to increase the overall power density of the flyback converter by reducing the magnetic core size. A typical method for reducing the volume involves increasing the switching frequency and operating the converter in critical-conduction mode or resonant mode to minimize switching loss and noise. The relationships between the size of magnetic core and the frequency, loss and temperature of the inductor are investigated in this section.

The influence of frequency on core size in a QSW flyback converter is demonstrated by designing the converter to operate at different frequencies. To select the minimum core size, first the value of the inductance and the volt-second on the coupled inductor need to be found at a given frequency. Using the state model in Chapter 2, the magnetizing inductance of the flyback transformer is designed for the worst case when the minimum input voltage is 36V and the full load of the output current is 2.5A to achieve ZVS for the entire operation range. The inductance

of the coupled inductor for QSW flyback is shown in Figure 3.18. The duty cycle is calculated and shown in Figure 3.18 at a nominal input voltage of 48V and 30W output power. The effective duty cycle becomes smaller because the resonant interval cannot be neglected at high frequencies.

The magnetic materials are selected on the basis of their performance factor at a given frequency, which is provided by some of the magnetics manufacturers. One example from Ferroxcube is shown in Figure 3.19. For different materials under the same core loss density P_v of 500mW/cm^3 at a given frequency, the smaller core can be used as the product of the frequency and maximum ac flux density increases. In other words, the core loss is smaller with the identical core size at higher frequencies.

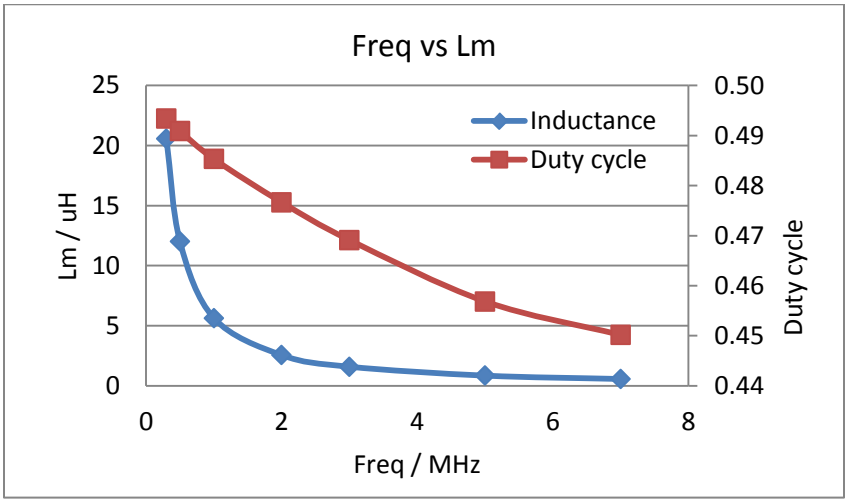


Figure 3.18. Inductance of coupled inductors for QSW flyback converter at different frequencies and duty cycles of the primary switch at V_{in}=48V, V_o=12V, I_o=2.5A.

The 3C96 has the best performance factor at 300kHz among the materials form Ferroxcube. 3F45 is the preferred material at 1MHz. As the frequency increases, the eddy-current loss in the

core also becomes significant. Material 3F5 is preferred at 3MHz and 4F1 at 5MHz. Table 3.6 shows the permeability and Steinmetz coefficients of different materials at certain frequencies.

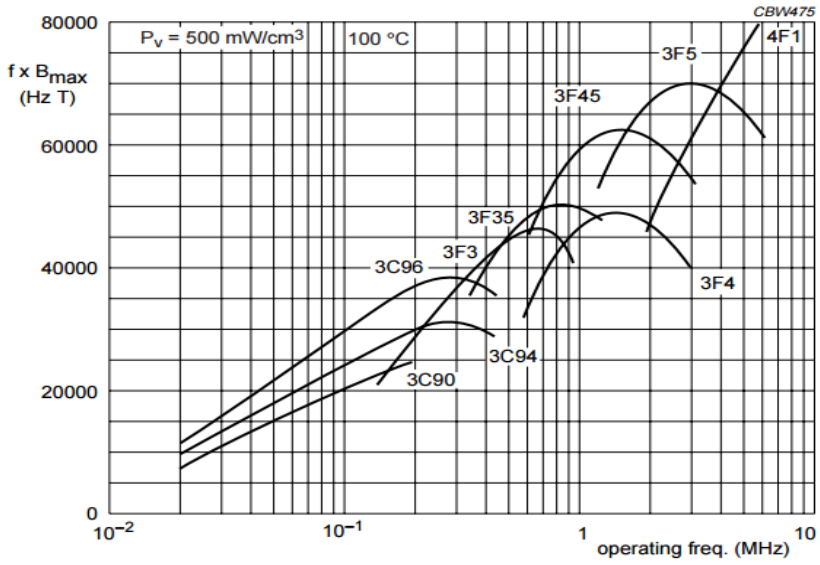


Figure 3.19. Performance factor at P_v=500mW/cc as a function of frequency for power ferrite materials [11].

Table 3.6 The permeability and Steinmetz coefficients of different materials at a given frequency

Freq (MHz)	**Material**	**Permeability**	**Kfe (kW/($m^3Hz^{\alpha}T^{\beta}$))**	**Beta**
0.3	3C96	2000	142939.6	2.522
1	3F45	900	802711	2.639
3	3F5	650	1242875	2.056
5	4F1	80	3827840	2.066

Following the design example in the previous section, the EI shaped core shown in Figure 3.9 is chosen for its better utilization of the window area. By simulating the ac winding loss of each design in ANSYS Maxwell, the ratio of ac resistance to dc resistance can be derived; the

design curves are plotted at each frequency, as shown in Figure 3.20, and these curves are used to determine the minimum core size within a 0.8W total magnetic loss budget. The Matlab file attached in the Appendix B illustrates the detailed iteration process.

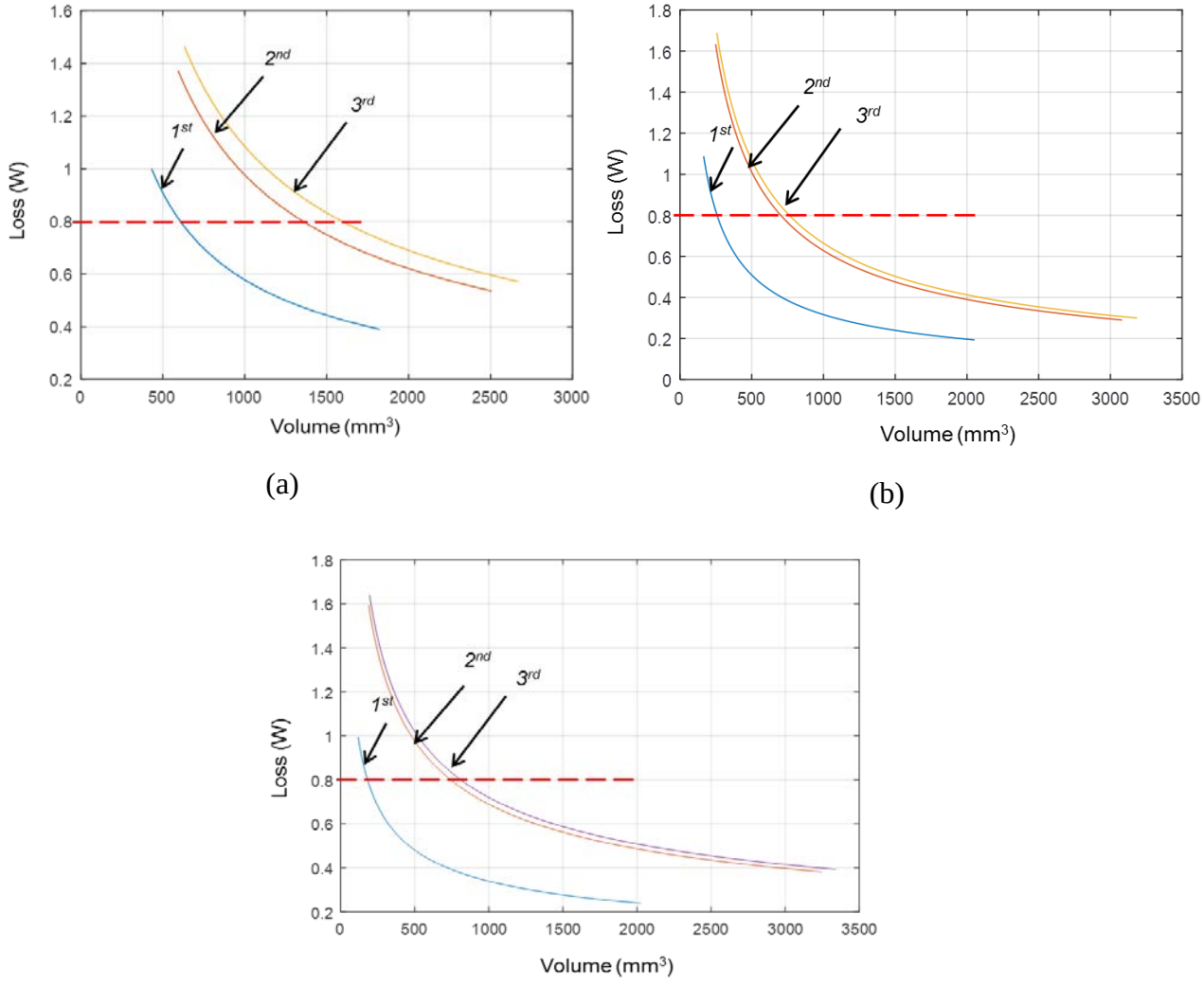
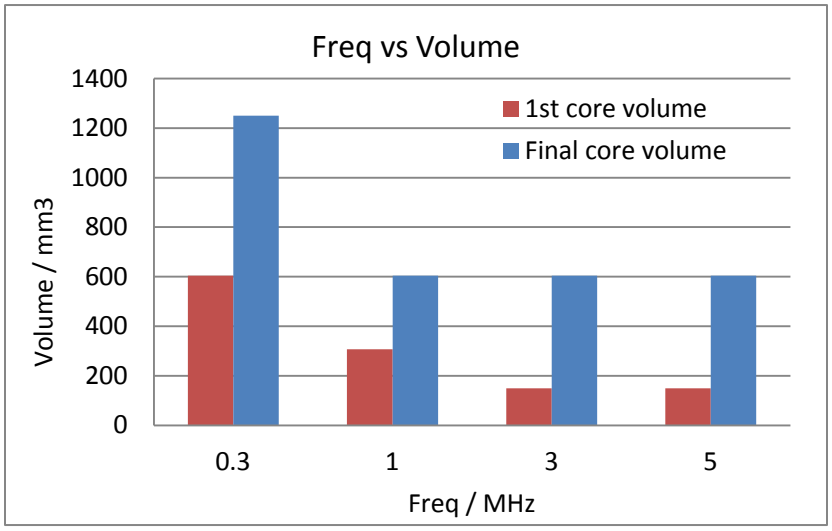


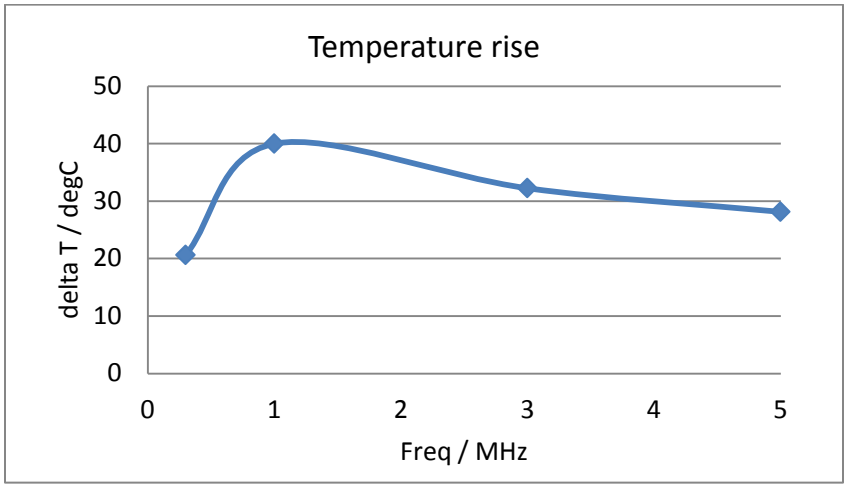
Figure 3.20. Total loss P_{total} as a function of volume V_e for $F_{Ri}(1)$, $F_{Ri}(2)$, and $F_{Ri}(3)$ at (a) 0.3MHz, (b) 1MHz and (c) 3MHz.

After the iterative process, EI23 is selected for use at 0.3MHz, and EI18 is chosen for 1MHz, 3MHz and 5MHz, as shown in Figure 3.21(a). The core loss and winding loss can be obtained by

FEA simulations with the designed core sizes, and the predicted temperature rise of each inductor is calculated by (3.21), as shown in Figure 3.21(b). The core volume cannot be further reduced even as the switching frequency increases, which is mainly restricted by the eddy effect on core loss at very high frequencies.



(a)



(b)

Figure 3.21. (a) Designed core volumes at different switching frequencies and (b) The predicted temperature rise at each frequency.

The design trade-off among core volume, magnetic loss and temperature rise for the inductor used at 5MHz can be predicted, and is illustrated in Figure 3.22. The temperature of the

EI18 core will increase approximately by 28 ºC with natural air cooling. To further increase the power density of the converter, the EI 14.5 can be used with more layers of PCB windings to dissipate the extra heat.

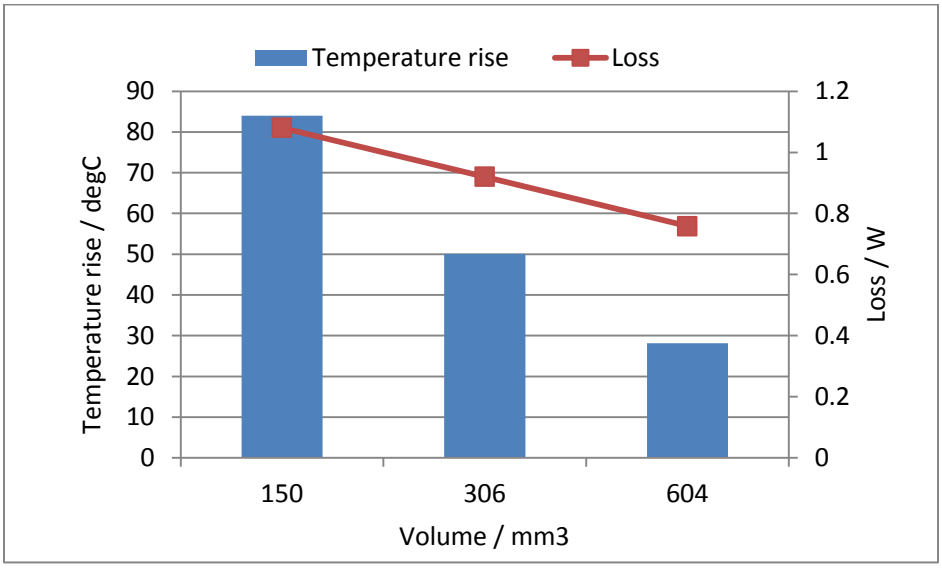


Figure 3.22. Design trade-off at 5MHz among core volume, temperature rise and magnetic loss.

3.7 Summary

A design methodology for selecting a minimum core volume for an inductor or coupled inductors with a significant ac flux swing was presented. The total loss is expressed as a direct function of the core volume based on the regression analysis of the geometric constant (K_{gac}). An iterative procedure is applied via finite-element simulation to find the minimal core size under the loss constraint. A design example of planar coupled inductors in a 5-MHz power converter illustrated the design procedure in great detail. The core loss was measured under rectangular excitation, and the winding loss was obtained from thermal measurement results.

By deriving the rms current in the windings, the design procedure is also applicable for other inductors with a large flux swing, such as a buck converter under critical mode operation. The

K_{gac} method is more effective for ferrite materials rather than powder iron cores with discrete relative permeability, as the inductance can be adjusted continuously by the air gap when the given number of turns is determined by the ac flux density.

By designing the converter to operate at different frequencies, the relationships between the size of magnetic core and the frequency, loss and temperature of the inductor are studied. To further improve the power density of the converter, a better cooling method is required to dissipate the extra heat for a smaller transformer.

3.8 Reference

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Chapter 4 Small-Signal Model of Quasi-Square-Wave Converter

Switching a converter at very high frequencies—even to the multi-megahertz range—can increase the closed-loop bandwidth and significantly improve the transient performance. However, using the conventional small-signal model of continuous conduction mode for quasi-square-wave converters introduces a huge mismatch for the placement of the dominant poles when compared to the experiment results. The double poles in high-frequency QSW converters are split widely, which cannot be predicted by the conventional model. This chapter introduces a modified small-signal model of the QSW converter to explain the double-pole splitting phenomenon and to analytically quantify the damping effect. The impacts of deadtime, input voltage and output power on control-to-output transfer function are also investigated in detail. The closed-loop bandwidth can be pushed much higher with this modified model, and the transient performance is significantly improved.

4.1 Introduction

To prevent both switches of the QSW converter from conducting simultaneously, i.e., shoot-through, a dead-time interval (i.e. a time interval when neither switch is on) is inserted between their gate drive signals. Both switches are off during the dead-time interval, and the magnetizing inductor resonates with the output capacitance of the switches to charge and discharge the energy stored in the capacitor. The current flows through the switch body diodes, or the switch conducts in reverse for eGaN FETs after the resonant interval. The driver deadtime will reduce the conversion efficiency of the converter because of the higher voltage drop across the body diode and eGaN FETs.

In addition to its impact on efficiency, a driver's deadtime or resonant interval also influences the damping of the transfer function for the power stage. The time interval that the inductor resonates with the output capacitance of the switches cannot be neglected in quasi-square-wave converter at high switching frequencies. The traditional small signal model in [1], [2] cannot predict the transfer function in quasi-square-wave mode operation, because the rising time and falling time of PWM switch are negligible for both continuous-conduction mode and discontinuous-conduction mode. There is no small-signal equivalent circuit of CRM or QSW converter, so the design of compensator can only depends on simulation [3], [4]. The circuit averaging method was adopted in [5] to obtain the small-signal model in critical load condition for a buck converter, but the control-to-output transfer function is not obtained analytically.

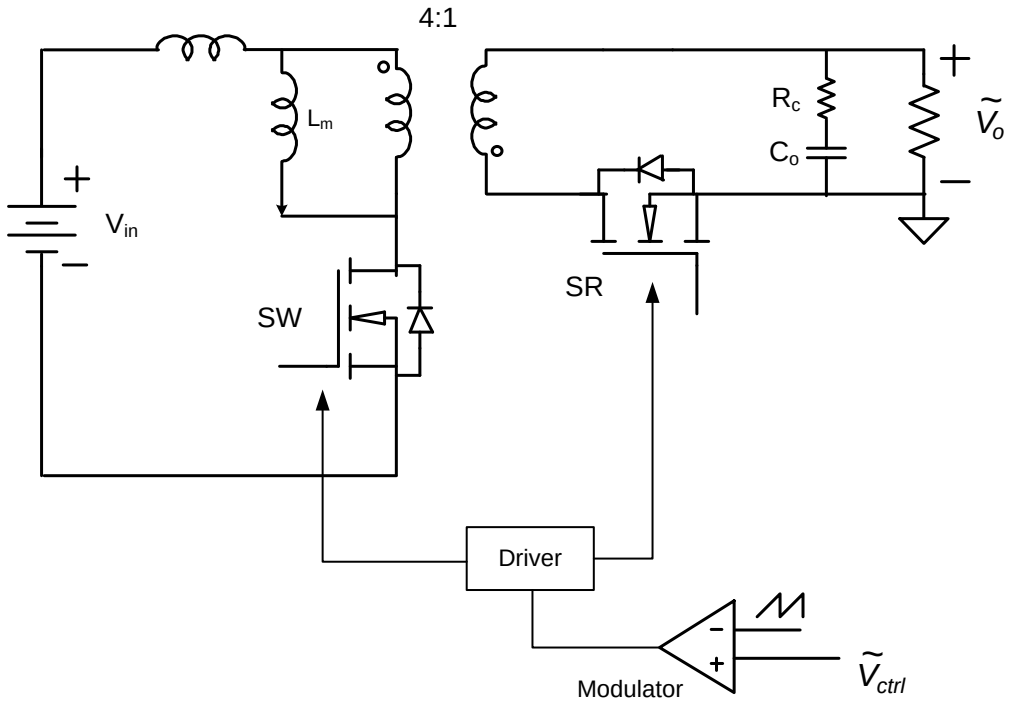


Figure 4.1. Power stage of QSW flyback converter to derive the control-to-output transfer function.

A voltage-mode-control QSW flyback converter illustrated in Figure 4.1 is used to evaluate the control-to-output transfer function. The specifications of the QSW converter are listed in Table 2.4. The timing of the converter can be calculated using the charge-based model introduced in Chapter 2.

Table 4.1 The specifications of QSW flyback converter

Input voltage	**Switching frequency**	**Output voltage**	**Output power**
36 V-72 V	5 MHz	12 V	0-30 W

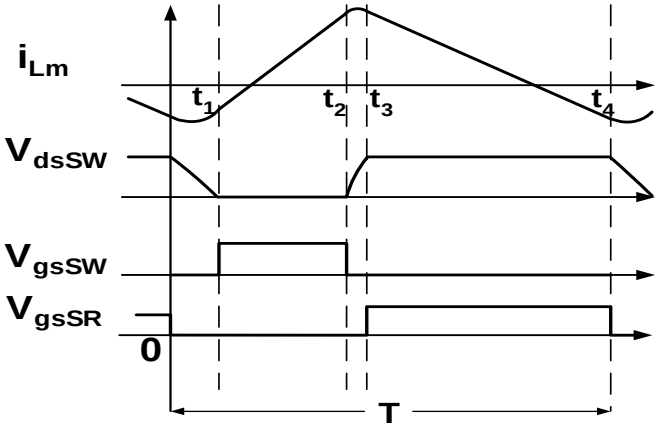


Figure 4.2. Typical steady-state waveforms for ZVS QSW flyback converter.

The typical steady-state waveforms shown in Figure 4.2 indicate that the inductor current is operated in continuous conduction mode (CCM). The small-signal model calculated by the CCM model is shown in Figure 4.3. The double-pole splitting phenomenon cannot be predicted by the conventional CCM model as shown in the simulation results in Simplis. The decades of degree phase error also prevents the system from operating at a higher bandwidth.

A QSW small-signal model is introduced to improve upon the conventional model by quantifying the damping effect resulting from the resonant interval. The following sections provide a detailed derivation of the analytical expression of the damping resistor, and an analysis of the impacts of the deadtime, input voltage and output power on the power stage control-to-output transfer function. A 5-MHz quasi-square-wave flyback converter was fabricated to validate theoretical analysis, and the dynamic performance is improved significantly with an accurate small-signal model.

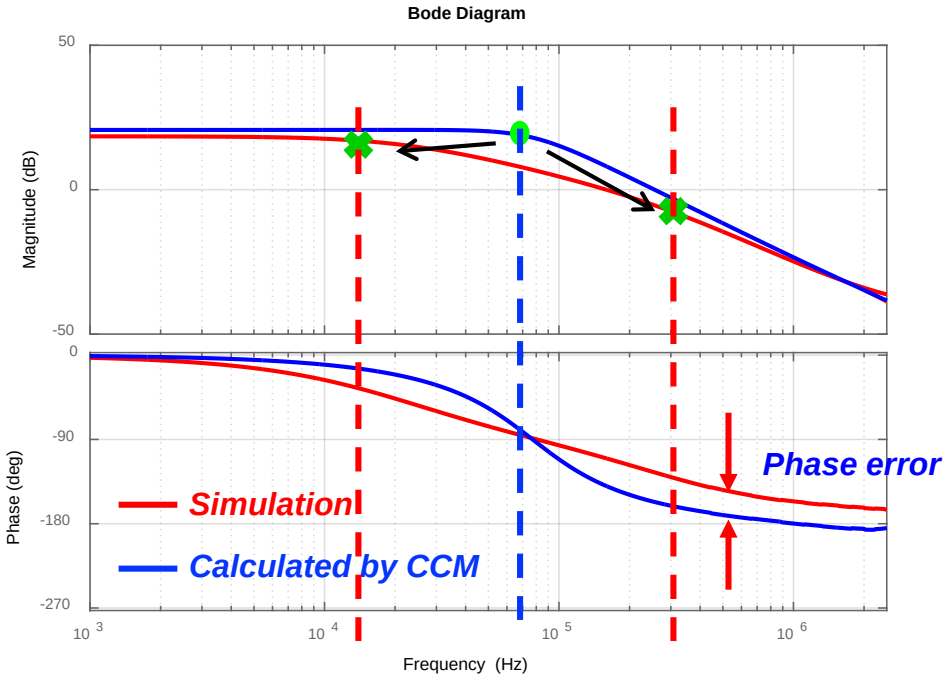
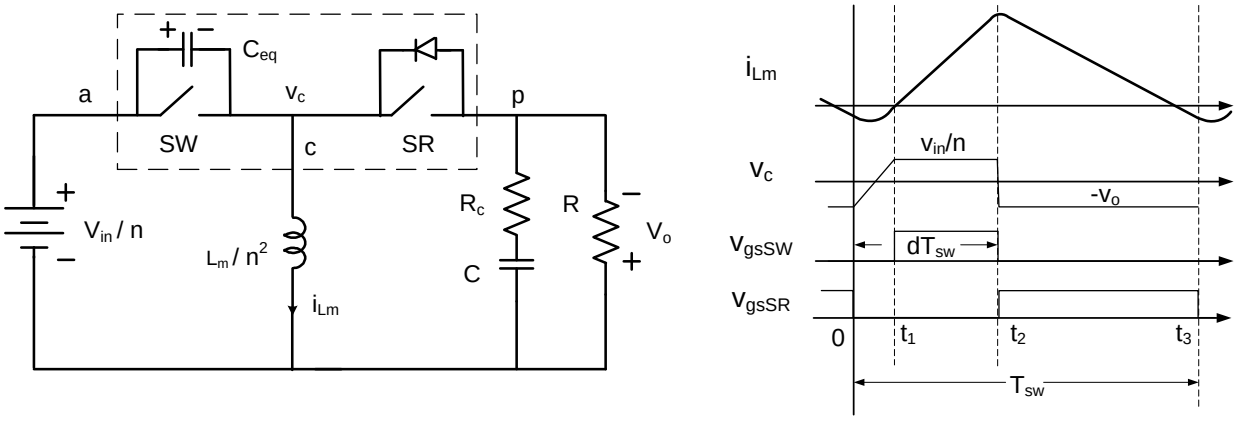


Figure 4.3. Simulation and calculation results of the control-to-output transfer function of QSW flyback converter.

4.2 Derivation of Small-Signal Model of QSW Converter

4.2.1 Conventional Small-Signal Model of PWM Converter in Continuous Conduction Mode

The conventional small-signal CCM model is based on the PWM switch model. The flyback converter shown in Figure 4.1 is taken as an example, but the methods used here are also applicable for other PWM converters. To simplify the analysis, the components on the primary side of the flyback converter are transferred to the secondary side with respect to the turns ratio, which is equivalent to the buck-boost converter in Figure 4.4(a) and the typical waveforms in Figure 4.4(b). The leakage inductance is in series with magnetizing inductance. Since the coupling of transformer is easily greater than 97% in practice, the leakage inductance is negligible. The functional block represents the total nonlinearity in these converters, and is shown as a three-terminal nonlinear device in Figure 4.5. The terminal designations a, p, and c refer to active, passive, and common, respectively.



(a) (b)

Figure 4.4. (a) Schematic of QSW buck-boost converter and (b) Typical waveforms..

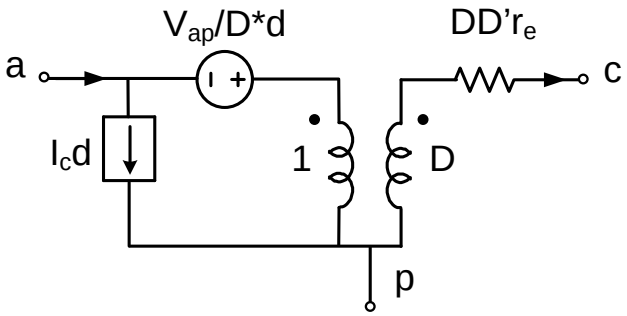


Figure 4.5. Equivalent small-signal model of the PWM switch.

In general, r_e is a function of the ESR of the capacitor and the load resistor R, which is relatively small and can be neglected. To derive the control-to-output transfer function, the input voltage source is shortened to ground and, as shown in Figure 4.6, the PWM switch is replaced by the equivalent circuit model in Figure 4.5.

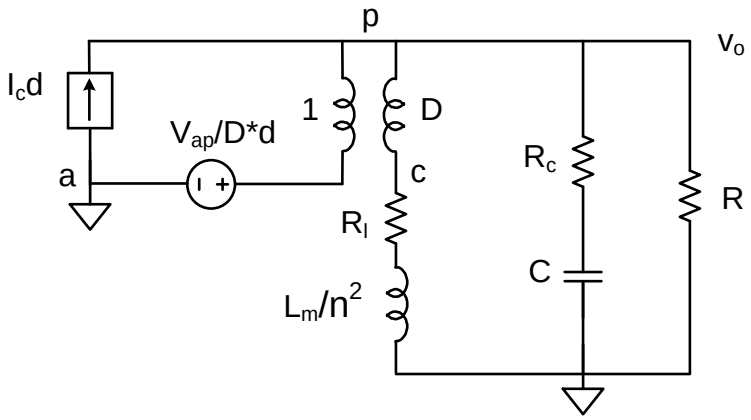


Figure 4.6. Small-signal model of buck-boost converter for the control-to-output transfer function.

The circuit-oriented control-to-output transfer function is

$$\frac{v_o}{d} = G_{do}\frac{(1+s/s_{z1})(1-s/s_{z2})}{1+s/\omega_0 Q+s^2/{\omega_0}^2} \tag{4.1}$$

where

$$G_{do} = \frac{V_{in}}{nD'^2} \tag{4.2}$$

$$s_{z1} = \frac{1}{R_c C} \tag{4.3}$$

$$s_{z2} = \frac{D'^2 R + R_l(D' - D)}{DL_m/n^2} \tag{4.4}$$

$$\omega_0 = \frac{n}{\sqrt{L_m C}} \sqrt{\frac{D'^2 + R_l/R}{1 + R_c/R}} \tag{4.5}$$

$$Q = \frac{1}{\omega_0} \frac{1}{\frac{L_m}{n^2(R_l + D'^2 R)} + C[R_c + R \parallel (\frac{R_l}{D'^2})]}. \tag{4.6}$$

4.2.2 Conventional Small-Signal Model of PWM Converter in Discontinuous Conduction Mode

The DCM operation of PWM converters differs from CCM operation by an additional time interval in each switching cycle during which an inductor current or capacitor voltage is clamped to zero or a constant when there are multiple energy storage elements. The inductor current of DCM operation rises in the first interval when the switch is turned on, reaches a peak when the switch is to be turned off, and resets to zero or a constant at the end of the second interval. The duty ratio of the SW and the SR are denoted by d_1 and d_2, respectively (see in Figure 4.2):

$$d_1 = \frac{t_2 - t_1}{T_{sw}} \tag{4.7}$$

$$d_2 = \frac{t_3 - t_2}{T_{sw}} \tag{4.8}$$

It is worth noting that the second duty ratio d_2 in DCM is not independent, but is replaced by d_1 according to the duty-ratio constraint [2]. Using state-space average method, the averaging

model of magnetizing current i_{Lm} and output capacitor voltage v_{co} for buck-boost converter can be expressed as

$$\frac{d\bar{i}_{Lm}}{dt} = \frac{d_1(v_{in} + \overline{v}_{co})}{L_m} - \frac{2\bar{i}_{Lm}\overline{v}_{co}}{d_1 v_{in} T_{sw}} \tag{4.9}$$

$$\frac{d\overline{v}_{co}}{dt} = \frac{\bar{i}_{Lm}}{C} - \frac{{d_1}^2 T_{sw} v_{in}}{2L_m C} - \frac{\overline{v}_{co}}{RC} \tag{4.10}$$

With the small-signal perturbation and linearization, the small-signal model can be obtained using the above equations:

$$\frac{d}{dt}\begin{bmatrix}\hat{\imath}_{Lm} \\ \hat{v}_{co}\end{bmatrix} = A\begin{bmatrix}\hat{\imath}_{Lm} \\ \hat{v}_{co}\end{bmatrix} + B\begin{bmatrix}\hat{v}_{in} \\ d_1\end{bmatrix} \tag{4.11}$$

where

$$A = \begin{bmatrix} -\frac{2M}{D_1 T_{sw}} & -\frac{2M}{D_1 R T_{sw}} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{4.12}$$

$$B = \begin{bmatrix} \frac{n^2 D_1(2+M)}{L_m} & \frac{2n^2 V_{in}(1+M)}{L_m} \\ -\frac{n^2 {D_1}^2 T_{sw}}{2L_m C} & -\frac{n^2 D_1 V_{in} T_{sw}}{L_m C} \end{bmatrix} \tag{4.13}$$

where $M=nV_o/V_{in}$. The control-to-output transfer function is obtained as

$$\frac{v_o}{d} = G_{do}\frac{(1 + s/s_{z1})(1 - s/s_{z2})}{(1 + s/s_{p1})(1 + s/s_{p2})} \tag{4.14}$$

where

$$G_{do} = \frac{n^2 D_1 V_{in} T_{sw} R}{2L_m M} \tag{4.15}$$

$$s_{z1} = \frac{1}{R_c C} \tag{4.16}$$

$$s_{z2} = \frac{2}{D_1 T_{sw}} \tag{4.17}$$

$$s_{p1} = \frac{2M}{D_1 T_{sw}} \tag{4.18}$$

$$s_{p2} = \frac{2}{RC}. \tag{4.19}$$

4.2.3 Small-Signal Model of QSW Converter

The switch-node voltage Vc (seen in Figure 4.4) is assumed to either follow the PWM signal exactly without delay, or to follow with a constant delay under all conditions in the conventional small-signal model. The rising time and falling time of PWM switch are negligible for both continuous-conduction mode and discontinuous-conduction mode [1], [2]. Figure 4.2 shows that the switch-node voltage waveform Vc does not remain constant under different input or load conditions during interval [0, t_1] due to the deadtime. Therefore the influence of this resonant interval on the small-signal analysis needs to be investigated.

To simplify this investigation, the model uses the charge equivalent capacitance C_{eq} of SW and SR shown in Figure 4.4, since it is a good approximation for the capacitance nonlinearity according to the analysis in Chapter 2. In addition, the turn-off current for SW is much higher than the turn-off current for SR, which means the resonant interval needed to charge C_{eq} is much shorter and can be ignored. The circuit averaging method is adopted here to derive the small-signal model for the QSW converter.

The inductor resonates with equivalent capacitor C_{eq} during the interval [0, t_1] in Figure 4.2. The average voltage at phase node Vc in one switching cycle can be expressed by

$$v_c = -V_o cos\omega t - Zi_{Lm}(0) sin\omega t \tag{4.20}$$

where

$$\omega = \frac{n}{\sqrt{L_m C_{eq}}} \tag{4.21}$$

$$Z = \frac{1}{n}\sqrt{\frac{L_m}{C_{eq}}} \tag{4.22}$$

The initial inductor current $i_{Lm}(0)$ at time zero is close to the valley current, which can be derived as

$$i_{Lm}(0) = i_{Lm} - \frac{n^2 V_o (1-D) T_{sw}}{2L_m} \tag{4.23}$$

where i_{Lm} is the average inductor current. Integrating (4.20) over the course of one switching cycle yields the average phase node voltage as follows:

$$\begin{aligned} v_c &= \frac{1}{T_{sw}}\left(\int_0^{t_1}(-V_o cos\omega t - Zi_{Lm}(0) sin\omega t)dt + \int_{t_1}^{t_2}\frac{V_{in}}{n}dt + \int_{t_2}^{t_3} -V_o dt\right) \\ &= \frac{V_{in}(dT_{sw} - t_1)}{nT_{sw}} - \frac{v_o(1-d)}{2}(1 + cos\omega t_1) - \frac{v_o \, sin\, \omega t_1}{\omega T_{sw}} - \frac{Zi_{Lm}}{\omega T_{sw}}(1 - cos\omega t_1) \end{aligned} \tag{4.24}$$

To apply the small-signal perturbation and linearization of v_c, d, v_o and i_{Lm}, the small-signal model can be obtained using the above equations:

$$\widehat{v_c} = K_d \hat{d} - K_o \widehat{v_o} - R_{res}\widehat{\iota_{Lm}} \tag{4.25}$$

where

$$K_d = \frac{V_{in}}{n} + V_o + \frac{V_o}{2}(cos\omega t_1 - 1) \approx \frac{V_{in}}{n} + V_o \tag{4.26}$$

$$K_o = 1 - D + \frac{1-D}{2}(cos\omega t_1 - 1) + \frac{sin\,\omega t_1}{\omega T_{sw}} \approx 1 - D \tag{4.27}$$

$$R_{res} = \frac{L_m(1 - cos\omega t_1)}{n^2 T_{sw}} \tag{4.28}$$

For most practical applications, R_{res} is large enough to have a significant impact on the control-to-output transfer function. The resonant terms in (4.26) and (4.27) are very small and can be neglected. Using PWM switch model, the small-signal equivalent circuit including damping resistor for QSW converter is shown in Figure 4.7(a). To derive the control-to-output transfer function, the input voltage source is shortened to ground; the equivalent circuit is derived and shown in Figure 4.7(b).

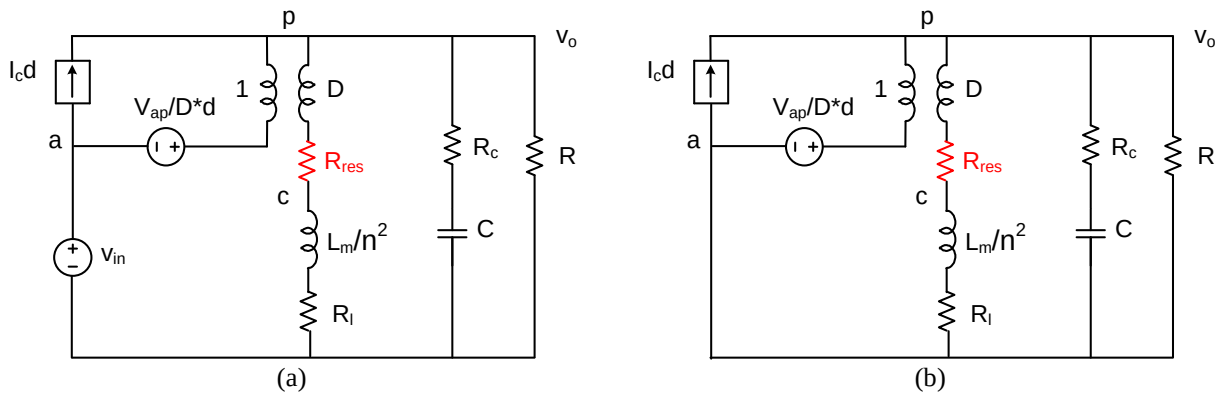


Figure 4.7. (a) Small-signal model including damping resistor for QSW buck-boost converter and (b) Equivalent circuit for control-output transfer function.

Due to the small magnetizing inductance in the QSW converter, the right half-plane zero moves beyond half of the switching frequency, which has a trivial impact on the transient response, in contrast to the conventional flyback converter. By including the propagation delay t_{delay} of all the components, the circuit-oriented control-to-output transfer function of the QSW converter can be expressed as

$$\frac{v_o}{v_c} = \frac{k_m G_{do}(1 + s/s_{z1})e^{-t_{delay}s}}{1 + s/\omega_0 Q + s^2/{\omega_0}^2} \tag{4.29}$$

where k_m is the modulation gain; G_{do} and S_{z1} are given by (4.2) and (4.3); and the denominator is the same as that in (4.1). Owing to the small inductance in QSW mode, ω_0 and Q can be simplified to the following expressions

$$\omega_0 \approx \frac{nD'}{\sqrt{L_m C}} \tag{4.30}$$

$$Q \approx \frac{D'}{n({D'}^2 R_c + R_l + R_{res})}\sqrt{\frac{L_m}{C}} \tag{4.31}$$

The dominant poles are complex-conjugate when the quality factor Q of the converter is greater than 0.5. On the other hand, the double poles may split and become two real poles if the damping resistor is large enough.

4.3 Parametric Study of Damping Effect on Control-to-Output Transfer Function

The impacts of deadtime, input voltage and output power on the control-to-output transfer function of the power stage are discussed.

Table 4.2 Values of parameters in QSW flyback converter

Magnetizing inductance L_m	0.85 uH
Turns ratio n	4
Output capacitor C	20 uF
ESR of output capacitor R_c	2.5 mΩ
Winding resistor R_l	50 mΩ

Given the specifications of nominal input voltage V_{in} = 48 V, full load P_o = 30 W, and the parameters listed in Table 4.2, the timing of the converter is calculated from the charge-based model.

4.3.1 Impact of Deadtime on the Control-to-output Transfer Function

A short duration of deadtime is required to avoid the shoot-through issue with high current spikes. Due to the limits of the specific device, the temperature, and lot-to-lot variation of the time delay, the deadtime may not be controlled exactly as shown in Figure 4.2. The gate-drive signal may be earlier or later than expected as indicated in Figure 4.8.

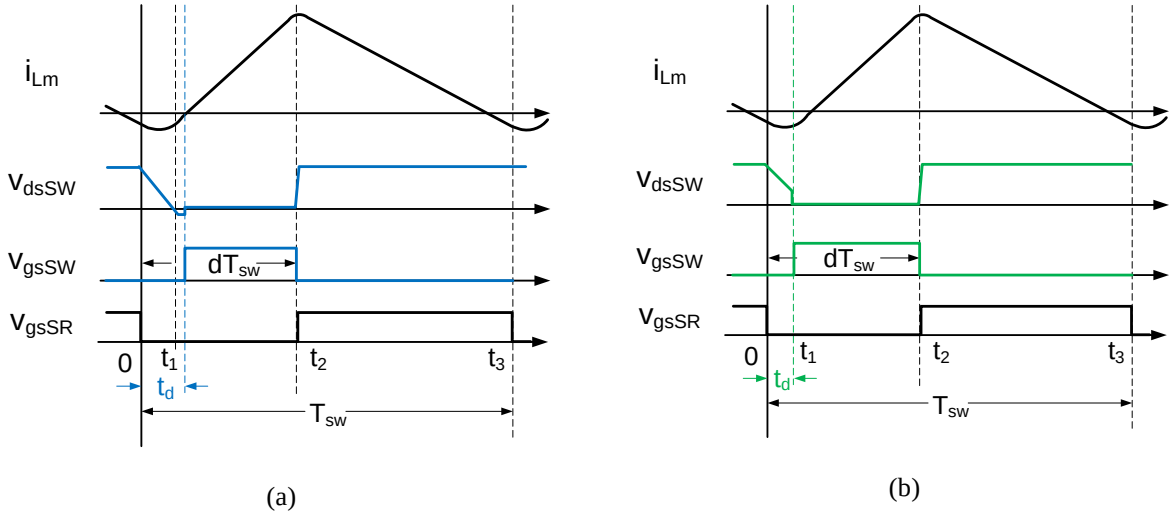


Figure 4.8. Waveforms of gate driving with (a) Late turn-on signal and (b) Early turn-on signal.

The Bode plots of different deadtimes with V_{in} = 48 V, V_o = 12 V, i_o = 2.5 A and f = 5 MHz are plotted and shown in Figure 4.9 to investigate the impact of deadtime on the control-to-output transfer function of the QSW converter . Based on the transient simulation at steady state, the resonant time t_1 is 8ns to achieve fully ZVS of input switch. When deadtime t_d is exactly equal to resonant time, the damping resistor can be calculated from (4.28) as 83.3mΩ and the

dominant poles are 18kHz and 383kHz. If the gate signal arrives late as shown in Figure 4.8(a), the body diode is conducting, and the control-to-output transfer function will not change. But if the driving signal is earlier as 6ns, the damping resistor will increase to 48mΩ and the poles are split to 25kHz and 270kHz; When t_d is 4ns, R_{res} is derived as 21.7mΩ and the real poles are located at 38kHz and 179kHz. As deadtime changes from 4ns to 8ns, resistance increases 3.8 times, and the damping is much stronger.

R_{res} will be zero when t_d is equal to zero , according to (4.28), and the model will be equivalent to the conventional CCM model. After running the switch-model based simulation to derive control-to-output transfer function in Simplis, it shows great agreement to the calculations by using the proposed model for different cases.

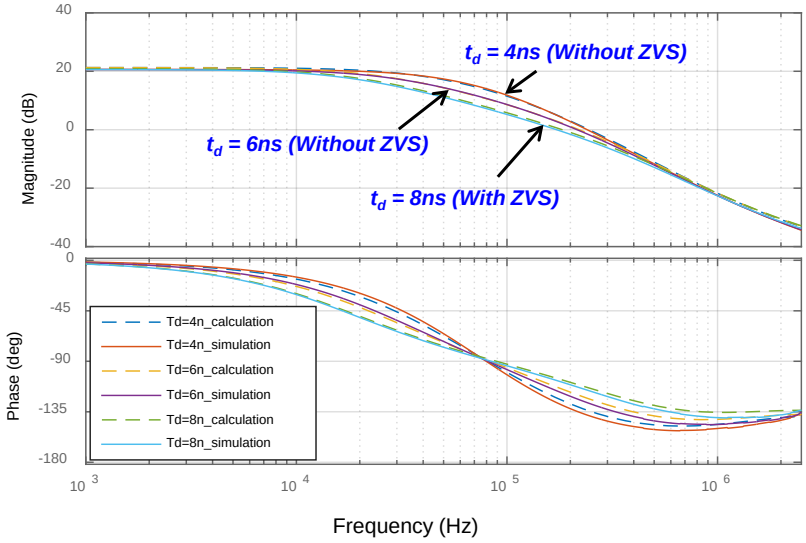


Figure 4.9. The control-to-output transfer function of the QSW converter with different deadtimes with V_{in} = 48 V, V_o = 12 V, i_o = 2.5 A and f = 5 MHz.

4.3.2 Impact of Input Voltage on the Control-to-output Transfer Function

The transfer function with V_{in} = 36 V, 48 V and 72 V under the same output voltage of 12-V, output current of 2.5-A and switching frequency of 5-MHz are shown in Figure 4.10 to study the impact of input voltage on the control-to-output transfer function and to verify the model under different input voltages. The duty cycle of SW is 60% when input voltage equals to 36 V; a deadtime of 22 ns is needed to fully achieve ZVS as illustrated in Figure 4.2 . The damping resistor is then calculated as 430 mΩ and the split poles are 4.2 kHz and 1.43 MHz. The duty cycle is 41% and t_d is 8 ns when V_{in} increases to 72 V. The R_{res} is 83.3 mΩ and the real poles are 23.4 kHz and 381 kHz.

The strong damping effect caused by the low line voltage is due to the larger duty cycle and longer resonant time according to (4.28) and (4.31). The theoretical calculations also match with Simplis simulations very well.

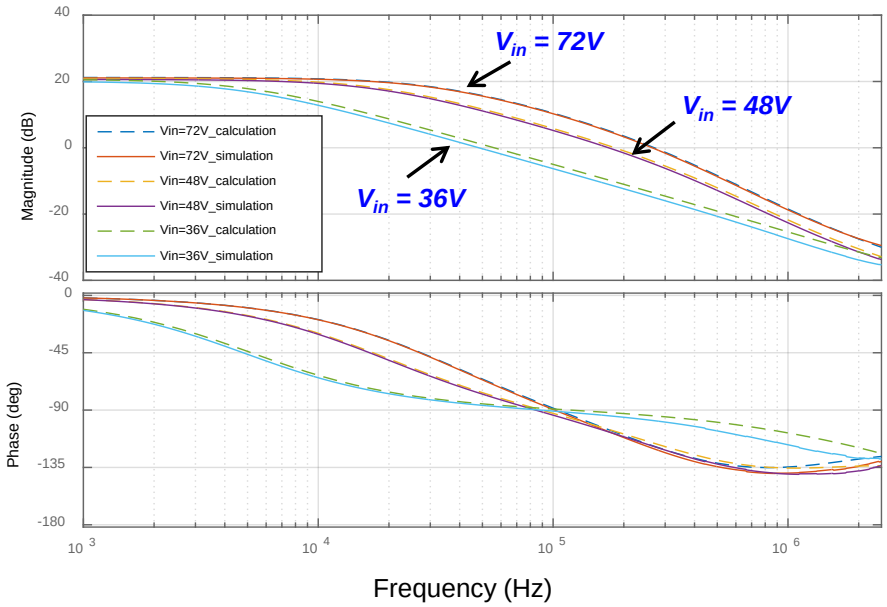


Figure 4.10. Control-to-output transfer function of QSW converter with different input voltages

with V_o = 12 V, i_o = 2.5 A and f = 5 MHz.

4.3.3 Impact of Output Power on the Control-to-output Transfer Function

The input voltage is kept the same at a nominal 48 V; the output voltage is constant at 12 V; and the switching frequency is 5 MHz. The deadtime is controlled to be 6 ns at light load and 8 ns at full load to achieve ZVS to sweep output current from 0.5 A to 2.5 A. The damping resistance is calculated as 48 mΩ and 83.3 mΩ, respectively. The first pole is moved from 24 kHz to 18 kHz, and the secondary pole is increased from 270 kHz to 383 kHz.

Since the magnetizing inductance in QSW-mode operation is relatively small, the quality factor Q from (4.31) indicates that the load will have little impact on the control-to-output transfer function, which is verified by the simulation results shown in Figure 4.11.

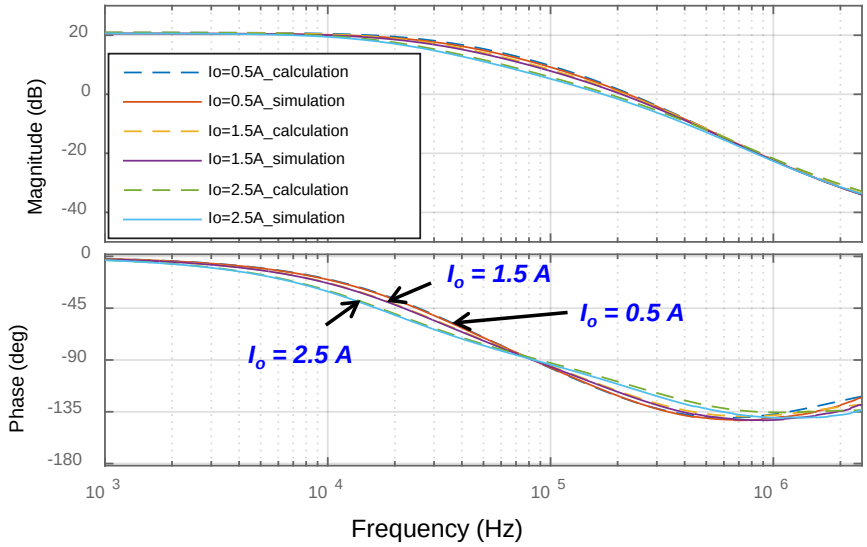


Figure 4.11. Control-to-output transfer function of QSW converter with different output currents with V_{in} = 48 V, V_o = 12 V and f = 5 MHz.

4.4 Experimental Verification

4.4.1 Open-loop Transfer Function

In order to validate the theoretical analysis of the small-signal model of the QSW converter, the open-loop transfer function from control V_{ctrl} to output V_o shown in **Figure 4.1** was measured with V_{in} = 48 V, V_o = 12 V and R = 5 Ω using an Agilent - HP 4396B network analyzer. Figure 4.12 shows the control-to-output transfer function of the measurements, and the calculation results of CCM, DCM and QSW model. With the given specifications and the same parameters shown in Table 4.2, the dominant poles are calculated to be at 14 kHz and 416 kHz showing great agreement between the experimental results and the conventional CCM model.

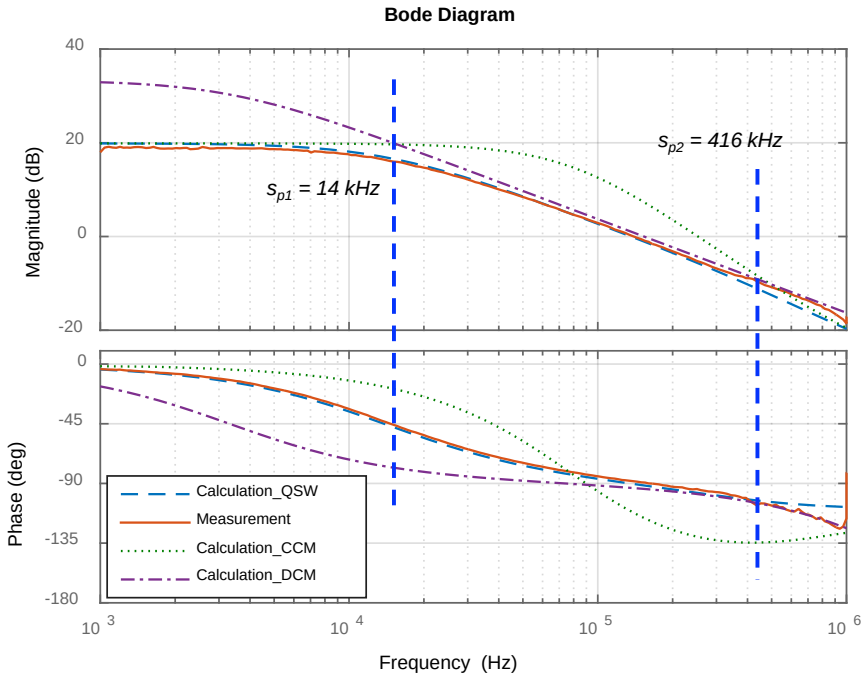


Figure 4.12. Calculation and measurement results of control-to-output transfer function for a QSW converter with V_{in} = 48 V, V_o = 12 V and R = 5 Ω.

4.4.2 Compensator Design

With the multi-megahertz switching frequency, hypothetically the closed-loop bandwidth of the QSW flyback converter can be pushed to be much higher than those of the conventional flyback converter. The accurate small-signal model of the QSW flyback converter introduced in the previous section helps to realize this higher bandwidth by adding a compensation network afterwards to stabilize the system.

A Type III compensator is employed to boost the phase and push the bandwidth, and the transfer function of the compensator is

$$H(s) = \frac{G(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s\left(1 + s/\omega_{p1}\right)\left(1 + s/\omega_{p2}\right)}. \tag{4.32}$$

The compensation network is designed to operate with a nominal input voltage of 48 V and under full-load conditions. The closed-loop dc gain is boosted by an integrator to minimize the steady-state error. The two low-frequency zeros are to compensate the two dominant real poles, which are placed at 20 kHz and 260 kHz. Two high-frequency poles at 1.9 MHz and 2.23 MHz are used to cancel out the ESR zero and attenuate the switching ripples, respectively. The gain of the compensator is equal to $3.65*10^8$. The bandwidth is designed at 250 kHz with an 81 degree phase margin and 21.6 dB gain margin.

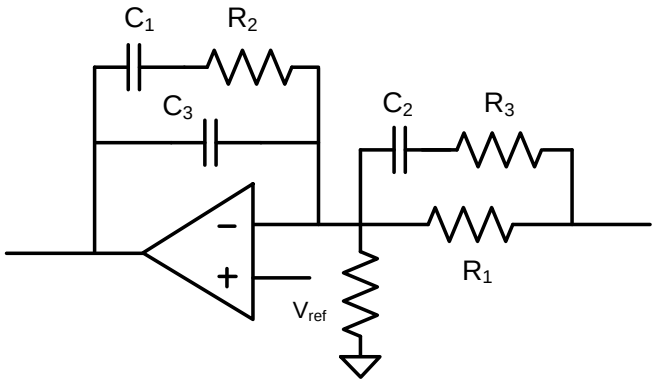


Figure 4.13. Schematic of Type III compensator.

To implement the Type III compensator with an RC network, as shown in Figure 4.13, the following equations are used to determine the values of the resistances and capacitances [6]:

$$\omega_{z1} = \frac{1}{R_2 C_1} \tag{4.33}$$

$$\omega_{z2} = \frac{1}{(R_1 + R_3)C_2} \tag{4.34}$$

$$\omega_{p1} = \frac{1}{R_3 C_2} \tag{4.35}$$

$$\omega_{p2} = \frac{1}{(C_1 \parallel C_3)R_2} \tag{4.36}$$

$$\omega_{p2} = \frac{1}{(C_1 + C_3)R_1} \tag{4.37}$$

Resistor R_1 is selected as 3.3 kΩ. Then by solving (4.33) - (4.37), the other components can be derived and are listed in Table 4.3.

Table 4.3 Value of resistances and capacitances in Type III compensator

R_1 (kΩ)	**R_2(kΩ)**	**R_3(kΩ)**	**C_1 (nF)**	**C_2 (pF)**	**C_3 (pF)**
3.3	4.4	520	1.8	160	16

Figure 4.14 shows the Bode plot of the loop gain for the QSW flyback converter by applying the Type III compensator to the system and closing the control loop in voltage mode. The crossover frequency is 262 kHz, the phase margin is 76 degrees, and the gain margin is 20 dB, which match very well with the theoretical design results.

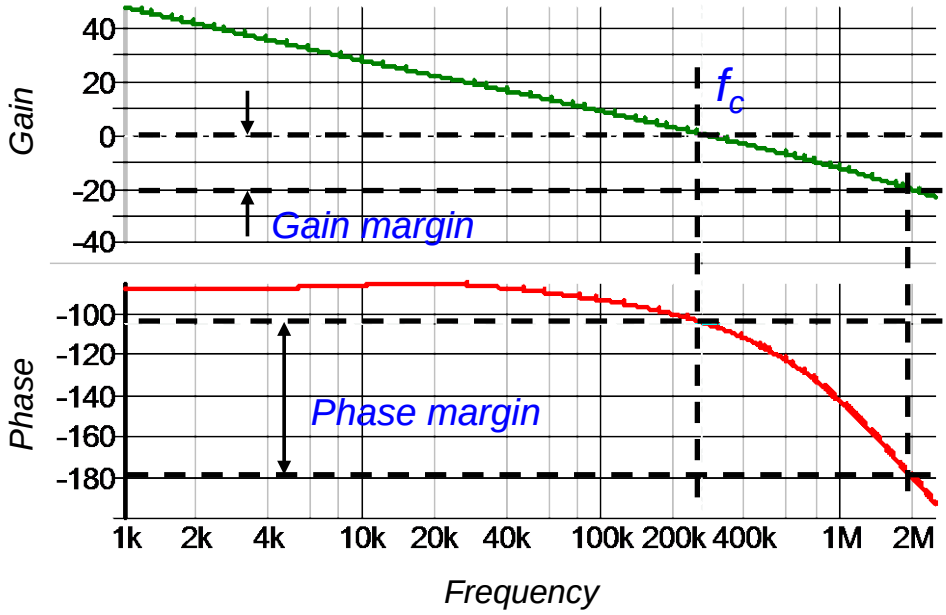


Figure 4.14. Simulated loop gain of QSW flyback converter with the compensator shown in Table 4.3.

The closed-loop bandwidth can be further raised by increasing the gain of the compensator. The trade-off is a smaller phase margin and gain margin. In general, a phase margin of 90 degrees means the system is very stable. A phase margin of 60 degrees is a good compromise between fast transient response and stability. Phase margins of 30 degrees or less cause the system to have substantial ringing when subjected to transients, and little tolerance for component or environmental variations. Figure 4.15 shows another design example to raise the

closed-loop bandwidth at 674 kHz where the phase margin is reduced to 50 degrees and the gain margin is 10 dB.

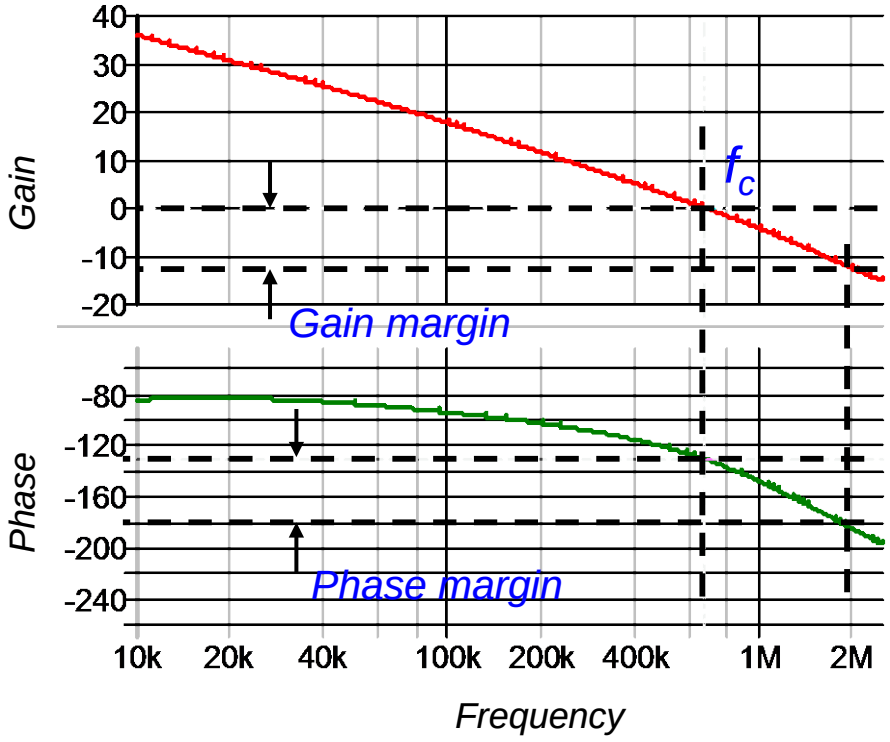
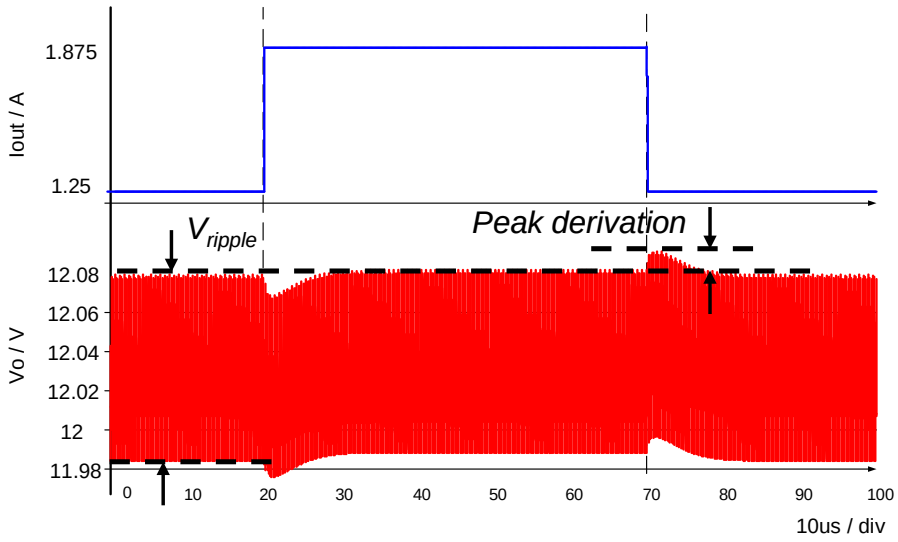


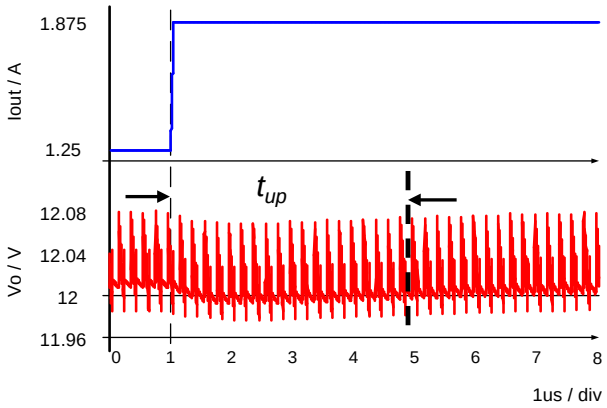
Figure 4.15. Loop gain of QSW flyback converter with crossover frequency at 674 kHz.

4.4.3 Load-step Response

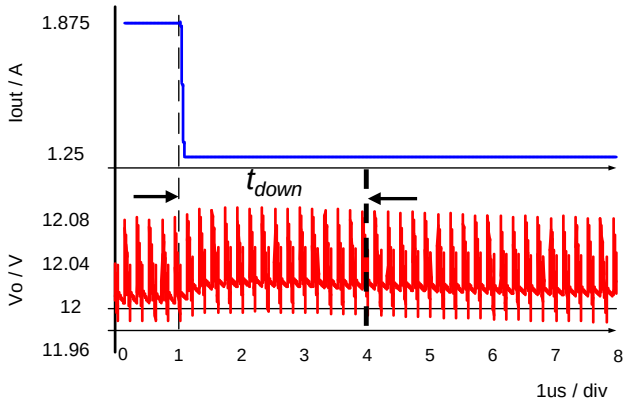
The load is changed to be between 50% and 75% of the full load to evaluate the transient performance after closing the feedback loop. Figure 4.16 shows the step-up and step-down responses in Simplis simulation with a bandwidth of 262 kHz for the QSW flyback converter.



(a)



(b)



(c)

Figure 4.16.(a) Simulation of 50-75-50% of load-step response for QSW flyback converter with a crossover frequency of 262 kHz, (b) Load step-up response and (c) Load step-down response.

The relatively large output voltage ripple is caused by a large current ripple in the QSW converter. The dynamic characteristic is quantified by peak derivation and settling times defined in Figure 4.16(a). To keep the ripple around 100 mV, as it is in the state-of-the-art commercial flyback converter, the output capacitance is chosen as 20 uF with an ESR of 2.5 mΩ. By pushing the switching frequency to be approximately 16 times higher, the peak derivation is 15 mV,

which is around 25 times smaller than in commercial products. The settling time defined in Figure 4.16(b) and (c) is also reduced significantly from 160 μs to 4.5μs for the step-up response, and from 160 μs to 3.8 μs for the step-down response. A comparison of the transient performance between the commercial flyback converter and the proposed work is summarized in Table 4.4.

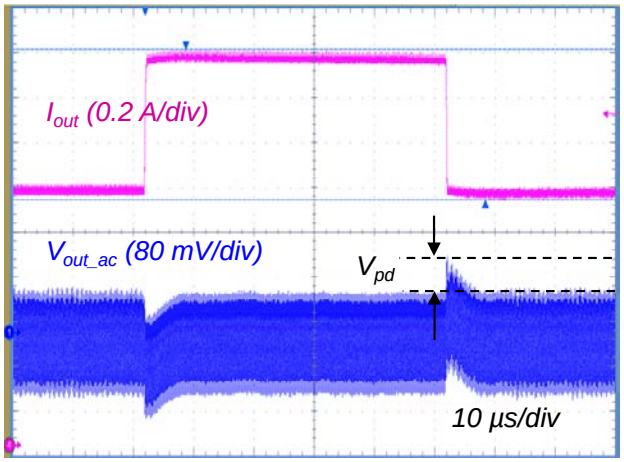
Table 4.4 Comparison of the transient performance between the commercial flyback converter and the proposed work.

	State-of-the-art	**Proposed Work**		
Switching frequency (kHz)	300	5000		
Output capacitance (μF)	188	20	20	20
Vripple (mV)	100	94	94	94
Designed BW (kHz)	N/A	106	262	674
Step-up settling time (μs)	160	11.7	5	0.8
Step-down settling time (μs)	160	11.2	4	0.6
Peak derivation (mV)	250	40	10	4

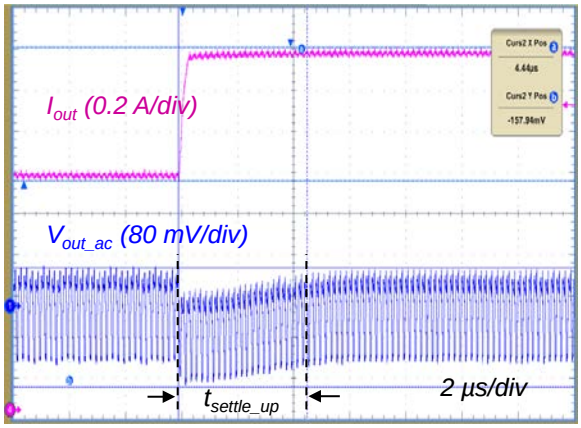
To verify the theoretical analysis of the small-signal model for the QSW converter, a test board was constructed, and a resistive load was built to emulate the load step between 50% and 75% of the full load. The experimental waveforms of i_{out} and V_{out} are shown in Figure 4.17 with the crossover frequency at 262 kHz; the settling time and peak derivation are listed in Table 4.5. The parasitic inductance in the PCB or ESL of the capacitor may introduce extra overshoot on the output voltage. The settling time of the model is in good agreement with the simulation.

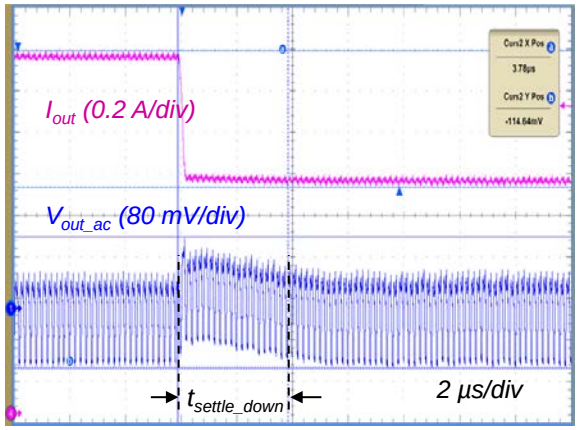
Table 4.5 Comparison of dynamic performance between simulation and experiment results

	Peak derivation (mV)	**t_{up}(μs)**	**t_{down} (μs)**
Simulation	10	5	4
Measurement	15	4.44	3.78



(a)





(b) (c)

Figure 4.17. (a) Experimental load-step response for QSW flyback converter with crossover frequency of 262 kHz, (b) Load step-up response and (c) Load step-down response.

4.5 Summary

The conventional small-signal CCM and DCM model cannot predict the transfer function in quasi-square-wave mode operation. A modified circuit-oriented small-signal model of QSW converter is proposed to analytically quantify the damp effect of control-to-output transfer function. The impacts of the deadtime, input voltage, and output power on the control-to-output transfer function of the power stage are analyzed in details. The double poles split more widely when the resonant time goes longer, which is verified by the simulation in Simplis. The measured control-to-output transfer function of 5-MHz QSW flyback converter has a great agreement to the calculation results, and the transient performance is improved significantly with high closed-loop bandwidth based on an accurate small-signal model.

4.6 Reference

[1] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode," in *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, no. 3, pp. 490-496, May 1990.

[2] Jian Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein and R. M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode," in *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 482-492, Jul 2001.

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Time-Controlled Synchronous Gate Drive," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6817-6828, Dec. 2015.

[5] W. Qiu, S. Mercer, Z. Liang and G. Miller, "Driver Deadtime Control and Its Impact on System Stability of Synchronous Buck Voltage Regulator," in *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 163-171, Jan. 2008.

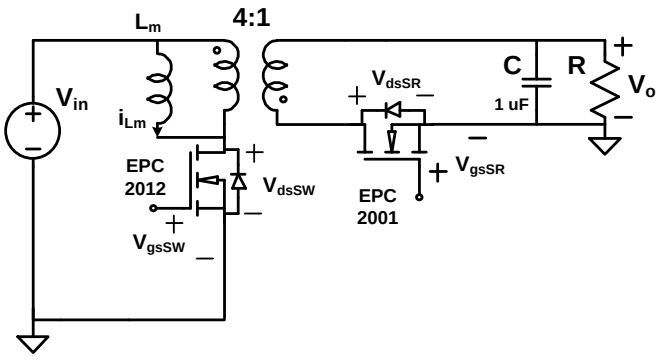
[6] H. Dean Venable, “The k factor: a new mathematical tool for stability analysis and synthesis,” Linear Technology, reference reading, available: http://www.linear.com.

Chapter 5 QSW Flyback Converter with Dead-time Control

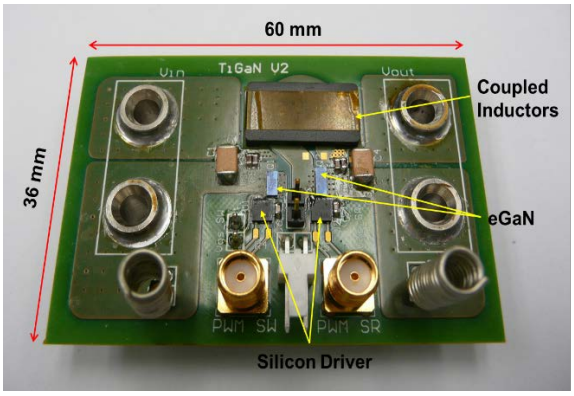
In order to verify the analysis of QSW flyback converter and evaluate its efficiency, the hardware for the power stage and control system of QSW converter is introduced in this chapter. The gate drive design, parasitic analysis, and loss breakdown are presented in detail. The dead time control schemes are compared, followed by a proposed solution of variable dead time control.

5.1 Power Stage of QSW Flyback Converter

The test board shown in Figure 5.1(b) was constructed. The footprint of the test board carrying the power stage is 32 mm × 28 mm. An EI core with a size of 18 mm × 10 mm occupies 30% of the power stage. An EPC 2012 eGaN FET (200 V) was selected to be the input switch, an EPC 2001 eGaN FET (100 V) was the synchronous rectifier, and a LM5114 was used to drive eGaN FETs. Table 5.1 lists the main components and test probes in the prototype.



(a)



(b)

Figure 5.1. (a) Schematic and (b) Test board of QSW flyback converter.

Table 5.1 List of components and test probe in the measurement shown in Figure 5.1(b)

Component Name	*Value and Part Number*
T1	L_m = 0.87 μH, n = 4:1
SW	EPC 2012
SR	EPC 2001
Driver U1, U2	LM 5114
10X Passive voltage probe	Tektronix TPP0500
Low voltage differential probe	Tektronix TDP1000

5.1.1 Parasitic inductance of the layout

The maximum allowable gate voltage of 6 V is one and a half volts above the recommended 4.5 V drive voltage [1]. This limited headroom requires an accurate gate drive supply, as well as a limited inductance between the eGaN FET and gate driver as the inductance can cause a voltage overshoot on the gate. The inductance of the gate loop will directly limit the switching speed of the device and should be minimized to achieve maximum efficiency.

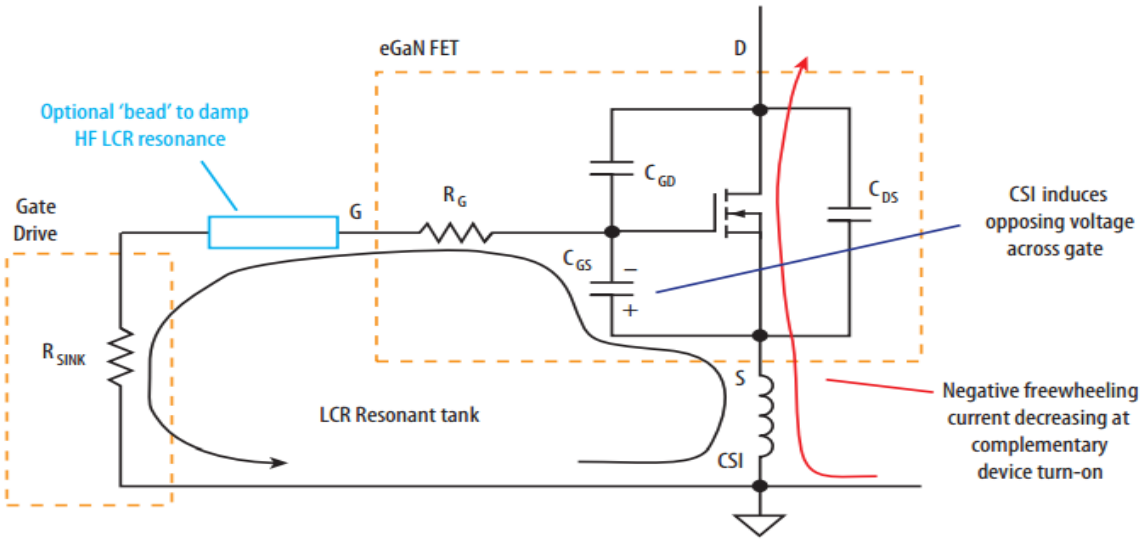


Figure 5.2. Equivalent partial power circuit with common source inductance [2].

The common source inductance shown in Figure 5.2 has significant impact on converter efficiency. The addition of CSI effectively induces a voltage across the inductance that opposes the gate drive voltage during di/dt, thus increases turn-on and turn-off times. It is therefore important to minimize common source inductance for optimum switching performance. Increasing the gate resistance or adding a ferrite bead can help damp the resonance, but the gate loop inductance will be increased with the extra components [3].

The threshold voltage of eGaN FETs is relative low around 1.4 V. High di/dt with common-source inductances may cause gate spike to false turn on the switches. Therefore, negative gate drive needs to be used as shown in Figure 5.3. In order to avoid the shoot-through issue, a zener diode was applied to create a -2 V between gate and source to turn the switches off in the presence of 0.7 nH of common-source inductance. The gate driver chip should be placed next to the eGaN FETs to minimize the loop inductance.

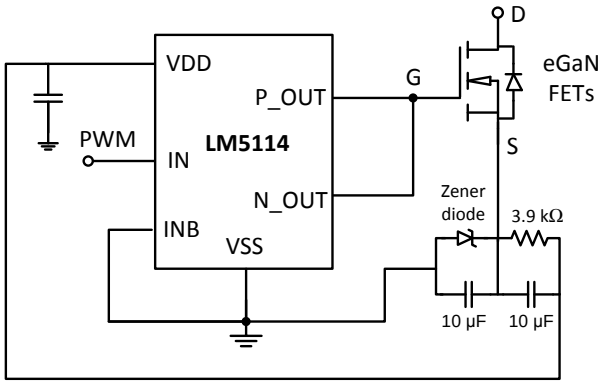


Figure 5.3. Schematic of negative drive for eGaN FETs.

To minimize the voltage stress on the eGaN FETs, the PCB layout for power stage was carefully designed to reduce the power loop inductance. The power connection to the drain and source are routed on the same layer of the PCB and terminate to one side of the FET, which is shown in Figure 5.4. The drain and source terminals are connected to additional layers by using

vias to further enhance their current carrying capability. Two-ounce thick copper for all layers ensures the lowest possible connection resistance.

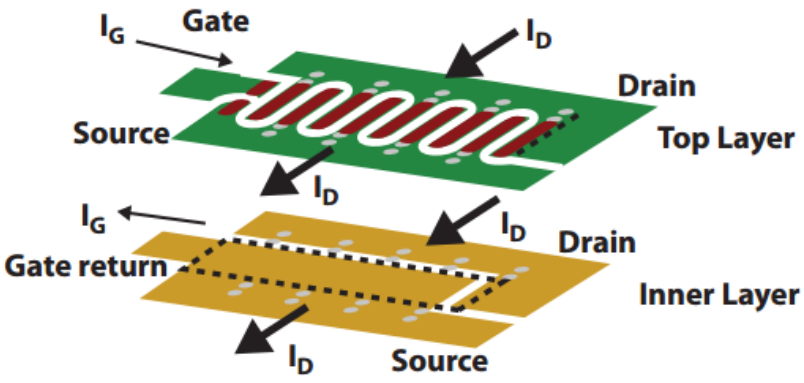


Figure 5.4. Layout of eGaN configuration [2].

Further reduction in the coupling between the gate-source circuit and drain-source circuit can be achieved by designing the two circuit's currents to be orthogonal with respect to each other. The 4-layer layout of the entire system is shown in Figure 5.5, and the parasitic inductances are simulated in Q3D. The detailed layout for power loop and gate driving loop are shown in Figure 5.6 and the simulation results are listed in Table 4.2.

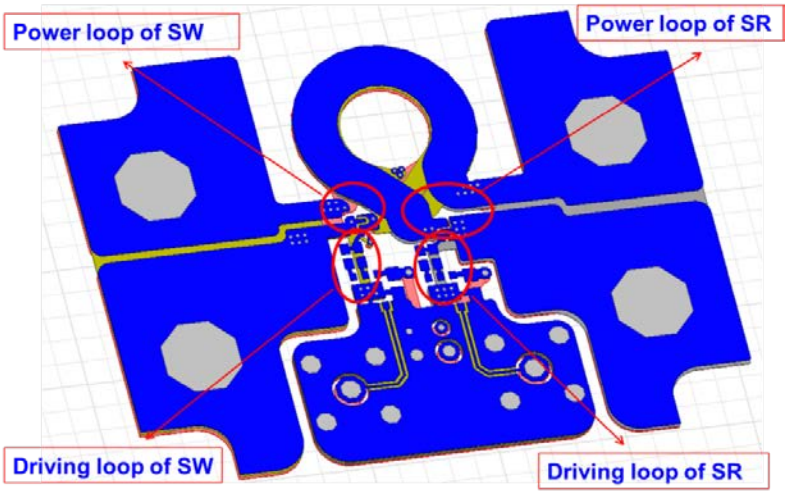


Figure 5.5. Simulation model of PCB layout in Q3D.

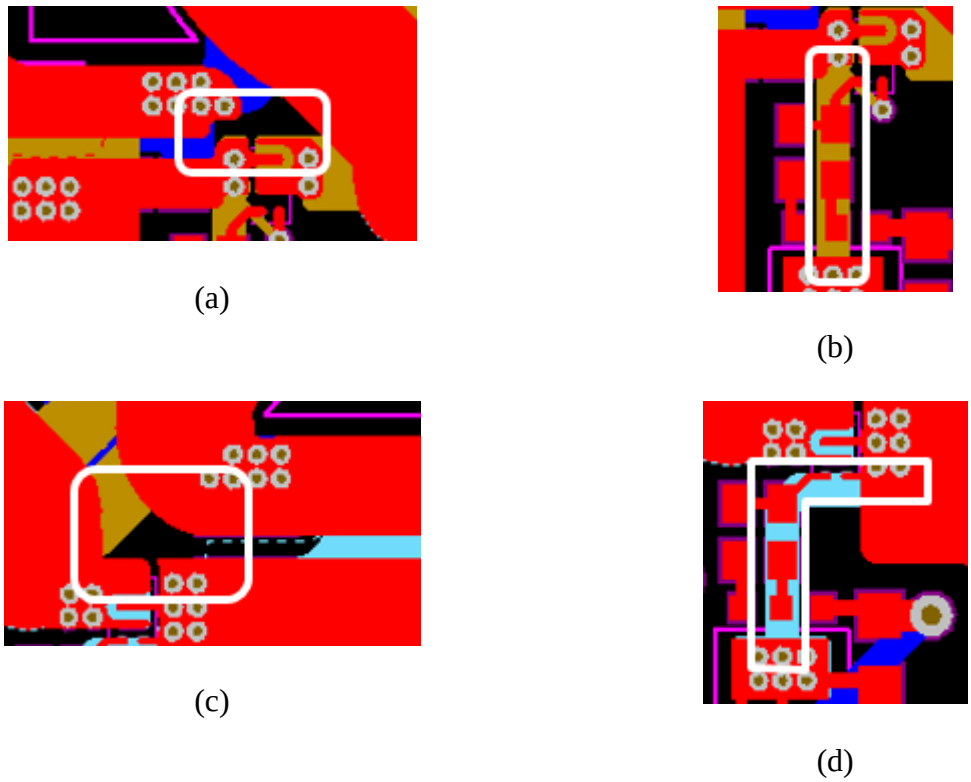


Figure 5.6. PCB layout for (a) power loop and (b) gate loop of the primary switch, (c) power loop and (d) gate loop of the secondary SR.

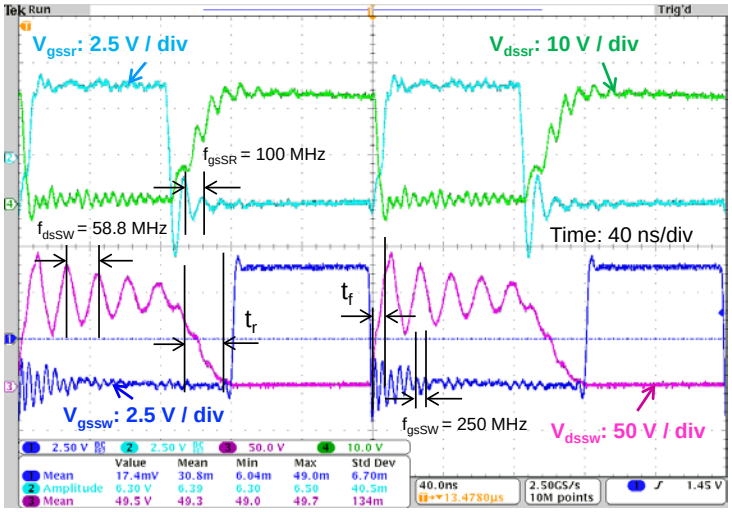


Figure 5.7. Waveforms of V_{gs} and V_{ds} for SW and SR with negative drive at V_{in} = 48 V, V_o = 12 V, f = 5 MHz, and P_o = 30 W.

Table 5.2 Simulated parasitic inductance for the layout shown in Figure 5.5

L_{SW_gate} (nH)	L_{SR_gate} (nH)	L_{SW_gate} (nH)	L_{SR_gate} (nH)
2	2	3.5	2.5

The parasitic inductance in the prototype can be estimated by measuring the ringing frequencies of the waveforms shown in Figure 5.7 when the resonant capacitances in the gate drive and power loop are known. Since the charge-equivalent capacitances provide a good approximation based on the analysis in Chapter 2, the parasitic inductances in the power loop and gate loop can be calculated with the given $C_{eq,Q}$. For example, when the input capacitance of switch SW is C_{iss_SW} = 100 pF as seen in the datasheet, the gate-loop inductance of input switch SW is L_{SW_gate} = 4.1nH. Following the same procedure, the other loop inductances can be derived and listed in Table 5.3. The L_{loop} includes the leakage inductance and the power-loop inductances which depend on the layout. The simulation results are matched with experimental waveforms by using these parasitics. The parasitics inside the gate drive chips which is around 0.5 nH ~1 nH are not included in the Q3D simulation.

Table 5.3 Parasitics for the test board shown in Figure 5.1(b)

Parasitic capacitor	C values (pF)	Parasitic inductor	L values (pF)
C_{iss_SW}	100	L_{SW_gate} (nH)	4.1
C_{iss_SR}	770	L_{SR_gate} (nH)	3.3
C_{oss_SW}	113.5	L_{loop} (nH)	64.5
C_{oss_SR}	916.8		

As shown in Figure 5.7, the rise time of the input switching is 18ns between the 90% and 10% value of the drain-source voltage, and the fall time is approximately 5ns from the 90% to 10% of V_{dssw}. Table 5.4 shows the consistent results between measurement and theoretical calculation,

which validates the charge based model of QSW flyback converter discussed in Chapter 2. The differences between the measured and calculated values for t_r and t_f are caused by several tens of picofarad parasitic capacitance from flyback transformers and measurement probes.

Table 5.4 Comparison of rising / falling time of V_{dssw} between calculation and measurement at V_{in} = 48 V, V_o = 12 V, f = 5 MHz, and P_o = 30 W

	Calculation	Measurement
Rising time t_r (ns)	4.5	5
Falling time t_f (ns)	15	18

5.1.2 Loss breakdown of QSW flyback converter

With the input voltage of 48 V and output voltage regulated as 12 V constantly at 5 MHz, Figure 5.8 shows the efficiency curve versus different loads with the peak value of 90.6%. The power density is 120 W/in^3.

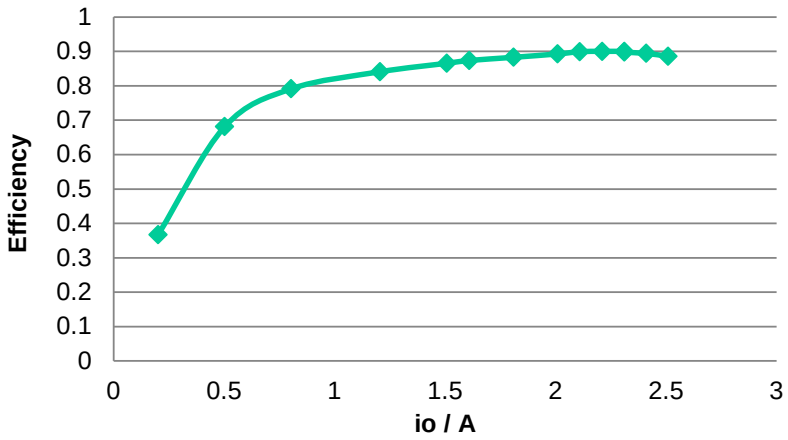


Figure 5.8. Efficiency curve versus different loads at Vin = 48 V, Vo = 12 V, and f = 5 MHz.

The losses on the switch can be calculated since switch currents can be estimated by simulation, and most parameters including R_{dson} and the gate charge of eGaN FETs can be found in the datasheet. The magnetic losses are evaluated by finite-element simulation, which is

discussed in Chapter 3. The total losses of QSW flyback converter measured at V_{in} = 48 V, V_o = 12 V, f = 5 MHz, and P_o = 30 W can be broken down and shown in Figure 5.9.Switch losses account for 60% of the total loss; 26.6% of the total losses are incurred in the coupled inductors; 53% of magnetic loss is winding loss because of the skin and proximity effects at megahertz range. The dead-time loss is significant and cause huge conduction loss on the switches.

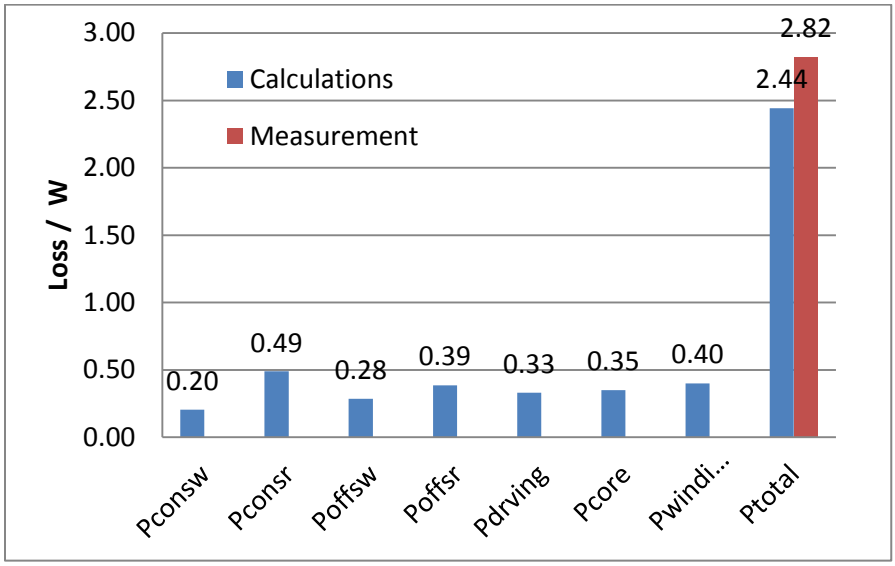


Figure 5.9. Loss breakdown of QSW flyback converter measured at V_{in} = 48 V, V_o = 12 V, f = 5 MHz, and P_o = 30 W.

Terminal loss from the interconnection, ESR of the components, and the parasitic resistance of PCB can cause the discrepancies between the calculation and measurement. Without considering the effect of dc bias, the core loss is also underestimated.

5.2 Adaptive Dead-time Control

5.2.1 Evaluation of dead-time loss

A proper duration of dead-time (i.e. a time interval when neither switch is on) is required to avoid shoot-through issue with high current spikes.

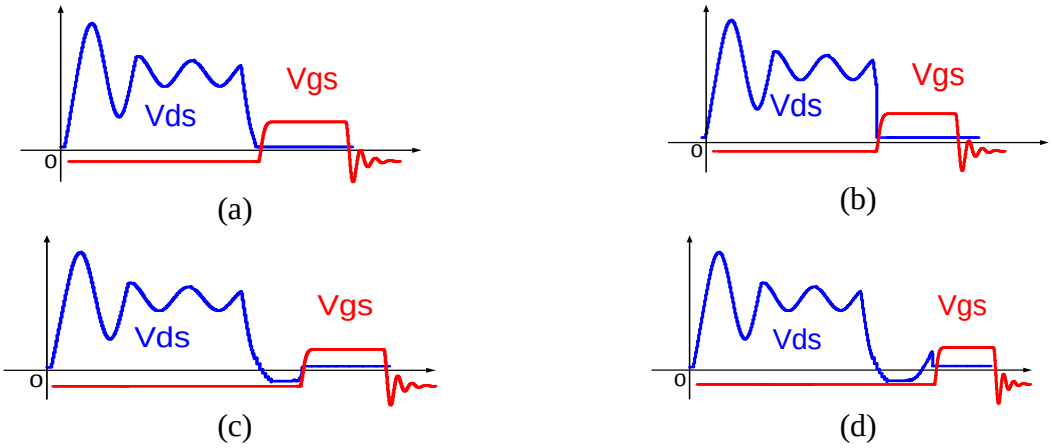


Figure 5.10. V_{ds} and V_{gs} waveforms with (a) ideal timing of drive signal, (b) early gate drive (nonzvs), (c) late gate drive arrival and (d) too much delay to lose ZVS.

As shown in Figure 5.10, large turn-on loss will be induced for high input voltage with early gate driving signal; on the other hand, the reverse voltage drop of 1.8-V for synchronous rectifier may cause high conduction losses with late drive arrival.

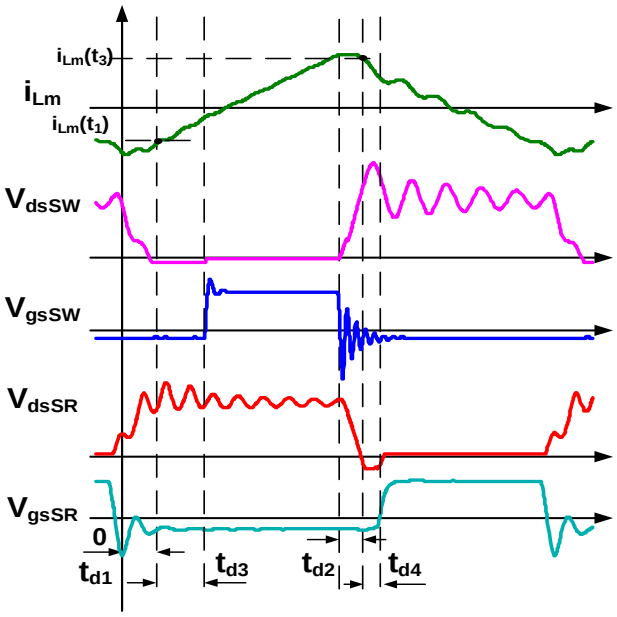
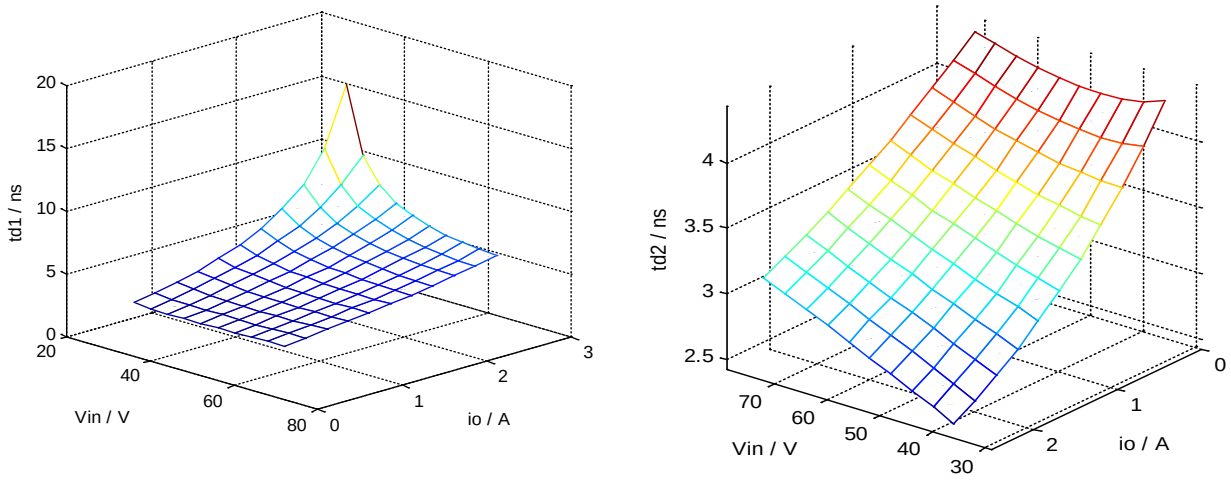


Figure 5.11. Definition of resonant time and delay time (t_{d1}, t_{d2}, t_{d3} and t_{d4}) for QSW flyback.

The typical waveforms of QSW flyback converter is shown in Figure 5.11. The resonant time t_{d1} and t_{d2} defined in Figure 5.11 alter with different input voltage and output power to charge and discharge the output capacitances of eGaN FETS, which can be derived from the charge based model from Chapter 2.

Figure 5.12(a) shows the resonant time t_{d1} varies from 4 ns to 17 ns depending on the input voltage and load condition. The moderate change of resonant time t_{d2} for the secondary SR is within 2.5 ns to 4.3 ns at various input and load shown in Figure 5.12(b).



(a) (b)

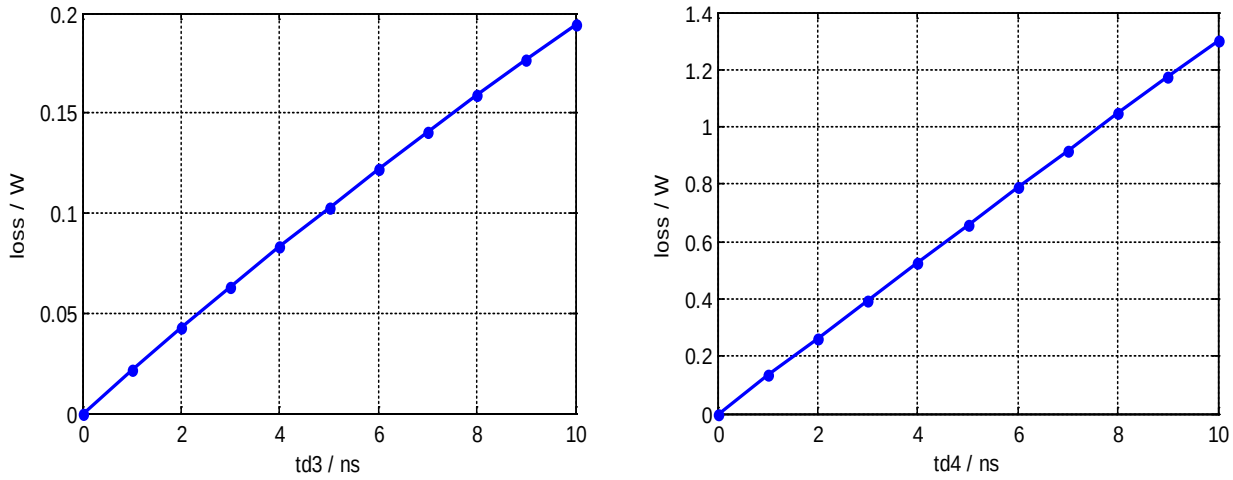
Figure 5.12. (a) Resonant time t_{d1} defined in Figure 5.11 at various input voltage and output current operation condition and (b) Resonant time t_{d2} defined in Figure 5.11 at various input voltage and output current operation condition.

The extra time interval t_{d3} and t_{d4} defined in Figure 5.11 should be zero in an ideal situation, which may not happen all the time. To quantify the loss generated by additional delay time, the following equations can be used:

$$P_{deadsw} = 0.5V_{sd}t_{d3}f\left[-2i_{Lm}(t_1) - \frac{nV_o}{L_m}t_{d3}\right] \quad (5.1)$$

$$P_{deadsr} = 0.5V_{sd}t_{d4}f\left[-2ni_{Lm}(t_3) - \frac{V_{in}}{L_m}t_{d4}\right] \quad (5.2)$$

where the reverse voltage drop V_{sd} is 1.8 V for EPC GaN FETs, switching frequency f is 5 MHz, and turns ratio n is 4. The worst case for dead-time loss for the primary SW is no load with large negative conduction current $i_{Lm}(t_1)$ which is equal to -2.41 A. Figure 5.13(a) shows the additional loss brings about 20 mW with one-nanosecond extra delay. The full load with 48-V rated input voltage is the worst case for the secondary SR, and has a resonant current $i_{Lm}(t_3)$ of 3.68 A initially. As shown in Figure 5.13(b), the dead-time loss generated by 10-ns gate signal delay could increase to 1.3 W, which is 4.3% of the total power, causing a significant impact on the total efficiency.



(a) (b)

Figure 5.13. Dead-time losses generated by additional delay time defined in Figure 5.11 (a) for the primary switch SW at V_{in} = 48 V and no load and (b) for the secondary SR at V_{in} = 48 V and full load.

5.2.2 Control algorithm

A dead-time controller circuit is required to set the proper dead-time to minimize the loss. Figure 5.14 shows the control structure of quasi-square-wave flyback converter. Compared to the traditional control method, it has voltage mode merging with adaptive dead-time loop. The turn-on of the switch is triggered by ZVS detection circuit, and the on-time is determined by voltage loop. A current reference signal needs to be added to the loop in order to stabilize the system. It can run both variable frequency and constant frequency operation.

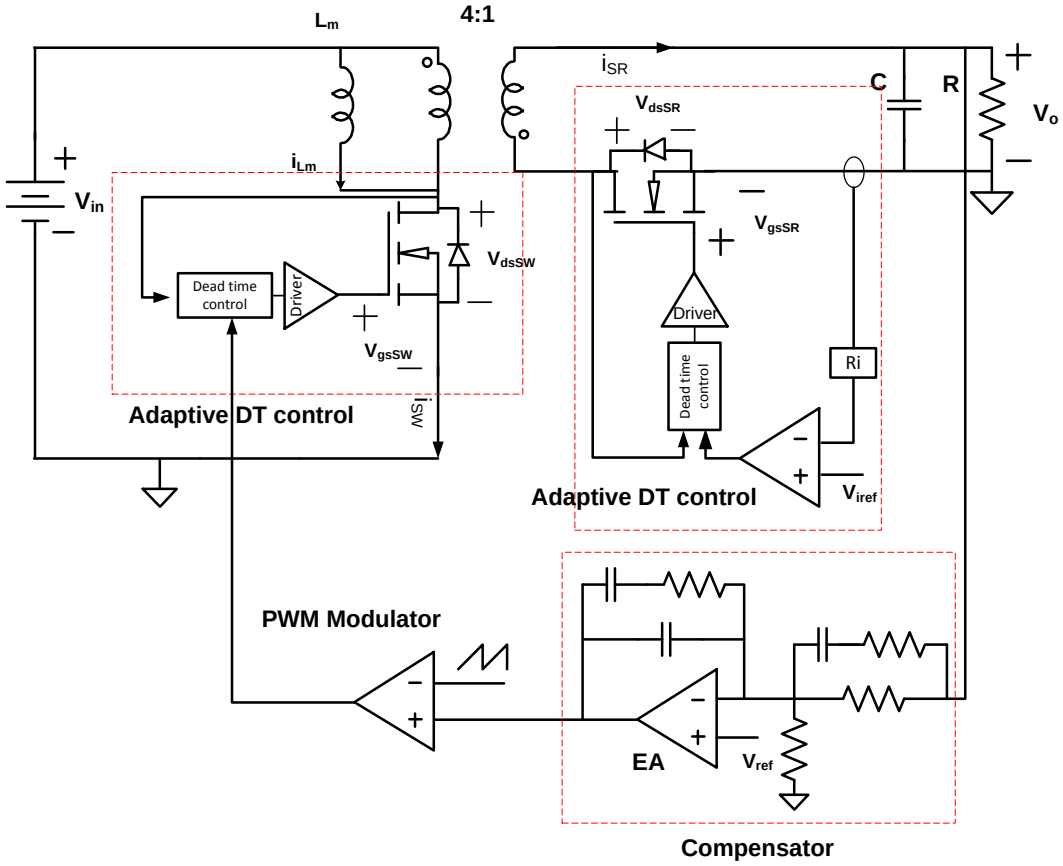


Figure 5.14. Control diagram of ZVS QSW flyback converter.

The operations of the controller are divided into ZVS and non-ZVS mode. To determine if the converter is in ZVS mode or non-ZVS mode, magnetizing current needs to be sensed to

determine if the resonant current is sufficient enough to discharge the output capacitances of the switches down to zero. The value of negative magnetizing current can be calculated at worst case which is the highest input voltage and heavy load, which is explained in Chapter 2. If the negative current is too small, i.e. $i_{Lm} > i_{SW\_ZVS}$, the flag i_{zvs} stays at zero, and turns-on of the primary switch is followed by the turn-off signal from SR. Otherwise, if the magnetizing current i_{Lm} is smaller than the threshold current i_{sw_zvs}, the flag i_{zvs} is stepping up to one as shown in Figure 5.15, which indicates the converter is in ZVS mode.

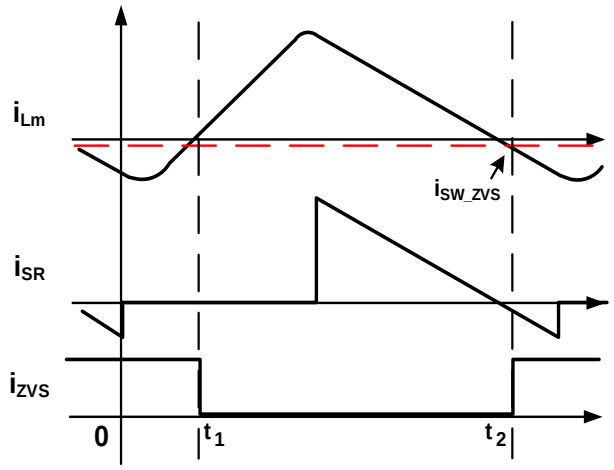


Figure 5.15. Threshold current sensing of magnetizing inductor for zero-voltage switching.

In ZVS mode, the turn on of both input switch and synchronous rectifier is triggered when the drain-to-source voltage decreases to zero. The turn-off time of input switch SW is determined by voltage loop, and the turning-off of SR is controlled by the clock signal with certain frequency. The detailed control logic of gate signal is shown in Figure 5.16, and the corresponding truth table is listed in Table 5.5.

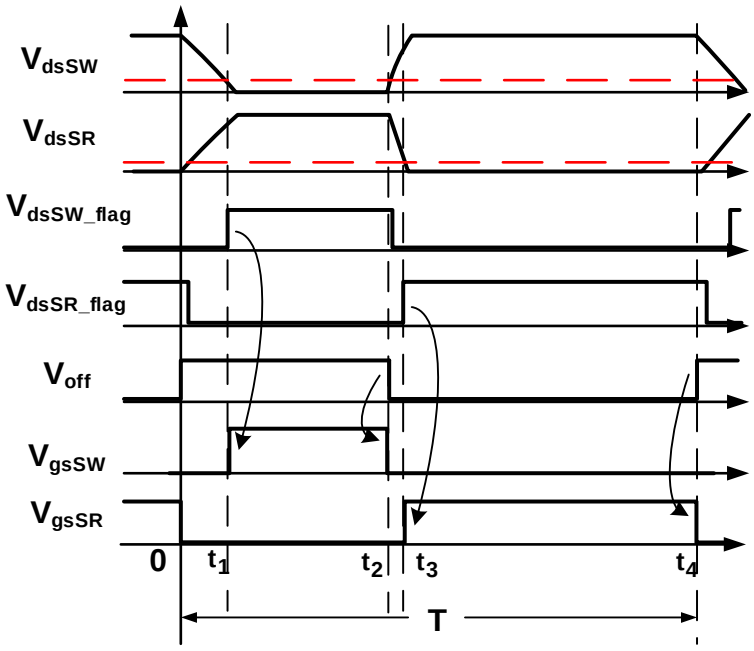


Figure 5.16. Control logic of gate signal V_{gsSW} and V_{gsSR} at steady state when ZVS is achieved.

Table 5.5 Truth table of control logic of gate signal shown in Figure 5.16

V_{dsSW_flag}	V_{dsSR_flag}	V_{off}	V_{gsSW}	V_{gsSR}
0	×	0	0	0
0	×	1	0	0
1	×	0	0	0
1	×	1	1	0
×	0	0	0	0
×	0	1	0	0
×	1	0	0	1
×	1	1	0	0

The switches cannot achieve ZVS during startup and transient, and the converter has to be operated at non-ZVS mode. It works similarly to the conventional hard-switching flyback

converter. The gate driving signals are controlled by PWM regulator and the waveforms are shown in Figure 5.17.

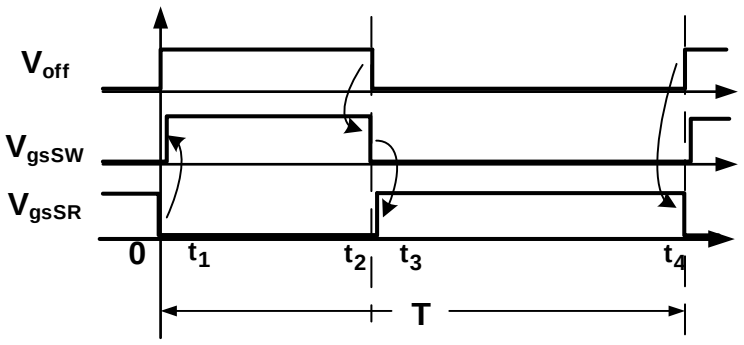


Figure 5.17. Control logic of gate signal V_{gsSW} and V_{gsSR} at non-ZVS mode during startup and transient.

Table 5.6 Truth table of control logic of gate signal V_{gssw}

i_{zvs}	V_{off}	V_{dsSW_flag}	V_{gsSR}	V_{gsSW}
0	0	×	0	0
0	0	×	1	0
0	1	×	0	1
0	1	×	1	0
1	0	0	×	0
1	0	1	×	0
1	1	0	×	0
1	1	1	×	1

By considering both ZVS and non-ZVS mode, the complete truth table of control logic for gate drive signal V_{gsSW} and V_{gsSR} are shown in Table 5.6 and Table 5.7. The logic equations of V_{gsSW} and V_{gsSR} can be expressed as

$$V_{gssw} = V_{off}(V_{dssw} i_{zvs} + \bar{V}_{dssr} \bar{\imath}_{zvs}) \quad (5.3)$$

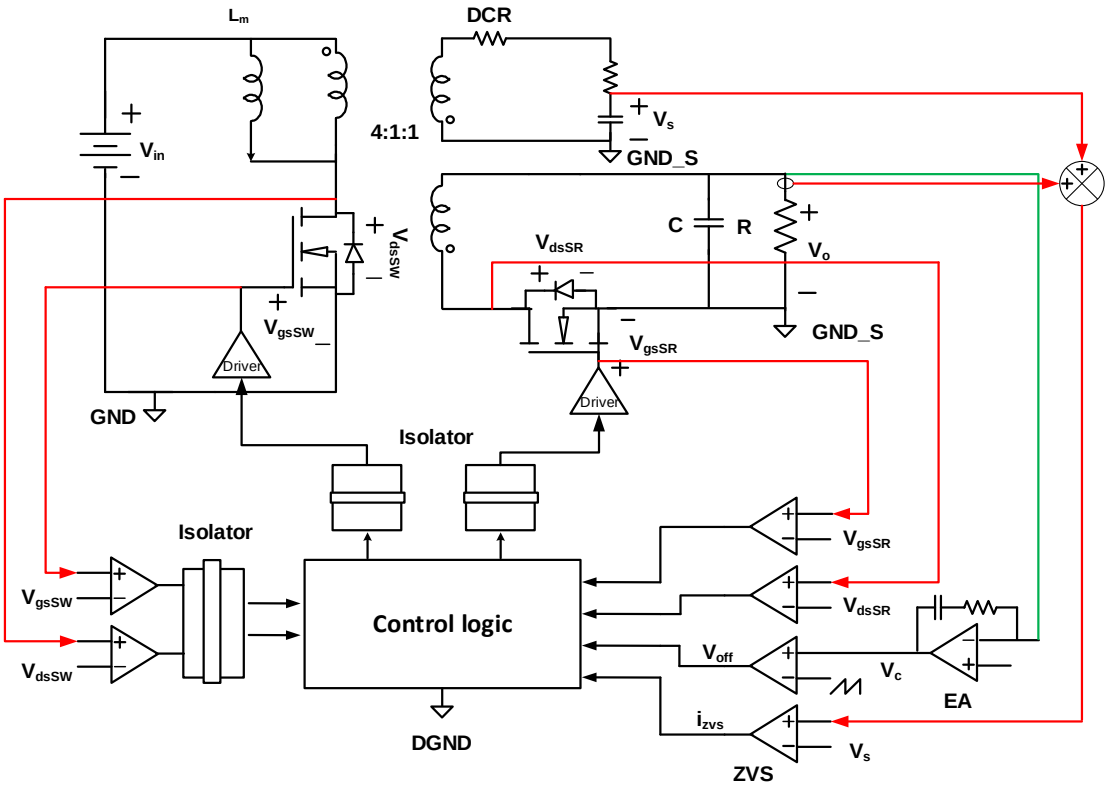
$$V_{gssr} = \bar{V}_{off}(V_{dssr} \bar{\imath}_{zvs} + \bar{V}_{dssw} i_{zvs}) \quad (5.4)$$

Table 5.7 Truth table of control logic of gate signal V_{gssr}

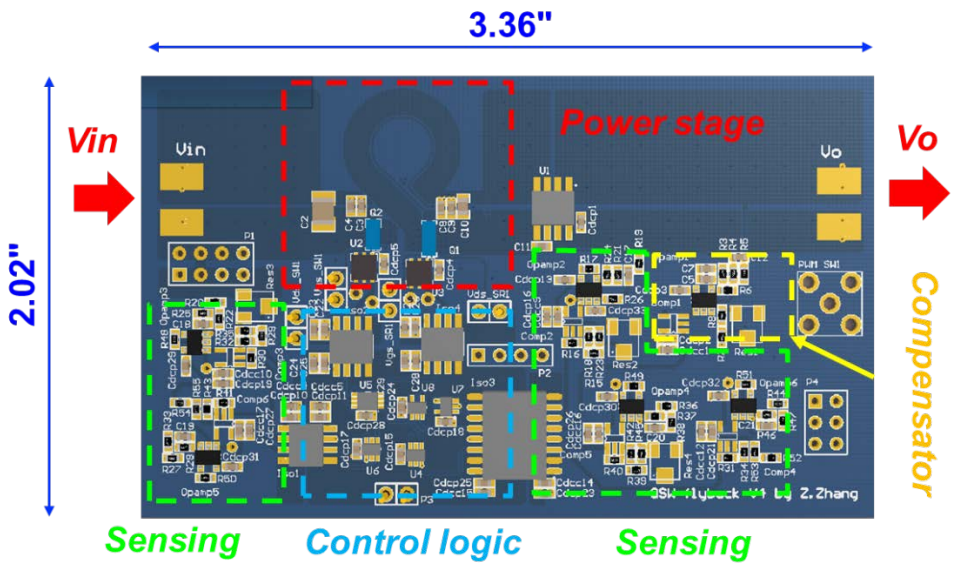
i_{zvs}	V_{off}	V_{dsSR_flag}	V_{gsSW}	V_{gsSR}
0	0	0	×	0
0	0	1	×	1
0	1	0	×	0
0	1	1	×	0
1	0	×	0	1
1	0	×	1	0
1	1	×	0	0
1	1	×	1	0

5.2.3 Experimental results

The magnetizing current is derived by adding ac and dc current together. Figure 5.18(a) shows the circuitry of DCR sensing to obtain the ac component of magnetizing current, and it also illustrates the other control block diagrams of voltage sensing for QSW flyback converter., A QSW flyback converter was built and shown in Figure 5.18(b) to verify the adaptive deadtime control. The key components used in prototype are listed in Table 5.8. The eGaN FETs EPC2012 (200 V) [4] and EPC 2001(100 V) [4] were selected as the input switch and the secondary SR respectively; 60V schottky diode (PMEG6030EP) [6] was connected in parallel with SR to reduce conduction loss.



(a)



(b)

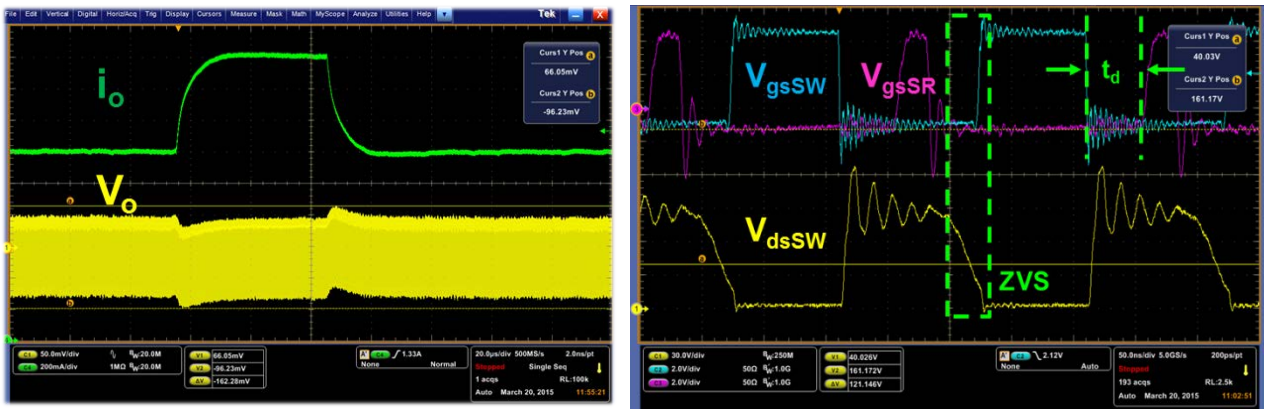
Figure 5.18. (a) Detailed control block diagram of QSW flyback converter and (b) Prototype of closed loop flyback converter.

Table 5.8 Key components of flyback topology shown in Figure 5.18

eGaN	*Schottky diode*	*Gate driver*
EPC2012, EPC2001	PMEG6030EP	LM5114
Comparator	*Amplifier*	*Schottky diode*
ADCMP600	AD8061	DFLS1200-7
Isolator	*Current source*	*NMOSFET*
Si8420, Si8410	LT3092	DMN2300U
Logic gate	*AND gate*	*Inverter gate*
74VC1G97	74LVC2G08	74LVC1GU04

With the voltage mode control, the load step between 50% and 75% of the full load is realized, and the waveforms of i_{out} and V_{out} are shown in Figure 5.19(a). Both switches can turn on softly by implementing the adaptive deadtime control. The waveforms of V_{gs} and V_{ds} are shown in Figure 5.19(b) at V_{in}=48V, V_o=12V, P_o=30W, and f=5MHz.

Because of the propagation delay of the comparator, isolator, gate driver and other logic gates listed in the Table 5.9 [7]-[9], the devices cannot turn on instantaneously and a delay happens (see in Figure 5.19(b)). A higher threshold voltage of V_{ds} in the comparator to detect the ZVS condition is applied to compensator the delay. If the turn-off current is very large, the resonant time to discharge the parasitic capacitance will be relatively small, which results in propagation delay that cannot be compensated. Especially for the SR with higher current on the secondary side, extra deadtime will cause huge conduction loss.



(a) (b)

Figure 5.19. (a) Transient response of 50%-75%-50% of full load and (b) V_{ds} and V_{gs} waveforms of QSW flyback converter at 5MHz.

Table 5.9 Propagation delay of components in test setup

Component Name	Part Number	Propagation delay (ns)
Comparator	ADCMP600	5
Gate driver	LM5114	15
Isolator	Si8420, Si8410	10
Logic gate	74VC1G97	2
AND gate	74LVC2G08	2
Inverter gate	74LVC1GU04	2

In order to quantify the issue of propagation delay at multi-megahertz frequency, the timing sequence of control signal to turn on synchronous rectifier is shown in Figure 5.20. Based on the control block diagram in Figure 5.18(a), when the output voltage is regulated to 12 V, the PWM signal V_{off} becomes zero. The input switch SW turns off after the delay time T_{delay_off} of

comparator and isolator. The drain-to-source voltage V_{dssr} of SR starts decreasing with $T_{resonant}$ time, which is usually less than 5 ns. The extra deadtime is the duration between the time when V_{dssr} reaches zero and the turn-on edge of SR. It includes the propagation delay of comparator, calculation of control block, delay of isolator and gate driver, which can be quantified as

$$T_{delay\_SR\_on} = t_{com} + t_{calc} + t_{iso} + t_{dr} \approx 36ns \tag{5.5}$$

Comparing to the resonant time of SR, it is impossible to compensate for the adaptive deadtime control at 5 MHz. A schottky diode has to be paralleled with SR to avoid large deadtime loss in this control scheme.

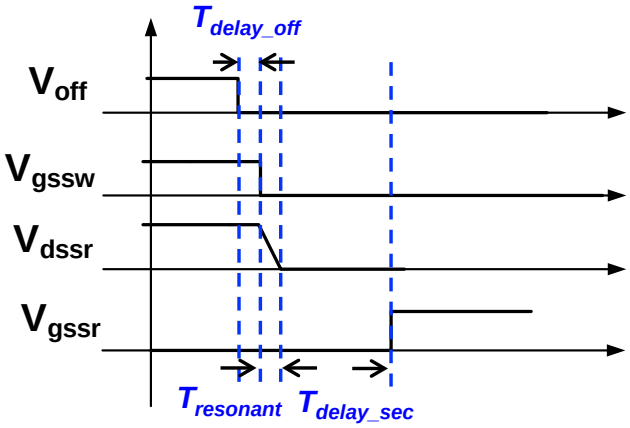


Figure 5.20. Timing of turn-on process of synchronous rectifier.

5.3 Proposed Variable Dead-time Control

The conventional adaptive deadtime control has several limitations at multi-megahertz frequency, including V_{ds} sensing, propagation delay and large deadtime loss etc. To overcome those issues, a variable deadtime control is proposed and illustrated in this section.

5.3.1 Control structure

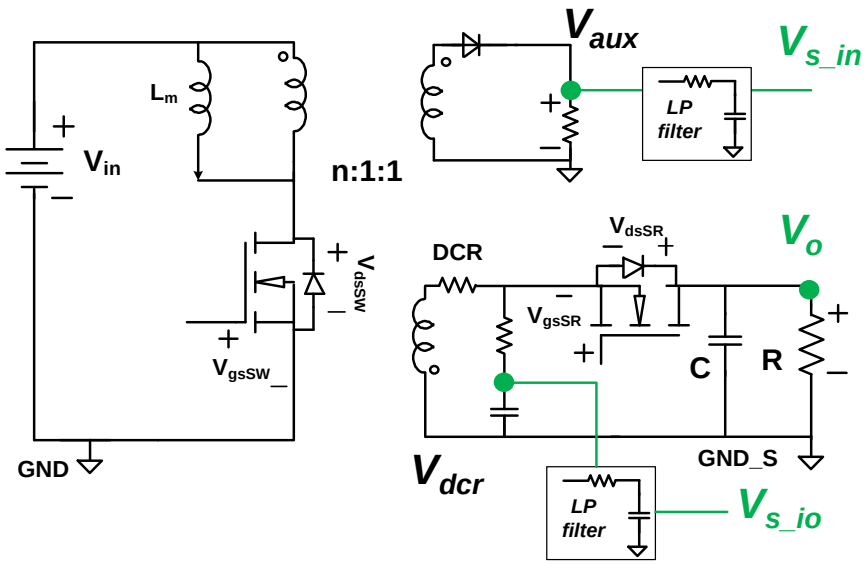


Figure 5.21. System diagram of QSW flyback converter with variable deadtime control.

Figure 5.21 shows the system diagram of QSW flyback converter with variable deadtime control including power stage, input voltage sensing circuits from an auxiliary winding, and dcr current sensing. Based on the steady-state model of QSW flyback introduced in Chapter 2, the resonant time of input switch SW is a function of input voltage and output current, which can be derived as a second-order interpolation and is shown in Figure 5.22.

$$t_{res\_sw} = C_0 + C_1 V_{in} + C_2 i_o + C_3 {i_o}^2 + C_4 V_{in} i_o \tag{5.6}$$

where C_0, C_1, C_2, C_3 and C_4 can be obtained from regression analysis. The deadtime should be controlled exactly to be equal to the resonant period to minimize the additional conduction loss from the reverse voltage drop of eGaN FETs. The resonant time of SR varies from 3 ns to 5 ns over the wide input and load range, so that the deadtime of SR can be simplified and kept constant as 5 ns.

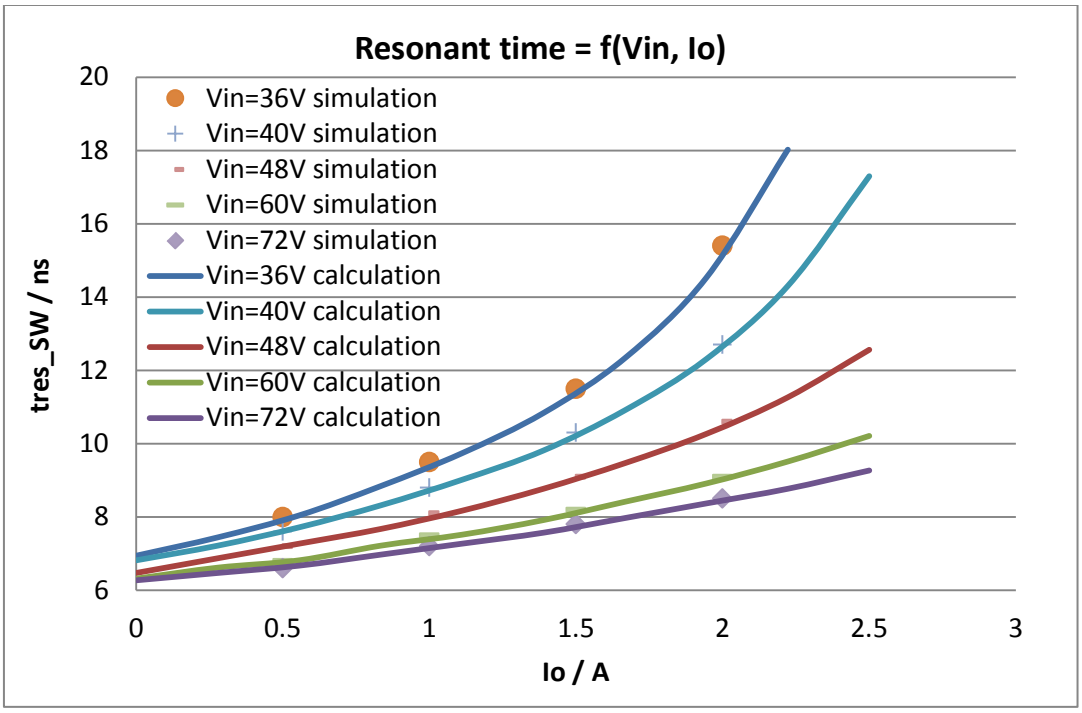
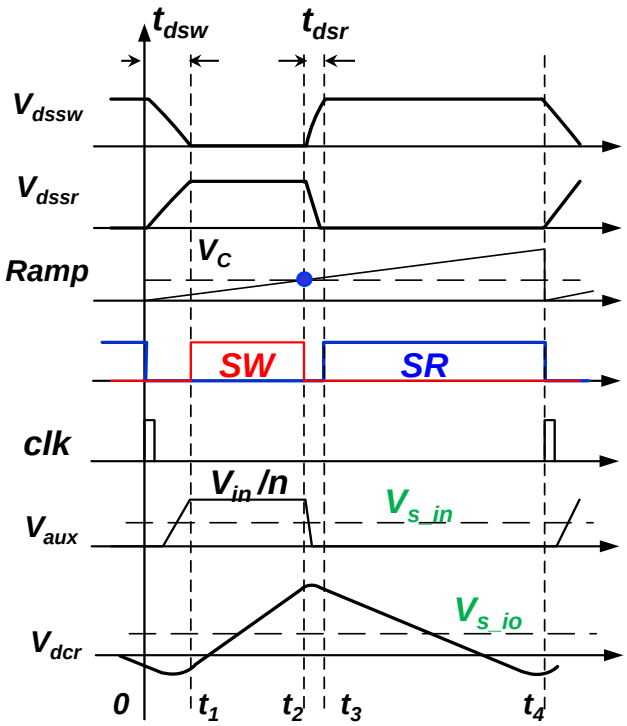
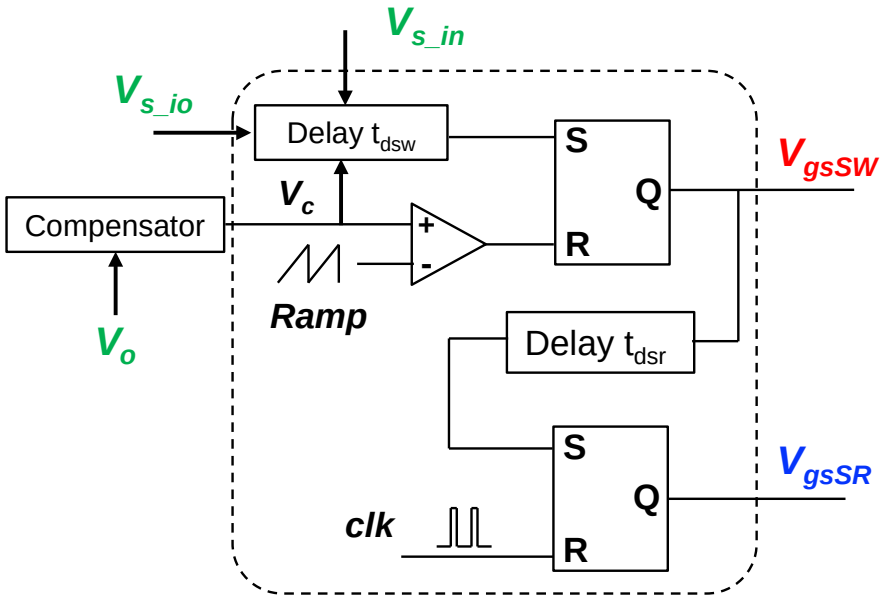


Figure 5.22. Resonant time of SW as a function of input voltage and output current.

The closed-loop system of QSW flyback converter is composed of a voltage regulator merging with a variable deadtime control loop. Figure 5.23(a) shows the typical waveforms of QSW flyback converter from Figure 5.21. The output voltage is regulated by the duty cycle of input switch SW, and the deadtime t_{dsw} between SR turning off and SW turning on is determined by certain input voltage and load current condition. A fixed deadtime t_{dsr} of 5 ns is used to turn on the SR, and the falling edge of gate drive is triggered by a clock signal of 5 MHz frequency. The detailed implementation of gate control for QSW flyabck converter is shown in Figure 5.23(b).



(a)

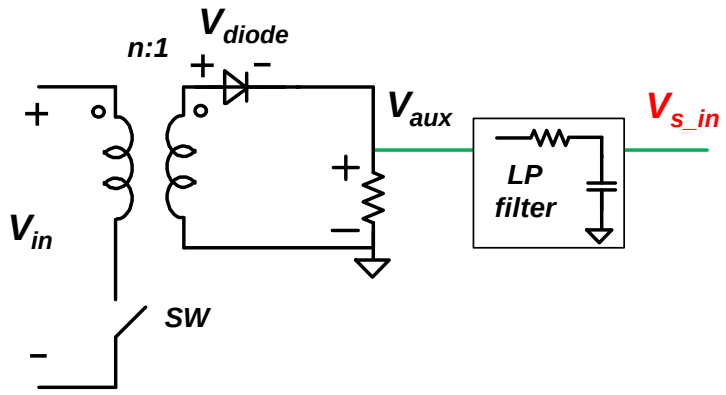


(b)

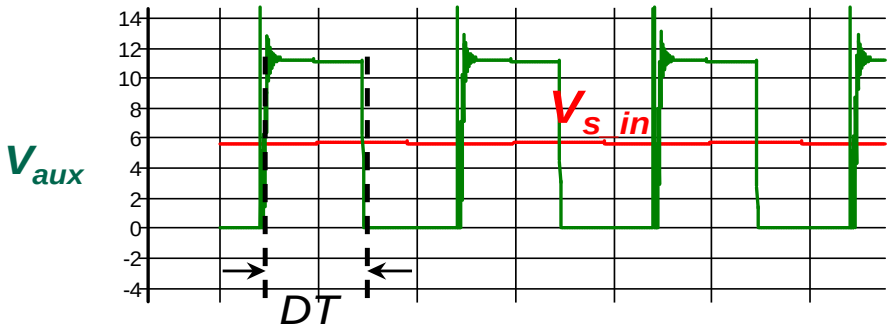
Figure 5.23. (a) Typical waveforms of QSW flyback converter shown in Figure 5.21 and (b) Block diagram of gate drive control.

5.3.2 Sensing circuit

There is no comparator in practical which can handle the voltage range of V_{ds} from 0 to 120V.A lossy resistive voltage divider has to be utilized in the approach of adaptive deadtime control. To avoid sensing the vulnerable drain-source voltage, the variable deadtime only requires the average signals of input voltage and output current.



(a)



(b)

Figure 5.24. (a) Voltage sensing using auxiliary windings and (b) Sensed input voltage waveforms in simulation.

An auxiliary winding with a diode rectifier is used to sense the input voltage as shown in Figure 5.24(a). When the input switch SW is on, V_{aux} equals to the reflected input voltage in the secondary side subtracting the voltage drop on the diode. V_{s_in} is the average value of V_{aux} after flowing through the low pass filter. By including the duty cycle D of SW (see in Figure 5.24(b)), the input voltage V_{in} can be calculated as

$$V_{in} = n\left(V_{s\_in}/D + V_{diode}\right) \tag{5.7}$$

A DCR sensing method [9] is applied and a RC network is paralleled with the secondary winding in order to sense the load current. By averaging the capacitor voltage, the information of dc load current can be obtained. As all the components are transferring to the secondary side, an equivalent T-model circuit of the transformer is shown in Figure 5.25(a). From Kirchoff's law, the voltage across capacitor can be deduced as

$$V_c(s) \cdot sRC + V_c(s) = i_m(s) \cdot sL_m + i_2(s) \cdot DCR_2 \tag{5.8}$$

$$V_c(s) = \frac{i_m(s) \cdot sL_m + i_2(s) \cdot DCR_2}{sRC + 1} \tag{5.9}$$

where DCR_2 is the dc resistance of the secondary winding. Based on equation (5.9), the load current can be derived when s is zero and is shown in Figure 5.25(b):

$$I_0 = i_2(0) = \frac{V_c(0)}{DCR_2} = \frac{V_{s\_io}}{DCR_2} \tag{5.10}$$

Since only dc load current is required, the time constant matching between RC network and magnetizing inductance and DCR_2 is not necessary. Compared to the previous deadtime control schemes, the sensing circuits are much easier to implement in the proposed variable deadtime control approach.

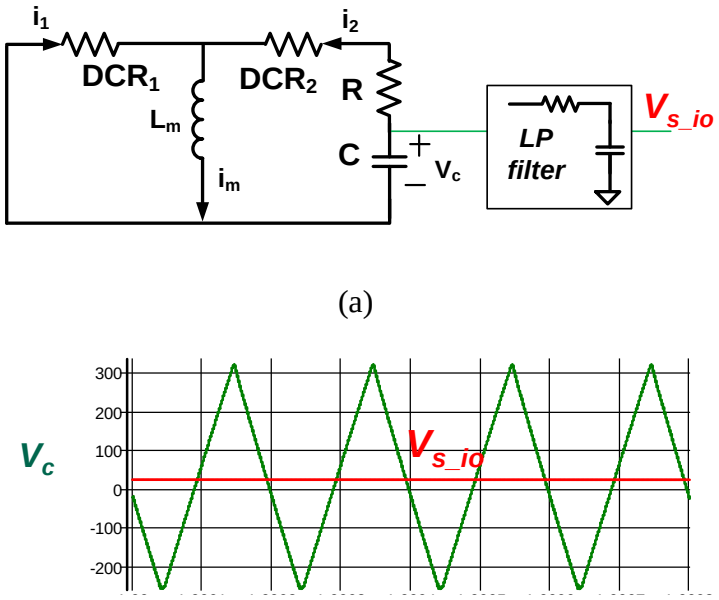


Figure 5.25. (a) Equivalent circuits of DCR current sensing for transformer and (b) Simulated current sensing waveforms.

5.3.3 Implementation of variable deadtime control

Since the controller cannot respond within one cycle of 200 ns when the converter is operated at 5 MHz, the variable deadtime control only ensures the right deadtime for steady state condition.

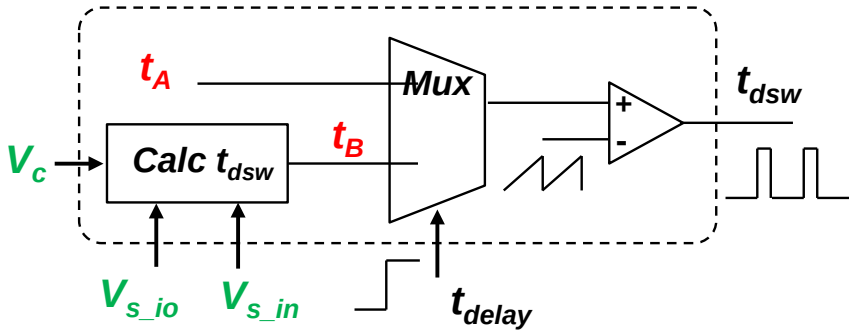


Figure 5.26. Block diagram of deadtime selection for SW.

During startup or transient period, the initial deadtime t_A is selected as shown in Figure 5.26. The deadtime t_B for the new operation condition needs to be calculated from (5.5), (5.7) and (5.10) after certain time including the calculation and propagation delay of the components in the loop. The switches may loss ZVS during the transient period, but it has little impact on the steady-state efficiency of the converter.

An example of input voltage variation from 48V to 36V is used to illustrate the mechanism of variable deadtime control, and the key waveforms of V_{in}, V_o, V_{ds} and V_{gs} are shown in Figure 5.27.

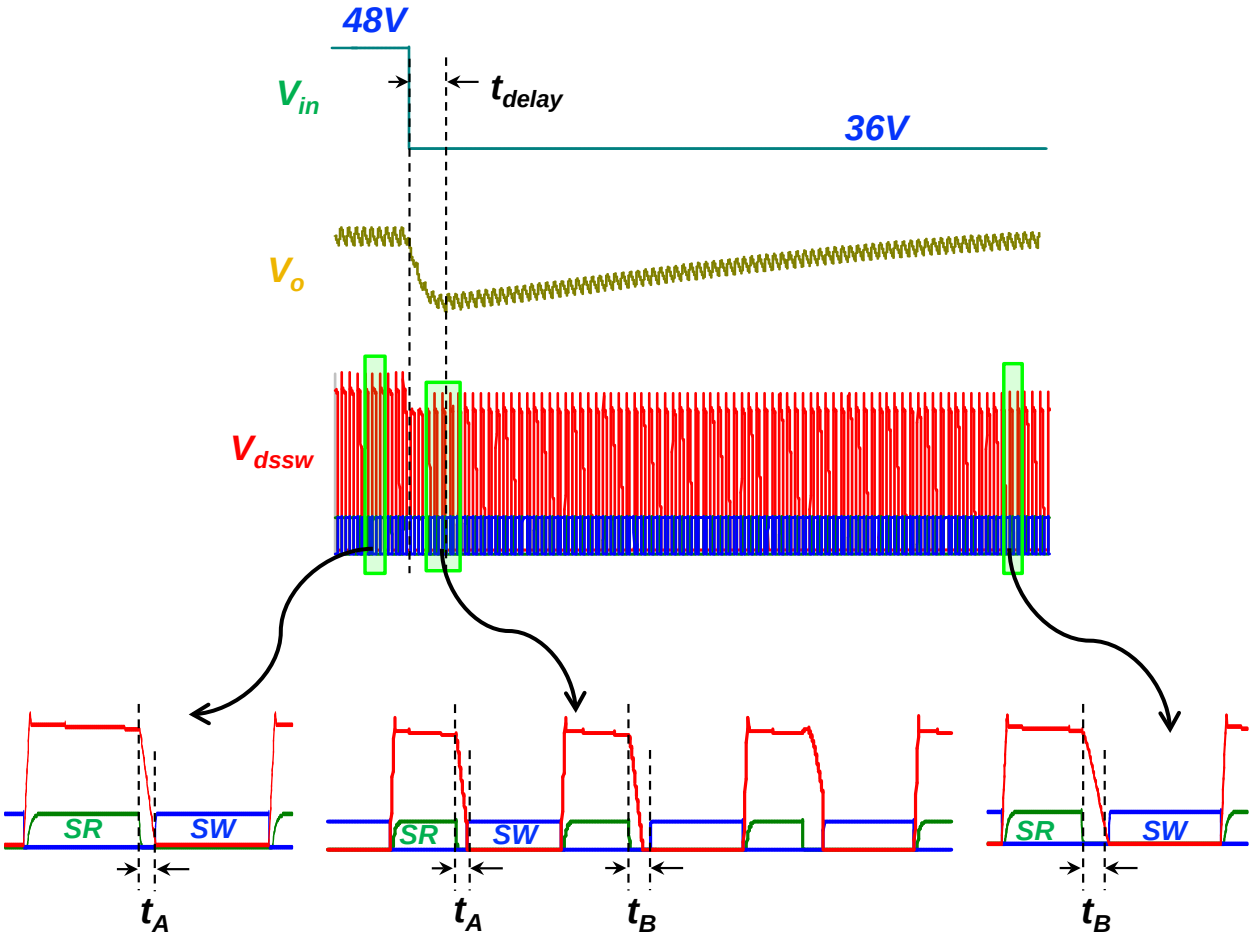
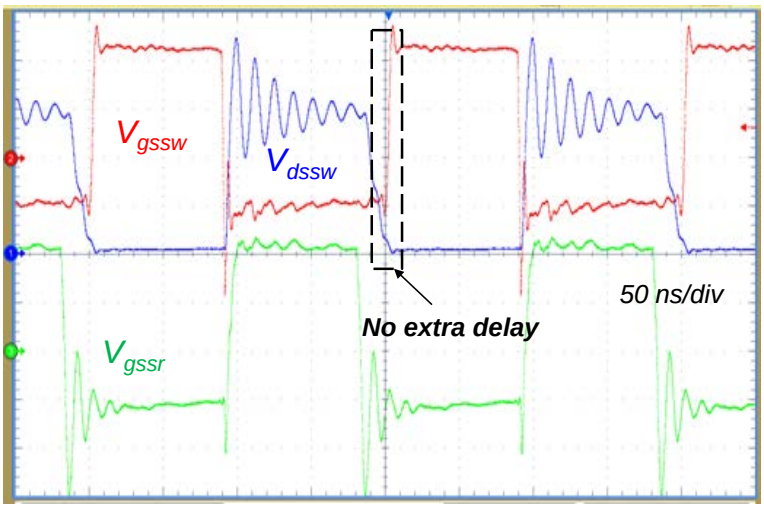
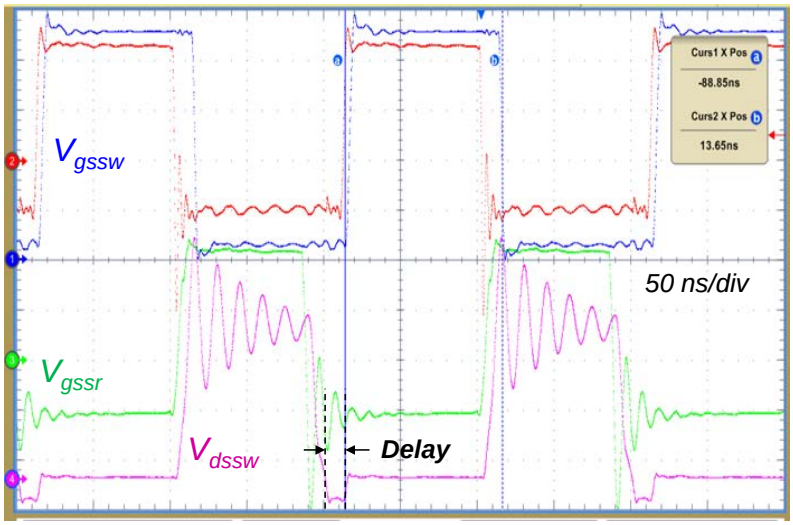


Figure 5.27. Key waveforms of V_{in}, V_o, V_{ds} and V_{gs} for the input step response.

For the input voltage of 48 V, load current of 2.5 A, and switching frequency of 5 MHz, the calculated deadtime between SR and SW is 12 ns. When V_{in} steps down from 48 V to 36 V, the new deadtime is obtained to be 20 ns after 5 cycles and the output voltage becomes stable after 50 cycles as shown in Figure 5.27.



(a)



(b)

Figure 5.28. The V_{gs} and V_{ds} waveforms (a) With and (b) Without perfect deadtime control at V_{in} = 48 V, I_o = 2.5 A, f = 5 MHz.

In order to evaluate the QSW flyabck converter with the proposed control schemes, gate driving signal is controlled with and without extra delay (see in Figure 5.28) to quantify the efficiency difference between fixed deadtime and variable deadtime control. The fixed deadtime is equal to 38 ns which is the half cycle of resonant period between parasitic capacitance and magnetizing inductance, and the extra delay is approximately 15 ns as shown in Figure 5.28(b). The efficiency comparison between the fixed deadtime and variable deadtime control is shown in Figure 5.29. The solid line is the measurement results with the optimized deadtime, and the dotted line is the results with constant delay for the SW. By using variable deadtime approach, the converter can save 0.3 W power loss, which improves the efficiency by 1 % at 30 W output condition.

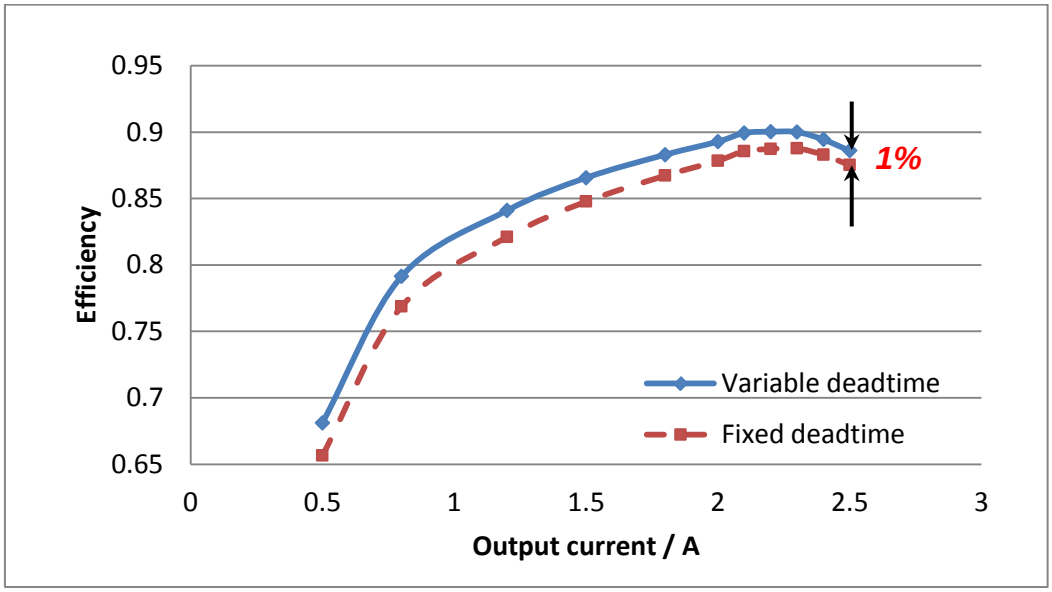


Figure 5.29. Efficiency comparison between variable deadtime control and fixed deadtime control.

In the future, a microcontroller such as TMS320F28075 can be implemented to realize the variable deadtime control. The F2807x is a 32-bit floating-point microcontroller based on TI's

industry-leading C28x core. It has 100 kB total RAM, three internal 12-bit ADCs and the CPU frequency of 120 MHz, which enables the controller to calculate and update the deadtime within one microsecond for input or load step response. For real cost-sensitive application, smart analog gate driver chips should be a solution for high frequency converter with deadtime control schemes.

5.4 Summary

A prototype of 30 W QSW flyback converter was fabricated to validate the theoretical analysis. Especially for the common source inductance, the layout of gate loop needs to be minimized to avoid the false turn on issue at 5 MHz switching frequency. To reduce the conduction during deadtime, an adaptive deadtime control method was implemented and several limitations including V_{ds} sensing and propagation delay are detected at multi-megahertz frequency. A variable deadtime control was proposed and thoroughly illustrated in this section to overcome those issues. Based on the theoretical analysis, the total efficiency can be improved by 1% at 30 W output condition.

5.5 Reference

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Chapter 6 Conclusion and Future Work

6.1 Conclusion

With the fast development of telecom, computer, and network systems, it is desired to reduce both power consumption and volume. The emerging gallium nitride (GaN) power device technology which exhibits better performance figure of merits than the existing silicon devices provides a good opportunity to further push the switching frequency. A high efficiency, high power density and high bandwidth flyback converter is promising for PoE application, but a host of other issues, such as switching losses, high-frequency magnetic losses, layout parasitics, and the gate driving circuit also challenge the hypothesis that the power density of the flyback converter can be improved by increasing the switching frequency from hundreds of kilohertz to multiple megahertz with the same efficiency. This work is to evaluate the performance of flyback converter such as the limitation of switching frequency and efficiency by using GaN FETs. The design trade-off between sizes, losses, thermal and dynamic performance needs to be identified.

This dissertation started with the discussion of soft-switching techniques, since it has to be utilized at multi-megahertz even with GaN FETs which has much better performance figure of merits. Quasi-square-wave flyback converter was selected to be the topology, and a charge based steady-state model was developed by considering nonlinear capacitance. The circuit parameter of magnetizing inductance can be designed to guarantee zero-voltage switching for the entire input and load range; and device size can be selected to optimize the total efficiency. The timing of the converter can also be obtained for control with this model.

Since the coupled inductor occupies approximately 30% of the printed circuit board, it is critical to increase the overall power density of the flyback converter by reducing the magnetic core size. A design methodology for selecting a minimum core volume for an inductor or coupled inductors with a significant ac flux swing was presented. At the same time, the system must stay within the loss or thermal constraints. An iterative semi-numerical approach with FEA tool is applied for winding loss calculation when proximity and fringing effect is significant. The quasi-square-wave (QSW) flyback converter was fabricated and verified by experiment. The planar coupled inductors with a size of ER 18×10 mm^2 were designed with the leakage inductance of 30 nH. ZVS is achieved for both switches, and the peak efficiency is 90.6% up to 30 W. With the similar power level and efficiency, the power density is 14% better than state-of-the-art flyback converter. By designing the converter to operate at different frequencies, the relationships between the size of magnetic core, frequency, loss and temperature of the inductor were studied. To further improve the power density of the converter, a better cooling method is required to dissipate the extra heat for a smaller transformer.

A modified CCM small signal model of QSW converter was derived to explain the double-pole splitting phenomenon and a small-signal damping resistor was added to analytically quantify the damp effect of control-to-output transfer function. The impacts of the deadtime, input voltage, and output power on the control-to-output transfer function of the power stage were analyzed in details with this equivalent circuit. The model can also simplify and speed up the design process of compensation network. By pushing the switching frequency to be approximately 16 times higher compared to commercial flyback converter, the peak derivation is approximate 25 times smaller, and the settling time is also reduced significantly for the 50-75-50% of load-step response.

The work also studied the issue of large dead-time loss caused by reverse voltage drop from eGaN. A variable deadtime control scheme was proposed for high frequency isolated converter. Comparing to conventional adaptive deadtime control, the vulnerable drain-source voltage is not required to sense, and the propagation delay for deadtime calculation is not critical in the proposed control method. Comparing to the most popular fixed deadtime control, the total efficiency can be improved by 1% at full load based on the theoretical analysis.

6.2 Future work

The emerging GaN devices show promising future for high switching frequency and high power density in the converter. There are still some remaining research opportunity can be further explored that are related to this work.

First, to simplify the driving loop design and provide reliable driving signal at high frequency, intelligent gate drive chips can be a good direction. By integrating GaN FETs, gate driver and control IC, the gate loop inductance is minimized and the propagation delay in the control loop can be significantly reduced.

Second, in order to fully implement the benefit from GaN FETs, the passive components especially for magnetics need to take more effort. Since the development of high-frequency magnetic material is a long-term research, custom magnetic structure is an alternative way. With the customized magnetic design, such as special core structures or the placement of airgap, the power density can be further improved.

The thermal management also needs to be taken into consideration, especially for the small LGA or BGA package of enhancement mode GaN from EPC. The modeling of thermal impedance for eGaN FETs and the planar magnetic components needs to be addressed in more

details in the future. It is also necessary to develop new cooling methods or novel structure of heat sink for GaN application to dissipate extra loss and achieve high power density.

Appendix A Charge Based Circuit Model for QSW Flyback Converter

Based on the steady-state model of QSW flyback converter, the attached matlab code helps to design the value of magnetizing inductance to ensure zero-voltage switching for entire input and load range. The steady-state voltage and current waveforms can be plotted with the designed inductance.

```
% ============================================================

% Initialization %

Lm0=0.85e-6;


Vin=48;

Vo=12;

n=4;

io=2.5;

fs=5e6;



%%%%%% EPC2012

a=3.75e17;

b=5.16e9;
```

```
%%%%%% EPC2001

x=2.3e16;

y=5.86e8;


Q1_init=(-b+(b^2+4*a*(Vin+n*Vo)).^0.5)/2/a;

Q2_init=(-y+(y^2+4*x*(Vin/n+Vo)).^0.5)/2/x;


%%%%% linear cap charge balance

% b=(Vin+n*Vo)/Q1_init

% a=0

% y=(Vin/n+Vo)/Q2_init

% x=0


% %%%%%% linear cap energy balance

% b=(Vin+n*Vo)^2/2/(3.93e-11*(Vin+n*Vo)^2+2.73e-9*(Vin+n*Vo)-2.35e-8)

% a=0

% y=(Vin/n+Vo)^2/2/(2.46e-10*(Vin/n+Vo)^2+9.34e-9*(Vin/n+Vo)-4.98e-8)

% x=0

% % %

% Q1_init=(Vin+n*Vo)/b;
```

```
% Q2_init=(Vin/n+Vo)/y;
 % %%%%%% linear cap datasheet
% b=1/0.064e-9;
% a=0
% y=1/0.43e-9;
% x=0
%
% Q1_init=(Vin+n*Vo)/b;
% Q2_init=(Vin/n+Vo)/y;

for k=1:4
    deltaLm=0.05e-6;
    Lm=-deltaLm*(k-1)+Lm0;

ilm_init=-5*sqrt(((Vin+n*Vo)*Q1_init-(Vin/n+Vo)*Q2_init)/Lm)
if ((Vin+n*Vo)*Q1_init-(Vin/n+Vo)*Q2_init<0)
    fprintf('Error: no energy.\n');
    ilm_init=0;
end

deltat=1e-9;
```

```
size=200;


for j=1:50000
    deltai=0.001;
    ilm0(j)=ilm_init+deltai*(j-1);


    if (ilm0(j)>=0)
        flag1=0;
        fprintf('Error: positive current.\n');
        break;
    end


    %%%%%% Interval 1
    [ theta1, ilm1, time_profile, ilm_profile, Q1_profile, Q2_profile, V1_profile, V2_profile, flag ]
= resonance_interval(ilm0(j), Vin, n, Vo, a, b, x, y, Lm, Q1_init );


    if (flag==1||flag==2||flag==3)
        continue
    end


    if (flag==100)
```

```
        theta1(j)=theta1;
        ilm1(j)=ilm1;
        interval1(j)=length(time_profile);
        for t=1:interval1(j)
            interval1_time(j,t)=time_profile(t);
            interval1_ilm(j,t)=ilm_profile(t);
            interval1_Q1(j,t)=Q1_profile(t);
            interval1_Q2(j,t)=Q2_profile(t);
            interval1_V1(j,t)=V1_profile(t);
            interval1_V2(j,t)=V2_profile(t);
        end
    end

    %%%%%% Interval 4
    ilm3(j)=sqrt(2*io*Vo/Lm/fs+ilm0(j).^2);
    theta4(j)=Lm/n/Vo*(ilm3(j)-ilm0(j));
%     size=20;
        for t=1:size
            interval4_time(j,t)=theta4(j)/size*t;
            interval4_ilm(j,t)=ilm3(j)-n*Vo/Lm*theta4(j)/size*t;
            interval4_Q1(j,t)=Q1_init;
```

```
        interval4_Q2(j,t)=0;
        interval4_V1(j,t)=Vin+n*Vo;
        interval4_V2(j,t)=0;
    end

%%%%%% Interval 3
[ theta3, ilm2, time_profile3, ilm_profile3, Q1_profile3, Q2_profile3, V1_profile3,
V2_profile3, flag ] = resonance_interval(-ilm3(j), Vin, n, Vo, a, b, x, y, Lm, Q1_init );

if (flag==1||flag==2||flag==3)
    continue
end

if (flag==100)
    theta3(j)=theta3;
    ilm2(j)=-ilm2;
    ilm_profile3=fliplr(ilm_profile3);
    Q1_profile3=fliplr(Q1_profile3);
    Q2_profile3=fliplr(Q2_profile3);
    V1_profile3=fliplr(V1_profile3);
    V2_profile3=fliplr(V2_profile3);
```

```
    interval3(j)=length(time_profile3);
    for t=1:interval3(j)
        interval3_time(j,t)=time_profile3(t);
        interval3_ilm(j,t)=-ilm_profile3(t);
        interval3_Q1(j,t)=Q1_profile3(t);
        interval3_Q2(j,t)=Q2_profile3(t);
        interval3_V1(j,t)=V1_profile3(t);
        interval3_V2(j,t)=V2_profile3(t);
    end
end

%%%%%% Interval 2
theta2(j)=(ilm2(j)-ilm1(j))*Lm/Vin;
    for t=1:size
        interval2_time(j,t)=theta2(j)/size*t;
        interval2_ilm(j,t)=ilm1(j)+Vin/Lm*theta2(j)/size*t;
        interval2_Q1(j,t)=0;
        interval2_Q2(j,t)=Q2_init;
        interval2_V1(j,t)=0;
        interval2_V2(j,t)=Vin/n+Vo;
    end
```

```
error(j)=1/fs-theta1(j)-theta2(j)-theta3(j)-theta4(j);
if (abs(error(j))<0.01/fs)
    flag1=1;
    time_final1=[ interval1_time(j,1:interval1(j)) ];
    time_final2=[ theta1(j)+interval2_time(j,1:size) ];
    time_final3=[ theta1(j)+theta2(j)+interval3_time(j,1:interval3(j)) ];
    time_final4=[ theta1(j)+theta2(j)+theta3(j)+interval4_time(j,1:size) ];

    ilm_final1=[ interval1_ilm(j,1:interval1(j)) ];
    ilm_final2=[ interval2_ilm(j,1:size) ];
    ilm_final3=[ interval3_ilm(j,1:interval3(j)) ];
    ilm_final4=[ interval4_ilm(j,1:size) ];

    Q1_final1=[ interval1_Q1(j,1:interval1(j)) ];
    Q1_final2=[ interval2_Q1(j,1:size) ];
    Q1_final3=[ interval3_Q1(j,1:interval3(j)) ];
    Q1_final4=[ interval4_Q1(j,1:size) ];

    Q2_final1=[ interval1_Q2(j,1:interval1(j)) ];
    Q2_final2=[ interval2_Q2(j,1:size) ];
```

```
Q2_final3=[ interval3_Q2(j,1:interval3(j)) ];

Q2_final4=[ interval4_Q2(j,1:size) ];


V1_final1=[ interval1_V1(j,1:interval1(j)) ];

V1_final2=[ interval2_V1(j,1:size) ];

V1_final3=[ interval3_V1(j,1:interval3(j)) ];

V1_final4=[ interval4_V1(j,1:size) ];


V2_final1=[ interval1_V2(j,1:interval1(j)) ];

V2_final2=[ interval2_V2(j,1:size) ];

V2_final3=[ interval3_V2(j,1:interval3(j)) ];

V2_final4=[ interval4_V2(j,1:size) ];


time_final=[ time_final1 time_final2 time_final3 time_final4 ];

ilm_final=[ ilm_final1 ilm_final2 ilm_final3 ilm_final4 ];

ilm_pri=[ ilm_final1 ilm_final2 zeros(1,length(ilm_final3)) zeros(1,length(ilm_final4)) ];

ilm_sec=[ zeros(1,length(ilm_final1)) zeros(1,length(ilm_final2)) ilm_final3 ilm_final4 ];

Q1_final=[ Q1_final1 Q1_final2 Q1_final3 Q1_final4 ];

Q2_final=[ Q2_final1 Q2_final2 Q2_final3 Q2_final4 ];

V1_final=[ V1_final1 V1_final2 V1_final3 V1_final4 ];

V2_final=[ V2_final1 V2_final2 V2_final3 V2_final4 ];
```

```
        break
    end


end
    if (flag1==1)
        Lm_value(k)=Lm
        duty(k)=time_final3(1)*fs
        duty1(k)=(time_final3(1)-time_final2(1))*fs
        iswoff(k)=ilm_final3(1)
        isroff(k)=abs(ilm_final1(1))*n
        ipp(k)=max(ilm_final)-min(ilm_final);
        irms_ilm(k)=rms(ilm_final);
        irms_pri(k)=rms(ilm_pri)
        irms_sec(k)=rms(ilm_sec)*n
        iswdead(k)=abs(ilm_final2(1))
        isrdead(k)=ilm_final4(1)
    else
        break
    end
end
```

```
if (flag1==1)
%     % Charge waveform
%     subplot(3,1,1)
%     plot(time_final*1e9,ilm_final)
%     grid on
%     hold on
%     subplot(3,1,2)
%     plot(time_final*1e9,Q1_final*1e9)
%     grid on
%     hold on
%     subplot(3,1,3)
%     plot(time_final*1e9,Q2_final*1e9)
%     grid on
%     hold on

%     % Voltage waveform
    figure
    subplot(3,1,1)
    plot(time_final*1e9,ilm_final)
    grid on
    hold on
```

```
    subplot(3,1,2)
    plot(time_final*1e9,V1_final)
    grid on
    hold on
    subplot(3,1,3)
    plot(time_final*1e9,V2_final)
    grid on
    hold on
%
 % Simulation waveform Vdssw_Vdssr_0.98u
%    subplot(2,1,1)
%    plot(time*1e9,Vdssw)
%    grid on
%    hold on
%    subplot(2,1,2)
%    plot(time*1e9,Vdssr)
%    grid on
%    hold on

%    % Voltage waveform
%    subplot(2,1,1)
```

```
%     plot(time_final*1e9,V1_final)
%     grid on
%     hold on
%     subplot(2,1,2)
%     plot(time_final*1e9,V2_final)
%     grid on
%     hold on
% %
%     t1=time_final2(1)
%     t2=time_final3(1)
%     t3=time_final4(1)
%     t4=1/fs
%
%     tsw=time_final2(length(time_final2))-time_final2(1);
%     td=time_final3(length(time_final3))-time_final3(1);
%     tsr=1/fs-time_final4(1);
end
% ================================================================

% ================================================================

      function [ resonance_time, ilm_residual, time_profile, ilm_profile, Q1_profile, Q2_profile,
V1_profile, V2_profile, flag ] = resonance_interval( ilm_init, Vin, n, Vo, a, b, x, y, Lm, Q1_init )
```

```
% calculate resonant time and inductor current
%   Detailed explanation goes here
    deltat=1e-10;
    flag=3;


    for i=1:1000
        if (i==1)
            ilm(i)=ilm_init;
            v1(i)=Vin+n*Vo;
            Q1(i)=Q1_init;
            v2(i)=0;
            Q2(i)=0;
            t(i)=0;
            area(i)=0;
        else
            ilm(i)=ilm(i-1)+(Vin-v1(i-1))*deltat/Lm;
            area(i)=area(i-1)+(ilm(i)+ilm(i-1))*deltat/2;
            qa=a/n^2+n*x;
            qb=2*a*Q1(1)/n+2*a*area(i)/n+b/n+n*y;
            qc=a*Q1(1).^2+a*area(i).^2+2*a*area(i).*Q1(1)+b*area(i)+b*Q1(1)-Vin-n*Vo;
            if (qa==0)
```

```
    Q2(i)=-qc./qb;
else
    Q2(i)=(-qb+(qb.^2-4*qa*qc).^0.5)/2/qa;
end
if (qb.^2-4*qa*qc<0)
    fprintf('Error: no solution.\n');
    error=1;
    flag=0;
    break
end
v2(i)=x*Q2(i).^2+y*Q2(i);
Q1(i)=area(i)+Q1(1)+Q2(i)/n;
v1(i)=a*Q1(i).^2+b*Q1(i);
t(i)=t(i-1)+deltat;
if (t(i)>=200e-9)
    fprintf('Error: too much time.\n');
    error=2;
    flag=0;
    break
elseif (Q1(i)<=0)
    flag=1;
```

```
            resonance_time_est=t(i);
            ilm_residual_est=ilm(i);
            break
        end
    end
end

if (flag==1)
    resonance_time=resonance_time_est;
    ilm_residual=ilm_residual_est;
    time_profile=t;
    ilm_profile=ilm;
    Q1_profile=Q1;
    Q2_profile=Q2;
    V1_profile=v1;
    V2_profile=v2;
    flag=100;
elseif (flag==0)
    resonance_time=0;
    ilm_residual=0;
    time_profile=0;
```

```
            ilm_profile=0;
            Q1_profile=0;
            Q2_profile=0;
            V1_profile=0;
            V2_profile=0;
            flag=error;
        elseif (flag==3)
            resonance_time=0;
            ilm_residual=0;
            time_profile=0;
            ilm_profile=0;
            Q1_profile=0;
            Q2_profile=0;
            V1_profile=0;
            V2_profile=0;
            flag=3;
        end
    end
% ============================================================
```

Appendix B Kgac Methodology for Magnetic Design

The geometrical specifications, A_p and K_g constants of commercial ER, EI cores are listed in the following tables.

Table B.1 Geometrical specifications, Ap and Kg constants of commercial ER cores

ER	A_c (mm^2)	W_A (mm^2)	MLT (mm)	V_e (mm^3)	A_p (mm^4)	K_g (mm^5)
906	8.47	2.80	11.00	120	23.72	18.26
1126	11.9	2.80	13.35	174	33.32	29.70
1426	17.6	5.10	15.08	333	89.76	104.76
1826	30.2	15.00	19.48	667	453.00	702.29
2313	50.2	19.50	25.13	1340	978.90	1955.46
2517	89.7	31.72	34.56	2370	2845.28	7384.90
2521	100	52.00	34.56	4145	5200.00	15046.30
3021	108	73.44	34.56	4970	7931.52	24786.00

Table B.2 Geometrical specifications, Ap and Kg constants of commercial EI cores

	A_c (mm^2)	W_A (mm^2)	MLT (mm)	V_e (mm^3)	A_p (mm^4)	K_g (mm^5)
E9.5	8.47	1.40	16.65	100.38	11.85	6.03
E11	11.9	1.40	19.24	149.70	16.65	10.30
E14.5	17.6	2.55	25.76	306.44	44.90	30.68
E18	30.2	7.50	30.94	604.13	226.50	221.05
E23	50.2	9.75	40.06	1250.00	489.50	613.47

Notes: $A_p = A_c W_A,\ K_g = (A_c^2 W_A)/MLT$

For the iterative Kgac method, ac winding loss can be simulated from Ansys/Maxwell and the ratio of Rac/Rdc can be derived. The attached matlab code is used to plot the critical design curve of total magnetic loss and core volume. After several iterations, the volume of magnetic core can be determined.

```
% ============================================================
%    Initialization     %
clc
 rho=1.724e-8;    idc=2.5;
Vin=48;     n=4;    u0=4e-7*pi;


% ac resistor  %
alpha1=1; alpha2=1;


% 5MHz 4F1  %
f=5e6;
D=0.45;
ur=80;
L=0.85e-6;
beta=2.0556;
kfe=43.0746*5e6^1.1836;
alpha1=4.23; alpha2=4.74;          %  % 5MHz alpha   EI11 n=4 lg=0.095 1st iteration
```

```
alpha1=4.8; alpha2=5.17;          %  % 5MHz alpha   EI18 2st iteration


% % 3MHz 3F5  %
% f=3e6;
% D=0.469;
% ur=650;
% L=1.59e-6;
% beta=2.0562;
% kfe=1242875000;
% alpha1=5.31; alpha2=4.28;         %  % 3MHz alpha   EI11 n=4 lg=0.12 1st iteration
% alpha1=5.92; alpha2=4.61;         %  % 3MHz alpha   EI18 2st iteration


% 1MHz 3F45  %
% f=1e6;
% D=0.485;
% ur=900;
% L=5.64e-6;
% beta=2.6385;
% kfe=802711000;
% alpha1=4.56; alpha2=3.71;         %  1MHz alpha   EI 14.5 n=8 lg=0.19 1st iteration
% alpha1=4.57; alpha2=4.62;         %  % 1MHz alpha   EI18 2nd iteration
```

```
% % 0.3MHz 3C96  %
% f=0.3e6;
% D=0.493;
% ur=2000;
% L=20.57e-6;
% beta=2.52204;
% kfe=142939000;
% alpha1=2.736; alpha2=3.58;          %  300k alpha  EI18 n=8 lg=0.068  1st
% alpha1=3.387; alpha2=4.4;           %  300k alpha  EI23 n=8 lg=0.12  2st

d=1-D;

Bac=30e-3;
Bac=10e-3:1e-3:50e-3;

%--------EI-------
% a1=2.3472;      a2=1.964;     Ku=0.07;
a1=1.5333;      a2=2.021;     Ku=0.11;
```

```
K2=(idc^2/(n^2*d^2)*(D^0.5*(D+alpha1*d)+d^0.5*(d+alpha2*D))+(Vin*D/L/f)^2/12*(alpha1
*D^0.5+alpha2*d^0.5))*rho*(Vin*D/2/f)^2*(D^0.5+d^0.5)/Ku./Bac.^2;


K1=kfe*Bac.^(beta)*8/pi^2;

Ve=(K1/a1/a2./K2).^(-1/(a2+1));


Ptotal=K1.*Ve+a1*K2.*Ve.^(-a2);


%-----------------------------------------------
% %   EI9.5   %
% Wa=3.2e-6;
% Wa=1.4e-6;      Ac=8.47e-6;     MLT=16.65e-3;      Volume=100e-9;
% % Volume95=Ac*lm
% %   EI11  %
% Wa=3.338e-6;
% Wa=1.4e-6;      Ac=11.9e-6;     MLT=19.24e-3;     Volume=149.7e-9;
% % Volume11=Ac*lm
% % %   EI14.5   %
% Wa=5.43e-6;
% Wa=2.55e-6;      Ac=17.6e-6;     MLT=25.76e-3;     Volume=306e-9;
% % % Volume145=Ac*lm
```

```
% %   EI18  %
% Wa=7.52e-6;
% Wa=7.5e-6;      Ac=30.2e-6;     MLT=30.94e-3;     Volume=604e-9;
% % Volume18=Ac*lm
% %   EI23   %
% Wa=9.76e-6;
% Wa=9.75e-6;      Ac=50.2e-6;     MLT=40.06e-3;     Volume=1250e-9;
% % Volume23=Ac*lm


%--------------------------------
n11=Vin*D/(2*f*Ac*Bac)
n22=round(n11/4);
n11=n22*4


B=Vin*D/f/2/n11/Ac
Pc=kfe*B^beta*Volume*8/pi^2


% %  winding loss  %
R1=rho*n11^2*MLT/Ku/Wa*(D^0.5+d^0.5)/D^0.5;
R2=rho*n22^2*MLT/Ku/Wa*(D^0.5+d^0.5)/d^0.5;
```

```
ilmdc=idc/n/d;

ilmac=Vin*D/(L*f);

ilmrms=(ilmdc^2+ilmac^2/12)^0.5;

il1rms=D^0.5*ilmrms;

il2rms=d^0.5*n*ilmrms;

il1dc=idc*D/n/d;

il1acrms=(il1rms^2-il1dc^2)^0.5;

il2acrms=(il2rms^2-idc^2)^0.5;


Pw=(il1dc^2+il1acrms^2*alpha1)*R1+(idc^2+il2acrms^2*alpha2)*R2


Pt=Pc+Pw


% %  Temperature rise EI %

a3=20.077;

a4=0.677;


At=a3*(Volume)^a4;

deltaT=(Pt/At/10)^0.833

% ============================================================
```