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CPES
Center for Power Electronics Systems

2012 CPES ANNUAL REPORT
VIRGINIA TECH · BLACKSBURG, VIRGINIA

Center for Power Electronics Systems

2012 CPES ANNUAL REPORT
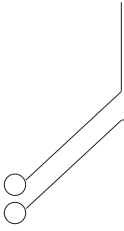
VIRGINIA TECH · BLACKSBURG, VIRGINIA

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INTRODUCTION

The Center for Power Electronics Systems at Virginia Tech is a research center dedicated to improving electrical power processing and distribution that impact systems of all sizes – from battery – operated electronics to vehicles to regional and national electrical distribution systems.

Our mission is to provide leadership through global collaborative research and education for creating advanced electric power processing systems of the highest value to society.

CPES, with annual research expenditures about $4-5 million US dollars, has a worldwide reputation for its research advances, its work with industry, and its many talented graduates. From its background as an Engineering Research Center for the National Science Foundation during 1998 - 2008, CPES has continued to work towards making electric power processing more efficient and more exact in order to reduce energy consumption.

Power electronics is the "enabling infrastructure technology" that promotes the conversion of electrical power from its raw form to the form needed by machines, motors and electronic equipment. Advances in power electronics can reduce power conversion loss and in turn increase energy efficiency of equipment and processes using electrical power. This results in increased industrial productivity and product quality. With widespread use of power electronics technology, the United States would be able to cut electrical energy consumption by 33 percent. This energy savings in the United States alone is estimated to be the equivalent of output from 840 fossil fuel based generating plants. This savings would result in enormous economic, environmental and social benefits.

OVERVIEW
CPES INDUSTRY CONSORTIUM

The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members.

The CPES industrial consortium offers:

- The best mechanism to stay abreast of technological developments in power electronics
- The ideal forum for networking with leading-edge companies and top-notch researchers
- The CPES connection provides the competitive edge to industry members via:
- Access to state-of-the-art facilities, faculty expertise, top-notch students
- Leveraged research funding of over $10 million per year
- Industry influence via Industry Advisory Board and research champions
- Intellectual properties with early access for Principal Plus and Principal members via CPES IPPF (Intellectual Property Protection Fund)*
- Technology transfer made possible via special access to the Center's multi-disciplinary team of researchers, and resulting publications, presentations and intellectual properties
- Continuing education opportunities via professional short courses offered at a significant discount

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

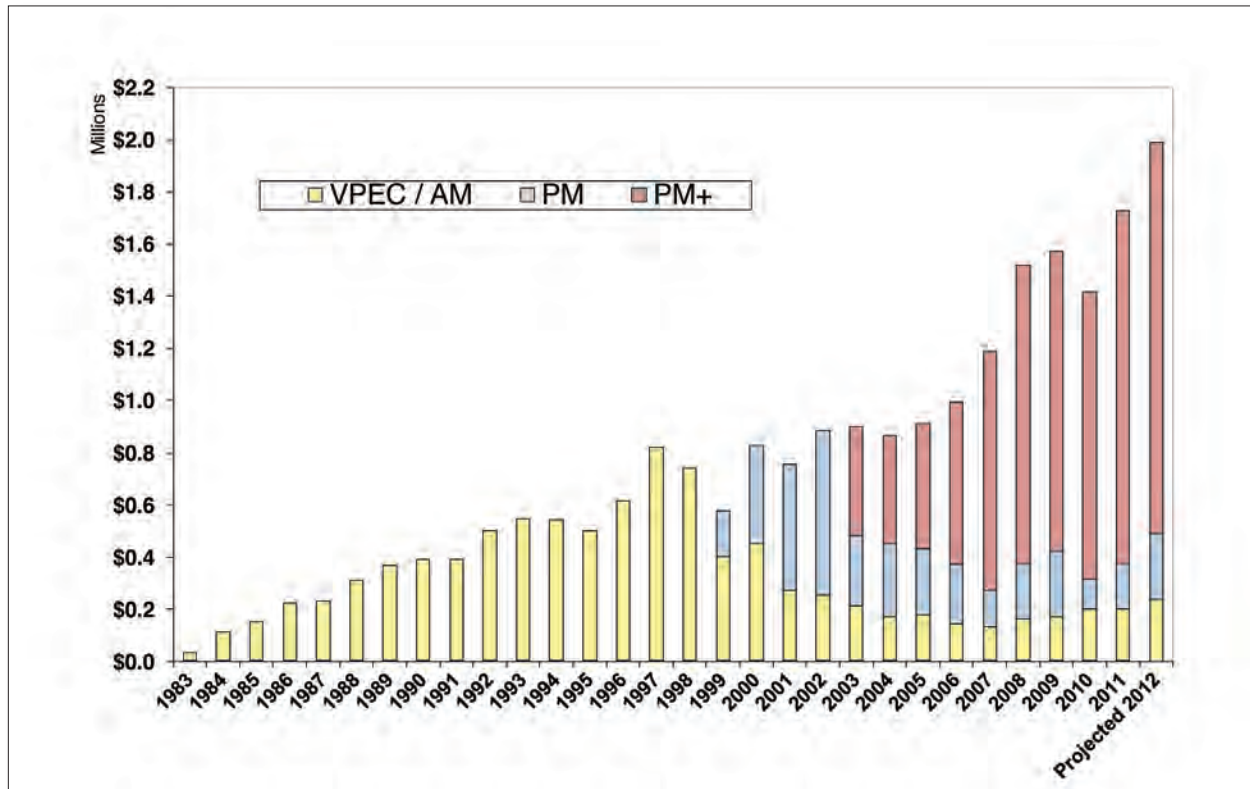## CPES MEMBERSHIP COMPANY GROWTH
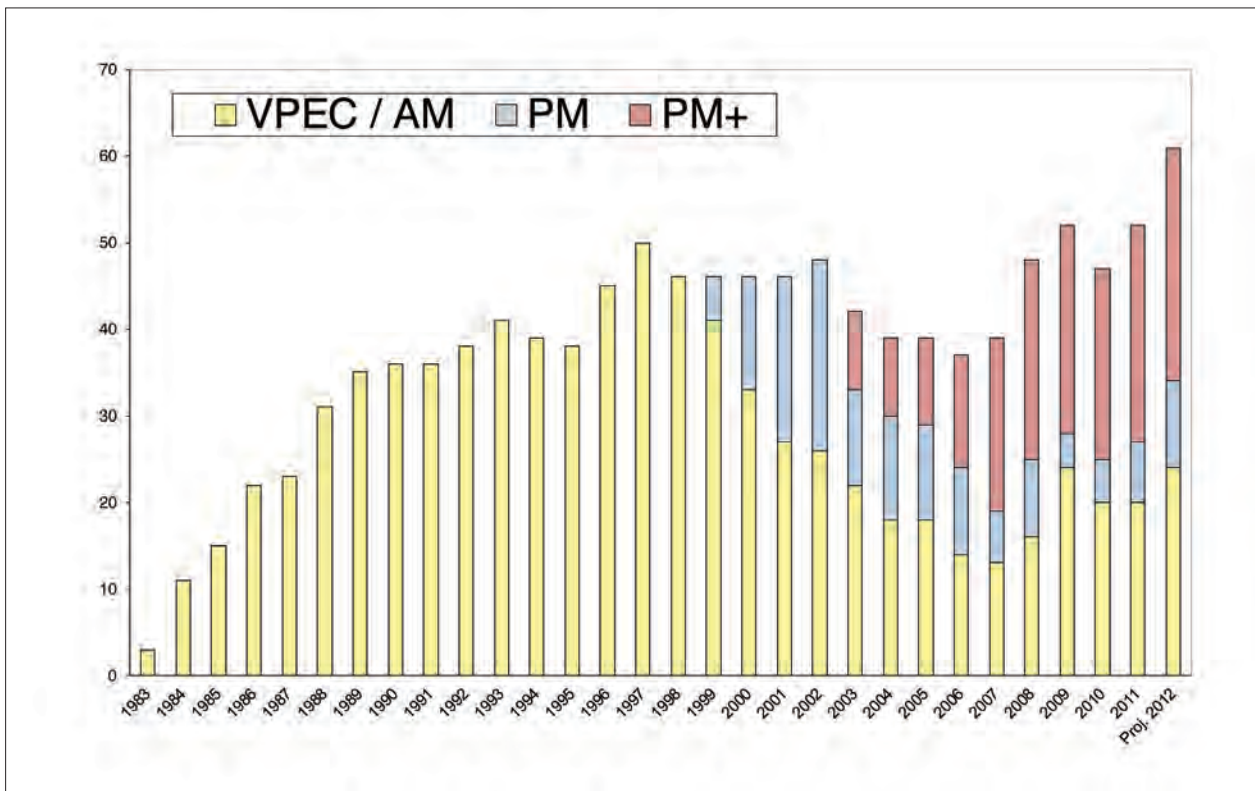
Principal Plus Members (annual contribution - $50,000) - gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research -- PMC (Power Management Consortium), HDI (High Density Integration), or REN (Renewable Energy and Nanogrids). They also have easy access to cutting-edge IPs via CPES IPPF* (Intellectual Property Protection Fund). Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each.
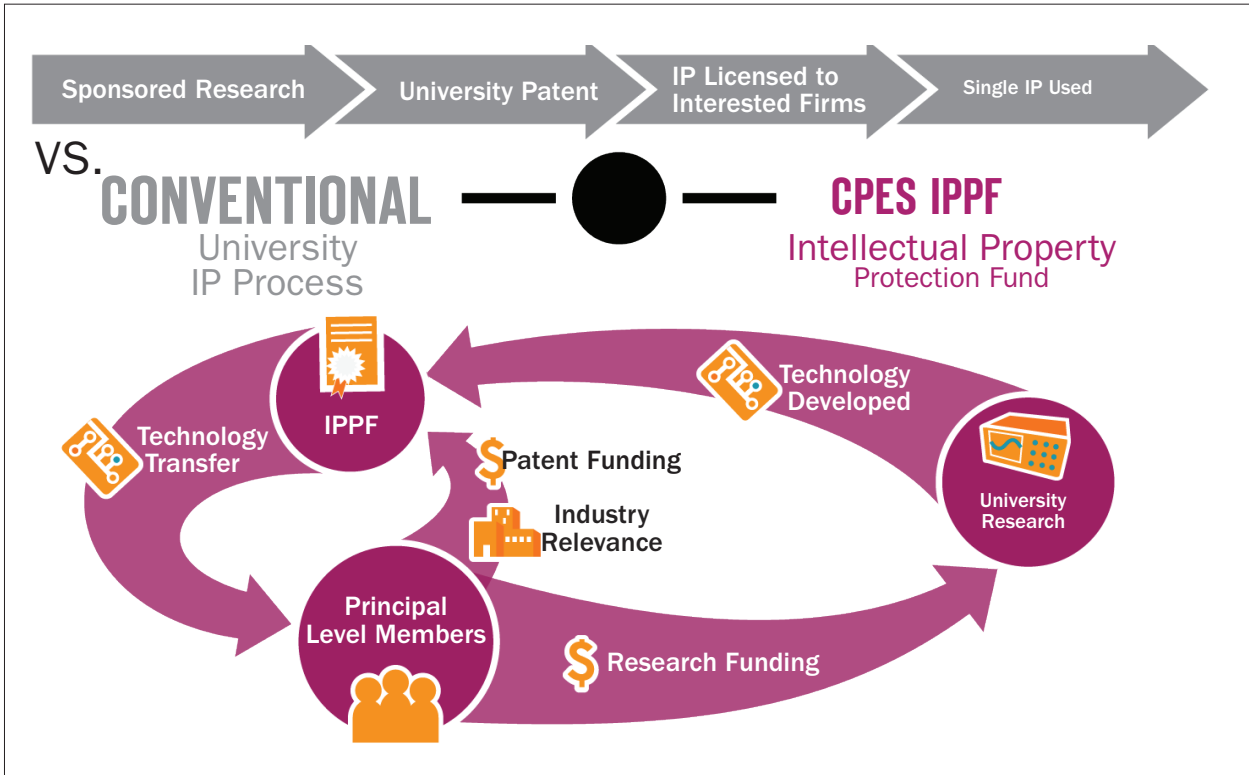
Principal Members (annual contribution - $25,000) - are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. They also have cutting-edge IP advantage via automatic IPPF* (Intellectual Property Protection Fund).

Associate Members (annual contribution - $10,000) - gain the competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges and continuing education to stay updated on new technologies.

Affiliate Members make in-kind hardware/software donations to CPES equivalent to $10,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires Center Director approval.

INDUSTRY MEMBERSHIP FUNDING GROWTH

Sponsored Research → University Patent → IP Licensed to Interested Firms → Single IP Used

VS. CONVENTIONAL University IP Process — CPES IPPF Intellectual Property Protection Fund

Technology Transfer — IPPF — Patent Funding — Industry Relevance — Technology Developed — University Research — Principal Level Members — Research Funding

Intellectual Property Protection Fund

*IPPF is a unique IP access mechanism that provides extraordinary IP advantage to all Principal-level members. IPPF is available automatically, at no additional cost, to Principal Plus and Principal members. IPPF members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by IPPF. Once a technology is protected, IPPF members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IPPF is applicable only to technologies developed by CPES-VT researchers under the CPES industry consortium.

CPES Mini-Consortium Program

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contribution of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

• PMC (Power Management Consortium)
• HDI (High Density Integration)
• REN (Renewable Energy and Nanogrids)

Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each.
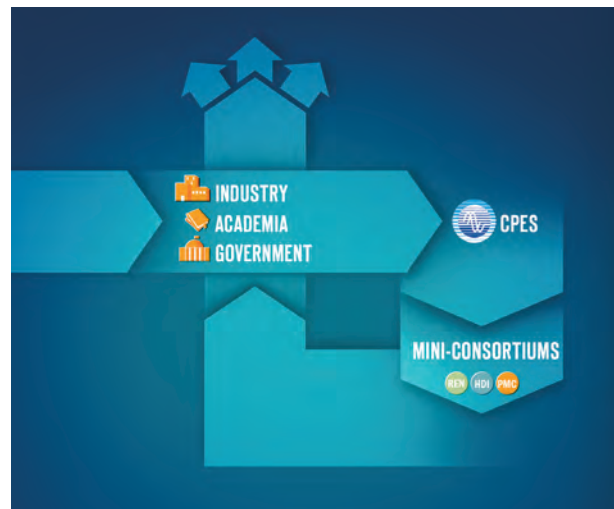
Power Management Consortium (PMC)

In 1997, at the request of Intel, CPES established a mini-consortium to address the issue of power managemenfor future generations of microprocessors, targeting at sub-1 volt and 100-200 amps current. As a result of this focused research, the CPES team has developed a multi-phased voltage regulator module. Instead of paralleling power semiconductor devices in order to meet the current demand and efficiency requirements, the research team has proposed to parallel a number of mini-converters. By paralleling the mini-converters and phase-shifting the clock signal, not only we were able to cancel the significant part of the output current ripple, but also to increase the ripple frequency by N time, where N is the number of channels we parallel. This has resulted in demonstrated improvement, specifically, 4 times improvement in transient response, 10 times reduction in output filter inductors, 6 times reduction in output capacitors, 6 times improvement in power density, and 3 times improvement in profile.

The new generation of Intel's microprocessor is operating at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This particular mode of operation is necessary to conserve energy, as well as to extend the operation time for any battery-operated equipment. The challenge for the voltage regulator module in this case is to provide a precisely regulated output with fast dynamic response in order to transfer energy as fast as possible to the microprocessor.

Today, every Intel processor is powered by such multi-phased VRMs developed by CPES. CPES researchers are continuing to conduct research in this particular subject by exploring new topologies in power semiconductor devices, magnetics, and integrated packaging concepts in order to improve the transient response and minimize the I2R loss due to continuous reduction in voltage as well as continuous increase in load current. We have been exploring a range of input voltages in VRM technologies, from 12V up to 48V, to accomplish this objective.

Mini-Consortium
Power Management Consortium (PMC)
(1998 – present)

CPES · Chicony POWER TECHNOLOGY · DELTA · HUAWEI · muRata · intersil · IOR International Rectifier · NXP

NEC/TOKIN · POWER INTEGRATIONS · LITEON · TEXAS INSTRUMENTS · LINEAR TECHNOLOGY · infineon · RICHTEK · ZTE中兴
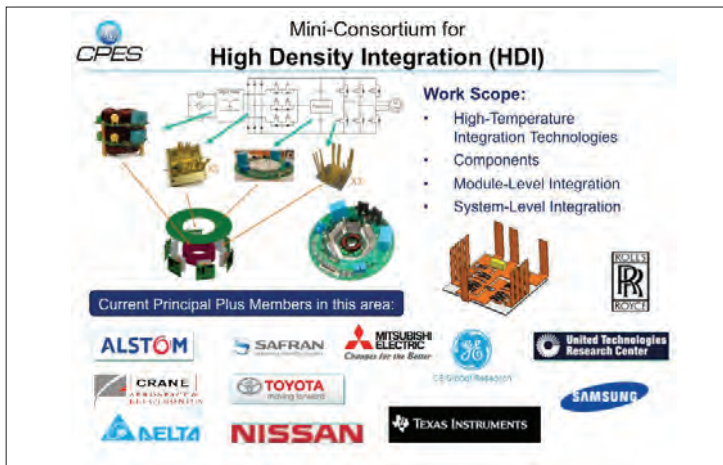
Work Scope:
- Devices and Magnetics
- Modeling and control (analog & digital)
- 3D integration
- High performance VRM/POL converters
- DC/DC converters and Bus converters
- EMI and PFC
- Power architecture and management

Mini-Consortium for
High Density Integration (HDI)

Mini-Consortium on High Density Integration (HDI)

Over the past two decades, CPES has secured research funding from major industries, such as GE, Rolls-Royce, Boeing, Alstom, ABB, Toyota, Nissan, Raytheon, and MKS, as well as from government agencies including the NSF, DOE, DARPA, ONR, U.S. Army, and the U.S. Air Force, in research pursuing high-density system design. CPES has developed unique high-temperature packaging technology critical to the future power-electronic industry.

In the proposed mini-consortium, the goal of high power density will be pursued following two coupled paths, both leveraging the availability of wide-bandgap power semiconductor, as well as high-temperature passive components and ancillary functions. The switching frequency will be pushed as high as component technologies, thermal management, and reliability permit. At the same time, the maximum component temperatures will be pushed as high as component technologies, thermal management, and reliability permit.

Mini-Consortium on Renewable Energy and Nanogrids (REN)

Building upon the Center's Sustainable Building Initiative (SBI) sponsored under the NSF ERC Program, with the initial focus on the development and demonstration of advanced power electronics technology for electrical systems in sustainable buildings, CPES will further develop ac and dc-based renewable energy powered system as a testbed, a living Lab, for future sustainable building electric power system.

The renewable and alternative energy sources would include primarily photovoltaic solar cells, wind generators, micro-turbines, fuel cells, and energy storage. The testbed will be used as a vehicle to address many of the nanogrid and grid interface related issues, such as dc bus architecture, energy/power management, and various forms of utility interface converters and inverters. The site of the "living lab" will be the home of CPES

in Whittemore Hall at Virginia Tech.

The program will concentrate on finding integrative solutions to satisfy the energy, functional, comfort, and zero-CO_2 emission goals for building/home environment.

Mini-Consortium for
**Renewable Energy and Nanogrids (REN)**
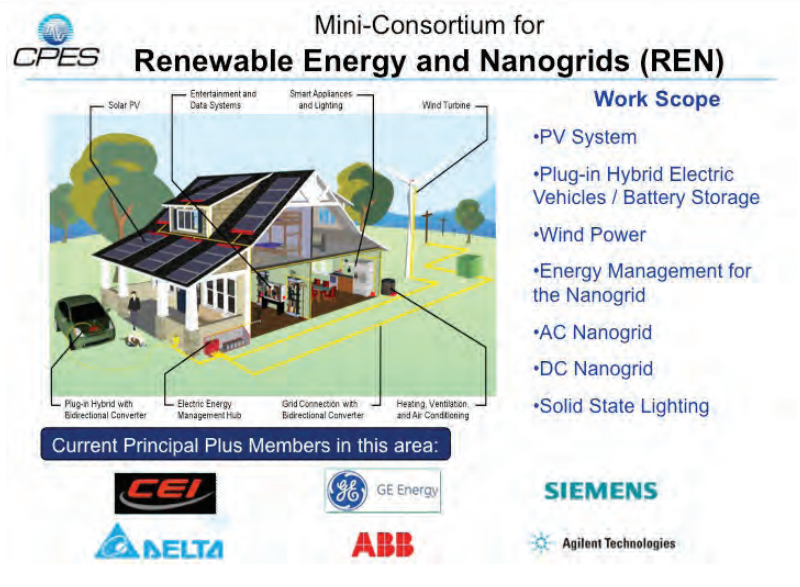
RESEARCH

I n its efforts to develop power processing systems to take electricity to the next step, CPES has developed research expertise encompassing five technology areas: (1) power conversion technologies and architectures; (2) power electronics components; (3) modeling and control; (4) EMI and power quality; (5) high density integration.

These technology areas target applications that in-clude: (1) Power management for information and com-munications technology; (2) Point-of-load conversion for power supplies; (3) Vehicular power conversion sys-tems; (4) Renewable energy systems.

In 2011, CPES sponsored research totaled approxi-mately $2 million. The following abstracts provide a quick insight to the current research efforts.

Application Areas

Power Management for Computers, Telecommunication

Point-of-Load Conversion

Vehicular Power Converter Systems

Renewable Energy Systems

Technology Areas

Power Conversion Topologies and Architectures

Power Electronics Components

Modeling and Control

Output Impedance Z_o

EMI and Power Quality

High Density Integration
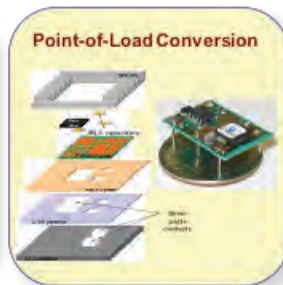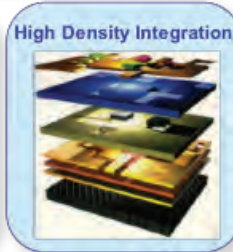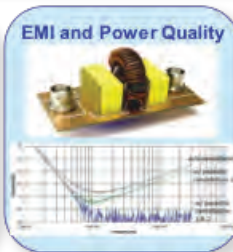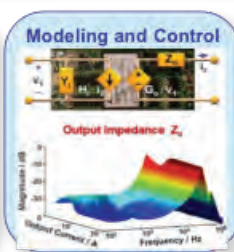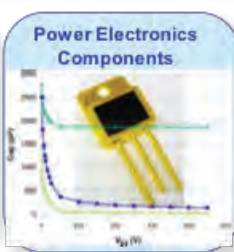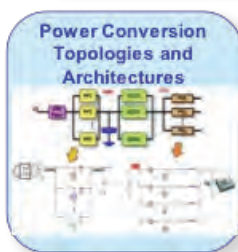
Sponsored Research

Power Supplies On A Chip (Psoc)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology)

Research collaborators: International Rectifier, University of Delaware

Performance Period: September 1, 2010- August 31, 2012

This project aims to develop a proof-of-concept prototype power supply on chip (PSOC) using GaN devices operating at 5-lOMHz. The target is to achieve a power density greater than 1000W/in3 with 88% efficiency. The proposed three-dimensional PSOC will be constructed using IR's GaN devices and Si gate driver IC's assembled on top of a 1 mm magnetic substrate using a high frequency soft magnetic FeNC flake nanocomposite (FeNc). Such a level of integration has never been attempted with a current greater than 5A. The proposed prototypes will extend the current to 20- 40A at 12V input voltage, targeting such applications as computer, mobile electronics, and telecommunication.

Isolated Converter With Integrated Passives And Low Material Stress

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency-Energy, Agile Delivery of Electrical Power Technology)

Research collaborators: University of Florida, University of Texas - Dallas

Performance Period: September 1, 2010- August 31, 2013

This project will develop a monolithic power converter to be used in efficient power adapters for mobile applications, such as netbooks. The chip converter will include the integration of a transformer, ultra-high-density capacitors, and a nano-magnetic material dispensable with high precision by low-cost inkjet printing. The magnetic structure, with a 3X improvement in energy storage, is introduced to keep the transformer volume at a minimum. The resulting highly efficient (>90%) converters with high power density will reduce the 15 tera watt-hours of energy consumed by notebooks and netbooks annually.

Gallium Nitride Switch Technology for Bi-Directional Battery to Grid Charger Application

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency - Energy, Agile Delivery of Electrical Power Technology)

Sub – Awardee of: HRL

Performance Period: October 1, 2010 – March 31, 2014

The purpose of the project is to develop efficient, high power, and cost effective power converters with application to the automotive sector. More specifically, it will utilize high voltage Gallium Nitride (GaN) on low cost silicon substrate switches operating at megahertz frequencies. GaN semiconductors process electricity faster than the silicon semiconductors used in most conventional EV battery chargers. These high-speed semiconductors can be paired with lighter-weight electrical circuit components, which helps decrease the overall weight of the EV battery charger. The innovative design will result in a battery-to-grid bi-directional charger that enables efficient, cost effective power management focusing on grid-interactive distributed energy systems for the automotive sector.

Dual Bi-Directional Silicon Igbts Modules Enables Breakthrough Pv Inverter Using Current-Modulation Topology

Sponsored by: ARPA-E, SunShot Program

Sub -Awardee of: Ideal Power

Performance Period: January 1, 2012- January 29, 2015

Ideal Power Converters is developing light-weight electronics to connect photovoltaic solar panels to the grid. Their technology explores innovative circuits using revolutionary transistor designs to develop solar panel electronics for commercial-scale buildings that are compact enough to be installed on walls or roof-tops. The project goal is to reduce the weight of these electronics by 98%, reducing the cost of materials, manufacturing, shipping and installation, and supporting the aggressive cost-reduction goals of the Department of Energy's SunShot Initiative. Virginia Tech's role will be the development of a mechanically balanced dual chip module using proprietary wave joints to enable low inductances, low strain and passive heat extraction via two-sided cooling.

Evaluation Of Very High Frequency Gan Converter

Sponsored by: The Boeing Company (July 1, 2010 – October 31, 2011)

Gallium-nitride (GaN) power electronics technology is expected to lead to significant increase in switching frequency of power converters. In this work, the impact of increased switching frequency on the EMI filter size and weight is examined for 28V low voltage bus aircraft applications. Preliminary design values show significant weight reduction of the differential-mode filter when the switching frequency goes over 1 MHz, while common mode filter cannot be improved. Power density calculations show that the use of GaN over Si transistors brings significant reduction on semiconductor losses and heatsink size, thus making power conversion at higher switching frequencies possible. In parallel to the design process, a fast switching GaN based phase-leg is built and used subsequently in the 2 MHz switching frequency LLC resonant converter implementation.

High Density Motor Controller

Sponsored by: The Boeing Company (August 1, 2005 – April 30, 2012)

In this project, a 10 kW high power density three-phase ac-dc-ac converter together with a high density PCB axial flux motor were developed and electrically evaluated. The converter consists of a Vienna-type rectifier front end and a two-level voltage source inverter (VSI). In order to reduce the switching loss and achieve a high operating junction temperature, SiC JFETs and SiC Schottky diodes are utilized. The design considerations for the phase-leg units, the gate driver, the input filter, the system protection and motor operation are investigated in detail. Experiments are carried out under different conditions, and the results verify the feasibility of the full system.

System Stability And Analysis

Sponsored by: The Boeing Company (October 22, 2004 – December 31, 2012)

CPES has developed design criteria and analysis tools for integrating ac and dc distributed power electronics conversion systems for the stable, safe and reliable operation of future aircraft electrical power systems. These power electronics systems combine numerous and different types of power converters, which when interconnected can easily interact with each other if no precautionary measures are taken. These interactions can easily lead to instabilities and system faults. Therefore, it is important to study the operation of the system carefully as part of its design process. As a demonstration testbed, CPES modeled a large electrical distribution system where it addressed the actual model implementation of the several components considered using the detailed switching models. CPES also evaluated the testbed correct operation by means of Lyapunov's indirect method—local assessment of large signal stability, studying as well the effect of faults in the system providing insight into the choice of models for the respective studies conducted. In addition, CPES developed ac system small-signal stability criteria. For the verification of these stability analyses, CPES is developing an AC impedance tester to be capable of measuring the synchronous d-q frame impedance of ac networks and power converters for later use in stability studies.

In order to facilitate complex system-level simulation and analysis, CPES is developing enhanced average models that should be capable of capturing not just the fundamental frequency but also the mid-frequency range (up to half of switching frequency) large-signal behavior of power converters. The enhanced converter models will enable the simulation and study of phenomena otherwise neglected by conventional average models, including distortion induced by dead-time, digital sampling, and other controller and power stage non-linearities.

Optimization of AC/AC Motor Controller Power Quality and EMI Filter Topology

Sponsored by: Hamilton Sundstrand (January 1, 2012- December 31, 2012)

The object of this work is the optimization of the combined power quality and EMI filters for motor controller comprising input power circuits fed by variable frequency power bus, and output power circuits that drive variable speed electric motors. The effect of the thermal and electrical characteristics associated with new materials with particular application on the EMI and PQ filters will be researched.

Sustainable Building Design Initiative

Sponsored by: The Institute for Critical Technology and Applied Science (ICTAS) at Virginia Tech (July1, 2009- June 30, 2011)

An interdisciplinary effort of the Center for Power Electronic Systems (CPES) and the Interior Design department to redesign the current CPES space integrating new technologies provides an advanced platform for research. The goal of the Interior Design team is to enhance the quality of the CPES work environment while providing a versatile space that encourages students to conduct

cutting-edge research on energy usage. Current industry standard is to wire a space with alternating current, which can limit daily operations. This particular space utilizes alternating current; however, the versatility of the space will allow CPES to one day rewire with direct current-providing dual-functionality and the ultimate in energy usage calculations. In addition, select pieces of furniture have been collaboratively designed with an integrated power supply-one step forward in an effort to eliminate the need for stationary electrical outlets that limit options for furniture placement and that are quite often aesthetically displeasing. A key component of any design is lighting; therefore, the Interior Design team has carefully designed this space to provide ample lighting and increased lighting controls. Not only will this allow more versatility for its users as the needs of the space changes, but also transforms the space into a living lab where the Interior Design team can conduct tests on perceptions of brightness under fluorescent and LED light sources. Furthermore, the Interior Design team will conduct tests on specified cradle-to-cradle materials, their durability, and the amount of off-gassing of volatile organic compounds (VOC's).light sources.

High-Temperature Packaging of Planar Power Modules by Low-Temperature Sintering of Nanoscale Silver Paste
Sponsored by: NBE Technologies/DOE-SBIR (August 12, 2009 -September 30, 2012)

In present electric vehicles (PHEV/HEV/EV), an extra cooling loop is needed to lower the power-electronics coolant temperature below about 65°C from the radiator coolant temperature of 105°C. One way to reduce the cost of future EVs is to eliminate the extra cooling loop by developing reliable high-temperature power inverter modules that are sufficiently cooled by the radiator coolant. This calls for the development of power packaging technologies that can enable silicon and/or SiC power devices working at junction temperature in excess of 175°C. In the current phase of our power packaging research effort, we have focused on replacing the solder-reflow technique for die-attaching power chips by an emerging low-temperature joining technology (LTJT) which involves low-temperature sintering of silver powders. To reduce the process complexity of the conventional LTJT arising from the need of high pressure (30 to 40 MPa or 300 to 400 Kg-force per cm2, a nanosilver paste material was used to lower the die attach temperature below 270°C with zero

or less than 5 MPa pressure. This simplified LTJT is less likely to damage the chips and allows us to implement a planar packaging scheme for interconnecting both sides of the power devices without using wire bonds. The planar power modules have low parasitic inductances thus less ringing noises from the device-switching action and can be cooled from both sides of the devices for improved thermal management. The electrical performance of the planar power module was tested and the results show that it can work properly under 175°C junction temperature.

Nanoscale Silver Pastes for Low-Temperature Joining of Power Semiconductor Devices
Sponsored by: NBE Technologies/NSF-STTR (August 1, 2009- January 31, 2012)

The thermal performance of the sintered nanosilver was also evaluated. Experimental results show that the sample using sintered nanosilver for the die-attach has a 12.1% lower thermal impedance than the modules using SAC305 and SN100C solders. To check the degradation of the bonding layer, three samples using three die-attach materials were thermally cycled from -40°C to l25°C. The experimental results show that after 500 cycles, the thermal impedance of SAC305 samples and SN100C samples is increased by 12.8% and 15%, respectively, which is much higher than the sample using the sintered nanosilver for the die attach (increased by 4.1%).

Study and Development of an AC/DC Impedance Tester for Medium Voltage High Power Systems
Sponsored by: Newport News Shipbuilding—Huntington Ingalls (July 1, 2009 - April 30, 2012)

The objective is to identify and/or develop a feasible impedance measurement technique that be used for high power and medium voltage DC and AC power systems, and to develop an AC impedance tester that can be used to test impedances at AC and DC interfaces for systems up to 13.8 kV and 36 MW.

A Study of Power Conversion and Driving Circuit for Multiple Solid-State Light Sources on DC Distribution Systems
Sponsored by: Panasonic Electric Works (May 1, 2010 – April 30, 2011

This project includes two aspects: the first one is investigating different drive solutions for multi-channel LED driver. The two stages solution with commercial available driver ICs and the single stage resonant solution are compared in detail. Various operation conditions are con-

sidered and simulated. The second part of this project is design a 50W, 1 MHz resonant LLC-DCX converter for distribute DC system application. Detail design process, loss calculation, test results and hardware demonstration are included.

A Study of Multi-Channel Constant Current Driver for Multiple Solid-State Light Sources on DC Distribution System

Sponsored by: Panasonic Electric Works (April 1, 2011 – March 31, 2012)

Recently, many applications such as display backlighting, indoor lighting and street lighting, all prefer multi-channel LED drivers. In this project, a design methodology for MC3 LLC LED driver has been developed. The frequency-controlled analog dimming solution has been verified by both simulation and experimentation. The circuit behavior under open and short failure is investigated as well. Moreover, in order to achieve lower dimming ratio and keep higher efficiency, the hybrid control approach combining with asymmetrical PWM control and frequency control is proposed.

High-Temperature, High Power Density Power Converter for Embedded Generators

Sponsored by: Rolls Royce (January 1, 2011 – December 31, 2012)

The conducting project is to evaluate and demonstrate feasibility of developing a complete high-power, high-temperature, high-power-density bidirectional three-phase ac-dc power converter unit required to operate embedded generators in the temperature range of 200 250 °C. In the Phase II of this program, the focus is on the development and validation of the critical system components at the rated power and temperature, and on the functional integration of the equivalent low-temperature subsystems at reduced power level.

Based on the work conduced from Phase I and Phase II, the phase III of this project will concentrate on the final thermo-mechanical design, integration of all the system components and subsystems, and on testing, characterization, evaluation, and demonstration of the complete system at full power and high ambient temperature.

Terminal Modeling of Noise Source in Switching Power Converters

Sponsored by: Hispano Suiza, SAFRAN (October 1, 2010 -September 30, 2012)

The main objective of this research is to develop terminal models of noise sources in switching converters for easy EMI analysis. These models must be scalable for different load and source conditions. Conventional methods of EMI modeling use physics based models of semi-conductor devices and EMI coupling paths. Due to the complex nature of these models the simulations often fail to converge or lead to unusable results.

The efforts in this research are aimed at simplifying the simulations by using Thevenin or Norton models of these noise cells. Here "noise-cell" may refer to both device level (single device or a Phase-leg) and converter level abstraction. The final goal is to make a terminal EMI model of a 3-phase voltage source inverter (VSI) in to estimate EMI in power train set-up as shown above.

With the success of the generalized terminal modeling technique, another direction of research pursues in estimating the worst case EMI noise on a de bus that feeds several converters in parallel. In previous research, the generalized modeling technique was shown to accurately model switching power converters from the de input side. The aim is to estimate conducted EMI noise on de bus with terminal models of several converters in parallel. The converters may switch in a synchronized or in un-synchronized fashion. The technique should be able to estimate the worst case noise on de bus for un-synchronized switching of several converters.

High-Density Power Package with Gate Drive

Sponsored by: Toyota Motor Co. (July 1, 2010- June 30, 2011)

In recent years, planar packages such as the embedded-power module shown below have been introduced as a means to reduce package impedances, enabling potentially higher switching frequency. The module performance, however, is also determined by the gate driver and the interaction between the gate-driver and the power-module packages. Thus, the goal of the project is to identify the trade-offs among cost, performance, process requirements, etc. for a small number of layouts of the gate drive and the power module.

INTELLECTUAL PROPERTY

U.S. Patents Awarded

09.028
Electromagnetic Interference Noise Separator
Shuo Wang, Fred C. Lee
U.S. PATENT: 8,125,291
Issued: February 28, 2012

06.081
Method and Apparatus for Three-Dimensional Integration of Embedded Power Module
Michele H. Lim, Zhenxian Liang, J. Daan van Wyk
U.S. PATENT: 7,932,800
Issued: April 26, 2011

Invention Disclosures

12-044
10/7/11
Energy Storage for PFC by EV Motor/Generator
Khai Doan The Ngo, Hui Wang
Patent application sponsored by IPPF

12-031
10/4/11
Simplified Optimal Trajectory Control (SOTC)
for LLC resonant converters
Weiyi Feng, Fred C. Lee, Paolo Mattavelli
Patent application sponsored by IPPF

12-024
9/1/11
Anti-islanding Detection Algorithm and
Modeling Approach for Three-Phase Distributed
Generation Unit
Dong Dong, Dushan Boroyevich, Paolo Mattavelli
Patent application sponsored by IPPF

12-010
7/28/11
An Algorithm and Implementation System Architecture for the Measurement of Impedances in the D-Q Frame Domain
Gerald Francis, Rolando Burgos, Dushan Boroyevich, Fred Wang, Zhiyu Shen, Paolo Mattavelli, Kamiar Karimi, Sheau-Wei J Fu

12-009
7/28/11
Small-Signal Stability Criterion for AC Power System Interfaces Feeding Three-Phase High-Power Factor Rectifiers
Rolando Burgos, Dushan Boroyevich, Fred Wang, Kamiar Karimi

11-130
6/6/11
Hybrid Structure Packaging Method for High Temperature SiC Power Module
Ruxi Wang, Zheng Chen, Dushan Boroyevich

11-117
6/6/11
High Temperature Transformer Isolated Phase Leg Drive Drive for Silicon Carbide-Based Inverter/Converter
Ruxi Wang, Dushan Boroyevich, Milisav Danilovic, Zheng Chen

11-113
5/3/11
DC leakage current reduction for single-phase full-bridge converter
Dong Dong, Fang Luo, Dushan Boroyevich, Paolo Mattavelli
Patent application sponsored by IPPF

11-088
3/8/11
Distributed Magnetic Structure with Shaped Field Pattern
Khai Doan The Ngo, Jayashree Keezhanatham Seshadri
Patent application sponsored by IPPF

11-079
2/25/11
Current Sharing Method for Semi-Regulated Resonant Converters (update of 10-057)
Chanwit Prasantanakorn, Fred C. Lee
Patent application sponsored by IPPF

11-075
2/2/11
Two-Stage Bi-Directional Single-Phase Converter with DC-Link Capacitor Reduction
Dong Dong, Dushan Boroyevich, Ruxi Wang, Fred Wang
Patent application sponsored by IPPF

11-074
1/31/11
Three-Level Active Neutral-Point-Clamped Zero-Voltage-Switching Converter using Coupled Magnetic Circuit
Jin Li, Dushan Boroyevich, Jinjun Liu
Patent application sponsored by IPPF

VIRGINIA TECH FACILITIES
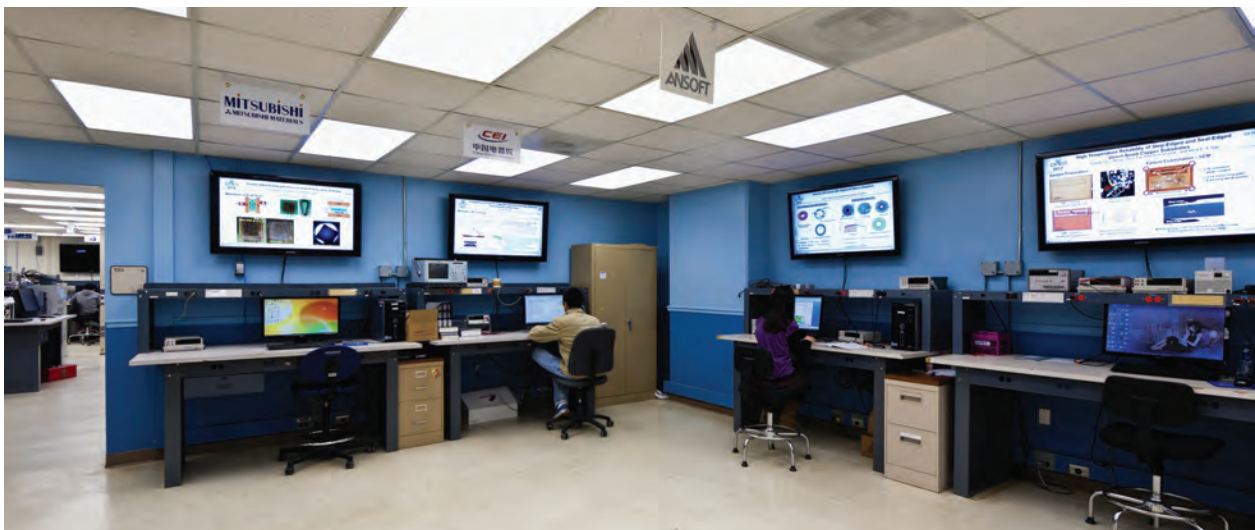
Introduction

The Center headquarters is located at Virginia Tech, occupying office and lab facilities encompassing more than 19,000 sq.ft. of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab and computer lab. In addition to the headquarters labs and offices, a research library and a large conference room with voice and video conferencing capabilities supporting remote site course instruction as well as interaction among CPES collaborators is maintained. Interactive collaboration is routinely facilitated through conference calls, WebEx online conferencing, student and faculty exchanges, and face-to-face research project review meetings.
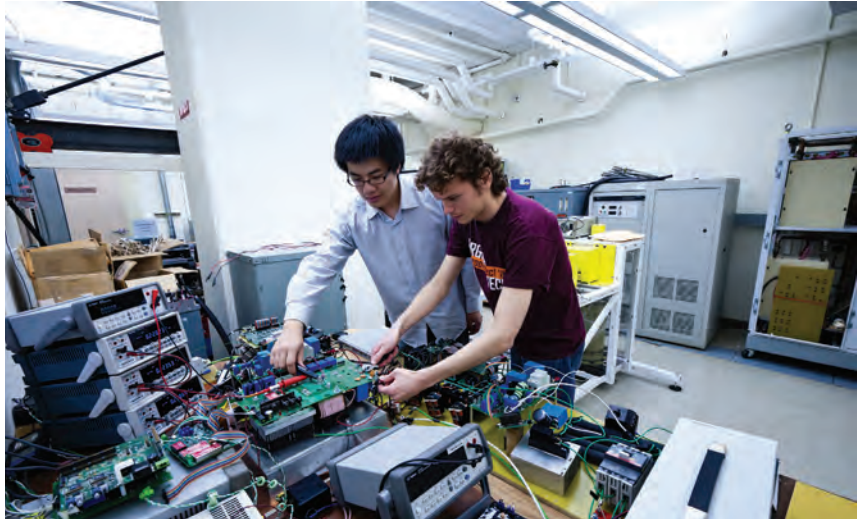
Electrical Research Laboratory

The electrical research laboratory is equipped with state-of-the-art power testing equipment, dynamometers, prototype PWB manufacturing equipment, an EMI chamber, a clean room, a mechanical shop. The Power Electronics Research Lab is equipped with state-of-the-art tools and instrumentation necessary for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6 kV, 1 MW. Each student bench is equipped with Dell Studio XPS computers with an i7 core processor and multiple GBs of RAM for running simulations. Standard instrumentation is comprised of GHz oscilloscopes, multi-channel function generators, electronic loads, network, spectrum, impedance, logic and power analyzers, thermal sensors and AC/DC bench supplies of all sizes. Specialized test room equipment includes: thermal imaging equipment, thermal cycling chambers, Hi-Pot tester, 3-D magnetic field scanner, EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, programmable and variable loads, and liquid cooled heat-exchanger.

Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculties, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab is established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide the state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 clean room space, and the addition of a dark room for photolithography processing. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro/electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. The IP lab also has the ability to mount bare dies and SMT components using high precision pick-n-place machine, solder reflow belt furnace, and convection reflow oven. The advanced vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. The wire bonding machines equipped

in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapuslants an automated precision dispensing system and a spin coater have been added in the lab. In addition, the IP lab has the full capability for low temperature co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The Component- and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Low and high power curve tracers, impedance analyzers, and precision multimeters can be used for electrical property measurements. Thermal performance evaluation can be made by the setup of thermocouples, optic-fiber sensors, IR imaging, and thermal diffusivity test system. Reliability analysis is performed using multipurpose bond tester on as-made modules and the ones after certain numbers of temperature/humidity cycling. An array of cross-sectioning and grinding/polishing equipment has been used to better understand the microstructure of electronic packaging materials.

Computer Lab

The Computer Lab supports all major software used in power electronics analysis and design including: SPICE, Saber, I-DEAS, Math Products – Matlab and Mathcad, Ansoft Products- Maxwell 2-D and 3-D finite-element analyzers,ePhysics, and Q3D, Mentor Graphics and Cadence circuit simulation software, SIMPLIS, PLECS, FLOTHERM circuit thermal analyzer software, and Inventor Professional.

High Power Lab

High power, high voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost sharing of more than $250K for renovations, the electrical research lab area at VT has been renovated and upfit to accommodate medium voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. A 1 MW Innovation Series medium voltage IGBT drive donated by GE is installed as a programmable load. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4160 V level. The unique installation distinguishes VT as one of a few select universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

PEOPLE

STUDENTS

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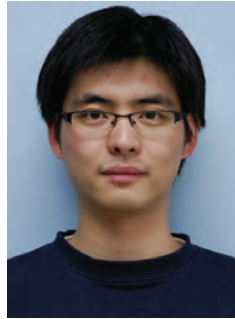
Zheng Chen

Han Cui

Milisav Danilovic

Dong Dong
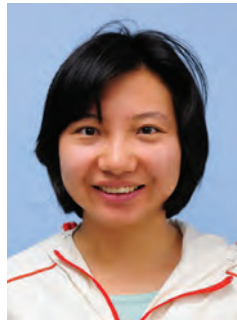
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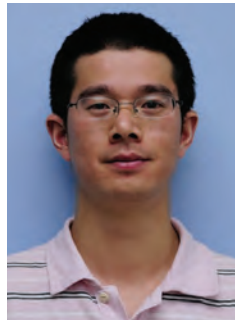
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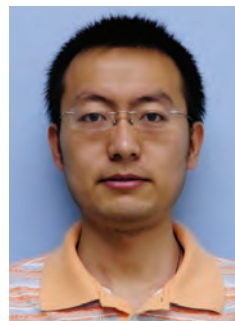
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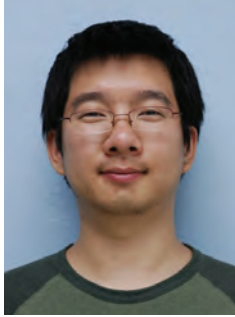
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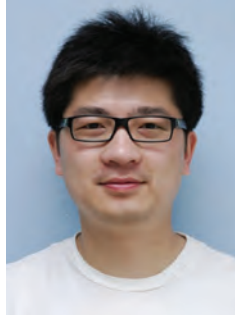
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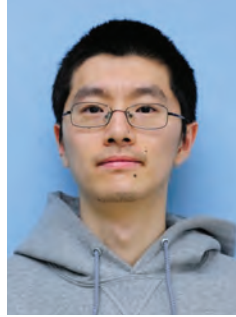
Tao Tao
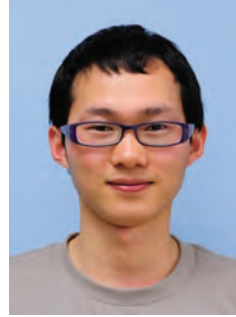
Shuilin Tian
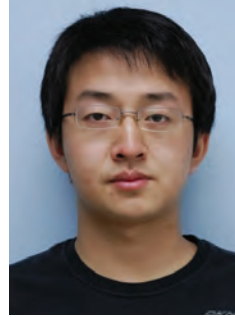
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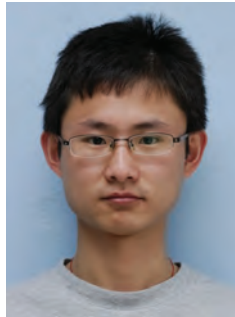
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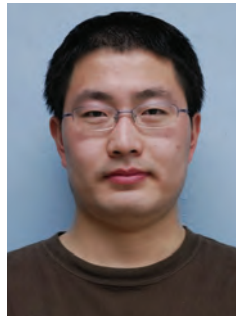
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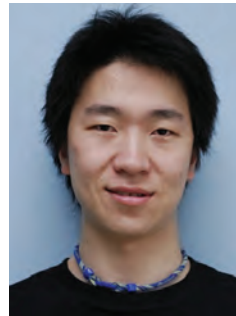
Xuning Zhang
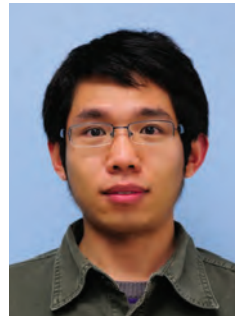
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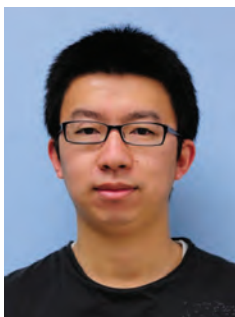
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PEOPLE

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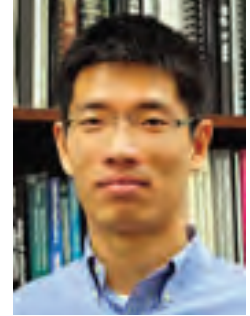
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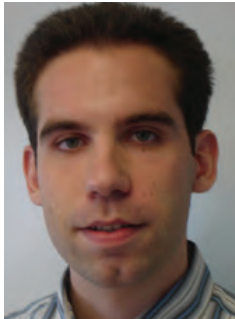
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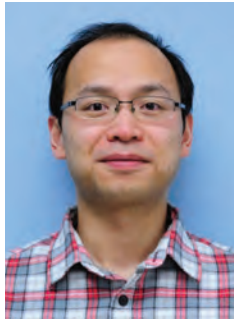
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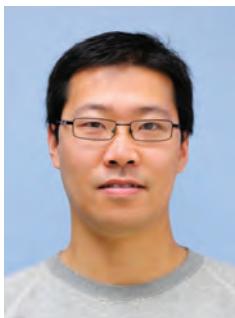
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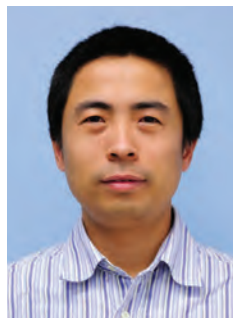
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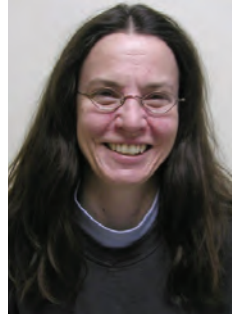
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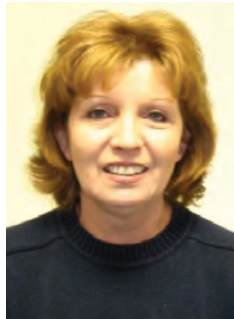
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PUBLICATIONS

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Design and Implementation of a High Power Density Three-Level Parallel Resonant Converter for Capacitor Charging Pulsed-Power Supply
Honggang Sheng, Wei Shen, Hongfang Wang, Dianbo Fu, Yunqing Pei, Xu Yang, Fred Wang, Dushan Boroyevich, Fred C. Lee, C. Wesley Tipton, IV
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Weiyi Feng, Paolo Mattavelli, Fred C. Lee, Dianbo Fu
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Yiying Yao, Guo-Quan Lu, Zheng Chen, Dushan Boroyevich, Khai D. T. Ngo
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Modularized Design Consideration of a General-Purpose, High-Speed Phase-Leg PEBB Based on SiC MOSFETs
Zheng (Henry) Chen, Milisav Danilovic, Dushan Boroyevich, Zhiyu Shen
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Variable Sampling Frequency in Iterative Learning Current Control for Shunt Active Filter in Aircraft Power Systems
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A Small Signal Model for V2 Control with Composite Output Capacitors Based on Describing Function Approach

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Small-signal Model Analysis and Design of Constant-on-time V2 Control for Low-ESR Caps with External Ramp Compensation

Shuilin Tian, Kuang-Yao Cheng, Fred C. Lee, Paolo Mattavelli

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Yipeng Su, Qiang Li, Mingkai Mu, Fred C. Lee

A New High Frequency Inductor Loss Measurement Method

Mingkai Mu, Fred C. Lee

Magnetic Characterization of Low Temperature Co-fired Ceramic (LTCC) Ferrite Materials for High Frequency Power Converters

Mingkai Mu, Yipeng Su, Qiang Li, Fred C. Lee

High Power Density, High Efficiency DC/DC Converter

Daocheng Huang, David Gilham, Weiyi Feng, Pengju Kong, Dianbo Fu, Fred C. Lee

A Novel Integrated Multi-Elements Resonant Converter

Daocheng Huang, Pengju Kong, Fred C. Lee, Dianbo Fu

Multi-Channel Constant Current (MC3) LLC Resonant LED Driver

Haoran Wu, Shu (Alex) Ji, Fred C. Lee, Xinke Wu

Lithium-Based Energy Storage Management for DC Distributed Renewable Energy System

Wei Zhang, Dong Dong, Igor Cvetkovic, Fred C. Lee, Dushan Boroyevich

Un-Terminated, Low-Frequency Terminal-Behavioral d-q Model of Three-Phase Converters

Igor Cvetkovic, Marko Jaksic, Dushan Boroyevich, Paolo Mattavelli, Fred C. Lee, Zhiyu Shen, Sara Ahmed, Dong Dong

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Ruxi Wang, Zheng Chen, Dushan Boroyevich, Li Jiang, Yiying Yao, Kaushik Rajashekara

Transformer-Isolated Gate Drive Design for SiC JFET Phase-Leg Module

Ruxi Wang, Milisav Danilovic, Dushan Boroyevich, Zheng Chen, Kaushik Rajashekara

Evaluation of the Switching Characteristics of a Gallium-Nitride Transistor

Milisav Danilovic, Zheng Chen, Ruxi Wang, Dushan Boroyevich, Paolo Mattavelli

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Dong Dong, Dushan Boroyevich, Paolo Mattavelli
2011 IEEE Energy Conversion Congress & Exposition (ECCE), Phoenix, Arizona, September 17-22, 2011

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2011 IEEE Energy Conversion Congress & Exposition (ECCE), Phoenix, Arizona, September 17-22, 2011

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Development of a 10 kW, High Temperature, High Power Density, Three-Phase AC-DC-AC SiC Converter
Puqi Ning, Di Zhang, Rixin Lai, Jiang Dong, Fred Wang, Dushan Boroyevich, Khai Ngo, Rolando Burgos, Kamiar Karimi, Immanuel Vikram, Eugene Solodovnik
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An Algorithm and Implementation System for Measuring Impedance in the D-Q Domain
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2011 IEEE Energy Conversion Congress & Exposition (ECCE), Phoenix, Arizona, September 17-22, 2011

AC Stability of High Power Factor Multi-Pulse Rectifiers
Rolando Burgos, Dushan Boroyevich, Fred Wang, Kamiar Karimi, Gerald Francis
2011 IEEE Energy Conversion Congress & Exposition (ECCE), Phoenix, Arizona, September 17-22, 2011

Development of an All SiC, High Power Density, Three-Phase Rectifier with Interleaving
Di Zhang, Puqi Ning, Fred Wang, Dushan Boroyevich, Rolando Burgos, Kamiar Karimi, Vikram Immanuel, Eugene Solodovnik
2011 IEEE Energy Conversion Congress & Exposition (ECCE), Phoenix, Arizona, September 17-22, 2011

Dynamic Performance Comparison of Current Mode Control Schemes for Point-of-Load Buck Converter Application
Yingyi Yan, Fred C. Lee, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Frequency Behavior and its Stability of Grid-interface Converter in Distributed Generation Systems
Dong Dong, Jin Li, Dushan Boroyevich, Paolo Mattavelli, Igor Cvetkovic, Yaosuo Xue
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

A Novel Anti-islanding Detection Algorithm for Three-phase Distributed Generation Systems ["Outstanding Presentation Award"]
Dong Dong, Jin Li, Dushan Boroyevich, Paolo Mattavelli, Yaosuo Xue
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Common-Mode EMI Noise Reduction for Grid-interface Converter in Low-voltage DC Distribution System
Dong Dong, Xuning Zhang, Fang Luo, Dushan Boroyevich, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

On discussion of switching frequency impacts on Dcfed motor drive EMI filter design

Fang Luo, Dushan Boroyevich, Paolo Mattavelli, Xuning Zhang

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

High Power Density EMI Filter Design with Consideration of Self-Parasitic

Ruxi Wang, Dushan Boroyevich, Handy Fortin Blanchette, Paolo Mattavelli

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

EMI Noise Attenuation Prediction with Mask Impedance in Motor Drive System ["Outstanding Presentation Award"]

Ruxi Wang, Handy Fortin Blanchette, Dushan Boroyevich, Paolo Mattavelli

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

CM Noise Containment in a DC-fed Motor Drive System Using DM Filter

Xuning Zhang, Fang Luo, Dong Dong, Paolo Mattavelli, Dushan Boroyevich

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Novel Non-isolated LLC Resonant Converters

Daocheng Huang, Xinke Wu, Fred C. Lee

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012,

Gallium Nitride Based 3D Integrated Non-Isolated Point of Load Module

David Reusch, David Gilham, Yipeng Su, Fred C. Lee

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

High Frequency Bus Converter with Low Loss Integrated Matrix Transformer

David Reusch, Fred C. Lee

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

R-Based MPPT Method for Smart Converter PV System

Li Jiang, Wei Zhang, Dong Dong, Igor Cvetkovic, Fred C. Lee, Paolo Mattavelli, Dushan Boroyevich, Pengju Kong

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Finite Element Analysis of Inductor Core Loss under DC Bias Condition ["Outstanding Presentation Award"]

Mingkai Mu, Feng Zheng, Qiang Li, Fred C. Lee

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Winding AC Resistance of Low Temperature Co-fired Ceramic Inductor

Qiang Li, Fred C. Lee

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Analytical Core Loss Models for Planar Inductors with Non-uniform Flux Distribution and Non-sinusoidal Excitation

Qiang Li, Mingkai Mu, Fred C. Lee

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Modeling of Planar Inductors with Non-uniform Flux Distribution and Non-linear Permeability for High-density Integration

Qiang Li, Yipeng Su, Mingkai Mu, Fred C. Lee, David Gilham

2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

A Hybrid Strategy with Simplified Optimal Trajectory Control for LLC Resonant Converters
Weiyi Feng, Fred C. Lee, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Low Profile LTCC Inductor Substrate for Multi-MHz Integrated POL Converter
Yipeng Su, Qiang Li, Mingkai Mu, David Gilham, David Reusch, Fred C. Lee
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Improving EMI Filter Design with In-Circuit Impedance Mismatching
Fang Luo, Dushan Boroyevich, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Design of Output Passive EMI Filter in Dc-Fed Motor Drive
Jing Xue, Fred Wang, Xuning Zhang, Dushan Boroyevich, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Analysis of Multi-Phase Hybrid Ripple-Based Adaptive on-Time Control for Voltage Regulator Modules
Brian Cheng, Feng Yu, Yingyi Yan, Fred C. Lee, Paolo Mattavelli, Wenkai Wu
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

A Transformer Assisted Zero-Voltage Soft-Switching Three-Level Active Neutral-Point-Clamped Converter
Jin Li, Jinjun Liu, Dong Dong, Paolo Mattavelli, Dushan Boroyevich, Yaosuo Xue
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

An Adaptive Dead-Time Control Scheme for High-Switching-Frequency Dual-Active-Bridge Converter
Jin Li, Zheng Chen, Zhiyu Shen, Paolo Mattavelli, Jinjun Liu, Dushan Boroyevich
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Digital Gain-Scheduled Control of a High Frequency Parallel Resonant DC-DC Converter
Marko Vulovic, Dushan Boroyevich, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Modeling Verification, Validation, and Uncertainty Quantification (VV&UQ) Procedure for a Two-Level Three-Phase Boost Rectifier
Sara Ahmed, Rolando Burgos, Chris Roy, Dushan Boroyevich, Paolo Mattavelli
2012 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 5-9, 2012

Theses & Dissertations

Current Sharing Method for Resonant DC-DC Transformers
Chanwit Prasantanakorn, *Thesis, January 21, 2011*

Low-Profile Magnetic Integration for High-Frequency Point-of-Load Converter
Qiang Li, *Dissertation, August 11, 2011*

Modeling of V2 Control with Composite Capacitors and Average Current Mode Control
Feng Yu, *Thesis, May 2, 2011*

Design of an Arbitrary Waveform Generator for Power System Perturbation
Justin Walraven, *Thesis, August 15, 2011*

Multi-Channel Constant Current (MC3) LED Driver for Indoor LED Luminaries
Haoran Wu, *Thesis, November 14, 2011*

APPENDIX
Assorted Research Nuggets

Laminated LTCC Ferrite Materials for High-frequency POL Converters

Low-temperature co-fired ceramic (LTCC) ferrite materials are promising candidates for forming the magnetic substrate of high-frequency converters. The inductors can be fabricated in the substrate, which means the power density of the converter can be dramatically increased. There are three types of LTCC ferrite tape material available from ESL ElectroScience®: 40010, 40011 and 40012. The performance of the LTCC ferrite can be improved by laminating different LTCC tapes and co-firing. The permeability and core loss density of several combinations of LTCC tapes are characterized and compared, and the best laminated LTCC materials for the high-frequency magnetic substrate of POL converters are chosen and verified.
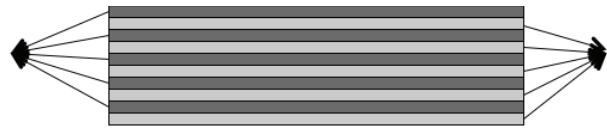
Fig. 1. Laminated LTCC concept
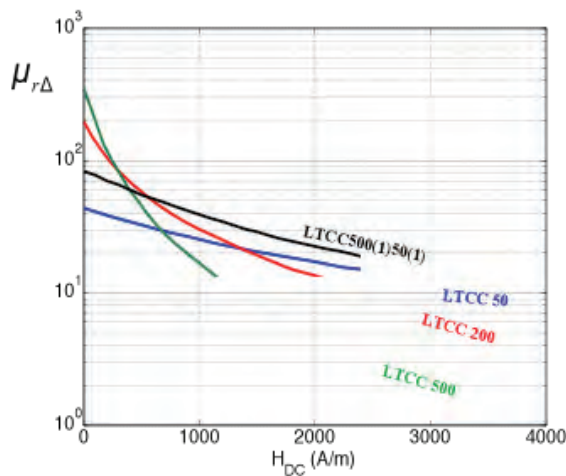
Fig. 2. Incremental permeability
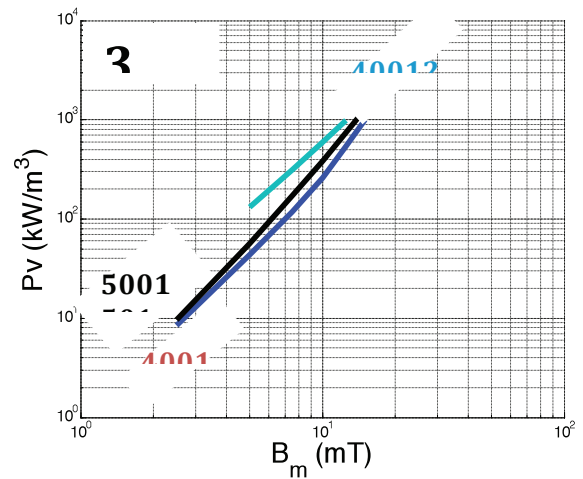
Fig. 3. Core loss density

Investigation of Tradeoffs between Efficiency, Power Density and Switching Frequency in a Three-Phase Two-Level PWM Boost Rectifier

Efficiency and power density are usually two important goals in power converter design. The goal of this paper is to develop an evaluation procedure to investigate the relationship between efficiency, power density and switching frequency. A three-phase two-level PWM boost rectifier is used as an example. The estimated efficiency and converter weight are shown to change as the switching frequency and power rating change. A comparison of this estimation with results obtained from a hardware prototype verify the estimation procedure.

Fig. 1. Three-phase two-level boost rectifier power stage design procedure.
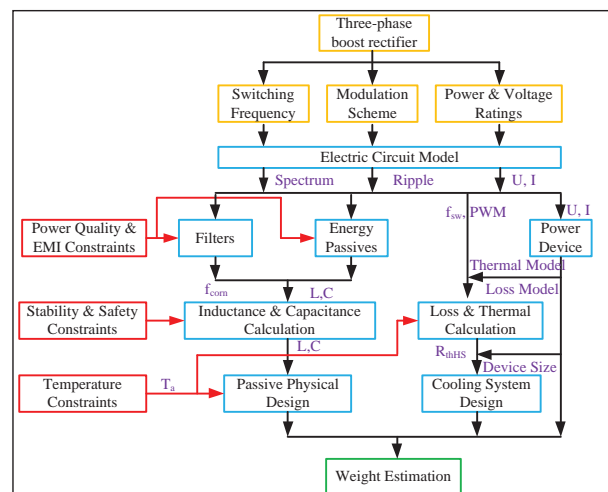
Higher Bus Voltage Impact on Power Converter Power Density

ndustry always has a strong will to increase the power distribution bus voltage due to the ever-increasing power consumption of the load, since a high-voltage power bus can lower I2R losses. In addition, a higher bus voltage can reduce the size and cost of cables. Besides the cables, the impact of higher voltage on other components is not clear; in particular, few studies have shown the impact of a higher-voltage bus on the power converter, which has voltage-sensitive components such as power semiconductors and capacitors. This paper studies the impact of higher bus voltage on the power density and efficiency of a converter. A dc-dc converter and a front-end motor drive are used as examples. Results show a varia-tion of power density along with power level and voltage level.

The following figure shows that the power density (without converter housing) changes with different voltage levels of the 1 kW dc-c converter and 10 kW motor drive. From these results, the following conclusions can be drawn:

• The power density of the converter without a filter does not change too much when the bus voltage is increased.
• The power density of the EMI filter increases when the voltage level increases.
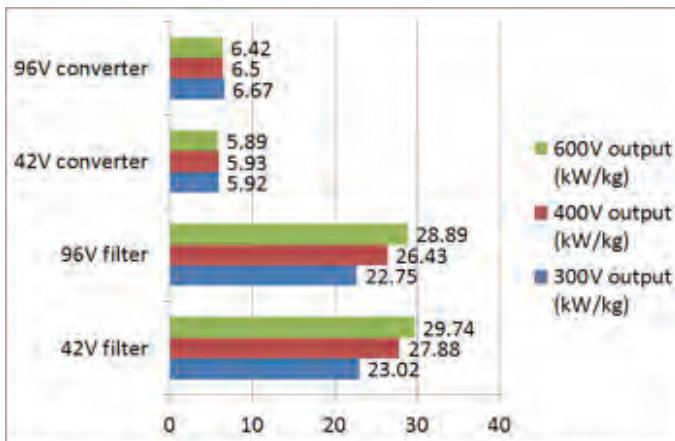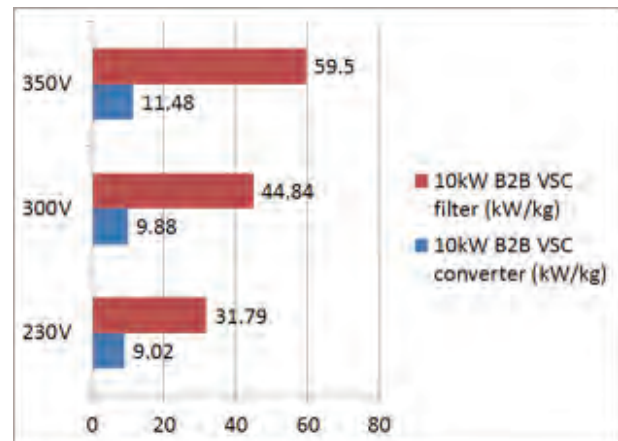
(a)   (a)

Fig. 1. Power density comparison (a) dc-dc converter and (b) motor drive

Experimental Verification of the Generalized Nyquist Stability Criterion for a Balanced Three-phase Ac System in the Presence of Constant Power Loads

Stability is a great concern for power systems with relatively small sources and multiple regulated power converters. Addressing this need, this paper presents an experimental verification of the generalized Nyquist stability criterion (GNC) for balanced three-phase ac systems. This criterion, developed by MacFarlane and Postlethwaite in the 1970's, was first proposed as a stability analysis tool for ac interfaces in the d-q frame in the late 1990s. Since then, however, very few papers have addressed the verification of this theory in a real power system given the intricacies of three-phase impedance measurement in the d-q frame. In this paper, a voltage source inverter feeding a boost rectifier is used to implement an experimental balanced three-phase system, where, by adjusting their respective control bandwidths, stable and unstable cases are found at the ac interface. Then, the d-q frame impedances of both converters are measured and the GNC is applied, showing how both stable and unstable cases can be effectively predicted.
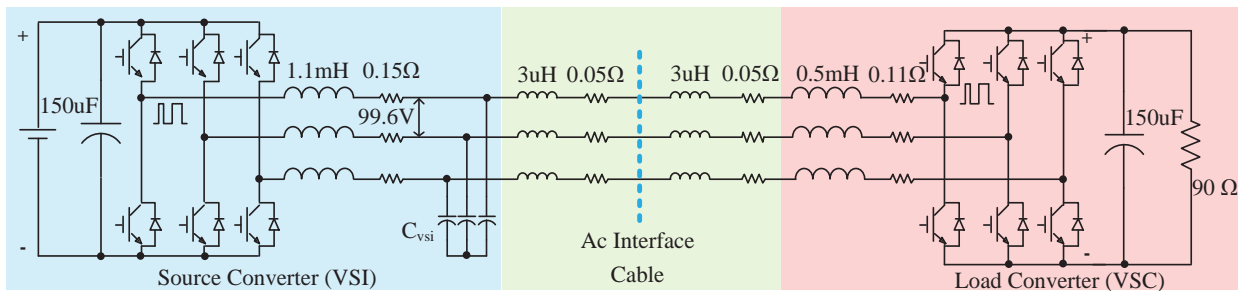
Fig. 1. Ac system for GNC verification
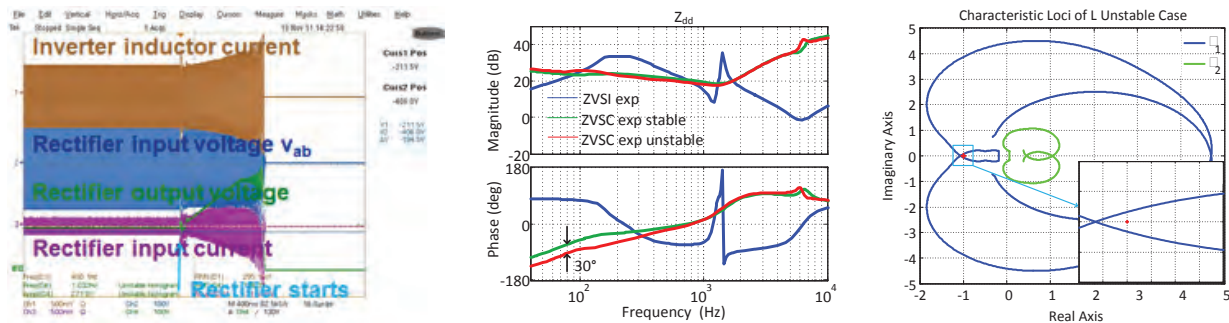
Fig. 2. Unstable case experiment results. (a) System waveforms (b) dd channel impedance (c) Characteristic loci.
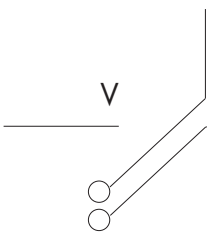
R-based MPPT method for smart converter PV system

In a smart-panel PV system, the maximum power point of the PV panel is mapped into a wide range at the converter output, which is associated with stiff current and voltage limits. Assuming perfect conditions where there is no mismatch among the attached panels, and using the most popular buck-boost topology, the output characteristics of the whole smart converter array also have a stiff voltage limit.

Traditional voltage control based MPPTs, e.g. P&O and IncCond, will cause instability problems if applied to such a system, because MPPT tends to move the operating point of the system to a high-voltage area. Once the system operating point reaches the knee point, another single perturbation to the right will cause the operating point to drop down the cliff.

To deal with this problem, the R-based MPPT method is aimed at giving freedom in both the system output voltage and the current when perturbation is conducted. Instead of perturbing voltage or current, the ratio of the smart converter array output voltage and current, which can be regarded as an equivalent resistance, is chosen as the perturbation variable, as shown in Fig.1. Since the steady-state operating points are at the voltage limit, the MPPT and current-limiting region can be found, which can solve the aforementioned instability problem. This is verified by both simulation and experiment.

(a)

(b)

(c)
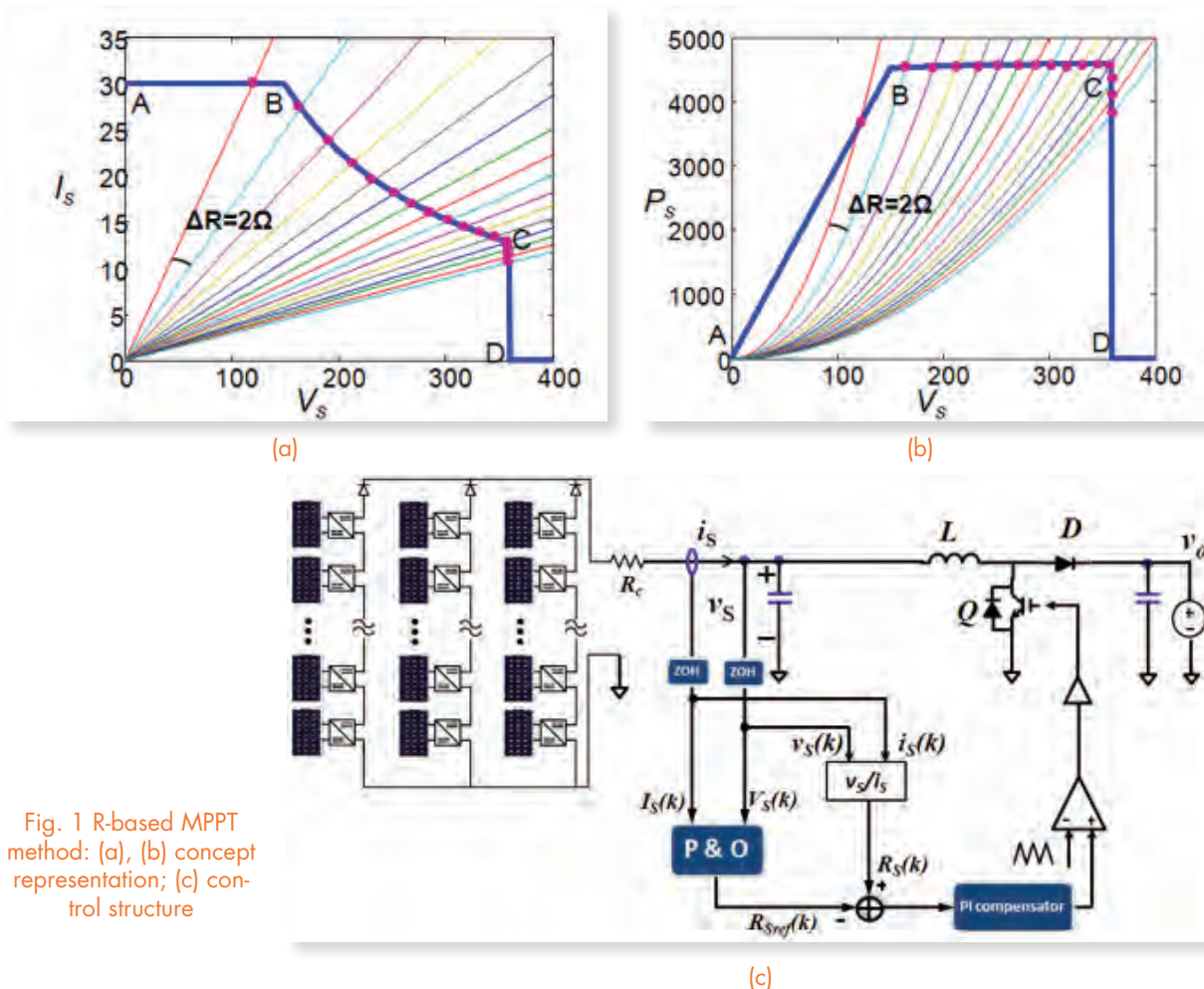
Fig. 1 R-based MPPT method: (a), (b) concept representation; (c) control structure

Inductor Structure with Improved Space Utilization

The core and winding of an inductor are designed to distribute flux so that energy is distributed uniformly in the core to utilize the magnetic material throughout the core volume. The structure proposed in this paper is designed to avoid crowding of the flux for low core loss. The winding is patterned for shorter length and larger area of cross-section for low winding loss. The footprint of a three-cell inductor is 1.48 times less than that of the conventional toroidal inductor with the same energy, maximum flux density, material properties, winding loss, and core loss.
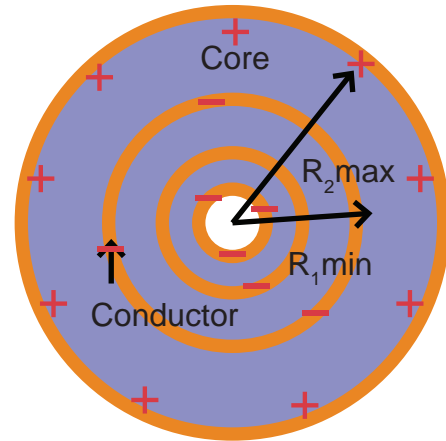
Fig. 1. Cross-section of core of 3-cell "constant-flux" inductor showing conductor and slots with + and – indicating the directions of flow of current
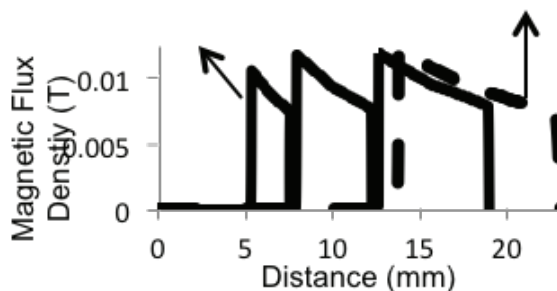
Fig. 2. Line plot of magnetic flux density of the inductor in comparison with that of toroidal inductor with same footprint area and toroidal inductor with same energy
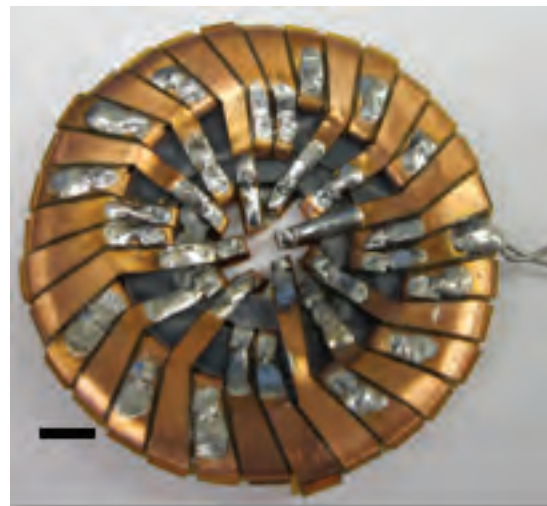
Fig. 3. (a) Three cells of inductor core made of ESL- 40010 LTCC green tape. The height is 1.4mm and the radiuses from the innermost to the outermost cell are 7.6mm, 12mm and 18.9mm respectively. (b) Three-cell constant-flux inductor with core of 40.5 x 40.5 x 2.2 mm3 made of LTCC green tape with relative permeability of 41 and winding of flat copper (of thickness 70 μm) having uniform distribution of flux density with Bmax = 0.015 T

Inter-phase Interleaving for Balanced Operation of a Three-Phase Voltage Source Converter with a Low Non-Triple Carrier Ratio

Three-phase PWM voltage source converters (VSCs) are the converters of choice in many medium- and high–power applications. For VSCs, very low carrier ratios (defined as the ratio of the switching frequency to the fundamental frequency) are usually adopted in applications with very high power requirements, where the switching frequency of high–voltage, high-current devices is very limited; and for applications with very high fundamental frequency, such as high-speed motor drives. This paper analyzes the impact of non-triple carrier ratios on the three-phase system performance infrequency domain. Specifically, the issue of system output voltage unbalance due to a non-triple integer carrier ratio, such as 7, is analyzed in detail. To mitigate this problem, a control method called inter-phase interleaving is proposed. With it, the three-phase system output voltages can be balanced, even with non-triple integer carrier ratios. The corresponding penalty of potential higher-current THD is also discussed in detail. The analysis and control method can be applied to both two-level and multi-level converters. Experimental results verify the analysis and the feasibility of the proposed control method.
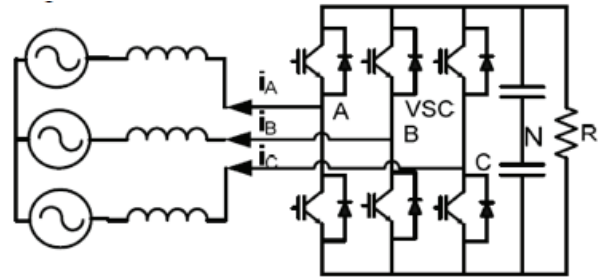
Fig. 1. Single VSC system under study
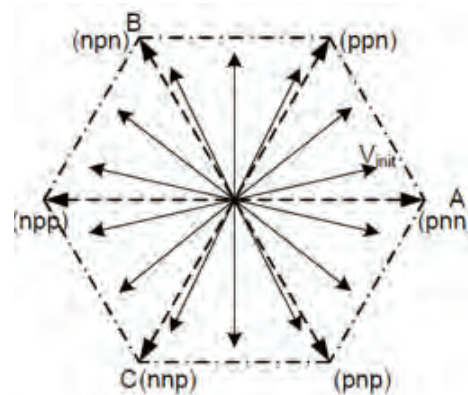
Fig. 2. Output vectors of ASVM (Rfs=7).
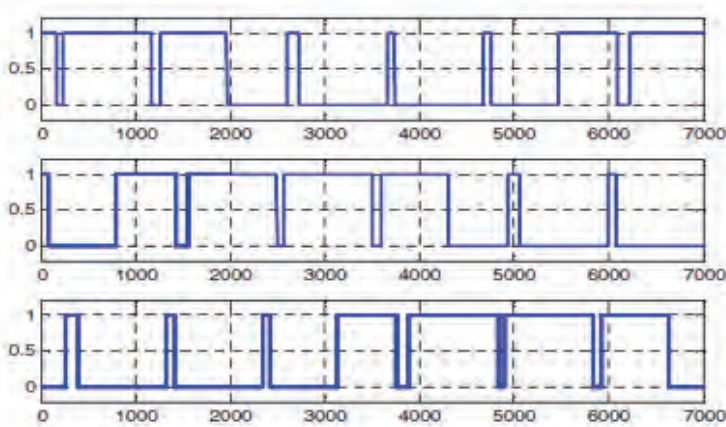
Fig. 3. Three-phase PWM waveforms for ASVM with inter-phase interleaving (Rfs =7).
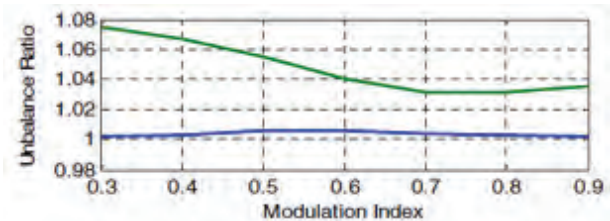
Fig. 4. Comparison of unbalanced ratio with/without inter-phase interleaving.
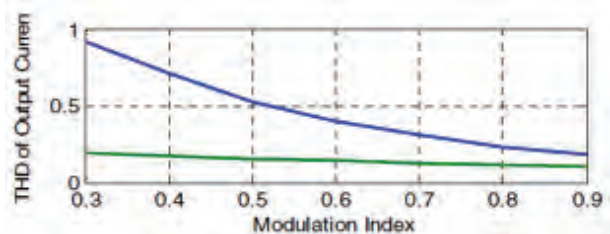
Fig. 5. Comparison of output current THD with/without inter-phase interleaving.

Frequency Behavior and its Stability in a Grid-interface Converter in Distributed Generation Systems

This paper presents a state-feedback model to predict the frequency behavior of the grid-interface converter, as shown in Fig. 1, which uses phase-locked loop (PLL) techniques, as shown in Fig. 2, to synchronize with the grid.
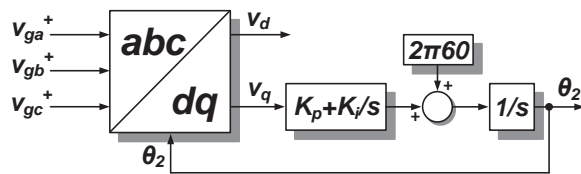
As shown in Fig. 3, the proposed model consists of two feedback systems. In addition to the typical negative feedback system, the frequency positive-feedback mechanism in the converter system is proposed and quantified in the model. The nonlinear behavior of the PLL under weak grid conditions can be accurately predicted, and the large-signal frequency stability region can be also estimated by the proposed model. It shows that large penetration of distributed generation (DG) units, a large reactive power variation, and a weak grid tend to destabilize the converter frequency operation. The proposed model can help study electric power system or microgrid operation under a large penetration of renewable energy resources with power electronic interfaces.

Fig. 1 Grid-interface converter under study

Fig. 2 Synchronous reference frame PLL
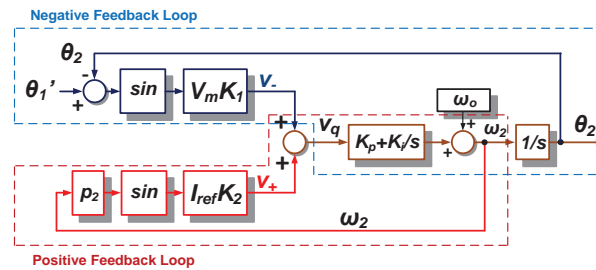
Fig. 3. Proposed PLL model
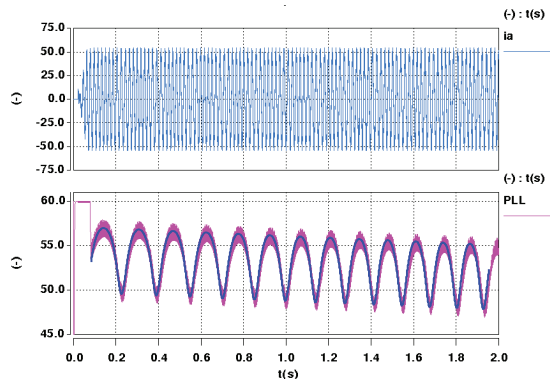
Fig. 4. Switching converter simulation results ω_2 (purple) [5 Hz/DIV], one-phase current ia (blue) [25A/DIV], and proposed PLL model output ω_2 (dark blue).

A Novel Anti-islanding Detection Algorithm for Three-phase Distributed Generation Systems

This paper presents a novel anti-islanding (AI) detection algorithm for three-phase (3) grid-interface converters, as illustrated in Fig. 1, in distributed generation systems. The synchronous reference frame PLL is widely used, as shown in Fig. 2. According to the analysis, the PLL output frequency can be directly observed to detect the islanding event, since the output will run out of the steady state (60Hz).
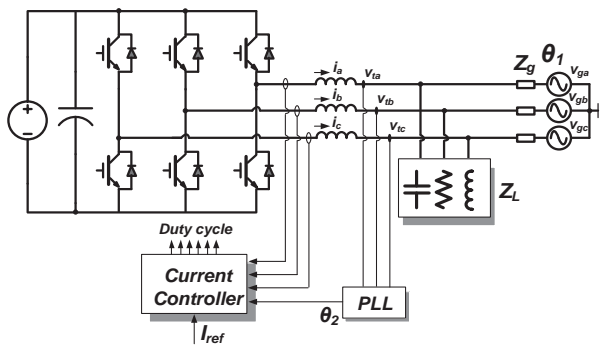
Fig. 1 Grid-interface converter under study

However, the PLL will be stable at 60Hz after the islanding event if the local load is the RLC load with 60 Hz resonant frequency. In order to effectively detect the islanding condition under this load, the SRF PLL is modified to be unstable when islanding occurs. As shown in Fig. 3, an additional feedback loop is used to destablize the PLL under islanding conditions.

Fig. 2 Synchronous reference frame PLL

As shown in Fig. 4, when islanding occurs, the PLL output will be unstable using the proposed method. The proposed algorithm has a small impact on the converter system operation and can be implemented easily.

Fig. 3. Proposed PLL for anti-islanding detection
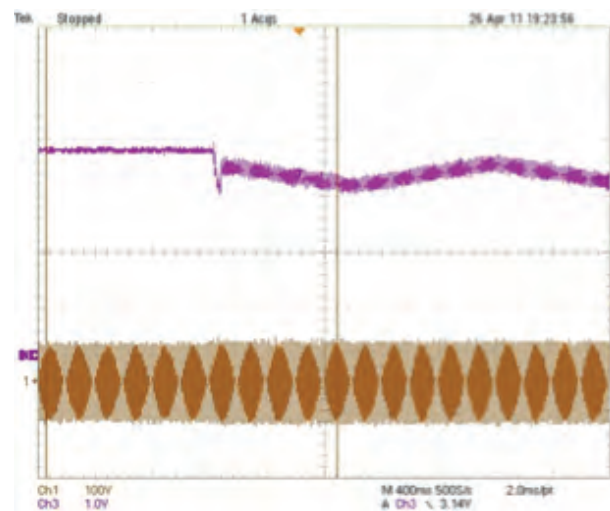
Fig.4.The proposed PLL output when islanding occurs:
 2 (purple) [6 Hz/DIV], one-phase voltage va (maroon) [100V/DIV]

Common-Mode EMI Noise Reduction for a Grid-interface Converter in Low-voltage DC Distribution System

Special attention is given to the electromagnetic interference (EMI) issues that arise in grid-interface converter systems where the radio frequency (RF) conducted emissions have to be considered on both the dc and ac sides, such as in the application of photovoltaic (PV) system, dc distribution systems, and charging systems in electric vehicles (EVs). This paper presents a brief overview of the recent EMI research activities in such applications as well as EMI filter design and measurement considerations.

Common-mode (CM) conducted EMI noise poses particular challenges to filter design in the grid-interface converter systems because the noise propagation paths are coupled between the dc and ac sides through the grounding capacitors. As shown in Fig. 1, the ac filter strucure not only reduces the leakage current on the dc-side, but also highly reduces the ac-side CM noise propagated into the single-phase utility. Thus, the total passive filter volume could be reduced. In addition, this ac filter strucure can also decouple the impact of the dc-side CM capacitors to ac-side CM noise level, which reduce the filter design process where both dc and ac-side EMI noise has to be attenuated.

As shown in Fig. 2, the investigated ac filter achieves a strong ac CM noise reduction compared to the typical ac filter strucure.
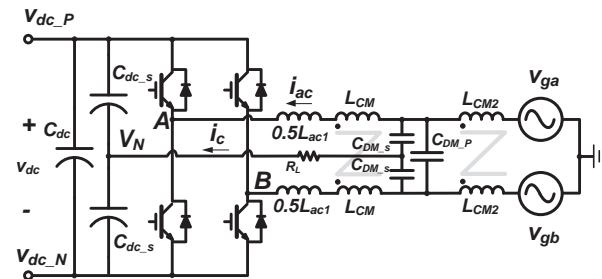
Fig. 1 Single-phase full-bridge with proposed ac filter structure
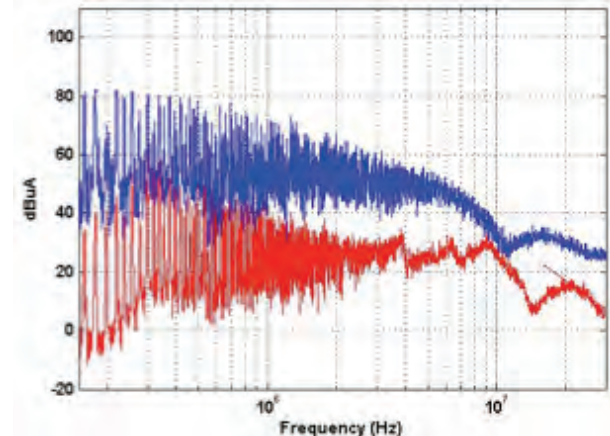
Fig. 2. Ac-side CM noise measurement with (red) and without (blue) the floating filter when the heatsink is floated.

Intergrid: A Future Electronic Energy Network?

The anticipated widespread usage of new power electronics technologies in electrical energy generation and consumption is expected to provide major efficiency improvements, while the deployment of "smart" grid technologies should improve the utilization and availability of electricity. This paper explores possible relationships between these two trends. Starting with an analysis of current and expected trends in the generation, transport and consumption of electrical energy, the paper contemplates possible future ac and dc electronic power distribution system architectures, especially in the presence of renewable energy sources. The considered nanogrid–microgrid–…–grid structure achieves hierarchical dynamic decoupling of generation, distribution, and consumption by using bidirectional electronic power converters as energy control centers.

It is quite imaginable that in the future, energy flow could be represented in the way shown in Fig. 1. Compared to today's scenario, there could be greater utilization of renewable and nuclear energy, with highly reduced engagement of biofuels, natural gas and petroleum. This possible scenario could be expected in 10, 20, or 30 years from now, and it would require electric energy infrastructure that is a double of today's in size and capacity.

To address this problem, it is then necessary to consider that the architectural concept of the future grid could consist of a number of semi-autonomous nanogrids with nanogrid Energy Control Centers (nECC) combined to form a bigger microgrid system, which in turn is interfaced to a higher-level distribution through a substation μECC, and so on, as shown in Fig. 2. The resulting system is a hybrid mix of ac and dc architectures comprising, pico-, nano-, micro-, and sub-grids that are dynamically decoupled and hierarchically interconnected to form a novel electric power grid structure: the intergrid.
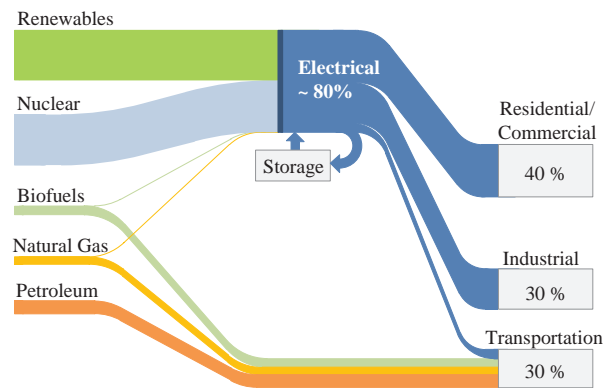
Fig. 1. A possible energy flow in a sustainable future
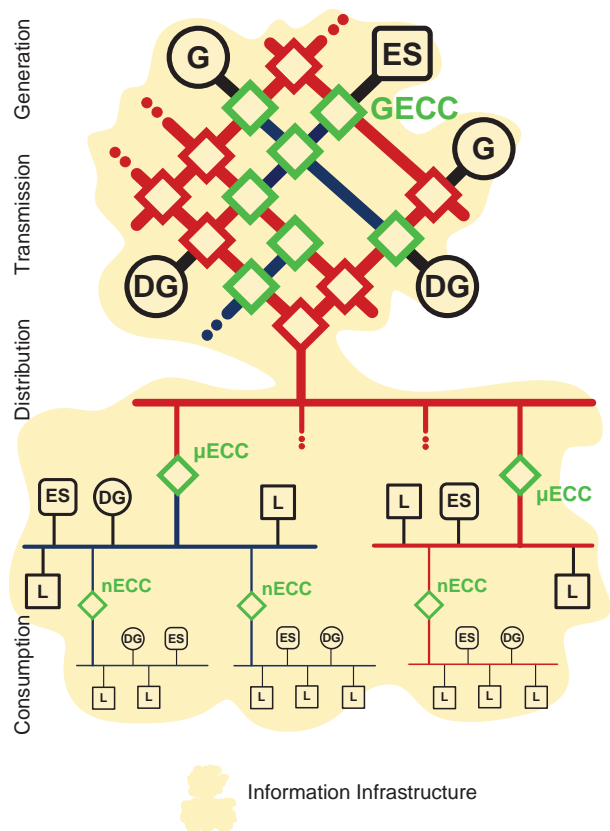
Fig. 2. Conceptual intergrid system structured as a hierarchical network of dynamically decoupled electronically interconnected sub-networks.

Analysis and optimization of a Smart Panel-Based PV Converter System

Residential PV systems always suffer from power loss that results in poor performance due to mismatches. Addressing and minimizing the power loss of PV systems under such conditions is critical to improving PV system efficiency in residential applications. A module composed of a PV panel with a dedicated MPPT DC-DC converter, which we call a smart panel, is proposed and illustrated in Fig. 1(a).

(a)
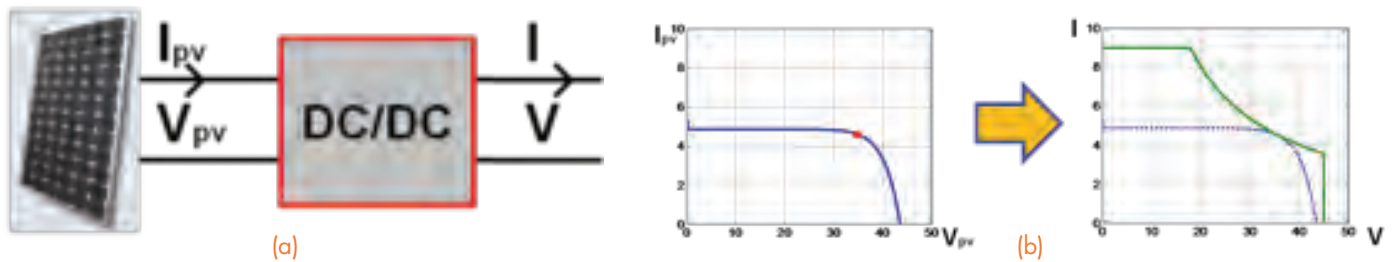
Fig. 1 Concept of smart panel   (a) Smart panel concept   (b) Input and output I-V curve of smart panel

The PV panel-level converter decouples the PV panel from other panels, and Fig. 1(b) shows its output curve mapped to a wide MPPT range. Due to safety and device rating issues with the smart converter (SC), voltage limitations and current limitations are added for protection.

Compared with a traditional centralized PV system, as shown in Fig. 2(a), a smart panel-based PV system, as shown in Fig. 2(b), offers advantages such as independent MPPT control, maximized solar power utilization, and flexible system architecture design. Through analyzing principles and the modeling of the smart panel-based PV system, we can determine that the common MPPT region of all the panels remains forever in the range shown in Fig. 2(c); a laxer limitation is shown in Fig. 2(b) for comparison.

Studying a small shading case inside the PV panel, such as bird droppings or a fallen leaf, indicates that this small shading has a disproportionate impact on energy production. A smart converter for PV cell strings is proposed to tackle such problems. Compared with other topologies of smart converters, a series connection of buck subpanel smart converters has been adopted, as shown in the upper part of Fig. 3(a), and the subpanel MPPT structure is optimized, as shown in the lower part of Fig. 3(a), which makes the solution much easier without suffering significant power loss. The detail control diagram is shown in Fig. 3(b).

(a)   (b)   (c)
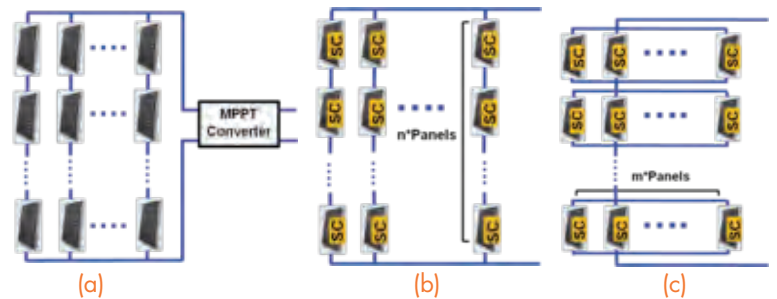
(a) Centralized MPPT (b) Smart panel based PV system (c) Optimized PV system
Fig. 2 Residential PV system architectures
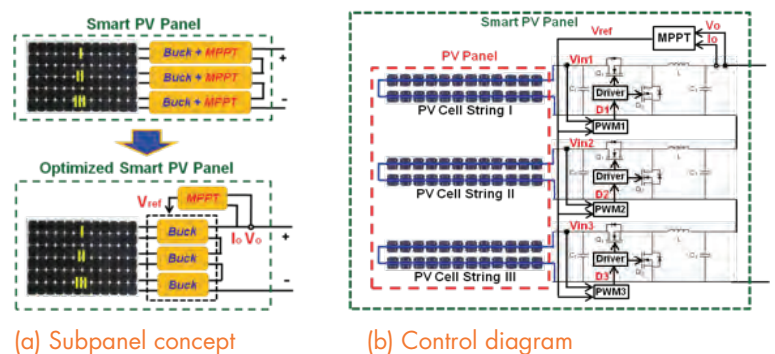
(a) Subpanel concept   (b) Control diagram
Fig. 3 Subpanel smart converter

Analysis of EMI Terminal Modeling of Switching Power Converters

CPES has been working on behavioral EMI-modeling techniques for nearly a decade. Over the years we have developed and improved several techniques and have tested them in applications ranging from dc-dc converters to three-phase inverters.

For this modeling technique, a generic three-terminal Norton equivalent was chosen as the noise model. This is shown in Fig. 1. The model is extracted by taking EMI measurements on the terminals of the converter under different conditions, and then simultaneously solving network equations for each of the conditions. The model was validated with experiments, and the EMI prediction results are shown in Fig. 2.

We have now focused our efforts on understanding the physical nature of EMI noise, as it is important that a connection be established between the model and the physics of the converter. Several points have been investigated, including the key issue of modeling non-linear time-variant converters with linear and time-invariant (LTI) circuits. Our experiments revealed that the parasitic inductance of the dc-bus and the input capacitor provides a constant and dominant impedance at the input
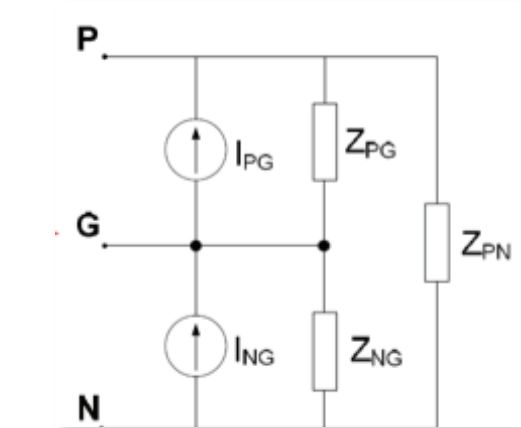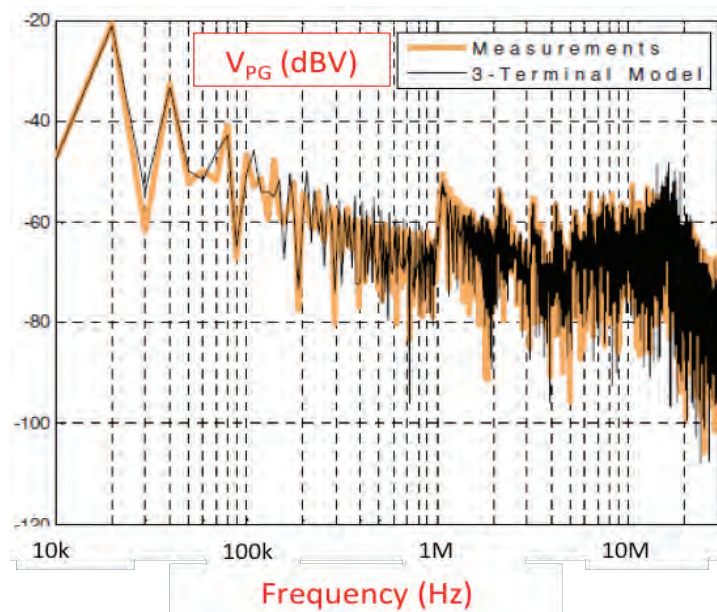
Fig. 1. Three-terminal noise model for terminal EMI modeling

of the converter, thus masking its time-variant behavior.

The other issue that was found and investigated was regarding the nature of extracted model impedances. It was found that in the extracted impedances of the terminal model, the real impedance was turning out to be negative at certain frequency points. This is was due to the small amplitude of the measured voltages at those points as well as the smaller size of the real part in comparison with the ideal part of the impedance. The issue was corrected with peak detection during a post-processing step. With these improvements, the impedances now have a physical meaning and the model can be run even in a circuit simulator. This is advantageous as one can now simulate EMI filters, cables, and the like with a terminal model to evaluate their effect on EMI.

Thanks to the investigations above, we have developed a more complete understanding of the limitation and pitfalls of the method, which will help in future development of the method itself.

Fig. 2. Prediction of conducted emissions on the LISN from the three-terminal model

Common-Mode EMI Terminal Modeling of DC-Fed Motor Drives

CPES has developed EMI behavioral models of dc-fed converters to predicted conducted emissions. The modeling technique was validated on buck, boost and ac converters such as half-bridge and three-phase inverters. Fig. 1 shows the terminal EMI behavioral model for a buck converter.

However, this model has two major limitations. The first limitation is that the models are valid only for one operating point; that is, re-modeling is needed if EMI prediction is needed for a different operating point. The second limitation was that the model is terminated, by which we mean that the load side of the converter is fixed. Thus the model in Fig. 1 can only predict conducted emission on the converter's input side, and once identified, it cannot be used to predict input-side EMI due to changes at the load side. This limitation is due to the black-box nature of the model, which means the load and its associated parasitics have been lumped together in a generic delta-network of impedances (ZPG, ZNG and ZPN). It is impossible to separate the load side from these impedances once the model is extracted.

In aerospace applications, however, the DO-160 standards dictate EMI limits on differential-mode (DM) and common-mode (CM) currents on all harnesses and cable assemblies. Thus for applications like motor drive systems, it becomes necessary to be able to predict changes in conducted emission at the dc side due changes at the ac side or vice versa. To solve this problem, the three-terminal model was modified to predict both dc-side and ac-side EMI noise on a motor drive system. Fig. 2 shows the motor drive and Fig. 3 shows its three-terminal behavioral EMI model. The model is a Thevenin equivalent

Fig. 1 Generalized three-terminal model of buck-converter based on Norton equvalent

with two noise sources and a two-port impedance matrix. Currently only CM noise is addressed, as at high frequencies it is the CM noise that is the most troublesome. The model parameters were calculated again by measurements in an in-circuit test. The model was validated by predicting dc-side and ac-side CM noise currents for a CM choke at the dc side and Y-capacitors at the ac side. These predictions are shown in Fig. 4. It is seen that the model predicts well, with the exception of some discrepancies around 1 MHz. At around 1 MHz, the S/N ratio was found to be poor due to the small amplitude of the measured voltages.

The future work includes improvement in model identification and predicting changes in the length of the harness (see Fig. 2). We also plan to research the prediction of EMI for changes in the operating conditions. This
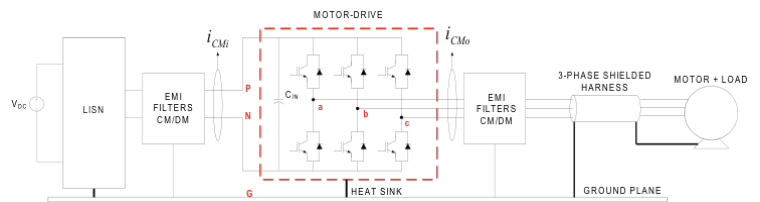
Fig. 2 Set-up of de-fed motor drive system

model can be very useful in understanding the interaction of dc and ac side EMI in a motor drive system and helping in the development of methods for the co-design of EMI filters for both sides.
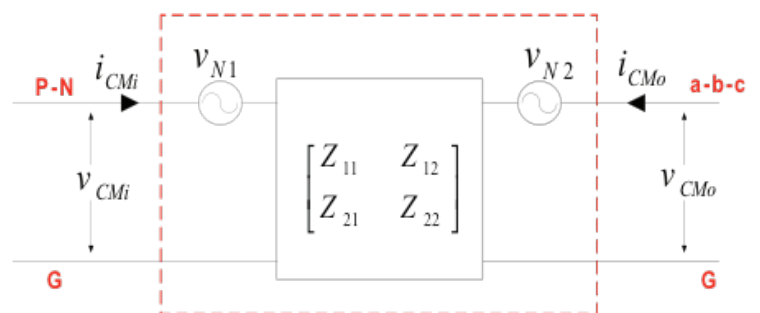
Fig. 3 Terminal model of the motor drive in CM

Un-terminated, Low-frequency Terminal-behavioral d-q Model of Three-phase Converters

The frequency-domain terminal-behavioral modeling of ac systems has been attracting more and more interest in engineering practice. New electronic power distribution systems built for airplanes, ships, electric vehicles, data-centers and even homes comprise a variety of power electronics converters with very different dynamic characteristics. If their behavior is not examined carefully before the system is integrated, instability can become a major concern. This work addresses low-frequency terminal-behavioral modeling of three-phase converters whose dynamics can be captured online in a non-intrusive way, and later decoupled from the source and load in order to get un-terminated model of a converter, or even a larger system.

The four-port network can be directly used to build the small-signal linear model of the ac-ac converter around the particular operating point (Fig. 1). The four matrices of transfer functions (2x2 each) can be defined as: Go- audio susceptibility, Zo- output impedance, Yi- input admittance and Hi- back current gain. The terminal-behavioral model consists of four separate sets of measurements on the 3-phase converter working at a desired operating point. Although 16 un-terminated transfer functions describe dynamics of the converter, a total of 24 functions need to be measured to decouple the source and load dynamics from the measured transfer functions.

Using two more matrices, transconductance and transresistance, the transfer functions must be decoupled, or "un-terminated," in order to fully characterize the dynamics of a particular converter. Expression (1) presents a generalized linear transformation that derives the un-terminated transfer functions from the measured, terminated functions (denoted with the letter m in the index) for any ac-ac, ac-dc, dc-ac and dc-dc converter. The result of decoupling is shown in Fig. 2.
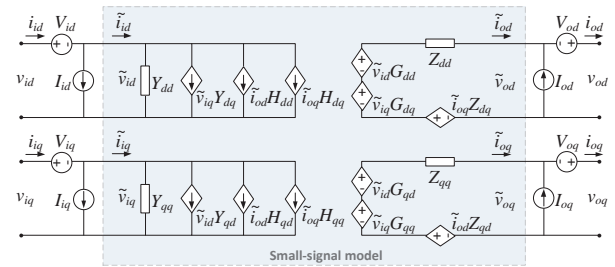
Fig. 1 Two port network terminal-behavior model
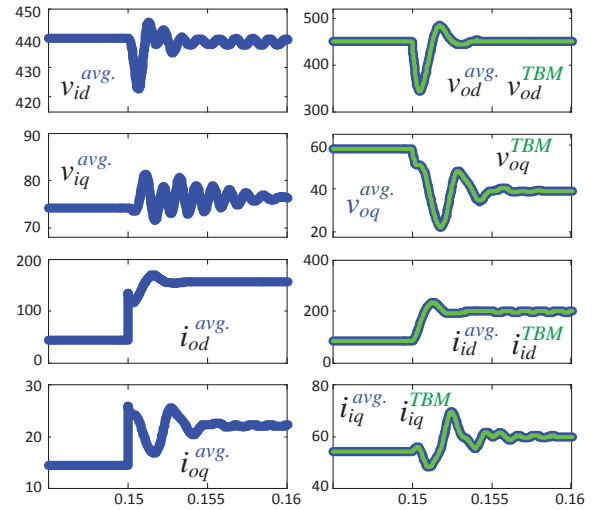
Fig. 2 Ac-ac converter time domain responses in d and q axes for the given load step, and comparison with the termial behavioral model

$$\begin{bmatrix} \mathbf{G}_o^x & -\mathbf{Z}_o^x \\ \mathbf{Y}_i^x & \mathbf{H}_i^x \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{om}^x & -\mathbf{Z}_{om}^x \\ \mathbf{Y}_{im}^x & \mathbf{H}_{im}^x \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}^x \end{bmatrix}^{-1}$$

where $\mathrm{x} = \{ \mathrm{ac-ac,\ ac-dc,\ dc-ac,\ dc-dc} \}$

Dynamic Interactions in Hybrid AC/DC Electronic Power Distribution Systems

Hybrid electronic power distribution systems have the majority of their loads interfaced to energy sources through power electronics converters. Furthermore, all alternative, sustainable, and distributed energy sources can only be connected to the electricity grid through power electronics equipment. However, one of the main challenges in designing and developing of these hybrid ac/dc systems has been the modeling and analysis of dynamic interactions between converters at the synchronous frequencies and above. To address these problems, this work employs terminal-behavioral modeling of power converters as a possible methodology for analysis, system-level design, and study of stability subsystem interactions.

The unstable operation of the power distribution sub-system depicted in Fig. 1 occurs as a result of insufficient bus capacitance Cb. Fig. 2 shows the time domain responses in both stable and unstable cases.

The Bode plots of the impedances at the DC interface (shown in Fig. 2) were obtained using small-signal analysis with the average model of the system, shown in Fig. 1. The load input impedance clearly shows the CPL characteristic up to a few kilohertz (ZL ≈ −180°). Under the stable case shown in the Bode plots in Fig. 2a, the magnitude of ZS is lower than ZL with a sufficient margin, while in the case shown in Fig. 2b, an equivalent source impedance resonant peak interacts with ZL, leading to unstable operation after the sudden load step at 0.1 s. The stability of the system in Fig. 1 highly depends on the return ratio,

$$(1) \quad L(s) = Z_S(s) \cdot Y_L(s)$$

which for the stable systems must not encircle point -1. Nyquist diagrams for both stable and unstable case are shown in Fig. 2.

Similarly, for the arbitrary ac system, the loci of the eigenvalues of return ratio L(s) (shown in (2)), as specified in the generalized Nyquist stability criterion (GNC), must not encircle the -1 point.

$$(2) \quad \begin{bmatrix} e_d(s) \\ e_q(s) \end{bmatrix} = \mathbf{eig}\ \ (s)\ \ \mathbf{g}\,(\mathbf{Z_S}(s) \cdot \mathbf{Y_L}(s))$$

The paper provides examples of dynamic interaction, and raises possibility of addressing stability by employing terminal-behavioral modeling.
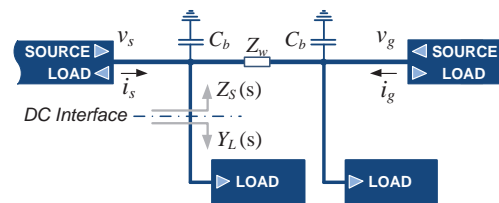
Fig. 1. DC subsystem under test

(a) stable case: (b) unstable case:
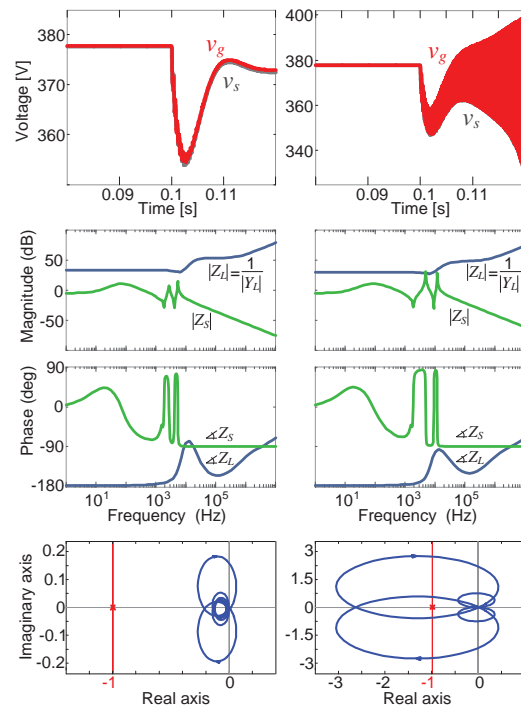
Fig. 2. Time-domain, frequency response waveforms and Nyquist diagrams of the return ratio for (a) stable, and (b) unstable cases at the DC Interface in Fig. 1.

Finite Element Analysis of Inductor Core Loss Under DC Bias Conditions

The finite element method is a popular way to analyze the magnetic core loss in complex core structures. However, accurate calculation of the inductor core loss under DC bias conditions is still a challenge, because magnetic properties like permeability and core loss density change when a DC pre-magnetization is present; especially for a saturable core. This paper proposes a method which can accurately calculate the inductor loss under DC bias current conditions. The method utilizes the material model built by curve-fitting the measurement data, and the model is effective and simple. To verify this approach, planar inductors with low-temperature co-fired ceramic (LTCC) ferrite are simulated, and the calculated core losses are experimentally verified.

Fig. 1. LTCC 40011 relative incremental permeability with Hdc
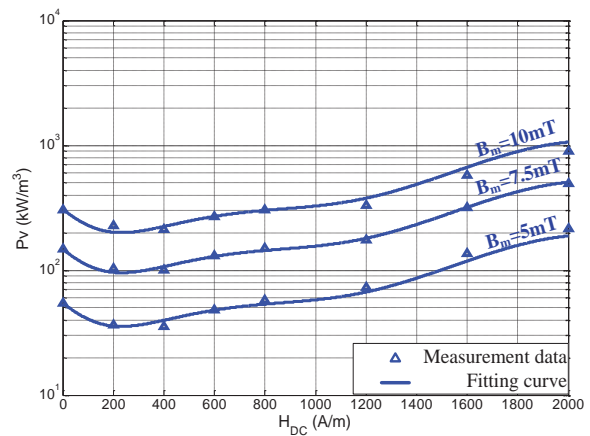
Fig. 2. LTCC 40011 core loss density as a function of Hdc (1.5MHz)
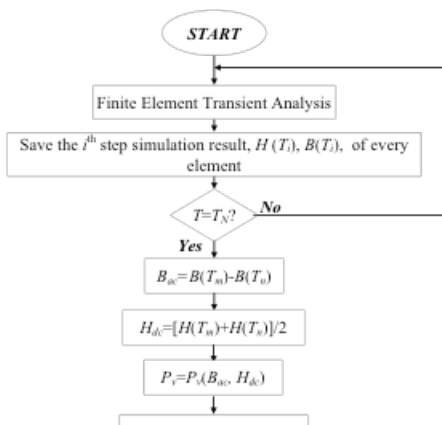
Fig. 3. Simulation flow chart
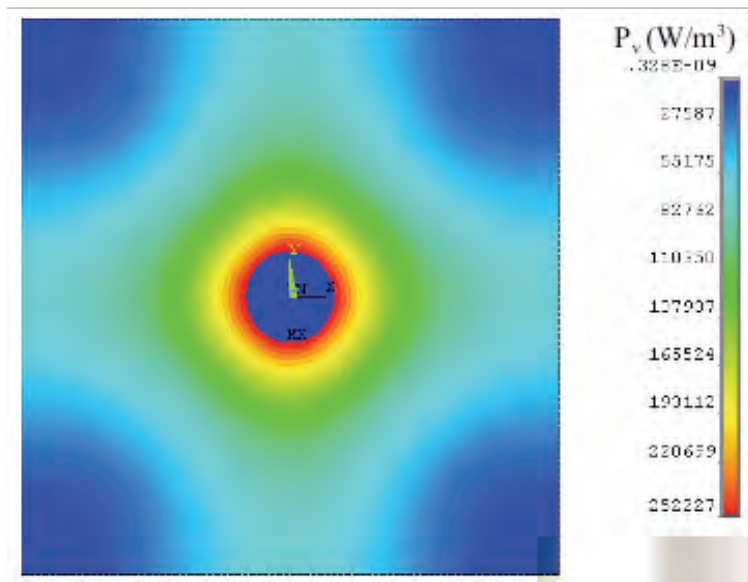
Fig. 4. Simulated core loss density distribution

High–Frequency, High Power Density 3D Integrated Gallium Nitride-Based Point-of-Load Module

Non-isolated POL converters are widely used in computers, telecommunication systems, portable electronics and many other applications. To design a high-power-density POL module, high switching frequency, high efficiency, small magnetic size, and good thermal management are all required. Silicon devices are not capable of good performance at an operation frequency of a couple of MHz. However, GaN devices are high-electron-mobility transistors (HEMT), and have a higher band gap, electron mobility, and electron velocity than silicon devices and offer potential benefits for high-frequency power conversion. With the depletion-mode GaN MOSFET from International Rectifier, a 3D integrated POL module has been designed to operate at up to 5MHz switching frequency for a 12V to 1.2V buck converter with a full-load current of 15A. This module employs a low-profile low-temperature co-fired ceramic (LTCC) inductor and can achieve a full-load efficiency of 82%, and 1200W/in3 power density at 5MHz.
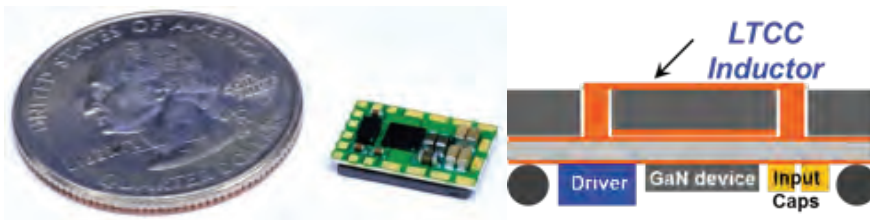
Fig. 1 3D integrated GaN based POL module
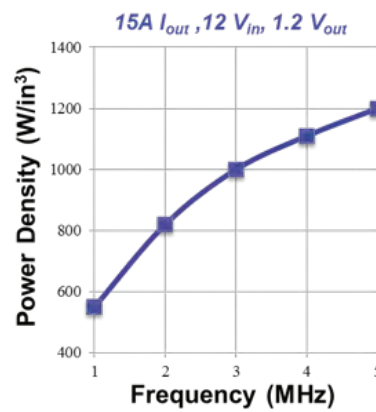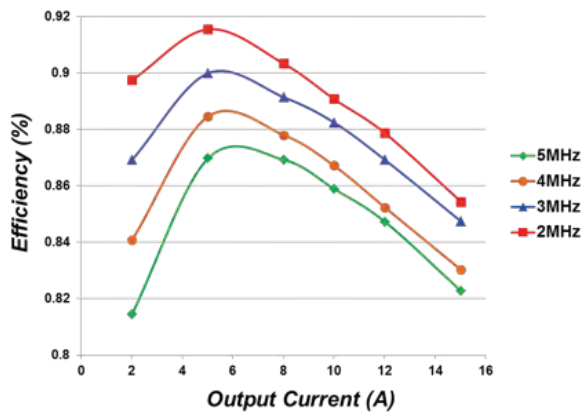
Fig. 2 Module efficiency and power density

EMI Noise Attenuation Prediction with Mask Impedance in Motor Drive Systems

This work presents insertion gain predictions for both the differential mode (DM) and the common mode (CM) of an EMI filter. The proposed approach, essentially based on measurements, allows prediction of EMI filter performance for high-complexity converters without time-consuming simulations. The key idea is to use direct measurements to represent a complex system by an equivalent circuit in the frequency domain. The source impedance, which is the more complex part of this equivalent circuit because of its non-linear time variation, is generally masked by external impedance and can be treated as a linear system. Experimental results for insertion gain prediction are included for second-order filters for both DM and CM on a three-phase SiC JFET Vienna/two-level converter.
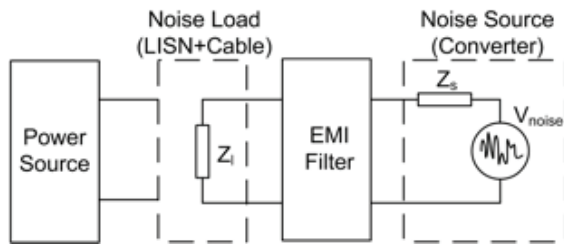
Fig. 1 Equivalent circuit to predict EMI filter insertion gain
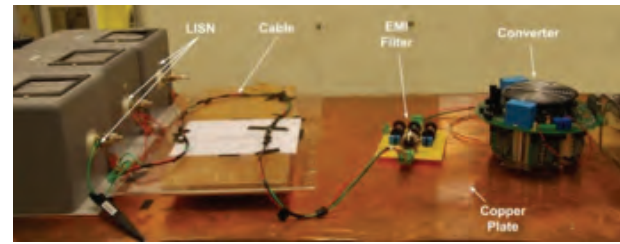
Fig. 2 Experimental test setup
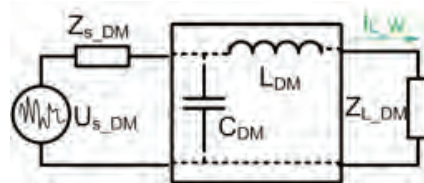
Fig. 3. Insertion gain calculation based on the impedance
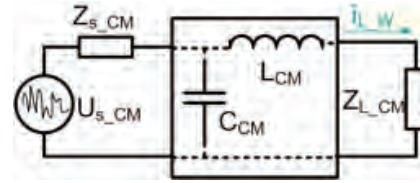
$$IG = \frac{1 - \dfrac{Z_{sDM}}{Z_{sDM} + (Z_{fC\_DM} \parallel (Z_{fL\_DM} + Z_{LDM}))}}{(Z_{fL\_DM} + Z_{LDM})(Z_{LDM} + Z_{sDM})} \quad (1)$$

$$IG = \frac{1 - \dfrac{Z_{sCM}}{Z_{sCM} + (Z_{fC\_CM} \parallel (Z_{fL\_CM} + Z_{LCM}))}}{(Z_{fL\_CM} + Z_{LCM})(Z_{LCM} + Z_{sCM})} \quad (2)$$
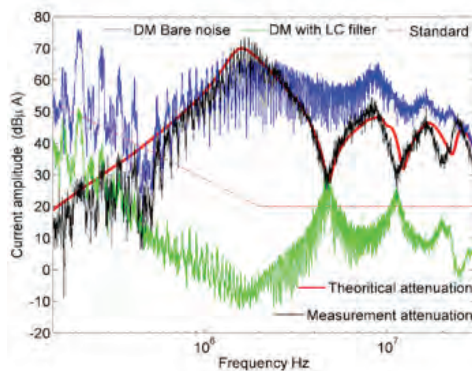
Fig. 4. DM insertion gain prediction
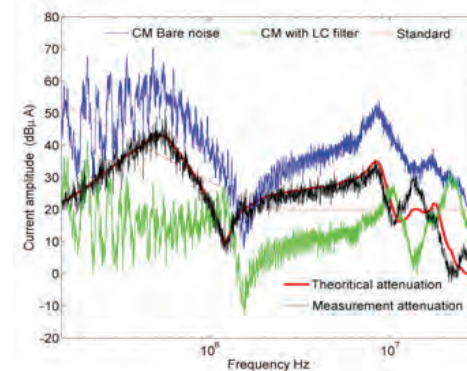
Fig. 5. CM insertion gain prediction

High Power Density EMI Filter Design with Consideration of Self-Parasitic

A compact EMI filter has become one of the critical requirements for a high-power-density converter design, especially in transportation applications. This paper proposes a design procedure for a more compact EMI filter with consideration of both low-frequency and high-frequency attenuation requirements. For the sake of simplicity, EMI filter trans-fer gain is utilized to conduct the analysis. With the proposed method, the best stage number and components value can be systematically derived for a given fixed operating point. From the design results, the multiple-stage EMI filter has a minimum volume even when the low-frequency and high-frequency attenuation requirements are high.
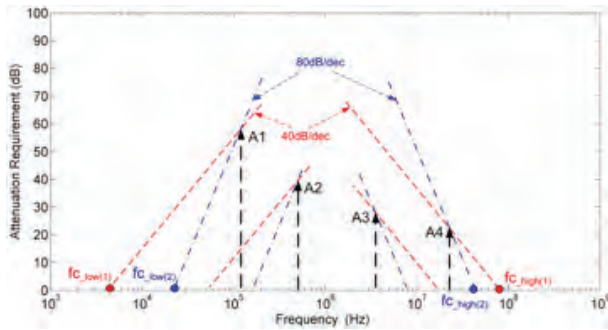
Fig. 1. Attenuation requirement for low and high frequencies
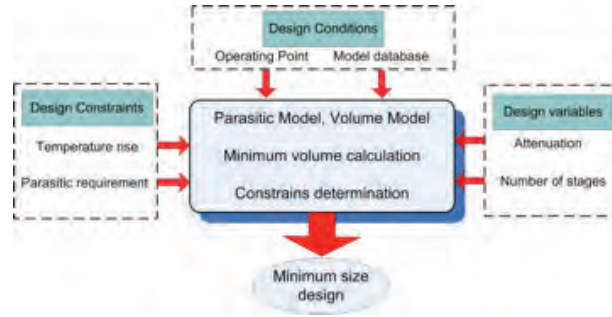
Fig. 2. Design procedure
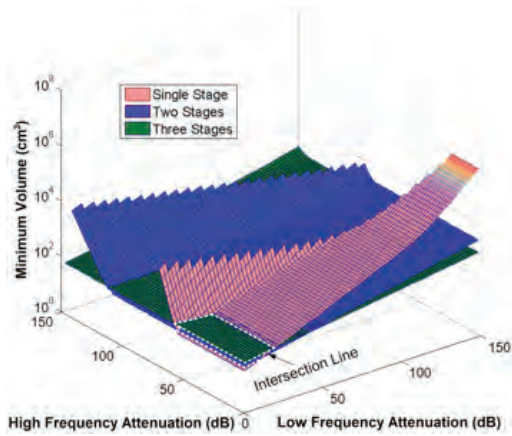
Fig. 3. Minimum volume design
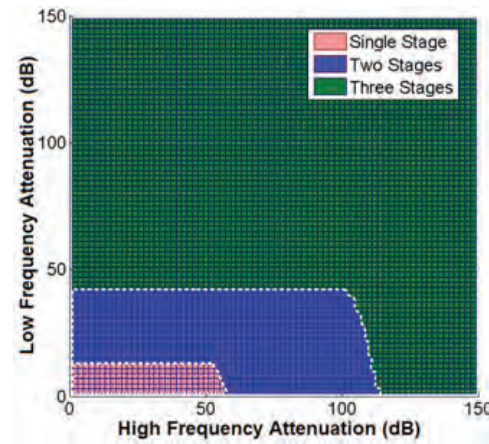
Fig. 3. Single stage or multiple stage selection

Optimal Trajectory Control of LLC Resonant Converter for LED PWM Dimming

Recently, the developers of many applications, such as display backlighting, indoor lighting and street lighting, have all favored multi-channel LED drivers. This paper proposes a novel PWM dimming solution with optimal trajectory control for a multi-channel constant current (MC3) LLC resonant LED driver. When PWM dimming is on, the LLC resonant converter operates under the full-load condition. The LED intensity is controlled by the ratio between the on-time and off-time of the PWM dimming signal. To eliminate dynamic oscillation when the MC3 LLC starts to work from the idle status, the first pulse-width of the gate driving signal is tuned based on the state-plane trajectory analysis. Thus the full-load steady state is settled within a minimal time. Under low dimming conditions, the LED intensity can be controlled more precisely.
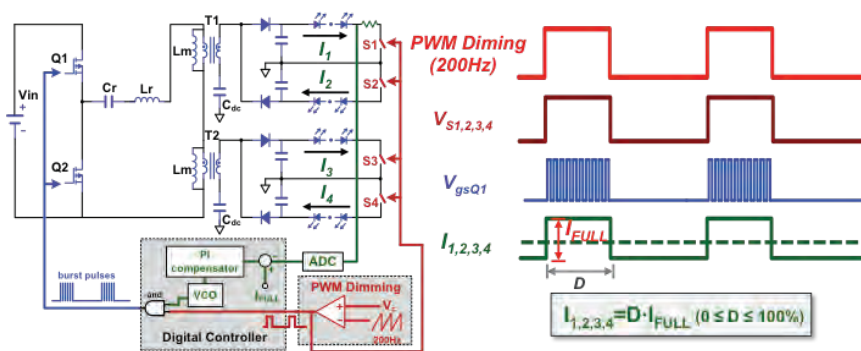
Fig. 1. MC3 LLC resonant converter LED driver with PWM dimming control
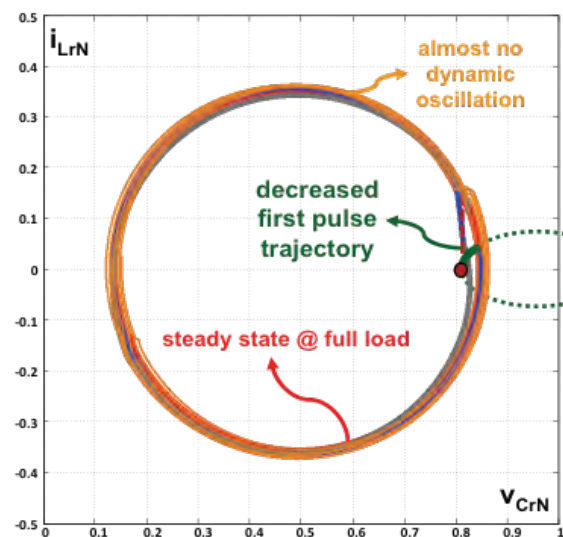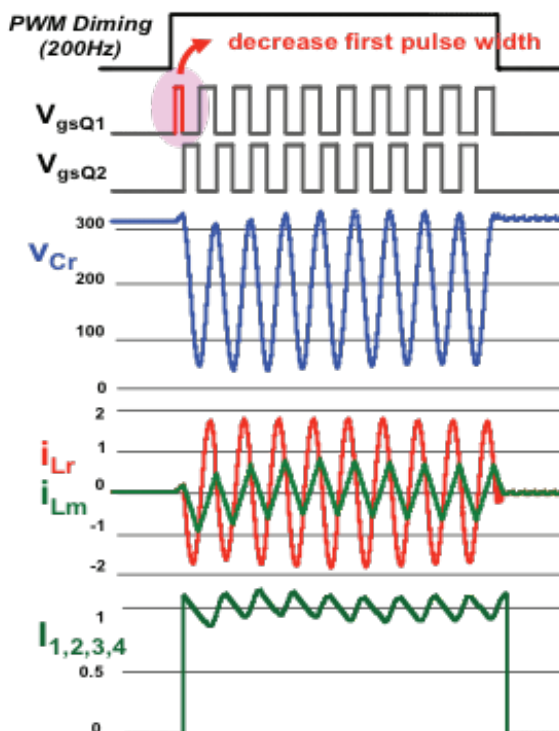
Fig. 2. Optimized pulse pattern for LED PWM dimming

Fig. 3 State-plane trajectory of optimal LED PWM dimming control

Compensation of DC-Link Pulsation in Single-Phase Static Converters

Single-phase AC power has a typical frequency that corresponds to twice the electrical grid frequency. Processing of such power made by voltage source converters (VSC) or current source converters (CSC) means there is a low-frequency oscillation of current or voltage along the DC link in the VSC or CSC, respectively. In order to avoid interference from these oscillations during power processing, it is necessary to use a large capacitor or inductor as part of the VSC or CSC. These oscillations degenerate the quality of power processing and are present in both operation modes: rectifier (AC-DC converter) and inverter (DC-AC converter).

In terms of hardware, compensation of such oscillating power can be achieved by adding an auxiliary leg and a energy storage circuit element to a standard converter. Here, these constitute the oscillating power compensator. The energy storage element is responsible for absorbing and delivering the oscillating power, which is naturally required by a single-phase converter. A general (VSC/CSC) single-phase converter, with power compensator, is presented in Fig. 1(a). Fig. 1(b) illustrates the particular composition for a VSC and CSC, with oscillating power compensation included.

(a) Generalized converter with oscillating power compensation   (b) Legend for VSC and CSC
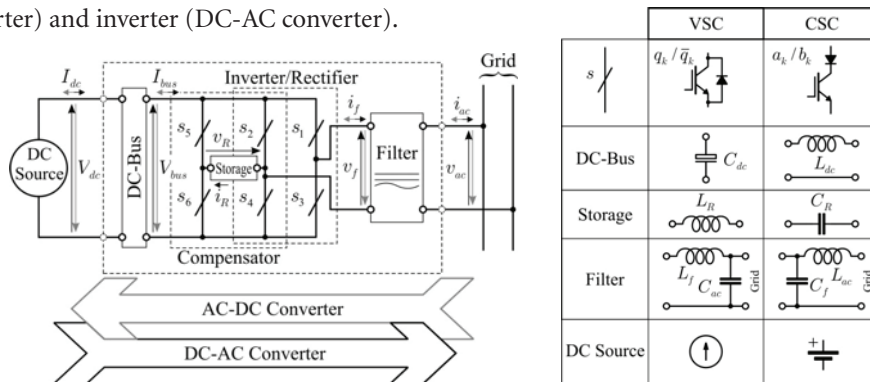
Fig.1 Single-phase AC converter

Fig. 2(a) shows AC voltage and current waveforms related to single-phase (VSC/CSC) converters. In Figs. 2(b) and 2(c) are shown the waveforms for the power compensator working as a rectifier and as an inverter, respectively. In order to achieve an effective compensation, the power compensator needs to generate a voltage, as illustrated in Figs. 2(b) and 2(c) (top). In Figs. 2(b) and 2(c) (bottom) is shown the behavior of the power on the AC side, DC bus and the compensator. It is possible to see that the power oscillation does not spread across the converter, so the power in the DC bus is continuous.

Fig. 2. Waveforms of the converters with oscillating power compensation, where (b) and (c) (top) are in the compensator side and (bottom) are the power in the converters
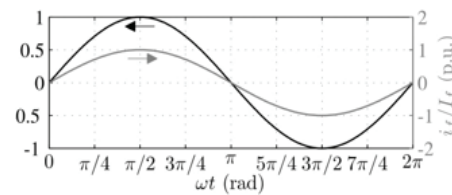
(a) Grid side
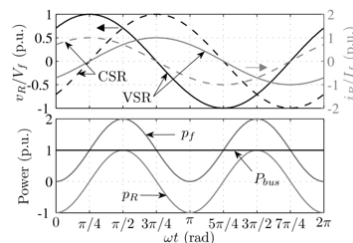
(b) Working as rectifier

(c) Working as inverter

Compensation of DC-Link Oscillation in Single-Phase to Single-Phase VSC/CSC and Power Density Comparison

This study proposes a technique to reduce the low-frequency DC link energy oscillation that occurs due to pulsating single-phase energy flow in a single-phase to single-phase voltage source converter (VSC) and current source converter (CSC) which operate connected to the grid. That pulsating energy is the major contributor to an increase in size of the passive components and the power losses in the converter. The pulsation reduction is achieved by incorporating two auxiliary active switches and one passive energy storage element to the rectifier and inverter side. Here, they will constitute the oscillating power compensator. The energy storage element will be responsible for absorbing and delivering the oscillating power, which is naturally required by a single-phase converter. The proposed (VSC/CSC) single-phase to single-phase converters, with power compensators, are presented in Fig. 1. Fig. 1(a) illustrates the topology for the VSC. In this case, the energy storage elements are the inductors $L_{(R_r)}$ and $L_{(R_i)}$. For the CSC, shown in Fig. 1(b), the storage elements are the capacitors $C_{(R_r)}$ and $C_{(R_i)}$. Additionally, these convertes are compared in terms of efficiency and power density.

Fig. 1. Proposed single-phase to single-phase converters with oscillating power compensation.
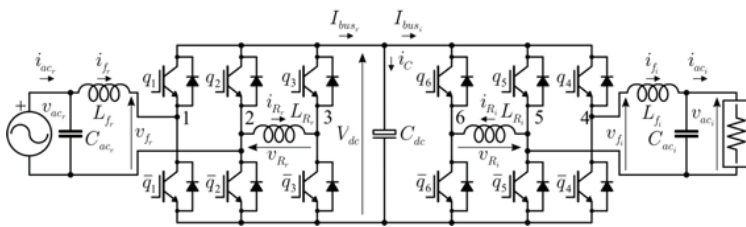
(a) VSC.
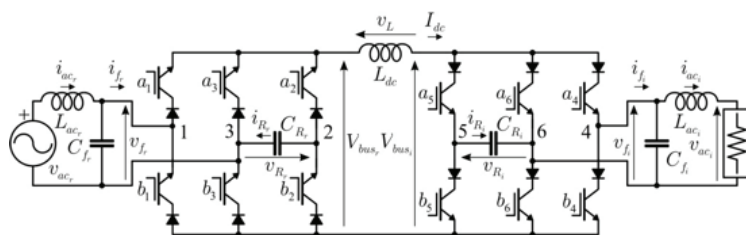
(b) CSC.

In Fig. 2 are a comparison and simulation results for the converters. The volume comparison results are shown in Fig. 2(a). The inductor size is mainly determined by maximum flux density and loss. Different ripple energy and supply frequency applications will lead to different materials to achieve minimum volume. In terms of energy density, the film capacitor is more compact for low ripple energy, high-frequency applications. Otherwise, an aluminum capacitor would be better. For most of the application range, the inductive ripple energy storage method is bulkier and heavier than capacitive energy storage.

For the VSC, shown in Fig. 2(b), the system operates at 1kW with a $V\_dc^*=320V$, and 110V/50Hz and 220V/60Hz for the rectifier and inverter sides, respectively. For the CSC, shown in Fig. 2(c), the system also operates at 1kW with an $I\_dc^*=14A$, and 220V/60Hz and 110V/50Hz for the rectifier and inverter side, respectively. In Figs. 2(b) and 2(c), (top), are shown the V_dc^*/I_dc^* for the VSC/CSC using a bus capacitor of 40µF (VSC) and a bus inductor of 30mH (CSC). With the DC capacitor and inductor values used, a DC ripple of 3.77V (VSC) and 0.22A (CSC) were reached. To obtain the same ripple seen for the proposed system, it would be necessary a capacitor C_dc of 2,200µF (VSC) and a inductor L_dc of 1,400mH (CSC) in a conventional converter. Thus it was possible to achieve a reduction of 55× in the DC capacitor of the VSC and 46.67× in the DC inductor of the CSC. In Figs. 2(b) and 2(c), (bottom), are shown the waveforms of the signals in the AC side of the VSC and CSC, respectively. It is possible to observe that it was reached the unity power factor for the current $i\_(ac\_r)$ provided for the grid and a good waveform for the $v\_(ac\_i)$.
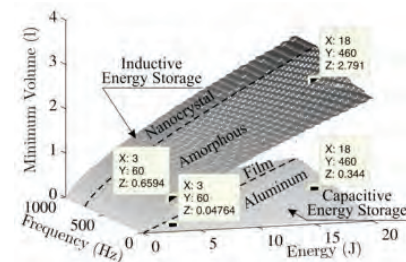
(a) Inductive and capacitive energy storage comparison results
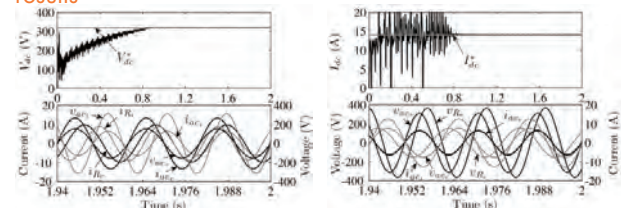
(b) Waveforms for the VSC   (c) Waveforms for the CSC

Fig. 2. Comparison and simulation results; (b) and (c) (top) are for the DC sides and (bottom) are for the AC sides

Digital Gain-Scheduled Control of a High-Frequency Parallel Resonant DC-DC Converter

This paper discusses the nonresonant-coupled parallel resonant converter and presents the design and simulation of a reference classical analog controller. Based on the strong relationship observed between low-frequency converter gain and the operating point, a band-limited gain-scheduled digital controller is proposed, designed, and simulated, showing an improvement of 5:1 with worst-case control bandwidth over the analog controller. A prototype is designed and built, and it experimentally validates the simulation results with good correlation.
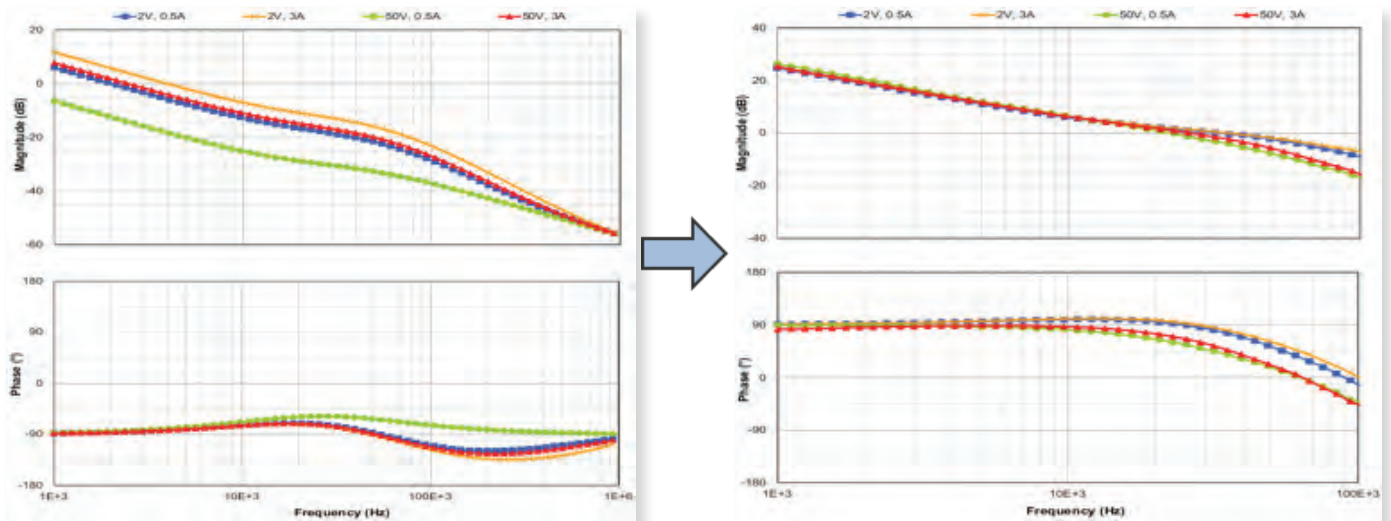
Fig. 1. Achieved improvement with gain-scheduled design
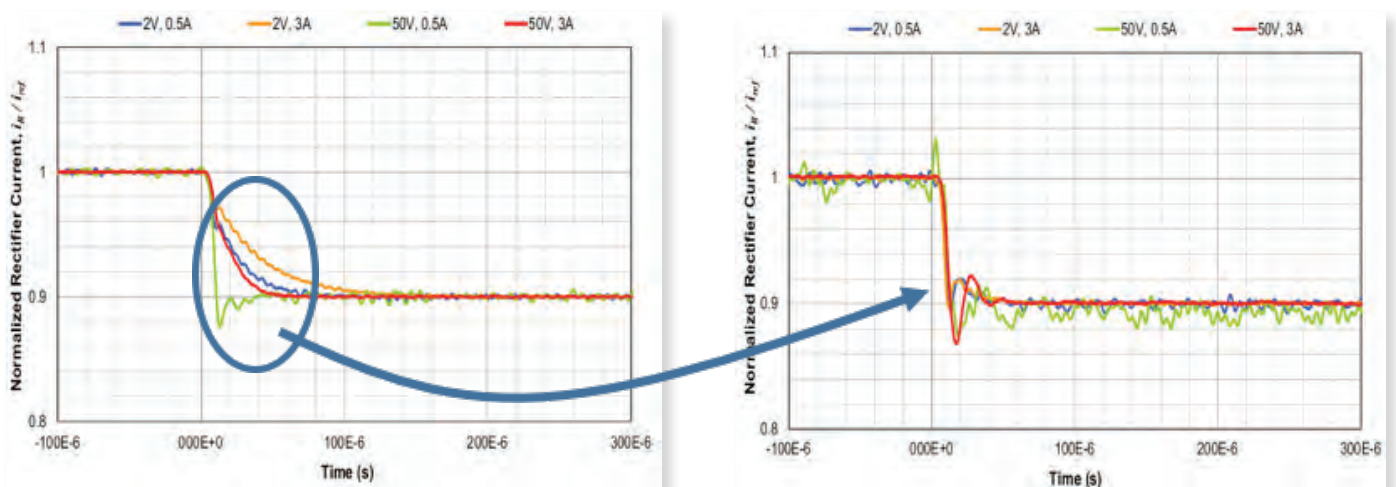
Fig. 2. Dynamic improvement with proposed gain-scheduled design

High-Power-Density, High-Efficiency DC/DC Converter

Efficiency and power density are two driving forces of front-end converters. For the front-end dc-dc converter, determining how to reduce the volume of the passive components and improve efficiency is very critical. Several methods for size reduction of these elements are shown below. To solve the hold-up time issue, this study proposes an LLC resonant converter to replace the PWM converter. An improved design method and an increase in switching frequency are utilized to increase the power density, while improved SR-driven methods are proposed to increase the efficiency. To challenge the limits of power density, magnetic and passive integration is employed, which results in a volume reduction of nearly 40%.

Fig. 1. Increasing efficiency and power density in a dc/dc converter
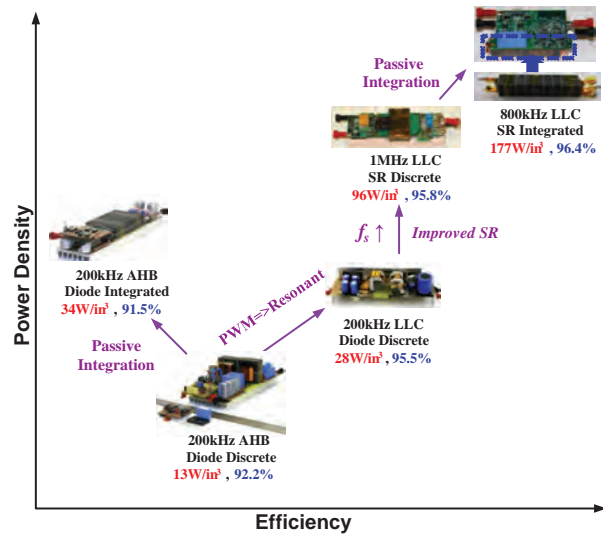
Novel Non-isolated LLC Resonant Converters

To shrink the size of passive components in the point-of-load buck converter, a high switching frequency is needed. However, the typical buck converter has large turn-on, driving, and turn-off losses at high switching frequencies. The typical benefits of LLC resonant converters are a lack of turn-on loss and little turn-off loss for the primary side switches and nearly ZCS (zero current switching) for the output rectifier, which are suitable for high-frequency DC/DC applications. However, the large turns ratio of the transformer is an issue due to the high ratio of input and output voltage.

The proposed non-isolated LLC converter can achieve ZVS, low turnoff loss and a self-driven synchronous rectifier. Due to the non-isolated technique, the turns ratio of the transformer is also reduced. The typical waveforms are shown in Fig. 1(c) below.

(a) t1-t2

(b) t2-t3
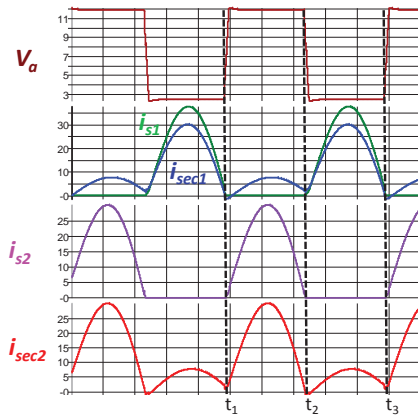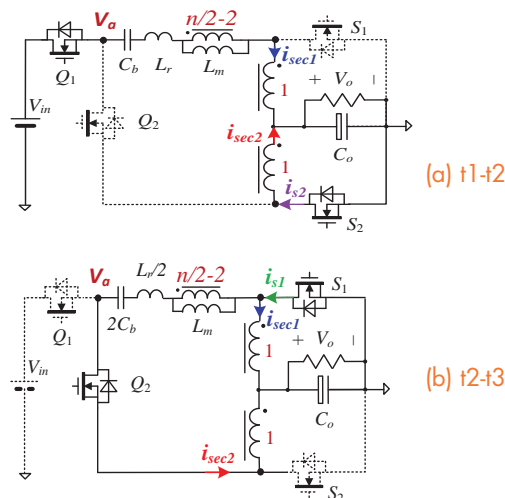
(c) Waveforms of non-isolated LLC converter

Fig.1 Novel non-isolated LLC resonant converter

A Novel Integrated Multi-Elements Resonant Converter

Multi-element resonant converters were proposed to solve startup and short-circuit protection problems LLC resonant converter meet. The notch filter is created to limit the inrush current during start up and short circuit, so that the power converter can be protected from destructive damage. However, more passive components are added to the resonant tank. The additional passive components impose the demand for integration efforts in order to alleviate their impact on converter size.

The magnetic and passive integration methods are given to improve the power density of passive components volume. Figure below shows the concept of magnetic integration. Firstly, the magnetizing inductance (Lm) can be controlled by air gap. The magnetic shunt between winding 1, 4 and windings 2, 3 represents the magnetic decoupling, which indicates the leakage inductance Lr. And, the magnetic shunt between winding 1 and winding 4 represents the leakage inductance Lp.
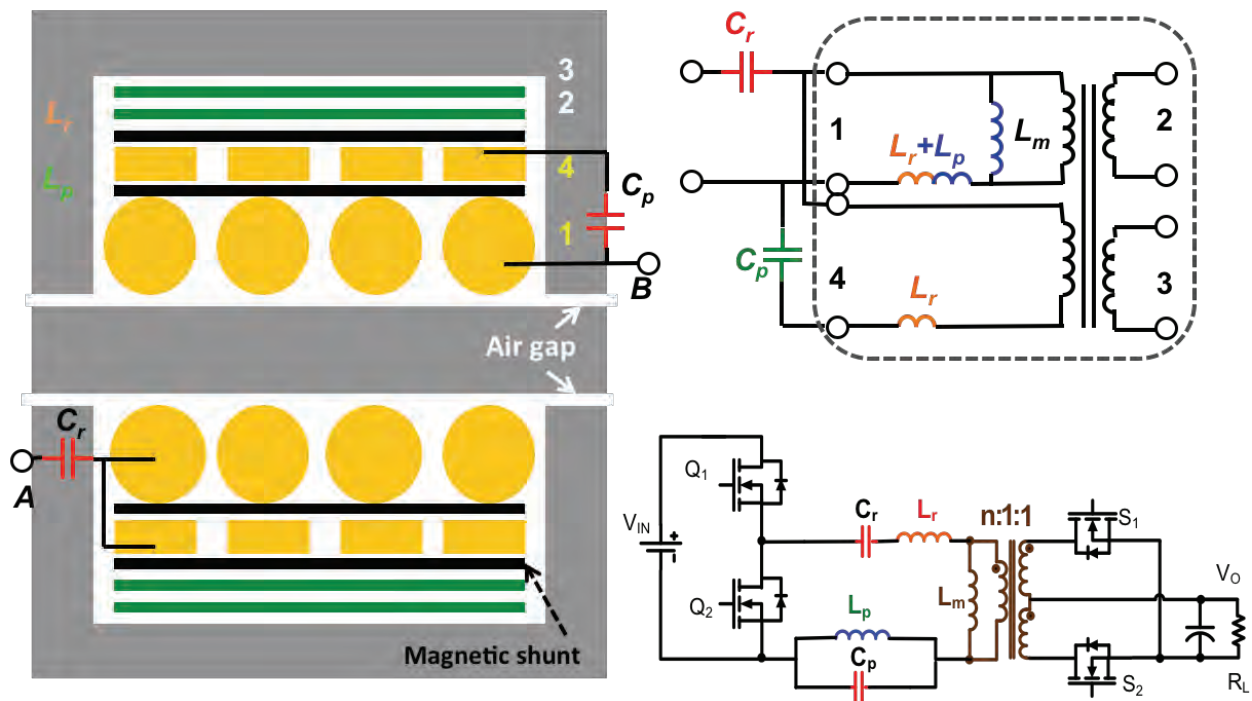
A Novel Hybrid Packaging Structure for High-Temperature SiC Power Modules

This work presents a novel hybrid packaging structure for high-temperature SiC power modules that combines the benefits of the wirebond packaging structure and the planar packaging structure. With the proposed hybrid structure, the power modules can achieve the same footprint as and similar parasitics than planar structures, but with a much easier fabrication process and more reliable top-side interconnections. The new structure and its fabrication process are presented, and a prototype module is built based on an SiC JFET.

Detailed comparisons are also conducted between the hybrid, planar, and wirebond structures, and the results reveal the better performances of the hybrid structure due to its smaller parasitics, lower switching loss and more flexible routing than the wirebond structure, as well as easier fabrication, more reliable top-side connection and more flexible die-attachment material selection than the planar structure. A three-phase multiple-chip SiC JFET hybrid structure power module is built and tested with a 250ºC junction temperature for verification.
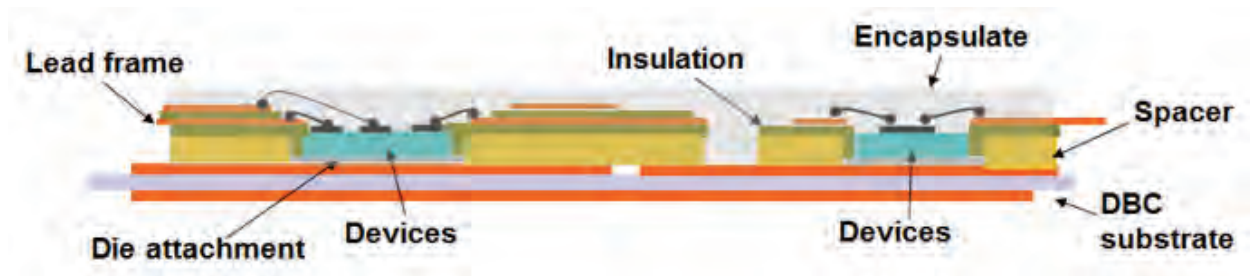
Fig. 1. Proposed packaging structure
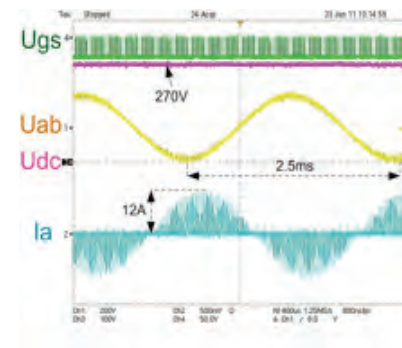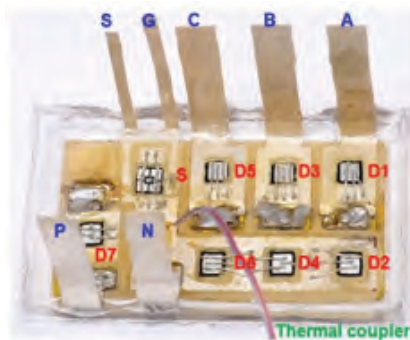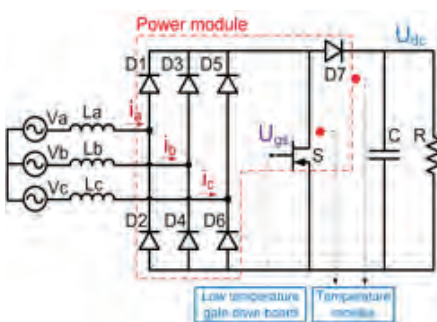
Fig. 2. Hybrid structure, three-phase power module and electrical test results

Fig. 3. Thermal test results (junction temperature around 225°C and case temperature 200 °C)
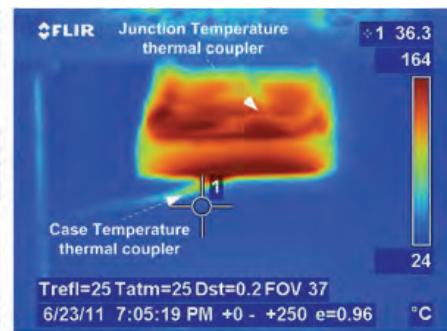
Power Electronics Package Thermomechanical Reliability Investigation for Large Temperature Excursion

This study confirms that high stresses between the metallization layer and ceramic in power electronics packaging lead to significant failures in the DBC substrate. This paper discusses the driving forces behind several different failure modes , and presents the results of a parametric study of an improved DBC substrate. Three different DBS substrates are compared, as shown in Fig. 1.

As seen in Fig. 2, the peak tensile peeling stress was verified by simulations and experiments as the major driving force of delamination. It is therefore the basis for improving the design and optimizing the process parameters so that power modules can have a high resistance to large temperature excursions.
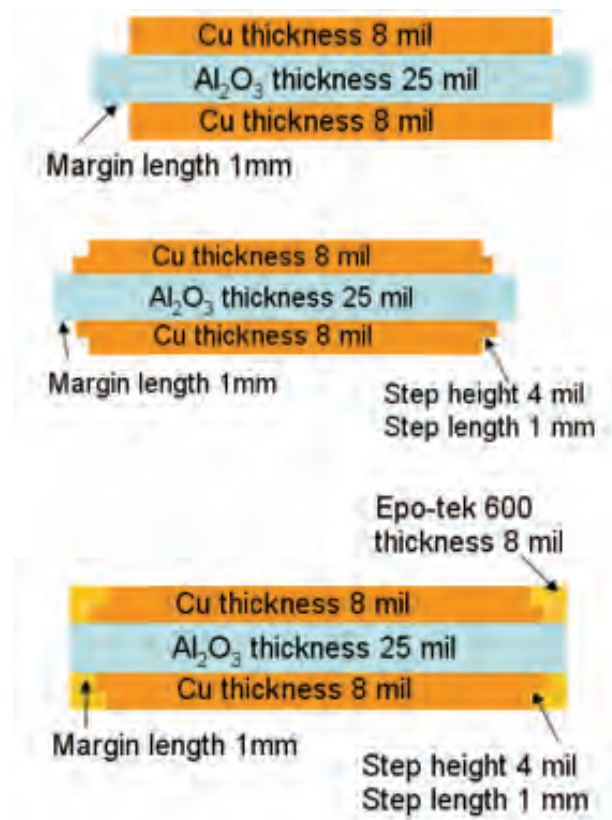
Fig. 1. Conceptual drawing of cross-sectioned DBC samples, showing dimensions
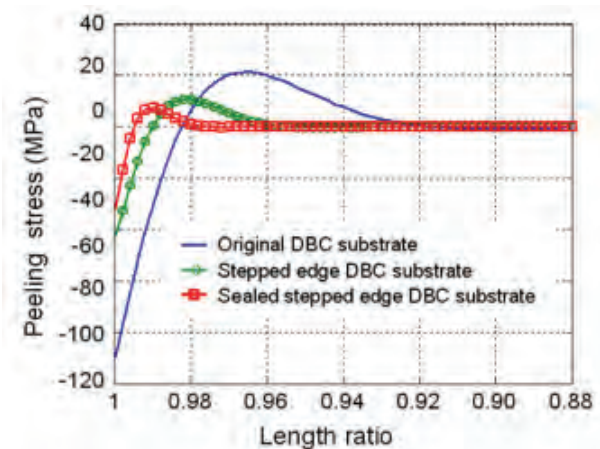
Fig. 2. Comparison of peeling stress along the midline

Characterization and Design of Three-Phase EMI Noise Separators for Three-Phase Power Electronics Systems

EMI filter design usually begins with noise measurement. Finding the best methods to accurately measure the noise voltage spectrum and to separate differential-mode and common-mode noise has become a fundamental challenge for EMI filter design. Previous work on noise separation work well for single-phase DC systems, but the same tool is needed for three-phase systems, as shown in Fig. 1.

In this paper, three-phase noise is first analyzed using a symmetrical component theory. Three-phase noise separators are modeled and characterized using symmetrical component theory and S-parameters. The critical formulas used to evaluate a three-phase noise separator are derived, and a function scheme and circuit structure for three-phase noise separators are proposed based on the theory developed, as shown in Fig. 2 and Fig. 3. The techniques for designing a high-performance, three-phase noise separator are explored, and a three-phase noise separator prototype is built, measured, and evaluated using the theory developed in this paper. The prototype is successfully used to measure electromagnetic interference in a practical three-phase power electronics system.
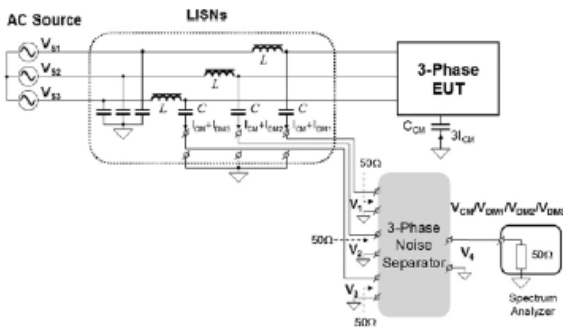
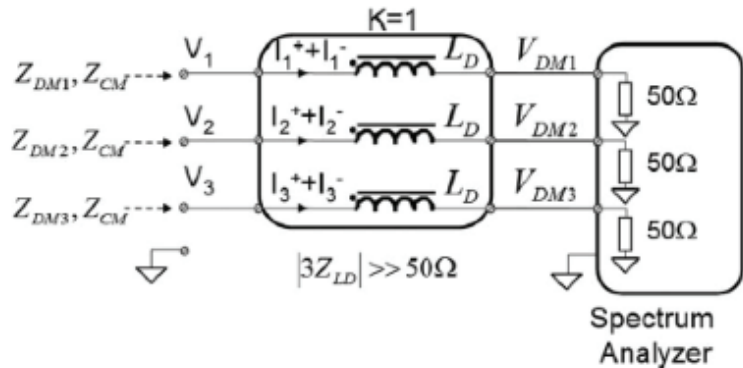Fig. 1 Three-phase system noise measurement
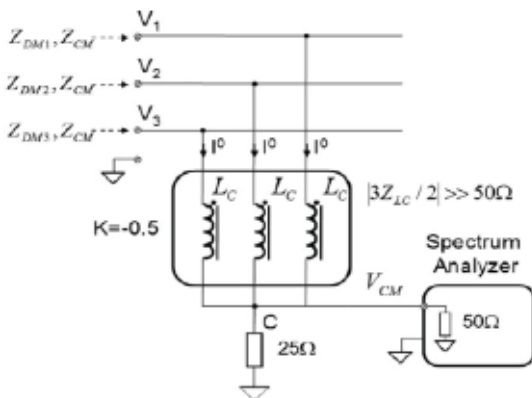

Fig. 2. DM noise separator circuit

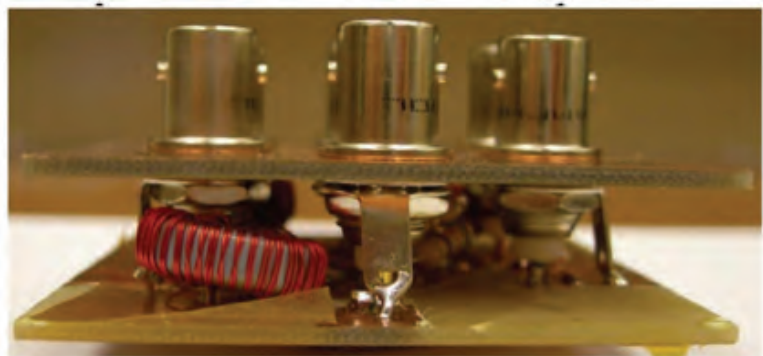Fig. 3. CM noise separator circuit

Fig. 4. Prototype of a three-phase noise separator

Phase-Locked Loop Noise Reduction via Phase Detector Implementation for Single-Phase Systems

A crucial component of grid-connected converters is the phase-locked loop (PLL) control subsystem that tracks the grid voltage's frequency and phase angle, as shown in Fig. 1. Therefore, accurate, fast-responding PLLs are required to provide these measurements for control and protection purposes. Illustrated in Fig. 2, this paper proposes a novel feedback mechanism for single-phase PLL phase detectors (PDs) using the estimated phase angle. Ripple noise in the estimated frequency, most commonly a 2 nd harmonic under phase-lock conditions, is reduced or eliminated without the use of low-pass filters (LPFs), which can cause delays

to occur and limit the overall performance of the PLL response to dynamic changes in the system.

The proposed method has the capability to eliminate the noise ripple entirely, and under extreme line distortion conditions can reduce the ripple by at least half. Other modifications implemented through frequency feedback are shown to reduce the settling time of the PLL up to 50%. The noise reduction can be easily seen in Figs. 3 and 4, which show the transient response of the proposed PLL system and the typical mixer-type PLL system. Mathematical analyses with simulated and experimental results are provided to confirm the validity of the proposed methods.
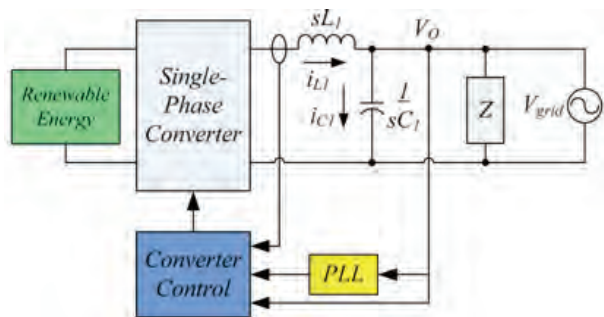

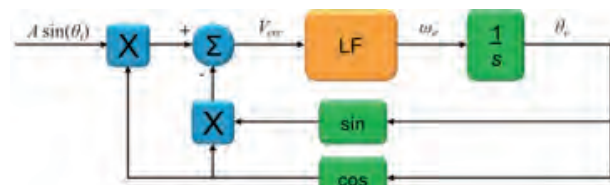Fig. 1. Renewable energy system diagram

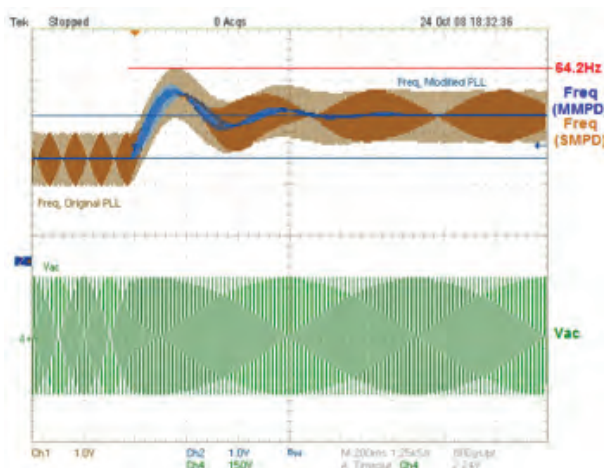Fig. 2. Proposed PLL system for single-phase application

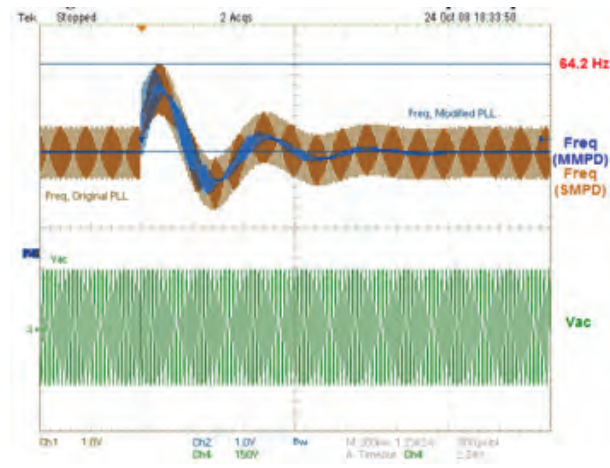Fig. 3. Frequency step response of proposed PLL (blue) and typical PLL (brown)

Fig. 4. Phase step response of proposed PLL (blue) and typical PLL (brown)

Simplified Optimal Trajectory Control (SOTC) for LLC Resonant Converters

This paper proposes a simplified optimal trajectory control (SOTC) for LLC resonant converters. During the steady state, a linear compensator like PI or PID is used, controlling the switching frequency (fs) to eliminate error. However, during load transients, the simplified optimal trajectory control (SOTC) method takes over, controlling the pulse widths of the driving signals. Using state-plane analysis, the pulse widths are estimated, letting the state variables track the optimum trajectory locus in the minimum period of time.
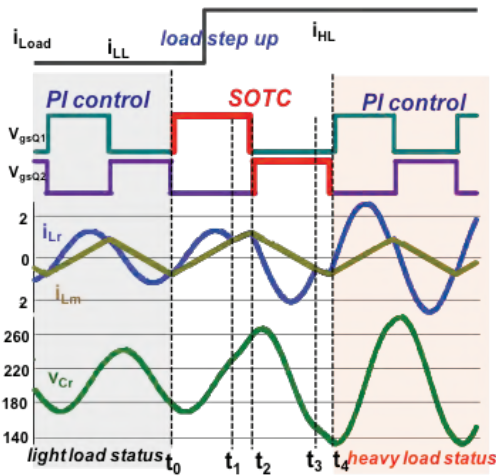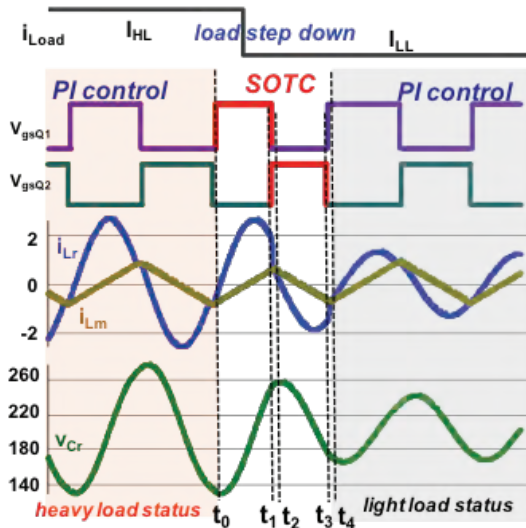

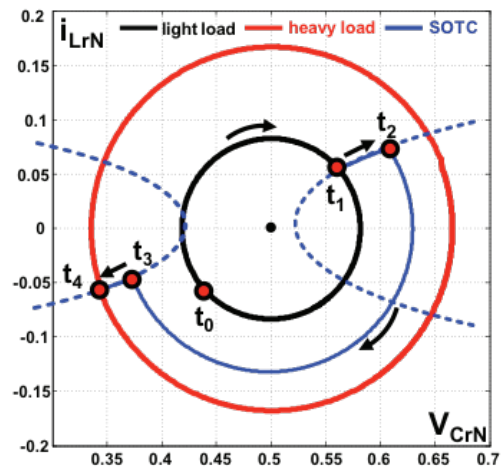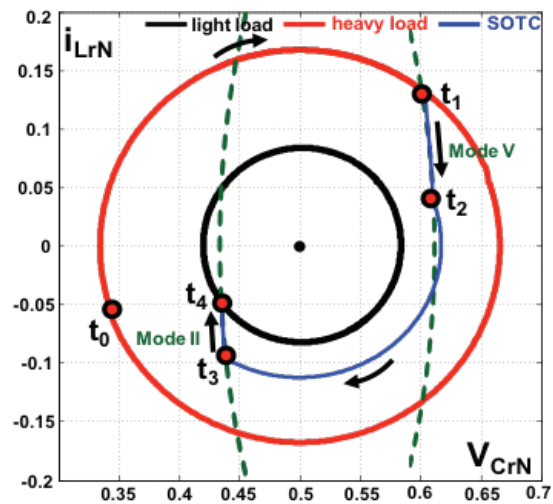Fig. 1. SOTC during load step-up

Fig. 2. SOTC during load step-down

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