Center for Embedded Systems for Critical Applications

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CESCA Newsletter
Center for Embedded Systems for Critical Applications

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In this edition:

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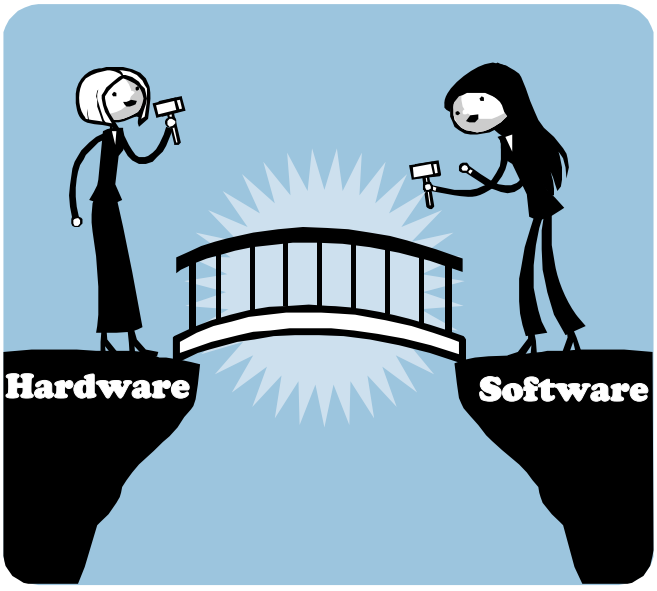
Several New Projects Awarded to CESCA!

Within a short few months since our inaugural newsletter, several research grants have been awarded to CESCA members. The hard work of all CESCA members has laid the foundation for these new projects. Many of the projects are interdisciplinary in nature, combining expertise of various faculty members and talents of research students. These range from merging FPGAs with network simulation to sub-threshold circuits and physically unclonable functions. These exciting, new endeavors not only push the research envelope, but also serve as tremendous educational opportunities to students involved.

This issue of the newsletter describes the new projects, as well as many other activities engaged by CESCA members. These include not only conference travel, but the summer often provides great opportunities for internships. We had more than a dozen students taking on summer internships this year! We also celebrate those students who have reached a milestone in their academic career and successfully defended their dissertations and/or theses. They continue to serve as ambassadors for CESCA, applying the knowledge acquired during their years here.

New Research Projects

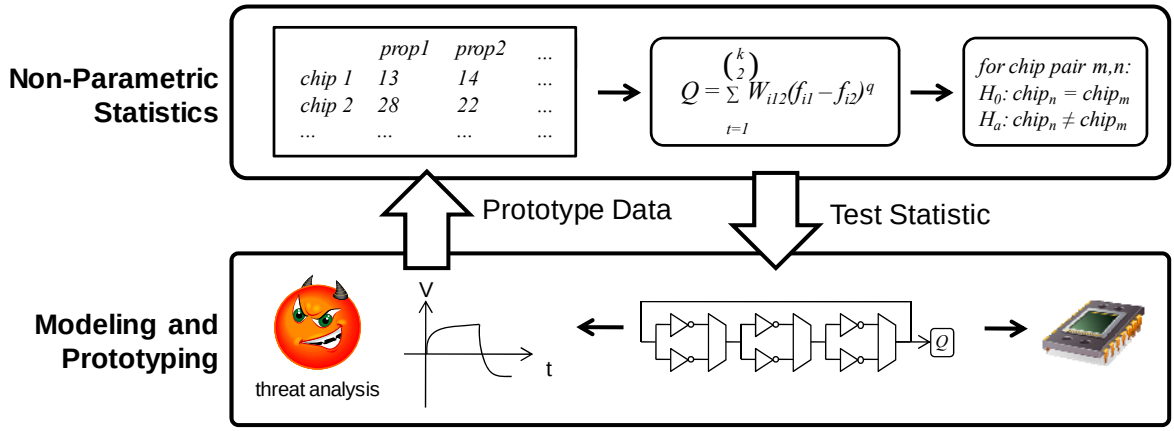
Cross-domain Design Tools for Sensor Network and Architecture



August 2009 Yaling Yang and Patrick Schaumont have received a three-year $424k NSF grant for research in "Cross-domain Design Tools for Sensor Network and Architecture ".The team will develop a novel tool, named Sunshine, to effectively support joint evaluation and design of sensor network hardware and software. The hardware and software communities of sensor network will use Sunshine to efficiently exchange mutual requirements and share the latest technology advances in each other's fields. Novel hardware architecture and platforms will be created and tested through Sunshine's cross-domain design environment. Sunshine also offers the opportunity for innovative cross-domain education.

This chip is your chip, this chip is my chip

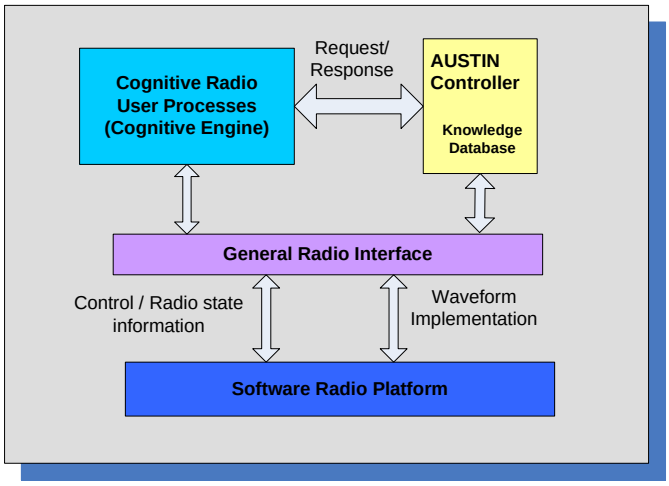
Patrick Schaumont, Leyla Nazhandali, and Inyoung Kim (Statistics Department) have received an ICTAS grant for research in "Unique and Unclonable Chip Identifiers". The team will define novel mechanisms to establish, in a secure and unique way, the identity of electronic chips. Chip-identity technology is useful for a rich and broad set of applications in pervasive security, for example in anti-piracy of software and anti-counterfeiting of products. The team will combine complementary expertise in advanced statistics, digital architectures, and advanced circuit design. The $98K grant is sponsored by the Institute for Critical Technology and Applied Science (ICTAS) at Virginia Tech, and provides seed funding for one year.



The first results of this research were published earlier this year at the International Conference on Field Programmable Logic and Applications, and at the IEEE International Workshop on Hardware Oriented Trust and Security.

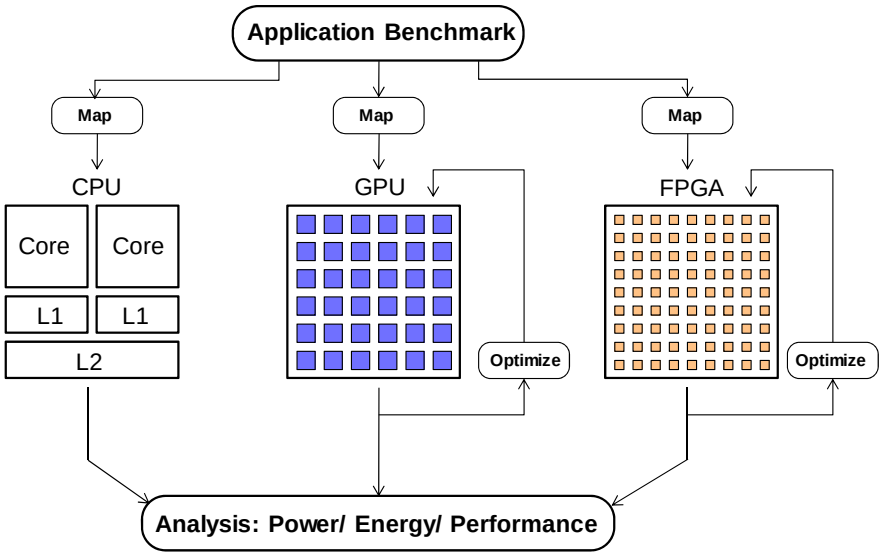
An Initiative To Assure Software Radios Have Trusted Interactions

Jeff Reed (PI) and three other VT professors, **Jung-Min Park**, Tom Hou, and Cameron Patterson, have been awarded with an NS project whose funding amount is $1M (VT's share is $400K) for two years. Software and cognitive radios will greatly improve the capabilities of wireless devices to adapt their protocols and improve communication. Unfortunately, the benefits that such technology will bring are coupled with the ability to easily reprogram the protocol stack. Thus it is possible to bypass protections that have generally been locked within firmware. If security mechanisms are not developed to prevent the abuse of software radios, adversaries may exploit these programmable radios at the expense of the greater good. Regulating software radios requires a holistic approach, as addressing threats separately will be ineffective against adversaries that can acquire, and reprogram these devices. The AUSTIN project involves a multidisciplinary team from the Wireless Information Network Laboratory (WINLAB) at Rutgers University, the Wireless@Virginia Tech University group, and the University of Massachusetts. AUSTIN will identify the threats facing software radios, and will address these threats across the various interacting elements related to cognitive radio networks. Specifically,



AUSTIN will examine: (1) the theoretical underpinnings related to distributed system regulation for software radios; (2) the development of an architecture that includes trusted components and a security management plane for enhanced regulation; (3) onboard defense mechanisms that involve hardware and software-based security; and (4) algorithms that conduct policy regulation, anomaly detection/punishment, and secure accounting of resources. Developing solutions that ensure the trustworthy operation of software radios is critical to supporting the next generation of wireless technology. AUSTIN will provide a holistic system view that will result in a deeper understanding of security for highly-programmable wireless devices.

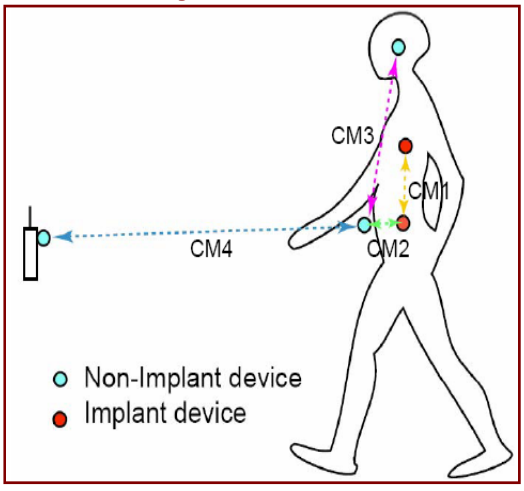
Bridging the Great Parallel Divide: Research and Education for Next-Generation Computing Platforms



Due to increasing power densities, the evolution of traditional computer architectures has become unsustainable. Computer architectures are facing one of the biggest challenges in many years: the transition of commodity single-processor architectures and sequential programming paradigms to heterogeneous, multi-processor architectures and parallel programming paradigms. This transition is complex and non-trivial, and it requires a close cooperation between the best minds in Computer Science (CS) and Computer Engineering (CPE). A research team, including Patrick Schaumont, Sandeep Shukla, Peter Athanas, from the ECE Department, and Wu Feng, Yong Cao, from the CS Department, received support from the College of Engineering to acquire a high-end parallel computer to drive research into this problem. The equipment, a server-based FPGA-accelerator and a GPGPU graphics processor, will be used for computer benchmarking, hardware-software codesign, electronic design automation, reconfigurable computing, and scientific simulation and visualization.

Ha collaborates with a Korean team in wireless body area network (WBAN) research

July 2009. A WBAN is characterized as short range, low power, and highly reliable wireless communications for use in close proximity to, or inside, a human body. Those applications require extremely low power wireless nodes so as to last for years without battery recharges or replacements. Dong Ha collaborates with Electronics and Telecommunications Research Institute (ETRI), Korea, in WBAN research, and his team investigates low power RF architectures for WBANs. The five-year project is sponsored by Korean government, and the amount of funding for Dong Ha's team is $80K for year 2009.



Faculty Honors

Jung-Min "Jerry" Park has been tenured and promoted to the rank of Associate Professor. His research interests are in network security, applied cryptography, and cognitive radio/software defined radio networks. Jung-Min "Jerry" Park has published his work in leading journals and conference proceedings. He is leading or participating in several sponsored research projects. Current sponsors include the NSF (National Science Foundation), SANS Institute (SysAdmin, Audit, Network Security), Samsung Electronics, and SCA Technica, Inc.

Sandeep Shukla travelled to Berlin, attended the Humboldt Foundation's annual conference, and attended a reception thrown by the German President Dr. Horst Köhler at his Schloss Belvue residence in Berlin. He was then honored at a separate ceremony for his winning the Bessel Award (a lifetime achievement award for extraordinary achievements within 12 years of one's PhD in any scientific field).

Sandeep Shukla also started as an associate editor for the new IEEE publication IEEE embedded systems letters whose first issue came out in September 2009.
Sandeep Shukla was also invited by the Computer Community Consortium (CCC) to serve on a panel for deciding the strategies for industry-government-academic collaboration for building a policy of research in the area of cyber physical systems.

Celebrating Graduates (Apr – Aug 2009)

- Nannan He (Advisor: Michael Hsiao), "Exploring Abstraction Techniques for Scalable Bit-precise Verification of Embedded Software," Ph.D, May, 2009. Her dissertation aimed to significantly extend the scalability of formal verification of embedded software. Several powerful abstraction and variable bit-width reduction techniques were proposed and developed, including those techniques borrowed from the hardware verification domain. Several orders of magnitude improvement in verification time have been achieved. She has joined as a post-doc at Oxford University, UK.
- Christian Tergino (Advisor: Patrick Shaumont), "Efficient Binary Field Multiplication on a VLIW DSP," M.S., May, 2009. Christian Tergino's research was in efficient mapping of cryptographic operations on an advanced DSP processor. His results, demonstrated using a TI OMAP processor, show that Binary-field Modular Multiplications can executed 6 times faster on a TI C64X DSP compared to a traditional ARM Cortex A8. He has joined Northrop Grumman in Virginia.
- Harini Jagadeesan (Advisor: Michael Hsiao), "Design and Verification of Privacy and User Re-authentication Systems," M.S., May, 2009. Harini's research focused on how to re-authenticate a user based on his/her keyboard and mouse profiles, a continual and low-cost extraction of user's behavioral profile. The accuracy of the system is 96% for application based user re-authentication. She has joined Microsoft in Redmond, WA.

Internships (Apr – Aug 2009)

Numerous CESCA students at Summer Internships in 2009, applying their knowledge to real world problems, ranging from hardware and software design, development, test, verification, and security analysis.

Sumit Ahuja	Cebatech Inc.
Karthik Channakeshava	Bell Labs
Zhimin Chen	Microsoft Research
Percy Dadabhoy	Qualcomm
Amol A. Deshpande	Viasat Inc.
Neha Goel	Intel
Eric Xu Guo	ISI East
Jihoon Jeong	Intel
Swati Kanaujia	Qualcomm Inc.
Saparya Krishnamoorthy	Intel
Avinash Lakshminarayana	Qualcomm
Abhranil Maiti	ISI East
Mahesh Nanjundappa	Intel Corporation
Sandesh Prabhakar	Qualcomm
Jatin Thakkar	Phoenix Integration

Patents and Publications (Apr – Aug 2009)

Patents:

August 2009. Dong Ha, along with four colleagues with Center for Power Electronics Systems (CPES), has been awarded a US patent (No. 7,570,037) entitled “Hybrid Control Methods for Digital Pulse Width Modulator (DPWM),” They devised a scheme to increase the resolution of the duty cycle for digital DC/DC buck converters.

Tutorial & Workshop:

Sandeep K. Shukla organized and presented a one day tutorial on Embedded Software Synthesis from Formal Specifications at the Design Automation and Test Conference (DATE 2009) in April 2009, at Nice, France. The other speakers at the tutorial included CESCA Alumni Prof. Hiren D. Patel who just finished his 2 year post doctoral work at the University of California at Berkeley, and joined as an assistant professor in the electrical and computer engineering department of University of Waterloo in Canada.
Sandeep Shukla also served as the program co-chair for the 4th International Workshop on Formal Methods in Globally Asynchronous and Locally Synchronous Design in April 2009 at Nice, France.

Book Chapters published during this period:

S. Ahuja, G. Singh, D. Bhaduri and S. Shukla, Fault and Defect-Tolerant Architectures for Nanocomputing, Chapter 10, Bio-inspired and Nanoscale Integrated computing (Ed. Mary Eshaghian-Wilner), Nature Inspired Computing Series, pp. 263-294, John Wiley & Sons, June 2009.

Conference and Journal Papers during this period are:

V. Vivekraja and L. Nazhandali, Circuit-level techniques for reliable physically uncloneable functions, *IEEE Hardware Oriented Trust and Security*, July 2009.

A. Maiti and P. Schaumont, Analysis and improvement of ring oscillator based physical unclonale function, *2009 International Symposium for Field Programmable Logic and Applications*

Z. Chen and P. Schaumont, Early feedback on side-channel risks with accelerated toggle-counting, *IEEE HOST (Hardware Oriented Security and Trust),* July 2009.

M. Banga and M. S. Hsiao, VITAMIN: Voltage inversion technique to ascertain malicious insertions in ICs*, IEEE HOST (Hardware Oriented Security and Trust),* July 2009.

K. Bian, J.-M. Park, M. S. Hsiao, F. Belanger, and J. Hiller, Evaluation of online resources in assisting phishing detection*, IEEE/IPSJ International Symp. on Applications and the Internet (SAINT 2009)*, Seattle, USA, July 2009.

N. He and M. S. Hsiao, An efficient path-oriented bit-vector encoding width computation algorithm for bit-precise verification*, IEEE Design Automation and Test in Europe Conference*, April 2009.

B. A. Jose, B. Xue, and S. K. Shukla, An analysis of the composition of synchronous systems, *4th Intl. Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS'09),* Electronic Notes in Theoretical Computer Science 245, pp. 69–84, Nice, France, April 2009.

B. Xue, S. K. Shukla, Modeling and Analyzing the Implementation of Latency-Insensitive Protocols Using the Polychrony Framework , *4th Intl. Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS'09),* Electronic Notes in Theoretical Computer Science 245, *Pages 3-22,* Nice, France, April 2009.

Y. Ma; Talpin, J.-P.; Shukla, S.K.; Gautier, T., "Distributed Simulation of AADL Specifications in a Polychronous Model of Computation," *Embedded Software and Systems, 2009. ICESS '09. International Conference on*, vol., no., pp.607-614, 25-27 May 2009.

A. B. MacKenzie, J. H. Reed, P. Athanas, C. W. Bostian, R. M. Buehrer, L. A. DaSilva, S. Ellingson, Y. T. Hou, M. Hsiao, J. Park, C. Patterson, S. Raman, and C. da Silva, Cognitive Radio and Networking Research at Virginia Tech, *Proceedings of the IEEE*, Vol. 97, No. 4, Apr. 2009, pp. 660 688.

K. Bian and J. Park, A Coexistence-Aware Spectrum Sharing Protocol for 802.22 WRANs, *International Conference on Computer Communications and Networks (ICCCN 09)*, San Francisco,USA,Aug.2009.

S. Xiao, J. Park, and Y. Ye, Tamper Resistance for Software Defined Radio Software, *IEEE Computer Software and Applications Conference (COMPSAC)*, July 2009.

Sangiovanni-Vincentelli, A.; Guang Yang; Shukla, S.K.; Mathaikutty, D.A.; Sztipanovits, J., "Metamodeling: An Emerging Representation Paradigm for System-Level Design," *Design & Test of Computers, IEEE* , vol.26, no.3, pp.54-69, May-June 2009

S. Ahuja, S. T. Gurumani, C. Spackman, S. K. Shukla, "Hardware Coprocessor Synthesis from an ANSI C Specification," *IEEE Design and Test of Computers*, vol. 26, no. 4, pp. 58-67, July/Aug. 2009.

J-S. Lee, and D.S. Ha, FleXilicon Architecture and Its VLSI Implementation**,** *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 8, pp. 1021-1033, August 2009.

Books Published During this period:

Fundamental Problems in Computing - Essays in Honor of Professor Daniel J. Rosenkrantz
Editors: Ravi, S.S.; Shukla, Sandeep K.
(Springer Netherlands) 2009

Metamodeling-Driven IP Reuse for SoC Integration and Microprocessor Design
Authors: Mathaikutty, Deepak A.; Shukla, Sandeep
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