Center for Embedded Systems for Critical Applications

VirginiaTech
Invent the Future

CESCA Newsletter
Center for Embedded Systems for Critical Applications

CESCA • 302 Whittemore Hall • Dep't. of ECE • Virginia Tech • Blacksburg • 24061 • USA

Jan. 2010 • Vol.3 • No.1

In this edition:

CESCA Offices & Labs
3rd Floor, Durham Hall
Virginia Tech

New Projects and Awards to CESCA!

New projects ranging from new evolutionary design of routing algorithms, to secure embedded systems, to fingerprint sufficiency assessment, in addition to several other new projects, have been awarded during the fall semester of 2009. Many of these projects are highly interdisciplinary, which taps into the synergy and expertise of CESCA faculty and student members.

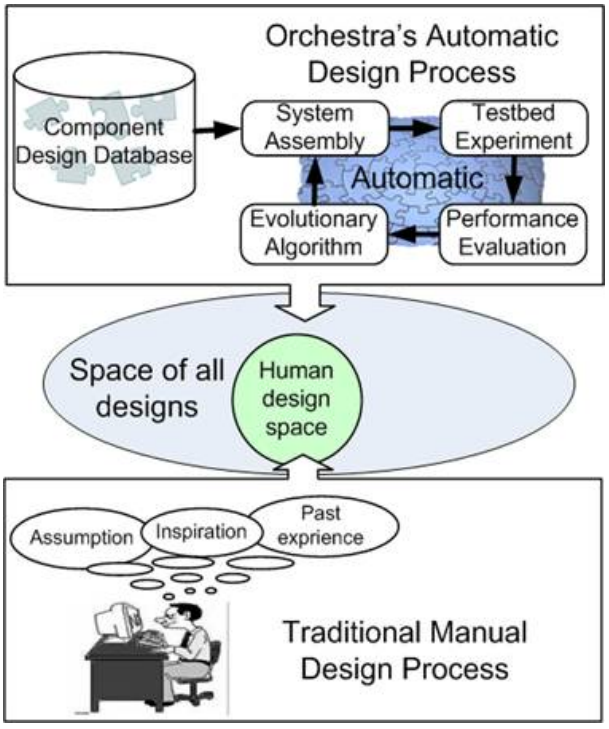
The research endeavors are periodically disseminated in scholarly journals and conference proceedings. Among the many papers published during fall 2009, a best paper award on energy harvesting deserves celebration. The high quality papers published by CESCA researchers continue to build strength into the research group.

This issue of the CESCA newsletter will feature the new projects awarded, as well as describing a few other activities. We also celebrate those students who graduated in fall 2009.

New Research Projects

Evolutionary Routing Protocol Design and Validation

Dr. Yaling Yang, Michael Hsiao and Luiz DaSilva were recently awarded with a $150k NSF project on developing an automatic routing protocol design engine named "Orchestra". Unlike traditional routing systems that are manually designed by network engineers, Orchestra, on the other hand, can automatically and intelligently assemble, test and verify a great variety of routing designs. Orchestra is the first architecture that introduces evolutionary design into the routing area. It accepts various designs of routing components as "genes" and automatically assembles them into a verified and workable routing protocols. Based on the performance of the assembled protocols, Orchestra switches and tunes designs of routing components to eventually identify the best design for various network settings.



The automatic design process of Orchestra will greatly ease a network engineer's burden of implementing and evaluating an entire routing system. The automatic integration of various component designs from different developers by Orchestra can efficiently explore a much larger design space for routing systems than any single network engineer can. Hence, new areas for routing designs that are not explored by humans can be automatically discovered by Orchestra. The large

collection of component designs in Orchestra also provides a common platform for comparing and evaluating different design choices. By varying Orchestra's testbed and simulation settings, different routing system designs can be evaluated under different environments.

Standard Performance Evaluation of Cryptographic Hardware and Software

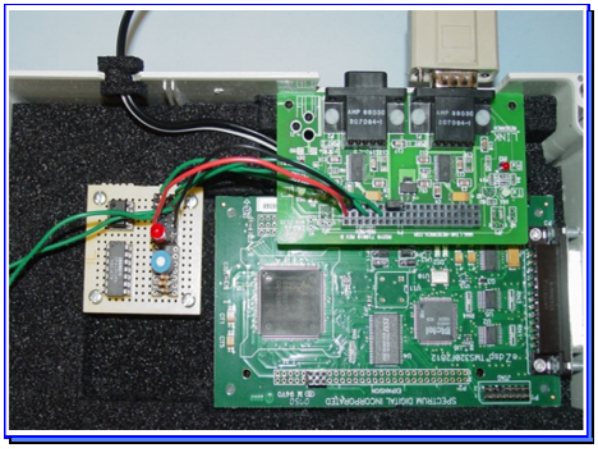
Patrick Schaumont and Leyla Nazhandali have received a three-year $544K grant through NIST's Measurement Science and Engineering Research Grants Program. In collaboration with George Mason University (lead institution) and University of Illinois at Chicago, the team will develop a performance evaluation infrastructure for cryptographic hardware and software. The infrastructure will allow to evaluate and compare the performance of competing crypto-algorithms when implemented in ASICs, FPGAs, as well as microprocessors. The CESCA team will specifically focus on performance evaluation on ASIC. A first milestone for the environment will be its application to submissions in NIST's SHA-3 contest for new hash functions. The SHA-3 standard will be a basis for future secure digital signature schemes. The environment will be available to the entire cryptographic community, allowing researchers to fairly, comprehensively, and automatically compare their new cryptographic algorithms, hardware architectures, and optimization methods against previous work.

Sufficiency Assessment for Latent Fingerprint Images

Lynn Abbott and Michael Hsiao have received funding for a 2-year project related to quality assessment of latent fingerprint images. They are co-PIs along with Ed Fox (Computer Science), Randy Murch (Center for Technology, Security and Policy), and Bruce Budowle (University of North Texas), with a total project amount is $855k. Fingerprint matching depends fundamentally on the quality of the available friction ridge patterns. The assessment of print quality is subjective, however, and inconsistent decisions can occur as a result. This project will focus on an effort to develop a quantitative approach for characterizing friction ridge pattern detail. All levels of the common hierarchical description are of interest, namely Level 1 (high-level patterns), Level 2 (minutia points), and Level 3 (pores and ridge contours). The standard will incorporate measures that are based on the principles of image representation, signal detection, deterioration modeling, and statistical pattern recognition. The long-term goal is to establish standards that can ensure quality and uniformity of practice.

Ha teamed up with companies receive three SBIR projects.

Dong Ha, teamed up companies and other researchers, was awarded three SBIR (Small Business Innovative Research) Phase I projects. The first project sponsored by NASA is to develop a low-power structural health monitoring system, which is capable of detecting and locating damage. The second project, also sponsored by NASA, is to develop a CMOS ultra-wideband impulse radar, which can perform accurate ranging and high bandwidth communications. The third project sponsored by Army is to investigate a wireless sensor system capable of operating at high temperature and powered by energy harvested from multiple sources such as air flow, thermal, and vibrations.



Other New Projects and Funding:

- Patrick Schaumont received an NSF project (amount: $118,830) entitled “Infrastructure to Collect and Analyze Circuit Variability in FPGAs”. This project will collect variability data on FPGAs and use it to construct a publicly accessible database.
- Patrick Schaumont in collaboration with CS and other ECE faculty members received a SCHEV equipment grant ($50K) from COE to purchase a high-end parallel computer.
- Dong Ha and Patrick Schaumont received a SCHEV equipment grant ($20K) from COE to purchase a high-end digital oscilloscope and near-field probe set for E-field and H-field with a pre-amplifier.

Best Paper Award

“Self-charging structures” wins *the* best paper prize at SMASIS 2009

Three CIMSS (Center for Intelligent Material Systems and Structures) members (Daniel Inman and his students Anton, and Erturk) and two CESCA members (Dong Ha and his student Na Kong) developed a self-charging structure, which won the best paper award at the ASME Conference on Smart Materials, Adaptive Structures and Intelligent Systems (SMASIS) in September 2009. The structure provides multifunctionality capabilities in a single device that can harvest vibration energy, stored harvested energy, and bear the load. The ‘self-charging structures’ are multilayered, composite devices consisting of active piezoceramic layers for scavenging energy, flexible thin-film battery layers for storing scavenged energy, and a central metallic substrate layer. A key advantage of the self-charging structure design is that, unlike traditional vibration energy harvesting devices that are designed as add-on components to a host system, self-charging structures can be integrated into a system to provide load bearing capacity and eliminate the mass loading effects found in conventional designs.

Celebrating Graduates (Sept - Dec 2009)

- Sandesh Prabhakar (Advisor: Michael Hsiao), "Algorithms and Low Cost Architectures for Trace Buffer-Based Silicon Debug," M.S., December, 2009. Joined Qualcomm.

- Vipul Chawla (Advisor: Dong Ha), “Power Line Communications – System Level Study and Circuit Design,” M.S., Sept. 2009

- Yexin Zheng (Advisor: Chao Huang), "Circuit Design Methods with Emerging Nanotechnologies," Ph.D., December, 2009.

Publications (Sept - Dec 2009)

Book Chapters:

- J. Park, K. Bian, and R. Chen, “Cognitive Radio Network Security,” in Cognitive Radio Communications and Networks: Principles and Practice, A. Wyglinski, M. Nekovee, and T. Hou (Eds.), Elsevier, Dec. 2009.

Journal and Conferences:

- H. Jagadeesan and M. S. Hsiao, "A novel approach to design of user re-authentication systems," *IEEE Conference on Biometrics: Theory, Applications and Systems*, September 2009.
- M. Chandrasekar and M. S. Hsiao, "Search state compatibility and learning for state space exploration," *TECHCON*, September 2009.
- S.R. Anton, A. Erturk, N. Kong, D.S. Ha, and D.J. Inman, “Self-charging structures using piezoceramics and thin-film batteries,” *ASME Conference on Smart Materials, Adaptive Structures and Intelligent Systems*, SMASIS2009-1368, (12 pages), September 2009.
- D. Zhou, J.K. Kim, J.-L.K. Bilé, A.B. Shebi, D.S. Ha, and D.J. Inman, “Ultra low-power autonomous wireless structural health monitoring node,” *International Workshop on Structural Health Monitoring*, pp. 797-804, September 2009.
- S. Park, S.R. Anton, D.J. Inman, J.K. Kim, and, D.S. Ha, “Instantaneous baseline damage detection using a low power guided waves system,” *International Workshop on Structural Health Monitoring*, pp. 505-512, September 2009.
- X. Guo, J. Fan, P. Schaumont, I. Verbauwhede, "Programmable and parallel ECC coprocessor architecture: tradeoffs between area, speed and security," *IACR Workshop on Cryptographic Hardware and Embedded Systems (CHES 2009)*, September 2009.
- A. Maiti, P. Schaumont, "Improving the quality of a physical unclonable function using configurable ring oscillators," *International Conference on Field Programmable Logic and Applications (FPL 2009),* September 2009.
- K. Bian, J. Park, and R. Chen, “A quorum-based framework for establishing control channels in dynamic spectrum access networks,” *ACM Annual International Conference on Mobile Computing and Networking (MobiCom 2009),* Sep. 2009.
- Shukla, S.K., "Model-driven engineering and safety-critical embedded software," *IEEE Computer*, vol.42, no.9, pp.93-95, Sept. 2009.
- Edgar G. Daylight, Sandeep K. Shukla, Davide Sergio, ”Expressing the behavior of three very different concurrent systems by using natural extensions of separation logic,” CoRR 0911.2034: (September, 2009), *Electronic Lecture Notes on Theoretical Computer Science,* Elsevier.
- S. Ahuja, Deepak A. Mathaikutty, Avinash Lakshminarayana, Sandeep K. Shukla, “*Accurate power estimation of hardware co-processors using system level simulation*”, pp. 399-402, *IEEE International SOC Conference*, Sep 9-11, 2009, .
- Bijoy A. Jose, Lemaire Stewart, Jason Pribble, and Sandeep K. Shukla, “EmCodeSyn: A visual environment for multi-rate data flow specifications and code synthesis for embedded applications,” *IEEE Intl. Forum on specification and Design Languages (FDL),* Sophia Antipolis, France, Sept. 2009.

- S. Prabhakar and M. S. Hsiao, *"Using non-trivial logic implications for trace buffer-based silicon debug," IEEE Asian Test Symposium*, November 2009, pp. 131-136.
- M. S. Hsiao and M. Banga, *"Kiss the scan goodbye: a non-scan architecture for high coverage, low test data volume and low test application time," IEEE Asian Test Symposium*, November 2009, pp. 225-230.
- M. Li and M. S. Hsiao, "An ant colony optimization technique for abstraction-guided state justification," *IEEE International Test Conference*, November 2009.
- S. Donglikar, M. Banga, M. Chandrasekar, and M. S. Hsiao, "Fast circuit topology based method to configure the scan chains in Illinois scan architecture," in *Proceedings of the IEEE International Test Conference*, November 2009.
- Edgar G. Daylight, Sandeep K. Shukla, “On the difficulties of concurrent-system design, illustrated with a 2×2 switch case study,” *Formal Methods Conference (FM 2009):* 273-288, November, 2009, Eindhoven, The Netherlands, Springer.
- Bin Xue, Sandeep K. Shukla, “Analysis of latency insensitive protocols using periodic clock calculus,” *IEEE High Level Design Validation and Test*, Nov. 4-6, 2009, San Francisco, USA.
- S. Ahuja, Sandeep K. Shukla, “MCBCG: Model checking based sequential clock-gating”, pp. 20-25, *IEEE High Level Design Validation and Test*, Nov 4-6, 2009, San Francisco, CA.
- M. Chandrasekar and M. S. Hsiao, "Diagnostic test generation for silicon diagnosis with an incremental learning framework based on search state compatibility,” *IEEE High Level Design Validation and Test, pp. 68-75, November 2009.*
- K. Bian and J. Park, “Addressing the hidden incumbent problem in 802.22 networks,” *Software Defined Radio ’09 Technical Conference*, Dec. 2009.
- B. Bahrak, A. Deshpande, and J. Park, “A policy reasoner for policy-based dynamic spectrum access,” *Software Defined Radio ’09 Technical Conference*, Dec. 2009.
- Sumit Ahuja, Deepak A. Mathaikutty, Avinash Lakshminarayana, Sandeep K. Shukla, “SCOPE: statistical regression based power models for co-processors power estimation, *Journal of Low Power Electronics*,” Vol.5, No.4, pp.407-415, Dec. 2009.
- C. Han and Y. Yang, “Compatibility between optimal tree-based broadcast routing and metric design,” *IEEE Globecom*, December 2009.
- C. Na and Y. Yang, "MRSD: Multirate-based service differentiation for the IEEE 802.15.4 wireless sensor network,” *IEEE Globecom*, December 2009.

Panel:

- Sandeep Shukla organized and chaired a panel discussion on Whether SystemC is a verification language or design language. The panelists were John Sanguinetti, CTO of Forte Design Systems, Anmol Mathur, CTO of Calypto Systems, Andres Takach, Project lead of CatapultC at Mentor Graphics, Masahiro Fujita, Professor of Tokyo University,and Nasib Naser, a Senior Engineer from Synopsys.

Visitor:

- Dr. Jean-Pierre Talpin, Director, Project ESPRESSO, INRIA, France visited FERMAT lab for a week during Oct 5 – Oct 14. 2009 for collaboration on embedded software synthesis for safety critical embedded software from polychronous specification.