Center for Embedded Systems for Critical Applications

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CESCA Newsletter
Center for Embedded Systems for Critical Applications

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In this edition:

CESCA Offices & Labs
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Inaugural CESCA Day!

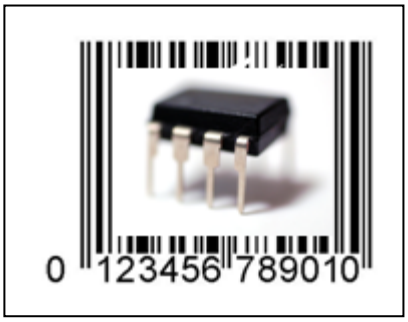
The Center for Embedded Systems for Critical Applications (CESCA) held its annual workshop titled "CESCA Day" at the Owens Banquet Hall in Blacksburg, Va., on May 6, 2010! Events included keynote, tutorials, poster sessions, and a student panel. A post workshop anonymous survey filled out online by CESCA students showed that the workshop was considered extremely favorably by students. Details on this successful CESCA Day are included in this newsletter.

CESCA continues to attract research funding. During the spring semester, several new projects were awarded. The product of CESCA's research in terms of publications continues to be strong. One paper won the best paper award! Several students graduated over the past few months.

This issue of the CESCA newsletter will feature the inaugural CESCA Day, the new projects awarded, the best paper award, as well as describing other activities.

New Research Projects

Foundations for Future On-chip Fingerprints

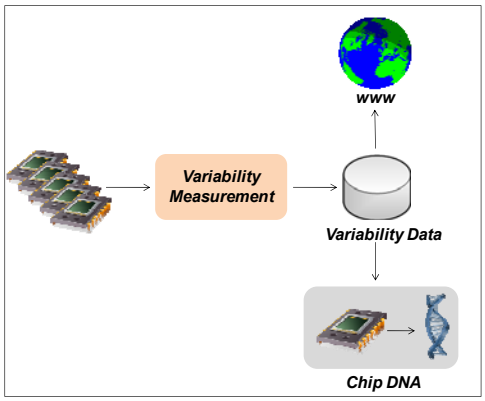


Patrick Schaumont, Leyla Nazhandali, and Inyoung Kim (Statistics Department) have received a three-year $675K grant through NSF's Trustworthy Computing Program. The project, starting in August 2010, will apply a cross-disciplinary approach to develop secure on-chip identifiers, combining expertise in statistical analysis, circuit design, digital architecture design, and embedded security. The team expects to develop techniques that will lead to on-chip fingerprints that prevent some common attacks, that will be more stable towards environmental changes and aging, and that will be significantly cheaper and easier to build and integrate. The project will validate these design techniques through prototype implementations of on-chip fingerprints in FPGA and ASIC. Through this foundational research, novel applications for secure electronic identification may be enabled. The project also includes the development of two new courses: a cross-disciplinary course in statistics and electronics for graduate students and an introductory crypto-course for pre-college students.

Related Research Results: A Large Scale Characterization of On-Chip Variability

In the Secure Embedded Systems (SES) lab of CESCA, we formulated a compact and portable experiment that could measure on-chip variability in hundreds of Xilinx Spartan 3E FPGAs used by the students in Computer Engineering major. This is a unique effort to utilize an existing valuable resource that would have remained unused otherwise.

There are two main purposes of this experiment. Firstly, we want to analyze this dataset for our research effort in PUF design. Some of the research goals are improving the stability of PUF signatures, enhancing the randomness in PUF, securing the PUF against attacks, and application of PUF to provide security to sensitive systems. The second purpose is to make this dataset publicly accessible for the research community. We believe this will help the researchers significantly as no such dataset of this size is available publicly so far.



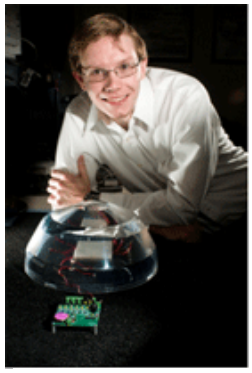
In the spring semester of 2010, we have been able to collect variability data from 125 90-nm FPGAs (Xilinx Spartan 3E - XC3S500E). Three SES members, namely Luke McHale (Junior student, Computer Engineering), Jeff Casarona (Senior student, Computer engineering), Abhranil Maiti (Graduate student, Computer Engineering) made this effort under the guidance of Patrick Schaumont (Assistant Professor, ECE Department). The detail of the experiment as well as the dataset is available at the location *http://rijndael.ece.vt.edu/variability/main.html*. Some initial analysis result is going to be published in IEEE International. Symposium on Hardware-Oriented Security and Trust (HOST) to be held at Anaheim, CA in June,2010. In future, we plan to expand this experiment with further analysis of the collected dataset. This project is supported by National Science Foundation (NSF) grant no 0855095.

Collaborative Research: Enhancing Access to the Radio Spectrum (EARS) Workshop

Sponsor: NSF, Start: 4/15/2010, Duration: 1 year, PIs: Jennifer T Bernhard (PI, UIUC), Jeff Reed (PI, VT), Jung-Min Park (co-PI, VT), Amount: $96K

Enhancing Access to the Radio Spectrum (EARS) is a multi-disciplinary activity whose goal is to improve the efficiency with which the radio spectrum is utilized and to improve access to the radio spectrum in support of current and new technologies. Achieving these goals will, among other impacts, improve the availability of wireless broadband to Americans presently without broadband access, as called for in the American Recovery and Reinvestment Act. Because the radio spectrum is a valuable but finite natural resource, improvements in spectrum efficiency will have significant economic impact to the nation and the world. This award funds the first step, which is an invitational workshop that will bring together some of the key researchers and policy makers involved in radio spectrum access. All relevant fields will be represented, including science, engineering, economics, and policy. The output of the workshop will include a vision for the future of radio spectrum access and use, and a prioritized list of research areas that can help achieve that vision.

Ha receives a Project for Solar and Thermal Energy Harvesting Research.

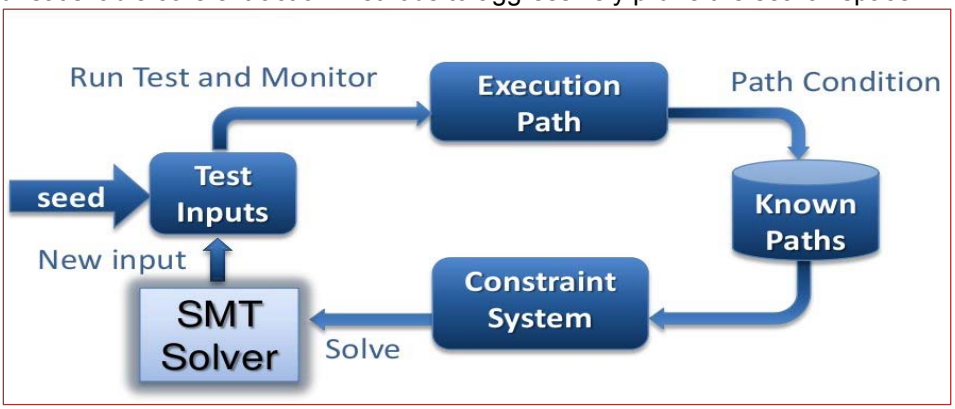

<Justin Cartwright>

Ha received a two-year project from Acellent Technologies, which develops a structural health monitoring sensor node for infrastructure. The major goal of the project is to develop an energy harvesting system for solar and thermal, which powers up the Acellent's sensor node. His team investigates all aspects of the energy harvesting system including design of a thermal harvester with a cooling system, a battery charging circuit, and voltage boosters and regulators. Currently, Ha's team is working with three companies in energy harvesting from solar, thermal, and vibrations. Ha has set up a CESCA lab to facilitate his group's

energy harvesting research. The amount of funding for the project is $150K for two years, and Ph.D. Student Justin Cartwright will lead the project.

Software Verification Research Funded by Intel

The goal of this one-year research for Michael Hsiao is to investigate and develop heuristics for concolic testing of software. In particular, control and data dependencies as well as non-chronological backtracking will be explored extensively. The dependency will be used to ensure that a test case that covers a branch also makes it observable at a primary output. The proposed approaches will optimize path exploration strategies, in addition to discovery of new heuristics and solvers (in Satisfiability Modulo Theories domain) that address software verification techniques. These include path pruning and unsatisfiable core extraction methods to aggressively prune the search space.



Best Paper Award

ASP-DAC Best Paper Award

<Dr. Domer receiving the award on behalf of the authors>

SCGPSim: A fast SystemC simulator on GPUs by Mahesh Nanjundappa, Hiren Patel, Bijoy Jose, Sandeep Shukla won the "Best paper award" in Asia South-Pacific: Design Automation Conference (ASP-DAC), 2010.

The objective of this paper was to speed up the simulation performance of SystemC designs at the RTL abstraction level by exploiting the high degree of parallelism afforded by today's general purpose graphics processors(GPGPUs). We mimic SystemC's discrete event simulation (DES) execution model using a model of concurrent threads which synchronize as and when necessary. This concurrent thread model was then ported to GPGPUs. Our simulation infrastructure, SCGPSim does the mapping and source-to-source (S2S) translation of synthesizable SystemC models into parallelly executable programs targeting an NVIDIA GPU. The translator retains the simulation semantics of the original designs by applying semantics preserving transformations. The resulting transformed models mapped onto the massively parallel architecture of GPUs improve simulation efficiency quite substantially. Preliminary experiments with varying-sized examples such as AES, ALU, and FIR have shown simulation speed-ups ranging from 30x to 100x. Considering that our transformations are not yet optimized, we believe that optimizing them will improve the simulation performance even further.

New Bradley Fellow

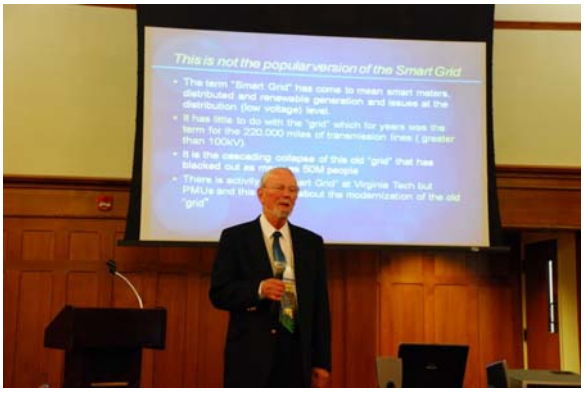
T. Shaver Deyerle IV has been selected as a Bradley Fellow of the ECE Department starting from Fall 2010, which is the most prestigious award available within the Department. Bradley Fellowships are available to outstanding U.S. Ph.D. applicants, and a Bradley Fellow is awarded in the amount of $27,500 and tuition for three academic years. Shaver Deyerle received a BS degree from Virginia Tech in Spring 2010 and will pursue his Ph.D. degree in analog, mixed-signal and RF IC design under Dong Ha's supervision. Shaver Deyerle was a summer intern at Cisco in 2008 and Qualcomm in 2009 and 2010. He was a project leader for Virginia Tech Autonomous Underwater Vehicle Team from 2006 to 2007 and has been active in Virginia Tech's FM radio station (WUVT) since Fall 2007. He is a recipient of numerous awards including the prestigious Micron Scholar award (sponsored by Micron Technology Inc.), Karl Egerer/Kollmorgan Electrical Engineering Scholarship (2009 -2010), Frederick C. Grant Scholarship (2009 – 2010), and the Mr. & Mrs. Gilbert Faison Scholarship (2008 – 2009).

CESCA Day (May 6, 2010)

<Prof. Scott Midkiff, the head of the Bradley Dept. of ECE>

The one day workshop was inaugurated by Prof. Scott Midkiff, the head of the Bradley Department of Electrical and Computer Engineering, and the keynote address was delivered by Jim Thorp, past head of ECE, and *Hugh P. and Ethel C. Kelly Professor Emeritus, Virginia Tech.* In his keynote address Thorp discussed the role of cyber physical systems in the Smart Grid, in particular, in the smart transmissions systems, by facilitating wide area measurements in power systems.

By design, CESCA day focused on the graduate and undergraduate students in CESCA. Currently CESCA has eight faculty members, and almost 60 graduate students, and around 10 undergraduate researchers working on various problems related to embedded systems design and deployment.



<Jim Thorp, past head of ECE>

In particular, CESCA focuses on fundamental design concepts and tools for low-power hardware design, VLSI, testing and verification, secure hardware and networking, sensor networks, formal models, and languages, vision and image processing, as well as applications such as structural health monitoring, finger print characterizations, smart power grid etc.

The workshop featured three tutorials by faculty on success strategies for graduate research, finding internships, co-op and job opportunities, and the key to write successful research articles. One major aspect of the workshop was two extensive poster sessions where 39 individual or groups of CESCA students showcased their research in two poster sessions. Each poster session for 90 minutes, and displayed around 20 posters from various students displaying their major research accomplishments.

Finally, a student panel, moderated by Prof. Lynn Abbott allowed some senior graduate students to express their views on the curriculum, research facilities, and exposures, and opportunities afforded to them by CESCA during their graduate studies, and their vision on future of CESCA.

A post workshop anonymous survey filled out online by CESCA students showed that the workshop was considered extremely favorably by students. A highlight of the survey results that about 10 masters student said that the event changed their mind towards a doctoral study path from their current plans of just getting a masters degree. This is an indicator of the fact that students actually were influenced by the various talks, tutorials, panel discussion and posters.


<CESCA Students at Lunch>


<CESCA Faculty during a Break>

<A group picture on CESCA Day, May 6, 2010>

Celebrating Graduates (Jan-May 2010)

- Jong-Suk Lee (Advisor: D. Ha), "FleXilicon: a New Coarse-grained Reconfigurable Architecturefor Multimedia and Wireless Communications" Ph.D. Jan. 2010.
- Dao Zhou (Advisor: D. Ha), "Ultra Low-Power Wireless Sensor Node for Structural Health Monitoring," M.S. Jan. 2010.
- Xueqi Cheng (Advisor: Michael Hsiao), “Exploring Hybrid Dynamic and Static Techniques for Software Verification,” Ph. D., February, 2010.
- Amol Deshpande (Advisor: Jung-Min Park), “Policy Reasoning for Spectrum Agile Radios”, M.S. May 2010.
- Swati Kanaujia (Advisor: Jung-Min Park), “Rogue Access Point Detection through Statistical Analysis”, M.S., May 2010.
- Sumit Ahuja (Advisor: S. Shukla), “High Level Power Estimation and Reduction Techniques for Power Aware Hardware Design”, Ph. D. May 2010.
- Mahesh Nanjundappa (Advisor: S. Shukla), “Accelerating Hardware Simulation on Multi-cores,” M.S., May 2010.

Publications (Jan - May 2010)

Book Chapter:

- Bijoy A. Jose, Bin Xue, Sandeep K. Shukla, and Jean-Pierre Talpin, Programming models for Multi-Core Embedded Software, Book Chapter in “Multi-Core Embedded Systems”, CRC Press, Taylor & Francis, London 2010

Journal and Conferences:

- H. Zhai, S. Sha, V.K. Shenoy, S. Jung, M. Lu, K. Min, S. Lee, and D.S. Ha, “An Electronic Circuit System for Time-Reversal of Ultra-Wideband Short Impulses based on Frequency Domain Approach,” IEEE Transactions on Microwave Theory and Techniques, Vol. 58, No. 1, pp.74-86, January 2010.
- S. Ahuja, W. Zhang, A. Lakshminarayana, S. K. Shukla, "A Methodology for Power Aware High-Level Synthesis of Co-processors from Software Algorithms," VLSI Design, International Conference on, pp. 282-287, 2010 23rd International Conference on VLSI Design, Bangalore, India, Jan 2010.
- B.A. Jose, S.K. Shukla, "An Alternative Polychronous Model and Synthesis Methodology for Model-Driven Embedded Software", Proceedings of Asia-Pacific Design Automation Conference, Taipei, Taiwan, Jan 2010, pp. 13-18, IEEE.
- M. Nanjundappa, H. D Patel, B. A Jose, S. K Shukla, "SCGPSim: A Fast SystemC Simulator on GPUs", Proceedings of Asia-Pacific Design Automation Conference, Taipei, Taiwan, Jan 2010, pp. 149 - 154.
- S. Prabhakar and M. S. Hsiao, "Multiplexed trace signal selection using non-trivial implication-based correlation," in Proceedings of the IEEE Symposium on Quality Electronic Design, March, 2010, pp. 697-704.
- A. Lakshminarayana, S. Ahuja, S. Shukla, "Coprocessor Design Space Exploration Using High Level Synthesis", to appear in the Proceedings of International Symposium on Quality Electronic Design (ISQED'10), pp. 874-884, March 2010, San Jose, CA, IEEE Press.
- S. Deyerle, D.S. Ha, and D.J. Inman, “A Low-Power System Design for Lamb Wave Methods,” SPIE International Symposium on Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring, (8 pages), March 2010.
- D. Zhou, N. Kong, D.S. Ha, and D.J. Inman, “A Self-powered Wireless Sensor Node for Structural Health Monitoring,” SPIE International Symposium on Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring, (12 pages), March 2010.
- S. Morozov, A. Maiti, P. Schaumont, "A Comparative Analysis of Delay Based PUF Implementations on FPGA," 6th International Symposium on Applied Reconfigurable Computing, March 2010.
- M. Li, Y. Zheng, M. S. Hsiao, and C. Huang, "Reversible logic synthesis through ant colony optimization," in Proceedings of the IEEE Design Automation and Test in Europe Conference, March 2010.
- Z. Chen, P. Schaumont, "pSHS: A Scalable Parallel Software Implementation of Montgomery Multiplication for Multicore Systems," Design, Automation and Test in Europe (DATE 2010), March 2010.
- M. B. Henry and L. Nazhandali, “From Transistors to MEMS: Throughput AwarePower-Gating in CMOS Circuits,” Design, Automation & Test in Europe Conference, DATE '10.pp.130-136, Dresden, Germany, 8-12 March 2010.
- M. Chandrasekar, N. P. Rahagude and M. S. Hsiao, "Search state compatibility based incremental learning framework and output deviation based X-filling for diagnostic test generation," in Journal of Electronic Testing: Theory and Applications, vol. 26, no. 2, pp. 165-176, April 2010.
- Yujun Li and Yaling Yang, "Rules for Designing Routing Metrics for Greedy,Face and Combined-Greedy-Face Routing", IEEE Transactions on Mobile Computing, Volume 9 , Issue 4, Pages: 582-595, April 2010.
- Bin Xue, Sandeep K. Shukla, "Analysis of Scheduled Latency Insensitive Systems with Periodic Clock Calculus", Journal of Electronic Testing, Vol. 26, No. 2. (1 April 2010), pp. 227-242
- Jens Brandt, Klaus Schneider, Sandeep K. Shukla: Translating concurrent action oriented specifications to synchronous guarded actions. ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES 2010), pp. 47-56, Stockholm, April 2010.
- Yujun Li and Yaling Yang, "Asymptotic Connectivity of Large-Scale Wireless Networks with a Log-Normal Shadowing Model", IEEE VTC 2010-Spring.

- Zhenhua Feng and Yaling Yang, "Throughput Analysis of Secondary Networks in Dynamic Spectrum Access Networks", IEEE Infocom 2010 Workshop on Cognitive Wireless Communications and Networking, 2010.
- N. Kong, D.S. Ha, A. Erturk, and D.J. Inman, “Resistive Impedance Matching Circuit for Piezoelectric Energy Harvesting,” Journal of Intelligent Material Systems and Structures. (Online version: http://jim.sagepub.com/cgi/rapidpdf/1045389X09357971v1).
- N. Kong, T. Cochran, D.S. Ha, H.-C. Lin, D.J. Inman, "A Self-powered Power Management Circuit for Energy Harvested by a Piezoelectric Cantilever," Applied Power Electronics Conference and Exposition, pp. 2154 -2160, February 2010.

Disclosures:

- J.-M. Park and B. Bahrak, "A methodology for spectrum access policy reasoning in cognitive radios", VTIP Disclosure No.10-046.
- D. S. Ha, T. S. Deyerle IV, and D. J. Inman, “A Low-Power Method for the Lamb Wave Method of Structural Health Monitoring,” VTIP Disclosure No. 10-127, 2010.

Invited Talks and Events:

- Dong S. Ha, “Low-Power Active Wireless Sensor Node for Structural HealthMonitoring,” University of Virginia, Charlottesville, April 19, 2010.
- Dr. Sandeep Shukla was invited to attend the US-German Frontiers of Engineering Conference organized jointly by the US National Academy of Engineering and Humboldt Foundation of Germany. Only 60 participants from US and Germany were invited to attend this conference. The conference was held at the Oak Ridge National Laboratory during April 25-27, 2010.

Conference Organizations:

- Patrick Schaumont served as vice program chair for the IEEE International Symposium on Hardware-Oriented Security and Trust.

End Note from Director

The University is on summer break now, and the campus is once again tranquil due to far fewer students enrolling for summer classes than regular semesters. It’s the right time to look back at what CESCA has achieved in the past one year and plan for the future. CESCA has made steady progress in all aspects towards becoming better as a broad based research center. CESCA has published about 70 journal and conference papers in the year 2009, and authored or edited several books and book chapters. Although the number itself does not reflect quality of CESCA research, but it speaks well of CESCA’s research activities. CESCA faculty members have been awarded numerous new research projects from small to medium scale in the past year, as reported in CESCA newsletters throughout the year, including a few in this newsletter. CESCA held 17 weekly seminars during 2009-10 academic year and most of speakers were external experts including a handful from other universities. CESCA seminars continuously drew good attendance. I hope it is due to the technical quality of seminars rather than pizza provided at the seminars! CESCA started the inaugural CESCA Day in early May this year, which was quite successful as evidenced by the student satisfaction survey. It provided an invaluable opportunity for all CESCA students and faculty to get to know each other’s research activities.

I believe CESCA is on the right track for succeeding as a research center. CESCA has created a culture of collaboration among different CESCA groups. While emergence of such culture is necessary, it is not sufficient for our collective success. We must nurture this collaborative spirit in order to flourish. In this regard, I ask each CESCA member to contribute to CESCA to the best of his/her capability. We know that a successful center does not come easily; it is the result of its members’ hard work. I wish all of you another productive summer. Thank you very much. Dong Ha