Very High Frequency Integrated POL for CPUs

Dongbin Hou

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Fred C. Lee, Chair
Qiang Li
Rolando Burgos
Daniel J. Stilwell
Dwight D. Viehland

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Abstract

Point-of-load (POL) converters are used extensively in IT products. Every piece of the integrated circuit (IC) is powered by a point-of-load (POL) converter, where the proximity of the power supply to the load is very critical in terms of transient performance and efficiency. A compact POL converter with high power density is desired because of current trends toward reducing the size and increasing functionalities of all forms of IT products and portable electronics. To improve the power density, a 3D integrated POL module has been successfully demonstrated at the Center for Power Electronic Systems (CPES) at Virginia Tech. While some challenges still need to be addressed, this research begins by improving the 3D integrated POL module with a reduced DCR for higher efficiency, the vertical module design for a smaller footprint occupation, and the hybrid core structure for non-linear inductance control.

Moreover, as an important category of the POL converter, the voltage regulator (VR) serves an important role in powering processors in today's electronics. The multi-core processors are widely used in almost all kinds of CPUs, ranging from the big servers in data centers to the small smartphones in almost everyone's pocket. When powering multiple processor cores, the energy consumption can be reduced dramatically if the supply voltage can be modulated rapidly based on the power demand of each core by dynamic voltage and frequency scaling (DVFS). However, traditional discrete voltage regulators (VRs) are not able to realize the full potential of DVFS since

they are not able to modulate the supply voltage fast enough due to their relatively low switching frequency and the high parasitic interconnect impedance between the VRs and the processors. With these discrete VRs, DVFS has only been applied at a coarse timescale, which can scale voltage levels only in tens of microseconds (which is normally called a coarse-grained DVFS). In order to get the full benefit of DVFS, a concept of an integrated voltage regulator (IVR) is proposed to allow fine-grained DVFS to scale voltage levels in less than a microsecond. Significant interest from both academia and industry has been drawn to IVR research.

Recently, Intel has implemented two generations of very high frequency IVR. The first generation is implemented in Haswell processors, where air core inductors are integrated in the processor's packaging substrate and placed very closely to the processor die. The air core inductors have very limited ability in confining the high frequency magnetic flux noise generated by the very high switching frequency of 140MHz. In the second generation IVR in Broadwell processors, the inductors are moved away from the processor substrate to the 3DL PCB modules in the motherboard level under the die.

Besides computers, small portable electronics such as smartphones are another application that can be greatly helped by IVRs. The smartphone market size is now larger than 400 billion US dollars, and its power consumption is becoming higher and higher as the functionality of smartphones continuously advances. Today's multi-phase VR for smartphone processors is built with a power management integrated circuit (PMIC) with discrete inductors. Today's smartphone VRs operate at 2-8MHz, but the discrete inductor is still bulky, and the VR is not close enough to the processor to support fine-grained DVFS. If the IVR solution can be extended to the smartphone platform, not only can the battery life be greatly improved, but the total power consumption of the smartphone (and associated charging time and charging safety issues) can also be significantly reduced. Intel's IVR may be a viable solution for computing applications, but the air core inductor with un-confined high-frequency magnetic flux would cause very severe problems for smartphones, which have even less of a space

budget. This work proposes a three-dimensional (3D) integrated voltage regulator (IVR) structure for smartphone platforms. The proposed 3D IVR will operate with a frequency of tens of MHz. Instead of using an air core, a high-frequency magnetic core without an air gap is applied to confine the very high frequency flux. The inductor is designed with an ultra-low profile and a small footprint to fit the stringent space requirement of smartphones.

A major challenge in the development of the very high frequency IVR inductor is to accurately characterize and compare magnetic materials in the tens of MHz frequency range. Despite the many existing works in this area, the reported measured properties of the magnetics are still very limited and indirect. In regards to permeability, although its value at different frequencies is often reported, its saturation property in real DC-biased working conditions still lacks investigation. In terms of loss property, the previous works usually show the equivalent resistance value only, which is usually measured with small-signal excitation from an impedance/network analyzer and is not able to represent the real magnetic core loss under large-signal excitation in working conditions. The lack of magnetic properties in real working conditions in previous works is due to the significant challenges in the magnetic characterization technique at very high frequencies, and it is a major obstacle to accurately designing and testing the IVR inductors. In this research, an advanced core loss measurement method is proposed for very high frequency (tens of MHz) magnetic characterization for the IVR inductor design. The issues of and solutions for the permeability and loss measurement are demonstrated. The LTCC and NEC flake materials are characterized and compared up to 40MHz for IVR application.

Based on the characterized material properties, both single-phase and multi-phase integrated inductor are designed, fabricated and experimentally tested in 20MHz buck converters, featuring a simple single-via winding structure, small size, ultra-low profile, ultra-low DCR, high current-handling ability, air-gap-free magnetics, multi-phase integration within one magnetic core, and lateral non-uniform flux distribution. It is found that the magnetic core operates at unusually high core loss density, while it is thermally manageable. The PCB copper

can effectively dissipate inductor heat with 3D integration. In addition, new GaN device drivers and magnetic materials are evaluated and demonstrated with the ability to increase the IVR frequency to 30MHz and realize a higher density with a smaller loss.

In summary, this research starts with improving the 3D integrated POL module, and then explores the use of the 3D integration technique along with the very high frequency IVR concept to power the smartphone processor. The challenges in a very high frequency magnetic characterization are addressed with a novel core loss measurement method capable of 40MHz loss characterization. The very high frequency multi-phase inductor integrated within one magnetic component is designed and demonstrated for the first time. A 20MHz IVR platform is built and the feasibility of the concept is experimentally verified. Finally, new GaN device drivers and magnetic materials are evaluated and demonstrated with the ability to increase the IVR frequency to 30MHz and realize higher density with smaller loss.

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General Audience Abstract

This research focuses on reducing the size, footprint, and power loss of the power supply for the CPUs in different applications, ranging from the big servers in data centers to the small smartphones in almost everyone's pocket. To achieve this goal, novel characterization, design, and integration technique is developed, especially for the bulky magnetic components, with much faster (~10X) switching speed than the nowadays practice. This research opens the door to the development of the next generation of CPUs' power supply with very high switching speed, simple structure, high integration level, and high current handling ability.

TO MY FAMILY

AND TO WHOM IT MAY CONCERN

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Chapter 1. Background and Introduction

Information technology greatly influences our daily lives in almost everything that we do. The information that can be accessed on the internet is infinite. In front of your PC, you can virtually visit any country you wish with pictures, information, and videos that create the feeling that you are there. Smartphones become smarter every day and laptops are taking the place of desktops more and more. All of these rely on the prosperity of the semiconductor industry. Every piece of integrated circuit (IC) is powered by a point-of-load (POL) converter, where the proximity of the power supply to the load is very critical in terms of transient performance and efficiency. With the trend in reducing the size and increasing functionalities of all forms of IT products and portable electronics, a compact POL converter with high power density is desired. A 3D integrated POL concept was proposed to increase the power density of the POL module. In the first chapter, the 3D integration technology will be reviewed and its remaining challenges will be demonstrated.

Moreover, as an important category of the POL converter, the voltage regulator (VR) serves an important role in powering processors in today's electronics, ranging from big servers in datacenters to small smartphones in almost everyone's pocket. A very high frequency integrated voltage regulator (IVR) concept in powering Intel's multi-core processor will be demonstrated in this chapter, and then the implementation of the IVR concept with 3D integrated magnetics in the smartphone application will be proposed. The available high frequency switching devices and magnetic materials for the integration will also be reviewed in this chapter.

1.1. 3D integrated point-of-Load (POL) module

The desire for smaller and smarter electronic devices generates a significant demand to improve the power density of the POL converter. For example, [1] demonstrates that more than 30% of the real estate of the desktop motherboard designed for Intel i7 CPU is occupied by voltage regulators. Reducing the size and number of the bulky inductors and capacitors and improving the POL power density would save remarkably valuable motherboard space for more functions and better performance.

The conventional POL products with >15A output current are usually constructed by discrete components, as shown in Figure 1.1, where the magnetic becomes the bottleneck for footprint and thickness and limits the POL power density to around 100W/in^3 [1, 2]. In order to reduce the converter footprint and fully utilize the available space, the 3-Dimensional (3D) integration concepts shown in Figure 1.2 are proposed, which elaborate the bulky magnetic component as a low-profile substrate where the active components are placed. [3-6] first explores the possibility of demonstrating the 3D integrated high current POL module with a low temperature co-fired ceramic (LTCC) inductor substrate. CPES has developed a series of generations of the POL module with high output current larger than 15A based on LTCC integration technology.

Figure 1.1. High current POL modules with discrete components.

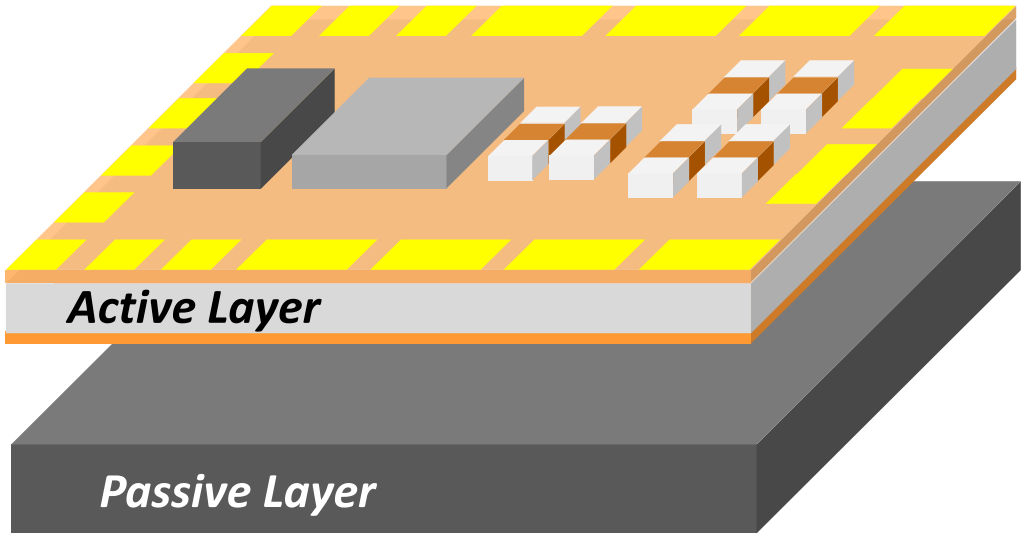
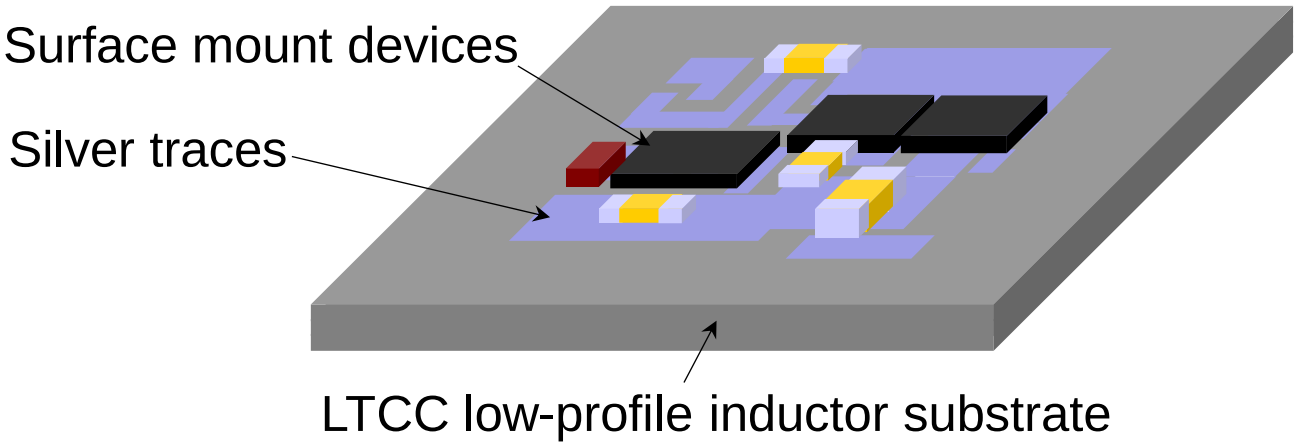


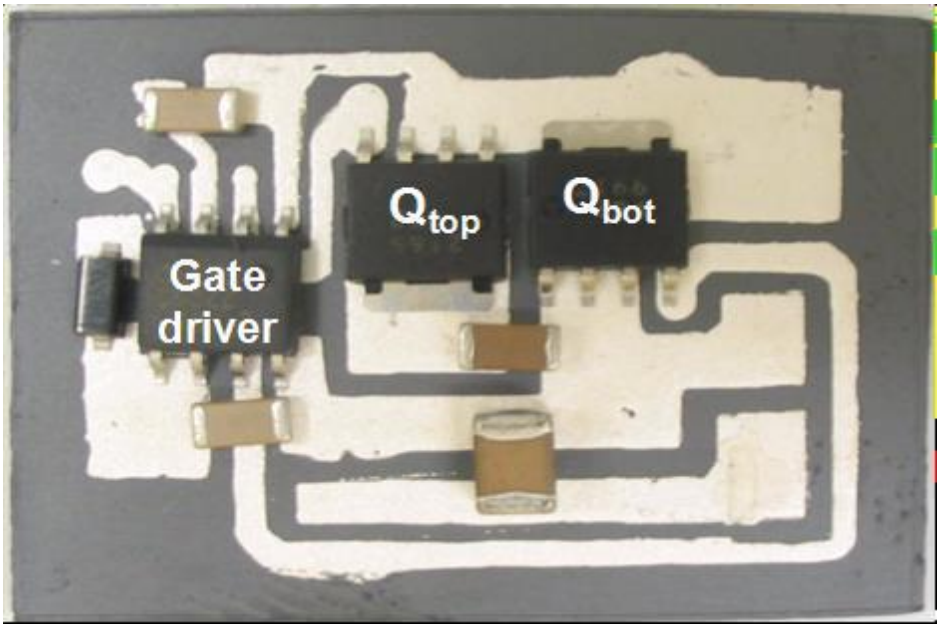
Figure 1.2. Basic structure of the 3D integration.

Figure 1.3 shows the first generation of the 3D integrated POL module, where the surface mount active devices as well as the capacitors are directly placed on the top of a low-profile LTCC inductor substrate. The connections of all of the components are implemented by the printed silver paste, which is co-fired with LTCC ferrite.

However, this earlier product has its limits for high-frequency operation. The parasitics introduced by the connection of each component are increased significantly by the inductor substrate, which causes large ringing and increase switching loss. Therefore, a slight modification has been made in the second generation of the 3D integrated POL module. As shown in Figure 1.4, a conductive shielding layer is added to block the magnetic interaction between the active layer and the LTCC inductor substrate. A comparison between the prototypes with and without the shield proves that both the ringing and efficiency are significantly improved by adding the shielding layer[7].



(a)



(b)

Figure 1.3. The first generation of the 3D integrated POL module with LTCC inductor substrate developed by CPES [7]: (a) the conceptual drawing, (b) the prototype.

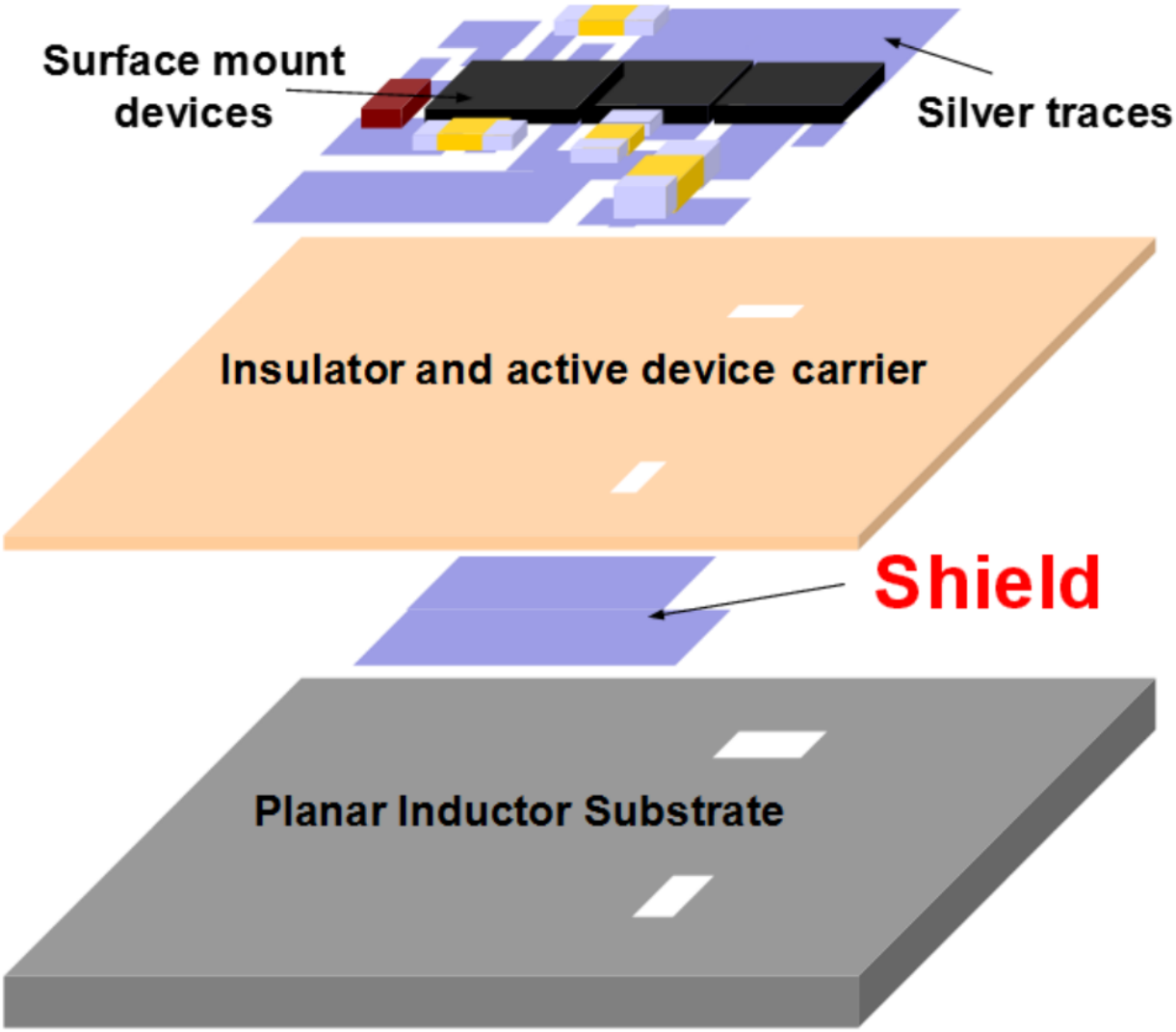


Figure 1.4. The second generation of the 3D integrated POL module with LTCC inductor substrate developed by CPES[7].

In the third generation of this product, the printed silver traces for the connection of components, the insulation layer, and the shielding layer are combined together, and implemented by a two-layer AlN (aluminum-nitride) DBC (direct-bonded copper) ceramic[2]. Because of the very high thermal conductivity of the AlN DBC, the heat generated from the active devices can be quickly and effectively spread out into a large volume rather

than be restricted in a small area. The temperature distribution of the whole module is almost uniform, without any hotspots. Furthermore, the active bare-die devices are embedded inside the AlN ceramic. As shown in Figure 1.5, this solution allows the placement of the decoupling capacitor directly on top of the active device, which minimizes the parasitic loop inductance to only 0.82nH. The ultra-low parasitics enable high-frequency operation of the POL converter, maintaining high efficiency. The prototype of the third generation integrated POL module shown in Figure 1.6 achieves 250W/in^3 power density with a 15A output current.

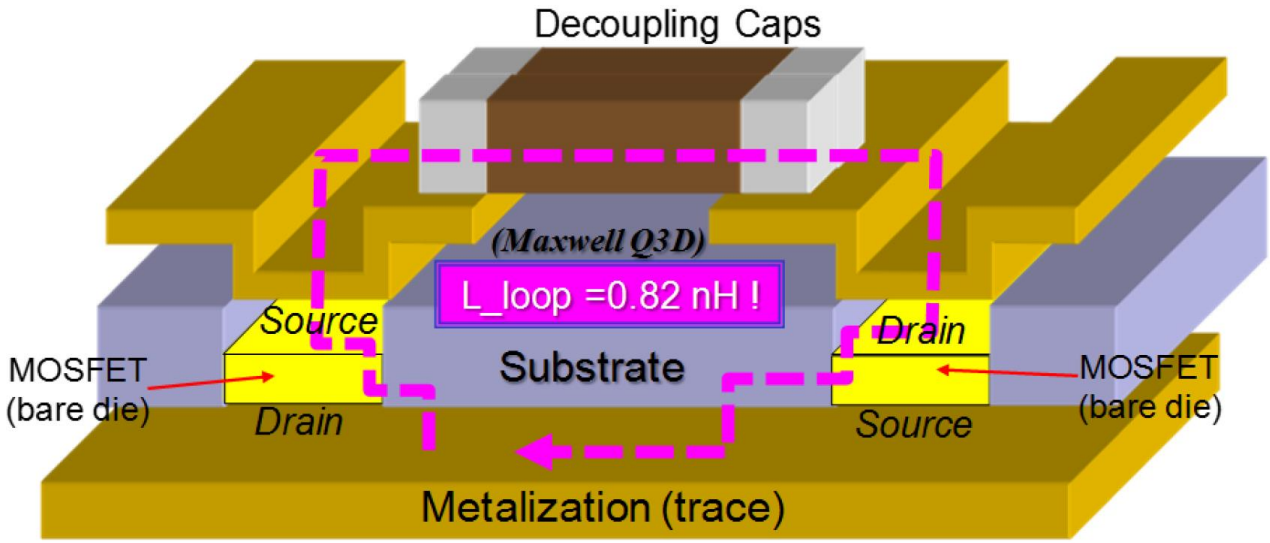


Figure 1.5.The active layer design for the third generation of the 3D integrated POL module at CPES[8].

The power density of the 3D integrated POL module can be further increased by magnetic inverse coupling or optimization of the flux pattern of the inductor. Taking the fourth-generation module as an example, the two-phase POL module with a LTCC inverse coupled inductor substrate as shown in Figure 1.7, increases the output current to 40A, and achieves power density as high as 500W/in^3 [9].

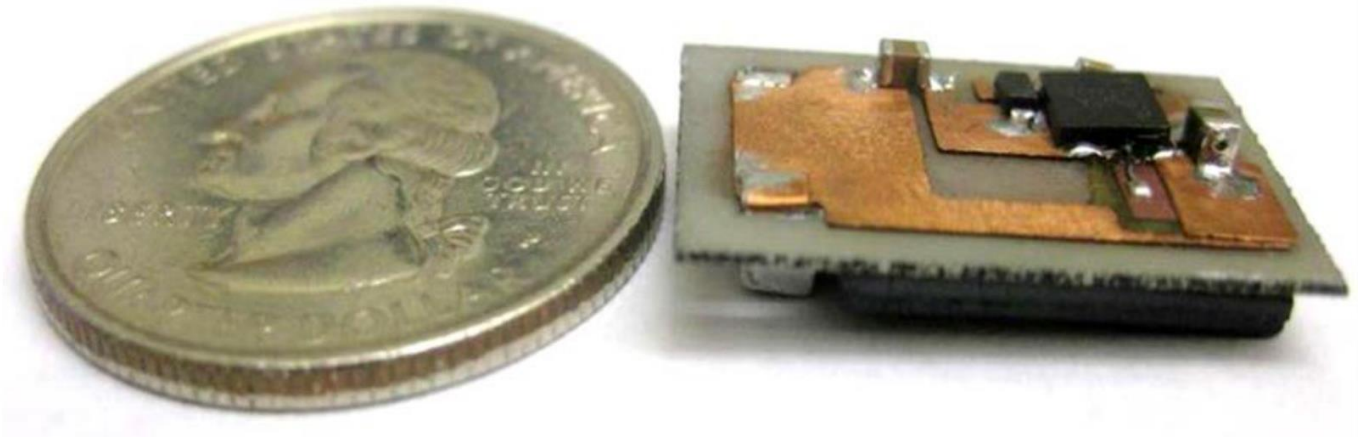


Figure 1.6. The prototype of the third generation 3D integrated POL module.

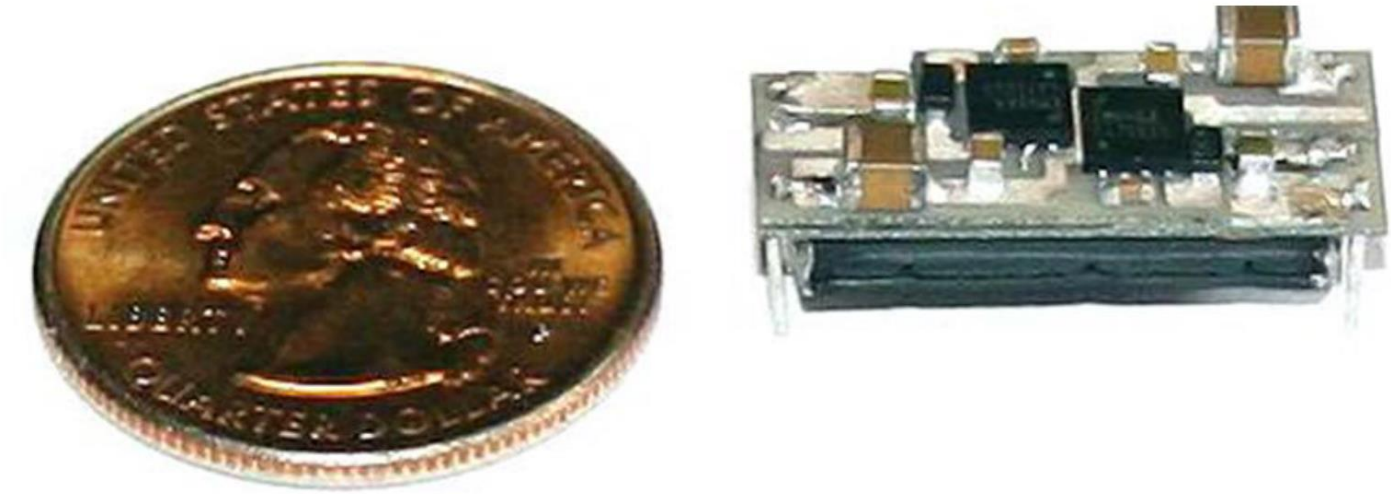


Figure 1.7. The fourth generation of the 3D integrated POL module with an LTCC inverse coupled inductor with lateral flux pattern [9].

Furthermore, [2] reveals the advantage of the lateral flux inductor in the low profile inductor substrate design. This design is one of the most critical issues for the 3D integrated POL module to achieve high power density. Many different magnetic structures have been tried to improve the performance of planar inductor substrates, such as the spiral winding designs in [10-13], meandering coil designs in [3-6, 14], and toroidal coil designs in [15-17]. To generalize the design guidelines for the planar inductor substrate, [2] proposed to categorize the different structures into two main groups, according to the flux path pattern. The spiral winding and meander coil are classified into the vertical flux inductor, in which the plane of the flux path is perpendicular with respect to the substrate. Meanwhile the toroidal coil is grouped into the lateral flux inductor, in which the plane of the flux path and the substrate are in parallel. The basic unit cells to construct the planar inductors with different flux pattern are illustrated in Figure 1.8.

(a) (b)

Figure 1.8. Basic unit cells for different planar inductors: (a) vertical flux inductor, (b) lateral flux inductor.

As we know, with a given winding cross-section area, a cylindrical winding gives the shortest magnetic path length. If the inductor thickness is limited to a certain value, sometimes the cylindrical winding can no longer be used. As an alternative, a rectangular winding with a higher aspect ratio has to be used to allow the passage of a certain current, which may decrease the energy density due to the increasing of the flux path length. In the lateral flux inductor, a cylindrical winding can always be used to minimize the flux path length, no matter what thickness it is. The flux distribution has essentially been decoupled from the inductor thickness. The comprehensive comparison in [2] shows that the maximum inductance density that can be achieved by the lateral flux inductor is always higher than that of the vertical flux inductor, especially when the output current of the inductor is higher than 10A and the required thickness of the inductor is below 3mm.

The inductance of the vertical flux inductor is mainly controlled by the length of the winding and sometimes the straight winding is bent for the real implementation, as shown in Figure 1.9.

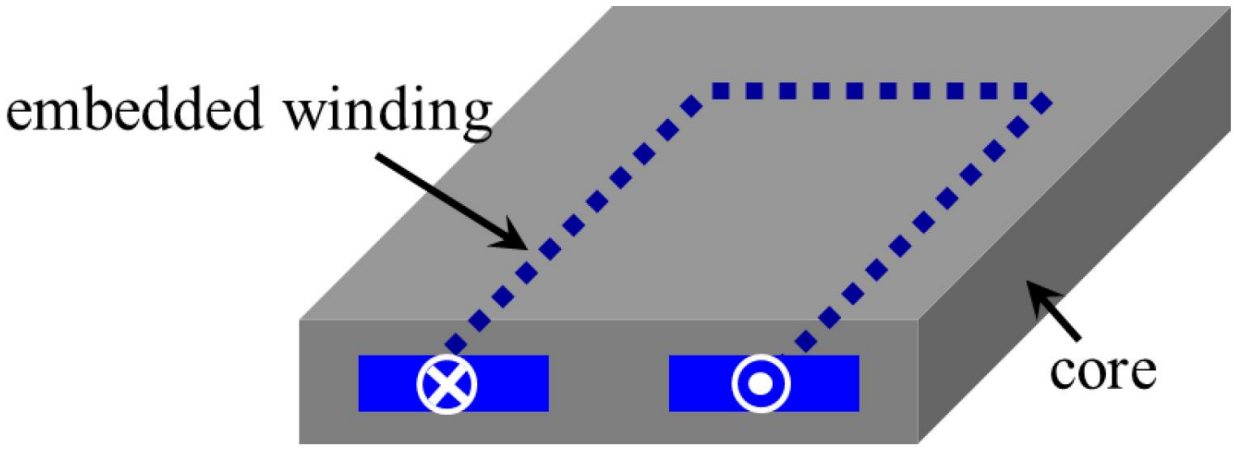
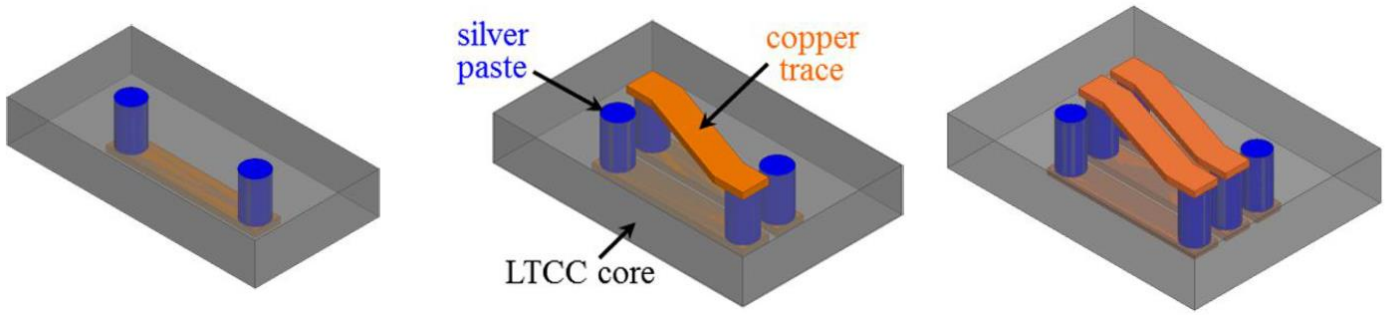


Figure 1.9. Real implementation of the vertical flux inductor in [7].

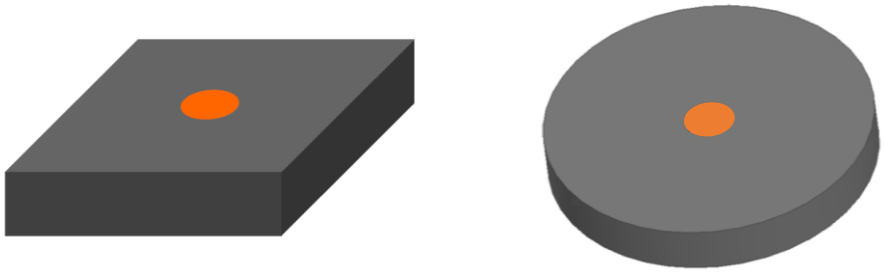
The single-turn lateral flux inductor is illustrated in Figure 1.10(a), and is essentially constructed by placing the two identical basic cells with lateral flux in Figure 1.8 (b) side by side, and then connecting them using the surface copper on the bottom of the core. The inductor structure can be easily extended to two-turn or three-turn structures by adding more vias and copper traces, as shown in Figure 1.10 (b) and Figure 1.10 (c). The adjacent turns should be placed as close as possible to increase the mutual coupling. Higher inductance density can be achieved by increasing the number of turns, while the resistive loss of the winding suffers. Both the analytical and finite element analysis (FEA) simulation models have been proposed and validated at CPES to predict the inductance [18] and core loss [19] of the lateral flux inductor substrate.



(a) (b) (c)

Figure 1.10. Real implementation of the LTCC lateral flux inductor in [2]: (a) single-turn structure, (b) two-turn structure, (c) three-turn structure.

The single-turn lateral flux inductor is essentially constructed by two lateral flux unit cells in square as shown in Figure 1.11 (a), which can be approximated and simplified by the circular shape disc core in Figure 1.11 (b), because there is very little flux in the four corners [2].



(a) (b)

Figure 1.11. Half core of the single-turn lateral flux inductor: (a) unit cell in square, (b) disc core in circle.

The DC and AC flux distribution of the disc core at different working conditions are compared in Figure 1.12[1]. The first column is the scales for DC flux and AC flux plotting. The second column is the DC flux distribution at the given DC current. The third column is the AC flux under the labeled AC peak current ripple and the corresponding DC bias in the second column. The AC peak current ripple is kept as 30% of the DC bias current for all the cases. Analysis shows that the DC flux is always distributed in the same manner, the inner core has a higher DC flux and the outer core has a lower DC flux, since the DC flux is only determined by Ampere's Law. The AC flux distributions at different working conditions are quite different from the DC flux distribution.

When the DC bias current is lower, such as 5A and 10A, the pattern of the AC flux distribution is similar to that of the DC flux, namely the inner flux is higher and outer flux is lower. If the DC bias current becomes high enough, like 15A and 20A, to saturate the inner part of the disc core, most of the AC flux has been pushed to the outer part of the disc core. Because the permeability of the inner saturated core becomes much lower, its magnetic reluctance is increased significantly, even though it has shorter flux path. The AC flux will automatically avoid the saturated core, where the reluctance is large. Only a very little AC flux is left in this region with high DC flux. This DC and AC flux counterbalance mechanism actually limits the AC flux, as well as the core loss in the saturated core, which makes the saturation not detrimental any more.

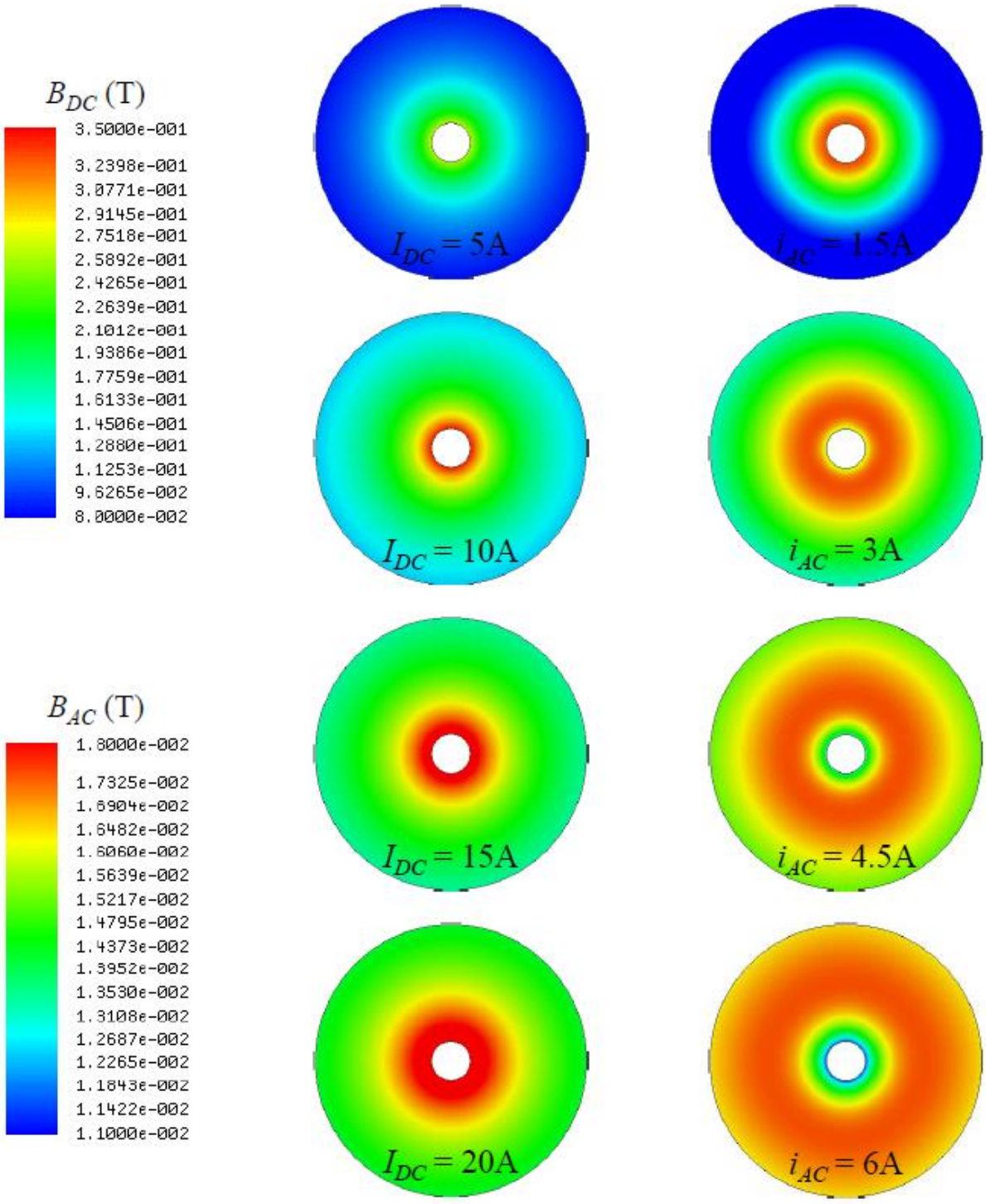


Figure 1.12. DC flux and AC flux distributions in disc core at different DC bias current[1].

Based on the LTCC ferrite core, the vertical flux and lateral flux inductor substrates are designed and fabricated for a 3D-integrated POL module. With the same inductance and core thickness (2mm), the lateral flux structure decreases the footprint by more than 30%. As a compromise, the DC resistance of the winding is increased by 18%. The prototypes of the different planar inductors are compared in Figure 1.13. By switching the flux pattern in the inductor substrate from vertical flux to lateral flux, the power density of the 3D integrated POL module is increased from 250W/in^3 to 350W/in^3.

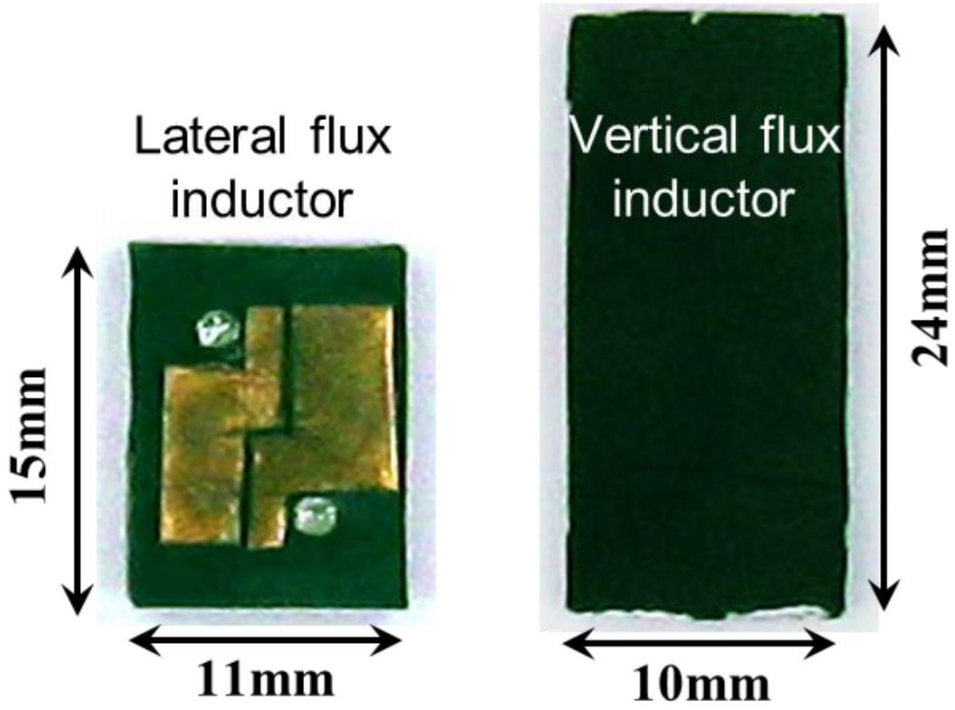


Figure 1.13. Prototypes comparison between the lateral flux inductor and vertical flux inductor [2].

The first three generations of modules developed by CPES use vertical flux planar LTCC inductors as the substrate. These are replaced by the lateral flux LTCC inductor in the fourth-generation product. The performance of the inductor substrate can be further improved by inverse coupling. The structure of a two-turn lateral flux

coupled inductor is illustrated in Figure 1.14. Two windings are embedded in one magnetic core, so their flux is magnetically coupled. With the marked current direction, inverse coupling between the two inductors is realized, which means the flux lines created by the currents in the different windings are in opposite directions. Compared with the non-coupled structure, the inverse coupled inductor has two unique benefits. First, the equivalent transient inductance, which impacts the transient speed of the converter, becomes smaller than the equivalent steady state inductance, which determines the steady state current ripple of the converter. Thus high efficiency and a fast transient can be achieved simultaneously [20]. Secondly, most of the DC flux in the core is cancelled by the inverse coupling. Therefore, the magnetic core of the inverse coupled inductor is operated at a much lower DC bias than the non-coupled inductor. Since the incremental permeability of LTCC ferrite is increased as the bias is decreased, the core volume of the inverse coupled inductor can be further reduced due to its larger permeability. With the proposed lateral flux structure, the power density of the fifth-generation POL module at CPES reaches 700W/in^3 with 40A output current.

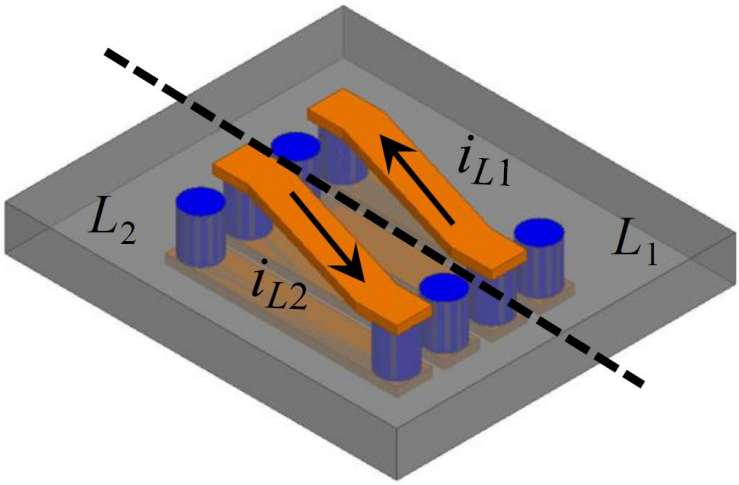


Figure 1.14. Two-phase invers coupled inductors with a lateral flux pattern [2].

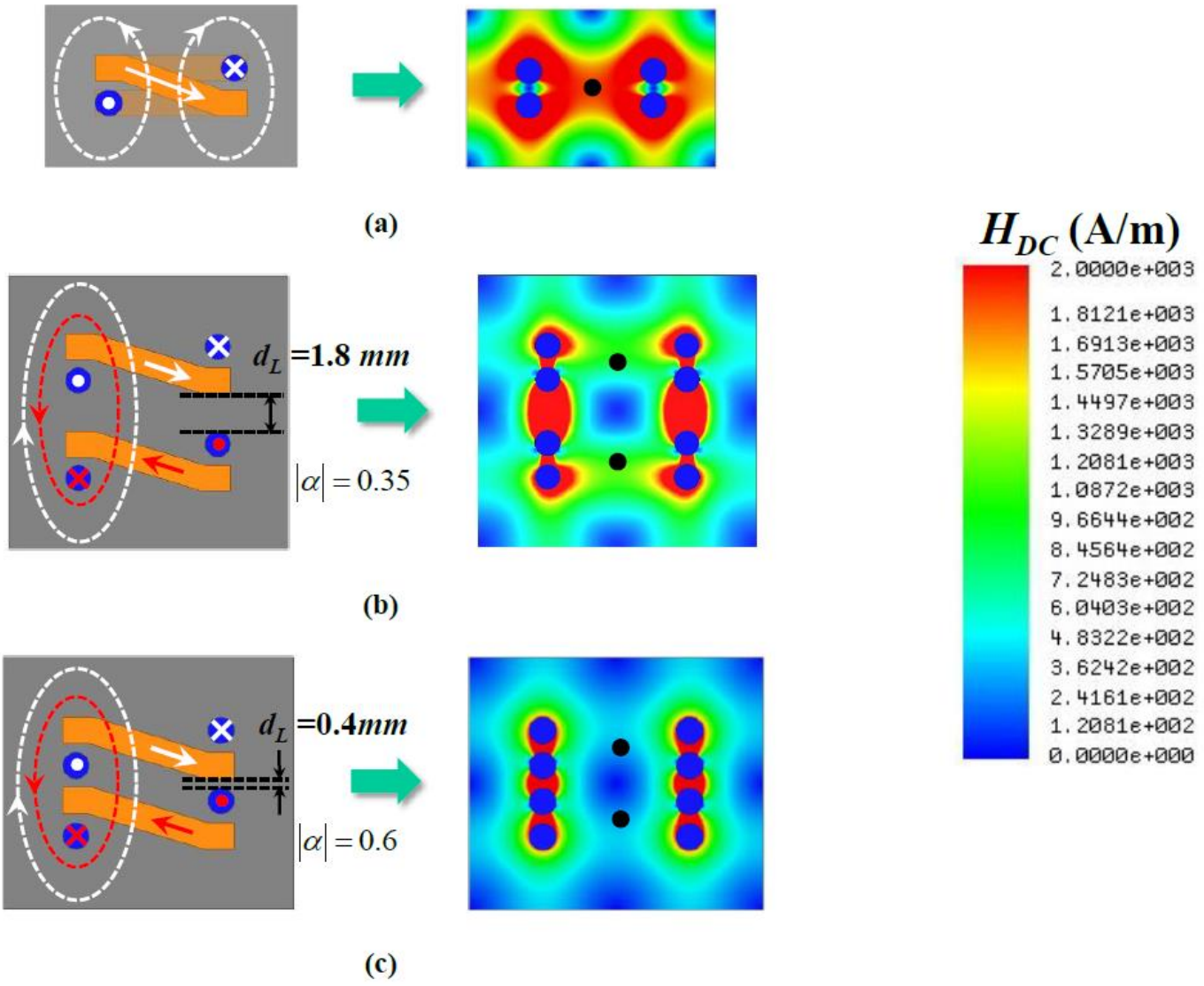


Figure 1.15. DC flux distribution of the lateral flux LTCC inductor with 10A current in each phase: (a) non-coupled; (b) inverse coupled with $|\alpha|$ = 0.3 and d_L=1.6 mm; (c)inverse coupled with $|\alpha|$ = 0.5 and d_L=0.4 mm.

Figure 1.15(a) shows the DC flux distribution of a single-phase non-coupled inductor with a 10A DC bias current. It can be seen that the H_{DC} value of the majority of the core is very large. Using the typical area in the center of the core marked by a black dot as the example, its operating point is at a DC bias higher than 2000A/m.

If two single-phase inductors are inversely coupled together with a 0.3 coupling coefficient and the DC bias current in each phase is still kept as 10A, the DC operating point of the core at the same marked point can be reduced to around 1000A/m, as shown in Figure 1.15 (b). The coupling is enhanced by decreasing the distance between two inductors (i.e. d_L). Figure 1.15 (c) illustrates that the coupling coefficient is increased to 0.5 with d_L=0.4*mm*, which causes the DC operating point of the core at the black dot point to be reduced to several hundred A/m. In Figure 1.15, the solid line is the direction of the inductor current and the dash line represents the flux line in the core. Because of the nonlinear B-H curve of the LTCC ferrite 40010[21], the incremental permeability is continuously increased as the coupling is enhanced, namely the DC bias in the core is decreased.

The LTCC coupled inductor is fabricated as shown in Figure 1.16. The two-phase 3D integrated POL module built with IR's GaN and LTCC coupled inductor is shown in Figure 1.17, whose power density achieves as high as 900W/in^3.

Figure 1.16. Fabricated lateral flux coupled inductor substrate for 4 MHz POL module.

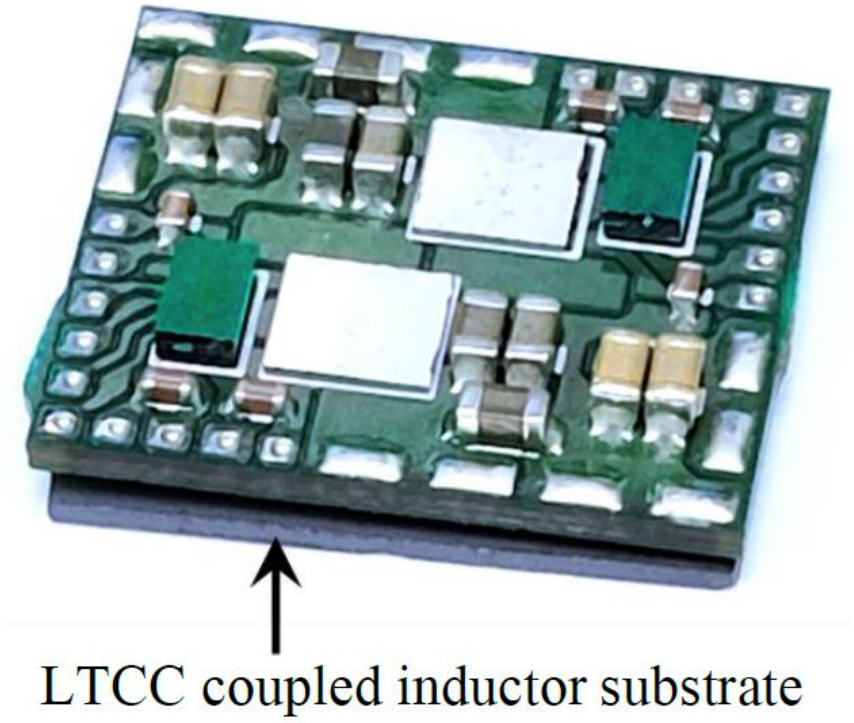


Figure 1.17. Two-phase 3D integrated POL module with IR's GaN and LTCC coupled inductor substrate.

To further improve the inductance density and make the 3D integration technology more standard and cost-effective, a metal-based flake magnetic material made by NEC-Tokin is introduced and the low profile inductor is embedded in the PCB to build the 3D integrated POL module[1]. The multi-layer PCB structure with embedded flake core is shown in Figure 1.18. The top and bottom layers are two C-stage fully cured laminates. The middle layer is the NEC flake magnetic core surrounded by a C-stage laminate. The B-stage prepregs are inserted between each layer, which can be molten to adhere different layers under heat and pressure.

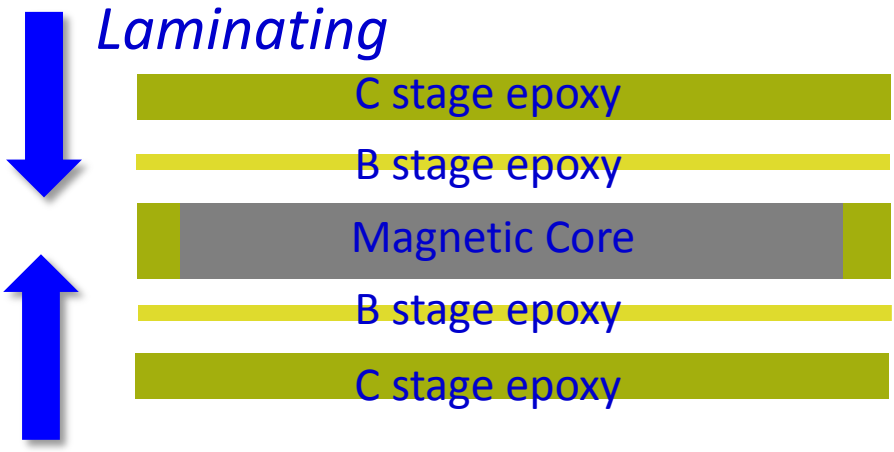


Figure 1.18. Laminating structure of PCB with embedded metal flake composite core.

The low profile inductor substrate with lateral flux pattern can fully utilize the superiority of the NEC flake composite, since the flake is laterally aligned. Following the similar structures of lateral flux LTCC inductor substrates shown in Figure 1.10, the lateral flux PCB inductor substrates with embedded NEC flake core are proposed as Figure 1.19. The NEC flake plate is sandwiched into FR4 epoxy. The copper layers are etched to form the surface winding of the inductor. The vias made of a co-fired silver paste in LTCC inductors are now replaced by conventional PCB vias.

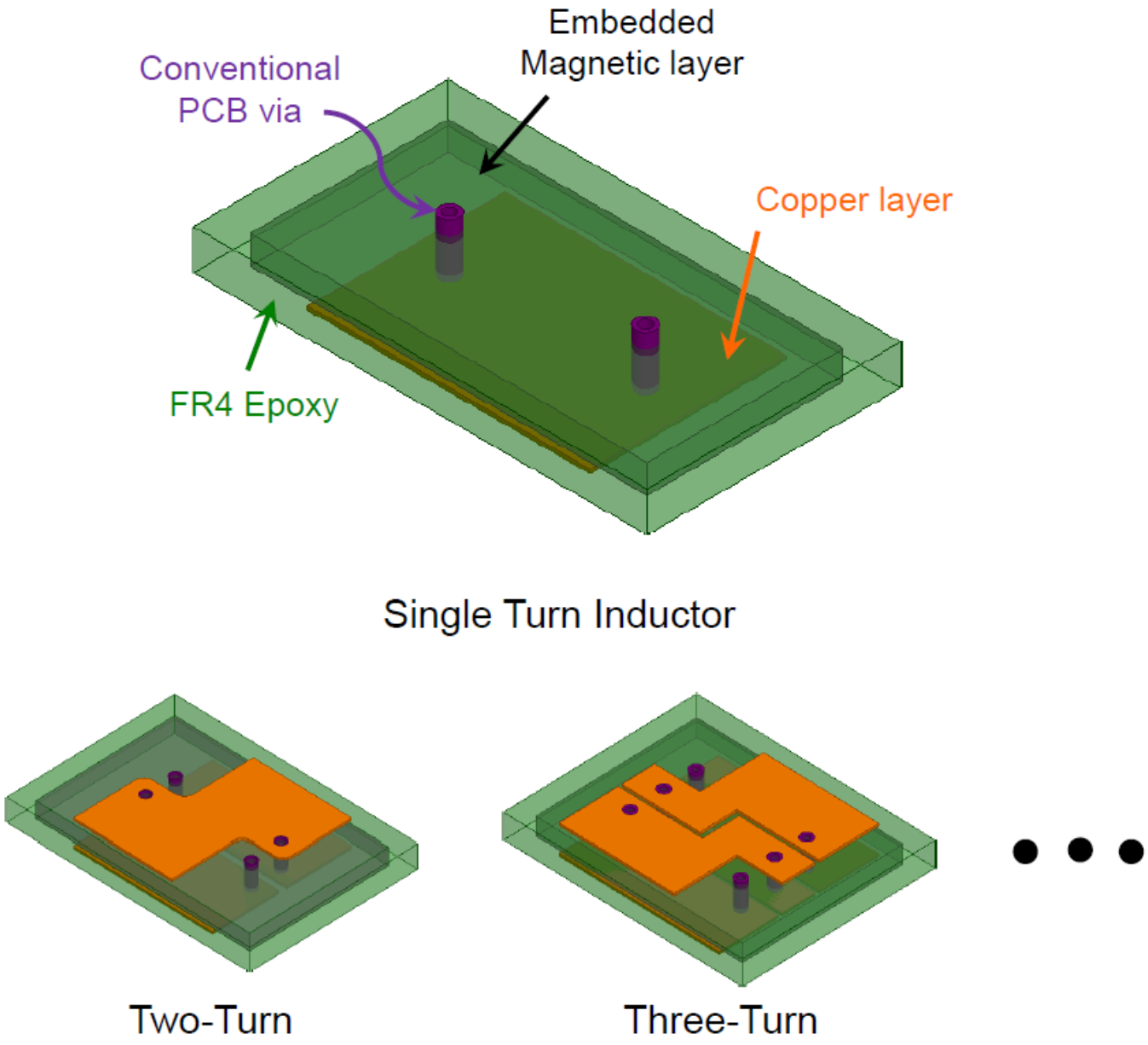


Figure 1.19. Lateral flux PCB inductor substrate with embedded NEC flake composite core.

In order to implement the PCB vias through the embedded core, the conventional process has to be modified slightly. As illustrated in Figure 1.20, the 2-layer PCB with embedded core is drilled with a larger hole size and then the hole is filled with the FR4 epoxy. The second drilling is done with a smaller hole size resulting in some FR4 epoxy left on the inside wall of the through via. Finally, the copper is electroplated onto the FR4 to connect the top and bottom surface windings.

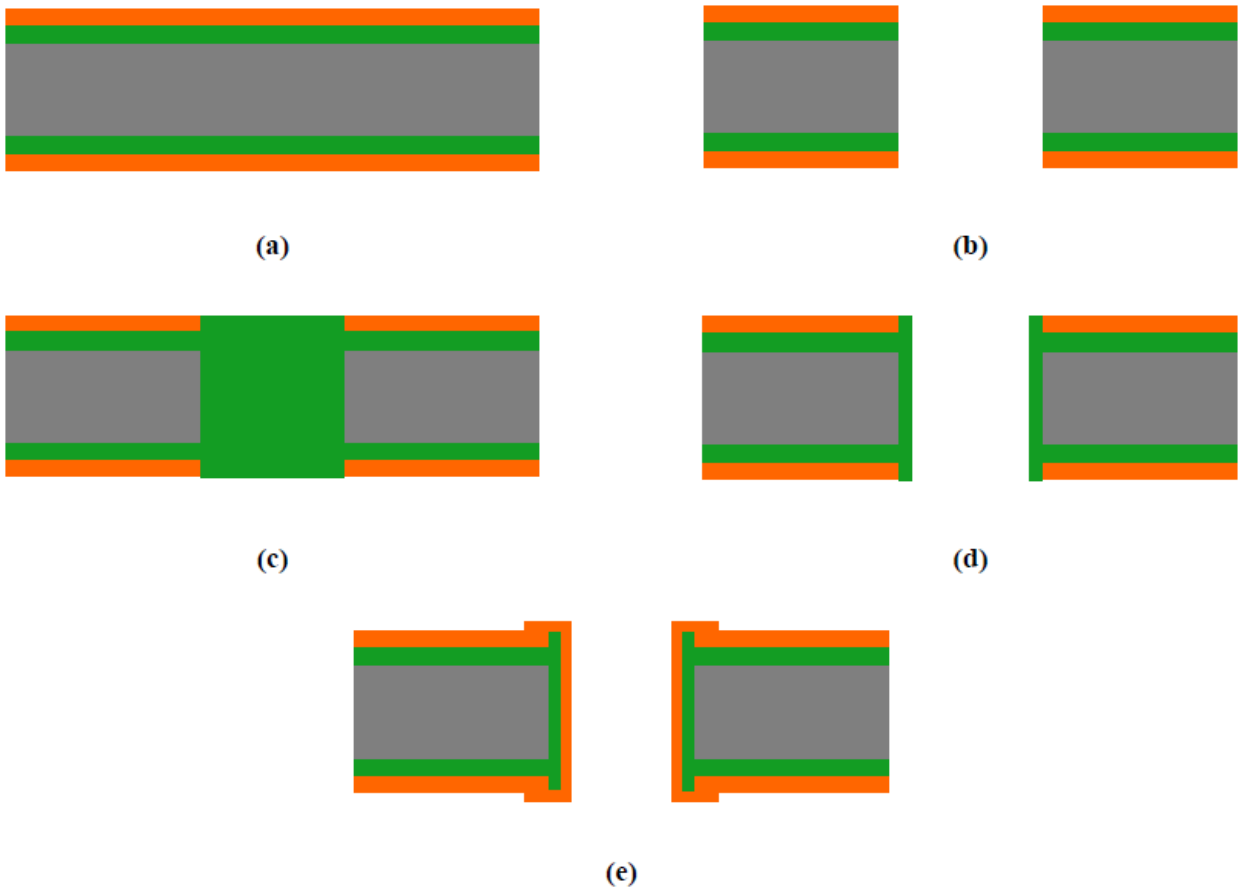


Figure 1.20. The fabrication process of the vias through PCBs with embedded core: (a) 2-layer PCB with embedded core, (b) first drilling with larger hole size, (c) filling epoxy into the hole, (d) second drilling with smaller hole size, (c) electroplating copper to form the via.

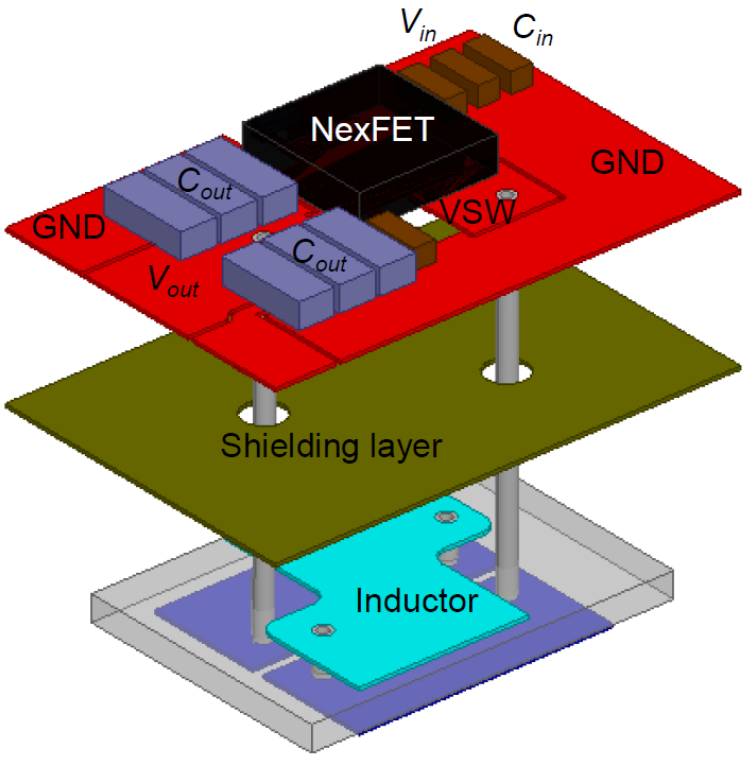
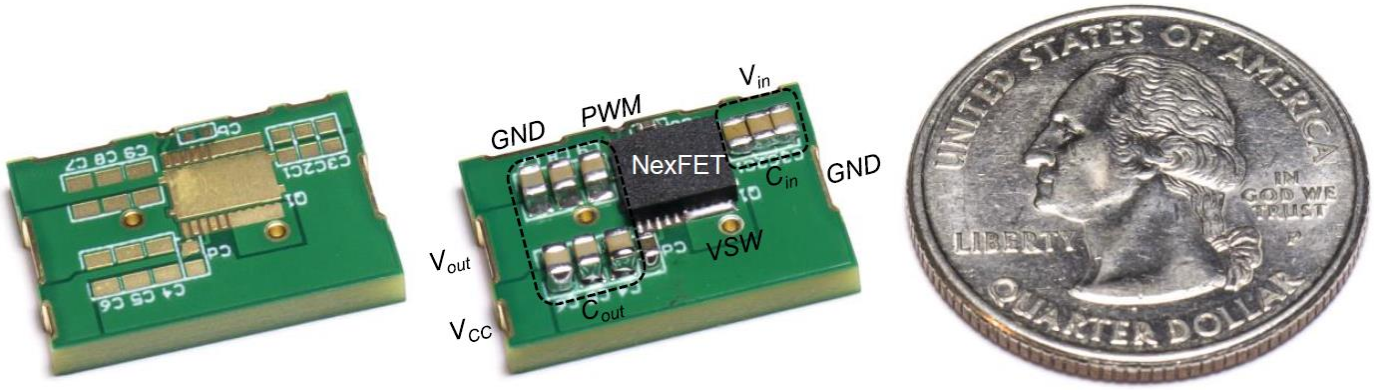


Figure 1.21. The expanded view of the 4-layer PCB structure for the 3D integrated POL module with embedded core.

The layout of the four-layer PCB with embedded core is illustrated in Figure 1.21. In this drawing, the multi-layer laminated structure is expanded and the distance between each layer is enlarged intentionally, so that the function of each layer is shown clearly. The input capacitors should be placed as close as possible to the IC chip, in order to reduce the parasitics introduced by the PCB trace. All of the components except the inductor are placed on the top layer, which is shown in the color red. The switching node point (VSW) and the output point (V_{out}) at the top layer are connected to the lower surface winding of the inductor at the bottom layer by two through plated vias. The upper surface winding of the inductor at the third layer is connected to the lower surface winding at the bottom layer by two blind vias. The NEC flake core is embedded between the third layer and the bottom layer.



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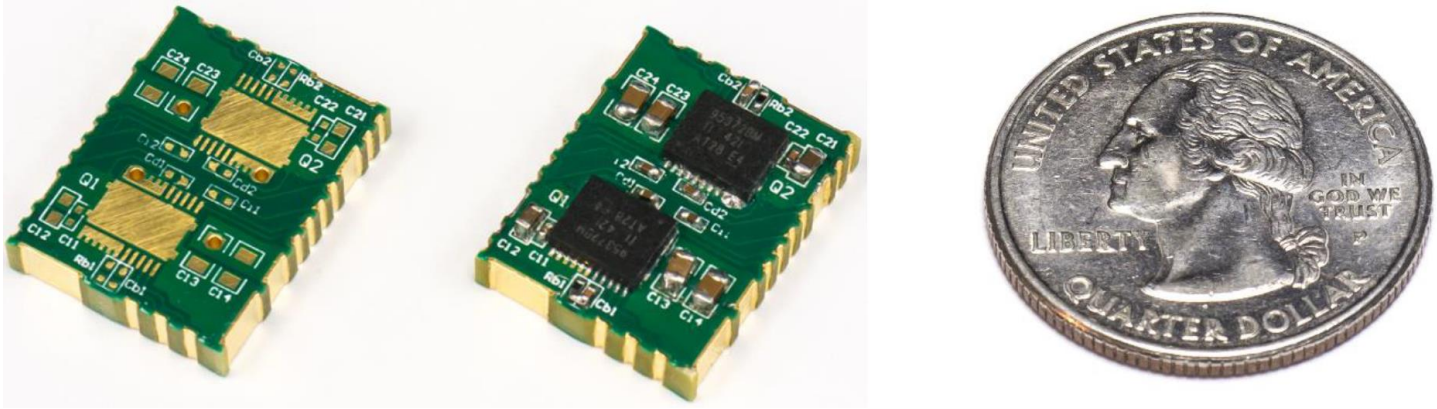


(b)

Figure 1.22. Prototype of Single-phase (a) and two-phase coupled (b) PCB integrated POL Module.

The prototype of the single-phase and two-phase coupled PCB integrated POL module is shown in Figure 1.22 (a) and Figure 1.22 (b), respectively. In each of the pictures the left hand side is the 4-layer PCB substrate with embedded core and the right hand side is the PCB substrate with the other components mounted. The 2oz copper is used for the first active layer and the second shielding layer, while the 4oz copper is employed for the third and fourth layers to decrease the resistance of the inductor winding.

Despite the achievement mentioned above, there are still several points that need to be improved in the 3D integrated POL module. First of all, the DC resistance (DCR) of the PCB integrated inductor is quite large and results in a significant efficiency drop. Due to the limitation of the copper thickness in the PCB trace and vias, the two-phase coupled PCB integrated inductor has a 4.3mΩ DCR for each phase, which leads to a more than 4% efficiency drop at full load condition. Secondly, further footprint reduction can be achieved significantly for the POL module with vertical mounting design. Thirdly, the non-linear inductance of the inverse coupled inductor can be further optimized using a composite magnetic core material to achieve a higher inductance density, better efficiency and dynamic balance, and a more effectively confined magnetic stray flux. Chapter 2 will address each of the three aspects and illustrates the improvements in detail.

1.2. Very high frequency integrated voltage regulator (IVR) for Intel's processors

The IT industry has grown rapidly in the last three decades. The microprocessors, which are also known as the central processing unit or CPU, are the key component in most of the applications such as computer systems and portable devices. To achieve better performance, more transistors are being integrated into the microprocessor.

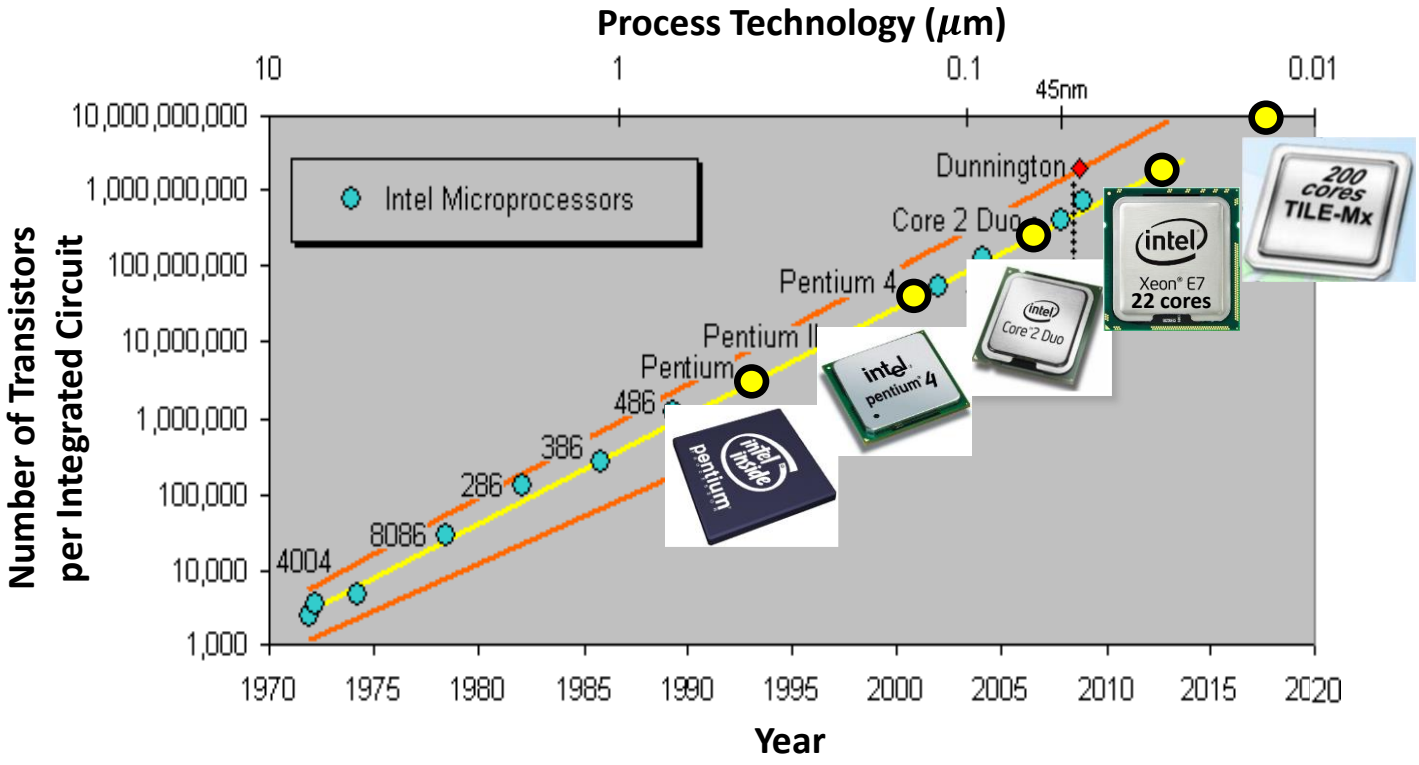


Figure 1.23. Roadmap of Intel microprocessors.

Figure 1.23 shows the CPU integrated transistor counts against the dates of introduction. The yellow line is the exponential growth with transistor counts doubling every two years, which is known as the Moore's law. Since the introduction of the high performance Pentium series CPU in the middle of 90s, Intel is able to follow Moore's law up to 4th generation of Pentium processor. However, after that point, the large energy consumption

of the processor places a "power wall" that stops the processor development from following Moore's law. To break the power wall and allow Moore's law to continuously prevail, Intel proposes multicore processors to improve the CPU performance while keeping energy consumption the same. From that points on, the multicore processors takes over and the processor core number continuously increases from 2 to 4, to 8, to 22, etc. It is even exciting that Tilera Corp., another CPU manufacturer, announced that they are developing 200 cores processor in one chip.

When powering multiple processor cores, as demonstrated in Figure 1.24, the energy consumption can be reduced dramatically if the supply voltage can be modulated rapidly based on the power demand of each core by dynamic voltage and frequency scaling (DVFS)[22-25]. However, traditional discrete voltage regulators (VRs) are not able to realize the full potential of DVFS since they are not able to modulate the supply voltage fast enough due to their relatively low switching frequency and the high parasitic interconnect impedance between the VRs and the processors. With these discrete VRs, DVFS has only been applied at a coarse timescale, which can scale voltage levels only in tens of microseconds (which is normally called a coarse-grained DVFS). In order to get the full benefit of DVFS, a concept of the integrated voltage regulator (IVR) is proposed to allow fine-grained DVFS to scale voltage levels in less than a microsecond [26, 27]. Significant interest from both academia and industry has been drawn to IVR research [28-33].

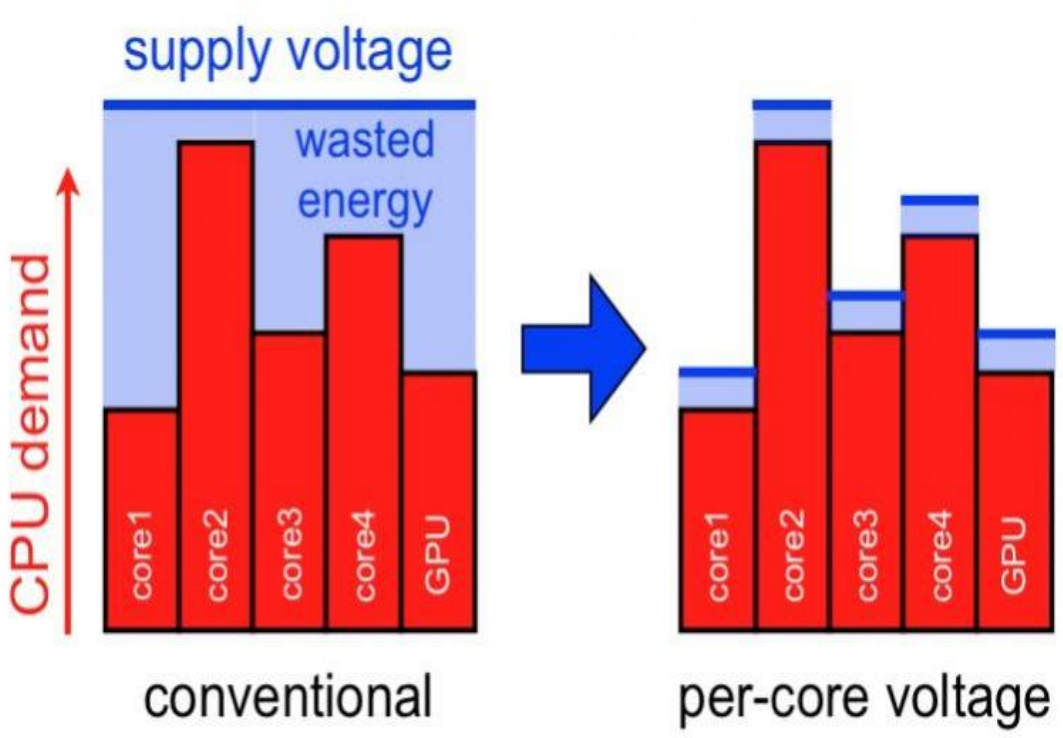


Figure 1.24. Energy saving by dynamic voltage scaling.

Recently, Intel has implemented two generations of very high frequency IVR. The first generation is implemented in Haswell processors[28] (Figure 1.25), where air core inductors are integrated in the processor's packaging substrate and placed very closely to the processor die[4]. The air core inductors have very limited ability in confining the high frequency magnetic flux noise generated by the very high switching frequency of 140MHz. In the second generation in Broadwell processors[29] (Figure 1.26), the inductors are moved out from the processor substrate to the 3DL PCB modules in the motherboard level under the die.

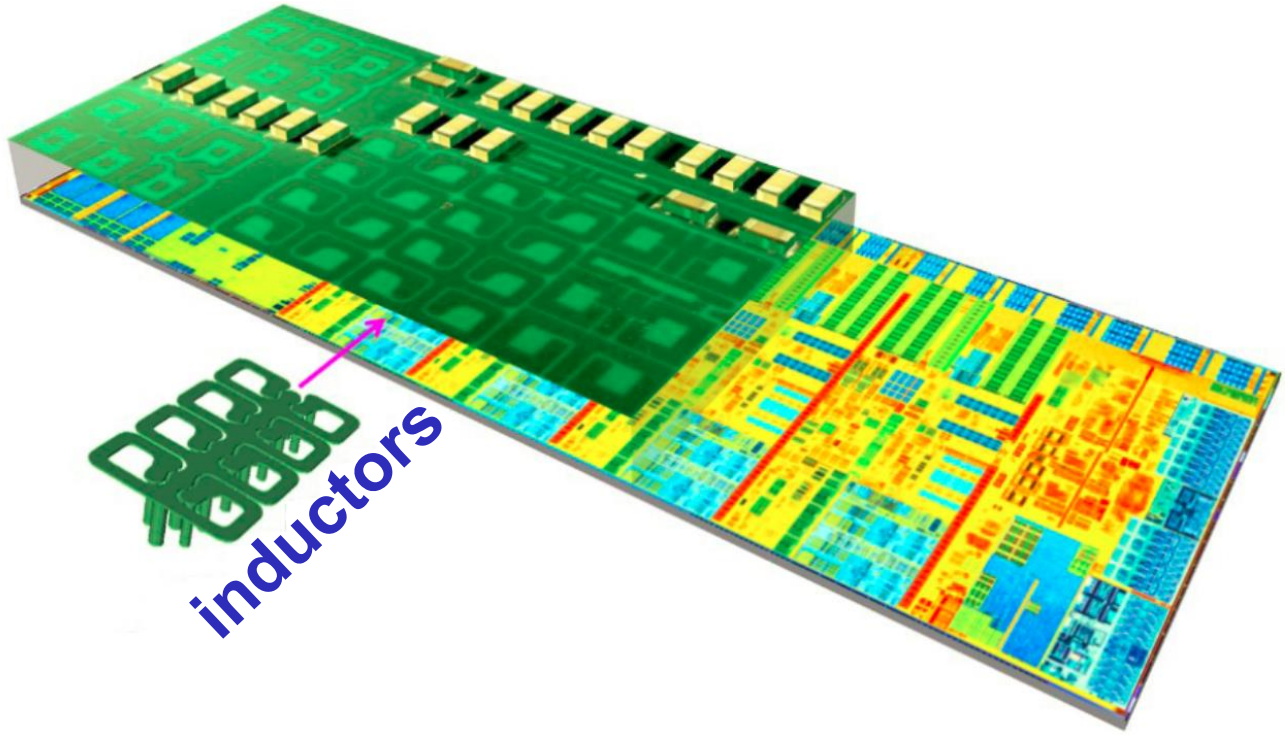


Figure 1.25. Intel's first-generation IVR structure for Haswell processors[28].

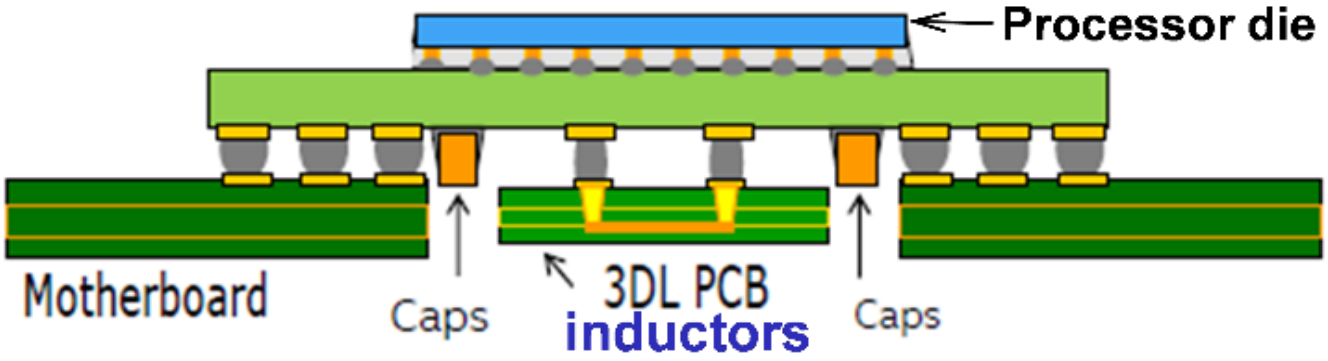


Figure 1.26. Intel's second-generation IVR structure for Broadwell processors[29].

1.3. Proposed integrated voltage regulator for smartphone processor with 3D integrated magnetics

In addition to computers, small portable electronics such as smartphones are another application that can be greatly helped by IVRs. The smartphone market size is now larger than 400 billion US dollars, and its power consumption is becoming higher and higher as the functionality of smartphones continuously advances. Today's multi-phase VR for smartphone processors is built with a power management integrated circuit (PMIC) with discrete inductors. Today's smartphone VRs operate at 2-8MHz, but the discrete inductor is still bulky, and the VR is not close enough to the processor to support fine-grained DVFS. If the IVR solution can be extended to the smartphone platform, not only can the battery life be greatly improved, but the total power consumption of the smartphone (and associated charging time and charging safety issues) can also be significantly reduced. Intel's IVR may be a viable solution for computing applications, but the air core inductor with un-confined high-frequency magnetic flux would cause very severe problems for smartphones, which have even less of a space budget. The thickness of a typical smartphone processor SOC is around 0.5mm-0.6mm, which is at least five times thinner than a typical server CPU. In such a small space, the fringing flux from the air core inductor could generates remarkable radiation EMI to interfere with the processor's die when the inductor and die are placed very closely to each other. In this research, we propose a three-dimensional (3D) integrated voltage regulator (IVR) structure for smartphone platforms. The proposed 3D IVR will operate with a frequency of tens of MHz. Instead of using an air core, a high-frequency magnetic core without an air gap is applied to confine the very high frequency flux. The inductor is designed with an ultra-low profile and small footprint to fit the stringent space requirement of smartphones.

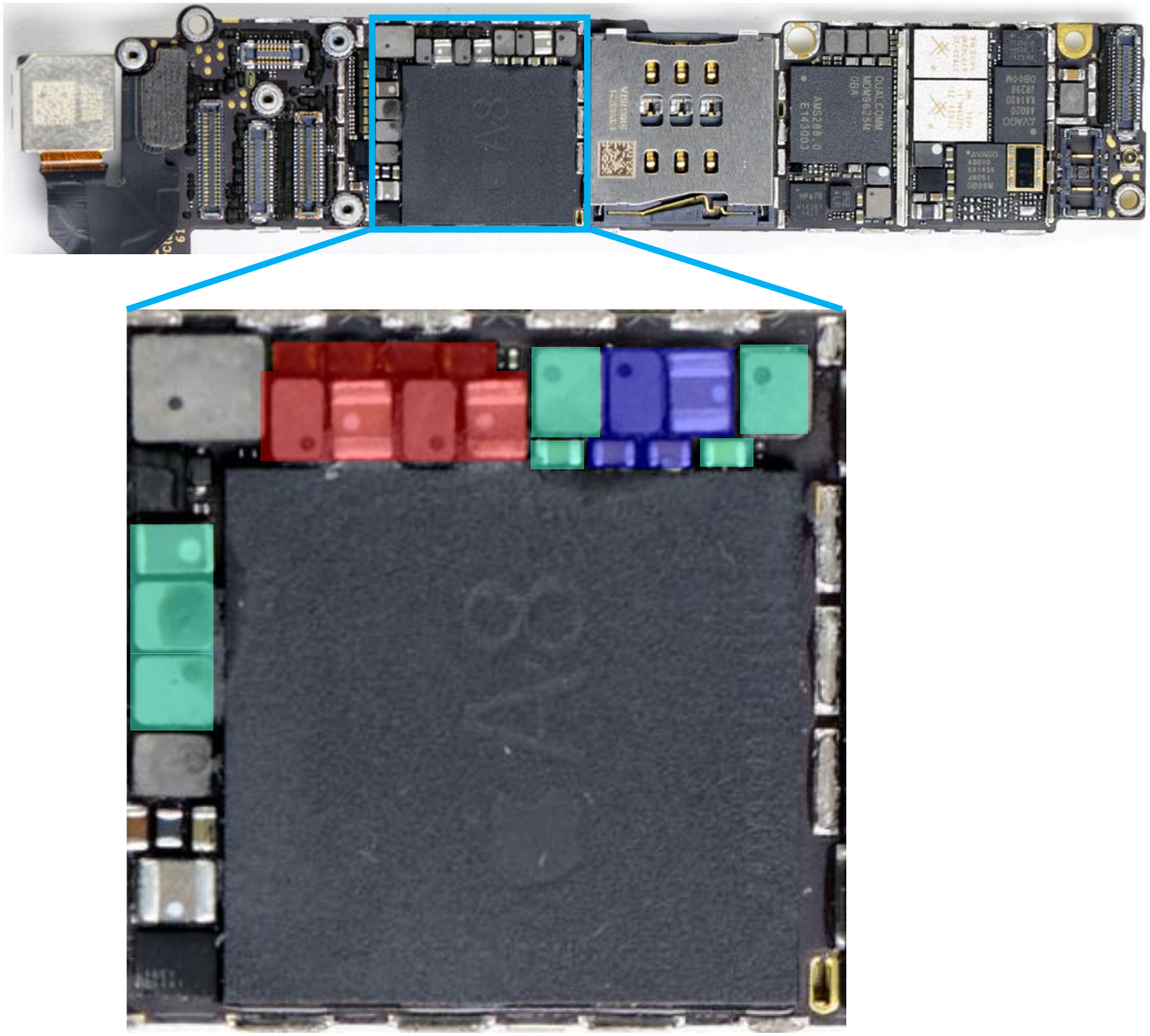
The numerous techniques available for inductor integration can be classified into the categories of either wafer-level integration [12, 13, 32-59] or package-level integration [4, 5, 10, 15, 17, 28, 60-81]. The wafer-level

integration is primarily based on inductor-on-silicon technology and package-level integration is primarily based on embedded inductor technology. The wafer-level integration usually has a higher current density, while the package-level integration usually has a higher current handling ability because a thicker inductor is much easier to be accommodated in the package-level integration. For wafer-level integration, the inductor is built with a semiconductor die and its current level is generally lower than 1A per phase. However, the total peak current of different power domains in today's smartphone SOC can reach 30A, and consumption is becoming higher and higher as the functionality of smartphones continuously advances. The limited current-handling capability of the wafer-level integrated inductor will require many phases to build the IVR, which will complicate the system design. For package-level integration, the magnetic component is co-packaged with the semiconductor die or used as a platform/substrate for the semiconductor device, and it can have a higher current-handling capability than the wafer-level integration. The inductor made with magnetic materials (carbonyl-iron/epoxy composite) working with both very high frequency (100MHz) and high current-handling capability (5.5A) is reported in [78], whereas a complicated multi-turn racetrack-type winding structure is used in this inductor, which causes a large winding DCR (18mΩ). In order to design a package-level integrated inductor to handle a relatively large current with a small winding DCR, this work adopts the special lateral flux inductor structure demonstrated in section 1.1 [82]. As revealed in previous work [82], the inductance density of the lateral flux inductor is independent of the core thickness, which makes it very suitable for low-profile inductor design. The proposed inductor structure in this work has a small winding DCR due to its simple winding structure. The lateral flux inductor structure also has a special non-uniform flux distribution that generates a very unique AC-DC flux auto-balance effect, which allows not only better utilization of the inner part of the core with a light load, but also allows for safe operation with partial saturation of the inner part of the core with a heavy load [83].

For a 3D IVR, since inductors will serve as the substrate for the active device, it's better to integrate all the inductors into a single magnetic core to simplify the manufacturing process. However, all of the previous inductor integration work demonstrates only up to two-phase inductor integration within one magnetic core. For example, two-phase coupled inductor integrations are demonstrated in [65, 68, 75]; and 3-8 phase coupled inductors based on a 1-to-1 coupling mechanism are reported in [32, 53, 54], However, these multi-phase inductors are not integrated on a single magnetic core (for example, the eight-phase coupled inductor is implemented with eight sets of magnetic cores [32]). In this work, we demonstrate an extension of the lateral flux inductor technology, raising the switching frequency from today's 1-5MHz[66, 68, 75] to 20-30MHz, achieving <0.1mΩ winding DCR, providing 3A per phase current-handling ability, and realizing >5 phase integration within one magnetic core.

Figure 1.27 (a) and (b) show the voltage regulator in an iPhone 6 motherboard. The red shaded areas indicate the output inductors and capacitors of a four-phase buck converter to power a dual-core CPU; the blue shaded areas indicate the output inductors and capacitors of a two-phase buck converter to power a quad-core GPU; and the green shaded areas represent some other functions such as the DDR, charger, vibrate driver, *etc*. The processor is placed on the front side of the motherboard, and the PMIC is placed on the back side of the motherboard. It can be seen that the passive components occupy a great deal of the footprint. With the 3D integrated structure proposed in this work, about half of the total footprint occupation of the voltage regulator can be saved, as illustrated in Figure 1.27 (c). The number of the capacitors can be significantly reduced at very high frequency due to the high bandwidth of the converter[84]. The thickness of the inductor is designed to be smaller than 0.5mm to fulfill the profile requirement of the smartphone (~1mm allowance for electronics on the motherboard). The design details will be illustrated in chapter 4. It is also worth noting that a bigger inductor thickness could be

applicable (or a more stringent thickness requirement could be fulfilled) if the inductor core can be embedded or partially embedded in the motherboard.



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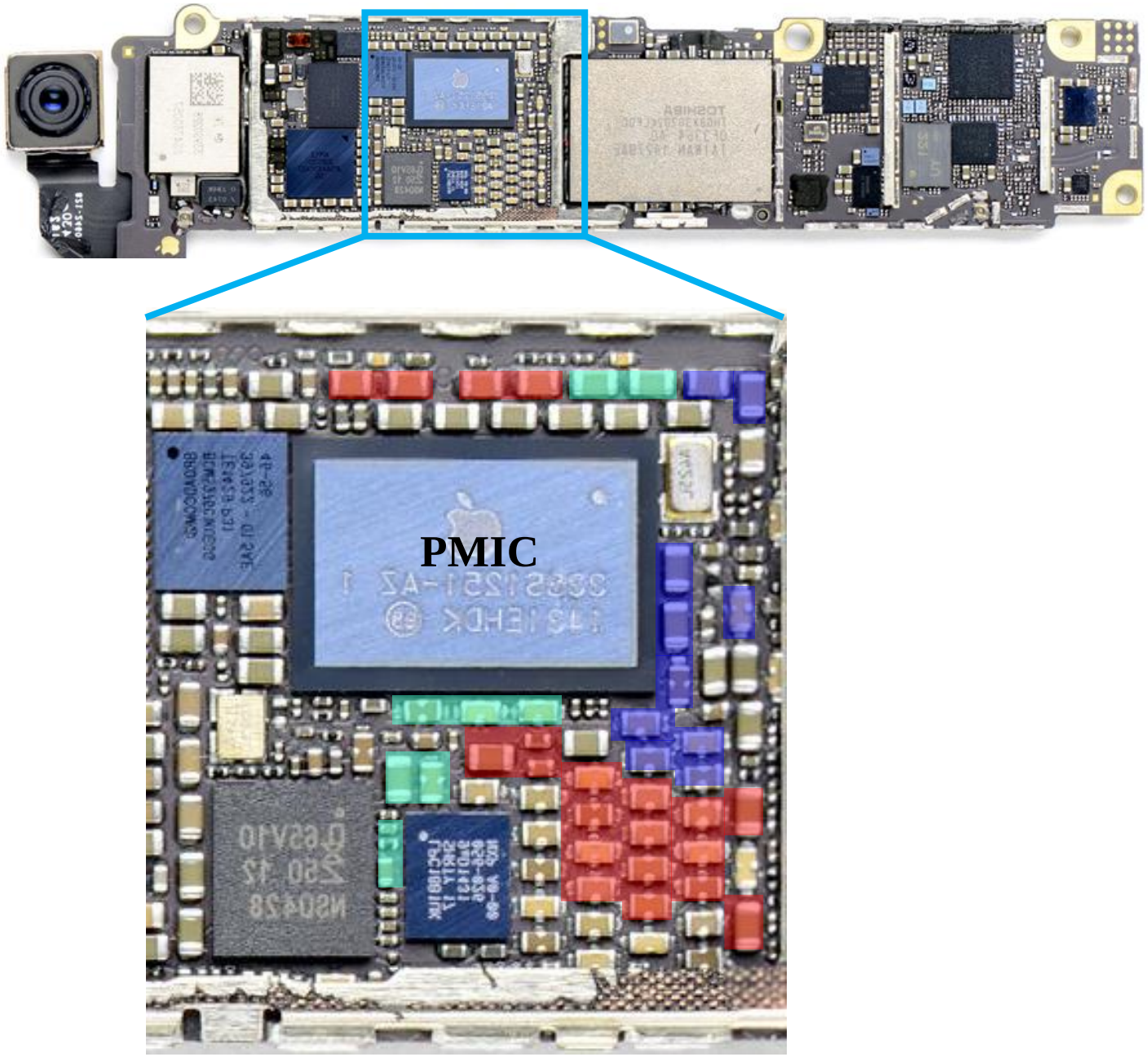

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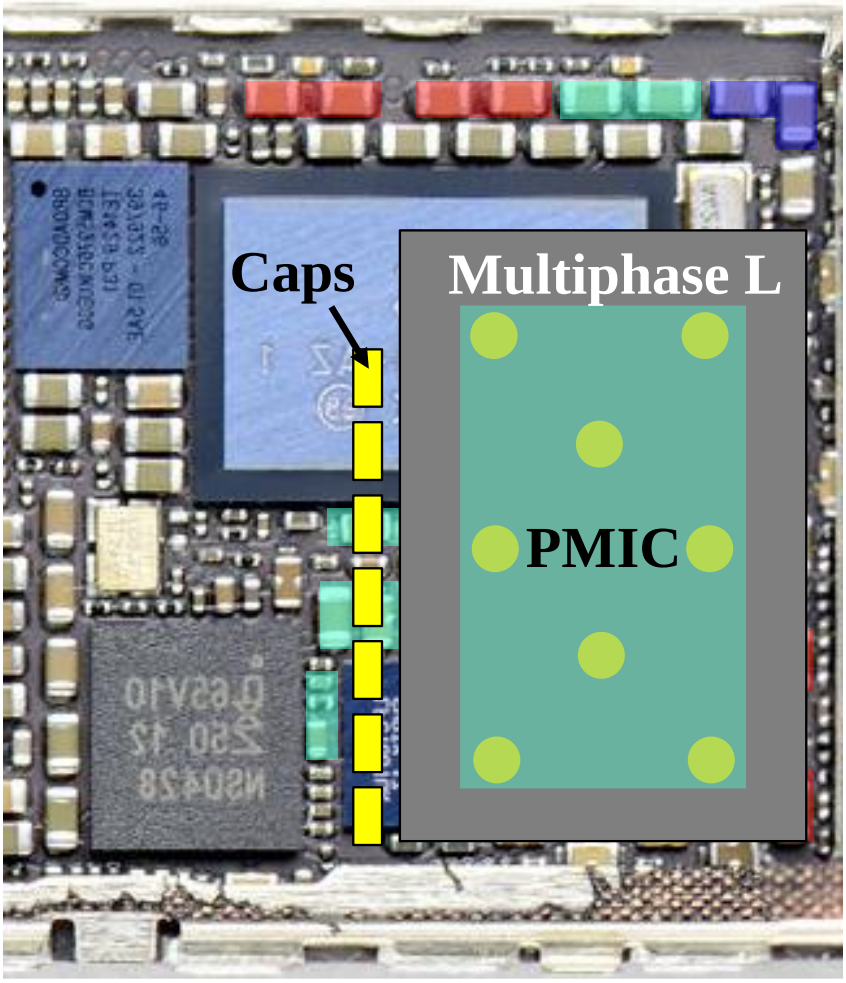


(c)

Figure 1.27. iPhone 6 motherboard. (a): Front view; (b): Back view; (c): Back view with proposed multi-phase integrated inductor (each via serves as a single-phase inductor) in a 3D stacked structure with the PMIC on top.

A unique magnetic structure is adopted to implement a single-core multi-phase inductor, which will serve as a substrate and be stacked with the PMIC to realize 3D integration. The system schematic is illustrated in Figure 1.28, in which the multiphase buck topology is chosen for the voltage regulator for the following reasons: 1) the buck converter is the dominant topology used in low-voltage step-down converters mainly due to its simplicity

and high efficiency compared to linear regulators; 2) the multi-phase interleaved buck converter can provide extra benefits of current ripple cancellation (and thus reduces the voltage ripple as well) at the output node[85]. Due to the help of magnetic materials and 3D integration, this very high frequency multi-phase VR will be small enough to be put right below the processor to support DVFS, as shown in Figure 1.29. Since the inductor is at the output terminal of the buck converter, the inductor location is more important than the active devices' location in determining the output voltage scaling speed and capability. Although the proposed 3D IVR has active devices outside the processor, the inductor is still very close to the processor. Its location is almost the same as that of the inductor module used in Intel's second-generation IVR for Broadwell (refer to Figure 1.26[29]).

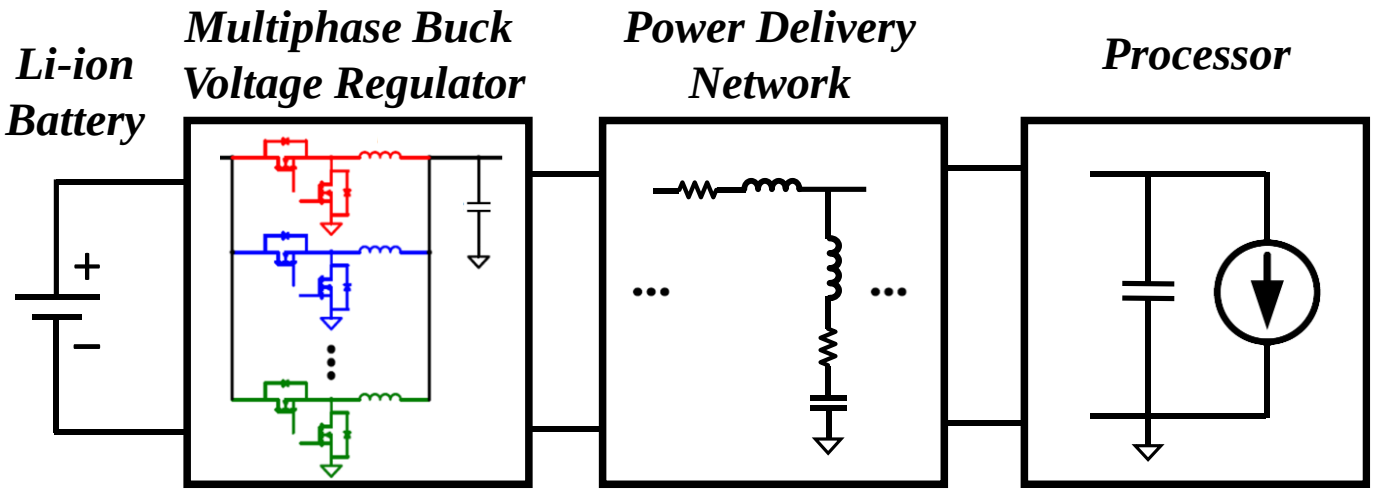


Figure 1.28. Schematic architecture of the voltage regulator system for smartphone processor.

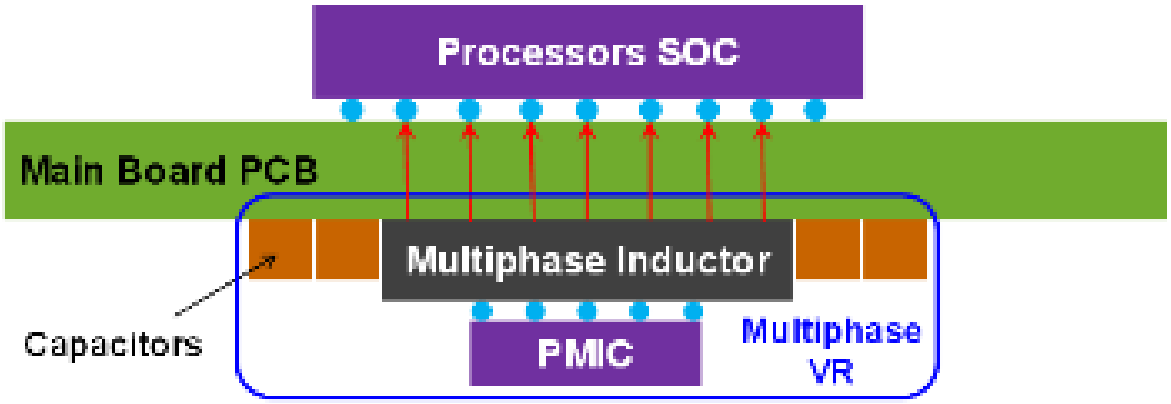


Figure 1.29. Proposed 3D IVR architecture for smartphone processors.

As mentioned before, Dynamic voltage/frequency scaling (DVFS) can save significant amount of processor energy by adjusting the operating voltage and frequency of the processor according to its instantaneous power requirement. A 15%-75% energy saving can be achieved with 5%~20% performance loss for the Xscale CPU [86]. Another example for a mobile CPU shows that a 23%-75% energy saving can be achieved with a 1-15% performance loss[25].

The other factor that impacts the energy saving ability of DVFS is the voltage scaling ability determined by the voltage regulator that powers the CPU. The higher the voltage scaling ability, the faster the DVFS can be performed to follow the instantaneous change of power demand from CPU, and thus can save more CPU energy. The voltage scaling ability is determined by the voltage regulator that powers the CPU, and generally speaking, the higher the switching frequency of a voltage regulator, the higher the voltage scaling ability it can offer. An example for a mobile CPU is presented by [27], in which the average normalized energy consumption of CPU and voltage regulator with respect to different voltage scaling ability is summarized in Figure 1.30. For the case with no DVFS (red curve), the higher energy consumption at a higher voltage scaling speed is caused by the higher loss of the voltage regulator running at a higher switching frequency. For the case with high frequency

DVFS (blue curve), the total energy consumption of the CPU and the VR decreases first and then slightly increases. These two curves can be combined together to extract the CPU energy saving by DVFS. For example, at the voltage scaling speed of 10mV/ns, 2% excessive energy is consumed by the VR, while a 15% overall energy savings is achieved. So as a summation, the CPU energy saving by DVFS is 17%.

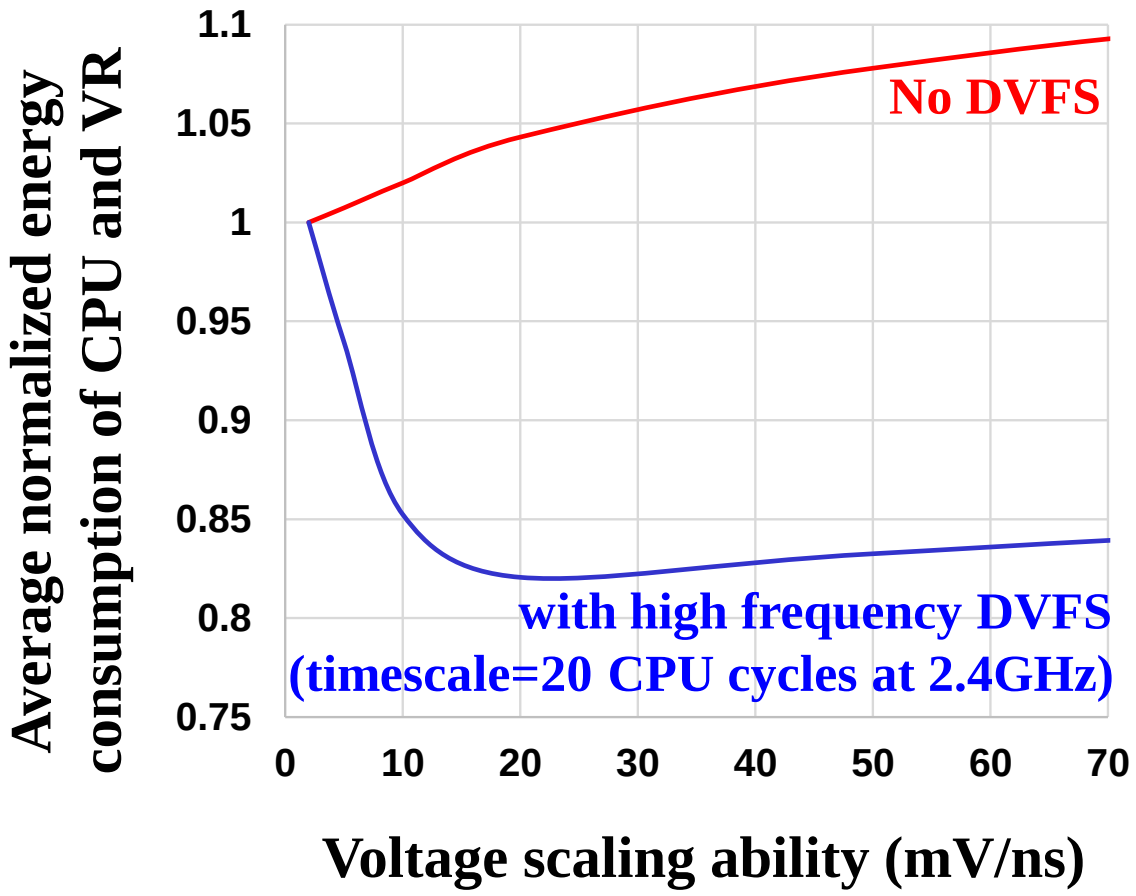


Figure 1.30. Average normalized total energy consumption of CPU and VR at different voltage scaling speed. The red curve shows the case with no DVFS, and the blue curve shows the case with high frequency DVFS[27].

The results at different voltage scaling speeds are summarized in Figure 1.31. It shows that the energy saving ability of DVFS increases very rapidly first, and then the increasing rate gradually slows down to a much lower value, like a saturation phenomenon. The blue dotted line in Figure 1.31 shows that the fast and slow increase trend interchange at around 12mV/ns. Furthermore, an approximately linear relationship between the voltage scaling ability and the VR switching frequency can be found in the published works[25, 31, 87, 88]. The linear relationship can be ascribed to the higher bandwidth with higher switching frequency Fsw. According to the linear relationship, the voltage scaling speed of 12mV/ns corresponds to about 40MHz switching frequency. This indicates that increasing the VR switching frequency to 40 MHz is very effective for energy savings by DVFS.

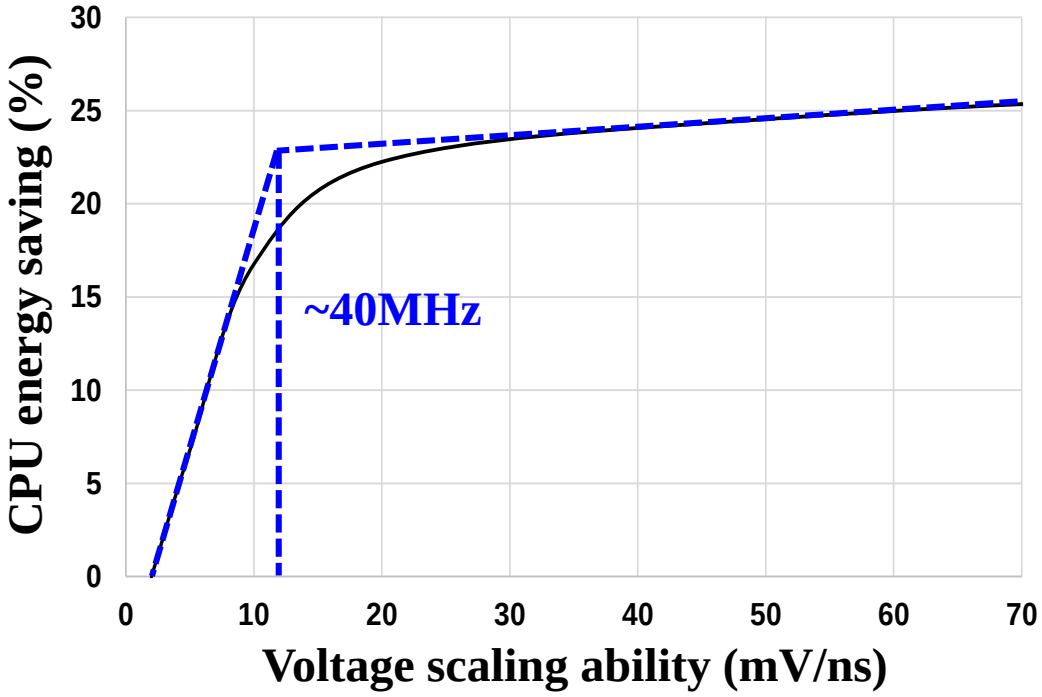


Figure 1.31. CPU energy saving respect to voltage scaling ability, and VR switching frequency (Fsw).

1.4. High frequency switching devices

Table 1.1 summaries the commercially available high frequency switching devices. It can be seen that several switching devices are capable of operating at multi-MHz, especially the SEMTECH's SC220 can switch at 20MHz and the EPC GaN device can operate at even higher frequencies. We will use these devices to build the IVR platform in chapter 4.

Table 1.1. Survey of commercially available high frequency switching devices

Manufacturer & Part #	Vin (V)	Vout (V)	Io_max	Phase #	Fsw
Dialog, DA 9063	1.5-5.5	0.3-3.3	12A	6	3MHz
TI, LP 8755	2.5-5	0.6-1.67	15A	6	4MHz
ADI, ADP 2121	2.7-5.5	1.8-2.3	0.6A	1	6MHz
ROHM, BU90002GWZ	3-5.5	3.3	1A	1	6 MHz
TOREX, XC9306B05G0R-G	2.5-5.5	0.8-5	1.2A	1	6MHz
MICREL, MIC 2285A	2.7-5.5	1-Vin	0.6A	1	8MHz
SEMTECH, SC220	2.7-5.5	1-Vin	0.65A	1	20MHz
LTC, LTC 3616	2.25-5.5	0.6-5.5	6A	1	<4MHz
MICREL, MIC 22205	2.9-5.5	0.7-Vin	2A	1	<4MHz
MAXIM, MAX 1536	3-5.5	0.7-Vin	3.6A	1	<1.4MHz
EPC, EPC 9036	<24	<Vin	25A	1	>10MHz

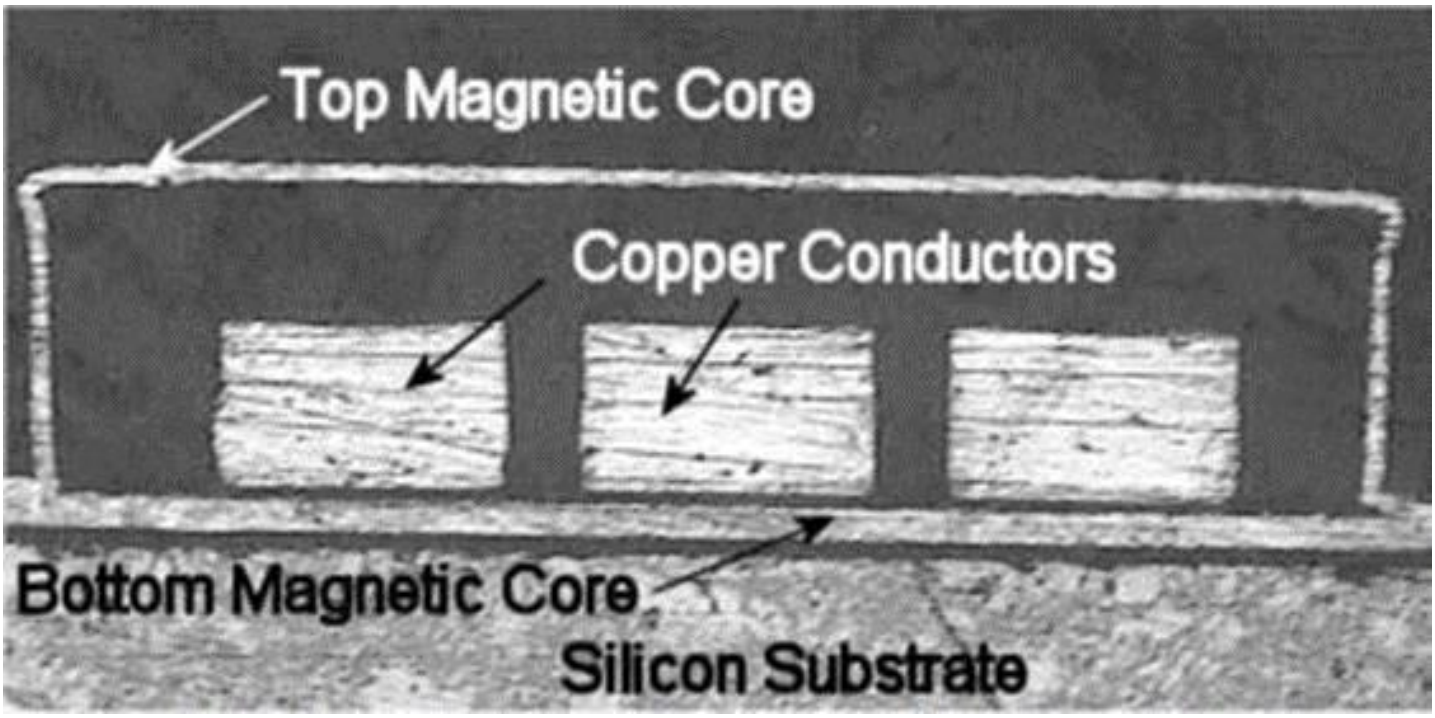
1.5. High frequency magnetic materials for integration

The survey of magnetic materials for high-frequency power conversions has been addressed in many publications [89-91]. The magnetic materials used for high-frequency (>1MHz) applications are usually composed of ceramic ferrites such as MnZn or NiZn ferrites. They usually have high permeability and high electrical resistivity as well as low loss, making them suitable for use at high frequencies. However, the ferrites need to be sintered at a very high temperature (>1400°C) to achieve the desired performance. Once sintered, the cores become too rigid and brittle to be suitable for magnetic integration.

On the other hand, magnetic powder cores, such as Kool Mμ and MPP from Magnetics Inc.[92], are usually made of metal or metallic alloys such as iron and permalloy and do not require a high temperature-sintering process. In addition, they are flexible enough to be fabricated into any core shapes for integration. However, they are electrically conductive and their applications are limited to low frequencies because of a dramatic increase in eddy current loss at higher frequencies, which increases much faster than the hysteresis loss. Many academic works have tried to modify the developing processes, with the aim to either improve the integrability of the ferrite core, or to reduce the high-frequency eddy current losses of the metal core.

Reference [89] reports a permalloy-polymer composite where the particles of the permalloy powder are coated with an insulating layer to reduce the eddy current loss in the MHz range of operation. A simple low-temperature solution based process is developed to coat magnetic powder with an insulating polymer dielectric. Compared with the commercial uncoated powder core, the core loss density of the composite with 84 vol% magnetic powder content at the multi-MHz can be reduced by 4 to 5 times. However, the polymer and coating material act as distributed air gaps, leading to relatively low equivalent permeability of the material.

The pure alloy magnetic materials can be utilized in the thin-film forms. To control its eddy current loss, the thickness of the thin film has to be reduced to the micrometer range. The alloy NiFe and CoNiFe thin films were first introduced for magnetic recording applications, then were later used for power conversion applications[10, 93, 94]. According to the measured data in [93], when the core thickness is reduced to 2.4μm, the CoNiFe core can have a core loss density as low as that of NiZn ferrite 4F1. The alloy thin films can be deposited on either the PCB[10] or the silicon[94] substrates by an electroplating process. Figure 1.32 show examples of the high-frequency integrated inductors on PCB and silicon substrates with electroplated NiFe core and spiral windings developed by Tyndall National Institute. The single layer NiFe cores are 5μm and 4.2μm, and are to be operated at 1MHz and 8MHz, respectively. The integrated inductors, however, are only capable of handling current lower than 500mA.



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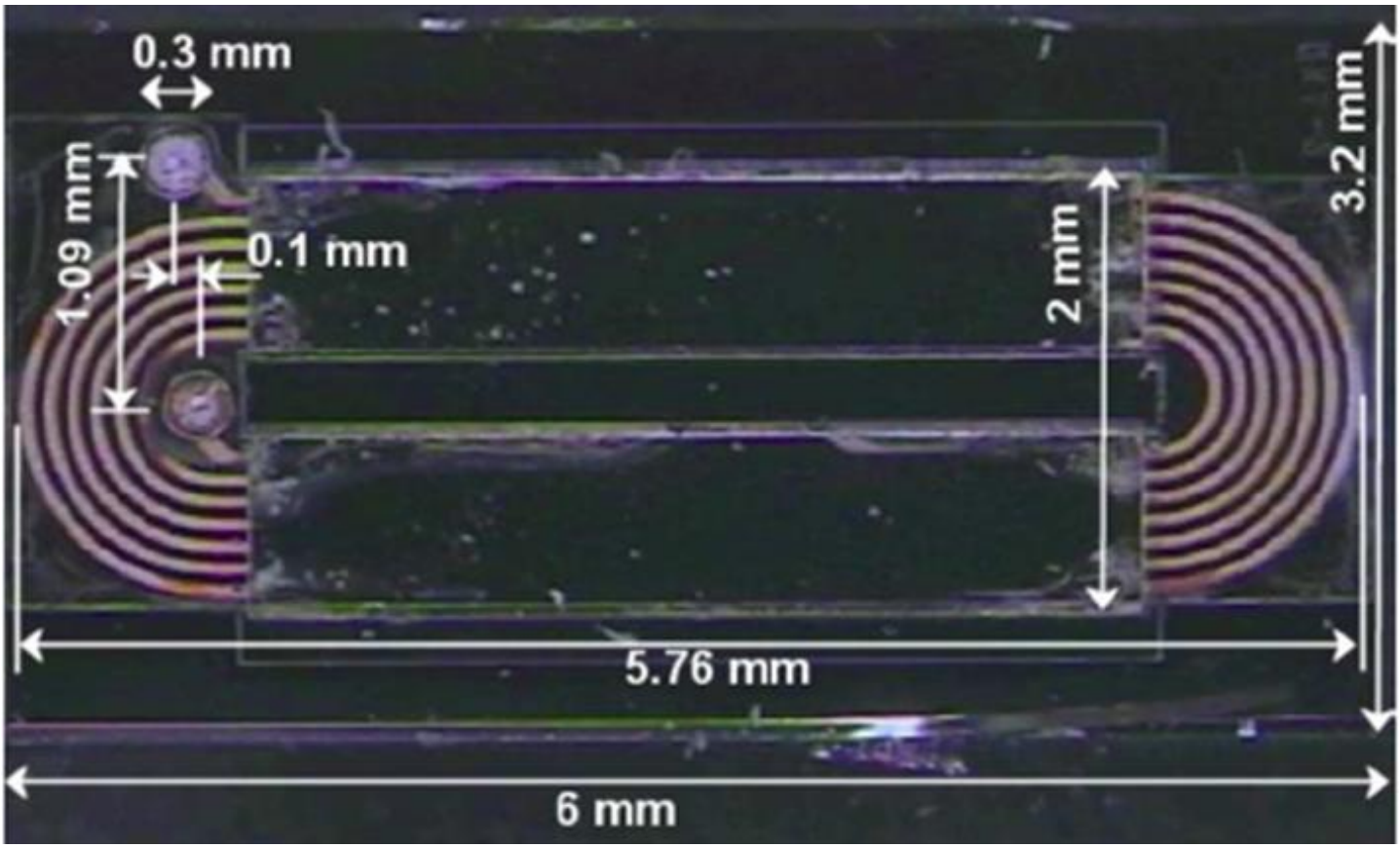


(b)

Figure 1.32. Integrated inductor on silicon substrate with electroplated NiFe demonstrated by Tyndall [94]: (a) cross-sectional view of the winding and core structure, (b) top view of the micro-inductor.

Research is ongoing to develop granular films where the magnetic particles are embedded in oxide insulating matrix phases leading to much higher dc resistivity than conventional alloy thin film. Co-Zr-O/ZrO2 is one example of the granular film materials which can achieve constant resistivity (300 $\mu\Omega$-cm) at operation frequencies up to tens of MHz. Figure 1.33 shows the example of magnetic integration on silicon substrate with a granular film core demonstrated by Dartmouth College[59]. A V-shaped groove is etched into the silicon, and

the CoZrO granular films, insulator and conductor are deposited into the groove. To improve the performance of the core material on the sloping sides, instead of a thick single CoZrO layer, 19nm CoZrO layers and 4nm ZrO2 layers are deposited alternately. However, the 4nm ZrO2 layers are too thin to confine eddy current into separate CoZrO layers. To further decrease the eddy current loss, every 100nm multilayer CoZrO 19nm / (ZrO2) 4nm film is separated by a 20nm ZrO2 layer. The integrated inductor is designed and optimized for a 7V to 3.3V, 1A buck converter. Because of its higher resistivity and the laminate structure (only 19nm each layer), it is found that the CoZrO granular films can achieve more than 10 times lower core loss density than the NiZn ferrite 4F1.

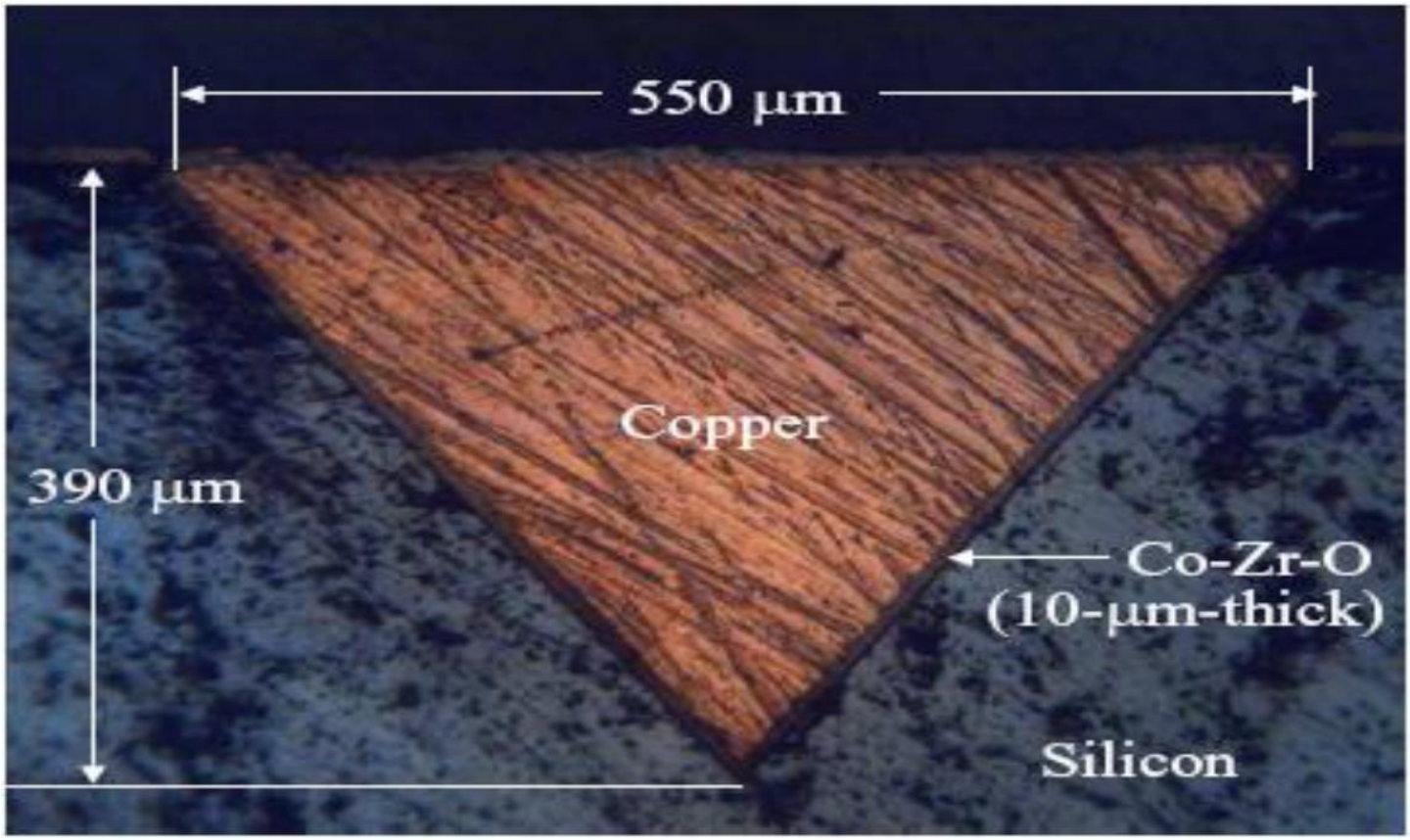


Figure 1.33. V-groove on chip inductor with large copper cross-sectional area to improve current capability of the on-chip inductor demonstrated by Dartmouth College [42].

As a summary, for the alloy thin film and granular film as well as their related integrated inductor, the core thickness of such magnetic materials are limited within several micrometers, which is only good for the wafer-level integration and the applications with current lower than 1A. The core thickness can be increased to the millimeter level by stacking hundreds or thousands of layers. However, electrical isolation is required between each layer. The complicated laminating process makes the alloy thin films unsuitable for the smartphone IVR application, where a certain core thickness in millimeter level is usually needed.

Ferrite polymer composite (FPC) material can also be produced to improve the integrability of the conventional sintered ferrite. In FPC, the ferrite powder is mixed with a polymer binder and then cured into a soft and flexible composite. One of the important advantages of the polymer-bonded magnetic material is the ease of molding, such as injection molding, which can save manufacturing costs. Using such technology, the core thickness can be manufactured in the several millimeters range. A 60W resonant converter with a PCB integrated magnetic substrate is introduced in [74], where the FPC is manufactured in layer and then laminated into the multilayer PCB with a standardized PCB process. However, the core loss density of FPC is more than 10 times larger than that of sintered ferrite and the relative permeability drops to only 10 to 20. In summary, composite materials such as FPC and metal composite, are easy to build into a large core thickness for package-level integration. However, it is difficult to control the high-frequency core loss density and increase the permeability material.

The low temperature co-fired ceramic (LTCC) ferrite material is actually ferrite particles mixed with a ceramic tape material. The thick film, flexible LTCC tape layers can be stacked together in various shapes, pressed, and then co-fired with sliver windings in an oven to create a hard ferrite structure [7, 60]. LTCC ferrite has much more flexibility for building integrated magnetic cores. As a thick film technology, it is also easy to use LTCC technology to fabricate a magnetic core in millimeter thickness level.

The other approach using the alloy magnetic materials is to mill it into flake with a high aspect ratio (i.e. around 1μm thickness and 100μm lateral size [95]). Professor John Xiao's group at the University of Delaware (UD) proposed and implemented processes for the metal flake composite material. After being coated with SiO_2, the metal flake is bound with an organic binder such as polyethylene (PE) or polyvinyl butyral (PVB). Then the composite can be either molded into any core shapes or built into thick-film (>50μm) form by tape casting. The thickness of the laminated thick film structure can be up to several millimeters. The soft metal composite can be cut and drilled with simple mechanical machines, which is desirable for the package-level integration. Because of the high aspect ratio, the flake has to be aligned to be parallel with the external magnetic field to minimize the eddy current loss. The tape casting process used in [95] has a somewhat aligning effect on the flake, but not enough. On the other hand, the permeability and core loss density of the metal flake composite are strongly related to the volume ratio of the metal flake. Generally speaking, a higher volume ratio is better. Due to a slight misalignment and relatively low volume ratio (only 20%), the UD's metal flake composite still has low permeability (below 50) and high core loss density.

Another metal flake composite material (named SENFOLIAGE) is developed by NEC/Tokin, in which both the alignment and the volume ratio of the flake is improved over that of the UD's material [15]. The NEC flake plates with different size and thickness are shown in Figure 1.34. In the fabrication process of the NEC flake as illustrated in Figure 1.35, the iron-based alloy powder is milled into flattened flake, and then aligned in horizontal plane. After coating with oxide material and binding with an organic binder, the hot pressure is applied to combine the flattened flake as a sheet shape. Finally, the flake plates are cured under temperature around 500ºC. A good alignments of the NEC flake material is displayed in Figure 1.36. The volume ratio of the NEC's metal flake is also higher than 50%. Therefore, its relative permeability is increased to several hundred.

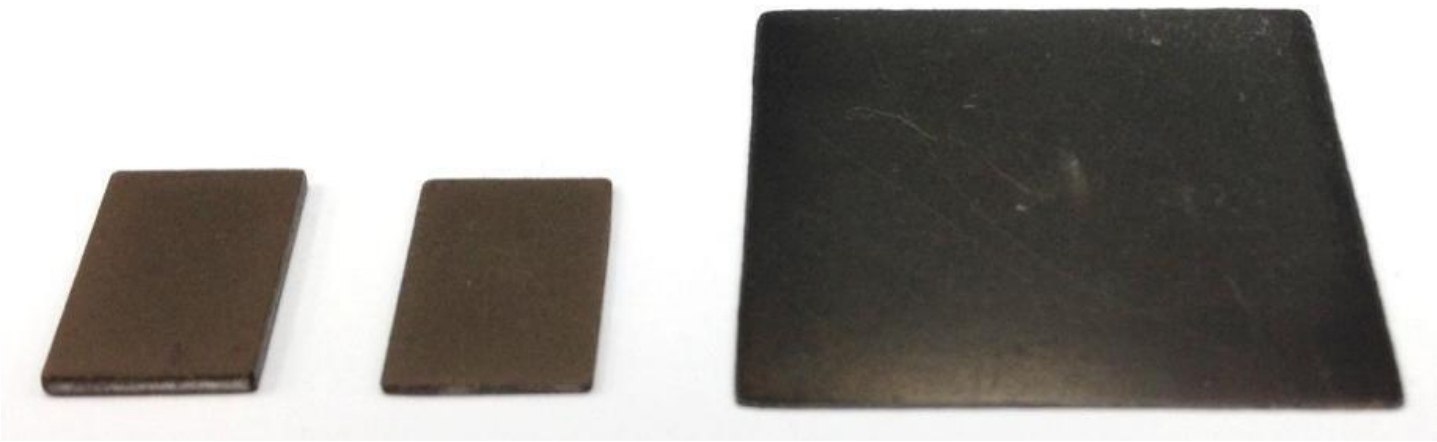


Figure 1.34. SENFOLIAGE metal flake composite plates developed by NEC/Tokin

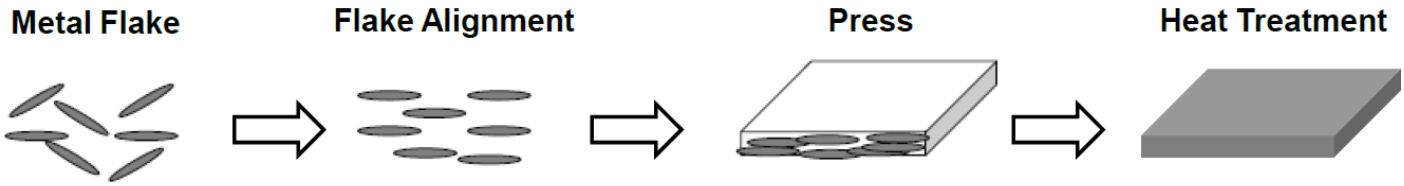


Figure 1.35. Aligning and binding processes for the SENFOLIAGE metal flake composite

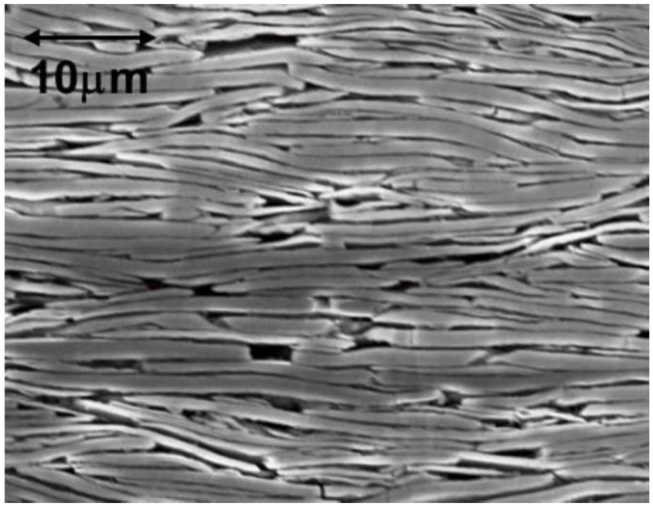


Figure 1.36. Cross section view of the microstructure for NEC metal flake composites.

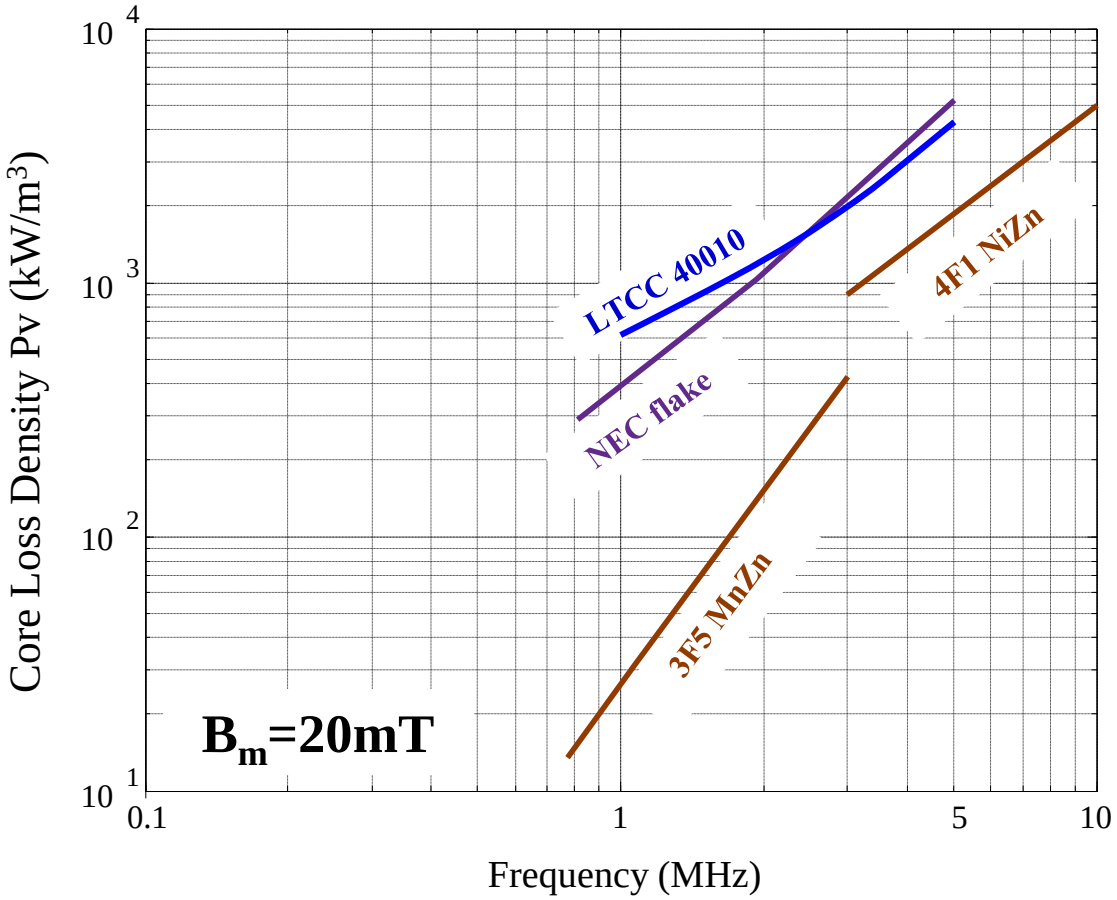


Figure 1.37. The comparison of y core loss density for different high frequency magnetic materials.

The core loss density of the 3F5 MnZn ferrite, 4F1 NiZn ferrite, LTCC, NEC flake material is summarized in Figure 1.37. It can be seen that the ferrite materials have lower core loss density, but they are not chosen in this work for the following reasons: 1) LTCC and NEC flake material have soft-saturating property, which makes them suitable for the air-gap free design in this work; while on the other hand, most of the conventional ferrite materials saturate very quickly even at a low DC biased level, which makes them not proper for an air-gap free design; 2) LTCC and NEC flake materials are formed by a thick film structure, which is more reliable than fragile ferrite materials to sustain the high pressure and high temperature required by the PCB integration process [15].

Comparing the LTCC and NEC flake material up to 5MHz, it seems like the LTCC material has a lower core loss density than the NEC flake material at high frequency. But the real core loss density of them at tens of MHz is unknown due to the limitation of the magnetic characterization technique. To address this issue and provide magnetic properties for the IVR inductor design, the investigation of very high frequency magnetic characterization technique is necessary and will be illustrated in Chapter 3.

1.6. Dissertation outline

Chapter 2 will demonstrate the improvement of the 3D integrated POL module with reduced DCR for higher efficiency, vertical module design for smaller footprint occupation, and hybrid core structure for non-linear inductance control.

Chapter 3 will illustrate the magnetic characterization technique in tens of MHz range. A new core loss measurement method will be proposed to enable the accurate measurement at very high frequency. The high frequency material candidates will be characterized up to 40MHz for the IVR inductor design.

Chapter 4 will focus on the design and verification of the very high frequency IVR for smartphone application with 3D integrated magnetics, featuring a simple single-via winding structure, small size, ultra-low profile, ultra-low DCR, high current-handling ability, air-gap-free magnetics, multi-phase integration within one magnetic core, and a lateral non-uniform flux distribution. Both single-phase and multi-phase integrated inductors will be designed, fabricated and experimentally tested in 20MHz buck converters. The new emerging GaN driver and magnetic material will also be investigated.

Finally the conclusion and future work will be presented in chapter 5.

Chapter 2. 3D Integrated POL for Datacenter CPUs

2.1. Packaging considerations for 3D integrated POL

A major limitation of the 3D PCB integrated inductor introduced in chapter 1 is its relatively large DCR due to the limited copper thickness in the PCB module. The primary source of DCR is the vertical vias in the inductor. As shown in Figure 2.1, the vias conduct the inductor current through a copper film that is electro-plated on the vertical surface of the vias, and the copper thickness is as small as 30μm. As a result, the four vias generates a total DCR of 1.76mΩ. The other source of the DCR comes from the horizontal surface winding that is made by the PCB copper trace. There are two kinds of surface windings: the top and the bottom surface winding, in which the bottom one generates more DCR than the top one due to its larger total conduction length. Even a relatively thick 4oz (0.14mm) copper is applied to the inductor surface winding trace in the PCB module, a relatively big DCR is generated. The DCR of the bottom and top surface winding is 0.7mΩ and 0.3mΩ, respectively. The DCR breakdown of the PCB integrated inductor is shown in Figure 2.2.

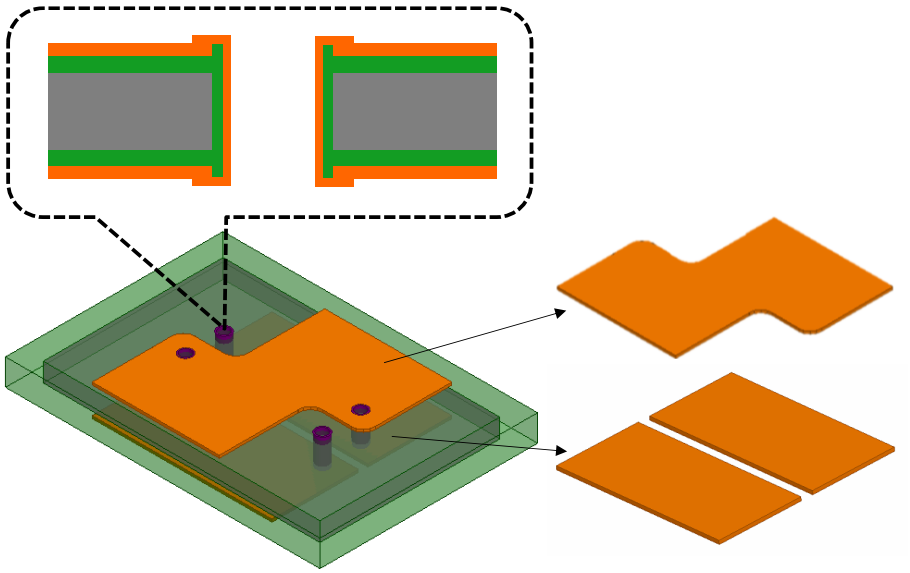


Figure 2.1. Vertical vias and surface windings of the PCB integrated inductor.

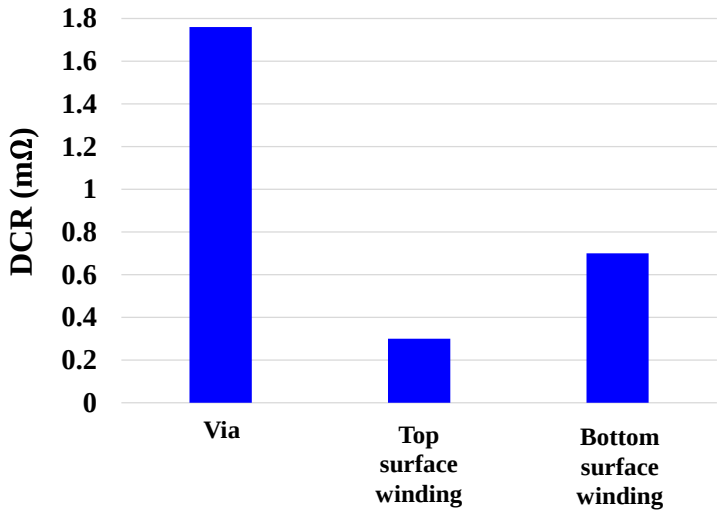


Figure 2.2. DCR breakdown of the PCB integrated inductor.

To overcome this problem, a copper pin can be used to fill into the vias to significantly enlarge the current conducting area. As shown in Figure 2.3, with the pin insertion, the via DCR drops significantly from 1.76mΩ to 0.1mΩ.

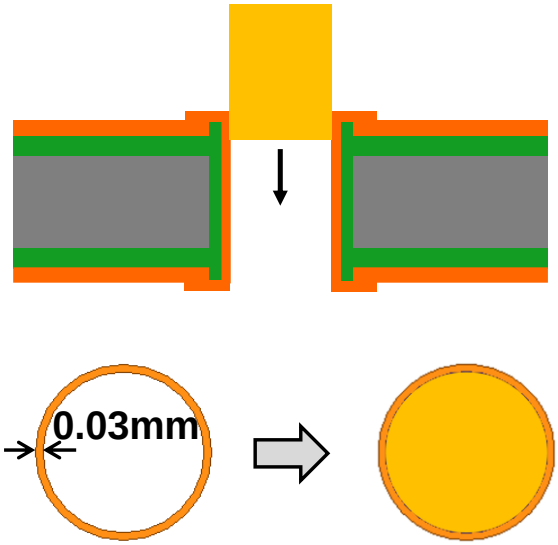


Figure 2.3. Filling the vias with copper to reduce DCR.

In addition, to reduce the surface winding DCR, a new design of the PCB layers is applied. In the previous design, as shown in Figure 2.4, the functions of the four PCB layers is designed as follows: the top layer is an active layer to connect the active components; the second layer is a shield layer to reduce power loop inductance [66]; the third and fourth layers serve as the top and bottom surface winding of the PCB integrated inductor. The mechanism of reducing loop inductance by utilizing a shield layer is shown by the lines in Figure 2.4. The power loop current generates flux (shown by the green solid lines in Figure 2.4), which will generate the opposite direction eddy current in the shield layer; this eddy current also generates flux (shown by the blue dotted lines in Figure 2.4), which cancels with the flux generated by the power loop current. Therefore, the loop inductance can be reduced.

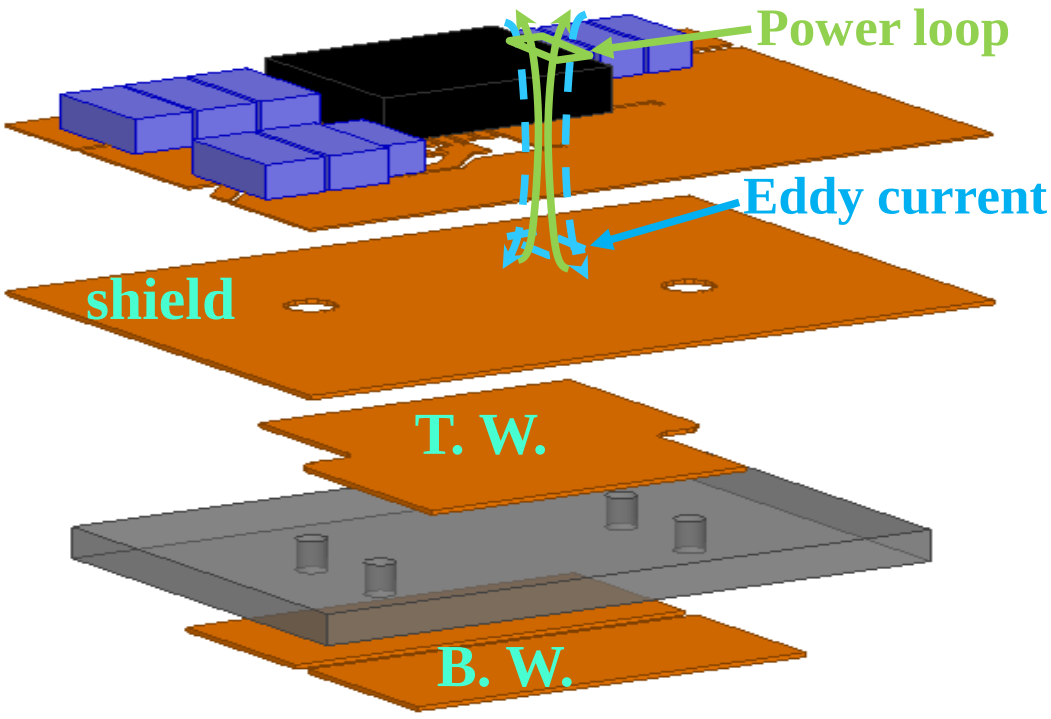


Figure 2.4. Previous design of the four PCB layers for the POL module.

To reduce the DCR and keep the power loop flux cancellation mechanism in the previous design, an improved design is proposed for the PCB module, as shown in Figure 2.5. In the improved design, the shield layer and inductor top surface winding layers (the second and third layers in the previous design) are merged into the second layer. In other words, the second layer in the new design serves as both a shield layer and an inductor top surface winding layer. This is realized by dividing it into two separate areas: shield area and top surface winding area. The shield area is designed to cover the area underneath the power loop, so that the feature of reducing the power loop inductance in the previous design can be kept in the improved design. After integrating the shield layer and top surface winding layer into the second layer, the third and fourth layer can be paralleled and serve as the inductor bottom surface winding together, and thus the bottom winding DCR can be reduced by half.

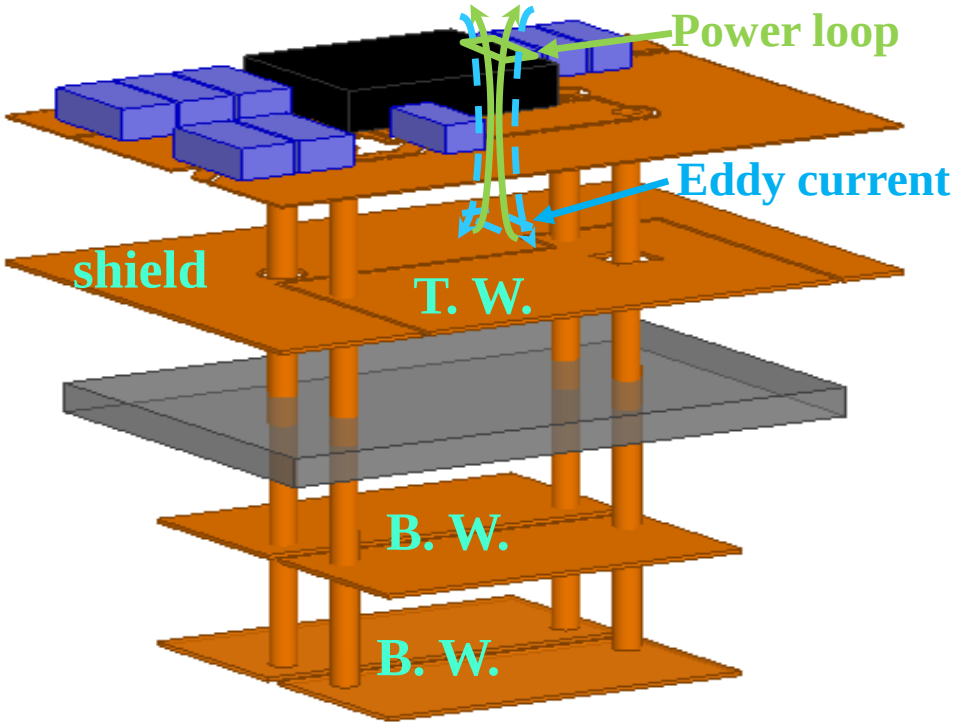


Figure 2.5. Improved design of the four PCB layers for the POL module.

With the improved design, the total DCR of the PCB integrated inductor is reduced by more than 70% from 2.8mΩ to 0.8mΩ, as shown in Figure 2.6.

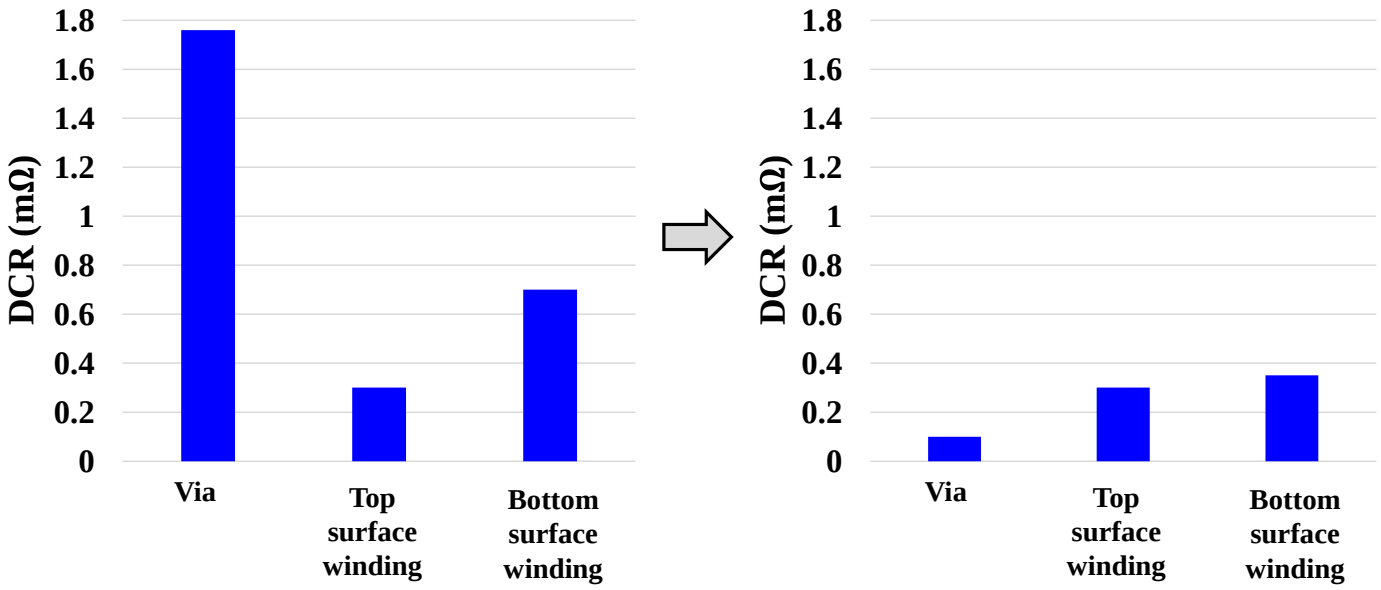


Figure 2.6. DCR reduction achieved by the improved design of the PCB integrated POL module.

The aforementioned design with reduced DCR can be applied to both the single-phase and two-phase coupled PCB integrated POL module, as shown in Figure 2.7. With the help of the new design, the efficiency of the two-phase module is significantly improved. As shown in Figure 2.8, a 4% efficiency boost at a full load condition is achieved by the improved design.

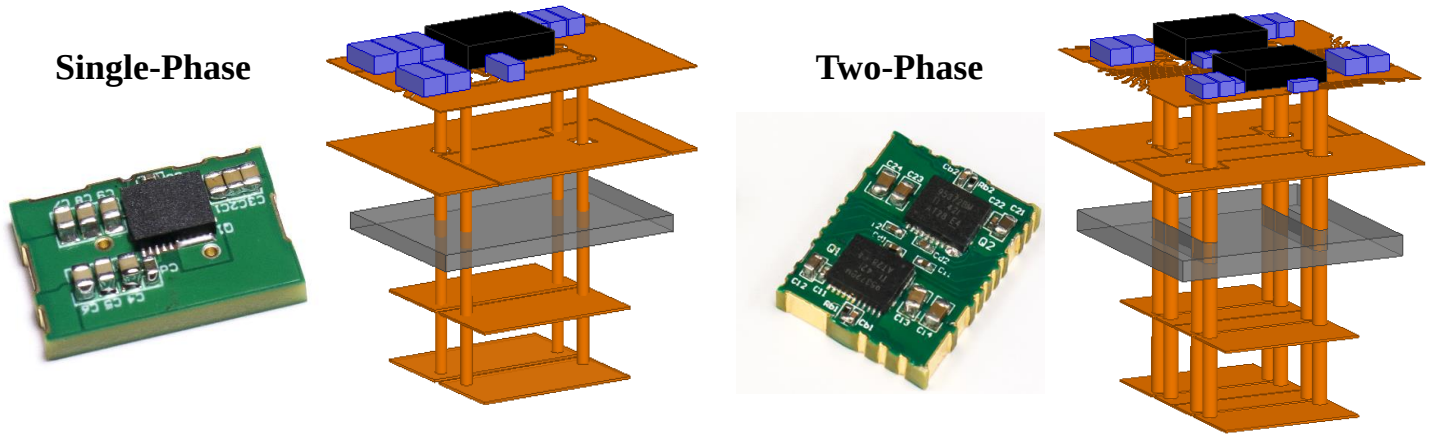


Figure 2.7. Applying the improved PCB design to both single-phase and two-phase coupled POL modules.

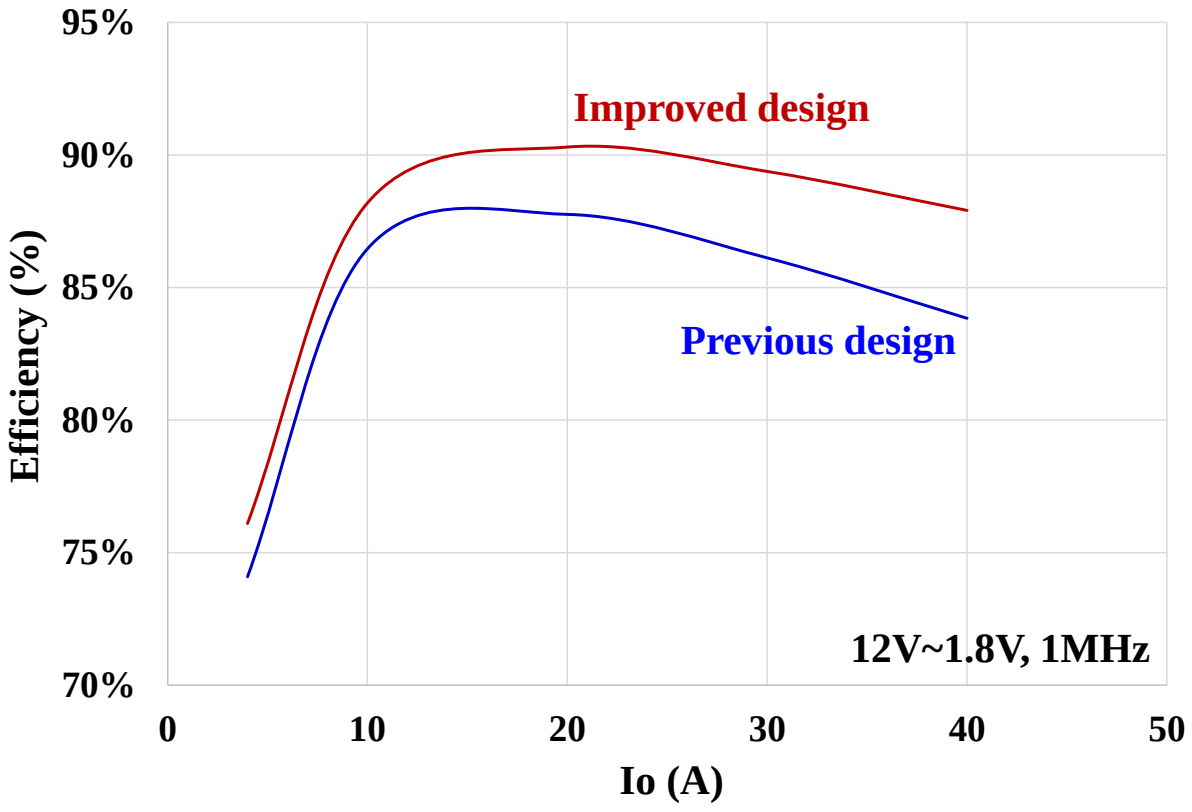


Figure 2.8. Efficiency improvement achieved by the improved design of the two-phase coupled POL module.

2.2. Design of vertical mounting POL with improved thermal management

In this section, a significant footprint saving of the POL module is demonstrated by using a vertical mounting design with an improved thermal management. Figure 2.9 shows an Intel two-processor, one-unit (2P 1U) server platform, in which it can be seen that the tallest parts on the server motherboard are usually the DDR card and the processor heat sink. The height of the vertical standing DDR card is usually larger than 30mm. On the other hand, the POL is designed to be laterally mounted on the motherboard, which leaves a lot of vertical space underutilized. To better utilize the space, we propose a vertical mounting design for the PCB integrated POL module. Its concept is shown in Figure 2.10. As the POL module is designed to be "standing" on the motherboard, a more than 70% saving of the footprint occupied by the POL can be achieved.

Figure 2.9. Intel's two-processor, one-unit (2P 1U) server platform.

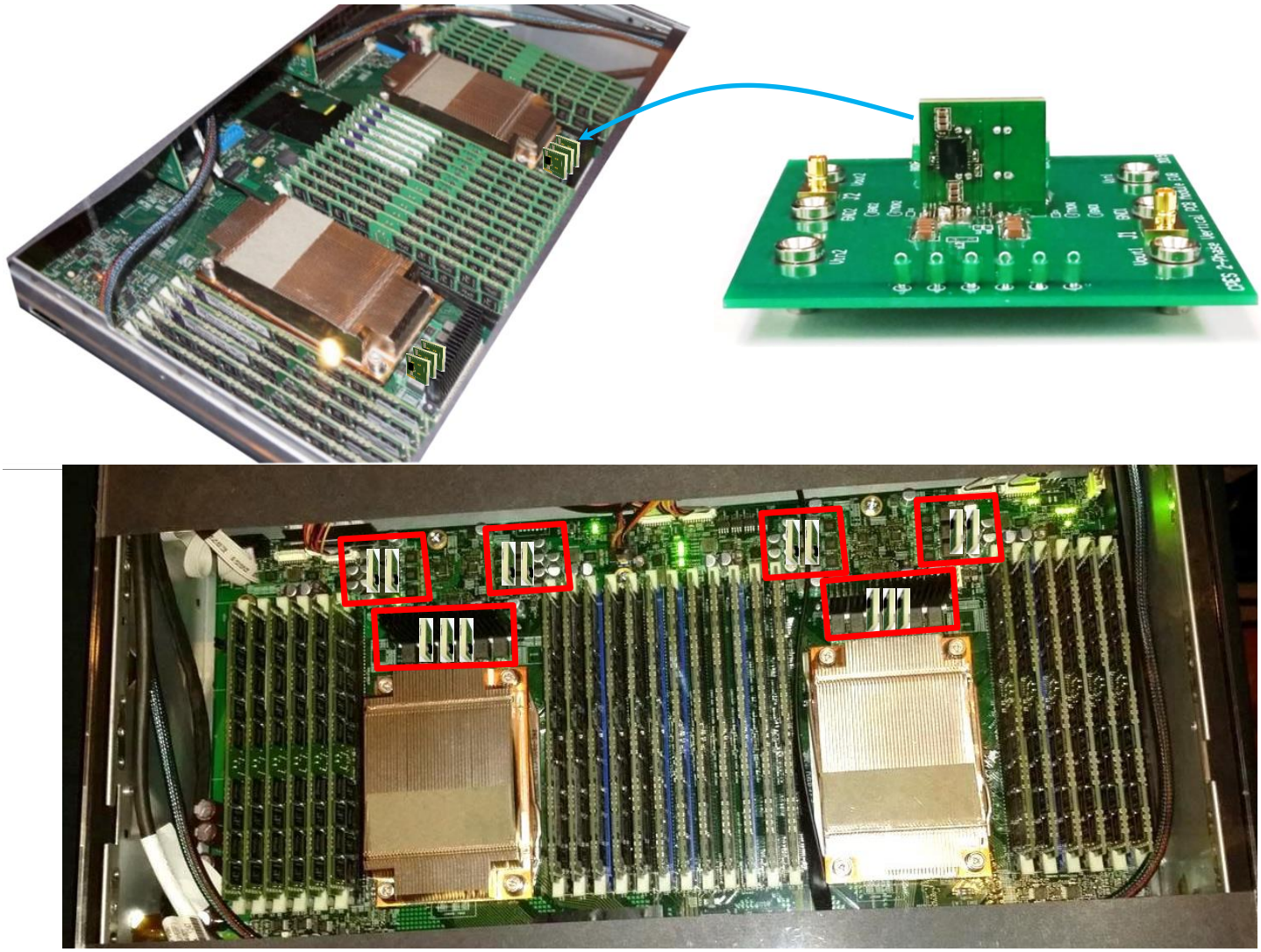


Figure 2.10. Demonstration of vertical mounting POL module concept in server platform.

To implement the vertical mounting POL module, there are several design points need to be taken into consideration. First of all, the input/output ports need to be relocated from two edges to one side of the module. As shown in Figure 2.11, for the lateral mounting POL, the input/output ports of the module are located at two different edges of the module; while for the vertical mounting POL, all the input/output ports have to be placed at one edge of the module, because there is only one edge that has physical contact with the motherboard. The

relocation of the input/output ports can be achieved by re-designing the layout of the copper trace in the active layer, as shown in Figure 2.12, but it would induce another issue in the magnetic coupling of the PCB integrated inductor. As shown in Figure 2.11 and Figure 2.12, due to the change of the current direction in the inductor, the magnetic coupling between the two phases would change from negative (inverse) coupling to positive (direct) coupling. Consequently, the POL module would lose the benefits gained from the negative coupling, including a higher steady state inductance than the transient inductance [96, 97] and an improved inductance density due to the DC flux cancellation in the magnetic core [68]. Therefore, a further design modification is made to keep the negative magnetic coupling by moving one of the Dr. MOS devices from one side of the module to the other side. As shown in Figure 2.13, by flipping one phase's PCB trace design from one side of the module to the other side, i.e. the first layer interchange with the fourth layer and the second layer interchange with the third layer, the negative magnetic coupling of the inductor and the associated benefits can be restored in the vertical design.

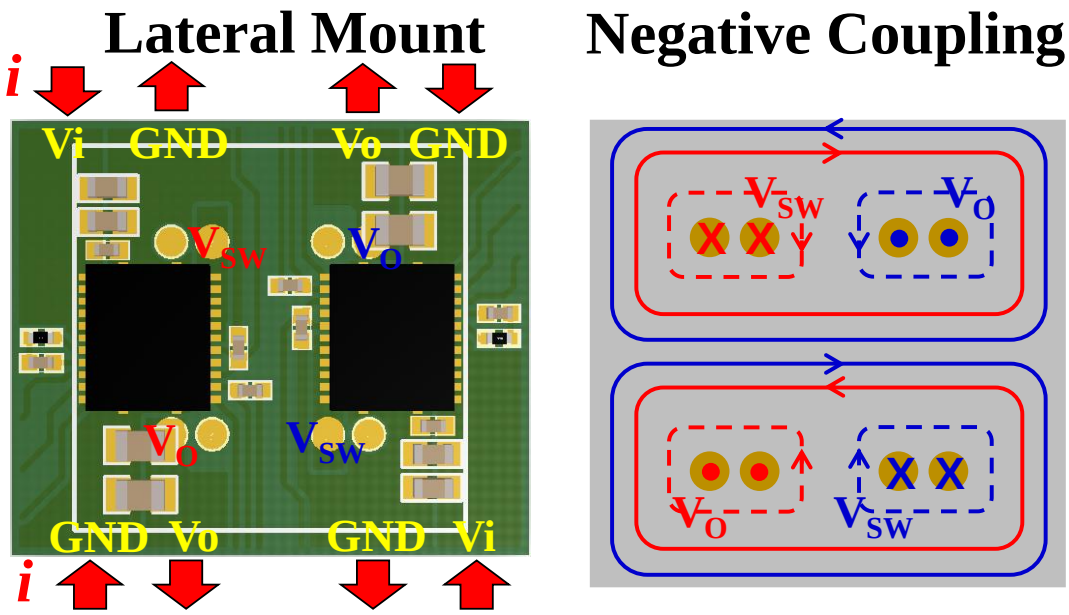


Figure 2.11. Input/output ports in the lateral mounting POL module and the magnetic coupling of the PCB integrated inductor.

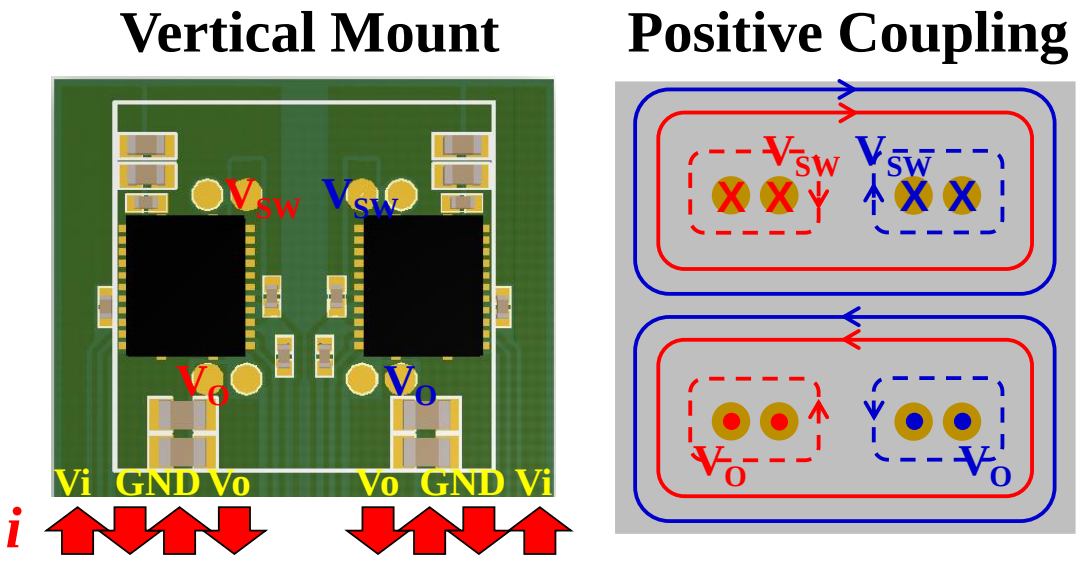


Figure 2.12. Input/output ports in the vertical mounting POL module and the magnetic coupling of the PCB integrated inductor.

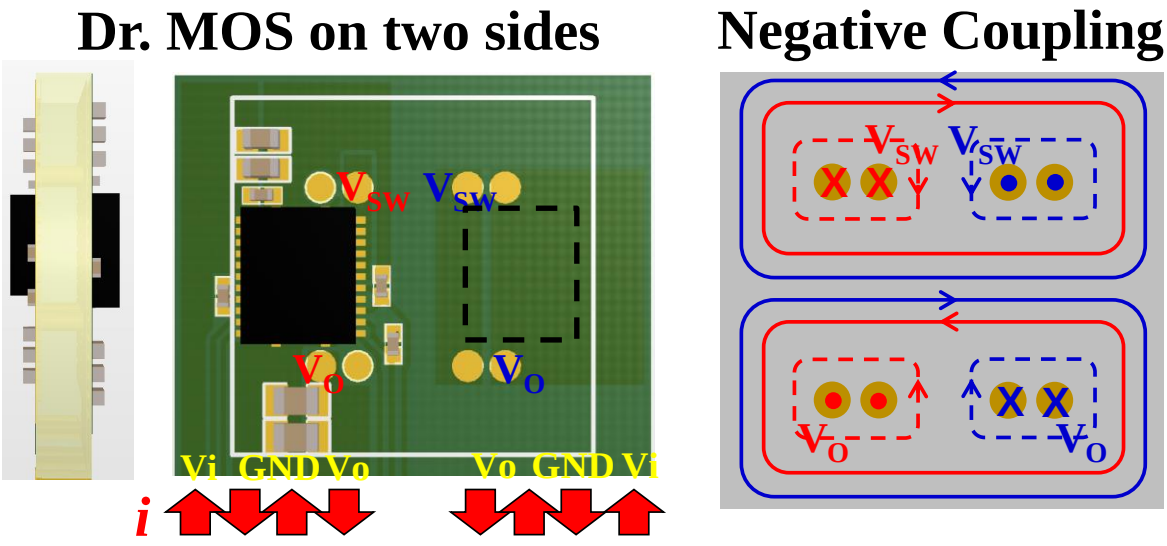


Figure 2.13. Vertical mounting POL module with Dr. MOS on both sides of the module to achieve negative magnetic coupling in the PCB integrated inductor.

Besides the electrical connection and magnetic coupling, another design aspect that needs to be considered is the thermal management. Unlike the lateral mounting POL module, it is not easy to attach a large and thick heat sink on the vertical mounting POL module. Therefore the thermal management of the vertical POL module needs to be carefully designed. To help the heat dissipation through the top side of the module, a double side cooling package of Dr. MOS is used in the design, as shown in Figure 2.14.

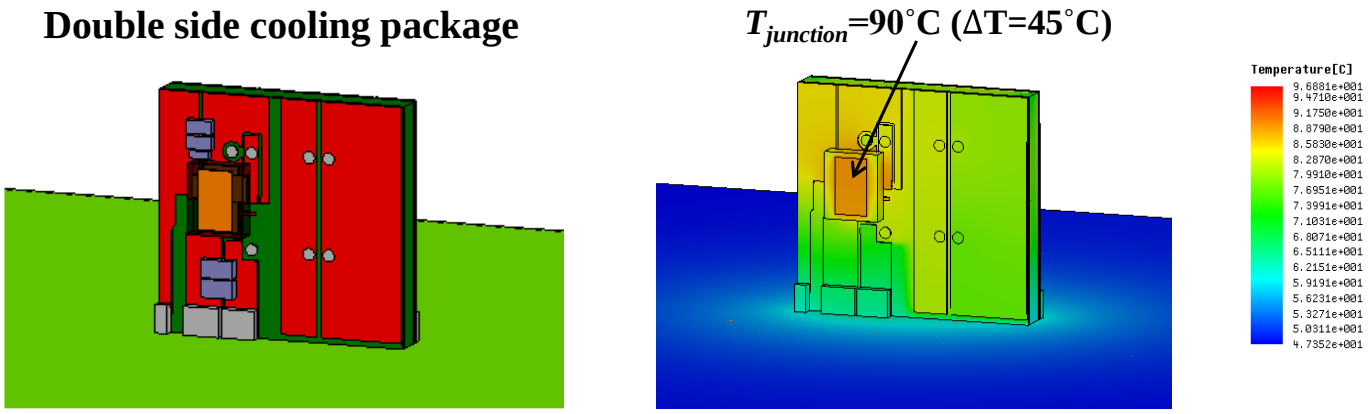


Figure 2.14. Thermal evaluation of the vertical mounting POL module with double side cooling package. The results are acquired with Ansys simulation tool at airflow of 400LFM, ambient temperature of 45ºC. A 60% max power is used here to represent thermal design power (TDP).

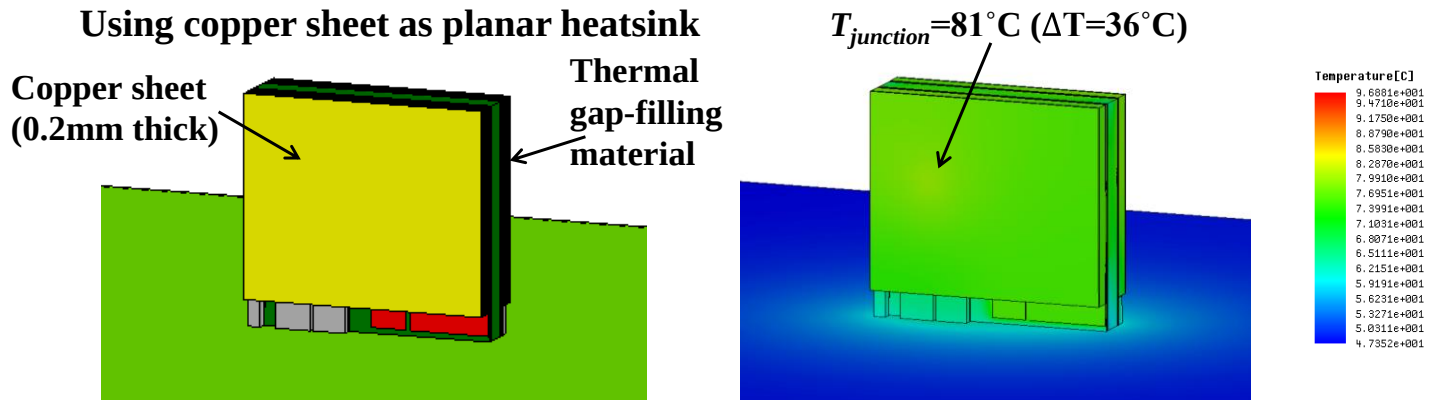


Figure 2.15. Thermal management of the vertical mounting POL module with planar heat sink.

Furthermore, a planar heat sink made by very thin (0.2mm thickness) copper sheet is attached on both sides of the POL module, as shown in Figure 2.15. The planar heat sink does not occupy much space, while it can provide a big surface area to effectively help the heat dissipation of the Dr. MOS. As shown in Figure 2.14 and Figure 2.15, a 20% reduction in junction temperature rise can be achieved with the planar heat sink.

2.3. Inverse coupled multi-phase VR with improved density and transient response

The two-phase coupled inductor working in synchronous buck converter has two equivalent inductances: a steady-state inductance L_{ss}, which impacts the steady state current ripple (a larger L_{ss} value is preferred) and a transient inductance L_{tr}, which impacts the load transient response (a smaller L_{tr} value is preferred) [96]. Based on an ANSYS's Maxwell FEA simulation [98], the L_{ss} and L_{tr} of a two-phase coupled PCB integrated inductor in the whole load range is plotted in Figure 2.16, which shows that both of them are highly non-linear. The non-linearity can be attributed to the non-linear permeability of the core material and the un-gapped inductor structure.

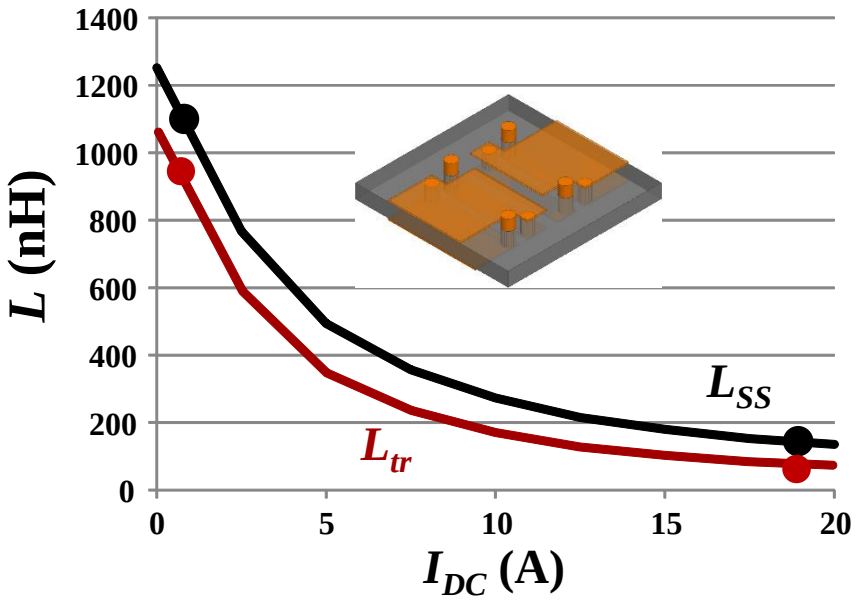


Figure 2.16. Non-linear inductance of the two-phase coupled inductor.

As shown in Figure 2.17, the non-linearity of L_{ss} is beneficial for the light load efficiency due to the large L_{ss} and small current ripple at light load condition [32]; while the non-linearity of L_{tr} is impeditive for the transient dynamics because a large light load L_{tr} slows down the transient response [99].

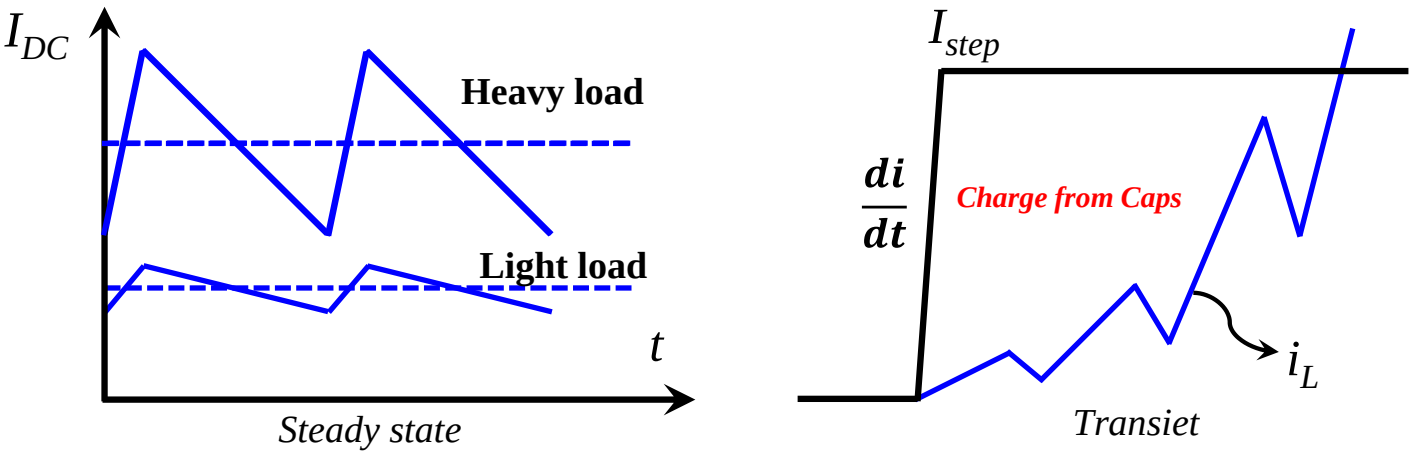


Figure 2.17. Trade-off between the efficiency and dynamics from the non-linear inductance.

To illustrate the non-linear inductance, the flux path in a two-phase reverse-coupled inductor is plotted in Figure 2.18. It can be seen that the coupled DC flux cancels each other in the surrounding path which encircles the two windings, while the leakage DC flux reinforces each other in the central path between the two windings. Consequently, the DC bias in the central path is much stronger than that in the surrounding path. The DC flux distribution (which determines the core permeability [15]) in the coupled inductor at both light load and heavy load conditions is plotted in the first column of Figure 2.19. From this one can identify the two key reasons for the large leakage inductance (which is equal to L_{tr} [96]) at light load condition: 1) the core has a much higher permeability at the light load condition than at the heavy load condition; and 2) the permeability increase at the central path (~150 times) is much higher than that at the surrounding path (~2 times), which leads to a much easier path (due to small reluctance) for the leakage flux at light load condition. To overcome the impediment caused by the large L_{tr}, a solution is proposed by adding a slot in the central path to block the leakage flux [99]. The DC flux distribution of the coupled inductor with slot is shown in the second column of Figure 2.19. It can

be seen that a large reluctance for leakage flux is created by the slot in the central path, and the core permeability is much more stable at different load conditions than the no slot structure because most of the magnetomotive force is now applied to the air slot. As a result, the non-linearity of the inductance can be remarkably reduced, as shown in Figure 2.20.

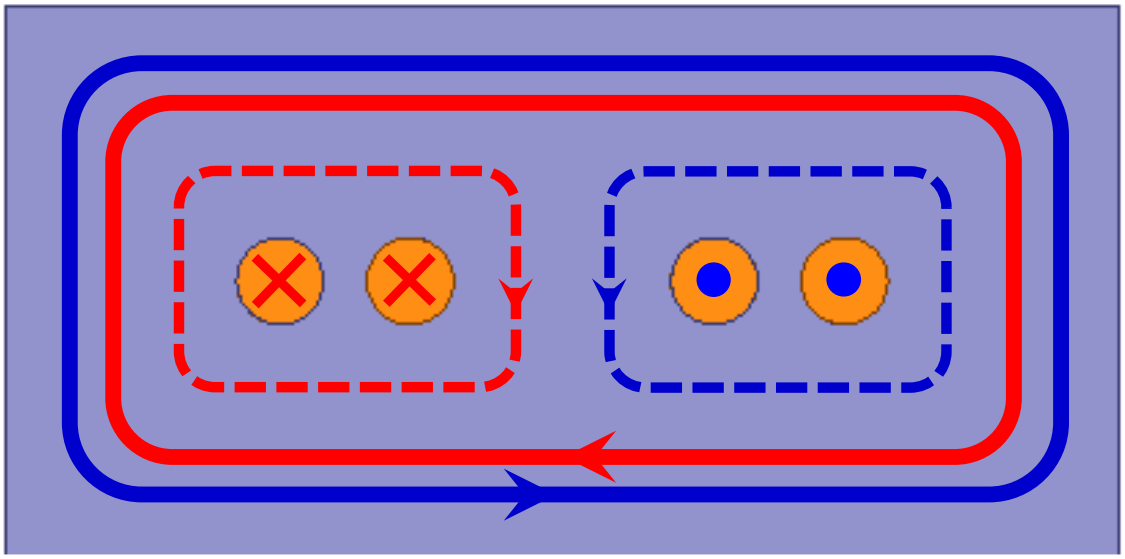


Figure 2.18. The flux path in a two-phase reverse-coupled inductor (only half core is shown due to symmetry). The solid lines indicate the coupled flux, and the dashed lines indicate the leakage flux. The cross and dot in the windings indicate the current direction.

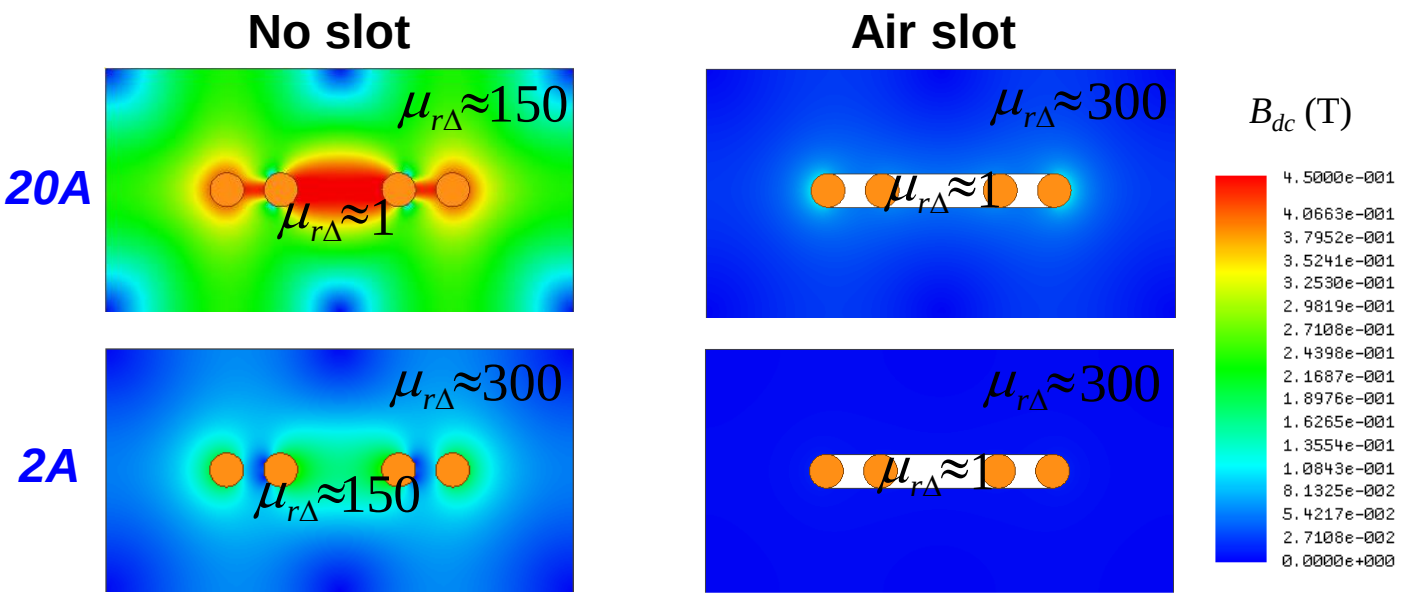


Figure 2.19. DC flux distribution for two-phase coupled inductor with no slot and air slot structure at full load and light load conditions.

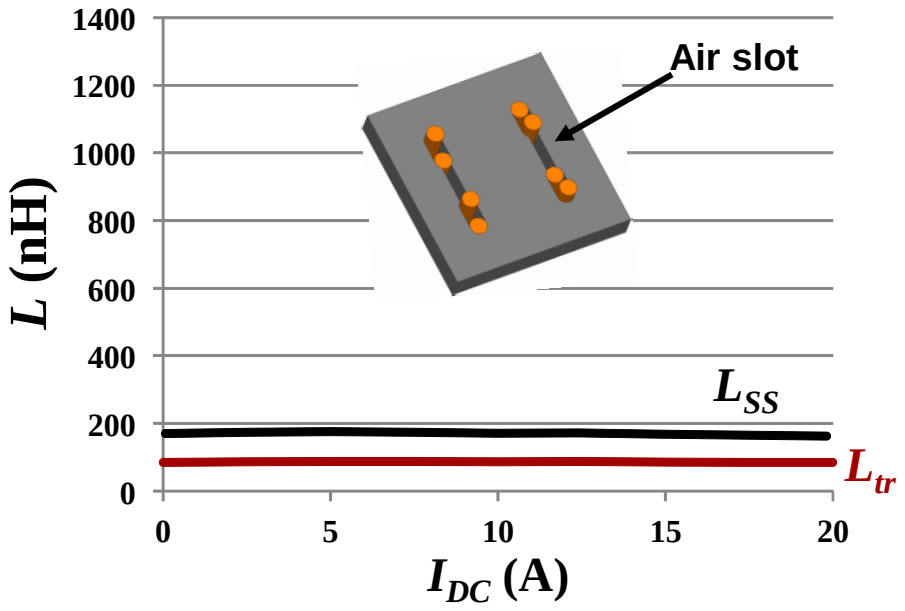


Figure 2.20. Almost constant inductance of coupled inductor with air slot structure.

Adding an air slot can effectively reduce L_{tr}, but it has to pay the price of 1) a fringing effect induced by the air slot, and 2) a significant reduction of L_{ss}, especially at light load, due to the much smaller inductance non-linearity when compared to the no slot structure. Therefore, filling a low permeability material into the slot is proposed to alleviate the fringing effect and to achieve a controllable non-linearity of inductance (and thus a controllable trade-off between L_{ss} & L_{tr}) by controlling the permeability of the filling material. The structure of the coupled inductor with the low permeability slot is shown in Figure 2.21.

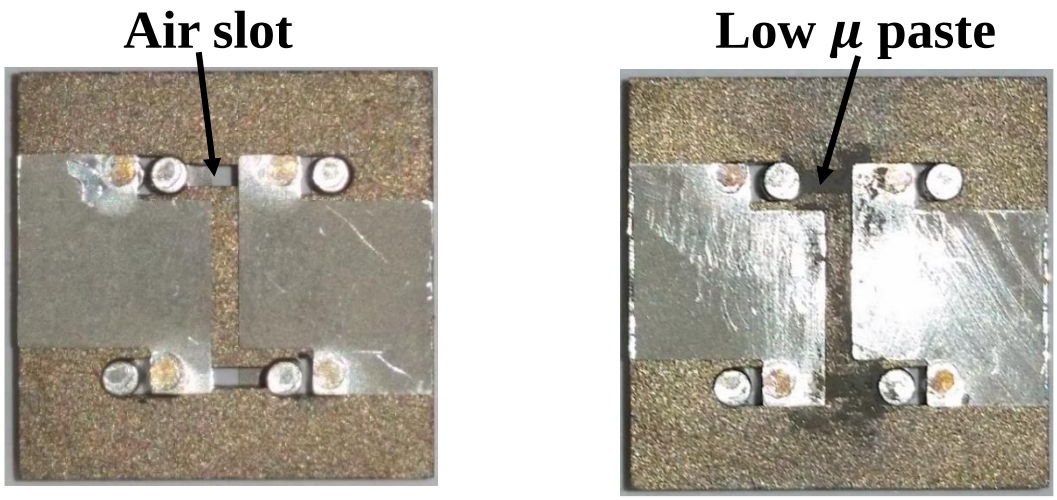


Figure 2.21. Two-phase coupled inductor with air slot and low permeability magnetic paste material in the slot.

In this work, a magnetic paste material with an initial relative permeability μ_i≈4 and 10 from NECTOKIN is used to fill the slot. The L_{ss} and L_{tr} of the coupled inductor with air slot and coupled inductor with different low μ slot are summarized in Figure 2.22. It can be seen that filling the air slot with low μ material can remarkably improve L_{ss} with a reasonable price of an increase in L_{tr}.

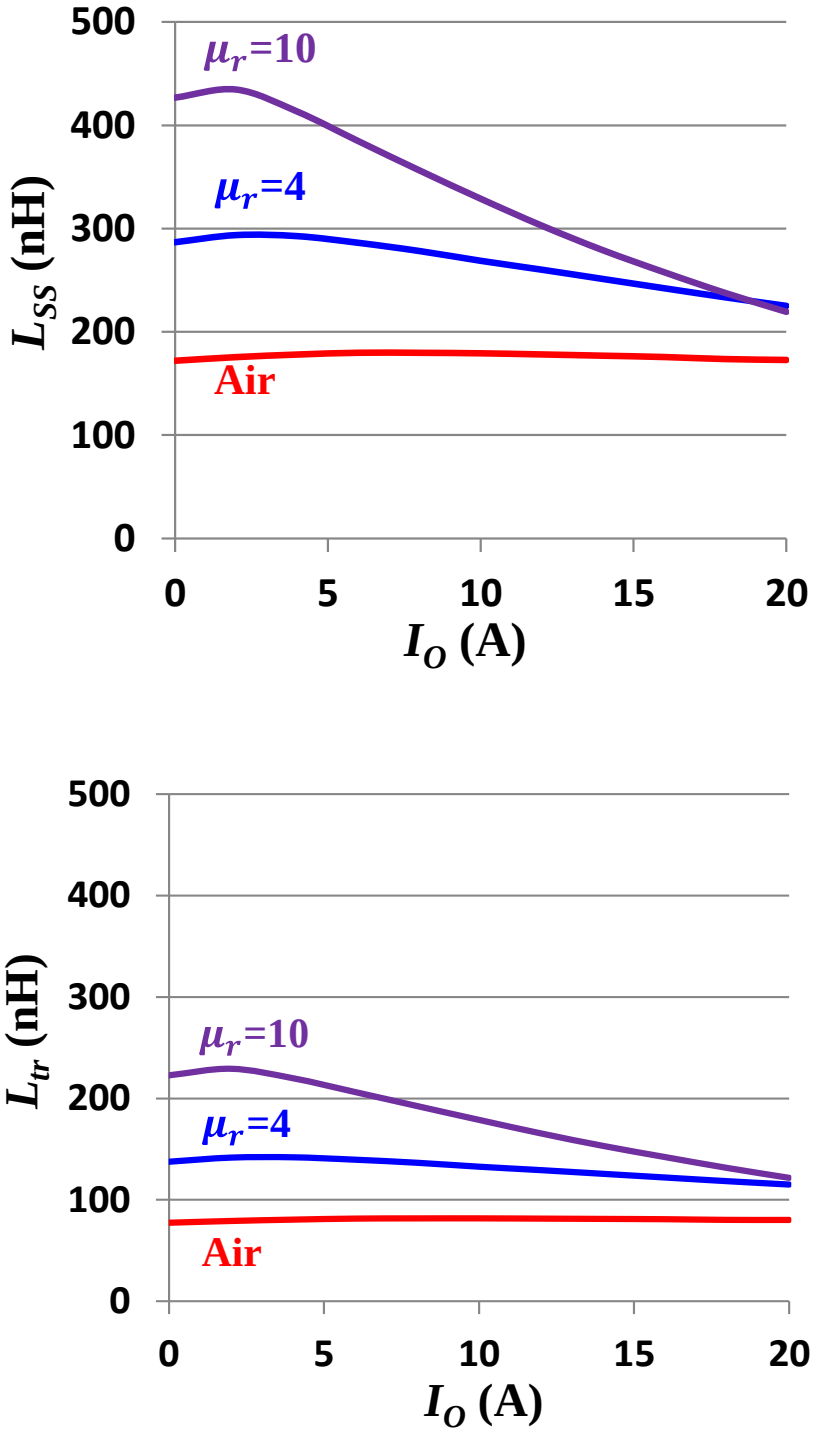


Figure 2.22. Inductance of the two phase coupled inductor with air slot and low μ slot with different low permeability magnetic paste materials.

The inductor loss under the full load current is also analyzed by FEA simulation [98], and the results are shown in Figure 2.23. It can be seen that the total inductor loss of the air slot structure and the low μ slot structure are similar to each other. For the structure with a low μ slot, the low μ paste material contributes only 4% of the total core loss due to its small volume portion.

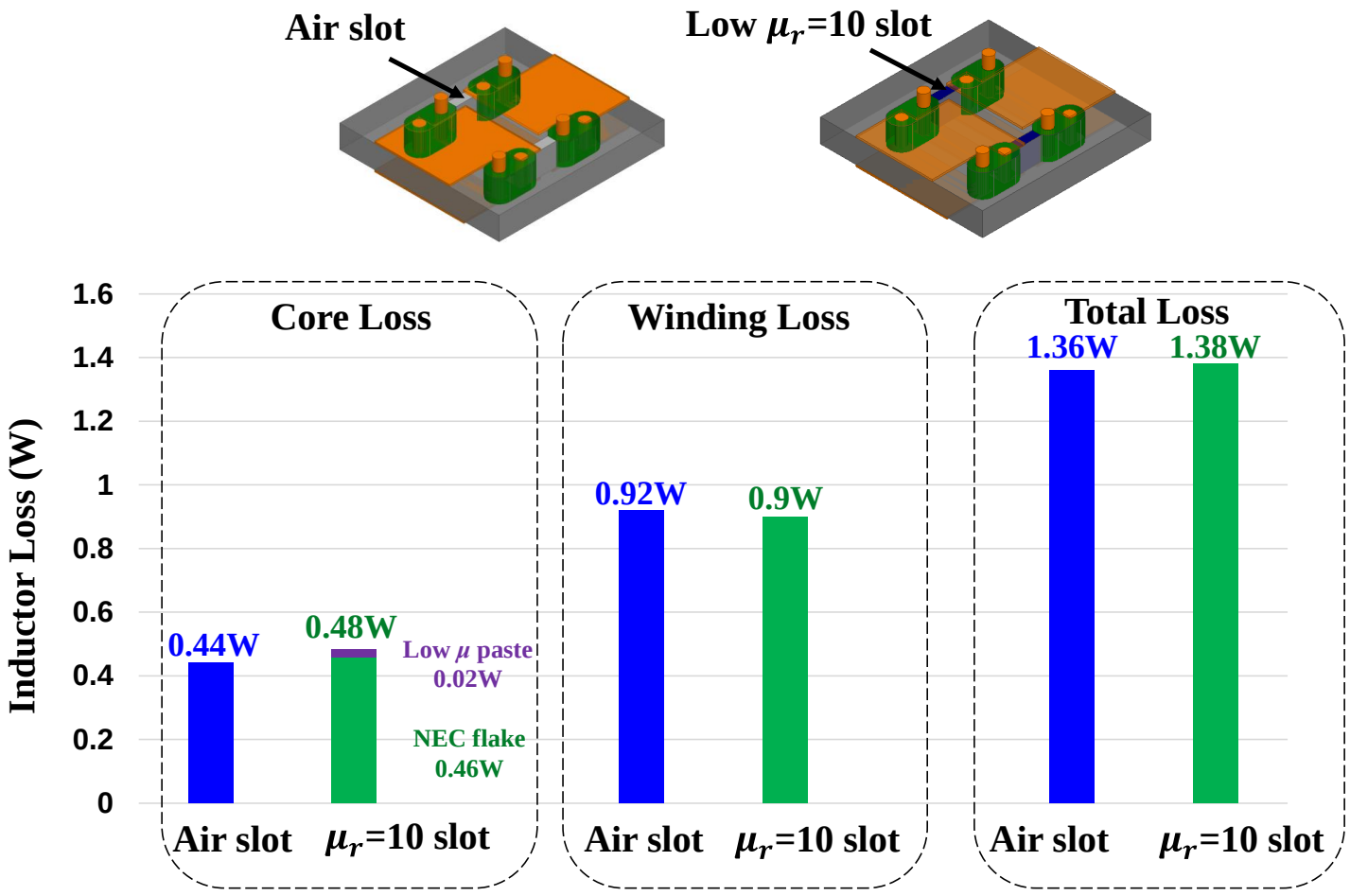


Figure 2.23. Inductor loss analysis of the two-phase coupled inductor with air slot and low permeability slot.

With the similar inductor loss, adding the low μ paste material can effectively improve the efficiency of the converter, as shown in Figure 2.24, because of the lower switching loss and conduction loss due to the smaller current ripple that stems from the larger steady state inductance.

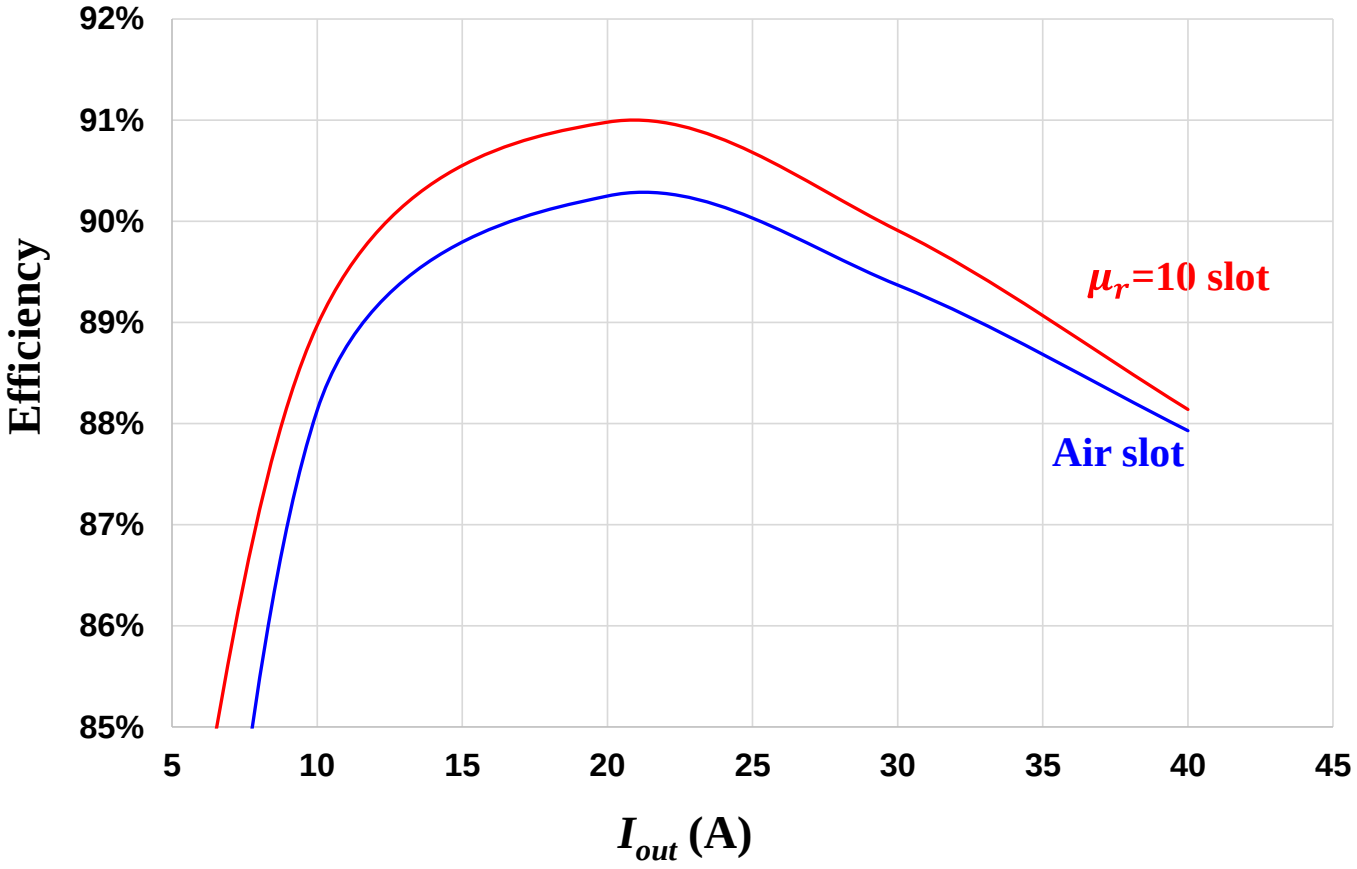


Figure 2.24. Efficiency improvement by adding the low permeability paste material in the slot of the two-phase coupled inductor.

Moreover, Figure 2.25 shows another benefit of adding the low μ paste material in the slot: the fringing flux around the slot can be effectively reduced for a smaller interference with the adjacent components.

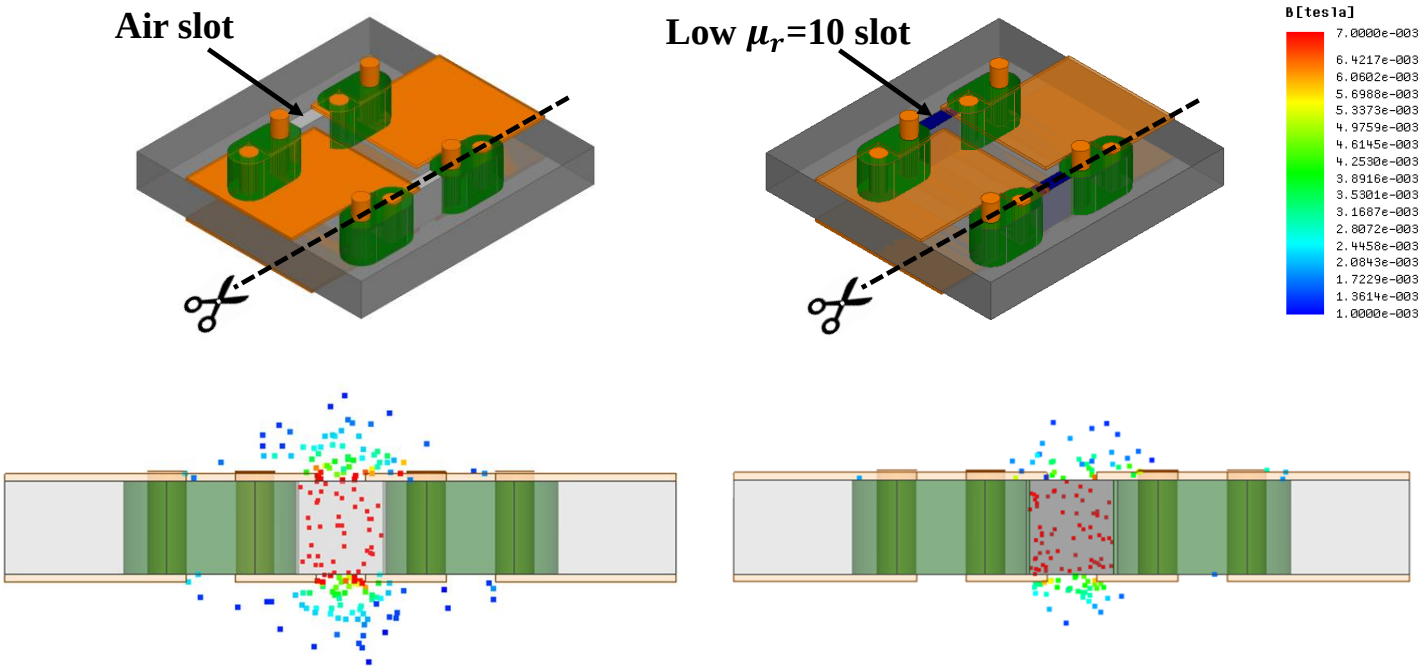


Figure 2.25. Improved fringing flux confinement by adding the low permeability paste material in the slot.

2.4. Summary

The 3D PCB integrated POL module is improved with a 2~4% efficiency boost by reducing the DCR by pin insertion and by merging the shield copper layer and top surface winding layer.

A >70% footprint savings is achieved by a vertical mounted POL design. The negative magnetic coupling in the core is preserved in the vertical design. An improved thermal management using planar heat sink is proposed for the vertical POL module.

Various low permeability paste materials are applied in the coupled inductor design to control the inductance non-linearity and reduce the fringing flux around the slot. Filling the slot with a low permeability paste can increase the instance density with almost no additional inductor loss.

Chapter 3. Magnetics Characterization and Core Loss Measurement

3.1. Limitation of existing core loss measurement techniques

The desire for smaller and smarter electronics in recent years generates a significant demand to improve the power density of converters, especially in the miniaturization and integration of the traditional bulky magnetics [16, 75, 100, 101]. To achieve this goal, power converter's switching frequency has been pushed higher and higher, which makes the core loss an important factor in magnetic design and converter efficiency. Therefore, accurate core loss measurement, especially at high frequencies, plays an important role in magnetic and thermal design[83, 102], as well as the exploration of new high-frequency magnetic materials[69, 103, 104].

Among the existing core loss measurement methods in the prior arts [105-117], the thermal method is a very common way to test the core loss [105-108]. In a basic calorimeter, the level of liquid coolant is fixed. At the beginning, the relationship between heat and the temperature difference or its rising rate is measured with a reference heat generator (for example using a resistor with known resistance). And then the reference heater is replaced with the device under test (DUT). By measuring the temperature differences or the rising rate, the loss can be estimated. Stirring is necessary for the uniform temperature of the coolant. A more sophisticated calorimeter uses the circulating coolant to measure the heat[105], as shown in Figure 3.1. The basic idea is to put the winded core in the thermal isolated chamber, and measure the temperature difference between the inlet and outlet coolant. With the temperature difference, the heat generated by the excited inductor can be calculated. Generally speaking, the thermal approach is a pretty universal way to test the core loss. It can measure the core loss under any desired excitation or bias. However, it has the following disadvantages: 1) the measurement process is very time consuming. Each measurement needs to wait until the temperature is stabilized. For temperature sensitive samples, the coolant temperature should return to its initial value after each measurement,

which further reduces the efficiency of such tests; 2) the winding loss is not easy to compensate, especially when the testing is performed at higher frequencies. Although some literatures proposed ways to excite the core without windings[108], a sophisticated setup is required to do so; and 3) when the loss is small and temperature rise is low, the accuracy is poor.

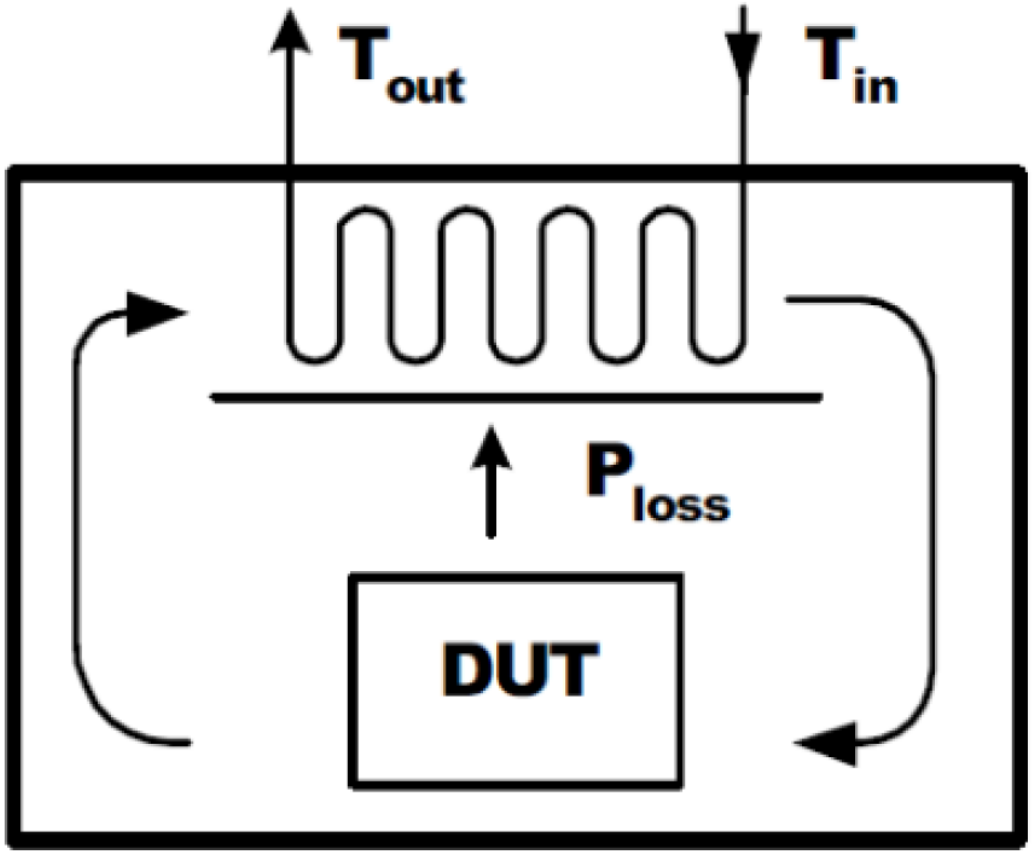


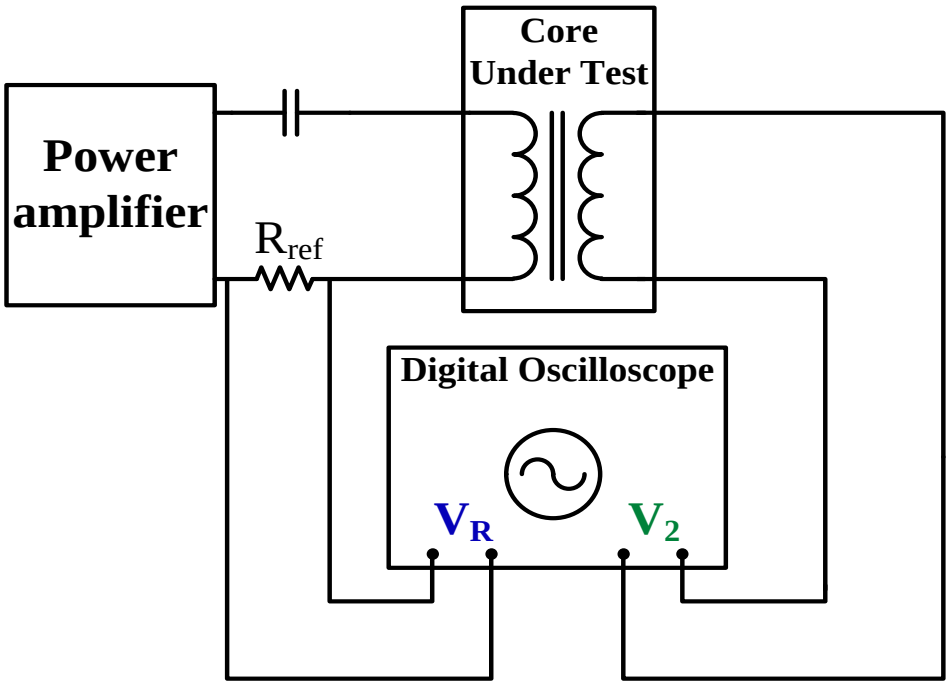
Figure 3.1. Closed type calorimeter

Besides the thermal method, the electrical method is much easier to implement. Among the electrical core loos measurement methods, the two-winding method is widely used and considered a classical method[114-117]. Its

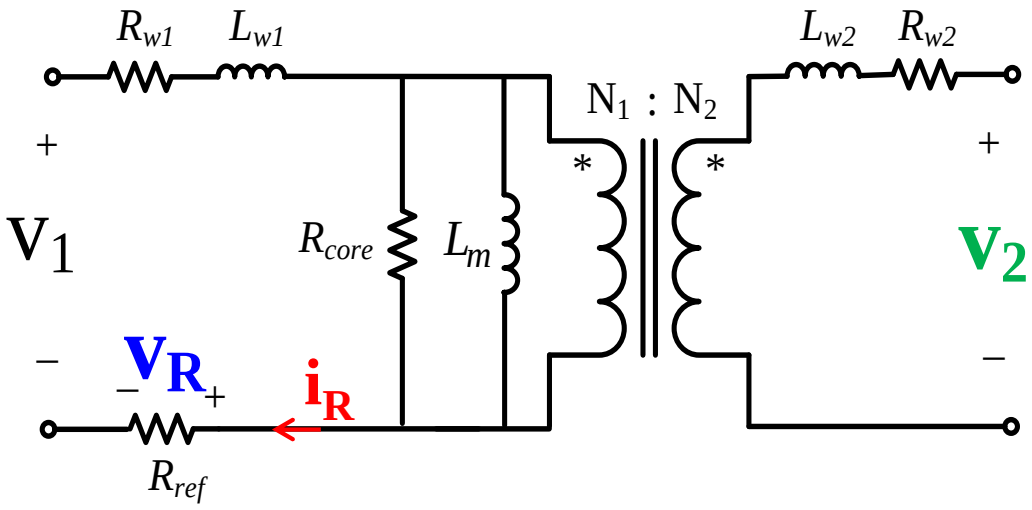
measurement setup and equivalent circuit are shown in Figure 3.2. The core loss can be extracted by integrating v_2 and v_R/R_{ref} over time. This method can exclude the winding loss from the measured core loss, and it is applicable to arbitrary wave excitation. However, it suffers from its sensitivity to phase discrepancy. The phase discrepancy is the phase angle difference between i_R and measured v_R. This discrepancy usually comes from the current sensing resistor's parasitic, a mismatch between probes, and an oscilloscope's sampling resolution; the influence of them becomes very severe at high frequency. For example, a 0.2Ω sensing resistor with a 1nH ESL will produce an 8.9° phase discrepancy at 5MHz. The measurement error Δ caused by the phase discrepancy $\Delta\varphi$ for sinusoidal excitation is [118]

$$\Delta = tan(\varphi_2) \cdot \Delta\varphi \tag{1}$$

where φ_2 is the phase angle difference between v_2 and i_R, which is very close to 90° since the impedance of magnetizing inductor L_m is usually much smaller than the equivalent core loss resistor R_{core}. This makes $tan(\varphi_2)$ very large and leads to the sensitivity to phase discrepancy. The relation between φ_2 and the measurement error is shown in Figure 3.3. For the rectangular excitation, a small phase discrepancy can also lead to a large measurement error at high frequency [119].



(a) Measurement set up



(b) Equivalent circuit

Figure 3.2. Set up and equivalent circuit of two-winding method. The R_{w1}, R_{w2}, L_{w1}, and L_{w2} correspond to the resistance and leakage inductance of the winding wires.

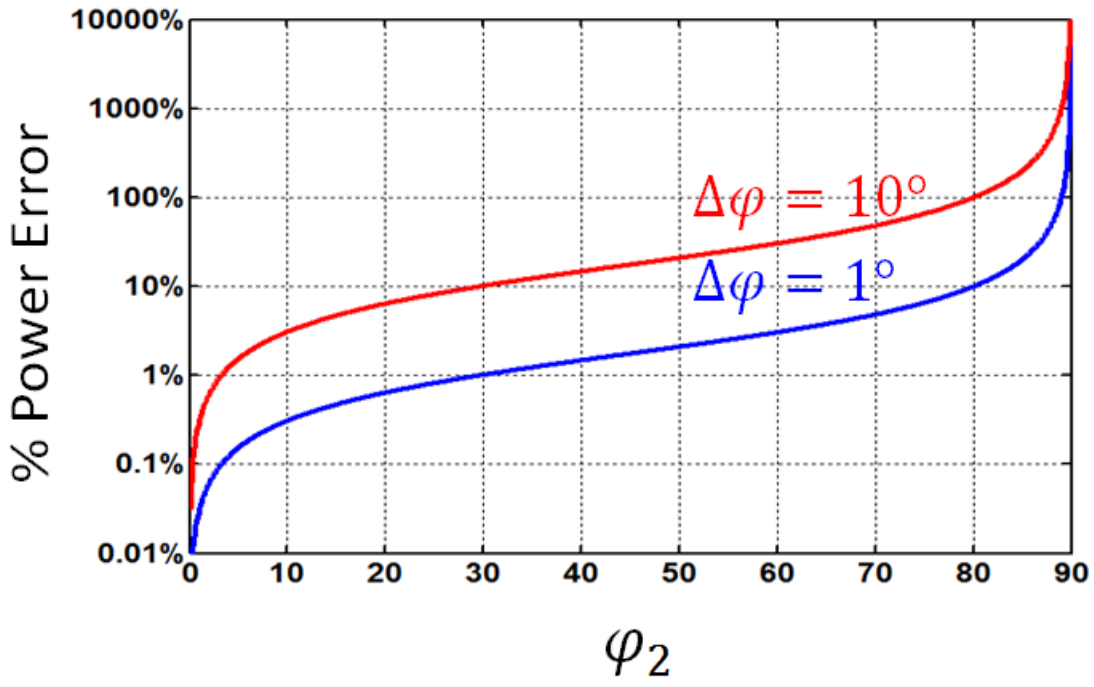


Figure 3.3. The relation between $\boldsymbol{\varphi_2}$ (phase angle between v_2 and i_R) and measurement error for 1° and 10° phase discrepancy.

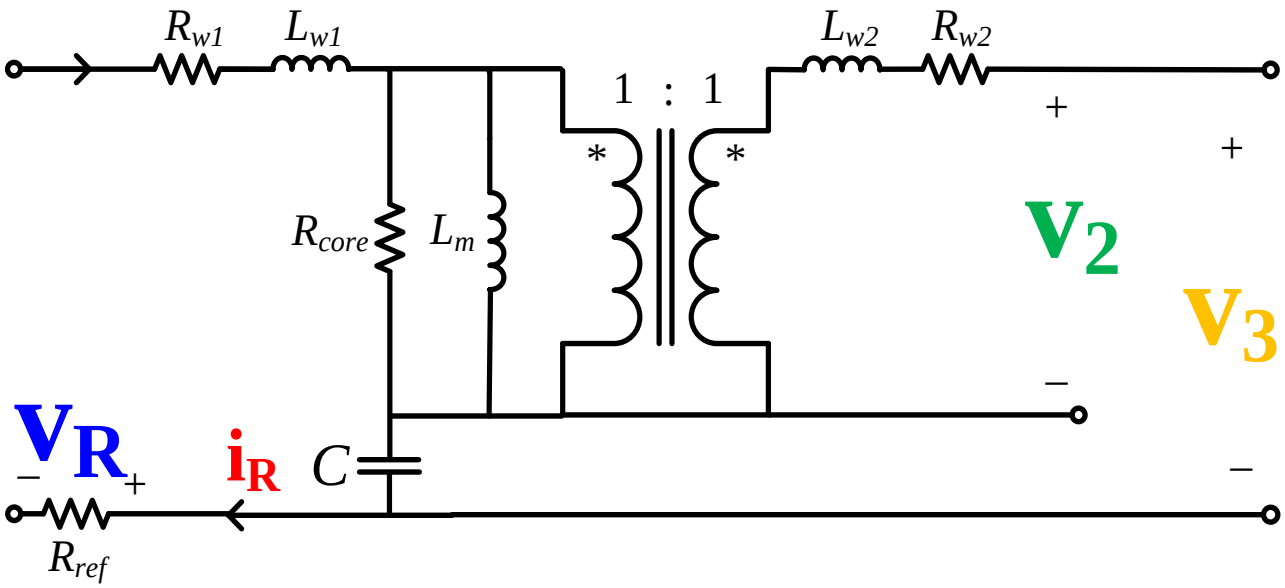


Figure 3.4. Equivalent circuit of Mu's capacitive cancellation method.

To overcome the drawback of the two-winding method, a capacitive cancellation method is proposed by Dr. Mu [110]. The idea is to decrease φ_2 from nearly 90° to nearly 0° by cancelling the reactive voltage of the testing core. The equivalent measurement circuit is shown in Figure 3.4. The cancellation of the reactive voltage is achieved by adding a cancellation capacitor *C* to resonate with the testing core, and by using the voltage across the resonant tank v_3 to calculate core loss (Equ. 2).

$$P_{core} = \frac{f}{R_{ref}} \int_0^T v_3(t) v_R(t) dt \tag{2}$$

where R_{ref} is the current sensing resistance, f is the excitation frequency, and T is the period of the frequency. Using this method, the measurement error Δ caused by the phase discrepancy $\Delta\varphi$ becomes

$$\Delta = \tan(\varphi_3) \cdot \Delta\varphi \tag{3}$$

where φ_3 is the phase angle difference between v_3 and i_R. When the cancellation capacitor exactly resonates with L_m at the excitation frequency, the reactive voltage of the testing core can be perfectly cancelled out, so $\varphi_3 = 0$, and thus an accurate result can be acquired. However, despite the certain tolerable range of the phase angle φ_3 [110], the value of the cancellation capacitor is still critical to the measurement accuracy. The critical capacitance to achieve a perfect cancellation (at excitation frequency $\omega/2\pi$) is

$$C_0 = \frac{1}{\omega^2 L_m}\left[1 + \left(\frac{\omega L_m}{R_{core}}\right)^2\right] \tag{4}$$

And the phase angle φ_3 is

$$\varphi_3 = \arctan\left[\left(1 - \frac{C_0}{C}\right) \cdot tan(\varphi_2)\right] \tag{5}$$

Based on Equ. 5, the relation between φ_3 and the cancellation capacitance C can be plotted in Figure 3.5. It can be seen that a small difference between C and C_0 can lead to a significant jump in φ_3, thus resulting in a big measurement error (according to Equ. 3), especially for low loss magnetic material (whose φ_2 is very close to 90°). Therefore, it is necessary to design and fine-tune the cancellation capacitor for each testing sample at each testing condition (frequency, flux density, temperature, etc.). This is a very time-consuming process and makes the standardization of the measurement instrument almost impossible.

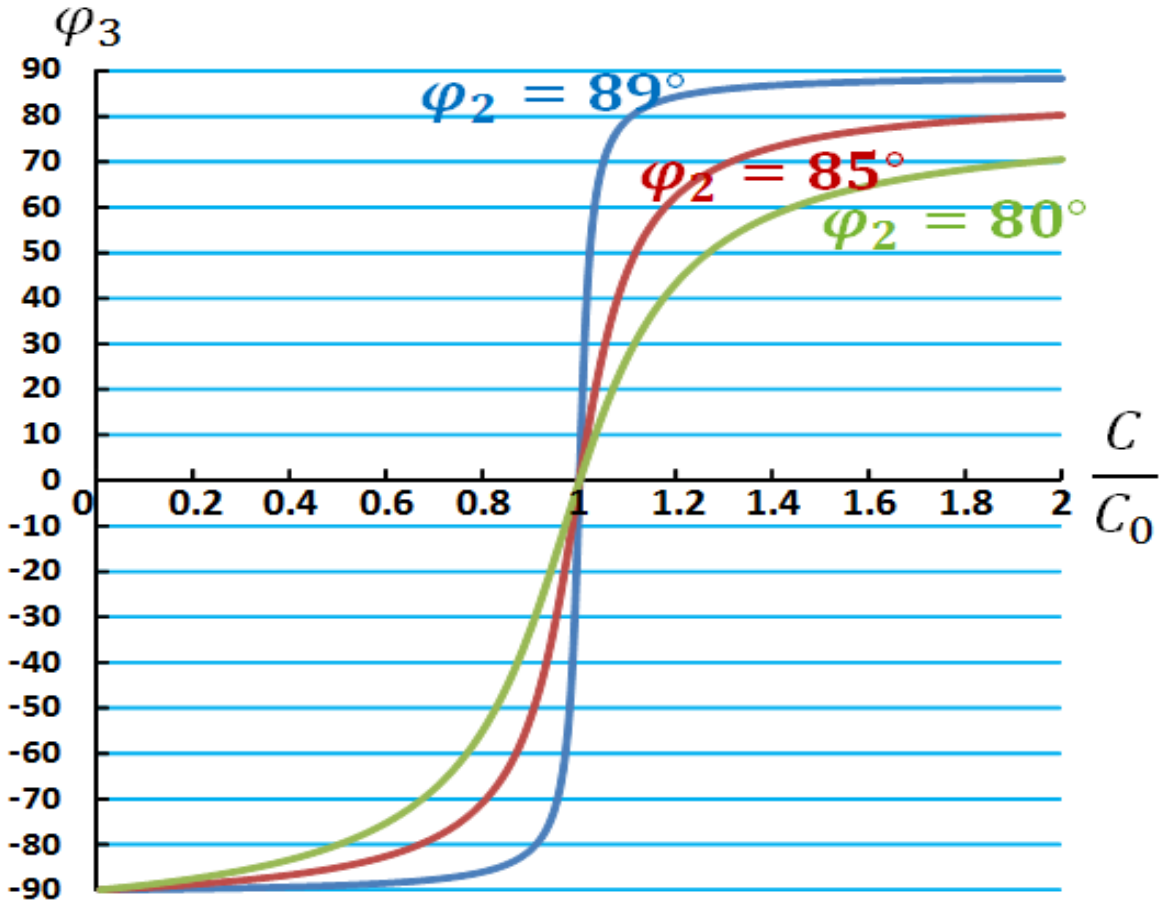


Figure 3.5. The relation between $\boldsymbol{\varphi_3}$ (phase angle between v_3 and i_R) and cancellation capacitance *C* in Mu's capacitive cancellation method. The three curves correspond to three values of $\boldsymbol{\varphi_2}$ (phase angle between v_2 and i_R).

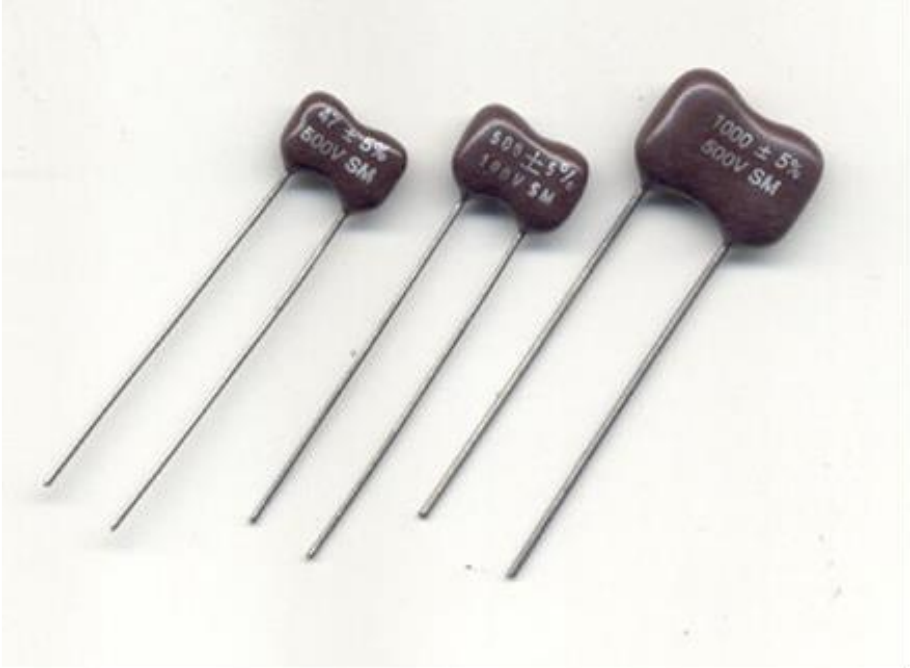


Figure 3.6. Resonant capacitors

The matching of the cancellation component becomes even harder at higher frequencies. The resonant capacitors used to serve as the cancellation component are shown in Figure 3.6. Table 3.1 summarizes the mismatch of the resonant capacitor when matching a sample core with L_m=0.38uH. It can be seen that when the measurement frequency becomes higher and higher in the tens of MHz range, the resonant capacitor becomes smaller and smaller. As a result, the mismatch between the closest catalog capacitor value and the ideal resonant capacitor value becomes larger too. Additionally, the measurement error caused by the mismatch is further enlarged due to the larger phase discrepancy at higher frequencies. Therefore, the mismatch will cause a much more significant measurement error in very high frequency.

Table 3.1. Resonant capacitor mismatch at different frequencies

Frequency	Resonant Capacitor	Closest Catalog Value	Mismatch
5MHz	2670pF	2700pF	1.1%
10MHz	667pF	680pF	1.9%
20MHz	167pF	180pF	7.2%
30MHz	74pF	68pF	8.8%
40MHz	42pF	39pF	7.7%

Dr. Mu's inductive cancellation method[111] is based on the same principle of the aforementioned Dr. Mu's capacitive cancellation method, whereas it uses an inductor instead of a capacitor to cancel the reactive voltage (Figure 3.7), which extends its application range from sinusoidal excitation to arbitrary excitation. Similar to the capacitive cancellation method, the accuracy of this method is also sensitive to the cancellation inductance value L. For sinusoidal excitation, the critical inductance needed to achieve the perfect cancellation is

$$L_0 = L_m \cdot \frac{R_{core}^2}{R_{core}^2 + (\omega L_m)^2} \tag{6}$$

And the phase angle φ_3 is

$$\varphi_3 = \arctan\left[\left(1 - \frac{L}{L_0}\right) \cdot tan(\varphi_2)\right] \tag{7}$$

Similar to the capacitive cancellation method, a small difference between L and L_0 can lead to a significant jump in φ_3 (as shown in Figure 3.8), and thus result in a big measurement error.

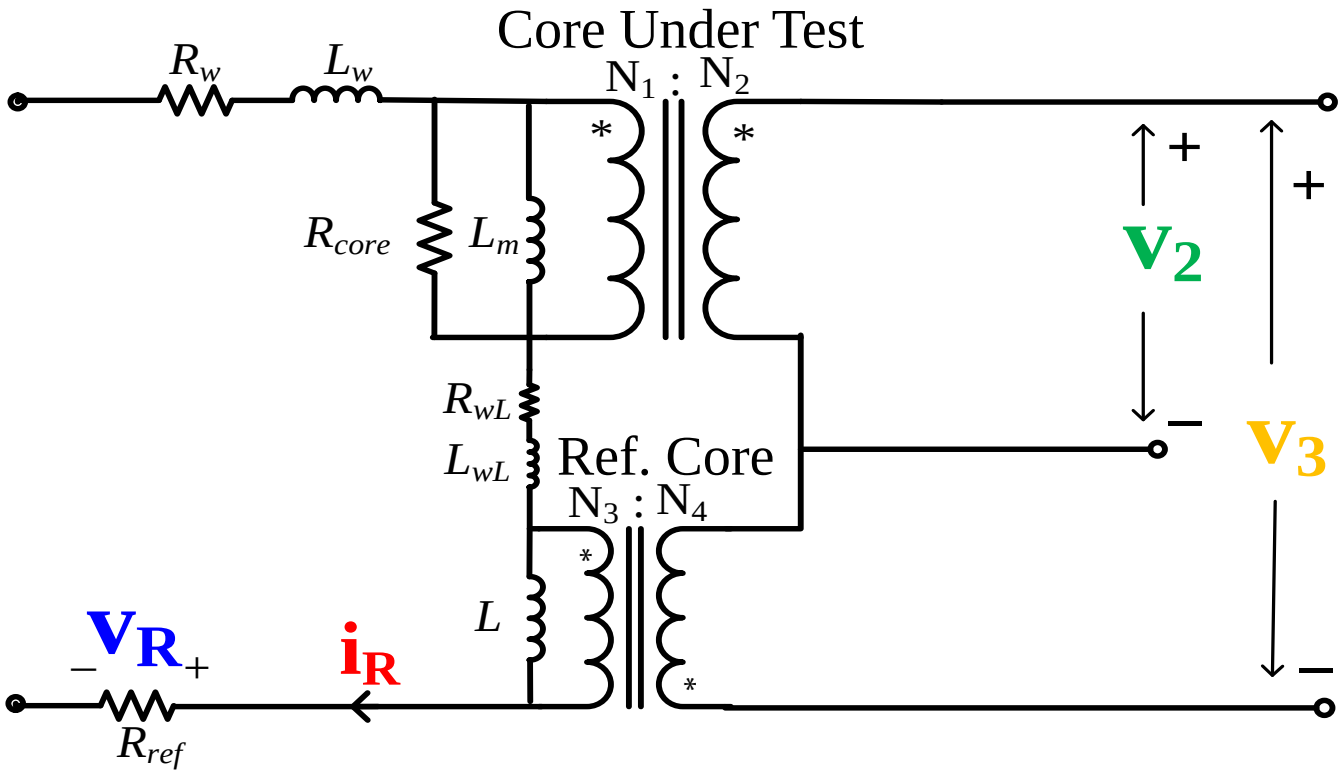


Figure 3.7. Equivalent circuit of Mu's inductive cancellation method. The R_w and L_w correspond to the resistance and leakage inductance of the winding wires of core under test; the R_{wL}, and L_{wL} correspond to the resistance and leakage inductance of the winding wires of reference core.

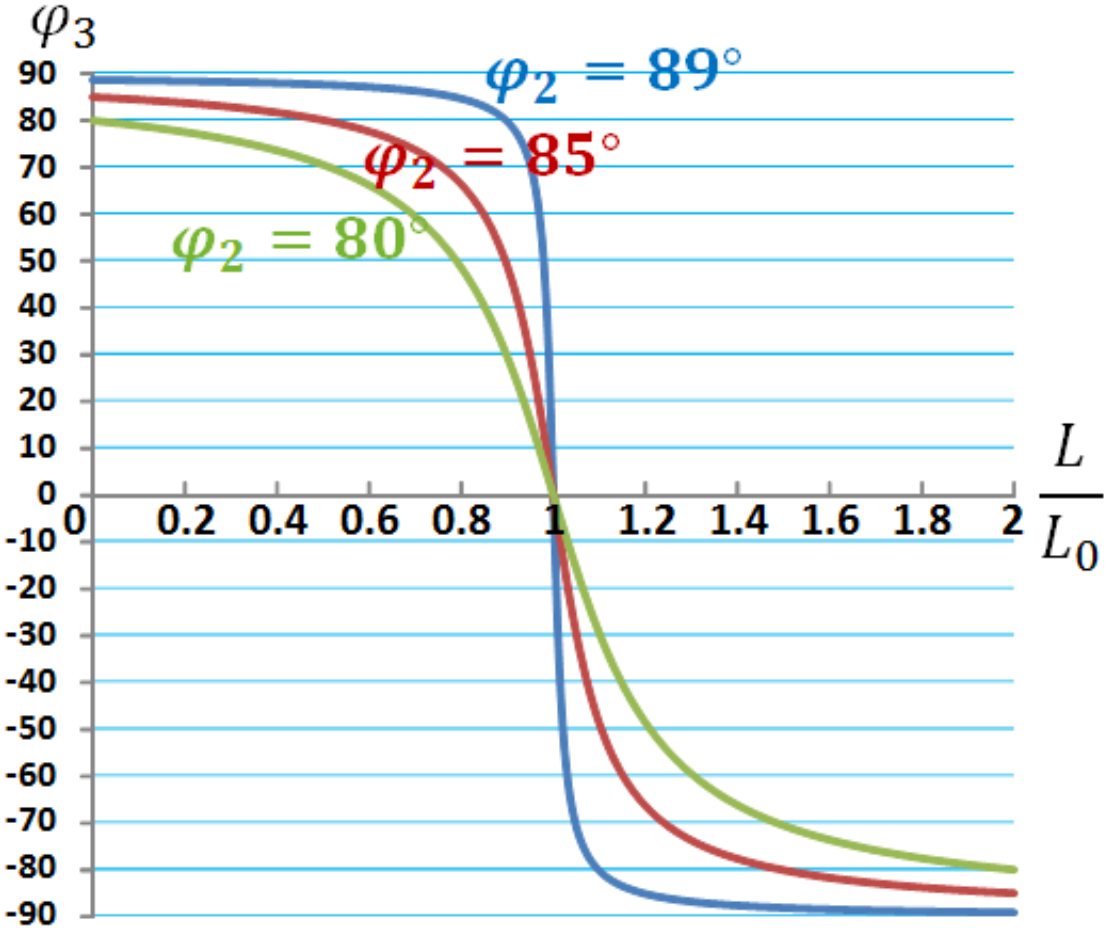


Figure 3.8. The relation between $\boldsymbol{\varphi_3}$ (phase angle between v_3 and i_R) and cancellation inductance L in Mu's inductive cancellation method. The three curves correspond to three values of $\boldsymbol{\varphi_2}$ (phase angle between v_2 and i_R).

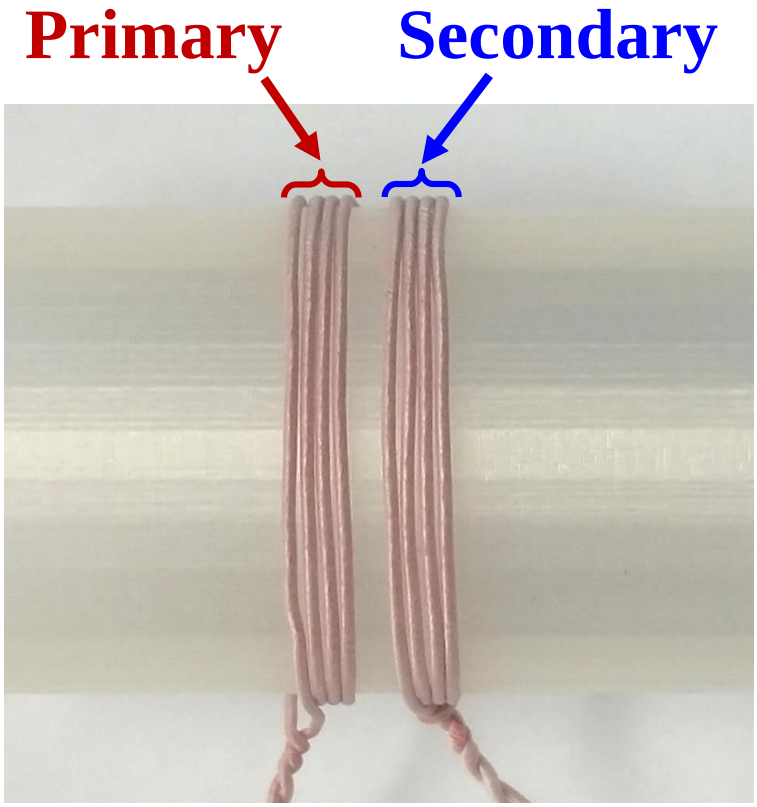


Figure 3.9. Air core transformer

The implementation of the air core transformer is shown in Figure 3.9. To match the magnetizing inductance of the core under test, one need to adjust the turns number and the distance between the primary and the secondary winding of the air core transformer. Again, a precise match is hard to achieve and a small mismatch will cause large measurement error in very high frequency range.

3.2. Proposed measurement techniques for high frequency magnetic characterization

A new method is proposed to overcome the accuracy sensitivity to the cancellation component. The equivalent circuits for both the capacitive and inductive cancellation versions are shown in Figure 3.10. The capacitive cancellation version can only be used for sinusoidal excitation, and the inductive cancellation version is applicable for arbitrary excitation. By comparing Figure 3.10 to Figure 3.4 and Figure 3.7, it can be seen that the proposed method is a better utilization of the similar circuit configuration of Dr. Mu's cancellation method, whereas the voltage across the cancellation component (v_L or v_C) is measured instead of v_3 to implement the partial cancellation concept. The working principle of both the inductive and capacitive cancellation version will be demonstrated and analyzed in the following discussion.

Let us consider the inductive cancellation version under sinusoidal excitation first. In the proposed method, three parameters are measured: i_R (by measuring v_R), v_2 and v_L. So three types of phase discrepancy may be involved in the measurement: $\Delta\varphi_i$ (phase discrepancy between measured v_R and real i_R), $\Delta\varphi_2$ (phase discrepancy between measured v_2' and real v_2), and $\Delta\varphi_L$ (phase discrepancy between measured v_L' and real v_L). We will analyze them in two steps.

Step 1: consider $\Delta\varphi_i$ only (assuming $\Delta\varphi_2 = \Delta\varphi_L = 0$).

At an excitation frequency of $\omega/2\pi$, we have

$$i_R = I_R \cdot sin(\omega t) \tag{8}$$

$$v_2 = V_2 \cdot sin(\omega t + \varphi_2) \tag{9}$$

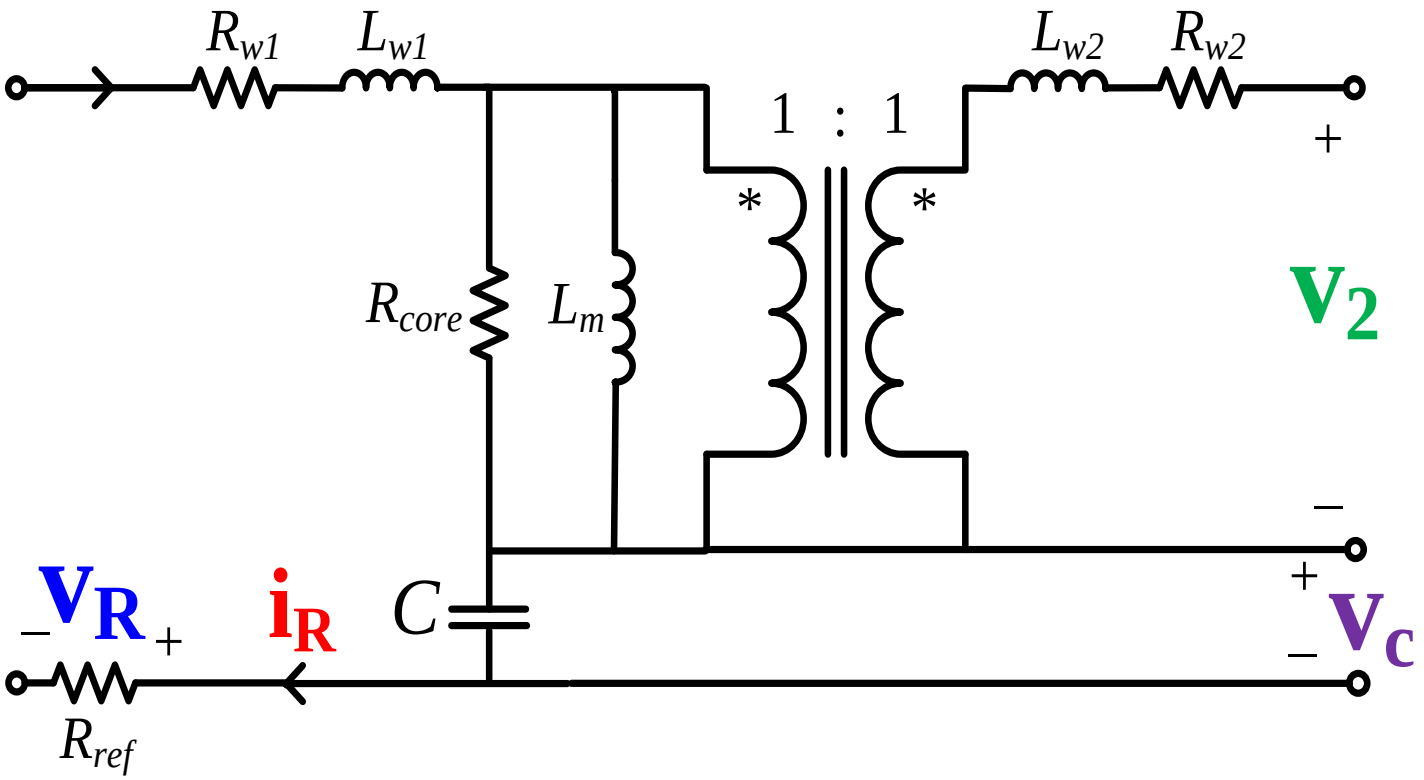
$$v_L = V_L \cdot \sin(\omega t + 90°) \tag{10}$$

According to ref. [118], the measured loss of the core under test is

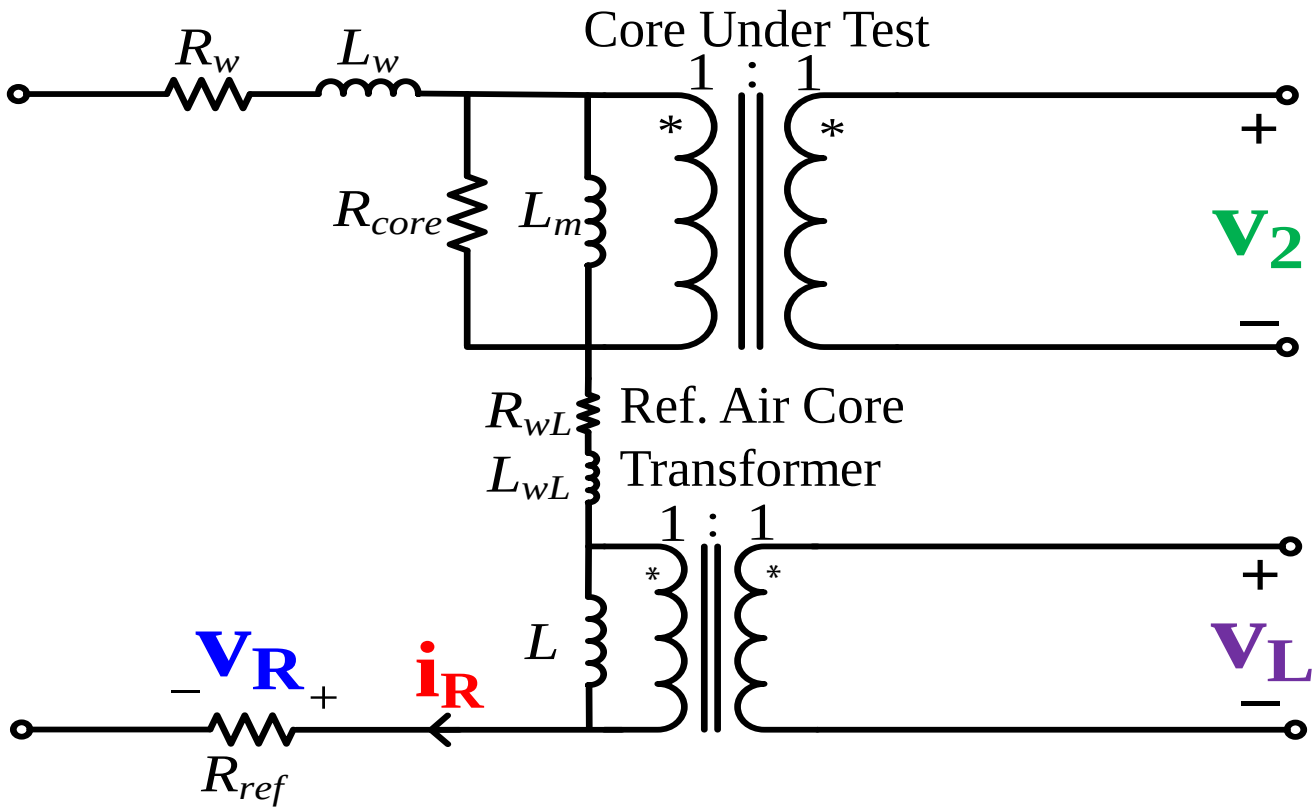
$$\frac{f}{R_{ref}}\int_0^T v_2 v_R dt = P_{core} + \Delta P_{core} = P_{core} + V_2 \cdot sin\varphi_2 \cdot I_R \cdot \Delta\varphi_i \tag{11}$$

where P_{core} is the real core loss and ΔP_{core} is the error caused by $\Delta\varphi_i$. Similarly, the measured power loss of the reference air core is

$$\frac{f}{R_{ref}}\int_0^T v_L v_R dt = V_L \cdot I_R \cdot \cos(90°) + V_L \cdot I_R \cdot \sin(90°) \cdot \Delta\varphi_i = V_L \cdot I_R \cdot \Delta\varphi_i \tag{12}$$



(a)



(b)

Figure 3.10. Equivalent circuit of proposed method. (a): capacitive cancellation; (b): inductive cancellation.

The result of Equ. 12 is proportional to the error in Equ. 11 (ΔP_{core}), with the proportion of

$$k = \frac{V_L}{V_2 \cdot sin\varphi_2} \tag{13}$$

This *k* factor is named *cancellation factor*, which represents the percentage of cancelled reactive voltage to the total reactive voltage.

Combining Equ. 11, 12, and 13, we can get the real core loss as

$$P_{core} = \frac{f}{R_{ref}} \int_0^T v_2 v_R dt - \frac{1}{k} \frac{f}{R_{ref}} \int_0^T v_L v_R dt \tag{14}$$

Then the remaining problem is how to find the cancellation factor k. The difficulty in finding k is that $V_2 \cdot sin\varphi_2$ cannot be measured out directly. Here we propose a method to find k by adding a phase perturbation $\Delta\varphi_i'$ into v_R with the de-skew function of the oscilloscope, as shown in Figure 3.11. The de-skew function is originally designed to compensate the propagation delay inherent in connecting cables and probes. However, the value of the phase discrepancy is unknown, so it cannot be easily eliminated by a certain de-skew value. In the proposed method shown below, we do not require a specific de-skew value to compensate the phase discrepancy. Instead, a relative arbitrary de-skew value can be used to find the cancellation factor *k*, so that the error caused by the phase discrepancy can be eliminated.

If we call the measured voltage of the current sensing resistor after the phase perturbation as v_R', we have

$$P_{core} = \frac{f}{R_{ref}} \int_0^T v_2 v_R' dt - \frac{1}{k} \frac{f}{R_{ref}} \int_0^T v_L v_R' dt \tag{15}$$

Combining Equ. 14 and 15, we have

$$k = \frac{\int_0^T v_L v_R' dt - \int_0^T v_L v_R dt}{\int_0^T v_2 v_R' dt - \int_0^T v_2 v_R dt} \tag{16}$$

After *k* is known, Equ. 14 can be used to extract the real core loss of the testing core.

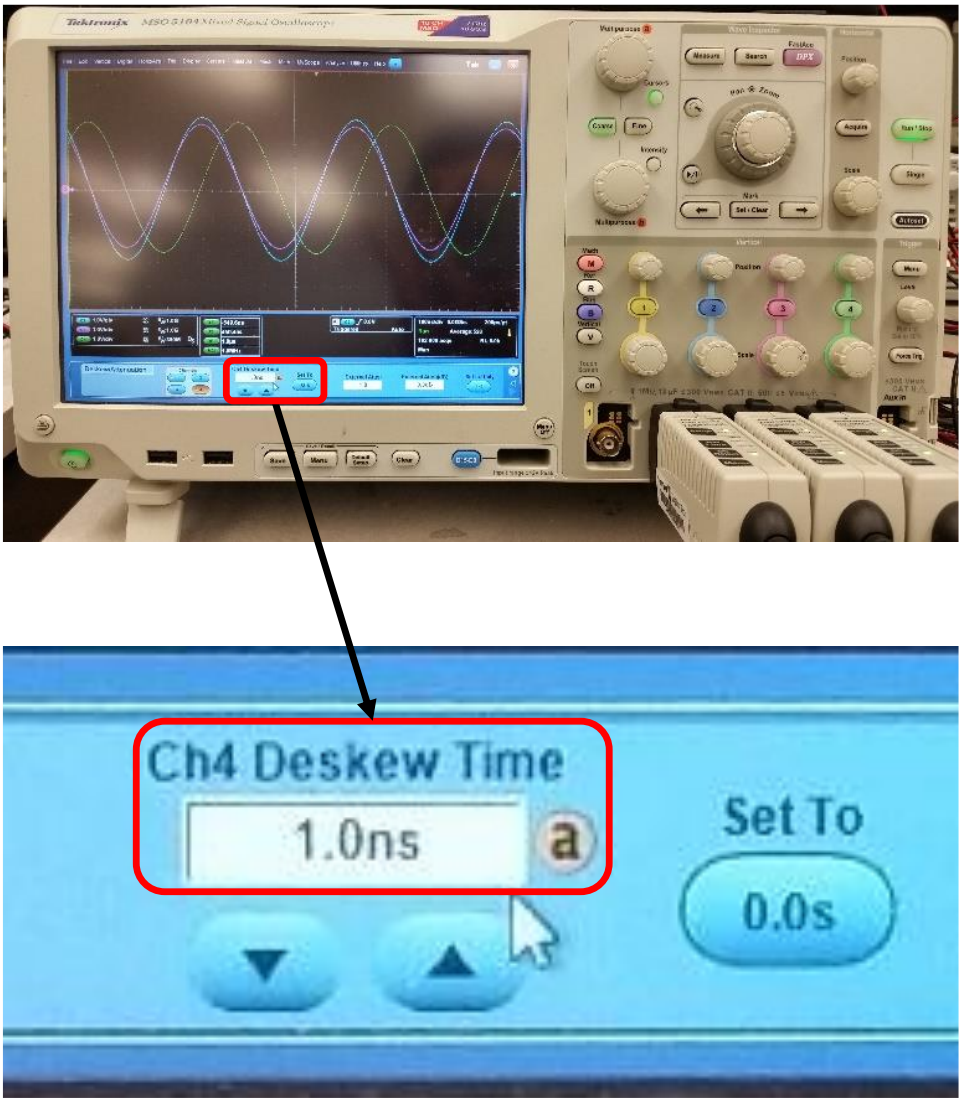


Figure 3.11. De-skew function in oscilloscope

To make a proper choice of $\Delta\varphi_i'$, two factors should be considered: 1) it should be a small perturbation to validate the linear approximation; 2) a too small value should also be avoided because the difference before and after the perturbation is used to calculate k in Equ. 16. In our measurement, we found that $\Delta\varphi_i' \approx 1°$ can be a proper choice.

Step 2: Consider all three phase discrepancy ($\Delta\varphi_i$, $\Delta\varphi_2$, $\Delta\varphi_L$) together (now the measured voltages are v_2', v_L', and v_R).

Following the same procedure in step 1, we can derive

$$\frac{f}{R_{ref}}\int_0^T v_2' v_R dt - \frac{1}{k}\frac{f}{R_{ref}}\int_0^T v_L' v_R dt = P_{core} + V_2 \cdot sin\varphi_2 \cdot I_R \cdot (\Delta\varphi_2 - \Delta\varphi_L) \tag{17}$$

The results show that there exists a measurement error of $[V_2 \cdot sin\varphi_2 \cdot I_R \cdot (\Delta\varphi_2 - \Delta\varphi_L)]$. The error comes from the remaining phase discrepancy$(\Delta\varphi_2 - \Delta\varphi_L)$, which is caused by the phase mismatch between the two probes for v_2 and v_L. To diminish this error, we can use the two probes to measure the same voltage v_2 simultaneously (so that two v_2' are generated by the two probes), and then observe the integration of $\frac{f}{R_{ref}}\int_0^T v_2' v_R dt$ calculated by each of them. The integration result from the two probes are $[P_{core} + V_2 \cdot sin\varphi_2 \cdot I_R \cdot (\Delta\varphi_i + \Delta\varphi_2)]$ and $[P_{core} + V_2 \cdot sin\varphi_2 \cdot I_R \cdot (\Delta\varphi_i + \Delta\varphi_L)]$, so the difference between them is $[V_2 \cdot sin\varphi_2 \cdot I_R \cdot (\Delta\varphi_2 - \Delta\varphi_L)]$, which is the same as the error involved in the measurement result. Then by adjusting $\Delta\varphi_2$ or $\Delta\varphi_L$ using the de-skew function, the difference between the two integration results from the two probes can be diminished, and thus the measurement error is diminished too.

For the inductive cancellation version under rectangular excitation, according to the analysis in [119], the previous Equ. 11, 12, and 13 for sinusoidal excitation become the following equations:

$$\frac{f}{R_{ref}}\int_0^T v_2 v_R dt = P_{core} + \frac{V_{2pp} I_{pp} \Delta t}{T} \tag{18}$$

$$\frac{f}{R_{ref}}\int_0^T v_L v_R dt = \frac{V_{Lpp} I_{pp} \Delta t}{T} \tag{19}$$

$$k = \frac{V_{Lpp}}{V_{2pp}} \tag{20}$$

where Δt is a small time delay caused by phase discrepancy, I_{pp} is the peak-to-peak value of magnetizing current, V_{2pp} and V_{Lpp} is the peak-to-peak value of V_2 and V_L shown in Figure 3.10(b). Then the same procedure discussed above for sinusoidal excitation can be applied to rectangular excitation.

For the capacitive cancellation version, it works in the same principle as the inductive cancellation version under sinusoidal excitation, while the previous Equ. 10, and Euqs. 12-16 become the following equations:

$$v_C = V_C \cdot \sin(\omega t - 90°) \tag{21}$$

$$\frac{f}{R_{ref}} \int_0^T v_C v_R dt = V_C \cdot I_R \cdot \cos(90°) + V_C \cdot I_R \cdot \sin(-90°) \cdot \Delta\varphi_i = -V_C \cdot I_R \cdot \Delta\varphi_i \tag{22}$$

$$k = \frac{V_C}{V_2 \cdot sin\varphi_2} \tag{23}$$

$$P_{core} = \frac{f}{R_{ref}} \int_0^T v_2 v_R dt + \frac{1}{k} \frac{f}{R_{ref}} \int_0^T v_C v_R dt \tag{24}$$

$$P_{core} = \frac{f}{R_{ref}} \int_0^T v_2 v_R' dt + \frac{1}{k} \frac{f}{R_{ref}} \int_0^T v_C v_R' dt \tag{25}$$

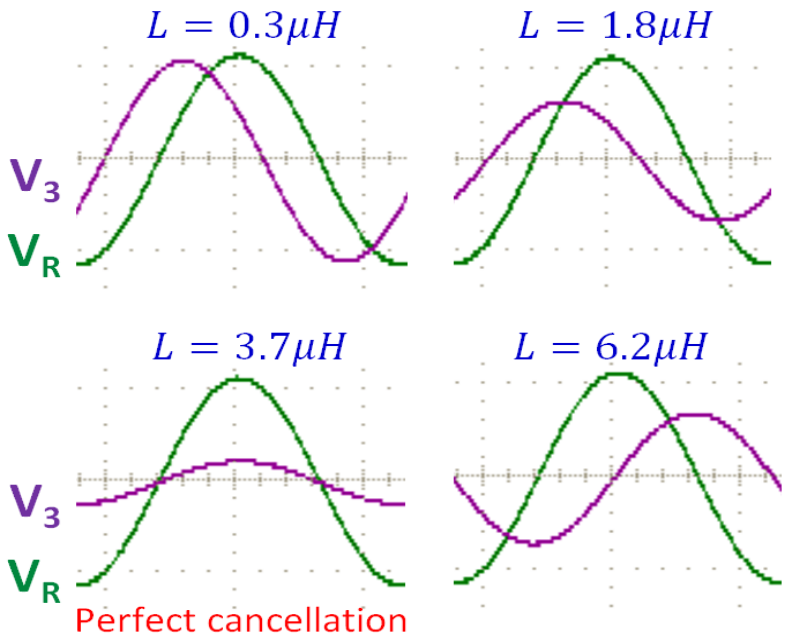
$$k = \frac{\int_0^T v_C v_R dt - \int_0^T v_C v_R' dt}{\int_0^T v_2 v_R' dt - \int_0^T v_2 v_R dt} \tag{26}$$

And the discussion in step 2 about diminishing the error caused by phase discrepancy between $\Delta\varphi_2$ and $\Delta\varphi_L$ holds the same for the phase discrepancy between $\Delta\varphi_2$ and $\Delta\varphi_C$ in the capacitive cancellation version.

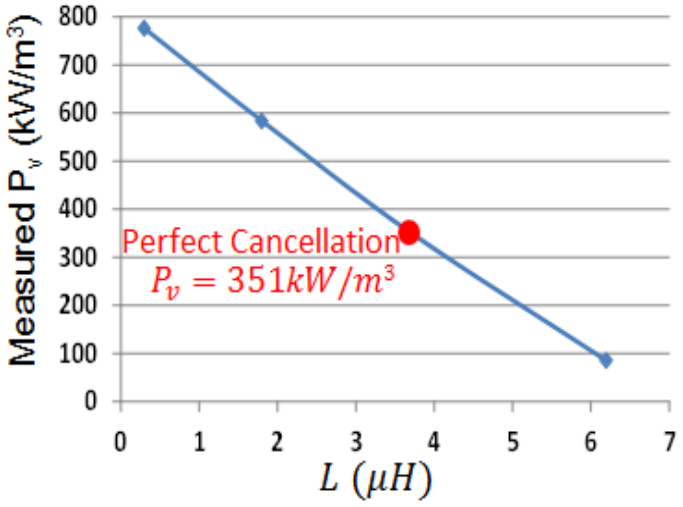
In another point of view, the effect of partial cancellation mechanism can be regarded as to create a virtual voltage measurement of $v_3 = v_2 - \frac{1}{k}v_L$ (for inductive cancellation) and $v_3 = v_2 + \frac{1}{k}v_C$ (for capacitive cancellation) to replace the initial $v_3 = v_2 - v_L$(for inductive cancellation) and $v_3 = v_2 + v_C$ (for capacitive cancellation) in Mu's cancellation method. As a result, the effective φ_3 can stay close to zero even when the cancellation component value *L* or *C* has a mismatch with its critical value L_0 or C_0 (in contrast to the significant jump of φ_3 shown in Figure 3.5 and Figure 3.8). Consequently, the measurement error can be minimized.

It is worth mentioning that the proposed method is applicable not only to the core loss measurement, but also to the total inductor loss measurement. By simply replacing the core under test with an inductor, and using the v_2 probe to measure the voltage across the inductor (with everything else kept the same), the measurement result will provide the total inductor loss including core loss and winding loss.

To verify the proposed method, the core loss of a 3F4 ferrite toroid core from Ferroxcube (TN10/6/4) is measured under sinusoidal excitation with a 2MHz frequency, a 20mT peak flux density, and 100ºC. The excitation voltage is supplied by a power amplifier (Amplifier Research® 25A250A) driven by a function generator (Tektronix AFG3102). The Tektronix TDP1000 differential probe is used to sense the voltage signal. The core loss is first measured using Mu's inductive cancellation method with a different cancellation inductance value *L*. The waveform and measurement result is shown in Figure 3.12. It shows that the measurement result is sensitive to the cancellation inductance value *L*. The perfect cancellation (v_3 and v_R in phase) is achieved at *L*=3.7uH, and the accurate core loss density is 351kW/m^3. Then the core loss is measured using the proposed method. The working waveform and corresponding result is shown in Figure 3.13. It shows that the measurement result with a different *L* can all match the accurate result from Dr. Mu's inductive cancellation method at the perfect cancellation condition (with an error $\Delta \leq 3\%$).



(a) Working waveform. v_3 in 5V/div, v_R in 50mV/div.



(b) Measurement result

Figure 3.12. Working waveform and measurement result using Mu's inductive cancellation method for sinusoidal wave excitation.

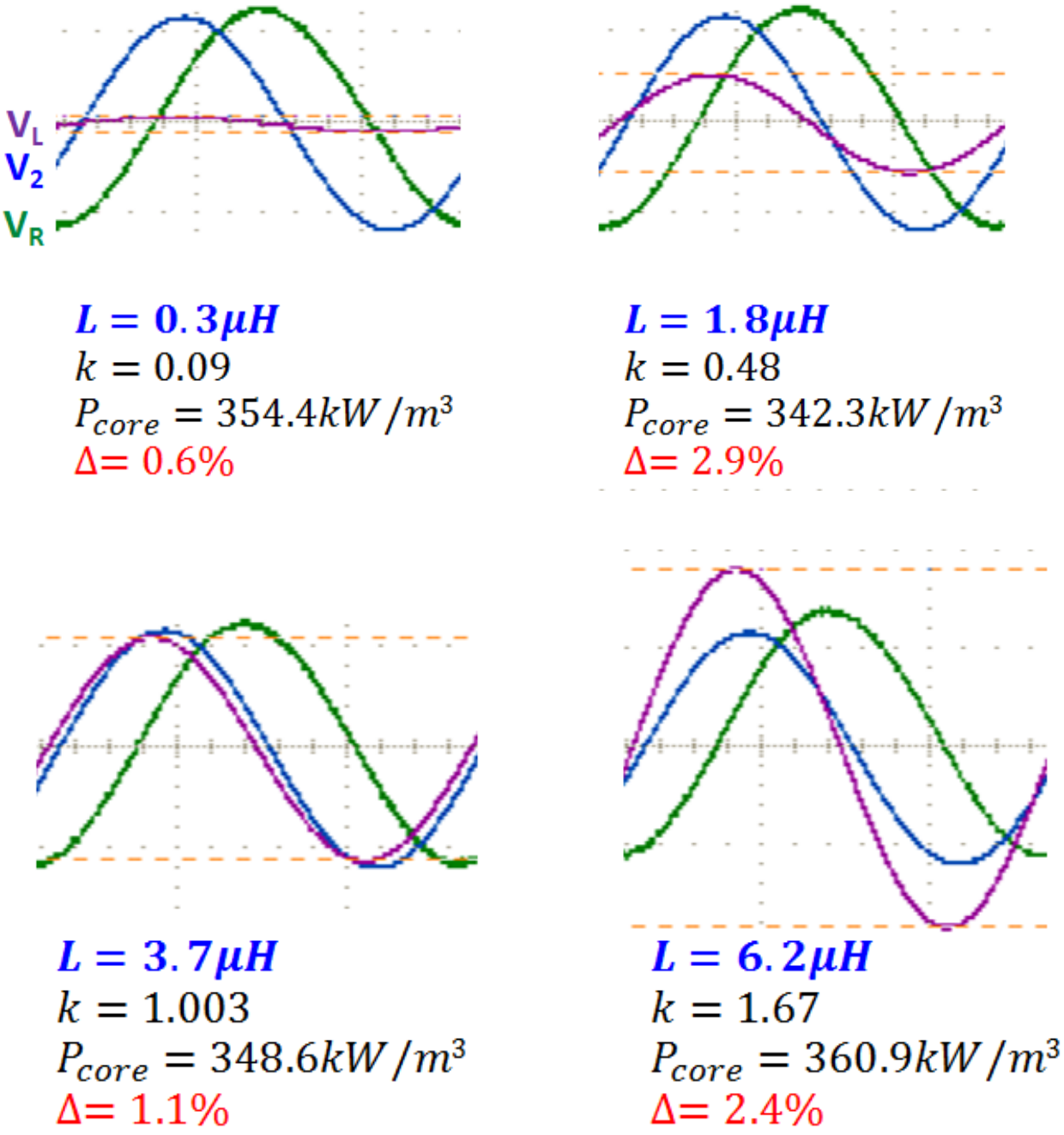


Figure 3.13. Working waveform and measurement result using proposed method for sinusoidal wave excitation. v_2 and v_L in 5V/div, v_R in 50mV/div.

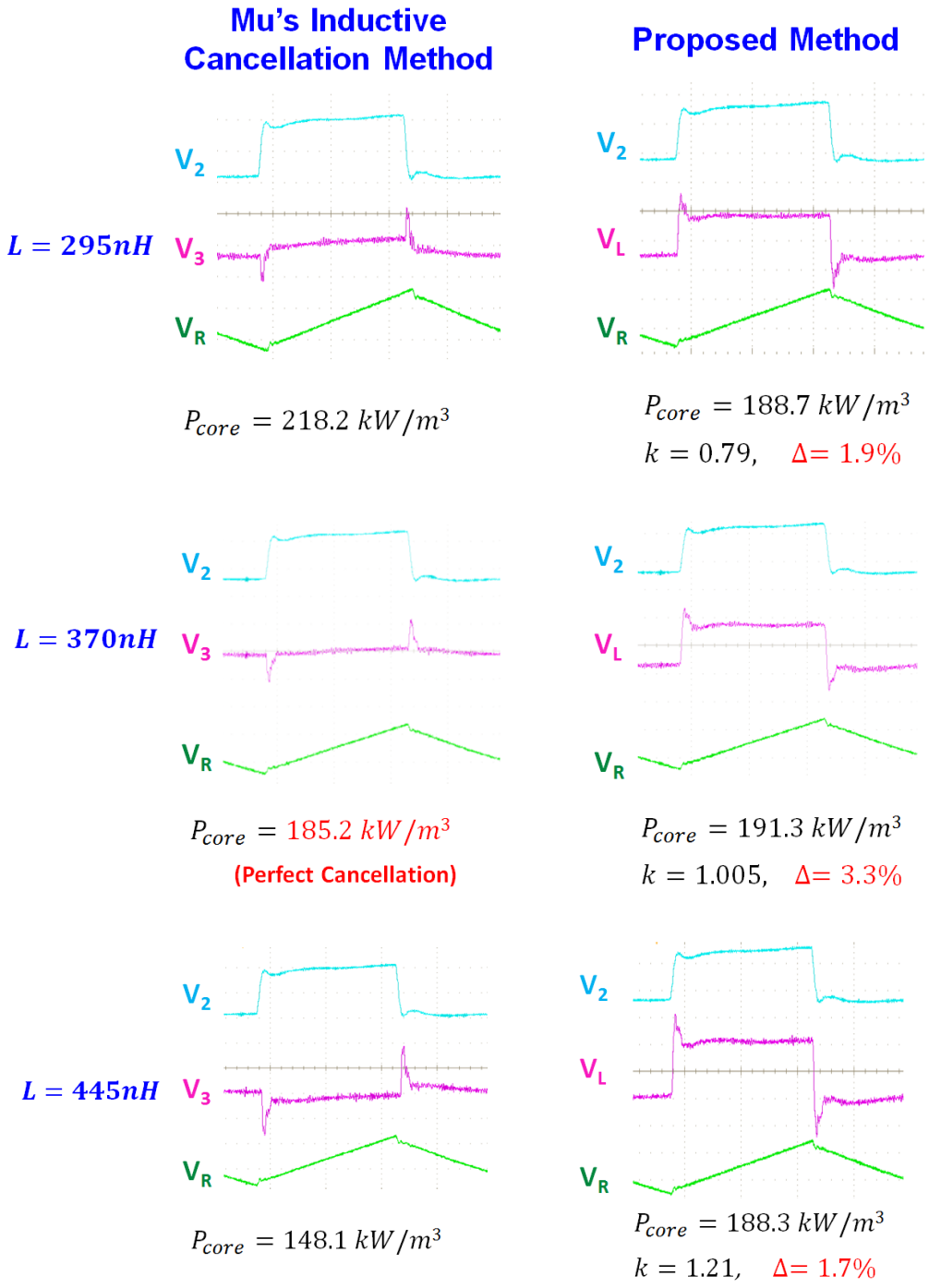
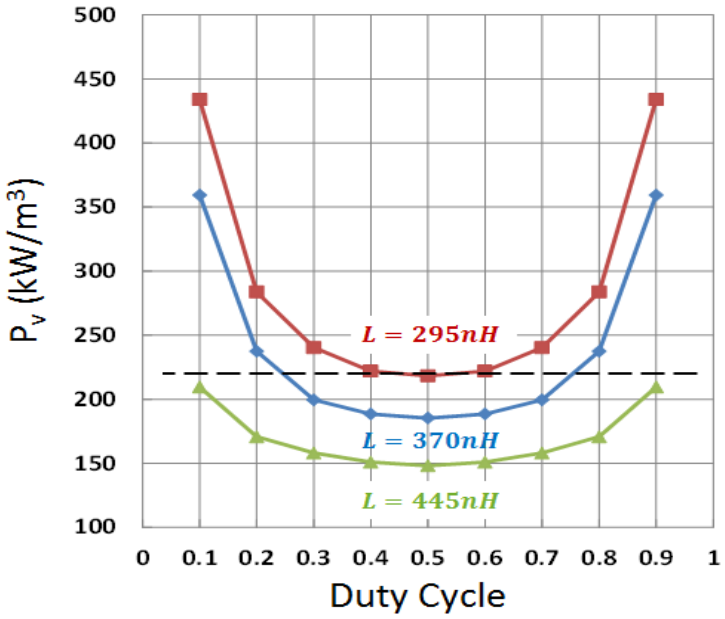
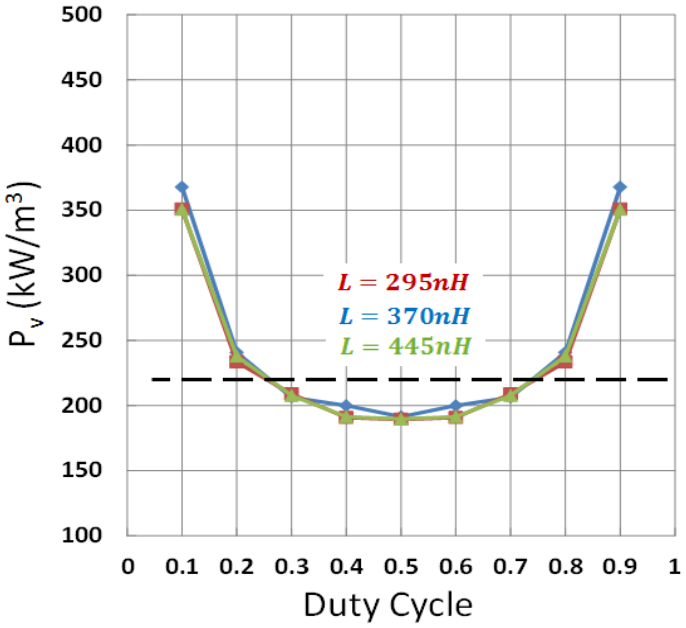


Figure 3.14. Working waveform and measurement result using Mu's inductive cancellation method and proposed method for rectangular wave excitation with 50% duty cycle. v_2, v_3 and v_L in 0.8V/div, v_R in 0.1V/div.

For the rectangular wave excitation, the core loss of an iron powder material -52 from Micrometals, Inc. is measured at 0.5MHz, with a 10mT peak flux density, and room temperature. The working waveform and measurement results using Mu's inductive cancellation method and proposed method are shown in Figure 3.14 and the measurement results using Mu's cancellation method and the proposed method is summarized in Figure 3.15. It can be seen that the proposed method can effectively overcome the accuracy sensitivity to the *L* value shown in Mu's inductive cancellation method. Furthermore, the core loss of 3F35, 3F4, and 3F45 ferrites from Ferroxcube are also measured using the proposed method under the rectangular excitation, and the results are summarized in Figure 3.16.



(a) Measurement result using Mu's cancellation method



(b) Measurement result using proposed method

Figure 3.15. Summary of measurement result for rectangular excitation with different duty cycle. The dashed line indicates the result for sinusoidal excitation.

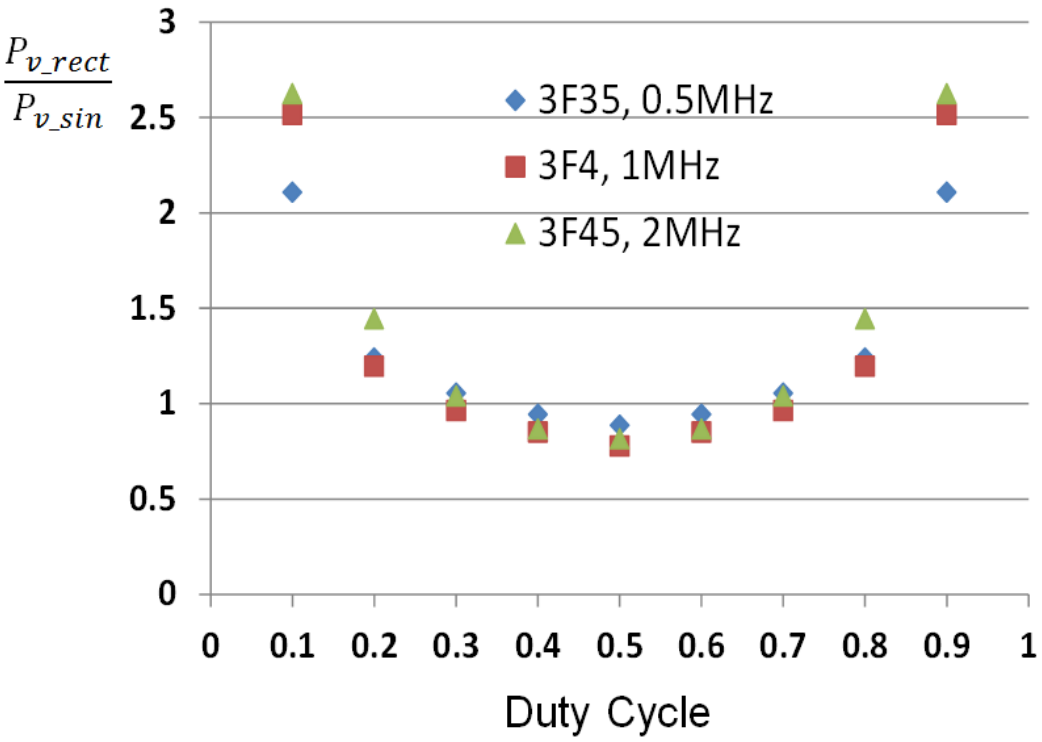


Figure 3.16. Measured core loss of 3F35 (B=50mT), 3F4 (B=40mT), and 3F45 (B=20mT).

To ensure the accuracy of the proposed measurement method, it is necessary to identify and analyze various error sources in the system, including amplitude discrepancy, phase discrepancy, parasitic capacitance, component tolerance, etc. They will be analyzed respectively in the following paragraphs.

For the amplitude discrepancy, the oscilloscope used in the measurement (Tektronix MSO5104) has an 8-bit resolution for an analog-to-digital (ADC) conversion. Considering the ADC digitizing error of $\pm 1/2$ least significant bit (LSB), the measurement error caused by the amplitude discrepancy is $\pm 0.196\%$. Moreover, the amplitude sensing error of the voltage probe is minimized by the Tektronix calibration fixture: 067-1686-00, and the random error in the measurement is further reduced by taking the average value of a large sampling number.

The amplitude measurement discrepancy can also cause an error in the measurement of the cancellation factor k in Equ. 16, especially when two different data sets are acquired before and after the de-skew process in the oscilloscope. But this error can be reduced by an alternative (and also more convenient) way of performing the de-skew process: instead of using the oscilloscope's de-skew function, one can save all the testing data of v_2, v_L, and v_R in a computer, and then use a simple computer program to perform the effective de-skew (i.e. a small phase shift) of v_R to get v_R'. In this way, the v_R and v_R' data used in the k calculation comes from a single data acquisition, and thus their amplitude discrepancy will cancel out in the numerator and denominator in Equ. 16. Therefore, it is safe to ignore the impact from v_R and in the worst case the error can be calculated by Equ. 27, which is less than 0.4%.

$$\frac{\Delta k}{k} = \left| \frac{\dfrac{\int_0^T v_L(1 \pm 0.196\%)v_R' dt - \int_0^T v_L(1 \pm 0.196\%)v_R dt}{\int_0^T v_2(1 \pm 0.196\%)v_R' dt - \int_0^T v_2(1 \pm 0.196\%)v_R dt}}{\dfrac{\int_0^T v_L v_R' dt - \int_0^T v_L v_R dt}{\int_0^T v_2 v_R' dt - \int_0^T v_2 v_R dt}} - 1 \right| = 0.39\% \tag{27}$$

For phase discrepancy, the source of it in the measurement system includes the ESL of the current sensing resistor, the phase mismatch between the voltage probes, and the scope sampling resolution limit (a detailed procedure of evaluating phase discrepancy is described in [120]). With the partial cancellation mechanism demonstrated above, it is safe to have <1% measurement error due to the phase discrepancy, which is not a significant contributor to the overall error.

For the parasitic capacitance, the source of it in the measurement system includes a transformer intra-winding capacitance, a transformer inter-winding capacitance, and a voltage probe input capacitance.

Figure 3.17(a) shows the simplified equivalent circuit with C_p (the total parasitic capacitance of the core under test, including transformer's intra-winding capacitance and v_2 probe's input capacitance). The existence of C_p causes an extra current flowing through it, and thus introduces a voltage drop on the sensing winding's parasitic L_2 and R_2. To quantify the error caused by the parasitic capacitance, we assume

$$R_{core} \ll \omega L_m \tag{28}$$

$$\omega L_m \ll \frac{1}{\omega C_p} \tag{29}$$

$$R_1, R_2, \omega L_1, \omega L_2 \ll \frac{1}{\omega C_p} \tag{30}$$

Under these assumptions, the error percentage can be approximated as

$$\Delta_{C_p} = \frac{P_{measured} - P_{actual}}{P_{actual}} = \frac{\int v_2 i_R \, dt - \frac{1}{k}\int v_L i_R dt - \int v_m i_{core} dt}{\int v_m i_{core} dt}$$

$$\approx C_p \left(\frac{R_2 R_{core}}{L_m} + \omega^2 L_2 \right) \tag{31}$$

In the measurement example of 3F4 shown before, C_p≈8pF, L_m≈3.7μH, L_2≈100nH, R_2≈0.1Ω, ω=2π ·2MHz, and R_{core}≈4.9kΩ, so Δ_{C_p}≈0.12%.

Besides C_p, the transformer inter-winding capacitance C_w can also cause an extra current and introduce a measurement error, as shown in Figure 3.17(b).

Assume that

$$R_{core} \ll \omega L_m \tag{32}$$

$$\omega L_m \ll \frac{1}{\omega C_w} \tag{33}$$

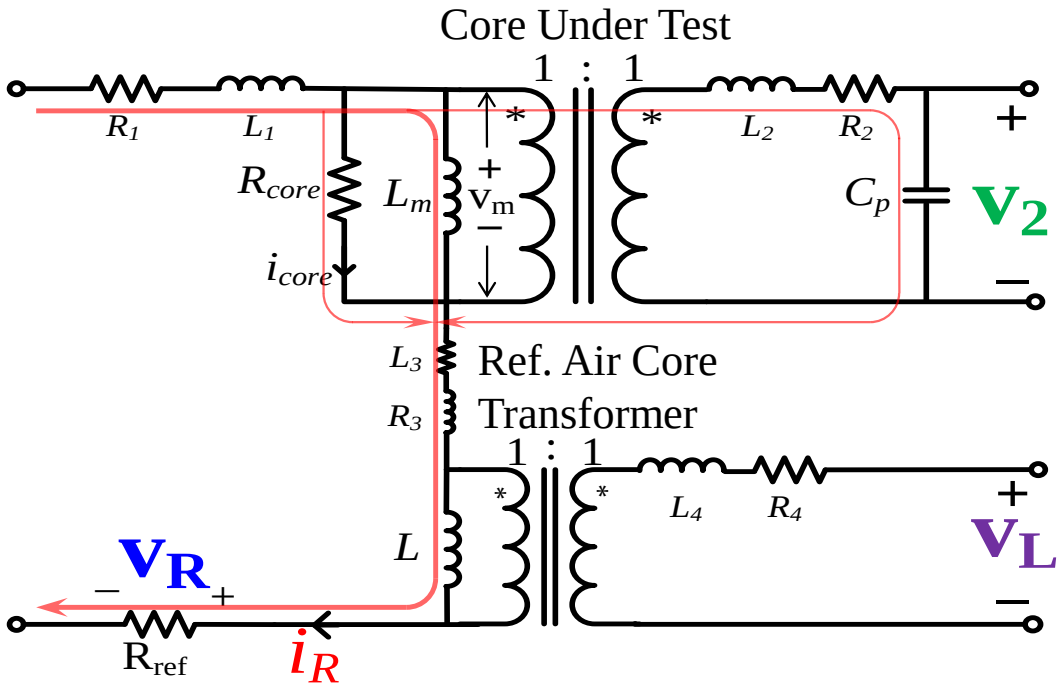
$$R_1, R_2, \omega L_1, \omega L_2 \ll \frac{1}{\omega C_w} \tag{34}$$

The error caused by C_w can be simplified as

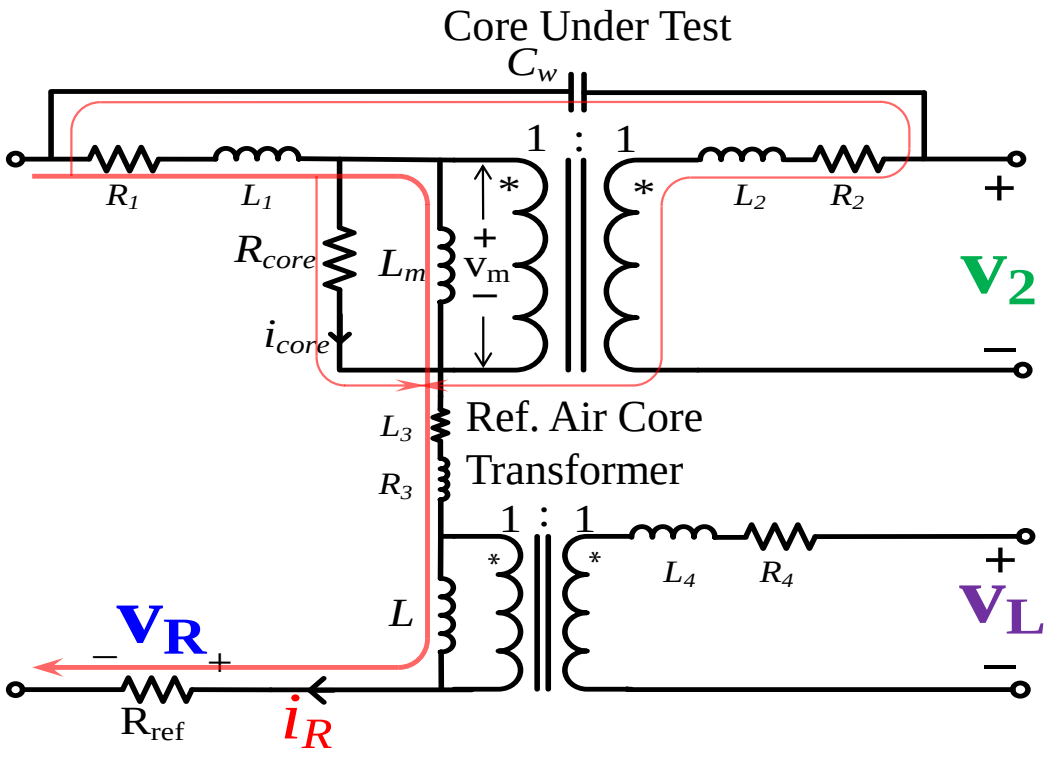
$$\Delta_{C_w} = \frac{P_{measured} - P_{actual}}{P_{actual}} = \frac{\int v_2 i_R \, dt - \frac{1}{k}\int v_L i_R dt - \int v_m i_{core} dt}{\int v_m i_{core} dt}$$

$$\approx -\frac{R_{core} C_w}{L_m^2}(R_1 L_2 + R_2 L_1) \tag{35}$$

For the aforementioned measurement example, C_w≈15pF, L_m≈3.7μH, R_1≈R_2≈0.1Ω, L_1≈L_2≈100nH, and R_{core}≈4.9kΩ, so Δ_{C_w}≈−0.011%.



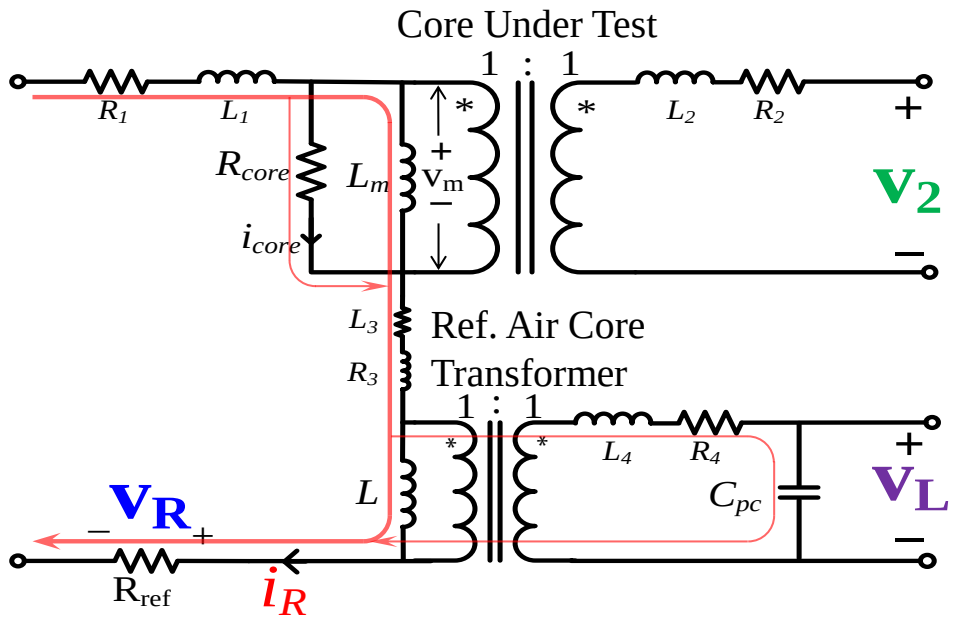
(a)



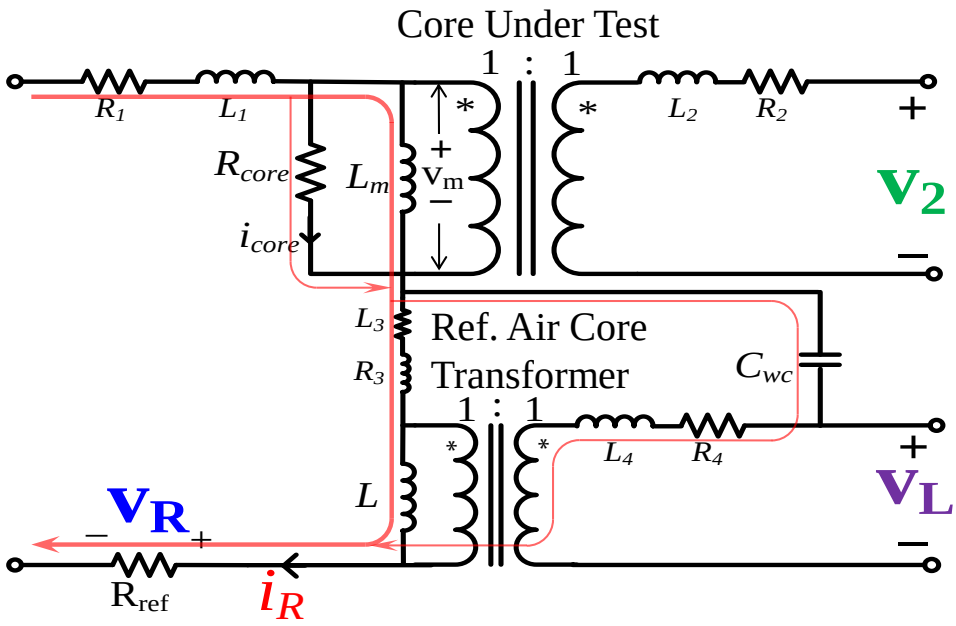
(b)

Figure 3.17. Simplified equivalent circuit with parasitic capacitance associated with the core under test. (a) with parallel capacitance C_p; (b) with transformer inter-winding capacitance C_w.

Besides the parasitic capacitance of the core under test, the parasitic capacitance associated with the reference core C_{pc} and C_{wc} are also be considered as shown in Figure 3.18.



(a)



(b)

Figure 3.18. Simplified equivalent circuit with parasitic capacitance associated with the reference air core transformer. (a)with parallel capacitance C_p; (b)with transformer inter-winding capacitance C_w.

Assume that

$$\omega L \ll \frac{1}{\omega C_{pc}} \tag{36}$$

$$\omega L \ll \frac{1}{\omega C_{wc}} \tag{37}$$

$$R_3, R_4, \omega L_3, \omega L_4 \ll \frac{1}{\omega C_{pc}} \tag{38}$$

$$R_3, R_4, \omega L_3, \omega L_4 \ll \frac{1}{\omega C_{wc}} \tag{39}$$

The error caused by C_{pc} and C_{wc} can be simplified as

$$\Delta_{C_{pc}} \approx -\frac{C_{pc}}{k}\left(\frac{R_3 R_{core}}{L_m} + \omega^2 L_3\right) \tag{40}$$

$$\Delta_{C_{wc}} \approx \frac{R_{core} C_{wc}}{k L_m^2}(R_4 L_3 + R_3 L_4) \tag{41}$$

For the aforementioned measurement example, with k=0.5, C_{pc}≈5pF, C_{wc}≈20pF, L_m≈3.7μH, R_3≈R_4≈0.2Ω, L_3≈L_4≈200nH, ω=2π ·2MHz, and R_{core}≈4.9kΩ, so $\Delta_{C_{pc}}$≈−0.3%, $\Delta_{C_{wc}}$≈0.1%.

3.3. Assessment of high frequency magnetic materials up to 40MHz

3.3.1. Permeability characterization

When there is no DC bias, an impedance analyzer can be used to test a toroidal magnetic core sample and provide permeability at very high frequencies. Figure 3.19 shows the measured relative permeability of LTCC and NEC flake materials up to 80MHz with no DC bias using an Agilent 4294A impedance analyzer and a 16454A magnetic material test fixture. It can be seen that the NEC flake material has a higher initial permeability than most of the LTCC materials at tens of MHz. The only exception is the LTCC 40012: its initial permeability is lower than the NEC flake material after 14MHz, while is higher before 14MHz. As shown in chapter 4, we will perform our design between 10MHz to 40MHz, and build our hardware platform at 20MHz. In this frequency range, the NEC flake has a higher initial permeability in most of the cases. Furthermore, the permeability of LTCC 40012 material has a much faster drop than the NEC flake as the DC bias level increases [21, 67, 68], which makes it not a proper choice in this work.

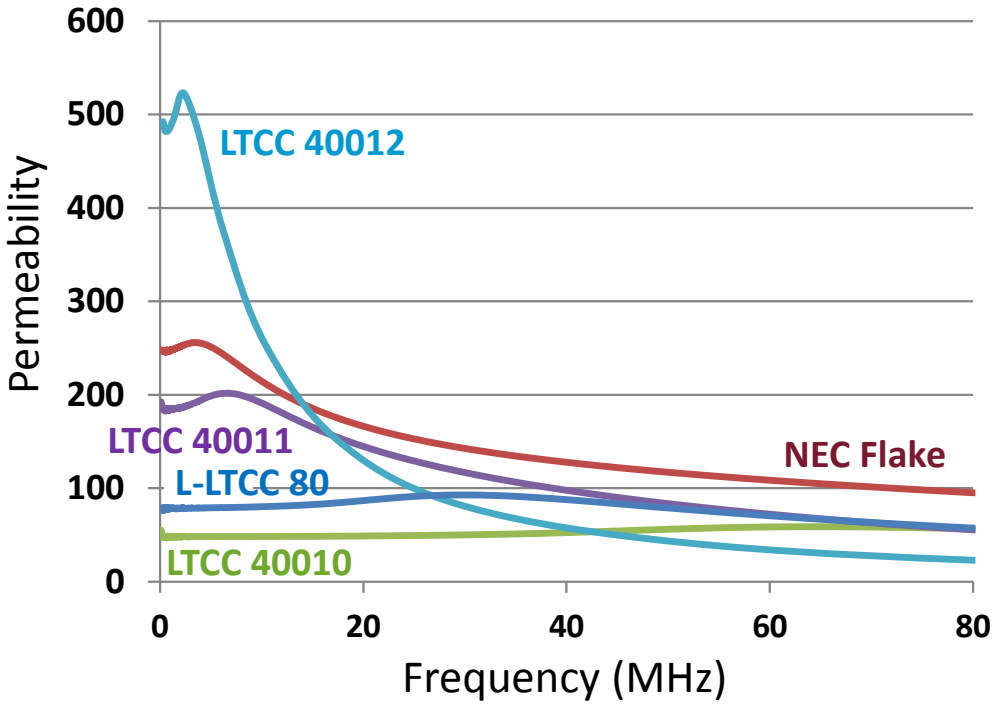


Figure 3.19. Permeability with no DC bias. LTCC 40010, 40011 and 40012 are from ESL ElectroScience®; L-LTCC 80 is the laminated LTCC material reported in[67].

To measure high-frequency permeability under a DC-biased condition, the internal DC bias of the impedance analyzer can be used, however the DC bias ability of the impedance analyzer is usually very limited. For example, the Agilent 4294A impedance analyzer can only supply <0.1A DC bias current, which is inadequate to generate the DC bias level that occurs in real applications. To overcome this problem, an external DC source is adopted to provide the required DC bias as shown in Figure 3.20. However, the impedance of the DC source will introduce a significant measurement error, as shown by the green curve in Figure 3.22. To minimize this error, the AC voltage cancellation method applied in [21] is implemented with the impedance analyzer, as shown in Figure 3.21. By using two identical core samples and reversed coupling polarities, the AC voltage generated on the two cores at the DC source side can cancel each other, thus the measurement error caused by the impedance of the

DC source can be diminished, as shown by the red curve in Figure 3.22. It is worth noting that to keep the two sample cores used in Figure 3.21 as identical as possible, it is suggested to use the same batch of samples and to perform an initial permeability measurement (without DC bias) on them separately to minimize the sample-to-sample permeability variation. In the measurement performed in this work, the sample-to-sample permeability variations is very small due to the existence of a distributed air gap in the magnetic cores. It is also worth mentioning that an alternative method for permeability measurement under DC bias using auxiliary DC-current winding is reported in[121], in which a function generator, a power amplifier, and a fine-tuned resonant capacitor at a given measurement frequency are required (instead of the impedance analyzer applied in this work). Using the measurement setup shown in Figure 3.21, the DC-biased permeability of the NEC flake and the LTCC 40010 is measured at different frequencies, and the results are summarized in Figure 3.23. In this comparison, the LTCC 40010 is chosen over the other LTCC materials because of its higher permeability under DC bias and lower core loss density at high frequencies [15, 21, 67, 68]. The comparison in Figure 3.23 shows that the NEC flake has a higher permeability than the LTCC 40010 at very high frequency and DC bias.

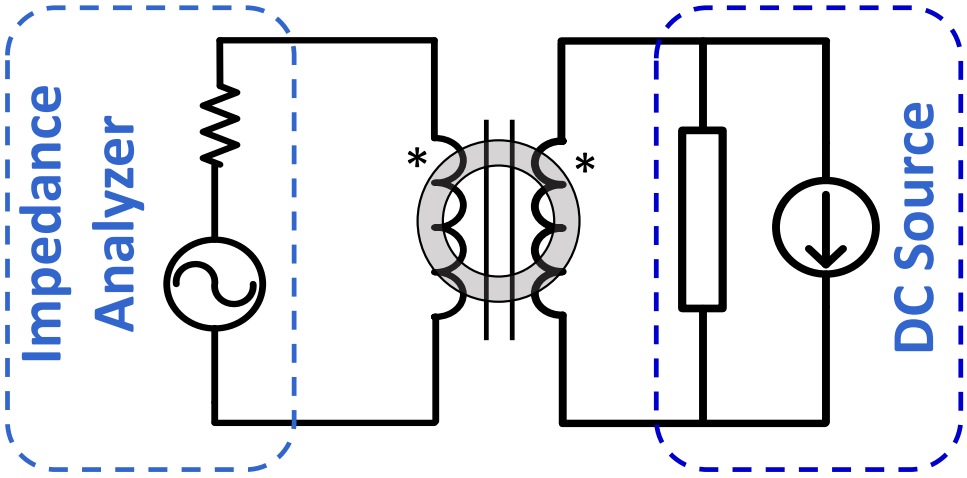


Figure 3.20. Permeability measurement setup with impedance analyzer and external DC source.

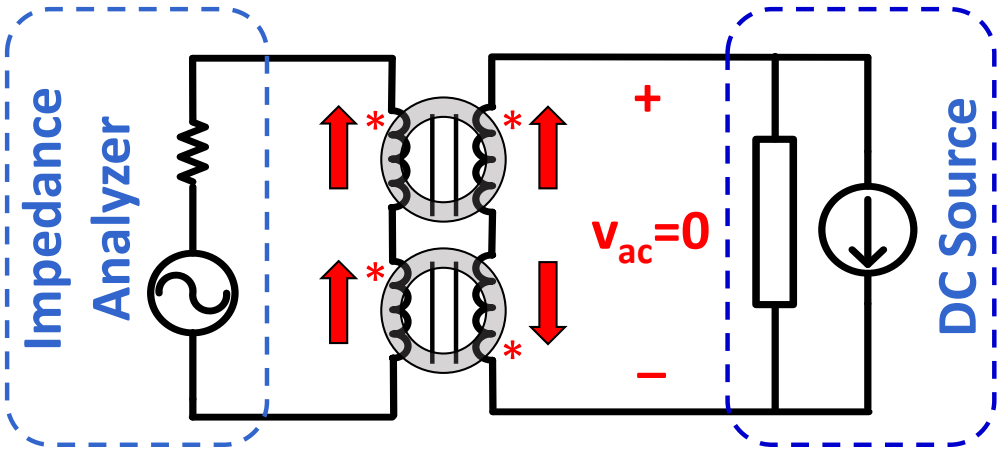


Figure 3.21. Improved permeability measurement setup with AC voltage cancellation.

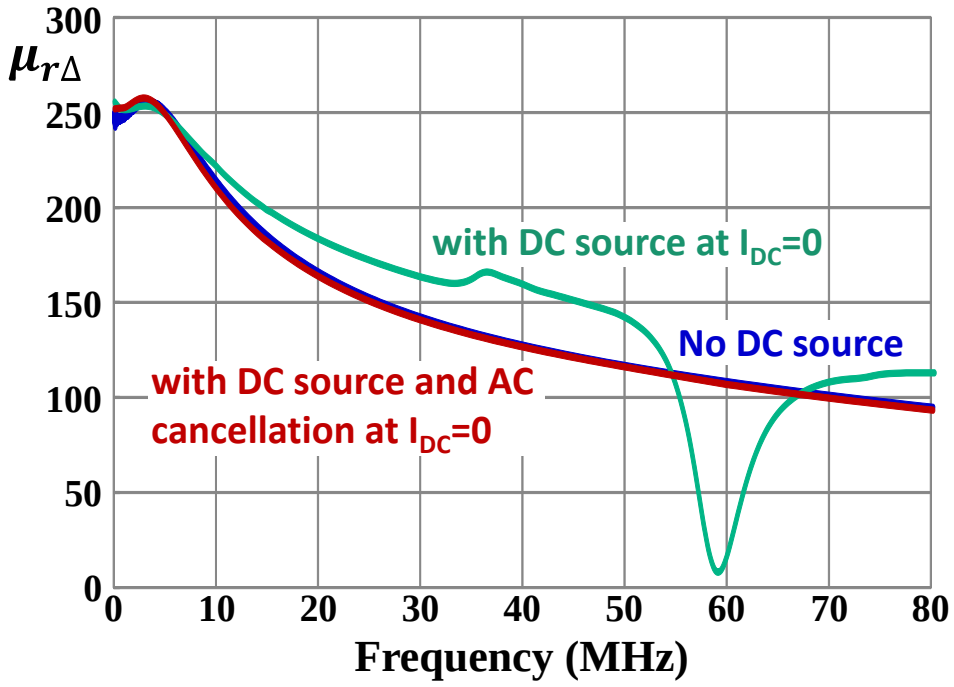


Figure 3.22. Measured permeability without DC bias from different setups. Blue: impedance analyzer without external DC source; green: Figure 3.20 setup; red: Figure 3.21 setup; I_{DC}: output current from DC source.

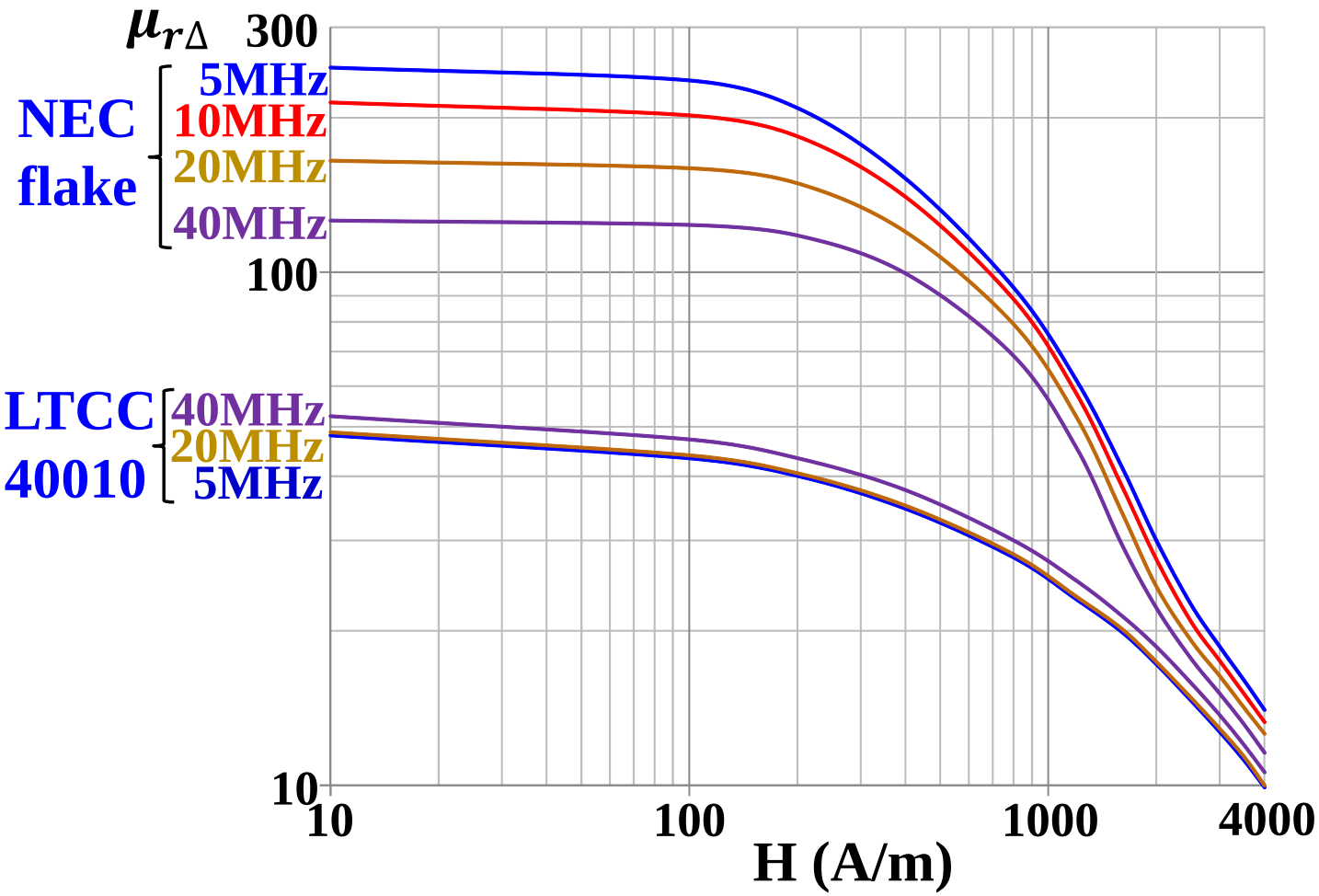


Figure 3.23. Permeability under DC bias of the NEC flake and LTCC 40010 material. Each curve corresponds to a certain frequency value. The LTCC 40010 is chosen over the other LTCC materials in this comparison because of its higher permeability under DC bias and lower core loss density at high frequencies [50, 51, 61, 78].

3.3.2. Core loss characterization

To perform a core loss measurement in the tens of MHz range, special care needs to be taken for the implementation of the measurement setup[122].

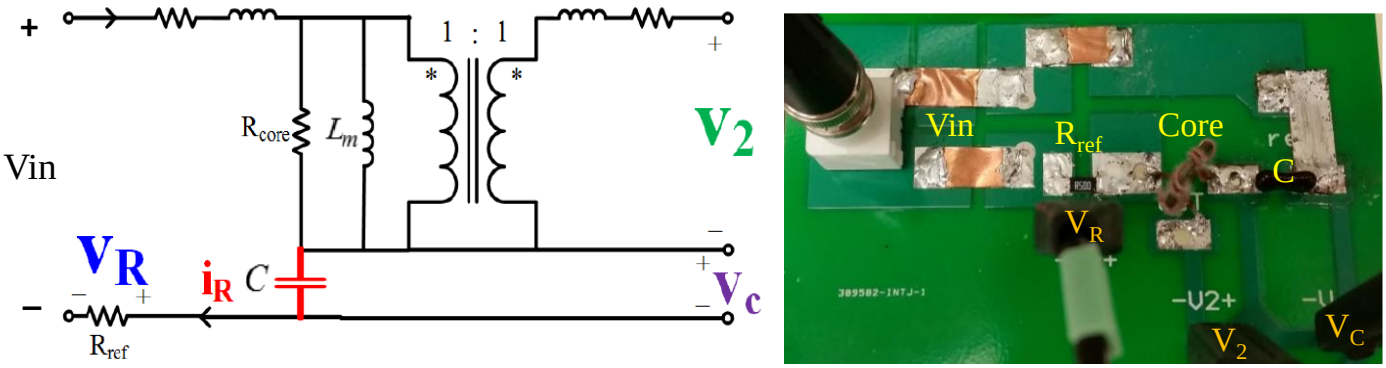


Figure 3.24. Core loss measurement schematic and physical setup using partial cancellation method [112, 113]. The magnetic core under test, current sensing resistor (R_{ref}), cancellation capacitor (C), and voltage probes for V_2, V_C and V_R are marked in the figure.

Table 3.2. Summary of equipment used in the core loss measurement setup

Equipment	**Manufacturer**	**Part number**
Power amplifier	Amplifier Research	25A250A
Function generator	Tektronix	AFG3102
Differential voltage probes	Tektronix	TDP 1000
Current sensing resistor	Stackpole Electronics Inc.	CSRN2512FKR500
Coaxial current shunt	T&M Research Products	SDN-414-10
Current probe	Tektronix	TCP0030

Figure 3.24 shows the measurement set up using the aforementioned partial cancellation method [112, 113]. The equipment is summarized in Table 3.2. The input port is excited by a power amplifier driven by a function generator; the voltage signal V_R, V_2, and V_C are sensed by differential voltage probes, from which the core loss P_{core} can be extracted using Equ. 24. The measurement results of the NEC flake material up to 40MHz are depicted by the black curve in Figure 3.25. It can be seen that the measured core loss density curve is a straight line before 20MHz, but an abnormal variation appears at higher frequencies, which indicates that a measurement problem exists at very high frequency. The first step we took to overcome the problem is to minimize the loops in the measurement circuit. As shown in Figure 3.26, the area of the driving loop, the V_2 sensing loop, and the V_C sensing loop are reduced by 93%, 95%, and 98%, respectively. The measurement result with the minimized loops is shown by the blue curve in Figure 3.25. It can be seen that the abnormal variation is pushed to a higher frequency than the original setup's result (black curve).

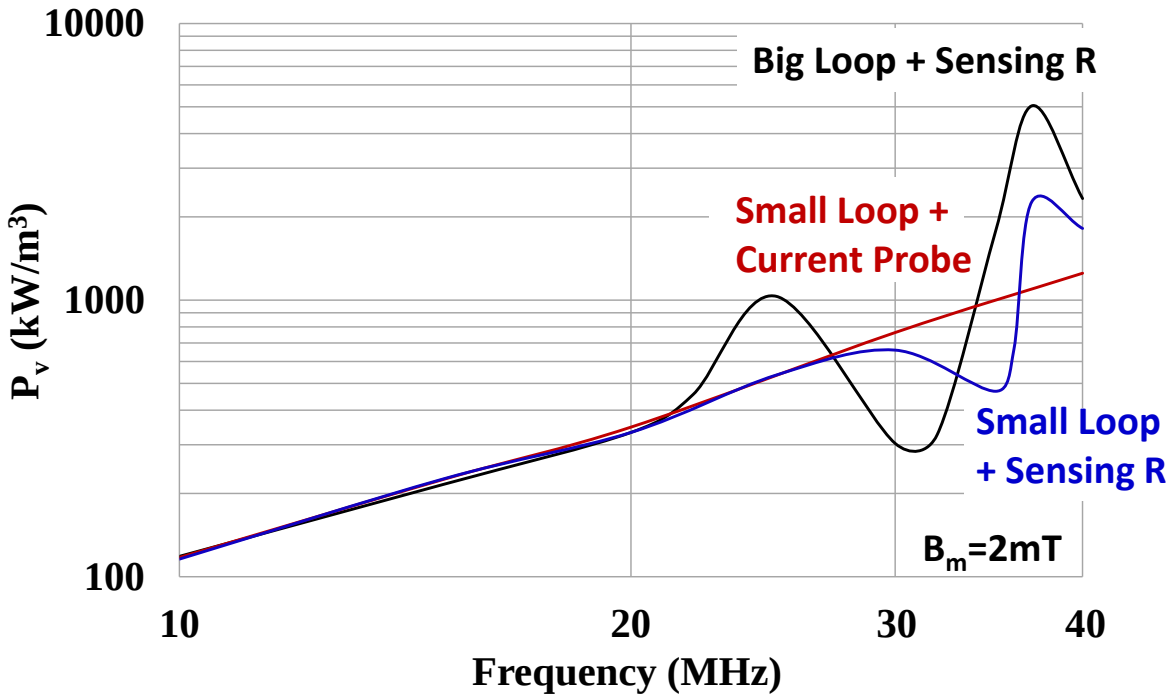


Figure 3.25. Measured core loss density of the NEC flake material with different measurement setups.

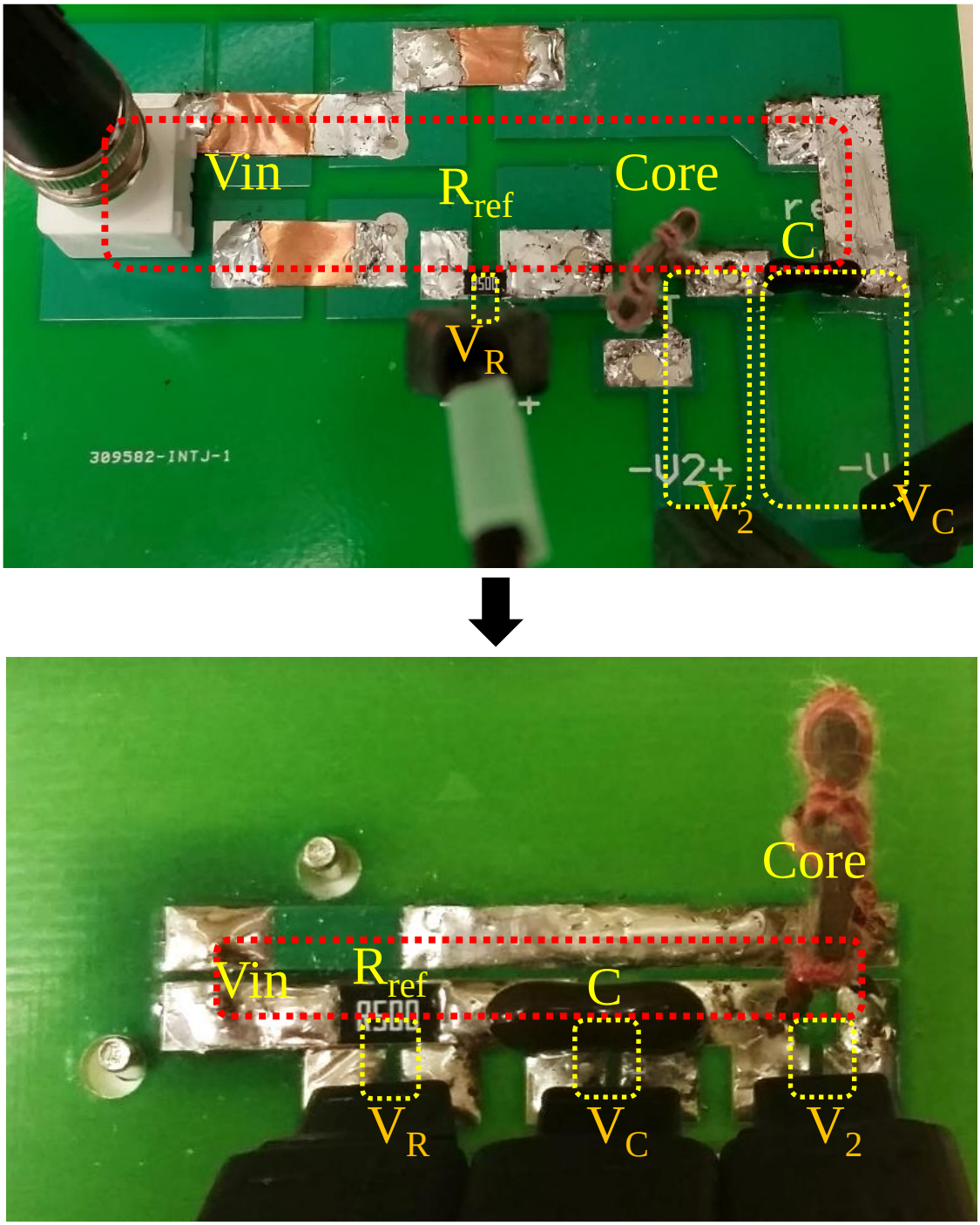


Figure 3.26. Minimizing loop area in the measurement setup. The driving loop is marked by red dotted line, and sensing loops by yellow dotted lines.

In the next step, three different current sensing methods (current sensing resistor, coaxial current shunt, and 120MHz bandwidth current probe) are compared at very high frequency. As shown in Figure 3.27, the three methods are used to measure the same current simultaneously for comparison. The magnitude of the excitation voltage is kept constant at different frequencies. The current sensing waveforms from the three different methods at different frequencies are summarized in Figure 3.28. At 10MHz, the three methods yield almost the same results, but when the frequency becomes higher, the results from the current sensing resistor and the coaxial current shunt show an abnormal magnitude variation, while the current probe is able to provide the most stable result among the three methods. Therefore, the current probe is adopted in the improved loss measurement setup, as shown in Figure 3.29. The time delay introduced by the current probe is taken care by the following two means in the measurement: 1) estimate the time delay with a high-Q (quality factor) inductor at the interested frequencies, and apply it as a phase compensation in the corresponding channel of the oscilloscope; 2) the exact delay in the measurement should be close to the estimated value, but with some small deviations, which is further taken care by the partial cancellation mechanism in the measurement method[112, 113]. The measurement results are shown by the red line in Figure 3.25, where no abnormal variation is observed.

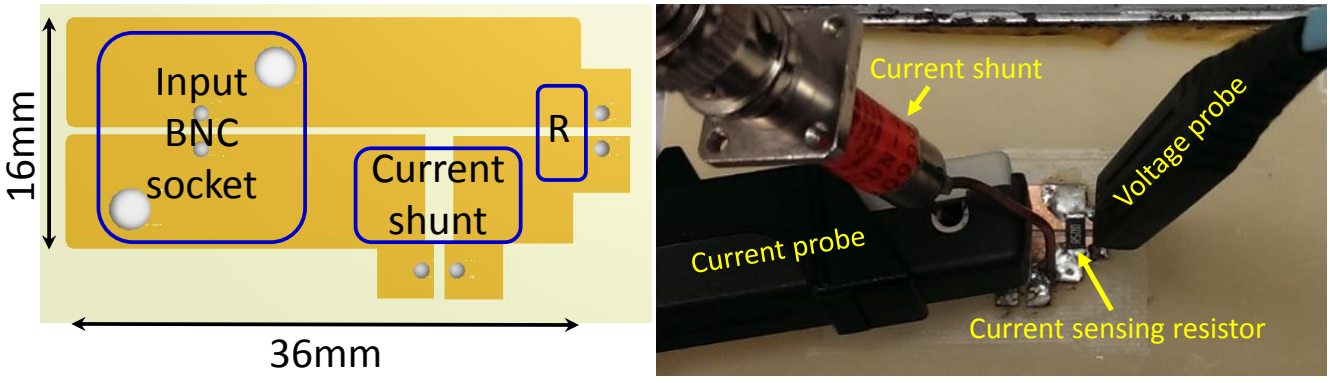


Figure 3.27. Board layout (with minimized loops) and physical setup for comparison of current sensing methods.

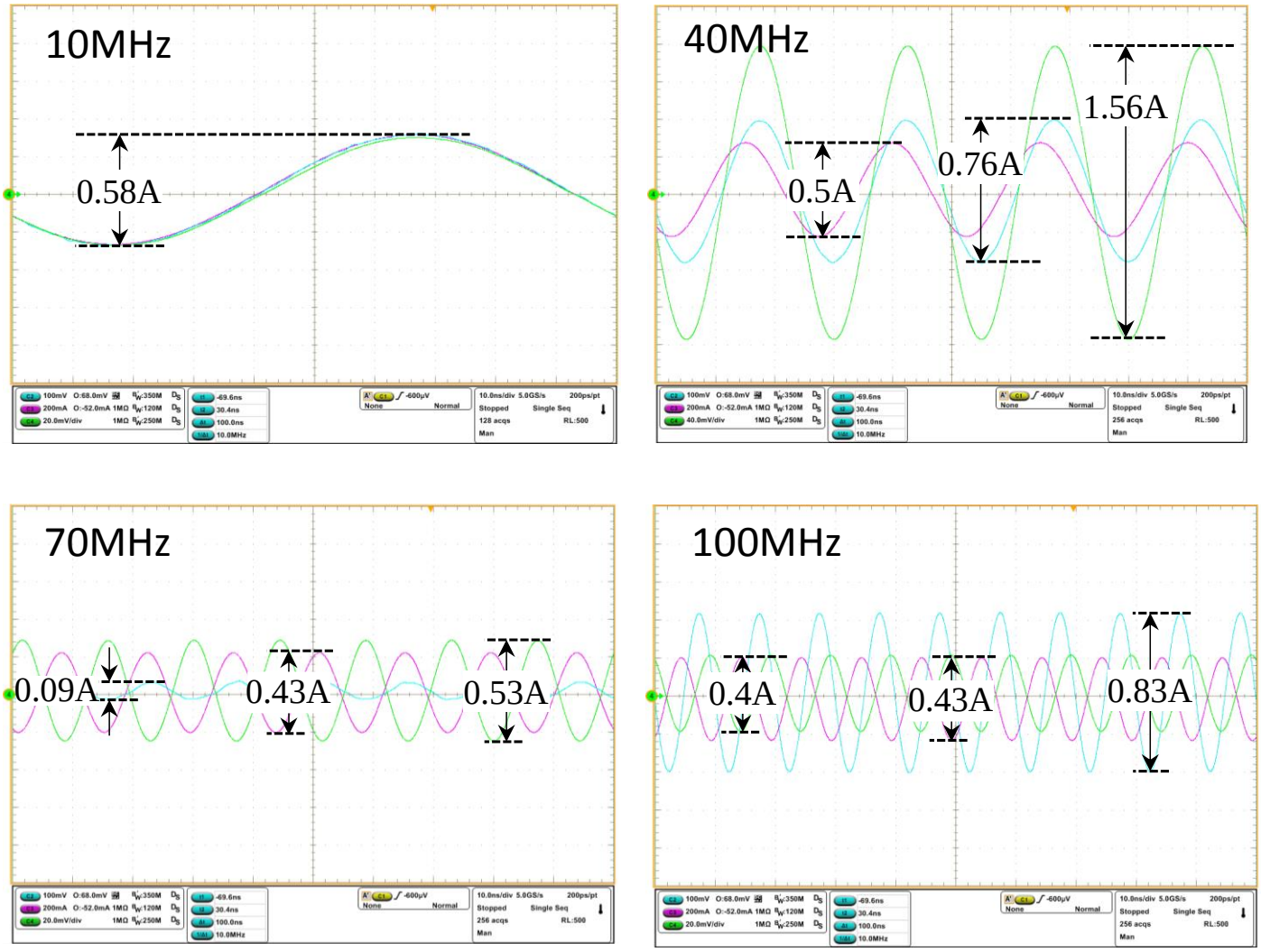


Figure 3.28. Current sensing waveforms with different methods. Blue: current sensing resistor; green: coaxial current shunt; purple: current probe. The measured current amplitude of each waveform is marked in the figure.

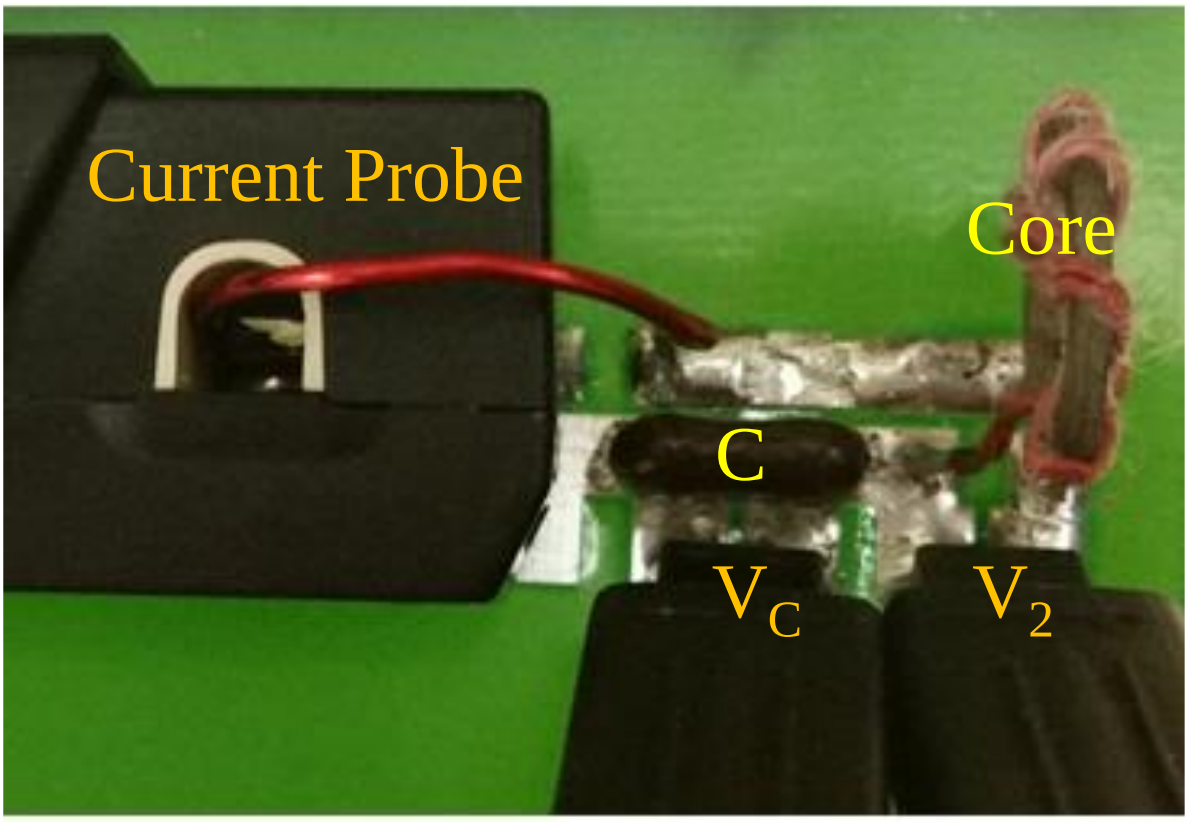


Figure 3.29. Improved loss measurement setup with minimized loops and current probe for the very high frequency test.

It is worth mentioning that the loss characterization technique discussed here is applicable not only to the core loss measurement, but also to the total inductor loss measurement. By simply replacing the core under test with an inductor, and using the V_2 probe to measure the voltage across the inductor (with everything else kept the same), the measurement result will provide the total inductor loss including core loss and winding loss.

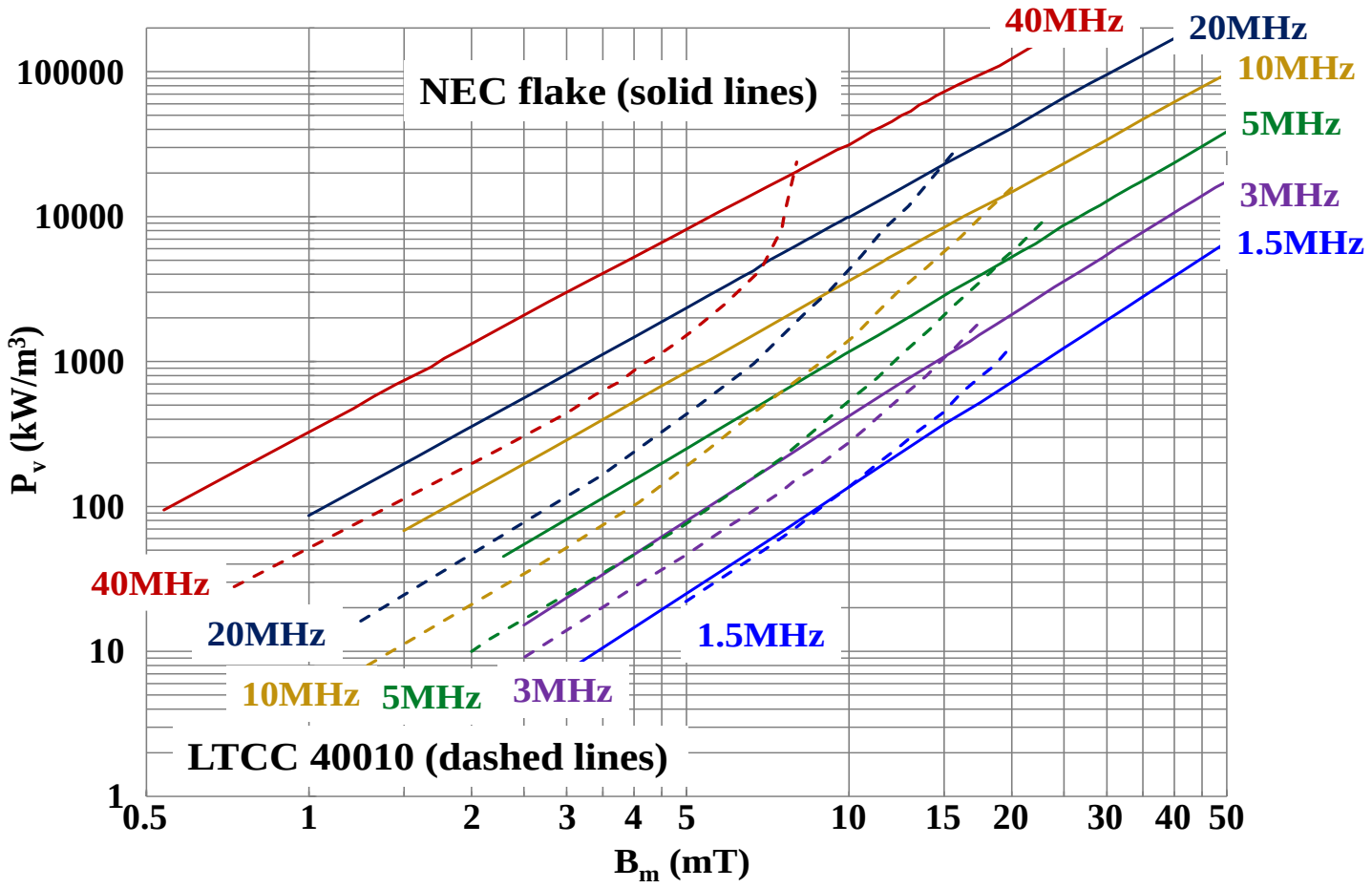


Figure 3.30. Measured core loss density of LTCC 40010 and NEC flake materials at very high frequency. The horizontal axis B_m represents the peak value of the flux density. LTCC 40010 is chosen over the other LTCC materials in the comparison because of its lower core loss density at high frequencies [15, 21, 67, 68].

According to the core loss comparison of LTCC 40010, 40011, 40012, L-LTCC 80 and NEC flake materials in previous works [15, 21, 67, 68], the LTCC 40010 and the NEC flake have a lower core loss density than the other LTCC materials at high frequency. Using the improved measurement setup shown in Figure 3.29, the core loss density of the LTCC 40010 and the NEC flake is measured and compared at frequencies up to 40MHz, as shown in Figure 3.30. The figure shows that the core loss density of the LTCC 40010 increases dramatically at a

higher flux density, especially at very high frequencies, while the core loss density change of the NEC flake maintains the same trend (as indicated by the straight lines in Figure 3.30) as B_m increases. This different behavior can be ascribed to the substantial difference in the magnetic material's composition and structure: ferrite ceramic (LTCC) and metal composite (NEC flake). Comparing the NEC flake and LTCC 40010 in the tens of MHz and B_m>15mT range (which is applied in the IVR inductor design in chapter 4), the NEC flake has a lower core loss density than LTCC 40010. It is also worth noting that the core loss density in this range is unusually high when compared with conventional design (often in about 1000kW/m^3 range). So an experiment is performed and demonstrated in chapter 4 to investigate whether a thermal issue exists due to the very high core loss density.

Based on the comparison above, the NEC flake material shows a better performance in both core loss density and permeability under a DC biased condition than LTCC materials in a very high frequency range. Therefore, the NEC flake material is chosen in chapter 4 for the design procedure for IVR inductors.

3.4. Summary

A new core loss measurement method for arbitrary excitation with a partial cancellation concept is proposed and experimentally verified with both sinusoidal and rectangular wave excitation. It overcomes the accuracy sensitivity to the cancellation component in the existing methods and enables an accurate measurement without fine-tuning of the cancellation component value.

Based on the proposed method, the magnetic characterization technique at very high frequency (tens of MHz) is investigated for IVR inductor design. The issue and solution in the permeability and loss measurement are demonstrated. The LTCC and NEC flake materials are characterized and compared at very high frequency, and the NEC flake shows advantage over LTCC materials from both a permeability and core loss density perspective.

Chapter 4. Very High Frequency Integrated Voltage Regulator for Mobile CPUs

4.1. Magnetic design trade-off including footprint, profile, loss, and frequency

4.1.1. Single-phase inductor design

According to the power requirements of smartphones, the buck converter design specifications are set as: input voltage range of 3.2V to 4.5V, output voltage range of 0.6V to 1.2V, and maximum load current of 3A for each phase. The nominal operating voltage of V_{in}=3.8V and V_{out}=1V is chosen for the inductor design. The very high switching frequency in tens of MHz allows the utilization of a very simple winding structure of only a single vertical via. The structure and flux line of the low profile lateral flux inductor is shown in Figure 4.1. A concentric ring model [18, 19] is used to calculate the inductance and core loss of this non-uniform flux inductor. The whole magnetic core is first divided into numerous concentric rings with almost uniform flux in each of them. By then integrating the inductance and loss of all the rings, the total inductance and core loss of the inductor can be acquired with the following equations:

$$L = h \cdot \int_{r_v}^{r_v+g} \frac{\mu_0 \cdot \mu_{r\Delta}(r)}{2\pi \cdot r} dr \tag{42}$$

$$P_{core\_total} = 2\pi \cdot h \cdot \int_{r_v}^{r_v+g} P_v(r) \cdot r \cdot dr \tag{43}$$

where, L is the total inductance, h is the core thickness, r_v is the via radius, g is the distance from the via to the edge of the core, μ_0 is permeability constant, $\mu_{r\Delta}(r)$ is relative permeability at each radius location of the core (different for each concentric ring), P_{core_total} is the total core loss, $P_v(r)$ is the core loss density at each radius

location of the core. For each concentric ring, its core loss density under rectangular excitation and DC bias is modeled using the rectangular extension of the Steinmetz equation (RESE) [123] with DC-bias impact factor[119, 124] with the following equation:

$$P_v(r) = \frac{8}{\pi^2[4D(1-D)]^{\gamma+1}} \cdot F(H_{DC}) \cdot k f^{\alpha} B_m^{\beta} \tag{44}$$

where, the first term $\frac{8}{\pi^2[4D(1-D)]^{\gamma+1}}$ accounts for the impact from rectangular excitation; the second term $F(H_{DC})$ accounts for the impact from DC bias; and the third term $k f^{\alpha} B_m^{\beta}$ accounts for the core loss density defined by the Steinmetz equation (a detailed description of this core loss model is presented in [119, 123, 124]).

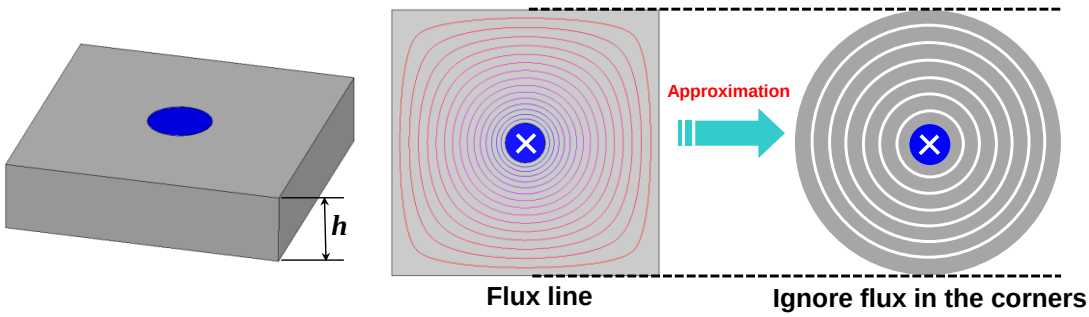
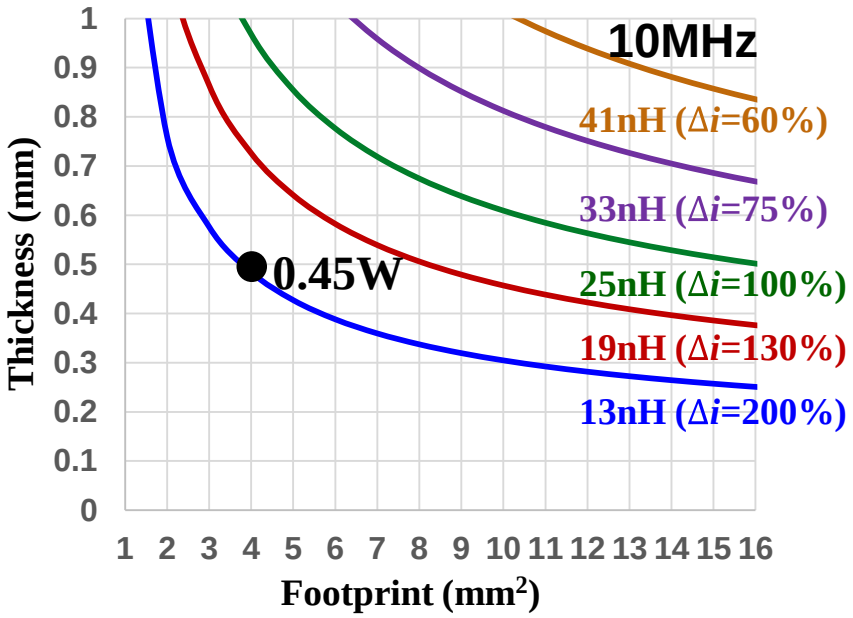
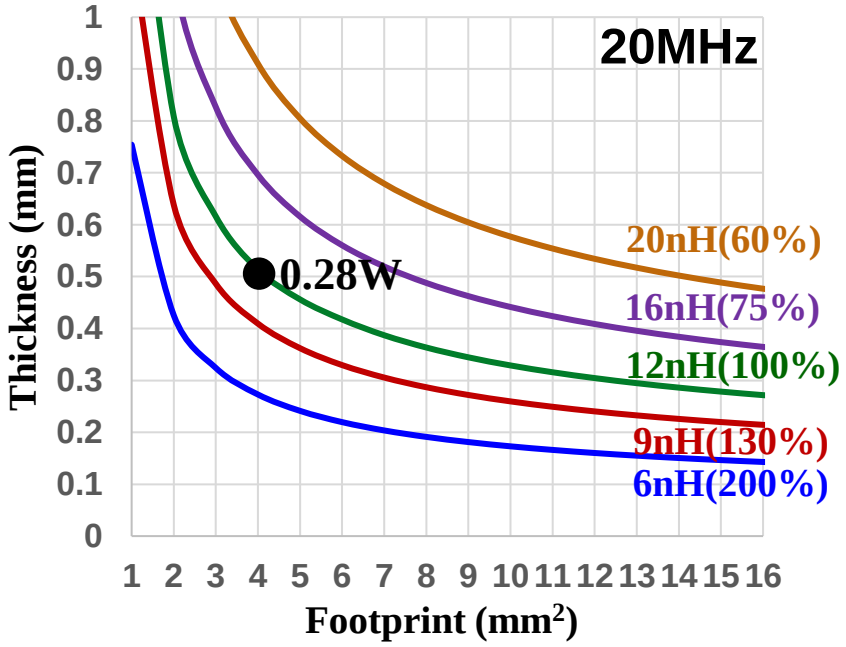


Figure 4.1. Structure and flux line of single-via, non-uniform flux inductor. By ignoring the weak flux at corners, the core can be approximated as a sum of a series of concentric rings with almost uniform flux in each of them[18].

The calculated inductor footprint and thickness at different frequencies with different inductances are shown in Figure 4.2. Each curve corresponds to an inductance value which generates a peak-to-peak current ripple from 60% to 200% at different frequencies. Since the permeability is not the same at different frequencies (as shown

in Figure 3.23), the inductor size does not reduce proportionally with frequency. Due to the very short winding length, the winding loss is very small and the core loss dominates the total inductor loss. The inductor core loss with a certain inductor footprint ($4mm^2$) and thickness (0.5mm) while at different frequency is shown in the figure by the black dots. It can be seen that the core loss becomes smaller as the frequency increases from 10MHz to 40MHz with the same core size. This is because the flux density reduction at higher frequency has a more dominant impact on core loss density than the frequency increase for the NEC flake material (given that the flux density and frequency are the two variables determining core loss density in Steinmetz equation). Therefore, it is beneficial for the inductor (from both a size and loss point of view) to operate at a higher frequency at least up to 40MHz. The inductor core loss at different inductor sizes is calculated and plotted at 20MHz as shown in Figure 4.3. It can be seen that for a given inductance, when the inductor footprint is reduced, the inductor thickness will increase, and the core loss and volume will decrease. For a given footprint, when the core thickness is increased, the core loss will decrease. A design example is chosen with a $4mm^2$ footprint and 0.5mm thickness to fit the stringent space requirement of a smartphone. It has an ultra-low DCR of only 0.07mΩ, which can be ascribed to its very simple winding structure and ultra-low profile. For this design example, the DC magnetic field strength H_{dc}, AC peak flux density B_m, and core loss density P_v are shown in Figure 4.4. It is worth noting that the core loss density in the very high frequency design is unusually high (>100000kW/m^3) when compared with conventional design (often in about 1000kW/m^3 range). Therefore, to investigate whether a thermal issue exists due to the very high core loss density, an experimental verification is performed in section 4.2.


10MHz
41nH (Δi=60%)
33nH (Δi=75%)
25nH (Δi=100%)
19nH (Δi=130%)
13nH (Δi=200%)
0.45W
Thickness (mm)
Footprint (mm²)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16


20MHz
20nH(60%)
16nH(75%)
12nH(100%)
9nH(130%)
6nH(200%)
0.28W
Thickness (mm)
Footprint (mm²)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

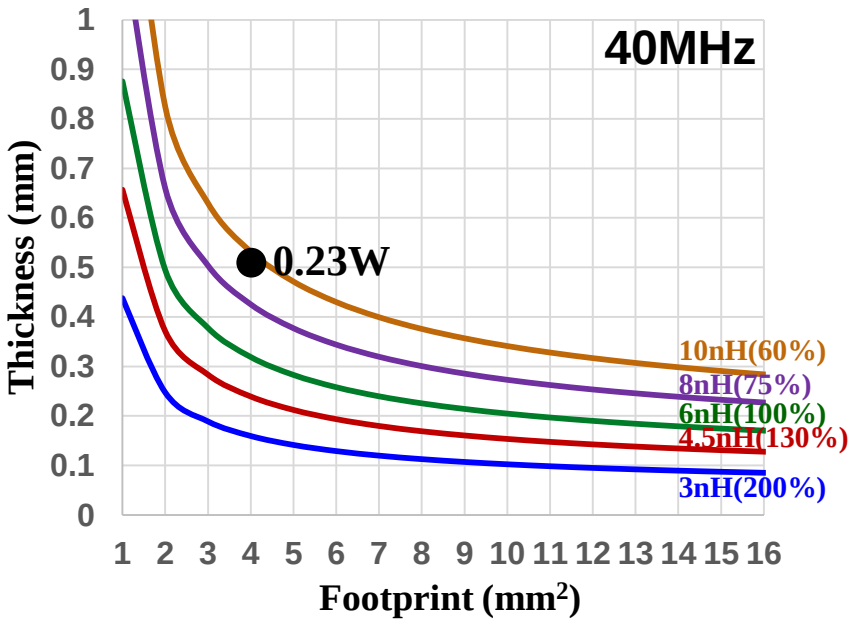


Figure 4.2. Designed inductor size for different inductances and frequencies. The number in parentheses shows the ratio of the peak-to-peak current ripple to the DC load current (3A). The dots indicate the core loss.

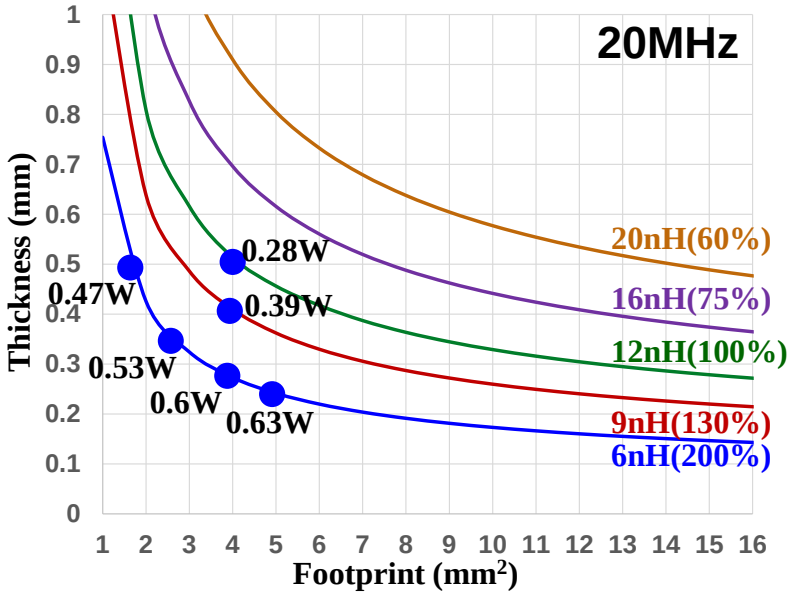


Figure 4.3. Calculated core loss at 3A full load current and different inductor sizes. Each dot corresponds to a certain inductor size.

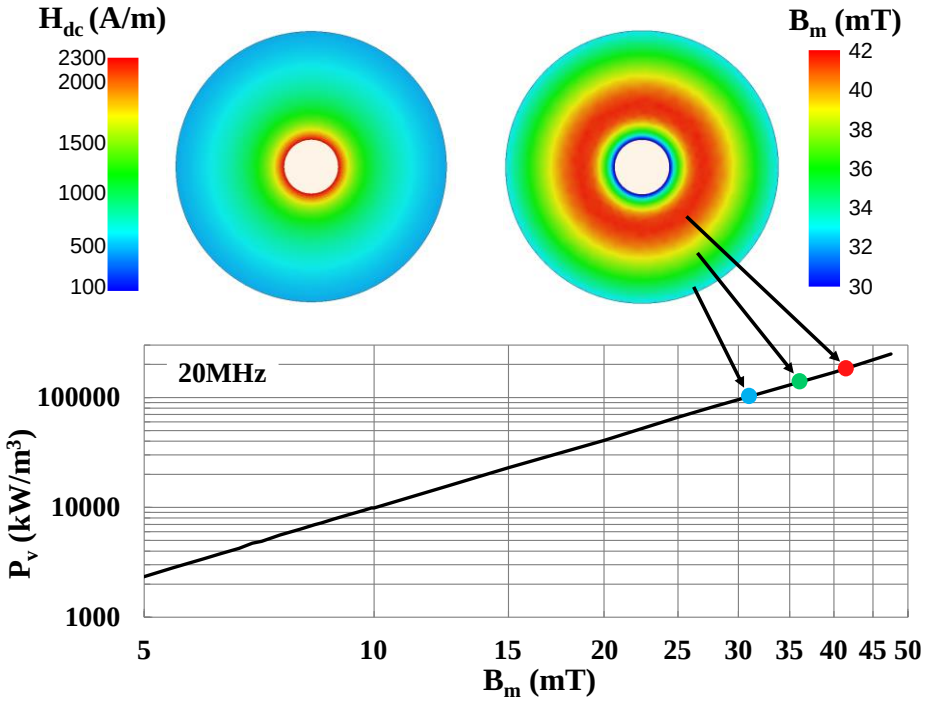


Figure 4.4. H_{dc}, B_m and P_v distribution of the core in the design example. The P_v vs B_m curve is from the material characterization results in Chapter 3.

4.1.2. Multi-phase integrated inductor design

Based on the single-phase inductor design discussed above, four-phase and five-phase integrated inductors are designed[125, 126]. Their flux distribution is shown in Figure 4.5. The four-phase integrated structure is a combination of four single-phase inductors. It can be seen from the flux distribution that the central part of the core is under-utilized, therefore a fifth phase is added in the center of the core to better utilize the total core volume and improve the inductance density. The five-phase integrated inductor has dimensions of 4mm×4mm×0.5mm. The self-inductance and magnetic coupling coefficient between each phase at full load condition are shown in Figure 4.6. It can be seen that the magnetic coupling between each phase is positive and relatively weak. As a result, the current waveform has a small distortion due to the weak coupling between phases, as shown in Figure 4.7. The core loss per phase of the four-phase and five-phase integrated core at full load condition is 284mW and 297mW, respectively, which is similar to the value of the single-phase inductor (277mW). It can be seen that there is almost no negative impact caused by adding the fifth phase in the center in terms of both the current ripple and the core loss. The multi-phase integrated structure can also be easily extended to more than five phases. For example, the inductor shown in Figure 1.27 (c) has an eight-phase integrated structure. It is worth noting that the four-phase and five-phase design is based on the single-phase inductor design as shown in section 4.1.1. The core thickness and the distance between each via is determined by the thickness (0.5mm) and footprint (4mm^2) of the single-phase inductor that we choose to start the multi-phase integration. To investigate the scalability of the multi-phase integration process, a different single-phase inductor with 0.3mm thickness and 8mm^2 footprint is used to start the same integration process and to form a five-phase integrated inductor, and we find that the coupling coefficient between each phases in the five-phase inductor stays almost the same as the case shown in Figure 4.6, and the self-inductance of each phase scales almost proportionally according to the original inductance of the single-phase inductor (~25% smaller than the case shown in Figure

4.6). Therefore the multi-phase integration process presented in this work has a good scalability for different inductor sizes.

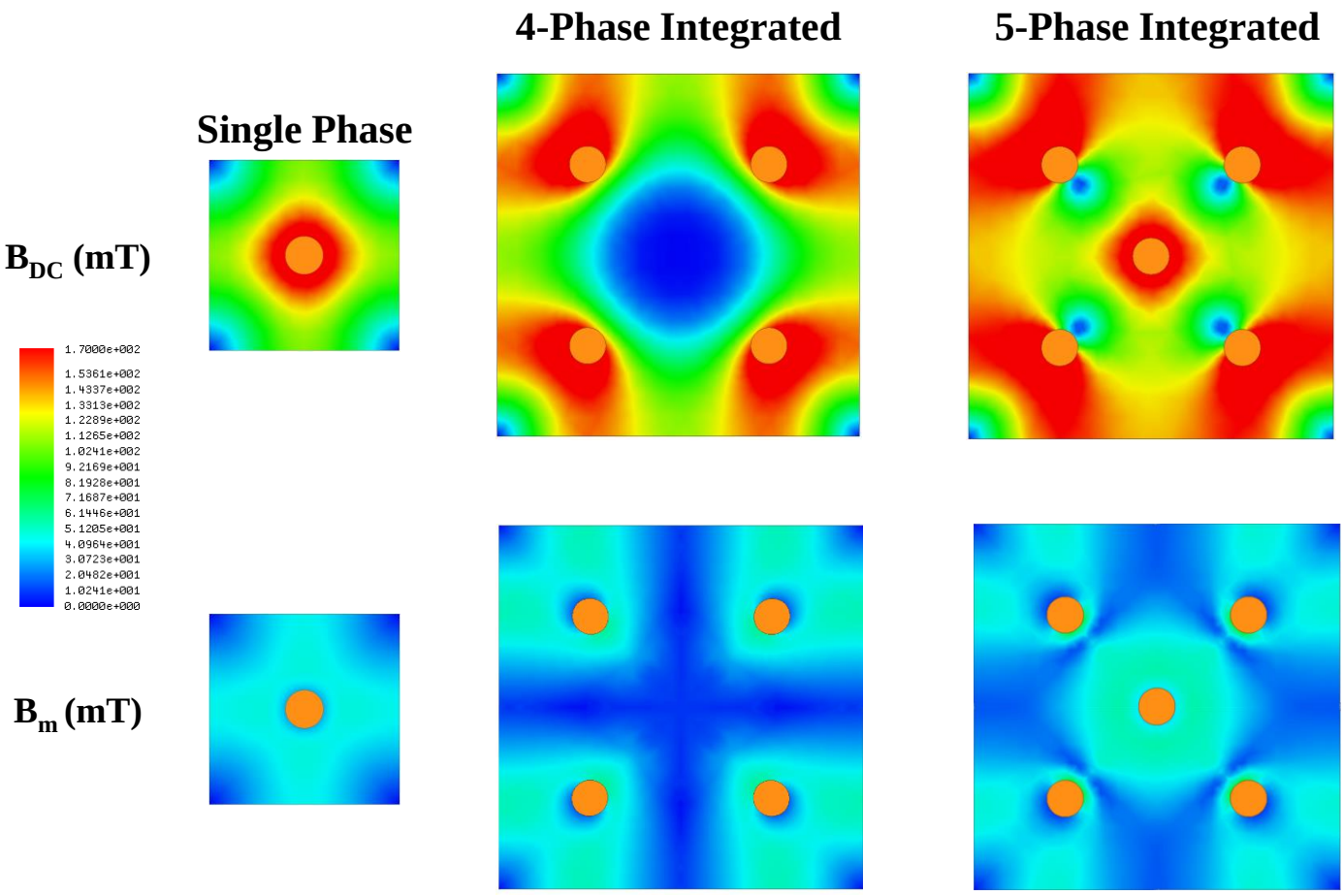


Figure 4.5. DC and AC flux distribution of the single-phase, four-phase, and five-phase integrated inductors.

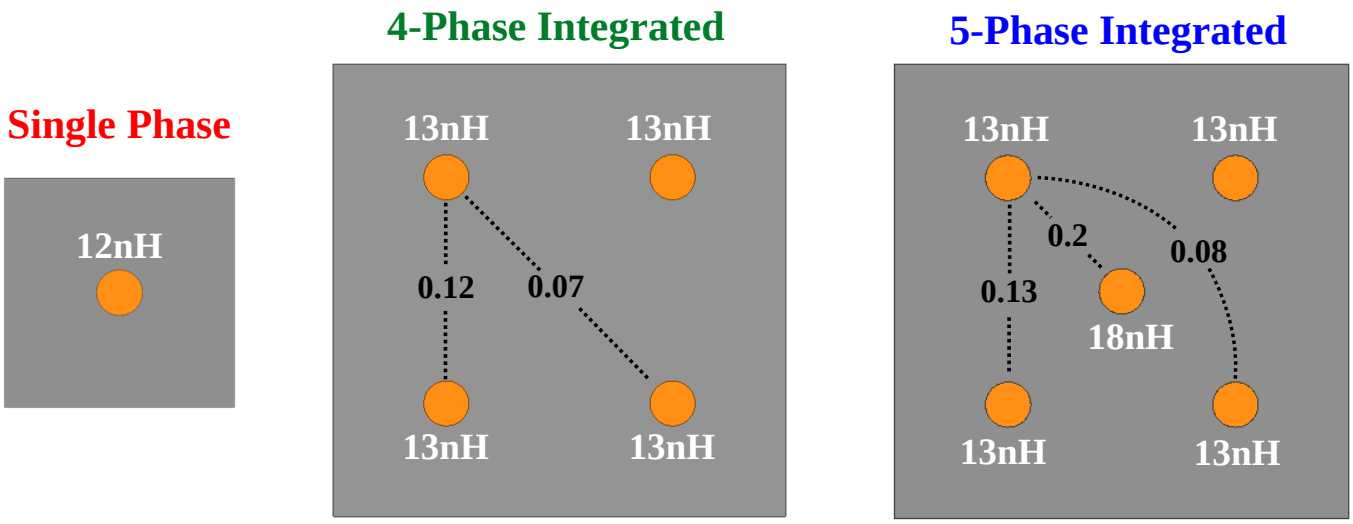


Figure 4.6. Self-inductance of each phase (represented by the number besides each via) and magnetic coupling coefficient between phases (represented by the number within the dotted lines) for different inductor structures. The results are acquired by FEA simulation using Ansys Maxwell.

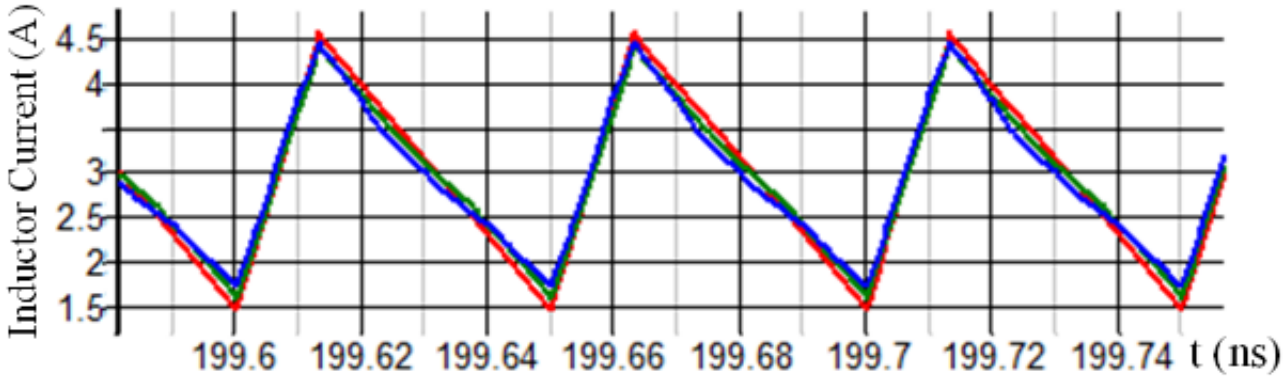


Figure 4.7. Current waveforms of different inductor structures. The results are acquired by circuit simulation based on the self-inductance and coupling coefficient shown in Figure 4.6. (Red: single-phase; green: four-phase integrated; blue: five-phase integrated.)

4.2. Feasibility assessment with multi-phase VR hardware up at 20 MHz

According to a survey of commercially available high frequency switching devices (Table 1.1), SEMTECH's Dr. MOS SC220 is capable of switching at 20MH, but the maximum load current that the SC220 can handle is only 0.65A. Thus, it is chosen to perform an underrated test at 0.6A (instead of 3A full load current in our design). On the other hand, the EPC9036 half bridge circuit (with EPC's EPC2100 GaN switch and TI's LM5113 driver) can sufficiently handle the full load current at tens of MHz, but its highest working frequency is limited by the minimum on-pulse width of the driver. The LM5113 driver has a minimum on-pulse width requirement of ~24ns. With the designed input/output value ($3.8V_{in}/1V_o$), the highest frequency is limited to 11MHz. To enable a higher operating frequency under the minimum on-pulse width requirement, a larger duty cycle is required. Therefore in the following test, an input/output voltage of $3.2V_{in}/1.6V_o$ is chosen to enable a 20MHz operating frequency all the while maintaining a similar inductor voltage-sec (and thus the core loss) as that of the designed working condition ($3.8V_{in}/1V_o$).

A single-phase inductor sample with a $4mm^2$ footprint and a 0.5mm thickness is fabricated, and its inductance measurement result is shown in Figure 4.8. It can be seen that the inductance at 0.6A load current is 30nH. To test the inductor loss using SC220, the loss of SC220 Dr. MOS is first measured using its buck evaluation board with a 30nH air core inductor running at $3.8V_{in}$ to $1V_{out}$, and a 0.6A load current at 20MHz, as shown in Figure 4.9. The measured total converter loss is 0.329W. Meanwhile, by measuring the DC and AC resistance of the 30nH air core inductor with an Agilent 4294A impedance analyzer, the air core inductor loss is determined to be 0.013W. Therefore, the loss from Dr. MOS is extracted as 0.316W. Then the air core inductor is replaced with the ultra-low profile inductor sample (as shown in Figure 4.10), and the total loss is measured as 0.552W under the same working condition. Accordingly, the inductor loss of the sample is extracted as 0.236W, which verifies the calculated value of 0.242W. After the test using the SC220, a further test using EPC9036 is performed to

enable measurement at full load condition. A similar approach to the aforementioned procedure is adopted for the EPC9036, which combines a set up with an air core inductor (as shown in Figure 4.11) and an inductor under test (as shown in Figure 4.12). The measured core loss at 20MHz and different load condition is summarized in Figure 4.13, which shows a good agreement between calculation and measurement.

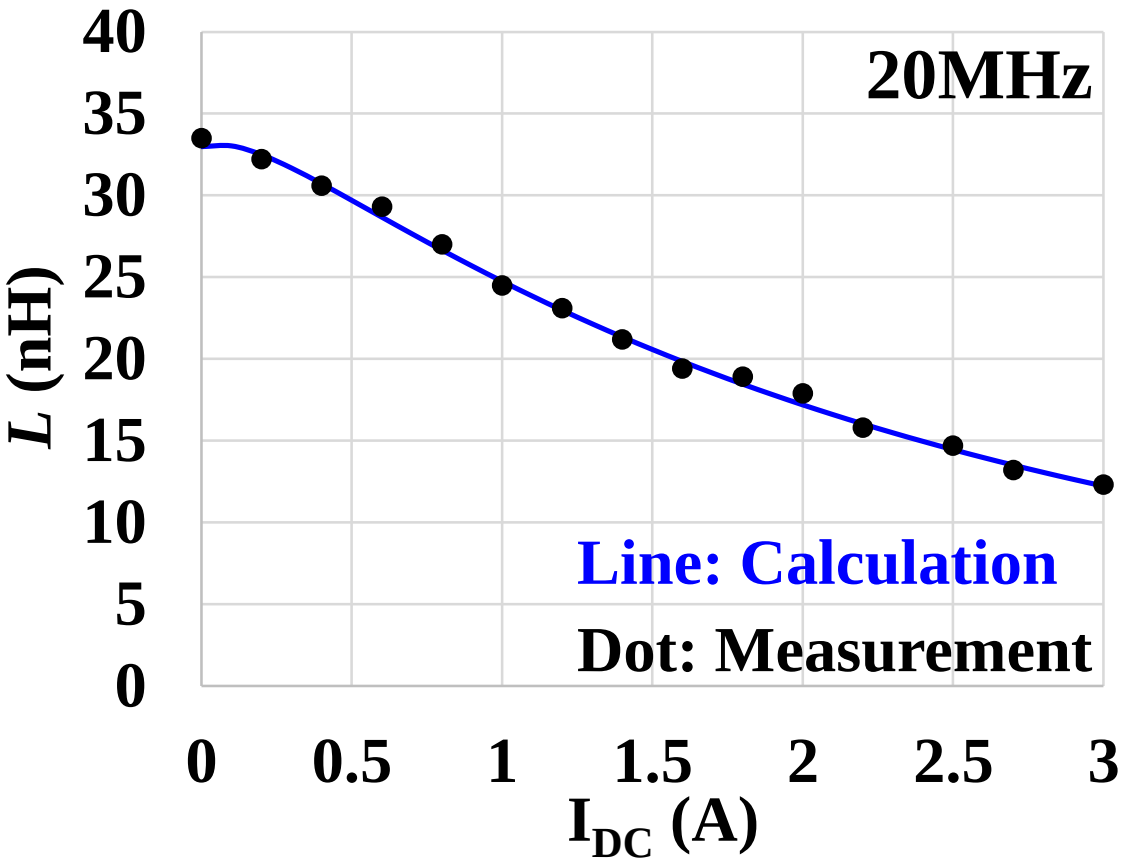


Figure 4.8. Measurement results of inductance under DC bias current.

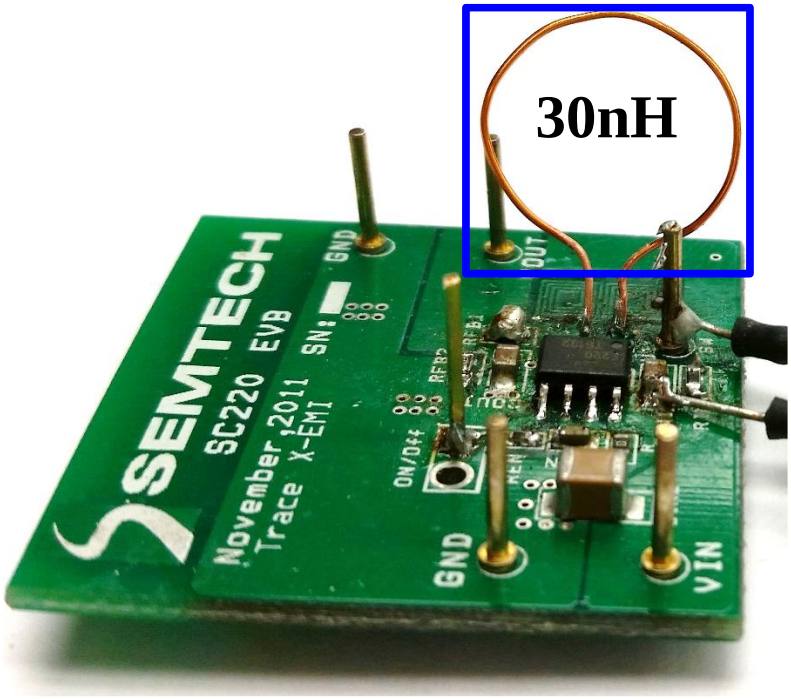


Figure 4.9. SC220 buck evaluation board with a 30nH air core inductor.

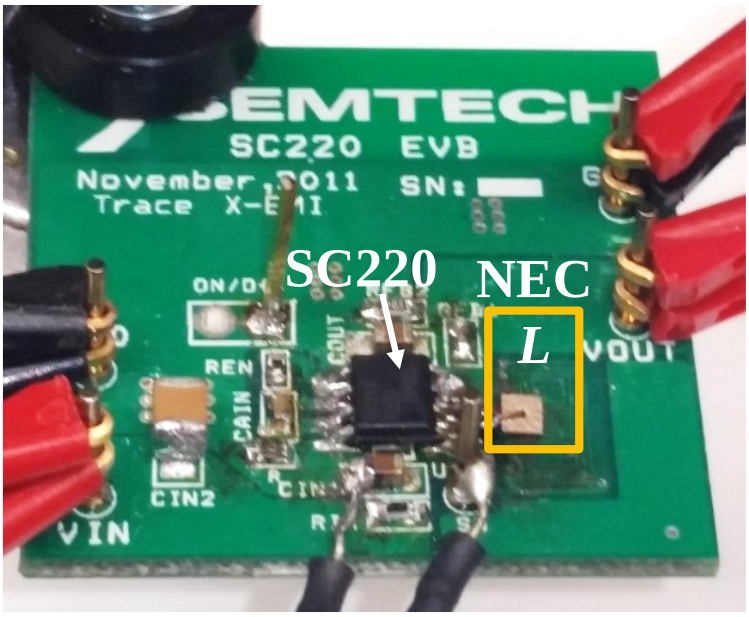


Figure 4.10. Testing setup for the single-phase inductor using SC220.

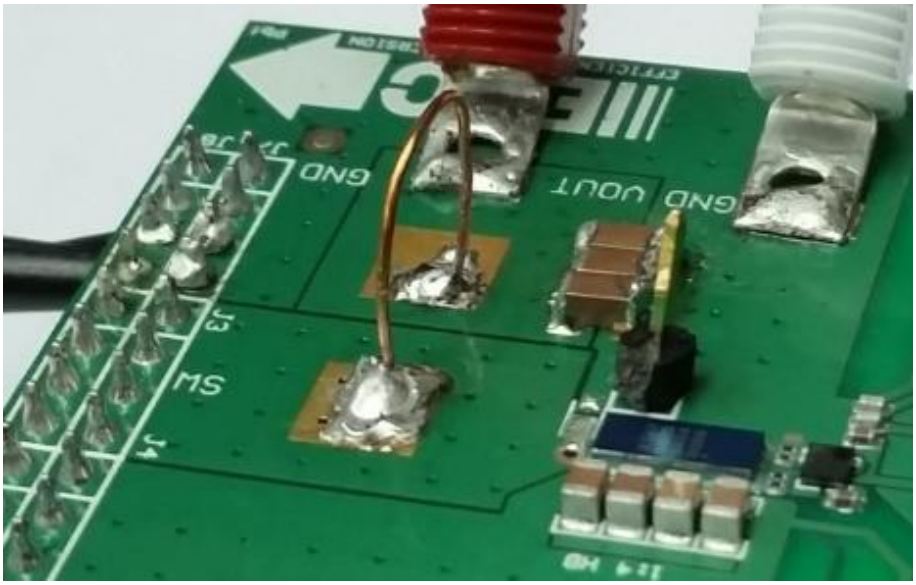


Figure 4.11. EPC9036 testing board with air core inductor.

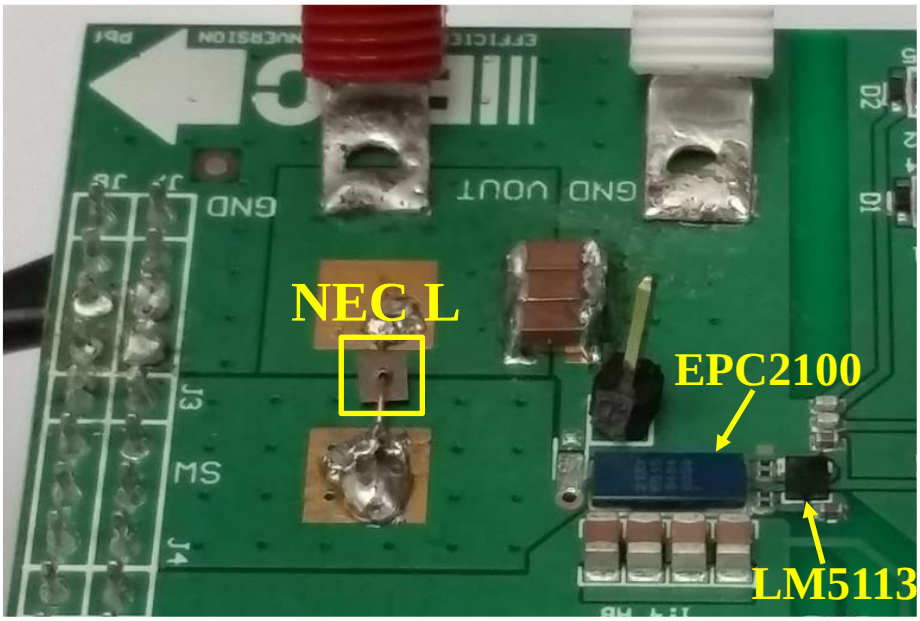


Figure 4.12. Core loss and thermal testing setup for the single-phase inductor using EPC9036.

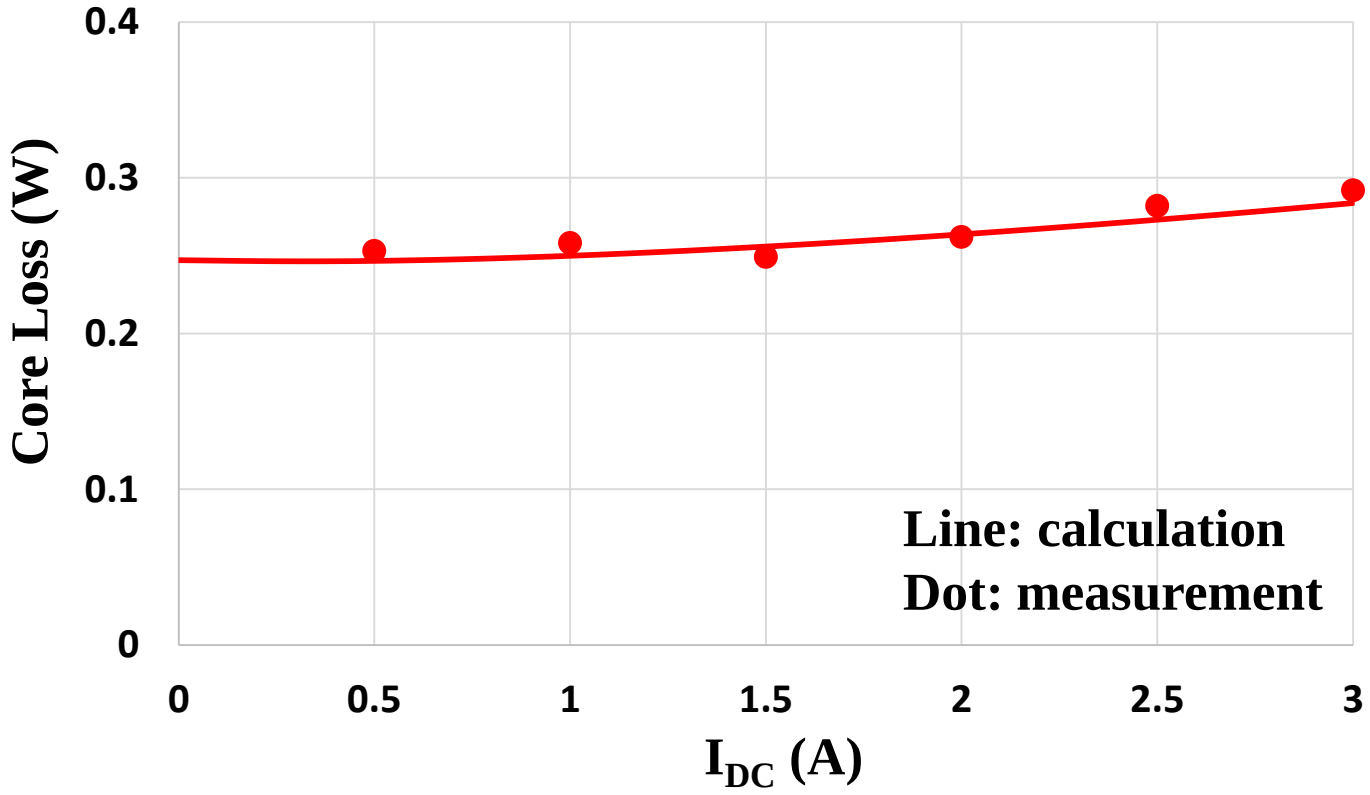
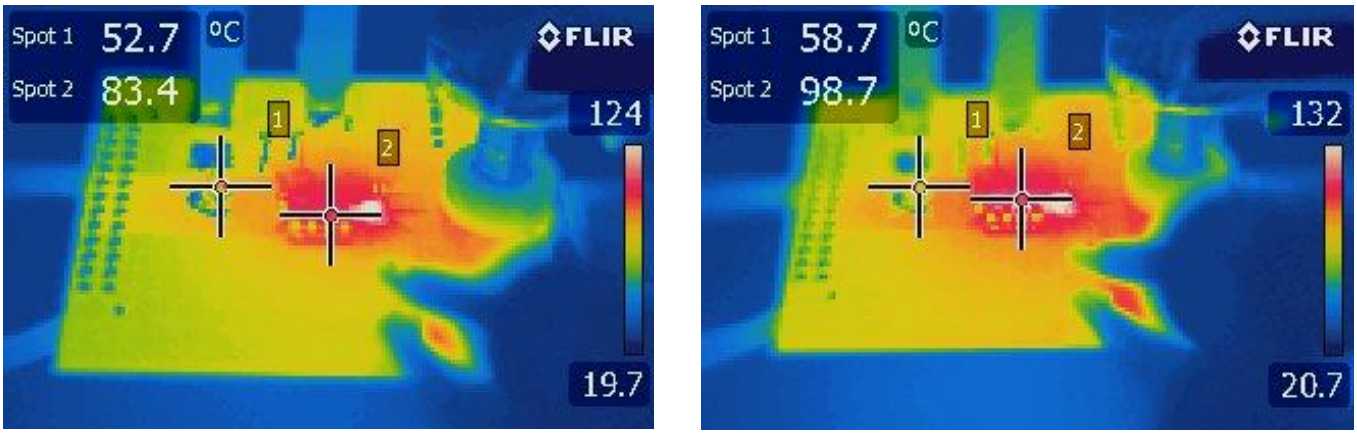


Figure 4.13. Measurement results of core loss at different load condition.

The thermal image of the EPC9036 circuit with single-phase NEC inductor is shown in Figure 4.14. It can be seen that at 20MHz with natural convection, the temperature rise of the inductor at light load (0.5A) is 33℃, and at full load (3A) is 38℃. No thermal issues are observed despite the unusually high core loss density, which can be primarily ascribed to the large surface-area-to-volume ratio of the ultra-low profile inductor structure. It is also worth noting that even though the core loss density is unusually high (>100000kW/m^3), the total core loss is still relatively small (<0.3W) because of the very small core volume.



(a) (b)

Figure 4.14. Thermal image of the EPC9036 testing circuit at 20MHz with natural convection under (a): 0.5A light load condition; and (b): 3A full load condition. Spot 1 indicates the inductor under test; Spot 2 indicates EPC2100 GaN switch.

To test the five-phase integrated inductor, a five-phase buck converter is built with five sets of EPC2100 and LM5113. The testing board is shown in Figure 4.15, and the thermal testing result is shown in Figure 4.16. It can be seen that at 20MHz and natural convection, the temperature rise of the five-phase integrated inductor is 65.2℃ at full load condition (3A per phase). Furthermore, based on the five-phase testing board, a 3D stacked structure of magnetic core within the PCB is built as shown in Figure 4.17, and its thermal testing result is shown in Figure 4.18. The magnetic core is in contact with the PCB ground layer for better heat dissipation. It can be seen that the temperate difference between the magnetic core and the PCB is small (6.7℃ difference between spot 1 and 2 in Figure 4.18), which indicates that the PCB can effectively help inductor heat dissipation and reduce its temperature rise. Comparing Figure 4.16 and Figure 4.18, it can be seen that the inductor temperature rise drops from 65.2℃ to 47.3℃ with the help of heat dissipation from the 3D stacked structure.

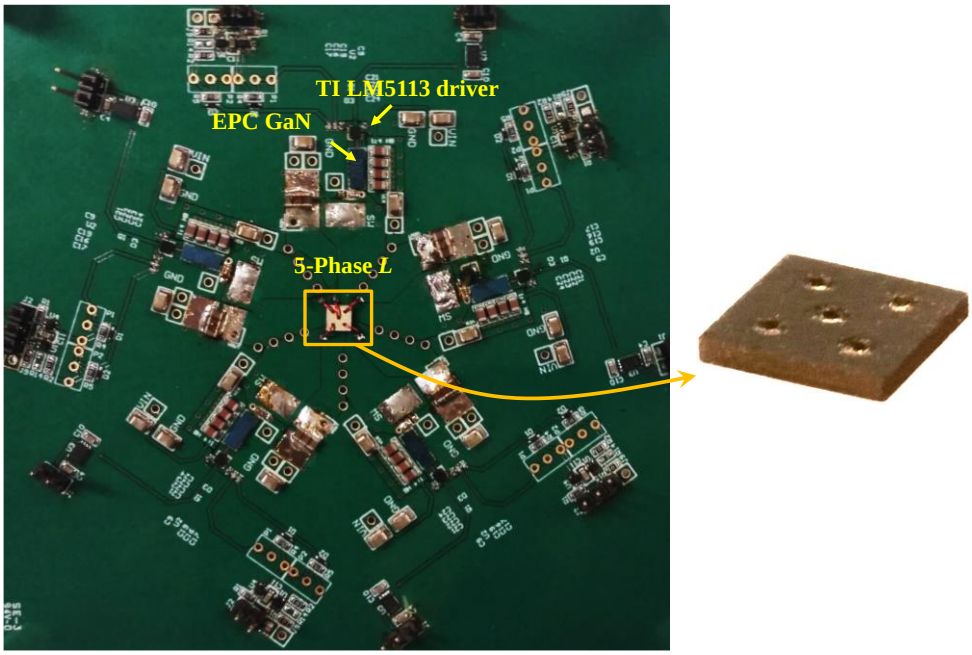


Figure 4.15. Five-phase testing circuit for the five-phase integrated inductor.

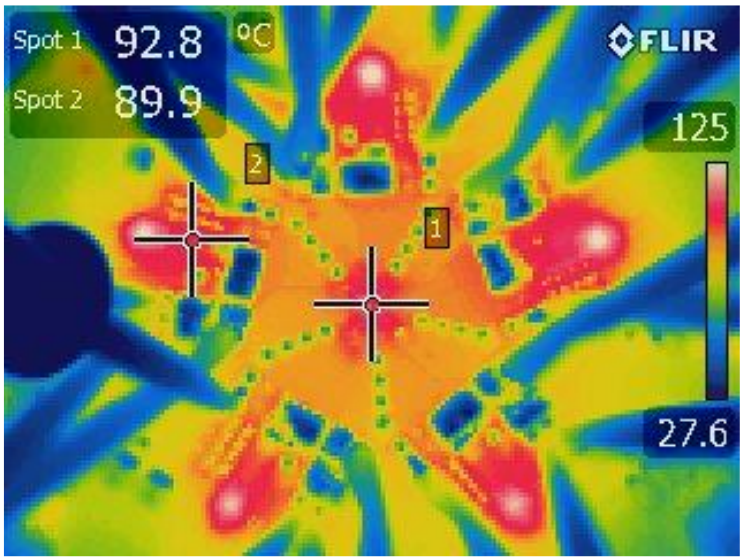


Figure 4.16. Thermal testing result with natural convection for five-phase integrated inductor. Spot 1 indicates the inductor under test; Spot 2 indicates EPC2100 GaN switch.

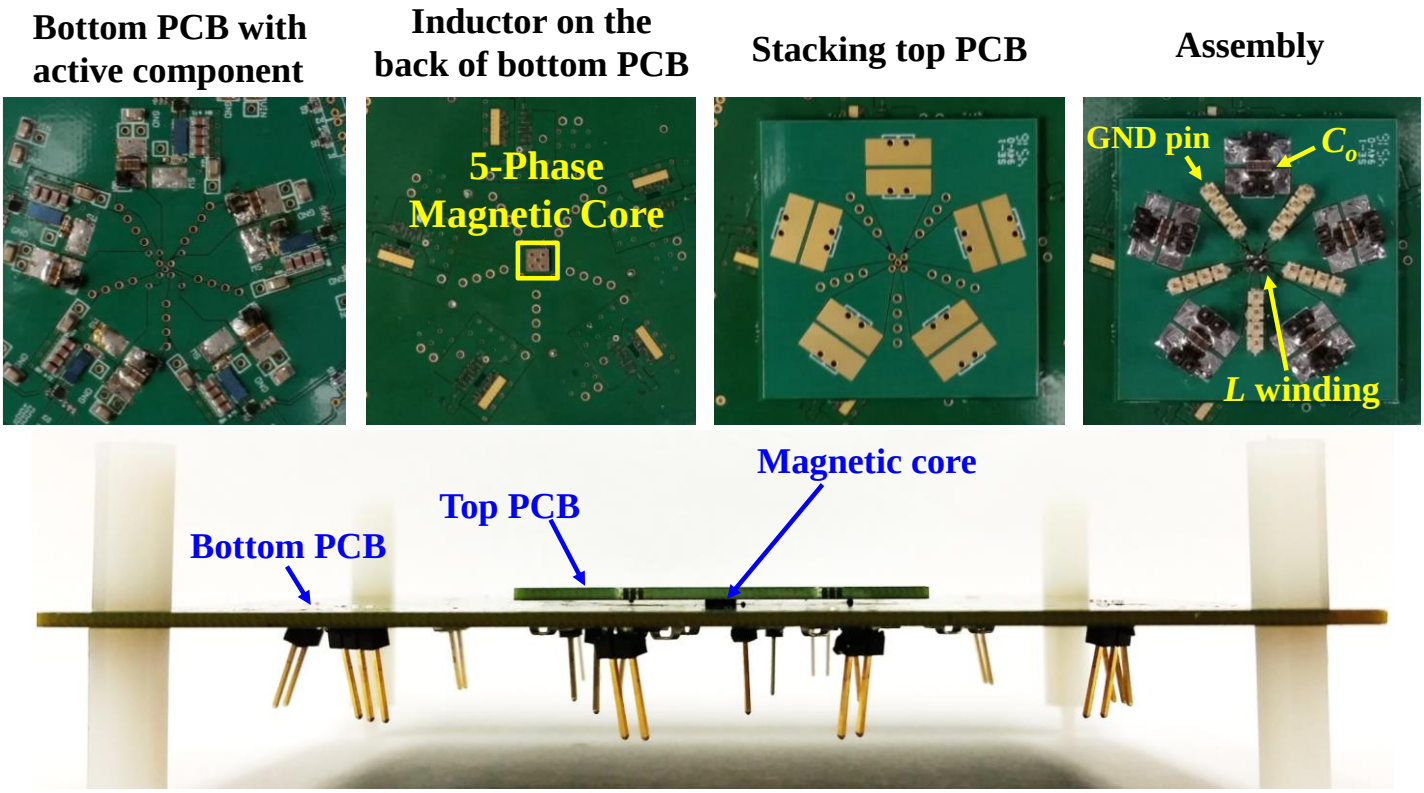


Figure 4.17. Testing board with 3D stacked structure of magnetic core within PCB. The step-by-step building process is shown in the top pictures, and the 3D stacked structure of magnetic core within PCB is shown in the bottom picture. The bottom PCB has the same active components (switching devices and drivers) and layout as the five-phase testing board shown in Figure 4.15.

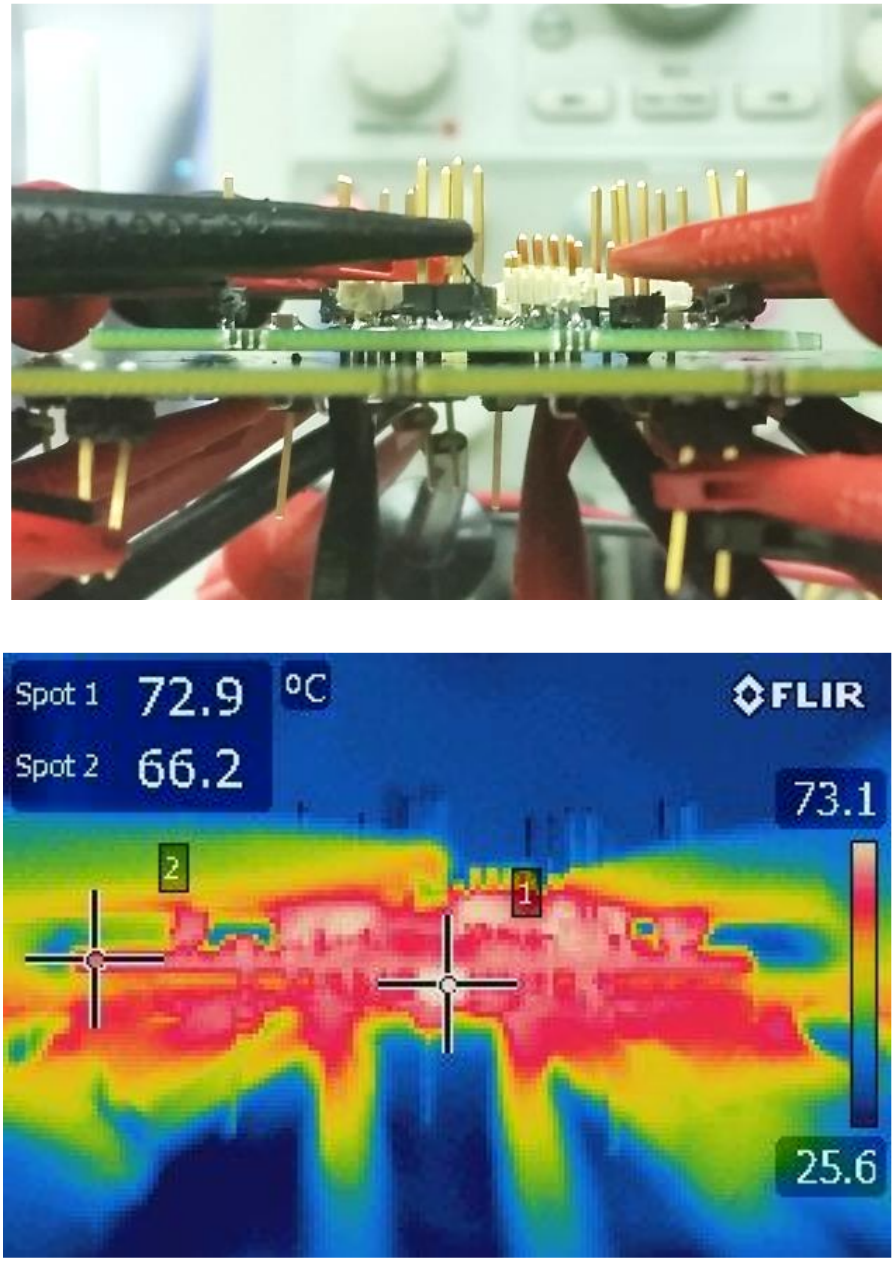


Figure 4.18. Thermal image of the 3D stacked testing circuit at 20MHz with natural convection under full load condition. Spot 1 indicates the inductor under test; Spot 2 indicates the edge of the PCB.

4.3. Prospection of next generation IVR with new GaN driver and magnetic materials

A new GaN device driver PE29100 from Peregine becomes commercially available very recently. Its picture is shown in Figure 4.19. Comparing to LM5113, the new driver allows the use of an external Schottky diode to reduce the driving loss. Besides, it also has a ~70% reduction on minimum on-pulse width when comparing to the LM5113 driver. As mentioned in section 4.2, due to the minimum on-pulse width requirement of LM5113 driver, the highest frequency is limited to 11MHz with the designed input/output value ($3.8V_{in}/1V_o$). To enable a higher operating frequency under the minimum on-pulse width requirement, a larger duty cycle is required. Therefore, in the aforementioned experiments using LM5113, an input/output voltage of $3.2V_{in}/1.6V_o$ is chosen to enable a 20MHz operating frequency. On the other hand, the new GaN driver PE29100 enables the IVR testing up to 30MHz with an input/output voltage of $3.8V_{in}/1V_o$.

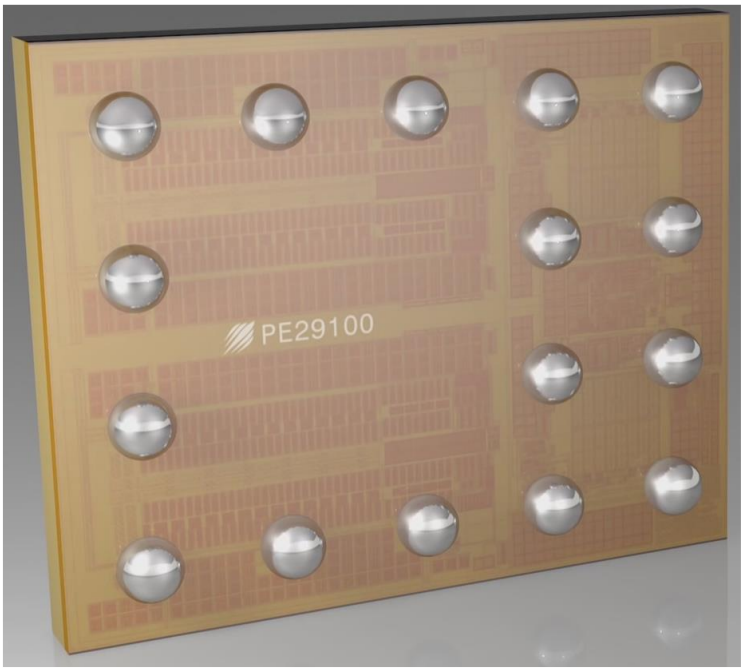


Figure 4.19. New GaN device driver PE29100 from Peregrine.

The testing setup with the new GaN driver is shown in Figure 4.20, and its thermal testing result is shown in Figure 4.21. By pushing the frequency from 20MHz to 30MHz, the inductor loss reduces from 0.28W to 0.25W, and the inductor temperature rise reduces from 38.4℃ to 34.7℃. The reason that the flux density reduction at higher frequency has a more dominant impact on core loss density than the frequency increase for the NEC flake material (given that the flux density and frequency are the two variables determining core loss density in Steinmetz equation).

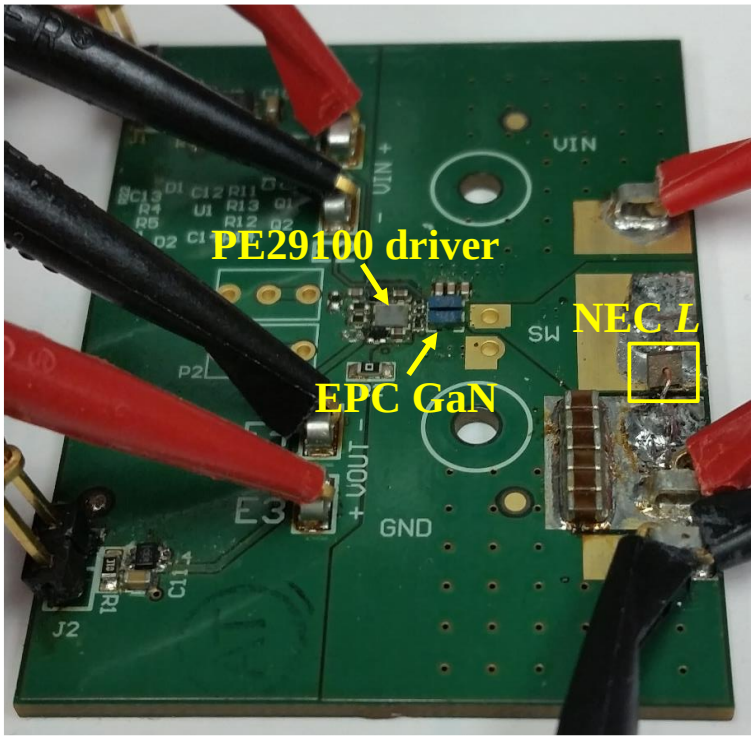


Figure 4.20. Test platform with new GaN driver enabling 30MHz switching frequency.

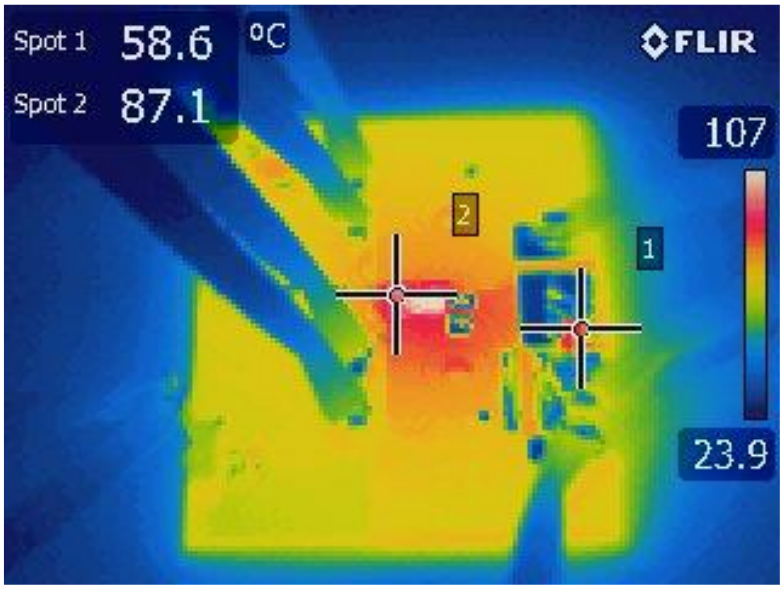


Figure 4.21. Thermal testing result at natural convection, 30MHz, 3.8Vin to 1Vo, and full load condition.

Besides the new driver, a new high frequency magnetic material is also developed by 3M as shown in Figure 4.22.

Figure 4.22. New high frequency magnetic material from 3M.

The core loss density comparison between the new material and the NEC flake material is displayed in Figure 4.23. It can be seen that the new material has a ~70% smaller core loss density than the NEC flake material at very high frequency.

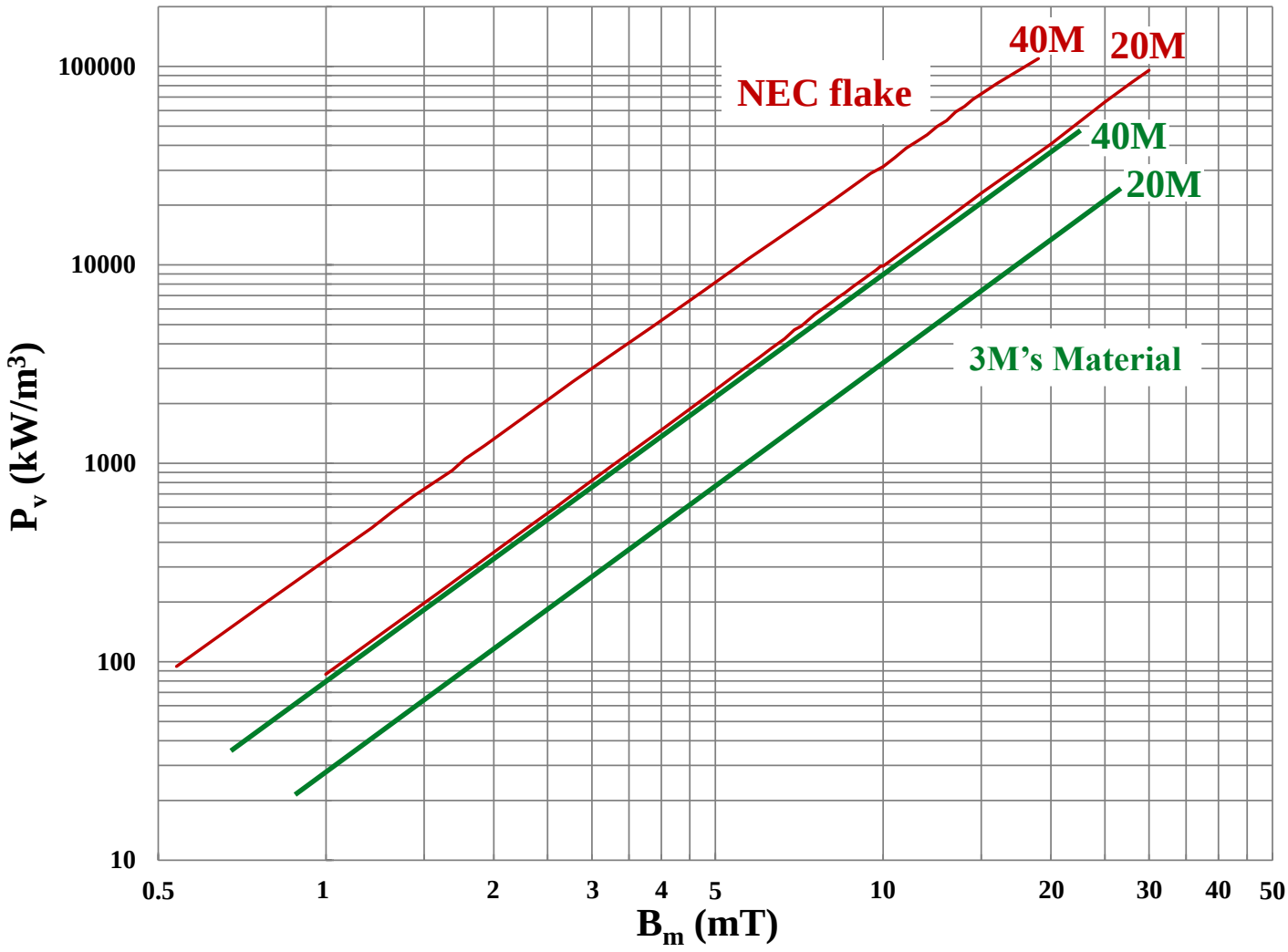


Figure 4.23. Core loss density of the 3M's new magnetic material and its comparison to NEC flake material at very high frequency.

The permeability under DC bias of the 3M's new magnetic material and its comparison to NEC flake material at very high frequency is shown Figure 4.24. It can be seen that in our interested DC bias range in the IVR design (marked by the purple zone), the 3M's new material has comparable permeability with NEC flake material. Furthermore, at higher frequency and higher DC bias level, the 3M's new material has higher a permeability than the NEC flake material, which makes it a good candidates for very high frequency, very high density design.

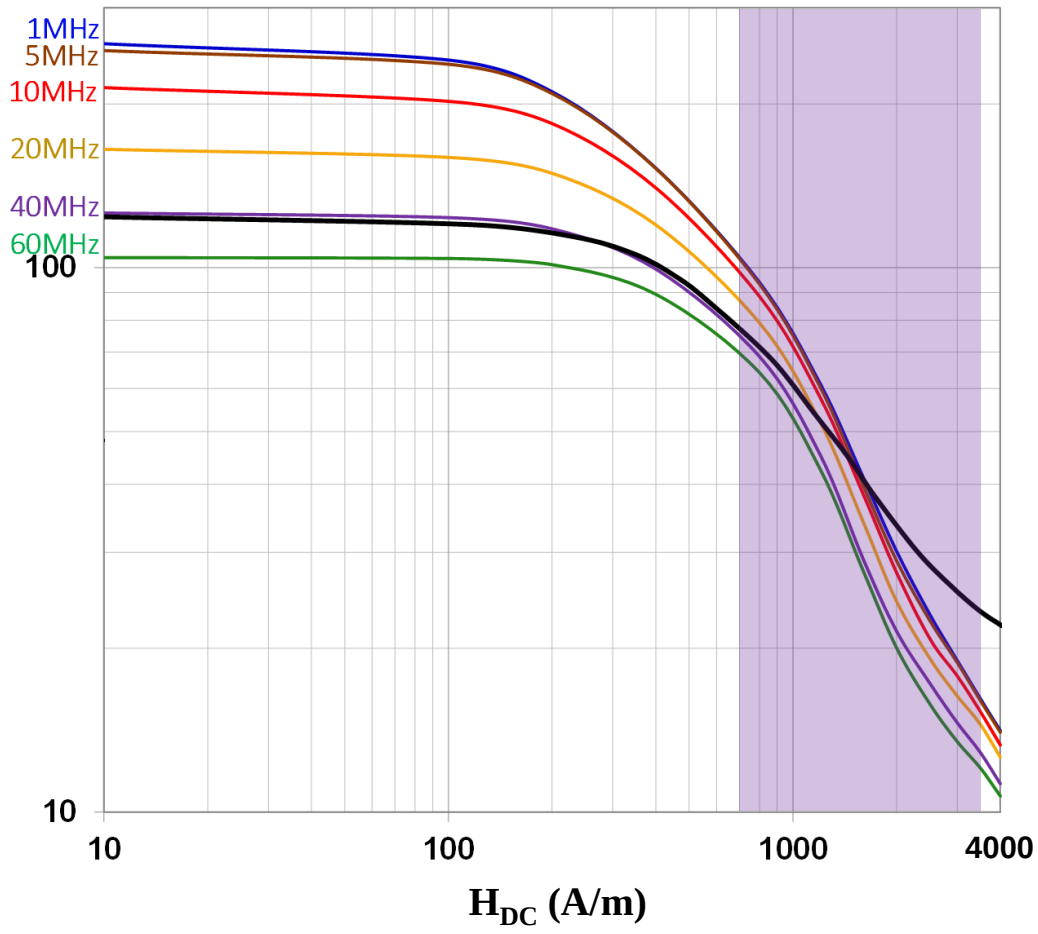


Figure 4.24. Permeability under DC bias of the 3M's new magnetic material and its comparison to NEC flake material at very high frequency. The interested DC bias range in the IVR design is marked by the purple zone.

4.4. Summary

The very high frequency 3D integrated voltage regulator for smartphone is proposed and demonstrated for the first time. Both a single-phase and multi-phase integrated inductor are designed, fabricated and experimentally tested in 20MHz buck converters, featuring a simple single-via winding structure, small size, ultra-low profile, ultra-low DCR, high current-handling ability, air-gap-free magnetics, multi-phase integration within one magnetic core, and lateral non-uniform flux distribution.

The magnetic core with the NEC flake material is operated at unusually high core loss density (>100000kW/m3), while it is thermally manageable. The PCB copper can effectively dissipate the inductor heat with 3D integration.

New GaN device drivers and magnetic materials can further increase the IVR frequency to 30MHz and enable higher density with smaller loss.

Chapter 5. Conclusions and Future Works

5.1. Conclusions

The 3D PCB Integrated POL module is improved with a 2~4% efficiency boost and a >70% footprint savings by reducing the DCR and vertical mounted design. Besides, various low permeability paste materials are applied in the coupled inductor design to control the inductance non-linearity and reduce the fringing flux around the slot.

A new core loss measurement method with partial cancellation concept is proposed and experimentally verified. It enables accurate core loss measurement at very high frequency without the fine-tuning of the cancellation component for each testing sample. Based on the proposed method, the magnetic characterization technique at very high frequency (tens of MHz) is investigated for the IVR inductor design. The issue and solution in the permeability and loss measurement are demonstrated. The LTCC and NEC flake materials are characterized and compared at very high frequency, and the NEC flake shows advantage over LTCC materials from both a permeability and core loss density perspective.

The very high frequency 3D integrated voltage regulator for smartphone is proposed and demonstrated for the first time. Both single-phase and multi-phase integrated inductor are designed, fabricated and experimentally tested in 20MHz buck converters, featuring a simple single-via winding structure, small size, ultra-low profile, ultra-low DCR, high current-handling ability, air-gap-free magnetics, multi-phase integration within one magnetic core, and lateral non-uniform flux distribution. The magnetic core with the NEC flake material is operated at unusually high core loss density (>100000kW/m3), while it is thermally manageable. The PCB copper can effectively dissipate inductor heat with 3D integration. New GaN device drivers and magnetic materials can further increase the IVR frequency to 30MHz and enable higher density with smaller loss.

5.2. Future works

With the new emerging very high frequency GaN driver from Peregrine and the new high frequency magnetic core material from 3M, the 3D integrated multi-phase IVR can be further pushed to 30~40MHz range. As a result, a significant reduction in both magnetic size and loss can be expected.

As the power switching device continues to advance, it is expected that a multi-phase integrated switch with tens of MHz operating frequency would emerge in the near future. It can perfectly accompany with the multi-phase integrated IVR design and 3D integration technique demonstrated in this work to promote the IVR product in the future smartphone.

More advanced packaging technology and thermal management of the smartphone IVR will play an important role to taking advantage of the higher switching frequency in the future.

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