Electrical Transport Properties of Barium Titanate-Based Capacitor Ceramics

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(ABSTRACT)

Electrical conduction mechanisms in $BaTiO_3$-based ferroelectric capacitor ceramics with an emphasis on the X7R type were studied. Dominant charge carriers in this material were identified as conduction band electrons below a temperature of 850°C. This was substantiated by the following results: negative Seebeck coefficients, zero galvanic cell voltage, and evidence of space-charge-limited currents in MLC capacitors and related ceramic.

Effects of chip thickness on the electrical parameters, as well as the I-V characteristics, were studied. Chip electrical parameters such as resistivity, dielectric constant, and activation energy were found to be independent of chip thickness. Effects of ambient were also studied and differences in current-voltage behavior were attributed to surface effects.

Complex impedance spectroscopy proved to be a useful technique in separating grain, grain boundary, and contact contributions to the total impedance. Impedance plots for X7R ceramic revealed negligible contact impedance.

The most probable electrical transport mechanism in X7R ceramic is small polaron hopping, although the possibility of combined small polaron hopping and grain boundary transmission cannot be excluded.

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Chapter 1. Introduction

Pure barium titanate ($BaTiO_3$) is an insulator with an energy band gap of about 3.1 eV at room temperature.[1,2] During World War II, the ferroelectric nature of $BaTiO_3$ ceramic was discovered. Since then, its high dielectric constant below the Curie temperature has found major applications in the capacitor industry. It can, in addition, be used in a variety of applications such as thermistors (utilizing its anomalous resistivity increase above the Curie temperature) and as a piezoelectric transducer (utilizing its piezoelectric property).

1.1 Barium Titanate as a Ferroelectric

From the study of point groups, which are composed of thirty-two crystal classes, it is well known that twenty-one crystal classes are not centrosymmetric. With only one exception (cubic 432), twenty classes show the so-called piezoelectric effect, which is characterized by induced polarization upon receiving stress.[3] In some piezoelectric crystals, the converse of the piezoelectric effect is also possible, i.e. the crystal will be strained when an electric field is applied. This is different from electrostriction in the sense that the former is a linear effect, whereas the latter is quadratic. Also, the strain will remain unchanged, if the applied field is reversed, in case of the

electrostriction. This effect actually occurs in any material, including eleven centrosymmetrical crystal classes.

Ten crystal classes out of the twenty piezoelectric crystal classes show spontaneous polarization, which is temperature dependent. If the temperature of the crystal changes, the pyroelectric effect will be observed due to the polarization change in the direction parallel to the polar axis. Some of the pyroelectric crystals, then, show ferroelectricity, which is characterized by a reversible polarization upon applying an electric field.

In principle, all ferroelectric crystals are pyroelectric and piezoelectric, or can be made so by poling. The relationships between these properties are shown as a Venn diagram in Fig. 1.

In 1920, Valasek first observed ferroelectricity in Rochelle salt.[4,5] Since then, many other ferroelectric crystals have been found, including potassium di-hydrogen phosphate, barium titanate, and a number of other compounds whose crystal structures are similar with these crystals.[3]

A ferroelectric crystal is characterized by a reversible polarization, a spontaneous polarization even in the absence of an external electric field, and a hysteresis loop. (Fig. 2)

Table 1 lists properties of some of interesting ferroelectric crystals (Curie temperature T_c, the spontaneous polarization P_s, and the Curie constant C).

Barium titanate is the ferroelectric material that has been most widely investigated. Its crystal structure is a perovskite-type, named after the mineral perovskite ($CaTiO_3$), and is shown in Fig. 3.[3,6,7] In this structure, the barium and oxygen ions combine to form a face-centered cubic lattice with the smaller titanium ions in octahedral interstitial sites located at the cube center. Hence, the coordination numbers for the barium and titanium ions to the oxygen ion are 12 and 6, respectively. Barium titanate is chemically and mechanically very stable, and exhibits ferroelectric properties at room temperature. In addition, it is available in virtually any shape in polycrystalline ceramic form.[3]

Pure $BaTiO_3$ undergoes a phase transition at 120°C, which is displacive and first order in character because the whole sublattice is displaced and the polarization is not continuous at the transi-

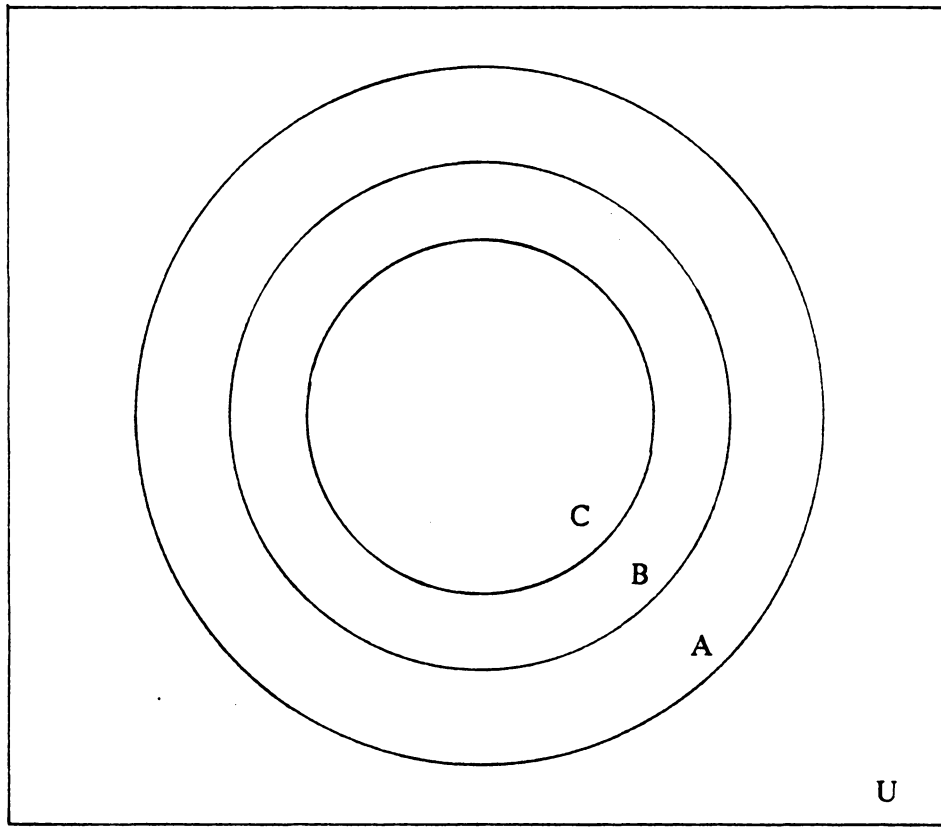

Figure 1. **A Venn diagram of crystal classes**

U : total crystal classes (32)

A : piezoelectric crystal classes (20)

B : pyroelectric crystal classes (10)

C : ferroelectric crystal classes ($\leq$ 10)

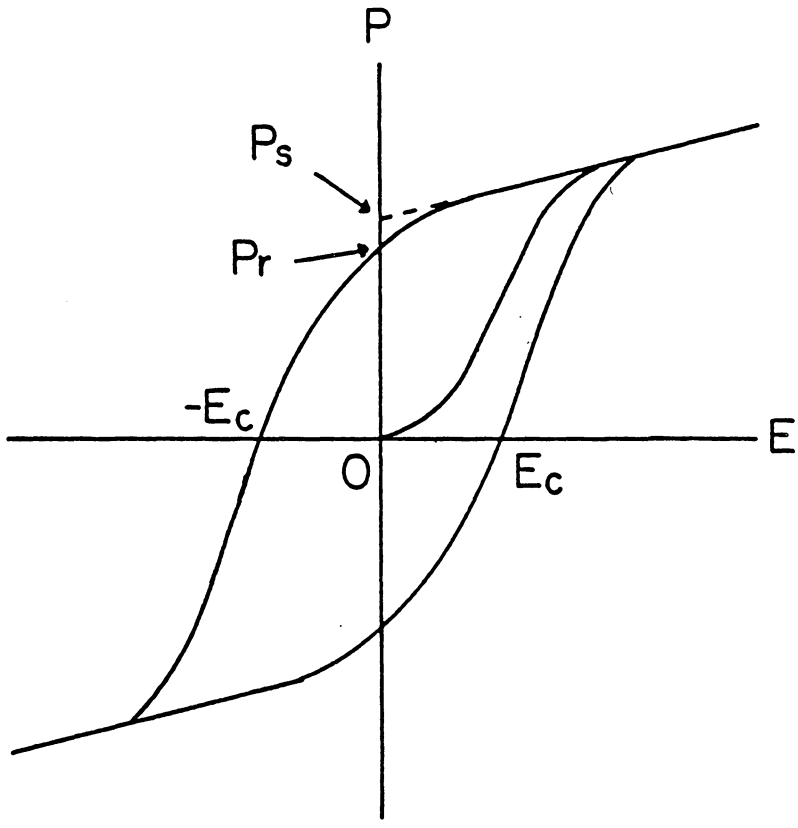

Figure 2. **A typical ferroelectric hysteresis loop** [7]

P_s : the spontaneous polarization

P_r : the remanent polarization

E_c : the coercive field

The polarization (**P**) is defined as the dipole moment (**p**) per unit volume averaged over the volume of a cell (v).

$$\mathbf{P} = \frac{1}{v}\ \mathbf{p} = \frac{1}{v}\Sigma\, q_n\, \mathbf{r}_n$$

where $\mathbf{r}_n$ is the position vector of the charge q_n .

Table 1. Properties of ferroelectric crystals [3,7]

Sample	T_c (°K)	P_s at T (°K) ($\times 10^{-6}$C/cm^2)		Year Reported	Curie Constant
$NaKC_4H_4O_6 \cdot 4H_2O$[1]	296	0.25		1920	2.2×10^3
KH_2PO_4	123	5.3	96	1935	3.3×10^3
KD_2PO_4	213	4.5		1942	
KH_2AsO_4	96	5.0	80	1938	
$(NH_2CH_2COOH)_3 \cdot H_2SO_4$[2]	322	2.8	293	1956	3.2×10^3
$(NH_2CH_2COOH)_3 \cdot SeO_3$[3]	295	3.2	273		
$BaTiO_3$	393	26.0	296	1945	1.5×10^5
$SrTiO_3$	~0	3.0	4		
$KNbO_3$	712	30	523	1951	2.0×10^5
$PbTiO_3$	763	> 50	300	1950	
$LiNbO_3$	1470	300			
$LiTaO_3$	890	23.3	720		

[1] Rochelle salt

[2] Tri-glycine sulfate

[3] Tri-glycine selenate

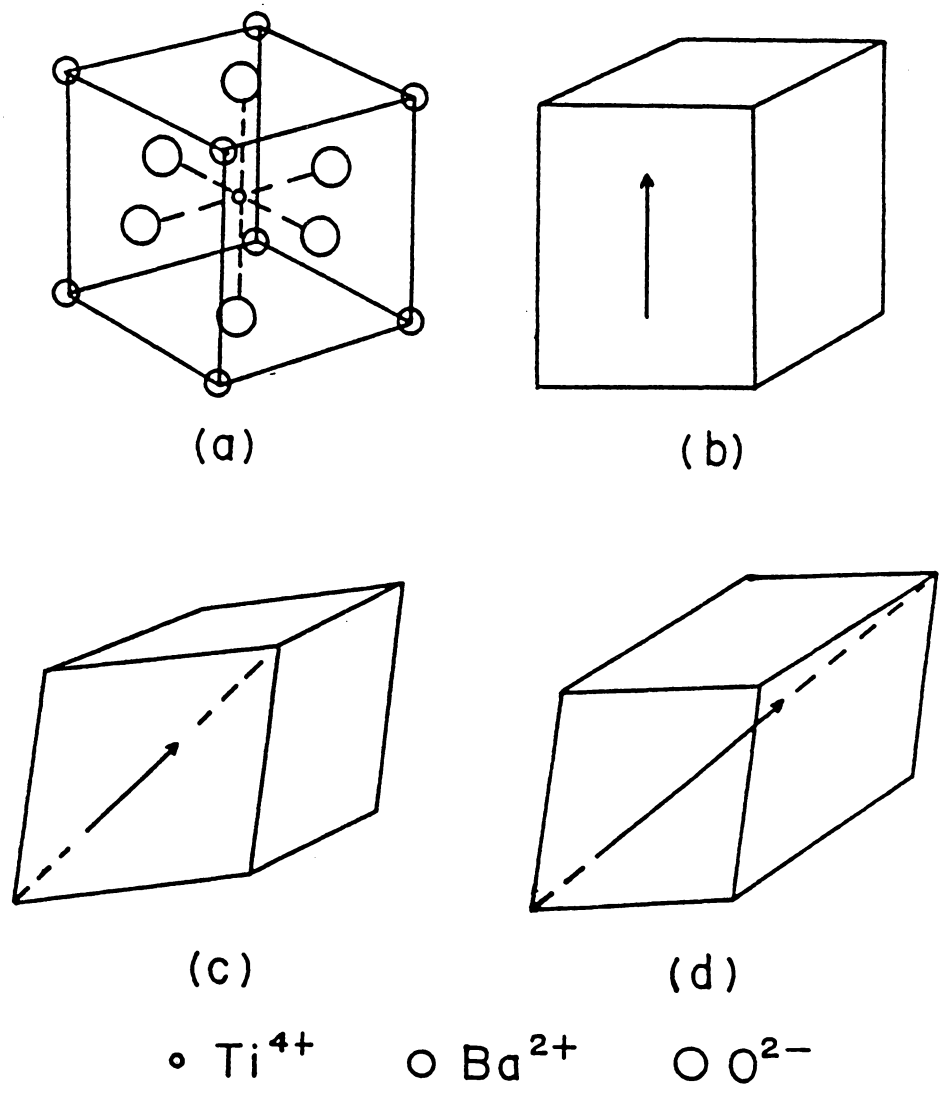

Figure 3. **Crystal structures and unit cells of barium titanate in different phases** [3,7,8]
(a) cubic unit cell
(b) tetragonal unit cell
(c) monoclinic unit cell
(d) rhombohedral unit cell

(In (b), (c) and (d), Arrows denote directions of the spontaneous polarization.)

tion temperature.[7] (This temperature is called the Curie temperature.) Above this temperature, the crystal is cubic perovskite type, and paraelectric. All of the spontaneous polarization disappears and the crystal behaves as a normal dielectric. Polarization is now directly proportional to the applied electric field, and does not show any hysteresis. Below the Curie temperature, to 5°C, the symmetry of the crystal is tetragonal. The cubic unit cell is distorted to produce a tetragonal unit cell, where one of the cube edges is expanded and the other two contracted ($c > a$; Fig. 3 (b)) At 5°C, the symmetry of the crystal changes to monoclinic and, finally, at $-$ 80°C, it changes to rhombohedral. (Fig. 3 (c),(d))

1.2 Barium Titanate as a Capacitor Dielectric

At present, many commercial capacitor dielectrics are based on barium titanate, although attempts have been made to use relaxor dielectrics which are based on lead-manganese-niobates (PMN). Barium titanate has a very high dielectric constant of about 1,500 compared to those of traditional porcelain dielectrics ($\sim$ 10). Also, it has a permittivity peak at the Curie temperature, and can be easily modified for practical applications by doping with other perovskite-type compounds.[9] Usually, a number of dopants are added to get desired capacitor characteristics. Their individual roles are different, and are summarized in detail elsewhere.[10]

The exact dielectric compositions vary widely from one manufacturer to another, and are, in general, proprietary.[11] Some of the desired modifications are a lowering of the permittivity peak from the Curie temperature (120°C) to near room temperature, flattening the permittivity versus temperature curve by grain growth inhibition, lowering the effective sintering temperature by forming liquid phase at the firing temperature, and increasing the high voltage stability. These can be achieved by mixing barium titanate with various additives.

Various $BaTiO_3$-based dielectric compositions are commercially available, with different specifications of temperature coefficient of capacitance (TCC). X7R and Z5U types are the types most

widely used, and the Electronic Industries Association (EIA) specifies their TCC tolerances as follows:

a) X7R : ±15% maximum capacitance change from +25°C value over the temperature range − 55°C to +125°C.

b) Z5U : +22% ~ −56% maximum capacitance change from +25°C value over the temperature range +10°C to +85°C.

It is noted from the above statements that neither compositions nor dielectric constant values are specified. Also, it is seen that the X7R's specification is more strict than the Z5U's from the viewpoint of temperature stability. Typical room temperature dielectric constant values for these two types are ~2000 and ~5000, respectively.

There are two types of failure modes in multilayer ceramic (MLC) capacitors; intrinsic and extrinsic. Extrinsic failure mechanisms are mostly due to processing defects such as delaminations, cracks, voids between ceramic layers, and electrode shunting. These defects are mainly responsible for most of the earlier breakdown of devices, and can be screened out by various test methods.[12] On the other hand, intrinsic failure mechanisms are due to the inherent chemistry and physics of the MLC device, and not due to faulty manufacture. The most important mechanism for intrinsic failure is ionic and vacancy migration coupled with metal diffusion from the electrode into the ceramic, and generally require longer term service period to appear than the extrinsic mechanisms. However, where the very high standard of reliability is required, for example, in military applications, these intrinsic failure mechanisms are just as important as extrinsic ones, and will become even more important, as dielectric layers become thinner to achieve volumetric efficiency.

Intrinsic degradation of insulation resistance, which appears as increase in leakage current with time, is the major failure concern for high resistance, high dielectric constant ferroelectric MLC and thick film capacitors.[13,14] These capacitors, unlike nonferroelectric capacitors such as titania-based

NPO (or COG) type,† show aging in both dielectric constant and dissipation factor with time. This is a consequence of the presence of ferroelectric domains, and fairly well understood.[15] However, very little research were carried out in degradation of insulation resistance which is responsible for capacitor lifetime. Better understanding of leakage current mechanisms in MLC capacitors is, therefore, of prime importance, and the main issue of this study. This will be discussed further in the next section.

1.3 Research Objectives

The main interest in $BaTiO_3$-based ceramic capacitors exists because of its excellent dielectric properties, and considerable research has been done in that area. However, relatively little has been done in the investigation of electrical transport mechanisms of capacitor leakage current, which results from the intrinsic degradation of the capacitor ceramics.

The dominant leakage current charge carrier in multilayer ceramic (MLC) capacitors, and its mode of transport, have not been established. The carriers can be electronic (electrons, holes) and/or ionic (cations, anions, vacancies). Several authors have reported conflicting conclusions regarding the nature of charge carriers, and their modes of transport, in MLC capacitors.[12,16,17] For $BaTiO_3$ ceramics, both n and p types of conduction have been reported, with the conductivity strongly affected by impurities and oxygen partial pressure.[18,19] Also, space charge limited current (SCLC) and Schottky current have been reported.[19-23] In order to better understand the electrical transport properties in high resistivity $BaTiO_3$-based capacitor ceramics, it is necessary to address the following questions.

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† NPO type has TCC tolerance of < 30 ppm/ °C from − 55°C to + 125 °C, and has usually a dielectric constant value of less than 100.

1) What is the dominant charge carrier in $BaTiO_3$-based capacitor ceramics? Does it change from ionic to electronic or from electronic to ionic at some temperature?

2) What are the sources of the charge carriers? Are they bulk carriers already present in the material, injected carriers from electrodes, or surface currents?

3) What is the carrier transport mode? Does it also change with certain parameters such as time, temperature, and applied voltage?

4) What role, if any, does the grain boundary play in the impedance of high resistivity ceramics?

It is the objective of this research to address these questions. These questions are approached by means of the following experiments:

1) Thermoelectric and conductivity measurements, which give information about the sign, concentration, and mobility of the dominant charge carrier;

2) Transference number measurements, which determine whether the charge carrier is electronic or ionic;

3) Current-voltage and current-temperature relationship measurements, which are determined by the mode of transport;

4) Complex impedance measurements, combined with d.c. resistivity measurements, which hopefully identify the separate contributions of grain, grain boundary, and contact impedances to the total impedance.

Chapter 2. The Theory of Electrical Conduction in Barium Titanate

In $BaTiO_3$-based multilayer ceramic capacitors, the dominant charge carrier and its mode of transport have not been conclusively clarified. The leakage currents have been attributed to various mechanisms such as Poole-Frenkel emission, [16] and to oxygen vacancy movement, [12,17] through the 1.38 eV activation energy for diffusion of oxygen vacancies in polycrystalline $BaTiO_3$.

In this chapter, several theories of conduction mechanisms in $BaTiO_3$ will be reviewed. These include ohmic current, space-charge-limited current, ionic current, Schottky current, and Poole-Frenkel current, and those transport mechanisms such as grain boundary barrier transmission and small polaron hopping transport.

Some of the proposed theories may be more pertinent to high resistance capacitor ceramics than others. In the following, each of the above will be presented in some detail and its applicability to capacitor ceramics will be considered.

2.1 Ohmic Current

Ohmic current is proportional to voltage and can exist both for electronic (electrons and holes) and ionic carriers (cations, anions, and vacancies). In this type of current conduction, the metal-insulator contact does not act as a blocking layer to current flow. The voltage V dependence of current I is expressed as[13]

$$I = V\frac{A}{d}\sum_i q_i \mu_i n_i \qquad (2.1)$$

where q_i is the charge of carrier i, A, d the cross-sectional area and thickness, n_i the concentration of carrier i, and μ_i the drift mobility of carrier i.

Eq. 2.1 is an another expression of Ohm's law. ($J = \sigma E$; σ = electrical conductivity) For transport dominated by small polaron hopping or by grain boundary transmission, the temperature dependence of I is contained in n and μ, and may be expressed in terms of activation energy E_A :

$$I = I_0 \exp\left[\frac{-E_A}{kT}\right] \qquad (2.2)$$

where I_0 is a constant at given voltage and E_A ($= E_{A,n} + E_{A,\mu}$) is the sum of the carrier concentration and mobility activation energies. In MLC capacitors, E_A may arise from grain boundaries or small polaron hopping.

Ohmic current is observed in almost all materials including dielectrics and even in rectifiers at low values of applied electric field.

2.2 Space Charge Limited Current (SCLC)

As the electric field at the cathode increases, the injected electron concentration across the electrode-insulator junction exceeds the native bulk electron concentration, assuming the current

carriers are only electrons. If the insulator is perfect and trap-free, this is the direct, solid-state analog of the thermionic vacuum diode, where vacuum is replaced by the insulator. Even though space-charge-limited ionic currents were reported for some materials such as ice, KCl, and SiO_2 films, the space-charge-limited current in MLC devices applies to electronic carriers because ions are not expected to be injected from the electrodes in this case.

For the perfect insulator with planar electrodes and shallow traps (where shallow traps are defined by the traps at the energy level E_t above the Fermi energy level E_f, or $(E_t - E_f)/kT > 1$), the current-voltage relation is given by[24]

$$I = \frac{9}{8} A\theta\varepsilon\mu V^2 / d^3 \qquad (2.3)$$

where ε is the dielectric constant and θ is a trapping parameter defined for shallow traps by the relation

$$\theta = \frac{n}{n_t} = \frac{N_c}{gN_t}\exp\left[\frac{E_t - E_c}{kT}\right] \cong \frac{N_c}{2N_t}\exp\left[\frac{-\Delta E}{kT}\right] \qquad (2.4)$$

where N_c is the conduction band density of states and N_t the shallow trap density, located at energy ΔE below the conduction band edge, g the ground-state degeneracy factor for the traps (assumed to be two), E_c the conduction band energy level. θ is a constant, independent of injection level, so long as the traps remain shallow. As shown in Eq. 2.4, it is defined by the ratio of free carrier concentration n to trapped carrier concentration n_t.

The above is for planar electrodes. Electron current from a hemispherical point cathode emitting toward a planar anode can be described by the relation[24,25]

$$I \cong \frac{2\pi\sqrt{2}}{3}\mu(\theta q\varepsilon n_0)^{1/2} V^{3/2} \qquad (2.5)$$

where n_0 is the thermal equilibrium concentration of free carriers and the other parameters were previously defined. This case may pertain to space-charge-limited current injected from rough points, such as electrode asperities present in MLC capacitors.[13]

The two types of SCLC described above are for specific electrode geometries and a single discrete shallow trap. In real cases, these are unlikely and the current-voltage relations are modified towards a voltage exponent greater than two due to distributed trap energy levels and diffusion currents which was neglected above.[24,25]

2.3 Ionic Current

One type of charge carrier which is always present in ionic solids is due to ions, and is available for electrical conduction even though its transference number is often small. It was reported that the dominant charge carriers in ceramic $BaTiO_3$ are not electronic but ionic below 300°C, whereas the electronic conduction prevails above 500°C.[26]

In contrast, Chang et al.[27] recently studied both undoped and acceptor-doped $BaTiO_3$ ceramics and concluded that, at oxygen partial pressures higher than about 0.01 atm, ionic conduction is not detectable below about 800°C for both types of barium titanates. In addition, similar ionic transference measurements were made for several types of $BaTiO_3$-based ceramics in this study, and the results show no significant ionic conduction in the temperature range of 400 ~ 850°C. This will be discussed in detail, in Chap. 5.

2.4 Schottky Current and Poole-Frenkel Current

In this case, the electron or hole currents increase due to the lowering of potential barrier by an external voltage, either at the electrode (Schottky effect) or at a trap or grain boundary in the

bulk (Poole-Frenkel effect). Both currents have exponential dependence on the electric field and can be expressed by the relation[13]

$$I = I_0 \exp\left[\frac{B}{T}(E/\varepsilon_r)^{1/2}\right] \qquad (2.6)$$

where B is a constant, E the electric field, and ε_r the relative dielectric constant.

Since Schottky effect only occurs at rectifying contact, this probably does not apply to MLC capacitors. However, the Poole-Frenkel effect cannot be excluded due to the possibility of electrons present in potential wells at traps and grain boundaries.

2.5 Grain Boundary Barrier Transmission

The transmission across grain boundaries controls the electron transport for polycrystalline materials such as varistors, PTC thermistors, and polycrystalline silicon, and the conductivity activation energy is determined by the grain boundary barrier height. Over certain voltage ranges, the current I can be expressed by Eq. 2.2.

$$I = I_0 \exp\left[\frac{-\varphi_B}{kT}\right] \qquad (2.7)$$

where activation energy E_A in Eq. 2.2 has been replaced by the potential barrier height φ_B. Assuming grain boundaries in high resistance capacitor ceramics may play the same role as those in grain boundary controlled devices, the model of possible role of grain boundaries for high resistance, high dielectric constant capacitor ceramics has been proposed under the following simplifying assumptions: [28] 1) the grains and the grain boundaries are homogeneous and uniform; 2) the charge due to the polarization discontinuity between grains is neglected; 3) the charge associated with the grain boundary is due to trapped electrons (at the grain boundary) and equal, compensating space charge; 4) the grain boundary itself is infinitely thin so that no other intergranular

phases or inclusions can exist there. This model is primarily based on the Schottky approximation, and the grain boundary potential energy diagram is shown in Fig. 4.

Both grain boundary capacitance and resistance are governed by grain boundary trapped charge Q_{GB}, which causes the conduction band barrier of height φ_B. Grain boundary capacitance for such a model is given by

$$C_{GB} = \frac{\varepsilon_r \varepsilon_0 A}{NW} \qquad (2.8)$$

where ε_r is the relative dielectric constant, ε_0 the absolute permittivity of free space, A the grain boundary area parallel to the electrodes, N the number of grain boundaries in series between electrodes, and W the grain boundary depletion layer width.

The grain boundary potential barrier transmission mechanism was originally proposed for semiconducting ceramics, where grain resistance is usually negligible. This will be discussed in greater detail in Chap. 3.

2.6 Small Polaron Hopping Mechanisms

There are probably two types of electronic conduction mechanisms which are pertinent to polycrystalline oxides. One of them, grain boundary barrier transmission, will be discussed in detail in Chap. 3, and is based on the classical band theory. The other is called hopping transport.

In ionic crystals with a narrow conduction band, a "polaron" may be formed as a result of the interaction between the electronic carrier and the lattice phonon. This quasi-particle "polaron" is the associates of the electronic carrier plus its polarization field. When the association is weak, a large polaron is formed, and this moves as quasi-free electrons in the electric field.

If the interaction between the carrier in the conduction band of a crystal and the lattice phonons is stronger than the conduction band width, i.e. if the lattice distortion induced by the electronic

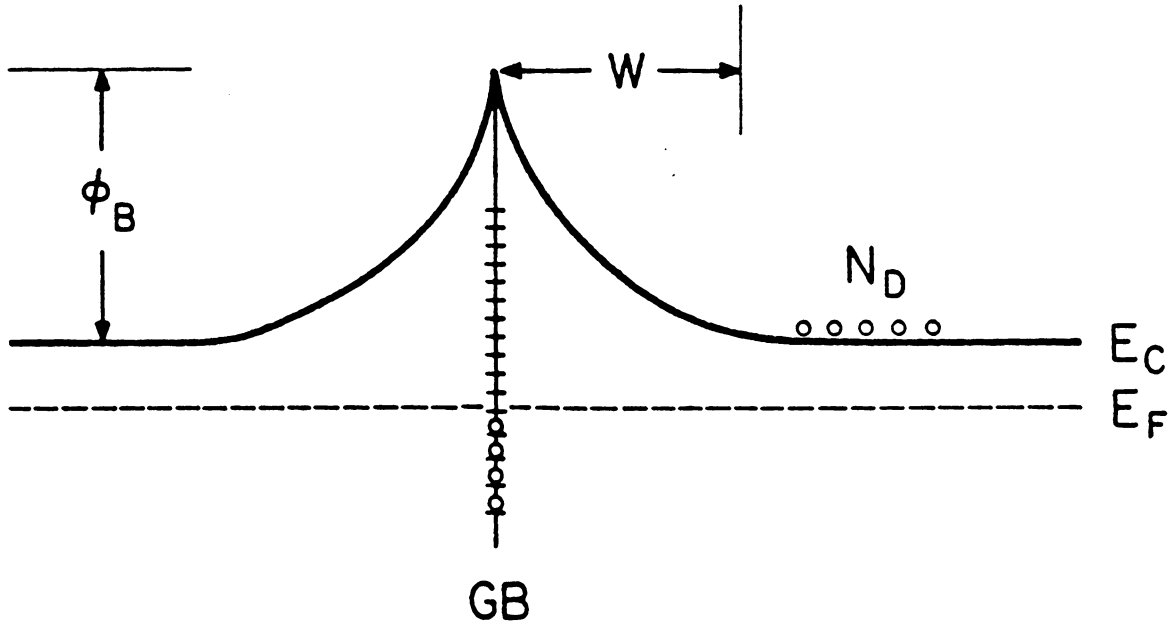

Figure 4. **Grain boundary potential energy barrier of n-type materials**

φ_B : zero-bias potential barrier height

W : the space charge width

N_D : the donor density in the grain

E_F : Fermi energy level

E_C : Energy level of the bottom of the conduction band ($\equiv 0$)

carrier has the dimension smaller than the lattice constant, a "small polaron" can be formed.[29] This small polaron can be transported in an electric field by two possible mechanisms.[30,31] At sufficiently low temperature, it travels like a free carrier but with very high effective mass m^*, where a classical effective-mass approximation is applicable. As temperature increases, the phonon energy increases, and the conduction band width also decreases. Hence, at temperatures roughly higher than the half of the Debye temperature Θ_D,† it moves by thermally activated hopping process from one hopping site to the next. (the classical band theory does not apply any more.)

The strength of the electron-lattice phonon interaction is given by a dimensionless coupling constant α [32,33]

$$\alpha = \frac{e}{h}\left[\frac{m}{2}h\right]^{1/2}\left[\frac{1}{\varepsilon_\infty} - \frac{1}{\varepsilon_s}\right]\left[\frac{m^*}{m\omega_l}\right] \qquad (2.9)$$

where ε_s and ε_∞ represent the static and optical dielectric constants, respectively, ω_l is the longitudinal optical phonon frequency near zero wave vector and m^* is the band mass of the electron. Usually, the values of α are higher in ionic crystals than in covalent crystals.

If an electron is injected into the conduction band of an ionic solid and the mobility of the electron is sufficiently low, the surrounding lattice atoms or ions become polarized by the charge of the electron, and lower the energy of the system by emitting longitudinal optical phonons. The number of lattice phonons surrounding the injected electron is given by $\frac{1}{2}\alpha$.[32] The energy reduction or polaron energy E_p is given by [31,33]

$$E_p = -\frac{1}{2}\frac{e^2}{r_p}\left[\frac{1}{\varepsilon_\infty} - \frac{1}{\varepsilon_s}\right] \qquad (2.10)$$

where r_p is the radius of the polaron.

Small polaron hopping mobility μ_p is written by [34,35]

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† The Debye temperature is defined by $h\omega_D/2\pi k$ where ω_D is the characteristic wavelength, and the other parameters have their usual meanings.

$$\mu_p = \mu_0 \frac{1}{2\pi} \frac{h\omega_0}{2\pi kT} \exp\left[- \frac{E_A}{kT} \right] \cong \mu'_0 \exp\left[- \frac{W_H}{kT} \right] \qquad (2.11)$$

where ω_0 is a characteristic optical phonon frequency, E_A or W_H the polaron hopping energy, μ_0 and μ'_0 are constants, and the other symbols have their usual meanings.

From Eq. 2.11, it is noted that the drift mobility is an exponential function of inverse temperature, and this is the main signature of small polaron hopping transport. (See Fig. 21)

In summary, the possible current types and transport modes pertinent to ferroelectric ceramics have been reviewed. The fundamental difference between the classical band transport (grain boundary barrier transmission) and small polaron hopping (quantum-mechanical tunnelling) lies in the fact that the carrier mobility is much less in the latter than in the former, and it is an exponentially increasing function of temperature in the latter, whereas it is normally a decreasing function of temperature in the former because of increasing lattice thermal energy.

Chapter 3. Review of Grain Boundaries in Electronic Ceramics

The presence of grain boundaries is considered to be the main cause for the resistivity anomaly above the Curie temperature of semiconducting $BaTiO_3$ ceramics, since this phenomenon is normally negligible in single crystal $BaTiO_3$ of the same composition.[36]

Hence, grain boundaries are very important in characterizing and analyzing the properties of ceramics. In this chapter, some of the known grain boundary theories, which are pertinent to the $BaTiO_3$ ceramics in an analysis of their electrical properties, will be reviewed.

3.1 The Grain Boundary Barrier Layer Models in Semiconducting Barium Titanate Thermistors

Since a large positive temperature coefficient of resistivity (PTCR) in semiconducting $BaTiO_3$ above the Curie temperature (120°C) was first reported by Haayman et al.[37] in 1955, there have been many experimental and theoretical approaches[2,36,38-54] explaining the mechanism of this resistivity anomaly.

Of those proposed models, Heywang's grain boundary barrier layer model[38,39] based on the Schottky approximation, is a widely accepted one, along with the modification by Jonker.[40]

In the following sections, the Heywang model will be reviewed, together with other proposed models.

3.1.1 The Original Heywang Model

In his original grain boundary barrier model,[38,39] Heywang explained the resistivity anomaly present in properly donor-doped $BaTiO_3$ in terms of the increasing barrier height above the Curie temperature. The decrease of the dielectric constant with temperature above the Curie temperature is responsible for the increase of the barrier height, and in a first approximation, the dielectric constant is generally assumed to be given by the Curie-Weiss law

$$\varepsilon_r = \frac{C}{T - T_0} \qquad (3.1)$$

where ε_r is the relative dielectric constant, C proportionality constant ($\sim 1.2 \times 10^5$), T_0 the extrapolated Curie point of $BaTiO_3$ ($\sim 383°K$), and T the absolute temperature. In Fig. 5, the Heywang model is shown schematically as a boundary between two n-type semiconducting grains with a number of grain boundary states in which conduction electrons can be trapped. The equilibrium potential barrier height can be obtained by integrating Poisson's equation for an electron ($\nabla^2 \varphi = \rho / \varepsilon$; ρ = the net space charge density) twice within the depletion layer. The resulting barrier height is given by

$$\varphi_0 = \frac{q^2 N_d}{2 \varepsilon_r \varepsilon_0} W^2 \qquad (3.2)$$

where q is the elementary charge, N_d the uniform donor density in the grain, W the thickness of depletion region or space charge width, ε_r the relative dielectric constant, and ε_0 the absolute permittivity of vacuum. If a number of electrons are trapped in the grain boundary states, depletion

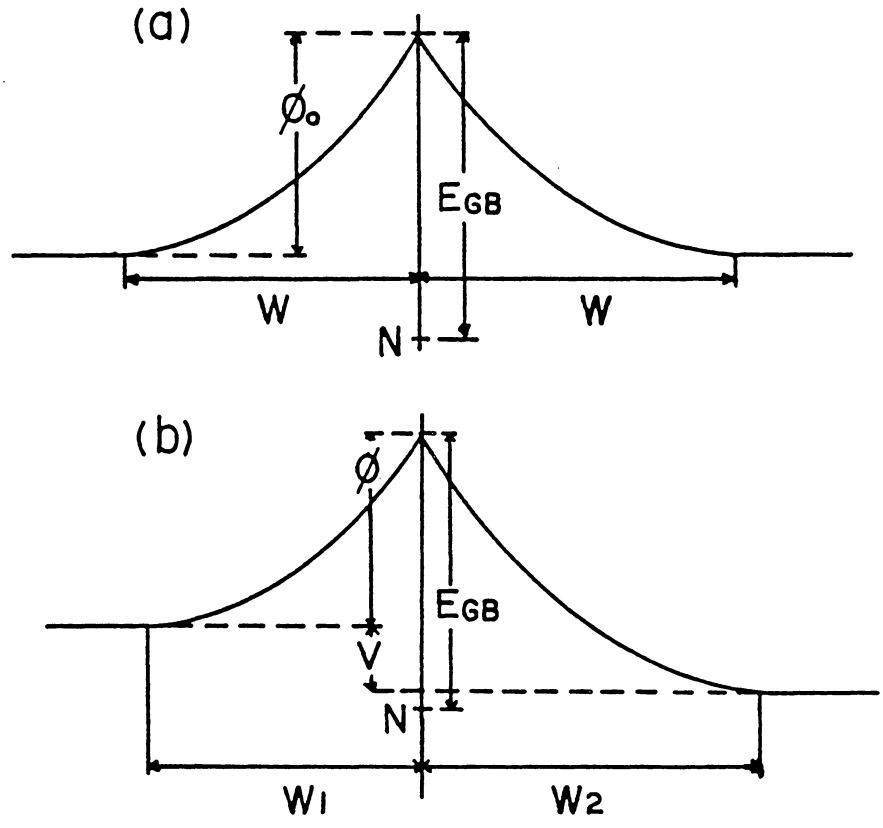

Figure 5. Band diagram of Heywang's grain boundary barrier model [38-40]

(a) and (b) : without and with voltage bias

φ, φ_o : grain boundary barrier height

N : the available grain boundary state density

E_{GB} : the grain boundary state energy below the conduction band edge

W, W_1, and W_2 : the space charge widths
($W_1 + W_2 = 2W$)

V : the voltage drop between two grains

layers with an effective thickness W will be developed on both sides of the barrier.[40] From the charge neutrality condition in the depletion region, assuming all of the acceptor levels are at the same energy E_{GB} [38-40] and the complete ionization of donor impurities,[45,46] the space charge width W can be expressed by [39]

$$W = \frac{Q_{GB}}{2qN_d} = \frac{N_{GB}}{2N_d} = \frac{1}{2N_d} \frac{N}{\exp\left[(\varphi_0 - E_{GB} - E_f)/kT\right] + 1} \qquad (3.3)$$

where Q_{GB} is the grain boundary charge, N_{GB} the occupied grain boundary state density, N the available grain boundary state density, E_{GB} the grain boundary state energy below the conduction band, E_f the Fermi energy, and k the Boltzmann constant. In Eq. 3.3, N_{GB} is temperature-dependent and given by the Fermi-Dirac distribution. Also, E_f is assumed to be independent of the grain boundary states and is given by the bulk (grain) properties.[48]

The Fermi energy level E_f is given for n-type semiconductors with fully ionized donors as:

$$E_c - E_f = kT \ln\frac{N_c}{n} = kT \ln\frac{N_c}{N_d}$$

or, setting E_c equal to zero as an energy reference,

$$E_f = kT \ln\frac{N_d}{N_c} \qquad (3.4)$$

where N_c is the density of states in the conduction band, and n the electron concentration in the grain.

Substituting Eq. 3.3 into Eq. 3.2, one obtains

$$\varphi_0 = \frac{q^2 N_{GB}^2}{8\varepsilon_r \varepsilon_0 N_d} \qquad (3.5)$$

From the above equation, it is clear that the potential barrier height is dependent on the grain boundary charge ($q N_{GB}$), the donor density in the grain, and the relative dielectric constant.[45] The resistivity ρ is assumed to vary exponentially with grain boundary barrier height:

$$\rho = \rho_0 \exp\left[\frac{\varphi_0}{kT}\right] \qquad (3.6)$$

where ρ_0 is a constant which includes the resistivity of the grain.

Heywang was able to explain qualitatively that resistivity increases of up to 4 orders of magnitude are due to the increase of grain boundary barrier height φ_0 above the Curie temperature, accompanied by the decrease of the relative dielectric constant ε_r .

However, in order to explain the low resistivity regime below the Curie temperature, a high-field dielectric constant ε_{eff} was assumed, as shown in Fig. 6. [39]

3.1.2 The Modified Heywang Model

Jonker pointed out that the value of 10,000 for a high-field dielectric constant assumed by Heywang below the Curie temperature is still not high enough to depress the barrier height φ_0 to a negligible value. [40] Considering the ferroelectric property of $BaTiO_3$ as the main cause of the disappearance of the barrier, he proposed that the domain pattern below the Curie temperature is built up in such a way that the grain boundary charge is compensated by the charge formation arising from the differences in the normal component of the polarization on both sides of the boundary. (Fig. 7)

In addition, Miller [41] tried to modify two of Heywang's assumptions, which were the uniform donor concentration in the depletion region and the single (discrete) grain boundary state energy. He found that the exact form of the donor profile is not critical in eliminating the discrepancy between the model and the experiment.

Kulwicki and Purdes [42] posed a question of applicability of Poisson's equation on which the Heywang model is based. According to them, Poisson's equation is not strictly applicable to

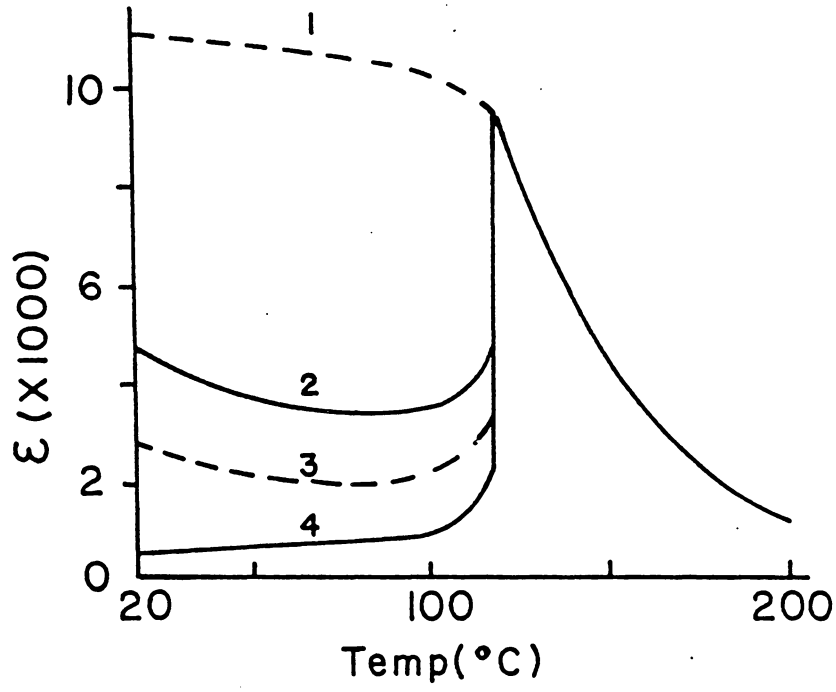

Figure 6. Dielectric constant of undoped $BaTiO_3$ [38,39]

1 (ε_{eff}) : the effective dielectric constant for large fields (e.g. 3 kV/cm)

3 ($\bar{\varepsilon}$) : the average dielectric constant for small fields (< 10 v/cm)

2, 4 (ε_c, ε_a) : dielectric constants measured perpendicular and parallel to the direction of the permanent polarization

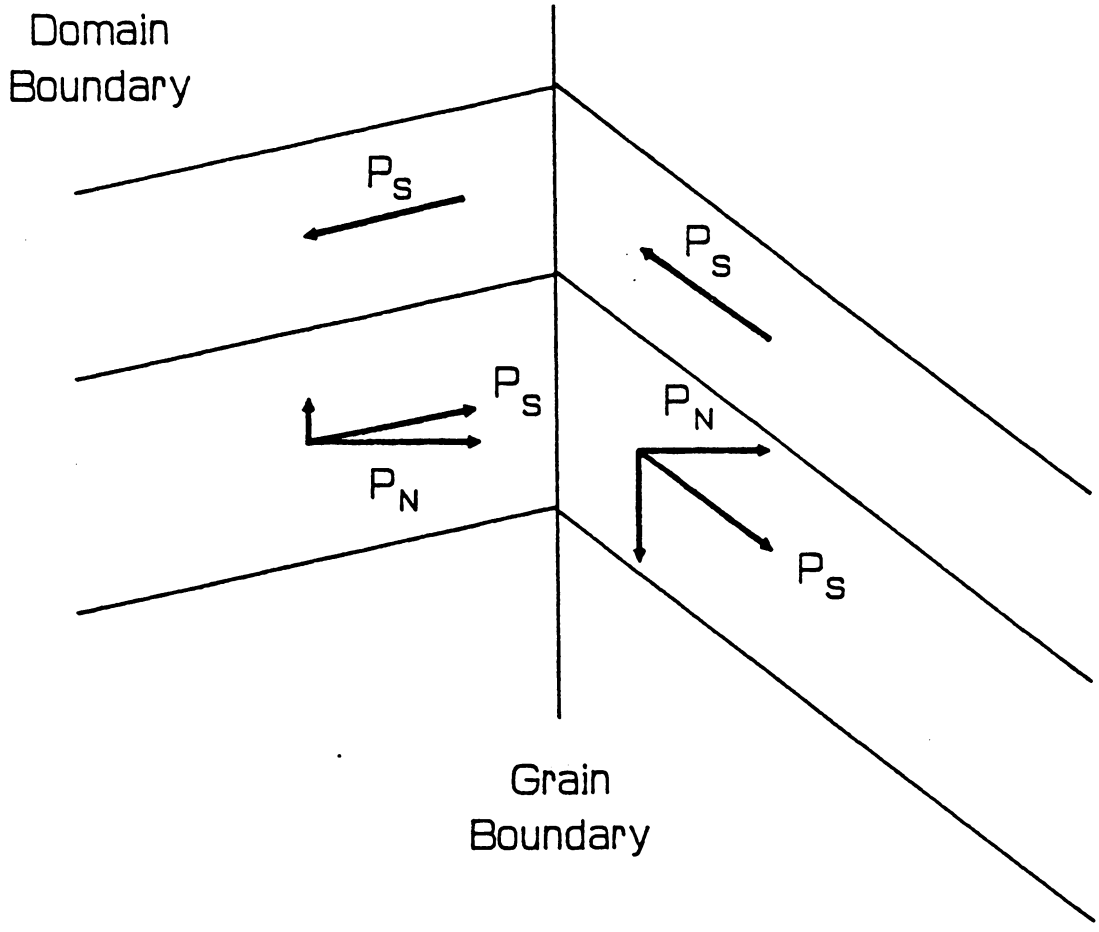

Figure 7. Ferroelectric domains at a boundary between two crystallites of different orientation, with compensating surface charges [40,43]

P_S : the spontaneous polarization

P_N : the normal component of the spontaneous polarization to the grain boundary

ferroelectric materials. They, then, derived an effective grain boundary state density N_{eff} below the Curie temperature, which is different from the occupied grain boundary state density by the relation

$$q N_{eff} = q N_{GB} - 2 P_S \cos \theta \qquad (3.7)$$

where $q N_{eff}$ is the total positive charge present in the depletion region, and $P_S \cos \theta$ is the normal component of the polarization. Unlike N_{GB}, N_{eff} can have negative values, and depending on the sign of N_{eff}, the depletion layer may or may not be formed. In the ferroelectric region below the Curie temperature, the depletion layer width W is given by $W = N_{eff} / 2 N_d$. Their theory accounts for the existence of a resistivity minimum at about 80°C, the increasing negative temperature coefficient (NTC) effect with increasing resistivity below the Curie temperature, and the reduced PTC effect with decreasing resistivity above the Curie temperature. However, it does not explain the resistivity jump at the Curie temperature. In the paraelectric region above the Curie temperature, Jonker's modified Heywang model[38-40] is considered to be more accurate.

Ihrig and Puschert[48] improved the Heywang model by assuming a distribution of grain boundary acceptor energy levels due to distortions in the interface region as a consequence of the lattice mismatch. They found a satisfactory agreement between the measured and calculated curves by doing so. The suggestion of an energetic distribution of acceptor levels is reasonable, because each acceptor may find a different environment.

While Ihrig and Puschert assumed barium vacancies as acceptor states (based on Daniels and Wernicke's defect chemistry study in $BaTiO_3$ [2]), Kuwabara[51] recently showed that the nature of acceptor states is not barium vacancies, but chemisorbed oxygen near the grain boundaries. However, they all concluded, overall, that the PTCR effect can be described almost completely by the Heywang model. The possibility of second glassy phase at the grain boundary has not been identified yet by experiments.[51]

The suggestion[49] that the negative grain boundary charge is compensated by a proper orientation of the spontaneous polarization below the Curie temperature requires further modifications since, even with an optimum alignment of the spontaneous polarization, a part of the negative grain boundary charge is uncompensated.[48] The residual barrier thus produced is believed to be re-

sponsible for a rather high resistance of PTC thermistors at room temperature.[49,53] Hence, the resistivity below the Curie temperature is still governed by the grain boundary potential barrier, and this residual barrier was identified by cathodoluminescence, where the grain boundaries appeared dark. [55]

Among other PTC models, those proposed by Gerthsen and Hoffmann, [53,54] and Daniels and Wernicke[2] should be noted. Gerthsen and Hoffmann proposed an extended grain boundary model, where a high resistivity intermediate layer was added between n-type grains. This model can explain not only the usual PTC characteristics, but also the observed non-linear current-voltage characteristics. Their model is different from n-p-n grain boundary barrier model proposed by Brauer,[56] which fails to explain the observed capacitance-voltage characteristics. Furthermore, based on the defect chemistry results in $BaTiO_3$ reported by Daniels,[57] a change from n-type to p-type conduction is not feasible at room temperature.[43] Hoffmann's extended grain boundary model, however, was found unnecessary by Ihrig and Puschert.[48] On the other hand, Daniels and Wernicke proposed the modified model with intrinsic grain boundary barrier layers, where the complete compensation between donors and acceptors would occur. According to this theory, the PTC maximum tended to occur at a very high temperature, and the subsequent decrease in resistivity would not be detected by experiments. Hence, this model may not be acceptable.[43]

3.2 The Models of Barrier Layer Capacitors

Barrier layer capacitors are characterized by electric energy storage, mainly by means of space charge polarization at interfaces between grains and/or between electrode and dielectric, whereas most multilayer ceramic capacitors are characterized by means of electronic, ionic and orientation polarization.[9]

There are two types of barriers which can act as blocking layers for the current flow; surface barriers and grain boundary barriers. The surface barriers are usually made by non-ohmic contact

at the surface. Since reduced or doped semiconducting $BaTiO_3$ is almost always n-type, the noble metals which have high work functions can be used to make rectifying contact. The capacitors, which utilize only the surface barrier, usually show too small a breakdown voltage to be useful for commercial applications. However, the grain boundary barrier layer (GBBL) capacitors can be made to have a much higher breakdown field (of about 10 kV/cm) by achieving high acceptor concentration.[58] Since the grain boundary barrier layer has a major influence on the barrier layer capacitor properties, it is worth while to review some of the models dealing with its characteristics.

Like PTC thermistors, the grains in GBBL capacitors are doped with aliovalent impurities and are thus semiconducting. But, in order to increase its insulation resistance, a high acceptor concentration is desired, whereas a low acceptor concentration is used in PTC thermistors.[58] Hence, the only difference between PTC thermistors and $BaTiO_3$-based GBBL capacitors is the amount of p-type acceptor impurities such as copper and manganese. In other words, PTC thermistors and GBBL capacitors can be considered to have the same phenomenological origin.[59] Therefore, the GBBL models are based on the Heywang model of PTC thermistors previously discussed in section 3.1. (Fig. 5) When the acceptor dopant concentration is high enough to give a thick grain boundary region, the width of which is greater than the charge carriers' mean free path, the GBBL capacitor behavior is observed.[59]

The above model originally proposed by Heywang[58] and Brauer[38] corresponds to an n-p-n junction where the p-region is thick enough to become an insulating material. This model was further developed by Wernicke[60] who demonstrates insulating grain boundaries rather than the p-type grain boundary layer.

Those models discussed so far are based on $BaTiO_3$-based ceramics, whereas the majority of GBBL capacitors in recent years are based on $SrTiO_3$. The advantages of $SrTiO_3$-based ceramics over $BaTiO_3$-based ones in GBBL capacitor applications are obvious. Since $SrTiO_3$ is non-ferroelectric, the capacitance value does not age, is not voltage dependent, nor highly temperature dependent, and the dissipation factor is low.[9] Also, due to higher conductivity of the grain, $SrTiO_3$-based GBBL capacitors can be used as high as 1 GHz in frequency.[9]

Recently, Park and Payne[61] proposed the n-c-i-c-n barrier model, which is similar to the n-i-n model, for $SrTiO_3$-based internal barrier layer capacitors, where c represents the compensated layer within the grain, and i the insulating boundary. This model is similar to the Heywang model with the exception that an insulating layer is included within the depletion region. The two-layer model proposed by Wernicke,[62] which was originally proposed by R. M. Glaister in 1961,[63] is shown schematically in Fig. 8 along with an equivalent circuit. According to this figure, a complete grain boundary structure is composed of two different types of layers; the intergranular layer, which is usually formed during second firing and has a different composition from that of the grains, and a barrier layer, which is formed by the diffusion of impurities into the grain, and has nearly the same composition as the grain interior. This model accounts for the most of the observed barrier layer capacitor characteristics.

3.3 The Models of ZnO-Based Varistors

ZnO has the crystal structure similar to that of wurtzite (hexagonal ZnS), and when it is doped with a small amount of impurities such as Bi and Mn, it shows very high nonlinear current-voltage characteristics, which can be expressed as[64-67]

$$I = C V^{\beta} \tag{3.8}$$

or

$$\frac{I_1}{I_2} = \left[\frac{V_1}{V_2}\right]^{\beta} \tag{3.9}$$

where C is a constant, and the nonlinear exponent β is defined by the relation[66]

$$\beta = \frac{dI/I}{dV/V} = \frac{d \ln I}{d \ln V} \tag{3.10}$$

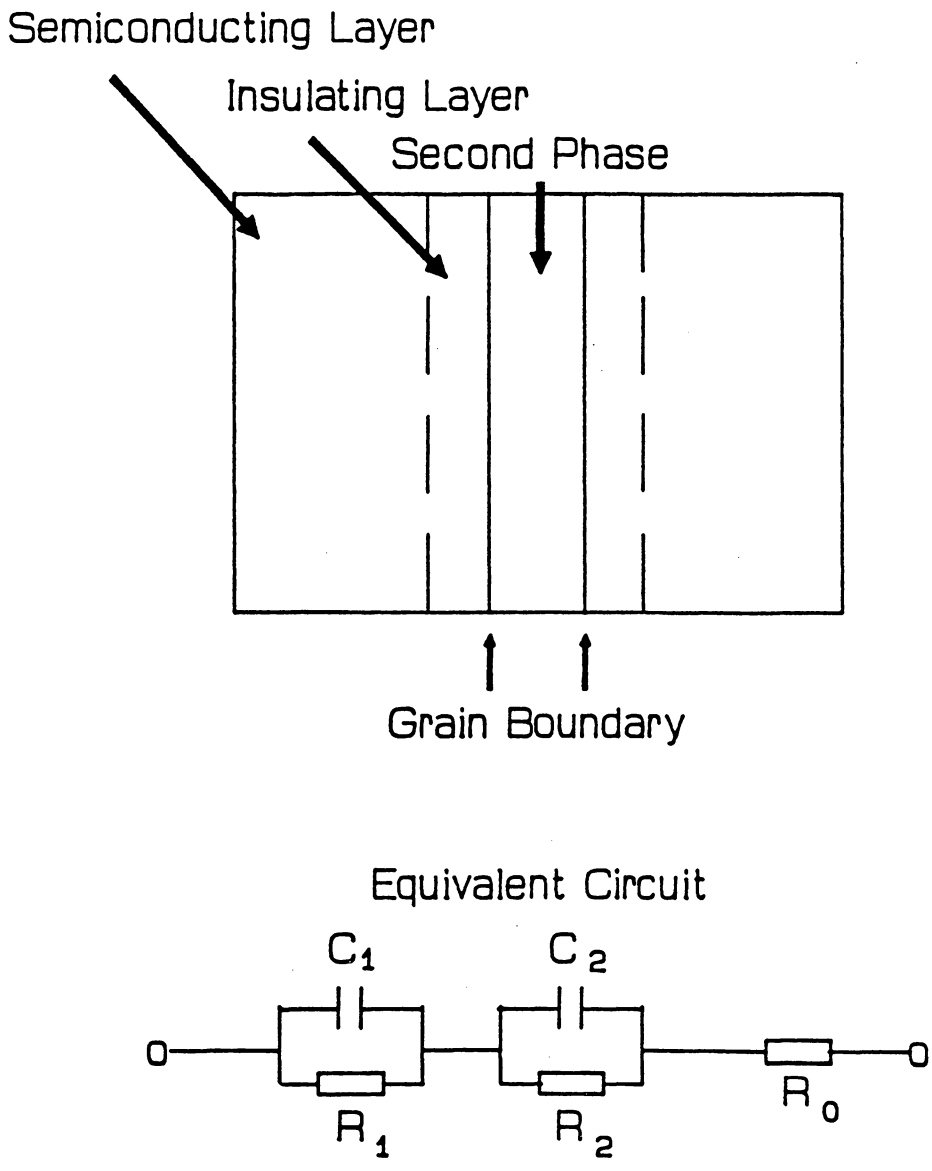

Figure 8. Microstructural two-layer model of $SrTiO_3$-based GBBL capacitors with an equivalent circuit representation [62,63]

It is noted that β is voltage dependent, and has a value in excess of 50 in the breakdown region.

Several conduction mechanisms have been proposed to explain the breakdown phenomena of varistor current-voltage curves: the mechanisms of avalanche breakdown, space-charge-limited currents (SCLC), thermal activation over a potential barrier, and tunneling. However, none can satisfactorily account for all of the general features of the observed varistor current-voltage characteristics, according to Mahan et al.[65] They proposed a hole creation model, in the breakdown region, where the holes are created on the forward side of the junction as the conduction band drops below the top of the valence band. Therefore, electron tunneling through an effectively thinned barrier layer results in the observed highly nonlinear current-voltage curves in the breakdown region. A certain threshold voltage is needed for the onset of the breakdown region, below which the ohmic region exists.

The microstructure of the ZnO varistor is essentially the same as that of the barrier layer capacitor, and hence the equivalent circuit of ZnO varistor can be represented as the one shown in Fig. 8.[68]

Typical current-voltage curves for a commercial ZnO varistor and a barrier layer capacitor are shown in Fig. 9 and Fig. 10, respectively.[69] Both figures show ohmic current region below about 10 volts, followed by exponential increase of current in super-ohmic region. This behavior is accompanied by a strong decrease in the activation energy. Both current increase and activation energy decrease have been attributed to a voltage dependent grain boundary barrier height.[65,69]

In summary, the possible grain boundary phenomena in electronic ceramics have been reviewed with an emphasis on semiconducting ceramics. Some of these theories may be pertinent in the case of high resistivity, high dielectric constant capacitor ceramics. Further clarification of this point will be attempted in the next two chapters, for the case of Corning® X7R-type capacitor ceramics.

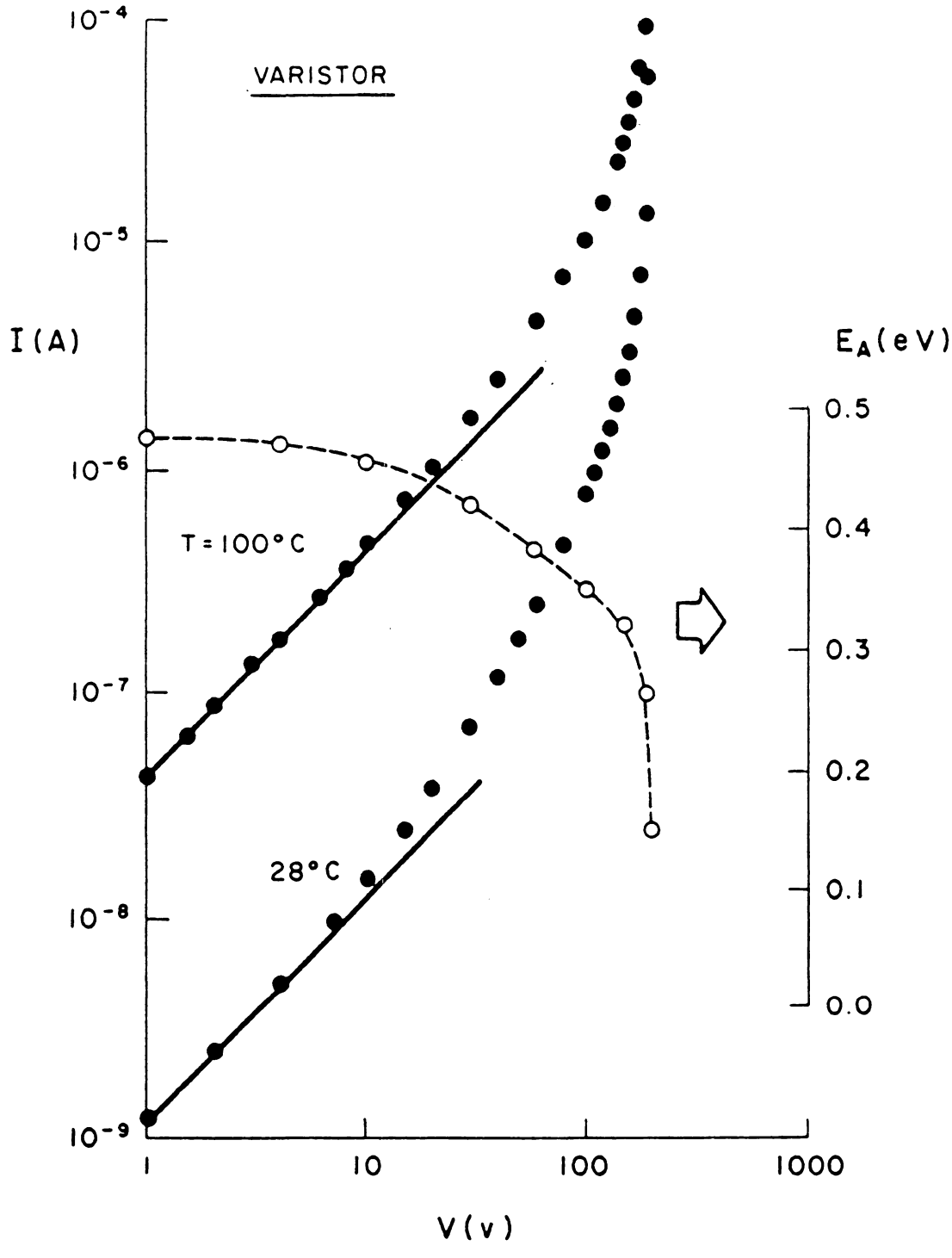

Figure 9. Current and activation energy versus voltage for a commercial ZnO varistor [69]

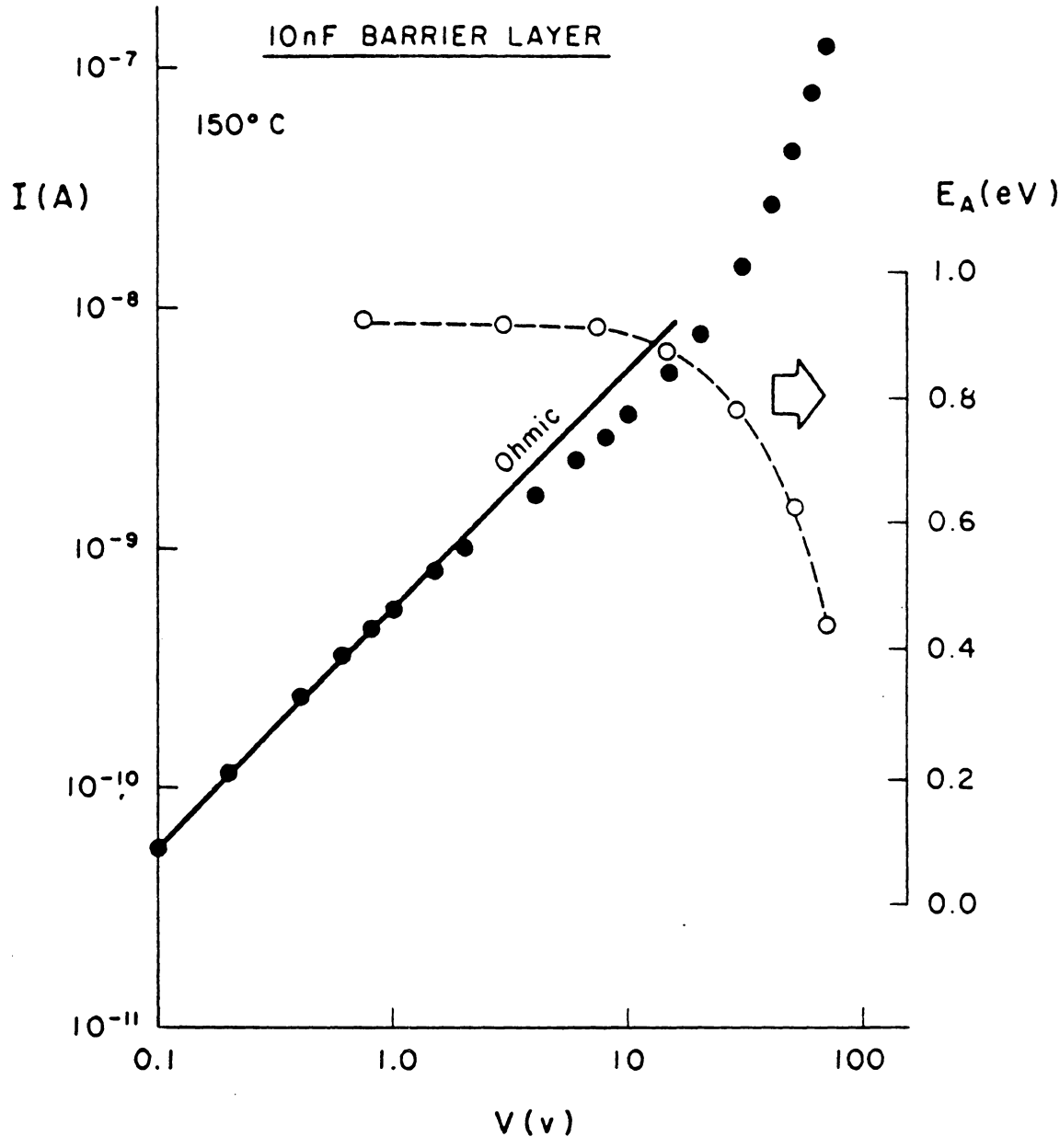

Figure 10. Current and activation energy versus voltage for a commercial barrier layer capacitor [69]

Chapter 4. Experimental Techniques

In order to identify the type of dominant charge carrier in $BaTiO_3$-based X7R type samples, both thermoelectric and ionic transference number measurements have been used. The former technique was used to determine the sign of charge carrier, and when it was combined with electrical conductivity data, one could determine the dominant charge carrier concentration and its drift mobility. The latter technique was used to determine whether the dominant charge carrier is ionic or electronic in nature. Hence, from the results obtained by these measurements, one could conclusively identify the dominant charge carrier species.

Once the dominant charge carrier was identified, its possible mode of transport was examined by current-voltage and current-temperature (activation energy) measurements, since the mode of transport is often characterized by a conductivity activation energy E_A. Also, the current-voltage measurements can be used to determine the source of charge carrier along with its current type. Complex impedance measurements were used to separate grain boundary and contact resistance from total resistance value, since this technique is the only possible technique to measure grain boundary resistance directly in high resistivity ceramics with small grain size ($\cong$ 1 μm). This can also aid in determining the possible transport mechanism, by examining the role of grain boundary in the material.

In the following, these measurement techniques and sample preparation procedures are described in detail.

4.1 Sample Preparation

Two sets of samples, indicated in Table 2, were used throughout the research period. The first set is composed of $BaTiO_3$-based X7R multilayer ceramic (MLC) capacitors and capacitor ceramics, and were supplied by Corning Electronics in Raleigh, North Carolina. The nominal chip dimensions of ceramic blanks are 0.621cm × 0.530cm × 0.218cm, and the broader faces of this "new" or as-received samples were painted or printed with Au-Pt ink,† followed by firing at 850°C for 10 minutes for electrical measurements.‡ In order to prepare semiconducting ceramics, these new X7R blanks were reduced to various degrees in forming gas, which contains 10% hydrogen and 90% nitrogen in volume. The reduction temperatures used were 900, and 1000°C, and the soaking time was 5 hours except for one sample lot which was heated for 44 hours in forming gas at 1000°C to produce heavily reduced samples. Lower reduction temperatures were also tried, but yielded very slow reduction rate and nonhomogeneous reduction due to lower values of oxygen diffusion coefficient at these temperatures. The test specimens from each reduction lot were cross-sectioned to optically check for reduction uniformity. Almost always, darker layers were found along the edges of the sample.[10] (These layers were identified by an optical microscope.) Hence, this outer layer of about 0.5 mm in thickness of each sample was removed by grinding and polishing to obtain

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† Engelhard No. A-3395. Electrode printing was done by Presco® model 435 screen printer using 325 mesh screen.

‡ Thermolyne® type 21100 tube furnace was used for electrode firing.

Table 2. Specimens used for the electrical measurements

	Sample	Thickness	Dimensions
First Set	100nF X7R MLC Capacitor [1]	~ 1.5 mil	
	X7R Blank [1]	~ 2.30 mm	~ 6.2 mm × 5.3 mm
	X7R Plate [1]	~ 1.12 mm	~ 1.0 cm × 1.0 cm
Second Set	$Ba_{0.99}TiO_{3-x}$ Disc [2]	~ 0.72 mm	~ 1.1 cm (diameter)
	$Ba_{1.01}TiO_{3+x}$ Disc [2]	~ 0.73 mm	~ 1.1 cm (diameter)
	$BaTiO_3$ Disc [3]	~ 0.85 mm	~ 1.1 cm (diameter)

[1] supplied by Corning Electronics, Raleigh, NC.

[2] supplied by Materials Research Laboratory, Penn State University,University Park, PA.

[3] supplied by Materials Research Center, Lehigh University, Bethlehem, PA.

$Ba_{0.99}TiO_{3-x}$ discs were sintered at 1325 °C for 2 hours. (95.6 percent TD)

$Ba_{1.01}TiO_{3+x}$ discs were sintered at 1375 °C for 2 hours. (94.1 percent TD)

$BaTiO_3$ discs were sintered at 1325 °C for 16 hours.

X7R samples were sintered at 1260 °C.

homogeneous samples. A low curing temperature silver epoxy† was applied to these hydrogen reduced specimens for electrical contact.

The specimens for current-voltage and complex impedance measurements were prepared from the "new" X7R blanks (i.e. unreduced) by polishing from one side so that samples with different thicknesses were obtained.

Electrode-ceramic interfaces were inspected using an optical microscope. Typical polishing procedures are as follows:[10]

1) A specimen was mounted onto a steel cylinder using epoxy. This specimen holding apparatus was used to obtain uniform polishing, i.e. to produce a specimen with uniform thickness. (For optical test specimens, Struers epoxy was used for the mounting material.) These epoxies were cured at room temperature.

2) Either rough grinding was performed on a rotary grinding wheel using 180 mesh grit sand paper, or hand grinding on various mesh grit papers of increasing order was used to reach the approximate depth desired.

3) Polishing was accomplished in two stages: rough polishing on a Buehler microcloth, using a slurry of 1 micron alumina, and fine polishing on a similar microcloth, using a slurry of 0.05 micron alumina.

The second set of samples includes "pure" $BaTiO_3$ ceramics whose compositions and processing conditions are known, whereas the first set is $BaTiO_3$-based commercial capacitor ceramics so that the exact compositions along with the processing conditions are proprietary. This second set in-

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† epo-tek® H20E, Epoxy Technology Inc., Billerica, MA. Curing schedule of 90°C for 90 minutes was used.

cludes undoped ("stoichiometric") and non-stoichiometric $BaTiO_3$. The latter includes both Ba-rich and Ba-deficient compositions.† (See Table 2)

Samples are of disc type with diameter of about 1.1 cm and thickness of 0.75 mm. These samples were mainly used to support our data obtained for the first set of samples. Non-stoichiometric barium titanates had been painted with Pt electrode paste, and were fired at 1000 °C for 8 hours. Undoped barium titanate disc was printed with Au-Pt ink, and fired at 850 °C for 10 minutes prior to electrical measurements.

4.2 Thermoelectric Measurements

As mentioned in section 2.1, the thermal activation energy for electrical conduction can be divided into the carrier concentration and mobility activation energies, i.e.

$$E_A = E_{A,n} + E_{A,\mu} \tag{4.1}$$

where all of the parameters were previously defined.

In an effort to determine these parameters for ceramic similar to that in MLC devices, thermoelectric measurements were made on chips of X7R ceramic fabricated similarly to MLC capacitors, but without the internal electrodes. (X7R "blank" or "plate")

A schematic of the experimental apparatus is shown in Fig. 11. The ceramic chip (6.21 mm × 5.30 mm × 2.18 mm) is mounted on a copper block using silver epoxy as an electrically conducting adhesive and electrode material. The thermocouples to measure the top and bottom temperatures of the chip, and the voltage leads, are also attached using silver epoxy. The sample is

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† These samples were provided by Materials Research Lab. of Penn State University and by Materials Research Center of Lehigh University. Actually undoped $BaTiO_3$ contains traces of impurities which are contained in the raw materials, and hence it may not be exactly stoichiometric.

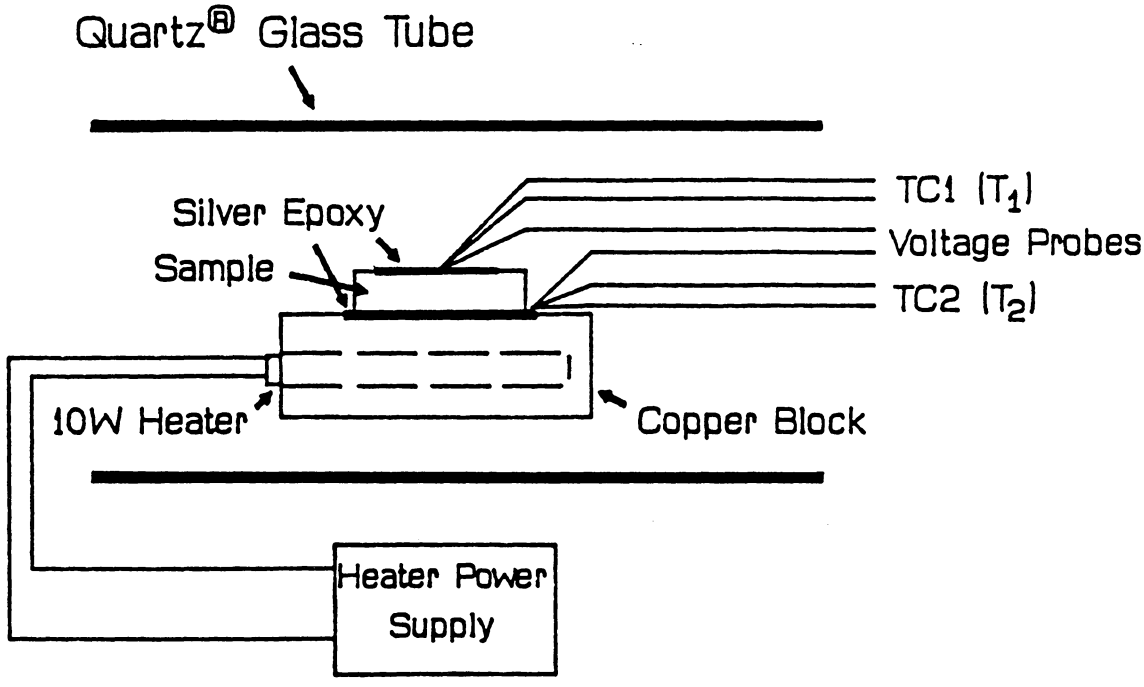

Figure 11. Thermoelectric measurements apparatus

placed in a temperature controlled tube furnace,† and a temperature difference ΔT is established by a 10 watt heater located inside the copper block. Both "hot" end (T_2) and "cold" end (T_1) temperatures were monitored by 0.1 °C resolution copper-constantan thermocouple digital temperature readout.‡ The output voltage ΔV is measured by a high input impedance electrometer.§ The input impedance of the electrometer ($10^{14}\ \Omega$) is at least 100 times higher than the chip resistance as measured between the voltage probes. If this condition is not satisfied, the measurement circuit will load the crystal, and ΔV will be reduced from its true value. For this reason, as-received X7R chips (blanks) needed to be heated above room temperature. The samples used in this study include as-received X7R capacitor ceramic chips (with no electrodes) as well as reduced X7R chips. In order to vary the relative amount of reduction, both annealing temperature and time were varied. (as mentioned earlier)

4.3 Electrical Resistivity and I - V Measurements

Both current-voltage and current-temperature measurements were made on a number of X7R blanks and $BaTiO_3$ using a three-electrode guard ring geometry.[70] (Fig. 12) Since the ultimate goal of this research effort is related to the current transport mechanisms of high resistance, high dielectric constant capacitors and ceramics, most of the electrical measurements were done for non-reduced samples. To compare the results obtained for non-electroded X7R chips with those for MLC capacitors, additional measurements on electroded Corning 100nF X7R MLC capacitor chips were made.

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† Lindberg (Type 54231) 1200 °C maximum temperature tube furnace with control console (Type 59344)

‡ Digicator ® Model 410B, Omega Engineering Inc., Stamford, CT.

§ Model 610C, Keithley Instruments Inc.

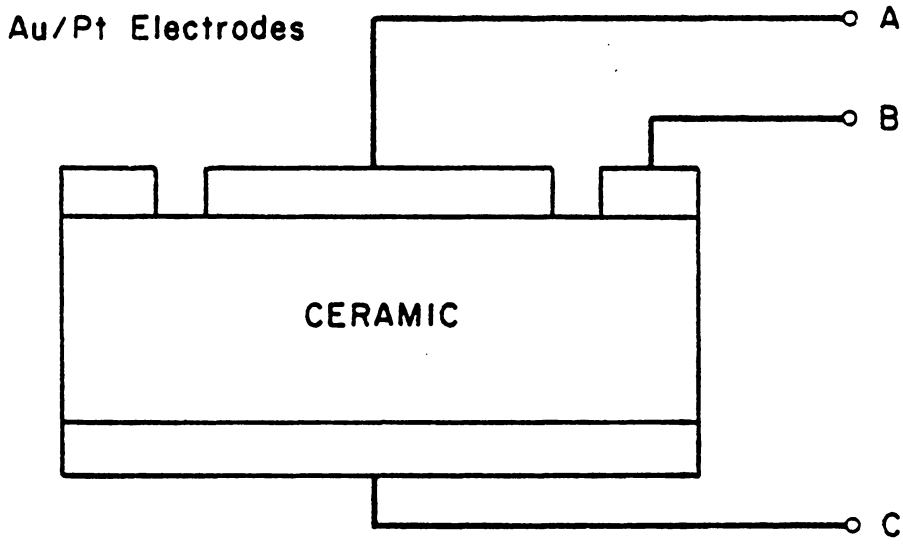

Figure 12. Three-electrode guard ring configuration

A : guarded electrode

B : guard electrode

C : unguarded electrode

For non-electroded X7R chips of varying thicknesses, I - V measurements were made from 10 to 1000 volts at 200 to 350°C, in both argon and air ambients. Au-Pt electrodes were fired onto the broad faces of samples at 850°C prior to electrical measurements. The lead wires inside the tube furnace were Teflon®-coated, and attached to the electrodes by means of silver epoxy. A copper-constantan thermocouple is directly attached to the cathode to measure the temperature of the sample.

For the resistivity measurements of similar X7R plates which were sintered at 1260°C with larger dimensions (1cm × 1cm × 0.12cm), the galvanic cell setup, which will be described in the next section, was used. To carry out the measurements at temperatures to 850°C, bare platinum lead wires were used.

In addition, thermal activation energies for electrical conduction were estimated from the slope of $\ln I$ versus $1/T$ plots.

4.4 Ionic Transference Number Measurements

The true test of ionic motion in a solid is mass transfer. If there is considerable movement of oxygen and oxygen vacancies in $BaTiO_3$-based ceramics, it should be detectable in a galvanic cell setup. The schematic of the setup is shown in Fig. 13, which is similar to the one used by Mitoff.[71]

Two quartz® (or vycor®) glass tubes were mounted vertically in a tube furnace (Thermolyne Type 21100). In most cases, vycor® glass tubes were used, as the maximum measuring temperature in this study was limited below 900 °C. Quartz® glass has a maximum operating temperature of about 1200 °C, and is more expensive than vycor®. (Maximum operating temperature of vycor® is about 950 °C.)

The transference number measurements utilize the electric potentials developed across the specimen when it is placed in the setup shown, with different oxygen partial pressures on the two sample faces.[26,72,73]

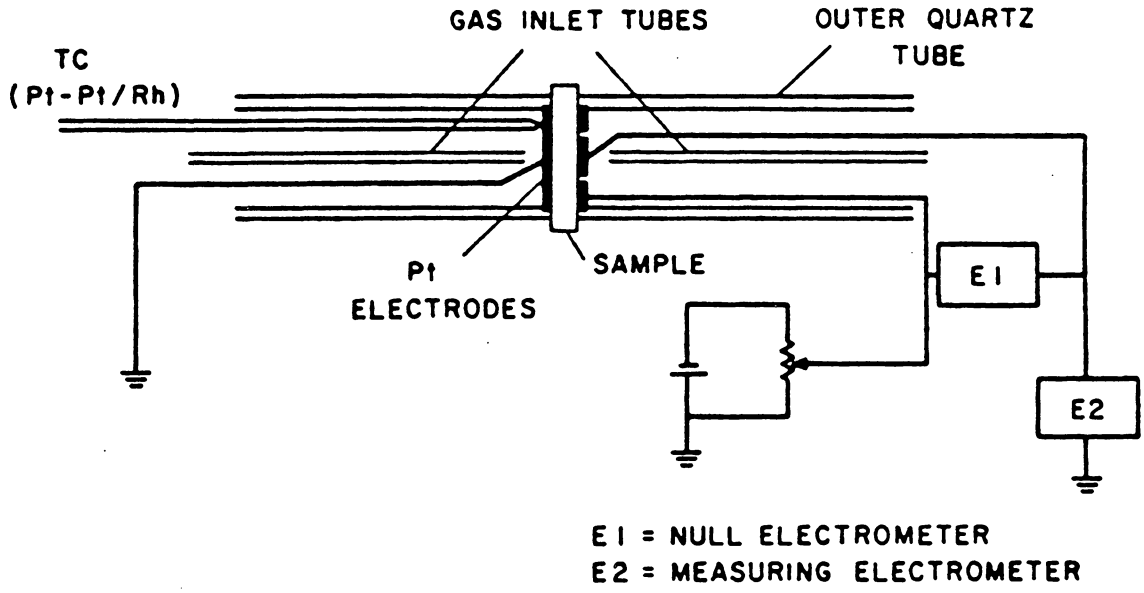

Figure 13. Schematic of galvanic cell setup, for transference number measurements

$$\text{porous Pt}, \ O_2(P_1) \left| \begin{matrix} BaTiO_3 \\ \text{ceramic} \end{matrix} \right| O_2(P_2), \ \text{porous Pt} \qquad (4.2)$$

Measured electrical potential V is due to an oxygen concentration gradient across a specimen and can be expressed by

$$V = t_i V_i \qquad (4.3)$$

where t_i is the ionic transference number, and V_i is the electrical potential for a pure ionic conductor, which is given by the relation[26,71]

$$V_i = \frac{RT}{4F} \ln \left[\frac{P''_{O_2}}{P'_{O_2}} \right] \qquad (4.4)$$

where R is the gas constant (8.314 J/mol-K), F the Faraday constant (96487 J/mol-volt), and T the absolute temperature.

Different oxygen partial pressures were produced using argon as a diluting gas at a flow rate of 100 or 200 cc per minute, and the minimum oxygen partial pressure obtained was 5×10^{-3} atm. When measurements were made, the potential of the guard electrode was set equal to that of the guarded electrode using a potentiometer, so that current flow between them was prevented.[71,74] (Fig. 13)

For $BaTiO_3$-based X7R ceramics, the electrical potentials were measured in the range of 400 to 850°C, and Y_2O_3-stabilized (9.4 mol %) ZrO_2 single crystal† was used as a standard pure ionic conductor, to check the results obtained for $BaTiO_3$.

Electrodes of Au-Pt ink (Engelhard No. A-3395) and Pt ink (Engelhard No. 6926, unfluxed) were screen printed using standard electrode printing procedure with 325 mesh screen and fired at 850°C and 1000°C, respectively.

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† Manufactured by CERES Corp., North Billerica, MA.

The samples measured include $BaTiO_3$-based X7R capacitor ceramics and both stoichiometric and non-stoichiometric $BaTiO_3$ ceramics.

4.5 Complex Impedance Measurements

Since the impedance (or admittance) measurement technique was first introduced by Bauerle,[75] the method has been widely used on semiconducting or semi-insulating ceramics such as PTC thermistors and ZnO varistors, and on ionic conductors such as Al_2O_3, MgO, and ZrO_2 oxygen sensor to probe contact, grain or grain boundary contributions to the total impedance.[76,77] These materials are either grain boundary controlled or single crystalline, so that one or more of the above contributions can be ruled out. This technique could be a very powerful tool in determining the relative contributions to the total impedance, and hence in identifying grain boundary impedance, in high resistance, high dielectric constant capacitors and ceramics.[28,78-80]

The method is based on the fact that an R-C lumped circuit produces a semicircle in the negative half of the complex impedance plane, as illustrated in Fig. 14. This can be extended to two or more R-C sections (Fig. 15), with a distinct semicircle appearing for each R-C section if the RC time constants (relaxation times) are very much different. If the semicircles are distinct, resistance values are determined from Z' intercepts, and capacitance values from the condition $\omega RC = 1$ at the semicircle minima, where ω is the angular frequency. However, this relation only applies when the center of a semicircle lies on the Z' axis, and should be used with a caution in real impedance plots.

Such complex impedance measurements were performed on as-received X7R plates and blanks, and $BaTiO_3$ ceramics. In order to separate semicircles into each contribution from grain, grain boundary and contact, voltage-biased techniques have been used along with samples with different thicknesses obtained by polishing mentioned before.[81] DC voltage-biased impedance measurements deserve some explanation, and will be described further below.

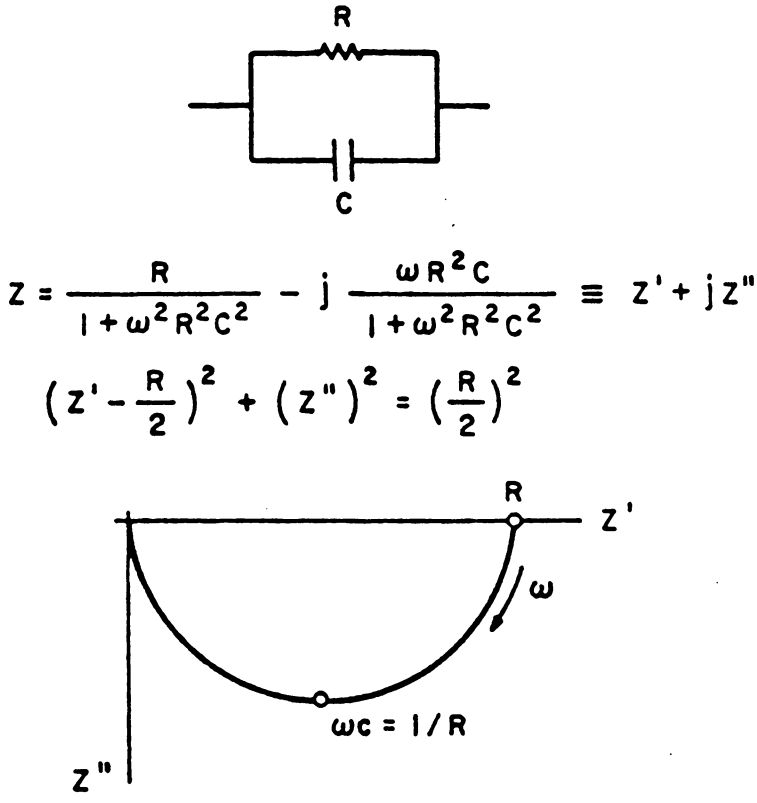

Figure 14. **Impedance plot for single R-C network**

- R, C : equivalent resistance and capacitance values of the circuit.
- Z', Z'' : real and imaginary part of the total impedance Z, respectively.
- ω : angular frequency (increases in the direction indicated in the above figure)

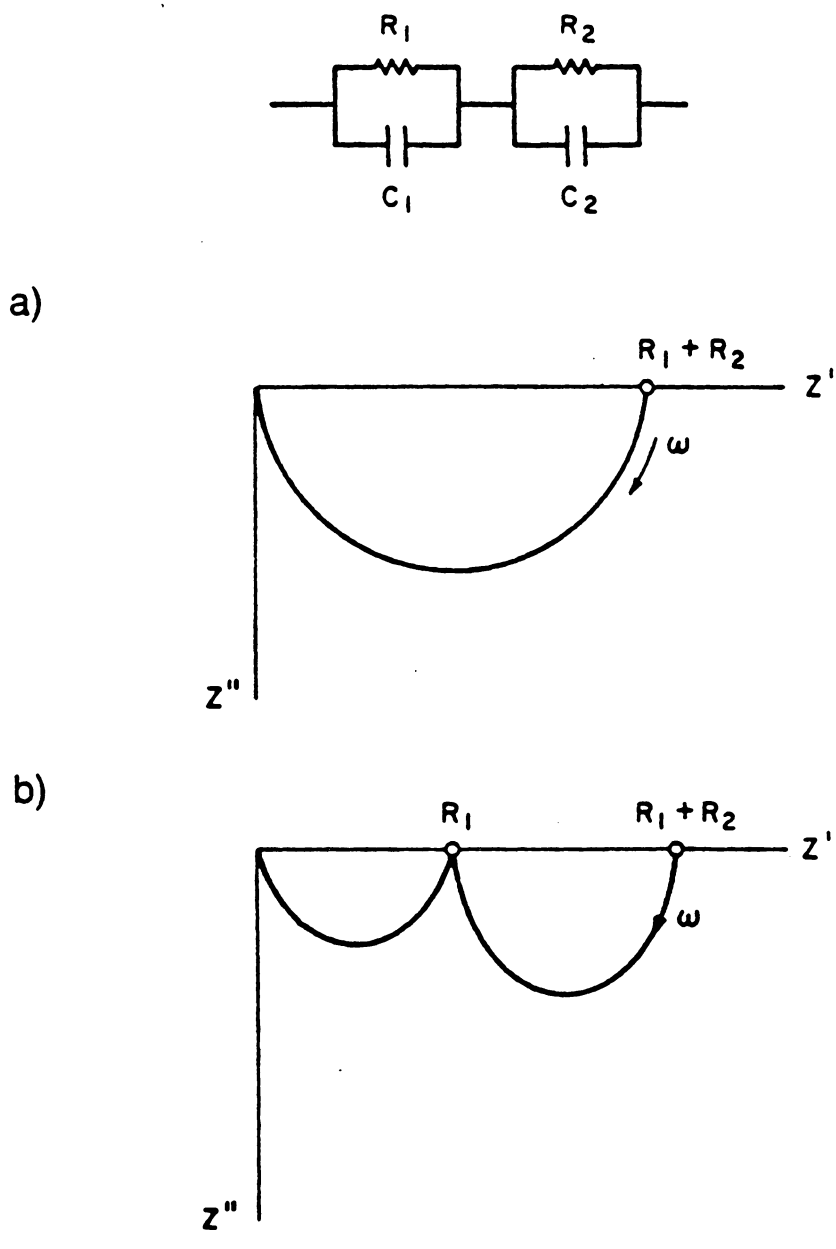

Figure 15. Impedance plots for two-section R-C network

a) $R_1C_1 = R_2C_2$
b) $R_1C_1 << R_2C_2$

The impedance measurements were made with a Hewlett-Packard 4192A Impedance Analyzer with an attachment allowing dc voltage bias up to ±200 V. The frequency range covered was 5 Hz to 13 MHz. The sample temperatures were maintained at values in the 400°C to 600°C range. This is because the upper resistance limit of the above bridge is only 1.2 MΩ , and elevated temperatures are required to bring sample resistances below this limit imposed by the instrument. Since our ultimate goal is a better understanding of $BaTiO_3$-based high resistance, high dielectric constant capacitors at the service temperature range of around room temperature, this measuring range might not be valid. Nevertheless, this could serve as a reasonable experimental tool to determine whether the grain boundary resistance is important or not, because the role of grain boundaries may actually be enhanced at such a high temperature due to the decrease in dielectric constant.

Other measurements done with the above impedance analyzer include capacitance measurements. These were done for X7R blanks with or without guard rings. The impedance analyzer was used to measure capacitance values and dissipation factors in a parallel circuit mode. The fringing field was neglected when a two-electrode specimen was used.†

Voltage-biased impedance measurements : This technique was originally devised by us for high resistance ceramics,[28,80,81] in an effort to identify the various semicircles for each contribution, such as grain, grain boundary, and contact. If a sample is known to be grain boundary controlled (like semiconducting ceramics and varistors), the applied dc voltage bias will reduce the size of the impedance semicircle, especially in the superohmic region corresponding to the observed dc I - V curve. By applying dc bias voltages within the superohmic region, to high resistance, high capacitance ceramics, it may be possible to differentiate one semicircle from the others, since at least

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† For ac impedance analysis, samples with two electrodes were mainly used, especially for polished samples. Hence, fringing effect around the edge of the sample might be a possible source of error when estimating dielectric constants. However, this found to be relatively negligible when compared to a three-electrode specimen. (< 10 %)

one semicircle has to be reduced in size. It is generally expected that grain boundary or contact resistance is more sensitive to the applied voltage than grain resistance, since the former is an exponentially decreasing function of voltage. This technique will be further explained in Chap. 5.

In this chapter, various experimental and specimen preparation techniques were reviewed. These include thermoelectric and ionic transference number (galvanic cell) measurements in order to determine the dominating charge carrier, and electrical resistivity, current-voltage and complex impedance measurements to determine their possible transport modes. These will be discussed, in more detail, in the next chapter with experimental results.

Chapter 5. Results and Discussion

5.1 Thermoelectric Effect

It has been established that thermoelectric effect measurements can be used to identify the sign of the dominant charge carrier in an unknown specimen by measuring the thermal voltage generated, when the specimen is subjected to a temperature gradient. This is because the majority carrier, in a semiconductor, diffuses to the colder end, until an equilibrium is reached between a chemical potential gradient and an induced electric field. Although this same role can conceivably be played by Hall effect measurements, the former is preferred because of the relative ease of the experiment, and most of all because of the low mobility capability of thermoelectric measurements. Hall effect measurements are generally good for materials with mobility higher than about $0.1 cm^2/V \cdot sec$, and they have not been successfully applied to X7R capacitor ceramics even for heavily reduced samples of low resistivity, at room temperature.[10] Hall mobilities were found to be less than 0.01 $cm^2/V \cdot sec$ for both as-received and reduced X7R samples. (Hall voltage is buried in noise.) For that reason, thermoelectric or Seebeck effect measurements have been widely used in low mobility ceramic materials.[82,83]

The thermoelectric or Seebeck coefficient S is defined by the relation,

$$S = \frac{\Delta V}{\Delta T} \qquad (5.1)$$

where ΔT is the temperature difference and ΔV the generated thermoelectric voltage between the two electrodes. (See Fig. 11) In order to check the validity of the experimental systems used, two preliminary measurements were performed. The first was a junction thermoelectric voltage effect measurement, which is necessary to prove that the measured thermoelectric voltage is not due to the voltage generated across the thermocouple junctions. As illustrated in Fig. 16, the measured thermal voltage generally contains thermoelectric voltages both due to sample and due to thermocouple junction. In order to obtain the true Seebeck voltage of the specimen, the junction thermoelectric voltage may be discounted by measuring two thermal voltages (V_1 and V_2), and by taking the mean value (ΔV). It was observed that ΔV calculated from the equation given in the figure was the same within experimental uncertainty as the thermoelectric voltage measured across the separate voltage probes. Hence, the junction thermoelectric effect was proved to be negligible, and subsequent measurements were done using voltage probes attached to the sample.

The second experiment was measurement of a standard material of known thermoelectric coefficient. A p-type silicon single crystal bar cut from a grown crystal was used for this purposes. This single crystal specimen has a room temperature electrical resistivity of about 70 Ω·cm, with dimensions 3.8mm × 3.8mm × 7.0mm. Thin film aluminum electrodes were thermally evaporated onto the smaller faces. The results are shown in Fig. 17, and are in close agreement with those in the literature.[84] The change of S values from positive to negative above about 230°C indicates that the intrinsic carrier concentration starts to dominate over the extrinsic carrier concentration. When both electron and hole concentrations are about equal, negative S values are expected, due to higher drift mobility of electrons, and this is verified in the figure.

The results are shown in Fig. 18 for as-received and hydrogen reduced X7R samples at 250°C. These results correlate well with the above linear relation.

The S values are shown versus temperature in Fig. 19, where measurements were made on an as-received chip at above 200°C. (due to its high resistance at lower temperatures)

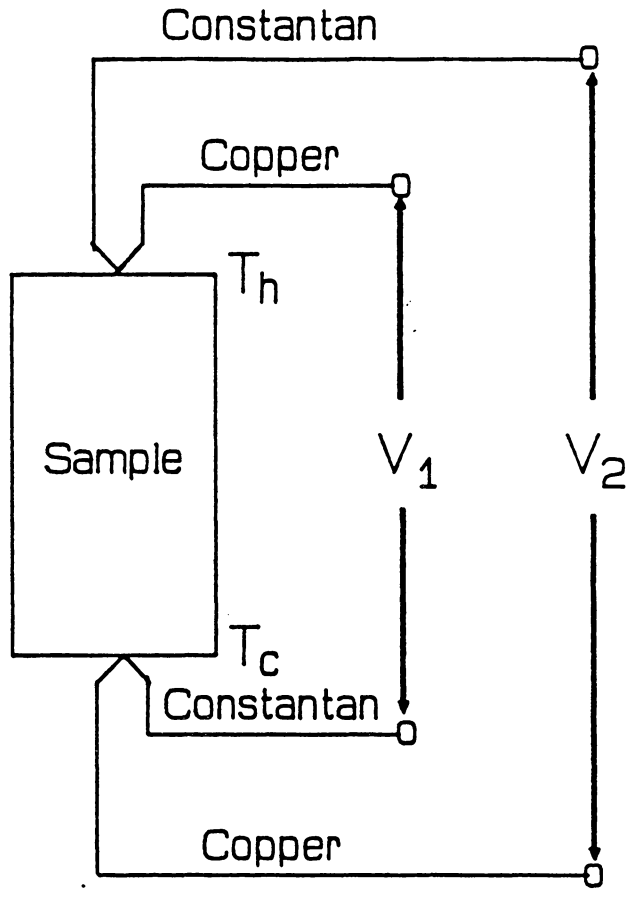

Figure 16. **Schematic to measure thermocouple effect on Seebeck voltages**

$$V_1 = \Delta V + V_J$$

$$V_2 = \Delta V - V_J$$

$$\therefore \Delta V = \frac{V_1 + V_2}{2}$$

(T_h : the temperature of "hot" end, T_c : the temperature of "cold" end)

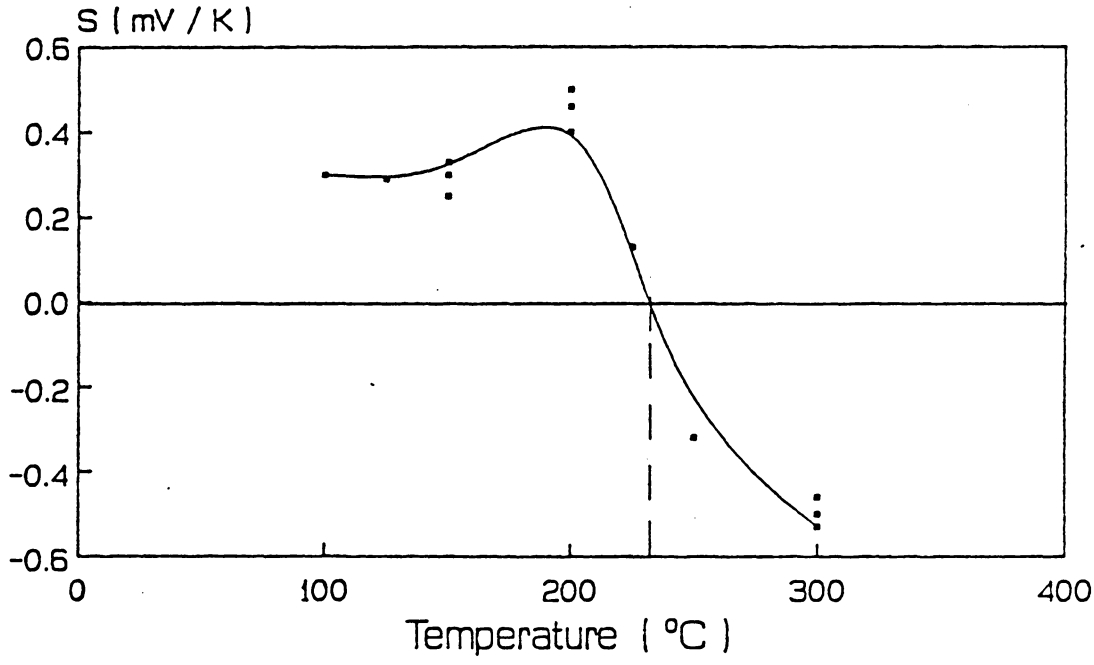

Figure 17. Thermoelectric coefficient of p-type Si versus temperature

- Sample is a bar cut from grown ingot with electrical resistivity of about 70 Ω·cm at room temperature. (3.8mm × 3.8mm × 7.0mm)
- Aluminum electrodes were thermally evaporated onto the smaller faces.
- Solid curve indicates best fit.

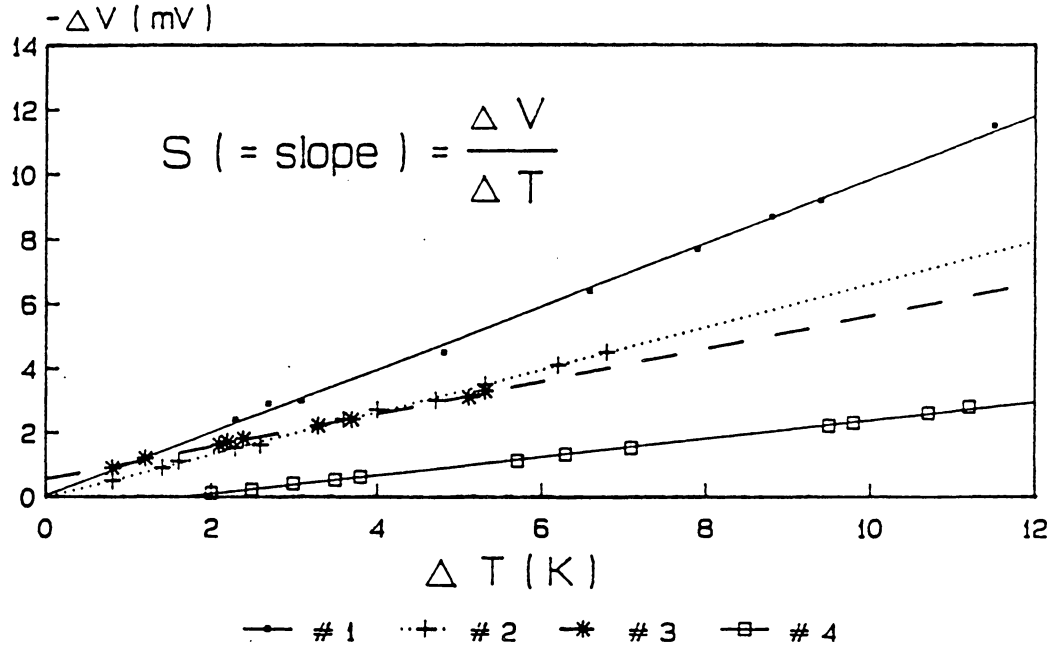

Figure 18. **Seebeck voltages for X7R chips at 250 °C, versus temperature difference between contacts**

#1 : as-received, #2 : reduced at 900 °C for 5 hours
#3 : reduced at 1000 °C for 5 hours, #4 : reduced at 1000 °C for 44 hours

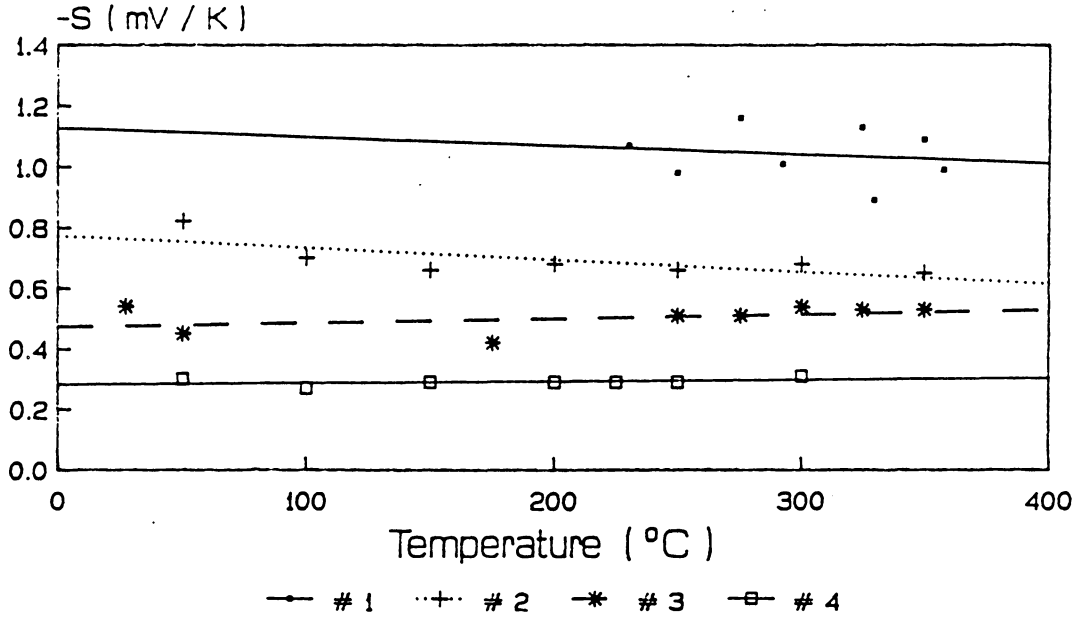

Figure 19. **Thermoelectric coefficients versus temperature for X7R chips**

#1, #2, #3 and #4 : same as Fig. 18

The flatness of the S versus T curves indicates that the charge carrier concentration is nearly independent of temperature. This is because the donor sources such as oxygen vacancies are nearly completely ionized above room temperature, and the temperature dependence of conductivity σ is mainly attributed to drift mobility. From the sign of S values for both as-received and reduced X7R chips, it can be concluded that the dominant charge carrier is negative. (such as an electron and/or an anion)

The dominant charge carrier concentration can be calculated from the Seebeck coefficient, if certain assumptions are made. In general, charge carrier concentration n can be calculated from the equation for the Seebeck coefficient S,[6,85]

$$S = \frac{k}{q}\left[\ln \frac{N_c}{n} + \frac{H^*}{kT} \right] \qquad (5.2)$$

where N_c is the density of the states in the conduction band, H^* a heat of transport,† and $k/q = 8.63 \times 10^{-2}$mV/K. Eq. 5.2 is based on the classical band picture, and does not apply to a small polaron hopping transport.

Electrical conduction has been attributed to small polaron hopping for single crystalline $BaTiO_3$,[85] for reduced single crystals of $LiNbO_3$,[86] for spinels,[82] and for wustite.[83] For the case of small polaron hopping, the heat of transport H^* is normally negligible, and the hopping site concentration N replaces the density of the states in the conduction band N_c . The concentration of small polarons can thus be found from the expression for the thermoelectric coefficient[85,86]

$$S = \frac{k}{q} \ln \frac{N}{n} \qquad (5.3)$$

where N is the hopping site concentration and n the small polaron concentration.

Due to the small drift mobility obtained for X7R ceramic samples, it was necessary to interpret our results by the small polaron hopping mechanism mentioned above. If the electrons are assumed to be trapped at the positive titanium ion sites,[85] then $N = 1.56 \times 10^{22}\,cm^{-3}$ (assuming

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† A heat of transport is associated with particle migration in a thermal gradient.

the X7R samples are pure $BaTiO_3$),† and n can be determined using Eq. 5.3. These n values are shown versus inverse temperature for $BaTiO_3$-based X7R chips in Fig. 20. The reduced samples have essentially constant carrier concentrations, with the most heavily reduced sample having $n \sim 5.0 \times 10^{20}\,cm^{-3}$ at room temperature, and the as-received sample having a weak temperature variation, with $n \sim 3 \times 10^{16}\,cm^{-3}$ at room temperature (extrapolated). All of the reduced samples were assumed homogeneous, since surface layers were removed by polishing.

In addition, if the above results are combined with the conductivity measurements, the drift mobility μ can be estimated from Ohm's law.

$$\sigma = \frac{1}{\rho} = nq\mu \qquad (5.4)$$

where all of the parameters were previously defined.

The drift mobility values thus obtained are shown versus inverse temperature in Fig. 21. Such linear characteristics are expected for small polaron hopping, as mentioned in Chap. 2. The thermal activation energies for carrier concentration $E_{A,n}$, mobility $E_{A,\mu}$, and conductivity E_A are shown in Table 3. It is noted from the table that the concentration activation energies are almost always negligible. This is because all of the donor impurities including oxygen vacancies are completely ionized, and because the band gap of $BaTiO_3$ is high enough to prevent any significant intrinsic carrier formation. (E_g is about 3.1 eV.) Thus, the conductivity activation energy is mainly due to the mobility activation energy.

The conductivity activation energy is $\sim$ 1.2 eV for the as-received X7R samples, which is close to that of a new X7R capacitor (1.2-1.3 eV). The decrease in activation energy of the reduced chip also corresponds to the similar decrease seen in degraded capacitors.[87] This decrease in activation energy with reduction could be due to the passivation of the grain boundary layer, which results in

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† This assumption is not strictly true, since X7R samples are not pure barium titanates. However, from Eq. 5.3, it is noted that the same percent of error occurs in the estimation of carrier concentration value, and this is usually negligible. ($\leq$ 10 %)

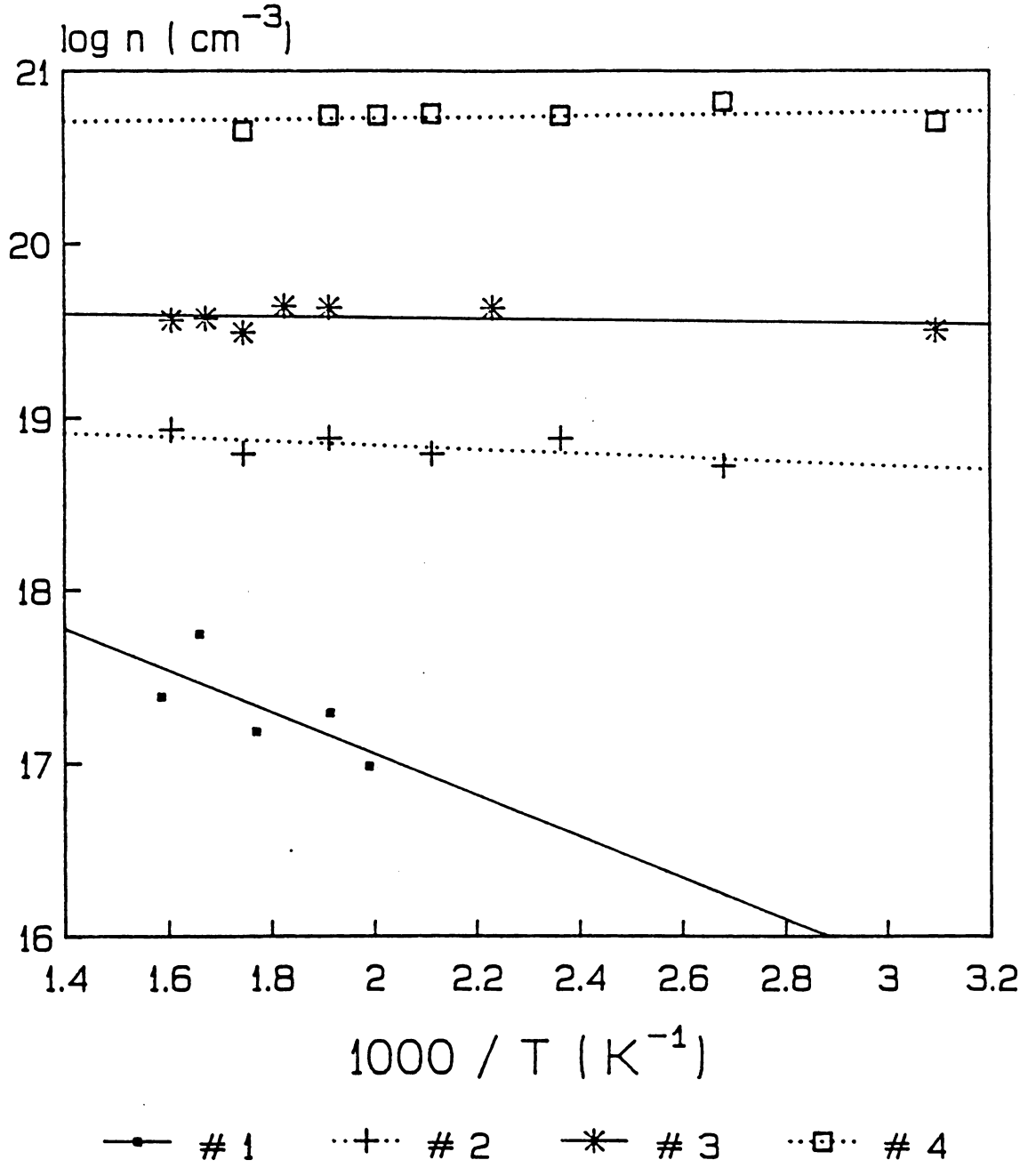

Figure 20. **Carrier concentration versus inverse temperature for X7R samples**

#1, #2, #3 and #4 : same as Fig. 18

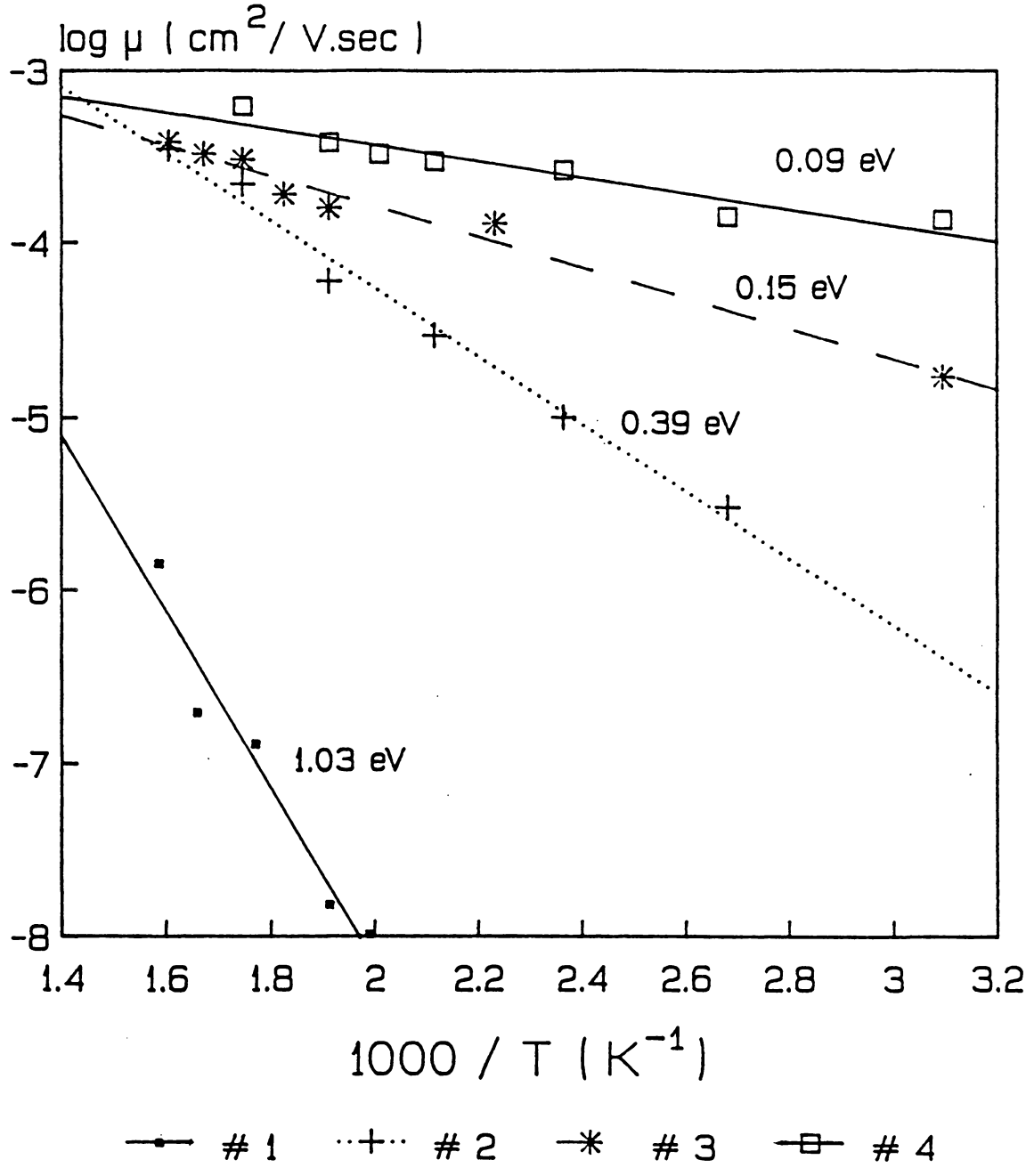

Figure 21. **Drift mobility versus inverse temperature for X7R samples**

#1, #2, #3 and #4 : same as Fig. 18

Table 3. Thermal activation energies (eV) of X7R samples

Sample	$E_{A,n}$	$E_{A,\mu}$	E_A
As-received	~ 0.19	~ 1.03	~ 1.22
Reduced #1	~ 0	0.39	0.39
Reduced #2	~ 0	0.15	0.15
Reduced #3	~ 0	0.09	0.09

Key) Reduced #1 : reduced at 900 °C for 5 hours

Reduced #2 : reduced at 1000 °C for 5 hours

Reduced #3 : reduced at 1000 °C for 44 hours

$E_{A,n}$: carrier concentration activation energy

$E_{A,\mu}$: drift mobility activation energy

E_A : conductivity activation energy

decreased barrier height. In addition, it could be due to the reduced polaron hopping potential. This will be discussed further, at least, for X7R samples in the Section 5.4.

The decrease in resistivity for reduced X7R ceramic chips can be attributed to mobility increase, accompanied by an electron concentration increase, with the temperature dependence residing almost entirely in the mobility.

In summary, the following can be concluded from the thermoelectric measurements:

a) Thermoelectric (Seebeck) coefficients for unreduced and reduced X7R ceramics were negative in all cases, indicating that the charge carrier was of negative charge (electron or anion).

b) The decrease in activation energy for the resistivity of reduced samples was largely attributed to drift mobility.

c) The weak temperature dependence of the carrier concentration indicated nearly complete ionization of donors above room temperature.

d) As the reduction process went further, the thermal activation energies for electrical resistivity and drift mobility dropped.

5.2 Transference Number Measurements

From the results obtained from the thermoelectric measurements in the previous section, it is concluded that the sign of the dominating charge carrier is negative in X7R ceramics. In addition to the thermoelectric results, the ionic transference number t_i was measured in an attempt to identify the dominant charge carrier species (electronic or ionic) in $BaTiO_3$-based ferroelectric capacitors and ceramics.

The experimental setup was described in Chap. 4. Galvanic cell voltages are shown in Figs. 22 and 23, for two cases: yttria stabilized zirconia (YSZ; 9.4 M% Y_2O_3) and several kinds of barium titanates at 700°C and 850°C, respectively. The zirconia sample serves as a pure ionic conducting reference,[88,89] and produces voltages slightly less than those predicted by the Eq. 4.4, rewritten here as

$$V_t = \frac{RT}{4F} \ln \left[\frac{P''_{O_2}}{P'_{O_2}} \right] \qquad (5.5)$$

which is represented by the solid line in Figs. 22 and 23. It is evident that the electrical transport in the zirconia sample used is nearly 100 % ionic, with better agreement occurring between the calculated curve and measured points at higher temperatures. The effect of temperature on galvanic cell voltages in the 500 to 850°C range is shown in Fig. 24.

According to Bray and Mertin,[76] 10 % yttria added zirconia has an electronic transport number of ≤ 0.005 in the pure oxygen-air galvanic cell. Also, Verkerk et al.[77] reported that the ionic transference number of yttria stabilized zirconia is about 1 in the temperature range of 600 to 900°K. It is noted from Fig. 23 that the possible errors for the measurements arises from the leaky O-ring seal,† and from the oxygen partial pressures which are estimated by flow rates, since the inversion of data points occurs when a different flow rate was used. (at 20 % O_2, the lower flow data shows a higher galvanic voltage, which is not likely.)

The more important galvanic voltage data from Figs. 22 and 23 are, however, those for $BaTiO_3$-based samples, which generate essentially zero voltages at all pressures and temperatures used. It is noted that each data point for $BaTiO_3$ in these figures represents data for four different types of $BaTiO_3$ used. These include $Ba_{0.99}TiO_{3-x}$, $BaTiO_3$, $Ba_{1.01}TiO_{3+x}$, and a $BaTiO_3$-based X7R capacitor plate. For all of these samples, oxygen ion diffusion is insignificant at temperatures above about 400°C, and therefore probably insignificant at lower temperatures.[90] Also, indirect confirmation of this point can be obtained from the single thermal activation energy over the tem-

† Either gold or platinum O-ring was used to obtain gas-tight seal between glass tube and sample.

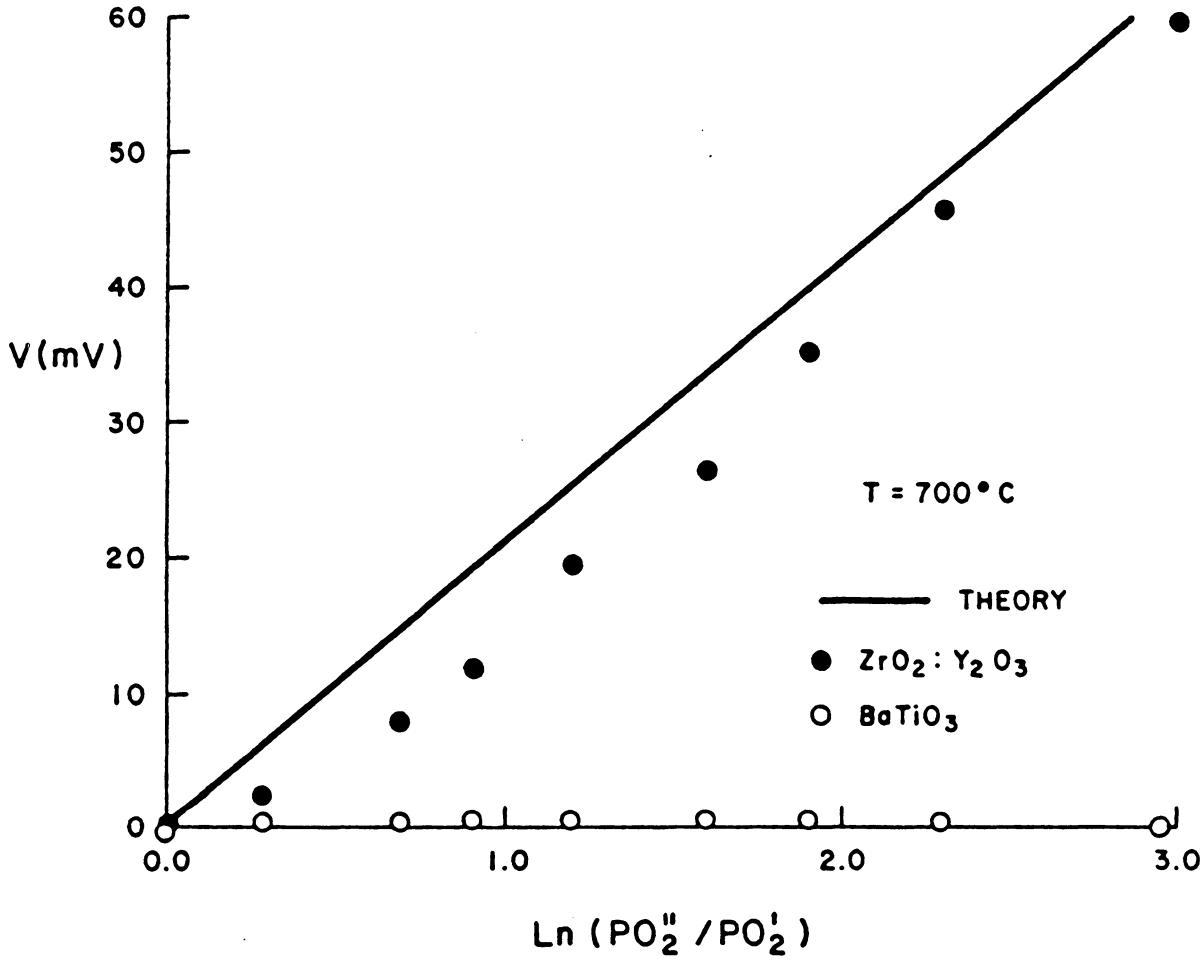

Figure 22. Galvanic cell voltage versus oxygen partial pressure ratio for yttria stabilized zirconia and several kinds of barium titanates at 700 °C (P''_{O_2} = 1 atm)

- Solid line is due to Eq. 5.5.

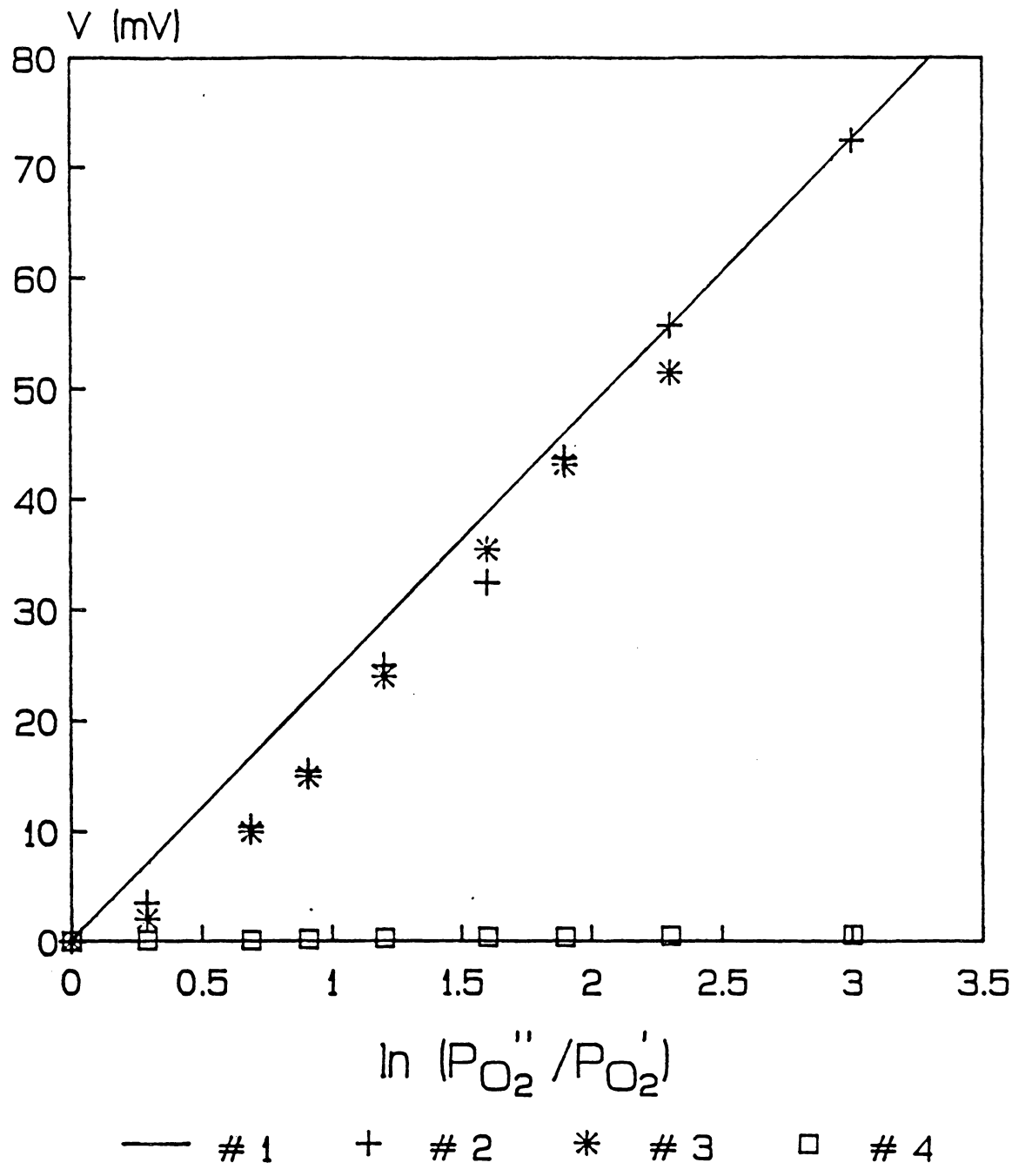

Figure 23. **Galvanic cell voltage versus oxygen partial pressure ratio for yttria stabilized zirconia and several kinds of barium titanates at 850 °C** (at two different flow rates, P''_{O_2} = 1 atm)

#1 : theory (100% ionic; Eq. 5.5), #2 : zirconia at a flow rate of 200 ml/min., #3 : zirconia at a flow rate of 100 ml/min., #4 : $BaTiO_3$ ceramics

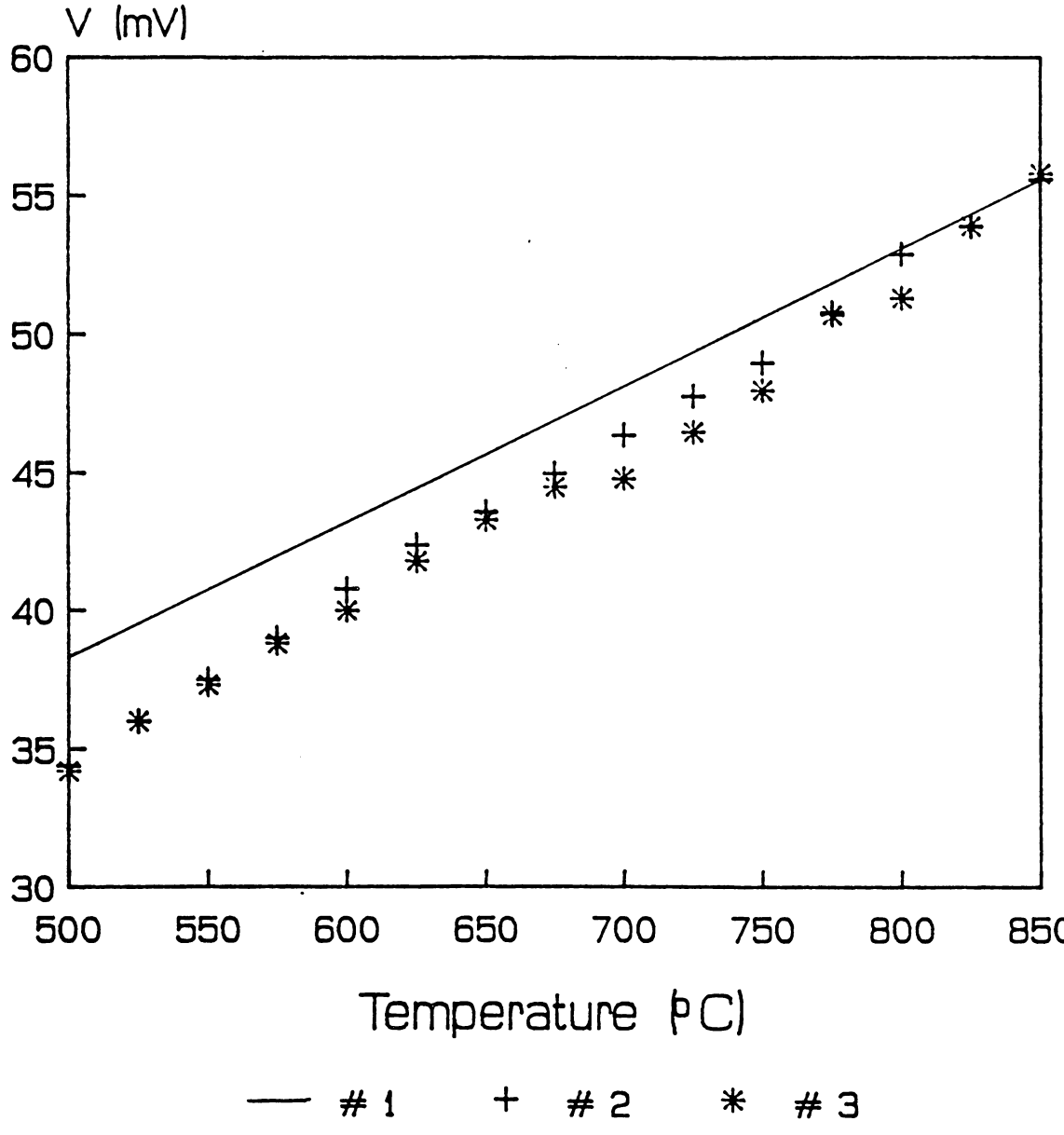

Figure 24. Galvanic cell voltage versus temperature for yttria stabilized zirconia single crystals at the flow rate of 200 ml/min. ($P''_{O_2}/P'_{O_2} = 10$)

#1 : theory (100% ionic; Eq. 5.5), #2 : cooling, #3 : heating

perature range of 150 to 600°C for X7R ceramic samples, which will be discussed in the next section. An electrical interpretation of this is that the rapid increase in electrical conductivity for these $BaTiO_3$ ceramics with increasing temperatures is not due to enhanced diffusion of oxygen or oxygen vacancies.

From this study, the following can be concluded:

a) Ionic transference numbers of various $BaTiO_3$-based ceramics were essentially zero in the temperature range of 400 °C to 850 °C, indicating that the dominant charge carrier in $BaTiO_3$ ceramics was not ionic, but electronic, above about 400 °C.

b) Above results were confirmed by the known ionic conducting reference (YSZ), which showed nearly 100 % ionic voltage, with better agreement occurring between the calculated curve and measured points at higher temperatures and flow rates.

5.3 Current - Voltage Relationships

From the results in the previous two sections, the type of charge carrier in $BaTiO_3$-based X7R capacitors and ceramics was identified to be the electron. It is, therefore, of interest to study the carrier transport mechanisms in these materials. In this section, the results of I-V measurements on chips of varying thickness will be presented to help clarify this problem. The effects of ambient on the electrode-ceramic interface is studied, and results are interpreted in term of thickness of the sample.

5.3.1 As-received X7R Capacitor Ceramic

Current-voltage characteristics for as-received X7R chips are shown in Fig. 25, at five temperatures, in argon and air ambients. The major points related to Fig. 25 are summarized below.[91]

a) There are two distinct regions of different voltage behavior; an ohmic region below about 400 V, and a super-ohmic region above about 400 V.

b) The upper voltage characteristic depends on the ambient; currents increase as roughly $V^{1.9-2.1}$ in argon, and as $V^{1.3-1.7}$ in air. The ohmic region is independent of the ambient.

Another important result is obtained when the current is plotted versus inverse temperature at different voltages, as shown in Fig. 26 for as-received X7R chips. The activation energies are found to be 1.31 ± 0.02 eV, and independent of voltage up to 1000 V (~ 4.4 kV/cm).

The upper voltage region in Fig. 25 can be attributed to space-charge-limited currents (SCLC). This is consistent with a model that we published,[13], where the near 3/2 power law-voltage dependence was attributed to SCLC emitted from electrode asperities, since current injection depends on metal electrode-ceramic interface properties. In that paper, it was proposed that a higher power law should evolve as the ceramic near the electrode degrades, for the increased conductivity of ceramic results in a more nearly planar effective electrode. This electrode-ceramic interface is exposed to the ambient through oxygen-permeable Au-Pt electrode. According to the above model, the I-V slope should increase in the super-ohmic region if the near-electrode ceramic becomes oxygen-deficient, and such slope increases are observed in Fig. 25, when the ceramic is exposed to argon gas.

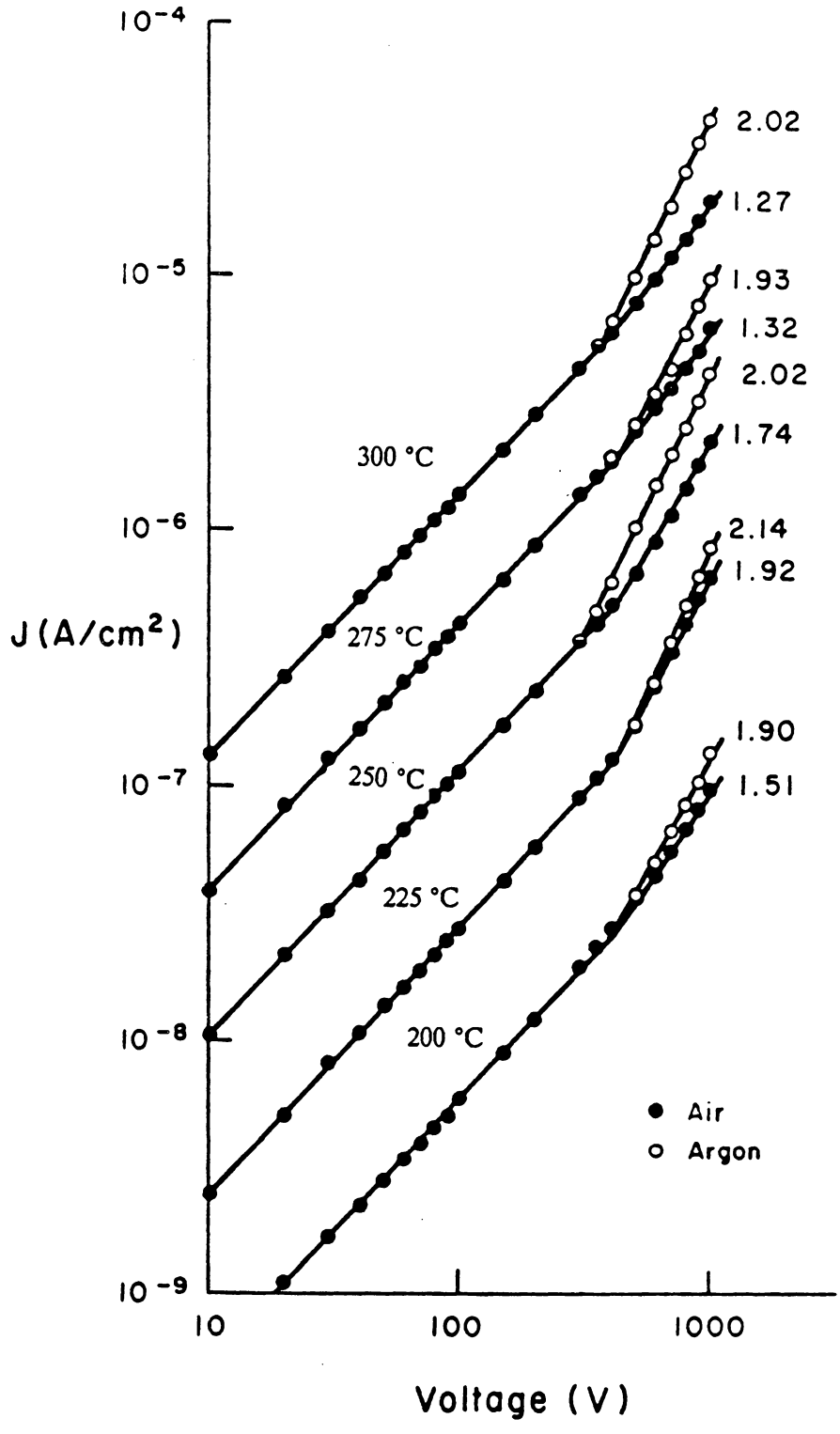

Figure 25. **Current-voltage curves for as-received chips in air and argon ambients at five temperatures** (chip thickness = 2.3 mm; from top to bottom 300, 275, 250, 225, and 200°C) (Numbers represent SCLC slopes.)

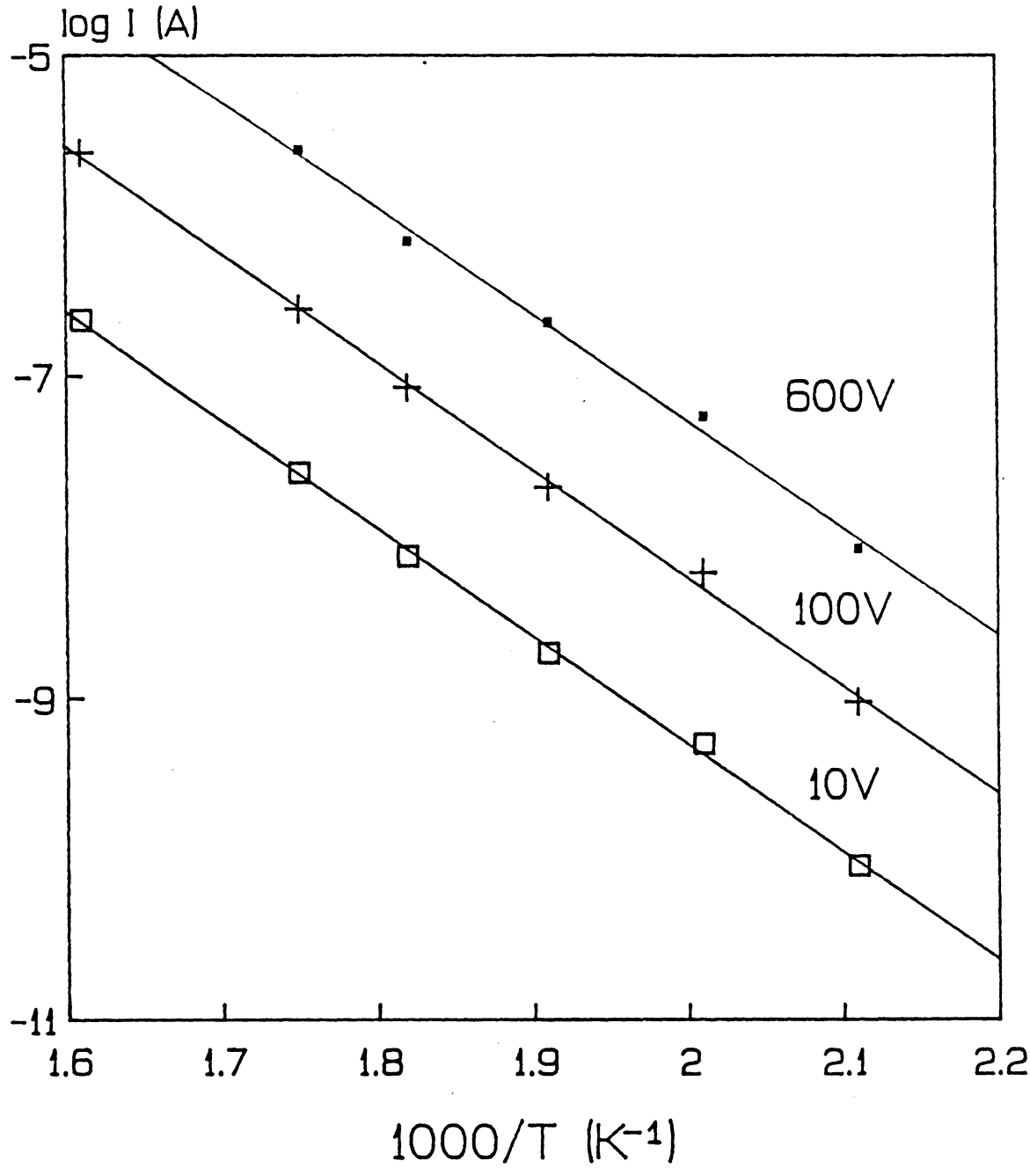

Figure 26. Current versus inverse temperature for the as-received X7R blanks at three different voltages

The time dependence of leakage current, as the ambient is changed from air to argon, is shown in Fig. 27, for electrode configuration A-C (see Fig. 12), at two voltages. The ohmic region, under these measuring conditions, is independent of ambient, as is the current measured in electrode configuration A-B (which measures surface conductance).

From this, it can be concluded that only a very thin region ($\cong$ several atomic layers) is affected if a ceramic is exposed to argon gas, and a small amount of oxygen leaves the ceramic. This is supported by the following observations.

a) Since no change is seen in the ohmic region, the ambient-sensitive part is a negligible fraction of total thickness or cross-section of the sample.

b) No change in surface conductivity was detected, both in the ohmic region and the SCLC region.

Therefore, it is concluded that the ambient dependence observed for as-received ceramics at higher voltages, above 400 volts, is probably due to a current injection mechanism that depends on the electrode-ceramic interface.

5.3.2 Effect of Sample Thickness on I - V Characteristics

Measurements made on X7R chips polished to different thicknesses are shown in Fig. 28. The effect of sample thickness was studied to see if the point emitter model can be applied, as the dielectric thickness decreases. Also, by polishing one side of the sample, it was hoped to find different superohmic behavior as the applied voltage polarity changed according to the space-charge-limited current models.[24]

A super-ohmic region (SCLC) is seen at higher voltages in all cases. The ohmic-to-superohmic transition voltage V_T is defined, and obtained from the figure by the cross point of two straight

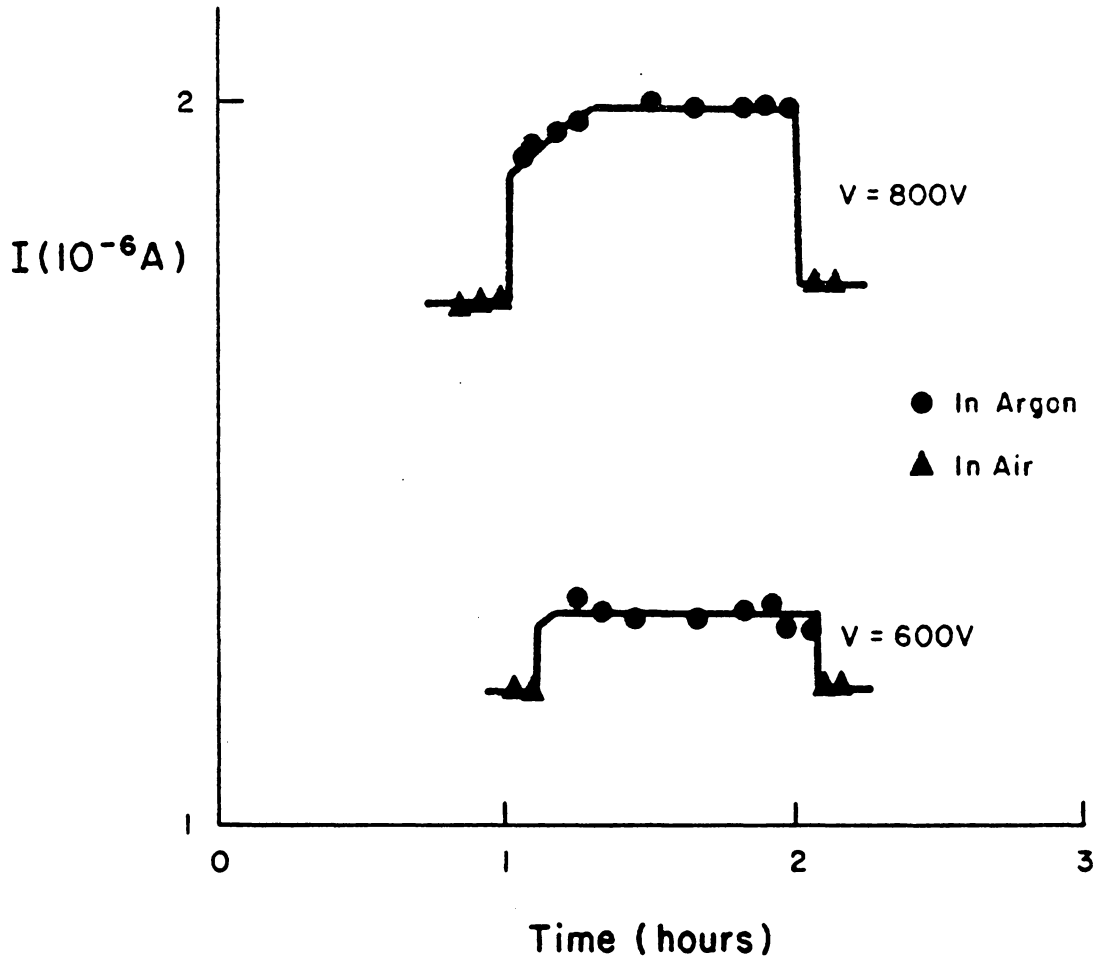

Figure 27. Time dependence of current as ambient is changed, for two voltages at 300 °C for as-received X7R blanks (A-C configuration)

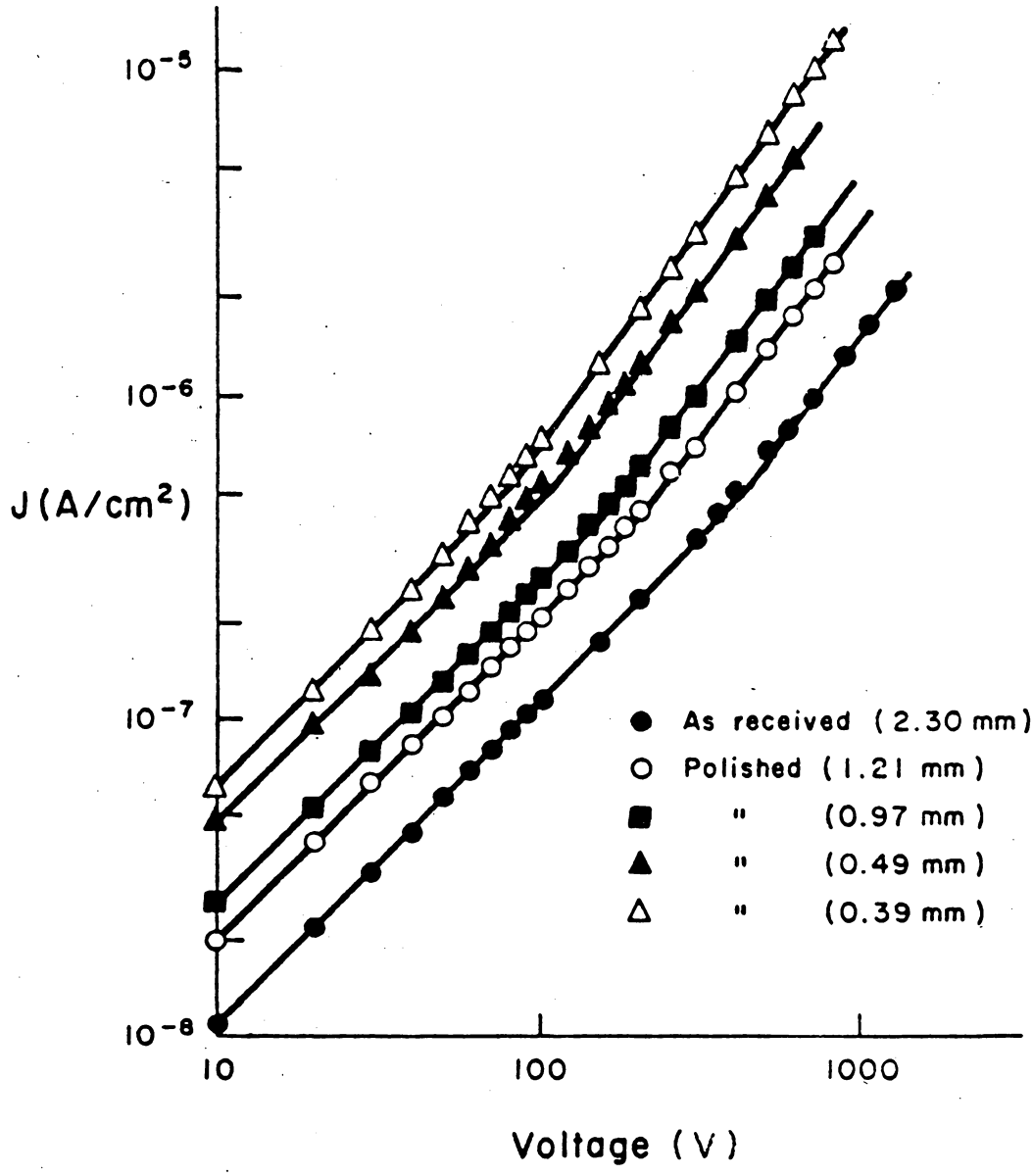

Figure 28. Current-voltage characteristics for chips polished to different thicknesses, measured in air at 250 °C

lines representing ohmic and superohmic regions. It is found that the transition voltage V_T is linearly decreasing with sample thickness d, i.e.

$$V_T \cong 172\,d \qquad \text{(d in mm)} \tag{5.6}$$

and this is shown in Fig. 29.

This linear thickness dependence of the transition voltage V_T is not consistent with either of SCLC theories presented in section 2.2. That is, if planar electrodes are assumed yielding a slope of two, V_T is given by combining Eqs. 2.1 and 2.3

$$V_T = \frac{8}{9}\frac{nq}{\varepsilon\theta}d^2 \tag{5.7}$$

where all of the parameters were previously defined. This equation predicts quadratic thickness dependence of the transition voltage, and in comparing with the resulting linear relationships seen in Fig. 29, the possibility of space-charge-limited current given by Eq. 2.3 may, thus, be questionable.

Also, the point injection model which was proposed to explain the 3/2 slopes observed in MLC capacitors is not adequate because it predicts the transition voltage-thickness relationship such as

$$V_T = \frac{9}{8\pi^2}\frac{nq}{\varepsilon\theta}\frac{A^2}{d^2} \tag{5.8}$$

which is obtained by equating Eqs. 2.1 and 2.5 for one type of charge carrier. According to this equation, the transition voltage V_T should increase as the sample thickness decreases.

In order to satisfy the observed linear relationship between V_T and d, the following equation best describes the relation between current density, voltage, and thickness in the superohmic region:

$$J \propto \left[\frac{V}{d}\right]^x \tag{5.9}$$

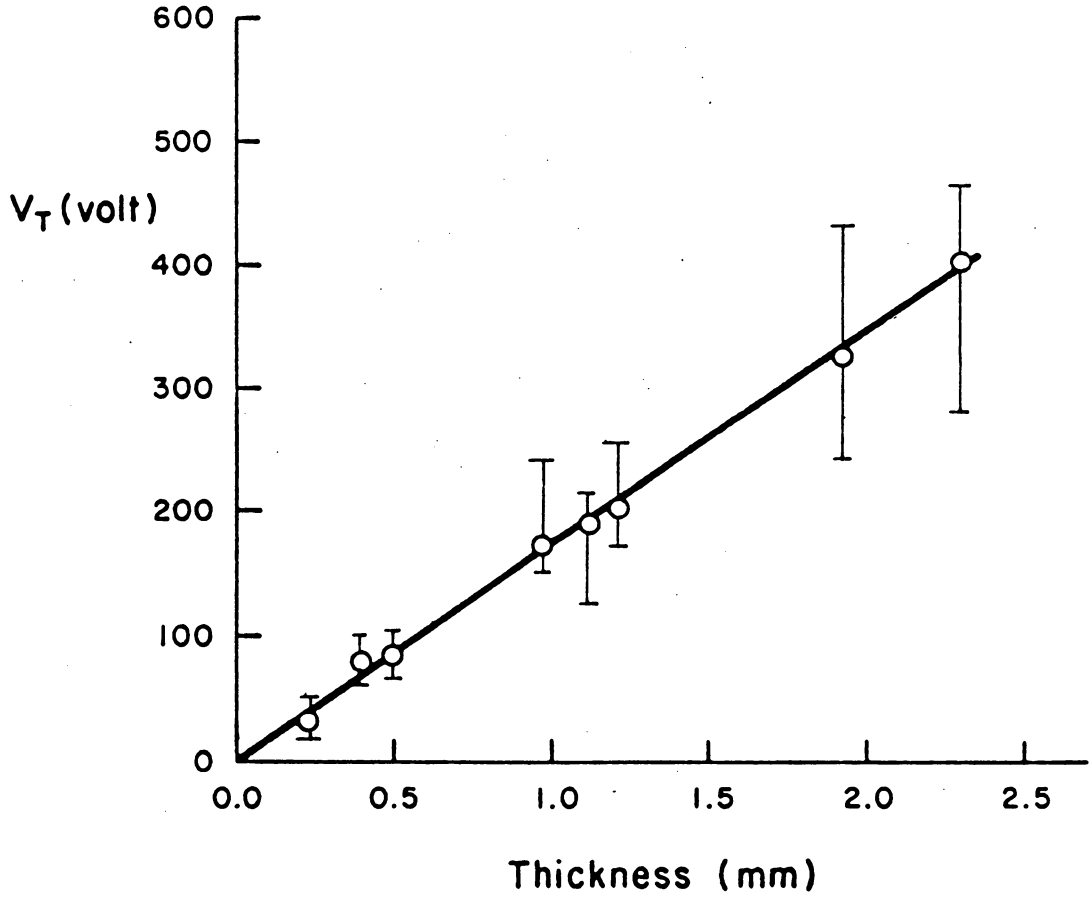

Figure 29. Dependence of transition voltage on sample thickness

where x is a constant which has the value between 1.3 and 2.1. This relationship is somewhat similar to the one proposed by Branwood et al.,[92] which described the observed superohmic characteristics in single crystal $BaTiO_3$, given by

$$I = a\frac{V}{d} + b\left[\frac{V}{d}\right]^2 \qquad (5.10)$$

where a and b are experimental constants.

According to SCLC theory for spherical electrodes of radius r_c (cathode) and r_a (anode), the current should be independent of thickness $(r_a - r_c)$ only if $r_a >> r_c$.[93] However, r_a for the samples used here should be represented by thickness d. In this case, the above inequality may not be satisfied, and in fact, even in the thinnest sample (0.22 mm), the thickness may be too large to apply the above point injector model compared to MLC capacitors.

The electrical parameters for the chips used are summarized in Table 4. (in calculating the dielectric constant, electric field fringing was neglected, when two-electrode samples were used.) It is seen that the resistivity and dielectric constant values are essentially independent of sample thickness, indicating that the modified surface region in X7R chips are not important in these parameters. Hence, it can be concluded from this study that contact resistance is not important. (Another piece of evidence which supports negligible contact resistance will appear in the next section.)

In addition, for a given chip, the transition temperature V_T is independent of temperature, as shown in Fig. 30, for chips of 1.21 and 2.30 mm thickness. This indicates that the voltage prefactors for the two current regions have equal temperature dependences. Since the ohmic prefactor for one type of carrier such as an electron $(nq\mu\frac{A}{d})$ is a function of carrier concentration and mobility and the prefactor for SCLC is the function of mobility only,† this indicates that the carrier concentration in this case is not a function of temperature, which was confirmed by thermoelectric measurements (see section 5.1). In other words, a temperature independent V_T is consistent with the fact that

† In the SCLC region, injected carrier concentration exceeds the native carrier concentration n_o, and the transport is governed by the magnitude of drift mobility.

Table 4. Electrical parameters of X7R chips for several thicknesses.

1. SCLC slope and resistivity : air at 250 °C
2. Dielectric constant : air at room temperature (~ 20 °C)

d (mm)	Superohmic Slope	Resistivity (Ωcm)	Dielectric Constant
2.30	1.3-1.8 †	4.1×10^9	2830
1.92	1.4	3.5×10^9	2878
1.21	1.3	4.1×10^9	2300
1.12	1.3	4.1×10^9	2430
0.97	1.3	3.9×10^9	2320
0.49	1.3	4.3×10^9	
0.39	1.4	4.2×10^9	
0.22	1.2	5.3×10^9	2880

† several measurements on several samples (as-received)

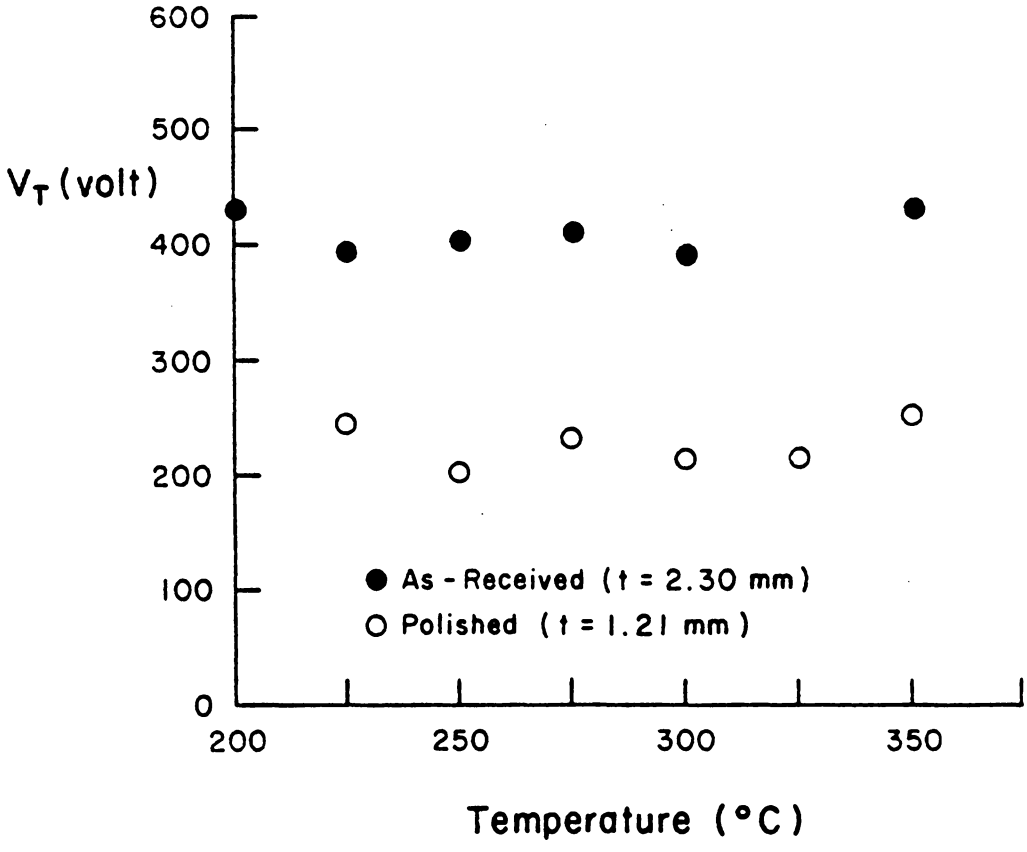

Figure 30. Dependence of transition voltage on temperature, for two chips

carrier concentration n is nearly constant,[13] and both ohmic and space-charge-limited currents are proportional to μ.

For comparison, I-V characteristics of a 100 nF X7R chip capacitor are shown in Fig. 31. From the figure, the following is noted:

a) The slopes of I-V characteristic curves are approximately equal to 1.5 within the measuring range of 10 to 300 V at the temperatures indicated. Using Eq. 5.6, with a thickness of 1.5 mil, V_T should be about 6 volts, and below this voltage, the ohmic region has to appear. Such a transition in the 1 to 10 volt range has been reported.[94]

b) Effect of ambient on the SCLC slopes is not observed. This is due to the fact that the electrodes in MLC capacitors are imbedded in the ceramic, so that the electrodes are not affected by the argon gas. Also, if the electrode is not oxygen permeable, which is true in MLC electrodes (lead-based), the electrode-ceramic interface will not change. Such an effect is observed in polished X7R blanks with silver electrodes (See top curve in Fig. 32), since silver is not permeable to oxygen. The same specimen, with Au-Pt electrodes, showed ambient dependence (See bottom curve in Fig. 32). The apparent difference in resistance could be due to slightly different electrode areas or due to different electrode materials.

5.3.3 Polarity Effect on I - V Characteristics

According to the point emitter model of space-charge-limited current (Chap. 2), the roughness of an electrode may be critical. In order to observe the effect of electrode-ceramic interface topology on leakage current, several chips were polished preferentially on one side and electrodes were applied to both sides. A typical example is shown in Fig. 33, where it is evident that polarity

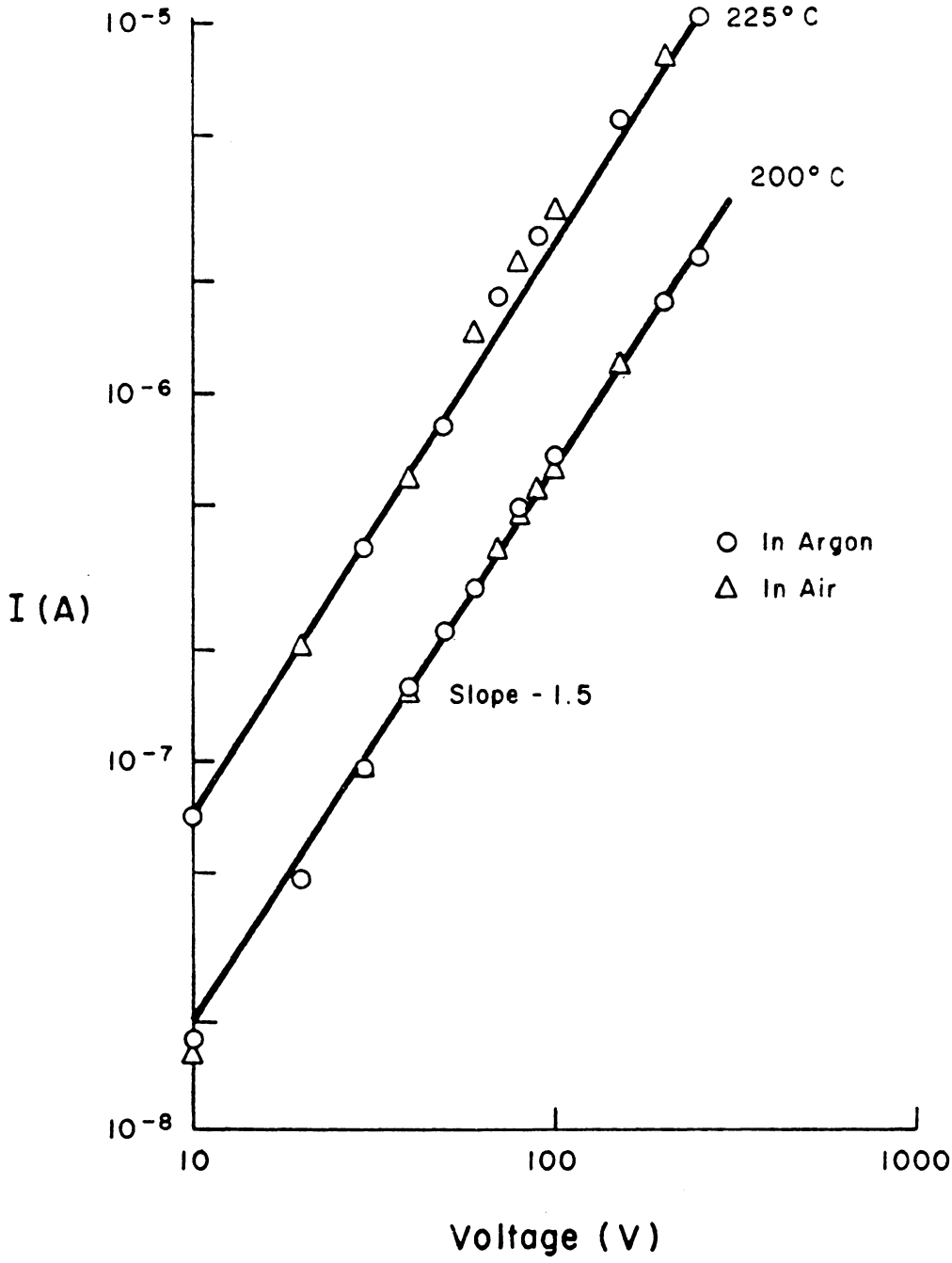

Figure 31. Current-voltage characteristics for 100 nF MLC X7R chip capacitor

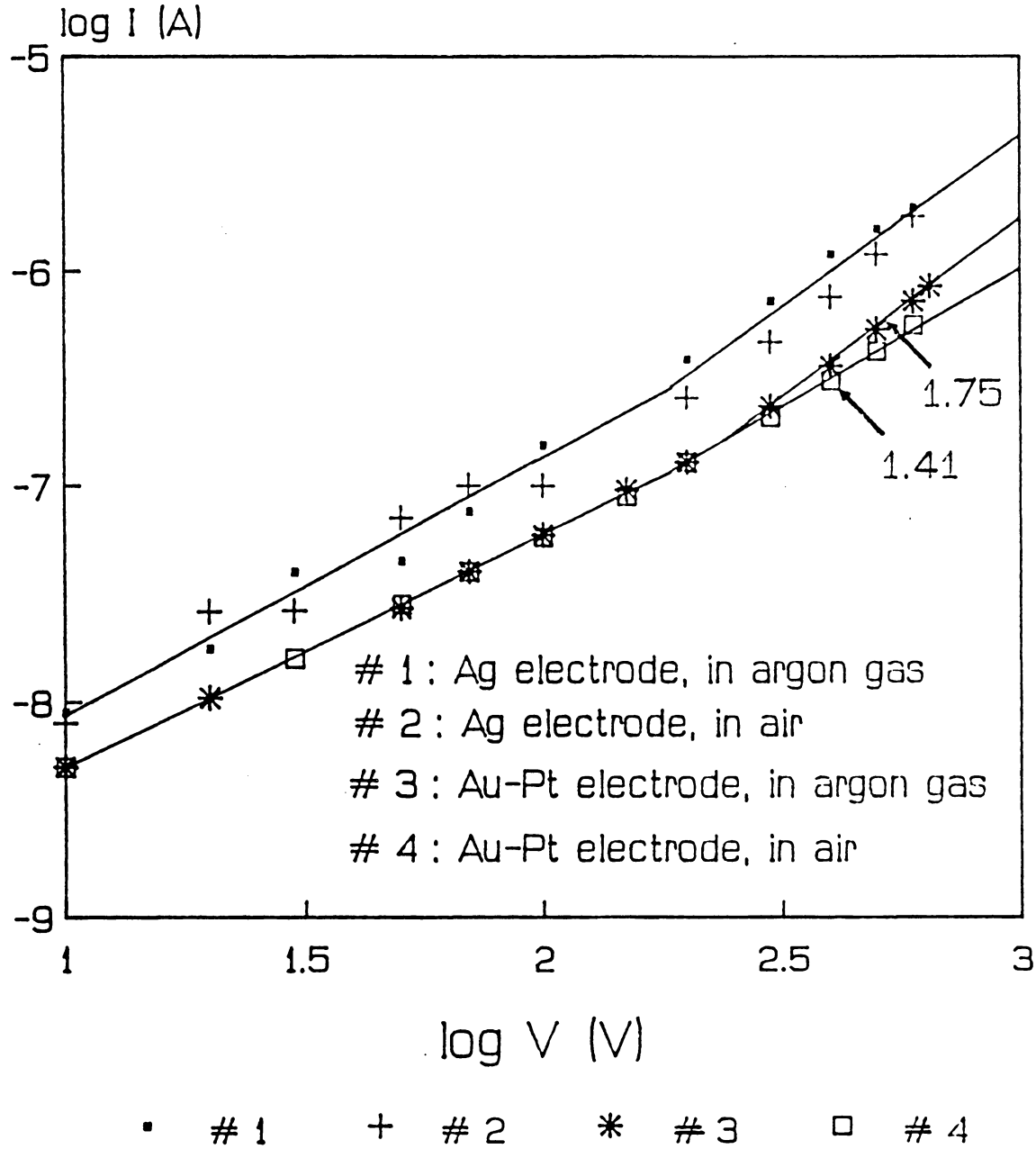

Figure 32. **Current-voltage characteristics for 0.57 mm chips polished on one side only with two different electrodes**
(Numbers denote SCLC slopes.)

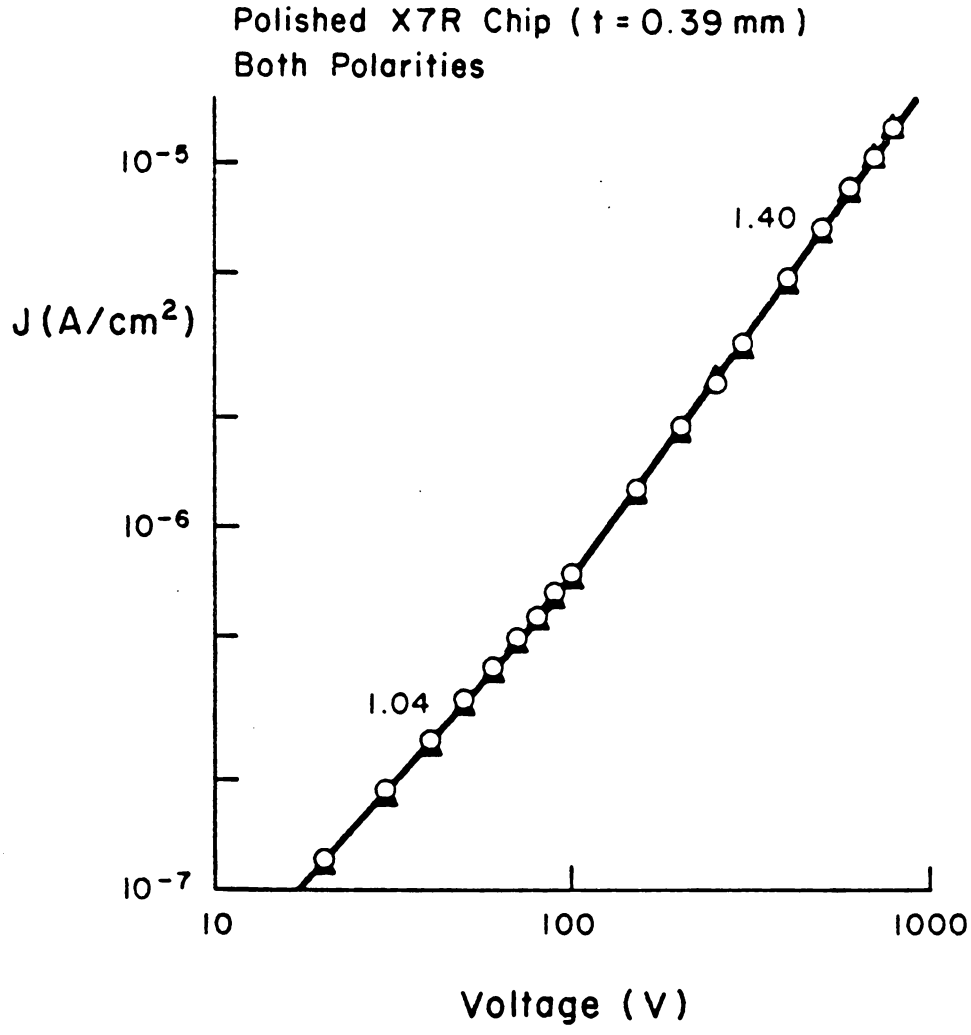

Figure 33. Current-voltage characteristics for 0.39 mm chip polished on one side only with Au-Pt electrodes

reversal has no effect on leakage current even above the transition voltage V_T, regardless of the surface smoothness by polishing. Scanning electron micrograph indicated that the polished side appeared much smoother than the unpolished side. (Fig. 34)

From this experiment, it was originally expected that polarity reversal would change leakage current, as was observed in thick-film capacitors.[91] However, this was not the case for X7R blanks, and could be due to the following:

a) The sample in Fig. 34 is 0.39 mm thick, and is at least 10 times thicker than MLC capacitors and thick film capacitors. This relative "thickness" could reduce the effect of electrode asperities compared to thin layers, so that enhanced emission from the point cathode could be nullified. This could explain the observed behavior in the ohmic region.

b) The polished side is still rough enough on a microscopic level to emit preferentially at certain locations.

c) The point emitters might be low-resistivity grain boundary regions near the electrode, in which case emission from the two sides would be more nearly symmetric. However, this does not account for the observed polarity effect in thick film capacitors.

d) The $V^{3/2}$ model may be incorrect.

Finally, it is worthwhile to present the capacitance measurements results as a function of sample thickness at a fixed frequency of 1 kHz, in order to verify that the data obtained in this section are not due to contact effects, but are the result of bulk properties. This will provide another measure to exclude contact resistance effects in Au-Pt electroded X7R capacitor ceramics, since capacitance per unit area values are expected to decrease inversely proportional to sample thickness for the capacitors with negligible contact resistance.

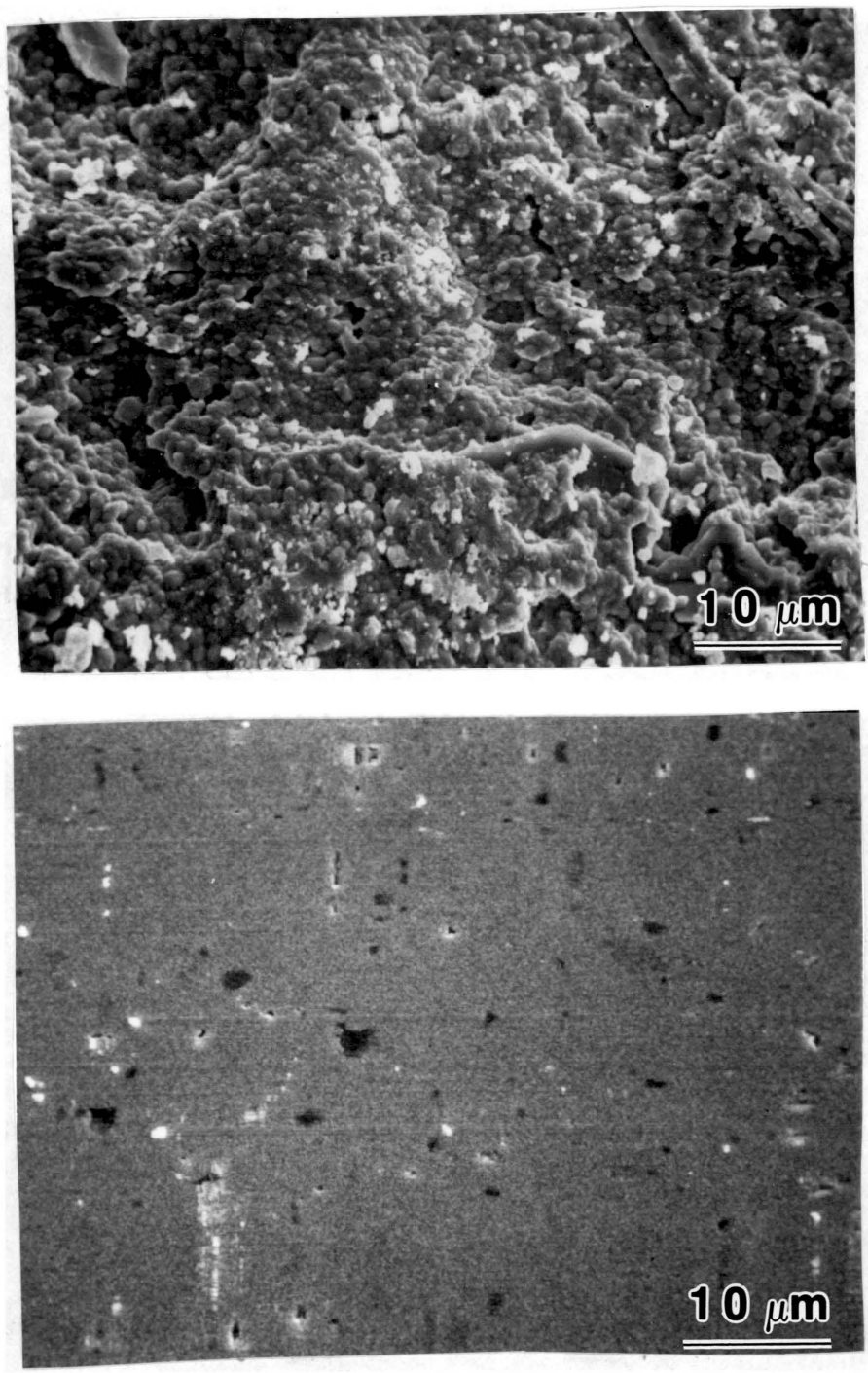

Figure 34. **Scanning electron micrographs of unpolished (top) and polished (bottom) X7R chips** (Polishing was done by 0.05 μm alumina powder.) (X2000)

If contact resistance was present, then contact capacitance would contribute to the effective capacitance, and ε_{eff} would not be constant with sample thickness. (Eq. 5.11)

$$C = \varepsilon_0 \varepsilon_{eff} \frac{A}{d} \qquad (5.11)$$

From Table 4 (p. 77), the constancy of ε_{eff} is evident and it can be concluded, based on this observation, that the contact resistance (hence contact capacitance) is negligible, and the properties measured are due to bulk of the samples.

In summary, the following can be concluded from the current-voltage, and resistivity measurements:

a) Noninternally electroded chips of varying thickness, made from ceramic similar to that of X7R MLC capacitor, exhibit ohmic and superohmic I - V behavior, with only the superohmic case dependent on ambient. The ambient dependence is attributed to changes at the electrode-ceramic interface, not to bulk effects.

b) Chip electrical parameters (resistivity, dielectric constant, activation energy) are independent of chip thickness, indicating that a modified surface region (distinguished from electrode-ceramic interface) is not important.

c) The ohmic-to-superohmic transition voltage varies linearly with sample thickness as $V_T = 172d$, requiring the superohmic I - V characteristics to vary as $(V/d)^n$, with n between 1.3 and 2.1.

d) Chips polished on one side only give polarity-independent currents.

5.4 Complex Impedance Measurements and Transport Mechanisms

Probably the two most dominant transport mechanisms for high resistance, high dielectric capacitance ferroelectric ceramics are small polaron hopping,[29,34,83,86] and grain boundary transmission.[28,45] For some material, the latter seems to be dominant, whereas for $BaTiO_3$-based X7R ceramics, the former seems more promising because the thermal activation energies are shown to be voltage-independent.[78]

One of the most direct methods for probing grain boundary impedance of electronic materials is complex impedance measurements.

In this section, the experimental impedance data for X7R ceramics and various types of $BaTiO_3$ ceramics are presented and discussed in the light of the transport mechanism along with some dc measurement data.

5.4.1 X7R Capacitor Ceramic

As-received X7R plates of 1.0cm × 1.0cm × 0.12cm plus four polished $BaTiO_3$-based X7R type capacitor chips of different thicknesses were used as samples. Thicknesses of polished chips were 0.14 mm, 0.21 mm, 0.41 mm, and 0.69 mm. Au-Pt ink (Engelhard #A-3395) was used as electrode material. The nominal area of these polished chips is 6.2 mm × 5.3 mm. The temperature ranged from 400 to 600 °C. This relatively narrow range was necessary due to the limitation imposed by the impedance analyzer,† and the conducting Ag epoxy. (since silver degrades at high temperatures and epoxy loses its adhesion)

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† Hewlett-Packard 4192A LF Impedance Analyzer: maximum resistance = 1.2 MΩ, frequency range of 5 Hz to 13 MHz

It is of interest to initially examine impedance plots for samples which are either known to be grain boundary controlled, or grain boundary free. The former case is represented by a commercial ZnO varistor, and the latter by a disc of single crystalline yttria stabilized zirconia.[28,95]

Some important results regarding this technique are the following:

a) The varistor yielded a single semicircle, which was attributed to grain boundaries. This is reasonable since, in the varistor, all of the applied voltage is dropped across the grain boundary, since the grain itself is semiconducting. Also, by applying dc voltage bias, the collapse of these grain boundaries occurred, resulting in the semicircle shrinkage. This indicates the usefulness of the voltage bias technique to probe grain boundary impedance.

b) The zirconia sample showed a semicircle attributable to its bulk (grain) plus a partial semicircle at lower frequencies which can be attributed to contacts.[96,97]

Figures 35 to 37 show typical complex impedance plots for polished X7R chips. From these figures, it is evident that the complex impedance plots for $BaTiO_3$-based X7R capacitor chips (supplied by Corning Electronics) always showed two overlapping semicircles, with the lower-frequency one having larger depression angle α. As pointed out by Kleitz et al,[97] the depression angle is usually very small for the intragrain semicircles. This depression of the circle center off the real axis is generally accepted as being due to local inhomogeneity.[98] (It is generally attributed to possible inhomogeneity present within the specimen, so that the statistical distribution of relaxation times is responsible.) This magnitude of the depression angle could be used to differentiate measured semicircles.

From Fig. 35, it is seen that impedance semicircles are reduced with voltage bias, with lower frequency ones more affected. If current conduction mechanism is wholly governed by the grain boundary potential barrier, only grain boundary impedance will be reduced with the applied voltage due to the decrease of the barrier. Since this was not exclusively observed in X7R samples, there

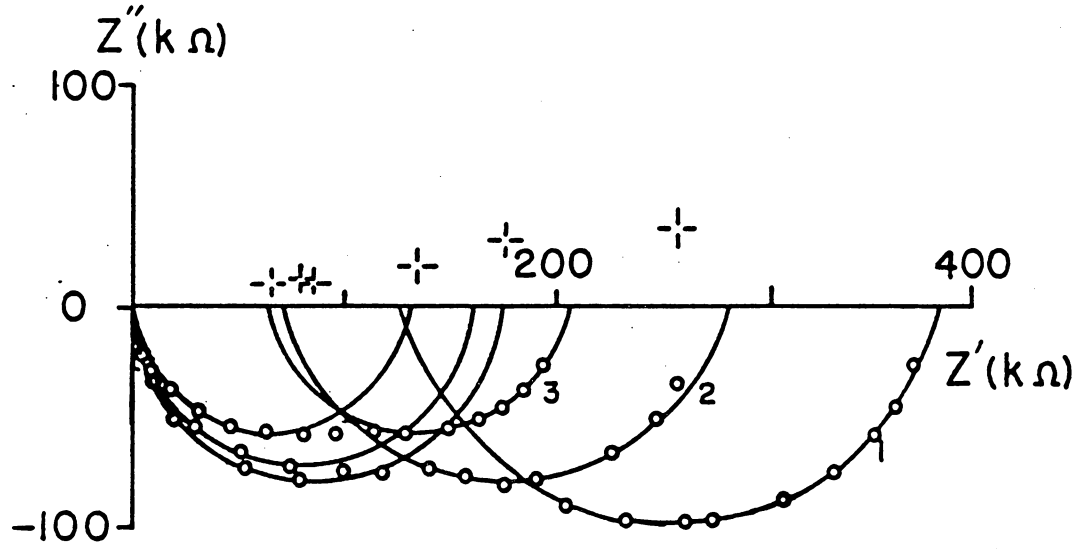

Figure 35. **Complex impedance plots for $BaTiO_3$-based X7R ceramic at different voltage biases at 462.5°C** (thickness = 0.41 mm ; cross points above Z′ denote semicircle centers.)

#1 : Zero bias, #2 : 50V bias, #3 : 100V bias

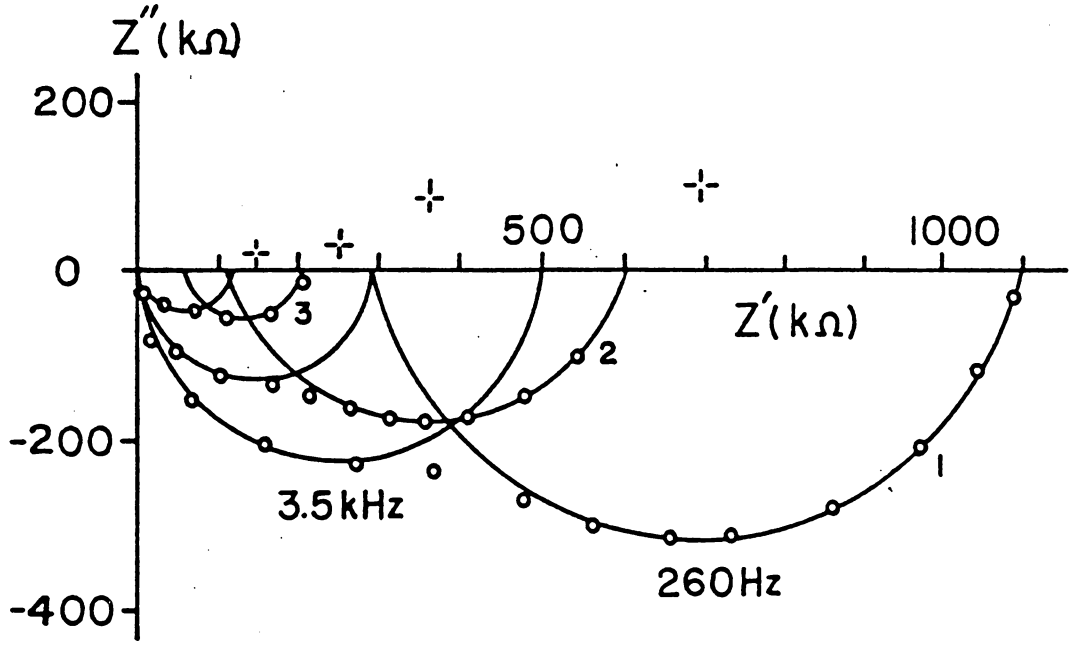

Figure 36. **Complex impedance plots for $BaTiO_3$-based X7R ceramics at 450 °C** (zero biases ; cross points above Z′ denote semicircle centers.)

#1 : 0.69 mm thick, #2 : 0.41 mm thick, #3 : 0.14 mm thick

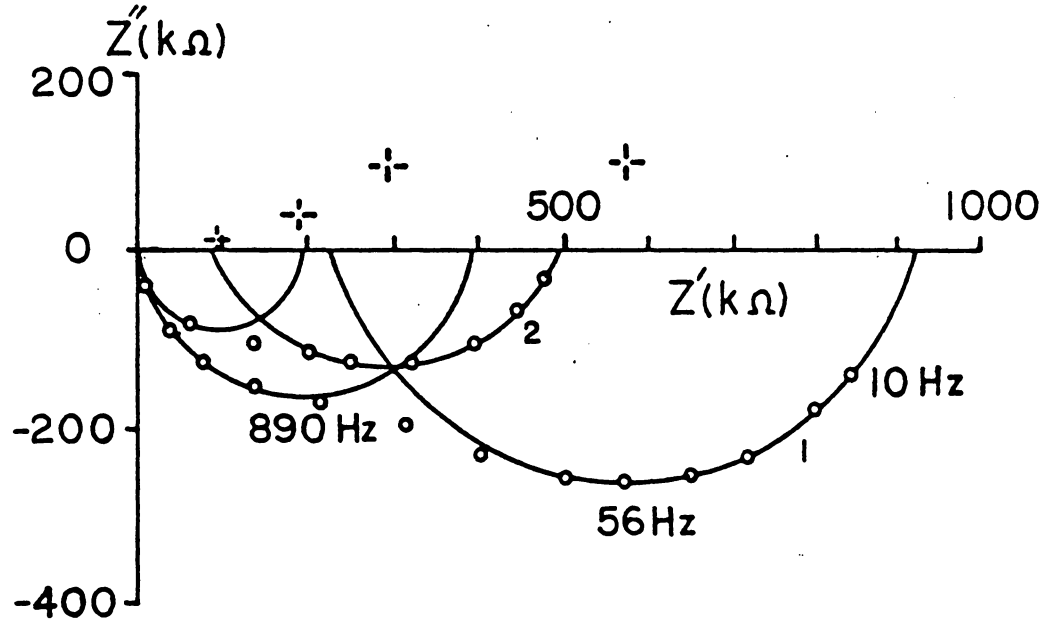

Figure 37. Complex impedance plots for $BaTiO_3$-based X7R ceramic at zero bias (0.14 mm X7R ; cross points above Z′ denote semicircle centers.)

#1 : at 400 °C, #2 : at 425 °C

could be some other possible conduction mechanisms. This will be discussed in detail below. (See Fig. 40, p. 97)

The two semicircles observed for X7R type ceramic were assigned to grain and grain boundaries, where the possibility of electrode effects was ruled out. One reason for the exclusion of electrode effects was that the overall structures of impedance plots for the samples of different thicknesses were all identical. (Fig. 36) Naturally, the shape change (change in the relative magnitude of semicircles) would be expected by changing sample thickness so as to maintain the contact impedance unaffected.

This can be seen from the resistance ratio versus sample thickness values where the ratio of the grain resistance to the grain boundary resistance is virtually constant with thickness. (Table 5) The other reason is because the estimated resistivity values for the samples of different thicknesses are nearly constant. (Tables 4 and 6) This excludes any significant electrode impedance. Now, the problem associated with assigning two semicircles to either grain or grain boundary contribution remains. As mentioned above, the relative magnitude of depression angles can be used as a rule. In all cases, the measured higher-frequency semicircles have very small depression angles, which is an indication of a grain semicircle. Hence, we can identify the existing two semicircles as those of the grain and grain boundary.

Another method used for assigning these semicircles comes from voltage-biased impedance measurements. If grain boundary barrier transmission is assumed to be the dominant current transport mechanism, a reduction of the grain semicircle with voltage bias would not be expected. In other words, voltage bias would only affect the grain boundary semicircle within the superohmic (or SCLC) regime. However, the measured impedance plots for X7R chips show the reduction of both semicircles, with the lower-frequency one (grain boundary semicircle) more strongly affected. If grain impedance is reduced within the superohmic region, the small polaron hopping potential barrier could be effected by voltage. From the resistance versus bias voltage plot, one can find the general trend of decreasing resistance with voltage, with the grain boundary resistance decreasing

Table 5. Resistance ratio versus dc bias voltage for polished X7R samples (R_g/R_{GB})

dc bias voltage	R_g/R_{GB}		
	#1	#2	#3
0 volt	0.58	0.65	0.46
10	0.73	0.71	0.51
20	0.70		
35	0.74	0.69	
50		0.72	0.51
100		0.88	0.61
150			0.47

Note) #1 : 0.14 mm X7R at 450 °C

#2 : 0.41 mm X7R at 462.5 °C

#3 : 0.69 mm X7R at 475 °C

Table 6. **Estimated resistivities from complex impedance plots for polished X7R samples at 450 °C**

chip thickness (mm)	resistivity (Ωcm)
0.14	1.59×10^6
0.21	2.31×10^6
0.41	1.77×10^6
"	1.92×10^6
0.69	1.90×10^6
1.12	2.17×10^6†

† resistivity value for 1.12 mm X7R plate (as-received) was adapted from dc conductivity data for comparison

more rapidly. Therefore, the current transport may be considered to be mixed grain boundary barrier and small polaron hopping transport.

It is evident from Fig. 38, which shows resistances versus inverse temperature, that the activation energies for grain and grain boundary contributions are similar, which may mean that those activation energies for grain boundary barrier transmission and small polaron hopping transport are approximately the same, if they are, indeed, responsible for each curve. The resistance values were deduced from the impedance plots assuming an equivalent circuit as two lumped R-C circuits connected in series. The activation energies of about 1.3 eV are typical for $BaTiO_3$-based material of this type. Another possibility, which may be very important in the transport mechanisms, is that a common mechanism dominates grain and grain boundary transport, if these are the two main modes. The only suitable candidate in this case would be small polaron hopping transport.

One result of a common activation energy is the linearity of the ln I versus 1/T plot over a wide temperature range. (See Fig. 39) Even if the transport mechanism changes over this temperature range, it will not be evident in a ln I versus 1/T plot if two mechanisms have the same activation energies, which is less likely.

There are other reasons that lead one to believe that the grain boundary may not play a significant role in carrier transport for X7R ceramic.

a) Single crystal and ceramic $BaTiO_3$ have similar thermal activation energies E_A, of about 1 to 1.3 eV.

b) Both Corning X7R ceramic, and capacitors, have E_A that are essentially independent of applied voltage. Grain boundary potential barriers are expected to be voltage dependent.[99]

c) $BaTiO_3$-based ceramic resistance has been reported to be independent of grain size, other parameters remaining constant.[100]

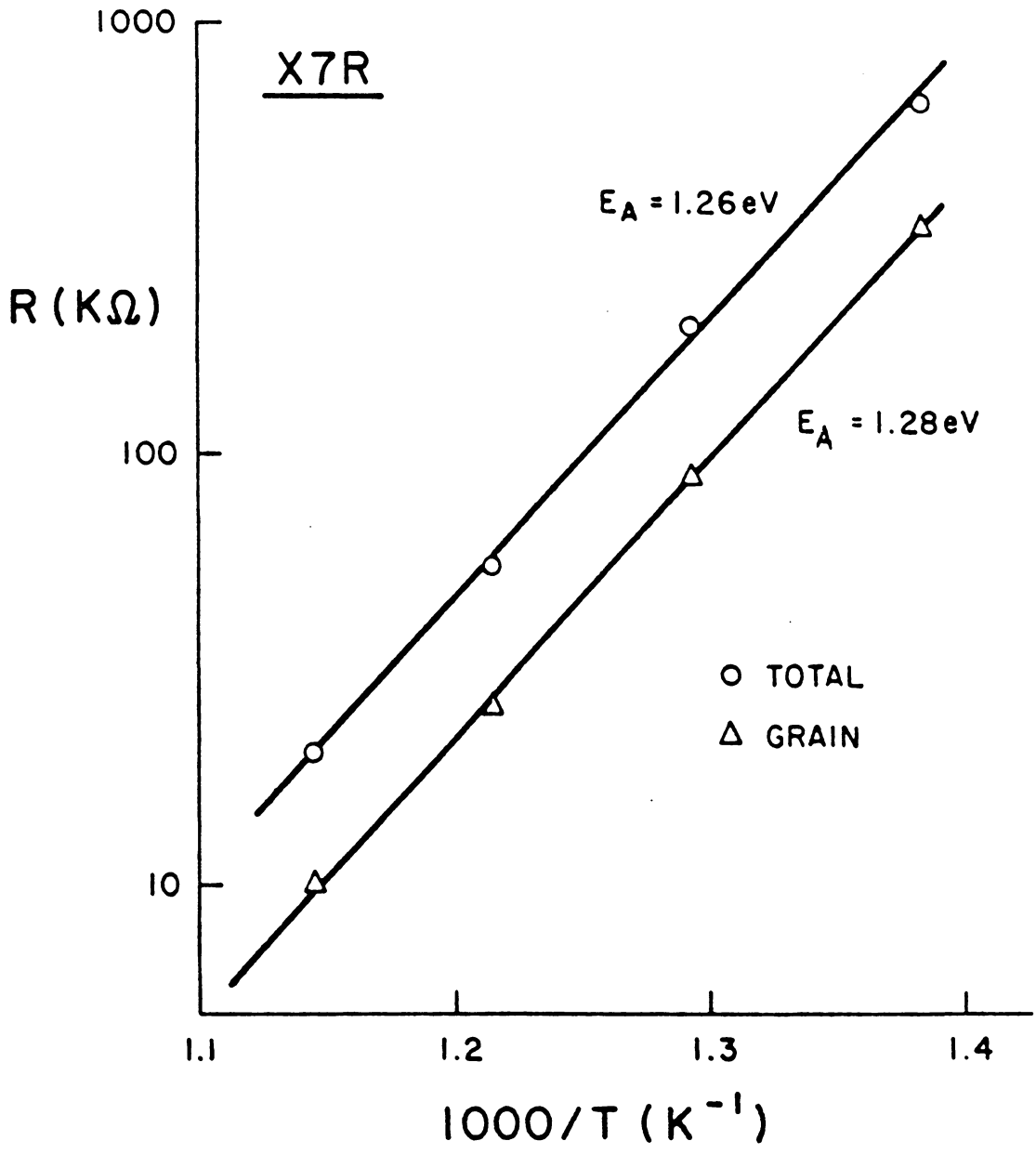

Figure 38. Total and grain resistances obtained from impedance plots versus inverse temperature for as-received X7R plates

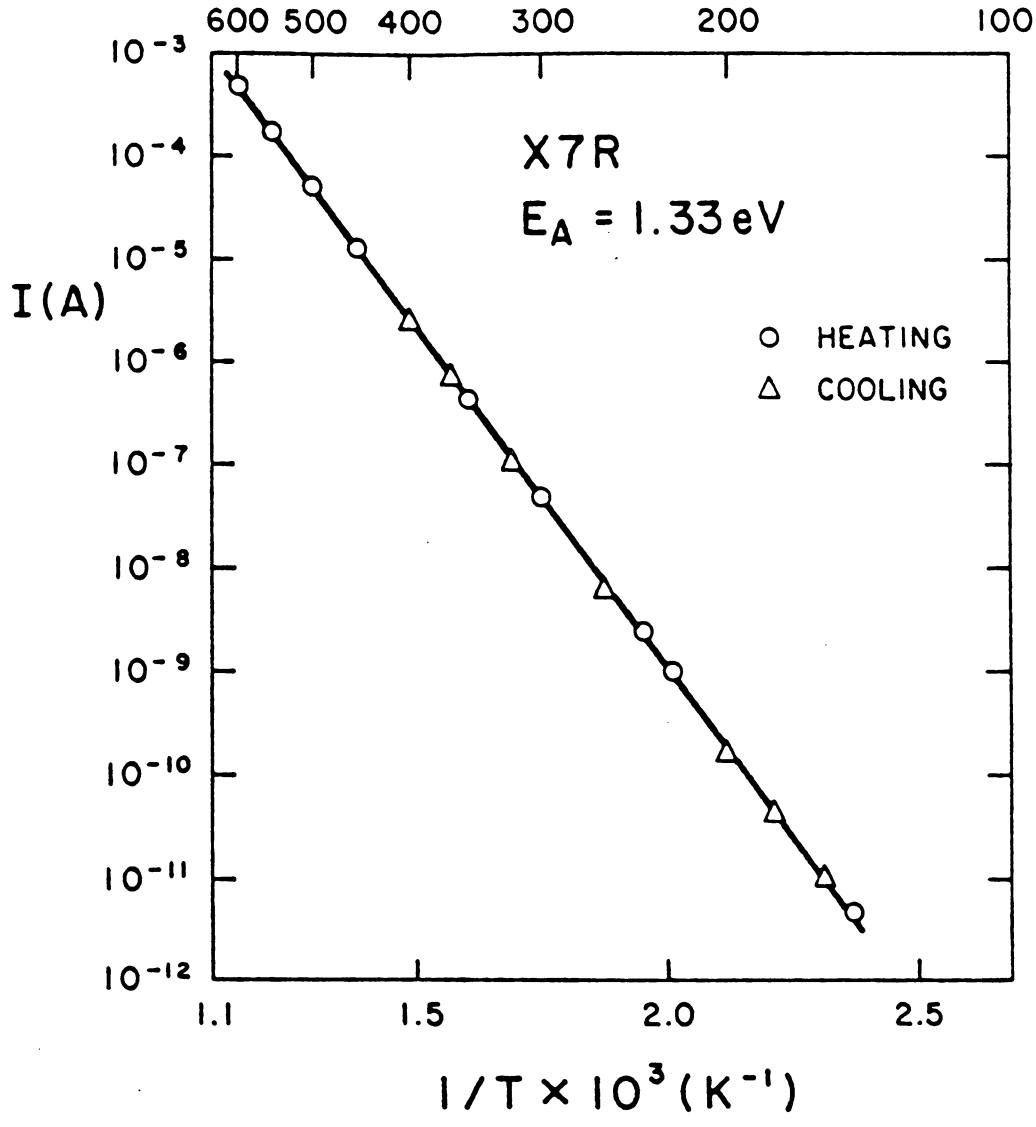

Figure 39. Current versus inverse temperature for as-received X7R plates from 150 °C to 600 °C, at the applied voltage of 10 V

d) The two apparent semicircles of X7R samples result in resistance values having nearly the same E_A (see Fig. 38). This could be coincidental, if one represents polaron transport, the other grain boundary transport. However, it is more likely that they are due to the same mechanism, possibly small polaron hopping.

From the resistance versus bias voltage plot (Fig. 40), one can find that grain resistances are not usually affected below the ohmic-superohmic transition voltage (V_T), whereas grain boundary resistances are gradually decreased with voltage. This verifies the usefulness of dc voltage-biased impedance technique for identifying impedance semicircles. This technique will be useful for further investigations, if we combine this with other measurements, especially for samples of varying grain sizes.

5.4.2 Non-Stoichiometric Barium Titanates

It is interesting to compare the impedance plots of commercial X7R ceramic with those of various $BaTiO_3$ ceramics of known composition. In this section, impedance results for non-stoichiometric barium titanates are presented, and some major points of interests are discussed.

The evidence of grain boundary impedance dependence on stoichiometry for $BaTiO_3$ discs can be seen in Figs. 41 and 42. The existence of grain, grain boundary and contact impedance for the Ba-rich disc at high, mid and low frequencies, respectively is shown in Fig. 42. The Ba-deficient disc shows only one impedance contribution. The difference could arise if the Ba-deficient sample is p-type, because of the high work function of the Pt electrodes,† resulting in low resistance ohmic contact. An interpretation of the grain versus grain boundary contributions from these samples probably depends on knowing relative grain boundary segregation, possibility of a TiO_2 phase.[28]

† Pt electrodes for these non-stoichiometric barium titanates were placed on the samples by Materials Research Laboratory of Penn State University.

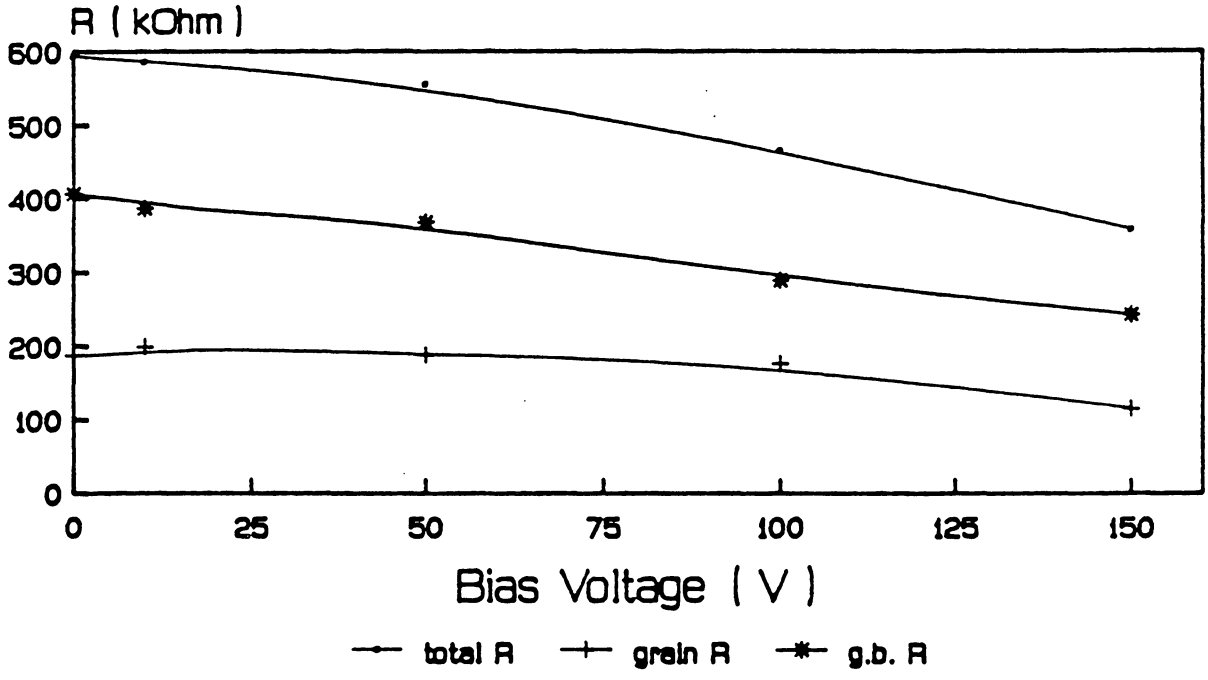

Figure 40. Total, grain boundary, and grain resistances (from top to bottom) versus bias voltage (thickness = 0.69 mm, T = 475°C)

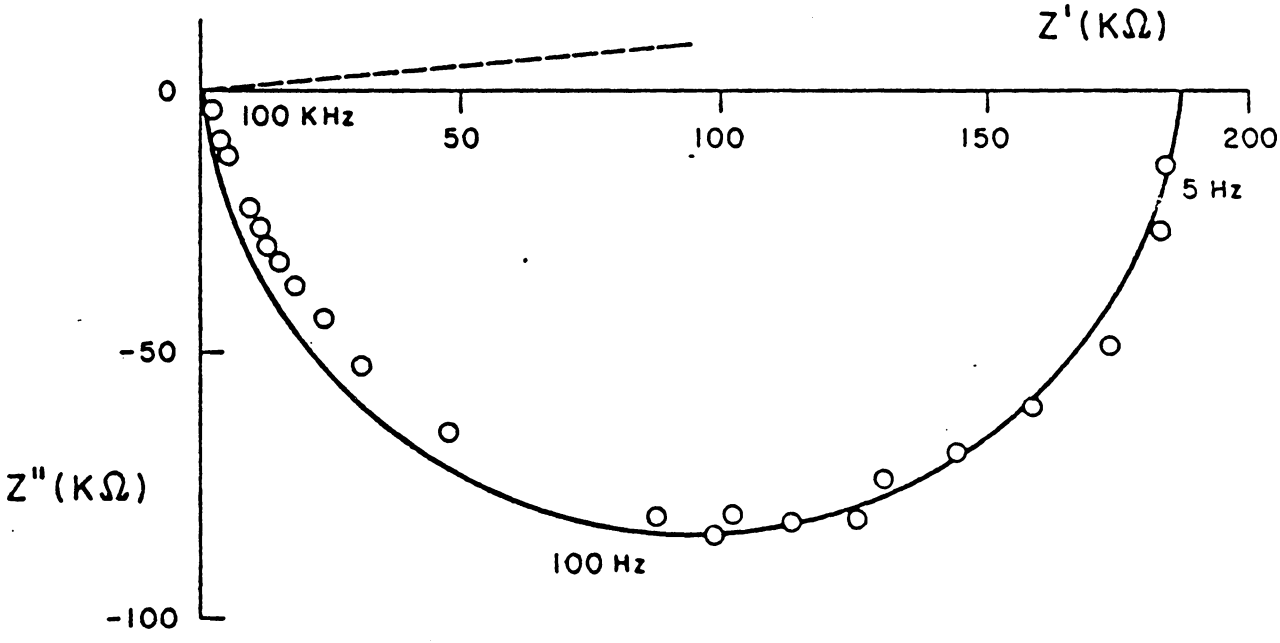

Figure 41. Impedance plot for Ba-deficient titanate ceramic disc at 400 °C ($Ba_{0.99}TiO_{3-x}$)

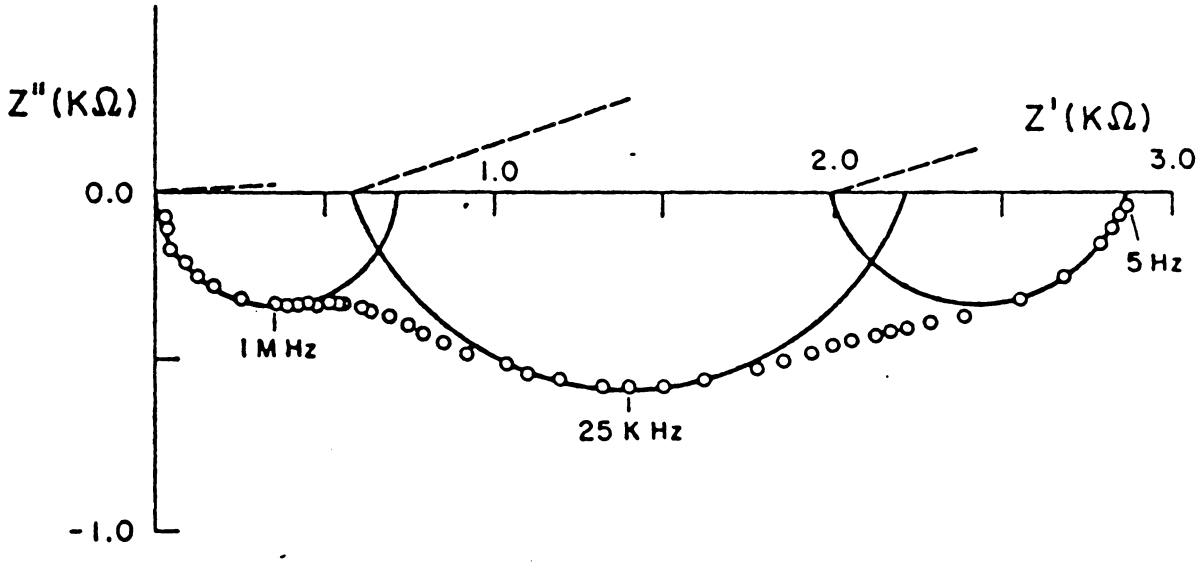

Figure 42. Impedance plot for Ba-rich titanate ceramic disc at 450 °C ($Ba_{1.01}TiO_{3+x}$)

This can be explained by the assumption that the grain tends to have a more stoichiometric structure, which is true in many cases due to defect chemistry of polycrystalline materials.

In summary, the following can be concluded from the complex impedance measurements:

a) Complex impedance plots for polished X7R ceramic give evidence of grain and grain boundary contributions, with none from contacts.

b) Voltage-biased impedance measurements can serve to separate grain, and grain boundary effects.

c) There is evidence of grain, grain boundary, and contact impedance for the Ba-rich disc. The Ba-deficient disc show only one impedance semicircle.

Chapter 6. Conclusions and Recommendations

The main objectives of this research were to examine electrical characteristics of $BaTiO_3$-based ferroelectric X7R capacitors and ceramics, and to address the questions regarding the dominant charge carrier and its mode of transport in these materials, as stated in Chap. 1.

From the results and discussions given in the previous chapter, the following are concluded:

1. For a specific type of commercial $BaTiO_3$-based ferroelectric X7R ceramic, the charge carrier for leakage current is the electron, at temperatures below 850°C. This has been ascertained by several independent results, which were described in detail:

   negative thermoelectric coefficients,

   zero galvanic cell voltages,

   evidence of space-charge-limited currents.

2. Complex impedance measurements proved to be useful in identifying the possible role of grain boundary impedance in dominating current transport mechanisms. The impedance plots for Corning $BaTiO_3$-based ceramic give evidence of grain and grain boundary resistance.

3. $BaTiO_3$-based chip electrical parameters such as resistivity, dielectric constant, and activation energy are independent of chip thickness, indicating that a modified surface region, which is known as a characteristic of ferroelectric materials, and is distinguished from the electrode-ceramic interface, is not important for such samples.

4. Noninternally electroded chips of varying thickness, made from ceramic similar to that of X7R MLC capacitors, exhibit ohmic and superohmic I-V behavior, with only the superohmic one dependent on ambient. The ambient dependence is attributed to changes at the electrode-ceramic interface, not to bulk effects.

5. A viable electical transport mechanisms in X7R ceramic is small polaron hopping.

6. Possible future research related to these topics include the following:

   - Extension of complex impedance measurements to lower temperatures, (This will require improved instrumentation with lower frequency capability and a higher resistance limit.)

   - Complex impedance measurements for samples with different grain sizes, other parameters being kept constant,

   - Extension of both Seebeck measurements and dc conductivity measurements to lower temperatures, in order to quantify transport mechanisms.

   - Extensive study of processing-microstructure-property relationships to obtain better understanding of these variables, leading to optimum property control.

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