Characterization and Application of Wide-Band-Gap Devices for High Frequency Power Conversion

Zhengyang Liu

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Fred C. Lee (Chair)
Qiang Li
Dong S. Ha
Virgilio A. Centeno
Alfred L. Wicks

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Abstract

Advanced power semiconductor devices have consistently proven to be a major force in pushing the progressive development of power conversion technology. The emerging wide-band-gap (WBG) material based power semiconductor devices are considered as gaming changing devices which can exceed the limit of silicon (Si) and be used to pursue groundbreaking high-frequency, high-efficiency, and high-power-density power conversion.

The switching performance of cascode GaN HEMT is studied at first. An accurate behavior-level simulation model is developed with comprehensive consideration of the impacts of parasitics. Then based on the simulation model, detailed loss breakdown and loss mechanism analysis are studied. The cascode GaN HEMT has high turn-on loss due to the reverse recovery charge and junction capacitor charge, and the common source inductance (CSI) of the package; while the turn-off loss is extremely small attributing to unique current source turn off mechanism of the cascode structure.

With this unique feature, the critical conduction mode (CRM) soft switching technique is applied to reduce the dominant turn on loss and significantly increase converter efficiency. The switching frequency is successfully pushed to 5MHz while maintaining high efficiency and good thermal performance.

Traditional packaging method is becoming a bottle neck to fully utilize the advantages of GaN HEMT. So an investigation of the package influence on the cascode GaN HEMT is also conducted. Several critical parasitic inductance are identified, which cause high turn on loss and high parasitic ringing that may lead to device failure. To solve the issue, the stack-die package is proposed to eliminate all critical parasitic inductance, and as a result, reducing turn on loss by half and avoiding potential failure mode of the cascode GaN device effectively.

Utilizing soft switching and enhanced packaging, a GaN-based MHz totem-pole PFC rectifier is demonstrated with 99% peak efficiency and 700 W/in^3 power density. The switching frequency of the PFC is more than ten times higher than the state-of-the-art industry product while it achieves best possible efficiency and power density. Integrated power module and integrated PCB winding coupled inductor are all studied and applied in this PFC.

Furthermore, the technology of soft switching totem-pole PFC is extended to a bidirectional rectifier/inverter design. By using SiC MOSFETs, both operating voltage and power are dramatically increased so that it is successfully applied into a bidirectional on-board charger (OBC) which achieves significantly improved efficiency and power density comparing to the best of industrial practice. In addition, a novel 2-stage system architecture and control strategy are proposed and demonstrated in the OBC system.

As a continued extension, the critical mode based soft switching rectifier/inverter technology is applied to three-phase AC/DC converter. The inherent drawback of critical mode due to variable frequency operation is overcame by the proposed new modulation method with the idea of frequency synchronization. It is the first time that a critical mode based modulation is demonstrated in the most conventional three phase H-bridge AC/DC converter, and with 99% plus efficiency at above 300 kHz switching frequency.

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General Audience Abstract

Power electronics and power conversion are enabling technologies for almost any applications that are powered by electricity. It is very widely used in consumer electronics, household and industrial appliances, automobiles, utilities, infrastructures, and etc. It is essential but at the same time people want it to be invisible. Therefore the development of power electronics is consistently moving toward high efficiency (less and less energy waste), high density (small volume and less weight), high reliability, and low cost.

Thanks to the development of silicon (Si) based semiconductor technology, especially silicon based power semiconductor devices, a great amount of achievements had been made in last three decades. However such high speed progress probably cannot be maintained for any longer since Si-based power devices are approaching their glass ceiling (theoretical limit) of what can be ultimately achieved. That is why people are looking for power devices made with material different than Si but with greater potential.

Gallium Nitride (GaN) and Silicon Carbide (SiC) based power devices are chosen due to its great potential. It is believed to outperform Si-based devices by 2-3 orders which means power converters made with GaN and/or SiC can be even more efficient, smaller and lighter, more

reliable, and of course with less cost. The most important approach to achieve such objective is high switching frequency.

In order to turn the vision into reality, there are a lot of technology barriers in front of us, which in summary are how to understand the device and how to use the device into real applications with efficient high frequency operation.

Therefore the major achievement of this work is comprehensive evaluation of GaN devices, and then demonstration of GaN and SiC in several AC/DC power converters for different applications.

In the evaluation of GaN devices, an accurate simulation model was built and verified. Then based on the assistance of the model, switching loss mechanism is elaborated. The major conclusion is GaN has large turn on loss and very small turn off loss so that soft switching, which at least achieves zero-voltage-switching (ZVS) turn on, is important for GaN.

Packaging related issues are addressed as well including analysis of package impacts on device performance and a new proposal of advanced package. It is very proud to claim that the proposal now are widely used by GaN device manufacturers into their real commercial products.

After the know-how of how to use GaN was built, the potential of GaN was demonstrated in several different applications. The focus of this dissertation is on its application in AC/DC rectifier/inverter. Critical mode based totem-pole rectifier/inverter were built for 1 kW server power, 6.6 kW on board charger, and 25 kW solar inverter. A series of challenges were identified and the corresponding solutions were proposed. Today, the proposed design is becoming a benchmark and many of the industrial people are adopting our technology and applying it into real high performance products

To My Family

And To Whom It May Concern

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Chapter 1. Introduction

1.1 Overview of Wide-Band-Gap (WBG) Power Devices

Recent emerging wide-band-gap power devices, including gallium nitride (GaN) transistors and silicon carbide (SiC) transistors, are expected to be promising candidates for high frequency power conversion techniques. Due to the advantages of the material, the WBG devices have the features of wide band gap, high electron mobility, and high electron velocity [A.1], [A.2]. Thus better figure of merits can be projected for GaN transistors and SiC transistors [A.3]-[A.5] than for the state-of-the-art Si transistors, which allow WBG devices to switch with faster transition speed and lower switching loss. By using WBG devices in a circuit design, the switching frequency can be pushed to more than 10 times higher compared to their Si counterparts, and achieves similar or even higher efficiency. Therefore it is able to achieve high frequency, high efficiency, and high power density power conversion at the same time. WBG devices also have enhanced thermal property compared to Si which means they can operate at high temperature environment that was not a possibility by using Si devices.

Table 1.1. Material properties of Si, SiC, and GaN [A.4]

Parameter	Si	SiC	GaN
Band Gap E_g (eV)	1.12	3.2	3.4
Critical Field E_{crit} (MV/cm)	0.3	3.5	3.3
Electron Mobility μ_n ($cm^2/(V \cdot s)$)	1500	650	990~2000
Permittivity ε_r	11.8	9.7	9

All of these advantages are stemmed from the basic physical properties of the material. Table 1.1 lists four key parameters of Si, SiC, and GaN.

First of all, both SiC devices and GaN devices are classified as WBG devices because the band gap energy E_g of these two materials are significantly higher than Si device. The band gap of a semiconductor material reflects the strength of the chemical bonds between atoms in the lattice. High band gap energy means an electron requires more energy to jump from one site to another site, or saying the lattice structure is more stable. Based on this, power semiconductor devices made of high band gap energy material usually have lower leakage current and higher operating temperature.

For the parameter critical electric field, it is also related to the chemical bonds of the material. Generally speaking the stronger bonds, the higher critical field. Equation 1.1 shows the relationship between breakdown voltage, drift region width, and critical field.

$$V_{BR} = \frac{1}{2} w_{drift} \cdot E_{crit} \tag{1.1}$$

According to this equation, the breakdown voltage is proportional to the width of drift region and the critical field. So for a given breakdown voltage, both SiC and GaN devices have around 10 times narrow drift region compared to Si device.

In order to support this critical field in the region, a certain amount of electrons should be depleted. So a higher critical filed also means higher concentration of carriers in the drift region. Equation 1.2 further shows the relationship, in which q is the charge of an electron, N_D is the total number of electrons, ε_0 and ε_r are vacuum permittivity and relative permittivity of the material respectively.

$$q \cdot N_D = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot E_{crit}}{w_{drift}} \tag{1.2}$$

According to equation 1.2, it is clear that if the electrical field is 10 times higher, and the drift region is 10 times smaller, then the total number of electrons is 100 times comparing SiC and GaN devices to Si device. This is the basis that both SiC and GaN devices has significant better performance than Si device for high frequency power conversion.

The on-state resistance of a device is calculated based on equation (1.3), in which μ_n is the mobility of electrons.

$$R_{\text{on}} = \frac{w_{drift}}{q \cdot N_D \cdot \mu_n} \tag{1.3}$$

Substituting equation 1.1 and 1.2 into 1.3, the on-state resistance is derived as equation 1.4. Then according to this equation, it is very clear that for given breakdown voltage, materials with higher critical field and electron mobility has significantly smaller on-resistance. And Fig. 1.1 [A.2], [A.6] is drawn based on this equation.

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot E_{Crit}^3} \tag{1.4}$$

In Fig. 1.1, the x-axis is breakdown voltage while the y-axis is specific on-resistance. The three solid lines are theoretical limit for Si, SiC, and GaN based on material properties. Si technology has become very mature over last three decades so that the state-of-the-art Si MOSFET is close to its theoretical limit. Recent Si Super Junction MOSFET even outperforms Si's limit. So there is still some margin that the performance of Si device can be continually improved in future.

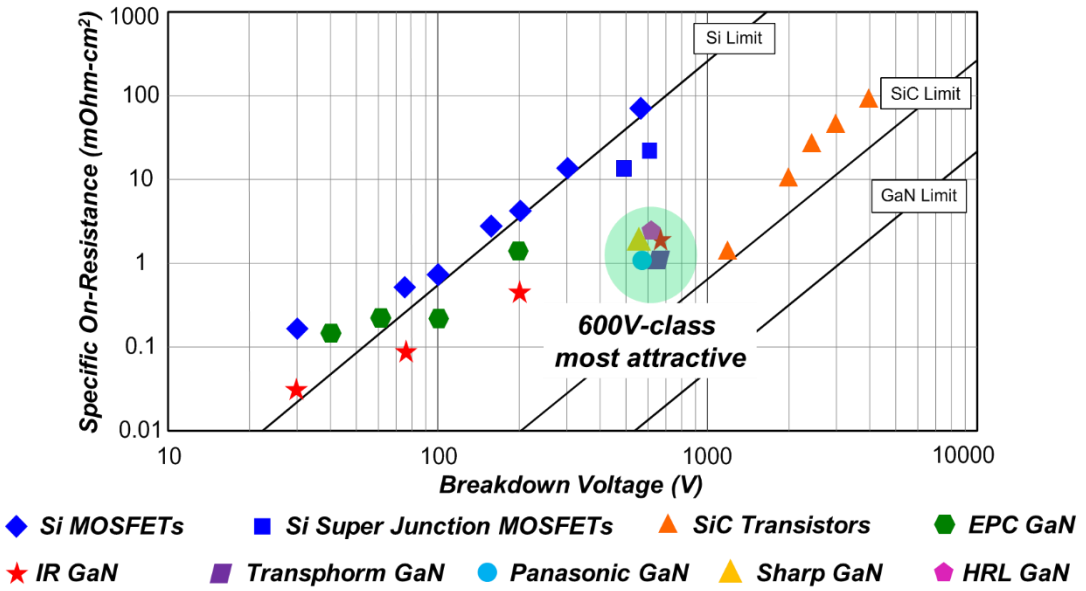


Fig. 1.1. Specific on-resistance vs breakdown voltage for Si, SiC, and GaN

SiC transistors are majorly targeted at high voltage and high temperature application because besides high band gap energy, SiC material also has significantly higher thermal conductivity which makes it ideal for high temperature operation. Generally, the voltage rating of SiC transistors are beyond 1200 V.

Emerging GaN devices have theoretical limit significantly higher than both Si and SiC. Many semiconductor companies recently jump into GaN market and they are marked on the graph as major GaN players. The early stage GaN device is premature so that they just outperform Si MOSFET but far behind its theoretical limit. What is more interesting is many GaN players are simplify focusing on 600V-class devices and it seems that is the most attractive market for GaN at current stage.

The research in this dissertation is focused on characterization and modeling of 600 V GaN devices, and applications of both 600 V GaN devices and 1200 V SiC devices for high frequency power conversion.

1.2 Enhancement Mode GaN vs Depletion Mode GaN

The conductivity of GaN device is based on its piezoelectric property. As shown in Fig. 1.2, by growing a thin layer of AlGaN on top of a GaN layer, a strain is created at the interface between AlGaN and GaN so that high concentration of electrons are induced which is also referred as two-dimensional electron gas (2DEG) [A.4], [A.5]. The electrons in the 2DEG region has high electron mobility and high conductivity, which is the basis of GaN high-electron-mobility transistor (HEMT).

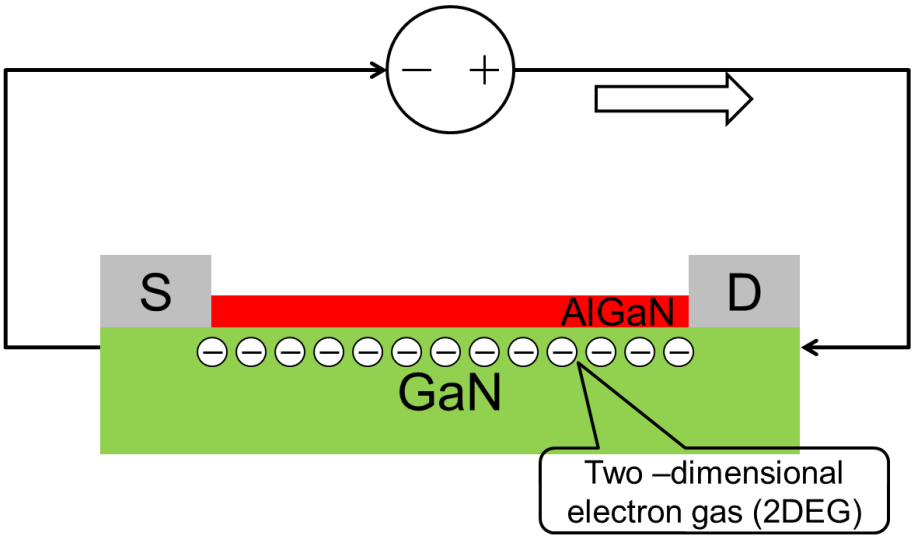
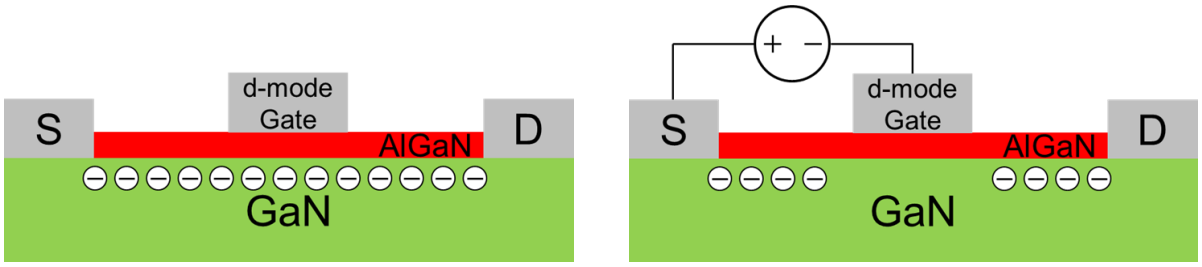


Fig. 1.2. Basic structure of GaN device and its piezoelectric property

Then if an external source is applied between drain terminal and source terminal, the GaN is conducting and current flowing through the channel of GaN device.

To control the on/off state of GaN device, a gate electrode is applied. According to different structures of the gate terminal, GaN device can be divided into two categories, depletion mode GaN device and enhancement mode GaN device.

The depletion mode GaN is more natural according to its piezoelectric property. With a simple d-mode gate electrode, the device is naturally conductive if no voltage is applied between gate and source. To turn off the device, a negative Vgs is applied so that the electrons under the gate area is depleted. The depletion mode GaN device is also named normally-on GaN device.

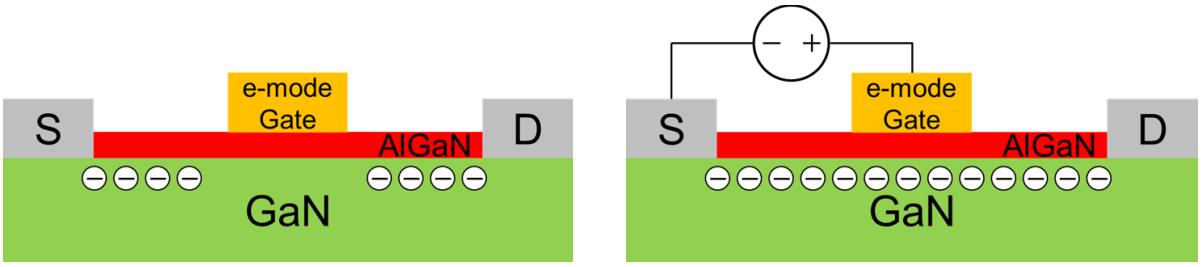


(a) (b)

Fig. 1.3. Basic structure of depletion mode GaN device, (a) on state, (b) off state

With a more complicated process, an e-mode gate can also be made on the GaN device. Different with the depletion mode GaN device, the enhancement mode GaN device is in off state if no external Vgs applied, while a positive Vgs is in need to turn on the enhancement mode GaN device.

Usually there are three popular structures have been used to create the e-mode gate including recessed gate, implanted gate, and pGaN gate.



(a) (b)

Fig. 1.4. Basic structure of enhancement mode GaN device, (a) off state, and (b) on state

To further compare depletion mode GaN device versus enhancement mode GaN device, the four quadrants I-V characteristics are plotted (based on simulation models) in Fig. 1.5 and Fig. 1.6.

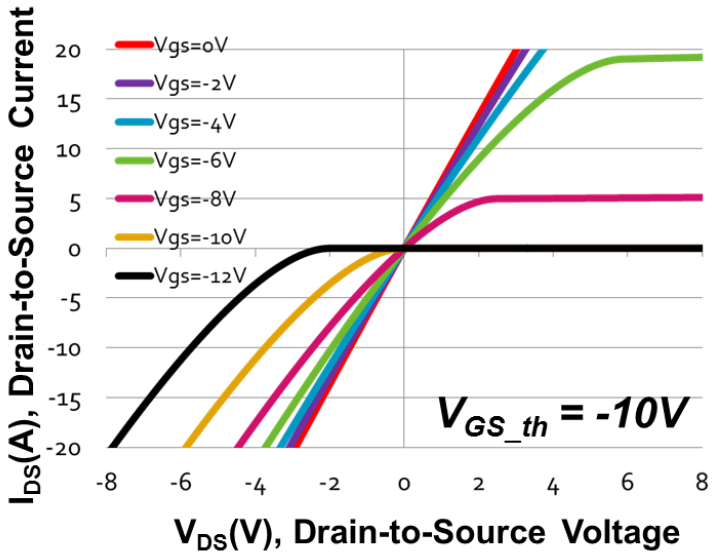


Fig. 1.5. I-V characteristics of depletion mode GaN

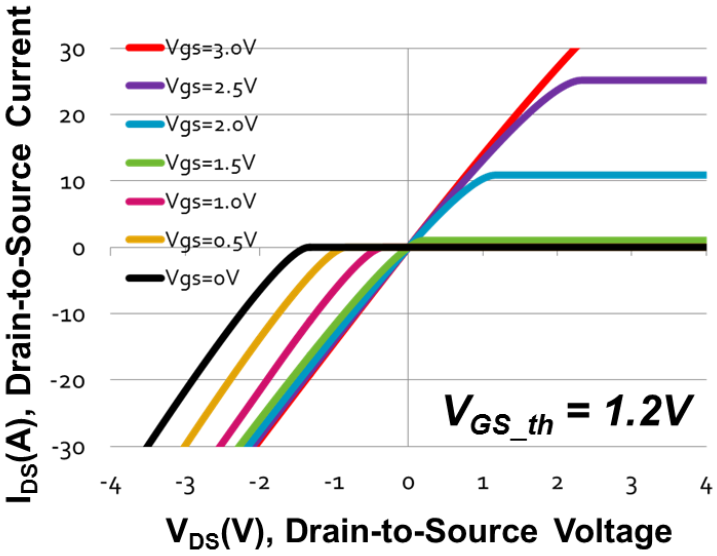


Fig. 1.6. I-V characteristics of enhancement mode GaN

The patterns of both four quadrant I-V family curves are similar while the major difference is the Vgs applied on each curve. For the depletion mode GaN device in this example, the threshold voltage is -10 V so that device is fully turned-on when Vgs equals 0 V while negative voltage is applied like -12 V to turn it off. In comparison, for the enhancement mode GaN device, the threshold voltage is positive like 1.2 V in this case, so that device is in off state when Vgs is equal to 0 V while positive voltage is in need like 3 V to fully enhance the channel.

Another similarity can also be observed from both the I-V family curves which is the reverse conduction mode. For traditional Si power MOSFET, there is a built-in body diode from source terminal to drain terminal so that if a positive voltage is applied on Vsd, the device can conduct without Vgs applied, and in this scenario, the device behaves like a diode. For the power GaN HEMT, it doesn't have a body diode. However, it is in a lateral structure and symmetric from both source side and drain side. This feature offers a reverse conduction capability in a very different mechanism compared to Si MOSFET. Since the GaN HEMT is lateral and symmetric, then a voltage higher than threshold voltage applied on either gate-to-source or gate-to-drain can turn on the device. As a result, in the third quadrant of the I-V family curve, the device can conduct when Vgd is higher than the threshold voltage. Take the enhancement mode GaN as an example, the black curve which is the I-V characteristic when Vgs equals 0 V. So In the first quadrant, it maintains off state before avalanche breakdown. In the third quadrant, the device start to conduct when Vds is lower than -1.2 V. The reason is when Vds equals -1.2 V, and Vgs equals 0 V, then Vgd is equal to 1.2 V which is just the threshold voltage. So further decreasing Vds will finally fully turn on the device with a positive Vgd driving voltage.

Similar reverse conduction mechanism is observed in the depletion mode GaN device. For example, the black curve is for Vgs equals -12 V condition. Then when Vds is lower than -2 V,

the Vgd is higher then -10 V which is the threshold voltage of the normally-on GaN device, so that it starts to conduct when further decreasing Vds.

The issue of this reverse conduction mode is it doesn't like a diode characteristic during conducting when current increases a lot the voltage drop increases a little, but more like a resistor with negative bias voltage. When applied the GaN device into circuit design, reverse conduction with off state Vgs, like the synchronous rectifier in dead time, leads to significantly higher conduction loss compared to Si MOSFET body diode conduction.

The solution to solve this issue is discussed in paper [A.7], [A.8], paralleling diode or fine tuning dead-time are two effective methods.

1.3 Characteristics of 600V Cascode GaN HEMT

Even the processing of the depletion mode GaN device is simpler than the enhancement mode GaN device, normally-on property is usually not preferred in application because firstly the driver design for normally-on device is more complicated since negative voltage is used; secondly there might be shoot-through risk during start-up and other abnormal situations.

To solve this issue but still utilizing the depletion mode GaN device, the cascode structure, as shown in Fig. 1.7, is widely used in most depletion mode GaN devices to make it like a normally-off device.

In the cascode structure, the depletion mode GaN is in series with a Si MOSFET. With this configuration, the gate-to-source voltage of GaN equals to the source-to-drain voltage of Si. So the Si MOSFET is used to control the on and off states of the GaN HEMT.

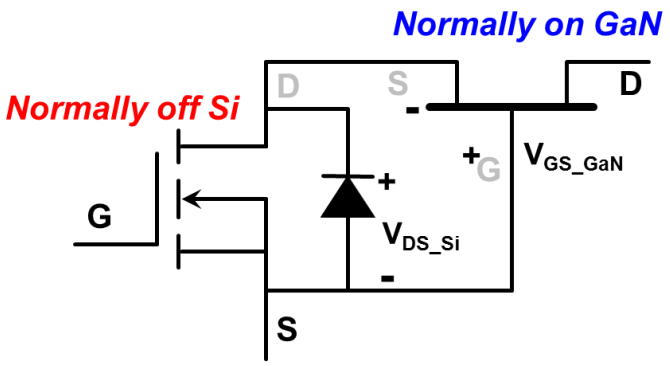


Fig. 1.7. Cascode structure for depletion mode GaN

In addition to drive GaN, the Si MOSFET also offers protection to avoid GaN gate breakdown. For example, for a 600 V depletion mode GaN, the threshold voltage is -22 V while the gate breakdown voltage is -35 V. Then a 30 V Si MOSFET is used in this cascode structure. On one hand, a 30 V MOSFET can make sure to turn off the GaN HEMT effectively while leaving some margin between the threshold voltage and fully turn-off voltage so that it is not easy to false turn on the GaN HEMT and there is enough voltage difference to turn-off the GaN HEMT quickly. On the other hand, the 30 V breakdown voltage provides some margin so that even at extreme case the Vds of Si MOSFET increases quickly but can still be clamped at 30 V through avalanche breakdown mechanism. Then the Vgs of GaN HEMT won't see voltage undershoot lower than -35 V in steady state.

One side effect of the cascode structure is that the Si MOSFET adds extra on-state resistance to the cascode device. Therefore the cascode structure is not suitable for low voltage device, like in a 40 V cascode device, the Si MOSFET could contribute more than 40% total on resistance, while this rate is reduced to below 5% in 600 V device.

In future, the on resistance of Si will only reduce in a limited range because Si technology is pretty mature, while the on resistance of GaN is likely to reduce dramatically since the GaN

technology has large room to improve. Then it can be predicted that the low voltage MOSFET occupies a larger percentage of on resistance with continued improvement on GaN.

Considering this reason, the cascode structure is not practical in low voltage device. So far the cascode structure are only adopted in 600V-class GaN HEMT.

Table 1.2. Driving characteristics of e-mode GaN and cascode d-mode GaN

	E-mode GaN			Cascode D-mode GaN		
Manufacturer	**EPC**	**HRL**	**Panasonic**	**IR**	**Sharp**	**Transphorm**
V_{GS_Max}(V)	**-5~6**	**0~3.3**	**-10~4.5**	**±20**	**±30**	**±18**
Recommended Gate Voltage (V)	**4.5**	**3**	**3.2**	**6**	**10**	**10**
V_{TH}(V)	**1.4**	**0.6**	**1.2**	**2**	**3.5**	**1.8**

The enhancement mode GaN device has many advantages like simple structure, simple packaging, no body diode reverse recovery effect, and no extra on resistance from Si MOSFET. However, the gate drive design is very critical for today's enhancement mode GaN device. A few examples are listed in Table 1.2 which shows that the device fully enhanced gate drive voltage is very close to the breakdown voltage of the gate. The safety margin is usually limited.

On the contrary, the gate drive design for the cascode GaN device is relatively simpler. Since the driving voltage is directly applied on the low voltage Si MOSFET, many commercial gate driver for Si MOSFET is compatible for the cascode GaN device. However there are quite a few special issues related to the cascade GaN device which will be illustrated in this dissertation.

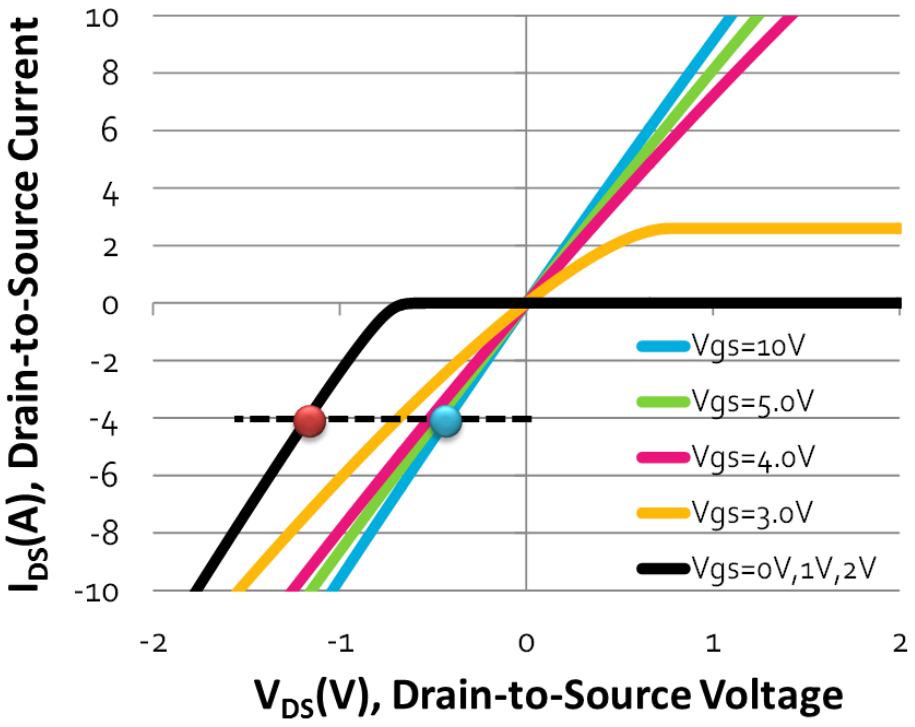
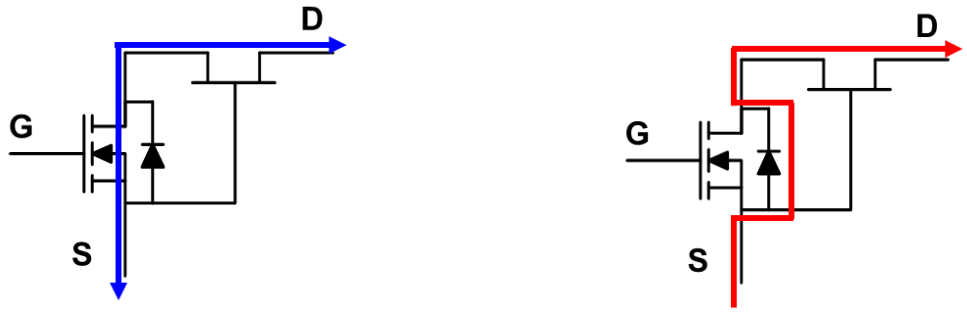


Fig. 1.8. I-V characteristics of cascode GaN HEMT

The I-V characteristics and conduction principle of the cascode GaN HEMT is shown Fig. 1.8 and Fig. 1.9. When 10 V gate drive voltage is applied, the Si MOSFET is fully enhanced. Since the on resistance of the 30 V Si MOSFET is very small (10 mOhm level), so the gate drive voltage applied on the depletion mode GaN HEMT is close to zero and the GaN HEMT is fully enhanced. In this conduction mode, the current flows through both the channel of the Si MOSFET and the channel of the GaN HEMT, so that the voltage drop equals to equation (1.5). The current can be bidirectional and it is symmetric in the first quadrant and the third quadrant (as the blue curve in Fig. 1.8). In this condition, since the on resistance of the 30 V Si MOSFET is much smaller than that of the 600V GaN HEMT, the total voltage drop is dominated by the GaN HEMT.



(a) (b)

Fig. 1.9. Conduction principle of cascode GaN HEMT, (a) Vgs=10V, (b) Vgs=0V

$$V_{DS} = I_{DS} \cdot (R_{ds\_GaN} + R_{ds\_Si}) \tag{1.5}$$

When the Si MOSFET is turned off by applying 0 V driving voltage, the cascode GaN HEMT is blocking in the first quadrant while still conducting in the third quadrant. The current first goes through the body diode of the Si MOSFET. Then the gate-to-source voltage of the GaN HEMT equals to the forward voltage of the body diode which makes it in on state. So the current also goes through the channel of the GaN HEMT like shown in Fig. 1.9(b). In reverse conduction mode, the voltage drop equals to equation (1.6) and is shown as the black curve in Fig. 1.8.

$$V_{SD} = I_{SD} \cdot R_{ds\_GaN} + V_{bd} \tag{1.6}$$

Comparing the two reverse conduction modes in the third quadrant, the current of the second going through the body diode has significantly high voltage drop and also high conduction loss. For example, as the red dot and blue dot marked in Fig. 1.8, given the same 4 A current, the voltage drop of the red dot is about twice the voltage drop of the blue dot, which means the conduction loss is almost doubled.

The reverse conduction modes are common if the cascode GaN HEMT is used as a synchronous rectifier or in a current bidirectional flowing converter. During dead time, the cascode GaN HEMT has significantly higher conduction loss compared to traditional Si MOSFET. So the dead time control is more critical for the cascode GaN HEMT than for Si MOSFET in order to avoid the high dead time loss.

Finally, when comparing the 600V GaN HEMT with the state-of-the-art Si MOSFET, dramatically performance improvement can be projected. Table 1.3 shows several key parameters comparison. Two devices have similar breakdown voltage and on resistance. Dynamic parameters and reverse operation parameters are compared. The total gate charge Q_g of GaN is smaller than one tenth of Si, which can translate to significantly smaller driving loss. The Q_{gd} of GaN, also known as the miller charge, is smaller than one fifteenth compared to Si so that much smaller voltage and current transition switching loss can be projected. Similarly, smaller E_{oss} means smaller CV^2 loss is hard switching turn on; smaller Q_{oss} means less resonant time, smaller duty cycle loss, and smaller root-mean-square (RMS) current in a resonant converter, so that smaller conduction loss on both power devices and other passive components. Last but not least, as the depletion GaN HEMT itself doesn't have body diode, so only the low voltage Si MOSFET contributes a smaller reverse recovery charge, the related revere recovery loss for the cascode GaN HEMT is also dramatically smaller than the Si MOSFET. All of the benefits indicate that the cascode GaN HEMT is superior for high frequency power conversion.

Table 1.3. Key parameter comparison between cascode GaN vs state-of-the-art Si

Parameter		GaN HEMT	State-of-the-art Si MOSFET
Static	V_{DS}	600V	600V
	R_{DS}	0.15Ω/0.18Ω[1]	0.14Ω/0.16Ω[1]
Dynamic	Q_g	6.2nC[2]	75nC[3]
	Q_{gd}	2.2nC[2]	38nC[3]
	E_{oss}	6uJ[4]	11uJ[4]
	Q_{oss}	28nC[4]	130nC[4]
Reverse Operation	Q_{rr}	42nC[5]	8200nC[6]
	t_{rr}	24ns[5]	460ns[6]

[1] T_j=25°C; [2] V_{GS}=0-4.5V, V_{DS}=100V, I_D=12A; [3] V_{GS}=0-10V, V_{DS}=480V, I_D=11.3A;
[4] V_{GS}=0V, V_{DS}=0-400V; [5] V_{DS}=480V, I_{DS}=9A, di/dt=450A/us; [6] V_{DS}=400V, I_{DS}=11.3A, i/dt=100A/us;

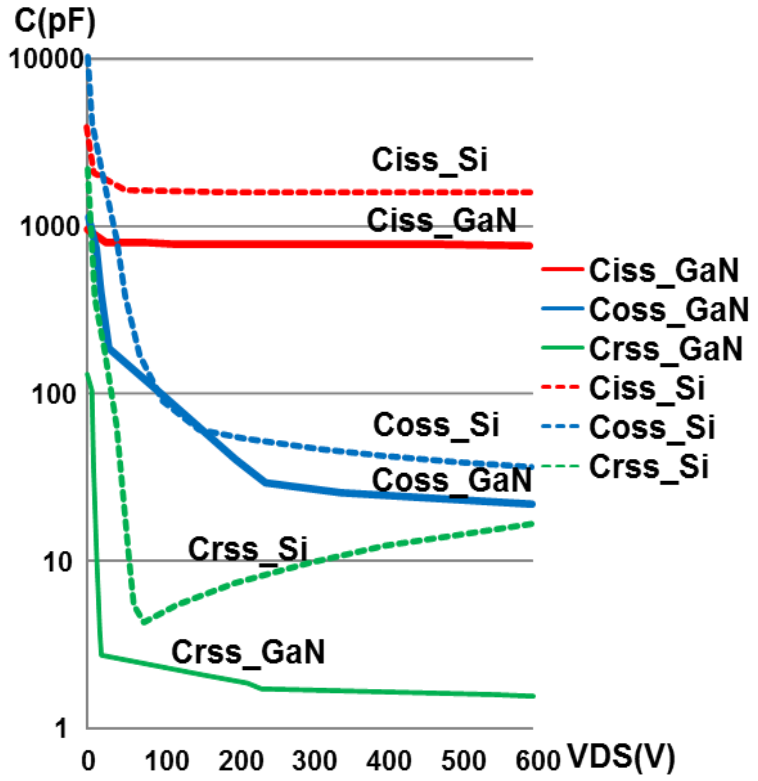


Fig. 1.10. C-V characteristics comparison between cascode GaN and state-of-the-art Si

Fig. 1.10 further compares the non-linear C-V characteristics of the GaN HEMT and the Si MOSFET, which clearly indicates that for all of the three parasitic capacitances (input capacitance

C_{iss}, output capacitance C_{oss}, and miller capacitance C_{rss}) the GaN HEMT are much smaller than the Si MOSFET. Particularly, the non-linearity of Si MOSFET is more prominent so that the capacitance in low voltage is usually tens of times larger than the capacitance in high voltage. The strong non-linear property further makes Si MOSFET longer turn-on and turn-off delay time and voltage/current rising/falling transition time. Consequently, it is even harder for Si MOSFET to be used in MHz high frequency. As a comparison, the non-linearity of the GaN HEMT parasitic capacitor is much alleviated so that switching transition can be finished significantly faster than the Si MOSFET.

1.4 Proposed Dissertation Outline

As both GaN devices and SiC devices are expected to be game changers, the dissertation would start from evaluation and characterization of 600 V GaN devices, modeling and packaging; then a series of soft switching AC/DC converters are demonstrated with GaN devices for low power applications and SiC devices for medium power applications.

The proposed dissertation outline is:

Chapter 1. Introduction

1.1 Overview of Wide-Band-Gap (WBG) Power Devices

1.2 Enhancement Mode GaN vs Depletion Mode GaN

1.3 Characteristics of 600V Cascode GaN HEMT

1.4 Proposed Dissertation Outline

Chapter 2. Characterization and Modeling of GaN Device

2.1 Package Parasitics Extraction and Simulation Model Development

Chapter 2. Characterization and Modeling of GaN Device

Through the comparison between GaN HEMT and Si MOSFET with similar breakdown voltage and on resistance, the dynamic parameters of GaN HEMT are far better than its Si counterpart. Therefore GaN HEMT is expected to achieve good efficiency at significantly higher switching frequency compared to Si.

A buck converter is built to evaluate GaN HEMT as shown in Fig. 2.1. Transphorm cascode GaN is used in this test circuit. The buck converter is operated at continuous conduction mode (CCM) which is the most straightforward operation mode in hard switching.

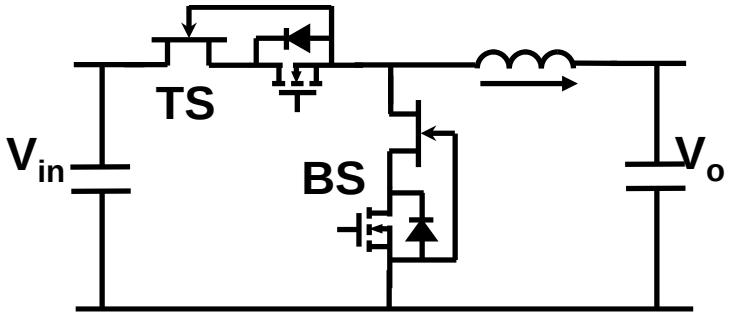


Fig. 2.1. Buck converter test circuit (CCM, V_{in}=380V, V_o=200V, I_{o_full}=6A, I_{ripple_p2p}=3A)

The tested efficiency is shown is Fig. 2.2. Although 99% efficiency is achieved at 100 kHz, the efficiency drops quickly as the switching frequency is pushed to 300 kHz and 500 kHz. This trend clearly indicates that a large portion of switching related loss existing. The turn-on waveform at full load condition is shown in Fig. 2.3 in which significant parasitic ringing are observed.

The test results are different from intuitive expectation since switching loss and parasitic issue are not significantly reduced by much improved dynamic parameters. In order to investigate the insight of switching behavior and switching loss mechanism, accurate simulation model is required.

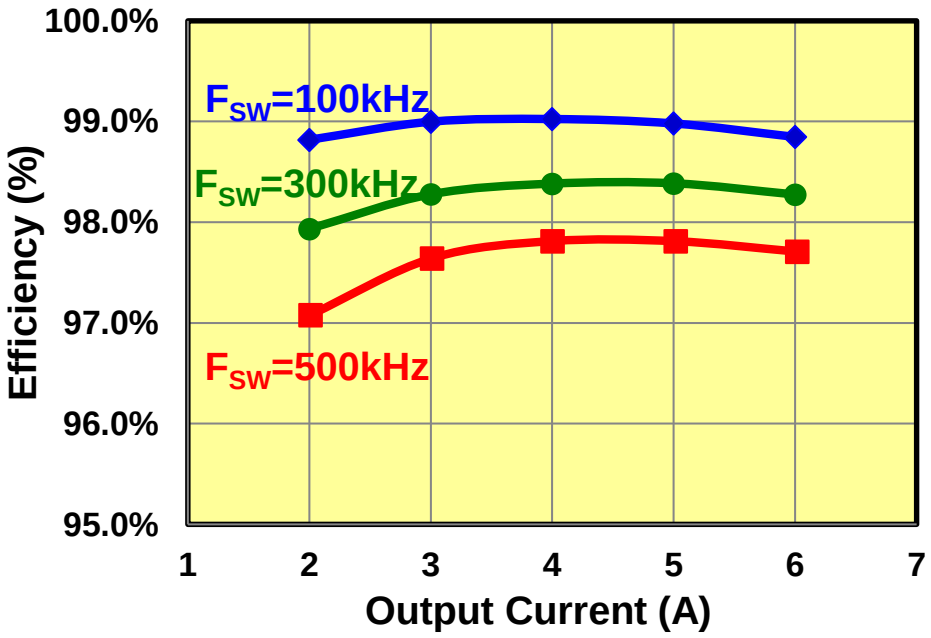


Fig. 2.2. Tested efficiency of buck converter at different switching frequency

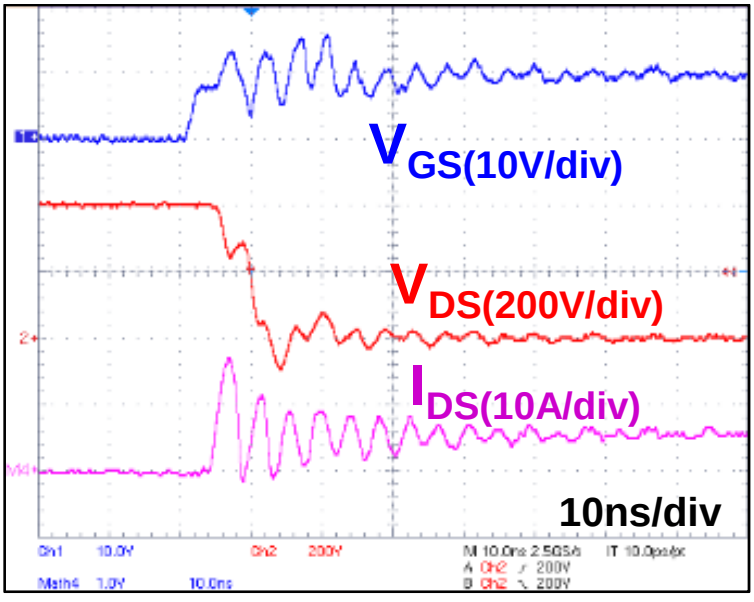
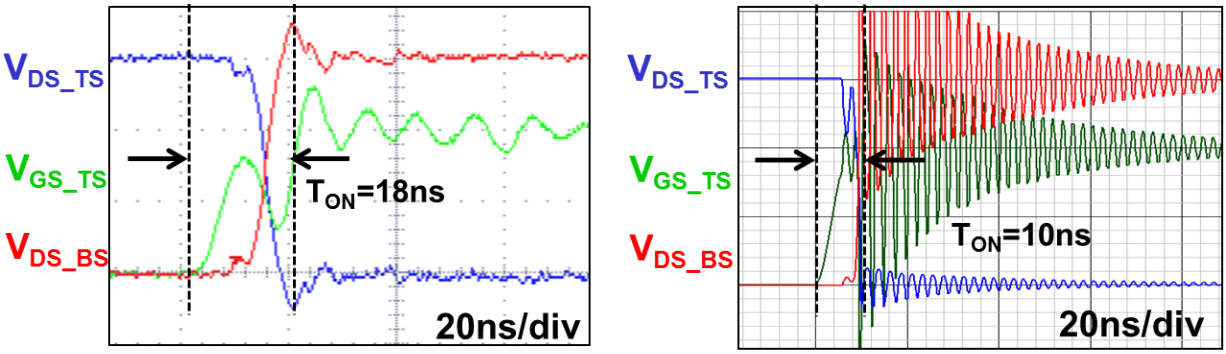


Fig. 2.3. Tested turn-on waveform at 380V/5A

2.1 Package Parasitics Extraction and Simulation Model Development

A SPICE (Simulation Program with Integrated Circuit Emphasis) based behavior-level simulation model is initially provided by the device manufacturer. SIMetrix is used for conducting the circuit simulation.

When the simulation model is first applied into a buck converter, the original simulation waveform doesn't match with the experimental waveform like shown in Fig. 2.4.

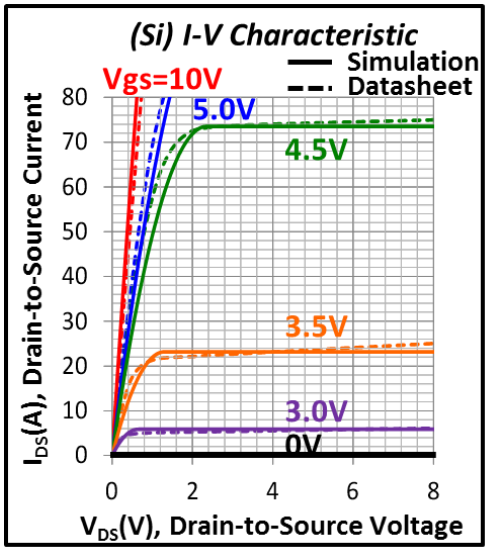


(a) (b)

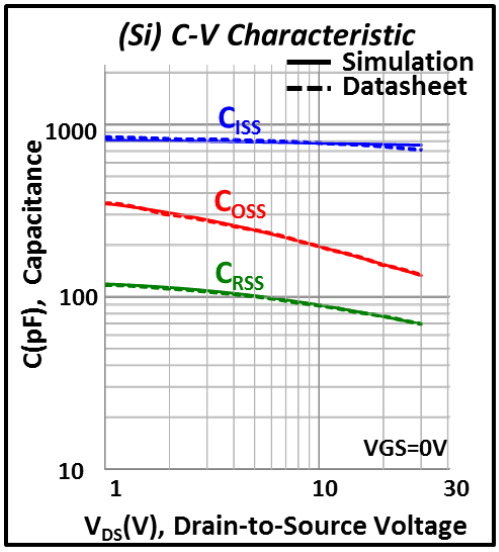
Fig. 2.4. (a) Experimental waveform and (b) simulation waveform comparison

In simulation, the delay time, rising and falling slopes, and transition time don't match with the experiment. The parasitic ringing in simulation is excessive with mismatched amplitude, frequency and damping effect. All of the mismatches make it unable to predict the GaN HEMT's switching performance in good accuracy.

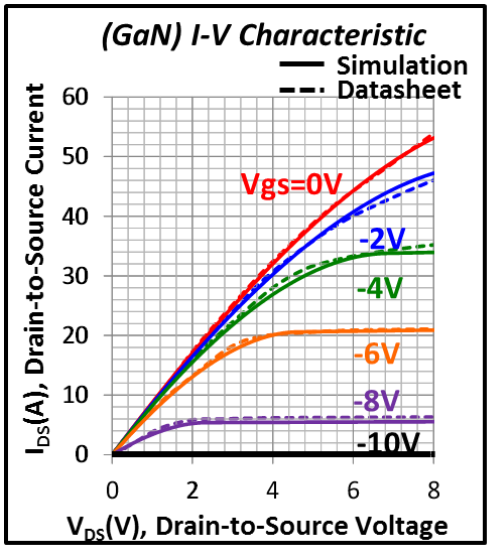
The simulation model modification starts from the basic characteristics of the device. In order to make it more clear, the lumped SPICE code is separated into two independent model so that the Si MOSFET and GaN HEMT can be evaluated separately.



(a)



(b)

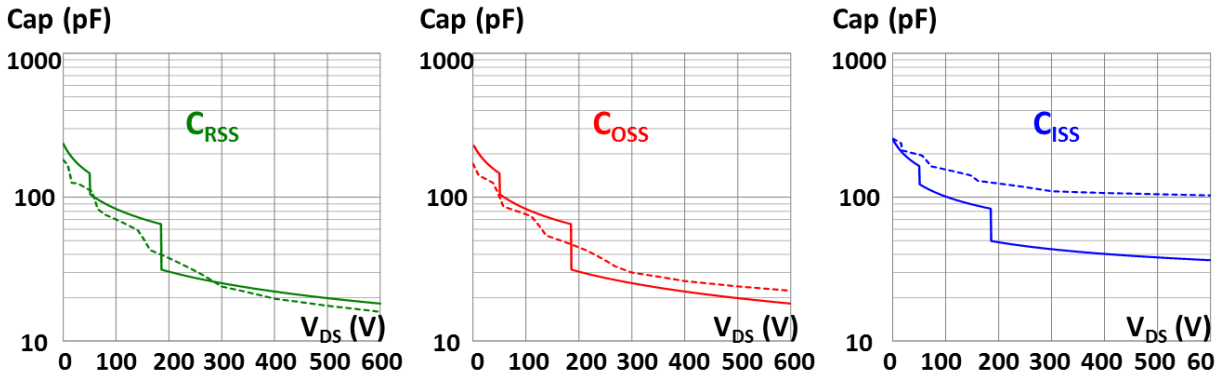


(c)

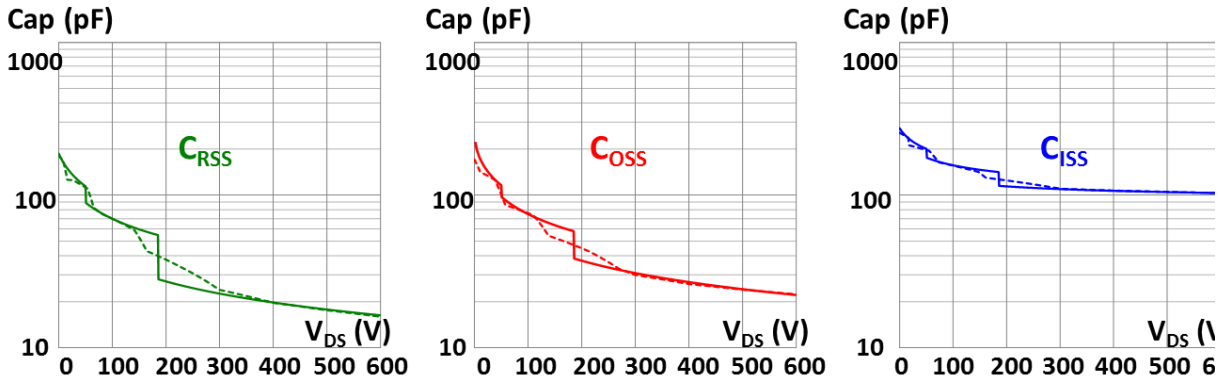
Fig. 2.5. Simulation model verification (a) I-V of Si MOSFET, (b) C-V of Si MOSFET, and (c) I-V of GaN HEMT

Fig. 2.5. is the I-V characteristic and the C-V characteristic of the Si MOSFET, and the I-V characteristic of the GaN HEMT. The accuracy is verified by comparing the simulated curves with measurements or datasheets.

The first mismatch is found in the C-V characteristic of the GaN HEMT as shown in Fig. 2.6. All of the three most important non-linear parasitic capacitance is closer to the datasheet after proper modification on the initial value and non-linearity coefficient.



(a)



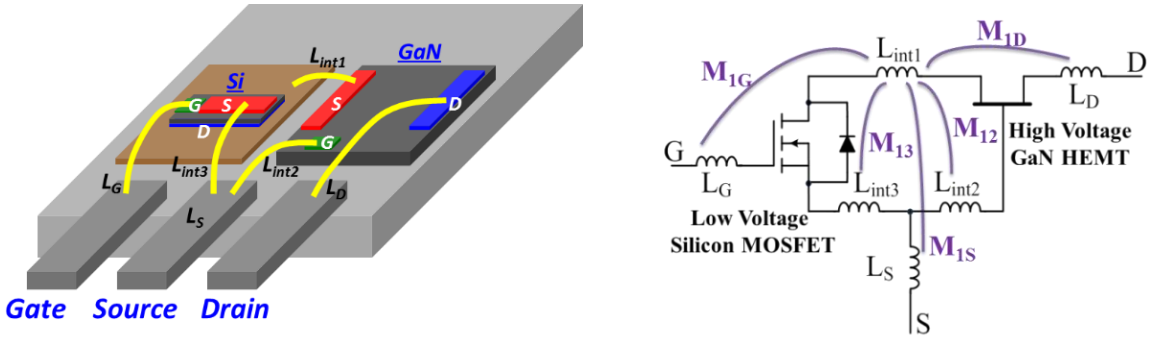
(b)

Fig. 2.6. C-V characteristic (a) before modification and (b) after modification. (solid line is from simulation, dashed line is from datasheet, all curves are obtained under V_{GS}=-24V)

Besides the not accurate C-V curves, another important issue is the simulation model lacks accurate package parasitic inductance, which is of major importance to describe the dynamic characteristic of the device.

Fig. 2.7 shows the typical bonding diagram of the cascode GaN HEMT in a traditional TO-220 package and its corresponding schematic. Inside the cascode package, the 600V depletion mode GaN die is on the right hand side of the lead frame, while the 30V Si MOSFET die is on the left hand side of the lead frame and mounted on a direct-bond-copper (DBC) substrate. Wire bonding process is used to achieve necessary electric connections.

According to Fig. 2.7 (b), it is clearly that many parasitic inductors are introduced due to the inter-connections between the GaN die and the Si die, and between the dies and the lead frame. Moreover, as the currents with fast transitions are confined in such a small area, the coupling effects between different conductors are significant. The mutual inductances of L_{int1} with the other inductors are labeled in Fig. 2.7 (b).



(a) (b)

Fig. 2.7. TO-220 cascode GaN HEMT package (a) bonding diagram and (b) schematic

The extraction of package parasitic inductance is implemented by Ansoft Q3D Extractor FEA simulation. According to electromagnetic theory, many parameters, like the dimensions, the positions, and the current directions of the conductors, have a significant effect on self-inductance and mutual-inductance. Among these factors, the dimensions and positions of the conductors can be determined based on the device bonding diagram. However, the current directions are sensitive

and important, but difficult to define correctly, which will determine the polarity of coupling coefficient and thus have a significant impact. For devices working in switch mode, it is critical to verify the current paths and differentiate parasitic inductance in turn-on and turn-off conditions. However, such criteria are often neglected

To be specific, Fig. 2.8 shows a cascode GaN HEMT that is assumed to be working as an active switch in a switch-mode power supply. The blue loop, the red loop, and the green loop represent device's power loop, Si MOSFET driving loop, and GaN HEMT driving loop, respectively. The arrows indicate the current directions of each loop. During turn-on and turn-off transitions, the power loop maintains its direction; the two driving loops change their directions instead. Another important assumption is that when a conductor involves in more than one loop, the specified current direction follows the current direction in the power loop. According to these criteria, the current direction of each conductor can be determined. The inductances can then be accurately extracted by solving Maxwell equations in the FEA simulation, which are shown in Table 2.1. Different values are applied when simulating different switching transition.

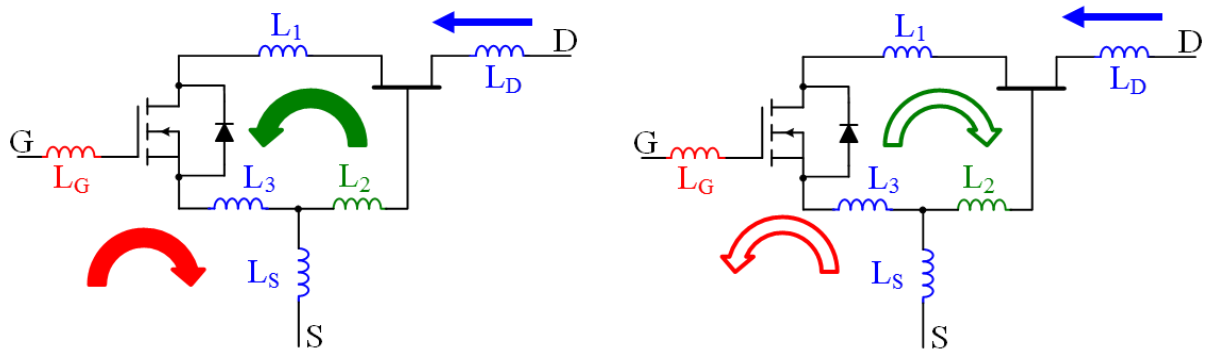


Fig. 2.8. Current directions of conductors in cascode package during (a) turn-on and (b) turn-off

Table 2.1. Package parasitic inductance extracted by Ansoft Q3D FEA simulation

Self+Mutual	*Turn On*	*Turn Off*
$L_1+\Sigma M_{1x}$	0.27 nH	0.26 nH
$L_2+\Sigma M_{2x}$	0.23 nH	0.17 nH
$L_3+\Sigma M_{3x}$	0.24 nH	0.43 nH
$L_S+\Sigma M_{Sx}$	0.57 nH	0.89 nH
$L_G+\Sigma M_{Gx}$	2.87 nH	3.12 nH
$L_D+\Sigma M_{Dx}$	1.89 nH	1.62 nH

It is important to point out that in this table, the effective parasitic inductance is the sum of self-inductance and mutual-inductance. The coupling effect leads to significant different for several parasitic inductance like L_3 and L_S, which are proved to be most critical common source inductance and have significant impact on the switching behavior of the cascode GaN HEMT in the next Chapter.

In order to verify the accuracy of the GaN HEMT simulation model, a double-pulse tester (DPT) is carefully designed and built with minimized parasitics as the test circuit to reveal the intrinsic switching performance of the device. The reason why DPT is used for simulation model verification is because the DPT can built up testing circuit to required steady state quickly without thermal limitation. With DPT, extreme testing condition is able to be measured, and high bandwidth current shunt with strict thermal limit can be adopted to improve measurement accuracy. This is especially important to characterize the ultra-high speed switching performance of the cascode GaN HEMT.

Fig. 2.9 shows the DPT schematic, PCB layout, and prototype. In this DPT, the 600V cascode GaN HEMT, also referred to DUT (device under test), is placed as the low side switch so that all signals are referenced to the ground and high bandwidth passive probes can be used for

measurement; the high side switch is a 600V GaN Schottky diode is used as the free-wheeling diode. It almost eliminates the reverse-recovery effect, and thus won't cause extra current overshoot and switching loss during the turn-on transition of the DUT. A high bandwidth current shunt is used to measure the current waveform of the DUT. Both current shunt and DUT is referenced to the ground so that no differential probe, usually has lower bandwidth, is in need.

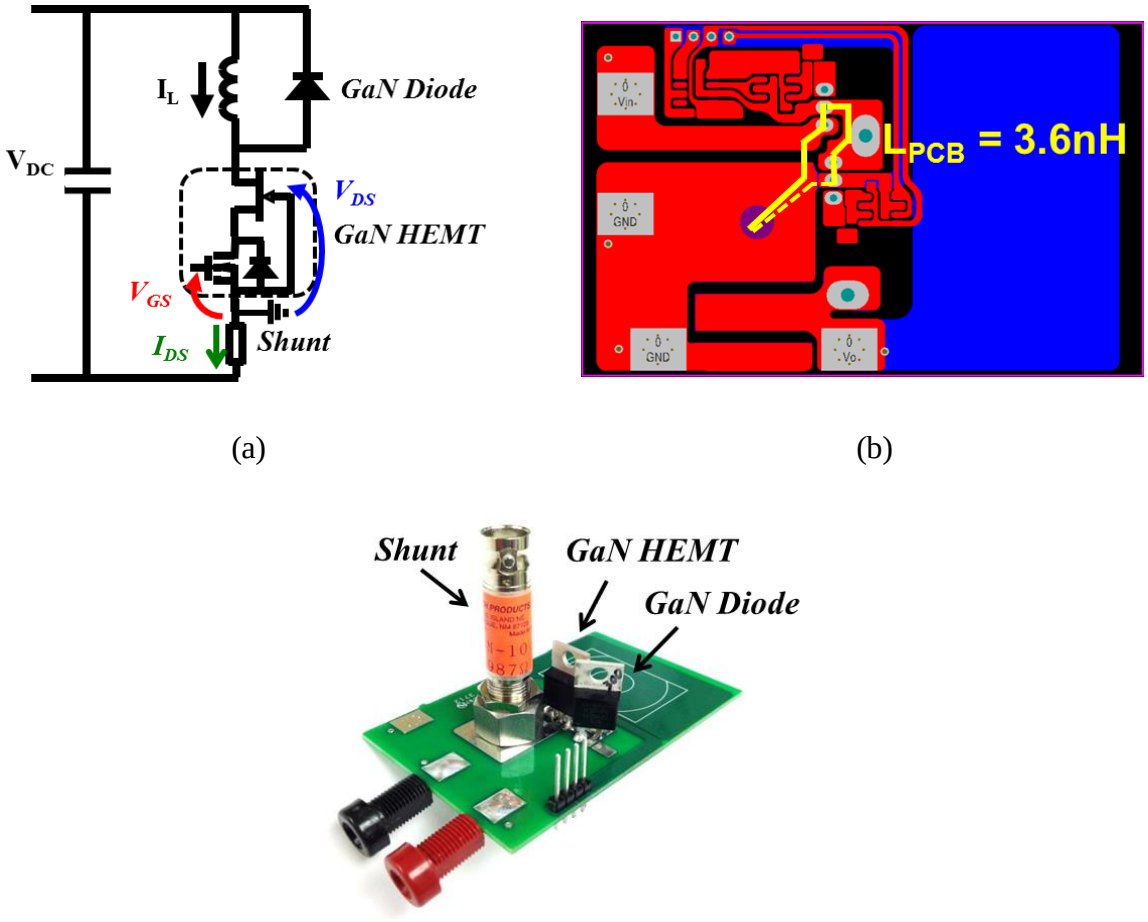
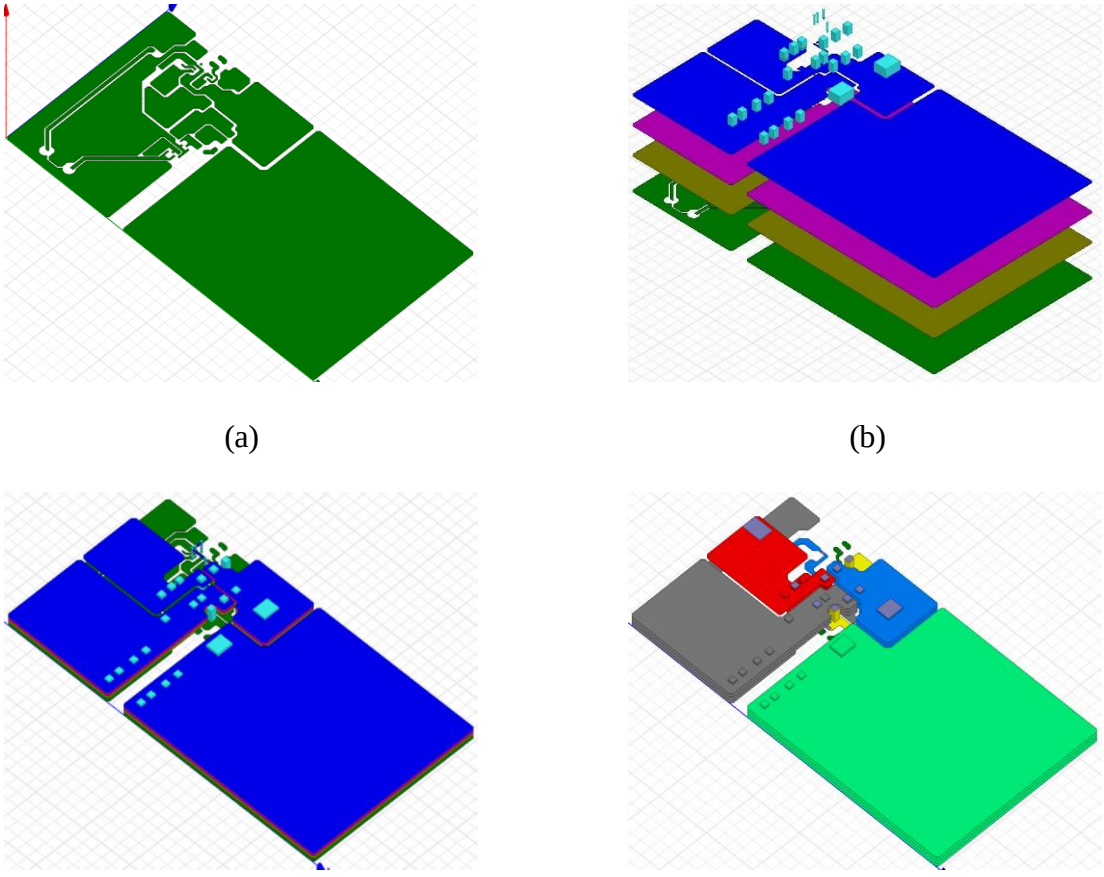


Fig. 2.9. Double-pulse-tester (a) schematic, (b) layout, and (c) prototype

In the DPT design, the critical loop is the high frequency commutation loop starting from the input capacitor, through the top switch and the bottom switch returning to the input capacitor (as the loop inclosed by the yellow curve). When doing layout, the design principle is to minimize the

loop inductance introduced by PCB trace. With optimized layout, the loop inductance is as low as 3.6nH as shown in Fig. 2.9 (b).



(a) (b)

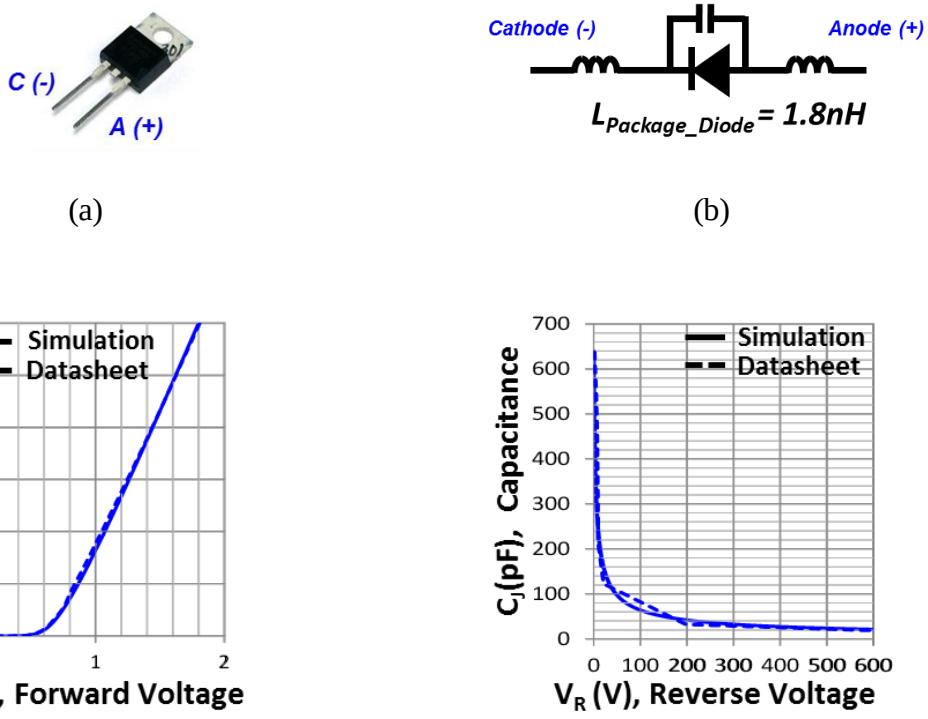
(c) (d)

Fig. 2.10. PCB parasitic inductance extraction process

Fig. 2.10 illustrates the parasitic inductance extraction of the PCB. Ansoft Q3D is used in this thesis to conduct FEA simulation. In general there are three steps. The first step is PCB file importation as shown in Fig. 2.10 (a) and (b). The copper traces, holes and vias are imported into Q3D layer by layer to make sure they are exactly the same as in the Altium Designer. Then the second step is assembly as shown in Fig. 2.10 (c). Different layers are all aligned according to one reference coordinate so that the relative position of every conductor pieces are accurate. The

thickness of copper trace and the distance between each layer are also clearly defined according to real manufacture parameters. The last step is net list and excitation assignment. Any conductors, including copper traces, holes and vias, physically connected are combined as one entity. Then one sink and one source are defined according to real working condition of the PCB to make sure all simulated self-inductance and mutual-inductance have clear physical meaning.

To prove the developed cascode GaN HEMT simulation model is accurate, each part of the DPT should also be modelled accurately. An accurate model for the GaN Schottky diode is also provided by device manufacturer, as shown in Fig. 2.11. The package parasitic inductance is extracted as 1.8nH. Both the simulated I-V characteristics and the simulated C-V characteristics are matching with its datasheet.



(a) (b)

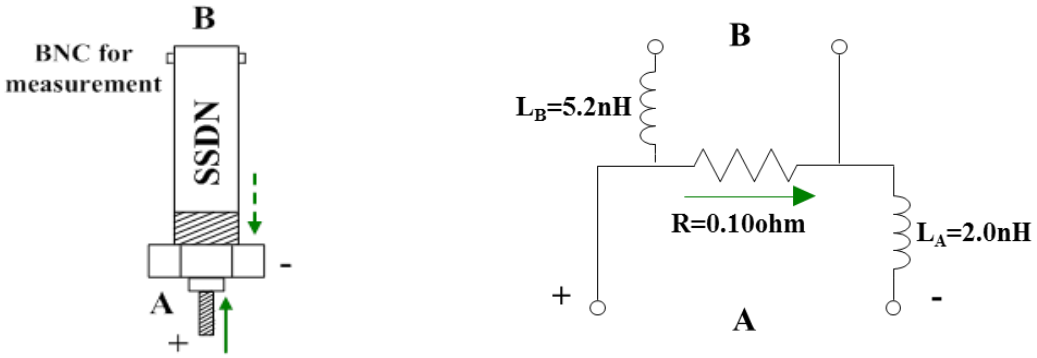
(c) (d)

Fig. 2.11. 600V GaN Schottky diode (a) package, (b) model, (c) I-V curve, (d) C-V curve

The current waveform of the DUT is measured by a coaxial current shunt (part number SSDN-10) manufactured by T&M Research Products Inc., which has accurate resistance, small parasitic inductance, and high bandwidth. Table 2.2 shows the electrical characteristic specifications [B.1] of the current shunt. The operation principle of the current shunt is elaborated in [B.2]. Following the same modeling method discussed in [B.2], the current shunt is modeled by the circuit shown in Fig. 2.12. Both of the parasitic inductances are measured by an Agilent 4294A impedance analyzer with proper adaptors.

Table 2.2. Electrical specifications of the coaxial current shunt

Part Number	Resistance	Bandwidth	P_{MAX}	E_{MAX}
SSDN-10	0.10 ohms	2000 MHz	2 W	2 J



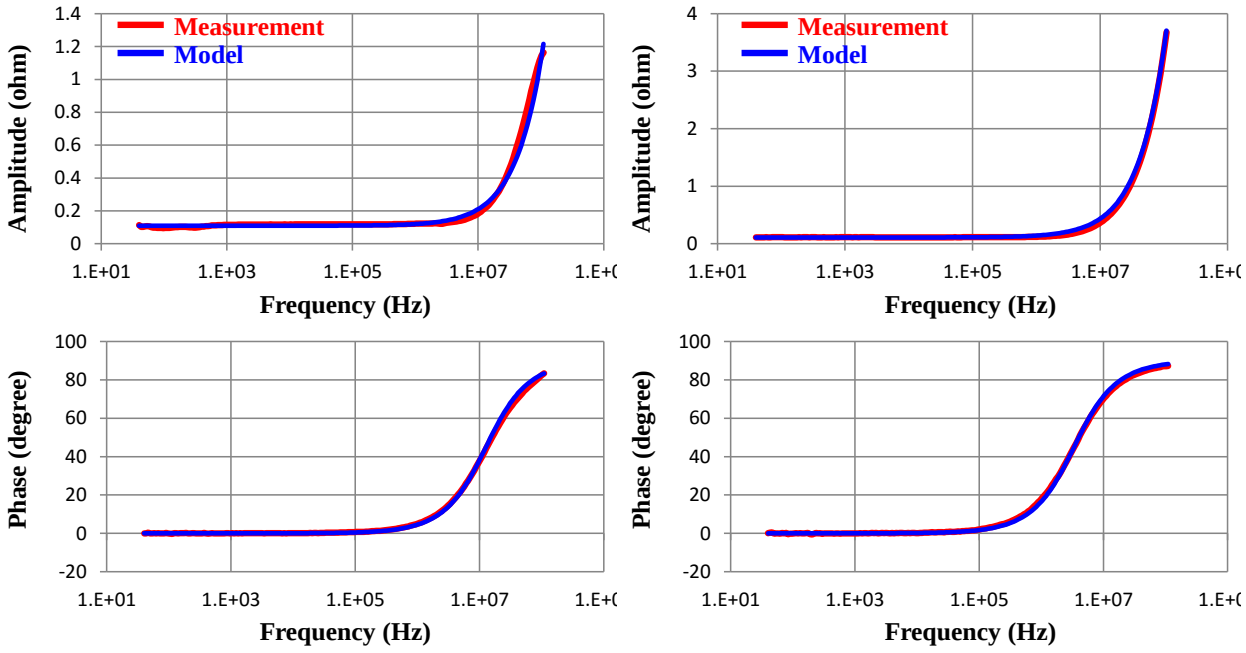
(a) (b)

Fig. 2.12. High bandwidth coaxial current shunt (a) prototype, (b) model

The secret of the high bandwidth is the shunt resistor is like an inductor-less resistor. Neither L_A nor L_B decide the bandwidth, because L_A is not in the measurement loop while L_B is not in the main current path. The bandwidth is actually decided by the parasitic inductance shared the two loops which is as small as tens of pH.

The selection of the current shunt is also a trade-off. A current shunt with larger resistance also has larger size so that the inductance introduced to the original power loop is too high. While a current shunt with smaller resistance has reduced magnitude on measured signal and smaller bandwidth which finally leading to less measurement accuracy. A proper current shunt is another key factor for accurate device characterization by DPT.

The model of the current shunt is verified by matching the impedance with the measurement results by impedance analyzer. Fig. 2.13 shows that the model matches well with measurement in terms of both magnitude and phase.



(a) (b)

Fig. 2.13. Current shunt impedance (a) terminal A, (b) terminal B

After each part of the DPT is well modelled, a series of double pulse tests are conducted to verify the simulation model and to analyze the switching performance of the cascode GaN HEMT. Fig. 2.14 shows a typical waveform of the double pulse test. During the first pulse, the inductor

current is quickly built up to the required current level. Then at the end of the first pulse, the turn-off transition is measured. Some dead time are applied between the first pulse and the second pulse so that the parasitic ringing is well damped. The dead time is also short enough so that the inductor current free-wheeling through the diode is almost the same before the second pulse. Then at the beginning of the second pulse, the turn-on transition is measured.

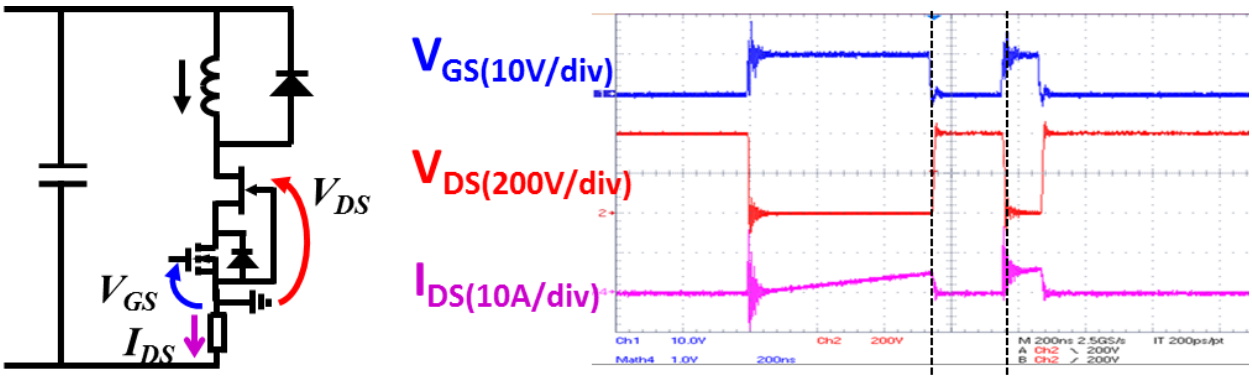
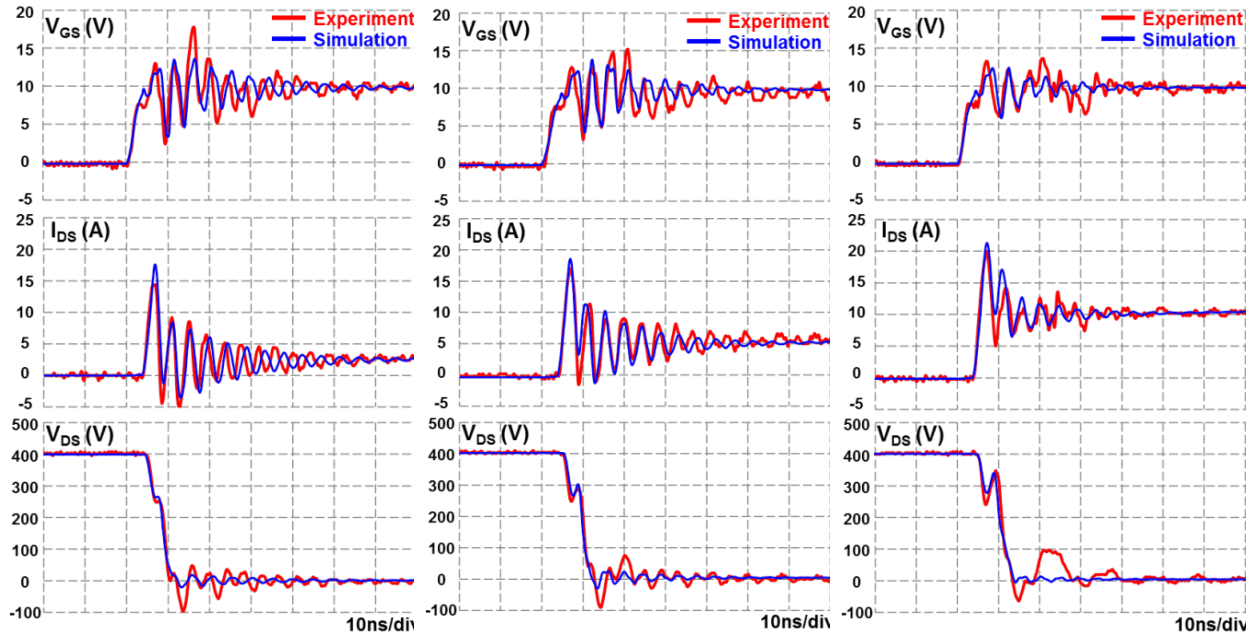


Fig. 2.14. Double pulse test typical waveform

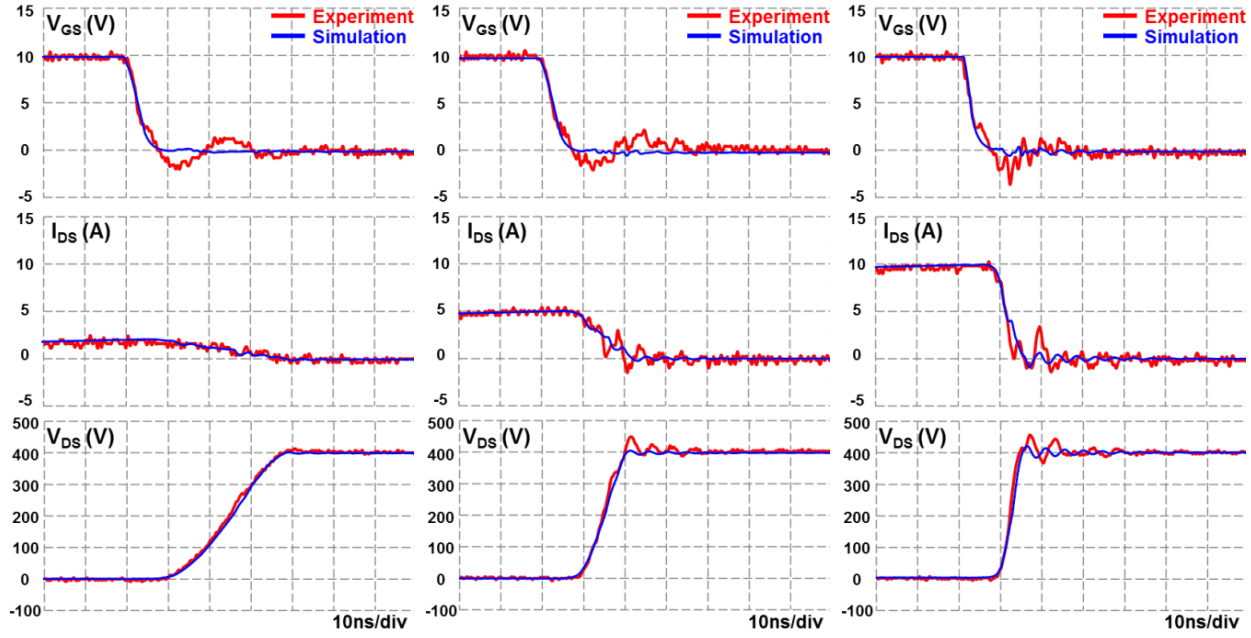
Zoom-in waveforms showing detailed switching transition process are listed in Fig. 2.15.

The accuracy of the cascode GaN HEMT simulation model is first verified by comparing simulation waveforms with experimental waveforms. The simulation match well with experiment in terms of switching transition time sequence, rising/falling slope, frequency, magnitude and phase of the parasitic ringing.

When comparing the simulation waveform before and after modification, the accuracy improvement is prominent. Both Fig. 2.16 and Fig. 2.17 indicate that the previous simulation model without modification has big mismatch with experiment, while the modified simulation model can predict the real switching performance of the GaN HEMT in high accuracy.



(a) (b) (c)



(d) (e) (f)

Fig. 2.15. Zoom-in switching waveforms (a) 400V/2A turn on; (b) 400V/5A turn on; (c) 400V/10A turn on; (d) 400V/2A turn off; (e) 400V/5A turn off; (f) 400V/10A turn off

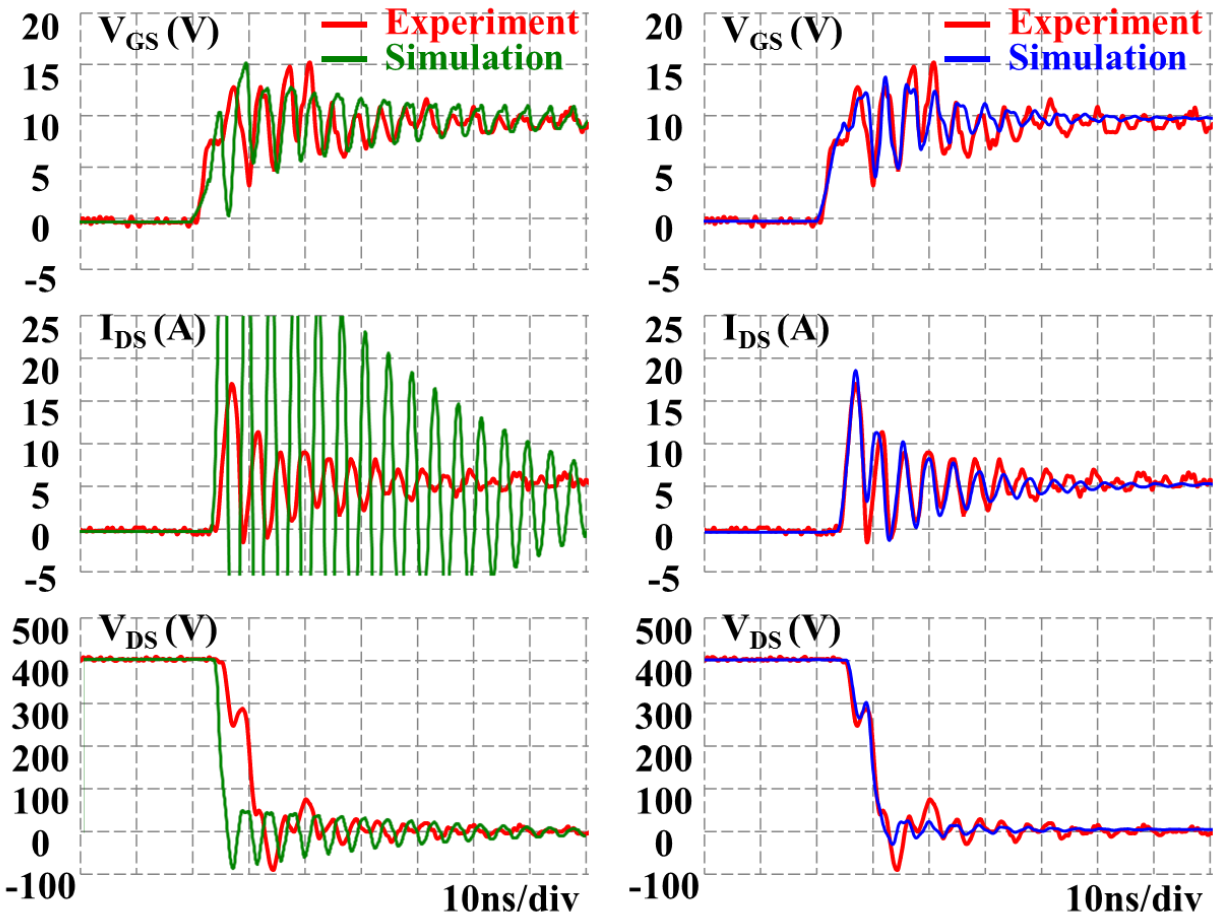
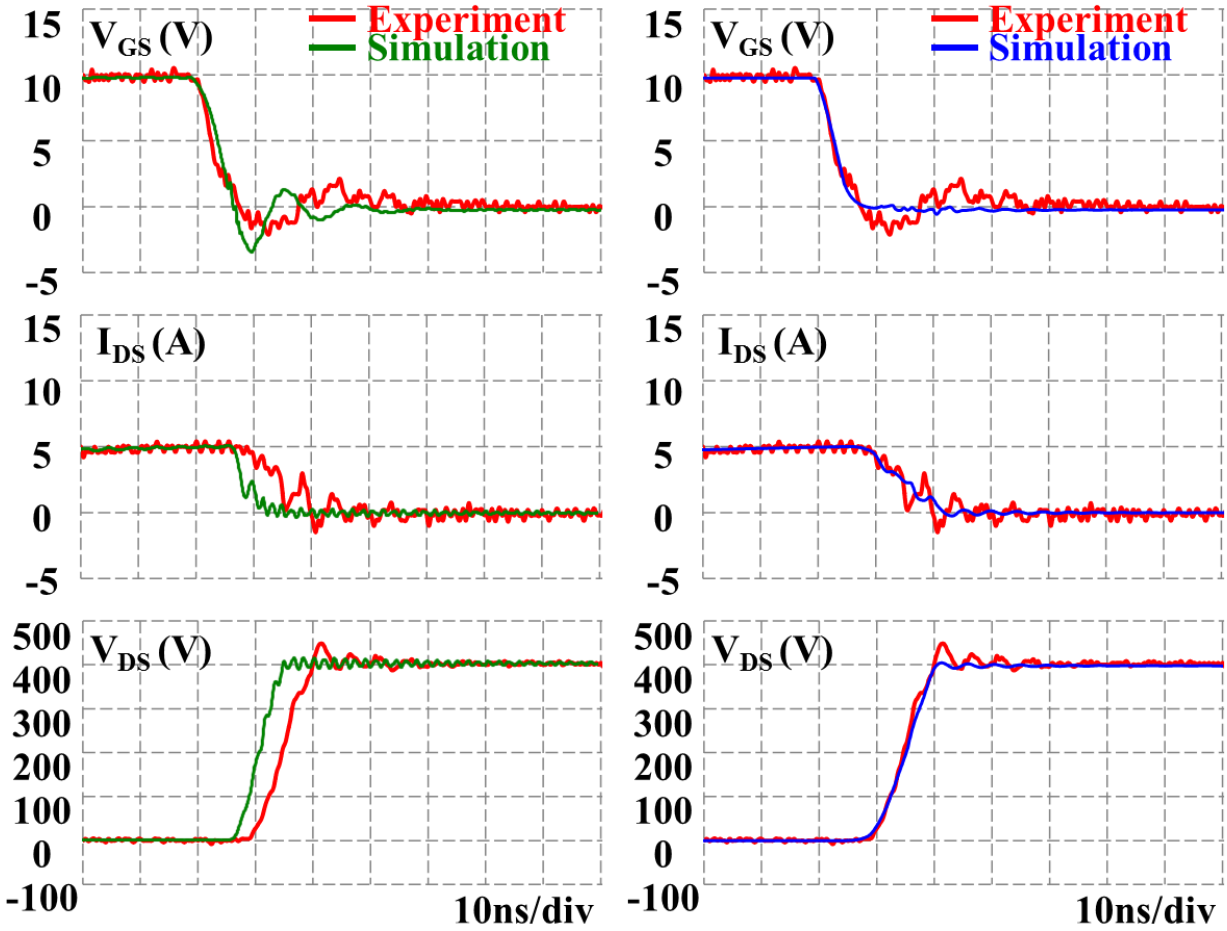


Fig. 2.16. Simulation model comparison (a) before modification and (b) after modification (turn on waveforms under 400V/5A condition)

Based on the switching waveforms, the switching energies can be defined and calculated. The turn-on energy (E_{ON}) and turn-off energy (E_{OFF}) are defined as the energies dissipated on the switch during turn-on transition and turn-off transition. Fig. 2.18 shows the calculation of E_{ON} based on the experimental waveforms of V_{DS} and I_{DS}. To be specific, the green curve is the product of V_{DS} and I_{DS} which is the instantaneous power dissipated on the device. Then the integral of the instantaneous power from t_1 (the instant when I_{DS} starts to increase) to t_2 (the instant when I_{DS} settled to steady state within 10% error band) is defined as E_{ON}. E_{OFF} is calculated following the

same method. In this way, the calculated switching energy will contain not only the main transition loss, which is usually the major part of switching loss, but also the ringing loss, caused by parasitic oscillation and is not negligible in this case, during the entire switching transition.



(a) (b)

Fig. 2.17. Simulation model comparison (a) before modification and (b) after modification (turn off waveforms under 400V/5A condition)

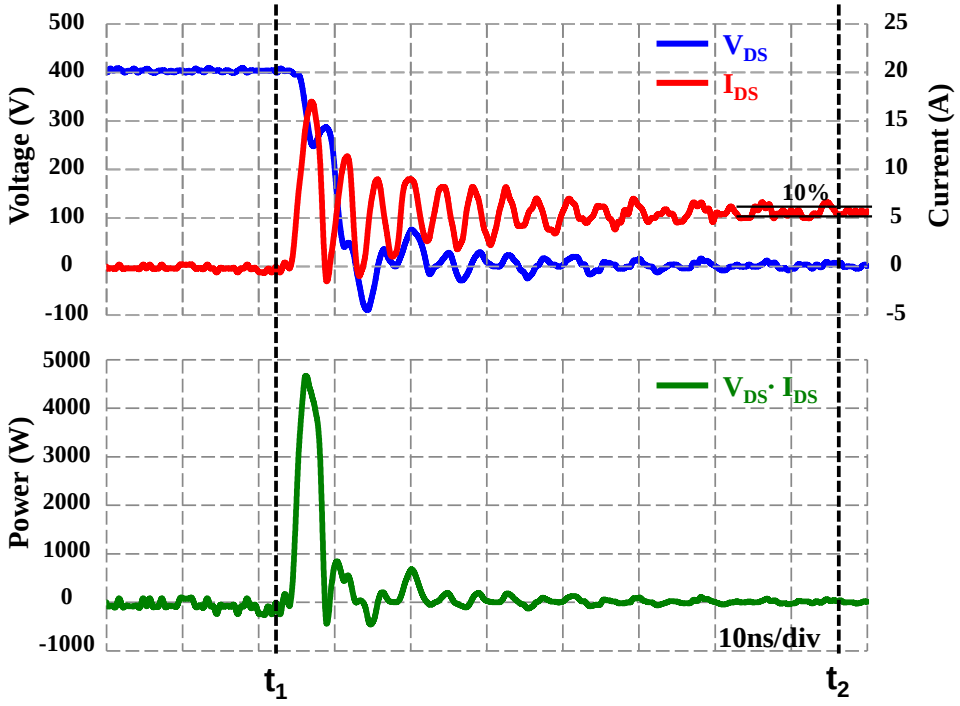
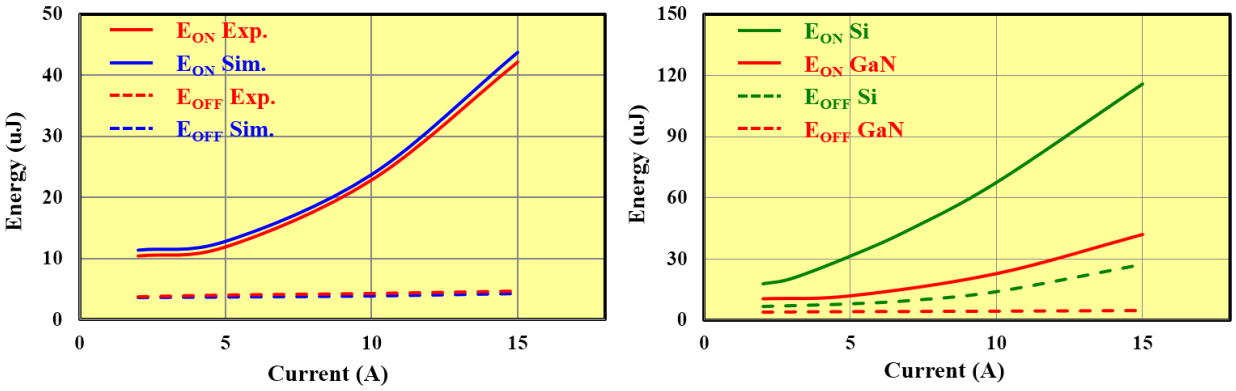


Fig. 2.18. Calculation of turn-on energy

The switching energies in different load currents are measured and shown in Fig. 2.19 (a). The results of the simulation also match well with experiments. It is a clear trend that the turn-on energy is much larger than the turn-off energy, which is due to severe current spikes and oscillations, in entire range of load current. This phenomenon is also observed in cascode SiC JFET [B.3]. In addition, the turn-on energy is a strong function of load current. In contrast, the turn-off energy is extremely small and almost constant under different load currents. This phenomenon is unique and related to the specialty of the cascode structure, which will be addressed in the next section.

The double pulse test is based on current waveform from device terminal. So the energy on C_{oss} is stored in turn off but dissipated during turn on. So the measured turn on energy is underestimated compared to real turn-on loss while the turn off energy is overestimated compared to real turn-off loss.

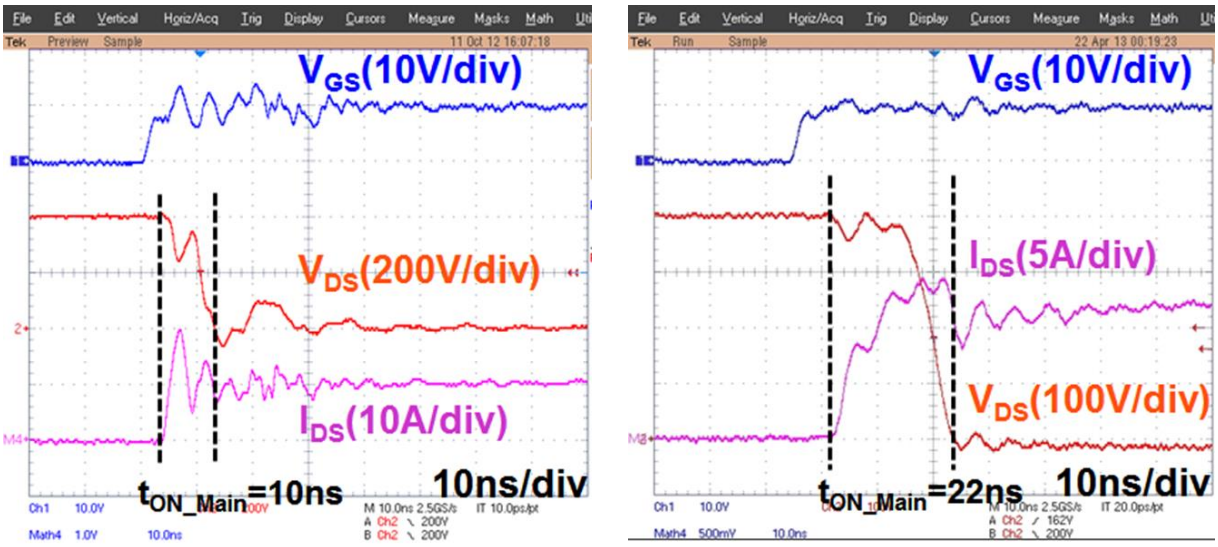


(a) (b)

Fig. 2.19. DPT switching energy comparison (a) experimental and simulation results of GaN, (b) comparison between GaN and Si

Compared to the state-of-the-art super junction Si MOSFET with similar voltage rating, current rating, and on resistance (part no. IPP60R160C6), the switching energy of the cascode GaN HEMT is significantly smaller as shown in Fig. 2.19 (b). In addition, unlike the almost constant turn-off energy of GaN, the turn-off energy of Si MOSFET will increase with the turn-off current gradually.

The turn-on waveform comparison is shown in Fig. 2.20. It can be observed that the dv/dt and di/dt of GaN is higher than Si MOSFET. Also the main transition time of GaN is significantly smaller than Si MOSFET so that the corresponding turn-on loss is much smaller. So at 400V and 10A turn-on condition, the turn-on time and turn-on energy of GaN is 10ns and 23.4uJ while that of Si is 22ns and 67.5uJ.

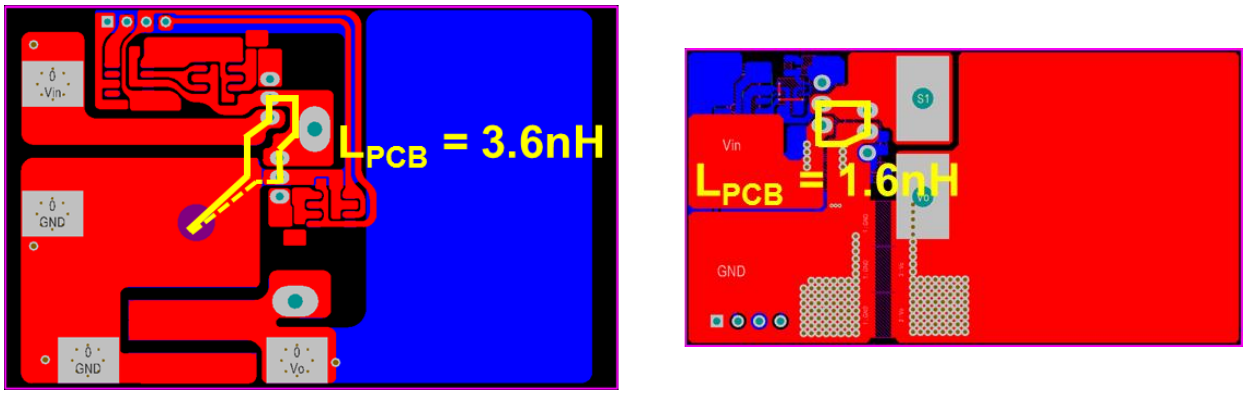


(a) (b)

Fig. 2.20. DPT turn-on waveform comparison between GaN and Si

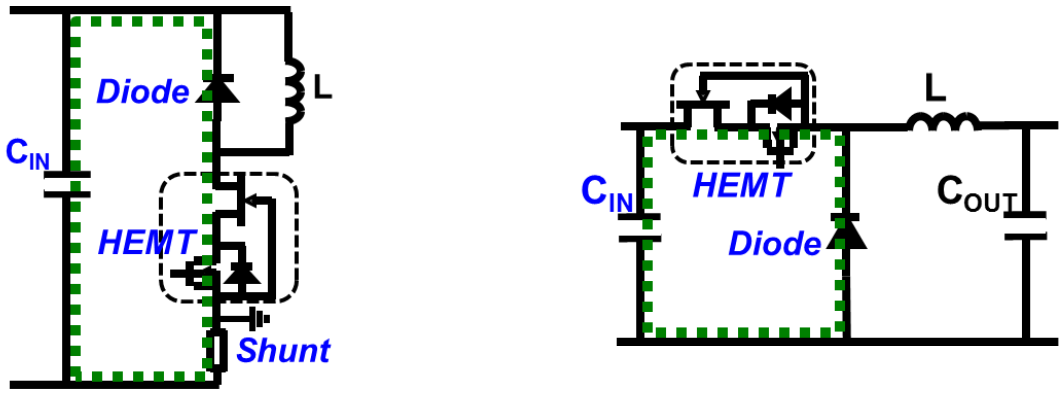
Even the simulation model is verified by experiment, there is still another concern that whether the switching energy measured in a double pulse tester can reflect the real switching loss distribution in a buck converter or boost converter because in a real continuously working converter there is no bulky current shunt inserted in the critical power loop and the corresponding parasitic inductance could be very different. So the impact of current shunt should be evaluated.

In order to compare the impact of current shunt in terms of switching loss measurement, a traditional buck converter is built for comparison. The buck converter uses the same devices as the DPT, while loop inductance introduced by PCB can further be shrunk as the current shunt is removed. Fig. 2.21 and Fig. 2.22 show the comparison of PCB and schematic, respectively. Table 2.3 shows the comparison of parasitic inductance on the commutation loop. More than 30% total commutation loop inductance is saved in an optimized buck converter design than an optimized DPT design.



(a) (b)

Fig. 2.21. Layout comparison between (a) double-pulse tester and (b) buck converter



(a) (b)

Fig. 2.22. Schematic comparison between (a) double-pulse tester and (b) buck converter

Circuit simulations are conducted for both buck converter and DPT, and corresponding switching loss distributions are compared in Fig. 2.23. As the buck converter has smaller loop inductance, higher turn-on loss and lower turn-off loss are observed. This trend is in accordance with the conclusions in [B.2]. However, the differences are not significant. Through this comparison, it can be concluded that under careful design, a double-pulse tester can reflect the trend of real switching loss distribution in a bridge configuration converter with small differences.

Table 2.3. Parasitic inductance comparison between DPT and Buck

	DPT	Buck
L_{PCB}	3.6 nH	1.6 nH
$L_{Cin\_Package}$	0.3 nH	0.3 nH
$L_{HEMT\_Package}$	3.0 nH	3.0 nH
$L_{Diode\_Package}$	1.8 nH	1.8 nH
$L_{Shunt\_Package}$	2.0 nH	-
Loop	10.7 nH	6.7 nH

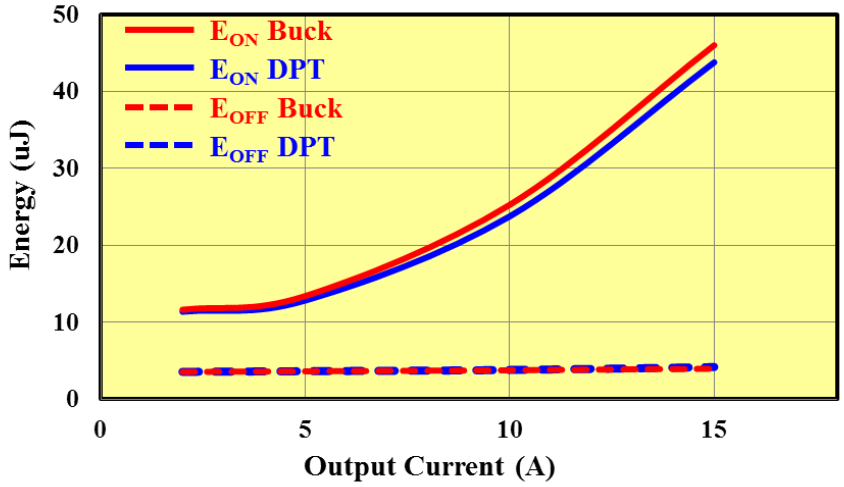


Fig. 2.23. Switching energy comparison between DPT and Buck

2.2 Switching Loss Mechanism Analysis and Soft Switching

After the development and verification of the simulation model, it is used as a tool to analyze the switching performance of a given power converter. For the application of bi-directional battery charger/discharger, a 380 V to 200 V bi-direction buck-boost converter is built with 600 V cascode GaN HEMTs as both the top switch (TS) and the bottom switch (BS) (Fig. 2.24). For TS driving, the ICs NCP5181 and ISL89163 are used in series; for BS driving only the ISL89163 is used. The

PCB is also carefully designed with minimized parasitic inductance of 1.6nH for the commutation loop and 3.3nH for the TS/BS driving loop.

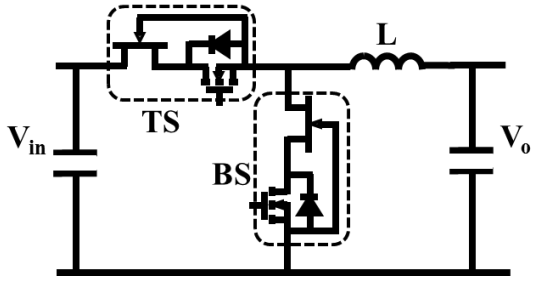


Fig. 2.24. Bi-direction buck-boost converter schematic

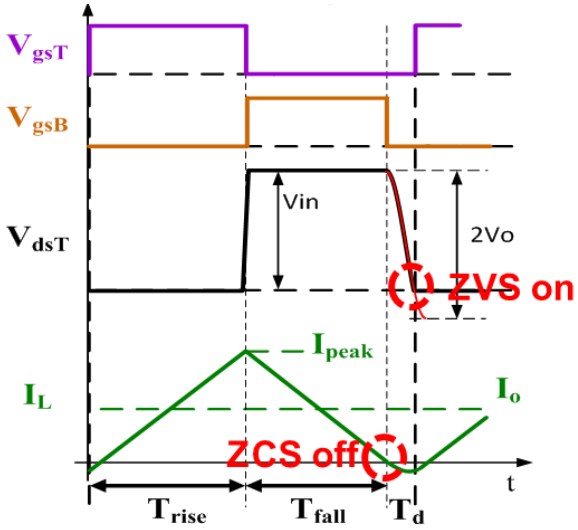
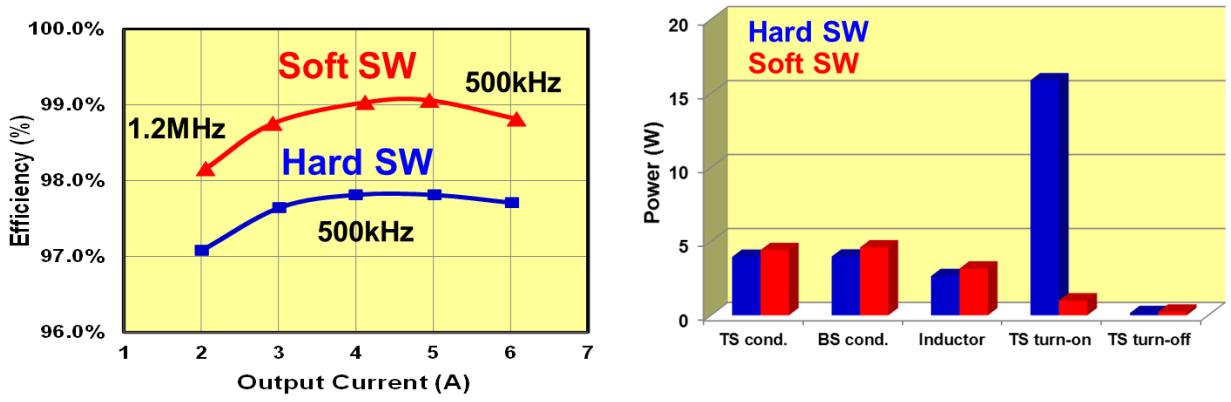


Fig. 2.25. Critical conduction mode operation

Fixed frequency continuous-current-mode (CCM) is used for the hard-switching; the inductor peak-peak current ripple is 3 A, which is 50% of the full load current. While variable-frequency critical conduction mode (CRM) is used for soft-switching demonstration; the CRM could achieve both ZVS turn-on of TS and ZCS turn-off of BS; the inductor peak-peak current ripple is more than twice the load current at any load conditions. The efficiency curves shown in Fig. 2.26 (a) reveals a clear trend that soft switching is superior to hard switching in all load ranges tested.

Furthermore, a converter loss breakdown is conducted and shown in Fig. 2.26 (b), in which the total inductor loss, including core loss and winding loss, are tested according to the methods proposed in [B.4]; the conduction loss and the switching loss are calculated by the developed simulation model.



(a) (b)

Fig. 2.26. Comparison between hard switching and soft switching (a) Buck converter efficiency, (b) loss breakdown at full load

In hard-switching conditions, the TS turn-on loss is the dominant part of total loss. Fig. 2.27 shows the corresponding TS turn-on waveforms. Even though the load current is only around 5 A, the current overshoot reaches 25 A peak value. This is due to the reverse-recovery effect and junction capacitor charging of the BS (highlighted by the red area). The crossover between the high-voltage and high-current overshoot results in a large turn-o n loss. It can also be observed that the di/dt is about 3000 A/us, which is much higher than the traditional 600 V Si MOSFET. This high speed is due to the inherent characteristics of the GaN HEMT.

When comparing hard switching with soft switching, the loss breakdown indicates that the TS turn-on loss is the dominant loss in hard-switching conditions, much larger than any other loss; this is why hard switching has much lower efficiency. In the soft-switching case, due to higher

turn-off current and RMS current, the price paid is a little bit higher conduction loss, turn-off loss and inductor loss, while turn-on loss is eliminated as a trade-off. In total, soft switching benefits a lot in terms of efficiency.

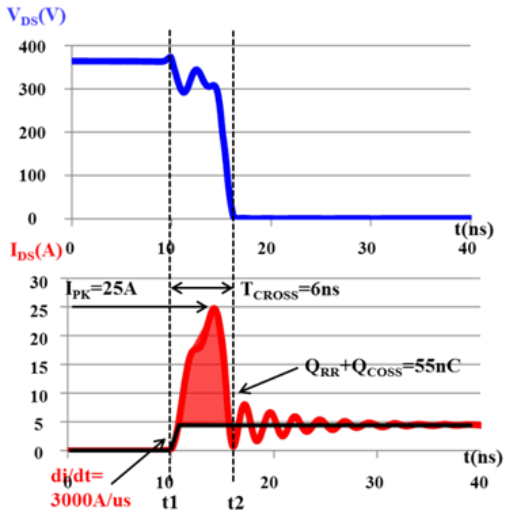
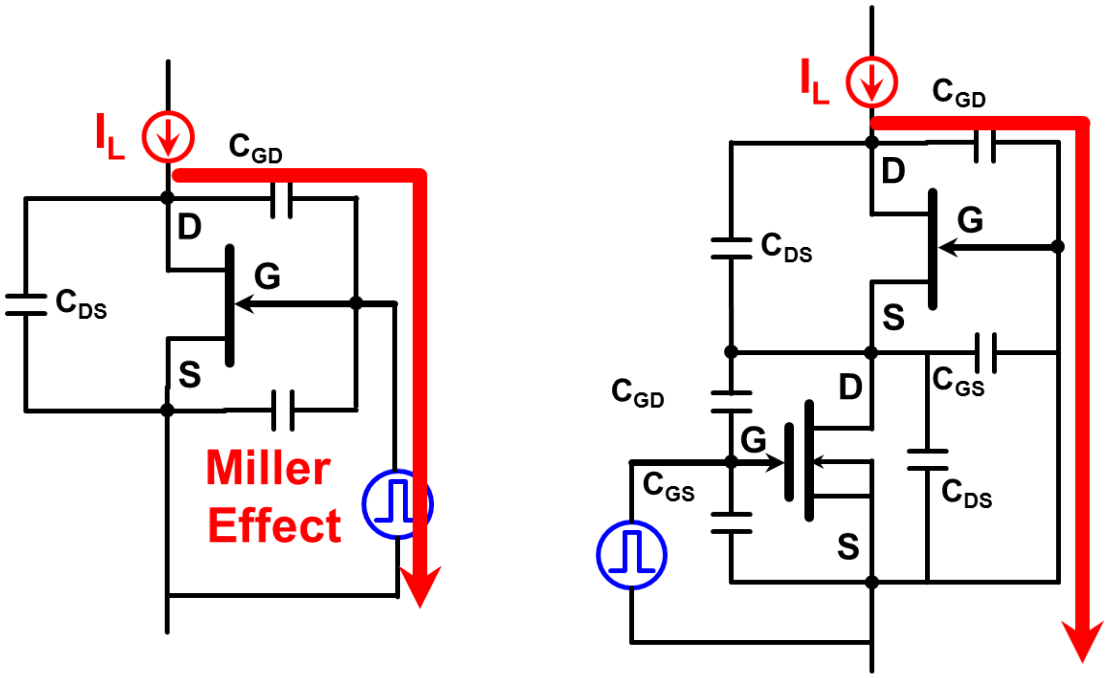


Fig. 2.27. Buck converter TS turn-on waveforms at CCM hard-switching condition

Another important phenomenon observed from both the switching energy distribution and the loss breakdown is the turn-off loss is extremely small and not sensitive to the load current. Similar trend was also observed in cascode SiC JFET mentioned in paper [B.3]. So it seems a common phenomenon existing in cascode structure. Using both the simulation model discussed in this thesis and the analytical model proposed in paper [B.5], the current source turn-off mechanism, which accelerates the turn-off transition and reduces turn-off loss, is discovered.

Fig. 2.28 introduces the basic concept of the ultra-fast turn-off transition in cascode structure by comparing the turn-off equivalent circuit between a normally-off GaN device and a cascode GaN device.



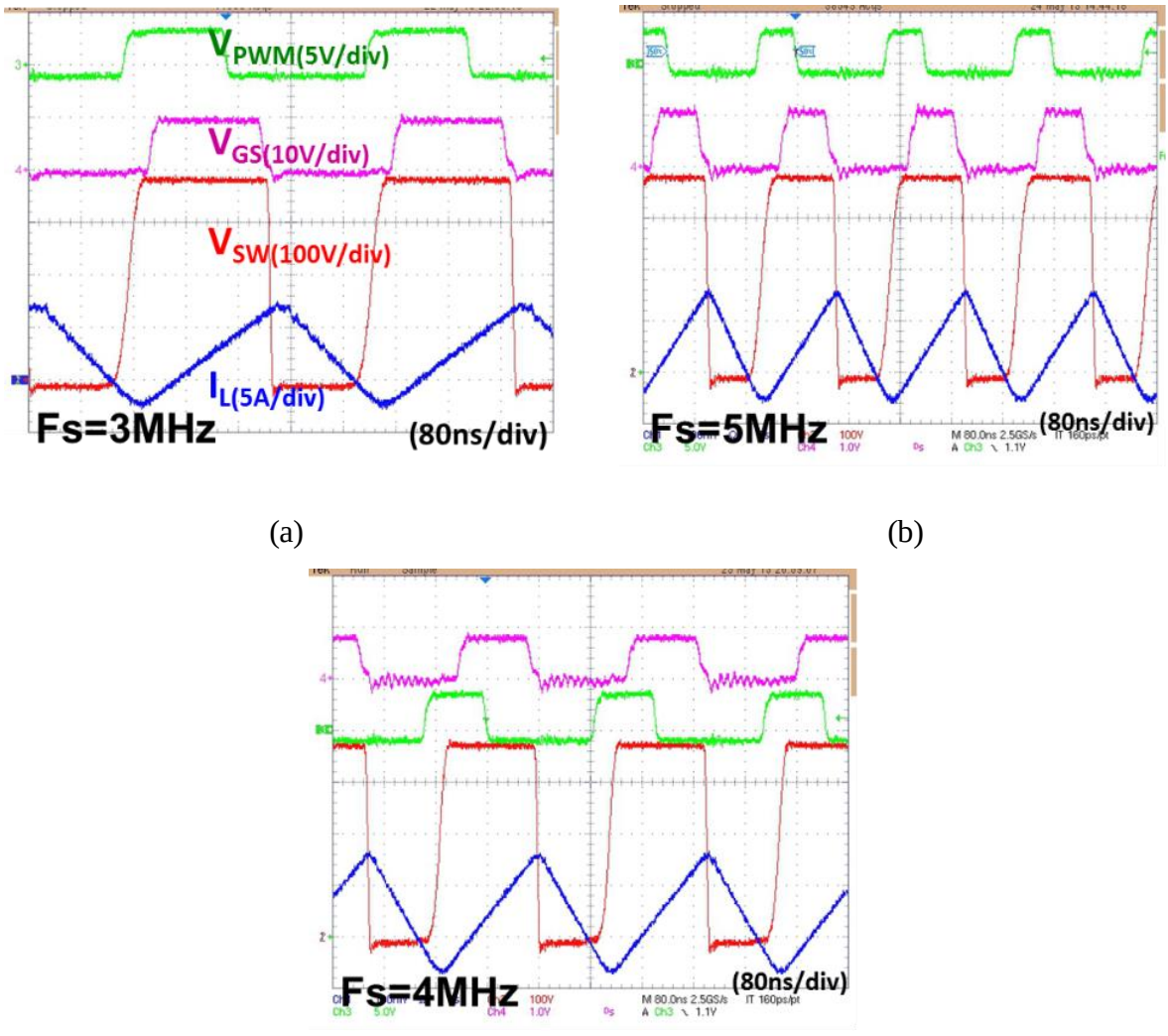
(a) (b)

Fig. 2.28. Turn-off equivalent circuit comparison (a) N-off GaN, (b) cascode GaN

For a normally-off GaN device, during turn off process the inductor current charges the C_{GD}, which referred as miller capacitor, so that the charging current affects the external gate driver. This current is in the same direction with the driving current to turn off the device. So the result is the miller capacitor current reducing the driving capability of the driver and leading to a miller plateau with high turn-off loss.

On the contrary, for a cascode GaN device, the current charging the miller cap of the depletion mode GaN device flowing out of the device without affecting the gate driver. So the miller capacitor is charged by a current source and gate driver can turn-off the device as fast as possible. As a result, the corresponding turn-off loss is extremely small and not sensitive to the turn-off current.

The unique feature of the cascode GaN HEMT further justifies the application of CRM mode because ZVS eliminates the dominant turn-on loss while turn-off loss maintaining in low level with high turn-off current compared to CCM operation. Also due to the high current ripple, the RMS current increases at the same time. However, GaN device has smaller specific on-resistance making it less sensitive to conduction loss. The trade-off between switching loss and conduction loss is even different for GaN device than for Si device.



(a) (b)

(c)

Fig. 2.29. CRM buck waveforms at (a) 3 MHz, (b) 4 MHz, (c) 5 MHz

With CRM operation and ZVS, high frequency and high efficiency are bale to be achieved at the same time. The switching frequency is further pushed to as high as 5 MHz. Fig. 2.29 shows the waveform at multi-MHz. For a 380 V to 200 V, 600 W output buck converter, 99% peak efficiency is still achieved at 5 MHz.

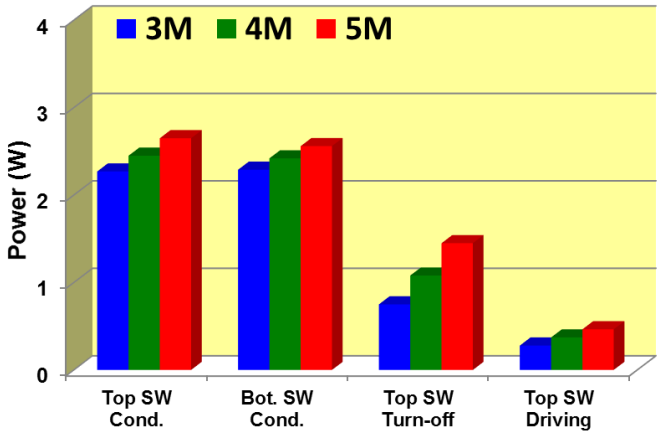


Fig. 2.30. Loss breakdown at 3-5 MHz

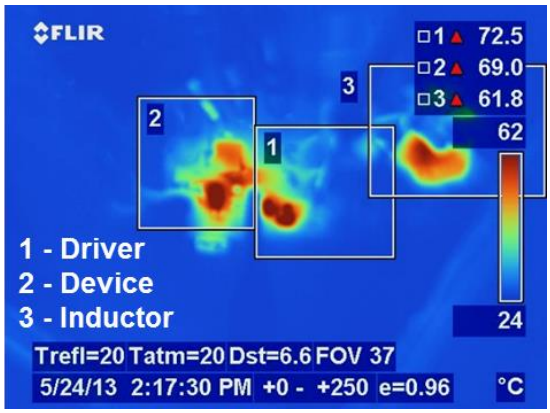


Fig. 2.31. Thermal image at 5 MHz

The loss breakdown shows that switching related loss are still very small. While thermal image further demonstrates that the temperature of the GaN device is well under control. The higher case temperature is 72.5℃. So the estimated junction temperature is below 85℃ leaving enough safety margin.

In summary, CRM mode soft switching benefits the cascode GaN HEMT. Multi-MHz frequency operation is achieved with 99% peak efficiency. Further pushing frequency and power is possible but limited by current packaging design which is illustrated in the next section.

2.3 Package Impacts of Cascode GaN

2.3.1 Common Source Inductance of Cascode GaN Package

Due to the merits of the cascode GaN HEMT, the device is able to switch at very fast speed. However, as a result of the parasitics introduced by the bulky package, large switching losses and severe oscillations are observed during the switching transitions, which definitely limit the switching performance of the device, and cause potentially more electro-magnetic interference (EMI) for none-optimum circuit designs.

Regarding packaging influence study, many efforts are spent on the Si MOSFET with a single switch structure [B.6]-[B.8]. It is a common sense that the common-source inductance (CSI), which is defined as the inductance shared by power loop and driving loop, is the most critical parasitics. The CSI acts as negative feedback to slow down the driver during the turn-on and turn-off transitions, and thus prolongs the voltage and current crossover time, and significantly increases the switching loss.

Recently, there have been some publications discussing the package influence for wide-band-gap devices, like the high-voltage SiC MOSFET and low-voltage GaN HEMT [B.2]. The devices also use a single-switch structure, and therefore the conclusions are similar to that of the Si MOSFET, in which the CSI still has major impact on the device's switching loss. However, due to the uniqueness of the cascode structure, the definition of the CSI is not straightforward. So far there have been few paper addresses this issue. In this thesis, the analysis starts from the identification of critical parasitic inductance.

Following the same definition of CSI in a single-switch structure, the CSI of the low-voltage Si MOSFET and of the high-voltage GaN HEMT are analyzed. From the perspective of the Si

MOSFET (Fig. 2.32(a)), the blue loop is the power loop and the red loop is the driving loop. It is clear that L_{int3} and L_S are shared by the two loops, so they are the CSIs of the Si MOSFET. Similarly, from the perspective of the GaN HEMT (Fig. 2.32(b)), the blue loop is still the power loop, but the driving loop is changed to the green loop. As a result, L_{int3} and L_{int1} are the CSIs of the GaN HEMT.

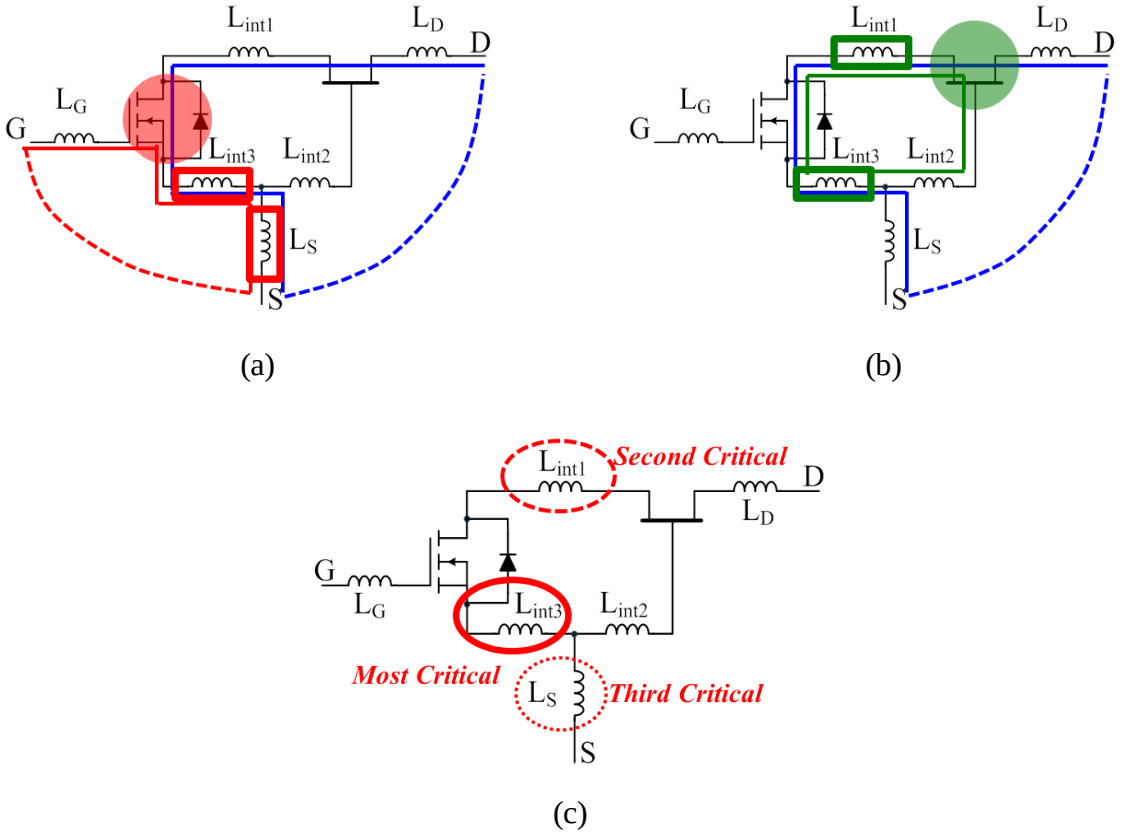


Fig. 2.32. Common source inductance in cascode package (a) Si's perspective, (b) GaN's perspective, (c) for cascode structure

Therefore, in terms of the cascode structure (Fig. 2.32(c)), since L_{int3} is the CSI for both the GaN HEMT and the Si MOSFET, it should be the most critical parasitic inductance. L_{int1} is estimated to be the second-most critical inductance, since it is the CSI of the high-voltage GaN

HEMT, which has the major switching loss. Last but not least, L_S is predicted to be the third-most critical inductance.

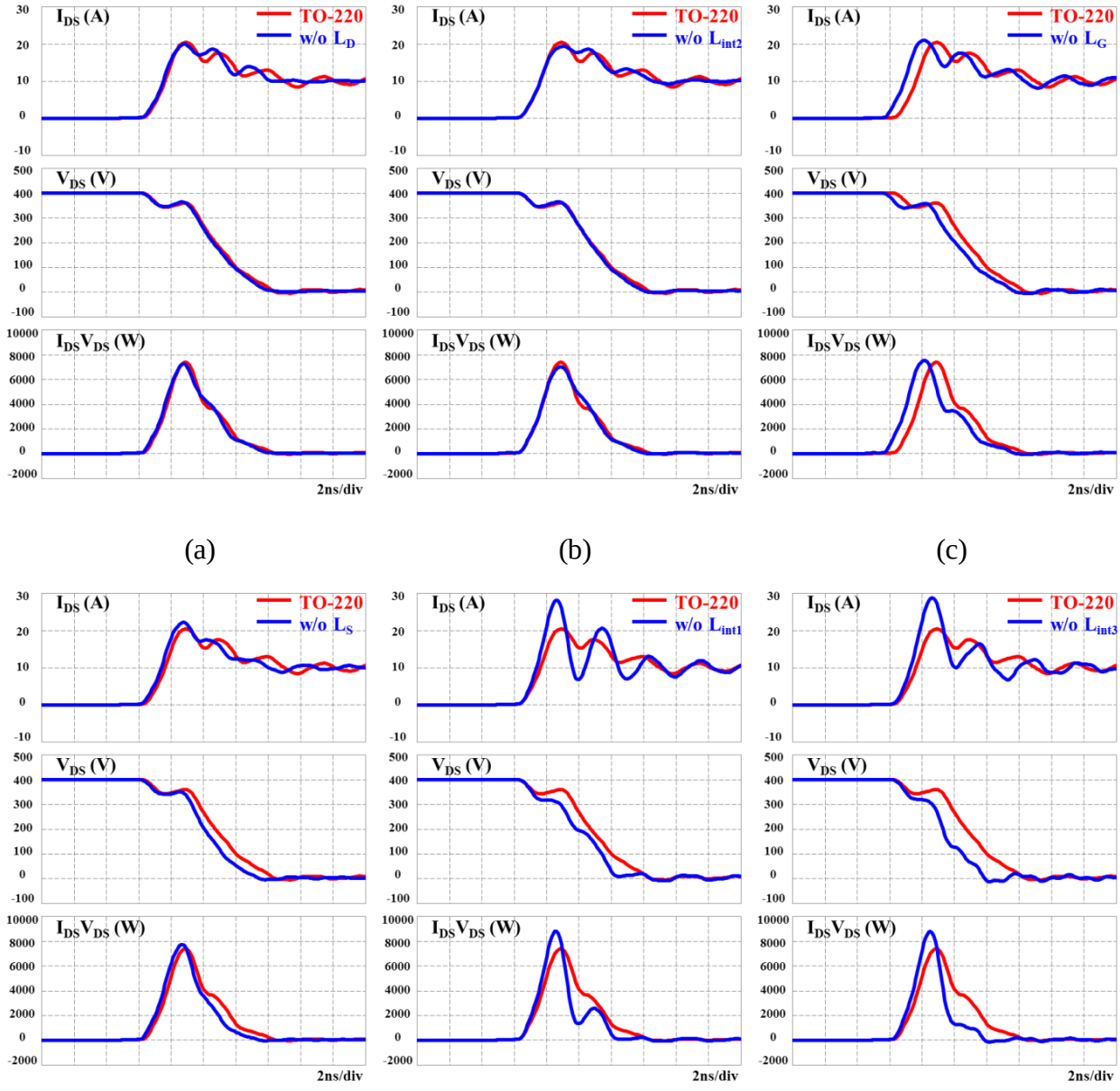


Fig. 2.33. Top switch hard-switching turn-on waveforms comparison at 400 V/10 A

After theoretical analysis, the simulation model is used to verify the predictions. A circuit-level simulation is conducted based on a buck converter design working in the continuous-current-

mode hard-switching condition. The switching loss during the hard-switching condition is the major concern. Since the turn-on switching loss is the dominant part, the turn-on energy at 400 V/10 A condition is chosen for comparison. A series of simulation waveforms is shown in Fig. 2.33, in which the simulation results based on the TO-220 package is always set as the benchmark (red line), while each comparison case (blue line) removes one of the six parasitic inductance to evaluate the impact of that specific parasitic inductance.

By comparing waveforms, the different impacts of each parasitic inductance can be observed. Without L_D or L_{int2}, the waveforms have almost no difference; without L_G, there is an obvious forward phase shift for I_{DS} and V_{DS}; however, in terms of turn-on energy, there is still no significant difference. In contrast, when without L_S, L_{int1} or L_{int3}, the I_{DS} has higher overshoot, while the V_{DS} has sharper falling edge compared to the benchmark; thus shorter transition times and smaller turn-on energies are observed in these three cases.

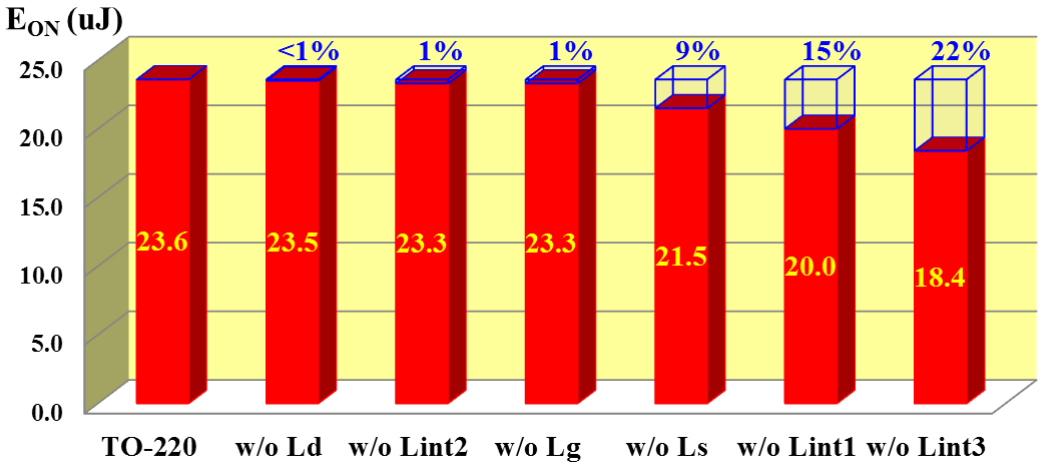


Fig. 2.34. Device turn-on loss comparison at 400V/10A

For better quantitative comparison, the simulated turn-on switching loss is shown in Fig. 2.34. Based on the TO-220 package case, the total turn-on energy is 23.6 uJ at 400 V/10 A condition,

which is set as the benchmark. By eliminating the impact of L_D, L_{int2} or L_G, the reduction of turn-on switching loss is negligible (around 1% of 23.6 uJ). On the other hand, when the critical parasitic inductance like L_S, L_{int1} or L_{int3} is removed, the turn-on switching loss will reduce significantly (9%, 15%, and 22% of 23.6 uJ respectively).

In summary, the simulation results have quantitatively justified the predictions of the theoretical analysis, that the L_{int3}, L_{int1} and L_S are identified to be the most critical package parasitic inductance. For future research regarding packaging improvement, these three inductances should be minimized in priority. Furthermore, it could be project that if an advanced package realized, which is able to eliminate all three critical parasitic inductances, the total device switching loss should have a significant reduction while better switching performance is expected.

2.3.2 Potential Failure Mode

As mentioned in Section 2.2, when the cascode GaN HEMT operates in CCM hard-switching buck converter, significantly high turn-on switching loss is observed. One of the major reason is the reverse recovery charge and junction capacitor charge of the bottom switch. The other major reason is the package parasitic inductance impact.

Fig. 2.35 shows the equivalent circuit of a buck converter with all device package parasitic inductors highlighted. Typical turn-on switching waveforms under 400 V/5 A condition obtained from simulation are shown in Fig. 2.36. In the switching waveforms, the black, green, and purple curves are V_{GS}, V_{DS}, and I_{DS} respectively, which are the external waveforms of the cascode structure. Furthermore, the red and blue curves are V_{SD_Si} and V_{GS_GaN} respectively, which are inside the cascode structure.

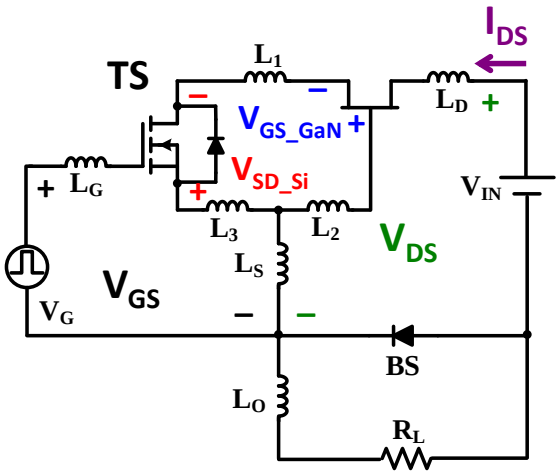
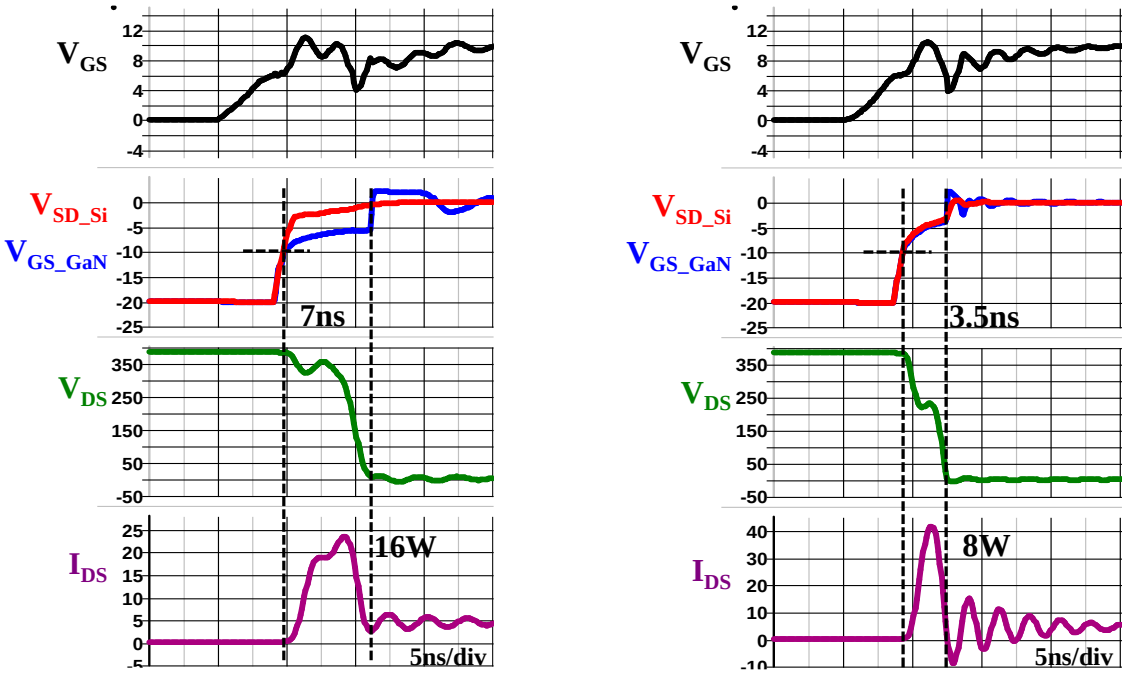


Fig. 2.35. Equivalent circuit of a buck converter with the cascode GaN HEMT



(a) (b)

Fig. 2.36. Turn-on waveform at 400V/4.5A (a) with package parasitic inductance, (b) without package parasitic inductance

As there is high di/dt existing in the high frequency commutation loop of the buck converter, during the turn-on transition time interval, significant voltage will be induced on L_{int1} and L_{int3}.

The essence of cascode structure is to control the GaN HEMT by controlling the Si MOSFET, or in other word, the blue curve should follow the change of the red curve. However, due to the induced voltage, the blue curve is not able to follow the red curve closely, and as a result, the GaN HEMT cannot turn on as fast as the turn-on of the Si MOSFET. Compared to the case without package parasitic inductance in Fig. 2.36(b), the main transition time and turn-on loss are increased from 3.5 ns to 7 ns and from 8 W to 16 W respectively. So the package influence in hard-switching turn on is significant turn-on loss increase.

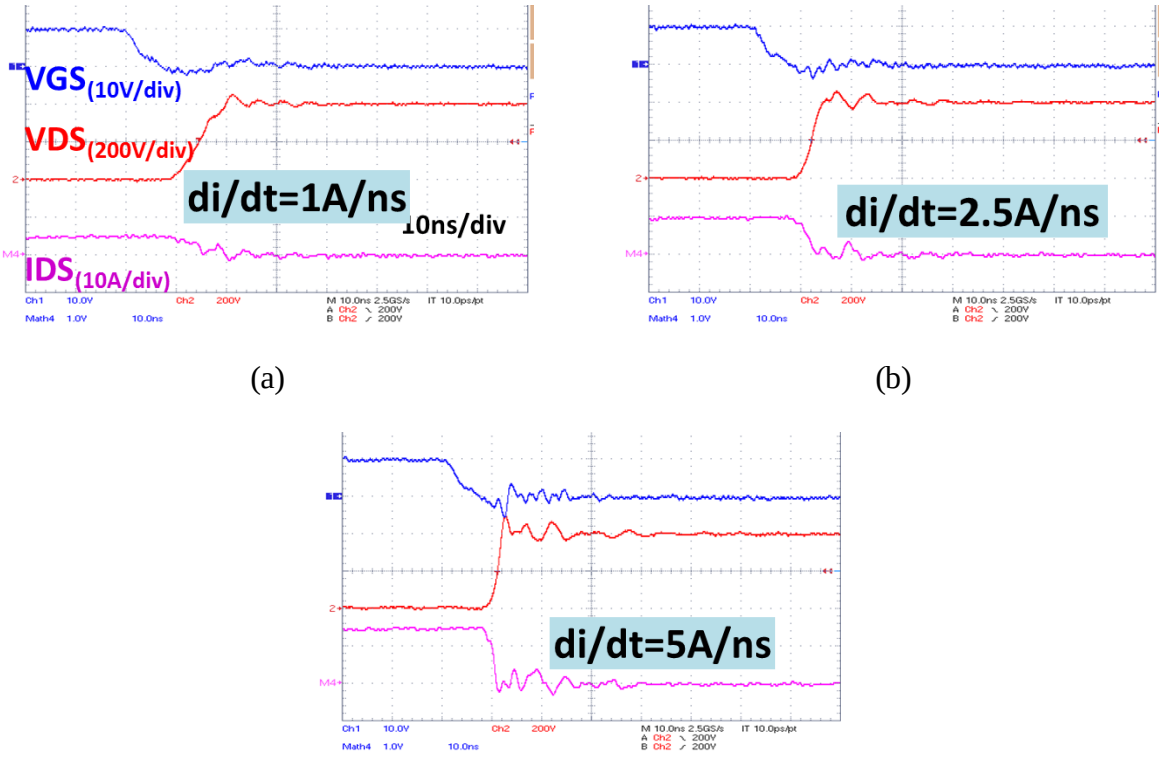
CRM soft switching can eliminates the high turn-on loss. However, even there is no issue from the point of loss, device failure is still observed at high current turn-off condition. Since di/dt increases with turn-off current quickly, the package effect will also be more significant.

Fig. 2.37 shows di/dt at different turn-off current. It is clearly that the di/dt increases quickly when the turn-off current increasing. At 15 A turn off condition, the di/dt achieves unprecedented 5 A/ns. And around this condition, device failure might be observed.

The reason for potential device failure is illustrated in Fig. 2.38, in which the black and red curve are V_{SD_Si} and V_{GS_GaN} respectively; while the green, gray, and blue curves are voltage induced on internal parasitic inductors L_{int1}, L_{int2}, and L_{int3} respectively.

$$V_{GS\_GaN} = V_{SD\_Si} + V_{Lint1} + V_{Lint2} + V_{Lint3} \tag{3.1}$$

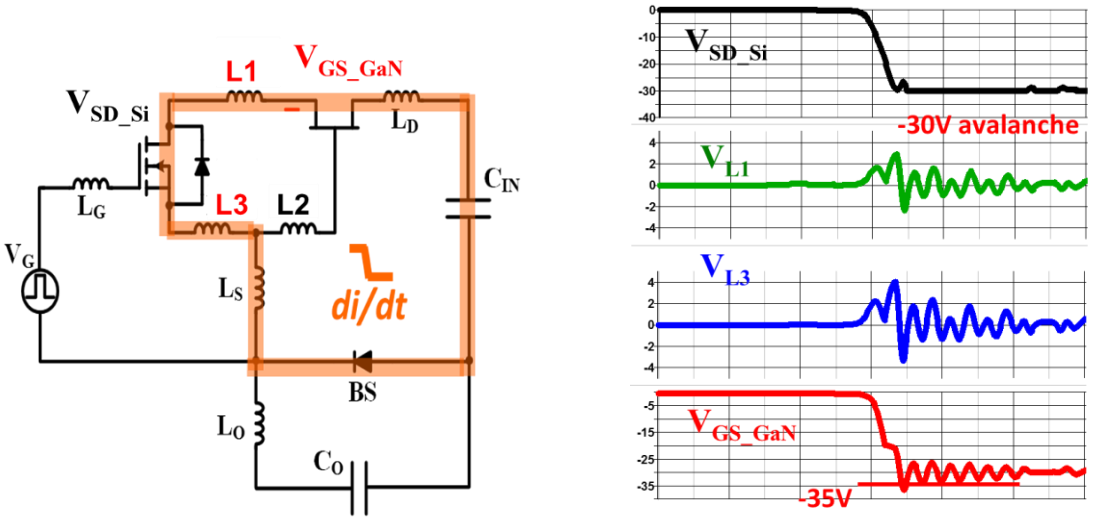
According to Kirchhoff's voltage law (KVL), V_{GS_GaN} should be the superposition of V_{SD_Si} with all voltage induced on the internal parasitic inductors as equation (3.1). So even V_{SD_Si} is clamped at -30 V due to the avalanche mechanism, V_{GS_GaN} is still vulnerable to high voltage spike. As shown in Fig. 2.38, the V_{GS_GaN} reaches -35 V.



(a) (b)

(c)

Fig. 2.37. Di/dt at different turn-off current (a) I_{OFF}=5A, (b) I_{OFF}=10A, (c) I_{OFF}=15A



(a) (b)

Fig. 2.38. Turn-off at 400 V/12 A (a) buck circuit schematic, (b) simulation waveform

So the package influence in hard-switching turn off is significant internal parasitic ringing which may cause device failure. For a robust design, the V_{GS_GaN} of GaN device requires more margin.

2.3.3 Package Improvement Method

Based on the analysis in last section, it is clear that the traditional package has significant side effect on the device switching performance. Since the most critical parasitic inductors had already be identified, the following package improvement will focus on eliminating pre-defined common-source inductance.

Four different packages for high voltage cascode GaN HEMT are shown in Fig. 2.39, in which the same GaN die and Si die are assumed. In Fig. 2.39(a) and (b), the TO-220 package and the PQFN package are industry common practice, while the PQFN plus package and the stack-die package are improved package based on previous analysis.

For the TO-220 package, as analyzed before, there are three common-source inductors existing, which are L_{int1}, L_{int3}, and L_S.

For the PQFN package, three leads are eliminated so that L_S is no longer existing. In addition, Kelvin connection is applied to provide a separate gate drive return loop. So for Si MOSFET, its power loop and driving loop are decoupled and no common-source inductance existing. However, the Kelvin connection can only affect Si MOSFET but have limited effect on GaN HEMT. From the prospective of GaN HEMT, L_{int1} and L_{int3} are shared by its power loop and driving loop. So they are still the common-source inductance for GaN HEMT.

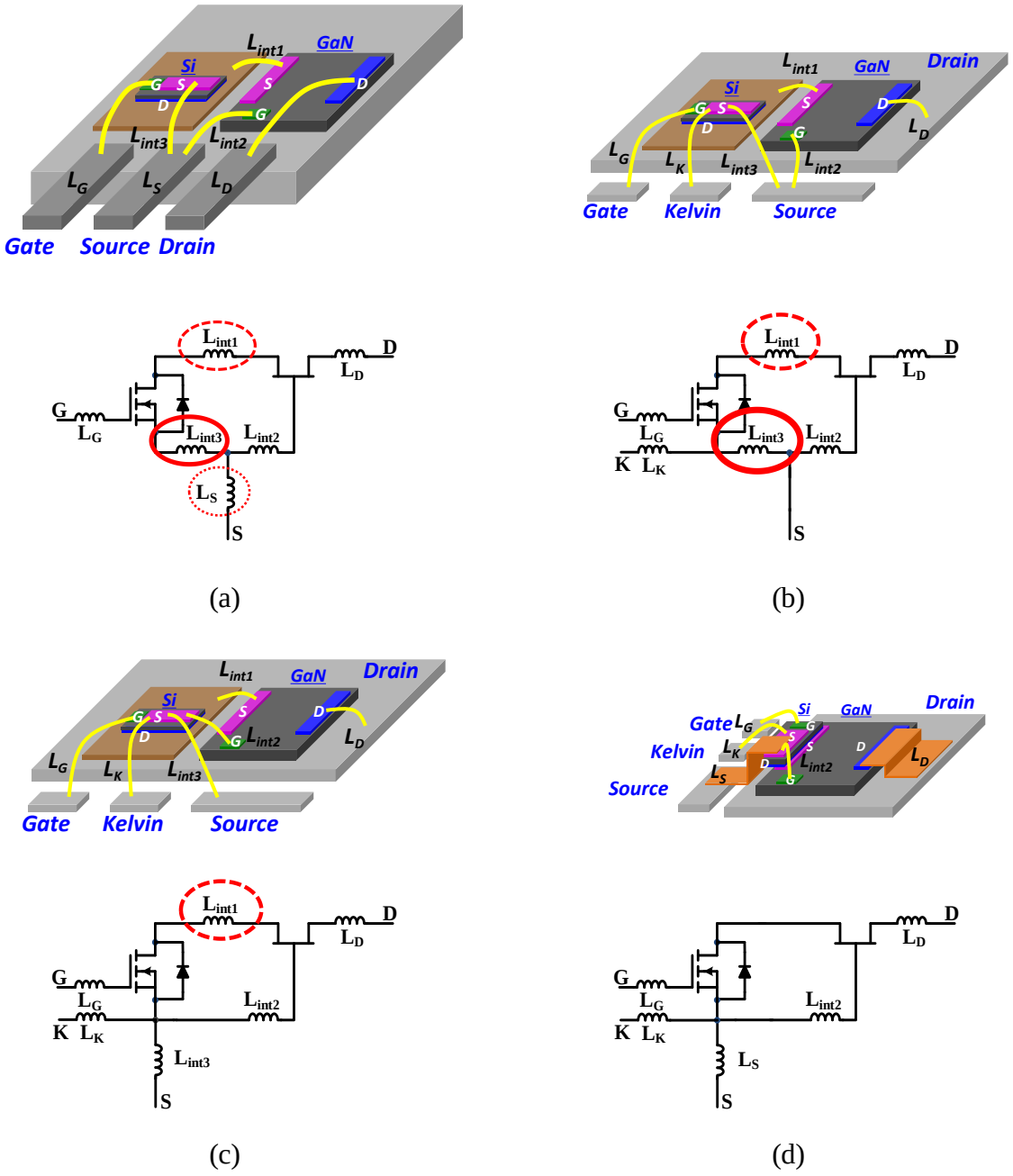


Fig. 2.39. Package bonding diagram and schematic for cascode GaN HEMT in different packages. (a) TO-220, (b) PQFN, (c) PQFN plus, (d) Stack-die

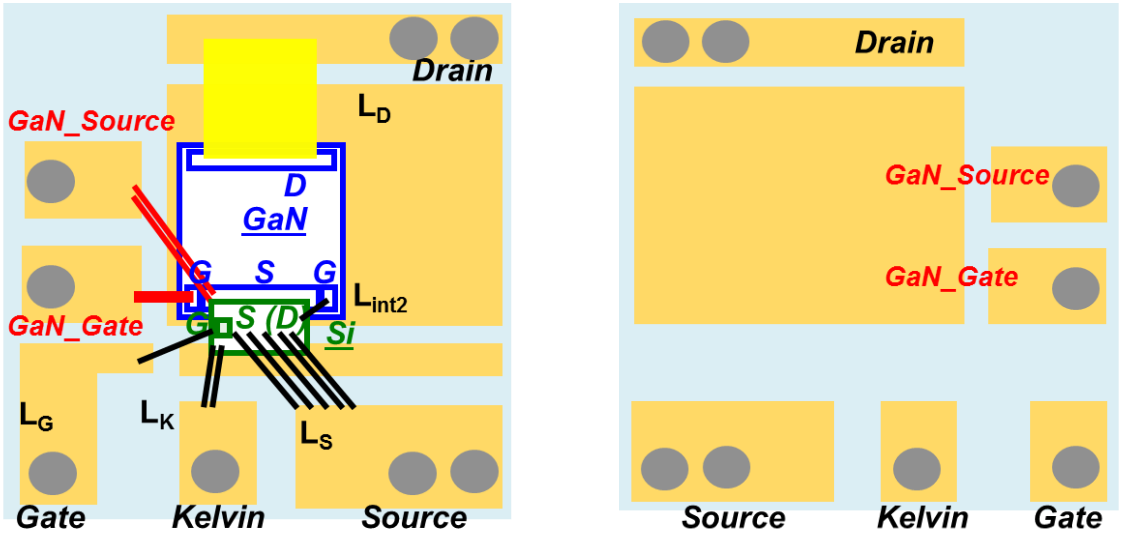
A simple but effective way to improve the cascode package is the PQFN plus package shown in Fig. 2.39(c). Comparing to traditional PQFN package, the major difference is redirecting bonding wire L_{int2}. The purpose of L_{int2} is to realize the connection between the gate pad of GaN

HEMT and the source pad of Si MOSFET. In PQFN package, one terminal of L_{int2} is on the gate pad of GaN HEMT while the other terminal is on the source pad of cascode device. With this arrangement, L_{int3} is included in the driving loop of GaN HEMT so that it becomes the common-source inductance of GaN HEMT. On the contrary, in PQFN plus package, one terminal of L_{int2} is still on the gate pad of GaN HEMT, while the other terminal is redirected to the source pad of Si MOSFET. In this way, the L_{int3} is excluded from the driving loop of GaN HEMT. Meanwhile, with Kelvin connection, it is also excluded from the driving loop of Si MOSFET. Finally, L_{int3} is no longer common-source inductance of this cascode device.

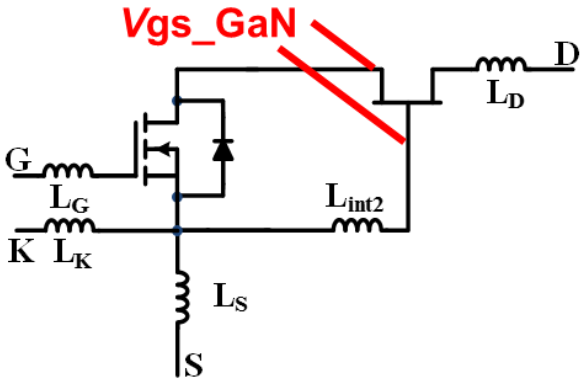
If maintaining Si MOSFET and GaN HEMT side-by-side configuration, further improvement beyond the PQFN plus package seems can hardly be achieved. In order to eliminate the last common-source inductance L_{int1}, the concept of stack-die configuration, which previously is used in the cascode package of SiC JFET and Si MOSFET [B.9], is a good candidate. As shown in Fig. 2.39(d), in the stack-die package of cascode GaN device, the Si MOSFET (drain pad) is mounted on top of the GaN HEMT (source pad) directly. With this stack-die package, there is no parasitic inductor shared by more than one loop, so all common-source inductances are eliminated. Thus the stack-die package is considered as the optimized package for cascode GaN device.

Among commercial GaN devices, there is a kind of advanced package introduced in [B.10] which makes the proprietary vertical structure GaN die embedded into a CMOS substrate, in which low voltage Si MOSFET and gate driver are all integrated. In this method, both external and internal parasitic inductance are minimized, and a fully integrated high-voltage cascode GaN HEMT with specifically designed gate driver is realized. However there are still at least two limitations to extend this method to other cases. First, the high voltage GaN HEMT is in proprietary vertical structure, while most popular high voltage GaN HEMT are usually in lateral structure.

Second, the low voltage Si MOSFET is based on many signal level MOSFETs in parallel not standard power MOSFET. As a comparison, the stack-die package proposed in this thesis is based on most common high voltage lateral GaN HEMT and low voltage vertical Si power MOSFET. So this method can solve the package related issue in general and be easily extended to other cascode GaN devices.



(a) (b)



(c)

Fig. 2.40. Design of stack-die package for cascode GaN HEMT (a) top view, (b) bottom view, and (c) schematic

Fig. 2.40 is the design for stack-die package prototype. The top view shows that the Si die is attached on the source pad of the GaN die directly. Then copper foil and bonding wires are both used to achieve necessary electrical connection. All external electrical terminals are clearly marked in which two pads for the gate terminal and the source terminal of the GaN die are purposely introduced so that the internal waveforms V_{GS} of the GaN HEMT can be measured through this package.

The designed stack-die structure has been packaged in a low profile format similar to the conventional PQFN package. As presented in Fig. 2.41, the packaged stack-die device can be easily surface-mounted on the testing board using solder reflow technique. The fabrication process includes two major steps: substrate preparation and device assembly.

Alumina direct bonded copper substrate (Al2O3 – DBC; Al2O3 15 mil, Cu 5mil) of high strength and good thermal conductivity was selected as the chip carrier for this power semiconductor assembly. Firstly, 1-mil thick adhesive Kapton® tape used as etching mask was covered the whole area on both top and bottom Cu surfaces of the DBC substrate. After laser patterning, the attached tapes were selectively removed according to the substrate layout. The exposed Cu areas have been then etched off by ferric chloride solution to form the circuitry. Multiple through holes were drilled on the developed Cu pads using the same CO2 laser machine. A picture of the substrate after laser drilling process is illustrated in Fig. 2.42(a). Next, the plasma-cleaned top Cu pads have been electro-plated by nickel (Ni) and gold (Au) successively, which helps to avoid the surface oxidation and facilitates further die-attachment and wire-bonding. The thickness of the Au finish surface is in the range of 20 to 30 μm. Subsequently, mounting pins with 0.5 mm diameter (head diameter of 1 mm) were inserted to the drilled through holes and firmly connected to both Au plated Cu surface pads by a solder reflow process using a lead-free solder

paste (Sn89Sb10.5Cu0.5, solidus temperature of 242°C). The extra parts of soldered pins were truncated and ground to be flush with the bottom surface of the substrate, as shown in Fig. 2.42(b). The prepared DBC substrate has been cleaned once again for the following device assembly step.

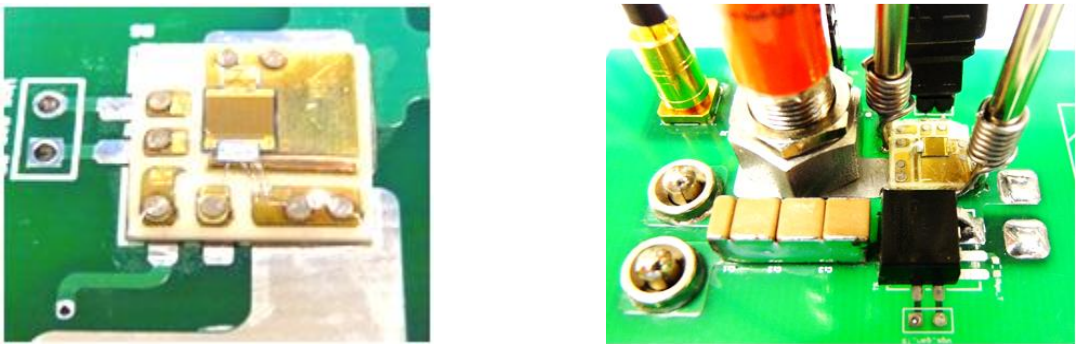
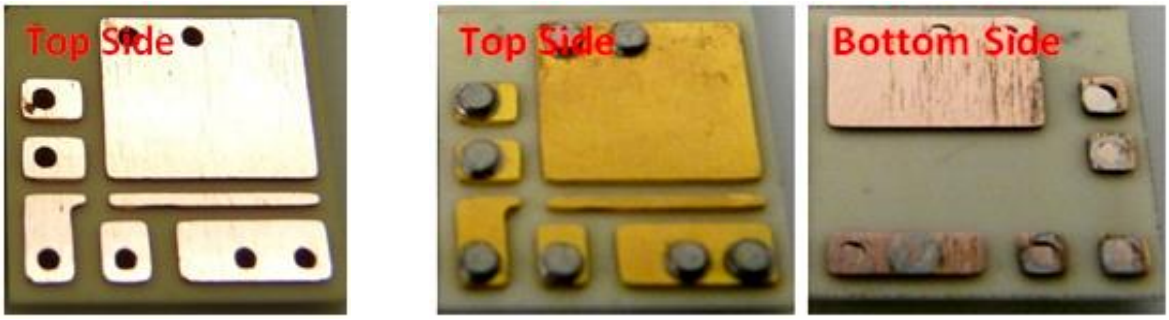


Fig. 2.41. Packaged stack-die device mounted on the double-pulse tester board with transparent silicone elastomer glob-top encapsulation



(a) (b)

Fig. 2.42. Patterned Al_2O_3 – DBC substrate: (a) top surface pads after etching and laser drilling, (b) electro-plated Au top surface with soldered pins and ground bottom surface

A 600 V GaN HEMT and a 30 V Si MOSFET bare dies were selected for the stack-die device assembly. The GaN die and a Cu spacer of the same thickness as GaN were first soldered on the substrate. The Cu spacer has been used in order to level the position of Si device mounted directly on GaN device. A solder mask protecting the channel area was applied on the top surface of GaN die with only source and drain pads uncovered. Then, the Si die was soldered on top of the GaN

die. The solder joint links the drain terminal of Si MOSFET to the source terminal of GaN HEMT without wire-bonding. A cut Cu foil (0.2 mm) with Au plating was also soldered simultaneously to make an electrical connection between GaN's drain terminal and the corresponding area on the DBC substrate. The solder paste used in this process is in lead-tin (Pb-Sn) eutectic composition which has a lower melting point of 183°C compared to the one used for the connection pin soldering. After device soldering, 2-mil aluminum (Al) wires were bonded between semiconductors and the electrical pads on the DBC substrate. The gate, Kelvin, and source electrodes on the substrate were wire bonded to the Si MOSFET and additional Al wires for GaN signal sensing were also bonded on the GaN device. Epoxy molding compound or silicone elastomer (as glob-top) was finally applied to encapsulate the packaged stack-die device for electrical/chemical protection and easy handling.

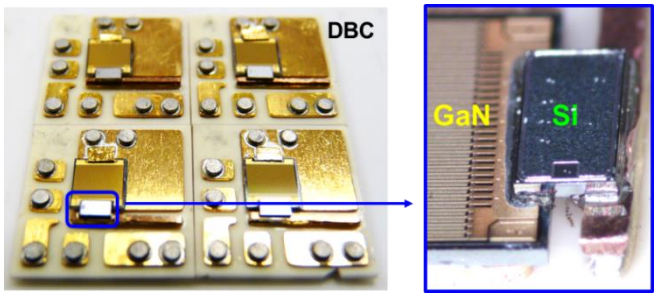


Fig. 2.43. Die attachment

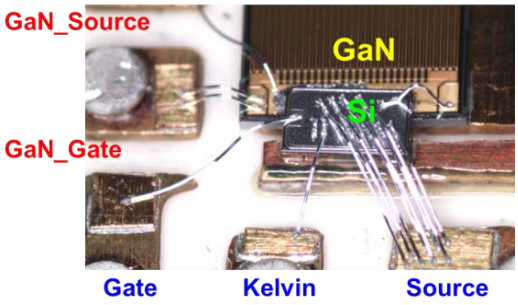
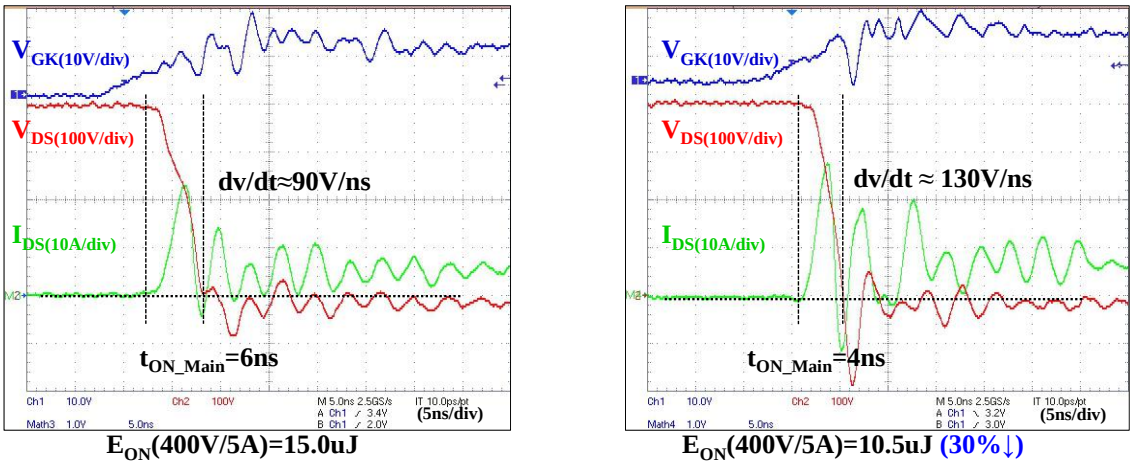


Fig. 2.44. Wire bonding process

2.3.4 Evaluation of GaN HEMT in Stack-Die Package

The performance of high-voltage cascode GaN HEMT in stack-die package is evaluated by comparing with a commercial product in TO-220 package. Both of them include the same GaN die and Si die, while the difference is method of packaging. Experimental result shows that the stack-die package has improvement in both hard-switching turn on and turn off.



(a) (b)

Fig. 2.45. Turn-on waveform comparison (a) TO-220 package, (b) stack-die package

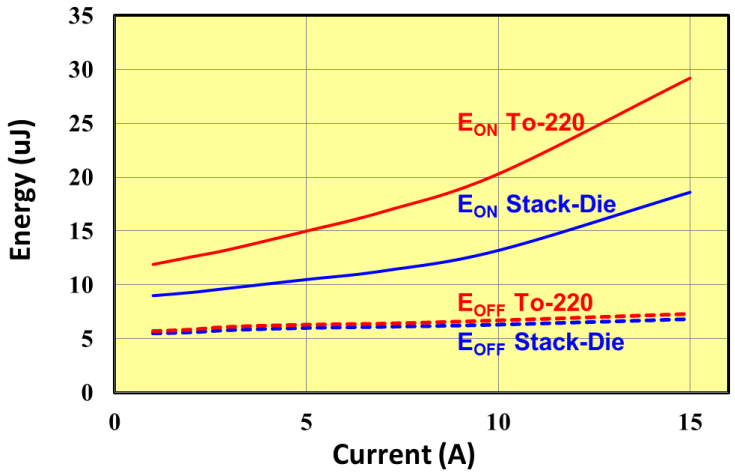


Fig. 2.46. Switching energy comparison for different packages

The two devices are tested under the same double-pulse tester setup in Chapter 2. Fig. 2.45 shows the turn-on waveforms at 400 V/5 A condition. In accordance with previous analysis, the stack-die package has faster switching transition speed compared to the TO-220 package. The dv/dt is increased from 90 V/ns to 130 V/ns, while the main transition time and turn-on switching energy is reduced from 6 ns and 15.0 uJ to 4 ns and 10.5 uJ respectively. 30% turn-on energy is saved at this condition.

Fig. 2.46 is the measured switching energy at different load current conditions. In all load range, the turn-on energy of the stack-die package is reduced significantly.

For the test under high current hard-switching turn off condition, the internal waveform V_{GS_GaN} in traditional package cannot be measured. So simulation model is used again in there to predict the internal waveform. Fig. 2.47 shows the simulated V_{GS_GaN} for different packages.

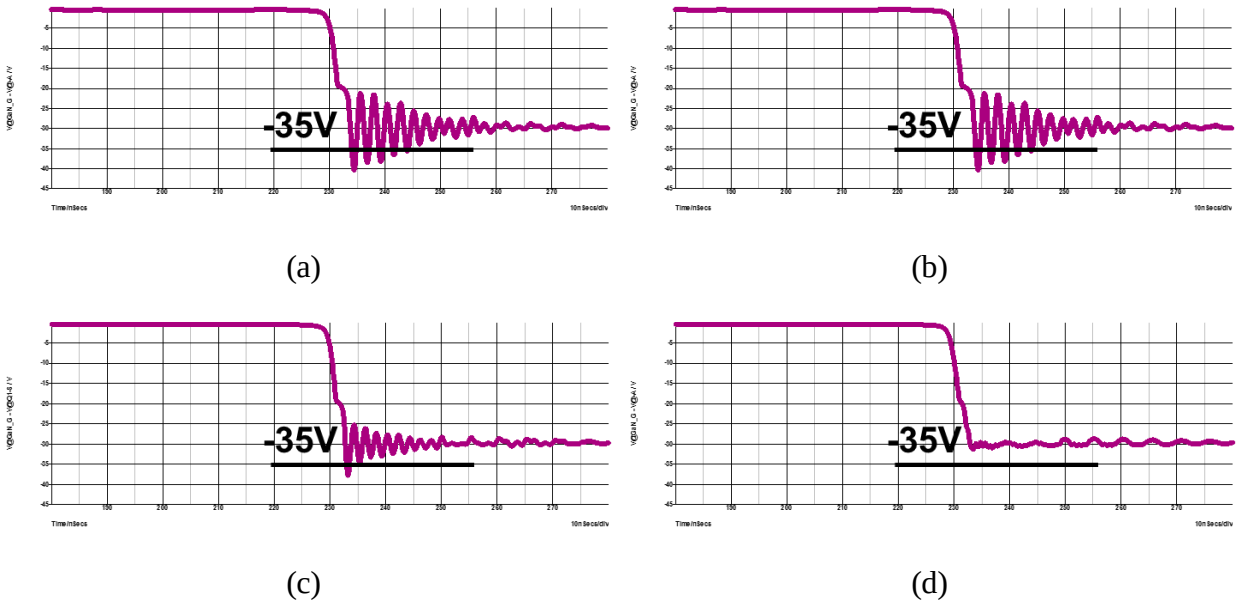


Fig. 2.47. Simulated V_{GS_GaN} for (a) TO-220, (b) PQFN, (c) PQFN plus, (d) stack-die

The simulated turn-off waveforms are under 400 V/15 A turn-off condition. It is clear that for TO-220 and PQFN, the parasitic ringing is likely to hit -40 V, which is far below -35 V. Between TO-220 and PQFN, there is no much difference because their internal bonding wire structure are very similar. So simply eliminating external through leads doesn't affect internal parasitic ringing.

For proposed PQFN plus package, since L_{int3} is no longer common source inductance and has no effect on the internal GaN driving loop, the parasitic ringing is reduced. However, for all these three cases, V_{GS_GaN} over -35 V is observed and if there is enough energy applied on the gate terminal of the GaN die, the parasitic ringing possibly cause device failure.

According simulation, the proposed stack-die package is able to solve the parasitic ringing effectively as shown in Fig. 2.47(d). The V_{GS_GaN} is well clamped at -30 V through Si avalanche breakdown mechanism protection.

With proposed stack-die package, the internal waveform is able to be measured. Fig. 2.48 is the measured turn-off waveforms of stack-die package under 400 V/15 A condition. The purple curve shows that V_{GS_GaN} is clamped at -30 V, while no voltage overshot occurs. The experimental waveform is a strong evidence that the proposed stack-die package for cascode GaN is very helpful to improve the stability of the GaN device.

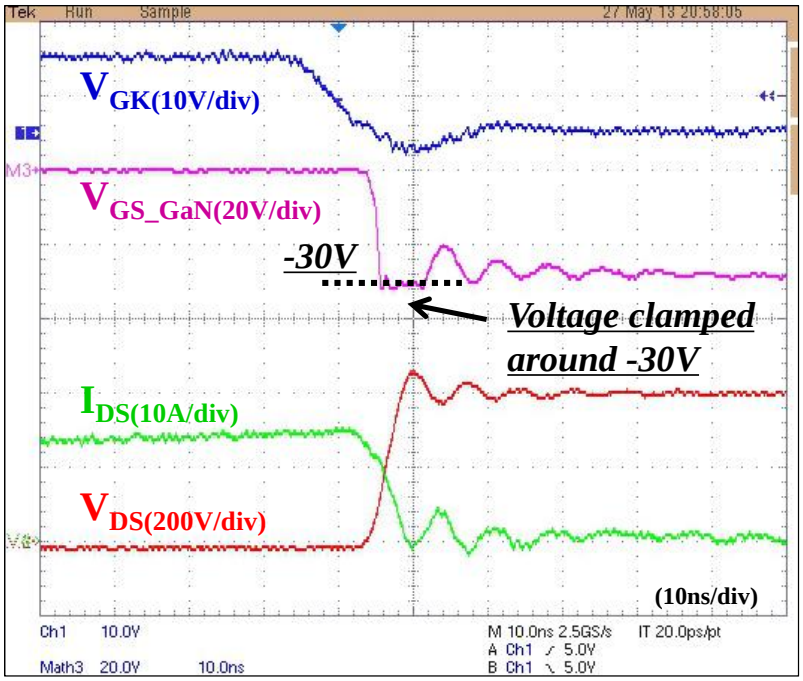


Fig. 2.48. Turn-off waveform of stack-die package

In summary, the high-voltage cascode GaN HEMT enables higher switching transition speed compared to traditional Si MOSFET and leads to great challenge for device package design. Traditional package is already a limitation to realize the promising performance of the GaN HEMT. To solve this issue, a stack-die package for the cascode GaN HEMT is introduced which eliminates

all package related common-source inductances, and thus, improves the device switching performance and stability significantly and makes the device more suitable for MHz high frequency operation.

Chapter 3. Application of GaN for PFC above MHz

With the advent of 600 V gallium-nitride (GaN) power semiconductor devices, the totem-pole bridgeless power factor correction (PFC) rectifier, which was a nearly abandoned topology, has suddenly become a popular solution for applications like front-end converters in server and telecommunication power supplies. This is mostly attributed to the significant performance improvement of the GaN high-electron-mobility transistor (HEMT) compared to the silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET), particularly its better figure-of-merit and significantly smaller body diode reverse-recovery effect.

The benefits of the GaN-based hard-switching totem-pole PFC rectifier is demonstrated in recent literature [C.1]-[0.6]. As the reverse-recovery charge of the GaN HEMT is much smaller than that of the Si MOSFET, hard-switching operation in totem-pole bridge configuration is practical. By limiting the switching frequency to be around or below 100 kHz, the efficiency could be above 98% for a 1 kW level single-phase PFC rectifier. Even though the simple topology and high efficiency are attractive, the system-level benefit is limited because the switching frequency is still similar to that of Si-based PFC rectifiers.

Previous studies show soft switching truly benefits the cascode GaN HEMT [C.7]-[C.10]. As the cascode GaN HEMT has high turn-on loss and extremely small turn-off loss due to the current-source turn-off mechanism [C.8], critical mode (CRM) operation is very suitable. A GaN-based critical mode (CRM) boost PFC rectifier has been demonstrated which exhibits the high-frequency capability of the GaN HEMT and shows it has significant benefits, as the volume of both the boost inductor and the DM filter are dramatically reduced [C.11], [C.12].

With a similar system-level vision, the cascode GaN HEMT is applied in the totem-pole PFC rectifier while pushing the operating frequency to above 1 MHz [C.13]-[C.15]. Several important issues, which are less significant at low frequencies, are emphasized at high frequencies, and corresponding solutions are proposed and experimentally verified.

The bridgeless PFC rectifier has clear advantages [C.16], [C.17] because it eliminates the diode rectifier bridge so that the conduction loss of the power semiconductor devices is reduced. Among different boost-type bridgeless PFC rectifiers, the dual-boost bridgeless PFC rectifier is popular in industry products because it has less conduction loss than boost PFC rectifiers; lower common-mode (CM) noise compared to conventional bridgeless boost PFC rectifiers; and only a low-side gate driver, rather than the high-side floating gate driver required by other rectifiers. However, in terms of topology, the totem-pole PFC rectifier is even simpler than the dual-boost bridgeless PFC rectifier. Performing a side-by-side comparison using Fig. 3.1 and Table 3.1, we see that the totem-pole PFC rectifier eliminates the usage of the silicon-carbide (SiC) Schottky diode and requires only four switches and one inductor. Therefore it is the most simplified topology among the boost-type bridgeless PFC rectifiers.

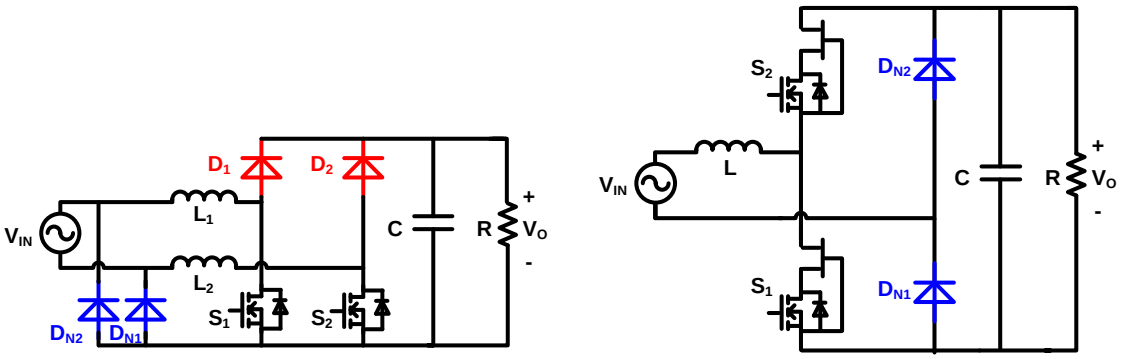


Fig. 3.1. Comparison between (a) Dual-boost bridgeless PFC rectifier and (b) Totem-pole bridgeless PFC rectifier

Table 3.1. Component count of dual-boost bridgeless PFC rectifier and totem-pole bridgeless PFC rectifier

	Dual-boost PFC	Totem-pole PFC
Active switch	2 (S_1/S_2)	2 (S_1/S_2)
SiC Schottky diode	2 (D_1/D_2)	0
Rectifier diode	2 (D_{N1}/D_{N2})	2 (D_{N1}/D_{N2})
Total switch count	6	4
Inductor count	2	1

Even though the topology of the totem-pole PFC rectifier is very simple, it is seldom used due to significant drawbacks that cannot be overcome by using a Si MOSFET. If used with continuous-current mode (CCM) hard-switching operation, it can hardly work because there is tremendous turn-on loss and parasitic ringing due to the reverse-recovery effect of the anti-parallel body diode. Use of the CRM totem-pole PFC has been reported in literature [C.19]-[C.22], and although the previous issue is alleviated by ZCS turn-off of the body diode and ZVS turn-on of the control switch, the increased current ripple still leads to higher conduction loss and higher turn-off loss. So the Si-based CRM mode totem-pole PFC rectifier is usually limited to applications that use low frequencies and a low power level.

The high-voltage GaN HEMT is able to extend the application of the totem-pole PFC rectifier. The significantly reduced reverse-recovery charge of the cascode GaN HEMT makes CCM operation practical within a certain frequency range (e.g. 50 kHz or 100 kHz). Furthermore, the turn-off loss of the cascode GaN HEMT is extremely small, so with CRM operation the switching frequency is able to be pushed to above 1 MHz while achieving good efficiency.

Fig. 3.2 shows the switching loss distribution of several GaN device samples. The switching loss are tested under similar double-pulse tester setup discussed in [C.8], [C.9]. The PCB layout

has minimized power loop and driving loop to achieve low parasitic inductance. 0 Ω external gate driving resistor is used to achieve fast possible switching transition speed. The energy stored in the output junction capacitor (E_{OSS}) is calculated according to turve tracer tested C_{OSS}-V_{DS} curve. For the testing results, the E_{OSS} is included in E_{off}. However, the E_{OSS} is actually dumped during turn-on transition. Therefore E_{OSS} is subtracted from E_{off} and added to Eon in the date post-process to reflect more accurate switching loss distribution.

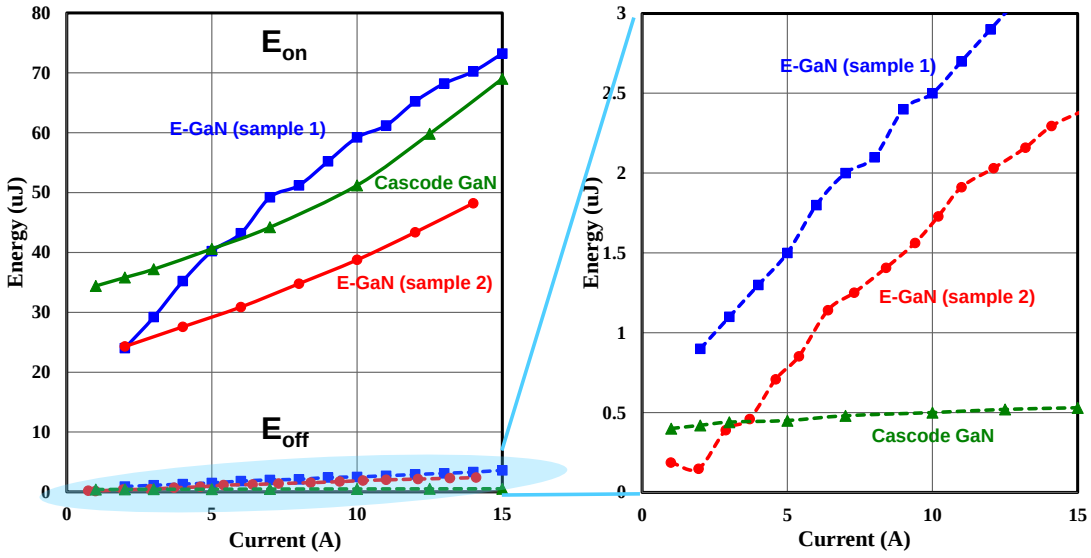


Fig. 3.2. Measured switching loss distribution of different GaN device samples

Fig. 3.2 exhibits that for both e-GaN and cascode GaN the turn-on loss is significantly larger than the turn off loss. The major reason is reverse recovery charge or junction capacitor charge induced high current spike during turn-on transition. In addition, when the E_{off} part is enlarged, the dashed green curve shows that the cascode GaN has small and relative flat turn off loss. It has clear advantage if it operates at high turn-off current. The insight of this phenomenon is already illustrated in [C.8], [C.9] which is a unique current-source turn off mechanism brought by cascode structure.

When traditional design approach applied to GaN-based totem-pole PFC operating at CCM hard switching condition, the significantly large turn-on loss is the bottle neck to pursue high frequency with reasonable efficiency target. As demonstrated in [C.1], [0.6], 99% efficiency is achieved at 50 kHz or 100 kHz but there is very limited system level benefits compared to Si-based design.

Based on the tested switching characteristic of GaN devices, soft switching is preferred in order to dramatically increase the switching frequency without efficiency reduction. Simple CRM soft switching operation is adopted which demonstrates superior advantages in [C.7]-[C.10]. Furthermore, a MHz CRM boost PFC rectifier was demonstrated with 98% peak efficiency. Hence the MHz totem-pole PFC is also designed in CRM and the following sections focus on detailed design considerations.

3.1 Modified CRM for Achieving ZVS

The CRM PFC rectifier utilizes the resonance between the inductor and the device junction capacitors to achieve ZVS or valley-switching [C.18]. For boost-type CRM PFC rectifiers, ZVS can be achieved only when the input voltage is lower than one-half of the output voltage, assuming a negligible damping effect, which is often true with good design and limited resonant cycles. Thus when the input voltage is higher than one-half of the output voltage, the drain-source voltage can only resonate to a valley point which is equal to ($2V_{in}$-V_o), so ($0.5CV^2$) loss occurs at the following turn-on instant.

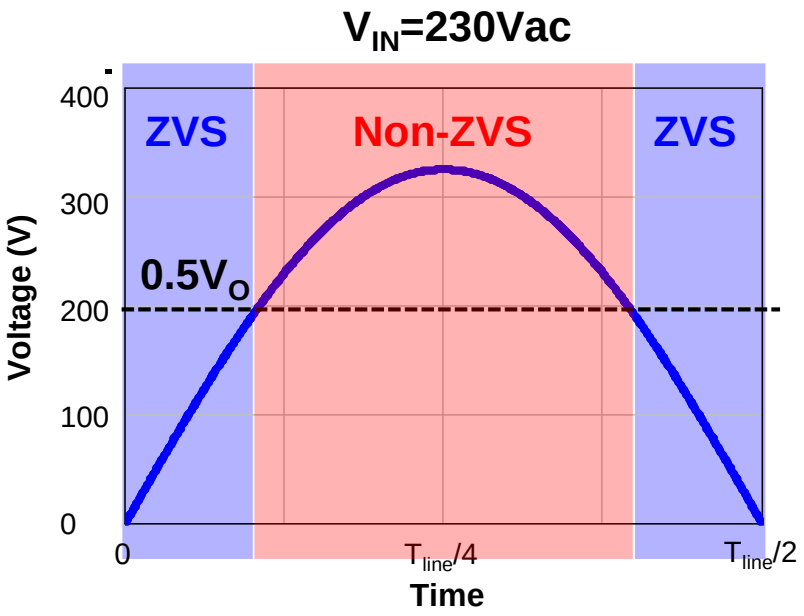
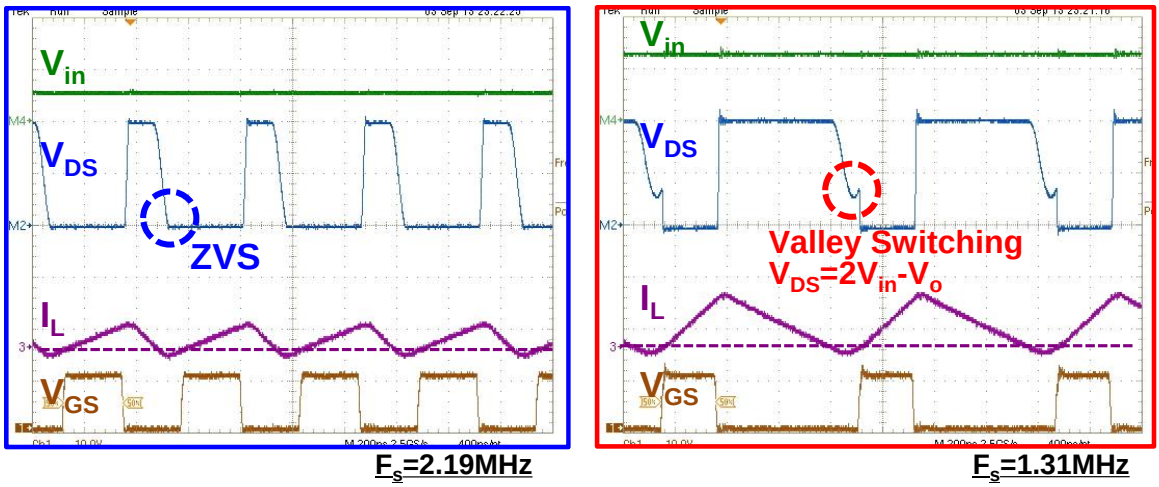


Fig. 3.3. ZVS and non-ZVS region in half lien cycle with 230Vac input an d400Vdc output



(a) (b)

Fig. 3.4. Zoom-in switching cycle waveforms in (a) ZVS and (b) non-ZVS conditions

The non-ZVS energy of each valley point switch is calculated at each operating point of a half-line cycle according to (3.1). Then the non-ZVS loss in a half-line cycle is also derived as the

product of non-ZVS energy and the switching frequency according to (3.2). The final step is to average the line-cycles so that the line-cycle averaged non-ZVS loss at different input voltages is calculated according to (3.3). Fig. 3.5 illustrates the calculation process.

$$E_{oss}(V_{in}, t) = \begin{cases} 0 & (V_{in} \le 0.5V_o) \\ 0.5C_{OSS}(2\sqrt{2}V_{in}\sin\omega t - V_o)^2 & (V_{in} > 0.5V_o) \end{cases} \quad (3.1)$$

$$P_{oss}(V_{in}, t) =$$

$$\begin{cases} 0 & (V_{in} \le 0.5V_o) \\ 0.5C_{OSS}(2\sqrt{2}V_{in}\sin\omega t - V_o)^2 f_s(V_{in}, t) & (V_{in} > 0.5V_o) \end{cases} \quad (3.2)$$

$$P_{oss\_ave}(V_{in}) = \frac{[\int_t^{t+T_{line}} 0.5C_{OSS}(2\sqrt{2}V_{in}\sin\omega t - V_o)^2 f_s(V_{in}, t)]}{T_{line}} \quad (3.3)$$

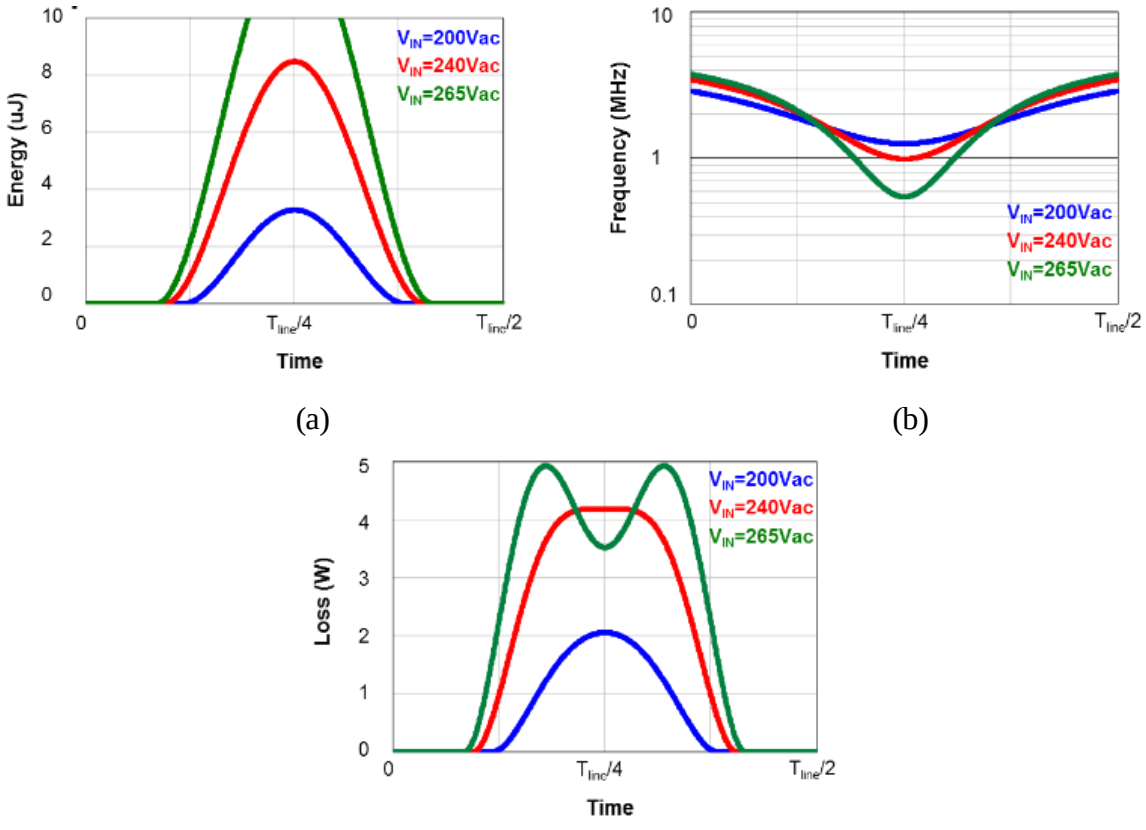


Fig. 3.5. Calculation process of non-ZVS loss (a) Non-ZVS energy distribution; (b) Frequency distribution; and (c) Non-ZVS loss distribution

As this loss is directly related to the switching frequency, when the frequency is pushed to the multi-MHz level, the non-ZVS loss is significant and dominant in the total converter loss, as shown in Fig. 3.6.

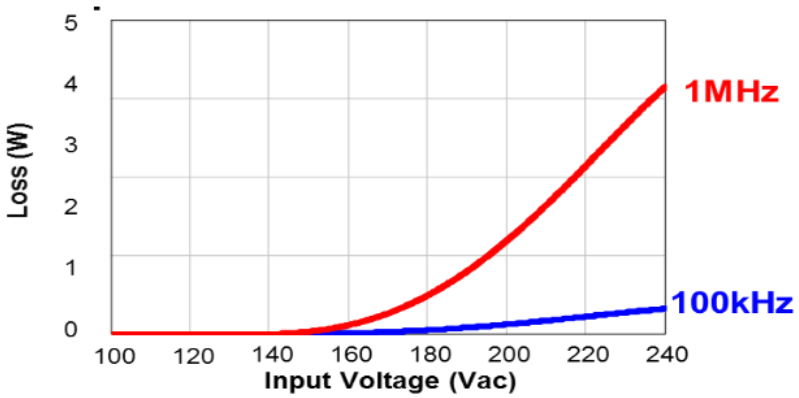


Fig. 3.6. Line-cycle averaged non-ZVS loss vs. input voltage

In order to solve this issue, the ZVS extension strategy explained in [C.19]-[C.22] is used. The concept is to modify the operation from CRM to quasi-square-wave (QSW) mode. Hence instead of turning off the synchronous rectifier (SR) right before the inductor current crosses zero, a short delay time is purposely added so that there is enough initial energy stored in the inductor to help achieve ZVS after the SR is turned off.

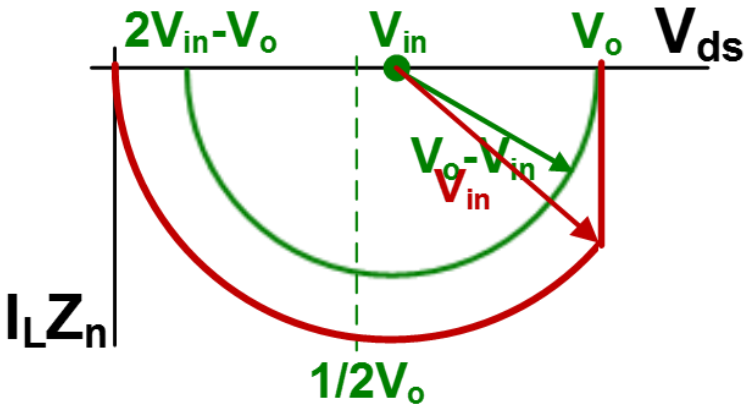


Fig. 3.7. Trajectory of resonance for CRM and QSW operations

The control of the ZVS extension is critical because if there is too much extra SR on-time, then there would be more circulating energy, increased current ripple and increased conduction loss; on the other hand, if there is not enough SR extra on-time, then ZVS cannot be achieved. To ensure an accurate calculation, a trajectory analysis (Fig. 3.7) is used which clearly illustrates the resonant status for CRM and QSW modes.

According to the trajectory, the minimum required negative current to achieve ZVS is calculated as (3.4). Then the required extra SR conduction time is further calculated with (3.5) in order to achieve the desired negative current. The calculation results are illustrated in Fig. 3.8. Within the two dashed lines is the non-ZVS zone, which requires ZVS extension control.

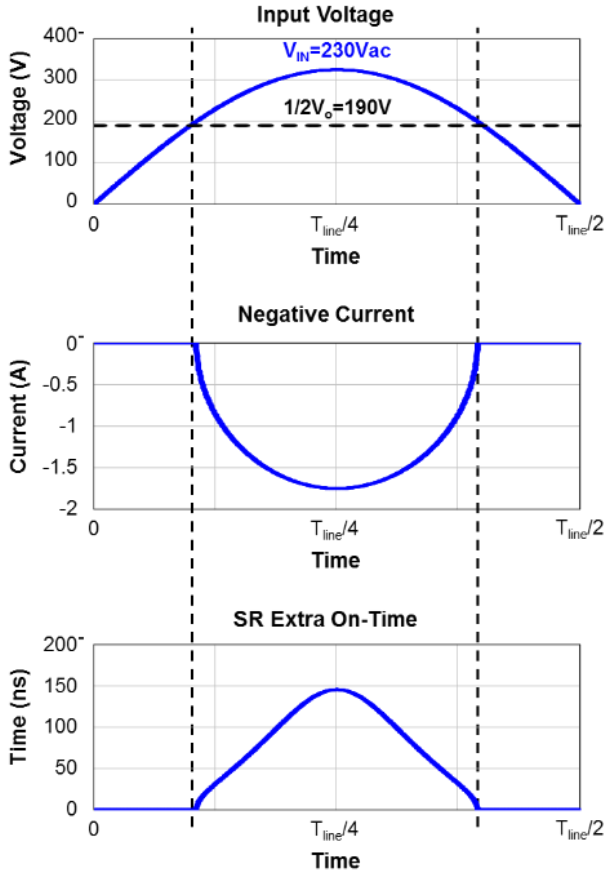
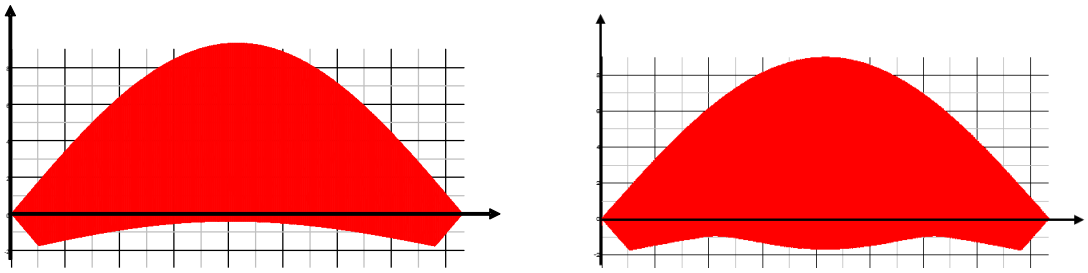


Fig. 3.8. Minimum negative current and SR extra on-time in half-line cycle to achieve ZVS extension

To further explore this ZVS extension control method, Fig. 3.9 shows the simulated half-line cycle inductor current without and with ZVS extension, while the experimental waveforms (Fig. 3.10 and Fig. 3.11) with entire line-cycle ZVS validates the ZVS extension strategy. The saved switching loss is significant because the total efficiency is increased by 0.3% to 1% from full load to half load, which is shown in later section.

$$i_{min}(t) = \frac{\sqrt{[2V_{in}(t)-V_o]V_o}}{\sqrt{L/2C_{oss\,(tr)}}} \tag{3.4}$$

$$t_{SR\_extra}(t) = \frac{L\sqrt{[2V_{in}(t)-V_o]V_o}}{[V_o-V_{in}(t)]\sqrt{L/2C_{oss(tr)}}} \tag{3.5}$$



(a) (b)

Fig. 3.9. Half-line cycle inductor current simulation waveforms (a) Non-ZVS and (b) With ZVS extension

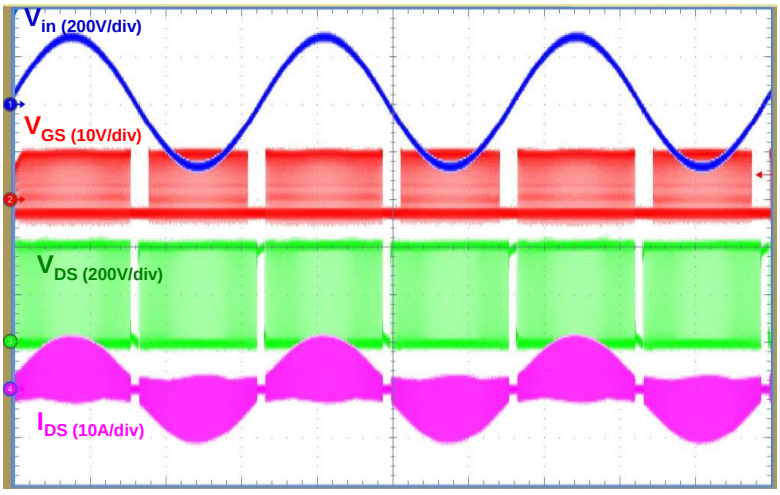
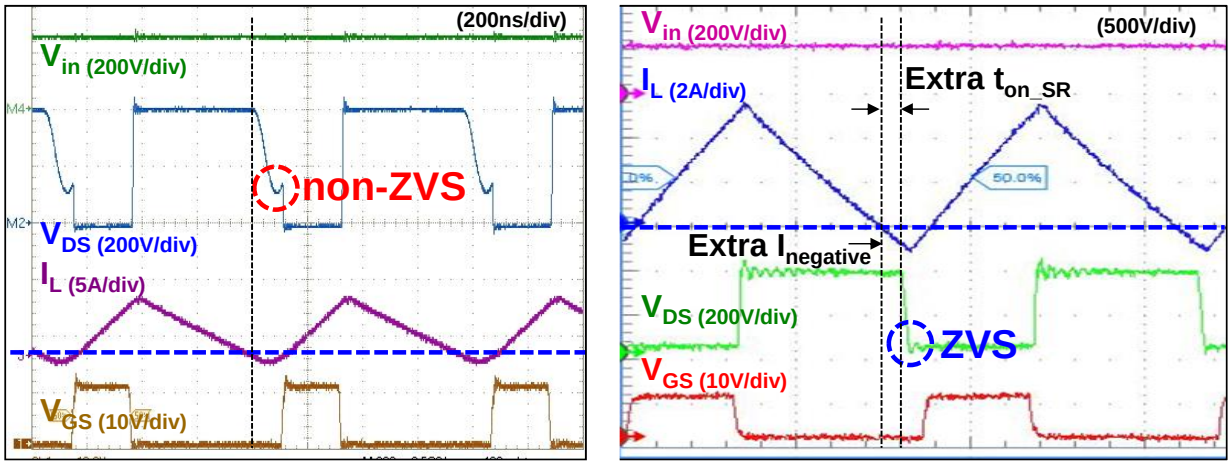


Fig. 3.10. Experimental line cycle waveforms with ZVS extension

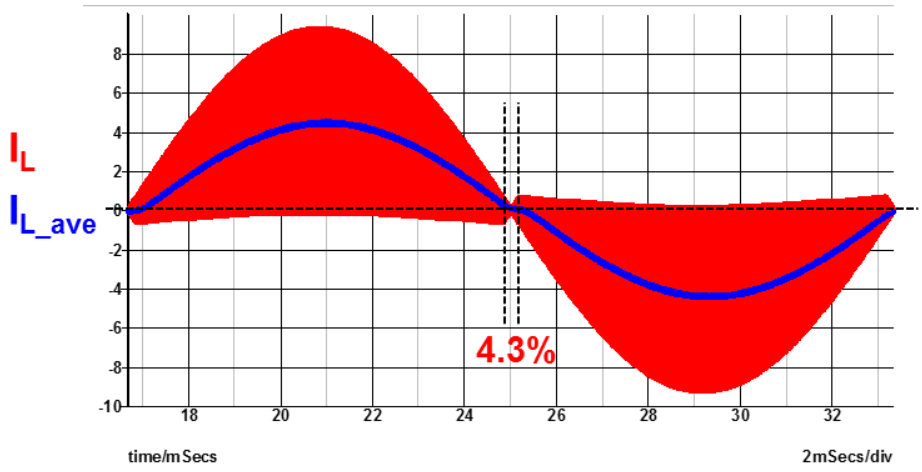


(a) (b)

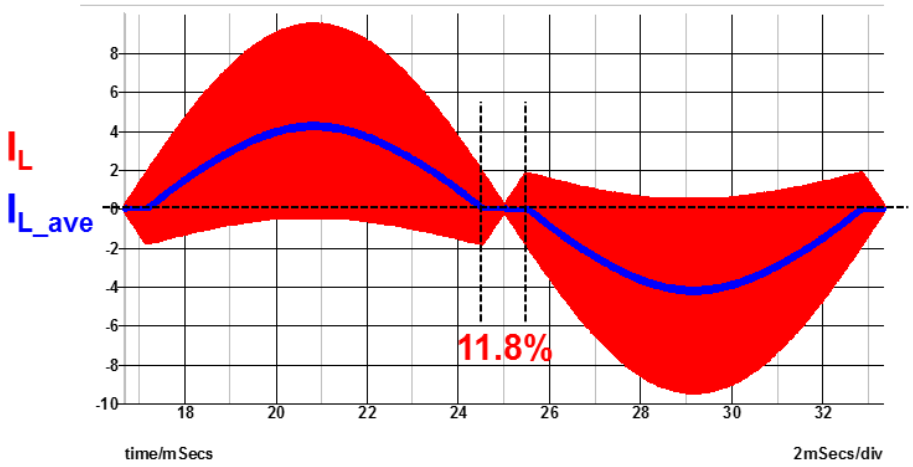
Fig. 3.11. Experimental waveform comparison of (a) Non-ZVS operation and (b) ZVS achieved after ZVS extension

3.2 Programmed On-Time to Reduce THD

The second high-frequency issue is related to the power quality and harmonics emission. Ideally, the CRM-mode PFC offers unity power factor with voltage mode (constant on-time) control. Since the on-time is constant, the envelope of the inductor peak current follows the shape of the input voltage. Then, if ignoring the negative current, the peak current of the inductor is always twice the average current, which means the input current always follows the shape of the input voltage. However, when the frequency is increased to the MHz range, the negative current during the resonant period is not negligible; thus there is a notable difference between the shape of the peak inductor current and the average inductor current. In addition, there is also a non-energy transfer time around the time the line voltage crosses zero in which the average inductor current is zero. Both of these lead to increased harmonics and a poor power factor, as shown in Fig. 3.12 and Fig. 3.13.



(a)



(b)

Fig. 3.12. Frequency impact on power factor and harmonics (a) 100 kHz constant on-time CRM PFC and (b) 1 MHz constant on-time CRM PFC

Variable on-time control is introduced in [C.23]. A similar concept is used in this paper but with improved and more accurate implementation by using digital control in order to solve the problems of increased harmonics and a poor power factor.

To realize the proposed control functions, microcontroller based digital control implementation is used. Therefore, an accurate mathematical model [C.24] to calculate detailed operation status is required. The mathematical model development process is elaborated in this section.

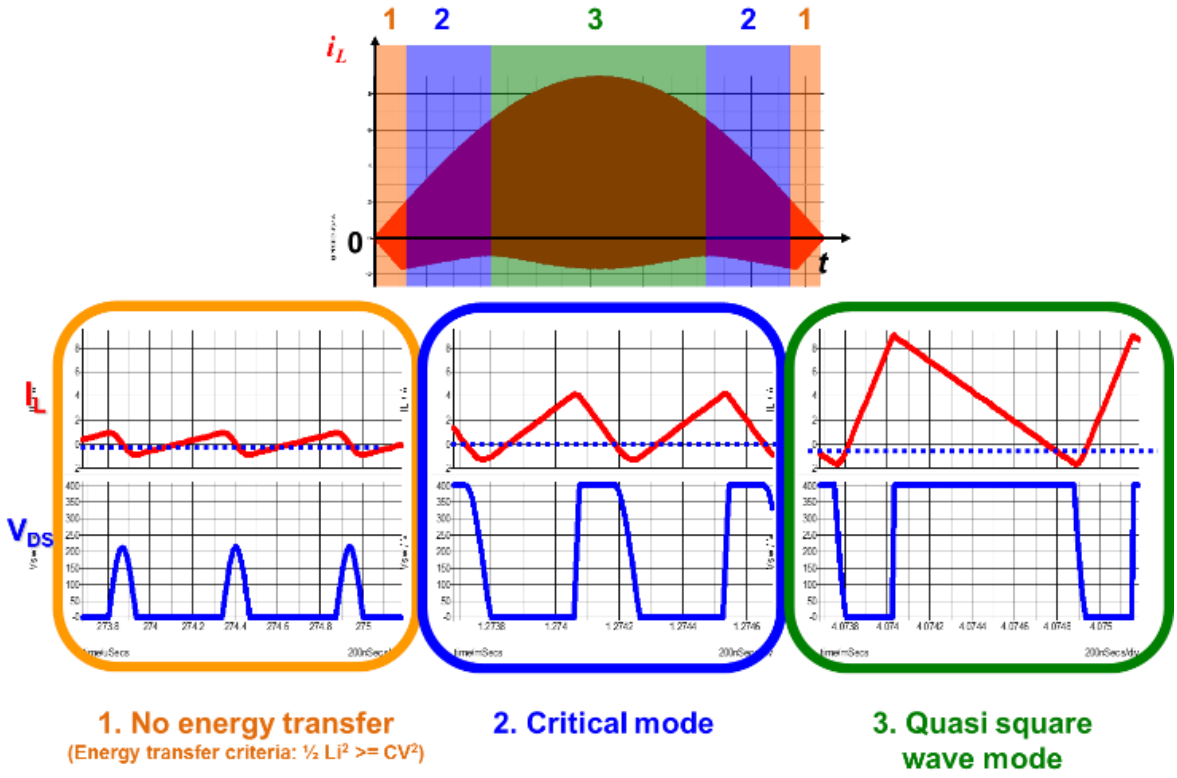


Fig. 3.13. Three operation modes in half-line cycle with voltage-mode constant on-time operation

3.2.1 Operation Mode Analysis

The topology is redraw in figure below including the equivalent output junction capacitor of each cascode GaN HEMTs, which plays an important role in operation analysis. Within this topology, S1 and S2 are cascode GaN HEMTs with Si MOSFET body diode (BD1 and BD2) and equivalent output junction capacitor (Co1 and Co2), operating at MHz switching frequency. SN1 and SN2 are Si MOSFET operating at line frequency. VIN is the input voltage source. L is the inductor. C is the output capacitor. R is the load with output voltage Vo across it.

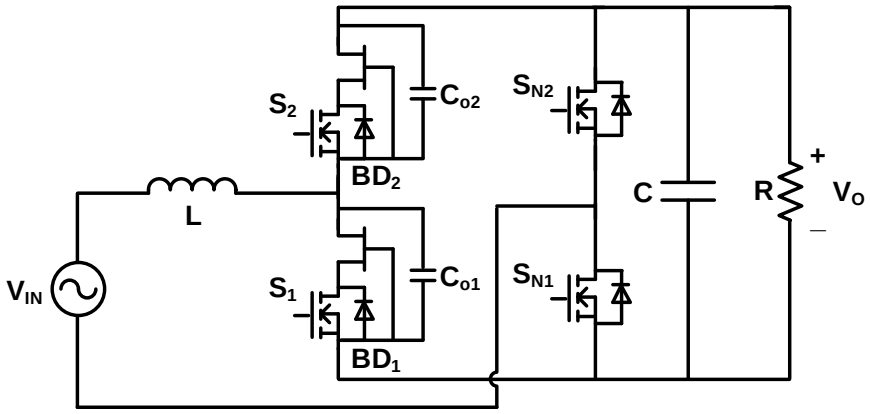


Fig. 3.14. Topology of GaN-based MHz totem-pole PFC with parasitic capacitor

Two sets of boost circuits act as PFC rectifier in each half line cycle. During positive half line cycle, SN1 is in the on-state and SN2 is in the off-state. S1 acts as the control switch and S2 acts as the SR. During negative half line cycle, SN2 is in the on-state and SN1 is in the off-state. S2 acts as the control switch and S1 acts as the SR. Because of the symmetry of the topology, the operation mode is identical during positive and negative half line cycle. So only the operation mode analysis during positive half line cycle is given in this section to derive the analytical model.

To derive the analytical model, the following two assumptions are made to simplify the derivation:

1. The voltage drop on the conducing device is ignored.

2. The input voltage is considered as constant within one switching cycle, since switching frequency is much higher than line frequency. This value is selected at the beginning of each switching cycle.

In one switching cycle, there are six stages which can be separated by time instants (t0, t1… t6) marked in the figure below.

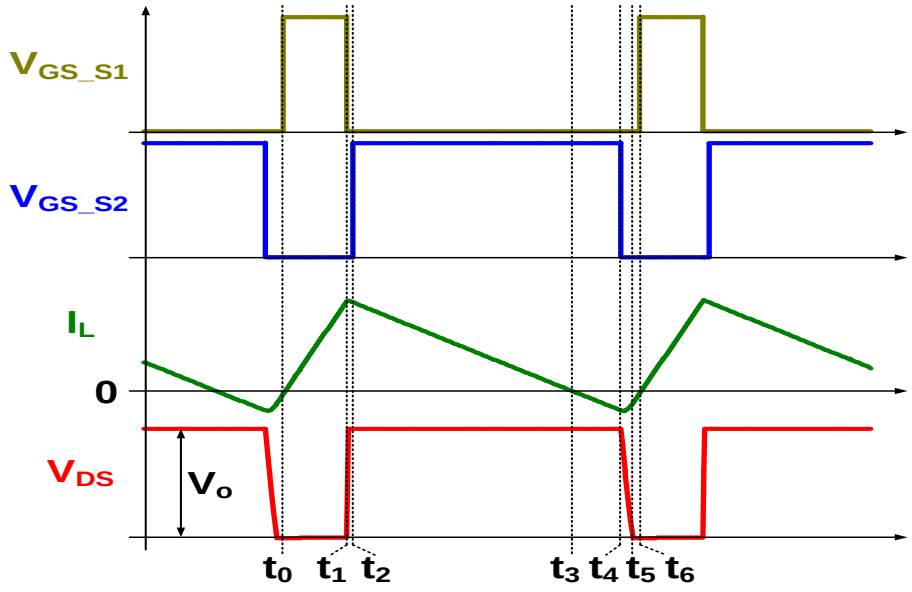
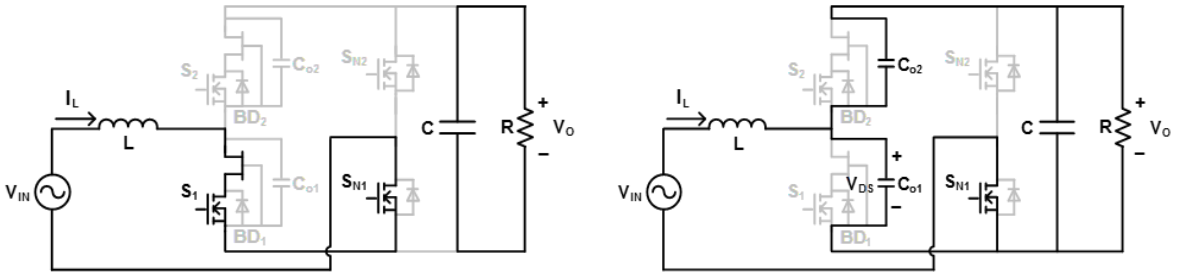
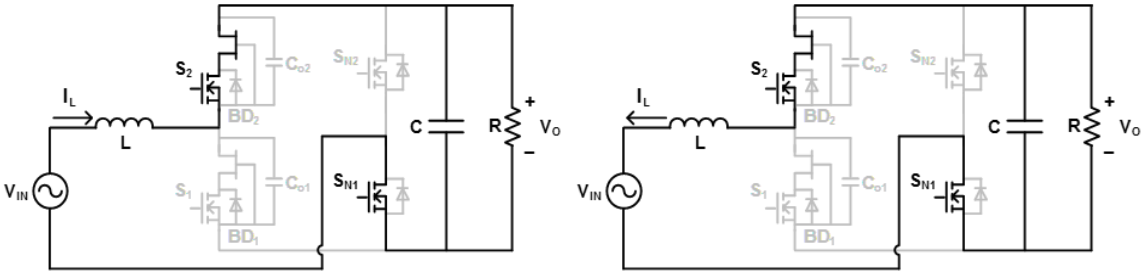


Fig. 3.15. Typical switching cycle operation waveform of totem-pole PFC

For each stage, the equivalent circuit is given in the figure below and the corresponding analytical model is derived.



(a) (b)



(c) (d)

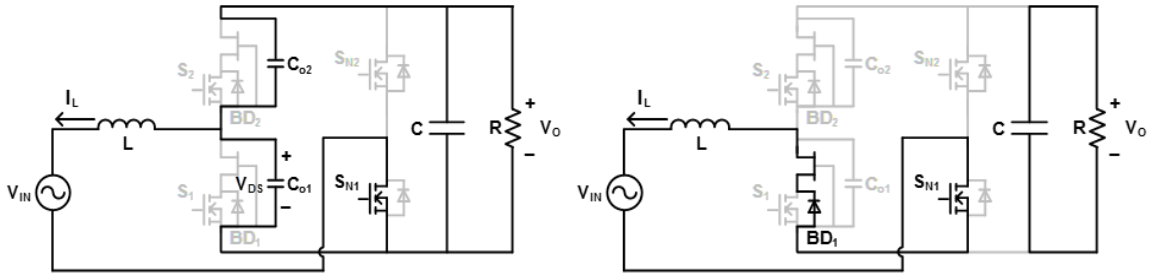


Fig. 3.16. Six operation stages in one switching cycle

Stage I: Control switch on period, [t_0, t_1]

At t0, the control switch S1 is turned on, as shown in Fig. 3.16 (a). The inductor current iL(t) starts to increase linearly, which can be expressed in equation (3.6). This stage ends when S1 is turned off at t1 instant.

$$i_L(t)=\frac{V_{in}(t_0)}{L}(t-t_0)+i_L(t_0) \tag{3.6}$$

Stage II: Resonance period 1, [t_1, t_2]

After S_1 is turned off at t_1, C_{o1} and C_{o2} starts to resonate with inductor L, as shown in Fig. 3.16 (b). During the resonance period, C_{o1} is charged and C_{o2} is discharged by inductor current. The inductor current, $i_L(t)$ and voltage across C_{o1}, $v_{DS}(t)$ can be expressed in equation (3.7) and (3.8).

$$i_L(t)=\frac{V_{in}(t_0)}{Z_n}\sin\omega_0(t-t_1)+i_L(t_1)\cos\omega_0(t-t_1) \tag{3.7}$$

$$v_{DS}(t)=V_{in}(t_0)\left[1-\cos\omega_0(t-t_1)\right]+i_L(t_1)Z_n\sin\omega_0(t-t_1) \tag{3.8}$$

Here $Z_n=\sqrt{\frac{L}{2C_{oss}}}$, $\omega_0=\frac{1}{\sqrt{2LC_{oss}}}$ and $C_{o1}=C_{o2}=C_{oss}$.

Stage III: SR on Period, [t2, t3]

After $v_{DS}(t)=V_o$ at t_2 instant, S_2 is turned on, as shown in Fig. 3.16 (c). The inductor current $i_L(t)$ starts to decrease linearly, which can be expressed as below. This stage ends when $i_L(t)=0$ at t_3 instant.

$$i_L(t)=-\frac{V_o-V_{in}(t_0)}{L}(t-t_2)+i_L(t_2) \tag{3.9}$$

Stage IV: SR extra conducting period, [t3, t4]

After iL(t)=0 at t3, under specific condition, SR is required to conduct for an extra period of time in order to achieve ZVS turn on of the control switch. The equivalent circuit is the same as that in Stage III, except for the polarity of inductor current, as shown in Fig. 3.16 (d).

If Vin(t) $\leqslant$ 0.5Vo, during this stage this extra period of time is not required. So at t3 instant, SR should be immediately turned off and this stage ends, which means t4 instant is identical to t3 instant.

If Vin(t) > 0.5Vo, during this stage, this extra period of time is required. So the inductor current can be expressed as below, which is quite similar to (3.9).

$$i_L(t)=-\frac{V_o-V_{in}(t_0)}{L}(t-t_3)+i_L(t_3) \tag{3.10}$$

The minimum required extra time for SR conduction will be derived later in the next section. So this stage ends after SR conduction lasts for the required extra period of time at t_4 instant.

Stage V: Resonance period 2, [t4, t5]

After S_2 is turned off at t_4, C_{o1} and C_{o2} starts to resonate again with inductor L. The equivalent circuit is the same as that in Stage II, except for the polarity of inductor current, as shown in Fig.

3.16 (e). During this resonance period, C_{o1} is discharged and C_{o2} is charged by inductor current. The inductor current, $i_L(t)$ and voltage across C_{o1}, $v_{DS}(t)$ can be expressed as below, which is similar to equation (3.7) and (3.8). This stage ends when $v_{DS}(t) = 0$ at t_5 instant with non-positive inductor current value.

$$i_L(t)=\frac{V_{in}(t_0)-V_o}{Z_n}\sin\omega_0(t-t_4)+i_L(t_4)\cos\omega_0(t-t_4) \tag{3.11}$$

$$v_{DS}(t)=V_{in}(t_0)\left[1-\cos\omega_0(t-t_4)\right]+V_o\cos\omega_0(t-t_4)+i_L(t_4)Z_n\sin\omega_0(t-t_4) \tag{3.12}$$

If $V_{in}(t) \leq 0.5V_o$, during this stage the inductor current is negative at t_5 instant.

If $V_{in}(t) > 0.5V_o$, during this stage to make sure ZVS turn on can be achieved, some margin should be left so the extra time is a little longer than the minimum required value, which makes the inductor current still negative at t_5 instant.

Stage VI: Body diode conduction period, [t5, t6]

After $v_{DS}(t) = 0$ at t_5 instant, BD_1, the body diode of control switch S_1 starts to conduct, as shown in Fig. 9(f). The inductor current $i_L(t)$ starts to increase linearly, which can be expressed as below, similar to equation (3.6).

$$i_L(t)=\frac{V_{in}(t_5)}{L}(t-t_5)+i_L(t_5) \tag{3.13}$$

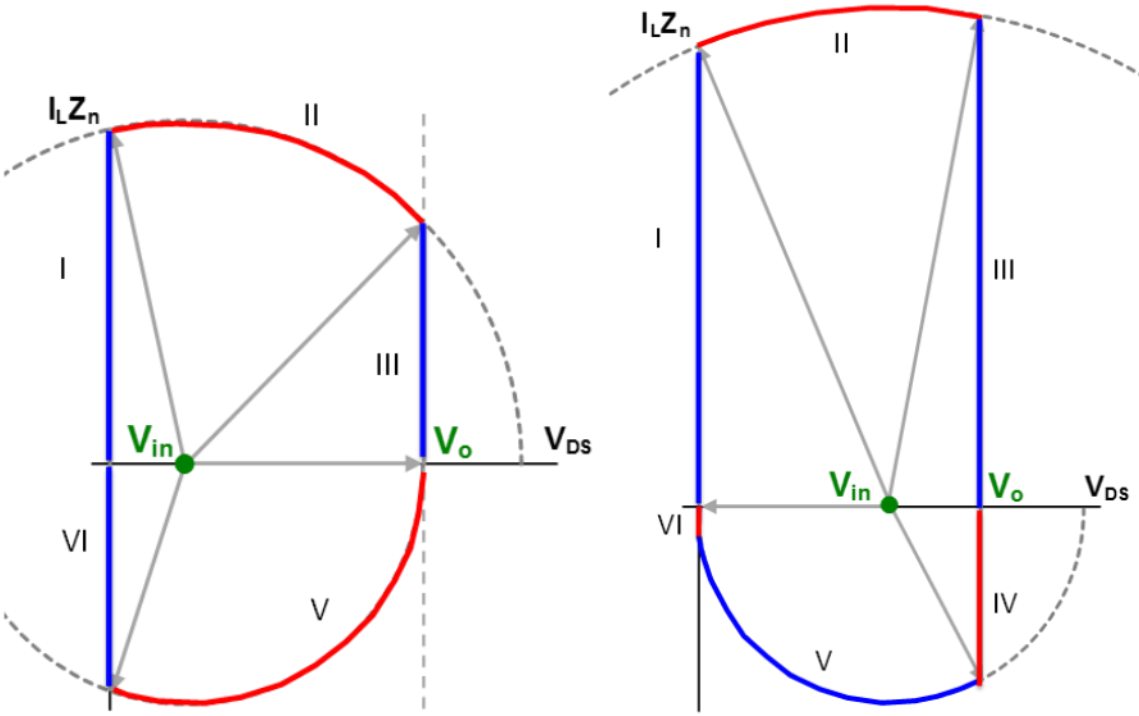
To achieve ZVS turn on, in this stage, the control switch should be turned on before iL(t)=0. So this stage ends at t_6 instant, when control switch is turned on with non-positive inductor current.

After t_6 instant, another switching cycle begins.

3.2.2 State-Space Trajectory Analysis

Based on the time-domain operation mode analysis and derivative analytical model, the state-plane trajectory is derived in this section to see the operation state more clearly in one switching cycle. Here the state-plane trajectory is under the same assumptions as previous section.

With V_{DS} as x axis, and $I_L Z_n$ as y axis, the state-plane trajectory shows the relation between I_L and V_{DS} in XOY plane over one switching cycle as Fig. 3.17. According to the polarity of (Vin(t) – 0.5Vo), the state-plane trajectory is separated into two cases, which are shown in Fig. 3.17 (a) and Fig. 3.17 (b), respectively.



(a) (b)

Fig. 3.17. State-plane trajectory: (a) Vin $\leqslant$ 0.5Vo, and (b) Vin > 0.5Vo

Fig. 3.18 (a) shows the trajectory over one switching cycle under Vin(t) $\leqslant$ 0.5Vo condition. Based on the operation mode analysis, the trajectory is separated into five parts corresponding to

Stage I, II, III, V and VI, respectively. Since here ZVS extension is not required, there is no Stage IV in this trajectory.

During Stage I, III and VI, the inductor current is linearly increasing or decreasing, so the trajectory is in parallel with y axis. While during Stage II and V, the resonance between inductor and switch output capacitance makes the trajectory be a circular arc, with the center at (Vin, 0).

Fig. 3.19 (b) shows the trajectory over one switching cycle under Vin(t) > 0.5Vo condition. Besides the aforementioned five stages, the Stage IV is also in this trajectory because ZVS extension is required here. This stage is similar to Stage III, in which the inductor current is linearly decreasing while VDS doesn't change. So the trajectory during Stage IV is also in parallel with y axis.

3.2.3 Proposed Programmed On-Time Control

This analytical model can be applied into voltage mode control for CRM PFC rectifier. This section is focused on how to achieve control functions using the previous analysis, including ZVS extension, and variable on-time control.

In order to achieve ZVS turn on of control switch during line cycle, ZVS extension is applied in the voltage mode control under Vin(t) > 0.5Vo condition, which means SR conducts for an extra period of time under this condition.

From the trajectory of Stage IV and V, the minimum required extra time for SR conduction can be derived as below:

$$t_{SR\_extra(\min)} = \frac{\sqrt{\left[2V_{in}(t_0) - V_o\right]V_o}}{V_o - V_{in}(t_0)} \cdot \sqrt{2LC_{oss}} \tag{3.14}$$

It should be noted that this minimum required value makes Stage V end when VDS = 0, and at the same time, iL = 0. With this minimum required value, there is no Stage VI in the trajectory and the control switch should be turned on immediately when Stage V ends. Earlier or later turn on of control switch results in non-ZVS loss. Practically, some margin is purposely added to make SR conduct for a little longer than the minimum required period of time.

Also, in order to improve power factor and THD of input current, variable on-time control is applied in the voltage mode control.

Define T_{on}, the on-time in one switching cycle, as the time interval from the instant when i_L = 0 during inductor current charging process, to the instant when control switch is turned off. From the state-plane trajectory, it can be seen that for specific PFC circuit components and specific power condition, the Stage I, II and III can all be determined by T_{on}, which means that the initial inductor current value, the final inductor current value and duration time for each stage can be simply determined by T_{on}.

Therefore, with specific PFC circuit components and specific power condition, the average input current is a function of T_{on}, that is:

$$I_{in\_avg}(t)=f(T_{on}) \tag{3.15}$$

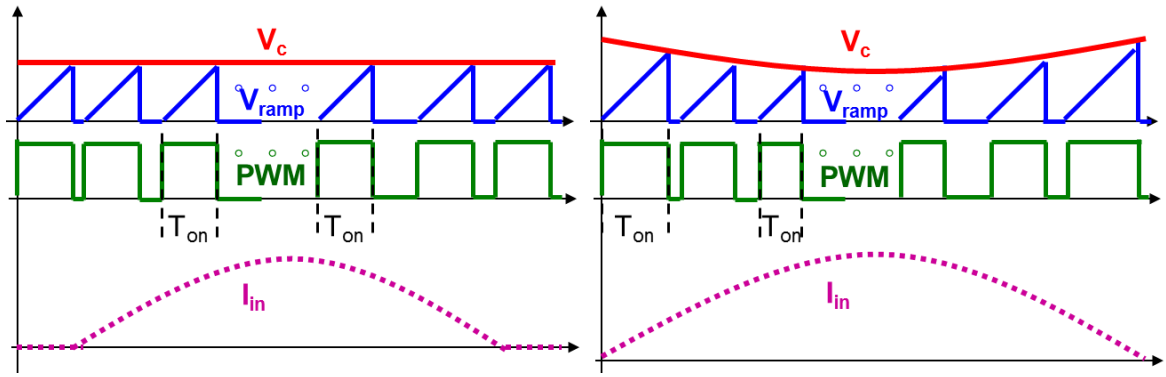
Based on input voltage V_{in}, and output power P_o, the reference value for input current can be calculated as below:

$$I_{in\_ref}(t)=\frac{\sqrt{2}P_o}{V_{in\_RMS}}\sin(2\pi f_L t) \tag{3.16}$$

Here f_L is the line frequency.

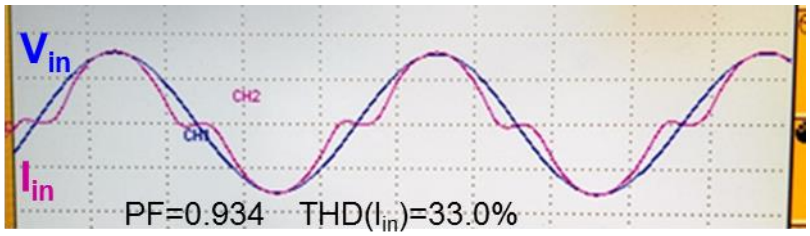
Finally, by making the average input current equal to the reference value in the whole line cycle, good power factor and low THD can be achieved, and $T_{on}(t)$ can be derived.

The concept is illustrated in Fig. 3.20. By increasing the on time near the zero crossing, the input current is again able to achieve good power factor. Fig. 3.21 shows the experimental verification.

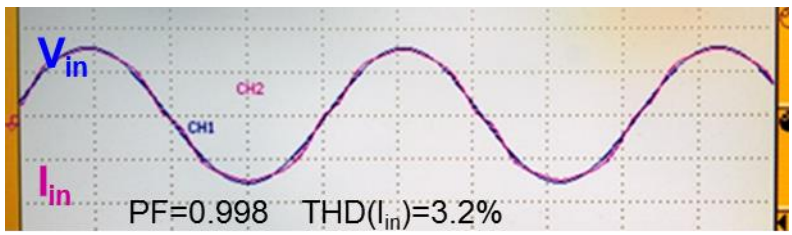


(a) (b)

Fig. 3.20. Concept diagram of CRM PFC with (a) Constant on-time control and (b) Variable on-time control



(a)



(b)

Fig. 3.21. Experimental verification (a) Constant on-time control and (b) Variable on-time control

3.3 Challenge of Interleaving to Reduce Current Ripple

Another drawback of the CRM PFC rectifier is the high current ripple, which leads to not only higher conduction loss but also higher DM noise than the CCM PFC rectifier. To deal with this issue, a two-phase interleaving structure is used to effectively reduce the DM noise by taking advantage of the ripple cancellation effect. Fig. 3.22 shows the preferred 2-phase interleaved totem-pole PFC topology.

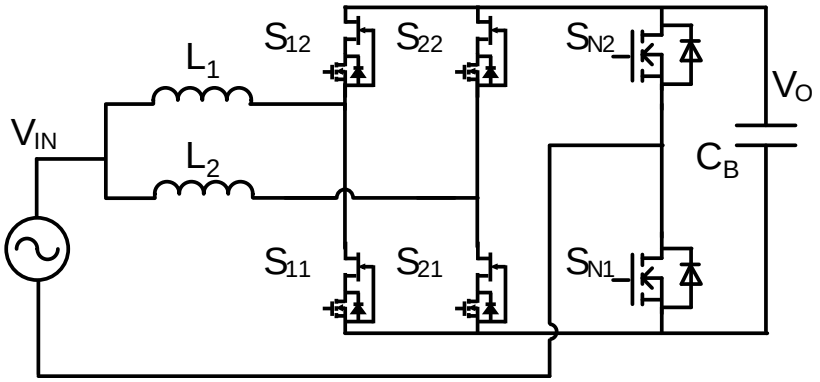


Fig. 3.22. Circuit diagram of two-phase interleaved totem-pole PFC with cascode GaN devices

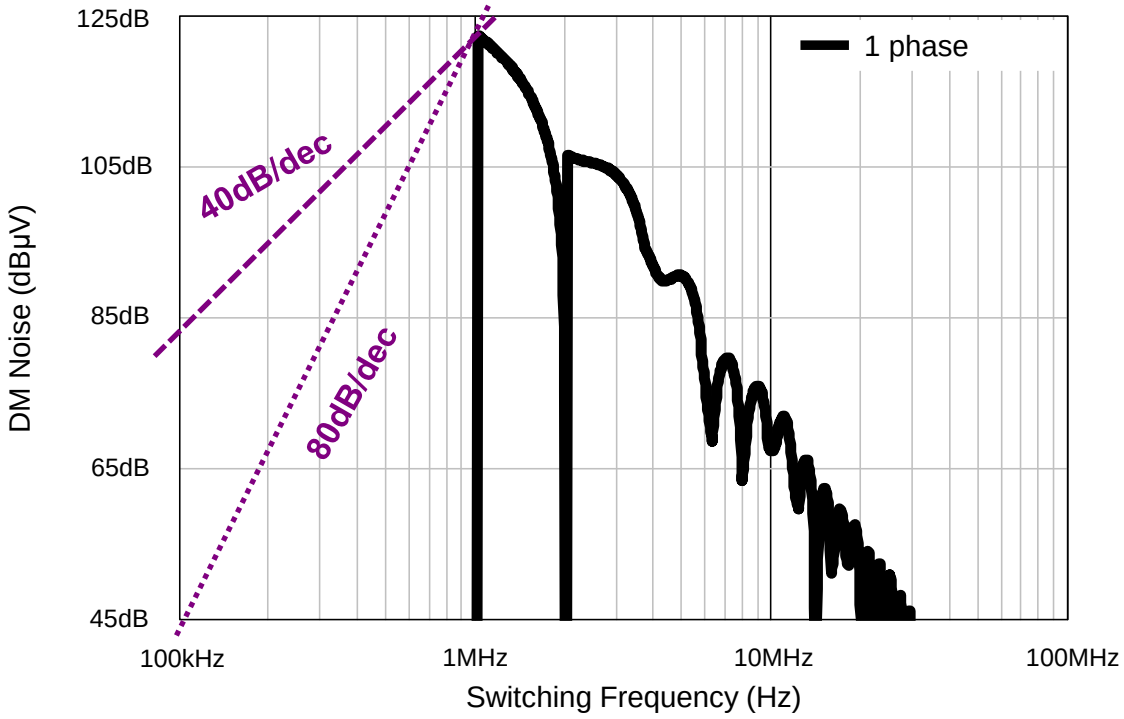
3.3.1 Impact of Interleaving Control on MHz Totem-Pole PFC and its Differential Mode (DM) Filter

For a single phase CRM PFC, the input current ripple is always more than two times higher than its average current. Multi-phase interleaving techniques are widely used so that the total input current ripple is reduced, which is beneficial to have a lower conduction loss, a longer capacitor lifetime, and most importantly, a smaller input filter size.

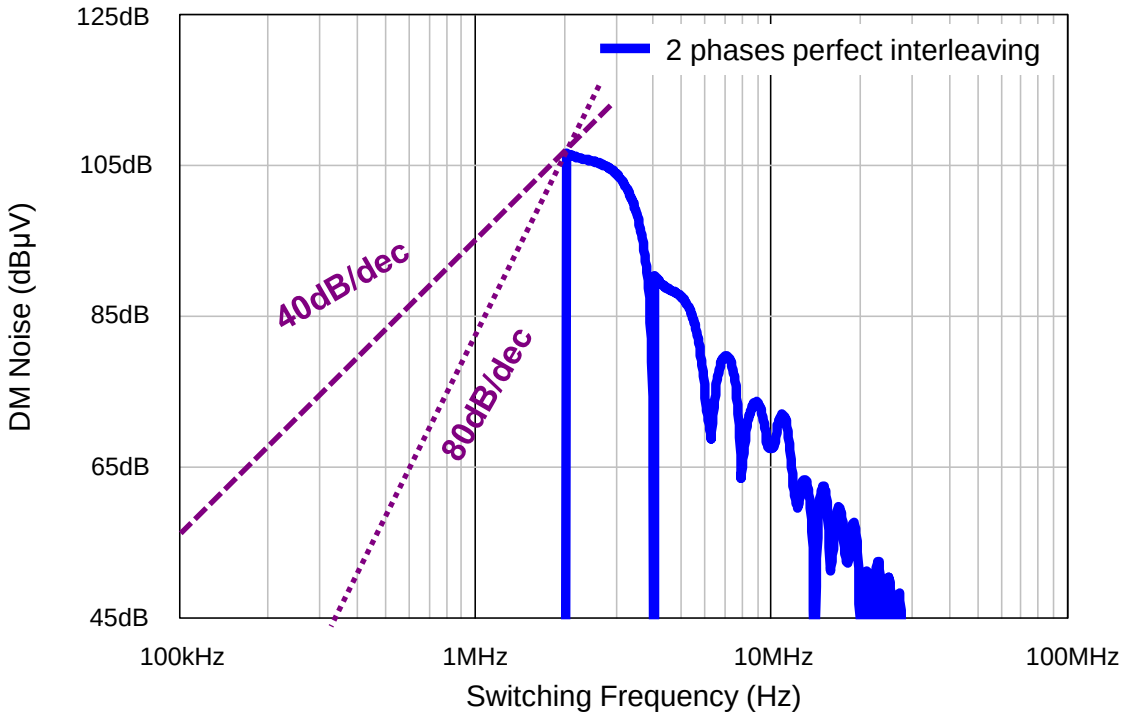
For a two phase interleaved CRM PFC, when the phase shift is 180 degrees, the first order components in the input current is totally canceled while only second order and higher orders

components exist. With the proposed DM noise model for CRM PFC [C.25], the DM noise spectrum is predicted for the dual-phase MHz totem-pole PFC (Fig. 3.23). It is clearly shown that the ripple cancellation effect is very sensitive to phase error. Even just a few degrees phase error leads to a quick increase of the first order noise components, while the critical value is 5 degree and 1 degree for 1-stage DM filter and 2-stage DM filter respectively.

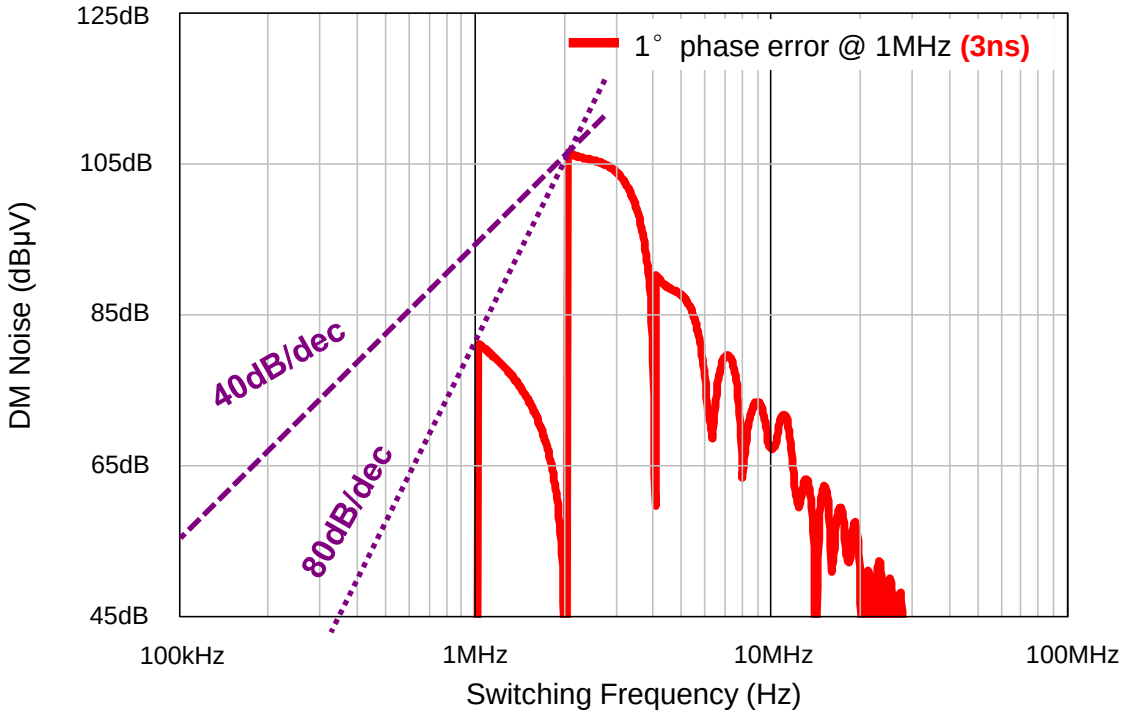
The critical value is chosen as 5 degrees, because when a 1-stage DM filter is used and the phase error is lower than 5 degree, the 40 dB/dec line firstly touches the DM noise at 2 MHz point. However, when the phase error is higher than 5 degree, it is the 1 MHz point who dominates the filter design. Thus it means the DM filter design cannot fully benefit from interleaving. For a 2-stage DM filter design, the critical value is 1 degree because 2-stage has 80 dB/dec attenuation, and thus it is more likely to be dominated by the 1 MHz point of the DM noise.



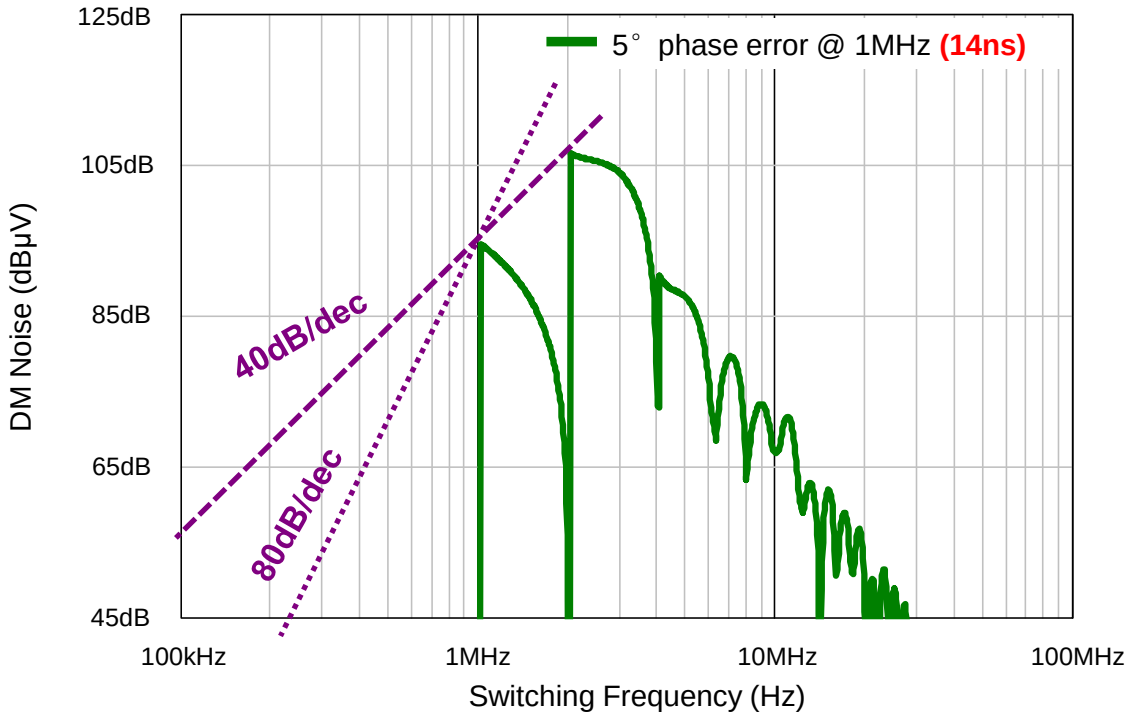
(a)


125dB
105dB
85dB
65dB
45dB
DM Noise (dBμV)
2 phases perfect interleaving
40dB/dec
80dB/dec
100kHz
1MHz
10MHz
100MHz
Switching Frequency (Hz)

(b)


125dB
105dB
85dB
65dB
45dB
DM Noise (dBμV)
1° phase error @ 1MHz (3ns)
40dB/dec
80dB/dec
100kHz
1MHz
10MHz
100MHz
Switching Frequency (Hz)

(c)



(d)

Fig. 3.23. Predicted DM noise spectrum for 1.2 kW MHz totem-pole PFC. (a) one phase; (b) 2 phases with perfect interleaving; (c) 2 phases with 1 degree phase error; and (d) 2 phases with 5 degree phase error

So in order to have full benefits on the DM filter, the phase error should be kept smaller than the critical value. Previously it is not a big issue to maintain a small phase error in frequency range like 70 kHz or 130 kHz PFC, however, when it increases to a multi-MHz frequency, it is really a challenge to make the phase error smaller than the critical value because only a few nano-second delay error leads to a significantly large phase error.

3.3.2 Performance Comparison between Closed-loop Interleaving and Open-loop Interleaving for MHz CRM Totem-Pole PFC

According to literature, previously proposed different interleaving control methods are divided into two categories: closed-loop interleaving [C.26]-[C.30] and open-loop interleaving

[C.31]-[C.36]. In this paper, a master-slave relationship between two phases, and the voltage-mode control are applied to both cases. Particularly the turn-on instant synchronization is used in an open-loop interleaving analysis. Fig. 3.24 and Fig. 3.25 illustrate the concept of two interleaving control methods.

The voltage mode controlled CRM PFC is usually preferred because no instantaneous or average current sensing is required. The bandwidth of the voltage loop is much smaller than the line frequency so avoid double-line frequency ripple in the output. The voltage mode controlled CRM PFC is also referred to as constant on-time CRM PFC since the peak current is roughly two times of the average current and unity power factor is achieved naturally with a constant on-time in a line cycle. In this paper, voltage mode is used for both closed-loop interleaving case and open-loop interleaving case.

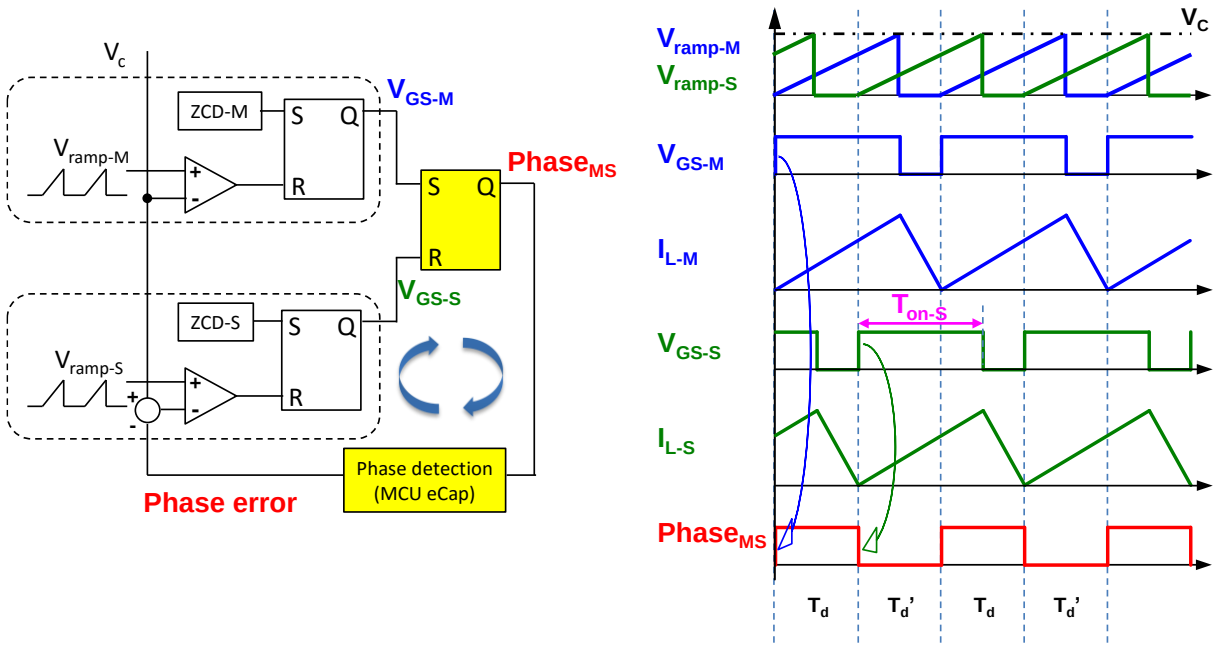


Fig. 3.24. Control diagram and typical waveforms of closed-loop interleaving with master-slave relationship and voltage-mode control

For the closed-loop interleaving shown in Fig. 3.24, the turn-on instants of both phases are triggered by the zero-current-detection (ZCD) signals. Thus soft-switching is guaranteed for both phases. The on-time of the master phase is determined solely by the voltage loop. The phase error between two phases is sensed and used to adjust the on-time of the slave phase so that the phase error can be minimized. Essentially there is a closed inner control loop as marked by the blue arrows. This method is also referred to as phase-locked-loop (PLL) based interleaving method.

For the open-loop interleaving shown in Fig. 3.25, the turn-off instants (or the on time) of both phases are determined by the voltage loop. However, only the turn-on instant of the master phase is triggered by the ZCD signal. For the slave phase, the instantaneous switching period of the master phase is detected, and then one-half of the sensed period is sent to the slave phase to determine the turn-on instant. One drawback of this method is soft-switching cannot be guaranteed in the slave phase without other performance trade off. Therefore the closed-loop interleaving method is usually preferred at low frequency (e.g. 70 kHz or 130 kHz) CRM PFC design.

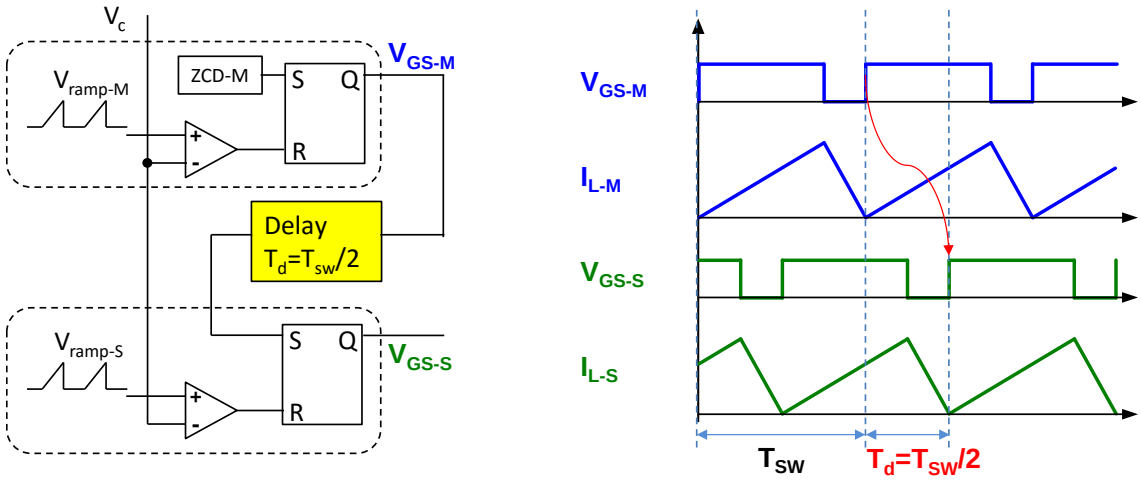


Fig. 3.25. Control diagram and typical waveforms of open-loop interleaving with master-slave relationship, voltage-mode control, and turn-on instant synchronization

For the system control implementation, no commercial controller supporting a MHz CRM PFC operation was available at the time of this research was conducted. Discrete components based analog control was tried for the first time, however they did not offer good enough control accuracy for interleaving, therefore, a MCU based control is considered a viable alternative to achieve good performance and reasonable cost.

A 60 MHz MCU is used in the hardware demonstration. When the interleaving control is implemented by the MCU, there are two limitations. The first limitation is that the interleaving control cannot be done cycle by cycle. As shown in Fig. 3.26, different control functions are executed in a series sequence so that the total control cycle takes 240 system clock cycles to complete. This is equivalent to 4 µs with a 60 MHz MCU so that the control cycle is much longer than the switching cycle. As a result, the interleaving control is performed once in each 4 µs.

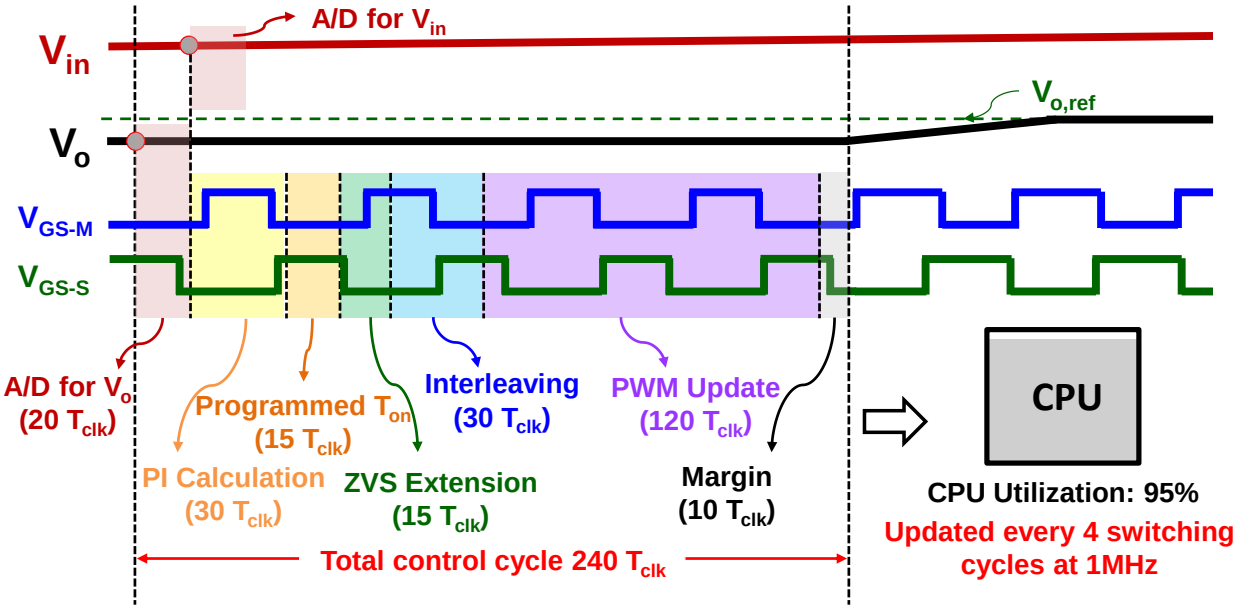


Fig. 3.26. MCU control implementation sequence (VGS-M and VGS-S are the gate driving signal of the control switch of the master phase and the slave phase respectively)

The second limitation is that all the control signals are synchronized to the MCU system clock. Then the switching period and delay time are all integer compared to the clock cycle. So even the nature of the CRM PFC is continuously smooth changing frequency but when implemented by MCU, the actual frequency is discrete.

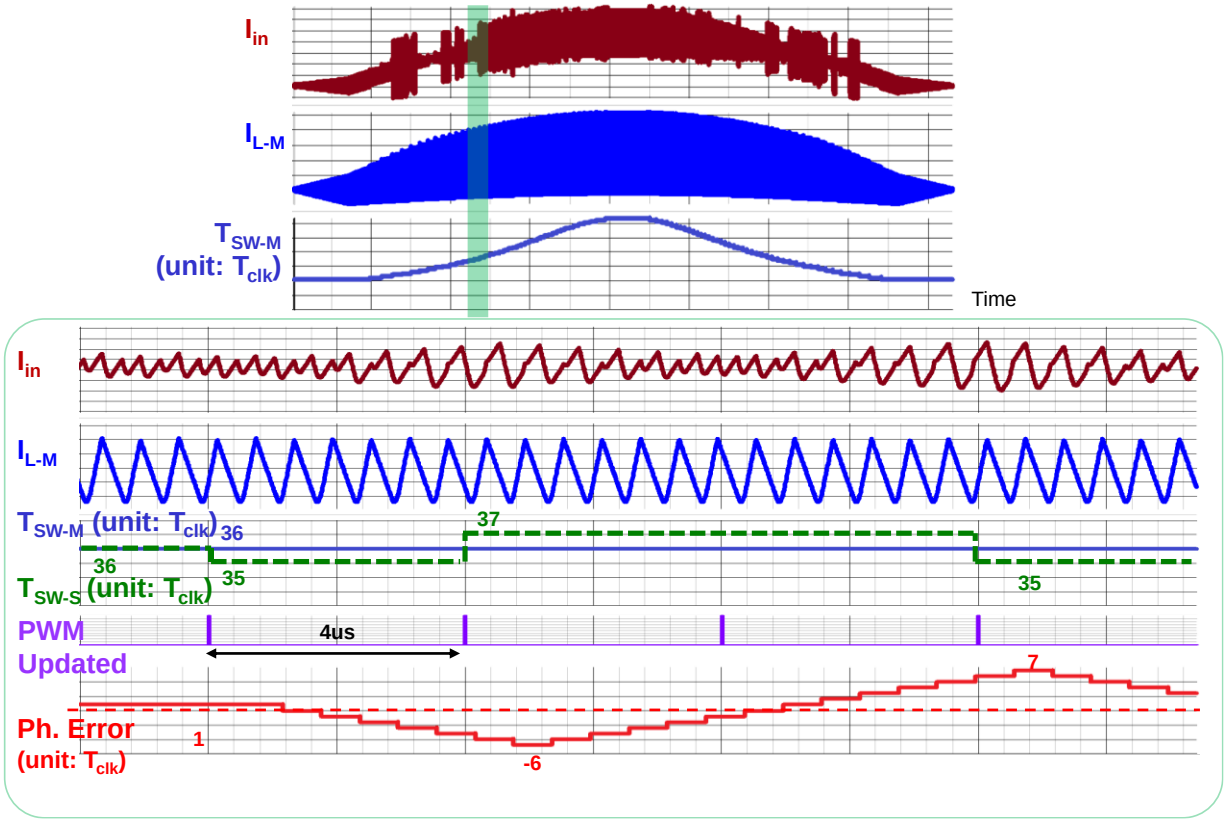


Fig. 3.27. Simulated closed-loop interleaving of MHz CRM totem-pole PFC (TSW-M and TSW-S are the switch period of the master phase and the slave phase respectively; Ph. Error is the calculated phase error between the master phase and the slave phase; all of the three variables use digitalized and normalized value to MCU clock cycles)

When the two limitations combine together, a phase error oscillation is observed with the closed-loop interleaving method. Fig. 3.27 shows the simulation waveform. There is significant oscillation in the half line cycle input current which indicates that the interleaving is not accurate. The zoom-in waveform further illustrates how the phase error is amplified and keeps oscillating.

The phase error between two phases is increased or decreased by one clock cycle in each switching cycle. This is the minimum variation of phase error as switching period must be an integer number of clock cycle, and the minimum variation of switching period is one clock cycle as well. The on-time variation of salve phase is adaptively calculated and implemented by the high resolution PWM submodule of MCU to achieve a minimum switching period variation and thus a minimum phase error variation. The adaptively controlled on-time is critical because larger on-time variation may result in more than one clock cycle switching period variation; while smaller on-time variation may result in the same switching period so that no phase error adjustment can be observed.

Due to this limitation, there is up to a 24 degree phase error at 1 MHz which is far larger than the critical value and thus, makes the closed-loop interleaving unacceptable. The 24 degree phase error is a worst case value because the phase error can oscillate between positive and negative four clock cycles at 1 MHz switching frequency condition.

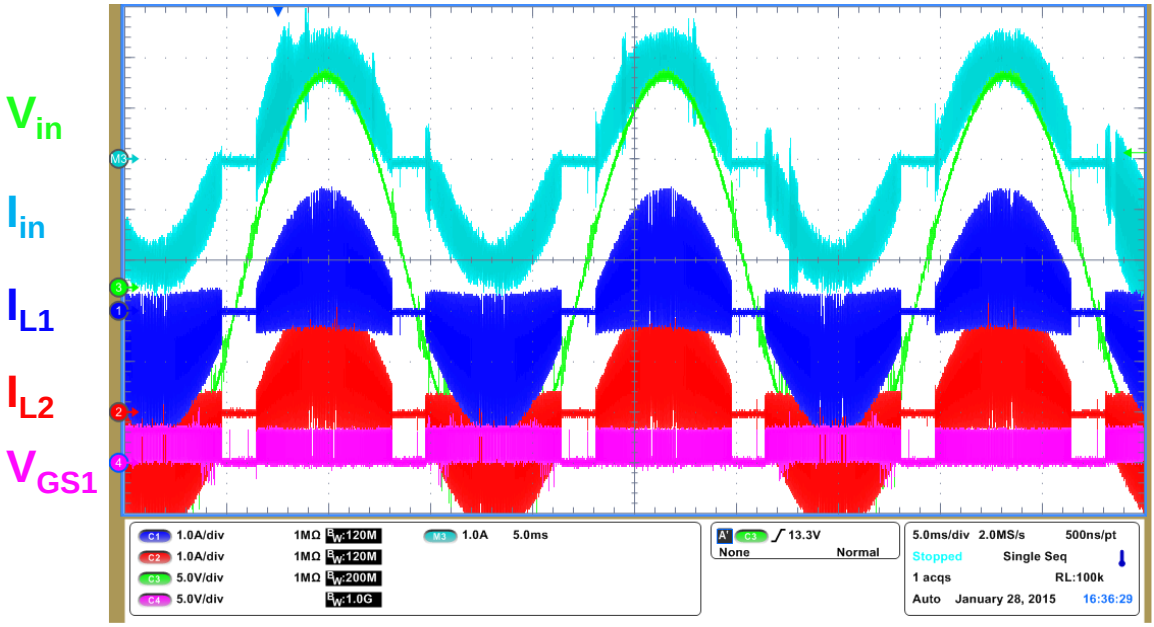


Fig. 3.28. Experimental waveforms of closed-loop interleaving of MHz totem-pole PFC

Fig. 3.28 is the experimental waveform with the closed-loop interleaving. The blue and the red waveforms are inductor current of each phase while the first waveform is the total input current after interleaving. Very similar to the simulation waveform, the measured total input current has an unstable ripple that randomly occurs as well. So with a 24 degree phase error, the first order component is becoming dominant and its magnitude is even higher than the second order component as indicated on Fig. 3.23.

On the contrary, the open loop interleaving has a small and non-amplified phase error. Although two limitations still exist, the phase error of the open-loop interleaving is able to stay smaller than one clock cycle. Detailed analysis of the phase error adjustment process of the open-loop interleaving with MCU implementation is shown on Fig. 3.29. It clearly shows that the phase error is small and it has no oscillation. The maximum phase error is only one clock cycle.

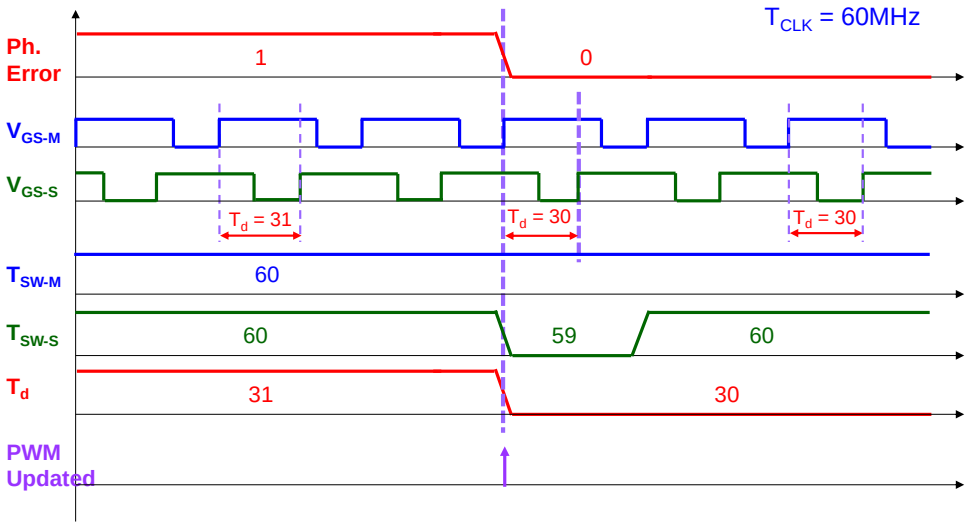


Fig. 3.29. Phase error adjustment with open-loop interleaving implemented by 60 MHz MCU (T_d is the delay time of the turn on instant of the slave phase compared to the turn on instant of the master phase)

Finally, Fig. 3.30 offers a side by side comparison which demonstrates that open-loop interleaving outperforms the closed-loop interleaving with a small and stable phase error. The blue

waveform is the inductor current of one phase. There is no difference between two interleaving methods. However, the total input currents shown in red color have significant difference. Both input currents have ripple cancellation effect as interleaving is implemented. For open-loop interleaving the ripple of the input current is minimized and its envelope is smooth which indicates well controlled and stable interleaving. In contrast, unstable ripple of the input current with closed-loop interleaving is shown in Fig. 3.30(a) which is caused by the phase error oscillation analyzed. Through this comparison, the open-loop interleaving is the preferred method since it has better ripple cancellation effect.

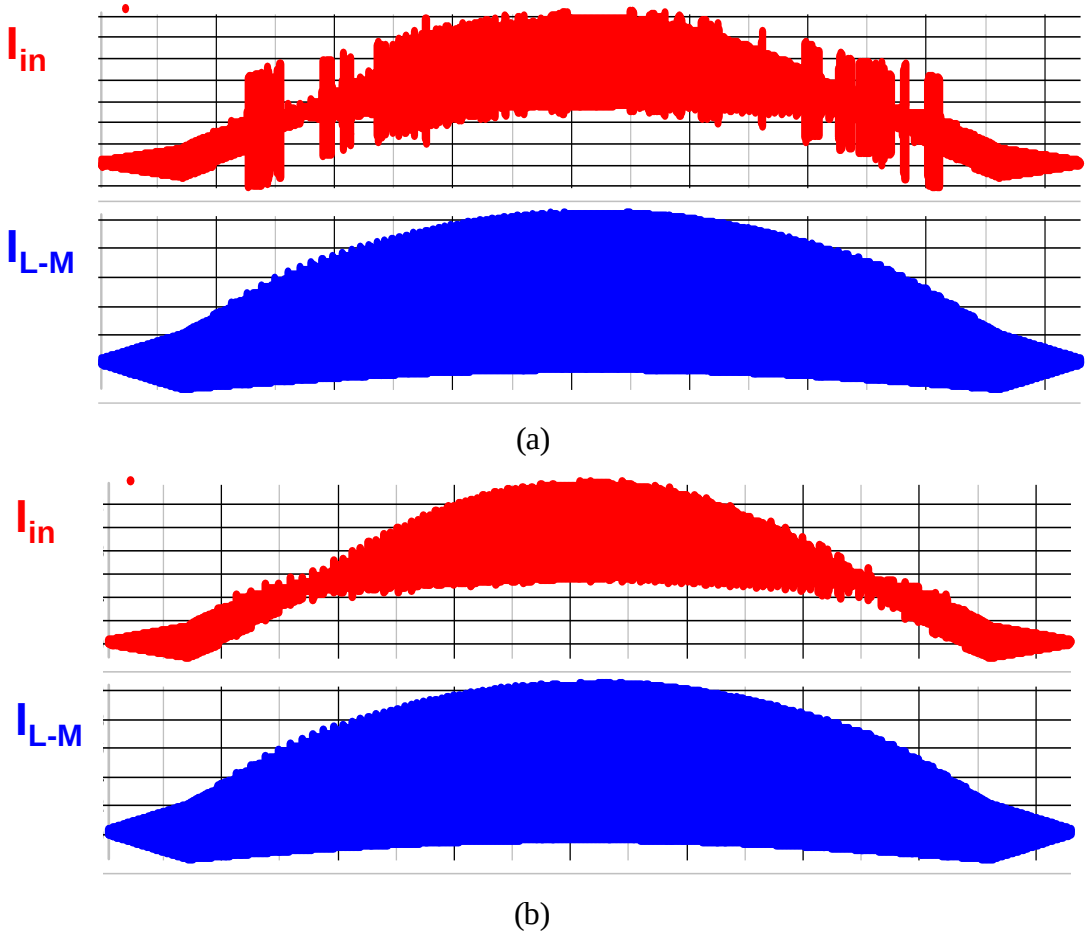


Fig. 3.30. Interleaving performance comparison of (a) closed-loop interleaving and (b) open-loop interleaving

3.3.3 Optimization of Open-Loop Interleaving

Due to the discrete frequency, there is always a one clock cycle phase error existing in an open-loop interleaving. With 60 MHz, this is equivalent to a 6 degree phase error at 1MHz which is still larger than the critical value. Besides increasing the CPU speed of the MCU, a software improvement is possible.

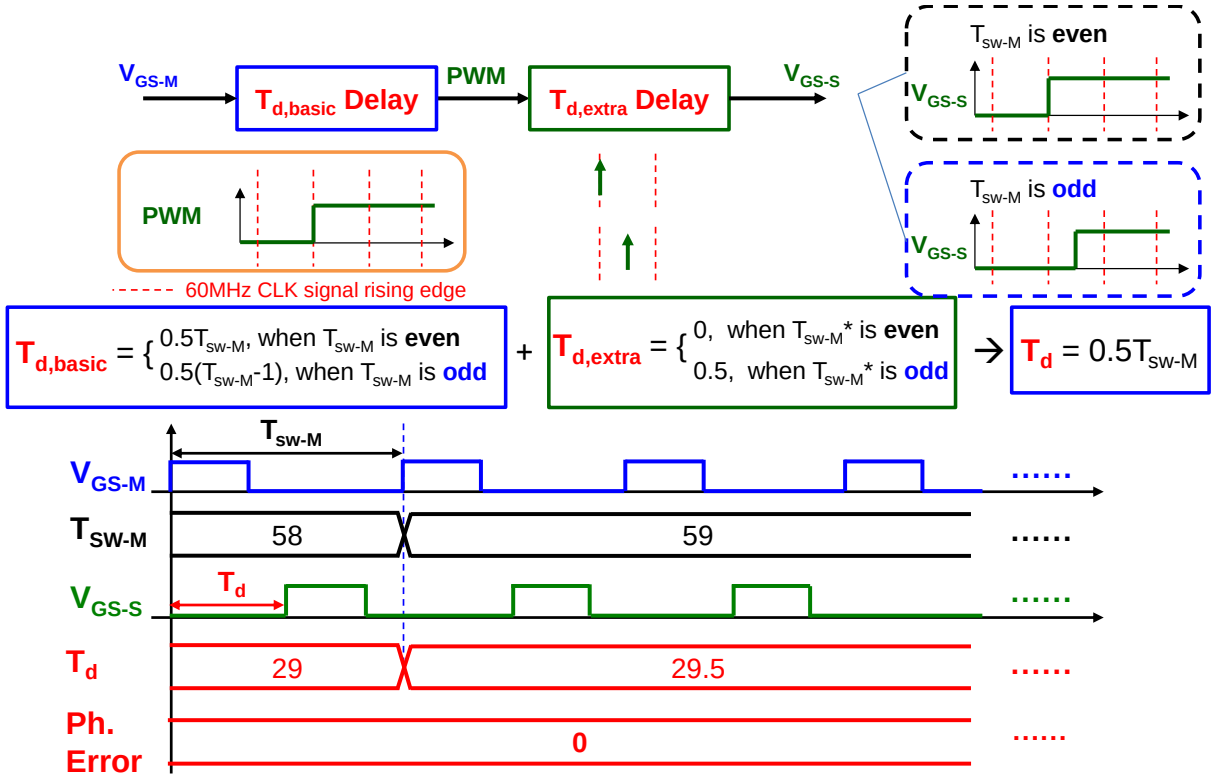


Fig. 3.31. Software optimization of open-loop interleaving ($T_{d,basic}$ is the basic delay time which must be an integer number of system clock; $T_{d,extra}$ is the extra delay time which can achieve zero or one-half system clock controlled by HALFCYCLE register in Dead-Band submodule)

Fig. 3.31 shows the improvement method. The idea is that the total delay time is divided into two separate parts. The basic delay time is still an integer of the system clock. At the same time, it is also possible to give another extra delay time which positions the PWM single edge with

one half clock cycle resolution. Then the edge is synchronized to the system clock when the master phase switching cycle is an even number; and the edge is placed in the middle of two adjacent system clocks to provide a one half clock cycle delay when the master phase switching cycle is an odd number. Ideally, when the two part delay times are combined, the total delay time is exactly equal to one half of the master phase switching period no matter if it is an even number or an odd number.

Fig. 3.32 further shows the phase error worst case of open-loop interleaving after the software optimization. It occurs in an abrupt change point of the switching frequency. Again, since the 4 µs control cycle is larger than the switching cycle, there is one half clock cycle phase error between the switching frequency change and next control cycle adjustment. It equals to a 3 degree phase error and it is smaller than the 5 degree critical phase error value if one stage DM filter is used.

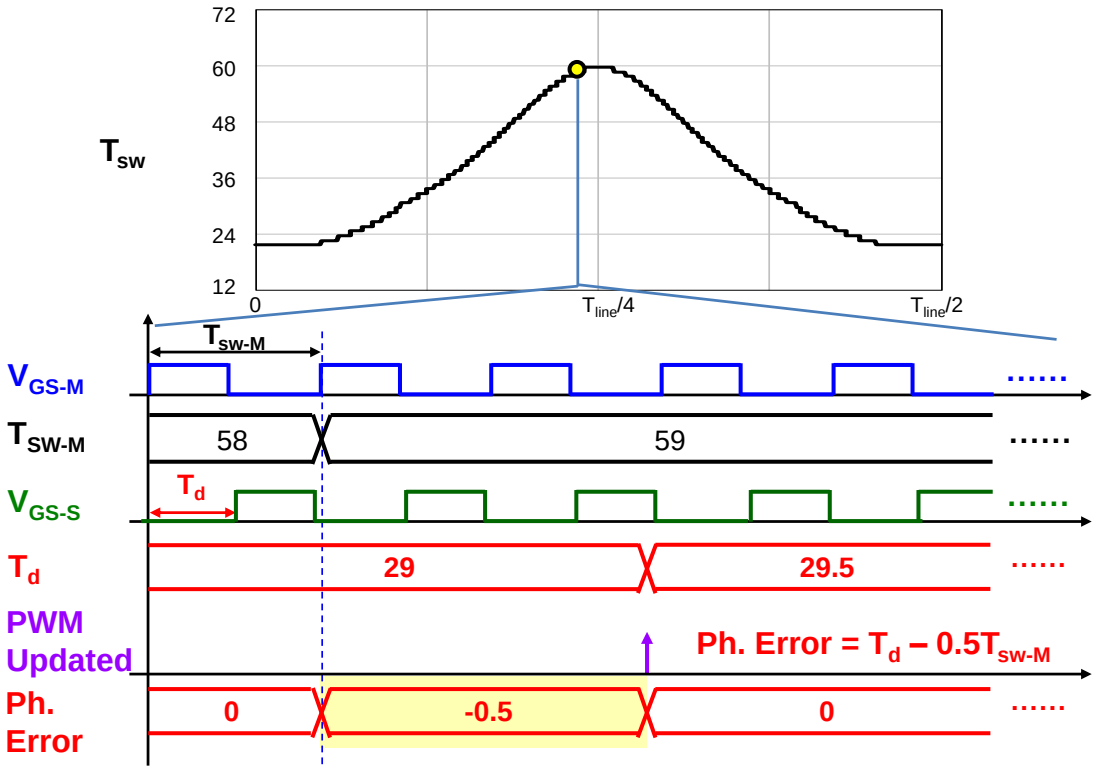
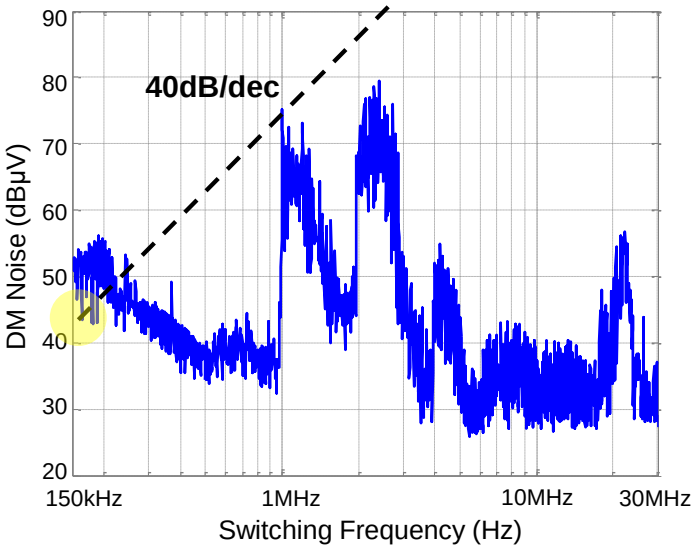
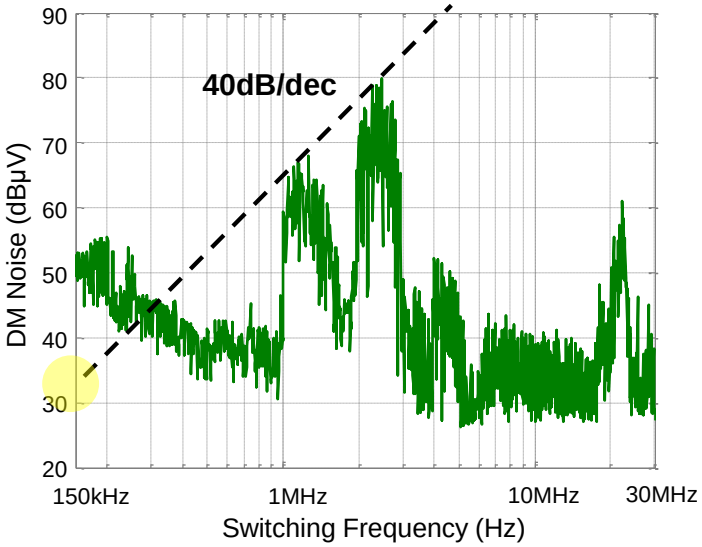


Fig. 3.32. Phase error worst case of open-loop interleaving after optimization

Fig. 3.33 shows the measured DM noise spectrum comparison before and after optimization. So with optimization method, the 2 MHz noise component became the dominant factor for the 1-stage DM filter design in Figure 12(b). Fig. 3.34 is the experimental waveform that shows good interleaving and ripple cancellation effect in different instant of a line cycle.



(a)



(b)

Fig. 3.33. Measured DM noise spectrum of open-loop interleaving (a) before optimization and (b) after optimization

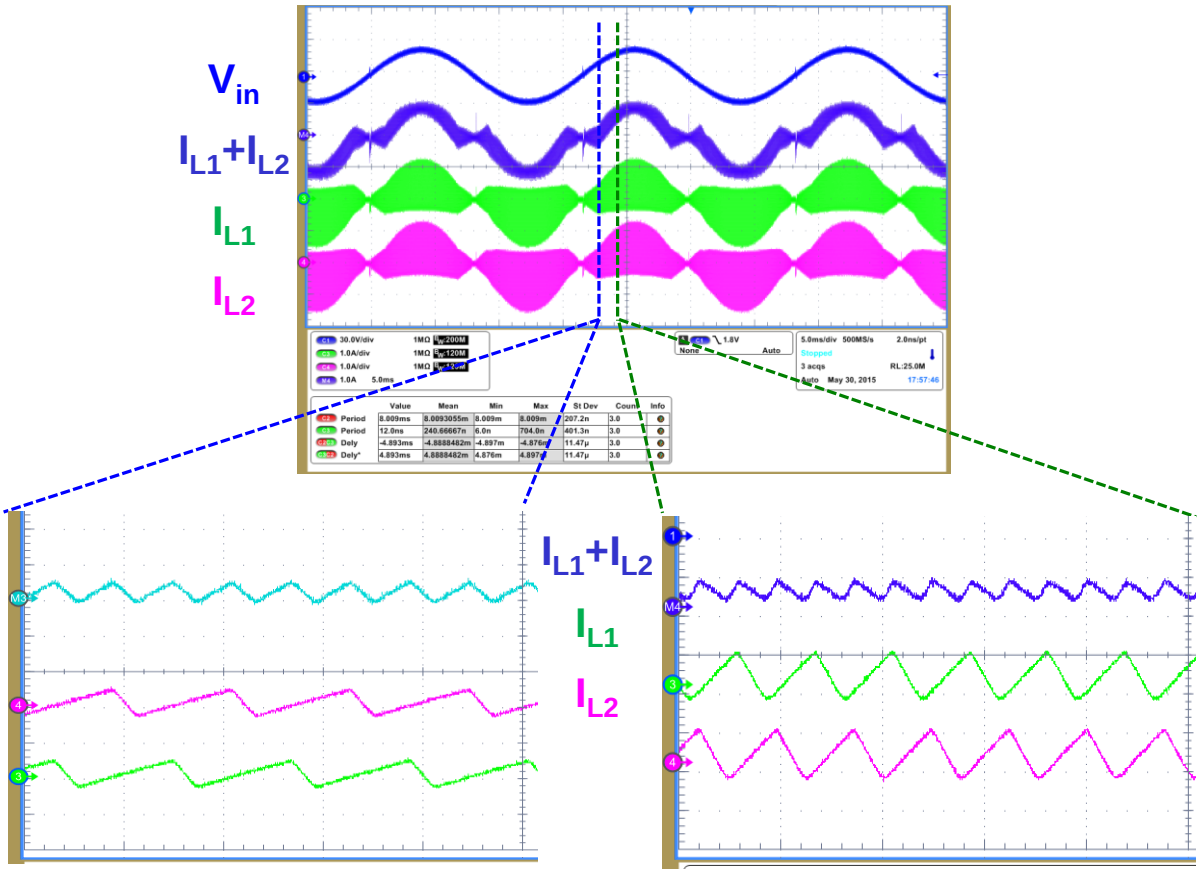


Fig. 3.34. Experimental waveform of open-loop interleaving

Table 3.2. Performance of interleaving with different MCU

	Series	CPU Speed	Closed-loop interleaving ($4xT_{CLK}$)			Open-loop interleaving ($0.5xT_{CLK}$)		
			Phase error	2-stage (1°)	1-stage (5°)	Phase error	2-stage (1°)	1-stage (5°)
Piccolo	F28027	**60 MHz**	24°	✗	✗	3°	✗	✓
	F28069	**90 MHz**	16°	✗	✗	2°	✗	✓
	F28075	**120 MHz**	12°	✗	✗	1.5°	✗	✓
Delfino	F28335	**150 MHz**	9.6°	✗	✗	1.2°	✗	✓
	F2837xS	**200 MHz**	7.2°	✗	✗	0.9°	✓	✓
	C28346	**300 MHz**	4.8°	✗	✓	0.6°	✓	✓

Even though the 60 MHz low cost MCU is used, the scope of the paper is not limited to one specific MCU. Several representative samples are selected for performance comparison and shown in Table 3.2. As a simple function of CPU speed, the corresponding phase errors with closed-loop interleaving and open-loop interleaving are calculated respectively and the benefits offered by open-loop interleaving are clearly seen through this comparison.

Based on the analysis and results, several system-level benefits can be projected including better efficiency, significantly improved power density due to size reduction of passive components and EMI filter, and better dynamic response under transient, which are all achieved by dramatically increased switching frequency enabled by GaN devices.

The high frequency impacts on the DM filter are shown in Fig. 3.35 and Fig. 3.36. By pushing the frequency 10 times higher, the volume of the DM filter is reduced at least 50% and a simple one-stage filter is sufficient to suppress the noise to be below the EMI standard. By making use of good interleaving, the volume is reduced by another 50%. Thus in total, the DM filter is just one-quarter of the size of a 100 kHz DM filter. Further analysis regarding EMI filter design for this MHz totem-pole PFC is included in [C.12].

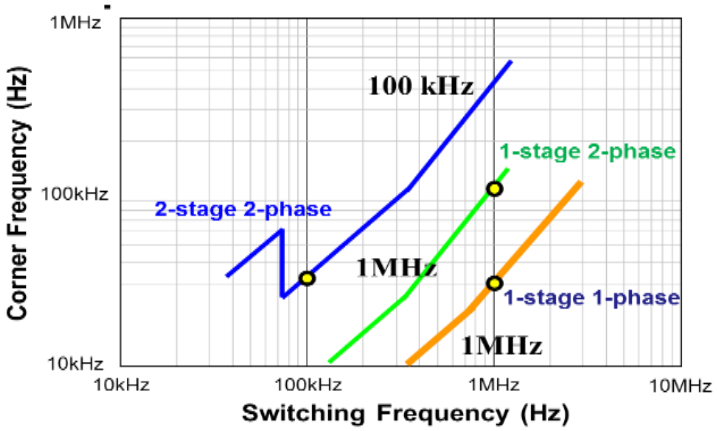


Fig. 3.35. Switching frequency impact on DM filter corner frequency

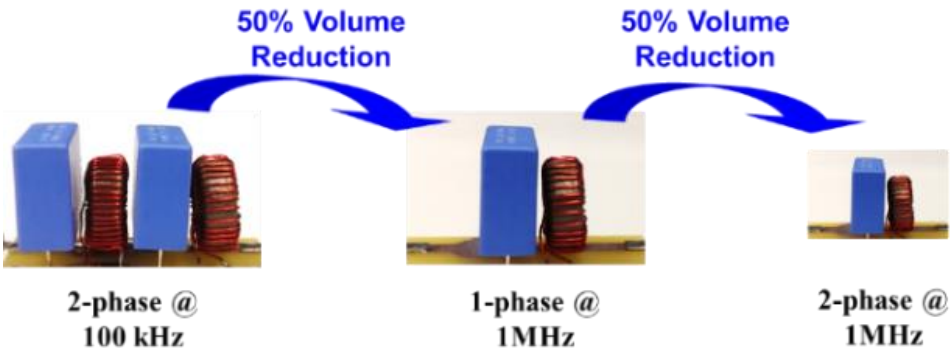
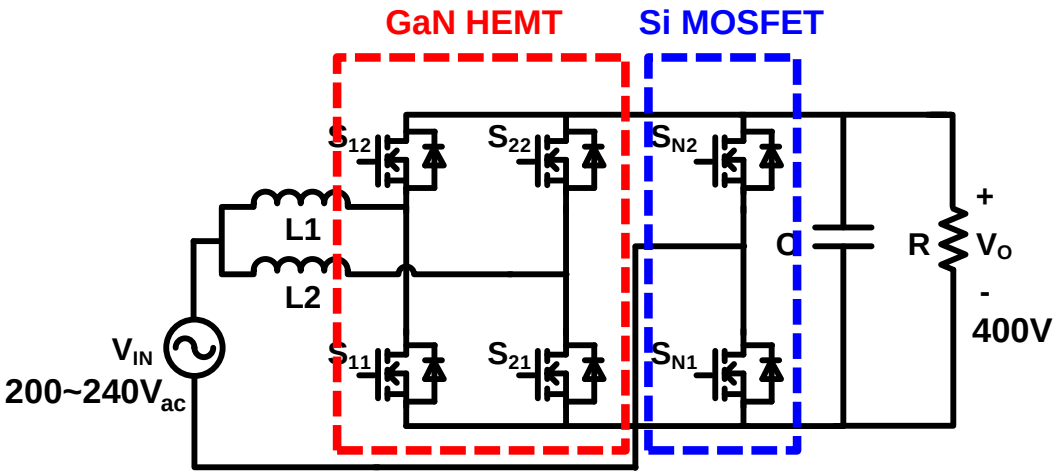


Fig. 3.36. DM filters for 100 kHz and 1 MHz totem-pole PFC rectifier

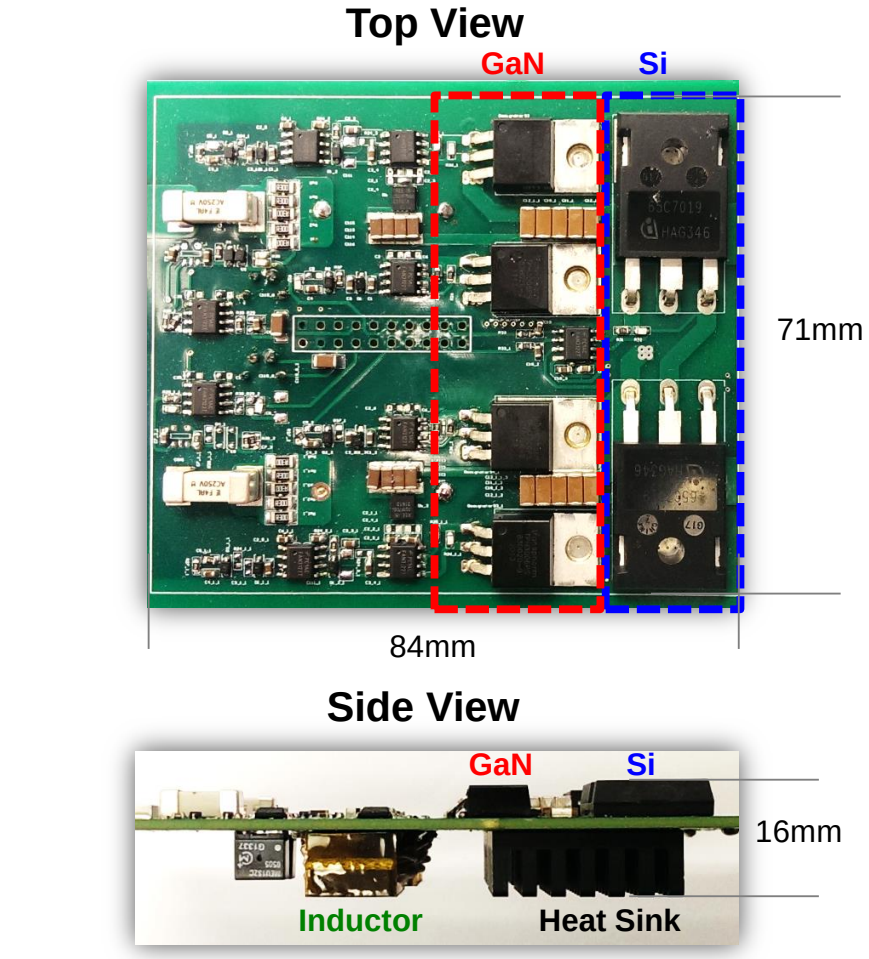
3.4 Hardware Demonstration

3.4.1 Discrete GaN vs. GaN Module

A MHz totem-pole PFC prototype is first demonstrated with discrete GaN devices. four discrete commercial cascode GaN devices in the TO-220 package (TPH3006PS) were used for the totem-pole bridgeless PFC rectifier, as demonstrated inside the red dashed circles in Fig. 3.37(a) and (b). The commercial cascode GaN device in the TO-220 package maintains the GaN HEMT and the Si MOSFET in a side-by-side configuration. The extra turn-on loss and turn-off ringing induced by this packaging structure severely impact the converter's efficiency and reliability. Additionally, the heat sink has to be mounted to the other side of the PCB, which makes thermal management difficult. Therefore, an integrated power module with the same functionality but improved electrical performance, reduced footprint/volume, and easy thermal management is greatly needed.


GaN HEMT
Si MOSFET
S12
S22
SN2
L1
L2
C
R
+
Vo
-
400V
VIN
200~240Vac
S11
S21
SN1

(a)


Top View
GaN
Si
71mm
84mm
Side View
GaN
Si
16mm
Inductor
Heat Sink

(b)

Fig. 3.37. Cascode GaN devices in dual-phase totem-pole bridgeless PFC rectifier: (a) circuit diagram and (b) PCB layout of the totem-pole bridgeless PFC with four discrete GaN devices in the red dashed circle. Inductors are mounted on the other side of the PCB

GaN-based multi-chip modules (MCMs) in three-phase bridge [C.37] and full-bridge circuit formats [C.38], [C.39] have been recently introduced, but they are still packaged in a traditional way that is similar to the Si-based insulated-gate bipolar transistor (IGBT) module. Some advanced packaging structures have also been developed for GaN-based half-bridge power modules to reduce power loop parasitic inductance and improve switching performance [C.40], [C.41]. But the manufacturing processes for these modules are quite complicated. In this work, a multi-chip GaN-based power module was built using the same packaging strategy employed for the discrete cascode GaN device in stack-die package. The module fabrication procedure starts with substrate preparation, followed by die-attachment and wire bonding processes. After soldering terminals and capacitors, the module is encapsulated and ready for testing.

Aluminum nitride direct-bonded-copper substrate (AlN–DBC; AlN 380 μm, Cu 170 μm) was used as the chip carrier for this power module assembly. The circuitry on top of the DBC substrate was developed using ferric chloride etching solution. Oxygen plasma was used to remove impurities and contaminants from the Cu surfaces before the plating process. The cleaned top Cu pads were electro-plated with nickel (Ni) and gold (Au) successively, as shown in Fig. 3.38(a). This additional metallization helps with the avoidance of the surface oxidation and facilitates the next die-attachment and wire-bonding processes.

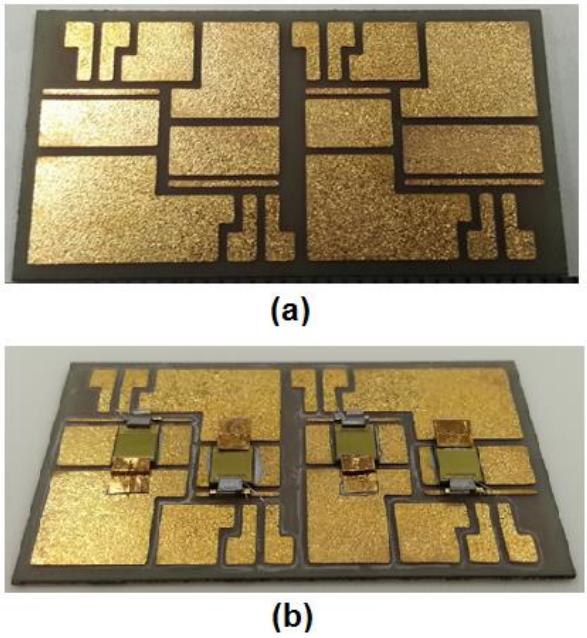


Fig. 3.38. (a) Patterned DBC substrate with Ni/Au plated surface; (b) cascode GaN devices mounted on the substrate in the stack-die structure. Cu sheets and bonding wires were used to make the inter-connections

Four pairs of 600 V GaN HEMT and 30 V Si MOSFET bare dice assembled in the stack-die structure were mounted on the DBC substrate, as illustrated in Fig. 3.38(b). The Si die was directly soldered on top of the GaN die with the assistance of a Cu spacer for the height adjustment. The solder jointly connects the drain terminal of the Si MOSFET to the source terminal of the GaN HEMT without wire-bonding. Au-plated Cu foils (200 μm thick) with preformed bends were also soldered simultaneously to make the electrical interconnection between the drain terminals of the GaN HEMTs and the designated area on the DBC substrate. After device soldering, 2-mil Al wires were bonded between the semiconductors and the electrical pads on the DBC substrate according to the optimized wire-bonding configuration.

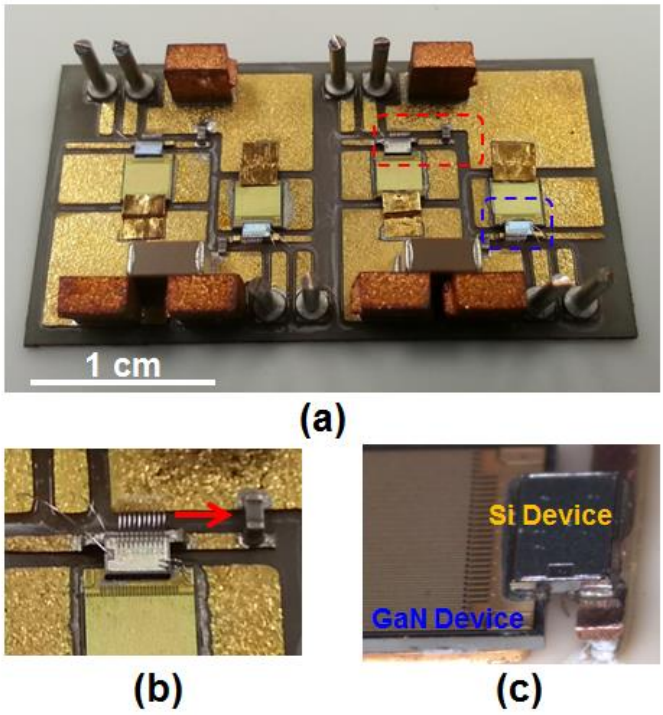


Fig. 3.39. (a) Fabricated GaN-based full-bridge power module with new features; (b) additional capacitor soldered in parallel to the drain-source terminals of the Si MOSFET; (c) zoomed-in image showing the stack-die structure

Four additional junction-capacitance-compensating capacitors and two decoupling capacitors, together with multiple Cu terminals, were soldered to the DBC substrate through another soldering reflow process. The solder paste used in this step is a lead-tin (Pb-Sn) eutectic composition ($Pb_{37}Sn_{63}$), which has a lower melting point of 183 °C compared to the one ($Sn_{89}Sb_{10.5}Cu_{0.5}$ solder paste with a melting temperature of around 240 °C) used for the device assembly. Therefore, solder joints formed in the previous stack-die attachment process will not reflow during this soldering step. Fig. 3.39(a) shows the assembled GaN-based MCM. Detailed features of the embedded capacitor and stack-die structure are provided in Fig. 3.39(b) and (c), respectively.

The fabricated MCM was placed into a silicone mold. The mold cavity was then filled with an epoxy-based encapsulant to cover all components in the package and subsequently cured for

one day at room temperature. After the encapsulated module was released from the mold, the extra parts of the Cu terminals were cut and ground to be flush with the surface of the cured epoxy encapsulant. Fig. 3.40 presents the encapsulated GaN-based MCM ready for electrical testing.

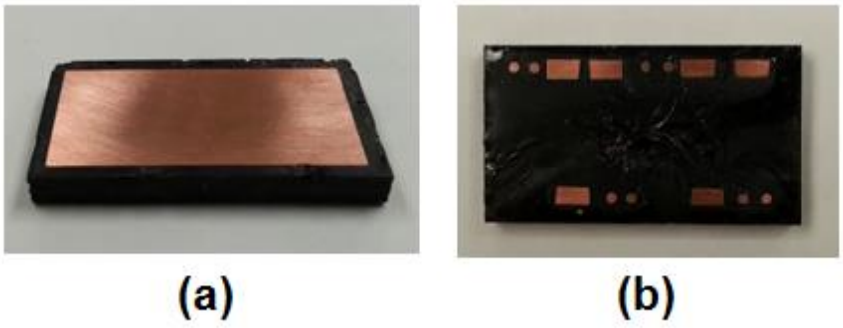


Fig. 3.40. GaN-based MCM encapsulated in epoxy material: (a) top Cu surface for direct heat sink attachment; (b) pin-terminals for surface-mount on the PCB substrate

The thermal performance of this GaN-based MCM was evaluated using both a finite element analysis (FEA) simulation tool and an infrared (IR) thermal imaging method. This simulation method has proven to be capable of accurately predicting the thermal performance of the discrete cascode GaN device [C.42]. Fig. 3.41(a) shows the built FEA 3-D thermal model for the power module with four cascode GaN devices.

The GaN-based power module was fabricated and mounted to a thermal test board (shown in Fig. 3.41(b) and (c)). The module was first conformal coated with silicone material for electrical isolation and protection. Then, a thin layer of black paint as used for the IR measurement of discrete device was applied on the surface for better IR image quality. Similar to the thermal analysis of the discrete stack-die packaged GaN device, different dc currents were applied to the power module to generate a series of power losses equivalent to different actual working conditions. Meanwhile, the same power losses were applied on the power module 3-D thermal model to simulate module temperature distribution.

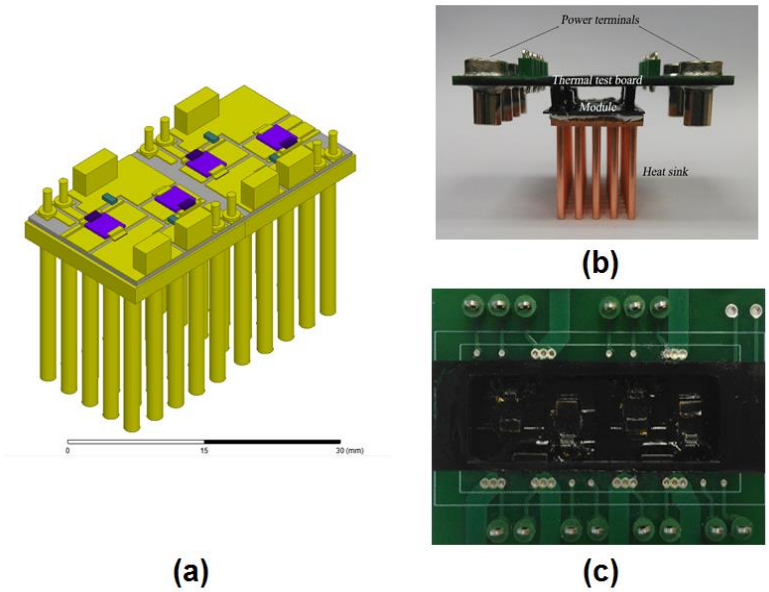


Fig. 3.41. (a) FEA 3-D thermal model; (b) side-view of thermal test board showing the heating sink attached to the DBC substrate; (c) top-view indicating the test area coated with black paint

An IR image of the experimental result and the thermal model temperature distribution are shown in figure below. The black box in Fig. 3.42 (a) is the boundary line of module and the other four small box are the temperature detecting zone set by IR camera. The comparison of simulation results and experimental results is shown in Fig. 3.43. The measured maximum temperature and the simulated peak temperature for the power module are almost the same.

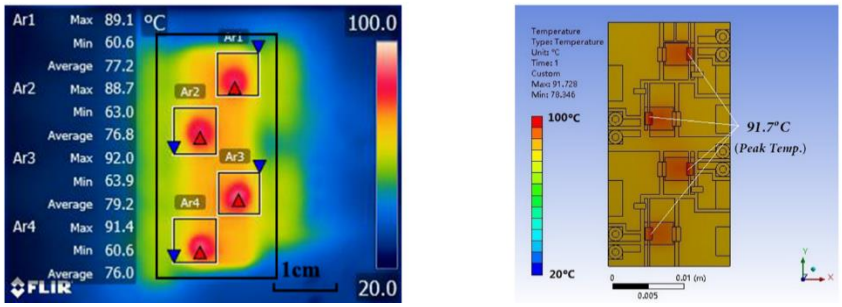


Fig. 3.42. Thermal analysis for the GaN-based power module: (a) Experimental IR image and (b) Simulation result. (Total power loss = 34 W, Ta = 20 °C)

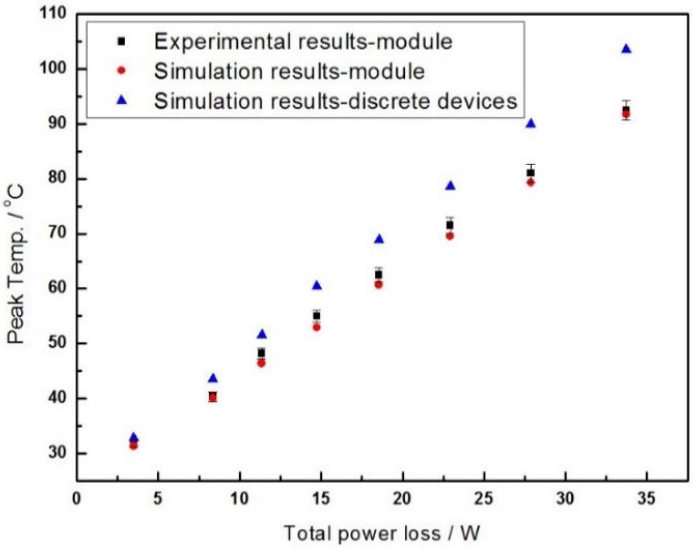
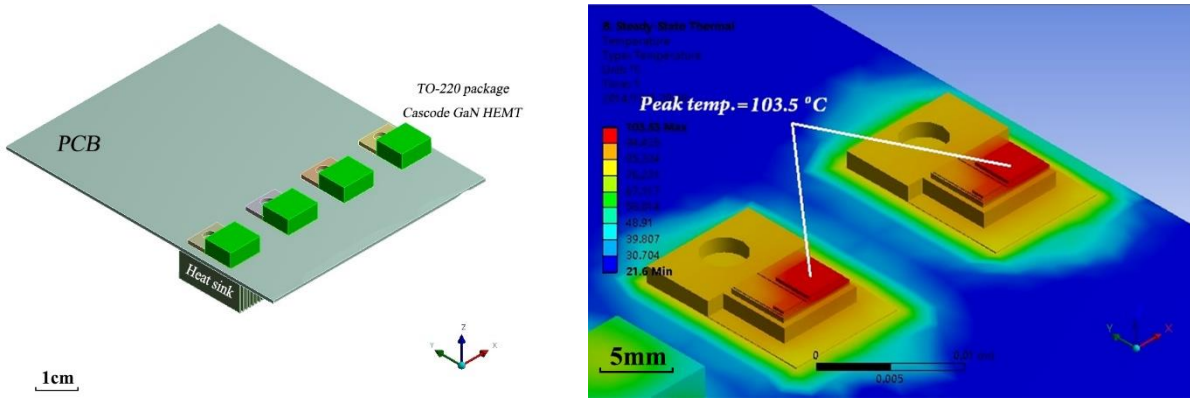


Fig. 3.43. Peak temperature comparison of GaN-based power module under different power losses

Moreover, in order to make a comparison of the thermal performance between discrete power GaN in TO-220 and proposed power GaN module, a 3-D thermal model of the totem-pole PFC rectifier with four discrete GaN devices was also built, as illustrated in Fig. 3.44 (a). A power loss equivalent to the other simulation conditions was applied to this model. The peak temperature shown in Fig. 3.44 (b) is around 103.5°C, which is nearly 12 °C higher than that of the new module simulated under the same conditions (used in Fig. 3.42 (b)). Therefore, the GaN-based multi-chip module has better thermal performance than the discrete devices for the designed totem-pole bridgeless PFC rectifier. The simulation results demonstrate that integrating cascode GaN devices in one module not only reduces the PCB footprint and increases the power density for the PFC rectifier but also improves the thermal dissipation capability. In addition, using Si and GaN dies in the stack-die packaging structure and the additional capacitors in parallel with the drain-source terminals of the Si MOSFET in this module can be expected to improve the electrical performance of this circuit. Hardware demonstration and experimental verification is included in the last of this chapter.



(a) (b)

Fig. 3.44. (a) Simplified thermal model for the PFC rectifier with four discrete GaN devices in the TO-220 package; and (b) Simulation result for PCB with four discrete GaN devices. (Total power loss = 34 W, Ta = 20 °C)

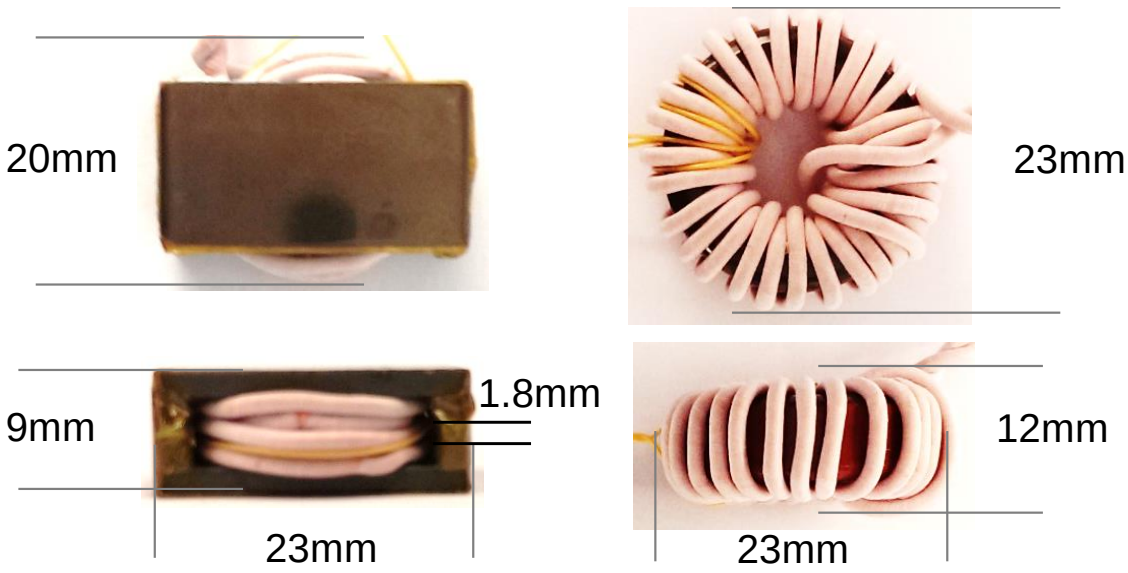
3.4.2 Discrete Inductor vs. Integrated Magnetics

The inductor design for MHz CRM PFC converter is also a challenge because at MHz frequency the winding loss usually increase significantly. Two inductors are made as examples shown in Table 3.3 and Fig. 3.45. The core loss and winding loss are measured according to the method proposed in paper [C.43], [C.44]. Inductor 2 made with powder core (-2 material from micrometals®) has high core loss owing to the nature of core material. On the contrary, the core loss of inductor 1 is smaller, however its winding loss is much higher than the other inductor although the winding length is much shorter. The significant winding loss of inductor 1 is highly related to the specific inductor structure, that the winding is embraced closely by the high permeability core material, so that MMF are exerted on a small volume of the winding area. This will cause higher magnetic field strength penetrating the winding and higher eddy current loss (Fig. 3.46). The large gap also generates more fringing flux, which makes the eddy current loss even higher. The toroid powder core is embraced by the winding, and the MMF around the winding is

exposed to the free space. So the eddy current loss on the winding is much lower compared to the ferrite case.

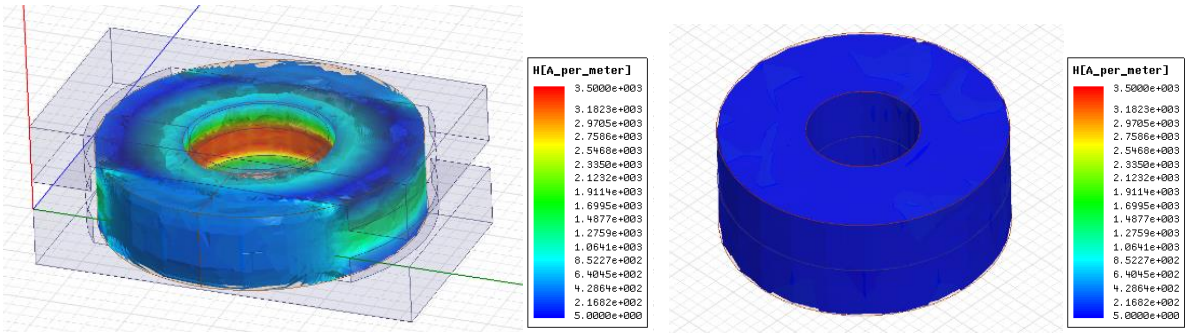
Table 3.3. Parameters of inductor design

	Inductor 1	Inductor 2
Material	Ferrite Ferroxcube 3F45	Powder Micrometals -2
Shape	ER23/3.6/13	T80(20.2/12.6/6.35)
Relative permeability	900	10
Winding	400/44 AWG	400/44 AWG
Turn	12	34
Core loss density (at $V_{in(t)\_peak}$)	1500kW/m^3	2600kW/m^3
Air gap	1.8mm	-
Core loss (at $V_{in(t)\_peak}$)	1.3W	3.11W
Winding loss (at $V_{in(t)\_peak}$)	3.76W	1.18W



(a) (b)

Fig. 3.45. Inductor design comparison. (a) inductor 1, (b) inductor 2



(a) (b)

Fig. 3.46. Simulated magnetic field strength in the winding regions of two studied cases, (a) The field penetrating the winding region in ferrite inductor (case 1), (b) The field penetrating the winding region of powder inductor (case 2)

The winding loss of litz wire is difficult to calculate very accurately. Here we use the square-field-derivative (SFD) method [C.45] to estimate the difference between the ferrite inductor (case 1) and the powder inductor (case 2).

With the simulated field, we can calculate the winding resistance of the two inductors, as shown in Fig. 3.47. At 1MHz, the ferrite inductor's resistance is about 3 times of the toroid powder inductor's, although it uses shorter winding. This is caused by higher field in the winding region, as the FEA simulation results shown in Fig. 3.46. To reduce the winding loss, litz wire with finer wire should be used.

With AWG 420/46 litz wire, both AC resistance of the ferrite and powder core can be reduced at 1MHz, as shown in Fig. 3.48. The ferrite core has more significant reduction because its winding loss is more sensitive to the penetrating field. With finer litz wire, the total inductor of the ferrite is lower than the powder core.

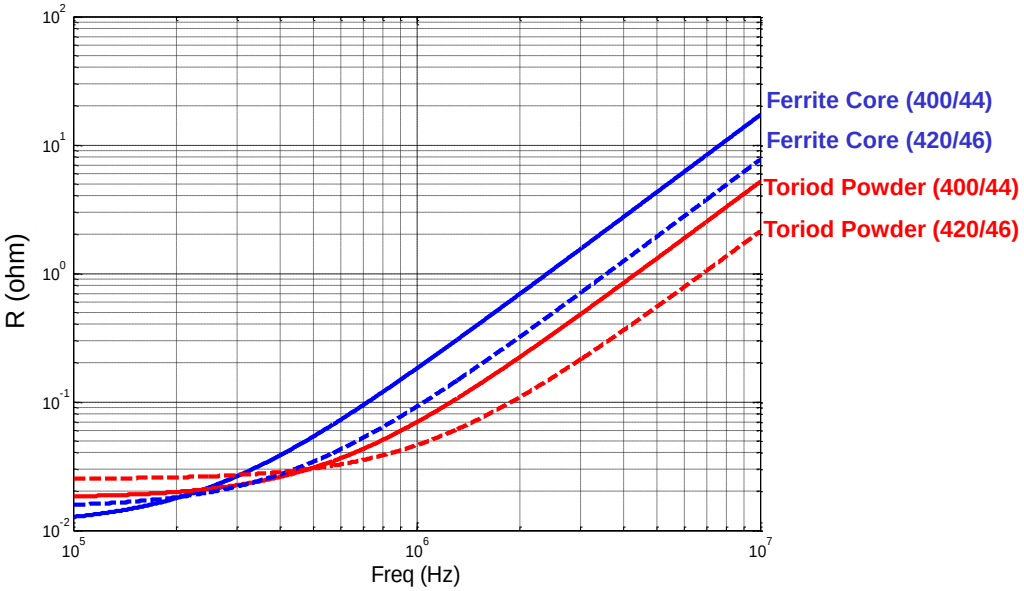


Fig. 3.47. Calculated AC winding resistance

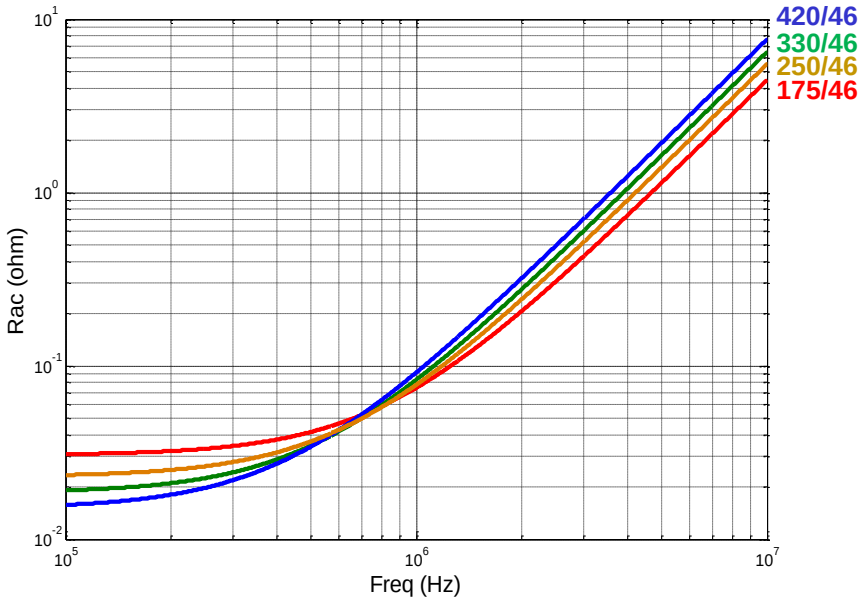


Fig. 3.48. Calculated AC resistance of different number of strands

The number of strands of the litz wire should also be optimized, because the more strands the lower DC loss but higher eddy current loss simply because more copper is exposed in the alternating field. Several litz wire with different number of strands are analyzed and tested.

As the comparison shown in Table 3.4, the inductor of lowest loss is the ferrite core with 250/46 litz wire is optimal. Its loss at the peak current is less than 2.8W, so the averaged loss over line cycle is even lower.

Table 3.4. Tested inductor with different number of stands

	DCR Loss/mW	ACR Loss/mW	Core Loss/mW	Total Loss/mW
170/46	596	1013	1300	2909
250/46	428	1066	1300	2794
330/46	362	1198	1300	2860
420/46	304	1308	1300	2912

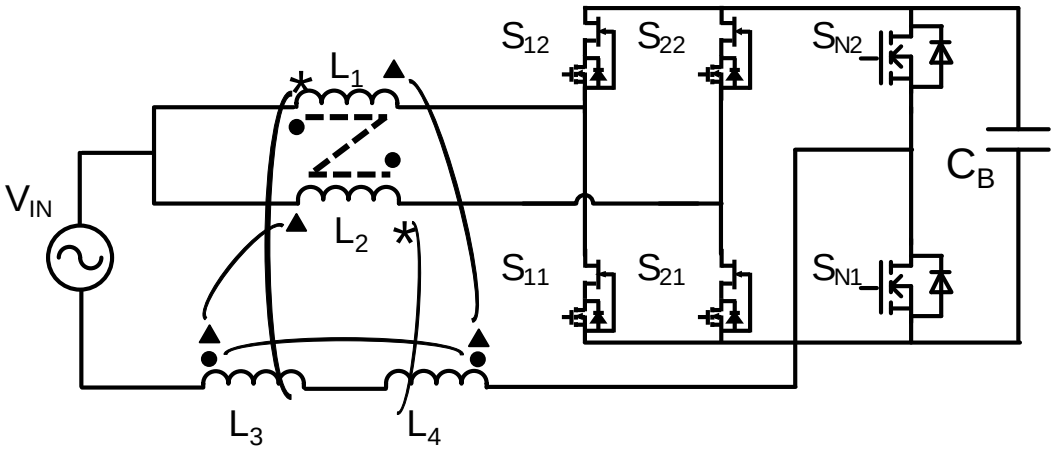


Fig. 3.49. Interleaved totem-pole PFC with inverse-coupled inductor and balance technique

As the switching frequency is increased to MHz, it is possible to integrate the inductors with PCB winding. At the same time, to further reduce the common-mode (CM) noise of the totem-pole PFC, balance inductors are added in the return path of the AC line so that the impedance of CM equivalent circuit is balanced and the CM noise is minimized. The totem-pole PFC with integrated inductor and balance technique is shown in Fig. 3.49. Detailed design considerations are published in [C.14].

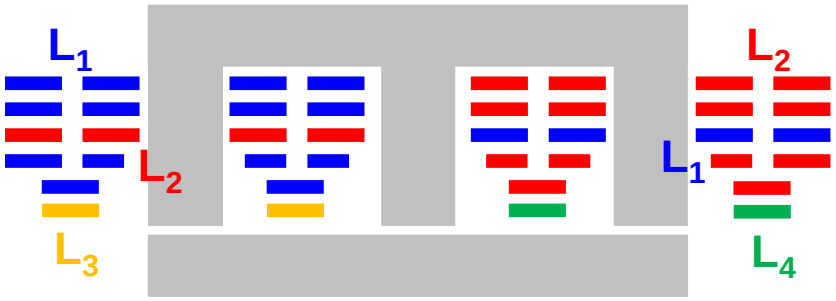


Fig. 3.50. Cross-section of integrated inductors with 6-layer PCB

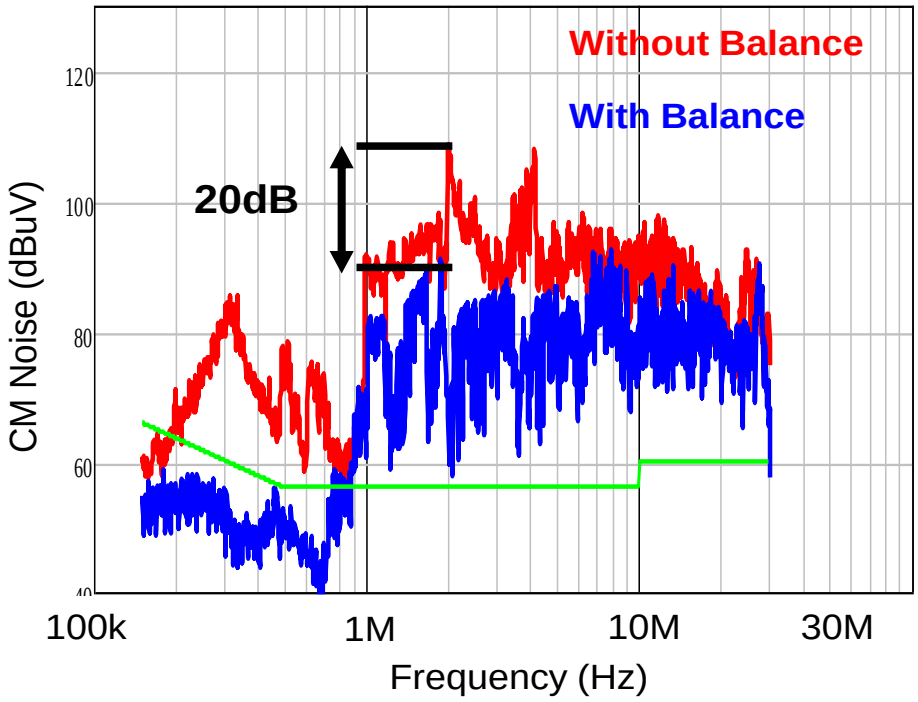
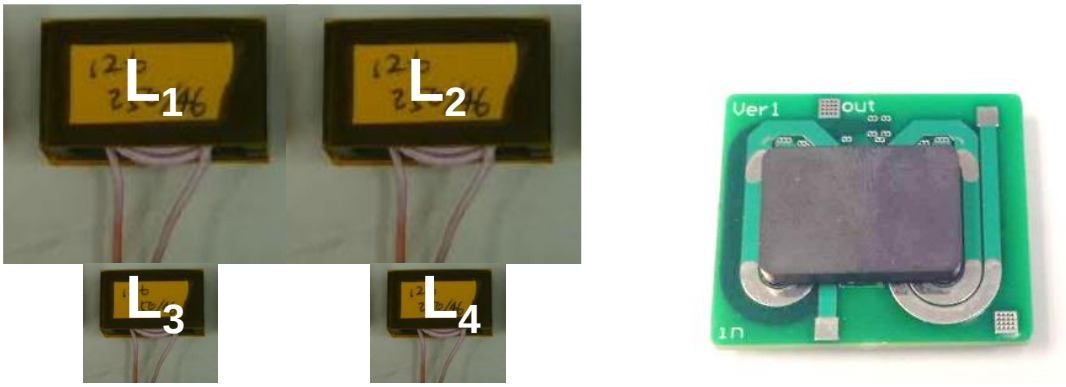


Fig. 3.51. Measured CM noise of the MHz totem-pole PFC

The coupled inductor is implemented with 6-layer PCB (Fig. 3.50). The main inductor for each phase are L_1 and L_2 which have five turns. One turn in the middle are swapped so that the winding of L_1 and L_2 are also interleaved. Since the current direction of L1 and L2 are opposite with 180 degree phase shift in the circuit operation, their magnetic flux are canceled by each other therefore the total AC winding loss are significantly reduced. One turn of L_1 and one turn of L_2 are relocated to the return path of the AC input so that the impedance of CM equivalent circuit are

balanced and consequently the CM noise is minimized [C.46]. The measured CM noise is shown in Fig. 3.51. 20dB reduction at 2MHz are observed by balance technique.

Fig. 3.52 is a comparison between conventional discrete inductors with litz wire winding and integrated inductors with PCB winding. To achieve similar electrical performance with discrete inductor, two large and two small inductors are required. The implementation is complicated and labor intensive. On the contrary, the proposed integrated inductor design has winding printed on the circuit board and well controlled coupling between four inductors so that it is possible to be made automated. The possible change on the manufacturing process is indeed a paradigm shift enabled by WBG devices.



(a) (b)

Fig. 3.52. Comparison between (a) discrete inductors and (b) integrated inductors

Finally, two totem-pole PFC prototypes are demonstrated as Fig. 3.53. Gen. 1 is the preliminary version with commercial cascode GaN device in TO-220 package. The inductor is underneath the PCB and made by litz-wire winding. Relative large heat sink is required since the device is soldered on PCB and most of the heat generated by the GaN devices has to go through PCB first and then reaching heat sink. 200 W/in^3 power density (without bulky cap) is achieved by Gen. 1.

Gen. 2 is an enhanced version with both GaN module, integrated inductor, and improved layout. Gen. 2 has higher efficiency due to eliminated cascode GaN internal non-ZVS loss; higher power density due to more compact module, inductor, and layout; better thermal conductivity due to directly attached heat sink to the module; and better reliability due to enhanced GaN module. [C.10]

(a)

(b)

Fig. 3.53. MHz totem-pole PFC prototypes (a) Gen. 1 with discrete GaN devices and litz wire inductors (b) Gen. 2 with GaN module and integrated inductors

Fig. 3.54 is the measured efficiency for both Gen. 1 and Gen. 2. With internal non-ZVS loss elimination, the efficiency is improved from Gen. 1 to Gen. 2 and the peak reaches 99%. It is as

good as state-of-the-art PFC operating at 100 kHz but has significantly improved power density and simple manufacturing process.

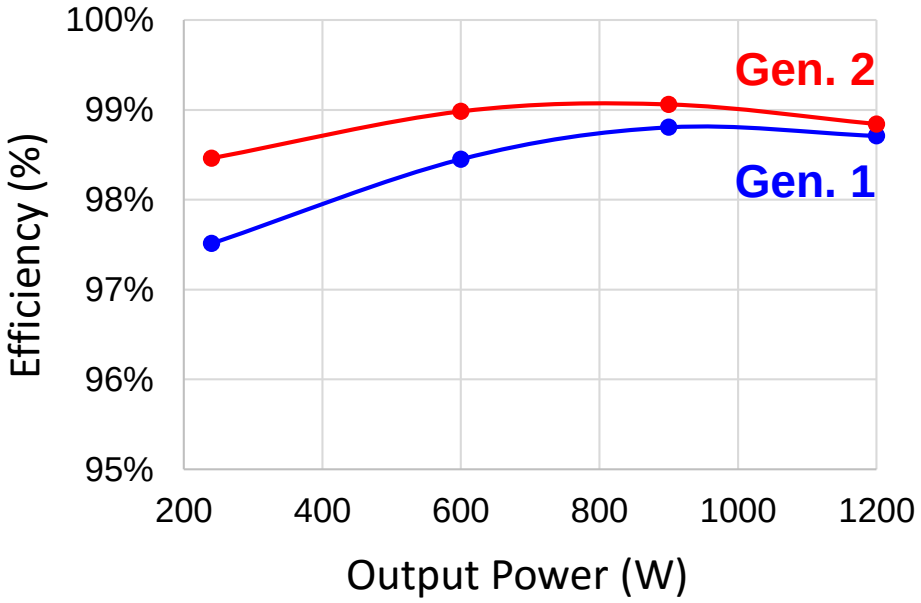


Fig. 3.54. Measured efficiency of the MHz totem-pole PFC

Chapter 4. Bidirectional Rectifier/Inverter

For applications like computer, server, and telecommunication power supplies, only unidirectional power flow is required from AC grid to DC load. While for applications like battery charger, renewable energy and energy storage system, bidirectional operation is desired.

The totem-pole PFC is naturally bidirectional since all switches are active switch with bidirectional power flow capability. Therefore it is possible to extend it from AC/DC rectifier to DC/AC inverter. This chapter focuses on the extension of totem-pole PFC to inverter mode and applied it to an on-board charger system for electrical vehicles.

4.1 Design Consideration for Grid Interface

4.1.1 Development of Universal Controller

The CRM PFC rectifier can achieve a good power factor with simple voltage mode and constant on-time operation. However, for the CRM inverter there is no simple way to achieve a good power factor other than conventional current-mode control. So far very little can be found in the literature regarding the CRM inverter. References [D.1]-[D.4] use hysteresis control for the CRM inverter. However the current-sensing method in [D.1]-[D.4] is not applicable for a multi-phase interleaved structure. High-frequency instantaneous current sensing actually becomes the bottleneck for the CRM inverter using hysteresis control. For example, the RC switching network based current sensing method [D.5] is not applicable, since the common-mode voltage across the inductor is too large in offline applications; the sensing resistor in series with the bottom switch doesn't work in the negative line cycle; the sensing resistor in the return path is good for single-phase topology but not applicable for a multiphase topology with interleaving; and the current

transformer (CT) method is applicable, but each high-frequency switch needs one CT connected in series, which makes the critical power loop very large, which can induce significant switching loss and parasitic ringing.

In order to avoid instantaneous current sensing, a hybrid control strategy combining average current control and part hysteresis control is proposed, as illustrated in Fig. 4.1. The average current loop shown by the blue curve controls the average current to track the desired sinusoidal reference; at the same time the zero current detection and programmed extra off-time control block, shown in green, controls the switching cycle CRM operation to achieve ZVS through the entire line cycle. It is equivalent to determining the negative current boundary.

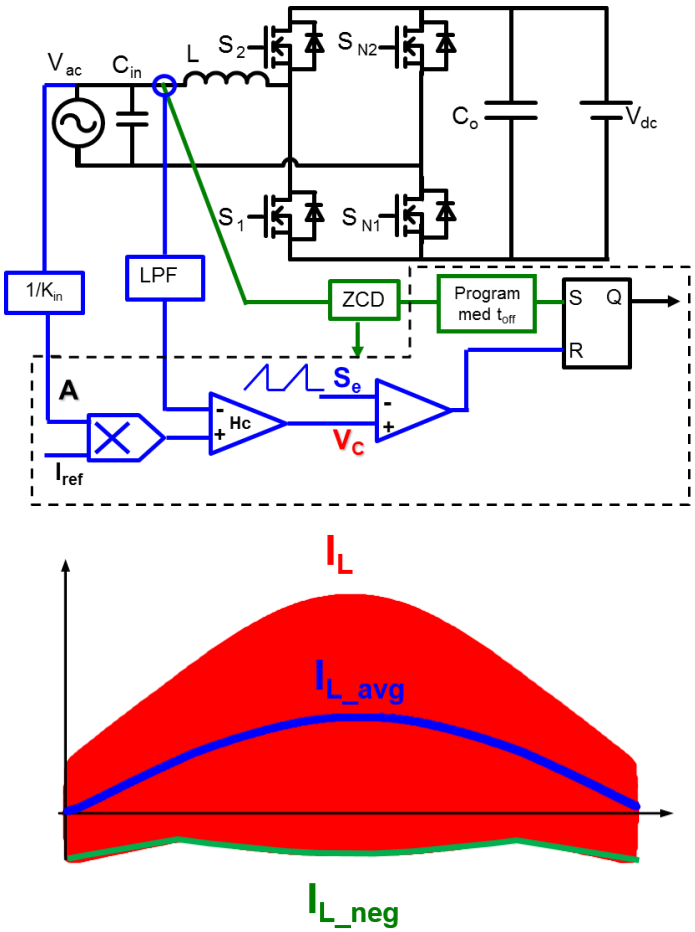


Fig. 4.1. Proposed CRM PFC/inverter with average current mode control

Microcontroller (MCU) TMS320F28075 is used to implement the proposed control. Details regarding the digital implementation are included in [D.6], [D.7]. The components included in the black dash-line box are all implemented by software in MCU. Low cost hall sensor ACS714 in SO-8 package is used to sense the average inductor current. It has limited bandwidth (up to 80 kHz) so that switching cycle current information is attenuated. However as only the average current at line frequency is to our interest so the bandwidth of the Hall sensor is adequate. The low pass filter (LPF) is optional. After two phase interleaving, the ripple current is significantly reduced due to 180o phase shift so in actual two phase implantation the LPF is not used. Proportional–integral (PI) controller is adopted to regulate the average current and it is also implemented by software in MCU.

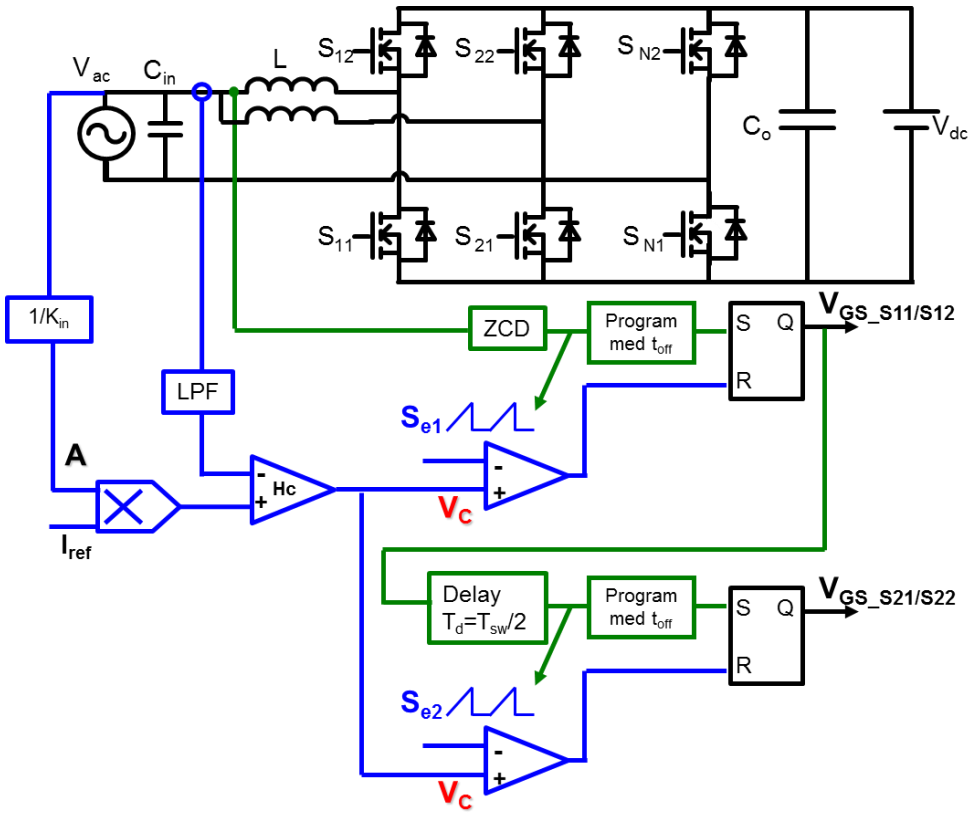
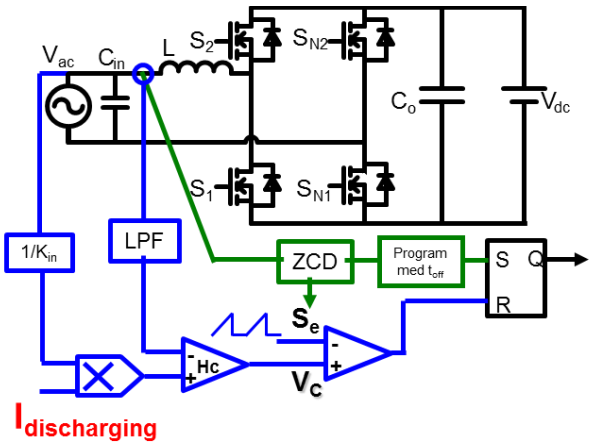


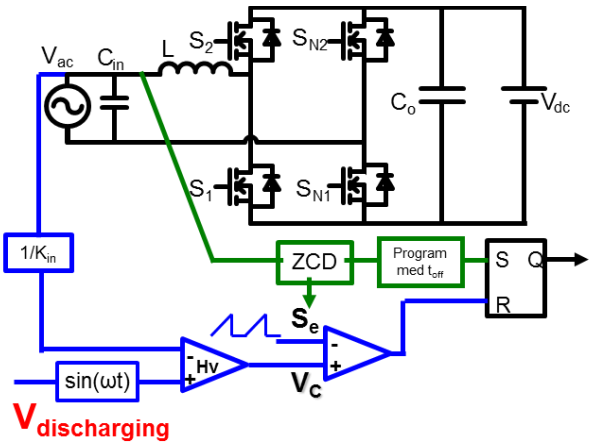
Fig. 4.2. CRM PFC/inverter with average current mode control and open-loop interleaving

For the two-phase interleaved CRM totem-pole PFC, the complete control diagram is shown in Fig. 4.2. As discussed in [D.23], open-loop interleaving method is used for more accurate variable frequency interleaving control at high switching frequency. One phase is treated as master phase and the other one is treated as slave phase.

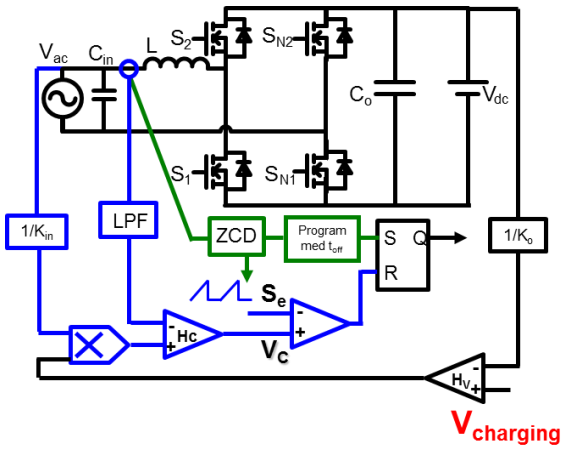
The basic concept shown in Fig. 4.1 can be used in grid-tied inverter, grid-tied rectifier, and stand-alone inverter (all shown in the figure below). Thus this control is universal for all operating conditions of the bidirectional on-board charger.



(a)



(b)



(c)

Fig. 4.3. Universal control for (a) grid-tied inverter, (b) stand-alone inverter, and (c) grid-tied rectifier

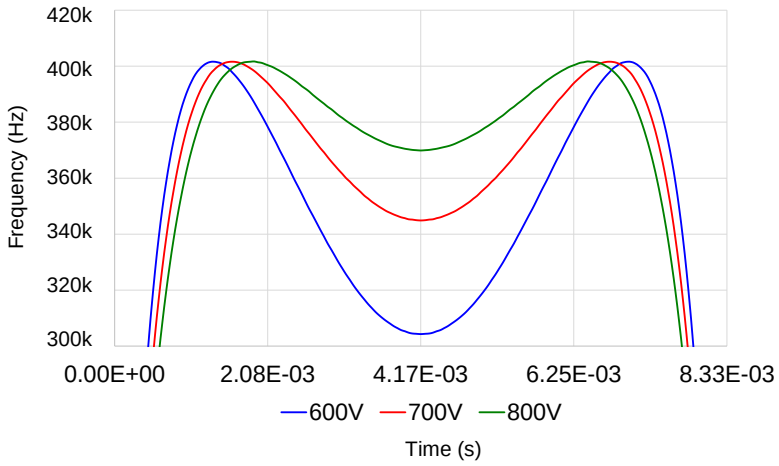


Fig. 4.4. Switching frequency distribution in half line-cycle at full load with different DC-link voltages

With ZVS soft-switching and small turn-off loss, it is possible to dramatically raise the switching frequency of the device. In this way the volume of the passive components and the EMI filter can be significantly reduced. However, the switching frequency of CRM PFC is variable for a large range, and it is important to evaluate this comprehensively. The inductor is designed so that at full-load conditions the minimum switching frequency with the highest current ripple (the

middle of the half-line cycle) is 300 kHz. Figure below shows the switching frequency distribution in a half line-cycle.

4.1.2 Achieving ZVS in Both Rectifier and Inverter

One important issue of a totem-pole PFC rectifier operating in CRM is that zero-voltage-switching cannot be realized through the entire line cycle. ZVS depends on the relation between input and output voltage.

As the switching frequency is targeted at above 300 kHz, failure to achieve ZVS causes significant switching loss and efficiency drop. The figure below is a comparison which shows the importance of achieving ZVS.

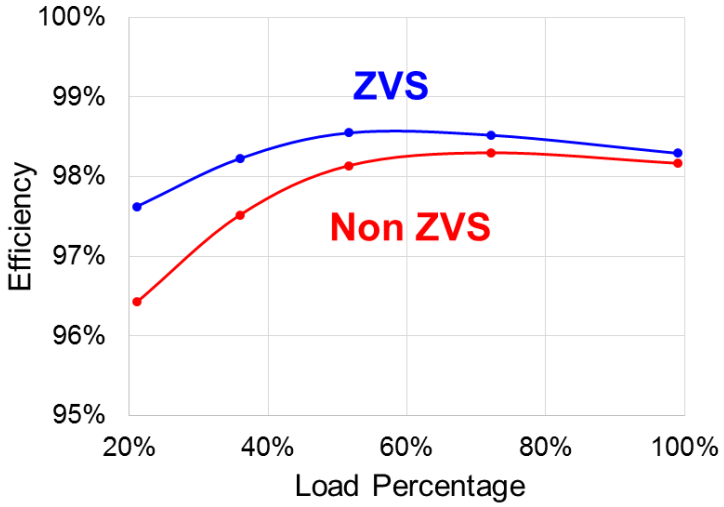
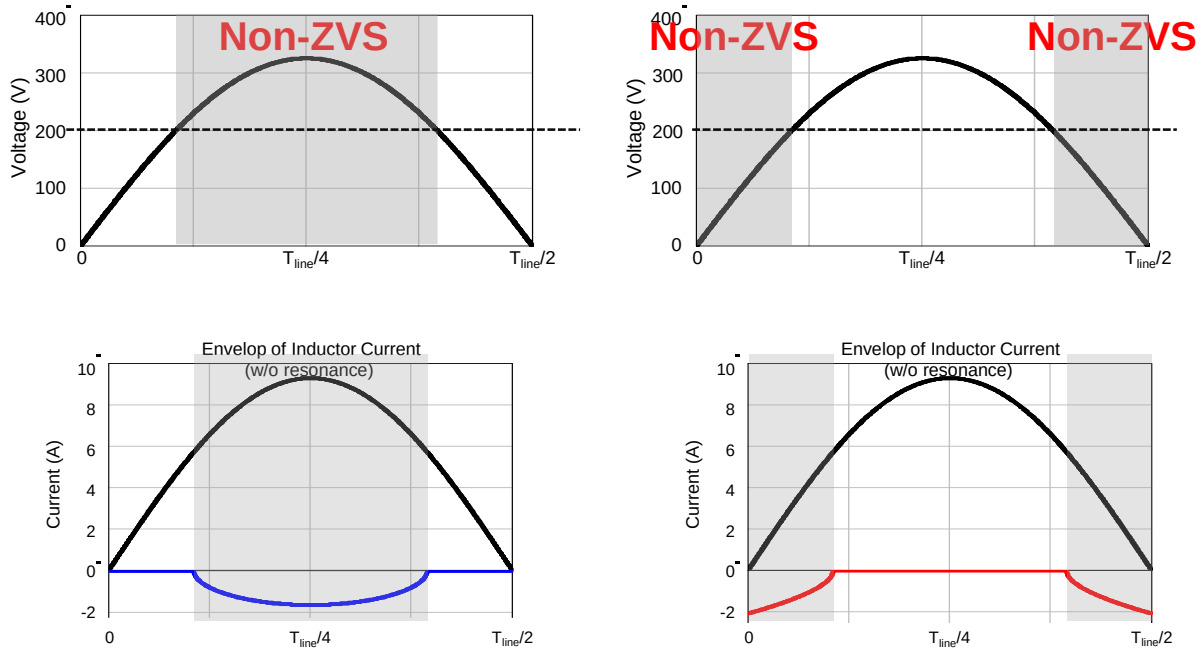


Fig. 4.5. Estimated efficiency curve of AC/DC stage in inverter mode at 240Vac and 800Vdc condition and a minimum frequency of 300 kHz

In order to realizing ZVS through entire line cycle, a ZVS extension strategy was proposed to solve this issue for GaN-based MHz totem-pole PFC. The similar concept can be used here, but a new concern is that the non-ZVS region is different for rectifier mode and inverter mode. Actually,

due to the feature of duality, the non-ZVS region is complementary between the rectifier and inverter. Fig. 4.6 shows the non-ZVS region in the shaded area and the corresponding desired extra negative current needed to achieve ZVS. The extra negative current is realized through programmed extra off-time. Equation (4.1) and (4.2) are used to calculate the required extra negative current. (i_{neg_rec} and i_{neg_inv} is the negative current in rectifier mode and inverter mode respectively; V_{ac} is the AC voltage; V_{dc} is the DC voltage; L in the inductance value of boost inductor; and Coss is the time equivalent output capacitance from 0V to V_{dc} of the 1.2kC SiC MOSFET). Fig. 4.7 shows the simulation waveform to verify ZVS extension for both rectifier mode and inverter mode. The simulation leaves a slight margin to guarantee ZVS. Otherwise the two waveforms should be identical, because both the topology and the operation mode have good symmetry.



(a) (b)

Fig. 4.6. Non-ZVS region and envelope of inductor current with ZVS extension operation for (a) rectifier mode and (b) inverter mode

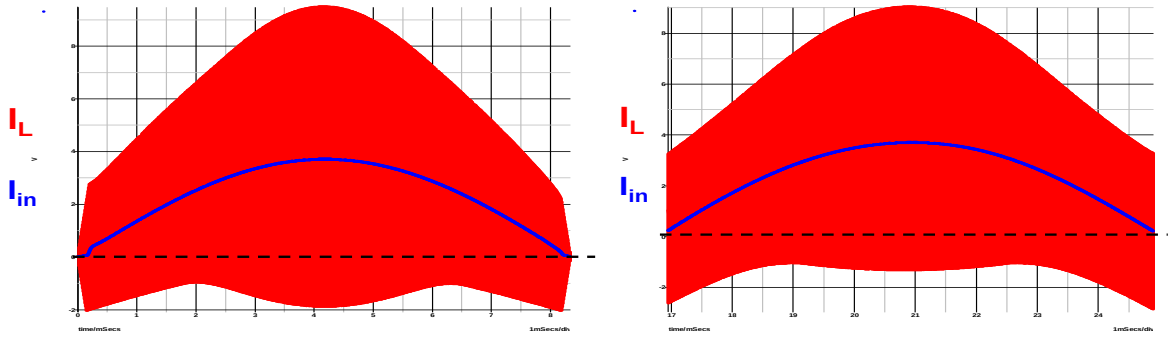
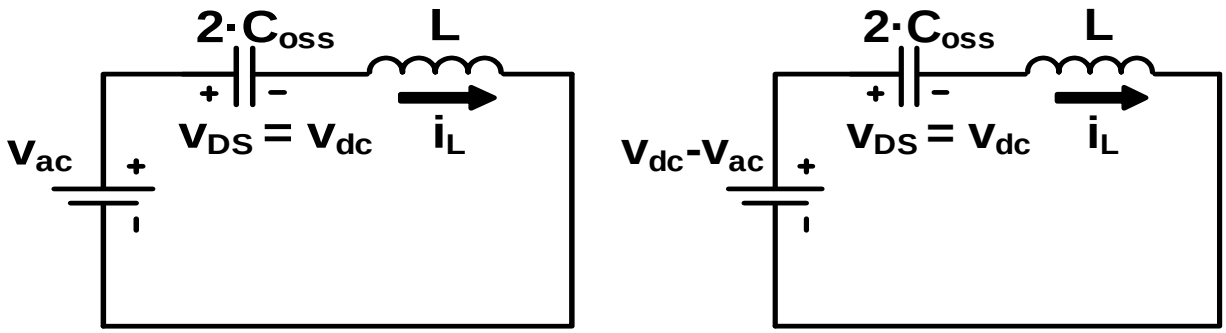


Fig. 4.7. Inductor current simulation waveform for (a) rectifier mode and (b) inverter mode

$$i_{neg\_rec}(t) = \frac{\sqrt{[2v_{ac}(t) - v_{dc}(t)]v_{dc}(t)}}{\sqrt{L/2C_{OSS}}} \quad (4.1)$$

$$i_{neg\_inv}(t) = \frac{\sqrt{[v_{dc}(t) - 2v_{ac}(t)]v_{dc}(t)}}{\sqrt{L/2C_{OSS}}} \quad (4.2)$$

The equivalent circuit during resonant time is shown in the figure below and state trajectories are used to illustrate the mechanism of non-ZVS and the ZVS extension.

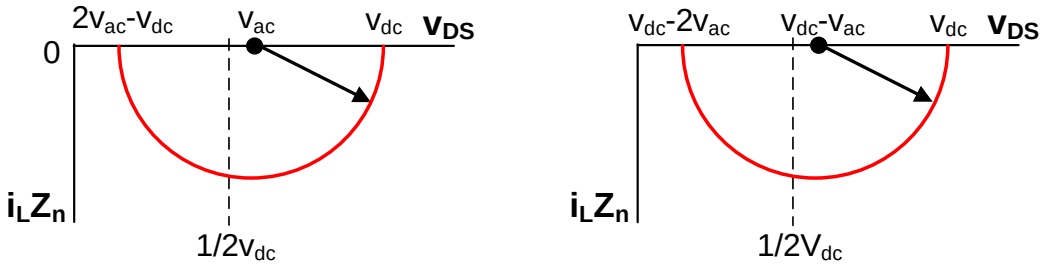


(a) (b)

Fig. 4.8. Equivalent circuit during resonant time (a) rectifier mode and (b) inverter mode

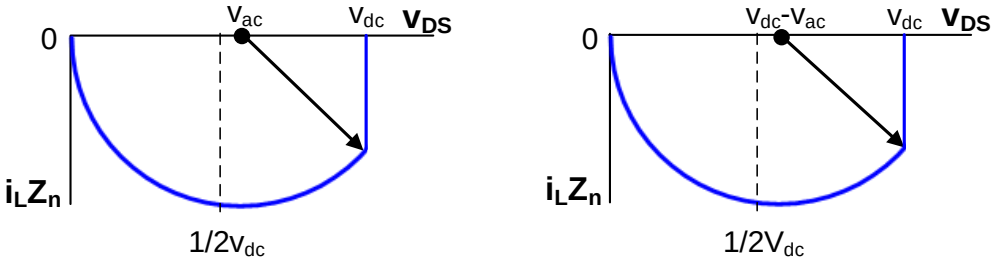
As the DC-link voltage is variable from 500V to 840V, the ZVS extension region is different for different DC-link voltage. As an example, Fig. 13 shows different non-ZVS regions. The boundary of ZVS and non-ZVS is when AC input voltage is equal to half of DC output voltage. Therefore at charging mode, the lower DC output voltage, the larger non-ZVS region. The peak of

the AC input voltage is about 340V so that when the DC output voltage is higher than 680V ZVS can be achieved through the line cycle. The non-ZVS of inverter is complimentary of rectifier.



(a) (b)

Fig. 4.9. State trajectory during resonant time for (a) rectifier mode and (b) inverter mode



(a) (b)

Fig. 4.10. State trajectory during resonant time with ZVS extension for (a) rectifier mode and (b) inverter mode

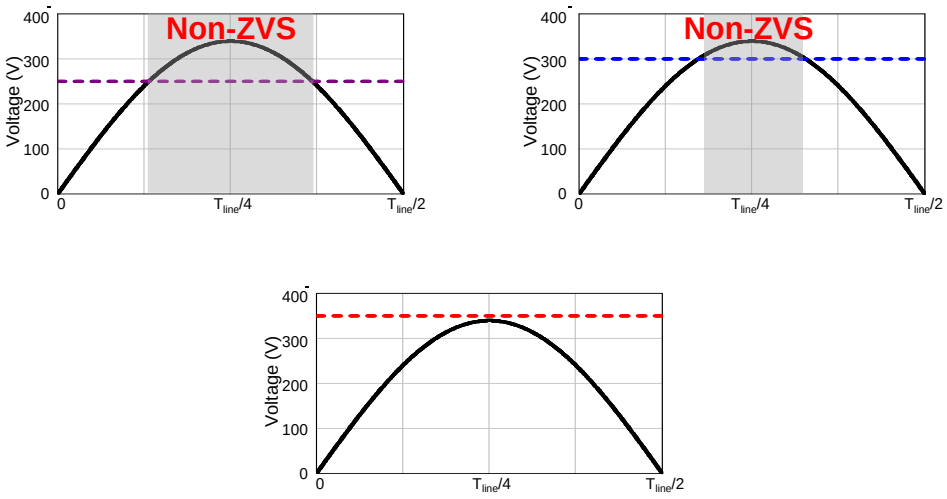


Fig. 4.11. Non-ZVS regions with different DC-link voltages and nominal 240Vac input at charging mode, when VDC=500V, VDC=600V, VDC=700V

4.1.3 Light Load Efficiency Improvement

The critical mode PFC is operating in variable frequency in nature. Loading percentage has strong impact on the frequency. The figure below shows the frequency distribution in half line cycle with different loading conditions. The input voltage is 240Vac and the output voltage is 600Vdc.

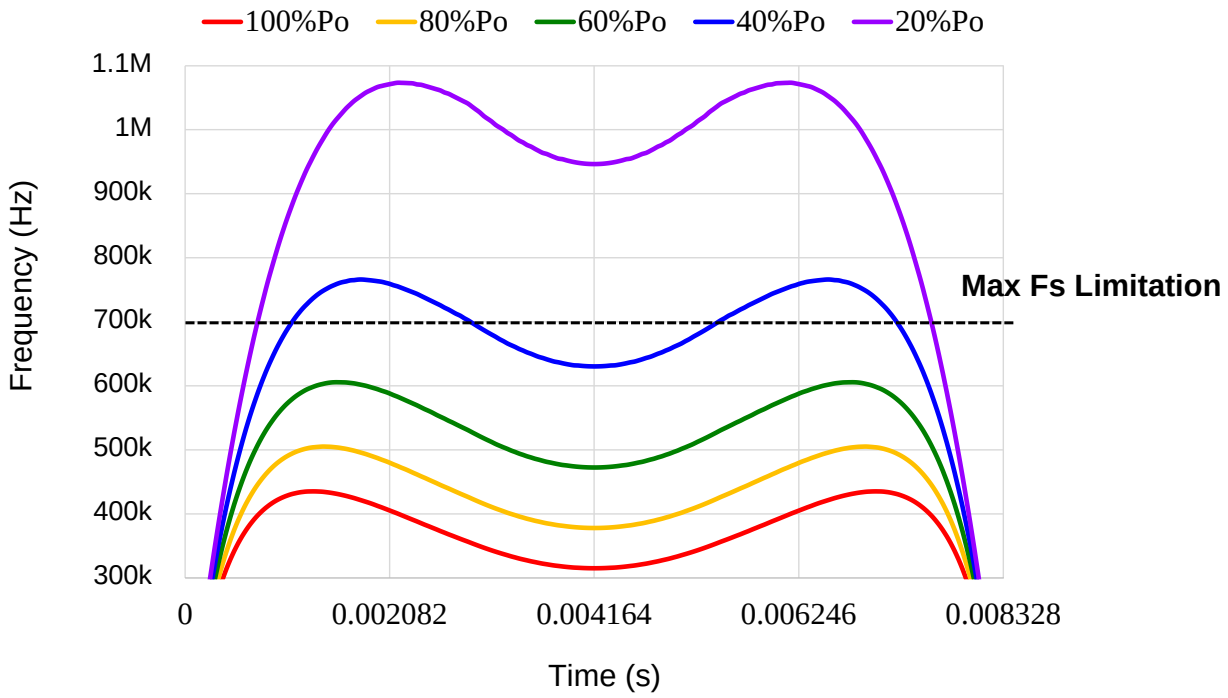


Fig. 4.12. Frequency distribution in half line cycle at different loading conditions. (240Vac, 600Vdc, full load 6.6kW)

As we purposely designed the frequency at peak of a half line cycle equals to 300 kHz at full load condition, the frequency is above 400 kHz in sometime within the half line cycle due to the variation of input sinusoidal waveform. Then from heavy load to light load, the input current keeps decreasing which leads to frequency increasing. Without frequency limitation, at 20% load

condition, the frequency is above 1 MHz. Due to the large frequency variation, the light load efficiency suffers.

The efficiency curve shown in Fig. 4.5 shows a quick drop in efficiency at light load conditions. In order improve light load efficiency, a frequency limitation is applied to the PFC as shown by the black dash line in the above figure.

When the original frequency is below the applied limit, the circuit maintains critical mode and when the original frequency is above it, the circuit enters DCM mode. Basically the off time is extended so that the inductor current stays at zero (resonating around zero considering parasitics) and the equivalent switching frequency is reduced.

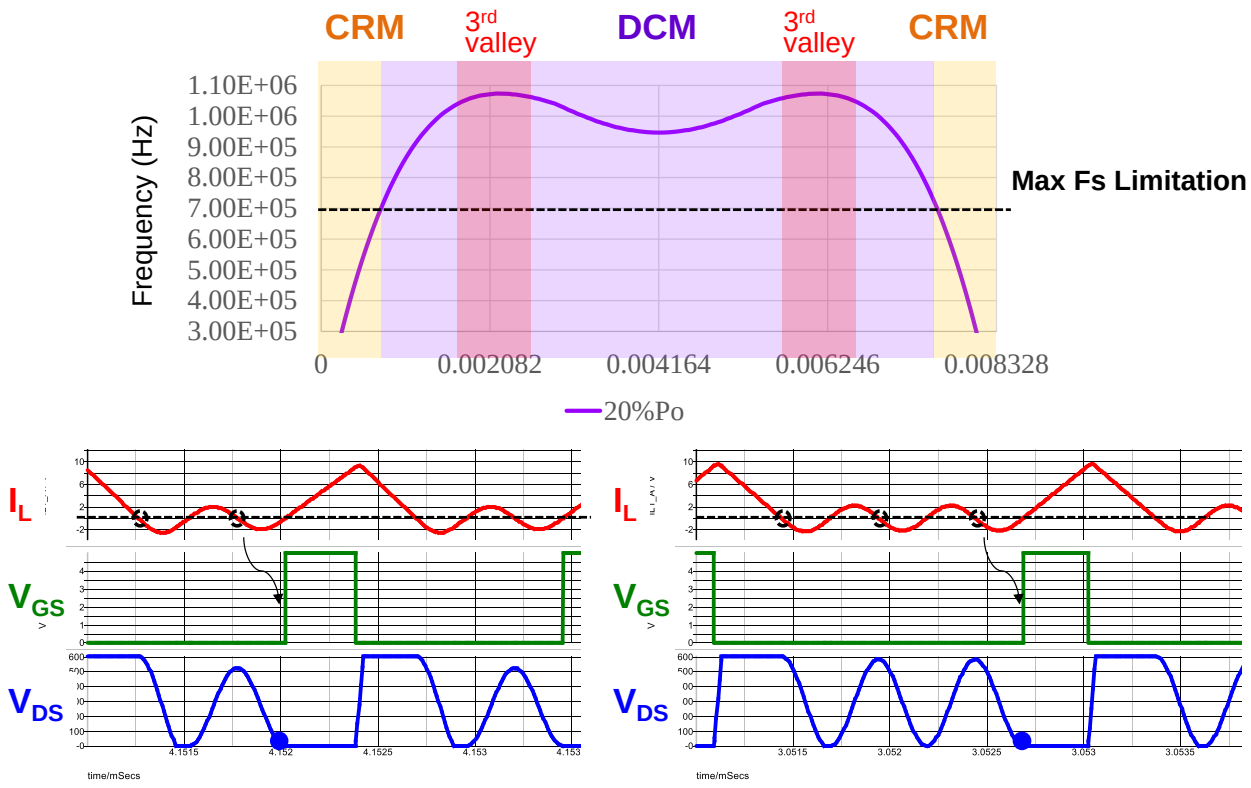
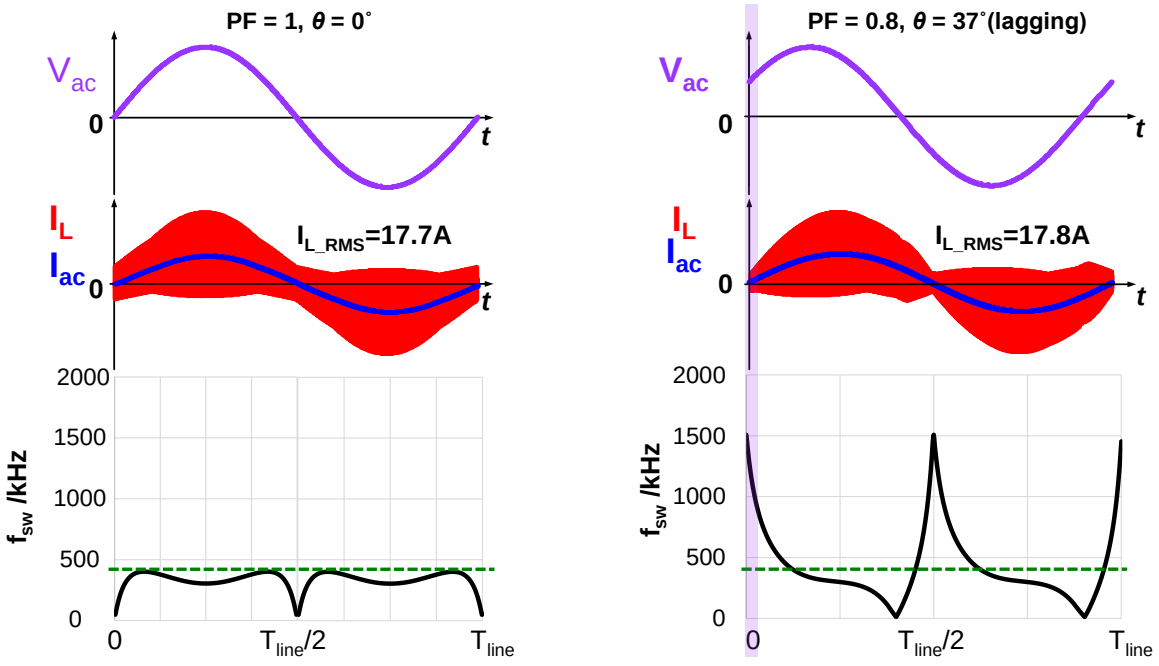


Fig. 4.13. Frequency limitation with DCM and valley skipping (20% load)

At the same time, valley skipping is used to keep non-ZVS loss as small as possible. The figure below shows the typical waveforms in a half line cycle at 20% load. The yellow area around AC line zero crossing indicates critical mode; the purple area in the middle is DCM specifically the circuit skips the first valley in the beginning and then it skips the second valley as well then frequency goes even higher like what is included in the red area. As a result, the light load efficiency is effectively improved.

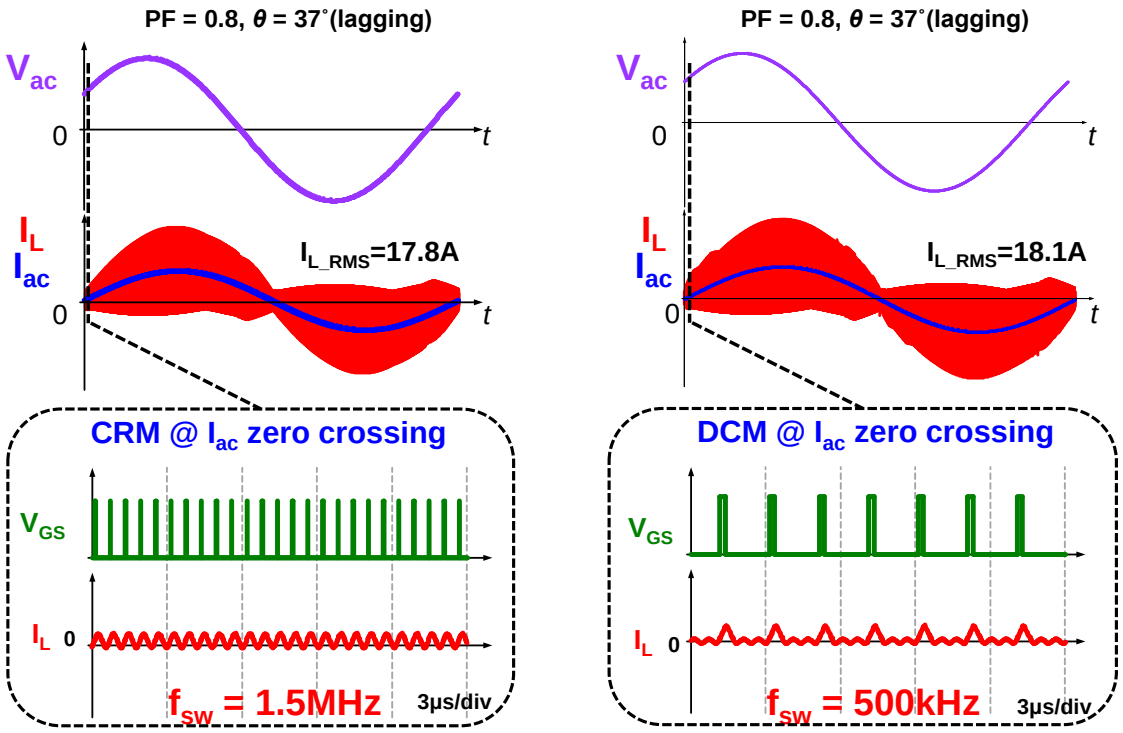
4.1.4 Provide Reactive Power

Reactive power is often required for a grid-tied inverter. The CRM totem-pole inverter is capable to support reactive power. Fig. 4.14 shows the simulation waveform when power factor is 1 and power factor is 0.8.



(a) (b)

Fig. 4.14. Simulation waveform and frequency distribution for CRM inverter with (a) unity power factor and (b) non-unity power factor



(a) (b)

Fig. 4.15. Simulation waveforms (a) before frequency limiting (pure CRM) and (b) after frequency limiting (CRM + DCM)

However the issue is at non-unity power factor condition, the zero crossing of AC current and AC voltage are not at the same time instant. During AC current zero crossing the AC voltage is not zero so that the switching frequency has to be pushed to very high value to maintain critical mode operation.

The drastically increased switching frequency induces large switching loss and driving loss. To solve this issue, frequency limiting with discontinues conduction mode (DCM) is adopted as in Fig. 4.15. Therefore the frequency during AC current zero crossing is clapped at around 500 kHz. It is one-third of natural CRM operation which means significantly reduced switching loss and driving loss.

4.2 Proposed Novel System Architecture for On Board Charger (OBC)

One of the most desired application for bidirectional AC/DC rectifier and inverter is on-board battery charger (OBC) for electrical vehicle applications.

Plug-in electric vehicles (PEVs), which include plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs), are becoming more and more popular due to their more efficient energy utilization and reduced combustion emissions. One crucial challenge of PEV commercialization is the demand for a lightweight, compact, and efficient on-board charger (OBC). The state-of-the-art level-2 OBC systems in volume production currently use Si-based technology. This restricts the maximum switching frequency up to 100 kHz which achieves only 3-12 W/in3 power density and at most 92-94% efficiency [D.14]-[D.15].

Emerging wide-band-gap (WBG) power semiconductor devices eliminates the need for the series low-voltage MOSFET and parallel fast-recovery diode since the reverse recovery effect of body diode is eliminated. Three power device for each switch using Si are replaced by a single device using GaN or SiC.

Furthermore, WBG devices provide the technology that enables a dramatic increase in the efficiency and power density of switch-mode power supplies with the potential for lower cost and better manufacturability. A high-efficiency, high-density on-board charger using E-mode GaN HEMTs has recently been demonstrated [D.15]. However the system is relatively complicated due to the added active filter and too many devices in parallel.

In this work, both 600V GaN devices and 1200V SiC MOSFETs are used to design a 6.6 kW OBC system. The target is to increase the switching frequency to be higher than 300 kHz and to achieve doubled or tripled power density, at least 95% efficiency, and integrated magnetics with

PCB winding and bi-directional power flow. Therefore the proposed design has not only good performance but simplicity and good manufacturability. The chart shown in Fig. 4.16 summarizes the state-of-the-art products [D.14]-[D.15] and the design target in this paper.

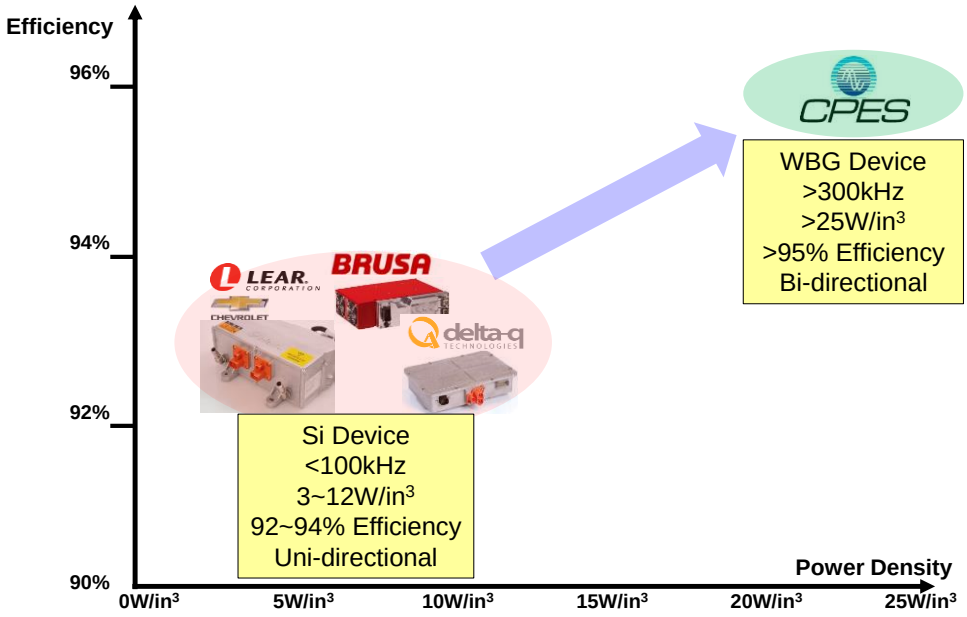


Fig. 4.16. Efficiency and power density of state-of-the-art products and target

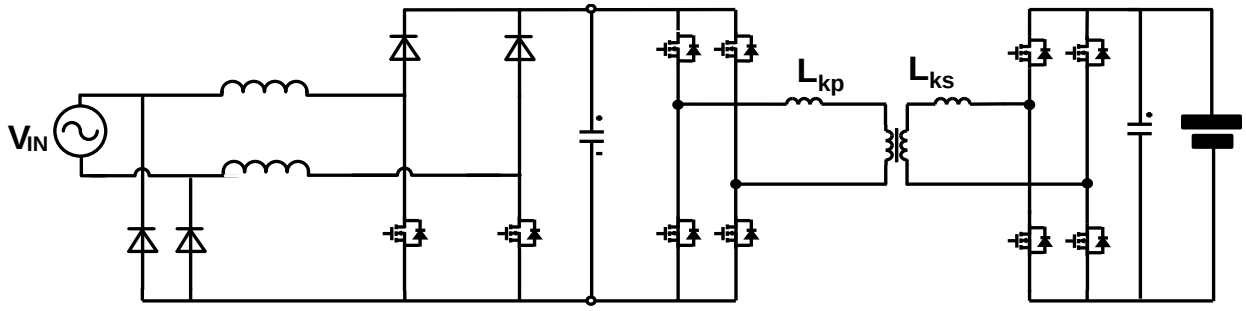


Fig. 4.17. Conventional Si-based OBC system architecture

Limited by the large reverse-recovery charge of Si MOSFETs, a conventional Si-based OBC design is unidirectional. Two-stage structures are most popular (Fig. 4.17), in which the first stage is usually a dual-boost bridgeless PFC rectifier to provide a fixed DC-link voltage and unity power factor; the second stage is usually a dual-active-bridge (DAB) isolated DC/DC converter which

provides the functions of isolation and regulation. The drawbacks of a dual-boost PFC rectifier are its unidirectional power flow and significant switching loss. The drawback of a DAB converter is high turn-off loss and limited ZVS region.

For use with WBG devices, the proposed topology is a totem-pole bridgeless PFC rectifier operating in critical conduction mode (CRM) as the AC/DC stage, and a CLLC resonant converter as the DC/DC stage. Fig. 4.18 shows the target lithium-ion battery charging profile. The basic system structure is shown in Fig. 4.19(a), which has a 400 V fixed DC-link voltage. The control of this structure is simple, but the challenge is that for PEV applications the output of the OBC system is connected to a battery that has a very wide voltage range. In order to have more flexibility, the actual output voltage range is set from 250 V to 450 V, which is close to a two-to-one variation. Therefore the wide output voltage range is a serious challenge to the design of the CLLC resonant converter.

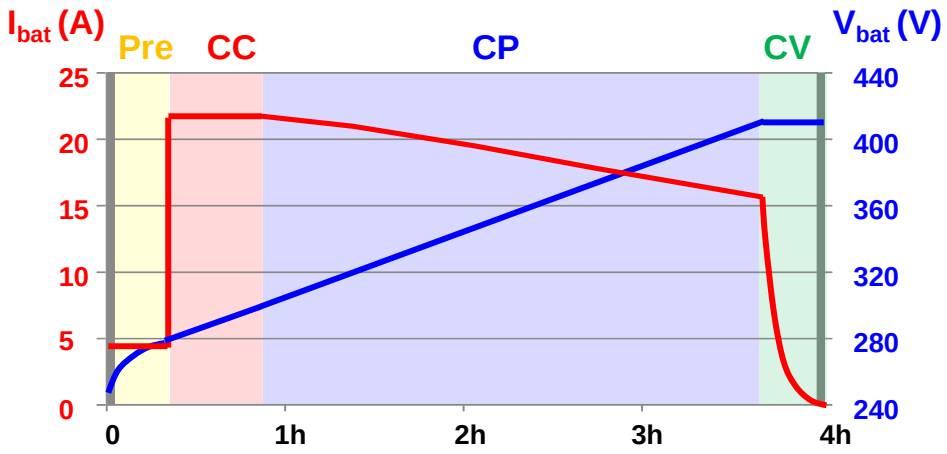
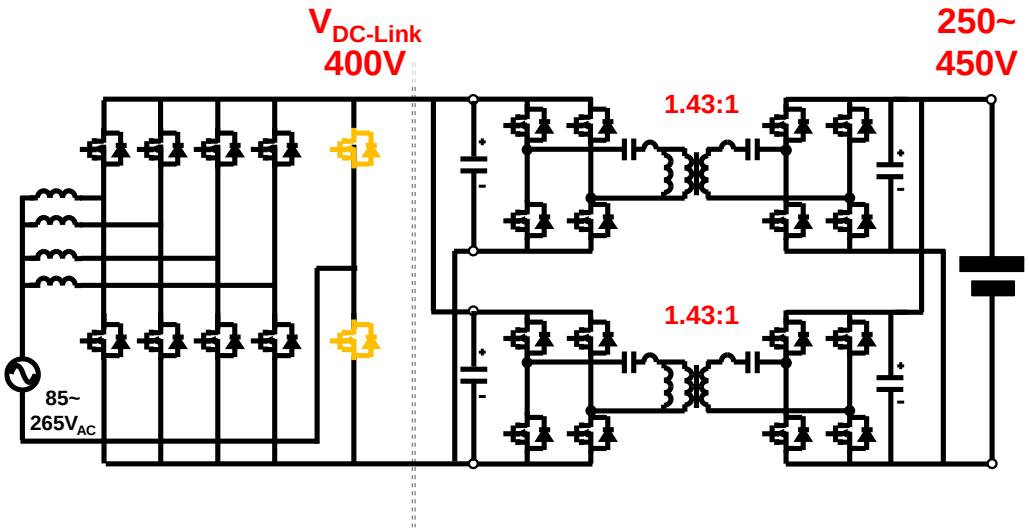


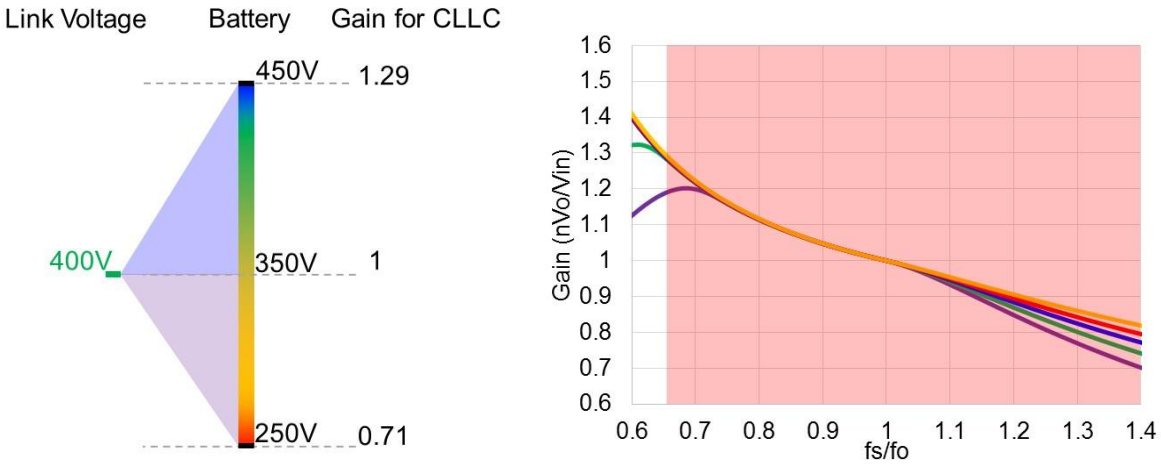
Fig. 4.18. Target battery charging profile

Specifically, the optimal operating point of a resonant converter is when the switching frequency (f_s) is equal to the resonant frequency (f_o). In the case of a wide output voltage range, the switching frequency of the resonant converter deviates dramatically from the resonant

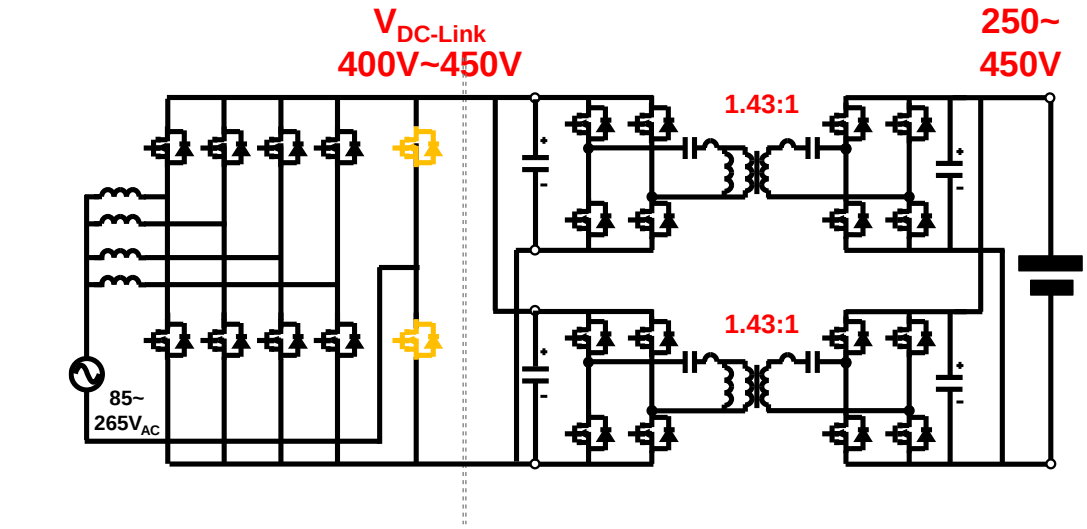
frequency in order to achieve the required wide voltage gain. Then the efficiency of the resonant converter suffers significantly. According to the curves shown in Fig. 4.19(a), the voltage gain is unity when the output voltage is 350 V and the switching frequency is equal to the resonant frequency. Then at the two boundaries when the output voltage is 250 V and 450 V, the gain is 0.71 and 1.29, while f_s is 140% and 65% of f_o, respectively.

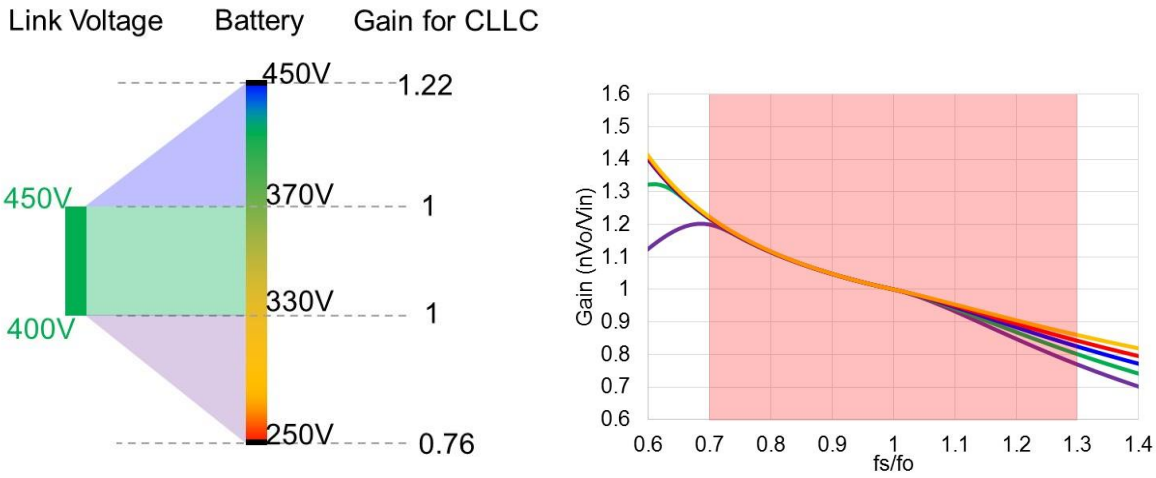
In order to alleviate this issue, we propose the structure of the variable DC-link voltage shown in Fig. 4.19(b), in which $V_{DC\text{-}link}$ is changed from 400 V fixed voltage to 400~450 V variable voltage. Comparing Fig. 4.19 (a) and (b), it can be seen that by changing the DC-link voltage, the gain range is reduced from 0.71-1.29 to 0.76-1.22, and there is a unity gain range in which the DC/DC stage does not need gain regulation. Since the gain range is reduced, the corresponding switching frequency range is also reduced to 70%-130% f_o. Therefore both the gain range and the frequency range become narrower; thus the efficiency is improved.



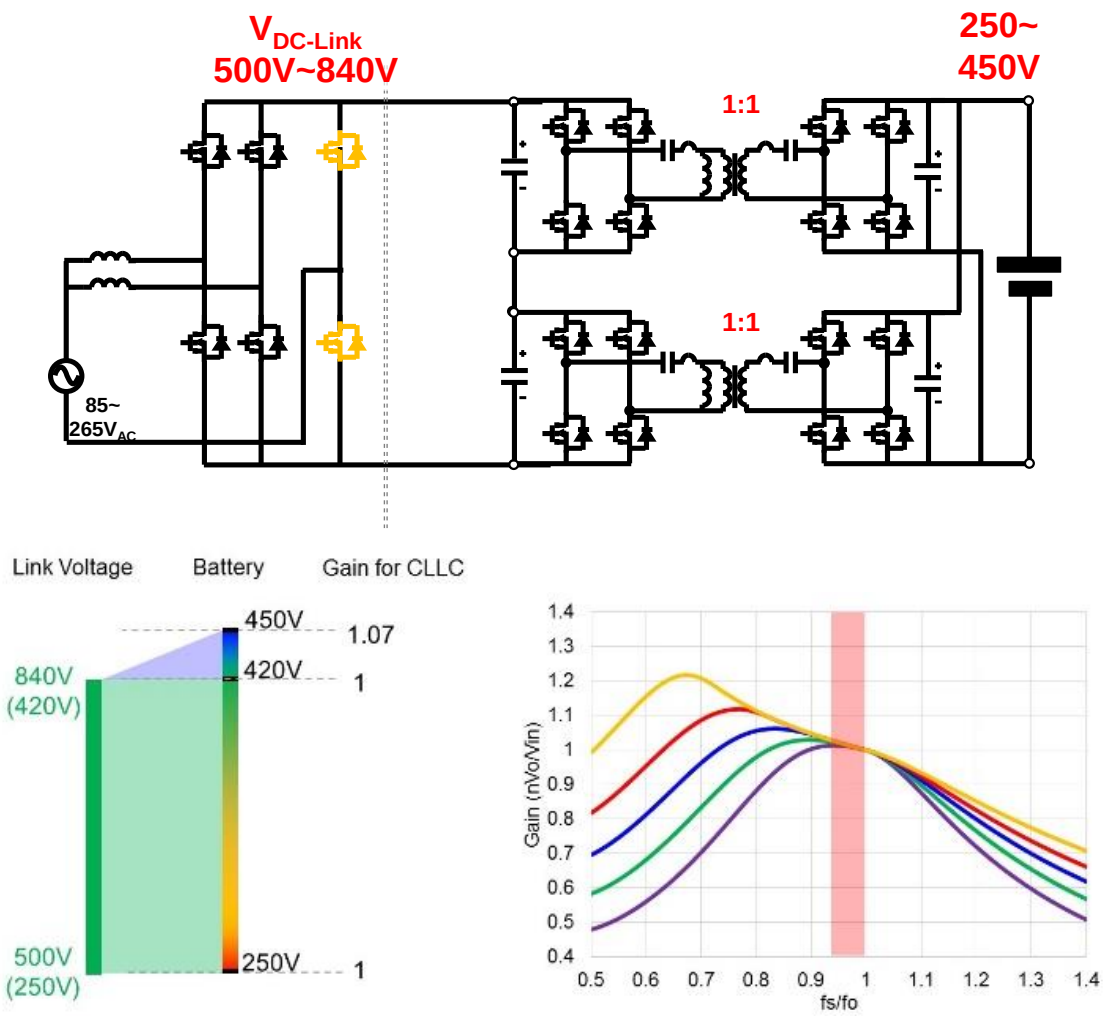

Link Voltage
Battery
Gain for CLLC
450V
1.29
400V
350V
1
250V
0.71
Gain (nVo/Vin)
fs/fo

(a)

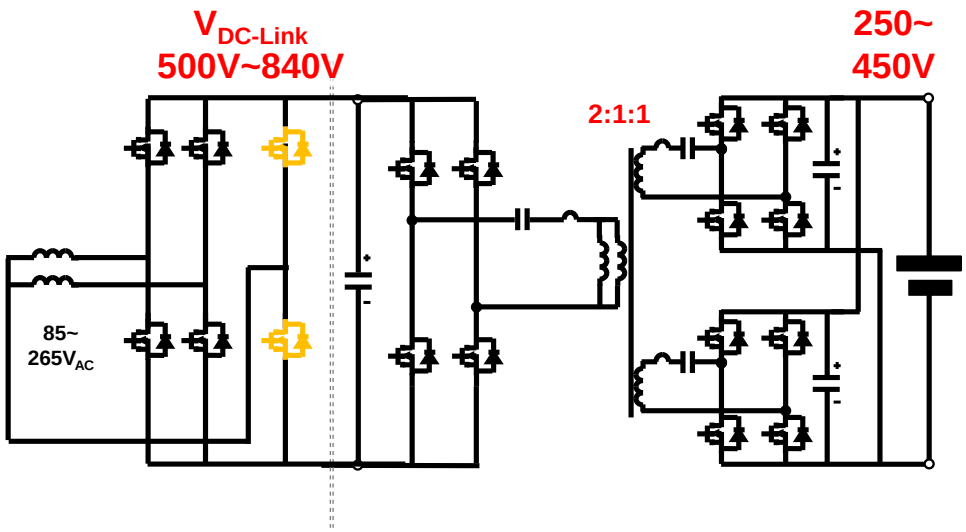

V DC-Link
400V~450V
250~
450V
1.43:1
1.43:1
85~
265V AC

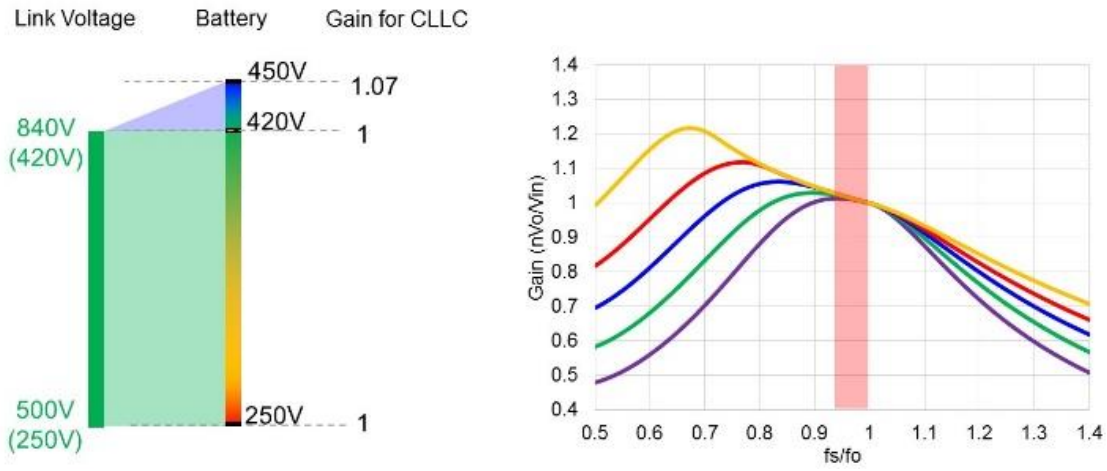

Link Voltage
Battery
Gain for CLLC
450V
1.22
450V
370V
1
400V
330V
1
250V
0.76
Gain (nVo/Vin)
fs/fo

(b)


V DC-Link
500V~840V
250~
450V
1:1
1:1
85~
265V AC
Link Voltage
Battery
Gain for CLLC
450V
1.07
840V
(420V)
420V
1
500V
(250V)
250V
1
Gain (nVo/Vin)
fs/fo

(c)


V DC-Link
500V~840V
250~
450V
2:1:1
85~
265V AC



(d)

Fig. 4.19. Four candidates for WBG-based OBC system architecture

With 600 V GaN devices, the DC-link voltage variation cannot be much wider. This is because the lower boundary is limited by the peak value of the AC input voltage, while the upper boundary is limited by the device voltage rating. Thus in order to further expand the DC-link voltage range, it is necessary to change 600 V GaN devices to 1.2 kV SiC MOSFETs in the AC-DC stage to allow wider DC-link voltage. It is possible to cause the DC-link voltage range to cover the entire battery voltage range with a 2-to-1 ratio. Furthermore, as 1.2 kV SiC MOSFETs can have a higher current rating, the AC/DC stage is simplified from a four-phase interleaving structure to a two-phase interleaving structure. The DC/DC stage still uses a module based on 600 V GaN devices, and their primary sides are connected in series so that only one-half the DC-link voltage is applied to each module. This is the major motivation of the third candidate shown in Fig. 4.19(c).

Benefiting from the wider DC-link voltage range, the frequency range of the DC/DC stage is significantly narrowed down to less than 10% variation. Thus efficiency is expected improve. However, the series-connected primary-side structure increases the conduction loss on both devices and transformers so that the overall efficiency is actually less than the second candidate.

To further improve the efficiency, a fourth candidate is proposed, as shown in Fig. 4.19(d). In this structure the primary-side switches of the DC/DC stage are changed from 600 V GaN devices to 1.2 kV SiC MOSFETs as well. As series connection is avoided, the conduction loss is dramatically decreased. This structure is the preferred one because the DC/DC stage operates like a semi-regulated converter which only deals with double line-frequency ripples, while the DC-link voltage is regulated by the AC/DC stage. Therefore the resonant converter operates close to the resonant frequency with optimal efficiency.

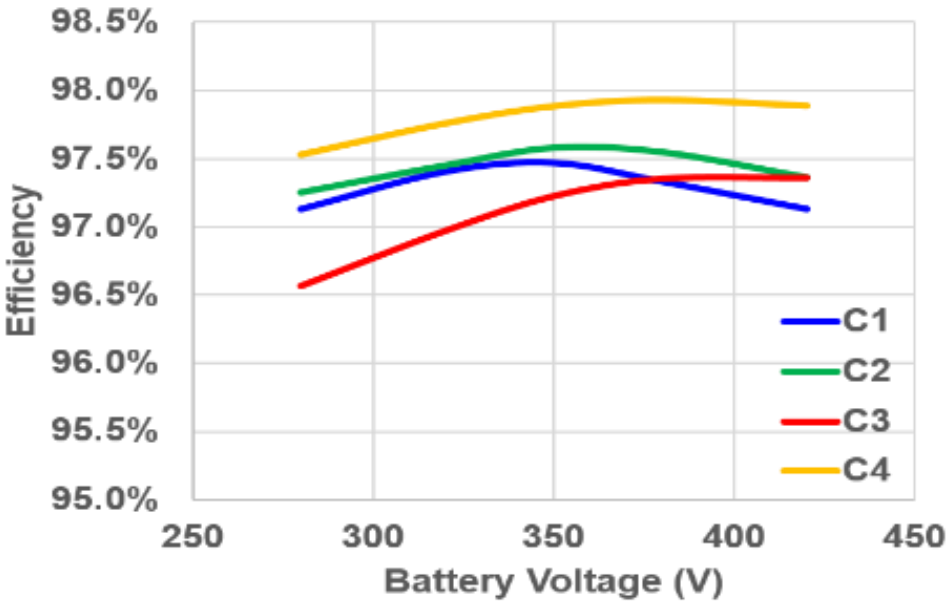


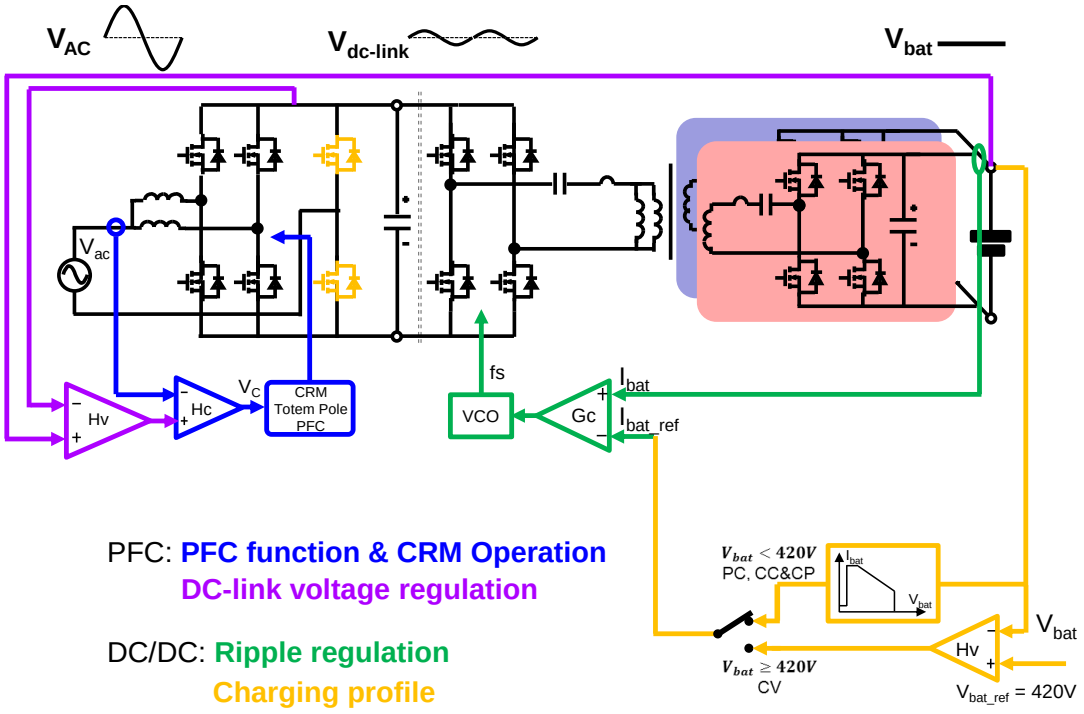
Fig. 4.20. Estimated efficiency of the DC/DC stage

The estimated efficiency versus charging voltage of the DC/DC stage of all four structure candidates are plotted on Fig. 4.20. The efficiency estimation is based on device switching loss measurement, the device analytical loss model, and finite-element-analysis (FEA) simulation of the transformer. The results further verify the previous analysis. Candidate 2 has higher efficiency than Candidate 1 due to its reduced gain range and frequency range. Candidate 3 has a monotonically increasing efficiency versus charging voltage. This is because the charging current

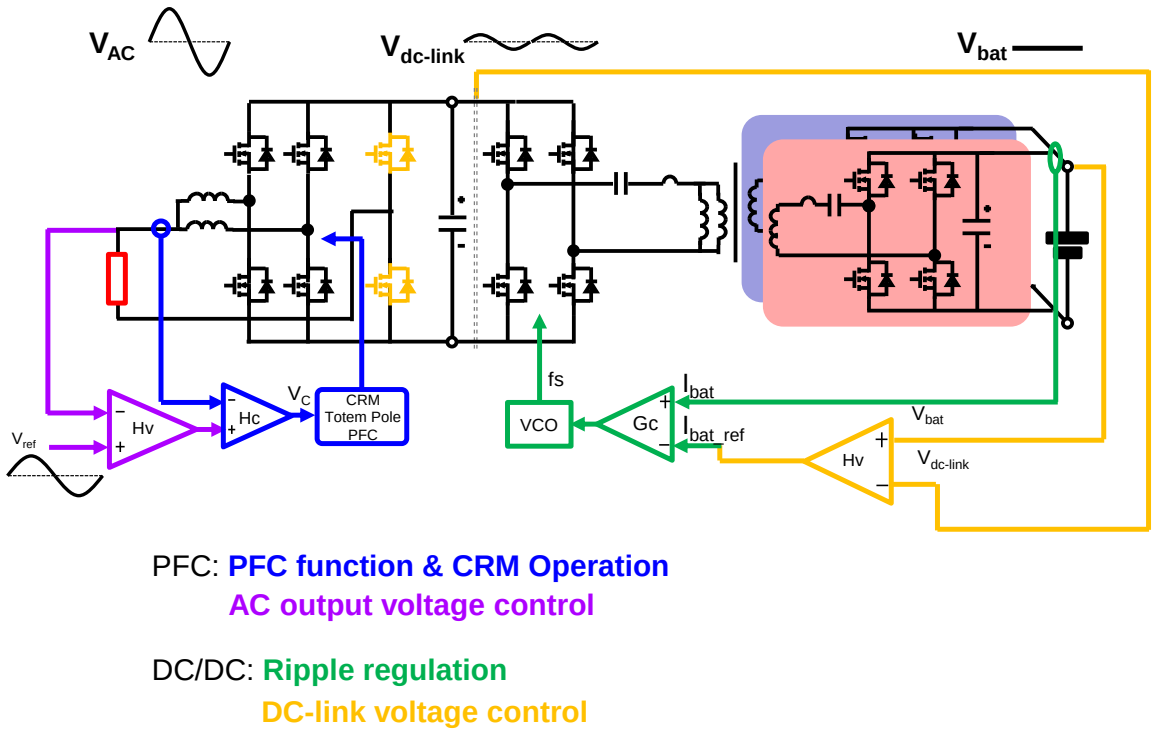
is larger at lower charging voltages, and the penalty of increased conduction loss due to series connection is more dominant. The issue is avoided in Candidate 4, and therefore it has significantly better efficiency than all the others.

Traditional control methods cannot easily be applied directly to the proposed system structure. Therefore the corresponding system control strategy is proposed. Fig. 4.21 (a) and (b) show the novel two-stage control strategy for the OBC system in charging mode and discharging mode, respectively.

In charging mode, the AC/DC stage performs power factor correction and DC-link voltage regulation according to the battery voltage, while the DC/DC stage operates as a semi-regulated converter which only regulates the double line-frequency ripple and makes sure the output voltage and current follow the desired charging profile. There is pre-charging, constant current charging, constant power charging, and constant voltage charging, depending on the battery voltage.



(a)



(b)

Fig. 4.21. Novel two-stage control strategy in (a) charging mode and (b) discharging mode

In discharging mode, the AC/DC stage still performs power factor correction, but it regulates the AC output voltage instead of the DC-link voltage in charging mode. At the same time, the DC/DC stage regulates the discharging current and the DC-link voltage. The major control blocks are identical for charging mode and discharging mode so that limited extra effort is required. The control of the entire OBC system is implemented by one microcontroller (TMS320F28075).

4.3 Hardware Demonstration

4.3.1 Evaluation of Suitable 1.2kV SiC MOSFET

Using a 1.2 kV SiC MOSFET is the key factor to designing a high-performance AC/DC stage and the primary side of the DC/DC stage. According to the conclusions in [D.16]-[D.18], soft-switching operation is desirable to achieve high efficiency with dramatically increased switching

frequency for GaN power devices. Furthermore, GaN-based MHz CRM PFC converters are demonstrated in [D.19]-[D.24] which achieve 99% efficiency. References [D.25], [D.26] have comprehensive characterization of 1.2 kV SiC power MOSFETs which show the turn-on loss is much larger than the turn-off loss. In the proposed OBC design, the DC/DC stage is a CLLC resonant converter that is able to achieve zero-voltage-switching turn-on (ZVS) and low-current hard-switching turn-off on the primary-side control switches. The AC/DC stage is a totem-pole PFC converter. When operating in critical conduction mode (CRM), the AC/DC stage is able to realize ZVS or the valley-point turn-on of the control switch and zero-current-switching (ZCS) turn-off of the synchronous rectifier. With soft-switching operation, switching-related losses are minimized. Therefore the conduction loss becomes the dominant factor in the total loss.

Table 4.1. 1.2 kV SiC Power MOSFET/JFET candidates (all data are from manufacturers' datasheet)

Manufacturer	GE	GE	Wolfspeed	Global Power Technologies	Microsemi	ROHM	USCi (SiC JFET in Cascode)
Device	GE12N025RF-3	GE12N65L-3	C2M0025120	GP1T025A120B	APT80SM120B	SCH2080KE	UJC1206K
$R_{DS(on)}$	25 mΩ (25˚C) 42 mΩ (175˚C)	25 mΩ (25˚C) 42 mΩ (200˚C)	25 mΩ (25˚C) 43 mΩ (150˚C)	25 mΩ (25˚C) 43 mΩ (150˚C)	40 mΩ (25˚C)	80 mΩ (25˚C) 125 mΩ (125˚C)	42 mΩ (25˚C) 105 mΩ (150˚C)
$R_{G(int)}$	1 Ω	1 Ω	1.1 Ω	10 Ω	-	6.3 Ω	1.2 Ω
Package	DE-150	TO-247	TO-247	TO-247	TO-247 / D^3PAK	TO-247	TO-247

In order to reduce the conduction loss, a 1.2 kV SiC MOSFET with a small on-resistance is preferred. Table 4.1 lists available 1.2 kV SiC MOSFET/JFET candidates with discrete packaging and the smallest on-resistance from different manufacturers. At the time this research was conducted, 25 mΩ at room temperature is the lowest available on-resistance of a 1.2 kV SiC

MOSFET/JFET. Therefore the devices from Microsemi, ROHM and USCi are not considered in this study.

The internal gate resistor ($R_{G(int)}$) is another important parameter, since switching loss is highly related to it. The device from Global Power Technologies Group has 10 Ω $R_{G(int)}$ which is about ten times the resistance of the devices from GE and Wolfspeed; thus it is also ruled out.

After the above considerations, only the devices from GE and Wolfspeed are left for detailed comparison. A double-pulse tester (DPT) is built to evaluate the switching performance. The device under test (DUT) is put on the low side, with the source terminal referenced to the ground. The free-wheeling device is the same device as the DUT to emulate the same half-bridge configuration in a real converter. The choke inductor is made with less than 10 pF EPC to reduce its impact on the DUT. The high-speed gate driver IXDN614SI is used to drive the DUT directly with 20 V on-state gate driving voltage and -5 V off-state gate driving voltage. There is no external gate resistor added in order to switch the DUT as fast as possible so that the turn-off loss is minimized. The PCB layout has both a minimized power loop and driving loop. A 2 GHz high-bandwidth current shunt resistor (SSDN-10) is used to measure the drain-source current waveform in the DUT, and it is connected to the scope with a 50 Ω terminated BNC cable. The drain-source voltage waveform is measured with passive high-voltage probe TPP0850. The gate-source voltage waveform is measured with passive probe TPP1000.

As the OBC operates under ZVS, there is no turn-on related loss. The turn-off waveforms and losses at different voltages and currents are measured and calculated, and Fig. 4.22 shows the tested waveforms of the turn-off transition at 800 V and 30 A. The waveforms of the GE and Wolfspeed devices in the TO-247 package overlap. As there is no external gate resistor, the switching transition is very fast with minimized turn-off loss. The curve of E_{OFF} is calculated as

the integral of the product of the drain-source voltage and current. The waveform comparison indicates that the switching transitions of the two devices are similar, though the GE device has lower turn-off energy. However, quite significant parasitic ringing is observed with both devices, especially in the gate-source voltage waveforms. The package-related parasitic inductances are the major reason for the ringing, since the TO-247 package has relatively long leads but no Kelvin source connection. Therefore the source terminal is shared by the power loop and the driving loop, which becomes a common-source inductor. Furthermore, the di/dt value during turn-off transition is large as there is no external gate resistor for turn-off loss reduction. Finally, large parasitic ringing in the gate-source voltage waveform is induced due to the combined effect of the two factors.

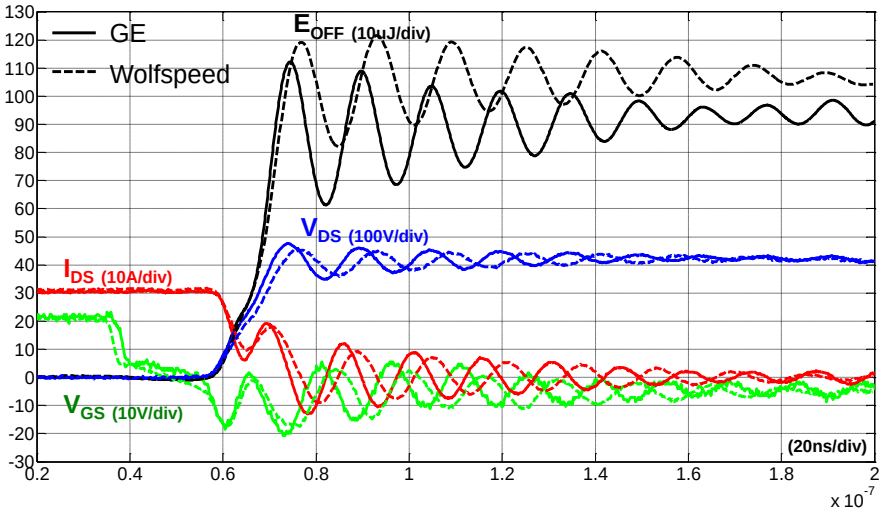
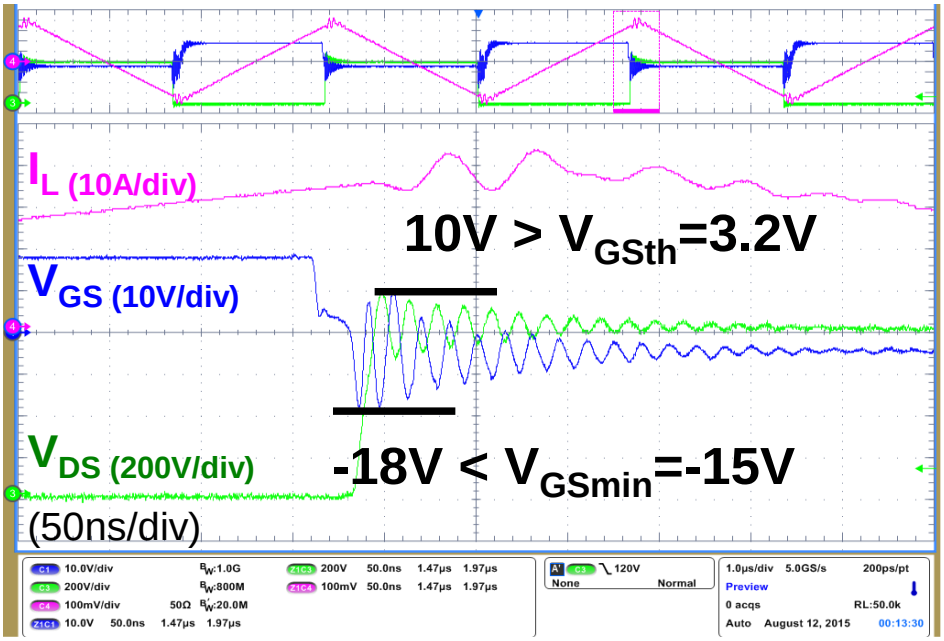


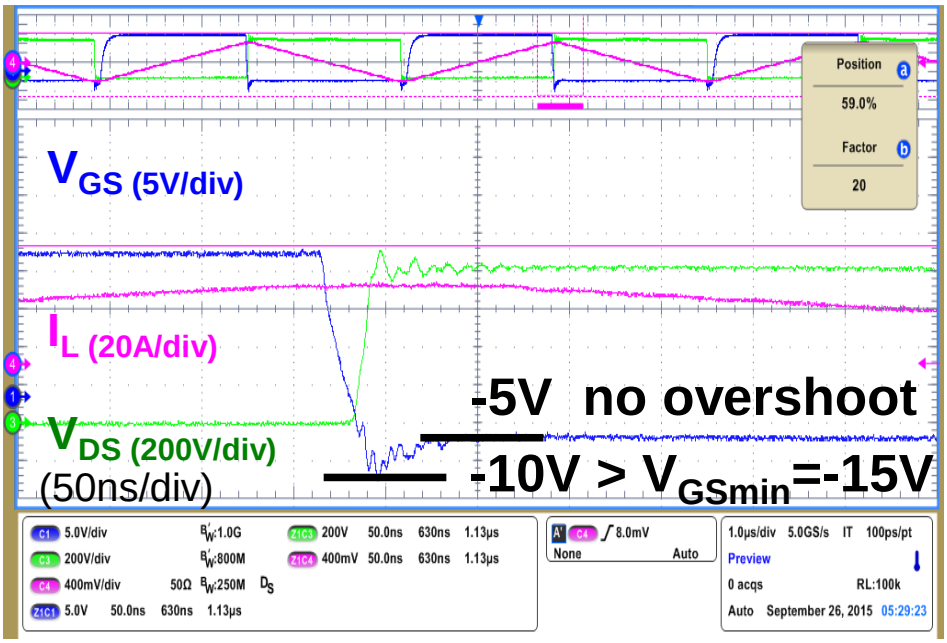
Fig. 4.22. Turn-off waveform with 800 V voltage and 30 A current

Due to the large parasitic ringing on the gate, two concerns are raised. The first concern is that the positive voltage in the ringing is higher than the threshold voltage, which may lead to false turn-on and shoot-through. The second concern is the negative voltage in the ringing is lower than the datasheet claimed minimum negative voltage value, so there could be gate breakdown risk.

Essentially the parasitic ringing shows the limitations of the TO-247 package when the device is operated at a switching frequency of hundreds of kHz.



(a)



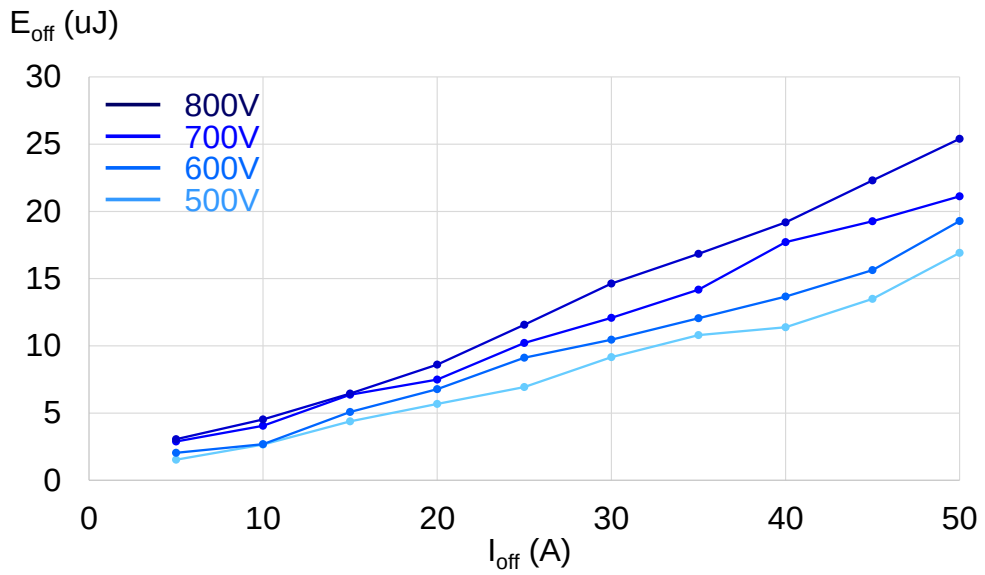
(b)

Fig. 4.23. Tested waveforms with 800 V/40 A/300 kHz/0 Ω R_G with (a) TO-247 package and (b) DE-150 package

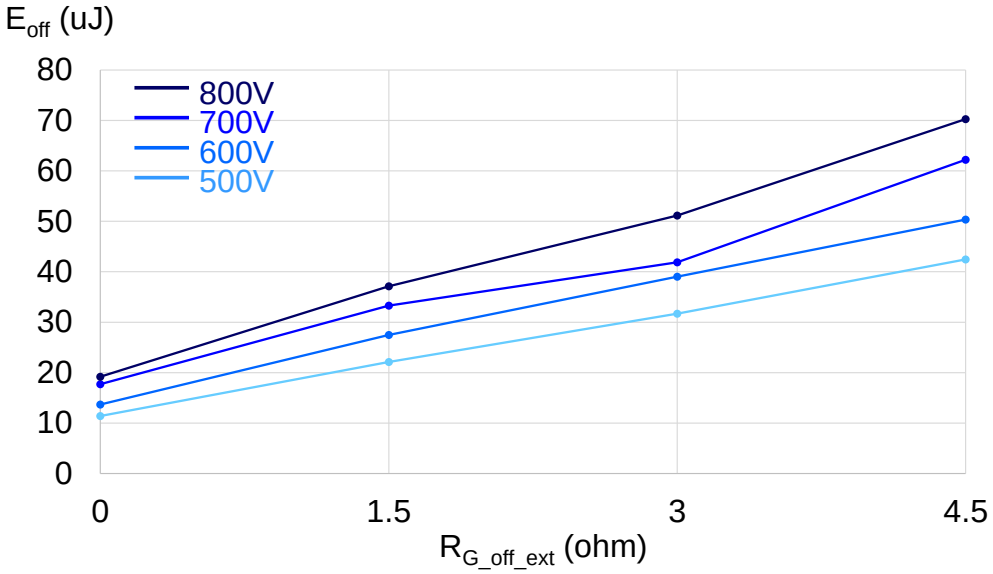
Better package is essential to enable high frequency operation of SiC devices. Another GE device with improved package, as known as DE-150, is then tested. This package is a RF power package with decoupled power and driving loops, reduced parasitic inductors, and a symmetric electric-magnetic field [D.27]. Therefore the parasitic ringing is dramatically reduced compared to the TO-247 package. Fig. 4.23 provides a comparison between the two packages under the same 800 V, 40 A, 300 kHz, and 0 Ω turn-off gate resistor operating conditions. The test circuit setups are almost identical, with the package as the only difference. The test waveforms of the DE-150 package shows that the parasitic ringing on the gate is significantly reduced with no false trigger risk nor gate breakdown risk. At the same time, there is about a 50% voltage spike reduction on the drain-source voltage. The frequency of the parasitic ringing of the DE-150 package is greatly increased, which also demonstrates the reduced critical power loop parasitic inductance.

After the comparison, the GE SiC MOSFET in the DE-150 package is chosen due to its small turn-off loss, small on-resistance at high temperatures, and more suitable package for high-frequency operation.

Since the proposed design has a DC-link voltage that varies from 500 V to 840 V, the device turn-off loss at different voltages and currents is tested and shown in Fig. 4.24(a). It is necessary to clarify that the energy stored in the output junction capacitor, often referred as E_{OSS}, is measured as a part of E_{OFF}, but it is actually dumped in the channel of the device during the turn-on transition. With ZVS, the E_{OSS} is recycled instead of lost. Hence the E_{OSS} is compensated from the measured E_{OFF} to reflect the real turn-off loss. Otherwise the E_{OFF} would be overestimated.



(a)



(b)

Fig. 4.24. Tested turn-off losses of the GE SiC MOSFET with (a) 0 ohm gate resistors at different voltages and currents; and with (b) different gate resistors at 40 A and different voltages

The gate resistor is another important factor that impacts the turn-off loss; therefore the turn-off losses with different gate resistors are also measured, as shown in Fig. 4.24(b). The figure clearly shows that a smaller gate resistor leads to a smaller turn-off loss.

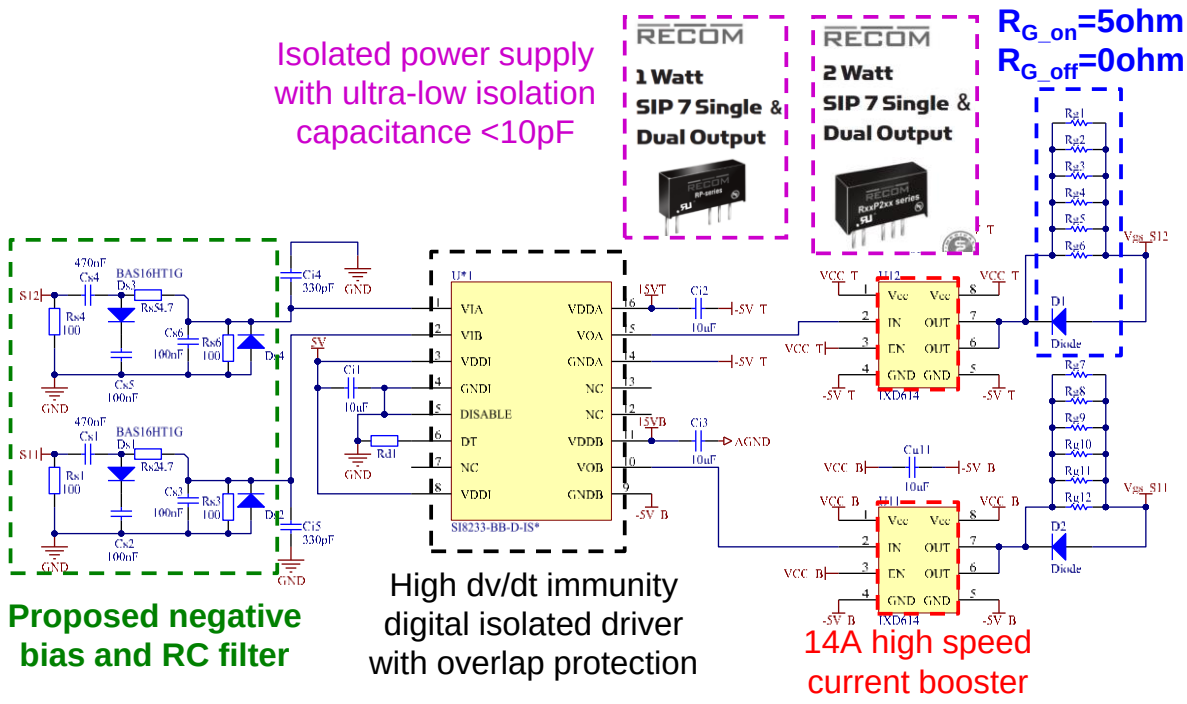


Fig. 4.25. Schematic of gate driver

The gate driver design is also a challenge to be tackled. With reference to work presented [D.28], the schematic of the gate driver design in this work is shown as Fig. 4.25. The PWM signals first go through bias and filter circuits to avoid interference from the power stage. A high-dv/dt immunity digital isolator (Si8233) is used to achieve isolated signal transfer. A high-speed current boost then drives the SiC MOSFET directly with 5 Ω turn-on gate resistor and 0 Ω turn-off gate resistor. Isolated power supplies with low parasitic capacitance provide positive and negative driving voltage separately.

Fig. 4.26 provides a comparison of switching losses between GE's 1.2 kV SiC MOSFET and a 600 V GaN HEMT sample tested with a similar DPT setup. The turn-on loss is significantly larger than the turn-off loss for both the tested SiC MOSFET and the GaN HEMT, which further justifies that ZVS is essential to both the SiC MOSFET and GaN HEMT to achieve high efficiency when operating at very high switching frequencies.

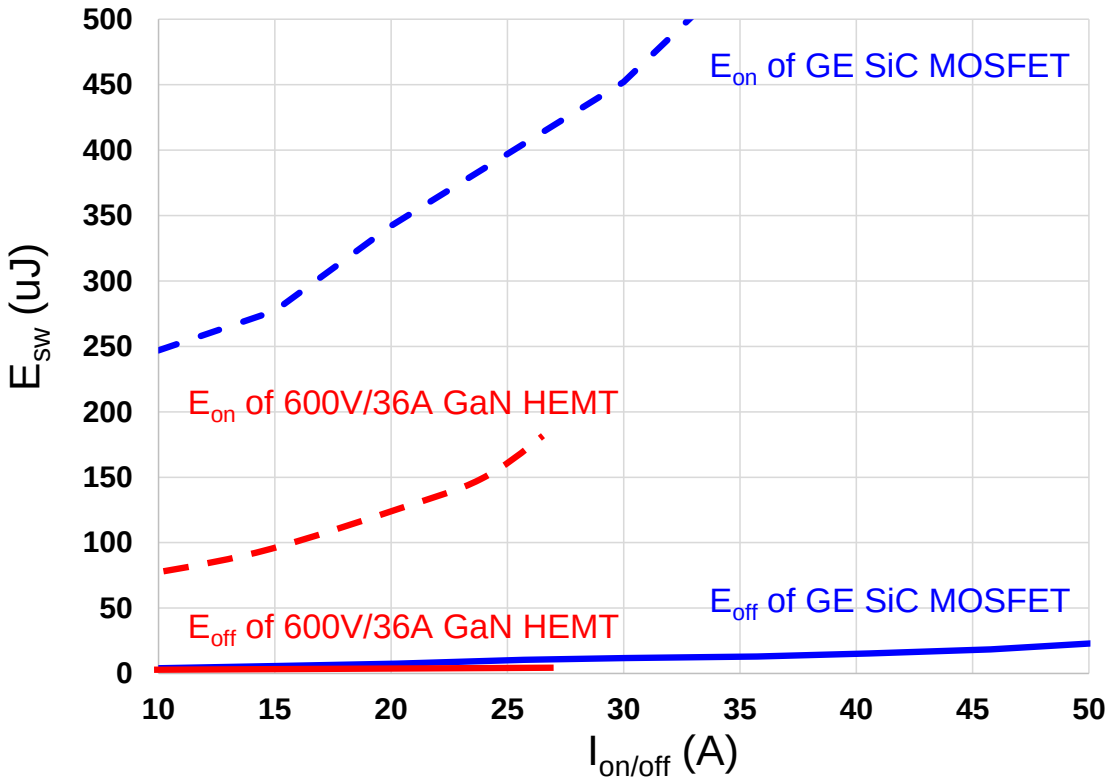


Fig. 4.26. Measured switching loss of GE's 1.2kV SiC MOSFET at 600V and a GaN HEMT sample at 400V

4.3.2 Prototype and Experimental Results

A prototype is built, as in Fig. 4.27. The AC/DC stage is on the top while the DC/DC stage is on the bottom. There are large spaces reserved for the EMI filters on both the AC side and DC side in accordance with the preliminary design. The power density of the total system is 37 W/in^3.

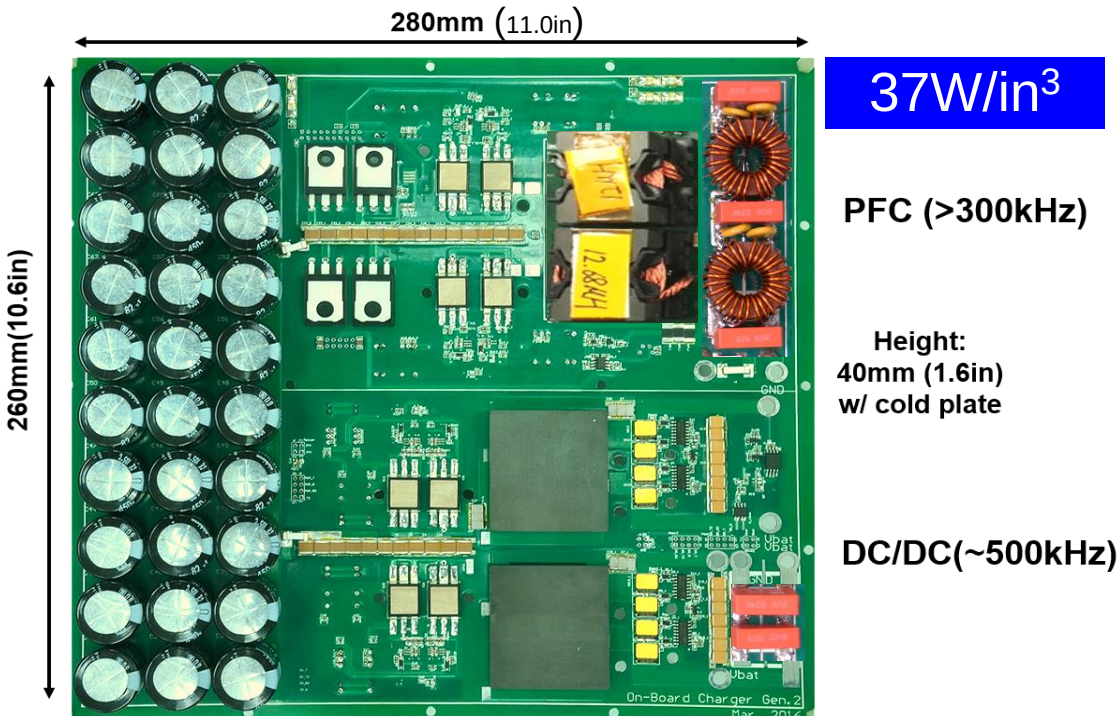
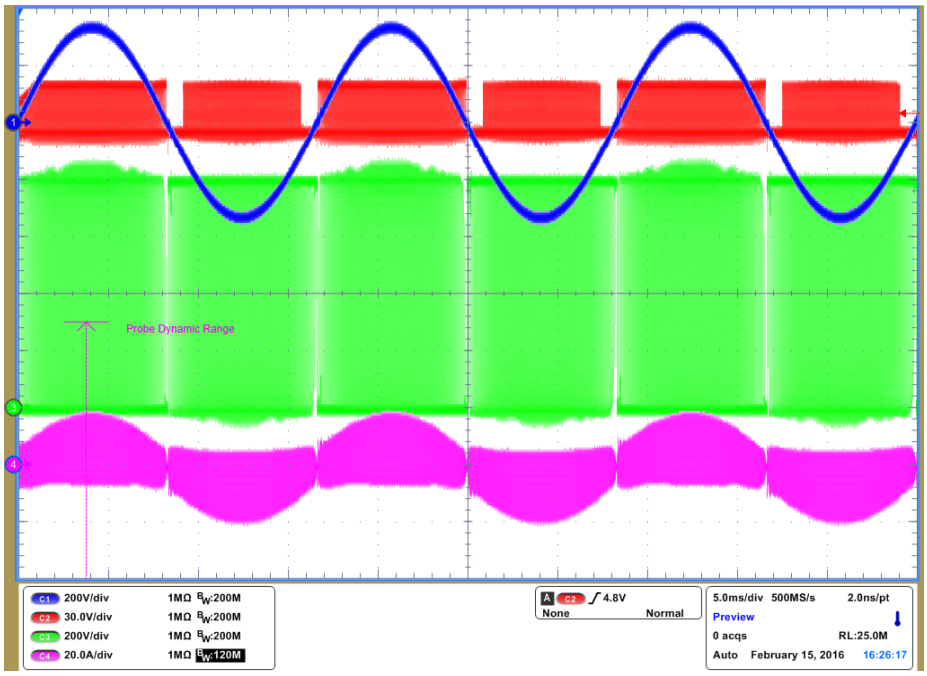


Fig. 4.27. Prototype of the 6.6 kW on-board charger

Fig. 4.28. shows the experimental waveform of the AC/DC stage with 800V DC-link voltage. The magnified waveforms show that ZVS is achieved through the entire line cycle.



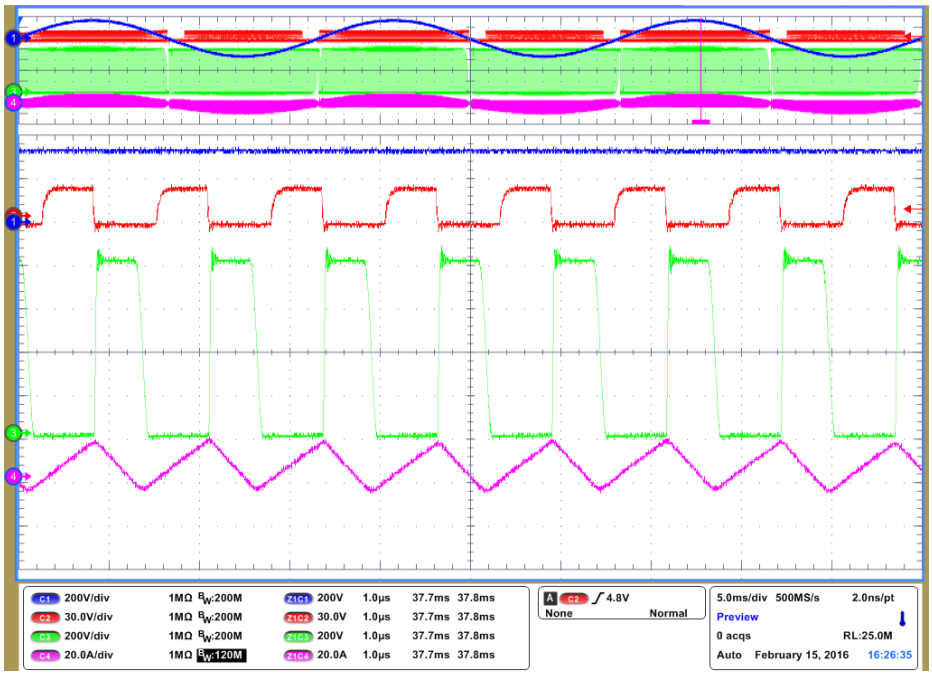


Fig. 4.28. Experimental waveform of the AC/DC stage at 800V/6.6kW in charging mode (CH1 is input AC voltage; CH2 is the VGS of the bottom switch of Phase 1; CH3 is the VDS of the bottom switch of Phase 1; CH4 is the inductor current of Phase 1)

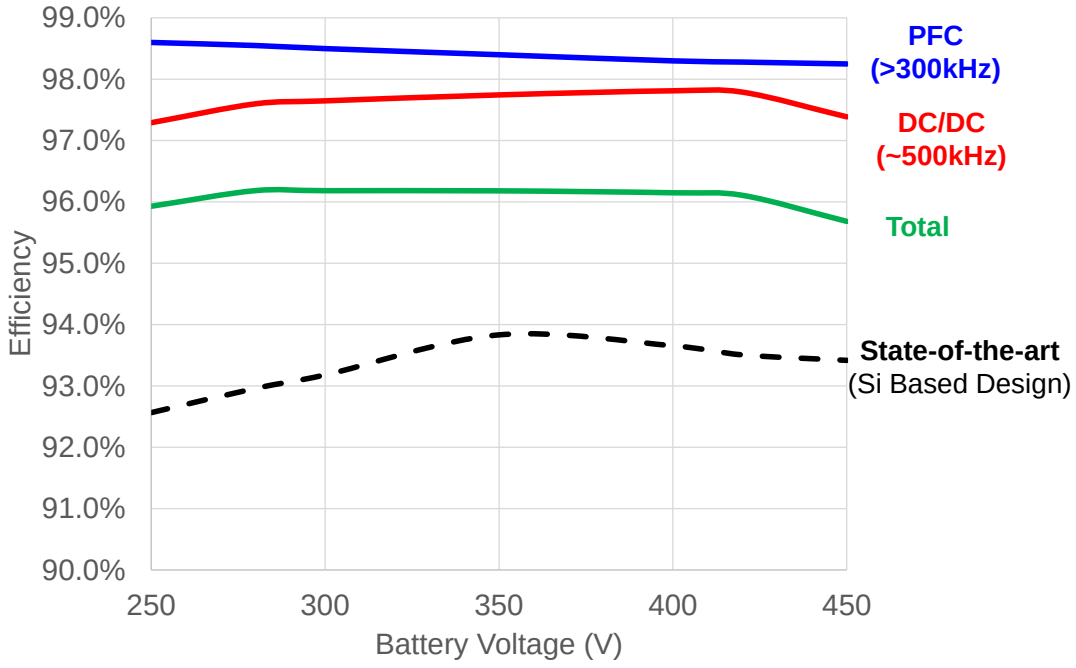


Fig. 4.29. Tested efficiency of AC/DC stage, DC/DC stage, and total system in charging mode in comparison with the state-of-the-art industry product

Fig. 4.29 is the tested charging mode efficiency of the AC/DC stage, the DC/DC stage, and the total system versus the battery voltage. Around 98.5% efficiency and above 96% efficiency are achieved by the AC/DC stage and the total system, respectively.

Comparing the efficiency to the state-of-the-art GaN-based design, the proposed approach has more than 2% higher at peak and more 3-4% higher across the total battery voltage range. The green curve is much flat which means that in the entire charging cycle the proposed design is most efficient. It can be calculated that there is 50% loss reduction per charging cycle thanks to the flat efficiency curve.

According to the developed loss model and the results of FEA simulations for magnetic components, the detailed loss analysis are shown in figure below. The power consumption of MUC is less than 1 W which is considered negligible so it is not included.

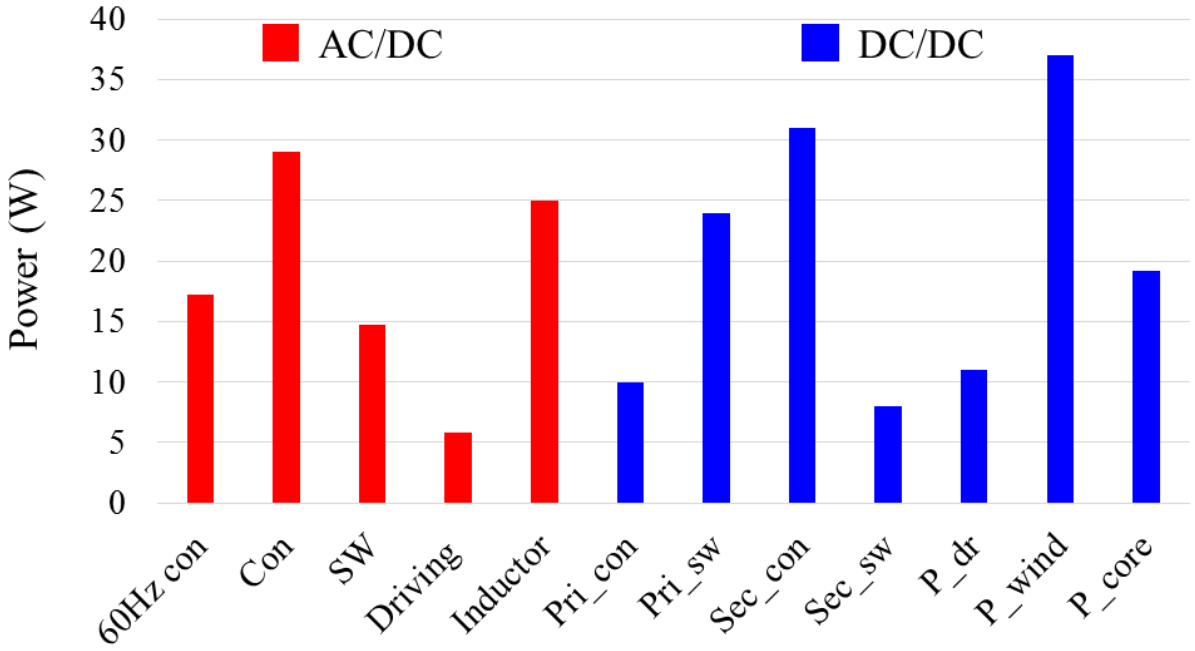


Fig. 4.30. Loss breakdown at 350V battery voltage and 6.6kW power in charging mode

In this loss breakdown, the red bar for AC/DC stage and the blue bar for DC/DC stage; "60Hz con" is the conduction loss of 1.2kV SiC switching at line frequency; "Con" is the conduction loss of 1.2kV SiC switching at high frequency; "SW" is device switching loss; "Driving" is device driving loss; "Inductor" is total inductor loss; "Pri_con" is primary-side device conduction loss; "Pri_sw" is primary-side device switching loss; "Sec_con" is secondary-side device conduction loss; "Sec_sw" is secondary-side device switching loss; "P_dr" is device driving loss; "P_wind" is transformer winding loss; and "P_core" is transformer core loss.

As an off-line power supply, there is specific requirement on the AC input power quality. The tested total harmonic distortion (THD) is shown in figure below which shows that from heavy load to light load the THD is below 5% limit.

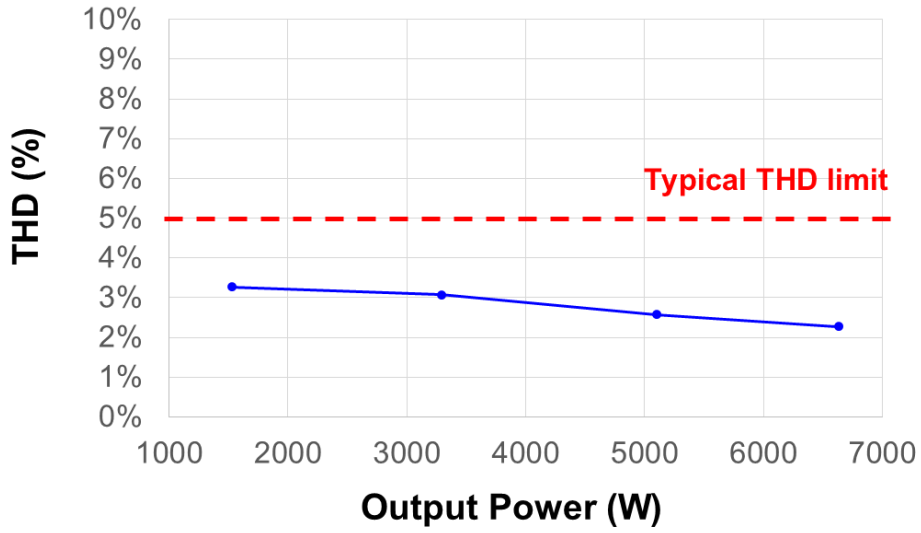


Fig. 4.31. Tested THD of AC/DC stage in charging mode

The next figure is the tested efficiency in discharging mode. The solid lines show efficiency at 250 V battery voltage. At this voltage, the on-board charger is operating at constant current charging so that the maximum output power is around 5 kW. The dash lines are efficiency at 400 V battery voltage.

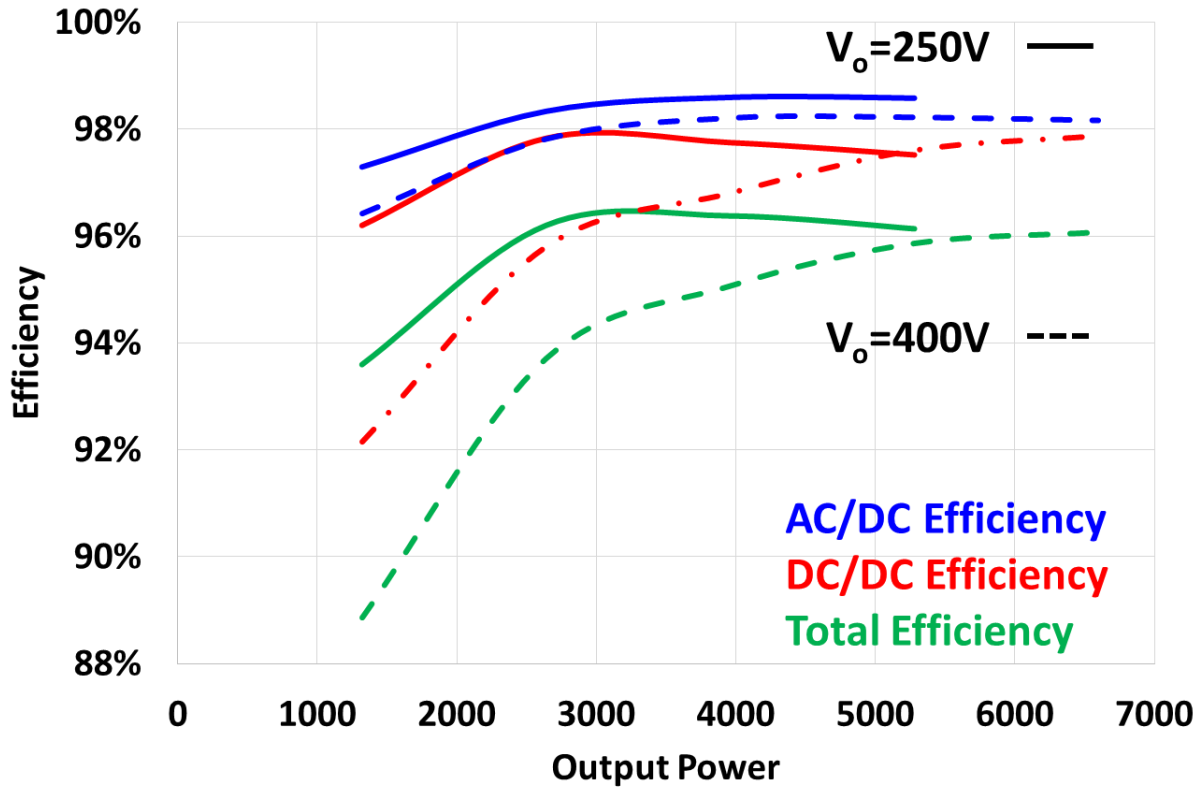


Fig. 4.32. Tested efficiency of AC/DC stage, DC/DC stage, and total system in discharging mode at 250V (solid line) and 400V (dash line) battery voltage.

EMI Noise and Filter Design

The differential mode (DM) noise and common mode (CM) noise for the total system is measured at full power and different input and output voltages. The worst case in terms of both CM noise and DM noise are both at 240Vac input and 300Vdc output (600Vdc link voltage) since both CM noise and DM noise are dominant by the AC/DC stage and the switching frequency at the peak point of half-line cycle is minimum at 240Vac to 600Vdc condition. The figures below are measured EMI noise and the red indicate the design guideline for the filter. Two stage EMI filter is assumed and the desired corner frequency for DM filter and CM filter are 140 kHz and 160 kHz respectively.

This result and conclusion is true for the AC/DC stage with non-coupled inductor but yet to be investigated for the AC/DC stage with coupled inductor and balance. It is expected that the balance can reduce the CM noise.

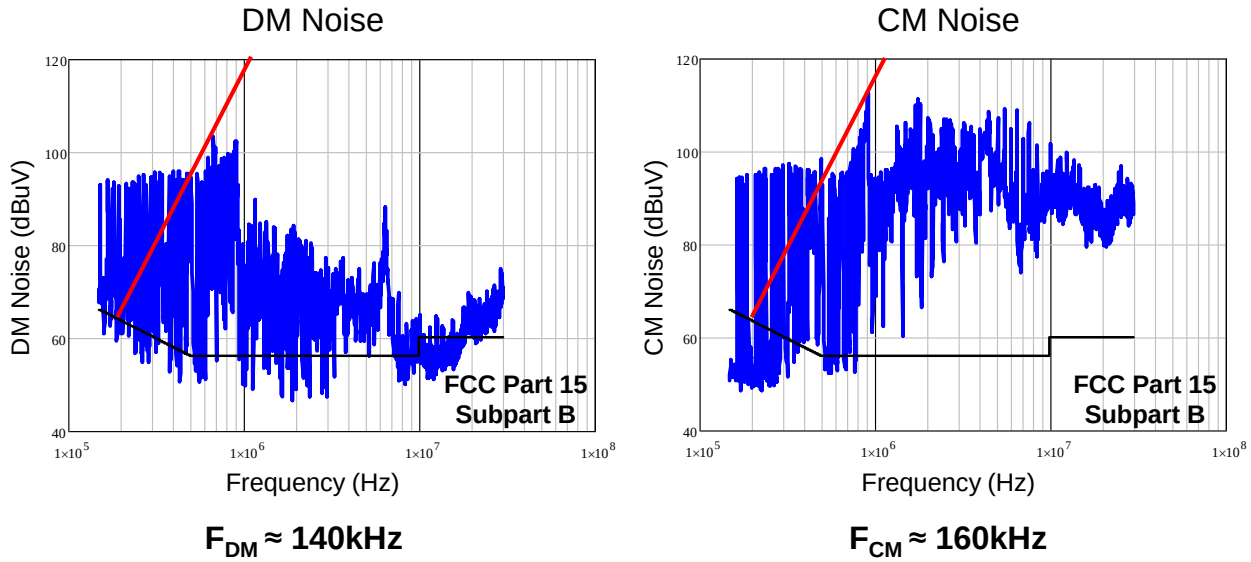
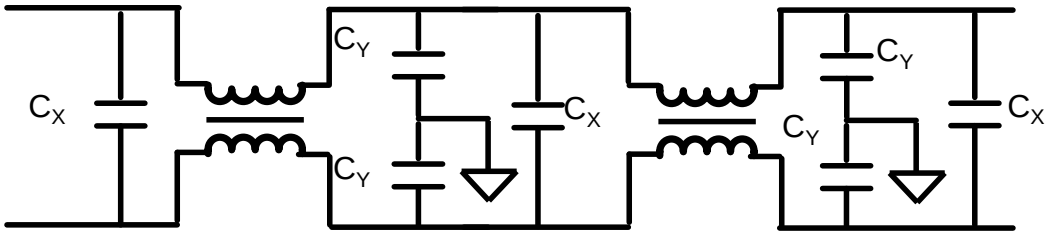


Fig. 4.33. Measured DM noise and CM noise at 240Vac, 300Vdc (600Vdc link), and 6.6kW

The design of EMI filter is demonstrated in the figure below. Based on the regulation of ground leakage current the Y-cap is selected first. Then the inductance of CM choke is determined according to the desired CM filter corner frequency. Then the leakage of CM choke is used as the inductance for DM filter inductor which is 4 uH. Finally the X-cap is calculated according to the desired DM filter corner frequency.

The testing results after EMI filter applied is shown in Fig. 4.35. With the proposed EMI filter design, the on board charger meets the regulation in FCC Part 15 Subpart B.



C_Y = 2.2nF ⟶ Lcm = 200uH ⟶ Ldm = 4uH ⟶ Cx= 824nF

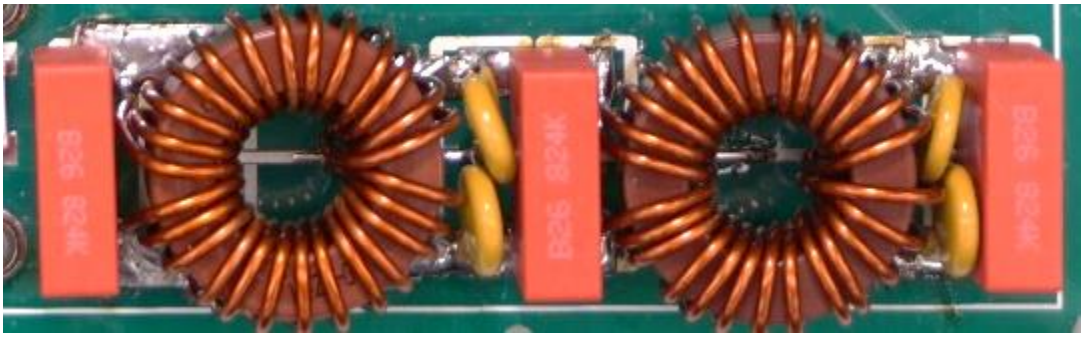


Fig. 4.34. Measured DM noise and CM noise at 240Vac, 300Vdc (600Vdc link), and 6.6kW

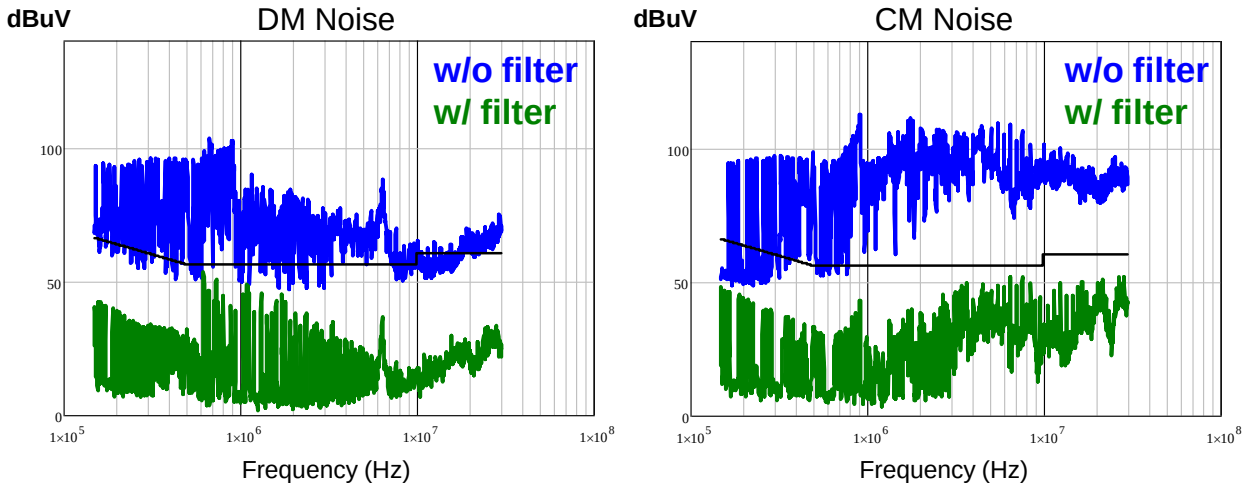


Fig. 4.35. Test results of EMI filter

Chapter 5. Extension to Three-Phase Rectifier/Inverter

Three-phase AC/DC converters are widely used in grid-tie applications, such as PV inverter systems, EV charging stations and data centers. Take the DC/AC stage in a PV inverter system as an example. In commercial products, the efficiency is usually as high as 97% ~ 99%. However, the power density is usually below 10 ~ 15 W/in^3 [E.1]-[E.5]. The power density is limited by Si devices which make the converter operate at tens of kHz (usually about 20 ~ 30 kHz).

With the emergence of wide-bandgap (WBG) semiconductor devices, the switching frequency is able to be pushed to higher level. This is because for the same voltage level and similar current level, the figure-of-merit (FOM) of WBG semi-conductor devices is better than that of Si devices, so the de-vice related loss of WBG semiconductor devices is smaller than that of Si devices. By pushing to higher switching frequency, the size of inductors and EMI filters can be reduced, which improves the power density, while at the same time, high efficiency, similar to the commercial products, is still able to be achieved.

For WBG semiconductor devices, the turn-off loss is usually extremely small compared with the turn-on loss. Also for WBG semiconductor devices, the turn-off loss does not have significant increase as turn-off current becomes larger, while the turn-on loss shows significant increase as turn-on current increases [E.6]-[E.10]. These special characteristics of WBG semiconductor devices make critical conduction mode (CRM) become the preferred operation mode, because in CRM operation, zero-voltage-switching (ZVS) soft-switching turn-on of the control switch is achieved, which helps to eliminate high turn-on loss, while has almost no penalty on the increase of turn-off loss and conduction loss, although there is an increase of current ripple and thus of RMS current value.

With CRM operation and ZVS soft-switching turn-on, the switching loss of the devices becomes small even operating at hundreds of kHz switching frequency. Therefore, ZVS soft-switching turn-on is the key factor to maintain high efficiency even operating at high frequency, and CRM operation is the simplest way to achieve soft switching without adding physical complexity to the converter. Then, the question is how to achieve CRM operation and ZVS soft-switching turn-on in three-phase AC/DC converter.

5.1 Prior Art of Three-Phase Rectifier/Inverter in CRM

Two CRM-based ZVS soft-switching methods are found in literature. One is based on three-phase H-bridge converter [E.10], the other is based on three-level T-type converter [E.11]. In both of these two methods, there are split capacitors at DC side, and the middle point of the split capacitors is connected to grid side neutral point. With the connection between DC side middle point and grid side neutral point, three phases are electrically decoupled and each phase can be regarded as an independent single-phase converter running at CRM operation. These two methods work well at tens of kHz switching frequency operation. While applied into the hundreds of kHz high frequency design, these two methods show very wide switching frequency variation which has significant disadvantage on switching related loss.

Prior Art 1: CRM Three-Phase Rectifier/Inverter with Split Caps

A three-phase rectifier/inverter operating in critical mode is proposed in [E.10]. In this paper, the targeted application is micro-inverters for grid-tied PV panels. The topology, typical waveforms, and equivalent circuit during on time and off time are shown in the figures below.

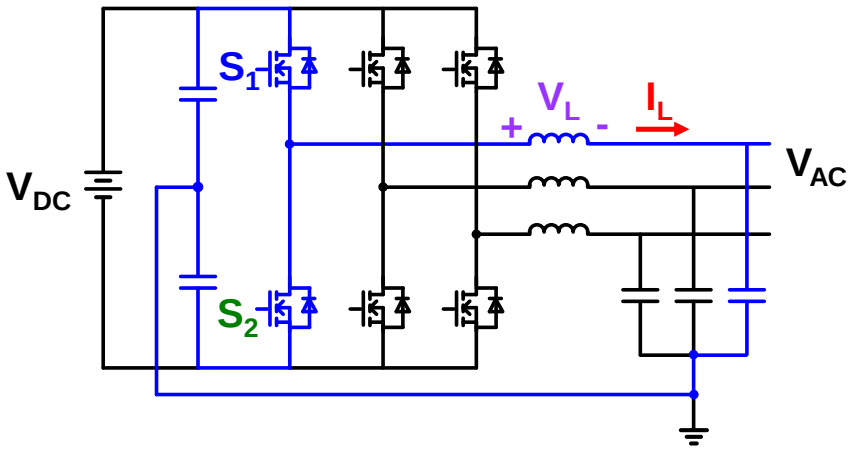


Fig. 5.1. Topology of CRM three-phase rectifier/inverter with split caps

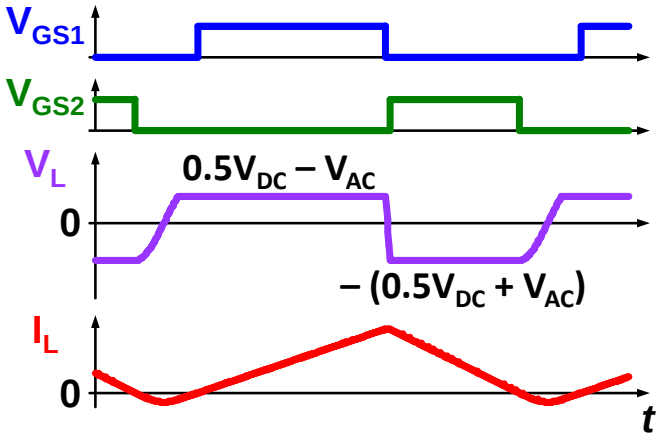


Fig. 5.2. Typical switching cycle waveforms

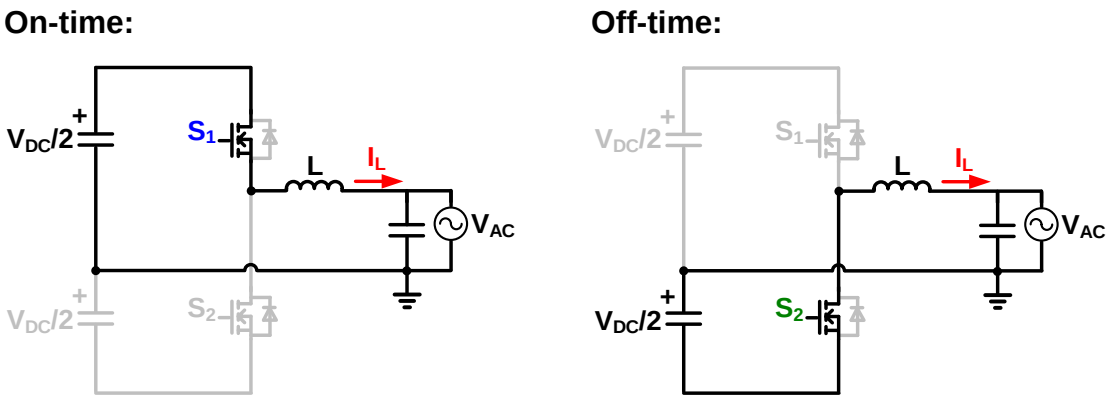


Fig. 5.3. Equivalent circuits during on time and off time (in positive line cycle)

There are two features which make the frequency variation very wide when operating at critical mode. The one thing is the circuit has split cap and the equivalent DC-link voltage is divided by two. Then at 277Vac to 800Vdc specification, one-half Vdc is much more close to AC voltage around peak point. The other thing is determined by the operation of this circuit, when the AC voltage is close to zero around the zero crossing of line cycle, both the inductor current charging and discharging is determined by one-half Vdc. Considering the very small current value and maintaining in critical mode, the frequency became significantly higher compared to the middle point of a half line cycle which has the minimum frequency.

The figures below show the simulated waveforms and switching frequency distribution in a half line cycle. As designed at 300 kHz at the middle point of a half line cycle, the frequency around AC voltage zero crossing is higher than 10 MHz which of course is a dramatic variation that cannot be accepted.

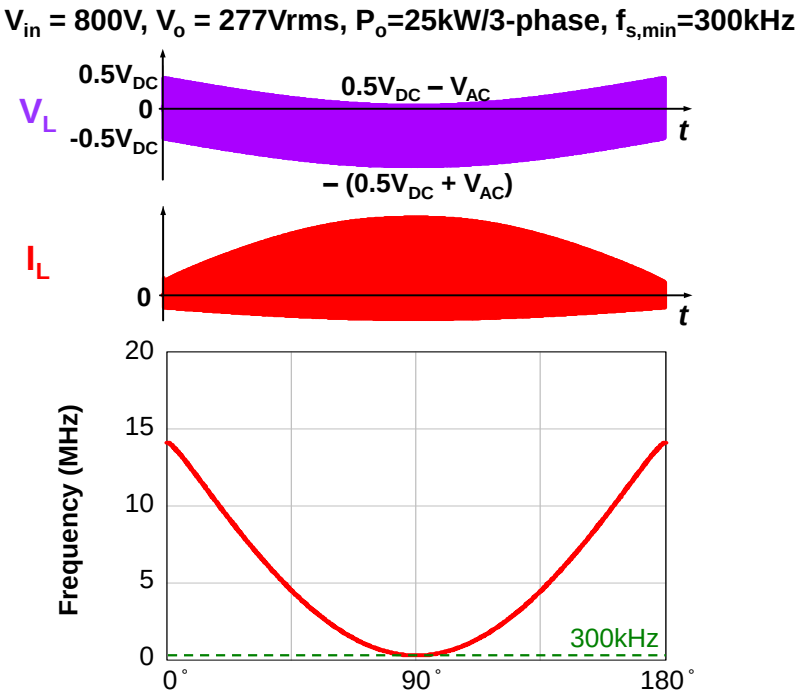


Fig. 5.4. Simulation waveforms and frequency distribution

Prior Art 2: CRM Three-Phase T-Type Rectifier/Inverter

The second reference is a critical mode (triangular current mode) three-phase three-level t-type rectifier/inverter proposed in [E.11]. This topology has split-cap as well which leads to wide frequency variation. The frequency distribution is equivalent to a boost PFC or totem-pole PFC operating with the same AC voltage but one-half DC voltage. The topology, typical waveforms, equivalent circuits, and simulations results are shown in the figures below. Here the minimum frequency at peak AC input voltage is kept the same as 300 kHz and the peak frequency is turned to be around 2 MHz. Although the frequency variation is much reduced compared to the prior art 1 but it is still too wide to be applied to the targeted high frequency design.

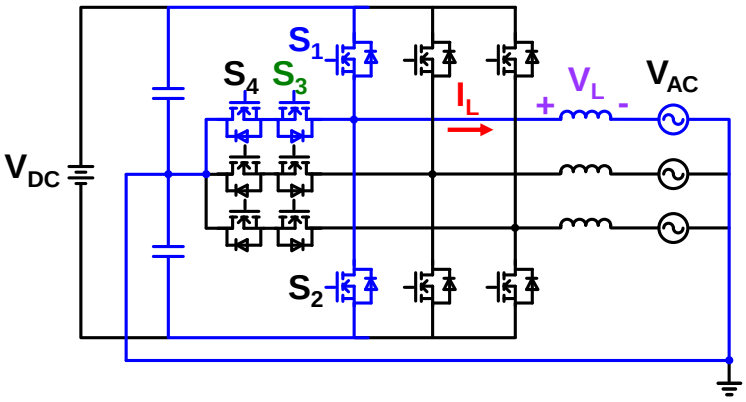


Fig. 5.5. Topology of CRM three-phase T-type rectifier/inverter

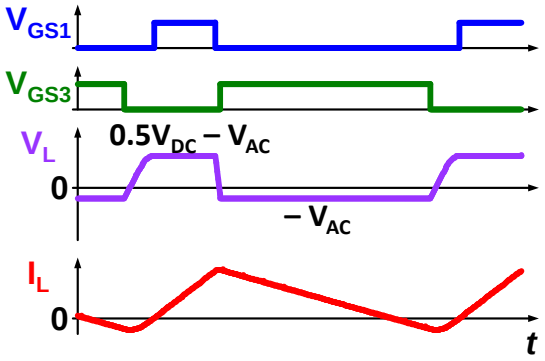


Fig. 5.6. Typical switching cycle waveforms

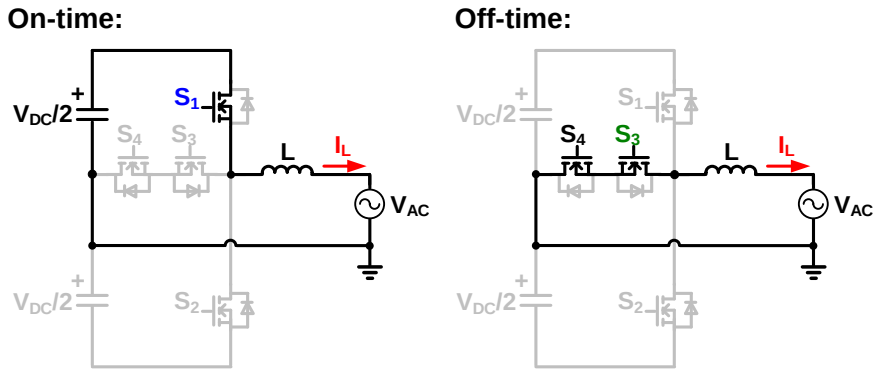


Fig. 5.7. Equivalent circuits during on time and off time (in positive line cycle)

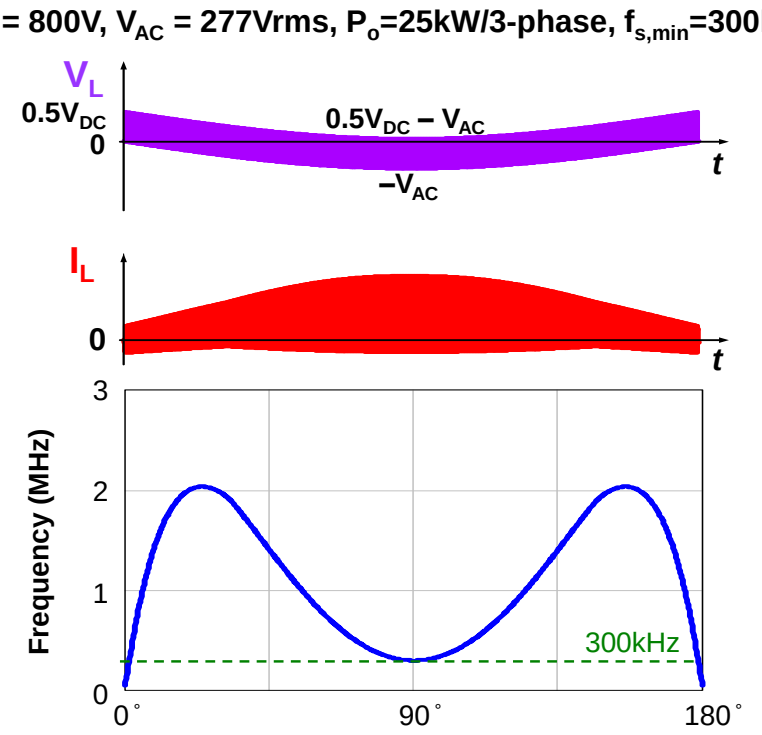


Fig. 5.8. Simulation waveforms and frequency distribution

To quantify the side impacts of large frequency variation on the circuit's performance, a device loss breakdown is given in the figure below. The frequency related loss including switching loss and driving loss are couple of times higher than the conduction loss which indicates that either the design is not appropriate or the frequency chosen is too aggressive. New high frequency

(hundreds of kHz) soft-switching modulation for three phase rectifier/inverter based on critical mode operation is desired and the proposed method is shown in the next section.

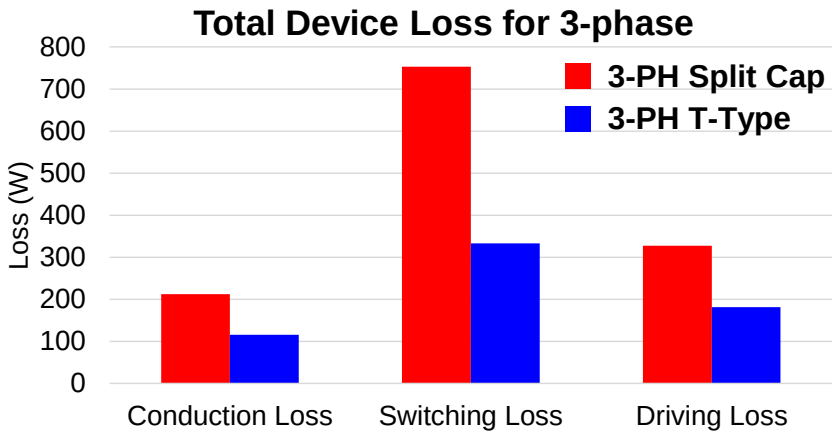


Fig. 5.9. Breakdown of device related losses and comparison

5.2 Proposed DPWM + CRM + Fs. Sync. DCM Modulation

5.2.1 Extension from Single-Phase to Three-Phase

Based on our previous study, for single-phase structure, the totem-pole PFC is well known as the simplest topology among all the bridgeless boost PFC structures [E.12]. By changing the two diodes to two active switches and operating these two active switches at line frequency, this converter is able to operate bi-directionally. In [E.13], high-frequency CRM control is proposed to achieve ZVS soft-switching and good power factor. With inductor current zero-current-detection (ZCD) and programmed Toff extension, whole-line ZVS soft-switching turn-on of control switch is achieved in order to re-duce switching loss and improve efficiency. With average current mode control and proper design of current loop parameters, good power factor and low total-harmonic-distortion (THD) is achieved. Experiment results show that around 98.5% peak

efficiency is achieved for this totem-pole AC/DC converter when setting minimum switching frequency at 300 kHz with this proposed high-frequency soft-switching CRM control.

While applied into three-phase high-frequency AC/DC converter design, this method shows a much narrower switch-ing frequency variation range compared with previous two literature survey results. With minimum switching frequency at 300 kHz, the peak switching frequency is around 500 kHz, which brings much smaller switching related loss. Therefore, it is promising to extend single-phase CRM control to three-phase AC/DC converter to achieve ZVS soft-switching and narrow switching frequency range, which helps to achieve high efficiency.

Since H-bridge structure shown in the figure below is the simplest topology of three-phase AC/DC converters, the analysis below is based on this structure. For three-phase AC/DC converters, the other two phase legs can be naturally used as the current returning path for one phase leg, so unlike totem-pole structure, there is no need for an additional phase leg operating at line frequency.

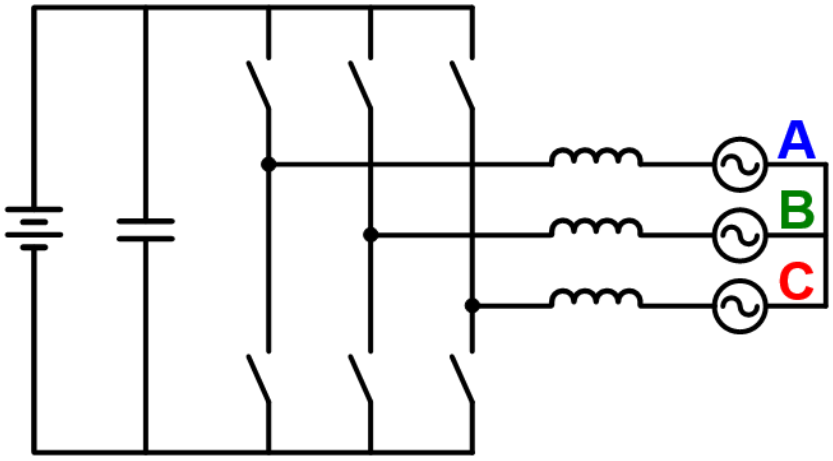


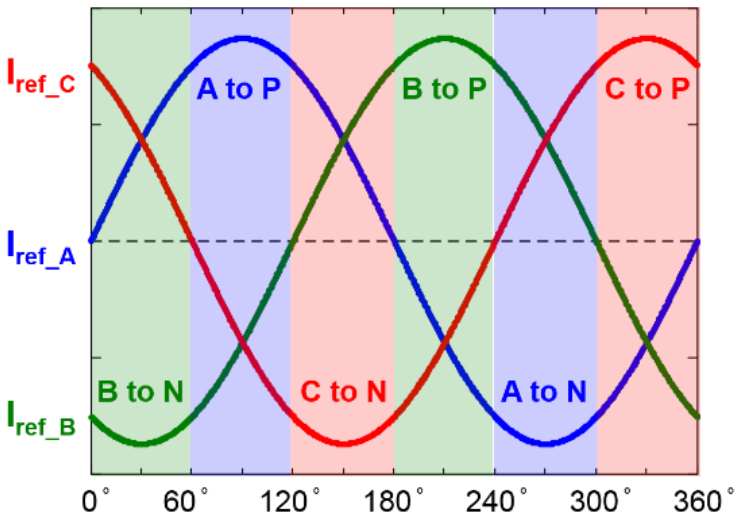
Fig. 5.10. Circuit diagram of three-phase H-bridge structure

However, for three-phase AC/DC converters, the summation of currents in three phases is zero at any instant, which means there are only two control freedom in the three-phase structure.

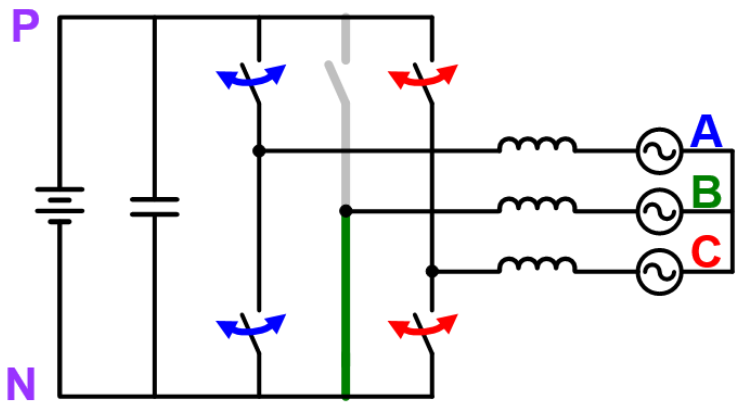
If currents in three phases are still controlled simultaneously, there is control conflict considering controller accuracy and tolerance.

Therefore, only the currents of two phases need to be controlled. If the current in these two phases are well controlled as sinusoidal shape and have good power factor, then the current in the third phase can be naturally in good sinusoidal shape. Here the traditional discontinuous pulse width modulation (DPWM) concept is adopted to achieve this two-phase control [E.14].

In DPWM, the whole line cycle is equally divided into six time regions. In each time region, there is one phase in which AC reference current is around the peak value. This phase is clamped to positive or negative DC bus according to the polarity of AC reference current. The clamping options in line cycle are shown in Fig. 5.11 (a). Take 0 ~ 60 degree as an example. During this 60-degree time region, the reference current in phase B is negative and its amplitude is around the peak value. Therefore, phase B is clamped to the negative DC bus as shown in Fig. 5.11 (b), which is denoted as "B to N" in Fig. 5.11 (a). The other two phases still run at CRM operation.



(a)



(b)

Fig. 5.11. (a) Line cycle DPWM clamping options (b) 0 ~ 60 degree DPWM clamping option in circuit

By applying CRM control and DPWM into the three-phase AC/DC converter, the control diagram of this DPWM-based CRM modulation (hereinafter "DPWM + CRM") during the first 60 degree time region is shown as an example in the figure below.

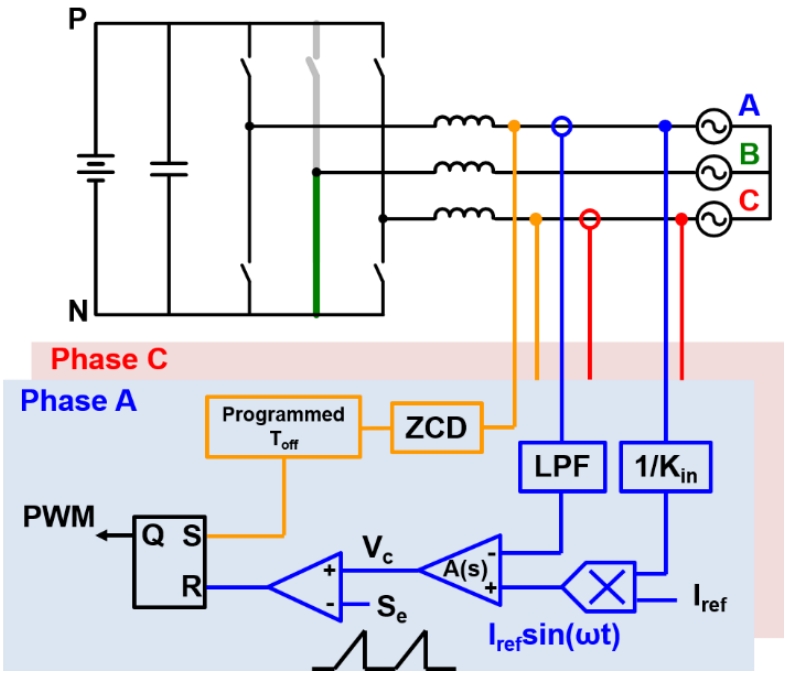
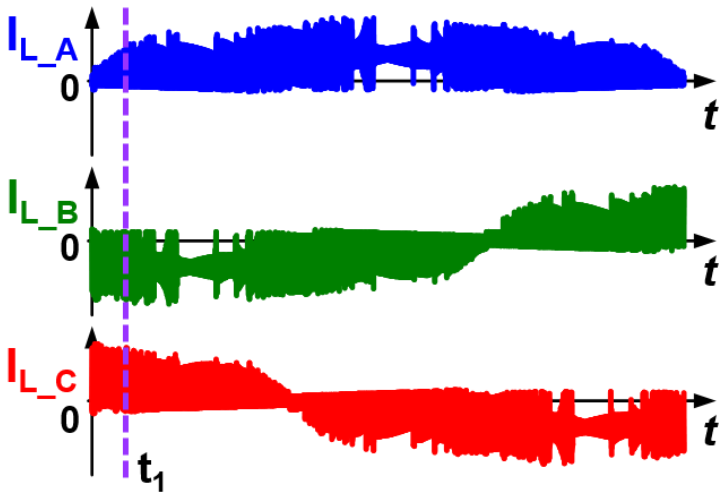


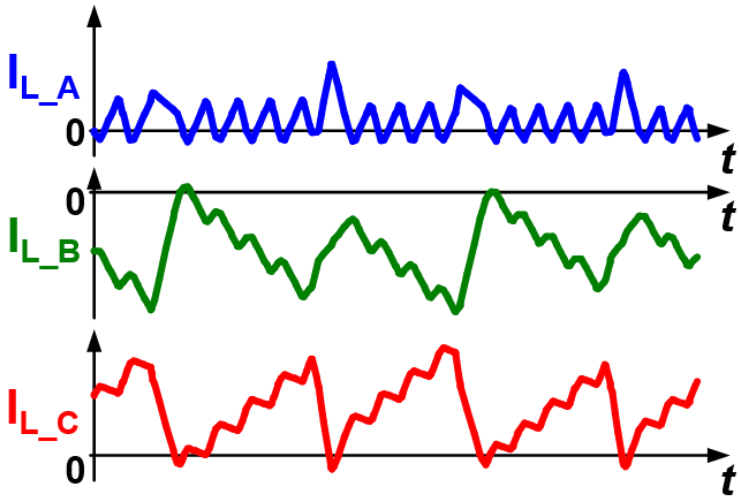
Fig. 5.12. DPWM + CRM control scheme in 0 ~ 60 degree

However, there is an oscillation issue with this DPWM + CRM modulation. Here Fig. 5.13 (a) shows the inductor current waveforms in three phases over a half line cycle, and Fig. 5.13 (b) shows the zoomed-in waveform at t1 instant. From the zoomed-in waveform, it can be clearly seen that there is severe oscillation in phase A inductor current waveform.

The reason of this oscillation lies in individual ZCD for each phase and the interaction among three phases. According to [E.13] or Fig. 5.12, ZCD involves the determination of control switch turn-on instant. Individual ZCD for each phase indicates individual turn-on instant, or non-synchronized turn-on instant for each phase. On the other hand, three-phase H-bridge topology in Fig. 5.10 does not provide electrical decoupling among three phases, which indicates switching action in one phase also has impact on the other two phases. Based on above two aspects, switching actions in each phase becomes unpredictable and even random, and therefore inductor cur-rent in one phase gets unpredictable and even random impact from the other two phases, resulting in oscillation.



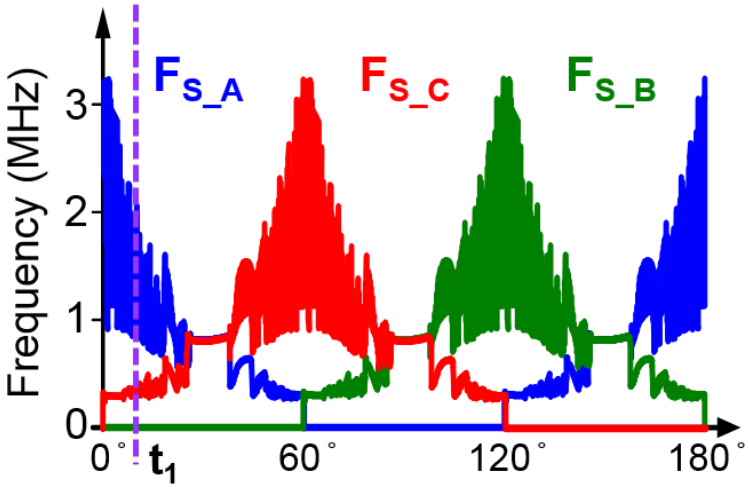
(a)



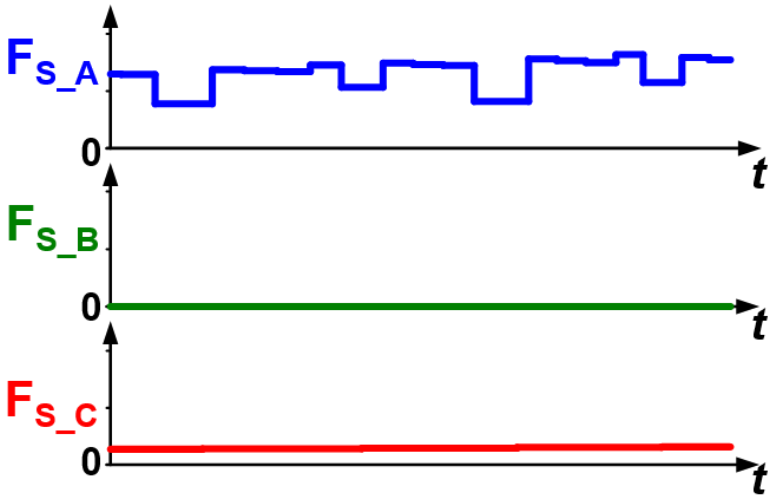
(b)

Fig. 5.13. Inductor current waveforms with DPWM + CRM modulation in three phases (a) over a half line cycle (b) around t1 instant (zoomed-in)

The oscillation also appears in switching frequency distribution. Here Fig. 5.14 (a) shows the switching frequency distribution in three phases over a half line cycle, and Fig. 5.14 (b) shows the zoomed-in switching frequency distribution at t1 instant. This can be explained in the same way in the above.



(a)



(b)

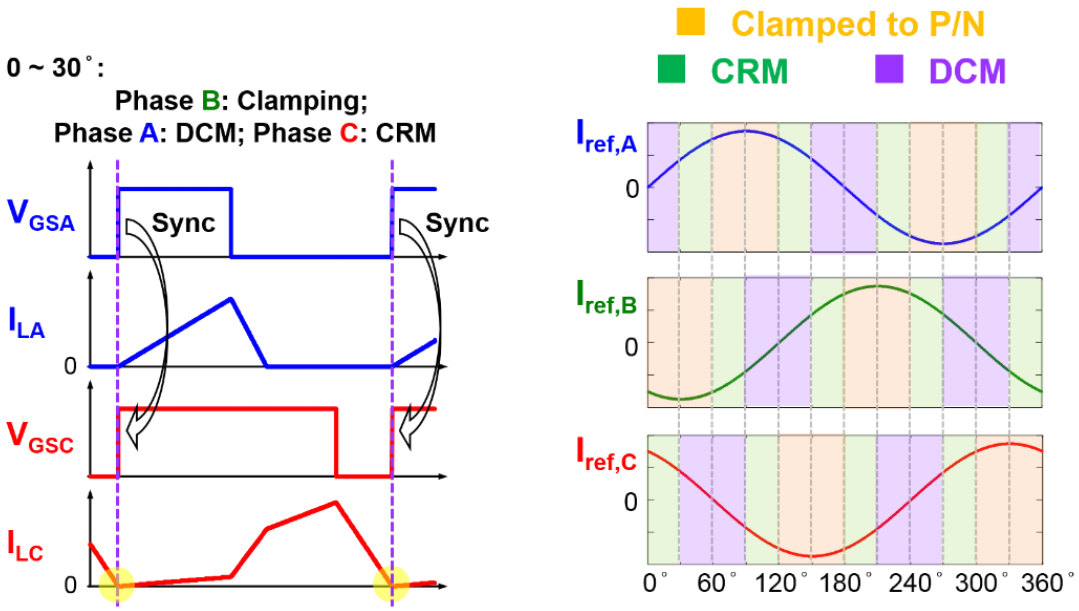
Fig. 5.14. Switching frequency distribution with DPWM + CRM modulation in three phases (a) over a half line cycle (b) around t1 instant (zoomed-in)

Also, according to Fig. 5.14 (a), it should be noted that the switching frequency distribution and variation range is totally different from single-phase totem-pole AC/DC converter case. This is because of the interaction among three phases, and thus inductor voltage excitation, or inductor current slew rate, in each phase becomes totally different, resulting in totally different switching frequency distribution and variation range. When setting minimum switching frequency at 300 kHz, the peak switching frequency is around 2 ~ 3 MHz, which is also not acceptable due to large switching related loss.

5.2.2 Frequency Synchronization

According to previous analysis, the oscillation issue results from individual ZCD in each phase and interaction among three phases. Since for this H-bridge structure shown in Fig. 5.10, the interaction among three phases cannot be avoided, then the key to solve the oscillation issue lies in the modification of control strategy related to ZCD.

From the control diagram in Fig. 5.12, turn-on instant is triggered by ZCD in each phase individually. This individual triggering mechanism causes unpredictable switching actions and thus oscillation issue. One simple idea is to synchronize the switching actions, or to synchronize the switching frequency.



(a) (b)

Fig. 5.15. (a) Implementation of switching frequency synchronization during 0 ~ 30 degree (b) Operation mode distribution in whole line cycle

Also, From Fig. 5.14 (a), it can be clearly seen that severe oscillation only happens at most in one phase during the half line cycle. For example, at first 30 degree of the half line cycle, phase A has more severe oscillation in switching frequency than phase C. Therefore, it is obvious that phase A should be synchronized to phase C. One simple way to implement this synchronization is to make phase A run at discontinuous conduction mode (DCM) operation, while phase C still runs at CRM operation. The turn-on instant of phase A is synchronized to that of phase C, which indicates the turn-on instants of phase A and phase C are both triggered by ZCD in phase C. The waveforms

of gate signals and inductor currents in phase A and phase C are shown in Fig. 5.15 (a) for better illustration. During 30 ~ 60 degree, according to the switching frequency of phase A and phase C, phase C is made to run at DCM operation, and its turn-on instant is synchronized to phase A turn-on instant, while phase A is still running at CRM operation. Both phase A and phase C turn-on are triggered by the ZCD in phase A.

All the analysis above can be applied to other time regions in the line cycle. The operation mode distribution of the three-phase converter in whole line cycle is shown in Fig. 5.15 (b).

It should be noted that in this DPWM-based synchronized CRM modulation (hereinafter "DPWM + CRM + Fs sync."), the control switch turn-off is still determined by the average current loop in each phase.

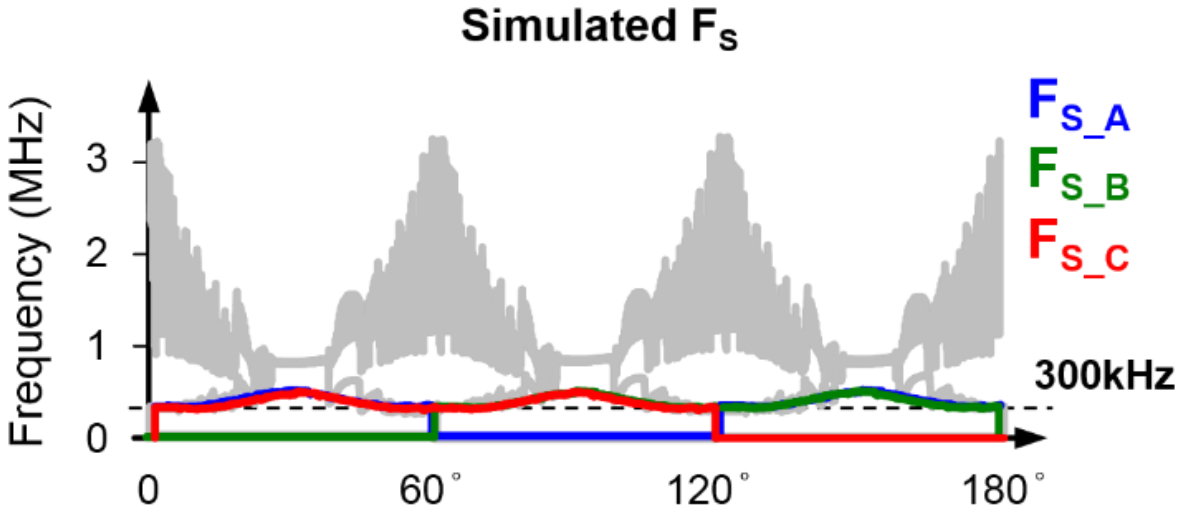


Fig. 5.16. Switching frequency comparison before and after synchronization

With the synchronization of switching frequency, there is a significant reduction in switching frequency when keeping the minimum frequency at 300 kHz. Comparison of switching frequency variation in three phases before (in gray) and after synchronization (in multicolor) over half line

cycle is shown in Fig. 5.16. The switching frequency variation range also shrinks, with peak switching frequency around 500 kHz. It can also be seen that after synchronization, there is no oscillation in switching frequency. The current waveforms will be shown in Section V. to verify that the current is well controlled with this new modulation.

Another important aspect of the performance with this modulation is whether ZVS is achieved during whole line cycle. Take the first 30 degree as an example. Here phase A operate at DCM, phase C operate at CRM, and phase B is clamped to negative DC bus. After phase C inductor current zero crossing point, the inductor and the junction capacitor of switch starts resonance, which helps to discharge switch junction capacitor. However, both phase A and phase C participate the LC resonance, and the equivalent circuit become a 4th order circuit, which is hard to find analytical solutions to this circuit. What is more, the initial condition of phase A is hard to identify, which also adds to the complexity of circuit analysis.

Therefore, simulation is used for ZVS analysis. Take phase C as an example and analyze ZVS when operating at CRM, that is, during the first 30 degree in half line cycle. Inverter mode operation is analyzed first. Three instants: t1, t2 and t3 are arbitrarily selected and the zoomed-in waveforms of gate signal, inductor current and drain-source voltage are shown respectively in the figure below. It can be clearly seen that at each instant, drain-source voltage is able to be discharged to zero before control switch turn-on. This is true for any instant during the first 30 degree, which indicates that ZVS is achieved naturally during the whole time region when operating at CRM under inverter mode. For 90 ~ 120 degree, phase C also operate at CRM and same conclusion is drawn.

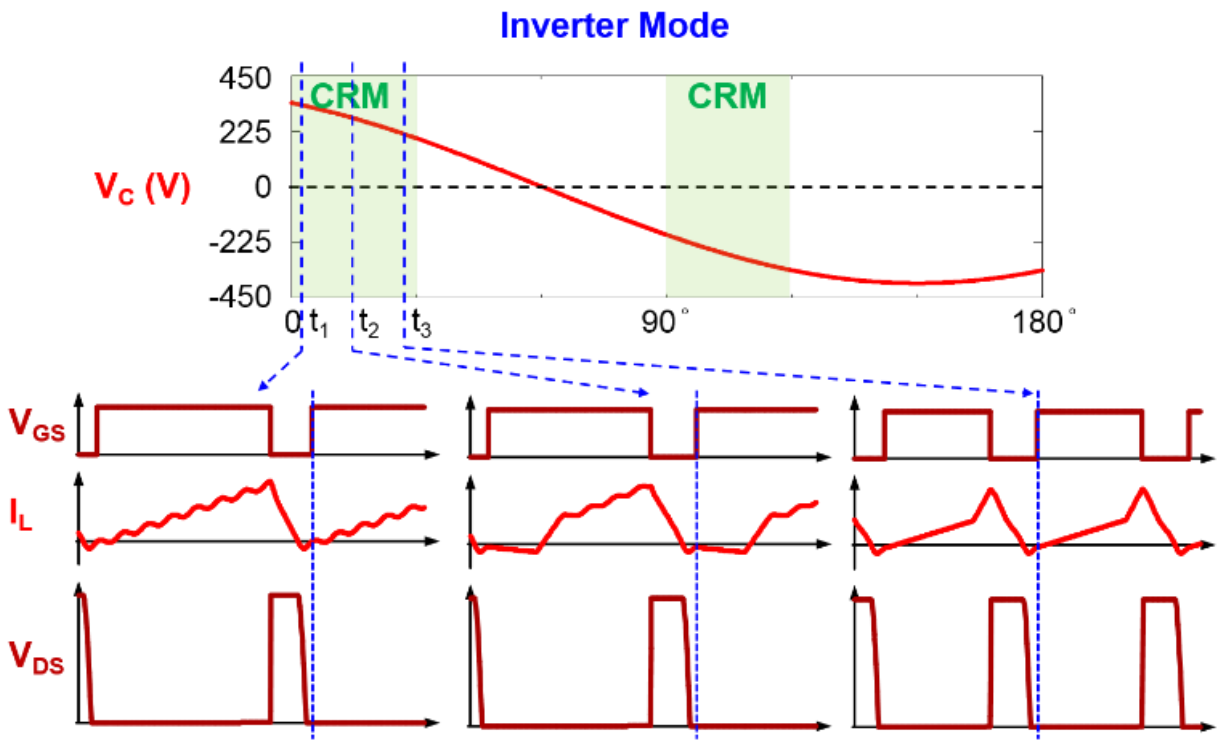


Fig. 5.17. ZVS analysis for the time range operating at CRM in inverter mode

In rectifier mode, however, the conclusion is opposite, that is, Non-ZVS is observed during the entire time region when operating at CRM. The figure below shows the waveforms of gate signal, inductor current and drain-source voltage around the same previously arbitrarily select three instants: t1, t2 and t3. It can be clearly seen that before control switch turn-on, drain-source voltage cannot be discharged to zero, which indicates Non-ZVS in the entire time region when operating at CRM under rectifier mode.

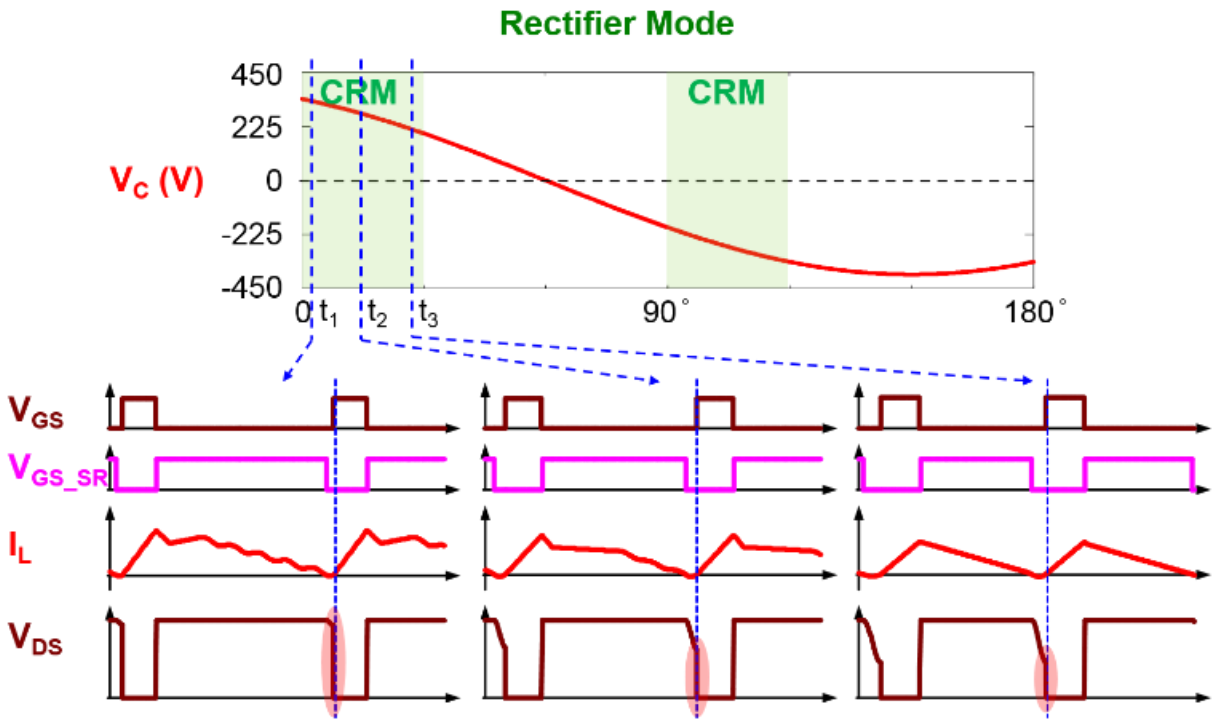


Fig. 5.18. ZVS analysis for the time range operating at CRM in rectifier mode

In order to solve the Non-ZVS issue in rectifier mode, Toff extension is required similar to [E.13]. The main difference is that in [E.13], the analytical required, or saying, optimal negative current is easy to obtain, however, here because of the high order equivalent LC resonance circuit and the initial condition which is hard to identify, there is difficulty in finding the optimal negative current for ZVS.

In simulation analysis, a fixed negative current boundary is applied for achieving ZVS during CRM operation in rectifier mode. The figure below shows that ZVS is achieved with Toff extension. The identification of optimal negative current boundary is part of future work.

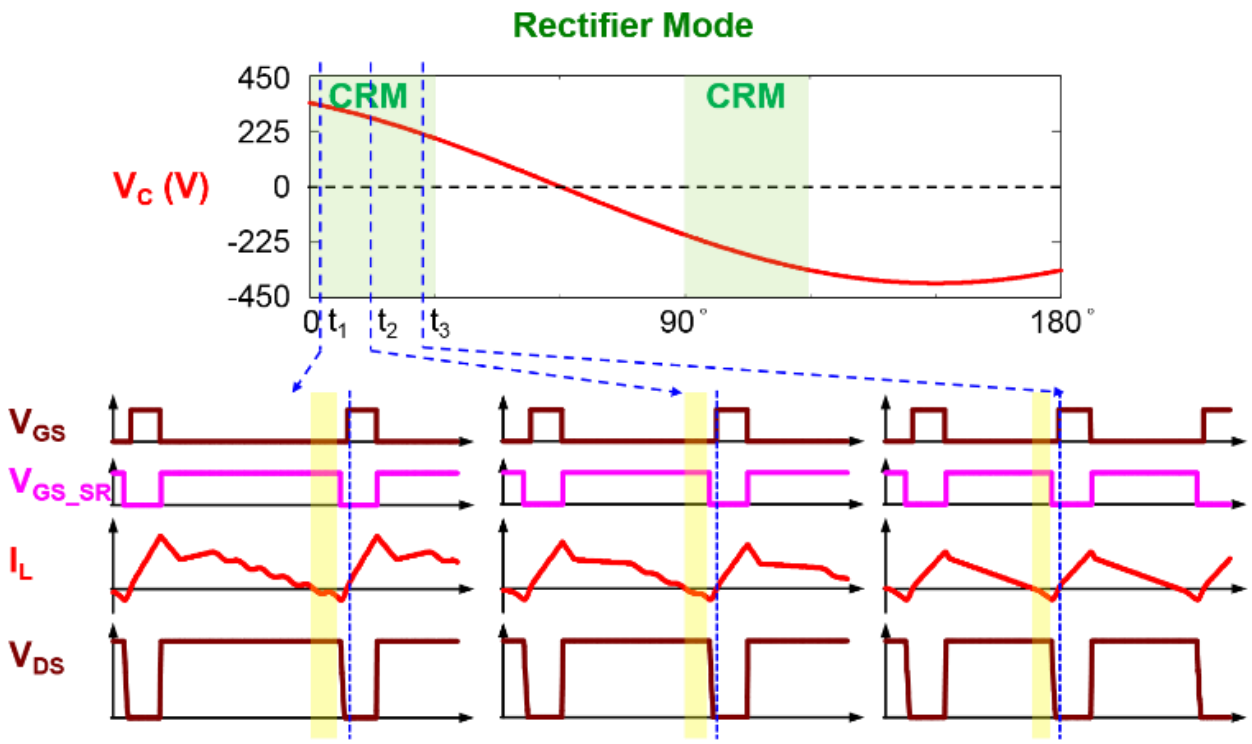


Fig. 5.19. Toff extension for achieving ZVS during operating at CRM in rectifier mode

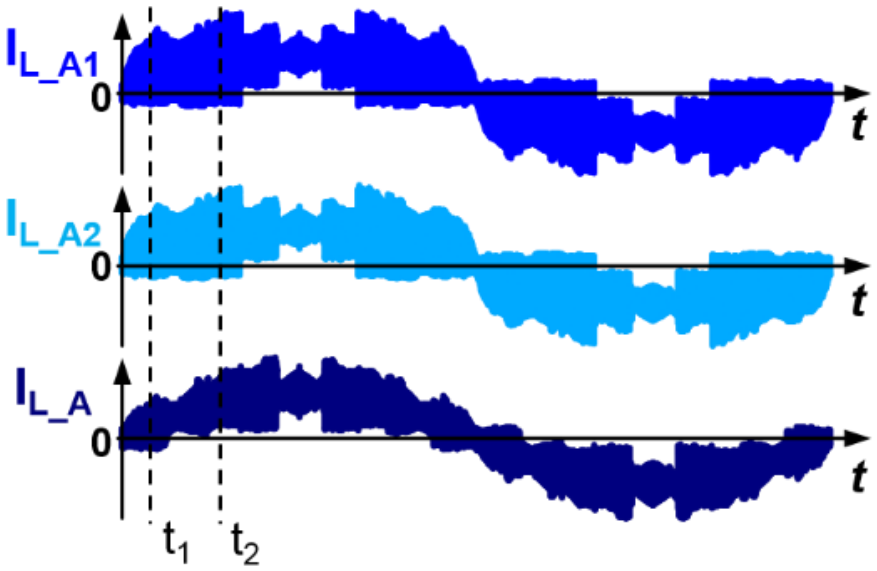
5.2.3 Simulation Verification

According to previous analysis, negative coupling is required to eliminate sub-harmonic oscillation in interleaved rectifier mode operation. In interleaved inverter mode, stable operation is still achieved with the application of negative coupling. Therefore, for bi-directional three-phase AC/DC design point of view, negative coupling is a must.

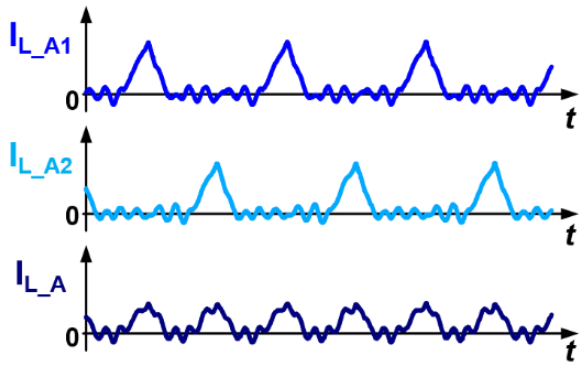
In this section simulation results are shown both for inter-leaved inverter mode operation and interleaved rectifier mode operation. The specification for the three-phase AC/DC con-verter is as below: VAC (RMS) = 277 V, VDC = 800 V, P = 25 kW for three phases, and minimum switching frequency is 300 kHz. The coupling coefficient is selected as 0.5 to provide strong enough coupling.

Fig. 5.20(a) shows the inductor current waveforms and total AC current in phase A during line cycle. Two instants: t1 and t2 are arbitrarily selected and the zoomed-in waveforms around

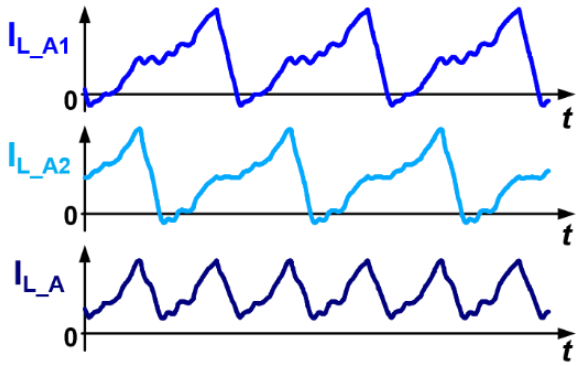
these two instants are shown in Fig. 5.20 (b) and Fig. 5.20 (c), respectively. The ripple cancellation effect can be clearly seen due to interleaving. It should be noted that junction capacitors of switches are considered in the simulation, and there-fore there is some ringing in inductor current due to LC resonance.



(a)



(b)



(c)

Fig. 5.20. Simulation waveforms in interleaved inverter mode in phase A (a) in-ductor current and total AC current during line cycle (b) zoomed-in waveforms at t1 instant (c) zoomed-in waveform at t2 instant

The figure below shows the simulation waveforms of total AC cur-rent (in multicolor) and average AC current (in black) in three phases. The THD of average AC current is around 2%, which indicates the AC current is well controlled as sinusoidal shape.

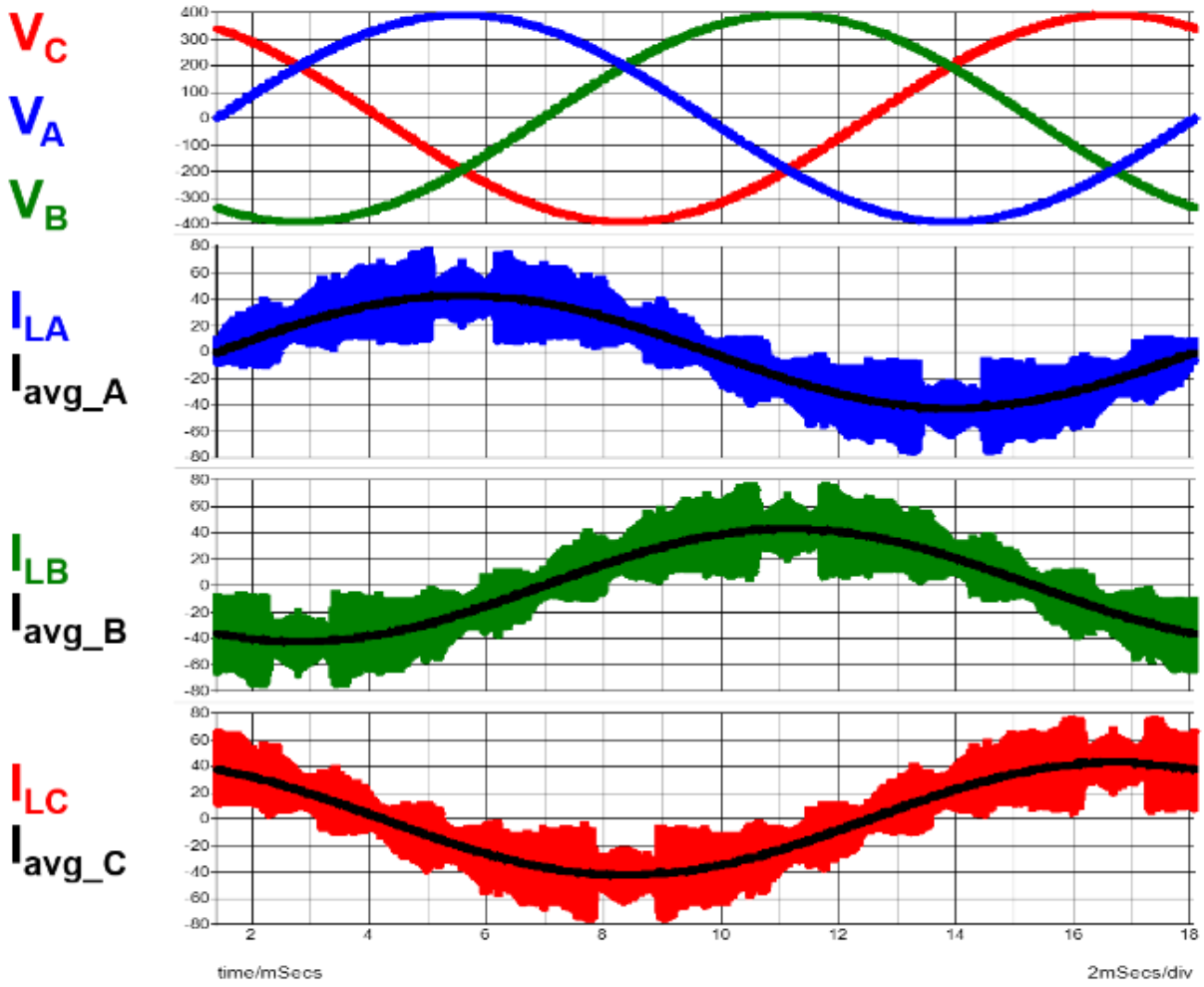


Fig. 5.21. Simulation waveforms of total AC current and average AC current in three phases under interleaved inverter mode

5.3 Hardware Demonstration

A three-phase rectifier/inverter was built to demonstrate the proposed modulation method. The figure below shows the prototype built with GE's 1200 V SiC MOSFET in DE-150 package. The dimensions are marked on the figure, and with 25 kW rated power the estimated power density is 81 W/in3 which is couple of times higher than the state-of-the-art products.

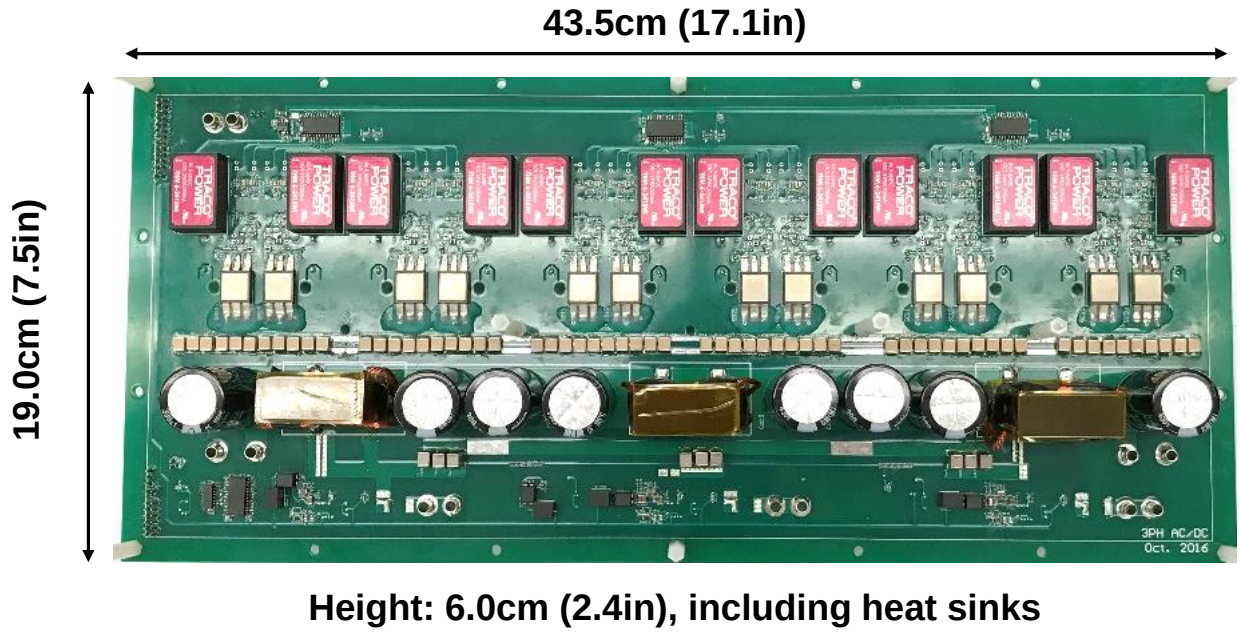


Fig. 5.22. Prototype of three-phase rectifier/inverter

Then the figure below shows the experimental waveforms in inverter mode. Both the AC voltage and current are in good sinusoidal shape. The tested THD is below 5%.

Zoom-in waveforms in different time instant are given which clearly shows that ZVS are achieved in the phase operating in CRM and in DCM which is in accordance with previous analysis. It is also shown that the switching frequency is synchronized between the phase in CRM and in DCM. The tested efficiency of single phase operating at inverter mode is shown in the last figure.

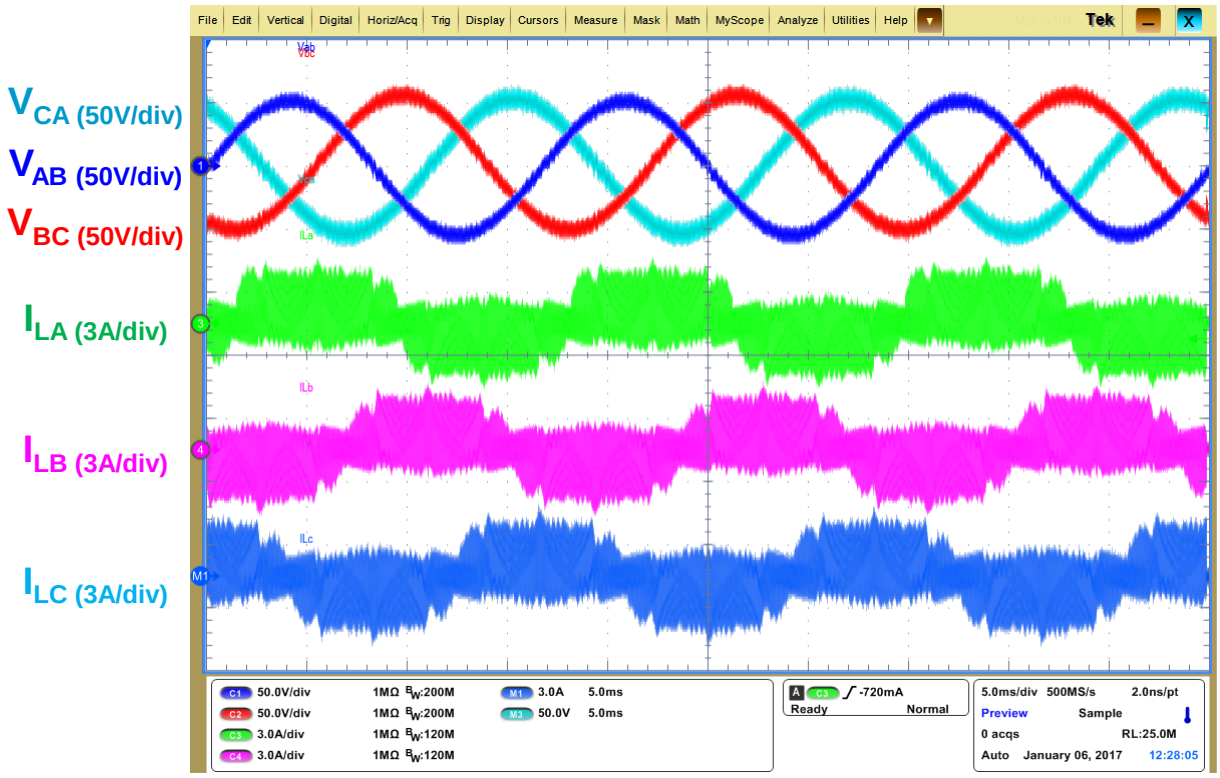


Fig. 5.23. Experimental waveforms in line cycle

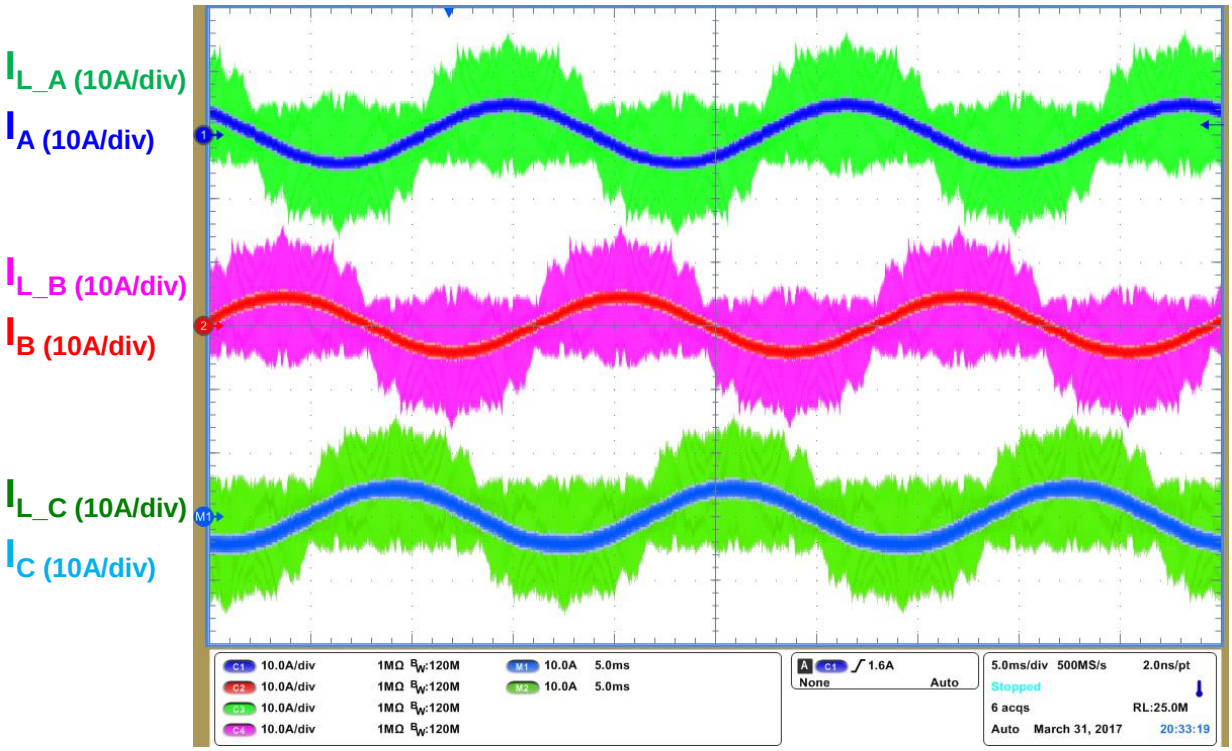


Fig. 5.24. Experimental waveform in line cycle with V_{DC} = 800V, P_o = 5.5kW (~50% Load)

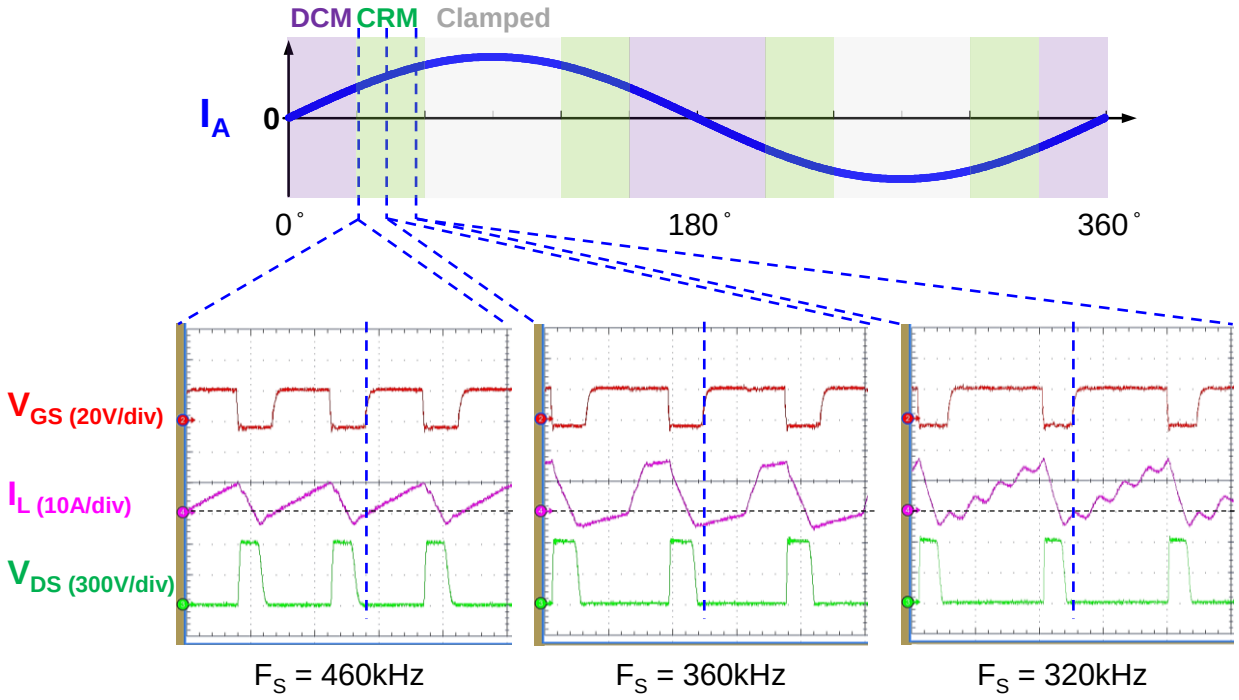


Fig. 5.25. Experimental waveforms in switching cycle of with CRM

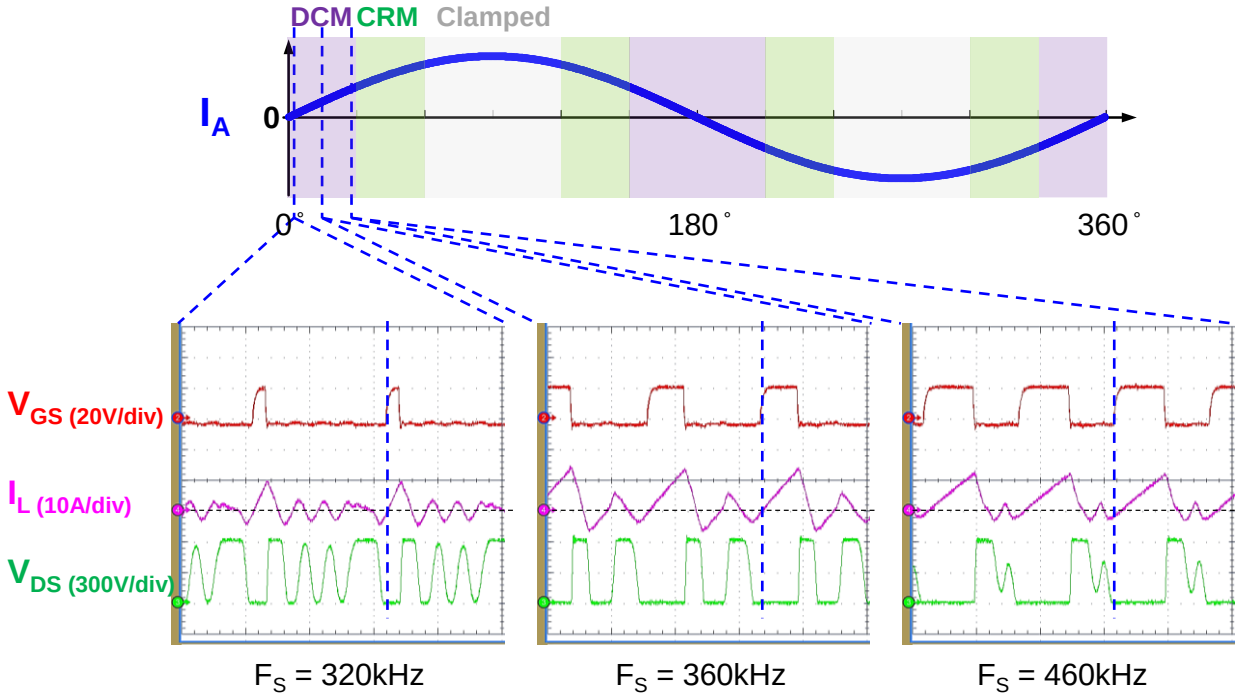


Fig. 5.26. Experimental waveforms in switching cycle of with DCM

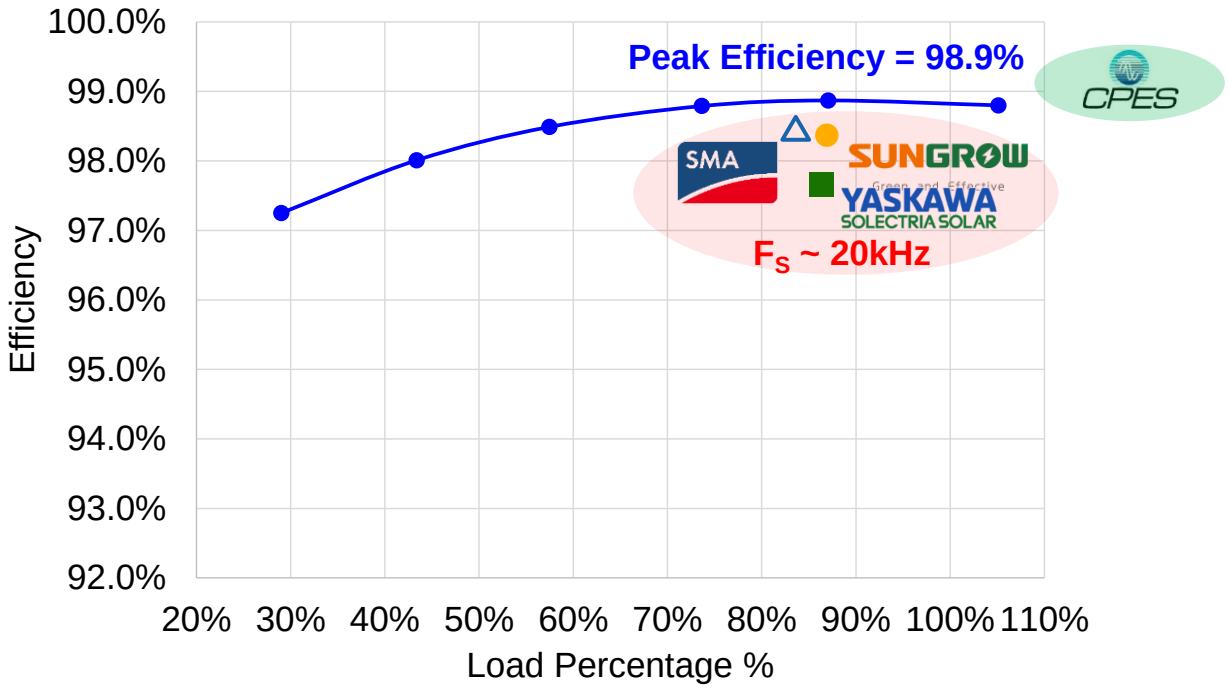


Fig. 5.27. Tested efficiency of inverter mode (V_{DC} = 800V, $V_{AC,L\text{-}N}$ = 277V, single phase full load = 12.5kW)

Chapter 6. Conclusions and Future Work

The emerging wide-band-gap devices have demonstrated significant improvement comparing to Silicon based devices. Comprehensive characterization of WBG devices is conducted in this work especially their behavior under very high switching frequency. It is discovered that both 600V-class GaN transistors and 1200V-class SiC MOSFETs have the character of large turn-on loss and small turn-off loss.

To further push frequency while maintaining high efficiency, soft switching is the most promising approach. For applications of AC/DC power factor correction rectifier and/or inverter, critical mode based soft switching techniques are very suitable. Several inherent issues of CRM rectifier/inverter are identified and the corresponding solutions are proposed and verified.

With the developed CRM PFC technology, high-frequency high-efficiency and high-power-density WBG-based AC/DC converters are demonstrated for several applications like 1 kW server power, 6.6 kW level-2 on board charger, and 25 kW three phase PV inverter. On one hand, this soft switching technology enables the potential of WBG devices to reality; while on the other hand, WBG devices dramatically extend the boundary of CRM soft switching from previous a few hundred watts low power applications to above kW and even tens of kW high power applications.

Control, packaging, and magnetics are three major challenges. For the concern of control, thanks to the wide availability of digital controllers, with MCU and DSP many of the proposed functions and features are successfully demonstrated.

Advanced packaging is not offered by device vender in the beginning. A lot of troubles were caused by the lousy packages in the beginning until we proved it by analysis and experiment and

further improved it by proposed new packaging methods in later time. Finally, many of our ideas got the attentions of device manufacturers and adopted in their products which dramatically improve the performance and reliability of new devices.

New material and new design methodology for magnetics are desperately in need to expedite the application of WBG devices in power electronics systems. PCB winding based inductor is firstly demonstrated in the MHz PFC and will be continually studied in CPES.

The boundary of power level of AC/DC converter operating in CRM is dramatically extended. But the question is where the boundary is and what the relation between device performance and the boundary is. It might be difficult to have a quick answer and it might need a lot of industry practice to approach it, but the good news is the value of rectifier/inverter with WBG devices and CRM soft switching caught more and more attentions and both academia and industry are moving towards this direction.

Reliability of the emerging WBG devices is still a big concern for industrial people to use them in real products. Although the proposed soft switching techniques and advanced packages are helpful to enhance the performance and reduce the failure rate of device to some extent, we didn't speed to much efforts on the evaluation of reliability. And according to my experience as a device user, I did observed that some GaN devices are very easy to fail during test. There is probably a long way to go in order to make GaN devices more reliable but I believe it is worthwhile and the era of WBG devices is coming in the very close future.

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