

Projection of TaSiO_x/In_{0.53}Ga_{0.47}As Tri-gate transistor performance for future Low-Power Electronic Applications

Sarat K. Saluru

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Mantu K. Hudait. Chair
Xiaoting Jia
Levon V. Asryan

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ABSTRACT

The aggressive scaling of silicon (Si) based complementary metal-oxide-semiconductor (CMOS) transistor over the past 50 years has resulted in an exponential increase in device density, which consequentially has increased computation power rapidly. This has pronounced the necessity to scale the device's supply voltage (V_{DD}) in to order to maintain low-power device operation. However, the scaling of V_{DD} can degrade drive current significantly due to the low carrier mobility of Si. To overcome the key challenges of dimensional and voltage scaling required for low-power electronic operation without degradation of device characteristics, the adoption of alternate channel materials with low bandgap with superior transport properties will play a crucial role to improve the computation ability of the standard integrated circuit (IC). The requirement of high-mobility channel materials allows the industry to harness the potential of III-V semiconductors and germanium. However, the adoption of such high mobility materials as bulk substrates remains cost-prohibitive even today. Hence, another key challenge lies in the heterogeneous integration of epitaxial high-mobility channel materials on the established cost-effective Si platform. Furthermore, dimensional scaling of the device has led to a change in architecture from the conventional planar MOSFET to be modified to a 3-D Tri-gate architecture which provides fully depleted characteristics by increasing the inversion layer area and hence, providing superior electrostatic control of the device channel to address short channel effects such as subthreshold slope (SS) and drain induced barrier lowering (DIBL). The Tri-gate configuration provides a 'steeper' SS effectively reducing leakage current (I_{OFF}), thereby decreasing dynamic power consumption and increasing device performance. Recently, Tantalum silicate (TaSiO_x) a high- κ dielectric has been shown to exhibit superior interfacial quality on multiple III-V materials. However, there is still ambiguity as to the potential of short-channel devices incorporating alternate channel (III-V) materials which is the basis of this research, to demonstrate the feasibility of future high-mobility n-channel InGaAs material integration on Si for high-speed, low-power, high performance CMOS logic applications.

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GENERAL AUDIENCE ABSTRACT

Everyone today is dependent on some sort of an electronic device be it a computer, laptop, tablet or a phone powered by the boom of the Silicon Valley. All of which have witnessed significant improvement in performance due to the increase in the number of transistors in a microprocessor (similar to horsepower of a car) which is made possible due to the dimensional scaling of the transistor device features (currently at 14nm). With increased transistor density, a higher power consumption is consequential creating a trade-off between performance and power consumption (battery life). However, there are limitations as to how small a transistor can be scaled. This has provided precedence to employ alternate materials such as III-V alloys and Germanium to reduce power consumption (due to a lower band gap; which dictates how much energy is consumed) while simultaneously improving device performance by providing a mobility boost (which is a property of the aforementioned materials that allows current to flow faster, thereby improving device performance). The aim of this work is evaluate leading device architectures incorporating alternate channel materials (InGaAs in particular which is a very suitable III-V alloy) to develop a simulation model that is calibrated to existing data to project device performance future transistor nodes.

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Chapter 1 – Introduction

1.1 Silicon-based MOSFET scaling history and limitations

Over the past 50 years, silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) have dominated the semiconductor industry ever since its first experimental demonstration in 1959 [1]. Following the demonstration of planar transistor architecture in 1960 [2] and then its implementation to create the first commercial integrated circuits (ICs) based on Si MOSFETs in 1964 [3], Moore's Law [4] was conceptualized in 1965 to capitalize on the dimensional scaling of Si-based MOSFETs to improve IC computing ability. Ever since, transistor feature sizes have been drastically scaled down, resulting in an exponential increase in device density, and thus computing power. However, conventional scaling of device dimensions becomes increasingly difficult mainly due to increased power consumption in addition to fundamental limitations. Fig. 1.1 [5] shows a data conglomeration of subthreshold (red) and active (blue) power densities from commercial Si MOSFETs. The trend demonstrates that subthreshold power density increases much quicker than active power density with gate length reduction. Adding to this, the subthreshold power density suggests to surpass active power density at the crossover point (black circle) below the 20-nm gate length. It is therefore very critical to scale transistor supply voltage (V_{DD}) with continued device dimensional scaling. The relation between V_{DD} and total power dissipation can be given by [6]:

$$P = n(CV_{DD}^2f + V_{DD}I_{OFF}) \quad (1.1)$$

where P is total power consumption, n is the number of transistors, C is the load capacitance, V_{DD} is supply voltage, f is the operation frequency, and I_{OFF} is the off-state current.

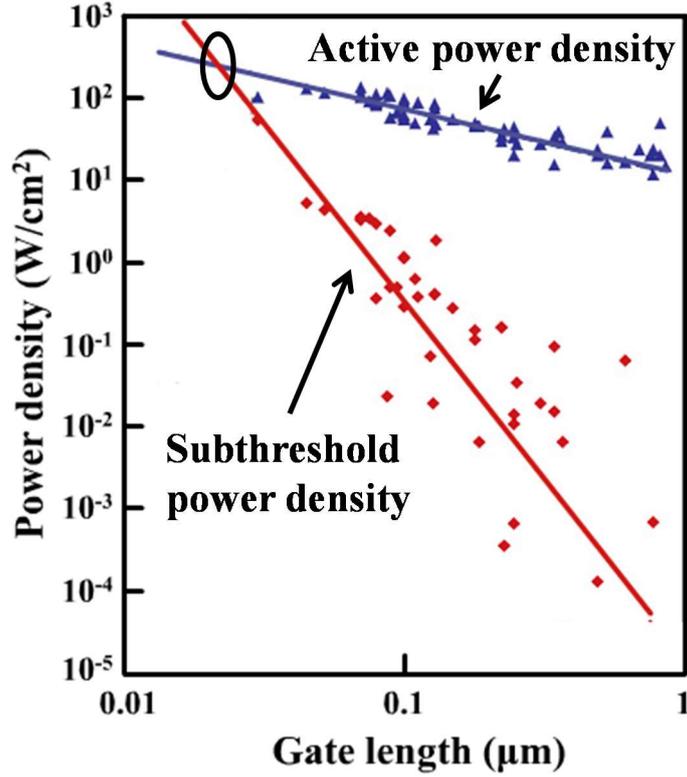


Figure 1.1 Active (blue) and subthreshold (red) power densities from commercial Si MOSFETs with gate lengths between 0.01 μm to 1 μm . The cross-over point (black circle) at sub 20-nm gate length indicates where subthreshold power density surpasses active power density [5].

However, V_{DD} scaling also greatly reduces the transistor drive (on-state) current, and thus, directly impacts device performance. The dependence between V_{DD} and I_{ON} can be expressed by [6]:

$$I_{ON} = \frac{W}{2L} \mu C_{ox} (V_{DD} - V_{TH})^2 \quad (1.2)$$

where I_{ON} is the ON current in the saturation region, W is the transistor width, L is the transistor length, μ is inversion charge carrier mobility, C_{ox} is the oxide capacitance, V_{DD} is the supply voltage, and V_{TH} is the threshold voltage. With the reduction of V_{DD} and subsequently V_{TH} , other parameters must be increased in order to improve or maintain constant I_{ON} .

Beyond the sub-100nm technology node, conventional scaling of device dimensions was no longer possible due to the impact of V_{DD} on device performance and thus, novel architectural innovations were introduced to the MOSFET as a means to ensure the continuity of Moore's Law [7]. At the 90 nm technology node, degrading drive current brought out the need to boost the carrier mobility, μ , through the implementation of uniaxial strain on the Si channel using silicon-germanium (SiGe) source/drains and silicon nitride (Si_3N_4) etch stops, thereby enhancing CMOS transistor drive current, I_{ON} , respectively [8]. At the 45 nm node, a metal gate along with a scalable high- κ gate dielectric was introduced in place of the conventional silicon dioxide (SiO_2) oxide to improve gate electrostatics thereby increasing oxide capacitance, C_{ox} , to further enhance transistor drive current, while at the same time reducing off-state leakage, an issue that had come to be of serious concern with SiO_2 scaling [9]. At the 22 nm node, a novel fin field effect transistor (FinFET) design was implemented bringing in the first generation of three dimensional transistor technology, yielding more gate control and thus further improving device performance at lower gate voltages while continuing dimensional scaling [10]. Currently in production are 14 nm transistors, which implement a taller fin design to aid with increased drive current [11]. Fig. 1.2 shows the evolution of the Si-based MOSFET as the industry scaled from the 130 nm node down to the 22 nm three dimensional node. However with smaller nodes that need to be observed in the future, fundamental constrains will restrict the performance of Si-based MOSFETs. As a result of this, alternate materials are under consideration to maintain the continuity of Moore's Law. According to the 2014 ITRS, III-V, germanium (Ge), carbon nanotube, and 2D materials (MoS_2 , WSe_2 , etc) are examples of such channel materials under consideration for future nodes [12].

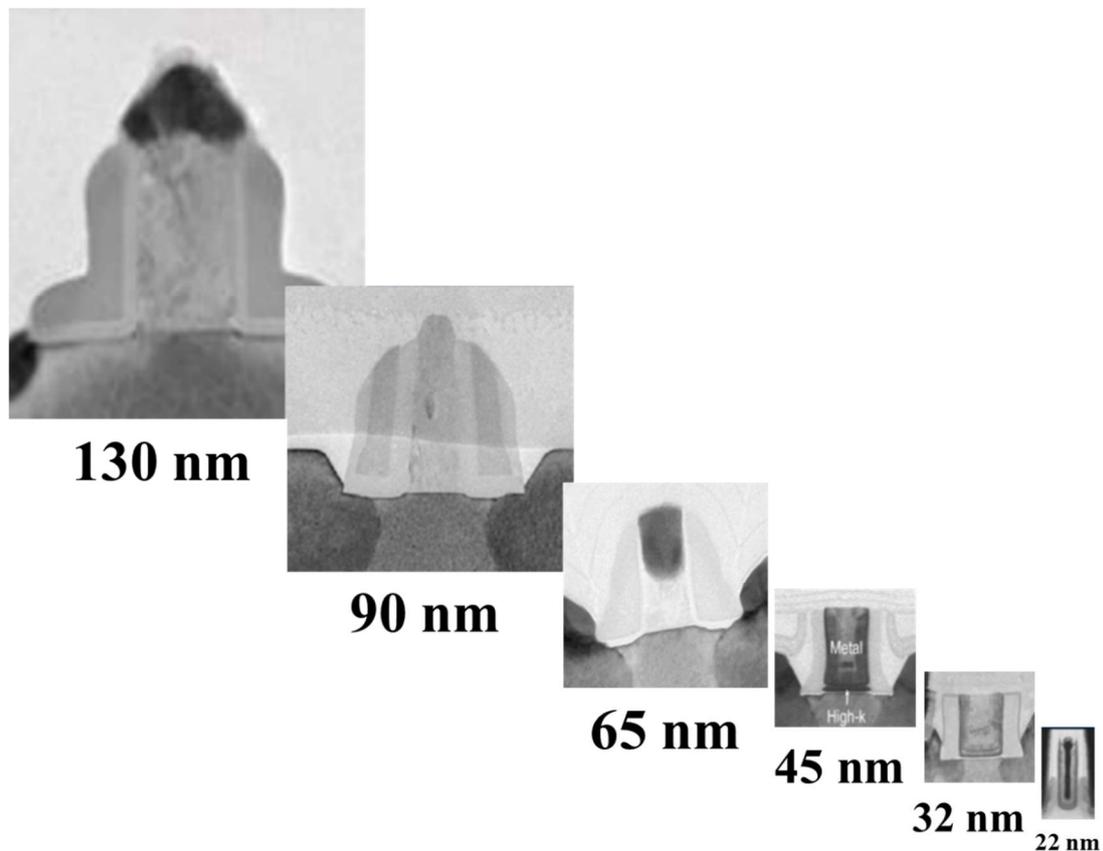


Figure 1.2 Fundamental changes in the Si-based MOSFET as starting at 130 nm node down to the 22 nm node [13]

1.2 Multi-gate FET's for improvement of electrostatic control

The aggressive scaling of gate features with the requirement of superior transport based alternate channel materials (Ge and III-V), has identified short channel effects like subthreshold swing (SS) degradation and drain induced barrier lowering (DIBL) as another obstacle despite the existing problem of engineering superior oxide/channel interfaces. Subthreshold swing degradation and DIBL are caused by the dominating encroachment of electric field lines from the drain into the channel region to deteriorate the gate's electrostatic control of the channel leading to the reduction of the threshold voltage (V_T). The distribution of the electric potential in the channel of a MOSFET is described by Maxwell's equation as [14]:

$$\nabla \cdot \mathbf{D} = \nabla \cdot \epsilon \mathbf{E} = \rho = \text{constant} \quad (1.3)$$

where \mathbf{D} , is the electric displacement field, ϵ is the permittivity of the material under consideration and, \mathbf{E} is the electric field in the region of consideration and ρ is the local density of electric charge. A conventional planar MOSFET can be described by Maxwell's equation/ Poisson's equation which describes the equilibrium between charge and field as:

$$\left[\frac{dE_x}{dx} \right] + \left[\frac{dE_z}{dz} \right] = \frac{\rho}{\epsilon} \quad (1.4)$$

where the lateral field in the channel is from the drain to source (x-direction) and vertical electric field from the gate (z-direction). 3-D transistors allow the application of gate induced electric field in the y-direction to increase the dimensionality of electrostatic control of the gate over the channel. The resulting three-dimensional Poisson's equation is described as:

$$\left[\frac{dE_x}{dx} \right] + \left[\frac{dE_y}{dy} + \frac{dE_z}{dz} \right] = \frac{\rho}{\epsilon} \quad (1.5)$$

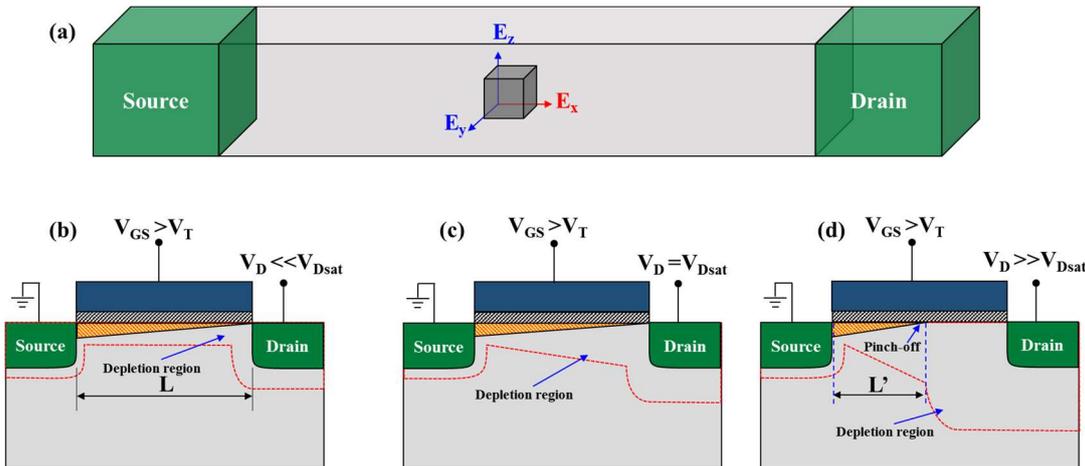


Fig. 1.3 (a) shows the distribution of electric field in the channel, E_z represents source-drain electric field line while E_x and E_y represent gate electric field lines. (b), (c) and (d) shows channel degradation for a MOSFET operated in linear, onset of saturation and deep saturation respectively.

Fig. 1.3 shows channel degradation as a consequence of the large depletion region due to penetrating drain-source field line. With comparison of equations (1.4) and (1.5), and a few simple assumptions a parameter called natural/geometric screening length (λ), which reflects the penetration of the drain electric field lines from the drain to the source, can be calculated, and the minimum gate length (L_g) is about 6-7 times the screening length (λ). Particularly, λ_N can be given by [15-17]:

$$\lambda_N = \sqrt{\frac{\epsilon_{ch} t_{ch} t_{ox}}{N \epsilon_{ox}}} \quad (1.6)$$

where ‘N’ is the effective gate number; N=1, 2, 3, 3.14, 3.4 and 4 for Single-gate, Double-gate, Tri-gate, Pi-gate, Omega-gate and Gate-all-around devices respectively. The above equation is valid for channels of radial and bi-lateral symmetry i.e., square/circular cross-section.

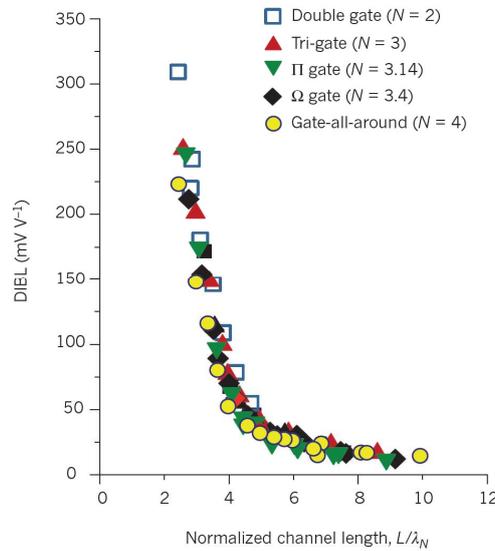


Fig. 1.4 Variation of DIBL with channel length, Short channel effects are more pronounced when $L/\lambda_N < 6$. The normalization masks the improvement of short-channel performance by multiple-gate structures by which need conventional single-gate MOSFETS would require \sqrt{N} times larger gate lengths for similar short channel performance [15]. Copyright © 2011, Rights Managed by Nature Publishing Group

A normalized parameter (L/λ_N) helps estimate short channel performance universally for a given material. Fig. 1.4 shows the variation of DIBL with channel length [15]. Short-channel effects pose a serious problem, both of which contribute to higher leakage current and the increase of DIBL causes the loss of switching speed as given in Eq. 1.7 [15, 18].

$$\frac{\Delta f}{f} = \frac{2\text{DIBL}}{V_{DD} - V_{TH}} \quad (1.7)$$

1.3 Impact of dielectric selection

With the introduction of the high- κ /Metal gate stack (HKMG) to replace of SiO_2 /poly-Si gate stack at the 45 nm node [9], the developed technology allowed thicker oxides for a given capacitance substantially reducing tunneling induced gate leakage. The comparison of high- κ and conventional SiO_2 is expressed by the equivalent oxide thickness (EOT) as:

$$\text{EOT} = \left(\frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{High-}\kappa}} \right) t_{\text{High-}\kappa} \quad (1.8)$$

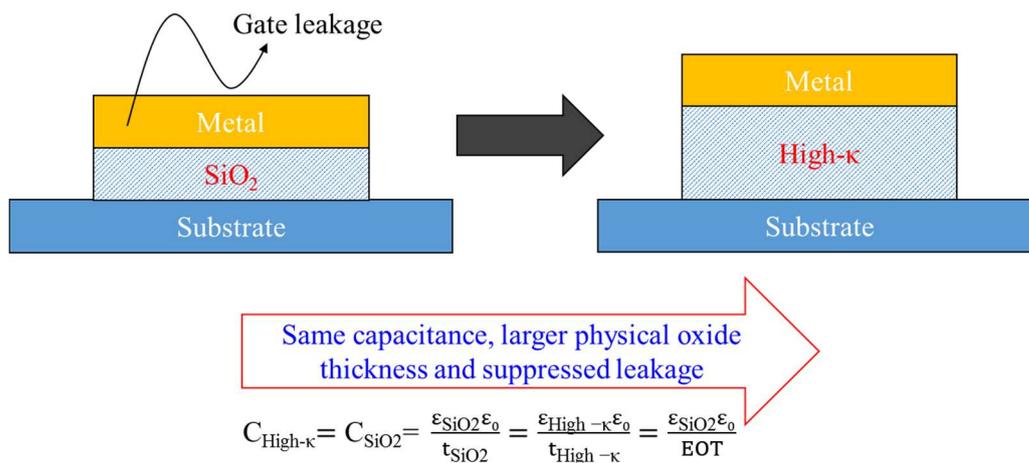


Fig. 1.5 Illustration of the replacement of SiO_2 /poly-Si gate stack with high- κ /metal (HKMG) to achieve same capacitance while suppressing gate leakage

With the implementation of alternate channel materials, the impact of high- κ dielectrics on device performance and short channel effects is immense as illustrated in Fig. 1.6. All simulations were conducted on Tri-gate $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The improvement is expected with the reduction of the natural length (λ_N) as discussed earlier.

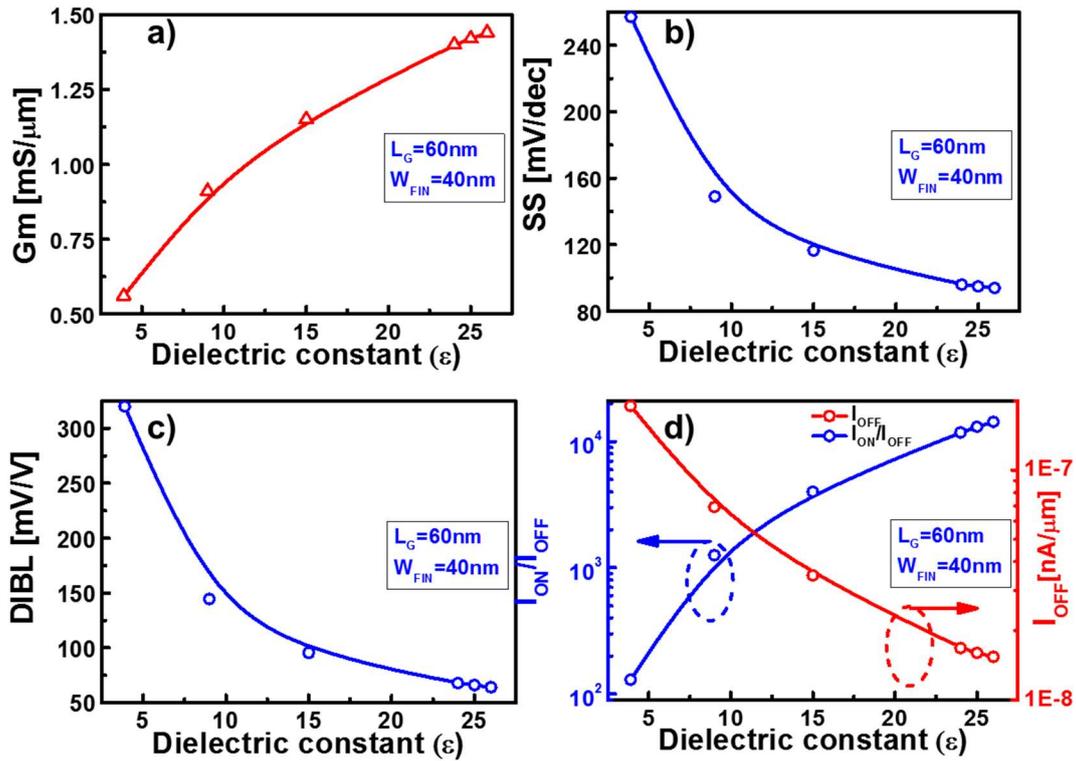


Fig. 1.6 (a), (b), (c) and (d) is an illustration of the impact of the choice of dielectric constant on device characteristics assuming uniform interfacial quality.

1.4 Semiconductor/oxide interface

The Si/SiO₂ interface is treated as ‘*the*’ ideal interface with no traps or states at the interface. But in real-life, the interface and bulk SiO₂ is not truly electrically neutral. This is a result of positive/negative charge at the interface (traps), mobile ionic charge and fixed oxide trap charge within the oxide all of which are a result of fabrication processes developed to optimize device performance. That being said, the electrical properties of a device are immensely sensitive to the interface quality, namely the

distribution of the interface trap density (D_{it}) distribution along the bandgap [14] as will be discussed in this work.

The perpetrator being traps formed due to dangling bonds at the interface, extensive work goes into engineering a more ideal interface, especially in the case of utilizing III-V materials as an alternate channel. The trapping of carriers (electrons or holes) creates a net charge at the interface. The probability of which can be modelled using Fermi-statistics which is based upon the energy relative to the Fermi-level (E_F) (while accounting for ground-state degeneracy depending on trap nature [14]) as shown in Eq. 1.9 and 1.10 for a donor-like trap and acceptor-like trap, respectively.

$$F_D(E_t) = \frac{1}{1 + g_D \cdot \exp\left(\frac{E_F - E_T}{K_B T}\right)} \quad (1.9)$$

$$F_A(E_t) = \frac{1}{1 + g_A \cdot \exp\left(\frac{E_T - E_F}{K_B T}\right)} \quad (1.10)$$

where $g_{A,D}$ (the ground-state degeneracy) is 2 and 4 for donor and acceptor states, respectively.

A very important note to make is the nature of traps, whether at the interface or in the bulk of the semiconductor can affect the nature of the D_{it} distribution. A trap is considered to be donor-like if it can be neutral or can become positive (by donating/giving up) an electron. Similarly, an acceptor is either neutral or becomes negatively charged by accepting an electron. Since the D_{it} is fixed for a particular energy level, the variance of surface potential affects the occupation probability with the sweeping of the Fermi-level across the forbidden band. The neutrality of a

semiconductor can vary from the interface to the bulk and can be measured with knowledge of the variation of surface potential with gate bias [14].

A general interface trap system is shown in Fig. 1.7 consisting of donor and acceptor traps relative to the charge neutrality level (E_{CNL})

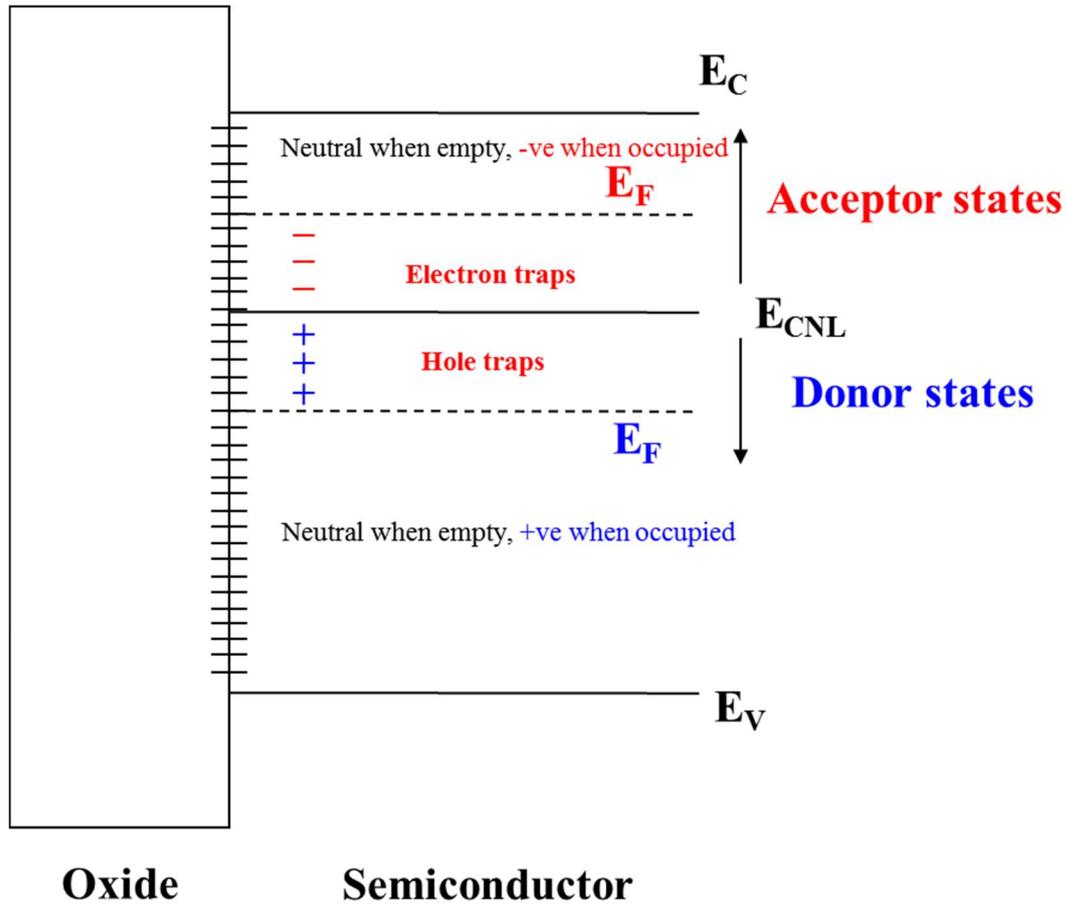


Fig. 1.7 Interface trap system consisting of donor-like and acceptor-like traps. When E_F is below E_{CNL} , the net charge is positive and when E_F sweeps past the neutrality level (E_{CNL}), the net charge is negative.

In order to calculate the total trapped charge at the interface (Q_{it}), we assume ideal Fermi-statistics (i.e, $T=0$ K), where the probability of occupation below E_F is 1, and above E_F is 0 to simplify calculations in the integral shown in Eq 1.11:

$$Q_{it} = \pm q \int D_{it} dE \quad (1.11)$$

The integral is positive below E_{CNL} and negative above it. This effective net charge per unit area (C/cm^2) can degrade device performance as will be discussed later in this work. The distribution of interface can be expressed as:

$$D_{it} = \frac{1}{q} \frac{dQ_{it}}{dE} \text{ \# of traps (cm}^{-2}\text{eV}^{-1}\text{)} \quad (1.12)$$

However, this expression does not distinguish the nature of traps [14]. With the consideration of traps, the application of bias to an MOS structure will observe the movement of the Fermi-level across the band edges (depending on polarity of the bias applied) changing the occupation probability of traps in the process. When the Fermi-level E_F , coincides with the charge neutrality level E_{CNL} , the interface is said to be neutral. A deviation of E_F from E_{CNL} creates a net charge which affects band bending. Band bending at the interface is determined by the balance between interface trap charge (Q_{it}) and the depletion charge (Q_D) in the depletion region of the semiconductor. The charge neutrality levels are shown in Table 1.1 [19, 20].

1.5 III-V alloys as an alternate channel material

With the requirement to explore high-mobility channel materials for future technology nodes, many III-V materials have been considered as possible replacements to conventional Si-based nMOSFETs. Since carrier mobility μ and I_{ON} are directly proportional, from Eq. 1.2, replacing Si-based channels with high-mobility materials will have a positive impact on I_{ON} , and thus, overall device performance. The bulk mobilities and bandgaps of several semiconductors under consideration are compared in Table 1.1. For high-performance complementary MOS (CMOS) logic, it seems logical to have III-V materials and Ge serve as the NMOS and PMOS channel material, respectively.

Parameters	InAs	Ge	In _{0.53} Ga _{0.47} As	Si	GaAs
Electron mobility (cm ² Vs)	4 × 10 ⁴	3900	12000	1400	8500
Hole mobility (cm ² Vs)	500	1900	300	450	400
Bandgap (eV)	0.354	0.661	0.74	1.12	1.424
Intrinsic carrier density (cm ⁻³)	1x10 ¹⁵	2x10 ¹³	6.3x10 ¹¹	1x10 ¹⁰	2.1x10 ⁶
CNL (from Ev) (eV)	0.5	0.1	0.53 (assumed)	0.2	0.55
ε	15.15	16.2	13.9	11.7	12.9

Table 1.1 Carrier mobility and bandgap of Si, Ge, and common III-V materials [19-21].

However, with reduction in bandgap, the exponential increase of intrinsic carrier density which by thermionic emission causes drastic leakage [22]. Hence, with improvement in mobility and reduction in bandgap, it is critical to maintain a low intrinsic carrier density. Indium gallium arsenide (In_xGa_{1-x}As) in particular with 53% Indium content (In_{0.53}Ga_{0.47}As) has an almost 10x improvement in electron mobility as compared to Si, the composition of indium (In) will be discussed later in this thesis. Furthermore, it's low bandgap of 0.74 eV, this ternary compound suitable for low-power devices operating at a low supply voltage ($V_{DD} \leq 0.5$ V). However, two major challenges must be dealt with before In_xGa_{1-x}As ($0.53 \leq x \leq 1$) can be considered a viable replacement as a future channel material: i) the heterogeneous integration of In_xGa_{1-x}As on Si substrate and ii) the development of a suitable gate stack for In_xGa_{1-x}As.

1.6 Heterogeneous integration of III-V on Si.

To make III-V materials a feasible alternate channel material, its compatibility with modern VLSI processes is crucial. The most economically feasible solution today is to heterogeneously integrate these epitaxially grown materials on to Si substrate rather than developing a processing using large-diameter bulk III-V wafers. The most concerning growth issue is the large lattice mismatch (7.8%) between the larger $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Si. As a result of the large lattice mismatch, direct epitaxial growth of these high mobility materials on to Si substrate results in the relaxation of the active layer film via the formation of misfit and threading dislocations, stacking faults and micro-twins [23]. These defects impact device performance by reducing both carrier mobility and lifetime while increasing junction leakage [21]. In addition to the lattice mismatch problem, there is also a thermal mismatch issue between $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Si due to the large difference in the thermal expansion coefficients of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($5.66 \times 10^{-6}/\text{K}$) and Si ($3 \times 10^{-6}/\text{K}$) [21]. The thermal mismatch will introduce a large density of thermal mismatch induced defects which also have a detrimental impact on device performance. The design of a proper buffer architecture to bridge the epitaxial III-V layer with the Si substrate is therefore imperative for heterogeneous integration of device-quality III-V on to Si substrate. A proper buffer utilizes wide bandgap materials and is low in both threading dislocation density (TDD) as well as root-mean-square (RMS) roughness. Large bandgap materials provide for both device isolation and the suppression of parallel conduction whereas low TDD and low RMS allow for a smooth template from which to grow defect-minimal, device-quality epitaxial $\text{In}_x\text{Ga}_{1-x}\text{As}$. This introduction will focus on some common buffer architectures that have been pursued in order to heterogeneously integrate $\text{In}_x\text{Ga}_{1-x}\text{As}$ on to Si substrate including

the composite GaAs/ $\text{In}_x\text{Al}_{1-x}\text{As}$ metamorphic buffer and the III-V on insulator (III-V-OI) approach, as well as their shortcomings.

1.6.1 The composite GaAs/ $\text{In}_x\text{Al}_{1-x}\text{As}$ metamorphic buffer

Since direct growth is clearly not an option due to the large lattice mismatch, grading the lattice constant via a composite metamorphic buffer to accommodate and filter out defects that can propagate through the material stack [23, 24]. The most important figures of merit and design constraints to evaluate the performance of a composite metamorphic buffer are active QW layer mobility (μ), sheet carrier density (N_s), low defect density of the epitaxially grown active layer, requirement for a low thermal budget $< 550^\circ\text{C}$ opposed to that of Si CMOS processing which is much higher, low total buffer thickness while maintaining the buffers ability to filter out dislocations without degrading the active layer mobility, the buffer's requirement of a large bandgap to eliminate parallel conduction through its highly insulating properties (low conductivity). However, there is a trade-off between the bandgap of the buffer layer and the growth process temperature which is a limiting factor since a large bandgap requires a higher temperature to relax misfit strain. Defects in the desired $\text{In}_x\text{Ga}_{1-x}\text{As}$ active layer are a result of at least three sources: i) the polar on nonpolar III-V/Si interface, ii) large lattice constant mismatch, and iii) atomic interdiffusion across the interface. These sources generally result in poor crystalline quality of the epitaxially grown films due to the formation of i) anti-phase domains (APD), misfit and crystal defects, ii) threading dislocations, iii) stacking faults and iv) micro-twins all having adverse effects on device performance. The prevention of APD's is possible by the monolayer scale control that is made possible by using molecular beam epitaxy (MBE) for the formation of III-V/ Si interface by using an appropriate off-cut Si substrate to

provide a “virtual” polar surface on Si which hence eliminates APDs, stacking faults and micro-twins from being formed. A 4°- offcut (100) Si substrate with a GaAs nucleation layer was developed creating a polar-polar “virtual” interface eliminating APDs. Following this, the deposition of graded $\text{In}_x\text{Al}_{1-x}\text{As}$ ($0 < x < 0.52$) within an overshoot and inverse grading in between ($x: 0.52 \rightarrow 0.7 \rightarrow 0.52$) to ensure full relaxation of the buffer while minimizing buffer thickness. The full relaxation of the composite metamorphic buffer allows the growth of defect-free $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The scaling of the composite buffer from $3.2\mu\text{m}$ to $1.3\mu\text{m}$ without the loss of mobility while maintaining a low RMS roughness was demonstrated aiding the quality of the scaled thin composite metamorphic buffer to effectively filter dislocations. It was also demonstrated that for a given N_s , the mobility in the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW layer grown on silicon via the composite buffer is equivalent to those in the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW layers grown on III-V substrates such as GaAs and InP [23, 24].

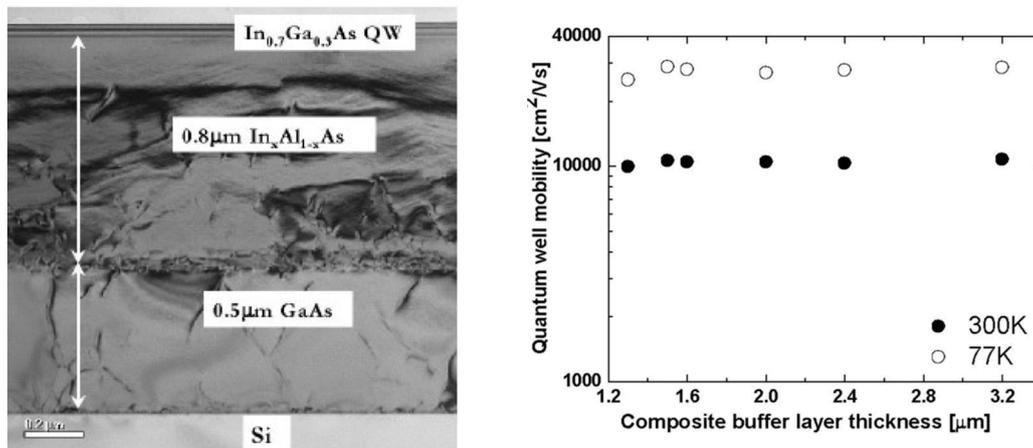


Fig. 1.8 On the left is the cross sectional TEM of the $1.3\mu\text{m}$ composite buffer showing the elimination of defects above the $\text{In}_x\text{Al}_{1-x}\text{As}$ overshoot. On the right $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW electron mobility versus composite buffer layer thickness on Si at 300K and 77K. No mobility degradation is observed, demonstrating that the metamorphic buffer architecture is effective in filtering dislocations with reduce thickness.[23, 24]

1.6.2 III-V on insulator (III-V-OI)

Through the incorporation of an oxide buffer, which is high bandgap in nature, the III-V-on-insulator (III-V-OI) approach offers a way of heterogeneously integrating III-V materials onto Si substrate with the benefits of both suppression of parallel conduction as well as effective device isolation. Furthermore, the main advantage of this route is the ability to simultaneously integrate Ge and III-V onto Si substrates for future photonics and High Performance Computing (HPC) [25, 26] instead of the employment of two separate buffer architectures. This is made possible by the utilization of Direct Wafer Bonding (DWB) [27-29].

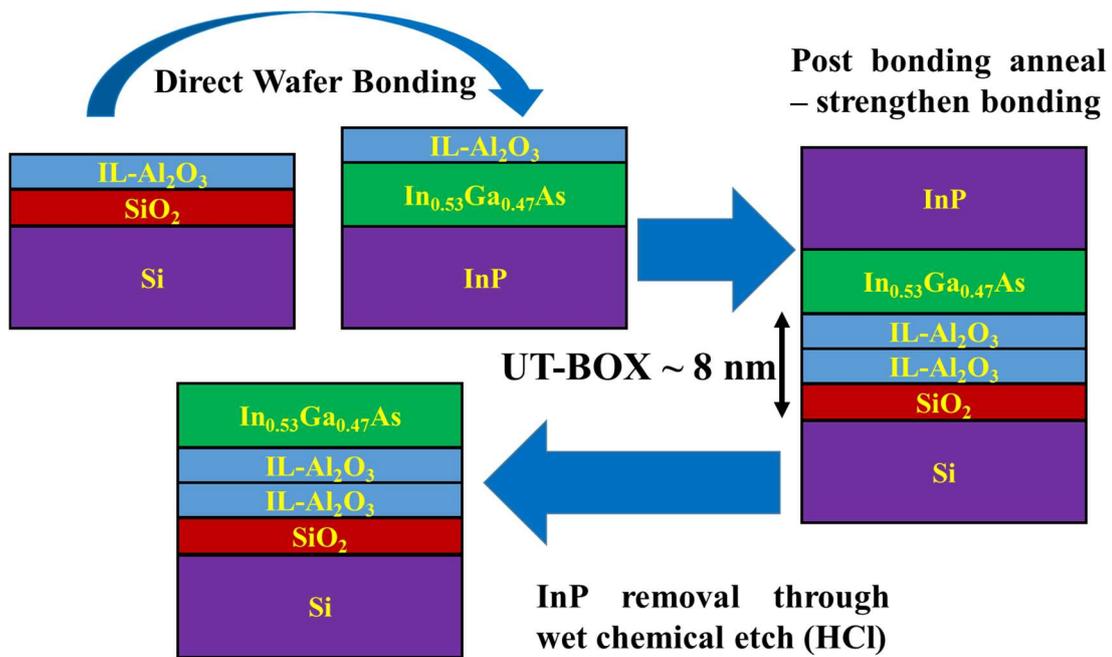


Fig. 1.9 Schematic of a simplified wafer bonding process to integrate $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ onto Si using an ultrathin $\text{Al}_2\text{O}_3/\text{SiO}_2$ Buried Oxide (UT-BOX) [25-29].

The deposition of SiO_2 with exposure to ECR plasma (Electron Cyclotron Resonance) allows for a smooth interface of very low surface *rms* (root mean square) roughness of 2\AA [28]. The superiority of the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface is utilized in this case allowing for the retention interfacial quality [30, 31]. This path has led to

the first demonstration of III-V/Ge CMOS logics on a Si wafer [27]. From a material characteristic standpoint, the III-V-OI and Ge-OI approach via bonding offers excellent surfaces for device definition. Despite the approaches ability to overcome the composite metamorphic buffer's shortcomings such as parallel conduction as well as device isolation, the major shortcoming of this approach is thermal mismatch between the III-V/Ge layer and the oxide layer. This is consequential to the fact that CMOS applications see usage in microprocessor logic, where a high thermal budget is typically induced as a result of regular computing usage. The thermal expansion coefficient of SiO₂ is $6.6 \times 10^{-7} \text{ K}^{-1}$ [32] where as that of In_{0.53}Ga_{0.47}As is $5.66 \times 10^{-6} \text{ K}^{-1}$ and for Ge is $5.9 \times 10^{-6} \text{ K}^{-1}$ [21]. The thermal expansion coefficient for Al₂O₃ is approximately $8.4 \times 10^{-6} \text{ K}^{-1}$ [33]. Despite the reduction in mismatch, the mismatch is still large, and hence it is possible for thermal defects to propagate through repeated exposure to high thermal budgets. Such defects deleteriously affect device performance.

1.7 Current technology node and the future of the transistor.

The current technology employed by the industry is the 2nd generation FinFET 14nm logic technology boasting superior electrostatic gate control over its planar counterparts, employing a 4th generation high- κ metal gate, and 6th generation strained silicon channel with enhanced mobility. The device showed off thin and tall fins ($W_{\text{FIN}}=8\text{nm}$ & $H_{\text{FIN}}=42 \text{ nm}$) driven at 0.7 V (V_{DD}). The n-FinFET boasted an extremely low sub-threshold slope (SS) $\sim 65 \text{ mV/decade}$ and DIBL $\sim 60 \text{ mV/V}$ [11]. However, the reduction in V_{DD} for future technology nodes is not possible due to the limitation of Silicon's high bandgap $\sim 1.12 \text{ eV}$. Furthermore, the limitation to the strain that can be applied to the Si material system to improve mobility and reduce supply limit is reached compared to the 22 nm 0.8 V supply voltage [10].

Despite silicon's superior short channel performance and cost efficacy, the material is near its limit as has been speculated for the past 2 decades. Hence, the industry will soon adopt alternate material channel for future technology nodes i.e., 10nm, 7nm and lower, where voltage scaling is possible ($V_{DD}=0.5V$) to reduce static power consumption and improve device performance through mobility enhancement. However, choice of high- κ dielectric is still a highly examined topic and is the basis of this work.

1.8 Thesis objectives and organization

The objective of this thesis is to understand leading alternate n-channel device architectures employing III-V materials, to further develop a model calibrated to the dimensional response of short channel effects and then project their performance for future technology nodes while understanding the dimensional requirements to optimize device performance. To achieve this, the exploration of the oxide/semiconductor properties is critical

This thesis is organized in to six chapters. *Chapter 2* presents a detailed study into leading alternate channel n-MOSFET architectures, their benefits and shortcomings and the adoption of newer systems to overcome previous shortcomings. This chapter also goes over the importance of high- κ dielectric selection and the superior interfacial and dielectric properties of the TaSiO_x/InGaAs interface compared to other high- κ dielectrics such as Al₂O₃ and HfO₂. Also, the basis of evaluating device performance is covered.

Chapter 3 is a detailed discussion of the development of the simulation model, material system band alignment and accommodation of quantum effects. The chapter also covers the methodology behind the objectives of the simulation and the

development of a material parameter library for the active layer and oxide. A theoretical D_{it} distribution is established for the $TaSiO_x/In_{0.53}Ga_{0.47}As$ interface with matched C-V and I_D-V_G characteristics and calibration of dimension variation to short channel effects to explain the model's simulation accuracy.

Chapter 4 is an insight on the dimensional influence (L_G/W_{FIN} and aspect ratio) of the Fin structure on short channel effects (DIBL & SS) and other device characteristics such as transconductance (G_m), I_{ON}/I_{OFF} ratio, static leakage (I_{OFF}), etc. The results of the scaled model to predict device performance of the 10nm node are also discussed.

Chapter 5 is a discussion of the ALD deposition process explaining the incorporation of SiO_2 into Ta_2O_5 to obtain $TaSiO_x$. Experimental results including the orientation dependant band alignment studies of $TaSiO_x/InGaAs$ are discussed along with resulting oxide quality and chemical composition.

Lastly, **Chapter 6** summarizes the conclusions of this work and presents the prospects for future avenues of research and investigation based upon this thesis' current findings.

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Chapter 2 – Leading alternate channel n-MOSFET architectures

2.1 Planar $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW FET with TaSiO_x high- κ gate dielectric

The first successful integration of $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW FET on Si with a thin ($1.3\mu\text{m}$) buffer posed one main problem, gate leakage (J_G) from the implementation of a Schottky gate far away from the channel [1], the next step was the development of a gate stack that could address the requirements of low gate leakage, the implementation of a thin gate oxide with superior electrostatic properties and strong carrier confinement with high effective carrier velocity within the QW layer. An advanced high- κ gate stack was developed implementing tantalum silicate (TaSiO_x) as the gate oxide demonstrating superior gate electrostatics over Al_2O_3 [2]. Figure 2.1 shows the improvement in gate capacitance with 40\AA (physical thickness) TaSiO_x and Al_2O_3 oxides deposited on InP.

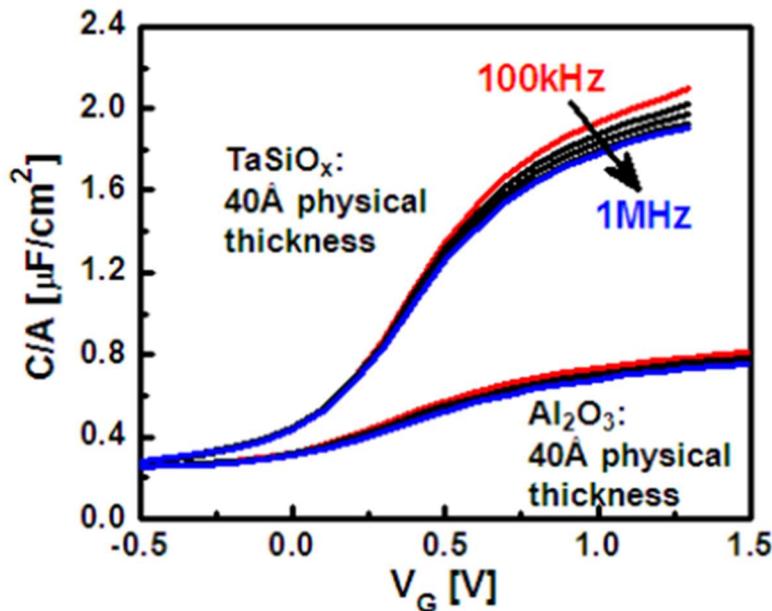


Fig. 2.1 Gate capacitance (C/A) versus gate bias (V_G) for 40\AA TaSiO_x & Al_2O_3 dielectrics on InP. TaSiO_x shows a higher accumulation capacitance over Al_2O_3 as a result of its higher dielectric constant (ϵ). Both structures show similar frequency dispersion (7%/decade) [2] Copyright © 2009, IEEE

In order to retain the high carrier mobility of the QWFET, the high- κ gate dielectric is deposited on the upper barrier rather than directly depositing it on the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW layer. The selection of InP as the upper barrier correlated to the reduction in frequency dispersion when switching from $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ (27%/decade) to InP (7%/decade) [2] suggesting that InP is a more suitable upper barrier material for high- κ dielectric integration. The resulting structure is shown Fig. 2.2 where the InP (2nm)/ TaSiO_x (4nm) gate stack is implemented with a Si δ -doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ upper barrier layer. The requirement for the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer in this case is pronounced to address the un-gated area between the channel and the source & drain. This depletion of carriers can cause the region to act highly resistive [3] which is undesirable. Hence, the introduction of δ -doping which ‘*un-depletes*’ this area acting as a carrier supply eliminates this problem.

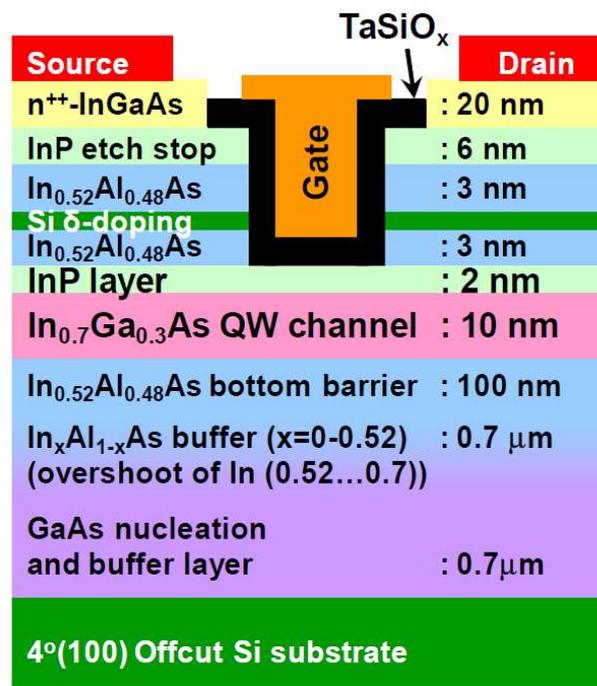


Fig 2.2 Schematic of $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QWFET on silicon with 2nm InP upper barrier layer and a 4nm TaSiO_x high-K gate dielectric, which form a composite TaSiO_x -InP gate stack. Copyright © 2009, IEEE

Furthermore, since the growth is metamorphic and a high surface rms roughness between 30-39Å is observed posing a processing issue due to the low thickness of the InP layer on top of the In_{0.7}Ga_{0.3}As QW layer [1]. The InP/TaSiO_x with 22 Å EOT composite gate stack shows superior C-V characteristics compared to the previously employed Schottky gate [1, 2] and reduction in gate leakage current (J_G) by 3 orders - as can be seen in Fig 2.3 (a) and (b).

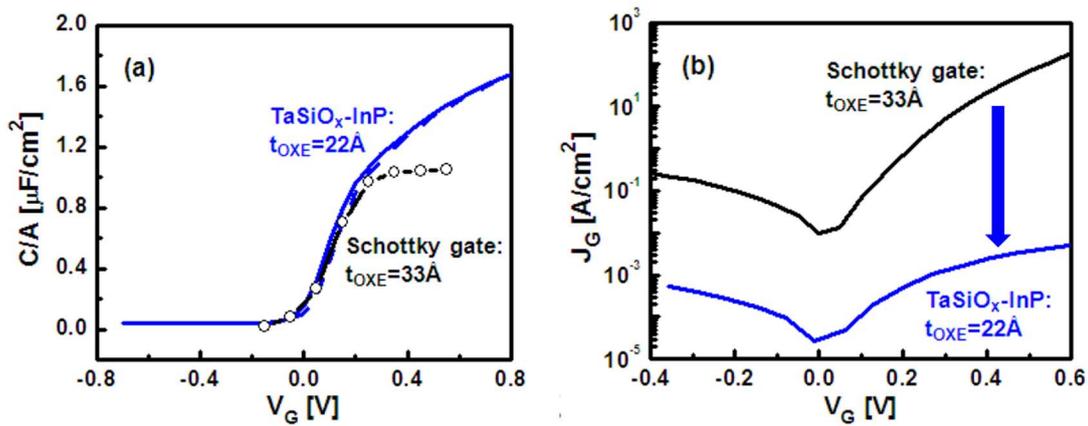


Fig. 2.3 (a) C- V_G measured on the In_{0.7}Ga_{0.3}As QWFET with the composite 4nm TaSiO_x-2nm InP gate stack showing minimal hysteresis. Included is C- V_G of the Schottky-gate QWFET with barrier layer $t_{\text{InAlAs}}=5\text{nm}$. **(b)** J_G versus V_G of In_{0.7}Ga_{0.3}As QWFET with the same composite gate stack and Schottky gate electrode as Fig. 2.3 (a) showing a 3 order (1000x) reduction in gate leakage [1, 2]. Copyright © 2009, IEEE

The resulting planar QWFET with gate length $L_G=75\text{nm}$ transfer characteristics ($I_D - V_G$) is shown in Fig. 2.4. The device demonstrated a DIBL $\sim 120\text{mV}/\text{V}$ and an SS $\sim 95\text{mV}/\text{decade}$. The extraction of short channel effects will be discussed further in section 2.5. The device also exhibited a 3.5x increase in effective carrier velocity (V_{eff}) over their strained Si MOSFET counter parts at a given DIBL for a gate over drive ($V_{\text{GS}}-V_{\text{T}}=0.3\text{V}$) at $V_{\text{DS}}=0.5\text{V}$ [4]. A peak $G_m\sim 1750 \mu\text{S}/\mu\text{m}$ and the low

SS~95mV/decade were the lowest reported compared to other III-V planar transistors with high- κ dielectrics in literature [5-7].

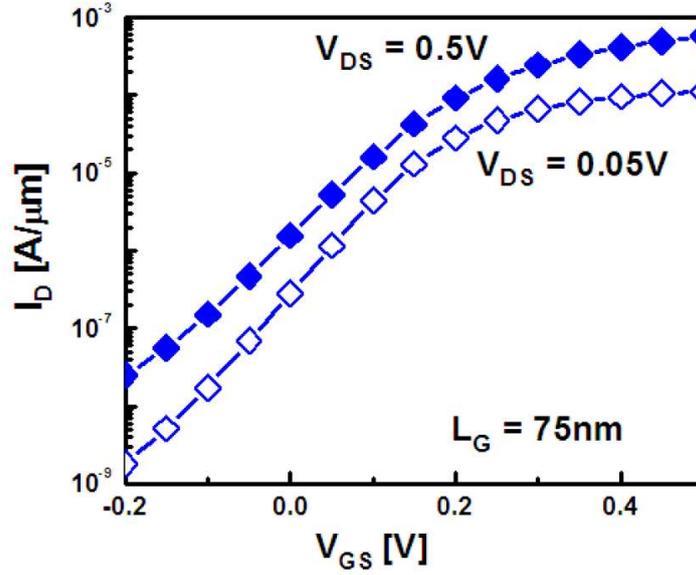


Fig. 2.4 Transfer characteristics (I_D - V_G) of the 75nm L_G planar $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QWFET with composite 4nm TaSiO_x -2nm InP gate stack. The device demonstrated a drive current $I_D \sim 0.49\text{mA}/\mu\text{m}$ at $V_{GS}=V_{DS}=0.5\text{V}$ and $I_{OFF} \sim 1.5\mu\text{A}/\mu\text{m}$ at $V_{GS}=0\text{V}$ [2].

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2.2 Non-Planar, Tri-gate InGaAs FET with TaSiO_x high- κ gate dielectric employing simplified raised S/D scheme.

The first demonstration of the planar $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QWFET with the composite TaSiO_x - InP gate stack brought an insight on superior interfacial properties and device characteristics such as transconductance (G_m), the multiple issues in the large un-gated area of the channel requiring the employment of the high bandgap Si δ -doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer to act as a carrier still brought about high resistance and was also the main contributor to total resistance due to the layers high bandgap. This lead to the implementation of a simplified and highly scaled raised Source/Drain scheme with a 5nm gate-source and gate-drain separation (L_{SIDE}) [8]. This lead to the development of

an intrinsic planar and non-planar QWFET with the improved scheme with resulting structures shown in Fig 2.5.

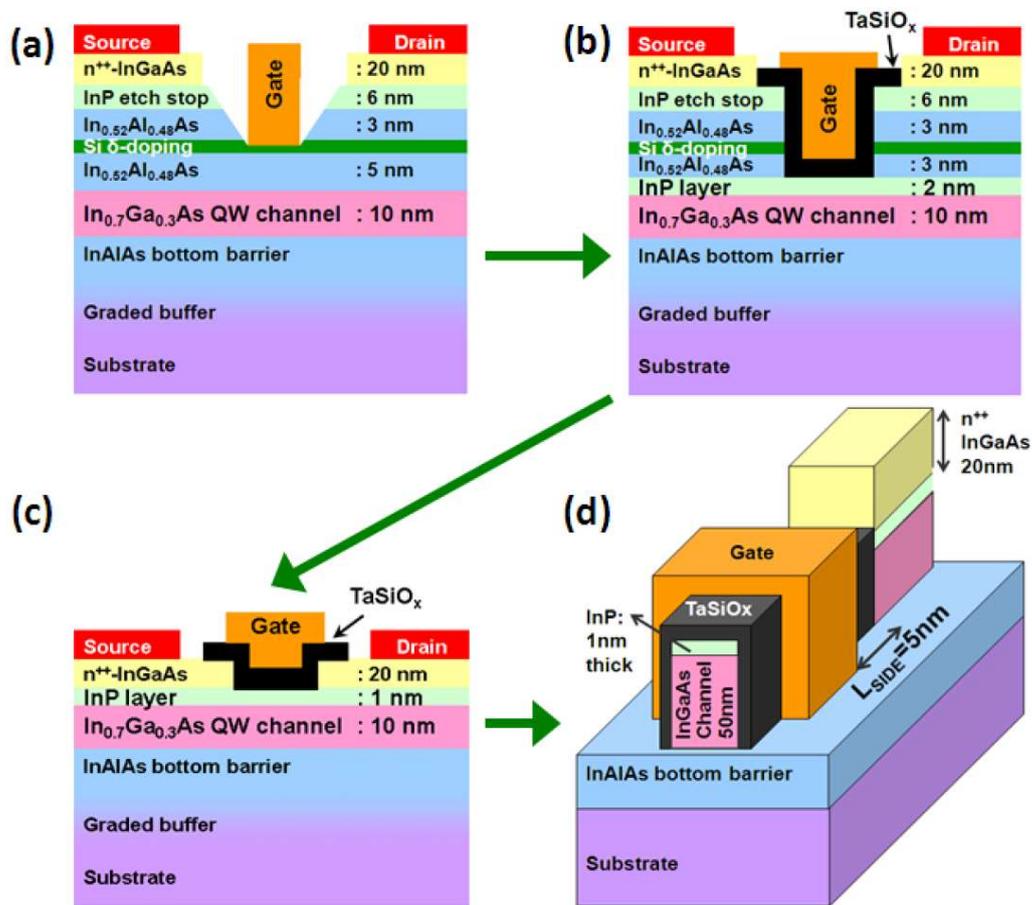


Fig. 2.5 Evolution of InGaAs QWFET from planar to non-planar, multi-gate architecture: (a) Planar Schottky gate QWFET with source/drain comprised of n^{++} InGaAs cap, thick upper barriers and Si δ -doping [1]. (b) Planar QWFET structure similar to (a) except the Schottky gate is replaced by high- κ /metal gate stack [2]. (c) Planar high-K QWFET similar to (b) except the thick upper barriers and Si δ -doping are removed in the S/D area [8]. (d) Non-planar, multi-gate high-K QWFET, with the transistor channel being in the shape of a “fin”, and ultra-scaled drain-gate and source-gate separations (L_{SIDE}) [8]. Eliminating the thick upper barriers and Si δ -doping in (c) and (d) while using n^{++} InGaAs cap as the carrier supply enables S/D contact area scaling with low resistance [9]. Copyright © 2010, IEEE

The overall resistance could be evaluated as:

$$R = 2(R_C + R_B) + R_{QW}, \quad (2.1)$$

where R_C is the contact resistance of n^{++} InGaAs contact resistance, R_B is the InAlAs barrier resistance of the S/D and channel, and R_{QW} is the resistance of the active InGaAs QW layer.

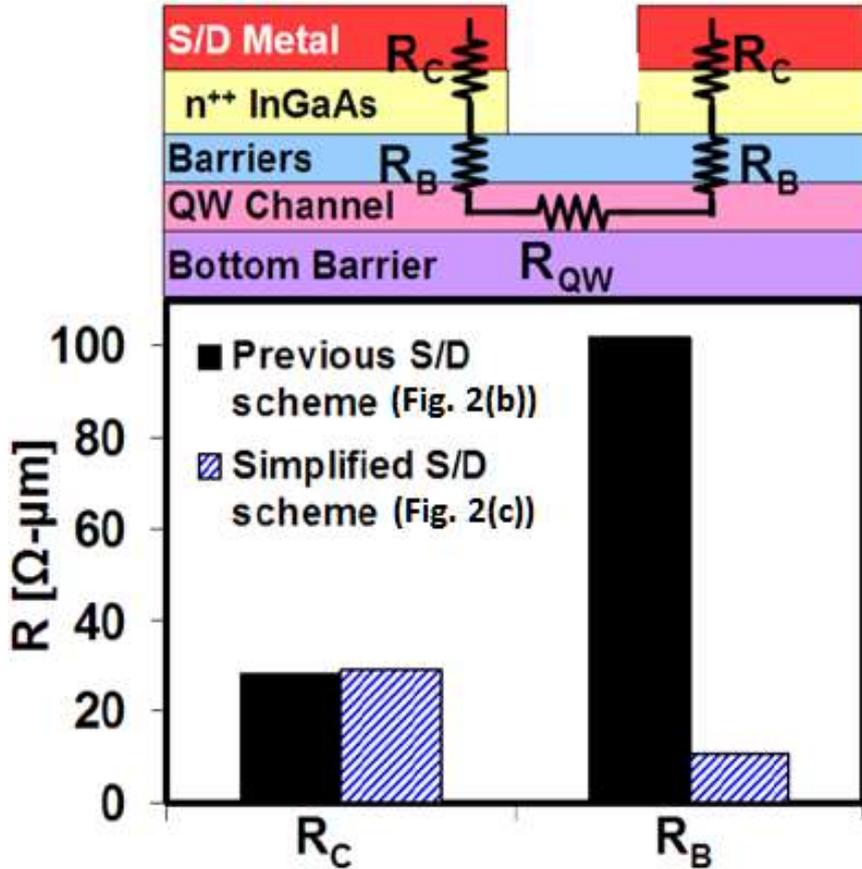


Fig. 2.6 Transfer length method (TLM) measurements show simplified raised S/D scheme in this work (Fig. 2.5(c)) achieves 90% reduction in barrier resistance (R_B) over previous scheme (Fig. 2.5(b)), while n^{++} cap contact resistance (R_C) remains identical as expected [2, 8, 9]. Copyright © 2010, IEEE

The reduction in barrier resistance in these structures was evaluated using the transfer length method showing a 90% reduction in barrier resistance as can be shown in Fig. 2.6 [1, 2, 8].

With the elimination of the thick upper barrier it was found that no degradation was observed in C-V and G_m -V characteristics indicating that the removal of the Si δ -doped layer does not affect device performance, in fact enabling S/D area scaling with low resistance [9]. This facilitated the fabrication of the non-planar multi-gate architecture shown in Fig. 2.5(d). The resulting fin structure exhibited superior C-V characteristics over its planar counterparts with further improvement with reducing fin width [8]. Furthermore, both planar and non-planar devices utilized a thin InP layer on the top (100) surface during the 2x reduction of D_{it} to $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ as compared to InGaAs [8]. The resulting wide-fin non-planar device of gate length $L_G=70\text{nm}$, and fin dimensions $W_{FIN}=60\text{nm}$, $H_{FIN}=50\text{nm}$ with scaled gate-source/gate-drain separation $L_{SIDE}=5\text{nm}$ and $T_{OXE} \sim 20.5 \text{ \AA}$ had transfer characteristics shown in Fig. 2.7.

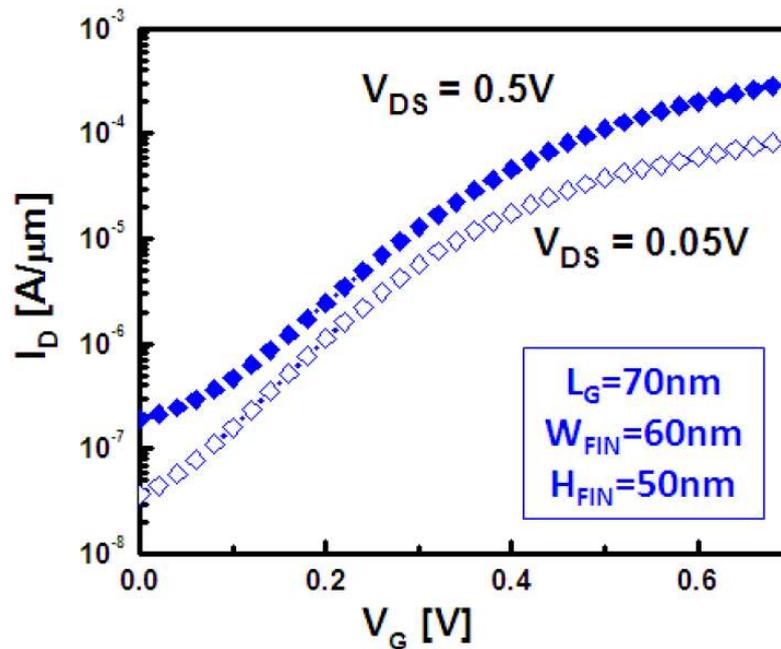


Fig. 2.7 Transfer characteristics of $L_G=70\text{nm}$ non-planar, multi-gate InGaAs QWFET with $W_{FIN}=60\text{nm}$ and $H_{FIN}=50\text{nm}$ $T_{OXE}=20.5 \text{ \AA}$ and $L_{SIDE}=5\text{nm}$ [8].

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The device exhibited a DIBL~111mV/V and an SS~122mV/decade and a drive current $I_D \sim 0.45\text{mA}/\mu\text{m}$ and reduced $I_{OFF} \sim 200\text{nA}/\mu\text{m}$, outperforming planar devices (InGaAs $T_{QW}=50\text{nm}$) in terms of short channel effects for a given gate length (320mV/V & 190mV/decade) as can be seen in Fig. 2.8 (a) and (b) [8, 10].

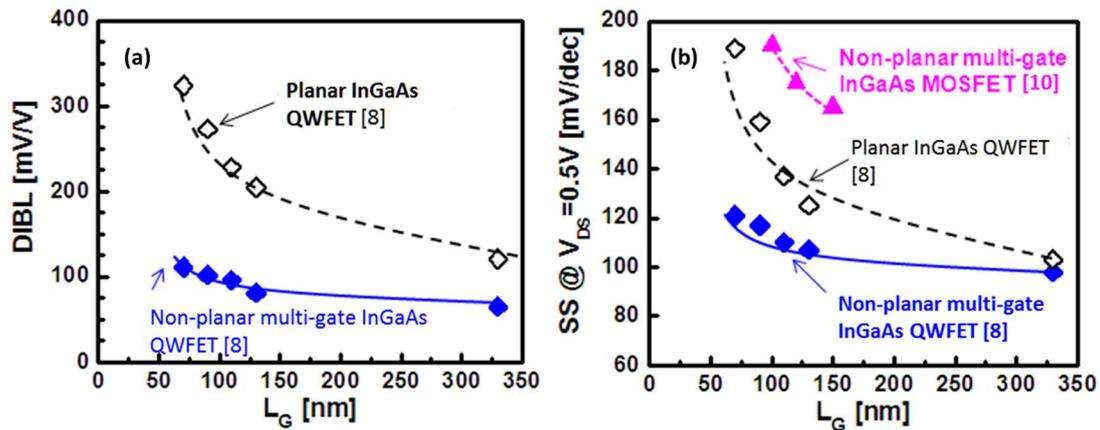


Fig. 2.8 (a) Drain induced barrier lowering (DIBL) versus L_G comparing the planar device (InGaAs QW thickness of 50nm) and non-planar, multi-gate QWFET device with $W_{FIN}=60\text{nm}$ and $H_{FIN}=50\text{nm}$. Comparing to the planar device, the non-planar device shows significant improvement in DIBL due to improved electrostatics [8].

(b) SS versus L_G comparing the planar device (InGaAs $T_{QW}=50\text{nm}$) and non-planar, multi-gate QWFET device with $W_{FIN}=60\text{nm}$ and $H_{FIN}=50\text{nm}$. The devices have $T_{OXE} \sim 21\text{\AA}$ and ultra-scaled $L_{SIDE}=5\text{nm}$ [8]. Comparing to the planar device, the non-planar device shows significant improvement in SS due to improved electrostatics. Included is the most recent non-planar, multi-gate InGaAs MOSFET device from [10]. © 2010, IEEE

The non-planar InGaAs QWFET with TaSiO_x is shown to outperform other non-planar devices showing the superior electrostatic benefits of TaSiO_x as gate dielectric with potential of scalability to improve gate electrostatics to counter short channel effects.

2.3 Non-Planar, 3-D Tri-gate InGaAs FET with low EOT TaSiO_x high-κ gate dielectric employing simplified raised S/D scheme.

Following the demonstration of the first non-planar Tri-gate FET with TaSiO_x high-κ dielectric, the requirement for improved electrostatics drove the TaSiO_x gate dielectric layer to be scaled further to demonstrate an equivalent oxide thickness, EOT=12Å while maintaining similar gate leakage characteristics (J_G) to exhibit superior short channel effects over a planar ultra-thin body InGaAs FET (T_{QW} =10nm), Fig. 2.9 [11]. The comparison is made to evaluate gate control and its impact on short channel effects between the two architectures. Furthermore, all reported III-V Tri-gate devices reported at the time had degraded dielectric quality and/or wide fin structures [8, 10].

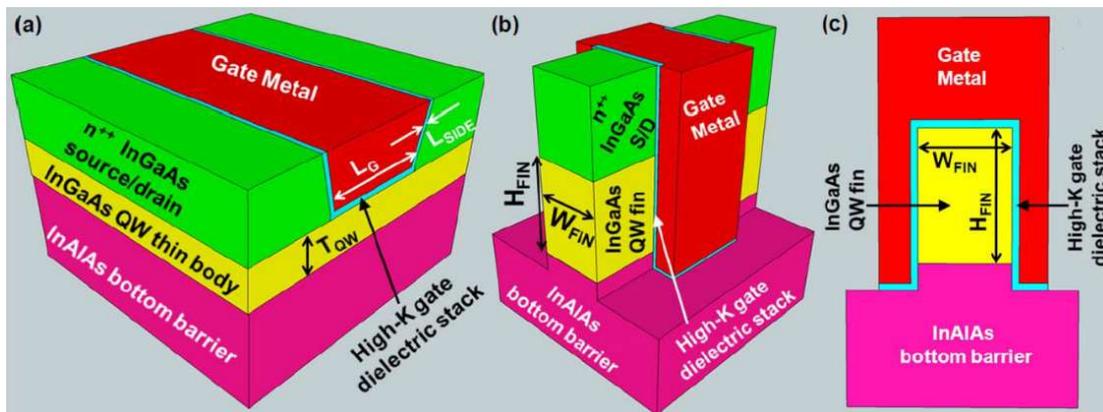


Fig. 2.9 InGaAs QWFET structures compared in [11] for electrostatics: (a) Thin-body planar InGaAs QWFET with high-K dielectric gate stack, scaled gate-to-source/gate-to-drain (L_{SIDE}) of 5nm, and body thickness (T_{QW}) ranging from 10nm to 50nm. (b) 3-D Tri-gate InGaAs QWFET with recessed gate and scaled high-κ dielectric gate stack (EOT=12Å), scaled L_{SIDE} =5nm, fin width (W_{FIN}) ranging from 30nm to 60nm, and fin height (H_{FIN}) ranging from 30nm to 50nm. (c) Cross-section of 3-D Tri-gate structure shown in Fig. 2.8 (b) [11]. Copyright © 2011, IEEE

It is important to note that to achieve Tri-gate transistors with tall H_{FIN} , the InGaAs QW must be lattice matched to the bottom barrier, $In_{0.52}Al_{0.48}As$, used in this work. This limits indium content of the QW to 53% ($In_{0.53}Ga_{0.47}As$) which has reduced mobility and increased m^* compared to higher indium content ($In_{0.7}Ga_{0.3}As$) thin body planar QWFETs [2, 8, 10, 11]. Both device structures in are grown by MBE. The requirement for narrow fins made the use of InP as an interfacial layer between the dielectric and the channel to reduce D_{it} redundant. The resulting C-V and transfer characteristics are shown in Fig. 2.10 (a) and (b). The 3-D Tri-gate device in Fig. 2.10 (b) shown had fin dimension $L_G=60nm$, $W_{FIN}=40nm$ and $H_{FIN}=40nm$ while the planar UTB planar InGaAs had $T_{QW}=40nm$. Both device demonstrated a highly scaled $EOT=12\text{\AA}$ [11]. These transfer characteristics are the shortest reported gate length with $TaSiO_x$ gate dielectric to evaluate short channel effects, and hence the data from this paper is used to develop the model in this work.

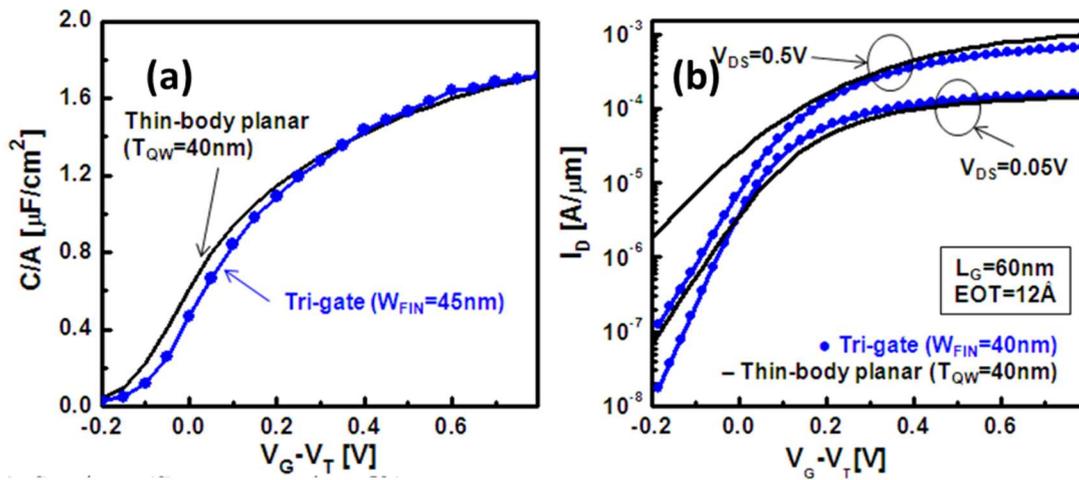


Fig. 2.10 (a) C- V_G characteristics of the 3-D Tri-gate and UTB-planar structure. (b) Transfer characteristics (I_D - V_G) of both structures having $L_G=60nm$. The Tri-gate architecture is shown to outperform the planar-UTB with steeper SS and lower DIBL due to improved electrostatics [11]. Copyright © 2011, IEEE

Furthermore, long channel transfer characteristics ($L_G=20\mu\text{m}$) with $W_{\text{FIN}}=45\text{nm}$ and $T_{\text{QW}}=40\text{nm}$ indicated the superior interfacial quality of the (110) sidewall interface. The long channel devices showed similar $SS\sim 60\text{mV/decade}$ with the tri-gate architecture having slightly higher drive current (I_{ON}) [11]. This indicated the superior quality of (110) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ to the high- κ interface on the fin sidewalls of the tri-gate devices [11]. The Tri-gate devices with W_{FIN} varying from 60nm to 30nm demonstrated short channel effects for L_G varying between 60nm and 325nm as shown in Fig. 2.11 (a) and (b).

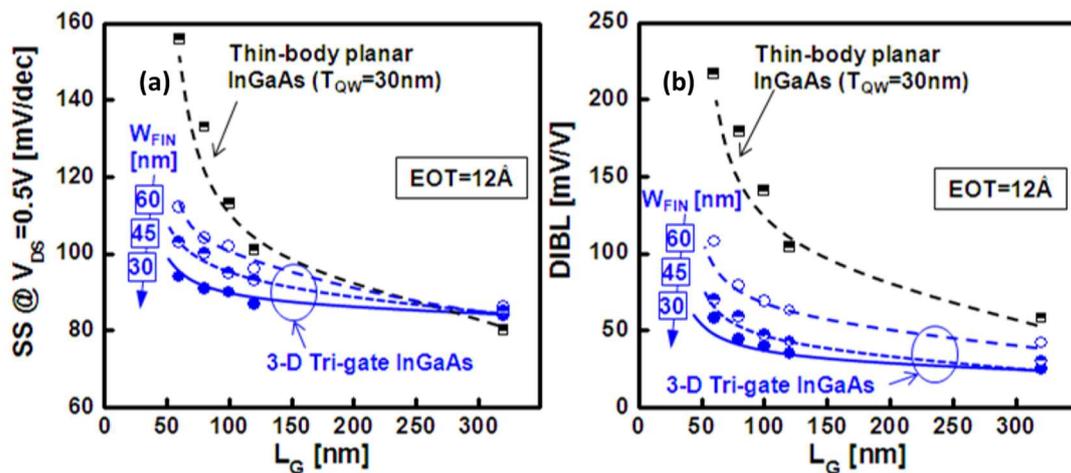


Fig. 2.11 (a) SS vs. L_G and (b) DIBL vs. L_G comparing planar thin-body devices ($T_{\text{QW}}=30\text{nm}$) and 3-D Tri-gate QWFET with $W_{\text{FIN}}=60\text{nm}$, 45nm and 30nm. All devices have same $\text{EOT}=12\text{\AA}$. The Tri-gate architecture shows significant improvement over thin-body planar devices which becomes more pronounced at shorter gate lengths [11]. Copyright © 2011, IEEE

The Tri-gate architecture ($W_{\text{FIN}}=30\text{nm}$) had also shown to outperform short channel electrostatics of the ultra-thin body planar QWFET ($T_{\text{QW}}=10\text{nm}$) and other reported non-planar III-V devices in literature [8, 10, 11], Fig. 2.12 (a) and (b).

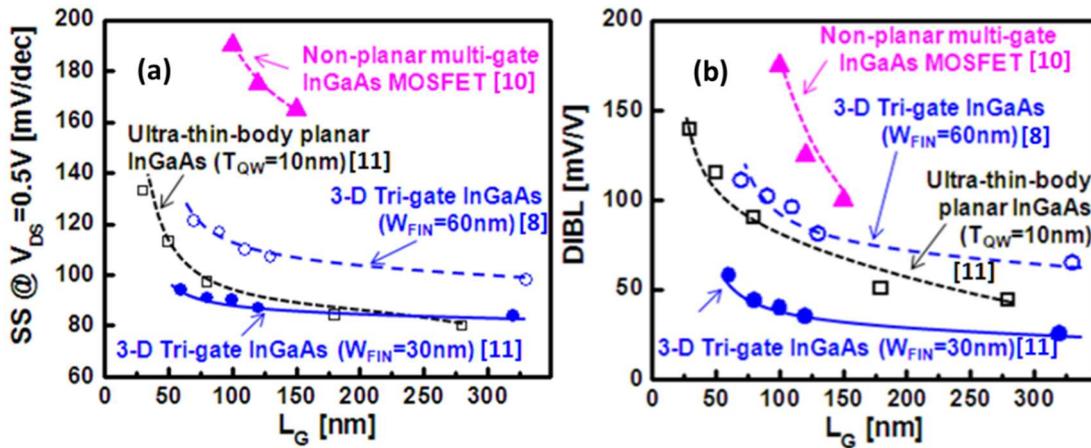


Fig. 2.12 (a) SS vs. L_G and (b) DIBL vs. L_G comparing the ultra-thin body planar device ($T_{QW}=10\text{nm}$) and 3-D Tri-gate QWFET device ($W_{FIN}=30\text{nm}$) with same $EOT=12\text{\AA}$. The Tri-gate devices are shown to achieve the steepest sub-threshold swing and smallest DIBL ever reported for any high- κ III-V FET [8, 10, 11].

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Since this is the shortest channel demonstrated with scaled TaSiO_x as high- κ dielectric ($EOT=12\text{\AA}$), the data reported in figures 2.9 and 2.10 will be used to calibrate the simulation model to the dimensional influence of the fin structure on short channel effects. A comparison of the evolution of this device's architecture is shown in Table 2.1.

	L_G (nm)	DIBL (mV/V)	SS (mV/decade)	I_{ON} (mA/ μm)	I_{OFF} (nA/ μm)
[2] Planar (70% Indium)	75	~120	~95	~0.49	~1500
[8] Tri-gate (1st generation)	70	~111	~122	~0.1	~200
[11] Tri-gate scaled oxide (2nd generation)	60	~65	~95	~0.2	~120

Table 2.1 Compilation of device characteristics of various transistor architectures employing $\text{TaSiO}_x/\text{InGaAs}$ system.

2.4 Evaluation of short-channel effects

The overwhelming progress made in the research of novel nanoelectronic devices such as Si nanowire FETs, III-V non-planar FETs, CNTs (Carbon Nanotubes) etc. require a systematic approach to benchmark these technologies against each other. This section deals with the evaluation of short-channel effects to benchmark device performance.

The operation voltage (V_{CC}) of the device is equal to the drain-to-source bias (V_{DS}) = 0.5V [12]. The threshold voltage (V_T) is selected at specified current $I_{DS}=1\mu A/\mu m$ [13, 14]. Approximately $1/3^{rd}$ of the gate voltage swing ($V_{GS}=V_{CC}$) below V_T is used to obtain the OFF-state current, I_{OFF} and $2/3^{rd}$ gate voltage (V_{GS}) overdrive provides the ON-state current, I_{ON} [12]:

$$I_{ON} = I_D \text{ at } V_{GS} = V_T + \frac{2}{3}V_{CC}, \quad (2.1)$$

$$I_{OFF} = I_D \text{ at } V_{GS} = V_T - \frac{1}{3}V_{CC} \quad (2.2)$$

Short channel effects such as DIBL are evaluated as the shift in V_T at $1\mu A/\mu m$ with change in V_{DS} bias between 0.05V and 0.5V.

$$DIBL = \frac{V_T(V_{DS} = V_{CC}) - V_T(V_{DS} = 0.05V)}{V_{CC} - 0.05V} \quad (2.3)$$

Sub-threshold slope (SS) is calculated over the region of operation (V_{CC}).

$$SS = \frac{\Delta V_{GS}}{n/\text{decades } I_D} \quad (2.4)$$

An example is shown in Figure. 2.13 extracting multiple device characteristics for low power operation and short channel effects.

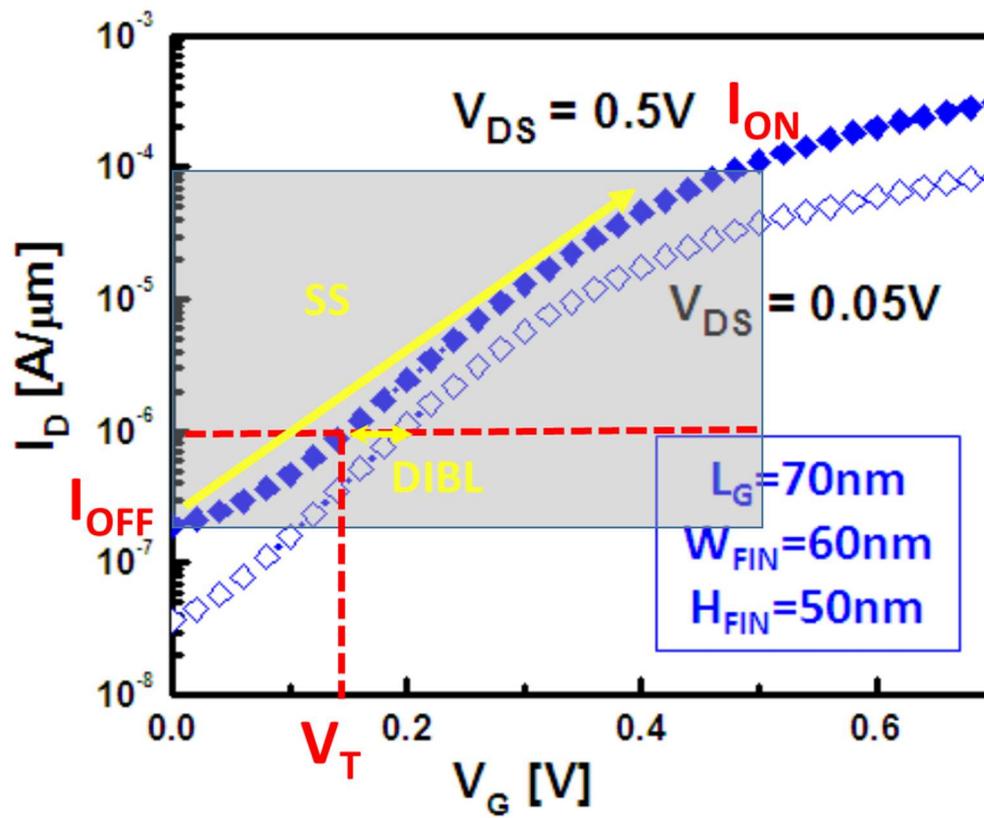


Fig. 2.13 An example of the extraction of device characteristics to evaluate short channel effects: SS and DIBL. Copyright © 2010, IEEE

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Chapter 3 – Simulation model development

3.1 Simulation methodology

The scaling of fin dimensions below 15 nm pronounces quantization effects requiring a model to appropriately calculate carrier density in quantized states. The calibration of the simulation model must account for quantization effects which makes short channel effects more sensitive to device scaling. Furthermore, it has been shown that the sensitivity of ΔV_T increases below 15nm due to the amplification of quantization effects with deviation from the classical model [1]. The model developed in this work aims to calibrate the response of the device's short channel effects to dimensional variation of the fin structure. The deviation of V_T roll-off in this case is critical as it can be underestimated in the classical model [1]. Fin structure also plays a very crucial role with trapezoidal fins providing the ability to obtain high yield density by reducing sidewall angle at the cost of electrostatic control [1].

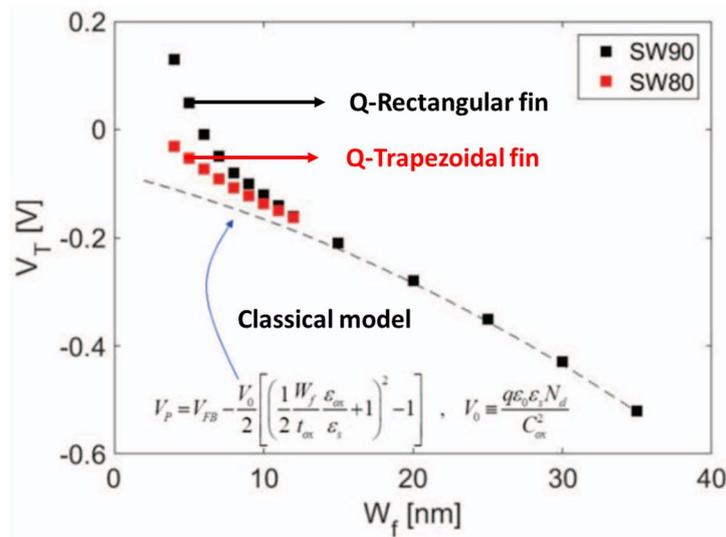


Fig. 3.1 V_T variation as a function of fin width (W_{FIN}) for rectangular and trapezoidal fins (SW90 and SW80) compared to calculations made using a classical model [1]. The deviation between the quantum and classical model is pronounced below 15nm.

The device structures simulated in this work take present day lithographic limitations into account with calibration to short-channel data presented for devices utilizing TaSiO_x as high- κ dielectric [2-4] and hence predict short channel device performance using TCAD's self-consistent Schrödinger-Poisson solver coupled with the modified local density approximation (MLDA) quantization model [5, 6] to apply appropriate quantum corrects and hence predict short channel effects for short channel thin fin structures. In the next few sections, we will discuss the physics model which are included in the simulation, the device structure and calibration.

3.2 Sentaurus TCAD device simulator

Sentaurus is a numerical simulator which simulates the electrical behaviour of semiconductor devices numerically. Device simulations can be thought as a virtual measurements of electrical behaviour of a semiconductor device, such as a transistor or a diode. The device can be represented as a meshed finite-elemental structure. Each node of the device has its own properties associated with it, such as material type (and hence bandgap, permittivity, effective mass, etc.) and doping concentration. Each node has several parameters calculated as required such as, electric field, generation and recombination rates, carrier concentration etc. Sentaurus device simulator can be used to simulate the electrical, thermal and optical characteristics of semiconductor devices with the ability to handle 1D, 2D and 3D geometries containing a comprehensive set of physical models that can be applied to all relevant semiconductor devices and operation conditions. Adding to this, the vast material database allows accurate simulations of heterostructures with the users input of relevant material parameters based on literature with relevance to the design of the simulation. A material wise physics section allows

for this while including material specific library files containing important parameters like carrier lifetime, average thermal velocity, trap time constant, etc. These parameters coupled with multiple physical models to account for physical phenomenon, both classical and quantum, provide accurate simulations of devices. After defining the device structure and the physics model, the simulator will solve the Poisson and carrier continuity equations by using discretization at each grid point of the mesh which is defined in the structure and get the numerical solution, these solutions can be displayed by post processing with the aid of other tools such as Sentaurus Visual for example, all of which are available in a GUI platform called Sentaurus Workbench.

The solutions to designed simulations are obtained by Sentaurus Device's non-linear Newtonian solver which simultaneously solves Poisson's and the carrier continuity equations to produce a converged unique solution. Fig. 3.5 is a flowchart of the simulation setup for the Sentaurus Device simulator.

Meshing is a very critical process during the development of the simulation model. Unnecessary mesh points can drastically increase computation time and even lead the non-linear Newton solver to not converge. Appropriate meshing must be applied to heterostructures interfaces, oxide/channel interfaces, and carrier injection areas. Once an appropriate meshing structure is established, mesh points must be reduced to improve computing efficiency without losing device behaviour.

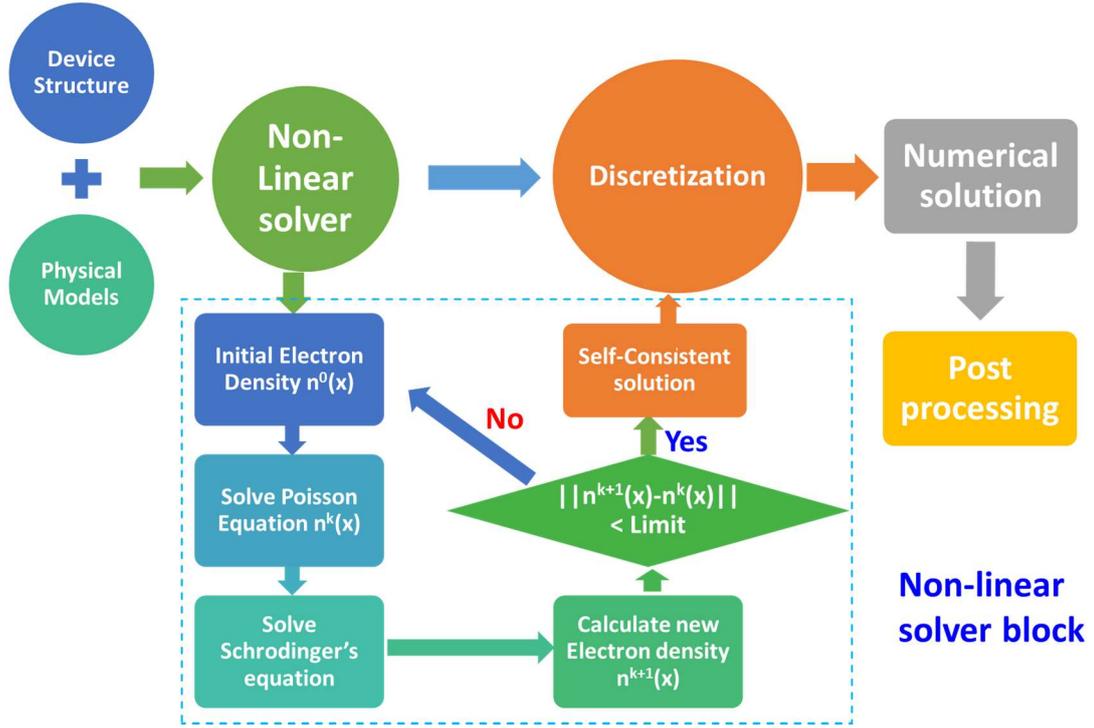


Fig 3.2 Flow chart of Sentaurus Device simulation setup.

3.3 The MLDA quantization model

The MLDA model [5, 6] describes a multiple-electron system in a constant potential as a function of a spatially varying perturbation while accounting for quantum mechanical reflection (of the wave function) from an attractive potential, a phenomenon due to which the local density of states at the insulator/semiconductor interface shows oscillations and reduces to a null value [5, 6]. This holds significant importance for the modeling of Tri-gate transistors, given the narrow fin structure, in order to accurately describe the superior gate electrostatic control observed in Tri-gate field effect transistors.

The confined electron density under Fermi statistics is given by [5-8]:

$$n_{MLDA}(\mathbf{r}, \varepsilon_F) = \int_{E_c(\mathbf{r})}^{\infty} D(\varepsilon, \mathbf{r}) f(\varepsilon, \varepsilon_F) d\varepsilon \quad (3.1)$$

where $f(\varepsilon, \varepsilon_F)$ describes the Fermi-Dirac statistics is given by:

$$f(\varepsilon, \varepsilon_F) = \frac{1}{1 + \exp\left(\frac{\varepsilon - \varepsilon_F}{K_B T}\right)} \quad (3.2)$$

and $D(\varepsilon, \mathbf{r})$ is the local Density of states accounting for band non-parabolicity. Since we are dealing with a non-parabolic ellipsoidal band, the dispersion relation can be expressed as [7, 8]:

$$\varepsilon(1 + \alpha\varepsilon) = \sum_j \frac{\hbar^2 k_j^2}{2m_j} \quad (3.3)$$

where ε is the energy, α is the band non-parabolicity, k_j are the components of \mathbf{k} -vector of the ellipsoidal band, and m_j are effective masses along the principal axis. With this, the local DOS can be expressed as [7, 8]:

$$D(\varepsilon, \mathbf{r}) = \frac{\sqrt{2m_1 m_2 m_3}}{\hbar^3 \pi^2} (1 + 2\alpha\varepsilon) \sqrt{\varepsilon(1 + \alpha\varepsilon)} \left[1 - j_0 \left(2x \sqrt{\frac{2m_x}{\hbar^2} \varepsilon(1 + \alpha\varepsilon)} \right) \right] \quad (3.4)$$

where m_1 , m_2 and m_3 are ellipsoidal effective masses along principal axes and j_0 is the 0th-order spherical Bessel function (Fig. 3.3) and x is the distance from the interface.

The spherical Bessel function can also be represented using Rayleigh's formula as [9]:

$$j_n(x) = (-x)^n \left(\frac{1}{x} \frac{d}{dx} \right)^n \frac{\sin(x)}{x} \quad (3.5)$$

Making the 0th-order Bessel function of the form as in Eq. 3.5 which is also viewed as the un-normalized sinc function.

$$j_0(x) = \frac{\sin(x)}{x} \quad (3.6)$$

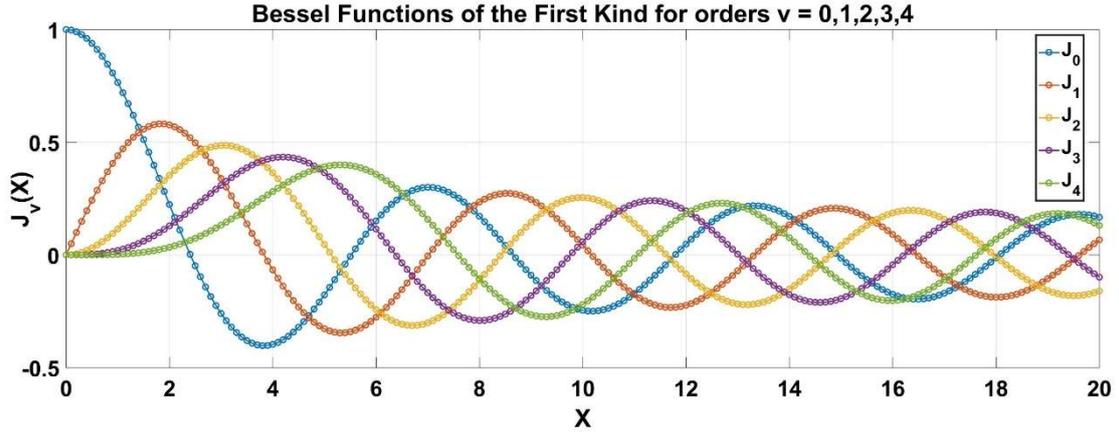


Fig. 3.3 Plot of the multiple orders of the Bessel function of the first kind generated in MATLAB.

This correlates to the direct application of the Dirichlet boundary condition (applicable to ordinary and partial differential equations to obtain solutions along the boundary of a domain) requiring $j_0(Tk)=0$ at the interface which in turn that $Tk=2\pi n$ [7].

Therefore, we employ the MLDA model to all simulations in this work [5-8]. Extensive work has been devoted to improving the MLDA model to account for the quantization effects in Double-gate and Tri-gate structures accounting for multiple semiconductor/insulator interfaces applicable to non-parabolic multi-valley (III-V) band structures [7, 8].

Furthermore, the quantum correction for carrier confinement in a QW shifts the carrier density centroid away from the interface by an additional spacing (t_{cen}) owing to the lack of carrier states. This can be observed in Fig 3.4 resulting in the capacitance model shown in the inset of the figure. Consequently, the effective gate coupling will reduce in the form while accounting for spacing [10, 11]:

$$\frac{1}{C_{ox'}} = \frac{1}{C_{ox}} + \frac{1}{C_{cent}} = \frac{t_{ox}}{\epsilon_o \epsilon_{ox}} + \frac{t_{cen}}{\epsilon_o \epsilon_{ch}} \quad (3.7)$$

where, ϵ_{ch} is the dielectric constant of the alternate channel and C_{cent} is the centroid capacitance and is a function of the potential of the QW ($\Psi_{s,QW}$).

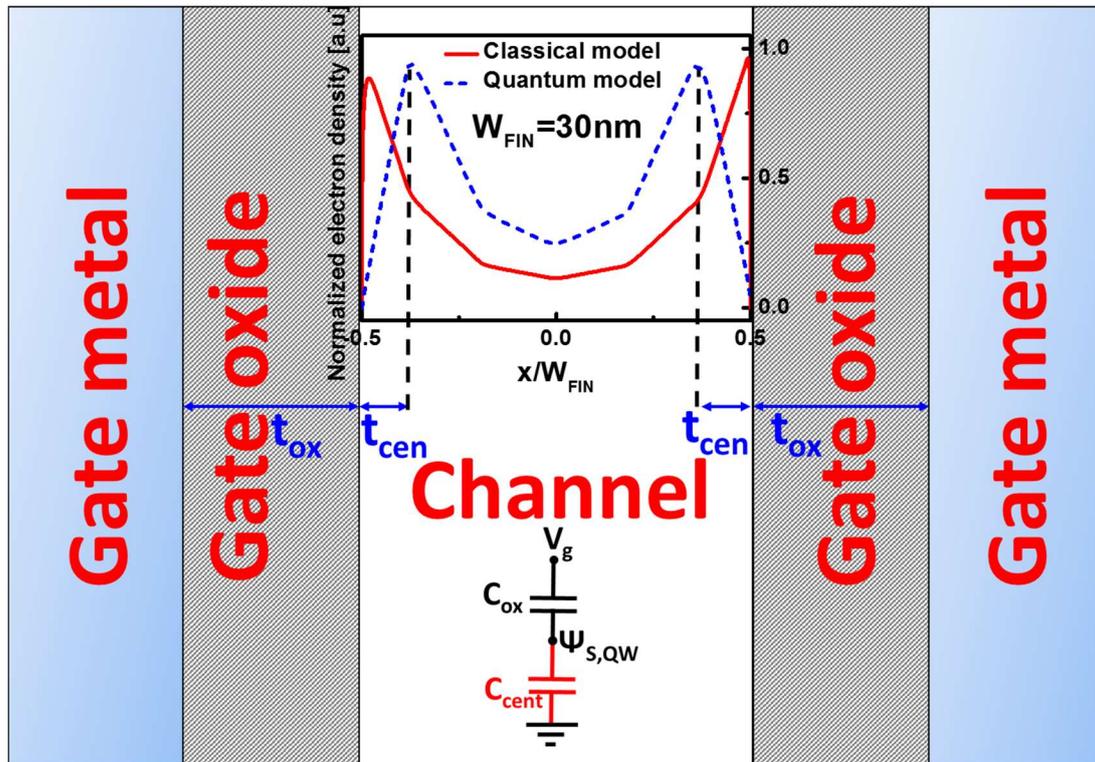


Fig 3.4 Schematic showing the shift of the normalized carrier density centroid away from the oxide/semiconductor interface. The carrier density for both models are normalized to the maximum carrier density of the classical model.

The reduced oxide capacitance will hence affect device DIBL and SS characteristics:

$$SS = \frac{K_B T}{q} \left(1 + \frac{C_D + C_{it}}{C_{ox'}} \right) \quad (3.8)$$

A degraded SS is evident in the quantum mechanical model as shown in Fig. 3.5. This increase in SS affects the threshold voltage (V_T) roll-off and hence worsens DIBL.

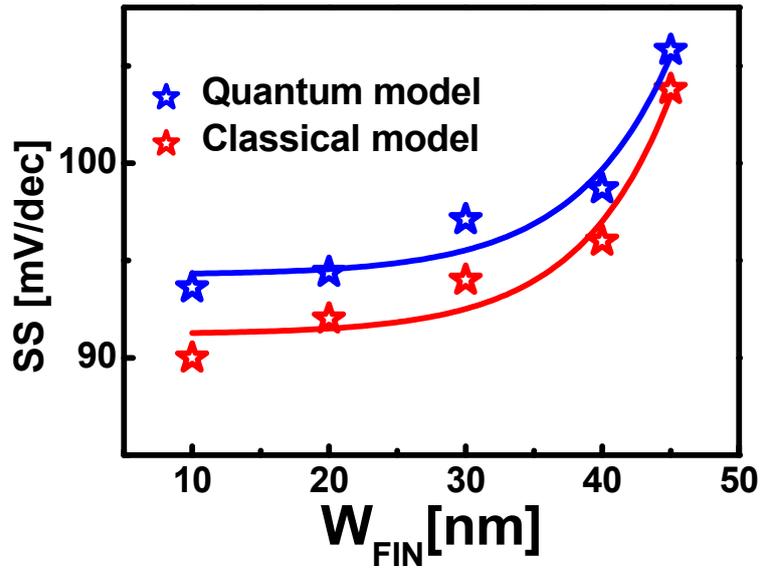


Fig 3.5 Comparison of the SS response between the classical and quantum model for the gate length of $L_G = 60$ nm. The underestimated SS in the classical case would simulate a more relaxed DIBL.

3.4 Device structure and key assumptions

An ultra-scaled gate-drain and gate-source separation ($L_{SIDE} = 5$ nm) InGaAs QW transistor was demonstrated, increasing effective gate area over the channel [3, 4] and hence improving electrostatic control. Subsequently, a simplified raised source/drain (S/D) scheme was employed with an epitaxially grown $In_{0.7}Ga_{0.3}As$ QW fin on an $In_{0.52}Al_{0.48}As$ bottom barrier (lattice mismatched system). However, this limited the critical thickness of the active layer due to strain induced dislocations due to film relaxation resulting in a shorter Fin height as discussed in Chapter 2.

To overcome this and optimize quantum confinement within the fin, the lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ system was employed to demonstrate taller fin height $H_{FIN}=50$ nm and width $W_{FIN}=30$ nm using inductively coupled plasma (ICP) dry etch [3, 4]. Following this, device quality ultra-high fin aspect ratio (H_{FIN}/W_{FIN}) long channel devices were demonstrated using a novel ICP etch process followed by a digital

etch which avoided dry etch damage improving device performance [1, 12]. Fin dimensionality plays a very influential role in improving device performance against short channel effects as will be discussed later in this work. Fig. 3.6 (a) and (b) shows the InGaAs QW fin structure with simplified S/D scheme [3, 4].

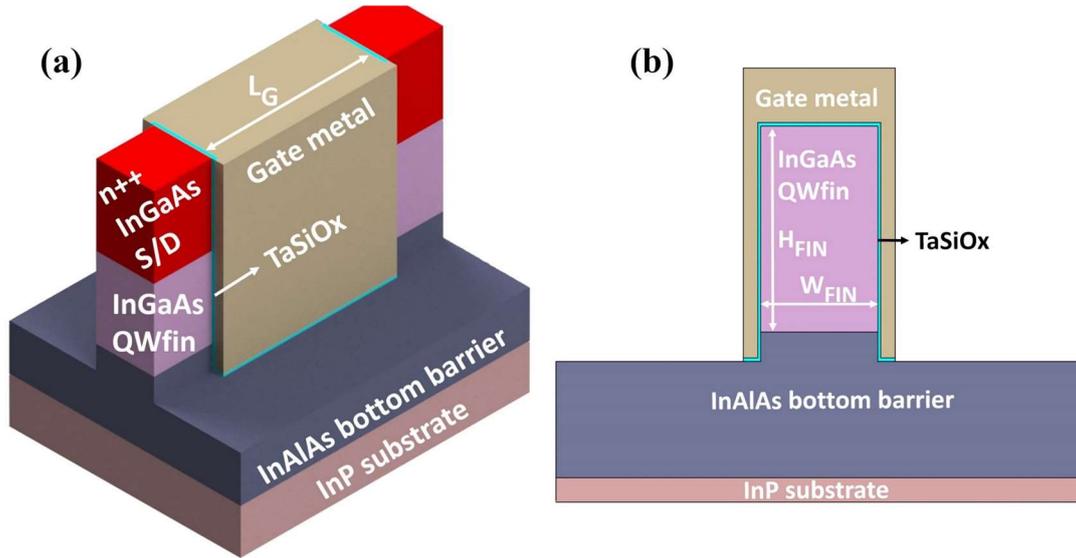


Fig. 3.6 a) Tri-gate InGaAs QW FinFET structure with simplified raised S/D scheme with scaled $L_{SIDE}=5\text{nm}$ [3, 4]. **(b)** Channel cross section with TaSiOx as gate dielectric on lattice matched (InGaAs/InAlAs) quantum well system.

The fin dimensions used to calibrate the models response to short channel effects are $L_G=60\text{nm}$, $W_{FIN}=40\text{nm}$ and $H_{FIN}=40\text{nm}$ with highly scaled $EOT=12\text{\AA}$ as discussed in Chapter 2 and reported in [4]. The channel cross section of this structure with $W_{FIN}=40\text{nm}$ is shown in Fig. 3.7. The n++ source/drain is doped $N_D=1 \times 10^{20}\text{cm}^{-3}$ and a channel doping of $N_A=5 \times 10^{17}\text{cm}^{-3}$ in these simulations.

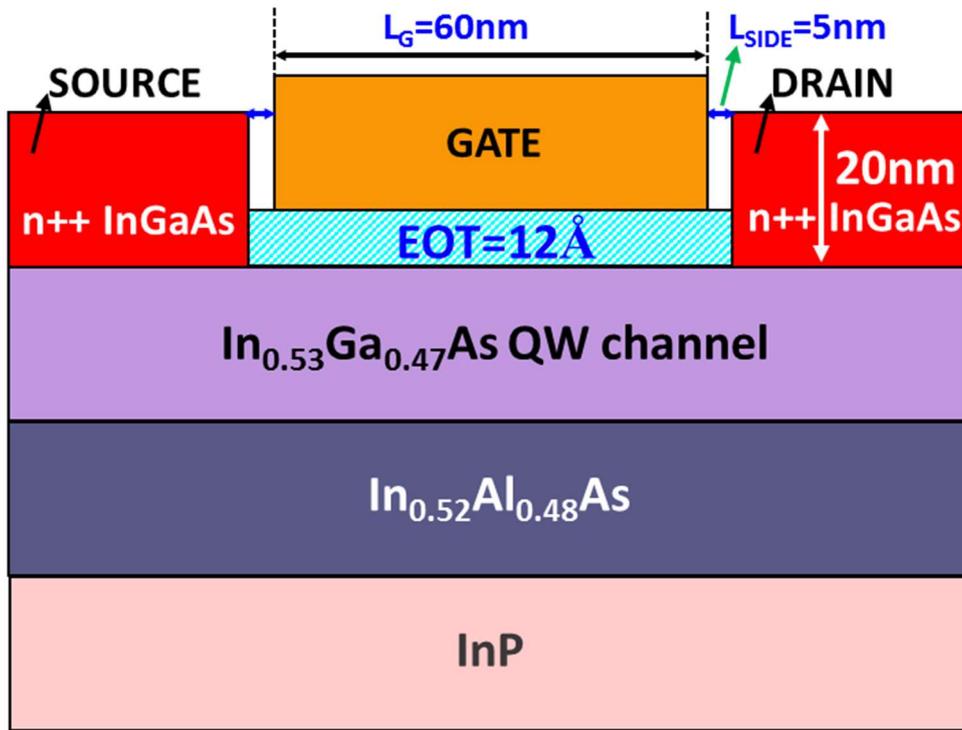


Fig 3.7 Channel cross section of Tri-gate device structure used to calibrate the model to the transfer characteristics and C-V reported in [4].

3.4.1 Band alignment and channel Band structure

The band-alignment of the lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ system applied to the simulations in this work is shown in Fig 3.8 [13-20]. Sentaurus allows for tuning of band alignment via Anderson's rule, which is rather crude but allows for simple alignment of intrinsic heterojunctions [21]. The band alignment of $\text{TaSiO}_x/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is still unknown, along with other material properties such as dielectric constant (ϵ_r) and bandgap (E_g). The bandgap of TaSiO_x has been shown to vary with the silicon composition [22, 23]. The model assumes the bandgap of TaSiO_x to be 4.6 eV which is also confirmed by our XPS analysis which will be discussed later in this work. The $\text{TaSiO}_x/\text{InGaAs}$ band alignment assumed in this work is calculated by the difference in electron affinities between InGaAs and Ta_2O_5 , 4.5 eV and 3.4eV

respectively to provide a $\Delta E_c \sim 1.4 \text{ eV}$ assume a $\text{Ta}_2\text{O}_5 - \text{InAs}$ like band alignment [24, 25].

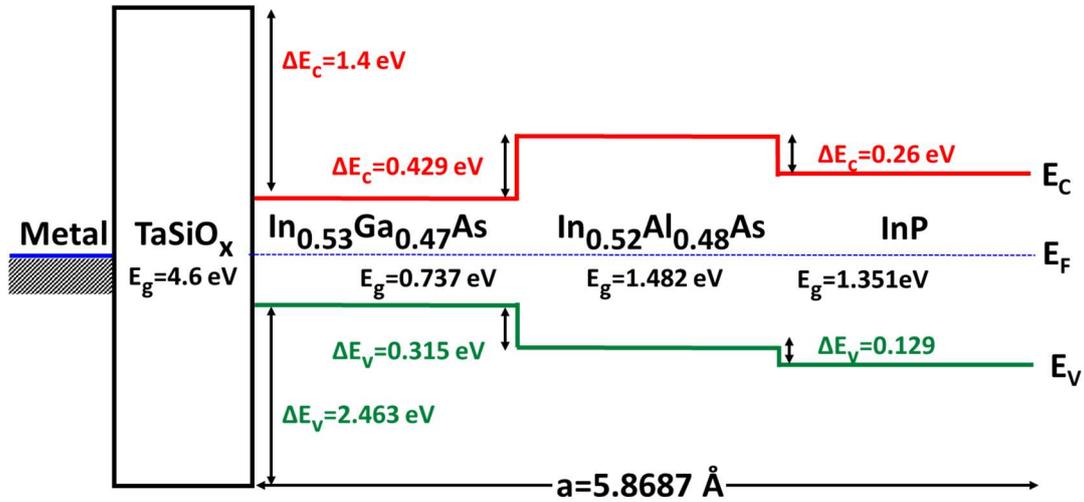


Fig. 3.8 shows the band alignment of the lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ QW system with TaSiO_x as gate dielectric.

The band structure of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ must account for non-parabolicity as discussed in the previous section along with proper assignment of valley dependant effective masses for accurate simulations. Fig. 3.9 shows the band structure of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [18, 20, 26] applied to simulations in this work.

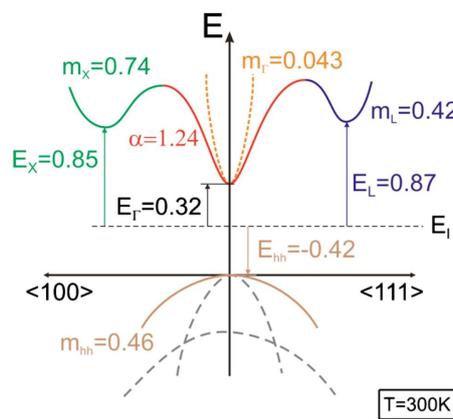


Fig. 3.9 Schematic band structure of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with valley dependant electron effective mass for $T=300 \text{ K}$. A non-parabolicity factor of $\alpha=1.24 \text{ eV}^{-1}$ is assumed in the Γ -valley [18, 20, 26]. Rights managed by AIP Publishing LLC.

3.4.2 TaSiO_x material and interfacial properties

Immense work has gone into uncovering the deposition process of TaSiO_x that demonstrated superior electrostatic properties on In_{0.53}Ga_{0.47}As with a vast study of the material properties [2-4, 22, 23, 27, 28]. And yet, there is only one reported data point with respect to interfacial quality [3]. The dielectric constant of TaSiO_x is shown to vary linearly depending on the molar fraction of Si present in the oxide unlike that band gap which shows a rather constant behaviour until the Si mole fraction exceed 40% [23]. The dielectric constant of Ta₂O₅ is shown to vary between 24~30 based on the process of deposition, nature of the oxide and annealing scheme employed. The dielectric constant of TaSiO_x was found to be $\epsilon_r \sim 13$ as will be discussed in the following sections of model calibration results.

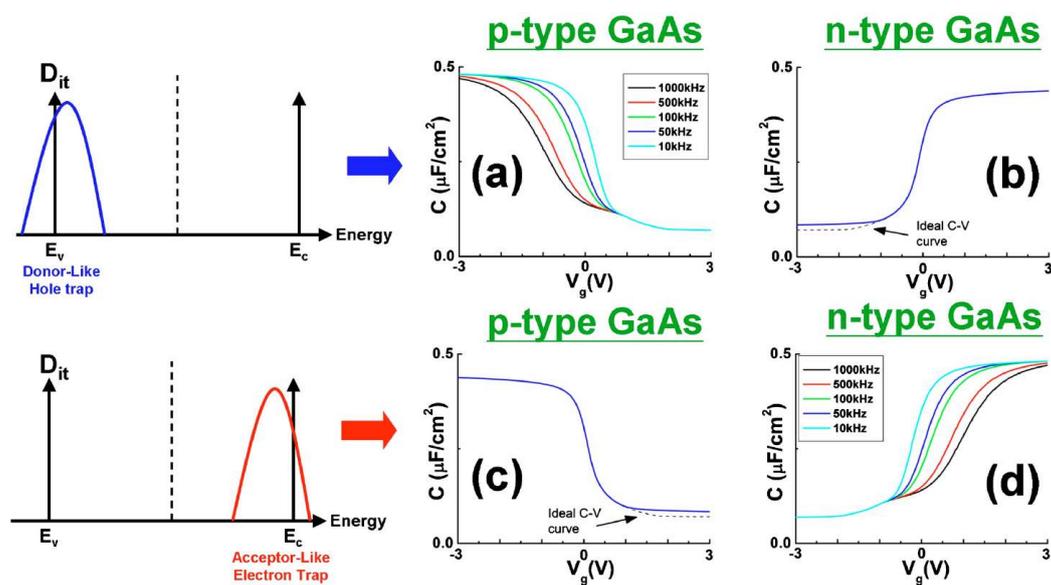


Fig. 3.10 Diagram of simulated C-V characteristics of the MOS structure with donor-like defect states [(a) and (b)] and acceptor-like defect states located at 0.1 eV above and 0.1 eV below conduction band edge [(c) and(d)] [29]. Rights managed by AIP Publishing LLC

The main thrust of this work is to develop a D_{it} distribution for the $TaSiO_x/In_{0.53}Ga_{0.47}As$ interface to model short channel effects which also agrees with transfer characteristics and gate electrostatics [4]. The density, nature and location of traps in the energy band at the interface can vary short-channel effects and device characteristics drastically [29]. Fig. 3.10 and 3.11 show the variance in C-V characteristics based on trap nature and location for an Al_2O_3 -GaAs MOSCAP [29]. The magnitude of the variation in C-V response is far less pronounced compared to short channel effects, which can vary drastically.

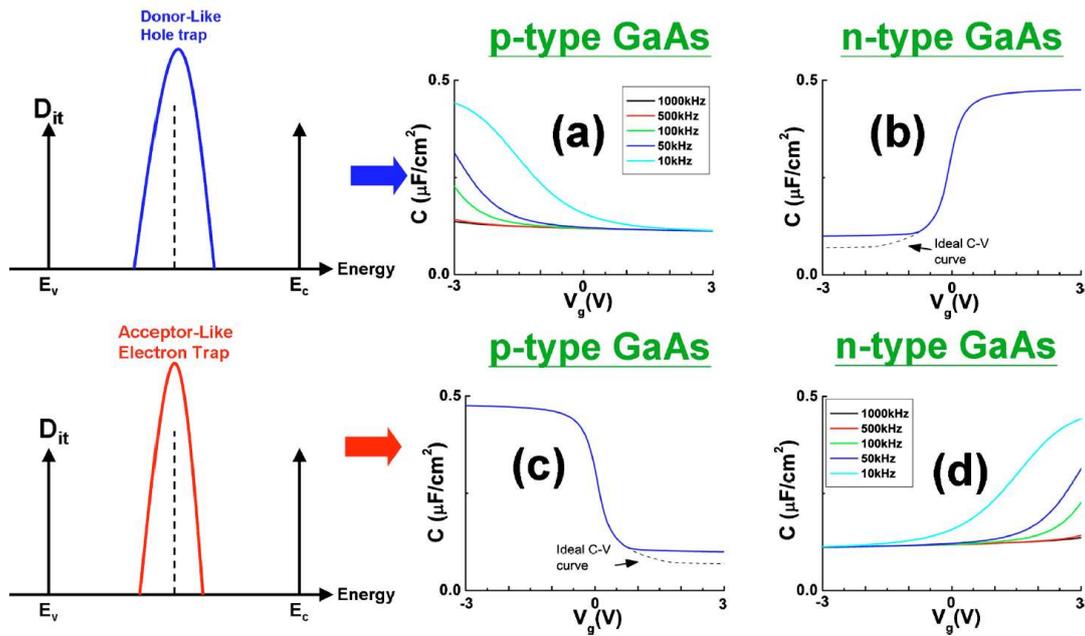


Fig. 3.11 Diagram of simulated C-V characteristics of the MOS structure with donor-like defect states [(a) and (b)] and acceptor-like defect states [(c) and (d)] located at mid-gap [29] Rights managed by AIP Publishing LLC

As mentioned before, the D_{it} distribution plays a crucial role in modelling short channel effects. Fig. 3.12 shows two different D_{it} distributions which have a comparable amount of trapped charge (Q_{it}) with the integral evaluated 0.2eV below the Valence

Band and 0.56eV over the conduction band which is the Γ -L energy band separation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [18, 20, 26]. The two distributions show similar subthreshold slopes $\sim 118\text{mV/decade}$. However, the resulting DIBL of both distribution is very different $\sim 144.6\text{mV/V}$ and 94.2mV/V respectively. In the case where Donor-Like Hole traps are dominating, severe degradation of DIBL occurs as shown in Fig 3.11 (a), Fig. 3.11 (b) has the same Q_{it} integral with a near 30% reduction in DIBL.

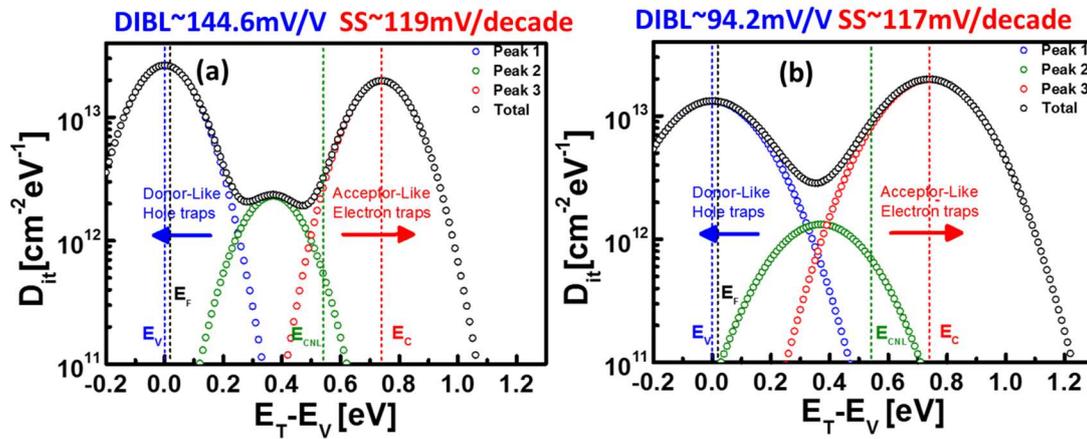


Fig. 3.12 (a) and (b) Two different D_{it} distributions with same Q_{it} integral exhibiting drastically different short-channel effects.

Since, the variation can be so drastic, it is critical to model a distribution which is consistent in providing results that agree with $C-V_G$, I_D-V_G , and the dimensional response of SS and DIBL response reported in [4]. The D_{it} distribution developed in this work is shown in Fig. 3.13, which as a unique distribution was able to calibrate the $C-V$ response of the fin structure, transfer characteristics reported in [4].

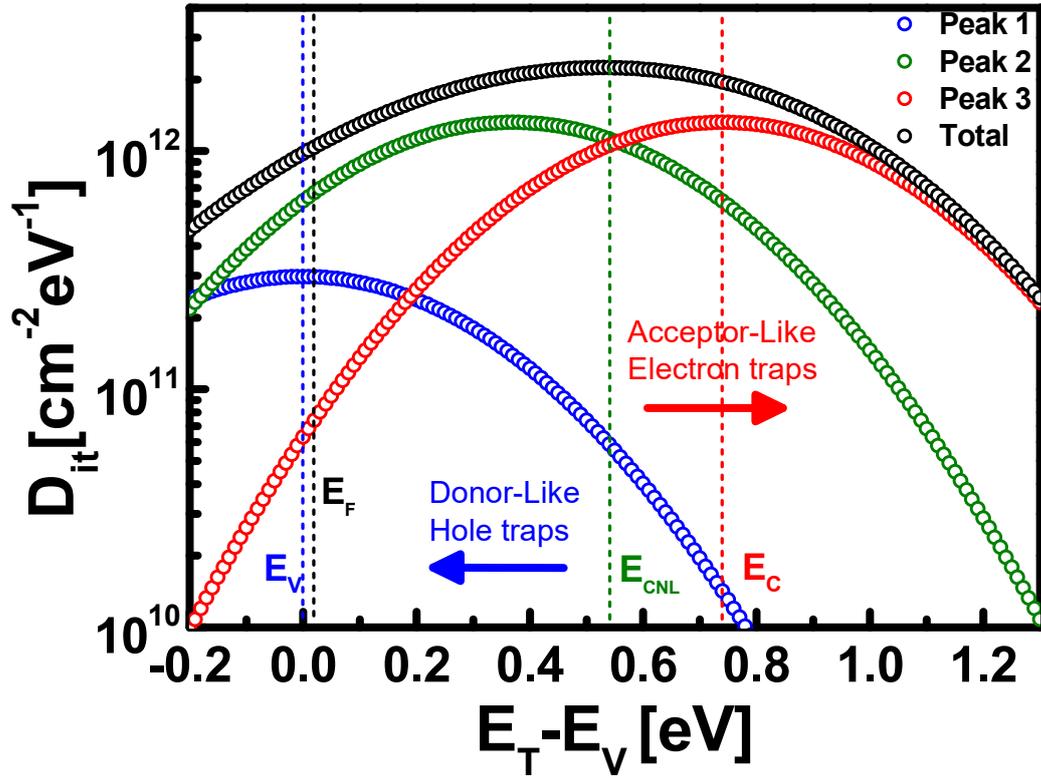


Fig. 3.13 Final D_{it} distribution implemented to calibrate data presented in [4].

The parameters implemented to all simulations is shown in Table 2.2.

Parameter	Value
$E_{g,\Gamma}$	0.74eV
$E_{g,X}$	1.33eV
$E_{g,L}$	1.2eV
N_{ch}	$5 \cdot 10^{17} \text{ (cm}^{-3}\text{)}$
N_{SD}	$1 \cdot 10^{20} \text{ (cm}^{-3}\text{)}$
$m_{e,\Gamma}^*$	$0.042m_0$
$m_{e,X}^*$	$0.74m_0$
$m_{e,L}^*$	$0.02m_0$
m_{hh}	$0.46m_0$
R_{SD}	$150 \Omega\text{-}\mu\text{m}$
σ_{Γ}	1.24eV^{-1}
$\kappa \text{ (TaSiO}_x\text{)}$	13

Table 3.1 Model simulation parameters

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Chapter 4 – Model Calibration and Results

4.1 Calibration results and discussion

With implementation of the D_{it} distribution discussed in the previous chapter, the model was calibrated to match the C-V response and the dimensional contribution to short channel effects reported in [1]. The response of the Tri-gate FET with unity fin aspect ratio is crucial to precisely determine the model's ability to estimate short channel effects (as discussed in Chapter 1) and hence for $L_G = 60$ nm, we base our model around the $H_{FIN}=W_{FIN}=40$ nm structure with transfer characteristics and dimension effect on short channel effects presented in [1]. Fig. 4.1 shows the calibrated C-V response of the Tri-gate QW fin structure with $W_{FIN}=45$ nm.

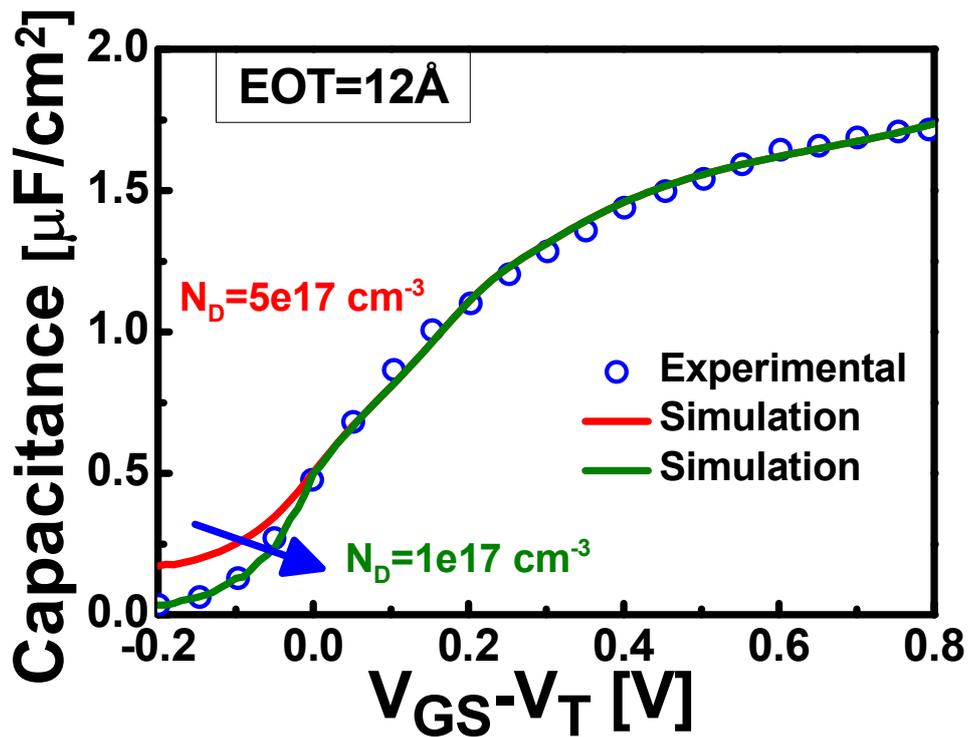


Fig 4.1 Simulated C-V characteristics using TCAD simulation fitted to presented experimental data [1]. The Tri-gate QW Fin width $W_{FIN} = 45$ nm and highly scaled (EOT=12Å) TaSiO_x as gate dielectric is in good agreement with presented experimental data.

As discussed in the previous chapter, the influence of the interfacial properties on device characteristics is crucial to calibrate device response. Depending on the magnitude, nature and position of traps, the C-V response, transfer characteristics and short channel effects of a device can be modelled [2]. Since we are modelling the device to follow the variation of DIBL and SS with L_G and W_{FIN} scaling based on previously presented data [1], a D_{it} distribution was developed which could agree with all variable parameters to calibrate the model to DIBL and SS response to dimensionality. The D_{it} distribution implemented consisted of 3 Gaussian curves to fit C-V, transfer characteristics and short channel effects. However, in the case of fitting DIBL, SS and C-V with a uniform distribution for several devices (i.e., multiple W_{FIN}), we prioritized matching the SS and DIBL response accepting a small error towards the depletion region as can be noted in Fig. 4.1. This can be attributed to p-type doping ($N_A=5 \times 10^{17} \text{cm}^{-3}$) in the channel of the FET structures used in calibrating the devices response to short channel effects as mentioned earlier. With equivalent n-type doping being applied to MOSCAP structures with C-V responses showing strong accumulation behaviour as reported in [1, 3, 4] which reduces the maximum depletion width (Eq. 4.1), thereby inducing a higher minimum capacitance in the deep depletion region of the C-V response as illustrated in [5].

$$x_{D,\max} = \sqrt{\frac{4\epsilon_0\epsilon_{ch}\ln\left(\frac{N_D}{n_i}\right)}{q^2N_D}} \quad (4.1)$$

This could suggest that, the n-type doping used in the structures of the C-V responses reported in [1, 3, 4] reduces to $1 \times 10^{17} \text{cm}^{-3}$ which would reduce the C_{\min} at high frequency (Eq. 4.2) to agree with the C-V response reported in [1].

$$\frac{1}{C_{\min, \text{HF}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{D}, \min}} \quad (4.2)$$

where $C_{\text{D}, \min}$ is the minimum depletion capacitance as a result of the maximum depletion width.

$$C_{\text{D}, \min} = \frac{\epsilon_{\text{ch}}}{x_{\text{D}, \max}} \quad (4.3)$$

Therefore, with increased doping $C_{\min, \text{HF}}$ increases. While this helps calibrate the C-V response reported in [1] by reduction the doping to $1 \times 10^{17} \text{cm}^{-3}$, a change in doping would affect the models response to DIBL due to variation of the extension of the depletion region into the channel.

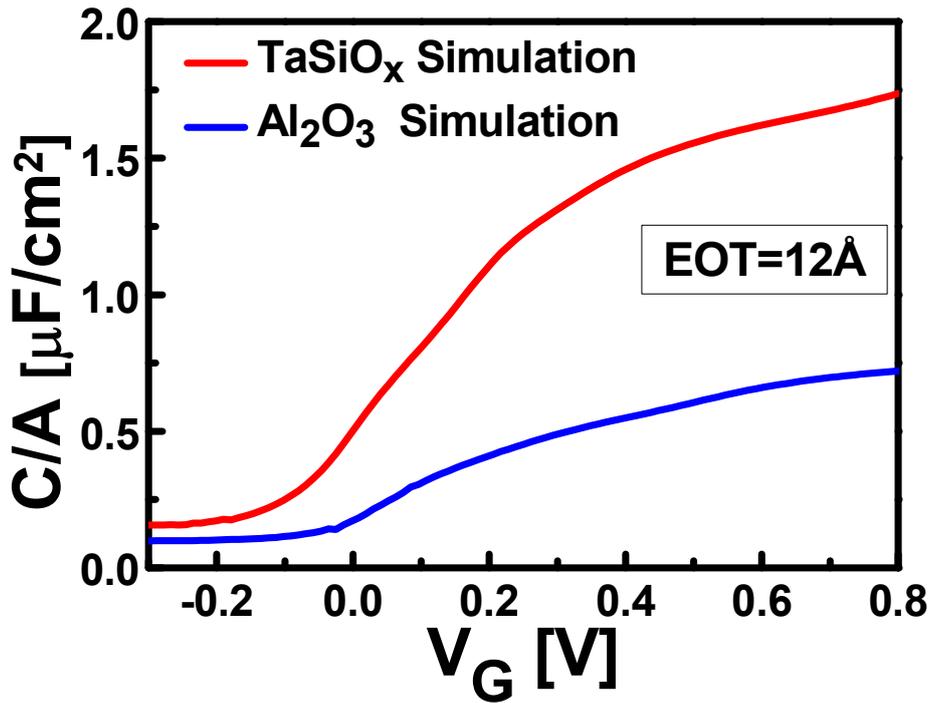


Fig. 4.2 Simulated comparison showing improved electrostatics with TaSiO_x (EOT=12Å) over Al₂O₃ as gate dielectric. Both models have the same doping $N_{\text{D}}=5 \times 10^{17} \text{cm}^{-3}$. The nature of the simulation agrees with data presented for the planar structure comparing Al₂O₃ and TaSiO_x as gate dielectrics [3].

The modeled Fin structure also shows the nature of improvement when compared to incorporating Al_2O_3 gate dielectric (Fig. 4.2) as reported in [3]. Both structures in this case have $N_D=5 \times 10^{17} \text{cm}^{-3}$ and an $\text{EOT}=12\text{\AA}$. Fig. 4.3 shows the simulated transfer characteristics (I_D - V_g) fitted to the experimental InGaAs QW Tri-gate FET ($N_D=5 \times 10^{17} \text{cm}^{-3}$) with $L_G = 60\text{nm}$ and $W_{\text{FIN}} = H_{\text{FIN}} = 40\text{nm}$ (unity fin aspect ratio). The effective channel width of the fin structure is given by $Z=2*H_{\text{FIN}}+W_{\text{FIN}} = 120\text{nm}$ [1]. The simulation yields favorable results in good agreement with experimental data.

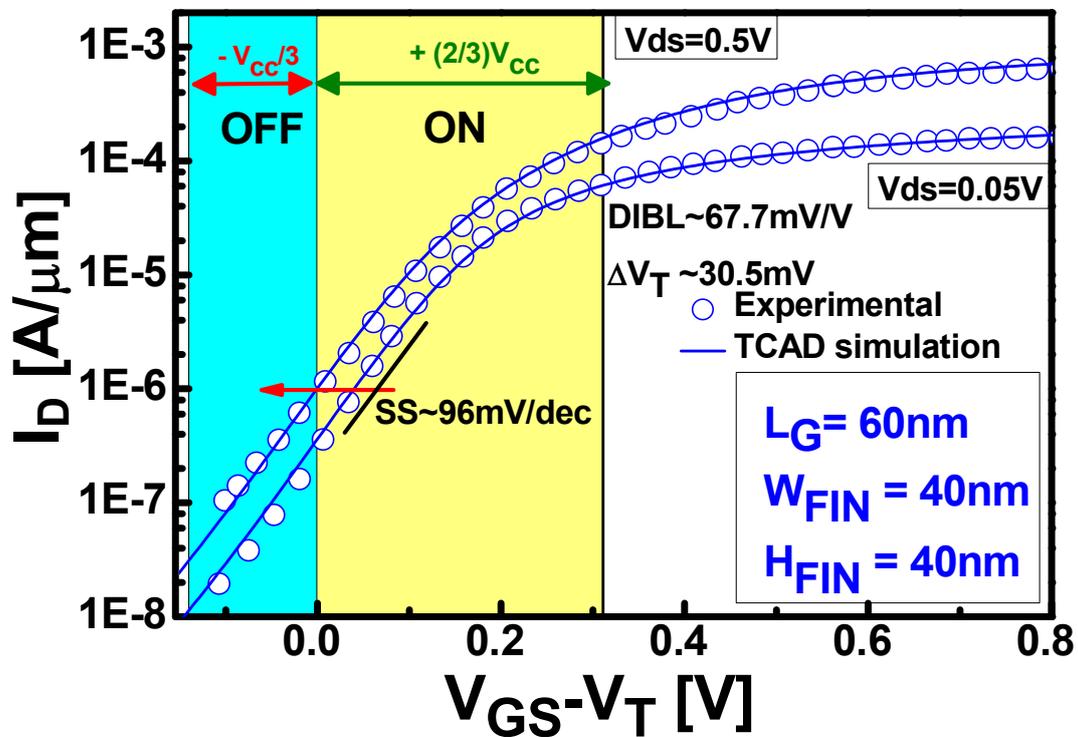


Fig. 4.3 Transfer characteristics using TCAD simulation fitted to match reported experimental data [1]. Device operation range shows a high $I_{\text{ON}}/I_{\text{OFF}}$ ratio $\sim 10^4$.

The transfer characteristics in Fig. 4.3 exhibit an $\text{SS} \sim 96\text{mV/decade}$ and a $\text{DIBL} \sim 67.7\text{mV/V}$ a peak transconductance (g_m) $\sim 1.4\text{mS}/\mu\text{m}$ and an $I_{\text{ON}}/I_{\text{OFF}}$ ratio $\sim 10^4$. The response of the model developed is extended to study the dimensional influence of the fin structure on short channel effects. Fig. 4.4 shows the calibrated DIBL response

as a function of gate length scaling ($L_G=60-325\text{nm}$) and fin width scaling ($W_{\text{FIN}}=45\text{nm}$ and 30nm) [1].

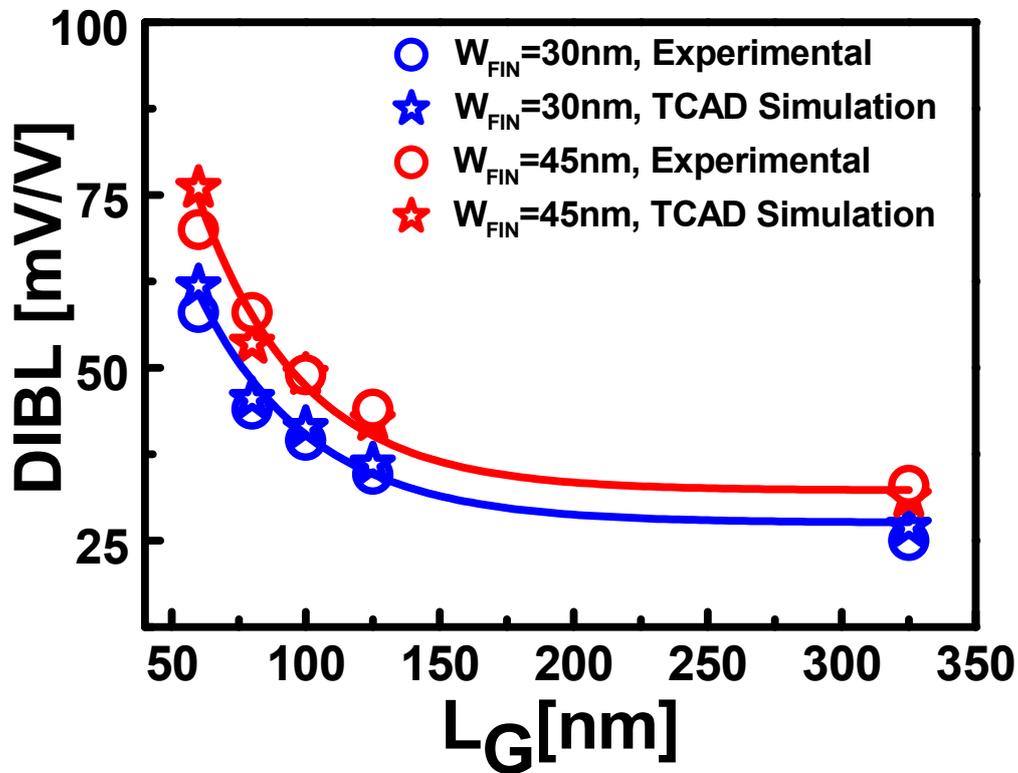


Fig 4.4 Simulated DIBL response with L_G scaling using TCAD simulation. The simulation of the Tri-gate QW fin has scaled to $EOT=12\text{\AA}$. Obtained data is in good agreement with the presented experimental data [1].

Fig. 4.5 shows the calibrated SS response as a function of gate length ($L_G=60-325\text{nm}$) scaling and fin width scaling ($W_{\text{FIN}}=45\text{nm}$ and 30nm) [1]. The amplification of short channel effects is exponential in nature with gate lengths below 150nm . The dimensional response of the Fin structure to model short channel effects is shown to be calibrated from the results in Fig 4.4 and 4.5. We will now look into how one could optimize a fin structure to reduce short channel effects.

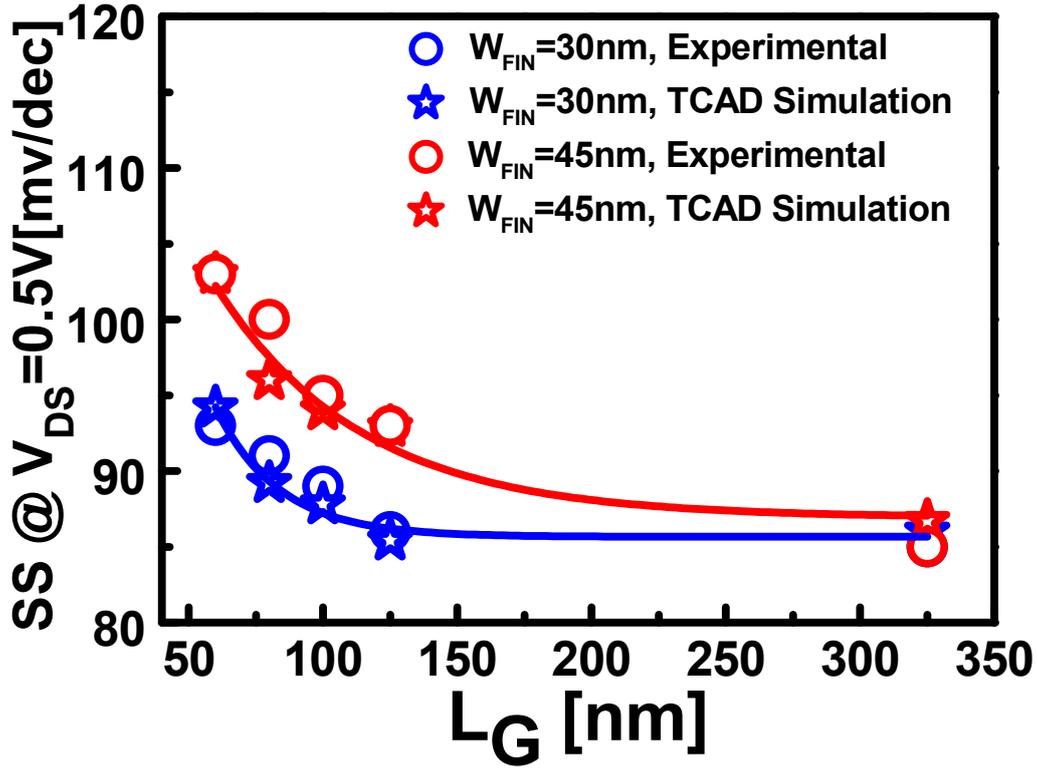


Fig 4.5 Simulated SS response with L_G scaling using TCAD simulation. The simulation of the Tri-gate QW fin has scaled to $EOT=12\text{\AA}$. Obtained data is in good agreement with the presented experimental data [1].

4.2 Fin scaling influence on device performance

As demonstrated in the previous section, we observe a reduction in short channel effects for a given gate length with reducing fin width. This is consequential to the improvement of electrostatic control of the gate to reduce the effect of the dominating drain induced depletion region. Depending on the material of the channel, the scaling factor of fin dimensions will play a major role in evaluating the dimensional requirements of a fin structure to counter short channel effects. Previous studies have shown that the lateral scaling (L_G/W_{FIN}) of plays a dominant role in dictating the fin structures performance against short channel effects over the Fin aspect ratio (H_{FIN}/W_{FIN}) whose improvement is not as effective to counter short channel effects, but

However, in case of the modelled InGaAs structure, the acquired results show much harsher restriction in fin dimensions to reduce short channel effects. Fig. 4.7 shows the variation of DIBL vs. L_G/W_{FIN} for the calibrated model.

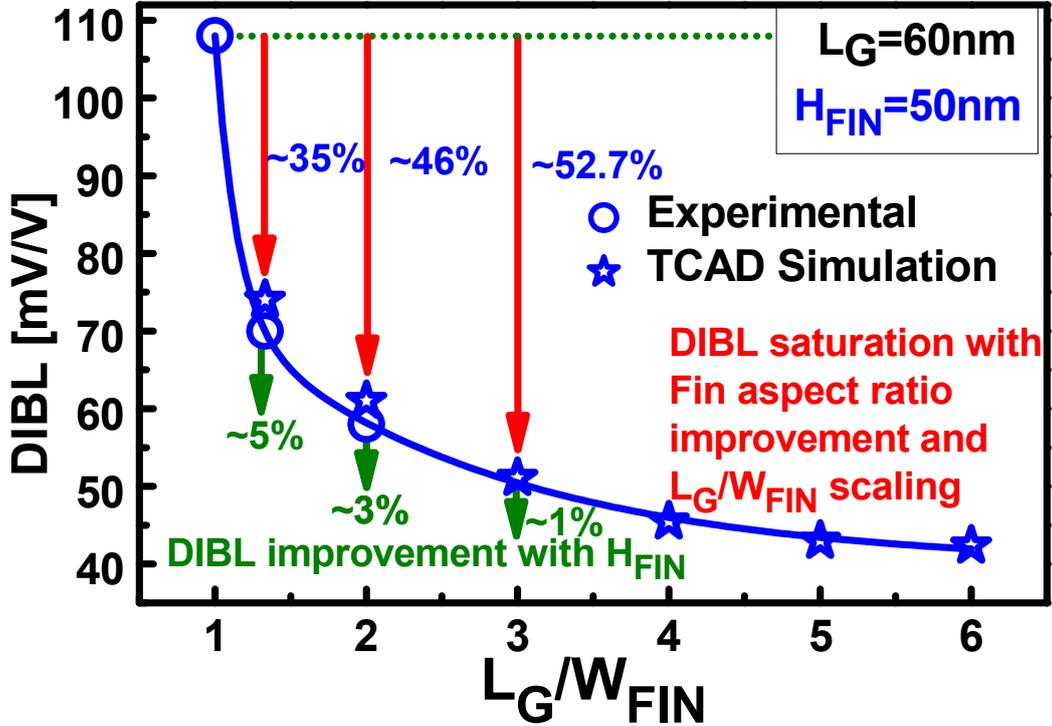


Fig 4.7 Drain Induced Barrier Lowering (DIBL) as a function of lateral scaling (L_G/W_{FIN}) for the calibrated Tri-gate model for $L_G=60\text{nm}$. Obtained data is in good agreement with reported experimental data [1].

As depicted in Fig. 4.7, a near 50% reduction in DIBL can be achieved for $L_G/W_{FIN} \sim 3$, which is a far-cry when compared to the case of Silicon with a near 100% increase in threshold dimensionality to mitigate short channel effects. However, the reduction in DIBL is more pronounced when compared to Subthreshold-slope, whose influence is not as affected by lateral scaling (L_G/W_{FIN}) of the channel. This is consequential to the dominance of traps to influence the subthreshold slope as discussed in the previous chapter governed as:

$$SS = \frac{K_B T}{q} \left(1 + \frac{C_D + C_{it}}{C_{ox'}} \right) \quad (4.4)$$

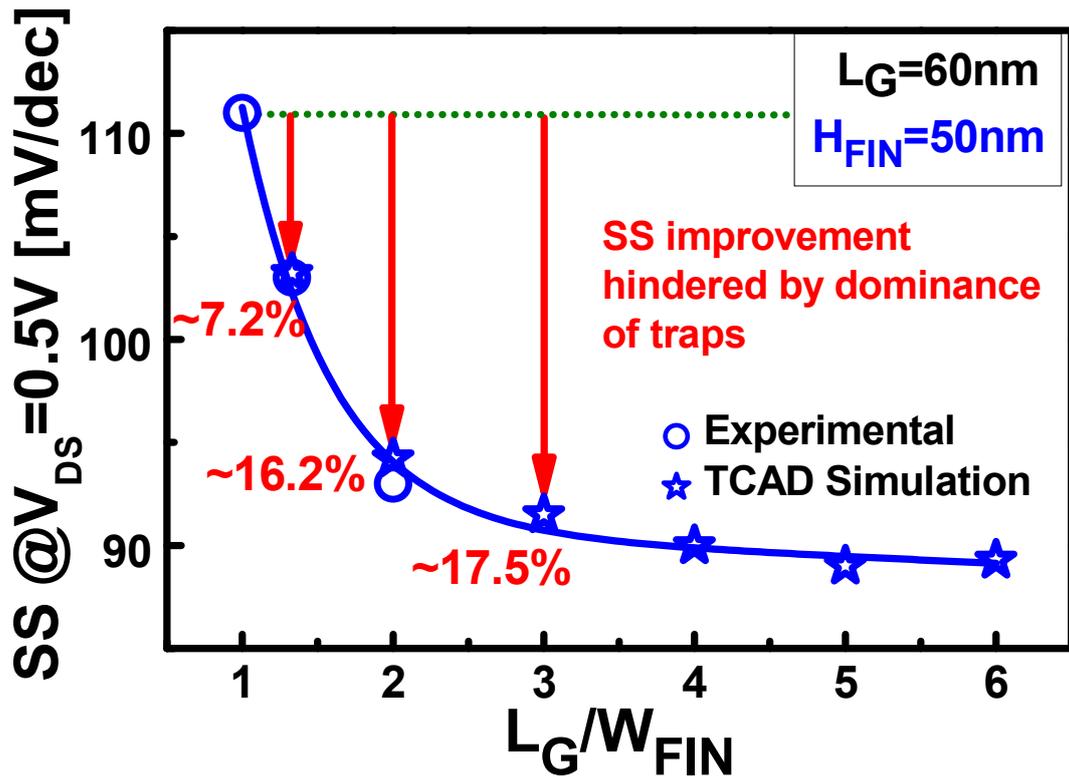


Fig. 4.8 Subthreshold slope (SS) as a function of lateral scaling ($L_G=10\text{nm}$,) for the calibrated Tri-gate model for $L_G=60\text{nm}$. Obtained data is in good agreement with reported experimental data [1].

Beyond the improvement observed from the lateral scaling of fin dimensions (L_G/W_{FIN}) which is the primary factor, higher aspect ratio fins can improve performance against short channel effects due to the dominance of sidewalls ((110) planes) for carrier transport. However, this improvement is meager compared to the lateral scaling of fins which will be discussed in the following section. The results obtained thus far aid the models integrity of short channel response to fin dimension scaling. The model is thus scaled down to $L_G=10\text{nm}$, while accounting for appropriate approximation of quantization of energy levels in the ellipsoidal non-parabolic $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ band using the MLDA model discussed earlier [9-12].

4.3 Short channel performance and benchmarking

Assuming transferable interfacial quality, the active layer is scaled to $L_G=10\text{nm}$, implying an $L_{\text{channel}}=20\text{nm}$ to study the performance of the short channel device against short channel effects. The requirement for ultra-high fin aspect ratios has pushed the industry to improve its lithographic and process capabilities to demonstrate thin fins.. High fin aspect ratio structures are typically subject to sidewall damage, fin bowing and cracking yield to severe yield issues [13, 14]. Ultra-high fin aspect ratios have been demonstrated on long channels as a promising step for the development of III-V QW Tri-gate technology [14]. However, device quality level high aspect ratio fin structures are yet to be demonstrated for short channel devices. Low aspect ratio structures have been demonstrated using inductively coupled plasma (ICP) dry etch with superior interfacial quality employing TaSiO_x as gate dielectric [1, 4]. Following this, high quality ultra-high fin aspect ratio long channel device were demonstrated using a novel ICP etch process followed by a digital etch which avoided dry etch damage improving device performance [14, 15], however these Nanowire structures implemented Al_2O_3 as gate dielectric and it's compatibility with TaSiO_x is yet to be explored to develop an optimized process. While the requirement for a strict vertical smooth etch still dominates the industries lithographic proprieties, trapezoidal fins can be employed to improve yield at the cost of gate electrostatic control by reduction of sidewall angle creating a trade-off to optimize process yield and device performance quality [15, 16]

The short channel effects of the scaled device are first evaluated for unity lateral ratio as explained earlier ($L_G= W_{\text{FIN}}=10\text{nm}$) and increasing fin aspect ratio which yields a small improvement in short channel effect performance and then scaled further to $W_{\text{FIN}}=7\text{nm}$. Fig. 4.9 shows the reduction of DIBL with increase in Fin aspect ratio for $W_{\text{FIN}}=10\text{nm}$ and 7nm .

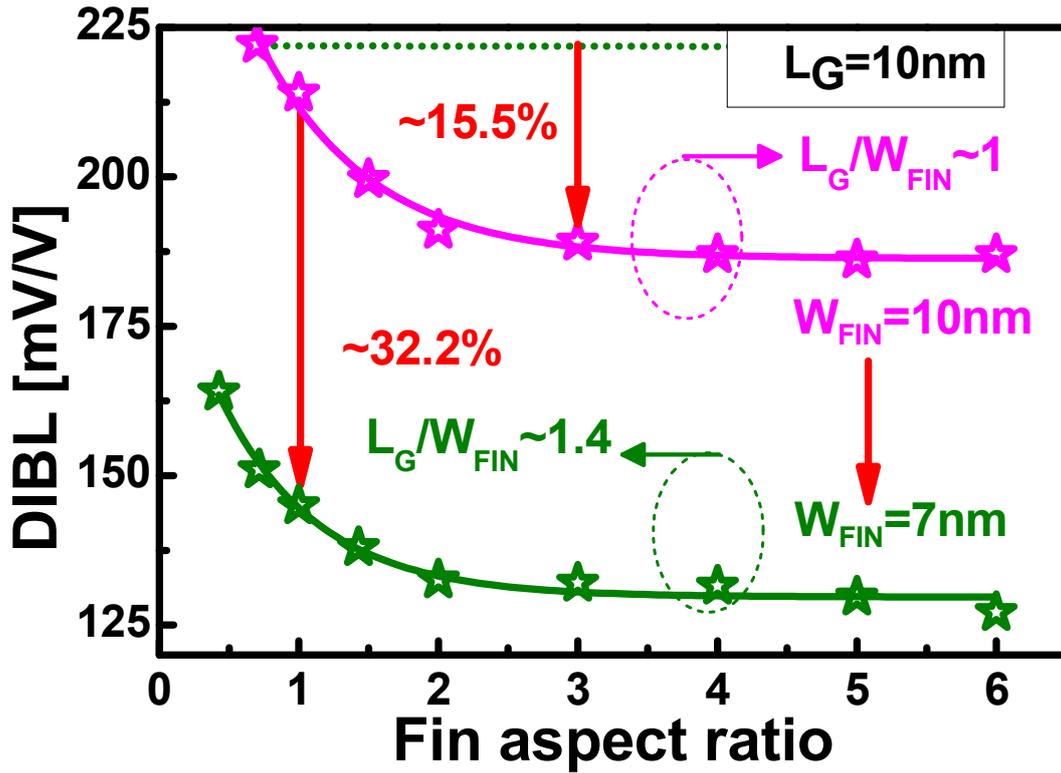


Fig. 4.9 Simulated DIBL response for $L_G=10\text{nm}$ and $W_{\text{FIN}}=10\text{nm}$ & 7nm .

A significant improvement with lateral scaling is observed as expected.

As expected, the improvement in lateral scaling factor (L_G/W_{FIN}) drastically improves, the $W_{\text{FIN}}=7\text{nm}$ fin exhibits a $\text{DIBL} \sim 125\text{mV/V}$. The reduction in SS however, is not as pronounced (Fig. 4.10), due to the limitations of the lateral scaling factor as discussed in the previous section.

The enhanced dependence of SS improvement on fin aspect ratio for $W_{\text{FIN}}=10\text{nm}$ and 7nm is due to the saturation of average lateral electric field from sidewall gates once carrier volume inversion of the fin structure takes place [17]. This is due to the superposition of electric field penetration from the sidewall gates with reducing W_{FIN} after carrier inversion within the fin. And hence, taller fins in this case consequentially improve sidewall gate control.

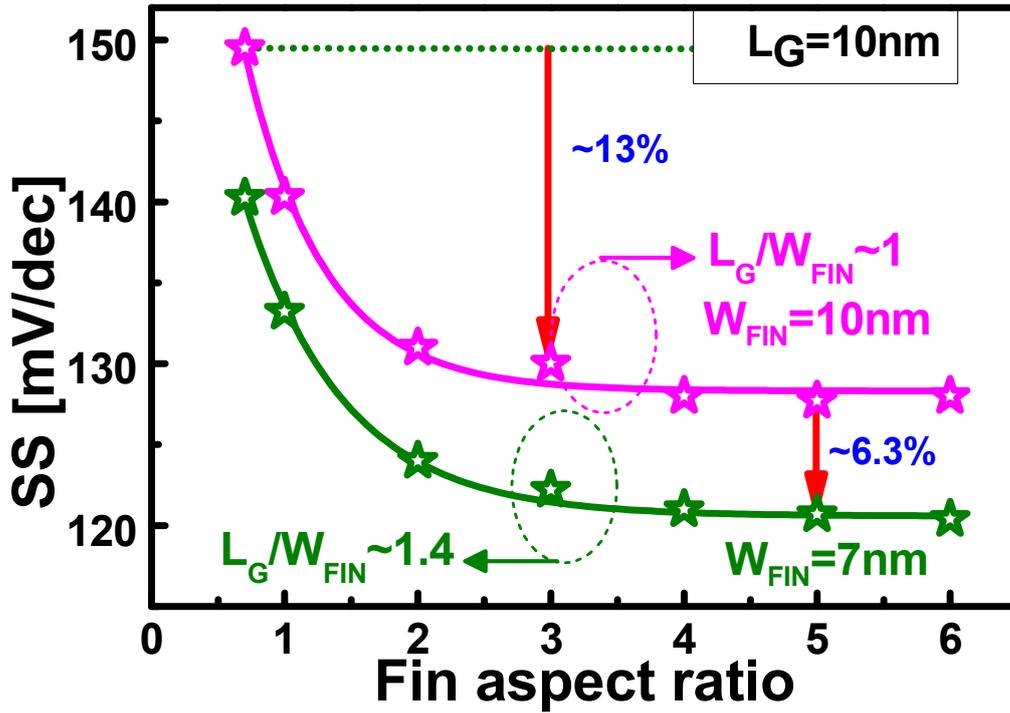


Fig. 4.10 Simulated SS response for $L_G=10\text{nm}$ and $W_{\text{FIN}}=10\text{nm}$ & 7nm . In the case of SS, Fin aspect ratio yields a significant improvement over lateral L_G/W_{FIN} scaling as explained below.

With the evaluation of short channel effects, it is important to evaluate device characteristics such as transconductance (g_m), leakage current (I_{OFF}) and $I_{\text{ON}}/I_{\text{OFF}}$ ratios. Fig 4.11 shows the variation of transconductance (g_m) with W_{FIN} scaling for a constant $H_{\text{FIN}}=50\text{nm}$. The scaling of W_{FIN} which reduces ON current (I_{ON}) [15] negatively impacts the transconductance (g_m) with increasing aspect ratio for $H_{\text{FIN}}=50\text{nm}$ as shown in Fig. 4.11 [18]. However, the severity of transconductance degradation reduces with scaling of the channel length which boosts ON current (I_{ON}) and hence improves the transconductance for given W_{FIN} [18, 19].

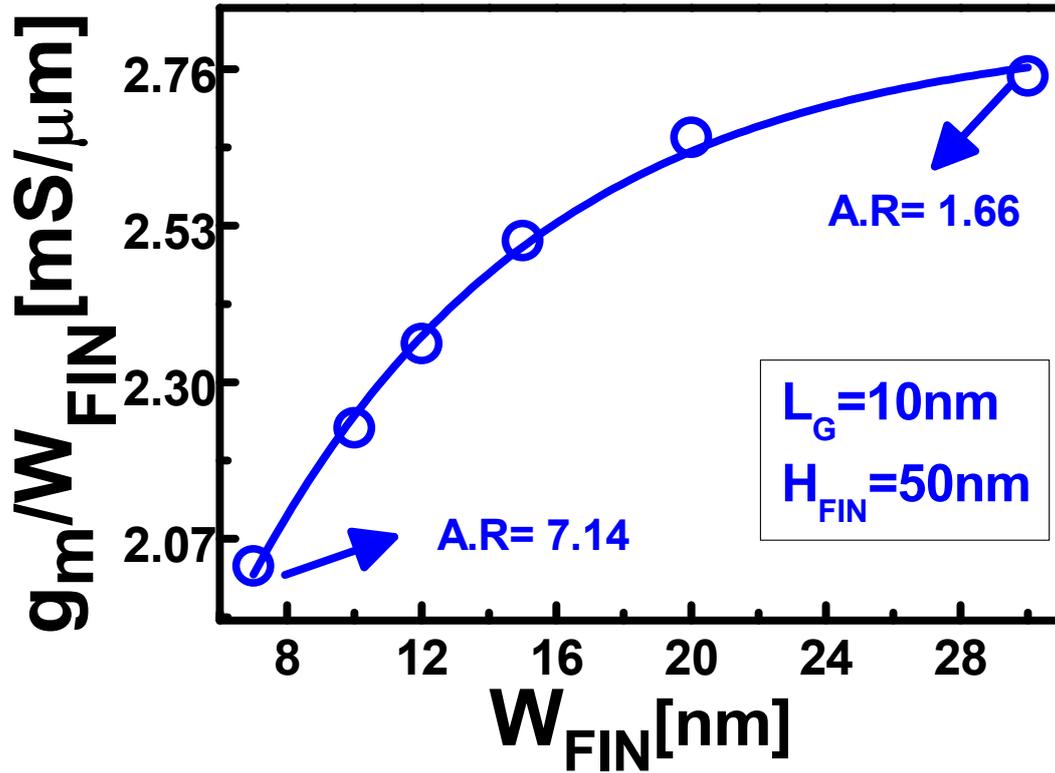


Fig. 4.11 Simulated transconductance (g_m) response with W_{FIN} scaling for $L_G=10\text{nm}$ and $H_{FIN}=50\text{nm}$. The reduction in transconductance with W_{FIN} scaling is as expected for increase aspect ratios.

The nature of transconductance degradation with increase in aspect ratio creates a tradeoff with optimizing subthreshold slope and the fins ability to contain charge. This leads to another benchmarking parameter which is the ratio of transconductance and subthreshold slope (g_m/SS) by which a devices ability to convert gate voltage to current is assessed. And the requirement for high aspect ratio fins can degrade this without improvement in interfacial quality by which subthreshold slope can be substantially reduced as discussed in the previous chapter. Fig. 4.12 is the performance benchmarking of the simulated model with $L_G=10\text{nm}$ with a high g_m/SS quotient.

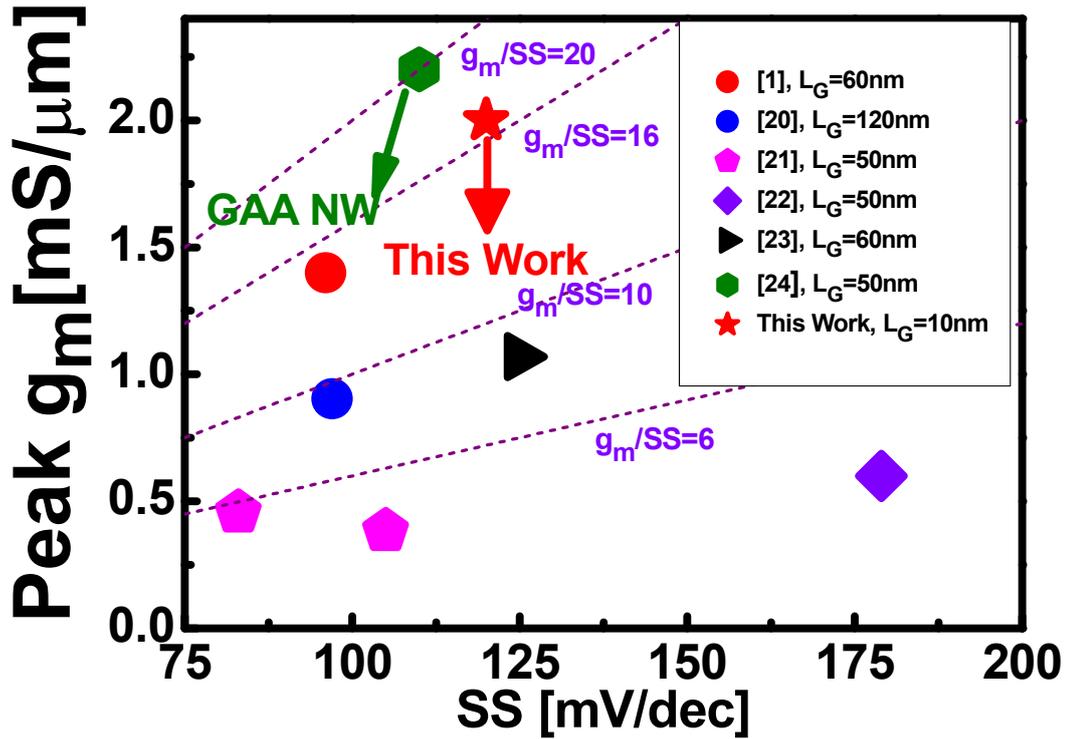


Fig. 4.12 Performance benchmarking of short channel ($L_G=10\text{nm}$) InGaAs QW tri-gate structure with highly scaled TaSiO_x ($EOT=12\text{\AA}$) as gate dielectric [1, 20-24].

From scaling of the model to a 10nm gate length, a significant improvement in the g_m/SS factor was observed despite the degradation of short channel effects. This can be correlated to the superior interfacial quality of the TaSiO_x/InGaAs system and the highly scaled gate-source and gate-drain separation of $L_{SIDE}=5\text{nm}$ allowing for a higher gated area of the channel which becomes even more critical with gate length scaling. Furthermore, the resulting leakage current (I_{OFF}) and I_{ON}/I_{OFF} ratio obtained is shown in Fig. 4.13. A degrade I_{ON}/I_{OFF} is inevitable due to W_{FIN} reduction which deteriorates drain current (I_D) [15]. However, the leakage current (I_{OFF}) is shown to sustain despite gate length scaling. This can be attributed to the employment of narrow fin structures that provide superior electrostatic control of the channel at short gate lengths. While W_{FIN} reduction plays villainous role to detrimentally impact drain current (I_D). The

improvement in gate electrostatics allows for a higher I_{ON}/I_{OFF} ratio therefore outweighing the reduction of drain current as indicated in Fig. 4.13.

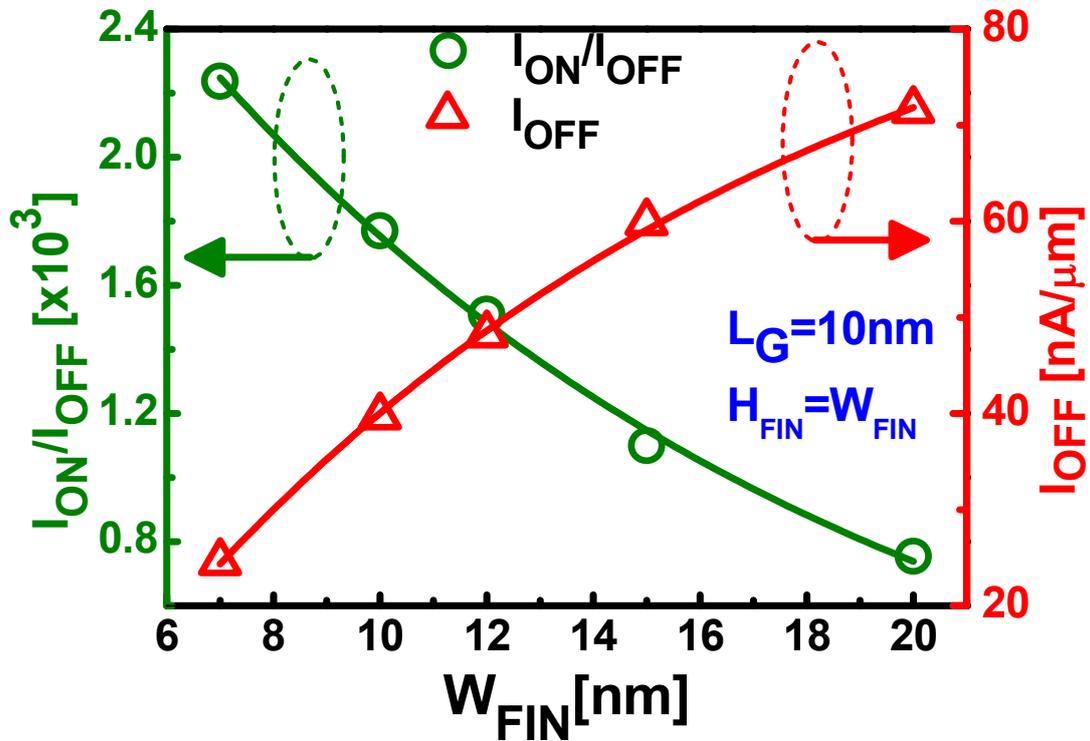


Fig. 4.13 Observed short channel ($L_G=10\text{nm}$) I_{ON}/I_{OFF} ratio shows increase with W_{FIN} scaling for given I_{ON} with simultaneous reduction in I_{OFF} shows improved gate control.

Table 4.1 is a performance benchmarking of the simulated short channel device model with other relevant work employing the same composition of Indium in the active layer.

Reference	Architecture	Oxide	L_G (nm)	V_D, V_G (V)	EOT (\AA)	DIBL (mV/V)	SS (mV/dec)	$\frac{I_{ON}}{I_{OFF}}$	g_m (mS/ μ m)
Intel [1] (2011)	Tri-gate	TaSiO _x	60	0.5,0.5	12	68	96	1.17×10^4	~1.4
MIT [14] (2014)	NW	Al ₂ O ₃	240	0.5,1.0	22	180	155	1×10^3	0.255
MIT [25] (2013)	NW	Al ₂ O ₃	80	0.5,1.0	22	360	305	$\sim 10^2$	0.73
UCSB [26] (2015)	UTB	HfO ₂	40	0.5,0.5	-	110	83	4×10^3	1.2
IMEC [24] (2015)	NW	IL/HfO ₂	50	0.5,0.5	-	103*	96-400	1.5×10^3 *	1.5-2.2
This work	Tri-gate	TaSiO _x	60	0.5,0.5	12	~67.7	96	1.17×10^4	~1.4
This work	Tri-gate	TaSiO _x	10	0.5,0.5	12	130	120	2.3×10^3	2.04

Table 4.1 Performance benchmarking of simulated short channel device

*At SS=96mV/dec

4.4 Carrier volume inversion and mobility enhancement

The scaling of fin dimensions leads to the quantization of energy levels, leading to an increased variation in the threshold voltage (V_T) and stronger lateral electric field penetration which causes carrier volume inversion [10-12, 15]. This leads to the shift in centroid charge towards the interface with reducing fin width as shown in Fig. 4.14. This can be accounted for by the utilization of the MLDA model, where the spatial variation of the root of the spherical Bessel function correlates to the shift in the distance of the charge centroid towards the interface (T_{cen}) with increase in energy. The non-parabolicity of ellipsoidal InGaAs plays a crucial role as it impacts energy level quantization in a detrimental fashion.

At the point of carrier volume inversion, mobility degradation due to carrier-sidewall scattering of the fin is minimized [17]. Further scaling of the fin will reduce T_{cen} thereby increasing sidewall scattering probability to cause mobility degradation. However, reduction in T_{cen} in this case can play the role of a double-edged sword with reduction of effective EOT to improve gate electrostatics. With this, the requirement for tall narrow-fin structures will pronounce this factor due to the dominance of (110) planes for electron transport and is critical to model quantum transport for future predictive analysis of device characteristics. While this model assumes a piece-wise constant mobility calibrated to data presented in [1] for $V_{DS}=50mV$ and $0.5V$, the main thrust of this work is to create a model capable of reciprocating implications of short channel effects with dimensional variation of the 3D fin.

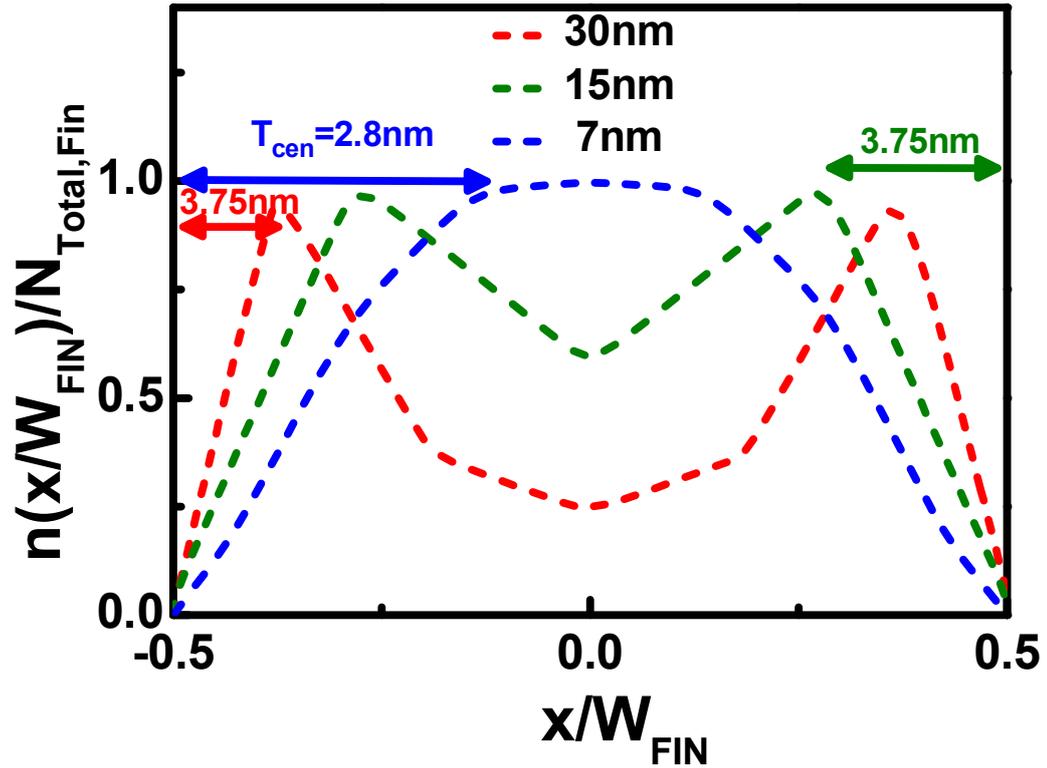


Fig. 4.14 Carrier density profile of the fin structure in the quantum regime. The quantization of energy levels leads to the shift of the charge centroid away from the oxide/semiconductor interface to cause carrier volume inversion within the fin to reduce the probability sidewall scattering events within the 3D active layer.

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Chapter 5 – Development of TaSiO_x process and band alignment with InGaAs

TaSiO_x has gained significant importance due to the ability of amorphous silicon interfacial layers to passivate III-V surfaces by the formation of Si-O species to substantially reduce dangling bonds (Ga³⁺-O) and improve C-V dispersion, thereby improving the quality of the integrated high-κ material [1-4]. Despite the successful integration of TaSiO_x on InGaAs to demonstrate interfacial quality on par with Al₂O₃ boasting a 2-fold gate electrostatic improvement [5], much about the oxide's deposition process (details like the growth temperature, type of precursors, number of cycles of Si pre-pulse as well as amount of Si inside the TaSiO_x) and band alignment with InGaAs is still unknown to the scientific community. Recently, there has been a surge in the study of TaSiO_x material properties and its integration onto both n-type and p-type InGaAs materials using chlorine based precursors (SiCl₄ and TaCl₅), however, all attempts to study the oxide's electrical properties have come short of the superior electrostatic properties with the formation of an indium oxide interfacial layer between TaSiO_x and InGaAs having a detrimental impact on gate electrostatics[6]. This has led to a growing suspicion that chlorine-based precursors are the root cause of the oxides' shortcoming on these materials [6-10]. Moreover, the byproducts of these chlorine-based precursor contaminate industrial standard stainless steel chambers as well as can etch the deposited oxide materials which could be the cause of the oxide qualities shortcoming [6-11]. Furthermore, these precursors are detrimental to InP based materials since chlorine etches InP materials and the reaction by-products can incorporate within the deposited oxide material. The atomic layer deposition (ALD) process of TaSiO_x in this work utilizes Tantalum (V)-ethoxide (Ta₂(OC₂H₅)₁₀) and Tris(tert-butoxy)silanol (Si(OH)(OC(CH₃)₃)₃) also known as TBOS for Ta and Si

precursor, respectively, and H₂O to develop a chlorine-free precursor based TaSiO_x process for device quality oxides. . In addition to the development of TaSiO_x oxide deposition process, the band alignment of TaSiO_x and its D_{it} distribution across the energy band is still yet to be experimentally verified. While this work has successfully demonstrated a theoretical D_{it} distribution, as discussed in Chapter-4, to reciprocate the superior electrostatic capabilities of TaSiO_x, band alignment studies are also performed to validate the band alignment employed in the simulations of this work, which will be discussed in the following sections.

5.1 Si Incorporation in Ta₂O₅ via Si: Ta Super-Cycles for ALD TaSiO_x on InGaAs

After we have established Ta₂O₅ deposition process conditions using Cl-free precursors, as discussed earlier using thermal ALD, TaSiO_x dielectric with a fixed Si alloy composition was investigated using thermal ALD technique. Fig. 5.1 shows the valve switching sequence during thermal ALD deposition of TaSiO_x and Si:Ta super cycle definition (1:5) targeting a ~30% Si in (Ta₂O₅)_{1-x}(SiO₂)_x layer on (100)InGaAs and (110)InGaAs. In addition, the different crystallographic oriented epitaxial layers

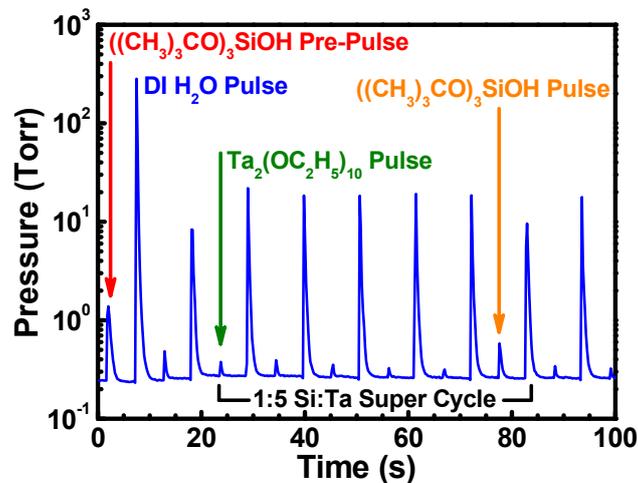


Fig. 5.1 Si:Ta super-cycle employed for the deposition of 30% Si TaSiO_x.

enable to determine the Si incorporation inside the TaSiO_x layer. The pre-pulsing of the Si from TBOS is implemented in order to bond Si with InGaAs prior to TaSiO_x deposition to avoid the formation of highly undesirable Ga³⁺-O dangling bonds with formation of Si-O species which has been demonstrated to reduce frequency dispersion considerably [1-4]. In order to verify whether the Si atoms from the ALD precursor enable to make a bond with crystallographic oriented InGaAs surface, XPS measurements were performed and Fig. 5.2 shows the TaSiO_x surface survey spectra as a function InGaAs orientation. The spectra were collected after removing the carbon 1s peak from each surface. One can find Si 2s/ 2p peaks from each oriented InGaAs, confirming the attachment of Si atoms on the surface of InGaAs. If the Si atoms doesn't incorporate into the TaSiO_x film, one shouldn't expect a Si 2s or 2p peak from the XPS scan. One can conclude that irrespective of the substrate orientation, Si was incorporated into the TaSiO_x layer. In future work, a systematic investigation of the Si incorporation into TaSiO_x layer as a function of InGaAs orientation and indium alloy composition using thermal as well as plasma enhanced ALD, where XPS measurements and spectroscopic ellipsometry measurements will be key measurement techniques to identify the chemical bonds in the oxide film as well as at the interface and bandgap of TaSiO_x as a function of Si incorporation. Cross-sectional TEM measurements at the oxide/InGaAs interface can further evaluate the interface abruptness, atomic cross-diffusion, and thickness of the oxide layer. In addition, the electrical quality of the TaSiO_x can be evaluated on InGaAs after fabricating MOS-Cs with to benchmark parameters such as EOT, D_{it}, hysteresis, C_{max}/C_{min}, flat-band voltage (V_{FB}), inversion behaviour, frequency dispersion, fixed oxide charge as a function of process conditions namely pre-and post-deposition and metal annealing.

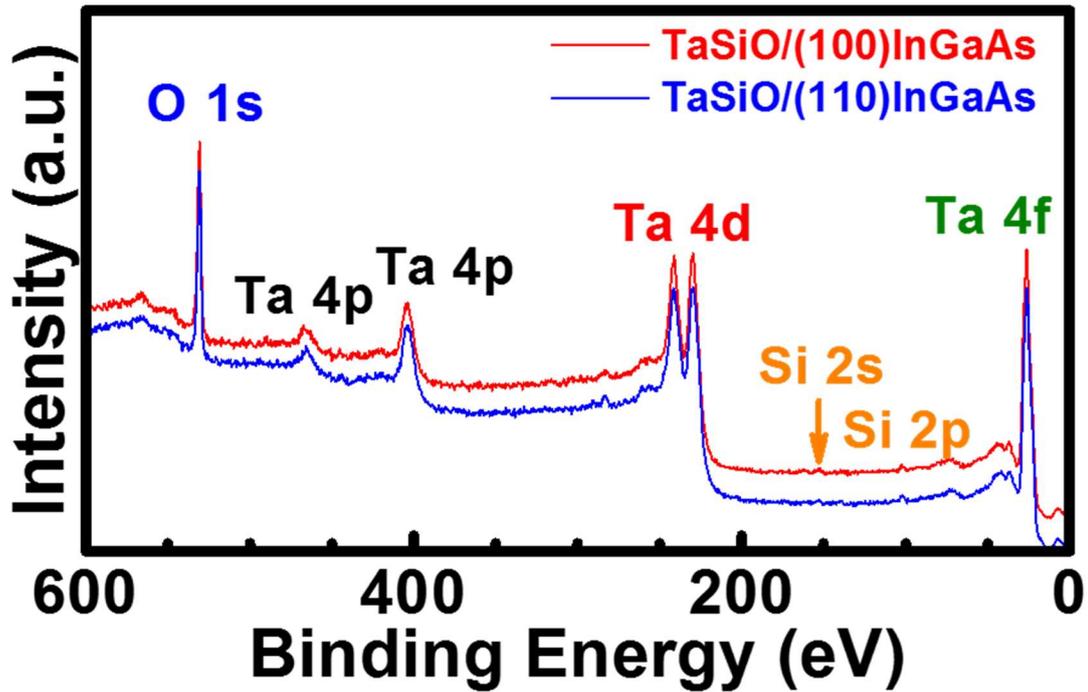


Fig. 5.2 Si incorporation observed *via* XPS surface surveys of TaSiO_x (100) InGaAs and (110) InGaAs. Both Si 2s and 2p peaks are evident.

5. 2 Band offset analysis of orientation dependent TaSiO_x/InGaAs interface

One of the most important considerations of selecting gate dielectric materials on InGaAs regarding the valence band and conduction band offset values, which should be larger than 1eV to block the carrier injection from the semiconductor to the insulator [12]. With respect to this, the integration of TaSiO_x on InGaAs active layer as well as understanding of the interfacial properties are vital for advancing further development of devices utilizing this system. In this section, detailed x-ray photoelectron spectroscopy (XPS) analysis was conducted to determine the orientation dependent band offset values of TaSiO_x on (100) and (110)InGaAs epitaxial layers. The crystallographic oriented InGaAs epitaxial layers were grown using solid source MBE

system on (100) and (110)InP substrates. During each layer growth, in-situ reflection high energy electron diffraction (RHEED) was used to monitor the surface. After the growth of each layer, films were characterized using x-ray diffraction for crystallinity and surface morphology by atomic force microscopy (AFM). After the deposition of TaSiO_x on crystallographic oriented (100) and (110)InGaAs epitaxial layers, the valence band offset (VBO) values were measured using Kraut's method [13]. The conduction band offset (CBO) values were calculated using the measured VBO values and the band gap energies of InGaAs and TaSiO_x, respectively.

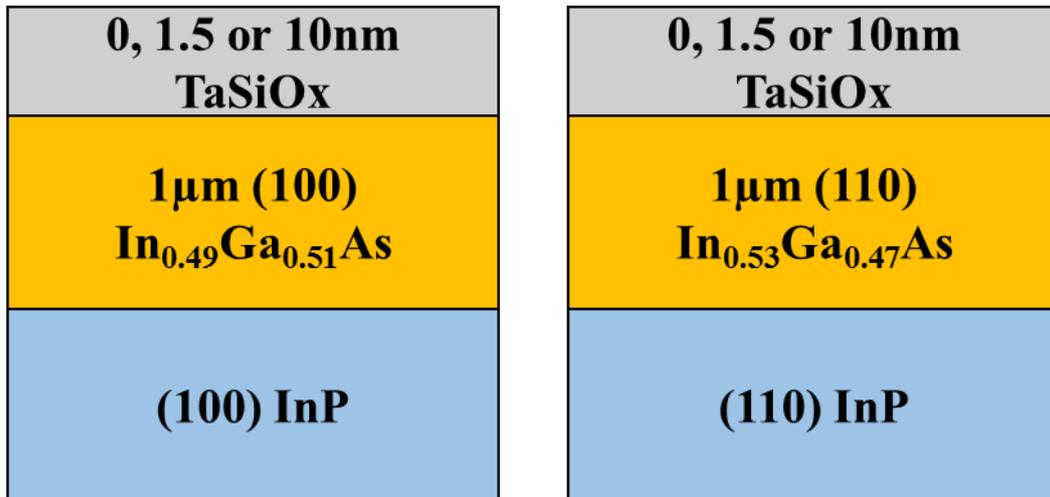


Fig. 5.3 Schematic diagram of high- κ dielectric TaSiO_x on integrated on two orientation (100) and (110) InGaAs for band alignment measurements

The band alignments of TaSiO_x on (100) and (110) InGaAs were investigated using the PHI Quantera SXM XPS system with a mono-chromated Al-K α (energy of 1486.7 eV) x-ray source. The VBO values between of TaSiO_x on (100) and (110) InGaAs were determined by measuring the binding energy from shallow core levels (CLs) of Ta4f and As3d and corresponding valence band maxima (VBM) from each material, respectively. The schematic diagram of the structures used in this study is shown in Fig. 5.3. As shown in Fig. 5.1, XPS spectra were collected from three samples

of each orientation: (1) 1.5nm TaSiO_x/1μm InGaAs was used to measure the CL binding energy of TaSiO_x/InGaAs interface; (2) 10nm TaSiO_x/1μm InGaAs was used to measure the CL binding energy of Ta and the VBM of TaSiO_x; (3) 1μm InGaAs without the top gate oxide layer was used to measure the CL binding energy of As and VBM of InGaAs. Native oxide on InGaAs surface was removed by a 10 minute (NH₄)₂S before loading into the XPS chamber. Sample charging occurred during XPS measurement and was a particular problem on the fully oxidized materials. Compensation of the charging by an electron flood source was used in all measurements to minimize the binding energy shift. Besides, the measured CLs and VBM binding energy values were corrected by shifting C1s CL peak to 285.0eV (however, this is not necessary to evaluate the band alignment). All XPS spectra were recorded using pass energy of 26eV and a step size of 0.025eV. Curve fitting was done by the CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background.

After collecting the binding energy information from each sample surface, the VBO value can be determined by Kraut's method:

$$\Delta E_V = [E_{CL}^{Oxide} - E_{VBM}^{Oxide}] - [E_{CL}^{InGaAs} - E_{VBM}^{InGaAs}] - [E_{CL}^{Oxide} - E_{CL}^{InGaAs}] \quad (5.1)$$

Where E_{CL}^{InGaAs} and E_{CL}^{Oxide} are the shallow CL binding energies of As3d and Ta4f, respectively. E_{VBM}^{InGaAs} and E_{VBM}^{Oxide} are the VBM of InGaAs and TaSiO_x, respectively.

This final correlates to:

$$\Delta E_V = [E_{Ta4f7/2}^{TaSiOx} - E_{VBM}^{TaSiOx}] - [E_{As3d5/2}^{InGaAs} - E_{VBM}^{InGaAs}] - [E_{Ta4f7/2}^{TaSiOx} - E_{As3d5/2}^{InGaAs}] \quad (5.2)$$

E_{VBM} of each material was determined by linearly fitting the leading edge of valence band spectra to the base line [12]. $\Delta E_{CL} = E_{CL}^{Oxide} - E_{CL}^{InGaAs}$ is the CL binding energy difference of Ta4f and As3d measured at the interface from 10nm TaSiO_x/1μm InGaAs

of each orientation. Once the VBO was obtained, the conduction band offset (CBO) can be estimated by:

$$\Delta E_C = E_G^{\text{TaSiO}_x} - \Delta E_V - E_G^{\text{InGaAs}} \quad (5.3)$$

Electronic excitations due to inelastic losses such as plasmon loss and band-to-band transitions in thin oxide films have been demonstrated to be characterized from photoemission signals appearing in the lower kinetic energy regime of primary core levels (O1s photoelectrons) [14-16]. And so, the bandgap of the oxide is determined by the onset (threshold) of the energy loss spectrum relative to the O1s spectrum.

Fig. 5.4 (a) and (b) show the non-carbon corrected Ta4f and VBM XPS spectra of 10 nm TaSiO_x/1μm (100) InGaAs, (c) and (d) show the non-carbon corrected As3d and VBM spectra of 1μm (100) InGaAs with no oxide, (e) and (f) show the non-carbon corrected Ta4f and As3d core level spectra from 1.5nm TaSiO_x/1μm (100) InGaAs at the interface, respectively. The determination of the bandgap of TaSiO_x taken as the onset of the loss peak and O1s core level is shown in Fig. 5.5(a) along with the resulting band alignment of TaSiO_x/ (100) In_{0.49}Ga_{0.53}As in Fig. 5.5 (b).

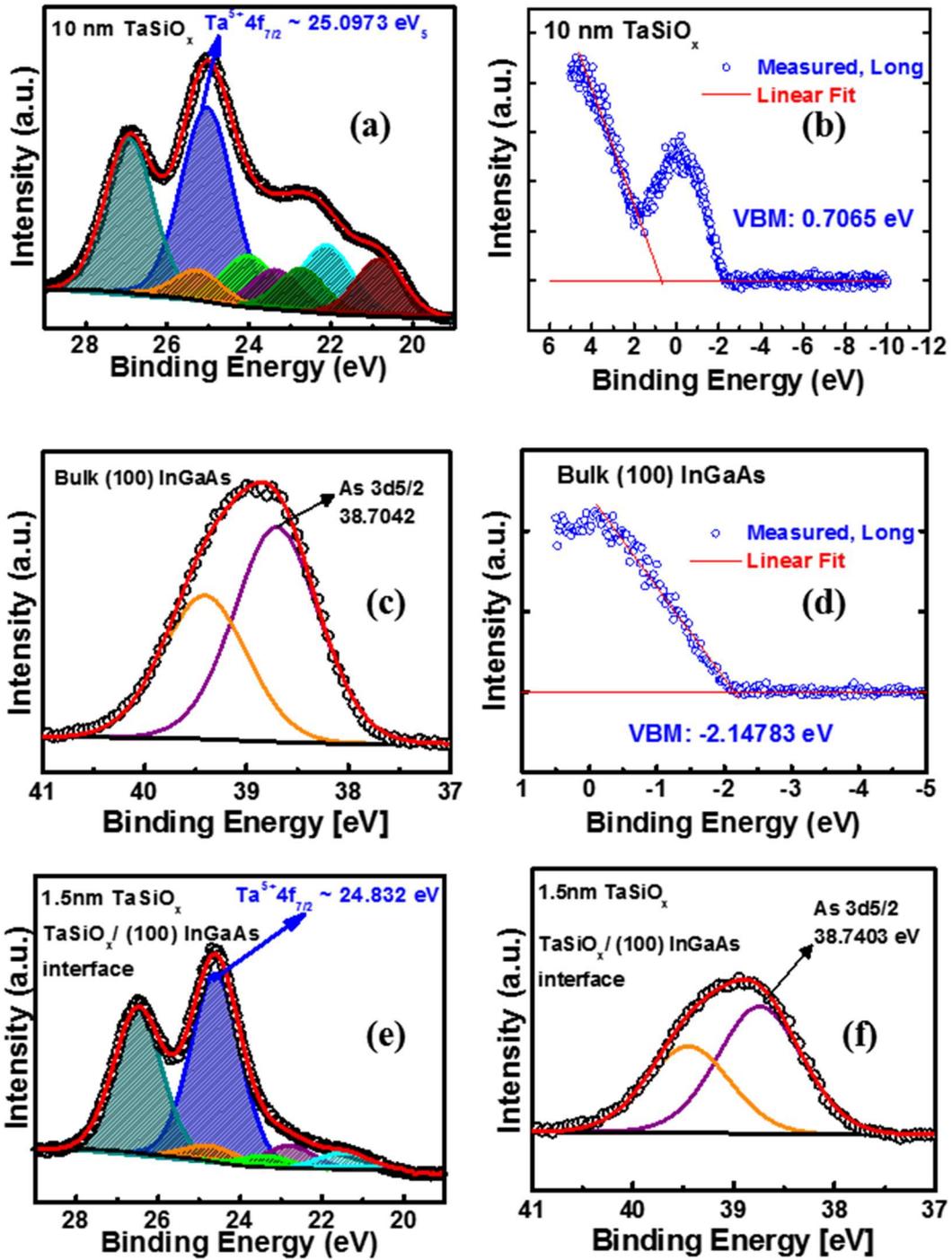


Fig. 5.4 (a) and (b) show the non-carbon corrected Ta4f and VBM XPS spectra of 10 nm TaSiO_x/1 μ m (100) InGaAs, (c) and (d) show the non-carbon corrected As3d and VBM spectra of 1 μ m (100) InGaAs with no oxide, (e) and (f) show the non-carbon corrected Ta4f and As3d core level spectra from 1.5nm TaSiO_x/1 μ m (100) InGaAs at the interface.

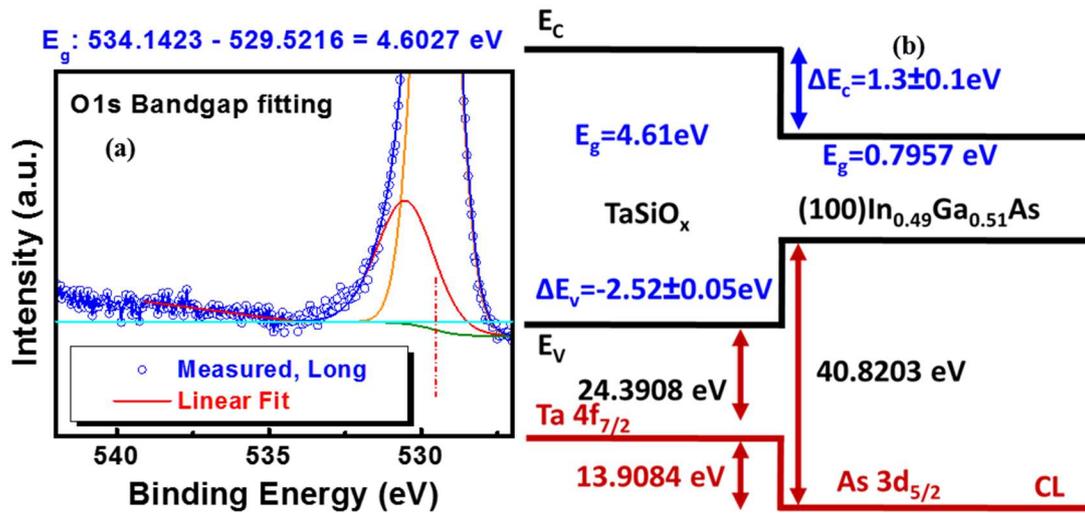


Fig. 5.5 (a) Determination of the bandgap of the dielectric deposited on (100) InGaAs as the onset (threshold) of the energy loss spectrum and the O1s core level. **(b)** Resulting band alignment of TaSiO_x/ (100) In_{0.49}Ga_{0.53}As

Fig. 5.6 (a) and (b) show the non-carbon corrected Ta4f and VBM XPS spectra of 10 nm TaSiO_x/1 μ m (110) InGaAs, (c) and (d) show the non-carbon corrected As3d and VBM spectra of 1 μ m (110) InGaAs with no oxide, (e) and (f) show the non-carbon corrected Ta4f and As3d core level spectra from 1.5nm TaSiO_x/1 μ m (110) InGaAs at the interface, respectively along with the resulting TaSiO_x bandgap determination and band alignment of TaSiO_x/ (110) In_{0.49}Ga_{0.53}As in Fig. 5.7 (a) and (b).

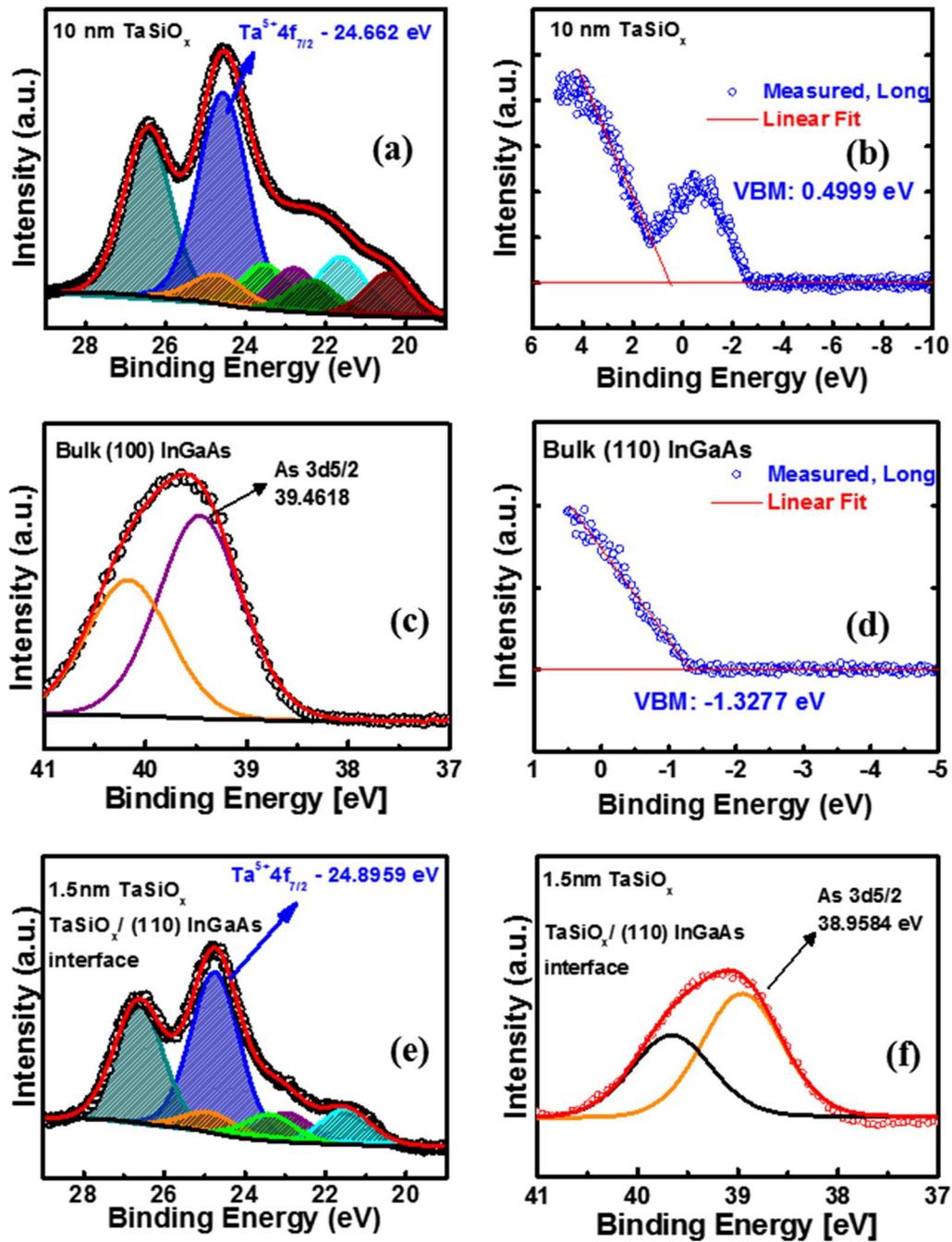


Fig. 5.6 (a) and (b) show the non-carbon corrected Ta4f and VBM XPS spectra of 10 nm TaSiO_x/1μm (110) InGaAs, (c) and (d) show the non-carbon corrected As3d and VBM spectra of 1μm (110) InGaAs with no oxide, (e) and (f) show the non-carbon corrected Ta4f and As3d core level spectra from 1.5nm TaSiO_x/1μm (110) InGaAs at the interface.

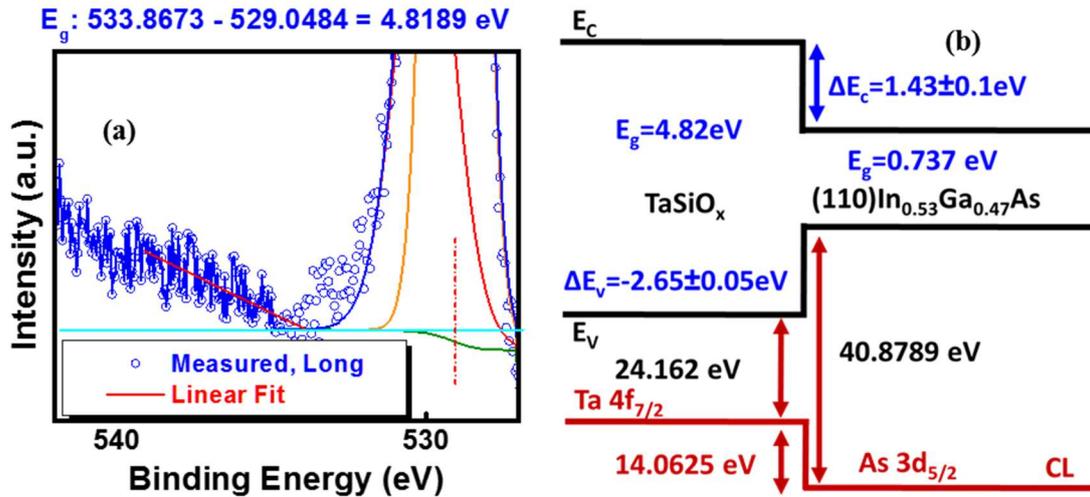


Fig. 5.7 (a) Determination of the bandgap of the dielectric deposited on (110) InGaAs as the onset (threshold) of the energy loss spectrum and the O1s core level. (b)

Resulting band alignment of TaSiO_x/ (110) In_{0.53}Ga_{0.47}As

	1.5 nm TaSiO _x	10 nm TaSiO _x	No TaSiO _x
(100) InGaAs	+1.6298 eV	+1.252 eV	+1.9636 eV
(110) InGaAs	+1.5343 eV	+1.6389 eV	+1.9465

Table 5.1 C1s Carbon correction obtained for XPS analysis

The resulting orientation dependent band alignment shows favorable confinement for n-channel InGaAs. It is to be noted that the incorporation of SiO₂ into Ta₂O₅ plays a crucial role in this. The theoretical conduction band offset (CBO) calculated based on vacuum and charge neutrality levels (CNL) of Ta₂O₅ on GaAs and InAs is 0.44eV and 1.46 eV respectively [17, 18]. With the electron affinities (χ) of GaAs, InAs, In_{0.53}Ga_{0.47}As and Si to be well established as 4.07eV, 4.9eV, 4.5eV 4.05eV and respectively [19]. Furthermore, the XPS investigation of the Si/SiO₂ interface yields a χ (SiO₂) as low as 0.9eV [20]. From Anderson's rule (which is rather crude and does not consider oxide/semiconductor interface polarity), the electron affinity of Ta₂O₅ is found to vary between 3.45-3.65 eV which would lead a $\Delta E_c \sim 0.9$ -1eV with In_{0.53}Ga_{0.47}As. However, the larger CBO obtained from the band alignment

studies performed on orientation dependent InGaAs yields higher CBO's which is a consequence of the incorporation of SiO₂ into Ta₂O₅ to reduce its electron affinity with the formation of TaSiO_x.

5.3 TaSiO_x deposition quality

In order to understand the TaSiO_x material quality which can affect the electrical transport characteristics of the InGaAs based MOS-Cs, a 10-minute (NH₄)₂S pre-clean was conducted to remove all native oxide species from the InGaAs surface followed by a preliminary TaSiO_x deposition to reduce the effect of native oxide regrowth during ALD. The requirement for thin oxide layers to reduce EOT leads to the vulnerability of increased gate leakage due to the increase in tunneling current. This tunneling current increases with increasing difference between the Fermi-levels of the semiconductor and metal [21]. However, depending on the polarity of the Fermi-level difference (if the Fermi-level of the semiconductor is below that of the metal), electrons from the metal can tunnel through the metal to occupy interface traps and instigate recombination leading to a loss of carriers. Furthermore, the formation of sub-oxides leads to the availability of oxygen vacancies in addition to the already existing surface (interface) states increases electron tunneling probability from the semiconductor (InGaAs) band to the metal gate [21, 22]. The existence of two spins for a given set of quantum numbers in fermions (except s-subshells) give rise to two possible states with a unique separation of binding energies. This is known as spin orbit splitting [23]. This gives rise to a relative ratio of areas between each doublet predetermined by its subshell (s, p, d or f). In the case of the f-subshell, the chemical species namely 4f_{7/2} and 4f_{5/2} have a corresponding area ratio of 3:4. With this, the fitting of sub-oxide peaks requires the constraint of spin orbital splitting between Ta4f_{5/2} and Ta4f_{7/2} orbitals ~ 1.9 eV with

the lower spin component taking the higher binding energy [24-26]. As mentioned earlier, the quality of an oxide is determined by the presence of native sub-oxides formed due to unfavorable deposition conditions. The most stable form of a tantalum based oxide is Ta_2O_5 exhibiting an oxidation state (O.S) of 5^+ . The average binding energy of $Ta^{5+}4f_{7/2}$ is 26.2 eV with that of pure Ta metal (0 oxidation state) ranging between 21.6 and 22.2 eV [24-28]. Inter oxidation state spacing was shown to vary between 0.9-1.3 eV and FWHM between 1.4 eV and 2.3 eV for the chemical species of Ta_2O_5 [24-28]. Thus resulting in a Ta 4f spectrum \sim 4.6-5.6 eV depending on the shift of the $Ta^{5+}4f_{7/2}$ species to higher binding energies. Fig. 5.8 shows the Ta4f spectrum of the carbon-corrected 1.5 nm $TaSiO_x/(100)$ InGaAs interface. The FWHM in this case is constrained between 1.4 - 1.6eV. The resulting data of peak position, FWHM and relative peak intensity of the sub-oxides formed is tabulated in table 5.2.

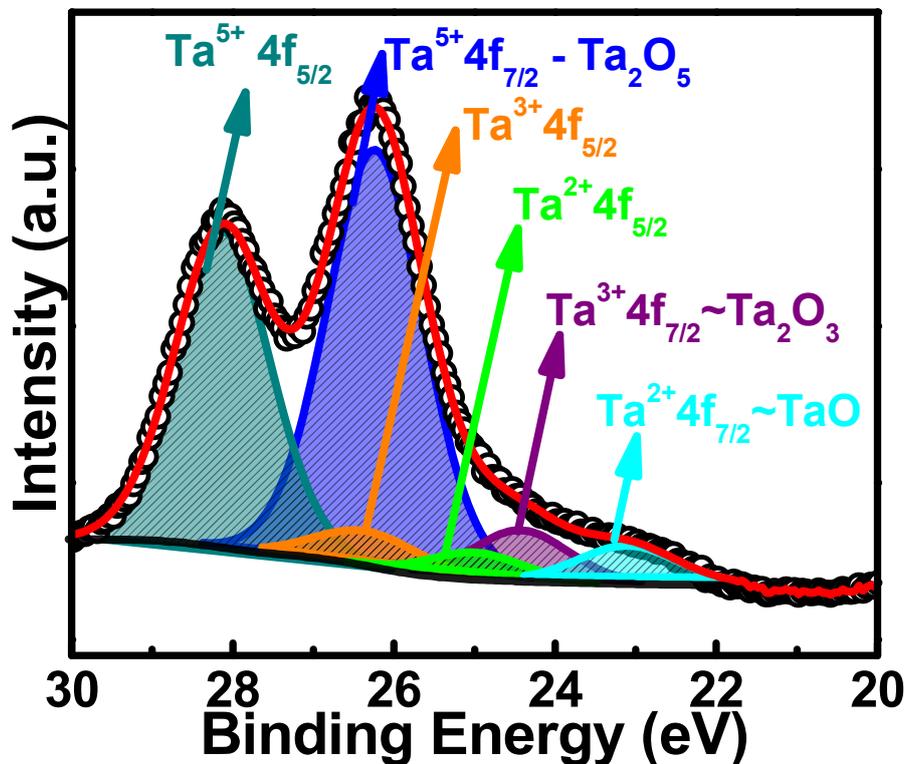


Fig. 5.8 Ta4f spectrum of the 1.5 nm $TaSiO_x/(100)$ InGaAs

	Peak (eV)	FWHM (eV)	Relative Intensity
Ta ²⁺ 4f _{7/2}	23.0944	1.49	0.192
Ta ³⁺ 4f _{7/2}	24.4248	1.4	0.224
Ta ²⁺ 4f _{5/2}	24.9944	1.41	0.178
Ta ⁵⁺ 4f _{7/2}	26.2287	1.42	1
Ta ³⁺ 4f _{5/2}	26.3248	1.55	0.22
Ta ⁵⁺ 4f _{5/2}	28.1287	1.4	0.836

Table 5.2 Peak parameters of Ta4f spectrum of the carbon-corrected 1.5 nm TaSiO_x/ (100) InGaAs interface.

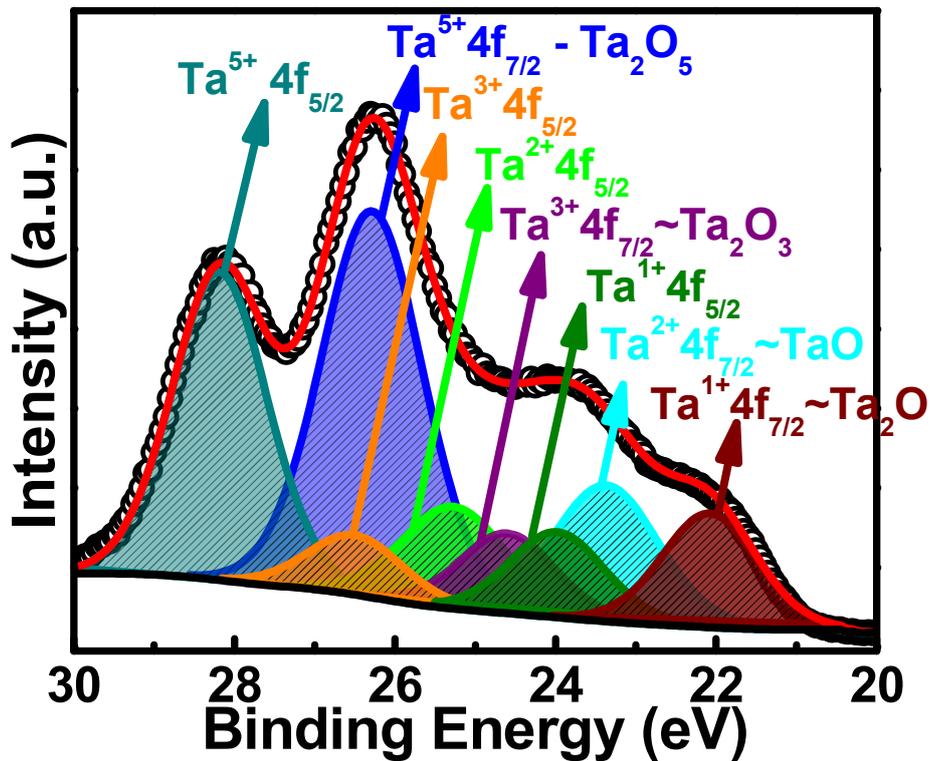


Fig. 5.9 Ta4f spectrum of the carbon-corrected 10 nm TaSiO_x/ (100) InGaAs interface depicting the formation of sub-oxides.

The formation of sub-oxides is detected, however the relative intensity is shown to be rather low. The 10 nm TaSiO_x/ (100) InGaAs Ta4f spectrum is shown in Fig. 5.9 with peak parameters compiled in Table 5.3.

The formation of sub-oxides is amplified in the thicker oxide with the domination of lower oxidations states exhibiting higher relative intensities. This could pronounce to a higher density of oxygen vacancies corresponding to a larger leakage density for a given field. There is significant formation of more metastable sub-oxides in the bulk oxide as compared TaSiO_x/InGaAs interface despite uniform deposition conditions. An appropriate annealing scheme, must be developed to reduce native oxide formation. A high temperature N₂ anneal has been shown to reduce tantalum based sub-oxides improving the stoichiometry of the oxide [27].

	Peak (eV)	FWHM (eV)	Relative Intensity
Ta ¹⁺ 4f _{7/2}	22.0793	1.4	0.306
Ta ²⁺ 4f _{7/2}	23.3698	1.53	0.371
Ta ¹⁺ 4f _{7/2}	23.9793	1.4	0.26
Ta ²⁺ 4f _{5/2}	25.2698	1.53	0.32
Ta ³⁺ 4f _{7/2}	24.5943	1.4	0.259
Ta ⁵⁺ 4f _{7/2}	26.2831	1.49	1
Ta ³⁺ 4f _{5/2}	26.4943	1.4	0.257
Ta ⁵⁺ 4f _{5/2}	28.1831	1.4	0.86

Table 5.3 Peak parameters of Ta4f spectrum of the carbon-corrected 10 nm TaSiO_x/ (100) InGaAs interface.

In the previous section, we observed a distinct variation in the band alignment and bandgap of TaSiO_x/InGaAs. This could be correlated to the orientation dependent

incorporation of silicon at the interface. The large bandgap obtained is more suited to the requirement for narrow fins to address short channel effects as discussed earlier in this work. We will now analyze the oxide quality of the TaSiO_x/ (110) InGaAs. Fig. 5.10 and is the Ta4f spectrum of the carbon-corrected 1.5 nm TaSiO_x/ (110) InGaAs interface depicting the formation of sub-oxides. The resulting interfacial quality is similar to that obtained in the TaSiO_x/ (100) InGaAs interface. The peak parameters of the Ta4f spectrum is compiled in table 5.4. Fig. 5.11 and is the Ta4f spectrum of the carbon-corrected 10 nm TaSiO_x/ (110) InGaAs with corresponding parameters compiled in Table 5.5.

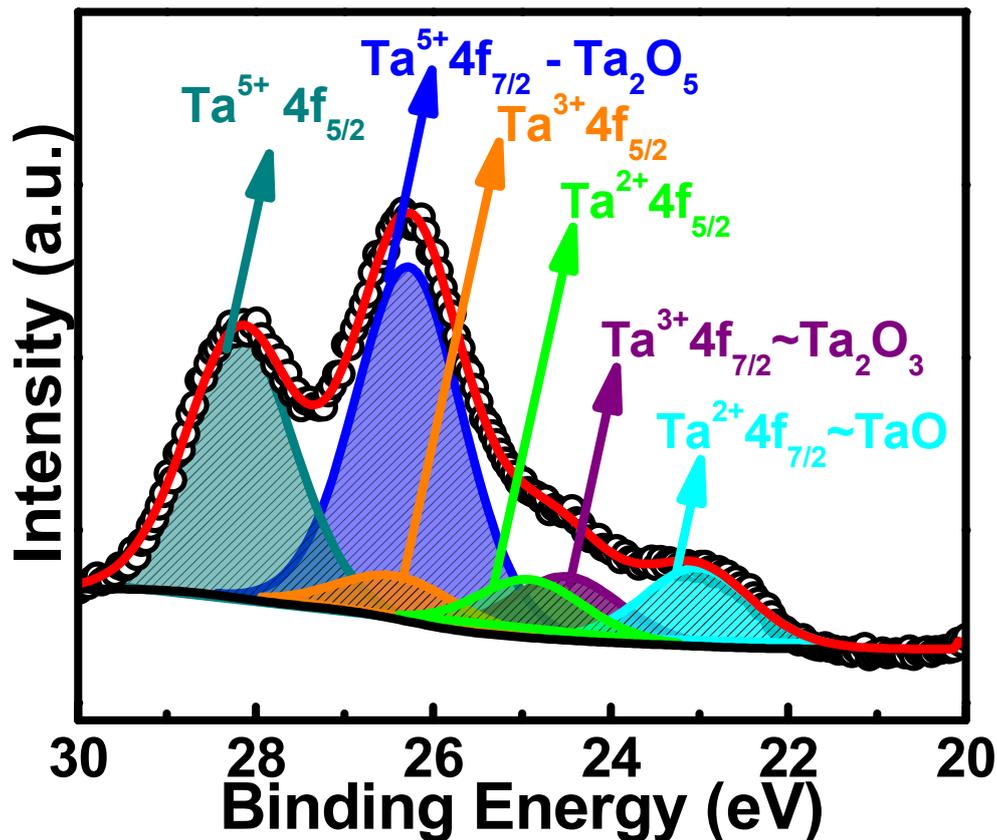


Fig. 5.10 Ta4f spectrum of the 1.5 nm TaSiO_x/ (110) InGaAs depicting the formation of sub-oxides at the interface.

	Peak (eV)	FWHM (eV)	Relative Intensity
$\text{Ta}^{2+}4f_{7/2}$	23.0944	1.46	0.309
$\text{Ta}^{3+}4f_{7/2}$	24.491	1.44	0.29
$\text{Ta}^{2+}4f_{5/2}$	24.9944	1.47	0.283
$\text{Ta}^{5+}4f_{7/2}$	26.2707	1.43	1
$\text{Ta}^{3+}4f_{5/2}$	26.3941	1.6	0.29
$\text{Ta}^{5+}4f_{5/2}$	28.1707	1.43	0.85

Table 5.4 Peak parameters of Ta4f spectrum of the carbon-corrected 1.5 nm TaSiO_x/ (110) InGaAs interface.

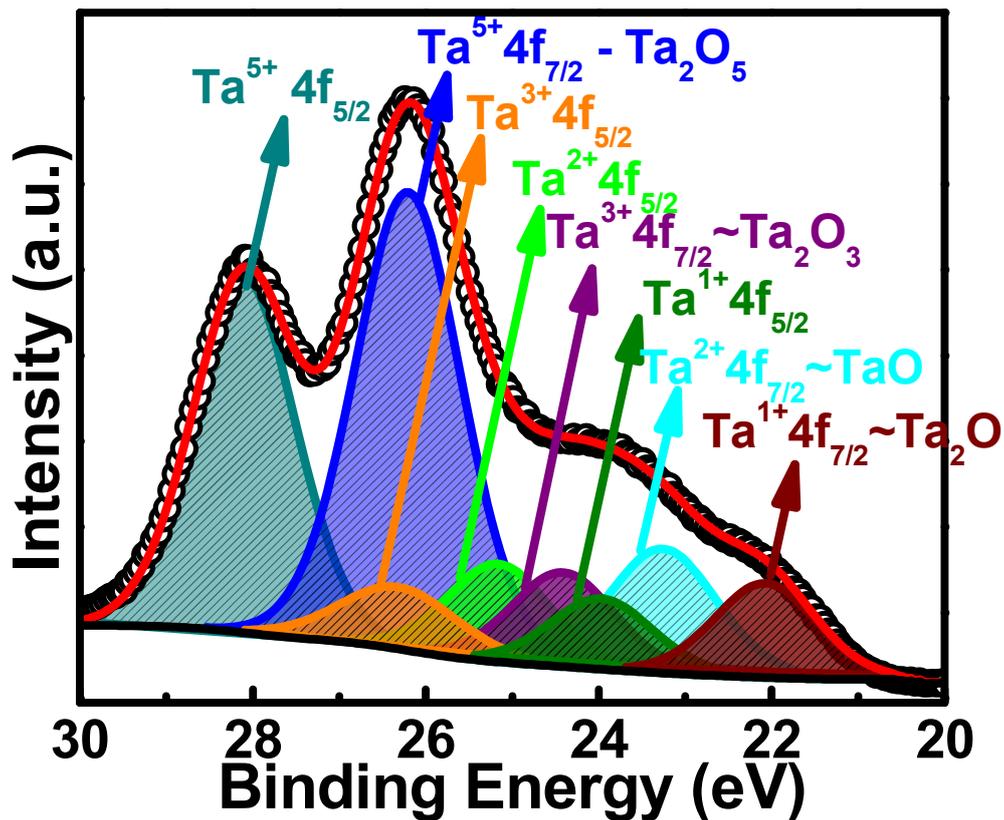


Fig. 5.11 Ta4f spectrum of the carbon-corrected 10 nm TaSiO_x/ (110) InGaAs interface depicting the formation of sub-oxides in the bulk of the oxide.

An improvement, if not significant, is observed with lower relative intensities of sub-oxides of all metastable states. This could be due to the difference in surface quality resulting from the $(\text{NH}_4)_2\text{S}$ pre-clean on two different orientations prior to deposition. Narrower and more distinct peaks are also observed with a more consistent FWHM.

	Peak (eV)	FWHM (eV)	Relative Intensity
Ta¹⁺4f_{7/2}	22.0699	1.4	0.227
Ta²⁺4f_{7/2}	23.2591	1.47	0.295
Ta¹⁺4f_{7/2}	23.9699	1.4	0.197
Ta²⁺4f_{5/2}	25.1591	1.4	0.265
Ta³⁺4f_{7/2}	24.4138	1.4	0.249
Ta⁵⁺4f_{7/2}	26.201	1.45	1
Ta³⁺4f_{5/2}	26.3138	1.46	0.221
Ta⁵⁺4f_{5/2}	28.101	1.4	0.832

Table 5.5 Peak parameters of Ta4f spectrum of the carbon-corrected 10 nm TaSiO_x/ (110) InGaAs interface.

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Chapter 6 – Conclusions and Future prospects

6.1 Summary

The material system consisting of epitaxial $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ heterogeneously integrated on Si substrate *via* a composite large bandgap $\text{In}_x\text{Al}_{1-x}\text{As}/\text{GaAs}$ buffer with overshoot ($x: 0.52 \rightarrow 0.7 \rightarrow 0.52$) to ensure buffer relaxation and mitigate defects away from the active layer, has recently been demonstrated as a novel solution for future high-speed CMOS logic applications. The low bandgap and high mobility of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ coupled with the lattice-matched, large bandgap nature of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ bottom barrier resulting from the $\text{In}_x\text{Al}_{1-x}\text{As}/\text{GaAs}$ buffer are promising for the development of high-speed MOSFETs operating within the low-power ($V_{DD} < 0.5 \text{ V}$) regime. Furthermore, the adoption of the FinFET design utilizing the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_x\text{Al}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ heterostructure, offers further improvement for I_{ON} while maintaining superior electrostatic gate control and reliable device operation with the utilization of highly scaled TaSiO_x as gate dielectric ($EOT=12\text{\AA}$), which becomes especially necessary with the aggressive trend in CMOS scaling. In this research, the existing device data employing the material system mentioned above is calibrated to predict the interfacial properties of $\text{TaSiO}_x/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ were comprehensively investigated with results summarized below:

- (1) The model whose device structure employed an ultra-low gate-source gate-drain separation of $L_{SIDE}=5\text{nm}$ with highly scaled TaSiO_x ($EOT=12\text{\AA}$), was calibrated to reciprocate:
 - i. Gate electrostatics (C-V) of the $W_{FIN}=45\text{nm}$ fin structure.
 - ii. Transfer characteristics of the $L_G=60\text{nm}$ device with unity aspect ratio $W_{FIN}=H_{FIN}=40\text{nm}$ to gain insight on device mobility and resistance.
 - iii. Dimensional influence of lateral and vertical scaling of the fin on short channel effects like subthreshold slope (SS) and Drain Induced Barrier Lowering (DIBL).

The calibration of the factors mentioned above requires the development of a consistent D_{it} distribution of the $TaSiO_x/In_{0.53}Ga_{0.47}As$ interface which allows for correlating results mentioned above.

- (2) The calibrated model was extended to study the dimensional response of the fin structure on short channel effects to gain insight on design rules to help reduce short channel effects with gate length scaling.
- (3) Assuming transferable interfacial quality, the model was scaled down to $L_G=10nm$ with appropriate quantization effects of the fin structure (MLDA) to project short channel effects for the 10 nm node. The short channel device has shown to outperform other demonstrated long channel architectures with the same alloy composition.
- (4) Orientation dependant band alignment studies of $TaSiO_x$ on (100) and (110) InGaAs were conducted to further confirm the incorporation of SiO_2 into Ta_2O_5 based on the change in the electron affinity to increase the CBO of $TaSiO_x/InGaAs$ making it suitable for integration on n-channel materials. The investigation further lead to obtain a larger bandgap in the (110) plane which is favourable for the development of tall and narrow fin structures with improved carrier confinement.

6.2 Prospects for future research

Further improvement can be extended with extended scaling of the $TaSiO_x$ gate stack to reduce EOT while maintaining low gate leakage (J_G) and with the reduction of D_{it} levels to compete with those as observed in Si-based devices. The $TaSiO_x/InGaAs$ interface has also been used to demonstrate a record low $SS < 60mV/decade$ on a III-V Heterojunction Tunnel Field Effect Transistor (H-TFET) [1].

The development of an annealing scheme for $TaSiO_x$ will play a crucial role along with the utilization of plasma enhanced ALD which allows for more freedom in processing conditions and a wider range of material properties when compared to

conventional thermal ALD. Despite the superior interfacial properties of TaSiO_x/InGaAs, the implementation of TaSiO_x on Germanium (Ge) will play a crucial role in the incorporation of a common dielectric on a III-V/ Ge alternate CMOS system.

This can be made possible by the development of an optimized process to fabricate MOS-C's of orientation dependent Ge and InGaAs to study the resulting gate electrostatics and D_{it} distribution of TaSiO_x on various orientations of Ge and InGaAs. A detailed investigation of the properties of TaSiO_x (E_g, ε/EOT, and χ) based on the incorporation of Si into TaSiO_x with the utilization of chlorine-free precursors will play a crucial role for this. This will allow for a common gate oxide for the integration of alternate channel CMOS on Si.

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