Comparison and Design of High Efficiency Microinverters for Photovoltaic Applications

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Abstract

With the decrease in availability of non-renewable energy sources coupled with the increase in the amount of energy required for the operation of personal electronic devices there has been an increased focus on developing systems that take advantage of renewable energy sources. Renewal energy sources such as photovoltaic (PV) panels have become more popular due to recent developments in PV panel manufacturing that decreases material costs and improves energy harvesting efficiency. Since PV sources are DC sources power conversion stages have to be used in order to interface this power to the existing electrical utility system.

The structure of large scale PV systems usually consists of several PV panels connected in series to achieve a high input source voltage that can be fed into a high power centralized DC-AC inverter. The drawback to this approach is that when the PV panels are subjected to less than ideal conditions. If a single PV panel is subjected to drastically less solar irradiation during cloud conditions, then its output power will drop dramatically. Since this panel is series connected with the other PV panels, their current output is also dragged low decreasing the power output of the system. Algorithms that have the power converter operate at different input conditions allow the system to operate at a maximum power point (MPP), however this only allows the system to operate at a higher power point and not the true MPP.

To get around this limitation a new PV system implementation was created by giving each panel its own DC-AC power conversion system. This configuration gives each panel the ability to operate at its own MPP increasing the total system energy harvest. Another advantage of the single panel DC-AC microinverter power conversion stage is that the outputs are parallel connected to the utility grid easily allowing the ability to expand the system without having to shut down the entire system.

The most prevalent implementation of the microinverter consists of a single power converter that uses the PV low voltage DC and outputs high voltage AC. In order to ensure that the double line AC ripple does not propagate to the PV panel a large bank of electrolytic capacitors are used to buffer the ripple. There is concern that the electrolytic capacitor will degrade over time and affect the system efficiency. To get around having to use electrolytic capacitors a two stage microinverter has been proposed. The two stage microinverter consists of a DC-DC converter that steps up the low DC voltage

of the PV panel to high voltage DC and the second stage is a DC-AC inverter that takes the high voltage DC and converts it to high voltage AC. There is a capacitor that connects the two power converter stages called the DC link capacitor which can buffer the double line energy ripple without using electrolytic capacitors.

This thesis focuses on the review of several DC-AC inverter topologies suitable for use in PV microinverter systems. Operation capabilities such as common mode noise and efficiency are compared. The main focus of the review is to determine the optimal DC-AC inverter using the performance metrics of cost, efficiency and common mode performance. A 250 W prototype is built for each inverter topology to verify its performance and operation.

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1 INTRODUCTION

Over the past decade there has been a rapid increase in the development of devices that are dependent on electricity in order to simplify human activities. With the expanding human population comes an even larger increased number of electronic devices. Traditionally most the energy provided to consumers is generated using non-renewable energy sources such as coal and petroleum whose supply will eventually become exhausted with continued human population expansion [1]. Concern for the availability of energy in the future has driven the increased adoption of renewable energy sources. One of the fastest increasing renewable energy sources is photovoltaic (PV) which has gone from 804 GWh in 2000 to 12,775 GWh in 2012 for the U.S. alone [2]. Government programs have helped to facilitate the adoption of PV generation systems by creating initiatives such as the DOE SunShot Initiative whose focus is on reducing the cost to generate power using PV through technological advancements. The cost of utility scale PV projects in the United States have dropped from 21.4 c/kWh in 2010 to 11.2 c/kWh in 2013 [3].

1.1 PV STRING INVERTER

PV panels are a DC power source and in order to interface the power that is generated by the panel to the utility grid a power electronics conversion circuit is required. A common configuration to integrate the PV panels into the grid is to series several panel to create a high voltage bus this is commonly called a PV string. The PV string is then fed into a centralized high power inverter that is around 3 -5 kW power rating, this configuration shown in Figure 1.1 is called a string inverter configuration [4].

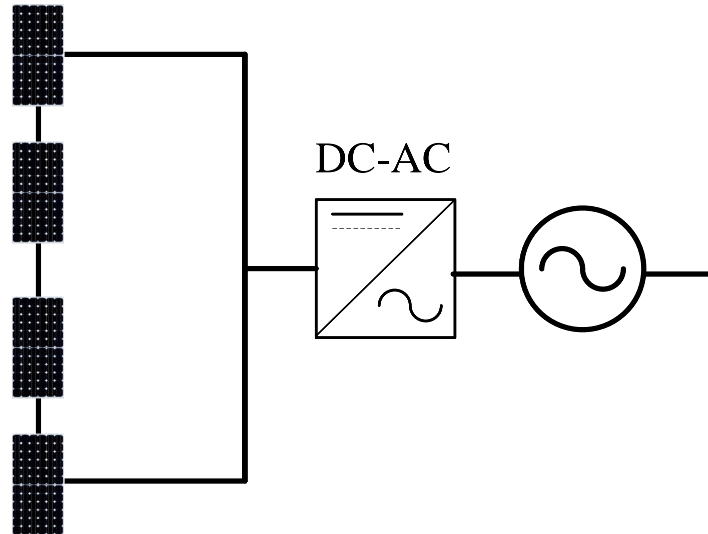


Figure 1.1: PV String Inverter Configuration

The problem with this configuration is that when there are adverse operating conditions such that one of the panels does not receive the maximum amount of irradiation causing the output current to decrease. The series configuration of the panels causes the total output current of the string to decrease limiting the power that can be produced. To get around this limitation there has been the development of control algorithms where the inverter controls the input voltage and as a result it can track the maximum power point (MPP) of the PV string. Using the inverter to implement the MPPT algorithm improves the energy harvest of the string, however it cannot truly track the MPP of each panel due to the series configuration.

1.2 Centralized Inverter with Power Optimizers

In order to improve the MPP tracking capability another PV system configuration has been proposed where each PV panel has its own DC-DC converter called a power optimizer whose output is connected in parallel as shown in Figure 1.2.

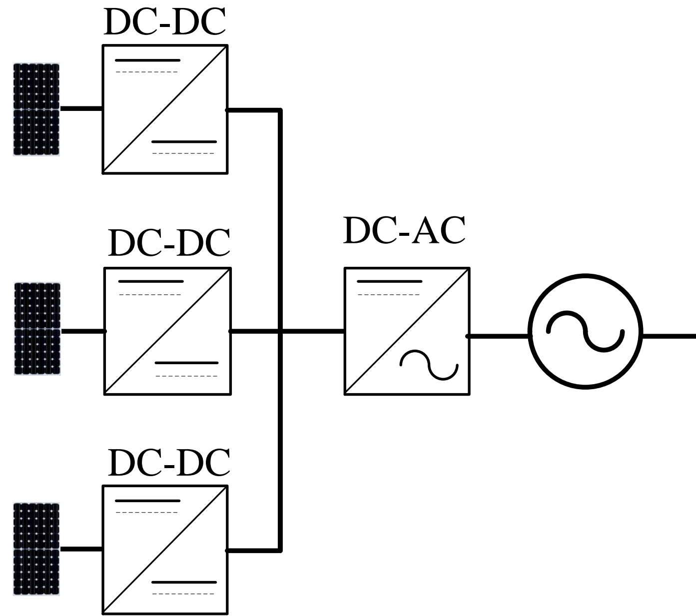


Figure 1.2: Centralized Inverter with Parallel Power Optimizers

The purpose of the power optimizer is to implement MPPT and to step up the PV panel voltage to a level that the inverter can use to operate [5]. The advantage of this system is that each panel can operate at its own MPP and not affect the other panels in the system. The disadvantage of this configuration is the increased costs of the optimizers and inability to expand the size of the system without adding additional centralized inverters.

1.3 Microinverter

A way to address the non-modularity of the power optimizer configuration is instead of having a single centralized high power inverter each panel will have its own inverter rated for the power of the PV panel. The output of each low power inverter can be connected directly to the AC grid in parallel, this configuration shown in Figure 1.3 with each individual unit referred to as a microinverter.

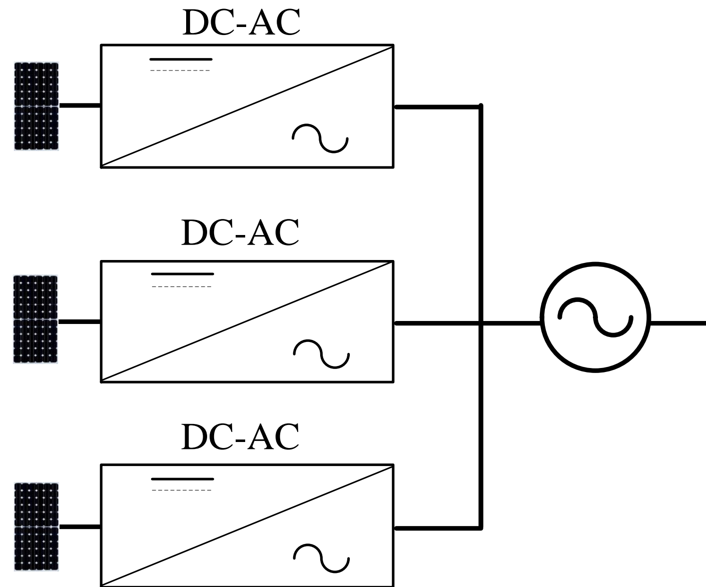


Figure 1.3: Several Microinverters Connected in Parallel

Each PV panel has the ability to run at its own MPP and the end user is able to increase the size of the PV system without having to add additional high power inverters with power optimizers. With the increased adoption of microinverters in PV systems there has been an increasing demand in reducing the costs of these systems in order to make system installation more attractive for prospective users [6]. In order to be cost effective there has been the establishment of the single stage microinverters.

1.3.1 Single-Stage Microinverters

Single-stage microinverters allow integration of DC renewables into the utility system with the simplest structure allowable [7]. The single-stage microinverter configuration consists of a buck-boost type converter using half wave SPWM and a full bridge unfolder to convert the half wave sinusoidal to full wave sinusoidal [8],[9]. The most widely used commercial single-stage microinverter is the M250 from Enphase, shown in Figure 1.4, which consists of interleaved quasi-resonant flyback converters and a full bridge thyristor unfolder with a California Energy Commission (CEC) efficiency of 96.5% [10], [11].

Figure 1.4 Enphase 250 W Single-Stage Microinverter

The simplicity of the single stage implementation comes with one caveat, there has to be high capacitance at the PV side in order to filter out the double line voltage ripple. The only way to achieve that high capacitance is to use electrolytic capacitors. The downside to using electrolytic capacitors is that the microinverter is located outdoors in potential harsh environmental climates causing increased degradation of the electrolytic capacitors. Increased maintenance is cost prohibitive for a PV system and as a result PV microinverters should have the same reliability as the life of the panel, which has been approximated to 20 years [12].

1.3.2 Two-stage Microinverters

In order to address the reliability issue of electrolytic capacitors the two-stage microinverter has been proposed, which allows the double line voltage ripple to be buffered in the dc link capacitor [13], [14]. The configuration of two-stage microinverter consists of a boost type dc-dc converter to step up the PV voltage to a high voltage for the primary stage and a dc-ac inverter to transform the high voltage dc to grid voltage [15]. Two-stage microinverters can be isolated or non-isolated; however, isolation is preferred due to safety in installations and affords the use of inverter topologies that generate higher common mode noise. Most popular two-stage microinverters are from Power One and SolarBridge. The SolarBridge Pantheon II microinverter consists of a current-fed full bridge converter to step up the PV

voltage and a unipolar full bridge inverter with reverse recovery avoidance [16], [17]. The CEC efficiency of the Pantheon II is 95%, which is low compared to the Enphase M250 [18]. The Aurora Micro from Power One, shown in Figure 1.5, has a CEC efficiency of 96% and uses interleaved quasi-resonant flyback converters for the dc-dc step up stage and an asynchronous unipolar dual-buck inverter for the second stage [19], [20].

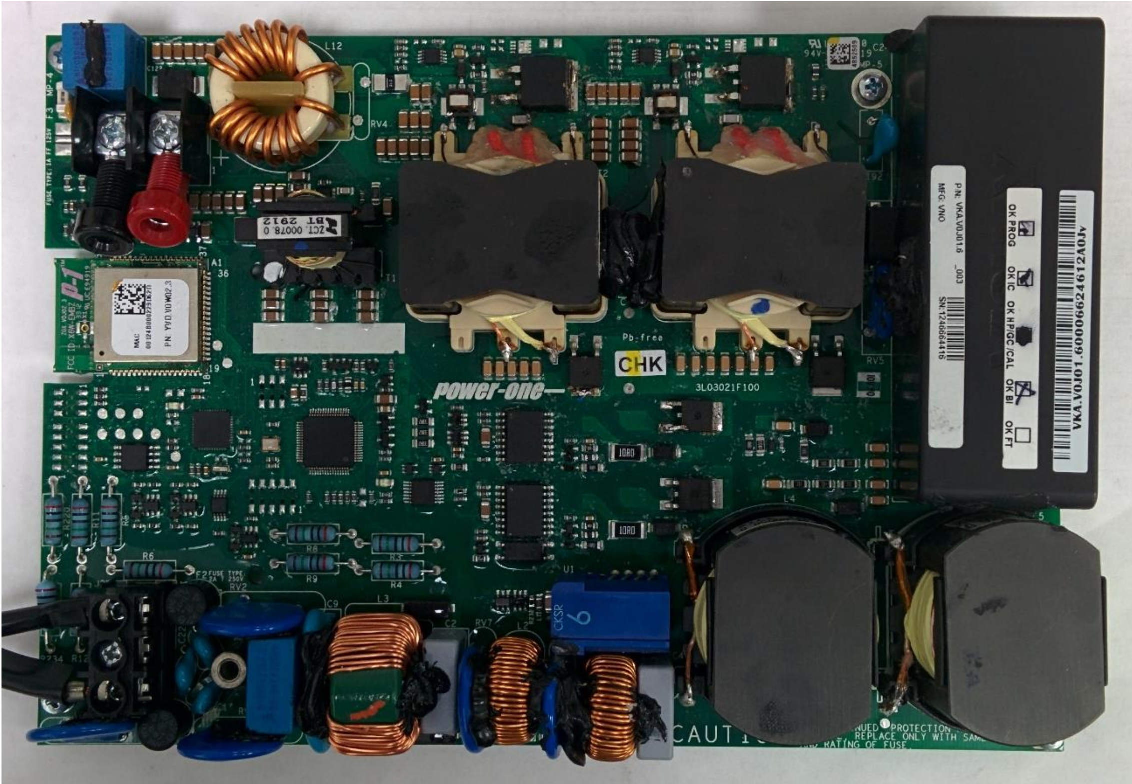


Figure 1.5: Power One 300 W Two-Stage Microinverter

The main drawback of the two-stage microinverter is that it is more difficult to achieve high system efficiency due to the losses in both power conversion stages. In order to have high system efficiency there has to be an emphasis on designing high efficiency dc-dc converters for the primary stage and high efficiency dc-ac inverters for the second stage.

1.4 Common Mode Noise

Evolution of inverter topologies and modulation schemes have come about as the result of two major goals; increasing efficiency and reduction of common mode (CM) noise. With improvements in semiconductor materials, semiconductor processing, and magnetic materials it has become easier to achieve high efficiency. CM noise reduction relies more on the inverter topology as well as the inverter system design and fabrication.

It is important to understand what the difference between what CM and differential mode (DM) signals are and how they affect electronic systems. DM noise follows the same direction as the input power. An example of a DM network consists of a pair of transmission lines and a resistive load as shown in Figure 1.6.

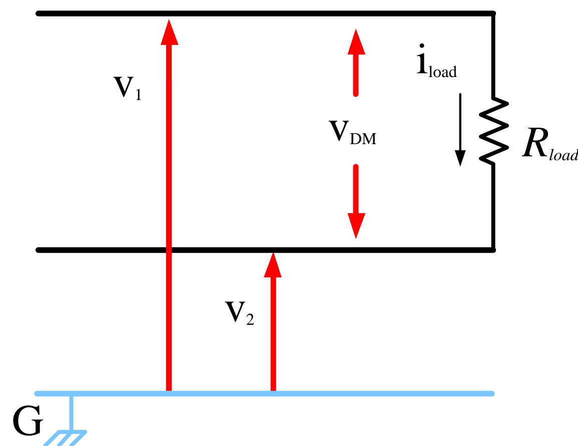


Figure 1.6: Differential Mode Signal Network

For a pure differential network the voltages V_1 and V_2 have the same magnitude with a phase difference of 180° [21], [22]. The resulting differential voltage V_{DM} can be determined to be

$$V_{DM} = V_1 - V_2$$

As long as both voltages are the same when referenced to the same ground then no current flows to ground and all current goes to the load. For the case of CM noise there are parasitic capacitive elements that connect each transmission line to the ground potential. The direction of CM noise is in the same direction referenced to the other signal going to the ground potential as shown is Figure 1.7.

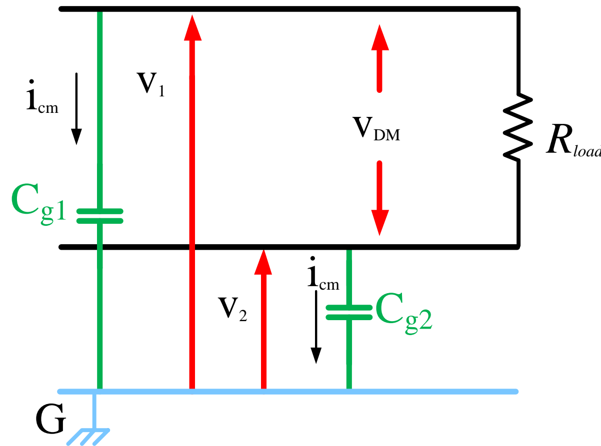


Figure 1.7: Common Mode Signal Network

In the case of a pure CM network the voltages V_1 and V_2 have the same magnitude with no phase difference this means that the $V_{DM} = 0$ [21], [22]. Since there is no voltage across the load there is no current going through R_{load} and all the current travels through the parasitic capacitance to ground. With there being a potential across the parasitic capacitances referenced to ground there is a resulting generation of electromagnetic radiation. This radiation is usually referred to a ground leakage current. If the leakage current magnitude is sufficient enough it can damage other electrical systems as well as pose a hazard to utility workers that are working on systems connected to the same ground potential.

There are two main areas of concern relating to the CM noise in a microinverter system, the CM loop path and the sources of CM noise. The CM loop paths for microinverter systems are roughly going to be the same regardless of topology and are more dependent on whether or not the system has galvanic isolation. The parasitic capacitive elements for a generic two-stage isolated microinverter system are illustrated in Figure 1.8.

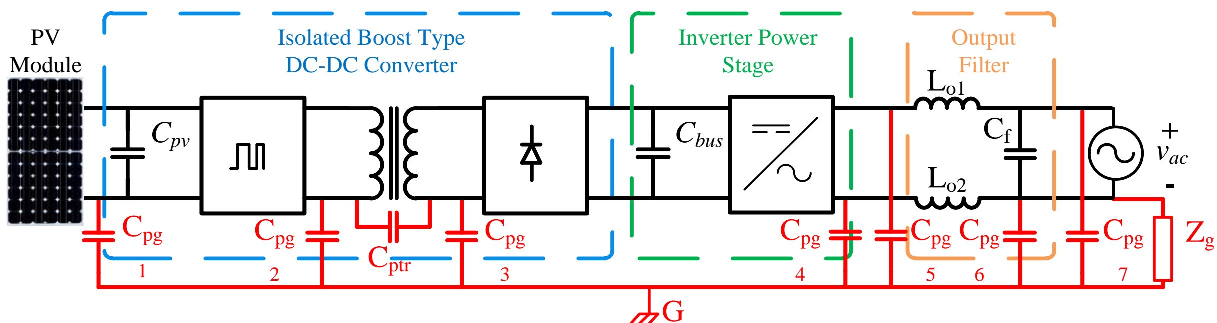


Figure 1.8: Common Mode Ground Loops for Two-Stage Isolated Microinverter

The main difference in the configuration of the isolated and non-isolated two stage microinverter is the presence of the parasitic capacitance C_{ptr}, connecting the primary and secondary of the isolation transformer. In the case of the non-isolated microinverter this capacitance is essentially shorted and the CM noise can travel unimpeded back to the primary DC-DC stage. For the isolated DC-DC stage this capacitance can actually help block the CM noise from going into the primary DC-DC stage. This is possible due to the small value of C_{ptr}, which is high impedance for most CM signals. If isolation is used in the DC-DC stage inverters with higher CM and higher efficiency can be utilized. In the event that the DC-DC converter is not isolated then inverter topologies with low CM noise have to be utilized.

The parasitic stray capacitances to the earth ground reference are represented with C_{pg1}-C_{pg7}. These capacitances value in the picoFarad (pF) range and can be low impedance for signals in the tens to hundreds of kHz or higher. The utility grid is connected to the ground through an inductive impedance Z_g, whose value is very low and could be considered as a short.

The major sources of CM noise are from the switching elements of the system. The noise from the switching elements can be further broken down into two parts, the first is the noise from the switching frequency itself and the second is from the transition itself [23]. The switching frequency for most power conversion systems in this power level go from tens to several hundred kHz, the main purpose of the output filters, input and output capacitance are designed to attenuate this noise. Noise from the switching transitions can induce the most leakage current due to the high difference in voltage over time (dV/dt) [24]. The output filter cannot handle this noise and additional electromagnetic interference (EMI) filter components are required to attenuate the noise. The stray capacitances that would experience the highest CM noise would those connected to switching nodes which include C_{pg2}-C_{pg5}, if their values are kept symmetrical with a low value then the CM noise effects could be minimized.

1.5 Goal and Scope of Thesis

This thesis will cover the analysis of several topologies that are candidates to achieve high efficiency for the DC-AC inverter portion of the two-stage microinverter system. The mode of operation for each inverter will be discussed along with the circuit structure. Analysis of the CM generated by each inverter topology will be compared. The next section will cover design of each individual inverter topology such as semiconductor device selection and inductor design. After the design of each topology the performance of each inverter will be estimated using a loss analysis of the designed components.

Experimental validation of the performance of each inverter will be carried out focusing on efficiency. Final assessment of each inverter topology will be carried out using a comparison of efficiency, cost and CM performance.

2 INVERTER TOPOLOGIES

By examining the different inverter configurations and each method operation it is possible to gain a basic understanding of their advantages and disadvantages. With the majority of inverter topology development being made to address the issues of CM noise and efficiency there have are many classes of inverter that have their own characteristics. For the voltage source inverter most of these inverters can be classified into the number of active switches required.

2.1 FOUR ACTIVE SWITCH INVERTERS

Topologies in the four active switch class include the full bridge inverter and the unipolar dual buck inverter.

2.1.1 Full Bridge Inverter

The basic topology for four switch VSI is the full bridge inverter as shown in Figure 2.1. The physical configuration of the full bridge VSI consists of two switch legs for a total of four semiconductor devices that have the ability to conduct current in the reverse direction either through the body diode in the MOSFET or the anti-parallel diode in the case of IGBTs. To generate a sinusoidal output the middle node of each switch leg is connected to an inductor for traditional modulation methods to filter out the switching ripple generated by the transistors.

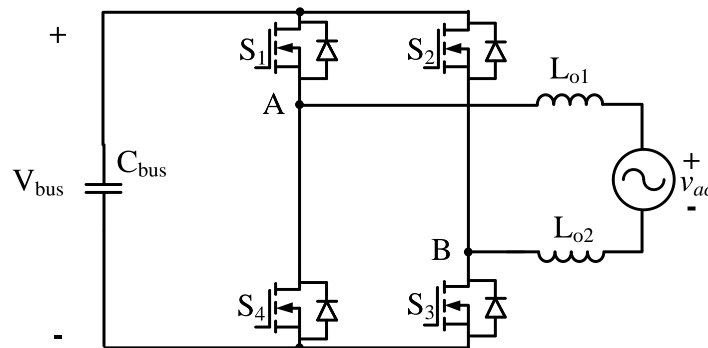


Figure 2.1: Full Bridge VSI

The greatest advantage of the full bridge VSI is the simplicity of the structure as well as the ability to run different modulation schemes in order to accommodate for different applications. There

are two main pulse width modulation (PWM) schemes to run the full bridge VSI, which include bipolar and unipolar. For the case of bipolar modulation there is only one implementation method.

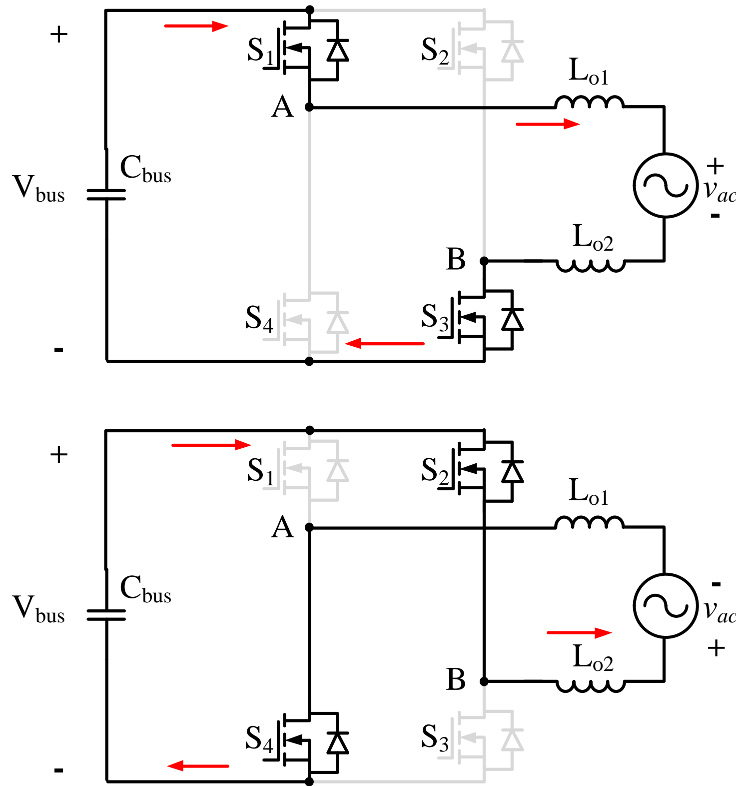


Figure 2.2: Bipolar Switching Modulation Scheme for Full Bridge VSI

In order to implement bipolar modulation as shown in Figure 2.2, the diagonal switches S_1 and S_3 are turned on at the same time allowing the current to flow to the output for positive line cycle. When S_1 and S_3 are turned off the complementary diagonal switches S_2 and S_4 are turned on allowing the current to maintain its direction through the output inductor. The transistor gating signals are generated with a sinusoidal voltage reference superimposed on a higher frequency triangular or sawtooth carrier. The resulting voltage across the middle switch leg nodes V_A and V_B has a bipolar variation that goes from the positive magnitude of the input V_{bus} to the negative magnitude of the input $–V_{bus}$. The signals to generate a sinusoidal output for bipolar modulation are shown in Figure 2.3.

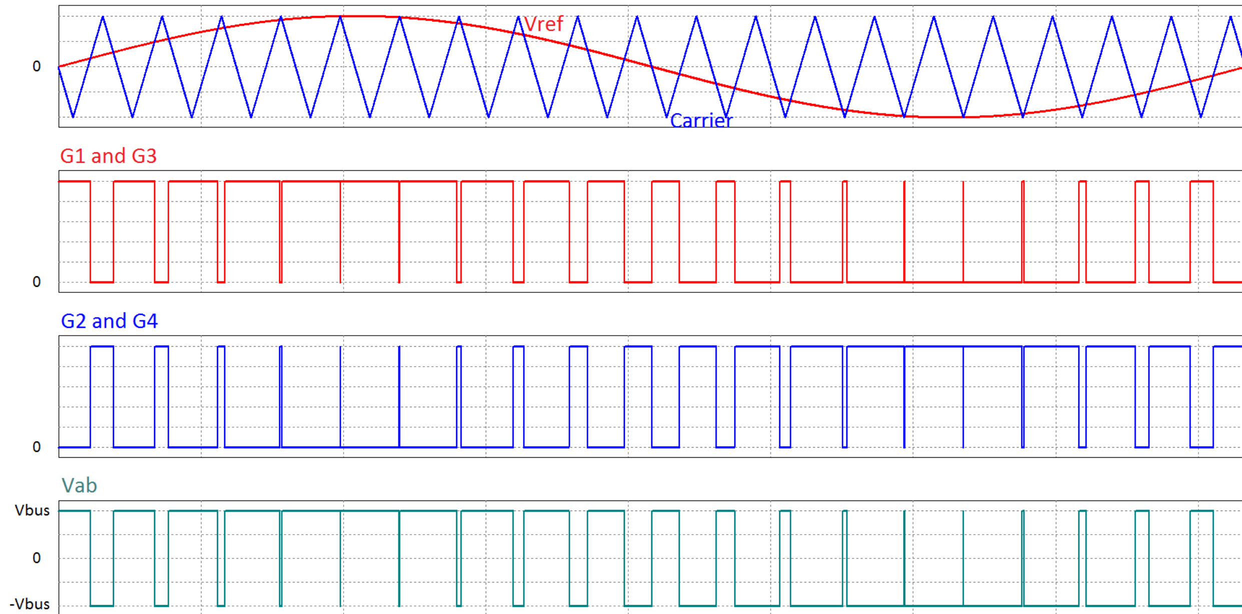


Figure 2.3: Modulation and Switch Node Output for Bipolar Modulation of Full Bridge VSI

The advantage to this method of modulation is that the middle switch leg voltages V_A and V_B are of a constant magnitude causing the CM voltage to be minimized as well as decreasing the leakage current going to earth ground. The biggest disadvantage of bipolar modulation is that the switching ripple in the output current is equivalent to the switching frequency with the key factor being that the voltage variation across the output filter is bipolar ($V_{bus} \rightarrow -V_{bus}$) this causes the core loss in the output inductor to increase as well as forcing the system to have a larger output filter to deal with the increased ripple. To get around the increased losses and output filter requirements unipolar modulation can be implemented.

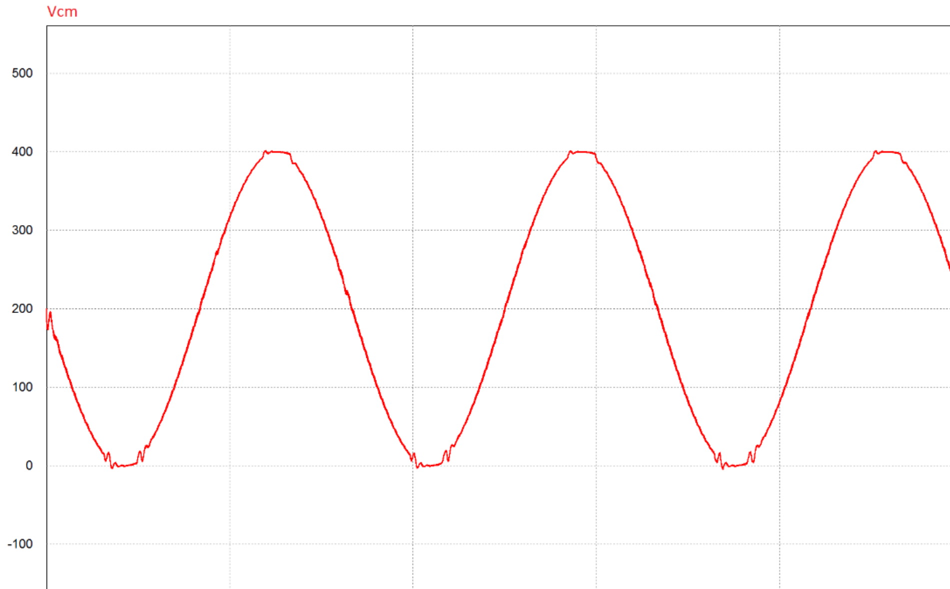


Figure 2.4: Common Mode Voltage of Full Bridge VSI with Bipolar Modulation

For an input voltage of 400 V, a switching frequency of 30 kHz and measuring the neutral point on the AC output to DC bus ground the CM voltage for bipolar modulation can be observed in Figure 2.4. The fundamental component of the CM voltage is low frequency with no high frequency components. The low frequency component of the CM voltage is not a major concern due to most of the stray capacitances being high impedance to low frequency signals due to their low capacitance value. Another advantage of the bipolar modulation for CM noise is that the dV/dt is gradual and not abrupt so the magnitude of the ground leakage currents should also be very small. Turn on and turn off of the diagonal switches have to be at the same moment otherwise the change in voltage at the switch nodes is uneven causing the generation of leakage current.

There are a number of different methods to achieve unipolar modulation the standard method of implementing unipolar modulation is to give each switch leg its own reference voltage which are phase shifted 180 degrees from each other. To implement dual reference unipolar modulation for the positive line cycle as shown in Figure 2.5, S_1 and S_3 are turned on at the same time, then S_3 is turned off and S_2 is turned on to allow the current to freewheel through S_1 and S_2. Next S_4 is turned on while S_2 remains turned on, then S_2 is turned off and S_3 is turned on to allow the current to freewheel through S_3 and S_4. The transistor gating signals are generated with two sinusoidal voltage references, phase shifted 180 degrees apart from each other, superimposed on a higher frequency triangular or sawtooth carrier. The resulting voltage across the middle switch leg nodes V_A and V_B has a unipolar variation that goes from the positive magnitude of the input V_{bus} to zero for the positive line cycle and from the negative

magnitude of the input $-V_{bus}$ to zero for the negative line cycle. The signals to generate a sinusoidal output for unipolar modulation are shown in Figure 2.6.

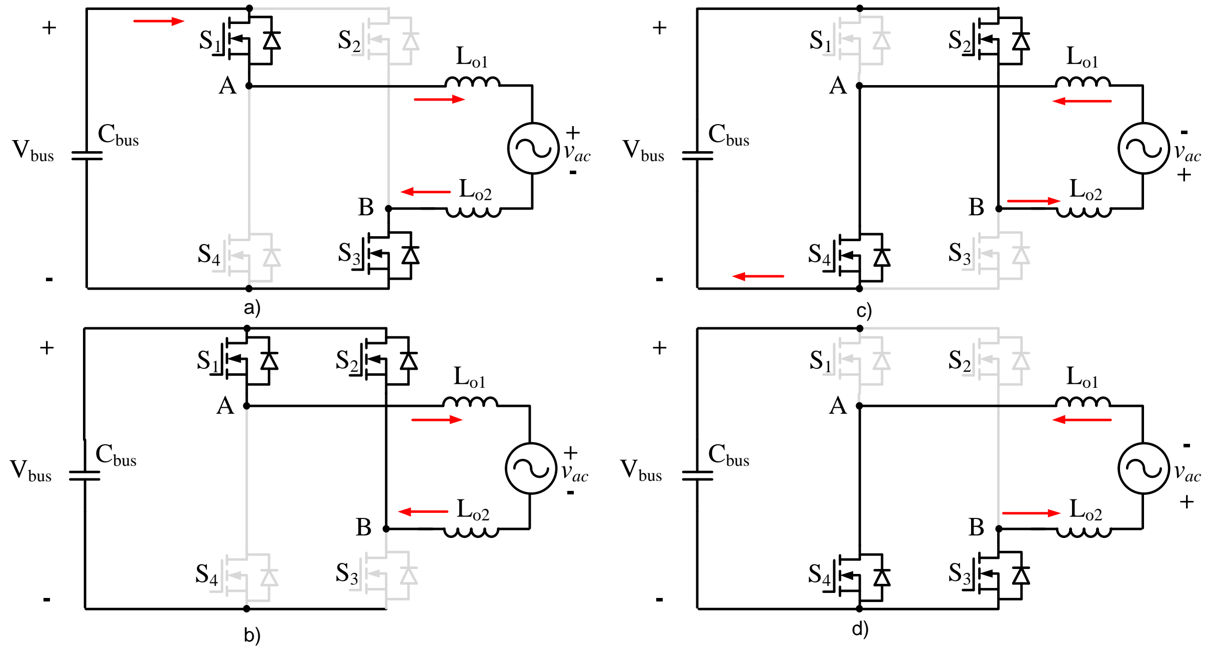


Figure 2.5: Unipolar Switching Modulation Scheme for Full Bridge VSI

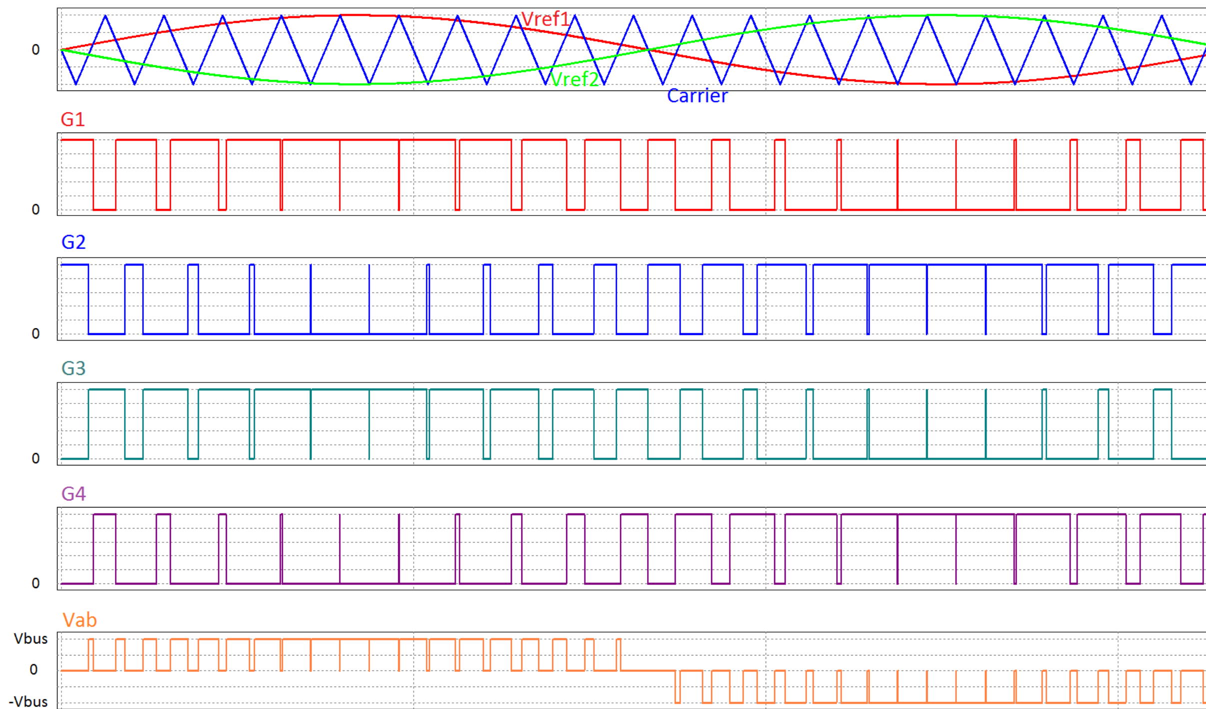


Figure 2.6: Modulation and Switch Node Output for Standard Unipolar Modulation of Full Bridge VSI

For unipolar modulation the switching ripple is equal to double the switching frequency, this causes the requirements for the output filter to be reduced compared to bipolar switching. Since the voltage across the output filter is only from V_{bus} to zero during positive line cycle and $-V_{bus}$ to zero during negative line cycle the voltage across the output inductor is reduced causing the core losses to also decrease. There is also a reduction in switching losses during the zero voltage regions of operation. The disadvantage of dual carrier unipolar switching is that the sum of the middle switch leg voltages V_A and V_B are not a constant magnitude causing the CM voltage and leakage currents to be very high.

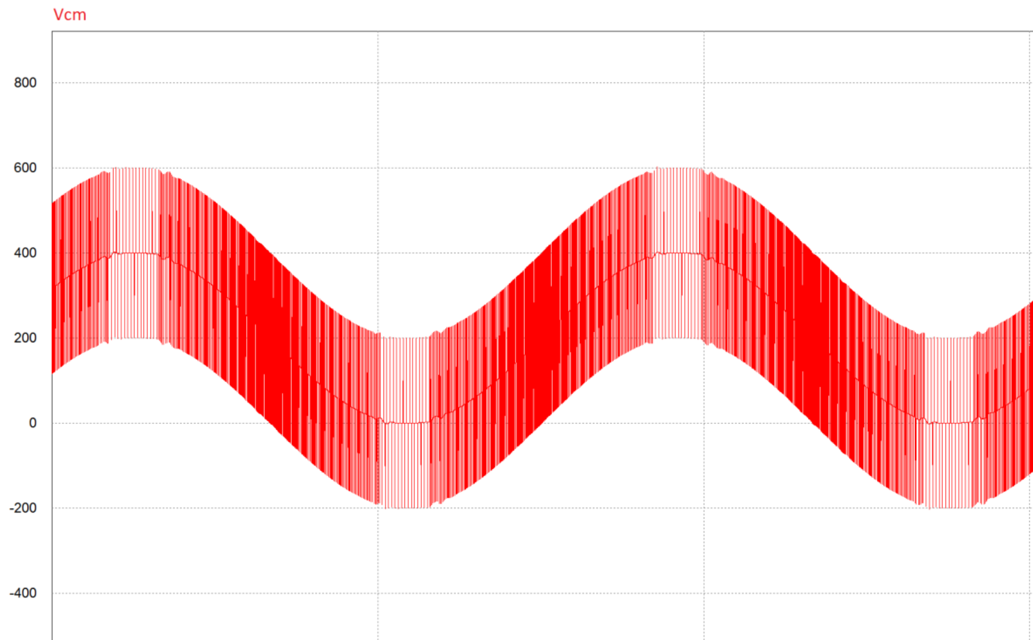


Figure 2.7: Common Mode Voltage of Full Bridge VSI with Standard Unipolar Modulation

With the same system specifications as the bipolar modulation case, the CM voltage for unipolar modulation can be observed in Figure 2.7. The fundamental component of the CM voltage consists of both low and high frequency components. The high frequency components are of major concern with the dV/dt magnitude also being very high. The CM noise for standard unipolar modulation is the highest for the full bridge topologies and for practical implementation addition design considerations need to be taken into account for the EMI and CM filters.

A variation of unipolar switching is to use a pair of switches running at high frequency and a pair of switches running at line frequency. There are multiple methods used to implement this configuration with the term being that this is asymmetrical unipolar modulation. For the most basic configuration both high frequency switches are on one switch leg and the low frequency switches are on the other

switch leg shown in Figure 2.8. This modulation method allows implementation with only one output filter inductor since there is only one high frequency switch node. The modulation scheme for this method for both positive and negative line cycle is shown in Figure 2.9.

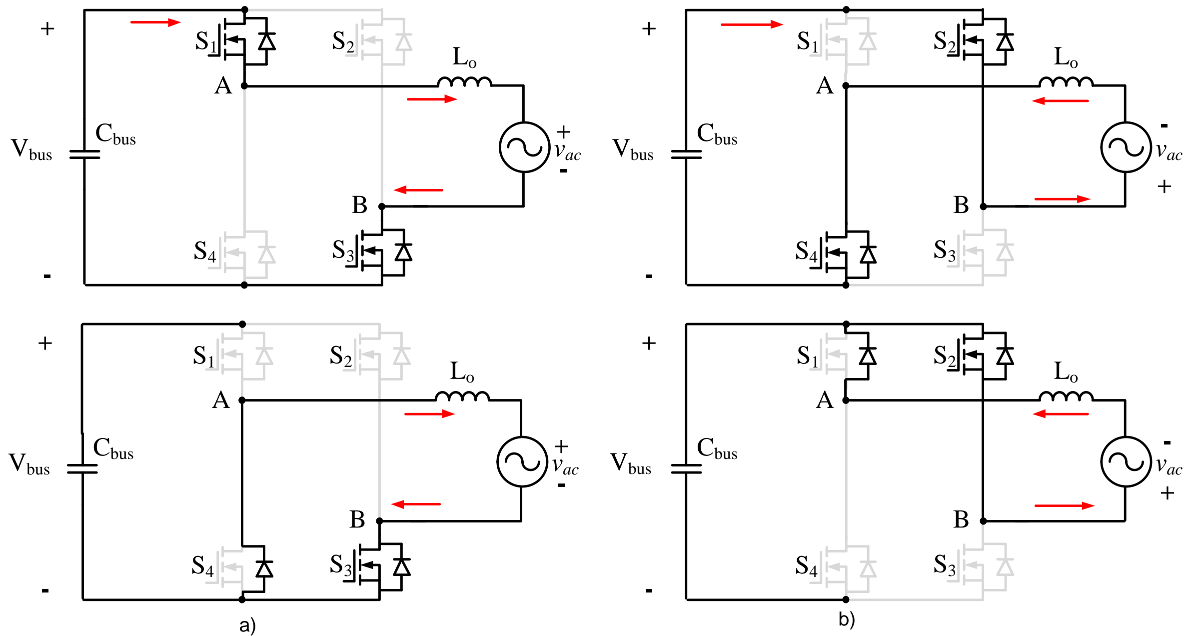


Figure 2.8: Asymmetrical Unipolar Modulation Scheme for Full Bridge VSI

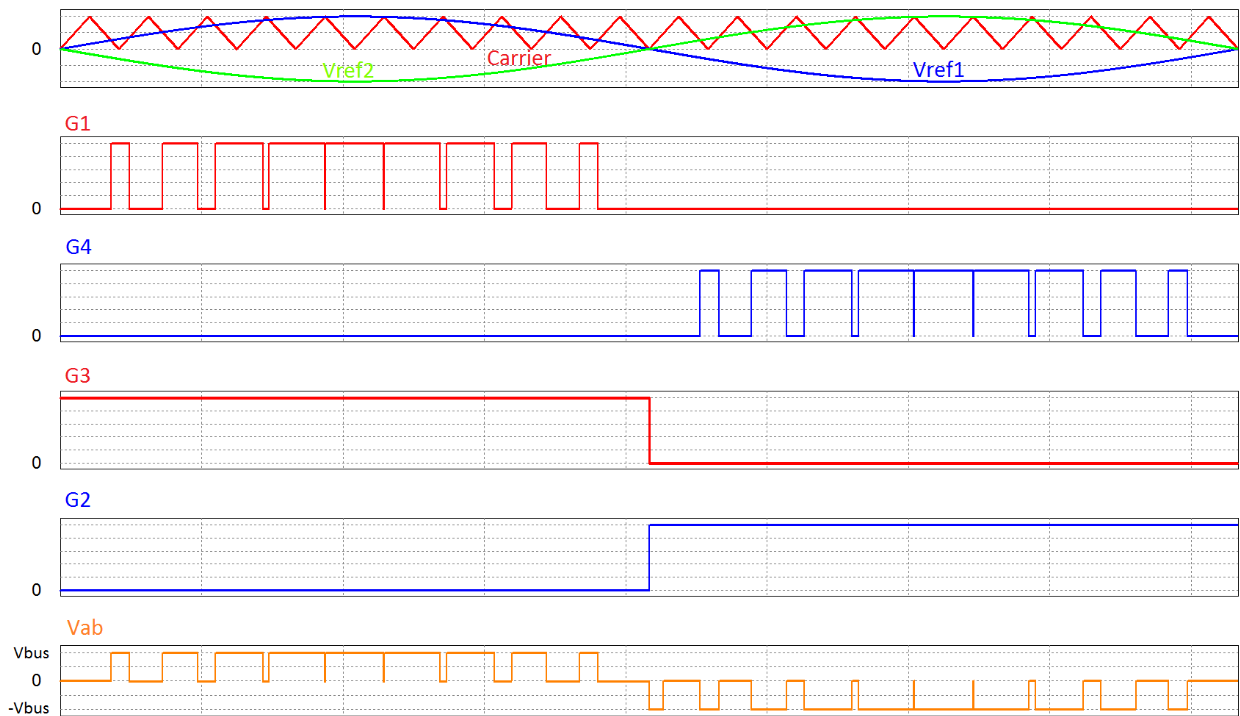


Figure 2.9: Modulation and Switch Node Output for Asymmetrical Unipolar Modulation of Full Bridge VSI

During the positive line cycle of operation S_1 operates at high frequency with S_3 turned on for the entire line cycle. When S_1 turns off the current freewheels through the body diode of S_4. For the negative line cycle S_4 operates at high frequency with S_2 turned on for the entire line cycle. When S_4 turns off the current freewheels through the body diode of S_1. Since the voltage across the output filter is the same as the conventional unipolar modulation, which is from V_{bus} to zero during positive line cycle and $-V_{bus}$ to zero during negative line cycle, the losses on the output filter are reduced. Since the high frequency switching is on one switching leg there only needs to be one output inductor simplifying the topology and reducing the cost of implementation. The CM noise is more manageable due to the inductor filtering out all the high frequency in the single output inductor with the fundamental frequency of the CM voltage being 60 Hz. A further variation to this modulation scheme for an all MOSFET configuration has the gating signal for the complementary high frequency switching being turned on during the freewheeling portion in order to reduce the conduction losses in the transistor by going through the lower resistance channel instead of the body diode. This method of gating is called synchronous rectification (SR) and is commonly used for lower voltage high power step down converters to minimize the high conduction losses due to the high output current. The gating signals for asymmetrical unipolar modulation using SR are shown in Figure 2.11.

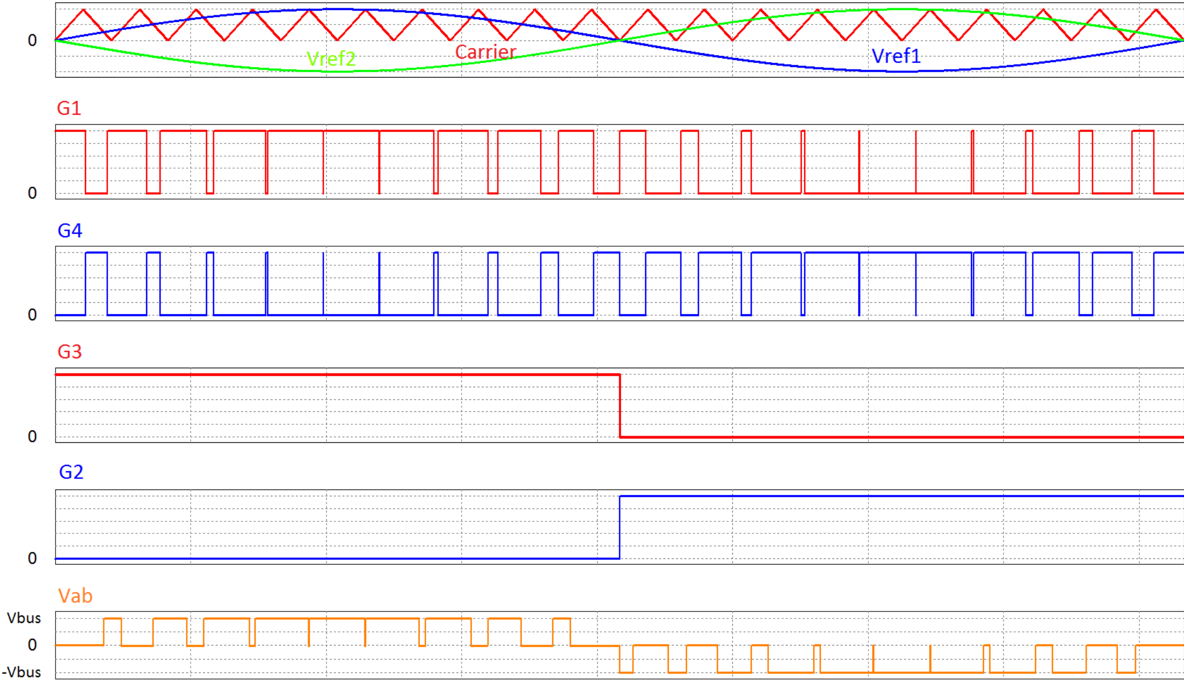


Figure 2.10: Modulation and Switch Node Output for Asymmetrical Unipolar Modulation of Full Bridge VSI using SR

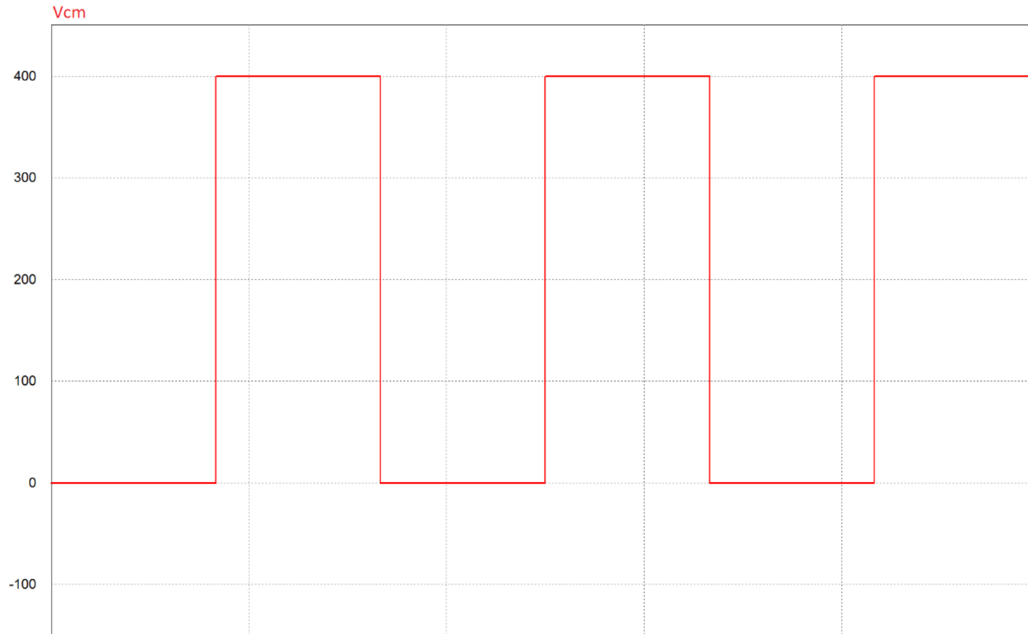


Figure 2.11: Common Mode Voltage of Full Bridge VSI with Asymmetrical Unipolar Modulation

Simulating the asymmetrical unipolar modulation method the CM voltage can be observed in Figure 2.11. The fundamental component of the CM voltage is consists only of low frequency components. The low frequency components are not a concern, with the impedance of the stray capacitance being very high for low frequency signals. The biggest concern is the sharp dV/dt transitions when the output polarity changes this could cause the magnitude of the low frequency leakage currents to be very high. The CM noise for asymmetrical unipolar modulation is the second lowest for the full bridge topologies with only bipolar modulation having better CM performance. The CM performance when running SR is the exact same as when not running SR.

The last possible configuration for unipolar modulation is to have the switches for each switch leg operate with one high frequency switch and one low frequency switch on the same switch leg. Since there are high frequency switches on both switch legs this modulation scheme requires output inductors for each switch leg. In Figure 2.12 the modulation scheme for the hybrid gating PWM scheme is shown for the positive and negative line cycles. During the positive line cycle S_1 switches at high frequency and S_3 remains on for the entire line cycle. When S_1 turns off the current freewheels through the body diode of S_4. During the negative line cycle S_2 switches at high frequency and S_4 remains on for the entire line cycle. When S_2 turns off the current freewheels through the body diode of S_3. Like other unipolar modulation schemes the losses on the output filter are reduced. The CM noise is similar to the dual

reference unipolar PWM, in order to minimize the CM voltage there has to be inductors on each output line.

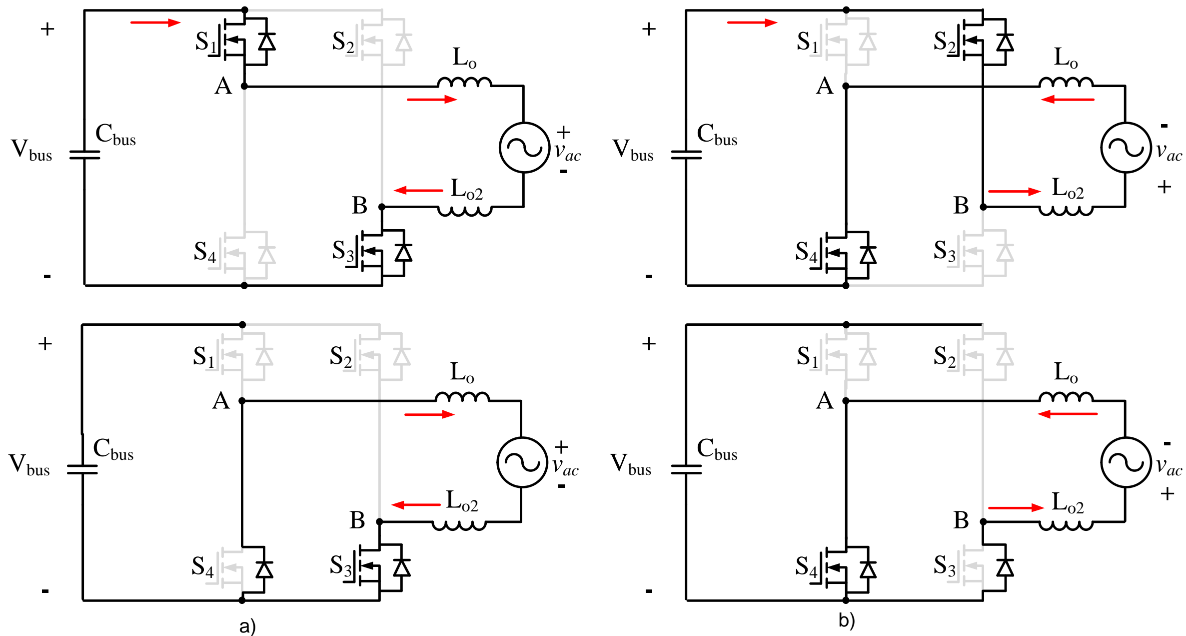


Figure 2.12: Hybrid Unipolar Modulation Scheme for Full Bridge VSI

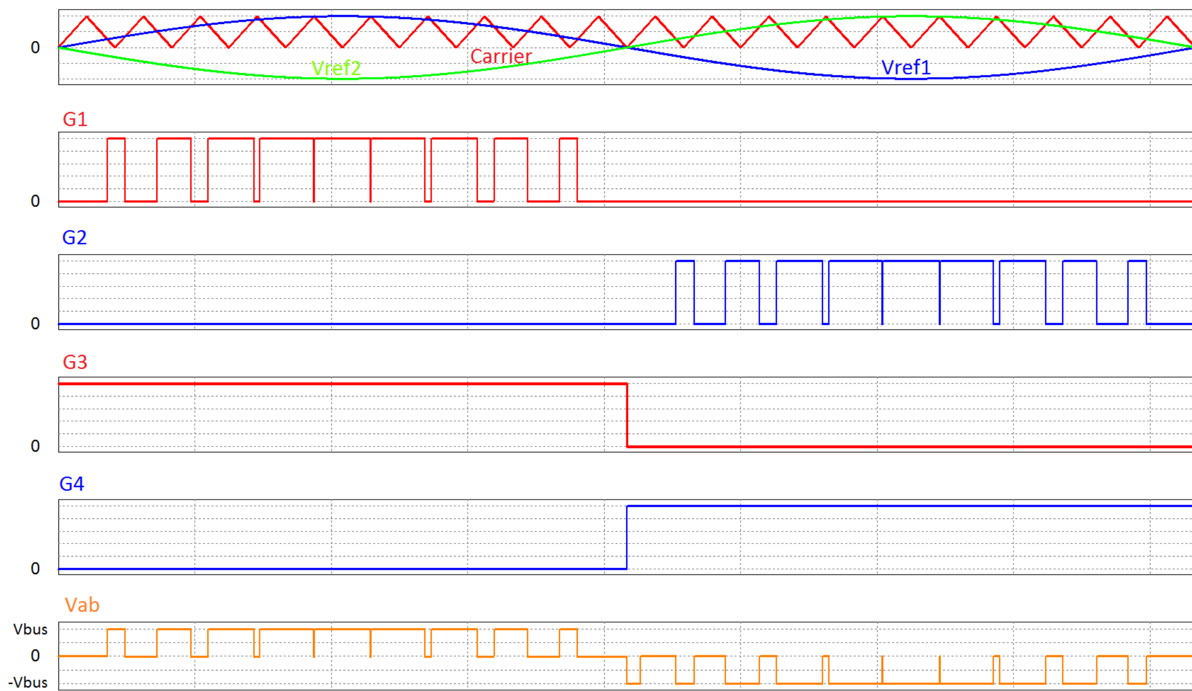


Figure 2.13: Modulation and Switch Node Output for Hybrid Unipolar Modulation of Full Bridge VSI

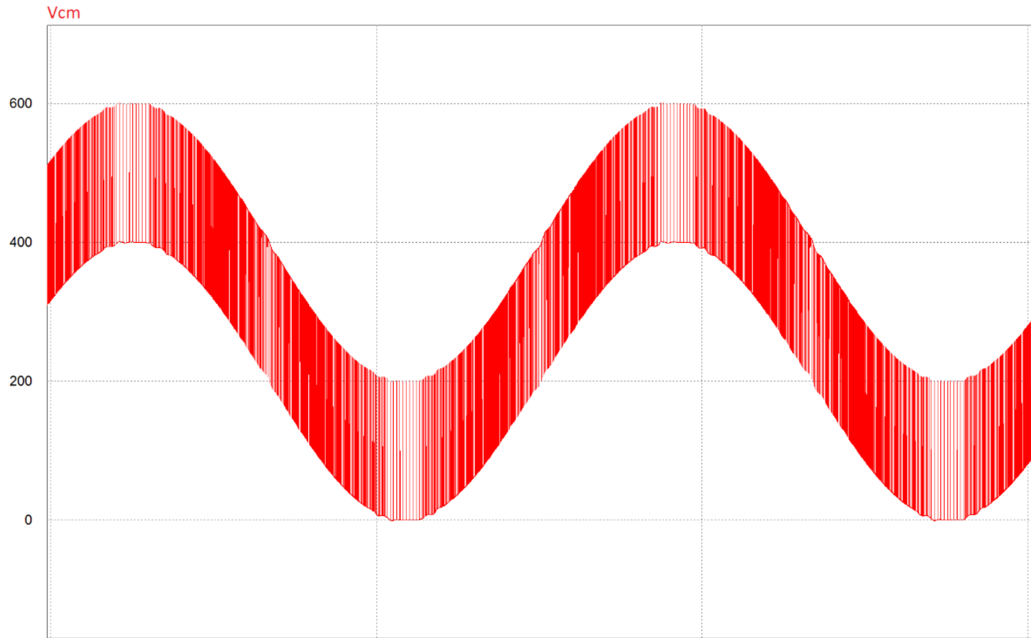


Figure 2.14: Common Mode Voltage of Full Bridge VSI with Hybrid Unipolar Modulation

The simulation of the CM voltage for hybrid unipolar modulation can be observed in Figure 2.14. The fundamental component of the CM voltage consists of both low and high frequency components. The magnitude of the high frequency CM noise is not as large as the standard unipolar modulation, however there is still substantial high frequency CM noise. The magnitude of the CM noise is less than the standard unipolar due to the reduced dV/dt. This method is the second worst CM performance of the full bridge VSI inverters with additional design needed to minimize the EMI and CM noise.

2.1.2 Unipolar Dual Buck Inverter

Another four active switch inverter topology is the asymmetrical unipolar dual-buck. The basic circuit configuration is that of two buck chopper converters that operate individually for half of the line cycle [20]. In order to run asymmetrical unipolar there are a pair of low frequency switches that connects the neutral point of the AC line to the negative point of the DC bus, which also helps reduce the CM noise. There are two possible configurations for this topology, negative rail in Figure 2.15a, and positive rail in Figure 2.15b. Their operation and performance are almost identical to each other.

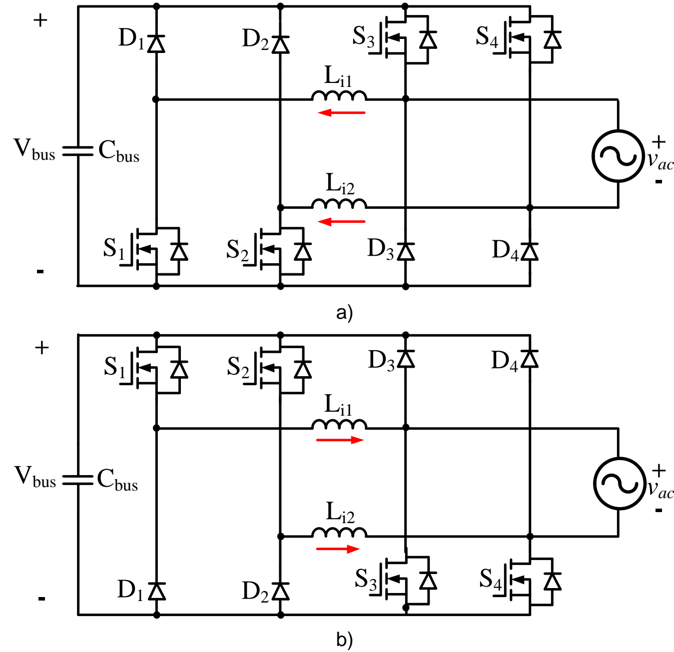


Figure 2.15: Unipolar Dual Buck Inverter with Negative Rail (a) and Positive Rail (b)

The advantage of the dual buck topology is that it can utilize MOSFETs for the high frequency switches without any reliability issues. If low reverse recovery diodes are used in the chopper diodes D_1 and D_2 there is potential to achieve very high efficiency. Another advantage is that each buck chopper only operates during one line cycle and not both the thermal distribution from power dissipation is improved over inverters that have continuous power dissipation. Since the operation for this inverter is unipolar there is low core loss on the inductor. Operation for the negative rail dual buck inverter (Figure 2.15a) is shown in Figure 2.16.

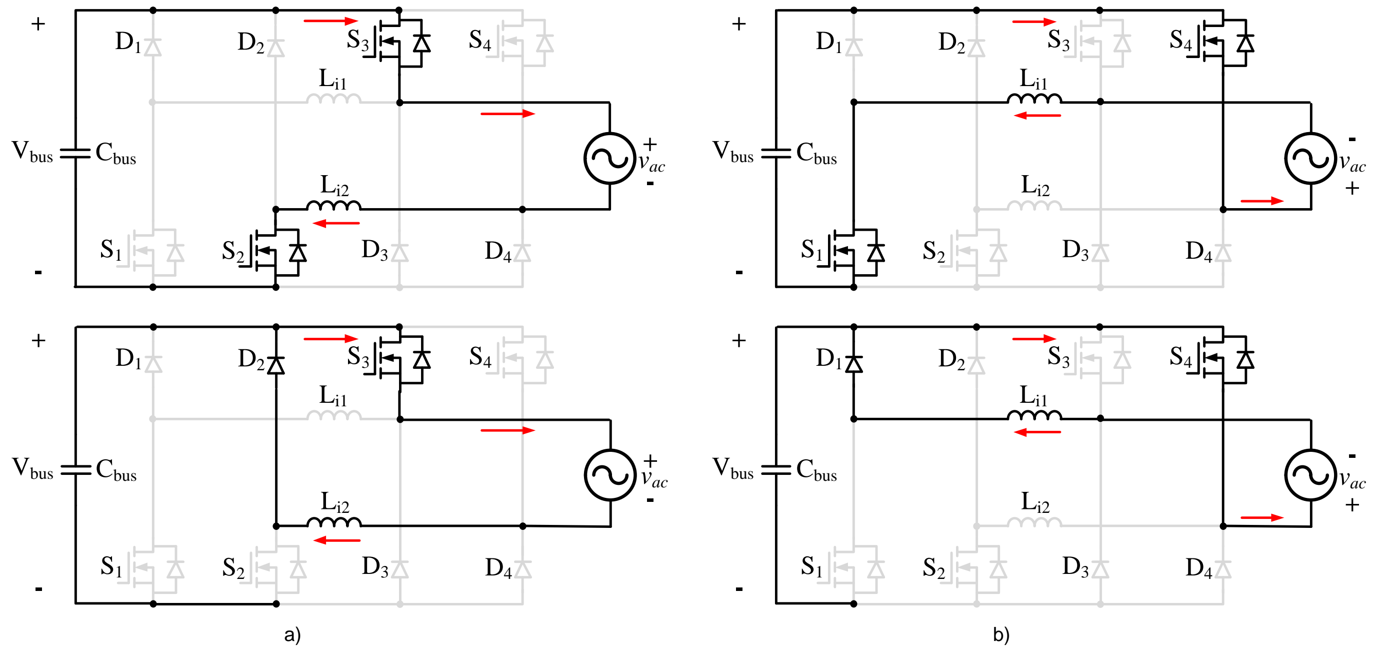


Figure 2.16: Modulation Scheme for Negative Rail Unipolar Dual Buck Inverter

For the positive line cycle S_2 operates at high frequency while S_3 remains on the entire time. After S_2 turns off the current freewheels through the diode D_2 and S_3. During the negative line cycle S_1 operates at high frequency while S_4 remains on for the entire cycle. After S_1 turns off the current freewheels through the diode D_1 and S_4. The diodes D_3 and D_4 serve no purpose in the operation of the circuit and are used mainly to clamp the high-side low frequency switches to the DC bus.

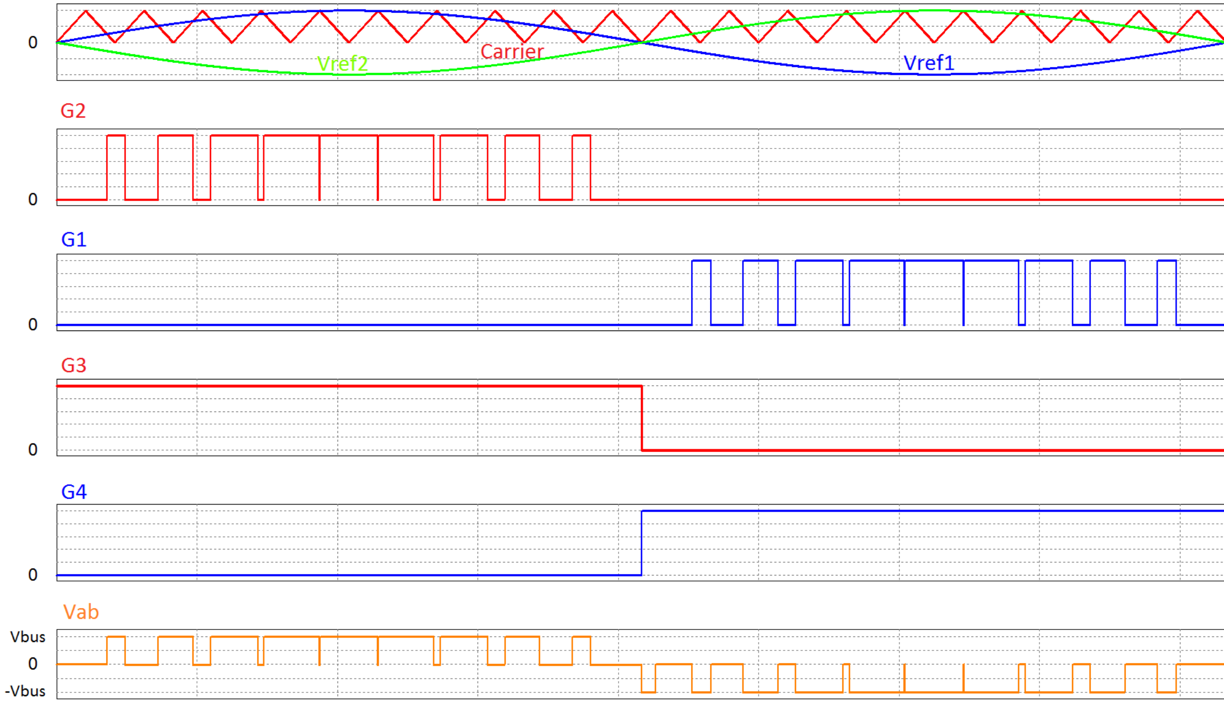


Figure 2.17: Modulation and Switch Node Output for Unipolar Dual Buck Inverter

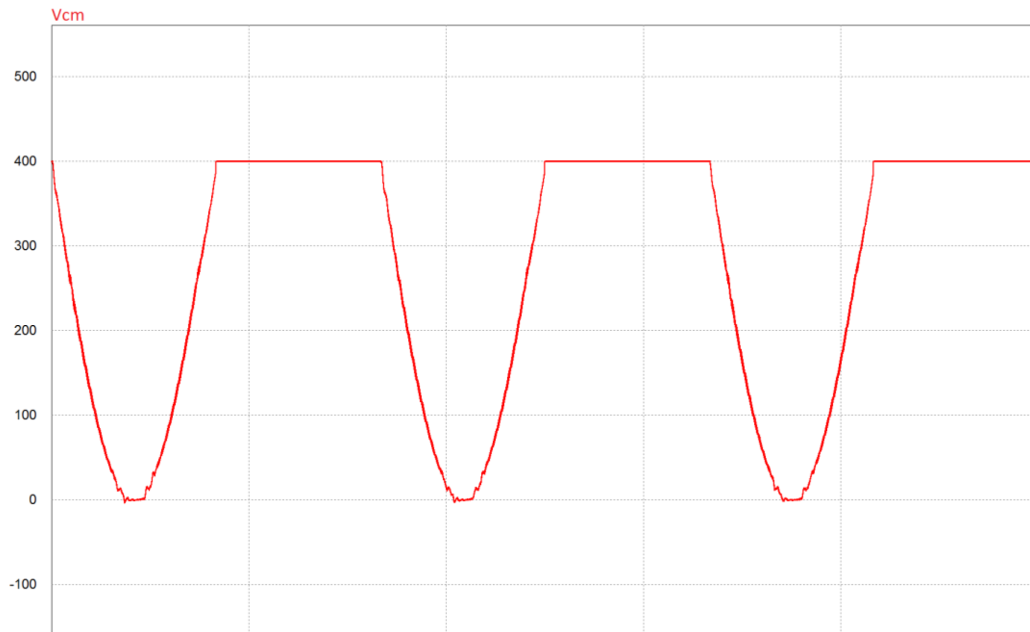


Figure 2.18: Common Mode Voltage of Unipolar Dual Buck Inverter

The unipolar dual buck inverter CM voltage is shown in Figure 2.18. The CM voltage fundamental component consists of only a low frequency component. The dV/dt of the voltage

transition is also gradual so the magnitude of the leakage currents should be minimal. The CM performance of the unipolar dual buck is only surpassed by bipolar modulation of the full bridge VSI.

The biggest disadvantage of the unipolar dual buck inverter is that two separate magnetics are required for operation increasing the system costs. Since each inductor is used only during one line cycle this decreases the magnetic utilization. Another disadvantage of the unipolar dual buck inverter is the possibility of short circuit illustrated in Figure 2.19.

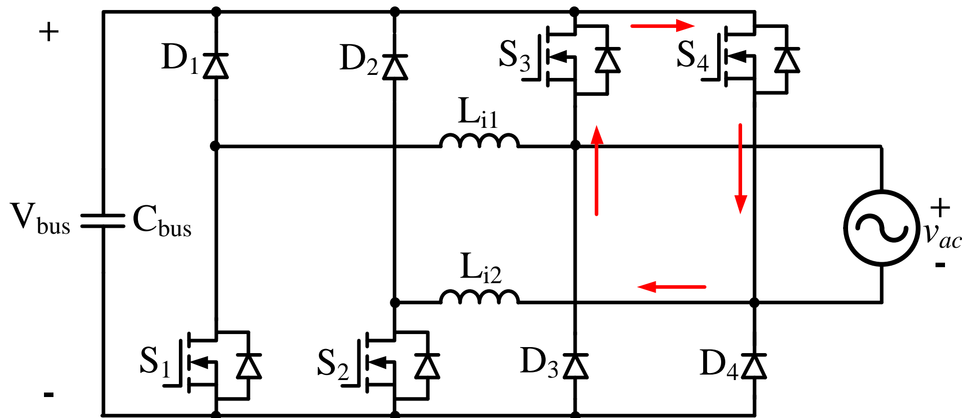


Figure 2.19: Short Circuit Path of Unipolar Dual Buck Inverter

To prevent the short circuit condition there are a number of different methods that can be employed. Thyristors could replace the MOSFETs used for the low frequency switches and since they are unidirectional devices the current cannot reverse conduct preventing the short circuit, however since thyristors have a fixed voltage drop this would increase the conduction loss of the system. Another method to prevent the short circuit is to place a high voltage diode in series with the low frequency switches making them unidirectional devices, this increases the conduction loss of the system. To get around trying to use unidirectional devices for the low frequency switches, an additional inductor could be placed between the switch and the AC line. This prevents the current from instantly building up and causing a short circuit, the disadvantage to this approach is that some energy is stored in the inductor which increases the leakage currents and CM noise. Adding two 200 micro-Henry (uH) short circuit prevention inductors to the CM noise simulation shown in Figure 2.20, highlights the increased leakage current of adding the additional inductors.

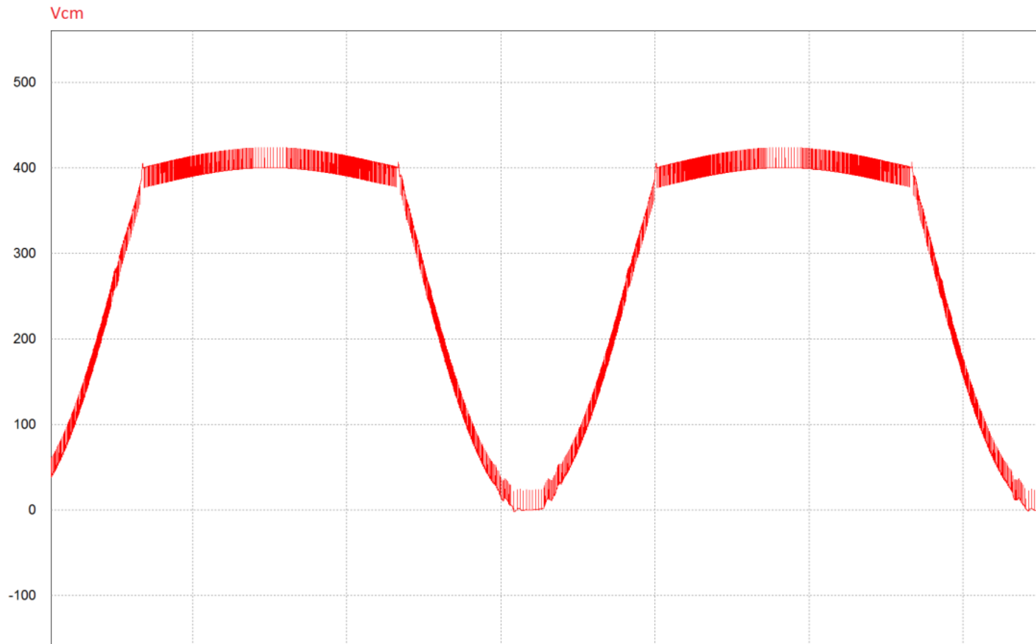


Figure 2.20: Common Mode Voltage of Unipolar Dual Buck Inverter with Short Circuit Prevention Inductors

2.2 Five Active Switch Inverters

After the four switch VSI the next inverter topology configuration class consists of five active switches. Five active switch inverters consist of the single buck inverter and the H5 from the German company SMA.

2.2.1 Single Buck Inverter

The basic configuration for the five switch inverter is a buck converter running at high frequency followed by a low frequency full bridge unfolder. In order to generate the sinusoidal output the high frequency switch receives a rectified sinusoidal reference and the low frequency switches operate at the line frequency to unfold the waveform from a rectified sinusoid to a full sinusoidal waveform. The topology, shown in Figure 2.21 is referred to as the single buck inverter.

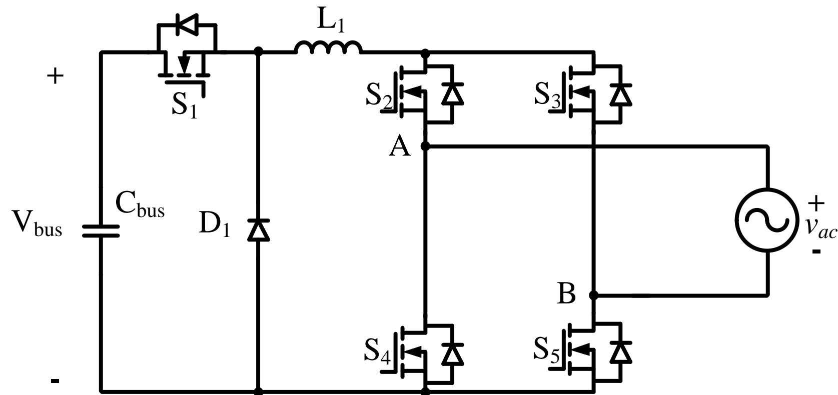


Figure 2.21: Single Buck Inverter

The single buck inverter's biggest advantage is similar to the unipolar dual buck inverter in that it can reliably utilize MOSFETs for the high frequency switch. Another advantage of the circuit is that only one magnetic is needed for operation increasing the magnetic utilization and decreasing the system cost. If MOSFETs are used for the full bridge unfolder the additional conduction loss from having an additional switch in the conduction path can be mitigated. The modulation operation of the converter is unipolar decreasing inductor losses and since the AC neutral point is always connected to negative point of the DC bus the CM noise is also reduced compared to standard unipolar modulation. The operation of the single buck inverter is shown in Figure 2.22.

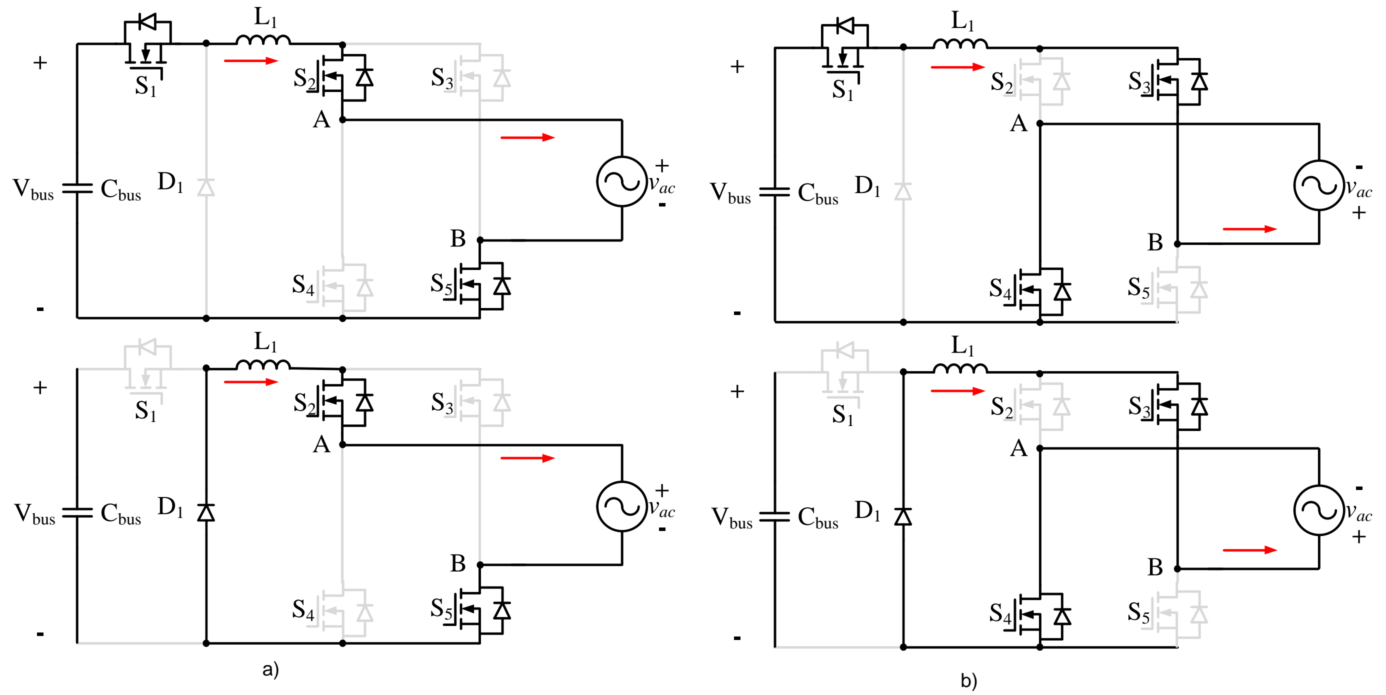


Figure 2.22: Modulation Scheme for Single Buck Inverter

At both the positive and negative line cycle S_1 operates at high frequency due to fact that the reference is a rectified sinusoid. During the positive line cycle after S_1 turns off the current freewheels through the diode D_1, S_2 and S_5. For the negative line cycle after S_1 turns off the current freewheels through D_1, S_3 and S_4.

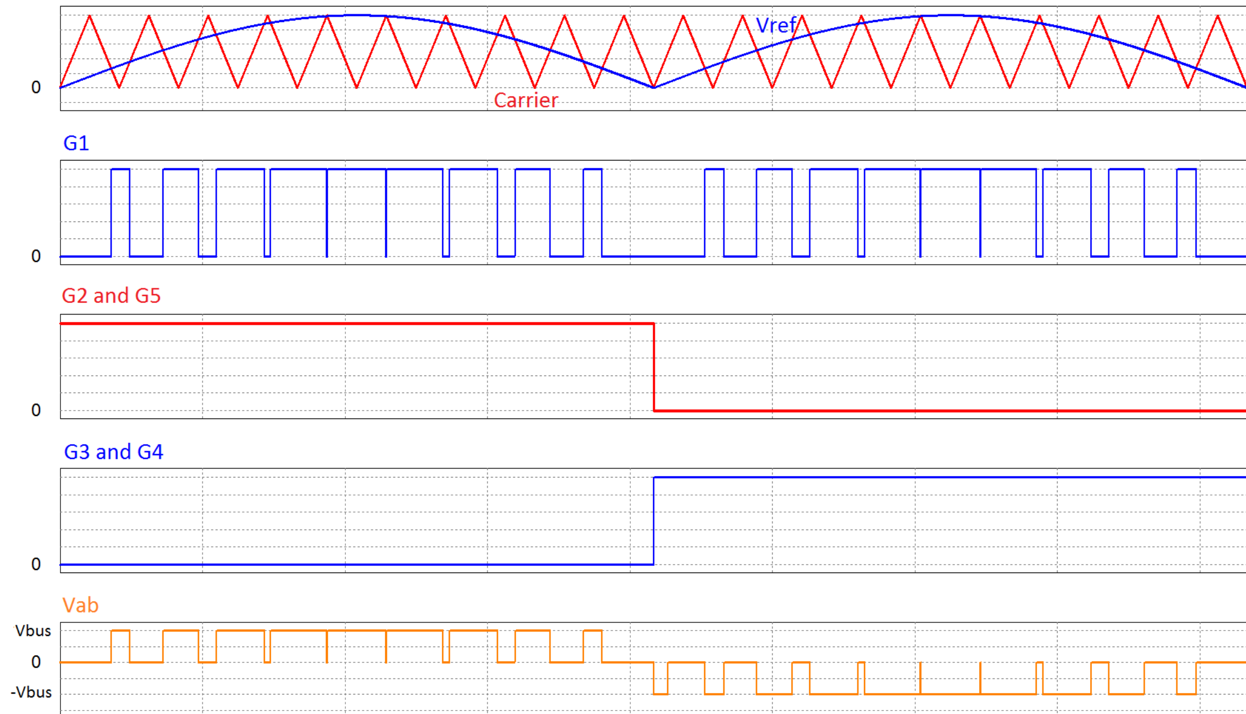


Figure 2.23: Modulation and Switch Node Output for Single Buck Inverter

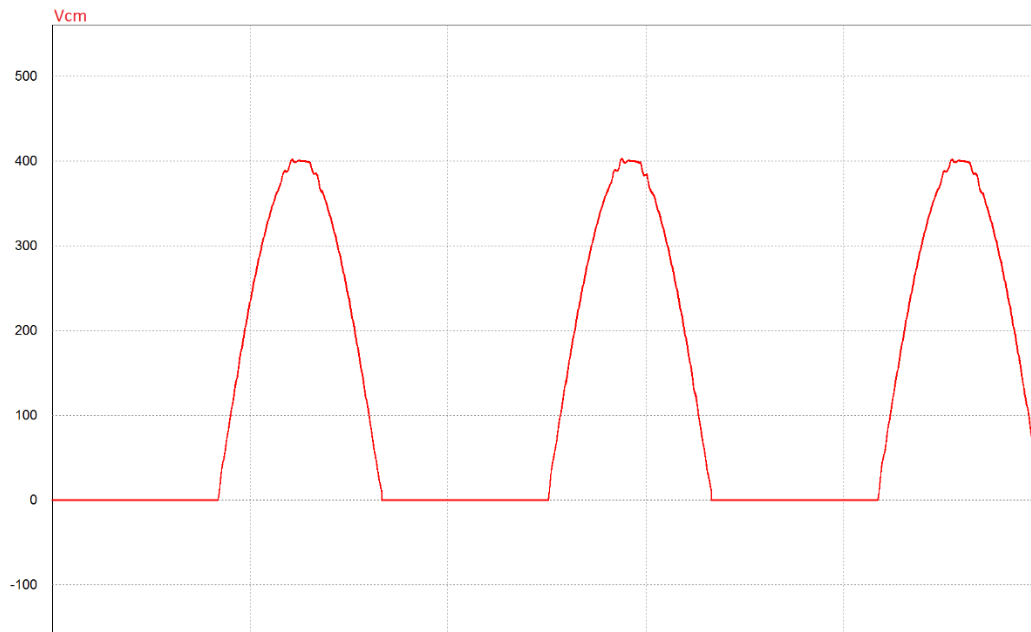


Figure 2.24: Common Mode Voltage of Single Buck Inverter

Simulation of the CM voltage for the single buck inverter is shown in Figure 2.24. The CM voltage fundamental component consists of only low. The dV/dt of the voltage transition is also gradual

so the magnitude of the leakage currents should be minimal. The CM performance of the single buck inverter is the same as the unipolar dual buck inverter.

The single buck inverter suffers from the same short circuit disadvantage that the unipolar dual buck suffers from. Using unidirectional devices for the low frequency switches is not as feasible for this topology due to the fact that there would be the maximum current going through two forward voltage drops. The only reasonable approach to eliminating the short circuit problem is to have inductors on the middle node of the unfolder full bridge to the AC line this comes with the issue of increased CM noise and losses in the inductors.

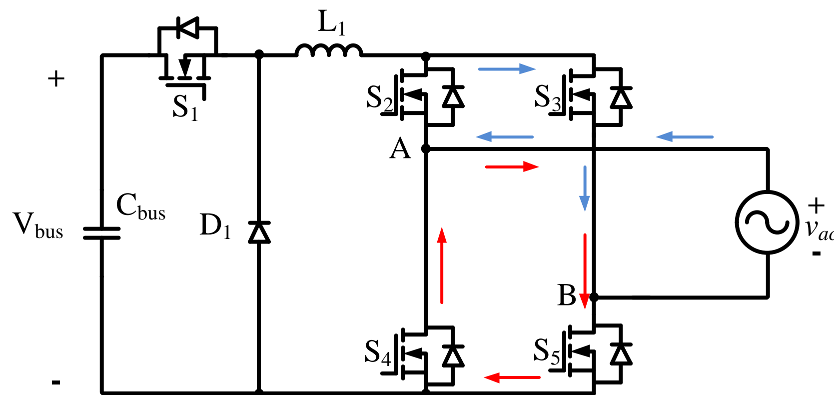


Figure 2.25: Short Circuit Path of Single Buck Inverter

2.2.2 H5 Inverter

A variation of the single buck inverter topology removes the freewheeling diode and places the output inductor on both AC lines. The gating modulation of this inverter topology is modified to reduce the CM noise. The high side switch continues to operate with a rectified sinusoidal reference, the bottom switches operate at high frequency during each half grid cycle and the top switches operate at line frequency. The inverter shown in Figure 2.26 is referred to as the H5 inverter.

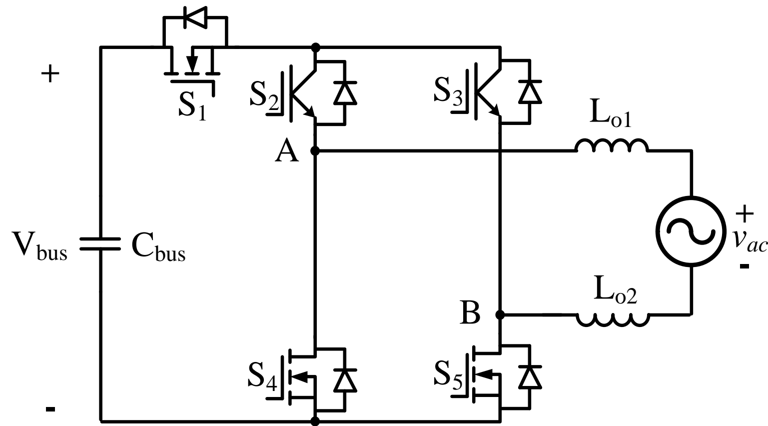


Figure 2.26: H5 Inverter

The main purpose of the H5 inverter design is the reduction of CM noise. This is achieved by having the middle node of the bridge switch legs equal to half the bus voltage during the freewheeling and switching periods. MOSFETs can be used without issue for S_1, S_4, and S_5 if the diodes parallel with S_2 and S_3 have low reverse recovery. Since the output waveform is unipolar there is reduced losses on the output filter. Having the output inductors on each AC line eliminates the risk of short circuit that was present on the single buck inverter. The modulation scheme for the H5 inverter is illustrated in Figure 2.27.

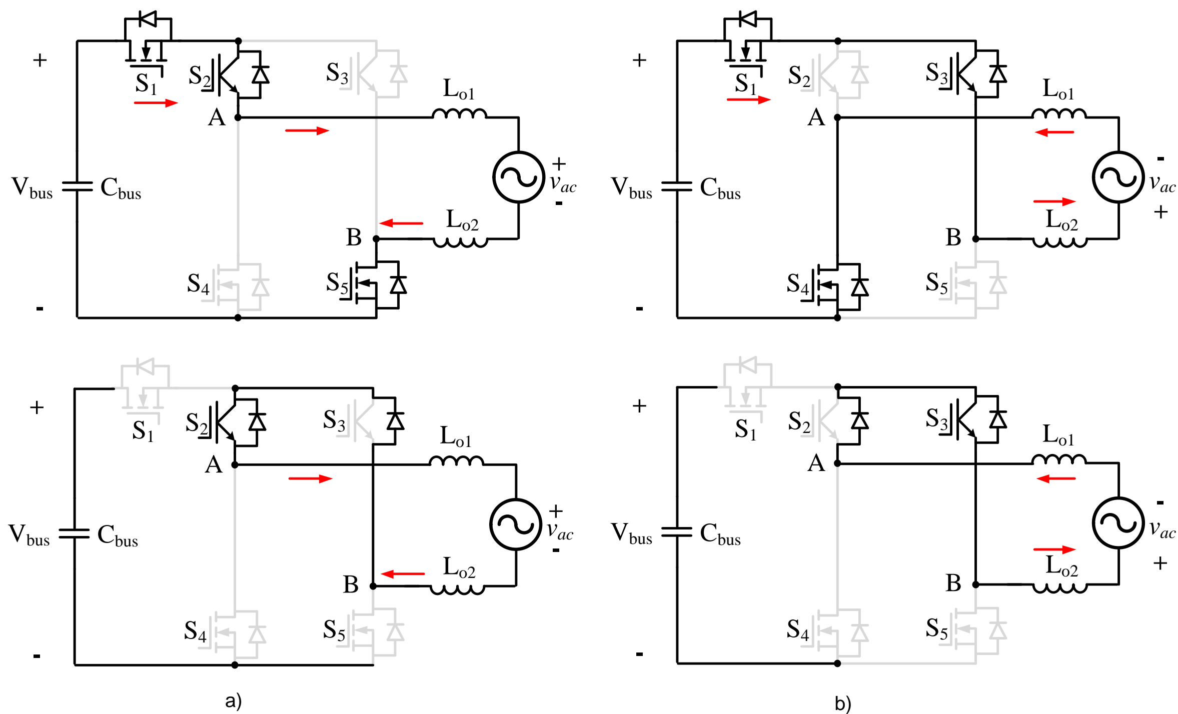


Figure 2.27: Modulation Scheme for H5 Inverter

When the inverter is operating in the positive line cycle switches S_1 and S_5 operate at high frequency, while S_2 is on during the entire line cycle. After S_1 and S_5 turn off the current freewheels through the parallel diode of S_3 and through S_2. During the negative line cycle switches S_1 and S_4 operate at high frequency, while S_3 is on during the entire line cycle. After S_1 and S_4 turn off the current freewheels through the parallel diode of S_2 and through S_3.

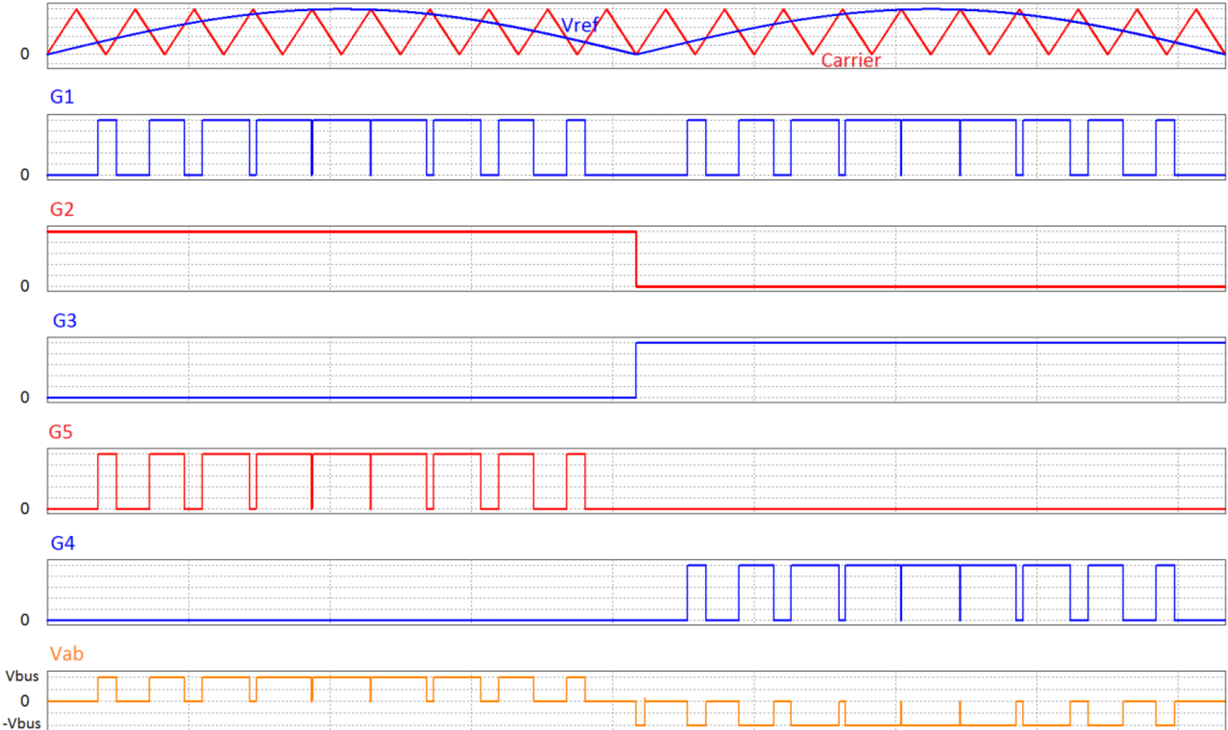


Figure 2.28: Modulation and Switch Node Output for H5 Inverter

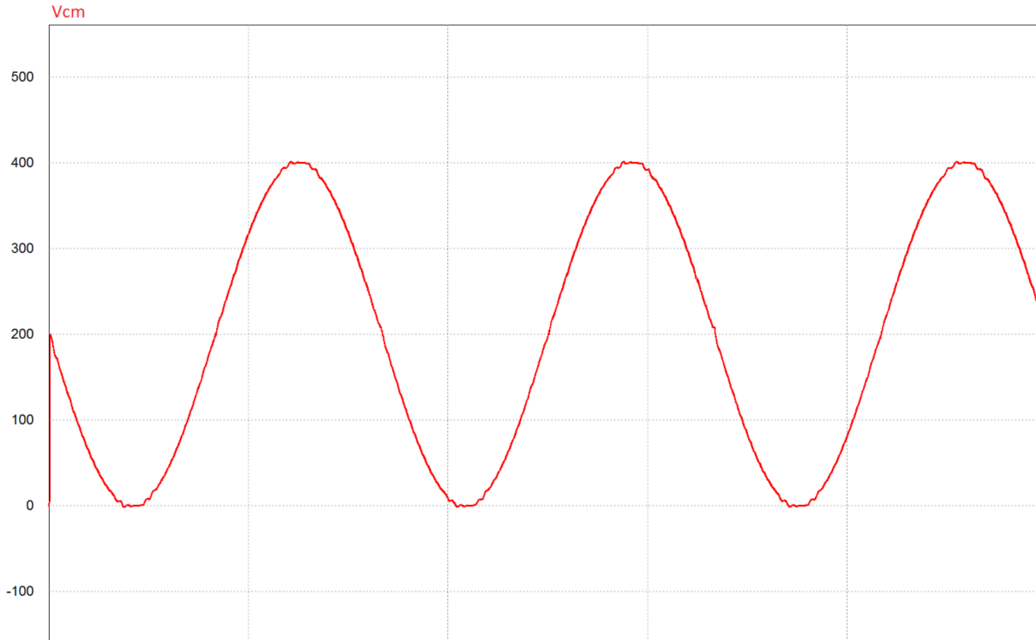


Figure 2.29: Common Mode Voltage of H5 Inverter

Figure 2.29 shows the simulated CM voltage of the H5 inverter. The fundamental component of the CM voltage is low frequency with no high frequency components. The low frequency component of the CM voltage is not a major concern due to most of the stray capacitances being high impedance to low frequency signal due to their low capacitance value. Another advantage of the H5 topology for the CM noise performance is that the dV/dt is gradual and not abrupt so the magnitude of the ground leakage currents should also be very small. The CM noise performance of the H5 inverter is similar to that of the bipolar modulation full bridge VSI.

For the H5 to work reliably and achieve the low CM noise the high frequency switches have to be synchronized very precisely to maintain a constant voltage across the middle switch nodes. The inverter physical parameters need to be as symmetrical as possible to ensure the parasitic capacitances are similar. The biggest disadvantage is that in order to use MOSFETs for the high frequency switches, IGBTs have to be used for the low frequency switches so that a low reverse recovery parallel diode can be used during the freewheeling portion of operation. This means that when the high frequency switches are on there is a fixed voltage drop in the conduction path and during the freewheeling period there are two forward voltage drops in the freewheeling path. The H5 topology has been patented by SMA [25].

2.3 SIX ACTIVE SWITCH INVERTERS

The next class of inverters consists of six switch inverter topologies that can decouple the inverter bridge from the grid during the freewheeling states to minimize CM noise. Topologies that use this method include the HERIC and SHREC inverters.

2.3.1 HERIC Inverter

A basic configuration for the six switch inverter topology consists of a full bridge VSI and two freewheeling commutation legs consisting of a MOSFET and diode in series with the orientation of the series diode opposite that of the body diode as shown in Figure 2.30. This inverter topology is referred to as the highly efficient and reliable inverter concept (HERIC).

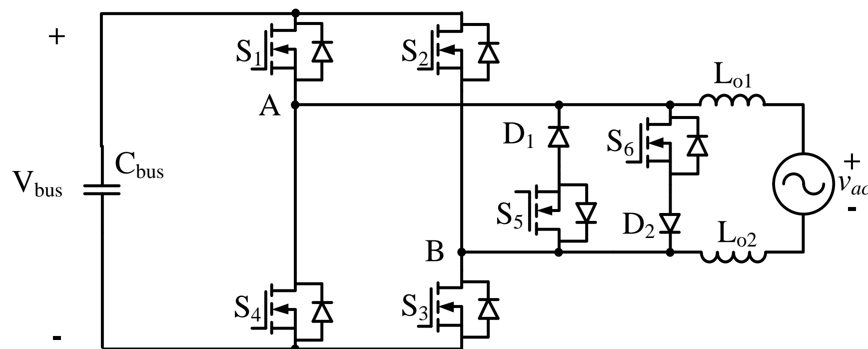


Figure 2.30: HERIC Inverter

The operation of the HERIC inverter is so that the middle switch nodes for each switch leg of the full bridge are equal to half of the bush voltage during the freewheeling and switching periods. Since the sum of the middle leg nodes are equal to the bus voltage during the switching periods keeping the voltage at those nodes constant and reducing the ground leakage current. Not only can the HERIC achieve low common mode noise but it can also use MOSFETs for all the active switches. This means that there is low conduction loss for the semiconductor devices. During the freewheeling operation the only conduction losses are the series diode voltage drop and the low frequency switch [26]. The losses on the output inductor is also minimized since the voltage across the middle switch nodes are unipolar. The operation of the HERIC inverter is shown in Figure 2.31.

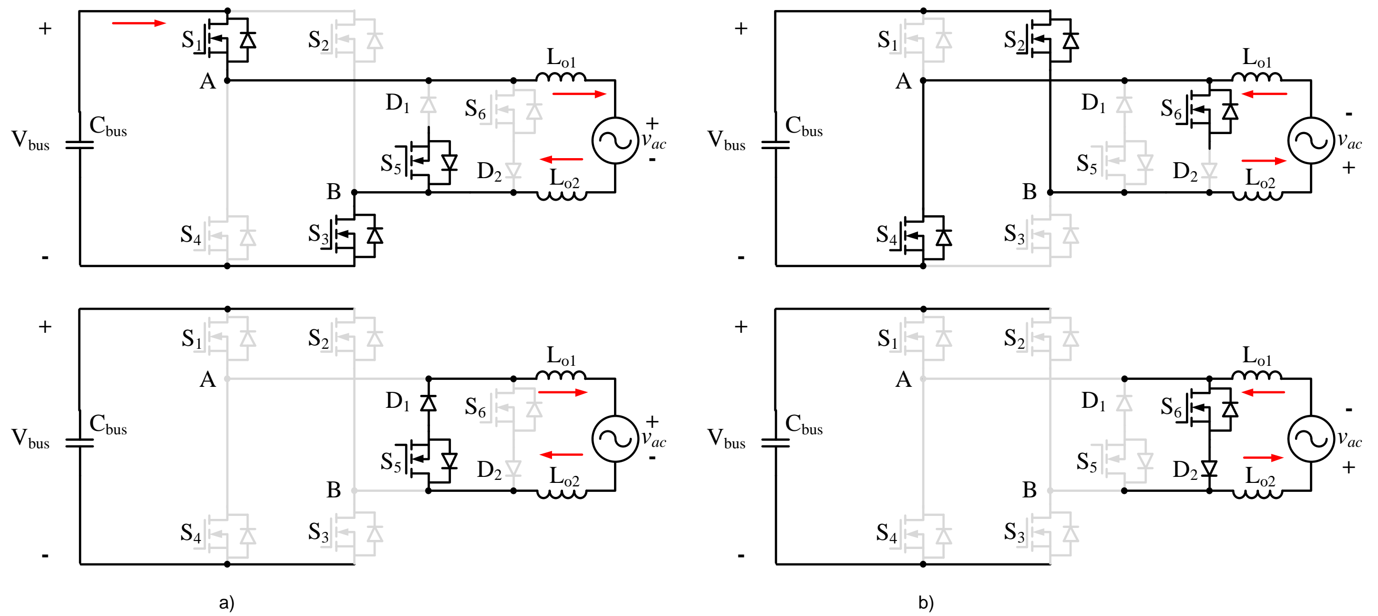


Figure 2.31: Modulation Scheme for HERIC Inverter

When the inverter is operating in the positive line cycle switches S_1 and S_3 operate at high frequency, while S_5 is on during the entire line cycle. The series diode D_1 prevents current from going through S_5 during the active switching period of the positive line cycle. After S_1 and S_3 turn off the current freewheels through the series diode D_1 and through S_5. During the negative line cycle switches S_2 and S_4 operate at high frequency, while S_6 is on during the entire line cycle. The series diode D_2 prevents current from going through S_6 during the active switching period of the negative line cycle. After S_2 and S_4 turn off the current freewheels through the series diode D_2 and through S_6.

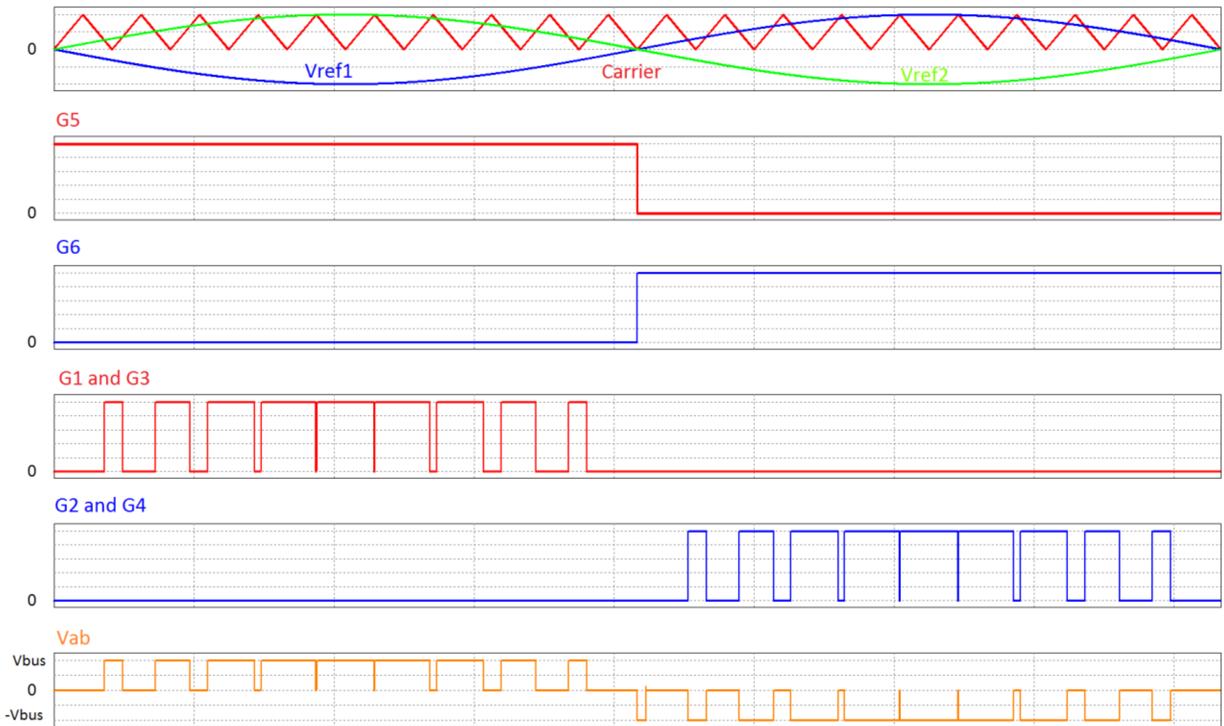


Figure 2.32: Modulation and Switch Node Output for HERIC Inverter

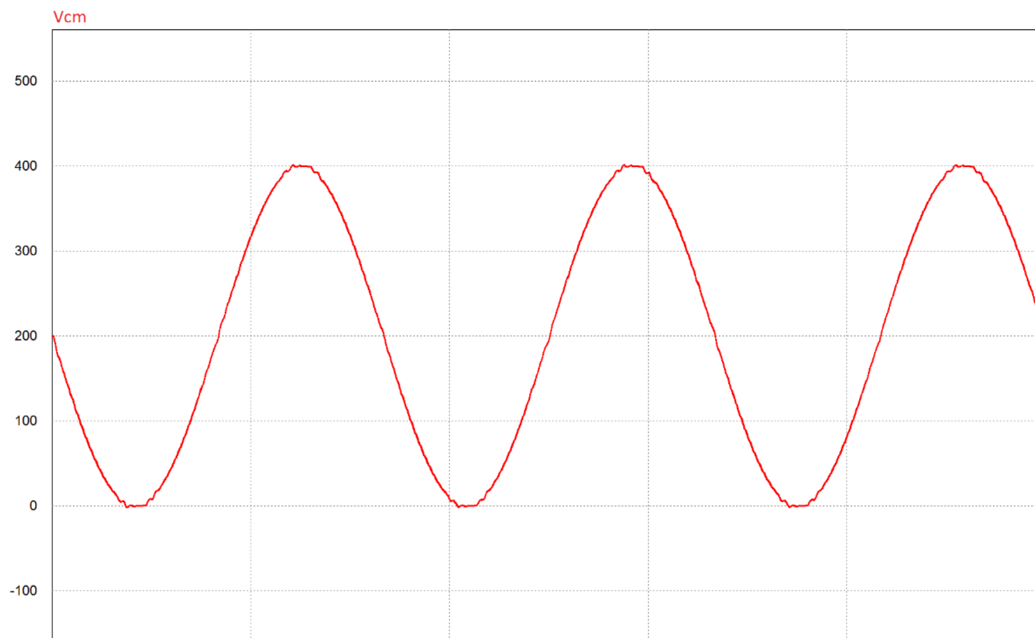


Figure 2.33: Common Mode Voltage of HERIC Inverter

CM voltage of the HERIC inverter can be observed in Figure 2.33. The fundamental component of the CM voltage is low frequency with no high frequency components. The magnitude of the ground leakage currents should also be very small due to the same dV/dt transitions. The CM noise

performance of the HERIC inverter is similar to that of the bipolar modulation full bridge VSI and H5 inverter.

For the HERIC to operate with low common mode noise there has to be symmetrical design in the circuit layout, output inductors and the semiconductor devices have to have similar parameters. Another issue with the operation of the HERIC is in order to drive the freewheeling separation switches there has to be additional gate driving circuitry required to drive them. The increased number of active switches makes implementation of this topology more costly. The HERIC inverter is patented by SUNWAYS [27].

2.3.2 SHREC Inverter

Another six switch topology that utilizes the same idea as the HERIC structure to achieve low CM voltage using grid decoupling switches is a hybrid of the dual buck inverter with the HERIC. The configuration consists of two buck legs for each line cycle for the active switching period and during the freewheeling period the buck legs are disconnected from the grid and the current flows through the switch and series diode branch. This inverter topology is called the super high reliability and efficiency converter (SHREC) illustrated in Figure 2.34 [28].

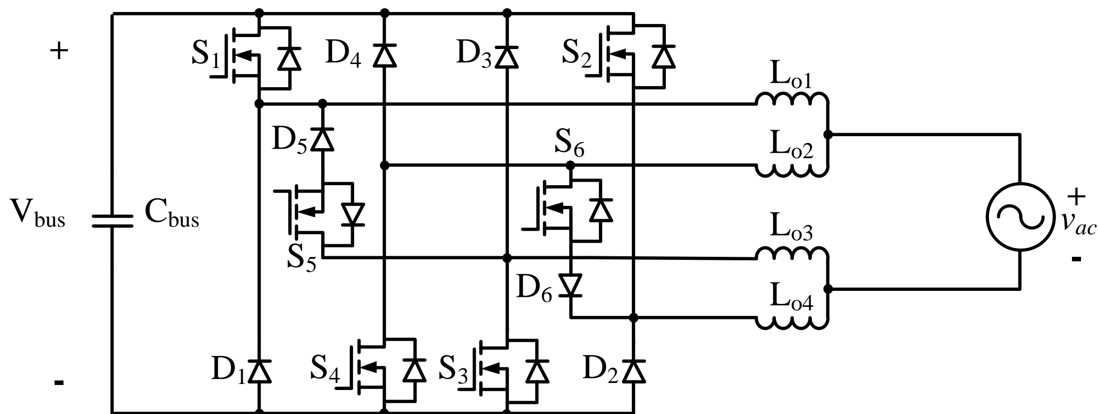


Figure 2.34: SHREC Inverter

The purpose of the SHREC inverter is to enhance the reliability of the HERIC inverter while maintaining the same efficiency and CM noise performance. The biggest advantage of the SHREC inverter is that there are no active switches connected in series eliminating the need for dead-time and the prevention of reverse current flow by using diodes. The inverter structure does not suffer from reverse recovery issues that most inverters have to accommodate for so the use of MOSFETs can be used to decrease the conduction losses during the active switching periods. The CM noise follows the

same principle as the HERIC in that the sum of the middle leg nodes are equal to the bus voltage during the switching periods keeping the voltage at those nodes constant and reducing the ground leakage current. Diodes D_1, D_2, D_3, and D_4 do not conduct and current and are used to clamp the switches to the DC bus allowing the use of low current conventional diodes. The voltage across the inductor is unipolar decreasing the losses in the output filter. With half of the converter operating during one line cycle the thermal distribution will also improve the efficiency for prolonged operation. To reduce the number of magnetics the inductors on the same line cycle for each buck leg can be coupled to one magnetic. Operation of the SHREC inverter is illustrated in Figure 2.35.

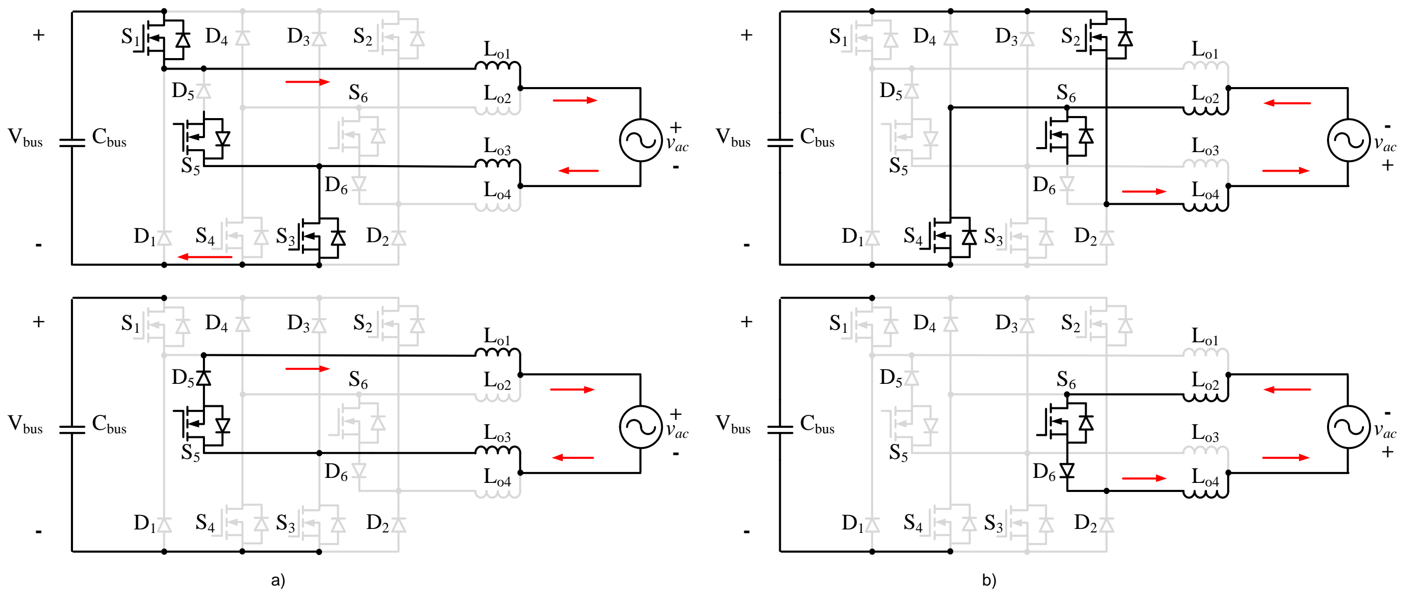


Figure 2.35: Modulation Scheme for SHREC Inverter

Operating in the positive line cycle the inverter switches S_1 and S_3 operate at high frequency, while S_5 is on during the entire line cycle. The series diode D_5 prevents current from going through S_5 during the active switching period of the positive line cycle. After S_1 and S_3 turn off the current freewheels through the series diode D_5 and through S_5. During the negative line cycle switches S_2 and S_4 operate at high frequency, while S_6 is on during the entire line cycle. The series diode D_6 prevents current from going through S_6 during the active switching period of the negative line cycle. After S_2 and S_4 turn off the current freewheels through the series diode D_6 and through S_6.

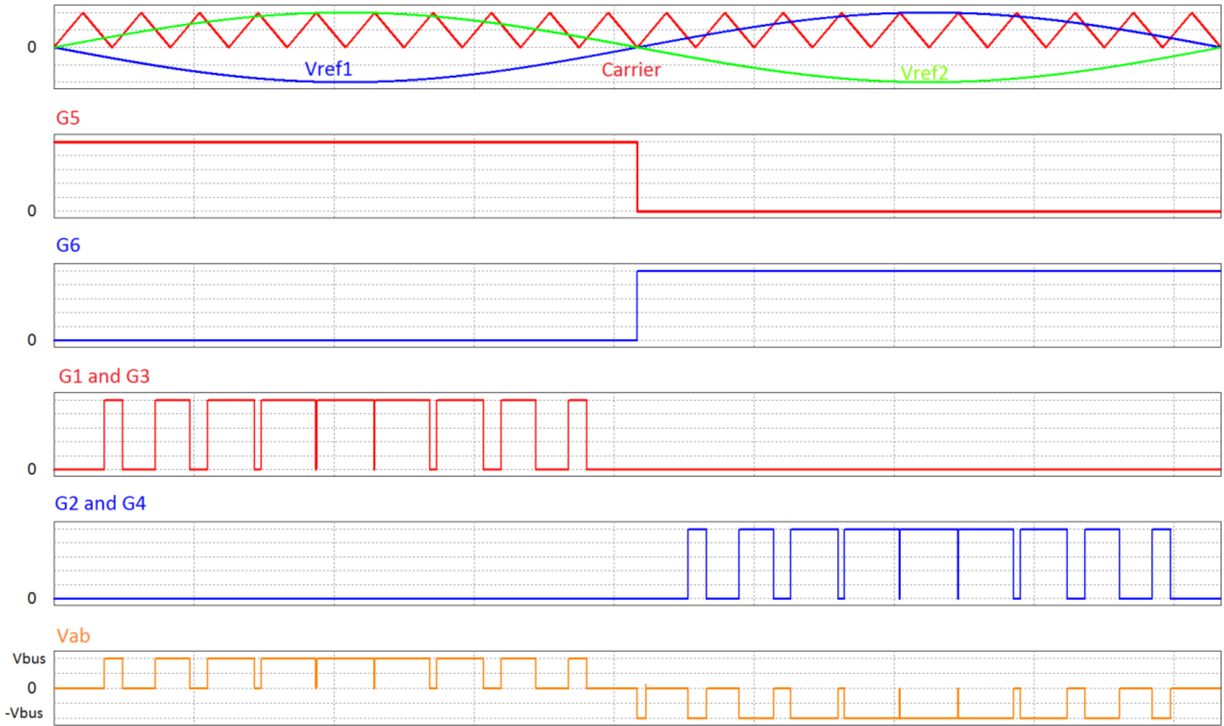


Figure 2.36: Modulation and Switch Node Output for SHREC Inverter

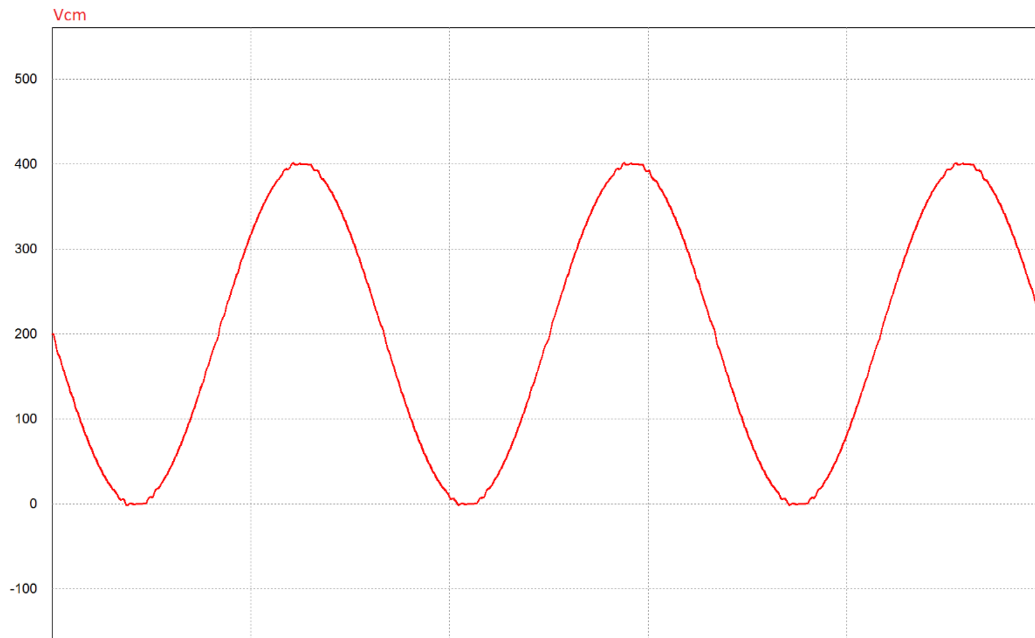


Figure 2.37: Common Mode Voltage of SHREC Inverter

The CM voltage of the SHREC inverter can be observed in Figure 2.37. The fundamental component of the CM voltage is low frequency with no high frequency components. The magnitude of the ground leakage currents should also be very small due for the same reason in the HERIC, H5 and

bipolar full bridge VSI. The CM noise performance of the SHREC inverter is similar to that of the bipolar modulation full bridge VSI, HERIC and H5 inverter.

The biggest disadvantage to this inverter is the large amount of components. There are six active switches, two freewheeling diodes, four clamping diodes and two coupled inductors. Coupling the output inductors only reduces the total number of inductors from four to two. Since there are two high side buck switches and two floating middle switches there has to a more complex auxiliary gating network to activate those switches since none of switches can have their gates charged using a bootstrap circuit.

3 INVERTER COMPONENT CHARACTERISTICS

For this section the design and selection of specific components in a single phase microinverter system will be covered. The criteria for the selection of the passive components such as the DC link capacitance, output filter inductor and output filter capacitor are examined. An overview of semiconductor devices and their operational behavior are discussed.

The specifications for a typical microinverter application do not vary over a wide range and for a typical PV installation are:

Parameter	Value
DC Link Voltage	370 – 400 V DC
Output Voltage	220 – 240 V_{rms} AC
Output Frequency	60 Hz
Output Power	170 – 300 W
Nominal Output Current	0.78 – 1.25 A_{rms} AC

Table 3.1: Microinverter System Specifications

From Figure 3.1 the major passive components in an inverter that is part of a multi-stage microinverter system consists of the DC link capacitor (C_{bus}), output inductor (L_i) and output capacitor (C_o). The DC link capacitor provides the energy to the inverter, while the output filter elements are used to attenuate the switching noise and create the sinusoidal output waveform.

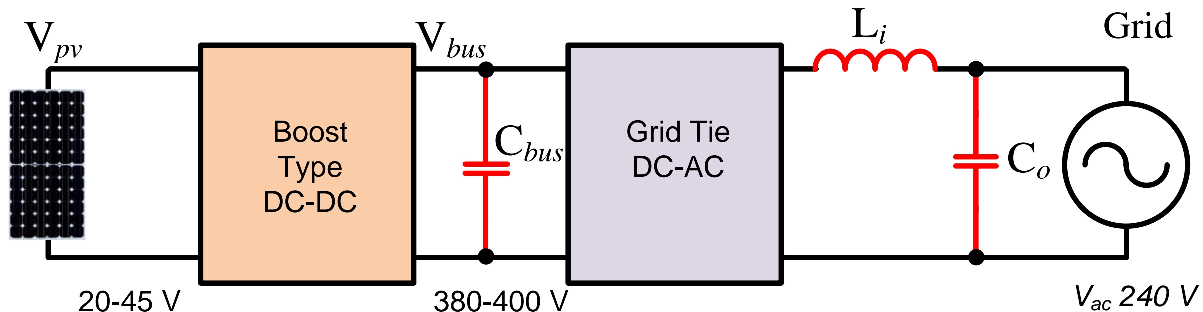


Figure 3.1: Major Passive Components of Two-stage Microinverter

3.1 CAPACITORS

The basic structure of a capacitor is two conductive plates (electrodes) that are separated by a dielectric material. The energy is stored in an electric field between the two plate electrodes. The equation for capacitance is given by

$$C = \frac{\varepsilon A}{d}$$

The capacitance is affected by the area of the electrode plate (A), the distance between the electrodes (d) and the permittivity of the dielectric material (ε). Larger capacitances can be obtained if the area of the electrodes are larger, however this increases the cost and size of the capacitor. Decreasing the distance between the electrodes can increase the capacitance but is limited by the dielectric breakdown field strength of the dielectric material. There are three main classes of capacitors that use different materials to achieve the voltage rating and capacitance values needed for different applications; film, ceramic and electrolytic.

The most important behavioral considerations for capacitors include the dissipation factor, temperature coefficient and DC-bias characteristic. The dissipation factor is the ratio of energy dissipated by the capacitor over the energy stored in the capacitor, a lower dissipation factor means that there are less losses in the capacitor. The resistive losses of the metal components, insulation resistance and dielectric losses are all included in the dissipation factor. Factors that affect the dissipation factor include the frequency of the ripple current through the capacitor as well as the dielectric material properties.

The temperature coefficient is the change in capacitance versus temperature. Generally as the temperature of the capacitor increases there comes a corresponding decrease in the capacitance. In an ideal capacitor there would be a constant capacitance with over all temperatures. How badly the temperature affects the capacitance is determined by the dielectric material.

The DC-bias characteristic is the change in capacitance with applied voltage. For some capacitor types when an external DC electric field is applied the orientation of the charges in the capacitor become fixed, which means that they cannot move with an applied AC field. The reduction in mobile charges means that their contribution to the dielectric constant is removed effectively decreasing the total capacitance. This effect is further exacerbated with an increase in applied DC electric field.

3.1.1 Film Capacitors

Film capacitors are widely used in most applications, they consist of a wide range of different materials with different dielectric constants. The most common materials for this class are polyester and polypropelene. A general physical construction of a film capacitor is shown in Figure 3.2 [29].

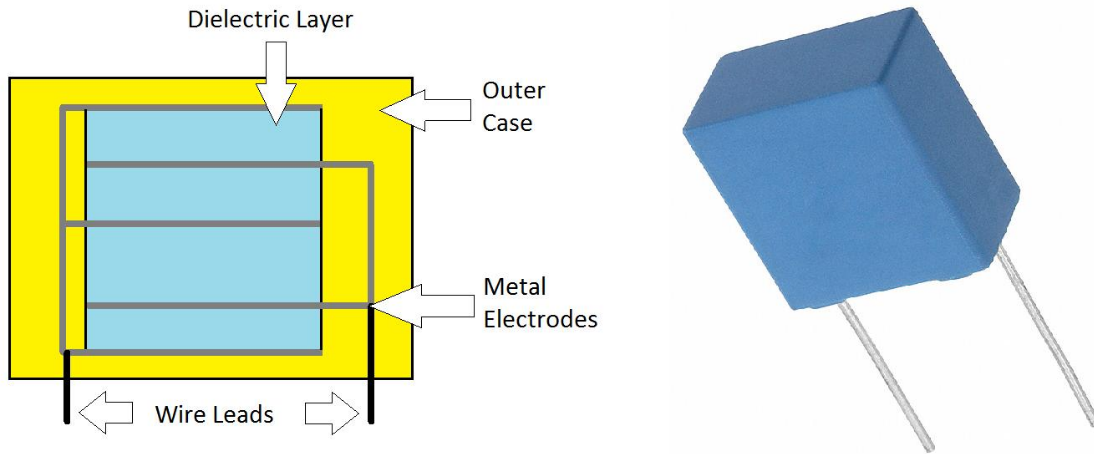


Figure 3.2: Film Capacitor Configuration

Film capacitors have the advantages of that can operate under conditions of high temperature, high tolerances, high reliability, stable capacitance and are non-polarized allowing them to be used in AC applications. The inherent structure of a film capacitor is similar to that of several capacitors in parallel this means that the parasitic resistances and inductances are very low for this class of capacitor. Film capacitors using the polyester material are the most common this is due to the low cost and high permittivity of the dielectric material for film capacitors. The problem with polyester is that it has the highest dissipation factor as well as the worst temperature coefficient among the other film capacitor types. The next most common type of film capacitor is polypropelene it has very low dissipation factor, high dielectric strength and low temperature coefficient. Polypropelene's biggest disadvantage is that its relative permittivity is very low causing the size of the capacitor to be larger compared to polyester for the same capacitance value [30], [31]. Key characteristics of the film capacitor materials are:

Material Characteristics	Polyester	Polypropelene
Permittivity ε (at 1 kHz)	3.3	2.2
Dielectric Strength (V/um)	580	650
Temperature Coefficient (ΔC/C) %	5	2.5
Dissipation Factor (at 1 kHz) %	0.4	0.015

Table 3.2: Film Capacitor Material Properties [32]

Compared with other capacitor types, film capacitors offer the best characteristics of dissipation factor, low parasitic elements, no DC bias characterisitic and low temperature coefficient. The biggest disadvantage of film capacitors are the low permittivity causing the capacitor size to be very large compared with capacitors made from other materials. Among the film capacitor materials polypropelene has the advantage in circuits with large AC components at high frequencies, while polyester would be better suited for applications that require larger capacitance with little AC ripple.

3.1.2 Ceramic Capacitors

The capacitor type that is used the most widely used in all electronic designs are ceramic capacitors. The high permittivity of the ceramic material allows the volume of ceramic capacitors to be very small. There are two main classes of ceramic capacitor class 1 and class 2. The physical construction of multilayer ceramic chip capacitors shown in Figure 3.3 are very similar to film capacitors.

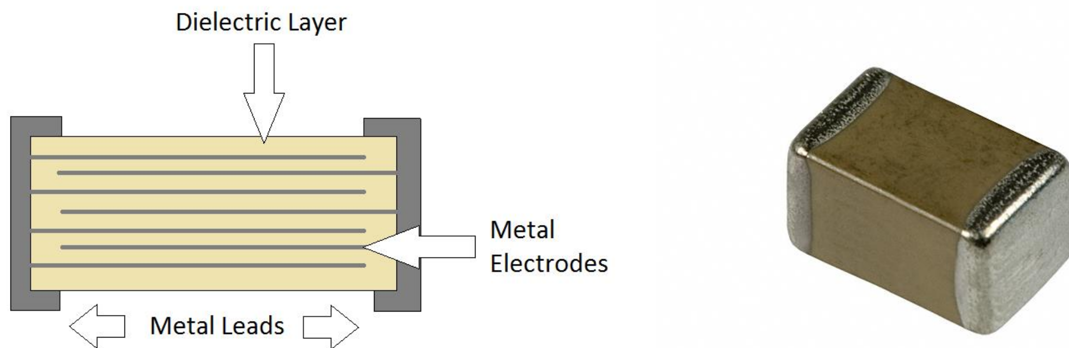


Figure 3.3: Multilayer Ceramic Chip Capacitor Configuration

Ceramic capacitor's main advantage is that the high dielectric constant of the material affords the ability to make a high capacitance over a small size. Ceramic capacitors are non-polarized and can be used in AC circuits. Since the physical structure is similar to film capacitors the parasitic inductances and resistances are very low. Since there are no wire leads on a surface mount ceramic capacitor the parasitic resistances can be lower than film capacitors. Class 1 ceramic capacitors consist of a paraelectric ceramic material, which is crystalline in composition [33]. Since paraelectric materials do not have a permanent electric dipole, DC bias does not affect the capacitance and is constant regardless of applied voltage [34]. The temperature coefficient of class 1 ceramic capacitors is constant and very low over all temperature ranges. Class 1 ceramic capacitors also have a very low dissipation factor. The

biggest disadvantage of class 1 ceramic capacitors is the low permittivity compared with class 2 ceramic capacitors. The classification codes for class 1 ceramic capacitors are:

Temperature Coefficient 10^{-6}/K Letter Code	**Multiplier of the Temperature Coefficient Number Code**	**Tolerance of the Temperature Coefficient Letter Code**
C: 0.0	0: -1	G: ±30
B: 0.3	1: -10	H: ±60
L: 0.8	2: -100	J: ±120
A: 0.9	3: -1000	K: ±250
M: 1.0	4: +1	L: ±500
P: 1.5	6: +10	M: ±1000
R: 2.2	7: +100	N: ±2500
S: 3.3	8: +1000	
T: 4.7		
V: 5.6		
U: 7.5		

Table 3.3: Class 1 Ceramic Capacitor Letter Codes for Temperature Coefficients. J. Prymak, M. Randall, P. Blais, and B. Long, "Why that 47 uF capacitor drops to 37 uF, 30 uF, or lower," Proceedings CARTS USA, 28 Symposium for Passive Electronics, 2008. Used under fair use, 2014.

The most commonly used class 1 ceramic capacitor is C0G (NP0), according to Table 3.3 the temperature drift is 0 with a tolerance of ±30 ppm/K [34].

Class 2 ceramic capacitors consist of a ferroelectric ceramic material [33]. Ferroelectric materials have a permanent electric dipole, DC bias greatly affects the capacitance and decreases over increasing applied voltage [34]. The temperature coefficient of class 2 ceramic capacitors is not constant and can vary greatly over all temperature ranges. Class 2 ceramic capacitors also have a very high dissipation factor. The greatest advantage of class 2 ceramic capacitors is the high permittivity. Classification codes for class 2 ceramic capacitors are:

Letter Code for Low Temperature	**Number Code for Upper Temperature**	**Letter Code for Change of Capacitance Over Temperature Range**
X : -55 °C	4 : +65 °C	P: ±10%
Y : -30 °C	5 : +85 °C	R: ±15%
Z : +10 °C	6 : +105 °C	S: ±22%
	7 : +125 °C	T: +22/-33%
	8 : +150 °C	U: +22/-56%
	9 : +200 °C	V: +22/-82%

Table 3.4: Class 2 Ceramic Capacitor Letter Codes for Temperature Coefficients. J. Prymak, M. Randall, P. Blais, and B. Long, "Why that 47 uF capacitor drops to 37 uF, 30 uF, or lower," Proceedings CARTS USA, 28 Symposium for Passive Electronics, 2008. Used under fair use, 2014.

A commonly used class 2 ceramic capacitor is X7R, going by Table 3.4 the temperature range is from -55 °C to +125 °C with a maximum capacitance change of ±15% [34]. Comparison the DC bias effects on the capacitance is shown for both class 1 (NP0) and class 2 (X7R) ceramic capacitors in Figure 3.4.

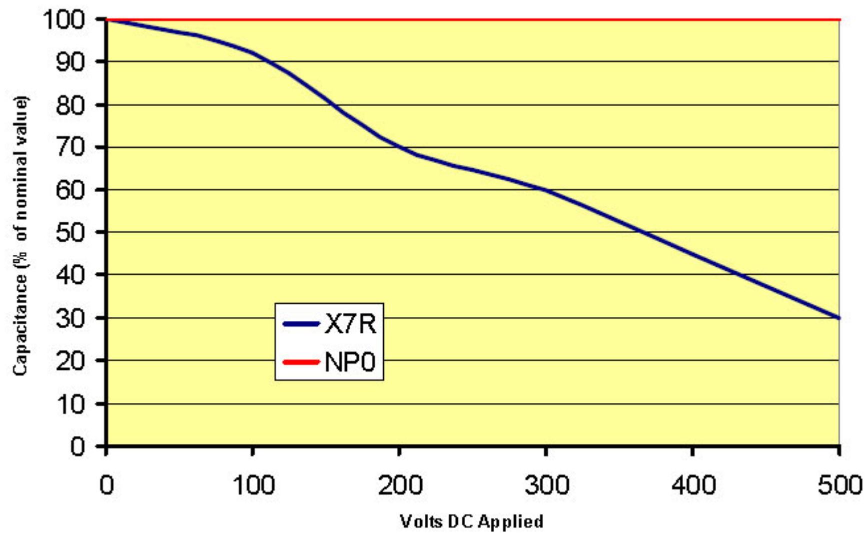


Figure 3.4: DC Bias Effects on Ceramic Capacitors. Johanson Dielectrics, "Basics of Ceramic Chip Capacitors," (December 1, 2007). Available: http://www.johansondielectrics.com/technical-notes/product-training/basics-of-ceramic-chip-capacitors.html. Used under fair use, 2014.

From the graph it is clear that the capacitance of class 1 type capacitors is constant with applied voltage, while the class 2 capacitance decreases with increasing applied voltage [35]. The temperature effects on capacitance for both classes of capacitors are shown in Figure 3.5.

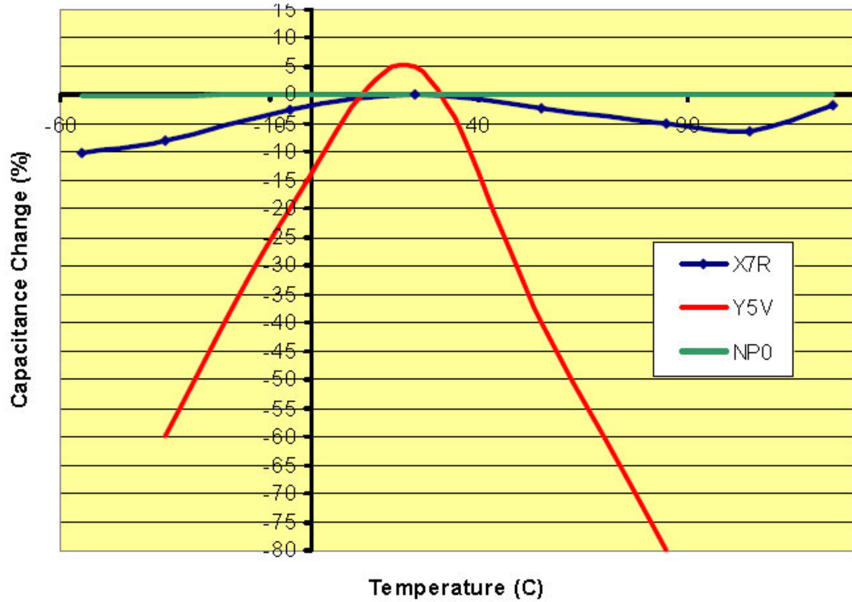


Figure 3.5: Temperature Coefficient Effects on Ceramic Capacitors. Johanson Dielectrics, "Basics of Ceramic Chip Capacitors," (December 1, 2007). Available: http://www.johansondielectrics.com/technical-notes/product-training/basics-of-ceramic-chip-capacitors.html. Used under fair use, 2014.

The capacitance of class 1 type capacitors is constant over the entire temperature range, while the class 2 capacitor changes at different temperatures [35]. Within the class 2 capacitors X7R has minimal capacitance change (up to ±15%) compared with the Y5V (from +22 to -82%). Key characteristics of ceramic capacitors are shown in Table 3.5.

Material Characteristics	Class 1 (NP0)	Class 2 (X7R)
Permittivity ε (at 1 kHz)	12	800
Dielectric Strength (V/um)	100	35
Temperature Coefficient (ΔC/C) %	0.3	15
Dissipation Factor (at 1 kHz) %	0.1	2.5

Table 3.5: Ceramic Capacitor Material Properties [32], [35], [36]

When comparing ceramic capacitors with film capacitors, class 1 ceramics have better characteristics except for dissipation factor and dielectric strength. The capacitance of class 1 ceramic capacitors is limited for higher voltages due to the low dielectric strength. The low dissipation factor and minimal temperature coefficient make class 1 ceramic capacitors ideal for resonant circuits and other circuits that require constant capacitance. Class 2 ceramic capacitor only advantage is the higher permittivity. The DC bias characteristic of the material relegates the use of class 2 ceramic capacitors to decoupling or bypass circuits.

3.1.3 Electrolytic Capacitors

The last major type of capacitor is the electrolytic capacitor. When applications require a large amount of capacitance, electrolytic type capacitors have one of the highest capacitance densities available. Aluminum wet electrolytic capacitors is the most commonly used electrolytic capacitor. The construction of an aluminum wet electrolytic requires using two aluminum foils where one has an insulating oxide layer. Between the two foils is a paper spacer soaked in electrolytic fluid. After stacking the materials it is then rolled into a cylindrical shape and placed inside an aluminum casing [37]. A cross section of the capacitor is shown in Figure 3.6.

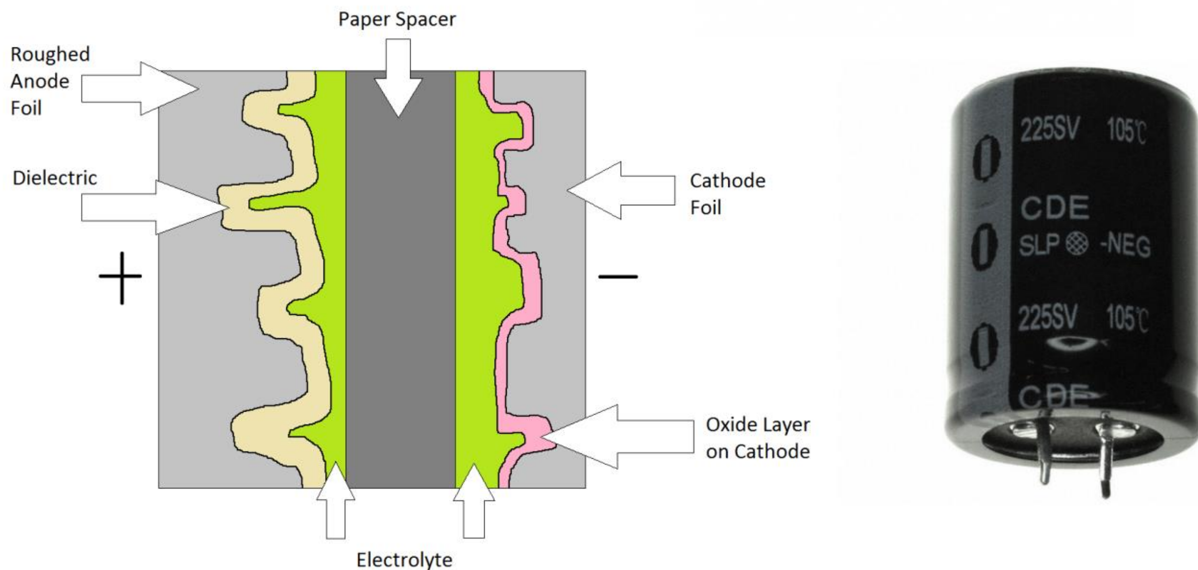


Figure 3.6: Aluminum Wet Electrolytic Capacitor Configuration

The oxide layer on the anode is the main dielectric component in the capacitor and since the thickness of the oxide is very small the capacitance that can be achieved is very high. Electrolytic capacitors are a polarized device and applying a reverse bias voltage will cause a breakdown in the dielectric material, this means that electrolytic capacitors can only be used in DC circuit applications. The biggest advantages of the aluminum electrolytic capacitor is the ability to achieve high capacitances with minimal cost. Aluminum electrolytic capacitors have very poor dissipation factor as well as large capacitance variations with temperature. Capacitance falls off rapidly and dissipation increases when the temperature of the electrolytic capacitor is below room temperature [37]. Characteristics of aluminum electrolytic capacitors are shown in Table 3.6.

Material Characteristics	Aluminum Electrolytic
Permittivity ε (at 1 kHz)	9.6

Dielectric Strength (V/um)	710
Temperature Coefficient (ΔC/C) %	8
Dissipation Factor (at 1 kHz) %	8

Table 3.6: Material Characteristics of Aluminum Electrolytic Capacitors [36], [38]

Aluminum electrolytic capacitors have a very high dielectric strength compared with other capacitor types, but the voltage rating is limited by the amount of oxide that can be grown on the anode foil. The capacitance above room temperature is increase for aluminum electrolytic capacitors this is due to the viscosity of the electrolytic fluid decreasing allowing improved conductivity. The optimal applications for aluminum electrolytic capacitors is coupling and ripple reduction of the voltage in DC-DC power converters.

3.1.4 Capacitor Lifetime

With the expansion of power conversion systems in renewable applications there is an increased concern with the lifetime of the electrical systems. Most PV panel manufacturers rate the lifetime of the PV panel to approximately 25 years. This means that the electrical components should also meet this lifetime in order to maintain an adequate costs versus power generation ratio. The major source of concern of failure in PV systems is the type of capacitor used.

Comparing the rate of decay for different capacitor types show that the performance of film capacitors is very good. The major source of performance reduction in film capacitors is the deformation of the dielectric during the circuit assembly procedure. The internal ESR of the capacitor increases as a result and the internal heat increases [39].

Class 2 ceramic capacitors decay through the ferroelectric process. Similar to the DC bias as the polarization of the dipoles decays or remains immobile the permittivity decreases causing the capacitance to decrease. This effect is prevalent in class 2 ceramic capacitors and not in class 1 ceramic capacitors. The effect or decay in class 2 ceramic capacitors can be reversed by heating the material above the Curie point to reset the dipoles. Class 1 ceramic capacitors does not face the accelerated aging of class 2 ceramic materials and is dependent on the natural degradation of the material due to the external influences [40].

Aluminum electrolytic capacitors are affected the most by external influences and circuit operation. The key point of issue is the electrolytic fluid in the capacitor. At lower temperatures the electrolytic fluid becomes too viscous increasing the parasitic series resistance in the capacitor. At higher temperatures the electrolytic fluid is susceptible to drying out. High ripple currents affect the

decay of the electrolytic capacitor with lower frequency ripple currents having more of a detrimental effect than high frequency ripple currents. Not using the electrolytic capacitor also affects the lifetime because the wet electrolyte will dry out, this can be seen in old equipment that hasn't been powered in years. An industry standard for measuring the lifetime of electrolytic capacitors uses the Law of Arrhenius, which simplified doubles the life of the capacitor for each 10 °C below the operating temperature of the capacitor. The structure of the lifetime model is given by the equation

$$L = L_o K_T K_R K_v$$

The resulting lifetime is L, where the nominal lifetime from the datasheet is L_o, K_T is the temperature factor, K_R is the ripple current factor and K_V is the voltage factor. The temperature factor K_T is from the Law of Arrhenius and is given as

$$K_T = 2^{\frac{T_0 - T_A}{10}}$$

T_0 is the maximum temperature rating of the capacitor and T_A is the ambient temperature. The impact of the ripple current can be determined by

$$K_R = K_i^{A * \frac{\Delta T_0}{10}} \quad where \quad A = 1 - \left(\frac{I_A}{I_R}\right)^2$$

I_A is the current ripple for the specified application, I_R is the nominal ripple current at the maximum temperature rating, ΔT_0 is the core temperature increase of the capacitor and K_i is an empirical safety factor depending on the maximum temperature rating [41]. Through the use of the lifetime estimation it is possible to design the system with electrolytic capacitors to have a long life. Long life for electrolytic capacitors is not guaranteed due to the fact that most of the assumptions are based on ideal operating conditions.

3.1.5 DC link Capacitor Selection

In two-stage microinverters the dc link capacitor acts as a buffer to prevent the double line voltage ripple from going back to the PV module it needs to be sized correctly in order to ensure the ripple on the dc link is not too high and that there is enough storage capacity for the low frequency

ripple. Using the power balance of the dc link capacitance equation (3) the required capacitance can be calculated using the input power (P_{in}), grid frequency (f_g) and voltage ripple on the capacitor ΔV_{dc}. The instantaneous output power of the inverter is

$$P_{out}(t) = \sqrt{2}V_{grid}\sin(w_{grid}t) * \sqrt{2}I_{grid}\sin(w_{grid}t)$$

This can be rearranged in terms to relate it to the input power

$$P_{out}(t) = V_{grid}I_{grid} * (1 - \cos(2w_{grid}t))$$

Where

$$V_{grid}I_{grid} = P_{in}$$

Giving a final equation of

$$P_{out}(t) = P_{in} * (1 - \cos(2w_{grid}t)) = P_{in} - P_{in}\cos(2w_{grid}t)$$

Using the equation for energy storage of a capacitor, the capacitance can be related to the output power

$$\int [P_{out}(t) - P_{in}]dt = \frac{1}{2}C_{bus} * (V_{dcmax}^2 - V_{dcmin}^2)$$

Relating the energy in the capacitor to the voltage ripple on the capacitor by

$$(V_{dcmax}^2 - V_{dcmin}^2) = 2 * V_{dc} * \Delta V_{dc}$$

Integrating the output power and setting it equal to the energy in the DC link capacitance can give and equation relating the system parameters to the DC link capacitance.

$$C_{bus} = \frac{P_{in}}{2\pi f_g * V_{dc} * \Delta V_{dc}}$$

The use of electrolytic capacitors is not advised due to their high series resistance which increases with low frequency ripple that is present on the DC bus. For ceramic capacitors the class 1 cannot achieve high enough capacitance and would require a large amount of parallel capacitors to achieve the desired capacitance. Class 2 ceramic capacitors suffer from the DC bias capacitance reduction and would also require a large number of parallel capacitors. To improve circuit operation it is recommended that film capacitors are used. Among the film capacitor types, polyester would be a more suitable choice for the DC link capacitor due to the lower cost and higher permittivity. The only downside to using film capacitors is the increased size and cost over using electrolytic capacitors.

3.1.6 Output Capacitor Selection

After determining the output inductor the output capacitance (C_o) can then be calculated using and selecting a cutoff frequency f_c around one-tenth of the switching frequency.

$$C_o = \frac{1}{(2\pi f_c)^2 * L_i}$$

A damping resistor should be placed in series with the output capacitor to avoid resonance with the grid impedance. The main considerations for the capacitor type to be used in the output capacitor is that the purpose of the output capacitor is to filter out the inverter switching noise in the output voltage. Since the output voltage is AC polarized capacitors cannot be used and since the voltage ripple is high frequency a capacitor with low ESR and dissipation factor should be used. To choose between a film capacitor and type 1 ceramic capacitor is more related to safety. Capacitors receive an additional safety rating called X or Y.

For X capacitors they are placed directly across the output, their main consideration is that its failure must cause a fuse or circuit breaker to open. The Y capacitors are from the line to earth ground and are not used for the output filter but for EMI considerations, and has the potential of causing shock to the user due to the chassis connection. The main advantage of using film over ceramic capacitors is that film capacitors exhibit a self-healing mechanism. This means that when there is a large voltage spike that fails the capacitor the metallization heats up and melts, the area around the breakdown is cleared and there is no short circuit [42]. Between the film capacitors polypropelene is the better material due to the low dissipation factor causing the temperature of the capacitor to remain low.

3.2 INDUCTORS

The basic structure of an inductor is any conductive material that has current flowing through it. A magnetic field is generated by the current flow, the magnetic field can be increased if there are more loops of the same conductor within vicinity of each other, which is caused by magnetic flux linkage. Introducing a ferromagnetic material within the field generated by the coils of the conductor increases the magnetic flux by inducing magnetization of the material. Inductance can be determined using

$$L = \frac{d\varphi}{di}$$

The inductance is determined by the amount of magnetic flux (ϕ) generated by a given current (i) [43]. The magnetic flux can be affected by the properties of the material that are enclosed by the current carrying conductors. The permeability of the material plays a major role in setting the inductance and can be considered an amplification factor of the magnetic flux. Of the ferromagnetic materials used for high frequency power conversion systems the most widely used are ferrite and powder alloy.

The most significant characteristic of an inductor is the core loss generated within the structure. Core loss is the result of a changing magnetic field. In ferromagnetic material the magnetic moments are aligned and rotate in response to a change in the magnetic field. The core loss occurs when particles cannot move in conjunction with the other particles, these particles are then forced to move back into alignment and generate losses in the form of heat. The term for this type of core loss is hysteresis. Another form of core loss is eddy currents, which are currents generated in the core by the magnetic field if the material is conductive [43]. Since ferrite and powder alloys are non-conductive materials there are minimal core losses due to eddy currents when operating at low frequencies.

The other major mechanism of loss in the inductor is the conduction loss that occurs in the windings of the inductor. The resistive loss of the windings in an inductor are

$$P_{copperloss} = {I_{rms}}^2 R$$

R is the DC resistance of the wire and I_{rms} is the current flowing through the inductor. The resistance of a solid conductor is given in

$$R_{dc} = \rho \frac{l}{A_w}$$

The resistivity of the material is ρ, the length of the conductor is l and the cross sectional area of the conductor is A_w. The problem is that the resistance of the conductor consists of not only the DC resistance, but also an AC resistance created by the high frequency ripple in the current. The current flowing through a conductor introduces a magnetic flux, the magnetic flux introduces eddy currents that oppose the magnetic flux. The eddy currents force the current to flow to the surface of the conductor. In the cross sectional area is large then there is the possibility that some of the area of the conductor is not used in the current flow. The penetration depth of the conductor material can be determined using the equation of skin depth

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

The skin depth (δ) is determined by the resistivity of the material, the permeability of the material (μ) and the frequency (f) of the current ripple through the conductor [43]. When there are multiple conductors in close proximity to one another there is a generation of flux that tries to induce a current on the adjacent wire. As a result the induced current opposes the current on the section of the conductor closest to the other conductor, this causes the main current to redistribute to the other side of the conductor effectively increasing the AC resistance. Combining the skin and proximity effects the AC resistance can be determined using

$$R_{ac} = \frac{h}{\delta} R_{dc}$$

Where R_{dc} is the resistance of the conductor with no AC component and the width of the conductors is h [43].

3.2.1 Ferrite

The most commonly utilized material for power conversion systems is ferrite. Ferrite consists of an iron oxide (Fe_2O_3) combined with other metals. Frequently used metal combinations for power

conversion applications include manganese-zinc (Mn-Zn) and nickel-zinc (Ni-Zn). The resistivity of the ferrite material is very high preventing the creation of current in the core material via eddy currents. The resistivity of Mn-Zn is around 1 Ωm compared with 10000 Ωm for Ni-Zn [43]. The higher resistivity of Ni-Zn means that the material is more suitable for higher frequencies (above 1 MHz) where the potential to induce eddy currents is higher [43]. Below the 1 MHz operational frequency Mn-Zn is preferred due to the higher permeability and saturation flux density over Ni-Zn [43]. Since ferrite is a ceramic material it can be formed into a variety of different shapes as shown in Figure 3.7.

Figure 3.7: Different Ferrite Shapes for Power Conversion Applications

The main advantage of ferrite is its low core loss compared with other magnetic materials due to the low eddy current effects on the core. Another benefit that ferrite has with core loss is the relative consistency of the atomic structure characterized by the high permeability of the material. This high permeability reduces the hysteresis losses that are generated by the particles moving with the applied magnetic field by allowing a more unimpeded path for the particles to move.

The disadvantages of using ferrite include the change in permeability with temperature, low saturation flux density limit, abrupt core saturation and fringing flux. For ferrite as the temperature increases the permeability increases over a wide range. This is evident in the graph of EPCOS ferrite material N97 showing the permeability versus temperature in Figure 3.8.

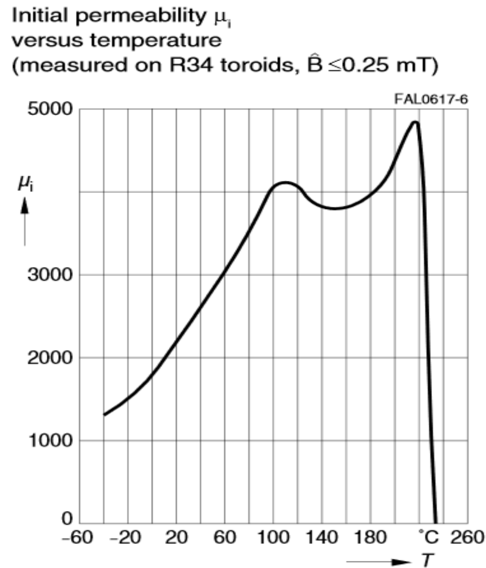


Figure 3.8: Permeability vs. Temperature for EPCOS N97 Ferrite. EPCOS, "Ferrites and accessories," N97 datasheet, Sept. 2006. Available: http://www.epcos.com/blob/528886/download/4/pdf-n97.pdf. Used under fair use, 2014.

The change in permeability affects the inductance and applications with a wide temperature variation could experience operational issues. Low saturation flux density is another potential problem with ferrite. The saturation flux density for ferrite is around 0.4 to 0.5 Tesla and this value decreases as temperature increases [44]. Figure 3.9 shows the saturation flux density for EPCOS N97 ferrite at 25° C and 100° C.

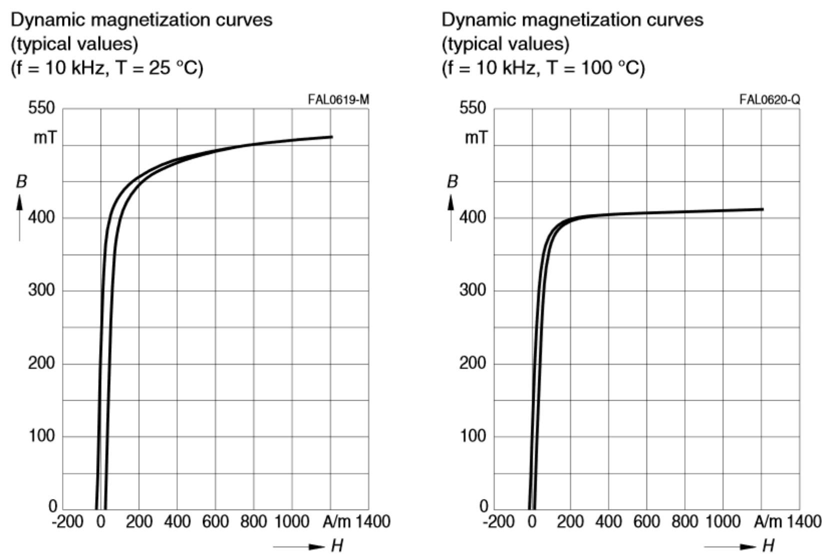


Figure 3.9: Saturation Flux Density Curves for EPCOS N97 Ferrite. EPCOS, "Ferrites and accessories," N97 datasheet, Sept. 2006. Available: http://www.epcos.com/blob/528886/download/4/pdf-n97.pdf. Used under fair use, 2014.

From the graphs the saturation flux density at room temperature is around 0.5 T and at 100° C this value drops down to about 0.4 T. Core saturation for ferrite is very abrupt with a sharp decrease in the inductance as the current increases. In order to ensure that the inductor does not saturate an air gap has to be used in the material. The air gap shifts the location of the saturation point further out with respect to current. Adding the air gap decreases the permeability of the material and creates an effect at the area of the gap called fringing shown in Figure 3.10.

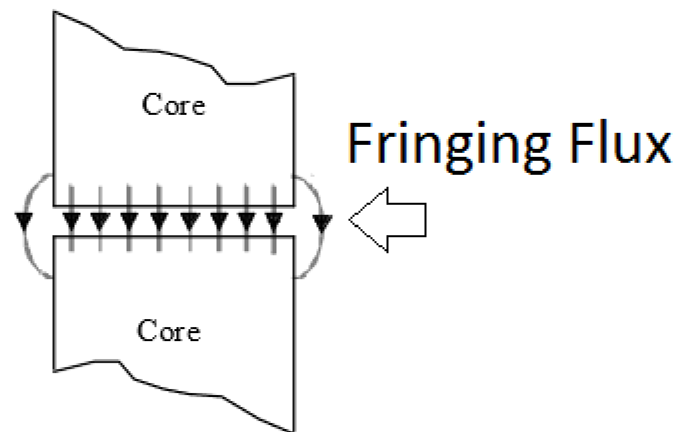


Figure 3.10: Fringing Flux across a Gapped Ferrite

Fringing tries to reduce the reluctance of the gap between the magnetic materials this causes an increase in the inductance [45]. Another side effect of fringing is that if there are conductors within vicinity of the fringing flux, there are eddy currents induced in the conductors cause the AC resistance to increase.

3.2.2 Powder Core

Another widely used material for magnetics in power conversion applications includes powder core material. Powder core material consists of iron powder mixed with an insulation material and compressed into a toroidal shape. The mixture of the iron powder with the insulating material gives a distributed air gap. Permeability of powder core magnetics are low due to the distributed air gap. The permeability is set by the size and distance of the iron particles, with the distance of the iron particles being set by the insulation material. The resistivity of powder core is on the same order as Mn-Zn ferrite, which is around 1 Ωm [43]. This means that the effects of eddy currents are minimal for frequencies below 1 MHz. Due to the nature of the insulating material and the bonding agents required

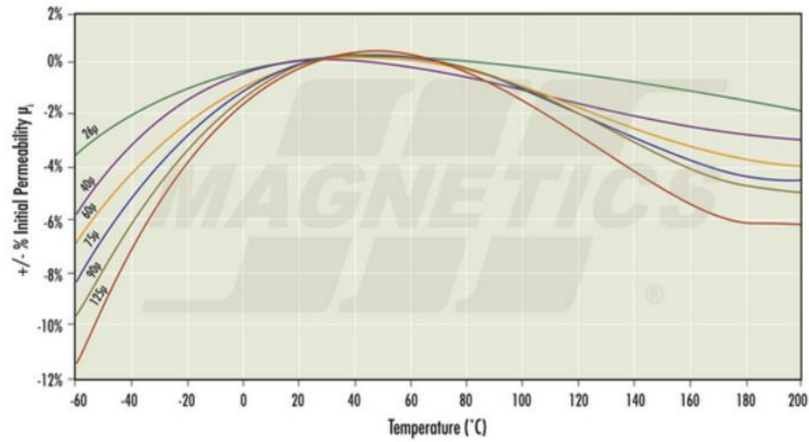
to ensure a solid form, the shapes for powder core are relegated to mainly toriods [46]. There are three main types of powder core material with different characteristics; molypermalloy powder (MPP), high flux, and sendust (Kool Mu) shown in Figure 3.11.

Figure 3.11: Magnetics Inc Powder Core Toroids, MPP (Grey), High Flux (Tan), Kool Mu (Black)

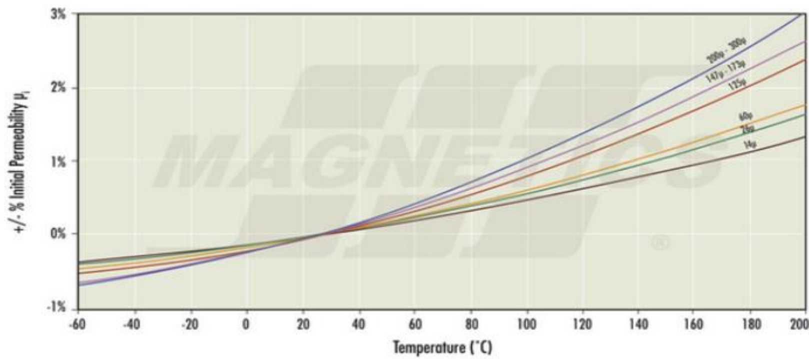
MPP core material composition consists of 80% nickel and 20% iron [46]. The core loss of MPP is the lowest among the powder core materials along with a higher permeability. Compared to ferrites and other powder core materials the cost of MPP cores are very high. For high flux material the core consists of 50% iron and 50% nickel [46]. The saturation level for high flux is the greatest compared to the other powder cores, around 1.5 T [43], [46]. Permeability of high flux is constant with high DC bias and the core size can be very small compared to the standard powder core material sendust. Sendust is one of the earliest powder core materials, with a composition of iron, silicon and aluminum. The saturation level of sendust is around 1.0 T which is between high flux and MPP [46]. The permeability of sendust is very low and can maintain its permeability with DC bias but not as well as high flux. Sendust is the cheapest powder core to make due to the fact that there is no nickel in the core material. It is possible to form U and E core shapes using sendust.

The advantages to using powder core material is the constant permeability with temperature, high saturation level, and softer inductance roll off at the saturation level compared to ferrite. Figure 3.12 shows the permeability versus temperature for Magnetics Inc three powder core types.

Permeability versus Temperature Curves
Kool Mµ®



Permeability versus Temperature Curves
MPP 14µ-300µ



Permeability versus Temperature Curves
High Flux

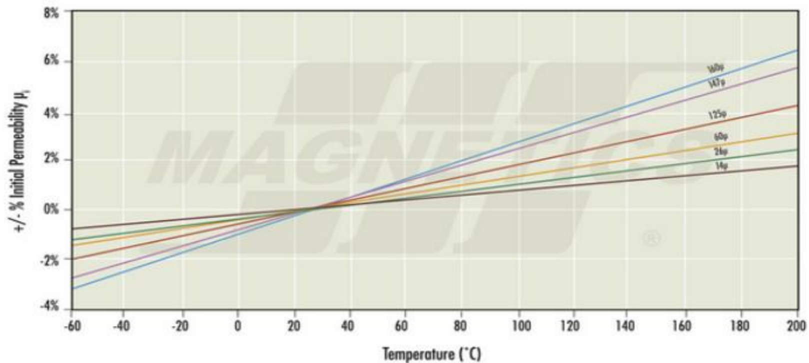


Figure 3.12: Permeability vs Temperature for Magnetics Inc Powder Core Materials. Magnetics Inc., "Powder Cores," Catalog, Bulter, Pennsylvania, pp. 3-14. Used under fair use, 2014.

From the graphs above MPP has the best temperature stability of the three powder core materials with a maximum deviation of 3% and sendust (Kool Mu) has the highest temperature deviation of 12%. The temperature deviation compared to ferrite for all three cases is minimal with ferrite having a permeability variation greater than 50% [47].

The saturation roll off for powder core material is not as abrupt as it is for ferrite [48]. Figure 3.13 shows a comparison between ferrite and powder core inductors with the same permeability.

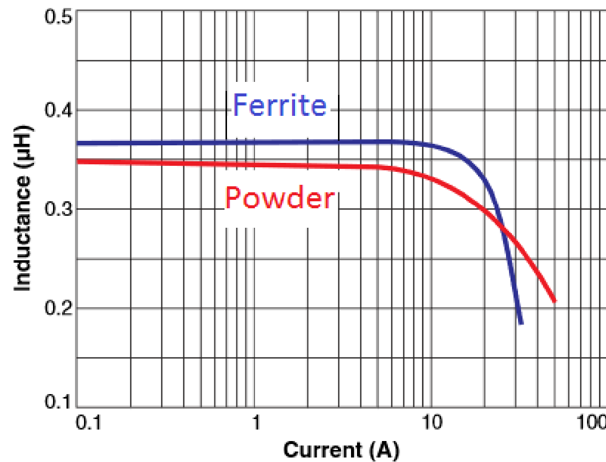


Figure 3.13: Inductance vs Current for Powder and Ferrite Core Inductors. Figure 1. L. Crane, "Ferrite and Powder Core Materials for Power Inductors," Coilcraft, Document 496-1, Feb. 2006, pp. 1-2. Used under fair use, 2014.

It is clear that the powder core inductor is able to maintain a higher inductance at higher currents.

The disadvantages of powder core are the low permeability, high core loss and cost. Since powder core materials naturally have a distributed air gap the permeability of the material is limited. This means that the number of turns required to achieve a specific inductance have to be very high or the use of the higher cost MPP material has to be used. Comparing the core loss between ferrite and all powder core materials are shown in Table 3.7.

Material	Core Loss (mW/cm^3)
MPP (125u)	2539.84
High Flux (125u)	5918.78
Sendust (125u)	4831.33
Ferrite (EPCOS N87)	375

Table 3.7: Core Loss of Various Magnetic Materials

The core loss for each material was calculated for a frequency of 100 kHz and an AC flux swing of 0.2 T. The N87 ferrite material from EPCOS is substantially lower than that of the powder core materials including MPP.

3.2.3 Inductor Filter Selection

The main purpose of the output inductor is to filter out the ripple from the high frequency switching of the inverter in the output current. The required inductance is calculated by using inductor volt-seconds balance and choosing a limit for the output current ripple Δi_{Li}. The inverter input voltage is represented as V_{dc}, inverter modulation index M and the switching frequency as f_{sw}. The inductor current is given by

$$V_L = L_i * \frac{di}{dt}$$

Volt-seconds balance for the inductor gives the inductor voltage as

$$V_L = V_{dc} - MV_{dc}\sin(wt) = V_{dc}(1 - Msin(wt))$$

Since maximum ripple occurs at the 50 % modulation index the inductance for specified system parameters can be calculated using

$$L_i = \frac{V_{dc}}{4 * \Delta i_{Li} * f_{sw}}$$

Designing the inductor for higher ripple will result in a lower inductance value and inductor size; however this comes at an increase of switching and conduction loss in the semiconductor devices. For the microinverter application the optimal material to use is ferrite. The high permeability and low core loss of the material outweighs any benefits provided by powder core material. Powder core material is more advantageous for higher current applications and since the maximum current that the output inductor would see is about 1.25 A_{rms} makes this advantage irrelevant. The other advantage of powder cores made irrelevant by the low currents in the microinverter system is the higher saturation limit. The temperature instability of ferrite’s permeability is addressed with the addition of an air gap in the material, which is already necessary in the design of an inductor.

3.3 Semiconductor Devices

The main component of any power conversion system is the semiconductor devices. Before the advent of solid state semiconductors, industry relied upon vacuum tubes to control the flow of power. With the emergence of silicon based bipolar devices the use of vacuum tubes in power systems was made obsolete. As the material processing of semiconductor material has improved the ability to implement semiconductor devices for higher power and voltage levels. New semiconductor device structures have also afforded the power converter designer the ability to operate systems at higher switching frequencies with improved efficiency. The two main purposes of power semiconductor devices is to control the direction of current flow in the case of rectifiers and to govern the amount of time that the current is flowing in the case of active power switches. Two major classes of rectifiers consist of Schottky diodes and P-I-N junction diodes. For active power switches the most commonly used devices are metal oxide semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs).

3.3.1 Schottky Diode

The simplest semiconductor structure is the Schottky diode, which consists of a semiconductor drift region in contact with metal. A Schottky rectifier structure is presented in Figure 3.14.

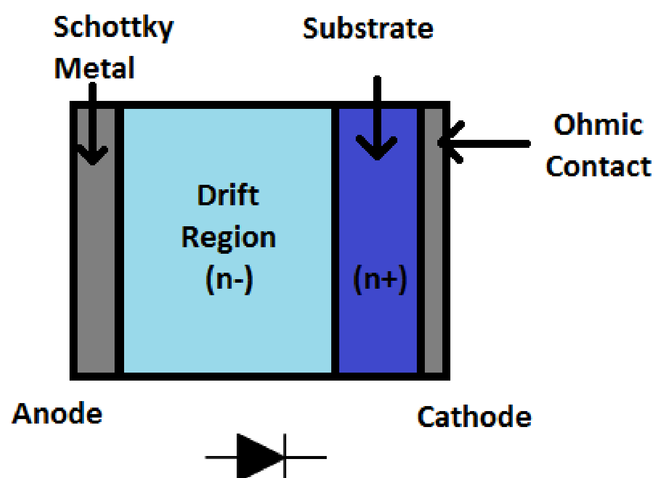


Figure 3.14: Schottky Rectifier Structure

When a reverse bias voltage is applied across the anode-cathode connection the voltage is solely distributed across the drift region given that the doping of the drift region is uniform. The outcome is that there is a triangular electric field distribution shown in Figure 3.15 [49]. The semiconductor device will undergo breakdown if the applied electric field is greater than or equal to the critical electric field of the semiconductor.

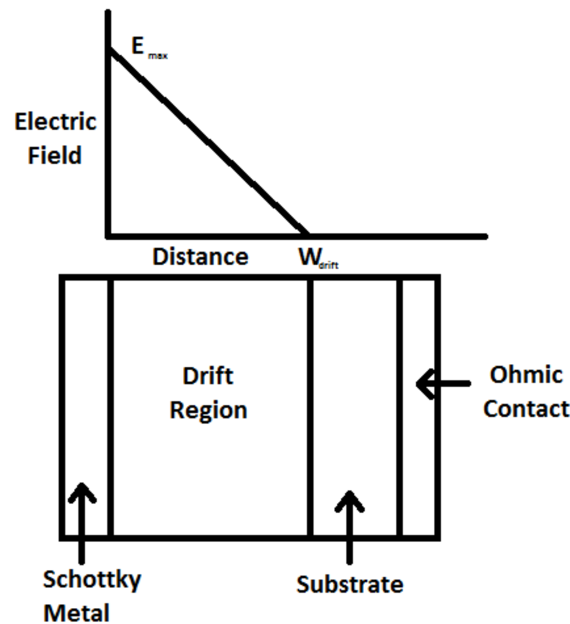


Figure 3.15: Electric Field Distribution of Schottky Diode

The next layer of the device is the substrate, whose purpose is to serve as a handle during the manufacturing of the device and to ensure that the secondary metal contact at the cathode has an ohmic characteristic [49]. Thickness of the drift region is very small and as a result an additional substrate layer is added to ensure rigidity of the semiconductor wafer. A metal-semiconductor contact is what forms a Schottky barrier and to ensure that there is only one barrier in a device the selection of the metal semiconductor interface needs to be specifically designed. To create a Schottky barrier connection there needs to be a difference between the energy required for an electron in the Fermi level position of metal to rest in free space (metal work function ϕ_M) with the energy required to move an electron from the conduction band of a semiconductor to free space (semiconductor electron affinity χ_S) shown in Figure 3.16 [49].

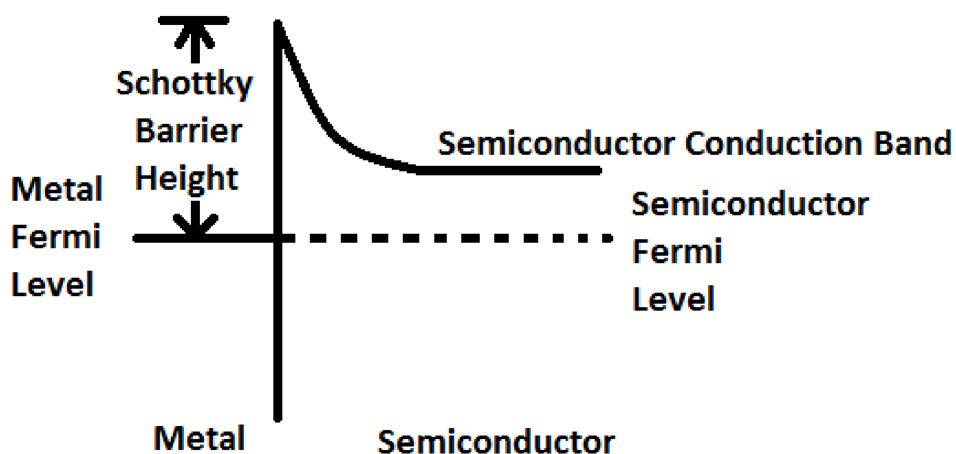


Figure 3.16: Energy Band Diagram for Metal-semiconductor Junction

If the barrier height is low then electrons can tunnel through the junction, this is achieved by selecting a metal with a low ϕ_M and having a high doping concentration in the semiconductor material [49]. An added benefit to the high doping concentration in the semiconductor material is a decrease in the resistivity of the material compared with the same material that has a lower doping concentration.

A Schottky diode is a majority carrier device meaning that the current transport through the device occurs as a result of movement of electrons from the semiconductor material into the metal over the Schottky barrier (thermionic emission current) [49]. Since the semiconductor material is lightly doped n-type material, whose free carriers are electrons, there can be no minority carriers involved in the current flow during conduction. The forward conduction power dissipation of the Schottky diode consists of the voltage drop across the metal-semiconductor junction, resistance of the drift region, resistance of the substrate region and resistance of the ohmic contact [49]. For a silicon based Schottky diode the forward voltage drop is dependent on the Schottky barrier height a lower barrier height means a lower forward voltage drop. Since the doping of the drift region is low the resistance of that region is higher compared with the resistance of the substrate region and its thickness is dependent on the desired blocking voltage. Resistance of the ohmic contact is set by the type of metal used and if the doping concentration of the substrate region is high enough a low contact resistance can be achieved. The major components of the forward conduction power dissipation are the drift resistance and forward voltage drop [49].

The biggest advantage of the Schottky diode is the absence of minority carriers in the drift region of the device. This means that the transition from the forward conduction state to the reverse

biased off state occurs quickly with no recovered minority charge to increase power dissipation allowing circuit operation at high frequency. The forward conduction loss of the Schottky diode is lower compared with standard silicon P-N junction diodes at 100 V or less blocking voltages.

Drawbacks to the Schottky diode include leakage current during the off state and low blocking voltages for silicon based devices. Leakage current of Schottky diodes occurs due to the low barrier height and similar to forward conduction the majority current carrier during this condition is due to thermionic emission. To reduce leakage current during the off state the Schottky barrier height has to be increased this results in an increase of conduction loss during the forward biased on state condition [49]. An increase in temperature of the device also lowers the barrier height and increases leakage current. Another effect that increases leakage current is barrier lowering as a result of increasing reverse bias voltage [49]. For silicon based Schottky diodes there is a limit on where it becomes advantageous to use in relation to the blocking voltage. In order to block higher voltages the thickness of the drift region has to be increased to sustain the electric field. When the breakdown voltage is below 100 V the resistance of the drift region is negligible and above 100 V the resistance of the drift region is significant to preclude the use of silicon Schottky diodes in high voltage applications.

3.3.2 P-I-N Diode

To overcome the blocking voltage limitation of Schottky diodes the silicon based P-I-N rectifier was developed for high voltage applications. Structurally the P-I-N diode is similar to the Schottky diode with the metal portion of the diode being replaced with a heavily doped p-type semiconductor region. The P-I-N rectifier structure is shown in Figure 3.17 [49].

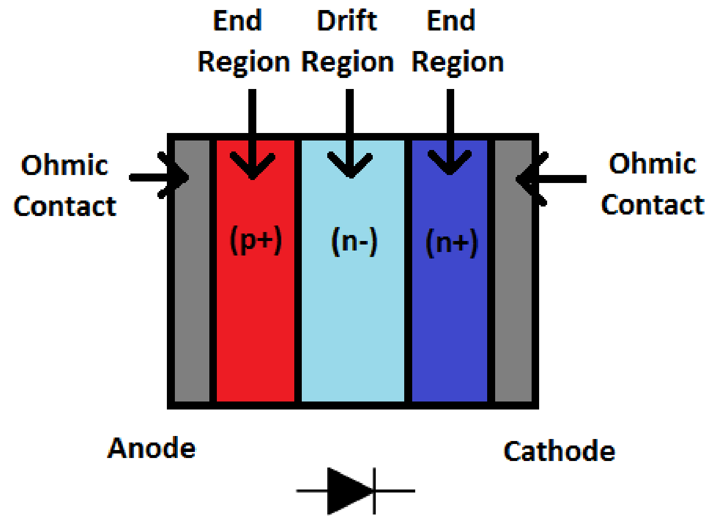


Figure 3.17: P-I-N Rectifier Structure

There are two possible field distributions when there is a reverse bias voltage is applied across the anode-cathode connection. The first field distribution has the electric field solely across the drift region of the device; the resulting field shape is triangular. This configuration of diode is called non-punch through (NPT). The other field distribution has some of the field distributed in the drift region with the remainder of the field dropped across the N+ end region. Electric field distribution in this design is trapezoidal in shape and is referred to as a punch-through (PT) rectifier. Field distributions for the NPT and PT diodes are shown in Figure 3.18 [49].

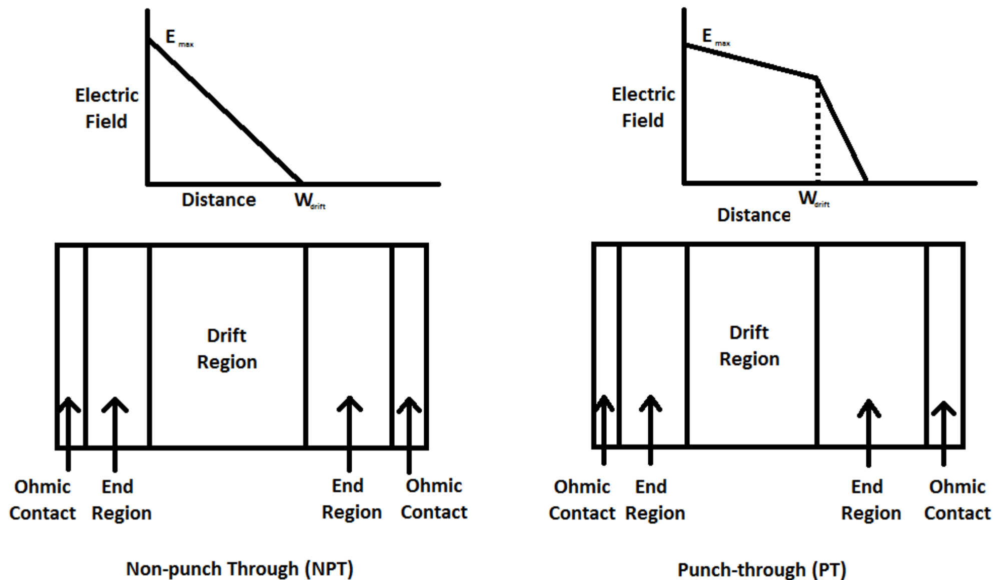


Figure 3.18: Electric Field Distribution of P-I-N Diodes

The doping of the drift region is using lightly doped N-type material, which is close to the doping levels of intrinsic semiconductor material (which is the I in P-I-N diode). Drift region width will be different between NPT and PT designs for the same blocking voltage. Since in the case of the NPT design the electric field is only across the drift region this means that the width of the drift region has to be wider than the PT design in order to support the entire electric field. For the PT design there is a gradual decrease in the electric field in the drift region with a rapid decrease in electric field in the N+ end region [49].

The purpose of both highly doped N+ and P+ end regions are to ensure that there is an ohmic contact on both terminals. These end regions also to provide minority carriers during operation in the forward conduction region. P-I-N diodes are a minority carrier device during which current transport occurs as a result of minority carrier injection into each semiconductor region. The levels of minority carriers injected into the drift region are higher than the doping levels of the material itself [49]. On-state conduction losses of the P-I-N diode are comprised of the voltage drop across the P-N junction, the voltage drop across the drift region and the voltage drop at the N+ end region [49]. For the PT diode the doping of the drift region is lower compared with the NPT diode with the same voltage blocking and current density characteristics. The lower doping of the drift region does not increase the conduction loss of the drift region due to the effects of the high minority carrier injection; this is referred to as conductivity modulation [49]. As a result the voltage drop in the drift region is reduced and is independent of the current density through that region. Conduction loss across the P-N junction is dependent on the minority carrier concentration in the drift region and the doping of the drift region. For the N+ region the losses are related to the majority carrier density and doping of the drift region [49].

P-I-N diodes can be utilized in higher voltage applications compared with silicon based Schottky diodes due to the lower forward voltage drop. Comparison between the two types of P-I-N diodes has the PT diode with a lower forward conduction loss due to the reduced thickness of the drift region.

The biggest drawback to the P-I-N diode is a result of its biggest advantage, the large concentration of minority carriers in the drift region to reduce the on-state conduction losses. During the transitions from the on-state to the reverse bias blocking state, the stored minority carriers have to be removed in order to generate the depletion region supporting the electric field. The time required for the diode to establish a steady-state open circuit off behavior is called reverse recovery time[49], [50]. Current through a P-I-N diode during the transition from the conducting state to the off-state is shown in Figure 3.19.

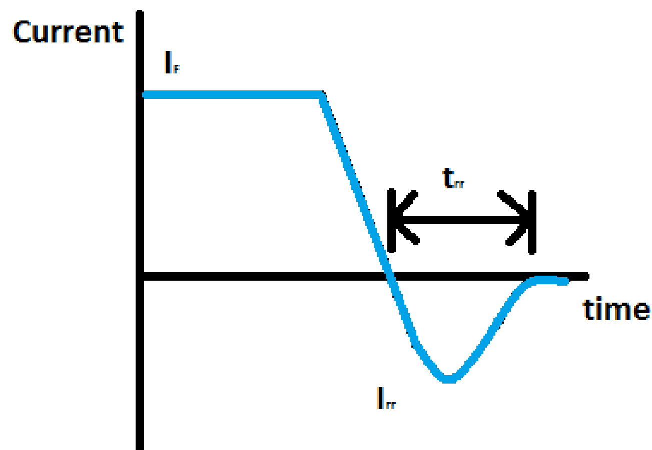


Figure 3.19: Current for P-I-N Diode during Reverse Recovery

When the voltage reverses across the diode the current linearly decreases and instead of stopping when the current reaches zero it continues to go in the negative direction. A peak reverse recovery current is reached and then the current reduces to a zero value for steady-state. The reverse current flows through the main active switch of the power electronics circuit increasing system losses. There is also a potential for the reverse current to effectively short out the power supply to the circuit. When comparing the two types of P-I-N diodes the reverse recovery characteristics are different between the NPT and PT designs. Since most of the majority carriers are located within the drift region the PT diode will exhibit lower reverse recovery time due to the thinner drift region requiring less time to remove the injected minority carriers [50]. The characteristic of the PT reverse recovery can be described as "snappy", which if there is a large recovery current there will be oscillations on the diode due to circuit parasitic inductances [50]. NPT diodes are classified as having a "soft" recovery limiting the oscillation of the diode at the cost of not being able to operate the circuit at high frequencies [50].

To reduce the reverse recovery there are manufacturing technologies used called lifetime control techniques [49]. Lifetime control introduces impurities into the semiconductor causes traps to form near the midgap of the energy bands [49]. This decreases the lifetime required for the mobile carriers to recombine back to their equilibrium state. The drawback to the lifetime reduction is the increase in on-state voltage drop due to the impurities introduced to the material.

3.3.3 MOSFET

In comparison with the diode rectifier structure, the metal oxide semiconductor (MOS) transistor is a voltage controlled active power switch that can be used to control the flow of current.

The first MOSFETs were using a lateral design and could not block high voltages. To overcome this problem a vertical structure was developed in order to use the device in high voltage applications. A basic vertical power N-channel MOSFET structure is shown in Figure 3.20.

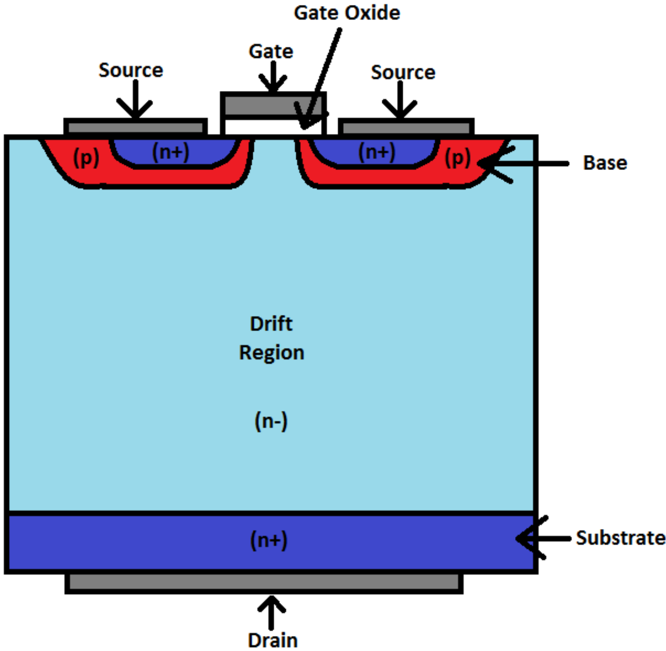


Figure 3.20: Vertical N-channel MOSFET Structure

Operation of a MOSFET involves the creation of a conductive channel along the surface of a semiconductor material below an insulating material that has a metal electrode with an applied voltage. For an N-channel MOSFET a positive voltage is applied to the gate this causes the P-type material base to invert to form an N-channel. Current flows from the source connection to the drain connection through the N-channel and the lightly doped drift region. For vertical power structures the N+ source and drain portions are separated by a P-base section [49]. In order to support high voltages across the device there is a lightly doped drift region that sustains the entire electric field.

MOSFETs are a majority carrier device where for a N-channel device only involves the flow of electrons [49]. Formation of the channel in the P-base region occurs when there is enough applied voltage to the metal gate electrode that causes the intrinsic level of the semiconductor to cross the Fermi level of the semiconductor. The positive gate charge repels the positive charge in the semiconductor material away from the semiconductor-oxide interface and increases the density of electrons. When there is sufficient gate voltage bias the high number of electrons form a channel in the case of a N-channel MOSFET, this condition is referred to as inversion [49]. Resistance of the channel

can be reduced by increasing the voltage at the gate electrode increasing the density of electrons in the channel. The gate voltage at which the channel transitions from having few electrons at the semiconductor-oxide interface to strong inversion of the channel is called the threshold voltage [49]. Threshold voltage is dependent on the thickness of the oxide and doping of the semiconductor region [49].

Power MOSFETs have an inherent parasitic N-P-N bipolar transistor formed by the source, P-base and the drift region. The bipolar transistor has a lower breakdown voltage compared with the breakdown voltage of the main device. Suppression of the parasitic bipolar transistor can be achieved by shorting the P-base region to the N+ source region through the metal electrode [49]. The connection from the P-base to the drift region creates and intrinsic body diode in the device from source to drain that conducts current when a forward bias voltage is put across the device shown in Figure 3.21.

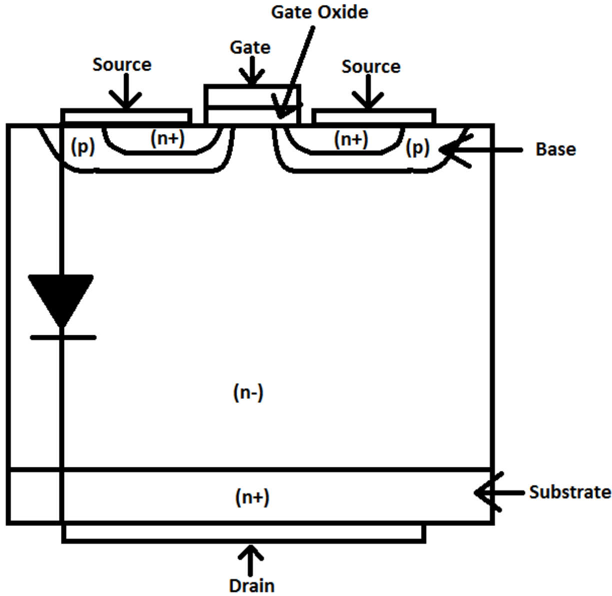


Figure 3.21: Intrinsic Body Diode of Power MOSFET

Reverse recovery performance of the internal body is very poor due to the long lifetime of the drift region. Similar to the P-I-N diode lifetime control processes can decrease the recovery time by injecting impurities into the drift region at the cost of increasing the resistance of the device [49].

The first commercially viable vertical power MOSFET structure is the vertical-diffused (VD) MOSFET shown in Figure 3.22 [49].

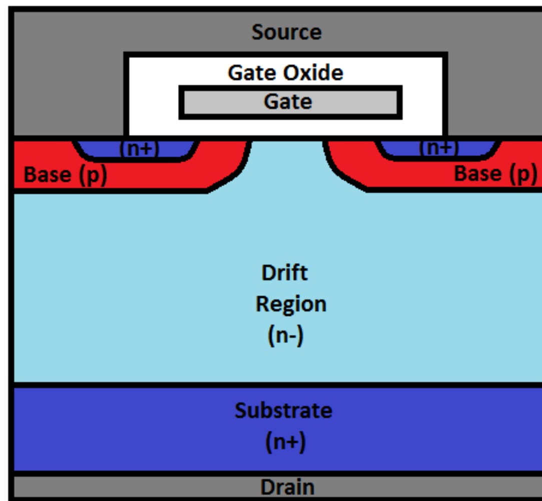


Figure 3.22: VD-MOSFET Configuration

A power device consists of multiple cells connected in parallel to increase the current capability. Different patterns and shapes can be used to increase the effective surface area of the semiconductor [49]. Breakdown of the internal resistive components of the VD-MOSFET are shown in Figure 3.23.

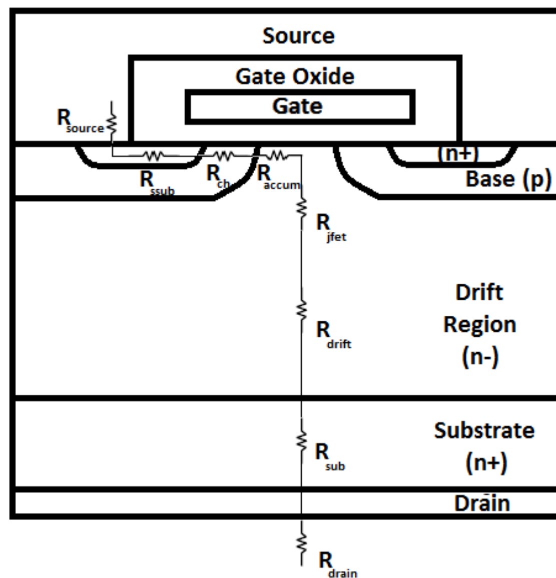


Figure 3.23: VD-MOSFET Internal Resistive Components

For high voltage MOSFETs the resistive portions that make the most contributions to the device's overall resistance include the drift region resistance (R_{drift}), jfet resistance (R_{jfet}) and the channel resistance (R_{ch}). R_{ch} is based on the thickness and doping level of the P-base region [49]. R_{drift} is one of the biggest contributors to the device's on resistance (R_{on}), which relies heavily on the required breakdown voltage to determine the thickness and doping [49]. The other major contributor to R_{on} is the R_{jfet} region and is a result of the depletion region formed between the drift region and P-base constricting the current flow through the drift layer. R_{jfet} effects on the resistance are based on the thickness of the P-base region and the width of the gate. The other substrate and contact resistances are minimal compared to the three main resistances and can easily be optimized to further minimize their impacts.

To eliminate the effects of R_{jfet} on the internal resistance an alternative MOSFET structure was developed called the trench MOS or U-MOSFET [49]. In the trench MOS the gate extends from the N+ source region through the P-base region and ends in the drift region shown in Figure 3.24.

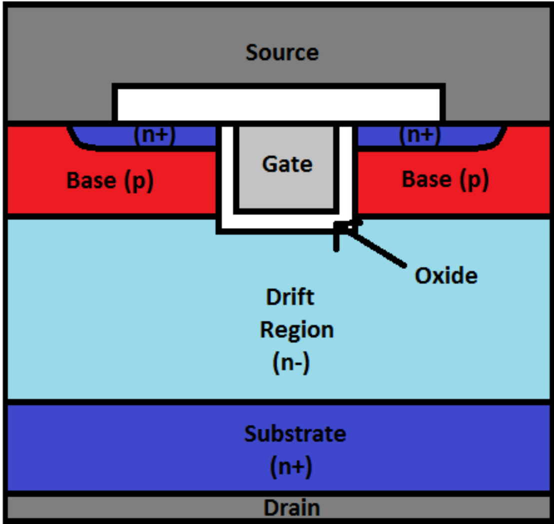


Figure 3.24: Trench MOSFET Configuration

With the trench MOSFET structure a vertical channel is formed and there is no R_{jfet} lowering the internal resistance. The major issue with using the trench MOSFET structure is that during the blocking mode of operation a high electric field is across the gate oxide due to the fact that the gate potential is a zero [49]. Use of the trench MOSFET is currently used in applications where the blocking voltage is 250 V or less.

The theoretical limit of the resistance of the drift region is related to the breakdown voltage required which in turn is related to the doping and width of the drift region. Development of a new

MOSFET structure has afforded the ability to go below the theoretical limit of the drift region resistance for vertical MOSFETs [51]. Called the superjunction MOSFET, it utilizes the compensation principle to drastically reduce the drift region resistance. In Figure 3.25 the superjunction MOSFET structure is similar to the VD-MOSFET with additional P-columns going through the drift layer [51].

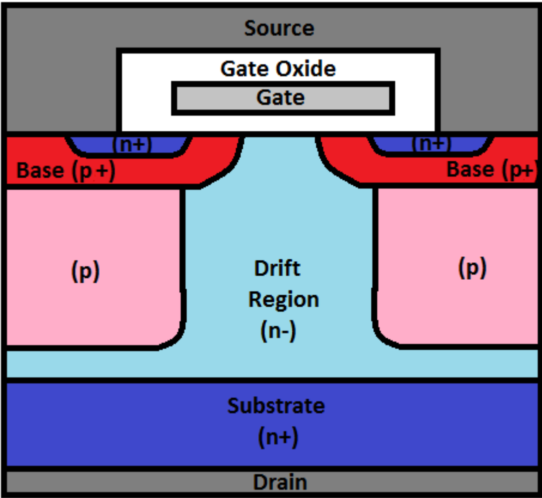


Figure 3.25: Superjunction MOSFET Configuration

Doping of the P-columns are set so that they are equal in doping to that of the drift region, this puts an equal number of donors and acceptors within lateral proximity of each other allowing compensation of both regions [51]. The end result is a low effective doping for the P-columns and drift region. Electric field distribution for the superjunction MOSFET is displayed in Figure 3.26.

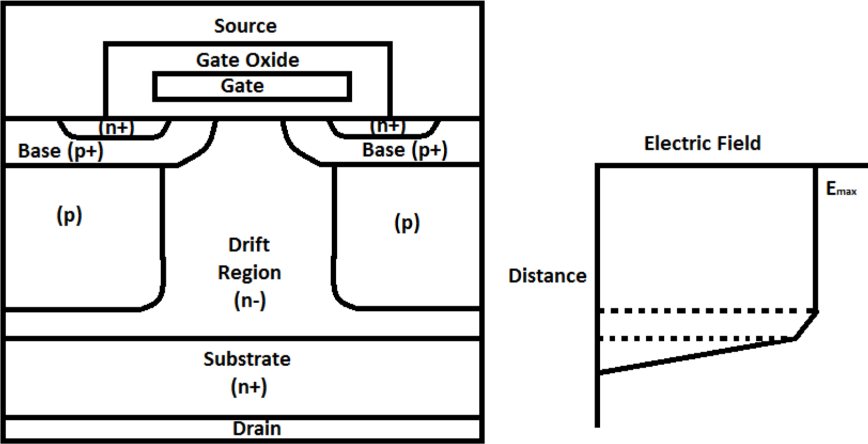


Figure 3.26: Electric Field Distribution of Superjunction MOSFET

For the rectangular field distribution the maximum voltage can be withstood at any thickness. This decouples the doping requirements for a specific blocking voltage [51]. Thickness of the drift region can be reduced and doping of the drift region can be increased as long as the P-column is also increased to compensate for the increased donors [51]. In the end R_{drift}, R_{jfet} and R_{ch} can be reduced to levels not thought possible for silicon based high voltage MOSFETs.

The biggest disadvantage of the superjunction MOSFET is the intrinsic body diode. Due to the high doping levels for the P-column and the drift region there is a very large amount of minority carriers in that region making the reverse recovery of the superjunction MOSFET long. As with VD-MOSFETs it is possible to use lifetime control to improve the reverse recovery characteristics of the body diode at the cost of higher internal resistances.

Switching characteristics of vertical MOSFETs is dependent on the parasitic capacitances across all three terminals of the device [51]. Equivalent circuit and structure with parasitic capacitances are in Figure 3.27.

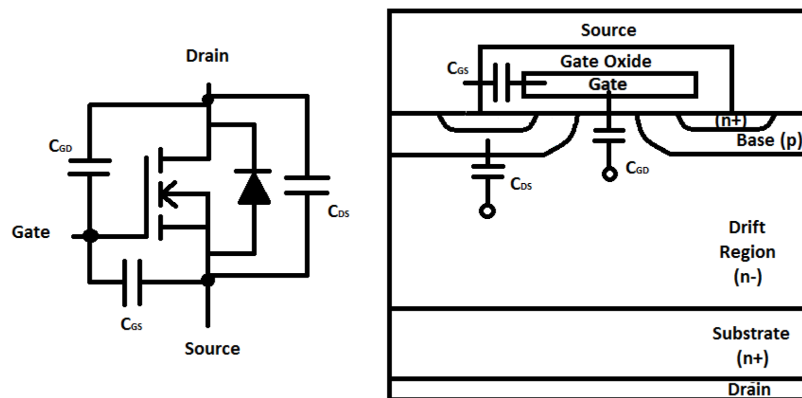


Figure 3.27: MOSFET Equivalent Circuit and Structure with Parasitic Capacitances

The turn on sequence for MOSFETs first has the voltage across the gate-source capacitance (C_{GS}) increasing linearly until the threshold voltage is reached at a time constant of the gate resistance and C_{GS} combined with the gate-drain capacitance (C_{GD}). Current through the drain of the MOSFET begins to flow with the gate voltage continuing to charge at the same rate. When the current through the drain reaches its peak value the voltage across the drain-source (V_{DS}) begins to decrease and the drain-source capacitance (C_{DS}) begins to discharge. Voltage at the gate no longer increases and remains constant while C_{GD} is being charged this region is referred to as the Miller plateau [51]. When the V_{DS} decreases to zero the Miller plateau region is passed and the gate voltage increases at a linear rate with a time constant of the gate resistor with the combined C_{GS} and C_{GD}. Switching power dissipation is the highest

after reaching the threshold voltage and during the Miller plateau region as a result of the drain current and voltage being very large [51]. MOSFET turn off sequence is opposite of the turn on sequence.

3.3.4 IGBT

Another class of voltage controlled active power switch is the IGBT. Before the creation of the IGBT there were several attempts to eliminate the complex driving systems required to run bipolar transistors by using a hybrid MOSFET-bipolar structure. The hybrid MOSFET-bipolar structure had many problems including poor switching performance and large die area. IGBTs have then surpassed bipolar transistors in medium and even high power ranges. A basic IGBT structure is shown in Figure 3.28.

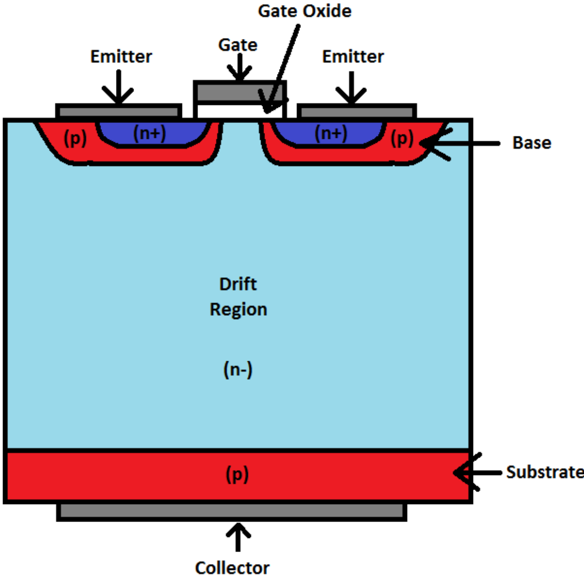


Figure 3.28: IGBT Structure

Comparing the IGBT structure with that of the MOSFET they are very similar with the only difference being that in the IGBT the substrate layer is made with P-doping while in the MOSFET the substrate layer is made with N+-doping. For all IGBT structures in order to conduct current in the reverse direction an additional freewheeling diode has to be parallel connected to the IGBT due to the fact that there is no intrinsic diode. Operation of the IGBT has it so that if there is a positive bias voltage across the collector-emitter connection without any gate bias voltage the device is in the blocking mode. When there is sufficient voltage applied to the gate to surpass the threshold voltage a N-channel is formed and electrons flow from the emitter to the collector [51]. Generation and removal of the channel follows

the same mechanism as that of the MOSFET. Creation of the newly formed channel causes holes to flow from the collector into the drift region and through the P-substrate of the emitter connection [51]. Since current flow is achieved through the movement of holes through the drift region this means that the IGBT is a minority carrier device. The drift region undergoes conductivity modulation similar to the P-I-N diode. An equivalent circuit for the IGBT is shown in Figure 3.29.

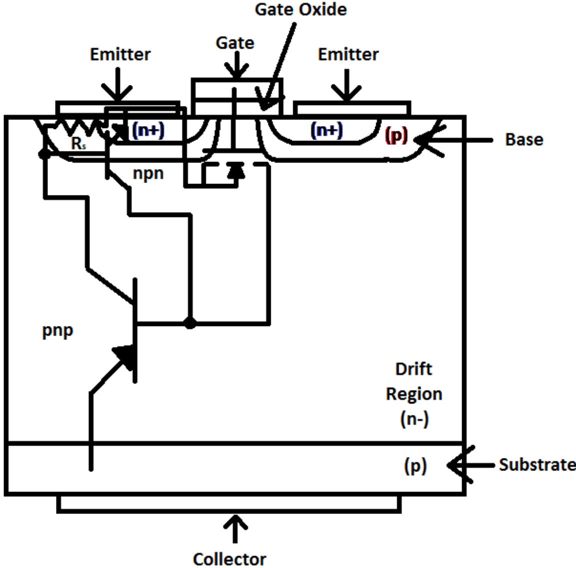


Figure 3.29: IGBT Structure with Equivalent Circuit

Since there is a PNPN structure within the device there is an addition parasitic NPN transistor with the metal contact at the emitter the NPN has its base shorted with a small resistance R_S [51]. At low currents the effects of the NPN transistor can be neglected, however at higher current there is a major issue called latch-up [51]. Latch-up is where the NPN transistor can be triggered into an on-state this causes the current to increase continuously with the added gain from the PNP transistor and the MOS gate cannot turn off the device resulting in its destruction [51].

One method to deal with the effects of latch-up is to add an additional N- buffer layer between the drift layer and collector P substrate. The doping of the drift layer is increased and the doping of the collector P substrate is heavily doped [51]. During blocking mode the electric field is partially distributed in the N- buffer region causing the electric field to have a trapezoidal shape. This IGBT configuration is called the punch-through IGBT (PT-IGBT) shown in Figure 3.30 [51].

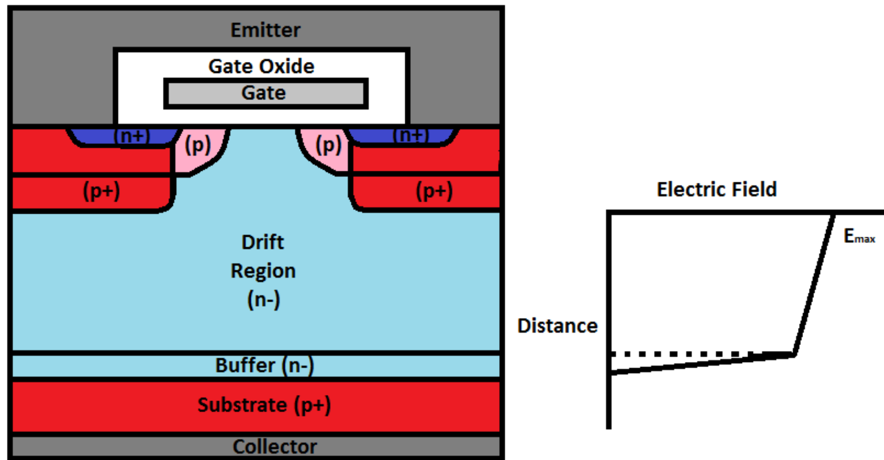


Figure 3.30: PT-IGBT Configuration and Electric Field Distribution

Another IGBT configuration to address the latch-up issue is the non-punch through IGBT (NPT-IGBT). The main difference from the traditional IGBT structure and the NPT-IGBT is the increased thickness of the drift region and the added P+ region overlapping the emitter. Increased drift region thickness allows the entire electric field to be contained within the drift region itself resulting in an electric field with a triangular shape. Figure 3.31 shows the NPT-IGBT configuration.

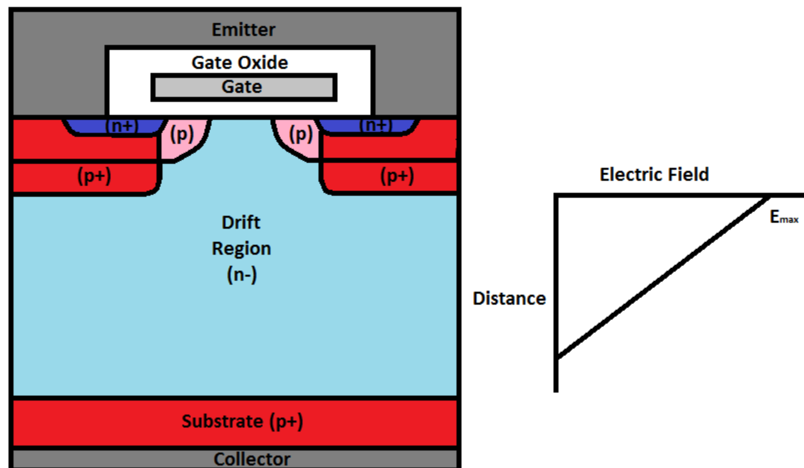


Figure 3.31: NPT-IGBT Configuration and Electric Field Distribution

Characteristic comparisons between the two different types of IGBTs have that similar to the P-I-N diode the conduction loss of the PT-IGBT is lower compared to the NPT-IGBT due to the thinner drift region and high conductivity modulation [52]. As the temperature increases the conduction loss of the PT-IGBT decreases due to the increased number of carriers, for the NPT-IGBT increased temperature causes the mobility of the carriers decreases causing the conduction loss to increase [51]. This characteristic for the NPT-IGBT can be beneficial in that if paralleling multiple IGBTs and the current is not balanced in each device then the conduction drop increases decreasing the current in that device causing both devices to share current equally [51].

As both the NPT-IGBT and PT-IGBT are planar structures they have a R_{jfet} region that is synonymous with conventional planar MOSFETs. Similar to the trench MOSFET a trench structure can be adopted for IGBTs to eliminate R_{jfet} and reduce the conduction loss. The trench IGBT structure is commonly used with the PT-IGBT structure to further enhance its lower forward conduction loss. A trench PT-IGBT is shown in Figure 3.32 [53].

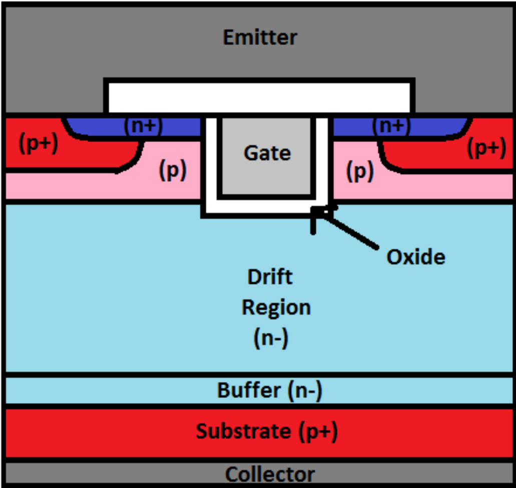


Figure 3.32: Trench PT-IGBT Configuration

The main disadvantage of the trench structure for IGBTs is the same as the MOSFET where the gate oxide formation can enhance the electric field at the corners. This problem can be solved by rounding the corners of the trench during fabrication [53].

Switching behavior of IGBTs is very similar to that of MOSFETs for the turn on mode of operation. The major difference between IGBTs and MOSFETs for switching characteristics is the turn off mode of operation. During turn off in the IGBT there is an additional tail current at the end of the

turn off period. The tail current is where the turn off current goes to a certain value and slowly decays to zero. Minority carrier charge in the drift region is what determines the time that it takes for the tail current to go to zero [51]. As the tail current is decreasing the voltage across the device is high, generating switching transition losses. Comparing the NPT-IGBT tail current with the PT-IGBT, the NPT-IGBT has a longer current tail period but the magnitude of the tail current is less [52]. Doping, lifetime control and further device structure optimizations can be made to further decrease the tail current and its effects [53].

3.3.5 Wideband-gap Semiconductor Materials

The previously discussed semiconductor structures have focused on their implementation using silicon as the semiconductor material. With the pursuit of smaller power conversion systems the focus has been on increasing the switching frequency to reduce passive component size while maintaining the high efficiency. Use of wideband-gap semiconductor material is providing a potential solution to improving the efficiency of the high frequency power converters. Prominent wideband-gap materials used in power conversion are compound semiconductors silicon carbide (SiC) and gallium nitride (GaN). Comparisons of the major material characteristics for different semiconductor materials are shown in Table 3.8.

Material Property	Bandgap (eV)	Breakdown Field (MV/cm)	Electron Mobility (cm^2/Vs)	Hole Mobility (cm^2/Vs)	Saturation Velocity (10^6 cm/s)	Thermal Conductivity (W/cm^2K)	Thermal Expansion (ppm/K)
Si	1.12	0.3	1450	450	10	1.5	2.6
SiC (4H)	3.25	3.0	900	125	22	5	5.12
GaN	3.44	3.0	1100	30	25	1.3	5.4

Table 3.8: Semiconductor Material Characteristics [54], [55]

A wider bandgap means that the material can safely operate at elevated electric fields [49]. Higher breakdown field means that the thickness of the drift region can be reduced to support the same electric field for a material with a lower breakdown field resulting in lower on-resistance [49]. Electron mobility is related to the conductivity of the material, a higher mobility means a lower resistivity [49]. High electron mobility and saturation velocity affect the switching performance of the device for majority carrier devices allowing for higher switching speeds.

A number of wideband-gap semiconductor devices are commercially available using SiC and GaN. One of the earliest commercially available wideband-gap devices was a high voltage Schottky diode using SiC [56]. Since SiC has a higher critical electric field compared with silicon the thickness of

the drift region can be substantially reduced allowing the Schottky structure to block voltages higher than 200 V. The elimination of reverse recovery in diodes for high voltage applications affords the ability to run higher switching frequencies due to the reduced switching losses. A major drawback to the SiC Schottky diode is that the semiconductor-metal junction has a larger barrier height compared with silicon P-I-N diodes increasing the on-state conduction losses [57]. Another disadvantage is that the temperature coefficient for SiC devices is positive causing the current carrying capability of the device to decrease with increased temperatures [57]. Another device structure that has been successfully created using SiC is the planar VD-MOSFET [58]. Using SiC for vertical MOSFETs increases the number of high power applications that were traditionally targeted more for IGBTs and other bipolar devices. SiC MOSFETs can now be used in applications from 1200 V and higher. The biggest concern for SiC VD-MOSFETs is being able to produce a reliable device in sufficient quantities [58]. Refinements to fabrication processes have improved the performance and quantities of SiC devices reducing their cost [58].

Progress on GaN devices has not reached the level of maturity that SiC has; however, current implementations have shown potential for major improvements in future wideband-gap semiconductor devices [58]. Initial commercial GaN designs include a lateral based MOSFET configuration referred to as a high electron mobility transistor (HEMT) created by the company Efficient Power Conversion (EPC) shown in Figure 3.33.

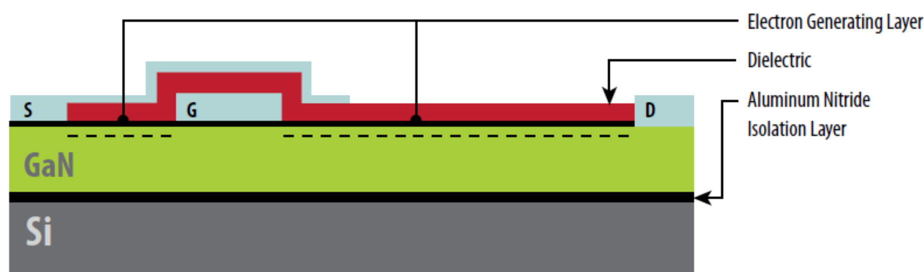


Figure 3.33: EPC GaN HEMT Structure. Figure 1. S. Colino and R. Beach, Appl. Note AN002, "Fundamental of Gallium Nitride Power Transistors," Efficient Power Conversion, 2011. Used under fair use, 2014.

EPC's device is grown on a silicon substrate then an aluminum-nitride (AlN) buffer layer is added on top of the silicon [59]. After the AlN layer, a lightly doped GaN layer is grown that will later serve as the conduction channel. The electron generating layer is aluminum –gallium-nitride (ALGaN) , which creates a layer of excess electrons in the GaN layer forming a channel [59]. For HEMTs from other companies the device is normally-on, with the EPC structure there is an additional process that depletes the GaN region under the gate making the device normally-off. Enhancing the region under the gate requires

adding a positive voltage, allowing electrons to flow between source and drain connections. For reverse conduction there is no built in parasitic diode, instead when gate-source voltage is zero a positive bias is generated between the gate and drift region causing the formation of a channel under the gate and allowing current to flow [59]. Major advantages of GaN include a low capacitances due to the lateral device structure allowing high switching frequencies and absence of minority carriers in the reverse conduction mode eliminating reverse recovery [59]. Due to the high switching performance of the GaN HEMT circuit parasitic elements need to be minimized for gate drive and loop inductance. Not accounting for circuit parasitics can generate large voltage and current oscillations during the switching transitions, destroying the device. Drawbacks to the EPC HEMT is its inability to sustain a large electric field laterally limiting the device operating voltage to 300 V, additional processing methods have to be introduced in order to use silicon as the substrate material due to the different thermal coefficients for GaN and silicon [54], [55]. Quality of the GaN material is deficient compared with the other semiconductor materials, however with refinements in processing it will improve over time [58].

For higher voltage applications the use of GaN has been approached using the normally-on HEMT configuration. The normally-on HEMT configuration allows the device to sustain a higher electric field compared with EPC due to the fact that the entire electric field is across the drain-source region and not just the depleted gate region. To get around the design challenges of incorporating a normally-on device the company Transphorm has incorporated the high voltage HEMT in a cascode configuration with a low voltage silicon MOSFET shown in Figure 3.34 [60].

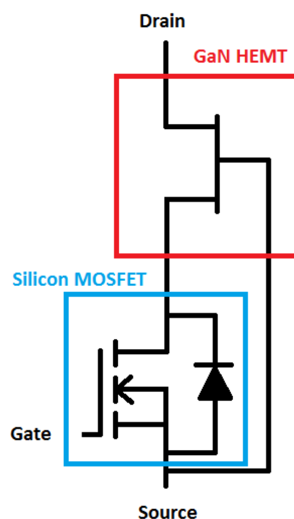


Figure 3.34: Transphorm High Voltage GaN Cascode Configuration

For the cascade configuration when there is no gate voltage on the MOSFET the gate of the HEMT is at the same potential as the source of the MOSFET and the source of the HEMT is at a different potential referenced to its own gate [61]. This causes the channel of the HEMT to become depleted and the entire electric field is across the HEMT. As a result the voltage requirement for the silicon MOSFET is very low [61]. During forward conduction of the device the MOSFET gate is positive pulling the gate and source of the HEMT to the same potential and allowing the current to flow through the channel of both the MOSFET and HEMT [61]. Similar to the EPC HEMT the switching performance of the high voltage HEMT can be very high along with reduced reverse recovery charge. A big drawback to the cascode configuration is that the total device performance is dependent on the low voltage silicon MOSFET, which adds resistance and reverse recovery loss to the device [58]. If the MOSFET has a large leakage current there is additional power dissipation when the device is off. Packaging is another issue with the inter-connects to the two devices adding parasitic capacitances and inductances, which affect the switching performance. As with the EPC GaN material Transphorm's GaN material is not as mature as its silicon counterparts but the use of the cascode structure has benefits of easier implementation compared with EPC [58].

4 Parameter Design and Experimental Results

In order to perform an accurate comparison analysis of the different types of inverters; several inverter topologies were designed, constructed and tested. The topologies that were tested include full bridge inverter using asymmetrical unipolar modulation, unipolar dual buck, single buck inverter and SHREC inverter. Testing specifications were set to follow a standard PV microinverter system setup with the system parameters listed in Table 4.1.

Parameter	Value
Input Voltage	380 V DC
Output Voltage	240 V AC
Output Frequency	60 Hz
Switching Frequency	30 kHz
Nominal Output Power	250 W
Nominal Output Current	1.04 A AC
Input Capacitance	60 uF

Table 4.1: Testing Specifications

The switching frequency is set to 30 kHz in order to provide an adequate balance between semiconductor switching losses and output filter size. Performance comparison of the different inverter topologies is carried out using a weighted efficiency average created by the CEC that factors the system efficiencies at different load conditions using the equation:

$$n_{CEC} = 0.04n_{10\%} + 0.05n_{20\%} + 0.12n_{30\%} + 0.21n_{50\%} + 0.53n_{75\%} + 0.05n_{100\%}$$ [62]

4.1 Test Setup

For all inverter topologies the testing configuration will be the same. The test setup is shown in Figure 80. Input power to the inverter was supplied using a single Power Ten power supply, 600 V P63C-60011. Output of the inverter was connected to several 225 W power resistors for stand-alone testing.

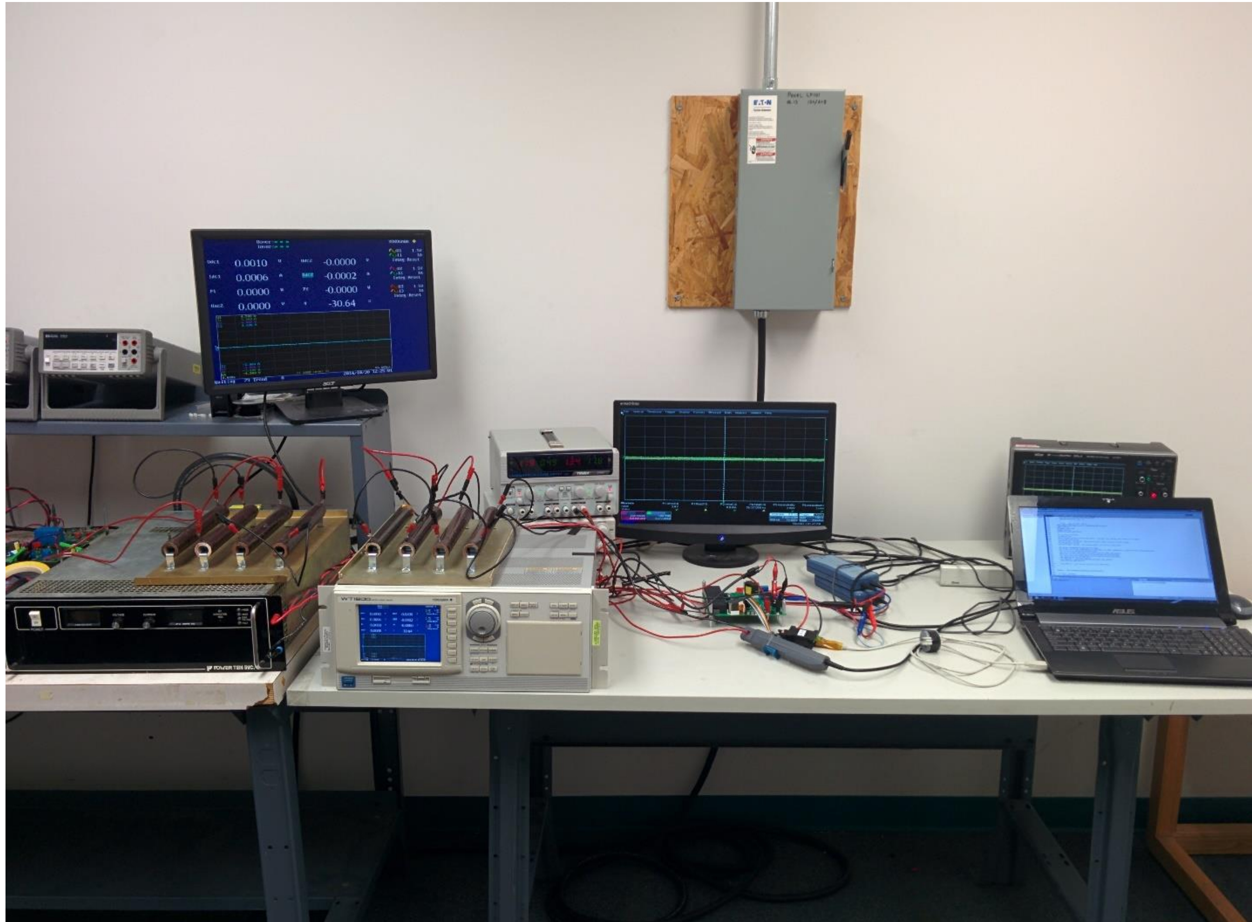


Figure 4.1: Experimental Test Configuration

Since the inverter generates a double line ripple on the input voltage and current it is not possible to accurately measure the input power of the inverter using digital multi-meters. Instead a digital power meter, the Yokogawa WT1600 is used due to the fact that it continuously integrate the instantaneous power giving accurate experimental measurements. Waveforms of the inverter output are provided with a Teledyne LeCroy 104MXs-B oscilloscope. Control of the inverter is carried out using a Texas Instrument's TMS320F28026 DSP integrated into the inverter PCB. DSP and other auxiliary functions are powered using a Tenma 72-6905 30 V power supply.

4.2 Output Filter

Since all inverters are operated at the same switching frequency the values of the output filter are going to remain the same with only the construction of the inductor varying from design to design. Using the parameters set in Table 4.1 the value for the output inductor can be calculated with the only

unknown value being the ripple current magnitude. Having a small current ripple reduces the core loss of the inductor but causes the value of the inductor to be very large. A large inductor increases the cost and size of the inverter. Having too low of an inductance value increases the current ripple causing higher conduction losses of the semiconductor devices, increased core losses in the output inductor along with higher resistive losses and increased harmonic distortion of the output. A peak to peak ripple of 36% gives an output inductance of 6 mH. Determination of the output capacitance can be obtained using the output inductance value calculated. Using the value for the output inductor and setting the cutoff frequency of the second order low pass filter to one tenth of the switching frequency the output capacitance has to be approximately 0.47 uF. A 0.47 uF film capacitor with a rating of 275 V AC and safety rating of X2 was selected.

Parameter	Value
Output Filter Inductor	6 mH
Output Filter Capacitor	0.47 uF

Table 4.2: Output Filter Component Values

4.3 Asymmetrical Unipolar Full Bridge Inverter Testing

The full bridge inverter provides the most basic structure of all the inverter topologies, and is the baseline metric for comparisons of all other inverters. Each modulation method for the full bridge inverter has its advantages and disadvantages. In order to achieve high efficiency it is necessary to utilize a unipolar modulation scheme; however, all full bridge unipolar modulation schemes have poor CM noise performance compared to bipolar modulation. Within the different unipolar modulation schemes there are different levels of severity for CM noise. Asymmetrical unipolar modulation was selected as the modulation scheme for testing the full bridge inverter because it has the least CM noise of the full bridge unipolar modulation techniques and if the primary input stage of the microinverter is isolated the effects of the CM can be mitigated.

4.3.1 Magnetic Considerations

Another advantage of the asymmetrical unipolar full bridge is the fact there is only one high frequency switch node requiring the use of only one inductor. For other modulation methods both switch leg middle points operate at high frequency, requiring the inductor to be split between the two output nodes. A single magnetic can be used to achieve inductances on both legs via the use of a coupled winding inductor. Coupling between the two inductors must be very tight in order to minimize

circulating energy between both windings. Tight coupling can be achieved using a bifilar winding pattern shown in Figure 4.2.

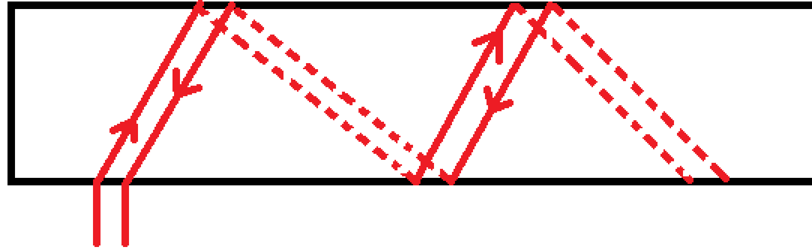


Figure 4.2: Bifilar Winding Structure

Using coupled inductors reduces the number of inductors required at the cost of added manufacturing complexity.

Since asymmetrical unipolar modulation requires one inductor so there is no need for any complex winding structure. To decrease the cost of the inverter and maintain the efficiency ferrite material from Ferroxcube 3C95 was used. Characteristics of 3C95 include low core loss, no increase in core loss over a wide temperature range and good performance for converters with a switching frequency up to 500 kHz. The core shape used to make the inductor is the RM12/I, which has a large window area allowing enough turns to reach the desired inductance of 6 mH and low volume keeping the size of the inverter output filter to a minimum. The inductor winding consisted of 22 AWG solid gauge wire allowing higher utilization of the window area and keeping the materials cost of the inductor low.

4.3.2 Semiconductor Considerations

For the full bridge inverter correct selection of semiconductor components are one of the major factors in achieving high efficiency. The biggest drawback to the full bridge inverter is that when using MOSFETs as the main switch the body diodes have to be utilized for the freewheeling conduction period. Since the body diode switching characteristics for high voltage devices are very poor it is very difficult to achieve high efficiency at high switching speeds. Since the conduction characteristics of high voltage MOSFETs are very low it is not possible to parallel high voltage low reverse recovery diodes due to the negative temperature coefficient of the body diode.

Options for semiconductor devices with acceptable body diode performance include superjunction MOSFETs with lifetime enhancement to improve body diode switching performance

(Infineon CFD2), SiC MOSFETs, GaN high voltage HEMT and IGBT with parallel SiC Schottky diode. Even with the lifetime enhancements the body diode reverse recovery for superjunction MOSFETs is still a major source of switching loss. Wideband devices using GaN and SiC promise higher efficiencies due to their improved switching characteristics and low reverse recovery. The major issue with wideband devices are the higher costs compared with silicon based semiconductors. IGBTs are often precluded from lower power applications due to their higher conductive losses compared with MOSFETs and the perception that they cannot operate at higher frequencies due to the switching losses caused by their tail current. With the development of Infineon's new Trenchstop 5 IGBT structure they have managed to use the trench configuration with high doping in the drift region to reduce conduction losses, while using a graded doping profile to achieve low switching losses and reduce tail currents. Not only does the Trenchstop IGBT have low switching losses its ability to parallel a SiC Schottky diode allows minimal reverse recovery current. Due to the lack of switching performance characterization in semiconductor datasheets, the best way to compare device performance is to run the inverter at the same switching frequency using each device.

For the high frequency switching device the major source of concern in the design is the reduction of switching loss, this is because the current that flows through the device is minimal and conduction losses play a lesser role in the system losses. The low frequency switch leg transitions at low frequency when there is no voltage and no current so the only concern for the low frequency switch is its conduction loss and size. The list of semiconductor devices tested with the asymmetrical unipolar full bridge are shown in Table 4.3.

Test Case	High Frequency Device	Low Frequency Device
Silicon Superjunction MOSFET	IPB65R310CFD	IPB65R045C7ATMA1
High Voltage GaN HEMT	TPH3002PD	IPB65R045C7ATMA1
SiC MOSFET	SCT2120AFC	IPB65R045C7ATMA1
Trenchstop 5 IGBT with parallel SiC Schottky Diode	IGP20N65F5 C3D03060E (diode)	IPB65R045C7ATMA1

Table 4.3: Semiconductor Devices Tested with Full Bridge Inverter

The low frequency device used in all test cases was Infineon's CoolMOS C7 45 mΩ 650 V superjunction MOSFET IPB65R045C7ATMA in TO-263 (D^2PAK), due to the fact that it is the lowest conduction loss device for that specific package size. For the high frequency test case using the superjunction MOSFET, Infineon's CoolMOS CFD2 310 mΩ 650 V IPB65R310CFD in TO-263 offers the best combination of conduction loss with reduced reverse recovery due to lifetime control. Transphorm's cascode GaN HEMT 290 mΩ 600V TPH3002PD in TO-220 (compatible with TO-263) offers

the best switching performance among Transphorm's product line for this power level. The first commercially available 650 V SiC MOSFET is Rohm's SiC VD-MOSFET 190 mΩ 650V SCT2120AFC in TO-220, offering excellent reverse recovery characteristics and low turn off switching losses. The last test case is using Infineon's Trenchstop 5 IGBT 20 A 650V IGP20N65F5 in TO-220, without built in parallel diode, the switching characteristics match or exceed those of the superjunction MOSFETs. Paralleling the IGBT with Cree's SiC Schottky diode 3A 600V C3D03060E in TO-252 (DPAK) eliminates reverse recovery current and improves switching performance of the IGBT.

4.3.3 Efficiency Results

Efficiency for each test case was carried using the same PCB to ensure a more accurate comparison of the different semiconductor devices. Figure 82 shows the test PCB used for all cases.

Figure 4.3: Full Bridge Inverter PCB

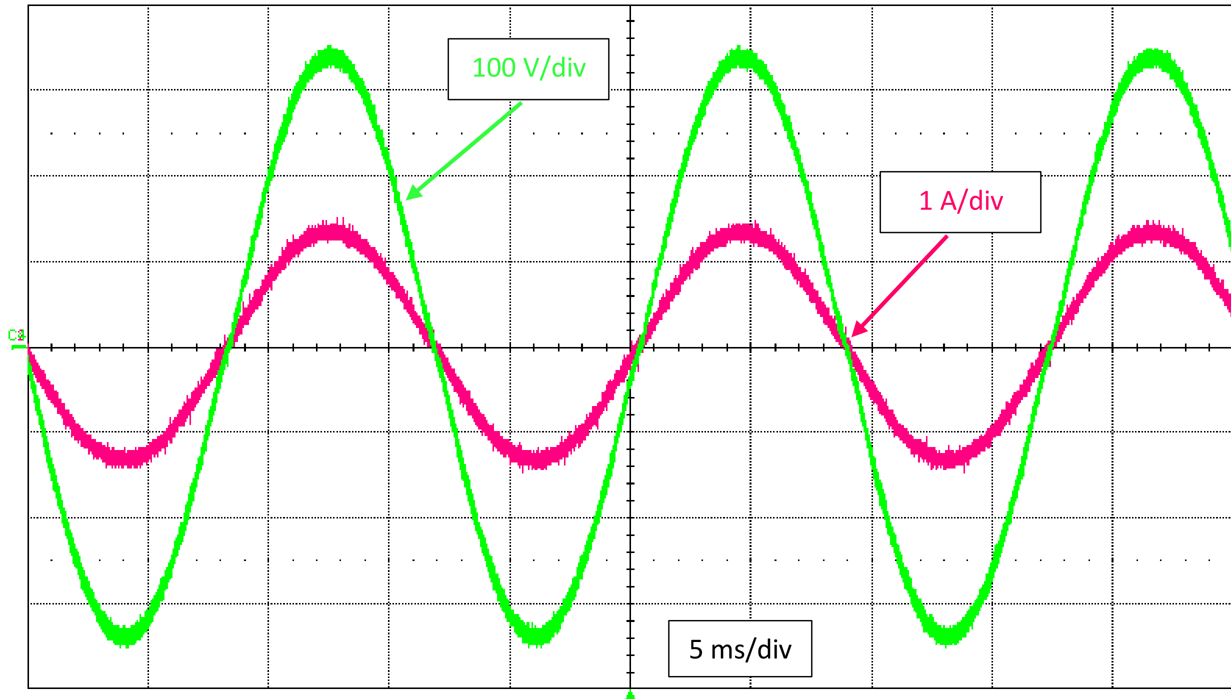


Figure 4.4: Full Bridge Inverter Output Voltage and Current at 100% Load

Using the Yokogawa WT1600 digital power meter the efficiency was measured for the asymmetrical unipolar full bridge inverter over the entire CEC range.

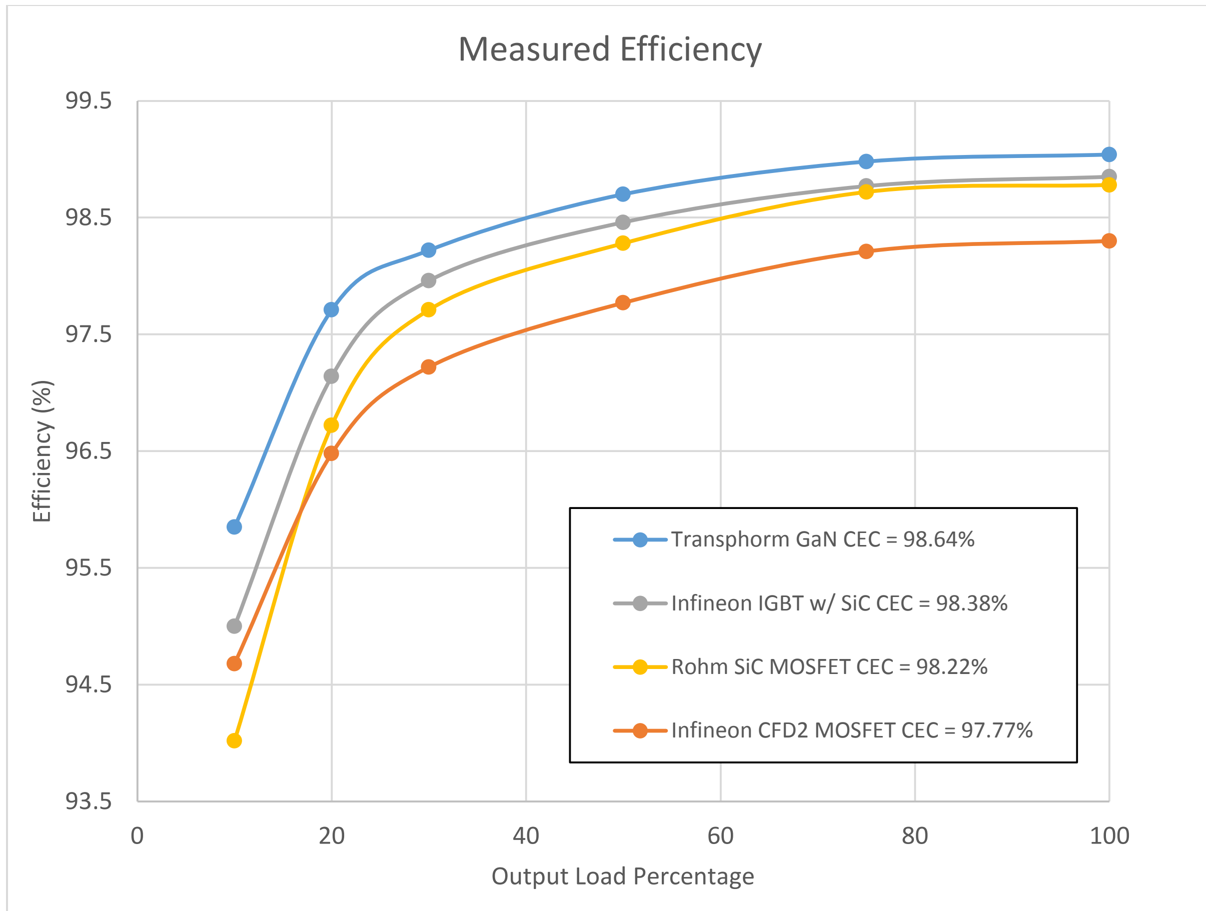


Figure 4.5: Full Bridge Inverter Efficiency for Different Semiconductors

From the results the best performance is achieved using the Transphorm GaN HEMT with a peak efficiency of 99.04% and CEC efficiency of 98.64%. The biggest surprise is the performance of the Trenchstop 5 IGBT with SiC diode with a peak efficiency of 98.85% and CEC efficiency of 98.38%. The switching performance of the Trenchstop 5 overcomes the higher conduction losses and outperforms the SiC MOSFET and CFD2 superjunction MOSFET.

4.3.4 Common Mode Noise Results

Using an isolated differential probe the CM voltage was measured from the output to ground shown in Figure 4.6. The CM voltage waveform matches the waveform from simulation of the asymmetrical unipolar full bridge VSI.

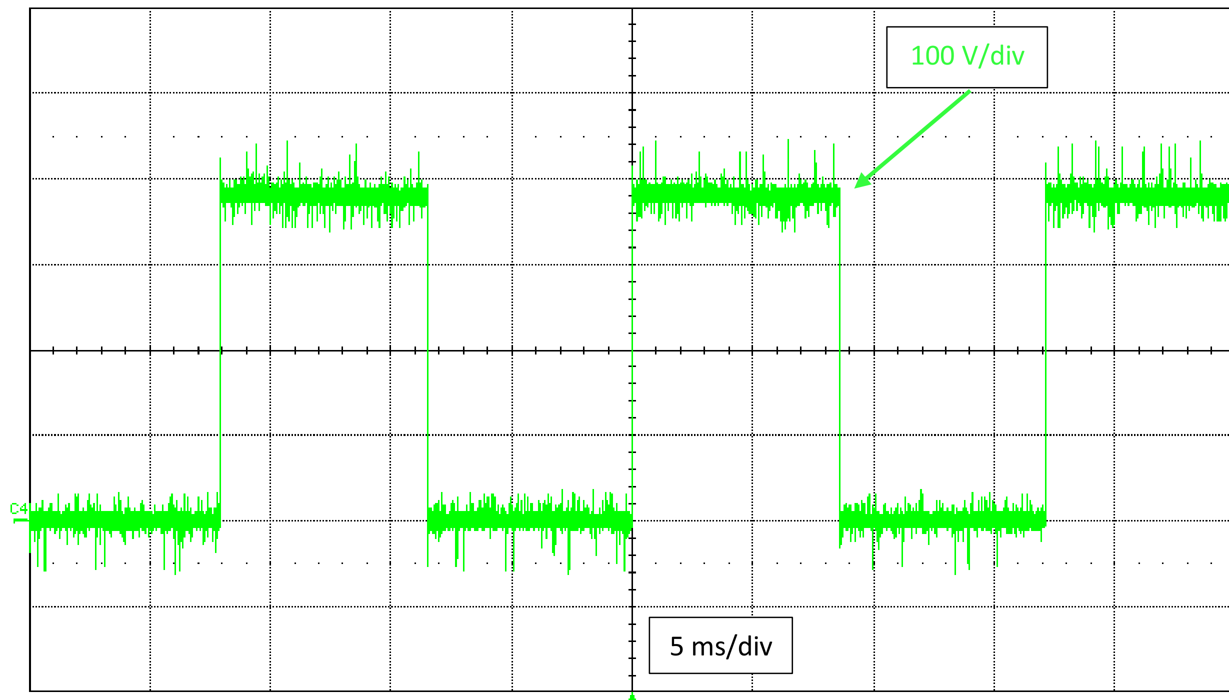


Figure 4.6: Asymmetrical Unipolar Full Bridge Common Mode Voltage

4.4 Unipolar Dual Buck Inverter Testing

The unipolar dual buck topology is another four active switch inverter like the full bridge, however, the topology requires the use of two additional diodes and one additional inductor to operate during the freewheeling period.

4.4.1 Magnetic Considerations

Magnetic core shape, material and wire remain the same as the full bridge inverter's design with the key difference being that the topology requires two separate inductors to operate. Current during the positive line cycle goes through one inductor and during the negative line cycle goes through the other inductor. Since the current going through both inductors is not the same it is not possible to couple the inductors to the same magnetic core. Even though the number of magnetics have increased the conduction and core loss in the magnetics are equivalently the same as one inductor due to the fact that there is no current flow during half the line cycle in one of the magnetics at a given time. This advantageous in dealing with the increase in resistance of the wire due to the effects of heating, as the current is distributed between to separate magnetics. Inclusion of another magnetic severely increases the cost of the system.

4.4.2 Semiconductor Considerations

Selection of semiconductor components for the unipolar dual buck inverter are not as constrained as selection for the full bridge inverter. For the full bridge inverter the high frequency switches had to have a body diode with good reverse recovery characteristics in order to achieve high efficiency. With the unipolar dual buck inverter the high frequency devices do not conduct through the body diode of the active switches allowing the use of superjunction MOSFETs that have poor body diode switching performance. The key design issue for this inverter is the use of low reverse recovery diodes for the freewheeling buck diodes. Use of SiC Schottky diodes can guarantee a reduction of switching loss at the penalty of higher cost and higher conduction losses. The low frequency switches should use devices with a low conduction loss since they transition at zero voltage and zero current periods.

For selection of the high frequency switches it should be a superjunction MOSFET with a low output capacitance and reasonable on resistance. Infineon's CoolMOS C7 225 mΩ 650 V superjunction MOSFET IPB65R225C7ATMA in TO-263 (D^2PAK), is a good device due to the low output capacitance and good switching characteristics. Active low frequency switches should be the same as the full bridge inverter low frequency switches, Infineon's CoolMOS C7 45 mΩ 650 V superjunction MOSFET IPB65R045C7ATMA in TO-263. Cree's SiC Schottky diode 3A 600V C3D03060E in TO-252 was selected as the freewheeling diode due to its low capacitance and negligible reverse recovery charge.

4.4.3 Efficiency Results

Efficiency testing of the unipolar dual buck inverter was carried using a modified PCB from the SHREC inverter shown in Figure 4.7.

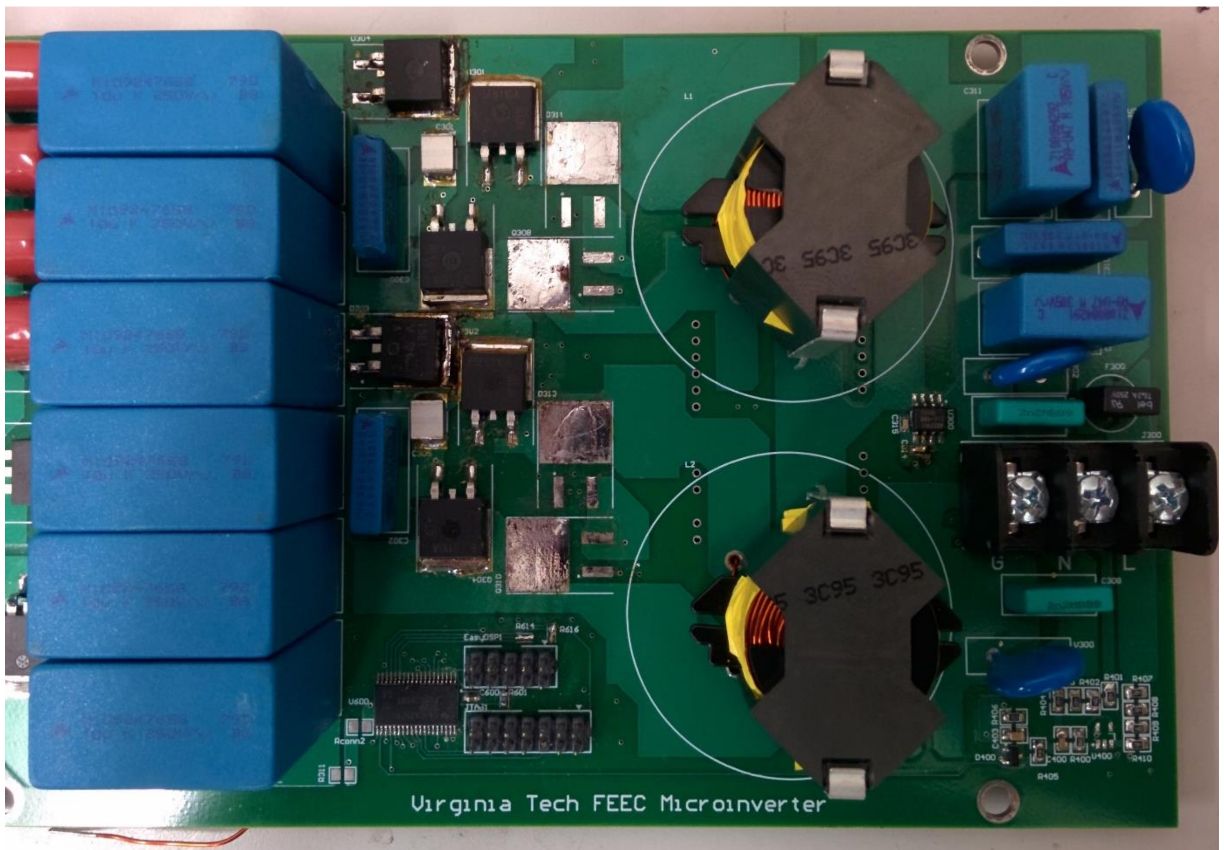


Figure 4.7: Unipolar Dual Buck Inverter Test PCB

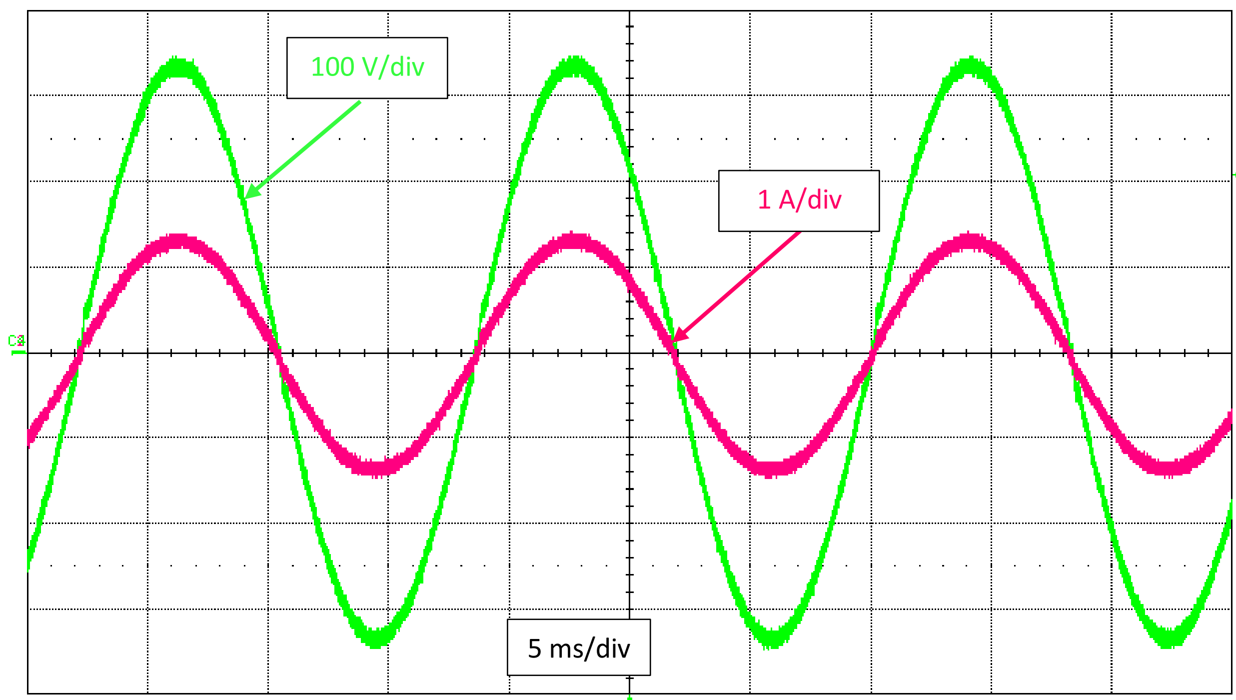


Figure 4.8: Unipolar Dual Buck Inverter Output Voltage and Current at 100% Load

The efficiency of the unipolar dual buck over the entire CEC efficiency range is shown below in Figure 4.9.

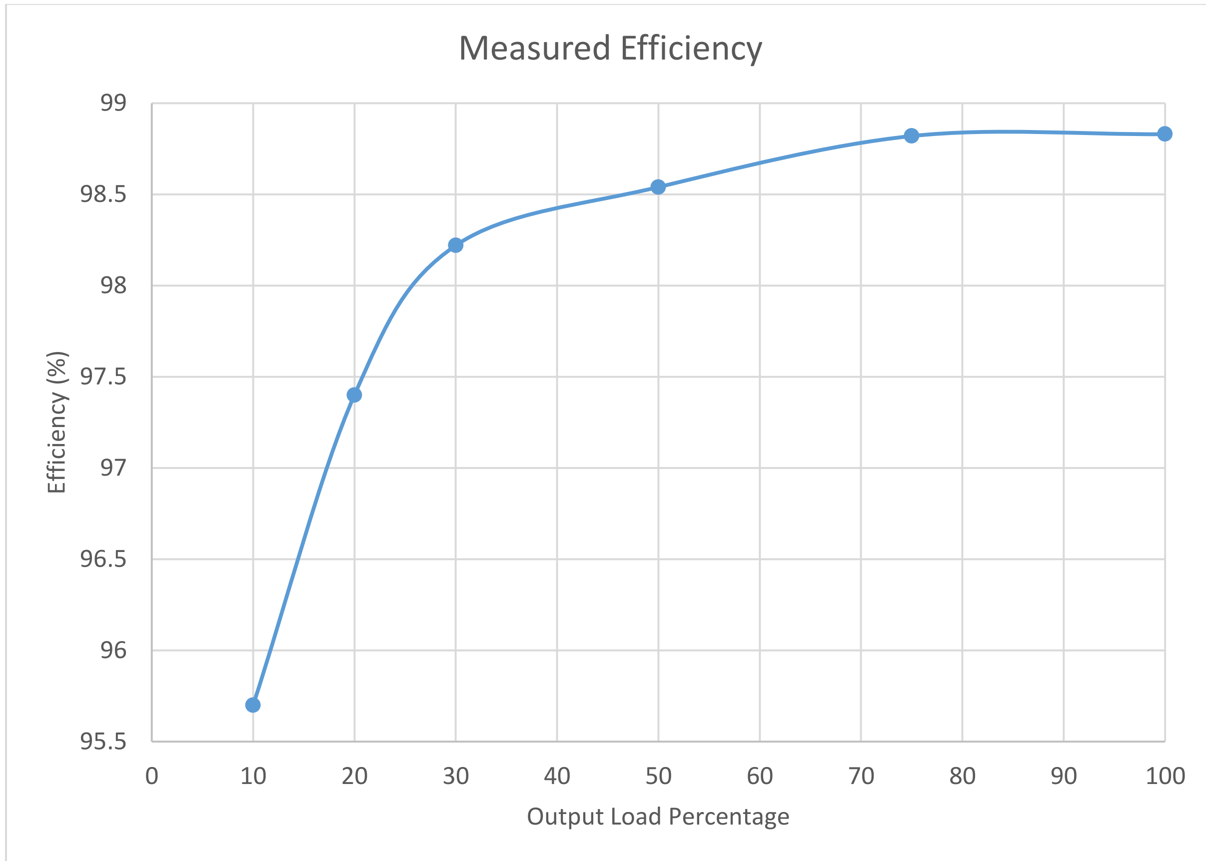


Figure 4.9: Unipolar Dual Buck Inverter Efficiency

Peak efficiency of the unipolar dual buck inverter is 98.83% and the CEC efficiency is 98.49%. Compared with the full bridge inverter the unipolar dual buck offers better performance with all test cases except for the case using the Transphorm GaN.

4.4.4 Common Mode Noise Results

Using an isolated differential probe the CM voltage was measured from the output to ground shown in Figure 4.10. The CM voltage waveform of the unipolar dual buck matches the simulation results.

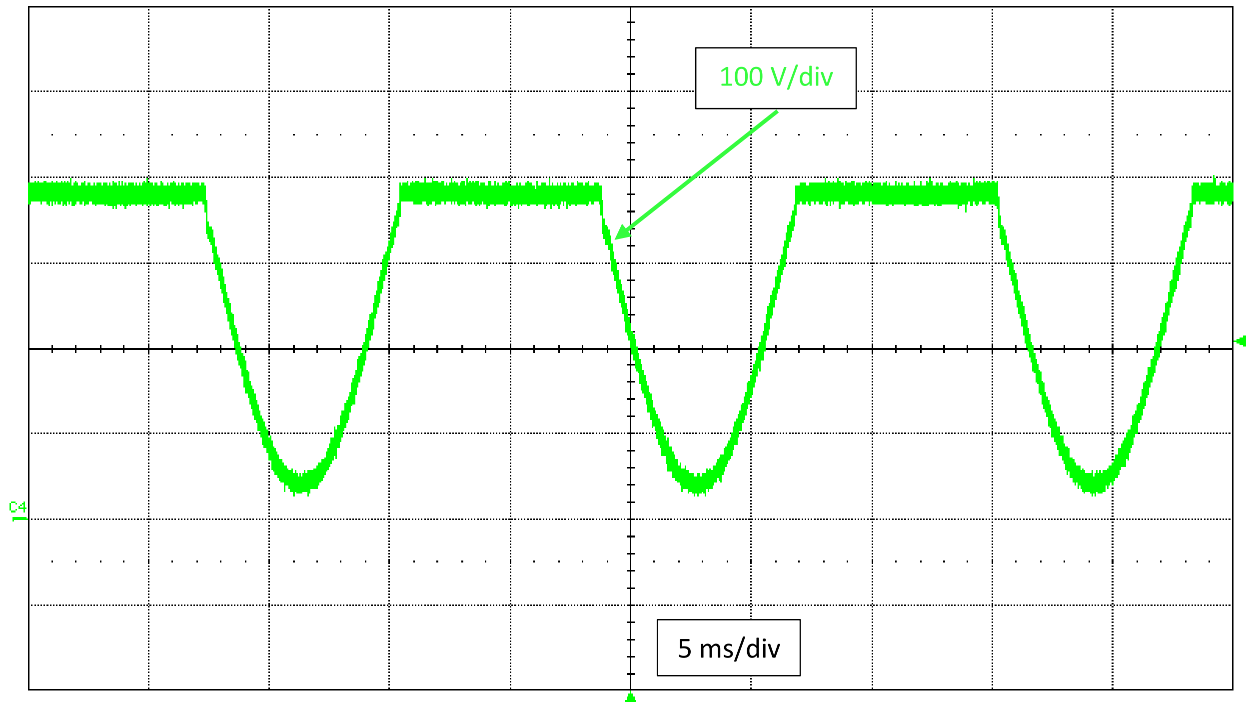


Figure 4.10: Unipolar Dual Buck Common Mode Voltage

4.5 Single Buck Inverter Testing

For the single buck inverter there are advantages to the dual buck topology and full bridge inverter. There is a high frequency buck stage, a single inductor and a full bridge unfolder used to change polarity of the output.

4.5.1 Magnetic Considerations

Magnetic core shape, material and wire remain the same as the full bridge inverter's design with the same number of inductors required. This offers an advantage over the unipolar dual buck in terms of cost reduction.

4.5.2 Semiconductor Considerations

The semiconductor selection for the single buck inverter has the same characteristics as the unipolar dual buck inverter with the ability to use superjunction MOSFETs when combined with SiC Schottky diodes offers good switching performance. For the full bridge inverter and unipolar dual buck output voltage polarity selection is carried out with one device per line cycle. With the single buck a low frequency full bridge polarity selector is required doubling the conduction losses for the low frequency

devices. Using the latest low on resistance superjunction MOSFETs the effects of the additional resistive loss are not as noticeable.

For selection of the high frequency switches it should be a superjunction MOSFET with a low output capacitance and reasonable on resistance. Infineon's CoolMOS C7 225 mΩ 650 V superjunction MOSFET IPB65R225C7ATMA in TO-263 (D^2PAK), is a good device due to the low output capacitance and good switching characteristics. In addition to the superjunction MOSFET an additional comparison to Transphorm's cascode GaN HEMT 290 mΩ 600V TPH3002PD in TO-220 was carried out. The low frequency full bridge uses, Infineon's CoolMOS C7 45 mΩ 650 V superjunction MOSFET IPB65R045C7ATMA in TO-263. Cree's SiC Schottky diode 3A 600V C3D03060E in TO-252 was selected as the freewheeling diode due to its low capacitance and negligible reverse recovery charge.

4.5.3 Efficiency Results

Efficiency for both test cases was carried using the same PCB to ensure a more accurate comparison of the different semiconductor devices. Figure 4.11 shows the test PCB used for both cases.

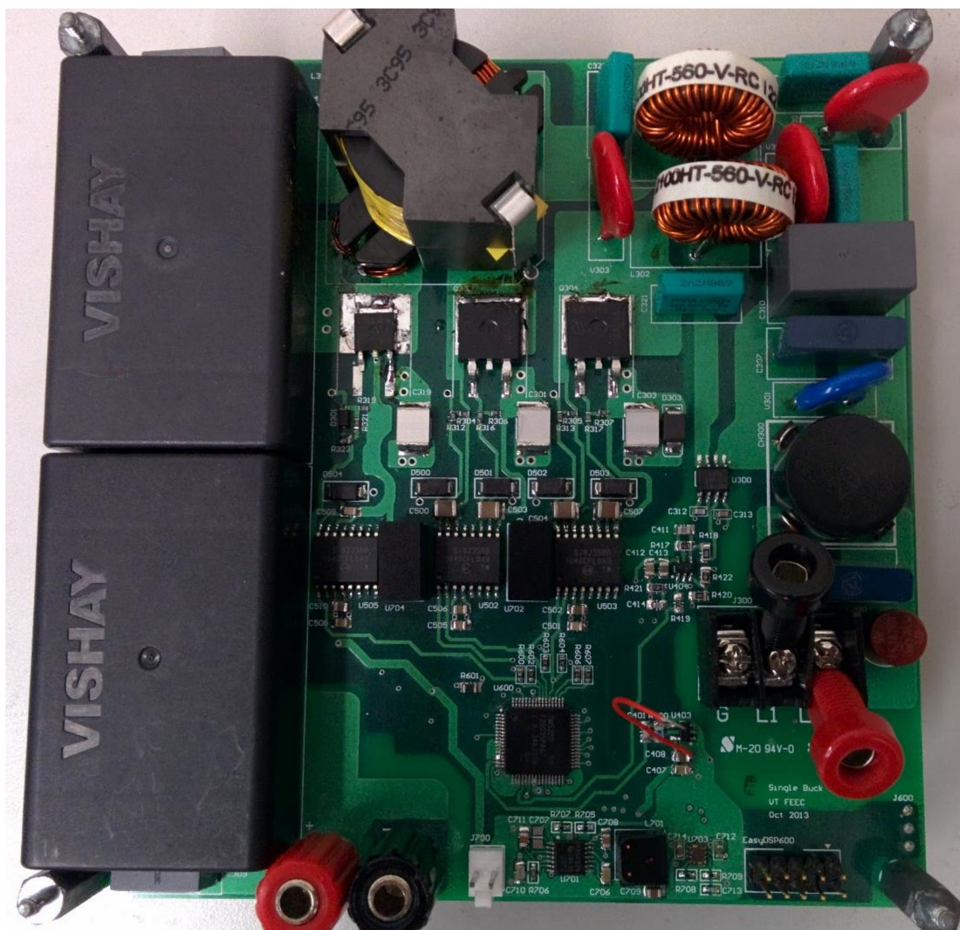


Figure 4.11: Single Buck Inverter Test PCB

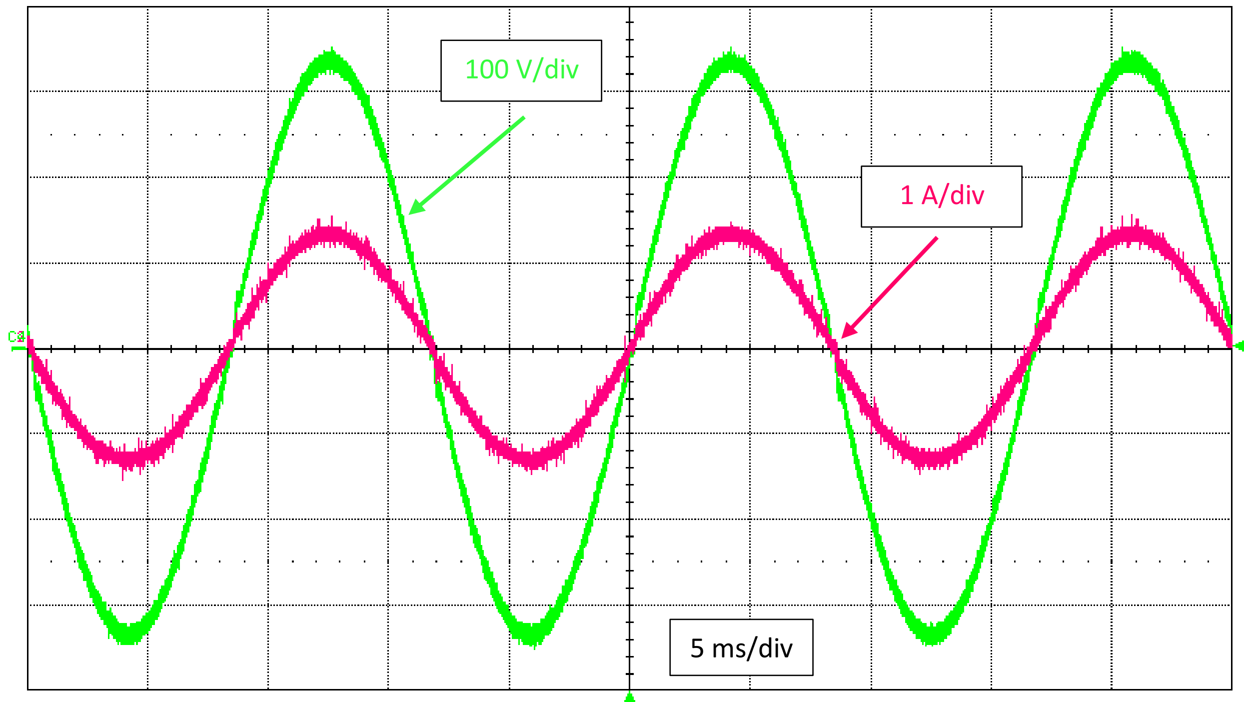


Figure 4.12: Single Buck Inverter Output Voltage and Current at 100% Load

The efficiency of the single buck inverter over the entire CEC efficiency range for both semiconductor devices is shown in Figure 4.13.

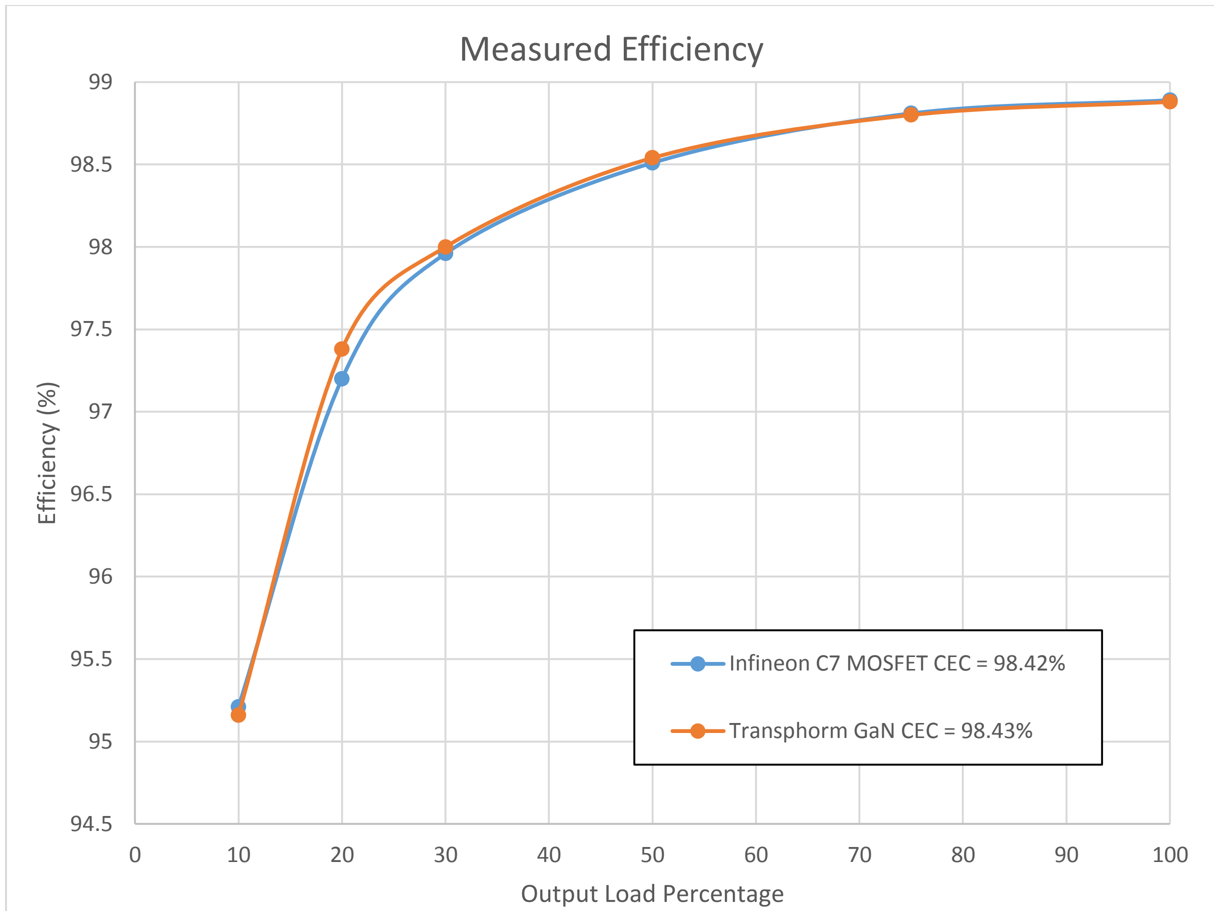


Figure 4.13: Single Buck Inverter Efficiency for Different Semiconductors

Performance of the Transphorm has a small improvement over Infineon's C7 superjunction MOSFET. The big difference between the two devices is the conduction loss, the on resistance for the C7 MOSFET is 225 mΩ while the Transphorm GaN is 290 mΩ. It is difficult to come to a conclusion about the difference in losses due to proximity of the efficiency that could be affected by measurement error.

4.5.4 Common Mode Noise Results

Using an isolated differential probe the CM voltage was measured from the output to ground shown in Figure 4.14. CM voltage of the single buck inverter is consistent with the CM voltage simulation results.

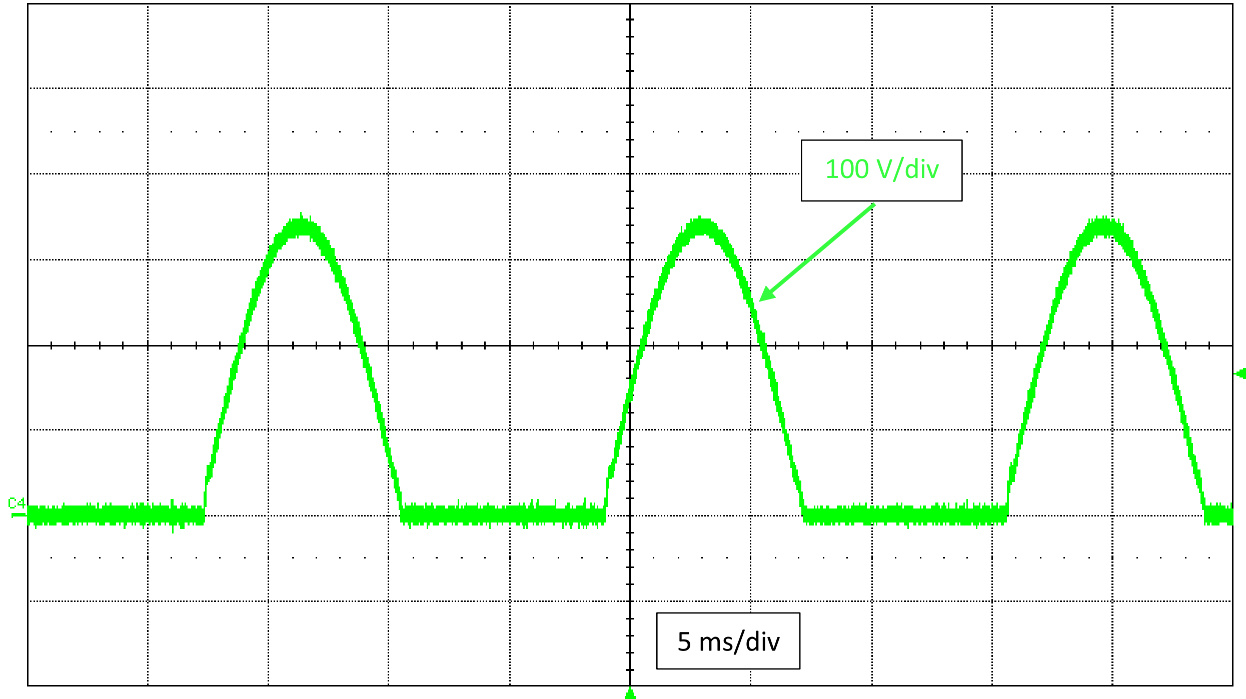


Figure 4.14: Single Buck Inverter Common Mode Voltage

4.6 SHREC Inverter Testing

The SHREC inverter's biggest advantages are the improvement of the inverter reliability by eliminating the possibility of shot-through conditions. CM performance is as good as the HERIC and bipolar full bridge inverters. Differences from the other tested inverters involve the large number of semiconductor devices and output filter inductors.

4.6.1 Magnetic Considerations

Magnetic core shape, material and wire remain the same as the other inverters test with the key difference being that the topology requires four inductors to operate. Current during the positive line cycle goes through two inductors and during the negative line cycle goes through the other two inductors. Since the current going through both inductors for each line cycle is the same it is possible to couple those two inductors to the same magnetic core, this reduces the total number of magnetic cores from four to two. Coupling between the two inductors must be very tight in order to minimize circulating energy between both windings. Tight coupling can be achieved using a bifilar winding pattern. Even though the number of magnetics have increased the conduction and core loss in the magnetics are equivalently the same as one inductor due to the fact that there is no current flow during

half the line cycle in one of the magnetics at a given time. This advantageous in dealing with the increase in resistance of the wire due to the effects of heating, as the current is distributed between to separate magnetics. Inclusion of another magnetic severely increases the cost of the system.

4.6.2 Semiconductor Considerations

Selection criteria for semiconductor components in the SHREC inverter are similar to all other tested inverters with the exception of the full bridge inverter. The key design issue for this inverter is the use of low reverse recovery diodes for the freewheeling diodes in each output decoupling switches. Use of SiC Schottky diodes can guarantee a reduction of switching loss at the penalty of higher cost and higher conduction losses. The low frequency switches should use devices with a low conduction loss since they transition at zero voltage and zero current periods.

For selection of the high frequency switches it should be a superjunction MOSFET with a low output capacitance and reasonable on resistance. Infineon's CoolMOS C7 225 mΩ 650 V superjunction MOSFET IPB65R225C7ATMA in TO-263 (D^2PAK), is a good device due to the low output capacitance and good switching characteristics. Active low frequency switches should be the same as the full bridge inverter low frequency switches, Infineon's CoolMOS C7 45 mΩ 650 V superjunction MOSFET IPB65R045C7ATMA in TO-263. Cree's SiC Schottky diode 3A 600V C3D03060E in TO-252 was selected as the freewheeling diode due to its low capacitance and negligible reverse recovery charge. The diodes that are in series with the high frequency switches do not carry any current and are used to clamp the active switches to the input voltage. Standard high voltage silicon diodes can suffice for these devices.

4.6.3 Efficiency Results

The test PCB for the SHREC inverter is shown below in Figure 4.15.

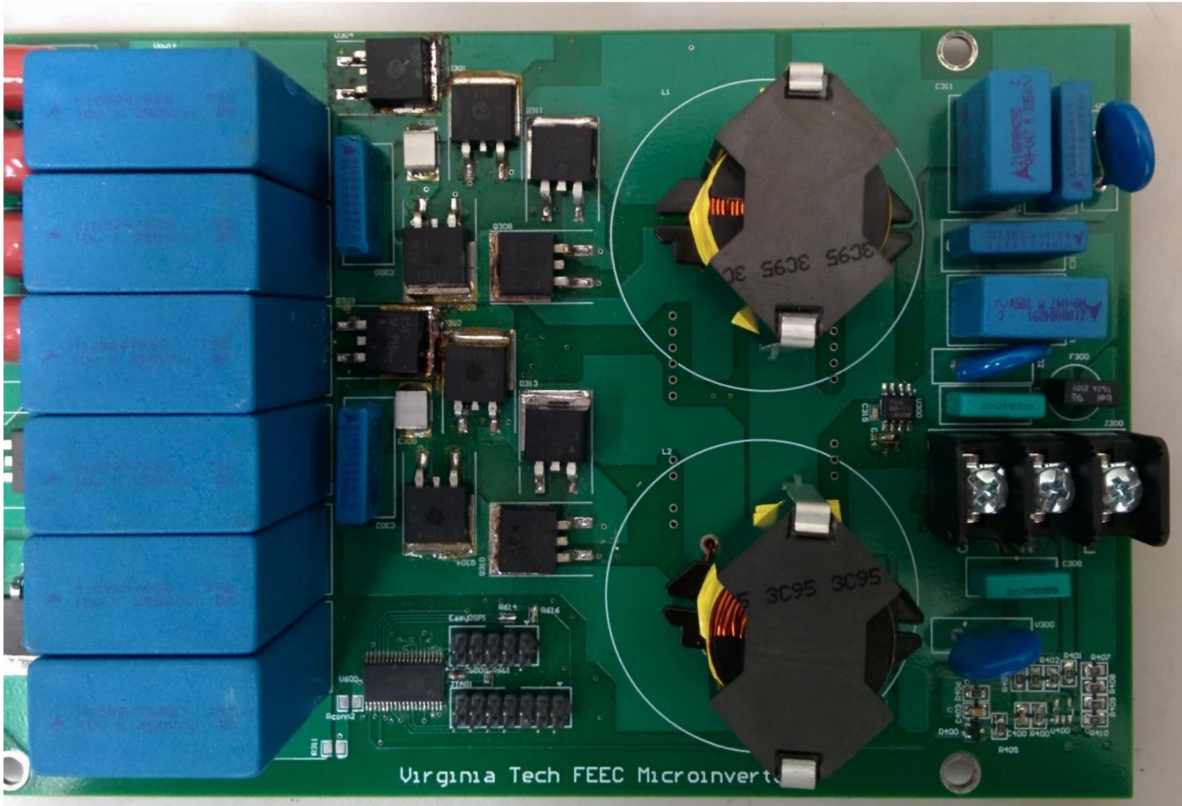


Figure 4.15: SHREC Inverter Test PCB

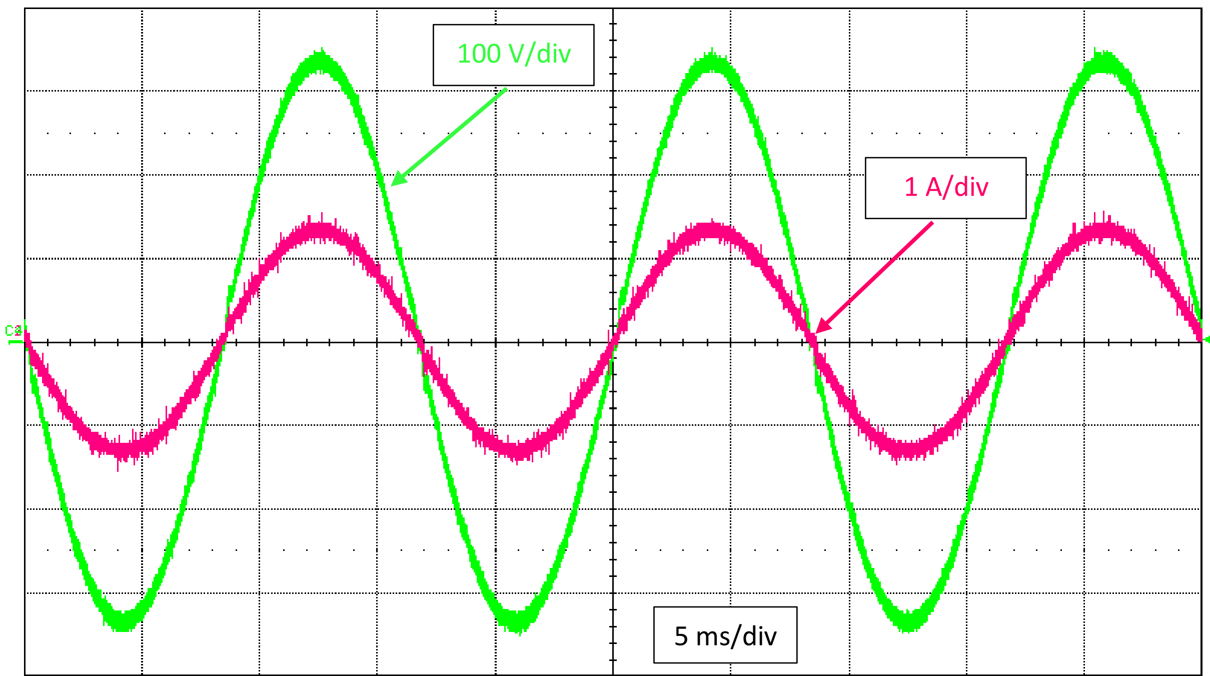


Figure 4.16: SHREC Inverter Output Voltage and Current at 100% Load

SHREC inverter efficiency over the entire CEC load range is shown in Figure 4.17.

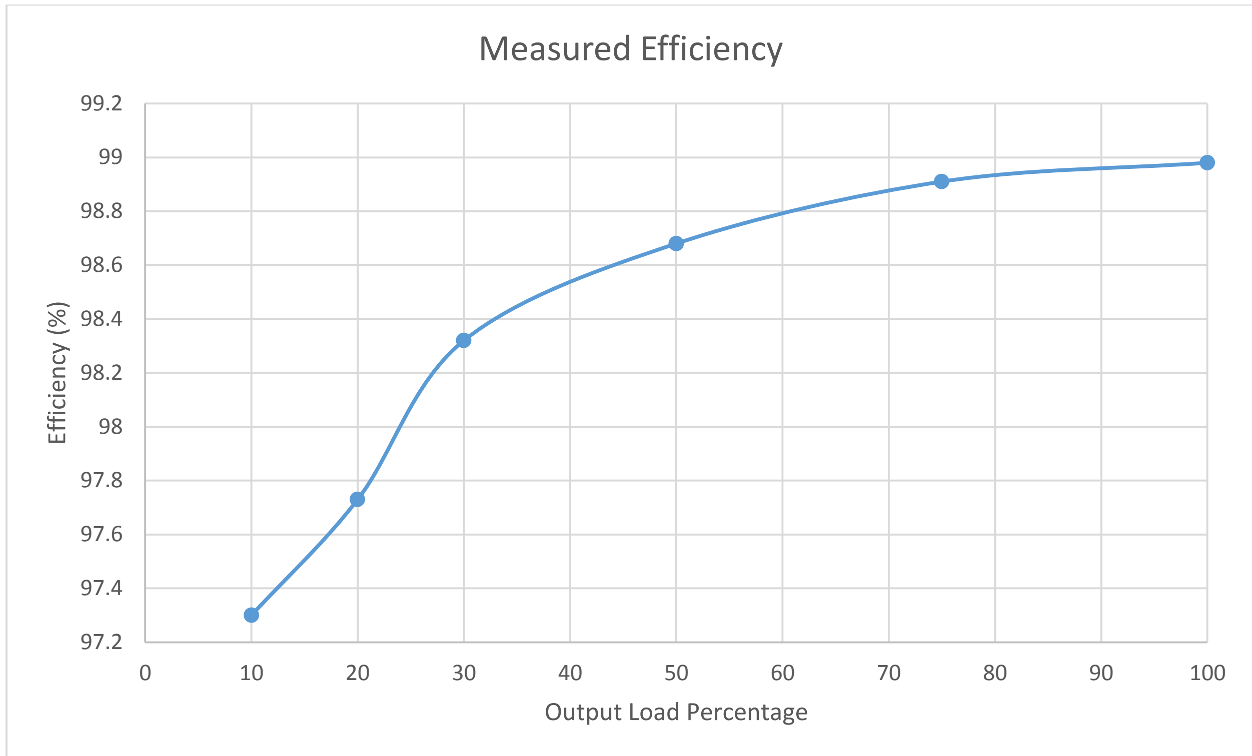


Figure 4.17: SHREC Inverter Efficiency

Peak efficiency of the unipolar dual buck inverter is 98.98% and the CEC efficiency is 98.67%. Compared with the most of the other tested inverters the efficiency of the SHREC is the highest due to the reduced switching losses because half the bush voltage is across each active device during the switching transition while all other compared topologies have the entire bus voltage across the active devices. One of the big disadvantages of the SHREC inverter is that there are two high frequency devices on during the active switching periods doubling the on state conduction losses compared to the other tested topologies.

4.6.4 Common Mode Noise Results

Using an isolated differential probe the CM voltage was measured from the output to ground shown in Figure 4.18. SHREC inverter CM voltage characteristics matches with the earlier CM voltage simulation results.

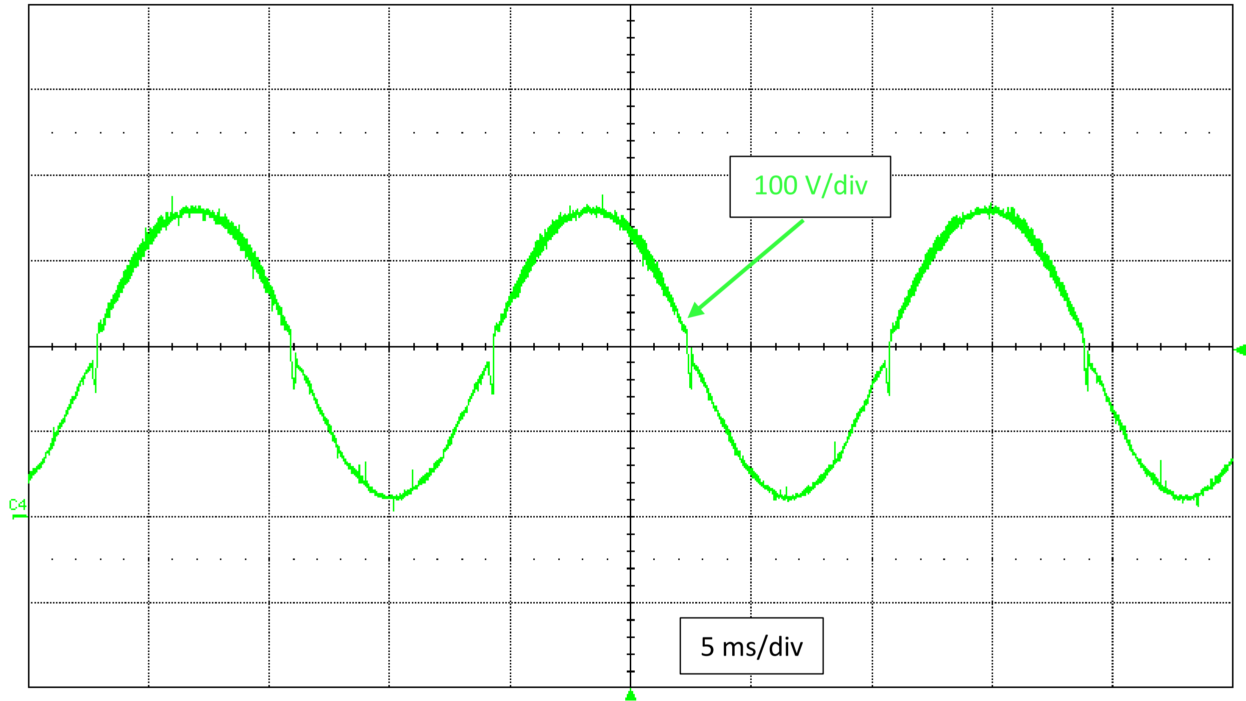


Figure 4.18: SHREC Inverter Common Mode Voltage

4.7 Test Result Comparison

Using the results from all inverter topologies that were tested it is possible to determine the optimal inverter configuration based on the merits of efficiency, component count and CM performance. Table 4.4 summarizes the key comparison characteristics for each tested inverter topology.

Inverter	CEC Efficiency (%)	CM Performance	Number Active Switches	Number Freewheeling Diodes	Number Inductors	Number Auxiliary Power Supplies	Cost
Full Bridge with CFD2	97.77	Fair	4	0	1	1	Low
Full Bridge with Trenchstop IGBT	98.38	Fair	4	0	1	1	Low
Full Bridge with GaN	98.64	Fair	4	0	1	1	High
Unipolar Dual Buck	98.49	Good	4	2	2	3	High
Single Buck	98.42	Good	5	1	1	2	Medium
SHREC	98.67	Best	6	2	2	5	High

Table 4.4: Inverter Efficiency Results and Characteristics

From the table it is clear that the SHREC inverter has the highest CEC efficiency of all the inverters tested. The inverter with the next highest efficiency is the full bridge using Transphorm's GaN HEMT. Lowest CEC efficiency is the full bridge inverter using Infineon's CFD2 superjunction MOSFETs. CM noise is the highest for all the full bridge inverters and the lowest for the SHREC inverter. Although the SHREC has the best efficiency and CM performance the system cost is the highest compared to the other inverters by a wide margin; due to the large amount of semiconductors required, two inductors and high number of auxiliary circuitry required to operate the active switches. The second highest cost inverter is the full bridge using GaN, the price of these semiconductors are very high with little cost reduction at higher volumes.

5 CONCLUSION

The majority of the microinverter analysis has been conceptual with only simulation and calculated comparisons for different inverter topologies. Drawbacks to this method of comparison include lack of accurate data for semiconductor device switching performance and difficulty in obtaining the core loss characteristics for an inverter. SPICE based simulations can improve the comparison, but the models for the semiconductor devices are linearized and do not take into account the layout and other parasitic elements that effect the device switching characteristics. In order to better understand the behavior and performance of different inverter topologies it is necessary to design, build and test various inverter systems using the same experimental setup. Comparing inverter topology performance from other papers can lead to an inaccurate comparison due to the variation in testing equipment, semiconductor devices and the power range at which the system was tested.

Several inverter topologies suitable for a PV microinveter system were covered detailing their modes of operation and behavior. Material considerations for components in an inverter system were covered to show how they affect the behavior, cost and reliability of the inverter. The major components that affect the performance of the inverter system include semiconductor devices and magnetic materials. Prototype circuits for several of the reviewed topologies were built and tested with different semiconductor devices used to compare their performance. Wideband-gap semiconductor devices were included in the testing to verify their impact on improving system performance. Using GaN HEMT devices and SiC Schottky diodes, high efficiency can be obtained for inverter topologies that often regarded has having limited performance.

System comparison using experimental results helps further validate the theoretical operation of each inverter topology while providing experience in practical implementation. The major points emphasized in this thesis include:

- Comparison of inverter topologies by covering modes of operation and characteristics that impact efficiency and CM performance.
- Discussion of key material characteristics that impact efficiency and reliability for PV microinverter applications in order to implement improved designs.
- Evaluation of newer wideband-gap semiconductor materials and how they impact efficiency and reliability.

- Prototypes for several inverter topologies were designed, built and tested to establish the validity of the inverter component design recommendations.
- Efficiency of a traditional full bridge VSI was improved to 99.04% peak using GaN HEMTs, surpassing the peak efficiency of all other tested inverters.

5.1 Future Work

Additional work can be performed to provide a more accurate comparison of inverter topologies as well as improving the performance of inverters.

- Looking into improving the accuracy of the core loss analysis for inverter systems.
- Determine if there is a more accurate method of characterizing semiconductor device switching performance.
- Investigate the performance of newer wideband-gap semiconductor devices.
- Research and design an interleaved full bridge inverter that uses boundary conduction operation to achieve zero voltage switching in order to evaluate its performance.

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