DC Fault Current Analysis and Control for Modular Multilevel Converters

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Abstract

Recent research into industrial applications of electric power conversion shows an increase in the use of renewable energy sources and an increase in the need for electric power by the loads. The Medium-Voltage DC (MVDC) concept can be an optimal solution. On the other hand, the Modular Multilevel Converter (MMC) is an attractive converter topology choice, as it has advantages such as excellent harmonic performance, distributed energy storage, and near ideal current and voltage scalability.

The fault response, on the other hand, is a big challenge for the MVDC distribution systems and the traditional MMCs with the Half-Bridge submodule configuration, especially when a DC short circuit fault happens. In this study, the fault current behavior is analyzed. An alternative submodule topology and a fault operation control are explored to achieve the fault current limiting capability of the converter.

A three-phase SiC-based MMC prototype with the Full-Bridge configuration is designed and built. The SiC devices can be readily adopted to take advantage of the wide-bandgap devices in MVDC applications. The Full-Bridge configuration provides additional control and energy storage capabilities. The full in-depth design, controls, and testing of the MMC

prototype are presented, including among others: component selection, control algorithms, control hardware implementation, pre-charge and discharge circuits, and protection scheme.

Systematical tests are conducted to verify the function of the converter. The fault current behavior and the performance of the proposed control are verified by both simulation and experiment. Fast fault current clearing and fault ride-through capability are achieved.

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Chapter 1. Introduction

1.1 Medium-Voltage DC Distribution System

Recent research into industrial applications of electric power conversion shows an increase in the use of renewable energy sources and an increase in the need for electric power by the loads. The Medium-Voltage DC (MVDC) concept can be an optimal solution. A general layout of a MVDC distribution system is shown in Fig. 1-1[1]. It is designed as a collection platform to integrate renewable energy, serve expanding loads, interconnect energy storage, interconnect grids and address future needs [2]. The MVDC distribution systems have been proved or proposed in a variety of applications such as shipboard integrated power systems [3]-[6], railway electrification systems [7], offshore wind farms [8]-[10], photovoltaic power stations [11] [12], data centers [13], electric vehicle charging stations [12], fuel cells [14] and so on. They are also capable of connecting with existing AC transmission systems or future High-Voltage DC (HVDC) systems [2].

Compared to traditional AC systems, the MVDC distribution systems exclude bulky line frequency transformers, thus significantly reduce the overall size and weight of the power conversion stations [8]. DC transmission and distribution can also reduce power losses because of absence of reactive current and less conversion stages when integrating distributed generation units and supplying DC-based loads [15]. In addition, using DC grids also eliminates reactive voltage drop and the need for phase angle synchronization [5].

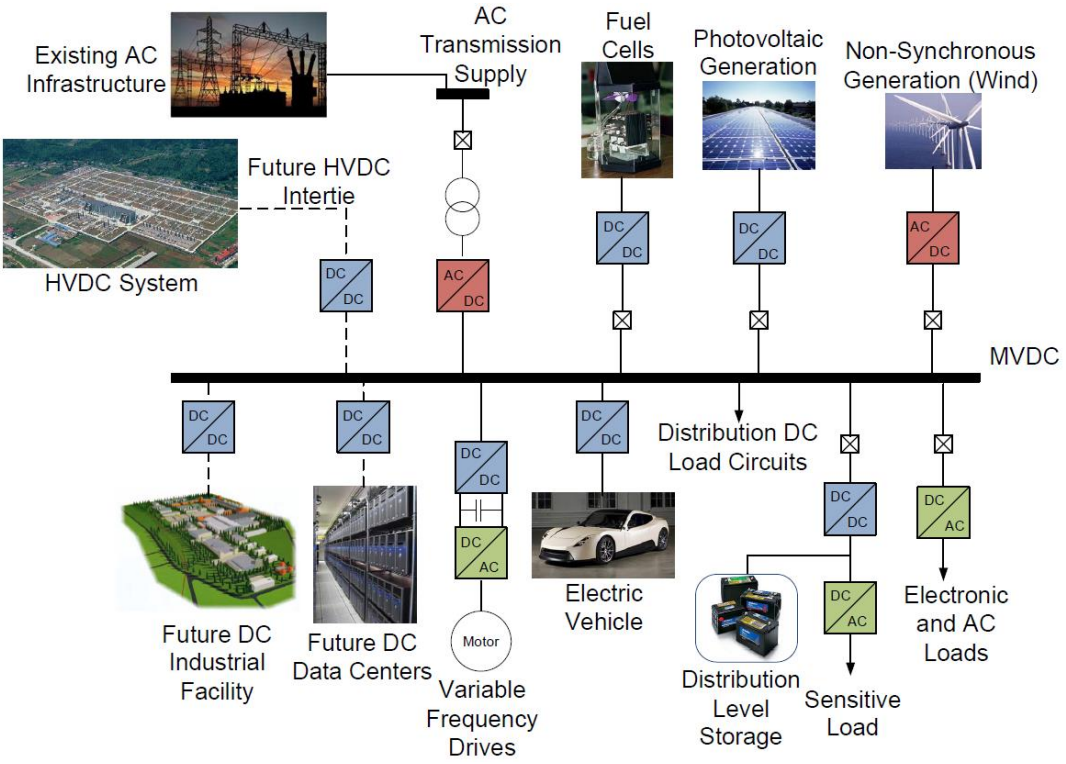


Fig. 1-1 The general structure of a MVDC substation

It is especially explored that MVDC distribution systems can be used as all-electric ship Shipboard Power Systems [3]. Both commercial and naval ships need to power many DC loads, such as propulsion, radar and weapon systems, and are also expected to integrate renewable energy sources and storage systems [4]. These make MVDC a perfect fit for the desired requirements and functions. IEEE Std 1709-2010 [5] has been defined as the recommended practice for MVDC power systems on ships and can be used as a guideline for relevant design and analyses.

1.2 Modular Multilevel Converter

The MVDC distribution system requires power converters for interconnection and power conversion. Voltage and current quality, efficiency, size and weight, cost, and modularity are

some major considerations. The Modular Multilevel Converter (MMC) [16] [17] provides an attractive solution. The circuit configuration of a MMC is shown in Fig. 1-2.

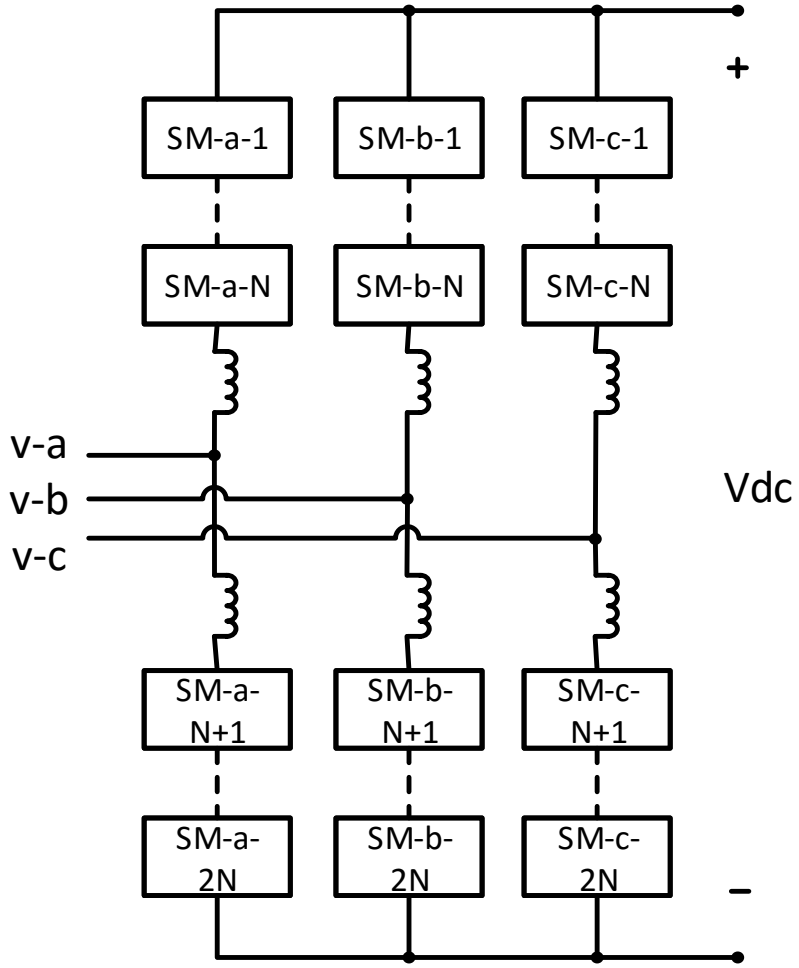


Fig. 1-2 Circuit configuration of a Modular Multilevel Converter

In the MMC topology, a group of series-connected identical submodules and inductors form a converter arm; then two series-connected converter arms form a converter phase-leg. It is recommended that the submodules should be based on Power Electronics Building Blocks (PEBBs) [5]. The converter PEBBs usually consists of a capacitor bank, a number of switching devices, auxiliary circuit, control hardware, sensors and protection devices. The conventional PEBB topology used in the MMC is a half-bridge [18]. However, to improve its operating

capability and performance as well as its fault-current limitation ability [19] [20], other PEBB topologies have been proposed and will be discussed in later sections.

In Fig. 1-2, the MMC is used to connect a three-phase AC bus and a DC bus, with power flowing either from AC to DC or from DC to AC. The multilevel AC voltage generated by the MMC has a low voltage step of $\frac{V_{dc}}{N}$ [21]; the phase shifting modulation can be applied to cascaded connected PEBBs, achieving a high equivalent frequency while maintaining a low actual switching frequency [22]. Therefore, the MMC has excellent power quality at both AC and DC terminals as well as low losses. Due to the use of identical PEBBs, the MMC has the benefits of modular design, simple realization of redundancy and scalability in terms of voltage and current, which allows it to operate at higher voltages and currents by connecting modules in series or parallel if necessary [17].

1.3 Challenges and Limitations

Fault response is one of the desired functions of the MVDC systems. According to IEEE Std 1709-2010, it is recommended that all the power converters should be designed to have the fault currents limit ability to minimize the need for load side circuit breakers [5]. When a fault happens, converters should be able to detect the fault, limit the fault current, reconfigure the system and protect equipment and cables, as well as achieve restoration of service after a fault [6]. Generally speaking, the systems require a series of coordinated actions by relays, fuses and converters to achieve the primary protection and also the backup protection [41].

However, the original MMC with the HB topology lacks the fault current limit ability and is vulnerable to a DC short circuit fault. Three methods for the DC fault current limiting are summarized in [23]. The traditional method employs an AC circuit breaker but has the drawback of a long switching time. It also requires thyristor switches [18] or double thyristor switches [24] to bypass the PEBB to protect the original switching devices. The second method employs a DC circuit breaker but is restricted by the immature technology. This leads our attention to the third method, which employs the converter itself to handle the fault [25] [26]. Since the MMC has distributed capacitances instead of a centralized bus capacitance, when certain faults happen, the internal energy storage has the potential to prevent stored energy from feeding the fault continuously. Various new PEBB topologies and new control methods have been proposed in order to achieve the DC-fault-handling capability of the MMC, which is defined as the ability to limit or clear fault current during the DC fault condition.

1.4 Thesis outline

Taking into account the threat of DC fault to the MVDC distribution system and the MMC, the focus of this work is to analyze the DC fault behavior of the MMC, and to explore and verify how the converter could provide fault current limit function.

Chapter 1 introduces the applications, benefits and challenges of the MVDC distribution system and the MMC. Chapter 2 describes the operation principle, modeling and control of the MMC. Chapter 3 conducts the DC fault behavior analyses, proposes a DC fault operation control and verifies it through simulation. Chapter 4 details the design of a converter prototype

used to verify current limit function and interprets the test results. Chapter 5 summarizes the work and discusses possible future work.

Chapter 2. Operating Principle and Control of Modular Multilevel Converter

The operating principle and the control of the Modular Multilevel Converter are introduced in this chapter. They are well investigated and discussed in the literature and are essential for this work. The configuration of a MMC with Half-Bridge (HB) PEBBs operating as a rectifier is shown in Fig. 2-1. MMCs built with other PEBB topologies or MMCs operating as an inverters are quite comparable.

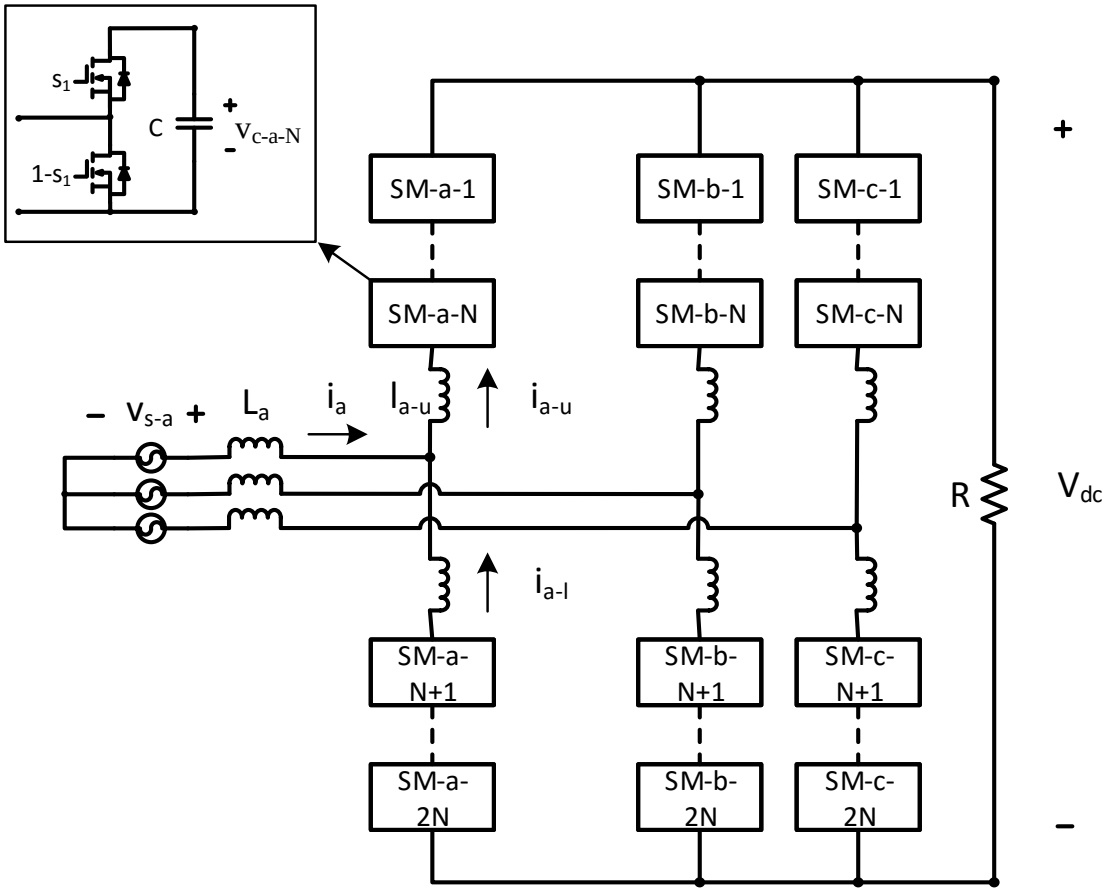


Fig. 2-1 Circuit configuration of a MMC with HB PEBBs operating as a rectifier

2.1 Operating Principle of Modular Multilevel Converter

During the steady state of the normal operation of a MMC, the voltages of all the capacitors in PEBBs remain around a constant value, which equals to:

$$v_C \approx \frac{V_{dc}}{N} \tag{2-1}$$

Where v_C is the instant voltage of one capacitor, V_{dc} is the rated DC bus voltage, N is the number of PEBBs in a converter arm.

By controlling the gate signals of the switching devices in the PEBB, the capacitor is either inserted into the converter arm or bypassed, resulting in a output voltage of v_C or 0. Assuming the direct modulation is used, which does not consider any compensations, the duty ratio of one PEBB in phase A is:

$$\begin{cases} d_{a-u} = \dfrac{1 - M\cos(\omega t)}{2} \\ d_{a-l} = \dfrac{1 + M\cos(\omega t)}{2} \end{cases} \tag{2-2}$$

Where d_{a-u} is the duty ratio of every PEBB in the upper arm of phase A, d_{a-l} is the duty ratio of every PEBB in the lower arm of phase A, ω is the output line angular frequency, M is the modulation index, which equals to:

$$M = \frac{\sqrt{2}V_{ac}}{V_{dc}/2} \tag{2-3}$$

Where V_{ac} is the RMS value of the desired AC voltage generated by the converter. Then the total voltage generated by all the PEBBs in one converter arm is:

$$\begin{cases} v_{a-u} = d_{a-u} \times v_c \times N \approx \dfrac{V_{dc}}{2} - \sqrt{2}V_{ac}\cos(\omega t) \\ v_{a-l} = d_{a-l} \times v_c \times N \approx \dfrac{V_{dc}}{2} + \sqrt{2}V_{ac}\cos(\omega t) \end{cases} \tag{2-4}$$

Where v_{a-u} is the total voltage generated by all the PEBBs in the upper arm of phase A, v_{a-l} is the total voltage generated by all the PEBBs in the lower arm of phase A. The sum of the two voltages is equal to the DC bus voltage, and an AC voltage is generated at the middle point of the phase leg. Equations (2-2)-(2-4) can be extended to phase B and C except that the AC voltages have a $-120°$ degree shift (phase B) and a $120°$ degree shift (phase C) compared to phase A. Thus, the MMC can have a steady power exchange with both the DC bus and the AC bus.

The upper arm current and the lower arm current of one phase share a common component and have another component with the same value but a different sign. The common component is also known as the circulating current, which can be defined as:

$$i_{a-circ} = \frac{i_{a-u} + i_{a-l}}{2} \tag{2-5}$$

Where i_{a-circ} is the circulating current of phase A, i_{a-u} is the upper arm current of phase A, i_{a-l} is the lower arm current of phase A.

Ref [27] [28] performed detailed harmonic analyses regarding the circulating current. The circulating current includes a DC component, a second order component and higher frequency components. The first two components are dominant. The DC component is one third of the DC bus current.

$$i_{a-circ} = I_{a-dc} + \sqrt{2} I_{a-2} \sin\left(2\omega t + \theta_2\right) + \cdots = \frac{I_{dc}}{3} + \sqrt{2} I_{a-2} \sin\left(2\omega t + \theta_2\right) + \cdots \tag{2-6}$$

Where I_{a-dc} is the DC component in the circulating current of phase A, I_{a-2} is the RMS value of the second order harmonic in the circulating current of phase A, I_{dc} is the DC bus current. However, only the DC component is desired as it flows through the DC bus to perform

power exchange. The seconder order harmonic, as well as the higher frequency harmonic, will increase the current stress and the losses of the switching devices [29].

Based on Kirchhoff's current law, the arm currents and AC current have the following relationship:

$$i_a = i_{a-u} - i_{a-l} \tag{2-7}$$

Where i_a is the AC bus current of phase A.

Therefore, the arm currents equal to:

$$\begin{cases} i_{a-u} = i_{a-circ} + \dfrac{i_a}{2} \\ i_{a-l} = i_{a-circ} - \dfrac{i_a}{2} \end{cases} \tag{2-8}$$

Equations (2-5)-(2-8) can be extended to phase B and C.

2.2 Closed-loop Control of Modular Multilevel Converter

The closed-loop control of MMC is needed to compensate the non-idealness in the actual converter and improve the performance. A lot of work [29]-[36] has been done in the literature. The control objective includes external voltage and current, circulating current, average capacitor voltage, capacitor voltage balancing, etc. In this study, the control methods proposed in [29]-[31] are employed. The complete control strategy can be divided into three levels: three-phase current loop control, phase leg control and individual PEBB control. Then gate signals are generated based on the overall control command.

2.2.1 Three-phase Current Loop Control

The scheme of the three-phase current loop control is shown in Fig. 2-2, which is based on [30]. Three-phase current is regulated to achieve the desired DC voltage and reactive power.

The input of the current loop control is the sensed DC bus voltage, the sensed AC bus voltage and current. The output is the three-phase AC voltage reference. A Phase-Locked Loop (PLL) is used to acquire phase information based on sensed voltage. The scheme of a PLL is shown in Fig. 2-3. A feedback angle information is used to transfer the three-phase voltage into d-q frame. Since the desired q axis component is zero (which means the acquired angle information is in phase with the original phase A angle), the q axis component is accumulated by a PI controller to acquire angular frequency, then the angular frequency is integrated to acquire phase information. After the state variables in PLL reaches the steady state, three-phase AC voltage and current can be accurately transformed into the d-q frame.

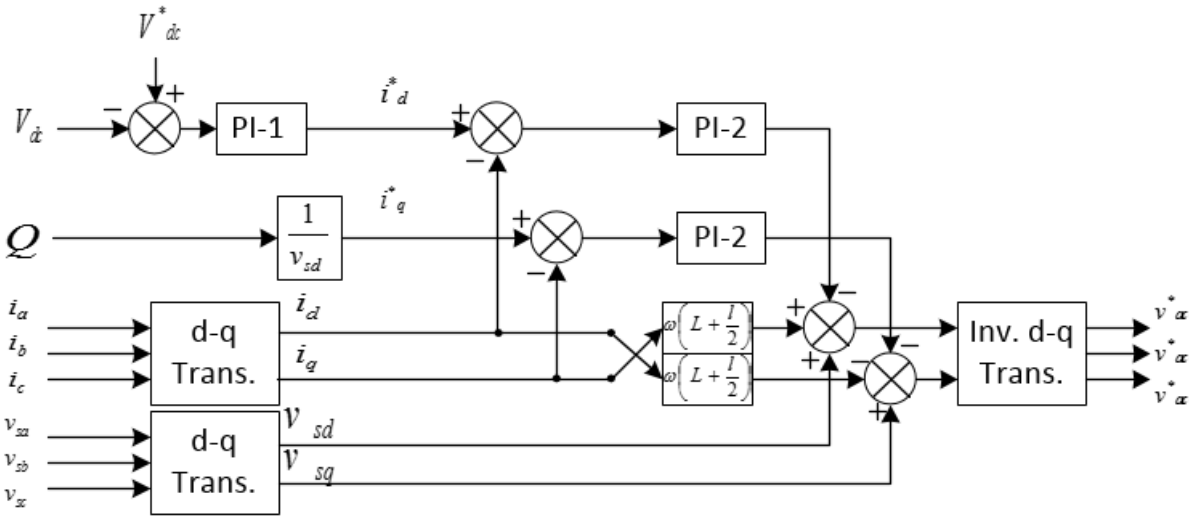


Fig. 2-2 Three-phase current loop control

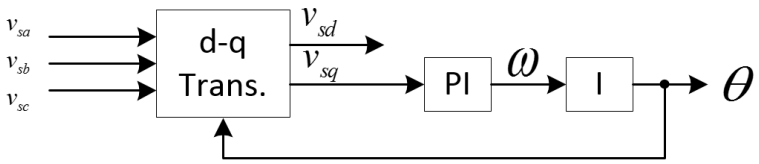


Fig. 2-3 Phase-Locked Loop

The error between the sensed DC voltage and the desired DC voltage is accumulated by a PI controller to provide the d axis current reference. When the DC voltage is lower than desired, the d axis current reference increases, controlling move active power transferring from the AC source to the converter, and then to the load. The desired reactive power, divided by d axis voltage, is the q axis current reference. Then another two PI controllers regulate the d, q axis currents to follow the references respectively. Voltage and current information is also added to achieve d-q decoupling.

2.2.2 Phase Leg Control

The scheme of the phase leg control is shown in Fig. 2-4, which is based on [29], [30]. In each phase, the circulating current is regulated to achieve the average voltage control and the circulating current suppression. As the converter has three phase legs, there are three separate phase leg controls (with the same structure and parameters) preformed at the same time.

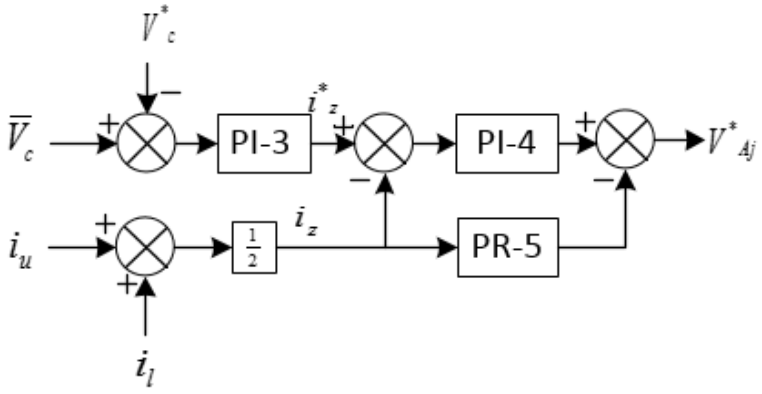


Fig. 2-4 Phase leg control

For each phase leg control, the input is 2N sensed PEBB capacitor voltages, the sensed upper arm current and lower arm current. The output is voltage command V^*_{Aj} for all the PEBBs in this phase leg.

First, the average value of 2N sensed PEBB capacitor voltage $\overline{V_C}$ is compared to the desired capacitor voltage value V^*_C. The error goes through a PI controller to generate a reference for the circulating current. If the actual average capacitor voltage is higher than the desired value, the circulating current reference increases, controlling more power flowing from the converter arm to the load, and releasing the energy in the capacitors and decreasing the voltage.

Then another PI controller controls circulating current to follow the reference. As the circulating current does not include fundamental frequency component of the arm current, this part of control will not affect the AC link current.

A quasi PR controller is placed in parallel with the fourth PI controller. The transfer function is:

$$G_{QPR}(s) = K_p + \frac{2\omega_c K_{r1} s}{s^2 + 2\omega_c s + (2\omega_0)^2} + \frac{2\omega_c K_{r2} s}{s^2 + 2\omega_c s + (4\omega_0)^2} + \cdots \quad (2\text{-}9)$$

Where K_p is the proportional gain, K_{r1} and K_{r2} are gain for different frequencies, ω_C is the bandwidth parameter, and ω_0 is line angular frequency.

The above controller can achieve high gain at the selected resonant frequency. In this case, the double line frequency is apparently selected to suppress the second order harmonic in the circulating current. It is also preferred to suppress higher frequency (240 Hz, 360 Hz and so on) to further improve the performance [29]. With the PR controller, the undesired AC components in the circulating current are almost eliminated, leaving only the DC component. By doing this, the system will have a higher efficiency.

2.2.3 Individual PEBB Control

The scheme of the individual PEBB control is shown in Fig. 2-5 and Fig. 2-6, which is based on [31]. For each PEBB, voltage is controlled individually. Then, all the control commands from all three levels are combined together to calculate the desired duty ratio of each PEBB. As the converter has 6N PEBBs, there are 6N individual PEBB controls (with the same structure and parameters) preformed at the same time.

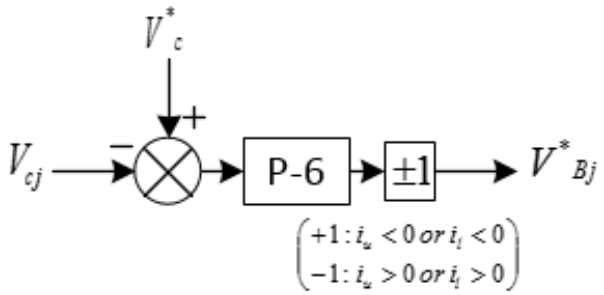
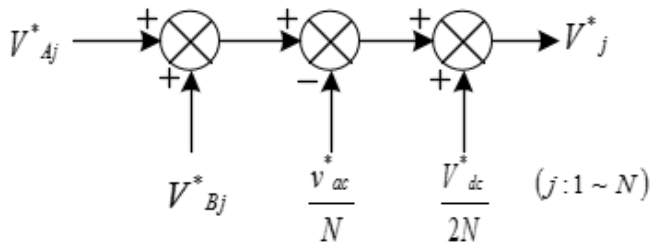
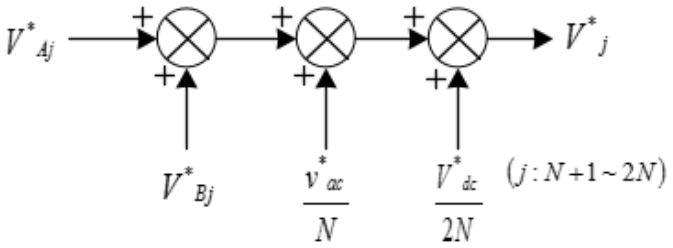


Fig. 2-5 Individual PEBB control



(a)



(b)

Fig. 2-6 Overall control command

For each individual PEBB control, the input is the sensed PEBB capacitor voltage, the sensed arm current as well as the aforementioned control commands (three-phase AC voltage reference and phase leg control command). The output is desired duty ratio d_j.

The scheme of the individual voltage control is shown in Fig. 2-5. The sensed capacitor voltage of the j[th] PEBB V_{cj} is compared to the desired capacitor voltage value V^*_C. The error is amplified by a proportional gain to calculate the value of the individual voltage control command. However, the polarity of the command depends on both the voltage and the current. For example, if the actual capacitor voltage is lower than the desired value, the capacitor should be charged more than usual or discharged less than usual. The instant charge/discharge state depends on the arm current. For $j = 1,2,\cdots,N$, the upper arm current is used; for $j = N+1, N+2,\cdots,2N$, the lower arm current is used. If the current is positive, the PEBB capacitor is being discharged. We can decrease the time the PEBB is being connected in the arm to let it discharged less than usual. Therefore, the control command should have a negative polarity. If the current is negative, the PEBB capacitor is being charged. We should increase the duty ratio. Therefore, the control command should have positive polarity.

Then all the control commands and DC reference are combined together, as shown in Fig. 2-6. V^*_{Aj} is the control command from phase leg control, V^*_{Bj} is the individual voltage control, v^*_{ac} is AC voltage reference from current loop control, V^*_{dc} is the desired DC bus voltage. The AC voltage reference is divided by N, the DC voltage reference is divided by $2N$. Then, the total voltage of upper arm and total voltage of lower arm approximately equals to:

$$\begin{cases} v_{a-u} \approx \dfrac{V^*_{dc}}{2} - v^*_{ac} \\ v_{a-l} \approx \dfrac{V^*_{dc}}{2} + v^*_{ac} \end{cases} \tag{2-10}$$

In this way, the converter arms keep balance with both the DC bus and the AC bus.

Finally, the overall control command is normalized by the desired capacitor voltage to calculate the duty ratio for each PEBB:

$$d_j = \frac{V^*_j}{V^*_c} \tag{2-11}$$

2.2.4 Modulation

After the duty ratio is calculated by the closed-loop control, the gate signals are generated using a certain modulation technique. The phase shifting and the level shifting carrier-based Pulse-Width-Modulations (PWMs) are two easy methods to achieve a proper operation [22]. The phase shifting method results in less ripple and less filtering requirements when compared to the level shifting. Space vector modulation can also be used to improve operation in terms of losses, common mode voltage and so on. However, the algorithm is extremely complicated when the converter has a lot of PEBBs [37]. In that case, the nearest level modulation can be an alternative because of easy implementation [38].

2.3 Simulation Verification

A simulation model is established in “MATLAB/Simulink”. The circuit configuration is the same as shown in Fig. 2-1. The specifications of the converter and the control parameters are summarized in Tab. 2-1 and Tab. 2-2 respectively. The interleaved phase shifting PWM is used as the modulation method for easy implement and good harmonic cancellation [31].

Tab. 2-1 Specifications of the converter in simulation study

Converter specifications		Component specifications	
Active power	3.5 MW	Load Resistance	14 Ω
Reactive power	0	Capacitor voltage	1 kV
AC line RMS voltage	4.16 kV	Capacitor voltage ripple	100 V
DC bus voltage	8 kV	PEBB capacitance	3.5 mF
Number of PEBBs in one arm	8	Arm inductance	4 mH
Line frequency	60 Hz	AC inductance	1 mH
Switching frequency	1 kHz		

The simulation results during the normal operation $0.2s \sim 0.4s$ are shown in Fig. 2-7. From the waveforms, it can be observed that DC voltage and reactive power are regulated well. The circulating current almost only has a DC component. Thus, the arm currents almost only have the DC component and the fundamental frequency AC component. The average value and the ripple of the capacitor voltage are also similar as expected.

Tab. 2-2 Control parameters used in simulation study

Controller	Parameters
PI-1	$K_p = 0.01, K_i = 1$
PI-2	$K_p = 4, K_i = 200$
PI-3	$K_p = 0.2, K_i = 20$
PI-4	$K_p = 2, K_i = 10$
PR-5	$K_p = 0.01, \omega_c = 10, K_{r1} = 25, K_{r2} = 5$
P-6	$K_p = 0.1$

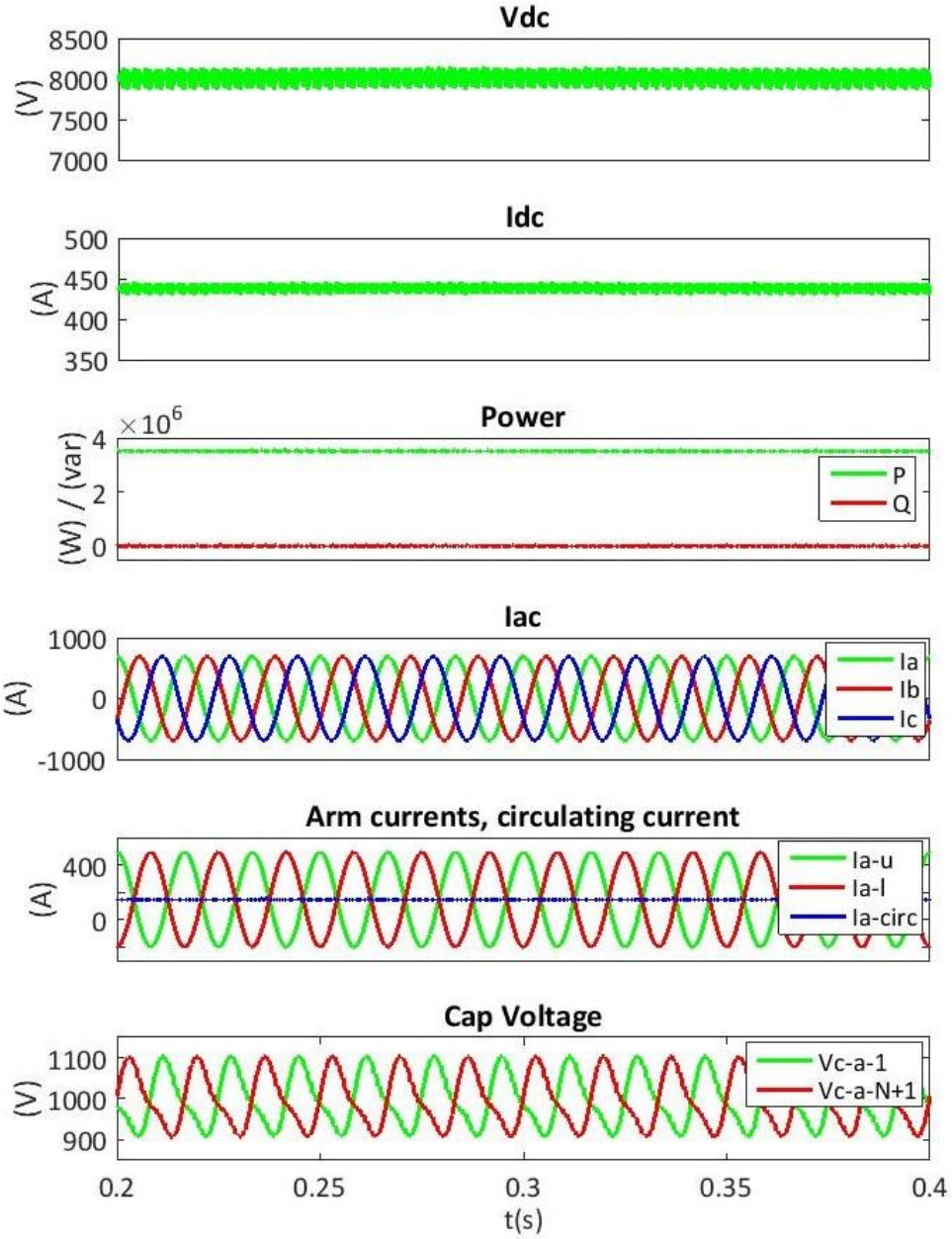


Fig. 2-7 Simulation results during the steady state of the normal operation

2.4 Summary

The operating principle and the closed-loop control of the MMC are introduced in this chapter. Then a simulation model is established to illustrate the operating principle and verify the performance of the closed-loop control. The simulation model is used as a platform for future study in this work.

Chapter 3. DC Fault Analysis and Control of Modular Multilevel Converter

The traditional Modular Multilevel Converter with Half-Bridge PEBBs is known to be vulnerable to a DC short circuit fault. However, the effect of the fault lacks exact analysis and description. Furthermore, in order to design a converter with the DC fault current limiting capability, a DC fault operation control is needed together with a selected PEBB topology.

3.1 DC Fault Current Analysis

The DC cable in the MVDC distribution system is likely to be exposed to a short circuit fault, which can lead to the formation of an arc. Different DC-arc models are reviewed in [39]. The behavior of an arc is highly variable. Under some circumstances, the arc resistance can be as low as 0.01 Ohm.

There are generally three types of sources of fault [40]. The first one is the capacitors between the DC bus. They discharge in a very short time and can contribute very high fault currents [40] [41]. However, the use of the MMC eliminates the need of DC filter capacitors, thus eliminating this risk. The second fault source is the DC sources. DC sources usually have built-in protections, including but not limited to: over-voltage protection and over-current protection. When a DC short circuit fault happens, the over-current protection is able to shut down the DC source and isolate it from the rest of the system, thus preventing the fault from developing. The third fault source is the AC sources, which contribute fault currents through the converter. This scenario is the focus of this work.

In the MMC operation, the switching frequency is much higher than the output frequency and the switching frequency is even equivalently increased by using the interleaved phase shifting PWM. As a result, an average model can be used to analyze the behavior of the converter [42] [43], as shown in Fig. 3-1. All the PEBBs in one arm can be combined together and considered as a controlled voltage source. The output voltage depends on the overall control commands. For example,

$$\begin{aligned} v_{a-u} &= \sum_{j=1}^{N}\left(\frac{V^*_{dc}}{2N}-\frac{v^*_{ac}}{N}+V^*_{Aj}+V^*_{Bj}\right)\frac{v_{cj}}{V^*_c} \approx \left(\frac{V^*_{dc}}{2N}-\frac{v^*_{ac}}{N}\right)\sum_{j=1}^{N}\frac{v_{cj}}{V^*_c} \approx \frac{V^*_{dc}}{2}-v^*_{ac} \\ v_{a-l} &= \sum_{j=N+1}^{2N}\left(\frac{V^*_{dc}}{2N}+\frac{v^*_{ac}}{N}+V^*_{Aj}+V^*_{Bj}\right)\frac{v_{cj}}{V^*_c} \approx \left(\frac{V^*_{dc}}{2N}+\frac{v^*_{ac}}{N}\right)\sum_{j=N+1}^{2N}\frac{v_{cj}}{V^*_c} \approx \frac{V^*_{dc}}{2}+v^*_{ac} \end{aligned} \tag{3-1}$$

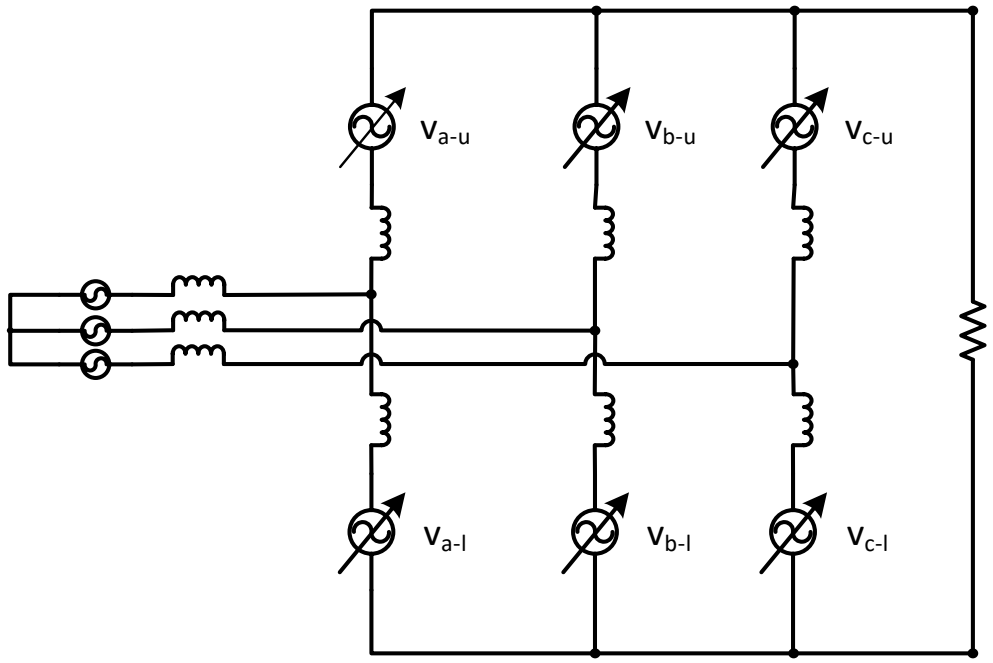


Fig. 3-1 Circuit configuration of a MMC using average model

In steady state, the values of the control commands (V^*_{Aj}, V^*_{Bj}) are much smaller than the DC, AC references ($\frac{V^*_{dc}}{2N}, \frac{v^*_{ac}}{N}$). The instant value of every capacitor voltage is close to the desired capacitor voltage so the output voltage of one controlled voltage source approximately

only includes the DC component and the fundamental frequency AC component. The converter arms have balance with both the DC and AC bus. However, when a pole-to-pole short circuit fault happens on the DC bus, the balance is interrupted.

Two types of current loops are considered and they are shown in Fig. 3-2 and Fig. 3-3. The type I involves two converter arms from the same phase leg as well as the DC bus, as shown in Fig. 3-2. The voltages and currents have the following relationship:

$$v_{dc} = v_{a-u} + v_{a-l} - \left(l\frac{di_{a-u}}{dt} + l\frac{di_{a-l}}{dt} \right) = v_{a-u} + v_{a-l} - 2l\frac{di_{a-circ}}{dt} \approx V^*_{dc} - 2l\frac{di_{a-circ}}{dt} \tag{3-2}$$

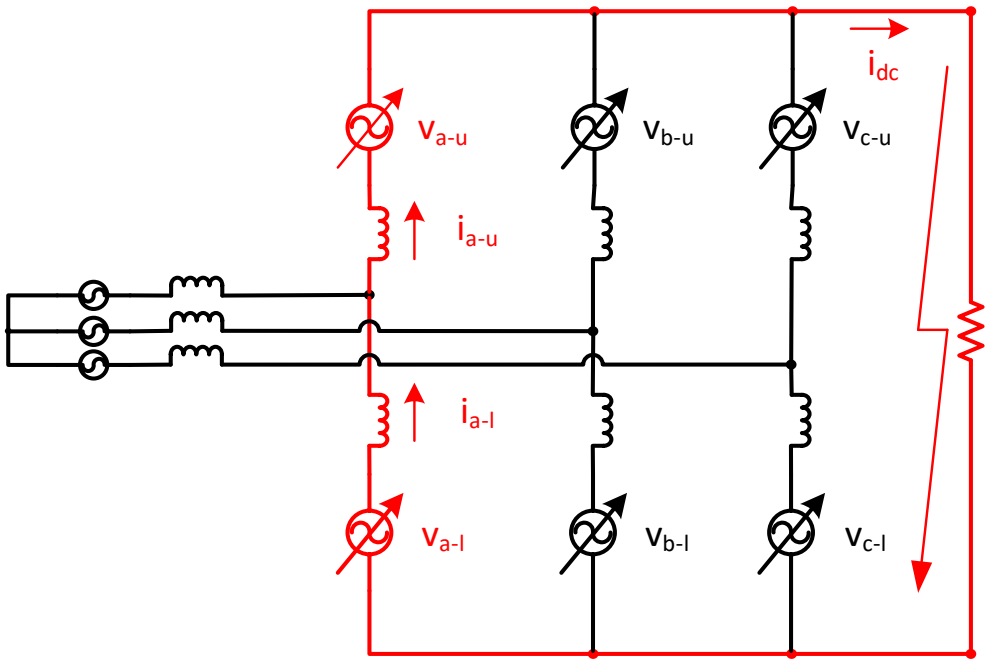


Fig. 3-2 A type I current loop of a MMC during DC short circuit fault

Where l is the inductance value for every arm inductor.

The DC bus voltage almost drops to zero after the short circuit fault happens. Then the DC voltage generated by the PEBBs causes an increase in the circulating currents. The DC load barely consume any energy. The energy stored in the capacitors flows to the arm inductors.

Since all the control loops only have limited bandwidth, they are not able to quickly respond after the fault happens. So in a short time period after fault happens,

$$\frac{di_{a-circ}}{dt} \approx \frac{V^*_{dc}}{2l} \tag{3-3}$$

The increase of the circulating current is almost linear and the increase rate only depends on the desired DC bus voltage and arm inductors.

Although the normal operation control is not designed for a fault condition, it may alleviate a little, mainly by the fourth PI controller, which is shown in Fig. 2-4. If the phase leg control command V^*_{Aj} is taken into account, the previous equation becomes:

$$v_{dc} = v_{a-u} + v_{a-l} - 2l\frac{di_{a-circ}}{dt} \approx V^*_{dc} + 2N \times V^*_{Aj} - 2l\frac{di_{a-circ}}{dt} \tag{3-4}$$

$$\frac{di_{a-circ}}{dt} \approx \frac{V^*_{dc} + 2N \times V^*_{Aj}}{2l} \tag{3-5}$$

In steady state, V^*_{Aj} is around zero. After the fault happens, the circulating current increases fast. The input of the fourth PI controller drops, so V^*_{Aj} will decrease. As a result, the increase rate of the circulating current is reduced. However, this response is much slower than the increase of the fault current. Furthermore, as each HB PEBB is only able to generate an instant voltage of v_C or 0, it is impossible to generate a negative voltage to decrease the fault current.

The above analysis is valid for all three phase legs. So:

$$\frac{di_{a-circ}}{dt} \approx \frac{di_{b-circ}}{dt} \approx \frac{di_{c-circ}}{dt} \approx \frac{V^*_{dc}}{2l} \tag{3-6}$$

$$\frac{d_{i_{dc}}}{dt} = \frac{di_{a-circ}}{dt} + \frac{di_{b-circ}}{dt} + \frac{di_{c-circ}}{dt} = \frac{3V^*_{dc}}{2l} \tag{3-7}$$

The type II current loop involves two converter upper (or lower) arms from different phase legs as well as the AC bus, as shown in Fig. 3-3. The voltages and currents have the following relationship:

$$v_{s-a} + v_{a-u} - v_{s-b} - v_{b-u} = l\frac{di_{a-u}}{dt} - l\frac{di_{b-u}}{dt} + L\frac{di_a}{dt} - L\frac{di_b}{dt} \tag{3-8}$$

Where v_{s-a} is the instant source voltage of phase A, v_{s-b} is the instant source voltage of phase B, L is the inductance value for every AC inductor.

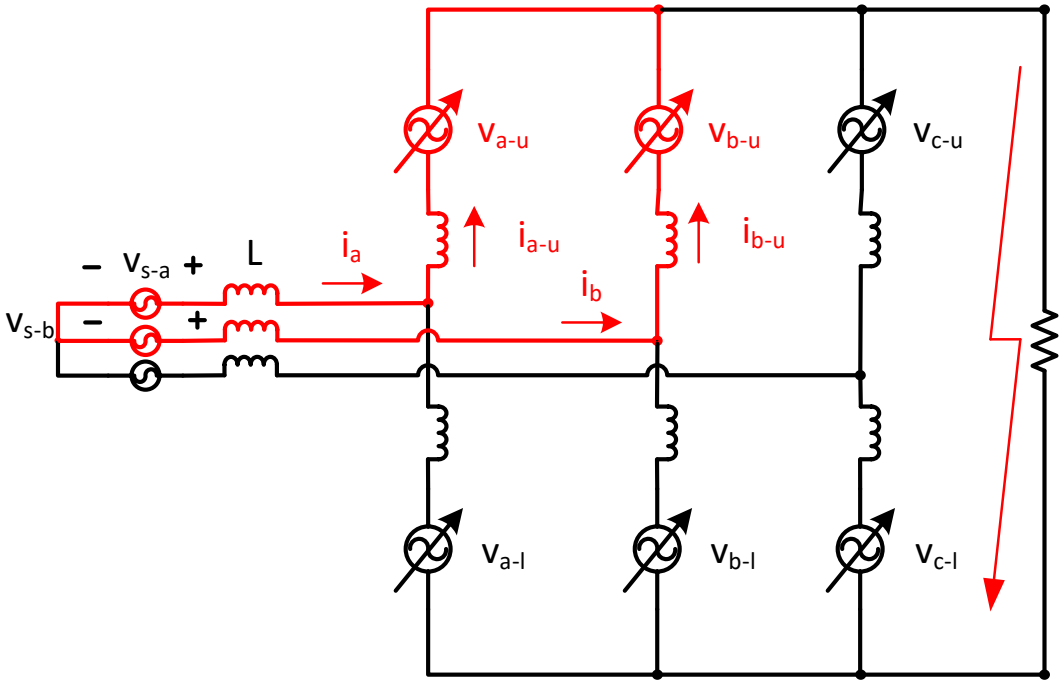


Fig. 3-3 A type II current loop of a MMC during DC short circuit fault

Use circulating currents and AC bus currents to represent arm currents.

$$v_{s-a} + v_{a-u} - v_{s-b} - v_{b-u} = l\frac{d\left(i_{a-circ} + \frac{i_a}{2}\right)}{dt} - l\frac{d\left(i_{b-circ} + \frac{i_b}{2}\right)}{dt} + L\frac{di_a}{dt} - L\frac{di_b}{dt} \tag{3-9}$$

Rearrange the above equation:

$$v_{s-a} + v_{a-u} - v_{s-b} - v_{b-u} = l\frac{di_{a-circ}}{dt} - l\frac{di_{b-circ}}{dt} + \left(L + \frac{l}{2}\right)\frac{di_a}{dt} - \left(L + \frac{l}{2}\right)\frac{di_b}{dt} \tag{3-10}$$

Similarly, between phase A and phase C:

$$v_{s-a}+v_{a-u}-v_{s-c}-v_{c-u}=l\frac{di_{a-circ}}{dt}-l\frac{di_{c-circ}}{dt}+\left(L+\frac{l}{2}\right)\frac{di_a}{dt}-\left(L+\frac{l}{2}\right)\frac{di_c}{dt} \tag{3-11}$$

Add Equation (3-10) and Equation (3-11) together and cancel three-phase component,

$$3v_{s-a}+\left(2v_{a-u}-v_{b-u}-v_{c-u}\right)=l\frac{d\left(2i_{a-circ}-i_{b-circ}-i_{c-circ}\right)}{dt}+3\left(L+\frac{l}{2}\right)\frac{di_a}{dt} \tag{3-12}$$

From the previous type I current loops, we have:

$$\begin{cases} l\dfrac{di_{a-circ}}{dt}=\dfrac{v_{a-u}+v_{a-l}-v_{dc}}{2} \\ l\dfrac{di_{b-circ}}{dt}=\dfrac{v_{b-u}+v_{b-l}-v_{dc}}{2} \\ l\dfrac{di_{c-circ}}{dt}=\dfrac{v_{c-u}+v_{c-l}-v_{dc}}{2} \end{cases} \tag{3-13}$$

Combine Equation (3-12) and Equation (3-13),

$$3v_{s-a}+\left(2v_{a-u}-v_{b-u}-v_{c-u}\right)=\left(\frac{2v_{a-u}+2v_{a-l}-v_{b-u}-v_{b-l}-v_{c-u}-v_{c-l}}{2}\right)+3\left(L+\frac{l}{2}\right)\frac{di_a}{dt} \tag{3-14}$$

$$3\left(L+\frac{l}{2}\right)\frac{di_a}{dt}=3v_{s-a}+\left(v_{a-u}-v_{a-l}\right)+\frac{1}{2}\left(-v_{b-u}+v_{b-l}-v_{c-u}+v_{c-l}\right) \tag{3-15}$$

If we just consider DC and AC reference for each controlled voltage source:

$$3\left(L+\frac{l}{2}\right)\frac{di_a}{dt}=3v_{s-a}-2v^{*}_{ac-a}+v^{*}_{ac-b}+v^{*}_{ac-c} \tag{3-16}$$

$$\left(L+\frac{l}{2}\right)\frac{di_a}{dt}=v_{s-a}-v^{*}_{ac-a} \tag{3-17}$$

$$\frac{di_a}{dt}=\frac{v_{s-a}-v^{*}_{ac-a}}{L+\frac{l}{2}} \tag{3-18}$$

The above analysis is valid for all three phases in a short time period after fault happens. As the DC bus voltage is not involved in the above equation, the short-circuit fault on the DC bus will not have a direct impact on the AC bus current. Even if we consider the phase leg

control command V^*_{Aj} for all three phase legs, it will be cancelled and Equation (3-10) is still valid.

When the normal operation control starts to react to the fault, the first PI controller, which is shown in Fig. 2-2, will generate a higher current reference as a result of the decreased DC voltage. Then the second PI controller will regulate the AC current to follow the reference, resulting in an increase in AC current.

In conclusion, in a short time after the DC fault happens, the DC current and all the arm currents increases fast and almost linearly but the AC current barely changes. The increase rate only depends on the desired DC bus voltage and arm inductors. After a while, the normal operation control slows down the increase rate of arm currents and DC current, but increases the AC current.

3.2 Module Topology Evaluation

As analyzed in the last section, during a DC short circuit fault, the PEBBs in the converter need to generate a negative voltage to decrease the fault current. Several newly proposed topologies [20], [44]-[49], as well as the original Half-Bridge topology, are summarized and evaluated in this section. At the cost of more switching devices and more losses, the MMCs with new PEBB topologies can interrupt the fault current by simply blocking all the active switching devices.

3.2.1 Half-Bridge Module

Fig. 3-4 shows the structure of a Half-Bridge (HB) module. It includes one capacitor and two complementary switching devices, which could be IGBTs, MOSFETs or other switching

devices. HB is the simplest topology among all possible choices. It also has the lowest conduction loss and switching loss.

However, the output voltage of the module can only be positive or zero. In other words, the module can only operate in two quadrants in terms of the output voltage-current relationship. As shown in last section, during the DC fault condition, a fault current through the PEBB will be negative using the direction defined in Fig. 3-4. For one PEBB, as the output voltage is either positive or zero, the capacitor is discharged or bypassed. In return, this PEBB will increase the fault current or have no impact. Therefore, the MMC with HB PEBB cannot limit or clear fault current. It has to rely on additional external components or equipment.

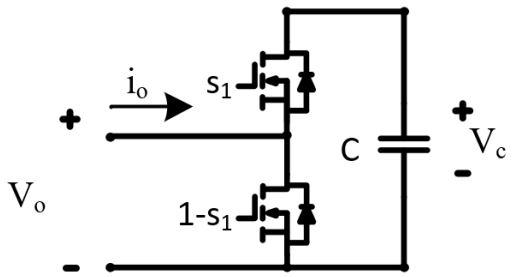


Fig. 3-4 Structure of a Half-Bridge module

3.2.2 Full-Bridge Module

Full-Bridge is a well-known alternative topology. The structure is shown in Fig. 3-5 (a). It includes one capacitor and two pairs of complementary switching devices. Each PEBB is capable of operating with either positive or negative voltage and current polarity. The four-quadrant operation provides maximum control flexibility.

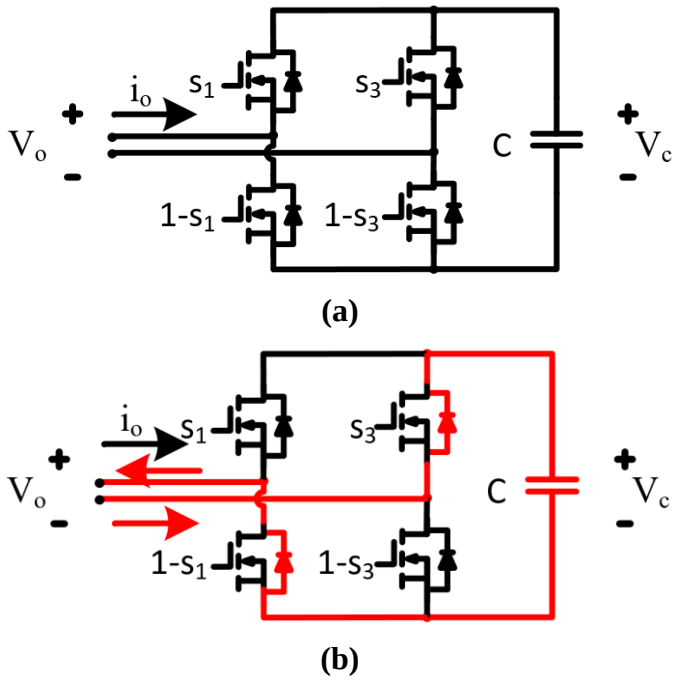


Fig. 3-5 Structure and fault current path of a Full-Bridge module

During the fault condition, after turning off all the active switching devices, no matter what direction the current flows in, the current will flow through diodes, charge the capacitor and in return be decreased by the capacitor. Therefore, the FB has the fault current blocking capability. The fault current path through the FB PEBB during a DC fault condition is shown in Fig. 3-5 (b). The output voltage of the module is negative in this case and the fault current can be decreased.

In order to validate that the MMC with FB PEBB is able to block fault current during the DC fault, one fault current loop is shown in Fig. 3-6. There are other current loops, but the analyses and conclusions are similar. For every PEBB in one loop, the output voltage is negative. As the AC source is the source of fault, in order to block the fault current, the following inequality should be satisfied:

$$v_{s-a} - v_{s-b} - 2 \times N \times v_c \leq 0 \tag{3-19}$$

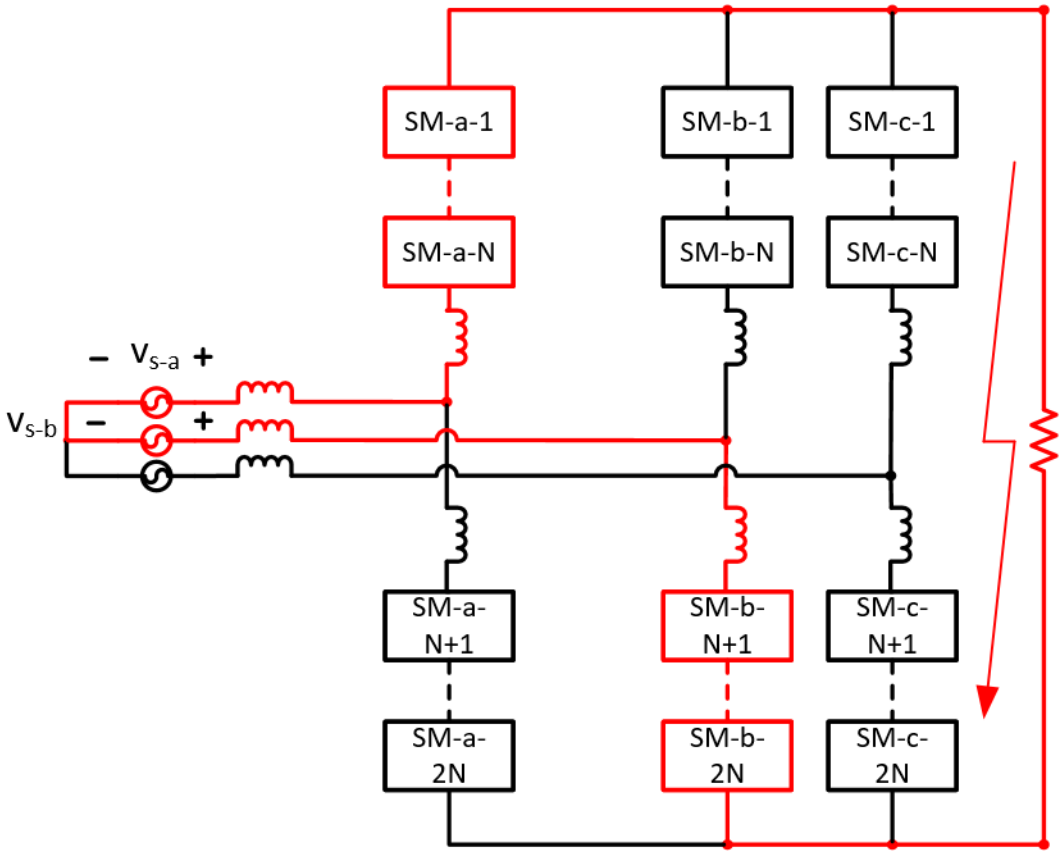


Fig. 3-6 A fault current loop of a Modular Multilevel Converter during DC fault

The left hand side of Equation (3-19) equals to:

$$v_{s-a} - v_{s-b} - 2 \times N \times v_c = \left(v_{s-a} - v_{s-b}\right) - 2 \times V_{dc} \tag{3-20}$$

Then Equation (3-19) is equivalent with the following inequality:

$$\left(v_{s-a} - v_{s-b}\right) - 2 \times V_{dc} \le \sqrt{2} V_{s-ab} - 2 \times V_{dc} \tag{3-21}$$

Where V_{s-ab} is the RMS value of line-to-line voltage of the AC source. Then,

$$\sqrt{2} V_{s-ab} - 2 \times V_{dc} = \sqrt{2} \times \sqrt{3} V_{ac} - 2 \times V_{dc} = \sqrt{2} \times \sqrt{3} \times \left(\frac{V_{dc}}{2\sqrt{2}} \times M \right) - 2 \times V_{dc} \tag{3-22}$$

As the modulation index M is always smaller than 1,

$$\sqrt{2} \times \sqrt{3} \times \left(\frac{V_{dc}}{2\sqrt{2}} \times M \right) - 2 \times V_{dc} < V_{dc} \times \left(\frac{\sqrt{3}}{2} - 2 \right) < 0 \tag{3-23}$$

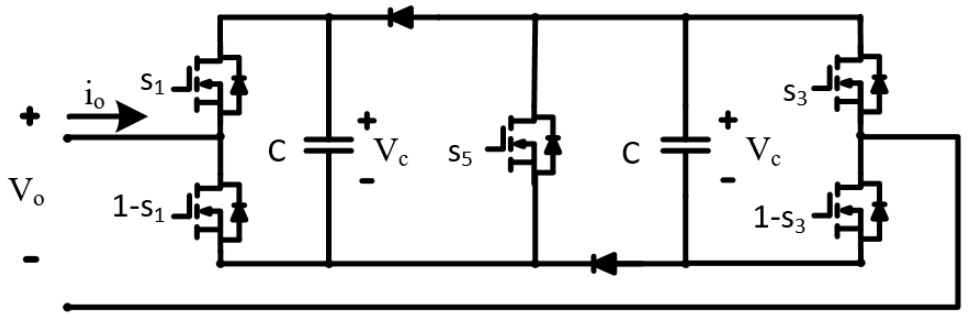
Therefore, the left hand side of Equation (3-19) will always be negative. When the arm current reaches zero, the diodes in PEBBs from the corresponding arm will no longer conduct. In this way, the fault current in the converter can be successfully blocked.

However, as the FB topology involves twice of the number of switching devices, the conduction loss will almost double. The switching loss will be similar or almost double depending on the modulation method. The exact increase of loss depends on the device characteristics, operation mode (rectifier or inverter), modulation index, etc. The loss comparison will be conducted in later section.

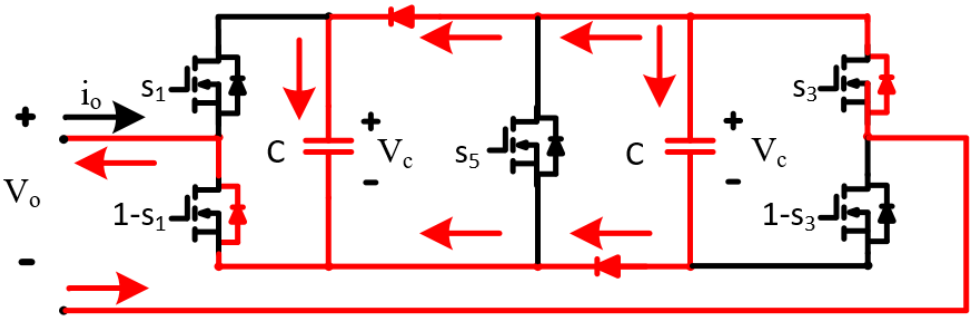
3.2.3 Clamp-Double Module

The structure of the Clamp-Double (CD) module is shown in Fig. 3-7 (a). Each module includes two capacitors, five controlled switching devices (two pairs of complementary switches and one extra switch) and two diodes. During normal operation, switch s_5 is constantly on, and then the whole module is equivalent with two HBs in series. There are three switches conducting at the same time for every two capacitors, which is one less compared to four switches for every two capacitors using the FB topology. The Clamp-Double module has less loss than the FB. Actually, it has the lowest loss among all topologies with fault-handling capability.

During the fault condition, by turning off all five active switches, the fault current flows through the diodes to achieve a negative output voltage. The fault current path through the Clamp-Double PEBB during the DC fault condition is shown in Fig. 3-7 (b).



(a)



(b)

Fig. 3-7 Structure and fault current path of a Clamp-Double module

MMC with Clamp-Double PEBB is also able to block the DC fault current by turning off all active switches. It is validated through a similar analysis, which is used in the FB case. With the same variables, Equation (3-19) is still applicable except that there are $\frac{N}{2}$ PEBBs in each arm since every CD module has two capacitors. The left hand side equals to:

$$v_{s-a} - v_{s-b} - 2 \times \frac{N}{2} \times v_c = \left(v_{s-a} - v_{s-b}\right) - V_{dc} \tag{3-24}$$

$$\left(v_{s-a} - v_{s-b}\right) - V_{dc} \le \sqrt{2} V_{s-ab} - V_{dc} \tag{3-25}$$

$$\sqrt{2} V_{s-ab} - V_{dc} = \sqrt{2} \times \sqrt{3} V_{s-a} - V_{dc} = \sqrt{2} \times \sqrt{3} \times \left(\frac{V_{dc}}{2} \times M\right) - V_{dc} \tag{3-26}$$

$$\sqrt{2} \times \sqrt{3} \times \left(\frac{V_{dc}}{2} \times M\right) - V_{dc} < V_{dc} \times \left(\frac{\sqrt{3}}{2} - 1\right) < 0 \tag{3-27}$$

Therefore, the fault current can be successfully blocked. However, the Clamp-Double PEBB can only generate negative output voltage when the current is also negative. The three-

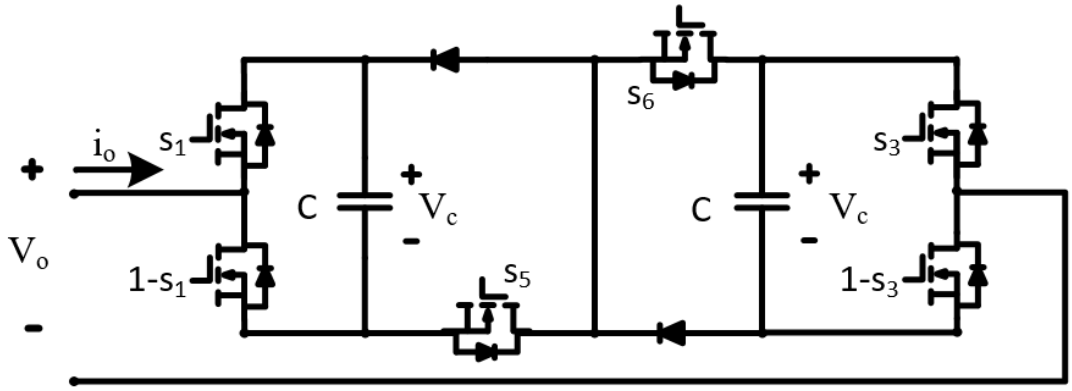
quadrant operation can only provide limited control flexibility. For some applications, for example STATOM operation, MMCs with CD PEBBs need extra control effort to achieve the same goal [50].

In addition, in each Clamp-Double PEBB, two capacitors are in parallel during the fault condition, as shown in Fig. 3-7 (b). Then the magnitude of the negative output voltage is only half of the maximum positive output voltage. This will lead to slower decrease in the fault current.

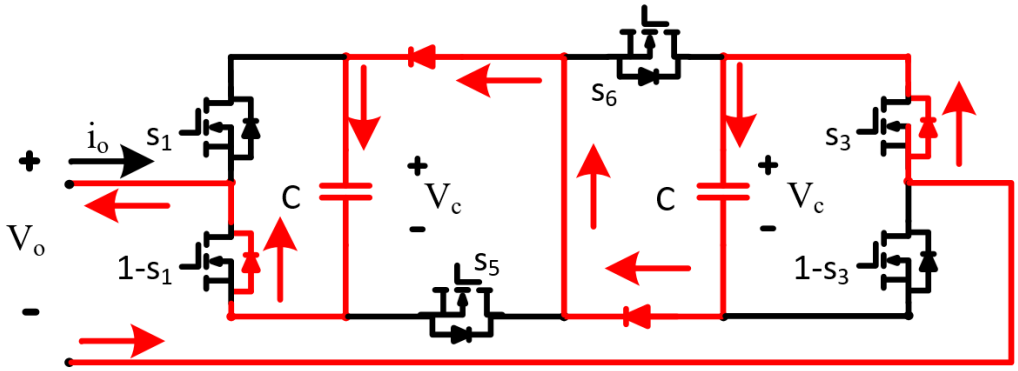
3.2.4 Three-Level Module

The structure of the Three-Level (TL) module is shown in Fig. 3-8 (a). It is similar to the Clamp-Double module except that switch s_5 in the middle is split into two switches s_5 and s_6. Both switches are constantly on during normal operation and turned off during the fault condition. The normal operation of the TL module is similar to the CD module.

With the use of one more switch, after turning off all active switches, two capacitors are in series during the fault condition. The fault current path through the Three-Level PEBB during the DC fault condition is shown in Fig. 3-8 (b). The magnitude of the negative voltage is the same as the maximum positive output voltage. The fault-current clearing behavior of the MMC with Three-Level PEBBs is similar to the MMC with FB PEBBs.



(a)



(b)

Fig. 3-8 Structure and fault current path of a Three-Level module

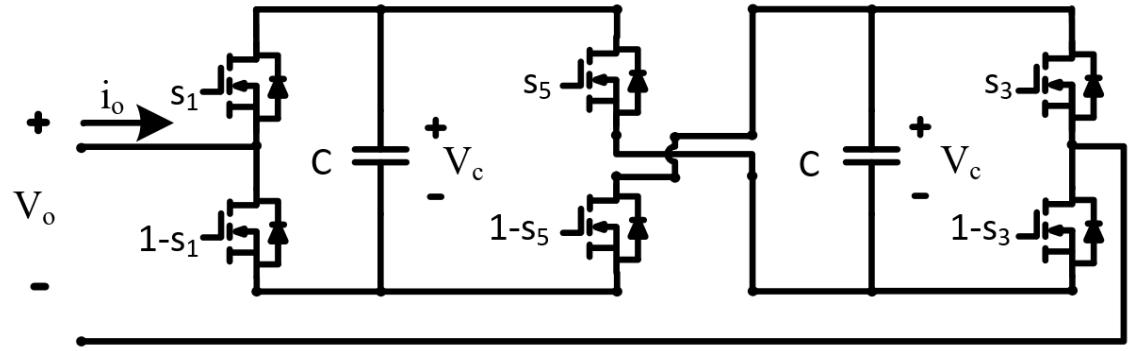
However, the Three-Level module is also limited to a three-quadrant operation. With four switches conducting at the same time for every two capacitors during normal operation, it has a similar conduction loss as the FB, which is more than the Clamp-Double module.

3.2.5 Cross-Connected Module

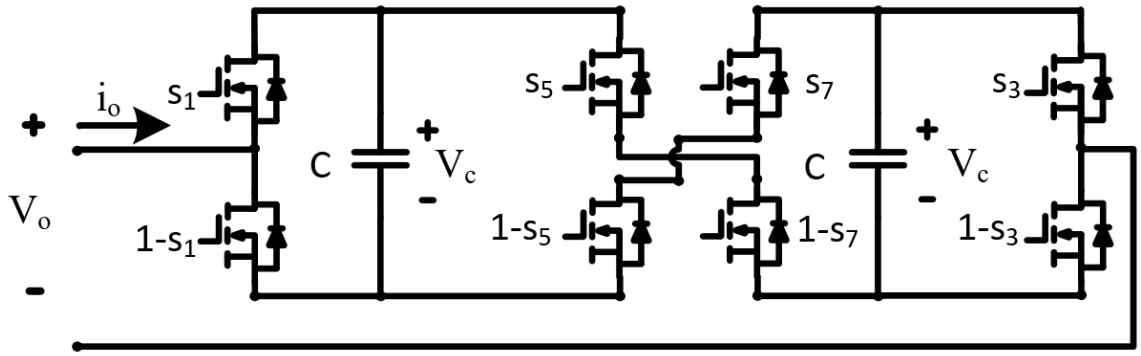
The structure of two kinds of Cross-Connected (CC) modules are shown in Fig. 3-9 (a) and (b) respectively. In (a), by controlling switch s_5 and the complementary switch, two HBs are connected in series or reversely connected in series. This provides a four-quadrant operation and the full ability to generate a negative output voltage.

However, when s_5 (or $1-s_5$) is on, the voltage stress on the other switch may be twice that of the capacitor voltage. To solve this, different switching devices may be used or two

devices may be connected in series. The latter is shown in Fig. 3-9 (b). In this case, the number of switches is similar with that of the FB, and the loss will be similar. This topology does not provide any advantage over the FB but will involve a series connection of switching devices, which could be challenging.



(a)



(b)

Fig. 3-9 Structure two Cross-Connected modules

3.2.6 Loss Comparison

The instant conduction loss of a semiconductor can be calculated using Equation (3-28) and Equation (3-29) for simplicity [51], [52]:

$$v_F = V_0 + R_0 \times i_f \tag{3-28}$$

$$p_c = v_F \times i_f \tag{3-29}$$

Where v_F is the instant forward voltage drop on the semiconductor, the forward voltage V_0 and the on state resistance R_0 are two constants, i_f is the instant current flowing

through the semiconductor and p_c is the instant conduction loss. Note that other loss models can be used.

The switching energy loss of a semiconductor in one switching cycle can be calculated using Equation (3-30) [51]-[53].

$$W_s = \frac{W_{on} + W_{off}}{V_{ref} I_{ref}} v_{CE} i_f \tag{3-30}$$

Where W_s is the switching energy loss in one switching cycle, W_{on} and W_{off} are the turn-on and turn-off energy loss at reference voltage V_{ref} and current I_{ref} , v_{CE} is the device voltage at the switching instant.

Then the average conduction loss and the average switching loss of a semiconductor can be calculated within one fundamental output time period.

$$P_c = \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} p_c(\tau) d\tau = \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} \left(V_0 i_f(\tau) + R_0 \times i_f(\tau)^2 \right) d\tau \tag{3-31}$$

$$P_s = f_s \times \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} \frac{W_{on} + W_{off}}{V_{ref} I_{ref}} v_{CE}(\tau) i_f(\tau) d\tau = \frac{f_s \omega \left(W_{on} + W_{off} \right)}{2\pi V_{ref} I_{ref}} \int_0^{\frac{2\pi}{\omega}} v_{CE}(\tau) i_f(\tau) d\tau \tag{3-32}$$

Where P_c is the average conduction loss, ω is the output angular frequency, P_s is the average switching loss, f_s is the switching frequency.

For every pair of complementary switches, it is only possible for current to flow through one MOSFET (or IGBT) or one anti-parallel diode, at any instant depending on the switch command and the current direction. The semiconductors with current flowing through in a Half-Bridge PEBB can be summarized in Tab. 3-1 using the circuit topology and definitions in Fig. 3-4, and assuming perfect complementary gate signals within each half-bridge module.

Tab. 3-1 Semiconductors with current flowing through

		Current Direction	
		Positive	Negative
s_1	1	D1	T1
	0	T2	D2

T_i is the MOSFET (or IGBT) of switch s_i, D_i is the diode of switch s_i, $i = 1,2$.

Since the equivalent switching frequency is much higher than the output frequency, it can be assumed that the arm current does not change within one switching cycle. The average conduction loss and switching loss of one semiconductor can then be calculated using the duty ratio (instead of gate signals), the arm current (instead of device current) and the capacitor voltage. Using the MOSFET (or IGBT) of switch s_1 within the PEBB located in the upper arm of phase A as an example, the losses are:

$$P_{c-a-u-T1} = \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} d_{a-u-s1}(\tau)\left(V_0 i_{a-u}(\tau) + R_0 \times i_{a-u}(\tau)^2\right) H\left(i_{a-u}(\tau)\right) d\tau \tag{3-33}$$

$$P_{s-a-u-T1} = \frac{f_s \omega\left(W_{on} + W_{off}\right)}{2\pi V_{ref} I_{ref}} \int_0^{\frac{2\pi}{\omega}} v_{CE}(\tau) i_{a-u}(\tau) H\left(i_{a-u}(\tau)\right) d\tau \tag{3-34}$$

Where d_{a-u-s1} is the duty ratio of switch s_1, i_{a-u} is the current flowing through the upper arm of phase A into the positive DC bus and $H(\ )$ is the Heaviside step function, which has an output of 0 when input is smaller than zero and has an output of 1 otherwise.

Therefore, the losses of every semiconductor can be calculated based on device parameters and converter operation variables. Use the same specifications of converter as described in Tab. 2-1 to estimate the losses of the converter. A 1.7 kV, 800 A IGBT device from ABB [54] is

selected as the switching device based the voltage and current rating. The loss characteristics of the selected device is summarized in Tab. 3-2.

Tab. 3-2 ABB 5SND 0800M170100 IGBT module loss characteristics

	IGBT	Diode
Forward voltage	1.25 V	1.19 V
On state resistance	1.25 mΩ	0.58 mΩ
Turn-on energy loss	160 mJ	0
Turn-off energy loss	220 mJ	150 mJ
Reference Voltage	900 V	900 V
Reference Current	800 A	800 A

For simplicity, only consider the DC component and the fundamental frequency component in both the duty ratio and the arm current; and also ignore the ripple on the PEBB capacitor voltage, the losses can be easily calculated by hand. The losses of one HB PEBB are estimated and presented in Tab. 3-3.

Tab. 3-3 Calculated losses of one Half-Bridge PEBB

Semiconductor	Conduction Loss	Switching Loss	Total Loss
T_1	66.22 W	101.47 W	167.69 W
D_1	52.01 W	9.67 W	61.68 W
T_2	8.33 W	24.50 W	32.83 W
D_2	215.46 W	40.05 W	255.51 W
Total	342.02 W	175.70 W	517.72 W

An alternative and more accurate way to calculate the losses of one PEBB is to use simulation to get the converter operation variables. In this way, all the harmonics, either caused by the power stage or the control signals, are included. The established simulation model,

which is described in Section 2.3, is used. Gate signals, arm current and device voltage are recorded for calculation. The results are shown in Tab. 3-4. The difference between the calculated losses and the simulated losses is actually negligible.

Tab. 3-4 Simulated losses of one Half-Bridge PEBB

Semiconductor	Conduction Loss	Switching Loss	Total Loss
T_1	66.42 W	101.16 W	167.58 W
D_1	52.12 W	9.66 W	61.78 W
T_2	8.71 W	24.84 W	33.55 W
D_2	216.23 W	39.46 W	255.69 W
Total	343.48 W	175.12 W	518.60 W

Simulation models may be time consuming to build especially when a large number of PEBBs are employed in the converter, or different PEBB topologies need to be compared. Using the first loss estimation method is easier as it does not require a simulation model. If an available simulation model exists, then using the second method is better as it is more accurate and requires easier calculation.

In this study, the second method is used to compare the losses of MMCs built with different PEBB topologies. The total device loss of converter is shown in Fig. 3-10.

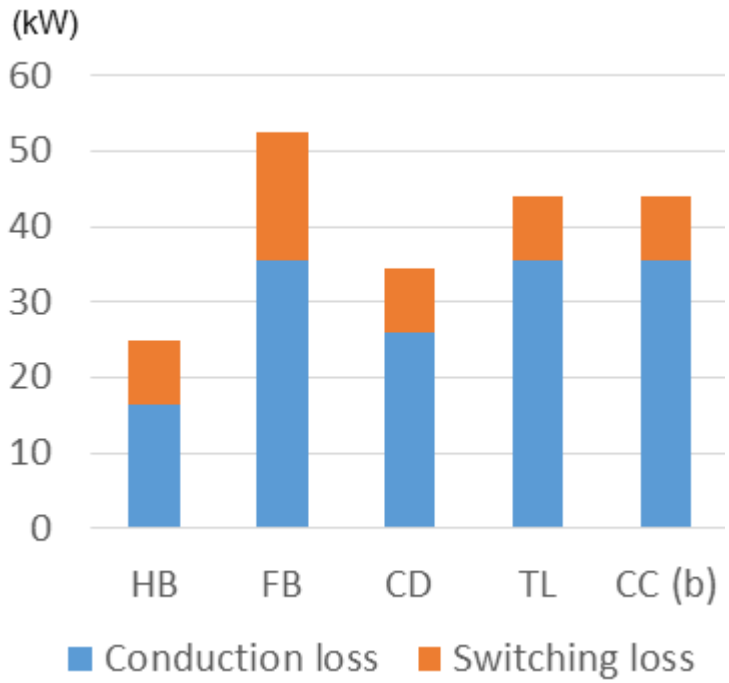


Fig. 3-10 Total device loss of MMCs with different topologies

In the above table, the HB has the lowest conduction loss and the CD has the second lowest conduction loss, about 58% more than the HB; the FB, the TL and the CC (b) have the highest conduction loss, about 116% more than the HB. The HB also has the lowest conduction loss, as well as the CD, the TL and the CC (b); the FB has higher switching loss, about 102% more than the HB. The FB can also have a similar switching loss if other modulation methods are used. The comparison is shown in later section.

3.2.7 Summary

In addition to the aforementioned topologies, there are other possible topologies such as the Flying Capacitor (FC) module, the Neutral Point Clamped (NPC) module and so on. They are not discussed in detail in this study because of the similarity with the above modules in terms of operation quadrants, negative output voltage magnitude and loss. Moreover, a

symmetric topology is preferred to avoid the difficulty of balancing multiple capacitors, thus some asymmetric topologies are not considered.

Another possible solution is to use hybrid PEBB topologies [20], [47]-[49], which means that two or more topologies are used in one converter to achieve the fault current blocking capability and minimize the total loss. However, the balancing among capacitors from different PEBBs can be challenging in practice. So a hybrid MMC is not considered.

The characteristics of the candidate topologies are summarized in Tab. 3-5.

Tab. 3-5 Comparison of candidate PEBB topologies

PEBB Topology		HB	FB	CD	TL	CC	
						(a)	(b)
No. of operation quadrants		2	4	3	3	4	4
DC fault blocking capability		×	√	√	√	√	√
Doubled voltage stress		No	No	No	No	Yes	No
Serial Connection of switches		No	No	No	No	No	Yes
Estimated loss compared to HB (per unit)	**Conduction loss**	1.00	2.16	1.58	2.16	-	2.16
	Switching loss	1.00	2.02	1.00	1.00	-	1.00
	Total loss	1.00	2.11	1.38	1.77		1.77

The essential characteristic when selecting a PEBB topology is ability to generate a controlled positive or zero output voltage to achieve the basic functionality of the MMC, and the DC fault blocking capability. A four-quadrant operation is highly preferred. Then low loss is preferred. The applicability should also be considered.

Based on the above guideline, the HB is the first to be eliminated because of its lack of DC fault handling capability. Then the FB, the CC (a) and the CC (b) are the remaining candidates since they can operate in four quadrants. However, the CC (a) involves a doubled voltage stress

on switch, and the CC (b) involves a series connection of switching device. Therefore, FB is selected as PEBB topology in this study.

3.3 Proposed DC Fault Operation Control

As discussed in the previous two sections, the MMC with traditional HB PEBB topology and the normal operation control is vulnerable to a DC short circuit fault. Fault currents rise quickly in the converter arms, potentially destroying the components in the converter, such as switching devices, inductors and capacitors. By employing PEBB topologies with DC fault blocking capability and turning off all the active switches, the MMC is able to clear the fault current in an uncontrolled way. Although handling the fault current is indeed the highest priority requirement during the fault, the main disadvantage of turning all the active switches is that converter cannot have any power exchange during the fault [55]. As a result, all the capacitor voltages will drop because of loss, which is not favorable when re-energizing the DC bus. Furthermore, it is desired that the rest of the system and the AC grid see as little impact as possible when clearing the fault currents and after the fault is isolated from the system.

Several control strategies are proposed to clear the fault and achieve the fault ride-through capability of the converter. In [56], the Half-Bridge topology is used. Even with the proposed control, the converter is only able to slow down the developing of the fault current instead of limiting or clearing the fault current. In [57], the PEBB capacitor voltages are not regulated well after the fault happens. [58] and [59] both utilize the current control of the normal operation to achieve the fault current control during the DC fault condition. There is a tradeoff

when designing current control because fault current control should have a bandwidth as high as possible but normal current cannot have a too high bandwidth. When the current control performs well during normal operation, the fault current clearing transient is much slower than the possible fastest transient.

Therefore, a DC fault operation control is proposed to achieve fast fault current clearing and PEBB capacitor voltage regulation. Together with the selected FB PEBB topology, the converter is able to continuously operate under the fault condition. The proposed control has a similar structure to the normal operation control, thus is easy to be implemented in addition to the normal operation control.

3.3.1 Fault Detection

As analyzed in Section 3.1, the increase of the DC current, as well as the circulating currents, is the key effect after the DC short-circuit fault happens, so this phenomenon can be used as the fault detection method. The DC current and circulating currents of three phases can be calculated based on the sensed arm currents. By using the DC current or circulating currents instead of directly using arm currents, the AC component in the arm currents will not have any influence during the fault detection process. In this study, the DC current is used for fault detection because the circulating currents may include a second order harmonic during the transient response (converter start-up or load change), which may falsely trigger the DC fault operation control.

3.3.2 Three-phase Current Loop Control

The scheme of the three-phase current loop control is shown in Fig. 3-11.

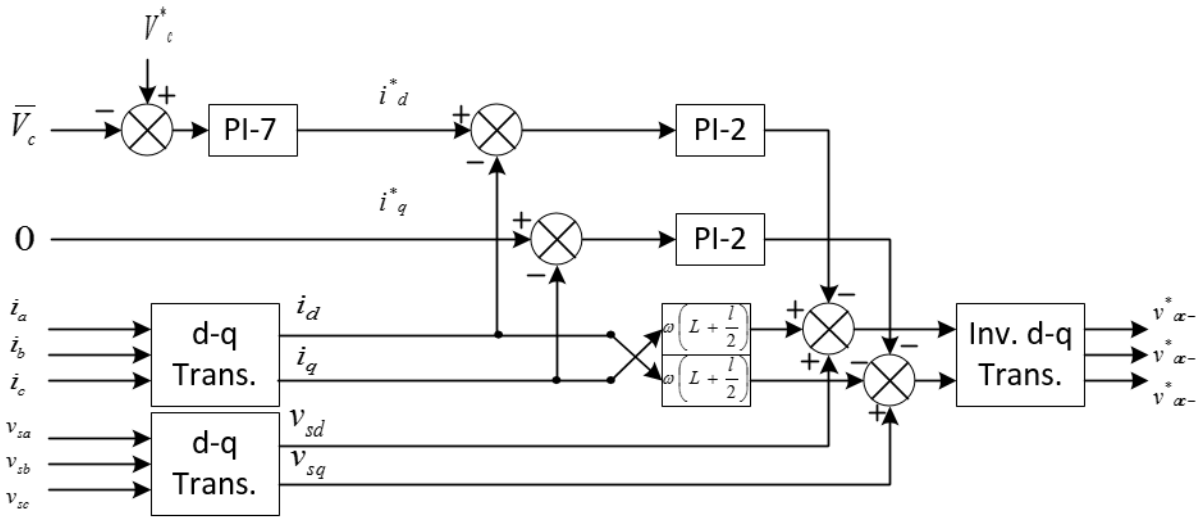


Fig. 3-11 Three-phase current loop control of fault operation

With a DC fault condition, the DC bus voltage is forced to be zero and it is impossible to regulate the DC voltage anymore. In addition, the DC load does not consume any power. However, the AC current can be controlled so that the three-phase AC source provide adequate active power to regulate the capacitor voltages. The error between the average value of all sensed capacitor voltages and the desired capacitor voltage is accumulated by a PI controller to give the d axis current reference. When the average capacitor voltage is lower than desired, the d axis current reference increases, controlling move active power transferring from the AC source to the converter.

Reactive power control is still fully functional. In this case, the desired reactive power is set to be zero.

3.3.3 Phase Leg Control

The scheme of phase leg control is shown in Fig. 3-12. From the fault current analysis, it is observed that phase leg control can reduce the developing rate of fault current. Therefore, it is modified to clear the fault current.

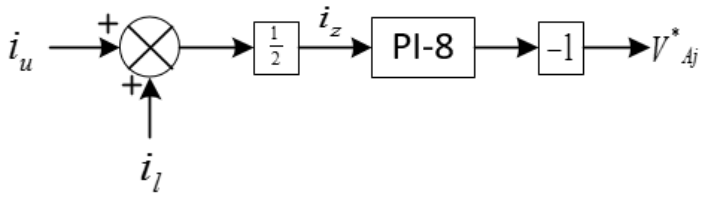


Fig. 3-12 Phase leg control of fault operation

Since the three-phase current loop of fault operation already includes average voltage control, the previous average voltage control at phase leg is removed. Then the reference for the circulating current is just zero. The circulating current suppression is also removed as the fault current control is already regulating the circulating current to be zero, and the second order harmonic in circulating current is not severe during fault operation as a result of little power being transferred.

A PI controller with a high proportional gain and a low integral gain is used to generate the control command to clear the fault current. The high proportional gain provides fast clearing of the fault current, the low integral gain provides steady state regulation and avoids oscillation during transient response. The fast transient behavior will be discussed in later section.

3.3.4 Individual PEBB Control

The scheme of the individual PEBB control is shown in Fig. 3-13 and Fig. 3-14.

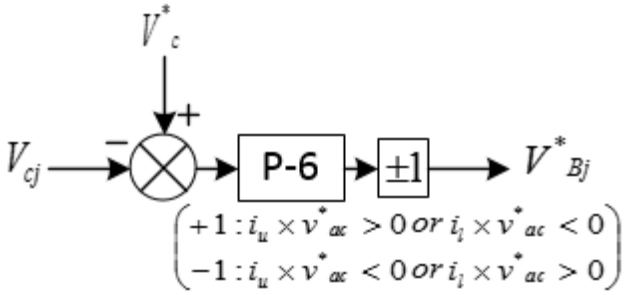


Fig. 3-13 Individual PEBB control of fault operation

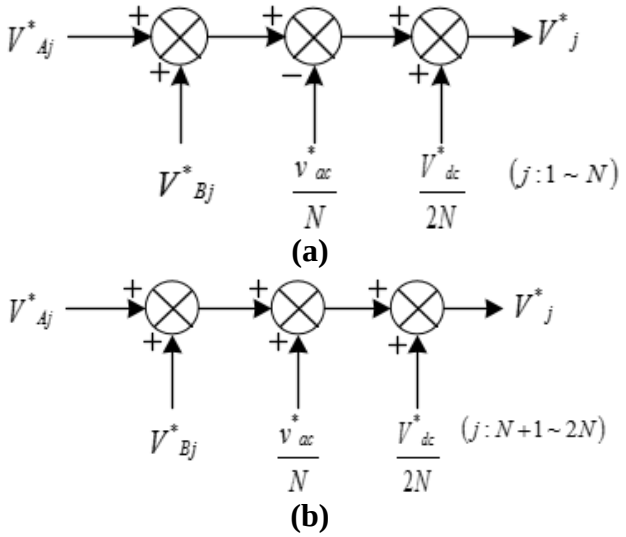


Fig. 3-14 Overall control command of fault operation

The individual voltage control is similar to normal operation except that the instant charge/discharge state depends on both the PEBB output voltage and the arm current.

The DC reference is removed from the overall control command as the DC bus has a short-circuit fault. In this way, the converter arm has a new balance with the zero DC bus, preventing feeding the fault current.

Take one PEBB in the upper arm of phase A as an example. The capacitor is reversely connected into the arm if:

$$V^*_j < 0 \tag{3-35}$$

Then the capacitor is being charged if:

$$\begin{cases} V^*_j > 0 \\ i_{a-u} < 0 \end{cases} or \begin{cases} V^*_j < 0 \\ i_{a-u} > 0 \end{cases} \tag{3-36}$$

The overall control command equals to:

$$V^*_j = V^*_{Aj} + V^*_{Bj} - \frac{v^*_{ac-a}}{N} \approx -\frac{v^*_{ac-a}}{N} \tag{3-37}$$

Then the capacitor is being charged if:

$$\begin{cases} v^*_{ac-a} < 0 \\ i_{a-u} < 0 \end{cases} or \begin{cases} v^*_{ac-a} < 0 \\ i_{a-u} > 0 \end{cases} \tag{3-38}$$

Equivalently, the capacitor is being charged if:

$$i_{a-u} \times v^*_{ac-a} > 0 \tag{3-39}$$

Similarly, the polarity of command for all the conditions can be determined.

Based on the above control schemes, during the fault current clearing time, the voltages and currents have the following relationship:

$$v_{dc} = v_{a-u} + v_{a-l} - 2l\frac{di_{a-circ}}{dt} \tag{3-40}$$

Where,

$$v_{a-u} \approx \sum_{j=1}^{N} \frac{\left(-\frac{v^*_{ac}}{N} + V^*_{Aj}\right)}{V^*_c} v_{cj} = \sum_{j=1}^{N} \frac{\left(-\frac{v^*_{ac}}{N} - K_{p8} i_{a-circ} - K_{i8}\int i_{a-circ}\right)}{V^*_c} v_{cj} \tag{3-41}$$

$$v_{a-l} \approx \sum_{j=N+1}^{2N} \frac{\left(\frac{v^*_{ac}}{N} + V^*_{Aj}\right)}{V^*_c} v_{cj} = \sum_{j=N+1}^{2N} \frac{\left(\frac{v^*_{ac}}{N} - K_{p8} i_{a-circ} - K_{i8}\int i_{a-circ}\right)}{V^*_c} v_{cj} \tag{3-42}$$

By using a high gain, when fault current is big, we can achieve:

$$\frac{\left(-\frac{v^*_{ac}}{N} - K_{p8} i_{a-circ} - K_{i8}\int i_{a-circ}\right)}{V^*_c} < -1 \tag{3-43}$$

$$\frac{\left(\frac{v^*_{ac}}{N} - K_{p8} i_{a-circ} - K_{i8}\int i_{a-circ}\right)}{V^*_c} < -1 \tag{3-44}$$

Then every capacitor is consistently reversely connected in the arm. The relationship among voltages and currents becomes:

$$0 = -2N \times v_c - 2l\frac{di_{a-circ}}{dt} \tag{3-45}$$

$$\frac{di_{a-circ}}{dt} = -\frac{N \times v_c}{l} \approx -\frac{V^*_{dc}}{l} \tag{3-46}$$

$$\frac{d_{i_{dc}}}{dt} = \frac{di_{a-circ}}{dt} + \frac{di_{b-circ}}{dt} + \frac{di_{c-circ}}{dt} \approx -\frac{3V^*_{dc}}{l} \tag{3-47}$$

Compared to Equation (3-3) and (3-5), the fault current is decreasing instead of increasing. The decreasing rate of fault current is twice that of the increasing rate before this control is implemented. This is also the fastest decrease rate the converter can achieve no matter what PEBB topology is used or what control method is used because all the capacitors are reversely connected in the arm to clear the fault current. This rate is valid as long as the calculated desired duty ratio is smaller than -1.

3.4 Simulation Verification

To verify the fault current behavior and the performance of the proposed DC fault operation control, a simulation model is established in "MATLAB/Simulink". The circuit configuration and the specifications are similar to the model described in Section 2.3 except that each block is a FB PEBB. The additional control parameters are summarized in Tab. 3-6.

Tab. 3-6 Additional control parameters used in simulation study

Controller	Parameters
PI-7	$K_p = 2, K_i = 10$
PI-8	$K_p = 20, K_i = 0.1$

The short-circuit fault on the DC bus is added at $0.4s$ and cleared after $0.2s$. It is modeled by a small resistor (0.01 Ohm). Fault is detected by monitoring the DC current. The threshold is set to be twice that of the DC current value in steady state of normal operation.

The proposed fault operation control is activated as soon as fault is detected. Other detection delay or action delay is not considered.

The simulation results during fault current developing and clearing ($0.3996s \sim 0.4010s$) are shown in Fig. 3-15. After fault happens, DC bus voltage drops to zero immediately. Then DC current increases almost linearly at first but increases slower later. In the first $50\mu s$, it increases from $437.9A$ to $572.8A$. The increase rate of the DC current during fault in simulation is approximately:

$$\frac{572.8-437.9}{50\times10^{-6}}=2.7\times10^{6}A/s \tag{3-48}$$

Based on (3-7), the calculated increase rate is:

$$\frac{3V^{*}_{dc}}{2l}=\frac{3\times8\times10^{3}}{2\times4\times10^{-3}}=3.0\times10^{6}A/s \tag{3-49}$$

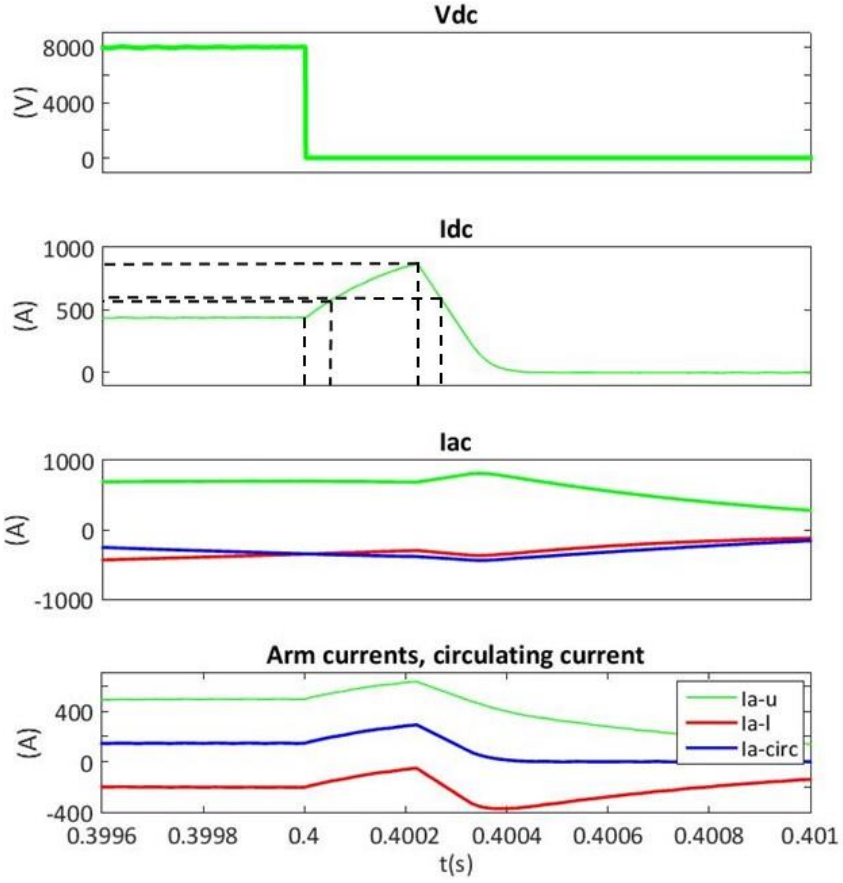


Fig. 3-15 Simulation results of fault current developing and clearing

The values from calculation and simulation are quite similar, indicating the effectiveness of the analysis. In simulation, all the controllers updates continuously, resulting in faster response. The effect of digital delay will be discussed in later section.

The DC current reaches the threshold in around $222\mu s$. Then the DC current begins to drop. In the first $50\mu s$, it decreases from $873.5A$ to $576.0A$. The decrease rate of DC current during fault in simulation is approximately:

$$\frac{873.5-576.0}{50\times10^{-6}}=5.9\times10^{6}A/s \tag{3-50}$$

Based on the previous analysis, the calculated decrease rate is:

$$\frac{3V^{*}_{dc}}{l}=\frac{3\times8\times10^{3}}{4\times10^{-3}}=6.0\times10^{6}A/s \tag{3-51}$$

The values from calculation and simulation are quite similar. The fault current decreases almost linearly until it becomes small enough. It eventually drops to zero in around $180\mu s$.

In the simulation waveforms, there is no sudden change on the three-phase AC current. Therefore, arm currents only include sudden change from the DC component. Upper arm current, lower arm current and circulating current are almost parallel with each other when increasing.

The simulation results of the whole process ($0.3s\sim0.8s$) are shown in Fig. 3-16. The DC fault happens at $0.4s$. Fault current develops for about $186\mu s$ before fault operation control is activated and is cleared in about another $180\mu s$. All the PEBB capacitor voltages will increase after the fault current developing and clearing period because capacitors absorb all the energy in inductors and energy from the AC source. The converter continuously operates in new steady state under the fault condition until the fault is removed. All the currents, as well

as active and reactive power, are around zero. All the capacitor voltages are regulated around the reference value. After the fault is removed, The control switches back to normal operation control and the load is re-energized.

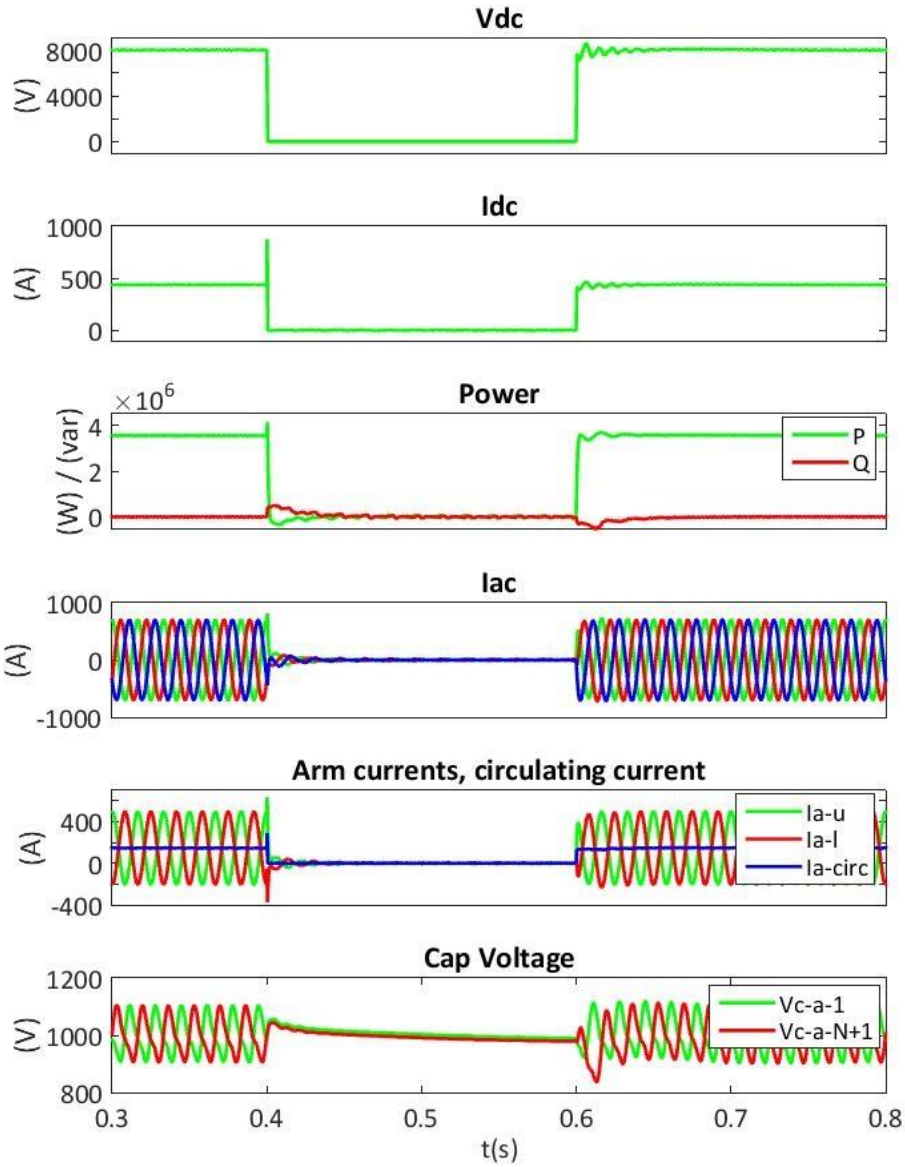


Fig. 3-16 Simulation results of fault clearing and system re-energizing

3.5 Summary

The DC fault current behavior is first analyzed in this chapter. As a direct effect of the fault, the DC current and all the arm currents increase fast and almost linearly but the AC current

barely changes. Then different PEBB topologies are compared. Full-Bridge is selected because of its fault handling capability, full control flexibility, and symmetric configuration despite the highest loss. Based on the fault current analysis and a selected PEBB topology, a DC fault operation control is proposed. The fault current behavior and the performance of the proposed control are verified by simulation.

Chapter 4. Design and Test of a SiC-Based MMC Prototype

A scaled-down three-phase Modular Multilevel Converter prototype is designed and built to experimentally verify the fault current behavior and the proposed DC fault operation control.

4.1 Converter Configuration and Specifications

Fig. 4-1 and Tab. 4-1 show the circuit configuration and the specifications of the converter respectively. With minor modifications, it is able to operate as either a rectifier or an inverter. The converter has a power rating of 45 kVA and a dc bus voltage rating of 1 kV, and comprises a single 1 kV Full-Bridge PEBB per arm (2 per phase-leg, 6 total) using SiC MOSFET power modules. This configuration retains the main properties featured by the MMC, such as the distributed energy storage. Thanks to the use of fast SiC devices, the converter still has a high equivalent switching frequency without requiring multiple series-connected modules. Therefore, despite of the reduced number of PEBBs, the converter's passive components do not suffer from harsher requirements. Then with the 1.7 kV SiC MOSFETs, a 1 kV DC bus can be generated, which is under consideration and use in commercial and military marine applications. Higher voltages can be easily achieved by increasing the number of PEBBs per arm.

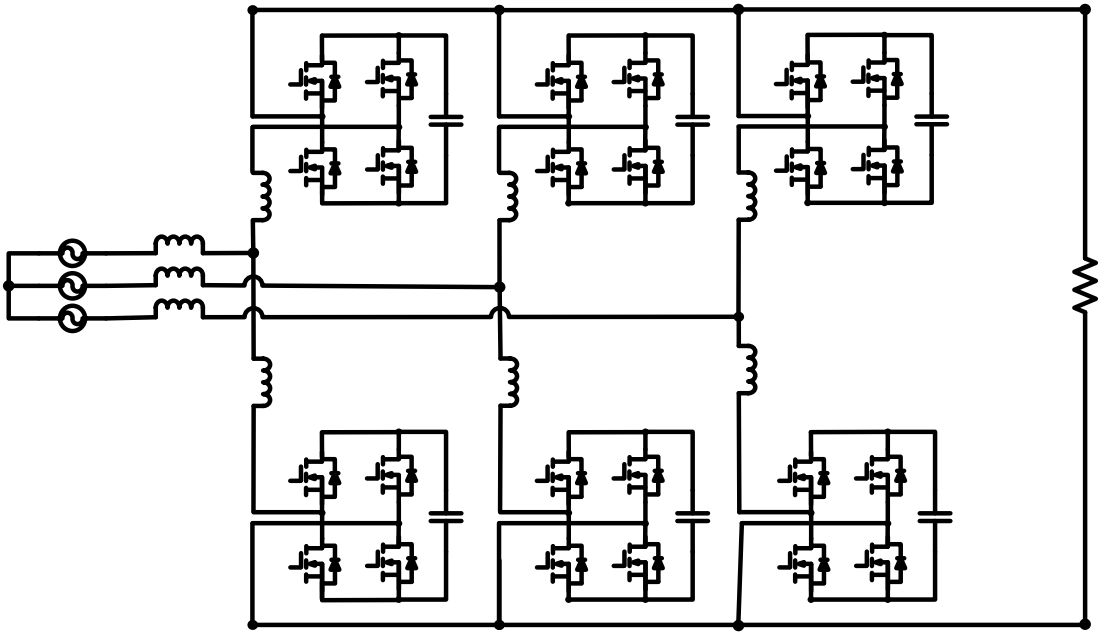


Fig. 4-1 Configuration of the converter prototype

Tab. 4-1 Specifications of the converter prototype

Converter specifications		**Component specifications**	
Active power	45 kW	Load Resistance	22 Ω
Reactive power	0	Capacitor voltage	1 kV
AC line RMS voltage	480 kV	Capacitor voltage ripple	200 V
DC bus voltage	1 kV	PEBB capacitance	210 μF
Number of PEBBs in one arm	1	Arm inductance	1 mH
Line frequency	60 Hz	AC inductance	1.5 mH
Switching frequency	100 kHz		

4.2 Design of PEBBs

The design of the converter prototype can follow a modular design procedure because of the modular configuration of a MMC. Each PEBB has a dc bus voltage rating of 1 kV. Fig. 4-2 depicts the PEBB and it includes SiC MOSFET modules with gate-driver units, a capacitor

bank, arm inductors, a planar dc bus, decoupling capacitors, a current sensor and a heat sink. The detailed design description of the PEBB is provided in following subsections.

This part of work is done in collaboration with Ms. Niloofar Rashidi Mehrabadi.

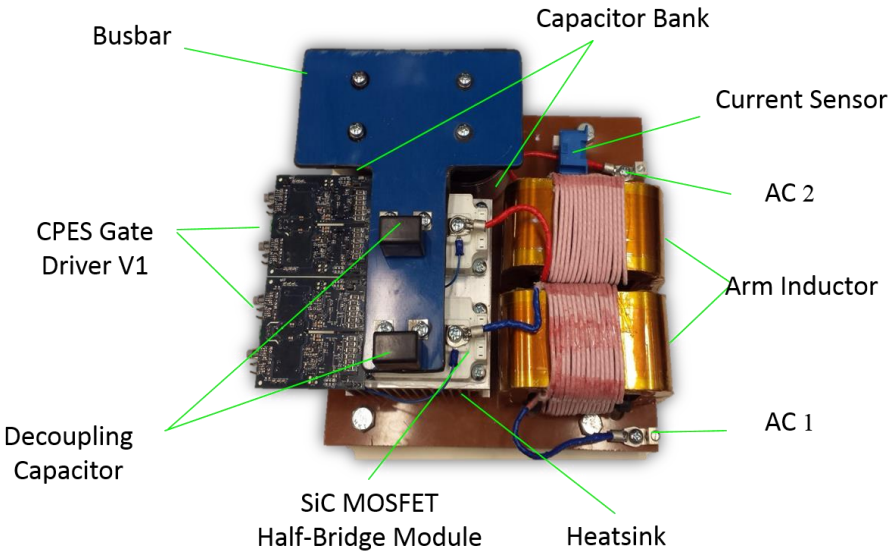


Fig. 4-2 Hardware prototype of a Full-Bridge PEBB

4.2.1 Switching Device and Gate Driver

Currently, Si IGBTs are largely used in the MMC [18], in accordance with its low switching frequency requirements and relatively low power density. The latter is one of the main shortcomings besides the lack of DC fault current limiting capability. However, the low power density has been recently overcome by developing new high frequency and switching-cycle modulation and control schemes [60]. The new schemes allow the MMC circuit to profit from a high switching frequency operation and achieve a high power density. Wide-bandgap (WBG) devices, such as SiC, have become a viable option to fully exploit the advantages of the MMC for MVDC systems. Benefitting from a tenfold higher blocking voltage, as well as a 10–100 times higher switching frequency, and higher operating temperatures (>200 °C) when

compared to Si counterparts, converters will have significant gains in terms of power density [61].

The CAS300M17BM2 SiC MOSFET half-bridge module from Cree [62] is selected as the switching device considering the voltage and current ratings, as well as the availability of the products. The module has a blocking voltage of 1.7 kV, a continuous current of 225 A at 90 °C and a junction temperature range of -40 °C to 150°C. It also has an ultra-low loss and is capable of high-frequency operation.

The CPES gate driver [63] has been especially designed for this half bridge module by fellow graduate students before this work. In this work, a similar design is used and 12 gate driver boards are assembled and tested for this converter prototype. The gate driver has a Miller-clamp circuit to attenuate cross-talk effect, Desaturation for short circuit protection and it is designed to achieve a high dv/dt immunity (>50 V/ns).

4.2.2 Capacitor Bank

The capacitor voltage ripple is important to assure the safe operation of a power electronic device and the functionality of the converter. Equation (4-1) is used to calculate the minimum required capacitance to achieve the desired voltage ripple [64]:

$$C_{\min} = \frac{P}{3\omega N M V_c \Delta V \cos\varphi} \sqrt{\left(1 - \left(\frac{M\cos\varphi}{2}\right)^2\right)^3} \qquad (4\text{-}1)$$

Where P is the active power of the converter, ω is the output angular frequency, N is the number of PEBBs per arm, M is the modulation index, V_c is the rated capacitor voltage, ΔV is the voltage ripple on the capacitor and $\cos\varphi$ is the power factor of the converter. Using (4-1), the minimum required capacitance is calculated to be 198 uF. Two

Cornell Dubilier Electronics (CDE) 420 uF capacitors rated at 900 V dc and 75 A are connected in series to meet the requirements.

4.2.3 Arm Inductor

The role of the arm inductors in the MMC is to suppress any high frequency components of the arm currents caused by the differences between the DC bus voltage and the total voltages generated by all the PEBBs in one phase leg. There are resonance frequencies associated with intrinsic even order harmonics of the circulating current [28], [65]. These second and fourth resonance frequencies are calculated using (2) and (3).

$$\omega_{2nd} = \sqrt{\frac{3N + 2M^2 N}{48lC}} \tag{4-2}$$

$$\omega_{4th} = \sqrt{\frac{15N + 8M^2 N}{960lC}} \tag{4-3}$$

Where N is the number of PEBBs per arm, M is the modulation index, l is the arm inductance, and C is the PEBB capacitance. The two corresponding inductance values to the resonance points are 0.77 mH and 3.3 mH respectively. Hence, the arm inductance value needs to be far away those values. It is set to be 1.0 mH. As shown in Fig. 4-2, the arm inductance is distributed between two ac terminals for common-mode considerations.

An amorphous core AMCC 630 is used to build the inductor due to its high saturation flux density (1.56 T). Three AC inductors are also built. The AC inductance is 1.5 mH. The turn number and air gap length of the arm inductor are set to be 38 and 5.4 mm; the turn number and air gap length of the AC inductor are set to be 40 and 4.3 mm, based on the calculation of Ms. Rashidi.

4.2.4 DC Planar Busbar

A DC planar busbar is designed, built and verified by Ms. Rashidi for each PEBB. It is used to connect the capacitors in series to form a capacitor bank and to connect the capacitor bank and the switching devices. The structure of the designed busbar is shown in Fig. 4-3, where copper is the conductor material, Kapton tape is the insulation material, garolite provides mechanical strength, and Hysol epoxy is used to bond the different layers together.

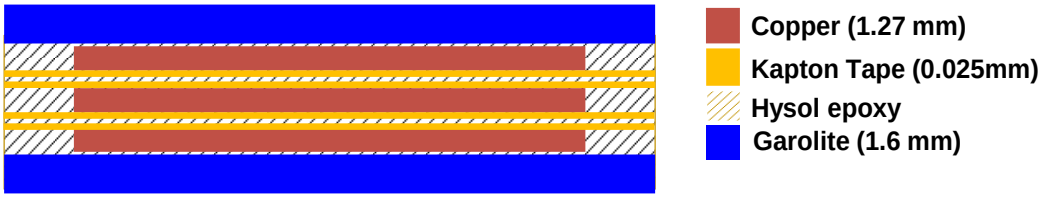


Fig. 4-3 Structure of the busbar layer

A small stray inductance is very important because of the high-speed switching transients. A decoupling capacitor is connected at the terminal of switching device to further decrease the interconnection inductance. The final loop inductance from Q3D simulation is 11.91 nH while the value from measurement is 12.82 nH.

All of the built busbars undergo a Hipot test to verify the insulation. The busbars can withstand 6 kV from the positive layer to the middle layer and from the middle layer to the negative layer. Then the busbar should be able to withstand at least 12 kV from the positive layer to the negative layer, which is much more than enough.

4.2.5 Thermal Design

It is extremely important to ensure that all the components in the converter operate within their rated temperature range. For the designed converter prototype, most of the losses come from switching devices, including conduction loss and switching loss.

The losses can be estimated using the same method as used in Section 3.2.6. The loss characteristics of the selected SiC MOSFET half-bridge module is summarized in Tab. 4-2.

Tab. 4-2 Cree CAS300M17BM2 module loss characteristics

	MOSFET	Diode
Forward voltage	0	0.925 V
On state resistance	6.67 mΩ	2.50 mΩ
Turn-on energy loss	13.0 mJ	0
Turn-off energy loss	10.0 mJ	0
Reference Voltage	900 V	N/A
Reference Current	300 A	N/A

The calculated losses and the simulated losses of one Full-Bridge PEBB are presented in Tab. 4-3 and Tab. 4-4.

Tab. 4-3 Calculated losses of one Full-Bridge PEBB

Semiconductor	Conduction Loss	Switching Loss	Total Loss
T_1	3.40 W	175.74 W	179.14 W
D_1	5.04 W	0	5.04 W
T_2	0.05 W	47.97 W	48.02 W
D_2	8.21 W	0	8.21 W
T_3	0.05 W	47.97 W	48.02 W
D_3	8.21 W	0	8.21 W
T_4	3.40 W	175.74 W	179.14 W
D_4	5.04 W	0	5.04 W
Total	33.39 W	447.43 W	480.82 W

Tab. 4-4 Simulated losses of one Full-Bridge PEBB

Semiconductor	Conduction Loss	Switching Loss	Total Loss
T_1	3.41 W	175.13 W	178.54 W
D_1	5.14 W	0	5.14 W
T_2	0.05 W	49.14 W	49.19 W
D_2	8.22 W	0	8.22 W
T_3	0.05 W	49.14 W	49.19 W
D_3	8.22 W	0	8.22 W
T_4	3.41 W	175.13 W	178.54 W
D_4	5.14 W	0	5.14 W
Total	33.65 W	448.55 W	482.20 W

The difference between the calculated losses and the simulated losses is negligible. It can also be observed that the total loss is dominated by the switching loss of the MOSFETs.

Using the data from Tab. 4-4 and the datasheet [62], the max temperature increase between junction to case is:

$$\Delta T_{JC-\max} = R_{thJCM} \times P_{M-\max} = 11.96°C \tag{4-4}$$

Where R_{thJCM} is the thermal resistance from junction to case for MOSFET and $P_{M-\max}$ is the maximum total loss for one of the MOSFET.

As shown in Fig. 4-2, the two SiC MOSFET half-bridge modules sit on a heat sink, with thermal grease in between and screws to suppress them for good heat dissipation. Wakefield-vette 511-6U heat sink [66] is used based on thermal resistance and size. An Orion OA 109AP-11-1 fan [67] is used to provide enough air flow to achieve forced convection for the heat sink. The temperature increase between case and environment is:

$$\Delta T_{CE} = R_{thCEH} \times P_{total} = 32.79°C \tag{4-5}$$

Where R_{thCEH} is the thermal resistance from case to environment for heat sink with forced convection, P_{total} is the total loss for one Full-Bridge PEBB.

Then the max junction temperature for the device when the converter is operating at full power is:

$$T_{J-\max} = T_{room} + \Delta T_{CE} + \Delta T_{JC-\max} = 69.75°C \quad (4\text{-}6)$$

Where $T_{room} = 25°C$ is the environment (room) temperature. The max junction temperature is much lower than the max rated junction temperature ($150°C$).

4.3 Control Realization and Considerations

To implement the normal operation control introduced in Section 2.2 and the DC fault operation control proposed in Section 3.3, certain control hardware is used. Additional control considerations are discussed to make the converter prototype functional and protected.

4.3.1 Control Hardware and Structure

16 sensing feedback channels are used, including 6 PEBB capacitor voltages, 6 arm currents, 3 AC bus voltages, 1 DC bus voltage. Then circulating currents, AC currents, average PEBB capacitor voltages (of 3 phases and of all PEBBs) can be calculated. After control calculation, 24 gate signals need to be generated for 6 Full-Bridge PEBBs and sent to gate drivers.

The LEM LF 205-S/SP3 current sensor [68] is used to sense the arm currents and can be observed in Fig. 4-2. The LEM LV 25-P/SP5 voltage sensor [69] is used to sense all the voltages and can be observed in Fig. 4-4. A sensor board is used to gather all the sensing signals, as shown in Fig. 4-4.

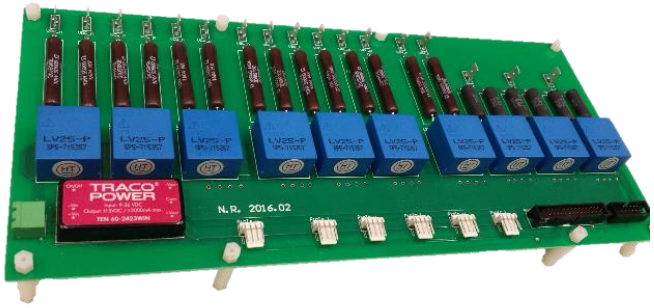


Fig. 4-4 The sensor board

The sensing information is transferred through a ribbon cable to a central controller. The central controller, as shown in Fig. 4-5, features Texas Instruments TMS320C28343 Delfino Microcontroller (MCU) [70] and Lattice LCMX02-4000HC Complex Programmable Logic Device (CPLD) [71]. The 200 MHz controller, sitting on Texas Instruments Delfino C28343 controlCARD [72], is used to process most of the control calculation tasks. As the controlCARD only provides 12 channels of Analog-to-Digital Conversion (ADC), an ADC board is used to perform the other 4 channels of ADC, as shown in Fig. 4-6. Analog Devices AD7924 [73] executes 4-channel, 12-bit ADCs and serially transfers the results to MCU through multichannel buffered serial ports (McBSPs).

The MCU has 9 PWM modules and is able to generate 18 channels of PWM signals. In the converter prototype, 12 channels of gate signals are generated by MCU and transferred to CPLD. Then the CPLD generates the 12 complementary gate signals with 400 ns deadtime. 24 gate signals are grouped in such a way that one group of 4 gate signals are intended for the switching devices for one PEBB. Six groups of gate signals are sent to the PEBBs through six optical fiber interface boards. The optical fiber interface board, as shown in Fig. 4-7, is able to receive electric or optical signals, convert to the other form and send it out.

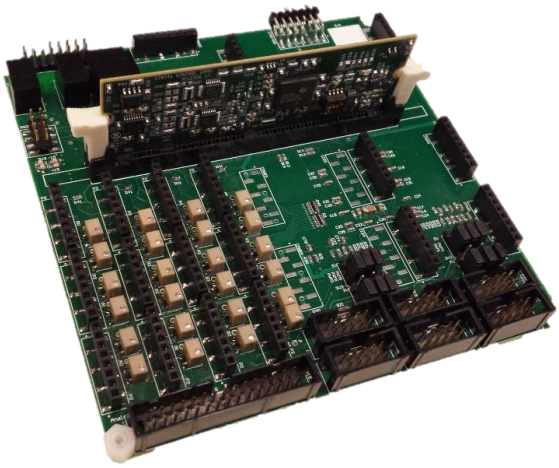


Fig. 4-5 The central controller

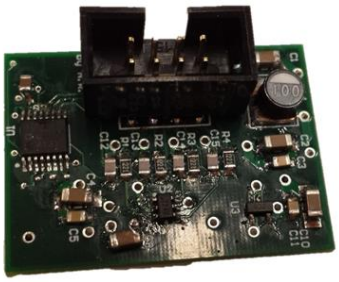


Fig. 4-6 The ADC board

Fig. 4-7 The optical fiber interface board

At the same time, the MCU is connected to a computer through an Ethernet cable. A compatible graphic user interface (GUI) is used on the computer to send commands and read the converter operation status. The control structure is shown in Fig. 4-8.

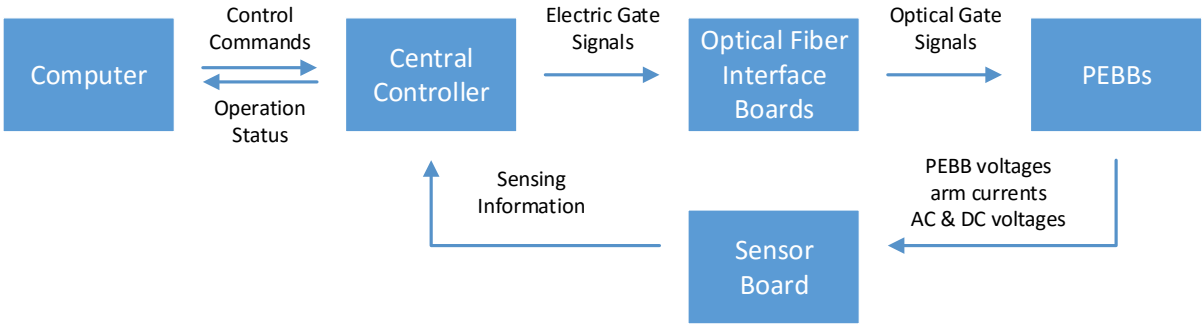


Fig. 4-8 The control structure

Some previous board design work by fellow graduate students in CPES was made use in this work. Then one central controller, one ADC board, six optical fiber interface board and one sensor board are assembled with the help of Ms. Rashidi. After that, all the boards are tested.

4.3.2 Pre-charge and Discharge

The PEBB capacitors need to be pre-charged to start normal operation and discharged after each test. In both processes, each PEBB is inserted into the arm or bypassed by controlling gate signals [17], [74]. The complete configuration of an inverter system is shown in Fig. 4-9.

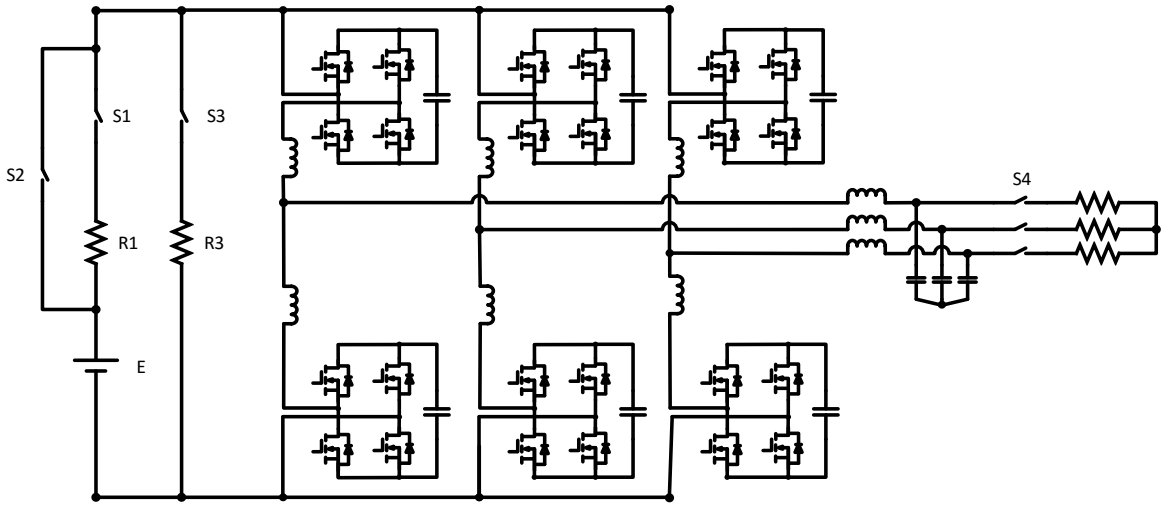


Fig. 4-9 Configuration of an inverter system

The DC voltage source serves as both the source during pre-charge and the source during normal inverter operation. R1 and R3 are two 2kΩ resistors, limiting pre-charge current and discharge current respectively. Solid State Relays (SSRs) are used to change connection in the system. S1 and S3 are two Crydom SSC 1000-25-12 DC SSRs [75], S2 is two parallel-connected DC SSRs to provide enough current capability, S4 is a Crydom HS053-D53TP50D 3-phase AC SSR [76]. Three 1.5 μF capacitors are connected prior to the AC SSR so that when S4 is turned off, capacitors can absorb the remaining energy of the AC inductors.

The operation sequence and actions of an inverter test is described as the following. At first, all relays are off. Then, the DC source is turned on and voltage is increased to the desired value (1 kV). A pre-charge command is sent from the computer to MCU in order to start the pre-charge process. S1 is turned on to connect the DC source with the PEBBs. All the PEBBs in the three upper arms are first pre-charged while the PEBBs in the lower arms are bypassed at the same time. When the voltages of all top PEBBs reach a threshold, the top PEBBs are bypassed and the bottom PEBBs are inserted into the arm to be pre-charged. When the voltages of all PEBBs in the bottom arms reach a threshold, the bottom PEBBs are bypassed and the top PEBBs are pre-charged again. Top PEBBs and bottom PEBBs need to be charged alternately and continuously because every PEBB voltage drops as a result of loss when not being charged.

The inverter operation will start if an inverter command is sent from the computer and all PEBBs are well charged. Relay S2 is turned on to bypass the pre-charge resistor and relay S4 is turned on to connect the AC load.

When a discharge command is sent from the computer, all the switching devices are first turned off, then all the currents in the system are soon cleared. After a pre-set delay (for example, 1 s), S2 and S4 are turned off and S3 is turned on to start discharge process. This is similar to the pre-charge process except that the top and bottom PEBBs are discharged only once respectively.

The complete configuration of a rectifier system is shown in Fig. 4-10.

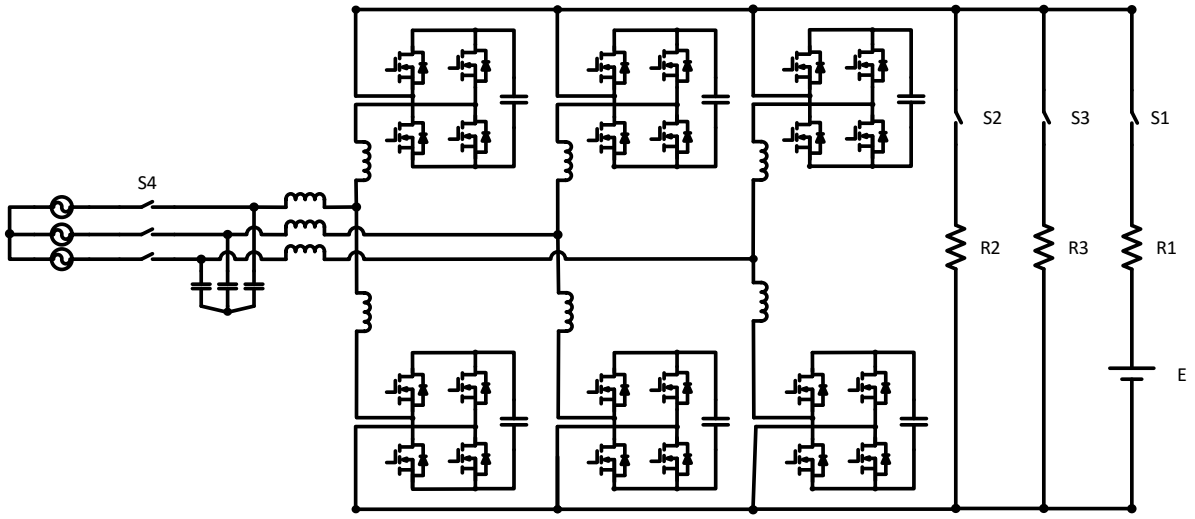


Fig. 4-10 Configuration of a rectifier system

The DC voltage source serves as only the source during the pre-charge and the AC voltage source is the source during normal rectifier operation. R1 and R3 are the same pre-charge and discharge resistors, R2 is a 22.2 Ω DC load. The same relays are used except S2 is used to connect the DC load.

The operation sequence and actions of a rectifier test is described as the following. At first, all relays are off. Then both the DC source and AC source are turned on and voltages are increased to the desired values (1 kV and 277 Vrms). A pre-charge command is sent from the

computer to MCU to start pre-charge process. The pre-charge process is the same as in the inverter test. Meanwhile, AC bus voltages are sensed and a Phase-Locked Loop (PLL) is enabled to acquire the frequency and phase information of the AC bus voltage.

The rectifier operation will start if a rectifier command is sent from the computer, all PEBBs are well charged and the PLL is synchronized. Relay S1 is turned off to disconnect the DC source, relay S4 is turned on to connect the AC source and relay S2 is turned on to connect the DC load.

When a discharge command is sent from the computer, all the switching devices are turned off first. After a pre-set delay, S2 and S4 are turned off, S3 is turned on to start the discharge process. This is the same as in the inverter test.

4.3.3 Protection

The full-bridge is well known to be capable of blocking current in either direction by impressing a voltage with opposite polarity [19]. This can be easily achieved by turning off all active switches. This feature is utilized as a general way of protection. In addition, the switch level protection also serves as a backup protection [25] in addition to the proposed DC fault operation control.

For the 16 sensing feedback channels, when the sensing information is transferred to the central controller, each sensing signal is compared to two pre-set electric levels, which correspond to an upper limit and a lower limit of the original sensed operation variable. Then all the comparison results are transferred to CPLD.

For the 24 gate driver channels, if one channel is working properly, it sends a “high” signal to the optical fiber interface board; if the protection of any one channel is triggered, it sends a “low” signal. Every Optical fiber interface board gathers four channels of information for one PEBB. It sends a “high” signal to CPLD if all four channels are working or a “low” signal if at least one channel has fault.

In addition, a manual switch is connected to CPLD through an optocoupler. It can be used for emergency stop.

CPLD collects all the information from sensing feedback channels, gate drivers and manual switch. If any channel reports a fault, the CPLD sets all gate signals to zero, preventing fault from developing. Gate signals are restored if no fault exists anymore and a fault clear signal is sent from MCU to CPLD. The latter is sent during the discharge process. Therefore, after a fault happens, the converter is designed to only be able to be discharged first before being powered again.

The complete control structure considering relays and protection is shown in Fig. 4-11.

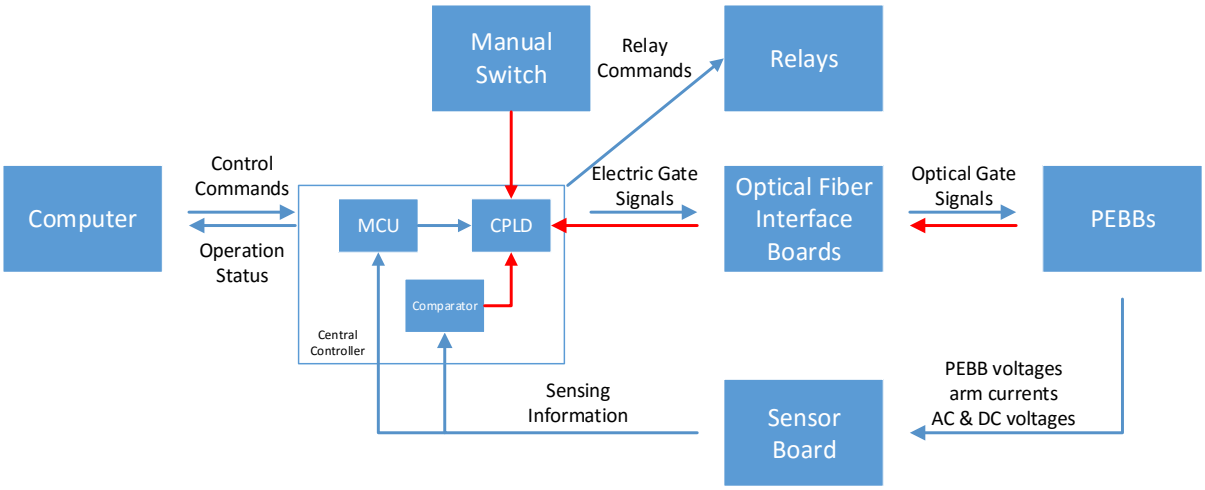


Fig. 4-11 The complete control structure

4.3.4 Code Implementation

The control function is implemented into the MCU using C language and into the CPLD using VHDL. The code is developed based on the example code, which is provided by the manufactures and modified by Dr. Zhiyu Shen.

In the MCU code, the essential initializations needs to be conducted first. Then a main loop is run forever, which includes the additional four channels of ADC, the communication with a computer and the actions for pre-charge and discharge. The twelve channels of ADC, the normal operation control and the fault operation control are implemented in the interrupt with a frequency of 25 kHz.

In the CPLD code, several different clocks are generated based on a 10 MHz input clock for different purposes. The twelve complementary gate signals with deadtime based on the twelve input gate signals and a 250 MHz clock. The final output gate signals depends on the twelve pairs of generated gate signals and all the fault information. The relay commands are passed through from the MCU to the corresponding relays.

4.3.5 Controller Discretization

The control parameters used in the converter prototype are summarized in Tab. 4-5.

Since the control is implemented using the 200 MHz digital controller, all the controllers are actually discrete controllers instead of ideal continuous controllers. The control frequency is 25 kHz.

There are three types of controllers used in the scheme: proportional controller, proportional-integral controller, and quasi proportional-resonant controller. The proportional

gain is not affected by the discretization. However, the integral gain and resonant gain need to be adjusted to provide the desired performance [77].

Tab. 4-5 Control parameters used in converter prototype

Controller	Parameters
PI-1	$K_p = 0.2, K_i = 5$
PI-2	$K_p = 15, K_i = 225$
PI-3	$K_p = 0.01, K_i = 25$
PI-4	$K_p = 1, K_i = 1$
PR-5	$K_p = 0.05, \omega_c = 10, K_{r1} = 10$
P-6	$K_p = 0.03$
PI-7	$K_p = 0.5, K_i = 50$
PI-8	$K_p = 2, K_i = 2$

Assume a continuous integral controller is:

$$y_i(s) = K_{i-c}\frac{1}{s}u_i(s) \tag{4-7}$$

Where $u_i(s)$ is the continuous input, $y_i(s)$ is the continuous output, K_{i-c} is the gain in continuous domain. Use the backward approximation [77]:

$$s \approx \frac{z-1}{zT} \tag{4-8}$$

Then in discrete domain, the controller is

$$y_i(k) = K_{i-c}\frac{1}{\frac{z-1}{zT_c}}u_i(k) \tag{4-9}$$

Where T_c is the control cycle. Then,

$$(z-1)y_i(k) = T_c K_{i-c} z u_i(k) \tag{4-10}$$

$$y_i(k+1) - y_i(k) = T_c K_{i-c} u_i(k+1) \tag{4-11}$$

$$y_i(k) = y_i(k-1) + T_c K_{i-c} u_i(k) \tag{4-12}$$

Therefore, the equivalent discrete integral controller is:

$$y_i(k) = y_i(k-1) + K_{i-d} u_i(k) \tag{4-13}$$

Where $u_i(k)$ is the discrete input, $y_i(k)$ is the discrete output, $K_{i-d} = T_c K_{i-c}$ is the gain in discrete domain.

Assume a continuous quasi resonant controller is:

$$y_r(s) = \frac{2\omega_c K_r s}{s^2 + 2\omega_c s + (\omega_0)^2} u_r(s) \tag{4-14}$$

Where $u_r(s)$ is the continuous input, $y_r(s)$ is the continuous output, K_r is the continuous resonant gain, ω_C is the bandwidth parameter, and ω_0 is desired resonant frequency. Use the Tustin's approximation [77]:

$$s \approx \frac{2}{T}\frac{z-1}{z+1} \tag{4-15}$$

Then in discrete domain, the controller is

$$y_r(s) = \frac{2\omega_c K_r \dfrac{2}{T_c}\dfrac{z-1}{z+1}}{\left(\dfrac{2}{T_c}\dfrac{z-1}{z+1}\right)^2 + 2\omega_c \dfrac{2}{T_c}\dfrac{z-1}{z+1} + (\omega_0)^2} u_r(s) \tag{4-16}$$

Then,

$$y_r(s) = \frac{2\omega_c K_r 2T_c(z-1)(z+1)}{(2(z-1))^2 + 2\omega_c 2T_c(z-1)(z+1) + (\omega_0)^2 T_c{}^2 (z+1)^2} u_r(s) \tag{4-17}$$

$$(z^2 + a_1 z + a_2) y_r(s) = (b_0 z^2 + b_1 z + b_2) u_r(s) \tag{4-18}$$

Where,

$$a_1 = \frac{2\omega_0{}^2 T_c{}^2 - 8}{\omega_0{}^2 T_c{}^2 + 4\omega_c T_c + 4} \tag{4-19}$$

$$a_2 = \frac{\omega_0{}^2 T_c{}^2 - 4\omega_c T_c + 4}{\omega_0{}^2 T_c{}^2 + 4\omega_c T_c + 4} \tag{4-20}$$

$$b_0 = \frac{4K_r \omega_c T_c}{\omega_0{}^2 T_c{}^2 + 4\omega_c T_c + 4} \tag{4-21}$$

$$b_1 = 0 \tag{4-22}$$

$$b_2 = -\frac{4K_r \omega_c T_c}{\omega_0{}^2 T_c{}^2 + 4\omega_c T_c + 4} \tag{4-23}$$

Therefore, the equivalent discrete integral controller is:

$$y_r(k) = -a_1 y_r(k-1) - a_2 y_r(k-2) + b_0 u_r(k) + + b_1 u_r(k-1) + + b_2 u_r(k-2) \tag{4-24}$$

Where $u_r(k)$ is the discrete input, $y_r(k)$ is the discrete output, a_1, a_2, b_0, b_1, b_2 are the gain in discrete domain.

After the above approximations, the discrete controllers should have almost the same performance compared to the original continuous controllers. However, the sample and hold effect needs to be taken into account. The transfer function of the effect is:

$$H_e(s) = \frac{1 - e^{-sT_c}}{sT} \approx \left(\frac{s}{\omega_n}\right)^2 + \frac{s}{\omega_n Q_z} + 1 \tag{4-25}$$

Where,

$$\omega_n = \frac{\pi}{T_c}, Q_z = -\frac{2}{\pi} \tag{4-26}$$

The sample and hold effect has little influence at low frequency. But it dramatically reduces the phase of the transfer function near the control frequency. Therefore, if the bandwidth is too

high, the sample and hold effect may cause an insufficient phase margin and thus an unstable condition.

In the proposed control scheme, the phase leg control is designed to achieve the fastest fault current clearing. However, the performance is limited by the control frequency. A lower proportional gain is used for stability concern.

4.3.6 Controller Initialization

As the transient response is the focus of the DC fault operation control, the controller initialization is very important. It includes both physical initialization in MCU and mathematical initialization of the values of the controllers.

As shown in Tab. 4-5, there are eight functionally different controllers. PI-1, PI-3, PI-4, and PR-5 are only used in normal operation control, PI-7 and PI-8 are only used in fault operation control, the others are used in both operations. When running the code, all the controllers have to be physically initialized to achieve a fast transient between two control modes. Whenever a controller is not used, the integral output should be reset to a default value. In most of the cases, zero is a good choice for the default value.

4.3.7 Modulation

Since the Full-Bridge is selected as the PEBB topology, it also provides more modulation flexibility. For a FB PEBB shown in Fig. 3-5, there are four switches separated into two pairs and each pair uses complementary gate signals. The connection relationship of the capacitor depends on the difference of two pairs of gate signals.

$$v_o = (s_1 - s_3)v_c \tag{4-27}$$

Where v_o is the instant output voltage of the PEBB, s_1 is the gate signal of switch S_1, s_3 is the gate signal of switch S_3, v_c is the instant capacitor voltage. Taking average in one switching cycle:

$$V_o = (d_1 - d_3)V_c \tag{4-28}$$

Where V_o is the average output voltage of the PEBB in one switching cycle, d_1 is the duty ratio of switch S_1, d_3 is the duty ratio of switch S_3, V_c is the average capacitor voltage. The equation is valid since the capacitor voltage changes much slower than the switching frequency.

Different PWM technologies can be implemented. The first method is to let the FB act like an HB. One pair of switches uses the same gate signals as an HB, the other pair of switches is not switching. For example, let:

$$\begin{cases} d_1 = d_j \\ d_3 = 0 \end{cases} \tag{4-29}$$

Then,

$$d_o = d_1 - d_3 = d_j \tag{4-30}$$

Where d_o is the equivalent output duty ratio of the PEBB.

Fig. 4-12 shows the carrier, reference signals and the output gate signals.

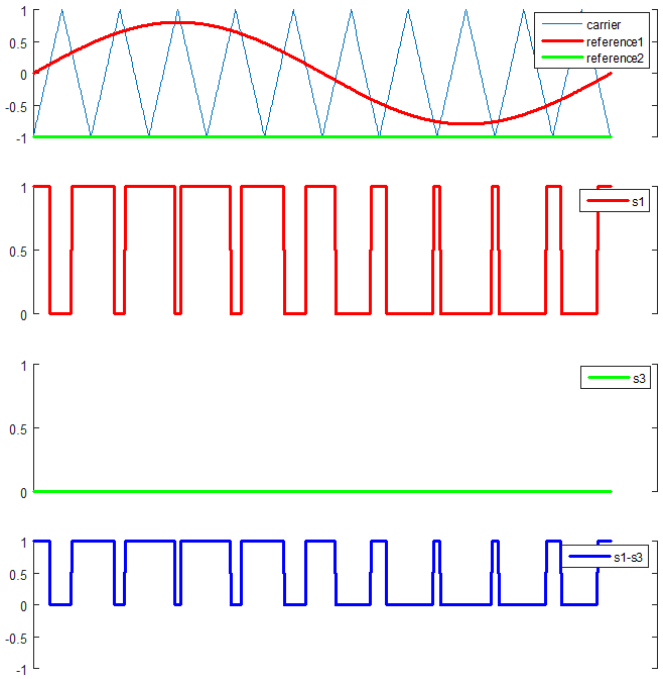


Fig. 4-12 Carrier, references and gate signals for HB-like PWM

In the above waveform, the output duty ratio is set to be similar with the real duty ratio for PEBB in normal operation.

$$d_o = \frac{1+0.8\sin\left(2\pi f_o t\right)}{2} \tag{4-31}$$

The ratio between the carrier frequency (switching frequency) and the output frequency is set to be small for better illustration. In real operation, it will be much larger.

$$\frac{f_c}{f_o} = 10 \tag{4-32}$$

The second method is the Bipolar PWM. All four switches are switching and they are switching at the same time. Let:

$$\begin{cases} d_1 = \dfrac{1+d_j}{2} \\ d_3 = \dfrac{1-d_j}{2} \end{cases} \tag{4-33}$$

Then,

$$d_o = d_1 - d_3 = d_j \tag{4-34}$$

Fig. 4-13 shows the carrier, reference signals and the output gate signals.

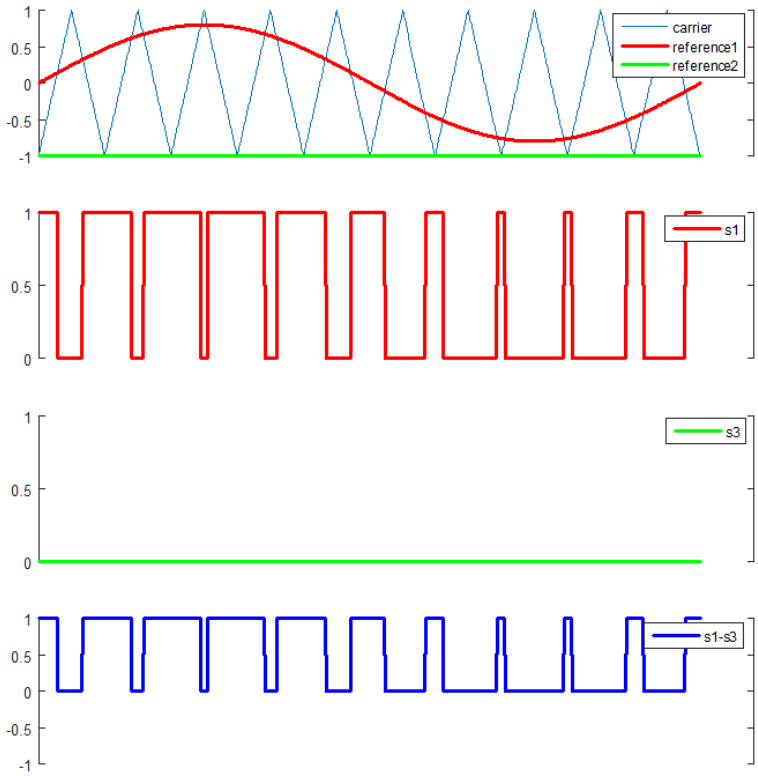


Fig. 4-13 Carrier, references and gate signals for Bipolar PWM

The duty ratio, output frequency and carrier frequency are the same as the previous case.

The third method is the Unipolar PWM. All four switches are switching but switching is only simultaneous within the same switch leg. Let:

$$\begin{cases} d_1 = \dfrac{1+d_j}{2} \\ d_3 = \dfrac{1-d_j}{2} \end{cases} \tag{4-35}$$

Then,

$$d_o = d_1 - d_3 = d_j \tag{4-36}$$

Fig. 4-14 shows the carrier, reference signals and the output gate signals.

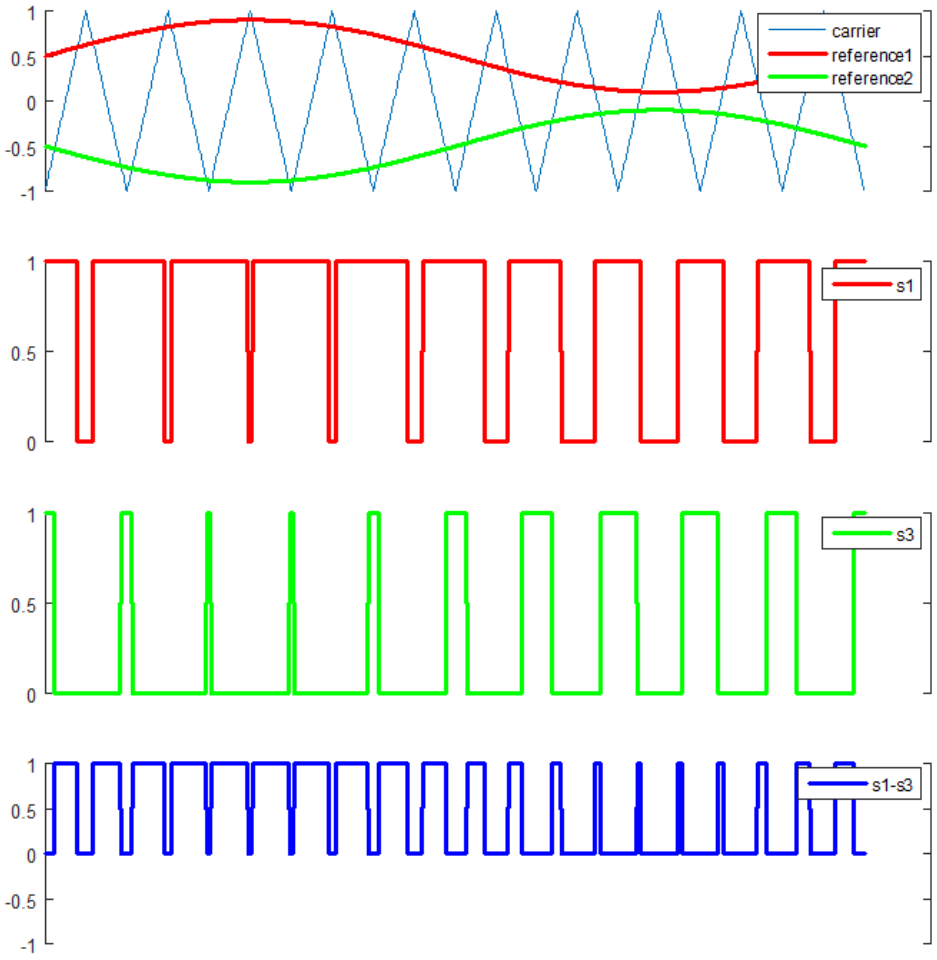


Fig. 4-14 Carrier, references and gate signals for Unipolar PWM

The duty ratio, output frequency and carrier frequency are the same as the previous case.

The HB-like PWM will lead to lower loss as one pair of switches does not have switching loss. However, it needs modification if the desired output is negative. The Bipolar and Unipolar PWM can be directly used to generate gate signals no matter whether the desired output duty ratio is positive or negative. For Bipolar PWM, the output is changing among positive, zero or negative even if the desired output is positive (or negative) in one switching cycle. For Unipolar PWM, the pulse number is doubled compared to the other two PWM technologies. In this way, the switching frequency is equivalently doubled and the switching ripple can be reduced. Unipolar PWM is therefore selected in this study.

4.4 Functional Tests of the Modular Multilevel Converter Prototype

The function and performance of the built MMC prototype are verified through experiments during the design and construction process. Different functional tests are conducted systematically for both function and safety reasons.

4.4.1 Switching Device and Gate Driver Test

The switching performance of every top or bottom switch of the SiC MOSFET half-bridge module and the protection action of every channel of gate driver unit needs to be tested. The former is tested by a Double pulse test (DPT), the latter is tested by a short-circuit test.

4.4.1.1 Double Pulse Test

Double pulse tests are usually used to test the switching characteristics of a switching device. The circuit configuration of the test setup is shown in Fig. 4-15.

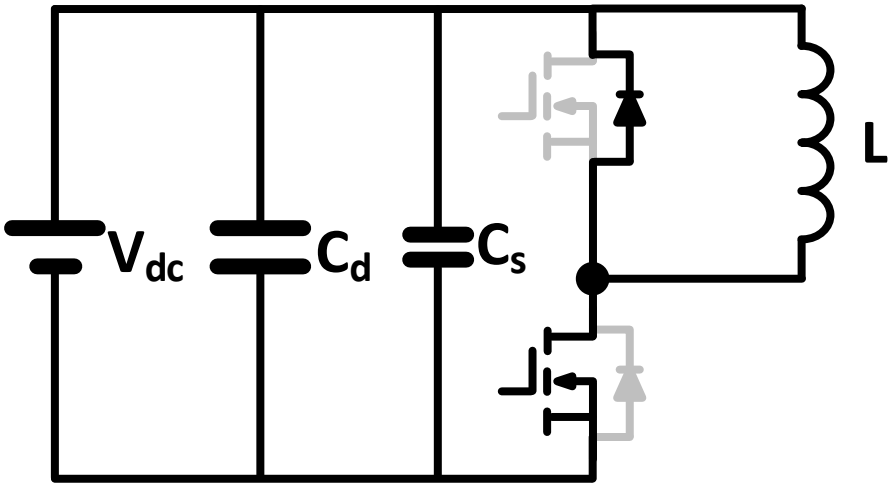


Fig. 4-15 The circuit configuration of the double pulse tester

V_{dc} is a DC voltage source to charge the bus to the desired voltage, C_d is the PEBB capacitor bank, C_s is the decoupling capacitor, L is the load inductor. In this setup, the bottom switch is the device under test (DUT). A function generator generates a gate signal for

the device. When the gate signal is high, the bottom switch is on and current flows through the MOSFET of the bottom switch. When the gate signal is low, the bottom switch is off and current flows through the diode of the top switch. By using a double pulse gate signal, the turn-off and turn-on actions are achieved. The test condition is 1 kV bus voltage and 50 A device current, which is close to switching condition in the normal operation of the final test. Every top or bottom switch of the SiC MOSFET half-bridge module and every channel of gate driver is tested. The turn off waveforms and turn on waveforms of one channel are shown in Fig. 4-16.

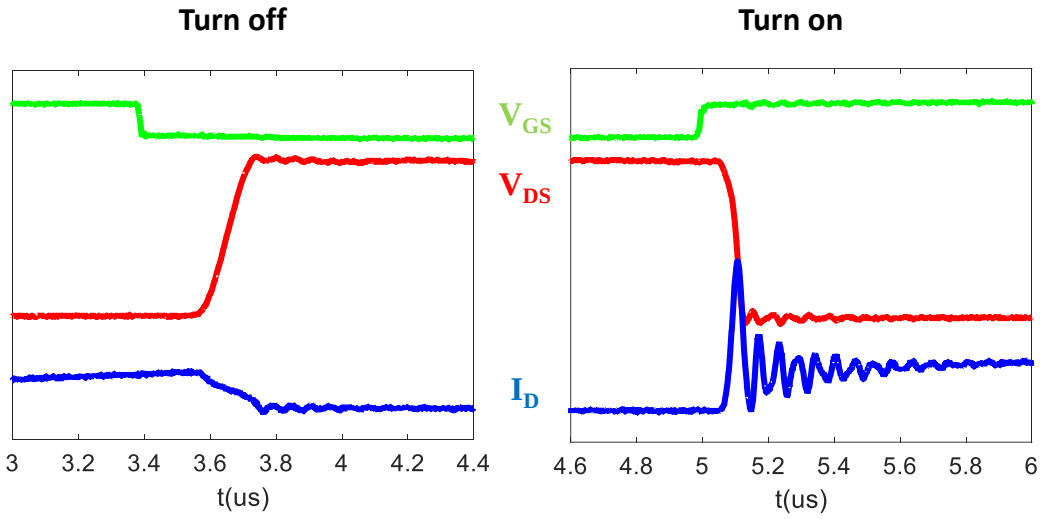


Fig. 4-16 The turn off and turn on performance from Double pulse test

The green waveforms on the top are gate-to-source voltage V_{GS}, the red waveforms in the middle is device drain-to-source voltage V_{DS}, the blue waveforms at the bottom are the device drain current I_D.

The waveforms on the left show the turn-off performance. V_{GS} drops from high (20 V) to low (-4 V), V_{DS} rises from 0 to 1 kV, I_D drops from 50 A to 0. The rising time for voltage

is about 110 ns, the change rate for voltage is about 7.35 V/ns; the falling time for current is about 151 ns, the change rate for current is about 0.26 A/ns.

The waveforms on the right show the turn-on performance. V_{GS} rises from low to high, V_{DS} drops from 1 kV to 0, I_D rises from 0 to 50 A. The falling time for voltage is about 47 ns, the change rate for voltage is about 17.21 V/ns; the rising time for current is about 14 ns, the change rate for current is about 2.88 A/ns.

4.4.1.2 Short-circuit Test

The selected gate driver units use Desaturation for short circuit protection. It monitors on-state drain-to-source voltage to tell whether there is over-current. Based on the gate driver design, the current threshold is about 320 A.

The test setup is exactly the same as the Double pulse test and the test condition is still 1 kV DC bus voltage. One single long pulse is generated by a function generator so that the device current can rise above the protection threshold. Every top or bottom switch of the SiC MOSFET half-bridge module and every channel of gate driver is tested. One set of the test waveforms are shown in Fig. 4-17.

The green waveform on the top is the gate-to-source voltage V_{GS}, the red waveform is device drain-to-source voltage V_{DS} and the blue waveform is the device drain current I_D.

When the drain current rises high enough, the protection is triggered. As a result, the gate signal is shut down, then current drops to zero and drain-to-source voltage rises to 1 kV. The maximum current before protection triggered is about 299 A.

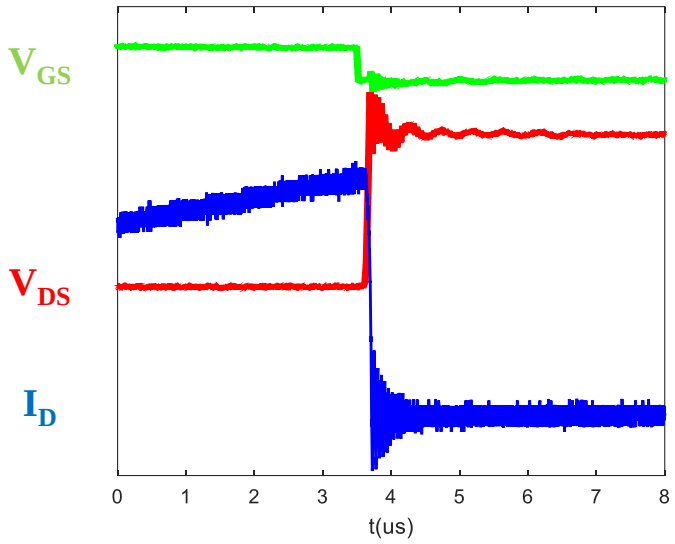


Fig. 4-17 The short circuit protection from short circuit test

4.4.2 PEBB Continuous Test

Every PEBB can be operated as either a DC-DC converter or a DC-AC converter to test the continuous operation performance. A continuous DC-AC test is used here. The circuit configuration of the test setup is shown in Fig. 4-18.

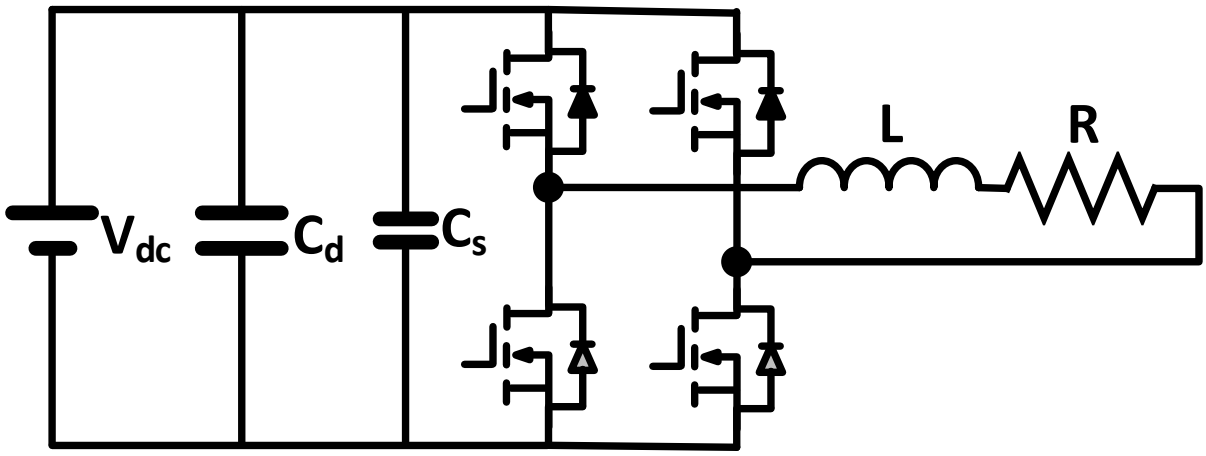


Fig. 4-18 The circuit configuration of the continuous DC-AC test

In Fig. 4-18, V_{dc} is the DC voltage source, C_d is the PEBB capacitor bank and C_s is the decoupling capacitor. All of the above are also used in a Double pulse test and a short circuit test. The load on the AC side is a RL load. The resistor is an 86.4 Ω resistor, the inductor is the 1 mH arm inductor. The test condition is: bus voltage is $V_{dc} = 1kV$, the modulation index is $M = 0.78$, the switching frequency is $f_s = 100kHz$, the output line frequency is $f = 60Hz$. The output apparent power is:

$$\frac{\left(V_{dc} \times M \div \sqrt{2}\right)^2}{\sqrt{R^2 + (2\pi fL)^2}} \approx 3.5kVA \tag{4-37}$$

The steady state operation waveforms are shown in Fig. 4-19.

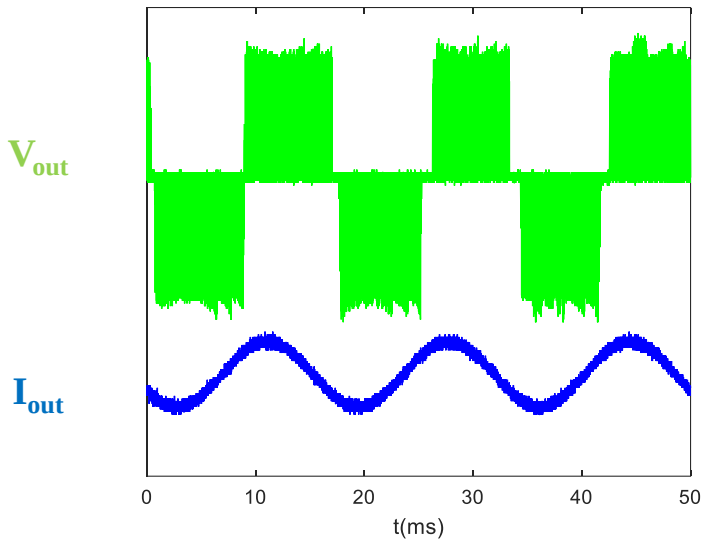


Fig. 4-19 PEBB continuous DC-AC test results

The green waveform on the top is output voltage V_{out} and the blue waveform at the bottom is the output current I_{out}. During half of the output line cycle, the output voltage is either 1 kV or 0; during the other half cycle, the output voltage is either -1 kV or 0. The output current has a RMS value of 6.83 A.

Open-loop gate signals generation, including deadtime generation, PEBB thermal design are also verified during the PEBB continuous test.

4.4.3 Converter Test

Fig. 4-20 shows the three phase converter mounted in the cabinet. Six PEBBs sit on the top three layers, three AC inductors and the AC relay sit on the bottom layer, the central controller and six optical fiber interface boards are mounted at the back of the cabinet.

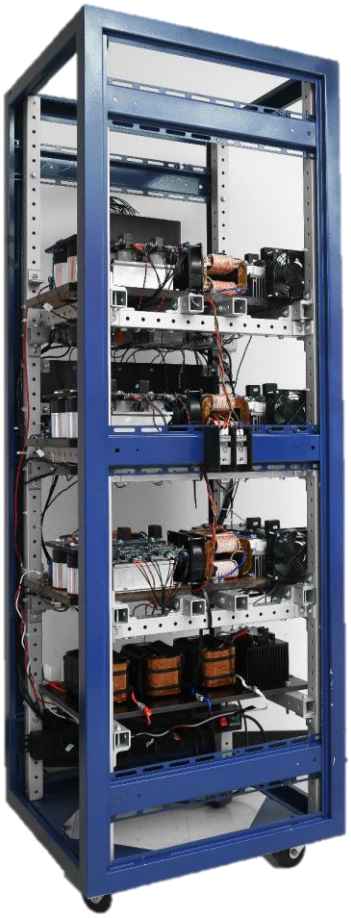


Fig. 4-20 Hardware prototype of a Modular Multilevel Converter

The converter final tests include both an inverter test and a rectifier test, following the operation sequences described in Section 4.3.2.

Prior to the final test, all the sensing feedback channels are tested and calibrated. All the protection channels are tested.

Although the PEBBs are test to the full voltage rating independently, due to EMI constraints at the moment, the converter tests cannot be conducted at the full voltage rating while addressing the EMI emissions.

4.4.3.1 Inverter Test

The inverter test is tested under 0.5 kV DC bus voltage. The load of each phase is a 14.4 Ω resistor. The output only includes active power:

$$\left(\frac{V_{dc}}{2}\times M \div \sqrt{2}\right)^2 \times R \times 3 \approx 4.0kW \tag{4-38}$$

The steady state operation waveforms are shown in Fig. 4-21.

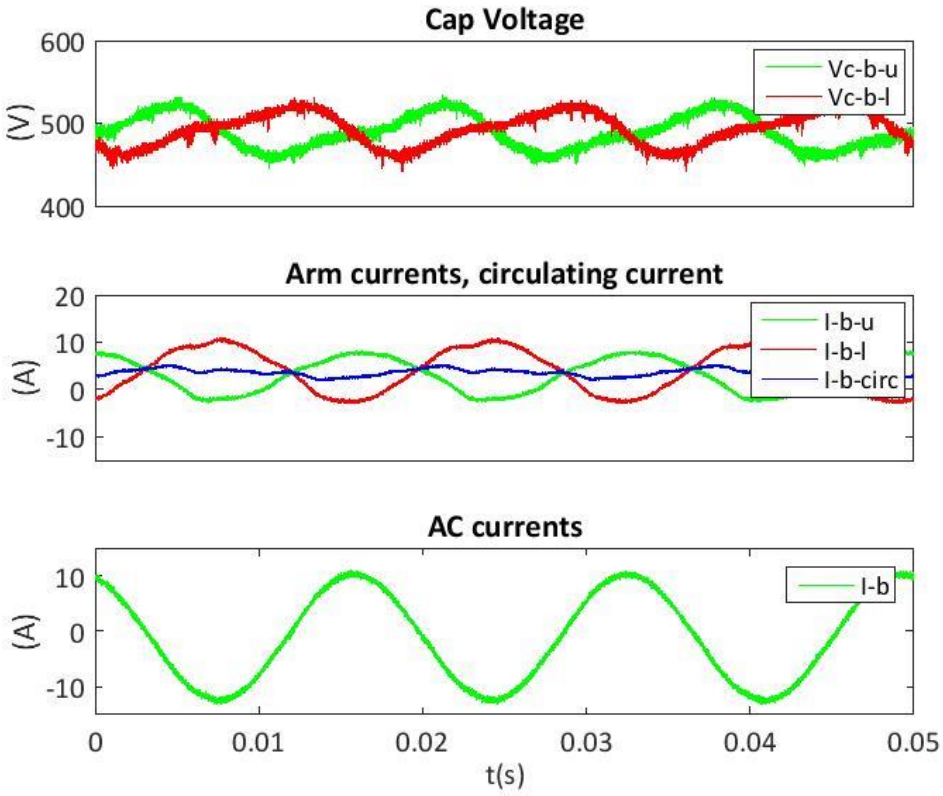


Fig. 4-21 Inverter test results

The first subplot shows the upper arm PEBB capacitor voltage and the lower arm PEBB capacitor voltage of phase B. They are regulated well around 500 V. The second subplot shows the upper arm current, the lower arm current and the circulating current of phase B. The second order harmonic in the circulating current is generally suppressed. The third subplot shows the AC output currents of phase B.

4.4.3.2 Rectifier Test

The rectifier test is tested under 130 V AC bus voltage (phase, RMS). The DC load is a 57.6 Ω resistor. The DC voltage references is 500 V. The output only includes active power:

$$\frac{V_{dc}^{\ 2}}{R} = 4.34kW \tag{4-39}$$

The steady state operation waveforms are shown in Fig. 4-22.

The first subplot shows the upper arm PEBB capacitor voltage and the lower arm PEBB capacitor voltage of phase B. They are regulated well around 500 V. The second subplot shows upper arm current, the lower arm current and the circulating current of phase B. The second order harmonic in circulating current is suppressed, so the circulating current mainly consists of DC component. The third subplot shows the DC output voltage. It is regulated well around 500 V. The fourth subplot shows the DC output current.

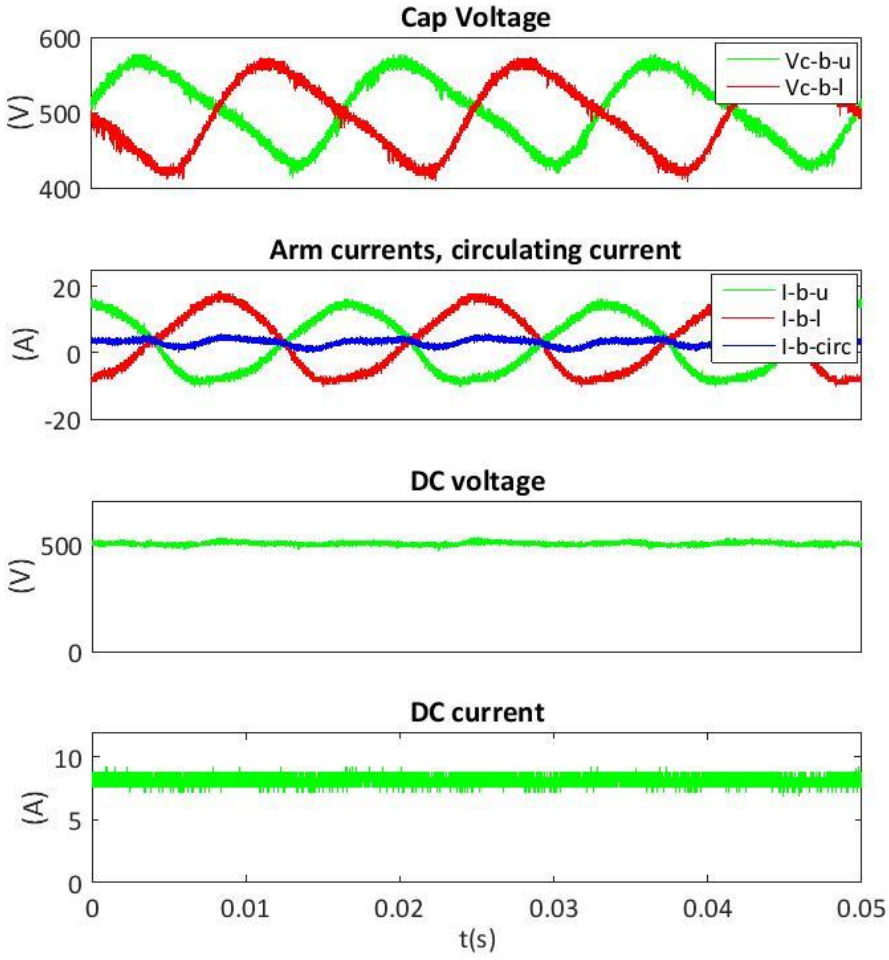


Fig. 4-22 Rectifier test results

4.5 DC Short Circuit Fault Test of the MMC Prototype

The DC short circuit fault test is conducted to experimentally verify the proposed DC fault operation control. The circuit configuration is almost the same when compared to the rectifier test except that one more resistor is connected through a relay between the positive and negative bus. The "short circuit" resistor has a value of:

$$R_{sc} = \frac{1}{6}R = 9.6\Omega \tag{4-40}$$

Where $R = 57.6\Omega$ is the normal rectifier test load.

The AC bus voltage is 130 V (phase, RMS), and the DC voltage references is 500 V. A command is sent from the computer to turn on the relay to connect the “short circuit” resistor to the bus to represent the fault. The experiment results during fault current developing and clearing are shown in Fig. 4-23.

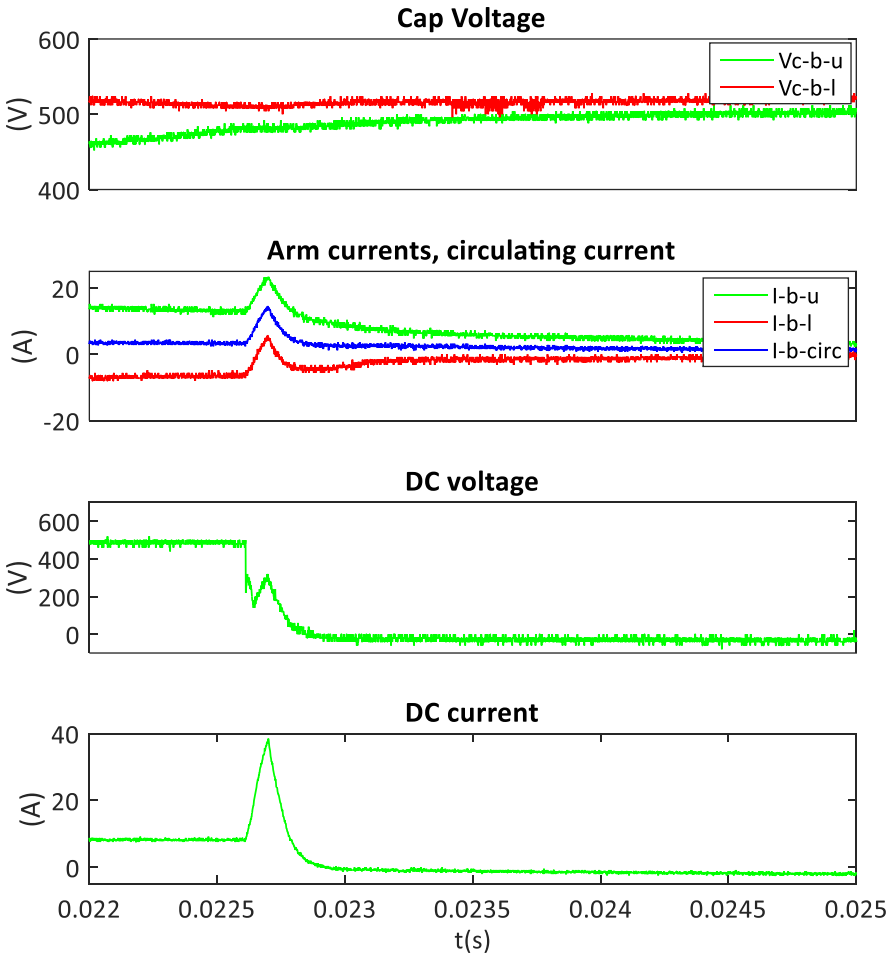


Fig. 4-23 Experiment results of fault current developing and clearing

At the instant when the fault happens, the currents of inductors cannot change immediately, therefore the DC current cannot change immediately either. As the impedance between the DC bus decreases instantly, the DC voltage drops instantly, but is still higher than zero. Then

because of the imbalance between the PEBBs and the DC bus, the fault currents start to develop in arm currents and the DC current. And the DC voltage increases with the current.

In the first $50\mu s$, it increases from $8.0A$ to $26.0A$. The increase rate of the DC current during fault in simulation is approximately:

$$\frac{26.0-8.0}{50\times10^{-6}}=0.36\times10^{6}A/s \tag{4-41}$$

Based on (3-7), the calculated increase rate is:

$$\frac{3V^{*}_{dc}}{2l}=\frac{3\times0.5\times10^{3}}{2\times1\times10^{-3}}=0.75\times10^{6}A/s \tag{4-42}$$

The change rate from the experiment is lower than the calculation results because the "short circuit" resistance is larger than zero. However, the behavior of the DC current is as expected.

The DC current reaches the peak value $38.4A$ in around $90\mu s$, which is a little more than two control cycles ($80\mu s$). Then the DC current begins to drop. In the first $50\mu s$, it decreases from $38.4A$ to $18.4A$.The decrease rate of the DC current during fault in the simulation is approximately:

$$\frac{38.4-18.4}{50\times10^{-6}}=0.4\times10^{6}A/s \tag{4-43}$$

Based on the previous analysis, the calculated decrease rate is:

$$\frac{3V^{*}_{dc}}{l}=\frac{3\times0.5\times10^{3}}{1\times10^{-3}}=1.5\times10^{6}A/s \tag{4-44}$$

The change rate from the experiment is lower than the calculation results because the control cannot achieve the fastest fault current clearing due to the limitation of the sample and hold effect. However, the behavior of the DC current is as expected. It eventually drops to zero in around $194\mu s$.

The experiment results during steady state of the fault operation are shown in Fig. 4-24.

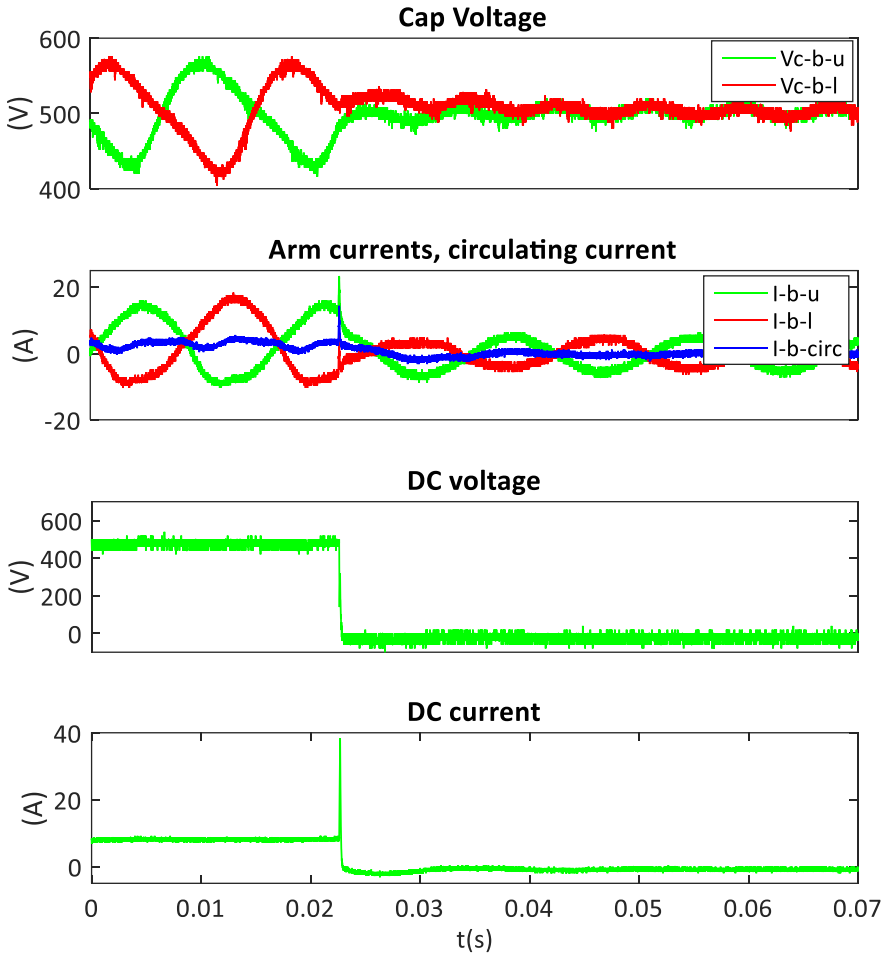


Fig. 4-24 Experiment results during steady state of fault operation

After the fault current is cleared, the converter reaches a new steady state with a zero DC bus voltage. Both the DC bus voltage and current are around zero. The arm currents include a nearly zero DC component and an AC component from the AC source to provide power to maintain the capacitor voltages. All the capacitor voltages are regulated well around the reference value.

A command is sent from computer to turn off the relay to clear the “short circuit” fault and restore the DC bus. The experiment results during re-energizing the DC bus are shown in Fig. 4-25.

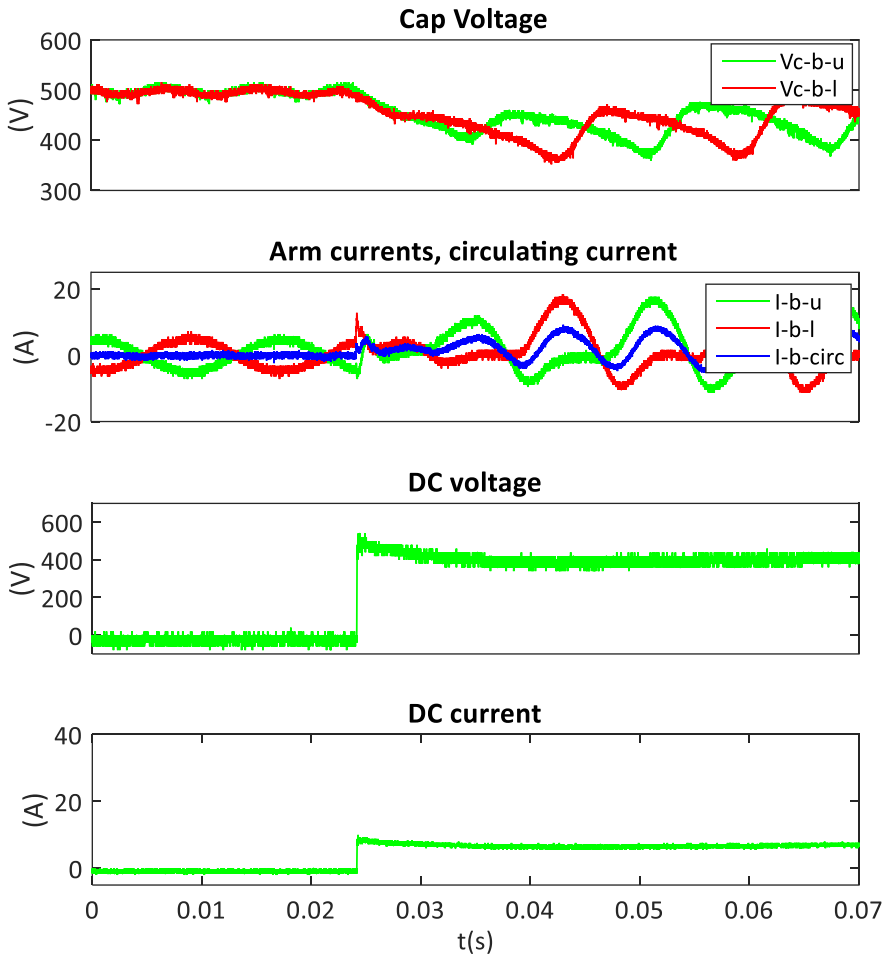


Fig. 4-25 Experiment results during re-energizing the DC bus

As soon as the control switches back to the normal operation control, the DC bus voltage is restored and so is the DC current. The capacitor voltages and arm currents reach the steady state after a short period of transient response.

4.6 Summary

1.7 kV SiC MOSFETs are used to build 1 kV PEBBs operating at 100 kHz. Then a three-phase Modular Multilevel Converter prototype for MVDC applications is built using the PEBBs. The prototype design details are discussed, including: hardware selection and design, control methods and hardware, pre-charge and discharge, as well as protection. Systematical tests are conducted from the component level, to the PEBB level, and then to the converter level to verify the function of the converter. A DC short circuit fault is generated by a small resistor. The experiment results verify the fault current behavior and the proposed DC fault operation control. The fault operation control is triggered in about $90\mu s$ and clears the fault currents in about $194\mu s$. The capacitor voltages are regulated well so that when the fault is cleared, the DC bus can be quickly restored.

Chapter 5. Conclusions and Future Work

The ability to survive a DC short circuit fault is the biggest challenge for the Modular Multilevel Converters in Medium-Voltage DC applications. In this study, the effects and corresponding solutions of a DC short circuit fault are explored through analyses, simulations and experiments.

A MMC with traditional Half-Bridge PEBBs and a normal operation control is demonstrated to lack the ability to deal with the DC fault. As a direct effect of the fault, the DC current and all the arm currents increase very fast, potentially destroying the components in the converter. After comparing different PEBB topologies, the Full-Bridge is selected because of its fault handling capability, full control flexibility, and symmetric configuration despite the highest loss. Based on the fault current analysis and a selected PEBB topology, a DC fault operation control is proposed. Specifically, it is designed to achieve fast fault current clearing and PEBB capacitor voltage regulation under a DC fault condition.

A three-phase SiC-based MMC prototype is designed and built. With the fast SiC devices, by increasing the switching frequency, the converter still has a high equivalent switching frequency without requiring multiple series-connected modules. The gate driver units, capacitor bank, arm inductors, AC inductors, busbars, thermal dissipating equipment and control hardware are selected or designed to achieve the desired operation. Pre-charge and discharge, controller discretization and initialization are discussed to implement the control schemes. In the FB-based MMC, turning off all switches is used as a universal protection method. Systematical tests are conducted from the component level, to the PEBB level, and

then to the converter level to verify the function of the converter, including the switching performance, continuous operation and protection action.

The fault current behavior and the performance of the proposed control are verified by both simulation and experiment. In the hardware test, a DC short circuit fault is generated by a small resistor. The fault operation control is triggered in about $90\mu s$ and clears the fault currents in about $194\mu s$. The converter is able to achieve a steady state with a zero DC bus voltage, and quickly restore the DC bus after the fault is cleared.

In the future, with the verified DC fault operation control, it is worth exploring how a converter with fault current limiting function can coordinate with other converters and relays. The preference is to have a whole MVDC distribution system with minimal requirements for relays, a minimal loss of loads and maximum control flexibility during a short DC fault. In addition to the worst case of a DC short circuit fault, the effects and solutions of other fault modes may need to be explored. The EMI emissions of the converter prototype also needs to be addressed.

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