Tensile-Strained Ge/$In_xGa_{1-x}As$ Heterostructures for Electronic and Photonic Applications

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ABSTRACT

The continued scaling of feature size in silicon (Si)-based complimentary metal-oxide-semiconductor (CMOS) technology has led to a rapid increase in compute power. Resulting from increases in device densities and advances in materials and transistor design, integrated circuit (IC) performance has continued to improve while operational power (V_{DD}) has been substantially reduced. However, as feature sizes approach the atomic length scale, fundamental limitations in switching characteristics (such as subthreshold slope, *SS*, and OFF-state power dissipation) pose key technical challenges moving forward. Novel material innovations and device architectures, such as group IV and III-V materials and tunnel field-effect transistors (TFETs), have been proposed as solutions for the beyond Si era. TFETs benefit from steep switching characteristics due to the band-to-band tunneling injection of carriers from source to channel. Moreover, the narrow bandgaps of III-V and germanium (Ge) make them attractive material choices for TFETs in order to improve ON-state current and reduce *SS*. Further, Ge grown on $In_xGa_{1-x}As$ experiences epitaxy-induced strain (ε), further reducing the Ge bandgap and improving carrier mobility. Due to these reasons, the ε-Ge/$In_xGa_{1-x}As$ system is a promising candidate for future TFET architectures. In addition, the ability to tune the bandgap of Ge *via* strain engineering makes ε-Ge/$In_xGa_{1-x}As$ heterostructures attractive for nanoscale group IV-based photonics, thereby benefitting the monolithic integration of electronics and photonics on Si. This research systematically investigates the material, optical, and heterointerface properties of ε-Ge/$In_xGa_{1-x}As$ heterostructures on GaAs and Si substrates. The effect of strain on the heterointerface band alignment is comprehensively studied, demonstrating the ability to modulate the effective tunneling barrier height (E_{beff}) and thus the threshold voltage (V_T), ON-state current, and *SS* in future ε-Ge/$In_xGa_{1-x}As$ TFETs. Further, band structure engineering *via* strain modulation is shown to be an effective technique for tuning the emission properties of Ge. Moreover, the ability to heterogeneously integrate these structures on Si is demonstrated for the first time, indicating their viability for the development of next-generation high performance, low-power logic and photonic integrated circuits on Si.

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Chapter 1 – Introduction

1.1. Scaling Limitations for Si-based Complimentary Metal-Oxide-Semiconductor and Interconnect Technology

The aggressive reduction of feature size in conventional silicon (Si) metal-oxide-semiconductor field-effect transistor (MOSFET) technology over the past five decades faces several key technical challenges moving forward. As device dimensions approach the atomic length-scale, reduction of supply voltage (V_{DD}) below 0.5 V while maintaining low OFF-state current, I_{OFF}, becomes increasingly difficult due to the transport mechanism governing traditional MOSFETs, *i.e.*, the thermionic emission of charge carriers from the source into the channel. This fundamentally limits conventional MOSFET switching characteristics, resulting in increased leakage current, a substantially reduced I_{ON}/I_{OFF} ratio, and increased static power consumption **[1–4]**. Fig. 1.1 **[1]** shows the trends in subthreshold (red) and active (blue) power densities as a function of decreasing gate length for commercial Si MOSFETs, suggesting that OFF-state power consumption will surpass ON-state power consumption as gate lengths approach the 22 nm technology node. Further, while V_{DD} scaling is necessary for maintaining device performance and minimizing active power dissipation as gate length is reduced, a fundamental trade-off exists between lowering threshold voltage, V_{TH}, and the OFF-state leakage current. The relationship between I_{OFF} and V_{TH} is given by **[5]**:

$$I_{OFF} = I_{DS} \cdot 10^{-V_{TH}/SS} \tag{1.1}$$

where I_{DS} is the drain to source current and *SS*, the subthreshold slope of the device, is the required change in gate voltage, V_{GS}, necessary to increase the output current by one

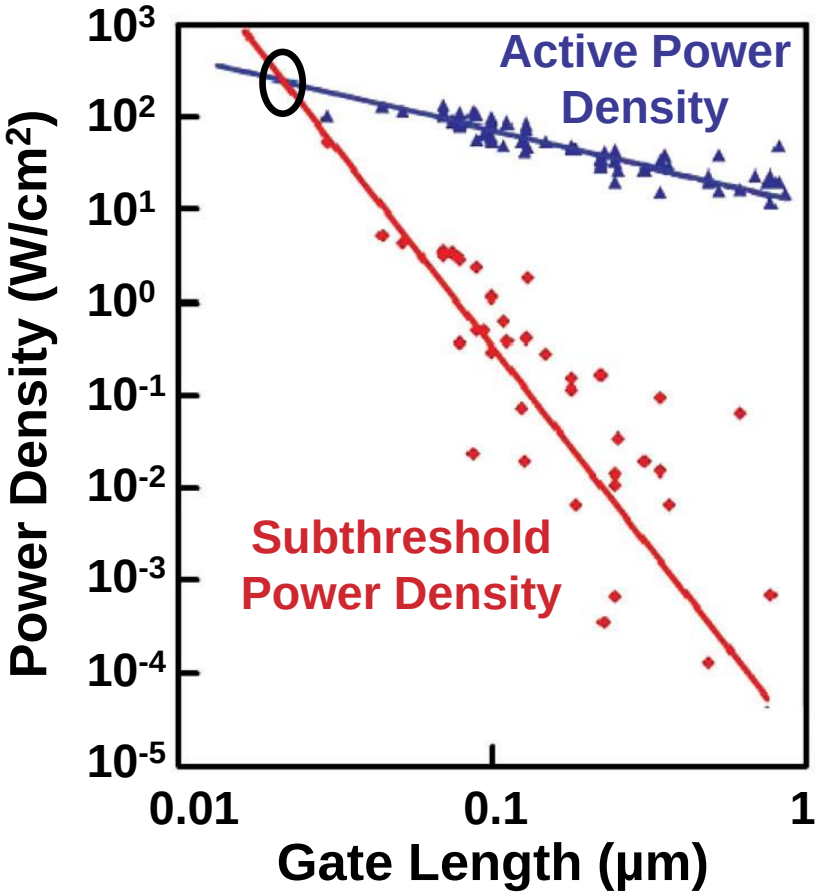

Figure 1.1 Active (blue) and subthreshold (red) power densities from commercial Si MOSFETs with gate lengths between 0.01 μm to 1 μm. As gate length approaches the 22 nm technology node, the fraction of total power consumption taken by the subthreshold power density is expected to increase. At the cross-over point (black circle), the OFF-state power consumption will surpass the ON-state power consumption [4]. Used with permission of Nanotechnology Reviews.

addition, the subthreshold slope can be defined as [6]:

$$SS = \frac{dV_{GS}}{d(log[I_{DS}])}\ [\mathrm{mV/dec}]\,. \tag{1.2}$$

In standard Si MOSFET technology, the subthreshold current is independent of V_{GS} and can be written as [7]:

$$SS = \frac{kT}{q}\ln(10)\left(1+\frac{C_{DM}}{C_{OX}}\right) \quad (1.3)$$

where kT/q is a thermal factor, C_{DM} is the depletion capacitance, and C_{OX} is the gate oxide capacitance. For $\frac{C_{DM}}{C_{OX}}$ close to zero, (1.3) approaches a lower limit of approximately 60 mV/dec at T = 300 K; however, practical *SS* is limited to 70-90 mV/dec due to short-channel effects as gate length are scaled below 1 µm [1, 2]. Fig. 1.2 [4] shows an approximate representation of the effect of decreasing V_{TH} on the OFF-state current by plotting the transfer characteristics (I_{DS} *vs.* V_{GS}) for conventional MOSFETs (black) assuming an ideal *SS* of 60 mV/dec. As suggested by (1.1), Fig. 1.2 shows that as V_{TH} decreases, the fundamental limit to *SS* necessitates that I_{OFF} increase exponentially in response. To circumvent the degradation in I_{OFF} while still allowing for scaling of V_{TH}, steep subthreshold slope switches (green) have been proposed, thereby drastically reducing I_{OFF} while maintaining high drive current. Due to the substantial decrease in I_{OFF} and the lower V_{TH} of steep subthreshold slope switches, such transistors are expected to significantly reduce subthreshold and active power consumption. One such transistor architecture, the tunneling field-effect transistor (TFET), is being extensively investigated as a potential replacement for Si MOSFET technology in the low- and ultra-low-power regimes (< 0.5 V and < 0.3 V, respectively) [2–6]. Operating on the band-to-band tunneling injection of carriers from the source into the channel, TFETs have the potential for steep subthreshold dynamics suitable for low-power logic applications [2–4].

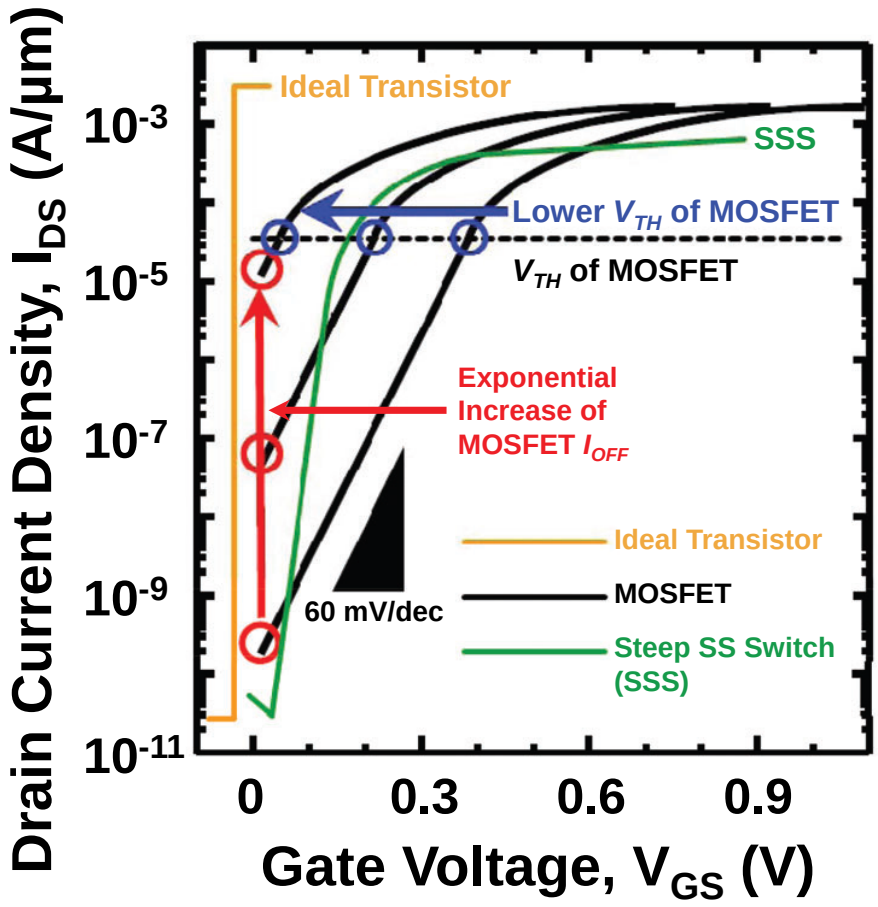

Figure 1.2 Comparison of the transfer characteristics (I_{DS} *vs.* V_{GS}) for an ideal transistor (orange), conventional Si MOSFET (black), and steep subthreshold slope switch (green). Due to the fundamental *SS* lower limit of 60 mV/dec at T = 300 K, I_{OFF} increases exponentially as V_{TH} is scaled down. **[4]** Used with permission of Nanotechnology Reviews.

Although several current efforts **[8–14]** have focused on compositionally tailored III-V type-II staggered gap materials, such as $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructures for low-power TFET applications, less attention has been devoted to $Ge/In_xGa_{1-x}As$ TFET heterojunctions **[15–17]**. In such TFET architectures, the heterointerface band alignment, and therefore I_{ON}, can be tailored by varying the indium (In) alloy composition in the

$In_xGa_{1-x}As$ "virtual substrate" and the doping of the Ge source region **[2, 3, 15, 16, 18]**. Additionally, the low bandgaps and low carrier transport and tunneling masses of Ge and $In_xGa_{1-x}As$ are expected to further enhance I_{ON}. Moreover, the incorporation of biaxial tensile strain (ε) into Ge thin films *via* epitaxy through $In_xGa_{1-x}As$ strain templates allows for further control over the band offsets at the Ge/$In_xGa_{1-x}As$ interface as well as improved carrier transport and tunneling properties. Whereas recent work **[16]** has demonstrated control over the heterointerface band offsets through tensile-strained Ge (ε-Ge)/$In_xGa_{1-x}As$ heterostructures with moderate strain, one of the objectives of this thesis is to comprehensively investigate the suitability of ε-Ge/$In_xGa_{1-x}As$ heterojunctions for TFET applications utilizing a wide range of strains on both GaAs and Si substrates.

In addition to the increased total power consumption resulting from enhanced OFF-state leakage current, metal interconnects are estimated to account for half to three quarters of the total power dissipation in state-of-the-art Si CMOS **[19, 20]**, thereby significantly limiting energy-efficient performance scaling in highly-scaled technology nodes. Due to the necessity of charging interconnects with a signaling voltage during data transmission, the total energy necessary for a transmission event using metal lines is challenging to reduce. This signaling energy is given by **[19]**:

$$E_s \geq C_l V_r^2 \tag{1.4}$$

where C_l is the metal line capacitance (in F) and V_r is the signaling voltage. In current Si CMOS technology, metal interconnect capacitances are on the order of ~2 pF/cm, thus limiting avenues for the reduction of the signaling energy to the optimization of the signaling voltage, V_r. Although present signaling schemes utilize signaling voltages below logic voltage, *i.e.*, low swing signaling, increasing noise levels make it difficult to

further scale V_r. Furthermore, due to the resistive loss in electrical interconnects without integrated repeating signal amplifiers, the bit rate transmitted *via* electrical lines is limited by **[19]**:

$$B \leq B_0 \frac{A}{L^2} \tag{1.5}$$

where A is the cross-sectional area of the interconnect, L is the length of the interconnect, and B_0 is a constant based on the interconnect resistance and capacitance (typically $B_0 \sim 10^{16}$ b/s for on-chip metal lines). One can find from (1.5) that as the metal interconnect cross-sectional area is scaled down and the interconnect length extended, the bit rate supported by the line is considerably reduced.

In order to address these challenges in interconnect scaling, optical data transmission has been proposed as an alternative approach to realizing low-energy, low-loss, and high-bit rate on- and off-chip communication **[19-22]**. In contrast to metal interconnect technology, optical data transmission requires photon-generation and photon-detection, both best described quantum mechanically rather than classically. As a result, the corollary to the metal interconnect signaling energy in optics is the optical energy required to discharge the total photodetector capacitance, C_d, and the electrical input to which the photodetector is connected by the necessary signal voltage, *i.e.* **[19]**:

$$E_p \geq C_d V_r \frac{\hbar\omega}{e} \tag{1.6}$$

where the $\left(\hbar\omega/e\right)$ term is the photon energy in eV. Examining (1.6) one can find that for optical interconnection to be feasible, the photodetector capacitance must be substantially smaller than the metal line capacitance (by a factor of 10 or more) due to the larger photon energy term. Therefore, this places a lower limit on the interconnect length at

which the benefits of optical data transmission will become viable (due to the interconnect capacitance being proportional to both length and cross-sectional area). Whereas some researchers have reported estimates as low as 50 μm for this cross-over point **[19]**, it is clear that photodetector capacitance is critical in realizing energy-competitive on-chip optical data transmission. However, it is also clear that for off-chip (intra-chip) communication to external processing nodes far exceeding the predicted cross-over point in length, optical data transmission offers increasing advantages in both energy efficiency and data rates.

Consequently, the integration of photonic devices for optical signal generation, detection, and modulation on the Si platform is urgently needed. Although the monolithic integration of Si-based optoelectronics is an obvious choice, the indirect bandgap of Si limits the realization of Si-based photonic devices **[23]**. Therefore, the hybrid integration of Ge and III-V optoelectronic devices with state-of-the-art Si CMOS technology is necessary for demonstrating feasible on- and off-chip optical interconnects. Moreover, Ge-based light sources and detectors on Si are indispensable for the successful implementation of intra- and inter-chip optical data transmission **[24-26]**. Whereas the III-V laser bonded to Si waveguide approach **[27, 28]** is limited in area and cost by the evanescently-coupled lasing mode and the high transistor count requirement of III-V transceivers, a tunable wavelength Ge laser could alleviate these constraints and provide a more scalable solution as device size decreases and integration density increases. Thus, the other primary goal of this thesis is to comprehensively study the effect of epitaxial strain on the suitability of band structure engineered Ge/$In_xGa_{1-x}As$ heterostructures for Ge-based light sources and detectors heterogeneously integrated on Si.

1.2. A Brief History of Tunnel-Field Effect Transistors

The gated p-i-n TFET structure was first proposed in 1978 by Quinn *et al*. at Brown University **[29]**. Nearly a decade later, Banerjee *et al*. at Texas Instruments **[30]** examined the electrical properties of a gated, three-terminal p-p^--n Si-based tunneling device. Following these results, Takeda *et al*. at Hitachi **[31]** demonstrated one of the earliest Si-based band-to-band tunneling MOS devices, which exhibited a lack of V_{TH} roll-off with further device scaling and showed promise for continuing transistor scaling deep into the sub-micron regime. In 1995, Reddick and Amaratunga at Cambridge **[32]** investigated the use of Si-based surface tunneling transistors as replacements for traditional MOSFETs in order to preserve performance and operational frequency improvements while circumventing standard CMOS scaling challenges. Shortly thereafter, Hansch *et al*. at the University of the German Federal Armed Forces **[33]** demonstrated experimental results from one of the earliest vertical tunneling transistor structures grown by Si molecular beam epitaxy (MBE). The epitaxial growth technique and vertical structure allowed for the inclusion of an abrupt, heavily doped pocket layer, substantially improving the output characteristics (I_{DS}-V_{GS}) of the fabricated devices. Subsequently, in 2004, Appenzeller *et al*. **[34]** reported the observation of the band-to-band tunneling phenomenon in carbon nanotube-based tunneling devices, providing a path towards ultimate device scaling by utilizing emerging two-dimensional materials. Stemming from increased industry pressure to maintain transistor performance and feature size scaling below the 90 nm technology node, research into alternative MOSFET architectures, including TFETs, has since undergone a swift expansion. As a result, different material systems, including Ge **[35, 36]**, $Si_{1-x}Ge_x$ **[32, 33]**, $Ge_{1-x}Sn_x$ **[37, 38]**, and

III-V **[4]**, **[9-14]** materials, and device architectures (line vs. vertical TFETs) have been at the forefront of state-of-the-art tunnel transistor research.

Most recently, TFETs utilizing binary and ternary III-V materials have seen rapid and substantial progress in operational characteristics, e.g., successive enhancements in I_{ON}, tunneling devices operating near or below 60 mV/dec SS, and improvements in effective I_{ON}/I_{OFF} ratios. Researchers have continued to exceed previous performance boundaries by leveraging novel, multi-material heterostructures, epitaxial strain engineering, and improved high-κ gate dielectric/channel interface engineering. Dewey *et al*. **[18]** demonstrated the first sub-60 mV/dec III-V TFET device operating at room temperature using an $In_{0.53}Ga_{0.47}As$ homojunction with an ultra-thin $In_{0.7}Ga_{0.3}As$ heavily-doped pocket layer at the source/channel interface. Although exhibiting sub-kT/q behavior, the device's drive current was inherently limited by the larger source/channel tunneling barrier resulting from the device's homojunction nature. Simultaneously, Mookerjea and Mohata *et al*. **[14]**, **[39, 40]** investigated the role of In composition on the electrical characteristics of $In_xGa_{1-x}As$ homojunction TFET devices, observing that an increase in In composition from 53% to 70% resulted in a 167% increase in I_{ON}, from 24 µA/µm to 60 µA/µm. The significant enhancement in I_{ON} was attributed to the reduction of the tunneling barrier height at the source/channel interface as a result of the decreasing $In_xGa_{1-x}As$ band gap with increasing In alloy composition. Following this work, Han *et al*. **[41]** demonstrated an $In_{0.53}Ga_{0.47}As$ homojunction TFET with an I_{ON} of 50 µA/µm and SS of 86 mV/dec operating at room temperature by utilizing a heavily-doped $In_{0.7}Ga_{0.3}As$ pocket layer at the tunnel junction and an HfO_2 gate dielectric.

Further heterostructure band engineering was explored *via* the development of the lattice-matched $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ staggered gap tunnel heterojunction. Particularly, Mohata *et al*. **[14]**, **[42]** reported several of the earliest $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ staggered gap TFETs with tunable effective tunneling barrier heights *via* engineering of the In and Sb compositions, respectively. By reduction of the tunneling barrier height through careful selection and control over increased In and Sb compositions, the I_{ON} and I_{ON}/I_{OFF} ratio of the fabricated vertical tunnel transistors was substantially improved with respect to similar-composition $In_xGa_{1-x}As$ homojunction TFETs. Using a $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ staggered gap tunnel heterostructure, Mohata *et al*. **[42]** demonstrated a heterojunction TFET with a high I_{ON} of 135 µA/µm and an I_{ON}/I_{OFF} ratio of 27,000. Subsequently, in 2013, Bijesh *et al*. **[43]** reported a near-broken gap TFET utilizing an $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ tunnel heterojunction that exhibited a record-high I_{ON} of 740 µA/µm operating at 0.5 V and with a cut-off frequency of 19 GHz. However, the SS characteristics of the device were limited to greater than 60 mV/dec as a result of increased trap-assisted tunneling during sub-threshold device operation.

In parallel to this work, several studies have investigated the use of Ge-based materials in homojunction and heterojunction TFET applications. Guo *et al*. **[15]** recently demonstrated the first experimental $Ge/In_{0.53}Ga_{0.47}As$ staggered gap heterojunction tunnel transistors *via* relaxed Ge growth on an $In_{0.53}Ga_{0.47}As$ strain template. However, due to the etch-back and regrowth procedure used in the formation of the p^+-Ge source, as well as misfit dislocations at the $Ge/In_{0.53}Ga_{0.47}As$ tunneling heterointerface, the drive current of the fabricated TFETs was noticeably limited. Also leveraging Ge-based TFET material systems, Han *et al*. **[37]** demonstrated relaxed and uniaxially-strained $Ge_{0.93}Sn_{0.07}$ p-

TFETs on Si with the highest reported drive current (~22 μA/μm) for a group IV-based p-type tunnel transistor. Moreover, the reported I_{ON} was comparable to broken-gap InAs/GaSb-based p-TFETs, indicating the viability of adopting Ge-based material systems for p-channel devices in CMOS TFET logic applications. Further improvement in $Ge_{1-x}Sn_x$ buffer technology to reduce active-layer, electrically-active defects and increase band-to-band tunneling carrier generation is expected to enhance the ON-current of such $Ge_{1-x}Sn_x$ TFET devices. Additionally, the adoption of a heterojunction device architecture (e.g., $Si_yGe_{1-x-y}Sn_x/Ge_{1-x}Sn_x$) has been proposed **[37, 38]** as an alternative path to improve Ge-based TFET drive current and SS. Table 1.1 summarizes the latest experimental results for group IV, III-V, and IV/III-V homojunction and heterojunction TFET devices.

1.3. A Brief History of Ge-on-Si Photonic Devices

The earliest attempts to develop Ge/Si heterojunction photonic structures date back to the 1960s. In 1963, Oldham *et al*. **[44]** described a photodiode heterostructure formed by the chemical vapor deposition (CVD) growth of n-Ge on a n-Si substrate. Although the device exhibited weakly rectifying behavior and a bias-dependent photo-response up to ~2.5 μm, the isotype nature of the n-Ge/n-Si heterostructure limited the photocurrent of the fabricated devices.

Little progress was made following the initial investigations into Ge heterointegration onto Si until the early 1980s, when industrial interest was revived following the successful development and implementation of optical fiber-based telecommunications. Particularly of interest were photonic devices operating in the key communication wavelength ranges of 1.3 μm and 1.55 μm. By this time, significant advancements had

also been made in the development of epitaxial techniques, such as CVD and the non-equilibrium MBE technique. Buffer architectures had been developed to accommodate the lattice mismatch between Ge and Si, e.g., the graded $Si_{1-x}Ge_x$ buffer in which the Ge composition can be graded to gradually alter the lattice constant from that of Si (5.431 Å) to that of Ge (5.658 Å). Luryi et al. **[45]** utilized such a buffer (1.8 µm in thickness) to grow Ge on Si and demonstrate the first epitaxial Ge-on-Si vertical p-i-n photodiode. The devices exhibited quantum efficiencies as high as 40% at 1.3 µm; however, they were limited by their high dark current density, J_{DARK}, ~50 mA cm^{-2}, an approximately 500-fold increase over similar structures fabricated from bulk Ge substrates. Subsequently, the introduction of strained-layer superlattices (SLS) utilizing $Si_{1-x}Ge_x$ was proposed in order to reduce the dislocation density in the active device region. Although Kastalsky *et al*. **[46]** reported moderate success in reducing active region dislocation density and J_{DARK} by two orders of magnitude using the SLS technique, quantum efficiency and photo-response were drastically reduced to as low as 3%. In order to circumvent the challenge of prohibitively-high dislocation densities when using Ge-based active regions, researchers attempted to fabricate near-infrared (NIR) photodiodes from $Si_{1-x}Ge_x$ SLS heterostructures. Temkin *et al*. **[47]** and J. C. Bean **[48]** used differing Ge atomic percentages to realize SLS-based photodiodes that exhibited external quantum efficiencies (EQE) surpassing 10% at 1.3 µm. The best photo-response was observed in SLS heterostructures using $Si_{0.4}Ge_{0.6}$, demonstrating low J_{DARK} (7 mA cm^{-2}) and a ~300 ps pulse response. However, carrier transport across the superlattice heterointerfaces was suggested to be limiting a factor due to the required 10 V reverse bias operation.

Following this work, rapid progress was made towards $Si_{1-x}Ge_x$-based waveguide photodetectors throughout the 1990s. In 1994, Splett *et al*. **[49]** demonstrated a $Si_{1-x}Ge_x$-based waveguide-coupled photodetector by coupling a $Si_{0.98}Ge_{0.02}$ waveguide with a 20-period $Si_{0.65}Ge_{0.45}$ multi-quantum well (MQW) photodetector. The fabricated devices exhibited 11% EQE at 1.3 µm under a 7 V reverse bias, with a very low J_{DARK} of 1 mA cm^{-2}. Similar performing structures were demonstrated by Huang *et al*. **[50]** utilizing $Si_{0.5}Ge_{0.5}$ SLS heterostructures. Also in 1994, Sutter *et al*. **[51]** reported a simplified, two-step heterointegration scheme for direct Ge growth on Si substrates *via* MBE. By utilizing a low-temperature nucleation growth step followed by a high-temperature active region growth, Sutter *et al*. were able to confine lattice mismatch-induced misfit defects to within ~50 nm of the Ge/Si interface, achieving Ge-based photodetectors on-par with those demonstrated earlier by Luryi *et al*. **[45]**. As a result, the two-step Ge direct-epitaxy growth technique became a CVD industry standard **[52]**. In conjunction with the development of a selective epitaxy process (typically *via* the patterning of defined regions using Si_3N_4, followed by Ge regrowth and chemical mechanical polishing) **[53]**, the successful implementation of a direct-epitaxy scheme for Ge-on-Si materials lead to a renewed interest in pure Ge-based photonic devices on Si.

Leveraging the advances in epitaxy and fabrication techniques made in the 1990s, recent advances in Ge-on-Si waveguide-coupled photodetectors have progressed significantly beyond the performance of the earliest Ge-on-Si devices. Utilizing butt-coupled p-i-n photodetectors with application-tailored intrinsic region (absorption) thicknesses and vertical device structures, Ge-on-Si photodiodes achieving high responsivity (~1 A/W, or > 80% EQE), large bandwidths (> 30 GHz) and modest dark

currents (as low as 29 mA cm^{-2}) have been realized **[54-59]**. Due to the high responsivity and bandwidth of such devices, J. F. Liu **[20]** posited that further reduction of device dark current could be achieved *via* optimization of device side-wall passivation during processing. Table 1.2 summarizes the latest experimental results for Ge-based photodetectors integrated onto Si.

1.4. Thesis Objective and Organization

The objective of this research is to systematically and comprehensively investigate the material, optical, and energy band alignment properties of ε-Ge/$In_xGa_{1-x}As$ heterostructures integrated on GaAs and Si substrates, including: (i) the structural design and characterization as well as the strain relaxation properties of ε-Ge/$In_xGa_{1-x}As$ heterostructures; (ii) engineering of the ε-Ge/$In_xGa_{1-x}As$ heterointerface, including the energy band alignment, through alloy composition control and epitaxial strain engineering for TFET applications; and (iii), band structure engineering *via* strain engineering and its impacts on the optical properties of tensile-strained Ge thin films for group IV nanophotonics applications.

This thesis is organized in to six chapters. ***Chapter 2*** provides an introduction to the operating principles of TFETs and discusses in detail the design considerations required for TFET device design. In addition, ***Chapter 2*** provides an outline for the integration of group IV and III-V photonic devices on Si and offers an overview of several band structure engineering techniques used to enhance the optical properties and performance of Ge-based optoelectronics.

Chapter 3 presents the experimental techniques used throughout this research, including the basic principles of molecular beam epitaxy (MBE) growth and key material, optical, and heterointerface characterization methods.

Chapter 4 presents a comprehensive investigation of the structural, morphological, and energy band alignment properties of MBE-grown ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures on GaAs substrates. A wide range of Ge strain states were studied, including 0.75%, 1.6%, and 1.94% (grown on $In_{0.16}Ga_{0.84}As$, $In_{0.24}Ga_{0.76}As$, and $In_{0.29}Ga_{0.71}As$ strain templates, respectively). The ε-Ge/$In_xGa_{1-x}As$ heterointerface of these structures was examined using transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) to determine the interface quality, coherence, uniformity, and abruptness as well as the energy band alignment at the ε-Ge/$In_xGa_{1-x}As$ heterojunction, respectively, as a function of strain. Based upon these results, the suitability of ε-Ge/$In_xGa_{1-x}As$ heterostructures for TFET applications is discussed.

Chapter 5 presents the heterogeneous integration of ε-Ge/$In_xGa_{1-x}As$ heterostructures on Si substrates using III-V metamorphic buffers and the comprehensive examination of the strain relaxation, energy band alignment, and optical properties of these structures. Ge thin films with 0.82% and 1.11% strain (grown on $In_{0.11}Ga_{0.89}As$ and $In_{0.17}Ga_{0.83}As$ strain templates, respectively) are analyzed using X-ray diffraction (XRD), micro-Raman spectroscopy, and micro-photoluminescence (μ-PL) spectroscopy and were found to be in good agreement with the expected strain and optical behavior of ε-Ge. Moreover, the ε-Ge/$In_xGa_{1-x}As$ energy band alignments on Si found via XPS followed the band offset trends found in ***Chapter 4***. Based upon these results, the applicability of ε-Ge/$In_xGa_{1-x}As$

heterostructures for tunable-wavelength group IV (e-Ge)-based nanophotonics on Si is discussed.

Lastly, ***Chapter 6*** summarizes the conclusions of this work and presents the prospects for future avenues of research and investigation based upon this thesis' current findings.

Table 1.1 Performance comparison of experimental group IV and III-V TFETs.

Reference	Source	Channel	Band Alignment	Dielectric	EOT (nm)	I_{ON} (μA/μm)	V_{DS} (V)	V_{GS} (V)	V_{ON}-V_{OFF} (V)	I_{ON}/I_{OFF}	SS_{point} (mV/dec)	SS_{avg} (mV/dec)
Guangle *et al.* IEDM, 2012 **[10]**	GaSb	InAs	Broken	Al_2O_3/HfO_2	1.3	380	1	1	2	7500	200	520
Guangle *et al.* IEDM, 2012 **[10]**	GaSb	InAs	Broken	Al_2O_3/HfO_2	1.3	180	0.5	0.5	1.5	6000	200	400
Mohata *et al.* VLSI, 2012 **[42]**	$GaAs_{0.35}Sb_{0.65}$	$In_{0.7}Ga_{0.3}As$	Staggered	Al_2O_3/HfO_2	2	135	0.5	1	1.5	27,000	169	350
Mohata *et al.* VLSI, 2012 **[42]**	$GaAs_{0.4}Sb_{0.6}$	$In_{0.65}Ga_{0.35}As$	Staggered	Al_2O_3/HfO_2	2	78	0.5	1	1.5	15,000	179	--
Mohata *et al.* IEDM, 2011 **[39]**	$GaAs_{0.5}Sb_{0.5}$	$In_{0.53}Ga_{0.47}As$	Staggered	Al_2O_3/HfO_2	1.5	60	0.75	1	1.5	>1,000	~300	--
Han *et al.* EDL, 2010 **[41]**	$In_{0.7}Ga_{0.3}As$	$In_{0.7}Ga_{0.3}As$	Homo-junction	HfO_2	1.2	50	1.05	2	--	>10,000	86	380
Mohata *et al.* IEDM, 2011 **[39]**	$In_{0.7}Ga_{0.3}As$	$In_{0.7}Ga_{0.3}As$	Homo-junction	Al_2O_3/HfO_2	1.5	60	0.75	1	1.5	6,000	~200	--
Mookerjea *et al.* IEDM, 2009 **[40]**	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	Homo-junction	Al_2O_3	4.5	24	0.75	1	1.5	10,000	~200	--
Dewey *et al.* IEDM, 2011 **[18]**	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	Homo-junction	$TaSiO_x$	1.1	5	0.3	0.8	0.9	70,000	58	190
Bijesh *et al.* IEDM, 2013 **[43]**	$GaAs_{0.18}Sb_{0.82}$	$In_{0.9}Ga_{0.1}As$	Staggered	Al_2O_3/HfO_2	2	740	0.5	2	2.5	~40	~300	--
Guo *et al.* JAP, 2013 **[15]**	Ge	$In_{0.53}Ga_{0.47}As$	Staggered	Al_2O_3	2.5	0.4	0.2	2	3	~300	177	--
Han *et al.*, AIP Adv., 2015 **[37]**	$Ge_{0.93}Sn_{0.07}$	$Ge_{0.93}Sn_{0.07}$	Homo-junction	HfO_2/SiO_2	--	18	-0.5	-1.5	2.5	~10	--	--

Table 1.2 Performance comparison of waveguide-coupled Ge photodiodes epitaxially grown on Si. All data is reported for -1V reverse bias, unless otherwise specified. Adapted from **[20]**.

Reference	Responsivity at 1.55 μm (A/W)		3dB Bandwidth (GHz)		J_{DARK} (mA/cm^2)	Device Design
	Maximum	Zero Bias	Maximum	Zero Bias		
Vivien *et al.* Opt. Exp., 2009 **[54]**	1.1	--	37 (at -3V)	17.5	1.6×10^4	Butt *p-i-n*
Feng *et al.* Opt. Exp., 2009 **[55]**	1 (at -4V)	0.2	42 (at -4V)	12	60	Butt *p-i-n*
Chen *et al.* Opt. Exp., 2009 **[56]**	< 1.1	--	50 (at -5V)	--	8900 (at -5V)	Bottom MSM (metal-semiconductor-metal)
Liao *et al.* Opt. Exp., 2011 **[57]**	0.95	--	36	--	29	Bottom *p-i-n*
Vivien *et al.* Opt. Exp., 2012 **[58]**	0.8	0.78	> 67	40 Gb/s	8×10^4	Butt
Novack *et al.* Opt. Exp. 2013 **[59]**	0.75 (at -2V)	--	60 (at -2V)	--	3750	Bottom *p-i-n*

References

[1] E. J. Nowak, Maintaining the Benefits of CMOS Scaling When Scaling Bogs Down, *IBM J. Res. Dev.* **46**, 169-180 (2002).

[2] A. M. Ionescu and H. Riel, Tunnel Field-Effect Transistors as Energy-Efficient Electronic Switches, *Nature* **479**, 329-337 (2011).

[3] A. C. Seabaugh and Q. Zhang, Low-Voltage Tunnel Transistors for Beyond CMOS Logic, *In IEEE Proc.* **98**, 2095-2110 (2010).

[4] Y. Zhu and M. K. Hudait, Low-Power Tunnel Field-Effect Transistors Using Mixed As and Sb Based Heterostructures, *Nanotechnol. Rev.* **2**, 637-678 (2013).

[5] R. Asra, M. Shrivastava, K. V. R. M. Murali, R. K. Pandey, H. Gossner, and R. V. Ramgopal, A Tunnel FET for VDD Scaling Below 0.6 V With a CMOS-Comparable Performance, *IEEE Trans. Electron Devices* **58**, 1855-1863 (2011).

[6] K. Boucart and A. M. Ionescu, Double-Gate Tunnel FET with High-κ Gate Dielectric, *IEEE Trans. Electron Devices* **54**, 1725-1733 (2007).

[7] S. M. Sze, *Physics of Semiconductor Devices*, 3rd Ed., Wiley: New York (2007).

[8] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, Role of InAs and GaAs Terminated Heterointerfaces at Source/Channel on the Mixed As-Sb Staggered Gap Tunnel Field Effect Transistor Structures Grown by Molecular Beam Epitaxy, *J. Appl. Phys.* **112**, 024306-1–024306-16 (2012).

[9] Y. Zhu, M. K. Hudait, D. K. Mohata, B. Rajamohanan, S. Datta, D. Lubyshev, J. M. Fastenau, and A. K. Liu, Structural, Morphological, and Defect Properties of Metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ P-Type Tunnel Field Effect Transistor Structure

Grown by Molecular Beam Epitaxy, *J. Vac. Sci. Technol. B* **31**, 041203-1–041203-7 (2013).

[10] Z. Guangle, R. Li, T. Vasen, M. Q. S. Chae, Y. Lu, Q. Zhang, H. Zhu, J. M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, Novel Gate-Recessed Vertical InAs/GaSb TFETs With Record High I_{ON} of 180 μA/μm at V_{DS} = 0.5 V, *In IEEE Int. Electron Devices Meet.*, 32.6.1-32.6.4 (2012).

[11] Y. Zhu, N. Jain, D. H. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, Structural Properties and Band Offset Determination of P-Channel Mixed As/Sb Type-II Staggered Gap Tunnel-Field Effect Transistor Structure, *Appl. Phys. Lett.* **101**, 112106-1–112106-4 (2012).

[12] Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M.K. Hudait, Band Offset Determination of Mixed As/Sb Type-II Staggered Gap Heterostructure for N-Channel Tunnel Field Effect Transistor Applications, *J. Appl. Phys.* **113**, 024319-1–024319-5 (2013).

[13] Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, Defect Assisted Band Alignment Transition From Staggered to Broken Gap in Mixed As/Sb Tunnel Field Effect Transistor Heterostructure, *J. Appl. Phys.* **112**, 094312-1–094312-9 (2012).

[14] D. K. Mohata, B. Rajamohanan, T. Mayer, M. K. Hudait, J. M. Fastenau, D. Lubyshev, A. K. Liu, and S. Datta, Barrier-Engineered Arsenide-Antimonide Heterojunction Tunnel FETs With Enhanced Drive Current, *IEEE Electron Device Lett.* **33**, 1568-1570 (2012).

[15] P. Guo, Y. Yang, Y. Cheng, G. Han, J. Pan, Ivana, Z. Zhang, H. Hu, Z. Xiang Shen, C. Kean Chia, and Y.-C. Yeo, Tunneling Field-Effect Transistor With Ge/$In_{0.53}Ga_{0.47}As$ Heterostructure as Tunneling Junction, *J. Appl. Phys.* **113**, 094502-1–094502-9 (2013).

[16] Y. Zhu, D. Maurya, S. Priya, and M. K. Hudait, Tensile-Strained Nanoscale Ge/$In_{0.16}Ga_{0.84}As$ Heterostructure for Tunnel Field-Effect Transistor, *ACS Appl. Mater. Interfaces* **6**, 4947-4953 (2014).

[17] Y. Bai, K. E. Lee, C. Cheng, M. L. Lee, and E. A. Fitzgerald, Growth of Highly Tensile-Strained Ge on Relaxed $In_xGa_{1-x}As$ by Metal-Organic Chemical Vapor Deposition, *J. Appl. Phys.* **104**, 084518-1–084518-9 (2008).

[18] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, Fabrication, Characterization, and Physics of III-V Heterojunction Tunneling Field Effect Transistors (H-TFET) for Steep Sub-Threshold Swing, *In IEDM Tech. Dig.*, 33.6.1-33.6.4 (2011).

[19] D. A. B. Miller, Device Requirements for Optical Interconnects to Silicon Chips, *Proc. IEEE* **97**, 1166-1185 (2009).

[20] J. F. Liu, Monolithically Integrated Ge-on-Si Active Photonics, *Photonics* **1**, 162-197 (2014).

[21] D. A. B. Miller, Physical Reasons for Optical Interconnection, *Int. J. Optoelectronics* **11**, 155-168 (1997).

[22] D. A. B. Miller, Optical Interconnects to Silicon, *IEEE J. Sel. Top. Quantum Electron.* **6**, 1312-1317 (2000).

[23] D. Liang and J. E. Bowers, Recent Progress in Lasers on Silicon, *Nat. Photonics* **4**, 511-517 (2010).

[24] J. F. Liu, X. Sun, R. Camacho-Aguilera, L. C. Kimerling, and J. Michel, Ge-on-Si Laser Operating at Room Temperature, *Opt. Lett.* **35**, 679-681 (2010).

[25] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, and J. Michel, An Electrically Pumped Germanium Laser, *Opt. Express* **20**, 11316-11320 (2012).

[26] S. Cho, B.-G. Park, C. Yang, S. Cheung, E. Yoon, T. I. Kamins, S. J. B. Yoo, and J. S. Harris, Room-Temperature Electroluminescence from Germanium in an $Al_{0.3}Ga_{0.7}As$/Ge Heterojunction Light-Emitting Diode by Γ-Valley Transport, *Opt. Express* **20**, 14921-14927 (2012).

[27] J.-M. Fedeli, B. B. Bakir, N. Olivier, Ph. Grosse, L. Grenouillet, E. Augendre, P. Philippe, K. D. Bordel, and J. Harduin, InP on SOI Devices for Optical Communication and Optical Network on Chip, *Proc. SPIE* **7942**, 79420O-1—79420O-9 (2011).

[28] G.-H. Duan, C. Jany, A. Le Liepvre, A. Accard, M. Lamponi, D. Make, P. Kaspar, G. Levaufre, N. Girard, F. Lelarge, J.-M. Fedeli, S. Messaoudene, D. Bordel, and S. Olivier, Hybrid III-V on Silicon Lasers for Photonic Integrated Circuits on Silicon, *Proc SPIE* **9002**, 90020X-1—90020X-6 (2014).

[29] J. Quinn, G. Kawamoto, and B. McCombe, Subband Spectroscopy by Surface Channel Tunneling, *Surf. Sci.* **73**, 190-196 (1978).

[30] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, A New Three-Terminal Tunnel Device, *IEEE Electron Device Lett.* **8**, 347-349 (1987).

[31] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, A Band to Band Tunneling MOS Device B^2T-MOSFET, *in IEDM Tech Dig.*, 402-405 (1998).

[32] W. Reddick and G. Amaratunga, Silicon Surface Tunnel Transistor, *Appl. Phys. Lett.* **67**, 494-496 (1995).

[33] W. Hansch, C. Fink, J. Schulze, and I. Eisele, A Vertical MOS-gated Esaki Tunneling Transistor in Silicon, *Thin Solid Films* **369**, 387-389 (2000).

[34] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors, *Phys. Rev. Lett.* **93**, 196805-1—196805-4 (2004).

[35] T. Krishnamohan, K. Donghyun, S. Raghunathan, and K. Saraswat, Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) with Record High Drive Currents and < 60mV/dec Subthreshold Slope, *in IEEE Conference Proceedings of the International Electron Devices Meeting (IEDM)* **(IEEE, 2008)**, 1-3.

[36] K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. D. Meyer, Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs, *IEEE T. Electron Dev.* **59**, 292-301 (2012).

[37] G. Han, Y. Wang, Y. Liu, H. Wang, M. Liu, C. Zhang, J. Zhang, B. Cheng, and Y. Hao, Relaxed Germanium-Tin P-Channel Tunneling Field-Effect Transistors Fabricated on Si: Impacts of Sn Composition and Uniaxial Tensile Strain, *AIP Advances* **5**, 057145-1—057145-12 (2012).

[38] S. Wirths, A. T. Tiedemann, Z. Ikonic, P. Harrison, B. Hollander, T. Stoica, G. Mussler, M. Hartmann, D. Grutzmacher, D. Buca, and S. Mantl, Band Engineering and

Growth of Tensile Strained Ge/(Si)GeSn Heterostructure Tunnel Field Effect Transistors, *Appl. Phys. Lett.* **102**, 192103-1—192103-4 (2013).

[39] D. K. Mohata, R. Bijesh, S. Majumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, Demonstration of MOSFET-like On-Current Performance in Arsenide/Antimonide Tunnel FETs with Staggered Hetero-junctions for 300 mV Logic Applications, *in IEEE Conference Proceedings of the International Electron Devices Meeting (IEDM)* (**IEEE, 2011**), 781-784.

[40] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu, and S. Datta, Experimental Demonstration of 100 nm Channel Length $In_{0.53}Ga_{0.47}As$-Based Vertical Inter-Band Tunnel Field Effect Transistors (TFETs) for Ultra-Low-Power Logic and SRAM Applications, *in IEEE Conference Proceedings of the International Electron Devices Meeting (IEDM)* **(IEEE, 2009)**, 1-3.

[41] Z. Han, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, $In_{0.53}Ga_{0.47}As$ Tunneling Field-Effect Transistors with an I_{ON} of 50 μA/μm and a Subthreshold Swing of 86 mV/dec Using HfO_2 Gate Oxide, *IEEE Electron Device Lett.* **31**, 1392-1394 (2010).

[42] D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan, and S. Datta, Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States Enabling Heterojunction Tunnel FETs with High Drive Current and High On-Off Ratio, *in IEEE Symposium on VLSI Technology (VLSI)* **(IEEE, 2012)**, 53-54.

[43] R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V. Nguyen, D. Gundlach, C. A. Richter, J. Maier, K. Wang, T. Clarke, J. M. Fastenau, D. Loubychev, W. K. Liu, V. Narayanan, and S. Datta, Demonstration of InGaAs/GaAsSb Near Broken-Gap Tunnel FET with I_{ON}=740μA/μm, G_m=700μS/μm and Gigahertz Switching Performance at V_{DS}=0.5V, *in IEEE International Electron Devices Meeting (IEDM)* **(IEEE, 2013)**, 687-690.

[44] W. G. Oldham, A. R. Riben, D. I. Feucht, and A. G. Milnes, Epitaxial Growth of Germanium on Silicon, *J. Electrochem. Soc.* **110**, 53C (1963).

[45] S. Luryi, A. Kastalsky, and J. C. Bean, New Infrared Detector on a Silicon Chip, *IEEE T. Electron Dev.* **31**, 1135-1139 (1984).

[46] A. Kastalsky, S. Luryi, J. C. Bean, and T. T. Sheng, *in Proceedings of the Electrochemical Society* **(Electrochem. Soc., 1985)**, 406.

[47] H. Temkin, T. P. Pearsall, J. C. Bean, R. A. Logan, and S. Luryi, Ge_xSi_{1-x} Strained-Layer Superlattice Waveguide Photodetectors Operating Near 1.3 μm, *Appl. Phys. Lett.* **48**, 963-965 (1986).

[48] J. C. Bean, Strained-Layer Epitaxy of Ge_xSi_{1-x}/(Si, Ge): Heterojunction Technology with Silicon-Based Materials, *in Proceedings of the 1st International Symposium on Si Molecular Beam Epitaxy* **(Electrochem. Soc., 1985)**, 337.

[49] A. Splett, T. Zinke, K. Petermann, E. Kasper, H. Kibbel, H.-J. Herzog, and H. Presting, Integration of Waveguides and Photodetectors in SiGe for 1.3 μm Operation, *IEEE Photonics Technol. Lett.* **6**, 59-61 (1994).

[50] F. Y. Huang, X. Zhu, M. O. Tanner, and K. L. Wang, Normal-Incidence Strained-Layer Superlattice $Ge_{0.5}Si_{0.5}$/Si Photodiodes Near 1.3 μm, *Appl. Phys. Lett.* **67**, 566-568 (1995).

[51] P. Sutter, U. Kafader, and H. von Kanel, Thin Film Photodetectors Grown Epitaxially on Silicon, *Solar Energy Mater. Sol. Cells* **31**, 541-547 (1994).

[52] S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, High Quality Germanium Photodiodes Integrated on Silicon Substrates Using Optimized Relaxed Graded Buffers, *Appl. Phys. Lett.* **73**, 2125-2127 (1998).

[53] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, Near Infrared Light Detectors Based on UHV-CVD Epitaxial Ge on Si (100), *Mater. Res. Soc. Symp. Proc.* **486**, 193-198 (1998).

[54] L. Vivien, J. Osmond, J. M. Fédéli, M. M. Delphine, P. Crozat, J. F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, 42 GHz p-i-n Germanium Photodetector Integrated in a Silicon-on-Insulator Waveguide, *Opt. Express* **17**, 6252–6257 (2009).

[55] D. Feng, S. Liao, P. Dong, N. N. Feng, H. Liang, D. W. Zheng, C. C. Kung, J. Fong, R. Shafiiha, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, High-Speed Ge Photodetector Monolithically Integrated with Large Cross-Section Silicon-on-Insulator Waveguide, *Appl. Phys. Lett.* **95**, 261105-1—261105-3 (2009).

[56] L. Chen, K. Preston, S. Manipatruni, and M. Lipson, Integrated GHz Silicon Photonic Interconnect with Micrometer-Scale Modulators and Detector, *Opt. Express* **18**, 15248–15256 (2009).

[57] S. Liao, N.-N. Feng, D. Feng, P. Dong, R. Shafiiha, C.-C. Kung, H. Liang, W. Qian, Y. Liu, J. Fong, J. E. Cunningham, Y. Luo, and M. Asghari, 36 GHz Submicron Silicon Waveguide Germanium Photodetector, *Opt. Express* **19**, 10967–10972 (2011).

[58] L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J. M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, and J. M. Fédéli, Zero-Bias 40 Gbit/s Germanium Waveguide Photodetector on Silicon, *Opt. Express* **20**, 1096–1101 (2012).

[59] A. Novack, M. Gould, Y. Yang, Z. Xuan, M. Streshinsky, Y. Liu, G. Capellini, A. E. J. Lim, G.Q. Lo, T. Baehr-Jones, and M. Hochberg, Germanium Photodetector with 60 GHz Bandwidth Using Inductive Gain Peaking, *Opt. Express* **21**, 28387–28393 (2013).

Chapter 2 – Design Considerations for Tensile-Strained Ge/$In_xGa_{1-x}As$ Multifunctional Devices

2.1 ε-Ge/$In_xGa_{1-x}As$ Tunnel Field-Effect Transistors (TFETs)

2.1.1. Fundamental Operation of TFET Devices

As noted in ***Chapter 1***, tunneling field-effect transistors (TFETs) are fundamentally different to conventional metal-oxide-semiconductor field-effect transistor (MOSFET) technology in that TFETs operate on the band-to-band tunneling (BTBT) injection of carriers from the source into the channel, as opposed to the thermionic injection principle upon which standard MOSFETs operate. As a result, the basic TFET device architecture deviates from current Si-based MOSFETs. A standard TFET is designed as a gated p^+-i-n^+ diode in which the gate lies over the intrinsic region. One benefit of the gated p^+-i-n^+ structure is that it is intrinsically reversed biased, resulting in ultra-low leakage current. Fig. 2.1 (a) shows the schematic cross-section of an *n*-type TFET device with applied source (V_S), gate (V_{GS}), and drain (V_{DS}) voltages **[1-3]**. For an *n*-type TFET, the p^+ region is considered the source, the intrinsic region serves as the channel, and the n^+ region is considered the drain. The schematic energy band diagrams for *n*-type and *p*-type TFET devices are shown in Figs. 2.1 (b) and 2.1 (c), respectively, wherein the OFF-state is represented by the red lines and the ON-state is represented by the green lines **[1-3]**. As shown in Fig. 2.1 (b), when the applied gate-source voltage bias is zero (*i.e.*, $V_{GS} = 0$), the BTBT process is suppressed due to the energy barrier (E_{beff}) between the source valence band maximum (E_V) and the channel conduction band minimum (E_C). As a result, there is a distinct lack of available states in the channel conduction band that are at an appropriate energy level to accept electrons tunneling from the valence band. Moreover, the OFF-

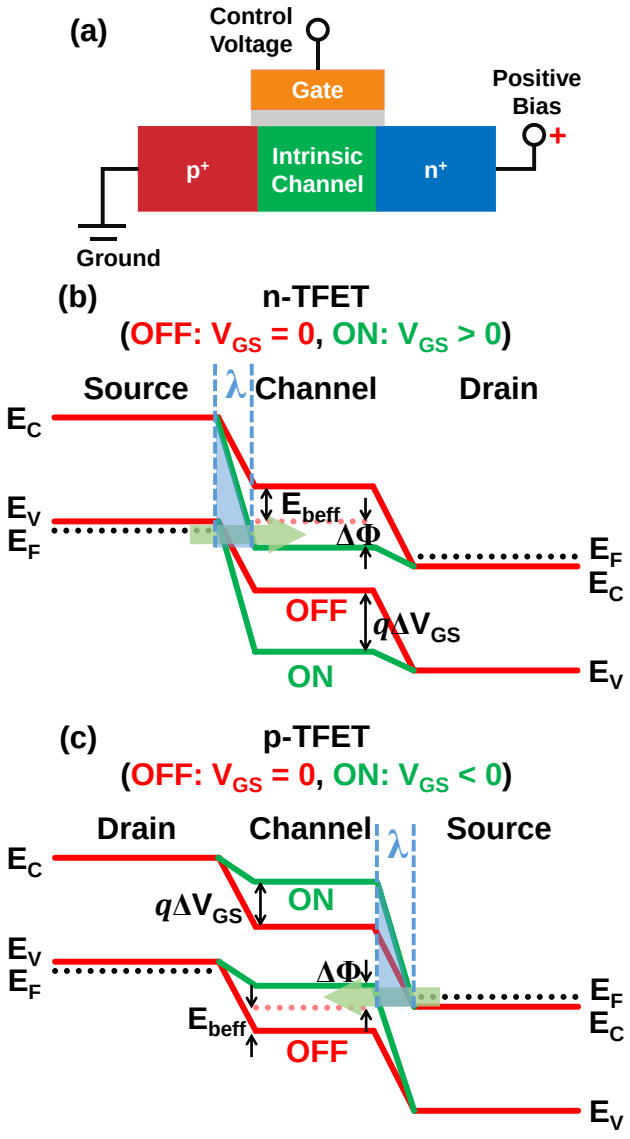

Figure 2.1 (a) Schematic cross-section of a p^+-i-n^+ TFET device with applied source (V_S), gate (V_{GS}), and drain (V_{DS}) voltages. (b) Schematic energy band diagram for an n-TFET in the OFF-state ($V_{GS} = 0$, $V_{DS} \geq 0$, red lines) and in the ON-state ($V_{GS} > 0$, $V_{DS} > 0$, green lines). (c) Schematic energy band diagram for a p-TFET in the OFF-state ($V_{GS} = 0$, $V_{DS} \leq 0$, red lines) and in the ON-state ($V_{GS} < 0$, $V_{DS} < 0$, green lines).

state p^+-i-n^+ diode leakage current between source and drain at zero bias is exceedingly low due to the source-channel energy barrier. As a positive V_{GS} is applied to the gate, the energy band alignment is altered, as shown by the green lines in Fig. 2.1 (b) **[1-3]**. The energy bands of the intrinsic channel region are pushed down by $q\Delta V_{GS}$ for increasing positive V_{GS}. At the point where the channel conduction band minimum is pushed below the source valence band maximum, E_{beff} no longer restricts the BTBT tunneling of electrons from the source to the channel, and the tunneling barrier width (λ) is significantly reduced. As a result, electrons from occupied states in the source valence band tunnel to unoccupied states in the channel conduction band within the energy window ($\Delta\Phi$) shown in Fig. 2.1 (b), thereby contributing to the tunneling current collected by the drain and thus the I_{ON} of the device **[1-3]**.

Similarly, Fig. 2.1 (c) shows a schematic energy band diagram for a *p*-type TFET device, which can be conceptualized as a mirror image of an *n*-type TFET **[1-3]**. In the case of symmetrically doped p^+-i-n^+ structures, this gives rise to ambipolar TFET behavior as a result of conduction and current flow for both negative and positive V_{GS}, which will be discussed further in ***Section 2.1.3***. As shown in Fig. 2.1 (c), the p^+ region is considered the drain, the n^+ region is considered the source, and the intrinsic region remains the channel for a *p*-type TFET structure. Comparing Figs. 2.1 (b) and 2.1 (c), one can see that the OFF-state energy band alignment is the same for both *p*- and *n*-type TFETs **[1-3]**. Likewise, the BTBT process is suppressed in *p*-type TFET devices with zero applied V_{GS} due to the energy separation between E_C in the source and E_V in the intrinsic channel. For *p*-type TFETs, the application of a negative V_{GS} pulls the energy bands of the intrinsic channel up, resulting in a conduction channel for tunneling carriers

once E_V in the channel is lifted above E_C in the source [1-3]. Mirroring *n*-type TFETs, conduction in *p*-type TFETs occurs as holes in the source conduction band tunnel into empty states in the channel valence band and are collected by the drain [3].

2.1.1.1. ON-State Current (I_{ON})

I_{ON} in TFET devices is primarily determined by the tunneling probability for the BTBT tunneling of carriers from source to channel [2]. As shown by the blue shaded region in Figs. 2.1 (b) and 2.1 (c), the tunneling barrier in a TFET structure can be approximated using a triangular potential [2, 3]. The tunneling probability can then be calculated using the Wentzel-Kramers-Brillouin (WKB) approximation given by [3, 4]:

$$T_{WKB} \approx e^{-2\int_0^w |k(x)| dx} \tag{2.1}$$

where $|k(x)|$ is the absolute value of the wave vector of a carrier inside the barrier, and $x = 0$ and $x = w$ are the spatial boundaries of the triangular potential barrier, as shown in Fig. 2.2 (a) [3]. The wave vector of a carrier inside a triangular potential barrier can be expressed as [3]:

$$k(x) = \sqrt{\frac{2m^*}{h^2}(V - E_C)} \tag{2.2}$$

where V is the potential energy of the carrier, m^* is the carrier effective mass, and h is Planck's constant. When considering the BTBT tunneling process, it is assumed that the tunneling carrier's potential is equal to the bottom of the energy barrier while the varying energy barrier height can be expressed in terms of a spatially varying electric **E** field. Thus, the wave vector of a carrier inside the triangular potential can be reduced to [3]:

$$k(x) = \sqrt{\frac{2m^*}{h^2}(-q\boldsymbol{E}x)} \tag{2.3}$$

Substituting (2.3) into (2.1) results in [3]:

$$T_{WKB} \approx e^{-2\int_0^{x_2}\sqrt{\frac{2m^*}{\hbar^2}(-qEx)}dx} \quad . \tag{2.4}$$

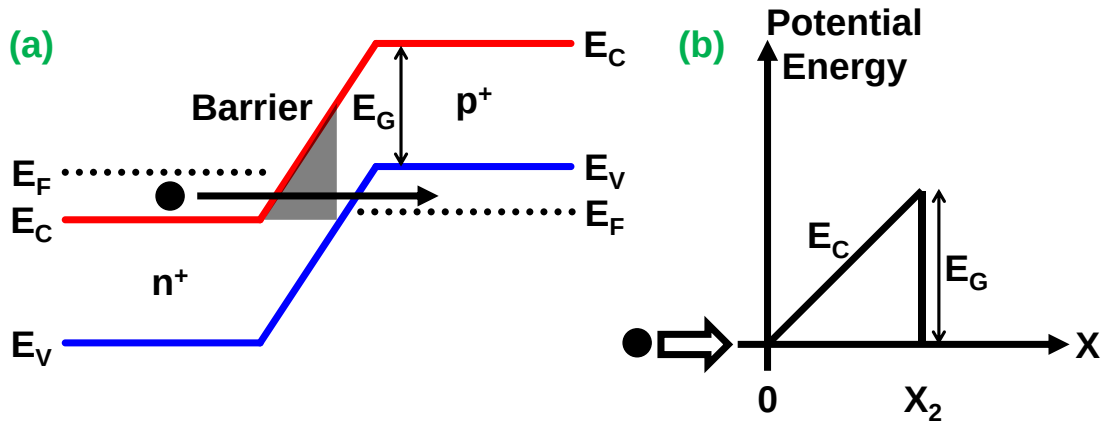

Figure 2.2 (a) Schematic energy band diagram showing a carrier tunneling from source to channel through a triangular potential barrier. (b) Representation of the triangular potential barrier a carrier must overcome to contribute to tunneling current.

triangular potential barrier having a uniform electric field ($\mathcal{E} = E_G/qx$) as shown in Fig. 2.2 (b), the general expression for the BTBT tunneling probability can be simplified to **[3]**:

$$T_{WKB} \approx e^{\frac{-4\sqrt{2m^*}E_G^{3/2}}{3q\hbar E}} \quad . \tag{2.5}$$

Although (2.5) is the general expression for the BTBT tunneling probability, it can be further generalized for TFET applications by accounting for the height and width of the tunneling barrier, ($\Delta\Phi + E_G$) and λ, respectively, in a TFET device. **E** in (2.5) can then be expressed as $\boldsymbol{E} = (\Delta\Phi + E_G)/\lambda$, allowing (2.5) to be expressed as **[3]**:

$$T_{WKB} \approx e^{\frac{-4\lambda\sqrt{2m^*}E_G^{3/2}}{3q\hbar(\Delta\Phi + E_G)}} \tag{2.6}$$

where E_G is the material bandgap. It follows from this analysis that ($\Delta\Phi + E_G$) is the triangular potential barrier height that carriers must overcome to tunnel from the source

to the channel. In order for significant BTBT to occur, several requirements must be met, including: (i) an availability of states in the source from which to tunnel; (ii) an availability of states in the channel into which carriers can tunnel; (iii) a sufficiently narrow tunneling barrier width; and (iv) momentum conservation for tunneling carriers **[5]**. Condition (iv) becomes increasingly relevant when using indirect bandgap materials, such as Ge, in TFET design. In the case of indirect semiconductors, lattice phonons are required for the conservation of momentum during tunneling, which results in the E_G term in (2.6) being replaced by E_G-E_P, where E_P is the phonon energy **[5]**. Additionally, the effective mass term m^* must be replaced by the reduced effective mass term $m^*_{\Gamma X}$ at the gamma point. A direct consequence of this is that BTBT current will be reduced for indirect bandgap semiconductors used in TFET devices. Furthermore, one can also find from (2.6) that the most effective method for increasing tunneling current is to reduce m^* and λ.

2.1.1.2. OFF-State Current (I_{OFF})

The dominate leakage current mechanism in an ideal TFET in the OFF-state is the p^+-i-n^+ leakage diffusion current between the source and the drain. However, in practice, there are several mechanisms that contribute to OFF-state leakage current in a TFET **[6]**: (i) leakage through the gate oxide; (ii) Shockley-Read-Hall generation-recombination (SRH G-R) in the depletion regions of the heavily doped source and drain; (iii) direct and defect-assisted tunneling; and (iv) ambipolar conduction. This subsection will focus on the less common later three mechanisms.

Fig. 2.3 (a) highlights the SRH G-R contribution to leakage current **[6]**. Commonly found in TFETs using low bandgap materials **[7, 8]**, SRH G-R is strongly correlated with

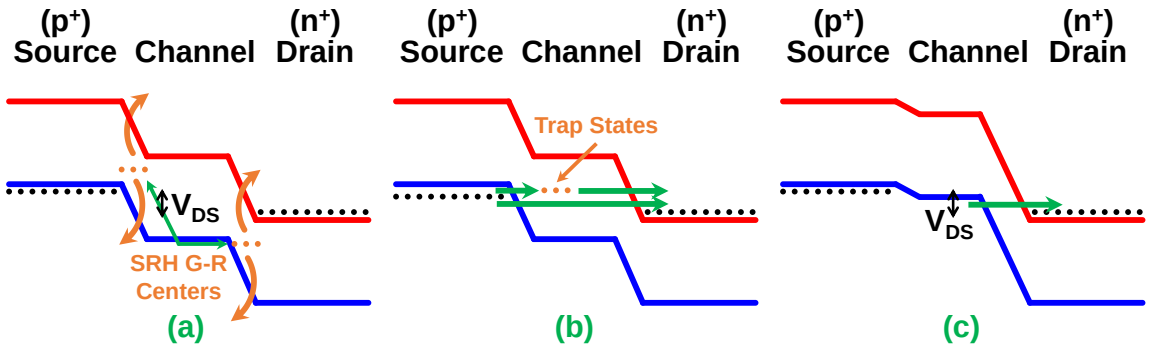

Figure 2.3 Schematic energy band diagrams for a n-TFET in the OFF-state showing contribution to the leakage current from: (a) Shockley-Read-Hall generation in the source and drain regions; (b) direct and defect-assisted tunneling from source to drain; and (c), ambipolar conduction in a symmetric TFET device.

temperature due to the dependence of SRH G-R on a material's intrinsic carrier concentration, n_i **[7, 8]**. It is well known that n_i is proportional to bandgap and temperature, *i.e.* $n_i \propto e^{-E_G/2kT}$, where E_G is the material's bandgap, k is the Boltzmann constant, and T is the temperature **[7]**. As a result, SRH G-R leakage current increases exponentially with temperature, degrading TFET device performance significantly at higher operating temperatures. This behavior has been demonstrated experimentally for n-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ TFETs, wherein the I_{ON}/I_{OFF} ratio was found to be reduced by several orders of magnitude within an operating temperature range of 25°C to 125°C **[8]**.

Fig. 2.3 (b) illustrates the defect-assisted (and direct) tunneling contributions to TFET leakage current **[6]**. As shown in Fig 2.3 (b), interfacial defects at the source/channel heterointerface result in the introduction of fixed charge that can act as traps within the bandgap or raise/lower the interfacial energy band alignment **[9, 10]**. If a significant number of defect states exist at the interface, the band alignment can be altered from a

type-II, staggered-gap band alignment to a type-III, broken-gap band alignment, thereby causing conduction in the OFF-state and impairing gate control over the device. This type of leakage current behavior has been demonstrated experimentally for mixed As-Sb-based TFET heterostructures, and is an important metric to consider for all heterojunction TFET architectures **[9, 10]**.

Lastly, Fig. 2.3 (c) demonstrates the ambipolar current contribution to TFET OFF-state leakage current **[6]**. As discussed earlier in the chapter, symmetrically doped p^+-i-n^+ TFET structures exhibit significant conduction when either positive or negative V_{GS} is applied to the gate due to the symmetric nature of the energy bands from source to drain. ***Section 2.1.3*** will further discuss ambipolar behavior and methods to control or suppress the contribution of ambipolar current to OFF-state current.

2.1.1.3. Subthreshold Slope (*SS*)

As discussed in ***Chapter 1***, the predicted lower *SS* of TFET devices is one of their key advantages over conventional MOSFET technology. One can find from Figs. 2.1 (b) and 2.1 (c) that the energy window, $\Delta\Phi$, created as a result of the overlapping E_C and E_V acts as a filter for the higher and lower energy tails of the carrier distributions in the source and drain regions **[2]**. The net effect of this filtering is that the TFET behaves as a MOSFET with a decreased thermal factor (kT/q), thereby allowing TFETs to achieve *SS* lower than 60 mV/dec at T = 300 K **[3]**.

The expression for the tunneling current for a reverse-biased *p*-*n* junction, given below, can be used to derive a general expression for the *SS* of a TFET deice **[3, 5, 11]**:

$$I = aV_{eff}e^{-\frac{b}{E}} \tag{2.7}$$

where V_{eff} is the applied bias at the tunnel junction, $\boldsymbol{E}$ is the electrical field, and a and b are coefficients determined by the cross-sectional device area and the devices' material properties, *i.e.* **[6, 11]**:

$$a = \frac{Aq^3\sqrt{2m^*/E_G}}{4\pi^2\hbar^2} \tag{2.8}$$

and

$$b = \frac{4\sqrt{m^*}E_G^{2/3}}{3q\hbar^2} \quad . \tag{2.9}$$

Utilizing the *SS* definition provided by (1.2) in Chapter 1, the *SS* for a TFET device can be rewritten as:

$$SS = \ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{GS}} + \frac{E+b}{E^2}\frac{dE}{dV_{GS}}\right]^{-1} . \tag{2.10}$$

Examining (2.10), one can find that unlike a conventional MOSFET, the *SS* of a TFET is independent of operating temperature (i.e., there is no kT/q thermal factor) in the ideal case **[6, 11]**. Rather, the ability of the gate voltage, V_{GS}, to modulate V_{eff} (reflected by the term dV_{eff}/dV_{GS}) is at the heart of TFET *SS* and energy-efficient device operation. This suggests that thin device bodies and scaled high-κ gate dielectrics are necessary to ensure that the applied gate bias can efficiently couple with the channel and directly modulate the channel energy band alignment **[11]**. Furthermore, for highly-scaled gate oxides in which the equivalent oxide thickness (EOT) approaches 1 nm, dV_{eff}/dV_{GS} in (2.10) is approximately unity, thus the expression for TFET *SS* becomes inversely proportional to V_{GS}. Fig. 2.4 (a) **[5]** highlights this behavior, wherein the increase in *SS* as a function of increasing V_{GS} is one of the primary differences between TFET and MOSFET operation. Also shown in Fig. 2.4 (a) is the effect of EOT on the *SS*

characteristics of a TFET device. Additionally, Fig. 2.4 (b) **[12]** shows the difference in subthreshold characteristics between a TFET and conventional MOSFET by plotting the transfer characteristics (I_{DS} *vs.* V_{GS}) of each. One can find from Fig. 2.4 (b) that unlike the MOSFET, the *SS* of a TFET device is not constant as a function of V_{GS} (as previously mentioned), and instead exhibits lower *SS* at lower V_{GS} and higher *SS* at higher V_{GS}. Moreover, this behavior has been observed experimentally **[13]** as well as in device simulation **[14, 15]**.

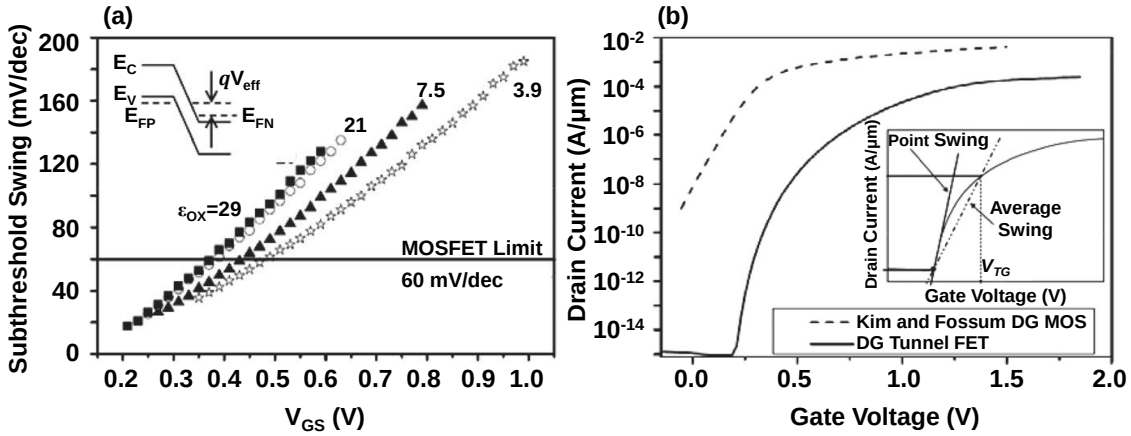

Figure 2.4 (a) Numerical simulation of the dependence of TFET point subthreshold slope (SS_{pt}) on gate voltage up to the threshold voltage (V_{TH}) of the device. Different curves represent different gate dielectric constants. The inset depicts a p^+-n^+ tunnel junction's energy band diagram under applied bias, V_{eff}. (b) Qualitative comparison of MOSFET (dashed) and TFET (solid) transfer characteristics (I_{DS}-V_{GS}) showing a clear dependence of SS_{pt} on the applied gate voltage for the TFET device. The inset shows the definitions of SS_{pt} and average SS (SS_{avg}), taken as the steepest *SS* on the I_{DS}-V_{GS} curve and the average *SS* from turn-on to V_{TH}, respectively **[5, 16]**. Used with permission of Nanotechnology Reviews.

As a result of the strong coupling between *SS* and V_{GS}, two definitions for *SS* have arisen in the literature, *i.e.*: (i) point *SS* (SS_{pt}); and (ii), average *SS* (SS_{avg}) **[16]**. The inset of Fig. 2.4 (b) **[5, 16]** illustrates the difference between SS_{pt} and SS_{avg}. One can find from the inset of Fig. 2.4 (b) that SS_{pt} is taken as the lowest possible *SS* value from the transfer characteristics, typically at the onset of applied gate bias. SS_{avg}, on the other hand, is taken from the point at which the device reaches its ON-state (up to V_{TH}) **[5]**, **[6]**, **[17]**, and is given by:

$$SS_{avg} = \frac{V_{TH} - V_{OFF}}{\log(I_{TH}/I_{OFF})} \tag{2.11}$$

where I_{TH} is the current value when $V_{GS} = V_{TH}$. Therefore, due to the stronger correlation between SS_{avg} and the ON-state of a device, SS_{avg} is considered to be the more important metric when comparing the transfer and subthreshold characteristics of different TFET designs.

2.1.2. Engineering of TFET Effective Tunneling Barrier Height (E_{beff}) and Tunneling Width (λ)

Fig. 2.5 demonstrates the three conventional TFET energy band diagrams based upon the band alignment at the source/channel interface, including: (a) homojunction, (b) staggered gap, and (c) broken gap TFET architectures. As can be seen from Fig 2.5 (a), the homojunction TFET design is based on a single-material p^+-i-n^+ configuration in which the source, channel, and drain have different dopant concentrations and types. As a result, the dopant profile and concentration at the source/channel interface are critical for maintaining a steep energy band profile and thus a narrower tunneling barrier width (λ) for carriers tunneling from the source into the channel. Due to the typically larger λ and effective tunneling barrier height, E_{beff}, as a result of the constant bandgap throughout the

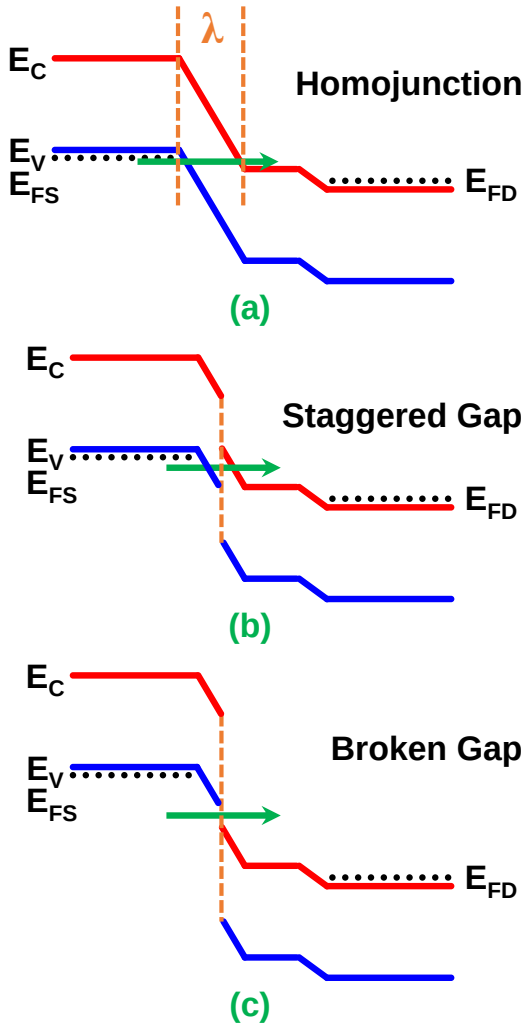

Figure 2.5 Schematic energy band diagrams for the three conventional TFET configurations in the ON-state, including: (a) homojunction; (b) staggered gap; and (c), broken gap. Homojunction tunneling current is limited by the larger tunneling barrier width (λ) in comparison to staggered or broken gap TFETs. Staggered gap and broken gap heterojunction TFETs use different materials for the source and channel regions in order to engineer the energy band alignment the source/channel heterointerface. As a result, λ and E_{beff} can be significantly reduced, thus enhancing I_{ON}. In the case of a broken gap heterojunction TFET, E_{beff} is negative and an additional reverse bias is needed to turn off the device.

heterojunction TFET architecture comprising two materials with different bandgaps for the source and channel regions. In such a staggered gap heterojunction TFET, the source/channel heterointerface exhibits a type-II energy band alignment, resulting in a reduced λ, and thus increased I_{ON} as compared to a homojunction TFET **[19, 20]**. Likewise, Fig. 2.5 (c) displays the energy band diagram for a broken gap heterojunction TFET in which the source/channel materials are selected such that the energy band alignment at the source/channel heterointerface is type-III. Due to the lack of an E_{beff} at zero applied bias, λ is effectively reduced to nearly zero, thereby suggesting that broken gap heterojunction TFET should have the highest I_{ON} of all TFET architectures.

Similar to engineering λ by carefully selecting the tunnel junction energy band alignment, E_{beff} can also be engineered to enhance TFET ON-state performance. In the case of an *n*-TFET, E_{beff} is defined as the energy separation between the conduction band minimum of the channel and the valence band maximum of the source, as shown in Fig. 2.1 (b). Correspondingly, E_{beff} for a *p*-TFET is defined as the energy separation between the valence band minimum of the channel and the conduction band maximum of the source, as shown in Fig. 2.1 (c). Note that in both cases E_{beff} is conventionally taken at zero applied gate bias. As can be seen by examining (2.6), the tunneling probability and hence tunneling current in a TFET depends exponentially on the effective tunneling barrier height at the source/channel tunnel junction, indicating that E_{beff} is critical to determining the ON-state drive current. Additionally, due to the TFET's often symmetric nature with respect to source/drain doping concentration and device geometry, E_{beff} at the drain/channel interface is also significant in determining the OFF-state leakage current of the TFET device **[10]**. Homojunction and staggered gap heterojunction TFET

architectures exhibit positive E_{beff} values, indicating that an applied gate bias voltage is necessary to turn on the device. In the case of a staggered gap heterojunction TFET, E_{beff} can be tailored by changing the materials (or alloy compositions) for the source and channel, thereby tuning the energy band alignment based upon careful selection of source/channel materials. As a result, E_{beff} can be significantly reduced in comparison to a homojunction TFET, dramatically improving I_{ON} at lower applied biases. As E_{beff} is tuned below zero (*i.e.*, negative), the source/channel energy band alignment transitions to a broken gap heterojunction, effectively eliminating the tunneling barrier for carriers at the source/channel heterointerface. As a result, substantial enhancement of I_{ON} is expected for broken gap heterojunction TFETs; however, the ON-state improvement comes at the cost of increased OFF-state leakage due to the lack of a blocking barrier preventing tunneling at zero gate bias. Therefore, broken gap heterojunction TFETs require the application of additional (reverse) gate bias in order to turn OFF the device **[21]**.

2.1.3. I_{ON} Improvement and Reduction of Ambipolar Through Source/Channel/Drain Bandgap Engineering and Dopant Selection

As shown in Fig. 2.1, the most simplistic design for a TFET consists of a gated p^+-i-n^+ diode with symmetrically doped source and drain regions featuring equivalent geometries. A direct consequence of this symmetric TFET configuration is matching electrical behavior of the device in the ON- and OFF-states, otherwise known as ambipolarity. Ambipolar devices exhibit *n*-type tunneling behavior at the source/channel junction under positive gate bias and *p*-type tunneling behavior at the drain/channel junction under negative gate bias. The ambipolar nature of a symmetric TFET thus contributes significantly to the leakage current of the device, degrading the I_{ON}/I_{OFF} ratio

as well as the subthreshold device characteristics. Therefore, the design of a TFET architecture must carefully consider the impact of ambipolar conduction on device and circuit performance, and should minimize ambipolarity through materials selection, energy band alignment engineering, and source/drain doping.

As discussed in the previous section, engineering of E_{beff} can be accomplished using different materials or alloy compositions for the source and channel regions. As a result of engineering the tunneling heterointerface band alignment and lowering E_{beff}, it is often the case that an asymmetry in bandgaps arises between the source and channel/drain regions. Thus, if the channel/drain material has a larger bandgap than the source material, E_{beff} in the reverse direction (at the drain/channel interface) is larger than E_{beff} in the forward direction (at the source/channel interface), thereby prohibiting OFF-state tunneling current. Furthermore, a larger bandgap channel material also benefits from a higher joint density of states, allowing for increased BTBT carrier generation and improved tunneling current. Moreover, selecting a lower bandgap source material has been predicted to significantly enhance I_{ON} at the risk of degrading I_{OFF} due to increased thermal emission across the source/channel interface **[15, 22]**. Hence, an effective approach to suppressing I_{OFF} while increasing I_{ON} would be to select a channel/drain material with a larger bandgap than the source material **[23]**, creating an asymmetry in the TFET design to engineer a smaller source/channel E_{beff} and larger drain/channel E_{beff}.

Additionally, the doping concentration of the TFET source and drain regions can be tailored to maximize I_{ON} while minimizing I_{OFF} **[5]**. In order to boost ON-state

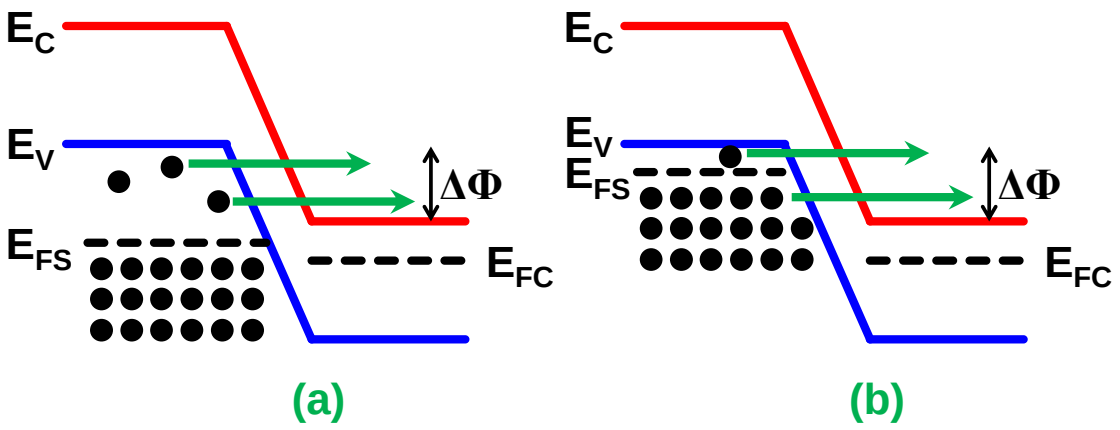

Figure 2.6 (a) Schematic energy band diagram for an n-TFET with a highly degenerate source doping. Electrons only partially occupy states above E_{FS} in the source valence band, thus reducing the total number of paired states in the energy window ΔΦ when the device is turned ON and degrading I_{ON} and *SS*. (b) Schematic energy band diagram for the same structure with a lower doped source. E_{FS} is closer to E_V, resulting in a larger number of occupied electron states in the source within the energy window ΔΦ that can pair to channel conduction band states and contribute to enhanced I_{ON} and *SS*.

performance, the source region near the channel should be heavily and abruptly doped, thereby enhancing the electric field at the source/channel tunneling junction, reducing the tunneling barrier width (λ), and increasing the tunneling current **[6]**. However, highly degenerate doping results in a quasi-Fermi level in the source, E_{FS}, that lies increasingly below (above) the source valence band maximum (conduction band minimum). As shown in Fig. 2.6 (a) for an n-TFET, the result of extending E_{FS} deep into the valence band is a decrease in the number of electrons occupying states in the energy range $(E_V - E_{FS})$ that can be paired with a state in the channel conduction band (under bias), thus reducing the tunneling current **[23]**. It therefore becomes important to design an

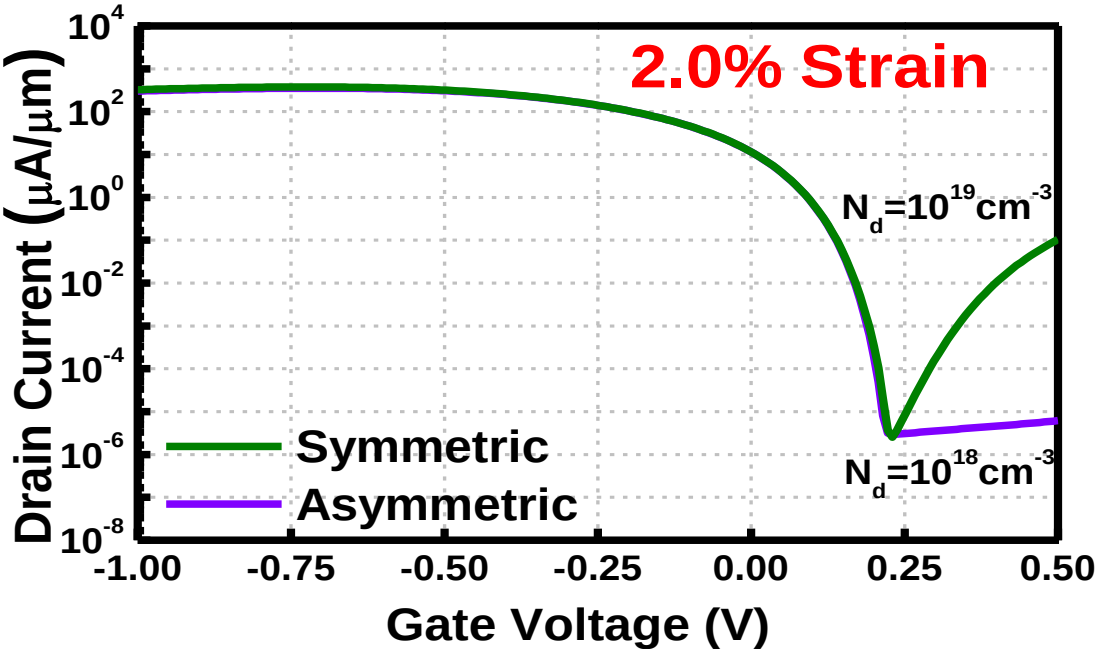

Figure 2.7 Simulated tensile-strained Ge/$In_{0.29}Ga_{0.71}As$ p-TFETs with two different drain dopings: $N_D = 10^{19}$ cm^{-3} (green) and $N_D = 10^{18}$ cm^{-3} (purple). An order of magnitude decrease in N_D results in a 10^4 reduction in I_{OFF} due to an increased E_{beff} at the drain/channel interface **[25]**. Used with permission of IEEE Transactions on Electron Devices. © 2015 IEEE.

the available electrons in the source valence band within the energy window ΔΦ that can contribute to tunneling current, as shown in Fig. 2.6 (b). Furthermore, the increase in available tunneling carriers at lower energy windows (gate bias) corresponds to steeper subthreshold characteristics in addition to enhanced I_{ON} **[6, 23]**.

Likewise, TFET drain doping must be optimized to reduce OFF-state leakage current and improve energy-efficient device operation. In the case of the source/channel junction, increased source doping resulted in a higher junction electric field, lower tunneling barrier width (λ), and increased tunnel current **[6]**. Therefore, to suppress OFF-state tunneling current, one approach would be to decrease the drain doping, thereby

decreasing the drain/channel junction electrical field, increasing λ, and decreasing tunneling current when the TFET is OFF **[24]**. Moreover, I_{ON} in a TFET is controlled by the BTBT generation of carriers at the source/channel interface, thus reducing the drain doping and increasing E_{beff} at the drain/channel junction has no impact on the ON-state device performance. Fig. 2.7 **[25]** illustrates the effect of asymmetric doping on the simulated transfer characteristics of a 2% tensile-strained Ge/$In_{0.29}Ga_{0.71}As$ p-TFET. As can be seen from Fig. 2.7, I_{OFF} in the case of the asymmetrically doped device is reduce by a factor of 10^4, indicating that optimal source and drain doping configurations can simultaneously result in high I_{ON} and significantly suppressed I_{OFF}.

2.1.4. Channel Length (L_g) Considerations for Device Operation

Aggressive channel length scaling has been a hallmark of the semiconductor industry for decades, resulting in increased device density and performance. However, the effect of channel length on TFET ON-state performance is less relevant due to the majority dependence of TFET drive current on the BTBT generation of tunneling carriers at the source/channel junction. Conversely, the OFF-state leakage current of a TFET is greatly impacted by channel length scaling due to the decreasing space chare region and hence increasing junction electric field **[26]**. As a result of the increasing electric field in the intrinsic region and at the tunnel junction(s) of an aggressively scaled TFET, the energy band diagram across the device is distorted, and begins to resemble the ON-state band alignment for a long channel TFET device. Moreover, due to the sharp band bending across the channel and high electric field at the junction(s), tunneling current is generated irrespective of applied gate bias **[26, 27]**. Therefore, at extremely scaled TFET channel

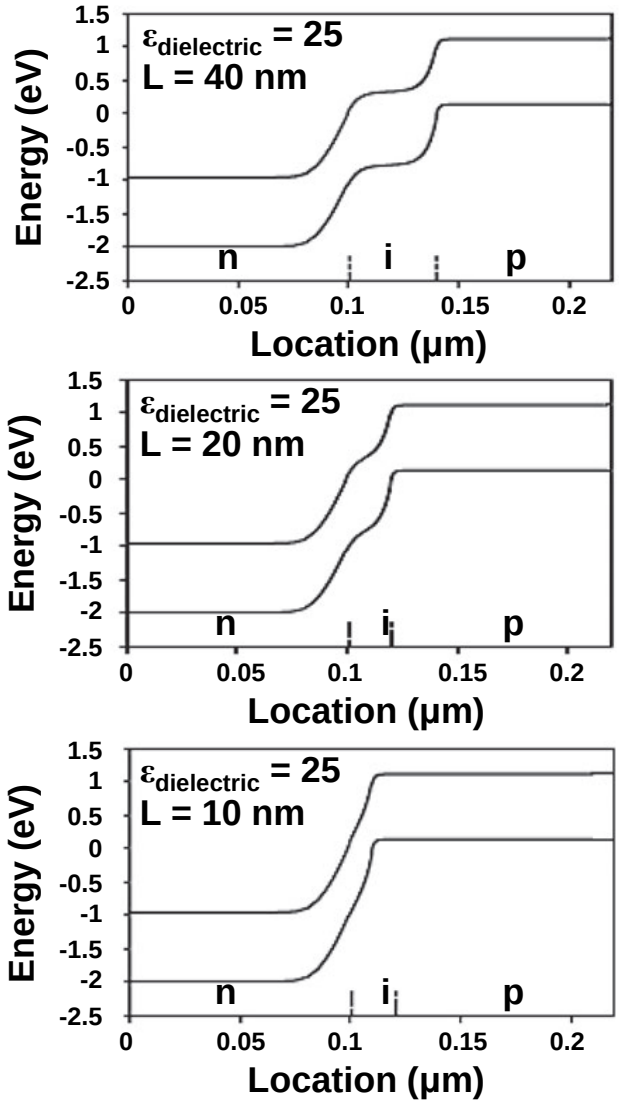

Figure 2.8 Schematic energy band diagrams for simulated TFETs with channel lengths of 40 nm, 20 nm, and 10 nm. At channel lengths of 40 nm and 20 nm, gate control over the ON/OFF states of the device is maintained. As channel length is scaled to 10 nm, the high junction electric field and field distributed across the channel distort the energy bands, causing Zener breakdown to occur **[26]**. Used with permission of Nanotechnology Reviews.

diodes, and is illustrated in Fig. 2.8 **[26]** for simulated TFETs with high-κ (ε = 25) gate oxides and gate lengths of 40 nm (a), 20 nm (b), and 10 nm (c).

As shown in Fig. 2.8 (a) for TFETs in which the electric field across the channel and at the junctions is distributed over a greater channel length (≥ 40 nm), the effect of channel length scaling on the intrinsic device band alignment is not observed. However, as channel length is further scaled down to 20 nm, as shown in Fig. 2.8 (b), the field in the space charge region and near the junctions begins to distort the energy bands in those areas, decreasing E_{beff} and λ and increasing the probability of OFF-state tunneling. Finally, one can find from Fig. 2.8 (c) that as channel length is scaled down to 10 nm, the built-in junction electric fields and field distribution across the channel are high enough to significantly distort the channel energy bands, resulting in a zero-bias (OFF-state) tunneling current due to the creation of an overlap energy interval (ΔΦ) similar to that in Fig. 2.6. Therefore, at highly scaled channel lengths, the gate loses its electrostatic control over the channel and I_{OFF} is substantially enhanced. Consequently, this suggests that TFET channel length scaling is not as beneficial to device operation as in conventional CMOS, placing a lower limit on the extent to which TFET channel lengths can be scaled.

2.2 ε-Ge/$In_xGa_{1-x}As$ Heterostructures for on Si ε-Ge Active Photonic Devices

As discussed in ***Chapter 1***, the scaling of metal interconnect length and half-pitch is approaching bottlenecks in both metal interconnect performance (*e.g.*, bit rate) and power dissipation (*e.g.*, interconnect energy) **[28, 29]**. As a result, the development of inter- and intra-chip optical data transmission is considered a promising path towards low-power

compute scaling by simultaneously benefitting from energy-efficient, high bandwidth optical data transmission and high-speed, electronic data processing **[30, 31]**. In order to realize such electronic-photonic integrated circuits (EPICs), CMOS-compatible light sources, photodetectors, and optical modulators are required **[30]**. Whereas silicon (Si) would be the ideal material for such photonic devices, its indirect bandgap (X-valley, 1.12 eV) and lack of a feasible Γ-valley minimum (3.4 eV) mean that new optical materials are necessary for the large-scale integration of optoelectronics on the Si platform **[32]**. Germanium (Ge), although initially an indirect bandgap material (L-valley, 0.664 eV), can be tailored to enhance direct-gap recombination through several materials engineering approaches that reduce or bypass the 136 meV separation between Γ and L valleys. This section will outline the most promising approaches to engineering the Ge band structure for the integration of Ge-based photonics with Si CMOS technology.

2.2.1. Band Structure Engineering

2.2.1.1. Strained-Engineered Ge

In general, strain engineering of material properties has been exploited for several decades to realize, for example, III-V quantum-well (QW) and quantum-dot (QD) lasers and electroabsorption modulators with tunable wavelengths **[33]**. In particular, the introduction of biaxial tensile strain into Ge thin films or substrates has several positive effects for Ge-based photonics applications. Predominantly, the most beneficial result of applying biaxial tensile strain to Ge is a reduction in the conduction band minima **[34-36]**. Furthermore, the Γ-valley minimum is reduced at a more rapid rate compared to the

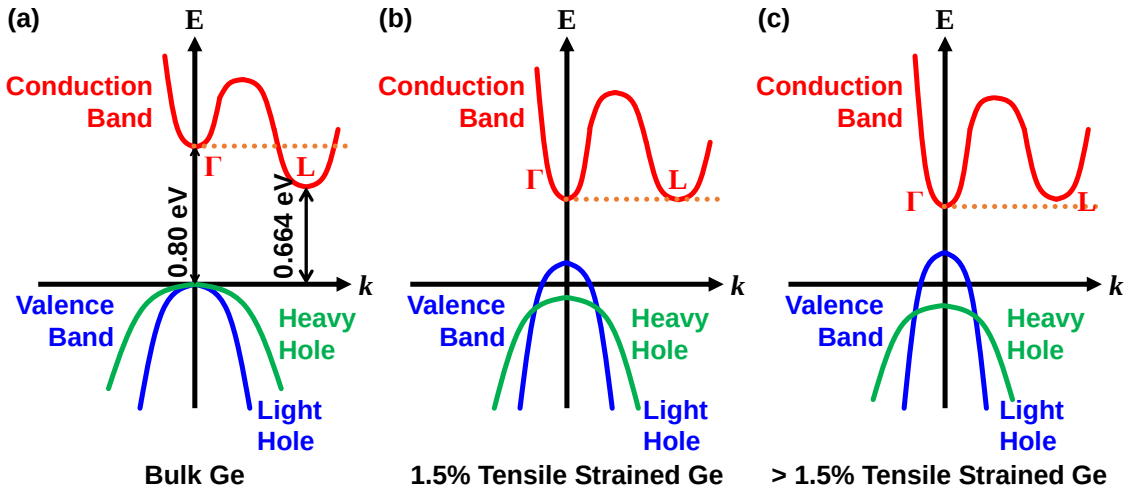

Figure 2.9 Schematic energy-dispersion diagrams for Ge illustrating three separate strain states: (a) unstrained (bulk-like) Ge in which the Γ-to-L-valley minima separation is 136 meV and the Γ-*lh* bandgap is 0.80 eV; (b) 1.5% biaxial tensile-strained Ge in which no Γ-to-L-valley separation exists and the Γ-*lh* bandgap is predicted to be ~0.52 eV; and (c), > 1.5% biaxial tensile-strained Ge in which the Γ-valley lies below the L-valley and the Γ-*lh* is predicted to be < 0.52 eV. Enhanced direct-gap Ge emission is expected for biaxial tensile strains exceeding the cross-over point between indirect and direct bandgap energies.

after which the direct bandgap of Ge will be narrower than the indirect bandgap **[34-36]**. Additionally, the introduction of biaxial tensile strain into Ge lifts the degeneracy of the light-hole (*lh*) and heavy-hole (*hh*) valence bands, resulting in a raised *lh* valence band and lowered *hh* valence band. Therefore, the combined reduction in conduction band minima and raising of the *lh* valence band maximum by strain engineering allows device engineers to tune the emission and absorption wavelength of Ge by tailoring the Ge bandgap. Moreover, the raising of the *lh* valence band and reduction of *lh* effective mass

with applied strain reduces the density of states in the valence band, thereby decreasing the threshold for optical transparency and lasing **[36, 37]**.

Fig. 2.9 qualitatively illustrates the effective of increasing biaxial tensile strain on the band structure of Ge at the Γ- and L- valleys. As Fig. 2.9 (a) shows, the initial Γ-to-L-valley separation for unstrained Ge is 0.136 eV **[38]**. By applying tensile strain to the Ge, the Γ-valley minimum is reduced at a faster rate than the L-valley minimum. At 1.5% biaxial tensile strain, the two minima are projected to be equal **[34-36]**, as shown in Fig. 2.9 (b). By engineering the strain level in Ge to be larger than the 1.5% threshold, the Ge can be transformed to a direct bandgap material, greatly enhancing optical emission intensity, as shown by Fig. 2.9 (c).

Experimentally, the influence of tensile strain on Ge optical properties has been demonstrated for process-induced **[39]**, micro-mechanical **[35]**, **[40]**, **[41]**, and epitaxial strain **[42-44]**. However, for the large-scale integration of tensile-strained Ge optoelectronics on Si, careful consideration has to be given to the compatibility of Ge stressors with CMOS processing technology **[29]**. Due to the complexity in integration and inability to finely tune the strain generated *via* processing and micro-mechanical techniques, epitaxially-induced strain is a promising stressor method that is expected to be fully-compatible with state-of-the-art CMOS process technology **[45, 46]**. Fig. 2.10 demonstrates the strained-layer epitaxy of Ge on an $In_xGa_{1-x}As$ strain template. When the InAs mole fraction is zero, Ge is quasi-lattice-matched to GaAs, as shown in Fig. 2.10 (a). By increasing the InAs mole fraction in the $In_xGa_{1-x}As$, the in-plane lattice constant of the Ge thin film is gradually stretched, generating a biaxial in-plane tension that is

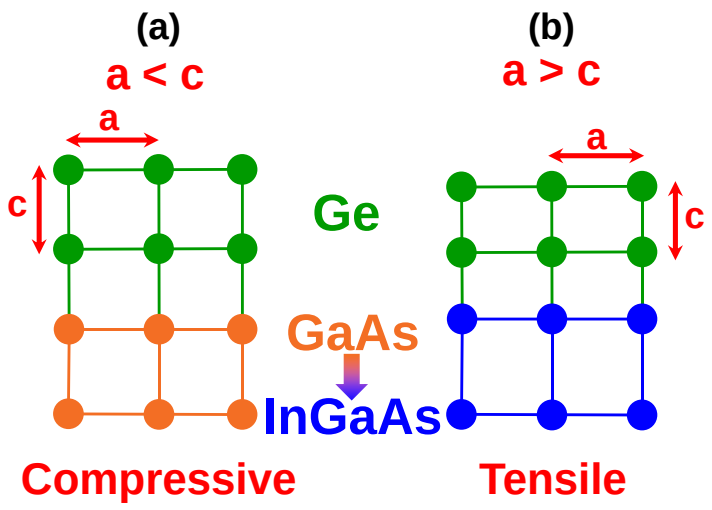

Figure 2.10 (a) Schematic illustration of Ge grown on quasi-lattice-matched GaAs exhibiting negligible compressive strain. (b) Schematic representation of Ge grown epitaxially on lattice-mismatched $In_xGa_{1-x}As$ strain templates. As the InAs mole fraction increases, the strain transferred to the epitaxial increases proportionally to the change in $In_xGa_{1-x}As$ in-plane lattice constant, thereby allowing precise engineering of the Ge band structure.

proportional to the increase in lattice constant and InAs mole fraction, as shown in Fig. 2.10 (b). Due to the precise control of the In alloy composition offered by epitaxial growth techniques such as molecular beam epitaxy (MBE), epitaxially-induced strain offers highly-tunable tensile-strained Ge thin films, affording device engineers greater design flexibility and a wider range of Ge optical properties.

2.2.1.2. Tin (Sn) Alloying

An alternative approach to engineering the band structure of Ge-based materials is through the alloying of Ge with α-phase tin (α-Sn) **[47-49]**. As Fig. 2.11 (a) shows, the diamond cubic phase of Sn (α-Sn) is a semiconductor with a negative direct band gap of -0.41 eV and positive indirect L-valley bandgap of 0.1 eV **[38]**. As a result, the Ge_xSn_{1-x}

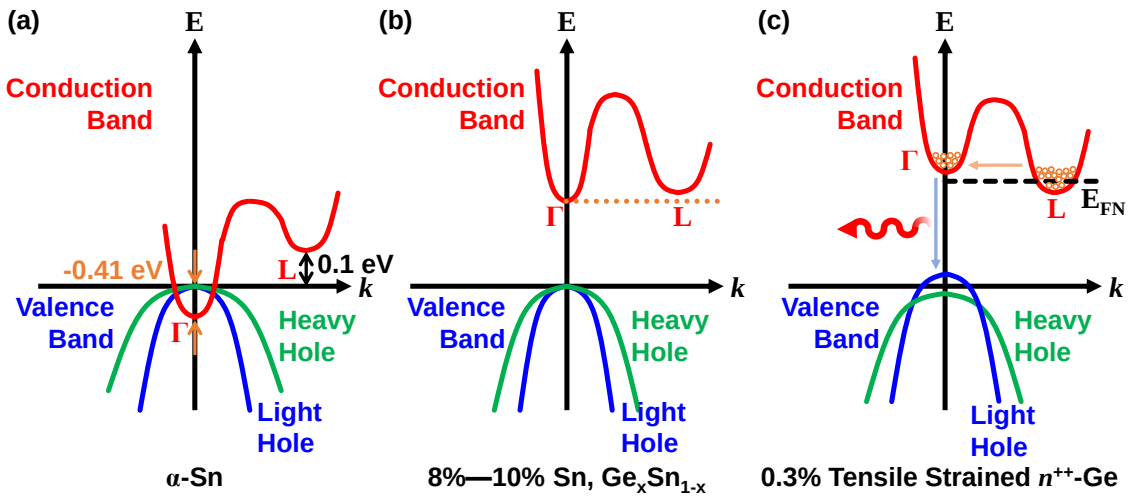

Figure 2.11 (a) Schematic energy-dispersion diagram for semiconducting α-Sn exhibiting a -0.41 eV direct bandgap and +0.1 indirect bandgap. (b) Schematic representation of the effect of Sn alloying on the Ge_xSn_{1-x} band structure. The Γ-valley minimum is reduced at a much higher rate than the L-valley minimum as a function of Sn alloy composition. (c) Schematic representation of the coupled effects of thermally-induced tensile strain and degenerate *n*-type doping on the Ge band structure. Pseudo-direct-gap Ge emission is obtained.

bandgap for increasing Sn compositions, as shown in Fig. 2.11 (b). Thus, through the incorporation of different Sn alloy compositions, the Ge_xSn_{1-x} optical emission and absorption wavelengths can be tailored on a per-application basis. Although several compositional values resulting in direct-gap recombination from Ge_xSn_{1-x} have been reported **[48-51]**, the thermal instability and compositional fluctuation of the Ge_xSn_{1-x} alloy have made it challenging to define an experimental direct-to-indirect cross-over point. Recent results therefore yield an estimated indirect-to-direct recombination transition point for Sn compositions in the range of 8% to 10%. The variability in Ge_xSn_{1-x} alloys is a direct result of the poor solid solubility of Sn in Ge under equilibrium

conditions (≤ 1% atomic) [29]. Therefore, it follows that non-equilibrium growth techniques, such as MBE or metalorganic chemical vapor deposition (MOCVD), are required for the growth and realization of Ge_xSn_{1-x} alloys for on-Si optoelectronic applications. However, an additional challenge arises with regards to the temperature stability of Ge_xSn_{1-x} alloys. Due to the low solid solubility of Sn in Ge, elevated thermal budgets, such as those commonly experienced during CMOS source/drain processing, result in severe Sn segregation [52], substantially degrading the crystalline quality and optical properties of the Ge_xSn_{1-x} alloy. Hence, the heterogeneous integration of Ge_xSn_{1-x}-based photonics with CMOS technology would require the optimization of thermal processes during photonic device fabrication as well as during CMOS processing and integrated circuit packaging, greatly limiting the feasibility of Ge_xSn_{1-x} photonic devices on Si.

2.2.1.3. Thermal Cycle Annealing and Degeneration N-Type Doping

A third scheme for enhancing direct-gap emission from Ge combines the use of degenerate *n*-type doping (10^{19}—10^{20} cm^{-3}) with low levels (0.2—0.3%) of tensile strain in order to compensate the 136 meV difference between the Γ- and L-valley minima [39], [53, 54]. By thermally quenching Ge films grown on Si substrates, a 0.2—0.3% biaxial tensile strain is transferred to the Ge layer due to the difference in thermal expansion coefficients between Ge and Si. This moderate strain amount is expected to decrease the Γ-to-L-valley separation by ~53 meV and reduce the Γ-*lh* bandgap to ~0.75 eV [53]. By degenerately doping the Ge film *n*-type, the quasi-Fermi level (E_{FN}) lies within the bottom energy levels of the L-valley minimum [54]. As a result, the energy states in the L-valley below E_{FN} are occupied, and upon carrier injection, some of the injected

electrons are forced to occupy states in the Γ-valley minimum. Electrons occupying states in the Γ-valley are then free to radiatively recombine with holes, generating direct-gap Ge emission, as shown in Fig. 2.11 (c). Moreover, due to the enhanced radiative recombination rate of direct-gap Ge emission, electrons in the Γ-valley are depleted at much faster rates than those in the L-valley, resulting in increased injection of electrons from the L-valley to the Γ-valley through inter-valley scattering during emission. Furthermore, the proximity of E_{FN} to the Γ-valley minimum (also due to the heavily *n*-type doping) corresponds to a lower injection level necessary for population inversion, allowing for net optical gain and providing a path towards low-threshold current Ge lasing **[37]**, **[55]**. Lastly, a distinct advantage to the coupling of moderate tensile strain and degenerate *n*-type doping is that the emission wavelengths lie much closer to the wavelengths used in L and C band optical communication, *i.e.* 1520—a 1630 nm **[29]**.

2.2.2. Electrical and Optical Confinement for Ge-on-Si Lasing

A final approach for achieving Ge-on-Si active photonic devices is to indirectly engineering the Ge band structure, rather than directly engineering it through strain, Sn alloying, or degenerate doping **[55, 56]**. Fig. 2.12 **[55]** shows a simulated schematic energy band diagram for a quasi-lattice-matched 3.3 nm Ge quantum well (QW) surrounded by two $Al_{0.18}Ga_{0.82}As$ barrier layers. In Fig. 2.12, the L-valley minimum energy level is shown in green (solid) whereas the Γ-valley minimum energy level is shown in blue (solid). Due to the ultra-thin Ge thickness, strong quantum confinement is exhibited in both the L- and Γ-valleys, as well as the light-hole (*lh*) valence band. Moreover, by selecting the barrier material such that electron confinement is enhanced in the L-valley in comparison to the Γ-valley, pseudo-direct-gap Ge recombination is

expected. An advantage to this approach is that the pseudo-direct-gap nature of the Ge QW offers enhanced thermal stability over other approaches that directly engineer the Ge band structure through thermally sensitive processes, such as high-strain engineering or high-Sn composition Ge_xSn_{1-x} alloying. Additionally, the emission wavelength of such III-V/Ge/III-V heterostructures is predicted to be closer to the C and L band communication wavelengths (1520—1630 nm), making them suitable for on-Si optical data transmission **[29, 55, 56]**. Likewise, the quantum confinement effect on the Ge band structure can be partially compensated by growing III-V/Ge/III-V heterostructures with high bandgap barrier layers that introduce moderate strain levels into the Ge, e.g., $In_xAl_{1-x}As$. However, attention must be paid to engineering alternative barrier layers such that the confinement in the L-valley always exceeds that of the Γ-valley. Further optimization of the inactive barrier material and Ge QW thickness can be performed to design III-V/Ge/III-V heterostructures with band alignments suitable for different lasing applications, *e.g.*, laser diodes operating at high temperatures.

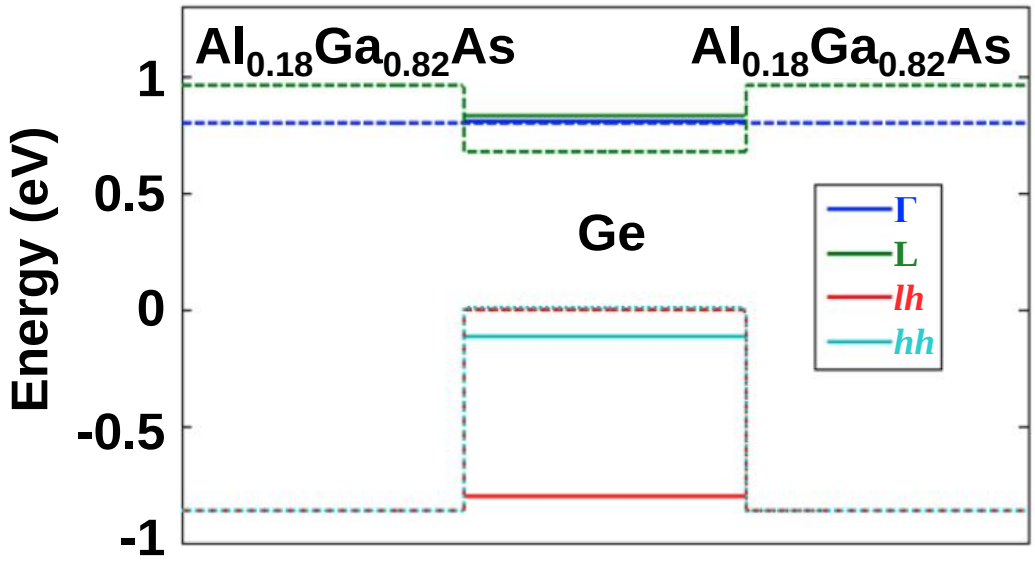

Figure 2.12 Simulated energy band diagram for a quasi-lattice-matched $Al_{0.18}Ga_{0.82}As/Ge/Al_{0.18}Ga_{0.82}As$ quantum-well (QW) heterostructure. The 3.3 nm Ge QW thickness results in enhanced L-valley quantum confinement when combined with barrier materials that further strongly confine the Ge L-valley. Solid lines show the energy levels in the QW and dashed lines show the band edges. **[55]** Used with permission of IEEE Journal of Selected Topics in Quantum Electronics. © 2013 IEEE.

References

[1] A. M. Ionescu and H. Riel, Tunnel Field-Effect Transistors as Energy-Efficient Electronic Switches, *Nature* **479**, 329-337 (2011).

[2] J. Knoch and J. Appenzeller, A Novel Concept for Field-Effect Transistors – The Tunneling Carbon Nanotube FET, *In IEEE Conference Proceedings of the Device Research Conference (DRC)*, 153-156 (2015).

[3] S. M. Sze, *Physics of Semiconductor Devices*, 3rd Ed., Wiley: New York (2007).

[4] L. D. Landau and E. M. Lifshitz, *Quantum Mechanics*, Addison-Wesley (1958).

[5] K. Boucart, Simulation of Double-Gate Silicon Tunnel FETs with a High-k Gate Dielectric. PhD Dissertation, Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland (2010).

[6] A. C. Seabaugh and Z. Qin, Low-Voltage Tunnel Transistors for Beyond CMOS Logic, *In IEEE Proc.* **98**, 2095-2110 (2010).

[7] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, Temperature-Dependent I-V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET, *IEEE Electron Device Lett.* **31**, 564-566 (2010).

[8] Y. Zhu, D. K. Mohata, S. Datta and M. K. Hudait, Reliability Studies on High-Temperature Operation of Mixed As/Sb Staggered Gap Tunnel FET Material and Devices, *IEEE Trans. Device Mater. Reliab.* **14**, 246 (2014).

[9] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, Role of InAs and GaAs Terminated Heterointerfaces at Source/Channel on the Mixed As-Sb Staggered Gap

Tunnel Field-Effect Transistor Structures Grown by Molecular Beam Epitaxy, *J. Appl. Phys.* **112**, 024306-1—024306-16 (2012).

[10] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, N. Monsegue, and M. K. Hudait, Defect Assistant Band Alignment Transistion from Staggered to Broken Gap in Mixed As/Sb Tunnel Field-Effect Transistor Heterostructure, *J. Appl. Phys.* **112**, 094312-1—094312-9 (2012).

[11] Z. Qin, Z. Wei, and A. Seabaugh, Low-Subthreshold-Swing Tunnel Transistors, *IEEE Electron Device Lett.* **27**, 297-300 (2006).

[12] T. Nirschl, S. Henzler, J. Fischer, M. Fulde, A. Bargagli-Stoffi, M. Sterkel, J. Sedlmeir, C. Weber, R. Heinrich, U. Schaper, J. Einfeld, R. Neubert, U. Feldmann, K. Stahrenberg, E. Ruderer, G. Georgakos, A. Huber, R. Kakoschke, W. Hansch, and D. Schmitt-Landsiedel, Scaling Properties of the Tunneling Field Effect Transistor (TFET): Device and Circuit, *Solid-State Electron.* **50**, 44-51 (2006).

[13] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors, *Phys. Rev. Lett.* **93**, 196805-1—196805-4 (2004).

[14] P. F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, Complementary Tunneling Transistor for Low Power Application, *Solid-State Electron.* **48**, 2281-2286 (2004).

[15] K. K. Bhuwalka, J. Schulze, and T. Eisele, Performance Enhancement of Vertical Tunnel Field-Effect Transistor with SiGe in the Delta p^+ Layer, *Jpn. J. Appl. Phys.* **43 (7A)**, 4073-4078 (2004).

[16] R. Asra, M. Shrivastava, KVRM Murali, R. K. Pandey, H. Gossner, and R. V. Ramgopal, A Tunnel FET for V_{DD} Scaling Below 0.6 V with a CMOS-Comparable Performance, *IEEE T. Electron Dev.* **58**, 1855-1863 (2011).

[17] K. Boucart and A. M. Ionescu, A New Definition of Threshold Voltage in Tunnel FETs, *Solid-State Electron.* **52**, 1318-1323 (2008).

[18] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, Tunneling Field-Effect Transistors (TFETs) with Subthreshold Swing (SS) Less than 60 mV/dec, *IEEE. Electron Device Lett.* **28**, 743-745 (2007).

[19] D. K. Mohata, R. Bijesh, S. Majumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, Demonstration of MOSFET-like On-Current Performance in Arsenide/Antimonide Tunnel FETs with Staggered Hetero-junctions for 300 mV Logic Applications, *in IEEE Conference Proceedings of the International Electron Devices Meeting (IEDM)* (**IEEE, 2011**), 781-784.

[20] D. Mohata, B. Rajamohanan, T. Mayer, M. Hudait, J. Fastenau, D. Lubyshev, A. K. Liu, and S. Datta, Barrier-Engineered Arsenide-Antimonide Heterojunction Tunnel FETs with Enhanced Drive Current, *IEEE Electron Device Lett.* **33**, 1568-1570 (2012).

[21] S. O. Koswatta, S. J. Koester, and W. Haensch, 1D Broken-Gap Tunnel Transistor with MOSFET-like On-Currents and Sub-60 mV/dec Subthreshold Swing, *in IEEE Conference Proceedings of the International Electron Devices Meeting (IEDM)* **(IEEE, 2009)**, 1-4.

[22] A. S. Verhulst, W. G. Vandenberghe, K. Maex, S. D. Gendt, M. M. Heyns, and G. Groeseneken, Complimentary Silicon-Based Heterostructure Tunnel-FETs with High Tunnel Rates, *IEEE Electron Device Lett.* **29**, 1398-1401 (2008).

[23] W. Lingquan and P. Asbeck, Design Considerations for Tunneling MOSFETs Based on Staggered Heterojunctions for Ultra-Low-Power Applications, *in IEEE Conference Proceedings of the Nanotechnology Materials and Devices Conference (NMDC)* **(IEEE, 2009)**, 196-199.

[24] M. Schmidt, R. A. Minamisawa, S. Richter, A. Schafer, D. Buca, J. M. Hartmann, Q. T. Zhao, and S. Mantl, Unipolar Behavior of Asymmetrically Doped Strained Si0.5Ge0.5 Tunneling Field-Effect Transistors, *Appl. Phys. Lett.* **101**, 123501-1—123501-4 (2012).

[25] J. -S. Liu, M. Clavel, and M. K. Hudait, Performance Evaluation of Novel Strain Engineered Ge-InGaAs Heterojunction Tunnel Field Effect Transistors, *IEEE T. Electron Dev.* **62**, 3223-3228 (2015).

[26] K. Boucart and A. M. Ionescu, Length Scaling of the Double Gate Tunnel FET with a High-K Gate Dielectric, *Solid-State Electron.* **51**, 1500-1507 (2007).

[27] K. K. Bhuwalka, M. Born, M. Schindler, M. Schmidt, T. Sulima, and I. Eisele, P-Channel Tunnel Field-Effect Transistors Down to Sub-50 nm Channel Lengths, *Jap. J. Appl. Phys.* **45**, 3106-1—3106-4 (2006).

[28] D. A. B. Miller, Physical Reasons for Optical Interconnection, *Int. J. Optoelectronics* **11**, 155-168 (1997).

[29] J. F. Liu, Monolithically Integrated Ge-on-Si Active Photonics, *Photonics* **1**, 162-197 (2014).

[30] D. A. B. Miller, Device Requirements for Optical Interconnects to Silicon Chips, *Proc. IEEE* **97**, 1166-1185 (2009).

[31] D. A. B. Miller, Optical Interconnects to Silicon, *IEEE J. Sel. Top. Quantum Electron.* **6**, 1312-1317 (2000).

[32] D. Liang and J. E. Bowers, Recent Progress in Lasers on Silicon, *Nat. Photonics* **4**, 511-517 (2010).

[33] J. Yang, P. Bhattacharya, and Z. Wu, Monolithic Integration of InGaAs-GaAs Quantum-Dot Laser and Quantum-Well Electroabsorption Modulator on Silicon, *IEEE Photonics Tech. Lett.* **19**, 747-749 (2007).

[34] M. V. Fischetti and S. E. Laux, Band Structure, Deformation Potentials, and Carrier Mobility in Strained Si, Ge, and SiGe Alloys, *J. Appl. Phys.* **80**, 2234-2252 (1996).

[35] J. R. Sanchez-Perez, C. Boztug, F. Chen, F. F. Sudradjat, D. M. Paskiewicz, R. B. Jacobson, M. G. Lagally, and R. Paiella, Direct-Bandgap Light-Emitting Germanium in Tensilely Strained Nanomembranes, *Proc. Nat. Acad. Sci.* **108**, 18893-18898 (2011).

[36] M. El Kurdi, G. Fishman, S. Sauvage, and P. Boucaud, Band Structure and Optical Gain of Tensile-Strained Germanium Based on a 30 Band k·p Formalism, *J. Appl. Phys.* **107**, 013710-1—013710-7 (2010).

[37] S. –W. Chang and S. L. Chuang, Theory of Optical Gain of Ge-$Si_xGe_ySn_{1-x-y}$ Quantum-Well Lasers, *IEEE J. Quantum Electron.* **43**, 249-256 (2007).

[38] O. Madelung, *Semiconductors: Intrinsic Properties of Group IV Elements and III-V, II-VI, and I-VII Compounds*, Vol. 22a, Springer: Berlin (1985).

[39] D. D. Cannon, J. F. Liu, Y. Ishikawa, K. Wada, D. T. Danielson, S. Jongthammanurak, J. Michel, and L. C. Kimerling, Tensile Strained Epitaxial Ge Films on Si(100) Substrates with Potential Application in L-Band Telecommunications, *Appl. Phys. Lett.* **84**, 906-908 (2004).

[40] M. El Kurdi, H. Bertin, E. Martincic, M. de Kersauson, G. Fishman, S. Sauvage, A. Bosseboeuf, and P. Boucaud, Control of Direct Band Gap Emission of Bulk Germanium by Mechanical Tensile Strain, *Appl. Phys. Lett.* **96**, 041909-1—041909-3 (2010).

[41] J. R. Jain, A. Hryciw, T. M. Baer, D. A. B. Miller, M. L. Brongersma, and R. T. Howe, A Micromachining-Based Technology for Enhancing Germanium Light Emission via Tensile Strain, *Nature Photonics* **6**, 398-405 (2012).

[42] Y. Huo, H. Lin, R. Chen, M. Makarova, Y. Rong, M. Li, T. I. Kamins, J. Vuckovic, and J. S. Harris, Strong Enhancement of Direct Transition Photoluminescence with Highly Tensile-Strained Ge Grown by Molecular Beam Epitaxy. *Appl. Phys. Lett.* **98**, 011111-1—011111-3 (2011).

[43] N. Pavarelli, T. J. Ochalski, F. Murphy-Armando, Y. Huo, M. Schmidt, G. Huyet, and J. S. Harris, Optical Emission of a Strained Direct-Band-Gap Ge Quantum Well Embedded Inside InGaAs Alloy Layers, *Phys. Rev. Lett.* **110**, 177404-1—177404-5 (2013).

[44] M. de Kersauson, M. Prost, A. Ghrib, M. El Kurdi, S. Sauvage, G. Beaudoin, L. Largeau, O. Mauguin, R. Jakomin, I. Sagnes, G. Ndong, M. Chaigneau, R. Ossikovski, and P. Boucaud, Effect of Increasing Thickness on Tensile-Strained Germanium Grown on InGaAs Buffer Layers, *J. Appl. Phys.* **113**, 183508-1—183508-7 (2013).

[45] K. Gallacher, P. Velha, D. J. Paul, S. Cecchi, J. Frigerio, D. Chrastina, and G. Isella, 1.55 μm Direct Bandgap Electroluminescence from Strained n-Ge Quantum Wells Grown on Si Substrates, *Appl. Phys. Lett.* **101**, 211101-1—211101-4 (2012).

[46] M. Clavel, D. Saladukha, P. Goley, T. J. Ochalski, F. Murphy-Armando, R. J. Bodnar, and M. K. Hudait, Heterogeneously-Grown Tunable Tensile Strained Germanium on Silicon for Photonic Devices, *ACS Appl. Mater. Interfaces* **7**, 26470–26481 (2015).

[47] J. Menéndez and J. Kouvetakis, Type-I $Ge/Ge_{1-x-y}Si_xSn_y$ Strained-Layer Heterostructures with a Direct Ge Bandgap, *Appl. Phys. Lett.* **85**, 1175-1177 (2004).

[48] R. Chen, H. Lin, Y. Huo, C. Hitzman, T. I. Kamins, and J. S. Harris, Increased Photoluminescence of Strain-Reduced, High-Sn Composition $Ge_{1-x}Sn_x$ Alloys Grown by Molecular Beam Epitaxy, *Appl. Phys. Lett.* **99**, 181125-1–181125-3 (2011).

[49] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca, and D. Grutzmacher, Lasing in Direct-Bandgap GeSn Alloy Grown on Si, *Nature Photonics* **9**, 88-92C (2015).

[50] W.-J. Yin, X.-G. Gong, and S.-H. Wei, Origin of the Unusually Large Band-Gap Bowing and the Breakdown of the Band-Edge Distribution Rule in the Sn_xGe_{1-x} Alloys, *Phys. Rev. B* **78**, 161203-1—161203-4 (2008).

[51] H. Perez Ladron de Guevara, A. G. Rodrıguez, H. Navarro-Contreras, and M. A. Vidala, Determination of the Optical Energy Gap of $Ge_{1-x}Sn_x$ Alloys with $0<x<0.14$, *Appl. Phys. Lett.* **84**, 4532-4534 (2004).

[52] S. Wirths, D. Stange, M.–A. Pampillon, A. T. Tiedemann, G. Mussler, A. Fox, U. Breuer, B. Baert, E. San Andres, N. D. Nguyen, J. M. Hartmann, Z. Ikonic, S. Mantl, and D. Buca, High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-Effect Transistors, *ACS Appl. Mater. Interfaces* **7**, 62-67F (2015).

[53] X.-C. Sun, J. F. Liu, L. C. Kimerling, and J. Michel, Direct Gap Photoluminescence of N-Type Tensile-Strained Ge-on-Si, *Appl. Phys. Lett.* **95**, 011911-1–011911-3 (2009).

[54] M. El Kurdi, T. Kociniewski, T.-P. Ngo, J. Boulmer, D. Débarre, P. Boucaud, J. F. Damlencourt, O. Kermarrec, and D. Bensahel, Enhanced Photoluminescence of Heavily N-Doped Germanium, *Appl. Phys. Lett.* **94**, 191107-1–191107-3 (2009).

[55] Y. Cai, Z. Han, X. Wang, R. E. Camacho-Aguilera, L. C. Kimerling, J. Michel and J. Liu, Analysis of Threshold Current Behavior for Bulk and Quantum-Well Germanium Laser Structures. *IEEE J. Sel. Top. Quantum. Electron.* **19**, 1901009-1—1901009-9 (2013).

[56] S. Cho, B.-G. Park, C.-J. Yang, S. Cheung, E. Yoon, T. I. Kamins, S. J. Ben Yoo, and J. S. Harris, Jr., Room-Temperature Electroluminescence from Germanium in an $Al_{0.3}Ga_{0.7}As$/Ge Heterojunction Light-Emitting Diode by Γ-Valley Transport, *Optics Express* **20**, 14921-14927 (2012).

Chapter 3 – Experimental Methodology:

Materials Synthesis and Characterization

3.1. Molecular Beam Epitaxy: Growth of Group IV and III-V Epilayers and Heterostructures

All structures studied in this thesis were grown by solid-source molecular beam epitaxy (MBE), which is a commonly used physical-vapor deposition technique found in industrial and academic settings at both the research and production scale. Under MBE growth conditions, thermal evaporation of high-purity, elemental liquid or crystalline sources generates a molecular beam of neutral atoms or molecules that is directed towards a growth substrate. In order to maximize the flux of material impinging on the growth surface and maintain a consistent growth environment, the growth chamber must be kept under ultra-high vacuum (UHV), *i.e.*, the residual gas pressure in the reactor chamber must be below 10^{-9} Torr. By maintaining such strict vacuum conditions, the mean-free path of the constituent atomic or molecular species is increased, thereby minimizing collisions between beam particles and the background vapor and promoting high-purity, low-defect epitaxy. A combination of oil-free roughing, turbo, ion, and cryogenic pumps are ordinarily employed to generate the UHV environment critical for MBE growth.

Fig. 3.1 shows a schematic diagram for a typical MBE reactor chamber **[1]**. In addition to using various pumping systems to maintain the UHV background, several measures are taken prior to growth to minimize residual atomic species contamination.

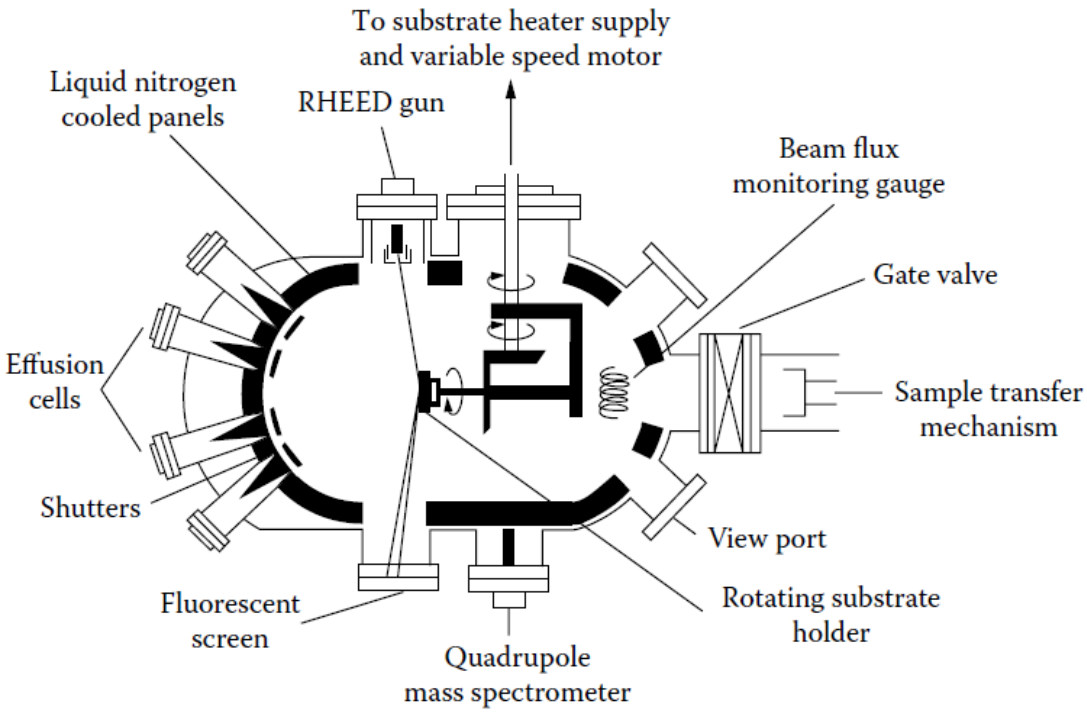

Figure 3.1 Schematic representation of a typical MBE growth chamber.

system to atmosphere. Further, baking of the individual effusion or cracking cells for each elemental species also aids in degassing the required growth materials and minimizing contamination. Additionally, as can be seen in Fig. 3.1, the walls of the growth chamber are cooled using a cryogenic (liquid N_2) shroud in order to minimize undesirable flux generation from atomic or molecular species coating the reactor's walls **[2]**. Similarly, components such as shutters and heaters are machined from highly stable, non-reactive and low-vapor pressure materials, *e.g.*, tantalum (Ta), molybdenum (Mo), or pyrolytic boron nitride (PBN). Growth substrates also undergo several degassing steps prior to being loaded into the growth chamber, including: (i) an 180^{o}C, three-hour long bake in a loading chamber to remove moisture from the substrate surface, substrate holder, and intro-chamber; (ii) a 300-400^{o}C (depending on the substrate material), two-

hour long bake in a buffer chamber to degas higher-temperature surface contamination before transferring to the growth chamber; and (iii), after transferring the substrate into the growth chamber, a high temperature oxide desorption in order to remove surface native oxides formed under ambient atmospheric conditions, thereby generating a pristine growth surface prior to epitaxy.

At this stage, thin-film epitaxy may proceed by heating of the effusion or cracking cells (shown in Fig. 3.1 as being mounted opposite to the substrate) and generating an elemental flux whose exposure time on the growth surface is actively controlled by individual motorized shutters. The flux levels needed during growth are routinely calibrated prior to substrate loading using an ion gauge (shown in Fig. 3.1 as being behind the substrate holder) to measure the beam-equivalent pressure (BEP) of each source for a given source temperature. In order to ensure film composition and thickness homogeneity across the growth surface, the substrate holder is typically rotated at a speed of six to eight revolutions per minute (rpm).

In situ monitoring of the growth (or oxide desorption) conditions at the sample surface is performed using reflection high-energy electron diffraction (RHEED) utilizing an electron beam nearly parallel to the growth surface. For the RHEED monitoring performed during the growth of the structures presented in this thesis, the incident beam energy and angle were 14.3 KeV and approximately 1^{o} to 2^{o}, respectively. Under these conditions, electron diffraction occurs following Bragg's law; however, due to the extremely shallow angle of incidence, electron penetration into the sample is limited to several surface monolayers, thereby only generating diffraction patterns of the two-dimensional surface lattice. Moreover, due to the high energies used in RHEED (at least

an order of magnitude greater than those used in X-ray diffraction), the Ewald sphere in reciprocal space is larger in diameter and thus encompasses a higher number of reflections **[1]**. As a result, the pattern in reciprocal space generated by the surface reflection of high-energy electrons incident on the two-dimensional growth surface consists of many elongated, narrow streaks (in the ideal case), as shown in Fig. 3.2 **[1]**. Hence, an effective method for identifying the growth mode at the growth surface is by monitoring the appearance and intensity of the RHEED pattern. Under uniform, ideal Frank-van der Merwe (2D, layer-by-layer) growth conditions, the RHEED pattern will reveal bright, narrow streaks consistent with rows of orthogonal, intersecting atomic planes at the growth front's terminating surface. If the growth mode were to deviate from the ideal and transition to the Volmer-Weber (3D, island formation) regime, this will be reflected in the RHEED as a loss of intensity and disruption (spottiness) of the sharp, narrow streaks seen in the previous scenario. Thus, due to the advantages of being able to monitor the quality of a growth at almost every stage, RHEED equipment is a common feature in most MBE systems, as shown in Fig 3.1.

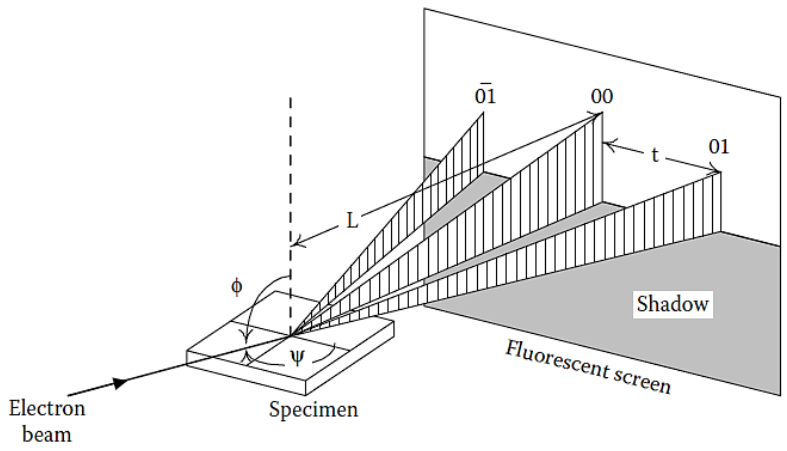

Figure 3.2 Schematic diagram of the RHEED surface analysis process.

3.2. Atomic Force Microscopy: Surface Morphology Characterization

Atomic force microscopy (AFM) is a scanning probe microscopy (SPM) technique that can routinely achieve angstrom-level vertical resolution during surface morphology characterization. As shown in Fig. 3.3, an extremely sharp tip attached to a cantilever is passed over a sample surface, resulting in a vertical deflection or force exerted upon the cantilever **[1]**. This deflection is measured by way of a laser diode, calibrated to the cantilever's top surface prior to measurement, wherein the reflected beam from the cantilever surface is incident upon a four-quadrant photodiode. As the cantilever moves across the sample, the deflection of the cantilever results in deflection of the position of the reflected beam on the photodiode with respect to it's initial position. This, in turn, is translated into a measure of the vertical movement of the cantilever and thus the height and morphology of surface features on the sample. Additionally, some AFM setups have a piezoelectric feedback system integrated into the sample mounting stage such that a constant force can be maintained on the cantilever tip as it scans the sample surface.

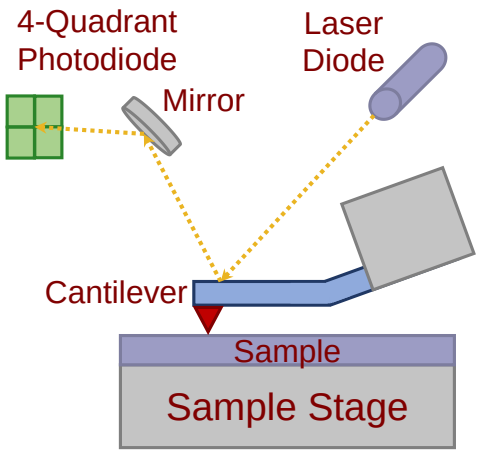

Figure 3.3 Typical atomic force microscopy setup, including: laser diode and four-quadrant photodiode for measuring vertical displacement, the cantilever and probe tip, and a piezoelectric sample stage.

3.3. X-ray Diffraction: Thin Film Strain and Relaxation Analysis

High-resolution X-ray diffraction (HR-XRD) is a vital step in the structural characterization of and determination of strain relaxation properties in heteroepitaxial layers. Fig. 3.4 shows a typical HR-XRD system, including: (i) an X-ray source (usually a copper (Cu) tube) that produces a broad spectrum, divergent beam of X-rays; (ii) a four-bounce Bartels monochromator that restricts the beam to a specific wavelength (energy) and angular divergence; and (iii), the sample and scintillation detector placement, including the rotation axes for both. In the most basic measurement, a rocking curve, the sample is rotated about the ω-axis, resulting in a spectrum containing peaks of various intensity, width, and angular position that directly correspond to the epitaxial layers present in the sample and their structural properties. These spectra are then used to analyze the strain relaxation properties and structural quality of the sample.

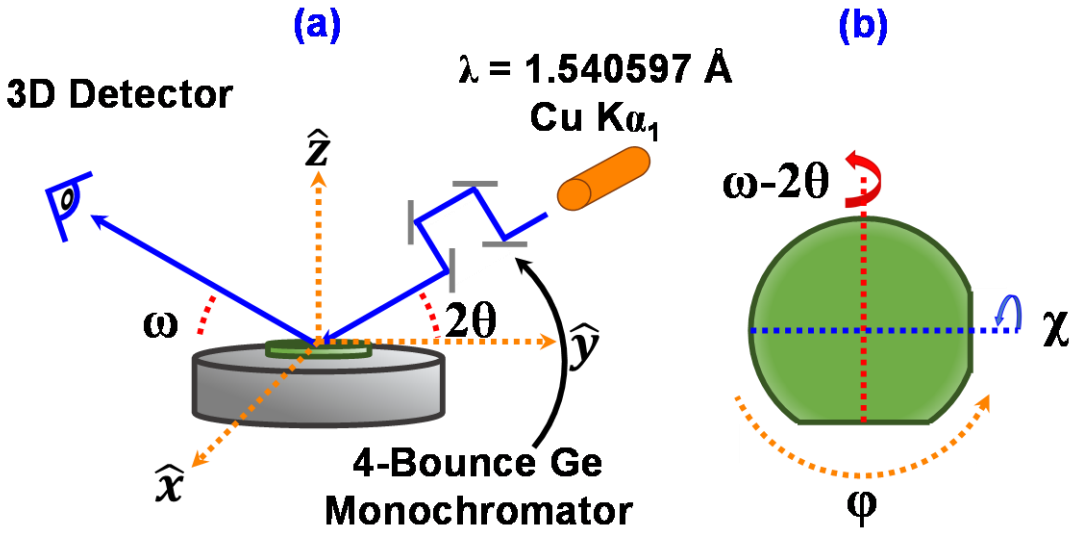

Figure 3.4 (a) Conventional high-resolution X-ray diffraction setup, including: Cu tube X-ray source, 4-bounce Ge monochromator, multi-axis sample stage, and 3D detector. (b) Sample surface showing the angular axes rotated during rocking curve and reciprocal space map measurements.

Basic structural analysis of XRD data utilizes the real and reciprocal space geometric equivalencies for angular diffraction, i.e., the Bragg and Laue equations, respectively. Fig. 3.5 shows the Bragg diffraction conditions for incident X-rays in a uniformly flat, periodic crystal structure wherein the spacing between crystal planes is given by *d* **[1]**. If the incident and reflection angles are equal to θ, then the path difference, Δ, between two parallel X-ray beams, *a* and *b*, is equal to $2d\sin(\theta)$. In this case, the condition for constructive interference becomes $\Delta = n\lambda$, where *n* is an integer and λ is the X-ray wavelength (1.540597 Å in this thesis). Thus, the Bragg diffraction condition is given by **[1]**:

$$2dsin\theta_B = n\lambda \tag{3.1}$$

where *n* is the order of reflection, θ_B is the Bragg angle, *d* is the inter-atomic plane spacing, and λ is the X-ray wavelength, as previously defined. The equivalent Laue equation for reciprocal space is given by **[1]**:

$$d\ (hkl) = \frac{a}{\sqrt{h^2+k^2+l^2}} \tag{3.2}$$

where *a* is the crystal's lattice spacing and (*hkl*) define the indices of the atomic plane under scrutiny in reciprocal space. Equating (3.1) and (3.2), the Bragg angle, θ_B (*hkl*), for an atomic plane specified by the (*hkl*) indices can be rewritten as:

$$\theta_B(hkl) = sin^{-1}\left(\frac{\sqrt{h^2+k^2+l^2}}{2a}\right) \tag{3.3}$$

The detailed strain relaxation procedure for diamond and zinc-blende semiconductors requires the recording of reciprocal space maps (RSMs), which consist of several hundred rocking curves taken at incrementally different ω center points in order to build a two-dimensional map (ω-2θ) of the diffraction angles (*vs.* intensity) present in the sample. As a result of asymmetric dislocation relaxation along the two orthogonal [110]

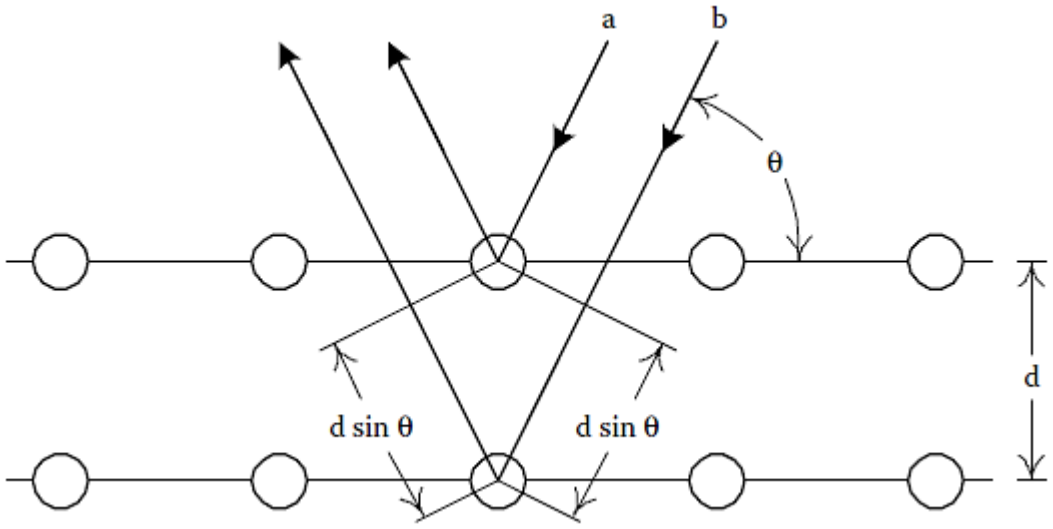

Figure 3.5 Schematic diagram of the Bragg diffraction condition for a single crystal, periodic structure.

and $[1\bar{1}0]$ directions, the in-plane lattice constants $a_{[110]}$ and $a_{[1\bar{1}0]}$ could be different. To account for this during measurement, the incident X-ray beam can be aligned with each orthogonal <110> in-plane direction in order to measure the anisotropy in strain relaxation in the sample, should any exist. In order to determine the alloy composition of ternary layers, the lattice mismatch and the strain relaxation properties for each epilayer in the sample, both symmetric (004) and asymmetric (115) RSMs must be recorded. Using Bragg's law, the in-plane, $a_{\parallel}$, and out-of-plane, $a_{\perp}$, lattice constants for each layer can be determined from the asymmetric (115) and symmetric (004) RSMs, respectively. Subsequently, the relaxed lattice constant, a_r, and epitaxial strain, ε, of each layer can be determined using **[3]**:

$$a_r = \frac{2\nu}{1+\nu} a_{\parallel} + \frac{1-\nu}{1+\nu} a_{\perp} \tag{3.4}$$

$$\varepsilon = \frac{a_r - a_s}{a_s} \tag{3.5}$$

where v is the Poisson ratio of each epilayer and a_s is the lattice constant of the substrate. For ternary materials, v is estimated using Vegard's law and the elastic constants for the binary materials composing the ternary layer, *e.g.*, InAs, GaAs, AlAs, *etc*. As noted earlier, relaxation with respect to the substrate for each epilayer can extracted along each <110> direction, and is given by **[3]**:

$$R_{[110]} = \frac{a_{\parallel,[110]} - a_s}{a_{\perp,[110]} - a_s} \text{ and } R_{[1\bar{1}0]} = \frac{a_{\parallel,[1\bar{1}0]} - a_s}{a_{\perp,[1\bar{1}0]} - a_s} \tag{3.6}$$

In the case of isotropic strain relaxation, $R_{[110]} = R_{[1\bar{1}0]}$, thus the average strain relaxation is $R = (R_{[110]} + R_{[1\bar{1}0]})/2$. The perpendicular lattice mismatch, $f_\perp$, for an epilayer with respect toan underlying virtual substrate can also be determined, and is given by **[4]**:

$$f_\perp = \frac{a_\perp - a_0}{a_0} \tag{3.7}$$

where a_0 is the relaxed lattice constant of the virtual substrate. Likewise, the parallel lattice mismatch for each $[110]$ and $[1\bar{1}0]$ direction is given by **[4]**:

$$f_{\parallel,[110]} = \frac{a_{[110]} - a_0}{a_0} \text{ and } f_{\parallel,[1\bar{1}0]} = \frac{a_{[1\bar{1}0]} - a_0}{a_0} \tag{3.8}$$

where $a_{[110]}$ and $a_{[1\bar{1}0]}$ are the epilayer's in-plane lattice constants along the $[110]$ and $[1\bar{1}0]$ directions, respectively. For a fully relaxed layer, the lattice mismatch, f_r, can be written as **[3]**:

$$f_r = \frac{1-v}{1+v} f_\perp + \frac{v}{1+v}\left(f_{\parallel,[110]} + f_{\parallel,[1\bar{1}0]}\right) \tag{3.9}$$

Fig. 3.6 shows a schematic representation of symmetric (004) and asymmetric (115) RSMs plotted according to **q** vector. The **q** vector of each epilayer in the schematic consists of two components, $\mathbf{q_x}$ and $\mathbf{q_z}$, corresponding to the angular splitting between ω and 2θ, respectively, in real space. As shown in the diagram, different strain states and

degrees of relaxation can result in different positions of the reciprocal lattice point (RLP) for each epilayer, including fully strained (pseudomorphic), fully relaxed (metamorphic), partially relaxed, or tilted (α) [5]. In the case of an ideal, fully relaxed epilayer without tilt, the (115) RLP will lie on a line of relaxation that intersects the (004) axis at an angle of 15.8°. On the other hand, a fully strained epilayer's (115) RLP will lie on a strain line that connects it *via* the (001) directed axis to its virtual substrate.

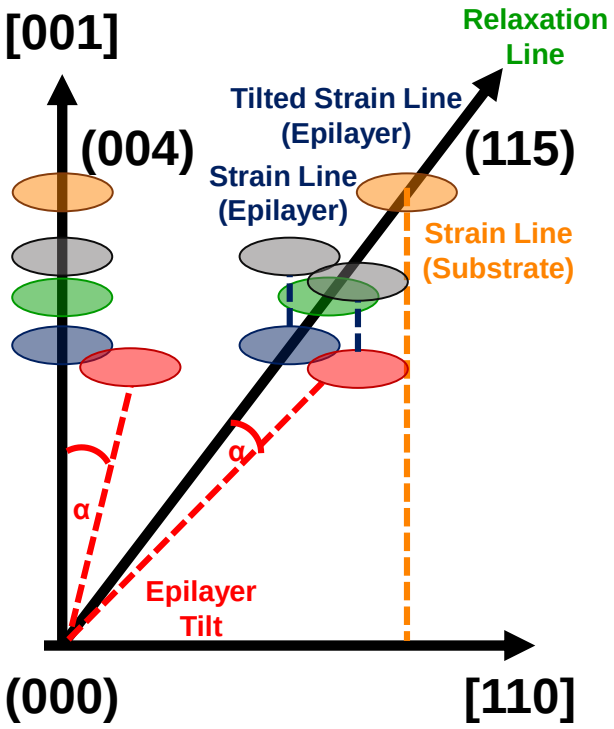

Figure 3.6 Reciprocal space schematic highlighting the sample orientations in real space as well as the crystallographic orientations in reciprocal space. The epitaxial layers of interest (blue, virtual substrate strain template, and green, strained layer) are shown under two different conditions: no epitaxial tilt (the virtual substrate strain template is orientated along the sample normal and full relaxation lines) and small epitaxial tilt (deviation away from the sample normal and full relaxation lines introduces an 'artificial error' in the measured strain relaxation properties).

3.4. Transmission Electron Microscopy: Defect and Structural Analysis

Cross-sectional high-resolution transmission electron microscopy (HR-TEM) is an excellent technique to characterize the long- and short-range structural quality of samples as well as the coherence and abruptness of heterointerfaces. In order to apply TEM imaging to semiconductor samples, electron transparent foils of thin film cross-sections must be prepared. Foils with thicknesses approximately 100 nm or less are necessary for the transmission through the sample of incident, high-energy electrons at the sample surface. Typical accelerating voltages used during TEM imaging vary from 100 KeV up to 1 MeV, depending on the instrument.

Fig. 3.7 shows a schematic diagram for a conventional TEM instrument **[2]**. High-energy electrons are collimated using magnetic condenser lenses and then focused on to the sample surface. Due to the high-energy nature of the electron beam and the extremely thin thickness of the sample, electrons are transmitted through the sample and scatter elastically or in-elastically with host atoms. In crystalline semiconductor samples, this can lead to Bragg diffraction for those electrons that scatter elastically in the sample. The diffracted beam is then brought into focus at the focal plane for the objective lens. In diffraction imaging mode, the first intermediate lens is focused on the back focal plane of the objective lens and the resulting diffraction pattern from the sample is magnified and projected by a combination of the intermediate and projection lenses. The diffraction spot pattern displayed on the phosphorous screen corresponds to different diffraction vectors, **g**, which are used to index and align the electron beam to a particular diffraction condition and assist in generating the final TEM micrograph. After diffraction alignment,

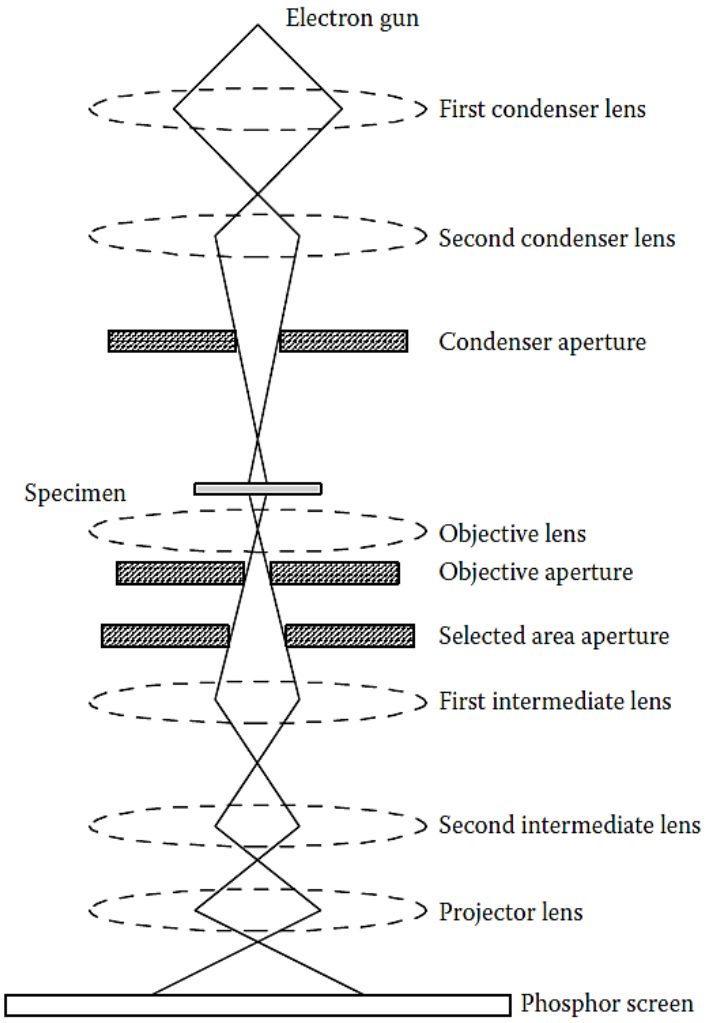

Figure 3.7 Schematic diagram showing a conventional transmission electron microscope.

inverted sample image formed by the objective lens. An aperture located at the back focal plane of the objective lens is used to select a singular diffraction condition for image formation, resulting in either a bright-field image if **g** = [000] or a dark-field image if a different **g** vector is selected. Magnification is enhanced by increasing the accelerating voltage of the electron beam.

Additional signals can be collected from the electrons that scatter in-elastically through the sample. In such cases, the transfer of energy from the incident electron beam to the host atoms generates X-rays as electrons in the host atoms radiatively relax. As the

energy separation between orbitals is different for different atoms, collection of the X-rays generated through in-elastic electron transmission can be used to determine the elemental composition of the sample. This technique is known energy-dispersive spectroscopy (EDS).

3.5. X-ray Photoelectron Spectroscopy: Heterointerface Energy Band Alignment Properties

X-ray photoelectron spectroscopy (XPS) is a useful technique for measuring the energy band alignment at semiconductor-semiconductor and oxide-semiconductor heterointerfaces. Fig. 3.8 (a) shows a conventional XPS system consisting of: (i) an electron gun, (ii) an aluminum (Al) anode, (iii) a crystal focus and monochromator, (iv) a magnetic collection lens and hemispherical energy analyzer, and (v), a photoelectron detector **[6]**. The electron gun generates Al-Kα (E = 1486.7 eV) X-rays from the Al anode target, which are then monochromated and focused by the crystal on to the sample surface. The X-rays impart enough energy to electrons in the material to eject some from the different electron core levels (*i.e.*, orbitals) in the host atoms, as shown in Fig. 3.8 (b). The X-ray-generated photoelectrons are emitted in all spatial directions; however, those that pass through the magnetic collection lens and enter the hemispherical energy analyzer are filtered with respect to kinetic energy. The relation between kinetic and binding energy for a photoelectron is given by $E_k = h\upsilon - E_b - \phi$ where $h\upsilon$ is the X-ray energy, E_b is the binding energy of a given atomic orbital, and ϕ is the work function of the sample material. Due to the different energy separations between orbitals in different atoms, the kinetic energy of a photoelectron can be used to determining the elemental constituents in the sample. However, the limited energy of the excited photoelectrons

results in a narrow escape depth of approximately 5 nm, beyond which photoelectrons generated *via* the incident X-ray beam loose too much energy through in-elastic collisions to escape the sample surface. It is worth noting that this electron mean free path limitation is also dependent on the sample material. Photoelectrons that are generated within the escape depth may also scatter in-elastically before reaching the sample surface, resulting in a broad-spectrum background in the recorded XPS spectrum. Those photoelectrons that scatter elastically and escape the sample surface result in high intensity peaks in the XPS spectrum and are used to identify the elemental nature of the sample as well as in the detailed band alignment analyses discussed in ***Chapters 4*** and ***5***.

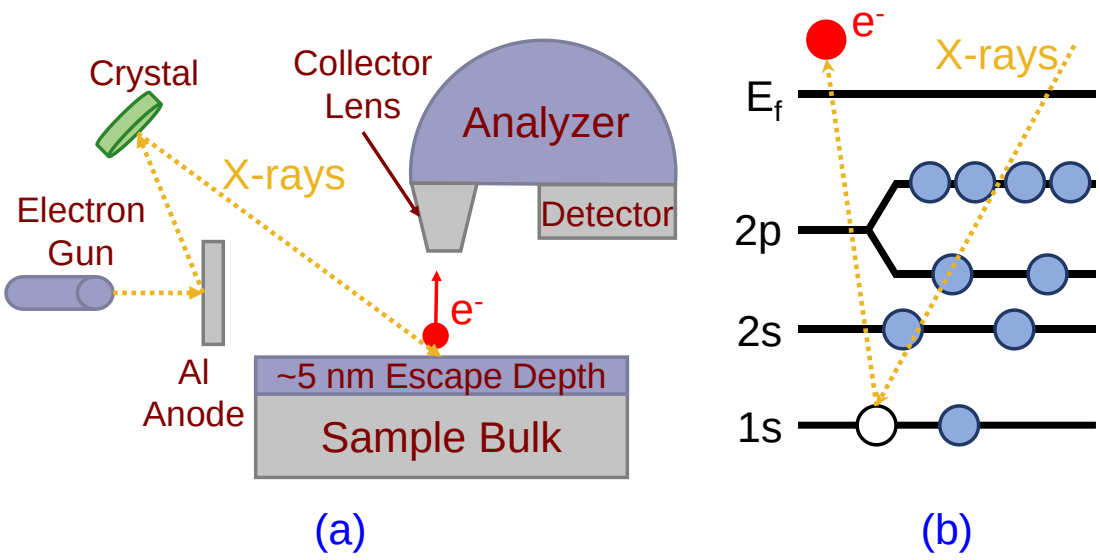

Figure 3.8 (a) X-ray photoelectron spectroscopy system, including: electron gun, Al anode, and crystal monochromator/focus [source components], sample, magnetic collector lens and hemispherical analyzer, and photoelectron detector. (b) Schematic diagram showing the nature of photoelectron generation.

3.6. Raman Spectroscopy: Thin Film Strain-State Analysis

Raman spectroscopy is a second-order (two-photon) optical measurement technique suitable for the characterization of strained semiconductor thin films and superlattices. It can be best understood as an in-elastic scattering process in which incident, monochromatic light is scattered at discrete frequencies above and below that of the incident frequency (Rayleigh scattering) **[7, 8]**. The source of these additional scattering frequencies are the vibrational modes, *i.e.*, phonon modes in a crystal, of the sample material. In the former case, radiation scattered with a frequency higher than the incident frequency is referred to as Stokes radiation, whereas in the latter case, radiation scattered with a frequency lower than the incident frequency is referred to as anti-Stokes radiation. Due to Stokes radiation being correlated with an increase in vibrational energy, and the fact that at room temperature most materials are in their lowest vibrational state, Stokes radiation is generally more intense than anti-Stokes radiation. Moreover, the vibrational, or phonon modes, that contribute to scattering are also correlated with the scattering geometry. In the case of back scattering from a (001) surface, such as the micro-Raman measurements performed in this thesis, the longitudinal optical (LO) phonons are polarized along the $\hat{z}$ direction, whereas the transverse optical (TO) phonons are polarized along the $\hat{x}$ and $\hat{y}$ directions. It follows that under (001) back scattering collection geometries, only the LO phonon modes will contribute to the detected scattered spectra. Furthermore, under strain, the normally degenerate phonon modes will be lifted, resulting in a change in the LO phonon mode frequency and thus a change in the observed Raman frequency **[8]**.

Fig. 3.9 shows a typical micro-Raman spectroscopy setup, in which an Ar laser is filtered, polarized, and focused on a sample surface through a confocal microscope down to a spot size of approximately 1 µm **[8]**. Commonly, the sample stage is automatic, thus allowing for a mapping of local stress in thin films by translation along the sample's X and Y in a well-controlled manner. The scattered light from the sample is collected through the microscope (known as a back scattering collection geometry) and directed into the double pre-monochromator, after which it enters the spectrometer prior to being detected by either a multichannel or CCD detector. As the back scattered light passes through the pre-monochromator and spectrometer, the position of the gratings and the width of the slits in both equipment determine the resolution and intensity of the detected spectral peak. In cases where the scattered intensity is low, a photomultiplier tube may be included in the measurement setup prior to the detection stage. In this thesis, a JY Horiba LabRam HR800 micro-Raman system equipped with a 514.32 nm Ar laser excitation source was used to independently measure the strain state of the Ge thin films and corroborate the strain relaxation analysis determined *via* XRD measurements.

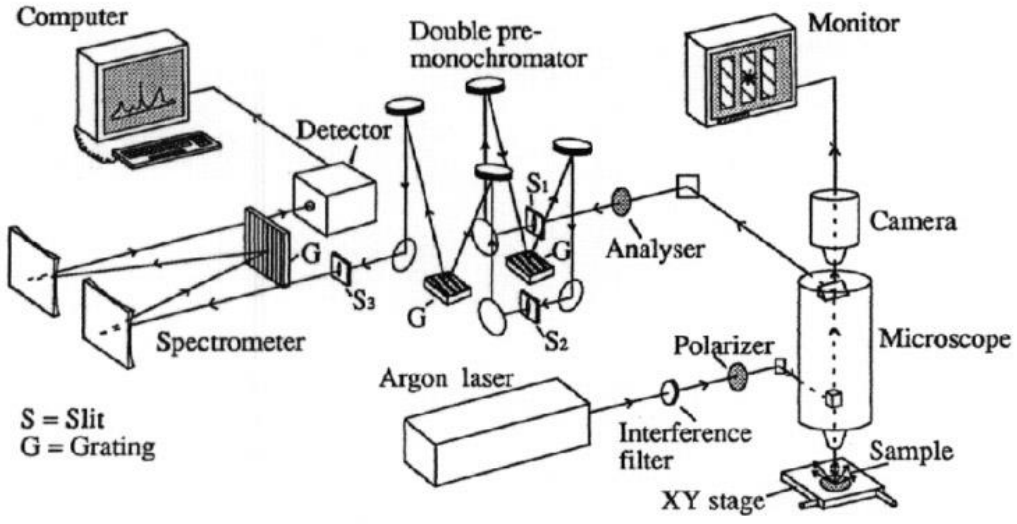

Figure 3.9 Micro-Raman spectrometer experimental setup.

3.7. Photoluminescence Spectroscopy: Analysis of Strain-Dependent Optical Properties

Photoluminescence (PL) spectroscopy is an especially valuable nondestructive, contactless measurement technique used for the investigation of the optoelectronic properties of semiconductors. In performing such measurements, a laser with above-bandgap photon energy is used to excite electron-hole pairs in the sample. The radiative recombination of the optically-pumped excess carrier population results in emission characteristics that are directly correlated with the electronic transitions in the sample. In addition to being used for determining the bandgap of electronic materials, PL spectra can yield a vast array of other material information, such as: (i) surface, interface, and impurity levels; (ii) defect levels; (iii) material quality, noting that as material quality decreases, the probability of non-radiative recombination increases; (iv) doping concentrations; (v) free- and bound-exciton recombination and binding energies; and (vi), strain or relaxation in thin-film strained-layer epitaxy **[9]**. In the case of a thin-film with residual strain or a pseudomorphic epitaxial layer, the bandgap energy (and thus emission energy) will change as a function of strain due to the simultaneous movement of the conduction band minima as well as a lifting of the heavy-hole and light-hole valence band degeneracy.

Fig 3.10 shows a conventional micro-photoluminescence (μ-PL) measurement system, including a Kr or Ar laser excitation source, filters to remove unwanted wavelengths, choppers to modulate the excitation beam for lock-in detection, a cryostat for cryogenic (liquid N_2 or He_4) sample measurement, a single or double grating monochromator, and detector (typical cooled to improve the signal-to-noise ratio) **[7]**. In

such a setup, the spectral (energy) resolution is limited by the focal length of the monochromator and the detection range is determined by the monochromator grating. For the μ-PL measurements performed in this thesis, an 800 nm laser source and a thermoelectric cooled InGaAs detector were used for optical pumping and detection, respectively.

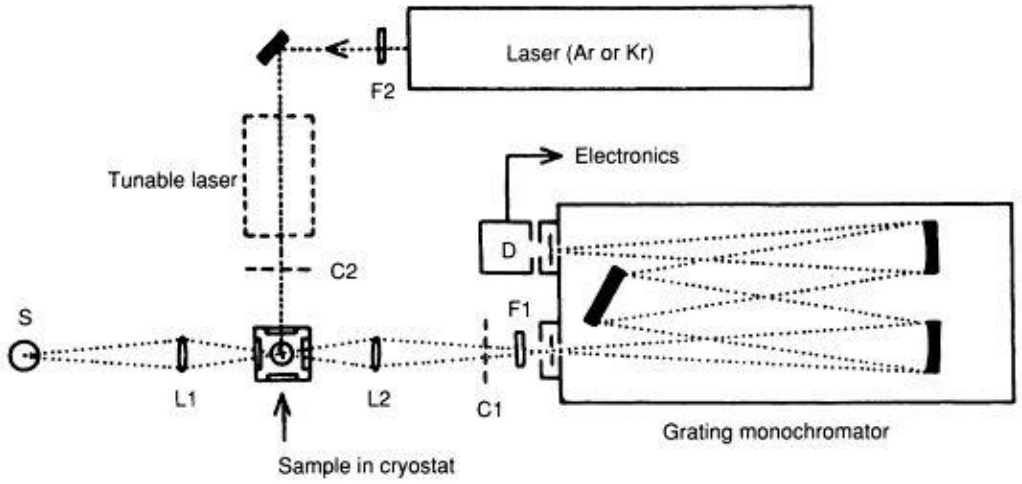

Figure 3.10 Conventional micro-photoluminescence (μ-PL) measurement system, including Ar laser and choppers (C1, C2), cryostat for cryogenic sample measurements, grating monochromator, detector, focusing lens (L2), and filters (F1, F2).

References

[1] J. E. Ayers, *Heteroepitaxy of Semiconductors: Theory, Growth, and Characterization*, Chapters 3 and 6, CRC Press (2007).

[2] U. W. Pohl, *Epitaxy of Semiconductors: Introduction to Physical Principles*, Chapter 7, Springer (2013).

[3] M. K. Hudait, Y. Lin and S. A. Ringel, Strain Relaxation Properties of $InAs_yP_{1-y}$ Metamorphic Materials Grown on InP Substrates, *J. Appl. Phys.* **105**, 061643-1—061643-12 (2009).

[4] P. F. Fewster, *X-ray Scattering from Semiconductors*, 2nd Ed., Chapter 4, Imperial College Press: London (2003).

[5] J. M. Chauveau, Y. Androussi, A. Lefebvre, J. Di Persio and Y. Cordier, Indium Content Measurements in Metamorphic High Electron Mobility Transistor Structures by Combination of X-Ray Reciprocal Space Mapping and Transmission Electron Microscopy, *J. Appl. Phys.* **93**, 4219-4225 (2003).

[6] J. C. Vickerman and I. S. Gilmore, *Surface Analysis – The Principle Techniques*, 2nd Ed., Chapter 3, Wiley (2009).

[7] S. Perkowitz, *Optical Characterization of Semiconductors: Infrared, Raman, and Photoluminescence Spectroscopy*, Chapters 2-6, Elsevier (1993).

[8] I. De Wolf, Micro-Raman Spectroscopy to Study Local Mechanical Stress in Silicon Integrated Circuits, *Semicond. Sci. Technol.* **11**, 139-154 (1996).

[9] G. D. Gilliland, Photoluminescence Spectroscopy of Crystalline Semiconductors, *Mater. Sci. Eng., R* **18**, 99-399 (1997).

Chapter 4 – Tensile-strained Ge/$In_xGa_{1-x}As$ Heterostructures for Low-Power, High-Speed Logic

As discussed in the preceding chapters, much of the recent research **[1–13]** into future TFET architectures has focused on compositionally tailored III-V type-II staggered gap materials, such as $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructures. By comparison, considerably less effort has been devoted to alternative Ge/$In_xGa_{1-x}As$ heterojunction TFET material systems **[13–17]**. In such hybrid group IV (Ge or Ge_xSn_{1-x}) and group III-V ($In_xGa_{1-x}As$) TFET architectures, the effective tunneling barrier height, tunneling current, and heterointerface band alignment can be tailored by varying the indium (In) alloy composition in the $In_xGa_{1-x}As$ virtual substrate **[10, 11, 13–16]**. A key challenge in realizing such Ge/$In_xGa_{1-x}As$ TFET devices is the trade-off between the In alloy composition of the $In_xGa_{1-x}As$ strain template and the strained-layer critical thickness, h_c, of the epitaxial Ge (Ge_xSn_{1-x}). Moreover, the ability to grow atomically precise tunneling interfaces with limited atomic species inter-diffusion while maintaining coherent strained layer epitaxy is necessary to maximize ON-state current (I_{ON}) and reduce trap-assisted tunneling and carrier recombination at the heterointerface, thereby suppressing leakage current (I_{OFF}) **[12]**. Whereas recent simulation **[13]** and experimental work **[14]** has either predicted significant enhancements in I_{ON} or demonstrated control over the tunneling barrier height through tensile-strained Ge/$In_xGa_{1-x}As$ heterostructures with moderate strain, this chapter provides a comprehensive experimental investigation of the structural, morphological, and band alignment properties of highly ($\varepsilon \leq 1.94\%$) biaxial tensile-strained Ge/$In_xGa_{1-x}As$ TFET heterostructures.

4.1. MBE Growth of ε-Ge/$In_xGa_{1-x}As$ TFET Heterostructures on GaAs

In this chapter, three tensile-strained Ge (ε-Ge)/$In_xGa_{1-x}As$ TFET heterostructures with different In compositions were grown *in-situ* by solid source MBE utilizing separate III-V and Ge growth chambers connected *via* an ultra-high vacuum transfer chamber. The Ge/$In_xGa_{1-x}As$ heterojunctions were integrated onto (100)GaAs substrates by way of an initial 0.25 µm GaAs buffer followed by a linearly graded $In_xGa_{1-x}As$ metamorphic buffer, thereby accommodating the lattice mismatch between the Ge/$In_xGa_{1-x}As$ active region and the GaAs substrate and minimizing defect and dislocation propagation through the layers of interest. Thickness in the range of 500 nm to 650 nm constant composition $In_xGa_{1-x}As$ was selected as a virtual substrate for the proceeding tensile-strained Ge growth, with the strain-transfer modulated by tailoring the In composition of the $In_xGa_{1-x}As$ virtual substrate.

The complete ε-Ge/$In_xGa_{1-x}As$ structures were grown on epi-ready semi-insulting (100)GaAs substrates that were 2° offcut towards the <110> direction, thereby minimizing the formation of anti-phase domain boundaries at the interface between the ε-Ge and GaAs ($In_xGa_{1-x}As$) modulation-doping (capping) layers **[18-23]**. All growth temperatures were monitored via thermocouple and controlled remotely using calibrated Eurotherm 2404/8 PID controllers. Substrate oxide desorption occurred at ~750°C in the III-V growth chamber under an over pressure of arsenic flux (~10^{-5} Torr), and was monitored in-situ using reflection high-energy electron diffraction (RHEED). RHEED patterns were also examined following each epilayer growth to monitor their associated surface reconstructions. For this work, three In compositions were considered, explicitly

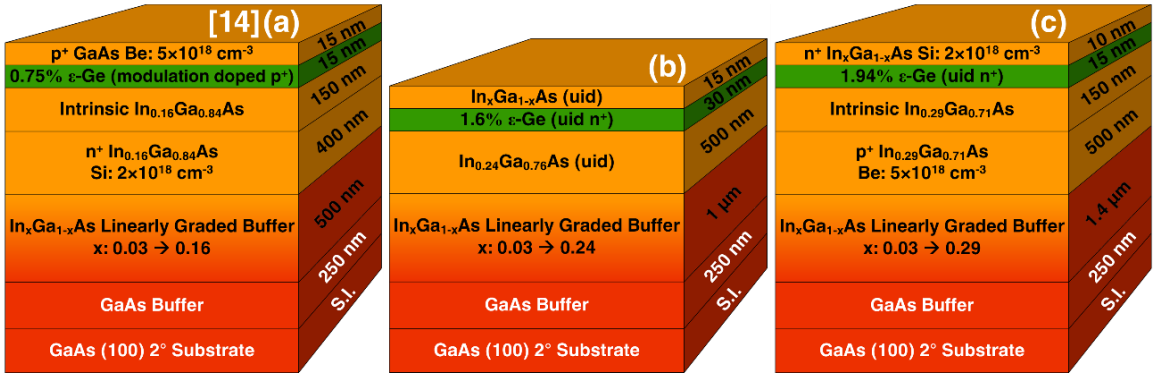

Figure 4.1 Cross-sectional schematics of the (a) 0.75% ε-Ge/$In_{0.16}Ga_{0.84}As$ **[14]**, (b) 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$, and (c) 1.94% ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structures. © 2015 IEEE.

(0.75% tensile strain), 24% (1.6%), and 29% (1.94%). As such, the In composition of the linearly graded buffer was varied from 3% to 16%, 24%, or 29%, respectively, utilizing corresponding strain grading rates of 2.23 % strain/µm, 1.70 % strain/µm, and 1.46 % strain/µm. The reduction in strain grading rate followed the increase in misfit between the constant composition layer and the GaAs substrate, thereby aiding in relaxation of the higher In alloy composition graded buffers **[24-26]**. Upon completion of the III-V metamorphic buffer growth, the substrate was cooled from the growth temperature of 550°C down to 150°C under an As_2 overpressure and then transferred *via* an ultra-high vacuum transfer chamber to the Ge growth chamber. Thin 15 nm to 30 nm tensile-strained Ge epilayers were then grown at 400°C on the $In_xGa_{1-x}As$ virtual substrates utilizing a low Ge growth rate of ~0.025 µm per hour. After epitaxial Ge growth, the samples were moved back to the III-V growth chamber for the growth of thin capping layers of GaAs or $In_xGa_{1-x}As$ in order to protect the ε-Ge surface from oxidation. Fig. 4.1 shows the labeled schematics for the 16%, 24%, and 29% In composition ε-Ge/$In_xGa_{1-x}As$ TFET structures, respectively. Note that Figs. 4.1 (a) and (c) are complete TFET

structures with practical source/channel/drain (p^+-i-n^+ or n^+-i-p^+) configurations. In the case of the $In_{0.16}Ga_{0.84}As$ structure (Fig. 4.1 (a)), the n^+ $In_{0.16}Ga_{0.84}As$:Si drain doping concentration was selected to be 2×10^{18} cm^{-3}, while the *p*-type (Be) drain doping concentration in the $In_{0.29}Ga_{0.71}As$ structure (Fig. 4.1 (b)) was chosen to be 5×10^{18} cm^{-3}. Additionally, whereas the ε-Ge epilayers of the $In_{0.24}Ga_{0.76}As$ (Fig. 4.1 (b)) and $In_{0.29}Ga_{0.71}As$ structures are unintentionally doped, that of the $In_{0.16}Ga_{0.84}As$ structure is modulation doped *via* the heavily p-type (5×10^{18}) GaAs:Be contact layer.

HR-XRD was utilized in the strain analysis of the ε-Ge/$In_xGa_{1-x}As$ heterointerfaces and was performed on a PANalytical X-Pert Pro system equipped with a Cu Kα-1 line-focused x-ray source. Both rocking curve and RSM measurements were used in determining the strain transferred to the Ge lattice as well as the composition of the underlying $In_xGa_{1-x}As$ virtual substrate. Surface morphology analysis was carried out using a Bruker Dimension Icon atomic force microscope in tapping mode. To characterize the structural quality of the ε-Ge/$In_xGa_{1-x}As$ TFET structures, including defect and dislocation confinement, film crystallinity, interface quality, and interface coherence of each ε-Ge/$In_xGa_{1-x}As$ heterojunction, cross-sectional TEM micrographs were captured using a JEOL 2100 microscope. The required electron transparent foils were prepared by a conventional mechanical milling procedure followed by a low-temperature Ar^+ ion milling. The energy band alignment properties of each ε-Ge/$In_xGa_{1-x}As$ heterointerface were investigated using XPS on a PHI Quantera SXM system utilizing a monochromatic Al Kα (1486.7 eV) X-ray source. All XPS spectra were recorded using a pass energy of 26 eV and an exit angle of 45°. Spectral analysis was

performed with CasaXPS v2.3.14 using a Lorentzian convolution with a Shirley-type background and corrected with the adventitious carbon peak binding energy of 285.0 eV.

4.2. Strain Relaxation Properties of ε-Ge/$In_xGa_{1-x}As$ Heterostructures Grown on GaAs

The relaxation state and residual strain of each TFET heterostructure shown in Fig. 4.1 were determined using HR-XRD. Fig. 4.2 shows the symmetric (004) rocking curves for the ε-Ge/$In_{0.16}Ga_{0.84}As$ **[14]** (top, green), ε-Ge/$In_{0.24}Ga_{0.76}As$ (middle, blue), and ε-Ge/$In_{0.29}Ga_{0.71}As$ (bottom, orange) TFET structures. As can be seen in Fig. 4.2, an increase in In composition of the $In_xGa_{1-x}As$ virtual substrate corresponds to an increase in the Bragg angle of the epitaxial Ge thin-film, thereby indicating a reduction in the out-of-plane Ge lattice constant ($a_{\perp}$) for increasing In composition. This can be explained by the following: as the lattice constant of the $In_xGa_{1-x}As$ virtual substrate increases with increased In composition, the in-plane Ge lattice constant ($a_{\parallel}$) becomes progressively stretched to accommodate the mismatch between the two layers. To compensate for the change in the Ge unit cell volume, the out-of-plane Ge lattice constant is reduced proportionally to the increase in the in-plane Ge lattice constant. Thus, the observed shrinkage in out-of-plane Ge lattice constant suggests the presence of an increasing in-plane biaxial tensile strain that is modulated by the composition of the underlying $In_xGa_{1-x}As$ buffer. Further investigation to quantify the relaxation state of the $In_xG_{1-x}As$ virtual substrates and tensile strain held by the Ge epilayers was performed using symmetric (004) and asymmetric (115) reciprocal space map analysis, as shown by Figs. 3 (a) and 3 (b), respectively. Using the (004) and (115) RSMs and the methods introduced in

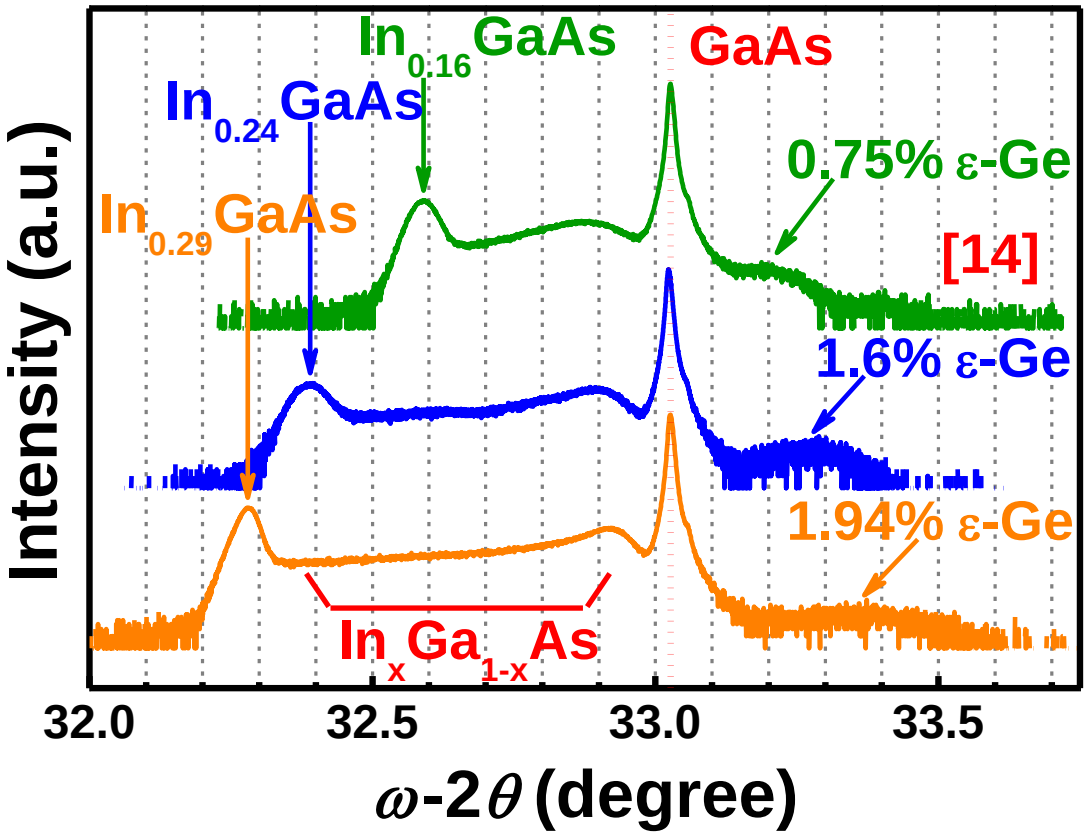

Figure 4.2 Symmetric (004) rocking curve (ω/2θ scan) of the strain-engineered ε-Ge/$In_{0.16}Ga_{0.84}As$ (green) **[14]**, ε-Ge/$In_{0.24}Ga_{0.76}As$ (blue), and ε-Ge/$In_{0.29}Ga_{0.71}As$ (orange) heterostructures. © 2015 IEEE.

were then used together with the material's Poisson ratio, ν, to compute the relaxed lattice constant, a_r, of the layer **[4, 28]**. Vegard's law was used along with the experimentally determined $In_xGa_{1-x}As$ relaxed lattice constant to evaluate the In composition and relaxation state of the $In_xGa_{1-x}As$ virtual substrate. The experimentally-derived In compositions were found to be 15.7% **[14]**, 23.7%, and 28.5% for the ε-Ge/$In_{0.16}Ga_{0.84}As$, ε-Ge/$In_{0.24}Ga_{0.76}As$, and ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structures, respectively, which were consistent with the design criteria. Furthermore, the 15.7% and 23.7/28.5% composition $In_xGa_{1-x}As$ virtual substrates were found to be approximately 90% **[14]** and 99% relaxed

with respect to the GaAs substrate, respectively, suggesting that the lattice mismatch between the GaAs substrate and ε-Ge/$In_xGa_{1-x}As$ active region was effectively accommodated by the $In_xGa_{1-x}As$ metamorphic buffer in all cases. Moreover, the amount of tensile strain within the Ge epilayers was found to be 0.75% **[14]**, 1.6% and 1.94% for the $In_{0.16}Ga_{0.84}As$, $In_{0.24}Ga_{0.76}As$, and $In_{0.29}Ga_{0.71}As$ virtual substrates, respectively. In addition, as can be seen in the asymmetric (115) RSM in Fig. 3 (b), the Ge reciprocal lattice point (RLP) for each heterostructure is aligned vertically with the $In_xGa_{1-x}As$ RLP (shown by the orange dashed lines), validating the pseudomorphic nature of the ε-Ge/$In_xGa_{1-x}As$ heterojunction. Table 4.1 shows the strain relaxation values of the $In_xGa_{1-x}As$ and tensile-strained Ge epilayers obtained from X-ray analysis.

The theoretical critical layer thickness (h_c) for each ε-Ge/$In_xGa_{1-x}As$ heterostructure was calculated using the energy balance model developed by People and Bean **[29]** for compressively strained systems, given by (4.1) below, and is also included in Table 4.1:

$$h_c \simeq \left(\frac{1-\nu}{1+\nu}\right)\left(\frac{1}{16\sqrt{2}\pi}\right)\left[\frac{b^2}{a}\right]\left[\left(\frac{1}{f^2}\right)\ln\left(\frac{h_c}{b}\right)\right] \tag{4.1}$$

where ν is the Poisson ratio of the epitaxially strained material ($\nu_{Ge} \approx 0.26$ **[30]**), a is that material's bulk lattice constant (a_{Ge} = 5.658 Å **[31]**), f is the lattice mismatch between the substrate and the strained epitaxial layer, h_c is the critical layer thickness of the strained epilayer, and b is the magnitude of the Burger's vector along the $\frac{a}{2}\langle 011\rangle$ slip direction ($b_{Ge} \approx 4$ Å **[29]**). In this model, the impact of the growth temperature was not considered in calculating the h_c value. It is worth noting that the designed ε-Ge epilayer thicknesses, 15 nm (ε-Ge/$In_{0.16}Ga_{0.84}As$), 30 nm (ε-Ge/$In_{0.24}Ga_{0.76}As$), and 15 nm (ε-Ge/$In_{0.29}Ga_{0.71}As$), remain well below the calculated h_c values, therefore it is expected

that the strain relaxation in the epitaxial ε-Ge would be minimal. This result reinforces the conclusion drawn via XRD analysis regarding the strain-state of the ε-Ge epilayers and the pseudomorphic quality of the ε-Ge/$In_xGa_{1-x}As$ interface. The calculated h_c reported here are also in good agreement with recent experimental work examining ε-Ge critical layer thickness in the low misfit regime **[32]**, thereby validating the suitability of the energy balance model in describing the ε-Ge/$In_xGa_{1-x}As$ material system. Thus, in conjunction with the predicted reduction in band gap and carrier effective mass in the Ge source **[33, 34]**, the pseudomorphic nature of the studied ε-Ge/$In_xGa_{1-x}As$ heterointerfaces is promising for the tailored design of ε-Ge/$In_xGa_{1-x}As$ TFETs with improved ON current and a modulated tunneling barrier height.

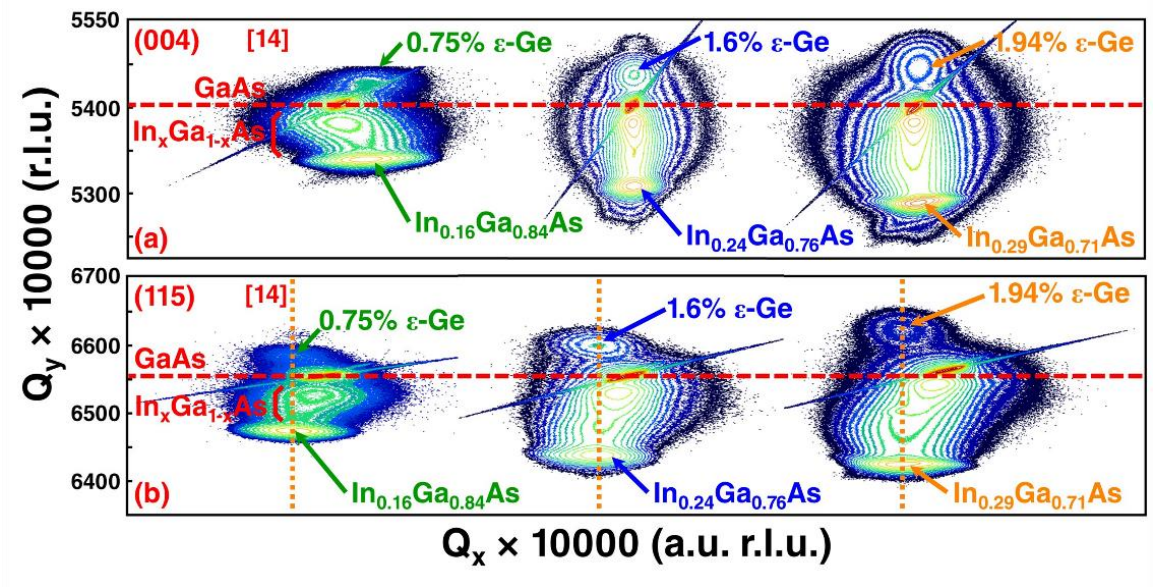

Figure 4.3 (a) Symmetric (004) and (b) asymmetric (115) reciprocal space maps (RSMs) of the TFET structures. The in-plane tensile strain values of the Ge epilayer were found to be 0.75% **[14]**, 1.6% and 1.94%, respectively. © 2015 IEEE.

Material	Lattice Constant (Å)			In Composition (%)	Tensile Strain, Ge (%)	Critical Layer Thickness (nm)
	Out-of-Plane ($a_\perp$)	In-Plane ($a_\parallel$)	Relaxed (a_r)			
ε-Ge/$In_{0.16}Ga_{0.84}As$ [14]	5.7201	5.7123	5.7164	15.7	0.75	270.8
ε-Ge/$In_{0.24}Ga_{0.76}As$	5.7506	5.7478	5.7492	23.7	1.6	42.6
ε-Ge/$In_{0.29}Ga_{0.71}As$	5.7693	5.7677	5.7685	28.5	1.94	25.9

Table 4.1 Summary of the strain relaxation properties of the ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures studied in this work. © 2015 IEEE.

4.3. Surface Morphology of ε-Ge/$In_xGa_{1-x}As$ Metamorphic Systems

Characterization of the surface morphology for each TFET structure is directly associated with the dominant strain relief mechanisms during growth, thereby providing important metrics for threading dislocation dynamics and residual stresses within the buffer. Metamorphic buffer architectures exhibit the formation of 60° a/2 <110> {111} misfit dislocations during relaxation, which can thereafter glide along {111} planes at a 60° angle toward the surface normal and propagate laterally along <110> directions **[35-37]**. The resulting cross-hatch pattern at the sample surface is therefore reflective of the relaxation state of the linearly graded buffer **[35–37]**. Figs. 4 (a)-(c) show the 20 µm × 20 µm AFM scans of the $In_{0.16}Ga_{0.84}As$ **[14]**, $In_{0.24}Ga_{0.76}As$, and $In_{0.29}Ga_{0.71}As$ TFET structures, respectively, all of which display the anticipated two-dimensional (2D) cross-hatch surface morphology. Figs. 4 (a) and 4 (c) reveal uniform, well-developed 2D cross-hatch patterns parallel to the [110] and $[1\bar{1}0]$ directions, whereas the cross-hatch shown in Fig. 4 (b) was weak due to the suppression of ridges and valleys resulting from an increased strained layer thickness ($t_{\varepsilon\text{-Ge}} + t_{In_xGa_{1-x}As}$). Furthermore, the granular appearance superimposed on the underlying cross-hatch patterns of the $In_{0.24}Ga_{0.76}As$ and $In_{0.29}Ga_{0.71}As$ sample surfaces (Figs. 4 (b) and 4 (c), respectively) is likely due to the transition from a Frank-van der Merwe (2D) to a Stranski-Krastanov (3D) growth mode during, but not before, the $In_xGa_{1-x}As$ capping layer growth. In such a 2D-to-3D growth transition, the ε-Ge epilayer serves as a strained virtual substrate for the subsequent $In_xGa_{1-x}As$ layer growth. The strain energy at the growth surface is sufficiently large such that while the $In_xGa_{1-x}As$ growth is coherent, it favors the formation of lower-energy

island-like $In_xGa_{1-x}As$ structures rather than uniform, planar epitaxy. Line profiles along the two orthogonal <100> directions are also included with each AFM micrograph, and show an increase in peak-to-valley height from 5 nm to 16 nm with increasing In buffer composition. The root-mean-square (rms) roughness for the $In_{0.16}Ga_{0.84}As$, $In_{0.24}Ga_{0.76}As$, and $In_{0.29}Ga_{0.71}As$ TFET designs was measured to be 1.26 nm **[14]**, 4.24 nm, and 4.34 nm, respectively. Moreover, the well-developed and uniform 2D cross-hatch surface morphology for each TFET structure supports a symmetric strain relaxation of the metamorphic buffer and is indicative of a low threading dislocation density **[4]**.

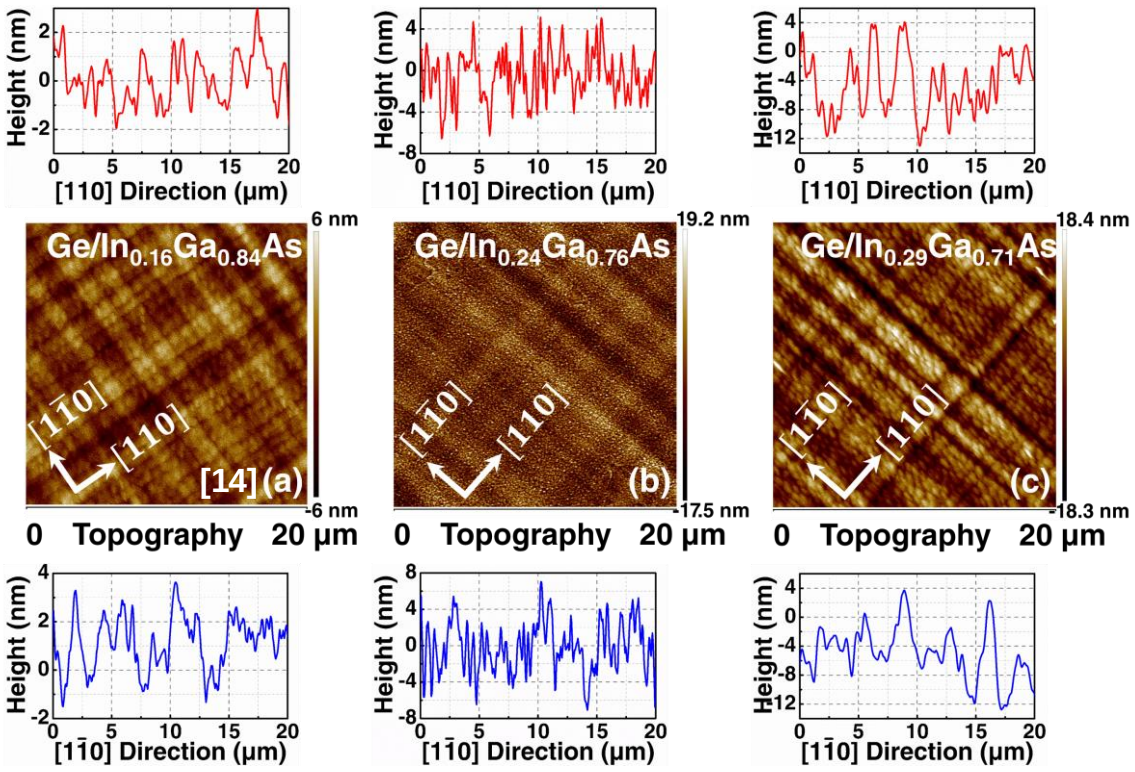

Figure 4.4 20 μm × 20 μm AFM micrographs of the (a) 0.75% ε-Ge/$In_{0.16}Ga_{0.84}As$ **[14]**, (b) 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$, and (c) 1.94% ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structures showing well-developed, uniform two-dimensional cross-hatch surface morphology. © 2015 IEEE.

4.4. Structural, Defect and Dislocation Analysis of ε-Ge/$In_xGa_{1-x}As$ Heterointerfaces

Further insight into the structural and crystalline quality of the ε-Ge/$In_xGa_{1-x}As$ active layer, in addition to the strain-state, was provided by low- and high-resolution cross-sectional TEM analysis. Fig. 5 **[14]** and Fig. 6 show the bright field cross-sectional TEM micrographs of the low- and high-strain (i.e., $In_{0.16}Ga_{0.84}As$ and $In_{0.29}Ga_{0.71}As$) TFET structures, respectively. As seen in Fig. 5 (a) and Fig. 6 (a), the $In_xGa_{1-x}As$ metamorphic buffer confines defect propagation via dislocation formation and glide, thereby effectively accommodating the lattice mismatch between the GaAs substrate and the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ (Ge/$In_{0.29}Ga_{0.71}As$) active region. The subsequent 550 nm (650 nm) $In_{0.16}Ga_{0.84}As$ ($In_{0.29}Ga_{0.71}As$) virtual substrate growth exhibits a minimal dislocation density that is not detectable at low magnification. Furthermore, the generation and confinement of mismatch-induced dislocations within the $In_xGa_{1-x}As$ linearly graded buffer supports the quasi-ideal relaxation of residual strain in the overlying virtual substrate, which is in agreement with the XRD and AFM analysis. Fig. 5 (b) and Fig. 6 (b) highlight the abrupt nature of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ and Ge/$In_{0.29}Ga_{0.71}As$ heterointerfaces, respectively. The high contrast observed between the Ge and the GaAs/$In_xGa_{1-x}As$ demonstrates uniform, sharp heterojunctions absent of dislocations, thus reinforcing the pseudomorphic nature of the epitaxial Ge as revealed by XRD analysis above. Moreover, the atomically abrupt interfaces are necessary to minimize the effective tunneling barrier width and increase the tunneling current in ε-Ge/$In_xGa_{1-x}As$ TFET device architectures **[1–12]**.

To further examine the transfer of strain from the $In_{0.16}Ga_{0.84}As$ ($In_{0.29}Ga_{0.71}As$) virtual substrate to the Ge epilayer, Fast Fourier Transform (FFT) analysis was performed within the active Ge and $In_{0.16}Ga_{0.84}As$ ($In_{0.29}Ga_{0.71}As$) source and channel layers as well as at their interface. Figs. 5 (c)-(e) and Figs. 6 (c)-(e) show the FFT patterns corresponding to the regions indicated with arrows in Fig. 5 (b) and Fig. 6 (b), respectively. As shown in Figs. 6 (c)-(e), the indistinguishable nature of the recorded diffraction patterns (i.e. the zone axis preservation across the heterointerface) suggest the near-perfect accommodation of the Ge in-plane lattice to that of the underlying $In_{0.29}Ga_{0.71}As$ channel. Likewise, the absence of diffraction spot splitting and satellite peaks in Fig. 6 (d) indicates a coherent epitaxial growth of the highly tensile-strained Ge with respect to the $In_{0.29}Ga_{0.71}As$ virtual substrate. Similar results can been seen for the low-strain TFET structure as seen in Figs. 5 (c)-(e). This combination of data from low- and high-resolution TEM analysis demonstrates the device-quality of the tunable ε-$Ge/In_xGa_{1-x}As$ heterostructures. Precise control over the In composition within the linearly graded buffer and the optimization of growth parameters thereby producing atomically abrupt heterojunctions with long-range uniformity and a complete strain transfer to the epitaxial Ge were achieved in this study. Coupled with a low defect density within the active layers, the observed control over the heterointerface quality in the studied TFET structures is critical for enhancing the device performance (e.g., tunneling current, effective tunneling barrier, etc.) in ε-$Ge/In_xGa_{1-x}As$-based TFET architectures.

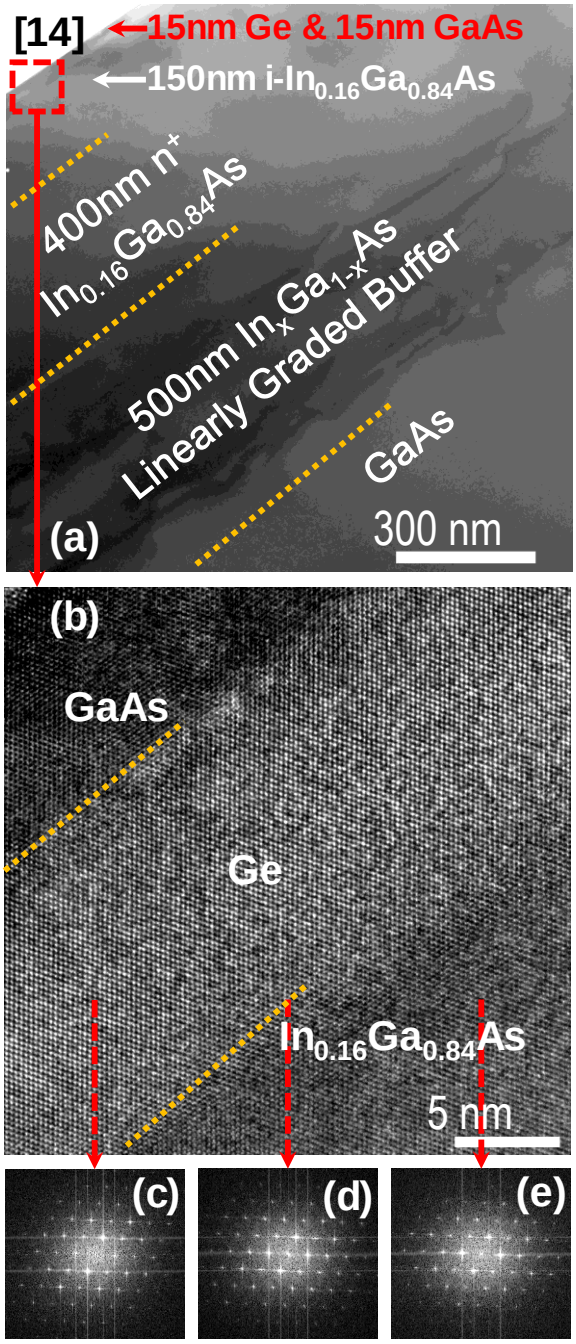

Figure 4.5 (a) Low-magnification cross-sectional TEM micrograph of the ε-Ge/$In_{0.16}Ga_{0.84}As$ TFET structure [14]. (b) High-magnification TEM micrograph of the GaAs/ε-Ge/$In_{0.16}Ga_{0.84}As$ heterojunction, and Fast Fourier Transform patterns corresponding to (c) ε-Ge, (d) the ε-Ge/$In_{0.16}Ga_{0.84}As$ interface, and (e) the $In_{0.16}Ga_{0.84}As$ virtual substrate. © 2015 IEEE.

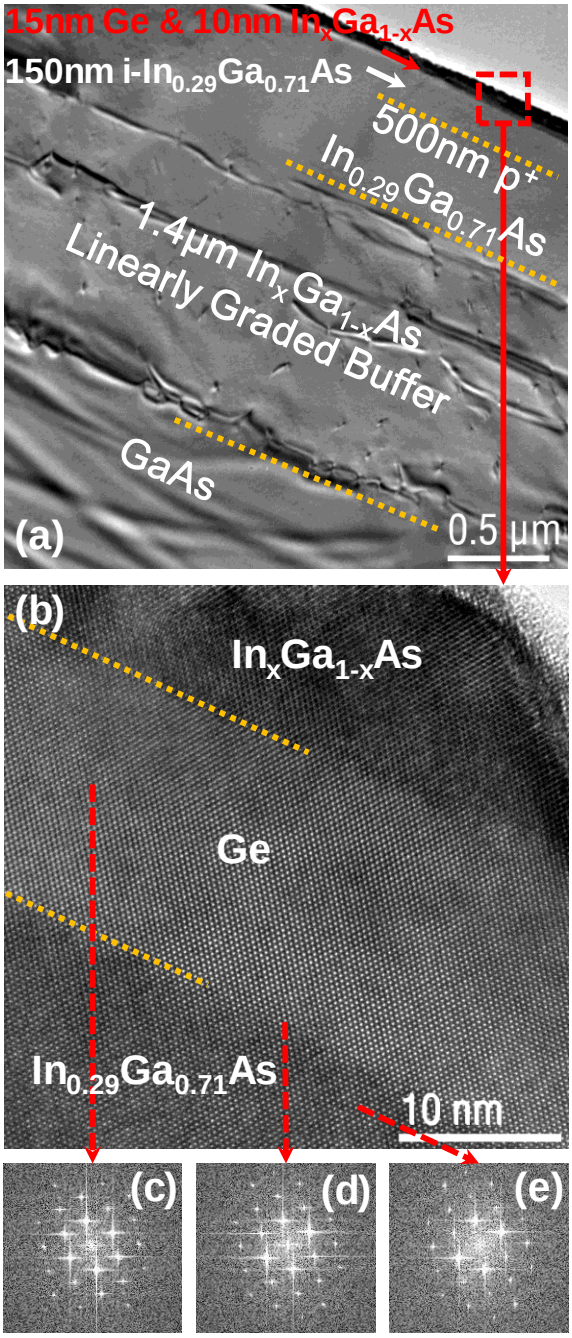

Figure 4.6 (a) Low-magnification cross-sectional TEM micrograph of the ε-Ge/$In_{0.29}Ga_{0.71}As$ TFET structure. (b) High-magnification TEM micrograph of the ε-Ge/$In_{0.29}Ga_{0.71}As$ heterointerface, and Fast Fourier Transform patterns corresponding to (c) highly-strained ε-Ge, (d) the ε-Ge/$In_{0.29}Ga_{0.71}As$ interface, and (e) the $In_{0.29}Ga_{0.71}As$ virtual substrate. © 2015 IEEE.

4.5. Strain Modulated Energy Band Alignments of ε-Ge/$In_xGa_{1-x}As$ Tunneling Heterojunctions

The band alignment properties of each ε-Ge/$In_xGa_{1-x}As$ heterointerface were investigated in order to quantify the impact of tensile strain and In alloy composition in the $In_xGa_{1-x}As$ virtual substrate on the source-channel effective tunneling barrier height (E_{beff}). The following XPS spectra were recorded for each ε-Ge/$In_xGa_{1-x}As$ structure: (i) the Ge 3d core level (CL) and valence band maxima (VBM) from a thick (> 10 nm, i.e. greater than the photoelectron escape depth for photoemission generated by the underlying $In_xGa_{1-x}As$) ε-Ge epilayer; (ii) the As 3d CL and $In_xGa_{1-x}As$ VBM from the $In_xGa_{1-x}As$ virtual substrate; and (iii) the Ge 3d CL and As 3d CL from a thin (< 2 nm, i.e. less than the photoelectron escape depth for photoemission generated by the underlying $In_xGa_{1-x}As$) ε-Ge epilayer. Surface native oxide was removed in-situ via a 5 s low energy Ar^+ ion sputter prior to collecting the XPS spectra. Utilizing the measured binding energy spectra, the valence band offset (ΔE_V) can be directly determined using the method introduced by Kraut et al. **[38]**:

$$\Delta E_V = (E_{Ge3d}^{\varepsilon-Ge} - E_{VBM}^{\varepsilon-Ge}) - (E_{As3d_{5/2}}^{In_xGa_{1-x}As} - E_{VBM}^{In_xGa_{1-x}As}) - \Delta CL(i) \qquad (4.2)$$

where $E_{Ge3d}^{\varepsilon-Ge}$ and $E_{As3d_{5/2}}^{In_xGa_{1-x}As}$ are the CL binding energies for Ge and As ($In_xGa_{1-x}As$), respectively, E_{VBM} is the VBM for each material, and $\Delta CL(i)$ is the binding energy separation between the measured interfacial As 3d and Ge 3d CLs, i.e. $E_{Ge3d}^{\varepsilon-Ge} - E_{As3d_{5/2}}^{In_xGa_{1-x}As}$, for each material was determined by performing a linear regression fitting of the leading edge of the valence band (VB) spectra referenced to the background-dependent base line

[7, 8, 12, 14, 16]. The conduction band offset (ΔE_C) can then be calculated using **[7, 8, 12, 14, 16, 38]**:

$$\Delta E_C = E_g^{In_xGa_{1-x}As} - E_g^{\varepsilon\text{-}Ge} - \Delta E_V \tag{4.3}$$

where $E_g^{\varepsilon\text{-}Ge}$ and $E_g^{In_xGa_{1-x}As}$ are the band gap energies of Ge and $In_xGa_{1-x}As$, respectively. Fig. 7 shows the measured CL and VB spectra for the 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$ heterojunction and the structural diagrams of the sample from which the spectra were recorded (insets). The measured binding energy separations were found to be 29.52eV, 40.74eV, and 11.57eV for the $E_{Ge3d}^{\varepsilon\text{-}Ge} - E_{VBM}^{\varepsilon\text{-}Ge}$, $E_{As3d_{5/2}}^{In_{0.24}Ga_{0.76}As} - E_{VBM}^{In_{0.24}Ga_{0.76}As}$, and $E_{Ge3d}^{\varepsilon\text{-}Ge} - E_{As3d_{5/2}}^{In_{0.24}Ga_{0.76}As}$ separations, respectively, resulting in a ΔE_V of 0.35±0.05 eV using (4.2). The tabulated uncertainty is attributed to the scatter of measured VBM data and the resulting variability in the exact position of the linear fit. Utilizing these measured data, the band gap energy for intrinsic $In_{0.24}Ga_{0.76}As$ at 293 K (1.09 eV) calculated using the equation proposed by Paul et al. **[39]**, the unstrained Ge band gap (0.67 eV), and (4.3), ΔE_C was calculated to be 0.07±0.1 eV. It is worth noting that due to the lack of available experimental band gap data for ε-Ge taking into account both the level of strain and potential quantization effects, the unstrained Ge band gap was used in determining ΔE_C. Fig. 4.8 shows the schematic band alignment diagram for the 1.6% ε-Ge/$In_{0.24}Ga_{0.76}As$ sample. Following the procedure outlined above, the energy band alignments for the 0.75% ε-Ge/$In_{0.16}Ga_{0.84}As$ and 1.94% ε-Ge/$In_{0.29}Ga_{0.71}As$ heterojunctions were determined. Table 4.2 summarizes the measured and calculated XPS data for each ε-Ge/$In_xGa_{1-x}As$ TFET heterostructure.

Fig. 4.9 shows the experimental band offset parameters for the ε-Ge/$In_xGa_{1-x}As$ heterojunctions investigated in this study as well as ΔE_C and ΔE_V values for relaxed-

Ge/$In_{0.53}Ga_{0.47}As$ and Ge/GaAs heterostructures taken from **[14]** and **[18]**, respectively. As can be seen in Fig. 8, ΔE_V (blue, closed squares) exhibited a linear dependence on the in-plane biaxial tensile strain held by the epitaxial ε-Ge. Moreover, it is worth noting that while ΔE_C (red, closed circles) appears to have also been a linear function of the tensile-strain amount, the exact strain-ΔE_C relation cannot be determined without further experimental quantification of the ε-Ge band gap that includes both strain-induced band gap lowering as well as filtering of the quantization-induced energy level increase. Nevertheless, the monotonic relationship observed between ΔE_V and the in-plane tensile strain agrees well with previous work **[40, 41]** investigating the role of misfit-generated strain on band alignments for elemental (Si/Ge) **[40]** and compound ($In_xGa_{1-x}As$/GaAs) **[41]** semiconductor interfaces. Furthermore, the demonstration of a feasible method to modulate E_{beff} via graded buffer composition suggests the viability of TFET architectures based on ε-Ge/$In_xGa_{1-x}As$ materials.

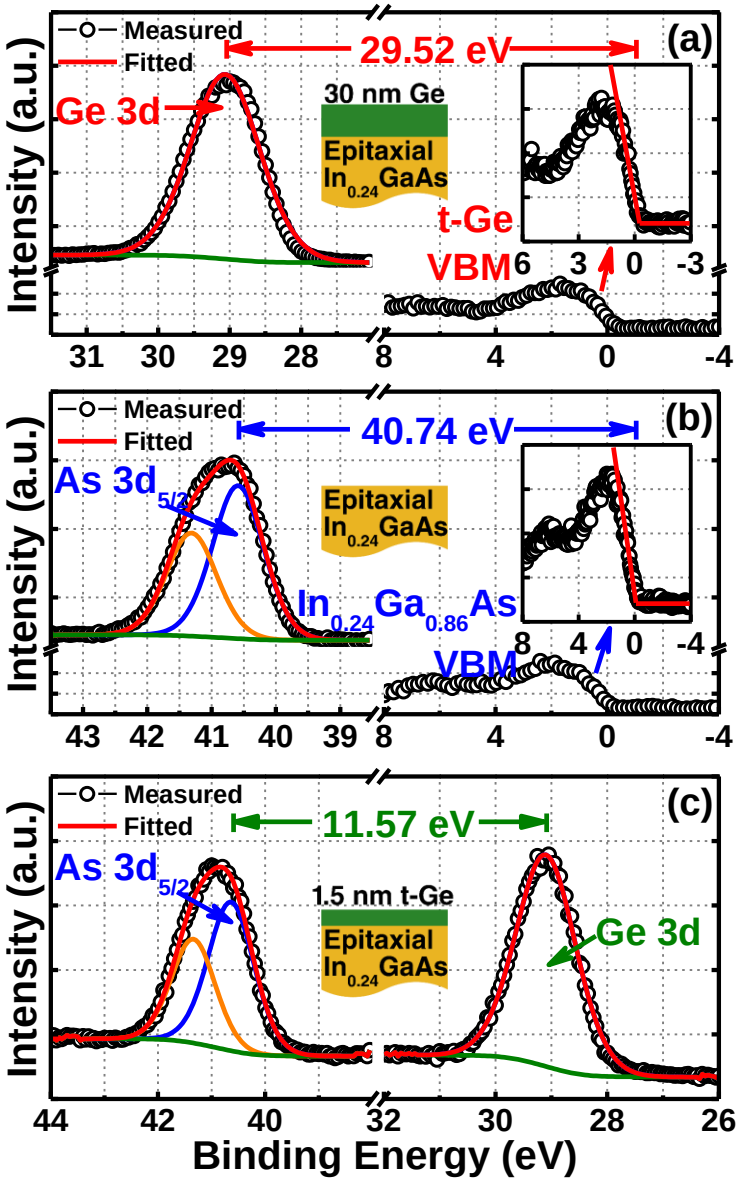

Figure 4.7 XPS spectra of (a) Ge 3d core level ($E_{Ge3d}^{\varepsilon-Ge}$) and valence band maximum, VBM ($E_{VBM}^{\varepsilon-Ge}$), from the 30 nm ε-Ge/$In_{0.24}Ga_{0.76}As$ sample, (b) As 3d core level ($E_{As3d}^{In_{0.24}Ga_{0.76}As}$) and $In_{0.24}Ga_{0.76}As$ VBM ($E_{VBM}^{In_{0.24}Ga_{0.76}As}$) from the $In_{0.24}Ga_{0.76}As$ virtual substrate, and (c), As 3d (E_{As3d}^{I}) and Ge 3d (E_{Ge3d}^{I}) core levels from the 1.5 nm ε-Ge/$In_{0.24}Ga_{0.76}As$ interface. © 2015 IEEE.

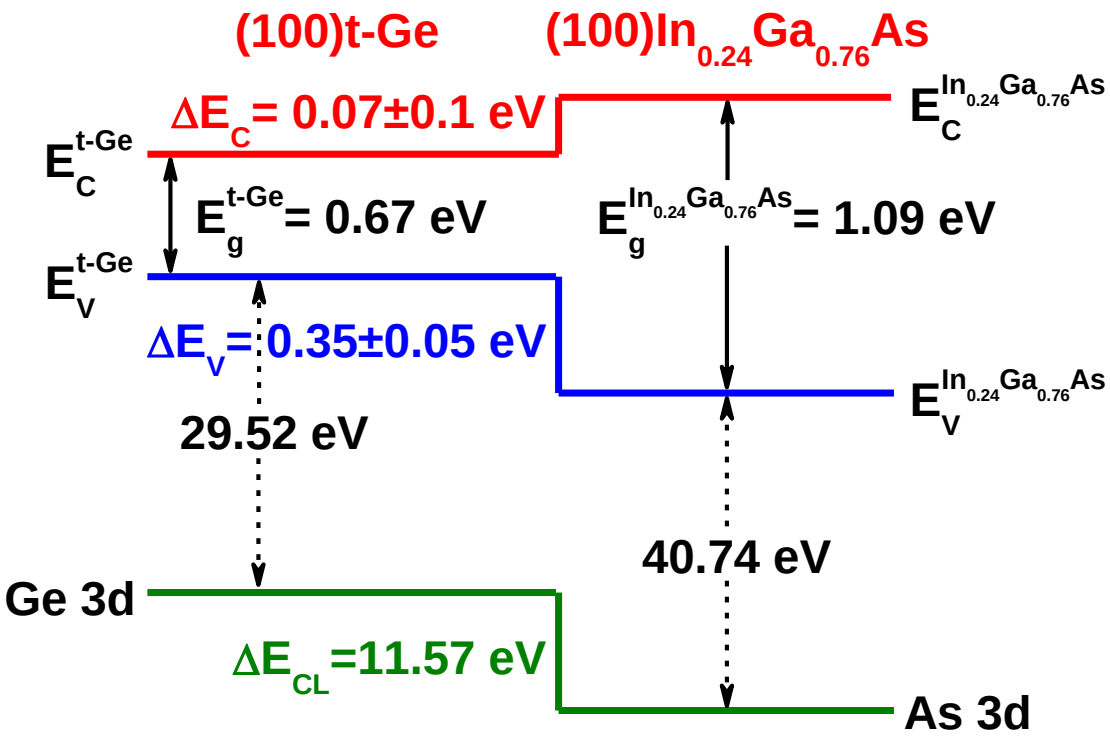

Figure 4.8 Schematic energy band alignment of the ε-Ge/$In_{0.24}Ga_{0.76}As$ heterointerface exhibiting a 0.35±0.05 eV valence band offset. © 2015 IEEE.

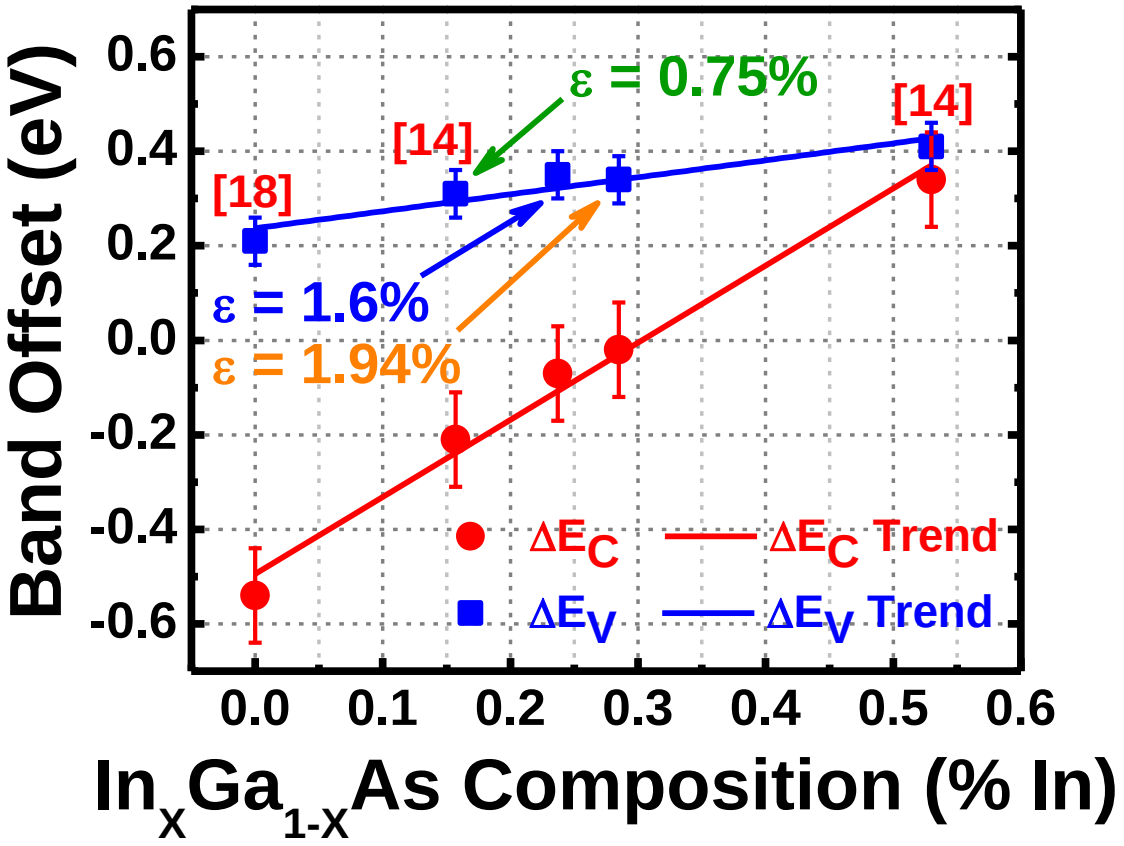

Figure 4.9 Valence band (ΔE_V) and conduction band (ΔE_C) offsets for the ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures studied in this work, as well as those investigated in **[14]**. Negative band offsets correspond to ($E_C^{\varepsilon\text{-}Ge}$) < ($E_C^{In_xGa_{1-x}As}$) and ($E_V^{\varepsilon\text{-}Ge}$) < ($E_V^{In_xGa_{1-x}As}$) for the conduction band and valence band, respectively. © 2015 IEEE.

Table 4.2 Summary of the measured and calculated XPS data of the ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures investigated in this study. © 2015 IEEE.

Heterostructure	Material Interface	Binding Energy Separation (eV)	Band Alignment Parameters	
			Measured ΔE_V (eV)	Calculated ΔE_C (eV)
ε-Ge/ $In_{0.16}Ga_{0.84}As$ [14]	15 nm ε-Ge on $In_{0.16}Ga_{0.84}As$	$E^{\varepsilon-Ge}_{Ge3d} - E^{\varepsilon-Ge}_{VBM}$ = 29.32	0.31±0.05	0.21±0.1†
	$In_{0.16}Ga_{0.84}As$	$E^{In_{0.16}Ga_{0.84}As}_{As3d_{5/2}} - E^{In_{0.16}Ga_{0.84}As}_{VBM}$ = 40.56		
	1.5 nm ε-Ge on $In_{0.16}Ga_{0.84}As$	$E^{\varepsilon-Ge}_{Ge3d} - E^{In_{0.16}Ga_{0.84}As}_{As3d_{5/2}}$ = -11.55		
ε-Ge/ $In_{0.24}Ga_{0.76}As$	30 nm ε-Ge on $In_{0.24}Ga_{0.76}As$	$E^{\varepsilon-Ge}_{Ge3d} - E^{\varepsilon-Ge}_{VBM}$ = 29.52	0.35±0.05	0.07±0.1
	$In_{0.24}Ga_{0.76}As$	$E^{In_{0.24}Ga_{0.76}As}_{As3d_{5/2}} - E^{In_{0.24}Ga_{0.76}As}_{VBM}$ = 40.74		
	1.5 nm ε-Ge on $In_{0.24}Ga_{0.76}As$	$E^{\varepsilon-Ge}_{Ge3d} - E^{In_{0.24}Ga_{0.76}As}_{As3d_{5/2}}$ = -11.57		
ε-Ge/ $In_{0.29}Ga_{0.71}As$	15 nm ε-Ge on $In_{0.29}Ga_{0.71}As$	$E^{\varepsilon-Ge}_{Ge3d} - E^{\varepsilon-Ge}_{VBM}$ = 29.37	0.34±0.05	0.02±0.1‡
	$In_{0.29}Ga_{0.71}As$	$E^{In_{0.29}Ga_{0.71}As}_{As3d_{5/2}} - E^{In_{0.29}Ga_{0.71}As}_{VBM}$ = 40.56		
	1.5 nm ε-Ge on $In_{0.29}Ga_{0.71}As$	$E^{\varepsilon-Ge}_{Ge3d} - E^{In_{0.29}Ga_{0.71}As}_{As3d_{5/2}}$ = -11.53		

† The previously reported ΔE_C value **[14]** has been recalculated using the unstrained Ge band gap (0.67 eV) for comparison with the data presented here.

‡ The calculated 293°K band gap of 1.03 eV for $In_{0.29}Ga_{0.71}As$ based on Ref. **[39]** was used for this calculation.

References

[1] Y. Zhu and M. K. Hudait, Low-Power Tunnel Field Effect Transistors Using Mixed As and Sb Based Heterostructures, *Nanotechnol. Rev.* **2**, 637-678 (2013).

[2] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, Fabrication, Characterization, and Physics of III-V Heterojunction Tunneling Field Effect Transistors (H-TFET) for Steep Sub-Threshold Swing, in *IEDM Tech. Dig.*, 33.6.1-33.6.4 (2011).

[3] D. K. Mohata, S. Mookerjea, A. Agrawal, Y. Li, T. Mayer, V. Narayanan, A. Liu, and S. Datta, Experimental Staggered-Source and N+ Pocket-Doped Channel III-V Tunnel Field-Effect Transistors and Their Scalabilities, *Appl. Phys. Exp.* **4**, 024105-1–024105-3 (2011).

[4] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, Role of InAs and GaAs Terminated Heterointerfaces at Source/Channel on the Mixed As-Sb Staggered Gap Tunnel Field Effect Transistor Structures Grown by Molecular Beam Epitaxy, *J. Appl. Phys.* **112**, 024306-1–024306-16 (2012).

[5] Y. Zhu, M. K. Hudait, D. K. Mohata, B. Rajamohanan, S. Datta, D. Lubyshev, J. M. Fastenau, and A. K. Liu, Structural, Morphological, and Defect Properties of Metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-Type Tunnel Field Effect Transistor Structure Grown by Molecular Beam Epitaxy, *J. Vac. Sci. Technol. B* **31**, 041203-1–041203-7 (2013).

[6] Z. Guangle, R. Li, T. Vasen, M. Q. S. Chae, Y. Lu, Q. Zhang, H. Zhu, J. M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, Novel Gate-Recessed Vertical InAs/GaSb TFETs with Record High I_{ON} of 180 μA/μm at V_{DS} = 0.5 V, in *IEEE Int. Electron Devices Meet.*, 32.6.1-32.6.4 (2012).

[7] Y. Zhu, N. Jain, D. H. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, Structural Properties and Band Offset Determination of p-Channel Mixed As/Sb Type-II Staggered Gap Tunnel-Field Effect Transistor Structure, *Appl. Phys. Lett.* **101**, 112106-1–112106-4 (2012).

[8] Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M.K. Hudait, Band Offset Determination of Mixed As/Sb Type-II Staggered Gap Heterostructure for n-Channel Tunnel Field Effect Transistor Applications, *J. Appl. Phys.* **113**, 024319-1–024319-5 (2013).

[9] D. K. Mohata, B. Rajamohanan, T. Mayer, M. K. Hudait, J. M. Fastenau, D. Lubyshev, A. K. Liu, and S. Datta, Barrier-Engineered Arsenide-Antimonide Heterojunction Tunnel FETs with Enhanced Drive Current, *IEEE Electron Device Lett.* **33**, 1568-1570 (2012).

[10] A. M. Ionescu and H. Riel, Tunnel Field-Effect Transistors as Energy-Efficient Electronic Switches, *Nature* **479**, 329-337 (2011).

[11] A. C. Seabaugh and Q. Zhang, Low-Voltage Tunnel Transistors for Beyond CMOS Logic, *Proc. IEEE* **98**, 2095-2110 (2010).

[12] Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, Defect Assistant Band Alignment Transition from Staggered to

Broken Gap in Mixed As/Sb Tunnel Field Effect Transistor Heterostructure, *J. Appl. Phys.* **112**, 094312-1–094312-9 (2012).

[13] J.-S. Liu, M. Clavel, and M. K. Hudait, Performance Evaluation of Novel Strain-Engineered Ge-InGaAs Heterojunction Tunnel Field-Effect Transistors, *IEEE Trans. Electron Devices* **62**, 3223-3228 (2015).

[14] Y. Zhu, D. Maurya, S. Priya, and M. K. Hudait, Tensile-Strained Nanoscale Ge/$In_{0.16}Ga_{0.84}As$ Heterostructure for Tunnel Field-Effect Transistor, *ACS Appl. Mater. Interfaces* **6**, 4947-4953 (2014).

[15] P. Guo, Y. Yang, Y. Cheng, G. Han, J. Pan, Ivana, Z. Zhang, H. Hu, Z. Xiang Shen, C. Kean Chia, and Y.-C. Yeo, Tunneling Field-Effect Transistor with Ge/$In_{0.53}Ga_{0.47}As$ Heterostructure as Tunneling Junction, *J. Appl. Phys.* **113**, 094502-1–094502-9 (2013).

[16] M. Clavel, P. Goley, N. Jain, Y. Zhu, and M. K. Hudait, Strain-Engineered Biaxial Tensile Epitaxial Germanium for High-Performance Ge/InGaAs Tunnel Field-Effect Transistors, *IEEE J. Electron Devices Soc.* **3**, 184-193 (2015).

[17] Y. Bai, K. E. Lee, C. Cheng, M. L. Lee, and E. A. Fitzgerald, Growth of Highly Tensile-Strained Ge on Relaxed $In_xGa_{1-x}As$ by Metal-Organic Chemical Vapor Deposition, *J. Appl. Phys.* **104**, 084518-1–084518-9 (2008).

[18] M. K. Hudait, Y. Zhu, N. Jain, and J. J. L. Hunter, Structural, Morphological, and Band Alignment Properties of GaAs/Ge/GaAs Heterostructures on (100), (110), and (111)A GaAs Substrates, *J. Vac. Sci. Technol. B* **31**, 011206-1–011206-14 (2013).

[19] M. K. Hudait, Y. Zhu, N. Jain, S. Vijayarghavan, A. Saha, T. Merritt, and G. A. Khodaparast, In Situ Grown Ge in an Arsenic-Free Environment for GaAs/Ge/GaAs

Heterostructures on Off-Oriented (100) GaAs Substrates Using Molecular Beam Epitaxy, *J. Vac. Sci. Technol. B* **30**, 051205-1–051205-11 (2012).

[20] M. K. Hudait and S.B. Krupanidhi, Atomic Force Microscopic Study of Surface Morphology in Si-doped epi-GaAs on Ge Substrates: Effect of Off-Orientation, *Mat. Res. Bul.* **35**, 909–919 (2000).

[21] M. K. Hudait and S. B. Krupanidhi, Self-Annihilation of Antiphase Boundaries in GaAs Epilayers on Ge Substrates Grown by Metal-Organic Vapor-Phase Epitaxy, *J. Appl. Phys.* **89**, 5972-5979 (2001).

[22] Y. Takano, M. Masuda, K. Kobayashi, K. Kuwahara, S. Fuke, and S. Shirakata, Epitaxial Growth of InGaAs on Misoriented GaAs(100) Substrate by Metal-Organic Vapor Phase Epitaxy, *J. Cryst. Growth* **236**, 31-36 (2002).

[23] S. M. Ting and E. A. Fitzgerald, Metal-Organic Chemical Vapor Deposition of Single Domain GaAs on Ge/Ge_xSi_{1-x}/Si and Ge Substrates, *J. Appl. Phys.* **87**, 2618-2628 (2000).

[24] W. Hu, B. Cheng, C. Xue, S. Su, Z. Liu, Y. Li, Q. Wang, L. Wang, J. Liu, J. Ding, G. Lin, and Z. Lin, Epitaxy of $In_{0.01}Ga_{0.99}As$ on Ge/Offcut Si (001) Virtual Substrate, *Thin Solid Films* **520**, 5361-5366 (2012).

[25] L. Yang, M. T. Bulsara, K. E. Lee, E. A. Fitzgerald, Compositionally-Graded InGaAs-InGaP Alloys for Metamorphic InP on GaAs, *J. Cryst. Growth* **324**, 103-109 (2011).

[26] K. E. Lee, E. A. Fitzgerald, High-Quality Compositionally Graded InGaAs Buffers, *J. Cryst. Growth* **312**, 250-257 (2010).

[27] F. Romanato, E. Napolitani, A. Carnera, A. V. Drigo, L. Lazzarini, G. Salviati, C. Ferrari, A. Bosacchi, and S. Franchi, Strain Relaxation in Graded Composition $In_xGa_{1-x}As$/GaAs Buffer Layers, *J. Appl. Phys.* **86**, 4748-4755 (1999).

[28] M. K. Hudait, Y. Lin, and S. A. Ringel, Strain Relaxation Properties of $InAs_yP_{1-y}$ Metamorphic Materials Grown on InP Substrates, *J. Appl. Phys.* **105**, 061643-1–061643-12 (2009).

[29] R. People and J. C. Bean, Calculation of Critical Layer Thickness Versus Lattice Mismatch for Ge_xSi_{1-x}/Si Strained-Layer Heterostructures, *Appl. Phys. Lett.* **47**, 322-324 (1985).

[30] J. J. Wortmann and R. A. Evans, Young's Modulus, Shear Modulus, and Poisson's Ratio in Silicon and Germanium, *J. Appl. Phys.* **36**, 153-156 (1965).

[31] O. Madelung, *Semiconductors: Intrinsic Properties of Group IV Elements and III-V, II-VI, and I-VII Compounds*, Vol. 22a, Springer: Berlin (1985).

[32] M. de Kersauson, M. Prost, A. Ghrib, M. El Kurdi, S. Sauvage, G. Beaudoin, L. Largeau, O. Mauguin, R. Jakomin, I. Sagnes, G. Ndong, M. Chaigneau, R. Ossikovski, and P. Boucaud, Effect of Increasing Thickness on Tensile-Strained Germanium Grown on InGaAs Buffer Layers, *J. Appl. Phys.* **113**, 183508-1—183508-7 (2013).

[33] M. V. Fischetti and S. E. Laux, Band Structure, Deformation Potentials, and Carrier Mobility in Strained Si, Ge, and SiGe Alloys, *J. Appl. Phys.* **80**, 2234-2252 (1996).

[34] K. H. Kao, A. S. Verhulst, M. Van de Put, W. G. Vandenberghe, B. Soree, W. Magnus, and K. De Meyer, Tensile Strained Ge Tunnel Field-Effect Transistors: k·p

Material Modeling and Numerical Device Simulation, *J. Appl. Phys.* **115**, 044505-1–044505-8 (2014).

[35] M. Natali, F. Romanato, E. Napolitani, D. De Salvador, and A. V. Drigo, Lattice Curvature Generation in Graded $In_xGa_{1-x}As$/GaAs Buffer Layers, *Phys. Rev. B* **62**, 11054-11062 (2000).

[36] A. M. Andrews, A. E. Romanov, J. S. Speck, M. Bobeth, and W. Pompe, Development of Cross-Hatch Morphology During Growth of Lattice Mismatched Layers, *Appl. Phys. Lett.* **77**, 3740-3742 (2000).

[37] A. M. Andrews, R. LeSar, M. A. Kerner, J. S. Speck, A. E. Romanov, A. L. Kolesnikova, M. Bobeth, and W. Pompe, Modeling Cross-Hatch Surface Morphology in Growing Mismatched Layers, *J. Appl. Phys.* **91**, 1933-1943 (2002).

[38] E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Eowalczyk, Precise Determination of the Valence-Band Edge in X-ray Photoemission Spectra: Application to Measurement of Semiconductor Interface Potentials, *Phys. Rev. Lett.* **44**, 1620-1623 (1980).

[39] S. Paul, J. B. Roy, and P. K. Basu, Empirical Expressions for the Alloy Composition and Temperature Dependence of the Band Gap and Intrinsic Carrier Density in $Ga_xIn_{1-x}As$, *J. Appl. Phys.* **69**, 827-829 (1991).

[40] E. T. Yu, E. T. Croke, and T. C. McGill, Measurement of the Valence-Band Offset in Strained Si/Ge (100) Heterojunctions by X-ray Photoelectron Spectroscopy, *Appl. Phys. Lett.* **56**, 569-571 (1990).

[41] S. Niki, C. L. Lin, W. S. C. Chang, and H. H. Wieder, Band-Edge Discontinuities of Strained-Layer $In_xGa_{1-x}As$/GaAs Heterojunctions and Quantum Wells, *Appl. Phys. Lett.* **55**, 1339-1341 (1989).

Chapter 5 – Heteroepitaxial Tensile-Strained Ge/$In_xGa_{1-x}As$ Integration on Silicon for Tunable Nanoscale Photonics

Chapters 1 and ***2*** highlighted the necessity of novel, Si-compatible photonic material systems, noting that interconnect bottlenecks for both inter-chip and intra-chip communication are projected to be major impediments to energy-efficient performance scaling **[1]**. As previously discussed, it will become increasingly challenging to transmit signals electrically *via* copper interconnects while maintaining low power consumption, low delay, and a high signal-to-noise ratio **[2]**. Although the monolithic integration of Si-based optoelectronics is an enticing approach to help meet the aforementioned bandwidth requirements, the indirect bandgap of Si limits the realization of Si-based photonic devices **[3]**. Thus, the hybrid integration of germanium (Ge) and III-V materials-based optoelectronic devices with traditional Si CMOS technology would be an innovative approach to leveraging the superior transport properties and large modulation bandwidth of Ge and III-V compound semiconductor material systems as well as the economy of scale of Si **[4-16]**.

Whereas $Ge_{1-x}Sn_x$ has gained wide-spread research interest **[17-19]** due to the modification of the $Ge_{1-x}Sn_x$ bandgap by tin (Sn) incorporation, the poor thermal stability of $Ge_{1-x}Sn_x$ results in Sn segregation **[19]** and restricts process and growth temperatures, as elaborated on in ***Chapter 2***. As an alternative to these approaches, this chapter will demonstrate the use of variable surface-terminated lattice constant buffering of III-V compound semiconductor metamorphic layers on Si. Subsequent strain layer epitaxy of Ge thin films on these tunable strain templates will validate the feasibility of band structure engineering *via* strain engineering using a material system that is robust with

respect to process flow and growth requirements. As discussed in ***Chapter 2***, band structure engineering can be used to improve the direct bandgap recombination probability in the tensile strained Ge (ε-Ge) films, enhancing infrared emission and demonstrating their applicability to the monolithic integration of on-Si photonics. Careful control over the modular tensile strain in the Ge epitaxial layers during growth, in tandem with the strain analysis, defect examination, morphological, and band alignment properties of these strained Ge material systems, will therefore provide a path to achieve group-IV-based lasers on Si.

5.1. MBE Growth of ε-Ge/$In_xGa_{1-x}As$ Heterostructures on Si

All samples studied in this chapter were grown on off-cut (100) Si substrates using an *in-situ* growth process utilizing separate solid-source molecular beam epitaxy (MBE) growth chambers for the Ge and III-V materials, connected *via* an ultra-high vacuum transfer chamber. The effect of substrate off-cut on the suppression of anti-phase domain boundary and stacking fault formation at the GaAs/Si interface is well-supported in the literature **[20, 21]** and was utilized to achieve device quality active layers in this work. GaAs and linearly graded $In_xGa_{1-x}As$ buffers were grown on Si to mitigate the defects and dislocations due to the significant lattice and thermal mismatch between Ge and Si. An $In_{0.11}Ga_{0.89}As$ or $In_{0.17}Ga_{0.83}As$ constant composition virtual substrate was grown at 550^{o}C prior to the Ge epilayer growth, followed by a slow cooling down to 150^{o}C and then transfer under ultra-high vacuum to the Ge chamber for strained-layer Ge epitaxy at a growth temperature of 400^{o}C and growth rate of ~0.1Å/s. During the substrate oxide desorption and periodically throughout each layer growth, reflection high-energy electron diffraction (RHEED) was used to monitor the surface reconstruction for growth-induced

defect patterns. The ε-Ge on Si samples were characterized *ex-situ* by high-resolution X-ray diffraction, atomic force microscopy, and low-temperature magneto-transport measurements. Select samples were then transferred to the III-V chamber for the upper $In_xGa_{1-x}As$ layer growth. Prior to the $In_xGa_{1-x}As$ cap layer growth, samples were held at 400°C for 30 min to thermally desorb residual Ge surface oxides formed during *ex-situ* materials characterization. RHEED was used to monitor the surface reconstruction of the ε-Ge layer during the oxide desorption as well as the upper $In_xGa_{1-x}As$ layer growth. The thorough desorption of native oxides from the ε-Ge epilayer is crucial in achieving an atomically abrupt, oxide-free heterointerface, thereby reducing the likelihood of generating electrically or optically active interfacial defect states **[22]**.

To determine the crystalline quality and relaxation state of the tensile-strained epitaxial Ge layers grown on Si, high-resolution triple axis X-ray rocking curves and reciprocal space maps were recorded from each sample using a PANalytical X-pert Pro system equipped with both PIXel and proportional detectors and a monochromatic Cu Kα (λ = 1.540598 Å) X-ray source. Select samples underwent further X-ray diffraction characterization following removal of the ε-Ge epilayer using an $NH_4OH:H_2O_2:H_2O$ (2:1:200 volume ratio) wet etch. Raman spectra acquired using a JY Horiba LabRam HR800 system equipped with a 514.32 nm Ar laser excitation source were used to independently confirm the strain-state of the ε-Ge thin films. To analyze the elemental composition of the structure, energy dispersive X-ray spectroscopy (EDS) was performed using a JEOL 2100 transmission electron microscope (TEM) operating in scanning TEM mode. The bandgap as a function of strain within each ε-Ge epilayer was characterized

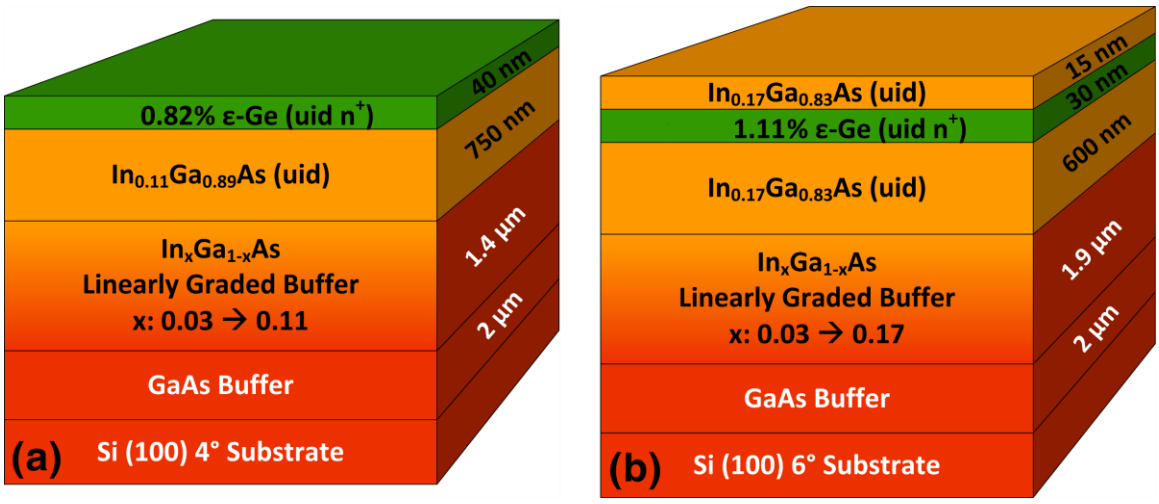

Figure 5.1 Cross-sectional schematic of (a) 0.82% ε-Ge/$In_{0.11}Ga_{0.89}As$ and (b) 1.11% ε-Ge/$In_{0.17}Ga_{0.83}As$ structures heterogeneously integrated onto Si. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

via micro-photoluminescence (µ-PL) spectroscopy using an 800 nm laser source and a thermoelectric cooled InGaAs detector for optical pumping and detection, respectively.

5.2. Strain Relaxation Properties of ε-Ge/$In_xGa_{1-x}As$ Structures Heterogeneously Integrated on Si

Fig. 5.1 shows the schematic diagrams of the ε-Ge/$In_xGa_{1-x}As$ heterostructures that were heterogeneously grown on off-cut (100) Si substrates and studied in this chapter. For the 1.11% ε-Ge sample, a 15 nm constant composition $In_{0.17}Ga_{0.83}As$ capping layer was grown in order to study the materials and optical properties of $In_{0.17}Ga_{0.83}As$ cladded ε-Ge optical cavities. The strain relaxation properties of these structures were investigated using HR-XRD. Fig. 5.2 shows the high-resolution triple axis symmetric (004) X-ray rocking curves from the 30–40 nm ε-Ge epilayers grown on (i) 750 nm $In_{0.11}Ga_{0.89}As$/1.4 µm graded $In_xGa_{1-x}As$/2 µm GaAs (0.82% tensile strain, green) and (ii)

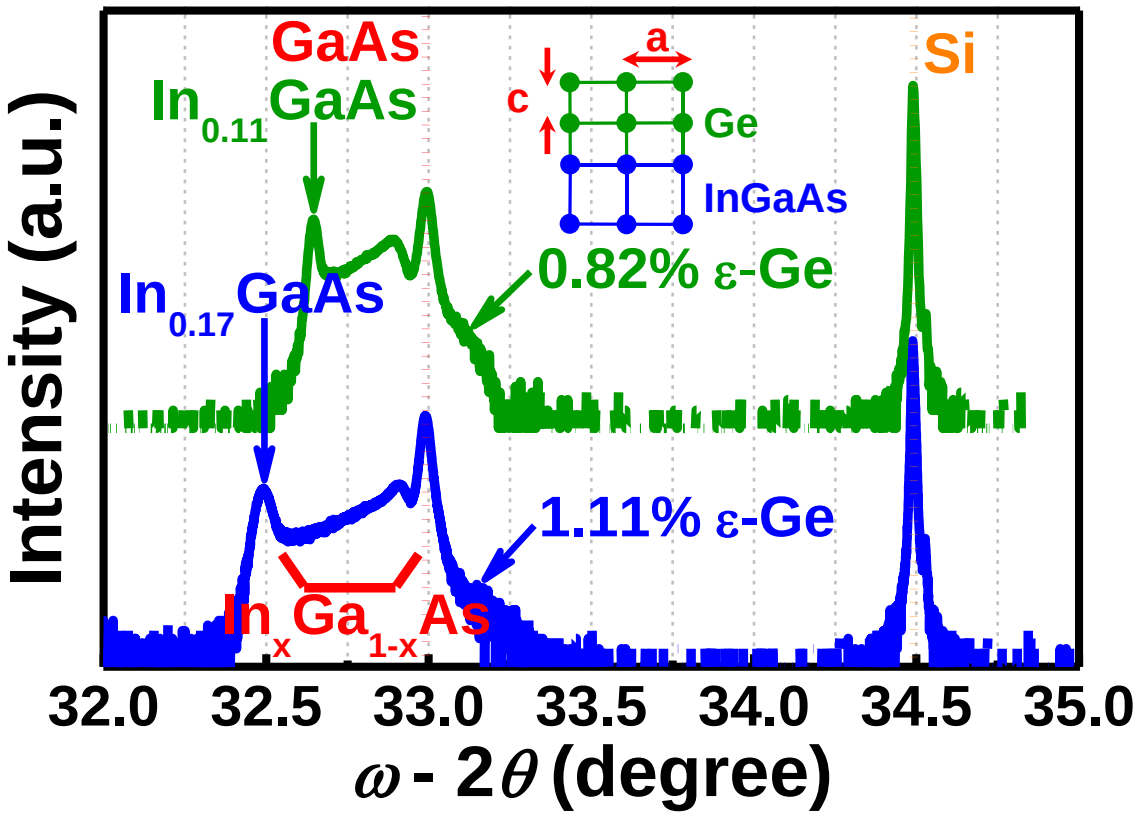

Figure 5.2. X-ray rocking curves from the 0.82% (green) and 1.11% (blue) ε-Ge on Si structures showing movement of the Ge Bragg angle with increasing tensile strain. Inset demonstrates the effect of heteroepitaxial mismatch on the in-plane lattice constant of the top-lying epilayer. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

metamorphic buffers on Si, respectively. Additionally, each diffraction peak in Fig. 5.2 is labeled with its corresponding epilayer. Likewise, Fig. 5.3 shows the symmetric (004) and asymmetric (115) RSMs of the ε-Ge/$In_{0.11}Ga_{0.89}As$ on Si structure, while Fig. 5.4 similarly shows the (004) and (115) RSMs taken from the ε-Ge/$In_{0.17}Ga_{0.83}As$ on Si structure. Also shown in Figs. 5.3 and 5.4 are the (004) and (115) RSMs recorded for each respective metamorphic buffer structure after removal of the ε-Ge ($In_{0.17}Ga_{0.83}As$/ε-Ge) topmost epilayer(s) using dilute $NH_4OH:H_2O_2:H_2O$ (2:1:200 volume ratio). For all

RSMs, each layer has been labeled to its corresponding reciprocal lattice point (RLP) for clarity. One can find from the symmetric (004) RCs in Fig. 5.2 and RSMs in Figs. 5.3 (a) and 5.4 (a) that the Ge RLP exhibits a larger Bragg angle as compared to the GaAs buffer RLP, indicating a smaller out of-plane lattice constant and thus the presence of tensile strain in the Ge epilayer. As shown in the inset of Fig. 5.2, due to the larger lattice constant of the $In_xGa_{1-x}As$ (x = 0.11, 0.17) strain template, the in-plane lattice constant of the heteroepitaxial Ge is stretched to accommodate the in-plane lattice constant of the $In_xGa_{1-x}As$ layer, resulting in a biaxial tensile-strained, pseudomorphic Ge epilayer with an expanded in-plane lattice constant (labeled as *a*) and reduced out-of-plane lattice constant (labeled as *c*). One can find from Figs. 5.2–5.4 that the diffraction peak and RLP of ε-Ge is partially suppressed by the intensity of the GaAs substrate as a result of minor Bragg angle modulation due to the moderate strain levels studied in this work. In order to mitigate error in the experimental strain relaxation analysis resulting from the partial superposition of the ε-Ge and GaAs diffraction peaks, only the centroid of the ε-Ge (004) RLP taken from the symmetric (004) RSM was used for quantitative analysis of the out-of-plane lattice spacing. Moreover, so as to more clearly distinguish the superimposed ε-Ge and GaAs peaks, Fig. 5.5 shows the symmetric (004) RSM of the ε-Ge/$In_{0.11}Ga_{0.89}As$ structure plotted along ω-2θ (a) prior to and (b) after removal of the ε-Ge layer. As seen in the inset of Fig. 5.5 (a), magnification of the Bragg angles surrounding the GaAs layer revealed the distinct outline of the ε-Ge peak, thus enabling a more accurate determination of the ε-Ge ω-2θ centroid prior to conversion to reciprocal lattice units. Furthermore, Figs. 5.3 (b) and 5.3 (d) (Figs. 5.4 (b) and 5.4 (d)) show the (004) and (115) RSMs for the $In_{0.11}Ga_{0.89}As$/GaAs ($In_{0.17}Ga_{0.83}As$/GaAs) metamorphic buffers following

wet etching of the terminating ε-Ge ($In_{0.17}Ga_{0.83}As$/ε-Ge) epilayer(s). One can find by comparing Figs. 5.3 (b) and 5.3 (d) (Figs. 5.4 (b) and 5.4 (d)) to Figs. 5.3 (a) and 5.3 (c) (Figs. 5.4 (a) and 5.4 (c)) that the ε-Ge RLP indeed contributes significantly to the broadening and intensity of the region in reciprocal space in proximity to the GaAs virtual substrate peak. The ability to clearly differentiate between the ε-Ge and GaAs diffraction peaks thus provides ancillary support for the strain-dependent shift in the ε-Ge RLP observed in Figs. 5.3 and 5.4. Further movement of the ε-Ge RLP can be achieved by providing increased tensile strain to the Ge layer through growth on higher indium (In) content $In_xGa_{1-x}As$ virtual substrates, thereby increasing the accuracy of the measured strain data.

As shown in Figs. 5.3 (c) and 5.4 (c) by the vertical alignment of the $In_xGa_{1-x}As$ and ε-Ge RLPs (orange dotted lines), the in-plane lattice constant of ε-Ge was found to be closely matched with the in-plane lattice constant of the $In_{0.11}Ga_{0.89}As$ and $In_{0.17}Ga_{0.83}As$ constant composition layers, signifying that the tensile strain transferred to the Ge was successfully modulated by varying the underlying $In_xGa_{1-x}As$ In alloy composition. The detailed analyses of the relaxation and strain states of the epitaxial Ge and $In_xGa_{1-x}As$ layers were evaluated by measuring the in-plane and out-of-plane lattice constants, *a* and *c*, for both Ge and $In_xGa_{1-x}As$ using the recorded symmetric (004) and asymmetric (115) RSM data. The relaxed lattice constant (a_r) of each layer was calculated using *a*, *c* and Poisson's ratio, *v*, for each material, noting that a relaxed Ge lattice parameter of 5.658 Å was assumed **[23]**. Table 5.1 summarizes the in-plane, out-of-plane, and relaxed lattice constants of the $In_xGa_{1-x}As$ (x = 0.11, 0.17) and ε-Ge layers as well as the amount of strain, relaxation, and epitaxial tilt determined *via* these measurements in conjunction

with the methods introduced in ***Chapter 3.3.1***. Using the relaxed lattice constant of $In_xGa_{1-x}As$ and Vegard's law, the In alloy composition of each $In_xGa_{1-x}As$ virtual substrate was determined to be 11.4% and 16.6%, which was consistent with the design criteria. The GaAs and $In_xGa_{1-x}As$ metamorphic buffers on Si were found to be ~90% and 82-87% relaxed, respectively. Additionally, the uncertainty in the experimental strain values for each ε-Ge/$In_xGa_{1-x}As$ heterostructure was derived using the measured effect of epitaxial tilt on the calculated in-plane and out-of-plane lattice parameters and thereby the strain held by the Ge epilayer. For the measured results presented in Table 5.1, the data used in the strain relaxation analysis were collected from RSMs in which the tilt of the $In_xGa_{1-x}As$ and ε-Ge layers was minimized with respect to the Si substrate. The resulting uncertainties were found to be ±0.06% and ±0.03% for the 0.82% and 1.11% ε-Ge, respectively. Consequently, the experimentally demonstrated tensile strain modulation due to increasing In alloy composition in $In_xGa_{1-x}As$ strain templates is expected to modify the Ge bandgap, an essential step towards achieving tunable wavelength Ge-based photonic devices, as will be discussed in the micro-photoluminescence (μ-PL) analysis below.

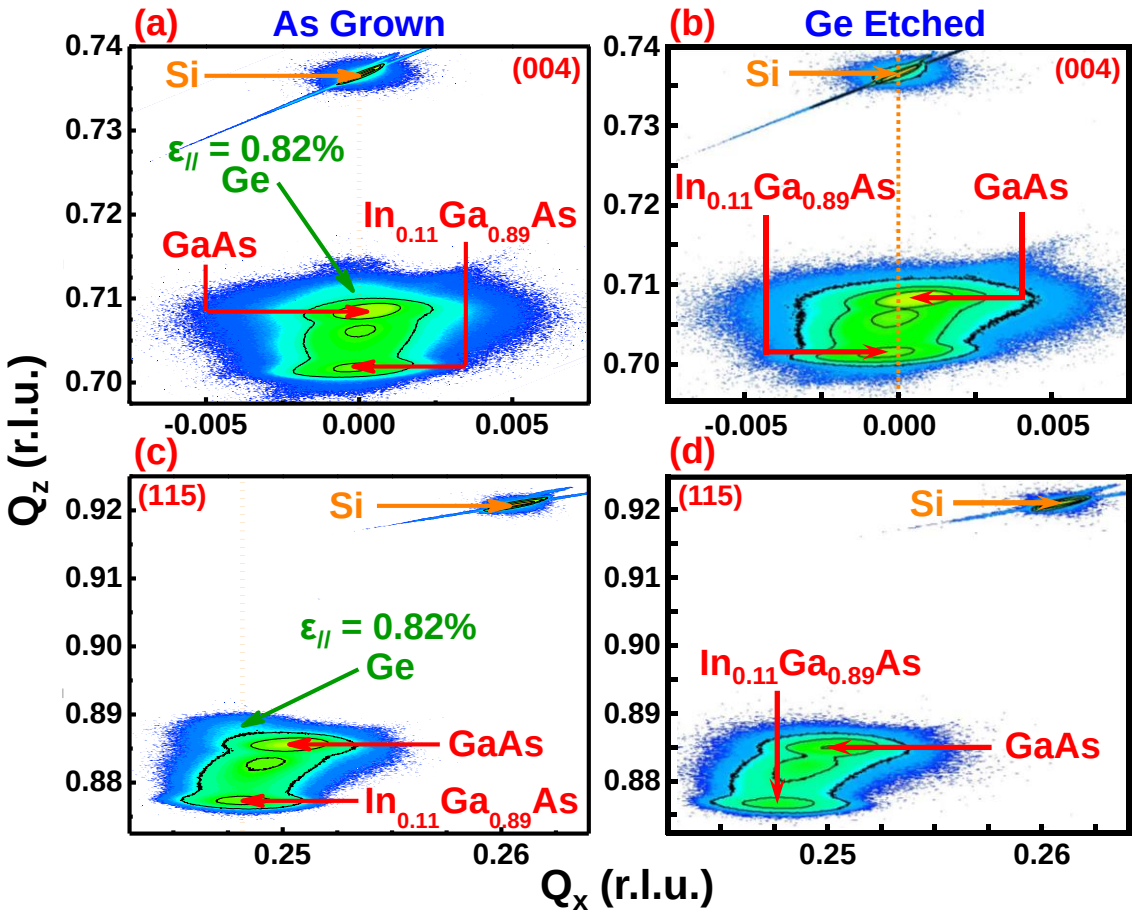

Figure 5.3 Symmetric (004) RSMs of the 0.82% ε-Ge/$In_{0.11}Ga_{0.89}As$ heterostructure (a) as-grown and (b) after wet etch removal of the ε-Ge epilayer, highlighting the position of the ε-Ge RLP (a) with respect to the background intensity of the $In_{0.11}Ga_{0.89}As$/GaAs metamorphic buffer (b). (c) and (d) show the same for the asymmetric (115) RSMs. Moreover, the Si RLP is clearly visible. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

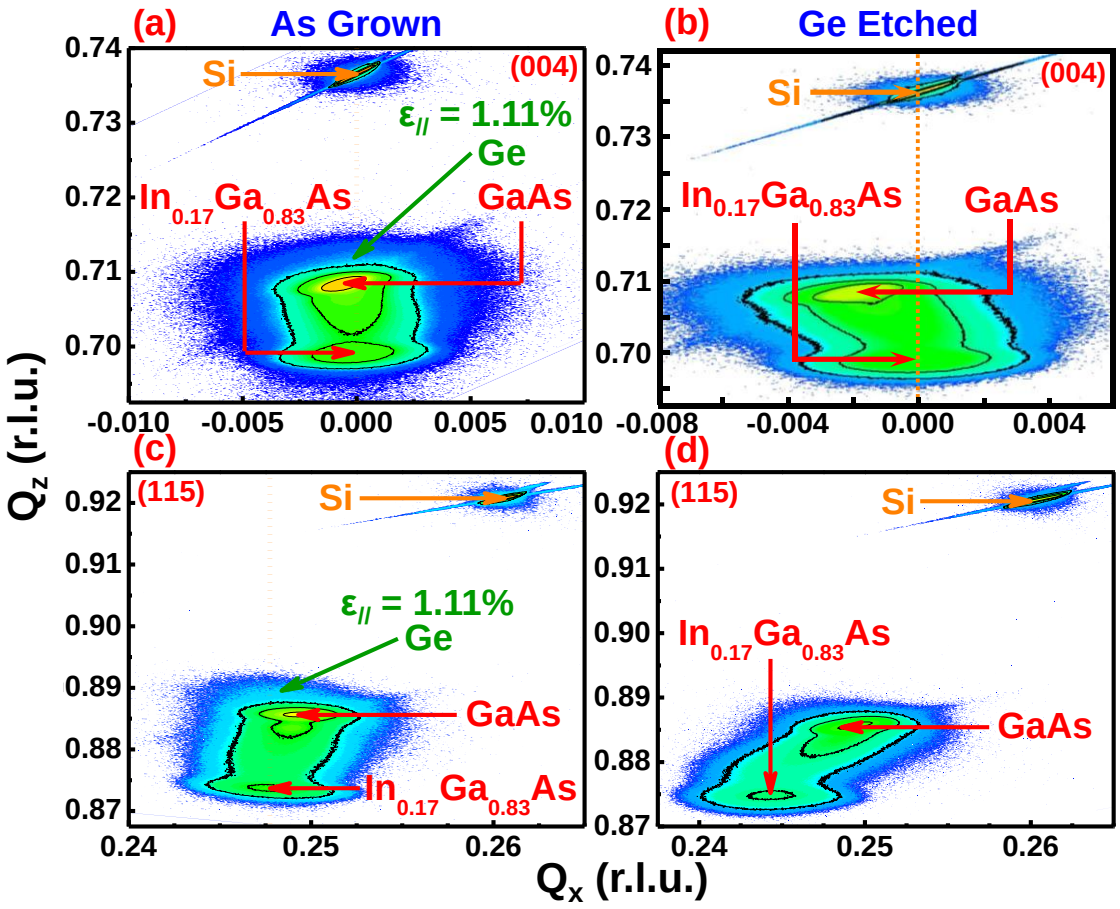

Figure 5.4 Symmetric (004) RSMs of the 1.11% ε-Ge/$In_{0.17}Ga_{0.83}As$ heterostructure (a) following the $In_{0.17}Ga_{0.83}As$ cap layer growth and (b) after removal of the top $In_{0.17}Ga_{0.83}As$ and ε-Ge epilayers by wet etching, emphasizing the position of the ε-Ge RLP (a) with respect to the background intensity of the $In_{0.17}Ga_{0.83}As$/GaAs metamorphic buffer (b). (c) and (d) show a similar comparison for the asymmetric (115) RSMs taken from the same $In_{0.17}Ga_{0.83}As$/ε-Ge/$In_{0.17}Ga_{0.83}As$ double heterostructure. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

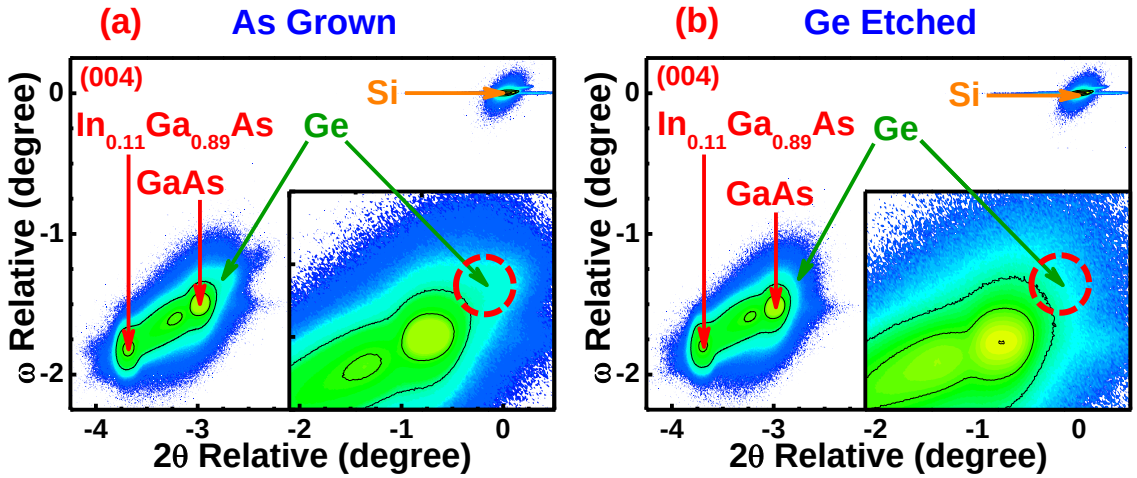

Figure 5.5 Symmetric (004) RSMs of the ε-Ge/$In_{0.11}Ga_{0.89}As$ heterostructure (a) as-grown and (b) after etching the ε-Ge epilayer in $NH_4OH:H_2O_2:H_2O$, revealing the position of the ε-Ge *ω-2θ* centroid (a) with respect to the background intensity of the $In_{0.11}Ga_{0.89}As$/GaAs metamorphic buffer (b). Insets show magnification of the region in proximity to the GaAs *ω-2θ* centroid, demonstrating a clear contribution from the ε-Ge diffraction peak to the detected diffraction signal. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

Material	Lattice Constant (Å)			In Composition (%)	Relaxation (%)	Epitaxial Tilt (arcsec)	Tensile Strain, Ge (%)
	Out-of-Plane (*a*)	In-Plane (*c*)	Relaxed (a_r)				
$In_{0.11}Ga_{0.89}As$	5.7073	5.6912	5.6996	11.4	82	-116	0.82±0.06
0.82% ε-Ge	5.6348	5.7045	5.658		-	-118	
$In_{0.17}Ga_{0.83}As$	5.7286	5.7106	5.7204	16.6	87	127	1.11±0.03
1.11% ε-Ge	5.6272	5.7208	5.658		-	117	

Table 5.1: Summary of the strain relaxation properties of the ε-Ge/$In_xGa_{1-x}As$ structures heterogeneously integrated onto Si. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

5.3. Raman Spectroscopic Strain Analysis of Ge Thin Films on III-V Buffers on Si

Fig. 6 (a) shows the shift in Raman frequency ($\Delta\omega$) as a function of strain in the ε-Ge layers studied in this chapter. As shown in Fig. 6 (a), the tensile strain shifts the position of the longitudinal optical (LO) phonon peak away from the bulk Ge LO peak, where the magnitude and sign of the wavenumber shift (positive/compressive or negative/tensile) are representative of the type of strain present in the system. The ε-Ge layers grown on Si using a GaAs/$In_xGa_{1-x}As$ graded buffer exhibit wavenumber shifts of -3.45 cm^{-1} and -4.96 cm^{-1} for the ε-Ge/$In_{0.11}Ga_{0.89}As$ and ε-Ge/$In_{0.17}Ga_{0.83}As$ structures, respectively, corresponding to 0.83% (green) and 1.19% (blue) tensile strain. Also shown in Fig. 6 (a) is the Raman shift of quasi-lattice matched Ge/AlAs on GaAs (grey) and on Si (orange). It is worth noting that due to the thermal and lattice mismatch present between each epilayer and the growth substrate, some level of residual strain exists in the layers of interest. One can see from Fig. 6 (a) that for epitaxial Ge grown quasi-lattice matched to AlAs/GaAs buffers grown on Si, the thermal mismatch between epilayer and substrate results in a tensile strained Ge thin film without the presence of an $In_xGa_{1-x}As$ stressor. This thermally-induced tensile stress must be accounted for when analyzing the Raman shift of ε-Ge heterogeneously integrated onto Si utilizing III-V buffer architectures. While it is well documented that the Ge-Ge phonon vibration mode is approximately 300 cm^{-1} and that a shift in phonon vibration mode with respect to this number is a result of crystallographic strain, an exact relationship between strain and wavenumber shift is only approximate. Recent work **[24]** has utilized the relation $\Delta\omega = -b\varepsilon_{//}$ to analyze Raman shift as a function of strain in tensile Ge thin films, where $\Delta\omega$ is the wavenumber shift (in cm^{-}

[1]) and *b* is a material parameter dependent on the material's phononic and elastic constants. Using the reported literature value of 415 cm^{-1} for b_{Ge} **[25]**, the wavenumber shift versus In alloy composition as well as strain versus In alloy composition relationships are shown in Fig. 6 (b). One can find from Fig. 6 (b) that tensile strain (green) determined from the Raman shift (blue) corresponds accurately to the theoretical misfit (red) for the In alloy compositions studied, thereby independently confirming the pseudomorphic nature of the strained Ge epitaxy. Moreover, the strain analysis demonstrated utilizing Raman spectroscopy was found to be in good agreement with the strain relaxation properties of the ε-Ge/$In_xGa_{1-s}As$ heterostructures on Si as determined *via* X-ray diffraction analysis, thereby highlighting the suitability of Raman spectroscopy for studying ε-Ge thin films with moderate strain levels.

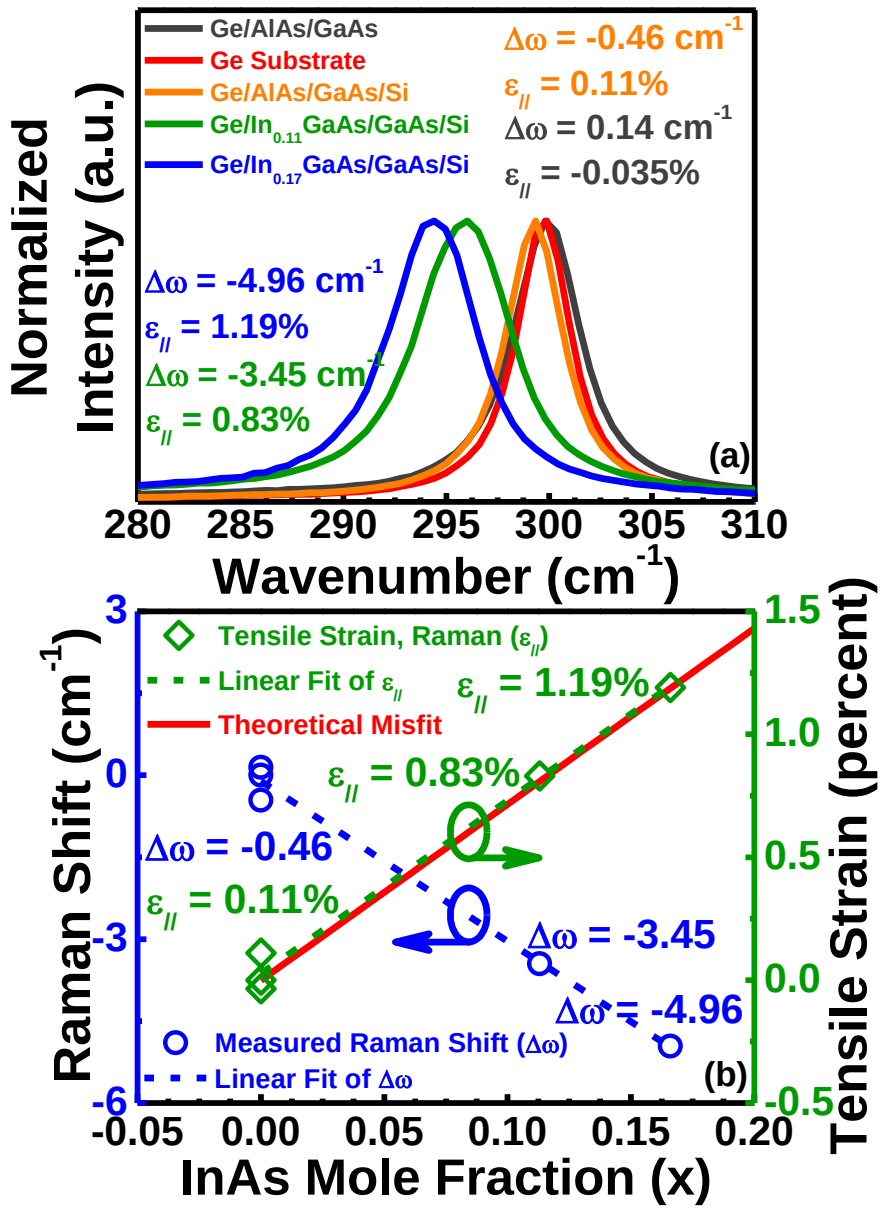

Figure 5.6 (a) Raman wavenumber shift due to strain-induced modulation of the Ge LO phonon modes. (b) Comparison of Raman-determined strain with wavenumber shift and the theoretical $Ge/In_xGa_{1-x}As$ misfit. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

5.4. Structural, Defect and Dislocation Analysis of ε-Ge/$In_xGa_{1-x}As$ Metamorphic Systems on Si

Additional investigation into the material quality and nature of the ε- Ge/$In_xGa_{1-x}As$ (x = 0.11, 0.17) heterointerface was performed by high-resolution cross-sectional transmission electron microscopy (TEM) analysis. Figs. 5.7 and 5.8 show the bright-field cross-sectional TEM micrographs of the ε-Ge grown on $In_{0.11}Ga_{0.89}As/In_xGa_{1-x}As$/GaAs/Si and $In_{0.17}Ga_{0.83}As/In_xGa_{1-x}As$/GaAs/Si, respectively. Cross-sectional TEM measurements were performed on various locations of the TEM specimen and the representative results are shown in Figs. 5.7 and 5.8. Moreover, all layers are labeled in each figure. The GaAs and linearly graded $In_xGa_{1-x}As$ buffers on Si were found to effectively mitigate the lattice mismatch induced defects and dislocations between the ε-Ge/$In_xGa_{1-x}As$ (x = 0.11, 0.17) layers of interest and the Si substrate. One can find from Figs. 5.7 (a) and 5.8 (a) that the majority of dislocations were confined within the linearly graded $In_xGa_{1-x}As$ buffer. Moreover, the residual strain within the top $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) layer was minimized due to the nominal accommodation of mismatch induced epitaxial strain *via* misfit dislocation formation and subsequent dislocation glide, corroborating the previously discussed strain relaxation properties for each $In_xGa_{1-x}As$ virtual substrate. Similarly, the apparent absence of threading dislocation propagation into the ε-Ge active region suggests a device-quality active region, further reinforcing the structural data found *via* reciprocal space mapping. Hence, the composite GaAs and linearly graded $In_xGa_{1-x}As$ buffer provided a high-quality virtual substrate for the tunable tensile-strained Ge heterogeneously integrated onto Si. Furthermore, high resolution

lattice indexing shown in Figs. 5.7 (c) and 5.8 (b) revealed the lattice line extending uninterrupted between the ε-Ge and $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) epilayers, indicating that the Ge in-plane lattice constant was internally registered with the in-plane lattice constant of the $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) strain template and demonstrating pseudomorphic tensile-stained Ge epitaxy in good agreement with the X-ray and Raman analysis presented earlier. Figs. 5.7 (d)-(f) and 5.8 (c)-(e) show Fast Fourier Transform (FFT) patterns representative of the regions denoted by arrows. The indexing of these FFT patterns indicates that the electron beam was parallel to the [011] orientation. Moreover, the FFT patterns obtained from the ε-Ge layer, ε-Ge/$In_xGa_{1-x}As$ heterointerface, and the $In_xGa_{1-x}As$ layer are identical and absent of diffraction peak splitting (satellite peaks), indicating the contribution of a singular lattice parameter to the diffraction peak reciprocal spacing in the FFT field-of-view and further validating the high quality, coherent epitaxial growth at the strained Ge/$In_xGa_{1-x}As$ interface. Accordingly, the cross-sectional TEM analysis suggests optical-quality film structures with atomically smooth interfaces, which is crucial to minimizing cavity losses in Ge-based photonic devices.

To further evaluate the atomic species profile across each heterointerface, energy dispersive X-ray spectroscopy (EDS) was utilized to perform an elemental mapping of the ε-Ge/$In_{0.11}Ga_{0.89}As$ heterostructure. Fig. 5.7 (b) shows the elemental mapping of the ε-Ge/$In_{0.11}Ga_{0.89}As$ structure where the Ge layer (green) was found to be uniformly distributed and the In (blue) exhibits a variable composition, as expected in the linearly graded $In_xGa_{1-x}As$ buffer layer, in addition to the composition profile of Si (red). The EDS analysis exhibits a uniform and sharp heterointerface between the ε-Ge and the

$In_{0.11}Ga_{0.89}As$ layer, with no apparent interdiffusion across any of the structure's heterointerfaces despite the increased thermal budget as a result of experiencing extended growth temperature conditions during the strained layer epitaxy of Ge. Therefore, the atomic scale imaging and microstructural analysis feedback loop is necessary for the large-scale heterointegration of tunable tensile-strained Ge on Si.

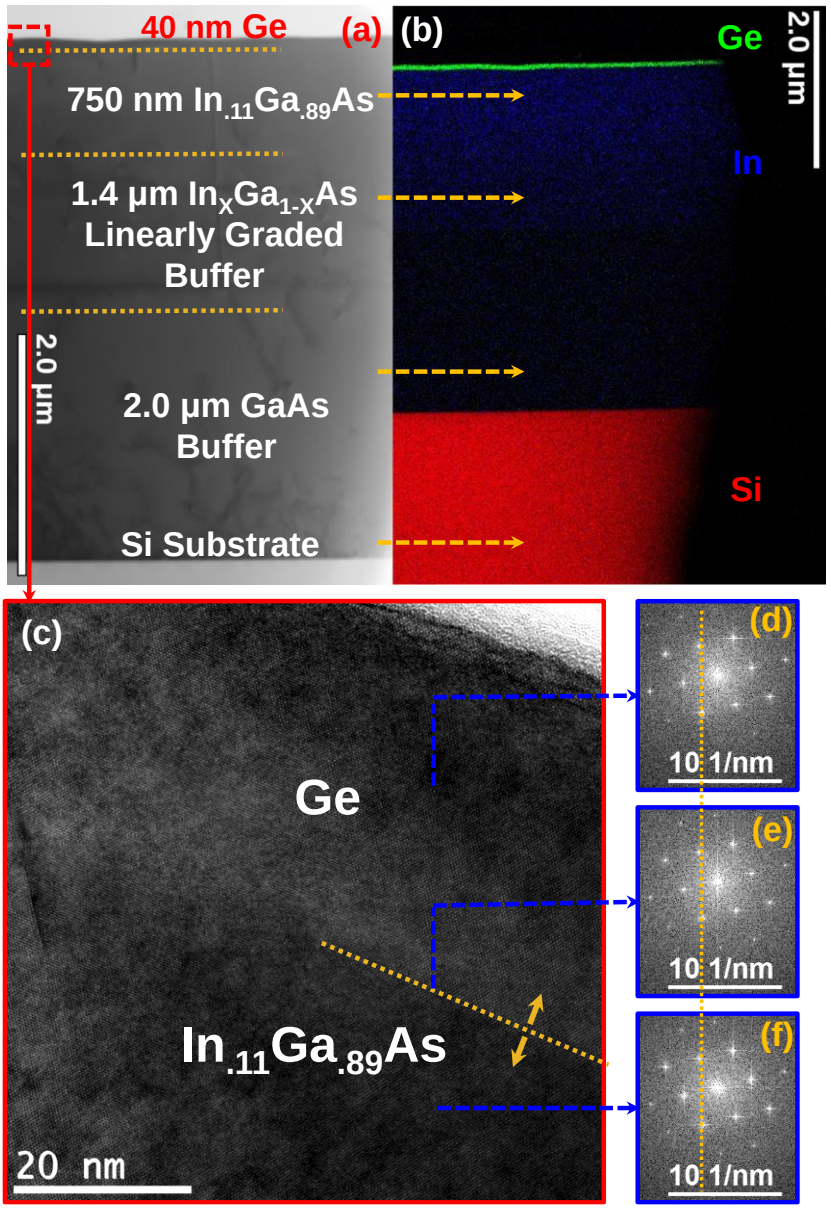

Figure 5.7 (a) Low-resolution cross-sectional TEM micrograph of the 0.82% ε-Ge/$In_{0.11}Ga_{0.89}As$ structure on Si. (b) EDS map of (a) showing distinct, abrupt boundaries between ε-Ge (green)/$In_{0.11}Ga_{0.89}As$ and GaAs/Si (red) as well as In grading (blue). (c)-(f) High-resolution micrographs of the 0.82% ε-Ge/$In_{0.11}Ga_{0.89}As$ heterointerface and detailed lattice line indexing (including FFT patterns) demonstrating the tensile nature of Ge with respect to the underlying $In_{0.11}Ga_{0.89}As$. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

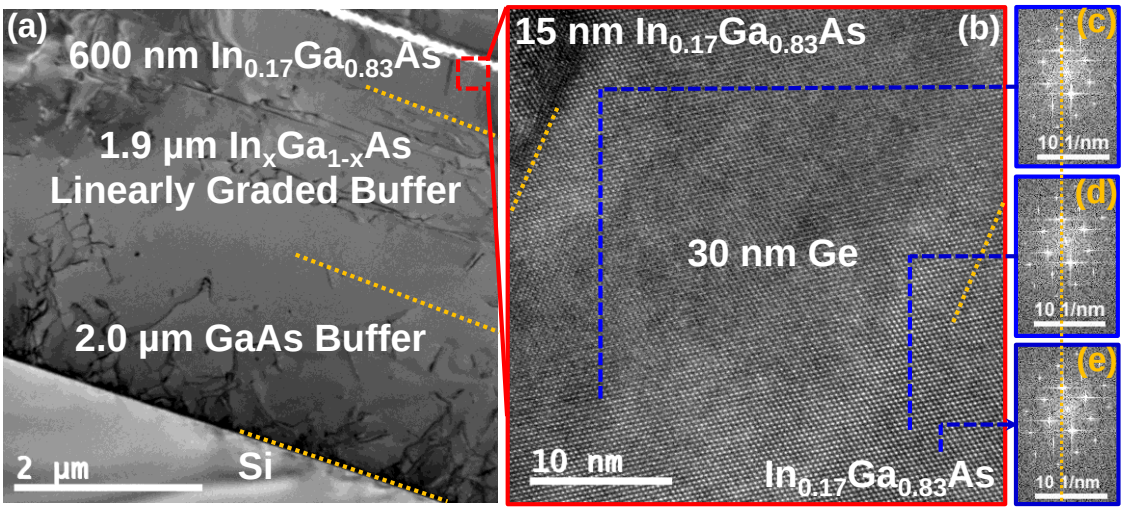

Figure 5.8 (a) Low-resolution cross-sectional TEM micrograph of the 1.11% ε-Ge/$In_{0.17}Ga_{0.83}As$ structure on Si. (b)-(e) High-resolution micrograph of the 1.11% $In_{0.17}Ga_{0.83}As$/ε-Ge/$In_{0.17}Ga_{0.83}As$ heterointerfaces and detailed lattice line indexing (including FFT patterns) demonstrating the tensile nature of Ge with respect to the underlying $In_{0.17}Ga_{0.83}As$. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

5.5. Optical Properties of Strain-Engineered ε-Ge Thin Films on III-V on Si

For this chapter, low-temperature μ-PL measurements were performed at 7.5K utilizing an incident power density of 860 kW/cm^2 and excitation wavelength of 800 nm. This high power density is required to obtain a reasonable PL emission intensity **[26, 27]**. Fig. 5.9 (a) shows the PL spectra obtained from 0.82% (blue) and 1.11% ε-Ge with (red) and without (green) the $In_{0.17}Ga_{0.83}As$ capping layer as well as quasi-lattice matched Ge on AlAs/GaAs (grey). The PL spectra have been shifted vertically for clarity. One can see from Fig. 5.9 (a) that the main peak position is red-shifted towards lower photon energies (higher wavelengths) due to the increase in tensile strain and corresponding reduction in ε-Ge bandgaps. Furthermore, from Figs. 5.9 (b) and 5.9 (c), one can see that each sample exhibits a convolved emission spectra containing a single, intense peak and a shoulder whose relative intensity is strongly strain-dependent.

The deconvolution of these spectral features into accurate transition energies requires considering several coinciding factors, most importantly measurement temperature and strain incorporation. Although it has been reported that experimental collection geometries normal to the sample surface (i.e., $\hat{z}$) favor conduction band coupling with the *hh* valence band **[28]**, cryogenic sample temperatures result in a rapid depopulation of the *hh* valence band due to its higher energy states. Consequently, radiative recombination between the conduction band minima and *lh* valence band increases as heavy-holes undergo rapid non-radiative relaxation into lower energy states within the *lh* valence band. The dominance of the L-*lh* and Γ-*lh* coupling at low measurement temperatures is seen experimentally through direct observation of the lower energy transitions, i.e.

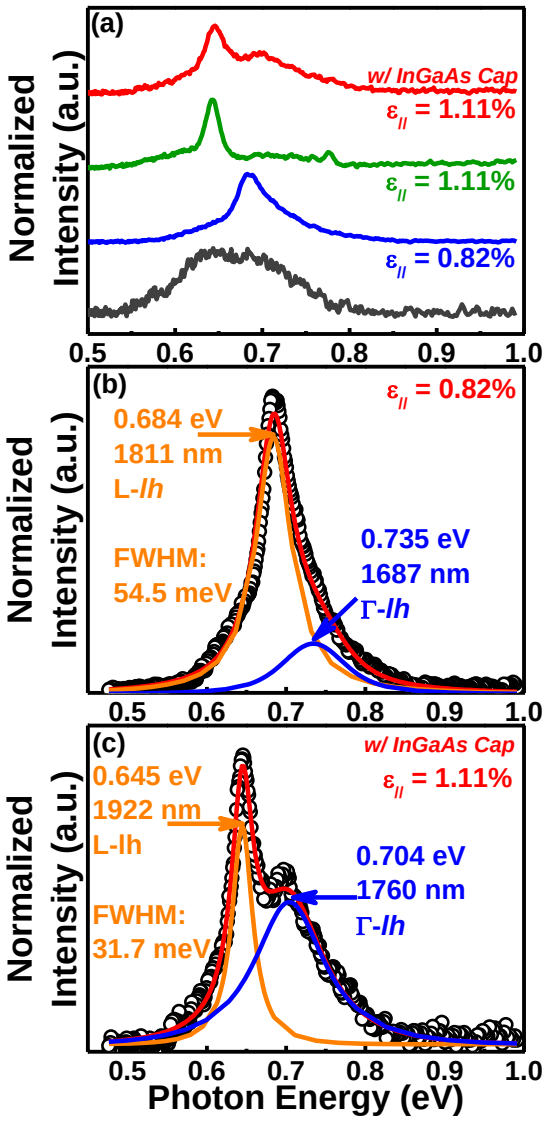

Figure 5.9 (a) Red-shift (plotted in photon energy) due to strain in the ε-Ge epilayers as measured by μ-PL at 7.5 K. (b) and (c) Gauss-Lorentzian fitting of the ε-Ge/$In_{0.11}Ga_{0.89}As$ (b) and ε-Ge/$In_{0.17}Ga_{0.83}As$ (c) emission. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

disparity in intensity between the deconvolved L-*lh* and Γ-*lh* transitions exists, which is in contrast to the reported **[26, 27, 29, 30-32]** nature of the competitiveness between direct and indirect optical transitions in Ge as a function of temperature. This can be

explained via the compounding effects of strain-dependent gain enhancement, prohibitively large energy separations between the L and Γ conduction band minima, and momentum contribution to the indirect L-*lh* recombination path from exciton-generated longitudinal acoustic (LA) phonons. In the former case, several theoretical **[33-36]** and experimental **[37, 38]** studies have demonstrated the effects of increasing tensile strain and doping concentrations on optical gain (or absorption) in Ge films. In particular, Virgilio et al. concluded that for a fixed optical pumping power, the absorption spectrum minimum (i.e., $\alpha(\hbar\omega)$) at the sample's surface trends approximately linearly towards lower photon energies as biaxial tensile strain increases **[33]**. The wavelength-dependence of the absorption coefficient in Ge films as a function of strain proposed by Virgilio and coworkers is found to be in good agreement with prior experimental results **[37, 38]** investigating the temperature- and strain-dependence of Ge optical absorption. From these previous results, one would expect that the lower energy spectral features would exhibit higher relative PL intensities when compared with the higher energy features, which is observed in Figs. 5.9 (b) and 5.9 (c). Nonetheless, one might anticipate that due to the low-temperature nature of the sample during optical characterization, Γ valley recombination would dominate due to reduced phonon-assisted momentum conservation between the L- and Γ-points in momentum space. This interpretation, however, fails to address the need for additional energy in order to surmount the L-Γ conduction band minima separation, which is in addition to the required momentum preservation. For unstrained, bulk Ge, the separation between the L and Γ minima is approximately 150 meV. Thus, although momentum conservation may be met via exciton-generated LA phonons at cryogenic measurement temperatures **[39-41]**, the

aforementioned L-Γ energy difference restricts radiative recombination primarily to L valley pathways for low-to-moderate strains and doping concentrations in which the L-Γ separation remains prohibitively large. It is worth noting that previous work **[42]** investigating similar ε-Ge/$In_xGa_{1-x}As$ double heterostructures revealed an integrated PL intensity power-dependence suggestive of exciton recombination for type-I ε-Ge/$In_xGa_{1-x}As$ heterointerfaces. The detailed analysis of the heterointerface energy band alignment for the structures studied in this work can be found in the subsequent section, suffice to say the structures indeed exhibited a type-I band alignment, thus reinforcing the notion that exciton-phonon interaction underlies the observed indirect radiative recombination **[43]**. Moreover, as higher tensile strains are incorporated, the more rapid lowering of the Γ valley minimum results in a similarly rapid decrease in the L-Γ separation energy, thereby enhancing direct gap recombination as validated by the increase in relative intensity and integrated peak area of the Γ-*lh* transition between Figs. 5.9 (b) and 5.9 (c).

Lastly, it is generally understood that the reduction in effective mass in the *lh* valence band due to strain correlates with a decreasing density of states and an increasingly restricted range of transition energies. Hence, it is expected that the full-width at half-maximum (FWHM) of the more prominent L-*lh* transition as well as the ratio of the integrated peak areas between L-*lh* and Γ-*lh* transitions (i.e., $I_{L\text{-}lh}$:$I_{\Gamma\text{-}lh}$) will both decrease as the biaxial tensile strain held by the Ge epilayer increases. Figs. 5.8 (b) and 5.8 (c) demonstrate that for increasing tensile strain, the FWHM of the L-*lh* transition indeed decreases from 54.5 meV at ε = 0.82% to 31.7 meV at ε = 1.11%. Likewise, the ratio of the L-*lh* to Γ-*lh* integrated peak areas also decreases from 1.95 at ε = 0.82% to 0.30 at ε = 1.11%, indicating that the increase in biaxial tensile strain strongly enhances Γ-*lh*

recombination via significant Γ-*lh* bandgap reduction as well as restricts the energy range for L-*lh* radiative recombination. Fig. 5.10 compares the experimentally observed bandgaps (symbols) and strain determined from μ-PL and XRD analysis, respectively, with the predicted dependence of the low-temperature Ge bandgap on increasing strain (solid lines) calculated using a 30×30 **k·p** formalism [44]. Additionally, the effect of decreasing ε-Ge epilayer thickness (t_{Ge}) on the ε-Ge bandgap due to energy level quantization is shown via the dashed (t_{Ge} = 40 nm) and dotted (t_{Ge} = 30 nm) lines. The measured L-*lh* (Γ-*lh*) bandgaps were found to be 0.684 eV (0.735 eV) and 0.645 eV (0.704 eV) for the ε-Ge/$In_{0.11}Ga_{0.89}As$ and ε-Ge/$In_{0.17}Ga_{0.83}As$ structures, respectively. This is in excellent agreement with the theoretical bandgap-strain relation shown in Fig. 5.10, noting that the quantization effect induced from decreasing ε-Ge layer thickness has a negligible impact on the measured bandgaps for the ε-Ge film thicknesses studied in this work. Furthermore, the demonstration of tunable wavelength ε-Ge epitaxial layers heterogeneously integrated onto Si is a key first step towards the monolithic integration of Ge-based photonic devices and optically active layers with state-of-the-art CMOS technology as well as the development of energy-efficient light sources for future on-chip optical interconnects.

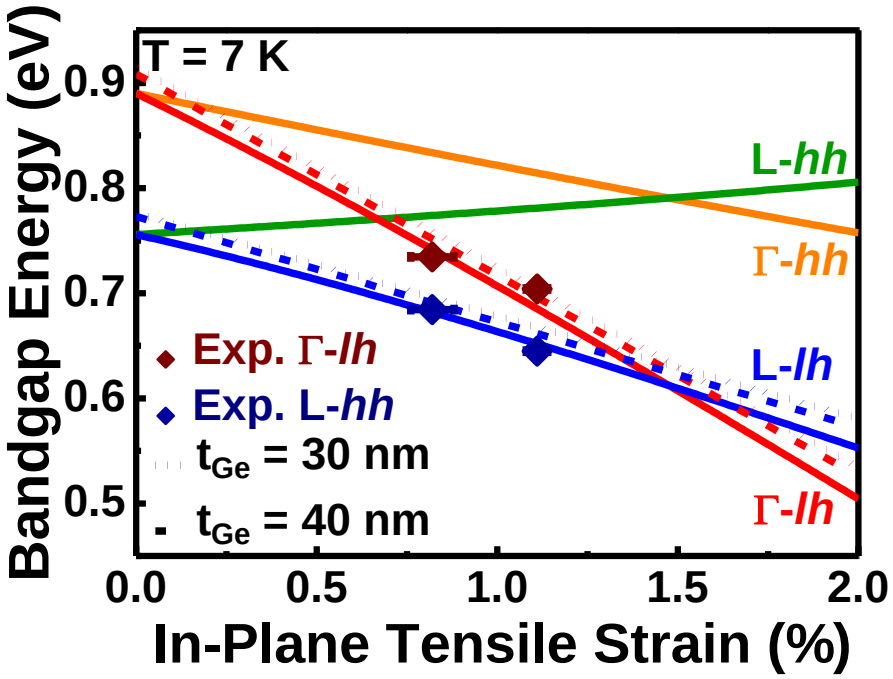

Figure 5.10 μ-PL determined bandgaps of 0.82% and 1.11% ε-Ge in comparison to the theoretical bandgap-strain dependence for Ge calculated using a 30×30 **k·p** model taking into quantization-induced bandgap enhancement at decreased ε-Ge layer thicknesses. Good agreement is found between the measured (symbols) and predicted (lines) bandgaps as a function of increasing tensile strain. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

5.6. Energy Band Alignments of ε-Ge/$In_xGa_{1-x}As$ Active Layers on III-V on Si

Understanding of the energy band alignment between ε-Ge and the underlying constant composition $In_xGa_{1-x}As$ layer is essential for evaluating carrier confinement in future ε-Ge-based optical devices on Si. The valence band and conduction band offsets at the ε-Ge/$In_xGa_{1-x}As$ heterointerface were determined using X-ray photoelectron spectroscopy (XPS) by measuring the atomic core level (CL) binding energies in ε-Ge (Ge 3d) and $In_xGa_{1-x}As$ (As $3d_{5/2}$), the valence band maxima (VBM) of each material, and the interfacial CL binding energy shifts in each material. In order to accurately determine the band offsets, three samples were selected for XPS analysis: (i) 40 nm (30 nm) ε-Ge on $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) was used to measure the CL and VBM binding energy spectra for ε-Ge; (ii) 750 nm (600 nm) $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) without the top ε-Ge layer was used to measure the CL binding energy of arsenic (As) and the VBM of $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$); and (iii) ~2 nm ε-Ge/$In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) was used to measure the CL binding energy shifts of Ge and As at the ε-Ge/$In_xGa_{1-x}As$ heterointerface. The binding energy was corrected by adjusting the carbon (C) 1s CL peak position to 285.0 eV for each sample surface. Residual native oxide was removed from the surface of Ge and $In_xGa_{1-x}As$ using dilute $NH_4OH:H_2O_2:H_2O$ (2:1:200 volume ratio) prior to loading into the XPS chamber. The valence band offset (ΔE_v) between the ε-Ge and the $In_xGa_{1-x}As$ layer was determined using Kraut's method **[45]**, which is widely used in the analysis of heterointerface band discontinuities at semiconductor/semiconductor **[46-49]** as well as dielectric/semiconductor **[50, 51]** heterojunctions. The positive charges generated during the XPS measurements were

neutralized by flowing electrons through the sample stage to prevent un-compensated electron loss that could potentially affect the interfacial band bending results due to sample charging. The valence band offset can be written as **[45]**:

$$\Delta E_V = (E_{Ge\ 3d}^{Ge} - E_{VBM}^{Ge}) - \left(E_{As\ 3d_{\frac{5}{2}}}^{InGaAs} - E_{VBM}^{InGaAs}\right) + \left(E_{As\ 3d_{\frac{5}{2}}}^{InGaAs}(i) - E_{Ge\ 3d}^{Ge}(i)\right) \quad (5.1)$$

where $E_{Ge\ 3d}^{Ge}$ and $E_{As\ 3d_{5/2}}^{InGaAs}$ are the CL binding energies of ε-Ge Ge 3d and $In_xGa_{1-x}As$ As $3d_{5/2}$ CLs, respectively, and E_{VBM} is the VBM of the corresponding material. E_{VBM} is determined by linearly fitting the leading edge of the valence band (VB) spectra to the photoemission background line. $E_{As\ 3d_{\frac{5}{2}}}^{InGaAs}(i)$ and $E_{Ge\ 3d}^{Ge}(i)$ are the CL binding energies of As $3d_{5/2}$ and Ge 3d measured at the heterointerface. The conduction band offset (ΔE_C) can be estimated by **[46-51]**:

$$\Delta E_C = E_G^{InGaAs} - \Delta E_V - E_G^{Ge} \quad (5.2)$$

where E_G^{InGaAs} and E_G^{Ge} are the bandgap energies of $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) and ε-Ge, respectively. The ε-Ge bandgap was extracted from μ-PL measurements as discussed above and assumes the experimentally determined Γ-*lh* bandgap in calculating ΔE_C, whereas the bandgap energy of $In_xGa_{1-x}As$ (x = 0.11, 0.17) was estimated from **[52]**. Figs. 5.11 (a) and 5.11 (b) show the CL and VB spectra from (i) ε-Ge, (ii) $In_{0.11}Ga_{0.89}As$ and $In_{0.17}Ga_{0.83}As$, and (iii) the ε-Ge/$In_{0.11}Ga_{0.89}As$ and ε-Ge/$In_{0.17}Ga_{0.83}As$ (b) interfaces, respectively. The inset shows the schematic layer diagram of the sample used for each measurement. From these spectra, the values of $E_{Ge\ 3d}^{Ge} - E_{VBM}^{Ge}$, $E_{As\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}$ and $E_{As\ 3d_{\frac{5}{2}}}^{InGaAs}(i) - E_{Ge\ 3d}^{Ge}(i)$ were determined to be 29.45 eV, 40.73 eV and 11.55 eV, respectively, for the ε-Ge/$In_{0.11}Ga_{0.89}As$ structure, and 29.45 eV, 40.72 eV and 11.56 eV for the ε-Ge/$In_{0.17}Ga_{0.83}As$ structure. ΔE_v was determined to be 0.27±0.05 eV (0.29±0.05

eV) using (5.1) and the measured binding energy differences. The uncertainty value is taken from the scattering of the VB data with respect to the linear fitting of the VBM position. ΔE_c was determined using (5.2) and the bandgap energy of intrinsic $In_{0.11}Ga_{0.89}As$ ($In_{0.17}Ga_{0.83}As$) at 300 K, i.e., 1.26 eV (1.19 eV) **[52]**. The tensile-strain modified Ge Γ-*lh* bandgap energies of ~0.70 eV and ~0.73 eV were determined from μ-PL measurements and resulted from the simultaneous lifting of the light-hole/heavy-hole valence band degeneracy and reduction of the Γ-point conduction band minima. Using these data, ΔE_c was calculated to be 0.26±0.1 eV (0.20±0.1 eV). It is worth noting that the fitting of the Γ-*lh* bandgap energy from the experimental μ-PL spectra becomes less precise at lower strain levels due to the decreased intensity of the Γ-*lh* optical transition (see μ-PL analysis section), resulting in an increased convolution between the L-*lh* and Γ-*lh* emission spectra and therefore increased error in the calculated ΔE_c value. Additionally, the temperature dependence of the optical bandgaps in Ge will correlate to an increase in ΔE_c as a function of increasing temperature due to the reduction in the Ge bandgap. Hence, the calculated ΔE_c values reported here provide guidance on the effect of increasing tensile strain at the ε-Ge/$In_xGa_{1-x}As$ heterointerface, however are associated with increased uncertainty as compared to the measured ΔE_v values.

Figure 5.12 shows the schematic band alignment diagrams for the (a) ε-Ge/$In_{0.11}Ga_{0.89}As$ and (b) ε-Ge/$In_{0.17}Ga_{0.83}As$ heterojunctions based on the results presented above. One can find from Figure 5.12 that the band alignment at the ε-Ge/$In_xGa_{1-x}As$ heterojunction is type-I for the strain states investigated in this work, which is essential for carrier confinement in the ε-Ge layer for group-IV-based photonic devices. Moreover, the shift in ΔE_V as a function of increasing tensile strain in Ge and In

alloy composition in the underlying strain template corroborates the trend previously reported for low-to-high strain ε-Ge/$In_xGa_{1-x}As$ heterojunctions grown on GaAs substrates [46], indicative of a successful integration scheme for tensile-strained Ge active layers on III-V metamorphic buffer architectures implemented on Si.

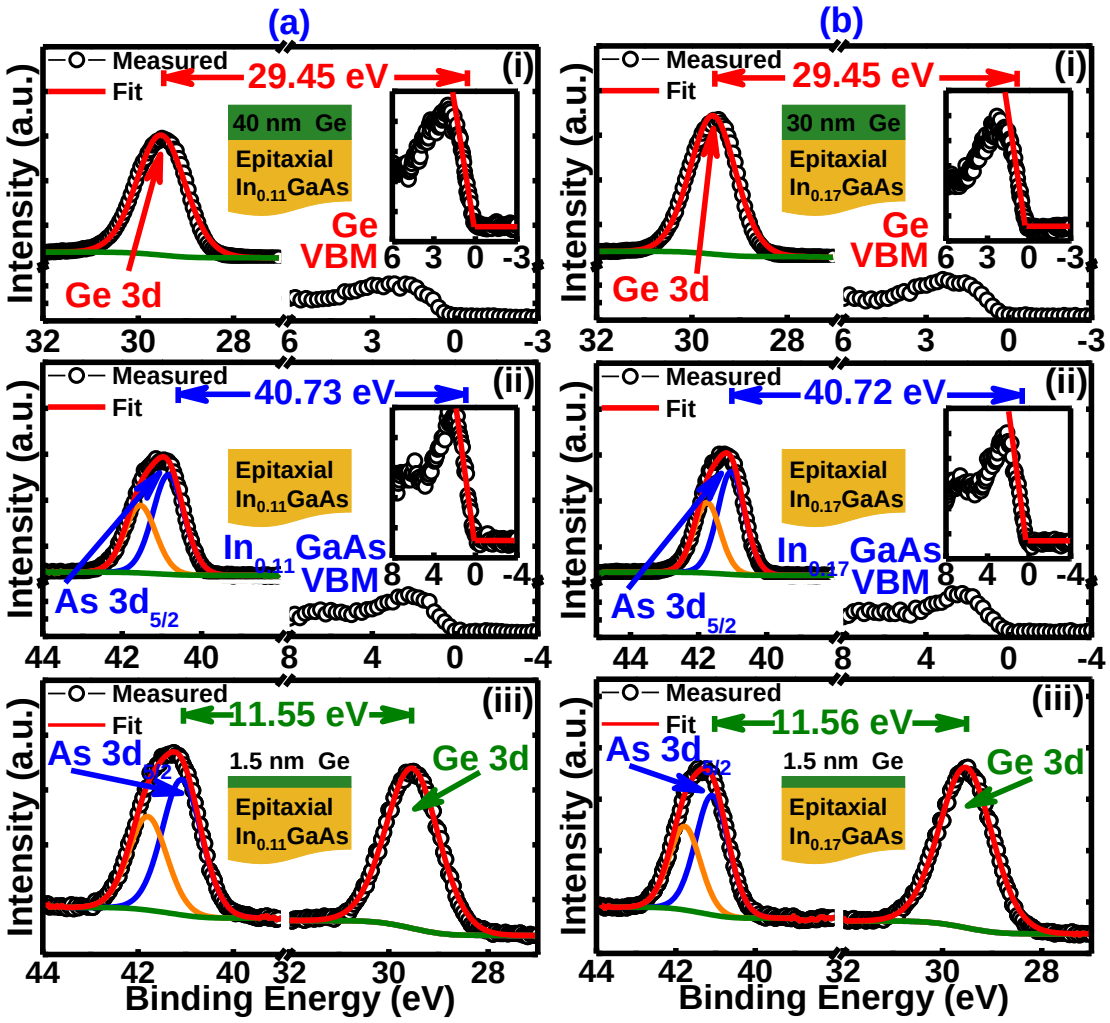

Figure 5.11 Representative photoelectron spectra used in the valence band analysis for the ε-Ge/$In_{0.11}Ga_{0.89}As$ (a) and ε-Ge/$In_{0.17}Ga_{0.83}As$ (b) structures, corresponding to (i) thick (>10 nm) ε-Ge emission, (ii) bulk $In_xGa_{1-x}As$ emission, and (iii) interfacial core level binding energy shifts. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

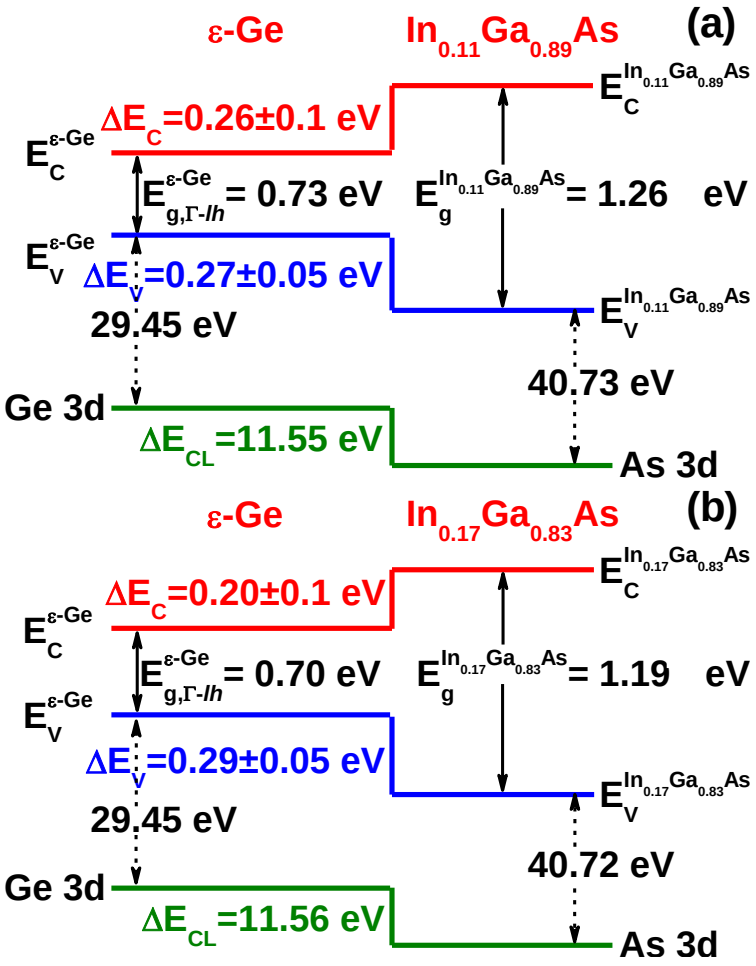

Figure 5.12 Experimentally determined band alignments for the ε-Ge/$In_{0.11}Ga_{0.89}As$ (a) and ε-Ge/$In_{0.17}Ga_{0.83}As$ (b) heterointerfaces utilizing the measured Γ-*lh* bandgaps. Reprinted with permission from Applied Materials and Interfaces. Copyright 2015 American Chemical Society.

References

[1] D. A. B. Miller, Device Requirements for Optical Interconnects to Silicon Chips, *Proc. IEEE* **97**, 1166-1185 (2009).

[2] D. A. B. Miller, Physical Reasons for Optical Interconnection, *Int. J. Optoelectronics* **11**, 155-168 (1997).

[3] D. Liang and J. E. Bowers, Recent Progress in Lasers on Silicon, *Nature Photonics* **4**, 511-517 (2010).

[4] J. Yang, P. Bhattacharya and Z. Wu, Monolithic Integration of InGaAs-GaAs Quantum-Dot Laser and Quantum-Well Electroabsorption Modulator on Silicon, *IEEE Photonics Tech. Lett.* **19**, 747-749 (2007).

[5] S. Jongthammanurak, J. Liu, K. Wada, D. D. Cannon, D. T Danielson, D. Pan, L. C. Kimerling, and J. Michel, Large Electro-Optic Effect in Tensile Strained Ge-on-Si Films, *Appl. Phys. Lett.* **89**, 161115-1—161115-3 (2006).

[6] Y.-H. Kuo, Y. K. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller and J. S. Harris, Strong Quantum-Confined Stark Effect in Germanium Quantum-Well Structures on Silicon, *Nature* **437**, 1334-1336 (2005).

[7] D. Ahn, C.-Y. Hong, J. Liu, W. Giziewicz, M. Beals, L.C. Kimerling, J. Michel, J. Chen and F. X. Kartner, High Performance, Waveguide Integrated Ge Photodetectors, *Optics Express* **15**, 3916-3921 (2007).

[8] L. Vivien, M. Rouviere, J.-M. Fedeli, D. Marris-Morini, J.-F. Damlencourt, J. Mangeney, P. Crozat, L. El Melhaoui, E. Cassan, X. Le Roux, D. Pascal, and S. Laval,

High Speed and High Responsivity Germanium Photodetector Integrated in a Silicon-On-Insulator Microwaveguide, *Optics Express* **15**, 9843-9848 (2007).

[9] J. E. Roth, O. Fidaner, R. K. Schaevitz, Y.-H. Kuo, T. I. Kamins, J. S. Harris and D. A. B. Miller, Optical Modulator on Silicon Employing Germanium Quantum Wells, *Optics Express* **15**, 5851-5859 (2007).

[10] N.-N. Feng, D. Feng, S. Liao, X. Wang, P. Dong, H. Liang, C.-C. Kung, W. Qian, J. Fong, R. Shafiiha, Y. Luo, J. Cunningham, A. V. Krishnamoorthy and M. Asghari, 30GHz Ge Electro-Absorption Modulator Integrated with 3μm Silicon-on-Insulator Waveguide, *Optics Express* **19**, 7062-7067 (2011).

[11] J. Liu, X. Sun, R. Camacho-Aguilera, L. C. Kimerling and J. Michel, Ge-on-Si Laser Operating at Room Temperature. *Optics Lett.* **35**, 679-681 (2010).

[12] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling and J. Michel, An Electrically Pumped Germanium Laser, *Optics Express* **20**, 11316-11320 (2012).

[13] S. Cho, B.-G. Park, C. Yang, S. Cheung, E. Yoon, T. I. Kamins, S. J. B. Yoo and J. S. Harris, Room-Temperature Electroluminescence from Germanium in an $Al_{0.3}Ga_{0.7}As$/Ge Heterojunction Light-Emitting Diode by Γ-Valley Transport, *Optics Express* **20**, 14921-14927 (2012).

[14] S. Assefa, F. Xia and Y. A. Vlasov, Reinventing Germanium Avalanche Photodetector for Nanophotonic On-Chip Optical Interconnects, *Nature* **464**, 80-84 (2010).

[15] J.-M. Fedeli, B. B. Bakir, N. Olivier, Ph. Grosse, L. Grenouillet, E. Augendre, P. Philippe, K. D. Bordel and J. Harduin, InP on SOI Devices for Optical Communication and Optical Network on Chip, *Proc. SPIE* **7942**, 79420O-1—79420O-9 (2011).

[16] G.-H. Duan, C. Jany, A. Le Liepvre, A. Accard, M. Lamponi, D. Make, P. Kaspar, G. Levaufre, N. Girard, F. Lelarge, J.-M. Fedeli, S. Messaoudene, D. Bordel and S. Olivier, Hybrid III-V on Silicon Lasers for Photonic Integrated Circuits on Silicon, *Proc SPIE* **9002**, 90020X-1—90020X-6 (2014).

[17] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca and D. Grutzmacher, Lasing in Direct-Bandgap GeSn Alloy Grown on Si, *Nature Photonics* **9**, 88-92 (2015).

[18] S. Wirths, A. T. Tiedemann, Z. Ikonic, P. Harrison, B. Hollander, T. Stoica, G. Mussler, M. Hartmann, D. Grutzmacher, D. Buca and S. Mantl, Band Engineering and Growth of Tensile Strained Ge/(Si)GeSn Heterostructure Tunnel Field Effect Transistors, *Appl. Phys. Lett.* **102**, 192103-1—192103-4 (2013).

[19] S. Wirths, D. Stange, M.-A. Pampillon, A. T. Tiedemann, G. Mussler, A. Fox, U. Breuer, B. Baert, E. San Andres, N. D. Nguyen, J.-M. Hartmann, Z. Ikonic, S. Mantl and D. Buca, High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-Effect Transistors, *ACS Appl. Mater. Interfaces* **7**, 62-67 (2015).

[20] M. K. Hudait and S. B. Krupanidhi, Self-Annihilation of Antiphase Boundaries in GaAs Epilayers on Ge Substrates Grown by Metal-Organic Vapor-Phase Epitaxy. *J. Appl. Phys.* **89**, 5972-5979 (2001).

[21] S. M. Ting and E. A. Fitzgerald, Metal-Organic Chemical Vapor Deposition of Single Domain GaAs on $Ge/Ge_xSi_{1-x}/Si$ and Ge Substrates, *J. Appl. Phys.* **87**, 2618-2628 (2000).

[22] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, N. Monsegue and M. K. Hudait, Defect Assistant Band Alignment Transition from Staggered to Broken Gap in Mixed As/Sb Tunnel Field Effect Transistor Heterostructure, *J. Appl. Phys.* **112**, 094312-1—094312-9 (2012).

[23] O. Madelung, *Semiconductors: Intrinsic Properties of Group IV, III-V, II-VI, and I-VII Compounds*, Vol. 22a, Springer: Berlin (1985).

[24] Y. Bai, K. E. Lee, C. Cheng, M. L. Lee and E. A. Fitzgerald, Growth of Highly Tensile-Strained Ge on Relaxed $In_xGa_{1-x}As$ by Metal-Organic Chemical Vapor Deposition, *J. Appl. Phys.* **104**, 084518-1—084518-9 (2008).

[25] Y.-Y. Fang, J. Tolle, R. Roucka, A. V. G. Chizmeshya, J. Kouvetakis, V. R. D'Costa and J. Menendez, Perfectly Tetragonal, Tensile-Strained Ge on $Ge_{1-y}Sn_y$ Buffered Si(100), *Appl. Phys. Lett.* **90**, 061915-1—061915-3 (2007).

[26] H. M. van Driel, A. Elci, J. S. Bessey and M. O. Scully, Photoluminescence Spectra of Germanium at High Excitation Intensities, *Solid State Comm.* **20**, 837-840 (1976).

[27] W. Klingenstein and H. Schweizer, Direct Gap Recombination in Germanium at High Excitation Level and Low Temperature, *Solid-State Elec.* **21**, 1371-1374 (1978).

[28] J. R. Sanchez-Perez, C. Boztug, F. Chen, F. F. Sudradjat, D. M. Paskiewicz, R.B. Jacobson, M. G. Lagally and R. Paiella, Direct-Bandgap Light-Emitting Germanium in Tensilely Strained Nanomembranes, *Proc. Nat. Acad. Sci.* **108**, 18893-18898 (2011).

[29] T.-H. Cheng, C.-Y. Ko, C.-Y. Chen, K.-L. Peng, G.-L. Luo, C. W. Liu and H.-H. Tseng, Competitiveness Between Direct and Indirect Radiative Transitions of Ge, *Appl. Phys. Lett.* **96**, 091105-1—091105-3 (2010).

[30] G. Grzybowski, R. Roucka, J. Mathews, L. Jiang, R. T. Beeler, J. Kouvetakis and J. Menendez, Direct Versus Indirect Optical Recombination in Ge Films Grown on Si Substrates, *Phys. Rev. B* **84**, 205307-1—205307-6 (2011).

[31] S. Manna, A. Katiyar, R. Aluguri and S. K. Ray, Temperature Dependent Photoluminescence and Electroluminescence Characteristics of Core-Shell Ge-GeO2 Nanowires, *J. Phys. D: Appl. Phys.* **48**, 215103-1—215103-6 (2015).

[32] Y. Huo, H. Lin, R. Chen, M. Makarova, Y. Rong, M. Li, T. I. Kamins, J. Vuckovic and J. S. Harris, Strong Enhancement of Direct Transition Photoluminescence with Highly Tensile-Strained Ge Grown by Molecular Beam Epitaxy. *Appl. Phys. Lett.* **98**, 011111-1—011111-3 (2011).

[33] M. Virgilio, C. L. Manganelli, G. Grosso, T. Schroeder and G. Capellini, Photoluminescence, Recombination Rate, and Gain Spectra in Optically Excited n-type and Tensile Strained Germanium Layers, *J. Appl. Phys.* **114**, 243102-1—243102-11 (2013).

[34] Y. Cai, Z. Han, X. Wang, R. E. Camacho-Aguilera, L. C. Kimerling, J. Michel and J. Liu, Analysis of Threshold Current Behavior for Bulk and Quantum-Well Germanium Laser Structures. *IEEE J. Sel. Top. Quantum. Electron.* **19**, 1901009-1—1901009-9 (2013).

[35] G. Pizzi, M. Virgilio and G. Grosso, Tight-Binding Calculation of Optical Gain in Tensile Strained [001]-Ge/SiGe Quantum Wells, *Nanotechnology* **21**, 055202-1—055202-7 (2010).

[36] S.-W. Chang and S. L. Chuang, Theory of Optical Gain of Ge-$Si_xGe_ySn_{1-x-y}$ Quantum-Well Lasers, *IEEE J. Quantum Electron.* **43**, 249-256 (2007).

[37] V. Sorianello, A. Perna, L. Colace, G. Assanto, H. C. Luan and L. C. Kimerling, Near-Infrared Absorption of Germanium Thin Films on Silicon, *Appl. Phys. Lett.* **93**, 111115-1—111115-3 (2008).

[38] J. Liu, X. Sun, L. C. Kimerling and J. Michel, Direct-gap Optical Gain of Ge on Si at Room Temperature, *Optics Lett.* **34**, 1738-1740 (2009).

[39] R. R. Lieten, K. Bustillo, T. Smets, E. Simoen, J. W. Ager, E. E. Haller and J.-P. Locquet, Photoluminescence of Bulk Germanium. *Phys. Rev. B* **86**, 035204-1—035204-5 (2012).

[40] G. A. Thomas, E. I. Blount and M. Capizzi, Indirect Recombination Mechanisms in Germanium. *Phys. Rev. B* **19**, 702-718 (1979).

[41] T. Nishino, M. Takeda and Y. Hamakawa, Indirect Exciton Absorption in Germanium. J. *Phys. Soc. Japan* **37**, 1016-1023 (1974).

[42] N. Pavarelli, T. J. Ochalski, F. Murphy-Armando, Y. Huo, M. Schmidt, G. Huyet and J. S. Harris, Optical Emission of a Strained Direct-Band-Gap Ge Quantum Well Embedded Inside InGaAs Alloy Layers, *Phys. Rev. Lett.* **110**, 177404-1—177404-5 (2013).

[43] S. Jin, Y. Zheng and A. Li, Characterization of Photoluminescence Intensity and Efficiency of Free Excitons in Semiconductor Quantum Well Structures, *J. Appl. Phys.* **82**, 3870-3873 (1997).

[44] M. El Kurdi, G. Fishman, S. Sauvage and P. Boucaud, Band Structure and Optical Gain of Tensile-Strained Germanium Based on a 30 Band k·p Formalism, *J. Appl. Phys.* **107**, 013710-1—013710-7 (2010).

[45] E. A. Kraut, R. W. Grant, J. R. Waldrop and S. P. Kowalczyk, Precise Determination of the Valence-Band Edge in X-Ray Photoemission Spectra: Application to Measurement of Semiconductor Interface Potentials, *Phys. Rev. Lett.* **44**, 1620-1623 (1980).

[46] M. Clavel, P. S. Goley, N. Jain, Y. Zhu and M. K. Hudait, Strain Engineered Biaxial Tensile Epitaxial Germanium for High-Performance Ge/InGaAs Tunnel Field-Effect Transistors, *IEEE J. Elec. Dev. Soc.* **3**, 184-193 (2015).

[47] Y. Zhu, D. Maurya, S. Priya and M. K. Hudait, Tensile-Strained Nanoscale Ge/$In_{0.16}Ga_{0.84}As$ Heterostructure for Tunnel Field-Effect Transistor, *ACS Appl. Mater. Interfaces* **6**, 4947-4953 (2014).

[48] J.-S. Liu, Y. Zhu, P. S. Goley and M. K. Hudait, Heterointerface Engineering of Broken-Gap InAs/GaSb Multilayer Structures, *ACS Appl. Mater. Interfaces* **7**, 2512-2517 (2015).

[49] M. K. Hudait, M. Clavel, P. S. Goley, N. Jain and Y. Zhu, Heterogeneous Integration of Epitaxial Ge on Si Using AlAs/GaAs Buffer Architecture: Suitability for Low-Power Fin Field-Effect Transistors, *Scientific Reports* **4**, 6964-1—6964-6 (2014).

[50] M. K. Hudait, M. Clavel, Y. Zhu, P. S. Goley, S. Kundu, D. Maurya and S. Priya, Integration of $SrTiO_3$ on Crystallographically Oriented Epitaxial Germanium for Low-Power Device Applications, *ACS Appl. Mater. Interfaces* **7**, 5471-5479 (2015).

[51] Y. Zhu, M. Clavel, P. S. Goley and M. K. Hudait, Growth, Strain Relaxation Properties and High-k Dielectric Integration of Mixed-Anion $GaAs_{1-y}Sb_y$ Metamorphic Materials, *J. Appl. Phys.* **116**, 134304-1—134304-9 (2014).

[52] S. Paul, J. B. Roy and P. K. Basu, Empirical Expressions for the Alloy Composition and Temperature Dependence of the Band Gap and Intrinsic Carrier Density in $Ga_xIn_{1-x}As$, *J. Appl. Phys.* **69**, 827-829 (1991).

Chapter 6 – Conclusions and Future Prospects

6.1. Summary

The tensile-strained Ge (ε-Ge)/$In_xGa_{1-x}As$ material system has recently been proposed as a novel candidate for the monolithic integration of alternate-channel, CMOS technology with nanoscale, group VI-based optoelectronics. The intrinsically low bandgap, low carrier tunneling and transport effective masses, and high mobility of group VI (ε-Ge, Ge_xSn_{1-x}) and III-V materials are promising for the development of steep subthreshold slope (SS) tunnel field-effect transistors (TFETs) operating in the ultra-low power ($V_{DD} \leq 0.3$ V) regime. By adopting the TFET device architecture and leveraging the band-to-band tunneling transport mechanism, such devices offer substantial improvements in SS reduction while maintaining high ON-state current (I_{ON}) necessary for fan-out and high-speed operation at the ultimate physical limits of CMOS scaling. The ability to tailor the heterointerface band alignment between ε-Ge and $In_xGa_{1-x}As$ by carefully controlling the indium (In) alloy composition, and hence strain in the ε-Ge, allows for greater flexibility in tuning the effective tunneling barrier height, E_{beff}, and thereby the operating voltage of the TFET device. Similarly, the reduction of the ε-Ge bandgap through band structure engineering *via* strain engineering provides a path for future nanophotonics applications based on direct bandgap, highly-strained ε-Ge. In this research, the material properties of ε-Ge/$In_xGa_{1-x}As$ heterostructures were comprehensively investigated. The results are summarized below:

(1) The structural, morphological, and band alignment properties of solid-source MBE-grown biaxial tensile-strained Ge/$In_xGa_{1-x}As$ TFET heterostructures on GaAs were systematically studied. Device-quality ε-Ge/$In_xGa_{1-x}As$ heterojunctions were observed for

in-plane strains within the epitaxial Ge of 0.75% ($In_{0.16}Ga_{0.84}As$), 1.6% ($In_{0.24}Ga_{0.76}As$), and 1.94% ($In_{0.29}Ga_{0.71}As$). High-resolution X-ray diffraction (HR-XRD) and transmission electron microscopy (TEM) studies validated the defect-free, pseudomorphic nature of the ε-Ge/$In_xGa_{1-x}As$ interfaces and confirmed the high crystalline quality and low dislocation density of the active device layers in the n^+-i-p^+ and p^+-i-n^+ structures. Moreover, the $In_xGa_{1-x}As$ virtual substrates exhibited uniform, two-dimensional cross-hatch patterns with root-mean-square (rms) roughness ~4 nm, as found by atomic force microscopy, suggesting a quasi-ideal relaxation of the metamorphic buffers and coherent strain transfer to the Ge lattice. The energy band alignment for each ε-Ge/$In_xGa_{1-x}As$ heterojunction demonstrated a positive, monotonic trend as a function of increasing strain, validating the ability to engineer the source-channel effective tunneling barrier height through pseudomorphic strained-layer epitaxy. The superior structural characteristics and tunable band alignment properties of the ε-Ge/$In_xGa_{1-x}As$-based TFET architectures studied in this work provide critical guidance for future low standby power, energy-efficient, high-performance tunnel field-effect transistor applications.

(2) Tunable tensile-strained Ge epilayers heterogeneously integrated on Si using composite GaAs and linearly graded $In_xGa_{1-x}As$ buffers grown by solid-source MBE were comprehensively investigated. HR-XRD provided the strain state of each ε-Ge layer as well as the micro structural quality of the Ge thin films and buffer architectures, revealing strain levels of 0.82±0.06% and 1.11±0.03% for the ε-Ge/$In_{0.11}Ga_{0.89}As$ and ε-Ge/$In_{0.17}Ga_{0.83}As$ heterostructures studied in this work. The tensile strain was further corroborated by micro-Raman spectroscopy, where the strain-induced peak shift with

respect to bulk Ge independently validated the strain state of the ε-Ge. Sharp heterointerfaces between each ε-Ge epilayer and the respective $In_xGa_{1-x}As$ virtual substrate were achieved, as demonstrated by low- and high-magnification TEM. Low-temperature micro-photoluminescence measurements demonstrated optical transitions from the L and Γ valley conduction bands to the light-hole valence band for all ε-Ge strain states studied in this work. Furthermore, the μ-PL measurements demonstrated an effective, strain-induced bandgap modulation, with L-*lh* (Γ-*lh*) bandgaps of 0.684 eV (0.735 eV) and 0.645 eV (0.704 eV) for the 0.82% and 1.11% strained Ge layers, respectively, that were in agreement with theoretical calculations for the Ge bandgap-strain relationship derived using a 30×30 ***k·p*** formalism. A type-I energy band alignment with valence band offsets of 0.27 eV and 0.29 eV for the ε-Ge/$In_{0.11}Ga_{0.89}As$ and ε-Ge/$In_{0.17}Ga_{0.83}As$ heterojunctions was revealed *via* X-ray photoelectron spectroscopy analysis, suggesting that the ε-Ge/$In_xGa_{1-x}As$ heterointerface is feasible for carrier confinement in optical devices utilizing increased strain. Consequently, the tunable tensile-strained Ge materials growth, structural and optical properties, and band offset parameters provide a path for the realization of novel Ge-based photonic devices integrated on Si.

Thus, this research demonstrates the feasibility of the ε-Ge/$In_xGa_{1-x}As$ material system for applications in ultra-low power, high-performance complimentary logic and Ge-based nanophotonics as well as their heterogeneous integration on Si. Experimental results, in close agreement with theoretical predictions, demonstrate the potential for group IV (ε-Ge, Ge_xSn_{1-x}) and III-V materials to extend electronic and photonic technology beyond state-of-the-art Si scaling. The superior structural and optical

properties of ε-Ge/$In_xGa_{1-x}As$ heterostructures on GaAs, and their transferability to large-area, low-cost Si, combined with a robust method of band structure and alignment engineering *via* epitaxial strain engineering, offers a unique opportunity to realize the monolithic heterogeneous integration of ε-Ge/$In_xGa_{1-x}As$ electronics and photonics on Si.

6.2. Prospects for Future Research

In order to leverage the research results discussed above and fully exploit the advantages of ε-Ge/$In_xGa_{1-x}As$-based electronic and optoelectronic devices, additional research must be done in the following areas:

(1) Recent device simulation results have predicted that the most viable ε-Ge/$In_xGa_{1-x}As$ TFET heterostructures for n- and p-MOS devices are: (i) p^+ Ge-*i* $In_xGa_{1-x}As$-n^+ $In_xGa_{1-x}As$, and (ii), p^+ Ge-*i* Ge-n^+ $In_xGa_{1-x}As$, respectively. In the case of the n-MOS TFET architecture, the high electron mobility $In_xGa_{1-x}As$ acts as the channel material while the source/channel interface occurs at the p^+ Ge/*i* $In_xGa_{1-x}As$ interface. Conversely, in the case of the p-MOS TFET design, the high hole mobility ε-Ge is best suited for the channel material while the source/channel interface occurs at the n^+ $In_xGa_{1-x}As$/*i* Ge interface. For either device architecture, there have been no experimental studies examining the relationship between strain and band alignment at the p^+ Ge/*i* $In_xGa_{1-x}As$ heterointerface for ε-Ge epilayers that are *in situ* doped with a *p*-type dopant. Thus, a similar investigation as to that performed in ***Chapter 4*** must be performed in order to verify the predictions of the computer-aided design (CAD) models and establish a procedure on record (POR) for the ε-Ge/$In_xGa_{1-x}As$ TFET design criterion. In doing so, the role of doping (*n*- or *p*-type) on the heterointerface band alignment would also be elucidated.

(2) In addition to the role of doping (*n*- or *p*-type) on the band alignment at the ε-Ge/$In_xGa_{1-x}As$ heterointerface, it is also essential to understand the effect of strain on the band alignment at the oxide/ε-Ge interface in MOS devices, a necessary step for realizing n- and p-channel ε-Ge/InGaAs TFETs. In order to effectively confine carriers to the channel and minimize gate leakage, the valence and conduction band offsets (ΔE_V and ΔE_C, respectively), should be > 1.0 eV for all strain levels investigated. Industry standard gate oxides, including Al_2O_3, HfO_2, and Ta_2O_5, must be integrated and characterized on ε-Ge (as well as *i* $In_xGa_{1-x}As$) in order to establish a common gate dielectric scheme that is viable for both *i* ε-Ge and *i* $In_xGa_{1-x}As$ channels. Moreover, a common passivation scheme must be developed for both *i* ε-Ge and *i* $In_xGa_{1-x}As$ materials such that the interface defect density, D_{it}, is minimized, thereby enhancing gate control over the channel and the source/channel interface and improving SS.

(3) Lastly, the primary objective of the research presented in this thesis is to demonstrate both *n*- and *p*-channel ε-Ge/$In_xGa_{1-x}As$ TFET devices. In order to achieve this goal, several challenges must be met, including: (i) designing, growing, characterizing and developing a POR for a high-bandgap metamorphic buffer, such as $In_xAl_{1-x}As$, that will minimize parallel conduction during device operation and is internally lattice matched to the active ε-Ge/$In_xGa_{1-x}As$ region; (ii) developing a device fabrication process flow for ε-Ge/$In_xGa_{1-x}As$-based nano-pillar and sidewall TFET architectures; and (iii), electrical characterization and reliability studies of the fabricated ε-Ge/$In_xGa_{1-x}As$ TFET devices as a function of strain (across multiple TFET device designs) and temperature. Moreover, these devices, once demonstrated on GaAs, must be transferrable to Si, as demonstrated in ***Chapter 5***. In doing so, measures must be taken

such that in implementing (i) on Si, additional surface roughness due to differing surface adatom mobilities between Al and In during growth must be minimized. This effect is compounded by the difference in thermal conductivity between Si and GaAs substrates. Furthermore, care must be taken to minimize the formation of additional threading dislocations when growing on Si, as propagation of such defects along the growth direction into the active layer will alter the band alignment properties of the device and therefore its electrical characteristics. In addition, the study of ε-Ge/$In_xGa_{1-x}As$ strain relaxation properties as a function of temperature are necessary to establish optimal thermal budgets to be monitored in (ii). By systematically and comprehensively investigating these areas, a path can be demonstrated for realizing ε-Ge/$In_xGa_{1-x}As$ complimentary TFET logic on Si.

Appendix

List of Publications

JOURNAL PAPERS:

1. N. Shehata, **M. Clavel**, K. Meehan, E. Samir, S. Gaballah and M. Salah, Enhanced Erbium-Doped Ceria Nanostructure Coating to Improve Solar Cell Performance, *Materials* **8**, 7663-7672 (2015).

2. **M. Clavel**, D. Saladukha, P. S. Goley, T. J. Ochalski, F. Murphy-Armando, R. J. Bodnar and M. K. Hudait, Heterogeneously-Grown Tunable Tensile Strained Germanium on Silicon for Photonic Devices, *ACS Appl. Mater. Interfaces* **7**, 26470-26481 (2015).

2. M. K. Hudait, **M. Clavel**, P. S. Goley, Y. Xie and J. J. Heremans, Magnetotransport Properties of Epitaxial Ge/AlAs Heterostructure Integrated on GaAs and Silicon, *ACS Appl. Mater. Interfaces* **7**, 22315-22321 (2015).

3. J.-S. Liu, **M. Clavel** and M. K. Hudait, Performance Evaluation of Novel Strain-Engineered Ge-InGaAs Heterojunction Tunnel Field-Effect Transistors, *IEEE Trans. Electron Devices* **62**, 3223-3228 (2015).

4. S. Kundu, B. Chen, H-C. Song, P. Kumar, S. Priya, **M. Clavel** and M. K. Hudait, Lead-Free Epitaxial Ferroelectric Material Integration on Semiconducting (100) Nb-Doped $SrTiO_3$ for Low-Power Non-Volatile Memory and Efficient Ultraviolet Ray Detection, *Sci. Rep.* **5**, 1-14 (2015).

5. P. D. Nguyen, **M. Clavel**, P. S. Goley, J.-S. Liu, N. Allen, L. J. Guido and M. K. Hudait, Heteroepitaxial Ge MOS Devices on Si Using Composite AlAs/GaAs Buffer, *IEEE J. Elec. Dev. Soc.* **3**, 341-348 (2015).

6. M. K. Hudait, **M. Clavel**, Y. Zhu, P. S. Goley, S. Kundu, D. Maurya and S. Priya, Integration of $SrTiO_3$ on Crystallographically Oriented Epitaxial Germanium for Low-Power Device Applications, *ACS Appl. Mater. Interfaces* **7**, 5471-5479 (2015).

7. S. Kundu, D. Maurya, **M. Clavel**, Y. Zhou, N. N. Halder and M. K. Hudait, Integration of Lead-Free Ferroelectric on HfO_2/Si (100) for High Performance Non-Volatile Memory Applications, *Sci. Rep.* **5**, 8494-8503 (2015).

8. **M. Clavel**, P. S. Goley, N. Jain, Y. Zhu and M. K. Hudait, Strain-Engineered Biaxial Tensile Epitaxial Germanium for High-Performance Ge/InGaAs Tunnel Field-Effect Transistors, *IEEE J. Elec. Dev. Soc.* **3**, 184-193 (2015).

9. M. K. Hudait, Y. Zhu, P. S. Goley, **M. Clavel** and N. Jain, Mixed-Anion $GaAs_{1-y}Sb_y$ Graded Buffer Heterogeneously Integrated on Si by Molecular Beam Epitaxy, *Appl. Phys. Exp.* **8**, 025501-025503 (2015).

10. Y. Zhu, **M. Clavel**, P. S. Goley and M. K. Hudait, Growth, Strain Relaxation Properties and High-κ Dielectric Integration on Mixed-Anion $GaAs_{1-y}Sb_y$ Metamorphic Materials, *J. Appl. Phys.* **116**, 134304-1—134304-9 (2014).

11. M. K. Hudait, **M. Clavel**, P. S. Goley, N. Jain and Y. Zhu, Heterogeneous Integration of Epitaxial Ge on Si Using AlAs/GaAs Buffer Architecture: Suitability for Low-Power Fin Field-Effect Transistors, *Sci. Rep.* **4**, 6964-6969 (2014).

12. N. Shehata, K. Meehan, I. Hassounah, M. K. Hudait, N. Jain, **M. Clavel**, S. El-Helw and N. Madi, Reduced Erbium-Doped Ceria Nanoparticles: One Nano-Host Applicable for Simultaneous Optical Down- and Up-Conversions, *Nano. Res. Lett.* **9**, 231 (2014).

CONFERENCE PAPERS:

1. N. Jain, **M. Clavel**, P. S. Goley and M. K. Hudait, Towards a Monolithic, All-Epitaxial and Reusable-Substrate Design for III-V-on-Si Solar Cells, 42nd IEEE Photovoltaic Specialist Conference, New Orleans, LA, June 14-19, 2015.

2. S. Kundu, **M. Clavel**, D. Maurya, M. K. Hudait and S. Priya, Charge Storage Properties of $Al/(1-x)BaTiO_3-xBa(Cu_{1/3}Nb_{2/3})O_3/HfO_2/p\text{-}Si$ Metal/Ferroelectric/Insulator/Semiconductor Devices, 61st AVS International Symposium and Exhibition, Baltimore, MD, Nov. 9-14, 2014.

3. N. Jain, Y. Zhu, **M. Clavel**, P. S. Goley and M. K. Hudait, Performance Evaluation of Monolithically Integrated 3J InGaP/GaAs/Si Tandem Solar Cells for Concentrated Photovoltaics, 40th IEEE Photovoltaic Specialist Conference, Denver, CO, June 8-13, 2014.