Design of Extreme Efficiency Active Rectifiers for More-electric Aircrafts

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ABSTRACT

The More-electric aircraft (MEA) concept has been raised since 1990s in order to increase fuel economy and reduce environmental impact of aircrafts. The fundamental of the concept is to replace pneumatic, hydraulic and mechanical systems in conventional aircrafts with its electrical equivalent that is lighter and more reliable. In this movement, power electronics technology plays a key role in interfacing the new types of electrical loads to the new aircraft electrical power system. One of the major tasks for power electronics circuits in MEA is to transfer aircraft variable frequency AC voltage into DC voltage, which could be conveniently utilized by different types of loads or power buses. The converters carrying out the task is commonly known as "rectifiers". This work aims at designing and constructing rectifiers that can work efficiently and reliably in more-electric aircrafts.

One of the major challenge for these rectifiers comes from the complex aircraft environment. The ambient temperature could be as high as 70 ℃. Moreover, active cooling for converters may not be desirable. To deal with this, rectifiers should achieve extreme efficiency (especially at full load) so that all the components are not overheated without active cooling. This work aims at achieving extreme converter efficiency through advanced converter topologies and design. Both single-phase and three-phase rectifiers are discussed in this work.

For single-phase rectifiers, this work focused on boost-type power factor correction (PFC) converters due to the promising efficiency and good PFC characteristics. The well-known two-level semi-bridgeless PFC boost rectifier, together with its interleaved and three-level counterparts, are studied and compared in this work. The operation principles of the converters are analyzed. Models and methods for converter efficiency evaluation are discussed. The efficiency evaluation of the topologies shows the advantage of three-level topologies and interleaved topologies in achieving higher efficiency and better thermal management.

For three-phase rectifiers, two-level boost rectifier, three-level neutral point clamped (NPC) rectifier and Vienna rectifier are investigated. The evaluation shows the advantage of Vienna rectifier in achieving high efficiency due to reduced switching loss.

Based on the evaluation of single-phase and three-phase active rectifiers, the author selected interleaved Vienna rectifier to achieve extreme efficiency and avoid overheating problem. The operation principle of the interleaved Vienna rectifier is introduced, with particular attention paid to the circulating current generated by interleaving operation. The design procedure for achieving maximum efficiency is described. Finally, a prototype of the proposed converter is constructed, which achieves 99.26% efficiency at nominal load.

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Table of Contents

List of Figures ix

List of Tables xiii

Chapter 1. Introduction 1

1.1 More-electric Aircrafts Concept 1

1.2 Role of Active Front-end Converters in More-electric Aircrafts 3

1.3 Objectives of This Work 6

1.4 Organization of This Work 6

Chapter 2. Design and Comparison of the AFE Converter for Single-phase Input 8

2.1 Introduction of High Efficiency Single-phase PFC Topologies 9

2.2 Operation principle of Single-phase PFC Boost Converters 11

2.2.1 Two-level Semi-bridgeless PFC Rectifiers 13

2.2.2 Three-level Bridgeless PFC Rectifiers 14

2.2.3 Interleaved Converters 16

2.2.4 Modulation of the Single-phase PFC Converters 18

2.3 Loss Analysis and Calculation 27

2.3.1 Loss Analysis 28

2.3.2 MOSFET Switching Loss Modeling 30

2.3.3 Simulation-based Converter Loss Calculation 36
2.4 Efficiency-oriented Design Procedure 38
2.5 Converter Design Results 39
2.6 Efficiency (Loss) Evaluation and Comparison 43
2.6.1 Comparison between Two-level PFC Converters 43
2.6.2 Comparison between Three-level PFC Converters 44
2.6.3 Comparison among Two-level and Three-level Converters 44
Chapter 3. Design and Comparison of AFE Converters for Three-phase Input 46
3.1 Introduction of High Efficiency Three-phase Rectifiers 47
3.2 Operation principle 49
3.2.1 Two-level Boost Rectifier 49
3.2.2 Three-level NPC Rectifier 50
3.2.3 Vienna Rectifier 52
3.3 Loss Analysis and Calculation 54
3.3.1 Loss Analysis 55
3.3.2 Loss Calculation 57
3.4 Efficiency (loss) Comparison 58
Chapter 4. Design and Implementation of a Dual-Channel Interleaved Vienna Rectifier 62

4.1 Introduction of Interleaved Vienna Rectifiers 62

4.2 Operation Principles of the Dual-channel Interleaved Vienna Rectifier 63

4.3 Circulating Current Generation and Attenuation in Interleaved Converters 64

4.3.1 Generation Mechanism of Circulating Current in Interleaved Converters 64

4.3.2 Circulating Current Attenuation Method 66

4.3.3 Design and Implementation of Inter-phase Inductors 67

4.4 Converter Design Procedure, Loss Estimation and Implementation 72

4.4.1 Converter Design Procedure 72

4.4.2 Converter Loss Estimation 75

4.4.3 Converter Implementation 76

4.5 Experiments and Performance Evaluation 76

4.5.1 Constructed Converter Prototype 76

4.5.2 Converter Testing and Evaluation 77

Chapter 5. Summary 80

References 83

List of Figures

Fig. 1. Conventional aircraft power distribution architecture, P. W. Wheeler, J. Clare, A. Trentin, and S. Bozhko, "An Overview of the More Electrical Aircraft," *Proceedings of the Institution of Mechanical Engineers, Part G: Journal of Aerospace Engineering*, vol. 227, pp. 578-585, 2013., Used under fair use, 2015. 2

Fig. 2. MEA power distribution architecture, P. W. Wheeler, J. Clare, A. Trentin, and S. Bozhko, "An Overview of the More Electrical Aircraft," *Proceedings of the Institution of Mechanical Engineers, Part G: Journal of Aerospace Engineering*, vol. 227, pp. 578-585, 2013., Used under fair use, 2015..... 3

Fig. 3. (a) Conventional aircraft electrical power generation. (b) MEA electrical power generation. , P. W. Wheeler, J. Clare, A. Trentin, and S. Bozhko, "An Overview of the More Electrical Aircraft," *Proceedings of the Institution of Mechanical Engineers, Part G: Journal of Aerospace Engineering*, vol. 227, pp. 578-585, 2013., Used under fair use, 2015. 4

Fig. 4. Electrical power architecture of Boeing 787 Dreamliner, E. Lavopa, P. Zanchetta, M. Sumner, and F. Cupertino, "Real-Time Estimation of Fundamental Frequency and Harmonics for Active Shunt Power Filters in Aircraft Electrical Systems," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 2875–2884, 2009., Used under fair use, 2015. 5

Fig. 5. Two-level semi-bridgeless PFC boost rectifier 11

Fig. 6. Interleaved two-level semi-bridgeless PFC boost rectifier..... 12

Fig. 7. Three-level bridgeless PFC boost rectifier 12

Fig. 8 Interleaved three-level bridgeless PFC boost rectifier. 12

Fig. 9. Charging and discharging of boost inductor in positive cycle. (a) charging state. (b) discharging state..... 13

Fig. 10. Basic operation principle of boost-type PFC converter..... 14

Fig. 11. Charging and discharging states of three-level bridgeless PFC rectifier..... 16

Fig. 12. (a) Working principle of interleaved PFC converter. (b) Equivalent circuit of interleaved PFC converter. 17

Fig. 13. Carrier-based modulation scheme for two-level semi-bridgeless PFC boost rectifier.... 19

Fig. 14. Simulated waveforms of two-level semi-bridgeless PFC boost rectifier 19

Fig. 15. (a) Modulation of interleaved two-level semi-bridgeless boost rectifier when duty cycle is smaller than 0.5. (b) Modulation of interleaved two-level semi-bridgeless boost rectifier when duty cycle is larger than 0.5. 21

Fig. 16. Simulated waveforms of interleaved two-level semi-bridgeless PFC boost rectifier 21

Fig. 17. (a) Modulation of three-level bridgeless boost rectifier when duty cycle is smaller than 0.5. (b) Modulation of three-level bridgeless boost rectifier when duty cycle is larger than 0.5. 23

Fig. 18. Simulated waveforms of three-level semi-bridgeless PFC boost rectifier 26

Fig. 19. Carriers for the interleaved three-level bridgeless PFC rectifier..... 27

Fig. 20. Simulated waveforms of the interleaved three-level bridgeless PFC boost rectifier 27

Fig. 21. Switching states transitions and switch commutations when $V_{ac} < V_{out}/2$ and $V_{ac} > 0$.... 30

Fig. 22. Switching states transitions and switch commutations when $V_{ac} > V_{out}/2$ and $V_{ac} > 0$.... 30

Fig. 23. Circuit for MOSFET switching loss prediction..... 32

Fig. 24. Waveforms during turn-on procedure 32

Fig. 25. Input current waveform of two-level semi-bridgeless PFC boost converter within one switching cycle..... 37

Fig. 26. Simulation-based converter loss calculation process 37

Fig. 27. Efficiency-oriented design procedure..... 38

Fig. 28. Loss distribution and total loss of optimized PFC rectifiers 42

Fig. 29. Two-level boost rectifier 48

Fig. 30. Three-level NPC rectifier 48

Fig. 31. Vienna rectifier..... 49

Fig. 32. Space vectors two-level rectifier DPWM and clamping options. 50

Fig. 33. Space vectors of three-level rectifier DPWM and clamping options. 51

Fig. 34. Space vectors of DPWMA and clamping options. 54

Fig. 35. Space vectors of DPWMB and clamping options 54

Fig. 36. Commutation of three-level NPC rectifier. 57

Fig. 37. Efficiency-optimized design procedure for three-phase rectifiers. 58

Fig. 38. Loss distribution and comparison of three-phase rectifiers. 59

Fig. 39. Topology of dual-channel interleaved Vienna rectifier. 63

Fig. 40. Circulating current generation mechanism. 64

Fig. 41. Simulated current of each sub-converter, circulating current, and the corresponding voltage difference. 65

Fig. 42. (a) Coupling inductor and flux generated by common current (I_A/2). (b) Coupling inductor and flux generated by circulating current (I_{cir}). 67

Fig. 43. (a) Transformer-like equivalent circuit of inter-phase inductor. (b) T-shape equivalent circuit of inter-phase inductor. 68

Fig. 44. Relationship between modulation, phase leg output voltage and circulating current. 69

Fig. 45. (a) Waveforms without enough impedance in the circulating loop at high frequency. High frequency ringing can be observed on I_{diff} (the difference between I_{A1} and I_{A2}), I_{A1} and I_{A2}. (b) Waveforms with high impedance inserted at high frequency. I_{diff}, I_{A1} and I_{A2} are less distorted. 72

Fig. 46. Efficiency-oriented design procedure for a dual-channel interleaved Vienna rectifier... 73

Fig. 47. Relationship between switching frequency and boost inductance, inter-phase inductance, and minimized loss. 75

Fig. 48. Converter prototype of dual-channel interleaved Vienna rectifier. 77

Fig. 49. Experimental waveforms of converter prototype under nominal load. 77

Fig. 50. Calculated loss distribution of interleaved Vienna rectifier at nominal load 78

Fig. 51. Temperature distribution of the converter prototype. 79

List of Tables

TABLE I. Single-phase AFE Converter Targets and Specifications 8

TABLE II. Reported Efficiency of High Efficiency PFC Converters 9

TABLE III. Converter Specifications and Requirements 39

TABLE IV. Semiconductor Device Candidates 41

TABLE V. Optimized Designs of Evaluated Topologies 42

TABLE VI. Comparison of Loss per Device in Single-Phase Converters 43

TABLE VII. Three-phase AFE Converter Targets and Specifications 46

TABLE VIII. Three-phase Converter Specifications and Requirements 59

TABLE IX. Comparison of Loss per Device in Three-Phase Converters 60

TABLE X. Semiconductor Device Candidates for the Dual-Channel Interleaved Vienna Rectifier 74

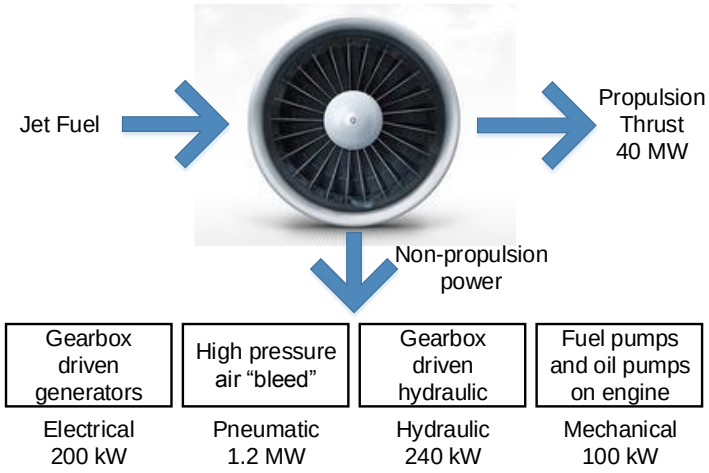
TABLE XI. Summary 82

Chapter 1. Introduction

1.1 More-electric Aircrafts Concept

Increasing fuel economy and reducing the environmental impact of airplanes have always been hot topics for aviation industry. Two major efforts have been taken to achieve these goals: increasing propulsive energy generation efficiency; reducing the take-off weight. More-electric aircraft (MEA) concept, namely, replacing pneumatic, hydraulic and mechanical equipment with its electrical equivalent, has been raised to help with reducing take-off weight. A study conducted by NASA [1] expects a 10% reduction in the take-off weight and a 9% reduction in fuel burn for a 200-seater aircraft by applying MEA technologies.

The MEA concept has gradually been accepted and implemented by aircraft manufactures. In early 2000, one of the three traditional hydraulic circuits on Airbus A380 is replaced with electrical circuits, which is considered as the first high power electricity appearance on commercial aircrafts. Meanwhile, the Boeing 787 Dreamliner has introduced electrical systems to replace pneumatic circuit and in the brakes [2]. The aircraft electrification has became the major trend for on board power distribution.



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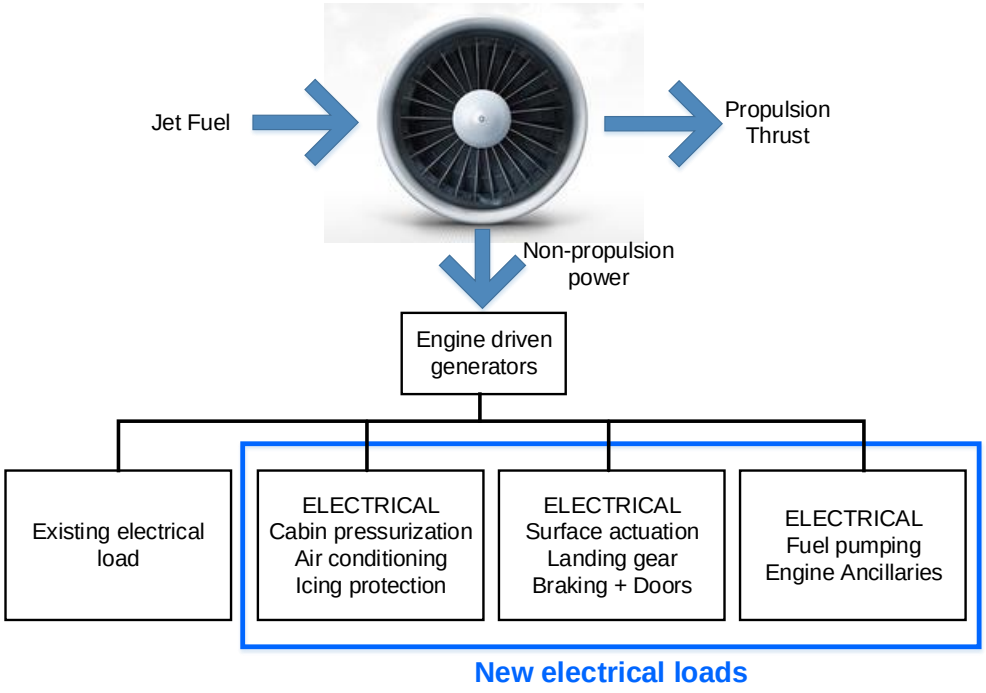
The conventional power distribution in an A330 /Boeing 777 size aircraft is shown in Fig. 1 , where the power generated by the turbine can be separated into two main parts: propulsion thrust and non-propulsion power. In a conventional design, main portion of the non-propulsive power is consumed by pneumatic systems (for cabin pressurization, air conditioning, etc.), hydraulic systems (for flight control, landing, etc.) and mechanical systems (for fuel pumps, oil pumps, etc.) [3].These systems are heavy and may require high cost on maintenance.



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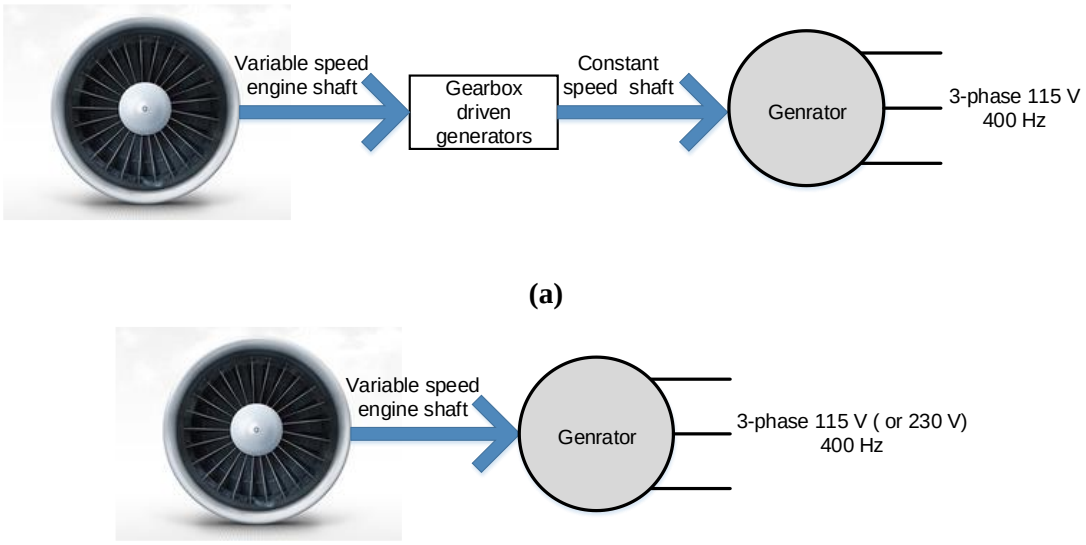
In a more-electric aircraft (shown in Fig. 2), all the non-propulsive power is expected to be consumed by electrical equipment, which considerably increases the electrical power demand. It is projected that, in a fully electrical A330 /Boeing 777 size aircraft, the total electrical power demand would be 1MW [3], which puts forward big challenges as well as great opportunities for electrical engineers.

1.2 Role of Active Front-end Converters in More-electric Aircrafts

With the increase in electrical power demand and changes in system configuration, advances in power electronics technologies are necessary to provide efficient and reliable interface between power generators and load. In a conventional aircraft, the generator is connected to the turbine via

a gearbox (Fig. 3 (a)). The gearbox transfers variable speed of the engine shaft to a constant speed shaft, which enabling the generation of 400 Hz, 115 V constant frequency three-phase power from generator feeding to the on-board electrical system. For a more-electric aircraft, the gearbox is eliminated and the generator is directed connected to the variable speed shaft of the turbine (Fig. 3 (b)), resulting in the generation of 360 Hz ~ 800 Hz, 115 V or 230 V variable frequency three-phase mains power. Some of the on-board loads, e.g. pumps, fans, are sensitive to power source frequency, which requires power electronics converters to interface different loads to the variable frequency mains.



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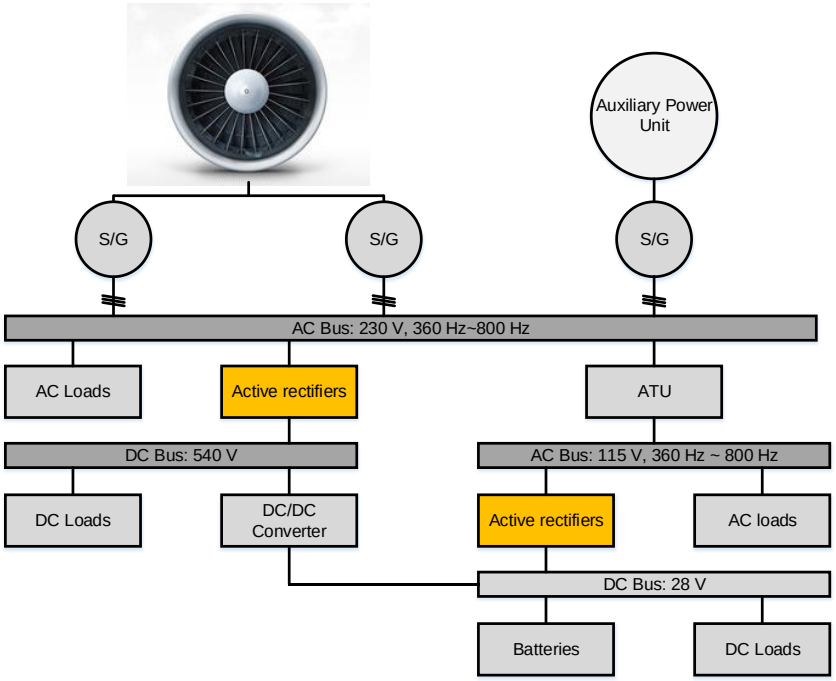
The electrical power architecture of a more-electric aircraft (Boeing 787) is shown in Fig. 4 in order to demonstrate the role of power electronics converters in more-electric aircrafts. In this configuration, active rectifiers (highlighted with yellow) that convert variable frequency AC

voltage into DC voltage are applied to serve as interface components connecting variable frequency AC buses to DC buses. For safety consideration, these active rectifiers are always required to provide galvanic isolation between the input and output. The most common converter configuration for achieving the requirements is a two-stage configuration with first stage active front-end converter providing regulated internal DC bus voltage and second stage isolated DC/DC converter providing galvanic isolation and regulated output DC voltage. Here, active front-end (AFE) converters, which are the main focus of this work, are one of the key components for interfacing the AC buses to DC buses. The function and specification of active front-end converters in more-electric aircrafts is not limited to first stage of bus interface. The active front-end converters may be applied to transfer single/three phase 115 V/230 V variable frequency source into regulated DC voltage, feeding to different types of load, e.g. electro hydrostatic actuators.



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Shunt Power Filters in Aircraft Electrical Systems," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 2875–2884, 2009., Used under fair use, 2015.

1.3 Objectives of This Work

Proper thermal management of power electronics converters are one of the key issue in improving converter reliability. For power electronics converters operating in aircrafts, where the ambient temperature can be as high as 70 ℃, it is even harder to keep all components in converters operating under proper temperature. There are two ways to avoid thermal induced device failure: using devices with higher permissible operation temperature; reducing temperature rise on devices. Either better thermal management design or device loss reduction is effective way to reduce device temperature rise. Moreover, it should be noted that, once device loss is below certain level, thermal management may not be a necessary. In other words, increasing converter efficiency not only increases fuel efficiency, but also reduces thermal management requirements.

The focus of this work is to achieve extreme converter efficiency through advanced converter topologies and design so that the converter can operate reliably under aircraft ambient (70 ℃ maximum) without active cooling. The target application is single phase and three-phase, 3 kW, active front-end converter fed by aircraft variable frequency AC voltage.

1.4 Organization of This Work

This work is organized as following: Chapter 1 introduces the concept of more-electric aircraft as and the role of active front-end in this concept, which serves as the background of this work.

Chapter 2 introduces the design and comparison of single-phase active rectifiers for this application, where the focus has been put on topology introduction, converter loss analysis and modeling, converter design and topology comparison. Chapter 3 extends the analysis developed for single-phase rectifiers to three phase rectifiers. Several three-phase topologies are analyzed and compared in this chapter in order to find out the proper topology to be built for this work. Chapter 4 focuses on the design, optimization and construction of an extreme efficiency interleaved Vienna rectifier, which is selected in Chapter 3. In this chapter, special attention has been paid to analyzing the generation and attenuation of circulating current in interleaved converters. Chapter 5 summarizes this work.

Chapter 2. Design and Comparison of the AFE Converter for Single-phase Input

This chapter presents a complete design and evaluation procedure for the single-phase AFE converter. TABLE I summarizes the targets and specifications of the converter, where high efficiency and power factor correction (PFC) are required. To begin, relevant literature was surveyed in order to narrow down techniques to help achieve high efficiency and a high power factor. Several topologies are considered based on the selected techniques. In order to find the most efficient topology, analytical methods for loss calculation are described, based on which design and optimization procedures for achieving maximum efficiency are proposed. With these methods, for each topology, the design that achieves the highest efficiency can be found analytically, resulting in the discovery of the best topology and design for this work.

TABLE I. SINGLE-PHASE AFE CONVERTER TARGETS AND SPECIFICATIONS

Items	Target/Specification
Input Voltage	Single phase 230 Vac
Input Frequency	360 Hz ~ 800 Hz
Output Voltage	TBD
Output Power	3 kW
Maximum Ambient Temperature	70 ℃
Efficiency	Higher than 99%
Cooling	Free Convection Air-Cooling
Power Quality Standard	DO-160F
Power Factor	Higher than 0.99

2.1 Introduction of High Efficiency Single-phase PFC Topologies

To fulfill the requirements of this work, it is necessary to consider not only efficiency but also input power factor correction characteristics. A survey of relevant literature was conducted in order to find PFC topologies that have the potential to achieve high efficiency. TABLE II summarizes the topologies, featured techniques, and their reported peak efficiency. Among the topologies, boost PFC converters achieve the highest efficiency. In terms of PFC characteristics, the theoretical PFC ability of buck-type, boost-type and buck-boost-type converters are analyzed in [15]. It is claimed that boost PFC converters are capable of achieving a power factor close to one [15]. Therefore, in this work, boost PFC converters are considered. To improve the efficiency of front-end PFC

TABLE II. REPORTED EFFICIENCY OF HIGH EFFICIENCY PFC CONVERTERS

Topology	Power (W)	Efficiency (Peak)	Features	Ref.
Buck PFC	100	97.5%	ZVS	[4]
	700	97%	Bridgeless	[5]
	100	97%	Burst Mode	[6]
Boost PFC	3300	99.1%	Bridgeless; Interleaved	[7]
	3300	99.3%	Resonant Transition Mode	[8]
	1200	98.9%	Bridgeless; Interleaved	[9]
	1000	98.4%	Three-level; Bridgeless	[10]
Flyback PFC	90	94%	Synchronous Rectification	[11]
	100	96%		[12]
Cuk PFC	150	95%	Bridgeless	[13]
Sepic PFC	130	95%	Bridgeless	[14]

converters for medium power applications such as telecom, electric aircraft, and electric vehicles, the industry has begun to look into bridgeless PFC converters due to their efficiency increase brought about by the elimination of one diode in conduction loop [16]. Several papers have been published conducting efficiency evaluations of numerous single-phase PFC converters [17, 18]. Ref. [17] has experimentally proven that, under the same conditions, bridgeless PFC boost rectifiers are more efficient than conventional PFC boost rectifiers. This work also claims that, among the many variations of bridgeless PFCs, when considering practical issues such as EMI filtering, gate-drives, and possible working mode (CCM, DCM or critical mode), one of the most practical topologies is the so-called semi-bridgeless PFC boost rectifier with diode clamping, which is shown in Fig. 1(a). Ref. [7, 8] adds that, to achieve higher efficiency, the clamping diode can be replaced by MOSFETs or capacitors. A 3.2 kW paralleled semi-bridgeless PFC boost rectifier with capacitor clamping achieving 99.3 % peak efficiency was presented accordingly in [7, 8]. To further expand limits, the interleaved two-level semi-bridgeless PFC boost rectifier was proposed in [9, 18], as it is believed to have the potential to achieve higher efficiency than the non-paralleled semi-bridgeless PFC boost rectifier.

Along with two-level converters, another group of single-phase PFC boost rectifiers – three-level boost rectifiers – are evaluated in this work. The three-level boost rectifier with a diode bridge is presented in [19], showing an improvement in efficiency due to the use of lower voltage rating devices. However, the use of the diode bridge degrades the total efficiency of the three-level converter. To solve this problem, a three-level bridgeless PFC boost rectifier is proposed in [20]. Though it is not called “bridgeless” in [20], the proposed topology is the bridgeless version of the

conventional topology. In this work, an interleaved three-level bridgeless PFC boost rectifier are proposed and evaluated to further increase the efficiency limits of single-phase PFC circuits.

2.2 Operation principle of Single-phase PFC Boost Converters

The topologies to be evaluated in this chapter are as follows: two-level semi-bridgeless PFC boost rectifier (2LPFC) with clamping (shown in Fig. 5); interleaved two-level semi-bridgeless PFC boost rectifier (I2LPFC) with clamping (shown in Fig. 6); three-level bridgeless PFC boost rectifier (3LPFC) (shown in Fig. 7); and interleaved three-level bridgeless PFC boost rectifier (I3LPFC) (shown in Fig. 8).

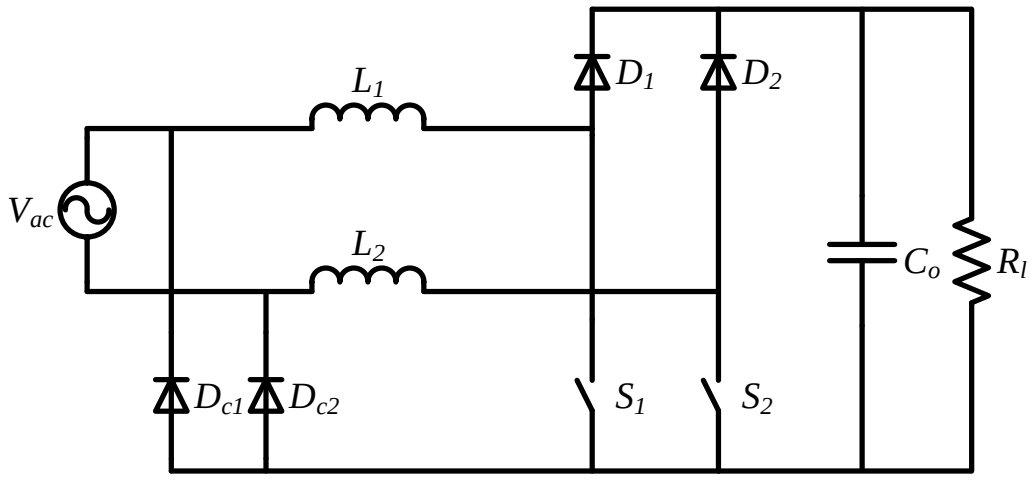


Fig. 5. Two-level semi-bridgeless PFC boost rectifier

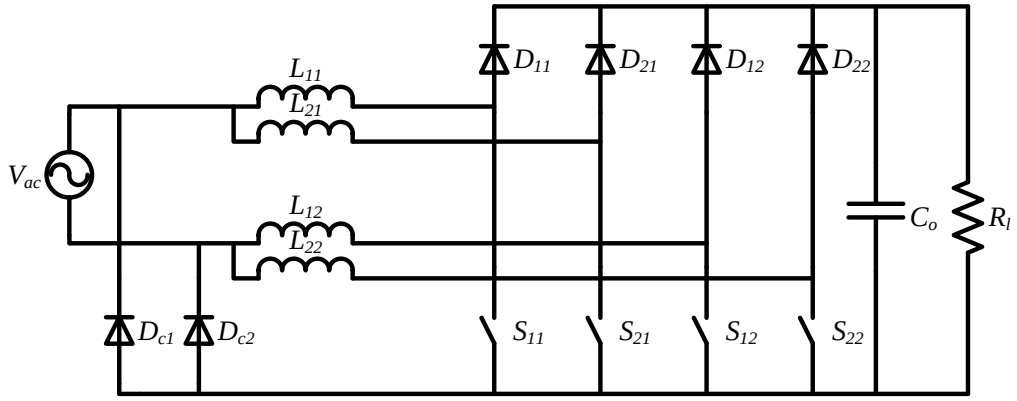


Fig. 6. Interleaved two-level semi-bridgeless PFC boost rectifier

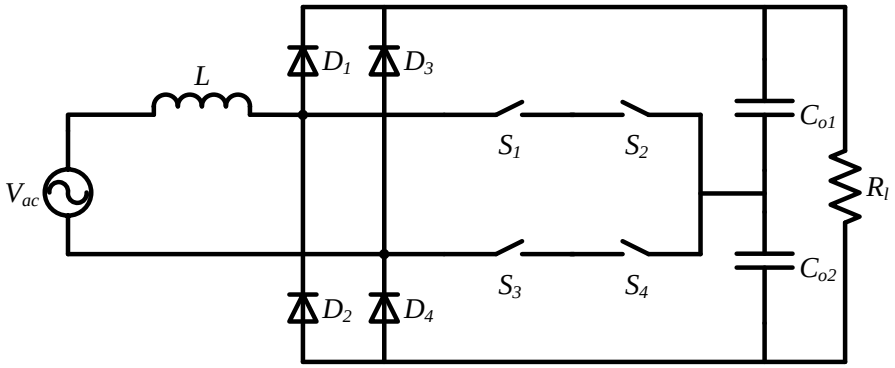


Fig. 7. Three-level bridgeless PFC boost rectifier

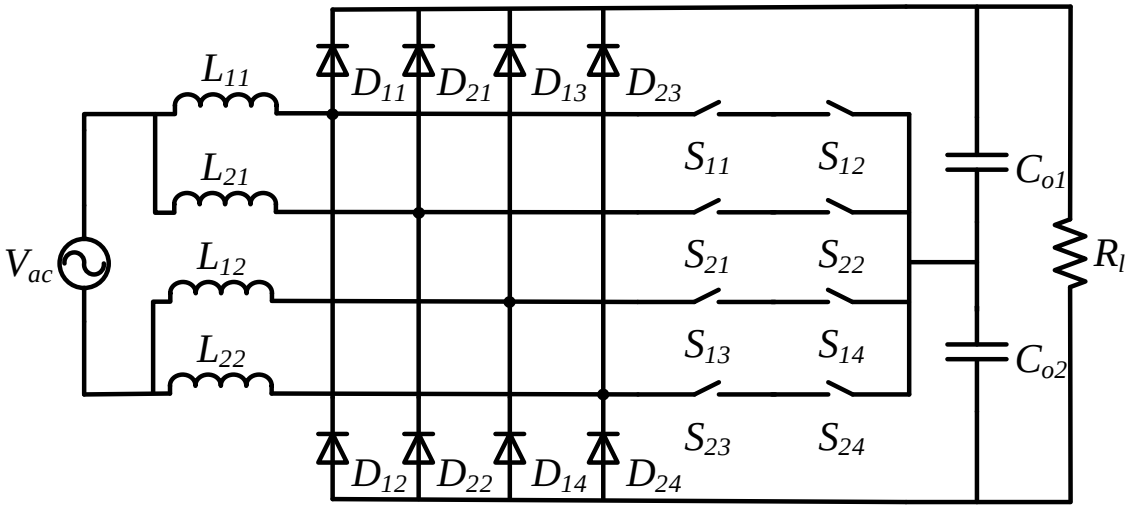


Fig. 8 Interleaved three-level bridgeless PFC boost rectifier.

2.2.1 *Two-level Semi-bridgeless PFC Rectifiers*

The topology of the two-level semi-bridgeless PFC rectifier is shown in Fig. 6. Herein, L_1, D_1 and S_1 form a boost converter that operates in the positive line cycle, and L_2, D_2, S_2 form a boost converter that operates in the negative line cycle. D_{c1} and D_{c2} serve as clamping diodes that clamp the negative rail of the DC bus back to the source, which helps reduce common mode noise [17].

The PFC characteristic is achieved by shaping the current in the boost inductors, namely L_1 and L_2. For example, in the positive line cycle where D_{c2} bypasses L_2, the current in L_1 will increase (charging the boost inductor) when S_1 is on (shown in Fig. 9 (a)) and vice versa (shown in Fig. 9 (b)). In the negative line cycle, S_2 shapes the current in L_2.

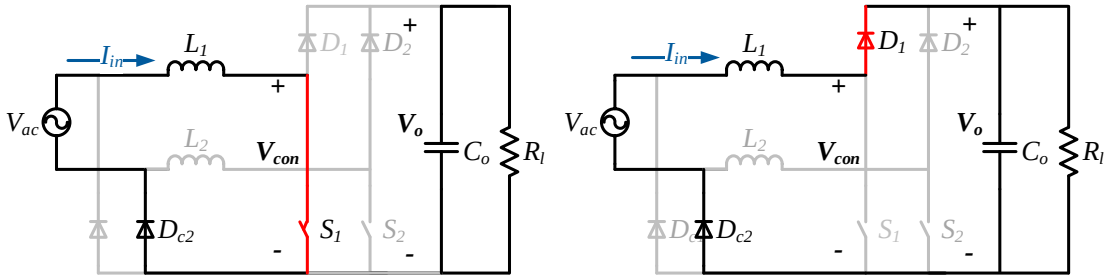


Fig. 9. Charging and discharging of boost inductor in positive cycle. (a) charging state. (b) discharging state.

In other words, the output of the phase legs (S_1, D_1 or S_2, D_2) can be modeled as a voltage source (shown as $\underline{V_{con}}$ in Fig. 10). The equivalent circuit is shown in Fig. 10. The amplitude and displacement angle of V_{con} can be controlled by sequencing the its two output states: $V_{con} = V_o$ (in positive half cycle, shown in Fig. 9 (b)) and $V_{con} = 0$ (shown in Fig. 9 (a)). By properly controlling the amplitude and displacement angle of the voltage source V_{con}, the current (I_{in}) in the boost inductor (L_{boost}) can be correctly shaped to achieve unity power factor.

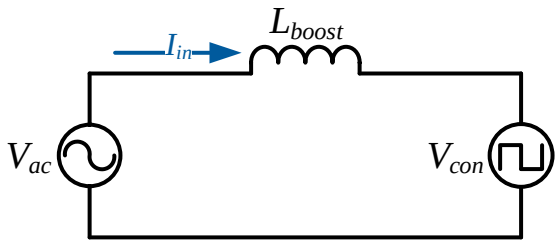


Fig. 10. Basic operation principle of boost-type PFC converter

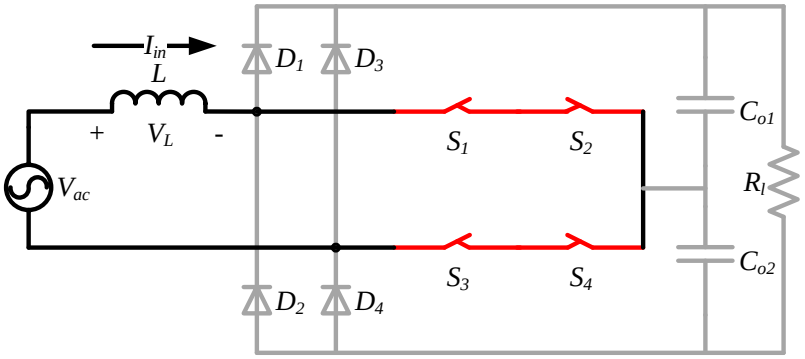
2.2.2 Three-level Bridgeless PFC Rectifiers

The topology of three-level bridgeless PFC rectifier is shown in Fig. 7. Herein, the output DC bus is split by two capacitors (C_{o1} and C_{o2}), allowing the use of low voltage devices. In this topology, S_1, S_2, D_1, and D_2 form one phase leg, and other devices form the other. S_1 and S_2 are connected in an anti-series manner, forming a four-quadrant switch. All the diodes (D_1, D_2, D_3, and D_4) should be capable of blocking the whole DC bus voltage while voltage stress on all the active switches (S_1, S_2, S_3 and S_4) is half of the DC bus voltage. S_1 and S_2 are driven by the same gate signal, as are S_3 and S_4.

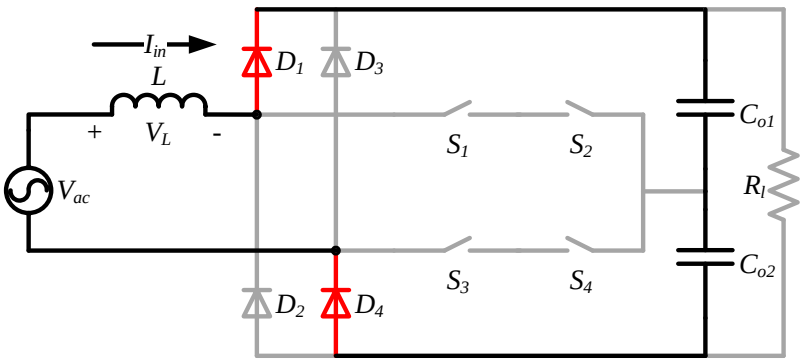
Similar to that of its two-level counterpart, PFC operation, i.e. input current shaping, is achieved by controlling the charging and discharging of boost inductor L. For three-level converters, inductor charging and discharging is more interesting due to the existence of the split DC bus. Possible charging and discharging states for positive line cycle (V_{ac}>0) are shown in Fig. 11. At any time, charging of the inductor can be achieved with S_1, S_2, S_3, and S_4 on (as shown in Fig. 11 (a)). At this state, the voltage applied to L is V_{ac}, which is positive. At any time, with S_1, S_2, S_3, and S_4 off (as shown in Fig. 11 (b)), the inductor is discharged. Discharging of the inductor can also be achieved either with S_1, S_2 on and S_3, S_4 off (shown as the blue path in Fig. 11 (c)) or with S_1, S_2 off and S_3, S_4 on (shown as the red path in Fig. 11 (c)) when V_{ac} is smaller than V_{out}/2. At these

states, voltage applied on L is V_{ac}-V_{out}/2, which is negative. When V_{ac} is larger than V_{out}/2, charging of the inductor can also be the same as the discharging states when V_{ac} is smaller than V_{out}/2 (as shown in Fig. 11 (c)). It should be noted that two charging (discharging) paths shown in Fig. 11 (c) will result in middle point unbalance because the current in the path connected with the middle point is not zero in these states. To keep the middle point voltage of the DC bus at V_{out}/2, the two states should be applied alternately.

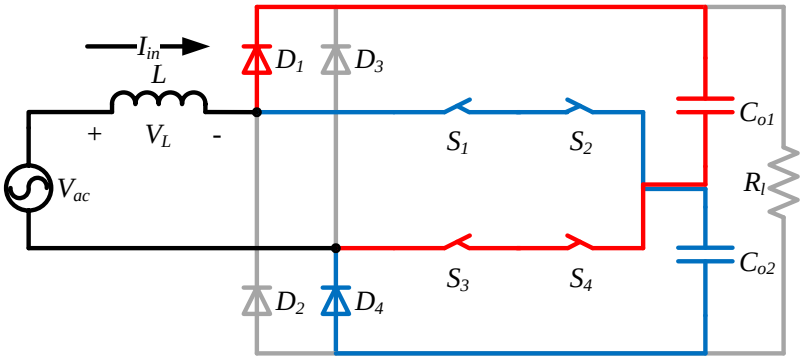
Similar principle introduced in Fig. 10 can also be used to explain the operation principle of three-level PFC converter. There are three possible states of V_{con} in a three-level converter, they are: V_o (shown in Fig. 11(a)), V_o/2 (shown in Fig. 11(b)) and 0 (shown in Fig. 11(c)). By properly sequencing these three states, unity power factor can be achieved.



(a) charging state



(b) discharging state



(c) discharging state when $V_{ac}<V_{out}/2$, charging state when $V_{ac}>V_{out}/2$

Fig. 11. Charging and discharging states of three-level bridgeless PFC rectifier

2.2.3 Interleaved Converters

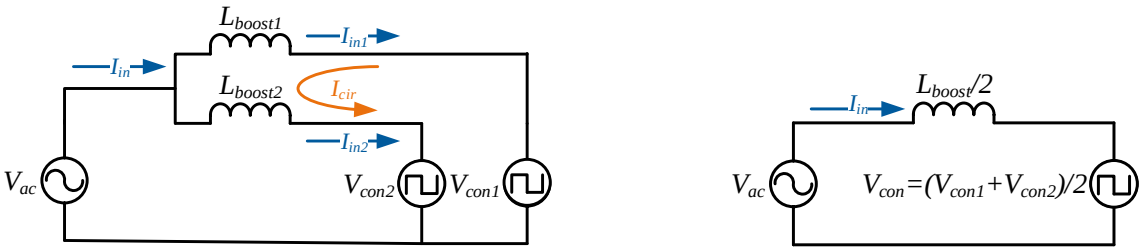
For the interleaved two-level converter shown in Fig. 6, L_{11}, L_{12}, S_{11}, S_{12}, D_{11}, and D_{12} form a sub-converter that can operate independently as a two-level semi-bridgeless PFC boost rectifier, as was previously described. The remaining components form the other sub-converter. The working principle of the interleaved converter is depicted in Fig. 12 (a) where the two sub-converters are modeled as two voltage sources V_{con1} and V_{con2}. The relationship between V_{con1}, V_{con2} and input current I_{in} can be expressed as:

$$I_{in} = I_{in1} + I_{in2} = L_{boost1}\frac{d(V_{ac} - V_{con1})}{dt} + L_{boost2}\frac{d(V_{ac} - V_{con2})}{dt} \quad (1)$$

Assuming that $L_{boost1} = L_{boost2} = L_{boost}$, we can get:

$$I_{in} = L_{boost}\frac{d(2V_{ac} - V_{con1} - V_{con2})}{dt} = \frac{L_{boost}}{2}\frac{d(V_{ac} - \frac{V_{con1} + V_{con2}}{2})}{dt} \quad (2)$$

Based on (2), the equivalent circuit of an interleaved PFC converter can be drawn as Fig. 12 (b). Here, the circuit structure is the same as equivalent circuit of non-interleaved two-level PFC converters introduced in 2.2.1. The equivalent output states of the converter phase legs are: V_o, $V_o/2$ and 0, where one additional output state ($V_o/2$) can be generated by interleaving two two-level converters. It is worth noting that the available output states of an interleaved two-level PFC converter is the same as that of three-level PFC converter. Similarly to the other converters introduced previously, unity power factor is achieved by properly sequencing the available output states.



(a) **(b)**

Fig. 12. (a) Working principle of interleaved PFC converter. (b) Equivalent circuit of interleaved PFC converter.

For an interleaved three-level PFC converter, the operation is a combination of interleaved two-level PFC converter and three-level PFC converter. Similar equivalent circuit as shown in Fig. 12 (b) can be drawn. The available output states are: V_o, $3V_o/4$, $V_o/2$, $V_o/4$ and 0 because each sub-converter (three-level PFC converter) has three output states (as introduced in 2.2.2).

2.2.4 Modulation of the Single-phase PFC Converters

Modulation scheme, together with control system, of a converter determines how the timing and sequence of the switching states. The modulation scheme for all the topologies studied in this work will be introduced in this part.

To begin, modulation of the two-level semi-bridgeless PFC boost rectifier is analyzed (depicted in Fig. 13). In Fig. 13, the orange triangular waveform is the carrier for S_1 and S_2 (they are gated with the same signal), and the red line is the duty cycle generated by the controller. It should be noted that the carrier frequency is the same as the switching frequency and input current ripple frequency in a two-level PFC converter. We assume that, within one switching cycle, the input voltage is constant, and its value is V_{ac}. Because the converter is fundamentally a boost converter, its duty cycle d_{2L} within this switching cycle should satisfy the following,

$$d_{2L} = \frac{V_{out} - V_{ac}}{V_{out}} \tag{3}$$

where V_{out} is the output voltage. A proper gate signal (green waveform) can be generated by comparing the carrier with the duty cycle (the gate signal becomes high when the carrier is smaller, and turns low when the carrier is larger). The resulting input current waveform is depicted as blue waveform in Fig. 13.

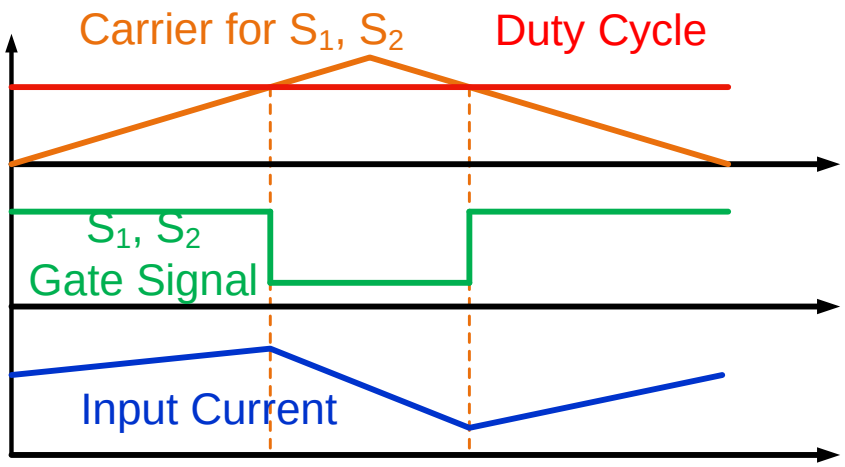


Fig. 13. Carrier-based modulation scheme for two-level semi-bridgeless PFC boost rectifier

The conventional controller for boost PFC rectifiers with diode bridges is applied to the bridgeless version. Applying the modulation shown in Fig. 13, simulation of of two-level semi-bridgeless PFC rectifier can be ran. The simulated operation waveforms are shown in Fig. 14, where the input current is in phase with input voltage, achieving unity power factor conversion.

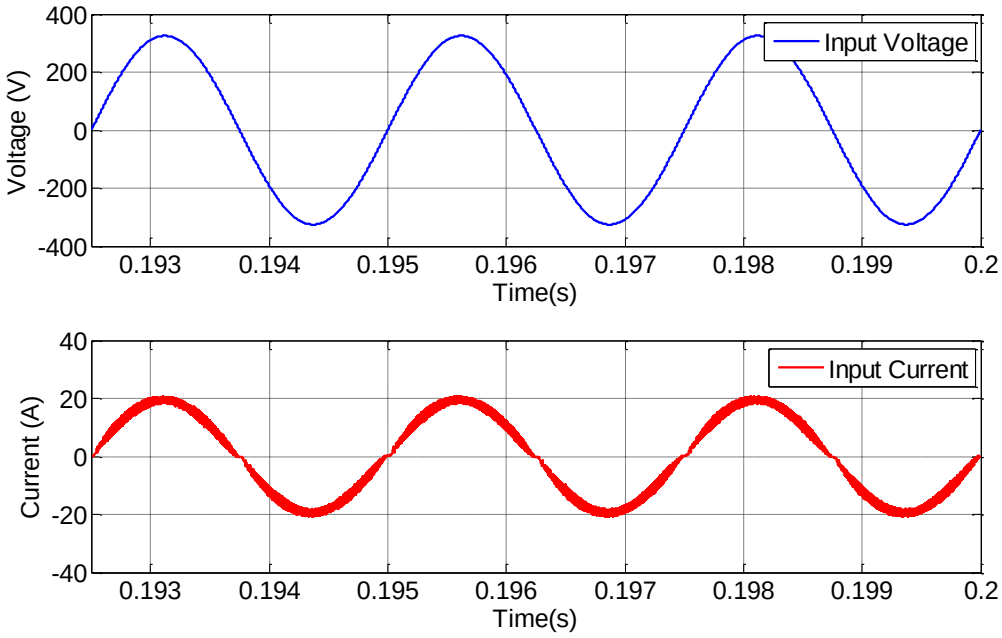
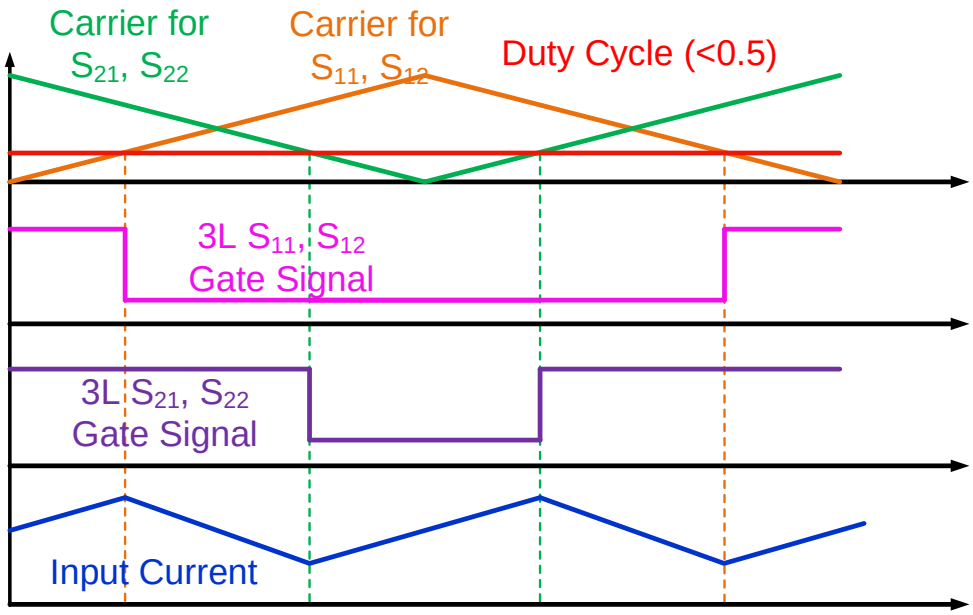
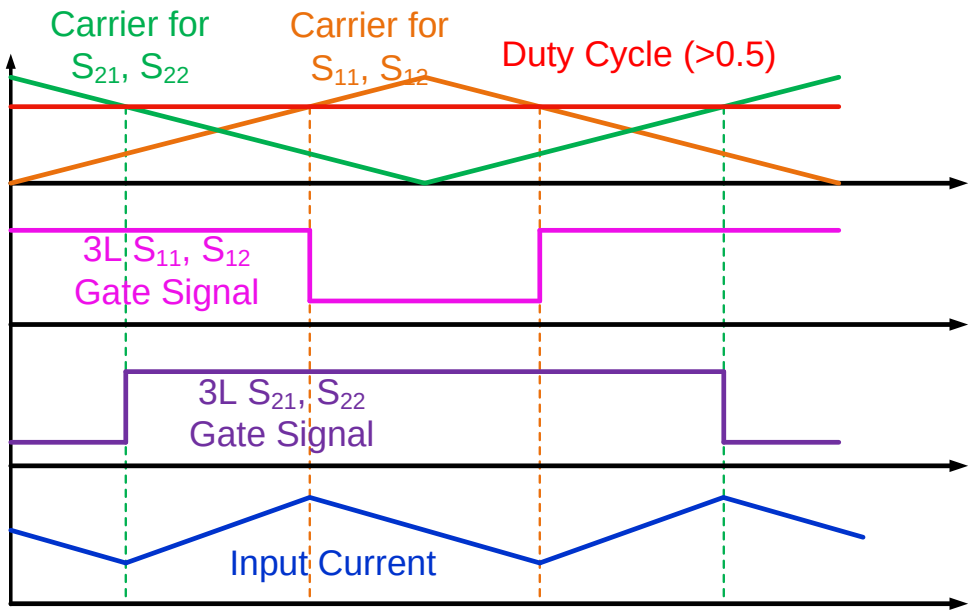


Fig. 14. Simulated waveforms of two-level semi-bridgeless PFC boost rectifier

For the interleaved two-level semi-bridgeless boost PFC rectifier, the modulation of each sub-converter is the same as non-interleaved two-level converter. In this study, the two sub-converters operate 180 ºout of phase, which helps smoothing of the input current. To operate the converter in an interleaved manner, a 180 º phase shift is introduced between the carriers for the two sub-converters (shown in Fig. 15). The simulated operation waveforms of an interleaved two-level semi-bridgeless PFC boost rectifier are shown in Fig. 16. Due to converter interleaving, the whole converter switches twice in one carrier period. Therefore, the carrier frequency should be one-half of the desired input current ripple frequency.



(a)



(b)

Fig. 15. (a) Modulation of interleaved two-level semi-bridgeless boost rectifier when duty cycle is smaller than 0.5. (b) Modulation of interleaved two-level semi-bridgeless boost rectifier when duty cycle is larger than 0.5.

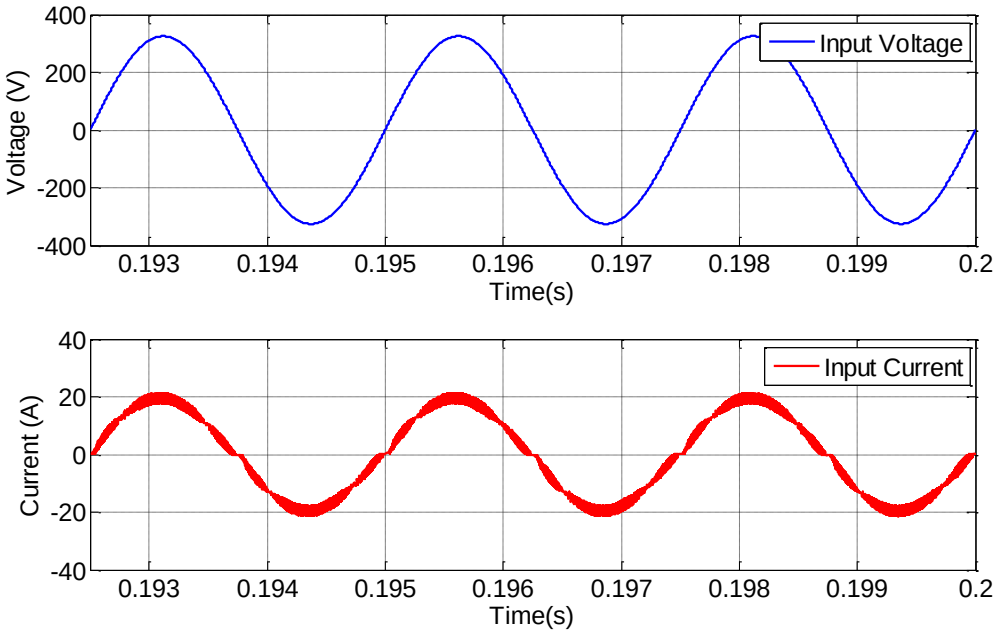
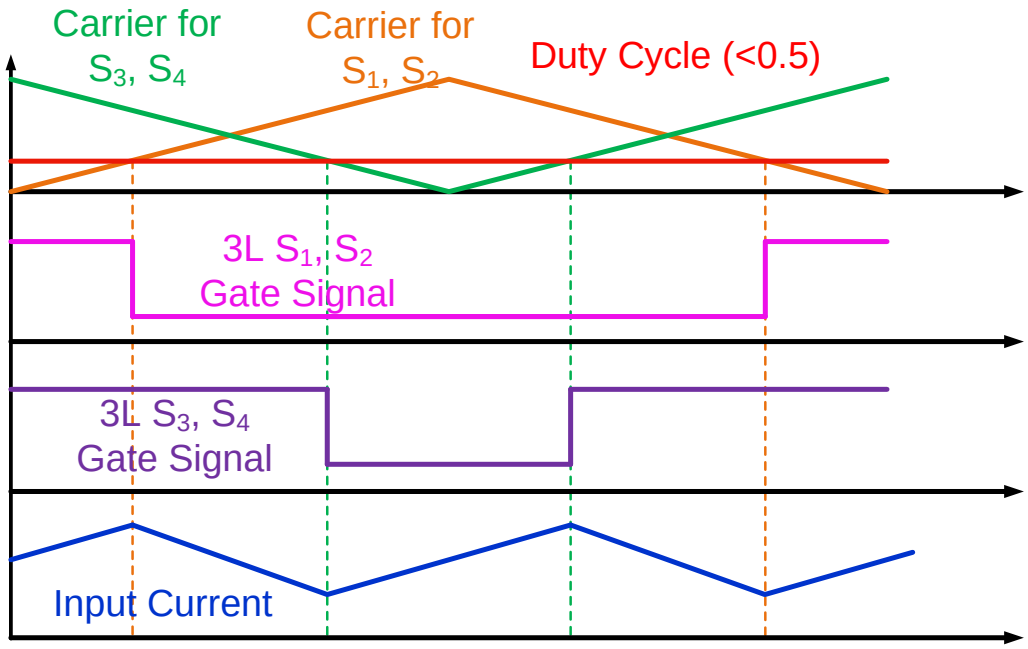


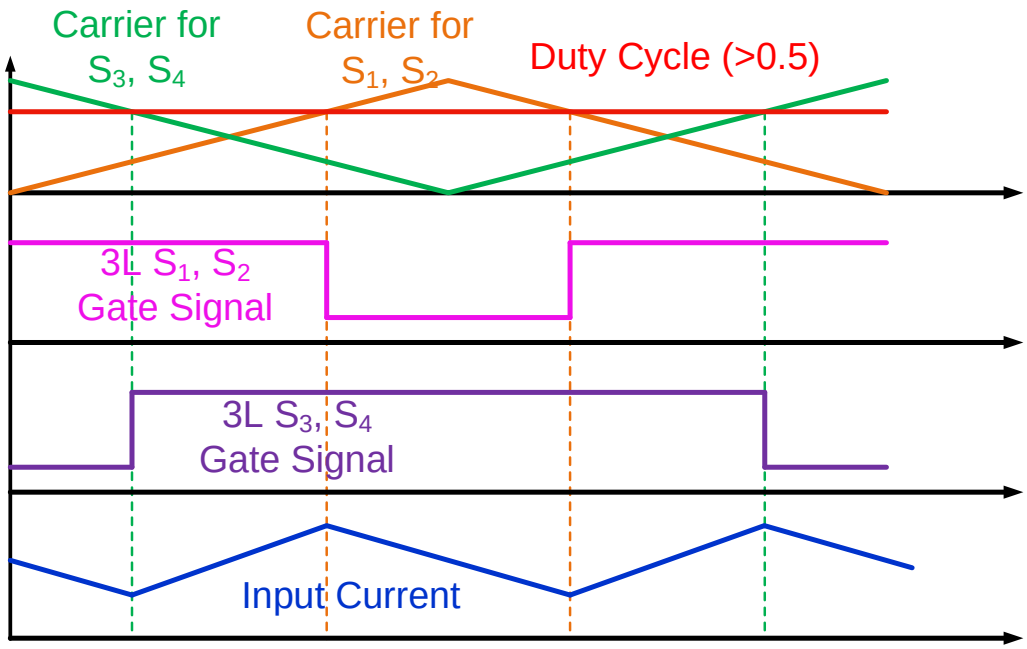
Fig. 16. Simulated waveforms of interleaved two-level semi-bridgeless PFC boost rectifier

To generate proper gate signals for a three-level bridgeless PFC rectifier, this work proposed a carrier-based modulation scheme that borrows the modulation concept from the interleaved two-level PFC converter and utilizes the same controller designed for conventional PFC boost rectifiers.

Noticing the similarity between phase leg output states between interleaved two-level PFC converter and three-level PFC converter (introduced in 2.2.3), for the three-level bridgeless PFC rectifier, two carriers with a 180 ^{o} phase shift between them (the same as interleaved two-level converter) are introduced. Fig. 17 depicts the carrier-based modulation scheme for the three-level bridgeless PFC rectifier, where the orange triangular waveform is the carrier for S_1 and S_2 and the green triangular waveform is the carrier for S_3 and S_4. The red line is the duty cycle generated in the same way as the two-level PFC boost rectifier. I.e. the duty cycle value d_{3L} is $(V_{out} - V_{ac}) / V_{out}$ assuming that input voltage V_{ac} is constant within one duty cycle. This allows the three-level PFC rectifiers to utilize the controller designed for two-level PFC rectifiers. Moreover, it should be noted that, within one carrier period, each phase leg switches once; i.e. the converter switches twice in one carrier period. Therefore, like interleaved two-level converter, the carrier frequency should be one-half of the desired input current ripple frequency.



(a)



(b)

Fig. 17. (a) Modulation of three-level bridgeless boost rectifier when duty cycle is smaller than 0.5. (b) Modulation of three-level bridgeless boost rectifier when duty cycle is larger than 0.5.

When $V_{ac} < V_{out}/2$ ($d_{3L} > 0.5$), the gate signals for S_1, S_2 and S_3, S_4, and the resulting current waveform are shown in Fig. 17 (a). Herein, the state where all the switches are on corresponds to the converter state depicted in Fig. 11 (a) where the boost inductor is being charged and voltage applied on the inductor is V_{ac}. The other state where one set of switches are on and the others are off corresponds to the converter state depicted in Fig. 11 (c) where the boost inductor is being discharged and voltage applied on the inductor is $V_{ac} - V_{out}/2$.

When $V_{ac} > V_{out}/2$ ($d_{3L} > 0.5$), the gate signals for S_1, S_2 and S_3, S_4 and the resulting current waveform are shown in Fig. 17 (b). Here, the state where all the switches are off corresponds to the converter state depicted in Fig. 11 (b), where the boost inductor is being discharged and voltage applied to the inductor is $V_{ac} - V_{out}$. The other state, where one set of switches are on and the others are off, corresponds to the converter state depicted in Fig. 11 (c) where the boost inductor is being charged, and voltage applied to the inductor is $V_{ac} - V_{out}/2$.

To verify the validity of the proposed modulation scheme, the inductor volt-sec balance should be proven. When $V_{ac} < V_{out}/2$ ($d_{3L} > 0.5$), assuming that input voltage is constant within one switching cycle, based on Fig. 17 (a), the total inductor charging time $T_{charge,1}$ is:

$$T_{charge,1} = [1-2(1-D_{3L})]T_s = [1-2(1-\frac{V_{out}-V_{ac}}{V_{out}})]T_s = \frac{V_{out}-2V_{ac}}{V_{out}}T_s \quad (4)$$

where D_{3L} is the duty cycle in this switching cycle and T_s is switching period. The total inductor discharging time $T_{charge,2}$ is:

$$T_{discharge,1} = 2(1-D_{3L})T_s = 2(1-\frac{V_{out}-V_{ac}}{V_{out}})T_s = \frac{2V_{ac}}{V_{out}}T_s \quad (5)$$

The total charging volt-sec is:

$$V_{ac}T_{charge,1} = \frac{V_{ac}V_{out} - 2V_{ac}^{\ 2}}{V_{out}}T_s \tag{6}$$

The total discharging volt-sec is:

$$(V_{ac} - \frac{V_{out}}{2})T_{discharge,1} = (V_{ac} - \frac{V_{out}}{2})\frac{2V_{ac}}{V_{out}}T_s = \frac{2V_{ac}^{\ 2} - V_{ac}V_{out}}{V_{out}}T_s \tag{7}$$

It can be easily verified that:

$$V_{ac}T_{charge,1} + (V_{ac} - \frac{V_{out}}{2})T_{discharge,1} = 0 \tag{8}$$

Therefore, the inductor volt-sec balance is proven when $V_{ac} < V_{out}/2$ ($d_{3L} > 0.5$).

When $V_{ac} > V_{out}/2$ ($d_{3L} < 0.5$), let $T_{charge,2}$ and $T_{discharge,2}$ be the total inductor charging and discharging times respectively. Then the inductor volt-sec balance can also be verified as follows:

$$(V_{ac} - \frac{V_{out}}{2})T_{charge,2} + V_{out}T_{discharge,2} = (V_{ac} - \frac{V_{out}}{2})\frac{2(V_{out} - V_{ac})}{V_{out}}T_s + (V_{ac} - V_{out})[1 - \frac{2(V_{out} - V_{ac})}{V_{out}}]T_s = 0 \tag{9}$$

Thus, the validity of the proposed modulation scheme is mathematically verified.

A simulation model based on the proposed modulation scheme and a controller built for the three-level PFC rectifier is also created in order to verify the validity of the topology and modulation scheme. The simulated waveforms are shown in Fig. 18, where input current is correctly shaped.

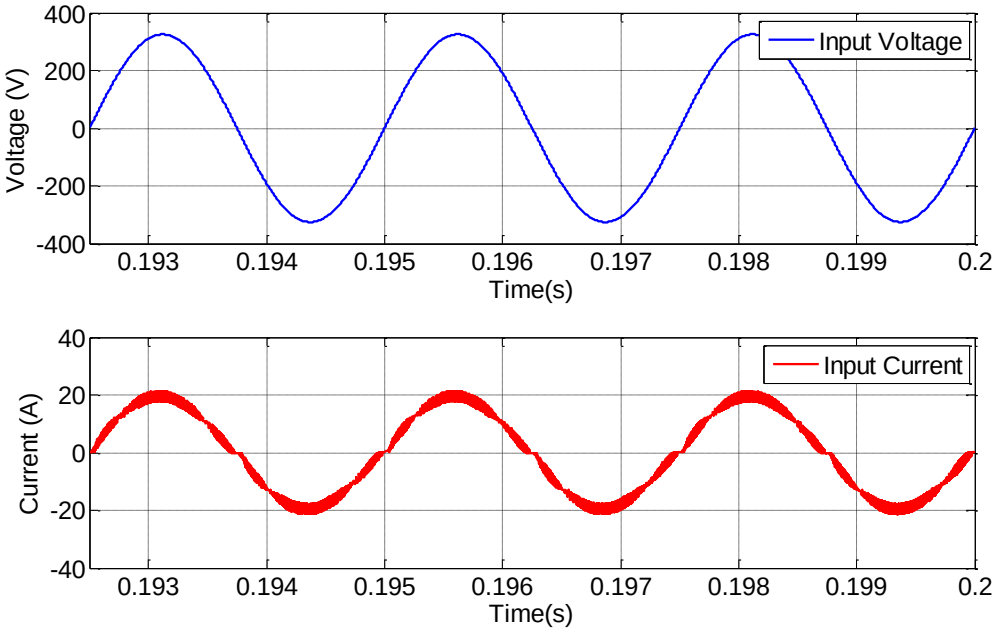


Fig. 18. Simulated waveforms of three-level semi-bridgeless PFC boost rectifier

For the interleaved three-level converter shown in Fig. 8, L_1, S_{11}, S_{12}, S_{13}, S_{14}, D_{11}, D_{12}, D_{13}, and D_{14} form a sub-converter that can operate independently as a three-level bridgeless PFC rectifier, with the remaining devices forming the other. As previously described, two carriers with a180 º phase shift are needed to modulate a single three-level converter. To operate the two sub-converters in an interleaved manner, four carriers with a 90 ºphase shift are applied (shown in Fig. 19). Due to the combination of converter interleaving and three-level operation, the interleaved three-level bridgeless PFC rectifier switches four times in one carrier period. Thus, the carrier frequency should be one-fourth of the desired switching frequency (input current ripple frequency). Simulated waveforms of the interleaved three-level bridgeless PFC rectifier are shown in Fig. 20 where the validity of the topology and modulation scheme is proven.

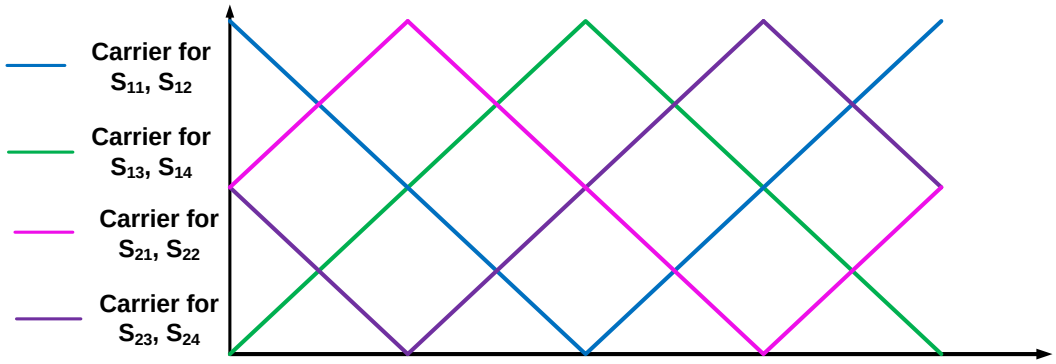


Fig. 19. Carriers for the interleaved three-level bridgeless PFC rectifier

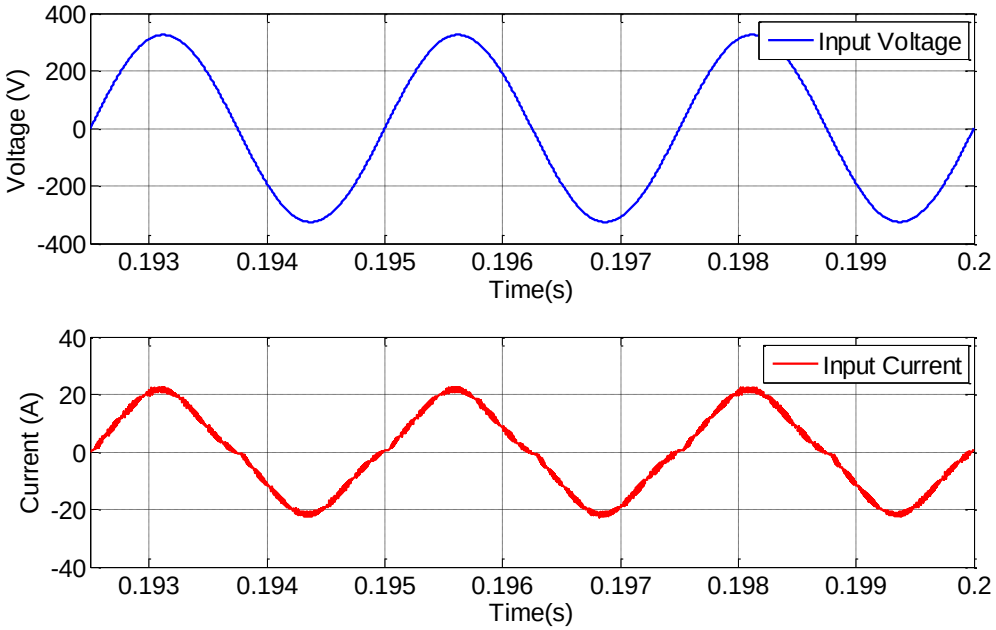


Fig. 20. Simulated waveforms of the interleaved three-level bridgeless PFC boost rectifier

2.3 Loss Analysis and Calculation

In this section, complete loss analysis and analytical loss calculation methods for previously introduced topologies are described, serving as the fundamentals of converter design and evaluation.

2.3.1 Loss Analysis

Converter loss mainly comes from conduction loss, inductor core loss, and switching loss.

Conduction loss is directly related to device resistance or forward voltage. With the knowledge of device conduction characteristics and current through a certain device, conduction loss can be calculated correspondingly. In this work, for active switches, MOSFETs are considered because of their ohmic conduction characteristics, which leads to smaller conduction loss under the target specifications.

Core loss occurs when magnetization of the inductor core changes. With the knowledge of flux density change and core material characteristics, core loss can be calculated using the Steinmetz equation [21].

Switching loss takes place when the current in one switch commutates to the other. For two-level converters, the commutation always takes place between the MOSFET and the diode connected to its drain, e.g. S_1 and D_1 in Fig. 5. For three-level converters, the situation is more complicated due to the existence of multiple switching states. When the converter operates in a positive line cycle and $V_{ac} < V_{out}/2$ (duty cycle < 0.5), as modulated by the proposed modulation scheme, the converter will transition sequentially among the states, as shown in

Fig. 21. When transiting from state 1 to state 2, S_1 and S_2 will be turned off. The load current commutates from S_1, S_2 to D_1. In state 2, voltage applied to the S_1, S_2 branch is half of the DC bus voltage. If S_1 and S_2 are connected in a common-source configuration, the voltage will be blocked by S_1. If they are connected in a common-drain configuration, S_2 will block the voltage. Therefore, when transiting from state 1 to state 2, commutation will take place between S_1 and D_1 (or S_2 and

D_1, as determined by the connection configuration). It should be noted that, during the commutation, voltage applied on D_2 changes from half the DC bus voltage to the whole DC bus voltage, which may result in addional capacitive charge loss. The transition from state 2 to state 3 is an inversion of the transition from state 1 to state 2. Thus, the devices involved in the commutation are the same. Similarly, commutation will take place between S_4, D_4 (common-source configuration) or S_3, D_4 (common-drain configuration) when transiting from state 3 to state 4 and from state 4 to state 1. When the converter operates in a positive line cycle and $V_{ac} > V_{out}/2$ (duty cycle > 0.5), the switching states are shown in

Fig. 22. The mechanism is similar to that described in the previous case, and for brevity, is not described again here. It can be seen here that commutations in three-level bridgeless PFC rectifiers always take place between one diode and one active switch, which is similar to what occurs in two-level PFC rectifiers. It is worth noting that, for three-level rectifiers, commutation voltage (voltage blocked by the diode or active switch during commutation) is half of the DC bus voltage while it is full DC voltage for two-level rectifiers.

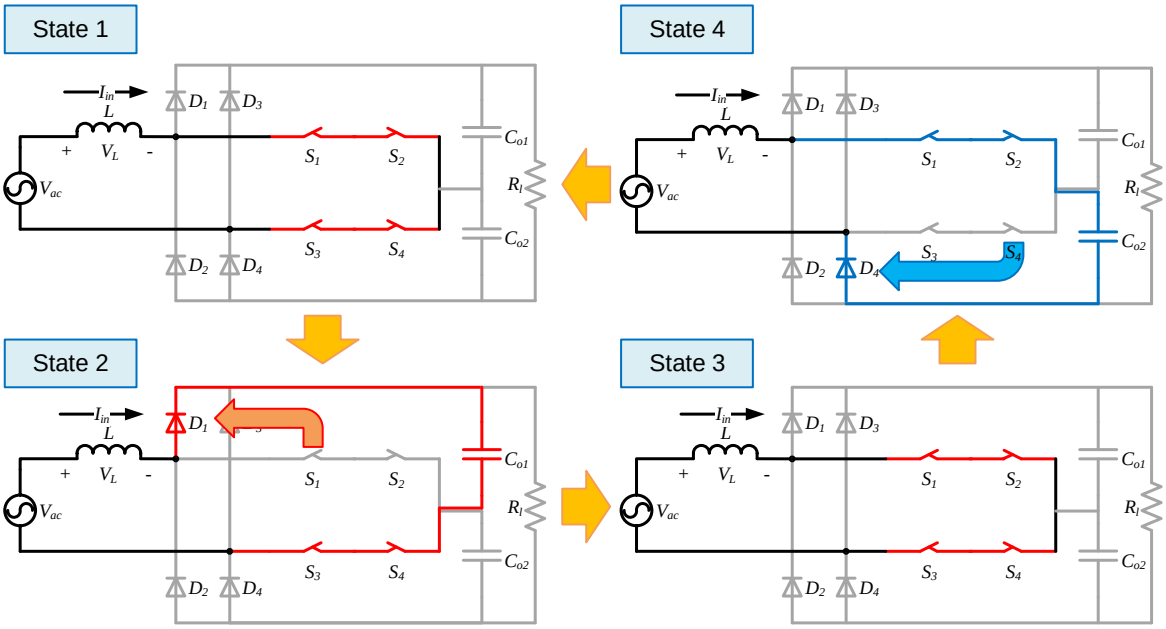


Fig. 21. Switching states transitions and switch commutations when $V_{ac} < V_{out}/2$ and $V_{ac} > 0$

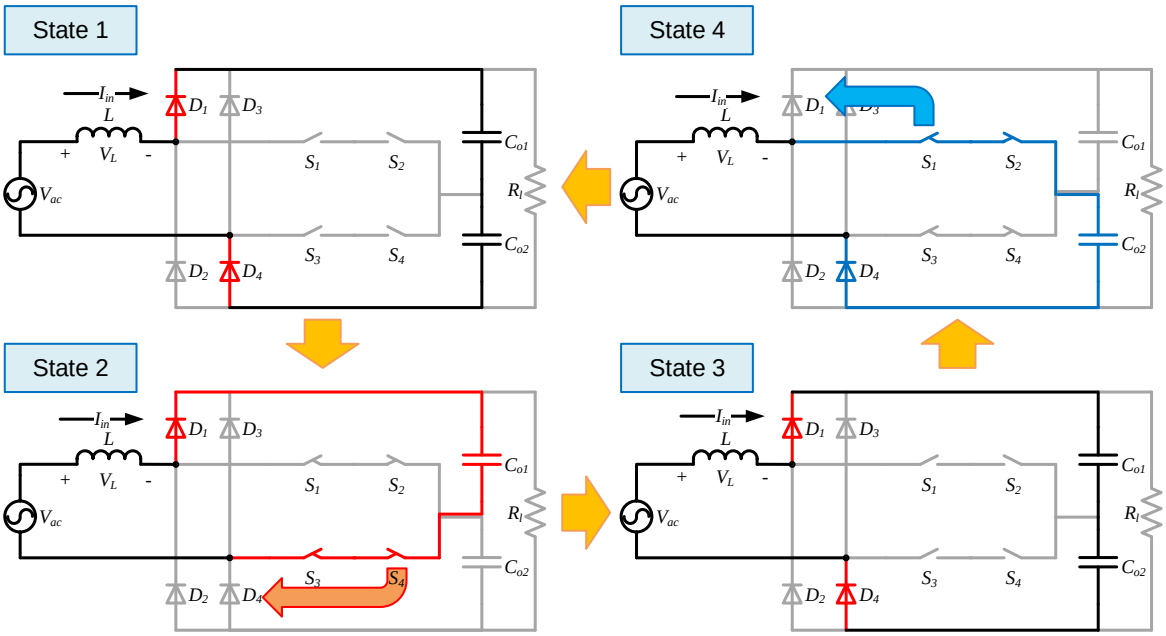


Fig. 22. Switching states transitions and switch commutations when $V_{ac} > V_{out}/2$ and $V_{ac} > 0$

2.3.2 MOSFET Switching Loss Modeling

The most accurate way to estimate MOSFET switching loss is by conducting tests such as the double pulse test to model the loss characteristics of semiconductor devices. However, if many

devices are involved, this method makes it time consuming to find the specifics that are most helpful for achieving maximum efficiency. Thus, an analytical loss estimation method that provides accurate loss estimation directly from datasheets of different semiconductor devices is more suitable for this work. However, switching of MOSFETs is a non-linear procedure, making switching loss modeling and calculation a tough task.

There are several analytical models for predicting MOSFET switching loss based on the information provided in the data sheets. One of the most accurate models is presented in [22], which explicitly shows the switching procedure , taking into consideration the nonlinearity of the MOSFET junction capacitors and loop inductors. Note that the model's solution is quite intricate, making it hard to implement. In this evaluation, a revised model, originated from a piecewise linear model proposed in [23] is used to predict MOSFET switching loss. The circuit used for explaining the model is shown in Fig. 23. The waveforms expected during the turn-on procedure are shown in Fig. 24. In this model, the gate charges of the MOSFET are used to calculate the turn-on and turn-off time instead of the non-linear capacitance due to the consistency of the charges in a wide voltage range. The loop inductors and the loss caused by charging the diode when turning on the switch are considered. Transition of the drain-to-source current and voltage are assumed to be linear. Typically, there are four intervals in a switching procedure, as shown in Fig. 24. The driving circuits, the parasitic and, most importantly, the gate charge dominating the interval, dominate the duration of each interval.

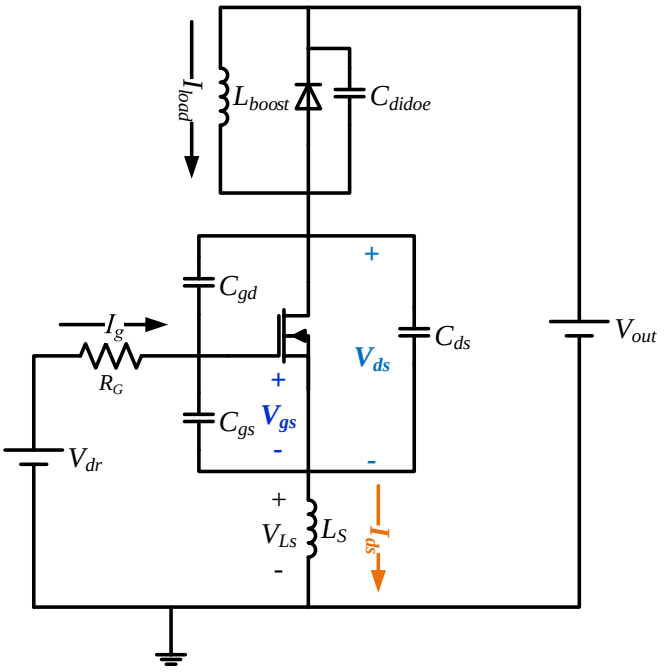


Fig. 23. Circuit for MOSFET switching loss prediction

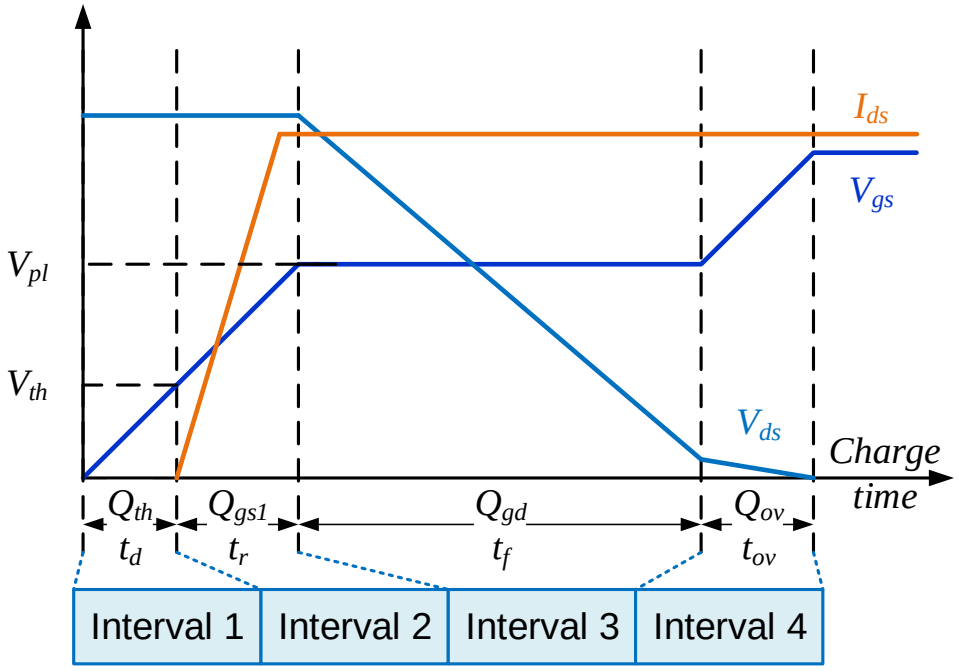


Fig. 24. Waveforms during turn-on procedure

The MOSFET turn-on procedure is described below:

Interval 1:

Gate voltage V_{gs} increases from zero to threshold voltage V_{th}. The gate charge that needs to be charged from driver is Q_{th}. There is no switching loss from this interval.

Interval 2:

Gate-to-source voltage V_{gs} increases from V_{th} to V_{pl} (plateau voltage of the MOSFET). In [23], it is assumed that V_{gs} stays at V_{pl} in this interval, while in this revised model, the variation of V_{gs} is considered, making it more accurate. At the same time, drain-to-source current rises to load current I_{load}. The gate charge provided by the gate driver during this interval is Q_{gs1}. Based on analysis, the following set of equations can be derived:

$$\begin{cases} V_{gs}(t) = \dfrac{V_{pl} - V_{th}}{t_r} t + V_{th} \\ V_{Ls} = L_s \dfrac{dI_{ds}}{dt} = L_s \dfrac{I_{load}}{t_r} \\ I_{gate,P2}(t) = \dfrac{V_{dr} - V_g(t) - V_{Ls}}{R_g} \\ Q_{gs1} = \int_0^{t_r} I_{gate,P2}(t) dt \end{cases} \tag{10}$$

where V_{Ls} is the voltage across common source inductance L_s, L_s is the common source inductance, I_{ds} is the drain to source current, t_r is the duration of this interval, R_g is the gate resistor, $I_{gate,P2}$ is the output current of the gate driver and V_{dr} is the gate driver output voltage.

Solving the equation set, the duration of this interval t_r is given by:

$$t_r = \frac{2R_g(\mathrm{Q}_{gs1} + \dfrac{L_s I_{load}}{R_g})}{2V_{dr} - V_{th} - V_{pl}} \tag{11}$$

Interval 3:

Gate voltage V_{gs} stays at V_{pl} due to the Miller Effect. Drain-to-source voltage begins to drop. The total charge required by the Miller capacitor is Q_{gd}, which can be found in the datasheet. Based on the analysis, the output current of gate driver $I_{gate,P3}$ during this interval is given by:

$$I_{gate,P3} = \frac{V_{dr} - V_{pl}}{R_g} \tag{12}$$

The duration of this interval is given by:

$$t_f = \frac{Q_{gd} R_g}{V_{dr} - V_{pl}} \tag{13}$$

It should be noted that the diode is also being charged during this interval and the current charging the diode junction capacitor will flow through the MOSFET channel, causing additional loss. The current charging the diode junction capacitor I_{diode} during this interval can be expressed as:

$$I_{diode} = C_{diode} \frac{d(V_{out} - V_{ds}(t))}{dt} = C_{diode} \frac{d(\frac{V_{out}}{t_f} \mathrm{t})}{dt} = \frac{C_{diode} V_{out}}{t_f} = \frac{Q_{diode}}{t_f} \tag{14}$$

where V_{out} is the DC bus voltage, and C_{diode} and Q_{diode} are the capacitance and total capacitive charge of the diode.

The resulting capacitive charge loss E_{cap} energy would be:

$$E_{cap} = \int_0^{t_f} I_{diode} V_{ds}(t) dt = \int_0^{t_f} \frac{Q_{diode}}{t_f} (V_{out} - \frac{V_{out}}{t_f} t) dt = \frac{1}{2} Q_{diode} V_{out} \tag{15}$$

Additionally, diode reverse recovery may take place during this interval due to the turn-off of the diode. Diode reverse recovery loss energy can be calculated as follows:

$$E_{RR} = Q_{RR} V_{out} \tag{16}$$

where Q_{RR} is the total reverse recovery charge of the diode.

Interval 4:

Gate voltage V_{gs} continues to rise, resulting in further reduction of the on-resistor. There is no switching loss in this interval.

Accordingly, the turn-on loss energy in this switching is given by:

$$E_{on} = \frac{1}{2} V_{out} I_{load} (t_{r,on} + t_{f,off}) + \frac{1}{2} Q_{diode} V_{out} + E_{oss,MOS} + Q_{rr} V_{out} \tag{17}$$

Turn-off of the MOSFET is similar to the turn-on process. For brevity, the derivations are not described here. The turn-off loss energy is given by:

$$E_{off} = \frac{1}{2} V_{out} I_{load} (t_{r,off} + t_{f,off}) \tag{18}$$

where $t_{r,off}$ and $t_{f,off}$ represent voltage rise time and current falling time resepectively during the turn-off procedure, and are given by:

$$t_{r,off} = \frac{-Q_{gd} R_g}{V_{dr,off} - V_{pl}}, \quad t_{f,off} = \frac{-2R_g (Q_{gs1} + \frac{L_s I_{load}}{R_g})}{2V_{dr,off} - V_{th} - V_{pl}} \tag{19}$$

where $V_{dr,off}$ is the MOSFET driver output voltage during the turn-off procedure. It can be zero or negative (if negative turn-off driving voltage is applied).

2.3.3 Simulation-based Converter Loss Calculation

Herein, using the loss calculation methods and models described previously, a simulation-based converter loss calculation method has been developed and implemented. With simulation, the current information in any switching cycle can be fully factored, based on which loss generated during a certain switching cycle can be calculated. For example, Fig. 25 shows the input current waveform in one switching cycle (from valley to valley) of a two-level semi-bridgeless PFC boost converter. Current flows through the MOSFET in the left part (from valley to peak) while the diode takes the current in the right part (from peak to valley). With the information gained from the simulation and the knowledge of conduction characteristics of the devices, conduction loss generated within this switching cycle can be easily calculated. Additionally, the current valley value and peak value are the turn-on current and turn-off current of the MOSFET, respectively. These can be determined through simulation as well. With the MOSFET switching loss model described previously, MOSFET switching loss can also be calculated. Moreover, theoretically, the flux density in the inductor is proportional to the input current; i.e. with knowledge of the input current, we can calculate the magnetization change of the inductor core. Using the Steinmetz equation, we can calculate the core loss. The complete simulation-based converter loss calculation process is depicted as a flow chart diagram in Fig. 26. A MATLAB script has been coded to implement the whole calculation. With the knowledge of converter operation point and device characteristics, the total converter loss and loss distribution can be completely calculated.

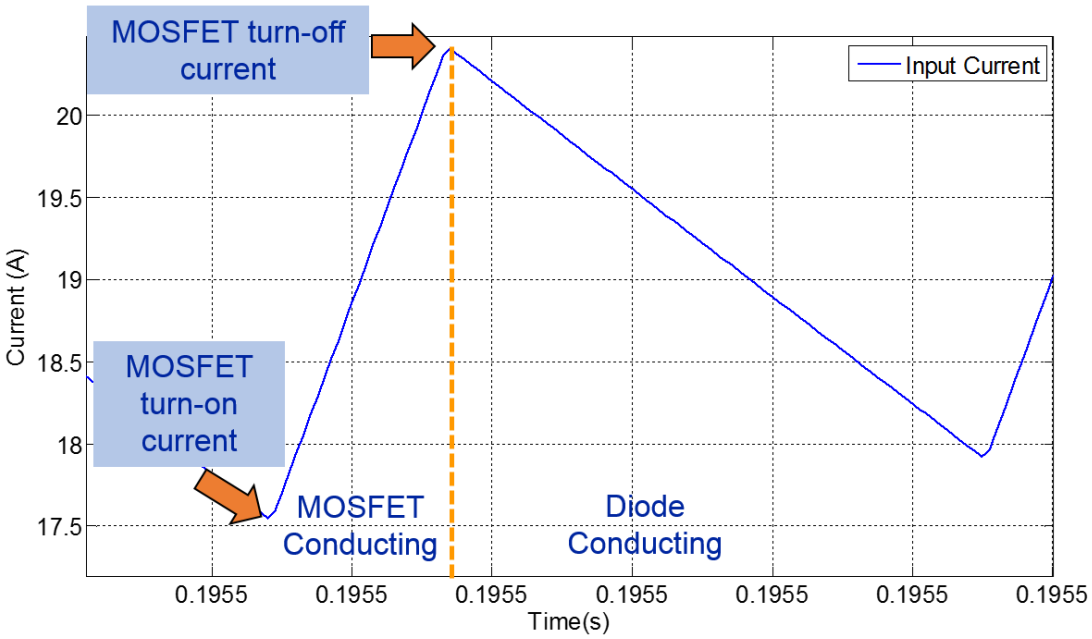


Fig. 25. Input current waveform of two-level semi-bridgeless PFC boost converter within one switching cycle

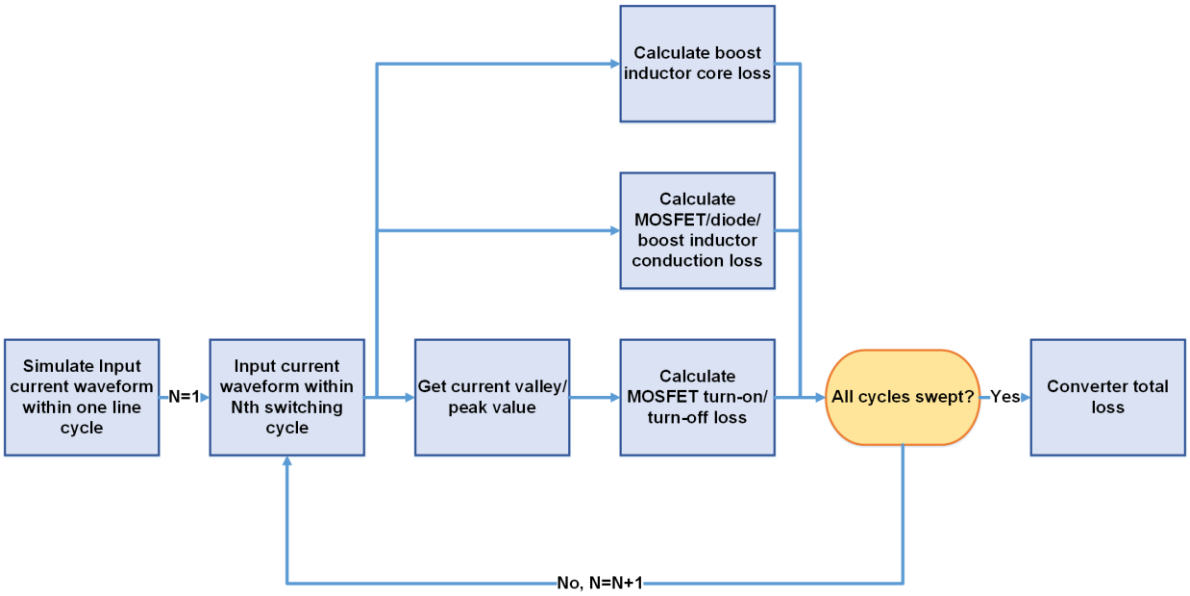


Fig. 26. Simulation-based converter loss calculation process

2.4 Efficiency-oriented Design Procedure

Proper design is a necessity for increasing converter efficiency. Specifically, all of the semiconductor devices should be carefully selected and all of the passive components should be properly designed to optimize converter efficiency. Based on the converter loss calculation method presented previously, the efficiency of different designs for a certain topology can be analytically calculated and compared in order to find the most efficient design. An efficiency-oriented design procedure has been developed and is depicted as a flow chart diagram in Fig. 27.

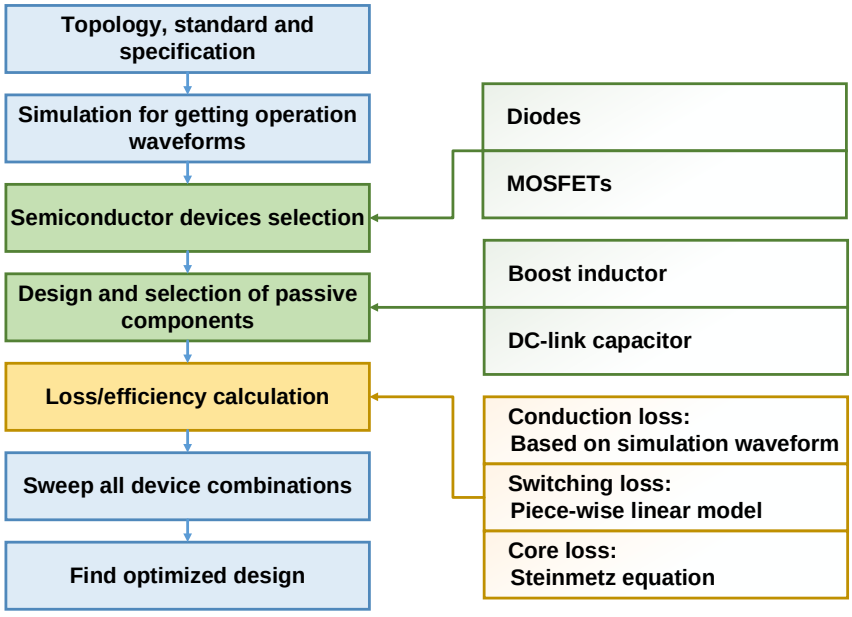


Fig. 27. Efficiency-oriented design procedure

The design procedure starts with the topology, standards, and specifications of the converter. Next, a program will be run to find the optimized design, namely, the combination of devices and inductor design that achieves the highest efficiency. The program starts with running the simulation. Then semiconductor devices are selected. In the next step, all passive components, namely the input boost inductors and DC bus capacitors, will be designed (mainly constrained by

the power quality standard). The converter loss/efficiency can be calculated accordingly. By sweeping different combinations of semiconductor devices (including different devices and different paralleling numbers), the semiconductor that achieves the lowest loss can be determined and will become the optimized design for this particular topology.

2.5 Converter Design Results

In order to find the most efficient converter design, an efficiency comparison based on the previously designed optimization procedure was conducted.

TABLE III. CONVERTER SPECIFICATIONS AND REQUIREMENTS

Input voltage	230 RMS Vac	Input current ripple frequency	70 kHz
Output voltage	400 Vdc	Maximum input current ripple	Below 20% of peak current
Output power	3 kW		

To make a fair and accurate comparison, all the converters were designed and optimized under the specifications and requirements listed in TABLE III. It should be noted that, to fulfill the requirements, different topologies rendered different designs: e.g., for a two-level semi-bridgeless PFC boost rectifier, switching frequency $f_{sw,2L}$ should be 70 kHz in order to generate a current ripple with 70 kHz frequency. According to [19], the maximum input current ripple of a two-level PFC boost rectifier is given by:

$$I_{ripple,\max,2L} = \frac{V_{out} T_{sw,2L}}{4L_{2L}} \tag{20}$$

where V_{out} is the DC bus voltage, L_{2L} is the boost inductance and $T_{sw,2L}$ is the switching period (1/ $f_{sw,2L}$). To keep the maximum input current ripple below 20% of peak current, its boost inductance L_{2L} should be large enough to satisfy:

$$\frac{V_{out}T_{sw,2L}}{4L_{2L}} \le 0.2I_{peak} \tag{21}$$

For a three-level bridgeless PFC rectifier, its switching frequency (carrier frequency for each phase leg) $f_{sw,3L}$ should be 35 kHz in order to generate 70 kHz current ripple frequency, as each phase leg switches once during one switching cycle. Its maximum current ripple is given by:

$$I_{ripple,\max,3L} = \frac{V_{out}T_{sw,3L}}{16L_{3L}} \tag{22}$$

where L_{3L} is the boost inductance and $T_{sw,3L}$ is the switching period (1/ $f_{sw,3L}$). Therefore, its boost inductance L_{3L} should satisfy:

$$\frac{V_{out}T_{sw,3L}}{16L_{3L}} \le 0.2I_{peak} \tag{23}$$

Interleaved rectifiers should have half the switching frequency (carrier frequency for each phase leg) of their non-interleaved counterparts, and the boost inductance for each sub-converter should be the same as that of their non-interleaved counterparts in order to keep the same input current ripple maximum amplitude and frequency.

All the semiconductor devices considered for efficiency optimization in this work are listed in TABLE IV. It should be noted that the voltage stress on the MOSFETs in three-level rectifiers is

half of the DC bus voltage (200 V) while the voltage stress on diodes in three-level rectifiers is the whole DC bus (400 V).

TABLE IV. SEMICONDUCTOR DEVICE CANDIDATES

600 V (650 V) MOSFETs					
Manufacture	Part Number	Current Rating (A)	Rdson (mΩ)	Qgs (nC)	Qgd (nC)
Infineon	IPW60R045CP	60	45	34	51
Infineon	IPW60R070C6	53	70	21	87
Fairchild	FCH76N60N	76	36	39	66
Fairchild	FCH47N60F	47	73	38	110
ST	STW55NM60ND	51	60	30	90
300 V MOSFETs					
ST	STW75NF30	60	45	36	69
Fairchild	FDA59N30	59	56	22	40
IR	IRFP4868PbF	70	32	60	57
600 V (650 V) SiC Diodes					
Manufacture	Part Number	Current Rating (A)		Qc (nC)	
ST	STPSC2006CW	20		24	
Infineon	IDH10S60C	10		24	
CREE	C3D20060D	28		50	
CREE	C3D16065D	22		42	
600 V Si Diodes for Clamping Diodes in Two-level Rectifiers					
Manufacture	Part Number	Current Rating (A)		Forward Voltage (V)	
Infineon	IDP23E60	23		1.5	
ST	STTH30L06	30		1.1	

All the boost inductors are designed based on Ferroxcube 3C90 ferrite material.

By sweeping all the converter efficiencies of all possible device combinations, following the design procedure developed previously, the most efficient designs are found. They are listed in TABLE V:

TABLE V. Optimized Designs of Evaluated Topologies

Topology	MOSFET	Diode	Clamping	Boost Inductance (μH)	Switching Frequency (kHz)
2LPFC	IPW60R45CP	2*STPSC2006CW	IDP23E60	390	70
I2LPFC	IPW60R45CP	2*STPSC2006CW	IDP23E60	390*2	35
3LPFC	FDA59N30	2*STPSC2006CW	None	195	35
I3LPFC	FDA59N30	2*STPSC2006CW	None	97.5*4	17.5

Their loss distribution and total loss are shown in Fig. 28:

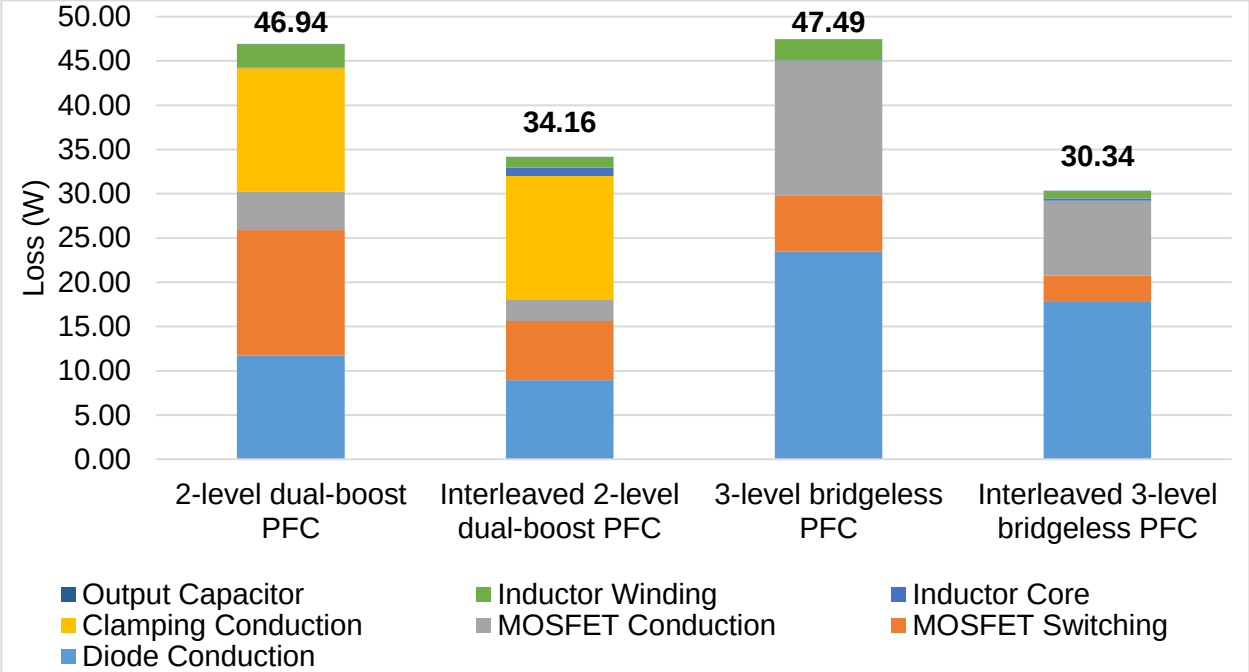


Fig. 28. Loss distribution and total loss of optimized PFC rectifiers

Additionally, the estimated loss on each single device in the converters are summarized in TABLE VI.

TABLE VI. Comparison of Loss per Device in Single-Phase Converters

	2-level PFC Converter	Interleaved 2-level PFC Converter	3-level PFC Converter	Interleaved 3-level PFC Converter
Carrier frequency (kHz)	70	35	35	17.5
MOSFET voltage stress (V)	400	400	200	200
Switching loss per MOSFET (W)	7.07	1.68	1.58	0.73
Conduction loss per MOSFET (W)	2.20	0.61	3.82	1.05
Loss per diode (W)	5.87	2.24	5.87	2.24

2.6 Efficiency (Loss) Evaluation and Comparison

2.6.1 Comparison between Two-level PFC Converters

Among the topology variants of two-level PFC rectifiers, the interleaved two-level semi-bridgeless PFC rectifier is found to be the more efficient, mainly due to reduced switching loss as a result of reduced switching current in the sub-converters. MOSFET conduction loss is not dominant in two-level rectifiers under the selected operation conditions. Therefore, interleaved rectifiers do not benefit a great deal from reduced MOSFET conduction loss.

Examining the “loss per device” summarized in TABLE VI, it can be clearly seen that devices in interleaved converter has much lower loss. This is a natural result brought by doubled the number of devices in interleaved converters. This indicated that interleaving converter not only helps with loss reduction but also helps with thermal management. With loss spread among the devices, interleaved converters can achieve better thermal performance.

2.6.2 Comparison between Three-level PFC Converters

Two of the most critical losses of three-level PFC converters are MOSFET conduction and diode conduction loss. Among the variants of three-level PFC converters, the interleaved three-level PFC rectifier has lower loss as a result of the reduced switching loss, reduced MOSFET conduction loss and reduced diode conduction loss brought about by its paralleling operation. Similar to two-level PFC converters, interleaving converter can help achieving better thermal performance.

2.6.3 Comparison among Two-level and Three-level Converters

Though the total loss of the two-level semi-bridgeless PFC boost rectifier is similar to that of the three-level bridgeless PFC rectifier, their loss distribution is quite different. For the two-level semi-bridgeless PFC boost rectifier, the dominant losses are MOSFET switching loss and clamping diode conduction loss. For a three-level bridgeless PFC rectifier, the biggest loses are MOSFET and diode conduction loss. The diode conduction loss of the three-level bridgeless PFC rectifier is twice that of the two-level semi-bridgeless PFC boost rectifier, as its diode conduction time is doubled (this can be mathematically proven) compared to its two-level counterpart. The MOSFET conduction loss of the three-level bridgeless PFC rectifier is also higher because the MOSFET branch in the three-level rectifier consists of two MOSFETs in series, and the R_{dson} of 300 V MOSFETs in its

design is equivalent to 600 V MOSFETs. To reduce MOSFET conduction loss, an interleaved three-level bridgeless converter should be considered. The switching loss of the three-level bridgeless PFC rectifier is benefited a great deal by its reduced switching voltage and the use of low-voltage-rating devices, making it a promising topology for push switching frequency.

Chapter 3. Design and Comparison of AFE Converters for Three-phase Input

This chapter presents a complete design and evaluation procedure for the three-phase AFE converter. TABLE VII summarizes the targets and specifications of the converter, where achieving high efficiency while maintaining a reasonable size are the main concerns in this work. This chapter is organized as follows: In section 3.1, topologies and techniques for high efficiency three-phase rectification are briefly reviewed. Proper topologies for this work are selected accordingly. In section 3.2, operation principles of the selected topologies are introduced. Based on converter design and loss calculation methods similar to those developed in Chapter 2, converter loss of all the three-phase candidates are analyzed and calculated in section 3.3. Results will be evaluated in section 3.4.

TABLE VII. THREE-PHASE AFE CONVERTER TARGETS AND SPECIFICATIONS

Items	Target/Specification
Input Voltage	Three-phase 230 Vac
Input Frequency	360 Hz ~ 800 Hz
Output Voltage	TBD
Output Power	3 kW
Maximum Ambient Temperature	70 ℃
Efficiency	Higher than 99%
Cooling	Free Convection Air-Cooling
Power Quality Standard	DO-160F
Power Factor	Higher than 0.99

3.1 Introduction of High Efficiency Three-phase Rectifiers

Three-phase rectifiers have been widely used in various industries, and increasing their efficiency has always been an important topic. For boost-type rectifiers, conventional two-level six-switch boost rectifiers have been most used, due to their simplicity. This type of converter is selected as a benchmark in this work. In order to achieve higher efficiency, three-level converters, such as three-level neutral point clamped (NPC) rectifiers (selected as the topology candidate in this work), are better options due to their lower switching voltage. This allows the use of lower voltage switches, which usually means lower on-resistance and/or smaller junction capacitors [24]. Among the three-level topologies, Vienna rectifiers have been widely used to achieve high efficiency [25, 26]. Several phase leg configurations for Vienna rectifiers have been proposed in [27-30]. To achieve minimum conduction loss, a configuration proposed in [29] where, for each phase leg, one diode is used for positive or negative rail clamping and two anti-series connected MOSFETs are used for middle point connection, is selected for evaluation in this work. With the use of SiC diodes, the reverse recovery loss from diodes in the Vienna rectifiers can be totally eliminated, which further makes the Vienna rectifier a promising topology in achieving high efficiency.

The topologies to be evaluated in this chapter are: the two-level boost rectifier (shown in Fig. 29); the three-level NPC rectifier (shown in Fig. 30); and the Vienna rectifier (shown in Fig. 31).

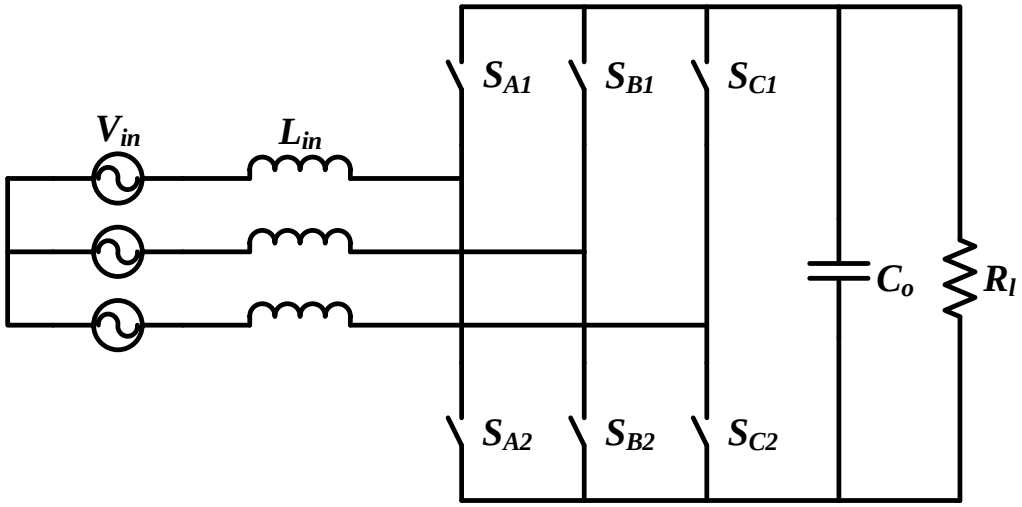


Fig. 29. Two-level boost rectifier

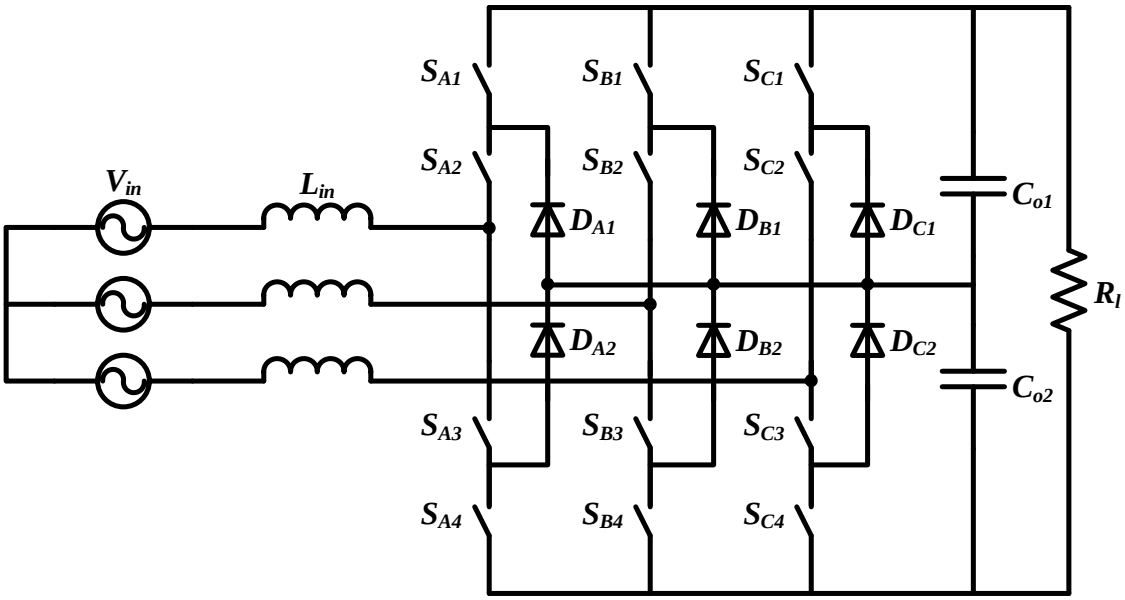


Fig. 30. Three-level NPC rectifier

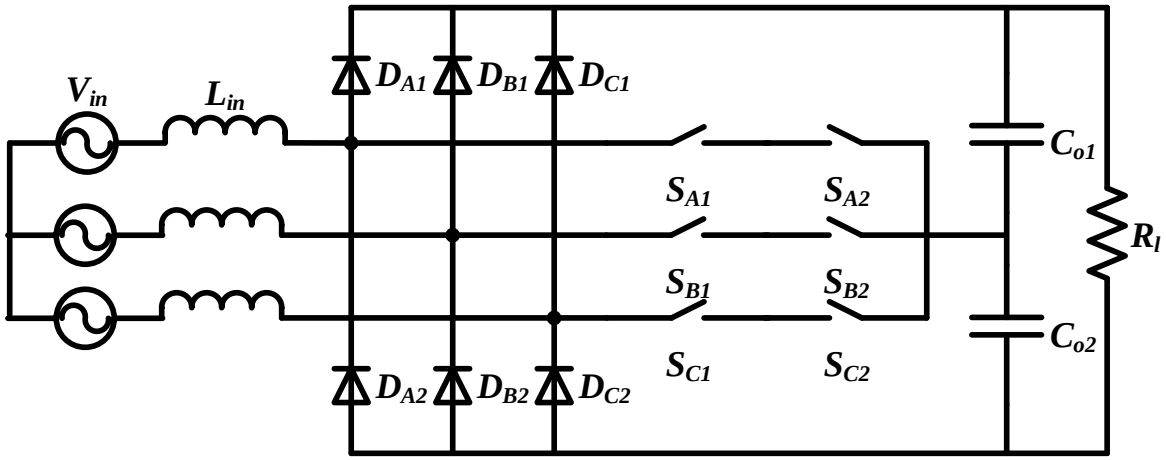


Fig. 31. Vienna rectifier

3.2 Operation principle

3.2.1 Two-level Boost Rectifier

In this converter, S_{A1} and S_{A2} constitute one phase leg, while S_{B1}, S_{B2} and S_{C1}, S_{C2} constitute the other two. The phase legs convert DC voltage into AC voltage. With proper modulation and control, the phase angle between the voltage generated by the six-switch bridge and the input of three-phase voltage can be well controlled and thus, achieve unity PFC for input.

A current controller designed in the d-q frame achieves the input current control: three-phase input currents are transferred into the d-q frame and two current compensators are designed to maintain designed the current values separately on the d axis and q axis. The modulator will process the output of the controller to generate proper gate signals.

To modulate the six-switch bridge, a space vector modulation (SVM) scheme [31] is implemented in this work. The space vector states in the d-q axis for a six-switch bridge are shown in Fig. 32.

To reduce converter switching loss, a discontinuous PWM (DPWM) scheme is adopted in order to avoid phase leg switching around their current maxima. The clamping options are also shown in Fig. 32 (A=p means in that sector, phase A is clamped to the positive rail). The space vectors selected to clamp phase A to the positive rail would be: [p n p], [p n n] and [p p p] ($-30^{o} \leq \theta < 0^{o}$) or [p n n], [p p n] and [p p p] ($0^{o} \leq \theta < 30^{o}$). Herein, p stands for positive rail clamping of the associated phase and n means the opposite.

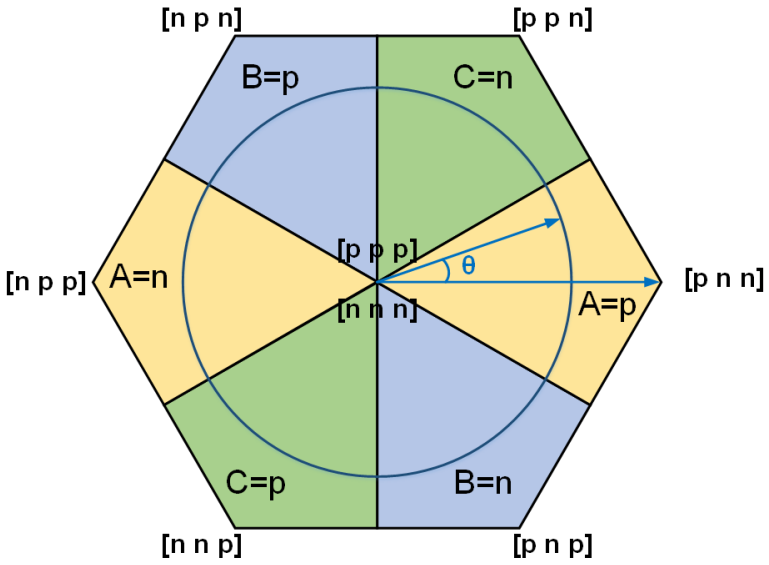


Fig. 32. Space vectors two-level rectifier DPWM and clamping options.

3.2.2 Three-level NPC Rectifier

In the three-level NPC rectifier shown in

Fig. 30, S_{A1}, S_{A2}, S_{A3}, S_{A4}, D_{A1}, and D_{A2} constitute a phase leg. Three different voltage levels can be generated by the phase leg: voltage of the positive rail (S_{A1}, S_{A2} on), voltage of the negative rail (S_{A3}, S_{A4} on), and middle point voltage of the DC bus (S_{A2}, D_{A1} on or S_{A3}, D_{A2} on, determined by current direction). The additional voltage level not only lowers voltage stress on the devices, but

also provides more flexibility in modulating the converter. The modulation scheme adopted for the three-level NPC rectifier is DPWM for three-level converters, which is similar to its two-level counterpart. The space vector states for the selected modulation scheme and clamping options are shown in Fig. 33.

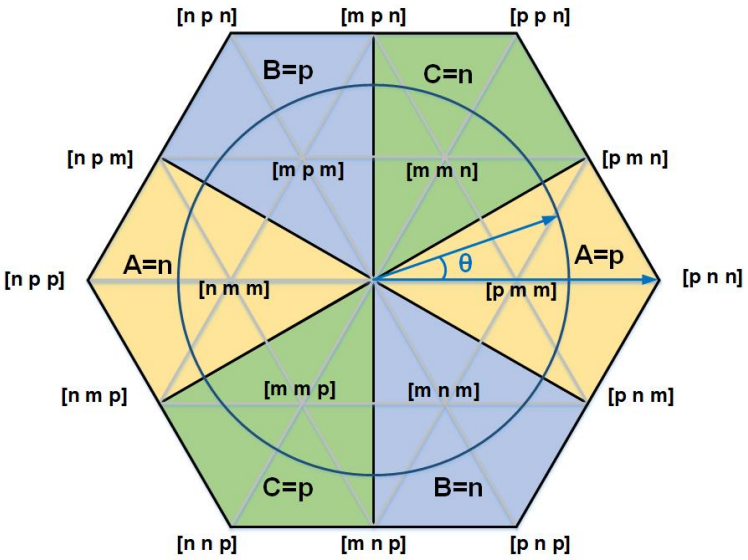


Fig. 33. Space vectors of three-level rectifier DPWM and clamping options.

The modulation index *M* for three-phase converters in this work is defined as:

$$M = \frac{V_{in,peak}}{\frac{V_o}{2}} \tag{24}$$

where $V_{in,peak}$ is the peak value of input phase voltage and V_o is the output voltage (DC bus voltage). For a boost rectifier, *M* is always smaller than $2\sqrt{3}/3$. To reduce switching loss, low DC bus voltage is always desirable; i.e. *M* should be kept reasonably high. In modulation design, it is assumed that *M* is always higher than $\sqrt{3}/3$ (V_o is less than 1126 V). In this case, the space vectors selected to clamp phase A to the positive rail would be: [p m m], [p n m] and [p n n] (-30º≤

$\theta < 0$) or [p m m], [p m n] and [p n n]. For these space vectors, p and n have the same meaning as in the two-level case, while m stands for clamping of the middle point.

3.2.3 Vienna Rectifier

In the Vienna rectifier shown in Fig. 31, S_{A1}, S_{A2}, D_{A1} and D_{A2} constitute a phase leg for phase A. It should be noted that, S_{A1} and S_{A2} are connected in an anti-series manner, forming a four-quadrant switch in order to block voltage from both directions. Like the three-level NPC rectifier, the DC bus of the Vienna rectifier is split by two capacitors, allowing the phase legs to generate three voltage levels. However, unlike the three-level NPC rectifier, the Vienna rectifier does not have the flexibility to generate all three voltage levels at one time due to its current-commutated property. E.g. for phase A, if current is flowing from the input side to the output side, only positive rail voltage (through D_{A1}) and middle voltage of the DC bus can be generated by the corresponding phase leg. Negative rail voltage cannot be reached because the current in phase A will not forward bias D_{A2} at this time. Therefore, the Vienna rectifier is a current-commutated rectifier where converter operation is determined by not only the switch's state but also the current direction. This property makes the Vienna rectifier a unidirectional converter; i.e. energy cannot feed from the DC bus to the AC inputs. Therefore, unlike other bi-directional topologies, there is no need to worry about shoot-through problems [26].

In the following modulation scheme analysis, it is assumed that the displacement angle between input current and voltage vectors is negligible. This is true when input filter is properly designed. For the modulation scheme design, the current-commutated characteristics should be carefully considered, as some of the space vectors may not be reachable when unity PFC is achieved. For

example, in Fig. 33, when $30^{o} \leq \theta < 210^{o}$, vectors that require negative voltage from phase B are not reachable because the current in phase B is positive therein. Two DPWM schemes (DPWMA, the space vector selection shown in Fig. 34, and DPWMB, the space vector selection shown in Fig. 35) for the Vienna rectifier have been proposed and evaluated in Ref. [32]. The modulation scheme applied in this work is selected based on these two schemes.

The clamping selection of DPWMA is described in Fig. 34. This modulation scheme features phase clamping around the maxima and zero-crossing of the associated phase current. For example, in Fig. 34, the blue circle represents the trajectory of the desired voltage vectors. In region 1 (marked with red outline, determined by the intersection points between small triangles formed by voltage vectors and blue circle) where the current in phase A is at its maxima, phase A is clamped to the positive rail. The space vectors selected to achieve the clamping are: [p n m], [p n n], [p m m] when $\theta < 0^{o}$ or [p m n], [p n n], [p m m] when $\theta \geq 0^{o}$. In region 2 where the current in phase B is close to zero, phase B is clamped to the middle points. The space vectors selected for this region are: [p m n], [p m m], [m m n]. It is worth noting that while the total duration of region 1 and region 2 takes one sixth of one fundamental period, the distribution between the two regions varies with the modulation index. As the modulation index increases, the duration of interval 1 will be longer; i.e. switching loss reduction is more effective because current in phase A is close to its maxima.

On the other hand, modulation index does not affect clamping duration distribution in DPWMB. Its clamping selection is described in Fig. 35. Different from DPWMA, all of the clamping is not achieved at the corresponding current maxima when DPWMB is applied. As a result, when the modulation index is high (as it is in this work), switching loss reduction achieved by DPWMB is

not as effective as that of DPWMA. This claim is also verified in Ref. [32]. To reduce converter loss, DPWMA is selected in this work.

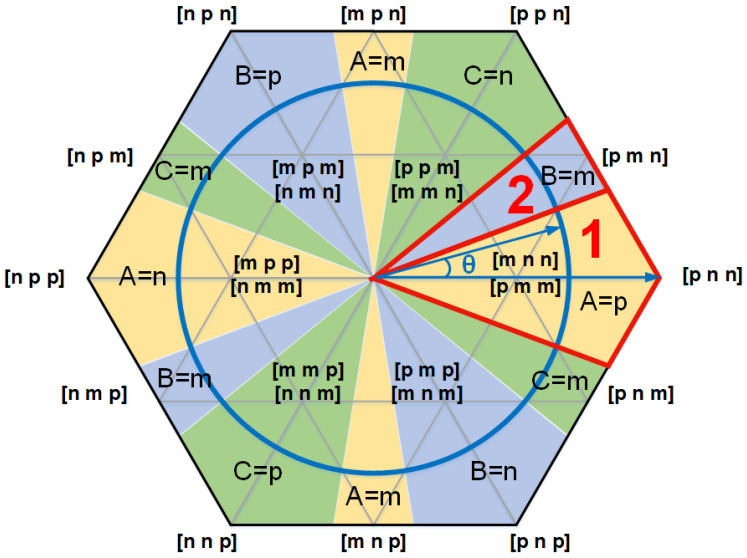


Fig. 34. Space vectors of DPWMA and clamping options.

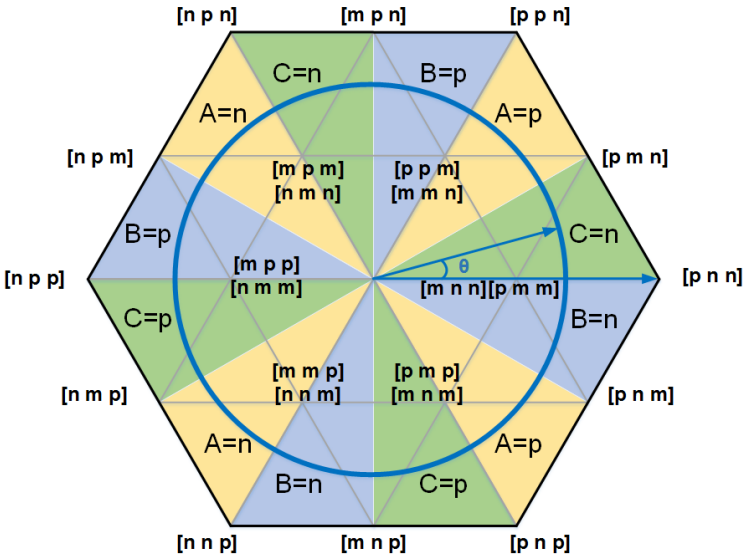


Fig. 35. Space vectors of DPWMB and clamping options

3.3 Loss Analysis and Calculation

In this section, the converter losses of all the candidates will be analyzed. This chapter starts with a loss analysis of the three-phase converters, where the commutations of the converters will be analyzed in order to facilitate switching loss calculation. With the loss calculation methods described in section 2.3, converter losses can be thoroughly calculated.

3.3.1 Loss Analysis

Similarly to single-phase converters, the three-phase converter's loss comes mainly from conduction loss, inductor core loss, and switching loss. Conduction loss and core loss analysis have been addressed in section 2.3. For purposes of brevity, these losses will not be discussed in this chapter.

To study switching loss, the commutations of all the topology candidates should be carefully analyzed. For two-level boost rectifiers, the commutation within a phase leg takes places between the upper switch and the lower switch, which is similar to the commutation found in two-level semi-bridgeless PFC boost rectifiers. The only difference is that, in the three-phase case, the Schottky diode is replaced with MOSFET. The reverse recovery loss of the MOSFET body diode should be considered in switching loss calculations. The piecewise linear MOSFET switching model developed in section 2.3.2 can be applied to calculate the switching loss of the two-level boost rectifier.

For the three-level NPC rectifier, within one switching period, the phase leg output voltage will be either positive (or negative) rail voltage or the middle point voltage of the DC bus. I.e. the phase leg output voltage will not jump from positive rail voltage to negative rail voltage, nor will the converse occur. For instance, with the selected modulation scheme, when $30^{o} \leq \theta < 60^{o}$ (as defined

in Fig. 33), the selected space vectors are [m m n], [p m n], and [p p n], where the output of phase A will be either positive rail voltage or middle voltage of the DC bus. The two corresponding switching states of phase A are shown in Fig. 36. The switching state for clamping of the positive rail is shown on the left, where S_{A1} and S_{A2} are on, and S_{A3} and S_{A4} are off. The blocking voltage of S_{A4} is clamped by D_{A2}. Thus, the blocking voltage of both S_{A3} and S_{A4} is half of the DC bus voltage. Switching from the state on the left to the state on the right requires turning S_{A1} off, and turning S_{A3} on, while S_{A2} is kept on and S_{A4} is kept off. The current commutates from S_{A1} and S_{A2} to S_{A3} and D_{A2}, which achieves clamping of the middle point. The blocking voltage of S_{A1} and S_{A4} are both half of the DC bus voltage. No voltage is blocked by S_{A2}. Therefore, during the transition, switching losses comes from the turn-off loss of S_{A1} and the turn-on loss of S_{A3}. When transitioning back, the reverse process should be applied, resulting in a turn-on loss of S_{A1} and turn-off loss of S_{A3}. No reverse recovery loss is generated by D_{A1} or D_{A2}, as they are not reverse biased in any switching state. As shown, the commutation in a three-level NPC rectifier resembles that found in two-level boost rectifiers, where commutation takes place between two active switches. Thus, the piecewise linear MOSFET switching model, as developed in section 2.3.2, can be used for switching loss calculation. It should be noted that, for three-level NPC rectifiers, unlike two-level converters, the switching voltage is always half of the DC bus voltage.

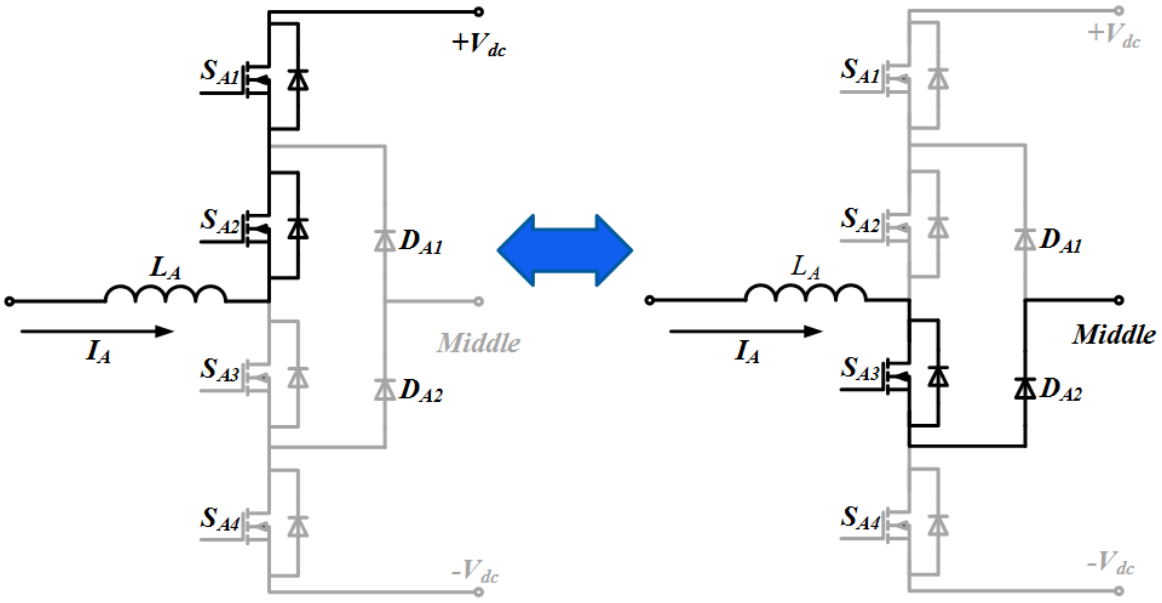


Fig. 36. Commutation of three-level NPC rectifier.

For the Vienna rectifier, in a certain phase leg, the commutation is the same as that of the single-phase three-level bridgeless PFC rectifier described in section 2.3. The same calculation method can be applied as well.

3.3.2 Loss Calculation

With the commutation analysis done in section 3.3.1 and loss calculation method (the MOSFET switching model, simulation-based, loss calculation) developed in section 2.3, the converter loss of three-phase rectifiers can be calculated accordingly. Attention should be paid to the differences between the loss calculation for single-phase rectifiers and three-phase rectifiers. Single-phase two-level converters are designed so that MOSFETs always commutate with SiC diodes. In the two-level boost rectifier and the three-level NPC rectifier, commutations take place between two MOSFETs, which induces MOSFET body diode reverse recovery loss.

In order to make a fair comparison, all the converters went through an efficiency-oriented design procedure. The procedure is provided in the flow chart diagram of Fig. 37.

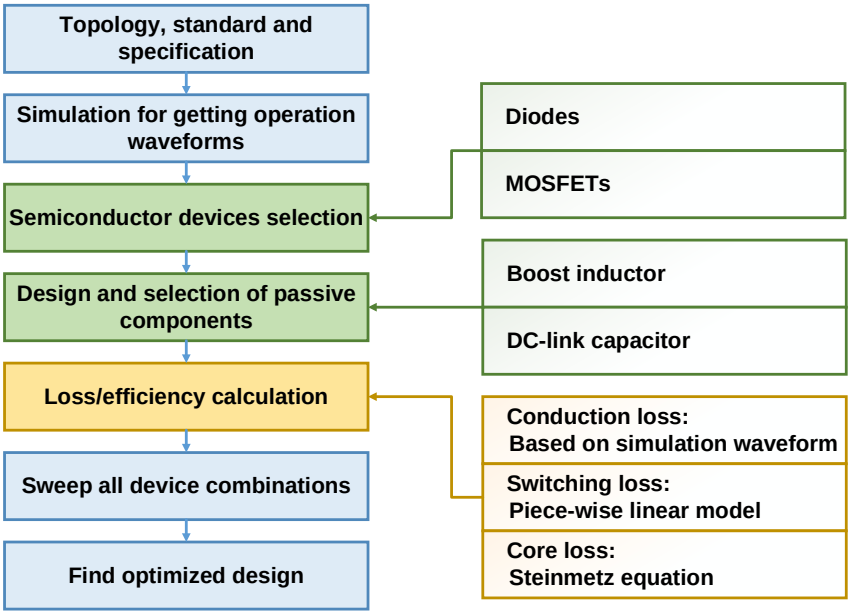


Fig. 37. Efficiency-optimized design procedure for three-phase rectifiers.

The design procedure starts with the topology, standards, modulation scheme and specifications of the converter. Then, a sweeping program will be run to find the optimized design. The sweeping program starts with selection of the semiconductor. All the passive components – namely the input boost inductors, and the DC bus capacitors– will be designed (constrained mainly by power quality standards) in the next step. The converter's loss/efficiency can be calculated accordingly. By sweeping different combinations of semiconductor devices (including different devices and different paralleling numbers), the semiconductor that achieves the lowest loss can be determined and will become the optimized design for the specific topology.

3.4 Efficiency (loss) Comparison

The converter requirements and specifications for the comparison of three-phase rectifiers are listed in TABLE VIII.

TABLE VIII. THREE-PHASE CONVERTER SPECIFICATIONS AND REQUIREMENTS

Input voltage	230 Vac	Switching frequency	44 kHz
Input frequency	400 Hz	Total harmonics distortion	Below 10%
Output voltage	650 V	Output power	3 kW

The loss distribution and total loss of the three-phase rectifiers are shown and compared in Fig. 38.

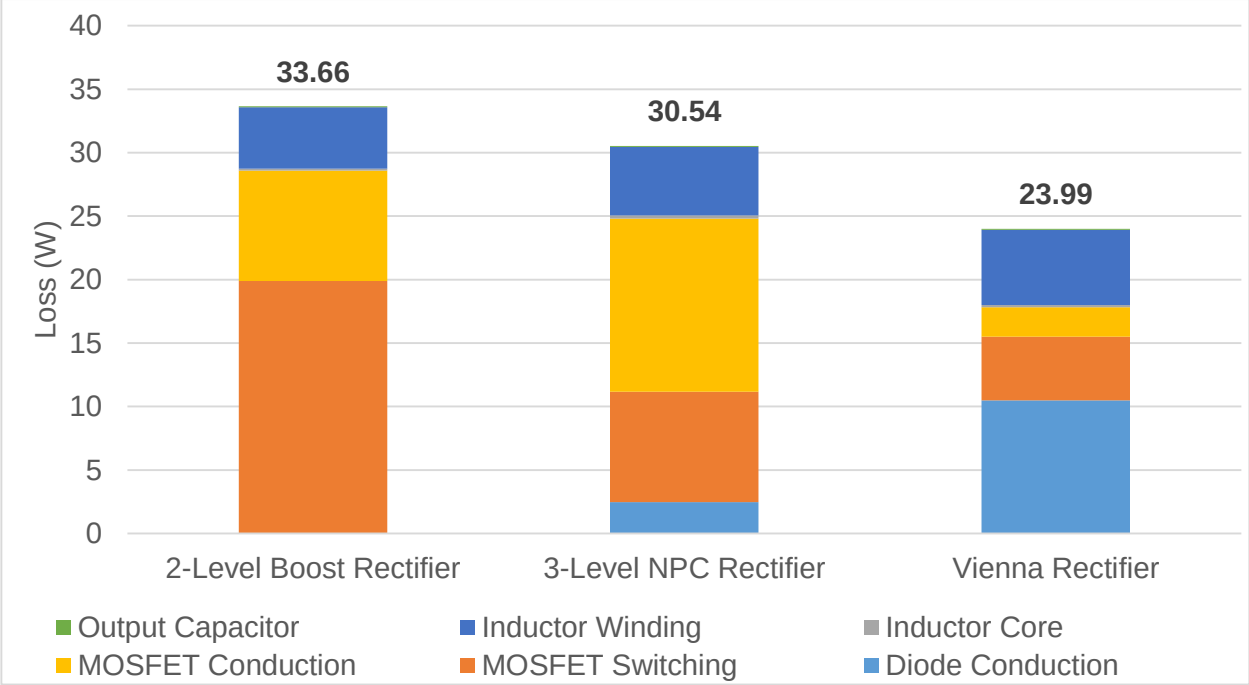


Fig. 38. Loss distribution and comparison of three-phase rectifiers.

In this comparison, the Vienna rectifier is found to be the most efficient. In comparison to two-level boost rectifiers, both three-level rectifiers (the three-level NPC rectifier and the Vienna

rectifier) achieve smaller loss due to reduced switching voltage. Moreover, switching loss of the Vienna rectifier is smaller than that of the three-level NPC rectifier, as reverse recovery loss is eliminated by the use of the SiC Schottky diode. This is the main reason that the Vienna rectifier outperforms the others.

The losses on each devices in the converters are given in TABLE IX.

TABLE IX. Comparison of Loss per Device in Three-Phase Converters

	2-level Boost Rectifier	3-level NPC Rectifier	Vienna Rectifier
Carrier frequency (kHz)	44	44	44
Boost inductance (μH)	720	360	340
MOSFET voltage stress (V)	650	325	325
Switching loss per MOSFET (W)	3.32	1.35 (loss on inner MOSFET)	0.83
Conduction loss per MOSFET (W)	1.45	1.14 (loss on inner MOSFET)	0.39
Loss per diode (W)	0	0.41	1.74

Here, it can be seen that loss on MOSFETs and diodes in Vienna rectifier is more evenly spread comparing to the other two topologies, which indicates that Vienna rectifier can achieve better thermal management.

In this work, the Vienna rectifier is selected as the basic topology to be built in order to achieve the work's objectives and specification targets. Moreover, the loss per device comparison of single-phase converters indicates that interleaving converters can help with achieving higher efficiency as well as thermal management. Thus, interleaved Vienna rectifier is selected to be constructed.

Chapter 4. Design and Implementation of a Dual-Channel Interleaved Vienna Rectifier

The advantage of the Vienna rectifier in achieving high efficiency was shown in the previous chapter. To explore its efficiency limits and avoid device overheating, interleaving the Vienna rectifier in order to help reduce conduction loss and switching loss is examined. The corresponding design and implementation issues of constructing a high efficiency interleaved Vienna rectifier will be discussed in this chapter.

4.1 Introduction of Interleaved Vienna Rectifiers

Paralleling switches or converters is a common practice used to achieve higher efficiency and better thermal management. In such practices, interleaving the gate signals of several sub-converters instead of simply gating them simultaneously could further enhance efficiency and power density [33-36]. The cancellation effect among interleaved sub-converters allows smaller input filters. In other words, the switching frequency of each sub-converter in the interleaved systems can be lower while achieving the same power quality with the same passive components, which lowers switching loss. Additionally, applying the interleaving technique may reduce the EMI filter size due to its cancellation effect among sub-converters [37]. Thus, a dual-channel interleaved Vienna rectifier, which combines the advantages of a Vienna rectifier and interleaved systems in achieving high efficiency, is selected to be built for this work.

4.2 Operation Principles of the Dual-channel Interleaved Vienna Rectifier

Fig. 39 shows the topology of the interleaved Vienna rectifier studied in this paper. In this topology, S_1, S_2, S_5, S_6, S_9, S_{10}, and the diodes directly connected to these MOSFETs form a sub-converter that can operate independently as a Vienna rectifier. The other switches form the other sub-converter. The two corresponding phase legs in different sub-converters are connected with an inter-phase inductor (shown as L_{MA}, L_{MB} and L_{MC} in Fig. 1). L_A, L_B and L_C are the input boost inductors for the converter. Two corresponding phase legs merged by the inter-phase inductor share the same boost inductor. E.g. the phase leg constituted of D_1, D_2, S_1, S_2 and the phase leg constituted of D_3, D_4, S_3, S_4 are merged by inter-phase inductor L_{MA} and share input boost inductor L_A.

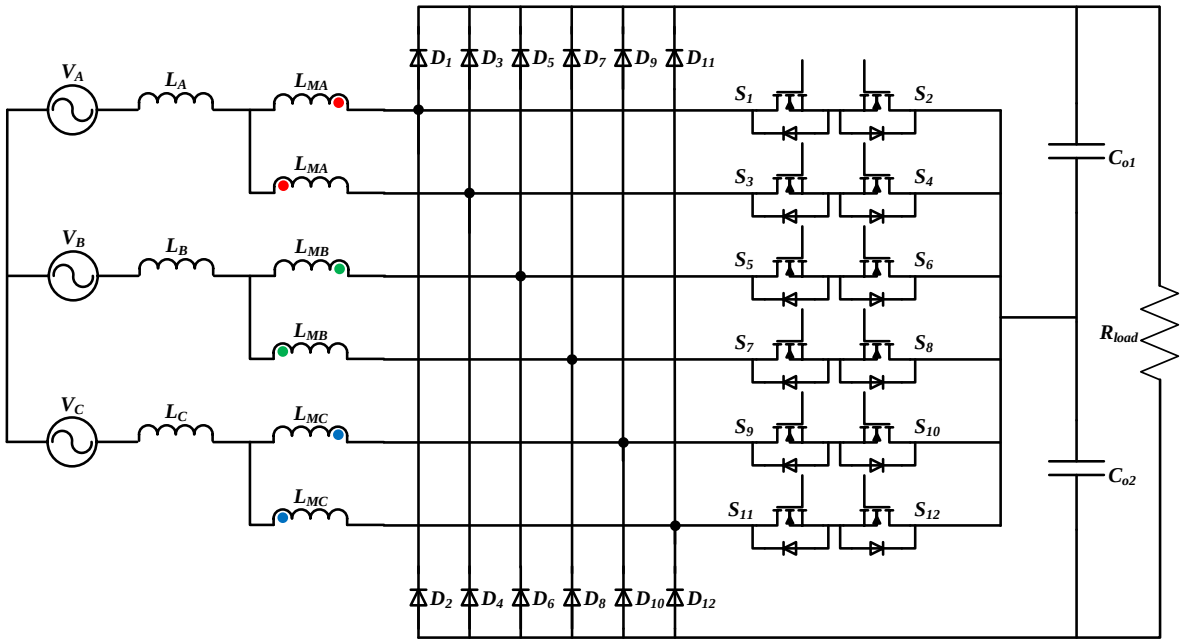


Fig. 39. Topology of dual-channel interleaved Vienna rectifier.

The operation principle of a single Vienna rectifier was introduced in Chapter 3. To operate the whole converter in an interleaved manner, we can introduce a phase shift between the carriers of the two corresponding phases in different sub-converters. With the two sub-converters interleaved, some current distortion in each interleaved phase will be canceled. I.e. the current peak (valley) in a certain phase will meet with the current valley (peak) in its counterpart, producing a smoother current waveform seen from the source side. As a result, the switching frequency of each sub-converter in the interleaved systems can be lower and still achieve the same input current quality (THD), which helps reduce switching loss.

4.3 Circulating Current Generation and Attenuation in Interleaved Converters

4.3.1 Generation Mechanism of Circulating Current in Interleaved Converters

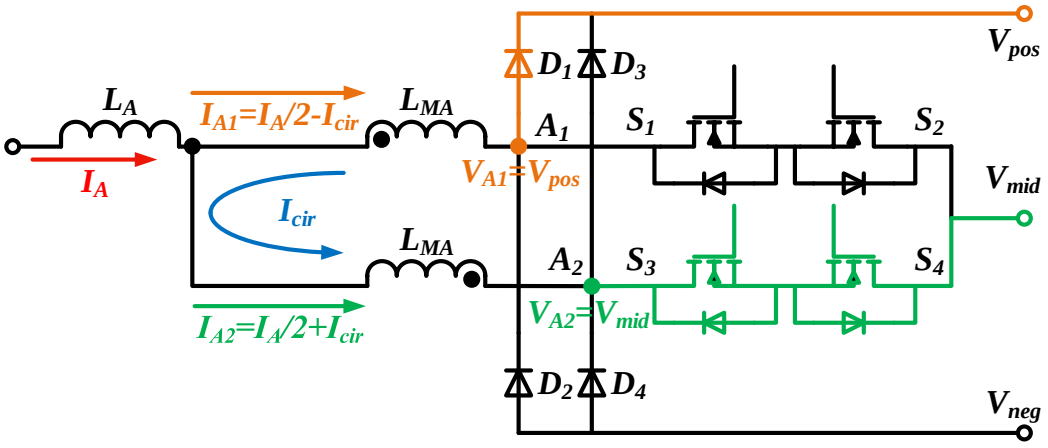


Fig. 40. Circulating current generation mechanism.

Interleaving two sub-converters brings unwanted circulating current into the system [35, 38]. Circulating current is the current produced by voltage differences between interleaved phases. As

shown in Fig. 40, the current flowing through the input boost inductor is defined as I_A. The common current flowing through each interleaved phase ((I_{A1} + I_{A2}) /2) is I_A/2. In addition, the difference between the two currents divided by two ((I_{A2} - I_{A1}) /2) is defined as the circulating current, I_{cir}. If point A_1 is clamped to the positive rail by diode D_1 and A_2 is connected to the middle point of the DC bus by S_3 and S_4, the voltage difference between A_1 and A_2 will generate current (I_{cir}) circulating within the two phases. Fig. 41 shows the simulated waveforms of the current in phase A of each sub-converter (I_{A1} and I_{A2}), the circulating current (I_{cir}), and the voltage difference between A_1 and A_2 (V_{A1} - V_{A2}). This clearly shows that the voltage difference determines the circulating current; i.e. when the voltage difference is positive, the circulating current increases, etc.

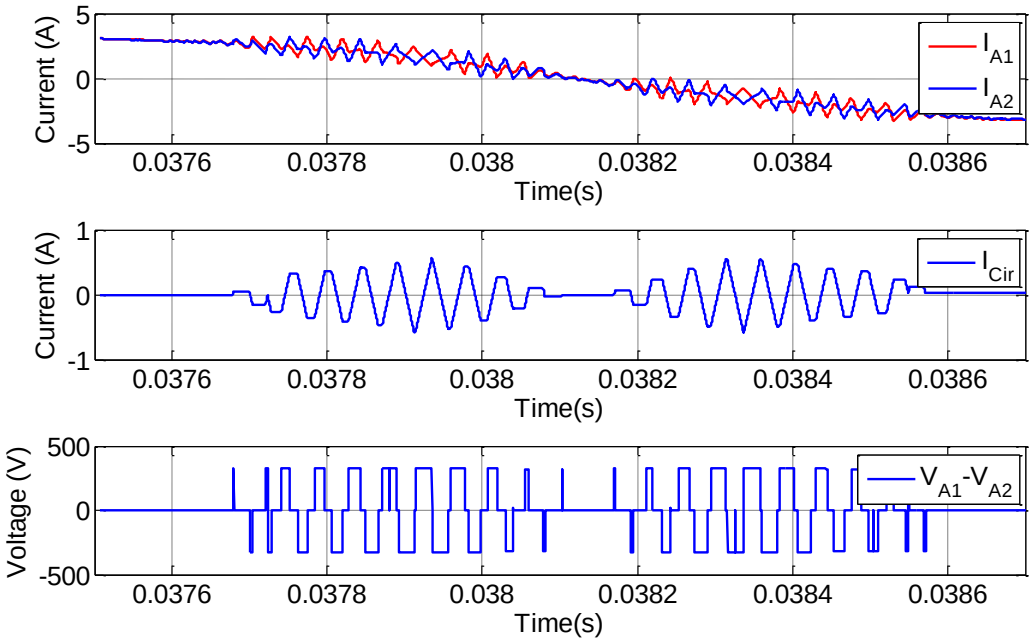
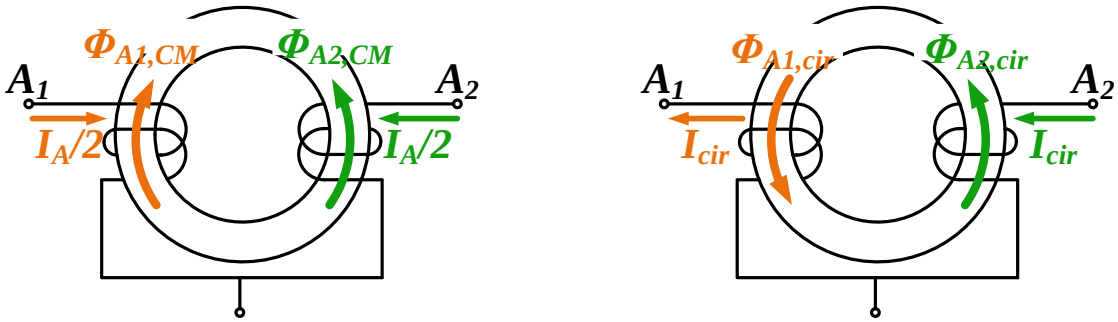


Fig. 41. Simulated current of each sub-converter, circulating current, and the corresponding voltage difference.

If the amplitude of the circulating current is too large, it will not only create additional conduction loss, but also impede the functionality of the converter. E.g. when I_A is positive, point A_1 should be clamped to either the positive rail by D_1 or the middle point of the DC bus by S_1 and S_2. However, if I_{cir} is so high that $I_{A1} = I_A/2 - I_{cir} < 0$, it will be impossible to connect point A_1 to the positive rail when S_1 and S_2 are off. Instead, it will be clamped to the negative rail, resulting in false modulation (Note that the Vienna rectifier is a current-commutated converter, where the operation is highly dependent on the current direction.). Thus, the circulating current in interleaved current-commutated converters should be well controlled.

4.3.2 Circulating Current Attenuation Method

The voltage difference between the two interleaved phases, which causes the circulating current, is inevitable in interleaved converters. In each switching cycle, the voltage difference is predetermined by the modulation scheme and working conditions. Thus, a practical method to attenuate the circulating current is to increase the impedance between the two interleaved points (in this case, A_1 and A_2) at frequencies close to and above the switching frequency. Adding coupling inductors (inter-phase inductors) between interleaved phases (such as L_{MA} for phase A_1 and A_2 in Fig. 40) can effectively increase the impedance of the circulating loop while maintaining only a minor influence on the common current ($I_A/2$) [35]. A physical implementation example of the coupling inductors and the flux in it is shown in Fig. 42.



(a) **(b)**

Fig. 42. (a) Coupling inductor and flux generated by common current (I_A/2). (b) Coupling inductor and flux generated by circulating current (I_{cir}).

It is clearly shown that, in the coupling inductor, the flux generated by the comment current (I_A /2) cancels each other. In other words, the coupling inductor will not affect the current carrying power. On the other hand, for circulating current, the flux generated by the circulating current reinforces each other, i.e. seen by circulating current, the coupling inductor is a real inductor, which adds high impedance to the circulating loop.

4.3.3 Design and Implementation of Inter-phase Inductors

The design guideline for inter-phase inductors in the dual-channel interleaved Vienna rectifier designates that the impedance of the coupled inductors should be high enough so that each sub-converter can work in continuous current mode (CCM). I.e. at any fundamental half cycle, the corresponding phase current stays positive or negative. Otherwise, modulation of the converter may fail. Additionally, because circulating current flows through circuit diodes and MOSFETs, good circulating current attenuation (high coupling inductance) will not only ensure functionality but also reduce semiconductor conduction loss.

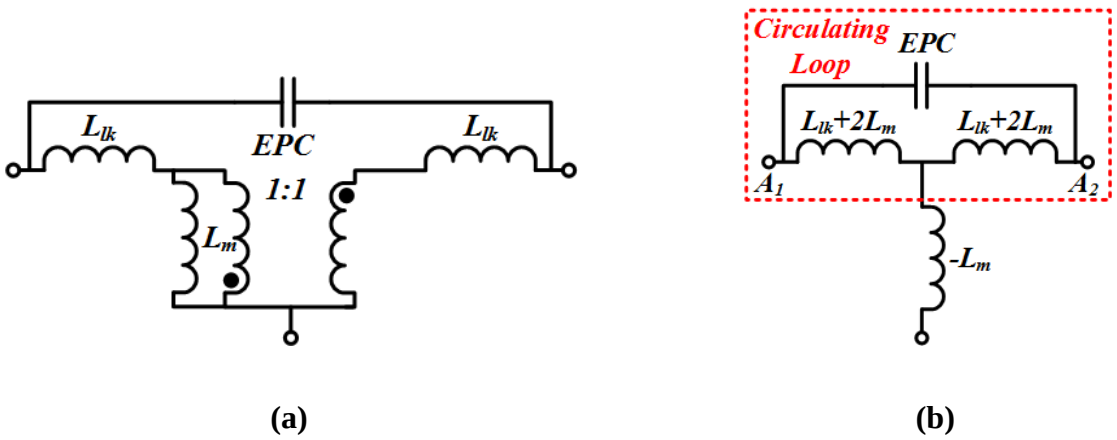


Fig. 43. (a) Transformer-like equivalent circuit of inter-phase inductor. (b) T-shape equivalent circuit of inter-phase inductor.

The equivalent circuit of the coupled inductor is shown in Fig. 43. From the transformer-like equivalent circuit (shown in Fig. 43 (a)), a T-shape equivalent circuit (shown in Fig. 43 (b)) can be easily derived, from which the inserted impedance of the inter-phase inductor is determined. In the equivalent circuit, an equivalent-parallel-capacitance (EPC), which comes from the parasitic capacitance between different layers of windings or capacitance between windings and the core of the inductor, lumped as one capacitor, is also included. At a frequency range close to switching frequency, the influence of EPC can be neglected. This is always true because the total capacitance of EPC is small in general.

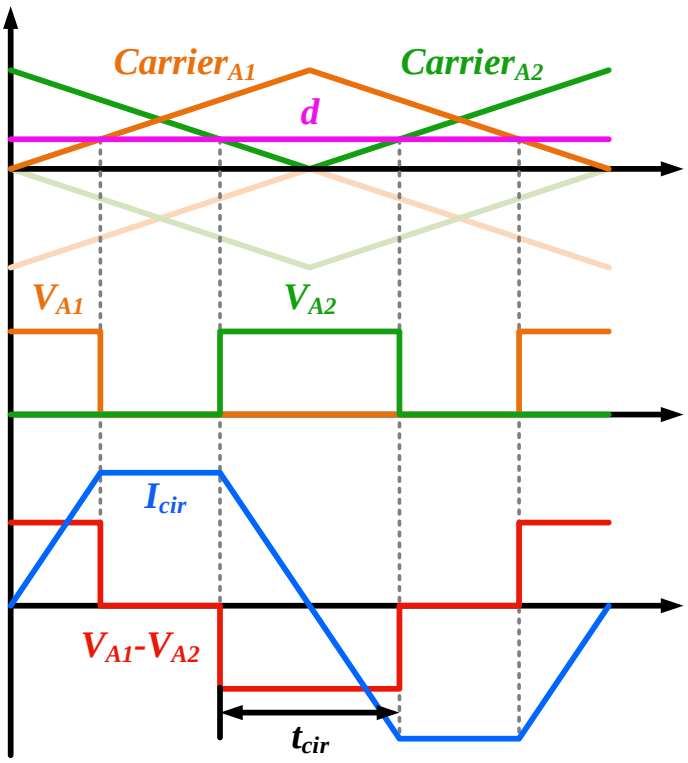


Fig. 44. Relationship between modulation, phase leg output voltage and circulating current.

The detailed waveform of modulator, phase leg output voltages of interleaved phases and circulating current are depicted in Fig. 44. Here, on the first axis, two carriers with 180 ºphase shift between each other are compared with the duty cycle given by the controller. The comparing result is used as gate signals for the two phase legs and the voltage outputs of the two interleaved phase legs, V_{A1} and V_{A2}, can be got correspondingly (shown on the second axis). The voltage difference that causes circulating current can be got based on V_{A1} and V_{A2}, and the relationship between the circulating current peak and the voltage applied across A_1 and A_2 ($V_{A1} - V_{A2}$) is as follows:

$$| I_{cir,peak} | = \frac{| V_{A1} - V_{A2} | \frac{t_{cir}}{2}}{4L_m + 2L_{lk}} \tag{25}$$

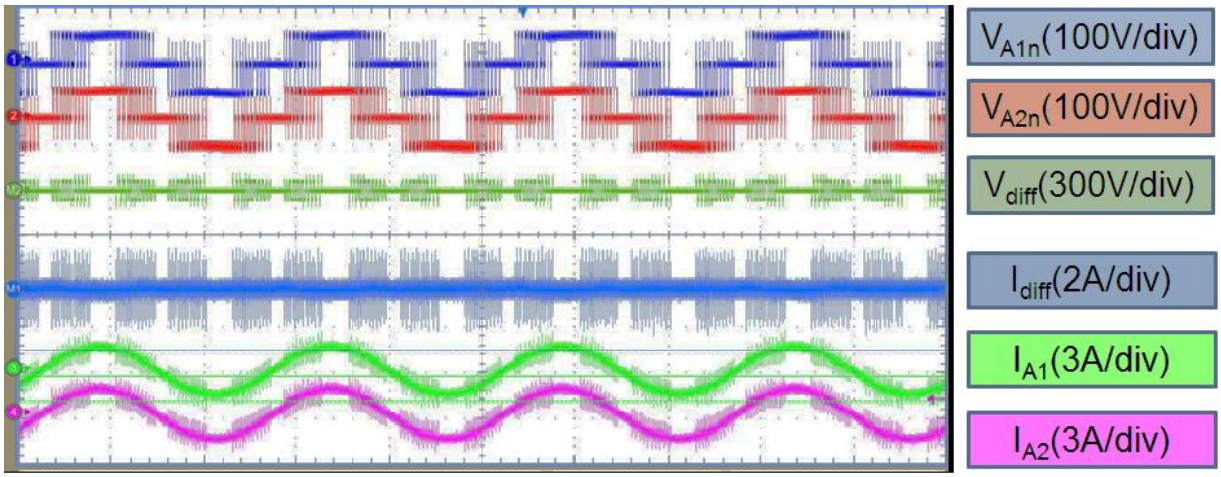
where $I_{cir,peak}$ is the circulating current peak value, $V_{A1,}$ VA_2 are the voltage outputs of the interleaved phase legs referring to the DC bus middle point, t_{cir} is the duration of positive (negative) voltage difference within a certain switching period, and L_m and L_{lk} are magnetizing inductance and leakage inductance of the inter-phase inductor respectively. $V_{A1} - V_{A2}$ will always be half of the DC-link voltage. However, in different switching periods, t_{cir} varies quite a bit. To ensure that the circulating current is always smaller than the input current within any switching period, the inductance of the inter-phase inductor in a certain switching period should satisfy:

$$| I_{cir,peak} | = \frac{| V_{A1} - V_{A2} | \frac{t_{cir}}{2}}{4L_m + 2L_{lk}} < | \frac{I_A}{2} | \tag{26}$$

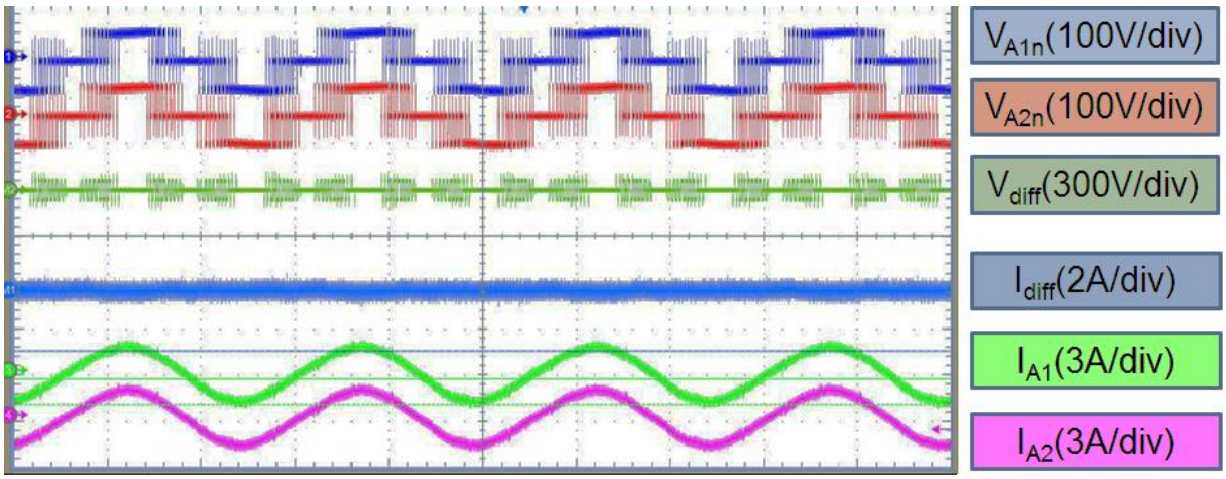
where I_A is the total input phase current of phase A (see Fig. 40) in a certain switching period. The final value for inductance must be greater than the largest value given by (26) when all switching periods within a fundamental period are examined. It should be noted that different modulation schemes result in different volt-second products being applied to the inter-phase inductor, and thus different required minimum inductance values. In addition, this value only sets the lower limit for the inter-phase inductance. In a real implementation, saturation and loss of the inductor should also be considered, which may result in higher inductance designs.

Another important issue in inter-phase inductor implementation is that EPC may not be negligible at high frequencies. While the inductance of the inter-winding inductor increases the impedance of the circulating loop, EPC may have a reverse effect on the total impedance, especially at high frequency. The voltage applied to the circulating loop may contain high frequency components, e.g. drain-to-source voltage ringing when using MOSFET switches (see V_{a1n} and V_{a2n} in Fig. 45,

which are the voltage potentials of point A_1 and A_2 respectively, referring to the middle point of the DC bus). As a result, high frequency current, generated by the high frequency components of the voltage, will flow through EPC and circulate between phases (shown experimentally as the high frequency spikes of I_{diff} in Fig. 45 (a)), which may impede the functionality of the converter. To avoid this, the system's winding structure/geometry is critical. In general, bifilar winding has higher EPC than non-bifilar winding. Moreover, additional coupled inductors, with superior high frequency characteristics (lower EPC), can be inserted in series with the original inductor to attenuate the high frequency circulating current. Circulating current with an additional high frequency coupled inductor to mitigate the impact of EPC is shown in Fig. 45 (b).



(a)



(b)

Fig. 45. (a) Waveforms without enough impedance in the circulating loop at high frequency. High frequency ringing can be observed on I_{diff} (the difference between I_{A1} and I_{A2}), I_{A1} and I_{A2}. (b) Waveforms with high impedance inserted at high frequency. I_{diff}, I_{A1} and I_{A2} are less distorted.

4.4 Converter Design Procedure, Loss Estimation and Implementation

4.4.1 Converter Design Procedure

Converter efficiency is the major concern in this work. The efficiency-oriented design procedure for a dual-channel interleaved Vienna rectifier is described as a flow chart diagram in Fig. 46.

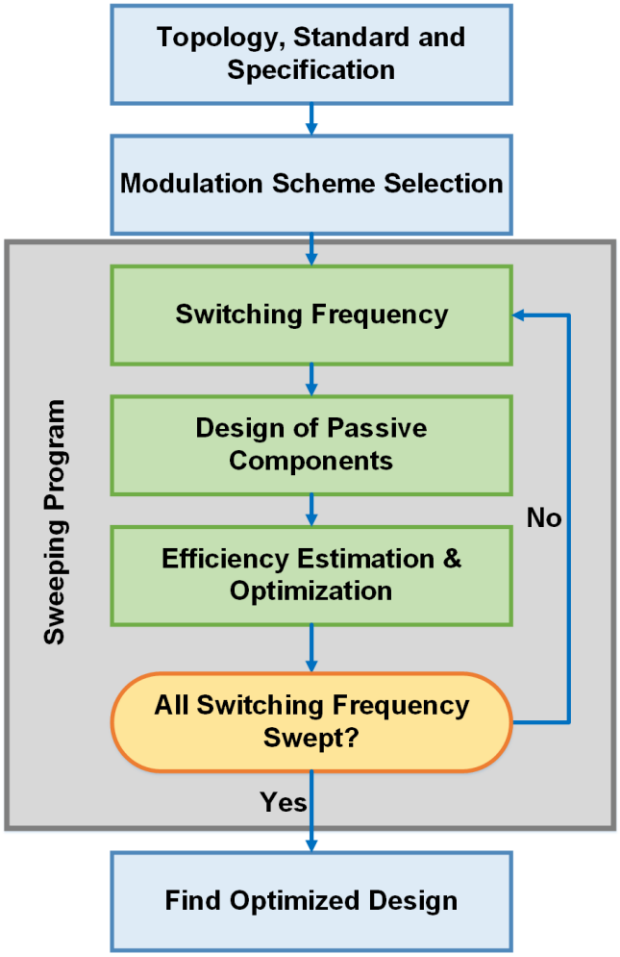


Fig. 46. Efficiency-oriented design procedure for a dual-channel interleaved Vienna rectifier.

This procedure starts with specifications and standards of the converter. To reduce the switching voltage of semiconductor devices while still leaving enough margins for boost-type rectification, the DC bus voltage is selected to be 650 V. The next step is to select the proper modulation scheme for the converter. Then a sweeping program will be run to find the optimized design. The sweeping program starts with switching frequency selection, after which all the passive devices – input boost inductors, inter-phase inductors, and DC bus capacitors – can be designed (constrained mainly by power quality standards) and their loss can be estimated accordingly. Several types of semiconductor devices are considered in this efficiency estimation and optimization. Under a

TABLE X. SEMICONDUCTOR DEVICE CANDIDATES FOR THE DUAL-CHANNEL INTERLEAVED VIENNA RECTIFIER

600 V (650 V) MOSFETs					
Manufacture	Part Number	Current Rating (A)	R_{dson} (mΩ)	Q_{gs} (nC)	Q_{gd} (nC)
Infineon	IPW60R045CP	60	45	34	51
Infineon	IPW60R110CFD	31.2	110	21	64
Infineon	IPP60R199CP	16	199	8	11
1200 V SiC MOSFETs					
CREE	C2M0160120D	17.7	160	6.9	13.6
CREE	C2M0080120D	31.6	80	10.8	18
1200 V SiC Diodes					
Manufacture	Part Number	Current Rating (A)	Q_c (nC)		
CREE	C4D10120A	10	66		
CREE	C4D15120A	15	96		
CREE	C4D20120A	20	130		

certain switching frequency, the conduction and switching loss from all combinations of

semiconductor device candidates (listed in TABLE X) could be analytically calculated. The design achieving the lowest loss will be chosen for the optimized design at this switching frequency. By sweeping different switching frequencies, the relationship between optimized total loss, design of passive components, and switching frequency can be analytically shown and we can determine the optimized design of a reasonable design with the highest efficiency

All the analytical models for loss calculation have been presented in section 2.3.

4.4.2 Converter Loss Estimation

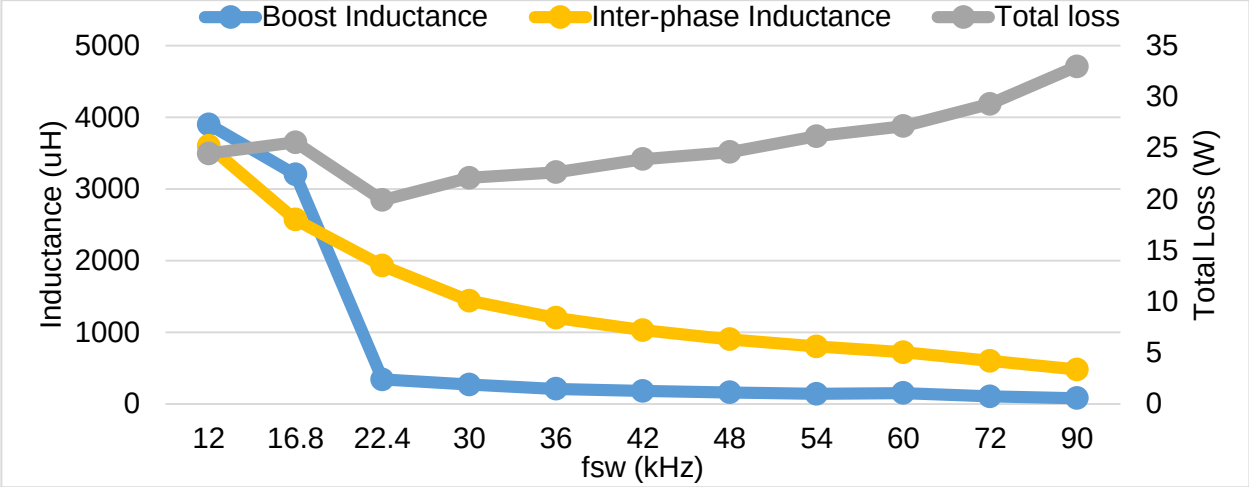


Fig. 47. Relationship between switching frequency and boost inductance, inter-phase inductance, and minimized loss.

Following the design procedure, we can determine the relationship between boost inductance, inter-phase inductance, optimized total loss, and switching frequency of each sub-converter (shown in Fig. 47). The boost inductance required below 22.4 kHz is determined by current harmonic limits. In the higher frequency range, power quality is no longer an issue. (This is true when twice the switching frequency is much higher than the highest frequency in the power quality requirements. In this case, it is 32 kHz.) The boost inductance is designed so that input current

THD is below 10%. To achieve maximum efficiency while maintaining a reasonable size, switching frequency is selected to be 22.4 kHz (estimated efficiency is 99.32%).

4.4.3 Converter Implementation

To achieve the optimized design, boost inductors are implemented using E55/28/21-3C90 cores with 40 turns, achieving 360 μH inductance. Inter-phase inductance is implemented via TX51/32/19-3C90 cores with 42 turns. An additional inter-phase inductor implemented with TX36/23/10 with 4 turns, which helps increasing the high frequency impedance of the circulating loop has been added in series with the big inter-phase inductor. Windings of both types of inductors are implemented with 120/36 litz wire. Based on the loss model presented previously, at 22.4 kHz switching frequency, CREE C4D15120A SiC Schottky diodes and CREE C2M0080120D SiC MOSFETs show the lowest semiconductor loss, and are therefore selected.

4.5 Experiments and Performance Evaluation

In this section, the converter prototype is tested. All testing results regarding functionality of the prototype, efficiency, and thermal performance will be presented.

4.5.1 Constructed Converter Prototype

The constructed converter prototype is shown in Fig. 48. The dimension of the prototype is 8.9 inches * 9.4 inches * 1.5 inches.

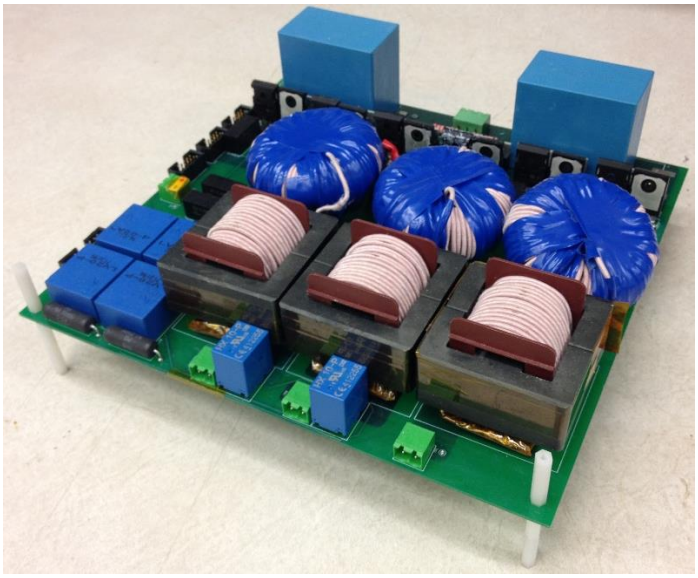


Fig. 48. Converter prototype of dual-channel interleaved Vienna rectifier.

4.5.2 Converter Testing and Evaluation

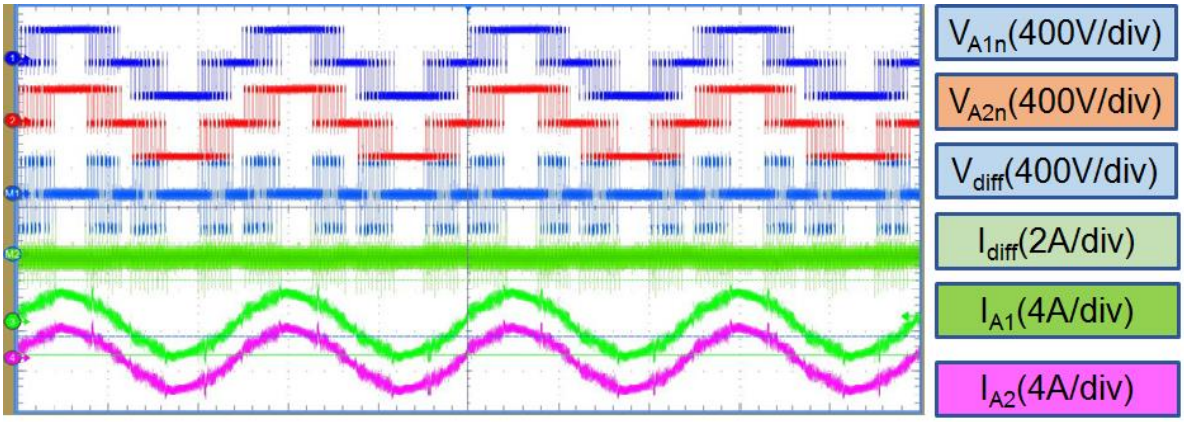


Fig. 49. Experimental waveforms of converter prototype under nominal load.

Experimental waveforms at nominal output power are shown in Fig. 49, where V_{A1n} and V_{A2n} are the voltage potentials of A_1 and A_2 (marked in Fig. 40. Circulating current generation mechanism.Fig. 40) and in reference to the DC bus middle point respectively. V_{diff} is the voltage difference between the two voltages, and is the cause of the circulating current. I_{A1} and I_{A2} are the

input currents of phase A_1 and phase A_2 (marked in Fig. 40). Their difference is shown as I_{diff}, which has been attenuated by the inter-phase inductor, and which stays close to zero.

Efficiency of the converter at nominal output power as measured by the Yokogawa PZ4000 power analyzer is 99.26%, which matches well with the efficiency estimated (99.32%) by the loss calculation method described previously.

The calculated loss breakdown at nominal load is given in Fig. 50. As can been seen, the total loss is dominated by diode conduction loss and MOSFET switching loss. Due to the interleaving structure, theoretically, the loss should be distributed among paralleled devices, which helps with reducing temperature rise of the devices.

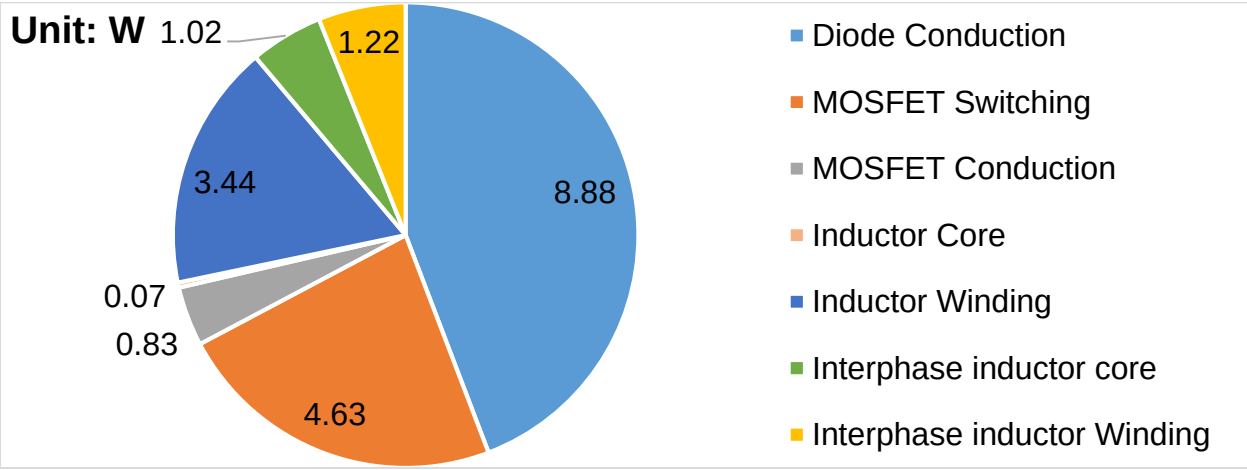


Fig. 50. Calculated loss distribution of interleaved Vienna rectifier at nominal load

The device temperature is measured with both a thermocouple and a thermal camera. At nominal power, and at ambient lab conditions, without any active cooling, the temperature distribution of the converter prototype is shown in Fig. 51. Measured with a thermocouple, the case temperatures on the diodes and MOSFETs are 53 ℃ and 74 ℃ respectively at steady state. Measured with a thermal camera, case temperatures on the diodes and MOSFETs are 61 ℃ and 73 ℃ respectively

at steady state, which is considered safe for the devices to work properly. This indicates that no active cooling is needed for the converter prototype. Moreover, if the ambient temperature reaches 70 ℃, with the same temperature rise tested under lab ambient temperature (29 ℃ on MOSFET and 50 ℃ on diode), the estimated device temperature (99 ℃ on MOSFET and 124 ℃) is below the temperature limit of both devices.

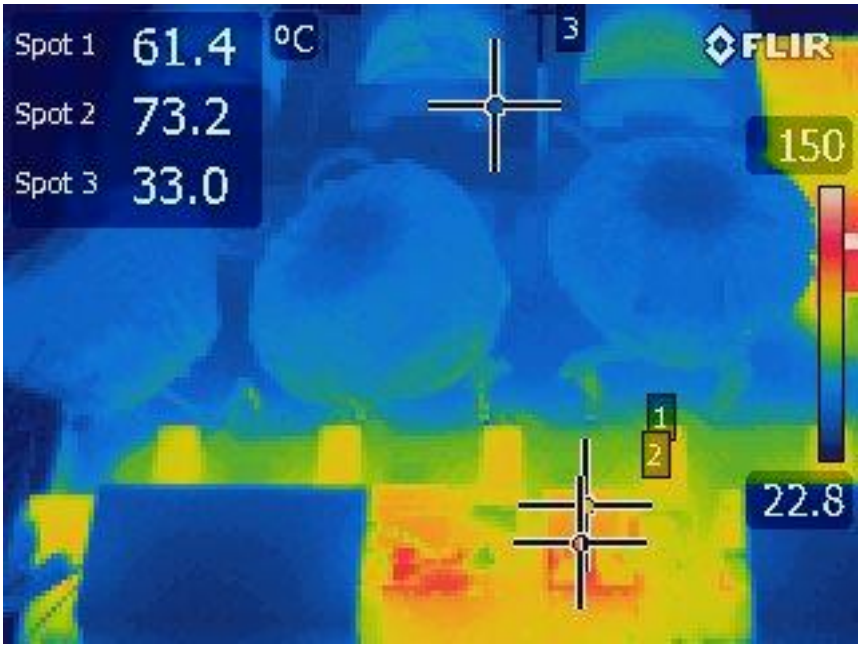


Fig. 51. Temperature distribution of the converter prototype.

Chapter 5. Summary

The design and optimization of AFE converters fed by an aircraft variable frequency AC source (single-phase/three-phase, 230 Vac) is presented in this report. The main focus of this work is to achieve extreme converter efficiency through advanced converter topologies and design.

In this work, the design and optimization of a single-phase PFC rectifier is discussed first. Four different topologies (the two-level semi-bridgeless PFC boost rectifier, the three-level bridgeless PFC rectifier, and their interleaved versions) are included in the topology evaluation. To begin, the operation principles of all the converters get a complete introduction, with special attention paid to the operation principle and modulation scheme of the three-level bridgeless PFC rectifier and interleaved converters. In order to analytically estimate the converter loss, a linear model for MOSFET switching loss calculation and a simulation-based loss calculation are developed. Based on these methods, the total loss of a converter with a certain design can be analytically predicted. An efficiency-oriented design procedure for this application is proposed accordingly, where the converter losses of different designs are analytically calculated and compared, thereby finding the most efficient and practical design. Assuming the condition that all converters are designed such that they achieve the same input power quality, the efficiency of their optimized designs are calculated and compared. Among the optimized designs of different topologies, the interleaved three-level bridgeless rectifier achieves the highest efficiency due to the low switching loss and low MOSFET conduction loss under interleaving operation. Under the specified working conditions, the three-level rectifier (non-interleaved) achieves a much smaller switching loss than its two-level counterpart while having comparable conduction loss. This makes the three-level

bridgeless rectifier and its interleaved version a promising topology in applications where both high efficiency and high power density are desired.

For the three-phase application, three topologies (the two-level boost rectifier, the three-level NPC rectifier, and the Vienna rectifier) are evaluated. The operation principles and commutation of different topologies are introduced first. In order to achieve high efficiency, modulation schemes for three-phase converters are discussed and DPWM is selected for boost-type rectifiers as it can effectively reduce switching loss by proper selection of space vectors. However, for Vienna rectifiers, due to the "current-commuted" property, DPWM should be modified to ensure proper modulation. Two DPWM schemes for the Vienna rectifier are introduced and that which helps achieve the lower switching loss is selected for this work. Based on the analytical loss calculation method developed for single-phase converters, a similar design procedure, aiming at maximum converter efficiency, is developed for three-phase converters. A comparison of the optimized designs of different topologies shows the advantage of the Vienna rectifier in achieving high efficiency. Therefore, the Vienna rectifier is selected to be the basic converter to be built for this work.

In order to further increase efficiency and thermal performance, a dual-channel interleaved Vienna rectifier is designed, constructed, and tested. In this part of the study, the operation of the interleaved Vienna rectifier is introduced with specific attention paid to the generation and attenuation of the circulating current. A complete design procedure for inter-phase inductors, which attenuates the circulating current in interleaved converters, is presented. A design procedure geared toward optimized efficiency is proposed, based upon which a converter prototype is built. The experimental results validate the functionality of the interleaved Vienna rectifier and the

design procedure. The specification targets, design and testing results of the converter prototype are summarized in TABLE XI. As shown, the main objectives/specification targets are met regardless of converter dimensions. With proper layout and device selection, the total size of the converter can be shrunk and the target size can be met.

TABLE XI. SUMMARY

Items	Specification Targets/Design	Testing Results
Input Voltage	230 Vac	230 Vac
Output Voltage	650 V	650 V
Output	3 kW	3 kW
Switching Frequency	22.4 kHz	22.4 kHz
Efficiency Achieved at Full Power	Higher than 99%	99.26%
Cooling	Free Convection Air-Cooling	Free Convection Air-Cooling

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