Design, Analysis and Experimental Evaluation of a Virtual Synchronous Machine Based Control Scheme for STATCOM Applications

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ABSTRACT

Because renewable energy sources are environment-friendly and inexhaustible, more and more renewable energy power plants have been integrated into power grids worldwide. To compensate for their inherent variability, STATCOMs are typically installed at the point of common coupling (PCC) to help their operation by regulating the PCC voltage. However under different contingencies, PCC voltage fluctuations in magnitude and frequency may impede the STATCOM from tracking the grid frequency correctly, hence worsening its overall compensation performance, and putting at risk the operation of the power plant. Further, the virtual synchronous machine (VSM) concept has recently been introduced to control grid-connected inverters emulating the behavior of rotating synchronous machines, in an effort to eliminate the shortcomings of conventional d-q frame phase-locked loops (PLL).

In this dissertation, the VSM concept is extended by developing a STATCOM controller with it, which then behaves like a fully-adjustable synchronous condenser, including the adjustment of its “virtual” inertia and impedance. An average model in two D-Q frames is proposed to analyze the inherent dynamics of the VSM-based STATCOM controller with insight into impacts from the virtual parameters and a design guideline is then formulated. The proposed controller is compared against existent d-q frame STATCOM control strategies, evincing how the VSM-based approach guarantees an improved voltage regulation performance at the PCC by adjusting the phase of its compensating current during frequency fluctuations, in both simulation and experiment.

Secondly, the dynamics of the VSM-based STATCOM controller in large signal sense is studied, especially its capability to ride through faults. Analysis is carried out with phasors to obtain a fundamental understanding at first and followed by state space equations to predict the transients analytically, which is validated by matching both simulation and experiment. The effects of two outer loops are also reviewed and some possible solutions are suggested and evaluated. Moreover, the relationship between the virtual inertia and the actual inertia is established and the

dc capacitor sizing is discussed in a possibly more economical way. The start-up process of a VSM-based STATCOM is presented to implement a practical prototype as well.

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Chapter I. INTRODUCTION

1.1 Background

Faced with more and more severe environment pollution and fossil resource scarcity, people have been seeking renewable and green energy, wind and solar mainly for now, to increasingly support power generation in the existing power grid. Many countries have promulgated acts and policies to encourage research and deployment of renewable energy and as a result the number of wind and solar farms is growing significantly in recent decades. However, due to less control over renewable sources, the output power can be unpredictable because they are often running in the maximum power point tracking (MPPT) mode. This randomness together with their lack of inertia, or spinning reserve, makes renewable energy not preferable from the grid's point of view due to the potential source-load power imbalance, uncertainty of operation and potentially harsh transients.

Additional compensation is often necessary to ensure a safe and economic operation when connected to the grid; e.g., it is a common solution to use STATCOMs to compensate large wind or solar farms to help the point of common coupling (PCC) voltage regulation and also enhance stability during transients. Compared to other applications of STATCOMs, compensation of renewable energy present interesting challenges not only because of the uncontrollable and random nature of the sources, but also due to the typically weak grid conditions since large wind or solar farms are often located in remote areas. When there is a grid contingency such as sources or loads switching in or out and single-phase or three-phase faults and also when the output power of renewable energy is fluctuating, variation in magnitude and frequency of PCC voltage as well as harmonics and unbalance is often observed, which prevents STATCOMs from tracking the PCC voltage accurately and thus influences the regulation performance of the latter.

In recent years, the virtual synchronous machine (VSM) concept has been introduced [1], as well as virtual synchronous generator (VSG) [2], or synchronverter [3, 4] and power synchronization control [5], inertial emulation [6] and synchronous power controller [7], which controls grid-connected inverters emulating the behavior of conventional

synchronous machines to obtain a better, grid-friendly transient response, and has been proposed primarily as a means to replace d-q frame phase-locked loops (PLL) that oftentimes introduce problems in their operation. Although the main concept proposed is the same in [1-3, 5-10], fundamental aspects and modeling details differ significantly between these approaches as different orders of differential equations of synchronous machines are used [9]. Regardless, the two main benefits of VSM-based control are power-based synchronization, which eliminates the PLL [4] and its potential instability [11], and virtual inertia, which is programmable during disturbances to achieve faster response than physical synchronous machines. As such, the key advantage of VSM type controllers over d-q frame controllers is the way to synchronize, where VSM-type remains inherently in harmony with the electrical system, while the d-q frame controller relies on the PLL to orient its control system and operation. This property prevents VSM type controllers from fighting with each other and running into instability, improves the transient responses when contingencies happen, and can remain stable even under islanding conditions.

There are different approaches of the concept, some using virtual inertia only [1, 2, 5, 6, 10], some adding virtual impedance also [7] and some implementing the full model of a synchronous machine [3]. Virtual impedance and virtual inertia will be implemented in the strategy proposed in this article to make the STATCOM operate as a variable synchronous condenser. With virtual inertia, the STATCOM will naturally synchronize with the grid accurately if there is any change in the frequency without any risks of losing synchronization. Virtual impedance can limit the harmonic produced by the converter itself and also reject that from the system ensuring immunity under harmonic perturbation, where additionally negative sequence impedance can be added to enhance the response in case of unbalanced phase voltages exists in the system; e.g., during asymmetrical faults. In such way, the VSM-based STATCOM will be less sensitive to power or voltage fluctuation induced by renewable energy sources or the grid itself, featuring better synchronization performance and thus achieving an improved voltage regulation than the conventional STATCOM controlled in the d-q frame. Furthermore, the VSM-based STATCOM can actively adapt to different scenarios using its adjustable “virtual” inertia and impedance. Furthermore, the VSM-based STATCOM can actively adapt to different scenarios using its adjustable “virtual” inertia and impedance.

1.2 Synchronization for grid-interfaced converters

For converters that interface with the ac power grid, synchronization is the fundamental task before other functionalities are implemented. In order to work together with each other, the same frequency with appropriate phases is essential either achieved by obtaining phase information from the system or by participating in the frequency regulation.

1.2.1 Phase locked loop

Typically a phase locked loop (PLL) serves to bridge a converter to a power grid, using different mechanics from the way how the dominating synchronous machines or generators stay synchronized in harmony naturally in the existing power system. A synchronous reference frame PLL (SRF-PLL) is easy to use and present a good performance on ideal occasions and many other enhanced PLLs have been proposed to get a better behavior against harmonic and negative component disruption. A traditional way is to use PLL based on synchronous reference frame, which translates the 3-phase sinusoidal voltage in abc frame into dc voltage in d-q frame in the steady state by Park's transformation [12]. A compensator is designed for a feedback loop to regulate the q channel component into zero, as shown in Figure I-1. The structure is simple to implement and however it may present some instability when multiple grid-connected converters are connected together as shown in [11, 13].

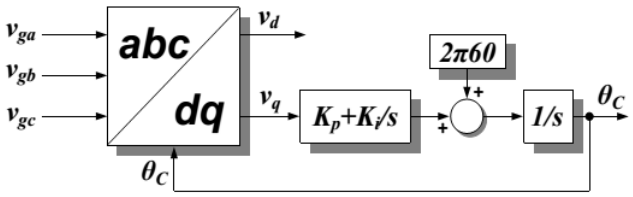

Figure I-1 Control blocks of SRF-PLL

1.2.2 Power-balance-based synchronization

The VSM and other similar concepts share the same method to synchronize, which is derived from the Newton's Law and called swing equation (1) describing the movements of an imaginary rotating shaft in Figure I-2 (a) corresponding to a 3-phase converter in Figure I-2 (b)

$$\begin{aligned} \frac{d\delta}{dt} &= \omega - \omega_n \\ M\frac{d\omega}{dt} &= P_{dc} - P_{ac} - D(\omega - \omega_n) \end{aligned} \quad (1),$$

where δ is known as the power angle, ω and ω_n are the detected frequency and grid frequency respectively, M and D are virtual angular momentum and virtual damping coefficient, P_{dc} and P_{ac} are input active power from dc side and output active power from ac side of the converter respectively. In that sense, the imaginary shaft is rotating at the speed ω which is driven by P_{dc} and braked by P_{ac}.

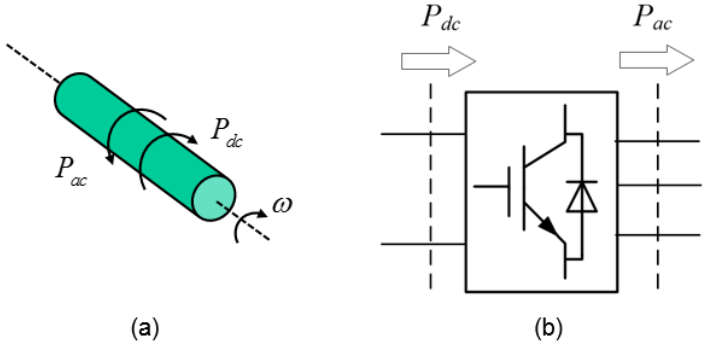

Figure I-2 Virtual synchronous machine concept

The dc input power is often a controllable variable and remains constant if no commands are given while the ac output power is determined by the power transfer equation

$$P_{ac} = P_{\max} \sin\delta \quad (2),$$

where P_{max} is a constant relative to the operating condition. If ω is greater than ω_n, δ and thus P_{ac} will become larger, and then ω will be decreased by the unbalance of input and output power, and vice versa. In the steady state, the two power will be equal and the frequency will be eventually the grid frequency and hence the converter is synchronized with the grid. If (1) is implemented in the controller for the converter, the synchronization behavior will be exactly the same with the rotating shaft, showing an emulation of synchronous machines. A basic structure of VSM based controller is depicted as Figure I-3 Control blocks of basic VSM controller with only virtual inertia presented where the transfer function G_{plant} represents the power transfer equation (2).

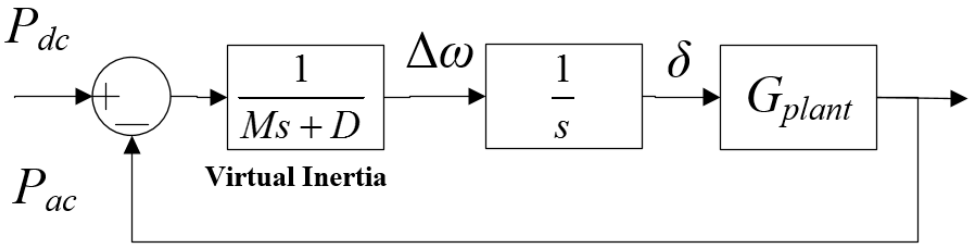

Figure I-3 Control blocks of basic VSM controller

1.3 Motivation and outlines

The virtual synchronous machine concepts have been proved in various references [1-3, 5-9] that it shows no worse response than the traditional D-Q frame PLL-oriented controllers and much greater behavior when it comes to islanding mode with the capability to enhance the stability of the power system. Indeed, the main benefits for VSM-controlled grid-interfaced converters are the friendliness to the grid and the ability to participate and even support the grid frequency and voltage. However in existing papers, many researchers have only proposed their concepts lacking in the analysis and insights into the basics of this kind of control methods and basically there is no complete design procedure. There is more to be done to explore the potentials of this methods by playing with programmable parameters which determines the output characteristics under different kinds of transients. It is necessary to look into the state-space equations or transfer functions to know what the impacts from the virtual parameters is.

Additionally, most of the papers are focused on inverters with the dc side connected with either PV panels, battery systems or HVDC ends [6, 14-20], while only one [21] has applied the idea to STATCOM but no details have been offered. The benefits of using VSM control in the STATCOM application over the conventional D-Q frame one has yet to be shown to demonstrate the advantages.

In such, the thesis will go as the following:

Chapter 2 gives an introduction of STATCOMs. The basic operation, conventional control schemes, typical applications and common topologies are presented.

Chapter 3 offers a review of virtual synchronous machine control concept and classifies all methods based on their control structure. Some existing applications are also provided.

Chapter 4 explains the VSM control application to STATCOM and offers small signal analysis given operating points based on proposed two D-Q frames, namely the system D-Q frame and the controller D-Q frame. From that the transfer functions can be obtained and parameter choices can be made with comparison with conventional D-Q frame controllers in both frequency and time domain. The VSM controlled STATCOM shows similar voltage regulation performance when there is only voltage variation in the system but a much better performance when the frequency is fluctuating. The design rules are based on trade-offs. Then a prototype STATCOM with both VSM and D-Q frame controller implemented. The control methods are verified in the hardware experiments. Without a synchronous generator running, the tests are limited with voltage fluctuation being the only case conducted. Also a larger power system with 4 generators divided into 2 areas with 2 tie lines connected where the power system is more practical to study the influence of the VSM controller. Similarly transient responses are compared between VSM and D-Q frame controllers and the same conclusion is extended to this test case.

Chapter 5 first describes a possible issue of the VSM controller during large transients, which is intrinsic in this control method and may lead to voltage collapse. A phasor explanation is given to show the nature behind and analytical analysis based on non-linear differential equations is provided to predict possible phenomenon. Moreover, some feasible solutions are proposed and compared to overcome the limitation of the VSM controller. This chapter is an addition to Chapter 2 as a consideration of large transients as well as a must to check if the STATCOM can sustain after given faults.

The last chapter summaries the work and discusses some possible future work.

Chapter II. BASICS OF STATIC SYNCHRONOUS COMPENSATORS

2.1 Basic operation of STATCOM

This kind of advanced compensator is based on converter composed of force-commutated power electronic devices and topology, first proposed by Gyugyi in 1979 [22]. Although the DC source of STATCOM can be both current and voltage, the most practical and used one is voltage source converter (VSC), shown in Figure II-1, along with its basic operation mode.

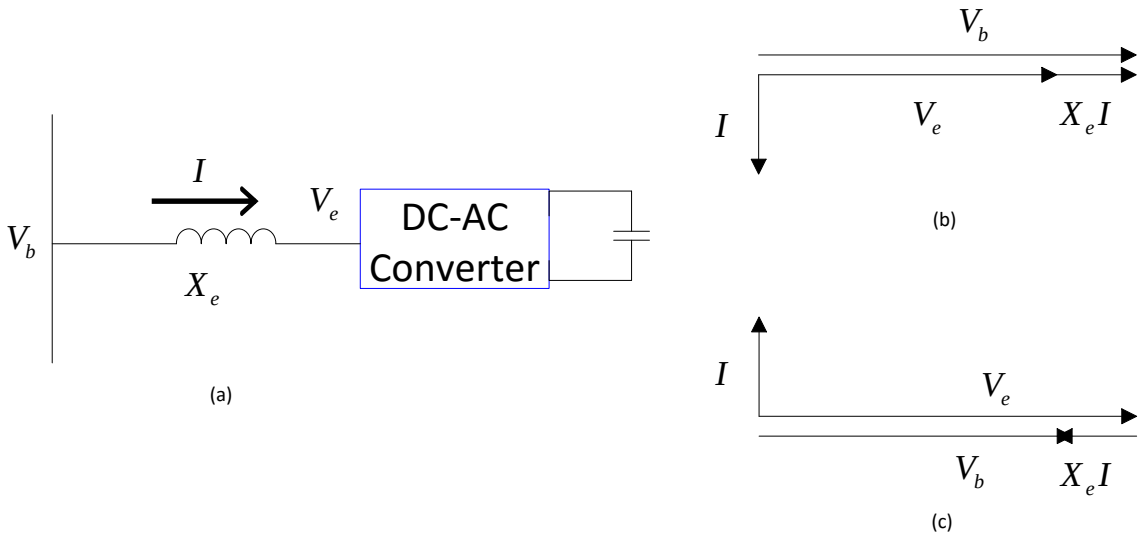

Figure II-1 Basic concept of STATCOM: (a) basic topology of STATCOM; (b) inductive mode; (c) capacitive mode

The VSC-STATCOM generates an AC voltage V_e $V_e$and shunt connects to the bus with the voltage V_b V_b via an equivalent inductance $X_e$$X_e$, which is often the leakage inductance of a transformer, where all the values are reflected to the primary side of a transformer. By controlling the output voltage of the converter by either firing angles or DC link voltage, it is easy to obtain a continuously controllable V_e $V_e$to control the compensating current and thus the reactive power compensation. The capacitor at DC side can be regarded as a reactive power source in a STATCOM. In practical applications, the losses of a STATCOM are compensated by the power system, that is, the STATCOM will

draw a little active power from the grid, which results in a small phase lag of the output voltage V_e.

Figure II-2 shows how STATCOM works to compensate by adjusting its output voltage. The solid lines describe the V-I characteristics of the STATCOM with the output voltage V_{e1} and the grid, where the intersection shows the operating point at the present with the bus voltage V_1. If the system voltage drops suddenly and therefore the bus voltage decreases to V_2', the STATCOM will be controlled to increase its output voltage to V_{e2} and obtain a new V-I characteristic to reach a new operating point with the bus voltage V_2. As Figure II-2 shows, V_2 is greater than V_2' and could be even greater than V_1 based on the compensation capability of the STATCOM and the system condition. In such way the bus voltage change is compensated.

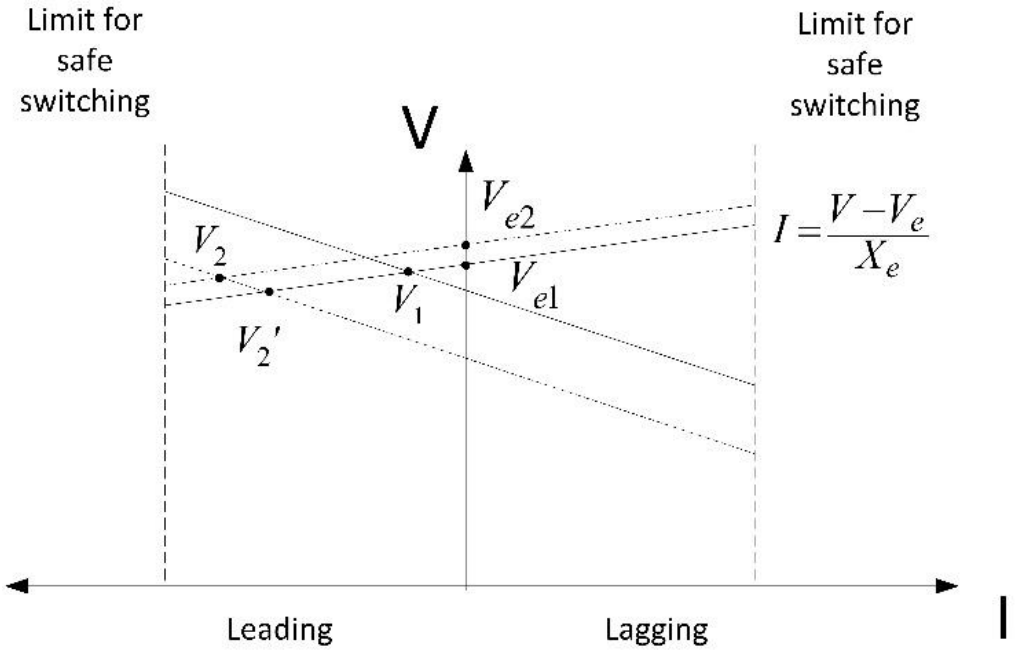

Figure II-2 Operating characteristics of STATCOM

2.2 Conventional STATCOM control

2.2.1 ABC frame control

A method that was common to control STATCOMs with GTOs or thyristors is based on abc frame, where the modulation index and the firing angle are the two controllable

variables. The modulation index *MI* is to adjust the output voltage magnitude, whose command is given by the ac bus voltage compensator. The firing angle α, that relates the active power transfer between the STATCOM and the grid, controls the dc bus voltage to keep it constant. Those two outputs of the controller are often synthesized into a sinusoidal reference voltage to generate the gate signal using sinusoidal pulse width modulation (SPWM) technique. This method is straightforward and simple to fulfill the requirements brought by the low switching frequency, which is mostly replaced with more complex controllers using advanced switching devices with higher switching frequency.

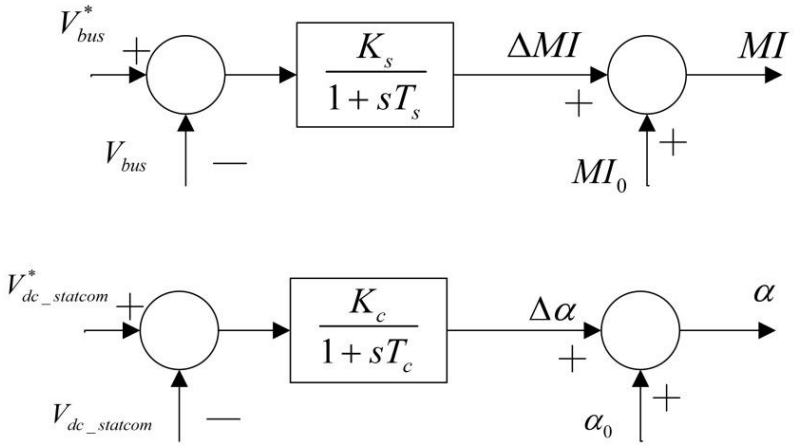

Figure II-3 ABC frame STATCOM controller

2.2.2 D-Q frame PLL-oriented vector control

The controller of a STATCOM in D-Q frame is built as a conventional cascaded controller with an outer voltage loop and an inner decoupled current loop to generate duty cycle *d* to the converter shown in Figure II-4, where superscript * stands for references and subscript d or q represents the corresponding variables in D-Q frame transformed from abc frame using the angle θ generated by the PLL as introduced in 1.2.1, as can be found in many references [23-25]. The PLL is a traditional synchronous reference frame PLL, which senses the q axis PCC voltage and regulates it to be zero. The inner current loop is decoupled in D-Q frame and to regulate the grid side current of the output filter where the d channel voltage loop providing the d channel current reference is to regulate the dc-link bus voltage of the STATCOM and q channel voltage loop giving command to q channel current reference is to regulate the PCC bus voltage. All the regulators in these loop are simple PI regulators without loss of generality, which are most common used in industry.

In order to damp the influence of synchronization due to possible grid voltage disturbances, the bandwidth of the PLL is often chosen to be relatively low. The inner current loop should be fast to ensure large frequency range under control but limited by the switching frequency. After obtaining the output voltage, space vector modulation (SVM) is usually used to generate the PWM signal to drive the converter.

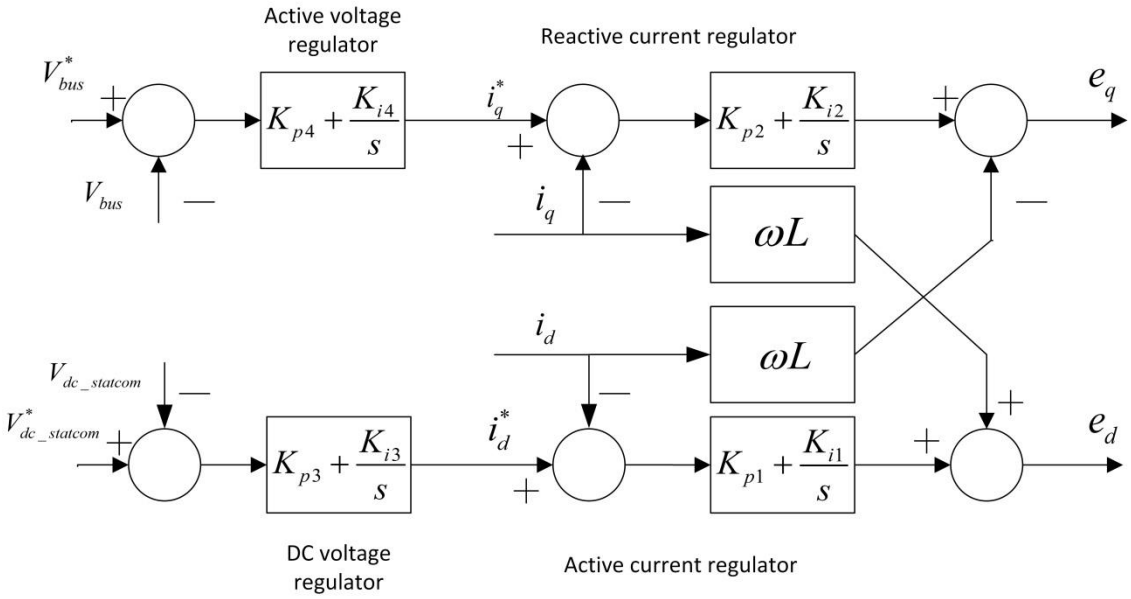

Figure II-4 D-Q frame PLL-oriented STATCOM controller

2.2.3 Effect of PLL

Since the PLL measures the grid voltage and tries to synchronize with this waveform, any disturbances in the grid voltage will propagate into the PLL loop. Furthermore because the Park transformation used to convert variables in abc domain into d-q domain is determined by the phase angle θ generated by the PLL, the disturbances will flow into not only the current references and also the duty cycles. The idea and explicit analytical model was presented in [11, 13, 26, 27]. While the PLL affects negligibly the transfer functions from duty cycle to current and from q channel current reference to PCC bus voltage, the most important impact of the PLL, especially its bandwidth, is on the ac impedance of the converter in d-q frame, which implies the small-signal stability of the system by studying the phase difference at the frequency where the source and load impedance intersect in qq channel. As stated and demonstrated in [26, 27], the criterion of stability relies on the ac impedance in the qq channel of the source and the load, and the bandwidth of PLL only

affects the impedance in the D-Q and qq channels. It indicates that PLL plays a key role in the small signal stability of a grid-connected inverter and the lower bandwidth of the PLL, the more phase margin in the qq channel.

2.3 Functionalities and applications

It is the control schemes that play the most important role in the operation of a STATCOM which decide the performance and behavior to any condition from one application to another. Almost all the control strategies are based on time domain other than frequency domain because the frequency domain methods consume huge time for computation and are thus not fast enough for the dynamic response. And among the time domain control approaches, transforming the three-phase variables into the D-Q synchronous rotating frame is very popular because the sinusoidal variables become dc values, which makes it easier to control using a low pass filter to extract the dc signals while it is advantageous to control in the abc frame under some certain cases. Based on different time scales, the STATCOM applications can be classified into stability issues, voltage regulation and long term issues, which will be discussed in details respectively below.

2.3.1 Stability issues

2.3.1.1 Small signal stability

Dynamic analysis required by the stability issues has always been challenging to power engineers for a large and complicated power system, for example, a power system under high penetration of renewable energies because for now there are no fast and robust enough mathematical solutions, either analytical or numerical, to a set of large quantities of highly nonlinear differential equations. Therefore at present, researchers are focusing on different specific cases and proposing solutions based on some given system topology and faults.

Power system oscillation damping is referred to the damping of inter-area oscillations with frequency 0.2 Hz to 2.0 Hz due to the development of interconnection of large power systems, which may cause stability problems. With faster response than major electric power plants, the capability of FACTS devices to suppress power system oscillations and

thus to increase system stability has been explored in many aspects. As achieving power flow control, a dynamic model for FACTS devices is necessary. The dynamic model is often a state-space model linearized around a given operating point and the damping is achieved by the FACTS device stabilizer (FDS) which is installed as a higher level local controller to control the effective active or reactive power output according to the command of a grid level global or local controller [28-43]. Chong Han etc. [44] conducted an impact study of a STATCOM in a 12-bus power system with two large wind farms connected and from the PV and VQ curves obtained from the simulation the article discussed the size and location of the STATCOM to ensure enough stability margin. The results showed that the STATCOM is minimized in size without losing its controllability when it is located right at the PCC, which is found out to be a common place to install the STATCOM. Nadarajah Mithulananthan [41] looked into the typical electromechanical oscillations and used Hopf bifurcation theory to study the influence of different controllers, locations and control signals. The PCCs of the renewable energies are often shown to be the critical point to maintain the voltage profile of the whole power system, which demonstrates Chong Han's results to some extent, although the choice of the placement still needs carefully investigating case by case [45, 46].

To simplify the problems as for local dynamic stability analysis where the part without renewable energies of the grid is simplified as a voltage source with a reactance, the impact of the STATCOM was studied with more detailed models of both the renewable energy and STATCOM. In [47], Pranesh Rao derived the state-space model of the STATCOM in the D-Q frame and compared various state feedback controllers where all the variables are local and thus accessible, lending background to many following papers. Woei-Luen Chen etc. and Li Wang etc. both used modal control theory to place the eigenvalues of the state models of the local system they derived to achieve desired damping effects with state feedback control [48-50]. After designing the structure of the control loops, the eigenvalues of the state model with respect to the parameters of the controller are placed using a state feedback controller according to the pole placement method or the eigen-structure assignment method to get the maximum damping according to the preset optimum functions and objectives. After acquiring the state-space equations, there are many

controllers to implement to manipulate the transfer functions [30, 32, 34] and thus to improve the steady-state and dynamic responses.

Although this kind of method can attain very accurate control to compensate the PCC voltage because the system is always controllable, it is parameter-sensitive and thus may fail because under some practical cases it is not enough to consider the dynamics of the STATCOM itself but the transients of the renewable energy sources and the grid should be taken into account, whose states and parameters are often not available or attainable but time-varying. Some advanced controllers which have been widely applied in some other FACTS applications [51-55] e.g. hybrid fuzzy control [33], H_∞ control [36], robust control [37], etc. are possible to be adopted in the dynamic stability analysis with renewable energies in order to grant a more robust characteristics.

2.3.1.1 Transient stability

Another important aspect of stability issues especially regarding to the wind farm case is the low voltage ride through (LVRT) capability, concerning the stability of the wind generators interacted with the voltage variance at the PCC [56-58]. During the system faults, the PCC voltage will collapse and there will be not enough reactive power for magnetic excitation for the generators, generating less electromagnetic torque. If the input source is kept constant, the generator will accelerate according to the mechanic equations and finally has to be disconnected to the grid for the safety consideration. And then it may trigger a chain reaction of disconnection of the generators due to the less input power to the grid and eventually result in the whole system collapse. Therefore the reactive power support during and after power system contingency is a critical issue.

However this is very challenging because the small signal model fails during faults with the system highly non-linear. Typically energy function methods are analytical but complex to obtain and solve while the numerical simulation is more common but takes more time with different cases [23-25, 49, 58, 59]. M. H. Haque [40] started from the equal area criterion to propose a control strategy thanks to continuously control capability of the STATCOM to improve the first swing stability limit by adjusting the equivalent damping torque for the generators. On the other hand in [24, 25], Marta Molinas etc. started from the quasi-stationary torque-speed curves of the wind generator to get the similar results.

2.3.2 Voltage regulation

The objective of voltage regulation can be stated as maintaining the voltage as perfectly balanced and sinusoidal waveforms with the designated magnitude and phase. For shunt-connected devices without the ability to provide active power like STATCOM, it cannot change the phase of bus voltage at which it is connected and hence the main function of a STATCOM is the compensation of unbalanced voltage, voltage sags and harmonics. As mentioned before, unbalanced voltage may damage the generators of the wind farm; voltage sags would influence the power flows and harmonics are not allowed to be largely injected into the grid. In order to address these problems, researchers have proposed different kinds of controllers. Most of the controllers have the inner current loop and the outer voltage loop to maintain the voltage at the PCC similar to Figure II-4.

P. S. Sensarma etc. derived a simple circuit model of the transmission line with a STATCOM and presented it in the s domain [60] to get the transfer functions with compensation of PI controllers. The error in the DC bus voltage of the STATCOM determined the reference of the active current in the d axis while the error in the PCC voltage gave the reference of the reactive current in the q axis, which is the routine of the current controller inside the STATCOM in the D-Q frame. Ben-Sheng Chen etc. [61] suggested using Bessel functions to analytically present all the output voltage harmonic components. Based on that it was shown that with high modulation index, the steady-state harmonics generated by the STATCOM could be minimized.

As for unbalanced voltage problems, there have been two kinds of controllers: ones based on the D-Q frame and ones based on the abc frame. To avoid disturbances from voltage distortion to phase, enhanced PLLs are proposed such as frequency locked loop [62], decoupled double synchronous frame PLL [63, 64] or other additional filters [65-67] to drag the positive voltage information. Clark Hochgraf [68] proposed the first papers taking the negative sequence voltage into account and used two control loops respectively for positive and negative voltage after separation by different Park transforms. Bostjan Blazic etc. [69] and Tzung-Lin Lee etc. [70] followed this idea. Bostjan Blazic designed the controllers for both d and q axes in the positive and negative rotating frame from the state-space model while Tzung-Lin Lee devised different virtual impedances for different

sequences. Christian Wessels etc. [25] used resonant controllers tuned at double the line frequency in the positive D-Q frame to realized the negative sequence control shown. Since the negative sequence currents can be performed in a negative rotating reference frame with PI controllers, the resonant controllers can pick up the negative sequence information if the negative sequence variables are transformed into the positive rotating reference frame by a coordinate transformation with twice the grid voltage angle, avoiding the sequence separation seen in the above papers. Proportional and resonant controllers are also implemented in other papers [71-75].

For the controller based on abc frame, Arindam Ghosh and Gerard Ledwich [76] derived the state space model of a STATCOM and used an infinite time linear quadratic regulator (LQR) to tune the feedback controller, which is more robust and performs better under the unbalanced case but lacks the steady-state operating point in the D-Q frame based controllers. Other papers uses instantaneous active and reactive power to generate current references [69, 71, 77-80].

2.3.3 Long term issues

For a longer time scale, the main purpose of the FACTS devices is to fully use the transmission lines and to direct the power flow through the designated paths. Hence STATCOM, as one of the FACTS devices, can be applied to power flow control by lessening the power flows through the heavily-loaded lines and maintaining the critical buses voltage to enhance the stability margin, where an interesting issue is the improvement of the total transfer capability (TTC). The term TTC is to define the amount of power that is available to transfer between interconnected transmission systems in a reliable manner and the term available transfer capability (ATC) is defined as the TTC minus the transmission reliability margin (TRM), the sum of existing transmission commitments (ETC) and the capacity benefit margin (CBM). These two terms are very important to evaluate all the economic transactions and enough TTC or ATC will ensure free market trading and an economical and safe operation under contingencies. The TTC is determined by system's thermal and voltage limits and stability margins [81] and the key of the calculation of ATC is the determination of the TTC.

A common used unified model for FACTS devices is the power injection model (PIM) [82-84] that studies the terminal power flow injection of FACTS devices and makes corresponding modifications to the original power flow equations. PIM can maintain the symmetry of admittance matrix and the Jacobian matrix is updated with only changes of the related buses. After applying the PIM into the conventional power flow program, there are some mathematical methods to compute TTC: transfer-based security constrained optimal power flow method, continuation power flow method, repeated power flow method [81, 85, 86], which intrinsically are all to solve a set of optimization problems, typically maximizing the load in the sink area, with large amounts of non-linear equality and inequality constraints. After obtaining the optimal solutions offline because of the huge computation, the references of the FACTS devices, e.g. STATCOMs, are set to guarantee the desired operation. Basically, the optimization has to be redone if the topology and any source or load changes, which raises the challenge of the fast convergence of the algorithm used.

Considering multiple STATCOMs in a power system, the coordination between them is a critical problem which should be regarded as a higher level control to provide the voltage references for the outer voltage loop. Hai Feng Wang [87] proposed a secondary voltage control of the STATCOMs to fully use capability of the STATCOMs to be the voltage profile agent of the nearby area, in which the STATCOMs behave like servers in the Internet to ask for each other's help and react according to their remaining capability.

2.4 Topologies and configurations

2.4.1 Basic topology

The basic topology is a 2-level VSC, which is shown in Figure II-5. As seen, this is quite simple and straightforward.

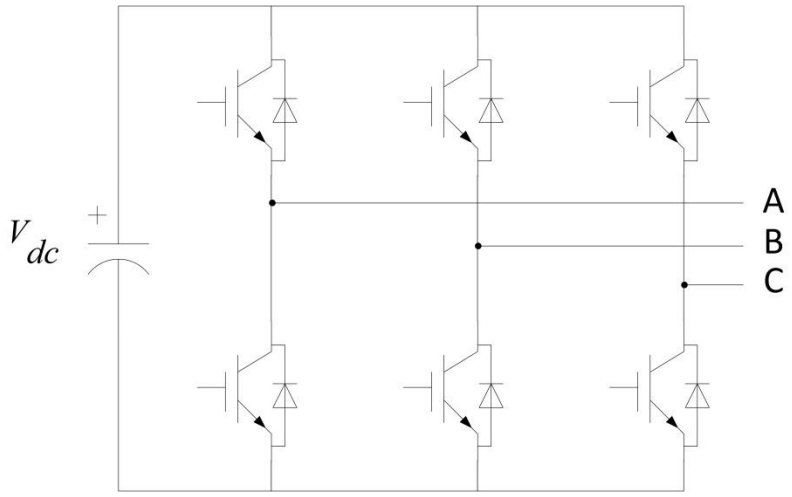

Figure II-5 2-level VSC

If applied in the high power level scenarios, the switching devices must be of high power rating such as IGCTs, GTOs or even thyristors working at the line frequency to produce quasi-square waveforms. This leads to a very high THD and the harmonics are not allowed to be directly injected to the grid. Researchers have made some improvement to reduce harmonics [88, 89], but the effects are not very evident compared to the following topologies. Therefore at the present, VSC based FACTS devices are no more applying the simple 2-level VSCs.

2.4.2 Multi-phase converter

A simple way to increase the power rating and to decrease harmonics is to parallel multiple converters with some certain phase shift by coupling transformers [90, 91]. The coupling transformer sum up all the quasi-square waveforms to generate a staircase voltage, which is more similar to a sinusoidal voltage and thus with less harmonics and then usually connect to the power system through a step up transformer. In most practical industrial applications, 48-pulse configuration is employed which can be classified into true-48-pulse topology and quasi-48-pulse topology, shown in Figure II-6 and Figure II-7 respectively.

The performance is acceptable as for the grid for the most cases but a disadvantage is the bulk transformer in the multi-pulse converter and the additional loss because of it. There are not much further improvement that can be done to multi-pulse converter due to the

repetitive parallel configuration and thus research focus have moved to the more flexible multi-level converter.

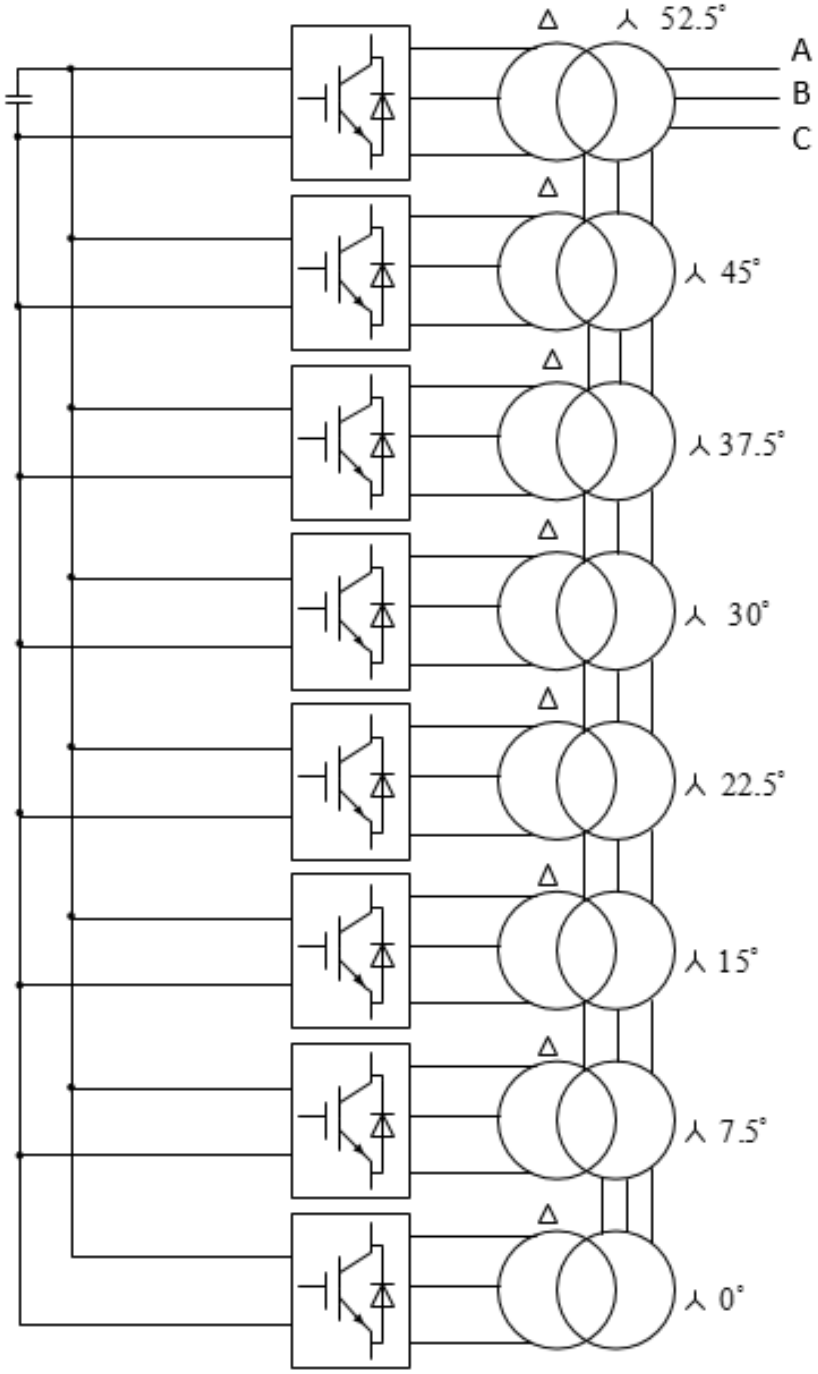

Figure II-6 True-48-pulse topology

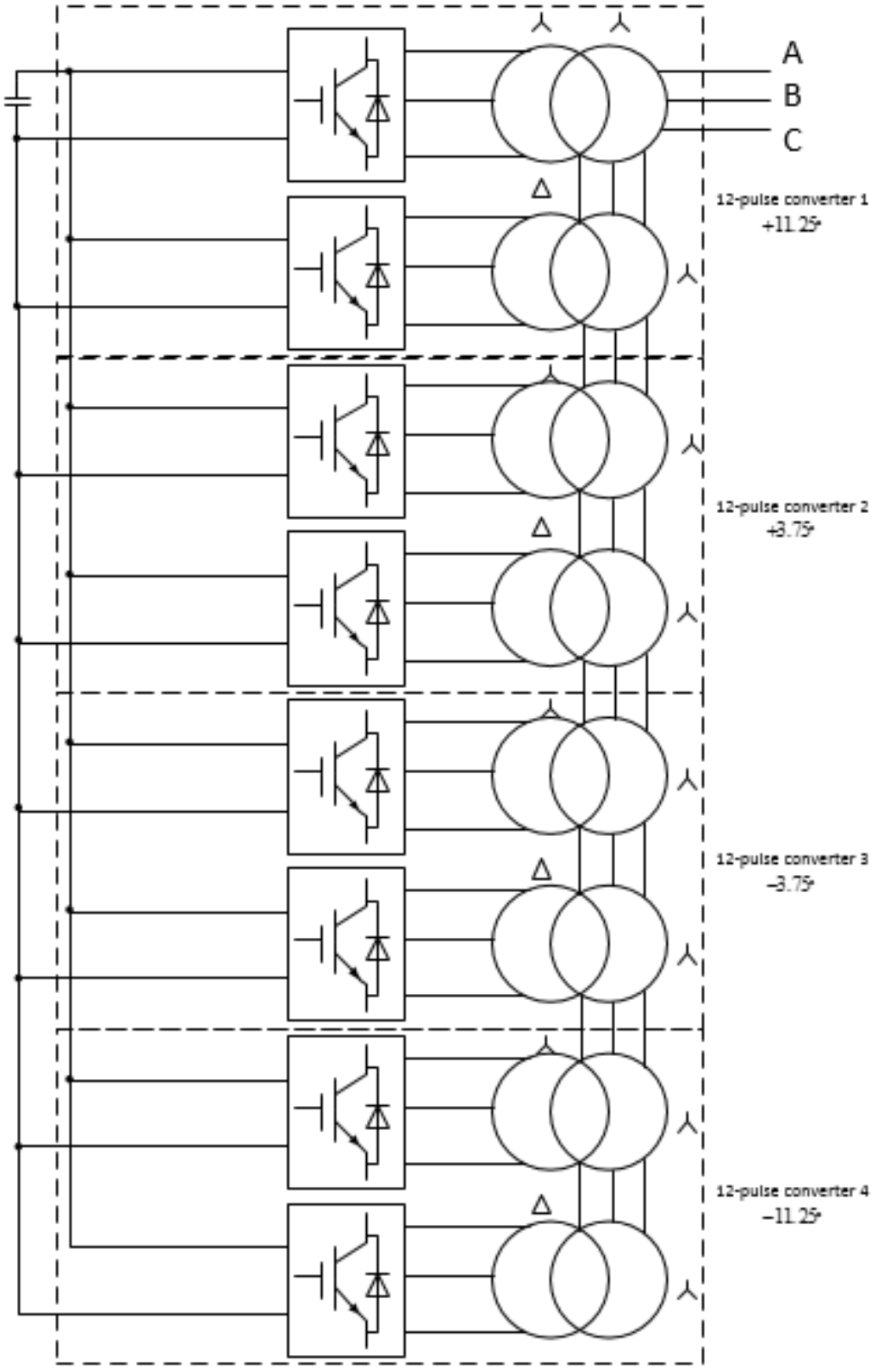

Figure II-7 Quasi-48-pulse topology

2.4.3 Multi-level converter

Another way to generate a staircase voltage is to use multi-level topology [91-106]. The basic idea is to divide the DC link voltage into n step voltages in an n-level converter or to use n individual DC voltages to produce a staircase voltage with (2n+1) levels connected to the power system without a transformer. With increasing the number of level, a better output waveform with less harmonic content can be achieved and even the output filter may be not necessary.

Basically, there are three major types of multilevel converters: diode clamped converter, capacitor clamped (also called flying capacitor) and cascaded converter. The diode clamped converter is shown in Figure II-8, using diodes to clamp the step voltages which are divided by n capacitors from the DC bus into n equal parts. To generate desired voltage value, only one switching sequence is possible, which on one hand simplifies the control scheme and on the other hand lacks the flexibility. For the most important problem of multilevel converter – voltage balancing, it is hard to handle when unbalanced voltage emerges due to harmonics or asymmetric losses unless applying PWM because there is no switching redundancy.

The capacitor clamped converter is shown in Figure II-9, using a ladder structure of capacitors where voltages on each capacitors differ from each other and the differences determine the voltage steps. Hence to generate a given voltage value, there are several different switching combinations. The flexibility enables capacitor clamped converter to manipulate switch sequences to control the voltages to maintain at the normal values. However, with this structure it is harder to start up since the pre-charge of each capacitor is not so straightforward as diode clamped converter does.

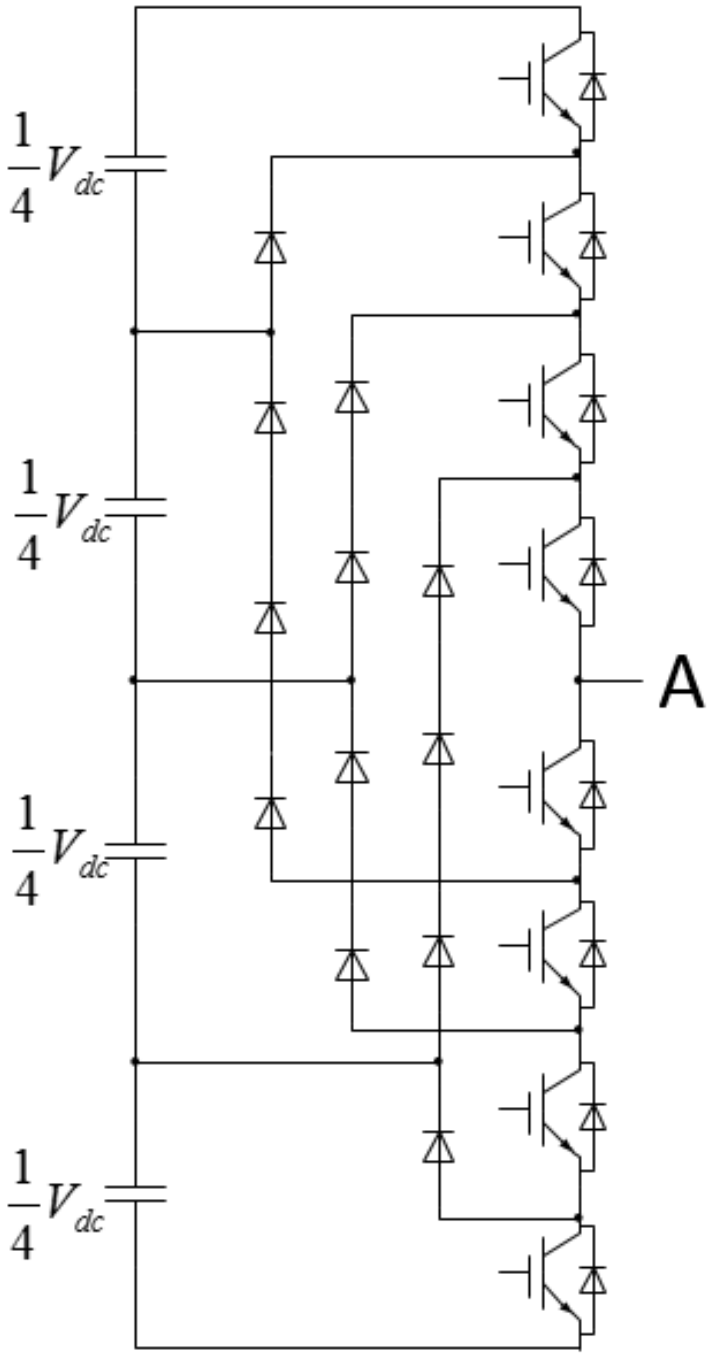

Figure II-8 Diode clamped converter – single phase

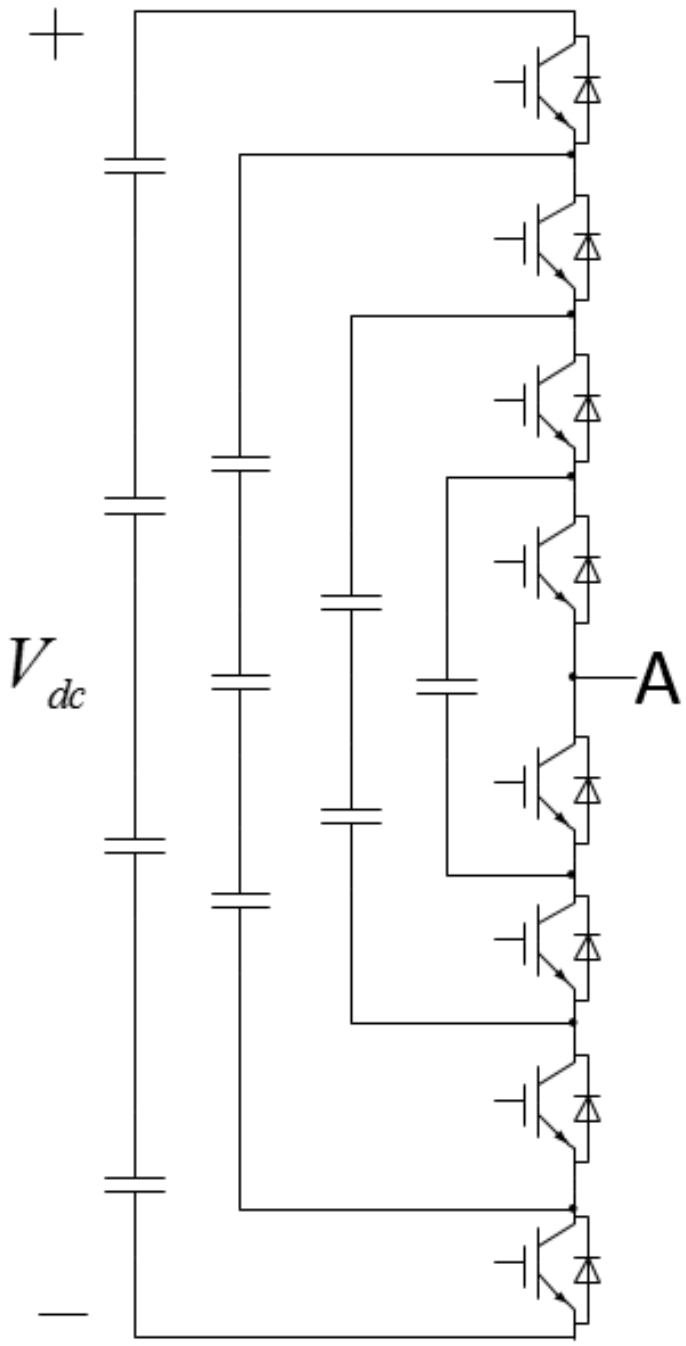

Figure II-9 Capacitor clamped converter – single phase

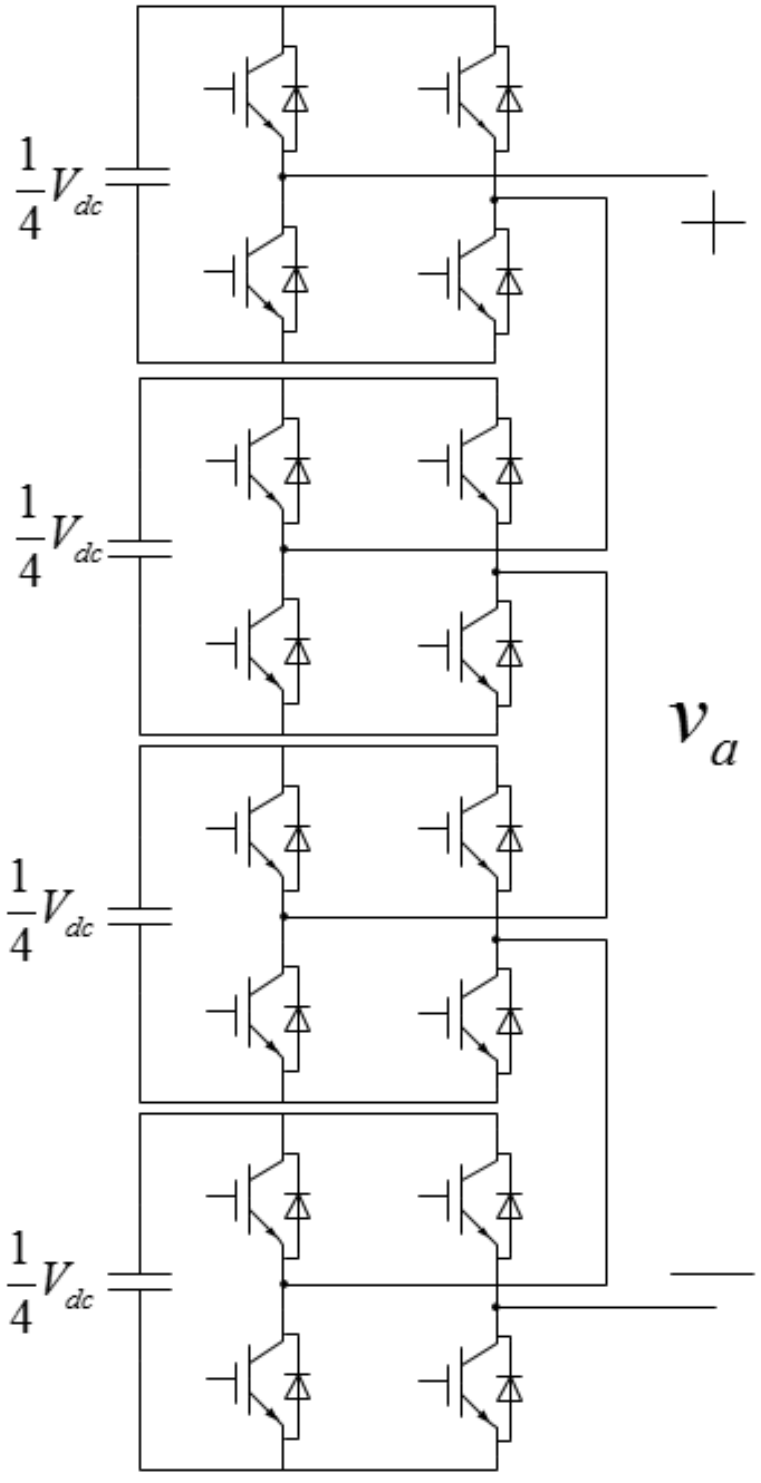

Figure II-10 H-bridge cascaded converter – single phase

The third and the latest one is the cascaded converter shown in Figure II-10. The step voltages can be either produced by individual DC voltages or divided from a DC bus voltage. The best advantage is that the cascaded converter is well modularized because of the same H-bridge or half-bridge structure. Each module acts like a 2-level VSC, capable of producing three voltages: +V, 0 and –V (V represents the voltage across each module capacitor) if using H-bridge structure and two voltages: +V and 0 if using half-bridge structure. As it is well modularized, the voltage balance is easy to accomplish just by changing the connection sequence.

All the three topologies are suitable for reactive compensation with little problem of voltage unbalance if working properly while diode clamped converter is not possible for active power delivery. Diode clamped converter installed with back to back configuration will see no difficulty of voltage balance because the unbalanced capacitor voltages on both side will compensate each other.

From the higher level control point of view, all kinds of topologies make no difference as long as the output fundamental voltage and current is satisfactory and not interfering with the control, which is true with present high switching frequency devices and with multi-level structures.

2.5 Summary

In this chapter, the basic operation of a STATCOM is discussed with its conventional control. Beyond that, a STATCOM can achieve different kinds of functionalities in different time scales depending on what types and levels of controller applied. Lastly a quick survey shows the common used topologies for STATCOMs.

Chapter III. VIRTUAL SYNCHRONOUS MACHINE CONTROL CONCEPT

3.1 Basic concept

The traditional generation in the present power system dominated by massive and centralized synchronous generators is now challenged by increasing penetration of intermittent and distributed generators (DG), which are composed of grid-interfaced converters harvesting renewable energy, whose impacts become non-negligible to the overall power system. An important change is the decrease in the total inertia in the power system when DGs are controlled simply by conventional cascaded voltage and current controllers and oriented by PLLs, shrinking the stability margin since not enough reserved energy exists unless large amount of alternate energy storage systems are hot standby, which is quite economically inefficient. Another concern is the potential interactions between PLLs, which could also present instability, when parameters are not carefully set as introduced in 1.2.1.

One way to integrate large proportion of DGs with good compatibility with the traditional power system is to step back to take advantages of synchronous generators by mimicking their behaviors, not necessarily emulating their long time constants and slow transient responses, but the mechanics of how they coordinate with each other in harmony, with the advanced technology of power electronics devices and digital controllers that can react a thousand times faster. With this idea, a concept that allows grid-connected converters to behave like synchronous generators arises using different orders of synchronous machine models. The core part is to emulate inertia, which is basically implemented as power-balance-based synchronization which is presented in 1.2.2.

3.2 Overview on control schemes

Back to 1981, G.J. Smollinger and W.J. Raddi [107] found the similarity in power transfer between a synchronous generator and an inverter, but nothing was further investigated especially on control because of the complexity limitation of controllers as well as low bandwidth constraints.

The first virtual synchronous machine based control scheme was proposed by H.P. Beck and R. Hesse in 2007 [1] with the name VISMA where they modeled the two windings of the stator in

d and q channels and the inertia too without any current loops. Basically there are five state equations in it: stator flux in d and q axis, excitation flux and two equations in the swing equation. Similar researches include [8, 43, 108, 109] by Jaber Alipoor, Yushi Miura and Toshifumi Ise where the researchers only use the swing equation in their synchronous machine model. Also in the first version of synchronverter [3, 21], no current controllers were presented but added in a later publication [4] where the swing equation was realized with the magnitude of the virtual back EMF generated by some reactive power command. Another similar scheme was proposed by M. Ashabani and Y.A.R.I. Mohamed [10] where they modified the swing equation implementation taking the dc bus voltage balance into consideration with also Pf droop and they added current controllers as well later [15]. In all the above models, the virtual back EMF is used directly to generate PWM signals, which corresponds to the dynamics of a traditional synchronous generator. In such, the output current is uncontrolled and limited either by virtual inductors or by actual boost inductors. Although this type of VSM control schemes is the simplest, the potential overcurrent issue hinders its application regarding to large transients.

A general control block diagram in Figure III-1 summarizes this type of control scheme where a generic grid-interfaced converter connects to the grid with an inductor, which could be a step-up transformer or an output filter. The grid voltage v_{abc} and current i_{abc} are measured to calculate active P and reactive power Q, and the grid voltage may be used also for some certain PLL to obtain the grid frequency f_{grid}, which is not necessary under most cases. The output voltage of the converter is synthesized with its magnitude V, which comes from either reactive power regulation "Q-ctrl" or ac voltage regulation "V-ctrl", and phase θ, which is generated from the VSM model used. The variables with superscript * mean the corresponding reference values. While the control structure remains like this, the VSM model is implemented differently in the above literature.

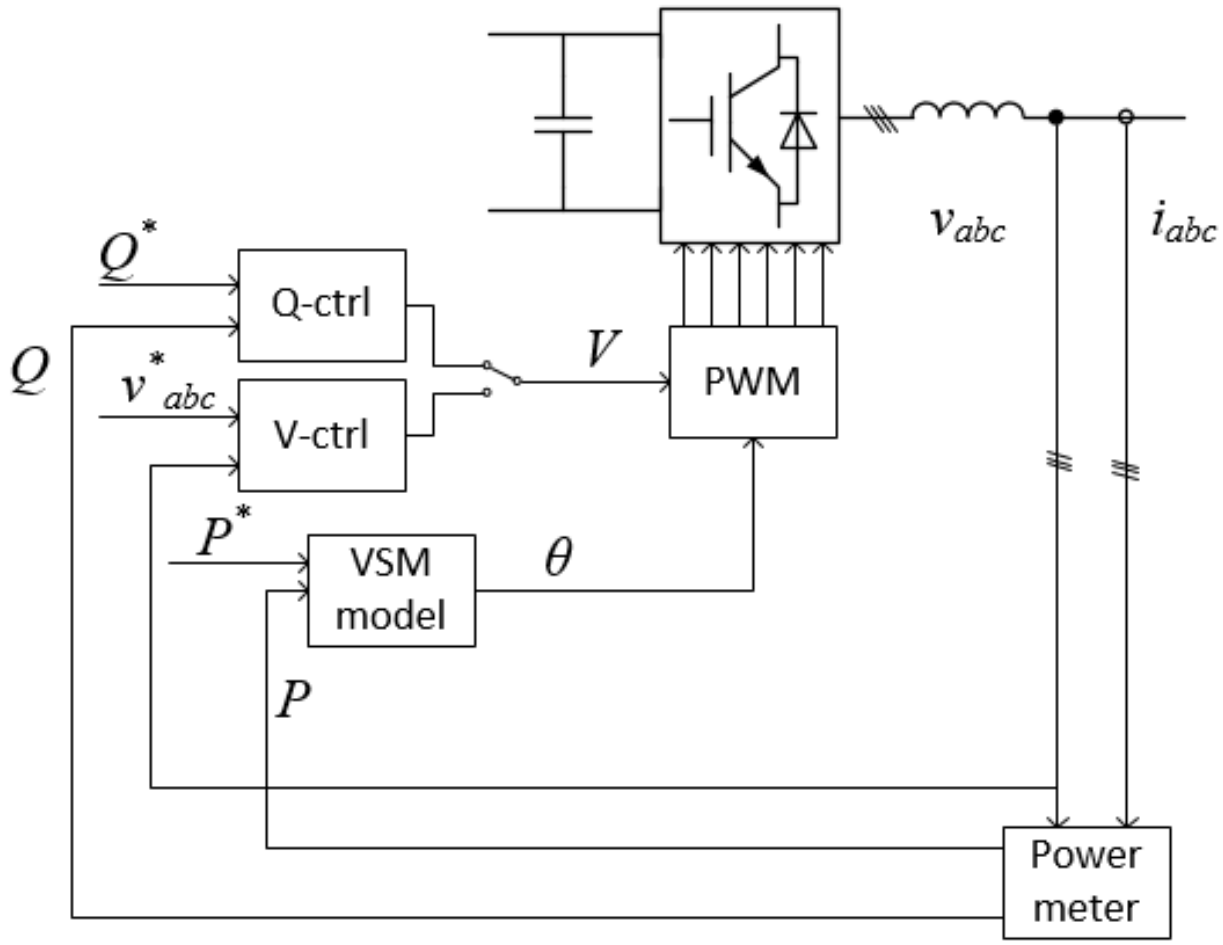

Figure III-1 VSM control scheme without current loop

Another kind of VSM control schemes is of a similar control structure with the conventional cascaded controller where inner current loops and outer voltage loops work together. This type was first published by Lidong Zhang, Lennart Harnefors and Hans-Peter Nee in 2010 [5] where they only chose to emulate the inertia by implementing the swing equation. VISMA was improved by the same authors [19, 20] where they control the output current instead of the virtual back EMF. The dynamics in the stator flux and swing equation remain in their model but a current control loop is added to overcome the previously mentioned problems. A major contribution of Pedro Rodriguez's work is to add virtual impedance [7, 110] which equivalently improves the current controller to fulfill advanced functionalities such as harmonic elimination and negative sequence compensation. Even a third level controller is shown in [111, 112] from Salvatore D'Arco and Jon Are Suul to obtain autonomous coordination with other units equipped with the same controller.

Similar control structure can also be found in the work of Jiebei Zhu etc. [6, 113] and Shuan Dong [114] as an improved version of synchronverter.

Figure III-2 depicts a generic control blocks for the VSM control schemes with inner current loop. The main difference from the previous kind is that the voltage vector generated by the VSM model goes through a current controller instead of being modulated directly, where the voltage vector can be called virtual back EMF to distinguish from the real output voltage vector. The current reference control block gives the current references, which can either be implemented into the VSM model adding the orders of the model, or a separate block named “virtual impedance” because of its physical meaning. There are a lot possibilities that the virtual impedance can provide such as to regulate current at different frequency and different sequence, to smoothen the transition from islanded mode to grid-interconnected mode, to provide additional damping and so forth. One can also implement an advanced current controller to simplify the virtual impedance but the complexity just moves from one block to the other. The current controller are typically realized in the D-Q frame for the convenience of the control. Again the phase information required by the Park transformation is obtained from PLL in some literature for parameter optimization or just unnecessarily.

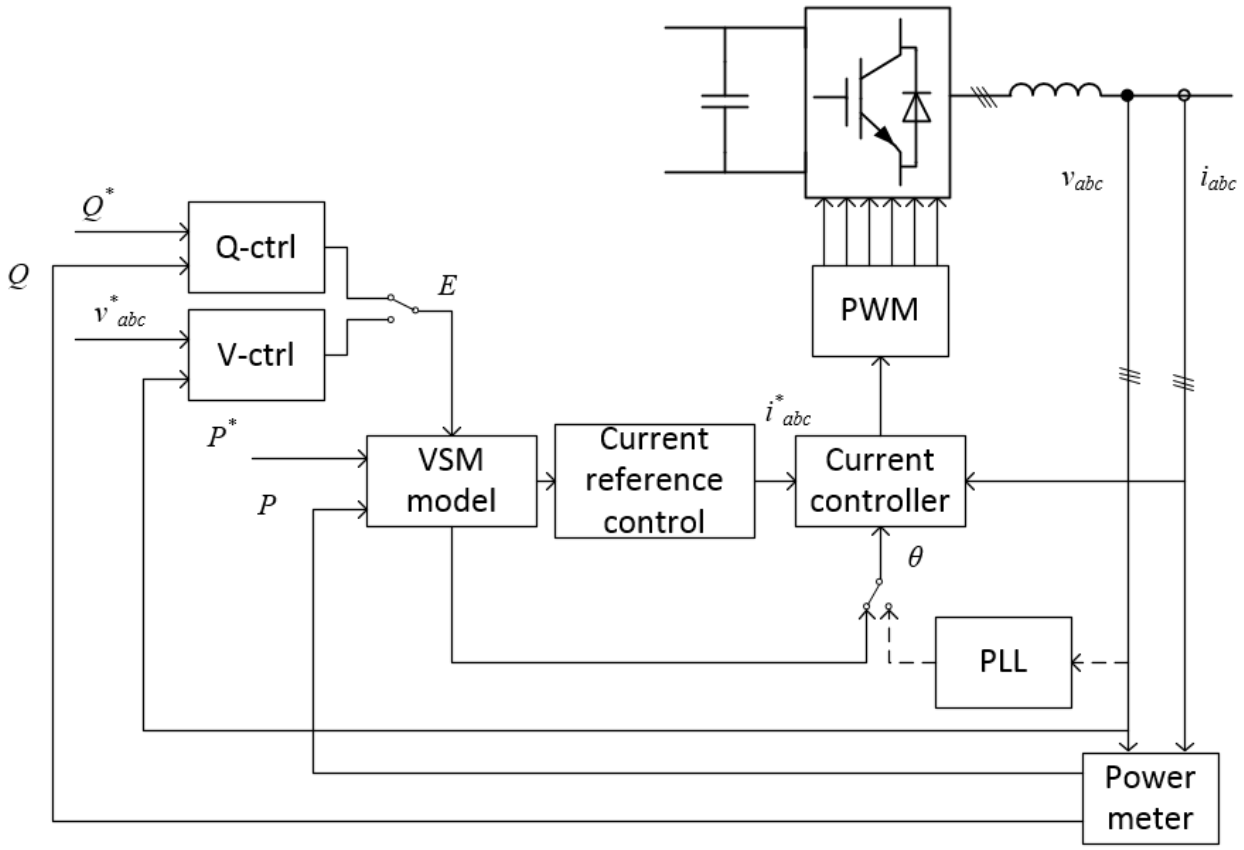

Figure III-2 VSM control scheme with current loop type 1

Another variation of the cascaded structure is as Figure III-3 as in [115] by Yan Du and [116] by Minyuan Guan. In those papers, the current reference is not given from the VSM model and the VSM model only serves as an alternate synchronization method replacing the PLL, making the structure more similar to the conventional cascaded controller. The current reference is traditionally acquired from the dc voltage regulator in d channel and ac voltage regulator in q channel, in which extra modifications can be made to achieve more functions. In such, the total control structure becomes more straightforward but no comparison has been made with the previous one.

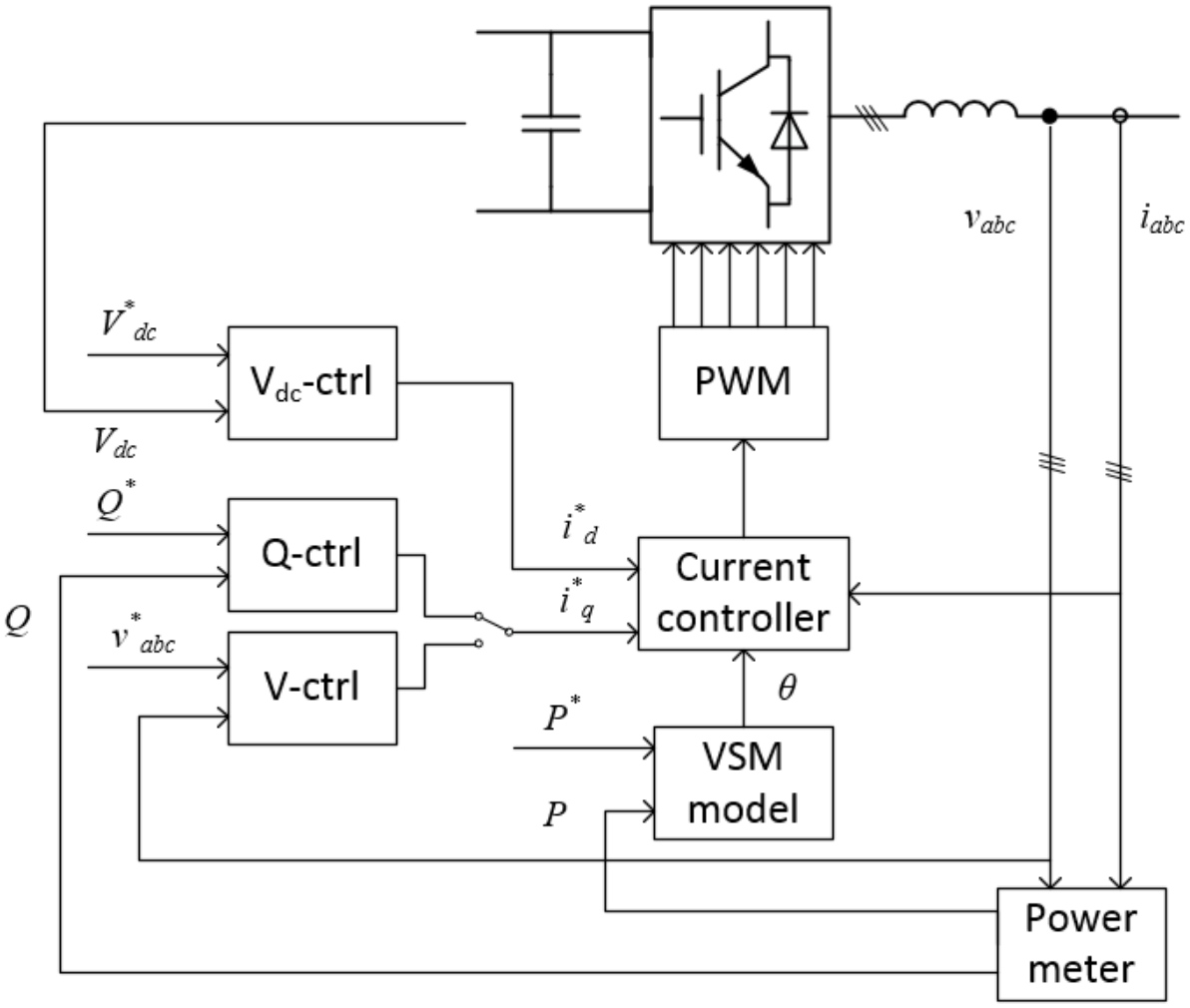

Figure III-3 VSM control scheme with current loop type 2

In principle, emulation of the inertia with the swing equations is enough to provide the frequency information of the power system. Therefore PLLs in the conventional D-Q-frame control can be replaced, or as a backup synchronization method during start-up or contingencies [4, 5]. In an interesting work by M.A. Torres etc. [117], a PLL is still used to acquire the grid frequency, which is different from the VSM frequency, in order to achieve self-tuning of the controller parameters.

In all, classified by control structures, there are two kinds: direct back EMF and additional current loop controller; classified by models from synchronous machines, there are typically two types: a simple model with only inertia and a full model with dynamics in flux and also inertia. Although each kind has different variants, more and more researches tend to cascaded controller with only inertia emulation. The first reason is that it is the virtual inertia that grants converters the

ability to use their stored energy to increase the total inertia in the power grid achieving frequency regulation [118] while keeping in harmony with other rotating units, on top of which droop functions are accessible in order to operate without centralized control. The second reason is that advanced controllers can take the maximum utilization of both the fast response of modern power electronics devices and also computation capability of digital processors, in order to achieve as many functions as possible, e.g. current harmonics attenuation and negative sequence compensation. More related publications can be found in details in these two overview papers [9, 119].

3.3 Ongoing activities

Besides papers about different models mentioned in the previous subsection, there are also some articles discussing design process and applications. However there is still a lot more to be investigated because this concept has recently drawn people's attention and no practical implementation is under operation yet.

3.3.1 Modeling and design

There are only a few papers where model and design process are given while the others just present control schemes conceptually without telling the reasons.

In [111, 112, 120], the authors derived the full state space model of the VSM controlled converter to obtain the pole-zero map to see the impacts and discussed the sensitivity from each states to each modes. Similar analysis can also be found in [14, 17] and [115]. This method requires full knowledge and is able to complete control over the whole system as long as the system is controllable, which is quite typical for the power system society. However the drawback is obvious: it needs large amount of computation and some parameters or states may not be attainable. A reduced model was derived in [18] to give some basic stability boundary analysis. On the other hand, design process based on transfer functions and Bode plots was proposed in [121, 122] where the computation burden can be decreased. Through some simplifications, control parameters can be tuned online to achieve better coordination and damping, as in [117, 123].

As for large signal models, the full state space model is seldom used because of the non-linearity. Lyapunov method and energy functions are often considered as good approaches as in [8, 15, 108, 109] but it is not possible to derive for a complex system.

3.3.2 Applications

The inherent nature of participation in frequency regulation of VSM-based control scheme makes it very suitable for all kinds of generation units, e.g. HVDC sending ends [6, 14, 16-18, 113, 124], PV farms [7], electric vehicles [125], STATCOMs [21, 121, 122] and generic distributed generation [3, 4, 8, 10, 15, 20, 112, 115, 116, 126] where they differ from each other on their specific operation conditions.

It is also intuitional to try to use the VSM control schemes to fulfill common power system functions, e.g. oscillation damping [8, 19, 43, 108, 117] and low voltage ride through [109, 127] by modifying the control loops, usually adding feedback and increasing the order of the compensators. However these have not been studied much since the VSM control schemes are under development.

3.4 Summary

In this chapter, the VSM based control schemes are reviewed and classified according to the implemented model and control structure. Although most existing literature is about proposals of different control schemes, modeling, design and applications are included as well.

Chapter IV. ANALYSIS AND COMPARISON OF VSM AND D-Q FRAME CONTROLLERS

This chapter focuses the implementation of the VSM controller to the STATCOM application based on a simple one-generator-infinite-bus system where both the VSM controller and D-Q frame controller are compared. In order to get a deeper understanding of the VSM controller, the control blocks as well as transfer functions are derived. By doing that, one can choose the parameters and design the compensators in order to achieve desired performance.

4.1 Introduction of the test bed

Figure IV-1 is a simple but general test case where a STATCOM is helping a renewable energy source (shown as a wind turbine in the figure) with parameters listed in Table IV-1 [58], which is representative. In this case, a wind farm is providing power to an infinite bus bar with a shunt connected STATCOM tracking and regulating the PCC voltage v_{PCC}. The wind turbines are lumped into one generator; the STATCOM is modeled as 2-level converter because the topology does not count much in the control point of view; and the grid is interfaced with a step-up transformer. An LCL filter is often implemented because of the requirements in IEEE-1547 harmonic standard.

One thing to mention is that because the work of this article is focused on the control of the STATCOM, the wind turbine is simplified as a simple synchronous generator with varying magnitude and frequency without any advanced control [44]. This simplification is not valid for researches on the wind turbines, but since the focus of this work is the analysis of the VSM controlled STATCOM and the STATCOM only senses the information at the PCC, only the output characteristics of the wind farm are of interest.

Also, it is easy to set different values for the impedance of the source and the grid in order to present a weak grid where the renewable energy is dominating. In this simplified test bed, most of the grid contingencies can be simulated: changing the mechanical input power of the induction generator to imitate input power fluctuation, adding harmonics or negative sequence voltage to grid voltage to mimic voltage disturbances during transients, shorting the infinite bus to emulate fault, among others.

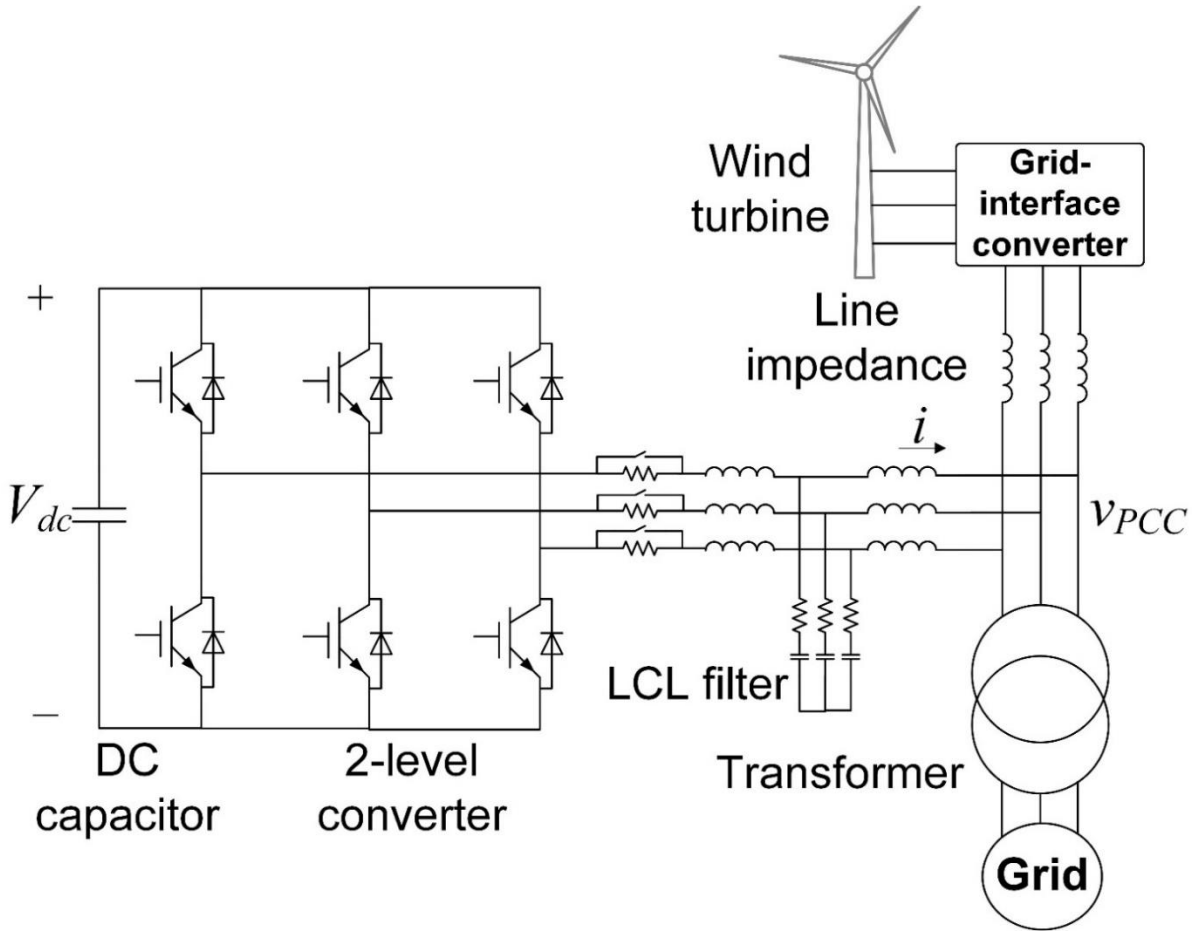

Figure IV-1 Single line diagram of the 3-phase test bed

Table IV-1 Parameters of the test bed in simulation

Symbol	Description	Value
V_{dc}	DC bus voltage	1200 V
V_g	Grid ac bus phase to phase voltage	690 Vrms
$V_{PCC,\ uncomp}$	PCC bus phase to phase voltage, uncompensated	667 Vrms
$V_{PCC,\ comp}$	PCC bus phase to phase voltage, compensated	690 Vrms
Q	Output reactive power	80 kvar
P_{wind}	Nominal output power of wind farm	100 kW
L	Line inductor	10 mH
C_{dc}	DC bus capacitor	2000 μF

4.2 VSM control

4.2.1 Loop structure

With the generic idea of VSM based controller in mind, it can be implemented for a STATCOM as well. The proposed VSM-based STATCOM has a virtual back EMF *e* and virtual impedance *Z* implemented in the controller as a synchronous machine looking from the PCC voltage v_{PCC} in the equivalent circuit sense as shown in Figure IV-2. The introduced virtual impedance which is between *e* and v_{PCC} includes the actual impedance by tuning the output V-I characteristics in the VSM controller, providing the possibility to control the output current. As such, the additional degrees of freedom from the virtual impedance grant the capability first to regulate the current at different frequency in order to attenuate the harmonics or deal with negative components, and secondly to achieve overcurrent protection.

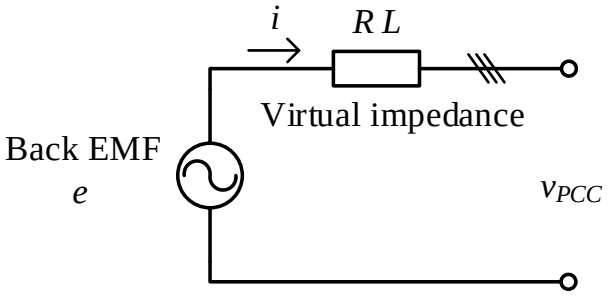

Figure IV-2 Equivalent circuit of VSM controlled STATCOM

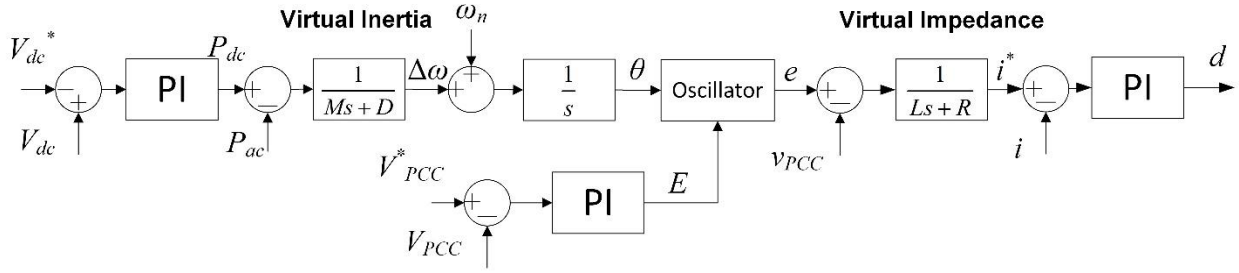

Figure IV-3 VSM control blocks for STATCOM

Figure IV-3 presents the control blocks of the VSM controller, where the core part which applies the swing equation in the upper middle with virtual inertia *M* and virtual damping coefficient *D*, providing the phase θ of the back EMF, which synchronizes with the grid in the steady state with a phase difference known as power angle, instead of using the PLL to track the

grid voltage. The feedback of this loop is the output power of the STATCOM and the reference comes from an outer voltage loop to be introduced below. It is called power loop.

There are two outer voltage loops: one to maintain the dc bus voltage and the other to regulate the PCC bus voltage as the main function of a STATCOM, just as the two outer voltage loops in the conventional D-Q frame controller. Because the STATCOM is supposed to provide or absorb reactive power only without the capability to generate active power, there will be zero active power transferred between the STATCOM and the grid if losses are neglected. But during transients, the zero active power balance is not naturally guaranteed and it is necessary to use the error in the dc-link voltage V_{dc} through a compensator to regulate it. If the dc bus voltage is lower than the nominal value, the STATCOM should absorb some active power from the grid to boost it. Therefore P_{dc} will then become negative and the phase of the back EMF will decrease, leading to a larger power angle to take active power from the grid. The dynamics are the opposite if the dc us voltage is higher than the nominal value. This process is related to the active power to maintain dc bus voltage so the loop is named as Pf loop. In the conventional synchronous generator control, there is another loop called QV loop to control the magnitude of EMF in order to regulate the terminal voltage. It is also implemented similarly in the proposed control strategy that the error in the magnitude of v_{PCC} will go through a compensator to generate the amplitude of the virtual back EMF E. If the PCC bus voltage drops, the back EMF tends to go up to increase the output current to compensate.

The back EMF is then converted into abc frame as e by the oscillator with its phase position θ and amplitude E, then subtracted by the PCC bus voltage v_{PCC} and divided by the virtual impedance to obtain the current reference, which emulates the circuit dynamics shown in Figure IV-2. The inner current loop is realized in D-Q frame to regulate the compensating current in the VSM controller, generating the duty cycle d.

The control structure can also be drawn as in Figure IV-4 as a practical implementation in simulation or hardware where all the control variables of inner loops are converted into dc values by Park transformation with the phase information generated by the power loop. The two outer loops are inherently based on dc values and thus irrelevant from the phase information. Notice that the virtual back EMF has always zero q channel components because the D-Q frame is aligned along with the back EMF vector.

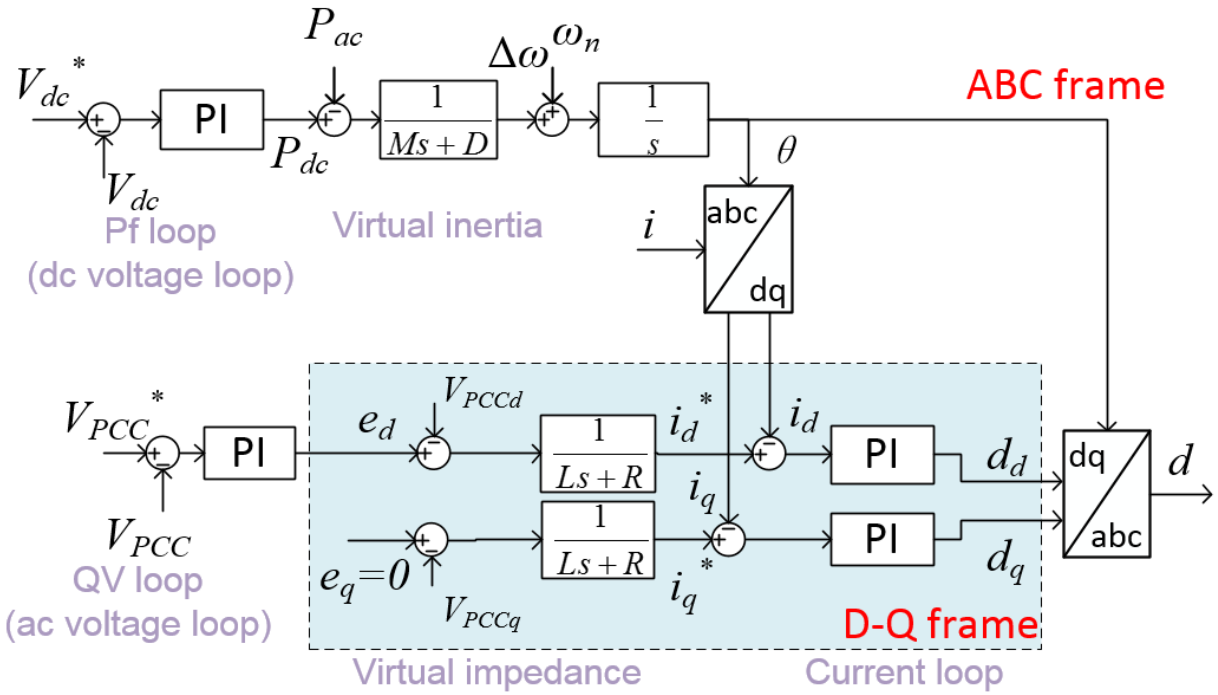

Figure IV-4 Practical VSM control blocks for STATCOM

4.2.2 Effects of virtual parameters

4.2.2.1 Effects of virtual inertia

As noticed in Figure IV-4, the power loop generates the power angle which transform variables from abc frame to D-Q frame, and this shall bring dynamic responses to the system even when the duty cycle is given as a fixed value in the controller D-Q frame. To see this phenomenon, all the control loops except the power loop are disabled as Figure IV-5 shows and linearized around the nominal operating point. There are basically two pairs of double poles, which are associated with the resonance between ac inductor and dc capacitor, potentially causing trouble. Sweeping *M* and *D*, the trajectory of the system poles are displayed in Figure IV-6 and Figure IV-7 with arrows indicating the parameters increasing, showing that too small value of either two leads to a pair of double poles on the right half plane. As such, when designing the power loop to synchronize with the grid, small values of the virtual inertia should be avoided and tuned with enough phase margin for the power loop.

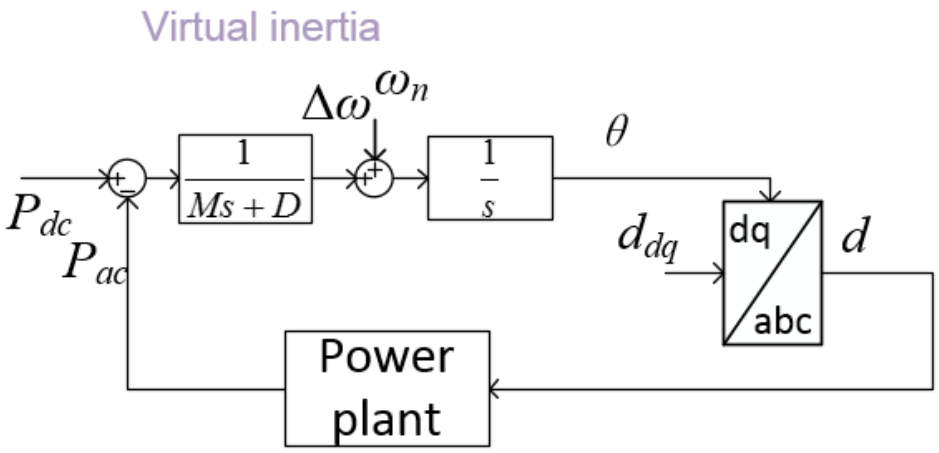

Figure IV-5 Control blocks of power loop and power plant

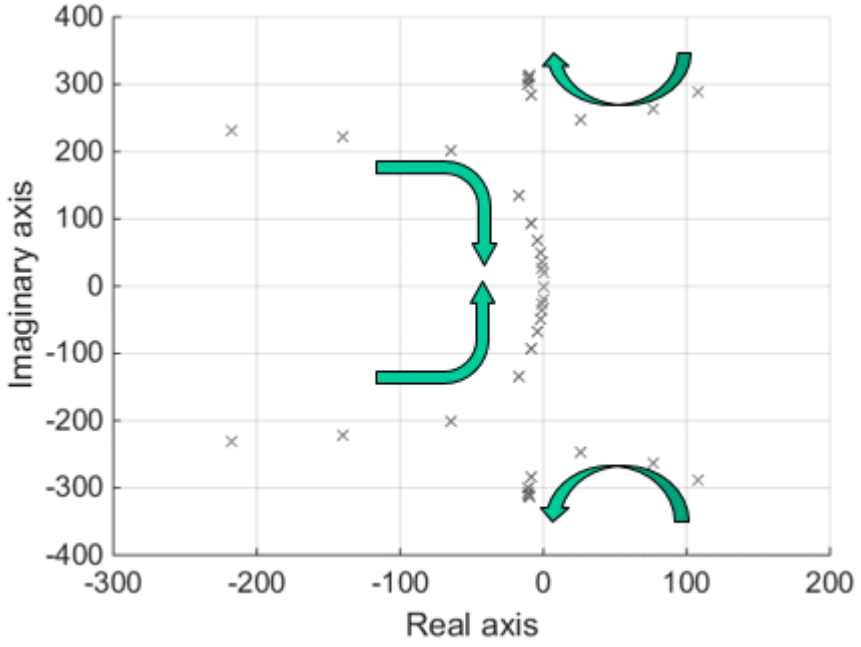

Figure IV-6 Open loop system poles trajectory with *M* increasing

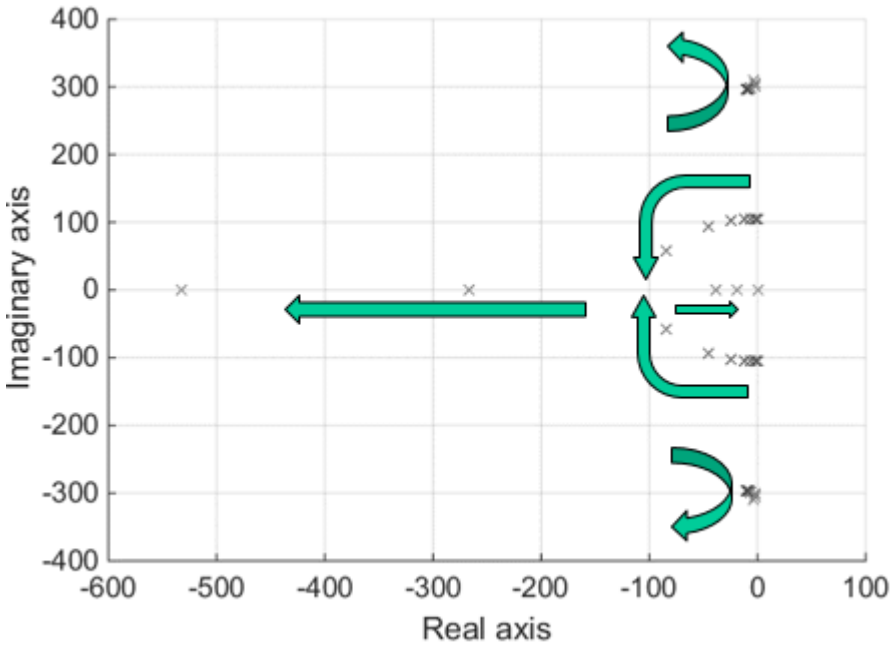

Figure IV-7 Open loop system poles trajectory with *D* increasing

For the next step, the transfer function from duty cycle to current in controller D-Q frame is calculated as $\mathbf{G_{id}}(s)=\mathbf{i}(s)/\mathbf{d}(s)$ with the virtual inertia taking effect, as shown in Figure IV-8. As mentioned before, the virtual inertia will influence the transfer functions, which can be observed in the Bode plots in Figure IV-9 with *M* and Figure IV-10 with *D* increasing indicated by the arrows. The influence from the virtual inertia only happens at low frequency range below 1-10 Hz, so it can be stated that the virtual inertia has little influence when designing the current compensator and to close the current loop at 200 Hz with desired phase margin regardless of virtual inertia. Therefore, the selection of *M* and *D* is almost not within the consideration of the inner current loop design.

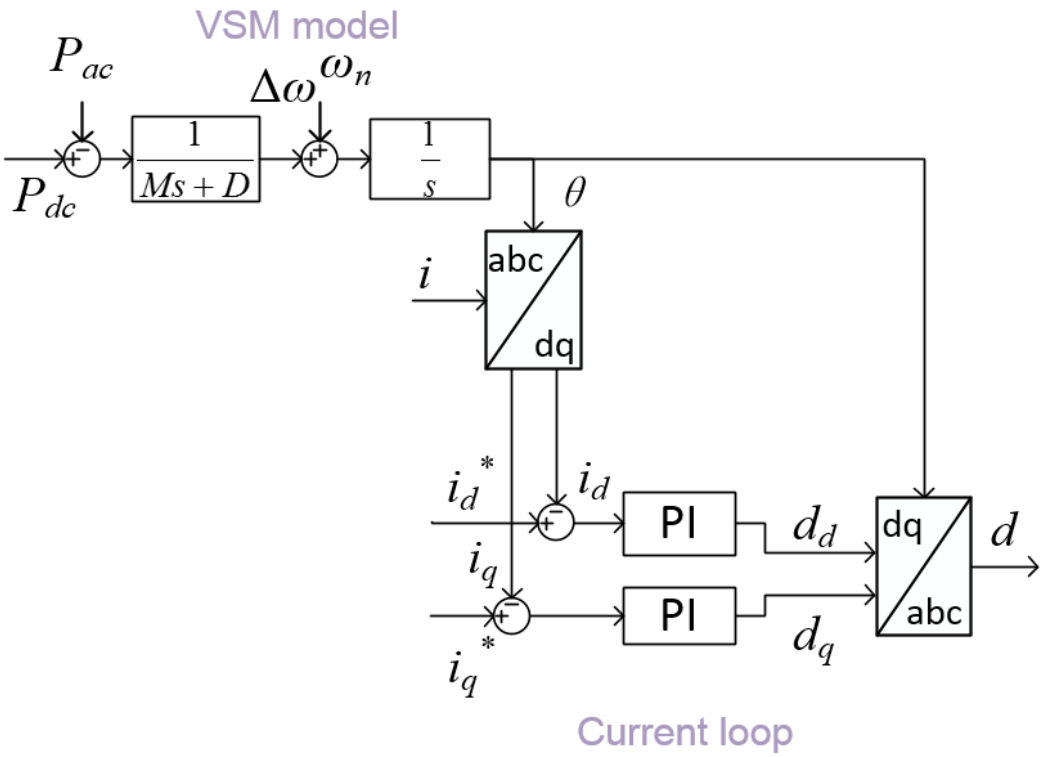

Figure IV-8 Control blocks of power loop and current loops

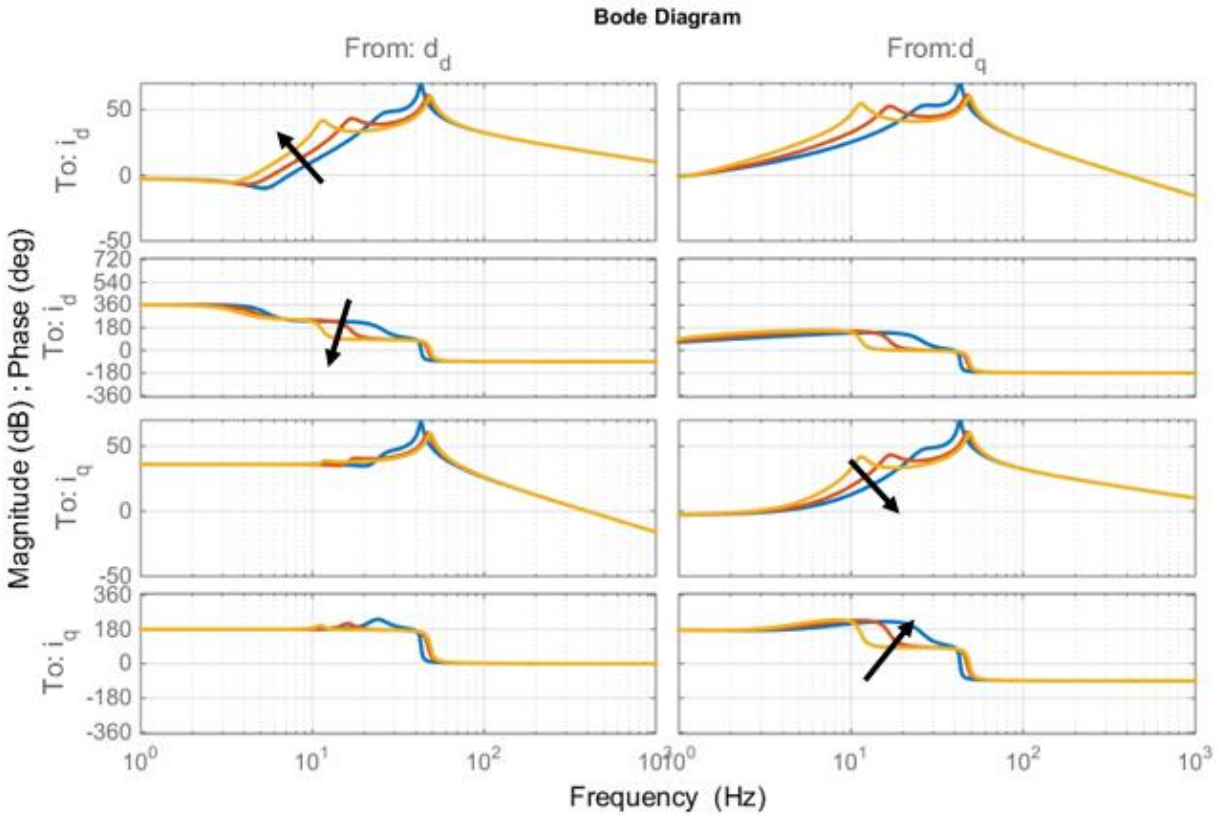

Figure IV-9 Effect of *M* on current loop transfer functions

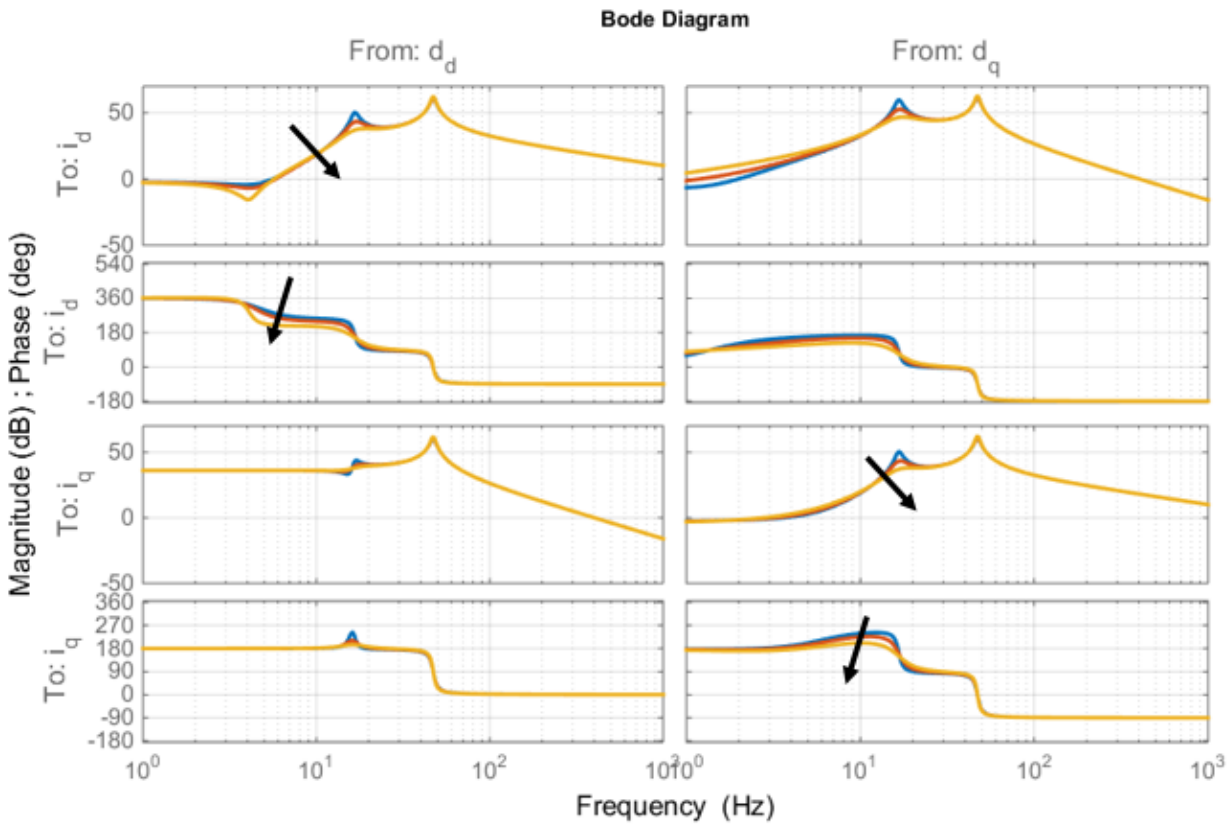

Figure IV-10 Effect of *D* on current loop transfer functions

Another interesting aspect is that the virtual inertia affects the ac impedance of the STATCOM in d-q frame also, which is shown in Figure IV-11 with only respect to *D* because there is little difference when *M* is changing. All the impedance are affected and larger *D* results in a lower impedance and better phase in the qq channel, which is preferable in the sense of stability issues.

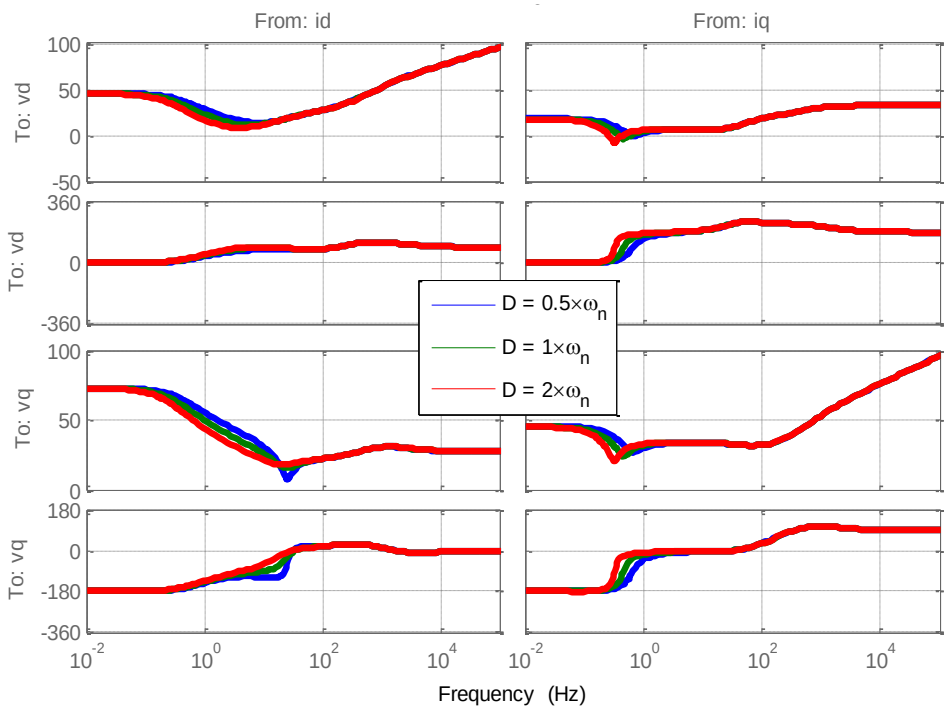

Figure IV-11 Effect of *D* on ac impedance

4.2.2.2 Effects of virtual impedance

Because the virtual impedance is outside the current loop, it has no impact on the current to duty cycle transfer functions. The virtual impedance implemented here is actually a low pass filter as a simple example and one important function is to filter out possible harmonics. The ratio of *R* and *L* is selected and fixed according to the desired harmonics spectrum where a lower limit is also determined. The same methodology is applied to the transfer function from current references to PCC voltage linearized as in Figure IV-12 with different magnitudes of *Z* keeping the ratio the same, shown in Figure IV-13. It is shown that with larger *Z*, the gain is smaller, which indicates that the regulation performance is weakened because the current references become smaller. But larger *Z* means stronger attenuation of harmonic components while introduces more P and Q coupling because of larger phase difference between two D-Q frames. So the trade-off is between the harmonic attenuation and controllability. It is more desirable to have as small virtual impedance as possible when complying with the grid code at the least price to control active and reactive power independently. Moreover the poles and zeros move due to the change in the ratio between virtual impedance and the impedance of the rest grid.

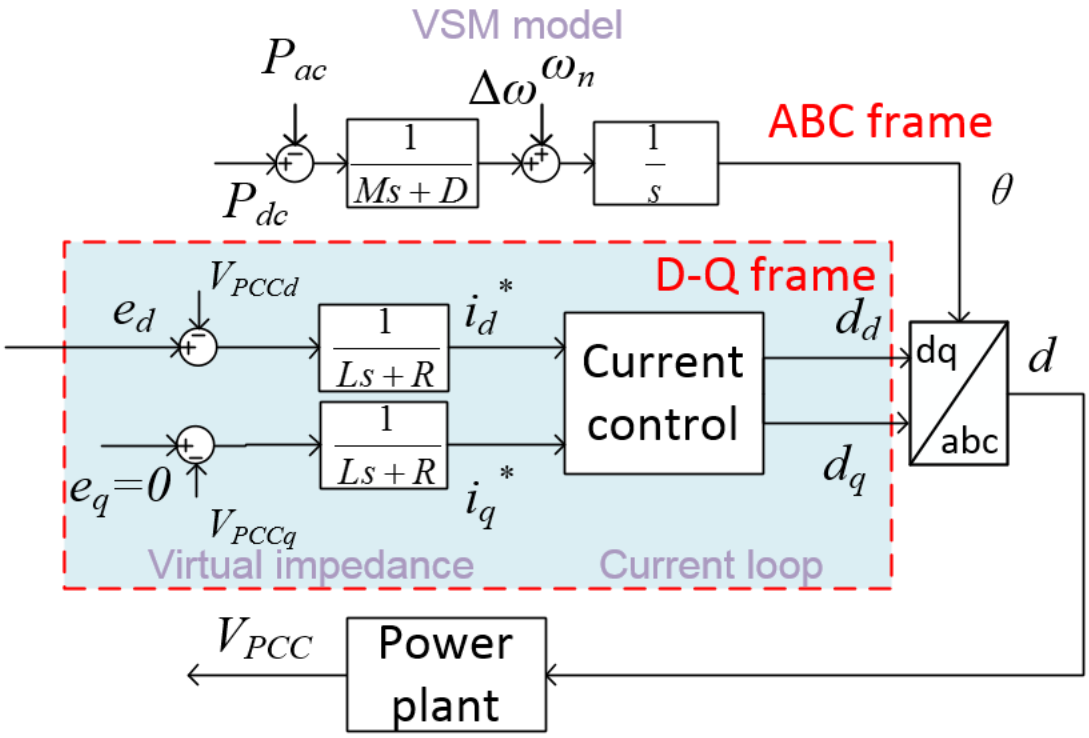

Figure IV-12 Control blocks of power loop, current loop and virtual impedance

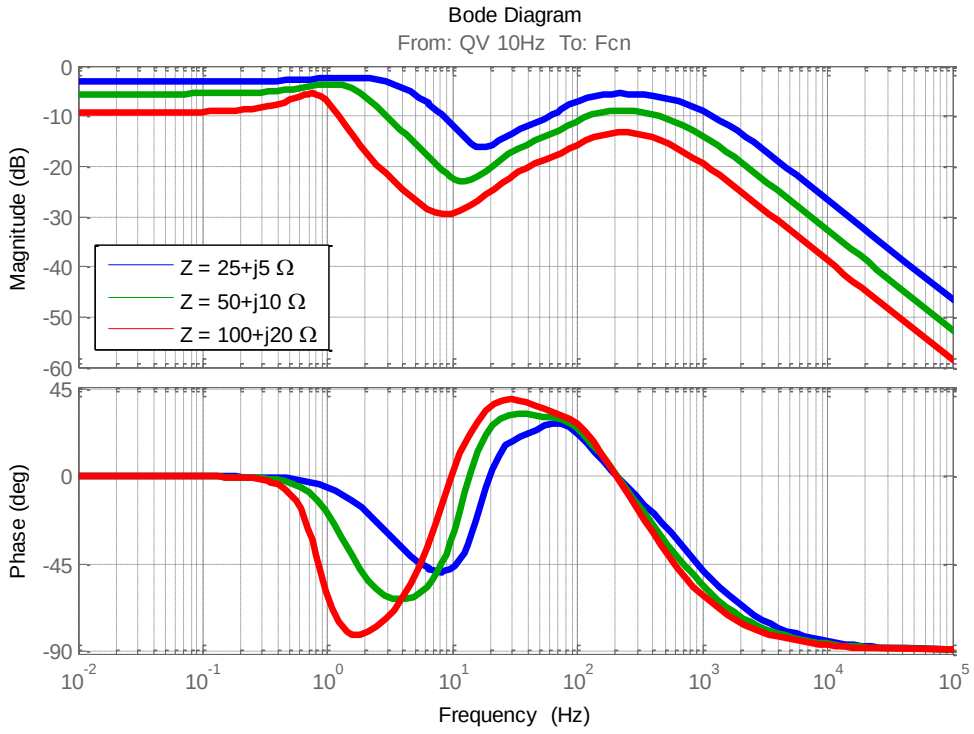

Figure IV-13 Effect of *Z* on QV loop transfer function

As for the ac impedance, the virtual impedance will take effects up to the current bandwidth as plotted in. Note that a larger virtual impedance leads to a larger ac impedance within bandwidths, showing the effectiveness of varying virtual impedance. For a STATCOM, which is a reactive source typically, a lower ac impedance is desired and thus a small virtual impedance will be good from this point of view. However, larger virtual impedance tends to have a better phase performance in qq channel, making the choice another trade-off.

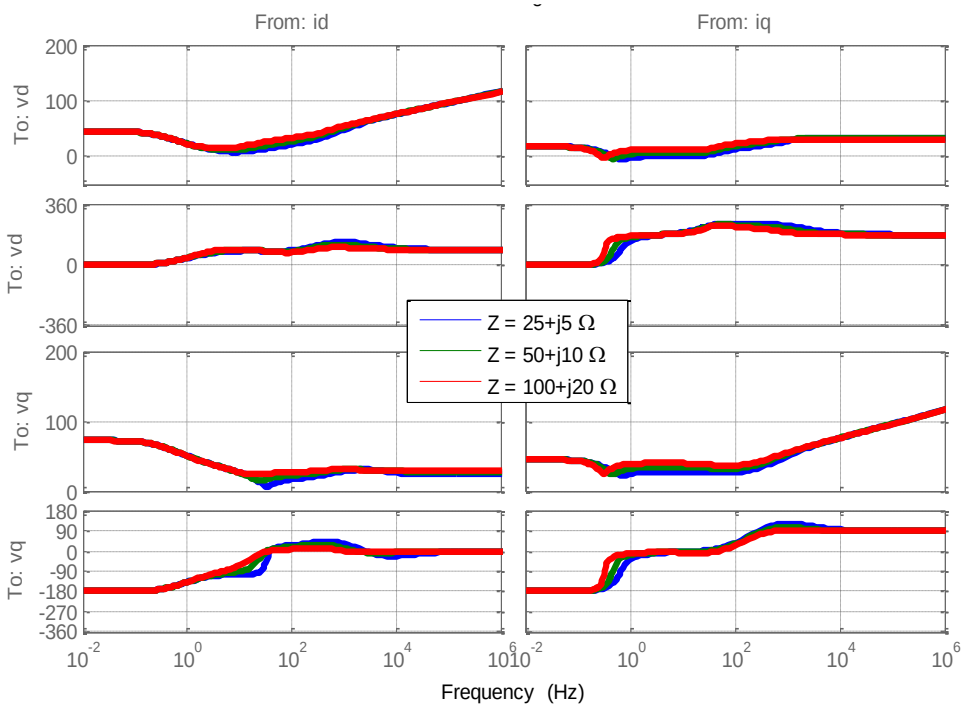

Figure IV-14 Effect of *Z* on ac impedance

4.3 Design rules of VSM controller

With the knowledge above, a design procedure is proposed.

Step 1, tune the virtual inertia loop by changing *M* and *D* to get a desired bandwidth with enough phase margin.

Step 2 design the current compensators. This has little to do with the virtual inertia choice.

Step 3, select the *R* and *L* ratio for virtual impedance based on desired harmonic spectrum.

Step 4, choose the magnitude of the virtual impedance to grant enough damping for selected harmonic components.

Step 5, design compensators for the outer voltage loops.

4.4 Comparisons between two controllers

After taking a look into two kinds of controllers individually, they can be compared in a fair way with the same inner current compensators and same bandwidth of the outer loops shown in Table IV-2. The two illustrated controllers are implemented in MATLAB/Simulink.

Table IV-2 Bandwidths of each loop in two controllers

VSM		D-Q frame	
	Bandwidth		Bandwidth
Power loop	10 Hz	PLL	10 Hz
Current loop	200 Hz	Current loop	200 Hz
QV loop	10 Hz	AC voltage loop	10 Hz
Pf loop	3 Hz	DC voltage loop	3 Hz

4.4.1 Comparisons in frequency domain

First, the power loop gain and the PLL loop gain are shown in Figure IV-15 where they have the same bandwidth and enough phase margins. The power loop gain from the VSM controller present larger gain before its bandwidth, meaning a stronger resilience to frequency change from the grid, which is anticipated.

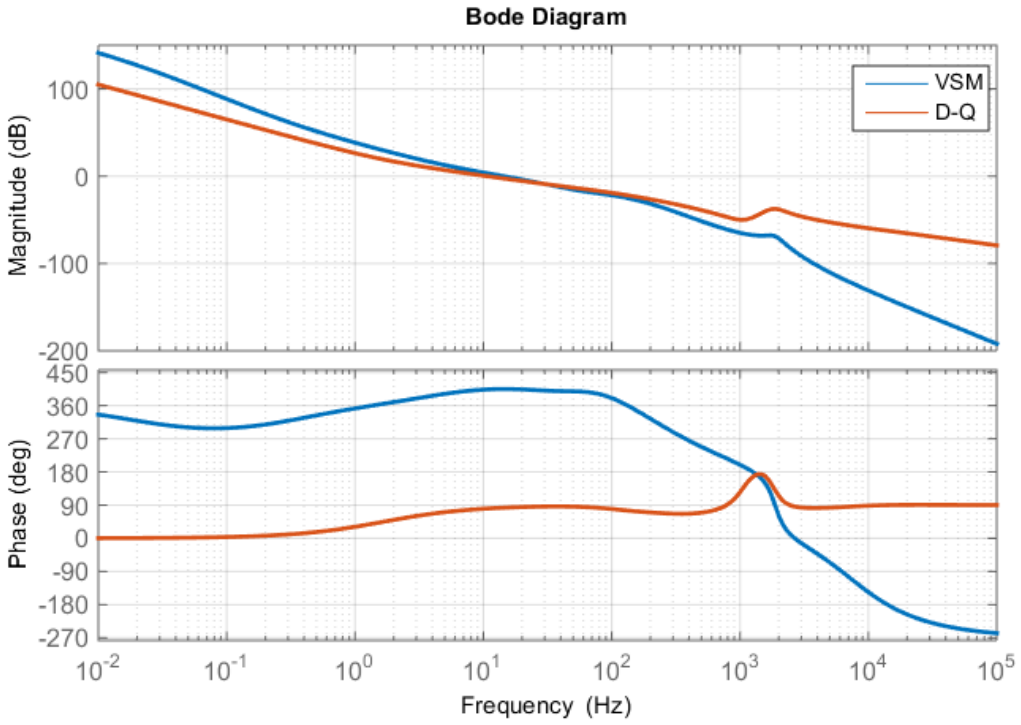

Figure IV-15 Synchronization loop gain of two controllers

Second, Figure IV-16 shows the current loop gains of the two types of controller. Although they differ from each other at low frequency range because of different synchronization methods, they converge together around their bandwidths, making them with the same bandwidths at 200 Hz, which is limited by the resonant peak of the LCL filter, and phase margins, about 68 degree in both d and q channels.

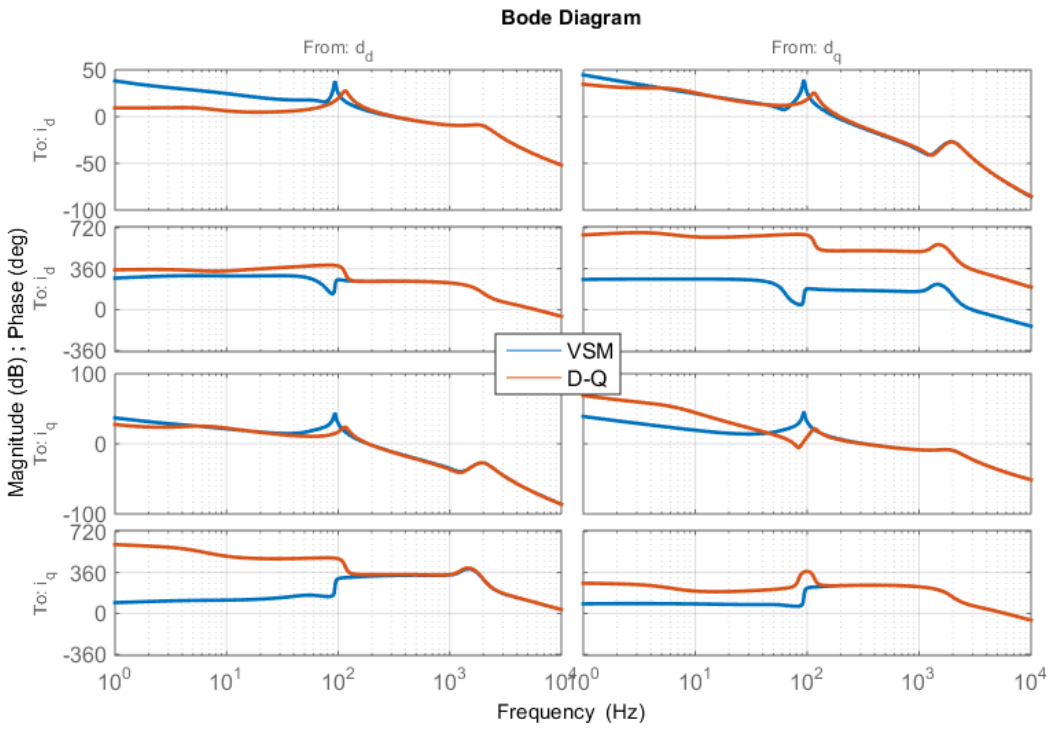

Figure IV-16 Current loop gain of two controllers

Third, the outer voltage loops of the two controllers are investigated in Figure IV-17 and Figure IV-18 respectively. As observed, through proper design both controllers achieve similar frequency responses at low frequency range up to their bandwidths, ensuring a fair comparison between the two controllers. The ac voltage loop bandwidth can be pushed higher upon the grid requirements to the STATCOM while the dc voltage loop should be slow enough not to interact with the inner loops.

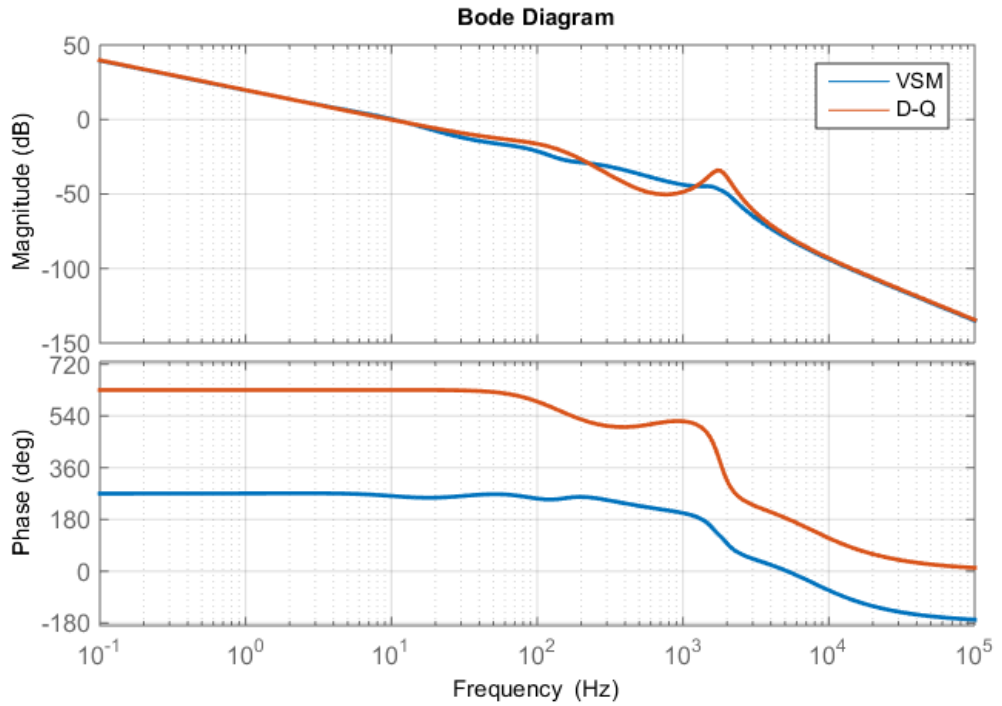

Figure IV-17 AC voltage loop gains of two controllers

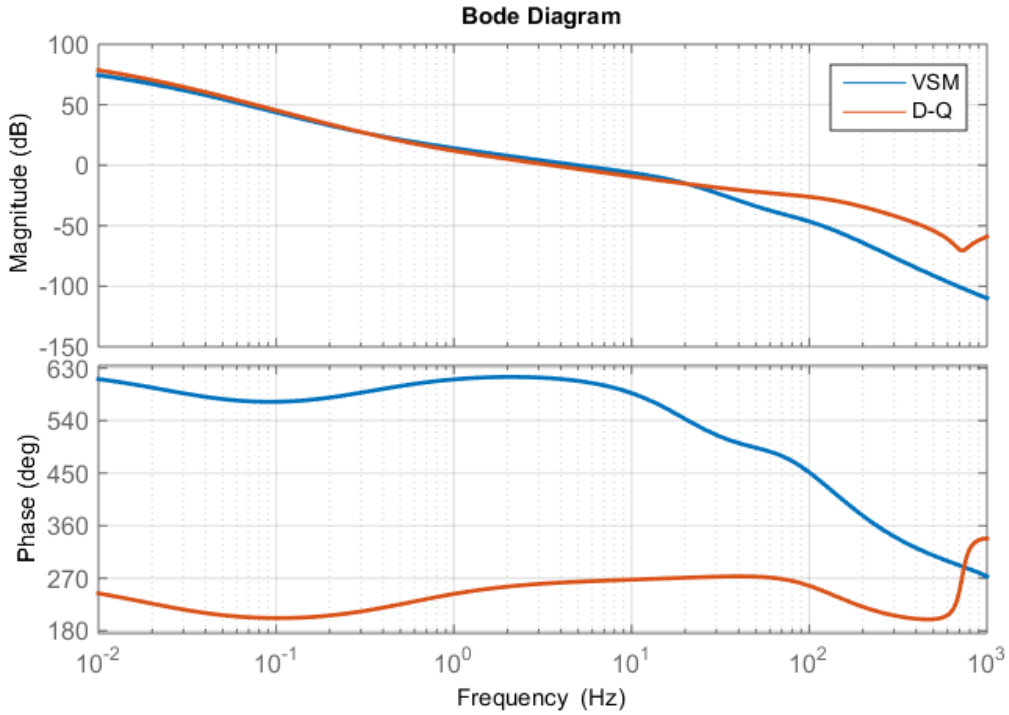

Figure IV-18 DC voltage loop gains of two controllers

There is a much more notable advantage of the VSM-based controller over the d-q frame one in the ac impedance in d-q frame. In the qq channel of the traditional d-q frame controller, the impedance is negative within the PLL bandwidth, which in this case is 10 Hz. If the load impedance intersects with the STATCOM impedance with a phase difference larger than 180 degree, the system is unstable because the PLLs fight with each other [13]. As the intersection often happens at several hertz, this phenomenon is similar to the sub-synchronous oscillation in the power system. As plotted in Figure IV-19, the qq channel impedance of VSM has a much smaller frequency range (about two decades) of negative impedance and thus has a much better phase margin when two impedance intersect. From this point of view, operating the STATCOM with the VSM-based controller presents a favorable feature that it is more stable in the small signal sense.

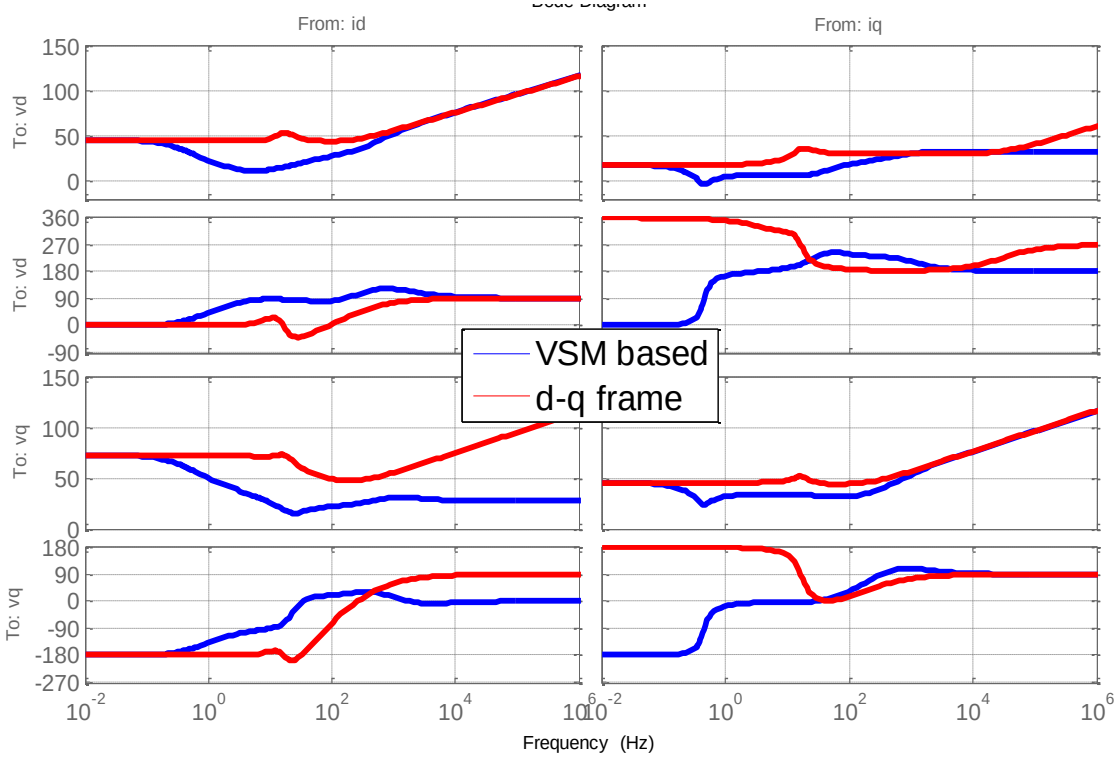

Figure IV-19 AC impedance of two controllers

4.4.2 Comparisons in time domain

Three tests are performed in this subsection: PCC voltage reference step change, source voltage sag and power fluctuation.

Figure IV-20 shows the PCC voltage reference step changing to 1.2 pu and the source goes through a voltage sag to 0.9 pu as plotted in Figure IV-21. Under these two cases, it takes very short time to reach the steady state corresponding to bandwidths respectively. Because the two kinds of controllers share the same bandwidth of the ac voltage loop, it is reasonable that they can achieve almost the same settling time. A similar patterns can be found on these two occasions where the d-q frame controller shows a first-order transient response due to well-designed damping, while the VSM-based controller presents some overshoot presenting the swinging axis of the imaginary rotating mass. Note that under both cases the VSM controller will swing to search the new steady state position, resulting in its frequency vary and active power compensation involved while the D-Q controller sees nothing because the PLL is locked. But it brings no better voltage regulation because there are no frequency changes and the D-Q controller is injecting current in the right phase while the VSM controller oscillates in its phase intrinsically but unnecessarily. This phenomenon can still be observed in the excessive PCC bus voltage for the VSM control due to its active compensation and variation in phase.

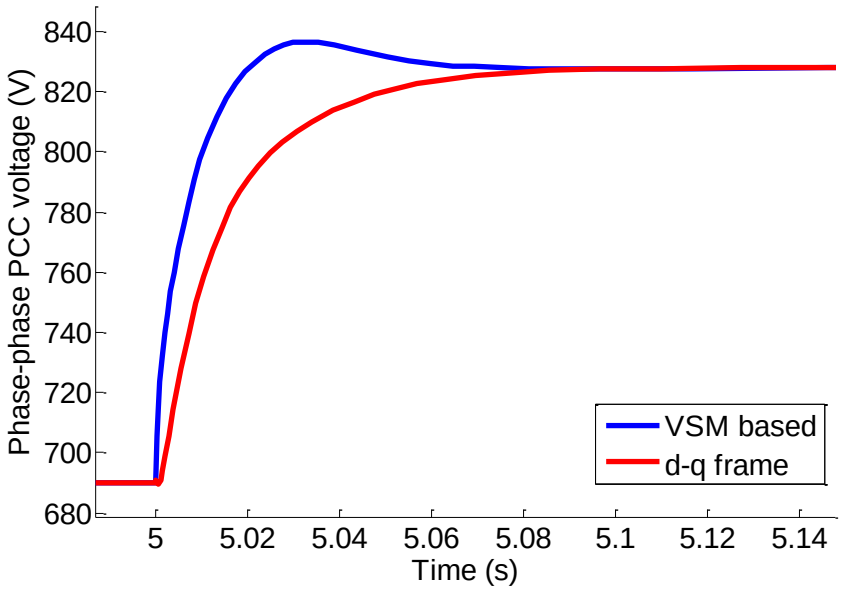

Figure IV-20 PCC voltage regulation performance when reference changes

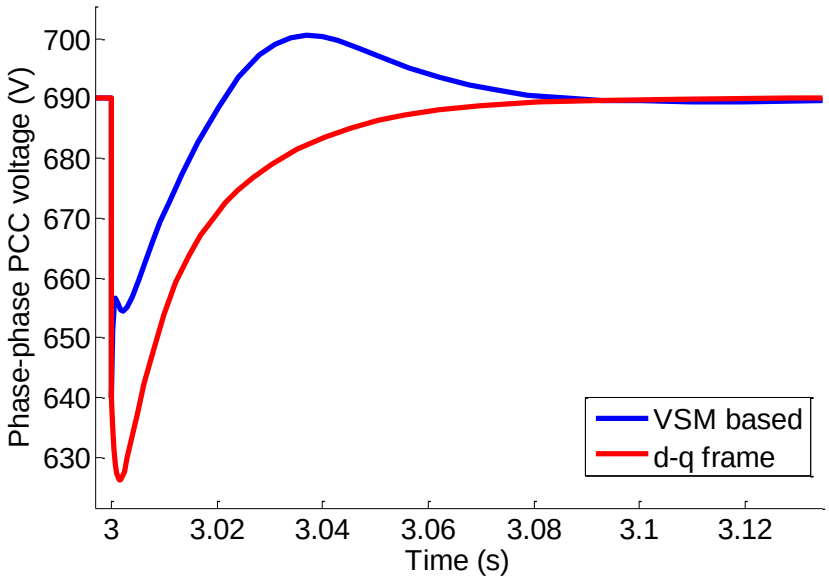

Figure IV-21 PCC voltage regulation performance during voltage sag

The advantage of the VSM-based controller is more significantly shown in Figure IV-22. The input power to the wind farm varies by 0.25 pu and hence the frequency of the output voltage will fluctuate around the nominal value and finally come back to it. It takes much long time to reach the steady state because the STATCOM has little capability of frequency regulation and the oscillation of frequency will not stop until there is no power imbalance applied in the rotating shaft in the wind turbine. As observed, the VSM-based controller regulates the PCC bus voltage much better than the traditional d-q frame one. A reason is that the VSM-based controller acting like a synchronous machine can automatically participate in the frequency regulation using its inertia, which is actually the energy stored in the capacitor here, and thus absorb or provide some active power during the transients. This effect will be stronger if there is some energy storage device connected to the dc link because the energy of the dc capacitor itself is very small compared to the source active power rating. In that sense, the STATCOM is equipped with the capability of frequency regulation during the transient but the cost is very large because the active power provided must be comparable to the main power source. Although the direct influence of the effort to regulate the frequency may be a minor reason depending on operating conditions, the characteristic of the swinging axis of the VSM-based controller provides a better synchronization of the STATCOM to the grid and ensures exerting the compensating current in the proper phase with respect to the source voltage, regulating the PCC voltage magnitude better and facilitating the recovery process of the power imbalance of the source. Thanks to the swinging mechanics of

the virtual inertia, the VSM controller will not follow the phase of the PCC voltage but counteract the change, compensating against the voltage variation. Conversely, the phase information of the PLL-oriented d-q frame controller relies on the voltage it detects and the corresponding compensating current is injected to the grid regardless.

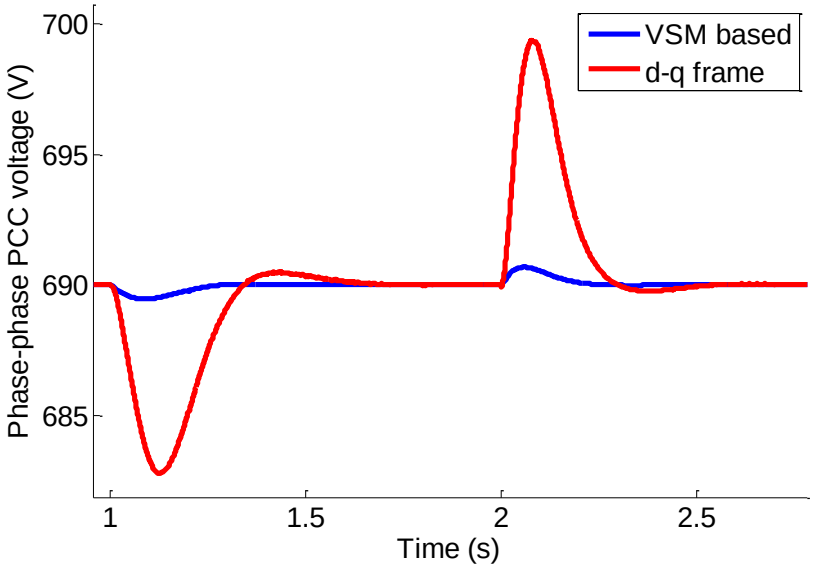

Figure IV-22 PCC voltage regulation when frequency fluctuates

4.5 Experimental verification

In order to verify the VSM control experimentally, a scaled-down prototype as Figure IV-23 is constructed in the laboratory. Because there is no generator running in the laboratory, it is replaced with a resistor load and the available tests are thus limited. In this case, the grid is providing power to the load when the STATCOM is still regulating the PCC bus voltage. Since there is only one power source in the system, the frequency is unique and no tests with frequency fluctuation can be done. With this test bed, the design for the VSM control can be verified and transient phenomena can be observed. Table IV-3 summaries the parameters of the test bed.

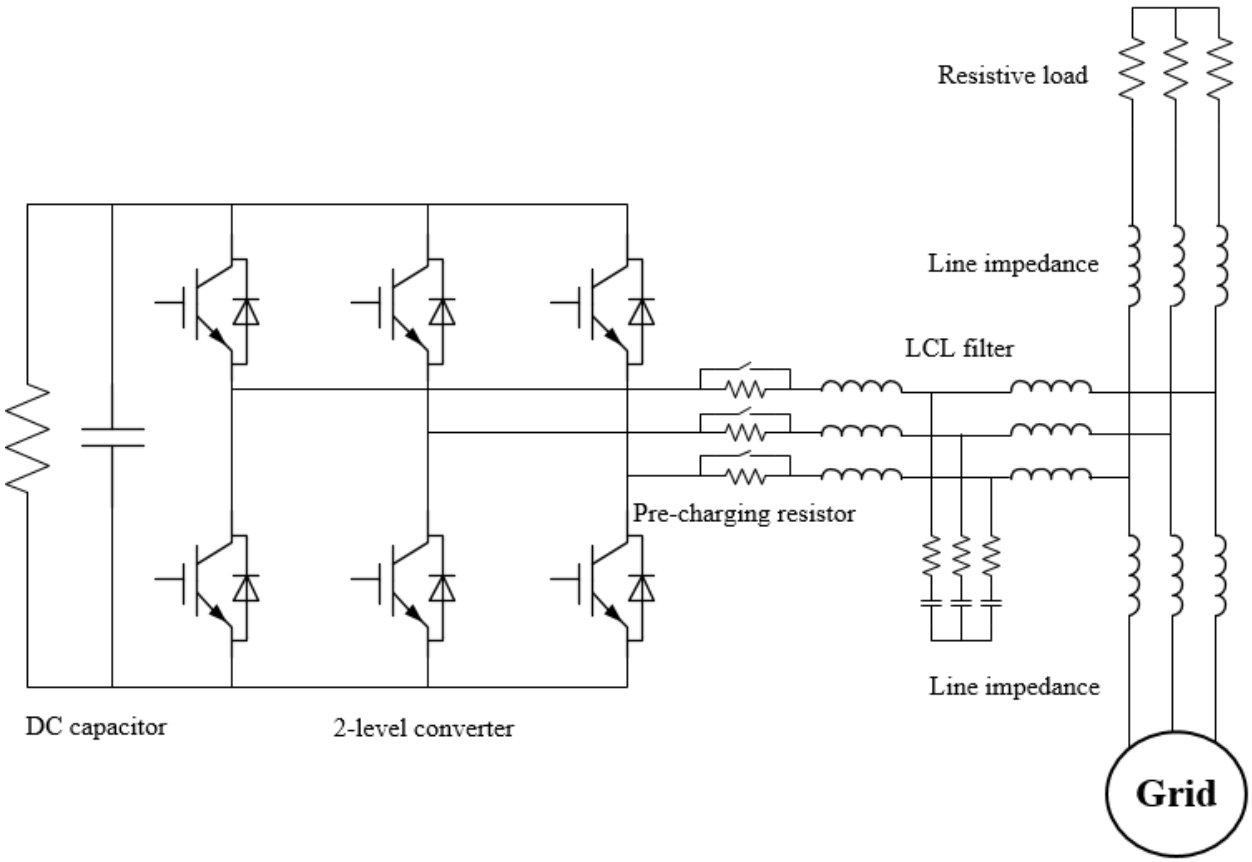

Figure IV-23 Schematics of prototype STATCOM with LCL filter

Table IV-3 Parameters of the prototype test bed

Symbol	Description	Value
V_{dc}	DC bus voltage	300 V
V_g	Grid ac bus phase to phase voltage	120 Vrms
$V_{PCC,\ uncomp}$	PCC bus phase to phase voltage, uncompensated	120 Vrms
$V_{PCC,\ comp}$	PCC bus phase to phase voltage, compensated	125 Vrms
Q	Output reactive power	1.65 kvar
I	Output current	7.66 Arms
R	Resistive load	15 Ω
L	Line inductor	1.2 mH

L_1	Inverter-side inductor of LCL filter	250 μH
L_2	Grid-side inductor of LCL filter	250 μH
R_c	Damping resistor of LCL filter	1 Ω
C	Capacitor of LCL filter	35 μF
C_{dc}	DC bus capacitor	600 μF
R_{dc}	DC bus discharging resistor	20 kΩ
R_{pre}	Pre-charging resistor	100 Ω
f_{sw}	Switching frequency	20 kHz

4.5.1 Hardware set-up

The experimental prototype of STATCOM with the grid and the load is shown in Figure IV-24 where the grid is emulated by a 3-phase ac power source, 6834b from HP and the converter is composed of a PM50CL1A060 IGBT module, controlled by a control board using a TMS320C28343 DSP card.

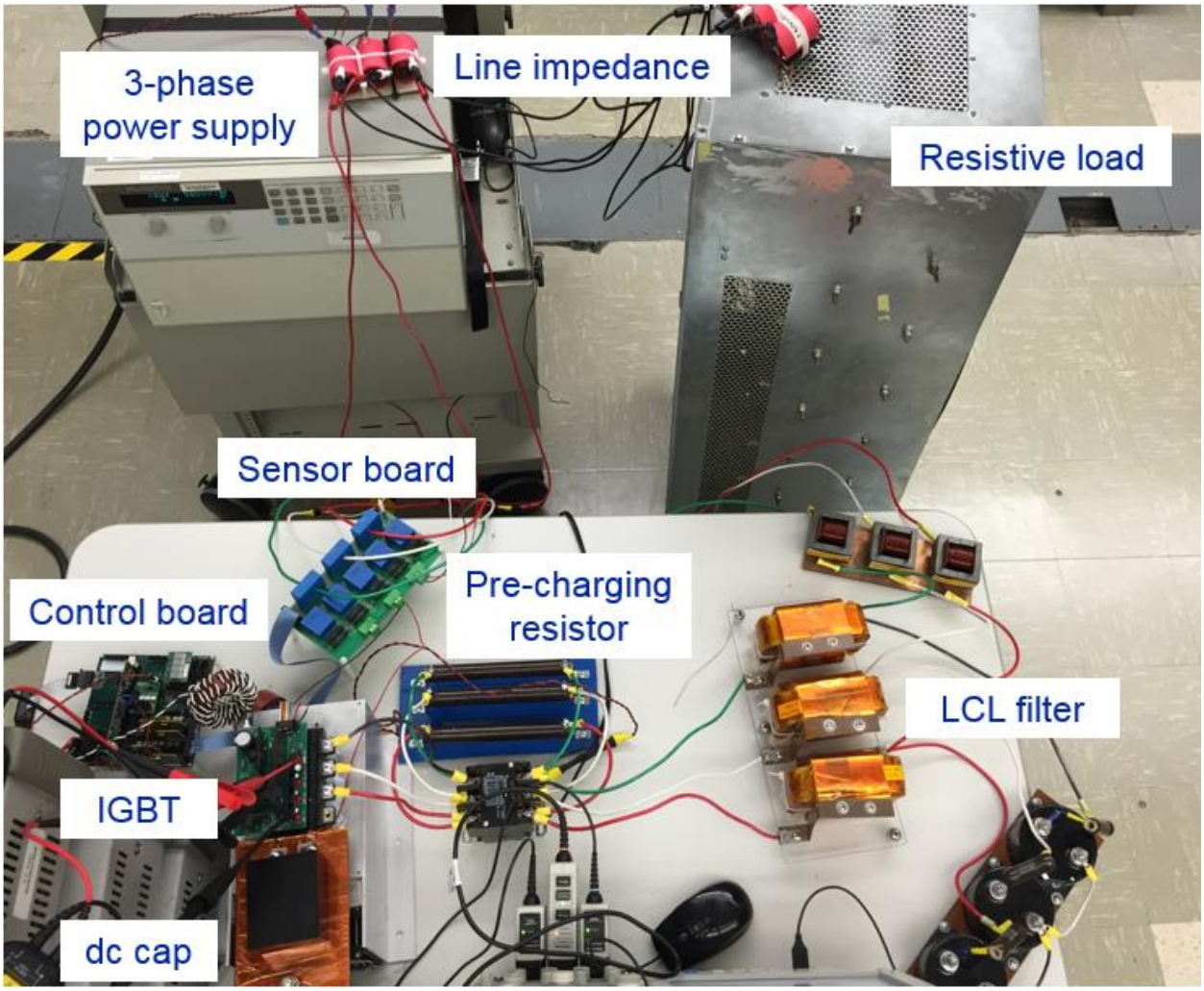

Figure IV-24 Hardware set-up for prototype STATCOM

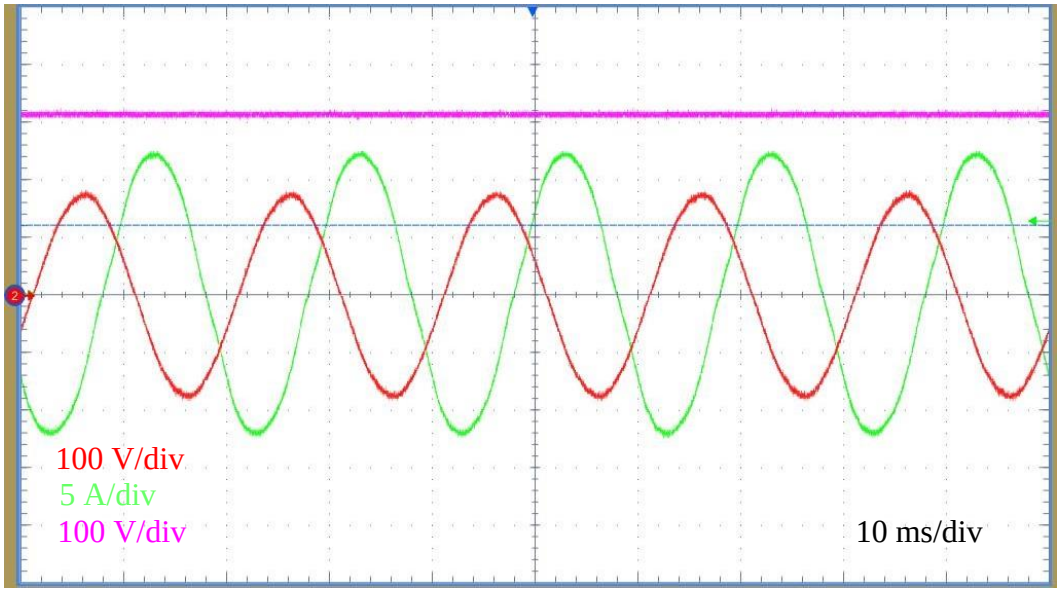

Figure IV-25 Steady-state waveforms of prototype STATCOM

Figure IV-25 shows the steady-state waveforms of the STATCOM where the green is the compensating current, the red is the PCC bus line to line voltage and the purple is the dc bus voltage. The current is lagging the line to line voltage for about 120 degrees, meaning that it is lagging the phase to neutral voltage for around 90 degrees with almost zero power factor. As seen the current waveform is good with the help of the LCL filter whose resonant frequency is around 2.1 kHz and also the attenuation of the current loop, yet with a little distortion due to dead time.

4.5.2 Transient responses

The two cases are conducted experimentally: PCC bus voltage reference step and grid voltage step. Figure IV-26 ~ Figure IV-33 show the results where the green is the compensating current, the purple is the dc bus voltage and the PCC bus voltage is extracted and calculated in MATLAB to show its rms value using Hilbert transform to obtain the envelope of the sinusoidal waveform so the noises are not directly reflecting the real noise on voltage.

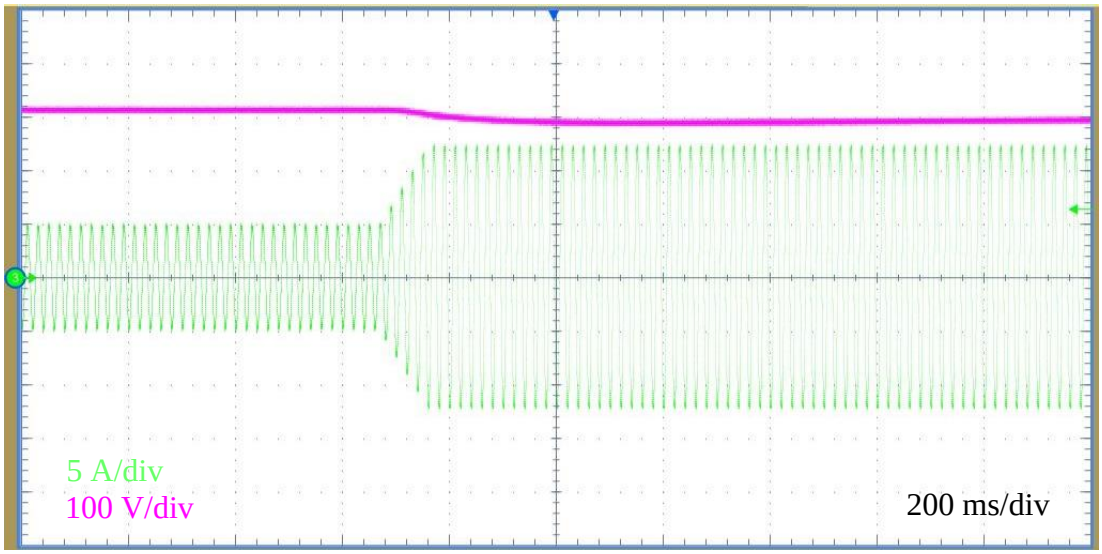

Figure IV-26 Waveforms when reference changes with D-Q controller

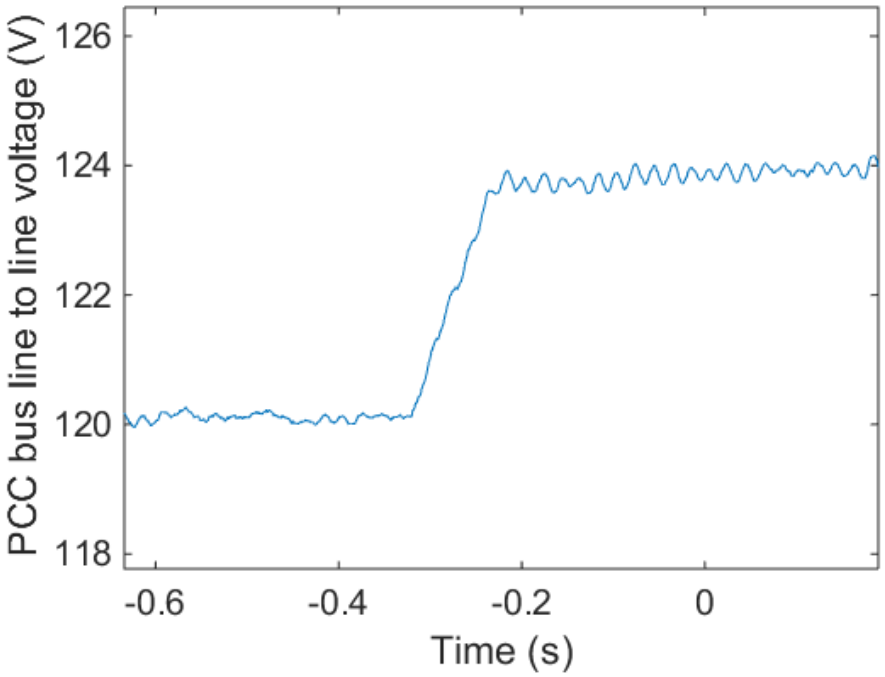

Figure IV-27 PCC voltage regulation performance when reference changes with D-Q controller

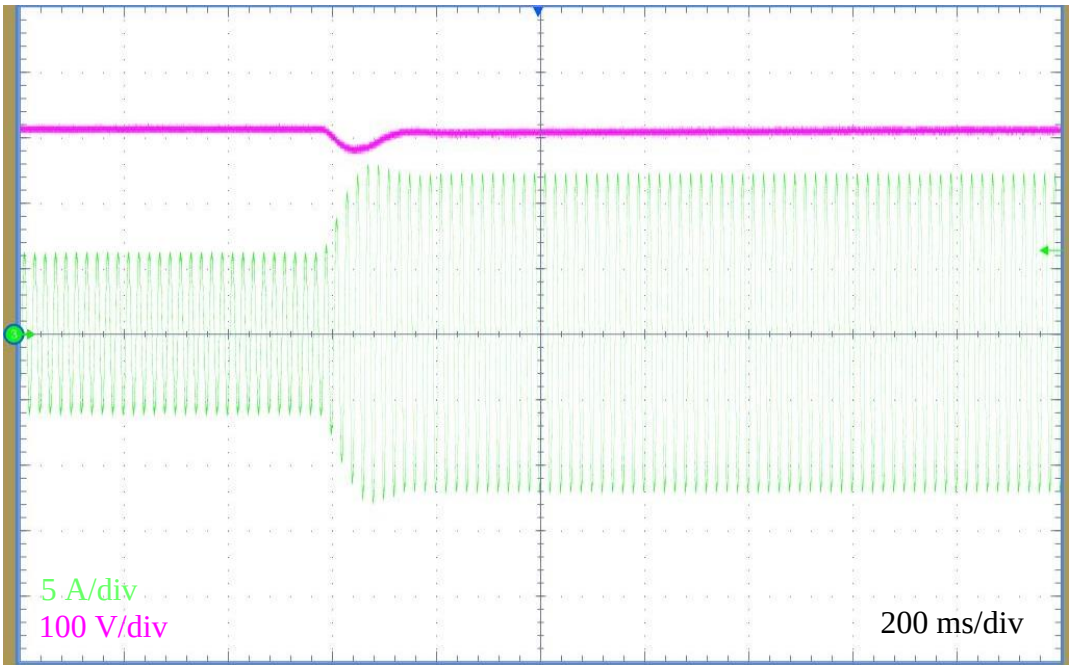

Figure IV-28 Waveforms when reference changes with VSM controller

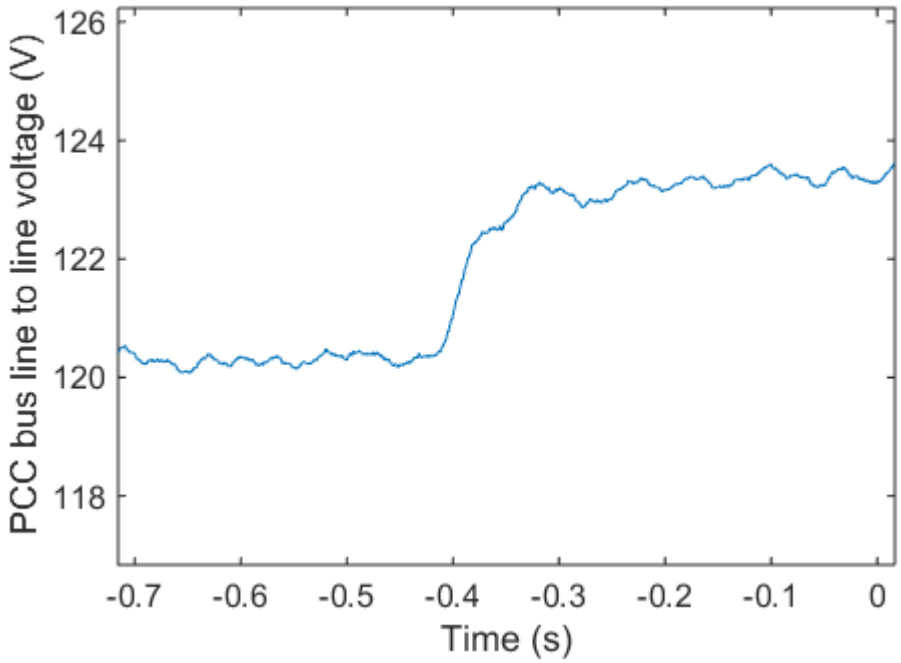

Figure IV-29 PCC voltage regulation performance when reference changes with VSM controller

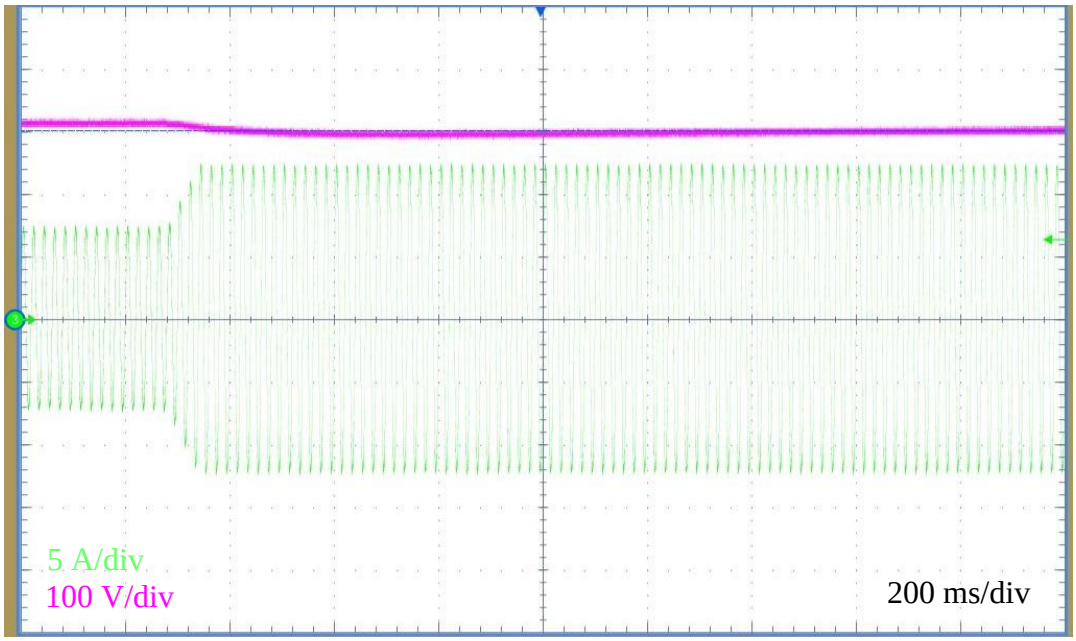

Figure IV-30 Waveforms during voltage sags with D-Q controller

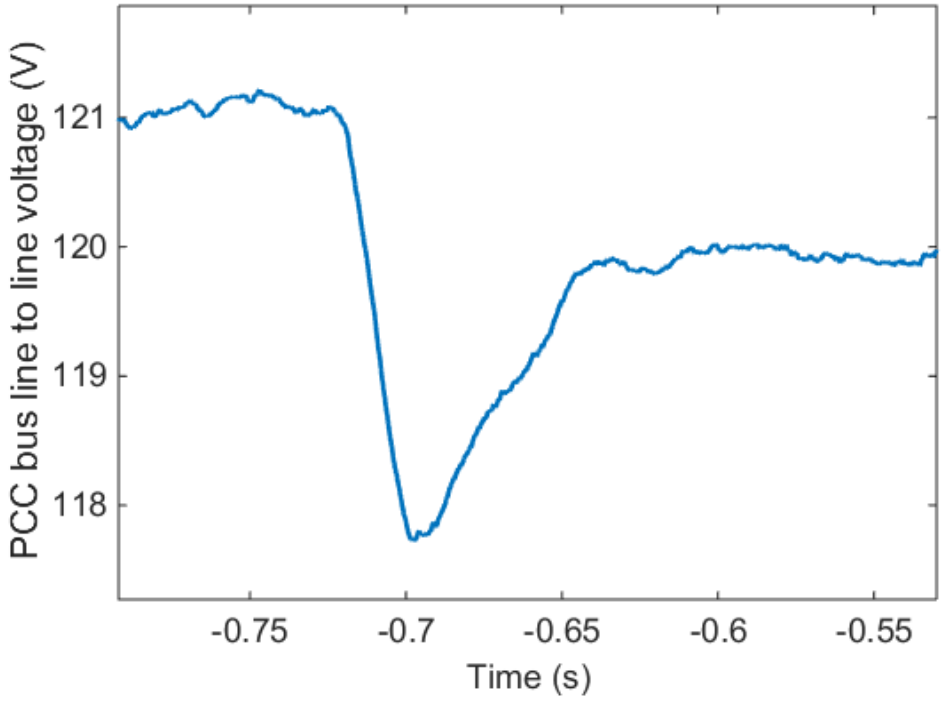

Figure IV-31 PCC voltage regulation performance during voltage sags with D-Q controller

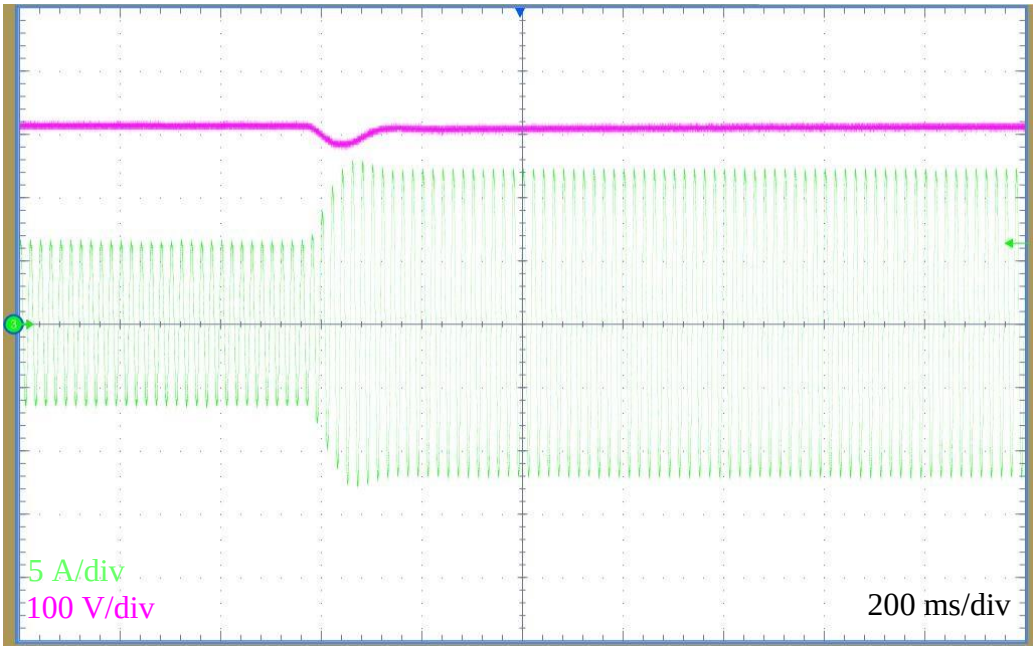

Figure IV-32 Waveforms during voltage sags with VSM controller

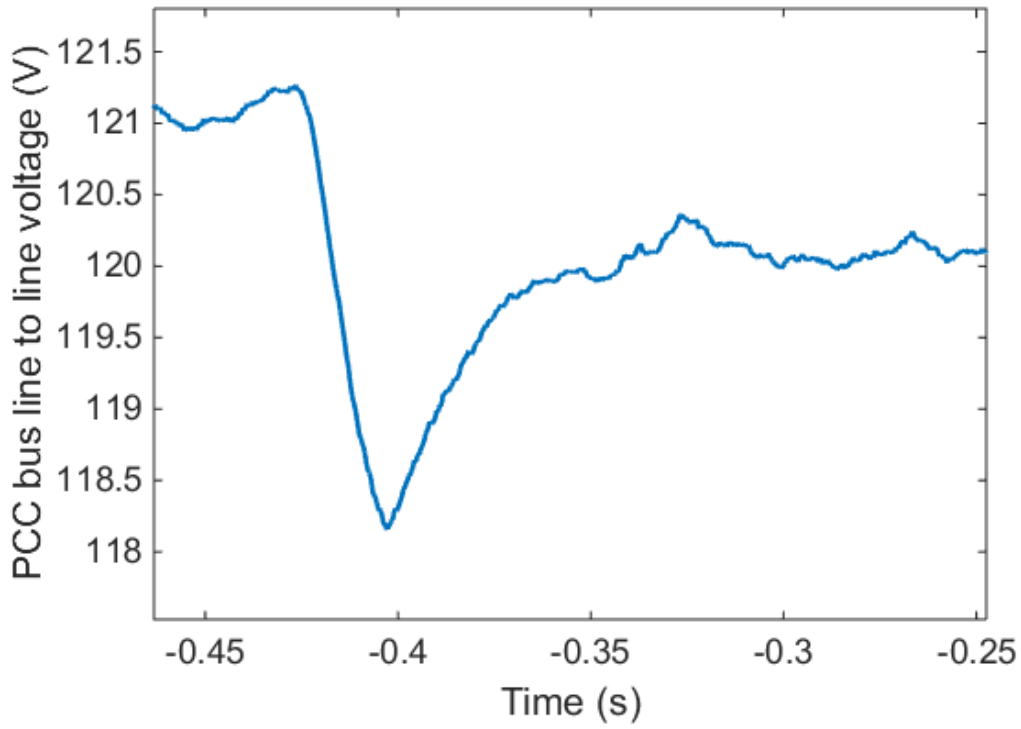

Figure IV-33 PCC voltage regulation performance during voltage sags with VSM controller

It is observed that the two controllers show similar dynamics, where the VSM controller presents a little larger voltage, which match the simulation results because in the two cases the voltage is the only changing variable. The difference can be more obvious if a larger line

impedance is used. Another observation is that the VSM-STATCOM always has larger variation in the dc bus voltage, indicating that active power is used during the transients inherently.

4.5.3 Transfer functions

The transfer functions in hardware are measured by sending small signal perturbations from the DSP code, sensing back desired signals and calculating in the DSP code provided by Software Frequency Response Analyzer (SFRA) from Texas Instruments.

Figure IV-34 ~ Figure IV-37 show the measured transfer functions of the current loop gains in d an q channels for the two controllers against simulation results. Note there is a significant difference above the line frequency where the simulation shows resonance while the experiment does not. It is because of the dead time, which causes the loss of duty cycle and add additional damping around the line frequency [128, 129]. The effect is more obvious in zero power factor cases because when the current crosses zero, the voltage is at its maximum. In the simulation, the average model is used and the dead time effect is not simulated. However, this in all is not a big issue since first the current bandwidth is higher than the resonant frequency and second it will be damped with loops closed. Except the resonance, the rest matches very well until half of the switching frequency at 10 kHz.

Figure IV-38 ~ Figure IV-41 show the measured transfer functions of the outer voltage loop gains for the two controllers against simulation results. The simulation and experiment results accord with each other very well except some mismatch in the dc voltage loop at low frequency range, which is introduced by the dc bus discharging resistor.

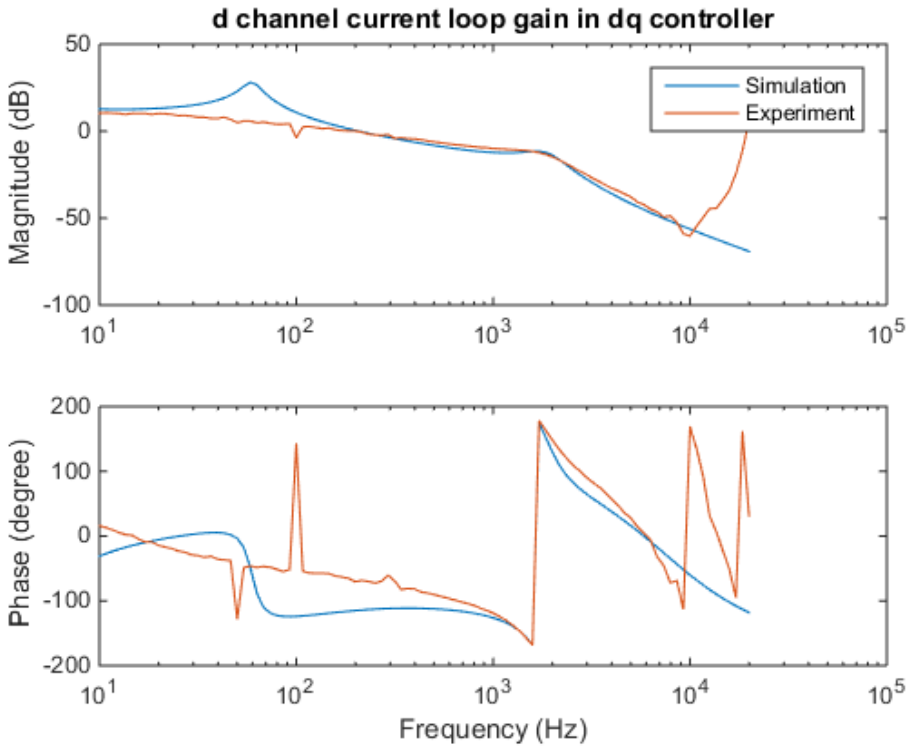

Figure IV-34 d channel current loop gain in D-Q controller

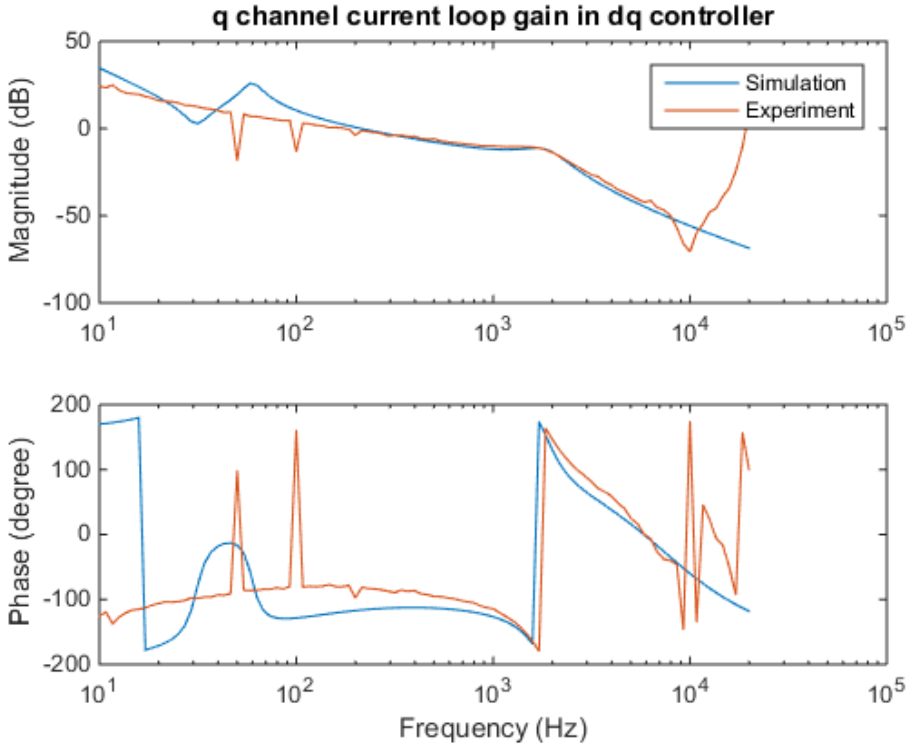

Figure IV-35 q channel current loop gain in D-Q controller

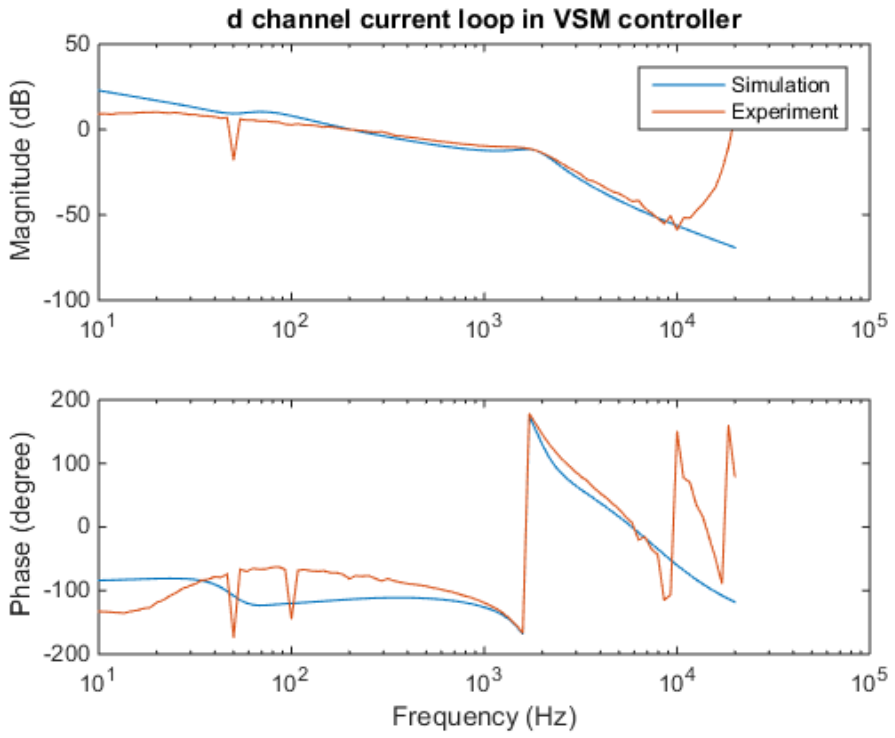

Figure IV-36 d channel current loop gain in VSM controller

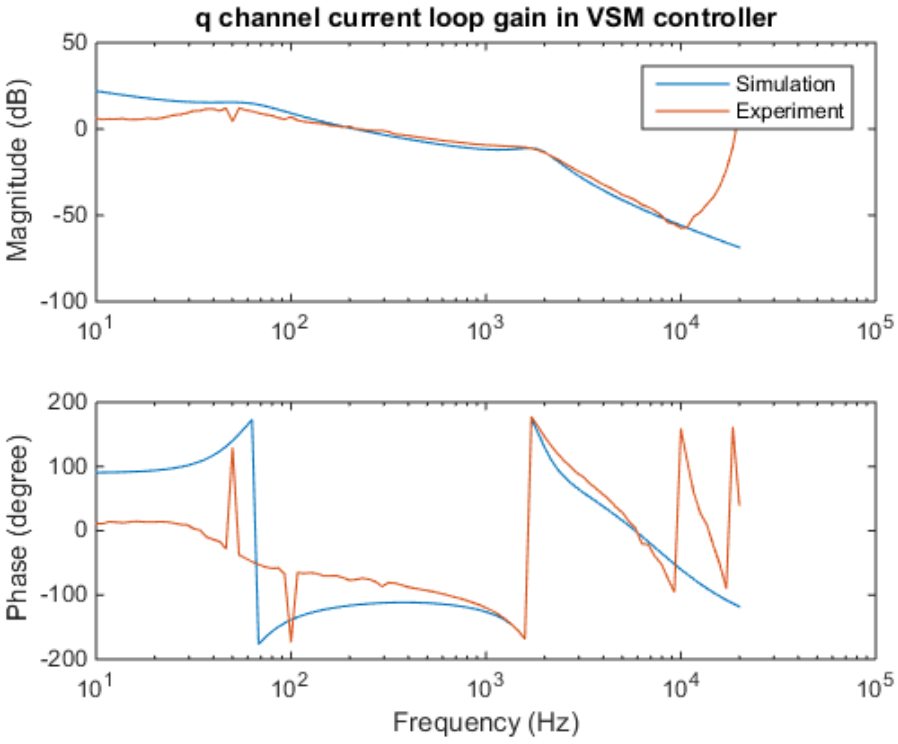

Figure IV-37 q channel current loop gain in VSM controller

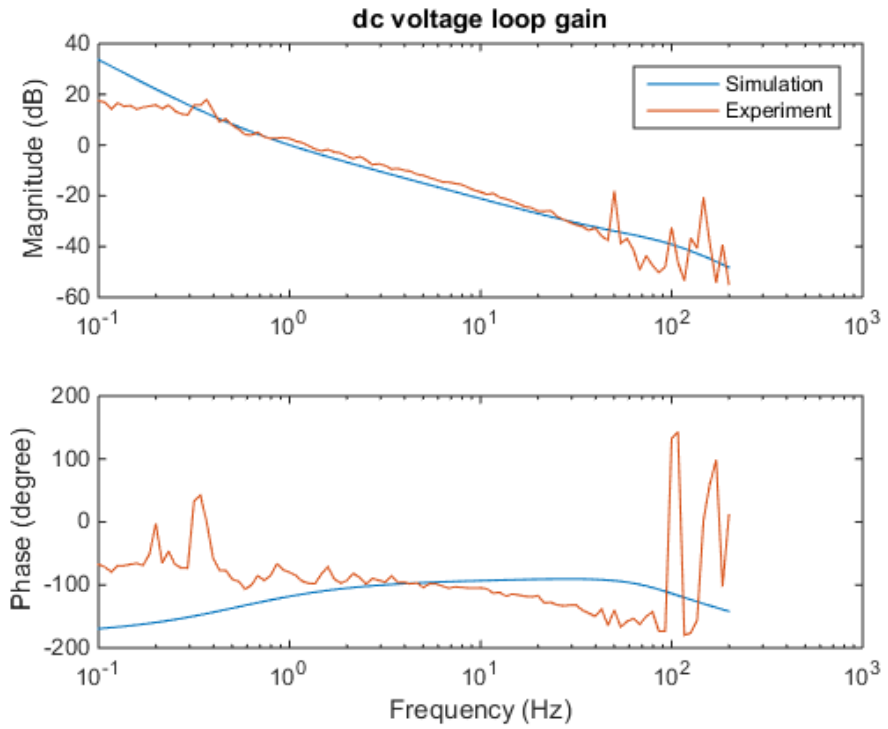

Figure IV-38 dc voltage loop gain in D-Q controller

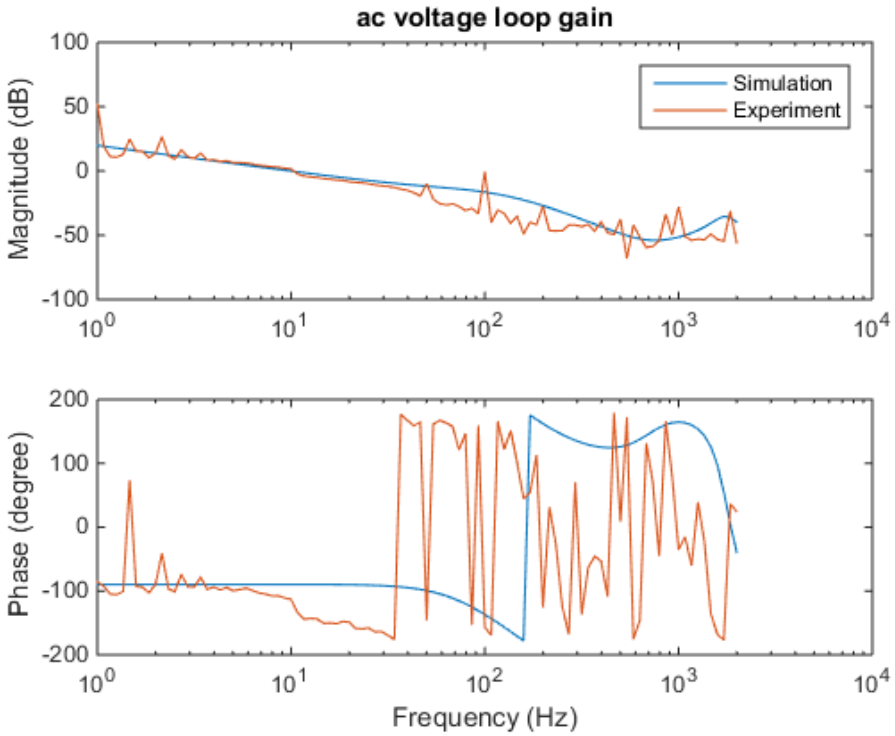

Figure IV-39 ac voltage loop gain in D-Q controller

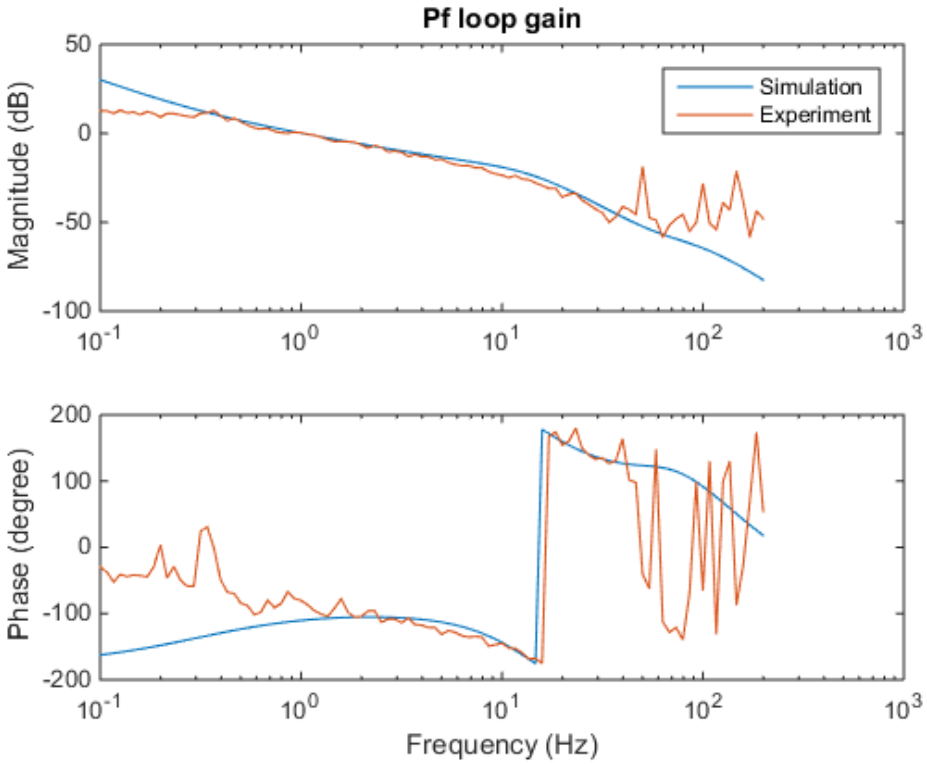

Figure IV-40 Pf loop gain in VSM controller

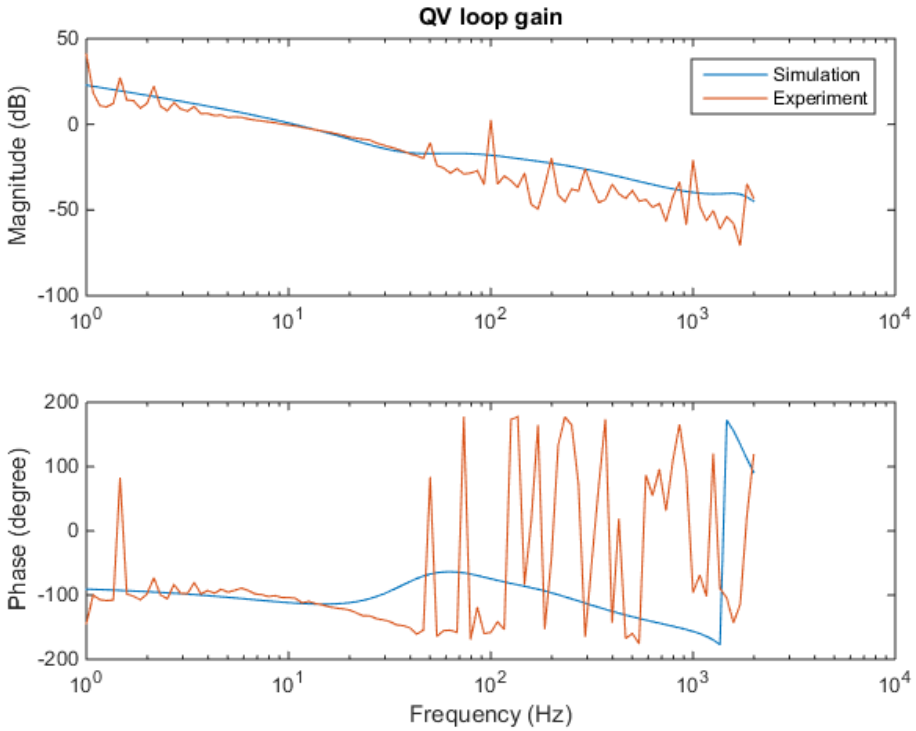

Figure IV-41 QV loop gain in VSM controller

4.6 A larger power system case study

In this section, the two controllers are evaluated in a larger transmission system as Figure II-20. It shows a 10-bus system divided into 2 areas with 5 buses and 2 generators on each side, connected with two tie lines. The generator 2 is a wind turbine, modeled as in the previous section 4.1 as a voltage source with varying magnitude and frequency without any advanced control while the other generators are traditional synchronous generators working in PV mode with the generator 4 being the reference bus. A STATCOM is connected at the output of the generator 2, helping regulate the PCC bus voltage by providing reactive compensation. The power flow calculation results in per unit are marked in the figure. The aforementioned two types of controllers are implemented in the STATCOM and the power system is simulated in MATLAB/Simulink. Again, they have the identical inner current compensators and the same bandwidths of corresponding loops as in Table IV-2.

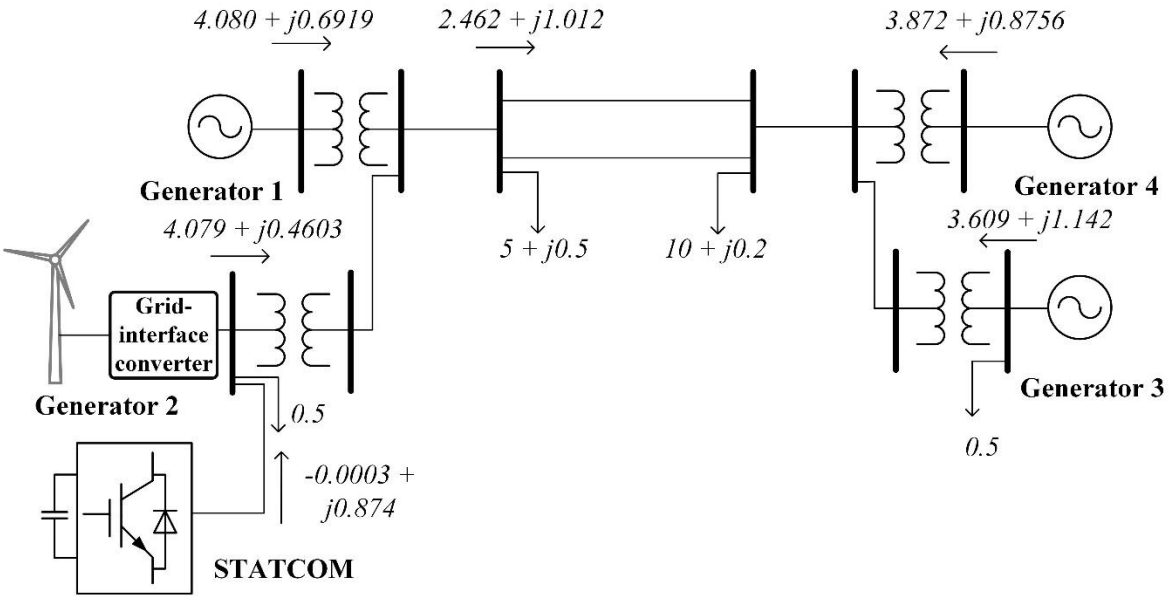

Figure IV-42 A 4-generator 2-area power system

The first test is to increase the reference of the PCC bus voltage from 1.0 pu to 1.05 pu. The PCC bus voltage and output power of the STATCOM are shown in Figure IV-43 and Figure IV-44 respectively. As in 4.4.2, only the ac voltage loop or QV loop is dominating so they perform similarly.

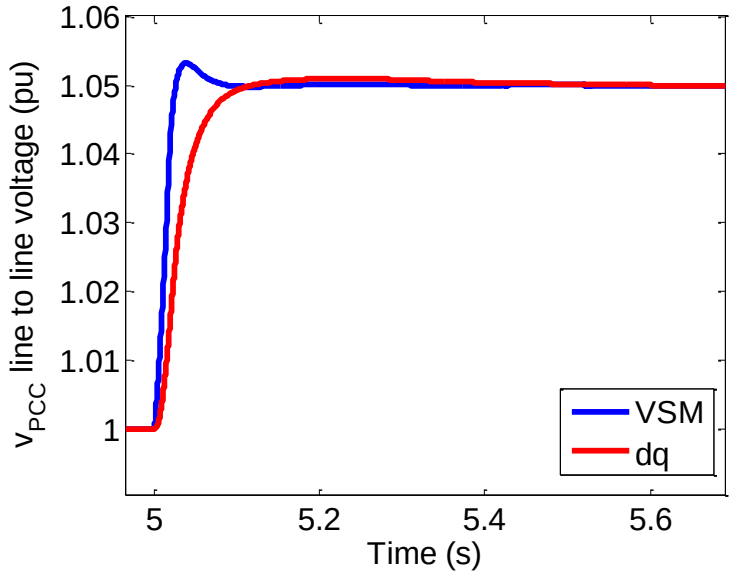

Figure IV-43 PCC voltage regulation performance when reference changes in a larger system

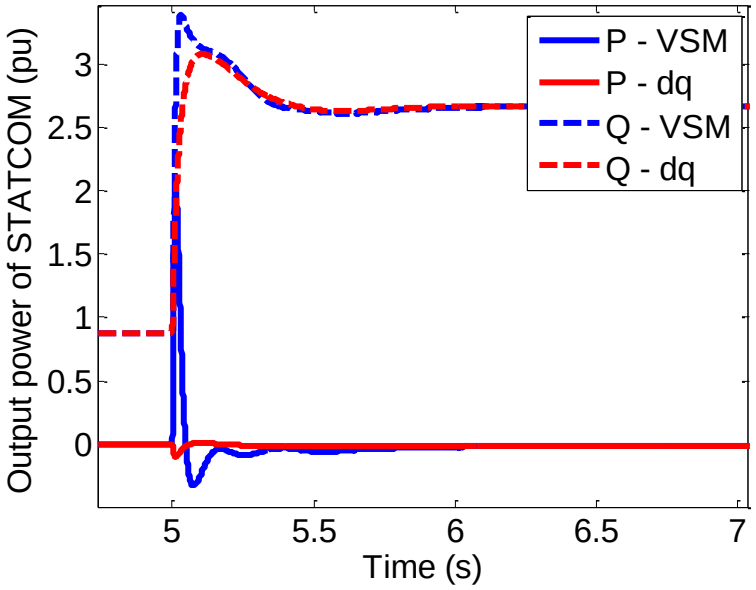

Figure IV-44 STATCOM output power when reference changes in a larger system

The second test is to apply an input power step down to the generator 2, causing the frequency oscillating. Similar to the results in 4.4.2, the VSM controller regulates the PCC bus voltage much better than the D-Q frame one because of the direction of its compensating current injection, shown in Figure IV-45. In Figure IV-46, the active power compensation of the VSM-STATCOM is obvious during the transients.

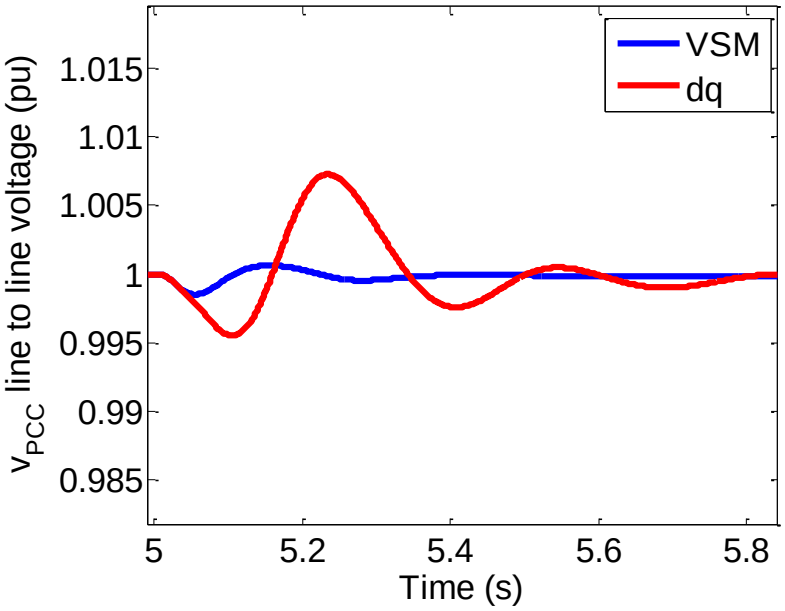

Figure IV-45 PCC voltage regulation performance when frequency fluctuates in a larger system

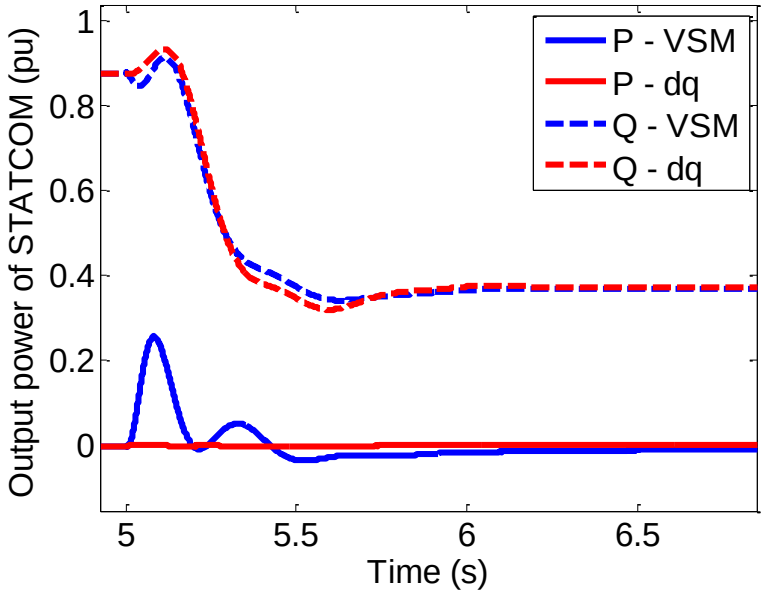

Figure IV-46 STATCOM output power when frequency fluctuates in a larger system

The third test is to make a step down to the excitation of the generator 2, resulting its terminal voltage fall. The VSM-STATCOM also shows a better regulation in Figure IV-47, unlike in 4.4.2, because this involves frequency variation due to the notable redistribution of the power flow.

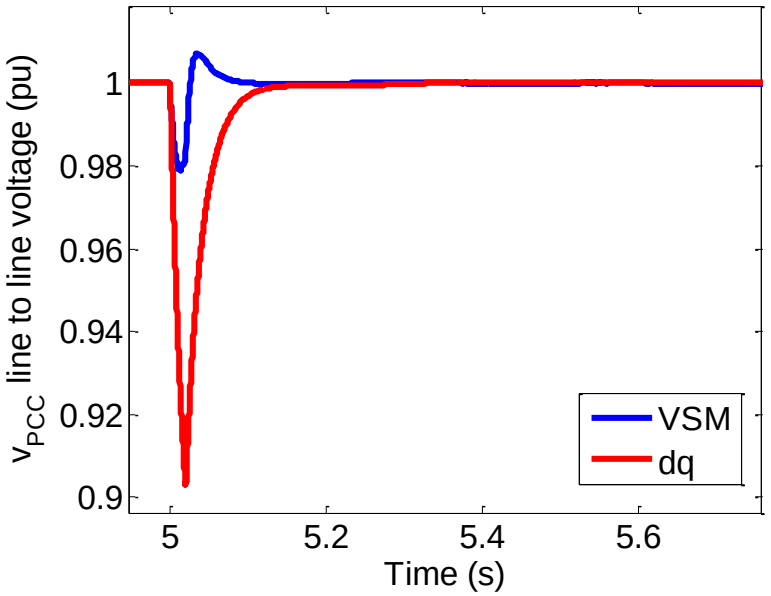

Figure IV-47 PCC voltage regulation performance when voltage sags in a larger system

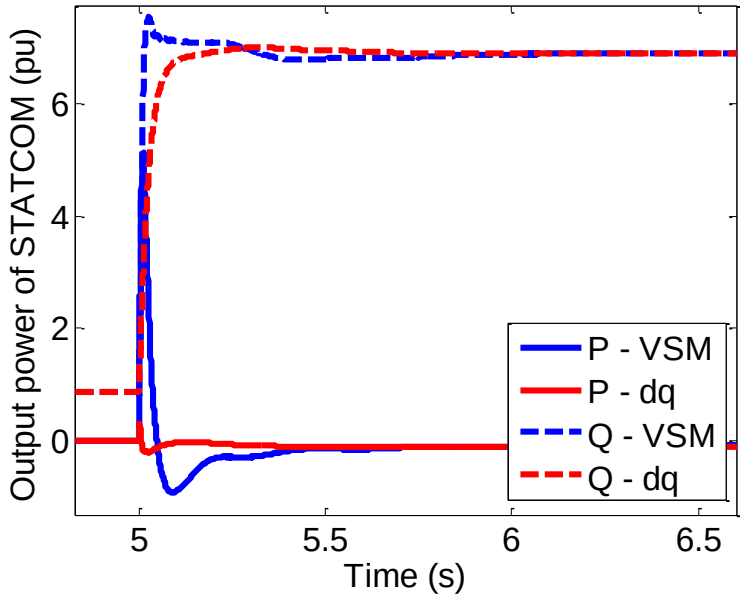

Figure IV-48 STATCOM output power when voltage sags in a larger system

The last test is to place a 3-phase fault in the middle of one of the tie lines, doubling the impedance. The VSM-STACOM again performs better regulation as in Figure IV-49 with its output power in Figure IV-50.

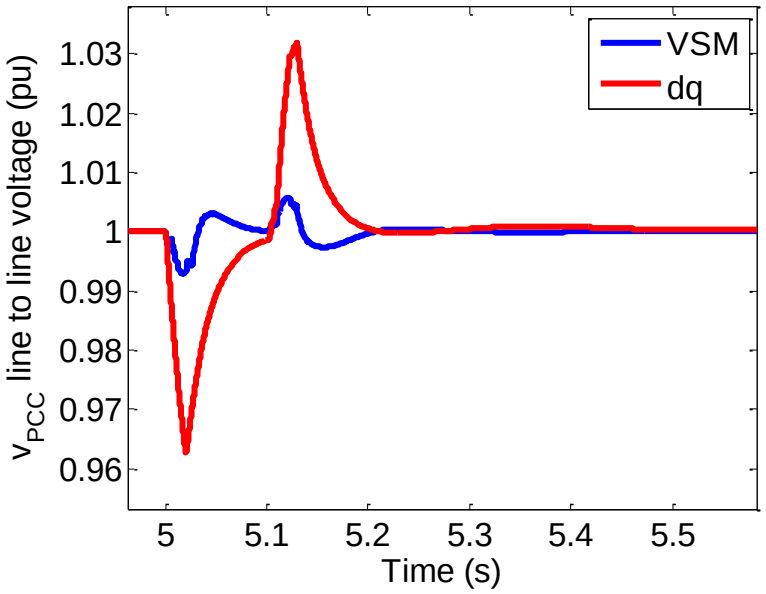

Figure IV-49 PCC voltage regulation performance during fault in a larger system

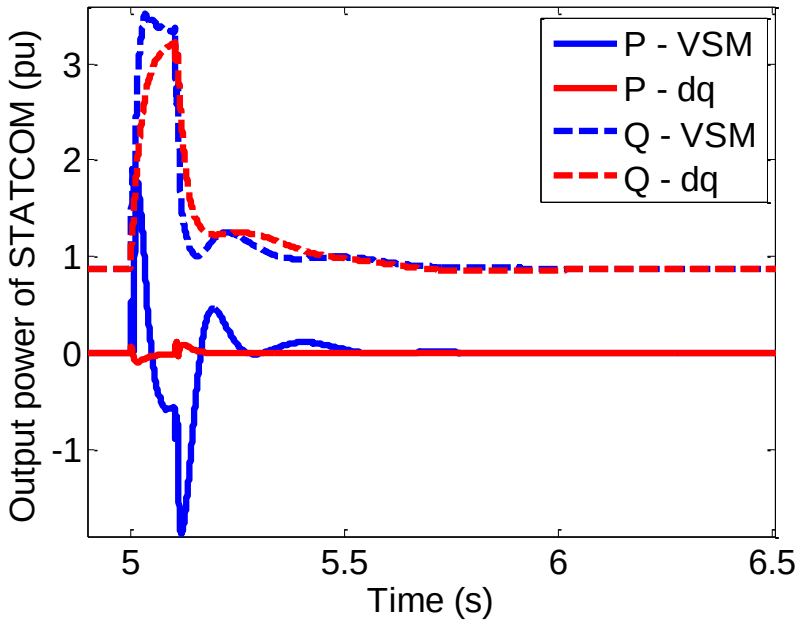

Figure IV-50 STATCOM output power during fault in a larger system

4.7 Summary

In this chapter, the VSM concept is applied to a STATCOM case and detailed small signal analysis is given. The design guideline is further proposed and the VSM controller is evaluated against the conventional D-Q frame controller in both frequency and time domain. It is found that

the VSM controlled STATCOM shows a significantly improved regulation performance under frequency fluctuation with the same current compensators and same bandwidths of outer voltage loops as the D-Q frame controller because of its different synchronization method. Additionally, the ac impedance of the VSM controller presents preferable regarding to stability issues.

Chapter V. PRACTICAL CONSIDERATIONS OF VSM-CONTROLLED STATCOM

The previous chapter discusses the VSM controller in a small signal sense around some given operating point, without consideration of large transients or start-up process. In this chapter, such practical issues are examined to complete the design of the controller and help to realize a hardware prototype.

5.1 Introduction

Since the VSM controller uses active power to synchronize, the utilization of stored energy is inevitable during transients, which can be a double-blade sword if not controlled properly, especially for the STATCOM application where reactive power compensation is the main purpose and concern. For example, a potential problem lies in the fact that there is no primary source providing active power in a STATCOM because it is mainly designed for reactive power compensation. For conventional D-Q frame STATCOMs, this is not a big concern because the decoupling control of active and reactive power and the PLL tracks the PCC voltage. Therefore when there is a fault, the PLL still locks the PCC voltage, only the output reactive power will grow up till the limit when the active power increase a little according to the increased losses. On the other hand for the VSM controller, the power loop will swing and adjust its phase position to satisfy the fault conditions while the active power compensation is taking place inherently. If a severe contingency occurs or a contingency lasts too long, too much active power could flow in or out of a VSM-STATCOM, making the dc capacitor voltage vary dramatically, possibly resulting in the dc voltage exceeding the maximum value of the switching devices and the capacitor itself, or the dc voltage dropping below the minimum value required to operate as an inverter.

To explain that, let us assume a three-phase-to-ground fault happens at the grid terminal at t=5s for 0.05 seconds in the test case in Chapter 2, which is a critical fault. The average model simulation results in Figure V-2 show that under such a scenario the VSM-STATCOM will fail because the dc bus voltage will be too low to operate as an inverter, which will leads to the controller being unable to control the STATCOM. Figure V-3 shows the active power transfer between the STATCOM and the rest of the system where the VSM-STATCOM presents much

greater active compensation during and after the fault than the DQ-STATCOM, which causes the problem described previously.

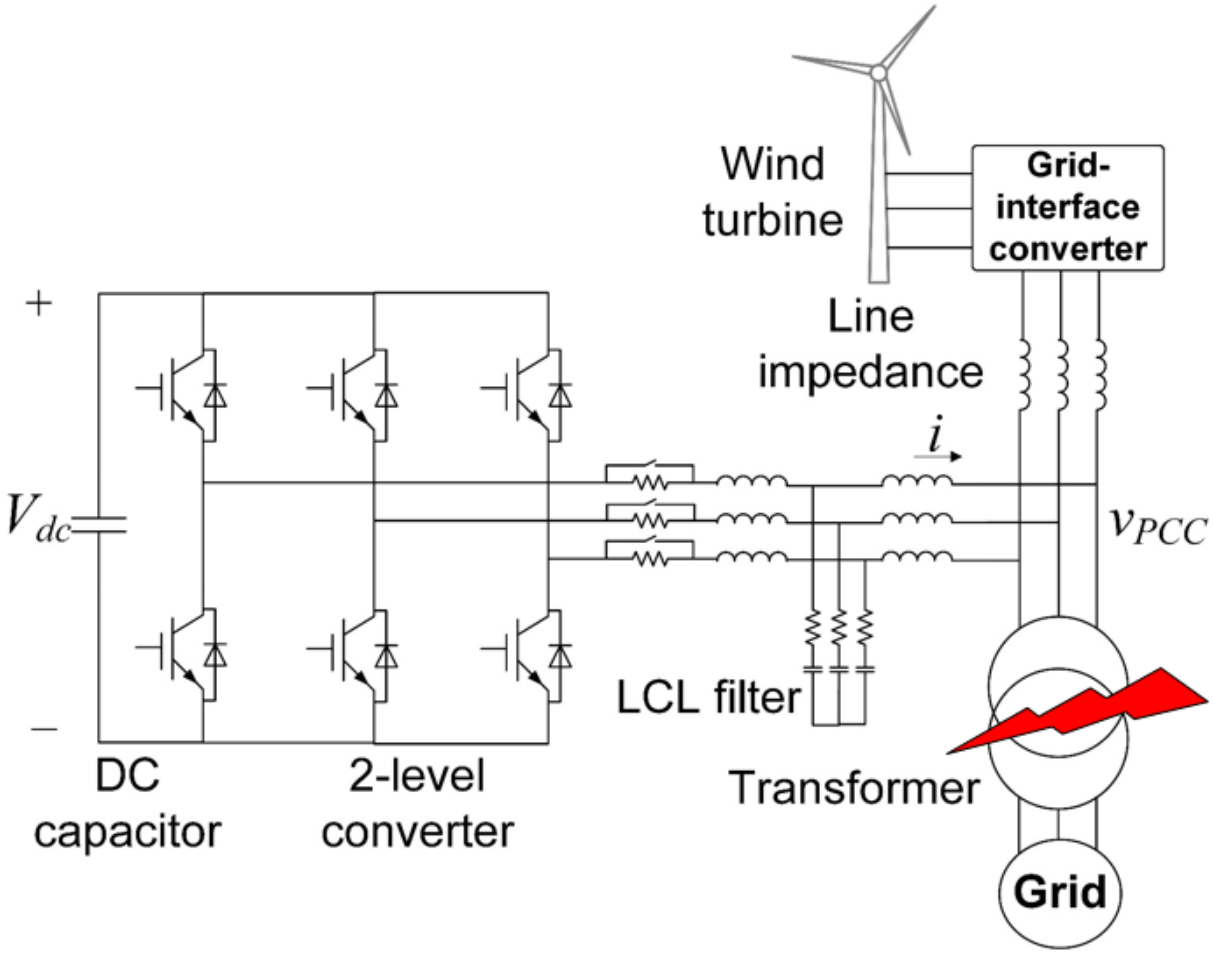

Figure V-1 Three-phase fault in the test bed

Note that this phenomenon is not unique in the STATCOM case. For a generic VSM-controlled converter, since the loop to regulate dc bus voltage or to control input power is relatively slow compared to faults, it is almost impossible for it to adjust its reference to maintain the dc bus voltage but just leave the power loop to take over. Therefore large transient analysis is necessary.

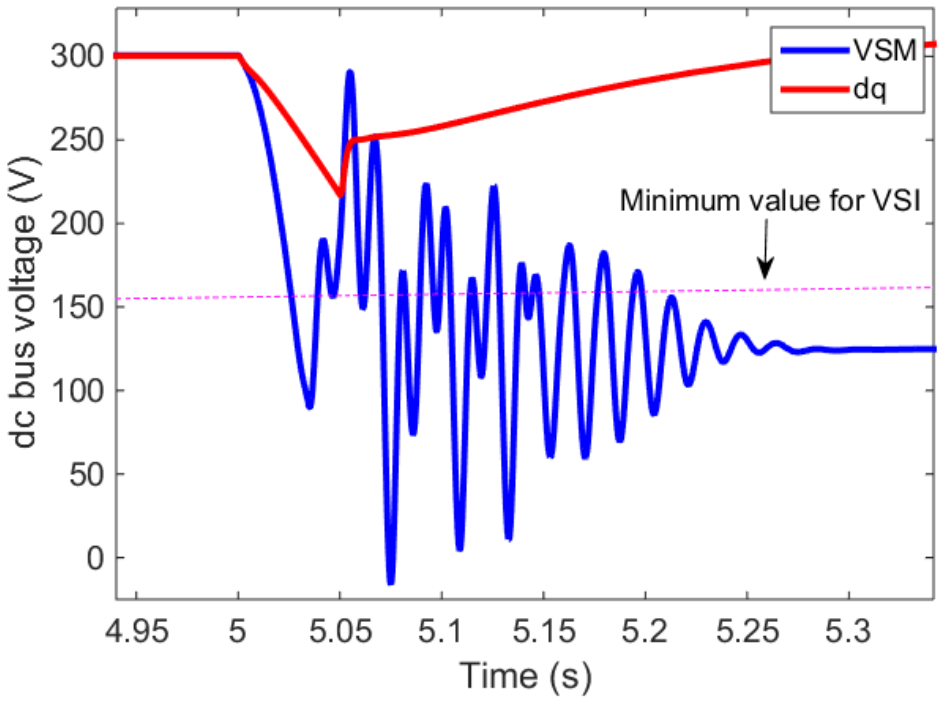

Figure V-2 Dynamics of dc bus voltage of two controllers under fault

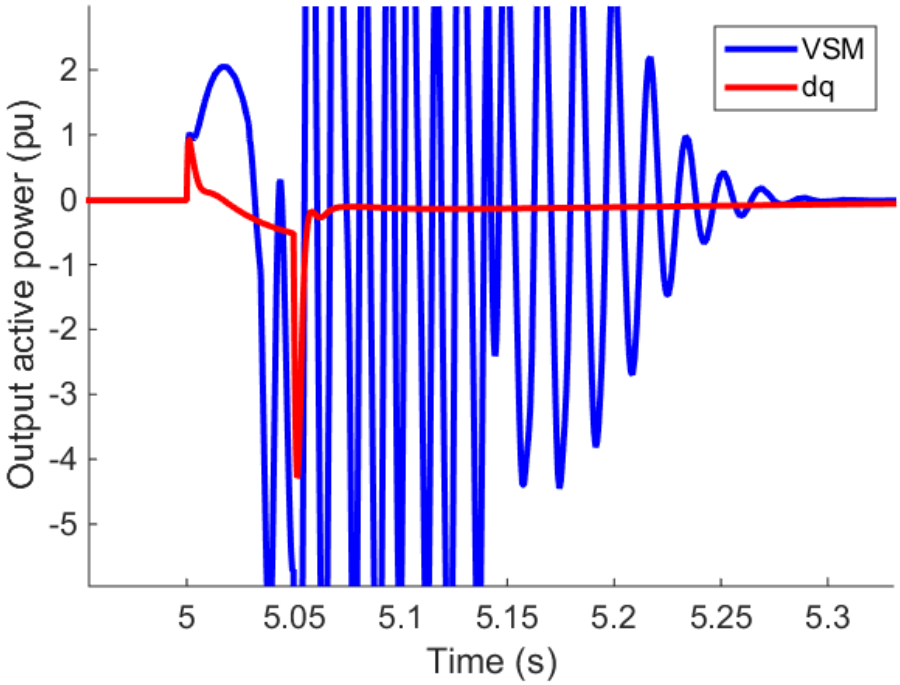

Figure V-3 Dynamics of output active power of two controllers under fault

5.2 Analysis on large transients

5.2.1 Preliminary assumptions

To start with, the following assumptions are made throughout the analysis.

First, the PCC voltage is constant during faults. This is actually assuming that 3-phase balanced faults happen at near ends and thus the PCC voltage is clamped by the ground or any impedances and sources left. Also 3-phase faults are considered in order to look into the worst case.

Second, the current loops work fast enough to be ignored. This is typically true because the current bandwidths are relatively high for a converter with PWM techniques. Therefore the current will be equal to its reference during discussed transients.

Third, the Pf loop doesn't change much during the transients. This is also because of its relatively low bandwidth. So the input power usually remains constant.

Fourth, the QV loop is frozen or saturated. Due to large changes in the PCC voltage, its compensator will accumulate errors so fast that it will hit the limit and be clamped to be a constant as well. But to simplify analysis, the magnitude of the back EMF is first set unvarying before and after faults in this section 5.2.

Note that the last two assumptions are not necessarily true at all time and the analysis will be extended where those two assumptions are not valid in the following section.

5.2.2 Phasor analysis

To gain a comprehensive understanding of the dynamics behind, phasor diagrams are plotted in Figure V-4. The black phasors are before the fault happens, in (a) the red phasors are the moment when the fault happens and in (b) the red phasors are the steady-state under the fault if time allows.

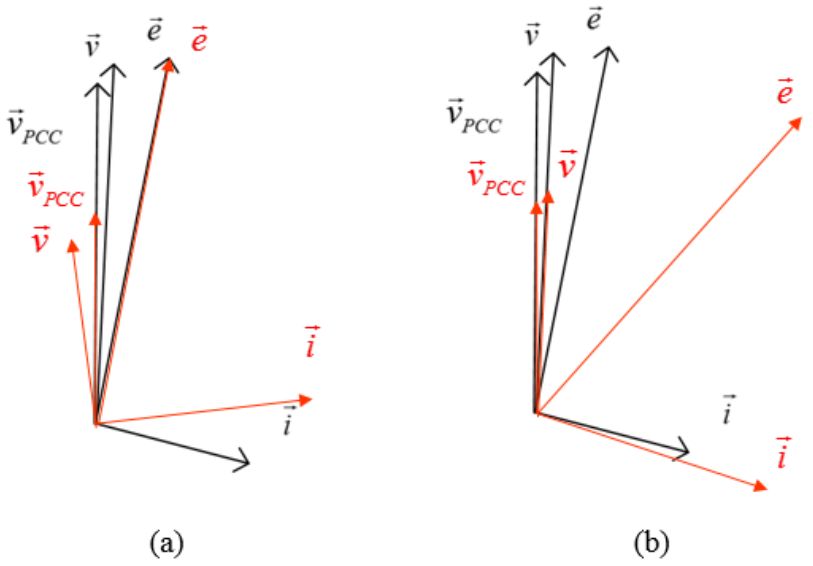

Figure V-4 Phasor diagrams of VSM-STATCOM during faults

Before the fault, the terminal voltage phasor $\vec{v}$ lags the PCC voltage phasor $\vec{v}_{PCC}$ by a small angle, which is exaggerated in Figure V-4, meaning that the STATCOM is absorbing some amount of active power due to losses in the STATCOM such as switch losses and the resistive losses of the filter and cables. The difference between these two phasors is physically the voltage drop on the filter. The compensating current phasor $\vec{\imath}$ lags $\vec{v}$ by a little more than 90 degrees, which is magnified in the figure as well, meaning that the STATCOM is absorbing some active power from the grid. The virtual back EMF phasor $\vec{e}$ is in the position according to the virtual impedance for given $\vec{v}_{PCC}$ and $\vec{\imath}$.

When the fault occurs, like presented in Figure V-4(a), the PCC voltage suddenly $\vec{v}_{PCC}$ drops to a very small value when the back EMF $\vec{e}$ stays where it is. The current $\vec{\imath}$ governed by the difference of $\vec{v}_{PCC}$ and $\vec{e}$ and the virtual impedance moves, and it then determines the terminal voltage $\vec{v}$. As in the figure, $\vec{v}$ is ahead of $\vec{v}_{PCC}$, indicating that the active power flow direction reverses and the STATCOM is providing some active power to the grid, thus causing the dc bus voltage to drop.

Meanwhile, the power loop starts working to slow down so as to decrease the phase of the back EMF $\vec{e}$, searching for the new steady-state as shown in Figure V-4(b) where the output power comes back to be equal to necessary losses. Before that position, the STATCOM keeps delivering active power to the grid with the dc bus voltage decreasing and beyond that the voltage goes up.

If it takes more time to reach the steady-state position the first time than the fault lasts, the dc bus voltage will decline all the way during the fault. If not, the voltage tends to rise because now the STACOM is taking more active power than it needs. Afterwards the voltage continues to oscillate until the dynamics of the power loop die out. Due to damping in the controller and resistors in the circuit, the maximum energy transferred is when the back EMF $\vec{e}$ arrives the steady state position or when the fault is cleared if the dynamics are too slow. If the dc bus voltage falls below the minimum allowable value, then the STATCOM will stop running as an inverter and collapse. As a result, the time period is critical as for whether the converter can stand during the fault. It can be inferred that a larger *M* which slows down the dynamics leads to more energy transferred.

5.2.3 State-space equations

With the assumptions in 5.2.1, the state space equations of the power stage with the VSM controller are simplified as (3) just describing the dynamics of the power loop and the virtual impedance. Because of the large disturbances brought by the fault, the trigonometric functions cannot be linearized and hereby the equations remain non-linear which are better solved numerically using the Runge-Kutta method.

$$\begin{cases} \dfrac{\mathrm{d}i_d}{\mathrm{d}t} = -\dfrac{R}{L} i_d + \dfrac{E - V_{PCC}\cos\delta}{L} \\ \dfrac{\mathrm{d}i_q}{\mathrm{d}t} = -\dfrac{R}{L} i_q - \dfrac{V_{PCC}\sin\delta}{L} \\ \dfrac{\mathrm{d}\delta}{\mathrm{d}t} = \Delta\omega \\ \dfrac{\mathrm{d}\Delta\omega}{\mathrm{d}t} = -\dfrac{D}{M}\Delta\omega - \dfrac{1}{M}\left(i_d V_{PCC}\cos\delta + i_q V_{PCC}\sin\delta\right) \end{cases} \tag{3}$$

All the variables in (3) corresponds to Figure IV-4 where the magnitude of the back EMF $E = e_d$ because its q channel value equals to zero. As long as those variables before the faults are known, the state-space equations are solvable and able to predict the following dynamics of the system under the assumptions made.

If the same fault happens again with the back EMF fixed or frozen at a given value (here it is chosen to be constant all the time), the calculation and simulation results are compared in Figure

V-5 and Figure V-6. It is shown that the state space model matches the average model in simulation very well.

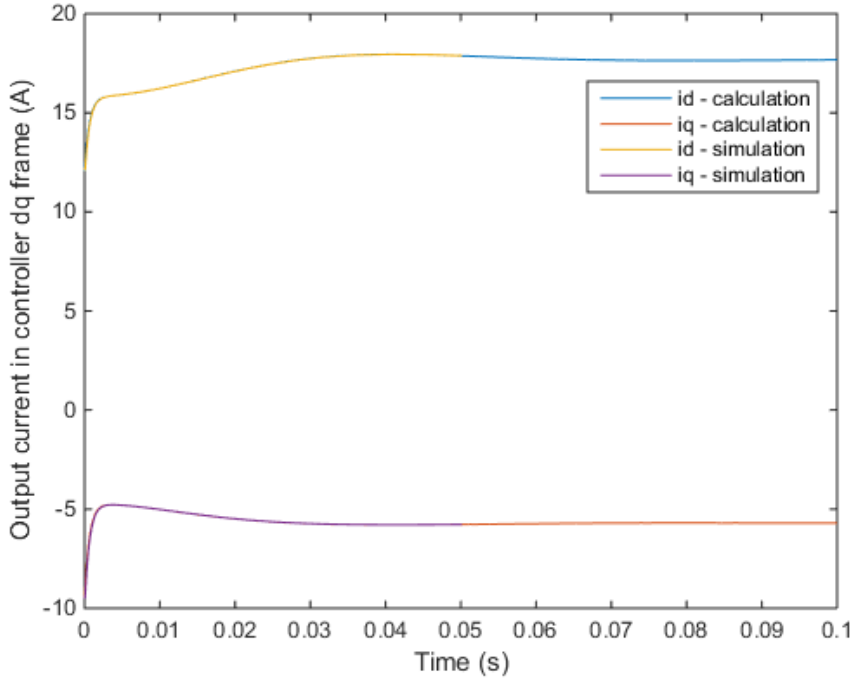

Figure V-5 Transients of output current in controller D-Q frame during fault with constant back EMF

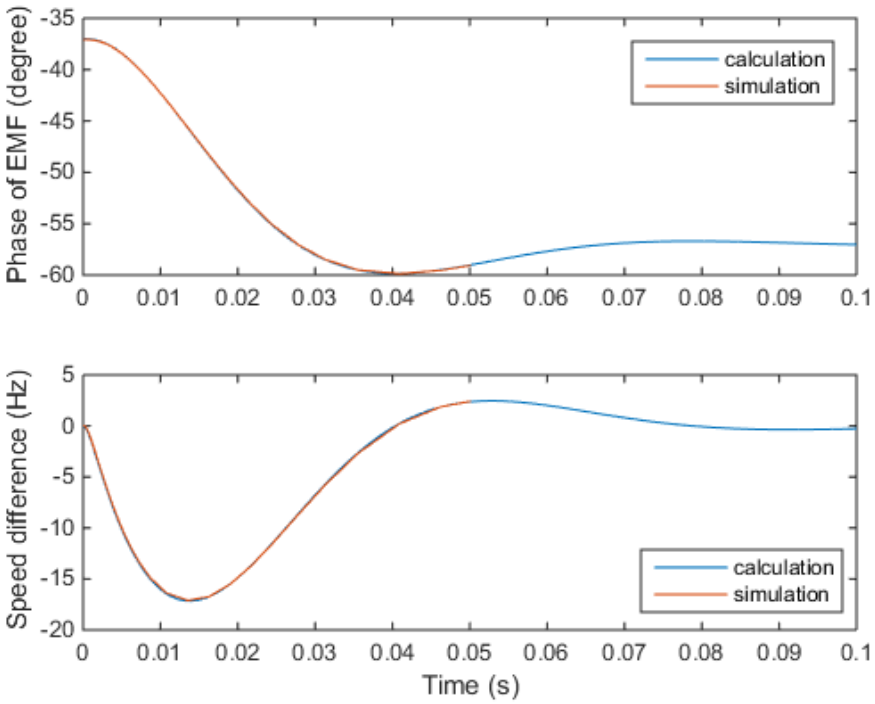

Figure V-6 Transients of frequency and phase of back EMF during fault with constant back EMF

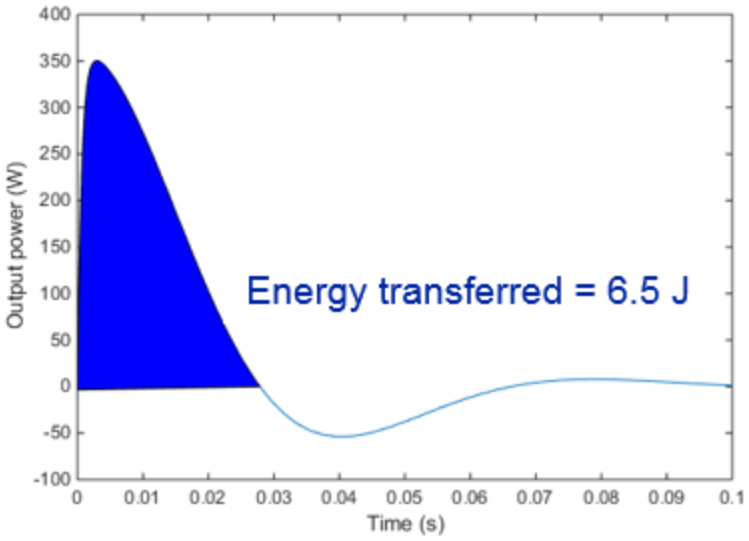

Figure V-7 Transients of output power during fault with constant back EMF

The output power and the maximum energy transferred during the fault, which is the integral of the output power from when the fault starts to when the power equals to zero first time or when the fault is cleared, can then be calculated in Figure V-7 where the shaded area presents the maximum energy. Having the energy in hand, the maximum dc bus voltage change is obtained according to (4) where W is the transferred energy, C is the dc capacitor value, V_{dc0} is the dc bus nominal voltage and ΔV_{dc} is the change in the dc bus voltage. Given the dc bus nominal voltage equal to 300 V, the lowest dc bus voltage is about 261 V and it matches the simulation results in Figure V-8, verifying the accuracy of the state space model.

$$\Delta W = \frac{1}{2} C \Delta \left(V_{dc}^2 \right) = \frac{1}{2} C V_{dc0}^2 \left[\left(\frac{\Delta V_{dc}}{V_{dc0}} + 1 \right)^2 - 1 \right] \qquad (4)$$

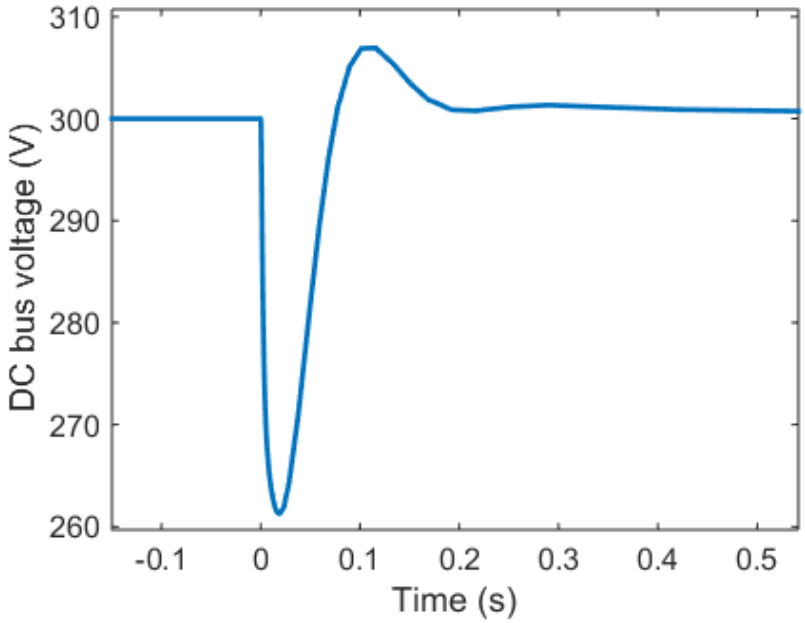

Figure V-8 Transients of dc bus voltage during fault with constant back EMF

5.2.4 Experimental verification

Because it is not possible for the power source to create a fault, the very large voltage drop emulates the fault without clearing it. In this case, the QV loop is rapidly saturated and the back EMF becomes a constant. If the fault is not cleared, the STATCOM will generate its maximum reactive power losing control of the PCC bus voltage while the Pf loop is free from saturation. Figure V-9 shows the transient of the dc bus voltage after the large voltage drop and the minimum value is about 261 V with the characteristics frequency equal to 5 Hz, which accords the calculation and the simulation.

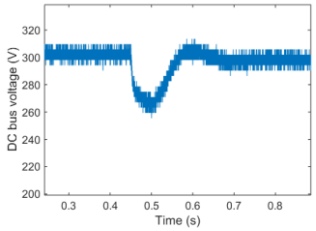

Figure V-9 Transients of dc bus voltage during large voltage drop

5.3 Effects of outer loops

In the previous section 5.2, discussions are made under assumptions that are valid at most time. This section shows some effects to strengthen the conclusions if the last two assumptions are not included. Detailed and accurate predictions can be made if more state space equations are added representing the outer loops, but here phasor analysis is still used for simplicity to give an intuitive understanding.

5.3.1 Effect of Pf loop

The effect from the input power command is usually small and negligible due to the long time constant. But under some extreme cases it could be the last straw that breaks the camel's back. Figure V-10 plots the phasor diagram again during the fault in which (a) is the same as Figure V-4(a) showing the time when the fault just happens.

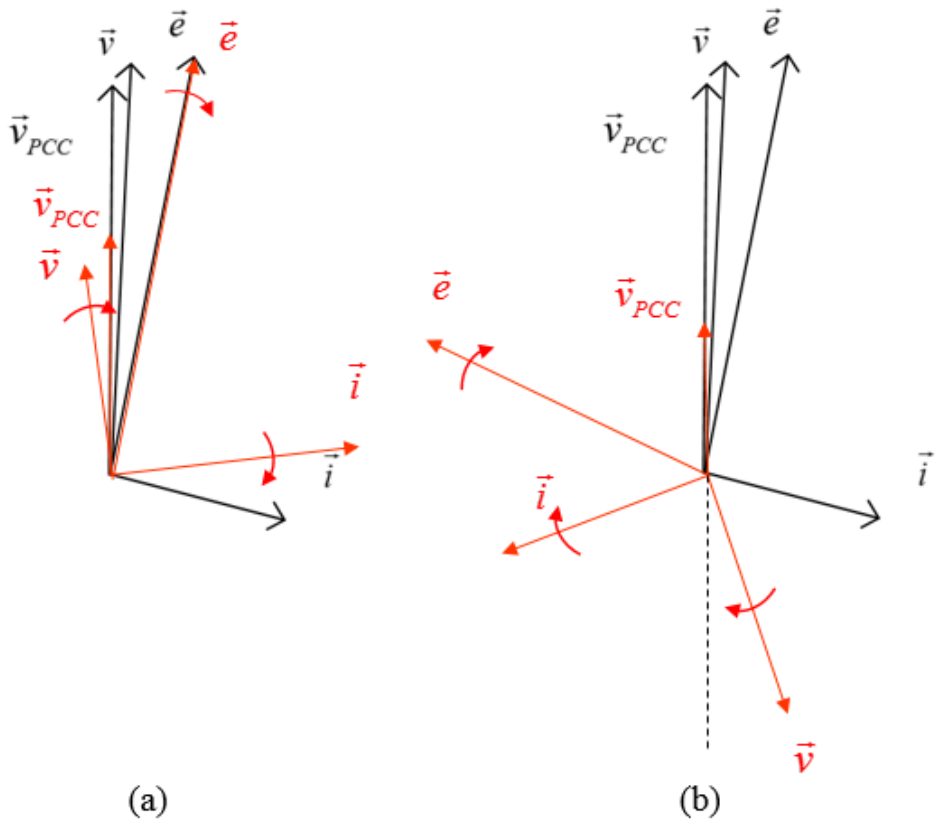

Figure V-10 Phasor diagrams of VSM-STATCOM during faults with Pf loop

As analyzed before, the dc bus voltage tends to decline. The Pf loop then tries to pull it back by turning the input power command to negative, which exerts additional power and accelerates the swinging in the marked direction. As such, the Pf loop is helping the situation. However, although it is unlikely to happen, if the virtual inertia and damping is too small, the phasors could be in the position as in Figure V-10(b) in red and cross the dashed line. Once crossing the dashed line, the active power will reverse its flow, from the STATCOM to the grid rather than the opposite direction, decreasing the dc bus voltage furthermore. It leads to a larger disturbance and worsens the situation.

5.3.2 Effect of QV loop

If the QV loop starts working, then the magnitude of the back EMF is no longer equal to the steady-state value before the fault. Because the QV loop is regulating the PCC bus voltage, its output – the magnitude of the back EMF will increase dramatically until hitting its limit as plotted in Figure V-11(b) while the case where the back EMF does not change shown in Figure V-11(a).

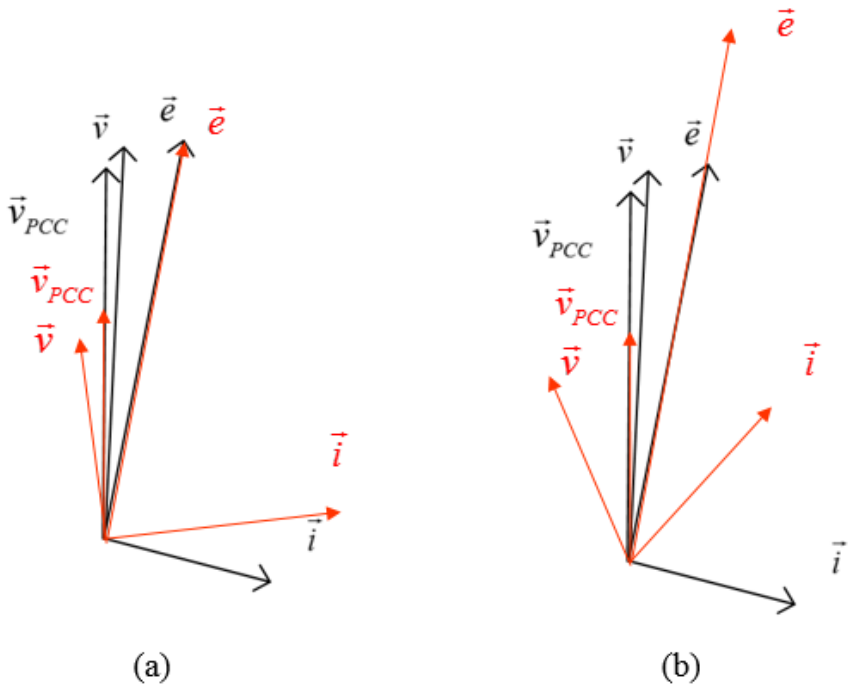

Figure V-11 Phasor diagrams of VSM-STATCOM during faults with QV loop

The compensating current rises as the magnitude of the back EMF and so as the active power involved making the dc bus voltage drop faster. The larger the back EMF is, the more active power the STATCOM outputs and the more energy it loses during the fault, illustrated in Figure V-12 with the virtual inertia M as another dimension, which is calculated with the help of (4) assuming the back EMF reaches the limit almost instantly. As observed, the transferred energy ΔW is monotonically increasing with either M or the magnitude of back EMF E, confirming the phasor analysis made previously. Therefore when M is at its minimum value, which is determined from the small signal stability margin in the previous chapter, ΔW is at the minimum with given limit of back EMF E shown in Figure V-13 as a vertical section of Figure V-12.

With given dc capacitor size, nominal dc bus voltage level, it is easy to calculate the maximum allowable transferred energy to ensure the operation of the converter, which has to be larger than the minimum transferred energy during any kinds of transients. To this end, in Figure V-12 a horizontal section at the maximum allowable transferred energy can be added, under which presents the feasible region of M and E. On the other hand, the maximum value of the back EMF should be as large as value corresponding to the rating of the STATCOM under normal conditions to make the full use of devices, which may shrink if it is outside the feasible region.

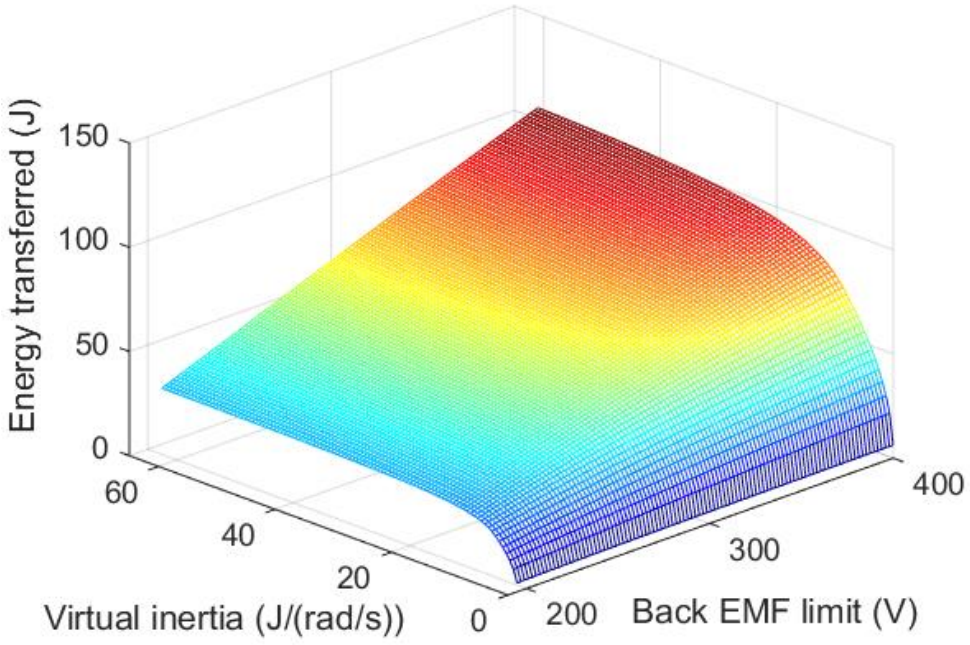

Figure V-12 Transferred energy as a function of virtual inertia and back EMF limit

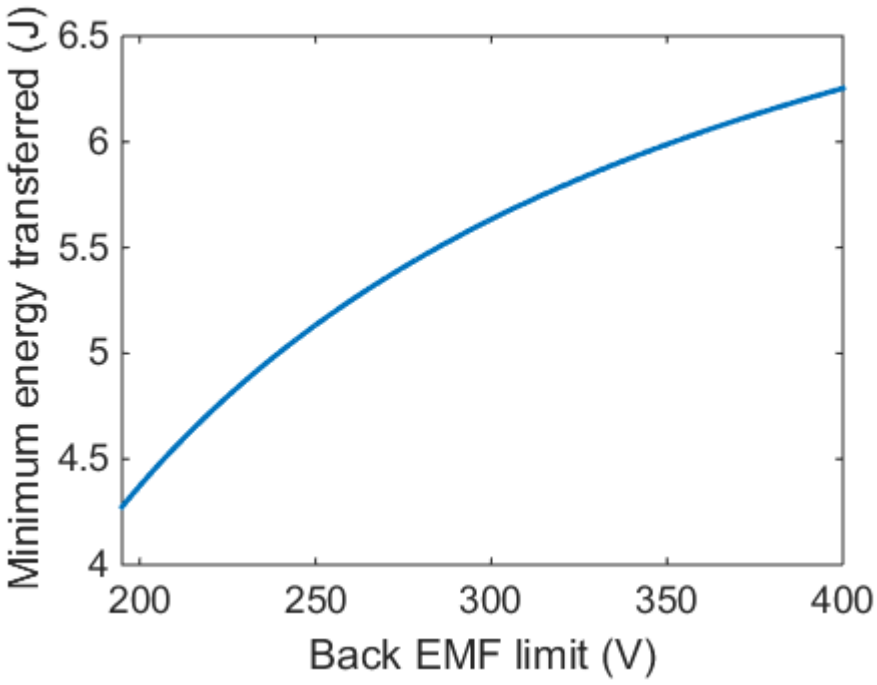

Figure V-13 Minimum transferred energy vs. back EMF limit

5.4 Possible solutions

The root of the issue of the dc bus voltage collapse is the use of active energy where the dc bus is only supported by a capacitor and the reserved active energy is limited. To address the possible issue of the dc bus voltage collapse, either the active power compensation should be limited or the total reserved energy should be increased. It leads to several possible solutions: change control parameters in (4), limit the magnitude of back EMF or increase the dc bus capacitor. The most important parameter in the controller is the virtual inertia, which influences the response speed of the power loop and thus the phase of all the phasors.

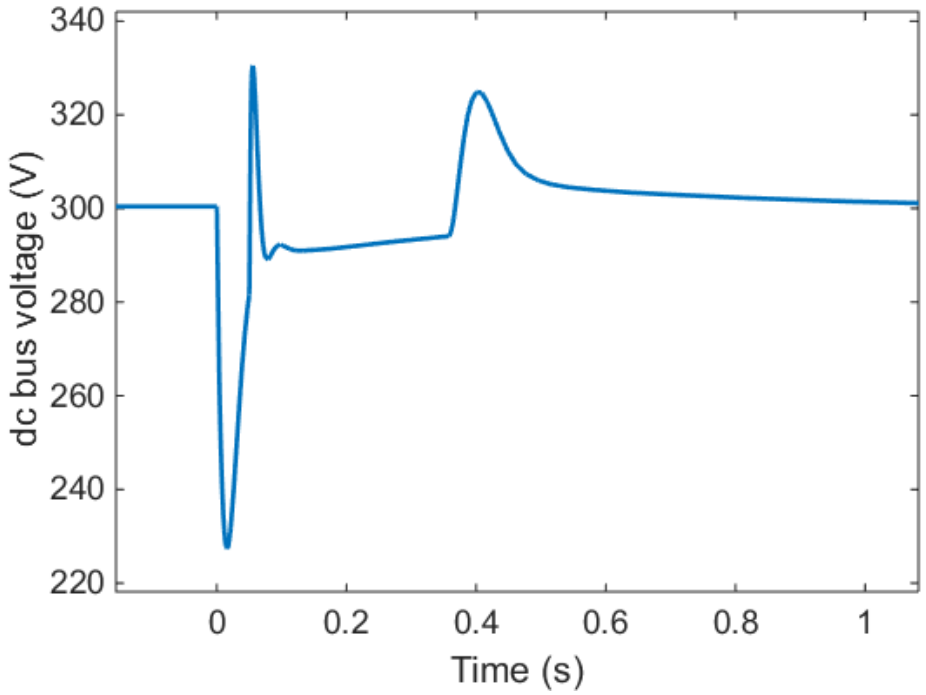

Figure V-14 Dynamics of dc bus voltage under fault with 1/5 virtual inertia

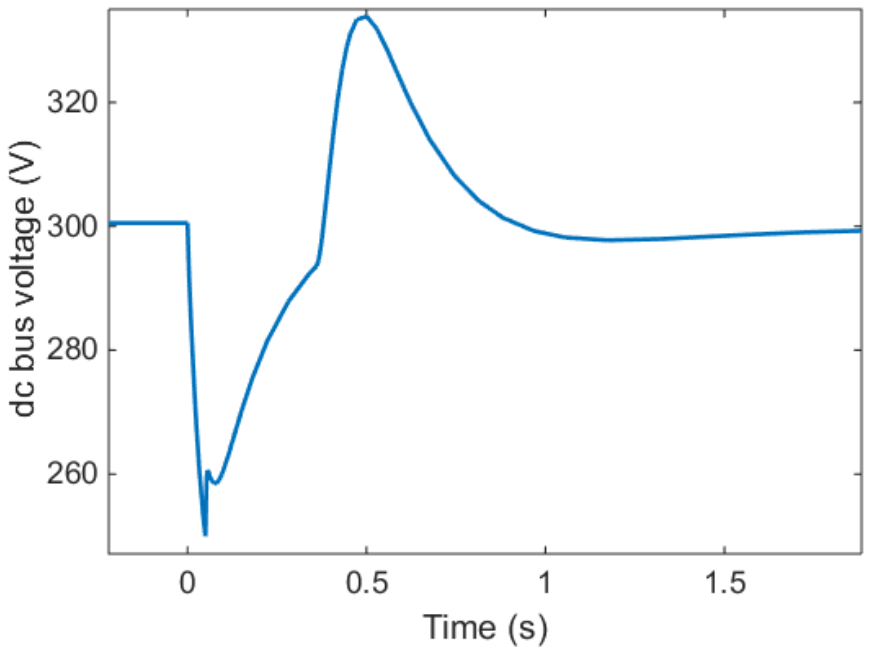

Figure V-15 Dynamics of dc bus voltage under fault with 5 times dc capacitor

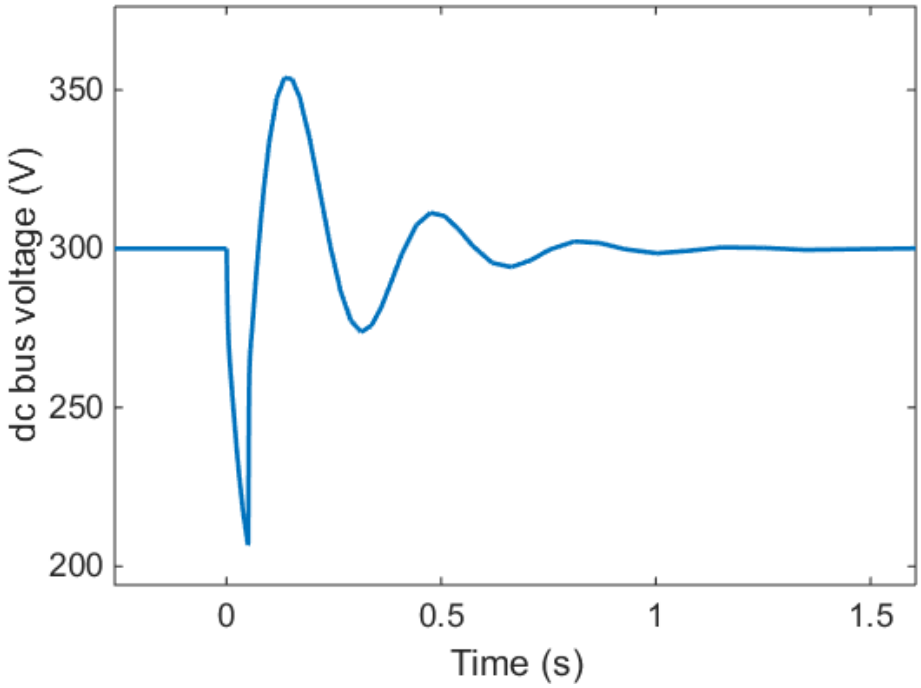

Figure V-16 Dynamics of dc bus voltage under fault with limiters on back EMF

Figure V-14, Figure V-15 and Figure V-16 show the simulation results with the above 3 solutions respectively. All the solutions successfully prevent the dc bus voltage from falling too low, with the method that increases the dc capacitor showing the least variation. It is anticipated

because it solves the problem fundamentally by enlarging the stored energy in the dc capacitor, but the cost is high and the capacitor cannot be changed online once implemented. Changing virtual inertia is easy to program but care must be taken to avoid going across the stability boundary. The addition of the limiter on the back EMF that helps clamp the active power compensation, which is also easy to implement in control codes, may reduce the steady-state operation region because the limit for the back EMF must be conservative to ensure the operation of the inverter, as referred in Figure V-12. However, a combination of the above solutions may provide advantages reducing their own drawbacks. In this way, the dc capacitor size can be smaller with a limiter on the back EMF, and some flexibility can be adjustable by tuning the virtual inertia online in order to go through faults without losing control of the STATCOM.

5.5 Final design guideline

Considering the issue during large transients, some design rules should be added to 4.3 which is only in a small signal sense.

The first thing is to check if the STATCOM can go through a given fault that is considered as the worst case. If not, find an acceptable set of parameters and redo the design process. The second thing is to set the proper limit for the back EMF when the design is finished using (3) if it is necessary to shrink the operating region. The design procedure is repeated and improved as follows:

Step 1, find the feasible region of M and E with given dc capacitor size and dc voltage value. Reduce the back EMF limit if necessary.

Step 2, tune the virtual inertia loop by changing M and D to get a desired bandwidth with enough phase margin.

Step 3 design the current compensators. This has little to do with the virtual inertia choice.

Step 4, select the R and L ratio for virtual impedance based on desired harmonic spectrum.

Step 5, choose the magnitude of the virtual impedance to grant enough damping for selected harmonic components.

Step 6, design compensators for the outer voltage loops.

Figure V-17 shows practical VSM control blocks where limiters are placed. The current limiters are for overcurrent protection considering the device rating and the duty cycle limiters are to prevent over-modulation.

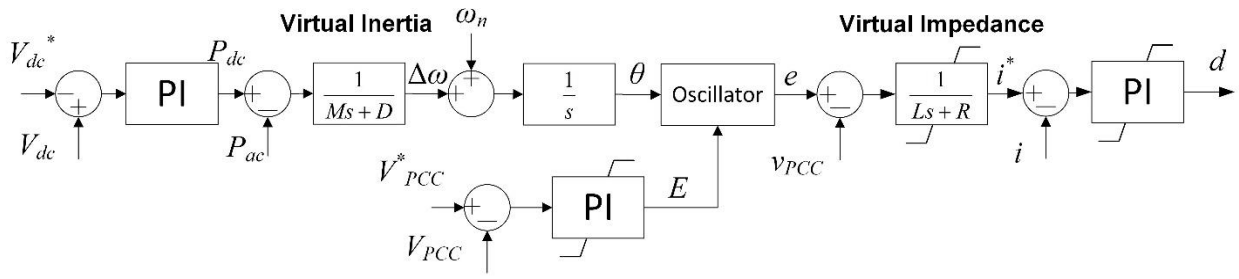

Figure V-17 Practical VSM control blocks for STATCOM

5.6 DC capacitor considerations

5.6.1 Relationship between virtual inertia and real inertia

As inferred previously, whether the STATCOM can go through a fault depends on not only the controller but also the size of the dc capacitor and the maximum allowable variation in the dc bus voltage. The size of the dc capacitor determines the stored energy and is the real inertia in the power stage. Equation (5) can be further derived into (5) where S is the apparent power of the converter and $\Delta\Omega$ is the frequency difference between two moments.

$$MS\Delta\Omega = \frac{1}{2}CV_{dc0}^2\left[\left(\frac{\Delta\bar{V}_{dc}}{\bar{V}_{dc0}}+1\right)^2-1\right] \qquad (5)$$

(6) is a general equation which applies to all converters equipped with the VSM control and links the virtual inertia and the real inertia. With given dc capacitor, nominal dc bus voltage and system frequency change, the more virtual inertia is designed to emulate, the more dc bus voltage variations is required, whose maximum value limits the maximum virtual inertia attainable in the VSM controller.

5.6.2 DC capacitor sizing

The first and the least requirement for the dc capacitor is that the ripple of the dc bus voltage should be limited. The shape and the spectrum of the output current is critical. For GTO-typed STATCOMs, limited to its switching frequency, the current loop bandwidth cannot be high enough

to ensure a sinusoidal waveform and therefore the dc capacitor should be selected carefully to avoid the resonance with the ac inductors [130, 131]. For a PWM-switched STATCOM, the ripple will be less [98, 132, 133] and under the three-phase balanced assumption, the minimum limit of the dc capacitor size is governed by (6) where m_a is the modulation index, I is the output peak current, ω is the line frequency and ΔV is the maximum ripple with those with a bar above being a per unit value without loss of generality.

$$\bar{C} = \frac{m_a \bar{I}}{2\omega \Delta \bar{V}_{dc}} \qquad (6)$$

Another requirement is the transient ride-through capability. A conservative design to absorb all the active power in the grid during the fault [134-136]. This functionality requires a much larger dc capacitor, as (7) where P is the demanded active power and t is the fault duration time.

$$\bar{C} = \frac{2\bar{P}t}{\bar{V}_{dc0}^2 \left[\left(\frac{\Delta \bar{V}_{dc}}{\bar{V}_{dc0}} + 1 \right)^2 - 1 \right]} \qquad (7)$$

However, the dc capacitor can be smaller when the energy during the transient can be calculated with the VSM controller implemented as (8) where W is the energy calculated with (3).

$$\bar{C} = \frac{2\Delta \bar{W}}{\bar{V}_{dc0}^2 \left[\left(\frac{\Delta \bar{V}_{dc}}{\bar{V}_{dc0}} + 1 \right)^2 - 1 \right]} \qquad (8)$$

If the space vector modulation is to be used, the dc bus voltage V_{dc} must be equal or larger than the ac line to line peak voltage and is better to be selected large enough to save room for modulation, typically 2 to 3 times. If choosing the PCC line to line rms value to be the voltage base and the output apparent power of the STATCOM to be the power base, a simple calculation example can be obtained by substituting into equations (6) ~ (8) with the dc capacitor value resulting in 0.0013 p.u., 0.069 p.u. and 0.006 p.u. respectively. As seen the dc capacitor can be largely reduced with more accurate estimation of the energy transferred during. But equation (8) only guarantees the ride-through capability of the STATCOM itself while reaching its maximum reactive power compensation without taking other units in the power system into consideration. It

is necessary to point out that in order to achieve other functionalities such as helping a wind farm ride through a fault [136], a larger dc capacitor and even energy storage system is expected.

5.7 Start-up process

Another practical consideration for VSM-STATCOM is the start-up process, which has not been mentioned in any references. Referring to synchronous condensers, there are typically two kinds of starting methods [137]. The first method is to connect a synchronous condenser to the grid via its transformer tapping down the voltage to speed up the torque, and then increase the secondary side voltage gradually to accelerate to the grid frequency. The second method is to use an additional motor to drive its torque to the grid frequency approximately, and then use a synchronizer to synchronize before closing the main circuit breaker.

With these ideas, there are also two corresponding method for a VSM-controlled STATCOM. The first one is to connect the converter to the grid and use the anti-parallel diodes of switching devices to charge the dc capacitor while in the meantime the controller begins to synchronize. When the dc bus voltage is stable and the synchronization completes, the converter starts switching with current loop and Pf loop running to charge the dc capacitor further to the nominal value before starting QV loop to compensate. The second one is to use a separate dc source to charge the dc bus voltage to the nominal value through a pre-charging circuit without connection to the grid and mimic a synchronizer to synchronize. After the dc bus is charged and synchronization is finished, a main circuit breaker is closed and all the loops except the QV loop start working to ensure smooth connection. Finally the QV loop is turned on to begin compensation.

Comparing these two method for a VSM-STATCOM, the first one is preferable because it is easier to implement without addition of an extra dc power source and potential danger due to failure mimicking synchronizer.

In all, the detailed start-up process is summarized in Table V-1. In the first step, a small trick is that before connection the feedback of the power loop should be an imaginary output power because there is no current flowing. The initial value of the back EMF is set to be the magnitude of the PCC bus voltage to ensure zero reactive compensation during the second step, which is not mandatory but is generic for all operation conditions.

Table V-1 Start-up procedure for VSM-STATCOM

	Controller	Hardware	Notes
Step 1	Start power loop with virtual impedance	DC capacitor charged by anti-parallel diodes	Imaginary output power used P_{dc}=0 E=V_{PCC}
If dc voltage charging completes && synchronization completes			
Step 2	Start current loop Start Pf loop	Bypass pre-charging resistor Start switching to charge	Actual output power used E=V_{PCC}
If dc voltage charging completes			
Step 3	Start QV loop		Reactive compensation begins

The start-up process is shown in Figure V-18 where the purple is the dc bus voltage and the green is the output current. The first event is step 2 when the controller starts and the dc bus voltage is charged up to the nominal value. It requires the phase of the back EMF swings according to the command from the dc side to charge and thus the output current oscillates with it. When the program detects that the dc voltage stops oscillating, the controller reaches its steady-state and begins to compensate, which is the second event in the figure. On the other hand, the start-up process of the D-Q controller is shown in Figure V-19 as a contrast. While charging the dc bus voltage, the PLL is still tracking the PCC bus voltage and there is no phase shift. The output current then seems smoother than that in the VSM controller.

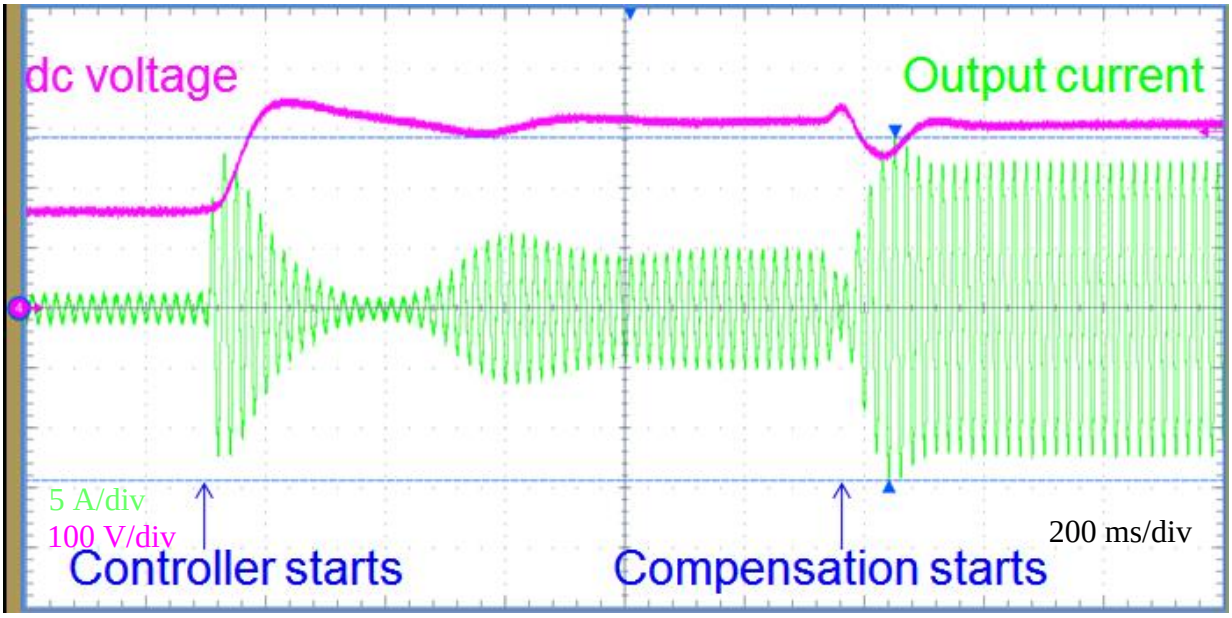

Figure V-18 Start-up process of VSM-STATCOM

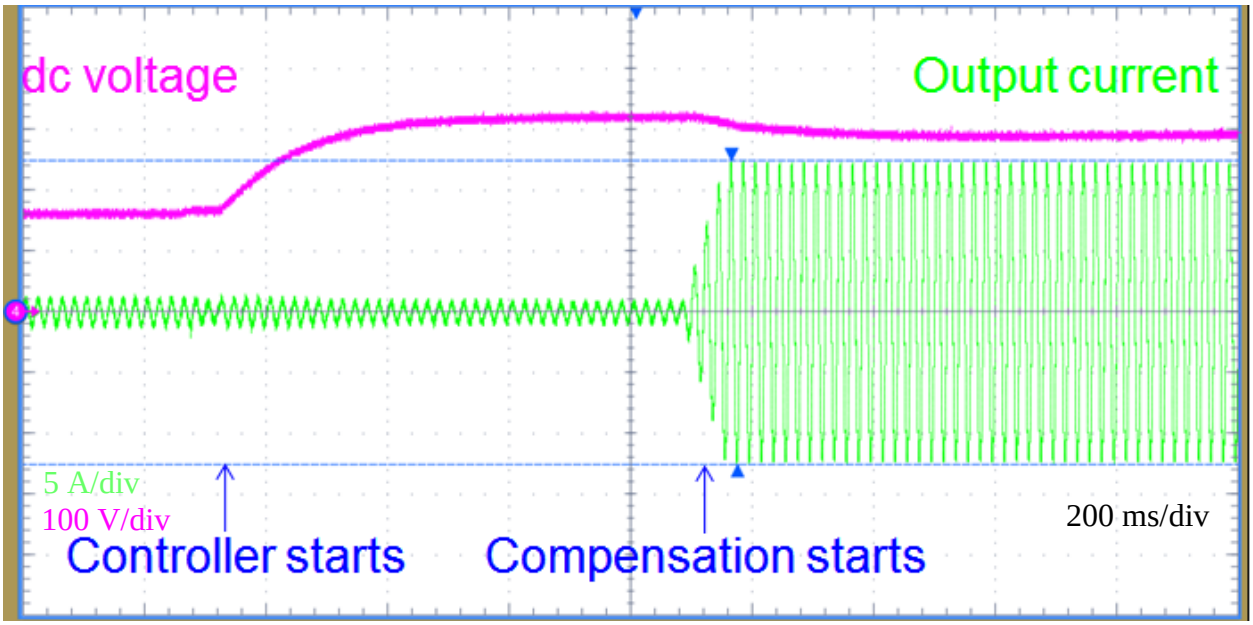

Figure V-19 Start-up process of DQ-STATCOM

5.8 Summary

In this chapter, the first contribution is to analyze a potential problem in VSM-STATCOMs brought by the control scheme, which renders the inherent trend to use the stored active energy in transients. This issue is modeled and some possible solutions are suggested to complete the VSM

controller design in a large signal sense. Moreover, the start-up procedure is proposed for the implementation of hardware.

Chapter VI. CONCLUSIONS AND FUTURE WORK

The recently proposed virtual synchronous machine concept is extended to STATCOM applications and shows greater voltage regulation performance when there is frequency fluctuation in the power grid. To this end, analysis of the VSM controller is given in two D-Q frames, namely the system D-Q frame and the controller D-Q frame. By studying the transfer functions of each loops and the impacts from every virtual parameters, a design guideline is proposed to utilize the VSM controller. When there is only voltage variation, the VSM controller shows similar performance as the D-Q controller while the VSM-STATCOM can adjust its phase and compensates more properly if frequency changes due to the inherent property of swinging. The conclusion is also partly verified experimentally.

However, the nature to use its active power during transients could make a VSM-STATCOM collapse because of possibly large changes in the dc bus voltage. To analyze the phenomenon, state space equations based on large signals are derived and proven to match the simulation results, which can help determine the active power flow during transients. Possible solutions are provided to address this issue successfully to avoid the limit of the VSM controller. Also the start-up process is discussed to facilitate the realization of practical implementation.

As for future work, first it is optimal to give a quantitative design procedure with respect to known system parameters and corresponding sensitivities in order to have a robust controller which can stand through different system operation points. Also the control structure is not proven to be the best yet and some improvements can be achieved by further investigation into the mathematical derivation of the equivalency between the VSM concept and synchronous generators where only the preferable part is utilized.

Furthermore, a VSM-STATCOM can be more effective during transients should there be any reserved energy like battery storage systems to support the PCC bus voltage, no matter during frequency fluctuations or faults. The additional control over the reserved energy should be addressed too. More experiments can be conducted if there are more units in the grid to see the impacts and interferences of the VSM controller and the others. Moreover, the analysis and the design methodology can be applied to other grid-interfaced converters for a better friendliness to the power grid.

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