Resistive Switching Behavior in Low-K Dielectric Compatible with CMOS Back End Process

Ye Fan

Thesis submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Mariusz Kriysztof Orlowski, Chair
Jean Joseph Heremans
Guo Quan Lu

October 18, 2016
Blacksburg, VA

Keywords: resistive switch, non-volatile memory, conductive filament, interconnect, low-k, TDDB

Resistive Switching Behavior in Low-K Dielectric Compatible with CMOS Back End Process

Ye Fan

Abstract

In an effort to lower interconnect time delays and power dissipation in highly integrated logic and memory nanoelectronic products, numerous changes in the materials and processes utilized to fabricate the interconnect have been made in the past decade. Chief among these changes has been the replacement of aluminum (Al) by copper (Cu) as the interconnect metal and the replacement of silicon dioxide (SiO_2) by so called low dielectric constant (low-k) materials as the insulating interlayer dielectric (ILD). Cu/low-k structure significantly decreases the RC delay compared with the traditional interconnect (Al/SiO_2). Therefore, the implementation of low-k dielectric in Cu interconnect structures has become one of the key subjects in the microelectronics industry. Incorporation of pores into the existing low-k dielectric is a favorable approach to achieve ultra low-k ILD materials.

To bring memory and logic closer together is an effective approach to remove the latency constraints in metal interconnects. The resistive random access memories (RRAM) technology can be integrated into a complementary metal-oxide-semiconductor (CMOS) metal interconnect structure using standard processes employed in back-end-of-line (BEOL) interconnect fabrication. Based on this premise, the study of this thesis aims at assessing a possible co-integration of resistive switching (RS) cells with current BEOL technology. In particular, the issue is whether RS can be realized with porous dielectrics, and if so, what is the electrical characterization of porous low-k/Cu interconnect-RS devices with varying percentages of porosity, and the diffusive and drift transport mechanism of Cu across the porous dielectric under high electric fields.

This work addresses following three areas:

1. Suitability of porous dielectrics for resistive switching memory cells. The porous dielectrics of various porosity levels have been supplied for this work by Intel Inc. In course of the study, it has been found that Cu diffusion and Cu^+ ion drift in porous materials can be significantly different from the corresponding properties in non-porous materials with the same material matrix.

2. Suitability of ruthenium as an inert electrode in resistive switching memory cells. Current state-of-the-art thin Cobalt (Co)/Tantalum Nitride (TaN) bilayer liner with physical vapor deposited (PVD) Cu-seed layer has been implemented for BEOL

Cu/low-k interconnects. TaN is used for the barrier and Co is used to form the liner as well as promoting continuity for the Cu seed. Also, the feasibility of depositing thin CVD ruthenium (Ru) liners in BEOL metallization schemes has been evaluated. For this study, Ru is used as a liner instead of Ta or Co in BEOL interconnects to demonstrate whether it can be a potential candidate for replacing PVD-based TaN/Ta(Co)/Cu low-k technology. In this context, it is of interest to investigate how Ru would perform in well-characterized RS cell, like Cu/TaO_x/Ru, given the fact that Cu/TaO_x/Pt device have been proven to be good CBRAM device due to its excellent unipolar and bipolar switching characteristics, device performance, retention, reliability. If Cu/TaO_x/Ru device displays satisfactory resistive switching behavior, Cu/porous low-k dielectric/Ru structure could be an excellent candidate as resistive switching memory above the logic circuits in the CMOS back-end.

3. Potential of so-called covalent dielectric materials for BEOL deployment and possibly as dielectric layer in the resistive switching cells. The BEOL reliability is tied to time dependent failure that occurs inside dielectric between metal lines. Assessing the suitability of covalent dielectrics for back-end metallization is therefore an interesting topic. TDDB measurements have been performed on pure covalent materials, low-k dielectric MIM and MI-semiconductor (MIS) devices supplied by Intel Inc.

Resistive Switching Behavior in Low-K Dielectric Compatible with CMOS Back End Process

Ye Fan

General Audience Abstract

While the scaling of conventional memories based on floating gate MOSFETs is getting increasingly difficult, novel types of non-volatile memories, such as resistive-switching memories, have recently been of interest to both industry and academia. Resistive switching memory is being considered for next-generation non-volatile memory due to relatively high switching speed, high scalability, low power consumption, good retention and simple structure. Additionally, these two-terminal devices operate by changing resistance from high resistance OFF-state (HRS) to low resistance ON-state (LRS) in response to applied voltage or current due to the formation and rupture of a conductive filament. In particular, Conductive Bridging Random Access Memory (CBRAM), also referred as Programmable Metallization Cell (PMC), is a promising candidate for a resistive memory device due to its highly scalable and low-cost technology. Currently, the interconnect RC scaling methods have reached their limits and there is an urgent need for alternative ways to reduce or remove the latency constraints in CMOS low-k/Cu interconnect. One method is building CBRAM directly into a low-k/Cu interconnects to reduce the latency in connectivity constrained computational devices and the chip's footprint by stacking memory on top of logic circuits. This is possible since the Cu metal lines and low-k/Cu interconnect already prefigure a potential RS device.

This work addresses three areas: Firstly, the suitability of porous dielectrics for resistive switching memory cells. Secondly, the suitability of ruthenium as an inert electrode in resistive switching memory cells. If Ru resistive memory device displays satisfactory resistive switching behavior, Cu/porous low-k dielectric/Ru structure could be an excellent candidate as resistive switching memory above the logic circuits in the CMOS back-end-of-line (BEOL). Thirdly, the potential of so-called covalent dielectric materials for BEOL deployment and possibly as dielectric layer in the resistive switching cells.

Acknowledgement

None of my works would not be possible without encourage, help, support and contribution of some people. I would like to start by expressing my thanks to those who somehow contributed to this thesis directly or through emotional support.

First and the foremost, I would like to express my deepest gratitude to my advisor Dr. Marius Orlowski for his great guidelines, encouragement, advice and support proposed with an utmost kindness from the beginning of my research. I am more than grateful to him for his trust in my skills and for the outstanding opportunities to do research he provided me. He is not only a supervisor to show how to systematically carry on scientific research, but also show how to be a foreseeing and visionary person. I am enormously thankful to him to give me an opportunity to pursue my master study with him and the financial support helping me focus greatly on my work. I also acknowledge my committee members for their time and suggestions.

I am thankful to Dr. Sean King and Intel Inc. for having provided me the opportunity to delve into a new field of study. I appreciate his suggestions and valuable advices to make our Capstone project work better.

I would like to acknowledge my colleague Rizwan Ali and teaching assistants Mohammad Al-Mamun and Ben Colon for guiding and helping me extensively during my research with their valuable suggestions and ideas. I am also thankful to my colleague Anshuman Verma for his guidance and help with device characterization and instrument operation at the first stages of my research.

I also give my thanks to Dr. Gino Manzo for teaching and guiding me during my two semesters Senior Design Project. From him I learned how to effectively communicate and cooperate in a research group, and many useful presentation skills.

Special thank you to Don Leber, manager of Micron Lab, Virginia Tech for helping me troubleshoot some of the most difficult processing steps of fabrication. Thanks for helping me looking for some tools and materials used in my experiments.

Last but not least, I would like to express my deepest love to my family members: my father, mother and brother. They have shown me unconditional and unbounded love, and they always encourage me to pursue my dream. Their support is the strongest driving force for me to go forward.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

This chapter starts with an introduction to the interconnect wires serving as an essential function in connecting the individual devices and carrying electrical signals in the integrated circuit. The challenge of lowering the interconnect time delays and power dissipation brought by the aggressive transistor scaling are discussed. After examining the surveyed results from literature, the low-k interlayer dielectric materials are reviewed. The resistive switching mechanism is addressed for a typical metal/insulator/metal structures. Studying on the electric characterization of porous low-k/Cu MIM devices is the motivation to this thesis.

1.1 MIM Devices and Interconnects

In the Integrated Circuits (IC's), interconnect means ideally a metal line of low resistivity (high conductivity) which connects the various electronic devices to carry current or to transport charge [1-2]. The interconnect wires not only transmit electrical signals but also distribute clock signals which control the timing and synchronize the operation [3]. The backend metallization includes the metal wires and the interlayer dielectrics (ILD). The interconnecting metal lines provide contact to each individual devices (e.g. transistor, resistor, and capacitor) on the silicon substrate. ILD can isolate and mechanically support the wires. There can be more than 10 layers of metal/dielectric/metal (MIM) in the interconnect structure.

Since the development of the ICs in 1960, aluminum (Al), Copper (Cu) or alloy (Al+Cu) have become the primary metal material for the interconnecting lines, and silicon dioxide (SiO_2) has been used as the insulating layer (dielectric material) to isolate the interconnecting lines and signals, and prevent an electronic short. SiO_2 has also been used as a gate material in the metal oxide semiconductor (MOS) devices. Al or Cu connects the gate of each device by interconnecting lines. The cross section of a typical interconnect structure is shown in Fig. 1.1 [4]. The upper layers are two interconnect metal lines and the transistors are at the bottom of the chip, separated by the interlayer dielectric (ILD). In 1997, IBM first introduced copper metallization in CMOS. The

announcements accelerated industry-wide commitment to switch to copper interconnects. Fig 1.2 (a) and Fig 1.2 (b) show two scanning electron microphotograph (SEM) images of interconnect architectures fabricated by IBM and MOTOROLA separately [5-6]. The interconnect lines firstly incorporate copper with oxide, and then introduce low-k dielectrics.

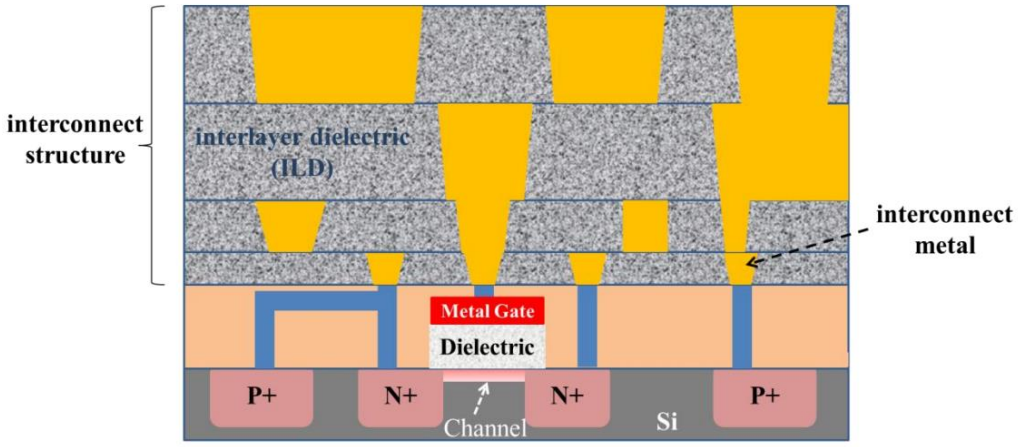
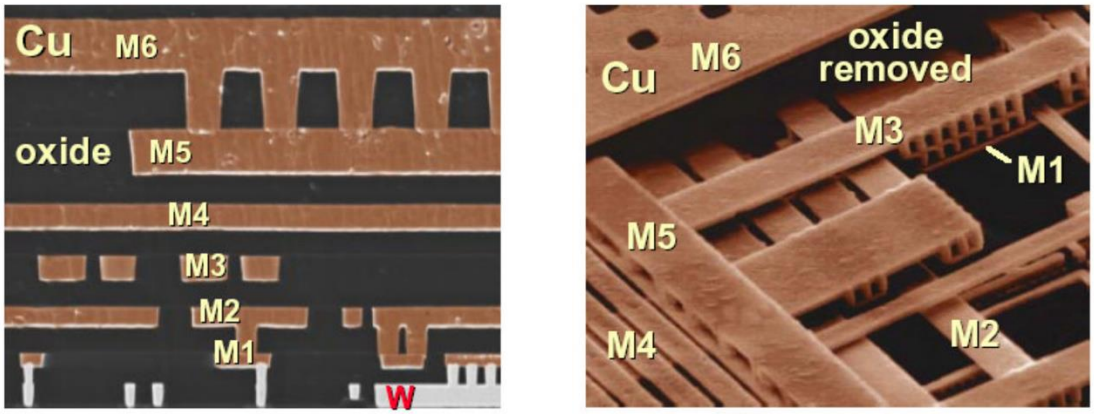


Figure 1.1 A cross-section schematic of an IC chip.



(a) (b)

Figure 1.2 Scanning electron microscopy (SEM) images of interconnect architecture (a) with Cu wire, Cu via, and ILD; (b) without ILD.

The structure of multilevel interconnect is often described in two parts: “local” and “global”, as is shown in Fig. 1.3 [7]. The local interconnect includes the first layer of the interconnecting line and the metal contact which connects the actives parts of the transistors. Commonly the local

wires are made by tungsten metal. The global interconnecting wires consists of multiple Al or Cu lines and vias, and insulating ILDs. The global and intermediate interconnects are two types of Backend-of-the-line (BEOL) [8]. Intermediate wires provide the lower-level connections and global wires connect the intermediate layers. Under the Moore's law, the traditional chip scaling is slowing down [9]. However, the BEOL scaling is the most problematic part of holding up the scaling train.

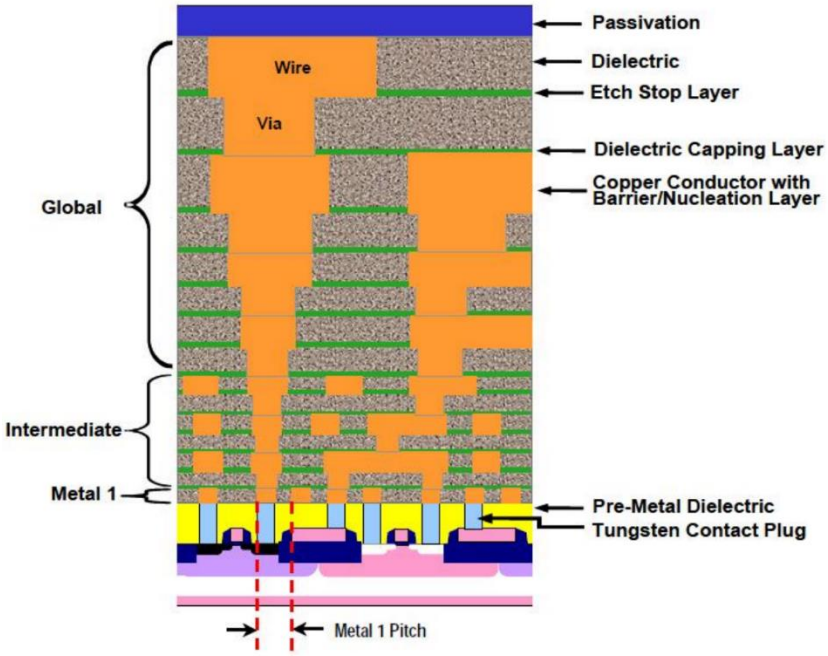


Figure 1.3 Cross-section of a multilevel interconnect structure.

1.2 Interconnect RC Delay

As the device scaling affect become significantly aggressive, the IC delay draws more and more attention [10-11]. Basically, the total IC delay is composed of two parts: (1) the intrinsic device delay, also known as the device gate delay, and (2) the interconnection delay, also called RC delay, where R is the metal wire resistance and C is ILD capacitance. The RC delay is the signal propagation time between transistors.

The complicated interconnect structure in Fig. 1.3 can actually be seen as numerous repetitions of a simple MIM capacitor, which is shown is Fig. 1.4. The interconnect metal line has a resistance (R) which is proportional to ρ/A, where ρ is the resistivity of the metal and A is the cross-sectional area of the interconnect wire. The capacitance of this MIM capacitor is equal to $k\varepsilon_o/d$, where k is the dielectric constant of the ILD material, ε_o is the permittivity of free space, and d is the dielectric thickness.

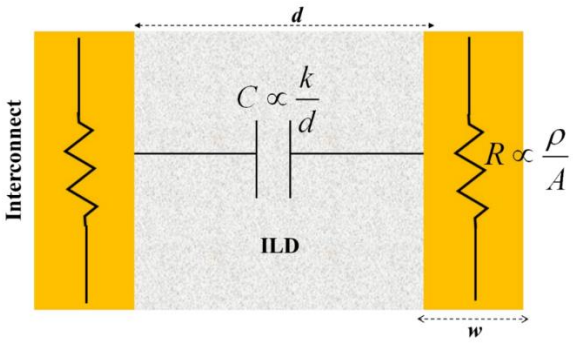


Figure 1.4 Schematic of a MIM capacitor model representing the interconnect structure.

Mathematically, the interconnect delay can also be approximately expressed as following expression with *R* and *C* [12].

$$RC = \frac{\rho}{w}\frac{L^2 k\varepsilon_o}{d} \tag{1.1}$$

The silicon ICs are developing towards smaller device dimensions, higher speeds, and higher devices densities. In order to increase the switching speed of the MOSFET devices, the physical size of devices has been continuously decreased (Moore's Law), and especially the gate length of the transistor has been dramatically decreased in the past decades and is currently at 14 nm in CMOS production [13]. According, the interconnection wires have become smaller and longer and the dielectric space has become narrower. In another words, the scaling of devices will cause the reduction of the size of the interconnect metallization (w) and insulation (d), which will result in larger interconnect resistance (R) and interconnect capacitance (C). Consequently, the interconnect

RC delay, signal cross-talk, and power dissipation will exacerbate and even will become the major factors that are limiting the device operation speed.

According to the Equation 1.1, based on the perspective of material property, the effective approaches to reduce the RC delay are increasing the interconnect metal conductivity and lower the dielectric constant of ILD.

Since 1997, copper replaced aluminum as the interconnect metal because copper has lower resistivity (bulk = 1.6 μΩ·cm) than aluminum (bulk = 2.6 μΩ·cm). In Fig. 1.5, the interconnect delay in copper wires with low-k ILD and aluminum wires with SiO_2 ILD are compared. From Fig. 1.5, it can be seen that Cu/low-k structure significantly decreases the RC delay compared with the traditional interconnect (Al/SiO_2). Therefore, the implementation of low-k dielectric in Cu interconnect structures has become one of the key subjects in the microelectronics industry [14].

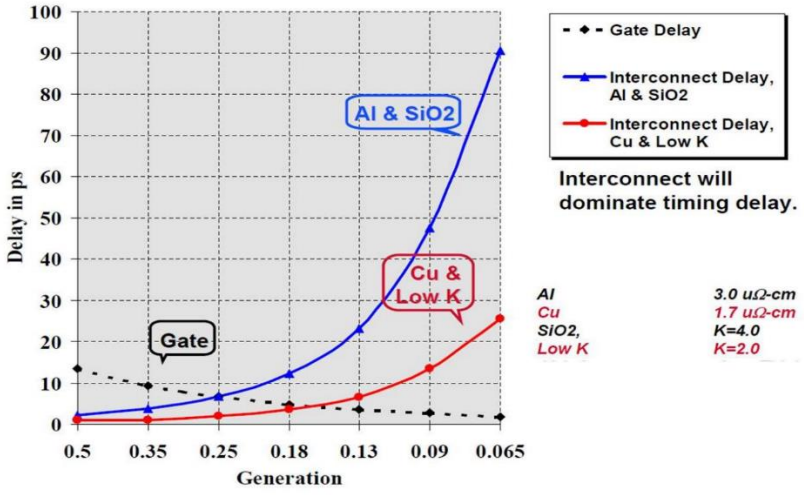


Figure 1.5 RC delay in Al/SiO_2 and Cu/low-k interconnects.

1.3 Low Dielectric constant (Low-k) Materials

Generally, low-k dielectrics are defined as the material with a dielectric constant less than 3.9 which is the value of the silicon dioxide dielectric constant. Therefore, it is important and significant to continually develop the dielectric materials with lower dielectric constant than

silicon dioxide, the standard dielectric material used for interconnect, to reduce the interconnect RC delay further.

According to the Clausius-Mossotti-Debye equation 1.2 [15], the reduction in dielectric constant of ILD can be achieved by incorporating the atoms and bonds which have a lower polarizability, or decreasing the density of the dielectric material.

$$\frac{k-1}{k+2} = \frac{N}{3\varepsilon_o}\left(\alpha_e + \alpha_i + \frac{\mu^2}{3kT}\right) \tag{1.2}$$

where N is the density of the material. α_e is the electronic polarization. α_i is the ionic polarization. $\frac{\mu^2}{3kT}$ describes the dipolar polarization, where μ is the orientation polarizability, k is the Boltzmann constant and T is the temperature.

Based on the equation, among all the possible approaches for decreasing the dielectric constant of ILD, the most effective approach is to reduce the volume density because the reduction of density indicates the decrease of the total number of electronic and ionic dipoles per unit volume. The density can be reduced by using lighter atoms such as C and H atoms and/or by introducing more free space around the atoms [16]. Accordingly, incorporation of pores into the existing low-k dielectric is a favorable approach to increase the free space and decrease the ILD density.

There are two methods for adding pores into existing low-k materials: subtractive and constitutive method [17-18]. In the subtractive method, a skeleton precursor mixed with an organic precursor (which is called porogen) is introduced by using the PECVD. During curing of the dielectric, the organic precursor burns out from the dielectrics, leaving nano-size pores [19]. The constitutive method for fabricating low-k materials is the porogenless structural approach. The porosity in the dielectric can be obtained by using particular precursors that contain molecular pores when the film cross-links during annealing, leaving behind pores [20-24]. The description of lowering dielectric constant is shown in Fig. 1.6.

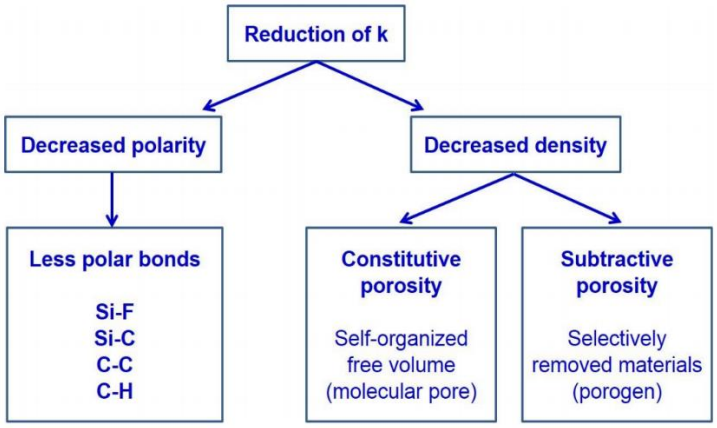


Figure 1.6 Description of lowering dielectric constant.

As described in Fig. 1.7, from 90 nm technology node, SiCOH materials have been mainly studied and used for interlayer dielectrics [25]. The SiCOH material is formed by introducing carbon molecular bonds (mainly through CH_3 groups) into a silica matrix, which reduces both the total polarizability as well as the density of the material. The SiCOH materials, therefore, is also called carbon-doped oxide (CDO) or organosilicate glass (OSG).

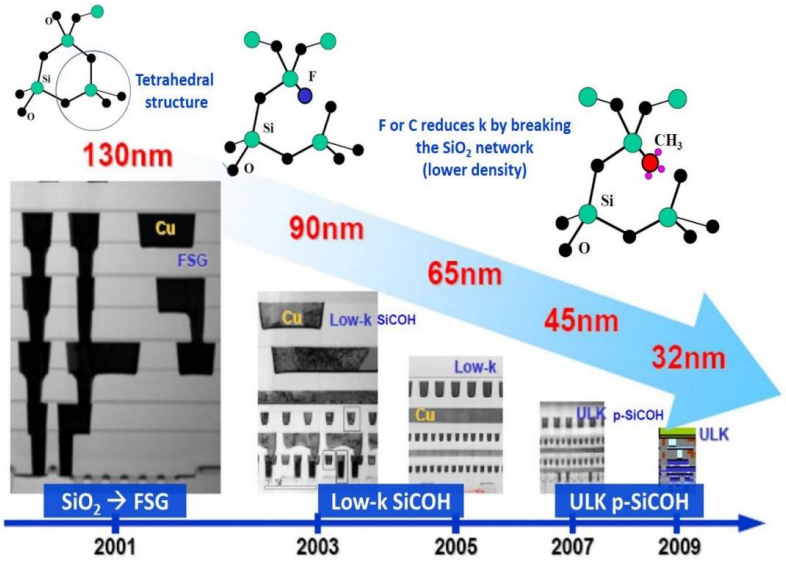


Figure 1.7 Trend of interlayer dielectric materials.

The implementation of SiCOH materials can reduce the effective k value from 3.9 for SiO_2 to 2.5 [26]. To achieve lower k value, the density of the material needs to be further reduced by

introducing porosity in the low-k material. With the introduction of porosity, the porous SiCOH materials can have a k value lower than 2.5. The low-k dielectric material used in this thesis is porous SiCOH and SiCH material provided by INTEL Corporation.

1.4 Basics on Resistive Memory

Implementation of low-k materials with substantially lower k values has stalled due to the high levels of interconnected nanoporosity that these materials contain which creates a myriad of problems for their implementation [27-30]. In addition, metal resistances for technologies smaller than the 32 nm node are now growing exponentially due to dimensional scaling leading to increased boundary and interfacial scattering effects [31] and limitations in scaling the thickness of the high resistivity Ta/TaN adhesion diffusion barrier layer relative to Cu [32]. Thus, current interconnect RC scaling methods have reached their limits and there is an imminent need for alternative ways to reduce or remove latency constraints in metal interconnects. One method for removing latency constraints in highly constrained computing is to bring memory and logic closer together [33]. Numerous alternative memory technologies are now being explored that have the potential to be co-integrated into a complementary metal-oxide-semiconductor (CMOS) metal interconnect structure [34-35]. However, from a cost perspective and ability to rapidly adopt and implement, a memory technology that can be fabricated using standard materials and processes already employed in BEOL interconnect fabrication would be the most attractive.

Resistive random access memories (RRAM) based on a resistive switching (RS) mechanism [36-38] offers the potential for co-integration and fabrication using exclusively native materials to a standard BEOL interconnect [39-40]. RRAM is a simple two terminal metal-insulator-metal device that is essentially the same as a CMOS metal interconnect system with metal vias being replaced by conductive RS cells [41-42]. It is also due to the synergy of materials used to make RS devices where the electrolyte/insulator is sandwiched in many cases between active (Cu) and inert (Ta, Ti, TiN, W) electrodes commonly utilized BEOL interconnects for various purposes [43-44].

In this section, the fundamentals of Resistive Memory and the switching mechanism of memory devices based on solid electrolytes will be reviewed, followed by introducing some basic concept and terminologies about RRAM. The modes of operation and operation of Conductive Bridge RAM (CBRAM) will be studied.

1.4.1 Fundamentals of Resistive Memory

Non-volatile memory technology plays a very significant role in the market of electronics products. It is widely used in mobile phone, digital camera, portal storage devices and so on. Until now, flash memory dominates the market of non-volatile memories, whose share of the market is above 90%. Several non-volatile memories based on different concepts have aroused extensive attention from both of industry field and academic field, such as Magnetoresistive RAM (MRAM), Phase change RAM (PRAM) and Resistive RAM (RRAM). Compared with other types, RRAM shows relatively high switching speed, high scalability, low power consumption, good retention and simple structure [45]. The device structure of RRAM is thin film stacks consist of a metal anode, an insulator, and a metal cathode which form an electrochemical cell. CBRAM is one type of RRAM, whose two metal electrodes are made of different materials. Its basic structure is given in Fig. 1.8. The active metal can be any oxidizing metal like Cu or Ag which has a moderate ionization energy, thus yielding ions readily. The solid electrolyte layer allows for relatively high mobility of metal ions. SiO_2, Ta_2O_5, TaO_x, $SrTiO_3$, AgGeSe, GeS, TaSiO, HfO_2 are available materials for the solid electrolyte. The inert metal material is usually Pt, Ir or W, characterized by efficient stopping barriers of Cu and Ag cations. Thus, the operation of resistive memory relies on ions and this type of device is also called nano-ionic device.

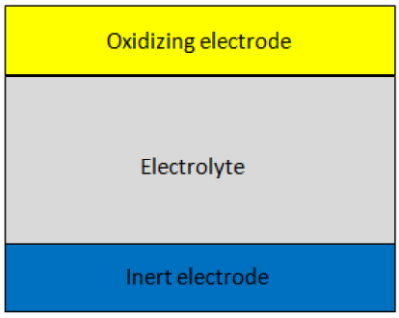


Figure 1.8 Stack structure of a CBRAM.

Resistive switching memories are typically two-terminal non-volatile electrical devices operated by switching between two resistance states. Device operates by applying voltage biases/pulses which induce a resistance change in the material. There are two states: high resistance state (HRS) /OFF state and low resistance state (LRS) /ON state. HRS and the LRS can be represented as logic values of 1 and 0, respectively. In the low resistance state, the corresponding device resistance is R_{on}. It can be controlled by an external selection of the imposed compliance current I_{cc}. The transition from the HRS to the LRS is called the SET process, while the transition from the LRS to the HRS is called the RESET process. In both SET and RESET processes, there are threshold voltages to toggle the resistance state, which are called SET voltage (V_{set}) and RESET voltage (V_{reset}). Fig. 1.9 describes the current flowing through an CBRAM device during the formation, the RESET and the SET operation. Formation is a specific SET operation performed on a fresh (i.e. yet untested device).

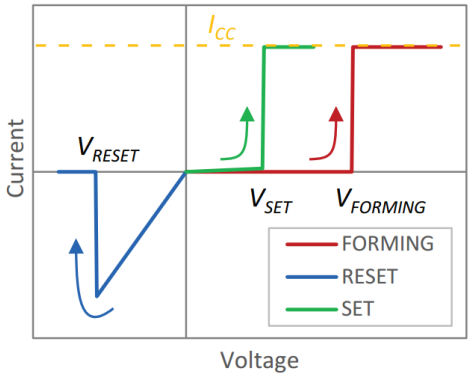


Figure 1.9 I-V curve of the different operations: FORMING, SET and RESET.

In CBRAM, a device in its HRS can be SET to LRS by applying V_{set}, while during RESET LRS is set back to HRS by applying an appropriate V_{reset}. Fig. 1.10 shows the schematic of the switching process in an CBRAM devices with an oxidizable Cu electrode and an inert Pt electrode. Under application of a positive bias to the Cu electrode, Cu ions are ionized at the Cu electrode interface with the dielectric and migrate through the solid electrolyte. These ions accumulate at the inert electrode because of its stopping power. The accumulated ions nucleate and grow to form a nanoscale metallic conductive filament (CF) connecting both electrodes. The initially highly resistive cell switches to LRS due to a short circuit between top and bottom electrode. Under reverse bias the filament is dissolved mainly by Joule's heating and partly by electrochemical ionization of Cu constituting the filament and the cell is switched back to the HRS.

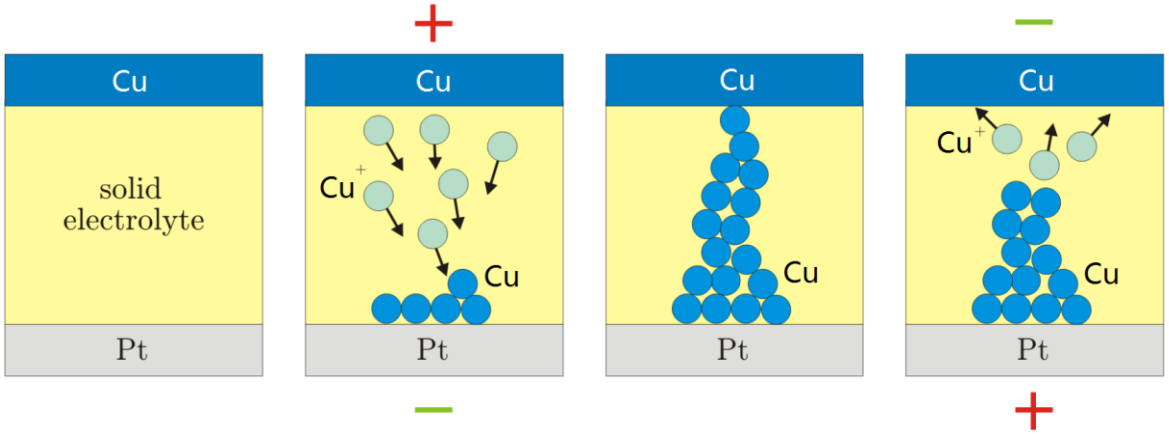
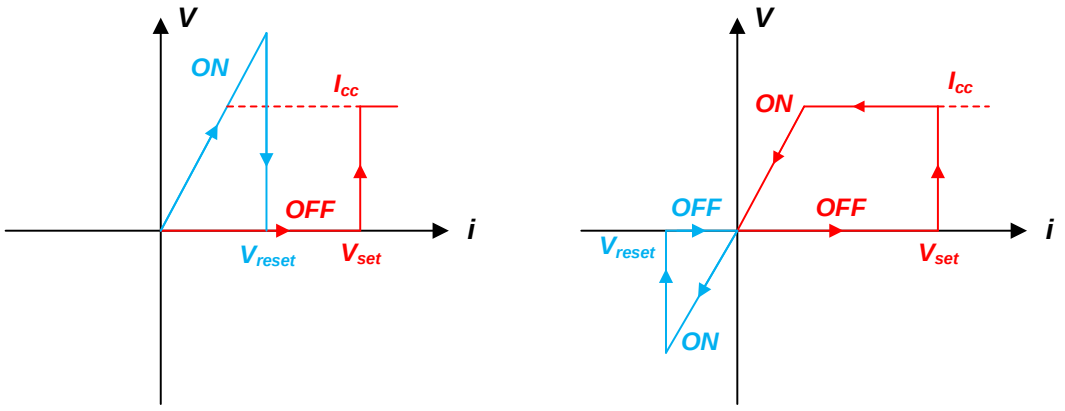


Figure 1.10 Schematic illustration of switching processes of CBRAM devices. (a) Off state; (b) switching on; (c) On state; (d) switching off.

Depending on voltage polarity of the reset operation, there are two modes of operation of the resistive switches, unipolar mode and bipolar mode as shown in Fig. 1.11. In the case of unipolar resistive switching, the polarity of the external voltage for the SET and RESET is the same. The RESET process is very likely thermally assisted due to the high current and tiny cross sections of the filament. For bipolar resistive switching, the polarity of the external voltage for

the SET and RESET is opposite. The Cu- and Ag-migration based memory cells are typical bipolar resistive switches.



(a) (b)

Figure 1.11 (a) Unipolar and (b) Bipolar modes of operations.

1.4.2 Parameters for Evaluation of Memory Device Performance

In order to systematically evaluate the resistive switching performance of devices in this studies, following set of terminologies are used to depict and compare the performance of devices.

Forming Voltage

After the fabrication, the memory cells are in very high resistive state: at the order of tens to hundreds of MΩ since no filament is present. When a high voltage bias is applied, a filament will be formed. The current increases dramatically at V_{form} and the cell switches to LRS. Therefore, FORMING is a phenomena of the formation of the conductive filament in the solid electrolyte for the first time in a fresh cell. Typically, V_{from} depends on the thickness of the dielectric and the materials of electrode metals and dielectric. Different polarity of forming voltage may create different conductive filament in the solid electrolyte.

Set Voltage

SET is the phenomenon of re-establishing the conductive filament after it has been ruptured at least once either by Joule's heating or by electrochemical migration of ions. The SET voltage (V_{set}) is usually lower than V_{form} of the device, possibly because the partial filament exists in the following SET process. SET leads the device into the LRS also called the ON state while the corresponding device resistance is R_{on}

Reset Voltage

RESET is the phenomenon of rupture of the conductive filament bridge either by the ion migration (bipolar mode) or thermal dissolution caused by Joule's heating (unipolar mode). RESET leads the device from a LRS to a HRS. The resistance of the switch during the reset is called as R_{off}.

Compliance Current

During the SET or FORMING process, a limiting current called compliance current (I_{cc}) is applied by the external circuit to prevent the devices getting permanently damaged. In the case of a set operation, the normal range of compliance current used in studies is 1 μA to 10 mA. For the reset operation, there is no need to apply a compliance current limit. When during a RESET operation a low enough compliance current is applied, the filament may never rupture.

Endurance

RRAM devices can be switched from HRS to LRS frequently but each operation can introduce damage known as degradation. Endurance is defined as the number of SET/RESET cycles that can be endured before the HRS and the LRS are no longer distinguishable [46].

Retention Time

Retention time shows the intrinsic ability of the resistive memory device to retain its stored state after it has been programmed or erased. All commercial products aim for a 10 years retention time, regardless of the percentage of time the device is turned on [47].

1.4.3 Switching Mechanism of Cu/TaO_x/Pt Device

Cu/TaO_x/Pt resistive device is a strong candidate for non-volatile memory, which can be switched between high resistive state and low resistive state based on the formation and rupture of two types of nanofilament. During the SET and RERSET operations, a Cu or oxygen vacancy conductive filament (CF) forms and ruptures in the Cu/TaO_x/Pt device in terms of the conduction mechanism. Under a positive bias, the Cu active electrode is oxidized to Cu^+ ions, drifting toward the Pt electrode under the influence of the high electric field. The following reduction-oxidation reaction occurs in the TaO_x layer:

$$Cu \rightarrow Cu^+ + e^- \tag{1.3}$$

The Cu^+ ions get reduced and deposited on the surface of the Pt electrode in the form of Cu atoms. The Cu conductive filament grows vertically until it reaches to the top Cu electrode, at which time the set occurs. After the set, the two electrodes are connected by the CF, leading the device switching from HRS to LRS. When a negative voltage bias is applied to the Cu electrode of a fresh device, the oxygen vacancy conductive filament can be established in TaO_x. The following electrode-reduction reaction occurs in the TaO_x layer:

$$TaO_x + 2e^- \rightarrow TaOx^{-1} + O^{2-} \rightarrow TaO_xV_o + O^{2-} \tag{1.4}$$

The O^{2-} ions migrate from the Cu electrode to the Pt electrode under the electric field pointing from Pt to Cu. Thus, a conductive filament is formed by migrating O^{2-} ions, resulting in vacancies V_o left behind. The device switches to LRS through the oxygen vacancy conductive

filament during the SET operation. Fig. 1.12 shows the two different types of conductive filaments inside a single Cu/TaO_x/Pt resistive device.

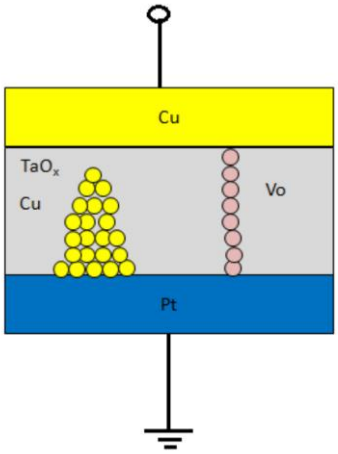


Figure 1.12 Two different types of conductive filaments inside a single Cu/TaO_x/Pt resistive device.

Chapter 2 Characterization of Porous BEOL Dielectrics for Resistive Switching

In this chapter, the porous back-end dielectric materials with porosity from 8% to 25% have been characterized in terms of their resistive switching behavior. Some of the devices incorporated diffusion barrier at either electrode or at both electrodes. The electrical characterization of porous dielectric devices adopts the standard resistive switching testing procedure. The findings show that about 10% of the samples display resistive switching behavior, of which devices with two diffusion barriers can be switched repeatedly, demonstrating that resistive switching in porous dielectrics is feasible. The properties of resistive switching established in this work provide a solid basis for further improvement of RRAM devices based on porous dielectrics compatible with CMOS back-end. In addition, the relation between mobility and diffusivity in porous materials have also been investigated.

2.1 Devices Structure and Fabrication

Devices Structure

The Metal-Insulator-Metal (MIM) structures investigated in this study have been manufactured by Intel Inc. and provided to VTech. The MIM structures have a Cu ground plate as a bottom electrode and top island-shaped W or Pt counter-electrode with various porous dielectrics sandwiched in between. The ILD materials are various nanoporous low-k a-SiOC:H and a-SiC:H dielectrics. The porosity of the ILD layers range between 8% and 25%. Since during the fabrication the MIM structures go through thermal processing at 300-400 ^{o}C, Cu will diffuse from the Cu electrode to the porous ILD layers and contribute to various forms of interconnect failure and poor resistive switching behavior. Since a thin SiCN layer is known to be a good Cu diffusion barrier, some devices in this study have 2nm of SiCN barrier layers, either at the Cu, or W/Pt electrode or both. Table 2.1 provides a summary of the various MIM structures investigated and specifies the metal electrodes, the dielectric type and absence or presence of the SiCN diffusion barrier.

TABLE 2.1 Materials employed in MIM structures received from Intel Inc..

Sample #	BE Dielectric Barrier	Dielectric	TE Dielectric Barrier
394(W)	None	a-SiC:H (k=3.1, 8% porous, 1.3 g/cm^3)	None
389(W)	None	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	None
635(W)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	None
557(W)	None	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	2 nm SiCN
391(W)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	2 nm SiCN
643(W)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2g/cm^3)	None
640(W)	None	a-SiOC:H (k=2.5, 25% porous, 1.2g/cm^3)	2 nm SiCN
388(W)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2g/cm^3)	2 nm SiCN
394(Pt)	None	a-SiOC:H (k=2.5, 25% porous, 1.2g/cm^3)	None
635(Pt)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	None
640(Pt)	None	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	2 nm SiCN
391(Pt)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm^3)	2 nm SiCN
388(Pt)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2g/cm^3)	2 nm SiCN

Fig. 2.1 further schematically depicts the four types of devices investigated in this work. The top electrodes are composed of either W/Al or Pt/Al.

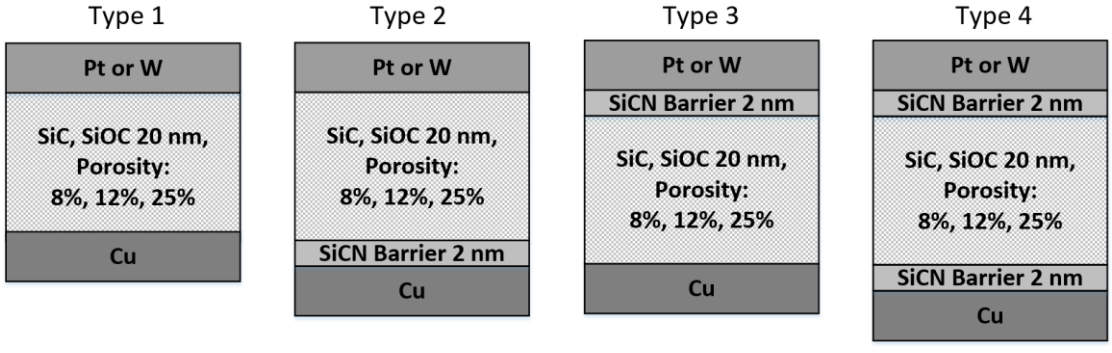
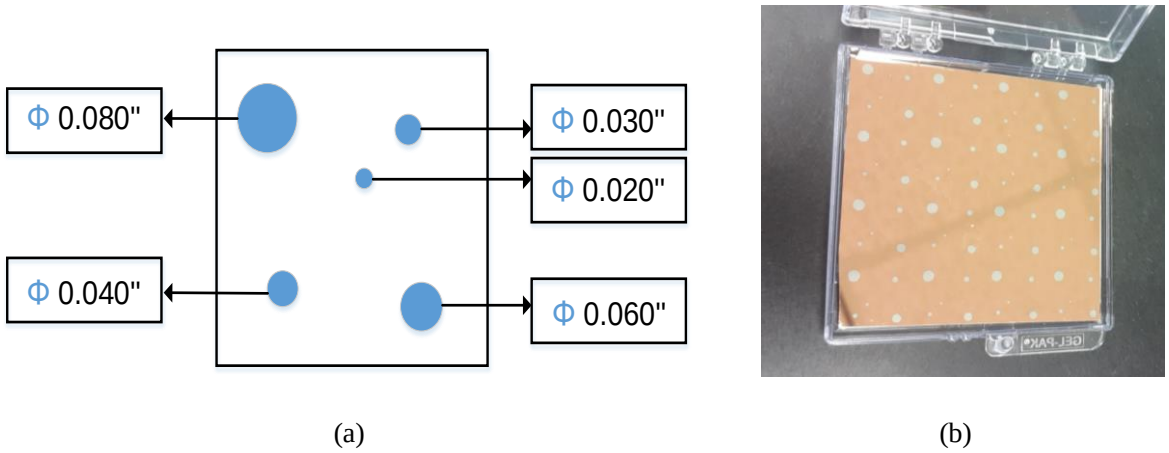


Figure 2.1 Cross-sections of the four types of devices investigated.

Fabrication

This MIM device fabrication starts with a 300 mm diameter Si (001) substrate coated with a 100 nm thick thermal oxide. A standard Ta/TaN adhesion layer followed by Cu seed layer were then deposited on the oxide using industry standard physical vapor deposition (PVD) methods. An electrochemical plating method was then utilized to grow a thick Cu film that was subsequently thinned to approximately 300 nm in thickness via chemical mechanical polishing. Various nanoporous low-k a-SiOC:H and a-SiC:H dielectrics as shown in Table 2.1 were then deposited on the blanket Cu base electrode using standard plasma enhanced chemical vapor deposition (PECVD) methods that have been described in [48-51]. In some cases, a dense 2 nm a-SiCN:H dielectric barrier material was deposited just before or after deposition of the nanoporous dielectric.

The Si/Cu/low-k substrates were next cleaved into 2×2” coupons and the island shaped top electrodes were the formed by shadow masked thermal or electron beam evaporation of 10 nm W or Pt. An additional 200 nm of Al was deposited by thermal evaporation to complete the top electrode structure. The top electrodes are circular and composed of either W/Al or Pt/Al. There are five sizes of the top electrode with diameter ϕ of 0.020’’, 0.030’’, 0.040’’, 0.060’’, and 0.080’’. Device layout is shown in Fig. 2.2 (a). This layout is repeated all over the sample and remains constant for all type of samples. Fig. 2.2 (b) gives a top view of all samples.



(a) (b)

Figure 2.2 Top view of the device layout for (a) single device, and (b) multiple devices.

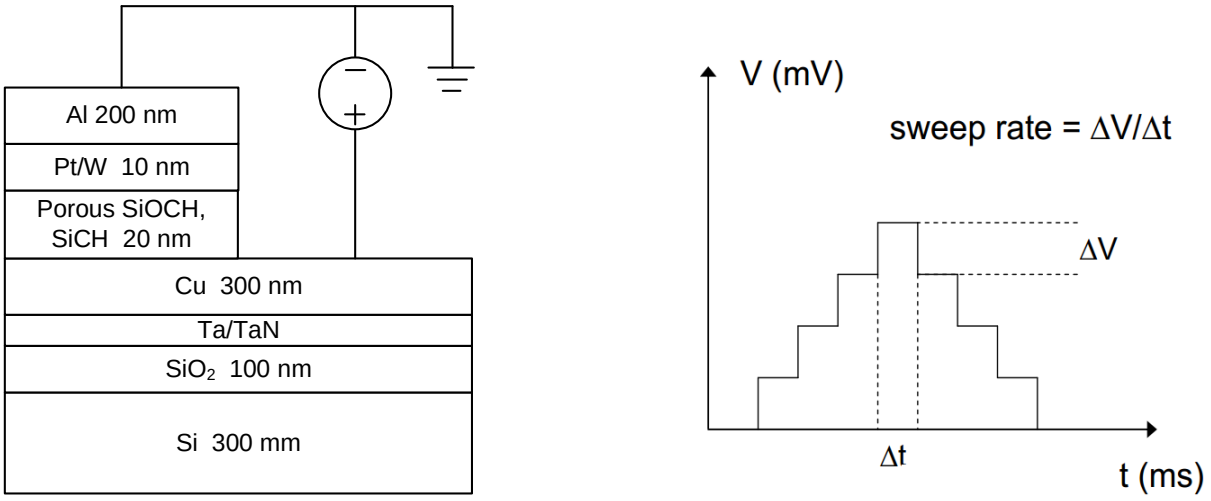
2.2 Characterization Methodology

To demonstrate whether the resistive switching in porous dielectric is feasible, the porous dielectric devices have been subjected to the standard resistive switching characterization, which will be discussed in this section.

2.2.1 Standard Resistive Switching Characterization

For the purpose of electrical characterization, the Keithley 4200–SCS (Semiconductor Characterization System) has been used to characterize the resistive switching behavior of the porous dielectric devices. This system allows a complete characterization of devices, materials and semiconductor processes at different temperature.

The experimental set-up is represented in Fig. 2.3 (a). Positive or negative voltage sweep was applied on the bottom electrode Cu while the Pt/Al and W/Al top electrodes were connected to the ground. The voltage applied is a DC voltage. The two most important parameters of this characterization circuit are the voltage sweep rate and compliance current. Voltage sweep rate is defined as the rate of change of voltage with time. The devices are stressed with a linear ramp voltage having a natural interval time of 50 ms per step size. In other words, if the device has a sweep rate of 0.01 V step size, it essentially means that the sweep rate is 0.2 V/s. The schematic diagram of a dual sweep from 0 V to a maximum voltage and back to 0V is given in Fig. 2.3 (b). The voltage is ramped up from 0 V at a specified step size and until a specified stop voltage is reached. The voltage is then stepped back to zero volts. The process and electrical characterization of these devices have been performed using Keithley 4200 SCS.



(a) (b)

Figure 2.3 Experimental Set – Up (a) Cross sectional view of porous low-k devices; (b) Schematic illustration of voltage sweeping mode in DC characterization.

All devices have been subjected to the standard resisting switching characterization as shown in Fig. 2.4 The voltage is being ramped starting at 0 V on the positive bias axis while the current is being monitored. Cu cations dissolve in the solid electrolyte and migrate through it. Gradually Cu cations are electrochemically reduced on the Pt or W electrode. As more Cu atoms accumulate, a nanoscale metallic conductive filament (CF) forms providing a conductive path between two electrodes. The state transition from HRS to LRS is called SET process characterized by a critical voltage V_{set}. At a critical voltage V_{set}, the current increases very rapidly indicating that the device became highly conductive. For a fresh device cell, a significantly higher positive voltage is needed for the SET process, which is known as forming voltage. Usually, lest the device be damaged, a compliance current I_{cc} is applied to limit the current flowing through the device. The level of I_{cc} determines in many instances the nature of the filament and the value of the on-state resistance, R_{on}. After the forming or setting operation, when the voltage is ramped down, the device displays in most cases an ohmic behavior of the on-state and characterized by R_{on}. A high current passing through the filament can rupture the bridge and restore HRS. This is called RESET process of the device characterized by a critical voltage V_{reset}. When the current, at negative bias, reaches a critical high current I_{reset} at V_{reset}, the conductive state is ruptured and the device reverts to the off-

state characterized by a high resistance, called R_{off}. The current collapses to a small value characterized by high resistance R_{off}.

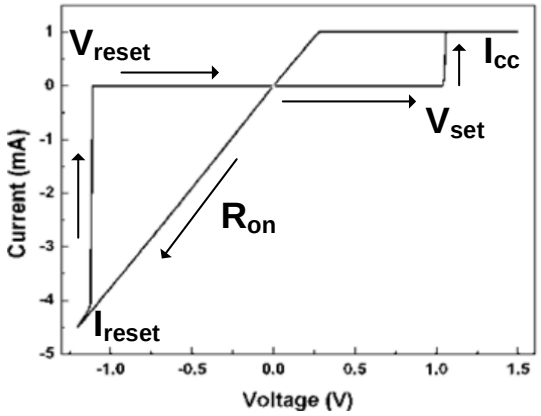


Figure 2.4 Standard resistive switching characterization. The quantities being monitored are: R_{off}, V_{set}, R_{on}, V_{reset}, and I_{reset}.

2.2.2 Keithley Calibration of Temperature Coefficient of Resistance (TCR) Measurement

Temperature Coefficient of Resistance (TCR)

In any material, the internal resistance will change as the temperature changes. The rate of resistance change based on temperature is referred to as the Temperature Coefficient of Resistance (TCR) and is defined by the coefficient α in eq. (2.1). The resistance of a conductor at any given temperature can be calculated from a knowledge of the temperature, TCR, its resistance at a standard temperature, and the temperature of operation. The equation for this resistance temperature dependence can be expressed in general terms as:

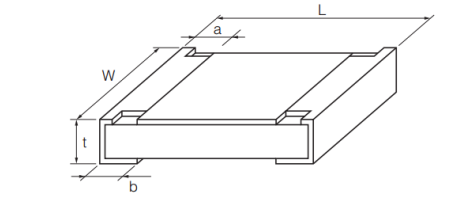
$$R = R_{ref}[1 + a(T - T_{ref})] \tag{2.1}$$

where R is the resistance at temperature T. R_{ref} is the resistance at temperature T_{ref}. T is the material temperature after operation. T_{ref} is the reference temperature. In this study, the room temperature of 25°C is used as reference temperature to calculate TCR. The α constant is known as temperature

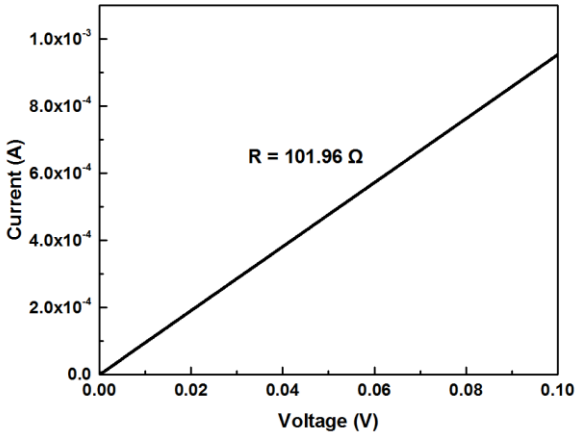
coefficient of resistance, and symbolizes the resistance change factor per degree of temperature change. If TCR is a positive number, it means that material resistance increases with increasing temperature. Positive TCR generally indicates metallic conduction behavior. On the other hand, a negative TCR indicates semiconductive conduction behavior. It is known that TCR of bulk Cu is $\alpha = 0.0039K^{-1}$. We use TCR to identify the type of filament formed in our devices.

Keithley Calibration of Resistance Measurement

The test sample is a 100 Ω (1% tolerance) thick film resistor produced by Panasonic Inc.. Fig. 2.5 (a) shows the package image of this 100 Ω thick film resistor. The test set-up is conducted by ramping the voltage sweep from 0 V on the positive bias axis to 0.1 V. The current increases to 952 μA when the voltage reaches to 0.1V, as is shown in Fig. 2.5 (b). Therefore, the resistance of this film resistor is 101.96 Ω measured by experiment. Considering a 1% tolerance of the resistance, there is just 1% error of testing, which may be introduced by the series resistance in nickel probes.



Part No. (inch size)	Dimensions (mm)				
	L	W	a	b	t
ERJ3R□ ERJ3EK (0603)	$1.60^{\pm0.15}$	$0.80^{+0.15}_{-0.05}$	$0.30^{\pm0.20}$	$0.30^{\pm0.15}$	$0.45^{\pm0.10}$



(a) (b)

Figure 2.5 (a) Package image of the 100 Ω thick film resistor; (b) I-V characteristic of the resistor.

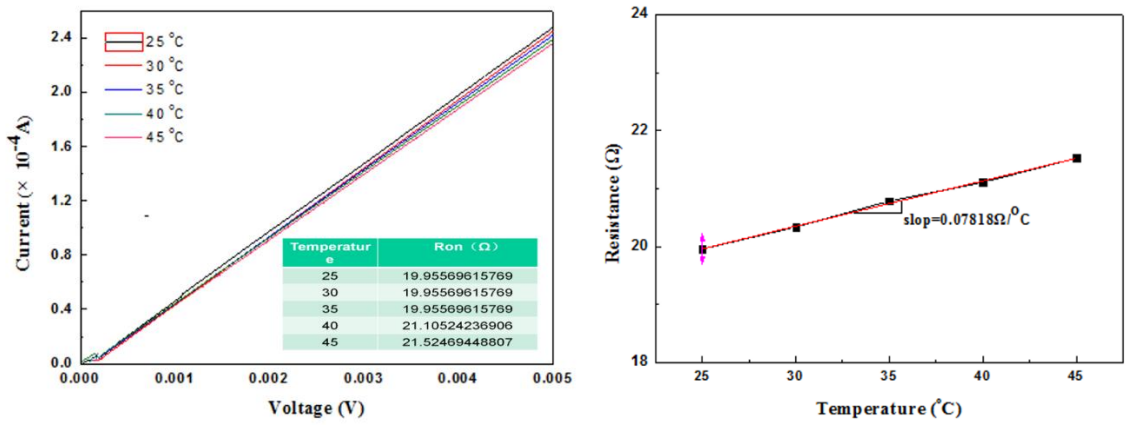
Keithley Calibration of TCR Measurement

For the purpose of measuring the TCR of materials, a temperature controller is need to connect to the variable temperature probe station. The model S-1060R automative Temperature

controller (Lucas Signatone Corp.) is used to control the temperature of Chuck on the probe station. Its control heaters and calibrated thermometers for active temperature control with a typical stability of 0.05K in the entire temperature range of 5-450 K.

There are three important and basic test conditions that have been explored and summarized through numerous TCR measurements. (1) The vacuum pump should be always turned off during the measurement. The vacuum pump is usually used to remove the gas molecules between the wafer and chuck, leading the wafer sticking tightly to the chuck because of the vacuum. However, in case of the TCR measurement, the flowing air under the wafer will reduce the surface temperature of wafer, resulting in inaccurate testing results. Thus, the vacuum pump should be turned off before placing the probe. (2) During the testing, the temperature controller should also be turned off. It is suggested that first the device should be heated to the target temperature, and then be maintained at this temperature for 10 minutes, and subsequently turning off the temperature controller afterwards, followed by measuring the R_{on} at small voltage values (0.1V). (3) The testing samples need to be placed at the upper-right corner of the chuck, because the thermocouple is under the upper-right corner of the chuck and will thus provide most reliable temperature reading.

To calibrate the TCR measurement by Keithley and verify the test conditions given above, an experiment of measuring the Cu line is conducted. Fig. 2.6 indicates the testing sample of $Cu/TaO_x/Pt$ devices seen from the microscope. Two probes are placed on the ends of a Cu line. The Cu line is stressed with a linear ramp voltage starting from 0 V to 5 mV. The temperature of Cu line increases range from 25°C to 45°C, with a temperature step of 5°C, heated by the temperature controller. The currents flowing through the Cu line under five different temperatures are recorded, as is shown in Fig. 2.6 (a). It can be seen that the increasing of slops for each curve is uniform. Based on the data from Fig. 2.6 (a), the TCR of Cu line is $0.003918K^{-1}$ by curve fitting, which is exactly the same as $0.0039K^{-1}$ for bulk copper. We therefore conclude that Cu lines 300 nm thick and at least 1 μm wide behave like bulk copper.



(a) (b)

Figure. 2.6 (a) I-V characteristics of Cu line; (b) TCR of Cu line.

Based on the above experiments, relatively accurate TCR values can be achieved if the test is operated under the three TCR testing conditions as summarized above.

2.3 Characterization Results

2.3.1 Intrinsic Conductive State

When the porous devices were subjected to this type of electrical characterization, it was found that 90% of all four types of devices were conductive from the beginning with a low resistance of 50 Ω and below. The remaining 10% of the devices showed various degrees of resistive switching behavior, which will be described in more detail in the subsequent sections. In order to determine the nature of this initial conductance for each type of a device, the resistance has been plotted as a function of the area of the top electrode. A typical result is shown in Fig. 2.7 In all device cases, it has been found that the resistance is inversely proportional to the area of the device, according to the relation $R_{on}=\rho \cdot d/A$, where $A=\pi(\phi/2)^2$ is the area of the top electrode and d is the thickness of the dielectric.

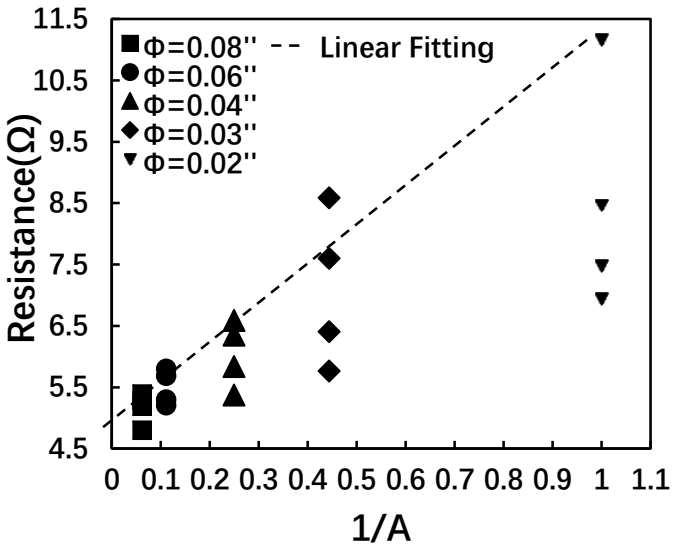


Figure. 2.7 Plot of the resistance as a function of the inverse value of the area of the top electrode in 635-Pt.

From these results it is concluded that the conduction is a bulk phenomenon and not filamentary conduction that is typical for resistive switching. To determine the nature of the conduction better, the temperature coefficient of resistance (TCR) for all types of the devices have been measured. We obtain a consistent value for TCR = 0.0026-0.0029 K^{-1}. An example of such TCR measurement is shown in Fig. 2.8.

The TCR value of TCR=0.0026 - 0.0029 K^{-1} is very close to the value that we have found for Cu filaments in Cu/TaO_x/Pt devices TCR =0.0031K^{-1}. However, a value of 0.0031K^{-1} is found when the R_{on} resistance of the filament is below 1000 Ω. For R_{on} of a few kΩ found in Cu/TaO_x/Pt devices is TCR ≈ 0.0028K^{-1}. This suggests that the initial highly conductive state is due to high concentration of Cu dissolved in the dielectric. The Cu diffusion must have taken place during the fabrication process. The process steps that are involved in the fabrication are: the deposition of porous dielectric, deposition of the SiCN diffusion barriers, and the deposition of the top electrode. The first two employed temperatures on the order of 400 °C for a few minutes whereas the latter was performed at temperatures closer to room temperature. Clearly, as the initial conduction has been observed also in type 4 devices, the diffusion barriers SiCN where not efficient enough in

preventing the Cu diffusion and shorting of the devices in most cells even with two diffusion barriers. However, as it will be shown in the next section, only devices with at least one barrier displayed resistive switching behavior indicating that the Cu diffusion was significantly reduced by the SiCN barriers.

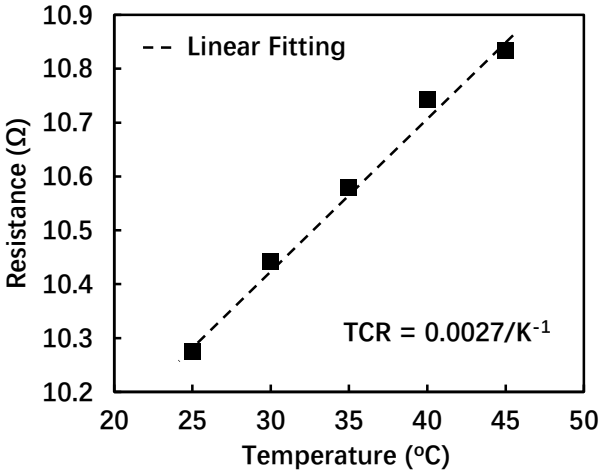


Figure 2.8 Resistance as a function of temperature for a device in 394-Pt that has been found highly conductive from the beginning.

The resistance of the samples that are conductive from the beginning as a function of the imposed I_{cc} current is investigated, i.e. the maximum current that is allowed to flow through the device. This means that voltage has been ramped up until the imposed compliance current I_{cc} has been reached. Thereafter, the device was characterized at small voltages to determine its resistance. A typical behavior is shown in Fig. 2.9. As can be seen, the resistance decreases linearly with inverse I_{cc} in an interval of very low I_{cc} values up to I_{cc} around 7-9 mA and at I_{cc} = 10 mA according to

$$R_{on} = 0.02/I_{cc} \tag{2.2}$$

and beyond I_{cc}=10 mA remains flat. This is a very interesting observation. The constant of 0.02 V in the equation 2.2 indicates that the minimum forming voltage of these devices is 0.02 V [52]. It appears that current flowing through the device deposits Joules heat, which leads to an elevated

temperature in the Cu-doped dielectric. Such a current-induced annealing could lead to: 1) a higher electrical activation of Cu by allowing Cu atoms to find substitutional sites where Cu can be easily ionized and thus contribute to conduction, and 2) to more Cu diffusion leading to a more uniform Cu distribution throughout the dielectric.

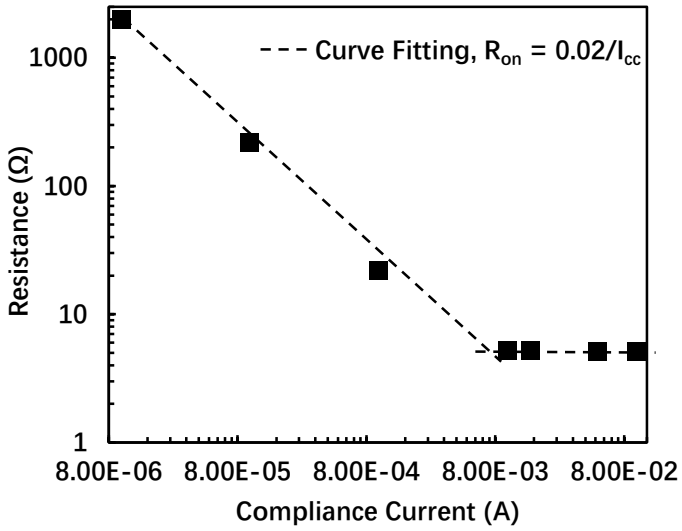


Figure 2.9 Resistance plotted as a function of the compliance current I_{cc} for a device in 391-Pt that shows low conductance state from the beginning.

When the current is high enough this kind of electric activation of Cu by annealing is complete and further increase of current does not lead to a higher electric activation. This can be seen in the interval 10 mA < I_{cc} < 100 mA where the resistance of the sample becomes constant: Our data has not enough resolution of the I_{cc} values to decide whether the change from the linear to flat behavior is sharp as indicated by the extrapolating lines in Fig. 2.9. or whether this transition is gradual as one would expect this for heat activated activation or diffusion phenomena. The experimental difficulty is that any measurement at a given I_{cc} leads to irreversible changes and one is quickly running out of not-yet-tested samples. A similar type of annealing effects can be observed when the I-V characteristic is carefully inspected at high resolution of the voltage scale. As shown in Fig. 2.10, the slope of the I-V changes from initially 72 Ω to a slope of 9.4 Ω at a very low voltage of 2.5 mV. This kind of behavior has been consistently observed for all samples. Another

manifestation of the same effect is shown in Fig. 2.11. Here the voltage at which the slope changes abruptly is also 2.5 mV. The currents at which the transition happens, are well below 1 mA, i.e. much lower than the critical I_{cc} current at which R_{on} becomes independent of I_{cc} as shown in Fig. 2.10. Moreover, in this case, it can be seen that the transition is very sharp, one linear slope changes abruptly into a different linear slope. This sharp transition with gradual increase of voltage and current is rather puzzling and indicates some kind of phase transition whose nature remains presently unclear.

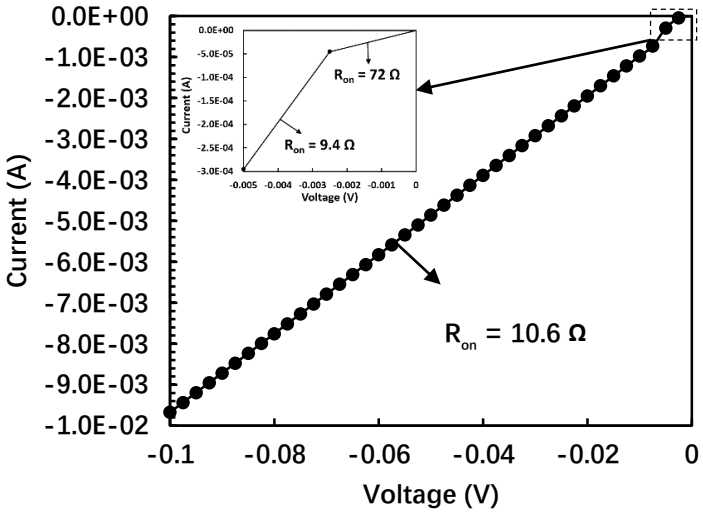


Figure 2.10 Sharp transition of I-V slopes observed on mV scale.

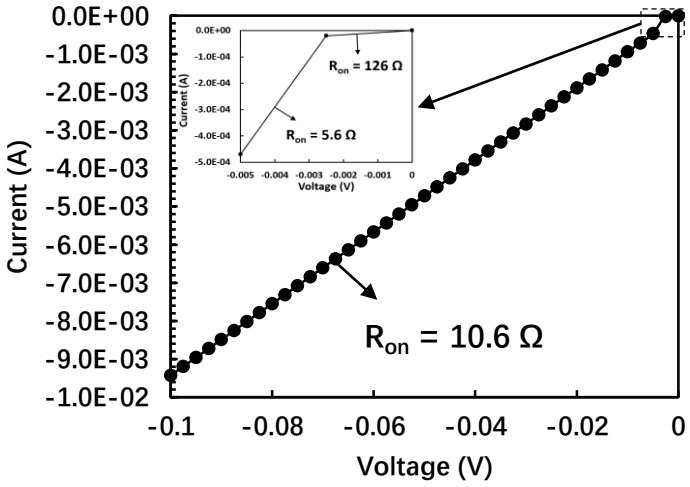


Figure 2.11 A similar transition of slopes of the I-V characteristic as in Fig. 2.10 for another device in 394-Pt.

2.3.2 Resistive Switching Behavior of the Porous-Dielectric Devices at Positive Bias Applied to Cu Electrode

Table 2.2 gives the forming voltages at positive and negative bias for the four type of devices. Overall, less than 10% of all cells show resistive switching phenomena. It is also noteworthy that only the cells with at least one diffusion barrier belong to this category. This indicates that in all cells the diffusion of Cu is very substantial. However, the diffusion barriers help to keep the Cu diffusion at bay.

TABLE 2.2 Forming voltages at positive bias for the four type of devices.

Sample #	BE Dielectric Barrier	Dielectric	TE Dielectric Barrier	Forming Voltage (+)
394 (W)	None	a-SiOC:H (k=3.1, 8% porous, 1.3 g/cm3)	None	N/A
389 (W)	None	a-SiC:H (k=3.1, 8% porous, 1.2 g/cm3)	None	N/A
635 (W)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	None	0.45 V
557 (W)	None	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	2 nm SiCN	0.5 V
391 (W)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	2 nm SiCN	0.6 V, 0.5 V
643 (W)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	None	0.84 V, 0.9 V 1 V
640 (W)	None	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	0.6 V, 0.43 V, 0.5 V
388 (W)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	2.1 V, 1.2 V, 0.89 V
394 (Pt)	None	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	None	N/A
635 (Pt)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	None	N/A
640 (Pt)	None	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	N/A
391 (Pt)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	2 nm SiCN	N/A
388 (Pt)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	2.3 V, 1.8 V, 1.4 V, 1.25 V

A typical behavior of resistive switching is shown in Fig. 2.12. In case of sample 391-W, the forming voltage (a voltage at which a filament is formed for the first time) is $V_{form} = 0.5$ V at $I_{cc} =$ 1mA the $R_{on} = 570$ Ω. The on-state cannot be reset, i.e. the device is permanently damaged. During the reset operation the on-state undergoes a secondary set leading to a lower on-resistance of R_{on}

= 7.8 Ω. In some cases, as shown in Fig. 2.13 for the sample 388-W, the conductive filament can be set at V_{form} = 2.1 V, reset back to the off-state at V_{reset} = -1.0V, and set again at positive bias at V_{set} = 1.4 V.

Overall, the best resistive switching behavior has been observed for devices with two diffusion barriers. Devices with tungsten electrode show better resistive switching behavior than samples with platinum electrode. Also, the best resistive switching behavior has been observed for dielectrics with the highest porosity of 25%. A summary of all results for forming voltage when positive bias is applied to the Cu electrode is shown in the 5th column of Table 2.2.

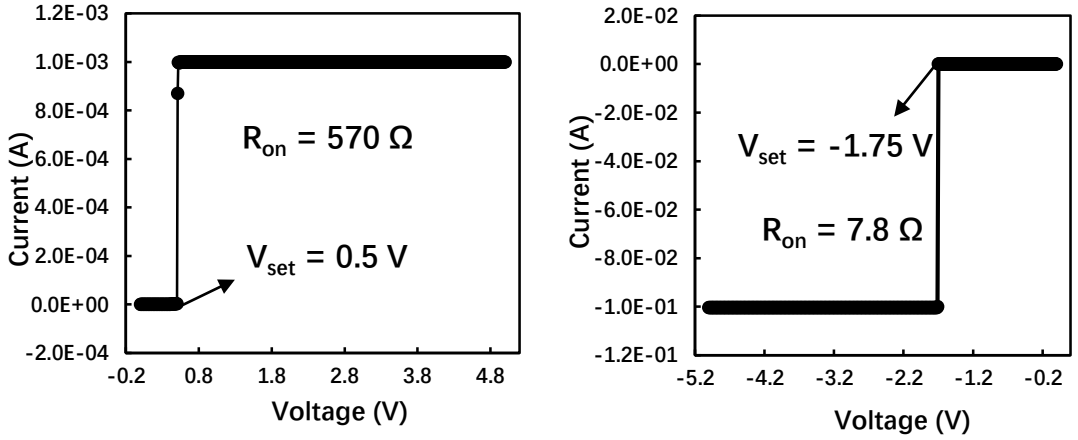
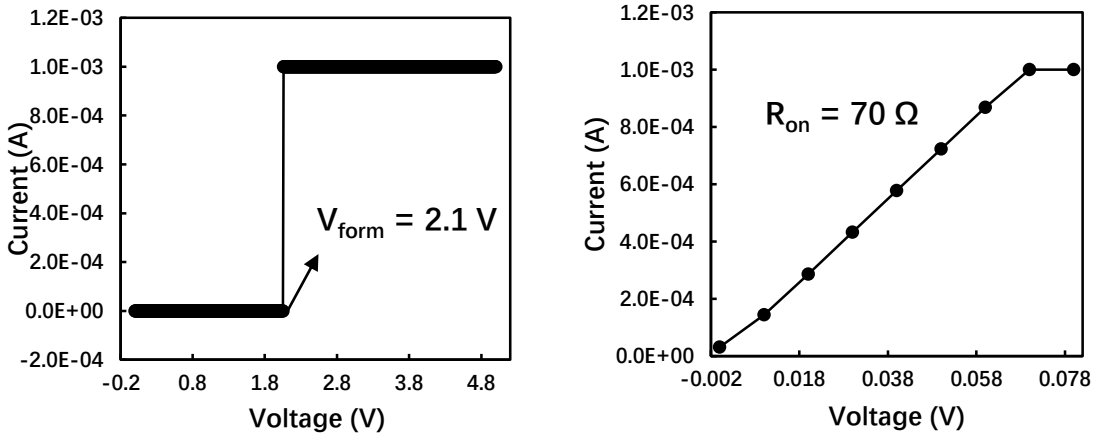


Figure 2.12 V_{form}=0.5V observed for sample 391-W, R_{on}=570 Ω at I_{cc}=1 mA. During the reset operation at negative bias, the device undergoes a secondary set at V_{set}=-1.75 V leading to R_{on}=7.8 Ω at I_{cc}=1mA.



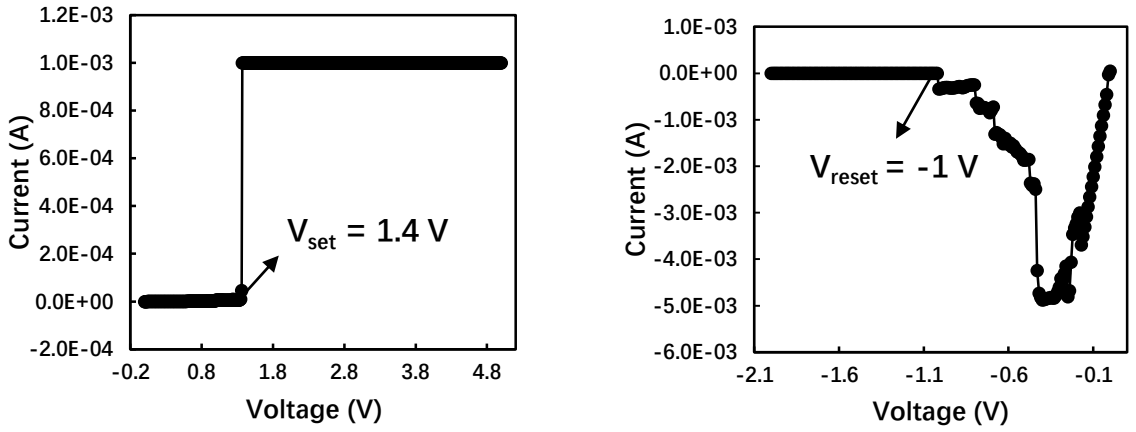


Figure 2.13 Full resistive switching cycle of forming, resetting, and setting has been observed for the sample 388-W.

Devices with tungsten electrode show generally a better resistive switching behavior. A conspicuous case is the direct comparison between the samples 388-W and 388-Pt as shown in Table 2.2. These samples are identical except for the counter electrode material. While 388-W can be set and reset several times, sample 388-Pt can be set only one time and is not resettable subsequently. In the present study, W has been deposited by PVD. Since W has a much higher melting temperature (3422 ^{o}C) than the melting temperature of Pt (1768 ^{o}C) the W films deposited by PVD have a much rougher surface than Pt films. The rougher surface and formation of conductive W or WSi or WCuSi asperities is much more conducive to the formation of local filaments than the relatively smooth Pt-dielectric interface. To render the local conductive filaments to be ruptured, we know from our previous work [53] that filaments must have a weak spot or a constriction where they can be ruptured. Conductive asperities of the W-dielectric interface provide such a constriction. When the current is high enough the filament will be ruptured at the junction, where the filament touches an asperity, since this constriction will offer the highest resistance and hence will lead to the highest Joules heat deposition.

From Table 2.2 it can be seen that dielectric materials with higher porosity have higher V_{form} voltages. Device 388-W with 25% porosity has a V_{form}=0.89 V-2.1 V, while device 391-W with 12% porosity has V_{form}=0.45 V-0.50 V.

2.3.3 Resistive Switching Behavior of the Porous-Dielectric Devices at Negative Bias Applied to Cu Electrode

When a negative bias is applied to the Cu electrode, the Cu ions will be moved toward the Cu electrode. Thus, in order to establish a conductive filament, some negatively charged defects or a bridge of conductive bonds needs to be established across the dielectric. Fig. 2.14 shows an example of a filament formation at negative bias for the sample 388-W.

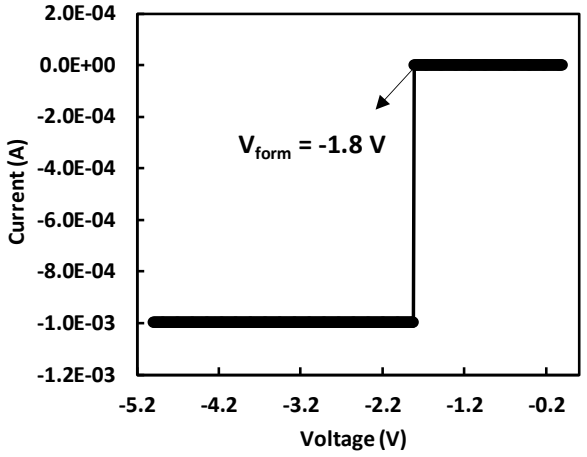


Figure 2.14 Filamentary forming at negative bias at V_{form} = -1.8 V for 388-W.

The device 391-W can be set and reset several times. The results are as follows: V_{form}= -0.48 V resulting in R_{on} = 60 Ω at I_{cc} = 1 mA. The first reset is observed at V_{reset} = 0.37 V and the subsequent set at V_{set} = -1.6 V. A summary of the results for negative bias stress is shown in column 5 of Table 2.3. Similarly, to the results obtained for positive bias and the resulting Cu filaments, samples with ILD of higher porosity show significantly higher forming voltage also at negative voltage bias. Also, comparing the results for samples 394-W and 394-Pt, one can see that devices with W electrode show much better resistive switching behavior. Thus all observations made in this context made on Cu filaments apply to the defect conductive filaments.

TABLE 2.3 Forming voltages at negative bias for the four type of devices.

Sample #	BE Dielectric Barrier	Dielectric	TE Dielectric Barrier	Forming Voltage (-)
394 (W)	None	a-SiOC:H (k=3.1, 8% porous, 1.3 g/cm3)	None	N/A
389 (W)	None	a-SiC:H (k=3.1, 8% porous, 1.2 g/cm3)	None	N/A
635 (W)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	None	-0.52 V
557 (W)	None	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	2 nm SiCN	-0.47 V
391 (W)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	2 nm SiCN	-0.9 V, -0.85 V
643 (W)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	None	-1.9 V, -1.3 V -1 V
640 (W)	None	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	-1 V, -0.91 V, -0.7 V
388 (W)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	-1.9 V, -1.6 V, -1.2 V
394 (Pt)	None	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	None	N/A
635 (Pt)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	None	-0.54 V
640 (Pt)	None	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	-0.55 V
391 (Pt)	2 nm SiCN	a-SiC:H (k=2.8, 12% porous, 1.2 g/cm3)	2 nm SiCN	-1 V, -0.87 V, -0.73 V
388 (Pt)	2 nm SiCN	a-SiOC:H (k=2.5, 25% porous, 1.2 g/cm3)	2 nm SiCN	-2.3 V, -2.2 V, -1.5 V

2.3.4 Dependence of Resistive Switching Behavior on I_{cc}

We have tested four of devices 391-W, 388-W, 391-Pt, and 388-Pt applying a much lower compliance current of I_{cc} = 10 μA, instead of the standard I_{cc} = 1 mA used so far. The results obtained confirm our previous findings: (i) V_{form} increases with increasing porosity, (ii) V_{form} is no affected by the choice of I_{cc} (except at a very low values), (iii) I_{cc} level is critical for volatile or non-volatile formation: while at I_{cc}=1 mA the on-state is non-volatile; at I_{cc} = 10 μA is often volatile as shown in case of sample 388-W in Fig. 2.15 with V_{form} = 2.2 V. When a conductive state is volatile, it means that upon unpowering the device, the device reverts spontaneously to the off-state. In the subsequent electrical stress, the device can be set again to the conductive state at $V_{set}(1)$ = 1.8 V. This state is volatile too as long as Icc remains low. In the subsequent set operations the conductive state can be set $V_{set}(2)$ = 1.8 V, and $V_{set}(3)$ = 1.5 V resulting in volatile state. Low

I_{cc} means according to the eq. (2.2) that R_{on} is large. A filament with large R_{on} is bound to be thin and therefore fragile and prone to spontaneous rupture when the device is unbiased.

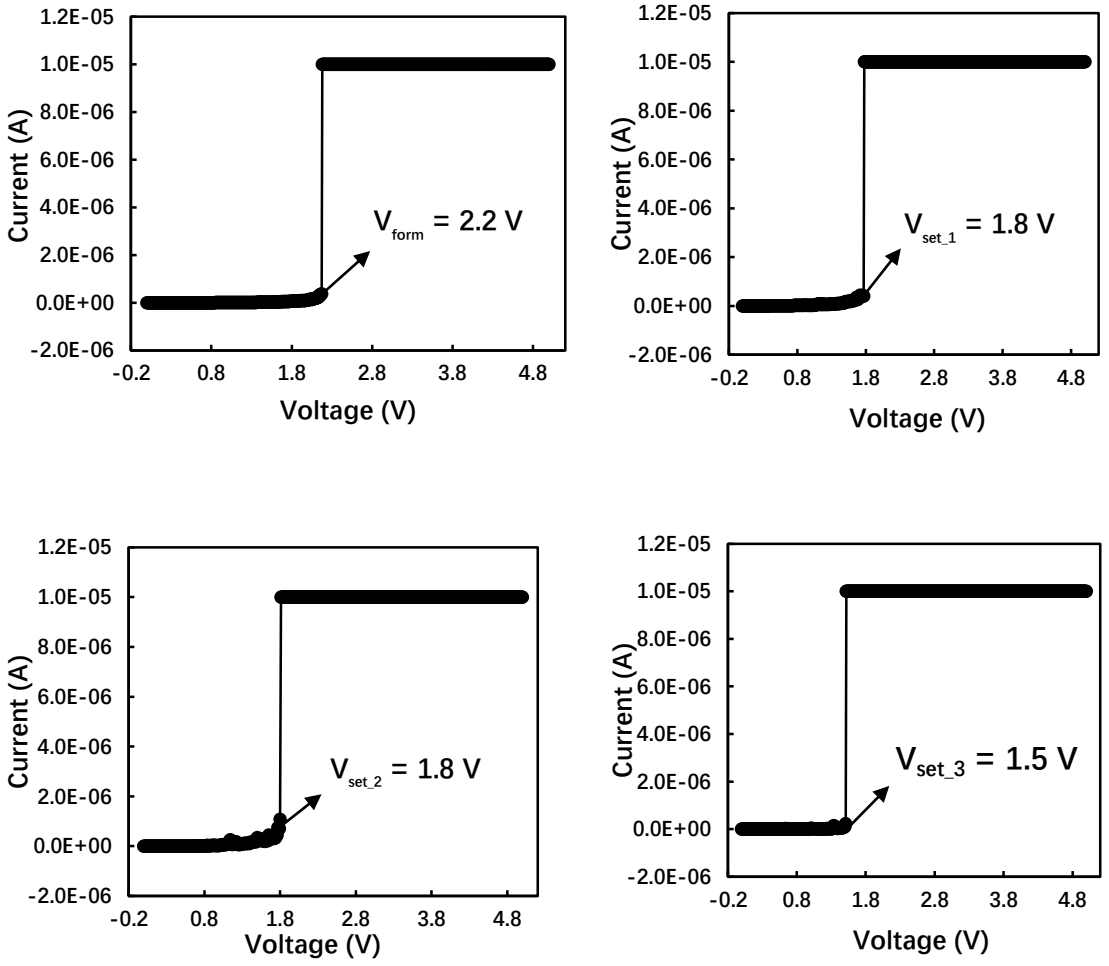


Figure 2.15 Volatile resistive switching behavior of the 388-W sample at I_{cc} = 10 μA.

2.3.5 Dependence of the On-State Resistance on Temperature

Above it has shown that the TCR of the intrinsic bulk conductive state of most devices was TCR = 0.0026-0.0029 K^{-1}, which is attributed to the bulk conductance of the dielectric doped highly with Cu. For those devices that have shown conductive filament formation we have performed the same characterization. One example is shown in Fig. 2.16 for the sample 391-W.

The conductive state has been set at positive bias by formation of a Cu filament. The TCR value is 0.0031 K^{-1}.

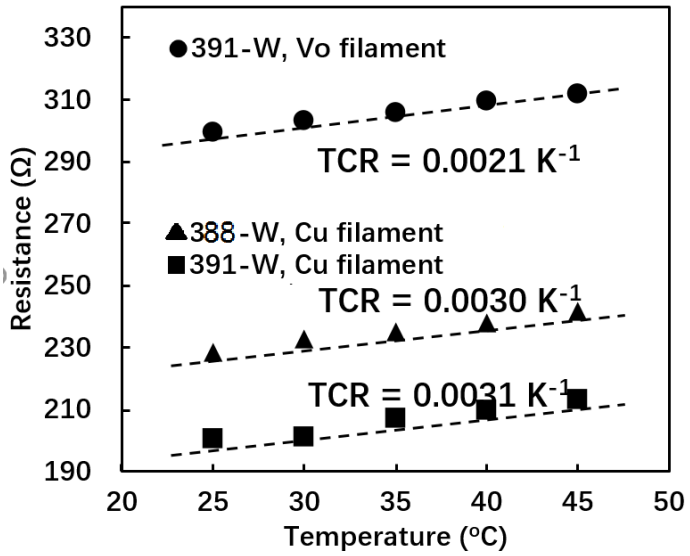


Figure 2.16 Resistance as a function of temperature for a filament formed in 391-W at positive bias (V_{form} = 0.58 V) and 391-W at negative bias (V_{form} = -0.73 V), and 388-W (25% porosity) at positive bias (V_{form} = 2.2 V).

This is exactly the same value that have been found for Cu filaments in Cu/TaO_x/Pt devices [54]. This finding confirms our hypothesis that for those devices that are not conductive from the beginning, a filament of high density Cu doping is being formed during the forming or setting operation.

The same characterization we have applied to filaments formed in the initially non-conductive devices at negative bias. An example of such measurements is shown for 391-W in Fig. 2.16. It can be seen that TCR for filaments formed at negative bias are very different from TCR for filaments formed at positive bias. In case of negative bias, we find typically TCR = 0.0021 K^{-1}. Thus it can be concluded that the filaments formed at positive and negative bias are of different nature. In Cu/TaO_x/Pt samples TCR=0.002 K^{-1} have been found for oxygen vacancy filaments. Since the value of TCR found for filaments formed at negative bias, we ascribe critical parts of the negative bias filaments to aggregation of oxide defects with an activation level close to the Fermi

level. It has been inquired as to whether the porosity of the material may have an impact of the TCR coefficient. In Fig. 2.12, it has shown TCR= 0.0031 K^{-1} for 391-W sample which has 12% porosity. Fig. 2.12 shows the TCR for sample 388-W which has 25% porosity. As it be seen from Fig. 2.12, a very similar TCR of 0.0030 K^{-1} for 388-W is obtained. Thus porosity does not seem to impact the composition of the conductive filament. This is plausible since once a Cu filament has been formed somewhere in the device it must have found a path avoiding pores in the oxide.

2.3.6. Dependence of Resistive Switching Behavior on Annealing of the Device

To study of the impact of the ambient temperature of V_{form} was made under the assumption that the dielectric has been rendered conductive by the Cu diffusion into the dielectric. The fact, that only few samples were not conductive from the beginning, was attributed to the insufficient homogeneity of the Cu distribution at sufficiently high activation levels. The samples have been measured at 27 ^{o}C (room temperature), 40 ^{o}C, 60 ^{o}C, and 100 ^{o}C. The chuck of the probing station was the heat source. The time of such an anneal was a typical set up time before the actual measurement has been performed. This time is between 4 and 5 min. The results confirm that with increasing temperature more and more samples became conductive from the beginning. At 100 ^{o}C all the samples (even those with two diffusion barriers) became conductive from the beginning. Some interesting additional findings have been made on devices conductive from the beginning. A sample in a conductive state at 27 ^{o}C and exposed to 40 ^{o}C and 60 ^{o}C could rupture spontaneously and become conductive again at a sharp voltage, V_{form} = 0.6 V at 40 ^{o}C. The device was fully conductive at room temperature, but became non-conductive at 40 ^{o}C at very small voltages. One observes that at 60 ^{o}C the rupturing effect seems to be more pronounced as it needs a higher voltage to restore the conductive state, V_{form} = 1.7 V. At 100 ^{o}C not a single device has been found that was not conductive from the beginning. Thus, it appears that excessive Cu doping leads to erratic resistive switching behavior. This behavior could be explained by non-uniform Cu diffusion caused by spatially non-uniform temperature distribution resulting from the selective Joules heat deposition within the quasi conductive porous dielectric.

From the results and discussions above, we conclude that although some extent of Cu diffusion into the dielectric appears to be desirable and useful to reduce the switching voltages (V_{form}, V_{set}, V_{reset}) of a memory cell, it has to be carefully controlled because excessive Cu diffusion renders them all conductive and resistive switching becomes either erratic or impossible. The extent of Cu diffusion will have to be further qualified and correspondingly tightly controlled to meet the requirements of reliability and endurance in a given temperature interval targeted for the specific deployment of the device. Although this will be a subject of future studies, it can already be ventured today to predict that engineering of Cu-diffusion barriers will have to play a crucial role in this effort.

2.3.7 Summary and Improvement

From our results it has seen that even devices with two metal diffusion barriers suffered from extensive Cu diffusion rendering most samples conductive from the beginning. One obvious remedy would be to make the SiCN barriers thicker. This will, naturally, increase the effective dielectric constant and hence the interlayer capacitance which is at cross-purposes with the motivation of introducing porous ILDs in the first place. Therefore, in order not to increase the capacitance value, it has been proposed to have only one diffusion barrier on the Cu side but to increase it from 2 nm to 3 nm, 4 nm, 5 nm. The lack of barrier on the W/Pt side could be advantageous in case of W electrode, as our results indicated that a rough W surface with some W penetration into the pores is conducive to formation of filaments with a constriction (or a weak link). Constriction in a filament defines the rupturing location of the filament leaving the remaining parts of the filament more or less intact. As to the choice of porosity, the results indicate that high porosity leads to high forming voltages. This may be related to the reduced global mobility of ions in porous dielectric as explained in more detail in the subsequent section. On these grounds dielectrics with 25% porosity for the purpose of acceptable resistive switching behavior should be excluded. It is proposed to complement the one thicker dielectric barrier postulated above with porous dielectric film with 8%, 10%, and 12%. Lower porosity materials will be conducive to

lower switching voltages with the tradeoff of a higher effective dielectric constant. An additional parameter could be a gradient of porosity in the dielectric film, if this is feasible during the process step of layer deposition. Both kinds of a gradient could be tried out: higher porosity at the Cu electrode and lower porosity at the W/Pt counter-electrode and vice versa. A gradient defined by the difference of 8% and 25% over 20 nm (or smaller) could be possibly realized. The reasoning behind this proposal is as follows. Large porosity leads to high V_{form} when it affects all the 20 nm of ILD thickness. But, when only 5 nm of the ILD displays high porosity and the rest lower porosity, the V_{form} might be greatly reduced. From our previous parts of this project we have estimated that the rupturing gap in a metallic filament should be about 4- 5 nm. Thus large porosity within 4-5 nm should not interfere much with good resistive switching properties.

Another way to suppress the Cu diffusion while keeping the SiCN diffusion barriers thin would be to deposit a smattering (using ALD) of Ti or TiN on the Cu electrode. The thickness of these layers could be 1 nm or less. This will reduce the Cu diffusion into the dielectric and provide a good bonding since Ti is very reactive with Si, O, and C. In this case, we propose a Ti or TiN layer of 0.3 nm, 0.6 nm, 1.0 nm followed by 2 nm, 3 nm, 4nm of SiCN with no barrier layer on the W electrode side. Thus Ti or TiN layer could be less than one full atomic layer. Its purpose is not to stop completely the injection of Cu ions into the dielectric but merely to lower its efficiency substantially. This measure could also improve the number of cycles of resistive switching.

2.4 Decoupling of Ion Diffusivity and Electromobility in Porous Dielectrics

Based on the characterization results discussed above, we have found that the best resistive behavior has been observed for devices with two diffusion barriers. Also, the best resistive switching behavior has been observed for dielectrics with the highest porosity of 25%. From Table 2.2 it can be seen that dielectric materials with higher porosity have higher V_{form} voltages. Device 388-W with 25% porosity has a V_{form}= 0.89 V - 2.1 V, while device 391-W with 12% porosity has V_{form}= 0.45 V-0.50 V. This finding appears rather puzzling in view of the fact that most of the devices even of high porosity where intrinsically conductive indicating a very high degree of Cu

diffusion. Therefore, the question poses itself: why should electromigration require higher electric field for more porous materials when the Cu diffusivity appears to be as strong in 8% as in 25% porous materials? In this section, the apparent decoupling of ion diffusivity and eletromobility in porous dielectrics will be discussed.

2.4.1 Relation between Mobility and Diffusivity in Porous Materials

In nonporous materials the diffusivity D and mobility μ of charged particles is related by the Einstein relation:

$$\mu = D \cdot \frac{q}{kT} \tag{2.3}$$

where k is the Boltzmann constant, T the absolute temperature and q the charge of a migrating ion. In terms of microscopic mechanisms, diffusivity and mobility are very related phenomena as shown in Fig. 2.17. The difference between diffusion and mobility is due the applied electric field lowering the barrier for the forward jump and increasing the barrier for the reverse jump. In two and three dimensions the difference between diffusion and electromigration is that diffusion is isotropic in homogeneous materials and electromigration is directional. Thus, when the jump frequency for diffusion in all directions (assuming isotropic diffusion) is proportional to $\exp(-E_a/kT)$ (where E_a denotes the activation energy), in case of an applied field the jump parallel to the electric field Eel the effective barrier is lowered E_a-qsE_{el} and becomes proportional to $\exp(-[E_a-qsE_{el}]/2kT)$ and against the field the barrier is increased E_a+qsE_{el} and the jump frequency becomes proportional $\exp(-[E_a+qsE_{el}]/2kT)$. Here, s is the jump distance of an elementary diffusion jump and q denotes the charge of the migrating ion. Thus we have for the jump frequency in the direction of the field

$$u_+ = u_o \exp\left(-\frac{E_a}{kT}\right) \cdot \exp\left(\frac{+E_{el}}{2kT} qs\right) \tag{2.4}$$

and in the opposite direction:

$$u_{-} = u_o \exp\left(-\frac{E_a}{kT}\right) \cdot \exp\left(\frac{-E_{el}}{2kT} qs\right) \tag{2.5}$$

The net jump frequency is

$$\upsilon_{net} = \upsilon_{+} - \upsilon_{-} = 2\upsilon_o \exp\left(-\frac{E_a}{kT}\right) \cdot \sinh\left(\frac{qE_{el}s}{2kT}\right) \tag{2.6}$$

The drift velocity of ions is $v_{net} \times s$ and expressed as

$$v_{drift} = 2\upsilon_o s \exp\left(-\frac{E_a}{kT}\right) \cdot \sinh\left(\frac{qsE_{el}}{2kT}\right) \tag{2.7}$$

For electric fields sufficiently small i.e. $E_{el} < kT/qs$ the drift velocity can be written as

$$v_{drift} = E_{el} \frac{qs^2 u_o}{kT} \exp\left(-\frac{E_a}{kT}\right) \tag{2.8}$$

with mobility μ independent of the electric field E_{el}:

$$m = \frac{qs^2 u_o}{kT} \exp\left(-\frac{E_a}{kT}\right) \tag{2.9}$$

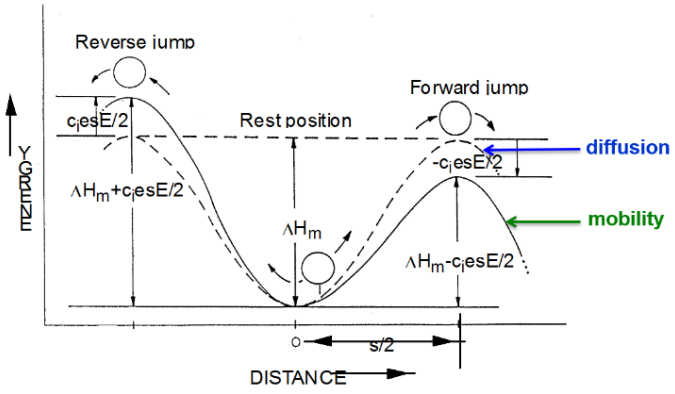


Figure 2.17 Elementary jumps in 1-D for diffusion and mobility of a charged particle in the electric field.

However, it is postulated that in porous materials the diffusivity and mobility are decoupled and the Einstein relation does not hold globally any more but only locally within contiguous material outside of the voids constituting the porosity. Nevertheless, mobility will be still proportional to diffusivity on a local as well as on global scale. A comparison of the concept of diffusion and mobility in porous media is shown in Fig. 2.18.

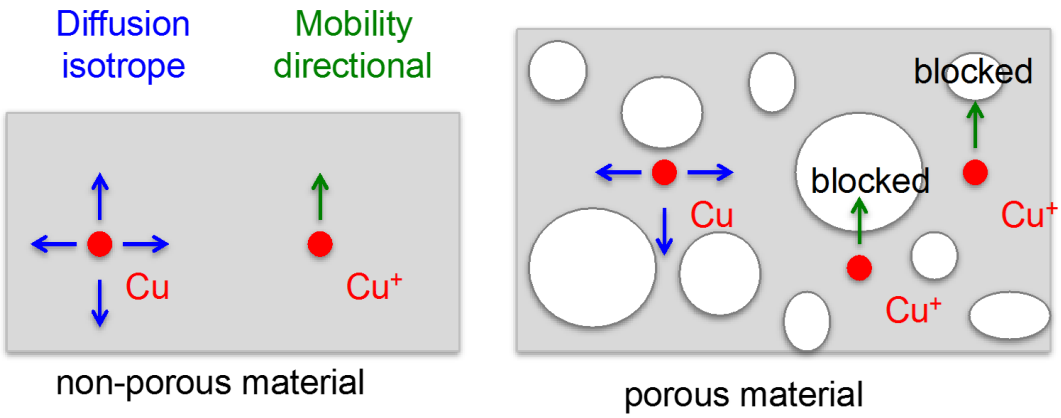


Figure 2.18 Comparison between diffusion and mobility in porous and non-porous materials.

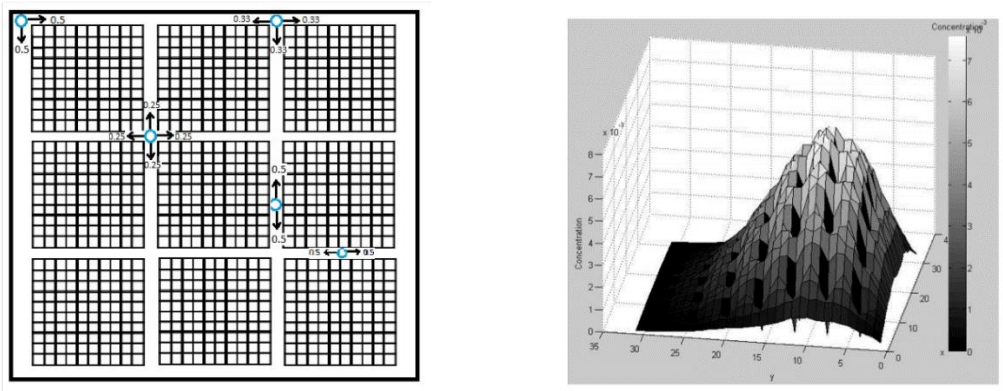
In porous materials, the voids lying in the path of the migrating ion present an impenetrable barrier for electromigration. They can be only overcome by a detour around the obstacle that can be brought about by the driving force of diffusion. It is proposed that the relation between diffusivity and mobility in porous materials can be described by a revised Einstein relation:

$$\mu = f_P \cdot D \cdot \frac{q}{kT} \quad where \quad f_P < 1 \tag{2.10}$$

The retardation factor f_p will depend on porosity, such that f_p will decrease with increasing porosity and pore morphology. In the mathematical limit of porosity of 100% the retardation factor will become zero, i.e. f_p (porosity=100%) = 0. Determining the factor f_p by means of a model for porous materials and drift-diffusion simulations is still in processing.

2.4.2 Principle of the Void Model and Drift Diffusion Simulation in 2D

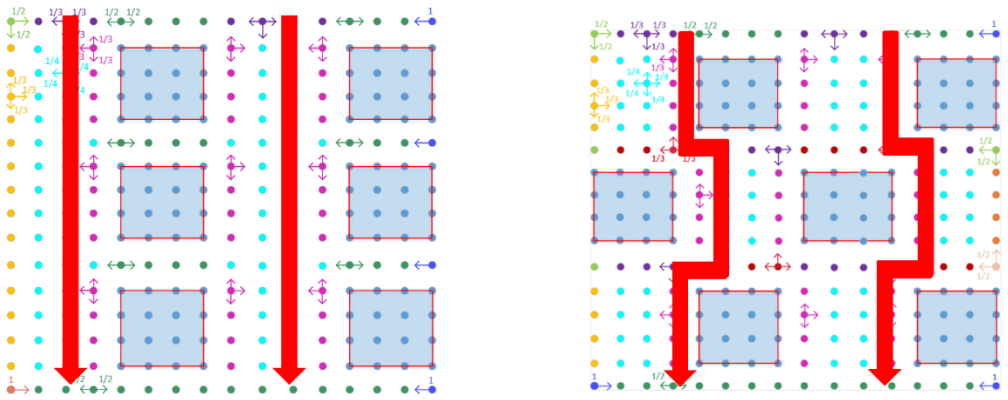
The principle of the void model and drift diffusion simulation in two-dimensions is shown in Fig. 2.19. As shown in the figure, the porosity of a material is just the percentage of void relative to the total volume of the material. In the 2D plane, the diffusion is shown according to the diagram with number indicating the respective probabilities of diffusion of a particle in a certain direction. Fig. 2.19 (a) gives a regular arrangement of large (9) voids in a 2D material cross-section. The particles are allowed to diffuse only in the spaces between the square voids. Fig. 2.19 (b) shows an example of drift-diffusion with particles starting to drift diffuse from the right under the influence of electric field pointing from right to left.



(a) (b)

Figure 2.19 (a) A regular arrangement of large (9) voids in a 2D material cross-section. (b) Example of drift-diffusion with particles starting to drift diffuse from the right under the influence of electric field pointing from right to left.

However, for the same porosity different distributions of voids are conceivable, leading to a critical assessment of the interconnectedness of the material between the voids which can be characterized by the factor of tortuosity. In Fig. 2.20 (b) the middle row of 2 voids has been shifted to block a direct path for particles drift-diffusion from top to bottom. Thus, for the same amount of porosity in the material, the way for a particle starting at the top to reach a bottom is more "tortuous" than in the case of a regular arrangement of voids as shown in Fig. 2.20 (a). Thus the factor f_p depends not only on the porosity but also on the tortuosity of the material.

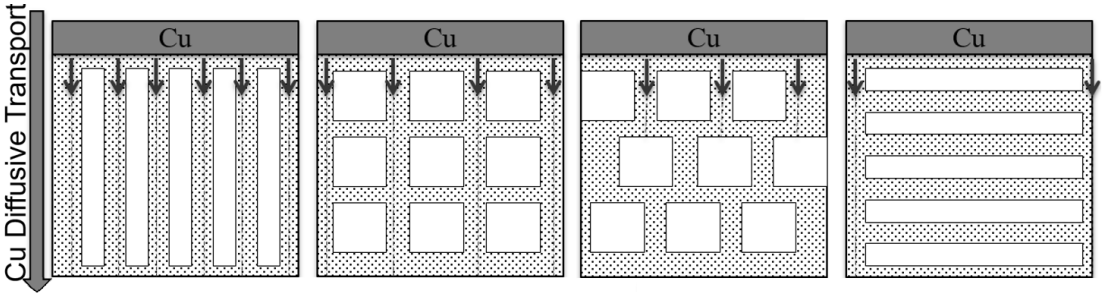


(a) (b)

Figure 2.20 (a) Regular arrangement; (b) More “tortuous” arrangement.

2.4.3 Morphology of the Voids with Different Degree of Porosity

If we consider purely diffusive transport of Cu across the dielectric for the same level of porosity of the dielectric. The arrangement of media with four different configurations are simulated and the numbers of Cu ions at the bottom electrode during same time are compared. For these four configurations of voids, the porosities are the same. Considering just purely diffusive transport, the column arrangement in Fig. 2.21 (a) is most effective, and the arrangement in Fig. 2.21 (d) is the least. These two for the diffusive transport are almost the same.



(a) (b) (c) (d)

Figure. 2.21 Purely diffusive transport of Cu across the dielectric in different arrangement of media with the same level of porosity of the dielectric.

However, in drift transport of Cu across the dielectric for the same level of porosity of the

dielectric, the shifted voids arrangement in Fig. 2.22 (d) is the least effective drift transport of Cu. The Cu ions are all blocked. So if compare the speed of Cu transport for diffusion and drift together, it can be found that: for both pure diffusion and pure drift, column arrangement is the strongest transport, for pure diffusion this is least effective. But for pure drift, the shifted voids arrangement no transport at all. In summary, diffusion transport is decoupled from drift transport in porous media. Morphology of the pores (pore size distribution) more important than porosity.

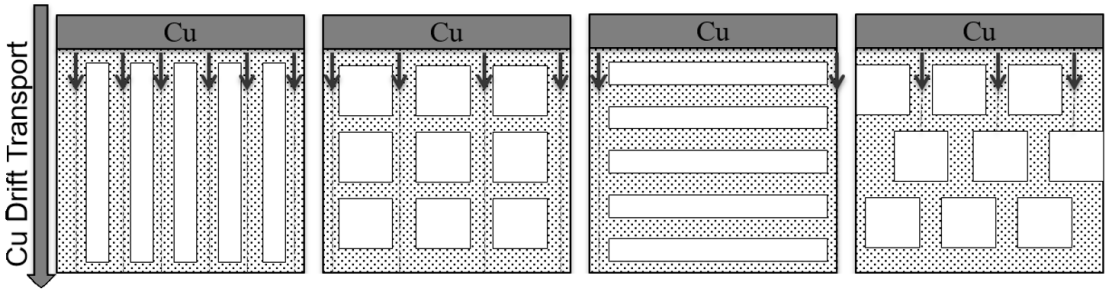


Figure 2.22 Drift transport of Cu across the dielectric in different arrangement of media with the same level of porosity of the dielectric.

Detailed simulations of pure diffusion, pure drift, and various degrees of drift-diffusion will be given elsewhere [55].

Chapter 3 Resistive Switching Comparison Between Cu/TaO_x/Ru and Cu/TaO_x/Pt Memory Cells

Building nonvolatile memory (NVM) directly into a CMOS low-k/Cu interconnect module would reduce latency in connectivity constrained computational devices and reduce chip's footprint by stacking memory on top of the logic circuits. One strong candidate for NVM is the well-behaved and well-characterized Cu/TaO_x/Pt resistive switching device. This device can be operated as a memory cell with copper (Cu) or oxygen vacancy (V_O) conductive filaments (CF). Under high electric field, Cu ions dissolve and migrate in the TaO_x layer. These cations are stopped by the inert Pt electrode and accumulate to form a Cu nanofilament, or nanobridge. When the filament connects Cu and Pt electrodes, the memory state of the device switches from high resistance to low resistance.

This chapter starts with the introduction of the fabrication process of the Cu/TaO_x/Pt and Cu/TaO_x/Ru resistive switching devices. Furthermore, the electric characterizations of these two types of devices have been discussed, which show many similarities and some notable differences.

3.1 Fabrication of Cu/TaOx/Pt and Cu/TaOx/Ru Resistive Switching Cells

3.1.1 Introduction

The RRAM is a highly promising candidate for new nonvolatile memory due to its low power consumption, high switching speed, good retention and endurance properties, and good complementary metal-oxide-semiconductor (CMOS) compatibility. These novel features of RRAM satisfy critical requirements in the replacement of NAND flash memory, which will be facing physical limitations in the near future as device sizes are scaled down. The conductive bridge RAM (CBRAM) is classified as one category of RRAM. In this cation-base device, also called electrochemical metallization memory (ECM), the metallic cation is the mobile species. The structure of CBRAM is active electrode/solid electrolyte/inert electrode, as shown in Fig. 3.1. This

simple structure allows compact integration compatibility with the BEOL of Si CMOS process.

Cu is a more preferable active electrode than Ag because Cu is used as an interconnection metal and is cost-effective. The inert electrode is usually platinum (Pt), tungsten (W), iridium (Ir), gold (Au) and Ruthenium (Ru). TaO_x is one of the most promising solid electrolyte materials because of two stable phases of TaO_2 and Ta_2O_5, which can also control the stable low- and high-resistance states [56]. Ta_2O_5 is selected in this research since it can improve the reproducibility of Cu-based CBRAM devices [57]. The oxygen-deficient Tantalum oxide TaO_x layer was deposited by evaporating the Ta_2O_5 pellets without oxygen injection into the evaporation chamber. Deposition of substoichiometric Ta_2O_x ($x < 5$) layer is a critical process in order to produce the required oxygen vacancies in these RS devices [58]. Therefore, Cu/TaO_x/Pt device is a strong candidate for non-volatile memory, which can be switched between high resistive state and low resistive state based on the formation and rupture of two types of nanofilament.

Since Pt is not an economic choice for industrial production and has been not used in BEOL, a BEOL-compatible replacement of Pt is highly desirable. A good candidate for a replacement of Pt is Ru which has been already deployed in the CMOS BEOL supplanting Ta or TaN as the liner material. Ru is about 45 times less expensive than Pt, and has similar properties as Pt. Pt and Ru are both transition metals with almost identical outer shell structure: Ru has one electron in the fifth orbital and 14 electrons in the fourth orbital, while the larger Pt atom has one electron in the sixth orbital and 15 electrons in the fifth orbital. In this research, Cu/TaO_x/Pt and Cu/TaOx/Ru devices have been manufactured in VTech clean room.

3.1.2 Devices Structures

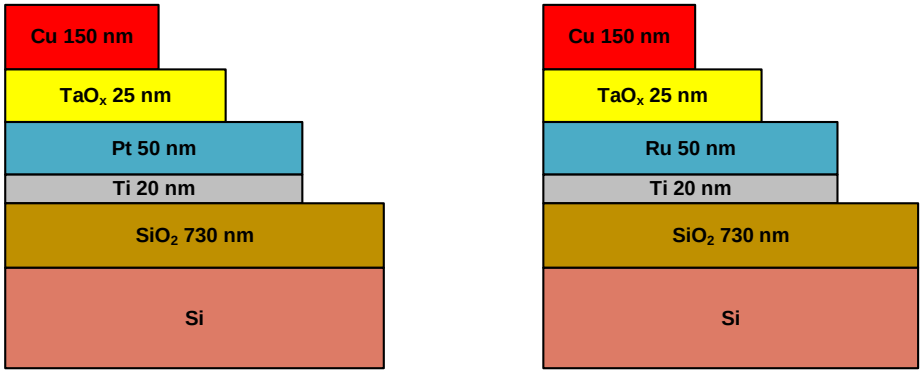
The Cu/TaO_x/Pt and Cu/TaO_x/Ru resistive switching devices mentioned above were both fabricated on silicon wafers. They were developed on 4 inches diameter silicon wafers in a crossbar array on a thermally oxidized Si wafer. The metal electrodes and the solid state electrolyte were deposited by e-beam evaporation and were patterned by lift-off technology. Samples fabricated are

given as follows:

1) Pt (50 nm)/ TaO_x (25 nm) / Cu(150 nm)

2) Ru (50 nm)/ TaO_x (25 nm) / Cu(150 nm)

The cross-section view of Cu/TaO_x/Pt device and Cu/TaO_x/Ru devices are shown in Fig. 3.1 (a) and (b) respectively. The exact thickness of each layer for the two types of devices are describes in Fig. 3.1. All four layers (Cu, TaO_x, Pt, Ru) have been deposited by e-beam PVD, with the following thicknesses 150 nm, 25 nm, 50 nm, 50 nm, respectively.



(a) (b)

Figure 3.1 Schematic layer structure of the cross section of (a) Cu/TaO_x/Pt resistive switching device; (b) Cu/TaO_x/Ru resistive switching device.

Both Cu/TaO_x/Pt and Cu/TaO_x/Ru resistive switches have a crossbar architecture that indicated in Fig. 3.2. The Cu anodes and Pt (Ru) cathodes are perpendicular to each other and one resistive switch cell locates at each cross point since it has a blanket layer of dielectric in between. The width of the metal lines varies between 5 μm and 25 μm.

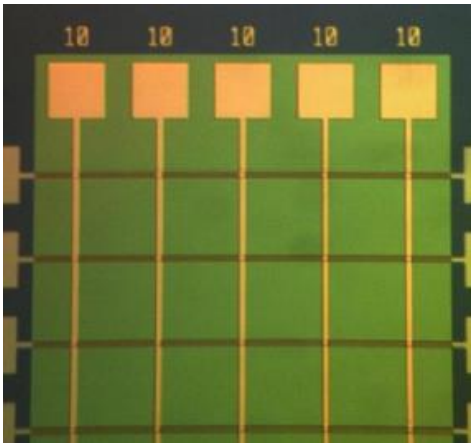


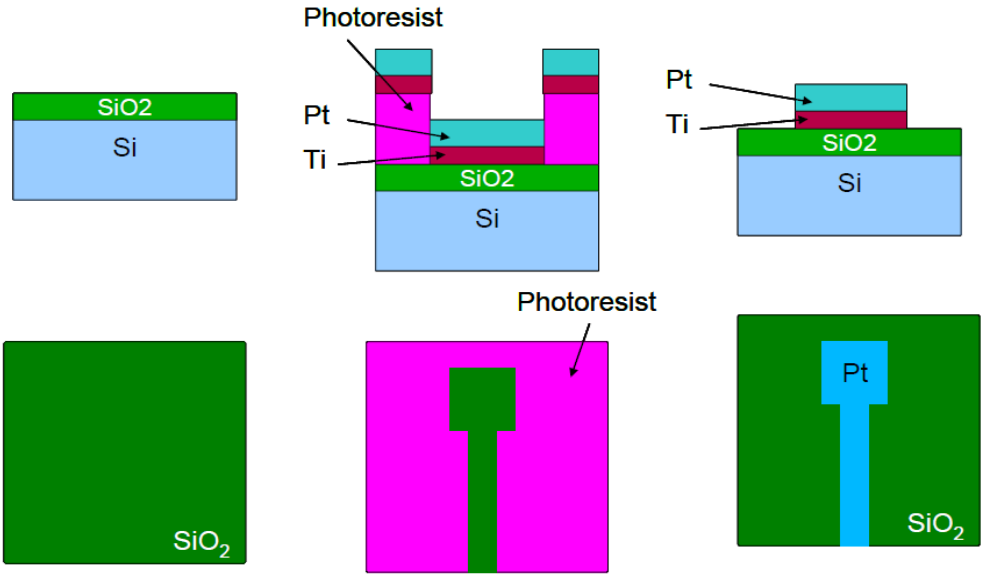
Figure 3.2 Micrograph of the crossbar architecture of the Cu/TaO_x/Pt device.

3.1.3 Fabrication Processes

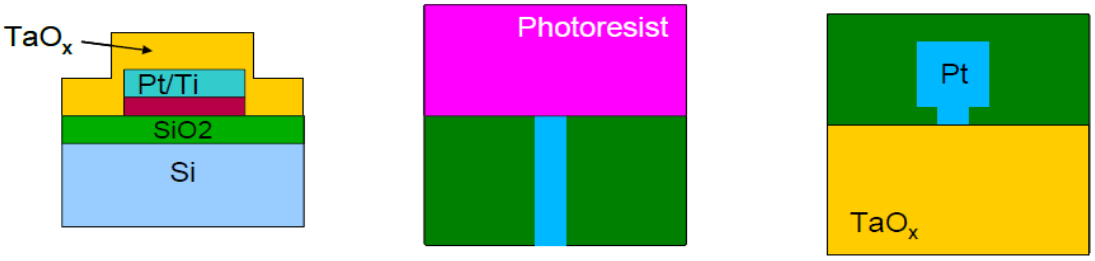
To deposit Pt/Ru/Cu layers, the process flow of lithography, e-beam evaporation and lift-off are needed to be performed. Therefore, the same process flow is repeated three times with different prerequisites and pre-conditions in order to fabricate the resistive switches which have three layers of material. In addition, a thin Ti layer (20 nm) is deposited before Pt deposition on the thermally oxidized SiO_2 for improving the adhesion of Pt. Both Cu/TaO_x/Pt devices and Cu/TaO_x/Ru devices have been fabricated on Si substrates having thermally grown oxide to improve adhesion. The Cu anode is the finish layer exposed to the air and moisture. A detailed review of the process flow as well the various optimizations applied to each of the process steps for the different devices will be discussed in this section.

The fabrication process flow of Cu/TaO_x/Pt device is shown in Fig. 3.3. Cu/TaO_x/Pt device and Cu/TaO_x/Ru device are fabricated at the same time. The only difference in the process flow of Cu/TaO_x/Ru device is replacing the Pt/Ti E-beam evaporation and Pt/Ti lift-off by Ru/Ti E-beam evaporation and Ru/Ti lift-off.

(1) Oxidation SiO_2 (2) Pt/Ti E-Beam Evaporation (3) Pt/Ti Lift-Off



(4) TaO_x E-beam Deposition (PVD)



(5) Cu PVD & Lift-OFF

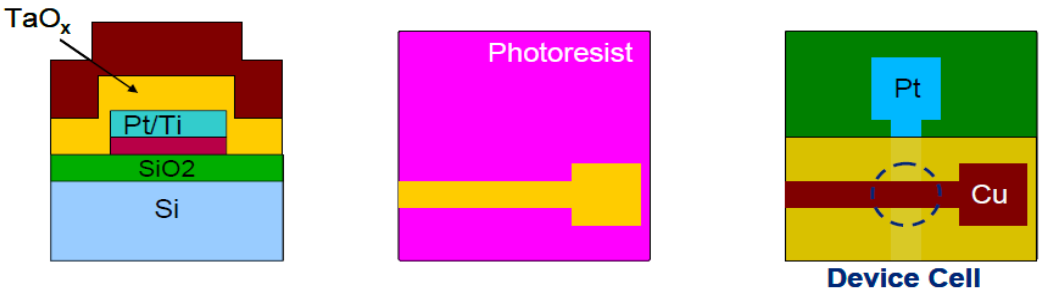


Figure 3.3 Process flow of Cu/TaO_x/Pt conductive bridge resistive devices. (1) Thermal oxidation of Si substrate. (2) Lithography and Pt/Ti e-beam evaporation. (3) Pt/Ti lift-off. (4) Lithography, TaO_x e-beam deposition, and TaO_x lift-off. (5) Lithography, Cu e-beam deposition, and Cu lift-off. [59]

(1) Wafer surface preparation and cleaning

In the manufacturing of key semiconductor devices, it is extremely important to reduce, as much as possible, the particle, metallic, organic, and other contamination that occurs in the manufacturing process. If left on the wafer surface, these contaminants can lead to serious problems during processing, like compromising wafer planarity during lithography, creating unperfected adhesion of the resist on the wafer surface, or provoking unwanted chemical reactions. Thus, the substrate (wafer) cleaning has become a critical process and a preliminary wafer cleaning is also needed at the beginning of every lithography process.

Both wet and dry cleaning procedures are used in the fabrication process. In wet cleaning, solvent and acids are used to dissolve the contaminate by converting it into a soluble compound and wash it off by force. The solvents used in wet cleaning commonly are acetone, IPA (isoprogyl alcohol) and DI (Deionized) water, which are used in sequence. Any solvent clean of silicon wafers is always followed by a DI water rinse, blowing drying using a nitrogen gun subsequently and then a dehydration bake. Dry cleaning processes use gas phase chemistry, and rely on chemical reactions required for wafer cleaning. Generally, dry cleaning technologies use less chemicals and less hazardous for environment but usually do not perform as well as wet methods, especially for particle removal.

(2) Thermal Oxidation

The Si substrate is thermally oxidized to provide an insulating SiO_2 layer as the foundation of resistive devices. The standard dry O_2/wet O_2/dry O_2 oxidation process is used in a thermal oxidation furnace. The first step is turning on the boiler with setting initially to 75°C and ramping slowly to avoid overshooting the desired temperature of 94-96°C. After turning on heat tape by setting toggle to 120 V, the temperature of furnace is ramped slowly up to 600°C by the center controller which is then followed by loading wafers into quatz wafer boat. It is made sure that the wafers to be oxidized into the boat are placed at evenly space distances and all surfaces to be

oxidized should face towards the rear of the furnace with the float of the wafer up. During the phase of temperature of the furnace ramps up to 1050 °C, the nitrogen purge will remain on until the oxidation is started. Once the furnace has reached 1050 °C, the oxygen flow is turned on with 1 liter/min rate and the dry oxidation runs for 5 minutes subsequently. After performing the initial dry oxidation, the wet oxidation begins with a reduced oxygen flow rate of 0.5-0.7 liters/min. It is important to notice that removing condensation from quartz nipple periodically by increasing the oxygen flow rate and then returning to normal flow rate (0.5-0.7 liters/min) is needed. Once we oxidation has been finished, the dry oxidation reruns for 5 minutes with 1 liter/min rate. Finally, the oxygen flow and nitrogen flow are turned off and the temperature of furnace is ramped down slowly to 80 °C (the temperature the furnace keeps at). Based on the Deal-Grove model of the rate of oxide growth [60], the 700 nm -750 nm of silicon dioxide deposited on the silicon at a furnace temperature of 1050 °C takes around 2 hours to complete.

(3) Photolithography

The thermal oxidation is followed by bottom electrode lithography. The photoresist consists of three components: a base material (resin), a photoactive compound (PAC) and a solvent. The solvent controls the mechanical properties of the PR. It is what makes the photoresist liquid, and also controls the viscosity. The PAC inhibits the dissolution rate in developer before exposure to UV light. However, after exposure to UV light it makes the photoresist highly soluble in developer. Cleaning the sample is very important to make sure that it is free from dust and dirt. Dehydration baking will ensure that any H_2O on the sample evaporates out. This is especially important for samples that oxidize easily (Silicon, for example). The oxides will then bond to water vapor available in the air. When the photoresist is then spin coated onto the sample, the photoresist will adhere to the H_2O and not to the sample. Prebaking makes the photoresist sensitive to UV light by removing the solvent component of the photoresist. Because the solvent is now mostly removed, the thickness of the photoresist is usually decreased by about 25 %. A short prebake will prevent UV light from reaching the PAC due to an excess of solvent remaining in the photoresist [61].

The next step is exposing the sample to UV light, using a mask to create both exposed and unexposed portions of photoresist. The areas that are exposed to the UV light will undergo a chemical reaction. The mask aligner MA-6 Karl Suss has been used for all the photolithographic processing of Cu/TaO_x/Pt and Cu/TaO_x/Ru devices fabrication. It can achieve the best resolution of 1 μm. Therefore, the dimensions of resistive devices are in μm range which is still suitable for demonstrating the generic device characteristics. Considering the requirement of lift-off, negative lithography is employed for defining the device active region. Fig. 3.4 gives the technique for both positive and negative lithography.

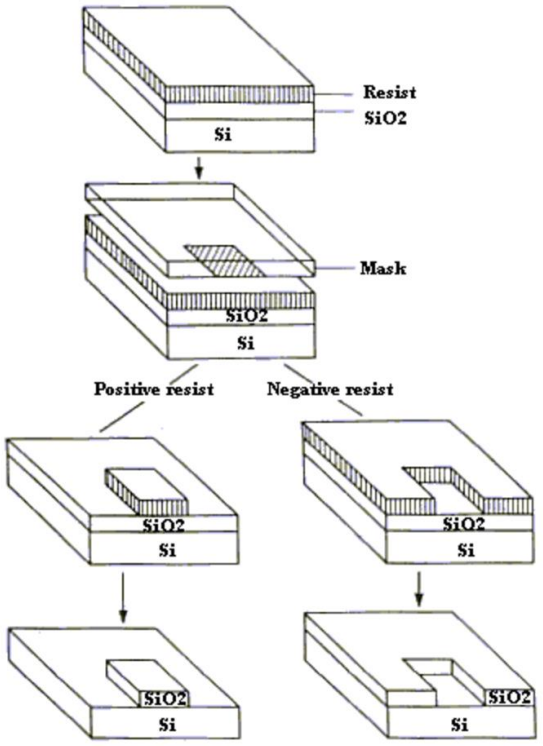


Figure 3.4 Schematic diagram of positive and negative lithography. [62]

A quartz photomask has been used in the photolithographic, as is shown in Fig. 3.5. To fabricate the Cu/TaO_x/Pt and Cu/TaO_x/Ru devices, each require three different mask pattern for bottom electrode (Pt/Ru), the solid electrolyte (TaO_x) and the top electrode (Cu) individually. This photomask comprises 4 mask patterns and 3 out of which are used to fabricate the Pt and Ru

devices. The mask on the top of the catalogue is used for patterning the bottom electrode. The mask on the right side is used for patterning the solid electrolyte and the one on the left is used for patterning the top electrode. Thus, for the bottom electrode, electrolyte and top electrode lithography, the mask is rotated by 90° and placed on the mask holder. The feature size on the mask ranges from 5 μm to 25 μm.

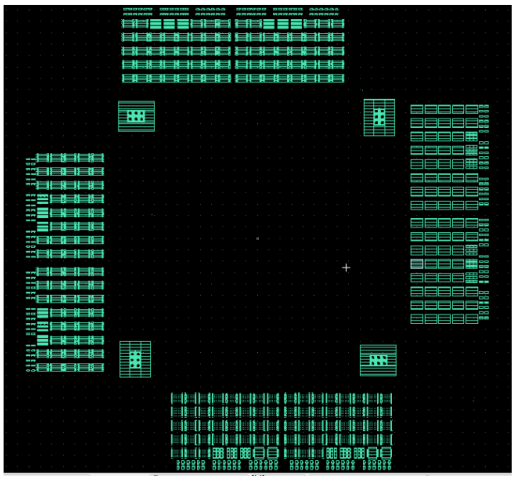


Figure 3.5 Quartz photomask of fabricating Cu/TaO_x/Pt and Cu/TaO_x/Ru devices. [63]

(4) Physical Vapor Deposition

The Physical Vapor Deposition (PVD) uses physical process (such as heating or sputtering) to produce a vapor of material. The PVD tool used in VTech cleanroom facility is the Kurt Lesker PVD 250. The electron beam (e-beam) evaporation is selected as the deposition method for Pt, Ru, TaO_x, Cu and Ti layers. The melting points of those five materials fare not high so that e-beam deposition is an effective way for manufacturing prototypes. The melting temperature for Ru of 2250 °C is higher compared with 1768 °C for Pt.

Fig. 3.6 illustrates the schematic diagram of the electron beam deposition. The deposited material is melted in the crucible at the bottom of the chamber. The electron beam is generated from a tungsten filament and reflect to the graphite crucible. This thermal energy reaching on the surface of source material sufficiently melts and evaporates the material to the above wafer. The

vacuum pump keeps the PVD chamber under low pressure. The substrate platen rotates constantly at 5 rounds/min during the deposition to improve the thickness uniformity of the deposited film. The deposition rates and parameters of Ti, Pt, Ru, TaO_x and Cu are listed in Table 3.1. The deposition rates are measured by quartz crystal microbalance in PVD, the Filmetrics F20 optical system, and the Dektak profiler.

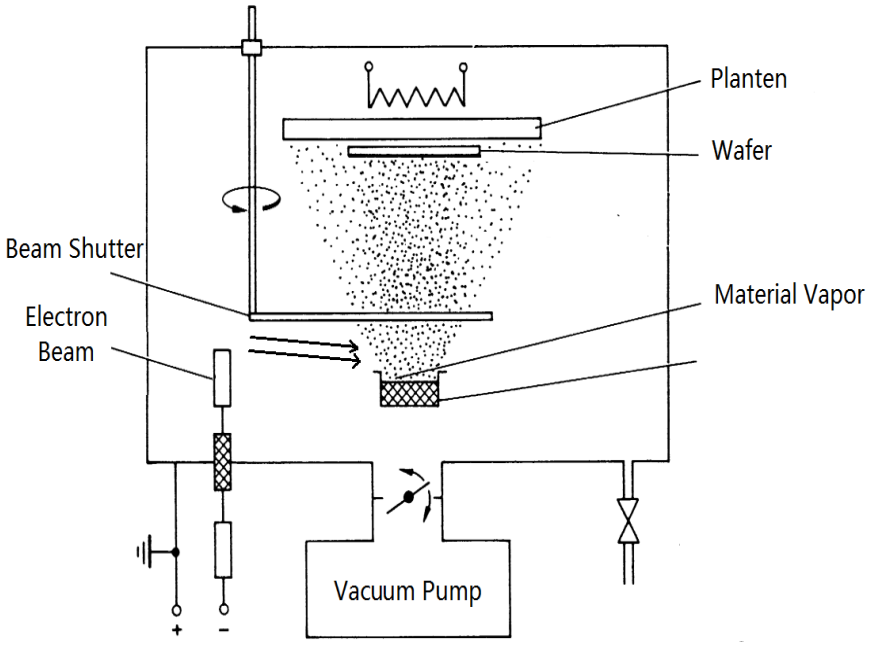


Figure 3.6 Schematic illustration of the electron beam deposition.

Table 3.1 Summary of electron beam deposition for Cu/TaO_x/Pt and Cu/TaO_x/Ru devices					
Material	Ti	Pt	Ru	TaO_x	Cu
Layer Thickness (nm)	20	50	50	25	150
E-Beam Deposition Rate (A/s)	0.3	0.2	0.6	2.3	3
Melting Temperature (°C)	1668	1768	2250	1872	1085
E-Beam Current (mA)	95	200	330	94	130
E-Beam Base Pressure (Torr)	2×10^{-6}	2×10^{-6}	2×10^{-6}	2×10^{-6}	2×10^{-6}
Density (g/cm^3)	4.43	21.45	12.3	8.2	8.93
Z-ratio	0.628	0.245	0.182	0.3	0.437
Tooling Factor	140	140	140	140	140

(5) Lift Off

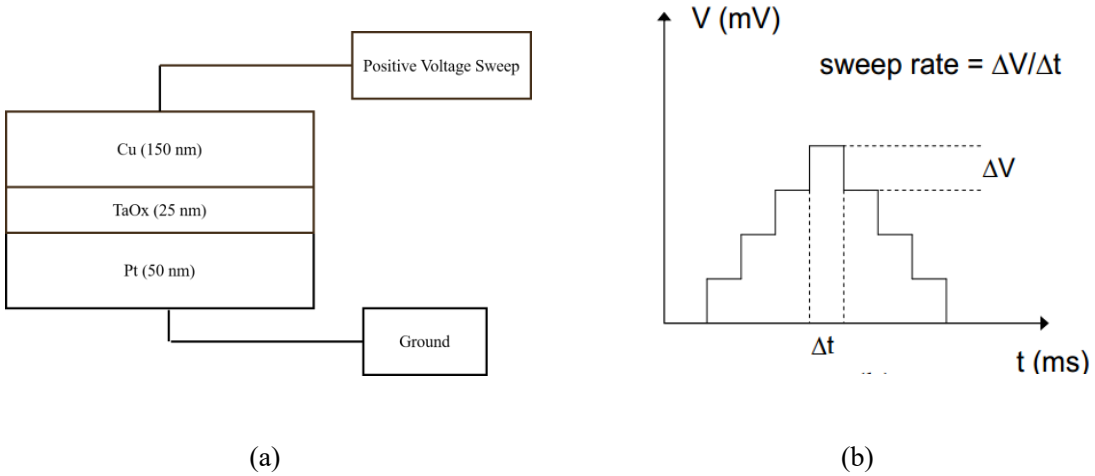
The lift-off technology is used for removing excessive materials and patterning the active region. In both Cu/TaO_x/Pt and Cu/TaO_x/Ru devices fabrication, three times of lift-off technology are performed to remove the excessive Pt/Ru, TaO_x and Cu. Acetone has been used as the liftoff solvent. The lift off of Pt, Ru and TaO_x is much easier than Cu which the former takes 3-4 minutes and the later takes 5-6 minutes.

3.2 Switching Characteristics of Cu/TaO_x/Ru and Cu/TaO_x/Pt Devices

3.2.1 Switching Characteristics of Cu/TaO_x/Pt Devices

For the purpose of electrical characterization, the Keithley 4200–SCS (Semiconductor Characterization System) has been used to test the I-V characterization of Cu/TaO_x/Pt devices. The two most important parameters of the characterization circuit are the sweep rate and compliance

current. Sweep rate is defined as the rate of change of voltage with time. The devices are stressed with a linear ramp voltage having a natural interval time of 50ms per step size. In other words, if the devices have a sweep rate of 0.01V step size, it essentially means that the sweep rate is 0.2V/s. The experimental set-up for Cu/TaO_x/Pt device is represented in Fig. 3.7 (a) and a dual sweep rate to trace the current with respect to voltage as given in Fig. 3.7 (b).



(a) (b)

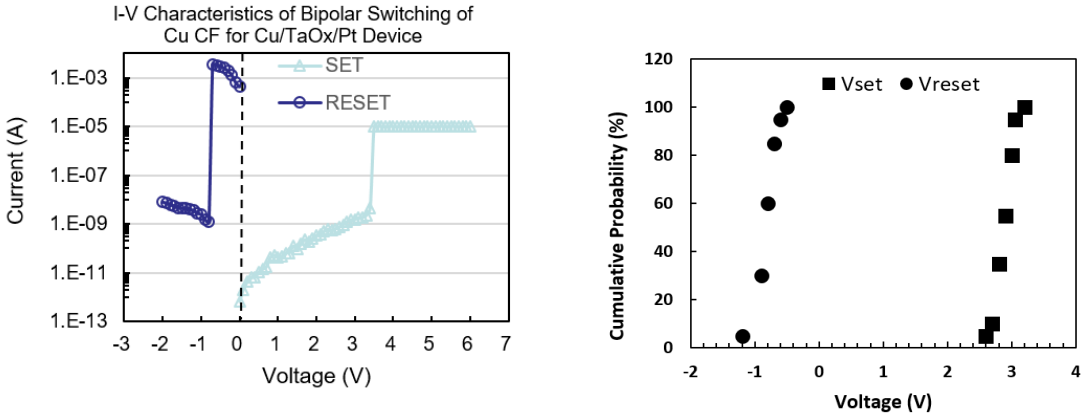
Figure 3.7 Experimental Set –Up (a) Cross sectional view of Cu/TaO_x/Pt nonvolatile memory devices; (b) Schematic illustration of voltage sweeping mode in DC characterization.

In the measurement, the bottom electrode is grounded and the bias voltage is applied to the top electrode as shown in Fig. 3.7 (a). When a positive voltage is applied to the active electrode, Cu cations dissolve in the solid electrolyte and migrate through it. Cu cations are electrochemically reduced on the Pt cathode. As more Cu atoms aggregate at the TaOx/Pt interface, a nanoscale conductive filament forms a conductive path between two electrodes. Table 3.2 gives the range of forming voltages and LRS (R_{on}) of CFs for different Cu/TaO_x/Pt devices under I_{cc} = 10 μA and voltage sweep rate rr = 2 V/s. The range of V_{form} is 4.1 V – 5.2 V.

Table 3.2 Typical forming voltage and On-resistance of $Cu/TaO_x/Pt$ devices.

	V_{from} (V)	R_{on} (Ω)
Sample 1	5.2	14,030
Sample 2	4.7	12,294
Sample 3	4.1	13,460
Sample 4	5.1	15,814
Sample 5	4.5	11,367

The state transition from HRS to LRS is called SET process characterized by a critical voltage V_{set}. A high current passing through the filament can rupture the bridge and restore HRS. This is called RESET process of the device characterized by a critical voltage V_{reset}. A $Cu/TaO_x/Pt$ device can be switched between the HRS and LRS based on the formation and rupture of two types of nanofilaments in the same device: Cu and oxygen vacancy conductive bridges based on the polarity of switching voltage. Fig. 3.8 (a) shows the bipolar switching by the Cu filament in $Cu/TaO_x/Pt$ device. The bipolar switching cycles have been repeated on $Cu/TaO_x/Pt$ devices. Fig. 3.8 (b) shows the statistical V_{set} and V_{reset} distributions of a single $Cu/TaO_x/Pt$ device with Cu CFs. It can be seen that for $Cu/TaO_x/Pt$ device the V_{set} is in the range of 2.6 V – 3.2 V and the $|V_{reset}|$ is in the range of 0.5 V – 1.21V.



(a) (b)

Figure 3.8 (a) I-V characteristics of bipolar switching of Cu CF; (b) V_{set} and V_{reset} distributions of Cu/TaO_x/Pt devices. The SET voltage is positive for Cu CFs.

Most of our fabricated Cu/TaO_x/Pt devices have good resistive switching behavior and the switching cycles of the Pt device are more than 20 times.

Fig. 3.9 shows SET voltage depends on RESET voltage. The subsequent V_{set} increases with the increase in the preceding $|V_{reset}|$. The conditions for the set operation are: I_{cc} = 10 uA and voltage sweep rate rr = 2 V/s, and the corresponding conditions for the reset operation are: rr = 2 V/s and no current limitation.

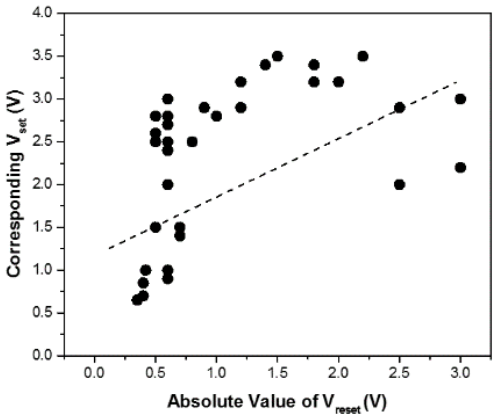


Figure 3.9 SET voltage depends on RESET voltage of Cu/TaO_x/Pt device.

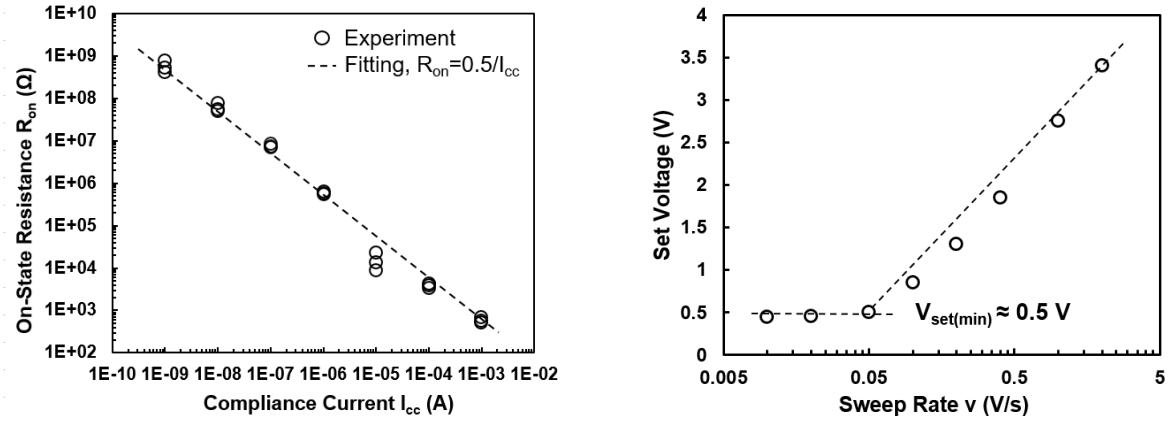
Once the metallic nanofilament connects the two electrodes, it will grow laterally to increase the diameter and reduce the resistance. This can be controlled by application of higher I_{cc}. When different levels of compliance current (I_{cc}) are applied to a CBRAM device, a characteristic dependence of LRS resistance (R_{on}) on I_{cc} is observed. The dependence of R_{on} on the compliance current is shown in Fig. 3.10 (a).

The $R_{on} - I_{cc}$ relation in following equation has been reported to be valid for numerous anode/electrolyte/cathode material systems [64].

$$R_{on} = \frac{K}{{I_{cc}}^n} \tag{3.1}$$

Where, n is a fitting parameter close to 1 for metallic CFs and K is a constant in units of volt. Based on the results in [65], it has been shown that the constant K in equation 3.1 is universally correlated to the minimum SET voltage ($V_{set(min)}$) for all metallic CFs reported so far. In Fig. 3.10 (a), voltage constant K is 0.5 V and exponent parameter n = 1 are obtained by curve fitting. The voltage sweep rate rr = 0.2 V/s is used for the set operation.

$V_{set(min)}$, required to switch the memory from off-state to on-state, can be extracted from V_{set} measurements at small voltage sweep rates. In Fig. 10 (b) the set voltage V_{set} as a function of ramp rate is plotted. The V_{set} decreases linearly with decreasing rate up to 0.05V/s and then stays constant at V_{set} =0.5 V. The minimum SET voltage is 0.5 V, which is same value of constant K.

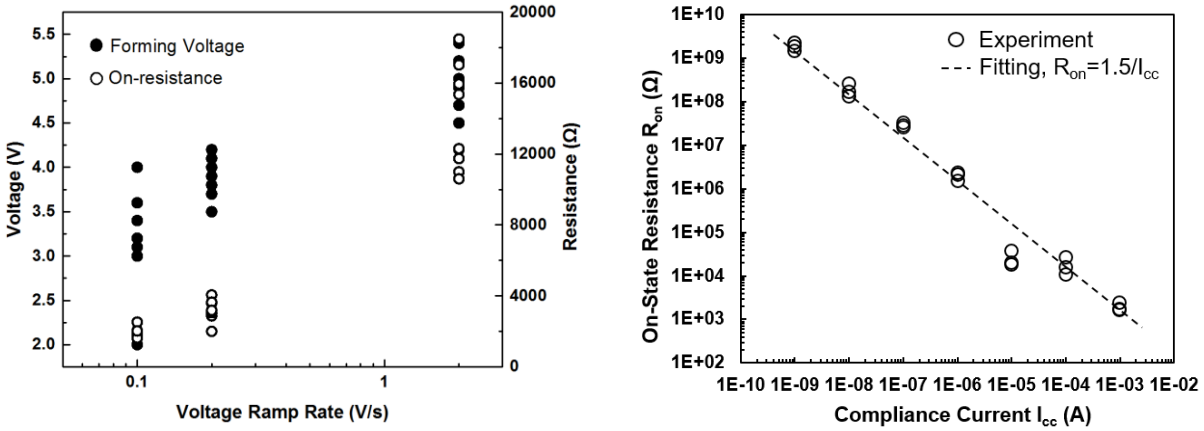


(a) (b)

Figure 3.10 (a) Dependence of on-resistance on compliance current for Cu/TaO_x/Pt device (rr =0.2 V/s); (b) Dependence of SET voltage on voltage sweep rate for the Cu/TaO_x/Pt device (I_{cc} = 100 μA).

Fig. 3.11(a) shows the dependence of forming voltage and on-resistance as a function of the sweep rates (0.1 V/s, 0.2 V/s and 2V/s). It was observed that at sufficiently small ramp rates rr=0.1V/s and below the R_{on} is independent of the ramp rate, but at higher ramp rates it increases with the ramp rate. The dispersion of R_{on} at high ramp rate is significant higher than at low ramp rates. Thus in addition, to the R_{on} dependence on I_{cc} (see eq.(3.1)) there is also dependence on high voltage sweep rate. When the dependence of R_{on} and I_{cc} is measured again but now at ten times higher ramp rate than in Fig. 11 (b) (i.e. 0.2 V/s → 2V/s), we obtain a dependence of R_{on} on I_{cc}

conforming with eq.(1) but with a significantly higher constant K: K=0.5V for rr=0.2V/s and K=1.5V for rr=2.0 V/s.



(a) (b)

Figure 3.11 (a) Dependence of Form voltage and on-resistance on voltage sweep rate (I_{cc} = 100 μA); (b) Dependence of R_{on} on I_{cc} for the Cu/TaO_x/Pt device (rr = 2 V/s).

Fig 3.12 depicts the dependence of R_{on} on voltage sweep rate under different levels of compliance current (5 μA, 100 μA and 1 mA). The range of voltage ramp rate is 0.1 V/s to 2 V/s. Obviously, it can be seen that R_{on} is larger at lower I_{cc}, which can be illustrated by Eq. (3.1). Under low compliance current (5 μA and 100 μA), R_{on} increases with increasing voltage sweep rate. However, in the case of high compliance current, R_{on} becomes independent with voltage ramp rate. It is possibly because the resistance of Cu CF is too small under high compliance current so that the voltage ramp rate will not introduce dominant influence on R_{on}.

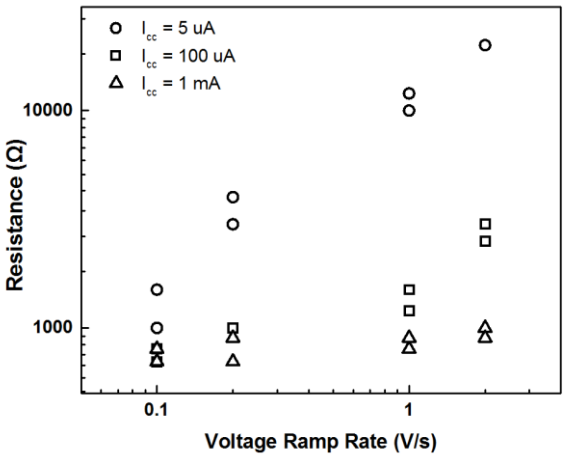


Figure 3.12 Dependence of on-resistance on voltage sweep rate (I_{cc} = 5 μA, 100 μA and 1 mA).

Fig. 3.13 illustrates the SET voltage is dependent on ambient temperature while the RESET voltage is almost independent on ambient temperature. V_{set} and V_{reset} of five different cells are plotted when the ambient temperature is 20 °C, subsequently increases to 85 °C and reduces back to 20 °C. It can be seen that the SET voltage at 85 °C is reduced by ~ 0.8 V compared with the set voltages at room temperature. The reduction of V_{set} with increasing temperature can be explained by three different mechanisms in TaO_x. (1) The ionization rate of Cu, the rate for Cu ionizes to Cu ion ($Cu \rightarrow Cu^+ + e^-$), is higher at high temperature. (2) The mobility of Cu ions in TaOx increases with increasing temperature. (3) The nucleation of Cu ions or the speed of forming the cluster of Cu at the interface of Pt electrode may accelerate also with increasing temperature, since all of those reactions are governed by Arrhenius law. However, the RESET voltage is independent with temperature. At the reset operation, commonly 500 °C at the top of conical shaped Cu CF is needed to rupture the Cu CF by Joules heating. Even if the ambient temperature increases from 20 °C to 85 °C, the increased ambient temperature of 85 C in the Cu CF is still well below 500 °C. Same reset voltages are still needed to reach to the required temperature (500 °C). Therefore, the reset voltage will be not affected much by the ambient temperature. Moreover, according to the Fig. 3.13, it can be observed that V_{set} has larger statistical range at 85 °C. This may be caused by

increased diffusion of Cu atoms at the Pt-TaO_x interface as well as random motion of Cu in the dielectric at 85 °C.

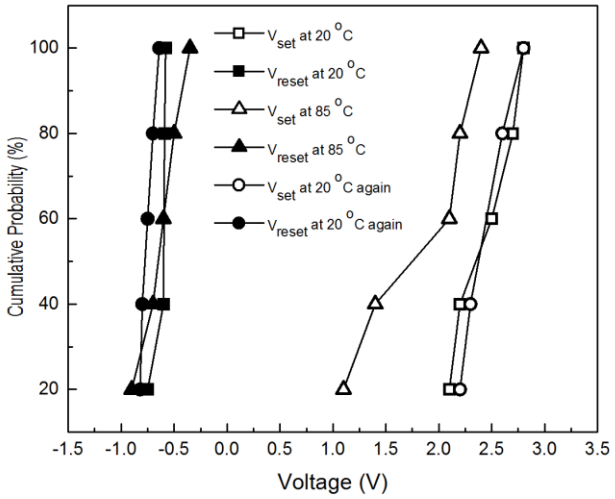


Figure 3.13 Dependence of V_{set} and Independence of V_{reset} on ambient temperature.

The current in the set operation would be slightly reduced at 85 °C because this metallic Cu CF so that the on-resistance will increases with temperature, as is shown in Fig. 3.14. Whereas, R_{off} slightly reduces with the increasing temperature due to more frequent electron hopping.

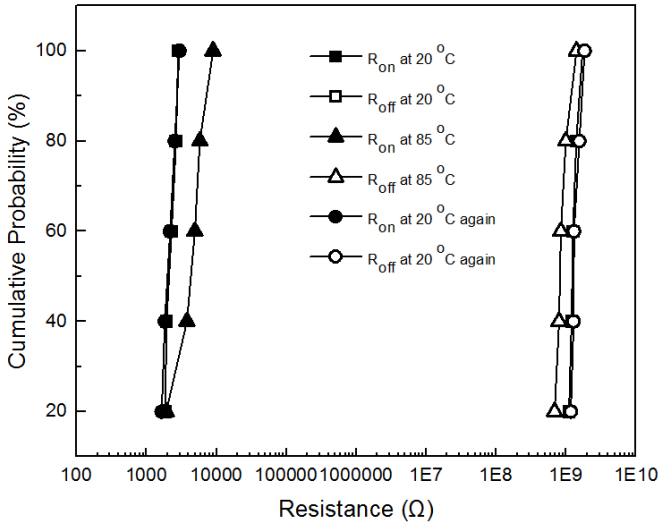
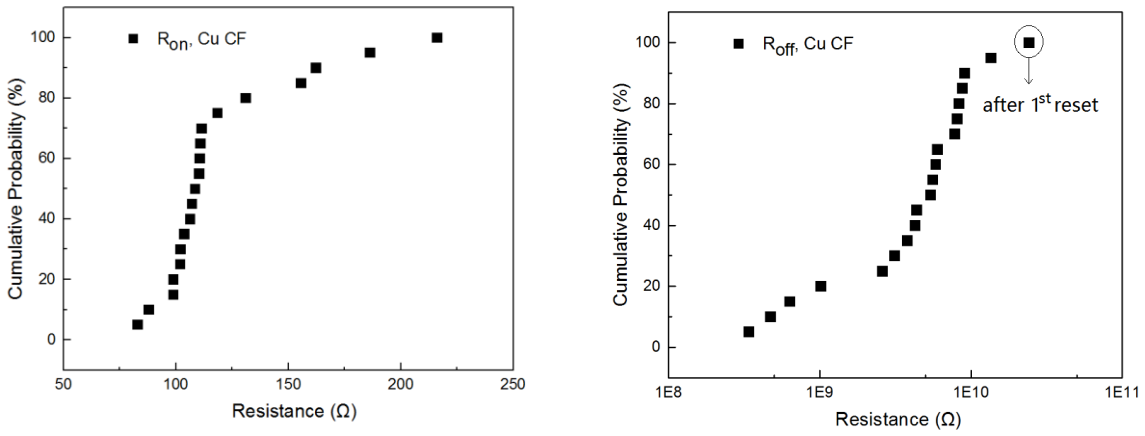


Figure 3.14 Dependence R_{on} at the SET operation and R_{off} at RESTET operation on temperature.

Figure 3.15 (a) and (b) show the distribution of R_{on} at the SET operation and R_{off} at RESET operation for Cu/TaO_x/Pt device respectively. The set and reset values have been taken from the same Cu/TaO_x/Pt device. In Fig. 4.15 (a), the value of R_{on} is not related to the sequence of SET operation and appears to be statistically distributed. In Fig. 4.15 (b), the highest value of R_{off} is obtained after the first reset operation and it is circled in the figure. The rest R_{off} distribution is also not related to the sequence of RESET operation.

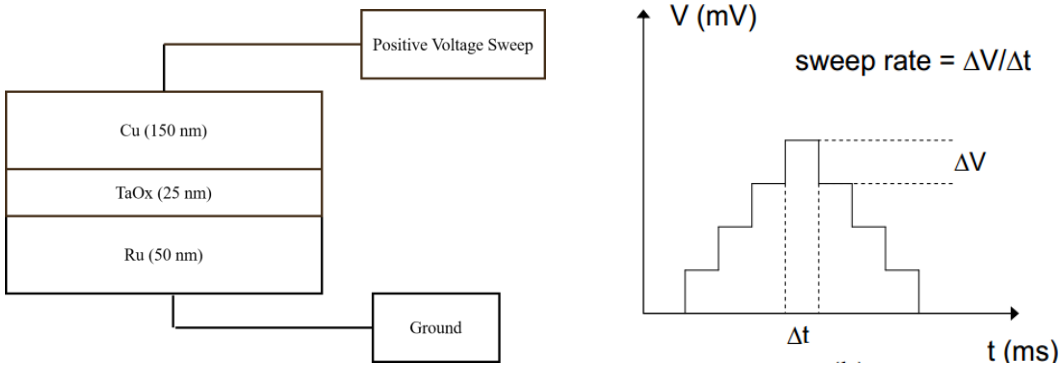


(a) (b)

Figure 3.15 Distribution of (a) R_{on} at the SET operation and (b) R_{off} at RESTET operation.

3.2.2 Switching Characteristics of Cu/TaO_x/Ru Devices

The experimental set-up for Cu/TaO_x/Ru device is represented in Fig. 3.16 (a) and a dual sweep rate to trace the current with respect to voltage as given in Fig. 3.16 (b).



(a) (b)

Fig. 3.16 Experimental Set –Up (a) Cross sectional view of $Cu/TaO_x/Ru$ nonvolatile memory devices; (b)Schematic illustration of voltage sweeping mode in DC characterization.

Table 3.3 gives the range of Form voltages and LRS (R_{on}) of CFs for different $Cu/TaO_x/Ru$ devices under I_{cc} = 10 μA and voltage sweep rate rr = 2 V/s. The range of V_{form} is 6.9 V – 7.8 V. Compared with Pt devices, Ru devices have higher forming voltages while the on-resistances are comparable. Compared with Pt devices, Ru devices have significantly higher forming voltage (by 2.0 – 2.5V) while the on-resistance is very similar and appears to be controlled only by the compliance current. This cannot be explained by the difference of the work function differences $\Delta\phi$(Pt-Cu) ≈1.3 eV and $\Delta\phi$(Ru-Cu)≈ 0.2 eV.

Table 3.3 Typical forming voltage and On-resistance of $Cu/TaO_x/Ru$ devices.

	V_{from} (V)	R_{on} (Ω)
Sample 1	7.6	15,432
Sample 2	7.5	12,050
Sample 3	6.9	13,260
Sample 4	7.8	10,868
Sample 5	7.2	11,845

In Fig. 3.17, a typical set and reset bipolar operation for Cu CF in $Cu/TaO_x/Ru$ device is shown. The V_{set} = 3.5 V at I_{cc} = 10 μA and V_{reset} = -3 V. The bipolar switching cycles have been repeated on $Cu/TaO_x/Ru$ devices.

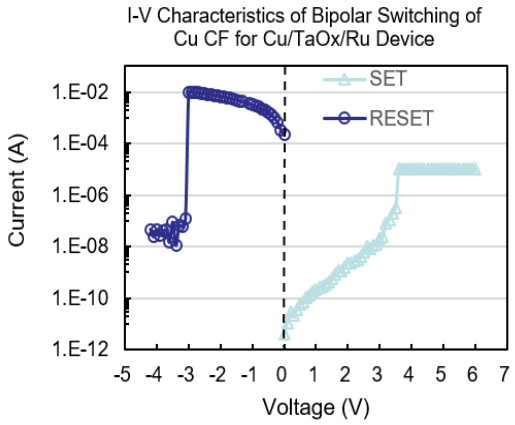


Figure 3.17 The bipolar switching by the Cu filament in Cu/TaO_x/Ru device.

Most of our Cu/TaO_x/Ru devices are becoming not resettable after a few set-reset operations. The failure of the Ru devices after a few switching cycles is likely to be related to the geometrical shape of the Cu filament.

Overall, the V_{set} values for Ru devices range from 3.8V to 5.0V significantly higher than the V_{set} values for Pt devices (3.1V – 3.4V) as shown in Fig. 3.8(b). Even higher in magnitude are V_{reset} values for Ru devices on those few devices that were resettable. The range of $|V_{reset}|$ values for Ru devices is 3.1 V – 3.8 V compared with a range of 0.6V-1.0V for Pt devices. Thus while it is more difficult to set a Ru device than a Pt device, the rupturing of the filament in Ru device is even more difficult or impossible (i.e. the device cannot be reset).

To inquire more into the nature of the filament formation in Ru devices, we have measured Ron dependence on I_{cc}. On a double logarithmic scale, on can see that R_{on} also decreases linearly with I_{cc} based on the eq. (3.1). As is shown in Fig. 3.18, the extracted parameters are K = 2 V and n = 1. The condition for the set operation is: voltage sweep rate rr = 0.2 V/s. It can be concluded that Cu/TaO_x/Ru devices has slightly higher constant K value than Cu/TaO_x/Pt device when the set operation is the same (rr = 0.2 V/s). As shown elsewhere with the exponent of I_{cc} in the denominator being close to 1, the constants 0.5 V and 2 V can be interpreted as the lowest possible V_{set} voltages under which the Pt device and Ru device can be set. This usually can be reached as a

limiting case for very slow voltage ramp rates. The difference in the minimum set voltage extracted from R_{on} - I_{cc} characteristics confirms that the V_{set} voltage for Ru devices is higher than for Cu device.

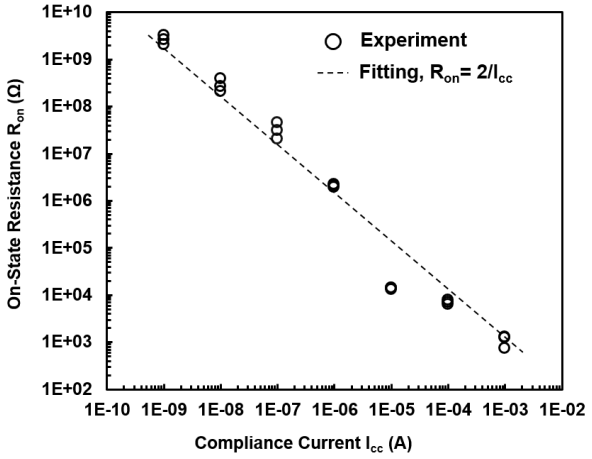


Figure 3.18 Dependence of R_{on} on I_{cc} for the Cu/TaO_x/Ru device.

It has been inquired as to the nature of the Cu filament in both devices by measuring the temperature coefficient of resistance (TCR); In Fig. 3.19 (a) and (b), it is found TCR (Ru-device) = 0.00236 K^{-1} and TCR(Pt-device) = 0.00235 K-1 at the same set conditions I_{cc}=10 μA for similar values of R_{on} which, within the accuracy of our measurement, means that the values are identical. Therefore, it can be concluded that under a positive voltage stress applied to the Cu electrode, Cu conductive filaments are formed in both devices. Same measurements have been repeated for a different set conditions at three orders of magnitude higher I_{cc}, I_{cc}=10mA. For I_{cc}=10mA we obtain much lower R_{on} for the filaments 510 Ω for Ru and 230 Ω for the Pt device. The results of the resistance as a function of temperature are shown in Fig. 3.19 (c) and (d). For both devices very similar TCR values are extracted: TCR (Ru)=0.0035 K^{-1} and TCR(Pt)=0.0036 K^{-1}. These values are typical of strong Cu filaments (for comparison the TCR of bulk Cu is 0.0039-0.004 K^{-1}). Therefore, we conclude that under a positive voltage stress applied to the Cu electrode, Cu conductive filaments are formed in both devices.

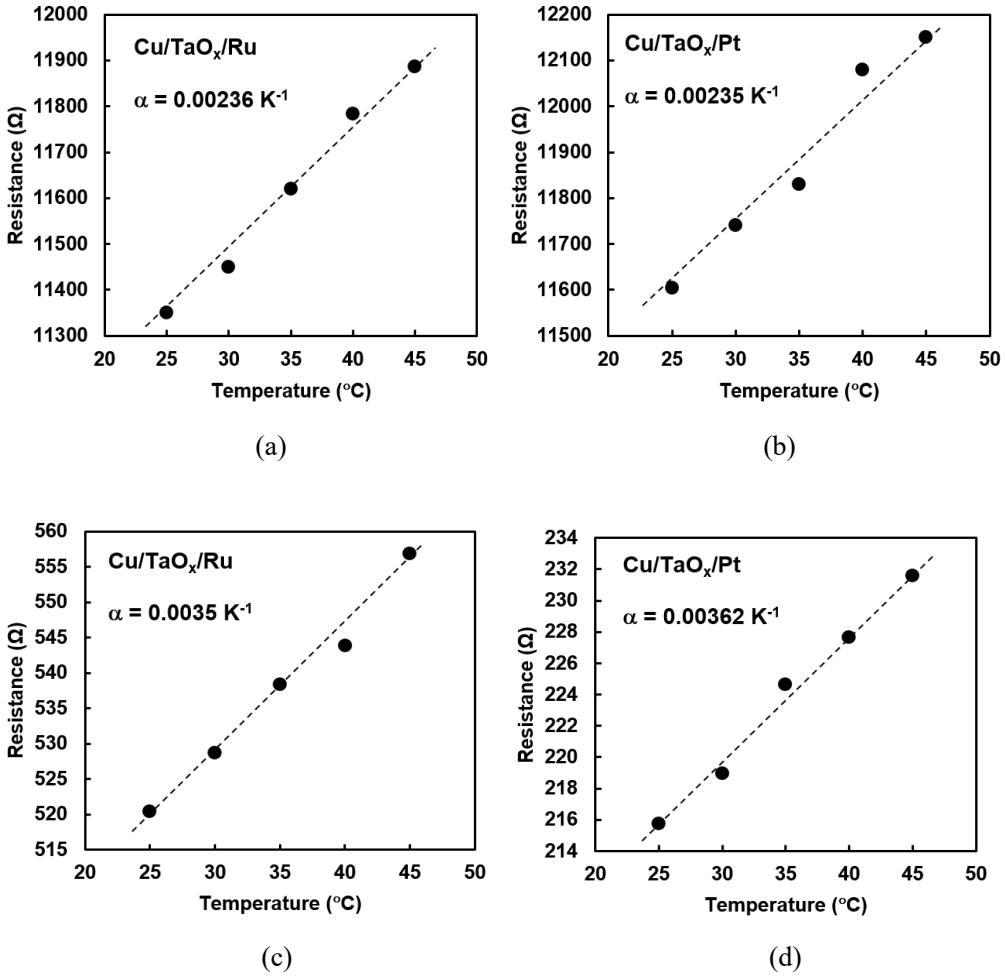


Figure 3.19 TCR of $Cu/TaO_x/Pt$ and $Cu/TaO_x/Ru$ under different I_{cc}; (a) TCR of Cu CF for Ru devices (I_{cc} = 10 μA); (b) TCR of Cu CF for Pt devices (I_{cc} = 10 μA); (c) TCR of Cu CF for Ru devices (I_{cc} = 10 mA); (d) TCR of Cu CF for Pt devices (I_{cc} = 10 mA).

3.2.3 Cu Filament Geometry in $Cu/TaO_x/Pt$ and $Cu/TaO_x/Ru$ Devices

It has been explained the much higher V_{form}, V_{set}, and V_{reset} values and the very limited switching capability of Ru device with a different geometrical shape of the Cu filament. Whereas the Cu filament for Pt device has approximately a shape of a truncated cone see Fig. 3.20, with the top radius, *a*, much smaller than the bottom radius, *b*, the Cu filament is more cylindrically shaped with *a* smaller but comparable to *b*.

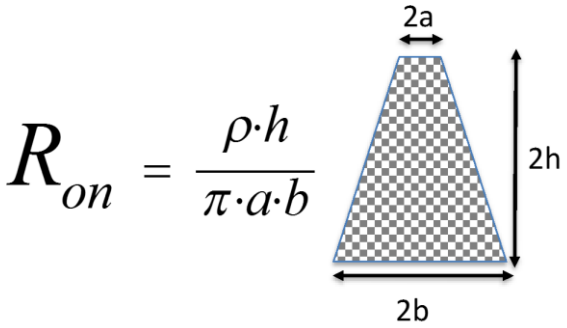


Figure 3.20 Geometric model of a truncated cone for conductive filament with the formula for on-state resistance, R_{on}.

With the assumed dimensions given in Fig. 3.20, the on-resistance of a truncated cone can be calculated as:

$$R = \rho \frac{h}{\pi ab} \tag{3.2}$$

For Cu/TaO_x/Pt devices, it is believed that the Cu filament evolution has in essence 4 stages i.e. vertical growth, lateral growth, lateral dissolution and vertical dissolution resulting from electric field driven ion migration and Joules heating in case of filament rupture. Just before the SET, the electric field is concentrated across the tip and as a result drives the ion migration vertically while before a RESET operation there is a lateral electric field at the top of the filament which drives the ion migration laterally. Based on this theory the structure of the conductive filament during the set and reset process should have a structure of a truncated cone as given by Fig. 3.21. The shape of the filament in the Pt device can be assumed to be conical with sharp tip at the Cu electrode.

For a sharply truncated cone the bulk majority of the resistance resides in the tip of the cone. This is also the locus of the Joules heat deposition according to $\int_0^{V_{reset}/rr} \frac{rr^2 \times t^2}{R_{on}} dt$ [66]. Therefore, during the reset operation, the tip of the cone becomes hot causing the diffusion of Cu atoms and rupturing thus the filament. For a cylindrically shaped filament the resistance is uniformly distributed and hence the Joule heating is also uniformly distributed. Because of the the metal

electrodes acting as heat sinks the maximum temperature occurs at half of the height of the cylinder. It is clear that the same maximum temperature is reached at much higher currents for the cylindrical shape than for the sharply truncated cone shape of the filament. Based on equation given in 3.2, we construct Cu filaments for the Pt and Ru device: b_{Pt} = 3 nm and a_{Pt} = 0.5nm of the Cu CF in Pt devices and b_{Ru} = 1.76 nm and a_{Ru} = 0.85 nm of the Cu CF in Ru device. The length of Cu CF h, which is also thickness of solid electrolyte, is 25 nm. The resistivity of copper filament is assumed to be 300×10^{-6} Ω•cm [67]. Based on equation in 3.2, the resistances of Cu CFs for Pt and Ru devices are 15,923 Ω and 15,966 Ω, respectively, which are almost the same values shown in Fig. 3.10 and Fig. 3.18. Thus although both Cu filaments have the same Ron, the Cu filament of the Ru device is much more difficult to be ruptured than the more cylindrical Cu filament of the Pt device.

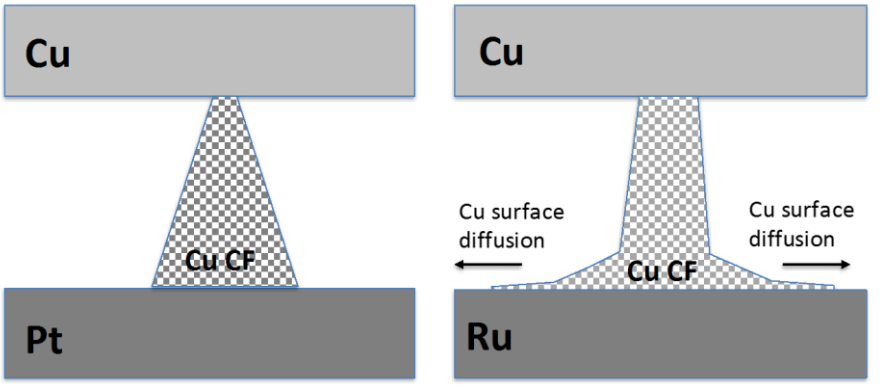


Figure 3.21 Hypothesized geometrical shape of Cu conductive filament structures for (a) Cu/TaO_x/Pt and (b) Cu/TaO_x/Ru devices.

What remains to be explained is the issue: why should Cu filament in Ru device have more cylindrical shape than in Pt device? Both metals are excellent Cu diffusion barriers. R. Chun et al [68] reported that a 20 nm Ru barrier prevents Cu diffusion at temperature up to 450 ^{o}C. Thus a Cu diffusion into Ru electrode which could weaken the base of the truncated cone and lead to a more cylinder like shape should be excluded. Ertl and coworkers [69] have shown that Cu adatoms display high interfacial diffusivity on Ru surfaces, which contributes to the excellent electroplating properties of Cu on Ru. Ru has a fairly high surface energy of 1.28 eV when compared with the

surface energy of Cu (0.69 eV) and of Pt (0.98 eV) [70,71]. Based on these reported values the wetting and also Cu adatom diffusion on Ru is expected to be significantly higher than on Pt surfaces. The higher interfacial diffusion of Cu on Ru than on Pt surfaces is likely to be responsible for lateral Cu transport at the bottom of the filament as shown in Fig. 3.21. The lateral Cu diffusion creates a broad base of the filament forcing the shape of the filament to adopt a more cylindrical form.

Chapter 4 Characterization of Time-dependent Dielectric Breakdown (TDDB) of Covalent Dielectrics

The reliability for current state of the art logic and memory devices is largely limited by the intrinsic ability of the various insulating dielectric materials utilized in these devices to retain their insulating state for the lifetime of the product. The objective of this work is to assess the suitability of covalent dielectrics for back-end metallization and potential collocated memory applications.

The BEOL (Back-End-Of-Line) reliability is tied to time dependent failure that occurs inside dielectric between metal lines. Dielectrics that break down at low electric-fields cannot be deployed. In case the dielectrics meet the reliability requirement, the next question is whether they are suitable for resistive switching memory cell applications.

4.1 Introduction

The reliability for current state of the art logic and memory devices is largely limited by the ability of the various insulating dielectric materials utilized in these device to retain their insulating state for the lifetime of the product. Specific examples where dielectric breakdown is problematic include gate dielectric wear out in complementary metal-oxide semiconductor (CMOS) transistors and time dependent dielectric breakdown (TDDB) of the interlayer dielectric (ILD) in metal interconnect structures. In contrast, some futuristic electrical devices actually take advantage of the ability to reversibly switch a dielectric from an insulating to a conductive state to perform memory and logic operations. At a fundamental level, the reliability physics of dielectric breakdown and resistive switching (RS) device operation should be similar or related. However, many aspects of the physics behind dielectric reliability and RS device operation are still poorly understood and a unified theory for both is lacking. This project seeks to fill in two specific gaps in the understanding of these two related phenomena that could lead to a more unified understanding.

The goal of this project will be to address a fundamental theory concerning electrical breakdown of dielectric materials. Specifically, it has long been held that polarizable (i.e. ionic) chemical bonds are strained/distorted in the presence of an electric field and under constant electrical (field) stress, some chemical bonds will eventually rupture or rotate to align themselves with the electric field creating this defects. With sufficient time and electrical stress, a percolating path of broken bonds will be created through which electrons can be easily transported and the dielectric "shorted out" or broken down. A corollary for this model is that materials made from purely non-polarizable (i.e. covalent) chemical bonds should be immune to time dependent dielectric breakdown failure. However, this hypothesis has not been stringently tested. Therefore, the goal of this project will be to directly perform TDDB measurements on pure covalent materials, low-k dielectric MIM and MI-semiconductor (MIS) devices supplied by Intel Corporation.

4.2 Devices Structures

The aim of this project to analyze the electrical reliability of covalent interlayer dielectric material. One of the most common method to confirm electrical reliability is to perform a time dependent dielectric breakdown. Fig. 4.1 gives us a schematic representation of the device structure which is MI-semiconductor (MIS) device. Such a structure is stressed under harsh conditions like high electric fields, elevated temperatures and prolonged time periods, in order to seek for a condition wherein the dielectric undergoes a breakdown or, in other words, fails to provide adequate isolation of the metal electrodes from each other. From an application point of view, if the identified materials survive such harsh testing conditions, it would indicate immunity to failure, and, hence, a high reliability of the device. Therefore, we would like to have information to what limits dielectric can be stressed.

A potential bias is applied to the carbon samples by connecting a voltage bias across the top Ti-Al metal electrode and the bottom highly doping P-type silicon substrate. While for the SOI and a-Si:H sample on SiO_2, the IV and TDDB measurements will need to be performed using two opposing topside electrodes.

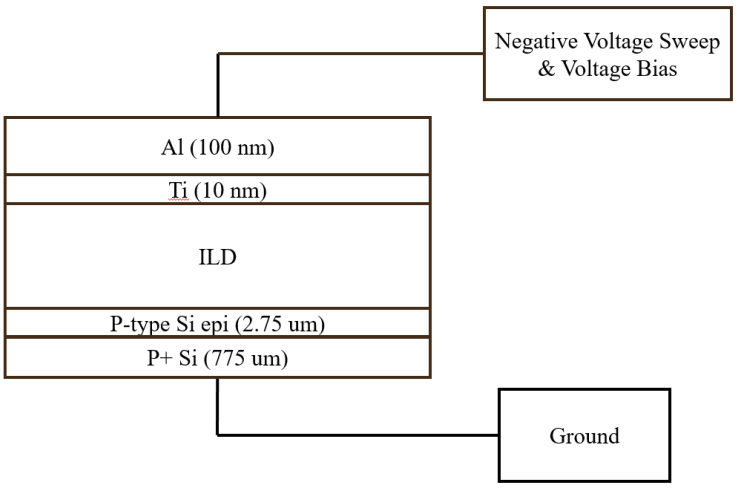


Figure 4.1 Schematic layer structure of the cross section of covalent dielectric interconnect.

Fig. 4.2 gives the device layout with top electrode of Al metal on the surface. Highly doping P-type silicon substrate is at the bottom of the samples. There are five sizes of the top electrode with diameter ϕ of 0.020”, 0.030”, 0.040”, 0.060, and 0.080”. Different feature sizes have been provided and this gives us the opportunity to play around with the current density while performing a voltage sweep test. This layout is repeated all over the sample and remains constant for all type of samples.

Figure 4.2 Top view of the device layout.

Table 4.1 gives a list of the interlayer dielectr ic that have been provided by Intel for electrical characterization. To do TDDB testing on the SOI samples (sample 37 and sample 74), the measurements will have to be performed in plane as opposed to the carbon samples where the IV

and TDDB measurements can be performed across the plane. However, since the breakdown voltage of SiO_2 is tremendous high (10 MV/cm) and the smallest distance between two top electrodes is 0.4cm, at least 4 MV of voltage bias is needed to breakdown the SOI samples. Considering the SOI samples will never breakdown with the Keithley 4200–SCS (Semiconductor Characterization System), Sample 37 and sample 74 were not subjected to a TDDB measurement.

Table 4.1 Intel TDDB samples

Priority #	Wafer #	Sample Description	Thickness	Bottom Electrode	Top Electrode	Bonding	Comment
1	D	Diamond	1 micron	Si	10 nm Ti/100 nm Al	C-C4	Crystalline, 0% hydrogen
2	295	DLC (Diamond like carbon)	100 nm	Si	10 nm Ti/100 nm Al	H0.5-C-C3.5	Amorphous, 27% hydrogen
3	307	a-C:H	500 nm	Si	10 nm Ti/100 nm Al	H-C-C3	Amorphous, 33% hydrogen
4	26	Polystyrene	100 nm	Si	10 nm Ti/100 nm Al	H2-C-C2	Amorphous, 50% hydrogen
5	377	a-Si:H (CVD)	10 nm	Si	10 nm Ti/100 nm Al	H-Si-Si3	Amorphous, < 3% hydrogen
6	37	a-Si:H (PECVD) on SiO2	100 nm	NA	10 nm Ti/100 nm Al	H-Si-Si3	Amorphous, 7% hydrogen
7	74	SOI (silicon on insulator)	10 nm	NA	10 nm Ti/100 nm Al	Si-Si4	Crystalline, 0% hydrogen
8	USF2-97	3C-SiC epi on Si	500 nm	Si	10 nm Ti/100 nm Al	Si-C4	Crystalline, 0% hydrogen

4.3 Test Methodology

Voltage Sweep Test

To perform voltage sweep test, Keithley 4200 SCS is used to characterize the whole samples. The samples are stressed with a linear ramp voltage having an interval time of 50 ms per step size. In the voltage sweep testing, voltage sweep rate of 0.2 V/s is used as the test condition. The schematic diagram in Fig. 4.3 gives a dual sweep from 0 V to a maximum voltage and back to 0V. The voltage is ramped up from 0 V at a specified step size and until a specified stop voltage is reached. Since the substrate epi is lightly p-type, reliable IV measurements of the dielectric can't be performed in the positive direction because a reverse biased diode is essentially formed, which means measuring the properties of that junction. So for these types of substrates, negative bias

always used to perform IV and CV measurements.

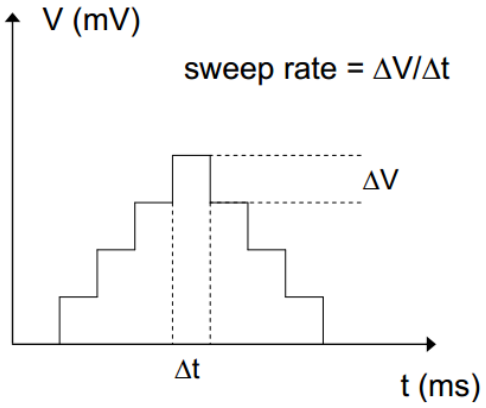


Figure 4.3 Schematic illustration of voltage sweeping mode memory devices in DC characterization.

After performing the linear voltage stress, temporary dielectric breakdown happens in all samples. It means the dielectric can recover after the removal of power supply. On retesting, such samples undergo a new breakdown.

Current Density vs. Electric Field

Since the device area size is varying for different samples, current density is a better indicator to investigate the dielectric breakdown by analyzing the relation between the current density and electric field.

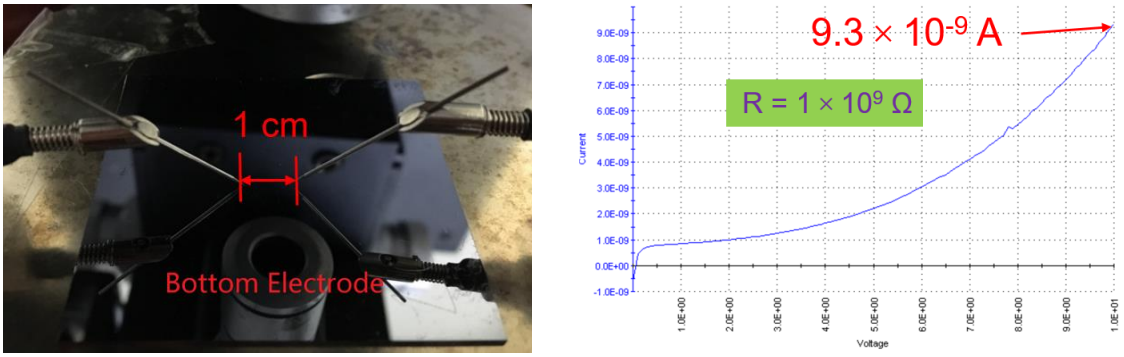
Time Dependent Dielectric Breakdown

The most commonly used test for the investigation of TDDB behavior is "constant stress". Constant stress tests can be applied in form of constant voltage stress or constant current stress. In the former, a voltage (that is often lower than the breakdown voltage of the dielectric) is applied to the top electrode, while its leakage current is being monitored. The time it will take for the dielectric to break under this constant applied voltage is called the time-to-failure. The test is then repeated several times to obtain a distribution of time-to-failure.

Bottom Electrode Contact Issue

According to the Table 4.1, the bottom electrode for all carbon samples are highly doping silicon substrate. However, it will introduce Schottky contact between silicon substrate and needle on the probe station, which will lead to the voltage bias applied on the dielectric is not accurate.

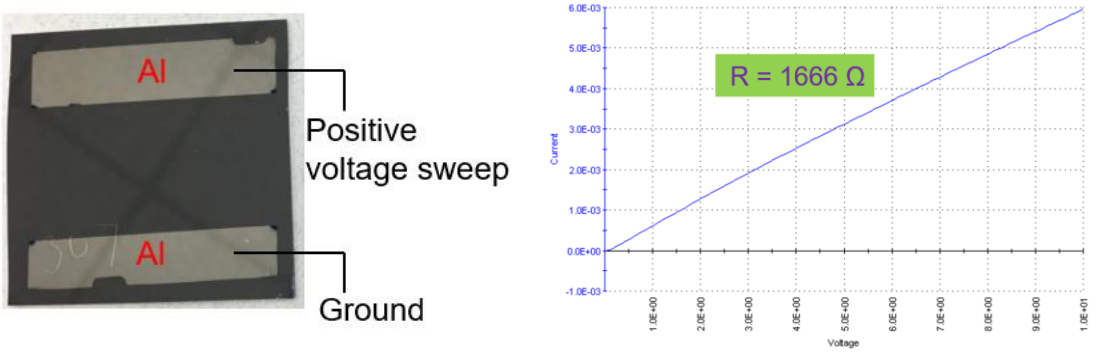
Fig. 4.4 (a) shows the test set-up of measuring the resistance of the bottom electrode in order to illustrate the Schottky contact issue. The resistivity of substrate is 80 Ω·cm. The thickness of bottom electrode and the distance between two needles are 775 μm and 1cm. Therefore, we obtain the calculated resistance of 1 cm length silicon substrate is 1032 Ω. Nevertheless, in Fig. 4.4 (b) the measured resistance of 1cm length silicon substrate is 1×10^9 Ω, which is significantly different with expected value.



(a) (b)

Figure 4.4 (a) Test-up of resistance of silicon substrate measurement; (b) I-V characteristic of resistance.

In order to eliminate the schotty contact, two thin Al film is deposited on the bottom electrode, as is shown in Fig. 4.4 (a). Fig. 4.4 (b) gives the I-V characteristic of resistance of 1cm length silicon substrate with metal contact. It can be seen that the resistance is 1666 Ω, which is closed to the value in calculation.



(a) (b)

Figure 4.5 (a) Test-up of resistance of silicon substrate measurement with Al contact;

(b) I-V characteristic of resistance.

Thus, the bottom electrode of all Intel samples are deposited with Al on surface.

4.4 Results and Discussion

Voltage sweep test is performed on five different Intel samples which have covalent materials as ILD, i.e. Polystyrene and a-C:H. All tested samples have a 0.02'' diameter size to guarantee same test conditions. The voltage sweep is ramped up from 0 V to 60 V with voltage sweep rate rr = 0.2 V/s. The test is operated at room temperature. It can be seen from Fig. 4.6 that for all samples the current increases with increasing electric field. Especially, the current in sample 26 is the highest compared with others. It because polystyrene in sample 26 has the highest percentage (50%) of hydrogen than other covalent dielectric, which makes the chemical bonds in polystyrene easiest to be broken. Therefore, Diamond in sample D1 absolutely has the lowest current and tremendous hard to breakdown.

Furthermore, when the voltage is ramped up, the current increases gradually without any abrupt change. Such gradual current increase is called soft breakdown of the dielectric. The soft breakdown is volatile, which means the conductive path disappears when the device is no longer powered. Or in other words, the dielectric recovers when the electric field is removed.

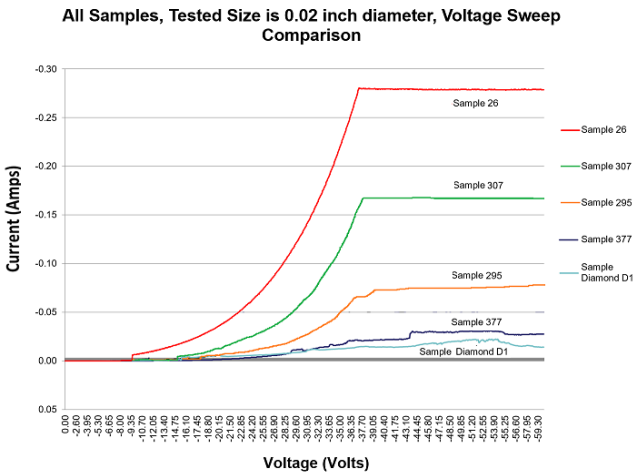
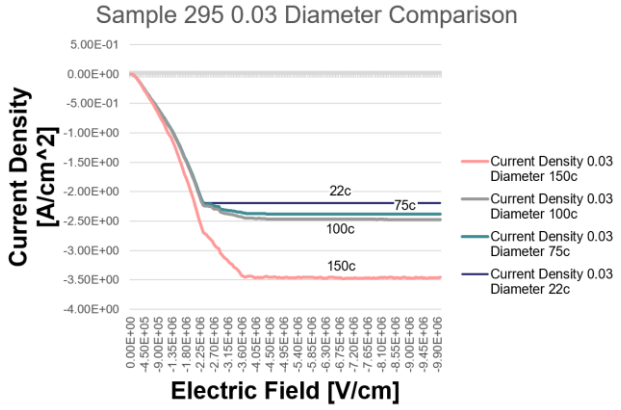


Figure 4.6 I-V Characteristic for covalent samples at room temperature.

Fig. 4.7 shows the dependence of current density on electric field for three different covalent dielectrics: Diamond Like Carbon (DLC, sample 295), a-C:H (sample 307) and Polystyrene (sample 26). The voltage sweep ramped up from 0 V to -80 V with rr = 0.2 V/s. All devices are stressed at elevated temperatures starting from 22 °C. All tested samples have a 0.03'' diameter size to guarantee same test conditions. It can be seen that the current density increases not only with increasing electric field and but also with increasing temperature. The higher temperature provides the mobile carriers with higher thermal energy and this leads to a faster dielectric breakdown.



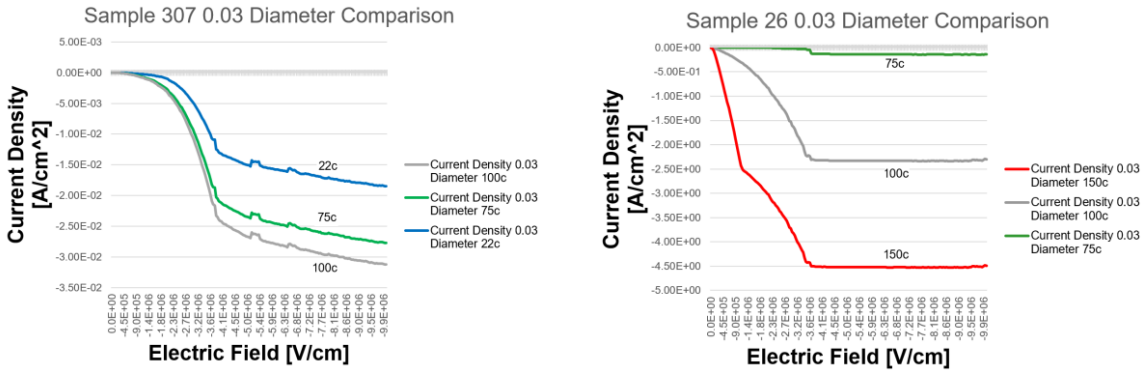
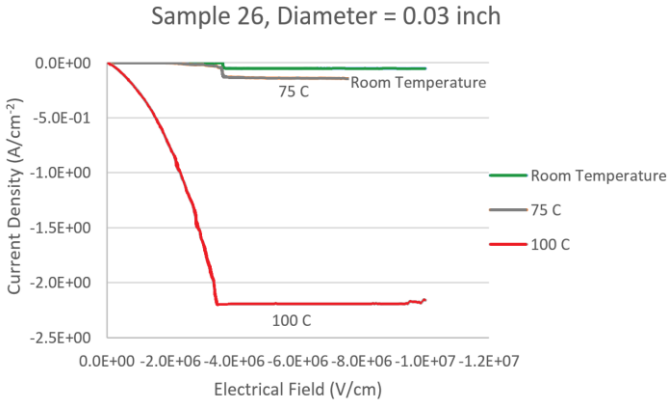


Figure 4.7 Current Density vs. Electric Field for samples with 0.03" diameter size.

Fig. 4.8 gives the dependence of current density on electric field for sample 26 with different device size. For devices with different size, it can observed that the current density gradually increases with increasing electrical field until it reaches to - 4×10^6 V/cm followed by keeping almost constant without limited by the I_{cc}. Moreover, the current density increases with increasing temperature and larger size device has higher current density. In all samples only soft breakdown has been observed and not a single instance of a hard (permanent) breakdown.



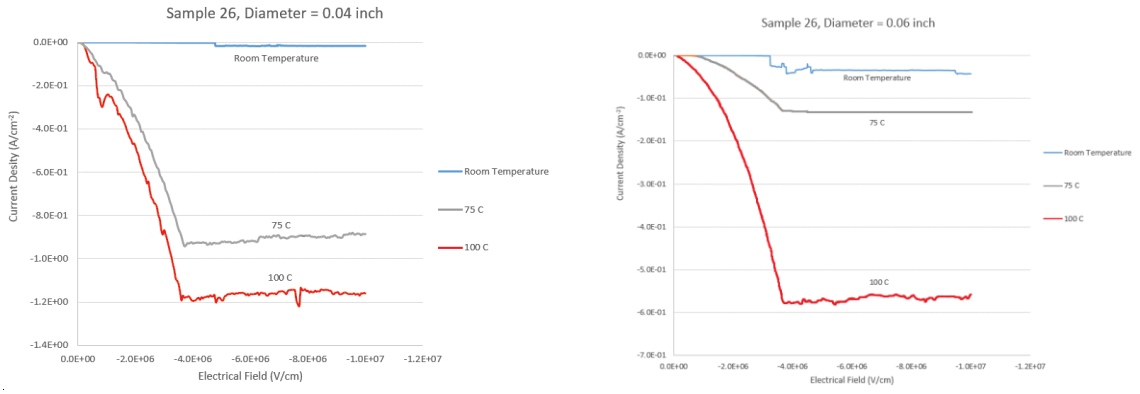


Figure 4.8 Current Density Vs Electric Field for different device sizes.

In Fig. 4.9, the dependence of current density on electric field for three different samples at 100 °C are compared. From the figure, sample 26 with Polystyrene as ILD has highest current density compared with other two. It because polystyrene has higher percentage (50%) of hydrogen than DLC (27%) and a-C:H (33%), which makes the chemical bonds in polystyrene easier to be broken.

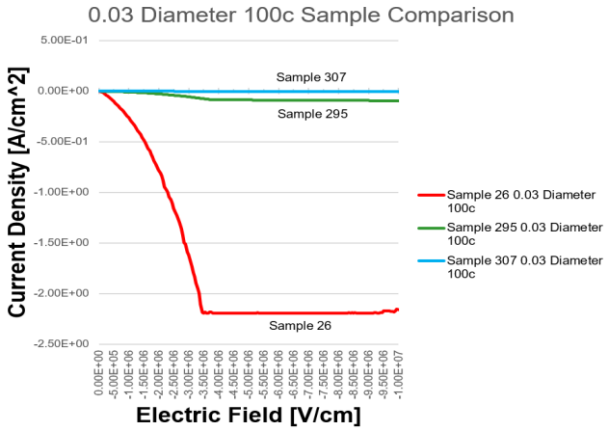


Figure 4.9 Current Density Vs Electric Field at 100 °C for sample 26, 295 and 307.

TDDB measurement on pure covalent materials are performed on sample 26, sample 295 and sample 307. For the TDDB testing conditions in sample 26, a voltage bias of -40 V is applied on the device for 2 hours. Permanent breakdown of dielectric is not observed at room temperature or even at high temperature (100 °C) for both sample 26 and sample 295, as is shown in Fig. 4.10.

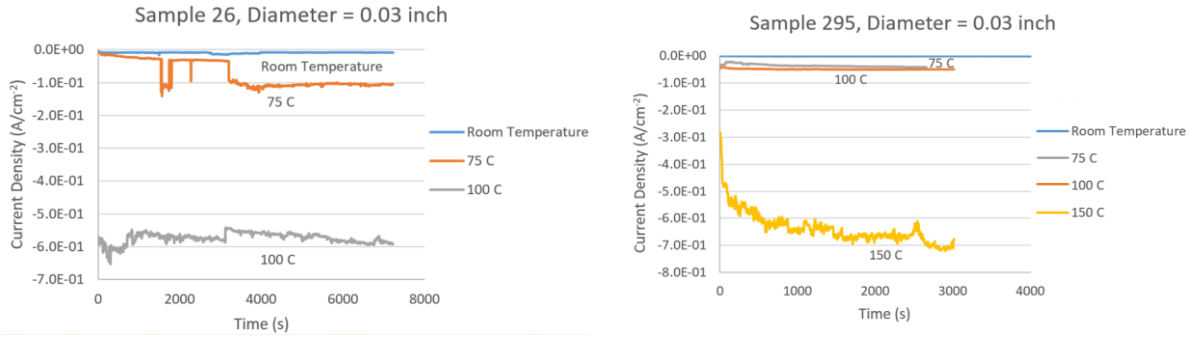


Figure 4.10 TDDB measurements on sample 26 and sample 295.

The TDDB measurements on sample 307 under elevated temperature stress is performed. Permanent breakdown of dielectric is still not observed at room temperature or even at high temperature. However, an interesting behavior of self-healing of breakdown is observed in TDDB testing on sample 307 for amorphous carbon, as is shown in Fig. 4.11. The current first increases, reaches a maximum value at 20 s and then reduces sharply settle at very low leakage currents of ~ $1x10^{-4}$ A/cm^2.

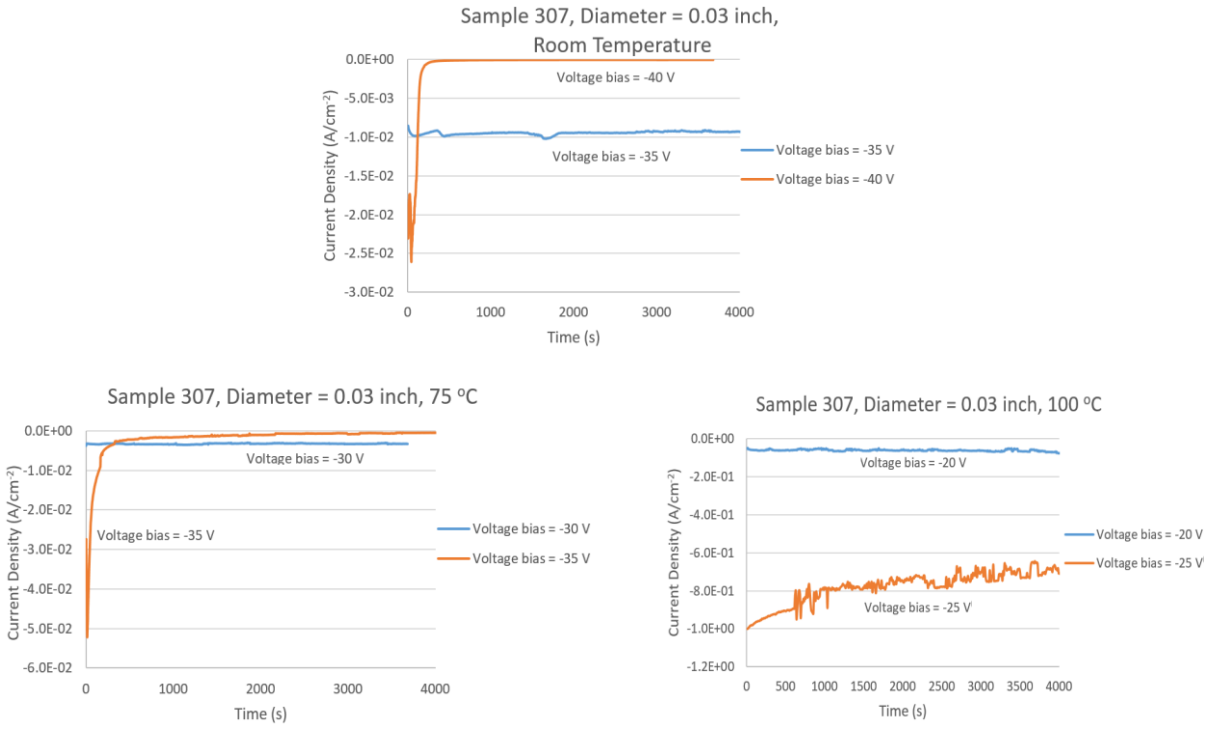


Figure 4.11 TDDB measurements on sample 307 under elevated temperature stress.

The self-healing effect is presently not understood, but is of significant technological interest as it opens a possibility to cure the dielectric with voltage stress for a short time (10~20 seconds) to generate a virtual immunity to TDDB for a wide range of applied voltages.

Chapter 5 Conclusion

5.1 Summary

MIM structures with porous insulators have been subjected to resistive switching electric testing methodology. The findings can be summarized as follows: (1) Overwhelming majority of the samples is conductive from the beginning. The conductance is a bulk phenomenon and can be attributed to high level of Cu doping in the dielectric. (2) A small portion of devices with at least one diffusion barrier displays resistive switching behavior of various degrees. While most of the devices can be set only once, some devices can be set and reset repeatedly. Thus resistive switching can be realized is porous devices. (3) The forming voltage of the filaments increases with the level of porosity. (4) The filament formation at positive and negative bias results in different types of filament. Filaments formed at positive bias applied to Cu electrode are Cu filaments and filaments formed at negative bias are attributed to defects or broken bonds of the dielectric matrix. Measurements of temperature coefficient of resistance have confirmed that both types of filaments have substantially different TCR coefficients. (5) Annealing of the samples at temperatures up to 100 °C rendered all samples more conductive. The conclusion is that annealing causes more Cu diffusion and more Cu activation. (6) The initial bulk condition depends sensitively on the applied compliance current I_{cc}. For I_{cc} smaller than 7-9 mA the resistance decreases with increasing current. At I_{cc}=7-9 mA the resistance of the device becomes independent of the applied I_{cc}. This may imply Joules annealing effects of the initial Cu distribution in the dielectric. (7) Further optimization of resistive switching devices based of porous dielectric materials will rely crucially on the engineering of the Cu diffusion barriers between the two electrodes of the device.

Evidence for decoupling of ion diffusivity and mobility in porous materials has been presented. The decoupling means that on a global scale the mobility is significantly smaller than the product of diffusivity and thermal voltage as predicted by the Einstein relation in homogeneous media. The retardation factor f_p will be a function not only of the porosity of the material but also of the interconnectedness of the matrix material, characterized by a parameter called tortuosity. A

numeric drift-diffusion model in 2D has been proposed which is being currently evaluated. From the simulations the retardation factor f_p will be determined as a function of porosity and tortuosity.

Cu/TaO_x/Pt and Cu/TaO_x/Ru devices have been manufactured in the VTech cleanroom. The electric characterization of both devices has shown many similarities and some notable differences. The forming and set voltages for Cu filaments in Ru devices are significantly higher (V_{form}(Ru)-V_{form}(Pt) ≈ 3V) than in Ru devices. In resistive switching devices the resistance of the conductive filament is a strong function of the imposed compliance current, I_{cc}. We find that the general behavior of R_{on} for Cu CF is similar for both devices for Ru device; It has been found $R_{on}=0.5/I_{cc}^{1.01}$ while for Pt device $R_{on}=0.61/I_{cc}^{1.08}$ at the same rr = 0.2V/s. As shown elsewhere with the exponent of I_{cc} in the denominator being close to 1, the constants 0.61 V and 0.5 V can be interpreted as the lowest possible V_{set} voltages under which the device can be set. This usually can be reached as a limiting case for very slow voltage ramp rates. The difference in the minimum set voltage extracted from R_{on}-I_{cc} characteristics confirms that the V_{set} voltages for Ru devices are significantly higher than for Cu devices. The major drawback of the Ru device is that while Pt devices can be switched repeatedly back and forth, while Ru device are becoming not resettable after a few set-reset operations or even after the first set operation. The failure of the Ru devices after a few switching cycles is likely to be related to geometrical shape of the Cu filament. This behavior is attributed to the reduced stopping power of Ru with respect to Cu diffusion compared with the stopping power of Pt.

5.2 Future Works

This research explores and evaluates the switching characteristics and mechanisms of metal/insulator/metal devices. In order to fully exploit the resistive switching on porous dielectrics, future investigation can be done in the following areas. First of all, the excessive Cu diffusion into dielectric has to be prevented. This may be accomplished by thicker Cu diffusion barriers at the expense of a higher effective dielectric constant. Plasma deposition of dielectric may be used to reduce the thermal budget that drives Cu diffusion. Finally, a thin inert metal barrier of Co, Ir, or

W may be deposited between Cu metal electrode and the dielectric. These approaches will be pursued in future work.

List of Publications

The work of this thesis is based on the following publications:

[1] Y. Fan, M. Al-Mamun, B.Colon, S. W. King, and M. K. Orlowski. Resistive Switching Comparison Between Cu/TaO_x/Ru and Cu/TaO_x/Pt Memory Cells, *230th Electrochemical Society Meeting*, Oct. 2016.

[2] Y. Fan, M. K. Orlowski, S. W. King and J. Bielefeld. Characterization of Porous BEOL Dielectrics for Resistive Switching, *ECS Trans*, 2016, vol. 72, issue 2, 233-240.

[3] Y. Fan, M. K. Orlowski, S. W. King and J. Bielefeld. Decoupling of Ion Diffusivity and Electromobility in Porous Dielectrics, *ECS Trans*, 2016, vol. 72, issue 2, 35-50.

References

[1] R.L. Geiger, P.E. Allen, and N.R. Strader, "VLSI design techniques for analog and digital circuits", *McGraw Hill*, p. 853, 1990.

[2] K. Fife, A. El Gamel and H-S-P Wong, *IEEE ISSCC Tech*. Feb., 48, 2008.

[3] E.G.Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits", *Proceeding of the IEEE*, vol. 89, Issue 5, pp: 665-692, 2001.

[4] Meng He, "Thermal and Electrical Stability of Metal/Porous Low-k Dielectric Interface", *Doctor of Philosophy Thesis*. 2011.

[5] D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, A. Stamper, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, P. McLaughlin, T. Katsetos, H. Rathore, R. Schulz, L. Su, S. Luce, N. Rohrer, and J. Slattery, *Tech. Dig. IEEE IEDM*, 376, 1997.

[6] R. Rosenberg, D. C. Edelstein, C. –K. Hu, and K. P. Rodbell, "Copper metallization for high performance silicon technology", Annu. *Rev. Mater. Sci*. 30 229-62, 2000.

[7] International Roadmap for Semiconductors (ITRS), *Semiconductor Industry Association*, 2009.

[8] Mikhail R. Baklanov, Paul S. Ho and Ehrenfried Zschech, *Advanced Interconnects for ULSI Technology*, 2012.

[9] Interconnect Challenges Grow, http://semiengineering.com/interconnect-challenges-grow -2/.

[10] K. Kuhn, *IEEE Trans. Elect. Dev*. 59, 1813, 2012.

[11] S. King, H. Simka, D. Herr, H. Akinaga, and M. Garner, *APL Mater*. 1, 040701, 2013.

[12] Shyam P. Murarka, Igor V. Verner, and Ronald J. Gutmann, "Copper – Fundamental Mechanisms for Microelectronic Applications", *John Wiley & Sons*. Inc., 2000, p. 6.

[13] 14 nm Process Technology: Opening New Horizons, http://www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf.

[14] Bohr, Mark T., "Interconnect scaling, The real limiter to high performance ULSI", *Electron Devices Meeting*, 39(9):241-244, 1996.

[15] C. Kittel, *Introduction to solid state physics*. Wiley, 1996.

[16] Yoonki Sa, "Mechanical Reliability of Porous Low-k Dielectric for Advanced Interconnect: Study of the Instability Mechanisms in Porous Low-k Dielectrics and their Mediation Through Inert Plasma Induced Re-polymerization", *Doctor of Philosophy Thesis*, 2015.

[17] Morgen, M., et al., "Low dielectric constant materials for ULSI interconnects". *Annual Review of Materials Science*, 30: p. 645-680, 2000.

[18] K. Maex, M. R. Baklanov, D. Shamiryan, F. Iacopi, S. H. Brongersma, and Z. S. Yanovitskaya, "Low dielectric constant materials for microelectronics", *J. Appl. Phys*. 93, 8793-884, 2003.

[19] Grill, A. *Journal of Applied Physics*. 93, no. 3. 2003. p. 1785.

[20] Kwak SI, Jeong KH, Rhee SW, "Nanocomposite low-k SiCOH films by direct PECVD using vinyltrimethylsilane", *J. Electrochem. Soc*. 151:F11–16, 2004.

[21] Tada M, Yamamoto H, Ito F, Takeuchi T, Furutake N, Hayashi Y, "Chemical structure effects of ring-type siloxane precursor on properties of plasma-polymerized porous SiCOH films", *J. Electrochem. Soc*. 154: D354–61, 2007.

[22] Tada M, Kawahara J, Hayashi Y, "Characterization of plasma-polymerized divinylsiloxane benzocyclobutene (DVS-BCB) polymer film"., *Mater. Res. Soc. Conf. Proc*. ULSI XVI: 579–85, 2001.
[23] Kawahara J, Kinimi N, Kinoshita K, Nakano A, Komatsu M, et al, "An organic low-k film deposited by plasma-enhanced copoloymerization". *J. Electrochem. Soc*. 154: H147–52, 2007.
[24] Wu Q, Gleason KK, "Plasma-enhanced CVD of organosilicate glass (OSG) films deposited from octamethyltrisiloxane, bis (trimethylsiloxy) methylsilanes, and 1,1,3,3-tetramethyldisiloxane". *Plasmas Polym.* 8:31-41, 2003.
[25] W. Volksen, R. D. Miller, and G. Dubois, "Low dielectric constant materials", *Chemical reviews*, vol. 110, no. 1, pp. 56-110, Jan. 2010.
[26] Low K and ultra low K SiCOH dielectric films and methods to form the same, *Patent US* 20060055004 A1.
[27] A. Grill, S. Gates, T. Ryan, S. Nguyen, and D. Priyadarshini, *Appl. Phys. Rev*. 1 011306, 2014.
[28] G. Antonelli, G. Jiang, R. Shaviv, T. Mountsier, G. Dixit, K. Park, I. Karim, W. Wu, H. Shobha, T. Spooner, E. Soda, E. Liniger, S. Cohen, J. Demarest, M. Tagami, O. Vander Straten, and F. Baumann, *Microelectron*. Eng. 92, 9, 2012.
[29] M. Baklanov, J. de Marneffe, D. Shamiryan, A. Urbanowicz, H. Shi, T. Rakhimova, H. Huang, and P. Ho, J. *Appl. Phys*. 113, 041101, 2013.
[30] M. Albrecht and C. Blanchette, *J. Electrochem. Soc.* 145, 4019, 1998.
[31] K. Moors, B. Soree, Z. Tokei, and W. Magnus, *J. Appl. Phys.* 116, 063714, 2014.
[32] E. Eisenbraun, Microelectron, "Ultimate limits of conventional barriers and liners-implications for the extendibility of copper metallization", *Eng.* 92, 67, 2012.
[33] H. Wong and S. Salahuddin, "Memory Leads the Way to Better Computing", *Nat. Nanotech*. 10, 191, 2015.
[34] K. Bernstein, R. Cavin, W. Porod, A. Seabaugh, and J. Welser, Proc. IEEE 98, 2169 , 2010.
[35] D. Nikonov and I. Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits", *Proc. IEEE* 101, 2498, 2013.
[36] R. Waser, R. Dittmann, G. Staikov, and K. Szot, *Adv. Mater.* 21, 2632, 2009.
[37] D. Jeong, R. Thomas, R. Katiyar, J. Scott, H. Kohlstedt, A. Petraru, and C. Hwang, *Rep. Prog. Phys.* 75, 076502, 2012.
[38] S. Clima, K. Sankaran, Y. Chen, A. Fantini, U. Celano, A. Belmonte, L. Zhang, L. Goux, B. Govoreanu, R. Degraeve, D. Wouters, M. Jurczak, W. Vandervorst, S. De Gendt, and G. Pourtois, *Phys. Status Solidi RRL* 8, 501, 2014.
[39] M. Tada, K. Okamoto, T. Sakamoto, M. Miyamura, N. Banno, and H. Hada, *IEEE Trans. Elect. Dev.* 58, 4398, 2011.
[40] N. Banno, M. Tada, T. Sakamoto, K. Okamoto, M. Miyamura, N. Iguchi, and H. Hada, *IEEE Trans. Elect.* Dev. 61, 3827, 2014.
[41] A. Edwards, H. Barnaby, K. Campbell, M. Kozicki, W. Liu, and M. Marinella, *Proc. IEEE* 103, 1004 , 2015.
[42] L. Sandrini, M. Thammasack, T. Demirci, P. Gaillardon, D. Sacchetto, G. De Micheli, and Y. Leblebici, Microelectron. *Eng*. 145, 62, 2015.

[43] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, *Mat. Sci. Engr*. R 83, 1, 2014.
[44] L. Goux and I. Valov, *Phys. Status Solidi* A 213, 274, 2016.
[45] I.Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Electrochemical metallization memories-fundamentals, applications, prospects," *Nanotechnology*, vol.22, no.5, 254003, 2011.
[46] Santosh Murali, "Investigation of Bipolar Resistive Switching in Zinc-Tin-Oxide for Resistive Random Access Memory", *Master of Science Thesis*, 2011.
[47] Konstantina Saranti, Sultan Alotaibi and Shashi Paul, "A new approach for two-terminal electronic memory devices - Storing information on silicon nanowires", *Scientific Reports*, 6:27506, 2015.
[48] S. King, M. French, J. Bielefeld, and W. Lanford, *J. Non-Cryst. Sol.* 357, 2970, 2011.
[49] W. Zhou, S. Bailey, R. Sooryakumar, S. King, G. Xu, E. Mays, C. Ege, and J. Bielefeld, J. *Appl. Phys.* 110, 043520, 2011.
[50] Y. Matsuda, S. King, J. Bielefeld, J. Xu, and R. Dauskardt, *Acta Mater.* 60, 682, 2012.
[51] Y. Matsuda, I. Ryu, S. King, J. Bielefeld, and R. Dauskardt, Small 10, 253, 2014.
[52] Tong Liu, Yuhong Kang, Sarah El-Helw, Tanmay Potnis, and Marius Orlowski, "Physics of Voltage Constant in Multilevel Switching of Conductive Bridge Resistive Memory", *Japanese Journal of Applied Physics*, Vol 52 084202, 2013.
[53] T. Liu, Y. Kang, S. El-Helw, T. Potnis, and M. Orlowski, *Mater. Res. Soc. Symp. Proc.* Vol. 1562, 552, 2013.
[54] T. Liu, M. Verma, Y. Kang, and M.Orlowski, *ECS Sold.Stat. Lett.*(1)1, Q11-Q13, 2012.
[55] R. Ali, Y. Fan, and M. Orlowski, "Modeling and Simulation of Ion Drift-Diffusion in Porous Media", to be published.
[56] T. Sakamoto, N. Banno, N. Iguchi, H. Kawaura, H. Sunamura, S. Fujieda, K. Terabe, T. Hasegawa, and M. Aono, "A Ta_2O_5 solid-electrolyte switch with improved reliability," in *Tech. Dig. – VLSI Symp.*pp. 38-39, 2007.
[57] N. Banno, T. Sakamoto, N. Iguchi, H. Sunamura, K. Terabe, T. Hasegawa, and M. Aono, "Diffusivity of Cu ions in solid electrolyte and its effect on the 154 performance of nanometer-scale switch," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3283-3287, 2008.
[58] J. Stevens, A. Lohn, S. Decker, B. Doyle, P. Mickel, and M. Marinella, J., "Reactive sputtering of substoichiometric Ta_2O_x for resistive memory applications", *Vac. Sci. Technol.*, A 32, 021501, 2014.
[59] Tong Liu, Yuhong Kang, Mohini Verma, and Marius Orlowski, "Novel highly Nonlinear Memristive Circuits for Neural Networks," *WCCI 2012 IEEE World Congress on Computational Intelligence*, June, 10-15, 2012.
[60] Thermal Oxidation, http://www-inst.eecs.berkeley.edu/~ee143/fa05/lectures/Lec_05.pdf.
[61] M. Verma, "Formation and Rupture of Nanofilaments in Metal/TaOx/Metal Resistive Switches", *M.S, Thesis*, 2012.
[62] Photolithography, http://www2.ece.gatech.edu/research/labs/vc/theory/photolith.html.
[63] Gargi Ghosh, "Dependence of Set, Reset, and Breakdown Voltages of a MIM Resistive Memory Device on the Input Voltage Waveform", *M.S. Thesis*, 2015.

[64] Tong Liu, Yuhong Kang, Sarah El-Helw, Tanmay Potnis, and Marius Orlowski, "Physics of the voltage Constant in Multilevel Switching of Conductive Bridge Resistive Memory", *Janpanese Journal of Applied Physics*, 52, 084202, 2013.
[65] Gargi Ghosh and Marious K. Orlowski, "Write and Erase Threshold Voltage Interdependence in Resistive Switching Memory Cells", *IEEE Tran. on Electron Devices*, Vol 62, No. 9, 2015.
[66] G. Ghosh and M. Orlowski, *IEEE Trans. on Electron Device*, 62(9), 2850, 2015.
[67] T. Liu, "Nonvolatile and Volatile Resistive-Characterization, Modeling, Memory resistive Subcircuits", *Doctor of Philosophy Thesis*, 2013.
[68] R. Chun, T. Arunagiri, Y. Zhang, O. Chyan, R. Wallace, M. Kim, and T. Hurd, *ECS Sol. State Lett*. 7(8) G154, 2004.
[69] K. Christman, G. Ertl, and H. Shimizu, *J. Catal.*, 61, 397, 1980.
[70] C. Yang, F. McFreely, B. Li, R. Rosenberg, and D. Edelstein, *IEEE El. Dev. Lett*. 32(6), 806, 2011.
[71] H. Skriver and N. Rosengaard, *Phys. Rev.* B 46(11), 7157, 1992.