A High Temperature Wideband Power Amplifier for a Downhole Communication System

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Abstract

As the oil industry continues to drill deeper to reach previously untapped wells, the operating environments for electronic systems become harsher, especially due to high temperatures. It is essential to design electronic circuits and systems to be able to withstand these extreme temperatures. The proposed power amplifier (PA) has been designed for a downhole communication system operating at an ambient temperature of 230ºC. GaN technology was chosen primarily due to its ability to function at a high junction temperature. The proposed PA was designed with Qorvo's T2G6003028-FL HEMT as it operates reliably at a high junction temperature (T_J) and also the package offers low junction to case thermal resistance (θ_{JC}). The proposed PA can operate reliably up to an ambient temperature of 230ºC using passive cooling opposed to active cooling. At 230°C it operates in class A with a peak PAE of 25.03%, maximum output power of 1.66 W, peak gain of 24.5 dB, center frequency of 255 MHz with 1dB ripple in the passband over a 60 MHz bandwidth, 1dB output compression of approximately 32 dBm, and OIP3 of 37.9dBm. CW measurements were taken for all parameters.

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Chapter 1

Introduction

As the oil industry continues drilling deeper to reach previously untapped wells, the downhole environments are becoming harsher, reaching higher temperatures and pressures which necessitate more robust electronics to reliably operate in these environments.

In drilling applications, electronics reside inside pressure compensated and partially temperature compensated capsules sent downhole to gather data. The electronics are not rated to operate at the well ambient temperature and after drilling for some time these capsules begin to heat up and need to be retrieved from the well to ensure no damage to the electronics. By designing electronics that can withstand much higher temperatures, the drilling operations can continue uninterrupted for longer periods of time before it is necessary to retrieve the capsules from the wells [1].

In addition to the ability to endure higher temperatures, higher data rates are important for downhole communication systems due to higher resolution sensors, faster data logging speeds, and additional tools available. Because of these reasons, it is important to increase the data rate from the contemporary downhole communication system data rates of approximately 4 Mb/s [2].

Schlumberger uses a classification system to better define oil wells by certain threshold which define various high-pressure, high-temperature (HPHT) wells (as shown in Figure 1) [1]. Despite wells being classified beyond 260°C the current drilling temperatures do not exceed 210°C [2]. This is due to the fact that the current electronics used in these systems can only be operated up to 150°C before being retrieved from the well. The electronics can be operated at an ambient temperature up to 210°C because of the temperature shielding that is provided by the capsules. These capsules keep the temperature inside the capsules lower than the well's ambient temperature for a period of time before finally reaching the outside ambient temperature [1]. An operation temperature of 230°C was chosen for this thesis research because it is much higher than current operating downhole systems and it was determined that electronics could be reliably designed to operate at this temperature.

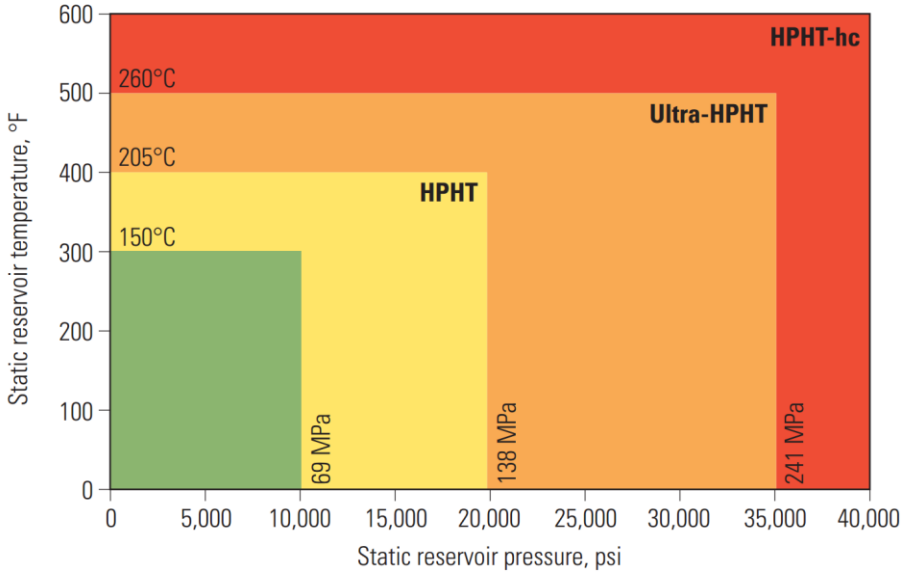

Figure 1: HBHT Classification System [1]. Used Under Fair Use, 2015.

This thesis work investigates the design of a linear power amplifier (PA) as a building block for a downhole RF communication system. Two major challenges faced for high temperature RF circuit design are:

- Few passive components are able to withstand such high temperature operation and therefore few off-the-shelf choices are available for passive components.
- The junction temperature of active devices used should not exceed their maximum temperature ratings to avoid device failure.

The first challenge can be mitigated by avoiding passive components, if possible, by designing the majority of the PA using microstrip. The second challenge can be overcome by choosing a technology able to operate at high junction temperatures. GaN devices, which are widely used for high power RF PAs, can reliably operate at extreme junction temperatures. Because of this, GaN technology would be a good choice for high temperature RF applications including downhole communications. Details of this research and ultimate selection of GaN technology will be described in Chapter 2. Due to weight contribution, power consumption, and added complexity, active cooling with fans is impractical to use downhole. The use of passive cooling by the use of a heat sink was necessary.

The PA design employed for this research is a typical linear RF PA technique because making improvements to existing PA topologies is not the thrust of this research. In addition, because this was designed for a wired system, the efficiency was not a concern. The purpose of the proposed PA is to provide a proof of concept of high temperature high frequency circuits. The proposed PA design is not only applicable for the downhole communication systems used in the oil industry. The space industry, aviation industry, and automotive industry all require high temperature high frequency electronics and information derived from this work can be directly applied to the high temperature high frequency electronics required in these industries. The contributions of this thesis research are as follows.

- Has been proven to operate for extended periods of time at 230°C (no less than 3 hours)
- High linearity PA with 1dB compression level over 32dBm measured at 230°C
- To our best knowledge, there is no existing PA designed to operate reliably for downhole communication systems at an ambient temperature of 230 °C or higher without the use of active cooling.

This thesis is organized as follows. Chapter 2 provides background for this research, research on high temperature semiconductor devices, and current research on high temperature PA design. Chapter 3 details the design procedure employed for the PA. Chapter 4 details the instruments used, the measurement procedures used, and the measured results for the PA at 230°C. Finally, chapter 5 concludes this work, discusses possible improvements, and outlines future research opportunities.

Chapter 2

Introduction

This chapter provides the background information necessary to understanding this work. Basic terminology used in RF circuit design will first be discussed. Following this section, important RF concepts such as stability, simultaneous conjugate matching, and bias tees will be explained. To conclude basic terminology and concepts important in RF design, linearity, efficiency, and conduction angle PAs will be introduced. Once the basic terminology and concepts in RF design have been discussed, important heat sink thermal considerations will be discussed to provide the reader with a basic understanding of what to consider when choosing to use a heat sink. Following this information regarding heat sink thermal concerns, an overview of research on semiconductor materials used at high temperatures will be provided. This section will review past and current research on semiconductor materials such as silicon germanium (SiGe), gallium nitride (GaN), silicon carbide (SiC), and gallium arsenide (GaAs) and what high temperature applications they have been used for. Once the reader has been provided an overview of how semiconductors have been used in high temperature environments, a more detailed analysis of high temperature effects on semiconductor materials will be provided. This chapter is concluded with a survey of research on past and current research on high temperature power amplifier design.

Basic Terminology / Concepts

Scattering-Parameters (S-parameters)

As the operation frequency of a circuit increases it becomes difficult to take measurements on voltages and currents making it impractical to use standard network classifications such as Z, Y, H, or ABCD parameters. S-parameters circumvent this impractically by defining the network by using incident and reflected waves [3]. The s-parameter matrix for a two-port network is defined in Eq. 1. And Table 1 explains what each individual s-parameters represents.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (1)$$

S-Parameter	Definition
S_{11}	Input reflection coefficient
S_{12}	Reverse transmission coefficient
S_{21}	Forward transmission coefficient
S_{22}	Output reflection coefficient

Table 1: 2-Port S-Parameter Definitions

Gain

The gain of a circuit is defined as the ratio of the output voltage, current, or power to the input voltage, current, or power were each type of gain is named accordingly (voltage gain, current gain, power gain). The important gain quantity for this work is the power gain and when this work refers to 'gain' this is the gain to which it is referring. The s-parameters for a two-port network give the gain of the circuit as S_{21}. S_{21} is the power gain of a network if it is expressed in decibels (dB) and it is the voltage gain of a network if expressed in linear units [3]. (Voltage gain is defined for the sake of completeness).

$$Power\ Gain = S_{21}(expressed\ in\ dB) \tag{2}$$

$$Voltage\ Gain = S_{21}(expressed\ in\ linear\ units) \tag{3}$$

Return Loss

The return loss of a network is the amount of power that is reflected away from the network. The input return loss (IRL) is the amount of power that is reflected back towards the generator and the output return loss (ORL) is the amount of power that is reflected back towards the load. Both the input and output return loss of a network can be derived from the s-parameters the given network [3]. For a two-port network the input and output return loss are defined.

$$Input\ Return\ Loss = |S_{11}|^{-2} \tag{4}$$

$$Output\ Return\ Loss = |S_{22}|^{-2} \tag{5}$$

Bandwidth

The bandwidth of a network is defined by an upper frequency and lower frequency which at these two frequencies the amplitude response is 3dB below the passband response. The ripple is a measure of the flatness in the passband and is defined as a certain amount of allowable variation the response can have [4]. A bandwidth may also be specified where the amplitude response at the upper and lower frequencies is at most 1dB below the passband response. When specified this way the ripple in the passband is also specified. An amplifier can be defined as being used for wideband operation if its bandwidth covers more than one channel of operation.

RF Stability

Designing stable networks is paramount in RF design in order to ensure that no wild oscillations occur that could compromise the system. The two types of stability that exist are conditionally and unconditionally stable networks and both are dependent on frequency range. Conditionally stable networks are only stable under certain loading conditions whereas unconditionally stable networks are stable regardless of the loading conditions. A network may be stable over the desired frequency range and still oscillate due to a large gain outside the operation frequency. Because of this it is good design practice to design an RF network to be unconditionally stable over a frequency range larger than the operation frequency to ensure no oscillations.

According to the Rollett Stability Factor (k), an RF network is defined as unconditionally stable within a certain frequency range if all of the following conditions are met: $k > 1$, $\Delta < 1$, $\Gamma_S < 1$, $\Gamma_L < 1$. If one of these conditions is not met than the network is conditionally stable [3].

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{6}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{7}$$

$$|\Gamma_{IN}| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| \tag{8}$$

$$|\Gamma_{OUT}| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right| \tag{9}$$

Using the above equations and concepts a condition for stability has been derived that can determine the stability of an RF network from one quantity rather than four. This quantity is known as μ and is defined [5] in Eq. 10. When this work discusses RF stability it will discuss this quantity and not the four mentioned above. The other four have been discussed here for the sake of completeness.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - (\Delta)(S_{11}^*)| + |S_{21}S_{12}|} > 1 \tag{10}$$

Simultaneous Conjugate Matching

If a transistor input or output is loaded with any impedance (other than an open or approximate open), the input and output impedance of the transistor changes based on these loading conditions. For example, if the desire is to conjugate match the output impedance of a transistor, once the conjugate match is in place, now the input impedance of the transistor will change. If now after conjugately matching the output impedance of the transistor the input impedance is conjugately matched, then the original output impedance of the transistor is now changed and the original output conjugate match is no longer a conjugate match. This example is a common situation in RF amplifier design and has been solved by the method of simultaneous conjugate matching.

By using the method of simultaneous conjugate matching it's possible to conjugate match both the input and output of a transistor at the same time thus circumventing the situation described above. The simultaneous conjugate match is accomplished by matching the input and output of the impedances of the transistor according to the equations described [3]. Figure 2 shows a general microwave circuit that this simultaneous conjugate match can be used for.

If the input matching network is designed to present an impedance of Z_S (from Eq. 13.) to the input of the transistor and the output network is designed to present and impedance of Z_L (from Eq. 14.) to the output of the transistor, then both the input and output of the transistor will be conjugate matched and maximum power transfer will occur [3].

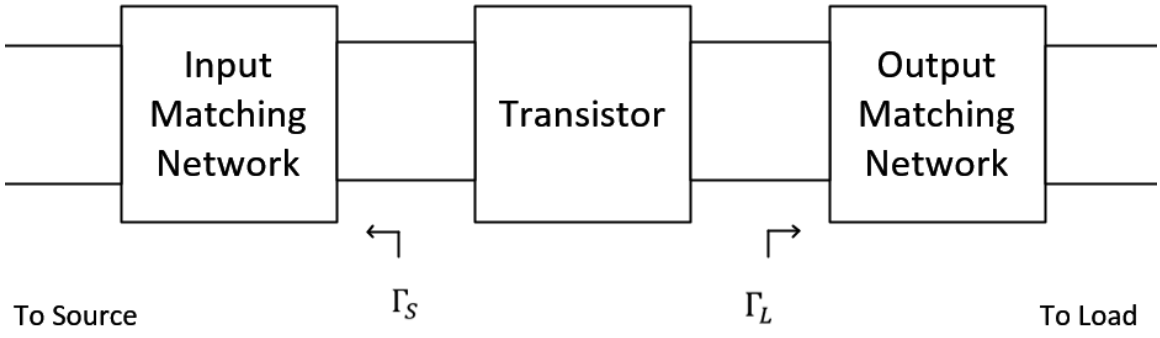

Figure 2: Simultaneous Conjugate Matching Example Network

$$\Gamma_S = \Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{11}$$

$$\Gamma_L = \Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{12}$$

$$Z_S = Z_0 \frac{1 + \Gamma_{MS}}{1 - \Gamma_{MS}} \tag{13}$$

$$Z_L = Z_0 \frac{1 + \Gamma_{ML}}{1 - \Gamma_{ML}} \tag{14}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{15}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{16}$$

$$C_1 = {S_{11}}^2 - (\Delta)(S_{22}^*) \tag{17}$$

$$C_2 = {S_{22}}^2 - (\Delta)(S_{11}^*) \tag{18}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{19}$$

RF Bias Tee

The purpose of the bias network was to provide the DC bias and RF signal to the active device. The network was designed so that the DC bias can be provided to the active device while simultaneously not allowing any RF signal to be fed to the DC input lines. This was done to ensure not only that no RF signal would reach the DC supply, but also to ensure matching networks could be more accurately designed. A traditional quarter wave DC input line would ensure an RF short circuit, but would be impractically long within the specified frequency range. Therefore a simple bias tee network design was chosen to be implemented such as shown in Figure 3.

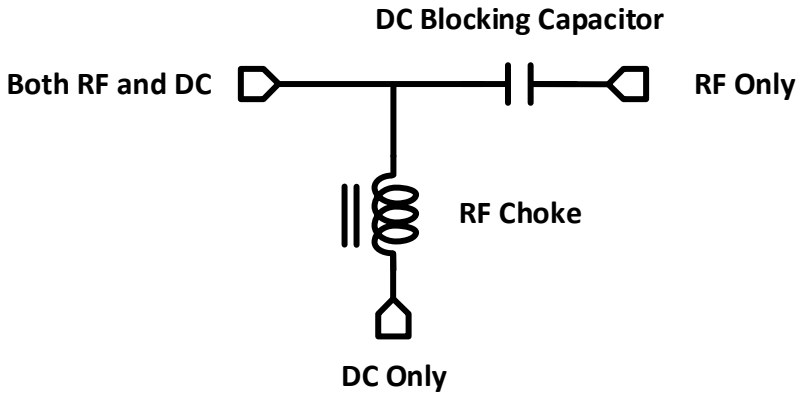

Figure 3: Basic Bias Tee Network

At the output of the bias tee both RF and DC are present so that the active device can be biased and see the RF signal. The RF choke needs to present a large impedance to RF signals in order to ensure little or no RF signal can pass and should therefore be chosen to have as large of a value as possible. The DC blocking capacitor should present a small impedance to the RF signal to ensure the full signal can pass unattenuated and should therefore also have as large of a value as possible. Both components should also have sufficiently high self-resonant frequencies as compared to the operation frequency of the circuit to ensure proper operation.

1dB Compression Point

In an ideal linear amplifier, the amplifier gain would follow a linear trend and the gain of the amplifier would be independent of the input power. However, due to non-linear effects at higher input power levels, the gain reduces as input power is increased past the amplifier's linear range. The 1dB compression point represents the point at which the gain of the amplifier reduces by 1dB from the gain of an ideal linear amplifier and is used as a figure of merit for the linearity of an amplifier or system [6]. It should be noted that other levels of compression such as 3dB or 6dB compression are specified for certain applications, however, the 1dB reduction in gain represents a 10% reduction in the gain and this is considered the first point at which a significant reduction in gain has occurred.

In Figure 4, the extended dotted line represents the gain of an ideal linear amplifier and the solid line represents the actual gain of the amplifier. The point $P_{in,1dB}$ is where the gain has reduced by 1dB from the ideal linear amplifier gain and this is the input 1dB compression point. Either the input or output power level at which the compression has occurred can be specified. When this work refers to the 1dB compression point it is referring to the output power level at which the compression has occurred.

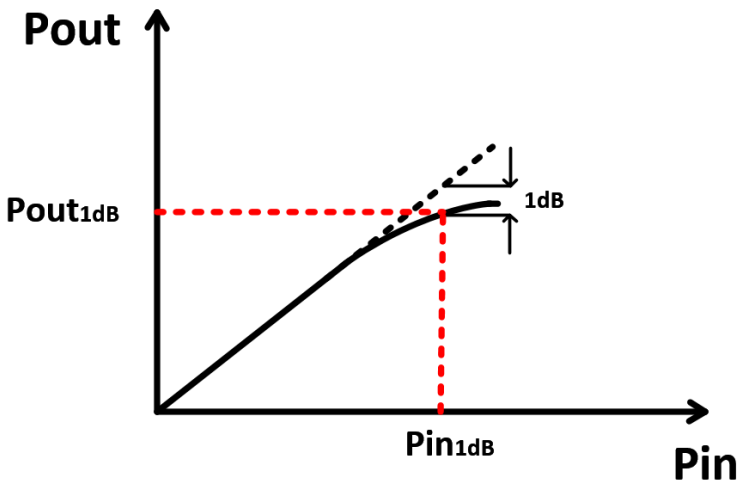

Figure 4: 1dB Compression Point Illustration

Third Order Intercept Point (IP3)

The third order intercept point (IP3) is a measure of the intermodulation due to the third harmonic of an amplifier or system and is a figure of merit of linearity. The IP3 is defined as the input (input IP3, IIP3) or output power (output IP3, OIP3) at which the amplitude of the fundamental frequency (Af_0) and the third harmonic (Af_3) are equal when two equal amplitude sinusoidal signals near the center frequency within the specified frequency range are applied to the input of the DUT [6]. Figure 5 shows an illustration of IP3. When this work refers to IP3 it is referring to the output IP3.

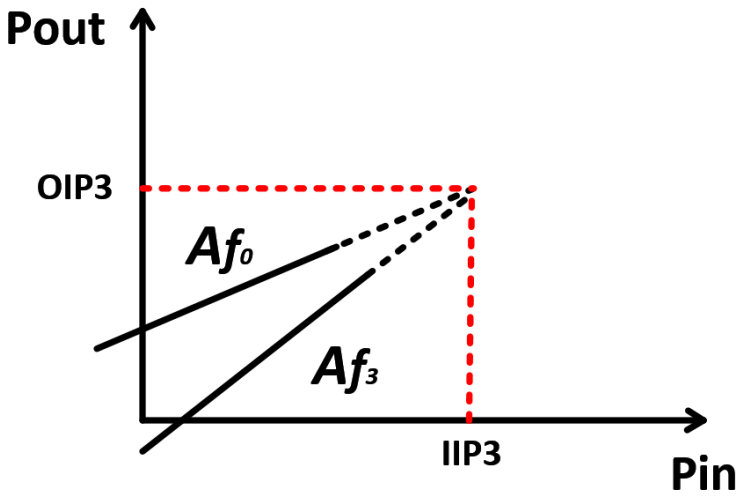

Figure 5: Third Order Intercept Point Illustration

Efficiency

The "drain efficiency" for a PA is defined in Eq. 20 where P_L is the average power consumed by the load and P_{supp} is the average power supply consumption. This drain efficiency expresses how well the supply power is converted into power provided to the load [6]. For example, a PA with an output power of 1W with an efficiency of 25% consumes 4W from the supply.

$$\eta = \frac{P_L}{P_{supp}} \tag{20}$$

Another metric of efficiency used for PAs is power added efficiency (PAE). PAE differs from drain efficiency in that it takes the input signal power into account in defining how well the conversion from the supply power to load power is [6]. PAE is defined in Eq. 21.

$$PAE = \frac{P_L - P_{in}}{P_{supp}} \tag{21}$$

Because the input signal power applied to a PA directly adds to the power provided to the load, PAE would clearly need to be used over drain efficiency to describe the overall PA efficiency in applications with high input signal. Further, it can be seen that for low input power applications the drain efficiency and PAE would be approximately equal.

Conduction Angle PAs

Many PA topologies exist for improving efficiency, providing high linearity, or for increasing output power. These topologies are categorized by classes such as A, B, AB, C, D, E, F, etc. The conduction angle PAs that exist are classes A, B, AB, and C. Conduction angle is defined as the period which the transistor in use is on, where, a conduction angle of 360° (or 2π) is fully on and a conduction angle of 0° the device is fully off [6]. These conduction angle PAs differ from the other classes because they change the bias point of the device to shape the drain current of the transistor in use whereas other classes use methods such as transistor switching or harmonic loading to shape the drain voltage and/or current waveforms. While heavy mathematical derivations exist defining the various classes, this work will provide a basic overview of these conduction angle PAs in this section.

Class A Operation

Class A operation is defined as setting the bias point of the transistor in use to a point where the drain current of the transistor in use is always on and thus has a conduction angle of 360°. In an ideal class A biased PA the output signal waveform is not distorted at all and this class of operation is therefore the most linear among conduction angle PAs. Despite being the most linear conduction angle PA, the maximum theoretical drain efficiency of this class of operation is $\eta = 50\%$ [6]. As the conduction angle is reduced, the linearity suffers but the drain efficiency drastically increases. Figure 6 shows a transistor biased in class A operation.

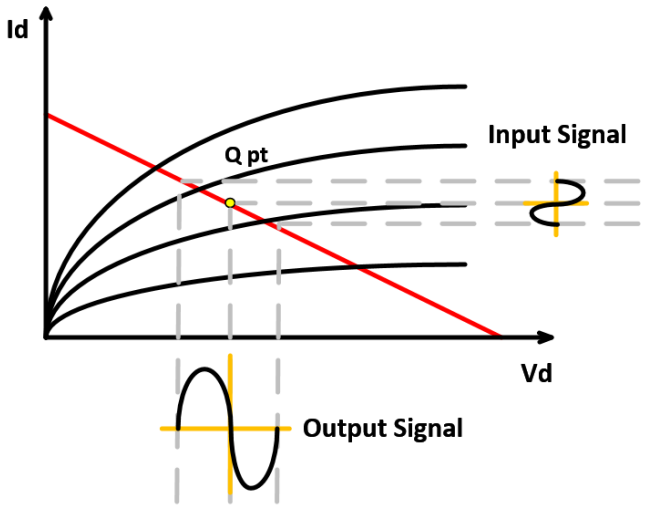

Figure 6: Class A Bias Point

Class B Operation

Class B operation is defined as setting the bias point of the transistor in use to a point where the drain current of the transistor will be on half of the time and has a conduction angle of 180°. In an ideal class B biased PA the output signal waveform would be distorted and therefore not provide linear operation. Despite this non-linear behavior, the maximum theoretical drain efficiency of this class drastically increases from a class A biased device to $\eta = 79\%$ [6]. Figure 6 shows a transistor biased in class B operation.

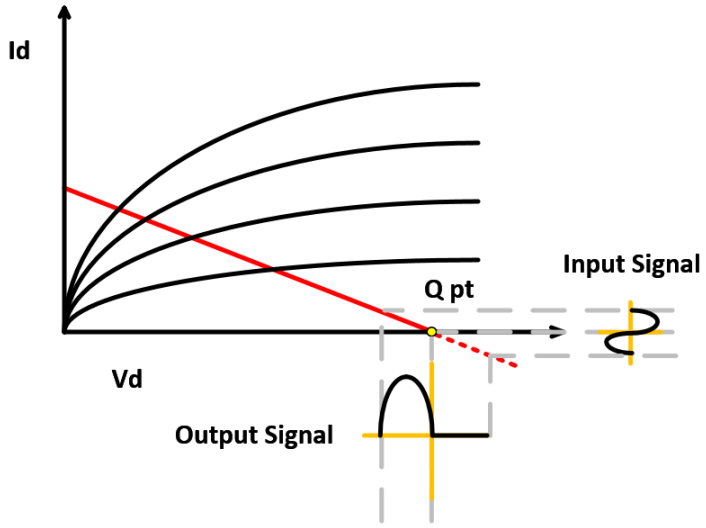

Figure 7: Class B Bias Point

Class AB Operation

Class AB operation is defined as setting the bias point of the transistor to be at a point between class A and class B operation and therefore the conduction angle is between 180° and 360°. An ideal class AB biased PA offers a drain efficiency between that of a class A and class B biased device at $\eta = 50 - 79\%$ [6]. Because of the favorable tradeoff between linearity and efficiency, this is a very commonly used PA bias. Figure 8 shows a transistor biased in class AB operation.

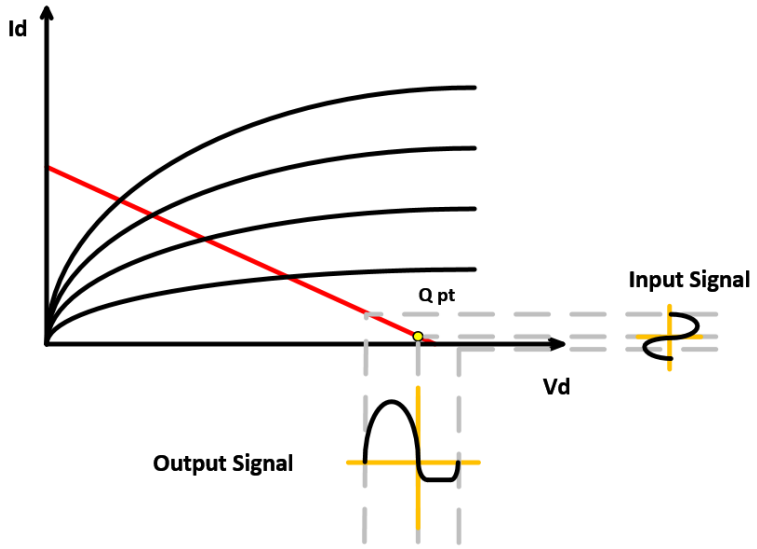

Figure 8: Class AB Bias Point

Class C Operation

Class C operation is defined as setting the bias point of the transistor to a point where the transistor in use is on less than half the time and the conduction angle is less than 180°. A device biased in class C operation is the most non-linear conduction angle PA and is no longer used in practical design. The maximum theoretical drain efficiency of this class is the highest among conduction angle amplifiers with the drain efficiency approaching $\eta = 100\%$. However, this maximum drain efficiency implies that the device is off and would therefore provide no power and is therefore not useful [6]. Figure 9 shows a transistor biased in class C operation.

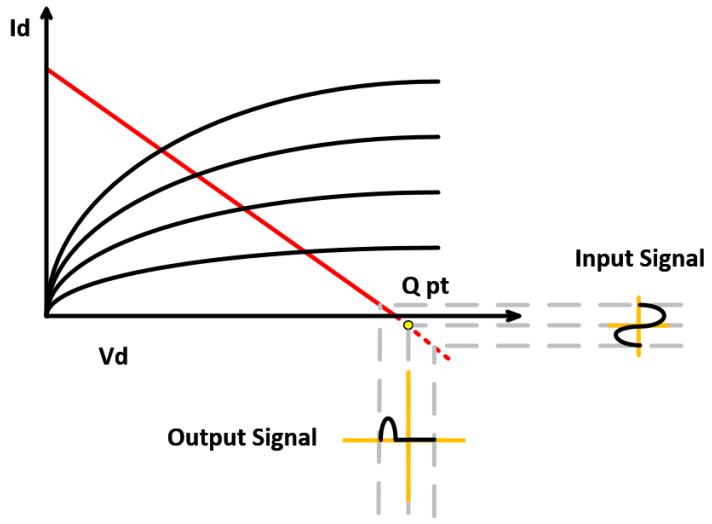

Figure 9: Class C Bias Point

Heat Sink Thermal Considerations

The purpose of using heat sinks in electronics is to keep the junction temperature of the active devices used below the maximum allowable junction temperature in order to ensure the devices do not fail. Careful selection of a heat sink ensures reliable operation under high power or high temperature applications.

The classic analogy to understand the thermal analysis used for heat sink selection is Ohm's law. Ohm's law is shown in Eq. 22. and the equation used in the selection of a heat sink is shown in Eq. 23 [7]. In thermal analysis, the thermal system is referred to as the thermal circuit just as in electrical analysis the electrical system is referred to as an electrical circuit.

$$Voltage\ (V) = Current\ (A)\ x\ Resistance\ (\Omega) \tag{22}$$

$$Temperature\ (°C) = Power\ (W)\ x\ Total\ Thermal\ Resistance\ (R_{\theta XX}) \tag{23}$$

Using these equations in conjunction with Figure 10 it's possible to see that temperature is analogous to voltage, power is analogous to current, and thermal resistance is analogous to resistance. The power dissipated by the device (noted 'P' in Figure 10) acts as a current source and this generated power travels through the thermal circuit as a current travels through an electrical circuit. As this power passes through each thermal resistance (noted '$R_{\theta XX}$' in Figure 10), a temperature (noted 'T_{XX}' in Figure 10) is generated just as when a current passes through a resistor it generates a voltage [7].

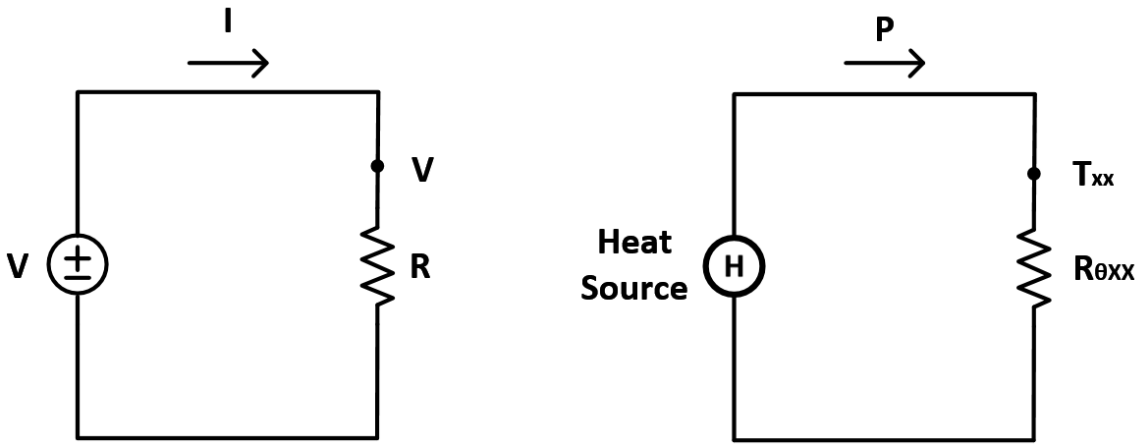

Figure 10: Example Thermal Circuit

When selecting a heat sink for an application Eq. 23. is rearranged and expanded to include more terms [7]. This expanded equation is shown in Eq. 24. If the power dissipated, ambient temperature, and thermal resistances are known, then it's possible to calculate the device junction temperature. This equation implies that by keeping the thermal resistance as low as possible and dissipating a low power it's possible to keep the device junction temperature low.

$$P_D = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}} \tag{24}$$

P_D: *Power disipated in the device* $[W]$

T_J: *Junction temperature* $[°C]$

T_A: *Ambient Temperature* $[°C]$

$R_{\theta JC}$: *Junction to case thermal resistance* $[°C/W]$

$R_{\theta CH}$: *Case to heat sink thermal resistance* $[°C/W]$

$R_{\theta HA}$: *Heat sink to ambient thermal resistance* $[°C/W]$

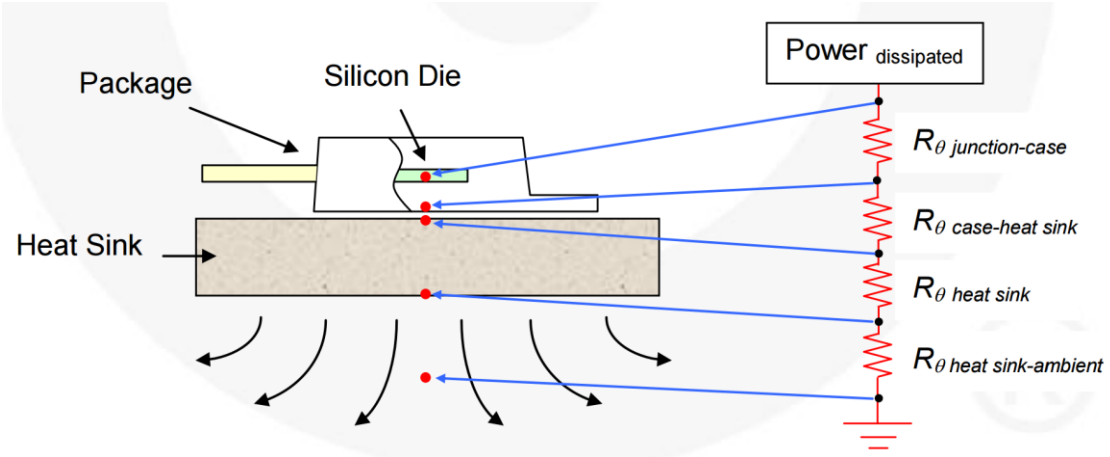

Figure 11: Example Package and Heat Sink Diagram [8]. Used Under Fair Use, 2015.

As both Eq. 24. and Figure 11 show, the heat sink to ambient $R_{\theta HA}$ is not the only thermal resistance that needs to be accounted in the selection of a heat sink. The junction to case thermal resistance $R_{\theta JC}$ depends on the package of the selected device, cannot be manipulated, and must be included in calculations. The case to heat sink $R_{\theta CH}$ represents the gap between the active device and heat sink. At an atomic level there exists an air gap between the device and heat sink which can contribute a non-negligible thermal resistance due to the fact that air is a good insulator. In order to reduce this resistive contribution, either more pressure can be applied mounting the device to the heat sink or a thermal paste can be selected.

High Temperature Applications of Semiconductor Devices

This section provides an overview of research on semiconductor materials used at high temperatures. A survey of literature showed that silicon germanium (SiGe), gallium nitride (GaN), silicon carbide (SiC), and gallium arsenide (GaAs) technologies appeared to be able to operate at high temperatures and these are the technologies discussed. The purpose of this background research was to make an informed decision on selecting a material that would be able to withstand high temperature operation without significant degradation in performance. Not only this, but the research should provide evidence that the technology does not degrade in high frequency performance as temperature increases.

Despite being low bandgap materials, SiGe and GaAs have both been proven to operate at high temperatures. Existing research on the subject of high temperature applications of SiGe and GaAs discusses how material properties and important design parameters change with increasing temperature. For the purpose of this research the operation temperature in these works was of particular interest. In summary it appeared that SiGe and GaAs would not the best choice for high temperature high frequency applications as they appeared to degrade too much under these conditions.

Due to its high bandgap and high electron mobility SiC has been used in high temperature high frequency applications. Research suggests that this material is well suited for this operation without significant degradation in performance and has been studied for its high temperature properties for years. Existing research discusses both high speed switching and analog circuit applications of SiC in relation to high temperature.

GaN technology has been known to be able to operate at high temperatures and be used for high frequency applications for many years. In addition to this, it is not limited to only high frequency applications, but is also used for switching and high power applications. There is still much research on the use of GaN for high temperature applications to this day. There is overwhelming research and evidence that GaN can be used for high temperature applications.

Research on High Temperature Applications of SiGe

Despite being generally recognized as not a viable option for high temperature applications due to its low bandgap energy, SiGe has been proven in literature to show that it can be used for such applications. T. Chen et al. demonstrated that SiGe off-the-shelf HBTs that are not optimized for high temperature operation are able to operate as high as 300°C [9]. The SiGe HBT used in the investigation was a SiGe HBT BiCMOS which integrated 0.20µm, 1.8V BV_{CE0}, 120GHz f_T, and 4.3V BV_{CE0}, 35GHz f_T together with 0.18µm, 1.8V Si CMOS devices. Gummel characteristics, f_T, and F_{MAX} were all measured at were taken for the device at 25°C and 300°C. f_T degraded as temperature was increased from room temperature to 300°C by approximately 48% with it being measured at 25°C to be 125GHz and estimated to be 65GHz at 300°C [9]. F_{MAX} also degraded as temperature was increased from room temperature to 300°C by approximately 38.5% with it being measured at 25°C to be 122GHz and estimated to be 75GHz at 300°C [9]. The current gain β for the device decreased as temperature was increased and the off-state leakage current was measured to be 1.6µA at 300°C [9].

Even further shown in the past decade G. Wang et al. investigated RF (at 6GHz) power performance of SiGe power HBTs at a junction temperature of 160°C to find that at this temperature performance degraded [10]. The devices used in the investigation were manufactured in a commercial SiGe BiCMOS process where the HBT had 40 0.9x0.16 µm fingers. F_{MAX} for the device was found to decrease from 26GHz at room temperature to 12GHz at 160°C. At the operation frequency of 6GHz, the small-signal power gain decreased from 21dB at room temperature to 10.5dB at 160°C and the linear gain decreased from 15dB to 10dB at 160°C [10]. The peak PAE was measured to be approximately 28% at room temperature and 6.8% at 160°C [10]. The power performance significantly degraded for this SiGe device but could be used for specific applications.

Other research into the effects of high temperature on SiGe were investigated by M. Bellini et al. This team developed a SiGe HBT using a BiCMOS-on-SOI process and investigated the device characteristics at room temperature and 330°C [11]. f_T degraded as temperature was increased from room temperature to 330°C from approximately 32GHz to 11GHz. F_{MAX} also was found to degrade as temperature was increased from room temperature to 330°C from approximately

40GHz to 12GHz. The current gain β for the device was also found to decrease as temperature was increased [11].

Research on High Temperature Applications of GaAs

Like SiGe, GaAs has a low bandgap energy which would suggest it may not be the best choice for high temperature operation. Despite this fact, there has been literature showing GaAs used for high temperature applications. One such study undertaken by K. Frickle et al. demonstrated an analog op amp able to withstand operation at 200°C without significant degradation in performance using AlGaAs/GaAs/AlGaAs DHBT technology [12]. The fabricated device exhibited high thermal reliability after performing a storage test at 400°C for 1000h showed no degradation in ohmic contact resistance. The measured open loop gain of the op amp was 49.5dB at room temperature and 35.8dB at 200°C [12].

In addition to analog circuits designed for high temperature applications, GaAs has also been used to design high frequency high temperature power amplifier. F. Y. Columb et al. demonstrated a PA operating in Q-band (42-46GHz) with record power levels measured at an ambient temperature of 90°C [13]. The technology used was a GaAs pHEMT fabricated on Raytheon's double-recess, self-aligned, 0.2μm T-gate power inGasAs/GaAs pHEMT process. At room temperature the measured output power for the device was 4W with an efficiency of 20% and an output power of 3W with an efficiency of 17% at 90°C [13].

Research on High Temperature Applications of SiC

With a high bandgap energy, SiC has been a clear choice for various high temperature applications for some time. N.S. Rebello et al demonstrated the advantages of using SiC over Si or GaAs by undertaking a comprehensive study of how important design parameters change over temperature for SiC, Si, and GaAs and using these measured results to design / simulate an analog op amp at 500°C with SiC technology [14]. The SiC MOSFETs used for the study were fabricated by CREE on 2 pm p-type epitaxial layers grown on Si-faced n-type wafers. The study measured threshold voltage, electron mobility, ON/OFF characteristics, drain current, leakage

current, and gate transconductance from room temperature to 300°C for SiC and compared it to Si and GaAs. It found that for the SiC device that threshold voltage decreases linearly from room temperature to 300°C, electron mobility first increases with temperature then decreases, leakage current is much lower due to the higher bandgap energy, and that transconductance increases at first and then decreases [14]. The SiC device performed the best with temperature as its leakage current was significantly lower than the Si and GaAs devices. Using the measured results at high temperatures, an NMOS SiC analog op amp was designed and simulated at 250°C and 500°C. The voltage gain decreased from 45dB to 39dB between 250°C and 500°C, the power consumption decreased from 0.56mW to 0.33mW, and the CMRR stayed the same between temperature at 28dB [14].

Just this past year another application of SiC has been implemented for high temperature operation. This application of SiC has been a novel high power 3 phase SiC inverter module demonstrated by Woo et al. This work uses 6 SiC DMOSFETs from CREE integrated into one package and the novelty of this work comes from the cooling of the module which uses a dual sided cooling technique with a top and bottom heat spreader [15]. Using this technique in conjunction with novel solutions on interconnects the module was able to withstand high junction temperature operation up to 220°C without degrading in performance [15].

Another study of the high temperature applications of SiC involved improving packaging technology to allow for increasing operation temperature of a power module. B. Grummel et al introduced a new power module packaging concept using SiC technology that allowed for operation at 300°C [16]. The group developed a half-bride circuit for the purpose of power electronics circuitry using this novel packaging technique. The new module is more simplified than previous implementations as it has only three elements including leadframes, SiC chips, and encapsulation [16]. It allows for high current and high power capability and has reduced package parasitic impedances which allow for lower power loss. The I-V characteristics of the device were taken from room temperature to 300°C and it was shown that the device was fully function at the elevated temperature but appeared to turn on at lower voltages as temperature was increased [16].

Research on High Temperature Applications of GaN

The high temperature applications of GaN have been recognized for years as research on the topic was investigated as far back as two decades. In 1995, M.W. Shin et al. demonstrated in with simulated and measured results that GaN could be a viable option for high temperature high frequency power applications [17]. Under class A bias conditions this team measured peak PAE, output power, and gain of a PA at room temperature to be respectively approximately 50%, 39dBm, and 20dB. It was possible to simulate performance at 500°C by calibrating the simulation software using the measured results at room temperature. The simulated peak PAE, output power, and gain of the PA at 500°C was found to respectively be approximately 33%, 35dBm, and 13dB [17].

Just several years after this publication S. Yoshida et al. investigated the reliability of GaN MESFETs at high temperatures in 1998. The MESFET used for the study had Au/Pt as a Schottky gate and Ti/Al as a source drain [18]. It was found that after heating the device at 400°C for 1000 hours no degradation of the metal-semiconductor interface was observed under the transmission electron microscope (TEM). Also, after heating the device at 400°C for 1000h a life test of the FET was conducted at 350°C by continuous current injection [18]. I/V characteristics before and after heating did not significantly and also the ohmic materials did not diffuse into the GaN layer at the extreme temperature thus confirming that this GaN device can be used reliably at high temperatures.

In recent years further research has been done on high temperature applications of GaN. Recently in 2011 X. Liu et al. designed a bootstrapped comparator which operated with a single-polarity power supply which was fabricated on an $Al_{0.26}Ga_{0.74}N$/GaN HEMT sample grown by MOCVD on a 4-in silicon substrate [19]. The important parameters of the comparator were measured at both room temperature and at 250°C and it was found that there was degradation in performance with increasing temperature. The measured voltage gain of the comparator at room temperature was 79V/V and 40V/V at 250°C. The unity gain bandwidth of the design at room temperature was 206MHz and 84MHz at 250°C [19].

GaN technology is not limited to high frequency applications but can also be used for fast switching purposes. Just this past year Z. Xu et al. demonstrated a GaN device that could be used for high voltage, high efficiency, and high temperature applications [20]. For this work, a 600V /

11A GaN HEMT from Transphorm was used and it was shown that the di/dt was able to reach 9.6 A/ns and dv/dt was able to reach 140 V/ns. This device was used for the application of fast switching that was able to withstand up to 200°C without degrading in switching speed or switching energy [20].

Another switching application of GaN which also demonstrated high temperature performance was shown by C. Liu et al. just this year [21]. This work uses a 650V cascade GaN power device from ON Semiconductor to show dynamic Rds_{ON}, leakage currents, and other parameters measured at a case temperature 150°C for 1000 hours and at room temperature. It was shown that the dynamic Rds_{ON} increased with temperature by less than 20% at 200°C. In addition to this performance the measured leakage current at 150 °C and 650 V is less than 100 nA [21]. While the case temperature was measured at 150°C the junction temperature was measured to be approximately 250°C.

State-of-the-art packaging techniques for GaN HEMTs have been developed to allow for high temperature and high power applications. One such advanced packaging technique for GaN HEMTs has been developed by A. Bajwa et al. [22]. This team has characterized the die-attachments used for the developed HEMT up to 450°C for its high-temperature stability. After assembling the package, electrical, thermal and thermomechanical effects were measured and it was found that the final assembled and packaged HEMT could survive up to 480°C [22].

Clearly, there have been many investigations into the effects of high temperature in GaN ranging from high frequency to high voltage applications. These studies have shown GaN is able to withstand high temperature operation without significant degradation in performance.

Thermal Characteristics in Semiconductor Devices

This section discusses semiconductor material properties that are important to consider in choosing a device to be used in high temperature operation and how they relate to temperature.

Band Gap (E_g) and Temperature

An important material property related to high temperature operation for semiconductor devices is the band gap energy (E_g) of the technology used. It can be found from Eq. 25 that as operation temperature is increased, the band gap energy of the semiconductor is decreased [23].

$$E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \tag{25}$$

$T: Temperature\ [K]$
$E_g: Band\ gap\ energy\ [eV]$
$E_g(0): Band\ gap\ energy\ at\ absolute\ zero\ on\ the\ kevin\ scale [eV]$
$\alpha_E\ and\ \beta_E: Material\ specific\ constants\ /\ fiting\ parameters [unitless]$

When the band gap energy of a semiconductor is low, it means that it takes less energy for electrons to travel from the valence band to the conduction band and as the temperature increases the electrons in the valence band will be provided energy. Therefore, under high temperature operation, because the band gap energy is decreased and the electrons are provided energy from the heat, electrons can more easily travel from the valence band to the conduction band of the device and turn the device on more easily causing a high leakage current. This is clearly undesirable as it can lead to the device unreliably being turned on under high temperature conditions.

For these reasons it is clear that a wide band gap semiconductor would operate best under high temperature conditions due to the fact that the band gap energy is much higher and therefore requires the electrons to have much more energy to turn on the device. Wide band gap is a subjective term but is generally recognized as a semiconductor material having a band gap greater than 1.5eV [24].

Electron Mobility (μ_N) and Temperature

For high temperature operation it is also desirable for a material to have a high electron mobility (μ_N). The relationship between electron mobility and temperature is derived empirically and changes among different materials. However, among most materials, as the operation temperature is increased the electron mobility of the semiconductor is decreased [25]. For example, the relationship for silicon is shown in Eq. 26.

For Silicon $$\mu_N = T^{-2.4} \tag{26}$$

Electron mobility is an important property in a semiconductor as it is directly related to the device's drain current (i_D) in any mode of operation excluding cutoff. Because drain current and the devices transconductance (g_m) are related, electron mobility also effects the device's transconductance. For MOSFETs, the relationship between electron mobility and drain current in the triode and saturation regions are shown in Eq. 27. and Eq. 28 [26].

Triode Region $$i_D = \mu_n C''_{OX} \frac{W}{L}\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right) v_{DS} \quad for\ v_{GS} - V_{TN} \geq v_{DS} \geq 0 \tag{27}$$

Saturation Region $$i_D = \frac{\mu_n C''_{OX}}{2} \frac{W}{L} (v_{GS} - V_{TN})^2 \quad for\ v_{DS} \geq (v_{GS} - V_{TN}) \geq 0 \tag{28}$$

The relationship between the electron mobility, drain current, and transconductance for MOSFETs is shown in Eq. 29 [26].

$$g_m = \frac{di_D}{dv_{GS}}|_{Q-pt} = \mu_n C''_{OX} \frac{W}{L} (V_{GS} - V_{TN}) = \frac{2I_D}{V_{GS} - V_{TN}} \tag{29}$$

Due to these relationships, electron mobility effects the device's cutoff frequency (f_T) for both BJTs and MOSFETs and therefore plays a key role in determining the high frequency behavior of the material. For MOSFETs, the equation used to determine the cutoff frequency is shown in Eq. 30 [26].

$$f_T = \frac{g_m}{2\pi\,(C_{GS} + C_{GD})} \tag{30}$$

A semiconductor material with a high electron mobility is desirable for high temperature high frequency applications because of the direct effect it has on the high frequency properties of the device (f_T). It can be said that as temperature increases, the cutoff frequency decreases and by choosing a semiconductor material with a high electron mobility this temperature effect can be reduced.

Thermal conductivity (k)

Another important semiconductor material property that is important to consider for high temperature operation is thermal conductivity (k) of the material. For high temperature operation it is desirable for a semiconductor material to have a high thermal conductivity to ensure that the thermal resistance of the die itself is as low as possible. Thermal conductivity and thermal resistance are related by Eq. 31 [27].

$$R_{TH} = \frac{d}{k\,A} \tag{31}$$

d: $Thickness$ $[m]$

k: $Thermal\ conductivity$ $\left[\frac{W}{m\,K}\right]$

A: $Cross\ sectional\ area$ $[m^2]$

As discussed previously, the lower the thermal resistance present is, the higher the power dissipated can be and the lower the junction temperature will be. Therefore, choosing a semiconductor material with a high thermal conductivity will ensure reliable operation at high temperature.

Maximum Junction Temperature (T_{JMAX})

One can conclude from the equations discussed in Heat Sink Thermal Considerations that in order to operate at high temperatures the main limiting factor is the maximum rated junction temperature (T_{JMAX}). The semiconductor material is not the only factor in determining the maximum junction temperature of a device [28]. The melting temperature of the device material, the maximum thermal runaway temperature, the melting point of the solder used for the die-attachment, and the high temperature operating life (HTOL) are all factors which determine the maximum rated junction temperature given in a device datasheet [28].

Semiconductor Material Properties Related to High Temperature

Table 2 details several semiconductor materials and their properties that are important to consider in high temperature operation.

Property	Silicon (Si)	Gallium Arsinde (GaAs)	6H-Silicon Carbonide (6H-SiC)	4H Silicon Carbonide (4H-SiC)	Gallium Nitride (GaN)
Bandgap, $E_g(eV)$	1.12	1.43	3.06	3.26	3.45
Electron Mobility, $E_c(kV/cm)$	300	400	2,500	2,200	2,000
Thermal Conductivity, k, σ_c, λ $(W/cm \cdot K)$	1.5	0.46	4.9	4.9	1.3

Table 2: Important Temp. Material Properties. [29]. Used Under Fair Use, 2015.

Due to its wide band gap, high electron mobility, and high thermal conductivity properties and supporting research showing its numerous applications under high temperature operation, it was decided that GaN would be the best candidate for high temperature high frequency operation.

Current Research on High Temperature PAs

High temperature PAs is not limited to just operating the device at a high ambient temperatures. There have been investigations into materials that allow for high temperature operation that have been used to design PAs. Other works have investigated operating PAs over a wide range of temperatures such that there performance stays the same over this wide temperature range. The following section details current and past research on high temperature RF PAs.

An evaluation of effects of high temperature on PA performance was undertaken by C. Yu et al. who researched the effects of electrical and temperature effects on a class AB PA from 45°C to 125°C [30]. The group found that the output power, efficiency, third order intercept point, and adjacent channel power ration (ACPR) all degraded as temperature was increased. The devise tested were 0.16x20 μm^2 nMOSFETs with thin SiO_2 thickness of 2.4 nm. The study reported that the device changed operating class from AB to B and eventually to C due to the decrease in threshold voltage as temperature was increased. After two hours of stress at 125°C the amplifier's ACPR degraded from 43dB to 39dB and the IIP3 degraded from 5.5dBm to -1.35dBm.

Yet another study on the effects of temperature on PA performance was performed by K.M. Chen et al. This work explored the effect of temperature on the small-signal power gain, PAE, and linearity for various bias voltages on a SiGe HBT operating at 2.4GHz biased in class A operation [31]. The devices used for the research were fabricated in a 0.24 μm high-voltage SiGe HBT process with high beta and cutoff frequency of 23 GHz. The power performance was measured at room temperature, 50°C, and 75°C and it was found that as temperature was increased, PAE degraded, power gain decreased, and linearity improved. From room temperature to 75°C under a bias condition of V_{BE} = 0.73V, PAE was found to decrease from approximately 45% to 35%, power gain decreased from approximately 23dB to 20dB, and IIP3 increased from -16dBm to -10dBm [31]. At a bias condition of V_{BE} = 0.84V, from room temperature to 75°C, PAE was found to decrease from approximately 39% to 29%, power gain decreased from approximately 23dB to 18dB, and IIP3 increased from 4dBm to 16dBm [31].

In addition to PAs able to operate at high ambient temperatures, temperature compensation techniques have been investigated in RF PAs. S. Chen et al examined several gate bias circuit topologies and their application to control the gate voltage of a class AB PA in order to provide

stable output power over a wide range of temperatures [32]. The class AB PA was designed using TSMC 0.18µm SOI technology at an operation frequency of 5.2GHz with a main transistor of 64 finger of 4.36µm each. The group showed that by using an adaptive gate bias opposed to a constant gate bias it was possible to have less sensitivity to operation temperature and yield a more constant output power. The output power changed by -8% from -40°C to +120°C using the adaptive gate bias opposed to changing by -16% using a constant gate bias. The PAE changed by approximately 5% using the adaptive gate bias opposed to changing by approximately 9% using a constant gate bias condition [32].

C.H. Liao et al. contributed to the study of temperature compensated PA design by designing a 14GHz temperature compensated PA able to generate an output power of 20W with 34dB gain [33]. The proposed design uses a four stage approach with one commercial medium-power MMIC and three GaAs transistors. The group achieves this compensation by sensing when the PA module is heated and adjusting the drain current of the power transistors accordingly by regulating the gate bias of these transistors controlled via an op amp control circuit. The group showed that they were able to compensate for constant output power over a temperature range of 40°C to 80°C [33].

In addition to temperature compensation techniques for PAs and measuring high temperature effects on PA performance, other research has gone into developing materials able to withstand high temperatures. Yamaki et al. demonstrated a GaN HEMT die able operate at a junction temperature of 280 °C for an extended period of time [34]. Using this designed die, the group implemented an inverse class F PA which has an output power of 200W and achieves high efficiency of up to 65.2% at this temperature [34]. A high temperature operating life (HTOL) test was performed to find that after 5000 hours of being exposed to 280°C the output power degraded by 0.5dB. Thermal conditions of the die / package (such as thermal resistance, maximum junction temperature, ambient temperature) are not stated in and the cooling technique used is not stated.

Chapter 3

Introduction

This chapter provides details of the design procedure / concerns for this project. The system overview and specifications for the design are discussed first and following this the final schematic for the design is shown. Once the specifications and final design are discussed, the concerns relating to the selection of the transistor used in the design is discussed. Following this, thermal design considerations related to the device chosen / power level chosen and the final thermal design used are explained. After this, a discussion of how important design parameters for the chosen transistor change as temperature is increased is discussed. Following this explanation, a discussion of how the bias point for the design was selected is undergone. After all important information regarding the active device is discussed, passive devices and interface materials selected for high temperature operation are discussed. Once the reader has an understanding of how the active, passive, and interface materials used in the design were selected, the design procedure is discussed. This section starts with a discussion of how the bias network was designed and then discusses the design of the stabilization network employed in this design. The chapter is concluded with a discussion of how the matching networks for the PA were selected / designed, how the design was prototyped, and finally the fine tuning needed for the final design.

System Overview

The power amplifier was designed for the down-hole communication system shown in Figure 12. The system design is for the RF modem which was used as an interface between the tools (which operate at baseband) and the coaxial cable. The PA needed to operate over the entire bandwidth of $RF_{Band\#1}$ and $RF_{Band\#2}$ from 230.5 MHz to 285.5 MHz. Figure 13 shows the system block diagram and where the in the system the PA is placed.

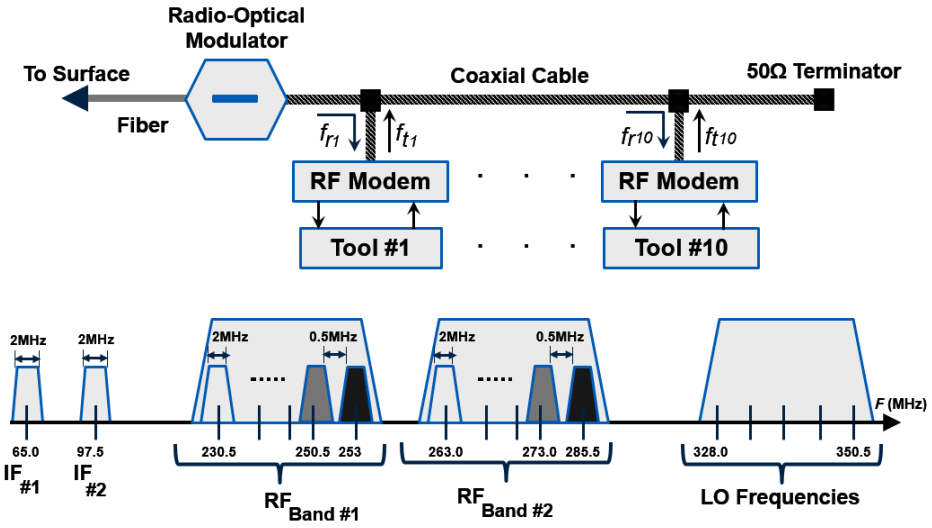

Figure 12 : System Overview for RF Modem

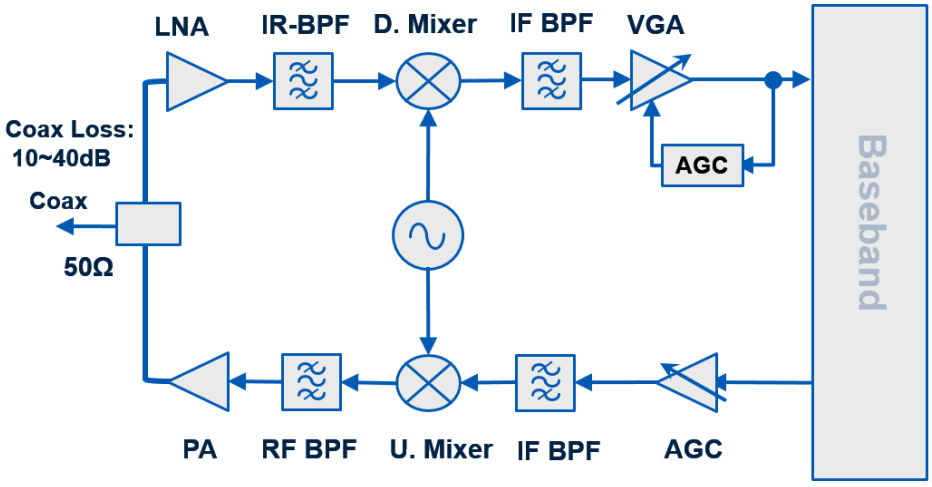

Figure 13: System Block Diagram for RF Modem

Specifications

In addition to operation at high temperature, the downhole system employs linear modulation scheme (FDMA) and wide bandwidth for increasing bit rate and spectrum efficiency. This requires the PA to process high data rate non-constant envelope signals. Therefore, the linearity and operation temperature were the most important specifications for this design. Because power lines provide the power to the downhole electronics, the PAE was not an important design requirement and was not specified or designed for, however, it was measured for completeness. As no digital pre-distortion (DPD) was employed in the system, class A operation was chosen for providing linear performance. Class A operation was chosen despite its high power consumption because of these linearity requirements and the bias level was carefully chosen with power and thermal constraints in mind as will be described.

Design Parameter	***Design Requirement***
Operation Temperature	230°C
Gain	> 15 dB
Gain Ripple	1 dB
Input Return Loss (IRL)	> 10 dB
Output Third Order Intercept (OIP3)	> 35 dBm
Output 1dB Compression	> 25 dBm
Operation Frequency	225 MHz – 285.5 MHz
Peak PAE	Not Specified
Stability (in band)	Unconditionally Stable

Table 3: List of Specifications

Schematic Diagram of the Proposed PA

Figure 14 shows the schematic diagram of the proposed PA.

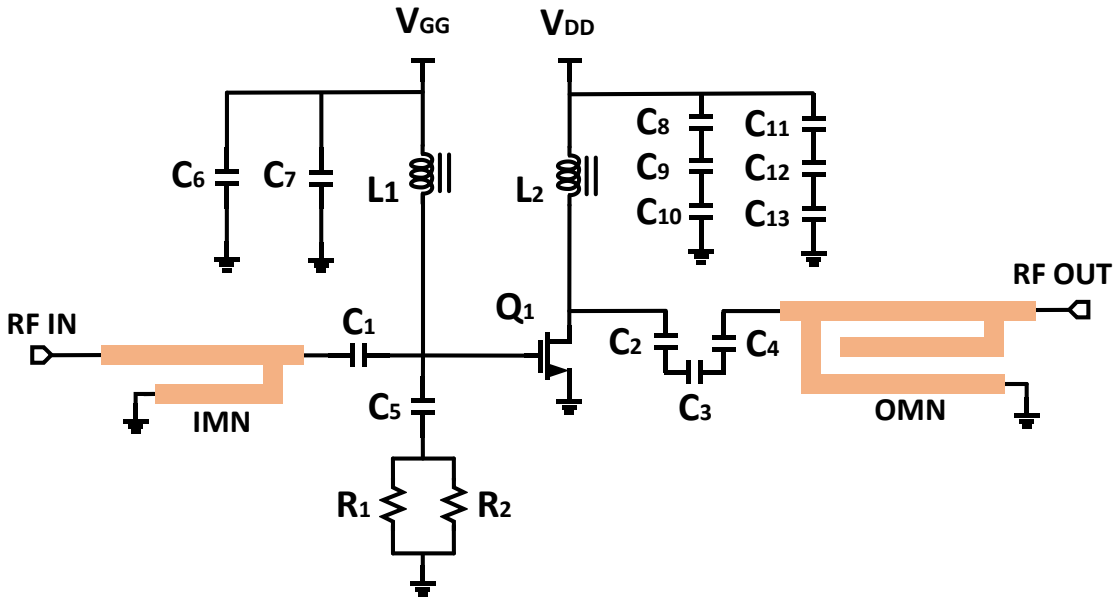

Figure 14: Schematic Diagram of Proposed PA

Together, C_1, C_2, C_3, C_4, L_1, and L_2 form the on-board bias tee for the PA. C_1 through C_4 are the DC blocking capacitors for this network. The reason there are three blocking capacitors (C_2, C_3, C_4) at the output of the active device is because the maximum voltage rating (11V) on the capacitors was lower than the drain voltage (28V). L_1 and L_2 are RF chokes used to ensure little to no RF signal will be present at the input of the DC voltage supplies.

Despite the low DC power dissipation at the gate of the active device, C_5 is used to ensure little to no DC power dissipation across R_1 and R_2. Both R_1 and R2 are used for RF stability and should only have RF power dissipated across them. The purpose of using two resistors in parallel is to reduce the power dissipation across these resistors.

C_6 through C_{13} are bypass capacitors used to ensure an RF short circuit in the specified frequency range and also that a smooth DC voltage is applied the gate and drain of the active device. Just as is the case with the output blocking capacitors (C_2, C_3, C_4) the purpose of having six capacitors to form the output bypass network (C_8 through C_{10} and

C_{11} through C_{13}) rather than using two capacitors like at the input is because of the voltage ratings of the capacitors used.

IMN and OMN are the input and output matching networks for the PA. They are used to present the proper impedances for simultaneous conjugate matching to the input and output of the active device. The IMN is also designed to have a low IRL in order to ensure minimal reflections in preceding circuitry in the system.

Table 4 below shows the component number, value, manufacturer, and summarizes the function of each component from the schematic diagram in Figure 14.

Component Number	Value	Manufacturer	Function
C_1, C_2, C_3, C_4, C_5	1 µF	IPDiA	DC Block
C_6, C_8, C_9, C_{10}	100 pF	IPDiA	Bypass
C_7, C_{11}, C_{12}, C_{13}	0.1 µF	IPDiA	Bypass
R_1, R_2	100 Ω	Vishay	Stability
L_1, L_2	1 µH	Coilcraft	RF Choke
Q_1	3028-FL	Qorvo	Amplifier

Table 4: Component Values, Manufacturer, and Function

This is a linear PA and operates in class A with a high gain and high output compression level for this application. As per specification, the input signal will not exceed a power level of $RF_{in} = 0\ dBm$ and the PA is used to amplify this small signal to an appropriate level for transmission across the lossy RF coaxial cable. Despite the small signal input and small signal operation, this PA is able to operate without compressing up to an input power of approximately 12 dBm.

Selection of Active Device Candidate

After deciding that GaN could be used for high temperature high frequency applications, the next step in the process was finding a COTS GaN transistor that be used for the design. The two main deciding factors in choosing the active device were its high temperature capabilities and its high frequency capabilities. If both these conditions were not met then another active device needed to be chosen.

From a thermal standpoint as described in Chapter 2, in order to operate at an ambient temperature of 230°C the active device package needed to have both a low junction to case thermal resistance and a high junction temperature. Because the desired ambient temperature was 230°C it was necessary to find a device whose maximum junction temperature was sufficiently higher than 230°C. If the junction to case thermal resistance was too high or the junction temperature was too low then the device would not able to operate as reliably at the desired ambient temperature.

From an RF standpoint, the active device needed to have a high gain in the specified frequency range as well as high linearity parameters (IP3 and 1dB compression). These RF specifications were more difficult to meet because most GaN transistors are rated to operate at gigahertz frequencies; not at the relatively low frequency operation of this PA. Not only this, but because operation at high ambient temperatures is not common in electronics, datasheets for RF transistors only specify important design parameters such as s-parameters, gain, or linearity parameters at room temperature (25°C) and 85°C. This would mean that whatever device was chosen would need to be measured at 230°C before making a final decision of whether or not the device could be used for the design.

After searching for a device that could meet both thermal and RF requirements at 85°C Qorvo's T2G6003028-FL GaN on SiC HEMT was the chosen candidate to be tested at the desired ambient temperature of 230°C. If after being tested at 230°C it showed it could be used to meet the PA specifications then this active device would be chosen.

The datasheet listed the gain in the specified frequency range (at 85°C) and appeared to meet the specifications [35]. The 1dB compression level was not listed at the desired frequency range but instead at 3GHz. It was assumed and later confirmed in measurement

that this high compression level would hold true at the specified frequency range as discussed in Chapter 4. The IP3 was not listed at all in the datasheet but it was correctly assumed that the IP3 would be greater than the output 1dB compression level. All design parameters in the datasheet were given at the optimum bias point of ($I_d = 200mA, V_d = 28V$). Table 5 below shows the important thermal and RF design parameters given in the datasheet [35].

Design Parameter	Value
Maximum Junction Temperature	275°C
Junction to Case Thermal Resistance	4.0 °C/W
Gain in Frequency Range (at 85°C)	> 20 dB
Input 1dB Compression (at 3 GHz and at 25°C)	~ 26 dBm

Table 5: T2G6003028-FL Thermal and RF Parameters from Datasheet

At the time, this device had the highest rated junction temperature of any COTS GaN transistor and would be a perfect selection in terms of thermal requirements ($T_J, R_{\theta JC}$). Not only this but because the device package was ceramic it would be able to withstand the high ambient temperature without melting unlike a plastic package.

Thermal Design Considerations

Background Information

As mentioned previously, the optimum bias condition described in the datasheet for the active device was $I_d = 200mA, V_d = 28V$. All measurements were taken using this datasheet bias condition because all datasheet information was given at this bias condition and by using the device at this bias point it was possible to compare measured results against known results to confirm the validity of the test set-up at room temperature. After confirming the datasheet results and learning that the device could meet all specifications at room temperature, it was decided to operate the device at the same bias point at the desired temperature of 230°C to see the effect of temperature. For these reasons the following thermal design was performed based on the active device being biased at the datasheet bias.

Later, after learning that the device could still meet specifications under the datasheet bias conditions at 230°C (as describe in Change of Parameter Values at 230°C) it was decided that this would be the bias condition used for the PA.

However, as discussed in Chapter 2, the power dissipated by the active device is the main thermal constraint. If the power dissipation at this bias point was too high then the device junction temperature could go above the maximum rated junction temperature and cause the device to fail. For this reason, a thermal investigation was performed to determine if this bias point could be used and also reliably operate above 210°C. It was also deemed necessary for the thermal design to include error margin so that if the active device was to consume more power than rated, or if the thermal resistances were miscalculated, these error margins would be large enough to not cause the junction temperature to exceed the maximum rating of $T_{JMAX} = 275°C$ causing the device to fail.

Thermal Design Equation Parameters

At the bias point of $(200mA, 28V)$ the device power dissipation would be $P_D = 5.6W$. In order to allow error margin for these calculations and any not included self-heating effects, $1W$ extra power was added to the power dissipation bringing P_D to be $6.6W$. This error margin may be excessive but ensures absolutely reliable operation. As stated in the datasheet for the device the junction to case thermal resistance was $R_{\theta JC} = 4.0°C/W$. As explained in Chapter 2 the total thermal resistance is $R_{\theta TOTAL} = R_{\theta JC} + R_{\theta CH} + R_{\theta HA}$. By substituting these values into Eq. 32 and setting the junction temperature to $T_J = 275°C$ it's possible to see that the maximum total sum of $R_{\theta HA}$ and $R_{\theta CH}$ will be $2.82°C/W$ to operate at an ambient temperature of $T_A = 230°C$ with sufficient error margin.

$$6.6W = \frac{275°C - T_A}{4.0°C/W + R_{\theta CH} + R_{\theta HA}} \tag{32}$$

Thermal Paste Selection and $R_{\theta CH}$ Calculation

It was necessary to find a thermal paste that could operate at an ambient temperature of $T_A = 230°C$ with a low thermal resistance. Chemtronics CW7100 thermal paste was found to be able to operate at this desired operation temperature with a potentially low thermal resistance and high conductivity [36]. To calculate $R_{\theta CH}$, the value of thermal conductivity from the thermal paste datasheet is used along with the mechanical dimensions of the active device in Eq. 33. The reason the mechanical dimensions are required is because this is where the paste will be spread.

$$R_{TH} = \frac{d}{k\,A} \tag{33}$$

d: $Thickness$ $[m]$

k: $Thermal\ conductivity$ $\left[\frac{W}{m\,K}\right]$

A: $Cross\ sectional\ area$ $[m^2]$

The cross section area A of the active device was calculated to be $A = 44.85\ mm^2$. The rounded corners of the active device were not taken into account as they were seen as negligible in the total area.

$$A \approx (13.97mm)(4.064mm) - 2 \times \pi(1.27mm)^2 - 2 \times (0.953mm)(0.94mm) = 44.85mm^2$$

Using this calculated cross sectional area and assuming the thickness of the thermal paste to be $d = 0.1mm$, the equivalent thermal resistance $R_{\theta CH}$ was calculated:

$$R_{\theta CH} = \frac{d}{L\ A} = \frac{0.0001\ m}{(5.6\ W/m\ K)(0.000004485\ m^2)} = 0.398\ K/W = 0.398\ °C/W$$

In order to include error margin in the calculations this value was rounded to $R_{\theta CH} = 1.0°C/W$.

Heat Sink Selection and $R_{\theta HA}$ Calculation

After calculating $R_{\theta CH}$ and including error margin, in order to reliably operate at an ambient temperature of $T_A = 230°C$ the value of $R_{\theta HA}$ needed to be lower than $R_{\theta HA} = 1.82°C/W$. The Wakefield-Vette 423K heat sink was chosen to be used in the design based on its very low thermal resistance at the given active device power dissipation. The heat sink to ambient thermal resistance was calculated using information provided by the datasheet to be $R_{\theta HA} = 1.0°C/W$ at $P_D = 6.6\ W$ [37]. This value of thermal resistance was increase by 33% for the purpose of error margin to $R_{\theta HA} = 1.33°C/W$.

Estimated Junction Temperature Including All Error Margin

After finding components with low thermal resistances and calculating thermal resistances for the active device to be used under the desired bias point, it was possible to include these thermal parameters in the thermal design equation to estimate the junction temperature T_J at an ambient temperature of $T_A = 230°C$. This calculation is shown in Eq. 34. and solving the equation yields a junction temperature of $T_J = 271.798°C$.

$$6.6W = \frac{T_J - 230°C}{4.0°C/W + 1°C/W \ + 1.33°C/W} \tag{34}$$

At a junction temperature of $T_J = 271.798°C$ the device could be expected to reliably operate over 10,000 hours according to the device datasheet quoted median lifetime [35]. Again, this junction temperature was calculated with much error margin and it is likely to not be the actual junction temperature meaning the device could probably operate for even longer.

Thermal Investigation Conclusion

After running the thermal analysis including error margin for the active device at the datasheet bias point using thermal paste and a heat sink that could support reliable operation at an ambient temperature of $T_A = 230°C$ it was decided that the PA could be designed to reliably operate at $T_A = 230°C$.

Change of Parameter Values at 230°C

As stated previously, information in the datasheet provides important design parameters at only 25°C and 85°C. Because the datasheets for most RF transistors did not specify important design parameters at the desired ambient temperature, in searching for an active device it was decided that it may have been necessary to test / measure parameters of more than one active device at the desired ambient temperature of 230°C before making a final decision on which device would be used to design the PA. Qorvo's T2G6003028-FL was the top candidate as it met both high temperature and high frequency specifications at 85°C and therefore was the first active device to be tested / measured at 230°C.

Despite doing calculations on the device power level, thermal resistances, junction temperature, and ambient temperature it was still unknown whether or not the device would actually operate at such a high ambient temperature because measurement had yet to be taken. Even further, it was unknown how the important design parameters such as gain, linearity, and RF stability would change with increasing temperature. As discussed in Chapter 2, research suggested that as temperature increases in GaN devices the gain of the device decrease. This may suggest the device would become more stable at higher temperatures but this was speculation.

After devising a test setup / testing procedure (discussed in detail in Chapter 4) it was possible to measure s-parameters (and therefore also measure RF stability), 1dB compression, and IP3 for this candidate active device. All these design parameters were measured under the datasheet bias condition of $(200mA, 28V)$.

As shown in Figure 15, the gain for this device appeared to decrease by approximately 6 dB in the specified frequency range by increasing the temperature from 25°C to 230°C. This decrease in gain was deemed acceptable for the purpose of design and it was decided that this device could still be used to meet the gain specification for the PA.

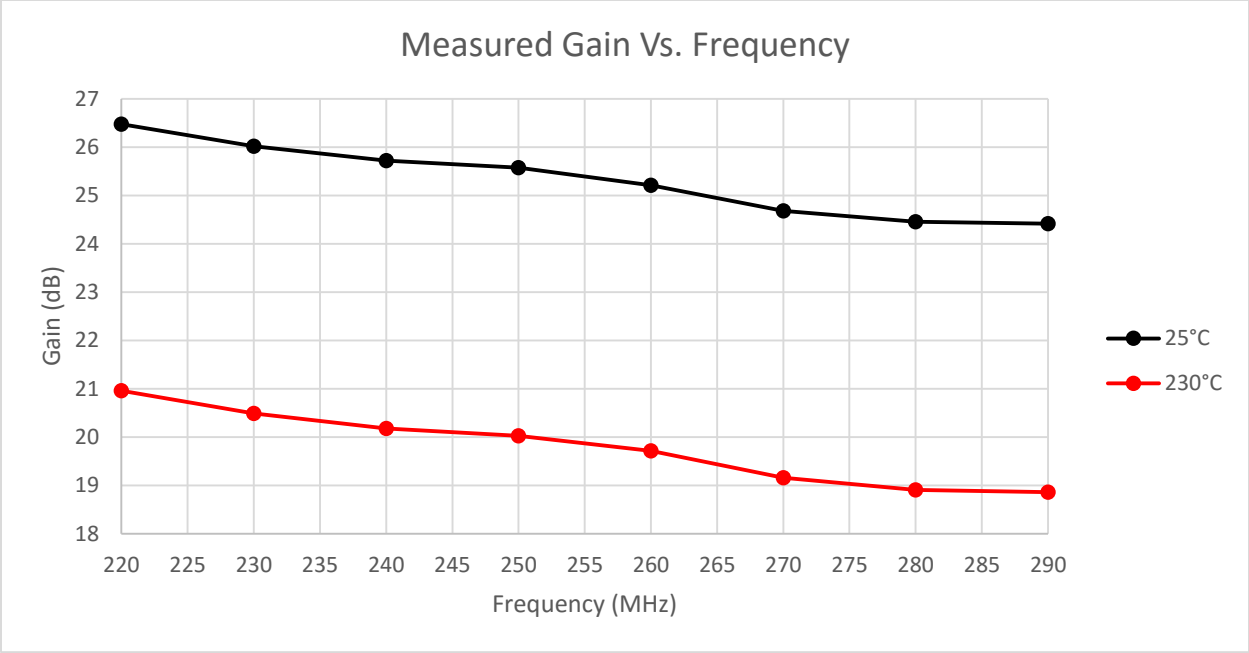

Figure 15: Measured Gain at 25°C and 230°C

In the specified frequency range the device was not unconditionally stable as shown in Figure 16. This was deemed acceptable because the gain was high enough that if a stabilization technique were to be employed, a drop in gain could be tolerated and the gain requirement could probably still be met.

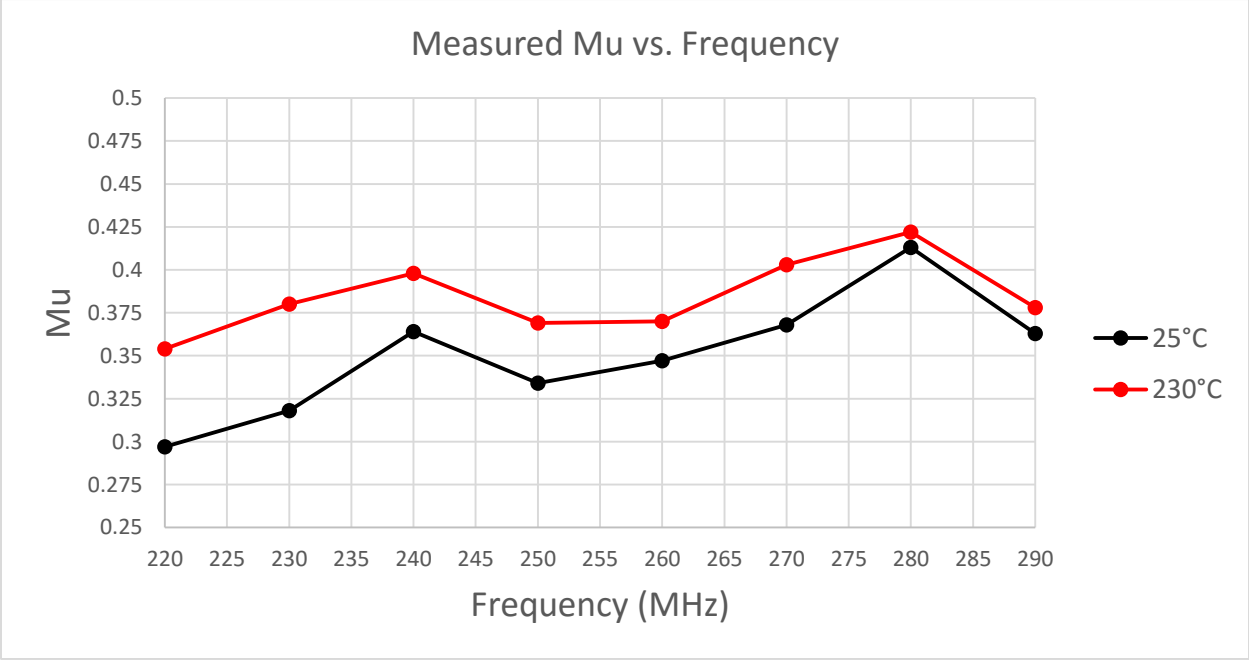

Figure 16: Measured Stability parameter Mu at 25°C and 230°C

Figure 17 shows the 1dB compression data taken for the device at approximately the operation center frequency. The 1dB compression point is slightly higher at 230°C than at 25°C likely due to the fact that the gain was lower at the desired operation temperature as shown in Figure 15. These results confirm that it was assumed correctly that the 1dB compression point would not change drastically between 25°C and 230°C.

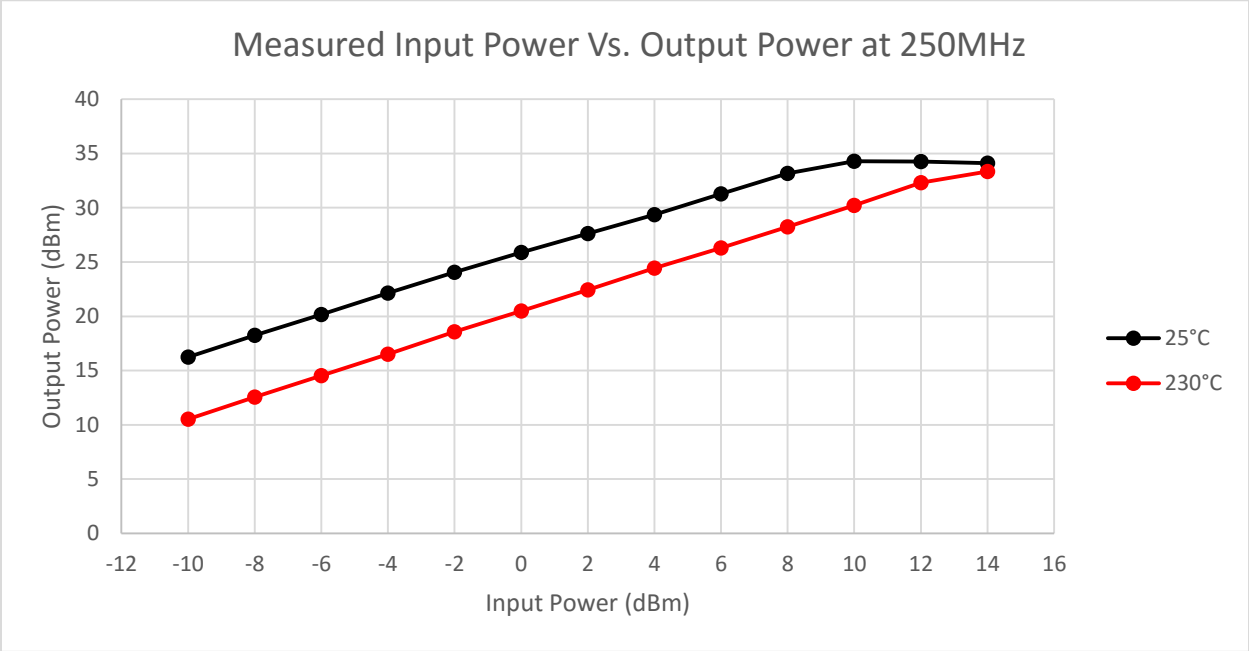

Figure 17: Measured 1dB Compression at 25°C and 230°C

Table 6 shows no change in IP3 from room temperature to the desired operation temperature. These results are consistent with the measured 1dB compression level and further confirmed that there was little to no change in linearity characteristics at elevated temperatures under the datasheet bias point.

Temperature	Output Third Order Intercept Point (IP3)
25°C	49.00 dBm
230°C	50.36 dBm

Table 6: Measured IP3 at 25°C and 230°C

Bias Point Selection

Clearly the important design parameters did not significantly degrade at high ambient temperature. After measuring these important RF design parameters at 230°C and learning that the device still could meet both thermal and RF requirements, no more active devices were tested and this was chosen to be the active device for this design. In addition, because the linearity parameters were relatively unchanged and the gain did not degrade significantly at 230°C at the datasheet bias point, the active device power consumption was at an acceptable level, and thermally reliable, it was decided that bias point would not be changed from the optimum bias point given in the device datasheet.

Because of linearity specifications it was decided to operate the PA in class A operation. Because of the low input drive (not exceeding a power level of $RF_{in} = 0\ dBm$) and high linearity at the bias condition and center frequency, it was assumed that the PA would be operating in its small signal region and therefore no load line analysis was necessary. However for the sake of completeness and in order to ensure the PA would be correctly biased in this class A operation, IV characteristics were taken on the active device at 230°C. The IV characteristics are shown in Figure 18. After deciding that the bias point would remain unchanged, the device s-parameters were exported so that they could be used in ADS to design the PA.

As temperature was increased the gate voltage would not provide the necessary drain current. In order to correct for this the gate bias was changed manually on the DC voltage supply to keep the bias current fixed at $Id = 200mA$.

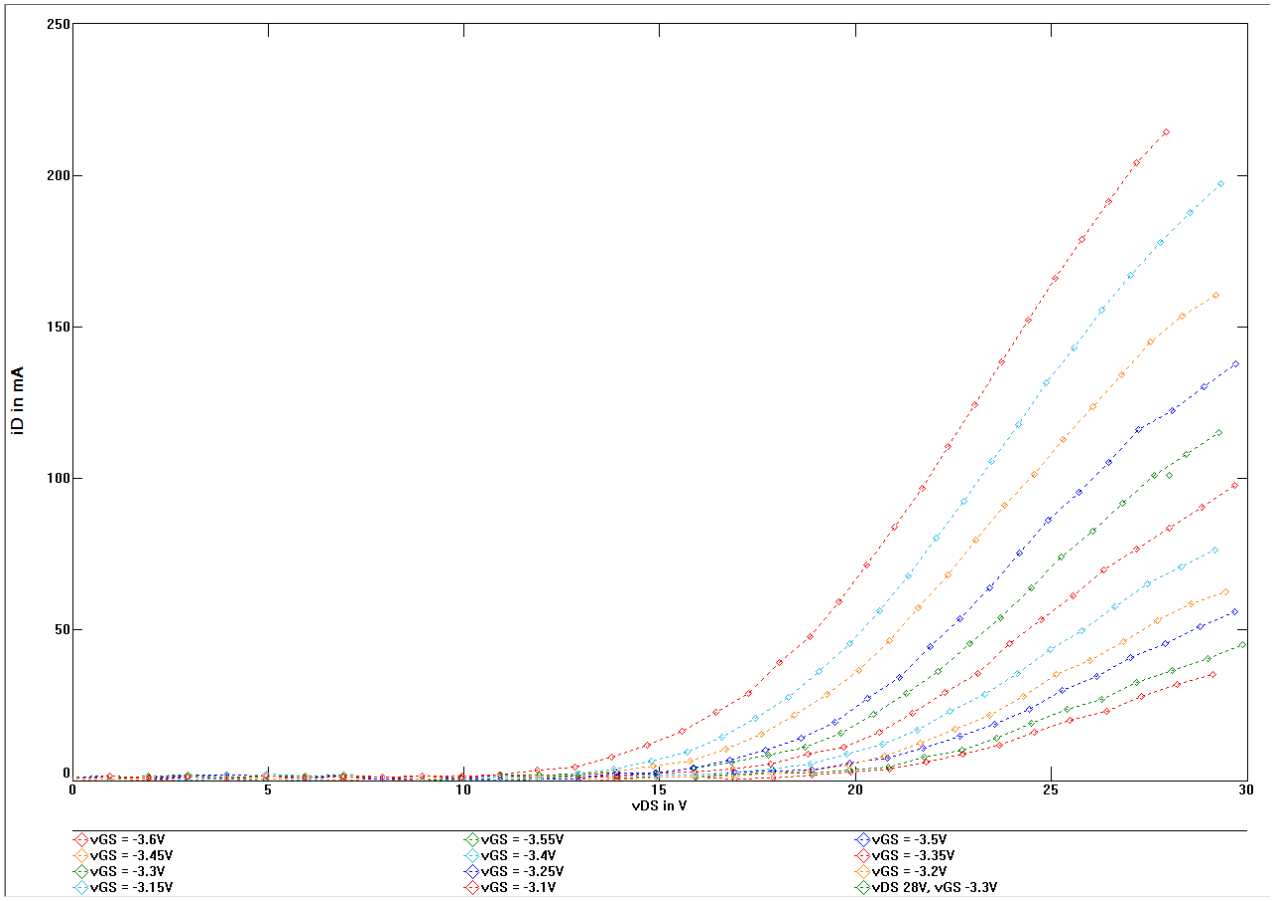

Figure 18: Measured IV Characteristics at 230°C

Selection of Passive Components

Background Information

Because high temperature high frequency electronics is not a matured field, one major challenge in this design was that there are few resistors, capacitors, and inductors that can withstand ambient temperatures above 200°C. Passive components that could operate above 200°C did not show promising performance according to datasheet information. These components would be temperature de-rated for power dissipation and / or component value. This posed a challenge in the design due to the sensitivity of component value at the specified operation frequency; in particular, any slight change in capacitance or inductance value in the matching networks could drastically degrade performance. It was necessary to choose components that could not only withstand operation at 230°C but also had high tolerances at these temperatures. In searching, both capacitors and resistors could be found that could operate at the specified frequency and ambient temperature after temperature derating with high component value tolerance but no inductors could be found.

For these reasons it was decided that microstrip matching networks would be used instead of discrete element matching networks and that passive components would only be used for components whose values could change and not affect the design drastically such as for RF chokes and DC blocking capacitors. This would ensure reliable operation and mitigate performance concerns with the design.

RF Choke Selection

The Coilcraft AT549RBT Extreme Temperature Coil was chosen because it was the only inductor that was rated to operate above 220°C at the desired component value, self-resonant frequency, and maximum current rating [38]. The greatest downside of this inductors was that the component value could vary significantly due to manufacturing and vary further with temperature by up to +300 ppm/°C to +500 ppm/°C. However, it was the highest value inductor available on the market that could operate at 230°C and deemed the best choice to use as the RF choke. The self-resonant frequency of these inductors is acceptable for the specified frequency range rated at approximately 450MHz.

Unlike other high temperature inductors available on the market, these inductors do no show temperature de-rating curves in the datasheet because they keep their value across the full temperature range without degrading in power rating. After measuring s-parameters on the inductors at 230°C at the specified frequency it was clear that these inductors were properly rated and could be used for this high temperature application.. The selection of component value will be discussed in the Bias Network Design section.

DC Blocking and Bypass Capacitor Selection

There are many capacitors available on the market that are rated to operate at 230°C and above, however, there are few that are able to keep the same component value at the elevated temperature. The IPDiA XTSC series capacitors had a wide range of values available and were chosen to be used for both the DC blocking capacitors and bypass capacitors after careful consideration [39]. Rated up to 250°C, at the time of selection these were the highest temperature rated surface mount capacitors available on the market. The datasheet state that the capacitors are rated to keep their component value over the full temperature range. Not only this, these capacitors are rated at a high self-resonant frequencies so they can be used in the specified frequency range. Just as with the inductor selection process, after measuring s-parameters at 230°C at the specified frequency it was clear that these inductors were properly rated and could be used for this high temperature application. The selection of component value will be discussed in the Bias Network Design section.

Resistor Selection

Not many resistors on the market are rated to operate above 200°C and further not many surface mount resistors are available. Small size surface mount resistors must be used in RF design to ensure few parasitics.

Because the purpose of the resistors was RF stabilization, unlike the capacitors and inductors, the resistor chosen needed to have much higher precision component values. If the component value varied too much from the design value it would affect important design specifications such as gain, RF stability, and IRL. For this reason it was

particularly important to choose resistors which varied very little at the desired ambient temperature.

Vishay-Dale Thin Film PATT series resistors were chosen to be used for this design not only because they were rated to operate up to 250°C but also were surface mount and could be used for RF applications [40]. The PATT series resistors had a very wide range of values so once a stabilization routine was employed in the design it would be likely that a component value would be available. These resistors were rated to not change component value but only in power rating as temperature was increased. At room temperature the resistors had a power rating of 200mW and at 230°C the power rating of the resistors dropped to 20% of the full rating meaning the resistors could only handle 40mW. As discussed in the Stabilization Network Design section, these resistors would be used at the gate of the active device and therefore would consume little power. Because of this the temperature de-rated power would not be an issue in the design.

Just as in the case with the capacitors and inductors, after measuring s-parameters at 230°C at the specified frequency it was clear that these resistors could be used for this high temperature application. The selection of component value will be discussed in the Stabilization Network Design section.

Interface Materials

As temperature is increased not only do circuit components need to withstand the extreme ambient temperatures but also all materials used in the design including PCB, solder, end-mount connectors, and screws.

PCB material

Because not all PCB is rated to operate at high frequencies due to high loss and high dissipation factors, it was necessary to find a board able to support high frequency operation. From a thermal view, the board must have a low coefficient of thermal expansion and low thermal coefficient of ϵ_r so that the matching networks would not change from their design at the desired operation temperature. Based on a survey of PCB materials available, Rogers 4003C was investigated because of its high frequency capabilities [41].

The coefficient of thermal expansion in the X, Y, and Z directions of the board was given in the datasheet respectively to be 11 $ppm/°C$, 14 $ppm/°C$, and $46ppm/°C$ and the coefficient of thermal expansion for ϵ_r was given to be 40 $ppm/°C$ (These were assumed to be given as °C per degree above room temperature).

Calculating the impedance [42] of the microstrip line for the maximum changes in these board properties showed that impedance of the line would change by less than 1% in the worst case scenario. Because of this negligible change in impedance and its high frequency capabilities it was chosen to be the board used in this design.

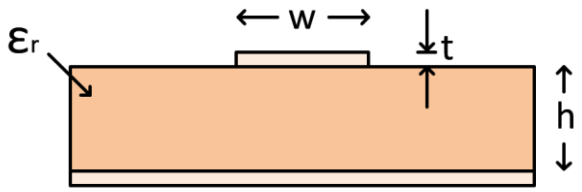

Figure 19: Microstrip Line

$For\ W/H \geq 1$:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2\sqrt{1 + 12\frac{H}{W}}} \tag{35}$$

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{eff}}\left[\frac{W}{H} + 1.393 + \frac{2}{3}\ln\left(\frac{W}{H} + 1.444\right)\right]} \tag{36}$$

High Melting Point Solder

The melting point of most common COTS solder is below 200°C and therefore a high temperature capable solder needed to be used in the design. To ensure no joints would melt at the desired ambient temperature, a solder with a sufficiently higher melting point than the ambient temperature would be best. A melting point of between 280°C to 300°C was desired because this was much higher than the ambient temperature but also this would be within the limitations of the tools available to solder with. Because most components chosen were surface mount, a paste based solder was preferred in order to properly solder the components. Ultimately, Indalloy 151 from Indium Corporation was chosen because of its melting temperature of 296°C and because it was available from the manufacturer in paste form [43].

End-mount connectors and screws

End-mount connectors were needed for the RF input / output and DC input / output lines. Unfortunately, there are no end-mount connectors on the market rated to operate above 200°C. Because of this, it was decided to research the melting temperature of all the materials used to make the connectors and ensure that they would not melt at the high ambient temperature. From the datasheet it was found that these connectors were made from a brass / copper allow for the body and fluorocarbon for the insulator. After finding the melting temperatures of the materials used to make the connectors was much higher than 200°C it was decided that it would be ok to use these connectors at the desired

operation temperature. Once repeated measurements were taken at the desired operation temperature using the connectors it was seen that temperature did not degrade the performance of the connectors.

The heat sink was used both for thermal properties but also as an RF ground for the circuit. Because of this, the screws were not only used to mount the PCB to the heat sink but also as a ground connection to create microstrip short circuit stubs. Because of this the s-parameters of the screws needed to be taken in order to more accurately model the short circuit stub. No temperature information was provided for the screws, but the material properties were given to be that the screws were made from steel and zinc-plated. As the case with the connectors, after finding the melting temperatures of the materials was much higher than 200°C it was decided that it would be ok to use these screws at the desired operation temperature.

Bias Network Design

Component Value Selection

The Coilcraft AT549RBT Extreme Temperature Coil selected to be used for the RF chokes (L1 and L2 in Figure 26) had the only value of $L = 1\mu H$ available and was chosen after determining that in the specified frequency range that value should provide a sufficiently high impedance on the DC line.

The IPDiA capacitors chosen for the DC blocking capacitors (C_1 through C_4 in Figure 26) were chosen to be $C = 1\mu F$ because this was the largest value available by the manufacturer at the time and would allow for an RF signal to pass through to the active device relatively unattenuated. Rated for 11V maximum operation voltage, three capacitors were needed at the output of the active device due to the drain bias of 28V. This lower capacitance of $C_{eq} = 0.33\ \mu F$ still provides a low impedance and allows for the RF signal to pass relatively unattenuated.

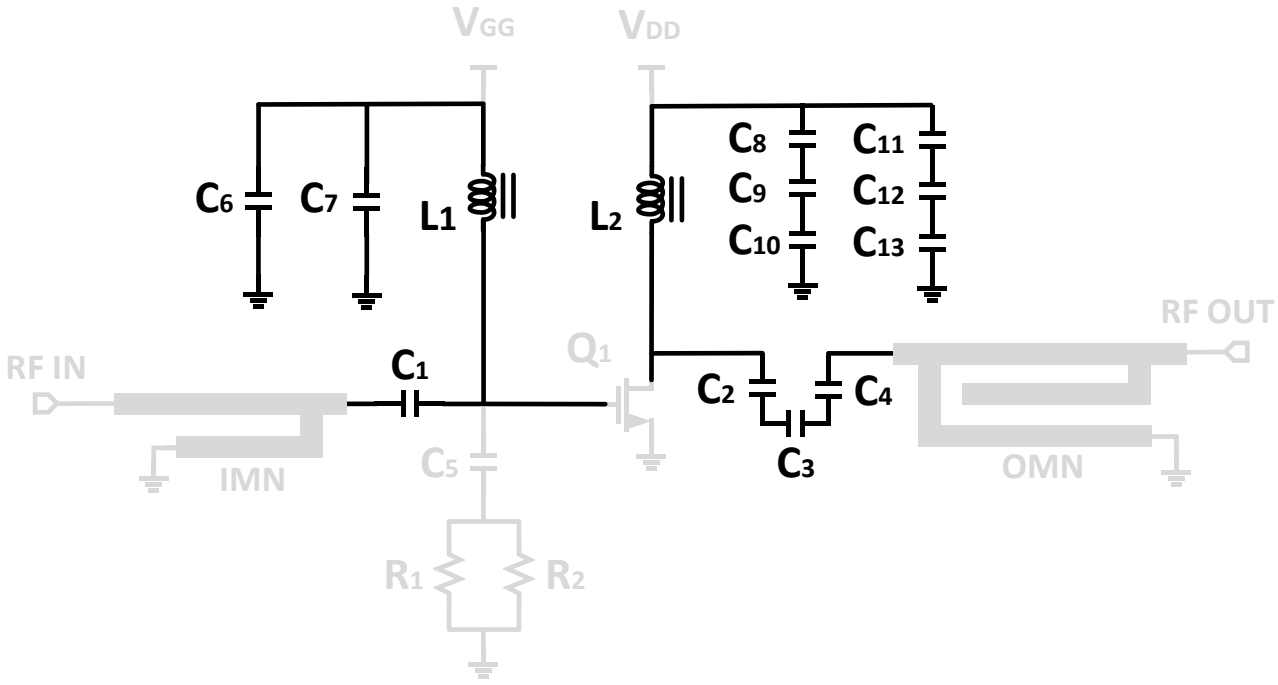

Figure 20: Bias Network in Black, Other Elements Shaded

Bypass capacitors (C_6 through C_{13} in Figure 26) were used on the DC input / output lines in order to further ensure no RF signal passes to the DC supply and also to ensure noise on the DC lines was common mode. For the DC input line, one capacitor value is chosen to be large ($C_6 = 0.1\ \mu F$) and the other value chosen to be small ($C_7 = 100\ pF$). The bypass capacitor should be chosen to be as large as possible in order to present a low impedance to the RF signal to short the signal to ground and also make noise common mode. However, high value capacitors tend to have low self-resonant frequencies which is a case with these IPDiA capacitors. Therefore a small value capacitor of $C = 100pF$ with a high self-resonant frequency of $SRF \approx 2.25GHz$ was placed in parallel with the large capacitor to increase the overall equivalent capacitance self-resonant frequency ensuring a short circuit at the specified frequency. It should be noted the IPDiA capacitor available with the value $C = 0.1\mu F$ had a self-resonant frequency of $SRF \approx 31.83\ MHz$ and was therefore chosen over $C = 1.0\mu F$ which had a significantly lower self-resonant frequency of $SRF \approx 4.75\ MHz$.

Again, as was the case with the DC blocking capacitors at the output of the active device, three capacitors were used of each low value and high value capacitor due to the voltage rating on the capacitors only being rated at a 11V maximum operation voltage. The output bypass capacitor values are as follows: $C_8 = 0.1\ \mu F$, $C_9 = 0.1\ \mu F$, $C_{10} = 0.1\ \mu F$, $C_{11} = 100\ pF$, $C_{12} = 100\ pF$, and $C_{13} = 100\ pF$.

Once these values were chosen for the bias network components, s-parameters were measured on all components and imported into ADS to be used in design.

Stabilization Network Design

In order to ensure no oscillations it was necessary to design the PA to be unconditionally stable in the specified frequency range.

Active Device Stability

Measuring s-parameters on the active device at 230°C showed the device was not unconditionally stable in the specified frequency range. Figure 21 shows Mu for the active device calculated from measured s-parameters at 230°C. Because of this it would be necessary to design a stabilization network for the PA.

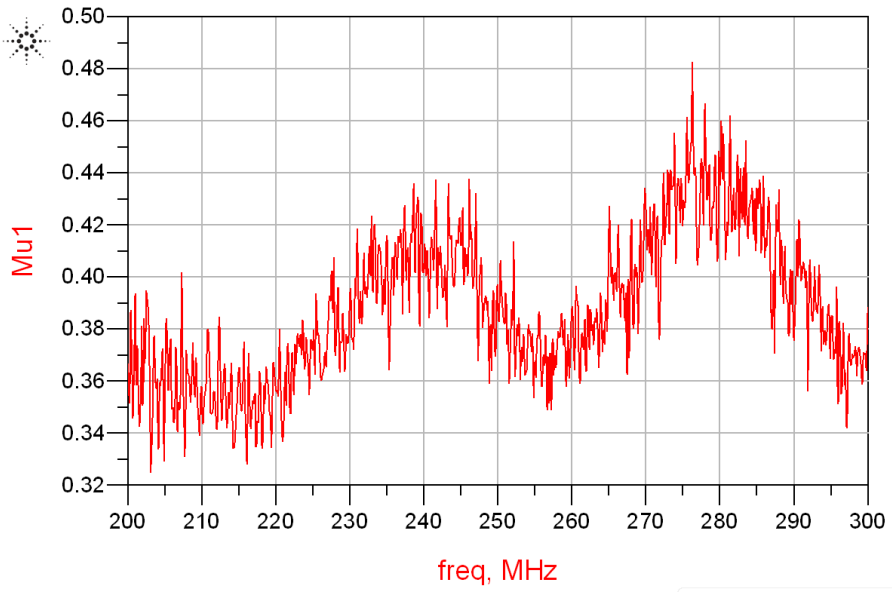

Figure 21: Calculated Mu for Active Device at 230°C

Stabilization Technique

The bias network was designed and simulated in ADS using measured s-parameters at 230°C for the active device, inductors and capacitors. After simulating the bias network with the active device, it was possible to implement a stabilization technique to ensure the device was unconditionally stable in the specified frequency range. Due to the high voltage and power levels at the output of the active device a shunt resistor at the gate was

determined to be the best topology for stabilization over the use of a shunt resistor at the drain.

Stabilization Resistor

Before the bias network was designed and simulated, neither a resistor capable of high temperature high frequency operation had not been found nor the value of the resistor determined. After determining the value of the resistor through simulation, a COTS resistor capable of high temperature high frequency operation was found and s-parameters were measured at 230°C. These s-parameters were then used in simulation to determine if the value of the ideal resistor chosen was correct or if the resistor value needed to be adjusted.

Stabilization Resistor Value Selection

In general for a shunted gate resistor stabilization topology, as the device becomes more stable the gain decreases. Therefore, the value of the resistor was chosen such that it did not decrease the gain by too much and allowed for the device to be unconditionally stable with reasonable error margin. The measured device stability and gain at 230°C is shown in Figure 22.

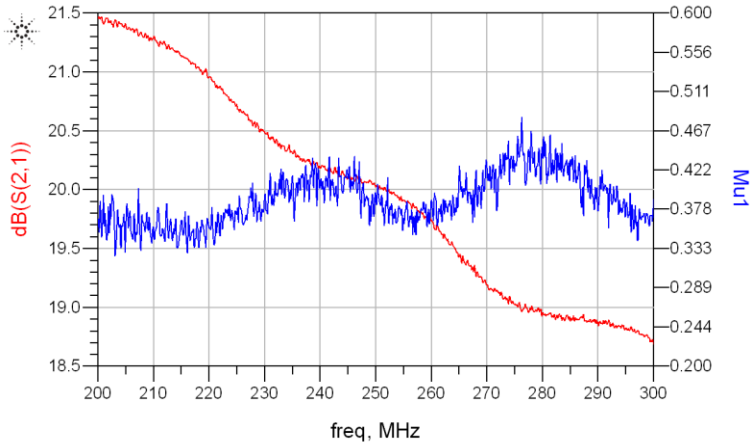

Figure 22: Measured Gain and Mu of Active Device at 230°C

Figure 23 shows the network gain and stability including an ideal shunted gate resistor of $R = 100\Omega$. Clearly, this value of resistance not only stabilizes the device with some error margin but also does not decrease the overall network gain by too much.

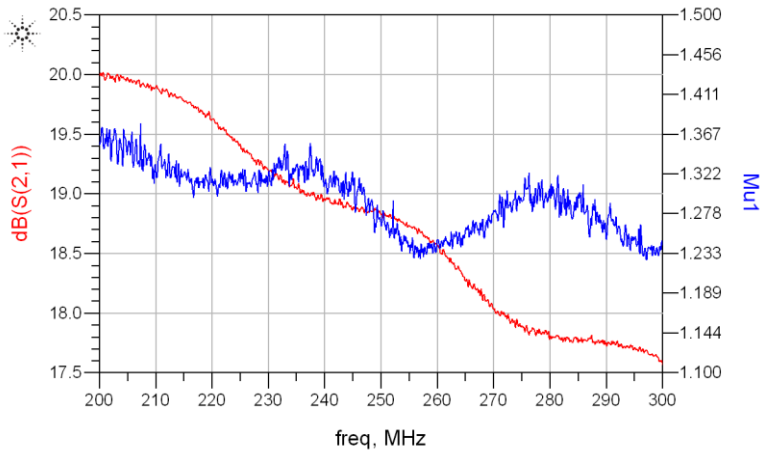

Figure 23: Simulated Gain and Mu including Ideal Shunted Gate Resistor

After finding a resistor able to operate at 230°C it was possible to measure the s-parameters at 230°C and import these results into ADS. As shown in Figure 24, the ideal resistor and measured resistor were showed close to the same results.

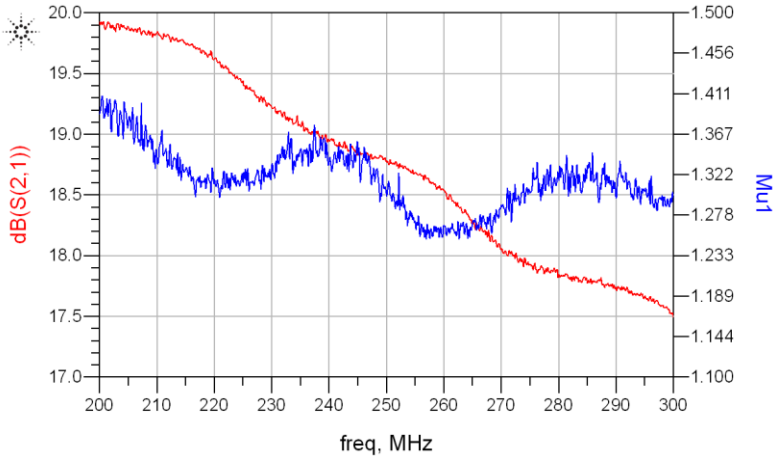

Figure 24: Simulated Gain and Mu including Resistor S-Parameters

Measured Stability Parameters at 230°C

After designing both the bias network and stabilization network and simulating to see promising results it was possible to print and populate a PCB. This design would include the bias network, stabilization network, and active device. As mentioned previously C_5

was used to ensure no DC power dissipation across the stabilization resistors. After confirming the shunted gate resistor R_1 stabilized the active device it would be possible to design the PA. The board was de-embedded up to the DC blocking capacitors in order to get accurate s-parameters for the network and to be used later in the design. Figure 19 shows the bias and stabilization network designed.

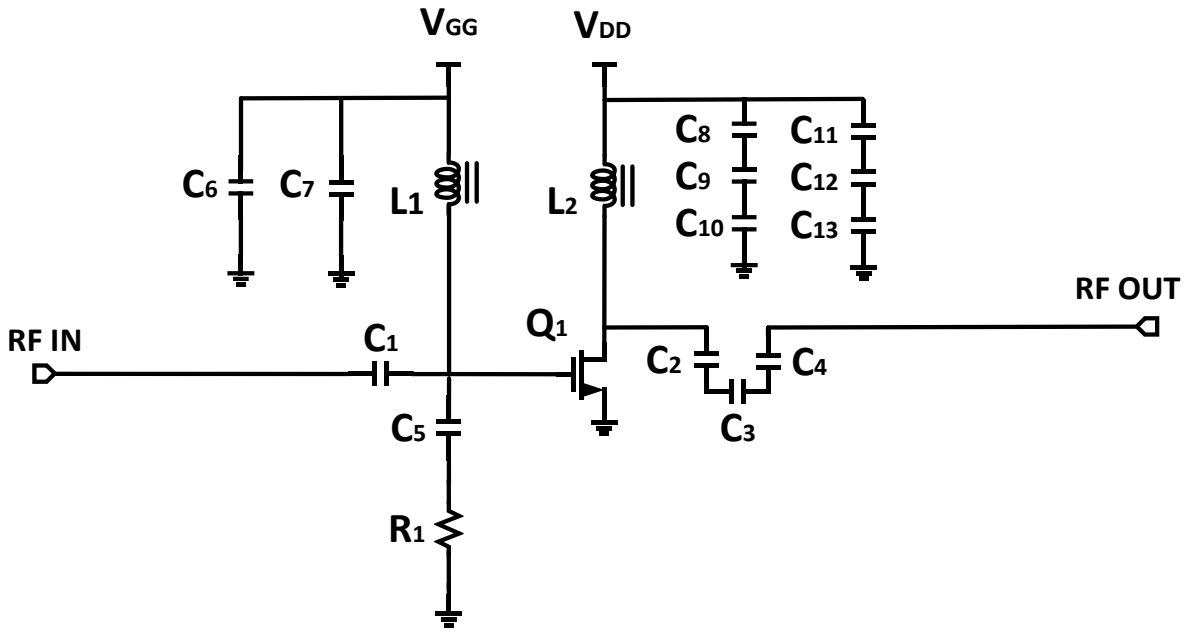

Figure 25: Bias and Stabilization Network

After measuring the network at the desired temperature it was found that the measured results did not match the simulation results as shown in Figure 26. The gain was higher than simulation and the network was not unconditionally stable over the specified frequency range as designed. In simulation it was found that as the gate resistor value was decreased, gain would decrease and stability would increase. Knowing that the resistor chosen would operate at 230°C, it was decided after measuring these results that rather than using the stability resistor value $R_1 = 100\Omega$, another resistor of the same value was placed in parallel with the first stability resistor to bring the total resistance down to $R_{EQ} = 50\Omega$ in hopes of increasing the stability and while not sacrificing too much gain.

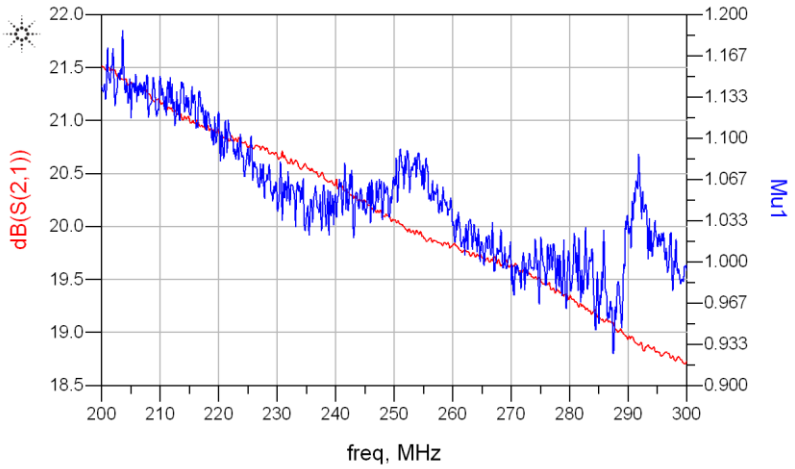

Figure 26: Measured Gain and Mu at 230°C for Entire Network

Figure *27* shows the redesigned stabilization network with two parallel resistors instead of the original designed one resistor network.

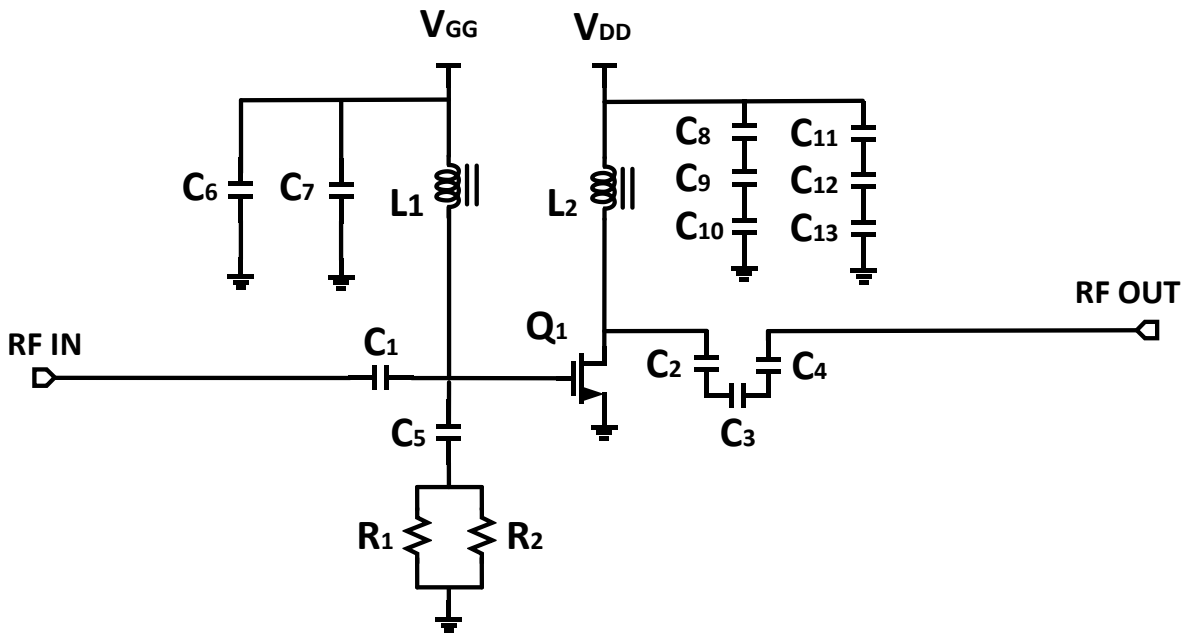

Figure 27: Bias and Redesigned Stabilization Network

After measuring the network with $R_1 = 100\Omega$ and $R_2 = 100\Omega$ it was found to confirm the simulation results which showed decreasing the gate resistor value decreased the gain

and improved stability. Figure 28 shows the measured gain and Mu for the network for the decreased stabilization resistance. Because the device was measured to be unconditionally stable and provide sufficient gain at 230°C it was decided that this stabilization network / bias network would be used for the final prototype.

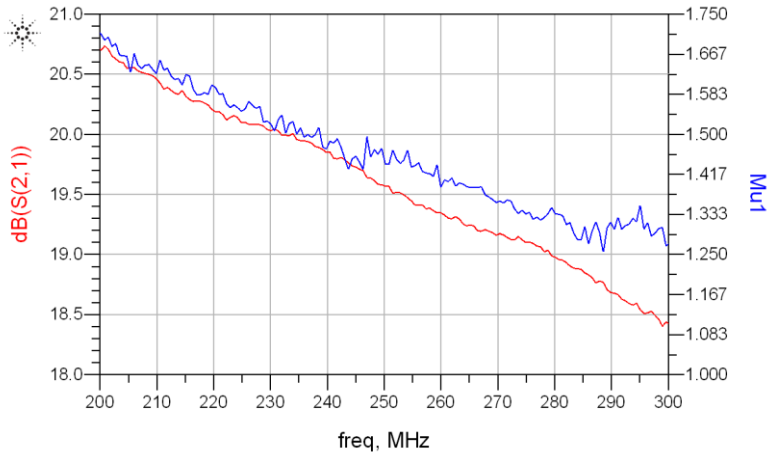

Figure 28: Measured Gain and Mu for Bias / Stabilization for R_{eq} = 50Ω

Once these s-parameters were measured for the network it was possible to design the PA matching networks.

Matching Networks

Background Information

Efficiency or PAE was not a concern in this design because the PA was designed for a wired system and all self-heating effects had been taken into account when choosing the bias level and heat sink. The measured 1dB compression level for the chosen bias at 230°C was high enough such that no load pull was necessary to get a higher saturated output power. Therefore, the matching networks were designed for simultaneous conjugate matching to ensure high gain and most effective power transfer from the input to output.

Board space was one main constraint when designing the matching networks. The area which the board would mounted on the heat sink had the dimensions of 33.9 mm X 139.7mm. The relatively low operation frequency would mean that the matching stubs could be as long as several hundred millimeters making designing entirely in that defined space challenging. It was possible to design the matching networks and board to protrude off the sides of the heat sink but undesirable because the PA was designed as part of a system and making the board unnecessarily long would waste space.

The other main design constraint, as discussed previously, the matching networks could not be designed with passive components like capacitors or inductors because few inductors are rated for low tolerances at the desired operation temperature. Because of this constraint the matching networks needed to be designed entirely in microstrip lines in order to ensure reliable operation at the desired operation temperature. Due to the low operation frequency tapered stubs would be unreasonably long / wide and could not be used for the matching network design as is convention in PA design. Therefore, the matching networks were designed as open and short circuit stubs to present a simultaneous conjugate match to the input / output of the entire network consisting of the active device, bias circuitry, and stabilization network. Because the heat sink was ground for the PA, it was necessary to use the mounting screws to create a short circuit stub.

Matching Network Design

The input and output impedances that needed to be provided for simultaneous conjugate matching were calculated using the measured s-parameters of the network consisting of the active device, bias circuitry, and stabilization network using the equations for simultaneous conjugate matching discussed in Chapter 2. The input impedance to be presented to the network was calculated to be $Z_S = 7.13 - j18.35$ and the output impedance to presented to the network was calculated to be $Z_L = 20.83 + j16.24$.

It was possible to design the matching networks to present the desired impedances using the Smith chart utility in ADS. Because the specifications called for wideband operation it was necessary to design the matching network Q values to be low. The networks were designed at the center frequency of 250MHz and it was possible to design each matching network Q to be low by using the Q circles on the Smith chart. The input network has a Q of approximately $Q \approx 3$ and the output network has a Q of approximately $Q \approx 1$.

After designing for low Q it was necessary to design both networks to provide low return loss. However, the return loss of the input network was of particular importance in this design. After designing the networks for low Q each network was optimized in ADS to provide the lowest possible return loss.

The designed input matching network is shown in Figure 29 and the designed output matching network is shown in Figure 30 . The network topology and response from 100 MHz to 400 MHz is also shown.

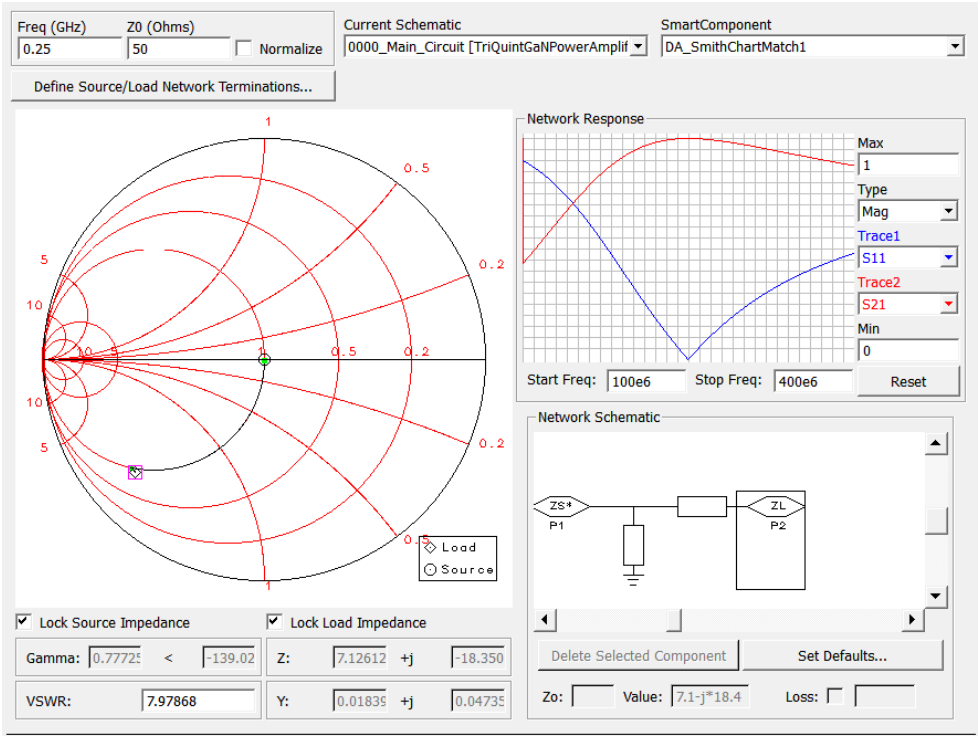

Figure 29: Input Matching Network Design

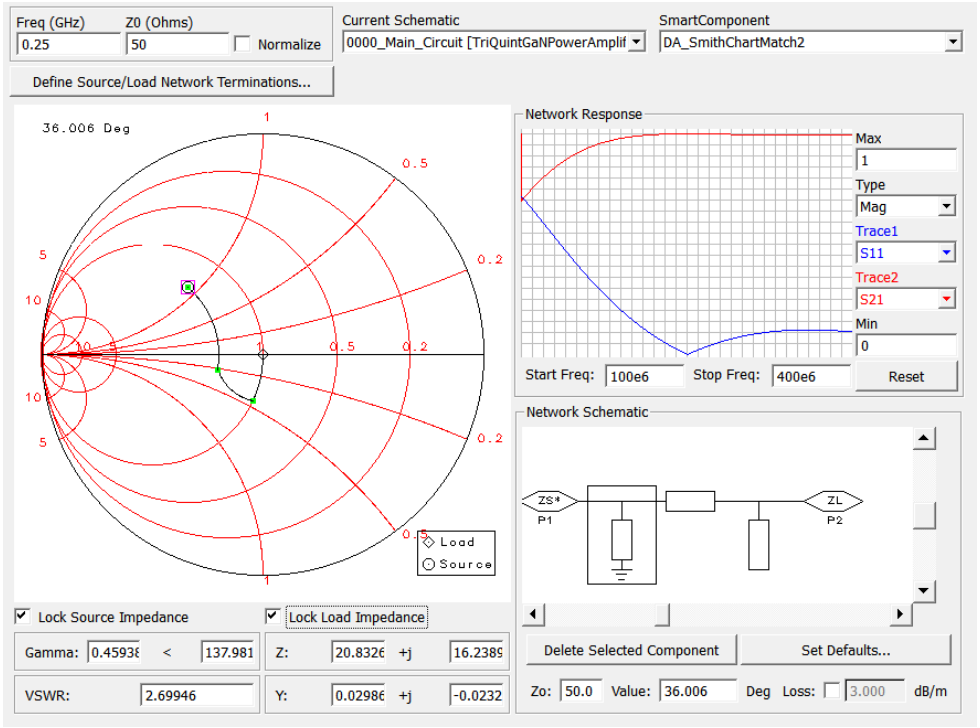

Figure 30: Output Matching Network Design

Matching Network EM Simulation

Because board space was a concern in the design of the matching, the layout / shape of each matching network was chosen in order to fit within the fins of the heat sink and not need to extend the board paste the edges of the heat sink. The input matching network layout is shown in Figure 31 and the output matching network layout is shown in Figure 32. These layouts differ from the designed input and output matching networks shown in the previous section because they have been optimized for both board space and also in order to account for the screws used to accomplish the shunt stub networks.

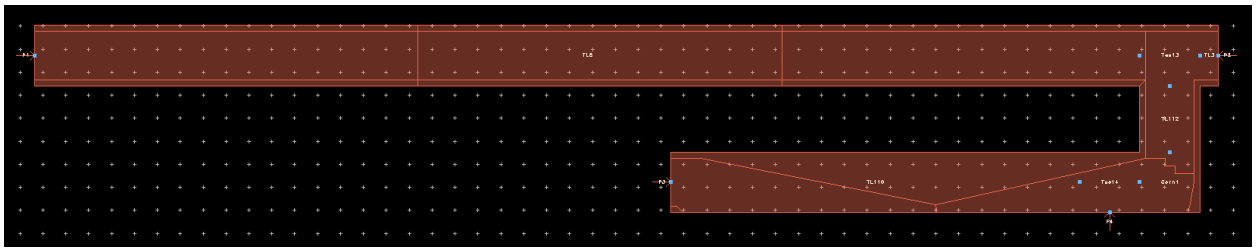

Figure 31: Input Matching Network Layout

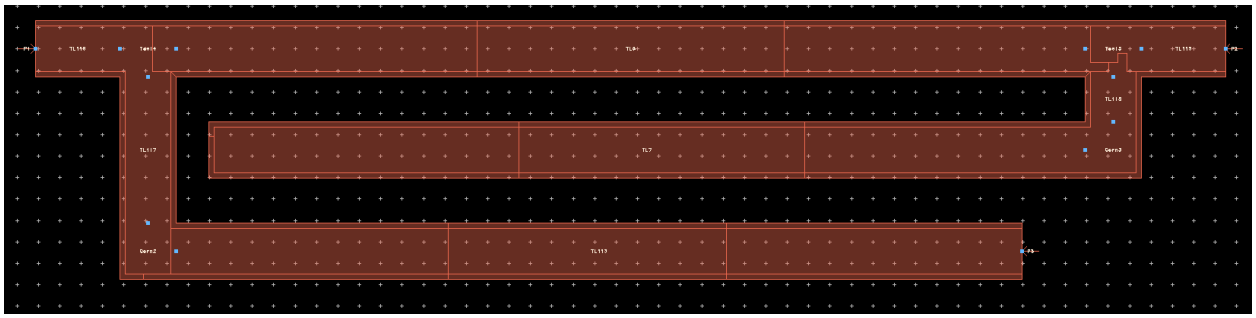

Figure 32: Output Matching Network Layout

Due to proximity of matching stubs and the operation frequency, an EM simulation for each match was run to see if there was any change in performance of the networks. The ideal schematic output matching network and EM simulation appeared to show similar results. However, this was not the case with the input matching network as it did not appear to yield the same results as the EM simulation. Because of the effects of high temperature operation on board parasitics was unknown, it was unknown whether or not an EM simulation would provide accurate results. Therefore, it was decided to design and optimize based on the ideal schematic stubs rather than use EM simulation results.

Prototyping

After meeting specifications in simulation it was possible to design the PCB and perform layout for the design. The final layout for the design is shown Figure 39, the bill of materials is shown in Table 7, and the final tested prototype is shown in Figure 34. The shunt stubs are accomplished using screws S_{14} and S_9.

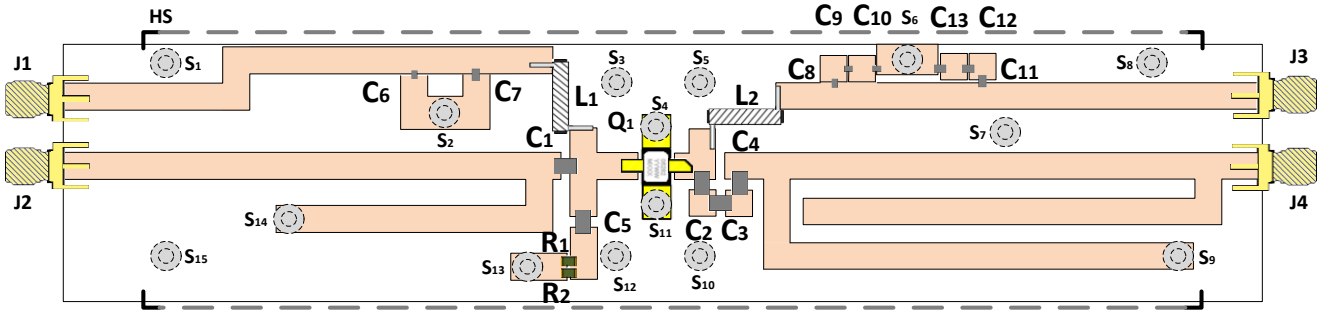

Figure 33: Final Prototype PCB Layouts

Reference	Value	Manufacturer	Function	Package	Part Number
C_1, C_2, C_3, C_4, C_5	1 µF	IPDiA	DC Block	1206	935.133.427.710
C_6, C_8, C_9, C_{10}	100 pF	IPDiA	Bypass	0402	935.133.424.310
C_7, C_{11}, C_{12}, C_{13}	0.1 µF	IPDiA	Bypass	0805	935.133.426.610
R_1, R_2	100 Ω	Vishay	Stability	0805	PATT0805E1000BGT1
L_1, L_2	1 µH	Coilcraft	RF Choke	-	AT549RBT102MLZ
Q_1	-	Qorvo	Amplifier	3028-FL	T2G6000328-FL
HS	-	Wakefield-Vette	Heatsink	-	423K
S_1 – S_8	-	Pololu	Screw / Nut	-	1957/1067
J_1 – J_8	SMA	Cinch	Connector	-	142-0701-801

Table 7: Final Bill of Materials

Figure 34: Final Tested Design Mounted on Heat Sink

Fine Tuning

After printing the PCB there was some discrepancy between the measured results and simulation results. The measured performance at 230°C on the network showed the IRL was lower than simulated and the gain was not as flat. Because of these discrepancies between simulation and measured results RF tuning was necessary to try to better match performance. In order to begin tuning the board for better performance, it was necessary to attempt to use simulation to match measured results. After recreating the measured results in simulation it would be possible to improve performance of the PA.

By inspecting the board once it was mounted on the heat sink it appeared as though there could be coupling between the input network short circuit matching stub and ground. Therefore, in simulation a capacitor of $C = 8pF$ was placed shunted to ground on the input network short circuit stub in an attempt to make the simulation match measured results. This capacitor appeared to allow simulation to match measured results

Once the measured results were created in simulation it was found that reducing the length of that same input stub would improve performance and allow the PA to more closely match the design. After cutting the input matching short circuit stub with an X-Acto knife and measuring the amplifier's performance at the desired temperature, it was found that this reduction in stub length greatly improved performance and matched the initial designed simulation results much more closely.

Chapter 4

Introduction

This chapter provides an overview of the measurement equipment used, measurement procedures employed, and shows the final measured results for the design at 230°C. Instruments used for measuring the important design parameters under high frequency operation and high temperature operation are discussed first. The instruments used were a convection oven, vector network analyzer (VNA), spectrum analyzer, signal generator, and an I/V curve tracer. After discussing the instruments needed and the instruments used, the measurement procedure for important RF parameters such as I/V characteristics, s-parameters, 1dB compression, power added efficiency (PAE), and third order intercept point (IP3) are discussed. Once the measurement equipment used and measurement procedure employed are explained to the reader, the final measured results for the design at 230°C are shown and discussed.

High Temperature RF Measurement Lab Set-up

Convection Oven

To take measurements at the desired ambient temperature an oven able to operate either at 230°C or higher was needed. Because cables would need to run from the inside to the outside of the oven where the RF measurement equipment was, an oven which could be accessed from the outside while it was operational was needed. Based on these requirements the Yamato DX-302 High Temperature Gravity Convection Oven was chosen. The DX-302 is able to operate well over the desired ambient temperature as it can operate up to 300°C [44]. Two air vents at the top of the oven serve the dual purpose of regulating the temperature of the oven and allowing cables be run from the inside to the outside of the oven during operation.

Vector Network Analyzer

A vector network analyzer (VNA) was needed in order to measure the s-parameters of not only the active and passive devices used in the design but also the completed amplifier. Because the PA was for a two-port device only two ports would be needed on the VNA.

The main requirement in choosing the VNA was the operation frequency. The instrument needed to be able to measure s-parameters over the specified operation bandwidth for each individual component used in the design and then the final PA. Ideally, the instrument should also be able to measure from DC to several gigahertz in order to see what the response of the PA was outside the bandwidth.

The PA was designed to operate at low power levels but was capable of having an output power of more than 1 watt. Because of this it was desired for the chosen instrument to have internal attenuation in order to ensure the instrument did not get damaged in the case that the PA oscillated and output more power than expected. If an internally attenuated instrument could not be found external attenuators would be used.

The Rohde & Schwarz ZVL13 Vector Network Analyzer was chosen because it met these requirements [45].

Spectrum Analyzer

A spectrum analyzer was needed to measure 1dB compression, saturated output power, IP3, and PAE.

The main requirement in choosing the spectrum analyzer was the operation frequency. The instrument needed to be able to measure the desired parameters over the specified operation bandwidth for each individual component used in the design and then the final PA. Ideally, the instrument should also be able to measure from DC to several gigahertz in order to see what the response of the PA was outside the bandwidth.

For the same reason as with the VNA, it was desired for the chosen instrument to have internal attenuation in order to ensure the instrument did not get damaged. If an internally attenuated instrument could not be found external attenuators would be used.

The Anritsu MS2665C spectrum analyzer was used because it could be used over the desired frequency range [46]. However, it did not have internal attenuation and an external attenuator was used.

Signal Generator

A signal generator was needed to sweep input power to take measurements for 1dB compression, saturated output power, IP3, and PAE.

The main requirements in choosing the signal generator were output power level and operation frequency. The generator needed to be able to operate within the specified frequency range and also needed to have an output power up to 20 dBm. In addition, it was desired that the signal generator be able to output two tones so that it could be used for IP3 measurements.

The Keysight E8257D PSG Analog Signal Generator was used because it could be used over the desired frequency range and also output the desired power level [47]. Unfortunately, this signal generator was not able to output two tones simultaneously and therefore another signal generator was needed. Another signal generator was not available in the laboratory but a spectrum analyzer available was able to output an RF signal in the specified frequency range at the desired power level and therefore could be

used as a second signal generator. The second spectrum analyzer used was the E4408B ESA-L Basic Spectrum Analyzer from Keysight [48].

I/V Curve Tracer

An I/V curve tracer was needed measure the I/V characteristics of the active device.

The main requirements in choosing the I/V curve tracer was the voltage and current limits of the instrument. It must be able to sweep the gate voltage from a negative value to zero and it must be able to sweep the drain voltage up to the bias point of $V_D = 28V$. Not only this but the instrument must be able to source the bias current of $I_D = 200mA$.

The Accent Optical Technologies DiVA D265 I(V) Analyzer met these requirements and was chosen to take the I/V curves for the active device [49].

Measurement Preliminaries

RF Coaxial Cables / Oven

The system specification called to use M17/152-00001 coaxial cable as the RF coaxial cable for the down-hole system due to its ability to operate at high frequencies and high temperatures. One drawback of using this cable is that it was only specified to operate up to 200°C. However, after calibrating at room temperature, operating at 230°C, and re-measuring the calibrated cables at room temperature, it was found that the cables did not degrade after being used. Because of this it was decided that this cable could be used reliably for the purpose of taking measurements at 230°C.

When taking measurements with the spectrum analyzer and signal generator, the loss of the input and output coaxial cables was not negligible and needed to be accounted for. The loss of the cables was measured and corrected in software.

In order to use these coax cables they needed to be cut and crimped to lengths that could run from inside the oven to outside the oven and to the measurement equipment. In order to take high temperature measurements, the coaxial cables were run from the RF measurement equipment to the DUT via the oven heat regulation vents as shown in Figure 35. The coaxial cables were set-up like this for all high temperature testing done in this work.

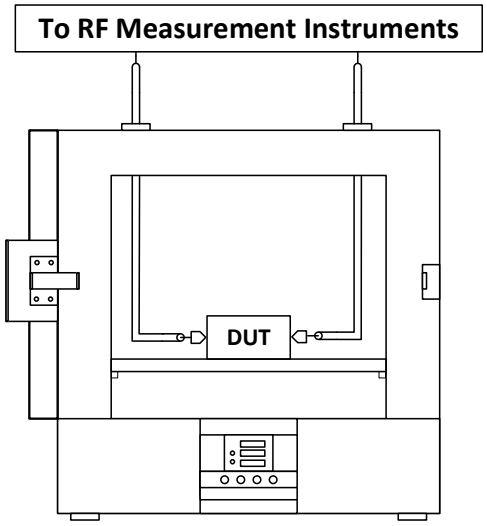

Figure 35: Yamato Oven and Coaxial Cables Measurement Set-up

VNA Calibration

The VNA needed to be calibrated in order to take accurate and reliable measurements on the final PA design. It was calibrated using a calibration kit which included an open, short, 50Ω, and through connection. The instrument was calibrated to the ends of the input and output RF coaxial cables so they would become the new measurement plane. Figure 36 shows in red where the VNA measurement plane was set and calibrated to.

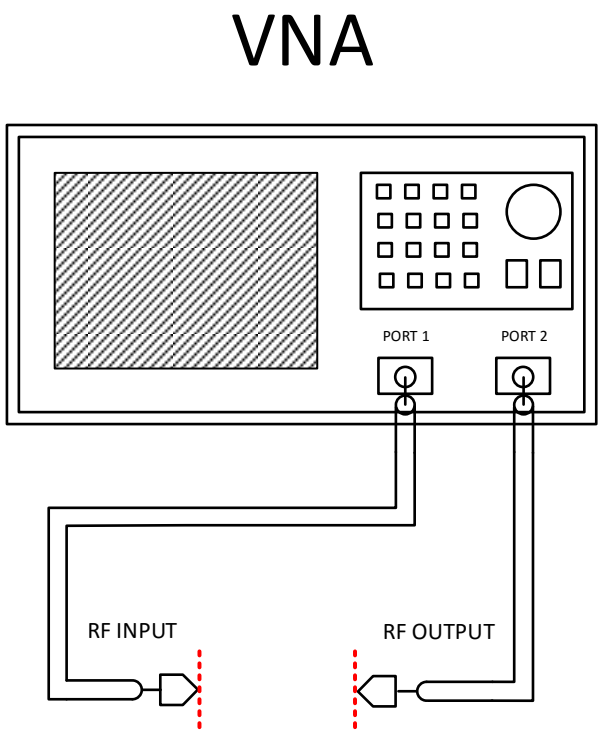

Figure 36: VNA Calibration

De-embedding Process

In order to take s-parameter measurements on the passive components, mounting screws, and the active device, the PCB board which the components were soldered to needed to be de-embedded. After calibrating to the ends of the input / output coaxial cables, the port extension utility on the VNA was used to move the measurement plane to the points on the PCB where each device to be measured was soldered. The port utility tool for the ZVL13 uses PCB board information (length of the input / output PCB lines and board permittivity) to de-embed the board from measurements. This de-embedded setup is shown in Figure 37. The red dotted lines show where on the PCB the port extension was used to. The DUT would sit at the center for a PCB board where the 'X' is placed. It should be noted that the active device needed to be biased using bias tees and these bias tees were simply de-embedded using the same procedure as discussed.

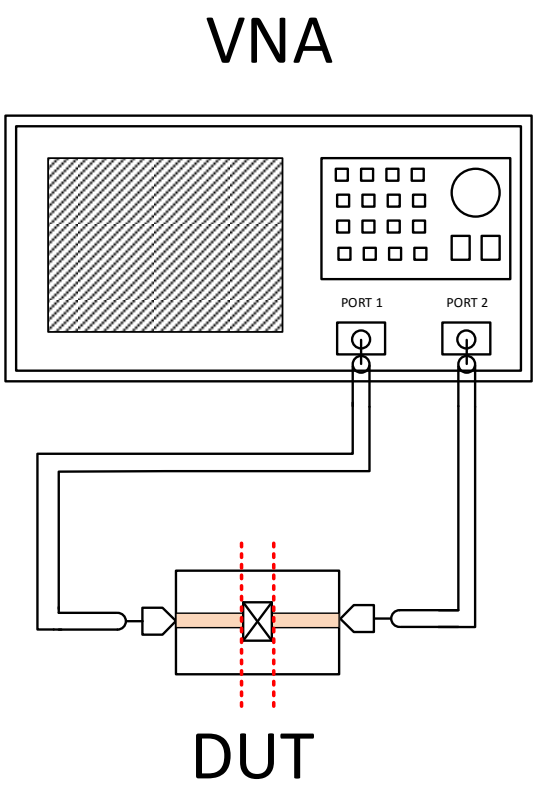

Figure 37: De-Embedding Process for VNA

Measurement Procedure

Measuring I/V Characteristics

I/V characteristics were measured with the Accent Optical Technologies DiVA D265 Dynamic I(V) Analyzer. Measurements were taken by connecting input and output coaxial cables to the gate and drain of the active device which was placed inside the oven just as showed in the previous section. Measurements were first taken at room temperature and then at intervals until the desired temperature of 230°C was reached. In order to ensure the active device would not get damaged at high temperatures pulsed I/V characteristics were taken as opposed to static I/V characteristics. The gate and drain voltages were sweep ranges were based on the bias point of $V_D = 28V$ and $I_D = 200mA$.

As temperature was increased, the gate voltage required to source the desired drain current of $I_D = 200mA$ was found to decrease. Not only did the gate voltage decrease but V_G was not always the same and varied by up to 10mV between each subsequent measurement from the initial value of V_G. The gate voltage was carefully monitored as temperature increased in order to make sure the I/V curves showed the drain current of $I_D = 200mA$. At room temperature it was found that the gate voltage required to set the desired drain current was found to be approximately $V_G = -2.6V$ and when the temperature had been increased to 230°C the gate voltage required had decreased significantly to approximately $V_G = -3.3V$.

The gate voltage was set to sweep from $V_G = -3V$ to $V_G = -2.7V$ at room temperature and was adjusted to sweep from $V_G = -3.6V$ to $V_G = -3.1V$ at 230°C. The drain voltage was set to sweep from $V_D = 0V$ to $V_D = 30V$. A maximum power rating on the instrument was set to be $P_D = 5.6W$ based on the bias point / thermal calculations in order to ensure safe operation.

Measuring S-Parameters / Stability

S-parameters were measured with the Rohde & Schwarz ZVL13 VNA. Measurements were taken on capacitors, resistors, inductors, mounting screws, and the active device chosen. After measuring s-parameters for each individual component and using these measured results to design the PA, s-parameters were taken for the final PA design.

The first step in taking s-parameters was calibrating the instrument to the ends of the input / output coaxial cable. The calibration was done from 9kHz to 1GHz to be able to see a wide range of response from each component to be measured. The internal attenuation was set to -30dBm at the receiving port of the VNA to ensure no damage to the instrument.

The passive components, mounting screws, and active device were each soldered individually to their own perspective PCB board. Once soldered / mounted to the PCB, the DUT was placed inside the oven. After placed in the oven the VNA port extension tool as used to move the measurement plane to the input / output of each component. Measurements were first taken at room temperature and then at intervals until the desired temperature of 230°C was reached.

For the s-parameter measurements taken on the final PA, the same calibration setting were used and the instrument was calibrated to the input / output coaxial cables. The final PA was also placed in the oven exactly as the individual components were. The only difference between these s-parameter measurements was that no port extension was used. Once the s-parameters were taken for the final design at the desired ambient temperature, stability parameters were calculated in ADS from the measured s-parameters.

Measuring 1dB Compression

1dB compression was measured using the Keysight E8257D PSG Analog Signal Generator and the Anritsu MS2665C spectrum analyzer. These measurements were first taken for the active device alone and then taken on the final PA design and the measurement procedure was the same for both. Just as was the case for the other measurements, measurements were first taken at room temperature and then at intervals until the desired temperature of 230°C was reached.

Measurements for the active device alone were taken by connecting input and output coaxial cables to the gate and drain of the active device which was placed inside the oven. The input coaxial cable was connected to the signal generator and the output was connected to the spectrum analyzer. Before beginning the measurements the loss of the input and output coaxial cables was measured. This was done by connecting each cable separately from the signal generator to the spectrum analyzer and setting the signal generator to output a known power level at a specified frequency. Once the loss of both cables was measured these losses were input into Excel to be accounted for.

After measuring the cable losses it was possible to take the compression measurements. The input power was swept from -10dBm to +10dBm at the center frequency and the edges of the specified bandwidth. The spectrum analyzer was set to sweep from 200 MHz to 300MHz in order to see the output power level of the DUT. Input and output power were input into Excel and corrected based on the loss of the cables.

Compression measurements for the final PA design were taken following the same procedure.

Measuring PAE

PAE for the final PA was measured using the Keysight E8257D PSG Analog Signal Generator, the Anritsu MS2665C spectrum analyzer, and a DC voltage supply. These measurements were only taken at the desired ambient temperature of 230°C.

Measurements were taken by connecting input and output coaxial cables to the final PA design which was placed inside the oven. The input coaxial cable was connected to the signal generator and the output was connected to the spectrum analyzer.

The input power was swept from -10dBm to +10dBm at the operation center frequency. The spectrum analyzer was set to sweep from 200 MHz to 300MHz in order to see the output power level of the DUT. While sweeping the input RF power the DC power consumption was noted.

The PAE was calculated in excel using the measured results at 230°C.

Measuring OIP3

OIP3 was measured using the Keysight E8257D PSG Analog Signal Generator, the E4408B ESA-L Basic Spectrum Analyzer, and the Anritsu MS2665C spectrum analyzer. These measurements were first taken for the active device alone and then taken on the final PA design and the measurement procedure was the same for both. Just as was the case for the other measurements, measurements were first taken at room temperature and then at intervals until the desired temperature of 230°C was reached.

Measurements for the active device alone were taken by connecting input and output coaxial cables to the gate and drain of the active device which was placed inside the oven. Coaxial cable and a combiner were used to combine the input signal from the E8257D and E4408B to the input of the active device and the output was connected to the spectrum analyzer. Before beginning the measurements the loss of the input and output coaxial cables was measured and corrected for in Excel just as done for 1dB compression measurements.

After measuring the cable losses it was possible to take the OIP3 measurements. The first signal generator was set to output a tone at 240MHz and the other was set to generate a tone at 260MHz. This was done so that the intermodulation products would cover the specified frequency range. The input signal power level from both the signal generators was equal and was set to a power level within the active device's linear range. The spectrum analyzer was set to sweep from 200 MHz to 300MHz in order to see the intermodulation products of the DUT.

The fundamental tone power levels at 240MHz and 260 MHz was measured and the power levels of the third order products was also measured at 220MHz and 280MHz.

The measurement procedure was repeated for the final PA design.

Measured Results

Measured I/V Characteristics

As stated previously, the device began to conduct at lower gate voltages as temperature was increased. Figure 38 shows the measured I/V characteristics at room temperature and Figure 39 shows the measured I/V characteristics at 230°C. The gate voltages are shown in the legends below the graphs. After measuring these results at 230°C it was evident that the chosen bias point could be used to operate the device in class A operation as desired.

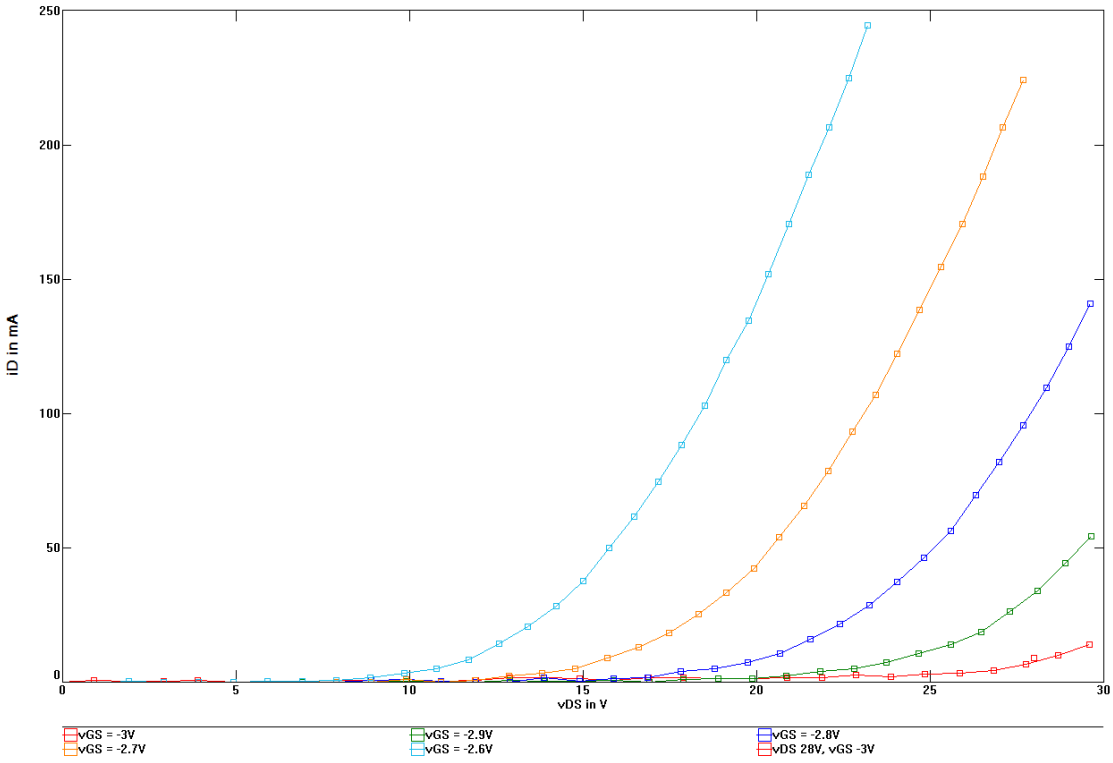

Figure 38: Measured I/V Characteristics Room Temperature

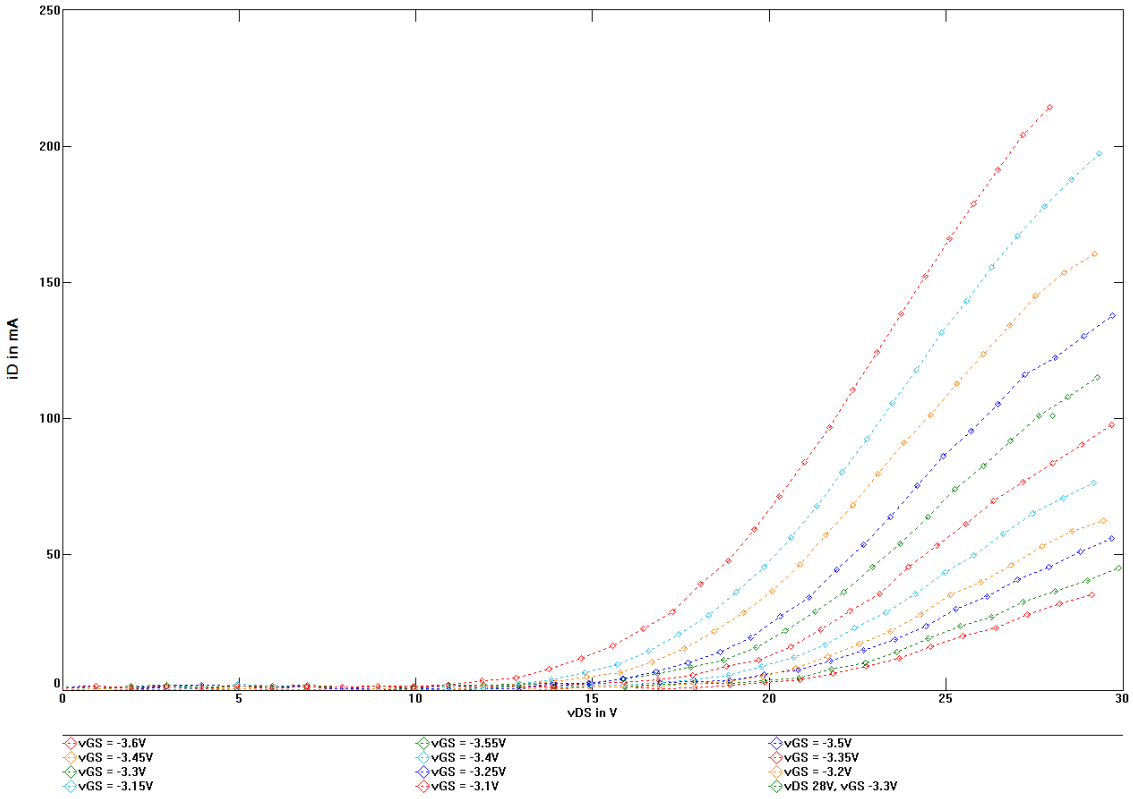

Figure 39: Measured I/V Characteristics at 230°C

Measured S-Parameters at 230°C

Because the PA was designed only to operate at 230°C, measurements were only taken on the final design at the desired temperature and not at room temperature or incrementally up to 230°C. The measured s-parameters at 230°C are shown in Figure 40.

The parameters that were designed for were IRL and gain so these are shown in more detail in Figure 41. The measured gain matched the simulated gain very closely and this is shown in Figure 42. The measured IRL matched the same shape as the simulated IRL but did provided lower IRL than expected. After RF tuning did not help to improve the design it was found that from a system standpoint the system could withstand the non-ideal IRL. The measured and simulated IRL are shown in Figure 43.

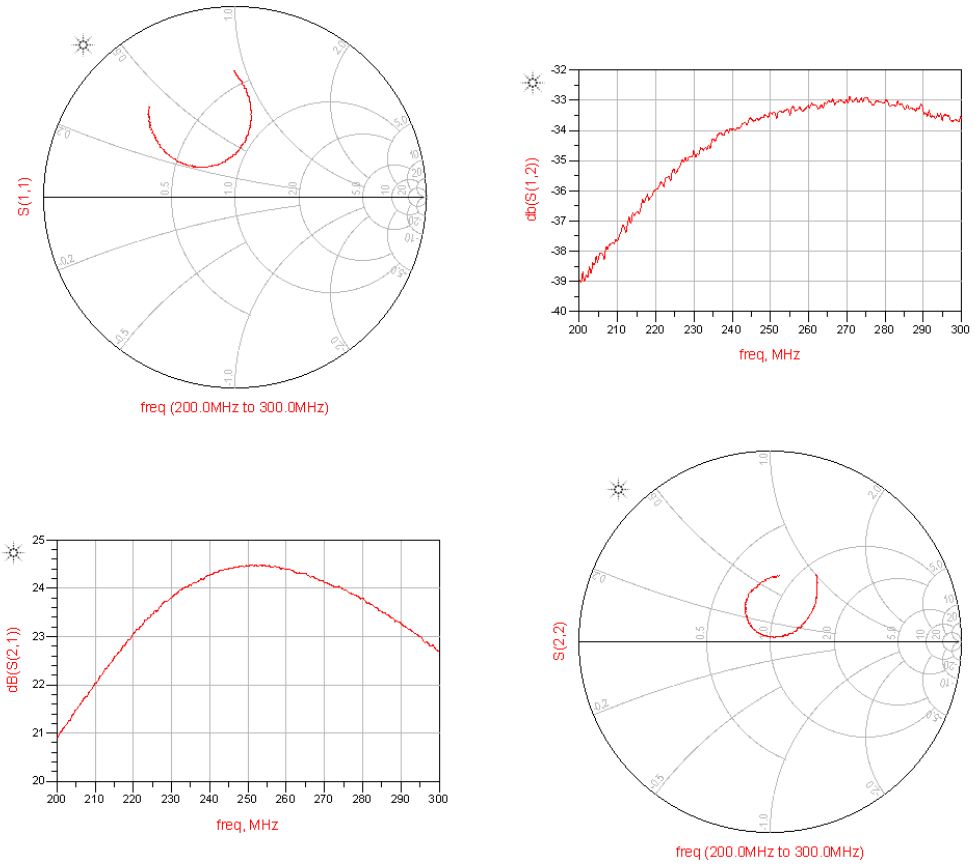

Figure 40: Measured S-Parameters at 230°C

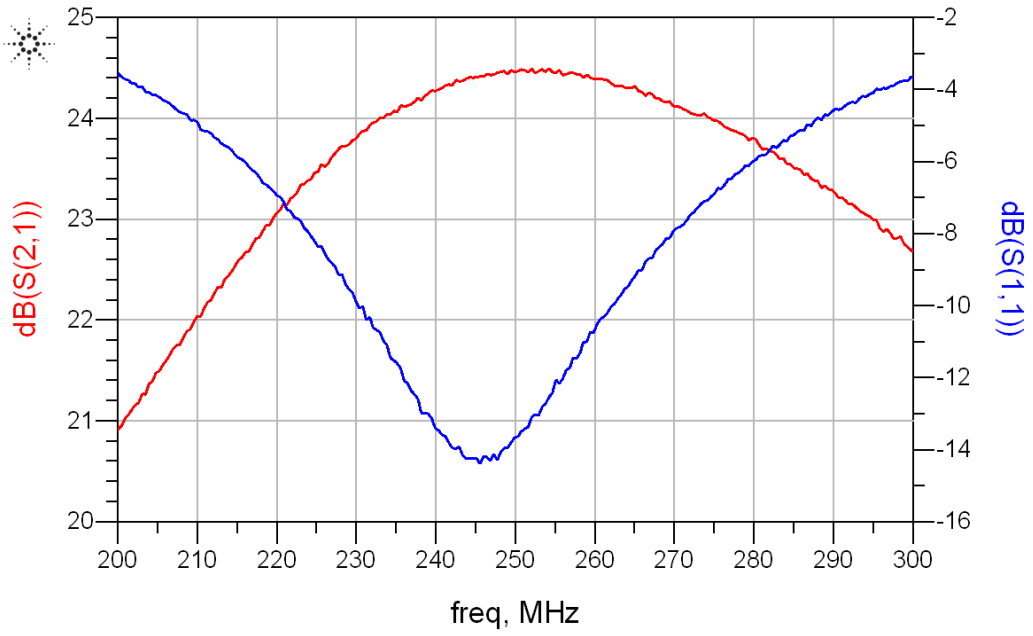

Figure 41: Measured Gain and IRL at 230°C

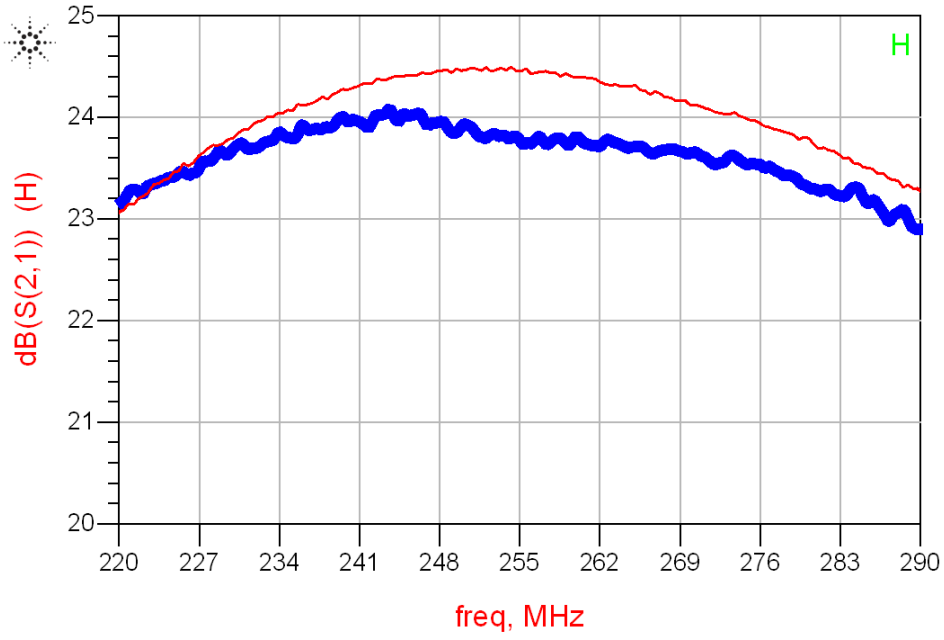

Figure 42: Measured Gain (red) vs. Simulated Gain (blue)

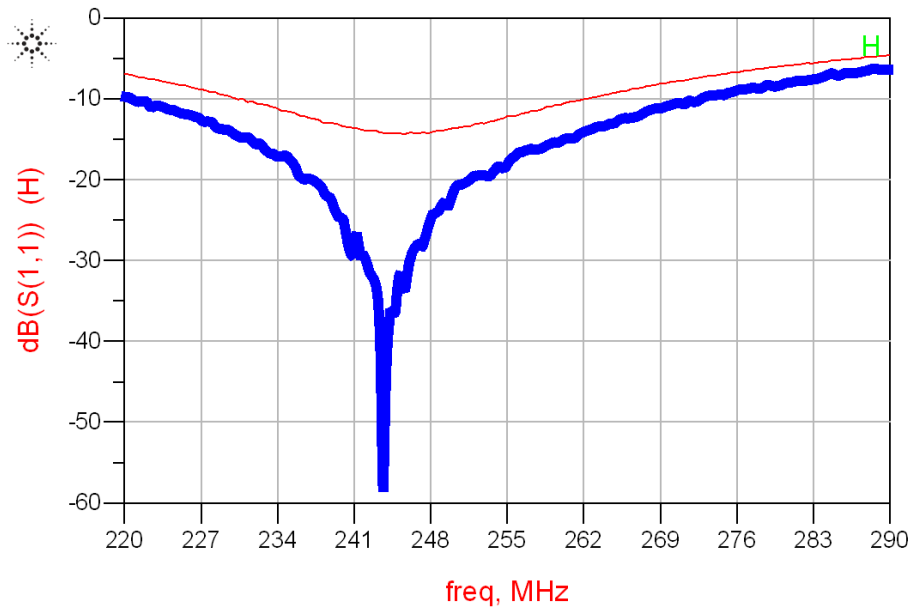

Figure 43: Measured IRL (red) vs. Simulated IRL (blue)

Measured Stability at 230°C

It was possible to calculate the stability of the final PA in ADS using the measured s-parameters at 230°C. It is clear from Figure 44 the PA was stable in the specified frequency range. Not only was the PA stable in the specified frequency range but also over a wider range of frequencies in order to ensure no oscillations. The device is conditionally stable from approximately 350MHz to 520MHz but this was not seen as a problem in the design and the PA was not found to oscillate at any point in its operation.

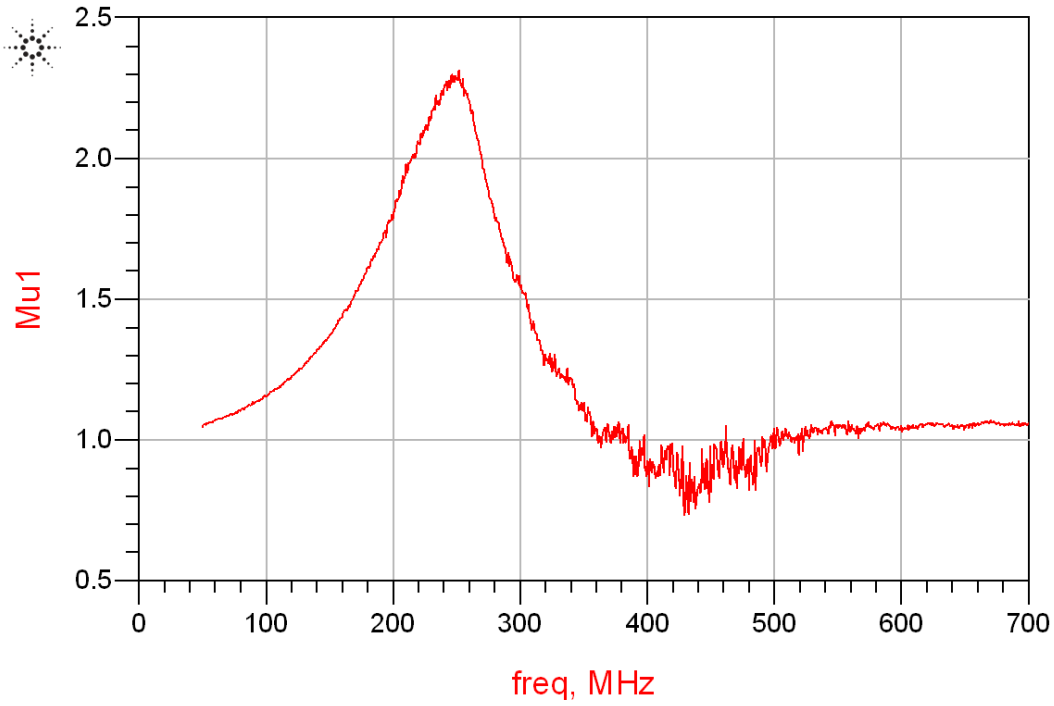

Figure 44: Measured Mu at 230°C

Measured 1dB Compression at 230°C

The measured 1dB compression for the final PA is shown in Figure 45. From the figure it was found that the compression level was approximately 32dBm. As expected, this compression level did not change from the measured results for the device alone shown in Chapter 3.

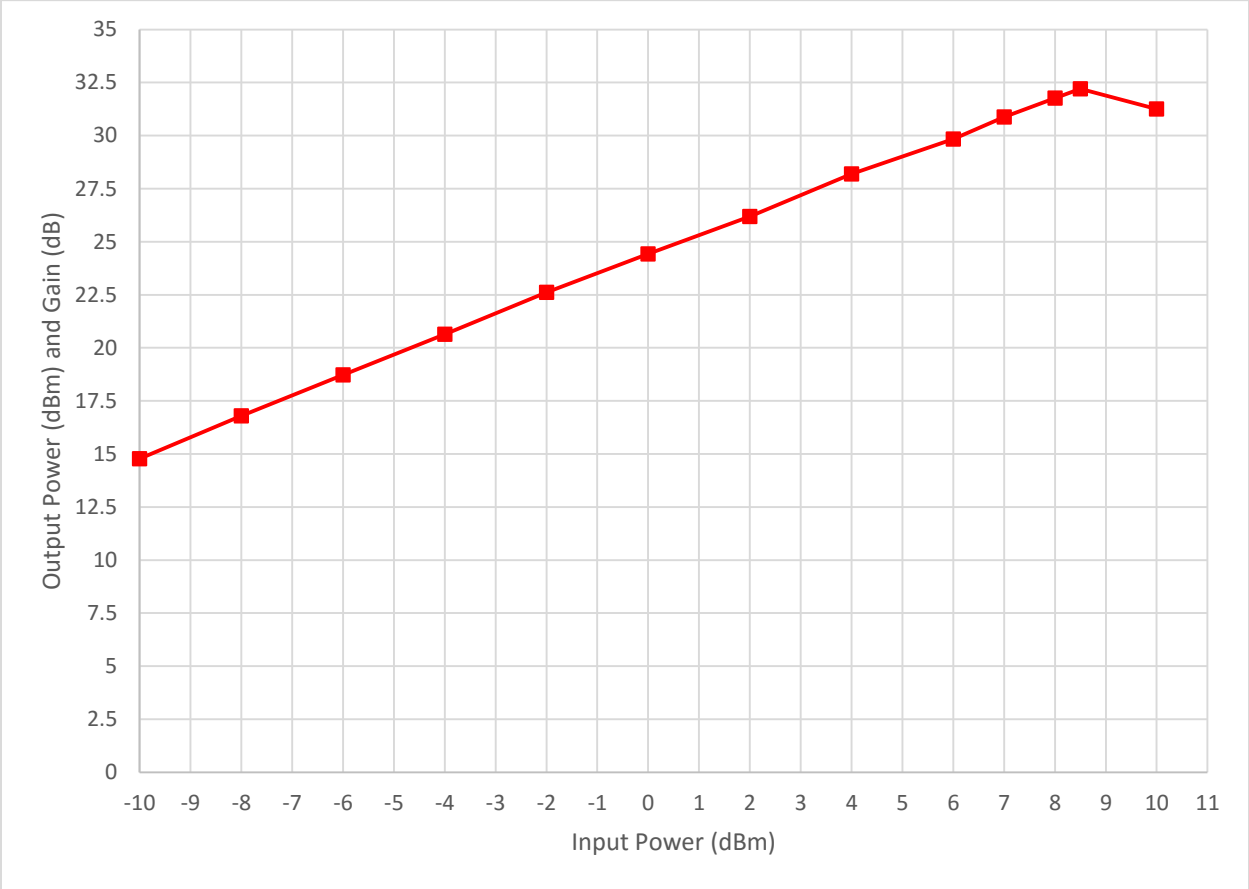

Figure 45: Measured 1dB Compression at 230°C

Measured OIP3 at 230°C

The measured OIP3 for the final PA is shown in Table 8. As expected, this OIP3 did not change significantly from the measured results for the device alone shown in Chapter 3. Also, the OIP3 was higher than the 1dB compression level as expected.

Fundamental Input Power	-18 dBm
Fundamental Output Power	3.84 dBm
Third Order Output Power	-64.27 dBm
Output Third Order Intercept Point	37.89 dBm

Table 8: Measured OIP3 at 230°C

Measured PAE at 230°C

The PAE for the device is shown in Figure 46. This is slightly lower than the expected PAE for a class A device but was deemed fine as PAE was not a parameter that was designed for.

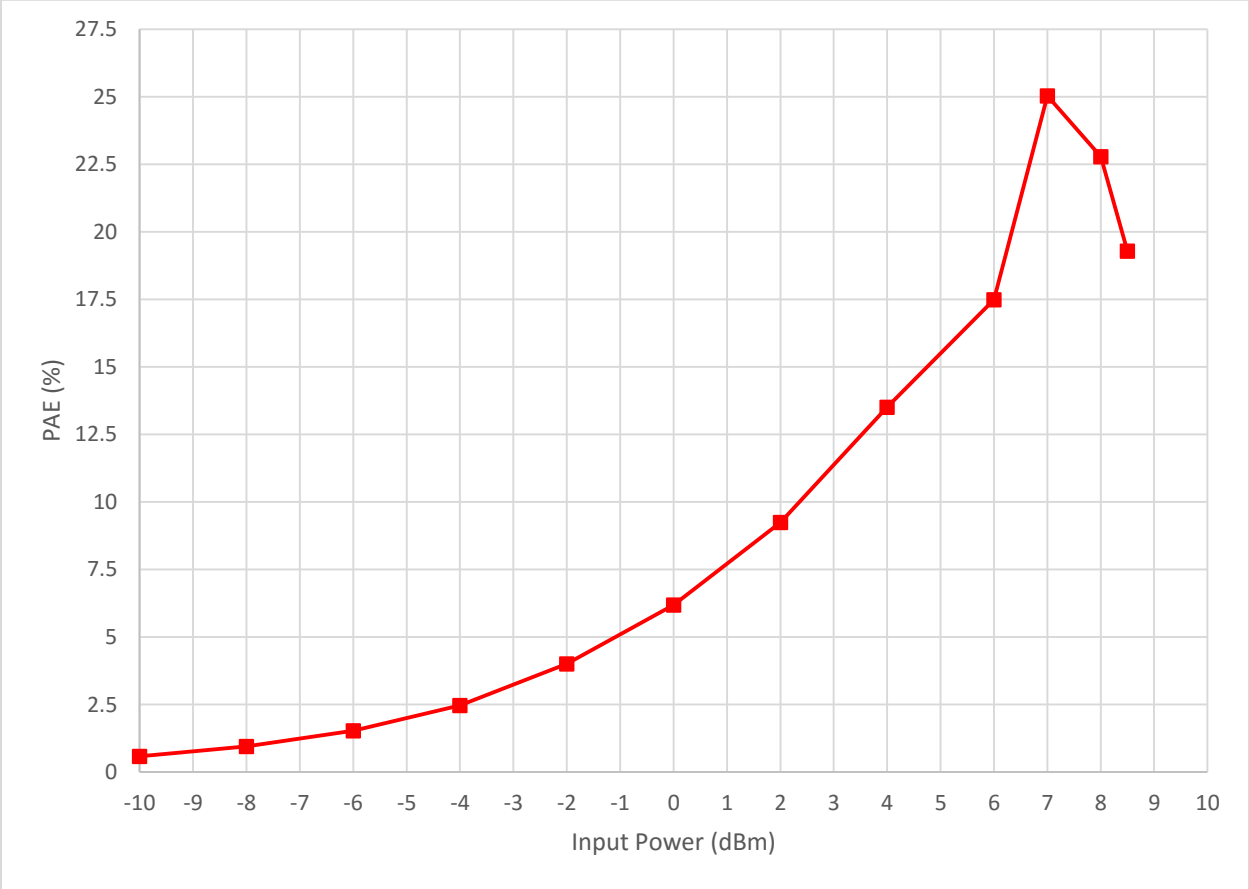

Figure 46: Measured PAE at 230°C

Final Measured Results

The final measured performance and design requirements are compared below in Table 10.

Design Parameter	**Design Requirement**	**Measured Performance**
Operation Temperature	230°C	230°C
Operation Frequency	225MHz – 285.5MHz	225MHz – 285.5MHz
Gain	> 15dB	~ 23.5dB – 24.5dB
Gain Ripple	1dB	~ 1dB
Input Return Loss (IRL)	> 10dB	> 6dB
Output Third Order Intercept (OIP3)	> 35dBm	~ 37.9dBm
Output 1dB Compression	> 25dBm	~ 32dBm
Power Added Efficiency (PAE)	-	~ 25.03%

Table 9: Summarized PA Performance

Chapter 5

Conclusion

As the oil industry continues drilling deeper to reach previously untapped wells, the downhole environments are becoming harsher, reaching higher temperatures and pressures which necessitate more robust and higher speed electronics to reliably operate in these environments. By designing electronics that can withstand much higher temperatures, not only can these electronics operate more reliably but also the drilling operations can continue uninterrupted for longer periods of time. This PA was designed as part of a downhole communication system designed to operate above 210°C and as such needed to be designed to reliably withstand these extreme temperatures.

The proposed PA is able to operate up to an ambient temperature of 230°C without the need for active cooling. It operates in class A with a peak PAE of 25.03%, maximum output power of 1.66 W, peak gain of 24.5 dB, center frequency of 255 MHz with 1dB ripple in the passband over a 60 MHz bandwidth, 1dB output compression of approximately 32 dBm, and OIP3 of 37.9 dBm. As discussed previously, the measured IRL did not meet the design requirement but it was later determined that the performance was fine for the system and did not need to be corrected. This performance is summarized in Table 9.

By using passive components, active components, and interface materials able to withstand extreme temperatures at the power ratings used it was possible to complete this design using COTS components. This design is the state-of-the-art for drilling applications as no other downhole electronics used to date are able to withstand these extreme temperatures. In extension, this design is a proof of concept of high temperature operation and its use is not limited to just the drilling industry but can also be used in other high temperature applications such as space, automotive, and the aviation industry. To the knowledge of this author no other RF PA has been designed to operate at this ambient temperature without the need for active cooling.

This design will be improved in the future to operate at a temperature independent bias condition which will allow for little variation in important design parameters such as linearity and gain over temperature. In addition, it will also be improved to consume less power and therefore operate at even higher temperatures. Finally, this PA will eventually be designed into an integrated circuit to have a smaller board footprint so that once it is deployed downhole it will not contribute as much weight to the overall system.

References

[1] C. S. G. DeBrujin, R. Greenaway, D. Harrison, M. Parris, S. James, et al. "High-Pressure High-Temperature Technologies". *Oilfield Review [Downhole Systems] vol. 20,* pp. 46-60.

[2] Schlumberger. (2015), "Surface systems: Data Delivery". *Wireline Services Catalog,* pp. 12-13.

[3] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, 2nd ed. Upper Saddle River, New Jersey: Prentice Hall, 1997.

[4] C. Bowick, J. Blyer, and C. Ajluni, *RF Circuit Design*, 2nd ed.: Elsevier, 2008.

[5] M. L. Edwards and J. H. Sinsky, "A new criterion for linear 2-port stability using a single geometrically derived parameter," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 40, pp. 2303-2311, 1992.

[6] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, New Jersey: Prentice Hall, 2012.

[7] W. S. Janna, *Engineering Heat Transfer* vol. 3. Boca Raton: CRC Press, 2009.

[8] Fairchild, "Heat Sink Mounting Guide," AN-4166 datasheet, 2014 [Revised Jun. 25th, 2014].

[9] T. Chen, W.-M. L. Kuo, E. Zhao, Q. Liang, Z. Jin, J. D. Cressler*, et al.*, "On the suitability of SiGe HBTs for high-temperature (to 300°) electronics," in *Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting*, 2004, pp. 217-220.

[10] G. Wang, G. Qin, Z. Ma, P. Ma, M. Racanelli, and G. E. Ponchak, "Power Performance Characteristics of SiGe Power HBTs at Extreme Temperatures," in *Reliability physics symposium, 2007. proceedings. 45th annual. ieee international*, 2007, pp. 584-585.

[11] M. Bellini, J. D. Cressler, and J. Cai, "Assessing the High-Temperature Capabilities of SiGe HBTs Fabricated on CMOS-compatible Thin-film SOI," in *Bipolar/BiCMOS Circuits and Technology Meeting, 2007. BCTM '07. IEEE*, 2007, pp. 234-237.

[12] K. Fricke, H. L. Hartnagel, W. Y. Lee, and M. Schussler, "AlGaAs/GaAs/AlGaAs DHBT's for high-temperature stable circuits," *Electron Device Letters, IEEE,* vol. 15, pp. 88-90, 1994.

[13] F. Y. Colomb and A. Platzker, "A 3-Watt Q-Band GaAs pHEMT Power Amplifier MMIC For High Temperature Operation," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, 2006, pp. 897-900.

[14] N. S. Rebello, F. S. Shoucair, and J. W. Palmour, "6H silicon carbide MOSFET modelling for high temperature analogue integrated circuits (25-500°C)," *Circuits, Devices, and Systems, IEEE Proceedings,* vol. 143, pp. 115-122, 1996.

[15] D. R. M. Woo, H. H. Yuan, J. A. J. Li, H. S. Ling, L. J. Bum, Z. Songbai*, et al.*, "High power SiC inverter module packaging solutions for junction temperature over 220°C," presented at the Electronics Packaging Technology Conference (EPTC). IEEE 16th, 2014.

[16] B. Grummel, R. McClure, L. Zhou, A. P. Gordon, L. Chow, and Z. J. Shen, "Design consideration of high temperature SiC power modules," in *Industrial Electronics, IECON 34th Annual Conference of IEEE*, 2008, pp. 2861-2866.
[17] M. W. Shin and R. J. Trew, "GaN MESFETs for high-power and high-temperature microwave applications," *Electronics Letters,* vol. 31, pp. 498-500, 1995.
[18] S. Yoshida and J. Suzuki, "Reliability of metal semiconductor field-effect transistor using GaN at high temperature," *Journal of Applied Physics,* vol. 84, 1998.
[19] X. Liu and C. K. J., "GaN Single-Polarity Power Supply Bootstrapped Comparator for High-Temperature Electronics," *Electron Device Letters, IEEE,* vol. 32, pp. 27-29, 2011.
[20] Z. Xu, W. Zhang, F. Xu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Investigation of 600 V GaN HEMTs for high efficiency and high temperature applications," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 131-136.
[21] C. Liu, A. Salih, B. Padmanabhan, W. Jeon, P. Moens, M. Tack*, et al.*, "Breakthroughs for 650-V GaN Power Devices: Stable high-temperature operations and avalanche capability," *Power Electronics Magazine, IEEE,* vol. 2, pp. 44-50, 2015.
[22] A. A. Bajwa, Y. Qin, R. Reiner, R. Quay, J. Wilde, P. Waltereit*, et al.*, "Assembly and Packaging Technologies for High-Temperature and High-Power GaN Devices," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* vol. 5, pp. 1402-1416, 2015.
[23] D. Wolpert and P. Ampadu, "Temperature Effects in Semiconductors," in *Managing Temperature Effects in Nanoscale Adaptive Systems*, ed: Springer, 2012, pp. 15-33.
[24] A. C. Beer, *Semiconductors and Semimetals: Deep Levels, GaAs, Alloys, Photochemistry*, 1st ed. vol. 19, 1983.
[25] B. V. Zeghbroeck. (2011). *Principles of Semiconductor Devices*. Available: http://ecee.colorado.edu/~bart/book/book/contents.htm
[26] R. C. Jaeger and T. N. Blacock, *Microelectronic Circuit Design*, 4th ed. New York, NY: McGraw-Hill, 2011.
[27] Hittite, "Thermal Management for Surface Mount Components," 2012.
[28] A. Semiconductor, "AN-1011: Defining Maximum Operating Junction Temperature (TJ)," 2005.
[29] B. Ozpineci and L. M. Tolbert, "Comparison of Wide-Bandgap Semiconductors for Power Electronics Applications," Oak Ridge National Laboratory 2003.
[30] C. Yu and J.-S. Yuan, "Electrical and Temperature Stress Effects on Class-AB Power Amplifier Performances," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 1346-1350, 2007.
[31] K.-M. Chen, A.-S. Peng, G.-W. Huang, H.-Y. Chen, S.-Y. Huang, C.-Y. Chang*, et al.*, "Linearity and power characteristics of SiGe HBTs at high temperatures for RF applications," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 1452-1458, 2005.

[32] S. Chen and J. S. Yuan, "Adaptive Gate Bias for Power Amplifier Temperature Compensation," *Device and Materials Reliability, IEEE Transactions on,* vol. 11, pp. 442-449, 2011.
[33] C.-H. Liao, C.-M. Tang, K.-L. Chen, D.-C. Niu, and R. Hu, "The design of 14GHz temperature-compensated 20Watt power amplifier module," in *Electric Information and Control Engineering (ICEICE), 2011 International Conference on*, 2011, pp. 2740-2742.
[34] F. Yamaki, K. Inoue, N. Ui, A. Kawano, and S. Sano, "A 65 % drain efficiency GaN HEMT with 200 W peak power for 20 V to 65 V envelope tracking base station amplifier," in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, 2011, pp. 1-4.
[35] TriQuint, "30W, 28V DC - 6GHz, GaN RF Power Transistor," T2G6003028-FL datasheet, Rev A. [Revised Dec. 2013].
[36] Chemtronics, "CircuitWorks Silver Conductive Grease," CW7100 datasheet, 2013.
[37] Wakefield-Vette, "Extruded Heat Sinks for Power Semiconductors," 423K datasheet, Jun. 2007.
[38] Coilcraft, "Extreme Temperature Coil," AT549RBT datasheet, 2014.
[39] IPDiA, "XTSC423.xxx - 0201 Extreme Temperature Silicon Capacitor," XTSC423 datasheet, 2014.
[40] Vishay Dale, "Precision Automotive High Temperature (155C at full rated power) Thin Flim Chip REsistor, AEC-Q200 Qualified," PATT datasheet, 2012 [Revised Oct].
[41] R. Corperation, "R04000 Series High Frequency Circuit Materials," R04000 Series datasheet, 2015.
[42] G. Gonzalez, "Matching Networks and Signal Flow Graphs," in *Microwave Transistor Amplifiers*, 2nd ed Upper Saddle River, NJ: Prentice Hall, 1997, p. 144.
[43] IndiumCorperation, "Indium Corp. Indalloy 151 Pb-Sn-Ag Solder Alloy," Indalloy 151 datasheet.
[44] Yamato, "Intruction Manual For Gravity Convection Ovens," DX300 datasheet, 2006.
[45] R. Schwarz, "R&S ZVL Vector Network Analyzer Operating Manual," ZVL datasheet, 2015.
[46] Anritsu, "MS2665C Spectrum Analyzer 9kHz to 21.2GHz," MS2665C datasheet, Jun. 2003.
[47] K. Technologies, "E8257D PSG Microwave Analog Signal Generator," E8257D PSG datasheet, 2015.
[48] Agilent, "ESA-L Series Spectrum Analyzers Data Sheet," ESA-L datasheet, 2012.
[49] Accent, "DiVA Dynamic I(V) Analyzer," D265 datasheet.