

A High Temperature Wideband Low Noise Amplifier

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Abstract

As the oil industry continues to drill deeper to reach new wells, electronics are being required to operate at extreme pressures and temperatures. Coupled with substantial real-time data targets, the need for robust high speed electronics is quickly on the rise. This paper presents a high temperature wideband low noise amplifier (LNA) with zero temperature coefficient maximum available gain (ZTC_{MAG}) biasing for a downhole communication system. The proposed LNA is designed and prototyped using $0.25\mu\text{m}$ GaN on SiC RF transistor technology, which is chosen due to the high junction temperature capability. Measurements show that the proposed LNA can operate reliably up to an ambient temperature of 230°C with a minimum noise figure (NF) of 2.0 dB, gain of 16.1 dB, and P1dB of 19.1 dBm from 230.5MHz – 285.5MHz. The maximum variation with temperature from 25°C to 230°C is 1.53dB for NF and 0.65dB for gain.

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Abbreviations

ADS	Advanced Design System (Keysight EEsof)
BOM	Bill of Materials
CD	Common Drain
CG	Common Gate
CMOS	Complementary Metal-Oxide Semiconductor (typically on Si/poly-Si/SiGe)
COTS	Commercial Off-the-Shelf
COTS	Commercial Off-the-Shelf
CPES	Center for Power Electronics Systems
CS	Common Source
DUT	Device Under Test
ENR	Excess Noise Ratio
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FD	Fully Depleted
FP	Field Plate
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IRL	Input Return Loss
LNA	Low Noise Amplifier
MAG	Maximum Available Gain
MSG	Maximum Stable Gain
NF	Noise Figure
NF _{min}	Minimum Noise Figure
OIP2	Output Second-order Intercept Point
OIP3	Output Third-order Intercept Point
OP1dB	Output 1-dB Compression Power
ORL	Output Return Loss
PA	Power Amplifier
PD	Partially Depleted
PTAT	Proportional to Absolute Temperature
RBW	Resolution Bandwidth
RF	Radio Frequency
SiC	Silicon Carbide
SMA	Sub-miniature A (connector type – mates with 3.5mm precision connectors)
SMT	Surface-Mount Technology
SOI	Silicon-on-Insulator
SRF	Self-Resonant Frequency
UWB	Ultra-wide Bandwidth
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency (IEEE; 30MHz – 300MHz)
VSWR	Voltage Standing Wave Ratio
ZTC	Zero-Temperature Coefficient

Chapter 1

1 Introduction

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1.1 Preface

Since the beginning of electrical communications in the 1800s, the boundaries of electronics have constantly been pushed to achieve more functionality and better performance. In today's society, the push is often an improvement over an existing system, but there has recently been a demand for electronics that can operate in harsh environments and can match the data performance and operation performance capable in normal environment systems.

A number of extreme environment industries, such as automotive, turbine engines, spacecraft, industrial, and deep-well drilling exist today with the incorporation of electronics to aid in the data capture and system performance.

1.2 Motivation

In each of the industries mentioned, the current capabilities of the electronic systems are limited by the functionality of the devices when placed directly in contact with the harsh environment. For this reason, the system is often isolated in some way from the environment, which typically reduces performance capability, or the capability is

drastically reduced (e.g. low frequency operation) in order to even function directly in the environment.

This calls for a tremendous opportunity to develop RF circuits that can work in extreme environments. High temperature, specifically, is one of the more interesting aspects and also seems to be one of most limiting factors. Since, as the temperature rises, less and less materials can maintain useful properties for electrical operation, the task of designing systems that can function has been limited. This is especially true in the RF and microwave fields due to the already difficult performance requirements at high frequency. With recent technological advancements, design for high temperature applications has finally become a possibility that shows improvement of existing systems and further extends the capabilities of extreme temperature systems.

1.2.1 Applications

In automotive, turbine, and spacecraft control engine data cannot easily be obtained do to the extreme temperatures in engines and jet propulsion (well over 500°C to several thousand degrees Celsius). Space instruments also can suffer from overheating via radiation which causes instrument failure. For industrial and geothermal, the temperatures can also reach hundreds of degrees. Industrial equipment often requires precise control of temperatures for manufacturing. Being able to increase the data rate and improve in the speeds and reliability will lead to advancements in the scientific understanding of our surrounding and allow many industries to create better products (through data logging).

Specifically, the oil industry has gradually moved to deeper and deeper wells to explore new reservoirs; however, the tools required to do so have become incapable of the harsher high pressure, high temperature (HPHT) environments. Figure 1.1 shows the classification system used in the oil industry, which is based on the limitations of current electrical and mechanical systems. HPHT is classified from temperature of 205°C – 260°C up to 241MPa and ultra-HPHT (the most extreme class) is rated at 260°C – 315°C up to 276MPa. In order to operate electronic systems at these extreme temperatures, mechanical insulation, such as installation of internal heatsinks and vacuum flasks for temperature shielding, are used [1]. In addition to these physical limits, the current systems use low frequency circuits that can achieve data rates of only approximately 4Mb/s at temperatures < 210°C [2].

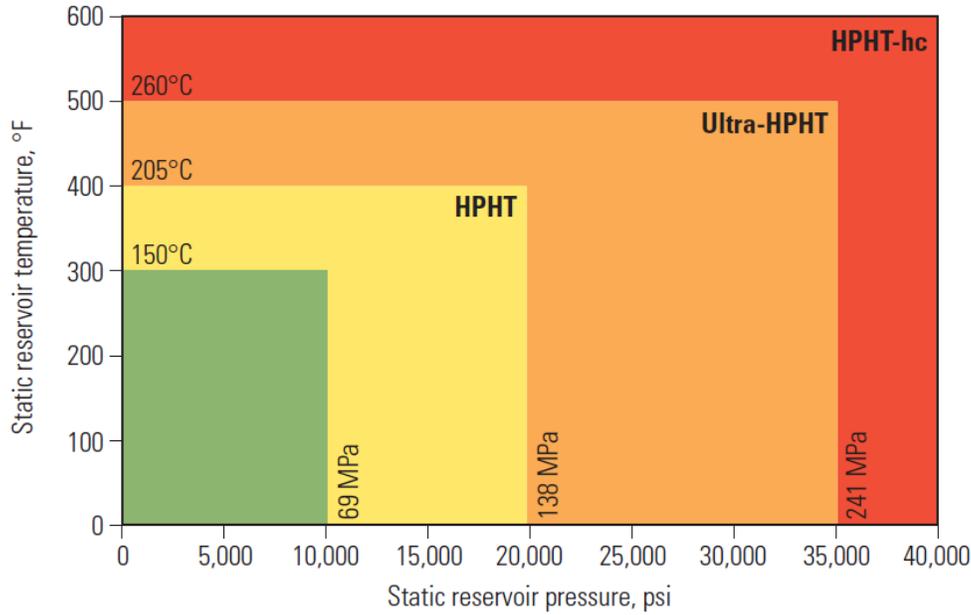


Figure 1.1: HPHT classification system [1] [fair use]

The mechanical and electrical systems in downhole operation are merely being buffered from the harsh conditions of downhole operation through the use of large heatsinks or vacuum tubes. This means that the time that they can operate reliably while drilling is short before the tools. As a result, the tools need to be regularly brought back to the surface in order to ensure they are not damaged [1].

The primary difficulty for downhole electronics is the temperature limitation, being that the pressures are handled mechanically. By increasing the ambient temperature capability, longer logging times and deeper drilling depths are capable. Several methods can be employed to achieve this with commercial off-the-shelf (COTS) devices: (i) increased max temperature capabilities of the devices, (ii) reduced power consumption of the devices, and (iii) reliable cooling and heat extraction techniques while downhole. The latter of the three is very impractical and is not investigated in this work.

1.2.2 Maturing Technology

One of the major reasons that extreme temperature RF electronics is even possible is due to the more recent advancements in device technology. Improvements in the fabrication of wide bandgap semiconductors that can also operate at RF frequencies along with the improved thermal packaging allows for these newer technologies to surpass the ubiquitous technologies for typical consumer electronics. Well matured technology can

withstand only a fraction of the intended need, requiring the use of mechanical systems to help extend the capabilities, but at little benefit. Although improvements in the properties of common technologies have helped, temperature extending techniques still hit theoretical physical property limits that barely even scrape the surface of possible applications.

Although relatively new in the commercial world, GaN was found to be the most promising technology for this application. GaN offers a reliable combination of high temperature and high frequency capability [3]. It also has been shown to be thermally robust [4] and can have very low NF [5] while simultaneously achieving high gain and high linearity. Although GaN is still in its nascent stages, the research into fabrication and reliability shows that it is a very promising technology [6]. SiC, alone, can reach high temperatures [3], but choosing a technology that operates at higher frequencies allows for the push into the radio and microwave bands, leading to much higher data rates.

To reduce power, the use of a transistor with small gate leakage current and low drain voltage allows for the low power control of the device current, which will be the primary factor in determining performance.

1.3 Summary

The LNA discussed herein has been designed as part of a downhole communication system under no existing limitations in frequency band or performance other than those determined through a system simulation.

The proposed LNA is designed and prototyped using 0.25 μ m GaN on SiC RF transistor technology, which is chosen due to the high junction temperature capability. A common source configuration with resistive feedback was selected for topology based on the stability and noise figure performance when the input is mismatched (for noise). Measurements show that the proposed LNA can operate reliably up to an ambient temperature of 230°C with a noise figure (NF) of 2.06 dB – 2.90dB, gain of 16.16 dB \pm 0.3dB, output return loss (ORL) of >15dB, and output 1-dB compression point (OP1dB) of 19.1 dBm over the frequency range of 230.5MHz – 285.5MHz. The maximum variation with temperature from 25°C to 230°C is 1.53dB for NF and 0.65dB for gain.

This is the first RF LNA that has been designed using GaN and operates at high temperatures above 200°C that exists in the literature at the time of this writing. Although other designs have managed temperature compensation in RF frequencies and numerous GaN LNAs have been made, none exploit the high temperature capabilities described in this work.

1.4 Thesis Organization

The organization of this thesis is as follows: Chapter 2 provides the most important background information that will be required to follow this work. Also covered is a literature review of existing works related to this design. Chapter 3 covers, in depth, the design process to achieve the listed specifications in the beginning of the chapter. The schematic is presented followed by a functional description of each component and the necessary considerations for use at high temperature. After individual components are covered, the RF topics are investigated and the chapter is concluded with the layout of the design. In Chapter 4 the measurement results of the design are covered in depth. All relevant RF tests are done and evaluated. Following the discussion of each test, the total results of performance over 25°C to 230°C are detailed in a single table to summarize. Finally, Chapter 5 concludes the work through investigation of issues and possible complications. With that covered, possible future work in the area is developed given the results of this proof of concept work.

Chapter 2

2 Background

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Chapter 2 covers brief details of some important concepts used in the design and testing of this LNA. It also highlights high temperature works with a literature review on relevant LNA works.

2.1 Definitions and Concepts

2.1.1 Bandwidth

Bandwidth is used to mean several different measurement points when used for different applications. For RF design, the term typically refers to the half power bandwidth response of a filter or filtered amplifier. It is defined as the frequency span where the maximum gain or in-band gain remain above half power (i.e. have not dropped by 3dB). All uses in this work will use the 3-dB bandwidth term and specify the power bandwidth if it is not 3dB.

The term wideband, which is used in the title, is generally accepted to mean a system that has a bandwidth that covers more than one transmit or receive channel in a system.

2.1.2 S-parameters

Scattering parameters (known as s-parameters) are a notation used in RF applications that make measurements in the microwave band obtainable (the short and open circuits used for z, y, h, and ABCD parameters are difficult to implement over broadband and could also cause the DUT to oscillate [7]). They are characterized in terms of travelling waves. A two-port would have four s-parameters representing forward gain, reverse transmission, and input/output return loss.

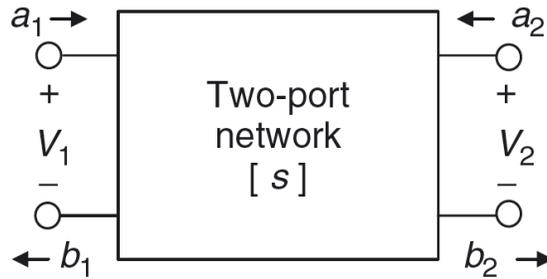


Figure 2.1: Two-port network representation for s-parameters [8] [fair use]

The a and b in Figure 2.1 represent normalized voltage waves traveling in the forward and reverse directions, respectively. This method allows for the small signal characterization of a two port using a single load matched to the characteristic impedance at each port [7]. It should be noted that the square of these wave are known as power waves. The following definitions assume a Z_0 system.

2.1.2.1 Forward Transmission

Forward transmission (i.e. forward gain) is the power gain observed from a voltage wave input at port 1 and measured at port 2 with no input at port 2.

$$s_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad (2.1)$$

If the magnitude of this value is squared, we can obtain a power gain

$$\text{Forward Transmission} = |s_{21}|^2(\text{dB}) = 20 \log \left(\frac{b_2}{a_1} \right) \bigg|_{a_2=0} \quad (2.2)$$

2.1.2.2 Reverse Transmission

Reverse transmission is the power gain observed from a voltage wave input at port 2 and measured at port 1 with no input at port 1. This parameter helps in determining

isolation from reflected and leaked signals at the output back to the input (which can lead to instability and distortion).

$$s_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad (2.3)$$

If the magnitude of this value is squared, we can obtain a power gain

$$\text{Reverse Transmission} = |s_{12}|^2 (dB) = 20 \log \left(\frac{b_1}{a_2} \right) \Big|_{a_1=0} \quad (2.4)$$

2.1.2.3 Return Loss

Return loss the reflected power observed from a voltage wave input at a port and measured at the same port with no input at the other port. It can also be expressed as a reflection coefficient at the port (in the equation below, Z_{T1} is the impedance seen looking into port 1).

$$s_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = \Gamma_{in} = \frac{Z_{T1} - Z_0}{Z_{T1} + Z_0} \quad (2.5)$$

If the magnitude of the inverse value is squared, we can obtain a return loss in power terms:

$$\text{Input Return Loss (IRL)} = |s_{11}|^{-2} (dB) = -20 \log(\Gamma_{in}) \quad (2.6)$$

where the same procedure is done for output return loss (ORL) with S_{22} .

These parameters are very useful for determining negative resistances generated by the two-port (which can lead to instability) and also detail the power lost at interfaces that and is reflected toward the sending end (which can cause distortions).

2.1.3 Noise Figure

Noise figure (noise factor in linear units) is a measure of the total output noise power relative to the total output noise power *if* the DUT added no noise (meaning that the source noise only experiences the gain of the DUT without more noise being added in).

Noise factor can be expressed in several forms, some of which are expressed below:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_i N_o}{S_o N_i} = \frac{1 N_o}{A_v^2 N_i} = \frac{N_o}{(4kTR_s)A_v^2} = 1 + \frac{N_a}{A_v^2 N_{RS}} \quad (2.7)$$

where SNR is the signal-to-noise power ratio, A_v is the *total* gain from the source to the load, N_a represents that noise added but the DUT, $N_{RS} = 4kTR_S$ is the noise power generated by the source resistance in a 1Hz bandwidth, and $N_o = N_{RS}A_v^2 + N_a$ is the total noise at the output.

The noise terms in (2.7) can be expressed using power spectral densities that can be derived directly from the circuit using superposition (with correlation where necessary) to determine the weight of the contributors of noise in the DUT.

Noise figure is simply the noise factor in dB:

$$NF = 10 \log(F) \text{ (dB)} \quad (2.8)$$

Also, using Friis' equation for noise, the total noise factor of cascaded two ports can be derived.

$$F_{tot} = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + \dots + \frac{(F_n - 1)}{G_1 G_2 \dots G_{(n-1)}} \quad (2.9)$$

where F and G are the noise factor and power gain, respectively, and the subscript denotes the stage in the cascade.

It can be seen that the first stage in a system dominates the total noise figure as long as it has a large enough power gain.

2.1.4 Compression

Compression is a measure of how an increase in input power affects the output signal through the generation of compressive third order harmonics.

If the first three harmonics are considered (with no memory/correlation),

$$y(t) = \alpha_1 A \cos(\omega t) + \alpha_2 A^2 \cos^2(\omega t) + \alpha_3 A^3 \cos^3(\omega t) \quad (2.10)$$

which yields a result at the fundamental expressed by

$$y(t)_{@ \omega} = \left(\alpha_1 A + \frac{3}{4} \alpha_3 A^3 \right) \cos(\omega t) \quad (2.11)$$

and if $\alpha_1 \alpha_3 < 0$, then the output will be compressed [9].

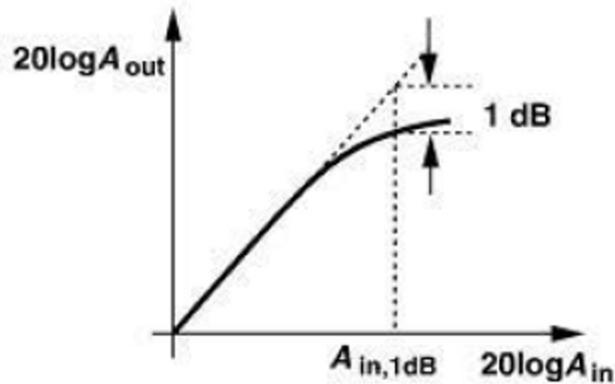


Figure 2.2: Typical 1-dB compression plot [9] [fair use]

Typically the 1-dB compression point is measured as a means to characterize the linearity of the device and represents an input/output power that can affect information signals. However, power amplifiers tend to measure 3-dB or higher compression for power efficiency reasons.

For LNAs, the input power is usually well below the input P1dB point, but the point can be used as a general point to not exceed. In fact, the P1dB point is of more concern when regarding a blocker. A large blocker has the ability to compress the desired signal significantly regardless of compressed the signal is through its own harmonics [9]. For this reason, the total input signal power needs to be at least several dB below the P1dB power level.

2.1.5 IP3 and IP2

Intermodulation products of the third-order (IP3) and second-order (IP2) are additional tests of linearity. Intermodulation is the nonlinearities generated by two close tones that mix in an amplifier and yield numerous undesired tones that fall in other bands. The IP3 and IP2 power levels are defined as the point where the first-order output power is equal to the third-order and second-order output power, respectively.

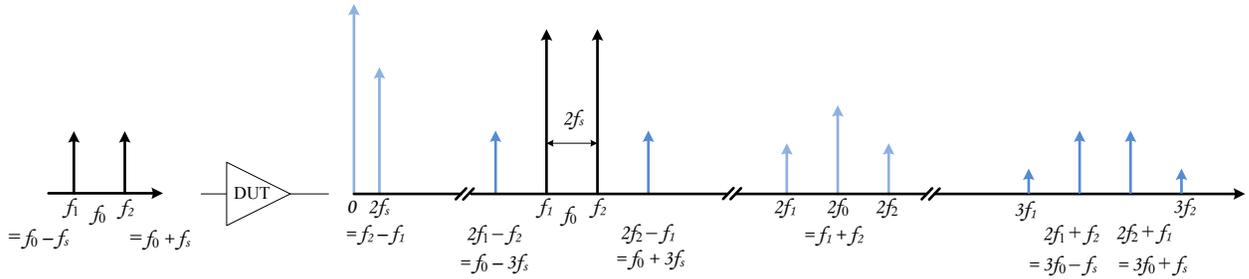


Figure 2.3: Two-tone test: first-, second-, and third-order products.

Again, the first three harmonics are considered but this time with two tones input,

$$y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 \quad (2.12)$$

where

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$$

which yields mixing product tones at all of the frequencies shown in Figure 2.3. The order of the generated tone can be quickly tested by summing the coefficients of the frequencies. That is, given a frequency combination $mf_1 + nf_2$, then $order = |m| + |n|$.

The importance of this is that two “interferers” are large enough and satisfy a mixing product that generates a tone on the desired signal, and then the signal is corrupted. This is particularly important for wireless communications, but is also important in wideband operations as multiple signals will be sent close to each other at detectable power levels. For instance, this work is a wideband LNA that will have two sets of ten channels equally spaced and around the same power level all present at the input of the LNA which will be mixed and present at the output before any filtering is done. This requires a high IP3 to ensure detectable signals. High IP2 levels ensure that leakage of second order terms that reach the mixer do not feedback and affect the signal and also ensure that there is not a large DC offset.

In order to test for IP3 and IP2, two tones are sent into the DUT and the output levels are measured. Since the third-order tone grows 3dB for every 1dB of the first-order tone (due to the cubic relation) and the second-order grows 2dB for every 1dB of the first-order tone, the points where the third- and second-order tones become equal to the first-order tone in output power can be mathematically determined as shown in Figure 2.4 and the following equations.

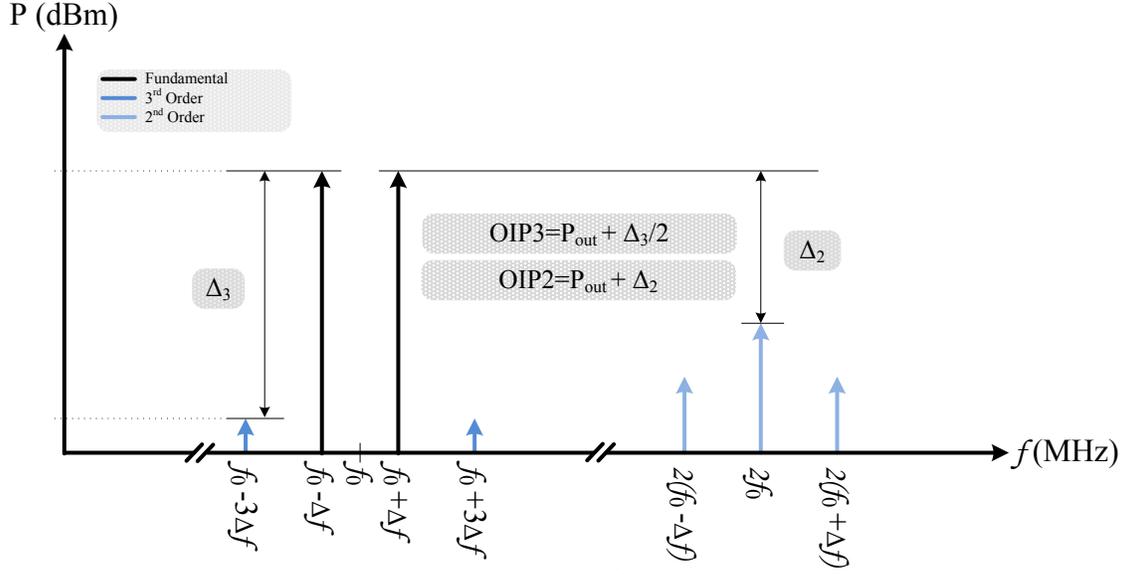


Figure 2.4: Calculation of OIP2 and OIP3.

$$OIP3 = \frac{1}{2} (3P_{out}^{f_0 \pm \Delta f} - P_{out,3rd}^{f_0 \pm 3\Delta f}) = P_{out}^{f_0 \pm \Delta f} + \frac{1}{2} (\Delta_3) \quad (2.13)$$

$$OIP2 = (2P_{out}^{f_0 \pm \Delta f} - P_{out,3rd}^{2f_0}) = P_{out}^{f_0 \pm \Delta f} + \Delta_2 \quad (2.14)$$

Linearity tends to be limited by later stages as shown with the following equations (referenced to the input and neglecting contributions far from the center frequency) [9]:

$$\frac{1}{IIP3_{tot}^2} \approx \frac{1}{IIP3_1^2} + \frac{A_1^2}{IIP3_2^2} + \frac{A_1^2 A_2^2}{IIP3_3^2} + \frac{A_1^2 A_2^2 A_3^2}{IIP3_4^2} + \dots + \frac{A_1^2 A_2^2 \dots A_{n-1}^2}{IIP3_n^2} \quad (2.15)$$

$$\frac{1}{IIP2_{tot}} \approx \frac{1}{IIP2_1} + \frac{A_1}{IIP2_2} + \frac{A_1 A_2}{IIP2_3} + \frac{A_1 A_2 A_3}{IIP2_4} + \dots + \frac{A_1 A_2 \dots A_{n-1}}{IIP2_n} \quad (2.16)$$

2.1.6 Stability

Stability is an important factor in any design. If the system is not stable, then undesired oscillations occur which require additional power and can corrupt a signal or even cause failure of operation. For this reason, it is important to test for stability and reduce the risks of instability.

Although being “conditionally stable” does not mean that a circuit will oscillate, the risk that a pole or zero in a real “linear, time-invariant” system satisfies the condition for

oscillation is too great to ignore. Since the transfer function greatly depends on the inputs and are also functions of the circuit parameters, the infinite possibilities make removing any possibility of instability ideal. For this reason, unconditional stability is often sought over as large of a bandwidth as possible.

Unconditional stability means that under no loading conditions will the two-port ever present a negative impedance (which is a necessary condition for sustained or growing oscillation in a real circuit – counteracts natural damping). Therefore, if any transmission loops satisfy the multiple of 360° phase requirement of the Barkhausen criterion, the loop gain cannot meet or exceed unity. This results in a damping effect for any oscillations that may try to sprout.

2.1.6.1 Stability Test

Although numerous stabilization tests exist (Mason, Stern, Linvill, Llewellyn, Rollett, Nyquist, etc.), the use of a single, straightforward test for unconditional stability is often enough.

The μ stability parameter is a test that can determine unconditional stability using a single equation without any need for auxiliary conditions and was originally derived for a two-port using s-parameters [10]. This parameter determines the minimum distance to the unstable region from the center of the unit smith chart (negative μ values represent that the unstable region encloses the center of the smith chart). The load μ is expressed in (2.17) (mapped via the Γ_L plane) and the source μ (tabulated as μ') is similarly formed (mapped via the Γ_S plane).

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21} S_{12}|} \quad (2.17)$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta| + |S_{21} S_{12}|} \quad (2.18)$$

where $\Delta = S_{11} S_{22} - S_{21} S_{12}$.

In order for the two-port to be unconditionally stable, either of the following conditions must be met or the circuit is conditionally stable (i.e. potentially unstable) [10]:

$$\mu > 1 \text{ or } \mu' > 1$$

If the circuit is conditionally stable, then more revealing stability analysis should be sought. The use of stability circuits can do just this and are developed from s-parameters of a two port; the equations for these are not covered here.

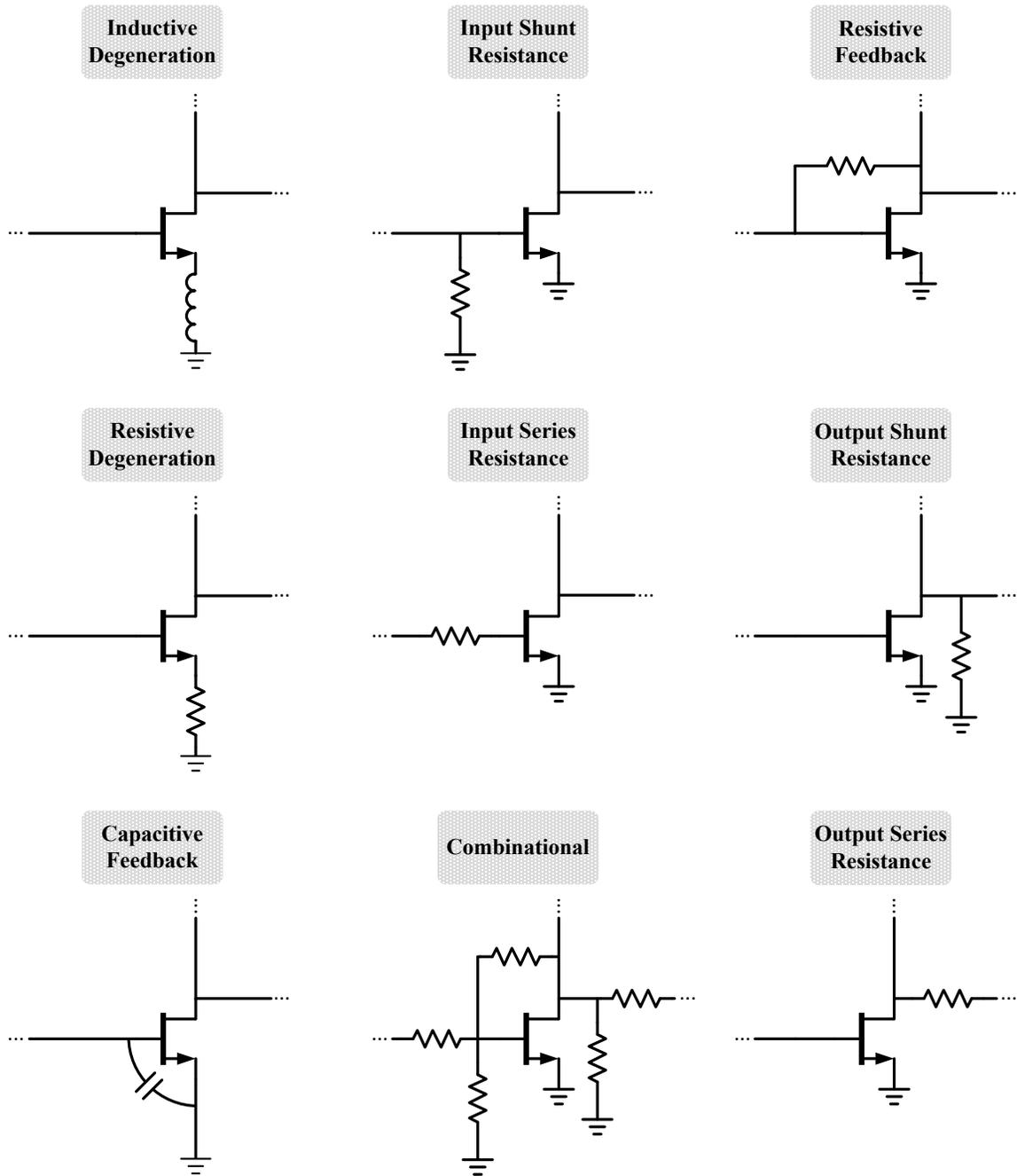


Figure 2.5: Some possible stabilization techniques.

2.1.6.2 Stability Techniques

Some basic stability techniques are covered here. The general idea of stabilization involves some form of negative feedback. This can be accomplished by means of sensed feedback (i.e. output fed back to input) or by means of loss (i.e. dampening growing signals in the direct path by means of canceling out negative resistance or conductance). Figure 2.5 shows several ways that stabilization can be implemented.

Some big drawbacks of resistive compensation are the power that will be lost and the noise that it will generate. Using frequency dependent stabilization can help in removing the negative effects of the resistance in the desired band, but if the stabilization is needed in-band, the drawbacks of each technique should be analyzed. The use of reactive components is usually attractive since they allow for stabilization with minimal noise contributions and can also aid in matching. Also, gain and stability are typically tradeoffs, so making the circuit extremely stable will often result in very poor performance.

2.1.7 Microstrip

Microstrip is a microwave transmission technique that allows for controlled characteristic impedances of traveling waves. This aspect allows for easy manipulation of matching networks for power transmission without the need for lumped elements. Additionally, microstrip is easy to build and connect devices at an affordable cost. Figure 2.6 shows two views of a microstrip line.

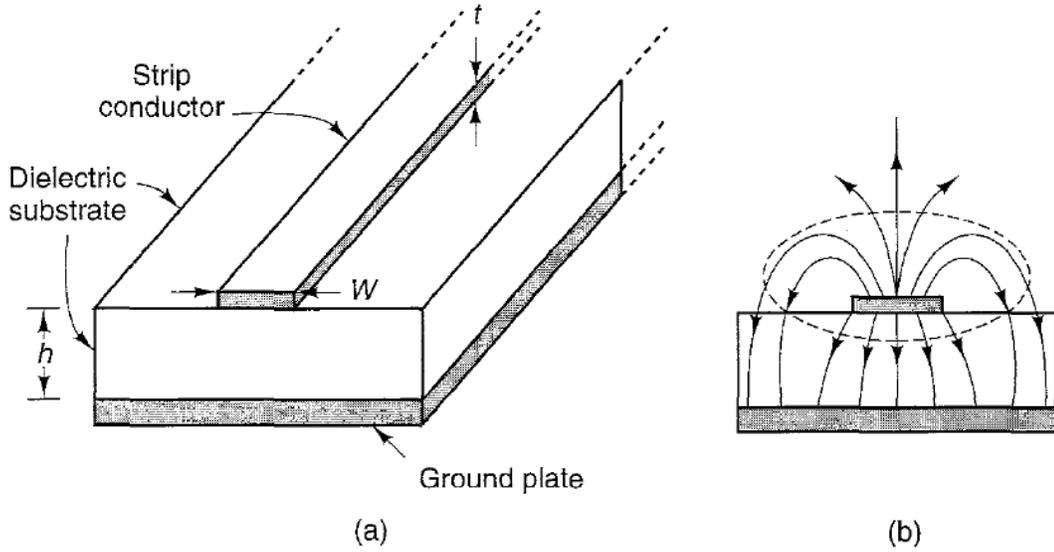


Figure 2.6: Microstrip geometry and field configuration. In (b), the solid lines represent electric field lines and the dashed line represents a magnetic field line. [11] [fair use]

The characteristic impedance, Z_0 , and effective relative dielectric constant, ϵ_{ff} , have been found to be approximated by (2.19) – (2.22).

For $W/h \leq 1$

$$Z_0 = \frac{60}{\sqrt{\epsilon_{ff}}} \ln \left(8 \frac{h}{W} + 0.25 \frac{W}{h} \right) \quad (2.19)$$

$$\epsilon_{ff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[\left(1 + 12 \frac{h}{W} \right)^{-1/2} + 0.04 \left(1 - \frac{W}{h} \right)^2 \right] \quad (2.20)$$

For $W/h \geq 1$

$$Z_0 = \frac{120\pi / \sqrt{\epsilon_{ff}}}{W/h + 1.393 + 0.667 \ln(W/h + 1.444)} \quad (2.21)$$

$$\epsilon_{ff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + 12 \frac{h}{W} \right)^{-1/2} \quad (2.22)$$

assuming that $t/h < 0.005$. If this is not the case, then the W/h in the above equations can be adjusted by replacing them with an effective value, W_{eff}/h .

For $W/h \geq 1/2\pi$

$$\frac{W_{eff}}{h} = \frac{W}{h} + \frac{t}{\pi h} \left(1 + \ln \frac{2h}{t} \right) \quad (2.23)$$

For $W/h \leq 1/2\pi$

$$\frac{W_{eff}}{h} = \frac{W}{h} + \frac{t}{\pi h} \left(1 + \ln \frac{4\pi W}{t} \right) \quad (2.24)$$

where $t < h$ and $t < W/2$.

The effective wavelength can be generalized as

$$\lambda_{eff} = \frac{\lambda_0}{\sqrt{\epsilon_{eff}}} = \frac{c}{f\sqrt{\epsilon_{eff}}} \quad (2.25)$$

where λ_0 is the free space wavelength.

Other factors to consider are losses and dispersion effects, which are outside the scope of this work. Since complex losses tend to be more present in the GHz range, the importance of these factors do not need to be heavily investigated operating at much lower frequencies. The datasheet of the material will generally be of more use than these equations, but it is important to see the effects on important parameters.

Most RF and microwave books do not discuss temperature effects of the board materials, though. It is apparent that with the use of copper metal, the metal sheets will expand and change the dimensions. The dielectric material used will determine what effects it will undergo with temperature and frequency; it trend to have to do with the polarization mechanism in the material – this trend may be shown in the datasheet. Also, the loss tangent would most likely increase due to thermal generation leading to excessive losses in stored energy and increased resistance to polarizing mechanisms. These effects are also beyond the scope of this work.

Once the change in properties of the microstrip can be estimated, reliable networks can be formed to aid in the transformation of impedances with low loss. The transmission line equation for input impedance of a lossless line is expressed in (2.26).

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta z)}{Z_0 + jZ_L \tan(\beta z)} \quad (2.26)$$

where β is the propagation constant (i.e. the change in phase with distance).

2.1.8 Matching Network

A matching network is a network that is inserted between the main two-port and the source and or load impedances in order to transform the impedance to obtain maximum power transfer, minimum noise figure, maximum power efficiency, and so on.

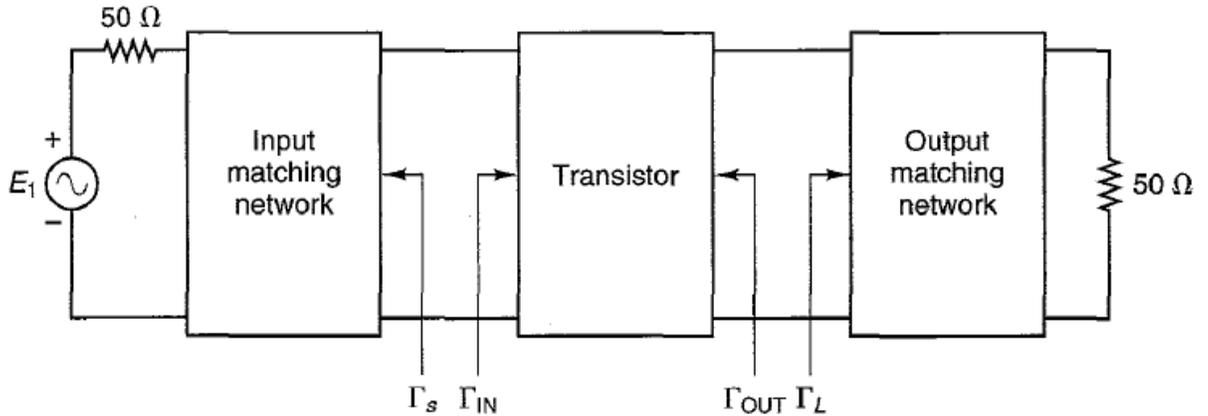


Figure 2.7: Block diagram including matching networks [11] [fair use]

Lumped elements and/or transmission lines can be used to achieve the transformation. Figure 2.8 shows an example of the transforming properties of transmission line as described by (2.26).

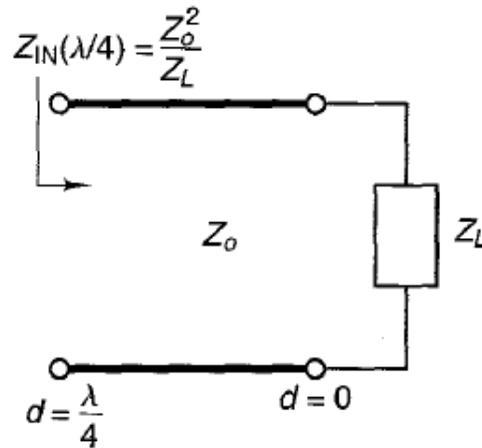


Figure 2.8: Example of impedance transforming effect of transmission line – quarter wave transformer [7] [fair use]

In most design, simultaneous conjugate matching is used. Since the embedded reflection coefficients of the two-port (Γ_{in} and Γ_{out}) depend on the load and source

impedances, a mathematically derived expression that ensures both the input and output transmit the maximum power to the two-port and load can be determined as follows [12].

$$\Gamma_S^* = \Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (2.27)$$

$$\Gamma_L^* = \Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (2.28)$$

Solving for the necessary source and load coefficients (considering an unconditionally stable two-port) yields the following equations:

$$\Gamma_S = \Gamma_{MS} = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (2.29)$$

$$\Gamma_L = \Gamma_{ML} = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (2.30)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (2.31)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (2.32)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (2.33)$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad (2.34)$$

If matching for other reasons than maximum power transfer at both ports, then typically the load condition needed for a specific performance is set before the other port is conjugate matched. If the optimum value depends on the other port loading, though, then a similar process as above can be performed through simple substitution in order to simultaneously achieve both conditions.

The other thing to consider in matching is the quality factor (Q) of the network. If band shaping is desired, then a high Q network can do this. However, microstrip tends to have moderate Q's at lower frequencies and also require larger lengths to implement. Fortunately, for wideband matching, a lower network Q is desired. The use of a smith

chart can aid in simplistic matching network design (the smith chart cannot be covered quickly enough to include). More advanced matching techniques are not covered in depth here, but can be seen in nearly any RF or microwave book.

2.2 LNA Topologies

A few topologies that are typically implemented for LNAs are briefly described below. Additional techniques have been applied to these circuits to aid in performance enhancement, but they are not covered in detail here.

2.2.1 Common Source Stage with Inductive Load

This topology consists of a normal common source configuration with a simple use of an inductor as the load. This allows for a large gain at resonance with the added benefit of a small voltage drop over the inductor (allowing for more headroom). The input is also not difficult to match which is attractive in front-end design. However, the internal feedback capacitance (gate-drain capacitance) can lead to a negative input impedance that typical ends up in the tens of GHz range.

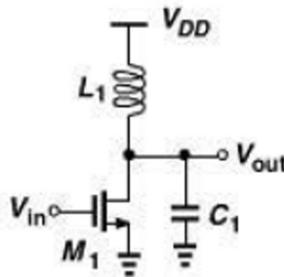


Figure 2.9: Common source with inductive load [13] [fair use]

In order to solve the potential instability of the negative input impedance due to C_F , an inductor can be used to cancel it. However, due to the large size needed for the inductor, this topology is not very practical.

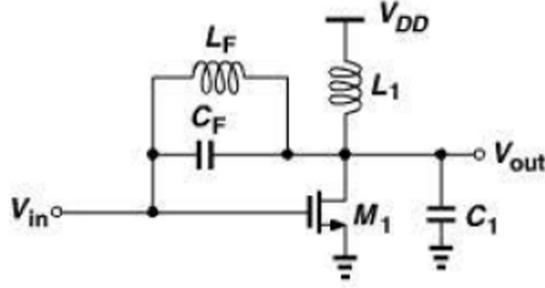


Figure 2.10: Common source with inductive load and neutralization of internal feedback capacitance [13] [fair use]

The configuration has no noise contributions other than the transistor itself, but stabilization could render that point insignificant.

2.2.2 Common Source Stage with Resistive Feedback

This topology incorporates a feedback resistor on a CS stage. It is only practical when the frequency of operation is much less than the unity frequency (f_T) of the transistor.

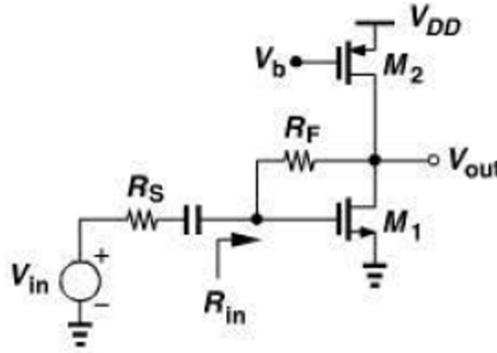


Figure 2.11: Common source with resistive feedback [13] [fair use]

In this topology, the input is fairly simple to match as the input impedance will be around $1/g_m$ for a large output resistance. Additionally, the noise of the feedback resistor is present directly at the output (i.e. it's not amplified).

For this LNA, the gain and NF are as follows ($g'_m = g_{m1} + g_{m2}$):

$$A_{v,tot} = \frac{(1 - g_m R_F)}{R_F + R_S + (1 + g_m R_S) R_X} R_X \quad (2.35)$$

$$NF \approx 1 + \frac{R_F}{R_S} \left(\frac{1 + g'_m R_S}{1 - g'_m R_F} \right)^2 + \frac{\gamma g'_m}{R_S} \left(\frac{R_S + R_F}{1 - g_m R_F} \right)^2 + \frac{1}{R_S R_L} \left(\frac{R_S + R_F}{1 - g_m R_F} \right)^2 \quad (2.36)$$

where

$$Z_{in} = \frac{R_F + R_X}{1 + g_m R_X} \quad (2.37)$$

$$Z_{out} = \frac{R_F + R_S}{1 + g_m R_S} \parallel r_o \parallel R_D \quad (2.38)$$

$$R_X = r_o \parallel R_D \parallel R_L \quad (2.39)$$

(note that if the LNA is matched on one side or simultaneously conjugate matched, then R_S and R_L should be replaced with the impedance seen at the source and load of the two-port).

If the input is matched by $R_S = 1/g_m$ (assuming that R_X is large):

$$A_v \approx 1 - \frac{R_F}{R_S} \quad (2.40)$$

$$NF \approx 1 + \frac{4R_S}{R_F} + \gamma + \gamma g_{m2} R_S \quad (2.41)$$

It can be seen that for short channel devices (which typically have $\gamma > 2/3$), the NF of a matched LNA tends to easily exceed 3dB. However, note that a finite output resistance can actually improve the NF in noisy transistors at the cost of a larger input impedance and lower gain.

2.2.3 Common Gate Stage

The common gate topology is an attractive choice for wide band operation. It also exhibits a low input impedance making it attractive for input matching and has a relatively package-independent input resistance [13].

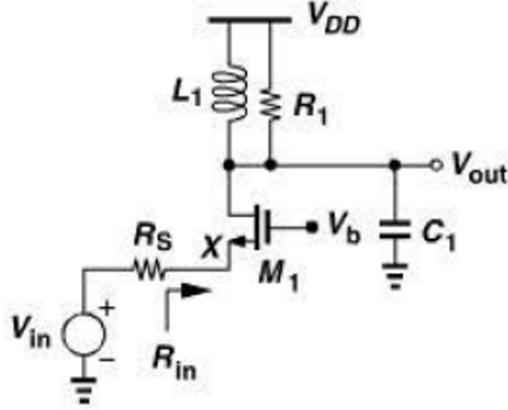


Figure 2.12: Common gate [13] [fair use]

For this LNA, the gain and NF are as follows:

$$A_v = \frac{g_m R_1}{1 + g_m R_S} \quad (2.42)$$

$$NF \approx 1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R_1} \left(1 + \frac{1}{g_m R_S}\right)^2 \quad (2.43)$$

and if the input is matched by $R_S = 1/g_m$:

$$A_v = \frac{g_m R_1}{2} \quad (2.44)$$

$$NF \approx 1 + \gamma + 4 \frac{R_S}{R_1} \quad (2.45)$$

This, again, has the possibility of exceeding 3dB in short channel devices. However, a small mismatch on the input using a higher g_m can help to reduce NF.

Also, if the output resistance is finite, the input resistance increases significantly. The use of a cascode transistor can help to reduce as it reduces the input impedance. The noise figure is still close to that seen above at low frequencies, but can become very large. Additionally, the headroom is reduced.

2.2.4 Cascode CS Stage with Inductive Degeneration

This topology uses an inductor on the source of a cascode CS stage as seen below.

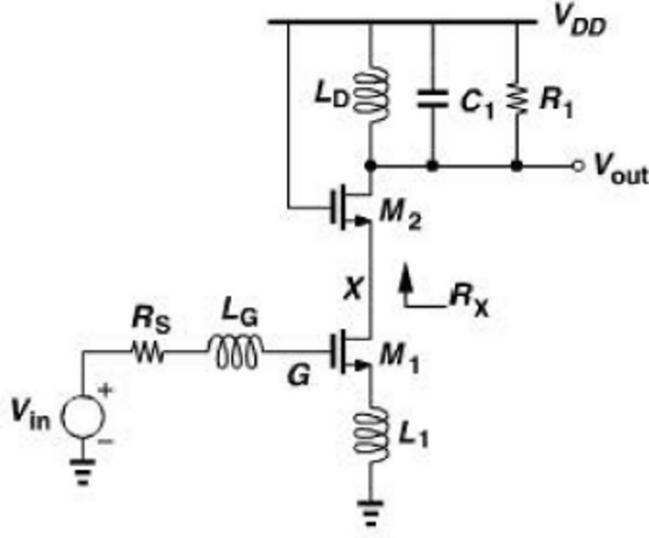


Figure 2.13: Cascode CS with inductive degeneration [13] [fair use]

By adding in the inductor, the input impedance can be easily matched since it generates a frequency-independent real part. This fact also is good for noise performance. Since no the degeneration is purely reactive, there is no noise added from a resistor. Degeneration also works to stabilize the device similar to a resistor.

For this LNA when as the selected resonance and if the input is matched using a derived relation $R_S = \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}} \right)^2 L_1 \omega_T$ with $\omega_T \approx \frac{g_m}{C_{GS,tot}}$ and ignoring the cascode noise:

$$A_v \approx -\frac{\omega_T R_1}{2\omega_0 R_S} \quad (2.46)$$

$$NF \approx 1 + g_m R_S \gamma \left(\frac{\omega_0}{\omega_T} \right)^2 + \frac{4R_S}{R_1} \left(\frac{\omega_0}{\omega_T} \right)^2 \quad (2.47)$$

This allows for much lower NF than the previous topologies with proper selection of component values and device properties.

2.2.5 Common Variants

There are some common variants of LNAs that help to improve the noise figure. Three of these topologies are shown in Figure 2.14.

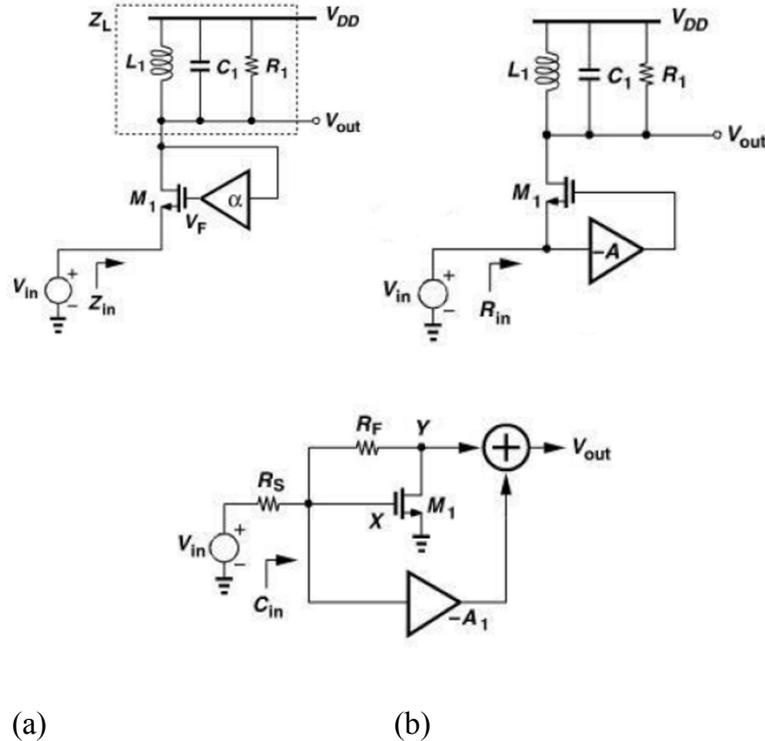


Figure 2.14: Some variants: (a) CG with feedback, (b) CG with feedforward, and (c) Noise cancelling LNAs [13] [fair use]

The above CG topologies work by using additional feeds to separate dependencies of transconductance on matching which allows for better noise design. Feedback helps boost the input impedance but reduces the gain. Feedforward boosts the transconductance (changing the input impedance). This allows for the NF to be reduced without restriction on the transconductance. The noise canceling uses phase shifting of a sampled noise node to help cancel out the noise at the output using an appropriate scaling factor. The additional amplifiers will add noise, but often it can be made to be less than what is removed.

2.3 Thermal Equations

As with all mechanical systems, electronic circuits must obey the laws of thermodynamics. This means that heat generated through power loss must flow through

the system. Fortunately, the concept of heat flow is directly analogous to that of current flow:

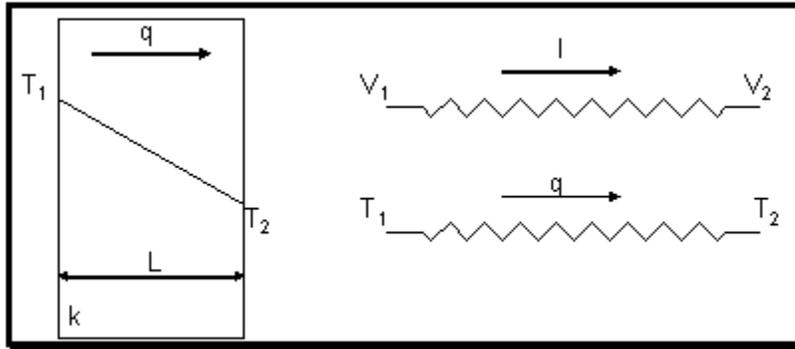


Figure 2.15: Electrical analogy of 1-D heat flow [14] [fair use]

As defined by Fourier’s law of heat conduction, heat flow, q , naturally occurs from high temperature to low temperature. The thermal resistance, θ (or R_θ), or thermal conductance, k , of heat is determined by the ability of a material to transfer heat without storing any energy.

Before determining the “thermal resistance”, it is important to understand the three modes of heat transfer:

Conduction: the transfer of heat *through* a material via energy transfer between colliding particles that make up the material. This transfer is influenced by the quantum mechanics and physics of a material [15].

Convection: the transfer of heat by means of bulk movement. That is, when a local area is heated, the physical properties (usually density) cause the bulk movement of that material to a different location allowing for heat transfer through space. It is considered *forced* convection if external means of moving the heat are used; i.e. a fan, and *natural* or *free* convection if not [15].

Radiation: the transfer of heat through electromagnetic waves which often depends on wavelength. The energy in a wave can be transferred through, absorbed by, or reflected from a material based on its properties. These wave always travel in straight paths and most gases tend to be transparent to a lot of forms of radiation [15].

Table 2.1 shows the 1-D heat flow equations for uniform surface, homogenous materials.

Table 2.1: Heat flow equations [15]

Mode	Equation	Descriptions
Conduction	$q_x = -kA \frac{dT}{dx} = -kA \frac{\Delta T}{\Delta x} \left[\frac{W}{m^2} \right]$	k : thermal conductance A : area perpendicular to heat flow
Convection	$q_c = \bar{h}_c A (T_w - T_\infty) [W]$	\bar{h}_c : film conductance T_w : temperature at surface
Radiation	$q_r = \sigma A_1 F_{1-2} \varepsilon_1 (T_1^4 - T_2^4) [W]$	σ : Stefan-Boltzmann constant $[W/m^2 \cdot K^4]$ A_1 : heat emitting surface area F_{1-2} : view factor; how surface 2 is viewed by surface 1 ε_1 : emissivity of surface 1

The nice thing about an assumed linear flow of heat is that a thermal circuit can be built for 1-D heat flow. It can be seen that radiation does not lend itself to a linear relation to temperature, but it can still be transformed into a linear resistance, however only at a single given temperature difference. Materials in series and materials in parallel of the heat flow path combine just as resistances do in a current path. The only thing is to manipulate the equations to form the V=IR format.

Table 2.2: Thermal resistance equations [16]

Mode	Arranged Thermal Equation	Thermal Resistance
Conduction	$\Delta T = \frac{\Delta x}{kA} q_x$	$R_k = \frac{\Delta x}{kA} = \frac{L}{kA} \left[\frac{K}{W} \right]$
Convection	$\Delta T = \frac{1}{\bar{h}_c A} q_c$	$R_c = \frac{1}{\bar{h}_c A} \left[\frac{K}{W} \right]$
Radiation	$\Delta T' = \frac{\Delta T'}{\sigma A_1 F_{1-2} \varepsilon_1 (T_1^4 - T_2^4)} q_r$	$R'_{\theta r} = \frac{\Delta T'}{\sigma A_1 F_{1-2} \varepsilon_1 (T_1^4 - T_2^4)}$

When all of the coefficients are found through datasheets or measurement, then a simple thermal circuit can be built as below. Usually, thermal radiation is ignored even though it does usually contribute to a non-negligible amount of heat transfer. Since

radiation travels in waves regardless of temperature gradient, the effect cannot be easily determined. If the system will be enclosed in small areas, then ignoring this mode should not cause problems.

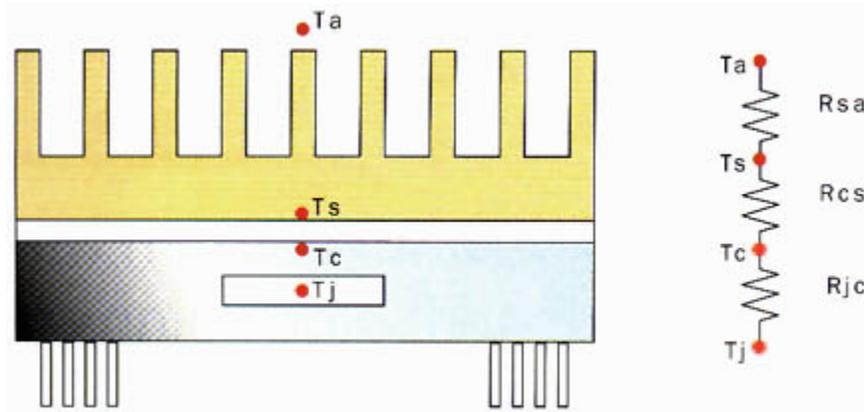


Figure 2.16: Thermal circuit of basic device on heatsink. [17] [fair use]

Of course, the thermal circuit may be more complicated than the above, but often the addition of a heatsink creates a low thermal resistance that is in parallel with much larger thermal resistances, so it dominates. The typical design equation considering a transistor in this case is expressed in (2.48).

$$P_D = \frac{T_J - T_A}{R_{\theta,tot}} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CS} + R_{\theta SA}} \quad (2.48)$$

where P_D is the *total* dissipated power (DC + RMS AC), T_J is the junction temperature of the transistor, T_A is the ambient temperature, and $R_{\theta JC}$, $R_{\theta CS}$, and $R_{\theta SA}$ are the thermal resistances for the junction-to-case, case-to-sink, and sink-to-ambient heat paths, respectively.

Typically, the thermal resistances are given in datasheets which leaves three variables. If any two of them are fixed based on some physical constraint (e.g. $T_J \leq T_{J,MAX}$) or a design constraint the requirements or limitations of can be determined. It is important to leave some room for error when calculating if the device is going to be pushed near its limits. Note that heat transfer is a very complicated science when dealing with real systems; however, a simple approximation of uniform, homogenous 1-dimensional heat flow can satisfy basic design needs.

2.4 High Temperature Device Materials – Applications

High temperature applications for electronics have always been present, but the ability of devices to work at these temperatures is still maturing. This section discusses some common materials used in analog circuits and presents several high temperature application uses of the materials (SiGe is not covered specifically since it is very similar to Si and tends to be geared more toward low power applications). The materials are compared at the end of the chapter.

2.4.1 Silicon (Si)

Silicon is the most matured and dominates the marketplace [18]. Despite its long history, the theoretical limitations of the material make it difficult to push the temperature capabilities. Despite this, a number of works have been done using the better performing SOI CMOS that are capable of wide temperature application. Almost all of the works seen use a zero temperature coefficient bias point for transconductance.

A bandgap reference using a 1 μ m FD SOI CMOS is designed in [19]. It is capable of achieving operation from 25°C to 300°C with a maximum bandgap voltage temperature coefficient of 200ppm/°C and <100ppm/°C on a 3V output voltage.

Another paper from the same group summarizes four high temperature applications using the same FD SOI CMOS [20]. In addition to the bandgap reference they have designed an instrumentation amplifier that can maintain a high gain up to 250°C and only experiencing a small degradation when taken to 300°C. Also, they have designed single-ended MOSFET-C filters that can maintain the same frequency response from 25°C to 300°C with automatic tuning. They also show a Σ - Δ ADC that can maintain 9 bits of resolution over the entire temperature range up to 300°C. Although this work is relatively old, the results are still valid.

2.4.2 Silicon Carbide (SiC)

SiC is still a maturing technology, but it has the benefit over Si over high power density, higher breakdown voltage, and better thermal performance. For these reasons, SiC has become very popular in power system designs. Since power dissipation and temperature are directly related, the material also lends itself to high temperature design, as well. The only drawback is that the frequency limitations of the materials are not

attractive for most RF and microwave operation (see Figure 2.17). It should be noted that several structures (i.e. polymorphs) exist in SiC (e.g. 3C-SiC, 4H-SiC, and 6H-SiC) which does change the properties slightly.

A family of CMOS analog and mixed signal circuits in SiC have been developed that have been tested and work up to 300°C [21]. This work presents PTAT and CTAT current reference, a Schmitt trigger, a two-stage OTA, and a folded cascode OTA all capable of very good performance (the OTAs have unity gain frequencies between 1-7 MHz). The work also mentions that several digital circuits created in the process (ring oscillator, Boolean shift register, and 4-bit asynchronous counter) have been shown to operate up 350°C in packaged form.

Another work [22] uses Cree's 4H-SiC lateral enhancement SiC technology to demonstrate a gate driver capable of working up to 400°C and 500kHz.

Also using a Cree wafer [23] developed a capacitive sensing transimpedance amplifier on P-type, Al-doped 6H-SiC and packaged in ceramic cases with gold bond wires which is capable of working up to 450°C and bandwidth >0.17MHz. The variation is very small and agreed very well with expected results.

It can be seen that SiC is very capable of high temperature applications, but the frequency limitations make it undesirable for RF and microwave sectors.

2.4.3 Gallium Arsenide (GaAs)

GaAs is the second leading technology being a popular choice for RF technology not long after the invention of the transistor, but it is still far from the widespread use of Si. It is an attractive option for high frequency operation, but it still doesn't compare to the high voltage and temperature capabilities of GaN (which can also reach similar high frequencies).

GaAs has already been used in high temperature applications for several decades. Discussed in [24], hall effect sensors that work up 300°C existed in the early 1990s and MMIC components for a X-band (8.0 – 12.0GHz) FMCW radar system for system operation temperatures up to 250°C have been developed. A number of RF and microwave circuits have been developed that work up to 300°C and some can even go up to 350°C. Shown in the paper is a MMIC, X-band mixer that works up to 300°C and only degrades <10dB over the entire temperature range using maximum conversion gain

biasing control. The paper mentions that design using high temperature GaAs have been tested from 400°C to 550°C.

GaAs is a very good candidate for high frequency, high temperature applications, but is still outperformed by the new GaN devices which can handle higher temperatures and higher power densities. Currently, GaAs is cheaper, but the rise of GaN is quickly closing the gap.

2.4.4 Gallium Nitride (GaN)

GaN is still a young technology with limitations in fabrication. However, the performance capabilities make an extremely attractive choice for high power and high temperature RF and microwave applications. It has become increasingly popular in the last decade as fabrication and packaging techniques improves and the theoretical limits of the device are quickly realized.

A lot of work has been done recently in developing GaN devices for high temperature operation (200°C – 600°C+) [25-29]. These works have investigated ways to produce GaN devices that can work at extreme temperatures for applications in the fields listed earlier. Unfortunately, the commercial availability of these devices has not fully been realized as of yet.

Some examples of high temperature GaN include a class-E PA that operates at 150°C with an output power of >30dBm and drain efficiency up to 75% [30], a zero-bias mixer that operates in the 2.4 – 2.5GHz range from room temperature up to 250°C with performance comparable to other mixers designed for room temperature, and a 58.58MHz lamb-wave oscillator [31] that operates up to 250°C with only a few dB degradation from room temperature.

2.4.5 Indium Phosphide (InP)

Although InP shows great performance when it comes to gain, noise figure, and high frequency operation, it is difficult to grow making it a slowly maturing technology [18]. Investigation into high temperature uses of this material turned up very little. All of the high temperature research found dealt with life tests or degradation at higher temperatures (which were often <100°C).

The life test on a K-band balanced MMIC amplifier using a 0.1µm InP HEMT shows that this device would not be very practical for long term use in applications requiring a

channel temperature greater than 200°C which would be approximately an ambient temperature <190°C [32]. This seems plausible given the values in Table 2.3. Perhaps with more maturing, the devices can reliably reach a higher temperature that makes it a practical option in high temperature electronics. Currently, GaAs is a better option for the same general performance [32].

2.4.6 Summary

The table below summarizes some important properties of typical substrate materials used in amplifiers.

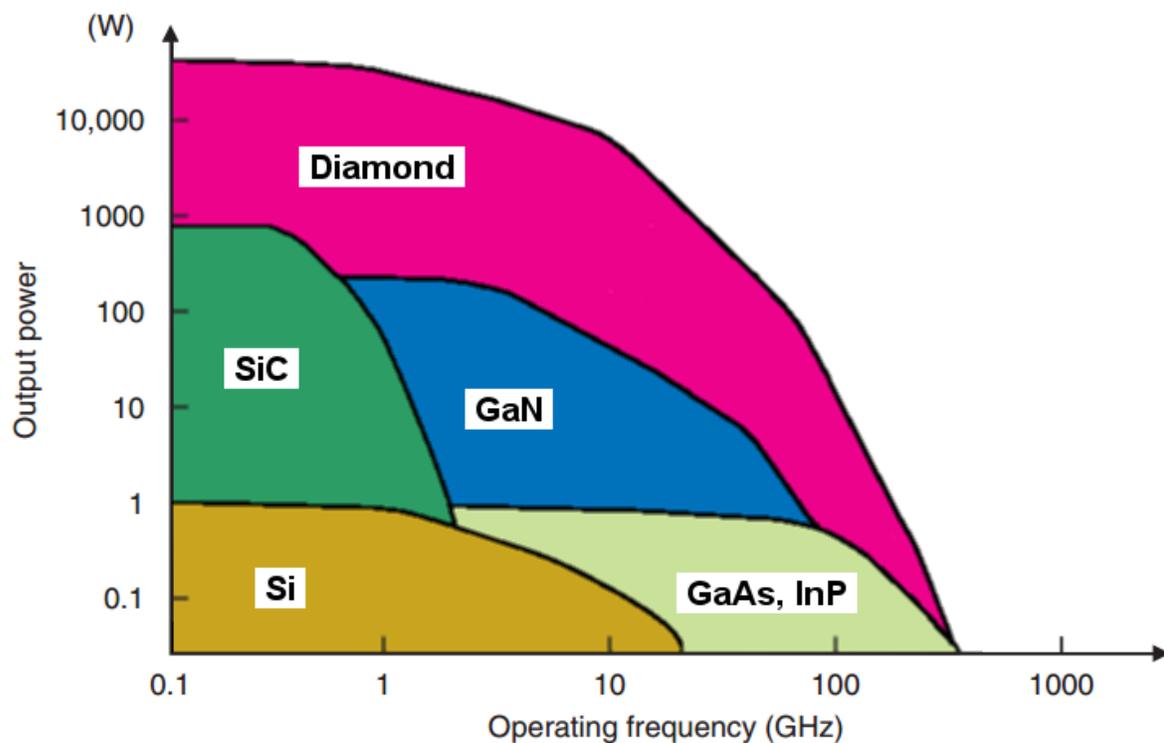


Figure 2.17: Frequency and power limits of some semiconductor technologies. [33] [fair use]

Something to note is that diamond theoretically outperforms all current wide bandgap materials (with over ten times better thermal performance and better power handling), but fabrication is still too difficult for commercial production.

Table 2.3: Comparison of Transistor/Monolithic Integrated Circuit Substrates^a [18] [fair use]

Property	Silicon	SiC	GaAs	InP	GaN
Semi-insulating	No	Yes	Yes	Yes	Yes
Resistivity ($\Omega \cdot \text{cm}$)	$10^3 - 10^5$	$> 10^{10}$	$10^7 - 10^9$	$\sim 10^7$	$\sim 10^{10}$
Dielectric Constant	11.7	9.7	12.9	14	8.9
Electron mobility ($\text{cm}^2/\text{V} \cdot \text{s}$)	1450	500	8500	4000	800
Saturation electrical velocity (cm/s)	9×10^6	2×10^7	1.3×10^7	1.9×10^7	2.3×10^7
Radiation hardness	Poor	Excellent	Very good	Good	Excellent
Density (g/cm^3)	2.3	3.1	5.3	4.8	6.1
Thermal conductivity ($\text{W/cm} \cdot ^\circ\text{C}$)	1.45	3.5	0.46	0.68	1.3
Operating temperature ($^\circ\text{C}$)	250	> 500	350	300	> 500
Energy gap (eV)	1.12	2.86	1.42	1.34	3.39
Breakdown field (kV/cm)	≈ 300	≥ 2000	400	500	≥ 5000

^aPure materials at room temperature

From Table 2.3, it can be seen that GaN and SiC are very good choices for high temperature operation and, although the frequency limits are dependent on device structure and size, GaN typically can exhibit frequencies in tens to hundreds of GHz.

The use of a GaN on SiC HEMT (as used in this work) exploits the great thermal properties, power/temperature capabilities, and overall robustness to high stress operation. GaN on SiC has a bandgap of 3.39eV, dielectric constant of 9.7, and thermal conductivity of 3.5W/(cm \cdot °C) [34]. Additional fabrication and packaging techniques can help improve the performance further. An example of this is the use of a field plate to extend the breakdown voltage by reducing the electric field at the junction (this is one technique used in the TriQuint GaN used here).

2.5 Temperature Effects – Device Physics

It is important to understand the basics of what will happen to a device as temperature increases so that proper selection and design can be done reliably. Although this section is specifically addressing semiconductors, thermal limitations of passive device are also

important and often require power derating. This section briefly covers some important temperature relations in semiconductors.

2.5.1 Bandgap Energy

The Varshni equation is one of the more popular relations for temperature effects on bandgap energy.

$$E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \quad (2.49)$$

where $E_g(0)$ is absolute zero band gap energy (in Kelvin) and α_E and β_E are material-specific constants [35].

It can be seen that at low temperatures, the bandgap is fairly constant, but as temperature increases, the energy rolls off and begin to decrease fairly linearly at high temperatures.

2.5.2 Carrier Concentration

Due to the large dependence on temperature for the intrinsic carrier concentration, the material becomes intrinsic at high temperatures [35, 36]:

$$n_i \propto T^{1.5} e^{\frac{-E_g(0)}{2kT}} \quad (2.50)$$

This leads to significant variations in the electrical behavior of the device and can lead to additional thermal variations and device failure.

2.5.3 Mobility

The mobility is also affected by temperature. However, the combination of mobility parameters are controlled by a dominant scattering effect which act in parallel

$$\frac{1}{\mu_{eff}(T, E_{eff})} = \frac{1}{\mu_{ph}(T, E_{eff})} + \frac{1}{\mu_{sr}(T, E_{eff})} + \frac{1}{\mu_{ch}(T, E_{eff})} + \frac{1}{\mu_{int}(T, E_{eff})} \quad (2.51)$$

The scattering effects are dependent on both the electric field and temperature. The above effects are due to phonon (μ_{ph}), surface roughness (μ_{sr}), Coulombic bulk charge (μ_{ch}), and Coulombic interface charge (μ_{int}) scattering [35].

At high temperatures, the phonon (i.e. lattice vibrations) scattering mechanism dominates with a temperature dependence of $T^{-3/2}$ *reducing* the overall mobility [35, 37]. The effective electric field also has a small inverse relation to temperature.

2.5.4 Threshold Voltage

The threshold equation is

$$V_{TH} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \quad (2.52)$$

$$V_{TH} = \left(\phi_{gs} - \frac{Q_{SS}}{C_{ox}}\right) + 2\phi_F + (C_{ox}\sqrt{2q\epsilon_r N_A})\sqrt{2\phi_F} \quad (2.53)$$

where

$$\phi_{gs} = \frac{kT}{q} \ln\left(\frac{N_A N_G}{n_i^2}\right) \quad (2.54)$$

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \quad (2.55)$$

and N_A and N_G are the substrate and gate doping concentrations, respectively, Q_{SS} is the surface charge density, C_{ox} is the oxide capacitance, V_{FB} is the flat band voltage, ϕ_{gs} is the gate-source contact potential, ϕ_F is the Fermi energy level, γ is the body effect parameter, and ϵ_r is the relative permittivity of the material [35].

Taking the derivative with respect to temperature gives

$$\frac{\partial V_{TH}}{\partial T} = \left(\frac{\partial \phi_{gs}}{\partial T}\right) + 2\frac{\partial \phi_F}{\partial T} + \frac{(C_{ox}\sqrt{2q\epsilon_r N_A})}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T} \quad (2.56)$$

with

$$\frac{\partial \phi_{gs}}{\partial T} = \frac{1}{T} \left[\phi_{gs} + \left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right) \right] \quad (2.57)$$

$$\frac{\partial \phi_F}{\partial T} = \frac{1}{T} \left[\phi_F - \frac{1}{2} \left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right) \right] \quad (2.58)$$

Using some typical values, the threshold voltage is seen to *decrease* with temperature [35, 38]. Factors such as doping concentration and oxide thickness change the rate of decrease.

2.5.5 Leakage Current

Leakage current is known to have an exponential relation to temperature. A typical approximation is for the subthreshold leakage current to double for every 10°C rise in temperature. There is also some gate leakage increase, but it is minor compared to subthreshold leakage,

$$I_{sub} = I_0 \left(e^{\frac{qV_{DS}}{kT}} - 1 \right) \propto \left(AT e^{-\frac{qE_G(0)}{2kT}} \right) \left(e^{\frac{qV_{DS}}{kT}} - 1 \right) \quad (2.59)$$

where A is constant determined by the material type, size, and doping [35, 39].

2.5.6 Additional Effects and Drain Current

Some other effects to note are that an increase in temperature tends to reduce the saturation velocity and increase the interconnect resistance [35]. Additionally, mechanical changes can cause expansion or compression of materials affecting dimensions, which can increase or decrease parasitics. Properties of the material will also change with temperature (e.g. permittivity) which will also influence the change in parasitics. The exact way it will go is dependent on the material, doping, and structure; however increased temperature tends to push materials away from the desired operation causing lower Q factors of conductors and a more conductive nature in insulators.

Taking all of the above when looking at the saturation region current

$$I_{D,sat} = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 - \lambda V_{DS}) \quad (2.60)$$

Since the dominating temperature effects are the *decreasing* mobility and *decreasing* threshold voltage, there exists a point where one dominates of the other causing either *decreasing* current with temperature or an *increasing* current with temperature, respectively. There may be some other slight changes in C_{ox} , the effective channel length L , and the channel length modulation, λ , but their effects are smaller.

Therefore, the device will have a point where is it thermally stable up to its physical limits, but another regime where thermal runaway is very likely.

2.6 Literature Survey

Few works on high temperature RF LNAs exist in the literature at the writing of this paper. [40], [41], and [42] highlight individual aspects of this work.

Regarding high temperature LNAs, [40] details a fully integrated 130-nm PD SOI CMOS 2.4GHz LNA with temperature compensation from 25°C to 200°C. This device uses a cascode common source with inductive degeneration topology and a zero temperature coefficient transconductance (ZTC_{gm}) bias point. The work is able to obtain 10dB gain and 3.4 – 5.7 dB NF at 2.4GHz over the temperature range. Due to the tuned nature of the design, performance significantly degraded away from the center frequency.

Additionally, [41] details a 700Hz low noise chopper amplifier for downhole operation up to 225°C. The technology is 1 μ m SOI CMOS, which is the current popular technology choice (disregarding gate length) for high temperature applications [3]. The output referred noise is as low as 25.6nV/ $\sqrt{\text{Hz}}$ (4.76dB NF with a 50 Ω source).

Regarding the technology, [42] shows the promising capability of GaN LNAs with a 0.2 μ m AlGaIn/GaN HEMT operating between 300MHz and 4GHz. The paper reports a gain of 18dB and noise figure around 1.5dB from 2 GHz – 4GHz (increasing to 4dB at 300MHz) with an output compression power level of 21dBm.

Unfortunately, no other application-relevant works could be found at the time of this writing in the literature. Most temperature related design in LNAs at present focus on cryogenic temperatures (typically for space) or discuss temperature compensation/improvement for ranges less than 85°C. The above works are compared in Table 2.4 against the work to be discussed as a quick comparison.

Table 2.4: Comparison of High Temperature LNAs

Design Parameter	This work	[40]	[41]	[42]
Temperature	230°C	200°C	225°C	25°C
Frequency	230.5 MHz – 285.5 MHz	2.0GHz – 2.6GHz	100Hz – 100kHz	0.3 GHz – 4.0 GHz
Gain	16.1dB	8.5dB	20dB	18dB
Noise Figure [†]	2.0dB – 2.9dB	5.2dB – 6.0dB	~4.76dB	1.5dB – 4.0dB
OP1dB	19.1dBm	-	-	21dBm
ORL	≥15dB	≥7dB	-	-
Technology	0.25μm GaN/SiC HEMT w/ FP	130-nm SOI CMOS	1μm SOI CMOS	0.2μm AlGaN/GaN HEMT

[†]With a 50Ω source impedance

Chapter 3

3 Proposed High Temperature LNA Design

Contents

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The LNA was designed with COTS components with an approach that exploited minimum observed noise figure and temperature insensitive gain. This was done at a low power level (for an RF power transistor) to ensure reliable operation while at ambient temperatures of 230°C. The design procedure harnessed traditional RF techniques to reduce complexity and validate a working design at a prototype level.

Chapter 3 discusses the design procedure in detail. First, the system specifications that facilitated the design choices are covered. Following the specifications is the selection of topology and the final schematic. The remaining sections elaborate on each

part of the design; how each device was chosen and employed as well as RF techniques to improve performance.

3.1 Specifications

This work was tasked for a downhole communications system with ten, 2MHz channels separated with 0.5MHz guard bands between receive (Rx) and transmit (Tx) channels and 10MHz between Rx and Tx bands (see Figure 3.1). The LNA was chosen to be wideband, covering the entire receive bandwidth with channel select filtering processed separately. The entire RF system incorporates an LNA, active mixer with voltage controlled oscillator (VCO), power amplifier (PA), and various microstrip filters. The achievable performance for each device heavily affects the requirement of other stages (predominately, the front end and back end tend to have the greatest influence if the mid-stages operate with reasonable specifications, as apparent in sections 2.1.3 and 2.1.5). Table 3.1 lists the given specifications. Note that the specified bandwidth does not account for the channel bandwidth on the band edges. Since the LNA is not band-tuned (with on-board filtering) the given specification will not degrade the signals on the band edges.

Table 3.1: Design specifications

Design Parameter	Specification
Frequency	$230.5\text{ MHz} - 285.5\text{ MHz}$
Gain	$\geq 12\text{ dB}$
Noise Figure	$\leq 2.0\text{ dB}$
OP1dB	$\geq 15\text{ dBm}$
OIP3	$\geq 25\text{ dBm}$
OIP2	$\geq 35\text{ dBm}$
Temperature	230°C

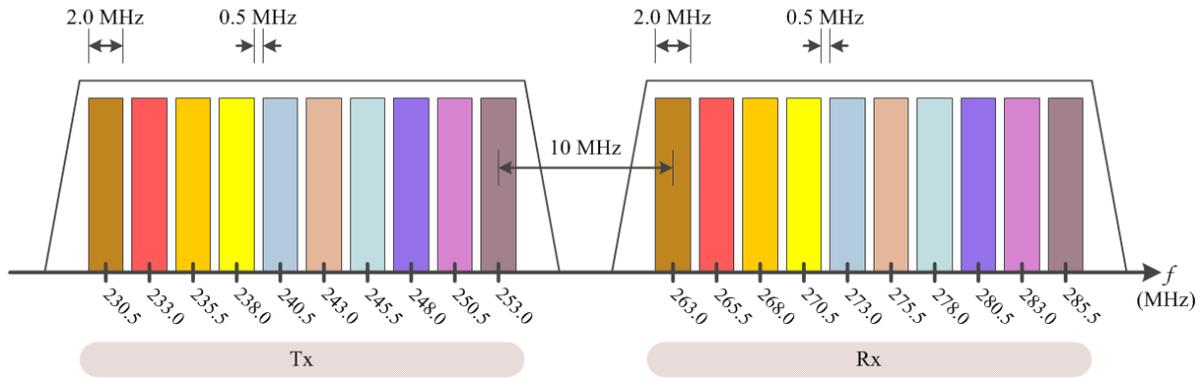


Figure 3.1: Frequency plan of the downhole system.

3.2 Selection of Topology

Section 2.2 discusses several relevant topologies for LNA design. The addition of a heat sink (which also serves as an extended ground plane) required the need for the source terminal on the HEMT to be grounded. This rules out CG topologies and the need for significant gain eliminates the CD topology. As a result, CS was the only feasible choice.

3.2.1 Common Source with Resistive Feedback

The topology selected for this design was CS with resistive feedback. The CS topology offers large gain and tends to be able to exploit better noise performance than CG configurations. Simulations showed that the CS configuration was capable of meeting the gain specification in-band (Figure 3.2); however, the device was not unconditionally stable and would require sacrifice of gain and noise to guarantee unconditional stability. With many biases producing greater than 6dB margin over the minimum specification, the sacrifice would very likely still allow the specifications to be met, especially since matching networks could improve the overall power gain.

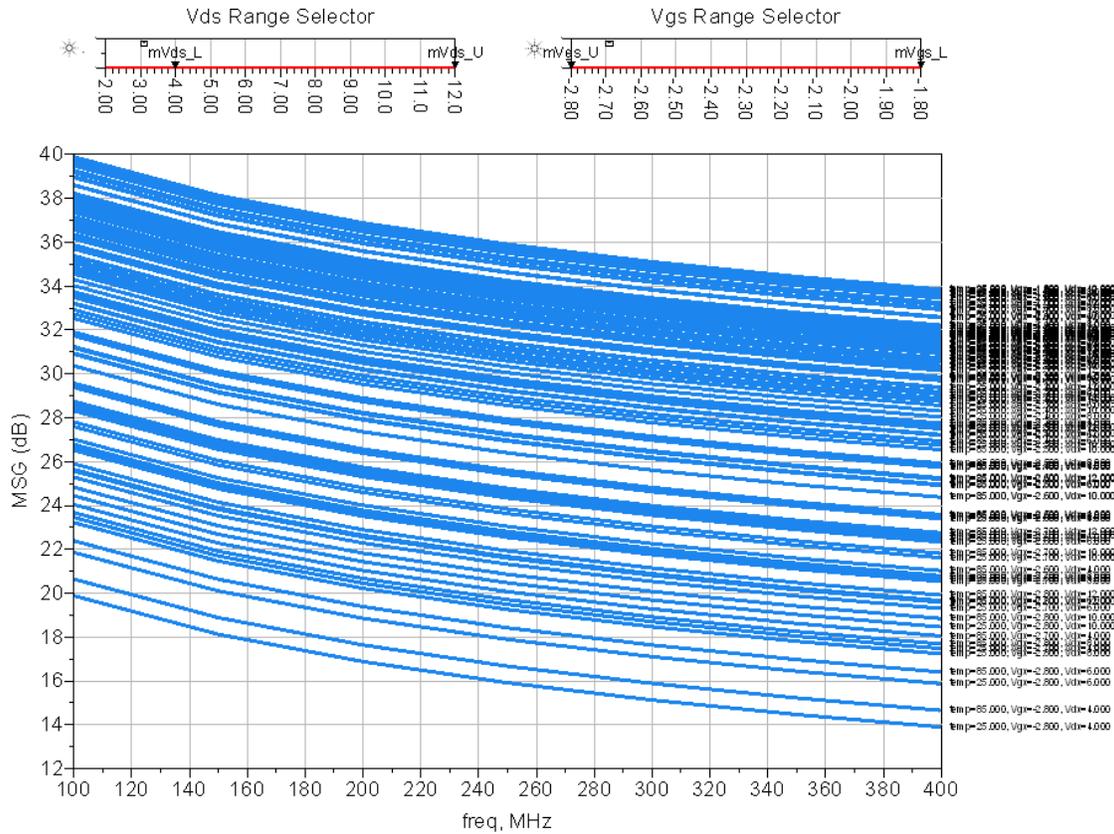


Figure 3.2: MSG simulation performance of the selected HEMT alone at 25°C (red) and 85°C (blue) from $V_{DS} = 4 - 12V$ and $V_{GS} = -2.8V - -1.8V$ (0528-Q3 model). [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

The noise figure of the device was unknown prior to selection, so the CS topology needed to incorporate stabilization and matching that degraded the noise figure as little as possible. The addition of the feedback resistor sacrificed the gain significantly, but would add minimal noise figure degradation. This aspect is discussed in more detail in section 3.10.

No other special compensation or feedback techniques to enhance the performance of the LNA in the frequency band were employed for sake of simplicity. As the device is operating in the VHF band, on-board bias tees and controlled impedance matching networks were employed. This is not part of the topology, but is an important part of the design in an RF circuit.

3.2.2 Troubles of Inductive Degeneration

Inductive degeneration is the most attractive topology for typical RF LNAs due to its ability to provide an easily matched input with little introduction of noise elements. Additionally, the inductor on the source terminal functions as a stabilizing device.

The inductor, however, only can be used to unconditionally stabilize a narrow band in the frequency range and can push the remaining frequencies closer to potential instability. If the stabilization is acquired in the desired band, then techniques can be employed to stabilize the device outside of this band using the additional poles and zeros of tuned elements to only introduce the loss needed outside of the frequency band so as not to introduce excess noise in the desired band.

This would require a significant increase in complexity of the board. In addition to this, the on-board source inductor would have to be both temperature insensitive over temperature and also be able to provide a low thermal resistance to heat flow (in the heat flow path from the package to the heat sink/ground). Measurements using inductive degeneration without out-of-band stabilization showed a large number of loads that incited oscillations at several GHz. Simulations also indicated that the board was extremely prone to oscillation around the same frequency.

It was desired to have a circuit unconditionally stable over as many frequencies as possible. Due to the complexity of tackling this task with inductive degeneration with unclear postulations as to the degradation in performance, the degeneration was dropped from use.

3.3 Final Schematic

With the selection of the topology, the schematic details were predominately defined by the requirements based on the transistor selected. Due to board size limitations which are restricted by the heat sink dimensions (see Figure 3.25 in section 3.8), the number of components was reduced to as few as possible to obtain the specifications. Figure 3.3 shows the complete schematic.

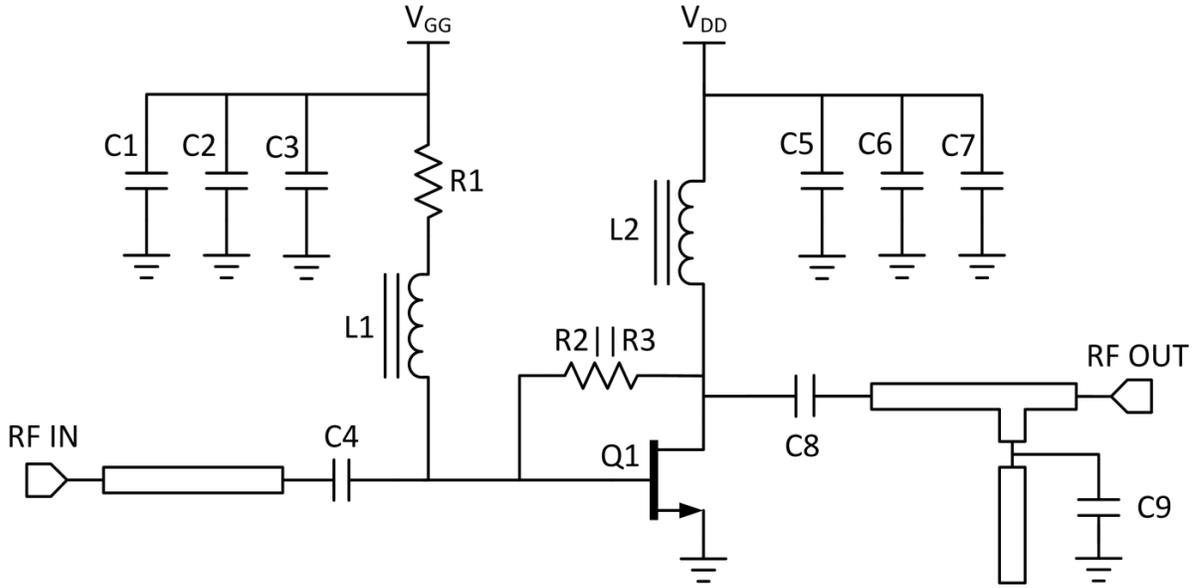


Figure 3.3: Schematic diagram of the proposed LNA.

The GaN HEMT (Q1) is configured in a simple CS configuration with resistive feedback, as discussed in section 3.2. The bias network consists of C1 – C8, L1, and L2. C1 – C3 and C5 – C7 function as bypass capacitors to filter out variations on the DC line due to RF leakage from the circuit and any noise from the supply. C4 and C8 are DC blocking capacitors and L1 and L2 are RF chokes (or DC feeds). Together, C4, C8 L1, and L2 function as an on-board bias tee (where the inductor passes low frequency signals, such as DC, and the capacitor passes high frequency signals; this is a three terminal device with a DC, RF, and DC+RF port). R1 serves as a low frequency stabilization shunt resistance. Additionally, R2 and R3 (which are two identical values in parallel due to power limitations of the device) serve as in-band stabilization; the reasons for this selection of stabilization are detailed in section 3.10. The feedback resistor pair also aids in temperature stability by helping to counteract the increasing drain current. The large lines at the input and output represent the microstrip matching networks. An additional capacitor C9 is placed in parallel with the open circuit stub on the output in order to reduce the length.

The above text offers a general description of the building blocks of the circuit; any relevant theory that requires more than a brief note is covered in chapter 2 but the design and selection related to this work is covered in detail in the following sections. The

component values are listed in Table 3.2 and the full bill of materials for the schematic above is provided in Table 3.7 which is in section 3.13.

Table 3.2: Schematic Values

Schematic Values			
Reference	Value	Manufacturer	Function
C1, C5	100 pF	IPDiA	Bypass
C2, C6	10 nF	IPDiA	Bypass
C3, C7	0.1 μ F	IPDiA	Bypass
C4, C8	1 μ F	IPDiA	DC Block
C9	4.7 pF	Presidio	Matching
R1	10 Ω	Vishay	Stability
R2, R3	1 k Ω	Vishay	Feedback/ Stability
L1, L2	1 μ H	Coilcraft	RF Choke
Q1	0528	TriQuint/Qorvo	Amplifier

3.4 Active Device Selection

The fundamental starting point in any design is selection of the technology (based on given/desired specifications). As mentioned in 2.4.6, GaN was selected as the device material based on a number of attractive properties.

Although GaN was fairly new to the commercial market when this research was initiated, there existed several companies with options of discrete GaN devices. Investigation into the GaN devices optimized for LNA design yielded unusable devices solely based on the thermal characteristics. Attention turned to power transistors, which would surely be a good solution to the thermal requirements; however, the noise performance was unclear.

3.4.1 Thermal Requirements

Since the target ambient temperature was 230°C, the maximum junction temperature of the device needed to be greater than this in order to support power dissipation. The only company offering COTS transistors that exceeded the 230°C temperature was TriQuint (now Qorvo). All of the power transistors available had $T_{JMAX} = 275^{\circ}C$. This

provided ample margin for power dissipation and reduced the need for thermal management.

Additionally, power devices are generally packaged to have very small thermal resistances allowing for greater power dissipation or, in this work, greater ambient temperatures.

3.4.2 Noise Performance of Power Devices

Since power devices are typically the last device in a system, the noise figure is not a concerning aspect. As a result, using a power device meant that there would be no information on the noise characterization of the device. However, due to the absolute necessity of the thermal capabilities, this aspect had to be sacrificed. Research on GaN (referenced in the introduction) implied that the noise figure of the device would be reasonable, at least. The noise tests done are discussed in detail in section 3.11.

3.4.3 Other Performance of Power Devices

In addition to the lack of noise characterization, power devices are typically optimized for large power consumption and high rail voltages. In order to reduce the thermal constraints, the operation would be as low power as possible based on certain design selections. It was unknown how accurate the models provided were at low bias conditions, far backed-off from the optimized biasing in the datasheet. Comparisons of different device models from Modelithics using simulation yielded that the best performance came from the lowest output power HEMT they offered in the PA models. They were compared based on the how the current and gain changed over temperature as well as the power requirement at select points. Plus, attention was directed at the tolerance of the device performance with small variations. The details of the selected device over temperature are reviewed in the next section.

3.4.4 Selected Device

The selected device was the T2G6000528-Q3 GaN RF Power Transistor (Figure 3.4). It is a 0.25 μm GaN on SiC Field Plate HEMT. The device datasheet [44] and GaN HEMT Model datasheet [43] list that it is optimized for 28V drain bias and is capable of an output saturation power level of $P_{3dB} = 10W$ at 3.3GHz.



Figure 3.4: 0.25 μ m GaN on SiC Field Plate HEMT – Model 0528-Q3 [44] [fair use]

The absolute maximum ratings and thermal characteristics are listed in Table 3.3. Due to the intended low power biasing, the primary concerns are the thermal limits. This package offers 12.4°C/W junction-to-case thermal resistance which will be low enough for operations below 1W regarding a $T_{JMAX} = 275^{\circ}C$ and $T_{AMBIENT} = 230^{\circ}C$. Despite that the other packages considered had lower package thermal resistances, they exhibited less ideal performance.

Table 3.3: T2G6000528-Q3 – Absolute maximum ratings and thermal reliability [44] [fair use]

Absolute Maximum Ratings	
Parameter	Value
Breakdown Voltage (BV_{DG})	100V (Min.)
Drain Gate Voltage (V_{DG})	40V
Gate Voltage Range (V_G)	-10 to 0V
Drain Current (I_D)	2.5A
Gate Current (I_G)	-2.5 to 7mA
Power Dissipation (P_D)	15W
RF Input Power, CW, $T = 25^{\circ}C$ (P_{IN})	34dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 seconds)	320°C
Storage Temperature	-40 to 150°C
Thermal Reliability	
Parameter	Value
Thermal Resistance (θ_{JC})	12.4°C/W

3.5 High Temperature Performance of Selected Device

The device was mounted to a test board, using bias tees to provide RF and DC. The complete testing procedure is covered in Chapter 4. The loss of the input and output lines were considered negligible for this test. The s-parameters were analyzed across temperature which is shown in Figure 3.5. Simulations showed that the gain increased several dB with temperature and the output impedance of the device experienced some shifting, but the input impedance and reverse isolation stayed relatively the same. This means that the input matching could stay relatively the same over temperature, but the output match would affect the gain based on where it was matched (in temperature). As the data only went to 85°C, the higher temperature trend was initially unknown.

Additionally, several tests were done to analyze the linearity of the device, but due to instability problems, a full temperature sweep was not possible. However, the data indicated that the OP1dB, OIP3, and OIP2 were exhibiting approximately 20dBm, 30dBm, and 40dBm around 230°C, respectively. It was assumed that the nonlinearity of the device would not be affected greatly in the completed design.

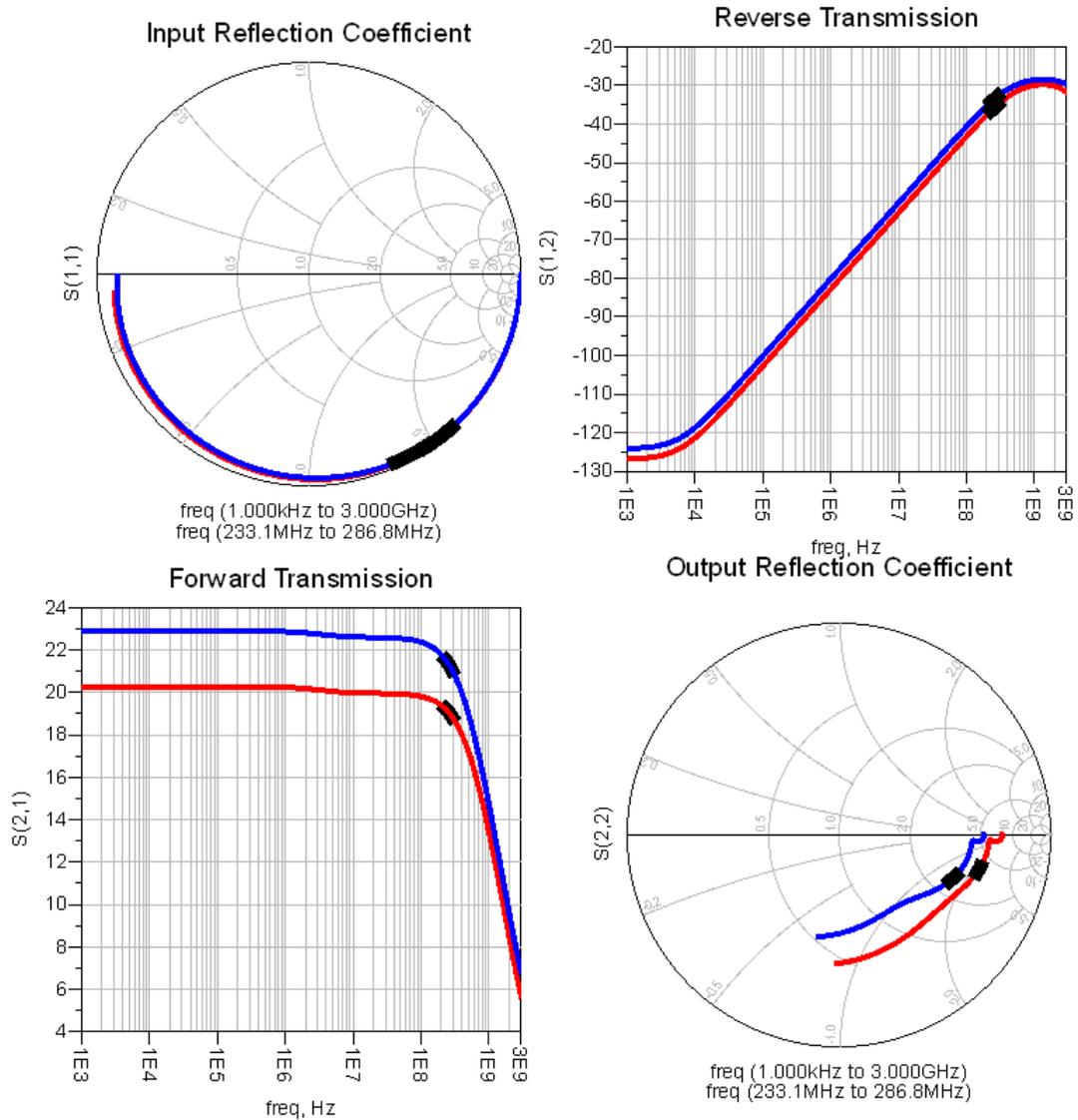


Figure 3.5: Device s-parameters at $T = 25^{\circ}\text{C}$ (red) / 85°C (blue) with the specified frequency band highlighted (black) – Model 0528-Q3 [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

3.6 Bias Point Selection

Prior to the selection of the bias point of ($V_{DD} = 4\text{V}$ and $I_D^{25^{\circ}\text{C}} = 28\text{mA}$ / $I_D^{230^{\circ}\text{C}} = 73\text{mA}$), several tests were done at drain biases of 4V, 8V, and 12V. However, before testing the biasing, the models provided by Modelithics [43] for Keysight’s Advanced Design System (ADS) were used to investigate power consumption and possible temperature insensitive points. The device I-V curves from the model are shown in

Figure 3.6 with four power levels marked for reference. It can be seen that low drain voltages are required in order not exceed the power limits set by the thermal analysis.

Additionally, the current increases with temperature (for low power biasing) which requires even lower power consumption at 25°C. As the model only shows up to 85°C, the actual current consumption was initially unknown. Limiting the 25°C power consumption to less than 0.5W was selected for initial testing.

It was found through testing that the 12V drain bias exceeded the maximum DC power as calculated in section 3.7. Additionally 8V showed a large growth of current over temperature, yet it was still within 1W of power consumption. For these reasons, the drain voltage of 4V was selected to aid in low power consumption.

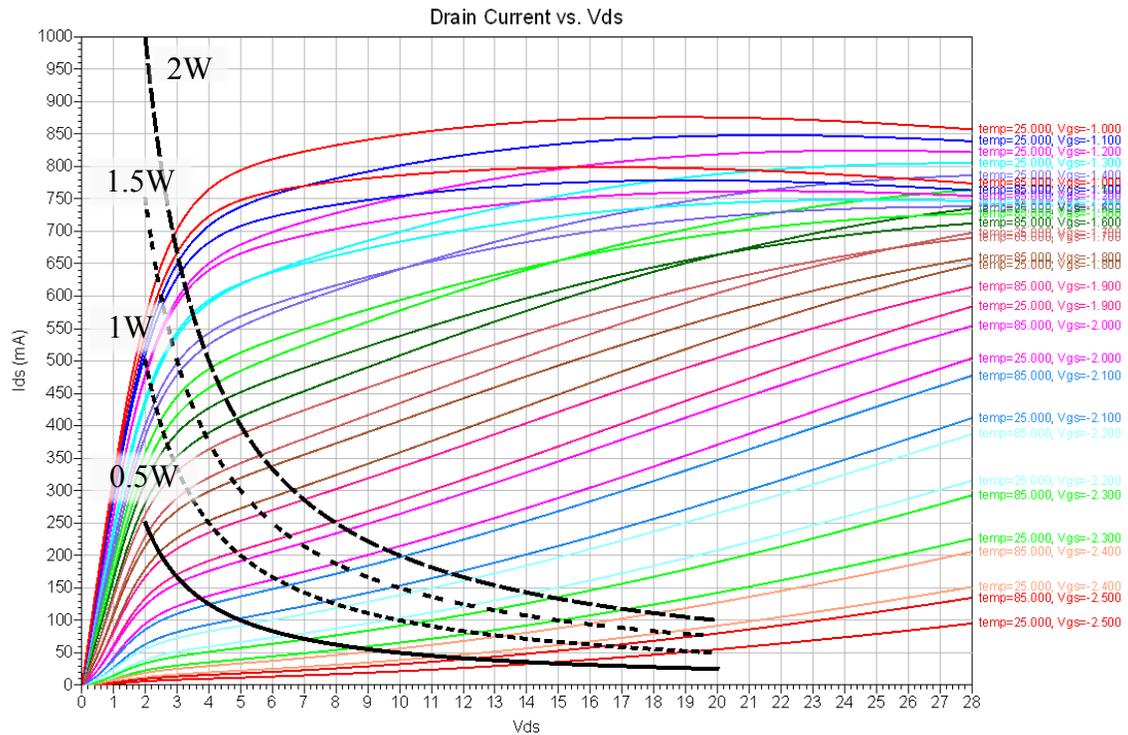


Figure 3.6: I_D vs. V_{DS} vs. V_{GS} at $T = 25^\circ\text{C} / 85^\circ\text{C}$ with $P_{DC} = 0.5, 1.0, 1.5,$ and 2.0W marked (black) – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Figure 3.7 shows the current consumption versus gate bias and temperature (up to 85°C). It can be seen that there exists a zero temperature coefficient (ZTC) I_D bias point.

However, the power consumption at this bias would be 2.43W as shown in Figure 3.8 which is too large for 230°C operation under the thermal restraints.

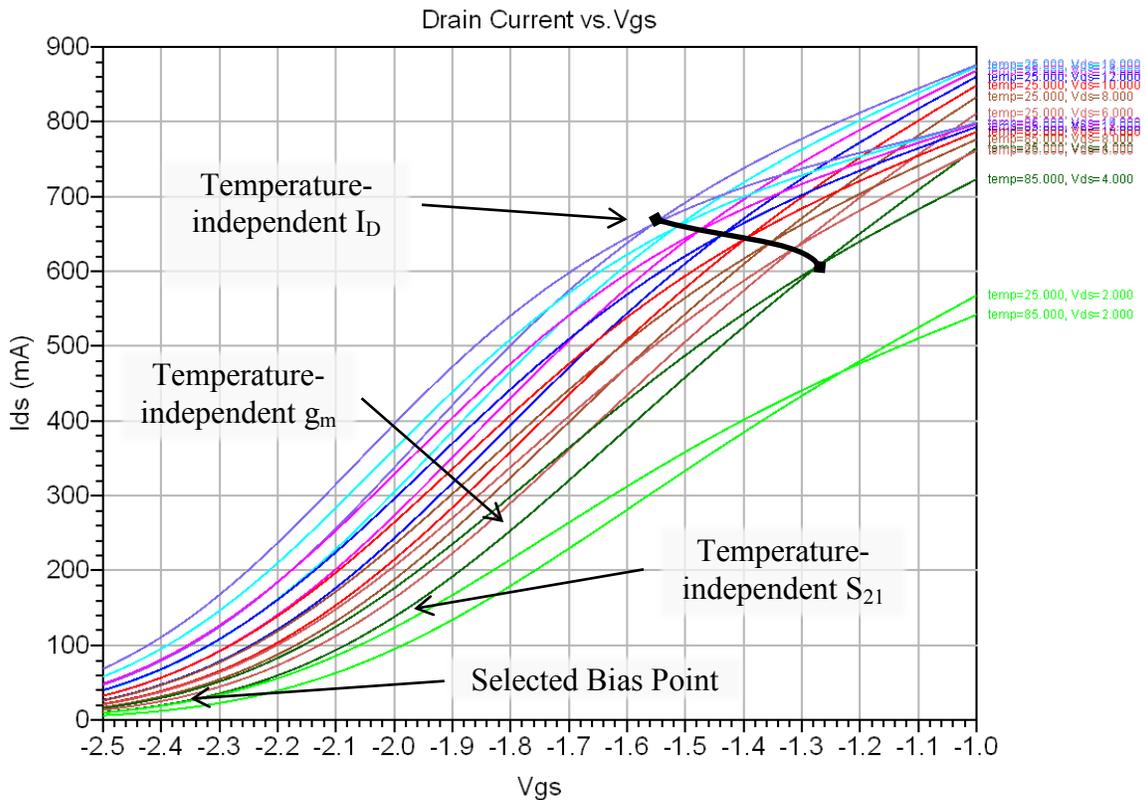


Figure 3.7: I_D vs. V_{GS} vs. V_{DS} at $T=25^\circ\text{C} / 85^\circ\text{C}$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

It should be noted that, since the selected bias will be to the left of the ZTC ID point in Figure 3.7, the current will increase with temperature. This has a higher potential for thermal runaway if proper heat extraction is not employed. However, GaN and SiC have great thermal properties [18, 34] that reduce this risk as well.

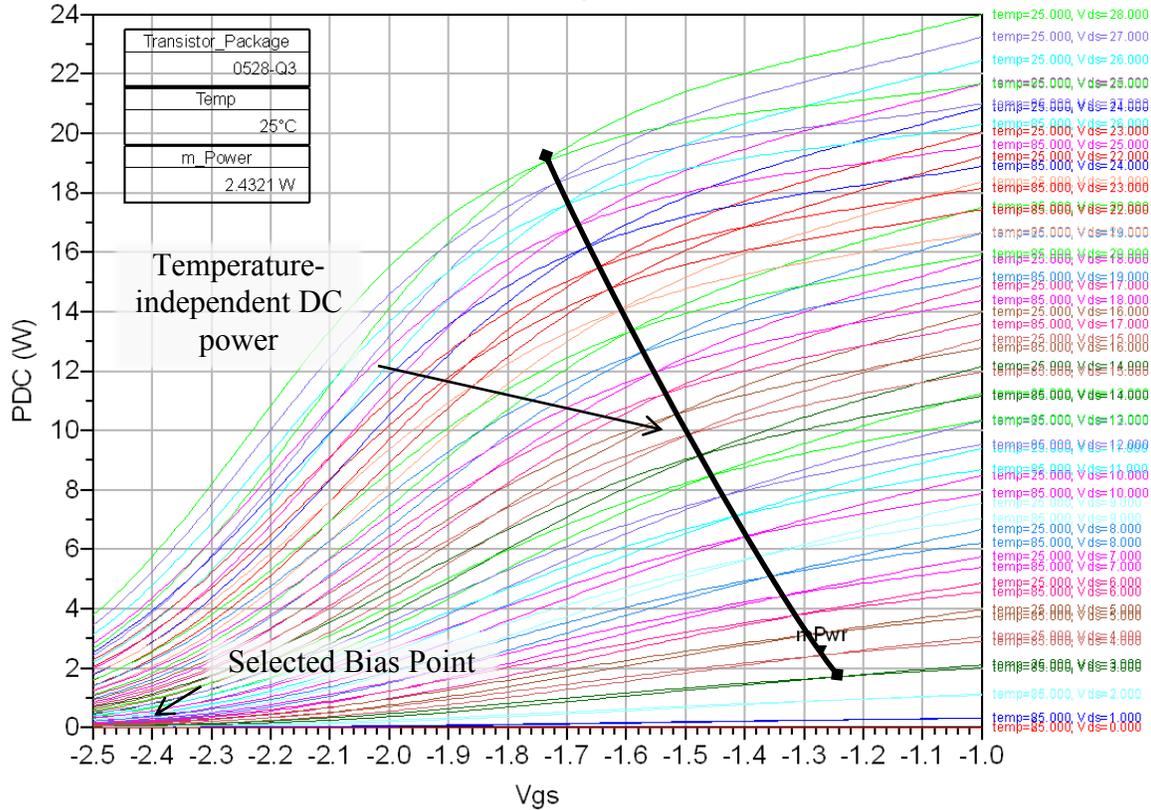


Figure 3.8: DC Power vs. V_{GS} vs. V_{DS} at $T = 25^{\circ}\text{C} / 85^{\circ}\text{C}$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Figure 3.9 shows the maximum stable gain (MSG) vs. gate control voltage. Again, there exists a ZTC point except this time the power consumption is within a range that can be implemented ($\sim 80\text{mW}$ at 25°C). Using a ZTC MSG implies that if the matching networks are adjusted to maintain a match, the gain will not vary over temperature. This is attractive for wide temperature-band matching using some form of control to aid in maintaining a matched condition. Using this approach, if the matching networks can be made to have little variance over temperature, then the gain performance should also exhibit little variance over temperature. The power consumption is referenced in the aforementioned plot against the bias conditions (Figure 3.8).

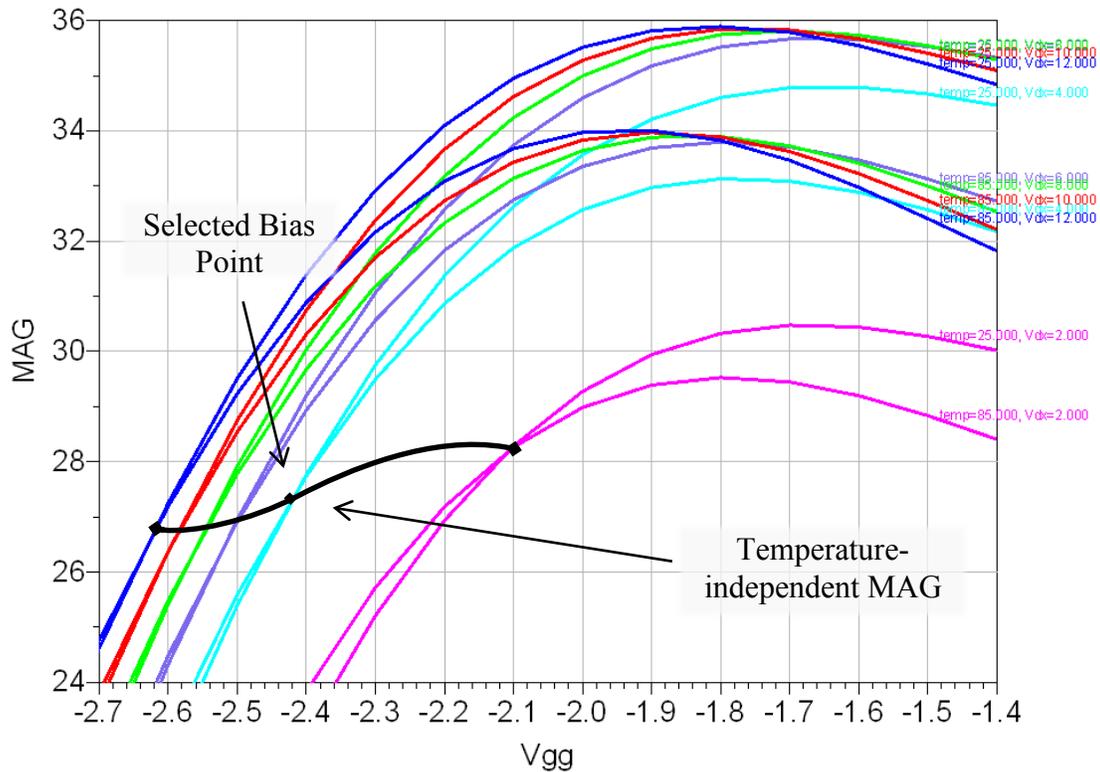


Figure 3.9: MSG vs. V_{GS} vs. V_{DS} at $T = 25^{\circ}\text{C} / 85^{\circ}\text{C}$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Also, the ZTC MSG bias condition did not change with frequency (only the level of the MSG shifts) as seen in Figure 3.10. This is useful for a wideband design in that it requires nothing more than setting the bias point and controlling the matching networks impedance at one frequency to maintain the match. The band shaping can be done externally to flatten the variance in gain over frequency, but the variance in gain at individual frequencies over temperature will be small or zero if biased properly.

Figure 3.10 shows the S₂₁ and MSG response for several gate voltages at $V_{DS} = 4.0\text{V}$. It can be seen that the gain for the selected bias ($V_{GS} = -2.4\text{V}$) actually varies with temperature by several dB. With a matching network made for 230°C operation, the mismatch should counteract the variance in gain at lower temperatures and help to stabilize the overall gain over temperature.

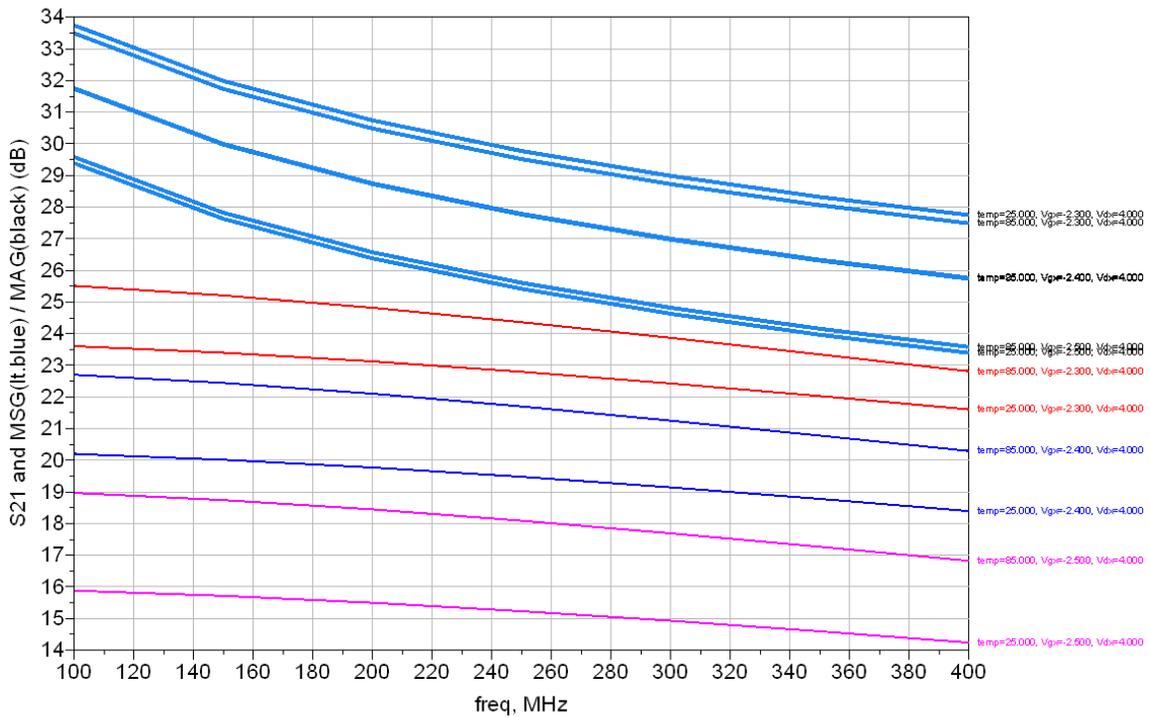


Figure 3.10: MSG vs. V_{GS} vs. V_{DS} at $T = 25^{\circ}\text{C} / 85^{\circ}\text{C}$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Although a temperature-independent gain bias condition may be easier to implement when controlled matching is not present, the power consumption required to do this with the selected device was too large. Figure 3.11 shows the gain and MSG for the bias condition ($V_{GS} = -2.0\text{V}$) using a 4.0V drain voltage that obtains a temperature-independent gain. The transconductance for this bias condition is four times larger than the selected bias, and as a result the current is also much larger (135mA at 25°C). With the larger increasing current (as suggested by Figure 3.7), the power consumption would quickly overheat the device.

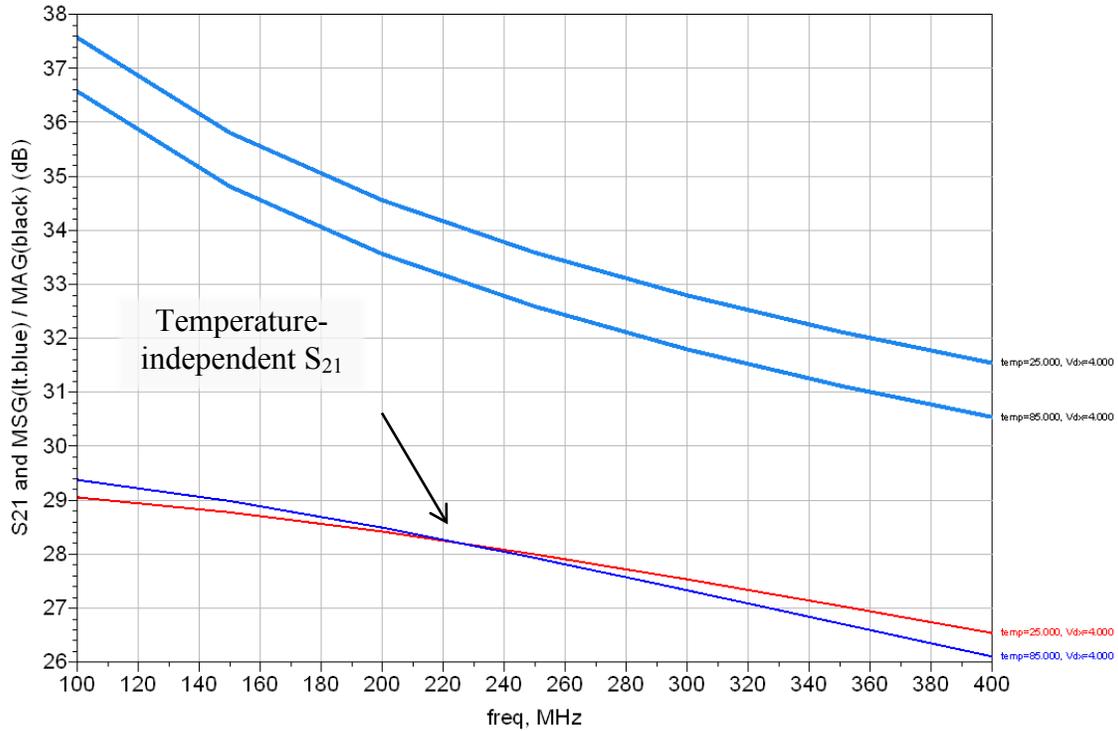


Figure 3.11: S_{21} /MSG at $V_{GS} = -2.0V$ and $V_{DS} = 4.0V$ at $T = 25^{\circ}C / 85^{\circ}C$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Another important aspect to consider in the bias point selection is the noise generation in the active device. Since the selected device is a power transistor, no noise data was provided to guide the selection and, as discussed in section 3.11, that data was not obtainable during this work.

Despite not having this information, several predictions could be made as to what should be sought in a bias condition. It is known that a higher transconductance, g_m , results in a lower noise figure [45] (although reducing g_m with other terms, e.g. proportionally with C_{gs} in the CS with inductive degeneration topology, can reduce the NF, too); therefore, the selected bias should provide a high transconductance which either increases or remains constant over temperature. As mentioned above, caution should be taken in choosing a positive temperature coefficient (i.e. PTAT) transconductance as this can lead to thermal runaway. The transconductance of the bias condition selected based on the ADS models is approximately $g_m = 125mS$ at $25^{\circ}C$ and $V_{DD} = 4V$. However, transconductance will increase with temperature proportionally to some square function.

Figure 3.14 indicates a 50mS increase over just 60°C increase. Rough estimates indicate that the g_m at 230°C should be between 300mS and 600mS; however, no test was performed at 230°C to verify the value.

There also exists a temperature-independent transconductance (ZTC_{g_m}) and a bias point where the transistor is capable of providing a large transconductance (up to approx. 700mS – 800mS), but these bias selections were avoided due to the high power requirement or large variation in gain over temperature. Figures 3.12, 3.13, and 3.14 show the transconductance from several perspectives:

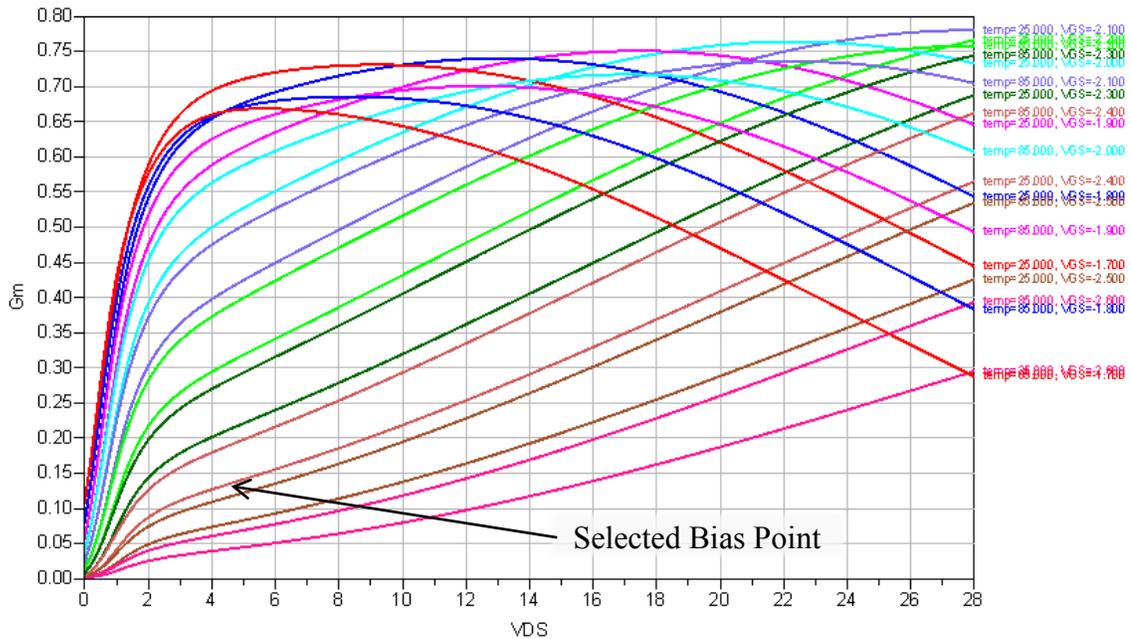


Figure 3.12: g_m vs. V_{DS} at $T = 25^\circ\text{C} / 85^\circ\text{C}$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Plotting the transconductance against the drain voltage shows that the ZTC_{g_m} bias points require either high current (the gate voltage is less negative) or high drain voltages, and both come at the price of high power consumption. Interestingly, the ZTC transconductance bias point is not the same as (or even close to) the ZTC drain current bias point. This means that if the bias point for ZTC_{g_m} is usable (under power or voltage limitations) and given that the gate control voltage is less in the ZTC_{g_m} case, the power consumption would increase (per Figure 3.8).

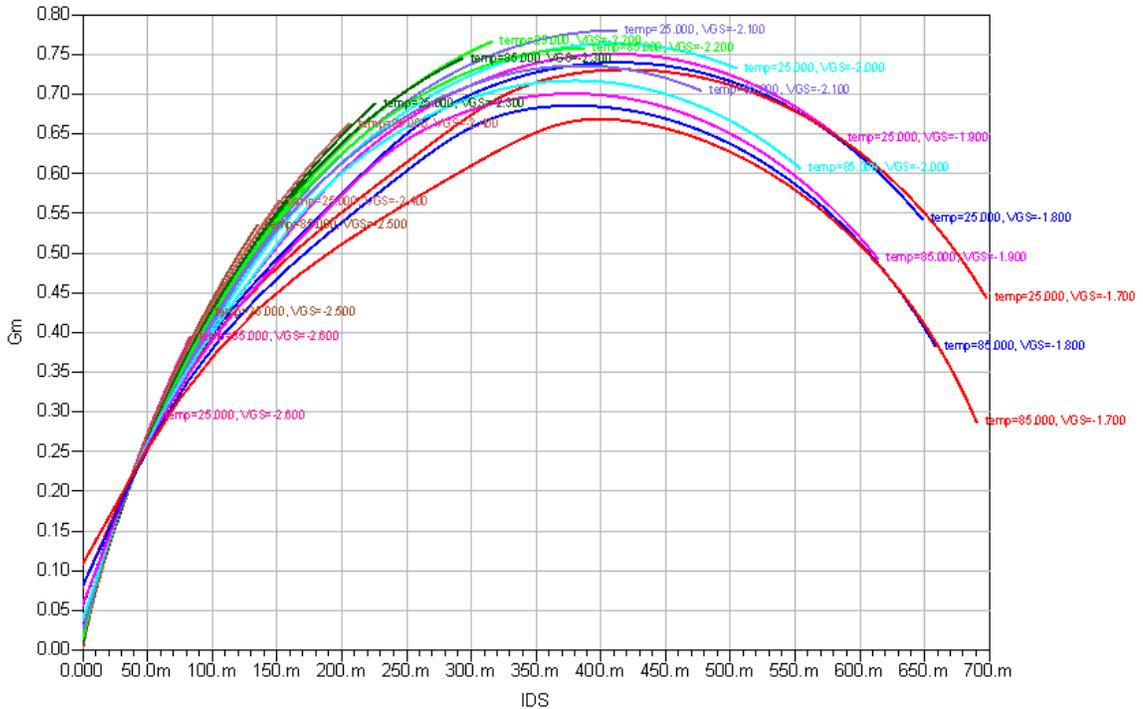


Figure 3.13: g_m vs. I_{DS} vs. $V_{GS} = 4V$ and $T = 25^\circ C / 85^\circ C$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Figure 3.13 is useful in seeing the maximum g_m and current required to achieve that point given a gate voltage. From there, the required drain voltage can be determined. Again, the power consumption required for this point ($I_D = 400mA$) would be close to or greater than 2W to be in the saturation region (see Figure 3.6).

To compliment these graphs, the transconductance is also plotted against VGS for the selected drain voltage of 4V in Figure 3.14. This shows that the g_m will increase with temperature for the selected ZTC MAG bias point. If the ZTC $_{g_m}$ bias point was selected, then the gain would drop drastically with temperature (Figure 3.9) not to mention the power consumption would rise rapidly (Figure 3.8).

Therefore, high and stable transconductance was traded for a ZTC gain. This bias point leads to an increasing g_m which will help suppress growing noise as temperature rises.

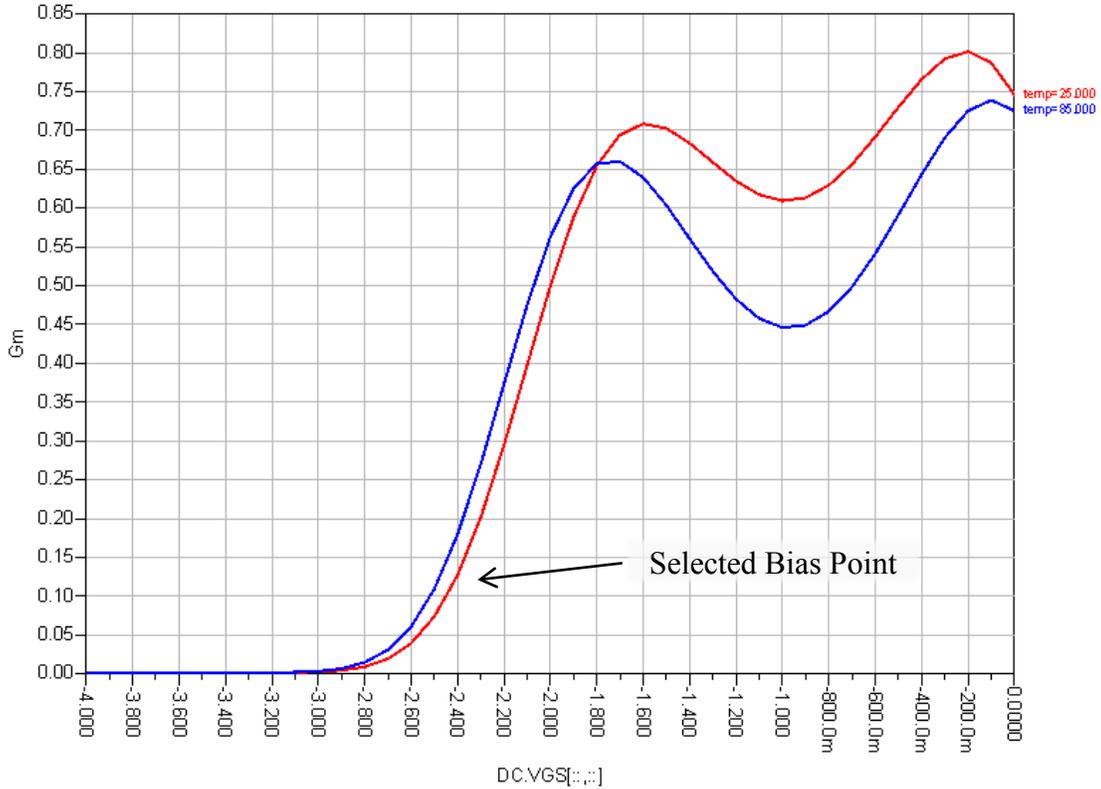


Figure 3.14: g_m vs. V_{GS} at $V_{DS} = 4V$ and $T = 25^\circ C / 85^\circ C$ – (0528-Q3 model) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

3.7 Thermal Considerations

Every design should always explore the limitations of all the devices to ensure that the performance is reliable and no failures arise. Section 2.3 details the following equations.

The device has a rated $R_{\theta JC} = 12.4^\circ C/W$ and $T_{JMAX} = 275^\circ C$ as mentioned in section 3.4. Using the thermal equations we have

$$P_{MAX} = \frac{T_{JMAX} - T_{AMBIENT}}{R_{\theta JA}} = \frac{T_{JMAX} - T_{AMBIENT}}{R_{\theta JC} + R_{\theta CA}} = \frac{275^\circ C - 230^\circ C}{12.4^\circ C/W + R_{\theta CA}} \quad (3.1)$$

In order to determine the maximum dissipated power, the case-to-ambient heat flow paths need to be determined and the associated thermal resistance calculated.

Table 3.4: Thermal Resistances/Conductivity of Board Materials [15, 44, 46-48]

Device	Thermal Resistance/Conductivity ¹
GaN Transistor (1528 Q3)	$\theta_{JC} = 12.4^{\circ}\text{C}/\text{W}$
R04003C Laminate (board dielectric)	$\kappa = 0.71\text{W}/(\text{m}\cdot\text{K})$
Copper	$\kappa \cong 390\text{W}/(\text{m}\cdot\text{K})$
Indalloy#164 (92.5Pb-5.0In-2.5Ag) ²	$\kappa = 25\text{W}/(\text{m}\cdot\text{K})$
Screws (Zinc-plated [Carbon] Steel)	$\kappa \cong 40\text{W}/(\text{m}\cdot\text{K})$
Convective Heat Transfer Coeff. Of Air	$h_c \cong 5 - 25 \text{ W}/(\text{m}^2\cdot\text{K})$

Table 3.5: Dimensions of Board Materials in Primary Heat Flow Path [44, 46]

Dimension	Dimensions of RO4003
Dielectric Thickness	1.524mm
Copper Thickness (per layer)	35 μm
Area	(arbitrary)
GaN Pad	4.699mm \times 3.683mm = 17.3mm ²
#2 Screw Diameter	86mil = 2.18mm

The best way to determine the heat flow is by using software that utilizes finite difference methods or similar techniques. However, a one-dimensional heat flow analysis using estimations should provide enough insight for this application.

Radiation was ignored both because the temperature difference between the generator and absorber is not too large and it is assumed that the radiation is contained in the immediate black body surroundings; therefore, it is not a significant method of heat transfer when the device is on. Note that this assumption of negligible radiation is not entirely accurate, but used to reduce the complexity of the estimation.

¹ Thermal conductivity was estimated at 230°C when trends were listed, otherwise it was assumed constant.

² Indalloy#164 is similar to Indalloy#151. The thermal conductivity was not listed for Indalloy#151, so the property of Indalloy#164 was used (5% In vs. 5% Sn won't affect much as these elements have similar thermal conductivities).

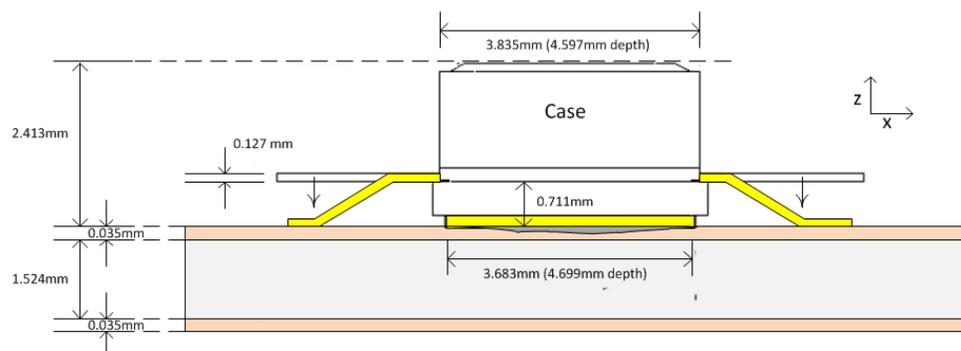


Figure 3.15: Side-view and dimensions of device (0528-Q3) on board material [44]

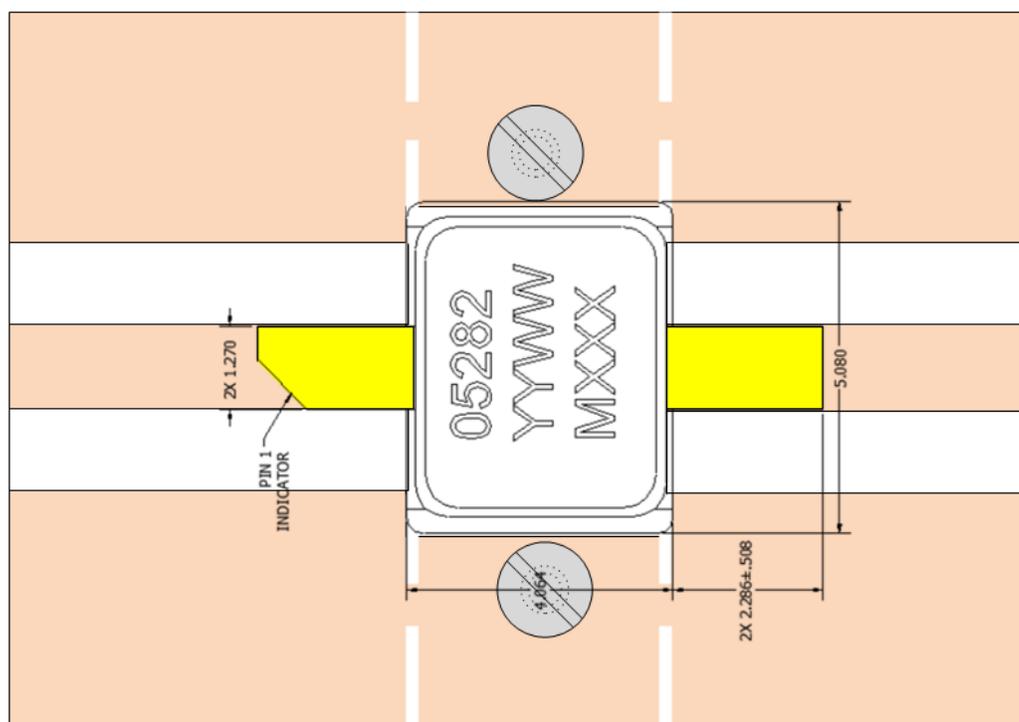


Figure 3.16: Top-view and dimensions of device (0528-Q3) on board material [44]

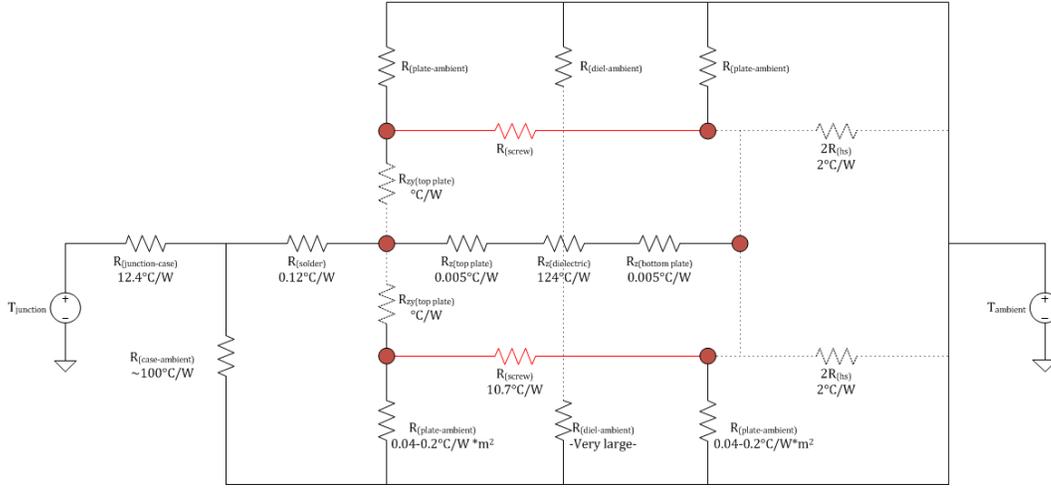


Figure 3.17: Equivalent thermal circuit.

In Figure 3.17, red circles represent interface loss (i.e. thermal contact resistance). However, it is assumed that bonding is well manufactured and thermal paste or solder will reduce the amount of air/roughness between materials to negligible amounts. The following equations estimate thermal resistances from the thermal circuit in Figure 3.17.

$$R_{Cu,z} = \left(\frac{1}{390 \left[\frac{W}{m \cdot ^\circ C} \right]} \right) \left(\frac{35 \mu m}{(3.683 mm)(4.699 mm)} \right) = 0.0052^\circ C/W \quad (3.2)$$

$$R_{Solder} = \left(\frac{1}{25 \left[\frac{W}{m \cdot ^\circ C} \right]} \right) \left(\frac{50 \mu m}{(3.683 mm)(4.699 mm)} \right) = 0.116^\circ C/W \quad (3.3)$$

$$R_{diel,z} = \left(\frac{1}{0.71 \left[\frac{W}{m \cdot ^\circ C} \right]} \right) \left(\frac{1.524 mm}{(3.683 mm)(4.699 mm)} \right) = 124.03^\circ C/W \quad (3.4)$$

$$R_{Cu,xy} = \left(\frac{1}{390 \left[\frac{W}{m \cdot ^\circ C} \right]} \right) \left(\frac{L}{(3.683 mm)(35 \mu m)} \right) = 19.9^\circ C/(W \cdot mm) \cdot L \quad (3.5)$$

$$R_{screw} = \left(\frac{1}{40 \left[\frac{W}{m \cdot ^\circ C} \right]} \right) \left(\frac{\sim 1.6mm}{\pi(1.09mm)^2} \right) = 10.72^\circ C/W \quad (3.6)$$

$$R_{surf-air} = \left(\frac{1}{5 \text{ to } 25 \left[\frac{W}{m^2 \cdot ^\circ C} \right]} \right) \left(\frac{1}{A_{surface}} \right) \quad (3.7)$$

$$= 0.04 \text{ to } 0.2^\circ C \cdot m^2/W \cdot \frac{1}{A_{surface}}$$

Several results can be disregarded due to the large thermal resistance: $R_{diel-ambient}$ and $R_{surf-air(Cu)}$ for the heat removal from the surface of the copper plating.

If the screws are placed close to the device, then the thermal resistance will not be too large. Assuming a 1.0 mm length of copper between the pad and the screw via

$$R_{Cu,xy} = 19.9^\circ C/(W \cdot mm) \cdot 1mm \approx 20^\circ C/W \quad (3.8)$$

The surface area of the device in contact with the air is as follows:

$$A_{surface} = 2(4.597)(2.413) + 2(3.835)(2.413) + (4.597)(3.835) \quad (3.9)$$

$$= 58.32mm^2$$

$$R_{surf-air} = 0.04^\circ C \cdot \frac{m^2}{W \left(\frac{1}{58.32mm^2} \right) \left(\frac{1000mm}{m} \right)^2} = 686^\circ C/W \quad (3.10)$$

However, this approximation may not hold well since it assumes that the ceramic case is entirely at the same temperature as the pad and may even be influenced by thermal radiation (which is being ignored in this estimation). Rough estimates calculated from thermocouple measurements and the following equations indicate that the surface-to-air thermal resistance can be assumed to be approximately $100^\circ C/W$. Without the heatsink, the thermal circuit is approximated to yield a total thermal resistance between junction and ambient of

$$\begin{aligned}
R_{eq} &= R_{\theta JC} + (R_{\theta CAir} \parallel \left(R_{\theta solder} + \left(R_{\theta z} \parallel \frac{(R_{\theta xy} + R_{\theta screw})}{2} \right) + R_{\theta surf-air} \right)) \\
&= 12.4 + (100 \parallel \left(0.12 + \left(124 \parallel \frac{(20 + 11)}{2} \right) + (\sim 1000) \right)) = 103^\circ C/W
\end{aligned} \tag{3.11}$$

This would allow for a maximum power dissipation (at $T_A = 230^\circ C$) of

$$P_{MAX} = \frac{275^\circ C - 230^\circ C}{103^\circ C/W} = 0.44W \tag{3.12}$$

With the heatsink, the thermal resistance is reduced significantly to

$$\begin{aligned}
R_{eq} &= R_{\theta JC} + (R_{\theta CAir} \parallel \left(R_{\theta solder} + \left(R_{\theta z} \parallel \frac{(R_{\theta xy} + R_{\theta screw})}{2} \right) + R_{\theta HS} \right)) \\
&= 12.4 + (100 \parallel \left(0.12 + \left(124 \parallel \frac{(20 + 11)}{2} \right) + 1 \right)) = 25.4^\circ C/W
\end{aligned} \tag{3.13}$$

Adding the heatsink allows for much greater power margin and also higher ambient temperatures (0.25W dissipated power assumed for calculation below).

$$P_{MAX} = \frac{275^\circ C - 230^\circ C}{25.4^\circ C/W} = 1.77W \tag{3.14}$$

$$T_{AMBIENT,MAX} = 275^\circ C - (0.25W) \left(25.4^\circ \frac{C}{W} \right) = 268.65^\circ C \tag{3.15}$$

The heat sink can improve the performance by creating a larger ground plane and also aid in the reduction of thermal excitation on the board (reducing the NF and extending the maximum ambient temperature capabilities). However, it is also relatively large and restricts the board dimensions (Figure 3.25 in section 3.8).

3.8 Passive Devices and Interface Materials

As introduced in section 2.5, all the materials and devices being used need to be carefully selected or designed in order to not degrade the reliability of the circuit. The following subsections discuss the selection of each passive/interface device. All the specific models selected are listed in Table 3.7 (section 3.13).

3.8.1 Resistors

Resistors needed to be included in the design to provide stabilization and feedback. Vishay offers precision automotive high temperature thin film resistors (PATT series) that have a rated operating range up to 250°C (Figure 3.18). The datasheet [49] claims a 0.1% tolerance of value at 25°C and is specified to have a $\pm 25\text{ppm}/^\circ\text{C}$ additional change in value up to 175°C. If it is assumed that this variation holds over the operating temperature, then an ambient temperature of 230°C would suggest approximately a 0.5% shift in value from 25°C to 230°C.

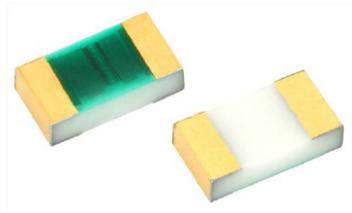


Figure 3.18: PATT series Vishay Dale Thin Film Resistors [49] [fair use]

Additionally, these resistors don't contribute much excess noise to the thermal noise they generate. Since the feedback resistor will always be in the direct signal path, its noise contributions are important to consider.

A derating curve is provided in the datasheet (Figure 3.19). At an ambient temperature of 230°C, the power limitation is derated to 20% of full power (0.2W for an 0805 package), which is 40mW.

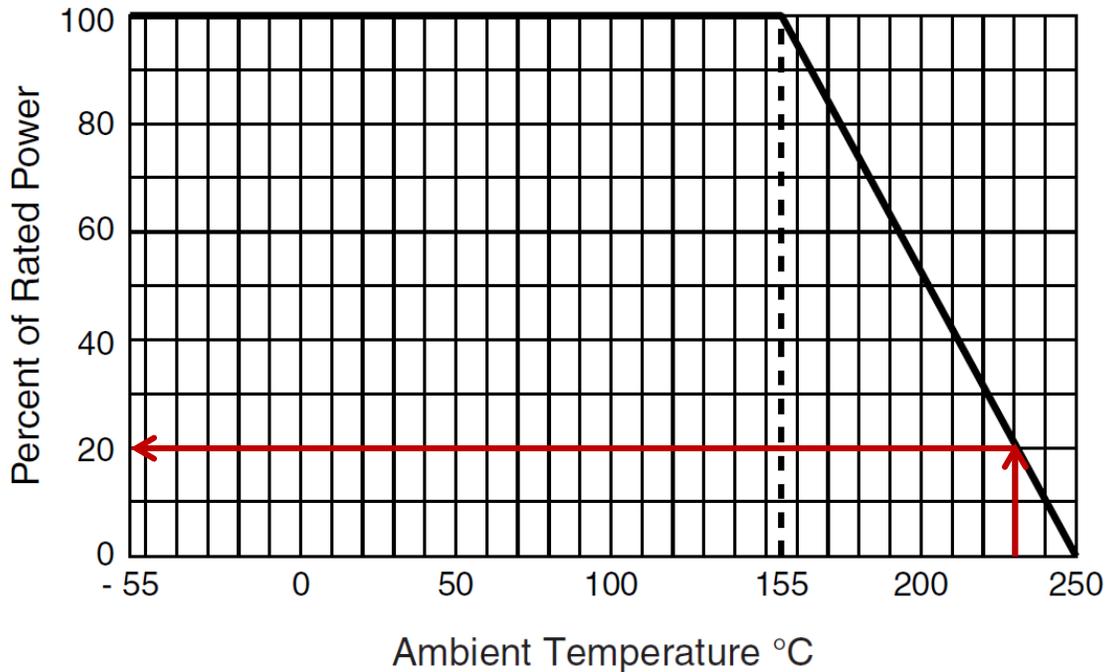


Figure 3.19: Derating curve for Vishay PATT resistor [49] [fair use]

3.8.2 Inductors (RF Choke)

High temperature coils are more difficult to find – the factors that contribute to inductance experience large changes over temperature. However, Coilcraft offers specialty inductors that can withstand high temperatures. They did offer air coils in the nH range; but, in order to reduce passive components factoring into performance, only the large core inductors were investigated for bias lines.

Coilcraft's Extreme Temperature coil (pictured in Figure 3.20) operates up to 300°C according to the datasheet [50]. The largest value available for purchase (1μH) was selected. The tolerance of this component is ±20% on the nominal value at room temperature and 300-500ppm/°C up to 250°C which is a 6-10% change over temperature from the actual value. It has a specified DC resistance of 15mΩ and a current handling capability of 1A. Both of these meet reasonable limits when factoring in the voltage drop and coil current.



Figure 3.20: Coilcraft 1 μ H inductors (AT549RBT102MLZ) [50] [fair use]

No derating or thermal resistance was mentioned. However, since the inductors would have less than 10% of the full rated current at 70°C backed off from the operating, derating concerns were ignored.

The last important factor was the on-board self-resonant frequency (SRF). The datasheet shows an SRF of around 350MHz (which is what was seen in measurement) and specifies that a transmission null will occur above 800MHz (see Figure 3.21). This offers no path for the currents at high frequencies to enter the circuit or the voltage rail. At 200MHz, the impedance of the inductor should be around

$$X_L = 2\pi(200\text{MHz})(1\mu\text{H}) = 1.257\text{k}\Omega \quad (3.16)$$

which is significantly higher than the low input impedance of the device ($\sim 25\Omega$). In fact the choke becomes irrelevant around 40MHz.

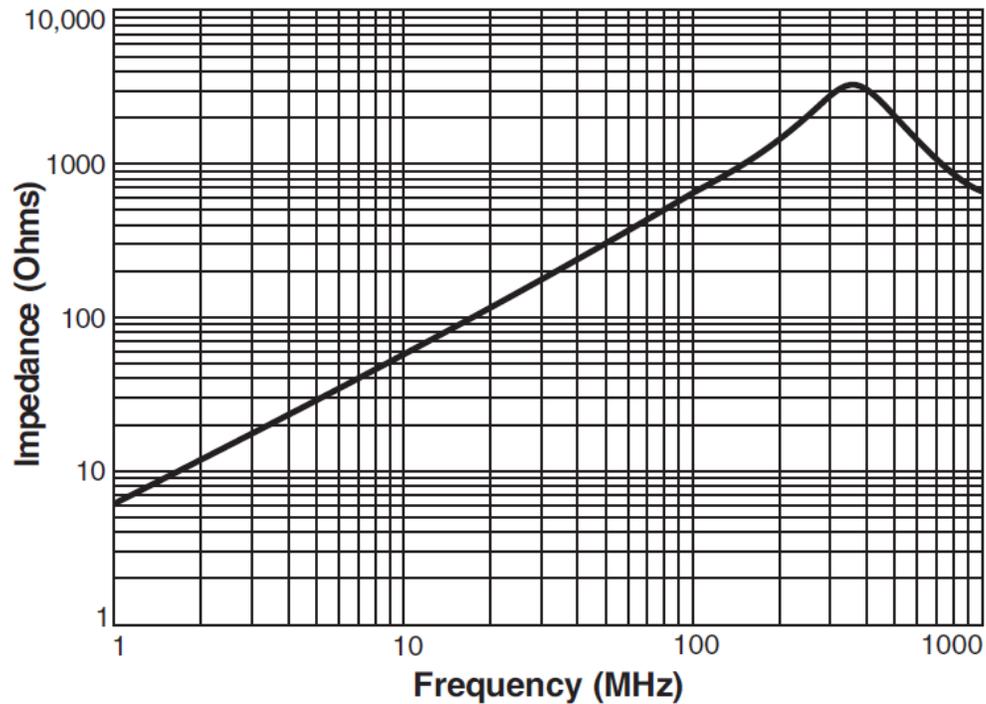


Figure 3.21: Impedance vs. Frequency – Coilcraft 1 μ H (AT549RBT102MLZ) [50] [fair use]

3.8.3 Capacitors

The capacitors were also difficult to select do to variances in common material properties. Two companies were approached for this application: IPDiA and Presidio Components. Both offered capacitors that could operate up to 250°C with relatively stable performance over the entire range.

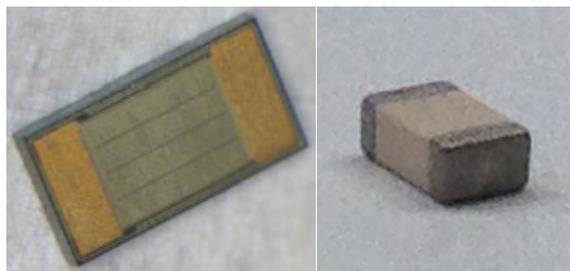


Figure 3.22: IPDiA (left) [51] and Presidio (right) capacitors [fair use]

IPDiA capacitors were used for DC blocking and bypass capacitors. IPDiA's silicon capacitor technology (deemed passive integrated connecting substrate (PICS)) outperformed both C0G (Electronic Industries Alliance (EIA) class 1 dielectric according to the RS-198 standard) and X8R (EIA class 2 dielectric according to the RS-198

standard) materials as seen in Figure 3.23. The datasheets [52-55] claim a 15% nominal variance and $< \pm 1.5\%$ temperature variance up to 250°C as well as a $0.1\%/V$ shift in value. The equivalent series inductance (ESL) and equivalent series resistance (ESR) are also provided, allowing for estimations of the SRF and quality. Although several different packages were used, the devices all had 11V working voltages and similar performance with exception of the packaging parasitics.

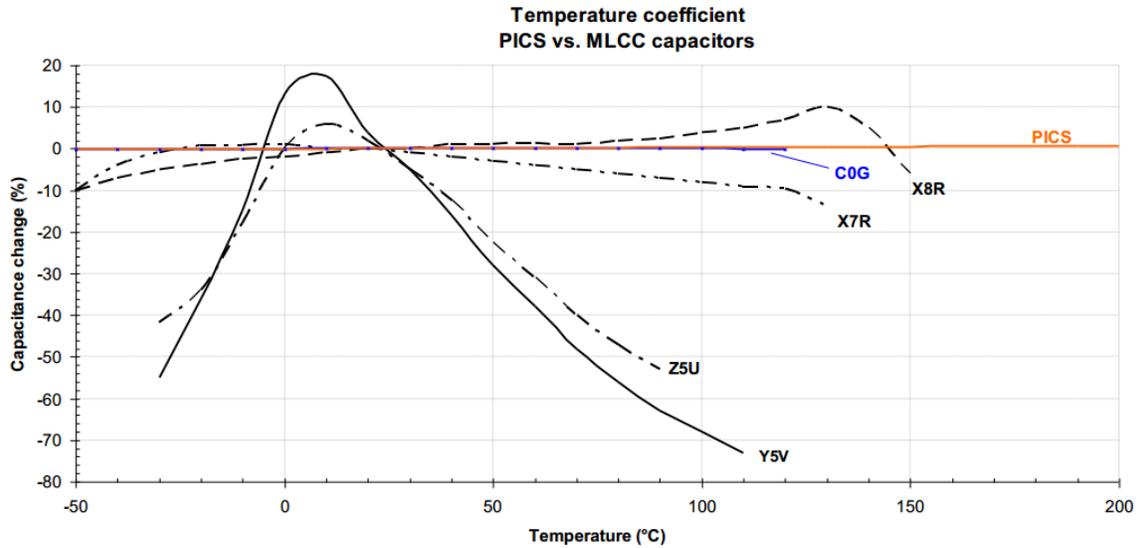


Figure 3.23: IPDiA’s PICS vs. MLCC (Multilayer Ceramic Chip) capacitors [52-55] [fair use]

The estimated SRF for each package is shown in table 3.6. Although the $1\mu\text{F}$ capacitor value has a low SRF, its primary function is to block DC and pass RF in the band of interest. The impedance of the 1206 capacitor at 300MHz (assuming it is purely inductive at this point) will be approximately

$$X_{C1206} \approx 2\pi(300\text{MHz})(1\text{nH}) = 1.9\Omega \quad (3.17)$$

which is still significantly small enough to pass RF. Of course, the capacitor offers adequate blocking of DC signals with an insulation resistance of $10\text{G}\Omega$ at 250°C and 3V (which is very close to the stress it will be under).

The wide spread in frequency for the bypass values (100pF , 10nF , and $0.1\mu\text{F}$) allows for the low impedance extraction of spurs and noise on the DC line far beyond the bandwidth of interest. The importance of the bypass capacitors and the performance of the bias design will be discussed in section 3.9.

Table 3.6: Estimated SRF of IPDiA capacitors [52-55]

Self-Resonant Frequency - IPDiA			
Capacitance	Package	ESL	SRF
100 pF	0402	100pH(max)	~2.25GHz
10 nF	0201	100pH(max)	~160MHz
0.1 μ F	0805	250pH(max)	~31.8MHz
1 μ F	1206	1nH(max)	~4.75MHz

A 4.7nF 0805 NP0 Presidio capacitor was used for the output matching network. The choice of this device here came down to the ease of mounting the Presidio capacitors (SMT) versus the IPDiA capacitors (flip chips). The NP0 (negative-positive 0 ppm/°C) dielectric offers temperature stability, which is very important for the matching network. Additionally, Presidio had a wide selection of capacitors available through Trendsetter Electronics for an affordable price. Unfortunately, Presidio’s datasheet catalog [56] didn’t provide as much detail as IPDiA’s regarding parasitics, but tests showed that it worked as expected. The selection of palladium terminations and high dielectric withstanding voltage assured reliable operation at high temperature with only RF power dissipating in it.

3.8.4 Board Material

The board material selected needed to be able to withstand the temperature and mechanical stress as well as provide a low loss tangent for high frequency operation. Rogers 4003C board was selected as it met these conditions very well. Estimates using specifications from the datasheet [46] on temperature-related variance showed negligible expansion of the board in three dimensions and <1% change in the relative dielectric constant. These calculations suggested controlled microstrip matching and characteristic impedances over a wide temperature range. Additionally, the glass transition temperature of the material (the point where a polymer changes from a hard substance to a soft, malleable substance) is >280°C which is sufficiently high to avoid structural failure of the design when operating at 230°C.

The board selected is a one-layer board with 1oz. cladding on the top and bottom. The dielectric height chosen was 60mil (1.524mm). A thicker substrate will require larger

lines for a given characteristic impedance, but will also reduce the effective wavelength. A 1oz. cladding offered low resistivity with little increase in the effective wavelength. Additionally, milling the boards with an LPKF Protomat S43 also limited the practical thickness for a “clean” print.

3.8.5 Solder

The solder was selected based on melting point and reliability of joint. Indalloy#151 (92.5%Pb, 5%Sn, and 2.5%Ag) [48] in the form of a dispensable solder paste was commercially available, offered a melting point of 296°C, and exhibited very low resistivity with sufficient strength ensuring that it wouldn’t melt while at 230°C.

3.8.6 Hardware (Screws/Nuts)

The screws were used to both secure the board to the heatsink and act as vias for top to bottom (i.e. ground) connections. High thermal and electrical conductivity screws were ideal, but simple carbon steel screws from Pololu worked well enough. The only constraint was getting small enough screws to conserve room. For this reason #2 7/16” length screws were used.

3.8.7 Connectors

The connectors were chosen to be SMA as this exhibited a reliable 50Ω connection up to 18 GHz. Although the Cinch datasheet [57] only rates the connectors from -65°C to 165°C, the individual materials were all capable of withstanding 230°C alone with a significant margin of several hundred degrees centigrade. This coupled with the small expansion rates of the material were enough to infer safe incorporation even with an unknown reduction in thermal limitations due to material interfacing. Testing showed no noticeable degradation in performance up to 250°C.

3.8.8 Heat Sink

In order to reduce thermal limits and thermal noise, a heat sink was selected with a thermal resistance of ~1°C/W according to Wakefield-Vette’s datasheet for the 423K extruded heatsink [58]. Figure 3.24 shows the curves for calculating thermal resistance. Using the red line, it can be seen that the thermal resistance is about 1°C/W or less. To calculate the thermal resistance from the natural convection curves (left and bottom

axes), the temperature rise is divided by the power dissipation: $R_{\theta HS} = \Delta T/P_D$. The degradation in efficiency due to a high ambient temperature was ignored for this.

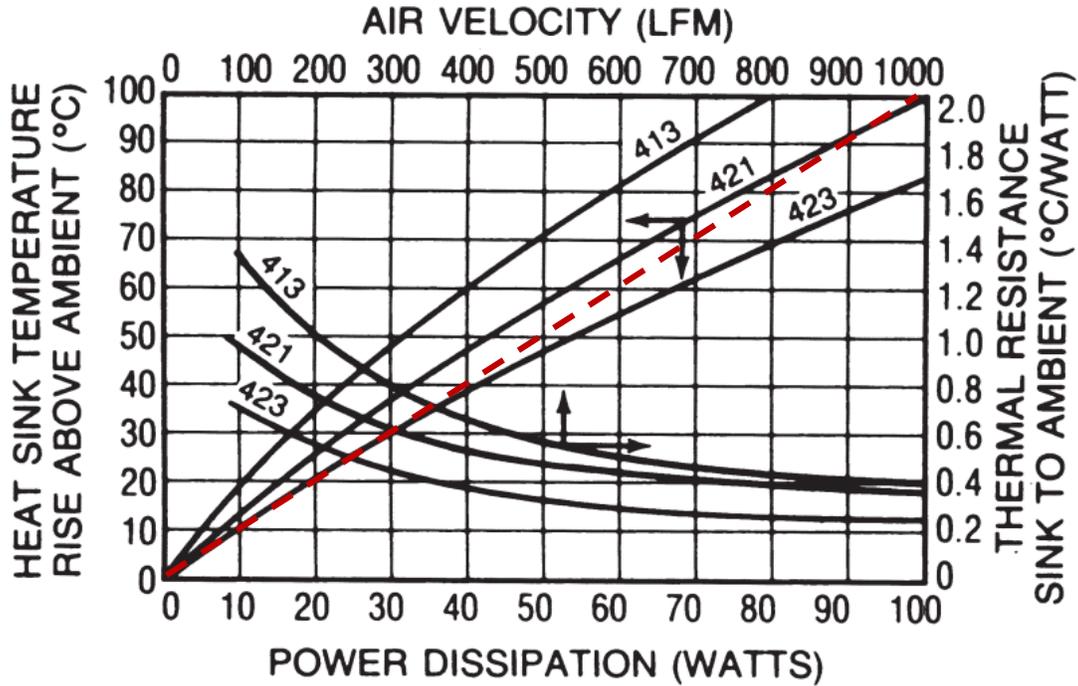


Figure 3.24: Natural and forced convection characteristics with 1°C/W line (red) [58] [fair use]

As mentioned, the heat sink dimensions also played an restricting factor in board layout. Figure 3.25 details the dimensions of the selected heat sink.

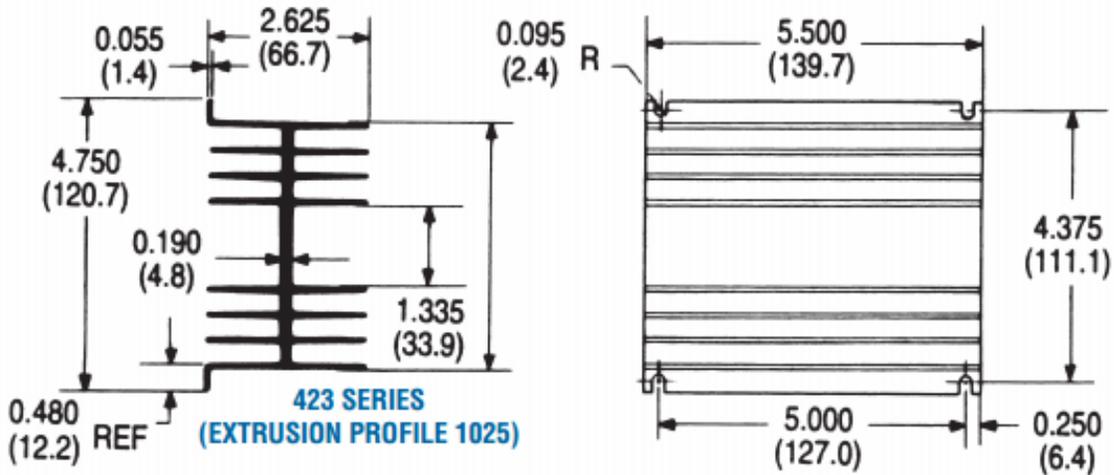


Figure 3.25: Heat sink dimensions [58] [fair use]

3.9 Bias Network Design

The bias network was facilitated using an on-board bias tee. DC and RF signals would be applied via different SMA connectors and combined at the transistor input and output.

During characterization the input of the transistor was seen to be lower than 50Ω and the output was close to 50Ω . This was also the case with the feedback topology selected. In order to ensure that the inductors and capacitors of the bias tee were sufficiently removed from the circuit in the frequency band of interest, it was desired to have the impedances of the bias tee much greater (ten times or more) than the input impedance of the LNA.

3.9.1 RF Choke

The largest inductor that could withstand the temperature of 230°C at the time of this writing was a $1\mu\text{H}$ cored inductor from Coilcraft. The datasheet [48] showed an impedance self resonant frequency (SRF) of approximately 350MHz . At DC, the inductor would provide a short with around $15\text{m}\Omega$ or resistance and at 200MHz , the inductor impedance was calculated as

$$X_L = \omega L = (2\pi)(200\text{MHz})(1\mu\text{H}) = 1.257\text{k}\Omega \quad (3.18)$$

This is large enough to be sufficiently removed from the RF current path. In fact, the inductor becomes irrelevant around approximately 40MHz . However, because of the SRF, the impedance will drop after 350MHz . This means that it will be a current path at some higher frequency. Assuming that the input of the device remains below 50Ω when this happens, the frequency where the inductor “re-enters” the circuit is calculated using the capacitor equation. The capacitance associated with a 350MHz SRF is

$$C_{1\mu\text{H}} = \frac{1}{\omega_{\text{SRF}}^2 L} = \frac{1}{((2\pi)(350\text{MHz}))^2 (1\mu\text{H})} = 0.207\text{pF} \quad (3.19)$$

and the inductor becomes important again at

$$f'_{1\mu\text{H}} = \frac{1}{(2\pi)(X'_L)(C_{1\mu\text{H}})} = \frac{1}{(2\pi)(500)(0.207\text{pF})} = 1.54\text{GHz} \quad (3.20)$$

This is about five times the maximum frequency in the band of interest and shouldn't cause any problems. It should be noted that the frequency may be slightly shifted from the calculated value to due parasitic inductances and capacitances on the board. However, the margin should be sufficient to account for this.

3.9.2 DC Blocking Capacitor

The same procedure is used for the blocking capacitors, albeit using the dual equations. A 1 μ H capacitor was selected from IPDiA. The datasheet [55] indicates that the ESL is 1nH max. The capacitor should fully pass signals in the band of interest. Like the inductor, the capacitor will eventually change impedances. The SRF is estimated as

$$SRF = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(1nH)(1\mu H)}} = 5MHz \quad (3.21)$$

This SRF is very low and may cause problems in the band of interest. The impedance of the “capacitor” in the band of interest will rise with frequency. In order to ensure that the signal passes with little loss, the impedance at the upper end is estimated

$$X'_C = \omega L_{1\mu F} = (2\pi)(300MHz)(1nF) = 1.885\Omega \quad (3.22)$$

This impedance is small enough and should cause little attenuation for passing signals. However, it is much larger than desired. A smaller package size could help in reducing this, but none existed for this value at the time.

3.9.3 Bypass Capacitors

The last part of the bias network to design was the bypass capacitors. These are important in order to remove noise, such as leaked signals, from the DC line to help provide a clean bias.

The selection of the capacitor values should be of ones that will provide small impedance over a wide frequency band. For this reason, several values are needed in parallel to account for the SRF of each individual capacitor.

The SRF design aspect is the most important one for bypass capacitors. Smaller packages often have less parasitics and, therefore, have higher self resonant frequencies. However, if all of the capacitors are chosen to have the same package, they will all have roughly the same inductance, just at different frequencies, causing a very minor

improvement (they would intercept the same inductive part of the impedance line in Figure 3.26, just at different frequencies). This would reduce the total inductance by however many capacitors are in parallel, but this cannot achieve as good of a response as using smaller package sizes with decreasing capacitance.

Three capacitors were used, all from IPDiA, and each in a different package size. For low frequencies, an 0805 0.1 μ F capacitor was used [54]; for mid-range frequencies, an 0201 10nF capacitor was used [52]; and, for high-frequencies, an 0402 100pF capacitor was used [53]. Figure 3.26 shows the impedance of the parallel combination of these capacitors with the maximum listed parasitics from their datasheets.

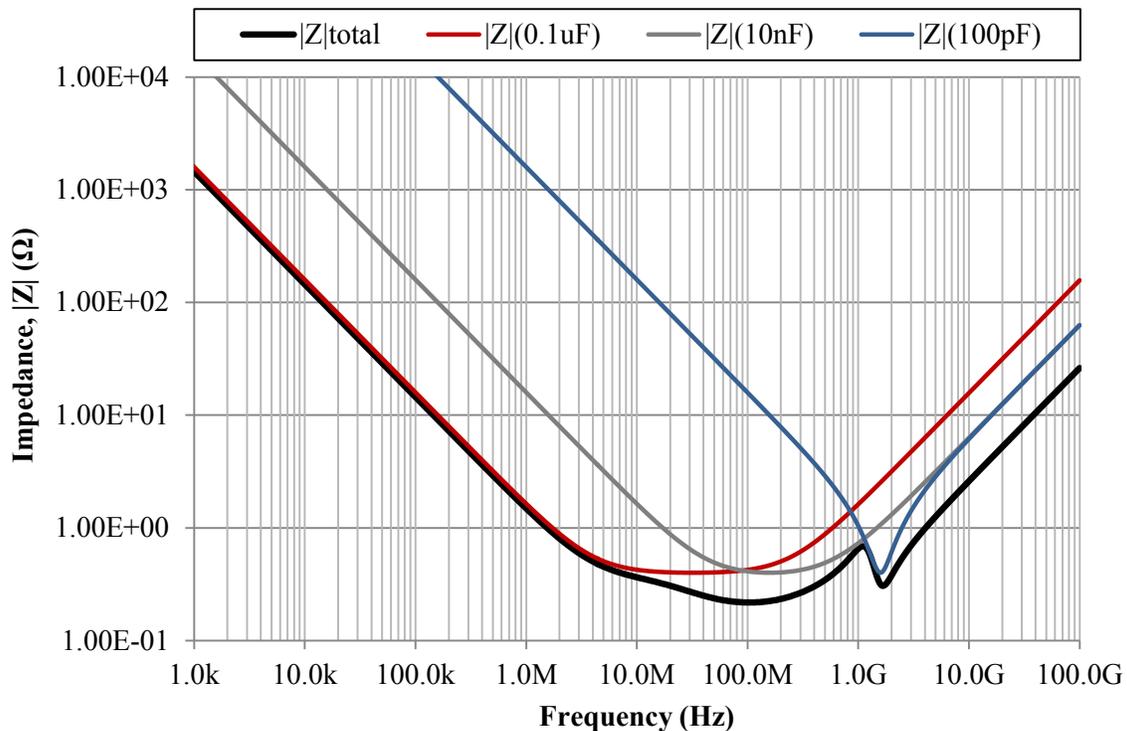


Figure 3.26: Impedance of bypass capacitor network vs. frequency

This combination of bypass capacitors provides a sufficient ground path for non-DC signals on the bias line up to very high frequencies ensuring a stable DC supply to the LNA. Even with variations due to board parasitics and placement, the bypass network is wideband enough to always provide a clean DC line.

3.10 Stabilization

The importance of stabilization is discussed in section 2.1.6 and is very much an interest in the LNA. It was decided that unconditional stability was the best option for robustness despite the degradation in performance needed to achieve it. The HEMT being used was found to be conditionally stable over much of the usable frequency range and had a high potential for instability in the frequency band of interest as indicated with the μ stability parameter in Figure 3.27.

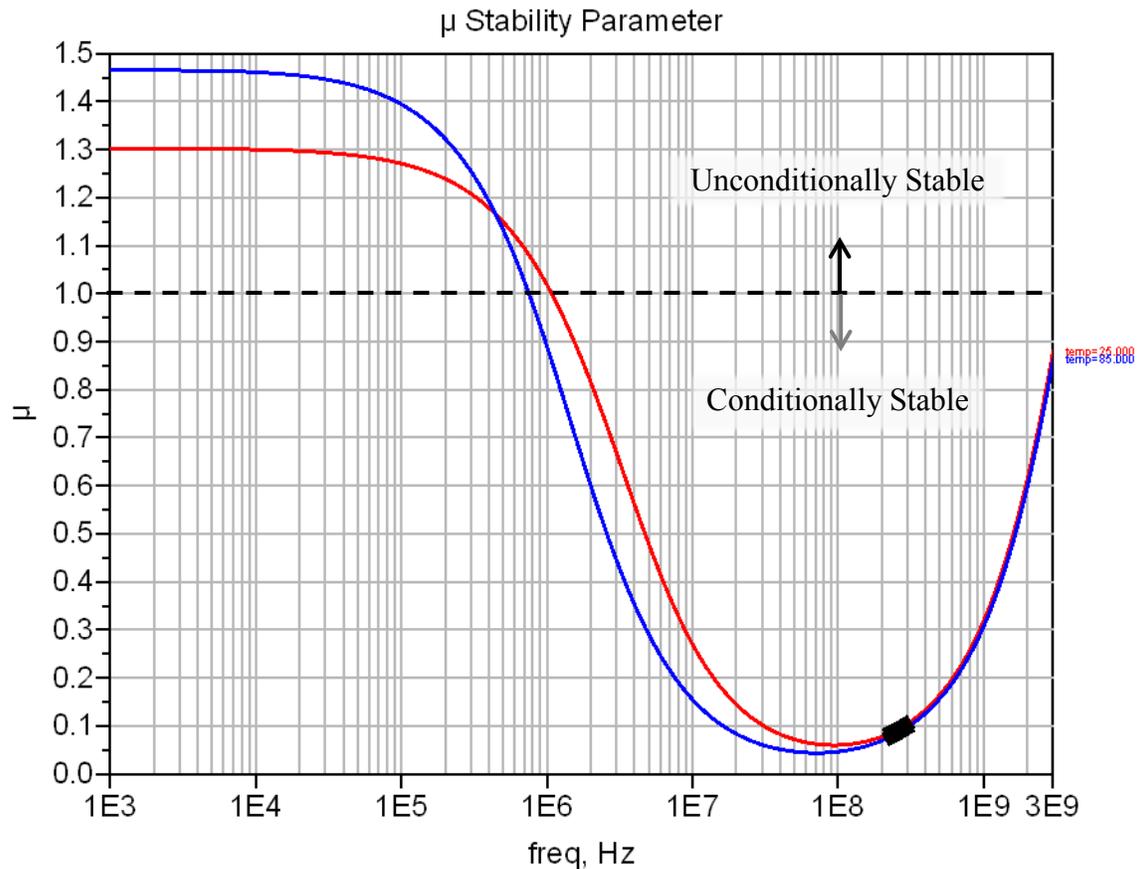


Figure 3.27: μ stability parameter of 0528-Q3 GaN HEMT model with the specified frequency band highlighted (black) [43] – [Simulation models utilized under the University License Program from Modelithics, Inc., Tampa, FL and TriQuint Semiconductor, Portland, Oregon]

Three stabilization techniques were considered: (i) inductive degeneration, (ii) series/shunt resistance on the gate and/or drain, and (iii) feedback. The reason the preferred inductive degeneration was not used is that it only created a narrow band where it stabilized the device unconditionally. Measurements showed that that topology was

actually unstable and oscillating under a large number of load conditions. In order to unconditionally stabilize the device over as wide a bandwidth as possible, the only two methods that yielded good results were a shunt resistance on the gate and feedback (the general technique is shown in Figure 3.28).

The values necessary to stabilize the device within the frequency band in each case were analyzed using output referred noise and ADS. The following derivations on the NF assume r_o to be large.

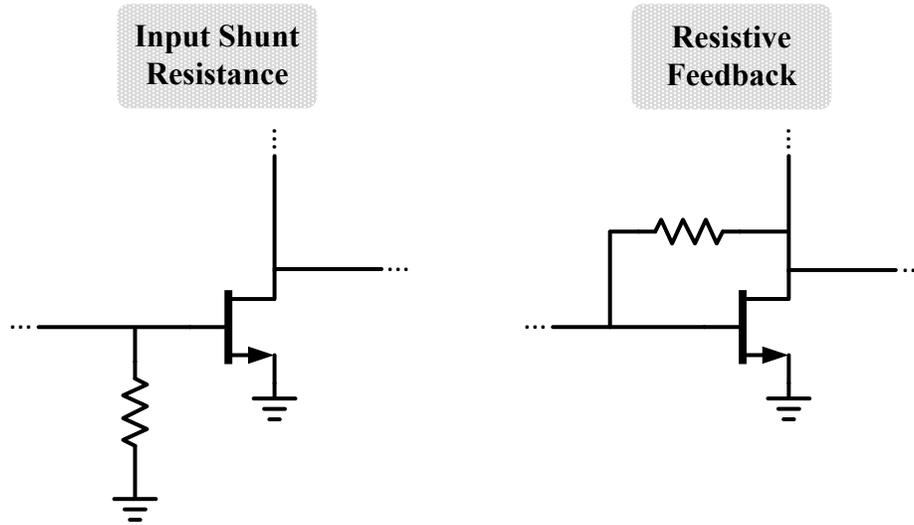


Figure 3.28: Basic stabilization techniques possible for wideband stability in this LNA.

For a shunt gate resistor

$$NF \approx 1 + \left(\frac{R_S}{R_{shunt}} \right) + \frac{\gamma R_S}{g_m (R_S \parallel R_{shunt})} \quad (3.23)$$

For a feedback resistor

$$NF \approx 1 + \frac{R_F}{R_S} \left(\frac{1 + g_m R_S}{1 - g_m R_F} \right)^2 + \frac{\gamma g_m}{R_S} \left(\frac{R_S + R_F}{1 - g_m R_F} \right)^2 \quad (3.24)$$

As the shunt required 50Ω or less, the noise contribution would be over 3dB increase in NF. For the feedback topology, estimation based on the transconductance from simulation ($g_m = 0.125$ S) and a moderate excess noise coefficient (since GaN exhibits low noise characteristics) of $\gamma = 1.2$, showed an increase of less than 1dB in NF with an R_F value of 500Ω . It was seen that the feedback could be unconditionally stabilized at just under $1k\Omega$, but some margin was sought. Using the room temperature values mentioned

above with the equations in section 2.2.2, gave theoretical values of 13.7dB for gain and 1.46dB for noise figure. Due to differences in actual impedances, transconductance, and noise coefficient, these values could shift by about 3dB in gain and 0.5dB in noise figure.

Additional stabilization was required for lower frequencies. To do this, resistive elements were placed in the feed lines behind the frequency dependent devices (i.e. RF chokes). The needed resistance on the drain side was $\sim 1\Omega$ which was assumed to be present through parasitics. On the gate side, a series 10Ω was needed.

Placing these in series with the inductors allows them to be present at low frequencies, when the inductor is acting as a short circuit, and to be “removed” at higher frequencies, when the inductor becomes an open circuit. It is important to do this so that the gain and NF is not compromised in the frequency band of interest.

After the addition of the 500Ω feedback resistor and 10Ω series resistor in the gate supply line, the μ stability parameter indicated an unconditionally stable LNA over all the test frequencies, as shown in Figure 3.29.

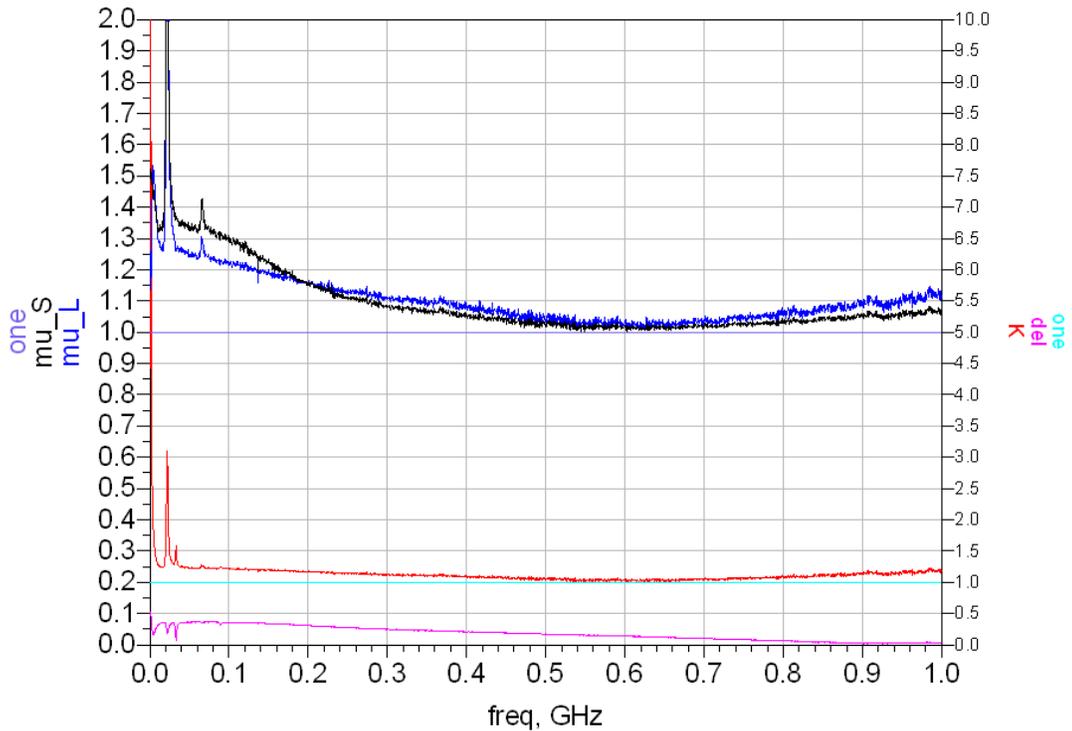


Figure 3.29: μ stability parameter of LNA without matching network.

3.11 Noise Characterization

As mentioned briefly in previous sections, the device chosen was intended and optimized for RF power applications. As the PA is typically the last stage in a transmit chain, the noise figure is often not a design factor for this stage based on the theory of Friis' equation.

In order to achieve a low NF in the LNA, some testing of the noise performance was needed. The device was biased and stabilized based on the selections discussed above and various source impedances were tested using a noise figure analyzer.

A single microstrip transmission line was printed using an LPKF Protomat S43 milling machine. The required effective half wavelength of the board was too large to fabricate, so three-fourths of a wavelength was used. On this board, three capacitors with SRFs high enough to be ignored were individually shunted at various locations on the board. This transmission line-capacitor filter allowed the impedance transformation of the 50Ω input to a number of points on the smith chart. The impedance seen at the input of the source-pull board was measured (in terms of the reflection coefficient, Γ_S) and software was used to embed the on-board transmission line (which was assumed to be a lossless microstrip transmission line). The NF was sequentially measured and attributed to the respective Γ_S . However, due to the required de-embedding of lossy filters needed to accurately display the NF on the analyzer, this method proved to be difficult and yielded questionable results.

Figure 3.30 shows the results for three tested frequencies: a trend can be seen in terms of improving and worsening NF; however, the error in the measurement is unclear and the presence of noise “circles” is not evident. This, alone, causes speculation about the accuracy of the measurement. The center frequency measurements are presented separately in Figure 3.31, for clarity.

Without the source-pull board, the presentation of a 50Ω source impedance yielded one of the lowest noise figures seen during testing, but also the flattest NF across the frequency band of interest. As the NF of this load condition was sufficiently low, the selection of this source loading was done for the prototype phase.

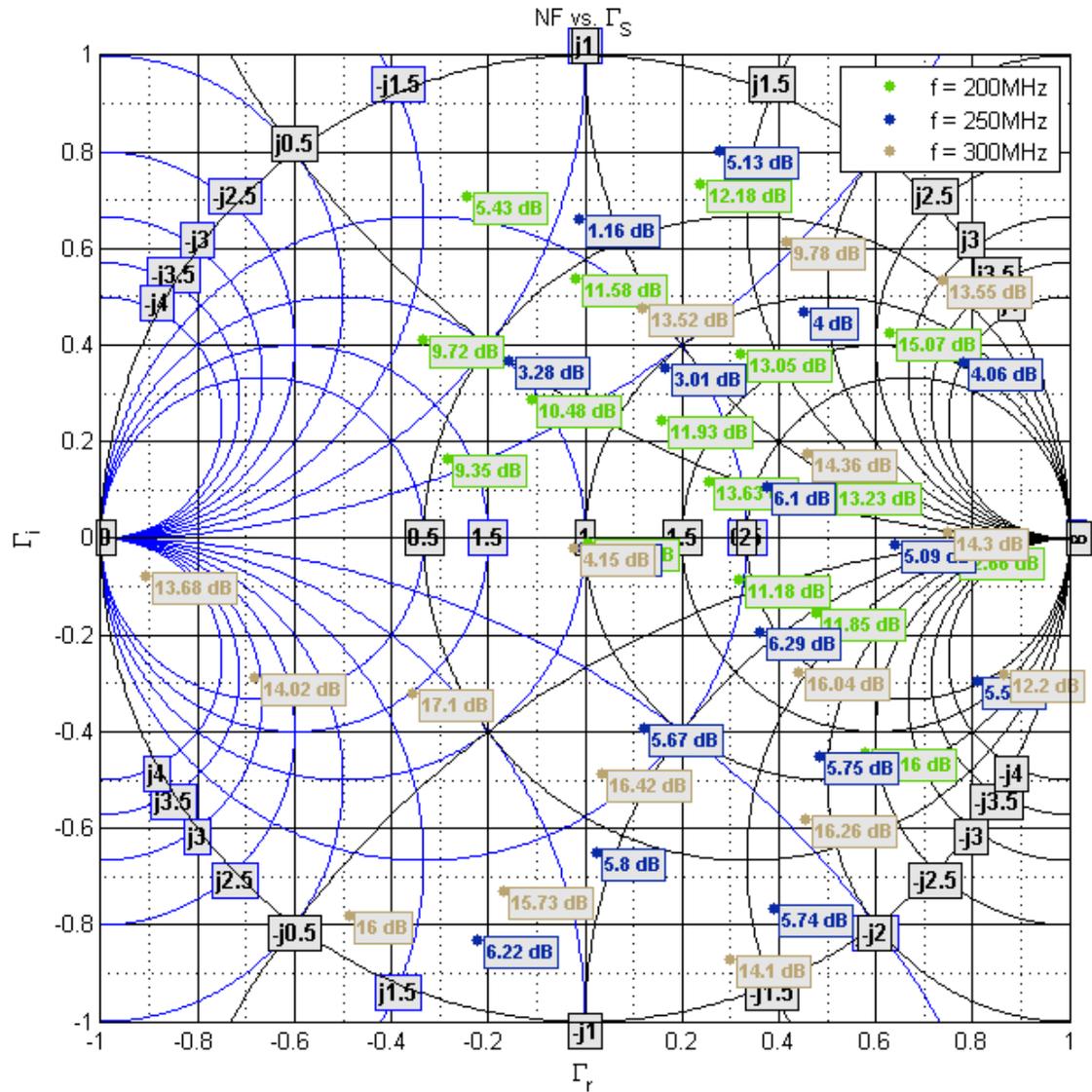


Figure 3.30: Measured NF mapped to the Γ_S -plane with hand-made source-pull technique

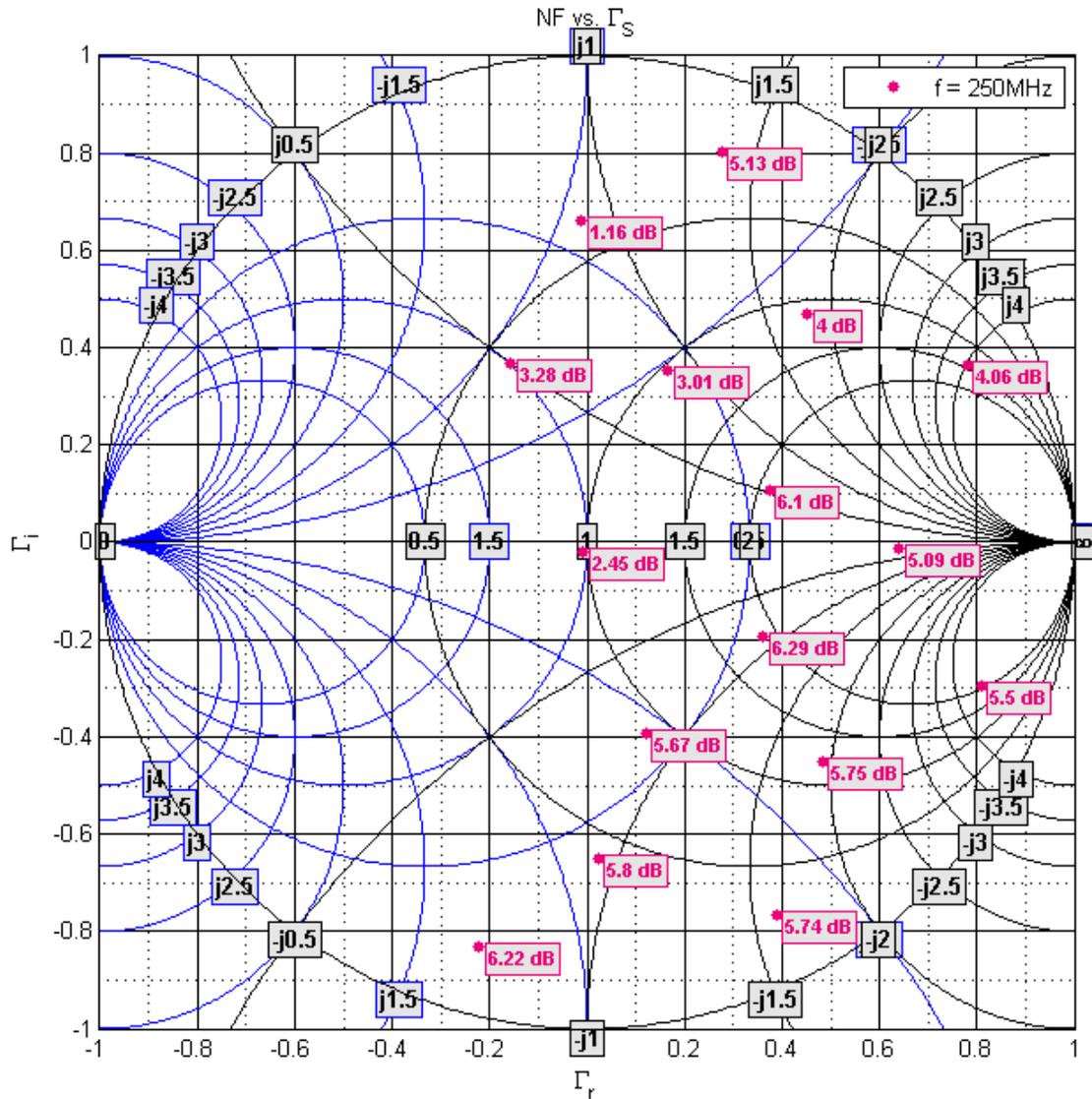


Figure 3.31: Measured NF mapped to the Γ_S -plane at 250MHz

Unfortunately, designing for minimum noise often requires a mismatch at the input, yet most microwave receivers need to have a matched input. To do this, NF is traded for the matching condition. Figure 3.32 shows the theoretical noise figure of the topology (equation 3.24) vs. the excess noise coefficient given the selected resistances for three cases: input matched with infinite output loading, input matched to a finite output loading, and the unmatched case used in this design. This design exploits the 50Ω source resistance mismatch case to yield lower noise figure.

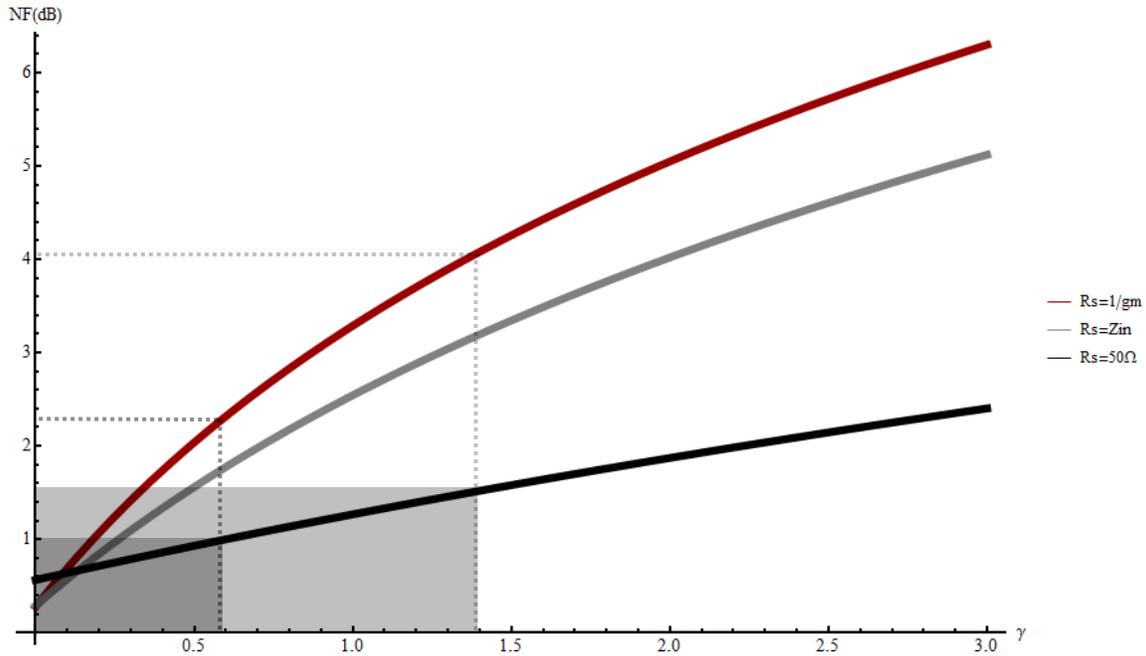


Figure 3.32: Theoretical NF of resistive feedback topology at 25°C.

Newer techniques use noise cancellation in the form of feedback and feedforward to effectively cancel noise present at the sensing port [13]. This typically can aid in reducing NF with the benefit of input matching and without sacrifice in performance (at the cost of complexity and total power consumption). As this work was a prototype for proof of concept, the complexity was designed to be kept as simple as possible in order to ensure reliable operation and aid in the true indication of single device performance.

3.12 Matching Networks

One of the last steps in the design process is the matching networks. These help present the intended load conditions over frequency to achieve a particular performance. The primary use of a matching network is to provide maximum power transfer between connections and present a fine-tune on the device bandwidth.

As discussed in the previous section, the selected source impedance was 50Ω. As the transmission line's characteristic impedance was also 50Ω, no matching network was required and the input line length was allowed to be any length considered lossless.

Since this LNA was designed for minimum noise (as determined from discrete measurements), the use of simultaneous conjugate matching was not employed. Very

rarely will the maximum available gain (MAG) and minimum noise figure (NF_{min}) coincide, requiring a mismatch at the input.

The output of the LNA was, however, conjugate matched to deliver the maximum power available from the two-port (i.e. LNA) to the load (i.e. next stage). The next stage is typically a filter or mixer, so a 50Ω load was considered. The network was designed in ADS using the smith chart tool (Figure 3.33). Open circuit stubs were favored in this design to allow for simpler tuning and reduce the effects of placing vias.

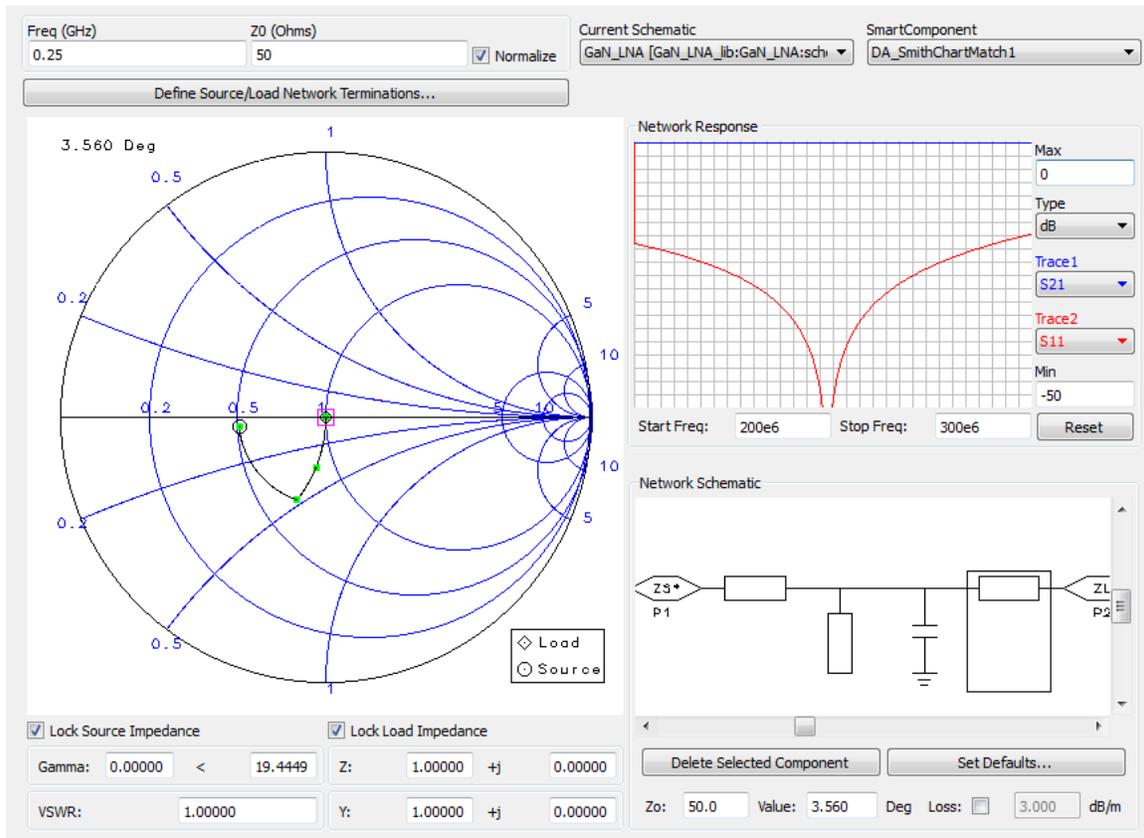


Figure 3.33: Output match design using a smith chart

The required open-circuit stub length to match the output was too long to fit on the LNA board (restricted by the heatsink dimensions). Therefore, a shunt capacitor was used in order to reduce the required stub line. Additionally, this allowed the stub to function as a fine tune on the capacitor value if needed.

3.13 Layout and Prototype

Once all of the design aspects were decided and measurements were taken on selected components, the EM simulation layout allowed an accurate representation of the performance to be expected. Because the frequencies of interest were considerable low, the onboard parasitics did not cause significant deviation from schematic simulations.

The simulation software also could not factor in the change in parasitic properties of the board material at high frequency despite the components having high temperature data incorporated. For this reason, the schematic simulation and EM/layout simulation were averaged in terms of expected operation. This was deemed appropriate due to the minimal differences between the two and the expected reduction of parasitic reactance in the board at high temperature. The board was also restricted by the heat sink dimensions (Figure 3.25 in section 3.8). The resulting layout can be seen in Figure 3.34 with the bill of materials (BOM) listed in Table 3.7.

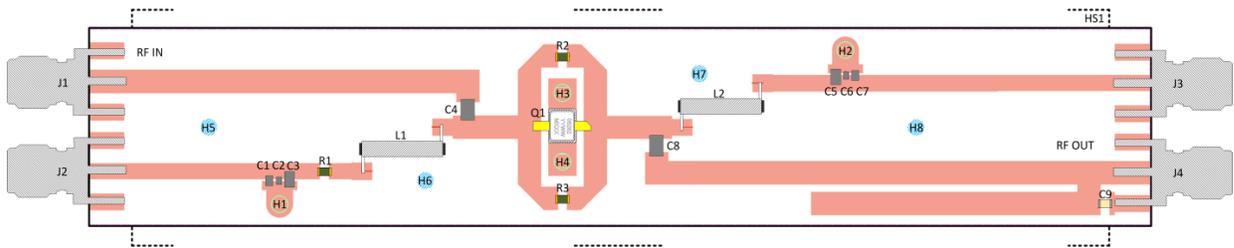


Figure 3.34: Layout of the proposed LNA

Table 3.7: Bill of Materials

Bill of Materials					
Reference	Value	Manufacturer	Function	Package	Part Number
C1, C5	100 pF	IPDiA	Bypass	0402	935.133.424.310
C2, C6	10 nF	IPDiA	Bypass	0201	935.133.423.510
C3, C7	0.1 μ F	IPDiA	Bypass	0805	935.133.426.610
C4, C8	1 μ F	IPDiA	DC Block	1206	935.133.427.710
C9	4.7 pF	Presidio	Matching	0805	HT0805NPO4R7C2P5
R1	10 Ω	Vishay	Stability	0805	PATT0805E10R0BGT1
R2, R3	1 k Ω	Vishay	Feedback/ Stability	0805	PATT0805E1001BGT1
L1, L2	1 μ H	Coilcraft	RF Choke	-	AT549RBT102MLZ
Q1	0528	TriQuint/Qorvo	Amplifier	Q3	T2G6000528-Q3
J1, J2, J3, J4	SMA	Cinch	Connector	SMA	142-0701-801
H1 – H8	Carbon Steel	Pololu	Screw/Nut	-	1957/1067
HS1	\sim 1 $^{\circ}$ C/W	Wakefield-Vette	Heatsink	-	423K
--	4003C	Rogers	Board	1oz	1ED/1ED, 60mil

The layout was exported via Gerber files to be printed with a milling machine (LPKF Protomat S43) accessed through the Center for Power Electronics Systems (CPES) lab at Virginia Tech. Once printed as accurately as possible with the machine, the board was populated with the selected devices with hot air and a high capacity soldering iron. The final design mounted to the select heatsink is shown in Figure 3.35.



Figure 3.35: Final design on a heat sink

3.14 Tuning

The measured performance was very close to the simulated performance; however, slight adjustments were needed in order to improve the design. Copper tape was used in the preliminary design to validate the matching network. This required tuning by means of cutting the open circuit stub to adjust the impedance of the stub.

In the final design, tuning by means of cleaning the circuit board and creating deeper trenches under small components helped to improve small variations and unintended leakage connections. Additionally, the bias was adjusted to fine tune the results to provide a near perfect match on the output at 250MHz and 230°C. Bias tuning was also used to exploit matching conditions of the LNA at each temperature, over temperature (see section 4.4.7).

Chapter 4

4 Experimental Results

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This chapter discusses the measured results obtained from the design discussed in chapter 3. The test instruments used to take measurements and the setup procedure followed are discussed first. Then concerns related to device from observations are discussed. Finally, the measured performance is detailed over temperature with graphs exhibiting actual data. The sections discuss observations seen in measurement and theories as to what causes the performance. The complete results are summarized in the final table.

4.1 Testing Instruments and Test Setup

4.1.1 Vector Network Analyzer (VNA)

A Rohde & Schwarz (R&S) ZVL13 VNA (9kHz – 13.6GHz) [59] was used to measure s-parameters and evaluate stability parameters (see Figure 4.1). The instrument provides two 50Ω ports, both of which deliver and receive signal power. The signals are fed through directional power splitters at each port and compared to the original signal for data analysis. With the measurement of each power wave, s_{11} , s_{12} , s_{21} , and s_{22} can all be obtained. Once known, the s-parameters alone can be used to calculate additional

information (such as stability) or can be mapped directly to the selected format (linear, log, smith chart, polar, impedance, admittance, etc.).

In order to take meaningful s-parameters, the settings were chosen by application. The frequency range was selected based on the measurement, often either between 1MHz and 1GHz or 200MHz to 300MHz (the approximate specified bandwidth) with 4001 points in each case. If the device was active (i.e. exhibiting gain) then the power output of the VNA was set to -30dBm; if the device was passive, then the power was set -10dBm. The resolution bandwidth was selected for medium speed (1kHz) as a tradeoff between accuracy and sweep time. The display was setup to show s_{11} , s_{12} , s_{21} , and s_{22} ; s_{11} and s_{22} were read on impedance smith charts and the others on dB-Linear scales.



Figure 4.1: R&S ZVL13 VNA [60] [fair use]

4.1.1.1 VNA Calibration

In order to use the VNA for precise measurements, the instrument needs to be calibrated to the desired reference plane to remove the additional interfaces (i.e. cables, adapters, the VNA itself, etc.)

A “Short, Open, Load, Thru” (SOLT) calibration was performed before measurements were taken using the end of the cables that would be connected to the PCB as the reference plane. A Maury Microwave 3.5mm calibration kit (8050CK11 [61]) was used for all VNA calibrations.

4.1.1.2 VNA De-embedding

During initial component tests, the calibration plane needed to be extended to the device terminations for accurate measurement as shown in Figure 4.2. This required de-

embedding of the board which is also incorporated in the VNA software. The selected method of de-embedding was through port-extension. This feature takes information regarding the effective relative permittivity, length of the line, and loss information to de-embed the lines. There also exists a feature that will automatically determine the port extension (with the DUT removed from the board) using minimum group delay as target. Both methods were used for any necessary de-embedding with aggregable results.

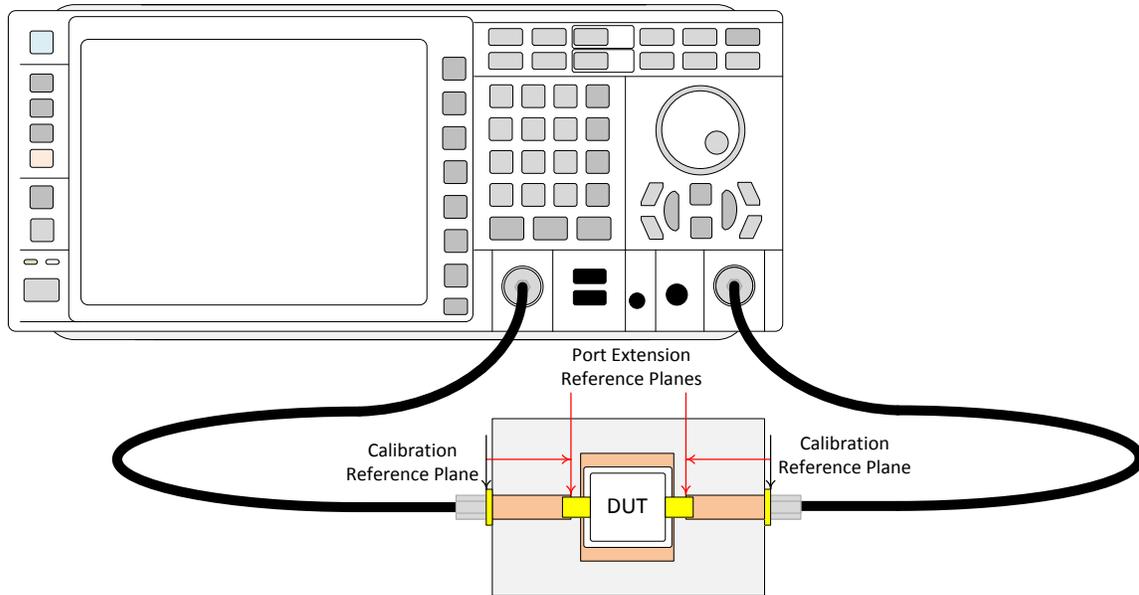


Figure 4.2: De-embedding with port extension.

4.1.2 Noise Figure Analyzer (NFA)

A Keysight (Agilent) N8973A NFA (10MHz – 3GHz) [62] was used to measure the noise figure of the LNA (see Figure 4.3). The instrument provides a noise source drive output (at the standard 28V) and one 50Ω input port. The noise source is connected to the 28V drive which generates a measurable amount of noise that is specified on the noise source case and calibration sheet. A Keysight (Agilent) 346C 15dB excess noise ratio (ENR) noise source was used [63]. In operation, the NFA pulses the 28V drive and measures the difference in output power between the “hot” (i.e. powered noise source) and “cold” (i.e. noise source off) conditions. Using some mathematical formulas and given the ENR of the noise source, the Y-factor is calculated. Using the Y-factor the NF, noise temperature, and gain can be derived and displayed on the screen. [64] is an application note that covers the theory and math for the above process. All measurements

taken make use of calibration, Keysight ENR tables, and appropriate loss compensation for cables and adapters used to interface the DUT.

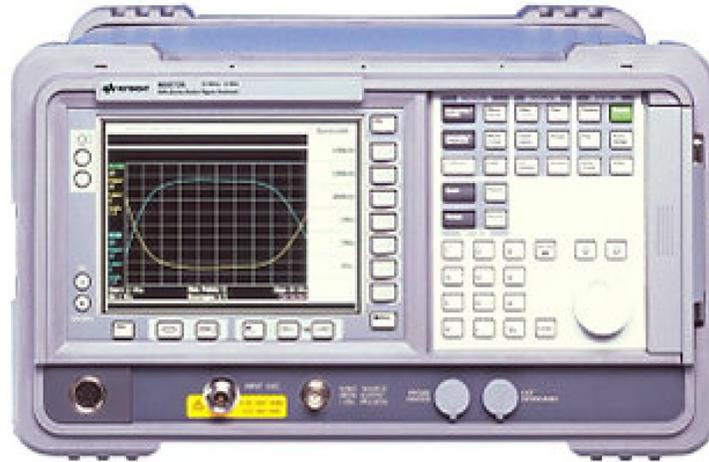


Figure 4.3: Keysight N8973A NFA [65] [fair use]

4.1.2.1 NFA Calibration

In order to use the NFA for precise measurements, the instrument needs to be calibrated to remove contributing factors that are not part of the DUT (i.e. cables, adapters, the NFA itself, etc.)

The calibration procedure involves connecting the noise source to the input of the NFA. Any cables that come after the amplifying section of the DUT can also be added into the calibration path. Several attenuation pads are selected for any ranging that takes place. Additionally, the frequency span, number of points, measurement type (amplifier, downconversion, etc.), filter bandwidth, and ENR table values must be specified prior to calibration. The NFA runs calibration with each pad and stores the information. During measurement, the NFA will apply a second stage correction using Friis' equation to remove the additional effects measured and entered in the loss compensation dialog.

4.1.2.2 NFA Loss Compensation

For additional devices or interface materials that are not included in the calibration path (i.e. anything before the DUT), the NFA has a dialog to enter in the loss for correction. The location is specified as Before DUT or After DUT, the loss is entered, and the temperature is entered. Using this information in conjunction with Friis' equation

and the calibration data, the measured NF can be corrected to yield the DUT contributions alone.

One downfall of this particular model is the lack of a loss compensation table. The loss compensation is taken for all frequencies, so any additional losses that are not considered constant over the measurement bandwidth will result in incorrect corrections.

4.1.3 Signal Generator

A Keysight (HP) E4411B Spectrum Analyzer with 50 Ω tracking generator option (9kHz – 1.5GHz) [66], a Keysight (Agilent) E8257D PSG Analog Signal Generator with High Output Power option (100kHz – 20GHz) [67], and a R&S SMB100A-B112 Vector Signal Generator (100kHz – 12.75GHz) [68] were used to test the linearity (compression and two-tone tests) of the LNA (see Figure 4.4). These instruments provide a clean signal from a 50 Ω port that is injected into the input of the LNA with the output analyzed on a spectrum analyzer. The SMB100A and E8257S generators were capable of outputting over 20dBm of power and were used for compression testing while the E4411B was used with one of the other generators for two-tone tests. Once the auto calibration (internal) was run for each instrument, the desired settings were entered for frequency and power; no further setup was required.



Figure 4.4: (left to right) E4411B [69], E8257D [70], and SMB100A [71] signal generators [fair use]

4.1.4 Spectrum Analyzer (SA)

An Anritsu MS2665C Spectrum Analyzer (9kHz – 21.2GHz) with the narrow resolution bandwidth option [72] was used for all spectrum analysis (see Figure 4.5). The SA offered a versatile range of resolution bandwidths (RBW) and video bandwidths (VBW) for accurate measurements. The SA also required no more calibration than running the internal factory calibration. Once completed, the desired frequency band, RBW, VBW, and display settings were set. A 9dB attenuator was also used on the input to protect the SA from large output signals. This value was compensated in the

instrument's reference level offset. The output of the DUT was connected to the input of the attenuator.

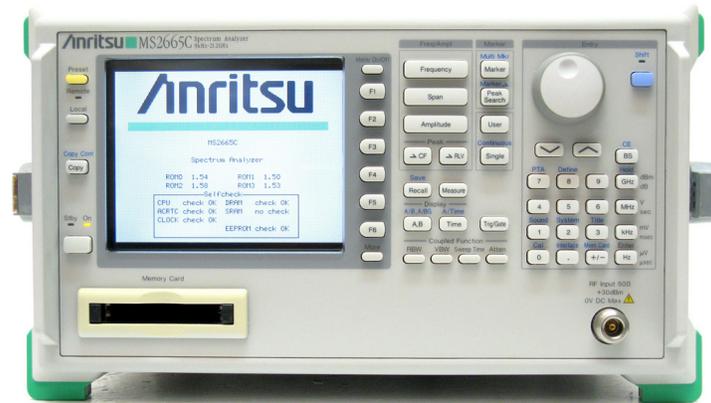


Figure 4.5: Anritsu MS2665C Spectrum Analyzer [73] [fair use]

4.1.5 Temperature Chamber

A Yamato DX302C Constant Temperature Drying Oven (+5°C – 300°C) [74] was used for high temperature measurements (see Figure 4.6). This oven could achieve the maximum temperature within 45 minutes with a $\pm 10^{\circ}\text{C}$ variation in the chamber under the influence of natural convection. No calibration was required. The device was placed in the oven and connected by cables through the vents on the top, the door was closed, the temperature was set, and the oven was run while monitoring measurements.



Figure 4.6: Yamato DX302C Natural Convection Oven [75] [fair use]

4.1.6 Programmable DC Supply

A Rigol DP832A Programmable Power Supply [76] was used to provide stable biasing (see Figure 4.7). This supply has three outputs, two capable of 30V, one capable of 5V, and all three capable of 3A. When a negative voltage was required, the connection was simply reversed in polarity. Channel two and three are not isolated, so the polarities of the connection had to remain the same when sharing a ground plane. The display allowed for easy monitoring of voltage, current, and power.

No calibrations were required, but over-voltage and over-current protection as well as voltage and current limits were set during testing to prevent damage to the devices.



Figure 4.7: Rigol DP832A Power Supply [77] [fair use]

4.1.7 Test Connections

Cables were assembled with connectors using the high temperature solder to ensure that the cable would remain connected at high temperature. Using these cables, the aforementioned instruments were connected in the necessary configuration.

When performing high temperature measurements, a high temperature cable was needed between each instrument and the board. Several feet of cable was used to provide enough length to reach into the oven. Figure 4.8 shows the connection and routing for testing in the oven.

All the RF instruments required type-N to SMA adapters so that the SMA cables that were made could connect. For the power supply, banana jacks with female BNC connectors were fitted with male BNC to female SMA adapters. The board itself was fitted with SMA connectors to avoid the need for additional adapters within the temperature chamber.

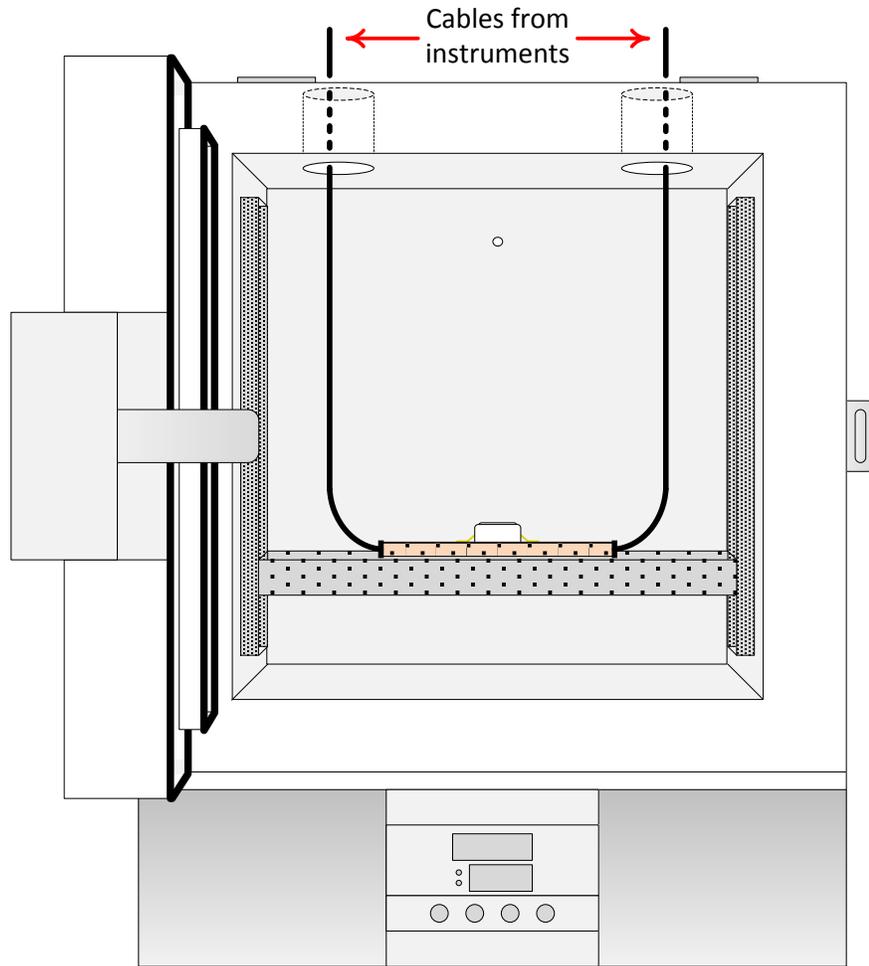


Figure 4.8: High temperature cable setup for oven use.

4.2 Test Procedure

4.2.1 Device Characterization

To validate the device datasheets and characterize each part over the desired temperature range, a simple testing procedure was completed.

A PCB of a single transmission line was made with a gap in the center (laid out using the suggested land pattern from the data sheet) for placing the device of interest. The device was soldering to the board using the high temperature solder and SMA end launch connectors were soldered to the ends. Figure 4.9 shows the basic layout.

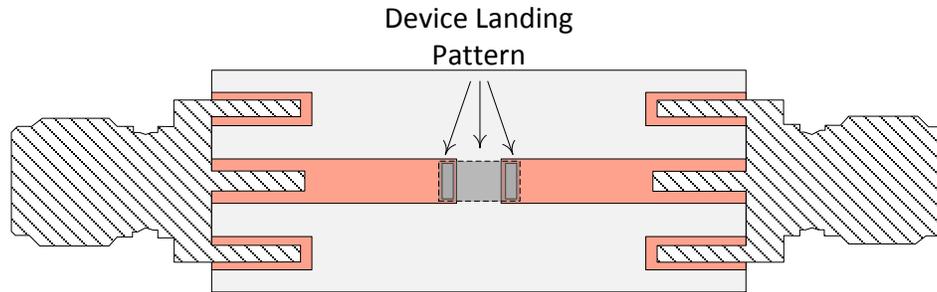


Figure 4.9: Board layout for device characterization.

Once assembled, the board was de-embedded using port extensions (see 4.1.1.2) using the VNA and the s-parameters were taken over a wide span of 1MHz to 1GHz with 4001 points of data. For several components, a wider span was taken (up to 4GHz) at 25°C for investigation into stability at higher frequencies. However, once analyzed, this frequency range was not needed for 230°C characterization.

It should be noted that 1MHz was selected as the lower bound so that the s-parameter data could be extrapolated (using cubic-spline algorithms) down to DC. The selection of the lower frequency should be below the skin effect transition frequency [78], [79],[80] of the board (about 3.5MHz for copper) in order to get a fairly accurate extrapolation.

4.2.2 S-parameters

To take s-parameters, the VNA was setup as described in section 4.1.1. Following the VNA setup and calibration, the DUT was connected to the VNA and powered (if necessary). If the device was being characterized, port extensions were applied. Additionally, port extensions were used on the LNA to de-embed the input and output lines for all tests prior to the design and inclusion of the matching networks; for final design measurements, no port extensions were needed. Once the VNA displayed the s-parameters as intended and points were analyzed, the data was exported via a *.s2p file for use in ADS simulations. This same test was done at several temperatures using the drying oven. The results of the test were compiled into one measurement data interchange format (or MDIF) file for simulation.

4.2.3 Stability

Stability was only measured for configurations including an active device; it was assumed that all passive devices were intrinsically stable. To evaluate the stability using

stability parameters, the VNA was setup as described in section 4.1.1. Following the VNA setup and calibration, the DUT was connected to the VNA and powered. Port extensions were used on the LNA to de-embed the input and output lines for all tests prior to the design and inclusion of the matching networks. A stability parameter was selected to be displayed. The VNA offers the Rollett stability factor and four forms of the μ stability parameter. As the μ parameter only requires one test for unconditional stability, it was selected as the measurement. For validation, both the μ and μ' factor with port one as the source were displayed.

The information shown in this test is also obtainable through simulation with the s-parameters; however, analysis on the VNA allowed for immediate adjustments to reconcile the lack of unconditional stability by slightly changing the bias or modifying the board to accommodate the variance.

4.2.4 Noise Figure

To measure the noise figure, the NFA was setup as described in section 4.1.1. The frequency range selected was only that of interest (200MHz – 300MHz). The number of average points was set to be 64 and the largest IF bandwidth was selected (4MHz) in order to have reduced jitter for a better noise estimation [81]. Following the NFA setup, calibration, and loss compensation, the DUT was connected to the NFA and biased. Once the data points for the entire band were display, minor adjustments were made for improvement by reducing crosstalk between cables and ensuring tight connections. The final data was then exported via a *.csv file and imported into Microsoft Excel.

4.2.5 1-dB Compression

The test procedure to measure the compression requires a single signal generator capable of high output power (>10dBm) and one spectrum analyzer. The high output power signal generator and spectrum analyzer were initialized as described in sections 4.1.3 and 4.1.4. The signal generator frequency was set to the approximate center of the band (250MHz). The compression was also tested at 200MHz and 300MHz to verify the performance at the ends of the frequency band.

The loss of the cables going from the signal generator to the LNA and going from the LNA to the SA were measured at the test frequency. These loss values are to be used to mathematically compensate the observed input power level (i.e. the displayed signal

generator output) and the observed output power level (i.e. the value read on the SA) using an Excel worksheet. The input power was increased in steps of 2dBm starting roughly 10 – 20dBm below the first noticeable sign of compression. With an Excel worksheet to calculate the compression level as the values are entered, the power should be increased until 3dB gain compression (determined by linear extrapolation from the linear gain region). The calculations are discussed in section 2.1.4.

4.2.6 Two-tone Tests (IP3 and IP2)

The test procedure to measure the compression requires two signal generators (or one with a dual output) and one spectrum analyzer. The signal generators and spectrum analyzer were initialized as described in sections 4.1.3 and 4.1.4. Since the LNA is wideband, the signal generators' frequencies were set close enough to be read on the SA at $\pm 10\text{MHz}$ tones around the center frequency which was set to the approximate center of the band (250MHz). The IP3 and IP2 were also tested at 200MHz and 300MHz to verify the performance at the ends of the frequency band. This selection of tone offset would create third-order tones $\pm 30\text{MHz}$ away from the center frequency. Although this is far away, they are still in the 3dB bandwidth of the LNA.

The loss of the cables going from the signal generators to the LNA were measured at the test frequencies selected. However, the loss of the cable going from the LNA to the SA had to be measured at all frequencies being recorded; these frequencies are the two test frequencies ($f_0 \pm 10\text{MHz}$), the third-order tones ($f_0 \pm 30\text{MHz}$), and the dominant second order tone ($2f_0$). These loss values are to be used to mathematically compensate the observed input power level (i.e. the displayed signal generator output) and the observed output power levels (i.e. values read on the SA) using an Excel worksheet. The input powers should be low enough to not cause any compression themselves. This value is generally the s-parameter power level of -30dBm. The power levels at the desired frequencies were recorded in an Excel worksheet setup to correct the actual power levels at the input and output ports of the LNA. The OIP3 and OIP2 were calculated using the equations in section 2.1.5.

4.3 Reliability

Prior to the discussion of the measurement results, a brief discussion of some reliability concerns are listed based both on observations and existing research.

4.3.1 Limitations of Passive Components

Although the GaN device has a theoretical lifetime of 36 years at a junction temperature of 240°C [44] (calculated using (4.1) with the derived thermal resistance and dissipated power, neglecting RF power), the passive devices reliability is not provided which compromises the reliability.

$$T_{J(230^{\circ}\text{C})} = (P_D)(R_{\theta JA}) + T_A \approx (0.24\text{W})(25.4^{\circ}\text{C/W}) + 230^{\circ}\text{C} = 236^{\circ}\text{C} \quad (4.1)$$

Additionally, the GaN HEMT has the capability of being used at higher temperature even into the ultra-HPHT environments; however, all of the passive devices have a maximum rated operating temperature of 250°C. It is surmised that the devices could function without degradation at least 10°C higher, but this was not tested. Another concern is that the current would increase requiring a re-evaluation of the power limits, which, if exceeding, greatly affects the reliability.

4.3.2 Drifting Gate Voltage

During testing, it was observed that the necessary gate voltage to obtain the drain bias current was rarely the same after a temperature cycle. Although the device performed the same at any given (I_D , V_{DD}) bias condition; this factor is concerning in regards to reliability.

Also, during startup of the circuit (at 25°C), it took a few minutes to settle into a stable current operation, requiring adjustments to the bias voltage as the current drifted off the desired point. Again, this variance questions the reliability of the device and provokes the need to further investigate this effect.

4.3.3 Reliability of GaN Devices

The reliability of GaN HEMTs have been investigated in [6]. The primary cause for short-term failure and degradation has to do with having high gate leakage current to begin with. This coupled with small current collapse ratio (due to interface traps and intentional traps that help the leakage current problem, such as Fe doping [82]).

Additionally, long term reliability seemed to also be affected by traps, specifically deep level traps in the buffer layer of the HEMT.

It seems that the reliability is strongly linked to gate leakage and undesirable deep level traps near the current paths. This means that the performance and reliability of the GaN device is heavily subjected to the fabrication processes and screening done by the manufacturer.

4.3.4 Continuous Performance

Contrary to the above concerns, there is reason to believe that the device is indeed stable, although sensitive to some minor factors previously discussed. The final design has operated with the same characteristics (when set at a specific I_D , V_{DD} bias condition) while at 230°C for an appreciable number of hours and has endured numerous temperature cycles during testing. This continuous performance gives reason to consider the device reliable when controlled to operate in the specified bias condition. Minor shifts may be observed, but the error seen is often within 1% degradation.

However, despite the continuous performance seen over these multitudes of test, no long-term stress test was run. From observations, the LNA has been observed to work at 230°C for over two continuous hours with zero degradation in performance.

4.4 Measurement Results

The final measurement results of the LNA are discussed in the remaining sections. The data was taken for several temperatures (all data was taken at 25°C and 230°C, some at intermediate temperature) and with high resolution where possible to provide the most insight in the LNA. The full summary of the results is presented in a table in section .

4.4.1 Stability

Figure 4.10 shows the load stability parameter, μ , of the final LNA design over the band of interest for six temperatures from 25°C to 230°C. Also, despite that this test requires no auxiliary tests for validation, the complimentary source stability parameter, μ' , is provided in Figure 4.11.

Both measurements show that the LNA is unconditionally stable at all temperature over this frequency range. Additionally, the μ parameters indicate that the unconditional stability is not only safely far from conditional stability (>1.1), but that the proneness to

instability decreased with increasing temperature. This attribute is believed to be a function of the stabilization technique, selected bias condition, and change in device properties with temperature.

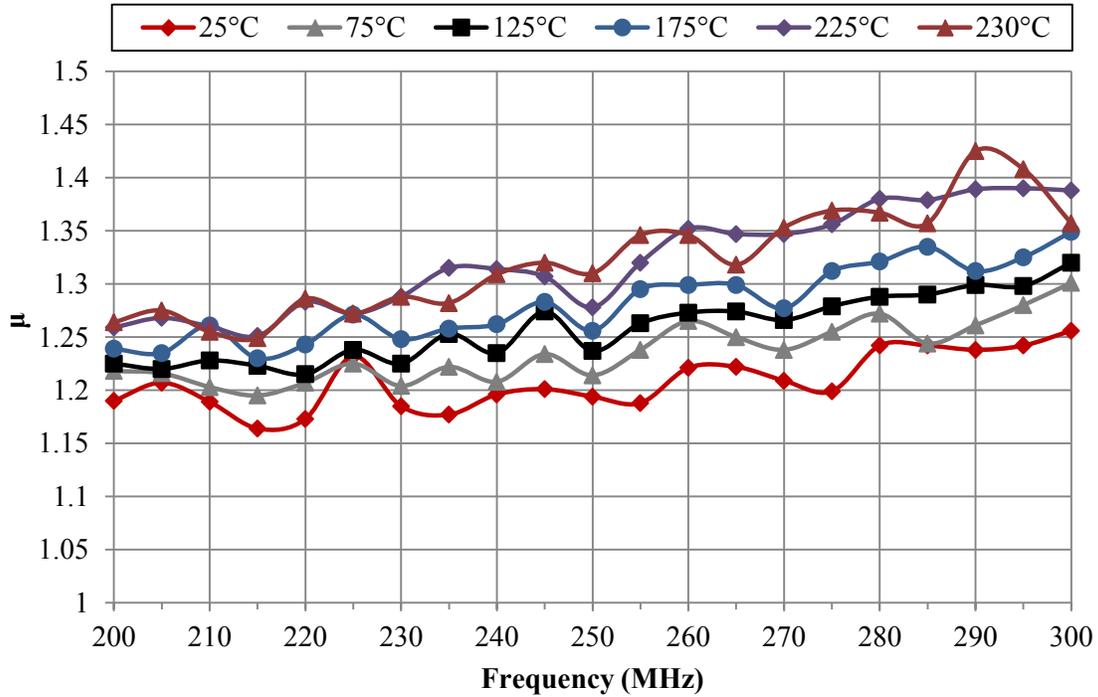


Figure 4.10: μ stability parameter vs. frequency vs. temperature

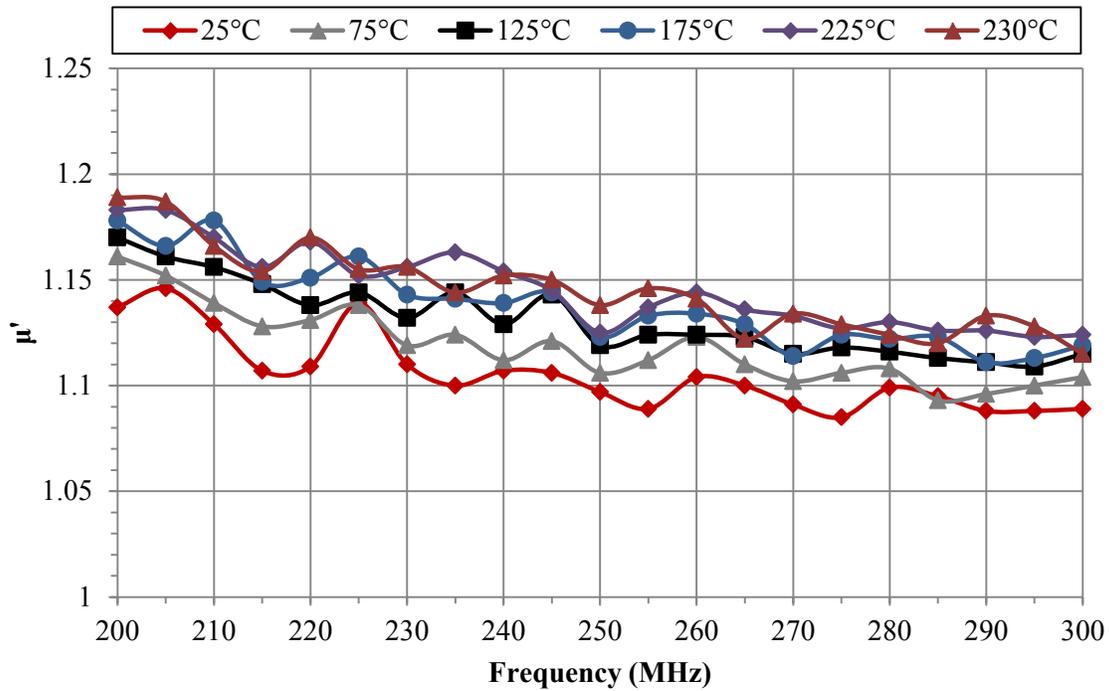


Figure 4.11: μ' stability parameter vs. frequency vs. temperature

4.4.2 S-parameters

Once the device is stable, the most revealing aspects of the performance are embedded in the device s-parameters. Figures 4.12, 4.13, 4.14, and 4.15 display the measured results of the forward gain, output return loss, input return loss, and reverse transmission, respectively, for six temperature ranges from 25°C to 230°C.

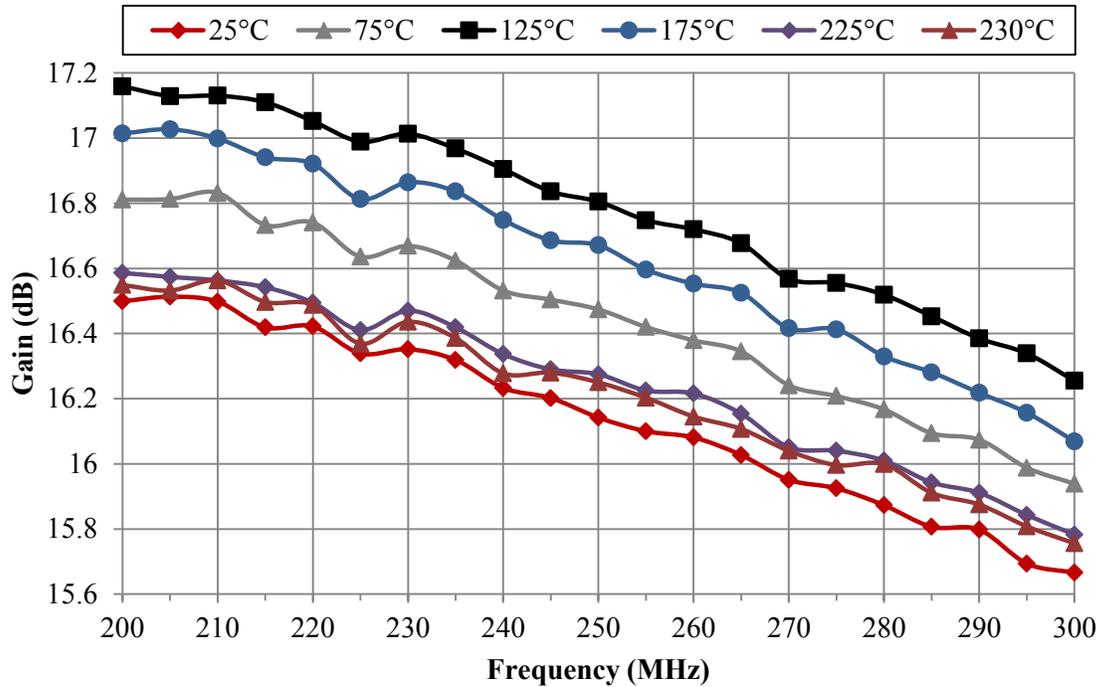


Figure 4.12: Forward gain

As discussed earlier (section 3.6), the device bias was selected to exploit a temperature-independent gain. The midband gain (and the average gain) was measured to be 16.2dB at 230°C. However; due to process variations, interactions with the board, and minor adjustments in the biasing; a small variation having a maximum of 0.69dB shift in gain can be seen over the temperature range.

It should also be noted, though, that the 25°C/230°C difference is very minimal (<0.13dB), but that the performance variation peaks around 125°C. This happens primarily due to the overlapping of improving matching conditions and the small drop in gain. That is; before this temperature, the gain is high and the match is good; but after this temperature, the gain is moderate and the match is great.

The LNA was not matched to be narrowband, nor was the gain shaped for any particular response. Due to this design feature, the gain does not exhibit a peak at the center frequency. Instead, it follows the natural amplification profile of the device (which is only slightly degraded from its open loop performance for stabilization and parasitics of the board layout). This lack of gain-profile-shaping degrades the total variation with

frequency; however, the 230.5MHz – 285.0MHz gain variation is only approximately $0.87\text{dB} \pm 0.08\text{dB}$ over the measured temperature range.

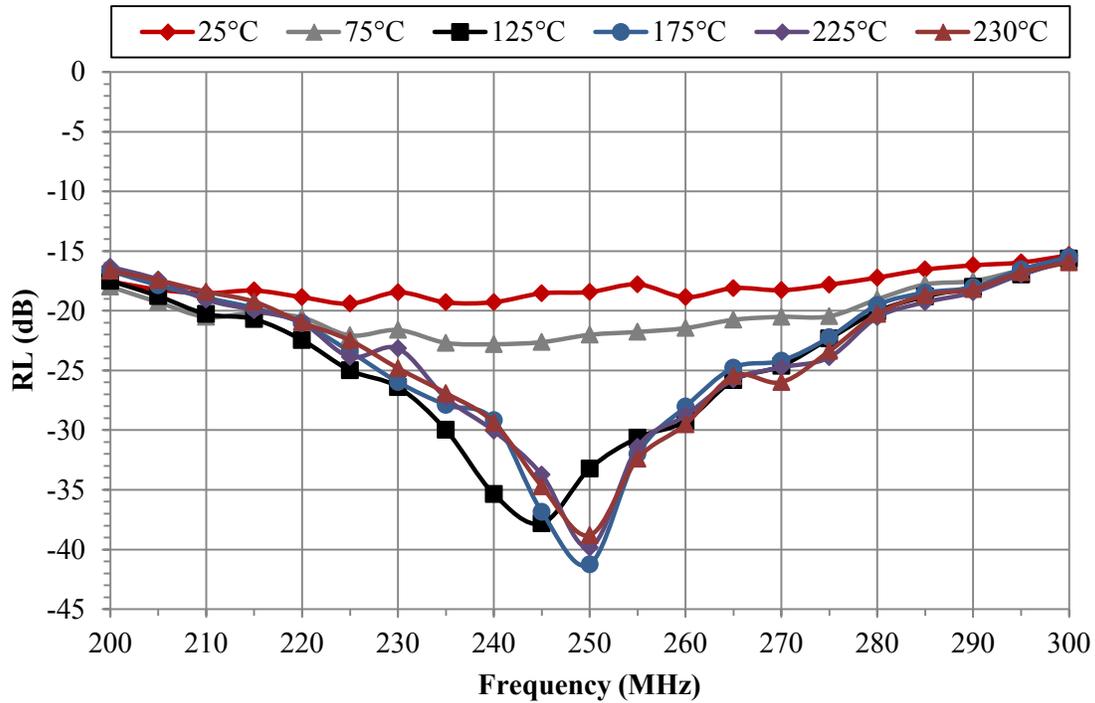


Figure 4.13: Output return loss

The output return loss shown (ORL) in Figure 4.13 is for the 230°C output match bias condition (i.e. the bias wasn't adjusted to maintain a match over temperature). The measured results indicate a very good return loss of $>15\text{dB}$ across all temperatures in the frequency band of interest. As expected with a temperature specified optimization, the matching improves with temperature as the output impedance drifts closer to the matched case over temperature. The smith chart plotting of this data is shown in Figure 4.16.

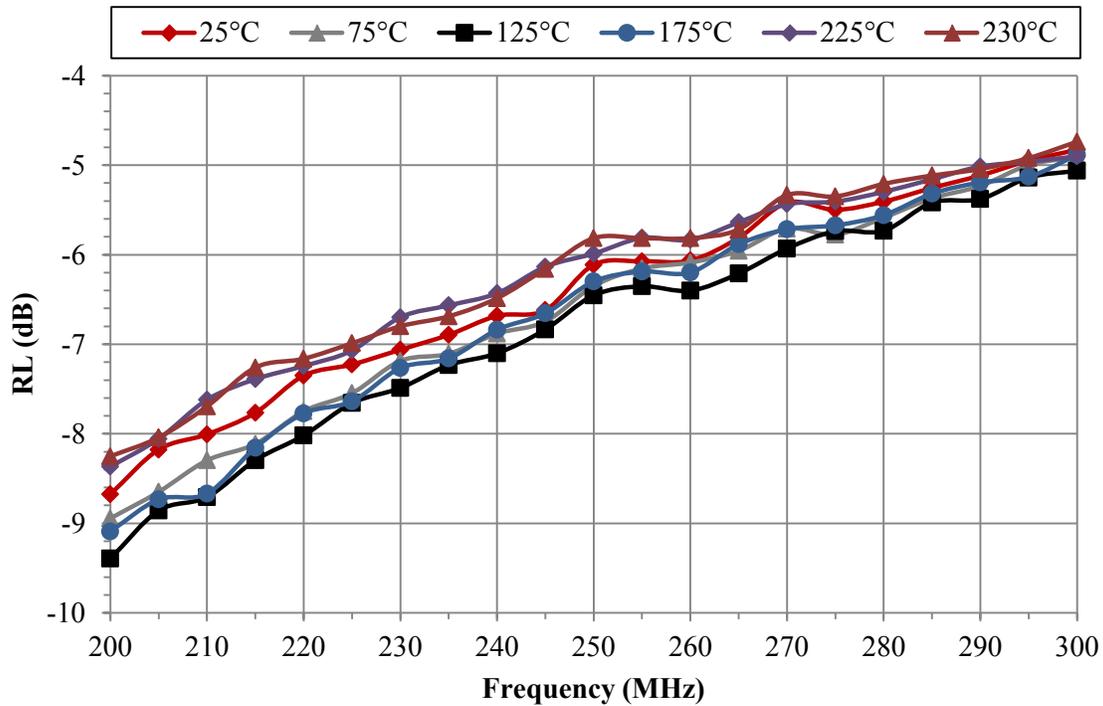


Figure 4.14: Input return loss

Since this LNA was designed for a better noise performance, the input return loss (IRL) was expected to be degraded. Because of this, the receiver must be able to withstand significantly non-ideal voltage standing wave ratios (VSWRs). This particular device didn't require a serious mismatch on the input to improve noise with an IRL >5dB for all temperatures over the frequency band. As can be seen, the IRL improved with lower frequency.

At the worst case IRL of 5dB, this presents a VSWR of 1.92 which is only 10% power loss. This is considered acceptable, especially since the source impedance should be relatively fixed in most high temperature applications at the present time (i.e. not wireless).

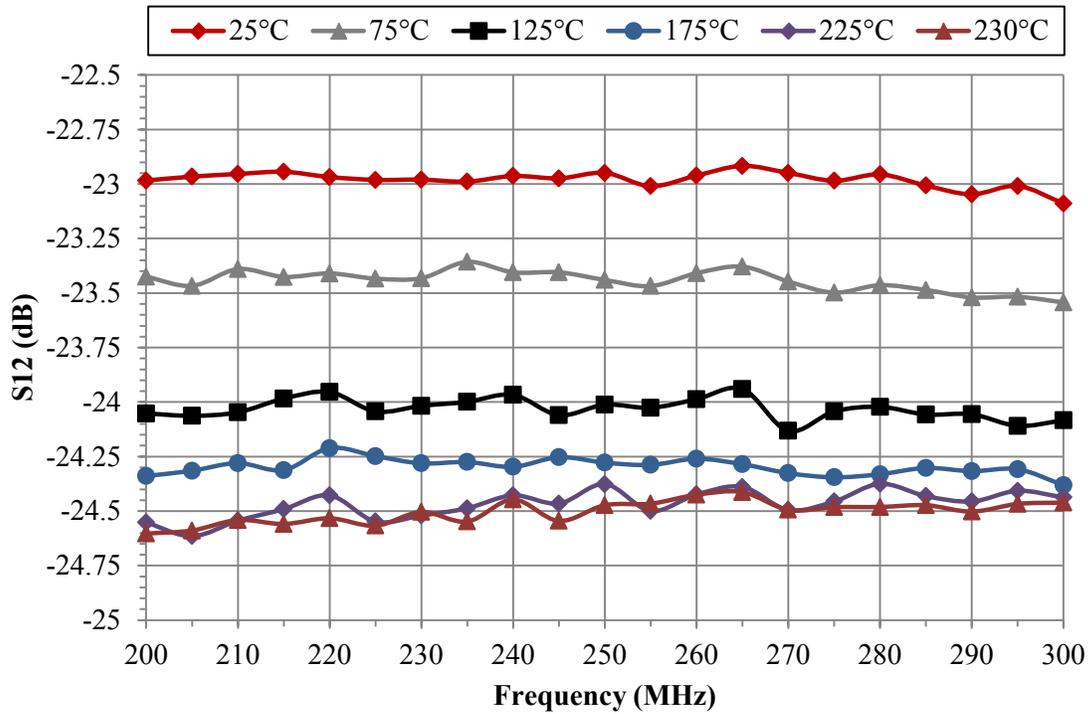


Figure 4.15: Reverse transmission

The last s-parameter to check is the reverse transmission. This is important so that reflected and spurious signals do not make their way back to the input where they can cause nonlinearities and unexpected variations in performance.

The measured reverse isolation was seen to be approximately 23 – 24.5dB over the temperature and fairly constant over the frequency band at each temperature. This should be significantly high enough to suppress any signal generated by the LNA itself to more than 6dB below the input and also mitigate high power spurs so that the input signal is not desensitized.

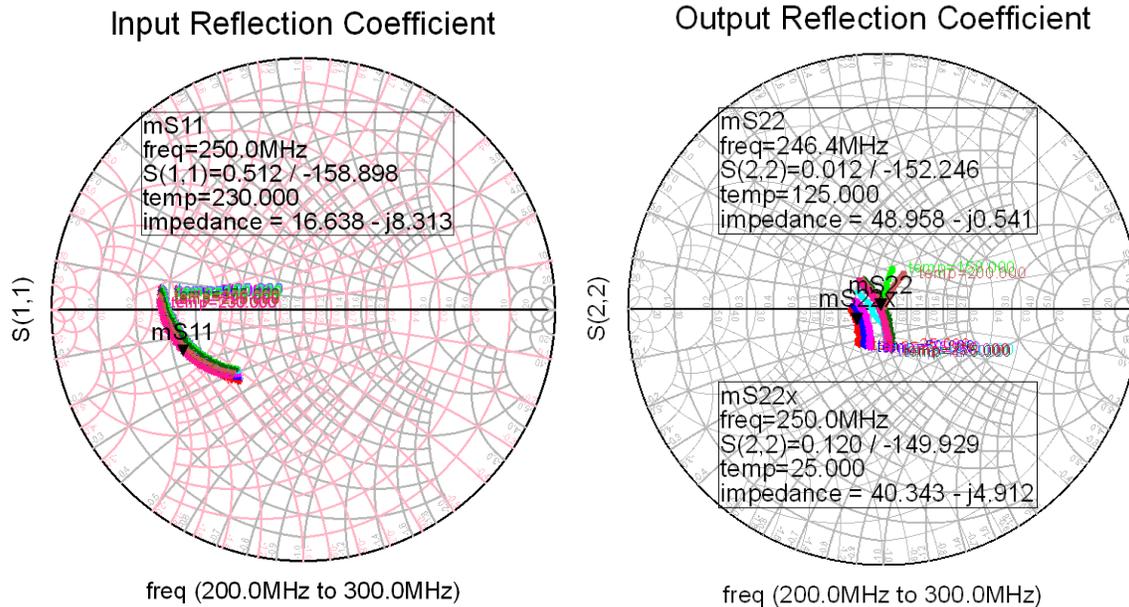


Figure 4.16: S_{11} and S_{22} mapped to the Smith Chart

Figure 4.16 is presented so show the smith chart mappings of the return losses (this incorporates impedance information).

4.4.3 Noise Figure

Another important test is the noise figure of the LNA. As mentioned in section 2.1.3, the front end amplifier has the important role of mitigating the noise contributions of the later stages. Because of this, it is paramount that the LNA has as low of a NF as possible.

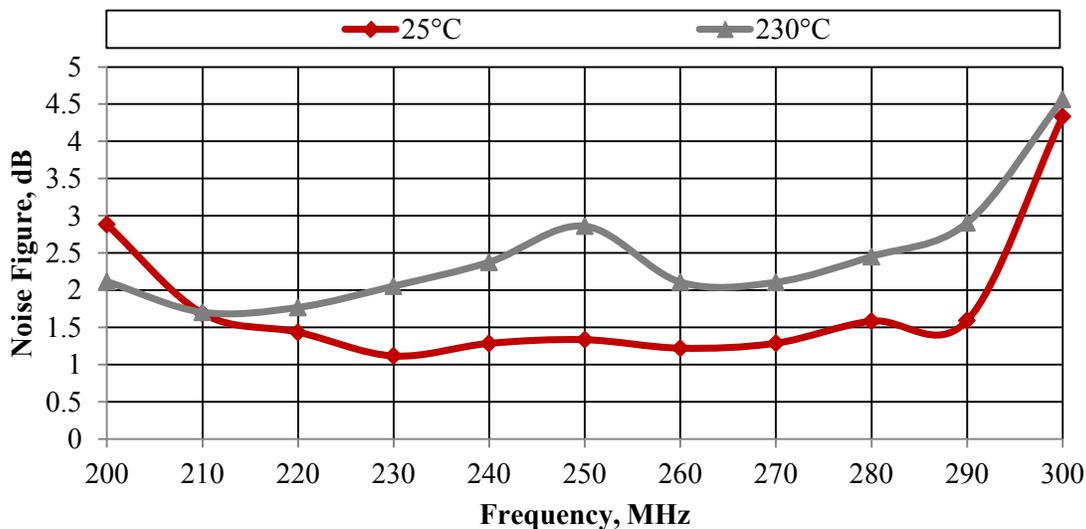


Figure 4.17: Noise figure vs. temperature

Data was only recorded at 25°C and 230°C, but it was observed during the heating cycle. For intermediate temperatures, the NF increased fairly linearly from the 25°C condition to the 230°C condition.

The large variations in the NF are due to the noise spurs cause by the assembly of the board. Lacking a preamplifier made this an issue that had to be endured; however, care was taken to reduce these spurious noise currents during measurement (it can be seen that this was done better for the 25°C test).

If the measurements are taken as de facto performance, the NF only degraded by approximately 1.5dB over the 205°C increase in temperature. At 230°C, the NF didn't exceed 2.9dB in the 230.5MHz – 285.0MHz range.

At 25°C, the noise remained in the 1.0-1.5dB range. If the hump in the 230°C is neglected (since it was caused by external factors), the NF shows a 1dB degradation over the temperature range. Unfortunately, the factors causing this performance could not be resolved, but the performance is still notable for 230°C operation.

4.4.4 1-dB Compression

Although the linearity of the front-end does not impact the system linearity greatly, it is still desired to have a clean signal for a wide range of input powers. The 1dB compression test describes self-induced gain compression.

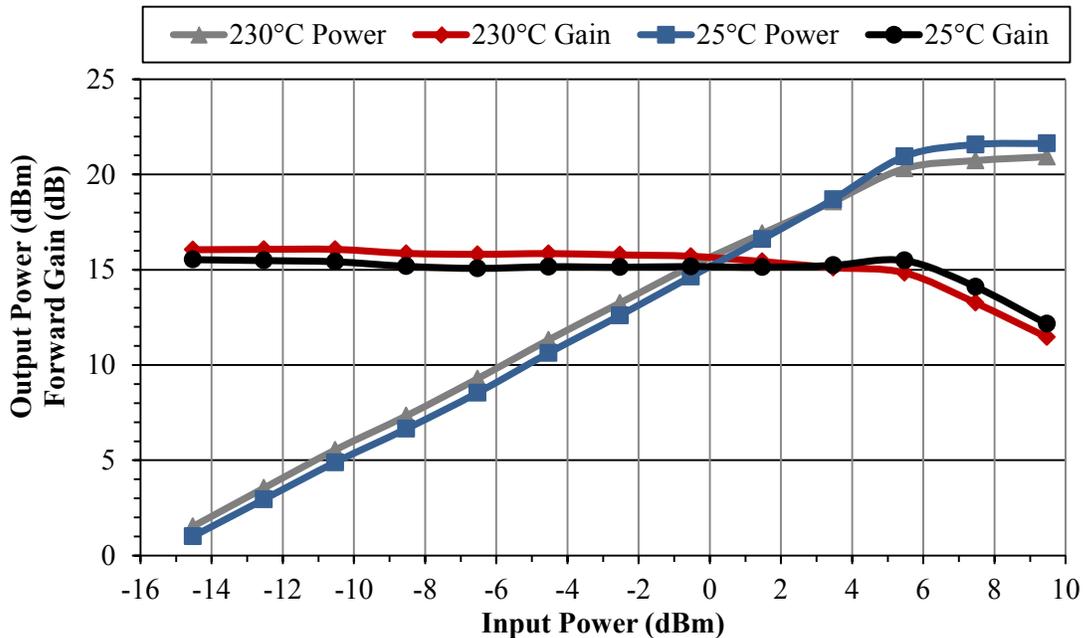


Figure 4.18: Compression testing vs. temperature

The compression was tested at both the frequency band edges and center, but, because the variance was small (caused by different gains at these points), the midband P1dB test is deemed revealing enough.

For this LNA, at 250MHz and 230°C, the input P1dB (IP1dB) power level was measured to be approximately +4dBm with an output P1dB (OP1dB) power level of 19.1dBm (note that the gain is 1dB compressed from the linear power region gain).

The P1dB did change with temperature, but only slightly. At 250MHz and 25°C, the P1dB levels were about +6dBm and 21.4dBm for the input and output, respectively. This is only a 2dB degradation in compression level over the temperature range from 25°C to 230°C.

4.4.5 Two-tone Tests (IP3 and IP2)

In addition to the compression test, the two-tone test help realize intermodulation products caused by interferers that can incite signals on desired signals. Again, the linearity of the first stage is typically not very significant in a system, but reducing nonlinearities is also desired.

Although the test for IP3 and IP2 are typically done so that the products are produced in the channel of operation, the tests for this LNA were relaxed so as to produce tones that were in the main band of use (IP3) and close by (IP2). As the LNA is capable of very wideband operation (>100MHz), this condition for the test was deemed acceptable.

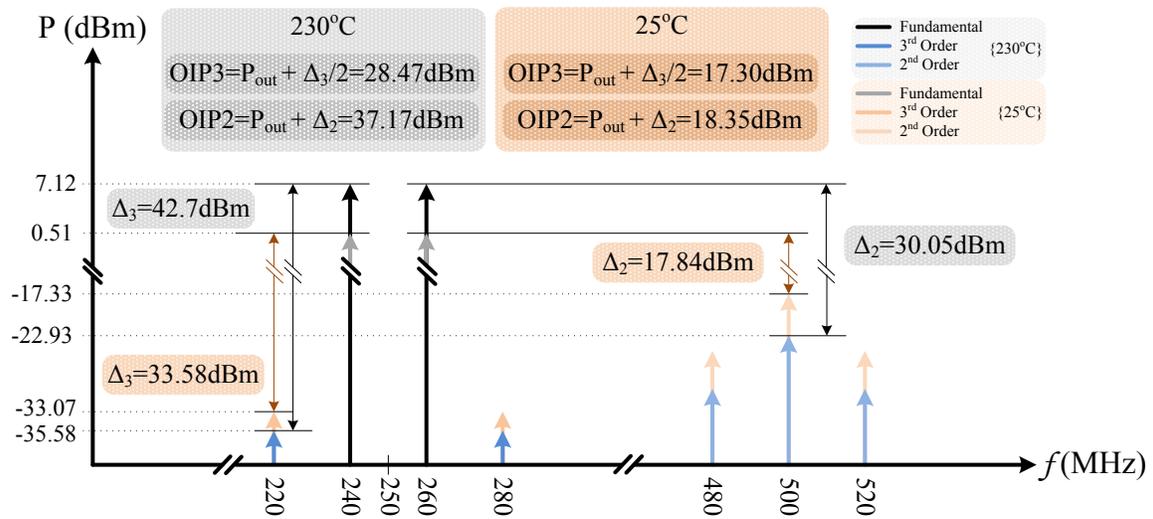


Figure 4.19: Two-tone testing vs. temperature

Figure 4.19 shows a basic diagram of the results of a two-tone test for IP3 and IP2. The measured values are shown for reference. Just like with the compression test, the two-tone test was done at the band edges and center, but the difference was not significant (<0.5dB variation).

The measured output IP3 (OIP3) and output IP2 (OIP2) centered around 250MHz and 230°C were measured to be 28.5dBm and 37.2dBm, respectively. The input power levels for these are simply the output levels less the gain (-16dB). For the 250MHz and 25°C case, the OIP3 and OIP2 were measured to be 17.3dBm and 18.4dBm, respectively.

It is noted that the IP3 and IP2 seem to improve with temperature and the compression degraded. This was not expected (compression and IP typically are directly related); however, the large mismatch and different temperature condition could be the reason. Also, the compression test at 25°C seemed to be self-reviving in the sense that it appeared to start compressing at a lower power level but then shows expansive characteristics that seemed to extend the compression point at 25°C. With this observation, both the IP and compression would improve with temperature, but certain circumstances at 25°C seemed to have improved the desensitization at this temperature for the compression test.

4.4.6 Drain Current Drift Under Constant Voltage Biasing

As mentioned above, the LNA was tested under the bias conditions that yielded an output match at 230°C. Data was taken to analyze the drift in the drain current over temperature for both a 25°C output matched case and 230°C output matched case (data results in the previous subsections). This data is presented in Figure 4.20.

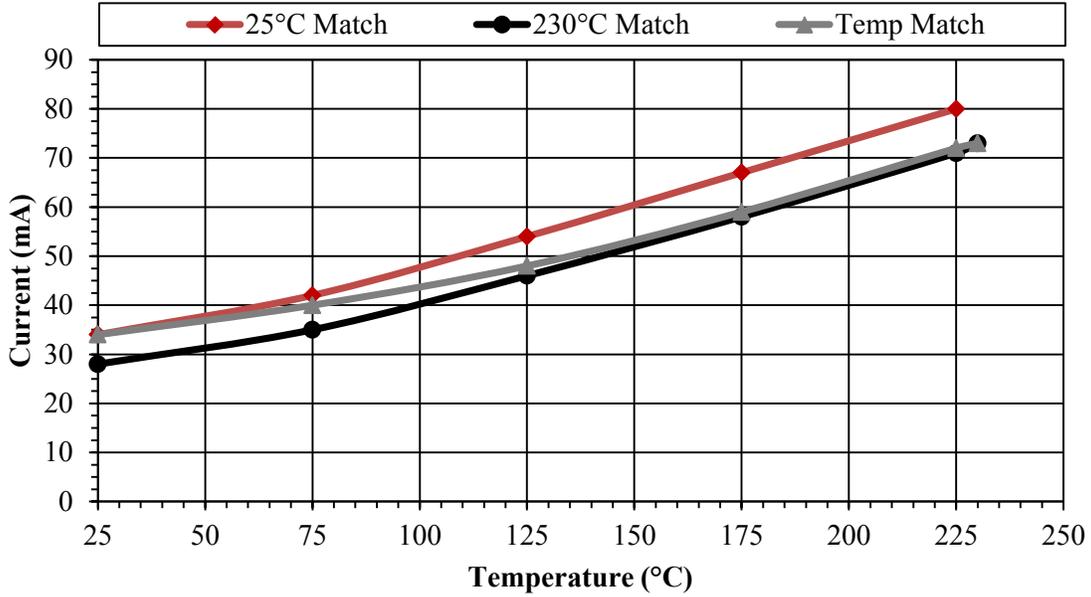


Figure 4.20: Drain current vs. temperature

It can be seen that the trend of current increase with temperature is fairly constant over a small bias change, but significantly far away to cause a noticeable degradation in performance at temperature far from the optimized matching condition.

The required drain current for a 230°C output match and $V_{DD}=4.0V$ was measured to be 73mA and the 25°C output match required 34mA. The drain voltage was held at 4.0V for all tests and approximately 13mA of current flowed through the feedback resistors. Calculating the total power consumption at 25°C and 230°C for the 230°C matched case yields

$$P_{DC,tot,230^\circ C\ match}^{25^\circ C} = (0.028A)(4.0V) = 0.112W \quad (4.2)$$

$$P_{DC,tot,230^\circ C\ match}^{230^\circ C} = (0.073A)(4.0V) = 0.292W \quad (4.3)$$

Note that, as 13mA flow through in the feedback resistor, $(13mA)(4.0V) = 52mW$ of power is not dissipated in the transistor. The true measure of dissipated power incorporates the output power minus the input power, but the levels of RF power are very small (at -30dBm input, the output would be approximately -14dBm; this results in a power reduction of 3.9mW). For this reason, the RF power additions/reductions are ignored.

For the 25°C matched case, the current is about 6.5mA higher. Therefore, the power levels would be greater by about 26mW.

4.4.7 Bias Conditions for Constant Output Match vs. Temperature

Also plotted in Figure 4.20 is the required current for an output match at every temperature (gray line). The line reveals how close the selected bias point was to the intended temperature-independent gain bias, exhibiting a slightly wider polynomial plot.

No tests were done to show the s-parameters or noise figure under this bias controlled condition, but inferences can be made as to the performance.

The gain would start higher and drop the entire rise in temperature, the return losses would be much sharper in band, the reverse isolation would probably not change much, the noise figure would also probably stay about the same, and the linearity would also have insignificant changes.

4.4.8 Ultra-Wideband Response

The ultra-wideband response is shown below for pedagogical purposes and to address some design choices that should be investigated in the next iteration of the design.

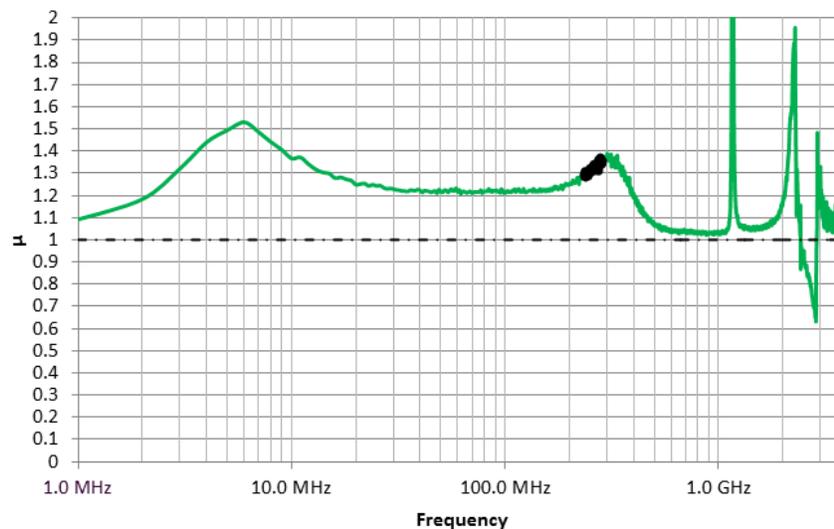


Figure 4.21: UWB stability parameter at 230°C from 1MHz to 4GHz – the black line represents the specified frequency band for operation

The choice to implement filtering off board results in a large band where amplification can occur (and not centered on the pass band). With this, the parasitics of the components and additional passbands of the microstrip cause a large gain peaking around 2.7GHz that pulls the LNA into conditional stability. For this, if a loading is

presented that is near the outer edges of the unit smith chart, an oscillation could occur. The addition of off-board filtering may be enough to remove this condition up at this frequency as long as it is not experiencing a second or third pass band in the region.

The output match can be seen to be very well positioned (black represents the frequency band of intended use).

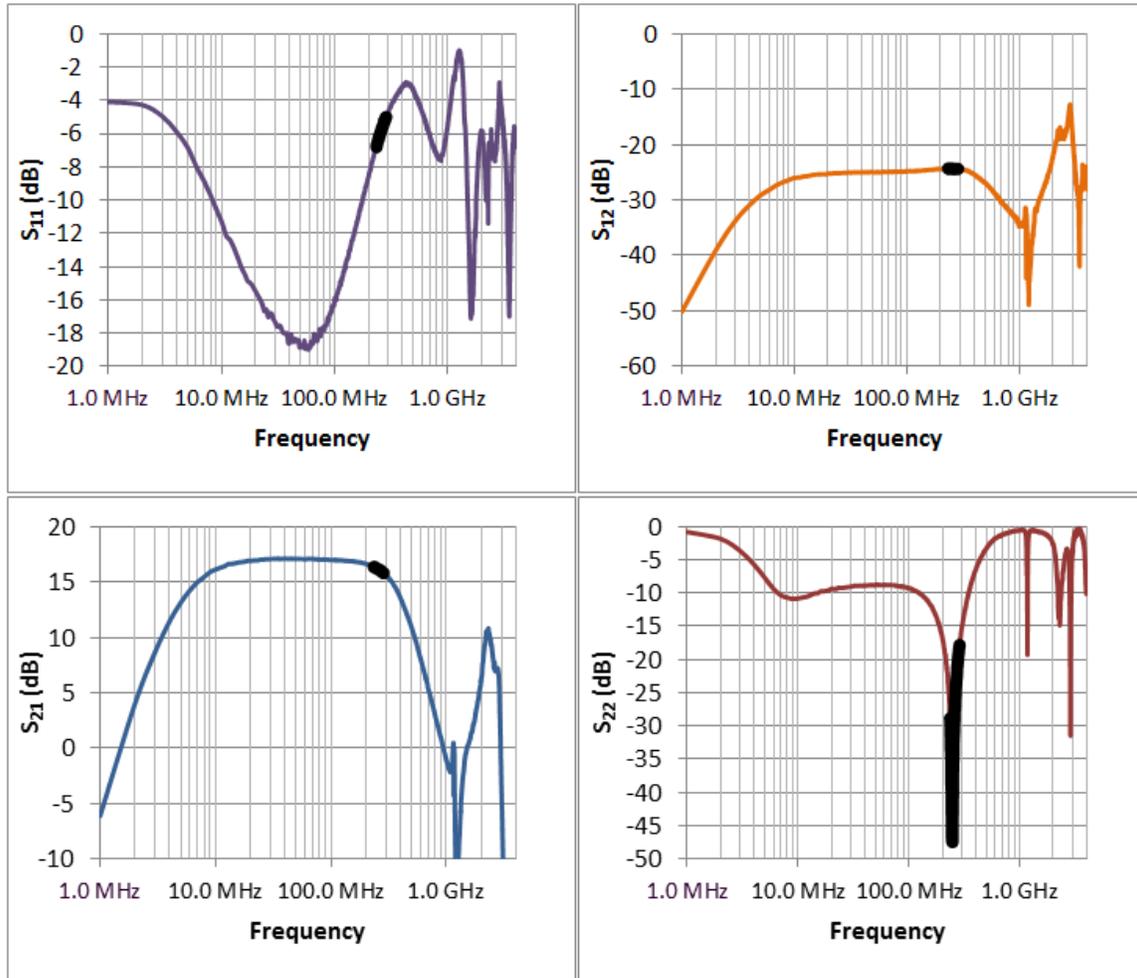


Figure 4.22: UWB response at 230°C from 1MHz to 4GHz – the black line represents the specified frequency band for operation.

4.4.9 Summary of Results

Table 4.1 summarizes the entire results of this LNA over the temperature range.

Table 4.1: Summary of Results

Design Parameter	Results					
Frequency	230.5MHz – 285.5MHz					
Temperature	25°C	75°C	125°C	175°C	225°C	230°C
Gain (dB)	16.08	16.37	16.70	16.54	16.19	16.16
Gain variance (dB)	±0.28	±0.30	±0.31	±0.32	±0.28	±0.28
Noise Figure (dB)	1.35	-	-	-	-	2.48
NF variance (dB)	±0.24	-	-	-	-	±0.42
ORL (dB)	≥16.2	≥17.5	≥18.0	≥18.0	≥18.5	≥18.2
IRL (dB)	≥5.1	≥5.2	≥5.4	≥5.2	≥5.0	≥5.0
Reverse Isolation (dB)	≥22.9	≥23.4	≥23.9	≥24.3	≥24.4	≥24.4
OP1dB (dBm)	21.4	-	-	-	-	19.1
OIP3 (dBm)	17.3	-	-	-	-	28.47
OIP2 (dBm)	18.35	-	-	-	-	37.17
μ	≥1.13	≥1.18	≥1.22	≥1.24	≥1.25	≥1.26
P_{DC} (mW)	112	140	184	232	284	292
I_D (mA) for output match with V_{DD}=4V at 250MHz	34	40	48	59	72	73

Chapter 5

5 Conclusion

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5.1 Summary

The above work describes the full design process for a 230°C capable LNA that is designed for low noise figure using traditional RF amplifier techniques. Good performance is exhibited across temperature from 25°C to 230°C. The LNA at 230°C is able to achieve a moderate gain of 16.16dB with a NF of 2.48dB and less than 0.5dB variation for both. The linearity is typical for GaN HEMT devices and is higher ubiquitous technologies, such as CMOS. The stability of the LNA is unconditionally stable of a very large bandwidth and the operation temperature allows for long-term use at high temperature according to the lifetime tests of the devices. Additionally, the LNA operates at fairly low power for an RF GaN power transistor. The performance is similar over the entire temperature range; notable changes as the temperature is lowered to 25°C are the improved NF (>1dB smaller), the worsened linearity, and the lower power consumption (<50%).

5.2 Conclusions

From the above proof-of-concept results, it is apparent that high temperature RF circuits is a fully realizable application that could easily incorporate more modern techniques in circuit design to increase performance for specific needs. With the growing need for better data acquisition and reliable, high frequency control circuits operating in extreme and harsh conditions, the field of high temperature RF and microwave circuits has a substantial room for growth – it adds the interesting challenge of temperature to the size, power, and frequency/speed focus that drive many commercial products today.

As this work was done for initial evaluation of practicality at a low RF frequency and using discrete component, the room for augmentation is large. Some complications with this design involve the stability of a device that was not intended for the power or frequency range being used. Additionally, the LNA was not input matched so as to avoid the need for more complicated circuitry during the evaluation of performance stage. Although the IRL is acceptable in many applications, matching is often desired. The use of an RF power transistor forfeited professionally tested data regarding noise performance. Also, one of the bigger design issues was the lack of a model above 85°C. The testing required to fully model the device at higher temperatures was not capable at this time, which sacrificed some freedom in design and also led to some ambiguity in design values.

5.3 Future Work

This work supports many paths that can be exploited for high temperature LNA design. Several of these aspects are improvements based on the final design and the rest regard thrusts for where this work supports new areas of this application.

Firstly, this design can be improved in several ways: the input of the LNA should be matched for wider acceptability in typically receiver chains. This match abdicates the ability to achieve the minimum noise figure in the LNA. However, this can be counteracted by employing a noise cancelling topology. For the cost of several more transistors and the biasing/power that comes with more devices, the noise could be even lower than that described here.

Secondly, the addition of a cascode transistor would could aid in increasing the gain significantly and also help to slightly reduce the NF through an increased circuit transconductance. Again, this comes at the cost of additional devices and more bias circuitry.

Thirdly, the LNA was designed to be as wideband as possible with the filtering being handled separately. The filtering can be done on board which will aid in the suppression of out-of-band spurs or interferers and aid in the stability at higher frequencies where component parasitics start to show up. As the requirement is considered wideband, the matching networks should be able to provide enough Q to both match and shape the pass band.

Fourthly, the use of a non-power device for the LNA should be explored. The use of a temperature-independent gain (among other temperature-independent biases) was not capable do to the large power required to achieve that performance. This led to a compromise to the next best temperature-independent bias, which relies on the control of matching networks to exploit the performance. A lower power device would exhibit these same useful bias points at power levels that can be implemented. However, this would typically come at the cost of higher junction-to-case thermal resistance. But, proper selection of the device and design can potentially make this point feasible.

Fifthly, the full DC, noise, small signal, and large signal characterization should be fashioned into a model that spans a larger temperature range. Accurately modeling can better assist in the selection of usable temperature compensation techniques that do not require controllers and will closely resemble the measured performance.

Sixthly, the move to IC design is an attractive option. A frequency increase would be required for reasonably sized boards and acceptable performance. However, the usability of an IC is much greater than discrete designs. Of course, there must be some difficulty. Aside from the parasitics at high frequency, the thermal design for an IC is much more difficult. Lower power consumption can aid in the feasibility, but the limitations of the fabrication and technology might make this a very challenging feat.

In the long term, a fully-integrated LNA that can operate in RF and microwave ranges at temperatures exceeding 250°C is a very realizable goal. As the technology fabrication is improved and the understanding of new materials is developed, high temperature

design will see tremendous expansion. As we continue to try to improve our understanding of extreme forged environments (e.g. engines) and explore farther depths of our world and beyond, the need and use of electronics will be forced to be able to handle harsher conditions than ever imagined by those in the nascent stages of electrical engineering.

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