SWITCH CAPACITOR FILTER DESIGN AIDS

by

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(ABSTRACT)

Two aids for the design of switched-capacitor filters (SCFs) are examined: breadboard modelling and computer simulations. A breadbroad was constructed based upon the same passive prototype of a seventh-order integrated filter. The breadboard met the original design specifications better than the integrated filter because the schematic and parasitics of the integrated filter were unknown.

Three computer programs, SPICE, DIANA, and TCAPS, are compared to determine their abilities and limitations in SCF design. SPICE is of limited value since it models switched capacitors as resistors. DIANA and TCAPS directly simulate the digital nature of switched capacitors, so they track in their predictions of

1) increased passband ripple,
2) increased cutoff frequency,
3) increased third notch frequency,
4) increased OBR.

On the basis of this comparison, it is not possible to determine if DIANA or TCAPS is the better program. However, both DIANA and TCAPS simulate SCFs far more accurately than SPICE.

ACKNOWLEDGEMENTS

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CHAPTER 1. INTRODUCTION

Accurate monolithic integrated filters are a reality with switched-capacitor (SC) techniques [1-4]. This is possible since the time constants of SC integrators are set by ratios of capacitor values, which can be controlled to tolerances of 0.1% to 0.5% [5]. In conventional active RC filters, integrator time constants are dependent upon the absolute value of an RC product, which cannot achieve the same accuracy in monolithic form.

In switched-capacitor filters (SCF), resistors are essentially replaced by capacitors and switches. Continuous current flow through a resistor is simulated by switching discrete charges stored on a capacitor from one point in a circuit to another [6]. In a way, one is designing a digital filter in which the charge stored on the capacitors of a SCF corresponds to the binary numbers stored in the data registers of a digital filter.

However, there are problems in designing SCFs. As in many digital filters, SCFs alias the frequency response about the clocking frequency of the switches. Also, the clock frequency has to be much greater than the cutoff frequency of the filter, f_{co}, or else the SC integrators introduce frequency warping of the filter poles and zeros [7-10]. Methods have been developed to minimize this effect [11-16].

Additional problems in SCF design are caused by component parasitics. The MOS transmission gates used to switch the capacitors have a non-zero resistance which increases with decreasing gate size.

Usually, one of the prime objectives of the integrated circuit design is to reduce the component size as much as possible. How small can the MOS switch size be reduced without increasing switch resistance to the point that the SCF's performance is affected? Similar questions can be asked of the MOS amplifier with respect to its gain-bandwidth product, input resistance, and output resistance.

All of these considerations point out the need for aids in the design of SCF, particularly in view of the high cost of an integrated test chip. Some work has been done to develop analysis and synthesis techniques [17-22], but many of these approaches are invalid when resistive elements are present. Also, all of the closed-form analytical techniques are very awkward to apply to higher-order filters. Therefore, the two main design aids investigated are construction of a breadboard, and simulation by computer.

Since a SCF is a hybrid analog-digital network, computer programs for digital networks cannot simulate the analog components. Likewise, programs for analog networks cannot deal with the digital aspect of SCFs. Several programs for the analysis of SC networks will be examined to determine their usefulness as design aids.

A computer simulation shows only the effects of parasitics modelled by the circuit designer. If the designer is not aware of a parasitic, or cannot include it due to program limitations, the simulation may not give an accurate indication of the filter's performance. Therefore, the more general programs will have a definite advantage over other programs.

If all significant parasitics are known and can be modelled by the program, computer simulation can be a great advantage in the final SCF design. Parasitic values can be changed and their effects on the filter's performance verified with relative ease.

Breadboard modelling has the advantage that unmodelled effects, which may be present in the integrated filter, can appear in the breadboard model.

An exact correspondence of element values in the integrated filter may not be practically obtained in the breadboard, but similar design strategies can be used. For example, the smallest capacitors on an integrated filter are of the order of . tenths of picofarads. It is not practical to obtain accurate capacitor ratios with discrete capacitors of that size. Since the SC integrator performance is dependent on ratios of capacitors, all capacitors can be scaled up to a larger value. Thus in this investigation, the breadboard of a SCF is also referred to as a scaled-capacitor filter or a scaled filter.

Additional problems with the breadboard are those typically associated with any hardware. First, one doesn't have the flexibility to quickly change element values, and second, the normal problems of ensuring that the wiring is correct and the components are working.

A seventh order elliptic SCF manufactured by Reticon is currently available commercially. A breadboard of this filter was constructed based on the same passive filter used in the Reticon design, as detailed in Chapter 2. The exact schematic was unknown, so reasonable

estimates of the filter's design were made. The goals in this part of the investigation were to determine how closely the scaled filter would predict the performance of the integrated filter, and to document the design of the scaled filter.

The goal of the computer simulation in Chapter 3 is to evaluate the abilities and limitations of three computer packages: DIANA, SPICE and TCAPS. The scaled filter designed in the first part of the thesis will serve as a basis of comparison. The computer packages are also used as design aids in the development and trouble-shooting of the scaled filter.

CHAPTER 2. A COMPARISON OF THE SCALED-CAPACITOR FILTER AND THE RETICON FILTER

An important aspect of any comparison is the need for a thorough understanding of the basis upon which the comparison rests. Without this, an explanation of performance differences would be virtually meaningless. The comparison of a breadboard filter with an integrated filter requires knowledge of at least three areas:

1. Design techniques
2. Construction techniques
3. Testing procedures

This chapter will describe these areas for both the breadboard and Reticon filters. In addition, test results will be compared and discussed.

2.1 The Scaled-Capacitor Filter

2.1.1 SC Integrators

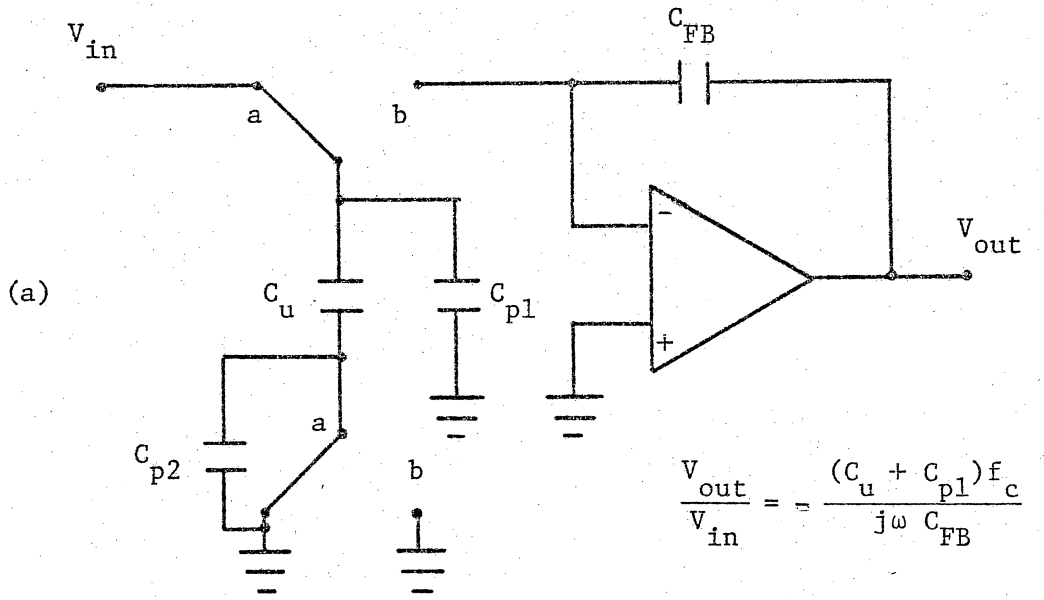
Before a detailed description of the design technique is undertaken, the SC integrators will be examined. The LDI (Lossless Discrete Integrator) [23] and bilinear integrators [11-13, 16] are two building blocks available to the SCF designer. However, since the structures discussed in this report operate with $f_c >> f_{co}$, only the LDI will be considered. This building block forms the basis for the Reticon as well as the scaled-capacitor filter.

The LDI has a parasitic-sensitive and a parasitic-insensitive version. "Parasitic" refers to the stray capacitances from the MOS

switch to ground, as shown in Figure 2.1-1. In the parasitic-sensitive integrator [7, 8, 9] of Figure 2.1-1a, C_{p2} is always connected from ground to ground and does not affect its operation. However, C_{p1} is directly in parallel with C_u at all times, and will increase the value of C_u by C_{p1}. If $C_u >> C_{p1}$, the effect on circuit performance is negligible, but with the capacitor values used in integrated circuits, C_{p1} could be of the same order of magnitude as C_u. Since the breadboard is to form an accurate model of the integrated filter, parasitic-sensitive integrators should clearly be avoided.

In the parasitic-insensitive integrator of Figure 2.1-1b, the stray capacitances are never in parallel with C_u [1, 10, 14]. When the switch is in position a, neither of the stray capacitors, C_{p1} nor C_{p2}, store any charge since their top plates are grounded through the switches. In position b, C_{p1} is effectively shorted since its top plate is connected to a virtual ground. At the same time, C_{p2} is charging up to V_{in} without affecting the charge on C_u. When the switch returns to position a, the accumulated charge on C_{p2} is discharged to ground, again without altering the charge on C_u. Since neither C_{p1} nor C_{p2} affect the SC integrator's performance, it is therefore parasitic-insensitive. Obviously, parasitic-free integrators should be used in both the Reticon filter and the breadboard filter.

Two types of parasitic-free integrator are available as shown in Figure 2.1-2: inverting and noninverting. Both have only negative summing inputs; this restricts the filter design and will be further discussed in Section 2.1.2.1. The derivation of the transfer function



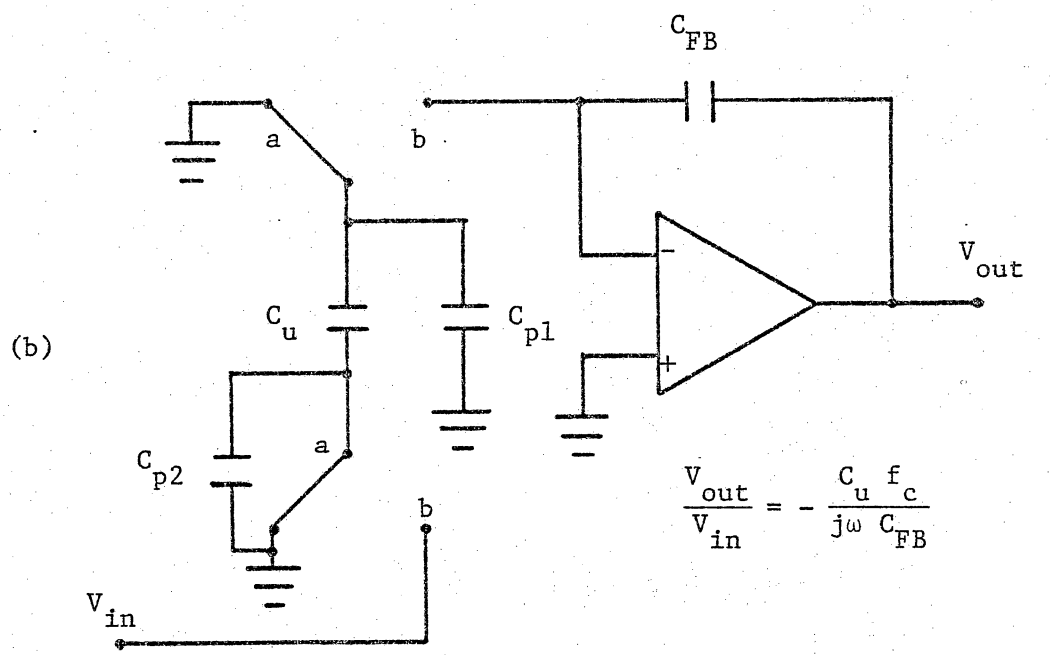


Figure 2.1-1. (a) Parasitic-sensitive inverting integrator, and (b) parasitic-insensitive inverting integrator.

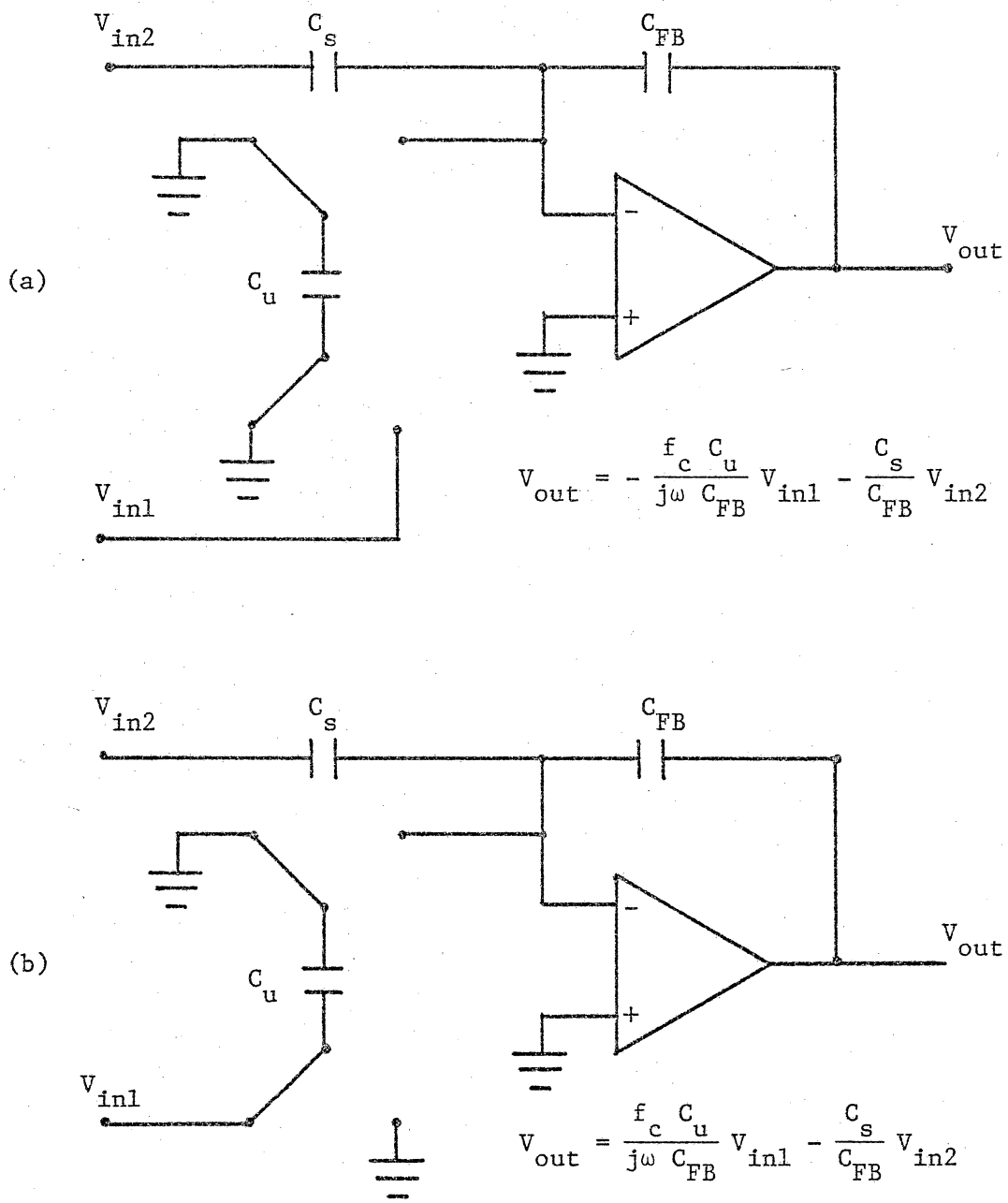


Figure 2.1-2. The two parasitic-free integrators used in the scaled filter: (a) inverting, and (b) non-inverting.

for these integrators is presented in Appendix 1. It is important to note that the transfer functions are valid only if $f_{clock} >> f_{co}$. Otherwise, frequency prewarping of the filter is necessary to set poles and zeros at the correct frequency. When $f_{clock} >> f_{co}$, the integrator time constant is set by the ratio of capacitors and not by the absolute component values. Also the time constant is inversely proportional to f_{clock}.

2.1.2 Leapfrog Filter Design

The leapfrog technique [7-9, 24, 25] is used in the design of SCFs for several reasons. The low sensitivity passband characteristics of the passive LC prototype can be retained by the SC realization. The filter response is relatively insensitive to changes in the element values. Furthermore, passive LC designs are already documented in existing tables.

When LDI stages are used in the leapfrog design, a canonical representation of the transfer function results. The LDI stages require one op amp for each integrator and the leapfrog design requires one integrator for each reactive element in the passive prototype. Therefore, only one op amp is required per reactive element in the passive prototype, and the number of op amps in the SCF is minimized. A conventional active RC filter would require inverters and is therefore non-canonic.

Another compelling reason for using the leapfrog design technique for the breadboard is that Reticon used it to produce their integrated filter.

The leapfrog design process can be divided into four main sections:

1) From tables, select a passive prototype which meets the design specifications.
2) Derive a signal flow graph which can be realized with switched capacitor integrators.
3) Calculate capacitor ratios of the SC filter by equating integrator time constants of the signal flow graph with those of the SC realization.
4) Maximize the dynamic range of the filter by adjusting loop gains.

2.1.2.1 Passive Prototype Selection

Filter specifications for the breadboard have already been set by the Reticon filter, as shown in Figure 2.1-3. According to the data sheet, the Reticon filter has a cutoff frequency of 1 kHz when the clock frequency is 50 kHz. The passive prototype of Figure 2.1-4a is selected from the design tables with a normalized transfer function shown in Figure 2.1-4b. This passive prototype exceeds the Reticon specifications, but it was known to form the basis for the Reticon filter.

2.1.2.2 Signal Flow Graph Development

The goal of this section is to develop the signal flow graph (SFG) so that equations of the SFG contain the same number of terms and the same sign for each term as the equations of the SC realization. This task is accomplished in six steps:

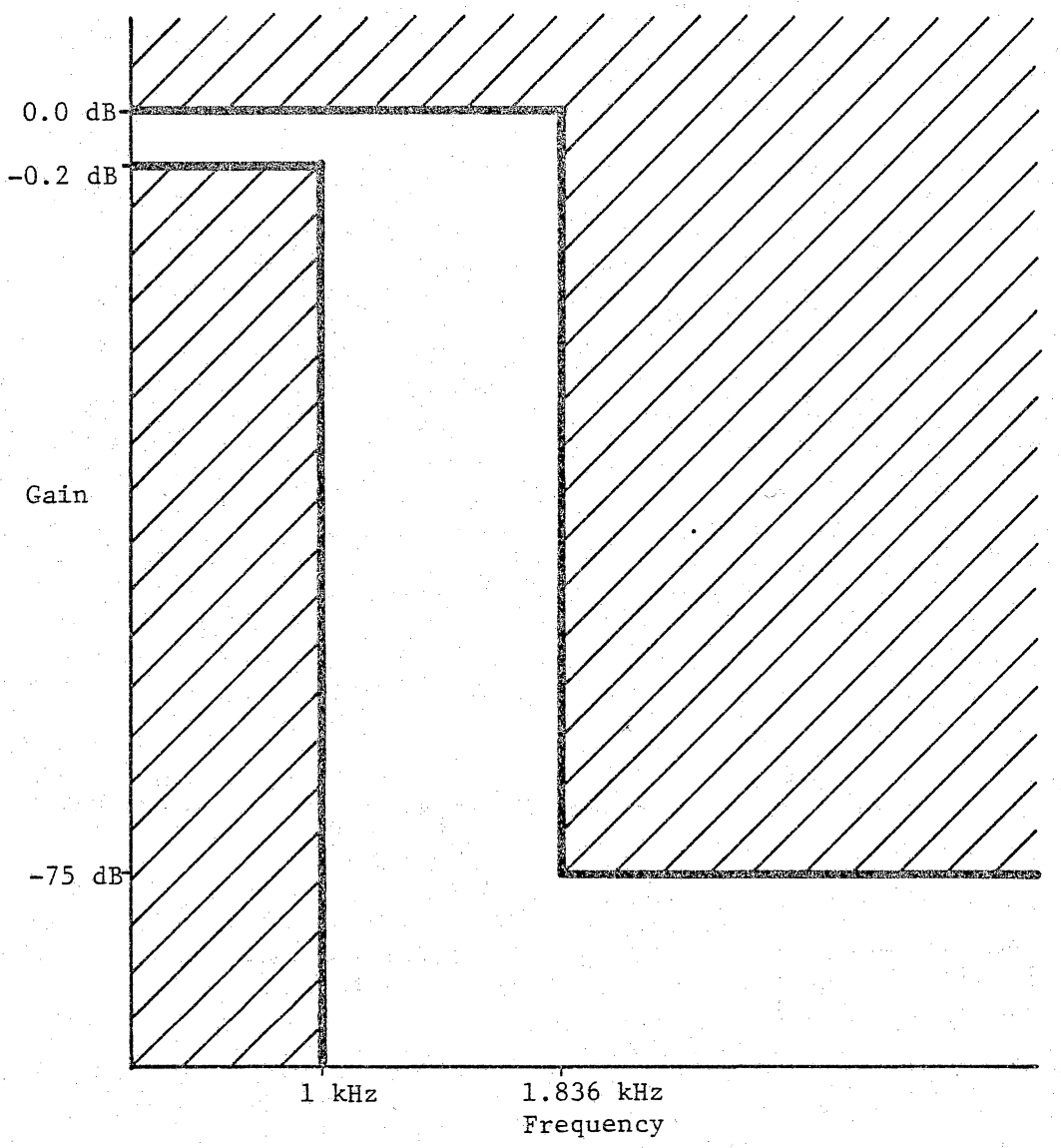
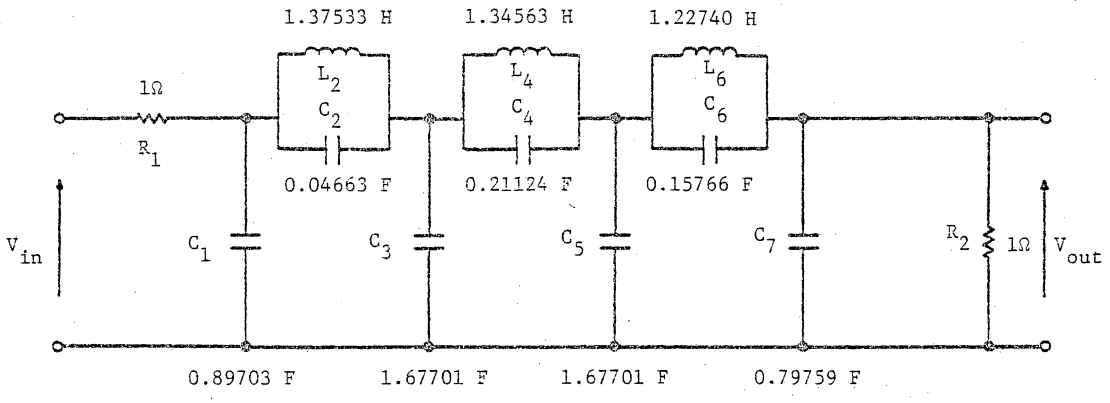
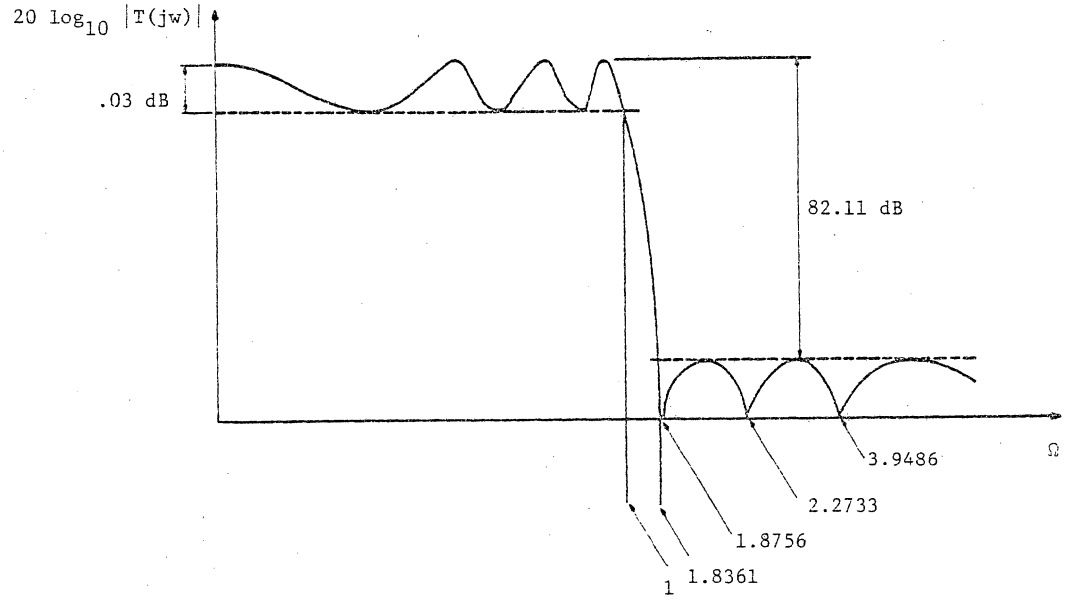


Figure 2.1-3. The design specifications of the scaled filter with f_{clock} = 50 kHz.



(a)



(b)

Figure 2.1-4. The normalized LC ladder prototype, (a), and it's normalized magnitude characteristic, (b).

Step 1. Change the series arm tank capacitors into voltage-dependent voltage sources.

Step 2. Construct a SFG based on the equations from the network of Step 1.

Step 3. Convert current nodes to voltage nodes.

Step 4. Reverse signs of appropriate nodes and branches to obtain a SFG which can be implemented with SC integrators.

Step 5. Adjust the overall gain so that the filter will have a 0dB insertion loss.

Step 6. Frequency denormalization.

The seventh order filter will be designed to illustrate these steps and further explanation will be given as necessary.

Step 1. Each series arm capacitor in the passive prototype acts in conjunction with the tank inductor to generate a pair of transmission zeros. These capacitors complicate the design of the SCF and lead to a non-canonic realization. To avoid this, voltage-controlled voltage sources (VCVS) simulate the action of the shunt capacitor. Consider the first several elements in the seventh order passive prototype shown in Figure 2.1-5a. If the interdependence of V_1 and V_3 is made explicit by two VCVSs, $V_a = V_3$ and $V_b = V_1$, as in Figure 2.1-5b, then:

$$V_1 = \frac{I_0 - I_2}{S(C_1 + C_2)} + V_a \frac{C_2}{C_1 + C_2} \qquad (2.1\text{-}1)$$

$$V_3 = \frac{I_2 - I_4}{S(C_2 + C_3)} + V_b \frac{C_2}{C_1 + C_3} \qquad (2.1\text{-}2)$$

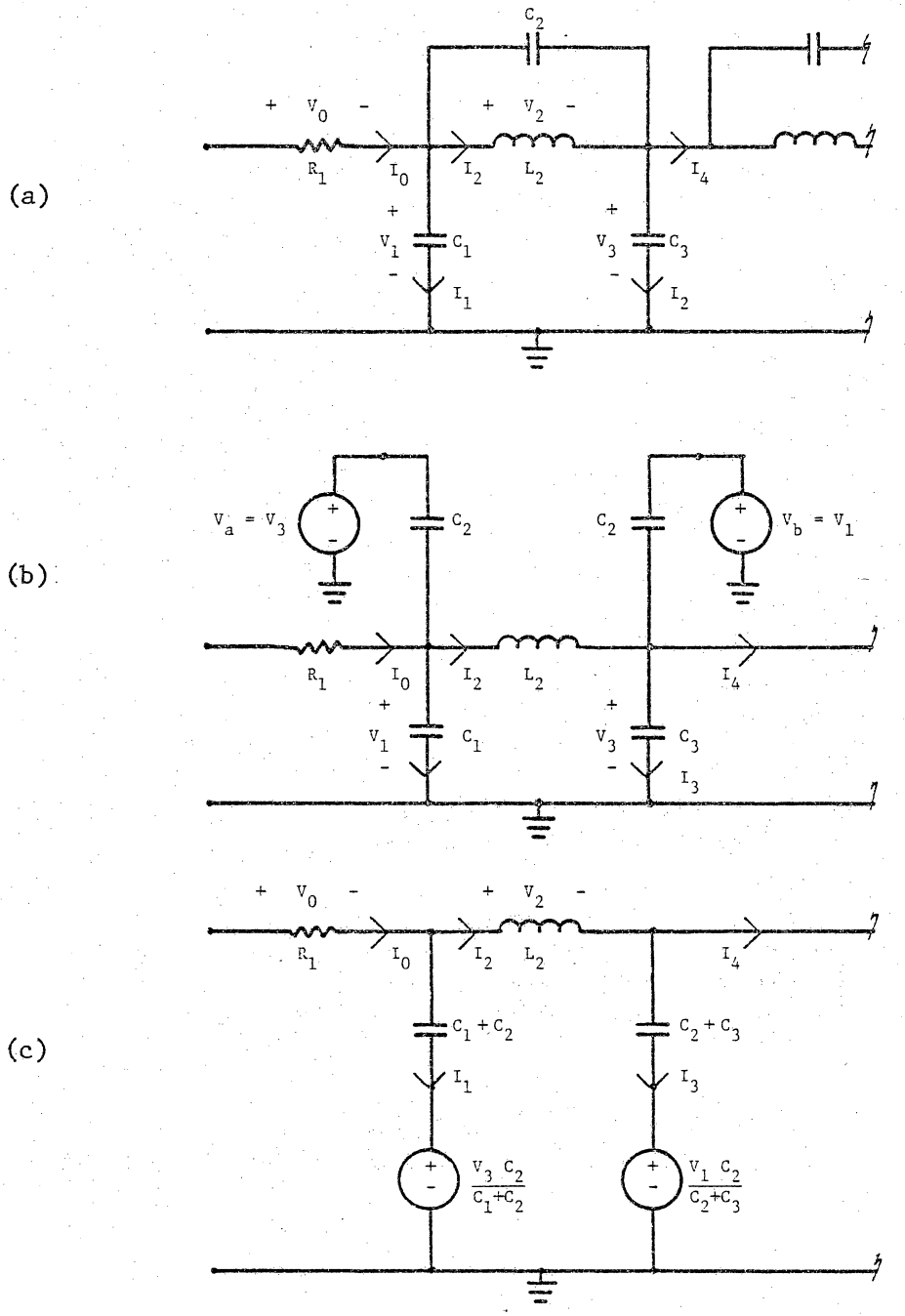


Figure 2.1-5. Replacing C_2 in (a) by two VCVSs in (c).

The effect of the shunt capacitor is to increase V_1 by some fraction of V_3 and increase the value of C_1 to $(C_1 + C_2)$. Similar observations can be made concerning its effect on V_3. An equivalent circuit, without the series arm capacitor, is shown in Figure 2.1-5c. The remaining shunt capacitors in the passive prototype are removed in a similar manner, resulting in the network of Figure 2.1-6.

Step 2. A SFG (Figure 2.1-7) is constructed with equations (Table 2.1-1) from the schematic of Figure 2.1-6 which relate the branch currents and the node voltages.

Step 3. The current nodes of the SFG are converted to voltage nodes, since only voltage nodes can be realized with existing SC building blocks. This conversion is achieved in two parts: first, all branches from a voltage source to a current source are multiplied by a scaling resistance, R_s. Next, all branches from a current source to a voltage source are divided by R_s. The value of R_s is arbitrary as far as the operation of the filter is concerned, since the proper loop gains are maintained. However, in the next section, it will be seen that a wise choice of R_s can simplify the circuitry of the SCF.

Step 4. Appropriate nodes and branches in the SFG are negated so that the filter can be realized with SC integrators. As noted earlier, LDI stages do not have positive summing inputs, so the SFG has to be changed to fulfill this requirement. All of the positive summing inputs are changed to negative summing inputs by negating V_3 and V_7 as in Figure 2.1-8. V_2' and V_6' were also negated under the mistaken impression that an integrator had to sample all its inputs at the same

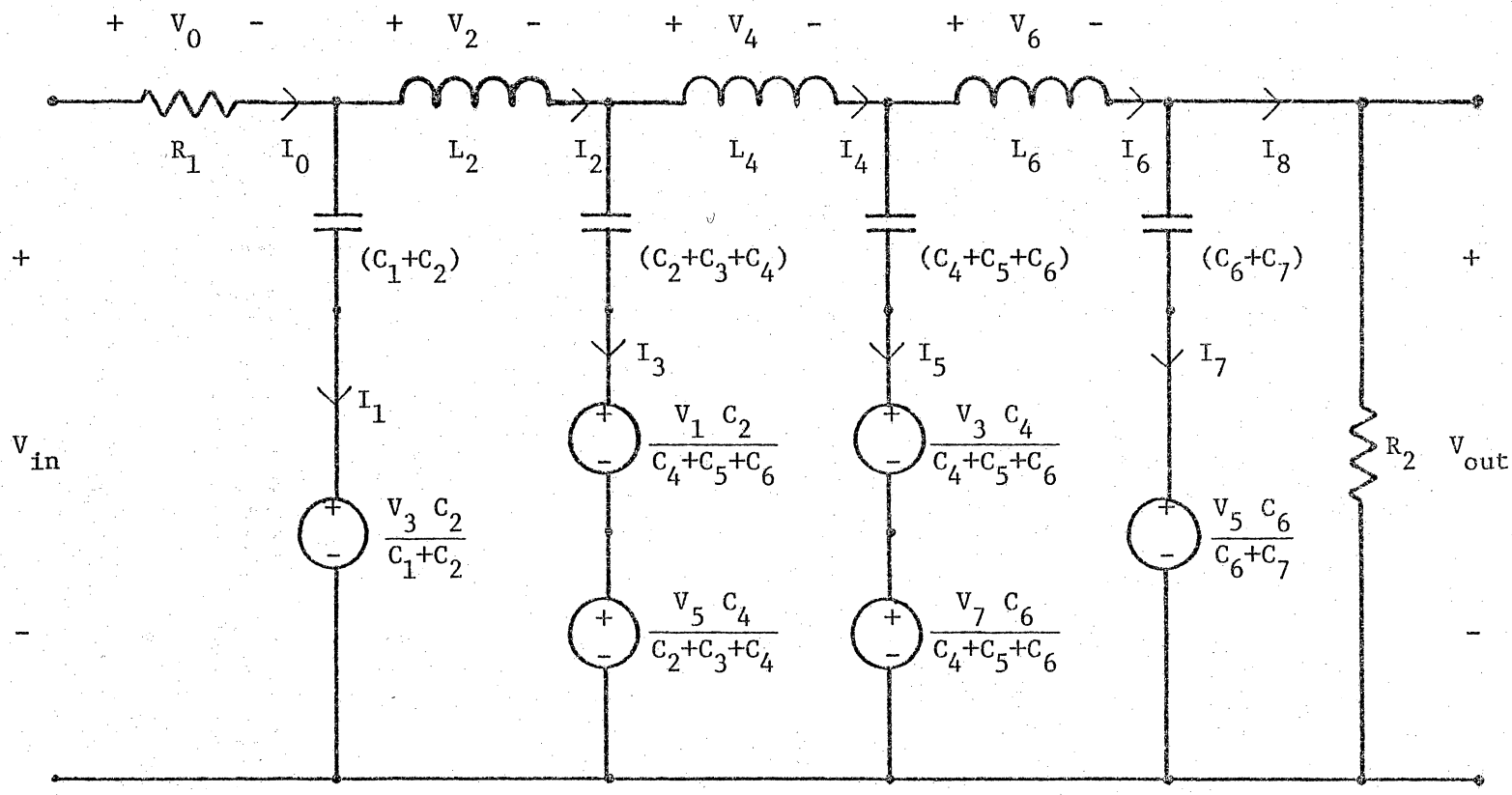


Figure 2.1-6. The passive prototype after the series arm capacitors have been replaced by VCVSs and modified values of shunt capacitors.

Table 2.1-1. The equations from the passive prototype used to develop the signal flow graph.

$$V_0 = V_{in} - V_1 \qquad I_0 = \frac{V_{in} - V_1}{R_1}$$

$$I_1 = I_0 - I_2 \qquad V_1 = \frac{I_1}{s(C_1 + C_2)} + V_3 \frac{C_1}{C_1 + C_2}$$

$$V_2 = V_1 - V_3 \qquad I_2 = \frac{V_2}{sL_2}$$

$$I_3 = I_2 - I_4 \qquad V_3 = \frac{I_3}{s(C_2 + C_3 + C_4)} + \frac{V_1 C_2}{C_2 + C_3 + C_4} + \frac{V_5 C_4}{C_2 + C_3 + C_4}$$

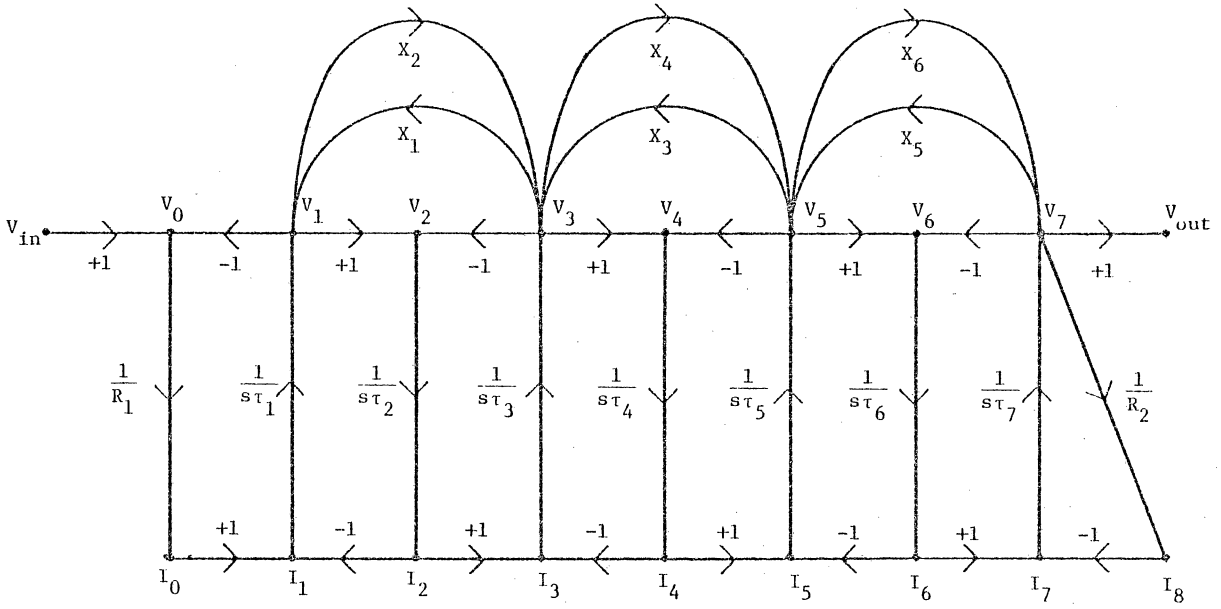
$$V_4 = V_3 - V_5 \qquad I_4 = \frac{V_4}{sL_4}$$

$$I_5 = I_4 - I_6 \qquad V_5 = \frac{I_5}{s(C_4 + C_5 + C_6)} + \frac{V_3 C_4}{C_4 + C_5 + C_6} + \frac{V_7 C_6}{C_4 + C_5 + C_6}$$

$$V_6 = V_5 - V_7 \qquad I_6 = \frac{V_6}{sL_6}$$

$$I_7 = I_6 - I_8 \qquad V_7 = \frac{I_7}{s(C_6 + C_7)} + \frac{V_5 C_6}{C_6 + C_7}$$

$$I_8 = \frac{V_7}{R_2}$$



$\tau_1 = C_1+C_2$ $\quad$ $\tau_5 = C_4+C_5+C_6$

$\tau_2 = L_2$ $\quad$ $\tau_6 = L_6$

$\tau_3 = C_2+C_3+C_4$ $\quad$ $\tau_7 = C_6+C_7$

$\tau_4 = L_4$

$$X_1 = \frac{C_2}{C_1+C_2} \qquad X_4 = \frac{C_4}{C_4+C_5+C_6}$$

$$X_2 = \frac{C_2}{C_2+C_3+C_4} \qquad X_5 = \frac{C_6}{C_4+C_5+C_6}$$

$$X_3 = \frac{C_4}{C_2+C_3+C_4} \qquad X_6 = \frac{C_6}{C_6+C_7}$$

Figure 2,1-7. SFG of the passive prototype.

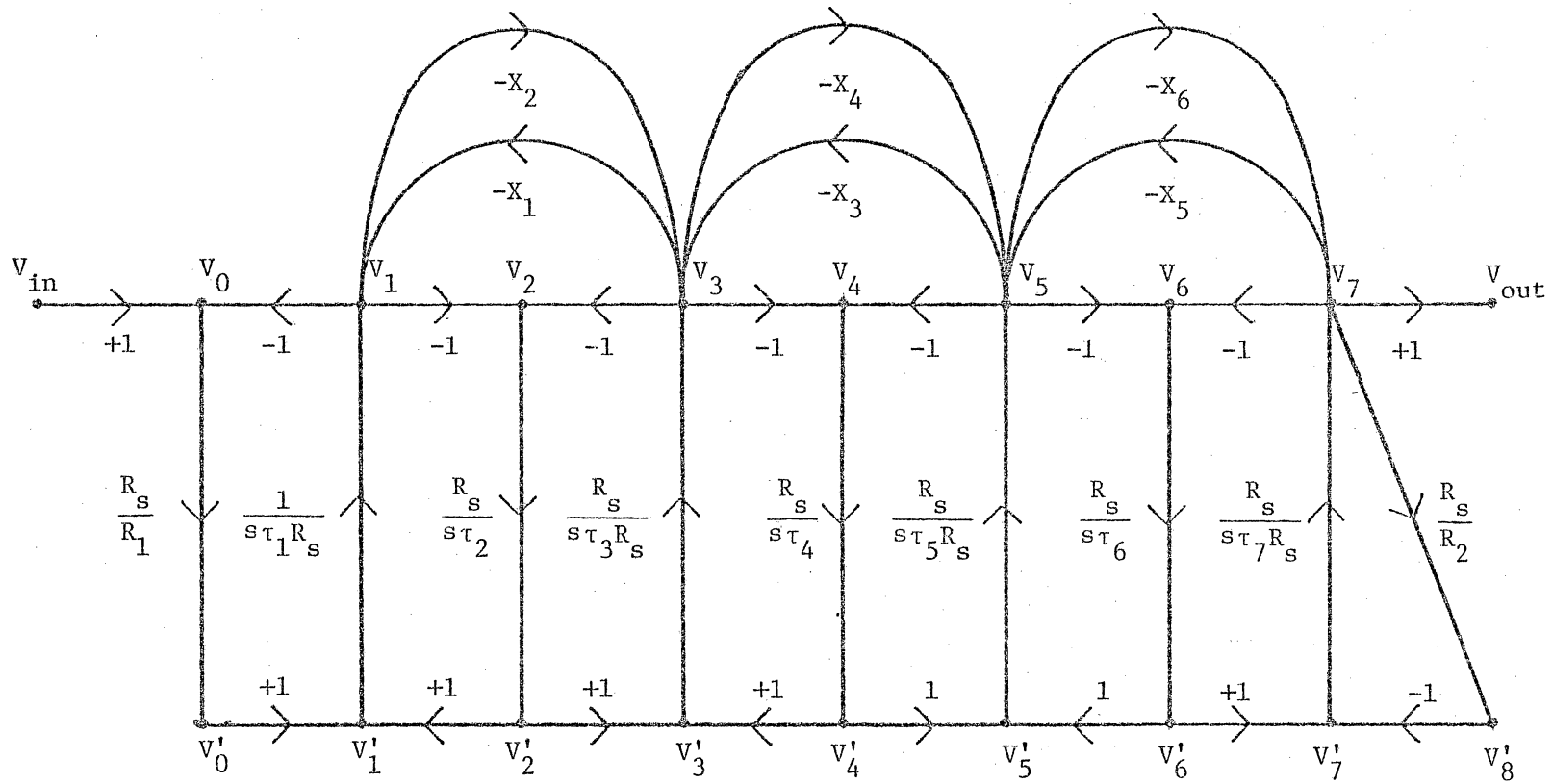


Figure 2.1-8. The current nodes of the SFG have been converted to voltage nodes and V'_2, V_3, V'_6, and V_7 have been negated.

time. Although, later found to be unnecessary, the extra inverted nodes clearly do not affect the idealized performance of the network.

To keep the loop gains unchanged, all input and output branches of V_2', V_3, V_6', and V_7 are multiplied by -1. One difficulty arises in this step: the SCF realization is no longer canonical, since an extra op amp is required to realize the -1 gain from V_7 to V_{out}. To avoid this, the branch from V_{in} to V_0 should be negated instead of the branch from V_7 to V_{out}. The same SFG results without an additional op amp since the filter input is negated instead of the filter output.

Unfortunately, this negation of the input was overlooked in the original design of the seventh order filter, and as a result, the scaled filter's response is 180° out of phase with the Reticon filter. Since the amplitude response, not the phase response, is the basis of the filter comparison, the validity of the scaled filter as a predictor of the integrated filter's performance is unaffected. All of the SFGs and schematics shown from this point will reflect this discrepancy.

Step 5. The filter gain is adjusted to produce a 0 dB insertion loss. The passive prototype is designed for matched loads, resulting in a 6 dB insertion loss for the SCF. This is overcome by increasing the gain of the input branch to 2.

Step 6. The passive prototype element values are normalized to a cutoff frequency of 1 rad/sec and a termination resistance of 1 Ω. The filter is denormalized to a different cutoff frequency and termination resistance by replacing the normalized element values with

$$R = R_T R_k \,, \qquad (2.1\text{-}3)$$

$$L = \frac{R_T L_k}{\omega_{co}} , \qquad (2.1\text{-}4)$$

and

$$C = \frac{C_k}{R_T \omega_{co}} , \qquad (2.1\text{-}5)$$

where R, L, and C are the denormalized element values; R_k, L_k, and C_k are the normalized element values; R_T is the resistance denormalization factor; and ω_{co} is the frequency denormalization factor.

For the seventh order filter, $\omega_{co} = 2\pi \cdot 1$ kHz, and the choice of R_T is discussed in the next section. For the present, the denormalization factors will be left explicitly in each term of the SFG, as shown in Figure 2.1-9.

The second section of the filter design is completed. The SFG of the passive prototype has been manipulated into a form which can be implemented with SC integrators. Moreover, the SCF will have a canonical realization, since the number of op amps have been minimized. Denormalization factors have also been incorporated into the SFG.

2.1.2.3 Calculation of Capacitor Ratios

The procedure outlined in this section of the SCF design sets the capacitor ratios, the scaling resistance, and the impedance denormalizer. The SFG of Figure 2.1-9 can be redrawn using integrator blocks with summing inputs as in Figure 2.1-10. Then SC integrators can be substituted for the integrator blocks.

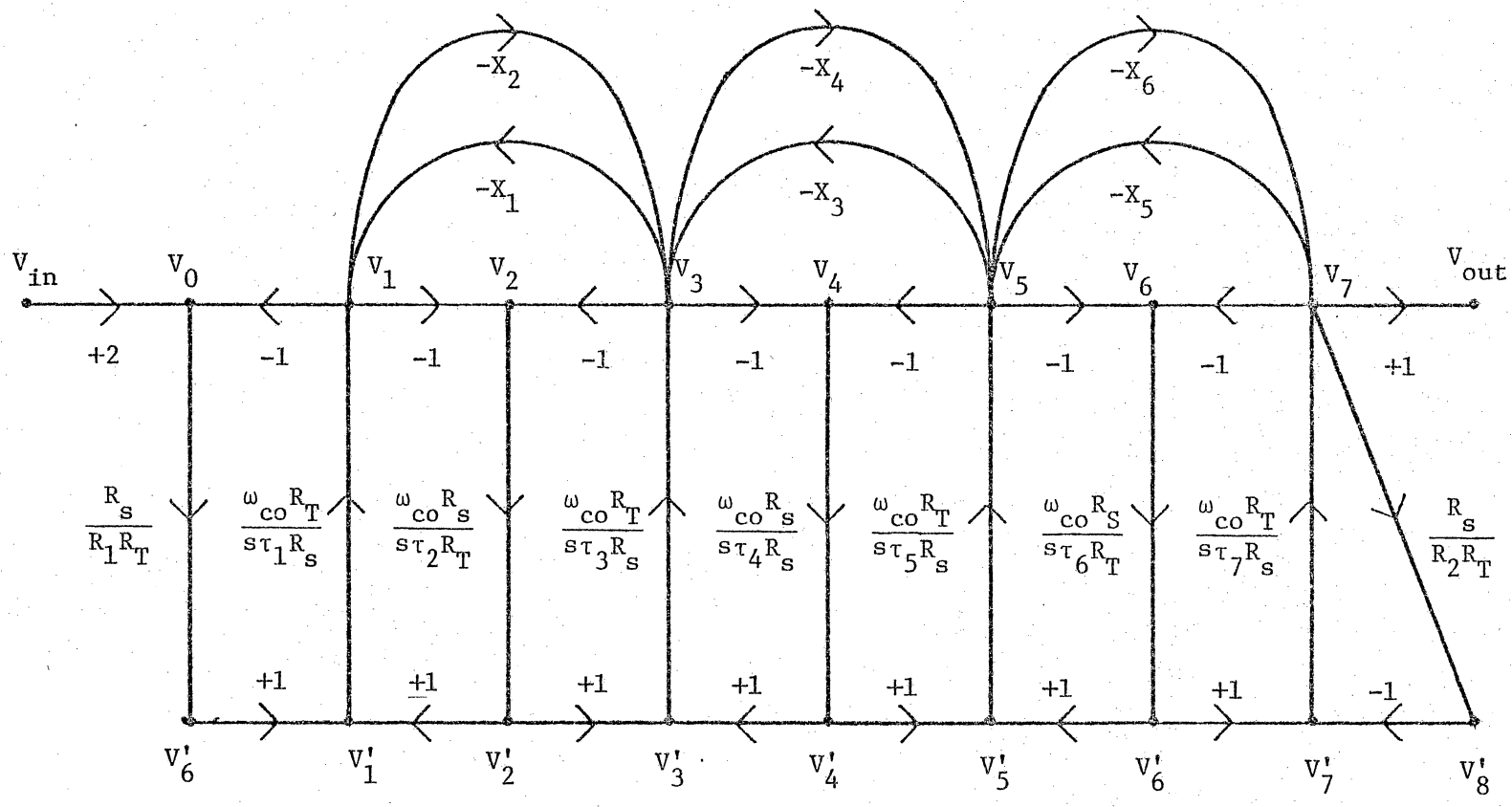


Figure 2.1-9. The denormalized SFG.

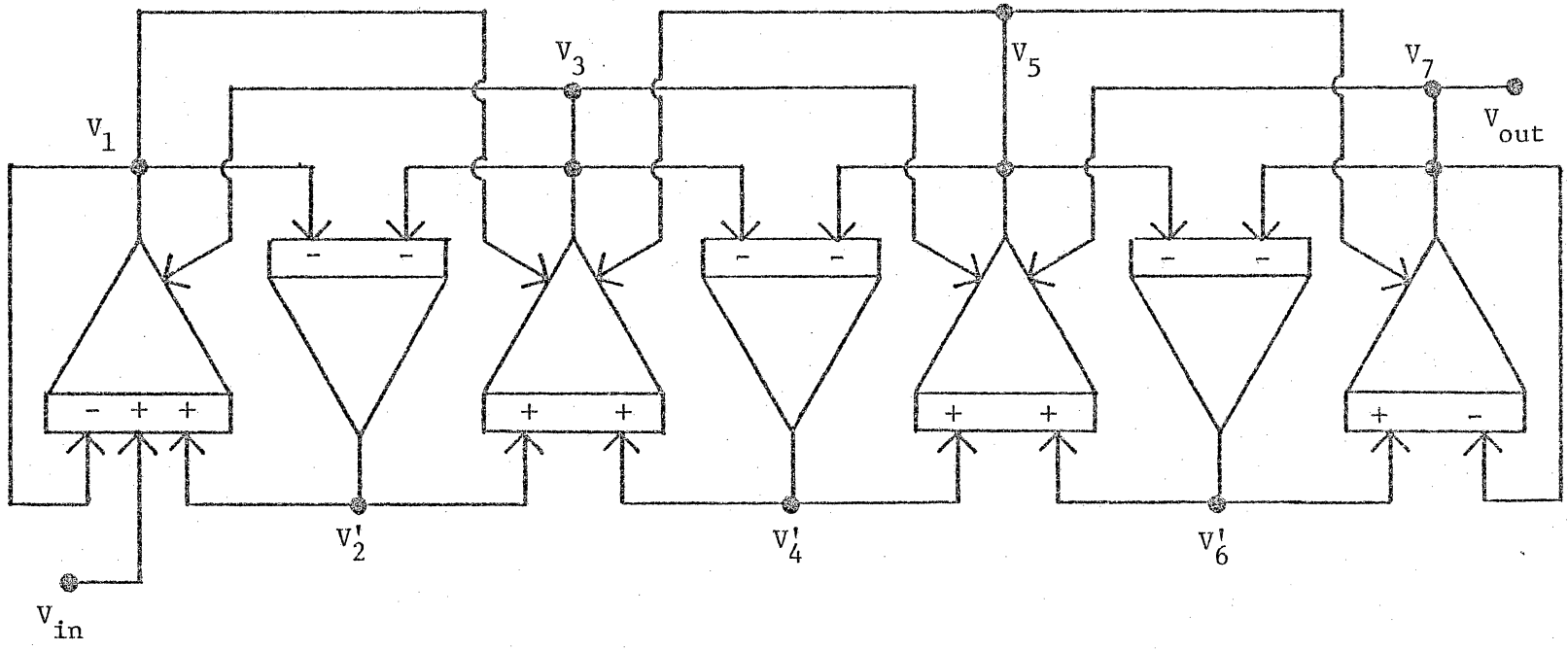


Figure 2.1-10. The SFG of Figure 2.1-9 is drawn as a block diagram, where the integrators can be replaced by SC integrators.

During this substitution, it is critical for the filter's performance to have the correct switch phasing between adjacent SC integrators. A switch phasing rule is developed in Appendix 2, and the results are presented here. First, a definition: when the switch is in position b on the integrators of Figure 2.1-2, the op amp is said to be sampling the switched capacitors. Then, to ensure proper filter performance, either

1) the op amps of all stages sample the switched capacitors on the same clock phase;

or

2) the op amps of alternate stages sample the switched capacitors on alternate clock phases.

A schematic of the seventh-order scaled-capacitor filter is drawn in Figure 2.1-11 using the second option of the switch phasing rule. The switched capacitors are labeled as unit capacitors (C_u) since they implement the unity gain branches of Figure 2.1-9.

The values of the capacitors are determined by comparing the equation of each stage of the SCF schematic with the corresponding stage of the SFG. For example, the first stage of the SCF has the following expression:

$$V_1^{SCF} = \left(2\, V_{in}^{SCF} - V_1^{SCF} + V_2'^{SCF}\right) \frac{f_c\, C_u}{sC_{I1}} - \frac{C_{c2}}{C_{I1}} V_3^{SCF} \qquad (2.1\text{-}6)$$

The first stage of the SFG of Figure 2.1-9 yields

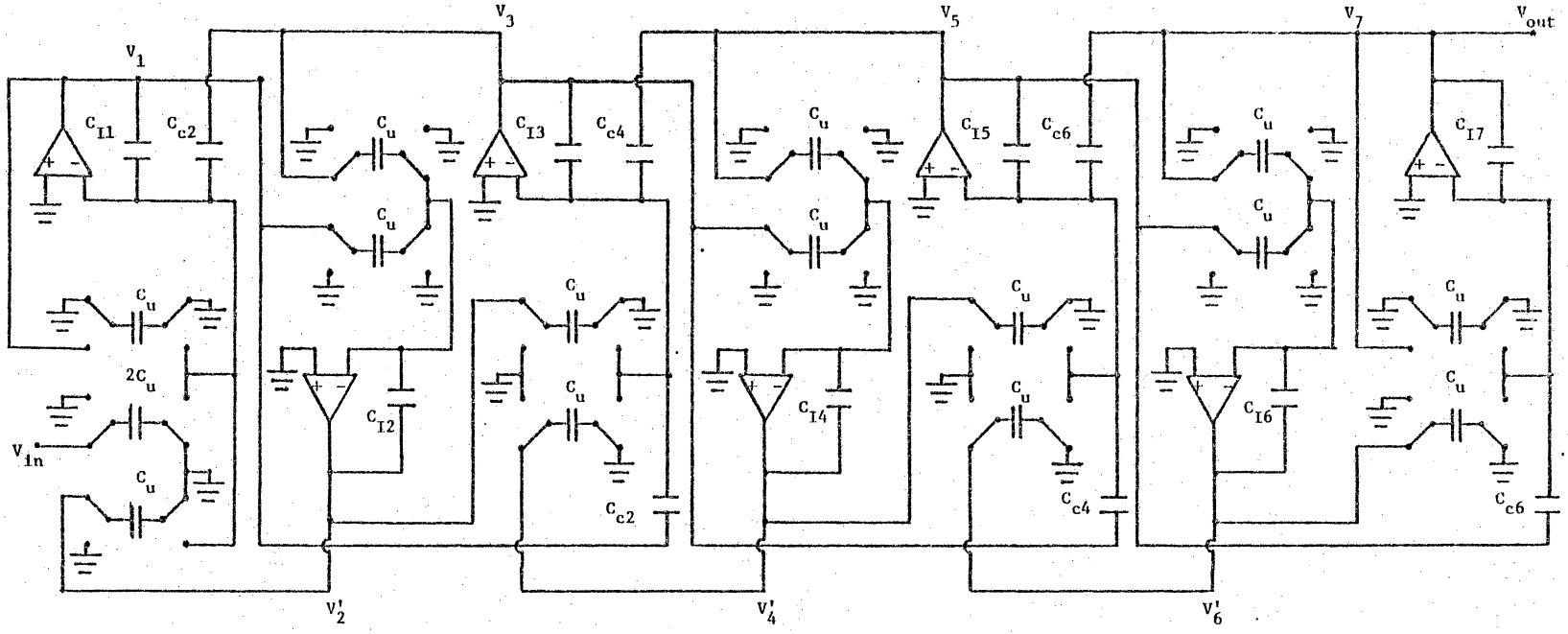


Figure 2.1-11. The scaled filter schematic results from inserging SC integrators into the block diagram of Figure 2.1-10.

$$V_1^{SFG} = \left(2 \frac{R_s}{R_T R_1} V_{in}^{SFG} - \frac{R_s V_1^{SFG}}{R_T R_1} + V_2'^{SFG} \right) \frac{\omega_{co} R_T}{s(C_1+C_2)R_s} - \frac{C_2}{C_1+C_2} V_3^{SFG} \tag{2.1-7a}$$

$$V_1^{SFG} = \left(\frac{2 V_{in}^{SFG}}{R_1} - \frac{V_1^{SFG}}{R_1} + \frac{R_T V_2'^{SFG}}{R_s} \right) \frac{\omega_{co}}{s(C_1+C_2)} - \frac{C_2}{C_1+C_2} V_3^{SFG} \tag{2.1-7b}$$

Equations (2.1-6) and (2.1-7b) will be equal if all of the coefficients are equal. With $R_1 = 1$, the following terms result:

$$\frac{\omega_{co}}{s(C_1+C_2)} = \frac{f_c C_u}{C_{I1}} \tag{2.1-8a}$$

$$\frac{R_T}{R_s} = 1 \tag{2.1-8b}$$

$$\frac{C_2}{C_1+C_2} = \frac{C_{c2}}{C_{I1}} \tag{2.1-8c}$$

Rearranging Equation (2.1-8a) yields

$$\frac{C_{I1}}{C_u} = (C_1+C_2) \frac{f_c}{\omega_{co}} \tag{2.1-9}$$

From Equation (2.1-8b), one can see that the choice of R_s and R_T is arbitrary as long as they are equal.

Combining Equations (2.1-8c) and (2.1-9) results in

$$\frac{C_{c2}}{C_u} = C_2 \frac{f_c}{\omega_{co}} \tag{2.1-10}$$

Similar equations, relating capacitor ratios to prototype values, are derived in Appendix 3 for the rest of the filter.

For the seventh order filter, f_c = 50 kHz and f_{co} = 1 kHz. Therefore,

$$\frac{f_c}{\omega_{co}} = \frac{50}{2\pi} \qquad (2.1\text{-}11)$$

Introducing this, along with the passive prototype values of Figure 2.1-4 into the equations of Appendix 3 results in the capacitor ratios shown in Table 2.1-2.

2.1.2.4 Dynamic Range Optimization

A filter was constructed using the capacitor ratios of the previous section, but the second notch at 2.27 kHz never appeared. Upon further investigation (see Appendix 4), maximizing the dynamic range of the SCF solved this problem.

The dynamic range of a switched capacitor filter is optimized in the same manner as for a conventional active filter [10, 26]. The gain of each stage of the filter is adjusted so that all stages will have the same maximum voltage. The procedure may be summarized as:

1) Run a computer simulation of the filter to determine the maximum signal level for each stage. The results for the seventh order filter were found to be:

$$|V_1|_{max} = 1.941 \text{ V}$$

$$|V_2|_{max} = 2.405 \text{ V}$$

Table 2.1-2. The capacitor ratios for the scaled-capacitor filter.

Capacitor Ratios	Value
$\frac{C_{I1}}{C_u} = (C_1 + C_2)\frac{f_c}{\omega_{co}}$	7.509
$\frac{C_{I2}}{C_u} = (L_2)\frac{f_c}{\omega_{co}}$	10.945
$\frac{C_{I3}}{C_u} = (C_2 + C_3 + C_4)\frac{f_c}{\omega_{co}}$	15.397
$\frac{C_{I4}}{C_u} = (L_4)\frac{f_c}{\omega_{co}}$	10.708
$\frac{C_{I5}}{C_u} = (C_4 + C_5 + C_6)\frac{f_c}{\omega_{co}}$	15.729
$\frac{C_{I6}}{C_u} = (L_6)\frac{f_c}{\omega_{co}}$	9.767
$\frac{C_{I7}}{C_u} = (C_6 + C_7)\frac{f_c}{\omega_{co}}$	7.602
$\frac{C_{C2}}{C_u} = (C_2)\frac{f_c}{\omega_{co}}$	.371
$\frac{C_{C4}}{C_u} = (C_4)\frac{f_c}{\omega_{co}}$	1.681
$\frac{C_{C6}}{C_u} = (C_6)\frac{f_c}{\omega_{co}}$	1.255

$$|V_3|_{max} = 2.030 \text{ V}$$

$$|V_4|_{max} = 2.403 \text{ V}$$

$$|V_5|_{max} = 1.610 \text{ V}$$

$$|V_6|_{max} = 1.651 \text{ V}$$

$$|V_{out}|_{max} = 1.000 \text{ V}$$

2) Define a gain normalization factor K_i for each stage:

$$K_i = \frac{|V_i|_{max}}{|V_{out}|_{max}}$$

Since $|V_{out}|_{max} = 1$ volt for this particular filter,

$K_i = |V_i|_{max}$, i = 1, ..., 7.

3) Adjust the loop gains for each stage by dividing all the input gains of the i^{th} integrator by K_i and multiplying all the outputs of the i^{th} integrator by K_i as shown in Figure 2.1-12.

4) Change the values of the capacitors in the SCF to reflect the changes in the signal flow graph. Each of the capacitors in the SCF of Figure 2.1-13a can be related to a gain in the signal flow graph as shown in Figure 2.1-13b. Ratios for all filter capacitors following the dynamic range adjustment are listed in Table 2.1-3.

Thus, the design of the SCF is completed. The basic integrator stages, the leapfrog design technique and its application to SCF have been discussed along with the optimization of the dynamic range.

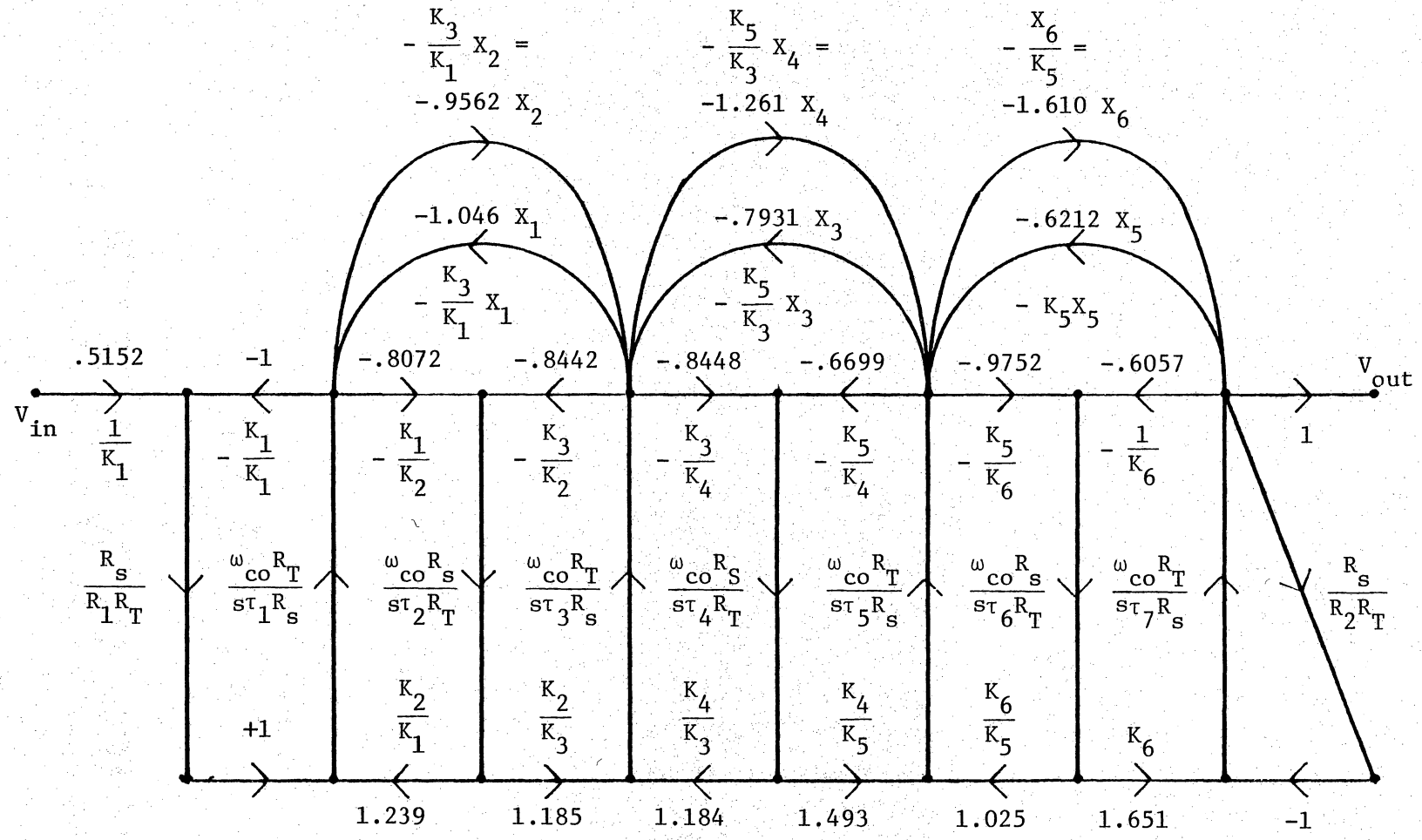


Figure 2.1-12. SFG of the passive prototype after the optimization of the dynamic range.

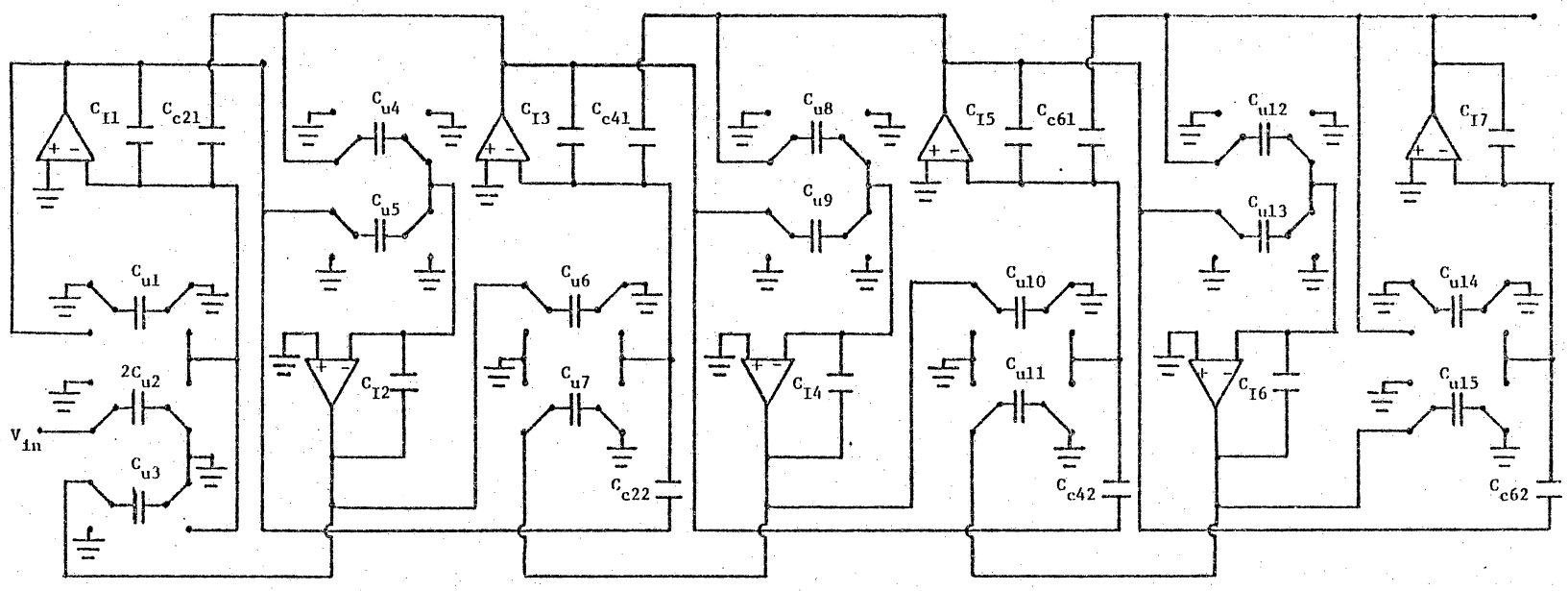


Figure 2.1-13a. The schematic of the seventh order filter relabelled for dynamic range optimization.

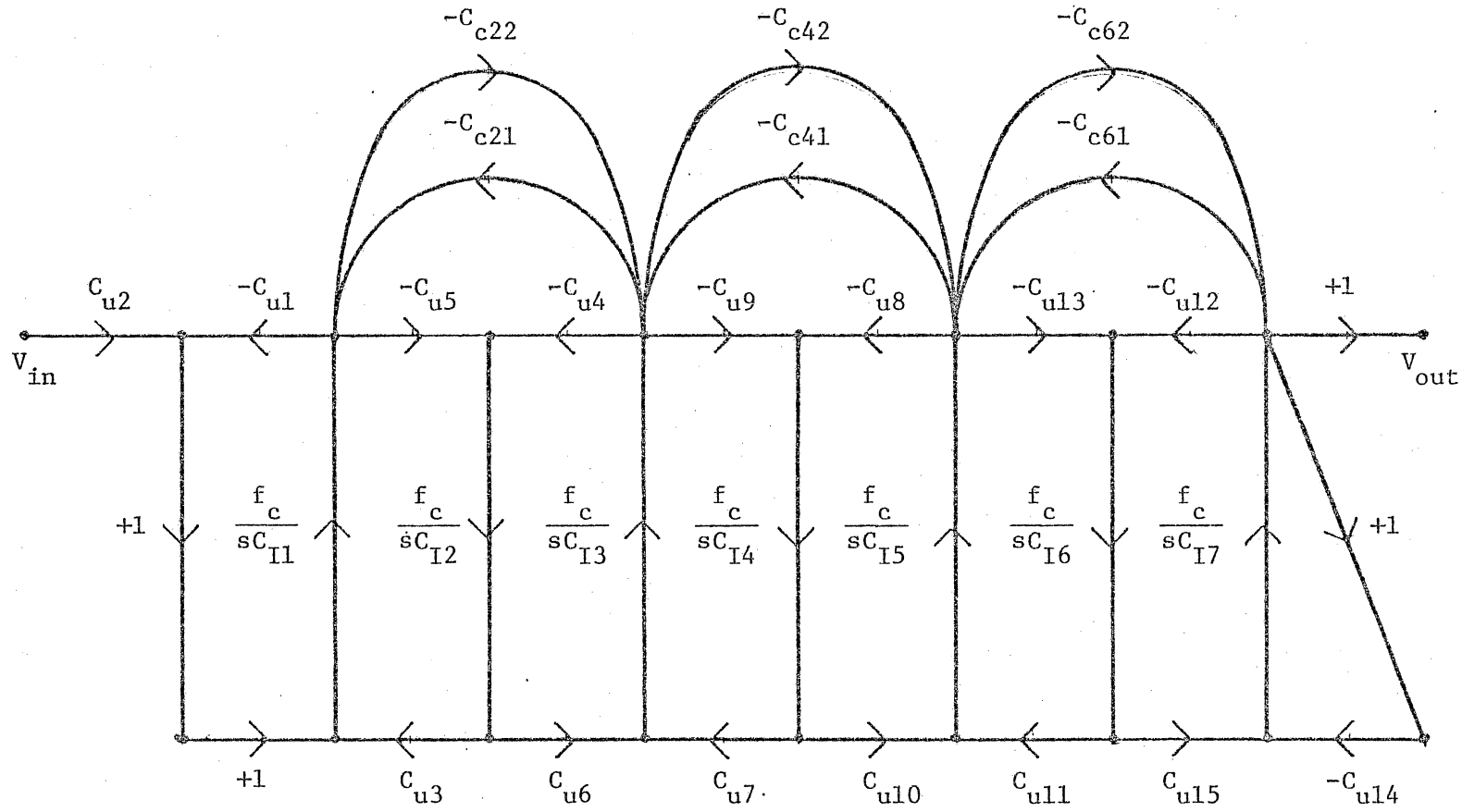


Figure 2.1-13b. SFG showing capacitor values.

Table 2.1-3. The calculation of capacitor values after the dynamic range adjustment.

$C_{u1'} = C_u$

$C_{u2'} = \frac{1}{K_1} C_u = 0.515\ C_u$

$C_{u3'} = \frac{K_2}{K_1} C_u = 1.239\ C_u$

$C_{u4'} = \frac{K_3}{K_2} C_u = 0.844\ C_u$

$C_{u5'} = \frac{K_1}{K_2} C_u = 0.807\ C_u$

$C_{u6'} = \frac{K_2}{K_3} C_u = 1.185\ C_u$

$C_{u7'} = \frac{K_4}{K_3} C_u = 1.184\ C_u$

$C_{u8'} = \frac{K_5}{K_4} C_u = 0.669\ C_u$

$C_{u9'} = \frac{K_3}{K_4} C_u = 0.845\ C_u$

$C_{u10'} = \frac{K_4}{K_5} C_u = 1.493\ C_u$

$C_{u11'} = \frac{K_6}{K_5} C_u = 1.025\ C_u$

$C_{u12'} = \frac{1}{K_6} C_u = 0.606\ C_u$

$C_{u13'} = \frac{K_5}{K_6} C_u = 0.975\ C_u$

$C_{u14'} = C_u$

$C_{u15'} = K_6 C_u = 1.651\ C_u$

$C_{c21'} = \frac{K_3}{K_1} = 1.046\ C_{c2}$

$C_{c22'} = \frac{K_1}{K_3} = 0.956\ C_{c2}$

$C_{c41'} = \frac{K_5}{K_3} = 0.793\ C_{c4}$

$C_{c42'} = \frac{K_3}{K_5} = 1.261\ C_{c4}$

$C_{c61'} = \frac{1}{K_5} = 0.621\ C_{c6}$

$C_{c62'} = K_5 C_{c6} = 1.610\ C_{c6}$

$C'_{I1} = C_{I1}$

$C'_{I2} = C_{I2}$

$C'_{I3} = C_{I3}$

$C'_{I4} = C_{I4}$

$C'_{I5} = C_{I5}$

$C'_{I6} = C_{I6}$

$C'_{I7} = C_{I7}$

2.1.3 Components and Construction of the Scaled-Capacitor Filter

2.1.3.1 Components

The op amp used in the breadboard is a Harris HA4605 fabricated by the bipolar process. Major specifications are:

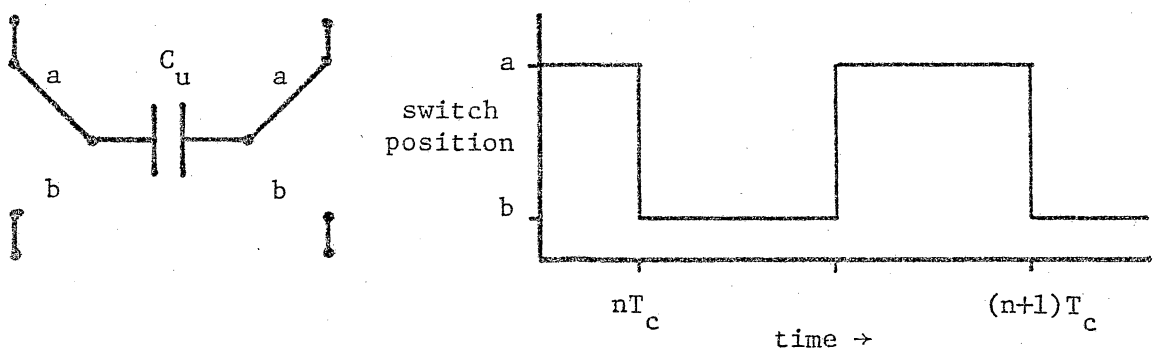
Input Resistance	100 kΩ
Gain-Bandwidth Product	8 MHz
DC Gain	250 k
Slew Rate	±4 V/μsec

The analog switch is a SPST Harris HI-201 having the following specifications:

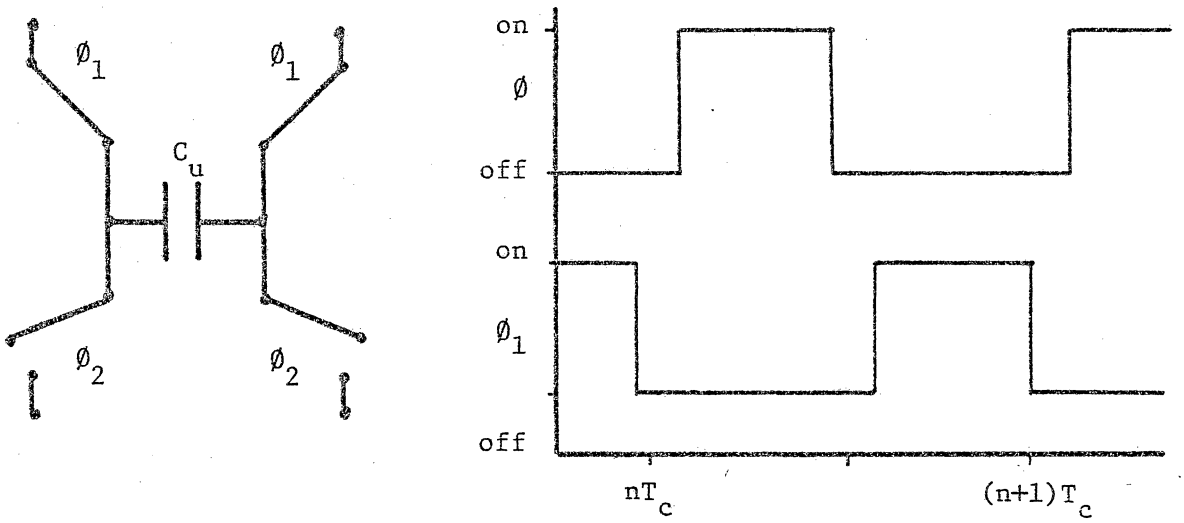
On Resistance	65 Ω
Switching Time	185 nsec
Switch Capacitance	5.5 pf

An initial design of the scaled filter used Harris HI-5046 which are DPDT switches. The HI-5046 is specified as a break-before-make switch, however there was some slight overlapping of switch phases which caused significant deterioration of the filter characteristic. Therefore, the SPST HI-201 switches with two clock sources are used, as shown in Figure 2.1-14 to prevent the switch phase overlap. The switch resistance of 65 Ω is an approximation derived from performance curves since the resistance is dependent upon the analog voltage level.

Capacitors on the scaled filter are a mixture of polycarbonate film and NPO with a Q of approximately 1000. A reasonable value of C_u was chosen as 150 pf to keep charging time constants well below the sampling period. Table 2.1-4 shows both the calculated and actual



(a)



(b)

Figure 2.1-14. The switched capacitor of (a) is realized with 4 switches and two non-overlapping clocks in (b).

Table 2.1-4. Ideal and actual capacitor values for the dynamically-ranged scaled filter

Capacitor	Ideal Values (pF)	Actual Values (pF)	Error
C_{u1}	150.0	150.9	0.6%
C_{u2}	154.6	156.0	0.91%
C_{u3}	185.9	185.5	-0.22%
C_{u4}	126.6	127.2	0.47%
C_{u5}	121.1	121.7	0.50%
C_{u6}	177.8	179.5	0.96%
C_{u7}	177.6	179.3	0.96%
C_{u8}	100.5	100.1	-0.40%
C_{u9}	126.7	128.8	1.66%
C_{u10}	223.9	224.0	0.04%
C_{u11}	153.8	152.1	-1.11%
C_{u12}	90.9	90.5	-0.40%
C_{u13}	146.3	145.2	-0.75%
C_{u14}	150.0	150.4	0.27%
C_{u15}	247.7	249.9	0.89%
C_{I1}	1126.4	1126	-0.04%
C_{I2}	1641.8	1647	0.32%
C_{I3}	2309.6	2310	0.02%
C_{I4}	1606.2	1613	0.42%
C_{I5}	2359.3	2355	0.18%
C_{I6}	1465.0	1469	0.27%
C_{I7}	1140.3	1142	0.15%

Table 2.1-4. Ideal and actual capacitor values for the dynamically-ranged scaled filter (Continued)

Capacitor	Ideal Values (pF)	Actual Values (pF)	Error
C_{C21}	58.1	58	-0.17%
C_{C22}	53.2	54	-1.5%
C_{C41}	199.9	201	+0.55%
C_{C42}	317.9	318	+0.03%
C_{C61}	116.9	116	-0.77%
C_{C62}	303.0	304	+0.33%

values of the filter capacitors. Capacitor values were kept within 2% of design values by checking them on a bridge (ESL Model 253). Also, capacitor ratios were within 1.5% of design values. Actual values were obtained with four or less capacitors and were not tweaked to improve the filter's performance.

2.1.3.2 Construction

The breadbroad was constructed using wirewrap techniques since wiring changes and corrections could be performed much easier than with other techniques such as point-to-point wiring with soldered connections or a printed circuit board. The power supply connections of all integrated circuits were shunted with .01 μF capacitors to bypass clock or input signals. Bypass capacitors were soldered to wirewrap pins to ensure good connections while all other capacitors were soldered to component carriers.

Each stage of the filter used one HA4605 chip (which has four op amps). Since only one op amp is required for each stage, the inputs of the three unused op amps were grounded. With this procedure, removing an op amp chip disabled only one stage of the filter instead of four stages, thus simplifying the troubleshooting of the filter.

Also, the HI-201 switches were wired to ease troubleshooting. The four SPST switches required by a switched capacitor are available on one HI-201, so each SC is connected to one HI-201. By removing one HI-201, one switched capacitor is removed; by removing one HA4605, one op amp is removed. Thus, sections of the filter can be isolated with relative ease.

Troubleshooting of the filter was achieved by comparing computer plots of the transfer function of sections of the filter with the breadboard performance of those sections. A typical example is shown in Figures 2.1-15 and 2.1-16; the transfer function plot generated by DIANA being used to check the performance of stage 5 to stage 7 of the SCF. By removing appropriate capacitors and chips, the circuit of Figure 2.1-16 was tested without rewiring the filter.

2.1.3.3 Experiment Setup

The experiment setup and equipment used to test the breadboard are shown in Figure 2.1-17. The 600 ohm resistor shunting the input of the filter matches the output impedance of the tracking generator, thus guaranteeing a constant input reference signal.

The clock source consists of a master generator, which sets the frequency, and two slave generators, which differentially set the relative phase between ϕ_1 and ϕ_2. This arrangement allowed maximum flexibility in setting the duty cycles and relative phases of the clocks. The clocks were initially set as follows:

1st: Set frequency on master clock

2nd: Set voltage levels on clock sources 0 → 10 V

3rd: Set duty cycle of each slave clock with duty cycle and frequency adjustment (when in triggerred mode TEK FG504 frequency is set by master clock and the frequency adjustment alters the duty cycle)

4th: Set relative phase between the two slave clock sources

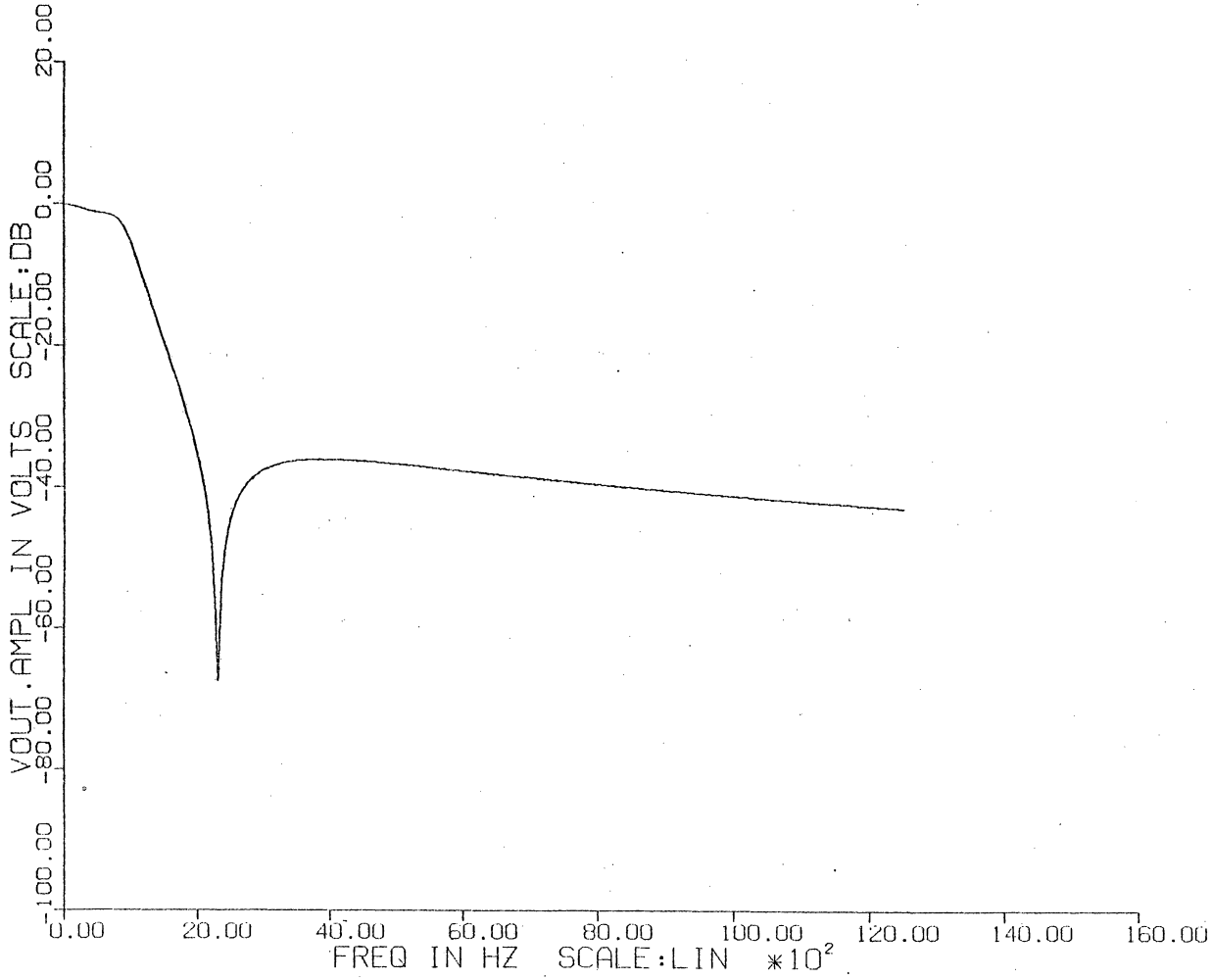


Figure 2.1-15. The wiring of Stage 5 to Stage 7 (shown in Figure 2.1-16) was checked with this computer plot from DIANA.

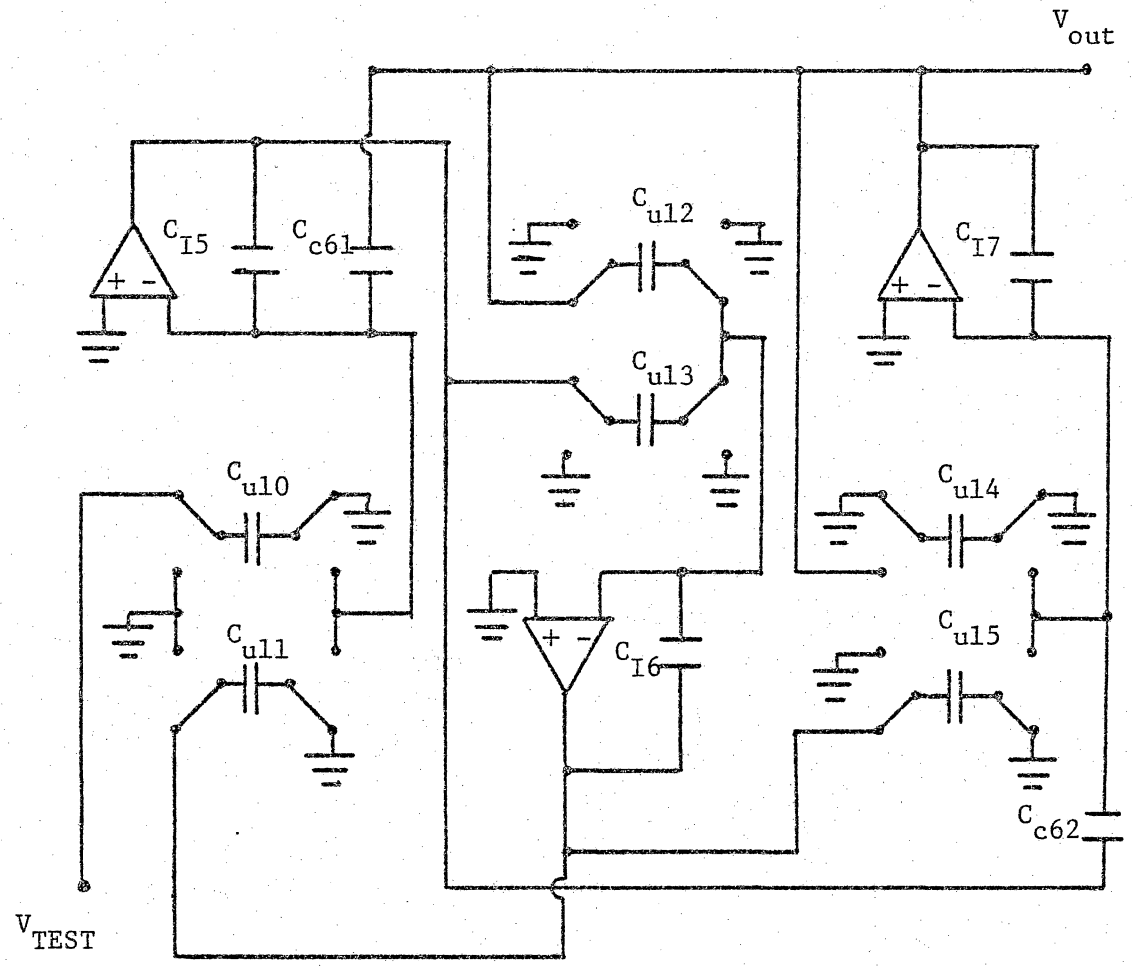


Figure 2.1-16. Connections on the scaled-filter to test Stage 5 to Stage 7.

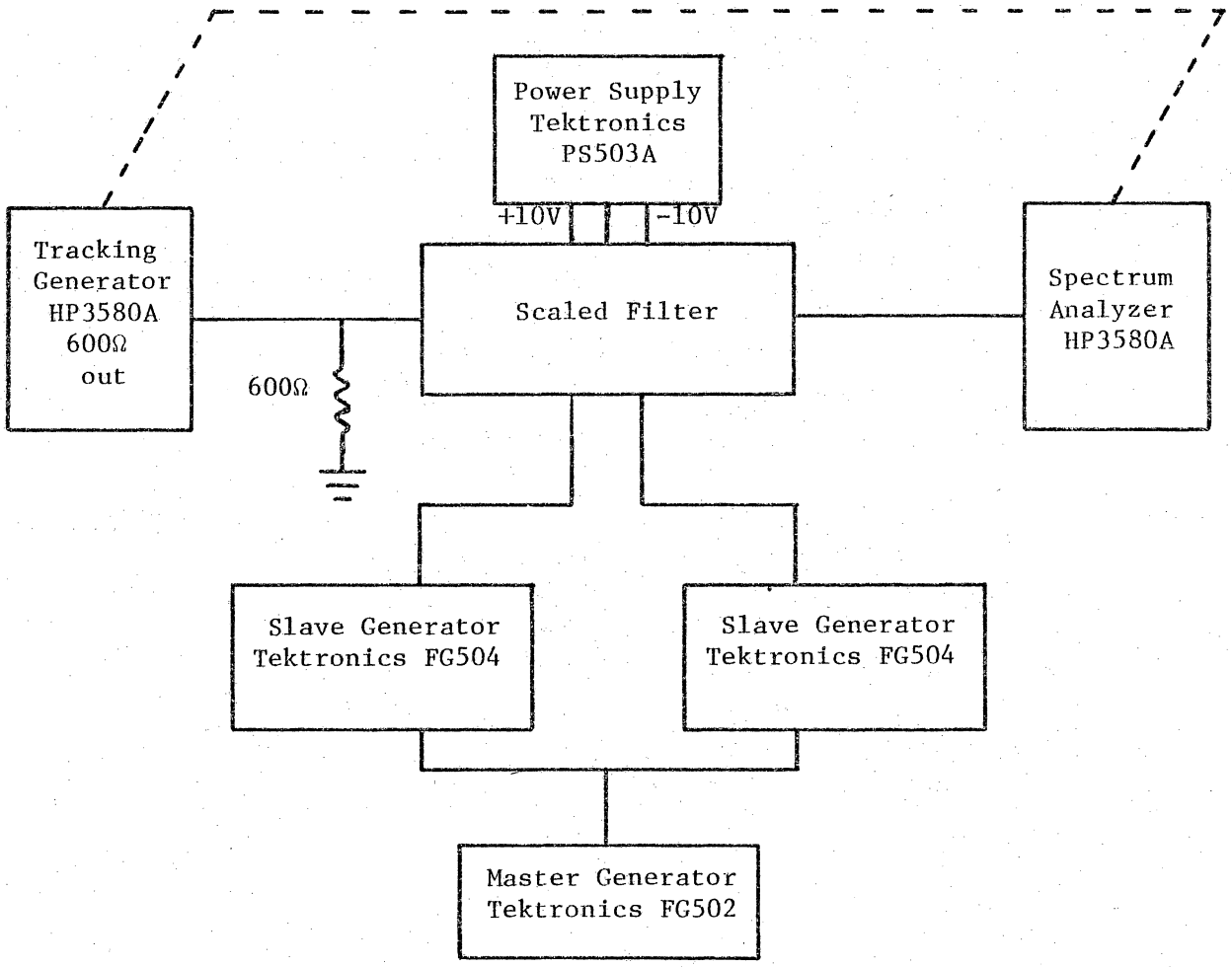


Figure 2.1-17. Test schematic for the scaled filter.

The relative phase between the clocks can be set with an accuracy of two percent due to the limitations of measuring the phase on an oscilloscope. Initially, this accuracy was thought to be acceptable, but during the testing, the phasing of the clocks affected the filter performance. A digital clock source, described in Appendix 4, was constructed to solve this problem.

2.2 The Reticon Filter

2.2.1 Design Differences

The Reticon filter design (Figure 2.2-1) became available approximately one year after the scaled filter was designed, constructed, and tested. The passive prototype used in the Reticon filter was known previously, but not the exact topology of the circuit. Inevitably, differences between designs occurred and these will be documented in this section.

The first difference is in the Reticon SFG shown in Figure 2.2-2. V_2', V_3, V_6', and V_7 are negated in the breadboard, while only V_3 and V_7 are negated in the Reticon filter. The result of negating additional nodes is to shift the locations of differential integrators in the filter. In both designs, there are two differential integrators: the Reticon filter has them in stages 3 and 5, while the scaled capacitor filter has them in stages 1 and 7 (compared Figure 2.2-2 with Figure 2.1-10). Reducing the number of differential integrators might possibly improve the filter's performance with low signal-to-noise ratios since low signal levels resulting from a difference operation might be

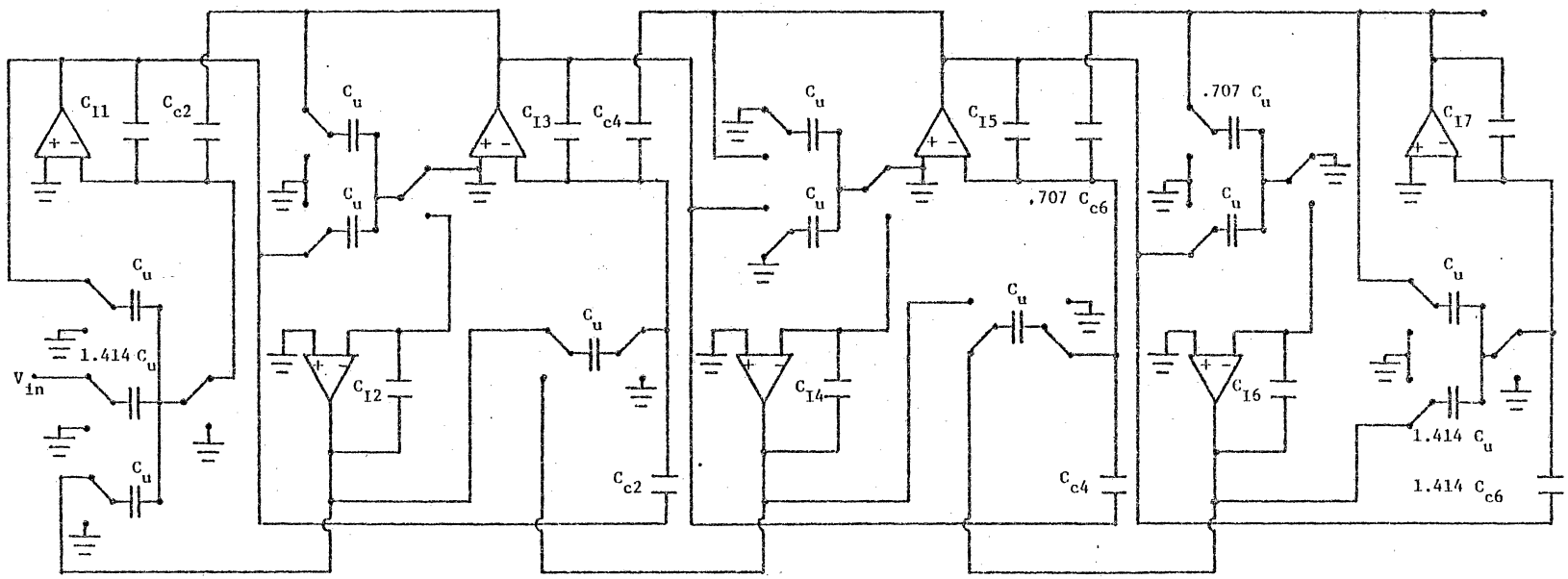


Figure 2.2-1. The schematic of the Reticon SCF.

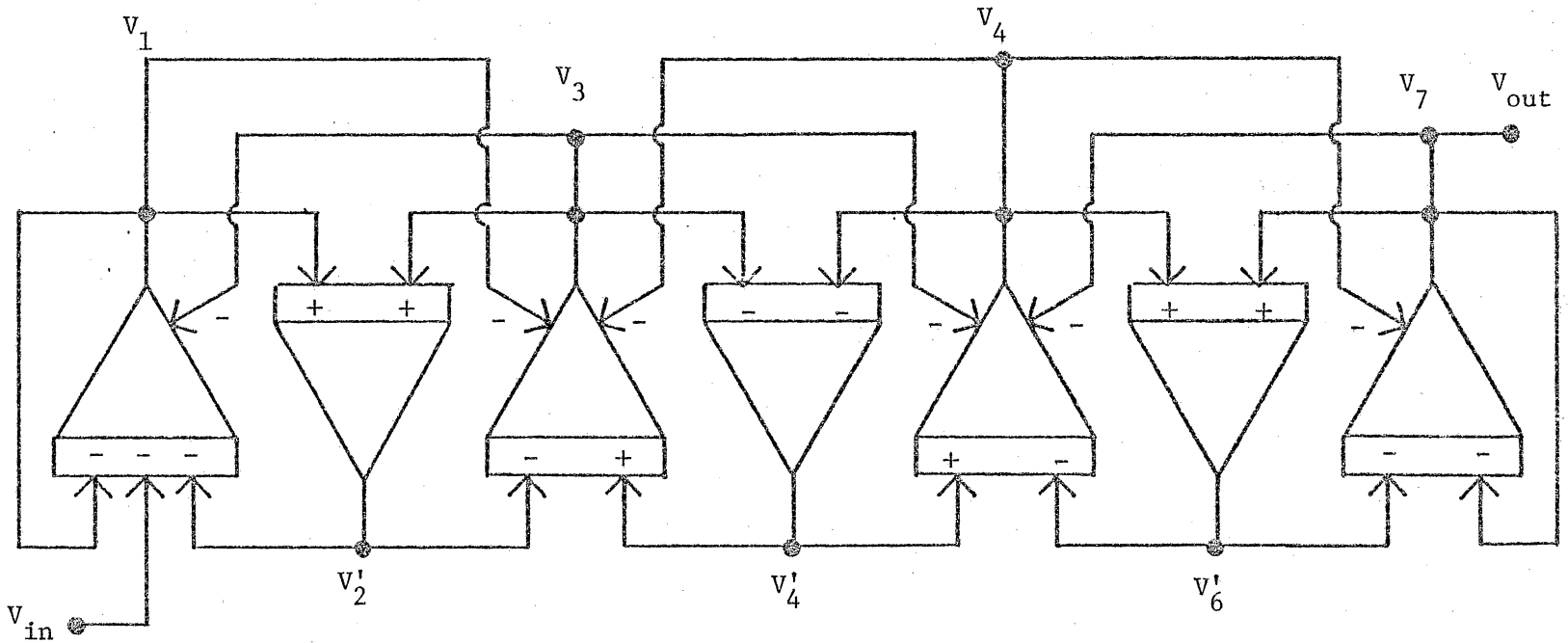


Figure 2.2-2. V'_2 and V'_6 are not negated in the Reticon filter as they were in the scaled filter.

eliminated. However, the performance effect of changing the location of the differential integrators was not investigated.

Another difference between the two filters is the number of switches in the Reticon filter is reduced by combining the operation of switches as shown in Figure 2.2-3. This option was considered in the design of the breadboard but was avoided since it could greatly complicate troubleshooting. Reducing the number of switches will improve the performance of the Reticon filter by eliminating switch noise sources. This would be a negligible improvement since the switch noise contributes very little to the total filter noise.

The third difference between the two filters is the specification of the cutoff frequency, which ultimately resulted in the Reticon filter capacitor ratios being nine percent higher than the SCF ratios. f_{co} was defined at -3.0 dB from the maximum for the Reticon filter; at -0.03 dB from the maximum for the scaled filter and the passive prototype. This resulted in the situation shown in Figure 2.2-4: the Reticon f_{co} is nine percent low according to the breadboard definition of f_{co}, while the breadboard f_{co} is approximately nine percent high according to the Reticon definition of f_{co}. In the design of the filter as discussed in Section 2.1.2.3 and Appendix 3, all capacitor ratios are proportional to f_c/ω_{co}. The need to meet different f_{co} specifications causes f_c/ω_{co} to differ for each filter and therefore the capacitor ratios will be changed as shown in Table 2.2-1.

The final design difference is that the dynamic range of the Reticon filter is not completely maximized. In the scaled filter, all the

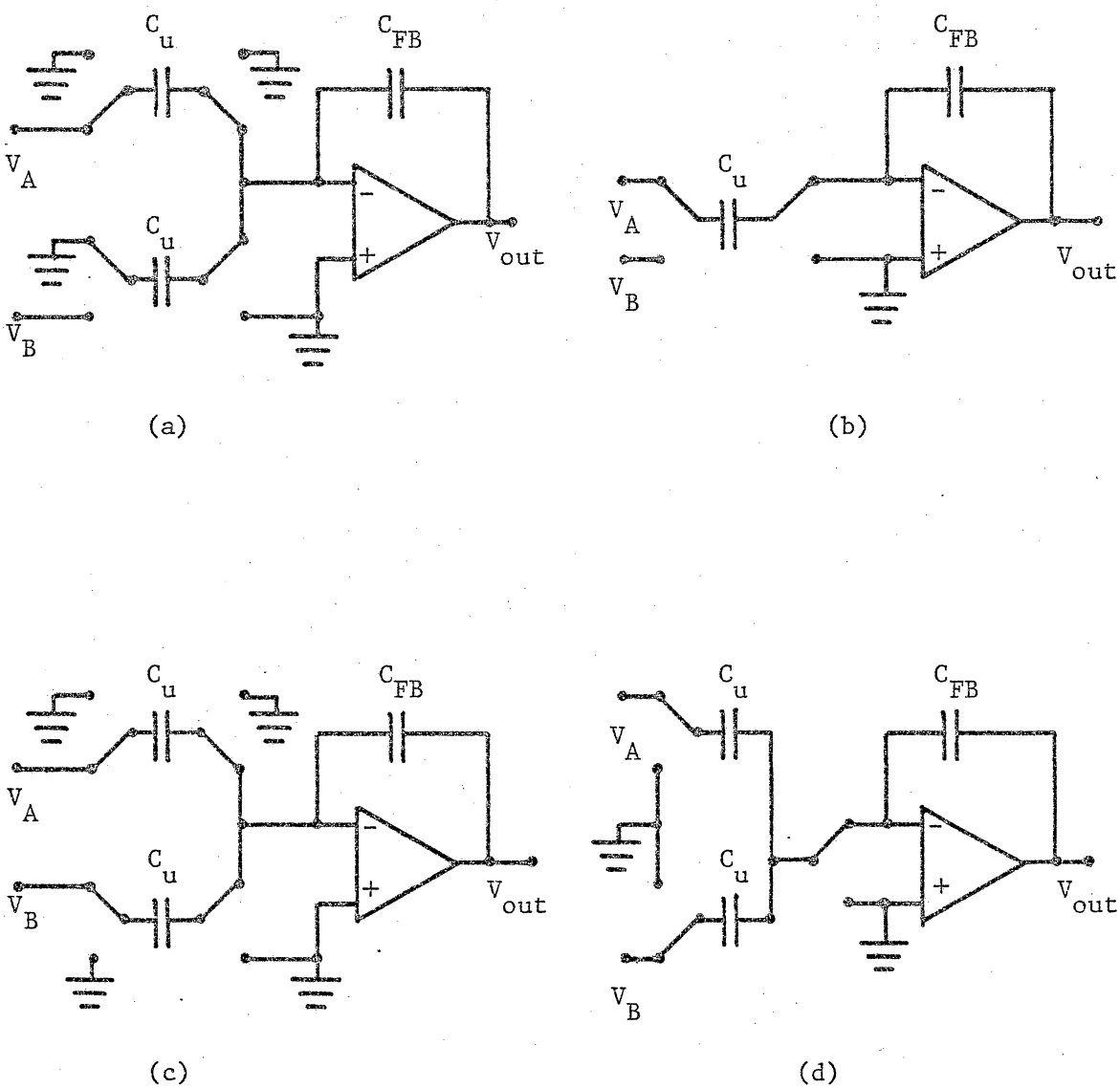


Figure 2.2-3. Typical examples of the switch reduction in the Reticon filter: the integrators of (a) and (c) are replaced by (b) and (d), respectively.

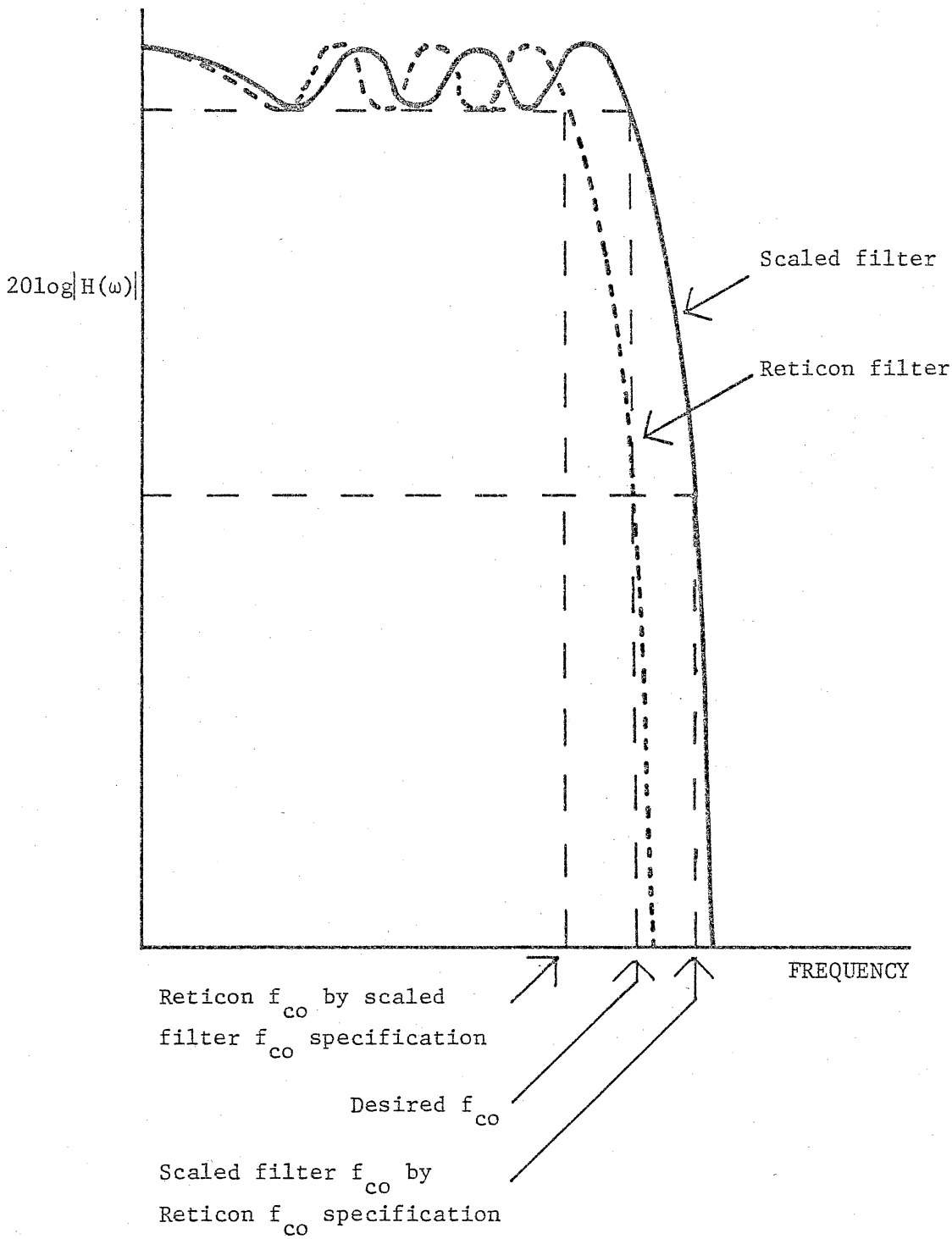


Figure 2.2-4. The different f_{co} specifications causes the Reticon filter to have a lower f_{co} than the scaled filter.

Table 2.2-1. The scaled filter capacitor ratios are 9% larger than the Reticon filter capacitor ratios

Capacitor Ratio	Scaled Filter Value	Reticon Filter Value	Reticon Value / Scaled Value
$\frac{C_{I1}}{C_u}$	7.509	8.183	1.090
$\frac{C_{I2}}{C_u}$	10.945	11.933	1.090
$\frac{C_{I3}}{C_u}$	15.397	16.779	1.090
$\frac{C_{I4}}{C_u}$	10.708	11.669	1.090
$\frac{C_{I5}}{C_u}$	15.729	17.153	1.091
$\frac{C_{I6}}{C_u}$	9.767	10.650	1.090
$\frac{C_{I7}}{C_u}$	7.602	8.285	1.090
$\frac{C_{C2}}{C_u}$	.371	.404	1.09
$\frac{C_{C4}}{C_u}$	1.681	1.832	1.090
$\frac{C_{C6}}{C_u}$	1.255	.967[1] 1.934[1]	.771[2] 1.542[3]

[1] Due to the dynamic range adjustment on the Reticon filter, there are two values for C_{C6}.

[2] $.771 = \frac{1.090}{\sqrt{2}}$

[3] $1.542 = \sqrt{2}\ (1.090)$

branch gains are modified so that all of the integrator outputs will have the same maximum voltage. In the Reticon filter, only the last stage is modified, by multiplying all the inputs to the seventh stage by $\sqrt{2}$ and multiplying all the outputs from the seventh stage by $\frac{1}{\sqrt{2}}$ As shown in Figure 2.2-5, the $\frac{1}{\sqrt{2}}$ factor on the branch connecting V_7 to V_{out} is transferred to the branch connecting V_{in} to V_0, so that the filter will remain canonical.

In view of the small size of the unit capacitor (~0.2 pF), it would probably be very difficult to obtain the multiple unit capacitor values required by a complete dynamic range optimization in an integrated circuit. Thus, only the seventh stage is modified. The lack of a complete dynamic range maximization should cause its dynamic range to be less than that of the scaled filter.

2.2.2 Reticon Filter Test Fixture

The schematic for the Reticon test fixture is shown in Figure 2.2-6. The tracking generator, spectrum analyzer, and power supply are the same ones used to test the scaled capacitor filter. The clock source is a CD4047 chip instead of the clocking arrangement used for the scaled capacitor filter. The components are mounted in IC sockets on a printed circuit board.

2.3 Filter Tests [32]

2.3.1 Out-of-Band Rejection (OBR)

OBR is the minimum attenuation of signals in the stop band relative to the peak signal level in the passband as shown in Figure 2.3-1.

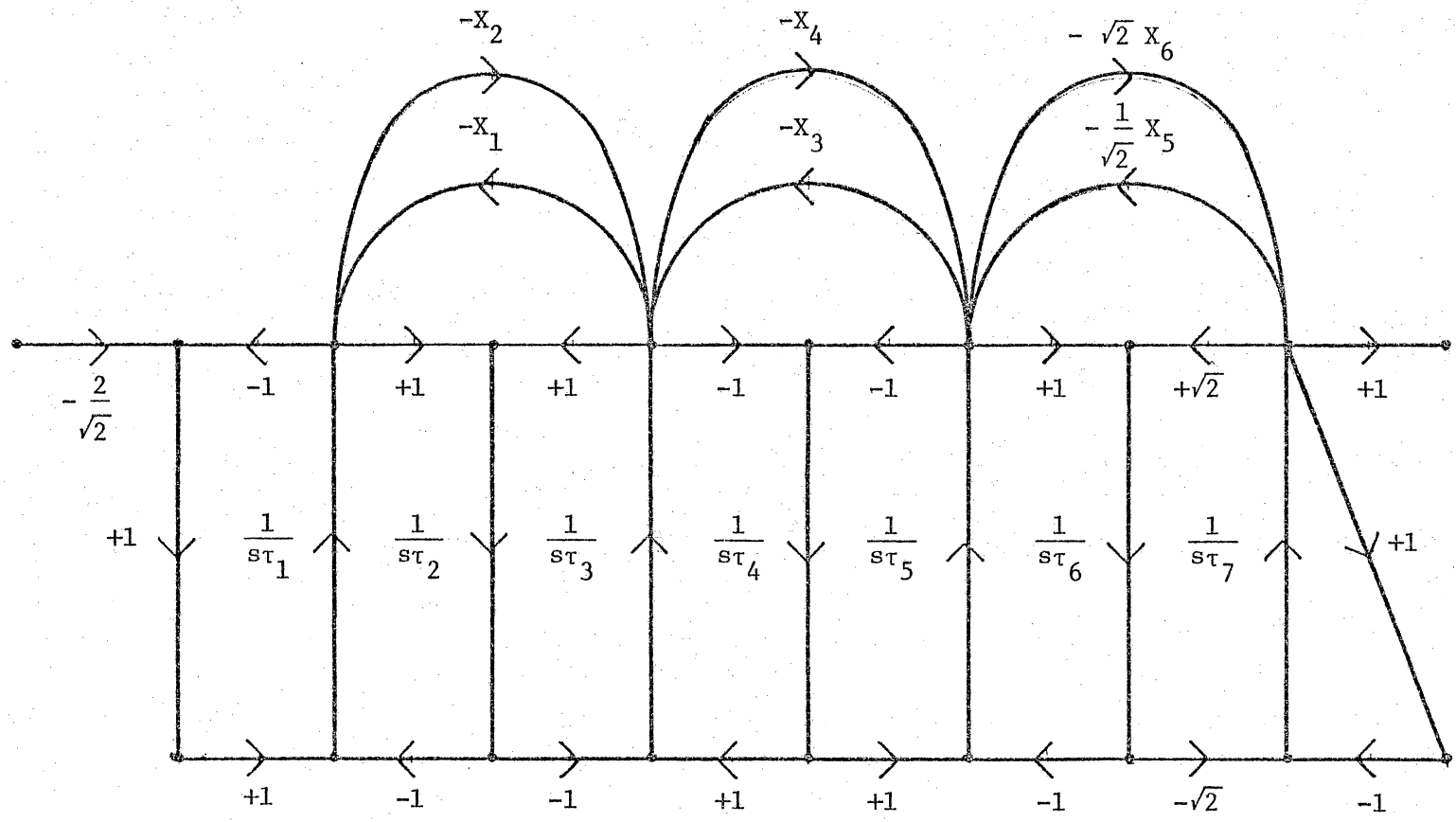


Figure 2.2-5. The gains of the last stage were adjusted by $\sqrt{2}$.

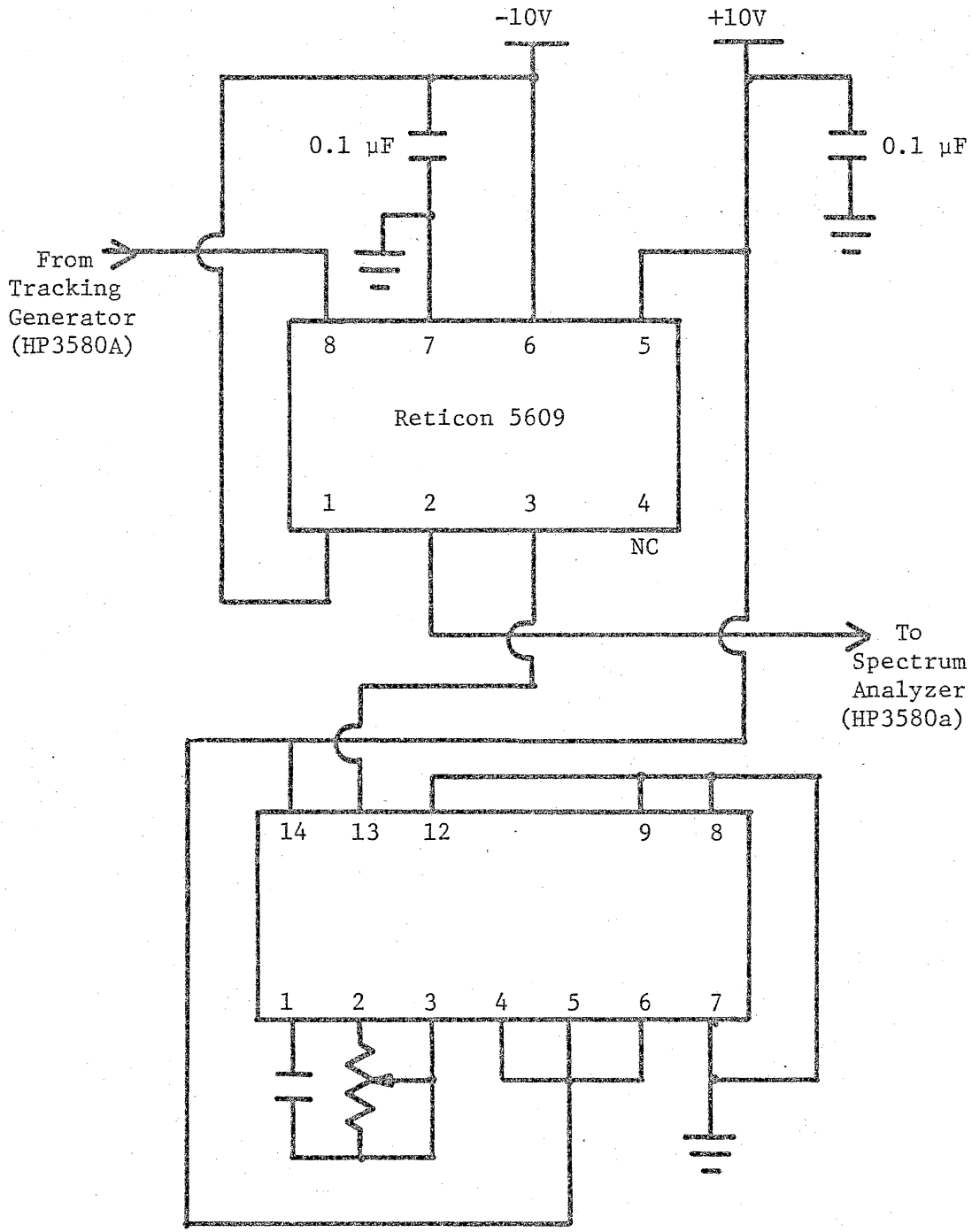


Figure 2.2-6. The test schematic for the Reticon filter.

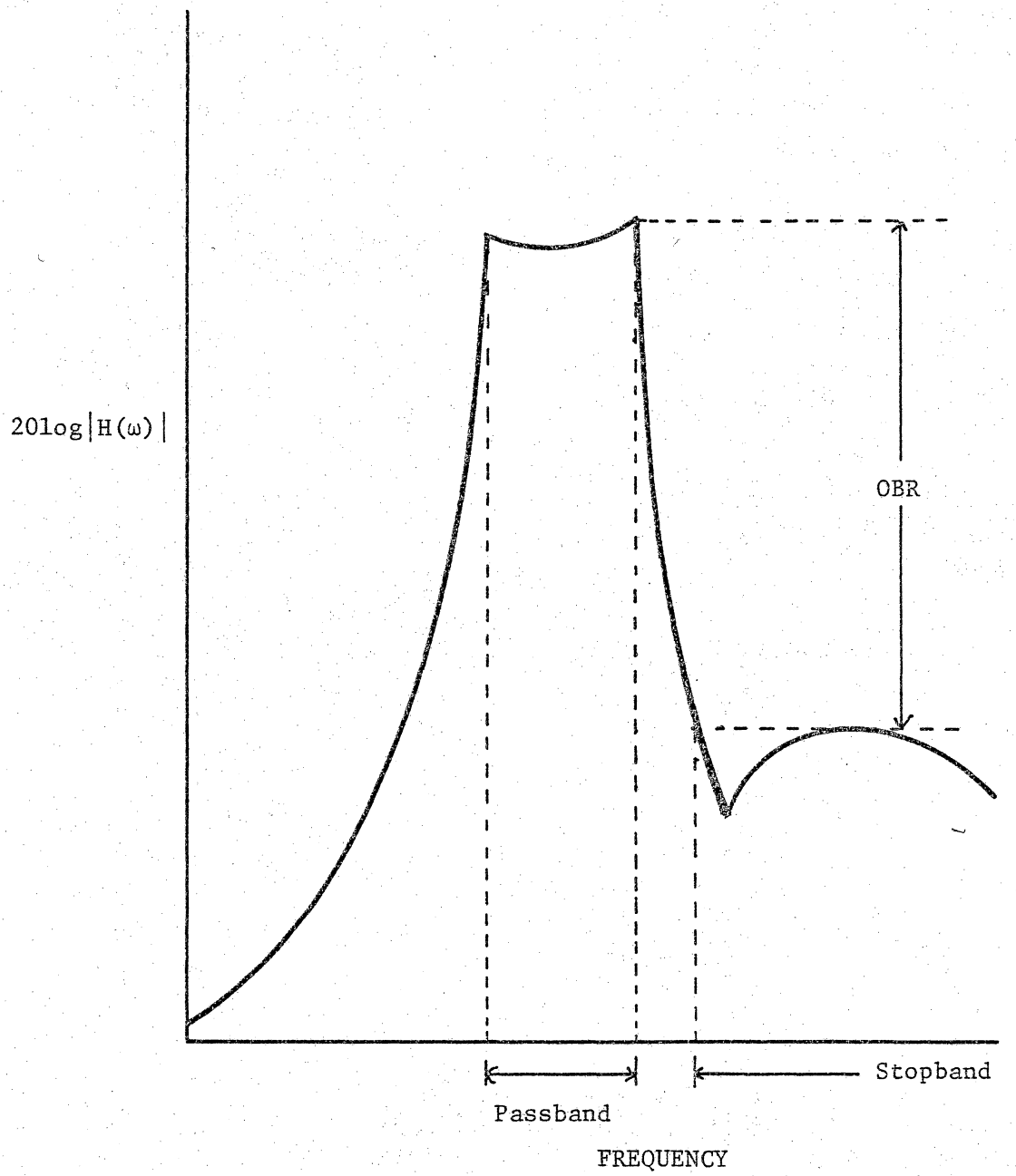


Figure 2.3-1. The definition of OBR used in testing the SCFs.

OBR is limited by:

1) filter self noise
2) input to output feed through in the filter and test setup
3) imperfect grounding
4) round-off errors of filter coefficients in finite impulse response filters.

2.3.2 Dynamic Range (DR)

DR is the maximum signal-to-noise ratio possible with a single tone input in the passband such that harmonic distortion components generated by the filter do not exceed the filter's noise floor level. Although Figure 2.3-2 only shows DR as the ratio of fundamental to second harmonic, the measurement is referred to the harmonic with highest level generated by the filter. A test signal frequency is usually selected to be in the center of the filter's passband. A high quality signal (at least 82 dB harmonic suppression) must be used so that its harmonics do not mask those produced by the filter.

2.3.3 Device Noise Floor (DNF)

DNF is the maximum noise level measured at the filter output with the filter input grounded, relative to the passband signal level. If the spectrum shows peaks in the noise floor due to peaks in the filter response, the highest one is taken as the DNF (see Figure 2.3-3).

2.4 Test Results

The responses of the Reticon filter and the scaled capacitor filter, in Figures 2.4-1 and 2.4-2, show good replication of the

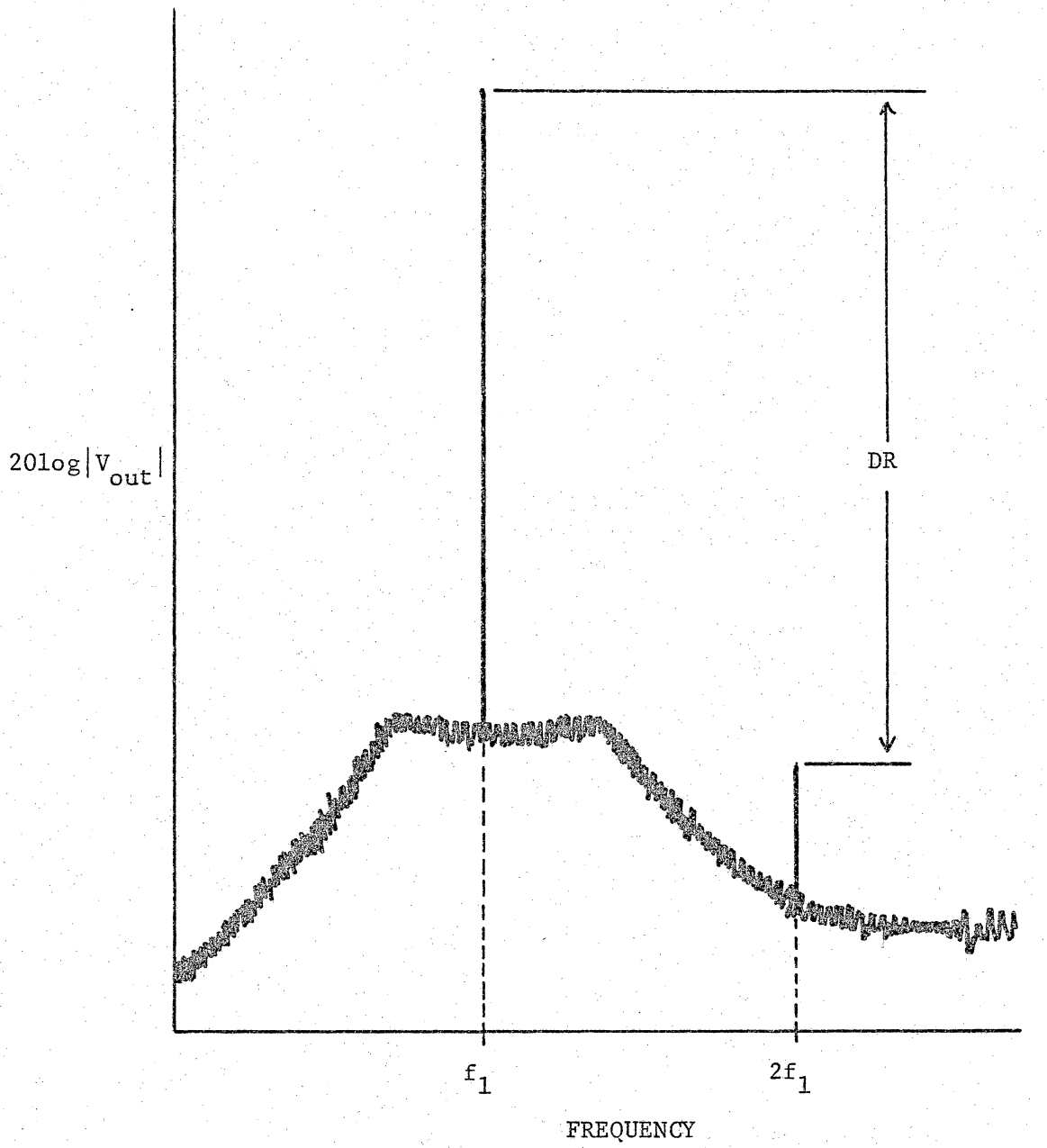


Figure 2.3-2. The dynamic range test.

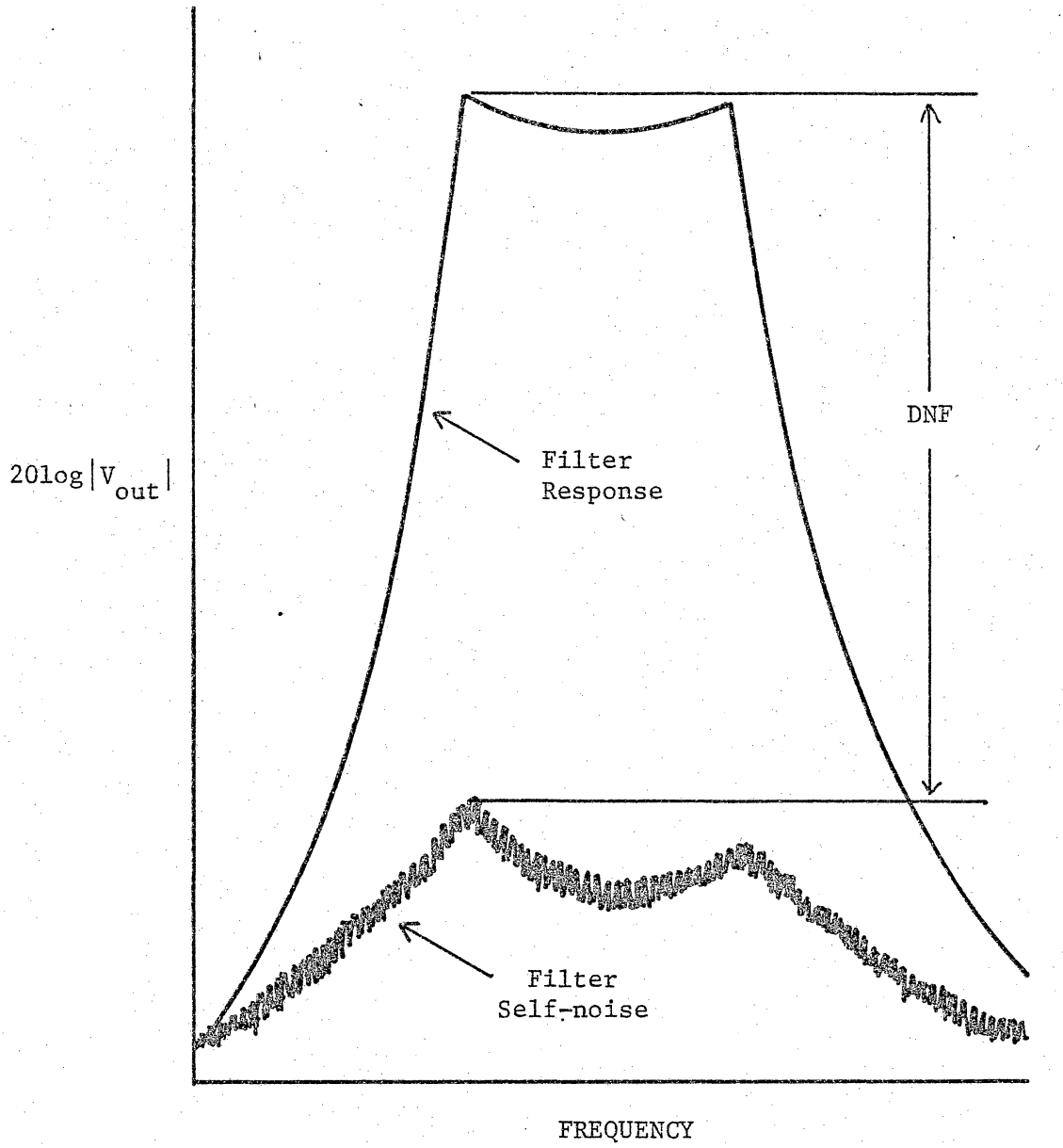
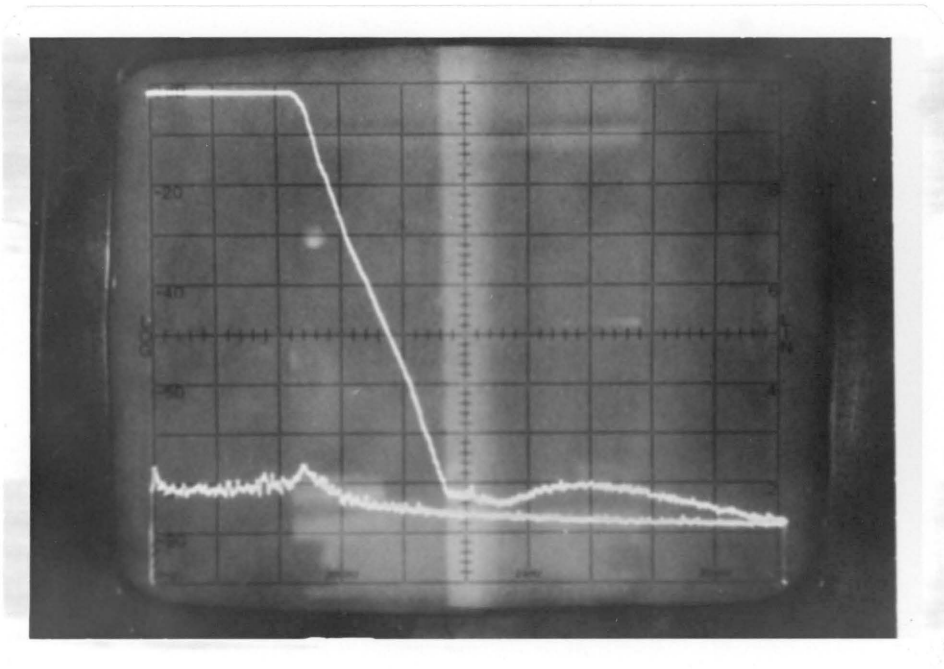
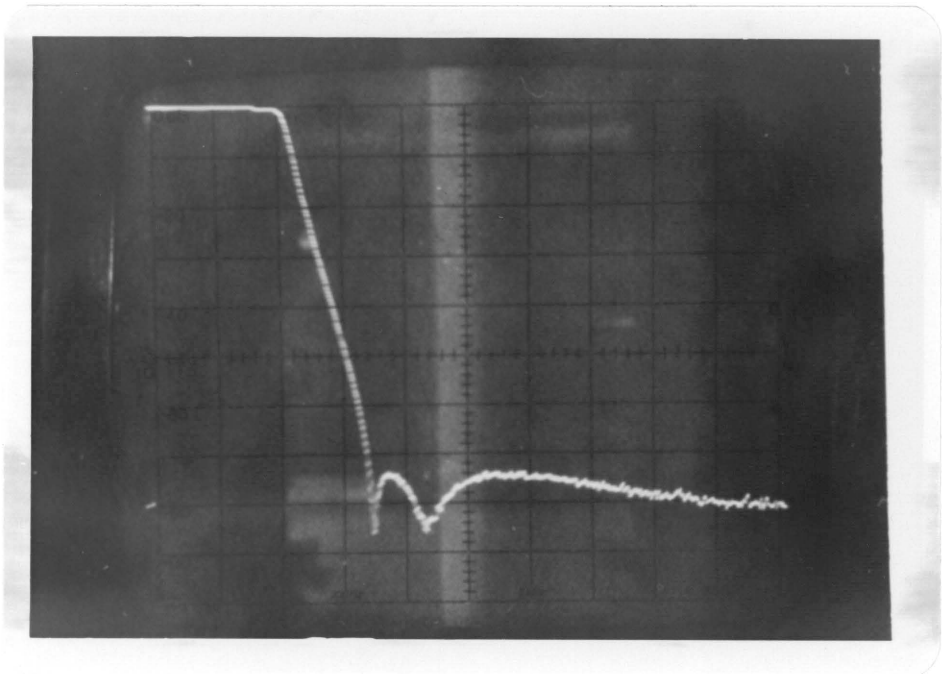


Figure 2.3-3. The device noise floor definition.



Reference Level	0 dB
Amplitude Scale	10 dB/div
Start Frequency	0 kHz
Frequency Scale	200 Hz/div
Resolution Bandwidth	10 Hz
f_{clock}	50 kHz

Figure 2.4-1. The response of the Reticon filter.



Reference Level	0 dB
Amplitude Scale	10 dB/div
Start Frequency	0 kHz
Frequency Scale	1 kHz/div
Resolution Bandwidth	30 Hz
f_{clock}	100 kHz

Figure 2.4-2. The response of the scaled-capacitor filter.

passband characteristics. However, the Reticon filter never displayed the stopband notches, which are clearly seen in the response of the breadboard. Reticon engineers also have not obtained the stopband notches in the integrated filter. The numerical comparison of the filter responses shown in Table 2.4-1 is approximate because the measurements were taken from the spectrum analyzer. A point-by-point measurement of the filter response would give more accurate results, but this was considered to be unnecessary in the context of this thesis. Additional test results for dynamic range and device noise floor are also presented in Table 2.4-1.

Some unexpected observations were made on the scaled capacitor filter. As the relative phase between non-overlapping clocks was changed, the stopband characteristics of the filter were altered. Notches would disappear or shift in location, as shown in Figure 2.4-3.

2.5 Differences in Results

The test results of the Reticon filter and the scaled filter show some slight differences. A possible reason for the missing notches in both filters is signal feedthrough in the test setup, either by coupling from the input to the output or through the power supply. Another possible cause for the missing notches in the Reticon filter is the partial DR optimization and the higher op-amp noise.

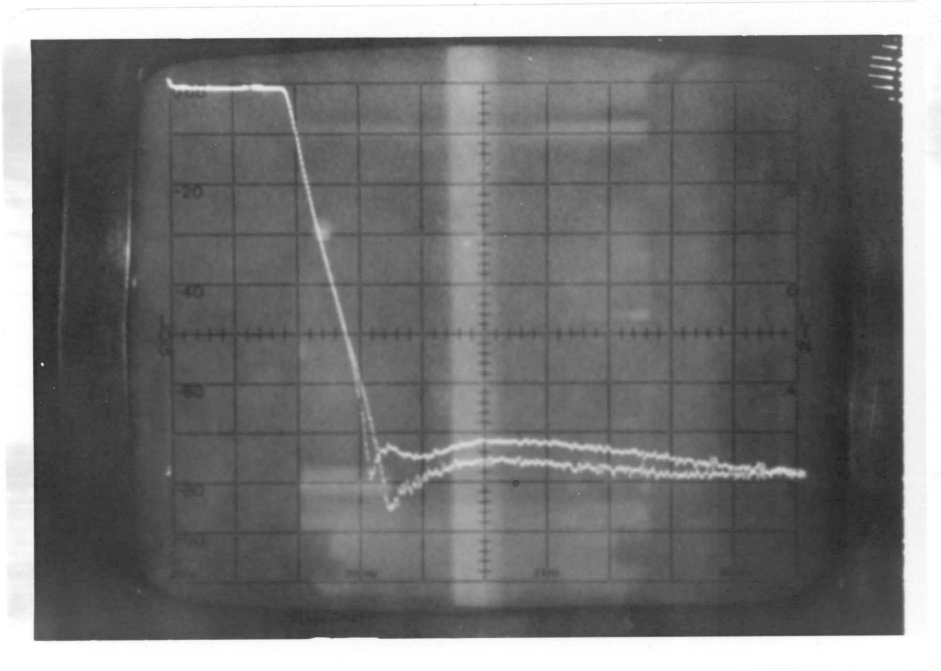
Signal feedthrough also contributed to the discrepancies in OBR for both filters. The Reticon filter's OBR is particularly sensitive to the power supply by-passing; differences of 10 and 20 dB have been

Table 2.4-1. A comparison of the scaled filter, the Reticon filter, and computer simulation.

f_c = 50 kHz f_{co} = 1 kHz	Scaled Filter	Computer	Reticon Filter
Passband Loss (DB)	0	0	1
Passband Ripple (DB)	0.2	0.081	0.4
Out-of-Band Rejection	78	82	79
Cut-off Frequency	1.0	1.0	0.94
First Notch	1.73	1.88	-(1)
Second Notch	2.15	2.27	-(1)
Third Notch	-(1)	3.95	-(1)
Dynamic Range (DB)	64	-(2)	62
Device Noise Floor ($DB/\sqrt{Hz}$)	100	-(2)	87

(1) Notches did not appear.

(2) No theoretical comparison of DR and DNF due to need for nonlinear modelling (DR) and noise analysis (DNF).



Reference Level	0 dB
Amplitude Scale	10 dB/div
Start Frequency	0 kHz
Frequency Scale	2 kHz/div
Resolution Bandwidth	100 Hz
f_{clock}	170 kHz

Figure 2.4-3. The result of changing the relative phase between $\emptyset_1$ and $\emptyset_2$ on the scaled filter.

noted with different by-pass networks. IBM engineers have independently confirmed this observation.

Ripple in the passive prototype is specified as .03 dB, but due to the digital nature of the SCF, DIANA predicted a ripple of .081 dB. The DIANA passband isn't equiripple, so the ripple is measured from the passband minima to the passband maxima. Further investigation of the increased ripple showed that if the seventh order filter is designed with higher values of f_c/f_{co}, the ripple extremes decreased. Furthermore, the passbands tended to become equiripple as shown in Figures 2.5-1 and 2.5-2. These observations show that the increased ripple is a second order effect of the digital nature of a SCF. The ripple of both the Reticon and scaled filters is much greater than the DIANA predictions. The causes of this increase are not within the bounds of this project and need to be investigated further.

When the notches are present in the scaled filter, the maximum error their location is 8% as compared to the computer predictions.

The cutoff frequency of the Reticon filter is 6% low at 940 Hz. According to the computer predictions, the Reticon cutoff frequency should be at 927 Hz or 7.3% low. This error is within the accuracy of the spectrum analyzer.

The lower noise floor of the scaled filter is due to its bipolar op amps. The Reticon filter uses the comparatively noisy MOS op amps.

The scaled filter's DR is 2 dB greater than that of the Reticon filter. This improvement should be greater in view of the lower noise amplifiers and the DR optimization of the scaled filter. Possibly,

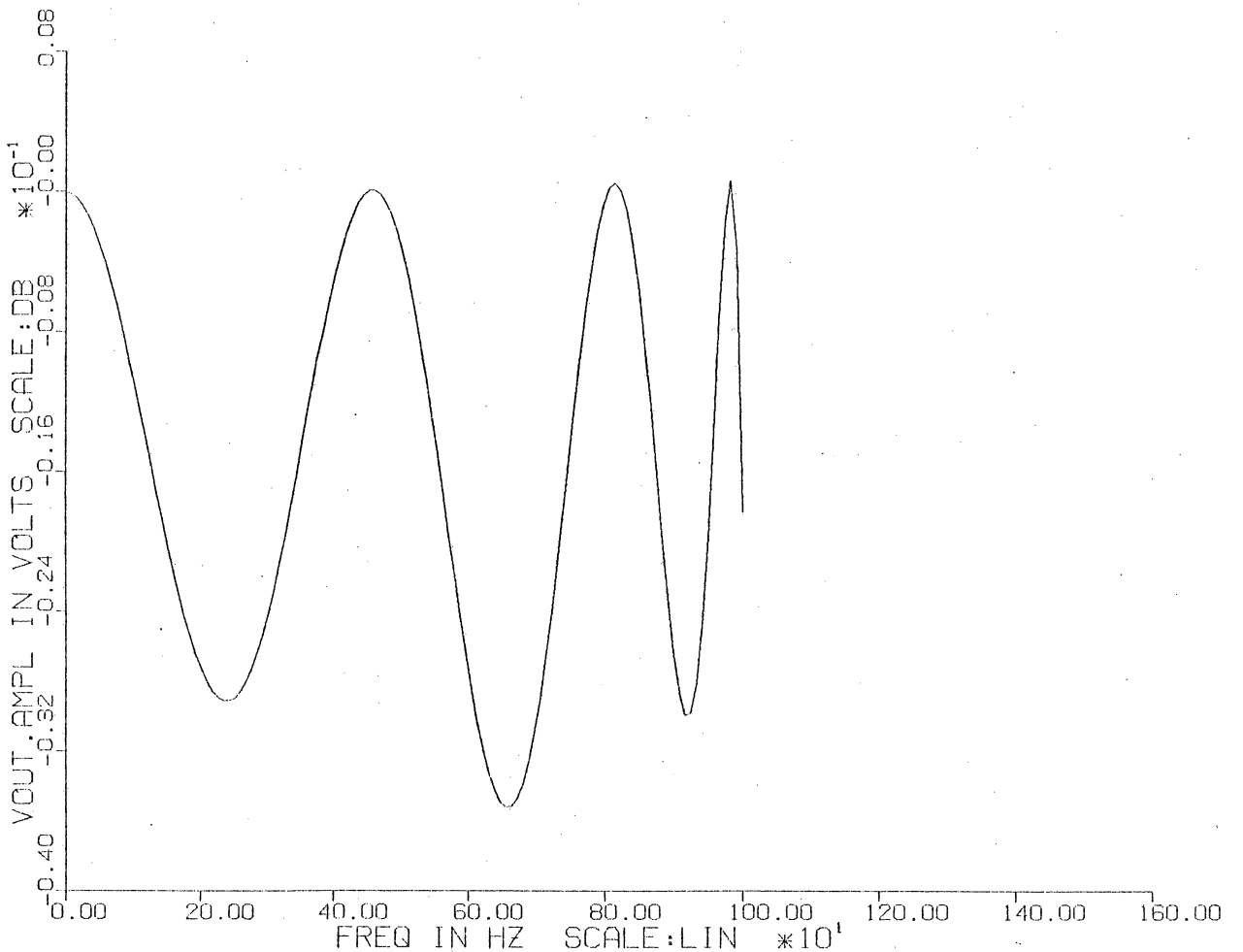


Figure 2.5-1. The passband of the seventh order filter with f_{clock}/f_{co} = 200.

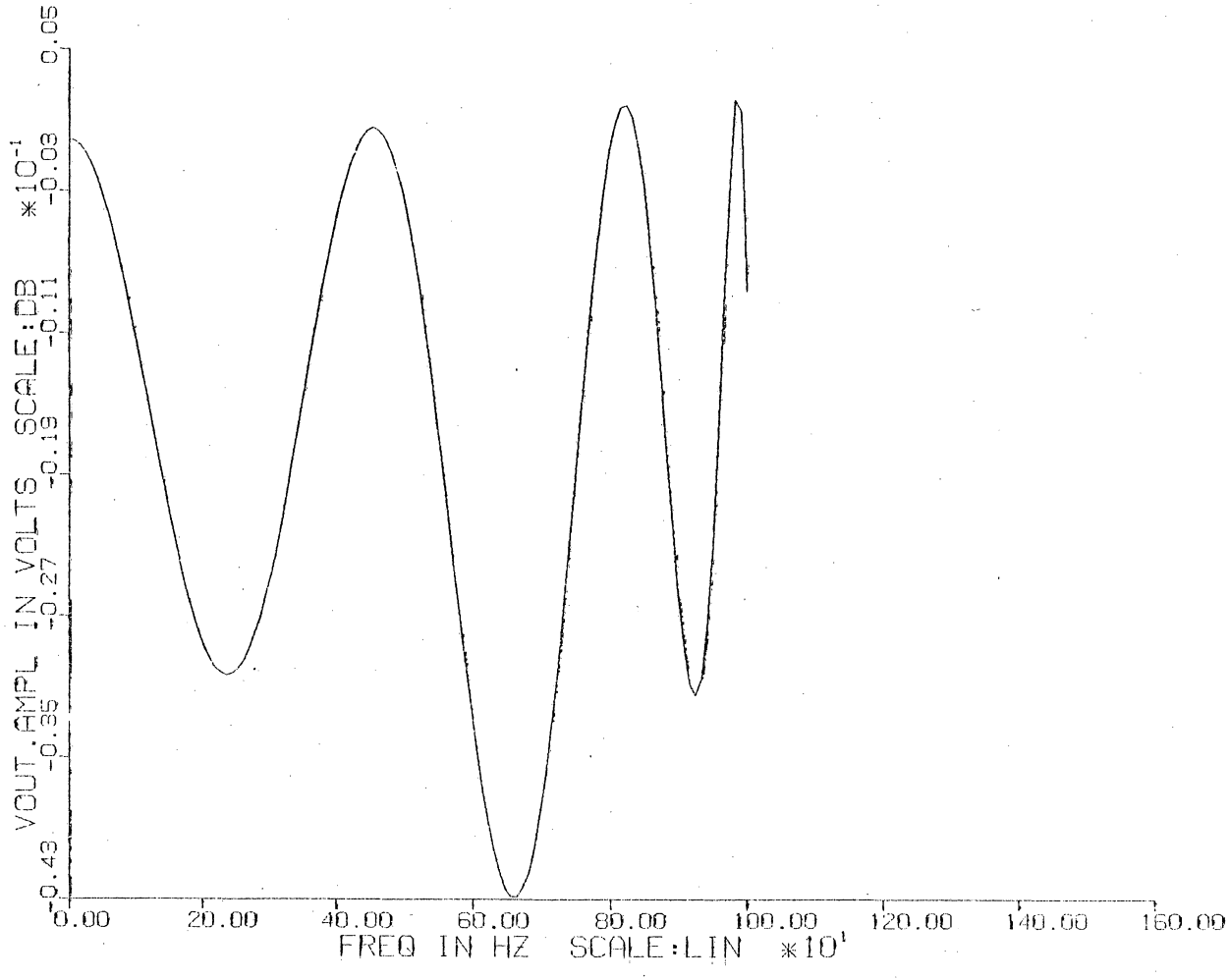


Figure 2.5-2, The passband of the seventh order filter with $f_{clock}/f_{co} = 100$,

the different filter topologies might prevent the scaled filter's DR from being much better.

A scaled filter has been constructed according to the same passive prototype used by the Reticon filter. The scaled filter met the original design specifications better than the Reticon filter because an exact replication of the Reticon was not possible. Some of the reasons for this were: the exact topology of the Reticon filter was unknown; the values of parasitics were unknown; capacitor ratios could not be accurately set with small values of discrete capacitors. However, the results show that a breadboard of a high order SCF can give very close results to the original design values. If the parasitic values and design constraints of the Reticon filter had been known, it would be reasonable to expect that the performance of the integrated filter could be predicted from the breadboard performance.

CHAPTER 3. SCF COMPUTER PACKAGES

Computer modelling is very useful in several stages of SCF design. The first stage is checking the passive prototype or the original active RC filter to ensure that the specifications of the SCF are met. This level of modelling requires conventional components such as inductors, capacitors, resistors, dependent sources and independent sources. Standard circuit analysis programs are readily available to perform this task.

A second use for computer modelling is to check the topology of the switched capacitor circuit. Ideal switches, capacitors, and amplifiers model the filter to determine whether the signal flow graph has been properly derived and also to check for proper switch phasing. The overall conversion of the passive prototype to a SCF is thereby verified. At this second level of modelling, a digital network is simulated with analog elements; charge is transferred from one capacitor to another in a step-wise fashion as in a digital circuit, yet ideal analog components are used. In conventional circuit analysis programs, the lack of a switched capacitor makes the simulation very awkward at best. An additional problem is that two frequencies are used in the filter: one for the signal, and the other for the clock. This requirement renders most computer packages which operate in the frequency domain unsuitable for switched capacitor analysis.

The third use for computer modelling in the design of SCFs is the analysis of second-order effects due to the non-ideal nature of components. Switch resistance, gain-bandwidth product of the op amp,

and input resistance of the op amp are some of the considerations which affect the filter performance. These second-order effects are of particular importance to the IC designer since one of his main constraints is minimum circuit size. The modelling at this level is more difficult since it can no longer be assumed that the capacitors transfer change instantaneously and RC time constraints must therefore be accounted for.

A fourth level of computer simulation is to analyze the non-linear effects in SCFs, such as dynamic range, intermodulation distortion and slew rate limiting of the op amps. No programs are available at present which incorporate non-linear models, so this level will not be discussed.

A number of SCF programs have been mentioned in the literature:

1) DIANA [27]: widely regarded as the most powerful program available; capable of yielding frequency response (magnitude and phase), sensitivity, and allowing variation in the gain and gain-bandwidth product of the amplifiers. This package can perform the second and third levels of simulation.
2) SPICE 2 [28]: time domain and frequency domain analysis; used to check design prototypes; otherwise of very limited value for SCF design.
3) ISCAP [29]: utilizes CAPECOD for circuit simulation, optimization and tolerance analysis. Useful only for checking ideal SCF.

4) SCAP I & II [30]: (a) SCAP I utilizes block partitioned macro-models; capable of analyzing a restricted class of structures; computationally more efficient than SCAP II. (b) SCAP II utilizes modified nodal analysis (MNA); more general than SCAP I. Both of these programs assume only an ideal SCF.

Of these programs, DIANA and SPICE were readily available. Also, an expanded version of TCAP [31], TCAPS (Transient Circuit Analysis Program for Switched-Capacitor Networks), was available for the simulation of SC networks.

The purpose of this chapter is to highlight the capabilities and limitations of SPICE II, DIANA, and TCAPS in SCF simulation and design. The end goal is not a detailed comparison to determine which program is "best" or "most accurate", but rather to understand how these three programs work and how they might be used in a design sequence.

3.1 SPICE II

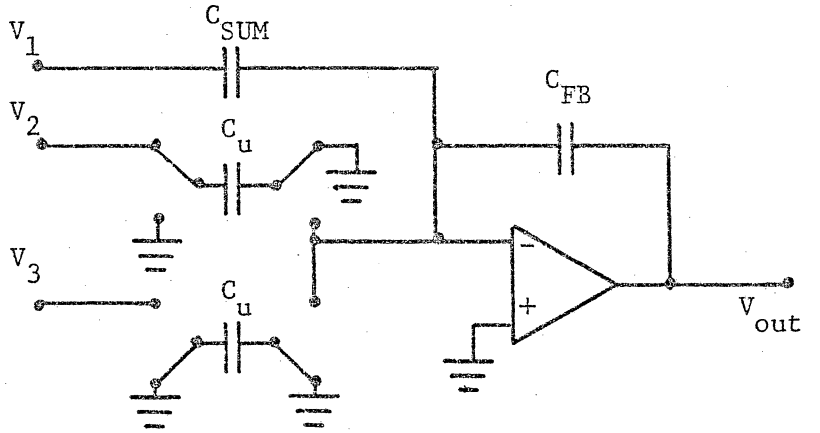
SPICE is the well known circuit analysis program originally developed for simulation of integrated circuits. It can be used in SCF design to check the passive prototype or the original active RC filter in the time domain or frequency domain. As mentioned previously, since SCFs operate with two frequencies, (the clock and signal frequency), SPICE cannot perform a frequency domain analysis of unmodified SCF.

However, it can check the development of a SCF signal flow graph. If all switched capacitors in the SCF are replaced by equivalent resistors and, where appropriate, -1 gain blocks, a topological check of the signal flow graph can be performed. In Figure 3.1-1, the SCs are replaced by resistors of value

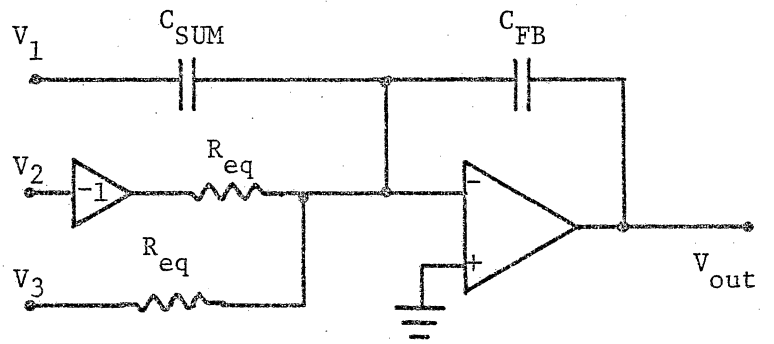
$$R_{eq} = \frac{1}{f_c C} \quad . \tag{3.1-1}$$

The V_1 input of the SC circuit is non-inverting, so a -1 gain block is inserted to make the equivalent network have a noninverting input for V_1. The integrating capacitor, the op amp, and the summing capacitor remain unchanged in the SPICE equivalent circuit. Errors due to incorrect switch phasing might not be found, and also the effects of the termination stages will not be seen. Another limitation of this method is $f_c >> f_{co}$, otherwise, Eqn. (3.1-1) is invalid and no equivalent network can be derived.

As an alternative, SPICE can model SCFs using Laker's equivalent networks [20], which replace switched capacitors with sample-and-hold elements, resistors, and capacitors. The sample-and-hold elements are modelled by lossless transmission lines [19] on SPICE. Therefore, switch phasing can be checked in addition to the topology of the signal flow graph. This approach is limited to ideal SC networks and is not a direct representation of the original network.



(a)



$$R_{eq} = \frac{1}{f_c C_u}$$

(b)

Figure 3.1-1. The original SC integrator of (a) is modelled on SPICE by the equivalent active RC integrator of (b).

3.2 DIANA

DIANA performs time domain and frequency domain analysis of analog SC and digital networks. The analog and digital simulations were not used in this project and thus will not be discussed. DIANA simulates ideal SC networks in the frequency domain by assuming that there are no time constants in the networks. As a result, DIANA is extremely fast for the simulation of ideal SC networks. When parasitic resistors are included in the simulation, a time domain simulation is performed, then the results are converted to the frequency domain via a FFT. Unfortunately, DIANA V6, the version of DIANA available for this project, could not model resistors and was limited to the analysis of ideal SC networks. DIANA V7, which was not available at the time of this project, can model resistors.

The network elements available in DIANA V6 are independent and dependent voltage sources, independent and dependent current sources, capacitors, ideal two node switched capacitors, and ideal three node switched capacitors. These elements can be combined to form new elements, called macros, for common SCF subcircuits. For example, the macro OPAMP, shown in Figure 3.2-1a, incorporates both the integrating capacitor and the op amp in one statement specifying the input terminals, the output terminals, and the capacitor value. Similarly, the switched capacitor macro, SCAB, is a series connection of two three-node SCs, with each capacitor having a value of 2C as shown in Figure 3.2-1d. These macros helped to eliminate mistakes in the transfer of a schematic to the DIANA input data file.

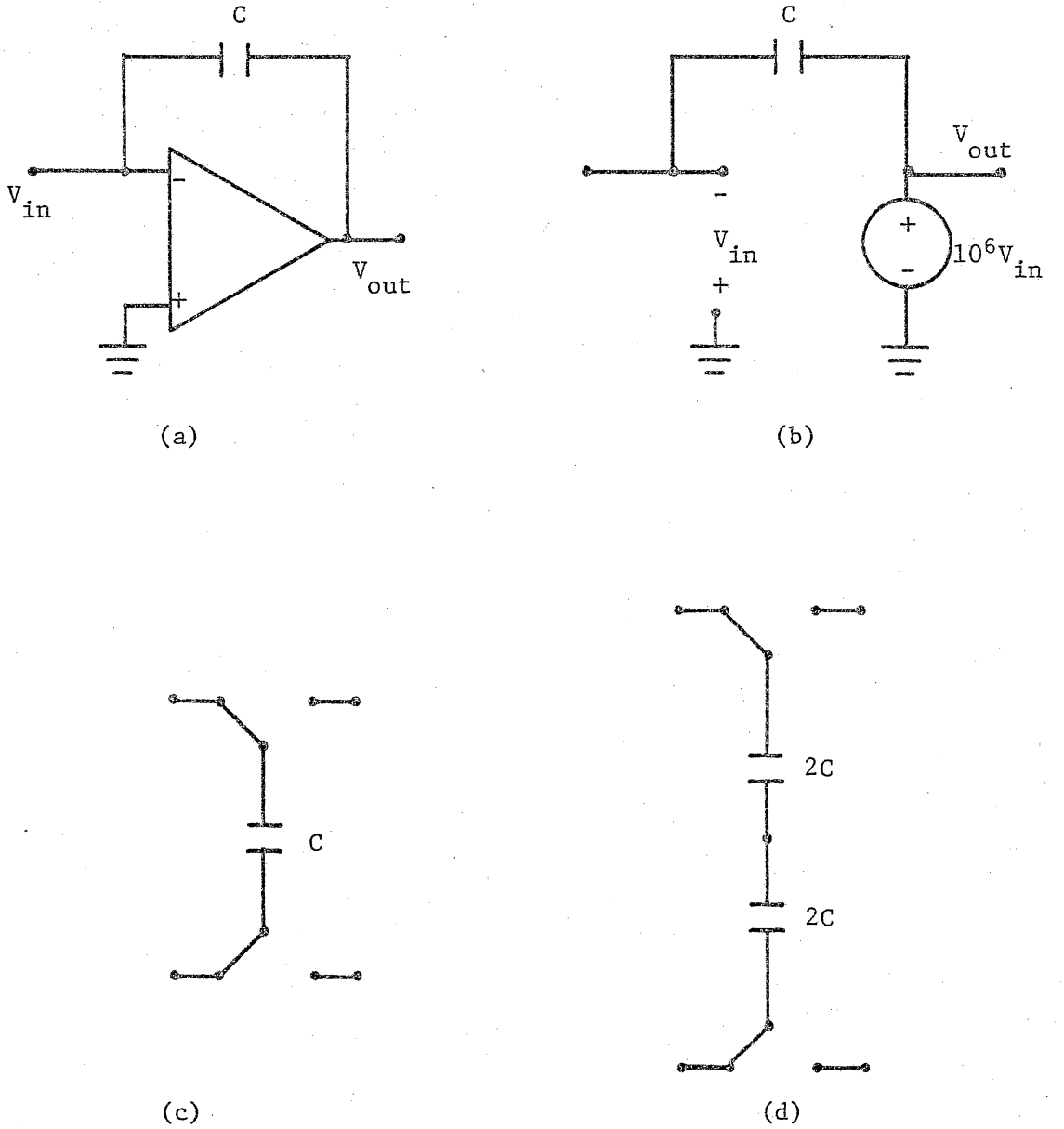


Figure 3.2-1. The DIANA macros for SCFs: an op amp and its integrating capacitor, (a), is modelled by an ideal voltage source, (b); a switched capacitor, (c), is modelled by two three-node switched capacitors, (d).

The switch phases in DIANA are controlled by two separate clocks which can have their duty cycles and relative phase set independently. In conjunction with the parasitics in DIANA V7, this feature enables the study of effects of the clock on the filter performance.

The DIANA program package consists of three main programs: MDL, DIANA, and PPR. MDL (Macro Definition Language) translates the macros used in the input file to the basic circuit elements used by DIANA. DIANA performs the processing to calculate the output data. Finally, PPR (Post Processor) prints or plots the data generated by DIANA.

Representative examples of the results of DIANA are shown in Figures 3.2-2 and 3.2-3. These are the amplitude and phase response plots for the scaled filter of Chapter 2. A comparison of DIANA with TCAPS and SPICE is presented in Section 3.4.

DIANA also has the capability to perform worst case studies of errors in capacitor values. A classical sensitivity analysis using

$$S_c^V = \frac{\frac{\partial V}{V}}{\frac{\partial C}{C}} \qquad (3.2\text{-}1)$$

cannot be undertaken since DIANA defines sensitivity as

$$S_c^V = \frac{(20 \log |V|)}{100 \cdot \frac{\partial C}{C}} \quad . \qquad (3.2\text{-}2)$$

However, an indication of filter sensitivity can be obtained using the following procedure:

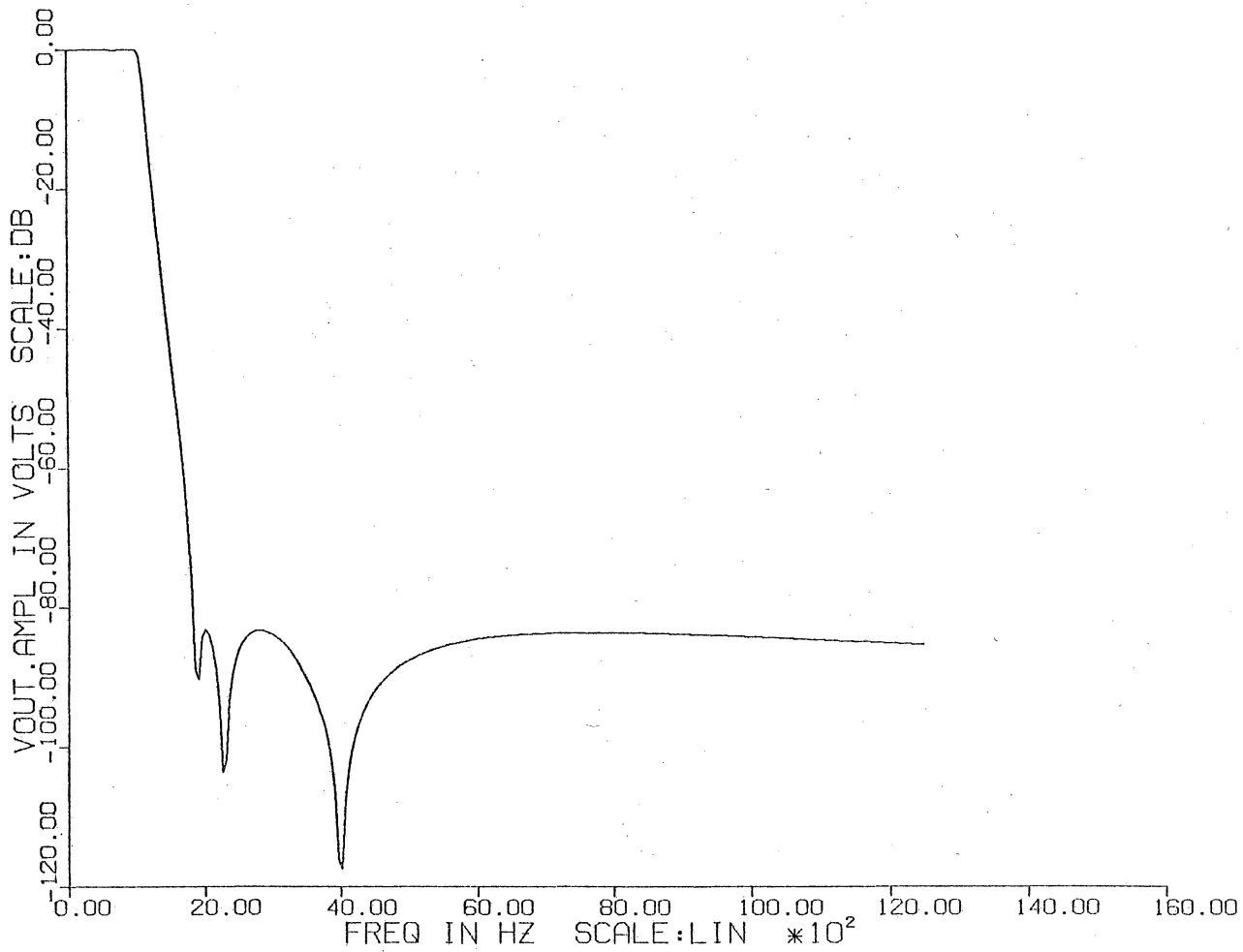


Figure 3.2-2. The seventh order filter amplitude response predicted by DIANA.

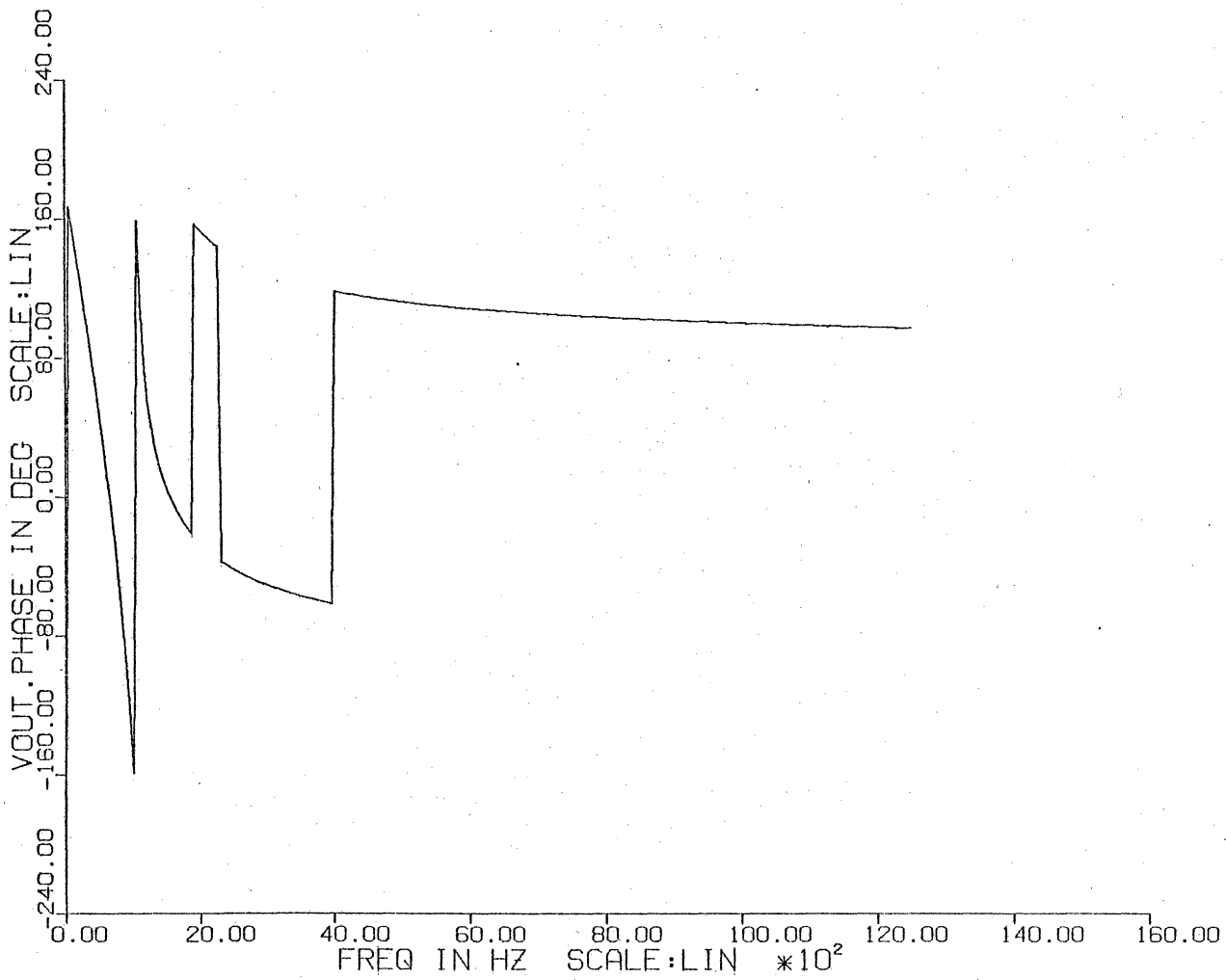


Figure 3.2-3. The phase response of the seventh order filter as predicted by DIANA.

1) Determine the direction of the output amplitude shift due to a change in value of all integrating and summing capacitors in the filter, using sensitivity results from DIANA.
2) Change all integrating and summing capacitor values so as to produce an increase of the output amplitude.
3) Simulate the filter response with DIANA using worst case direction shifts.
4) Compare the worst case filter response with the ideal response.

This procedure will indicate what component tolerances are required to achieve a given accuracy in the filter response. DIANA will not perform a sensitivity analysis on switched capacitors, so the assumption is made that all switched capacitors track in value, and any errors in capacitor values occur in the integrating and summing capacitors. Another assumption is that worst case shifts producing an amplitude increase are indicative of the shifts producing an amplitude decrease.

The results of the sensitivity analysis of individual capacitors, summarized in Table 3.2-1, were used to make 1%, 2%, and 5% worst case shifts in values. For each of the three cases a separate DIANA run calculated the response. The plots of the 5% worst case shifts are shown in Figure 3.2-4 and Figure 3.2-5. A comparison of numerical DIANA results in Table 3.2-2 show that notch locations are relatively insensitive to capacitor values. The ripple and cutoff frequency both show a gradual increase as the magnitude of the shifts increase. Arbitrary 5% value shifts, indicated in Table 3.2-3, verify

Table 3.2-1. The direction the capacitors should be shifted to produce a worst case situation.

Capacitor	Worst Case Shift to Produce An Increase In Amplitude
C_{I1}	Decrease
C_{I2}	Increase
C_{I3}	Decrease
C_{I4}	Decrease
C_{I5}	Decrease
C_{I6}	Decrease
C_{I7}	Decrease
C_{C21}	Increase
C_{C22}	Decrease
C_{C41}	Increase
C_{C42}	Decrease
C_{C61}	Increase
C_{C62}	Decrease

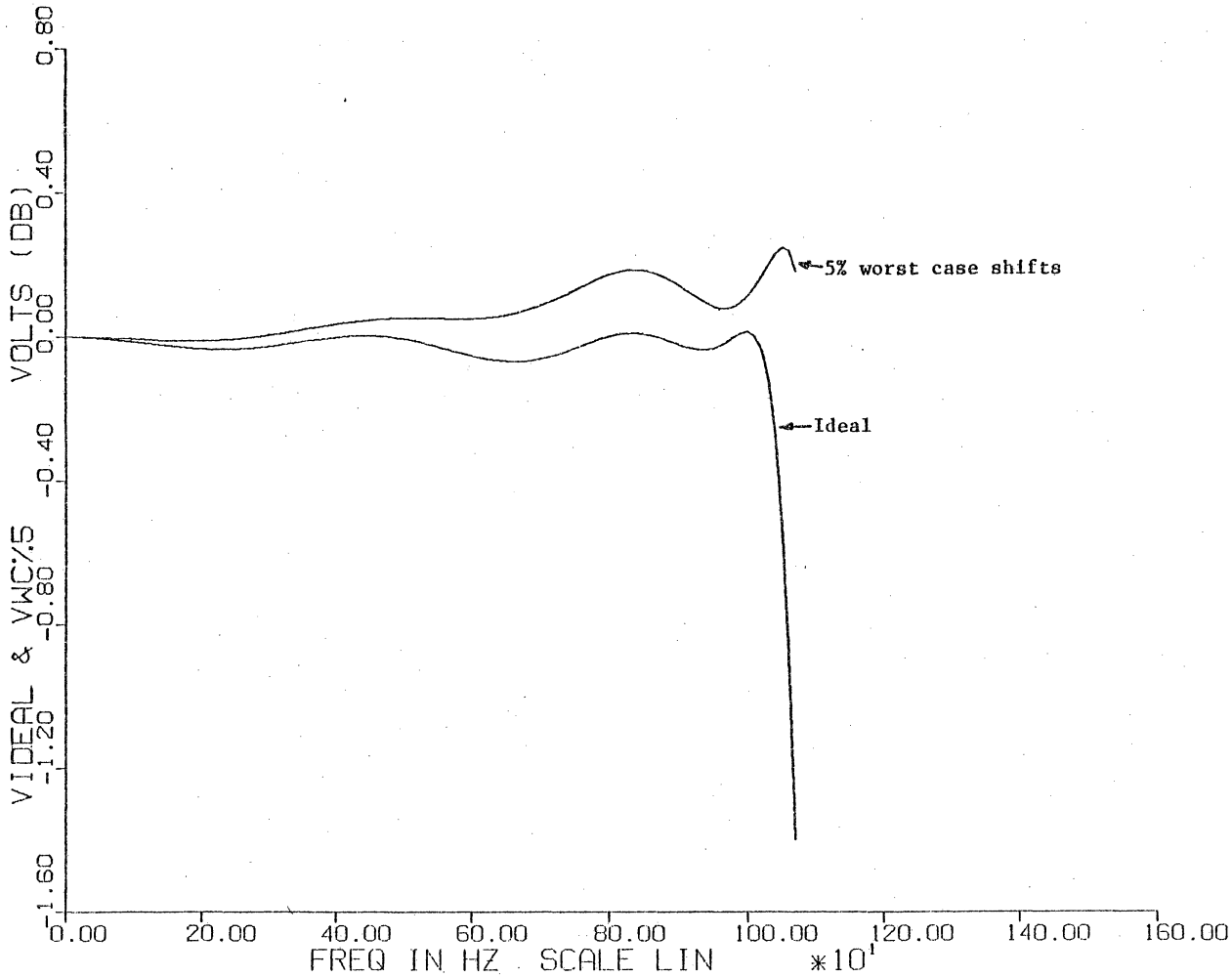


Figure 3.2-4. The results of a 5% worst case change in capacitor values on the passband of the seventh order filter.

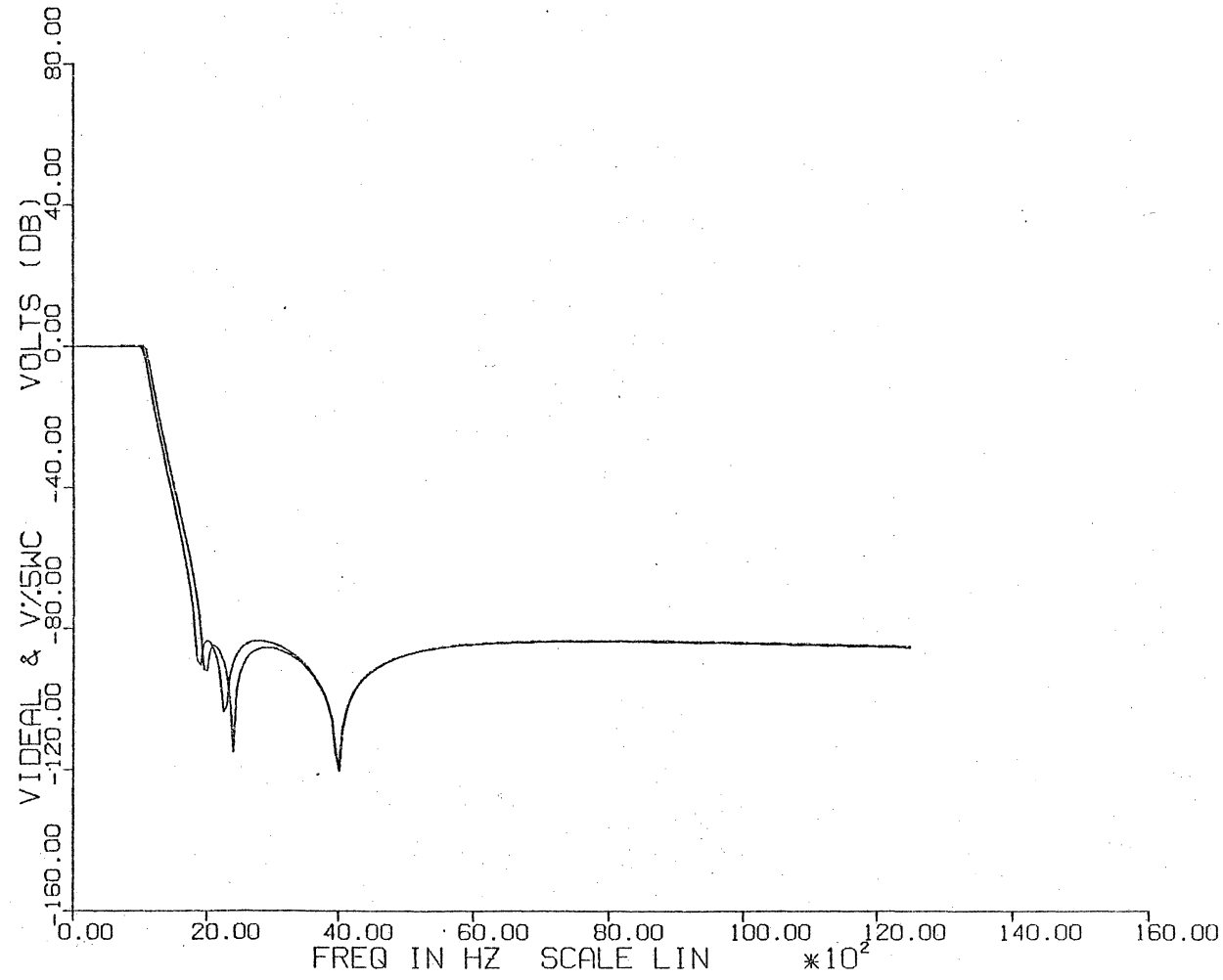


Figure 3.2-5. The results of a 5% worst case change in capacitor values on the response of the seventh order filter.

Table 3.2-2. The results of the worst case shifts on the filter characteristics.

Sensitivity Summary

Amount of Worst Case Shift	Ripple[1] (db)	f_{c0}[2] (kHz)	OBR (dB)	First[3] Notch (kHz)	Second[3] Notch (kHz)	Third[3] Notch (kHz)
0%	.081	1.017	83.1	1.882	2.284	3.991
1%	.1004	1.033	83.5	1.882	2.284	3.991
2%	.146	1.047	83.4	1.933	2.334	3.991
5%	.2541	1.077	83.3	1.983	2.384	3.991

[1] Non-equiripple passband; the ripple is the ratio of the passband maxima to the passband minima.

[2] Obtained by interpolation; resolution of ±25 Hz.

[3] Obtained by interpolation; resolution of ±50 Hz.

Table 3.2-3. The direction of the arbitrary worst case shifts.

C_{I1}	+
C_{I2}	-
C_{I3}	+
C_{I4}	-
C_{I5}	+
C_{I6}	-
C_{I7}	+
C_{C21}	-
C_{C22}	-
C_{C41}	+
C_{C42}	-
C_{C61}	+
C_{C62}	+

that worst case shifts were made.

3.3 TCAPS

TCAPS is an expanded version of TCAP which models switched capacitors and switched resistors as well as capacitors, resistors, independent and dependent sources. All analysis is performed in the time domain and then converted to the frequency domain to obtain the transfer function. At each time point, TCAPS sets up a conductance matrix $\underline{G}$ and solves

$$\underline{I} = \underline{G}\,\underline{V} \tag{3.3-1}$$

for the voltage, $\underline{V}$, by an iterative procedure. As a result of analyzing in the time domain, a phase response of the filter is not available. This program is particularly well suited for the analysis of second-order effects since many of the non-ideal elements can be modeled.

TCAPS models all elements by means of current sources and resistors. Capacitors are modelled by shunt resistances and dependent current sources. From the basic definition of a capacitor:

$$i = \frac{Cdv}{dt} \tag{3.3-2}$$

This relation can be approximated by a difference equation as

$$i_n = \frac{C}{\Delta t}\left(V_{(n)} - V_{(n-1)} \right) \tag{3.3-3}$$

or

$$i_n = G\,V_{(n)} - i_{(n-1)} \tag{3-3-4a}$$

where $G = \frac{C}{\Delta t}$, and

$$i_{(n-1)} = \frac{C}{\Delta t} V_{(n-1)} \qquad (3.3\text{-}4b)$$

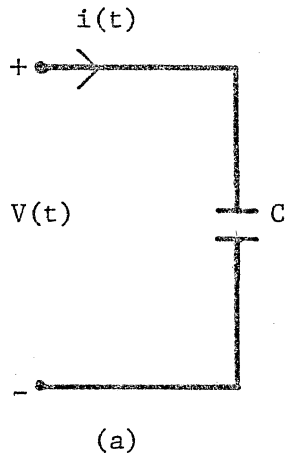
This is shown in Figure 3.3-1.

Switched capacitors are modeled by switching a capacitor between two different pairs of nodes with the initial capacitor voltage set by the previously calculated capacitor voltage as shown in Figure 3.3-2.

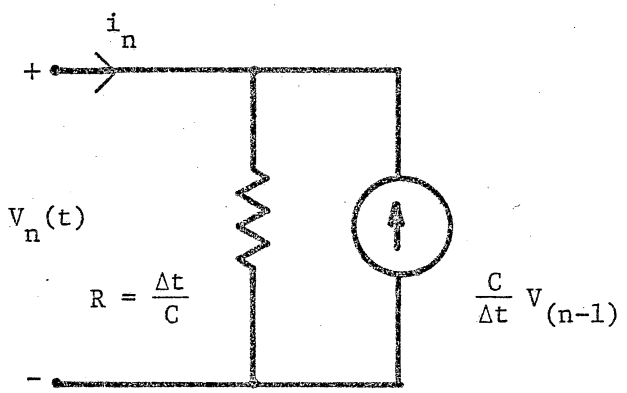
Four clock states define where the switches were previously connected at $(n-1)\Delta T$ and where they are presently connected at $n\Delta T$. In state 1 the switches at $(n-1)\Delta T$ were connected to nodes c and d and at nT the switches are connected to nodes a and b. The initial voltage of the capacitor at $n\Delta T$ is the last value calculated when the capacitor was connected to nodes c and d.

When the clock is in state 2, the switches at $(n-1)\Delta T$ are connected to nodes a and b and at $n\Delta T$ the switches will continue to be set to nodes a and b. The initial capacitor voltage at $n\Delta T$ is set by the value calculated at $(n-1)\Delta T$. The other two states are similarly defined.

Due to the way the switching has been defined, a minimum of four time-steps per clock cycle are necessary, even for the simulation of ideal SCFs. If resistive parasitics are added to the network, more time steps per clock cycle are required so that TCAPS can accurately calculate the charging of capacitors.

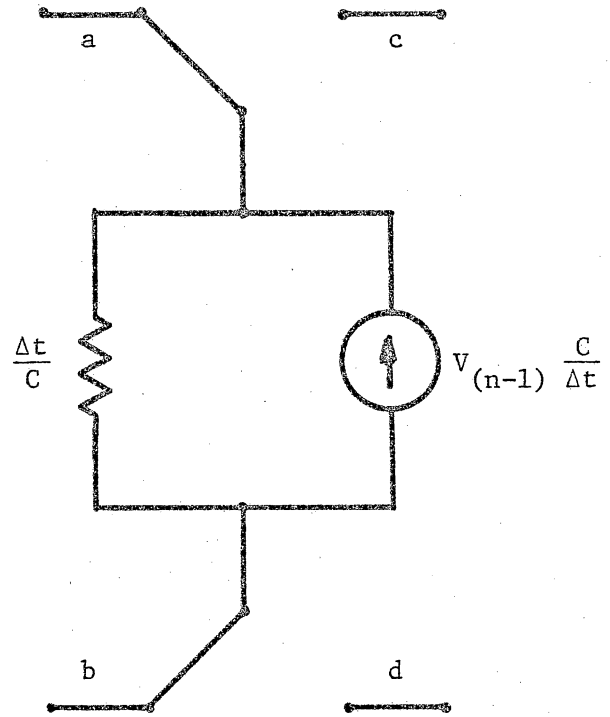


(a)



(b)

Figure 3.3-1. The capacitor of (a) is modelled by TCAPS as a parallel resistor and current source.



Clock State	Present Nodes	Previous Nodes	Initial Voltage
1	a, b	c, d	V_{cd}
2	a, b	a, b	V_{ab}
3	c, d	a, b	V_{ab}
4	c, d	c, d	V_{cd}

Figure 3.3-2. TCAPS switched capacitor.

At present, the duty cycles of the clocks are set at 50% and cannot be changed. However, TCAPS can be altered to give more flexibility as the need arises.

Switched resistors are modelled in a similar manner to the switched capacitor with the exception that voltages are not stored.

A current source and gyrator model a voltage source as in Figure 3.3-3. A voltage source adds an extra node and two extra elements. Therefore, if possible, a voltage source should be replaced by its Norton equivalent network to reduce the size of the matrix.

Most linear parasitics can be modelled using these basic elements. The gain-bandwidth product of an op amp can be modelled by adding a current source in shunt with a resistor and capacitor as shown in Figure 3.3-4. Switch resistance is simply incorporated by a series connection of a switched resistor and a switched capacitor, as shown in Figure 3.3-5. The switches on the common terminal are still connected in the same relative fashion regardless of the switch phase.

The simulation of the frequency response of an SCF is performed as shown in Figure 3.3-6. From an input file, which contains component types, values and interconnections, TCAPS forms conductance and current matrices. An approximation to a step, u(t), is applied to the system of equations and at each timepoint the system matrices are updated. Thus s(t), an approximation to the step response, is calculated. The exact step response cannot be simulated, since the step input u(t) is not an exact representation of a step as shown in

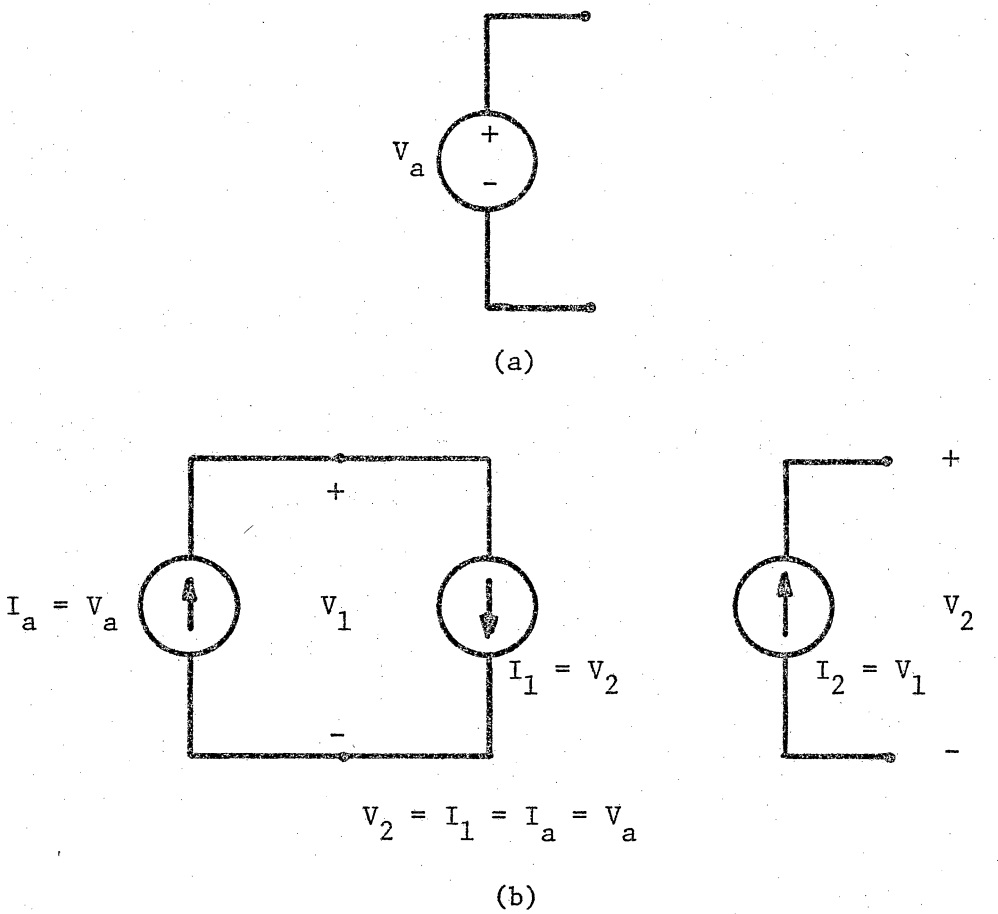
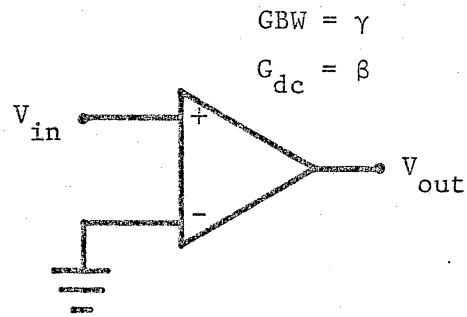
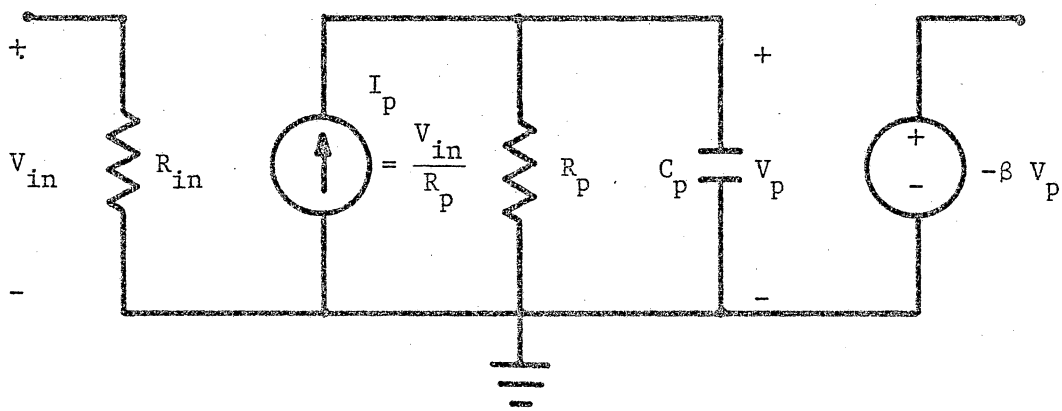


Figure 3.3-3. TCAPS models the voltage source of (a) by the current source and gyrator of (b).



(a)



$$R_p\ C_p = \frac{\gamma}{2\pi\beta}$$

(b)

Figure 3.3-4. An op amp with a gain-bandwidth product is modelled by TCAPS as shown in (b)

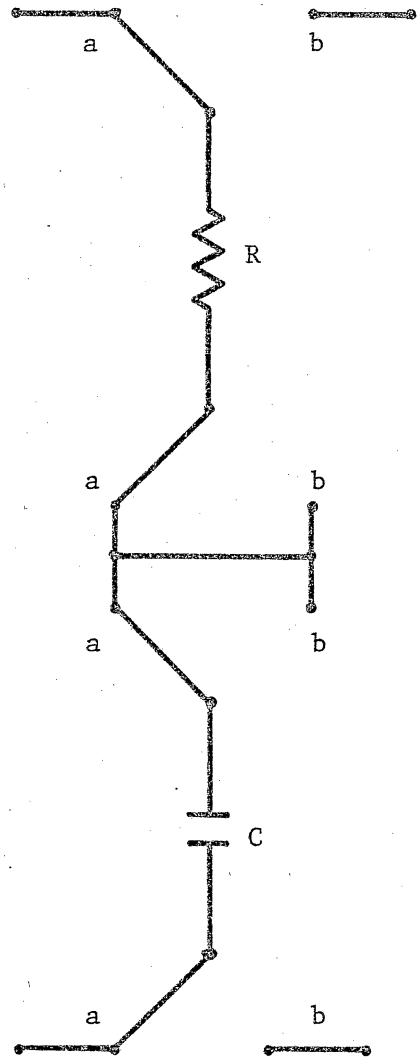


Figure 3.3-5. Switch resistance is incorporated by a series connection of a switched resistor and a switched capacitor.

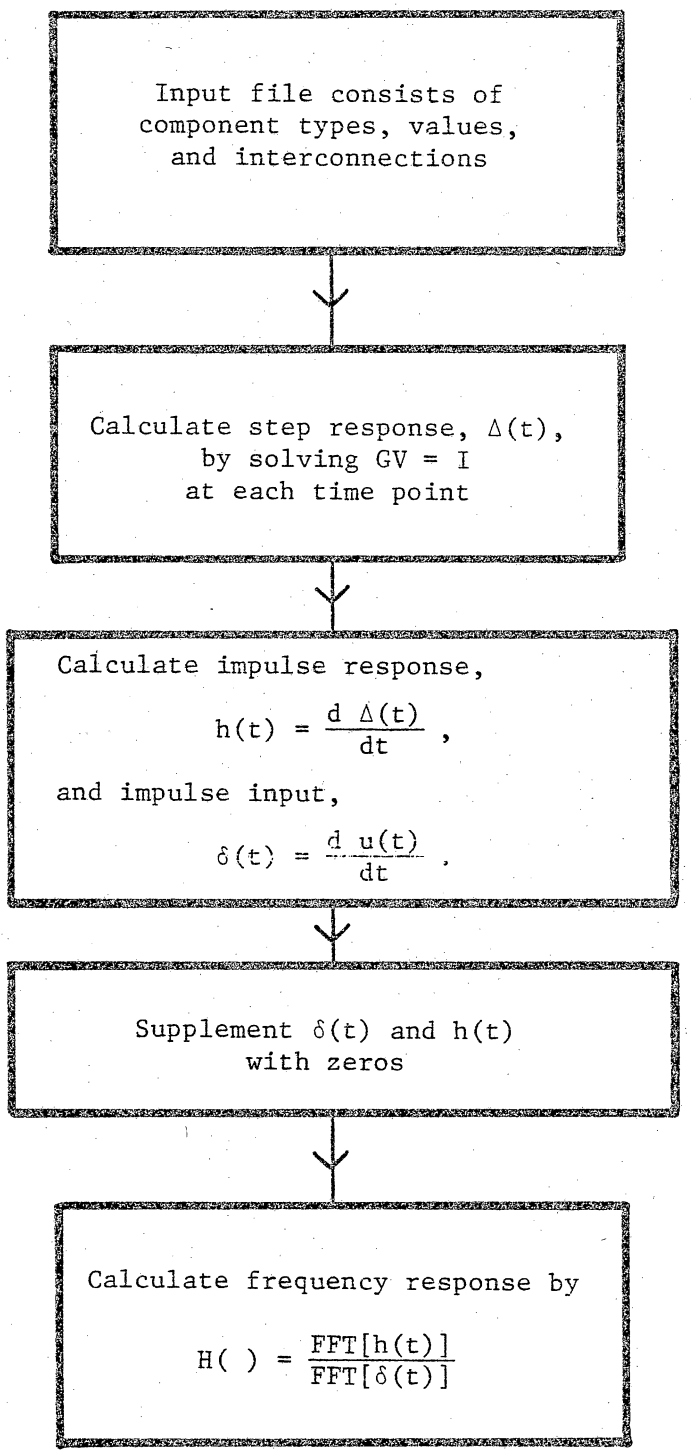


Figure 3.3-6. A flow diagram of TCAPS.

Figure 3.3-7.

Next, before the frequency response is calculated by deconvolution, $\delta(t)$ and $h(t)$ are determined by

$$\delta(t) = \frac{d}{dt} u(t) \tag{3.3-5}$$

and

$$h(t) = \frac{d}{dt} s(t) \ . \tag{3.3-6}$$

Again, $\delta(t)$ and $h(t)$ are approximations to the impulse function and the impulse response.

The resolution of the frequency response is increased by supplementing $\delta(t)$ and $h(t)$ with zeros. This increases the total time window of the input and response without increasing the computational burden, and decreases the frequency step size of the FFT. $\delta(t)$ is zero after $2\Delta T$ (see Figure 3.3-7) and $h(t)$ will be zero if the filter has reached a steady-state response. If $s(t)$ has not reached steady state, $h(t)$ will have a discontinuity when the trailing zeros are added. This results in ripple in the frequency response because the discontinuity introduces a small $\text{sinc}(\omega t)$ term in the frequency domain. Thus, a steady-state response is required to obtain the correct frequency response.

Finally, the frequency response is calculated by a frequency deconvolution,

$$H(\omega) = \frac{\text{FFT } [h(t)]}{\text{FFT } [\delta(t)]} \ . \tag{3.3-7}$$

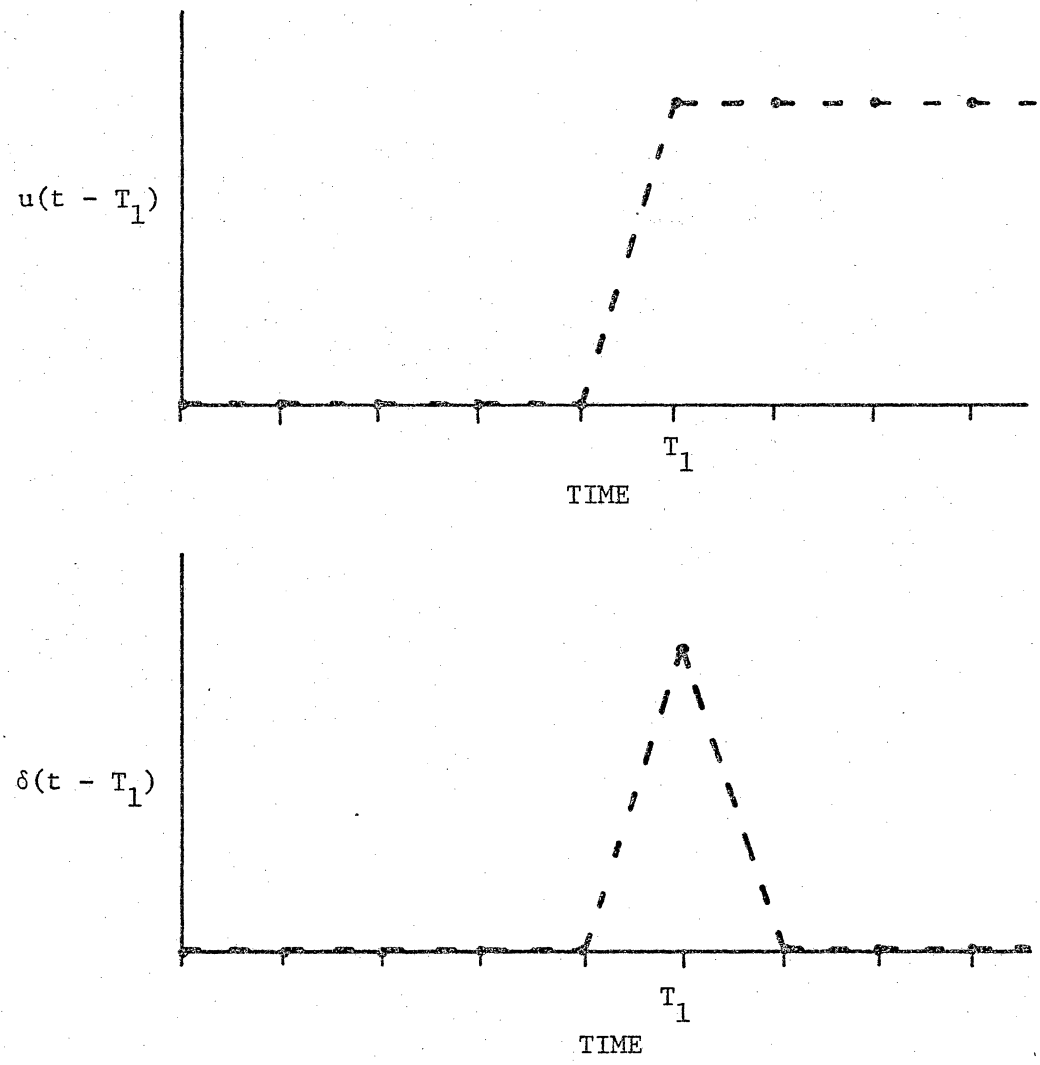


Figure 3.3-7. The step and impulse inputs are approximated by ramps.

$H(\omega)$ is exact since the errors introduced by the approximate nature of $\delta(t)$ and $h(t)$ have been removed through the deconvolution.

$s(t)$ is not deconvolved with $u(t)$ because in the frequency domain both $S(\omega)$ and $U(\omega)$ have zeros which fall close to, or in the frequency band of interest. This results in large errors in $H(\omega)$ at these frequencies. The obvious solution to this problem would seem to be decreasing the time duration of the input signal and thus increasing the frequency of the indeterminate regions so that they are out of the frequency band of interest. The best possibility is to simulate the impulse response of the filter.

However, due to the time varying-nature of the network, the impulse response of an SCF is not clearly defined. Consider the ideal SC integrator of Figure 3.3-8a with the switches originally in position b. The switches change positions as shown in Figure 3.3-8b, and the integrator has zero initial conditions. Since there are no time constants, all of the inputs shown in Figure 3.3-8c through Figure 3.3-8e will yield the response of Figure 3.3-8f. As long as $v_{in}(1\ \Delta T) = 1$ and $v_{in}(n\Delta T) = 0$ for all $n \geq 4$, the network will have the same response. Which of these inputs is the correct one? The frequency response of the network will be affected by the choice of input because of the frequency deconvolution. A basic assumption of the filter operation has been violated; namely, $f_{signal} << f_{clock}$ and hence the network can no longer be approximated as time-invariant. The problems with the definition of an impulse for SC networks cause this approach to be avoided in determining

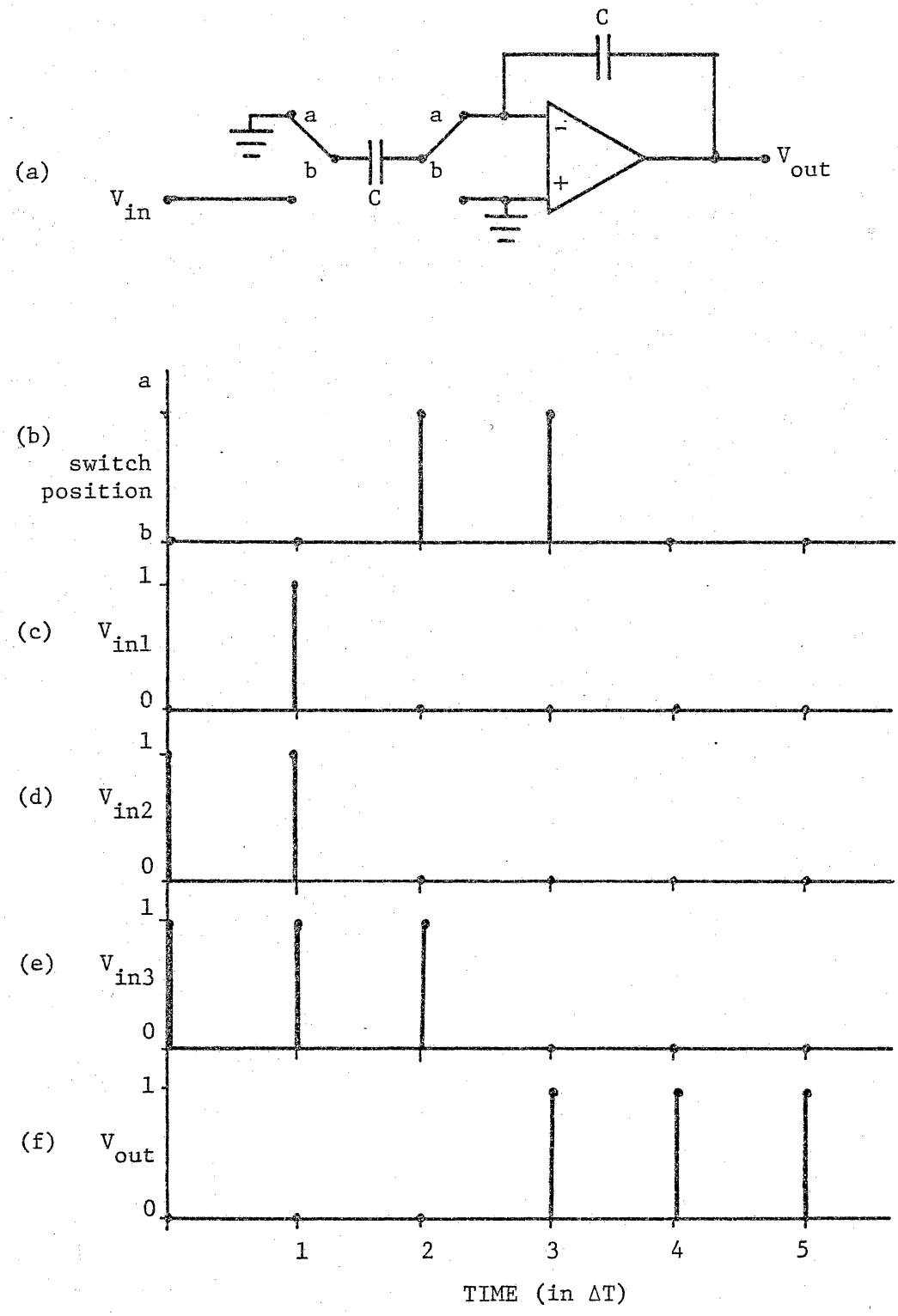


Figure 3.3-8. The impulse inputs (c) through (e) yield the same "impulse" response of (f).

frequency response.

The zeros in the step response and the problems obtaining an impulse response lead to the process outlined in Figure 3.3-6. By first simulating s(t), one avoids using an ill-defined input, then by taking the derivative of s(t), the zeros of u(t) and s(t) do not fall in the frequency band of interest.

As an example, consider the scaled filter of Chapter 2. For this filter, f_C = 50 kHz and so T_{clock} = 20 μsec. Since this is an ideal filter, only four time steps/clock cycle are required to calculate the step response. Thus

$$\Delta T = \frac{T_{clock}}{4 \text{ time steps/clock cycle}} = 5 \text{ μsec} .$$

A frequency resolution of approximately 25 Hz is required for the comparison of TCAPS with the other programs. If the impulse response is supplemented so that there are a total of 8192 timepoints, the total time window is 40.96 msec and the frequency resolution is 24.41 Hz.

The number of timepoints which should be calculated is a matter of trial and error. An initial guess of 3000 timepoints yielded the result should in Figure 3.3-10 for the seventh order filter. It is obvious that the filter has not reached steady-state because of the ripple in the stopband. When the step response is calculated out to 4096 timepoints, the filter is sufficiently close to steady-state that ripple is negligible, as shown in Figure 3.3-11.

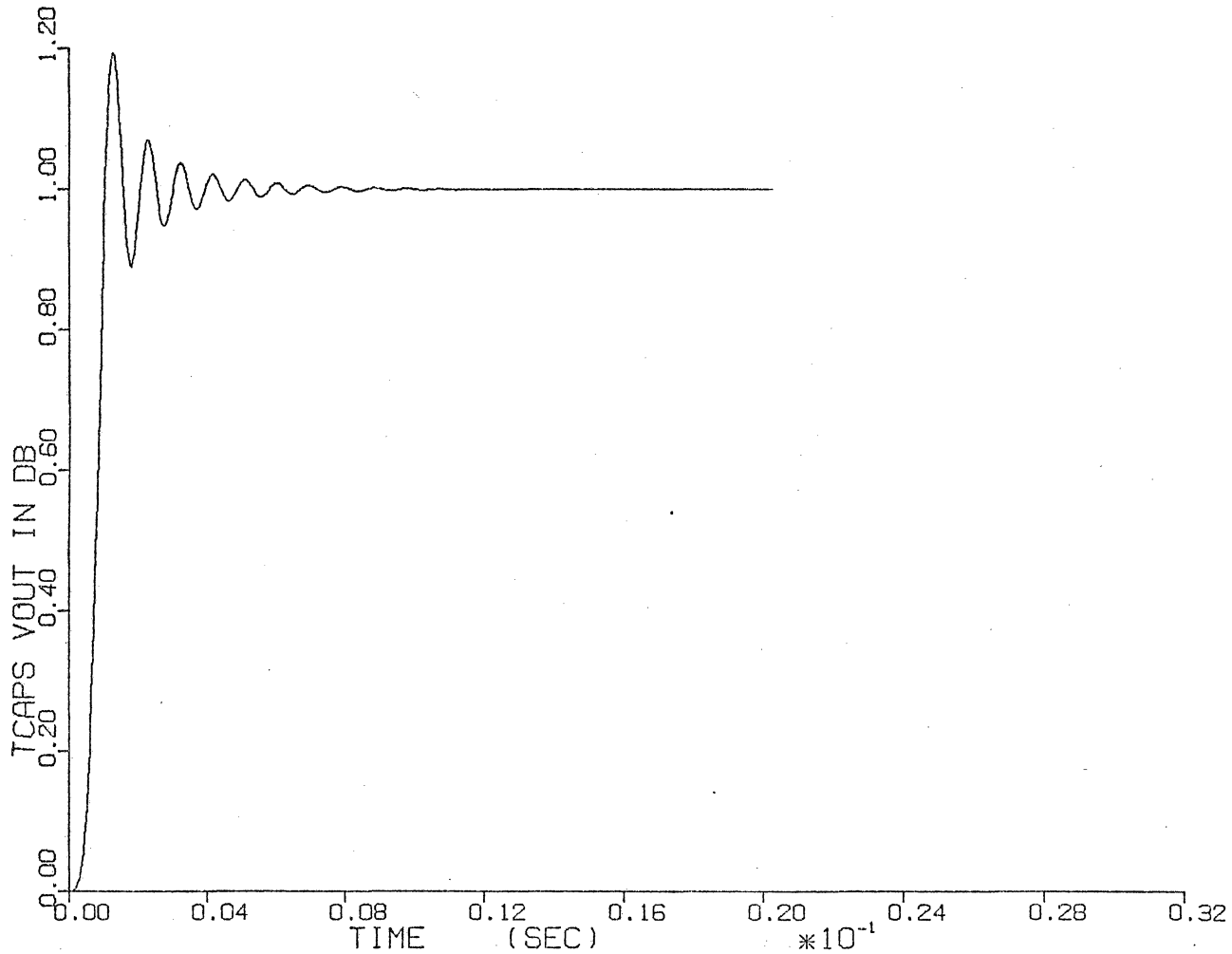


Figure 3.3-9. The step response of the seventh order filter simulated by TCAPS.

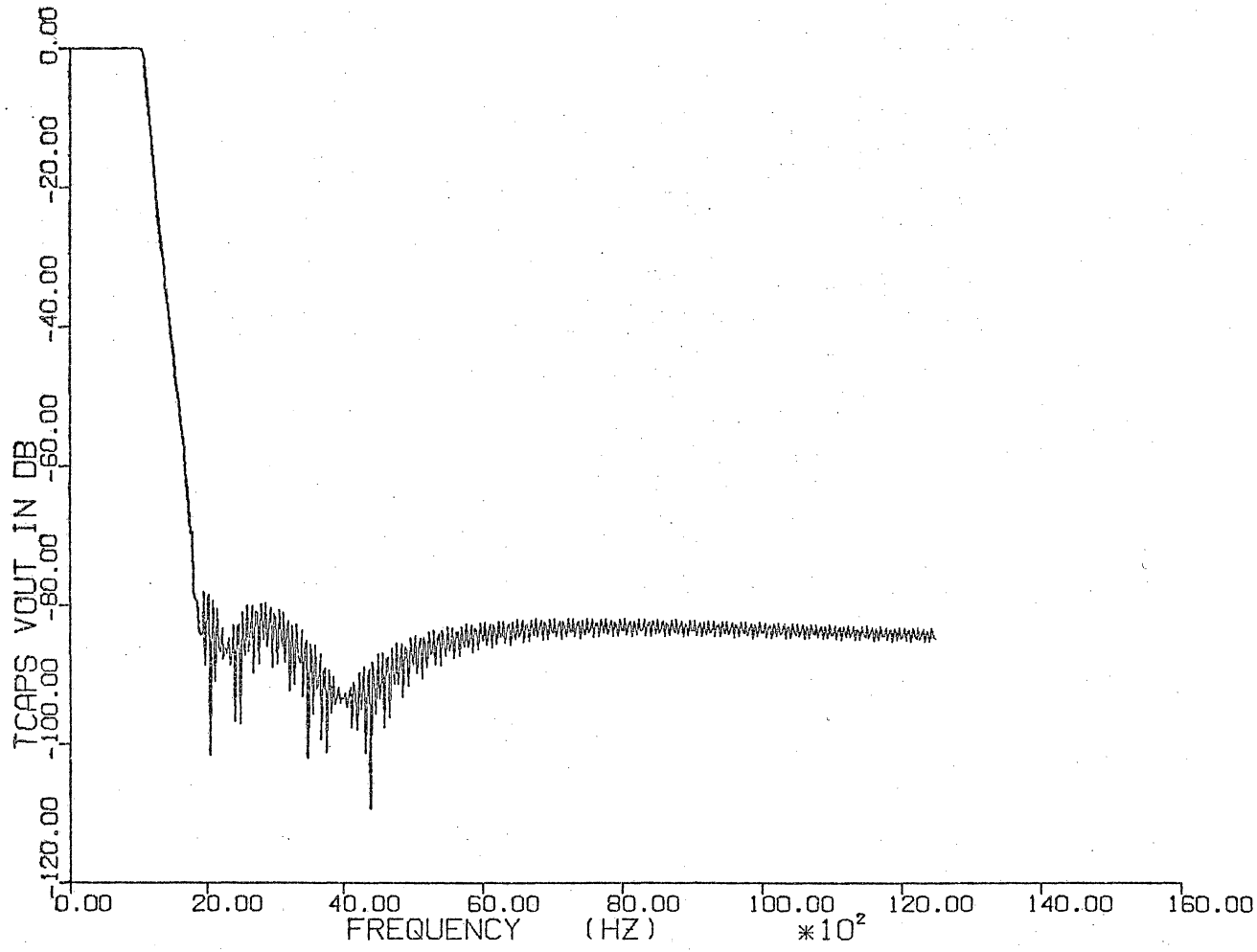


Figure 3.3-10. The frequency response of the seventh order filter with 3000 time points.

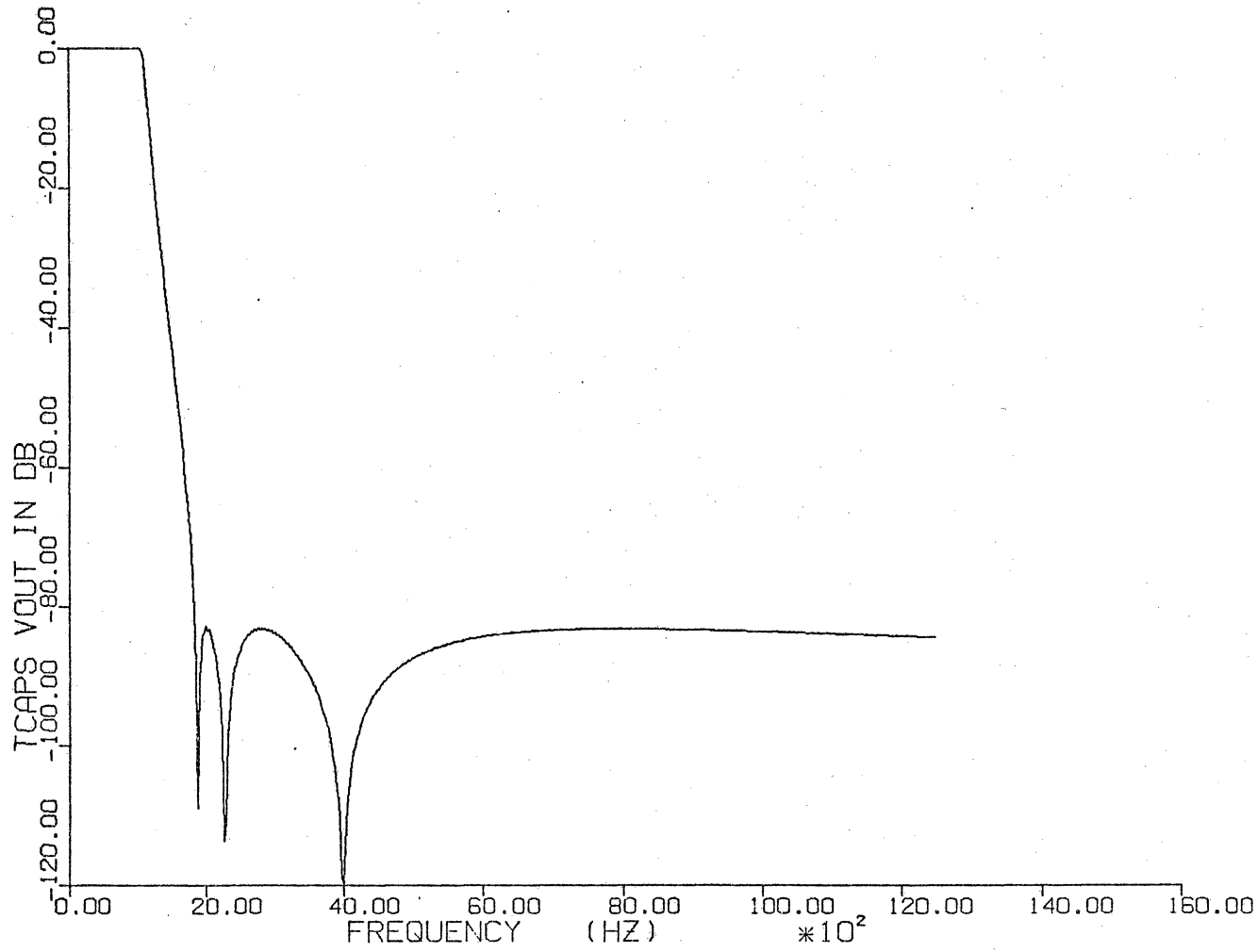


Figure 3.3-11. The frequency response of the seventh order filter with 4096 time points.

3.4 Results

Numerical results from SPICE, DIANA, and TCAPS for the seventh order SCF are shown in Table 3.4-1. These data were obtained from printed results rather than from plots. A frequency resolution of approximately 25 Hz was sufficient to resolve the notch frequencies in comparison with the practical results of Chapter 2, and also to give an indication of other filter parameters.

Passband ripple is defined as the difference, in dB, between the highest and lowest points in the passband, even for a non-equi-ripple passband. The ripple values should be regarded as an approximation since Δf is not small enough to accurately resolve passband maxima and minima locations. This is particularly true of the maxima; in all three programs the maximum is an isolated point surrounded by signal levels close to or below the passband minima.

The cutoff frequency, f_{co}, is not clearly defined for non-equil-ripple passbands. A definition which gives some indication of its value is:

> f_{co} is the frequency at the passband edge where the signal amplitude is equivalent to the passband minima, as shown in Figure 3.4-1.

The values of f_{co} in Table 3.4-1 were calculated by linear interpolation. In view of the large Δf and the relatively rapid change in signal amplitude at the passband edge, all of these values have an error of $\pm\Delta f/2$.

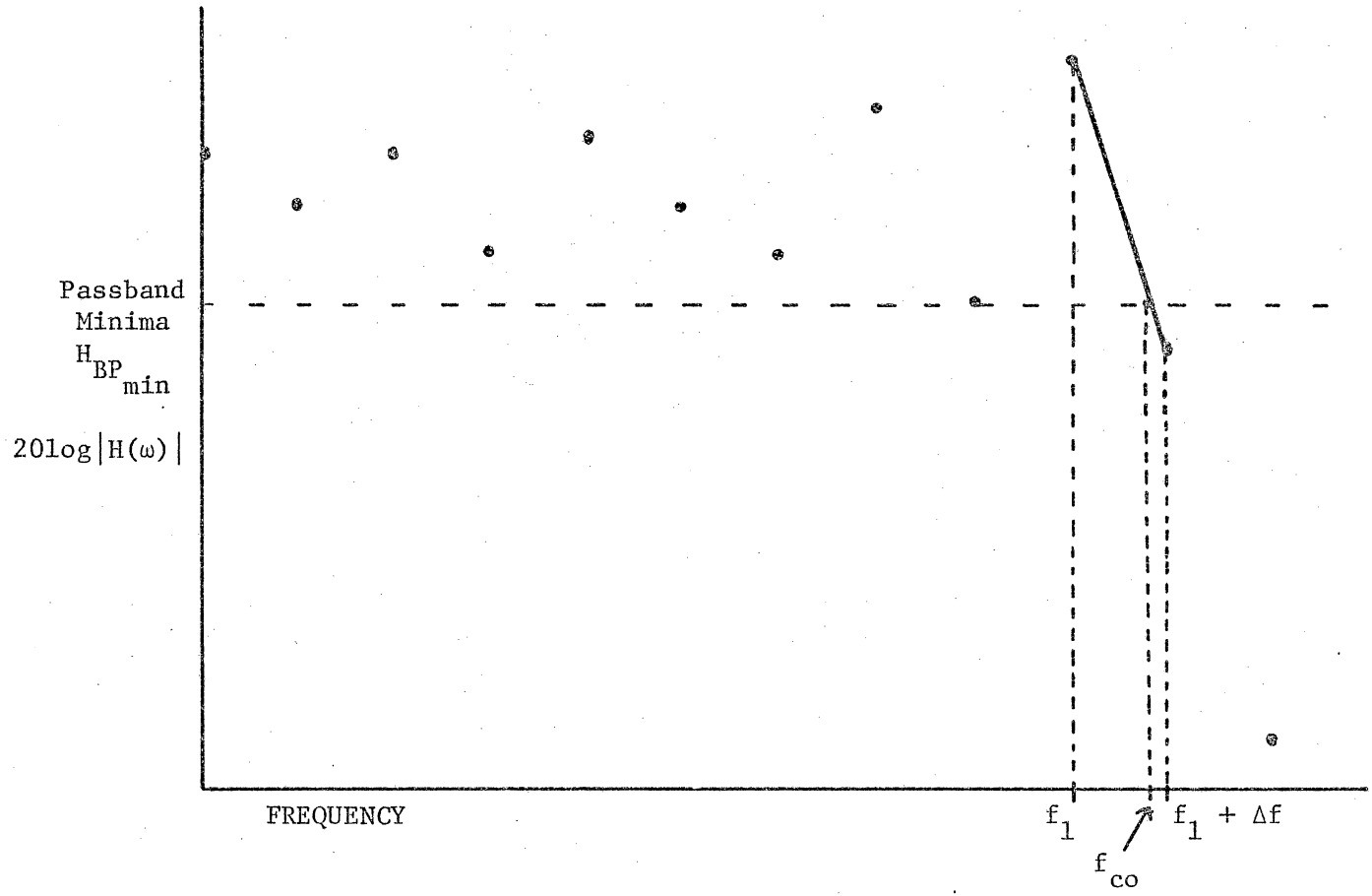


Figure 3.4-1. f_{co} was approximated by linear interpolation.

Table 3.4-1. A comparison of the results of the seventh order filter on SPICE, DIANA, and TCAPS.

Parameters	Design	SPICE	DIANA	TCAPS
Ripple (dB)	0.3 dB	.0280	.0792	.0711
f_{c0} (1) (Hz)	1000	997	1021	1016
OBR (dB)	82.11	82.11	83.34	82.8
1st (2) Notch (Hz)	1875.6	1880	1880	1880
2nd (3) Notch (Hz)	2273.3	2281	2281	2270
3rd (4) Notch (Hz)	3948.6	3960	3985	4003
f_{clock}	50 kHz	50 kHz	50 kHz	50 kHz

(1) Resolution of ±1.2%.

(2) Resolution of ±1.3%.

(3) Resolution of ±1.1%.

(4) Resolution of ±0.6%.

Notch frequencies are determined by the lowest stopband signal levels. Ideally, the amplitude at the notch will go to zero (or, in dB, negative infinity), but due to computer roundoff errors, this will never occur. Also, the notch frequency cannot be exactly determined since the notch could fall on either side of the stopband minima. Therefore, all notch frequencies have an error of $\pm \Delta f$.

OBR is the difference in dB between the passband maxima and the stopband maxima as previously defined in Section 2.3.

3.5 Discussion

For the simulation of the seventh order filter, the SPICE results met the design specifications for ripple, OBR, f_{co}, and notch frequencies, while the results of DIANA and TCAPS showed some deviations. In the SPICE simulation, switched capacitors are replaced by equivalent resistors thus changing the SCF into an analog equivalent network. Any effects of the switching on the filter's performance are removed since the network is essentially the passive prototype with a modified topology. Therefore, the SPICE simulation is much closer to meeting the original filter specifications than either DIANA or TCAPS. This does not indicate that DIANA and TCAPS are incorrect, but rather that SPICE is incorrect, since it cannot simulate a switched capacitor.

The increased ripple predicted by DIANA and TCAPS is caused by the low value of f_c/f_{co}. If f_c/f_{co} is increased, the LDI stages become more ideal, and the passband ripple decreases as shown earlier.

DIANA and TCAPS also track in predicting an increased value of f_{co} as compared to the SPICE results and the design values. It can be argued that the increase of f_{co} is a result of its specification; as the ripple increases, the passband minima are reduced in amplitude, thus increasing the measured value of f_{co}. However, if the frequency of -0.03 dB from the passband maxima is taken as an alternate cutoff frequency specification, DIANA and TCAPS still predict that $f_{-.03\ dB}$ is slightly greater than the design value, as shown in Table 3.5-1.

The values of OBR predicted by DIANA and TCAPS are greater than the design value.

While the three programs do not show any significant differences in the first two notch locations, DIANA and TCAPS do predict that the third notch is increased in frequency as compared with SPICE. This shift, due to the frequency warping effects of the LDI transform, is not as severe at lower frequencies relative to f_c, so the first two notch locations aren't affected as much as the third notch.

When compared to the original design, DIANA and TCAPS track in their predictions of

1) Increased passband ripple
2) Increased f_{co}
3) Increased third notch frequency
4) Increased OBR

SPICE does not show any of these effects since it cannot model the digital nature of a SCF.

Table 3.5-1. Different specifications of the cutoff frequency still show that DIANA and TCAPS have a higher f_{co}.

	f_{co}	$f_{-.03\ dB}$
Design	1000 Hz	1000 Hz
SPICE	997	948
DIANA	1021	1009
TCAPS	1016	1006

Table 3.5-2 summarizes the abilities and limitations of SPICE, DIANA V6 and TCAPS. On the basis of this comparison, it is not possible to state if DIANA V6 or TCAPS is the better package. TCAPS is a relatively slow program, but it can model resistive parasitics. DIANA V6 is very fast, but it can only simulate ideal SCFs. However, one can say that both DIANA V6 and TCAPS simulate SCFs far more accurately than SPICE.

Table 3.5-2. A summary of the abilities of TCAPS and DIANA V6.

TCAPS	DIANA V6
Time domain analysis	Frequency domain analysis
Slow	Fast
Models linear parasitics	Cannot model resistive elements (1)
Clock set at 50% duty cycle (2)	Variable clock duty cycle
-	Sensitivity analysis
-	Macros
Additional functions and network elements can be added i.e. non-linear elements, noise analysis	Limited to present capabilities

(1) DIANA V7 includes resitive elements.

(2) This can be modified; the TCAPS algorithm does not limit the duty cycle to 50%.

CHAPTER 4. CONCLUSIONS

Two aids for the design of SCFs have been examined: construction of a scaled filter, and computer simulation. Both methods have been found useful in the prediction of an integrated filter's performance.

A low-pass seventh order scaled capacitor filter has been designed with the same passive prototype used in an integrated SCF manufactured by Reticon. An exact replication of the integrated filter was not attempted for several reasons:

1) The impracticality of obtaining accurate capacitor ratios with very small values of discrete capacitors.
2) The unavailability of Reticon's schematic at the time of the project.
3) The unavailability of the Reticon amplifiers and switches.

Some reasonable guidelines were followed in the selection of components: low switch resistance, high op amp gain-bandwidth product, high Q capacitors, and small capacitor charging time constants. A switch phasing rule was developed which incorporates both phasing schemes appearing in the literature. Also, it was necessary to optimize the dynamic range of the filter so that all of the notches in the transfer function appeared. With these guidelines, the scaled filter was closer to meeting the original design specifications than the Reticon filter, with the exception of the OBR.

Now that the Reticon filter design is known, a logical next step is to investigate how closely a scaled filter must model the

integrated filter so that the integrated filter's performance can be replicated. How closely do the scaled filter's charging time constants need to follow those of the integrated filter? What methods, if any, can be used on the breadboard to model the integrated filter op amps?

Another topic for investigation is to determine the cause for the change in the filter transfer function when the relative phase between non-overlapping clocks is changed. Are some filter structures more sensitive? Is there an optimal phase setting for the clocks?

Also, this project was limited to examining one filter with a lowpass leapfrog design. Can scaled filters predict the performance of other structures such as biquads or state variable representations? Or other types of filters such as bandpass or highpass?

In the second part of this investigation, SPICE, DIANA V6, and TCAPS were evaluated to determine their usefulness as SCF design aids. The investigation was limited to linear networks and effects, since no programs were available which incorporated non-linear models. Each program is useful in different areas of the design process. SPICE is limited to the evaluation of the passive prototype and rudimentary checks on the topology of the SFG. DIANA V6 can simulate ideal SCFs (without resistors) and is extremely fast. TCAPS is the most general program of the three, since it can simulate parasitics in the filter.

Although DIANA V6 has some features, such as macros and sensitivity analysis, that TCAPS does not have, the DIANA user is limited to the

present abilities of the program. The TCAPS user, on the other hand, can modify the program to incorporate new features as needed, since TCAPS is written in FORTRAN.

A topic for further investigation is to establish if either TCAPS or DIANA V6 is more accurate by a detailed comparison of the results of these programs with the results of an analytical technique. The results of the seventh order filter simulation show good agreement between DIANA and TCAPS, but they are not sufficient to show if one is more accurate than the other.

Switch resistance and gain-bandwidth product can be studied with TCAPS, but guidelines need to be determined for setting the time step size of TCAPS when resistive parasitics are present. Too large a step size will lead to errors in the simulation, while too small a step will take an excessive amount of computational time. Also, it would be informative to compare the results of DIANA V7 and TCAPS on SC networks with resistive parasitics.

Another possibility for research is to expand TCAPS to include non-linear network models and noise simulation. With these capabilities, TCAPS could simulate intermodulation distortion tests, dynamic range tests, slew rate limiting of op amps, and device noise floor tests.

In the meantime, the two design aids examined here can test the design of SCFs. Each has separate advantages: the scaled filter can show the effects of unmodelled parasitics, while the computer simulations can accurately and quickly show the effects of known parasitics.

At present, neither one alone can give an accurate indication of integrated filter performance, so both are necessary in the design of SCFs. The eventual goal is to use computer simulations to predict SCF performance once all revelant parasitics are known, while the scaled filters will be a stepping stone to gain that knowledge.

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APPENDIX 1. PARASITIC-FREE SC INTEGRATORS

Inverting Integrators

Assume that V_{in} is a constant for $nT \leq t \leq (n + \frac{1}{2})T$. At $t = nT$ the switch is in position a as shown in Figure A1-1.

The charge on C_1 is given by

$$q_{C_1}(nT) = C_1 V_{in}(nT) \tag{A1-1}$$

Since C_1 is connected to the input of the op amp, its charge is subtracted from the existing charge on C_2.

$$q_{C_2}(nT) = C_2 V_{out}\left[(n - \tfrac{1}{2})T\right] - C_1 V_{in}(nT) \tag{A1-2}$$

At $(n + \frac{1}{2})$ the switch goes to position b and C_1 is discharged. No additional charge is added to C_2, so

$$q_{C_2}\left[(n + \tfrac{1}{2})T\right] = q_{C_2}(nT) \tag{A1-3}$$

$$q_{C_2}\left[(n + \tfrac{1}{2})T\right] = C_2 V_{out}\left[(n - \tfrac{1}{2})T\right] - C_1 V_{in}(nT) \tag{A1-4}$$

But by definition,

$$q_{C_2}\left[(n + \tfrac{1}{2})T\right] = C_2 V_{out}\left[(n + \tfrac{1}{2})T\right] \tag{A1-5}$$

Substituting Eqn. (A1-5) into Eqn. (A1-4) yields

$$C_2 V_{out}\left[(n + \tfrac{1}{2})T\right] = C_2 V_{out}\left[(n - \tfrac{1}{2})T\right] - C_1 V_{in}(nT) \tag{A1-6}$$

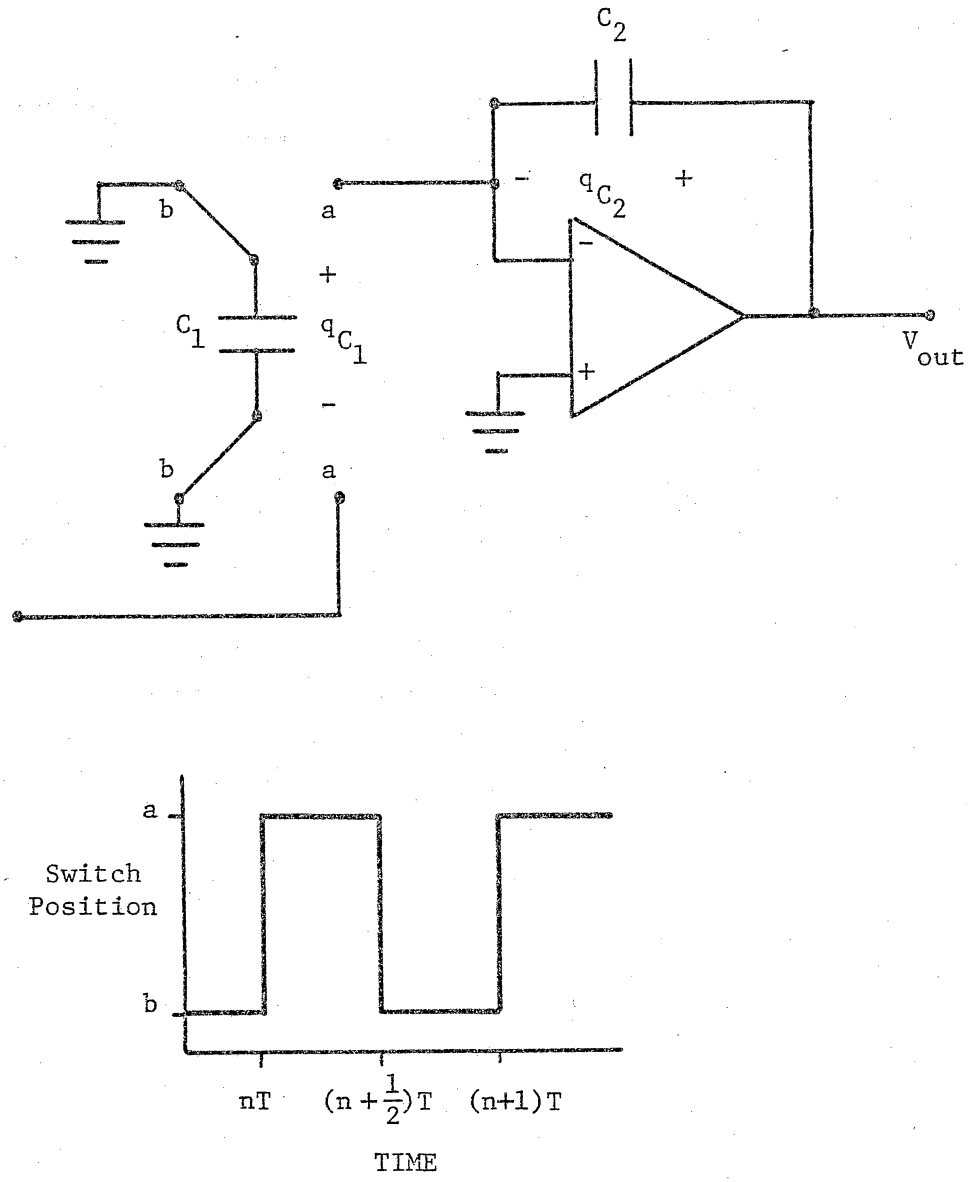


Figure A1-1. The inverting parasitic-free SC integrator.

Taking the Z-transform of the above expression results in

$$C_2 V_{out} Z^{\frac{1}{2}} = C_2 V_{out} Z^{-\frac{1}{2}} - C_1 V_{in} \qquad \text{(A1-7)}$$

Rearranging terms results in

$$H(Z) = \frac{V_{out}(Z)}{V_{in}(Z)} = -\frac{C_1}{C_2} \frac{1}{Z^{\frac{1}{2}} - Z^{-\frac{1}{2}}} \qquad \text{(A1-8)}$$

Evaluating H(Z) at $Z = e^{j\omega T}$, where ω is the signal frequency and T is the clocking period, results in

$$H(e^{j\omega T}) = -\frac{C_1}{C_2} \frac{1}{e^{\frac{j\omega T}{2}} - e^{-\frac{j\omega T}{2}}} \qquad \text{(A1-9a)}$$

$$= -\frac{C_1}{C_2} \frac{1}{2\, j \sin\frac{\omega T}{2}} \qquad \text{(A1-9b)}$$

$$= -\frac{C_1}{C_2} \frac{1}{j\omega T} \left[\frac{\frac{\omega T}{2}}{\sin\left(\frac{\omega T}{2}\right)}\right] \qquad \text{(A1-10)}$$

As $\frac{\omega T}{2}$ approaches zero, or equivalently as $f_c >> \omega$,

$$\frac{\frac{\omega T}{2}}{\sin\left(\frac{\omega T}{2}\right)} \rightarrow 1 \qquad \text{(A1-11)}$$

and

$$H(e^{j\omega T}) \simeq -\frac{C_1}{C_2}\frac{1}{j\omega T} \qquad \text{(A1-12)}$$

$$= -\frac{C_1}{C_2}\frac{f_c}{j\omega}$$

The network of Figure A1-1 will be an integrator if $f_c >> f_{signal}$.

Non-Inverting Integrator

Assume that V_{in} is a constant for $nT \leq t \leq (n + \frac{1}{2})T$ as before. In the network of Figure A1-2, the charge on C_1 is given by

$$q_{C_1}(nT) = C_1 V_{in}(nT) \qquad \text{(A1-13)}$$

The charge on C_2 was last changed at $(n - \frac{1}{2})T$, so at $t = nT$, the charge on C_2 is

$$q_{C_2}(nT) = V_{out}\left[(n - \tfrac{1}{2})T\right] C_2 \qquad \text{(A1-14)}$$

At $(n + \frac{1}{2})T$, the switch is in position b. C_1 transfers its charge through the op amp to C_2 resulting in

$$q_{C_2}\left[(n + \tfrac{1}{2})T\right] = C_2 V_{out}\left[(n - \tfrac{1}{2})T\right] + C_1 V_{in}(nT) \qquad \text{(A1-15)}$$

But by definition

$$q_{C_2}\left[(n + \tfrac{1}{2})T\right] = C_2 V_{out}\left[(n + \tfrac{1}{2})T\right] \qquad \text{(A1-16)}$$

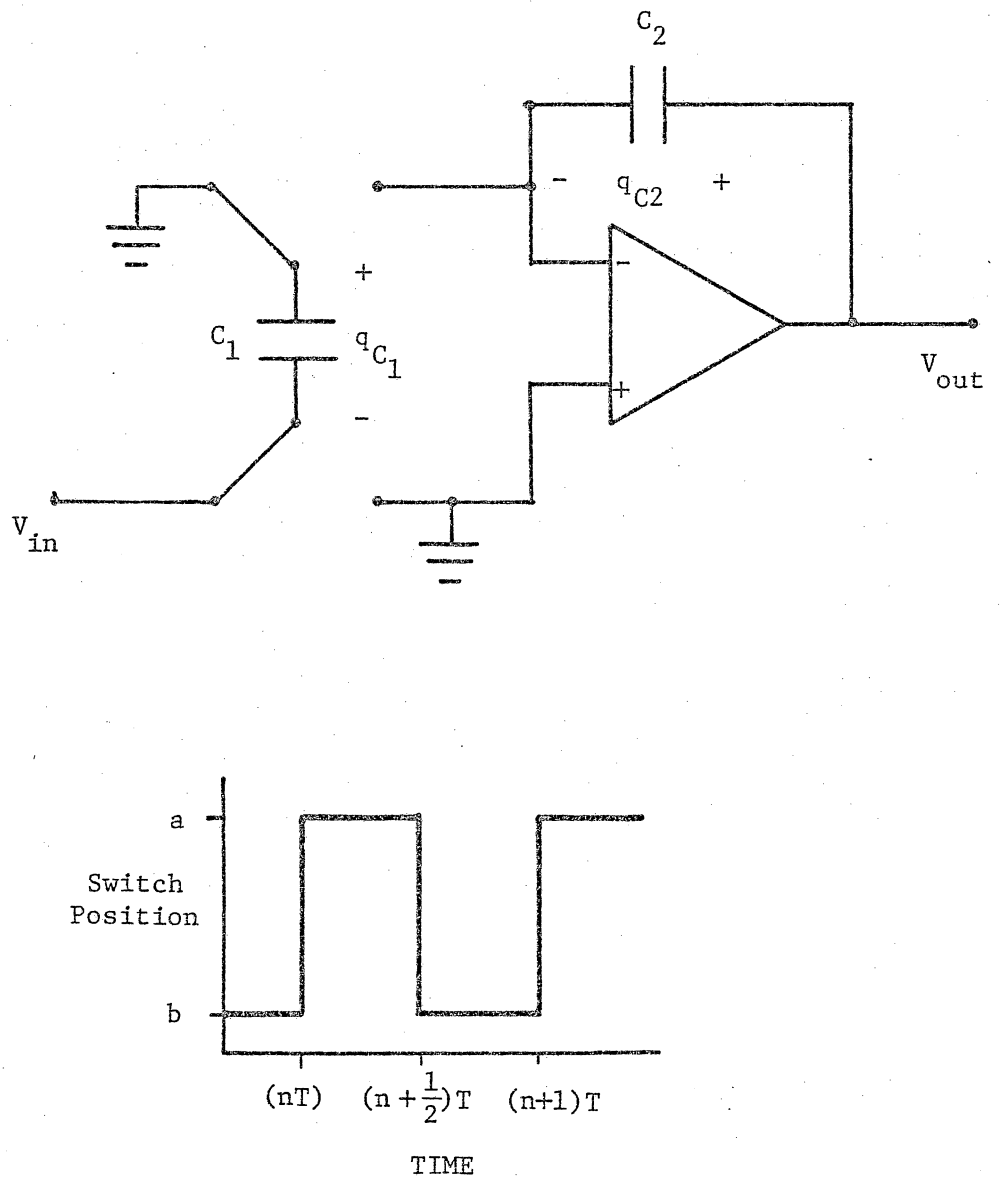


Figure A1-2. The non-inverting parasitic free SC integrator.

Substituting (A1-16) into (A1-15) results in

$$C_2\, V_{out}\left[(n+\tfrac{1}{2})T\right] = C_2\, V_{out}\left[(n-\tfrac{1}{2})T\right] + C_1\, V_{in}(nT) \qquad \text{(A1-17)}$$

Taking the Z-transform and rearranging terms results in

$$H(Z) = \frac{V_{out}(Z)}{V_{in}(Z)} = \frac{C_1}{C_2}\,\frac{1}{Z^{\frac{1}{2}} - Z^{-\frac{1}{2}}} \qquad \text{(A1-18)}$$

Following the same argument used in Eqns. (A1-9) to (A1-12)

$$H(e^{j\omega T}) \approx \frac{C_1}{C_2}\,\frac{f_c}{j\omega} \qquad \text{(A1-19)}$$

if $f_c >> \omega$.

APPENDIX 2. SCF CLOCK PHASING

Various methods of phasing the switches between adjacent stages of an SCF have been presented in the technical literature. Broderson [9] shows the switches of alternate stages transferring to the inputs of the op amps on alternate phases of the clock, while Martin [10] shows the inputs of op amps sampling the switched capacitors at the same time for all stages. In addition, Martin shows the output of a particular op amp being sampled by following stages on the same phase. Broderson follows the same rule except for the termination stages, while Trick and Davis [14] have the output of a stage being sampled at different clock phases. These various approaches make it difficult to determine a consistent rule for setting the clock phases.

To develop a general rule for the clock phasing, several different phasing schemes were examined on a third order filter with DIANA. A third order filter was chosen because it was general enough to try different phasing schemes, yet simple enough that details would not be masked.

All three phasing methods examined here used the block diagram shown in Figure A2-1. The first method shown in Figure A2-2 follows Broderson's approach in that the inputs of alternate op amps sample the switched capacitors on alternate clock phases. Furthermore, the outputs of the op amps are sampled at the same time instant except for the termination stages. The DIANA outputs of Figures A2-3 and A2-4 show that the filter performs as expected. The notch is well defined and at the desired location while the phase response exhibits

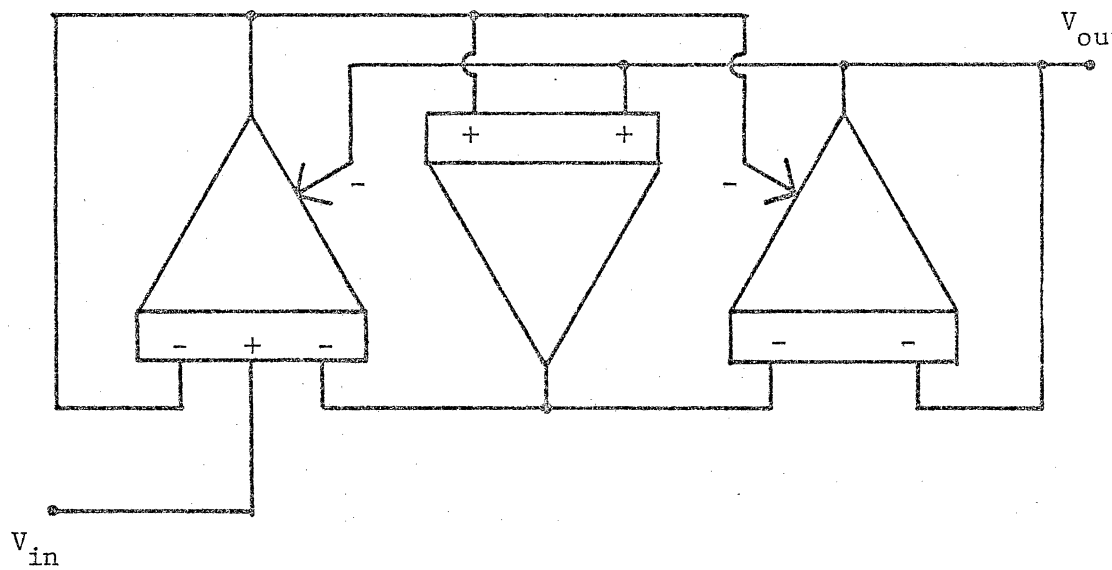


Figure A2-1. A third order SCF block diagram used to develop a switch phasing rule.

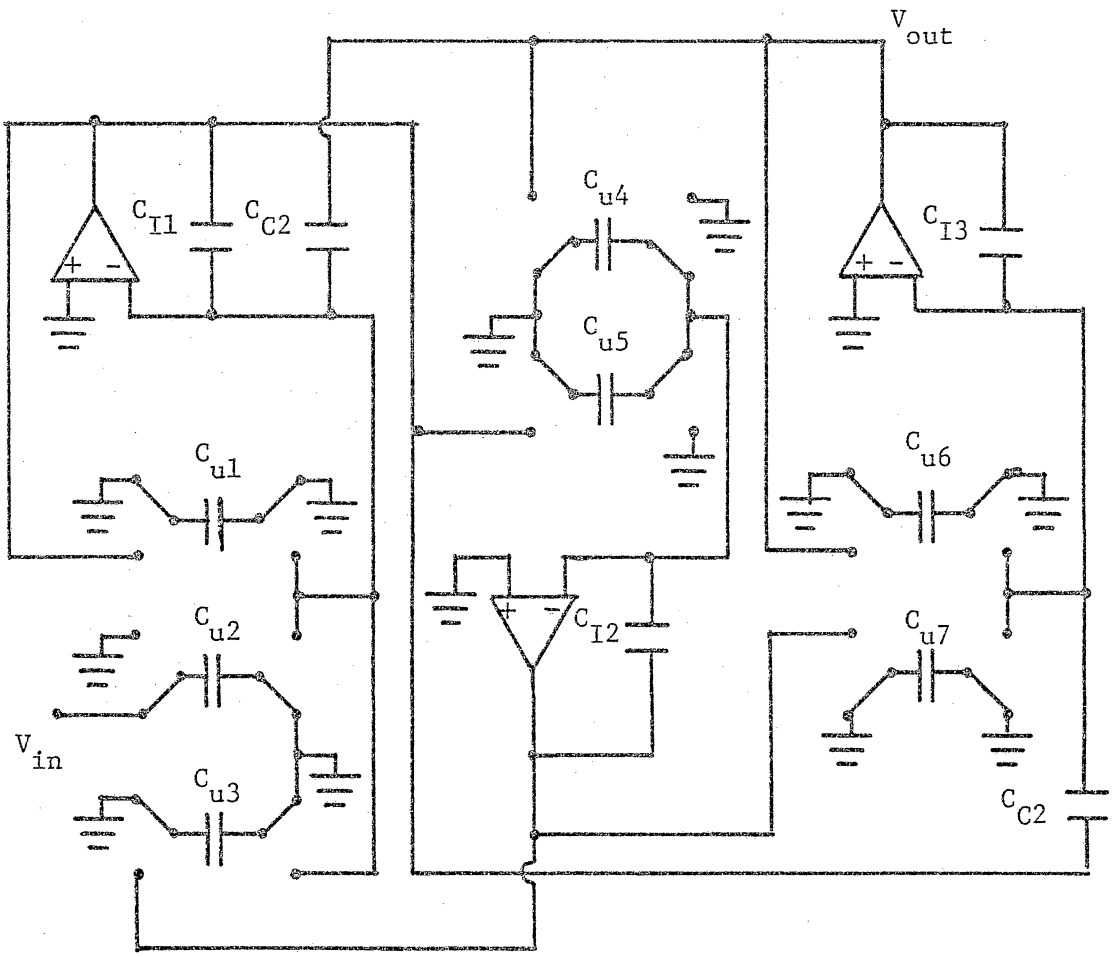


Figure A2-2. Clock phasing due to Broderson.

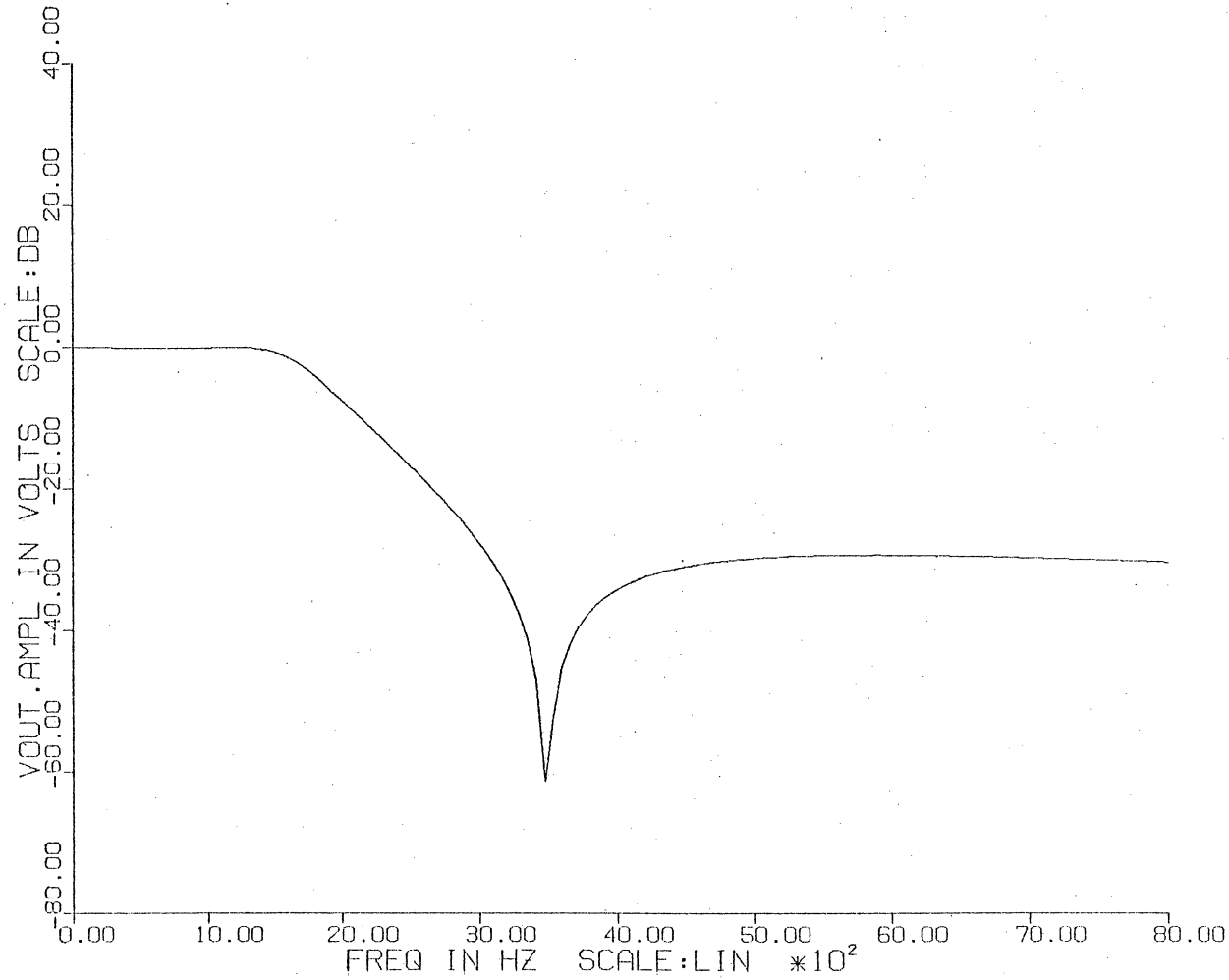


Figure A2-3. The simulated magnitude response for the SCF of Figure A2-2.

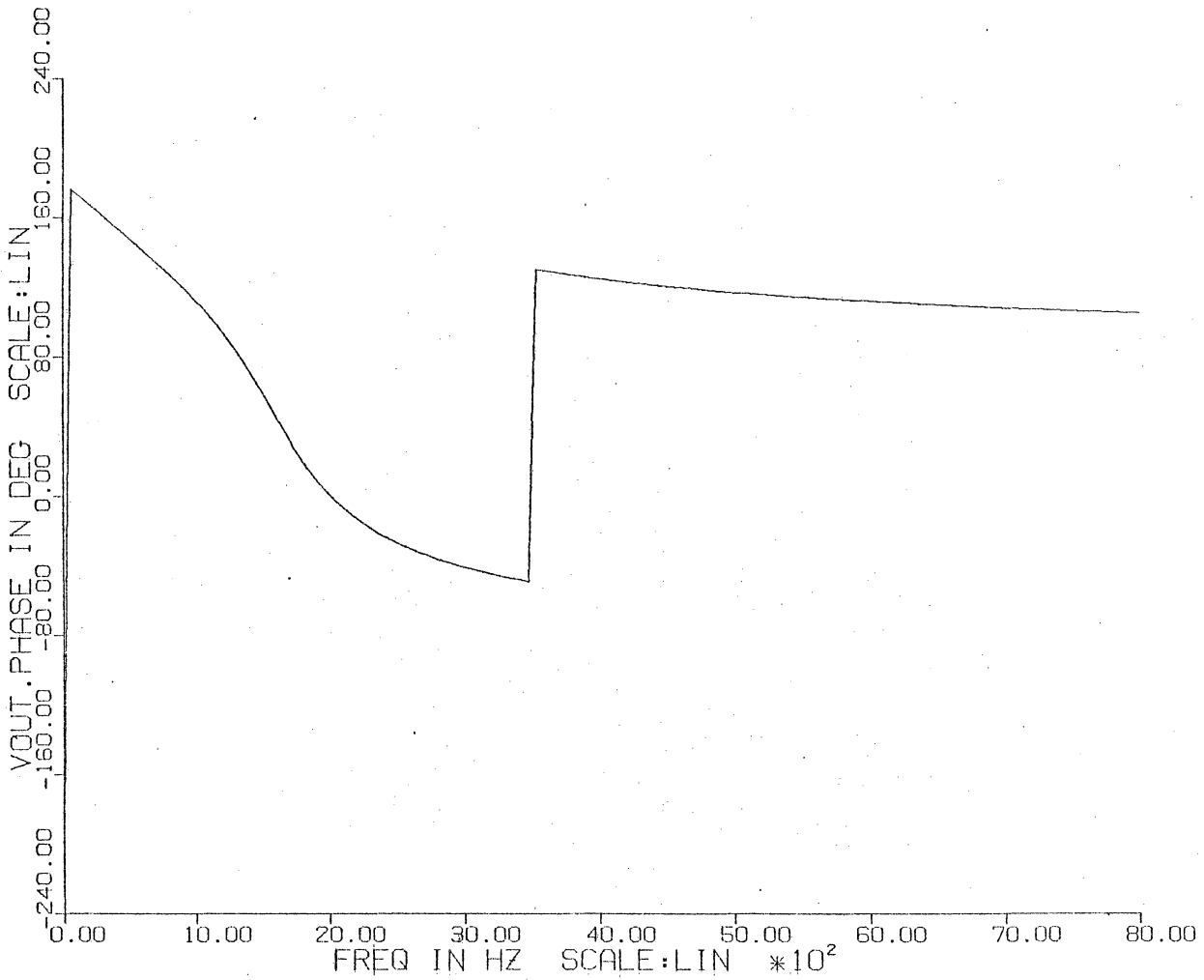


Figure A2-4. The simulated phase response for the SCF of Figure A2-2.

a sharp discontinuity at the notch frequency.

The switching arrangement shown in Figure A2-5 was selected at random. Basically the only difference is that the switch phasing of the third stage is reversed from that of Figure A2-2. The op amp of stage 1 samples the switched capacitor at ϕ_1 while stages 2 and 3 sample the switched capacitors associated with those stages at ϕ_2. This method does not yield a satisfactory response, as seen from the magnitude plot of Figure A2-6. The notch quality has clearly deteriorated while the stopband rejection has decreased by 2 dB. In addition, the phase response of Figure A2-7 shows no discontinuity at the notch frequency. The third arrangement is shown in Figure A2-8 and is similar to Martin's approach. All op amp inputs sample the switched capacitors at the same time, but the outputs of the op amps are not all sampled at the same time instant. This method of switching, together with that due to Martin, was simulated and found to yield identical results to those shown in Figures A2-3 and A2-4. Hence, these arrangements also perform satisfactorily.

The switch phasing method shown in Figure A2-9 is due to Trick and Davis. An all pole filter was designed using the original flowgraph from the LC prototype. The inputs of alternate op amps sample the switched capacitors on alternate clock phases. The output of a particular op amp is not necessarily sampled at the same time by all stages which it feeds. This arrangement was simulated and found to yield the desired output. In examining these four methods, the following procedure for clock phasing holds:

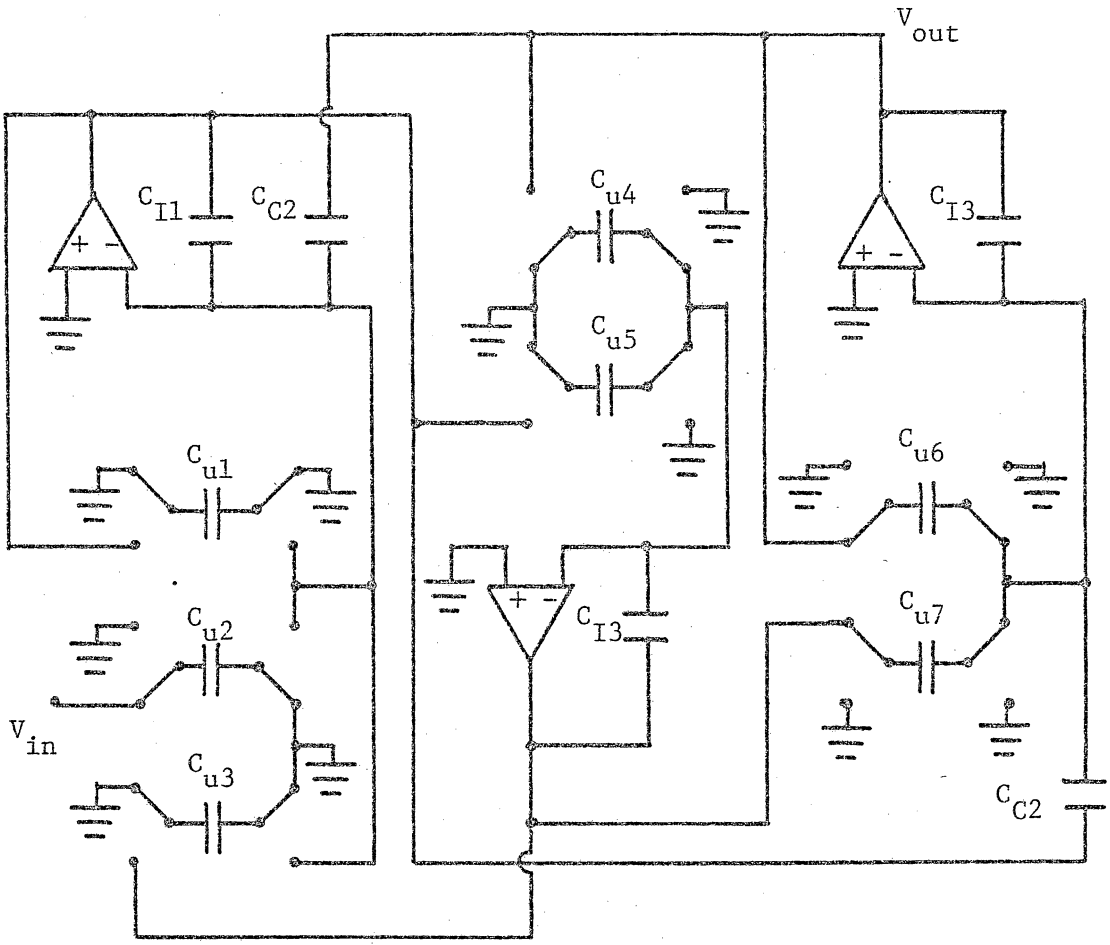


Figure A2-5. Random switch phasing of the third order SCF.

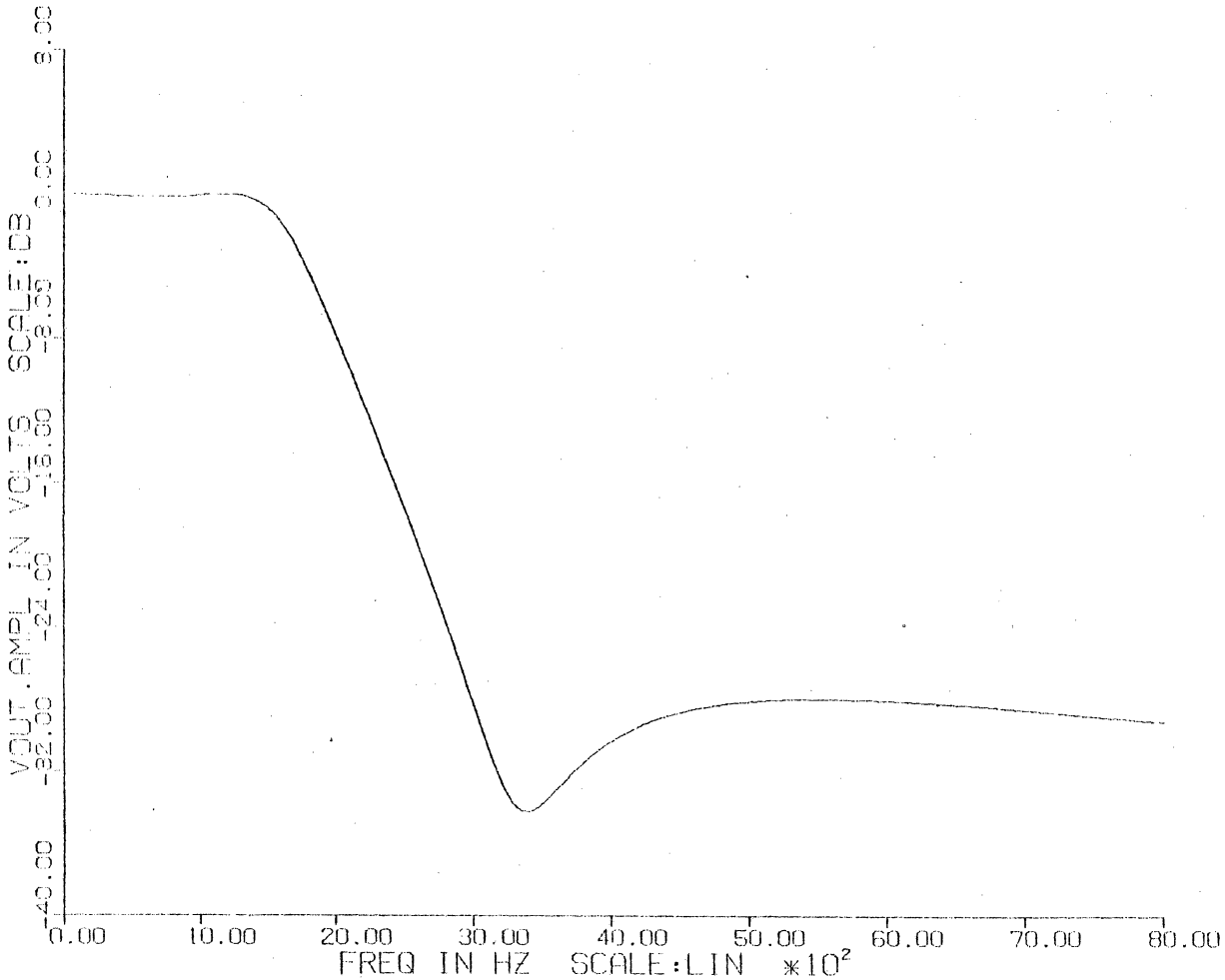


Figure A2-6. The simulated magnitude response for the SCF of Figure A2-5.

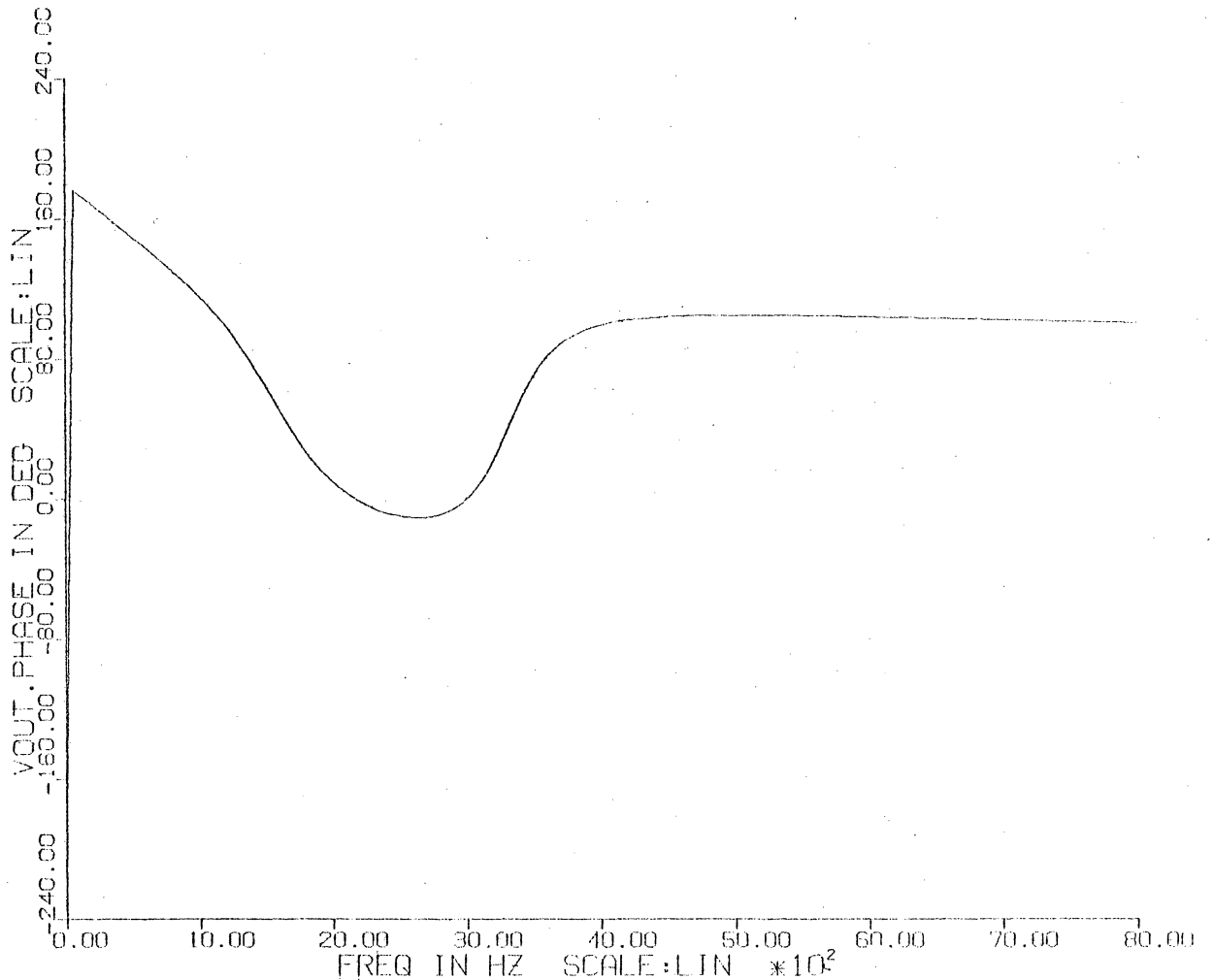


Figure A2-7. The simulated phase response for the SCF of Figure A2-5.

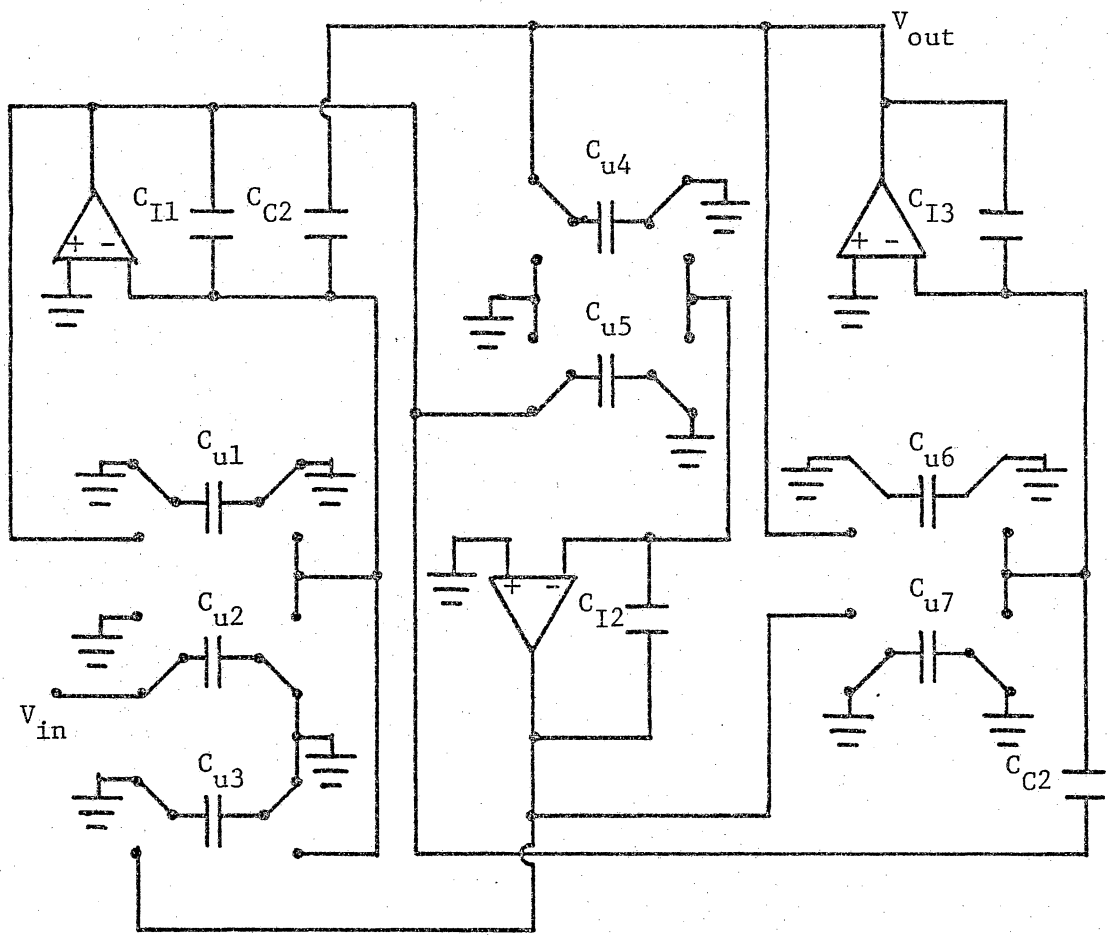


Figure A2-8. Switch phasing similar to Martin's.

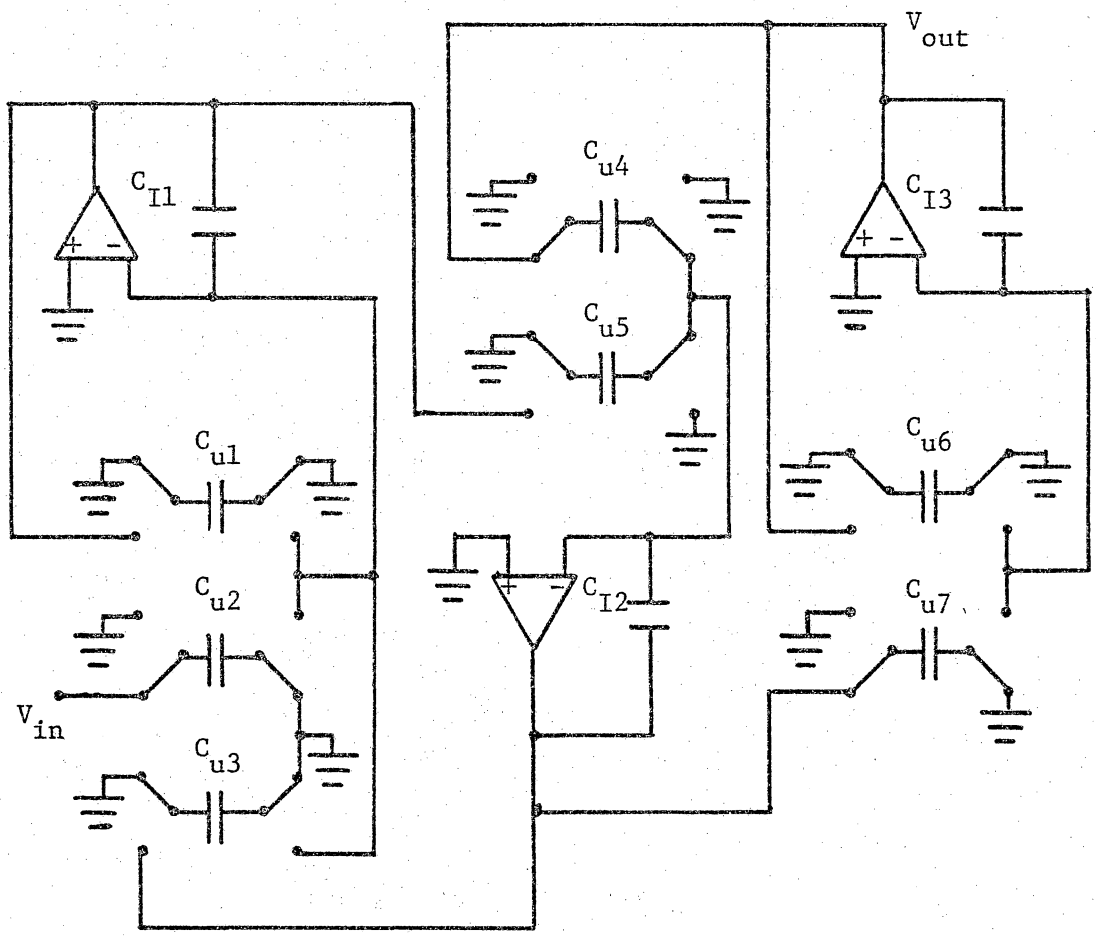


Figure A2-9. Switch phasing due to Trick and Davis.

1) Set up the block diagram to obtain the necessary negative summing inputs for the stages by negating appropriate nodes, then

2) Choose one of two methods for setting the switch phasing:

   a) have all the inputs of the op amps sample the switched capacitors at the same clock phase, or

   b) have the inputs of op amps on alternate stages sample the switched capacitors on alternate clock phases.

APPENDIX 3. DERIVATION OF CAPACITOR RATIOS

This appendix shows the development of the capacitor ratios for stages 2-7. First note that from the equalities for stage 1, $\frac{R_T}{R_S} = 1$.

Stage 2

$$V_2^{SFG} = \frac{\omega_{co} R_S}{sL_2 R_T} (-V_1^{SFG} - V_3^{SFG}) \tag{A3-1}$$

$$V_2^{SCF} = \frac{f_c C_u}{sC_{I2}} (-V_1^{SCF} - V_3^{SCF}) \tag{A3-2}$$

Comparing A3-1 and A3-2 results in

$$\frac{\omega_{co} R_S}{L_2 R_T} = \frac{f_c C_u}{C_{I2}} \tag{A3-3}$$

or

$$\boxed{\frac{C_{I2}}{C_u} = L_2 \left(\frac{f_c}{\omega_{co}}\right)} \tag{A3-4}$$

Stage 3

$$V_3^{SFG} = \frac{\omega_{co}}{s(C_2+C_3+C_4)} (V_2^{SFG} + V_4^{SFG}) - \frac{C_2}{C_2+C_3+C_4} V_1^{SFG} - \frac{C_4}{C_2+C_3+C_4} V_5^{SFG} \tag{A3-5}$$

$$V_3^{SCF} = \frac{f_c C_u}{sC_{I3}} (V_2^{SCF} + V_3^{SCF}) - \frac{C_{C2}}{C_{I3}} V_1^{SCF} - \frac{C_{C4}}{C_{I3}} V_5^{SCF} \tag{A3-6}$$

From (A3-5) and (A3-6),

$$\frac{\omega_{co}}{(C_2+C_3+C_4)} = \frac{f_c C_u}{C_{I3}} \tag{A3-7}$$

or

$$\boxed{\frac{C_{I3}}{C_u} = (C_2+C_3+C_4)\left(\frac{f_c}{\omega_{co}}\right)} \tag{A3-8}$$

Also,

$$\frac{C_{C2}}{C_{I3}} = \frac{C_2}{C_2+C_3+C_4} \tag{A3-9}$$

Substituting (A3-9) into (A3-8) results in

$$\boxed{\frac{C_{C2}}{C_u} = C_2\left(\frac{f_c}{\omega_{co}}\right)} \tag{A3-10}$$

In a similar manner,

$$\boxed{\frac{C_{C4}}{C_u} = C_4\left(\frac{f_c}{\omega_{co}}\right)} \tag{A3-11}$$

Stage 4

$$V_4^{SFG} = \frac{\omega_{co}}{sL_4}\left(-V_3^{SFG} - V_5^{SFG}\right) \tag{A3-12}$$

$$V_4^{SCF} = \frac{f_c C_u}{sC_{I4}}\left(-V_3^{SCF} - V_5^{SCF}\right) \tag{A3-13}$$

$$\frac{\omega_{co}}{L_4} = \frac{f_c C_u}{C_{I4}} \tag{A3-14}$$

$$\boxed{\frac{C_{I4}}{C_u} = L_4 \left(\frac{f_c}{\omega_{co}}\right)} \tag{A3-15}$$

Stage 5

$$V_5^{SFG} = \frac{\omega_{co}}{s(C_4+C_5+C_6)} (V_4^{SFG} + V_6^{SFG}) - \frac{C_4}{(C_4+C_5+C_6)} V_3^{SFG} - \frac{C_6}{C_4+C_5+C_6} V_7^{SFG} \tag{A3-16}$$

$$V_5^{SCF} = \frac{f_c C_u}{sC_{I5}} (V_4^{SCF} + V_6^{SCF}) - \frac{C_{C4}}{C_{I5}} V_3^{SCF} - \frac{C_{C6}}{C_{I5}} V_7^{SCF} \tag{A3-17}$$

From A3-16 and A3-17,

$$\frac{\omega_{co}}{C_4+C_5+C_6} = \frac{f_c C_u}{sC_{I5}} \tag{A3-18}$$

$$\boxed{\frac{C_{I5}}{C_u} = (C_4+C_5+C_6) \frac{f_c}{\omega_{co}}} \tag{A3-19}$$

Also,

$$\frac{C_6}{C_4+C_5+C_6} = \frac{C_{C6}}{C_{I5}} \tag{A3-20}$$

Substituting (A3-20) into (A3-19) results in

$$\boxed{\frac{C_{C6}}{C_u} = C_6 \left(\frac{f_c}{\omega_{co}}\right)} \qquad \text{(A3-21)}$$

Stage 6

$$V_6^{SFG} = \frac{\omega_{co}}{sL_6} \left(-V_5^{SFG} - V_7^{SFG}\right) \qquad \text{(A3-22)}$$

$$V_6^{SCF} = \frac{f_c C_u}{sC_{I6}} \left(-V_5^{SCF} - V_7^{SCF}\right) \qquad \text{(A3-23)}$$

Comparing (A3-22) and (A3-23) results in

$$\frac{\omega_{co}}{L_6} = f_c \frac{C_u}{C_{I6}} \qquad \text{(A3-24)}$$

$$\boxed{\frac{C_{I6}}{C_u} = L_6 \left(\frac{f_c}{\omega_{co}}\right)} \qquad \text{(A3-25)}$$

Stage 7

$$V_7^{SFG} = \frac{\omega_{co}}{s(C_6+C_7)} \left(V_6 - \frac{V_7}{R_2}\right) - \frac{C_6}{C_6+C_7} V_5 \qquad \text{(A3-26)}$$

$$V_7^{SCF} = \frac{f_c C_u}{sC_{I7}} \left(V_6^{SCF} - V_7^{SCF}\right) - \frac{C_{C6}}{C_{I7}} V_5 \qquad \text{(A3-27)}$$

Since $R_2 = 1\ \Omega$, (A3-26) and (A3-27) yield

$$\frac{\omega_{co}}{C_6+C_7} = \frac{f_c C_u}{C_{I7}} \tag{A3-28}$$

$$\boxed{\frac{C_{I7}}{C_u} = (C_6+C_7)\left(\frac{f_c}{\omega_{co}}\right)} \tag{A3-29}$$

All of these equations are summarized in Table 2.1-2.

APPENDIX 4. RECOVERY OF THE SECOND NOTCH

The second notch never appeared in the original seventh order filter. It was confirmed during filter testing that the notches were produced by the feedforward summing capacitors connecting stages 1, 3, 5, and 7. Removing one of these capacitors eliminates the notch associated with it. The notches are produced by the capacitors listed below:

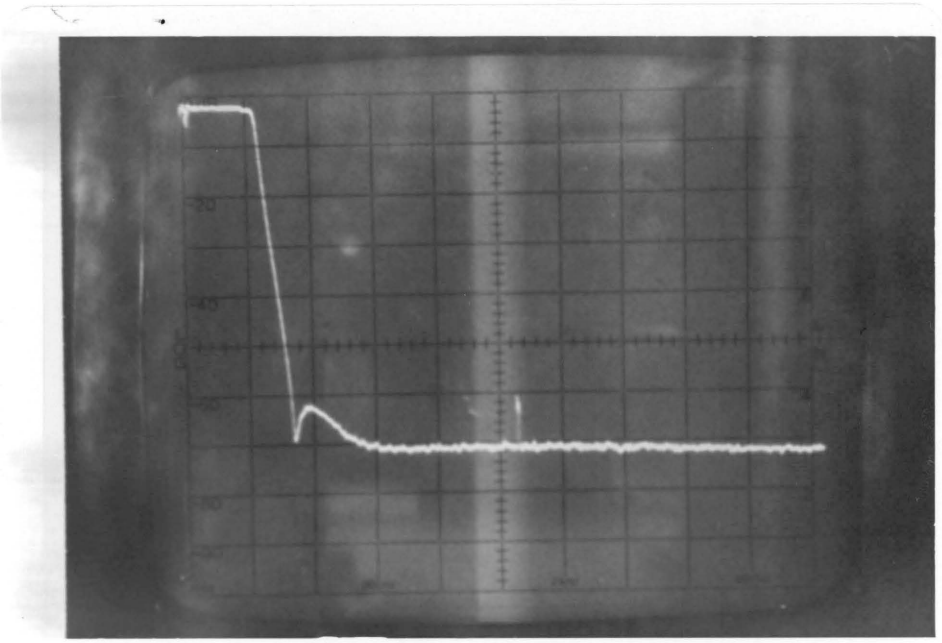
C_{C22}, the feedforward capacitor from stage 1 to stage 3, produces the third notch at 3,94 kHz.

C_{C42}, the feedforward capacitor from stage 3 to stage 5, produces the first notch at 1.87 kHz.

C_{C62}, the feedforward capacitor from stage 5 to stage 7, produces the second notch at 2.27 kHz.

Since the second notch never appeared, these capacitors were alternately removed from the scaled filter to verify that C_{C62} was connected, as shown in Table A4-1.

The first two tests show that C_{C62} was indeed connected in the filter, but the last two tests show that when the first notch is in the network, the second notch does not appear. Since the first notch at 1.87 kHz is produced in the filter before the second notch at 2.27 kHz, the introduction of the first notch reduces the signal level available at 2.27 kHz. This reduction is evidently sufficient to bury the feedforward signal from stage 5 to stage 7 in the op amp noise of the seventh stage.



Reference Level	-10 dBV
Amplitude Scale	10 dB/div
Start Frequency	0 kHz
Frequency Scale	500 Hz/div
Resolution Bandwidth	30 Hz
f_{clock}	25 kHz

Figure A4-1. The response of the scaled filter was missing the second notch before the dynamic range optimization.

Table A.4-1. Tests showed that the second notch was not produced when the first notch was in the filter.

Feedforward Capacitor	C_{C22}	C_{C42}	C_{C62}	RESULTS		
Produces	Third Notch	First Notch	Second Notch	First Notch	Second Notch	Third Notch
Test #1	Out	Out	In	No	Yes	No
Test #2	In	Out	In	No	Yes	Yes
Test #3	Out	In	In	Yes	No	No
Test #4	Out	In	Out	Yes	No	No

To check this,the S/N ratio of the seventh stage was increased by multiplying the voltage gains into the seventh stage by 10 and dividing the voltage gains out of the seventh stage by 10, as shown in Figure A4-2. The op amp internal noise can be shown explicitly as a separate source, as in Figure A4-3. After the gains are changed, the signal power levels are unchanged, since they are multiplied by 100 and divided by 100. However, the internal noise power of the seventh stage op amp is only divided by 100, thus increasing the S/N ratio by 20 dB for all inputs.

The changes of Figure A4-2 were made to the scaled filter and the second notch appeared as shown in Figure A4-4. This confirms that the S/N ratio of the feedforward path from stage 5 to stage 7 was too small.

Based on the results of these tests, the dynamic range of the filter was optimized. As shown in Figure 2.1-12, the S/N ratio of the seventh stage is increased as well as the remaining odd stages, thus producing the same effect as the gain adjustment described above.

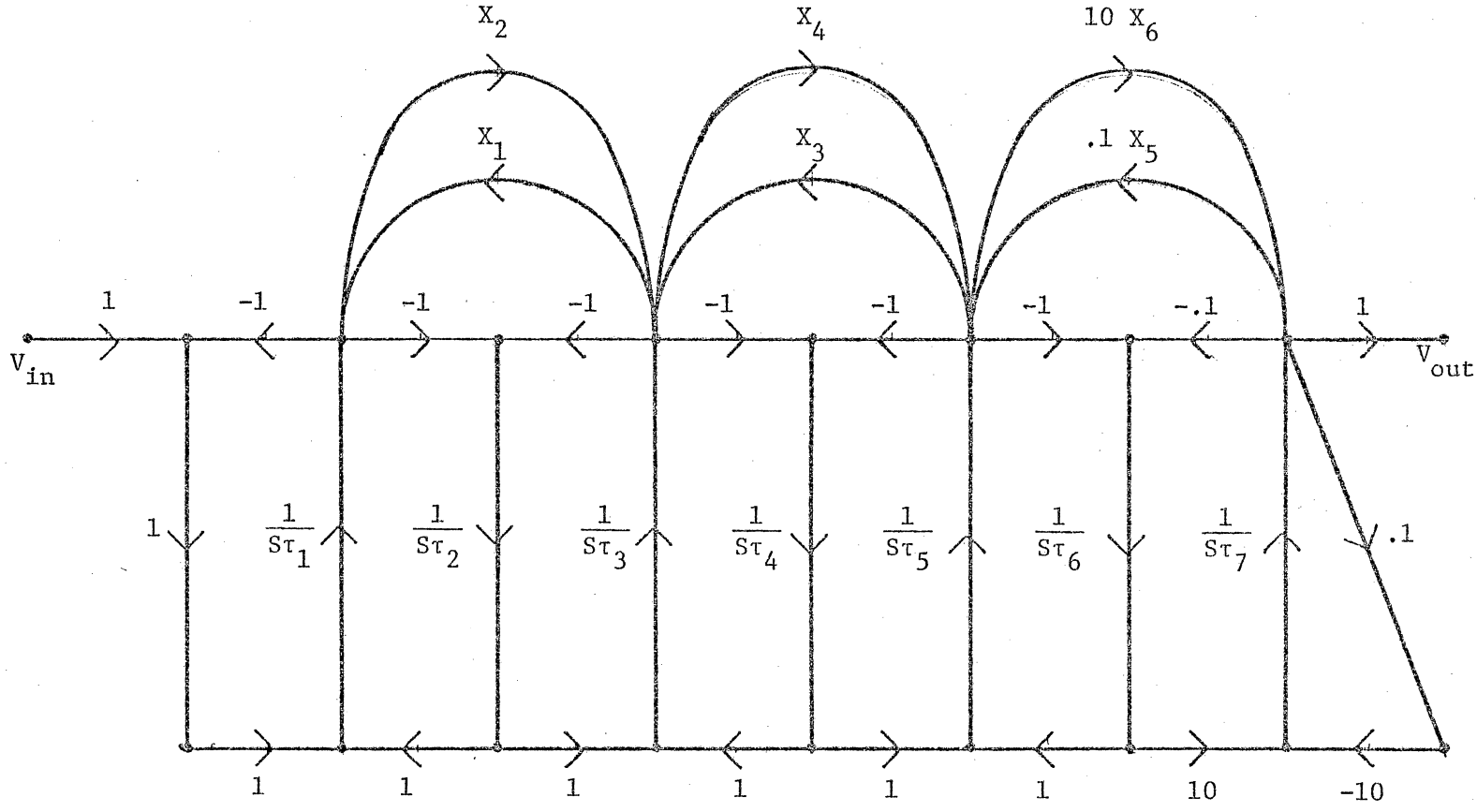
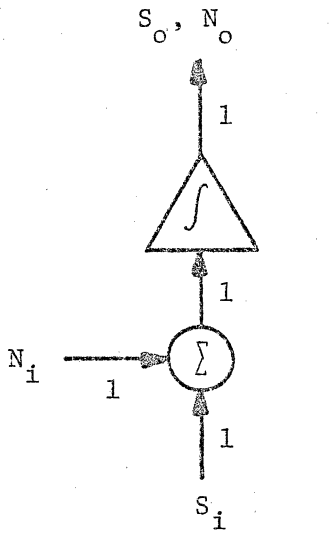
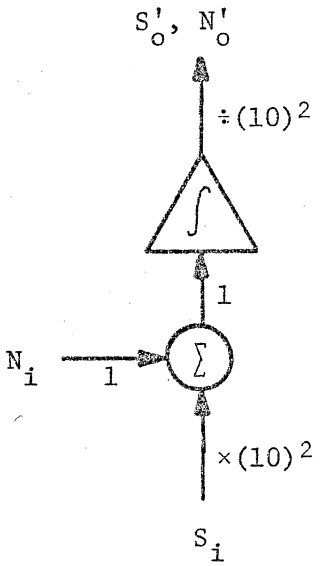


Figure A4-2. SFG showing the 10X gain adjustment of the seventh stage.

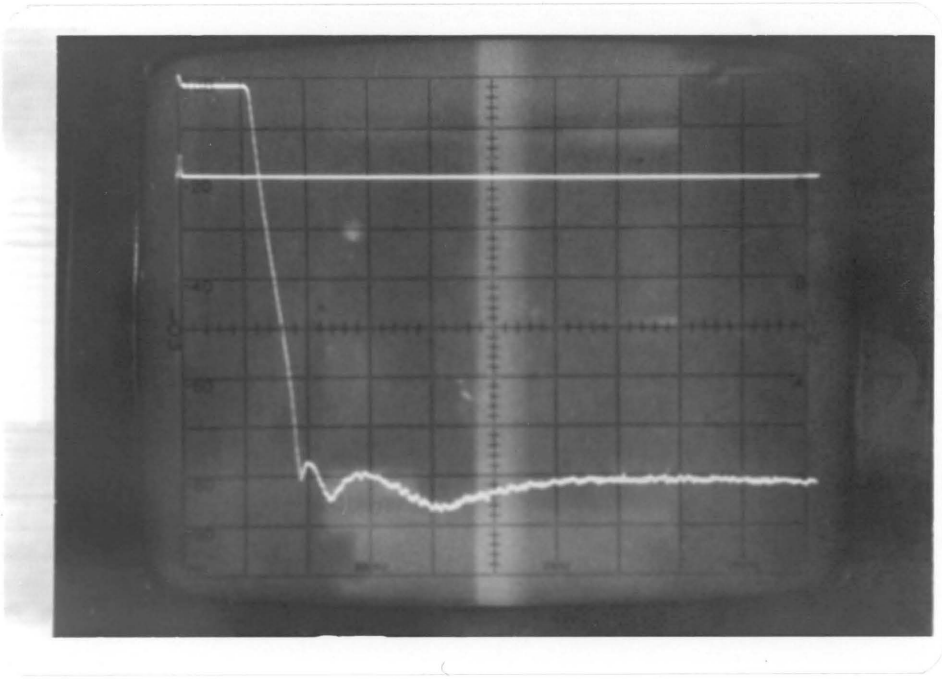


$$NR = \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}}$$



$$NR' = \frac{\frac{S_i}{N_i}}{\frac{S'_o}{N'_o}} = \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_{o/100}}} = \frac{NR}{100}$$

Figure A4-3. Changing the gains of the last stage reduces its noise power by 100.



Reference Level	+10 dBV
Amplitude Scale	10 dB/div
Start Frequency	0 kHz
Frequency Scale	500 Hz/div
Resolution Bandwidth	10 Hz
f_{clock}	25 kHz

Figure A4-4. The 10X gain adjustment in the last stage produced all three notches in the scaled filter.

APPENDIX 5. DIGITAL CLOCK SOURCE

The study of the scaled-capacitor filter pointed out the need for a very stable, precise clock source. The analog clock source of Figure 2.1-17 had to be set up every day and is subject to drift. Thus it cannot be set repeated to the same duty cycles or the same relative phase between ϕ_1 and ϕ_2. To avoid these problems, a digital clock source for ϕ_1 and ϕ_2 has been designed and built. This appendix presents the design details of the system.

The switched capacitor of Figure A5-1a is implemented with 4 SPST switches and 2 clocks ϕ_1 and ϕ_2, as shown in Figure A5-1b. The switches of Figure A5-1b are off when their clock inputs are high, and they are on when their clock inputs are low. A detailed diagram of the relationship between ϕ_1 and ϕ_2 is shown in Figure A5-2. As can be seen, four time intervals are necessary to specify ϕ_1 and ϕ_2:

1) T_1, the period of ϕ_1 ($T_1 = 1/f_{clock}$).
2) T_{1HI}, the time when ϕ_1 is high.
3) T_{12}, the time between ϕ_1 going high and ϕ_2 going high.
4) T_{2HI}, the time when ϕ_2 is high.

The period of ϕ_2 is not specified since ϕ_2 is synchronized with ϕ_1. Also, the duty cycles of ϕ_1 and ϕ_2 don't need to be set independently, so $T_{2HI} = T_{1HI}$.

In a digital network, these times are set by dividing the clock period T_1 into N subintervals. Then, by counting the subintervals, the desired time intervals may be accurately set. One drawback of this approach is the infinite resolution of analog system is not available.

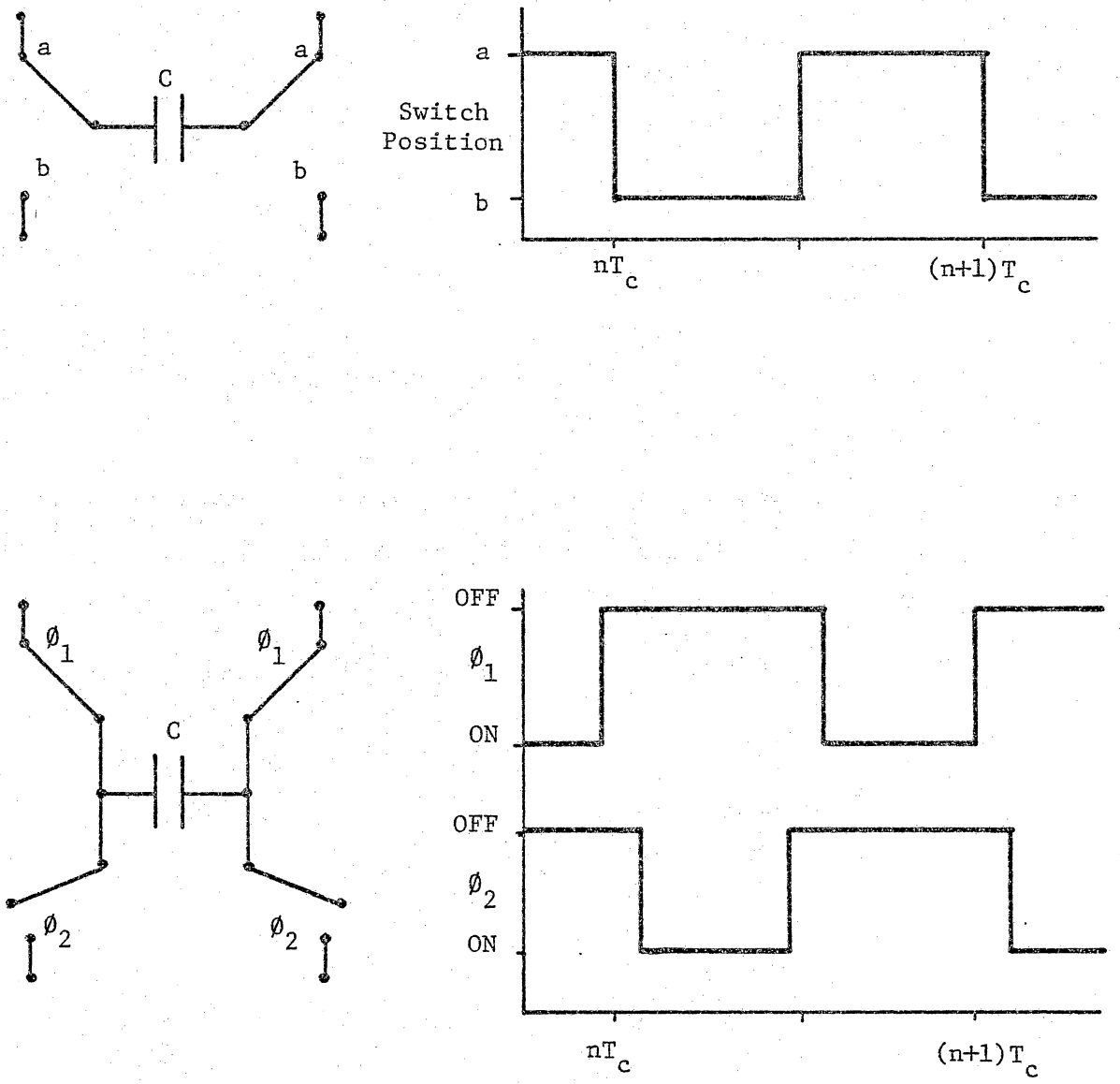


Figure A5-1. The switched capacitor of (a) is realized with 4 switches and two non-overlapping clocks.

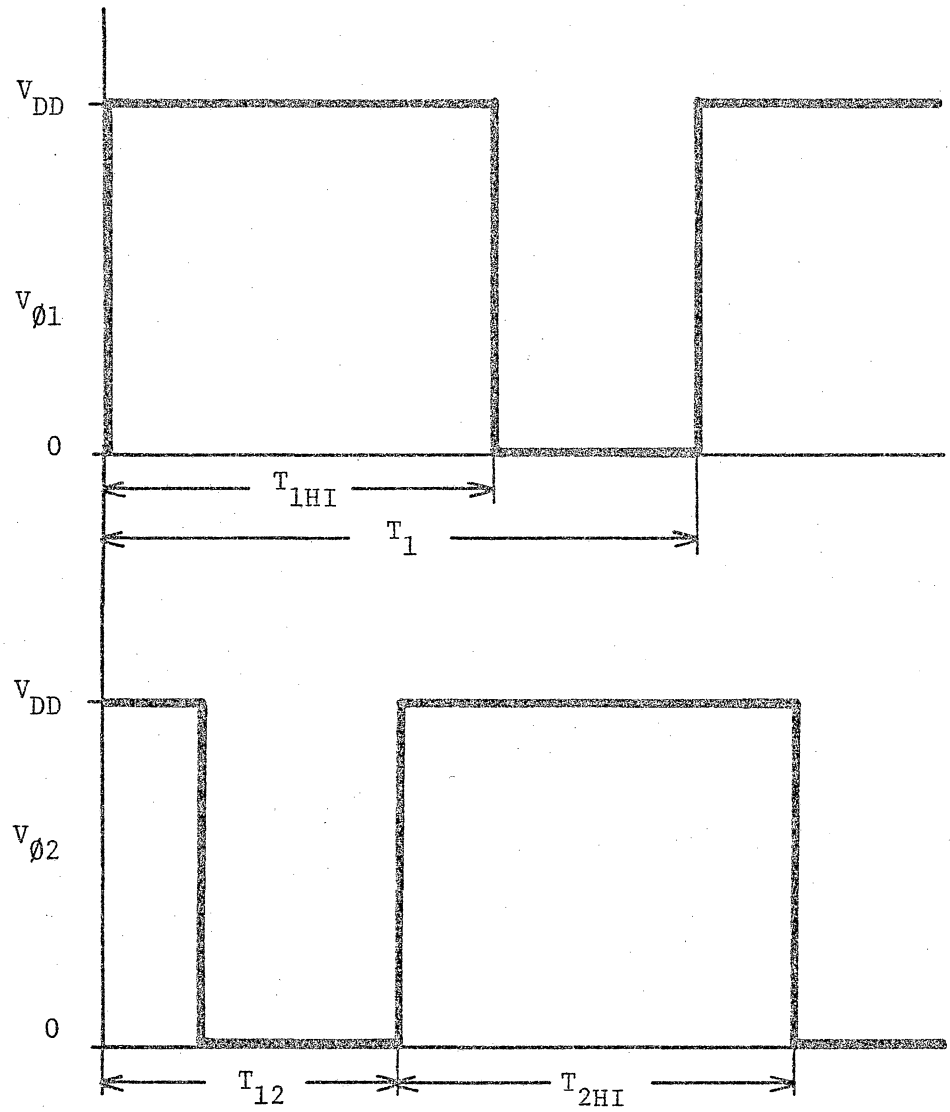


Figure A5-2. The relationship between ϕ_1 and ϕ_2 can be specified by T_1, T_{1OFF}, T_{12}, T_{2OFF}.

Only time intervals which are integer multiples of $\frac{T_1}{N}$ can be resolved. For this clock source, N was chosen to be 100 and therefore time intervals can be set to 1% of a period.

The clock period is divided into 100 subintervals by clocking a series of down counters at $100 \cdot f_{clock}$ as shown in Figure A5-3. When the counters reach zero they set or reset two RS flipflops, FF1 and FF2. Two of the counters, the Period Counter and the DC1 (Duty Cycle $\emptyset_1$) counter, in conjunction with FF1, control the duty cycle of $\emptyset_1$. The other two counters, the RP (Relative Phase) counter and the DC2 (Duty Cycle $\emptyset_2$) counter, along with FF2, controls the duty cycle of $\emptyset_2$ and the relative phase between $\emptyset_1$ and $\emptyset_2$.

The Period Counter is a divide-by-100 block. As shown in Figure A5-4, at the start of a cycle, it is loaded with 100 and counts down to zero. When it reaches zero, $S\emptyset_1$ (Set $\emptyset_1$) goes high, and the Period Counter is reloaded with 100 and commences counting down to zero again. $S\emptyset_1$ also sets FF1, causing $\emptyset_1$ to go high.

$S\emptyset_1$ loads the DC1 counter and the RP counter with, respectively, N_{1HI} and N_{12}. N_{1HI} is the percentage of the clock period that $\emptyset_1$ is high (analogous to T_{1HI}) and N_{12} is the percentage of the clock period between $\emptyset_1$ going high and $\emptyset_2$ going high. Both of these counters start counting down to zero.

When the DC1 counter reaches zero, R$\emptyset$1 goes high, resetting FF1, and causing $\emptyset_1$ to go low. DC1 will continue to count down until S$\emptyset$1 goes high, reloading it with N_{1HI}. $\emptyset_1$ will remain low until $S\emptyset_1$ occurs and sets FF1.

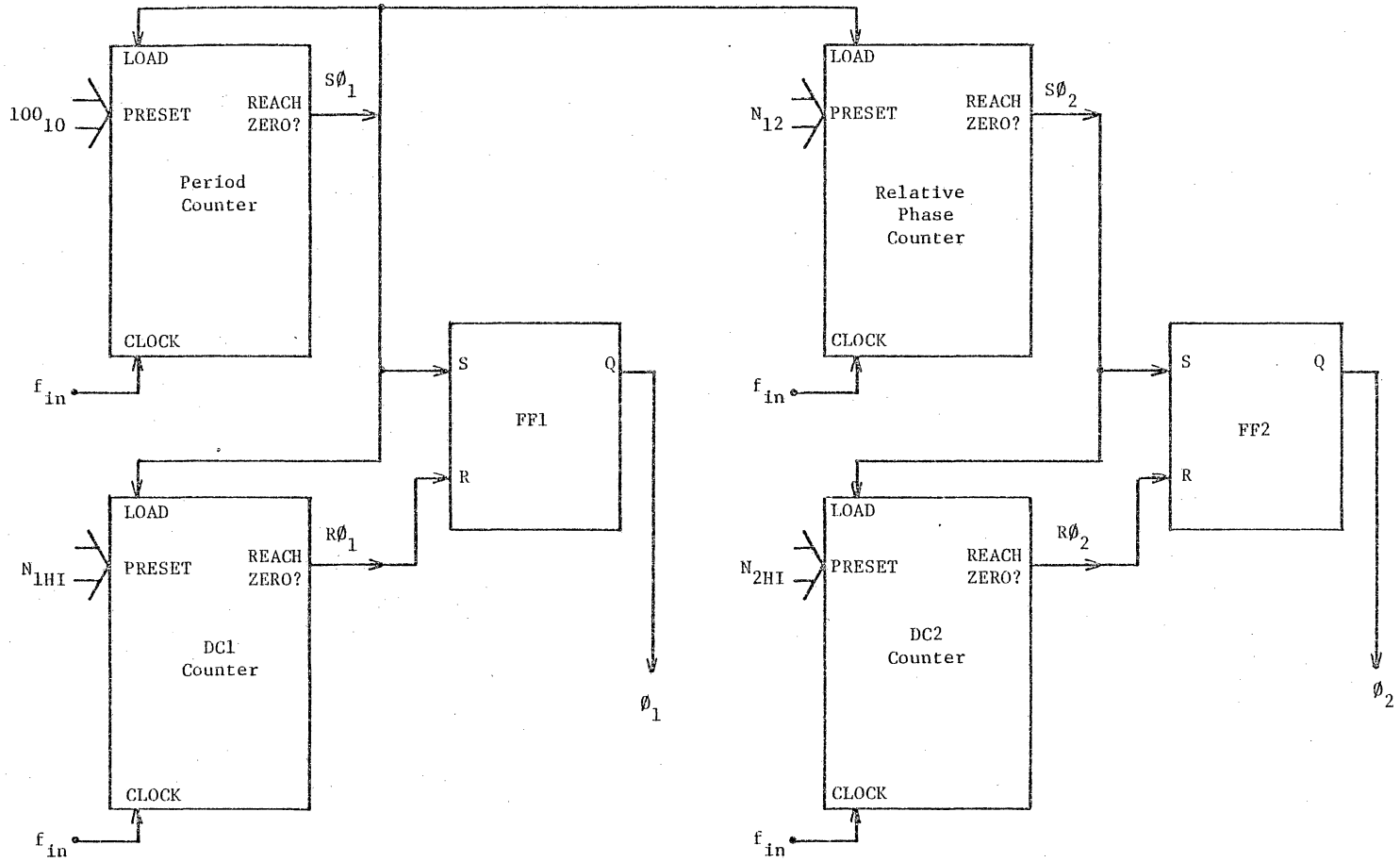


Figure A5-3. Block diagram for the digital clock source.

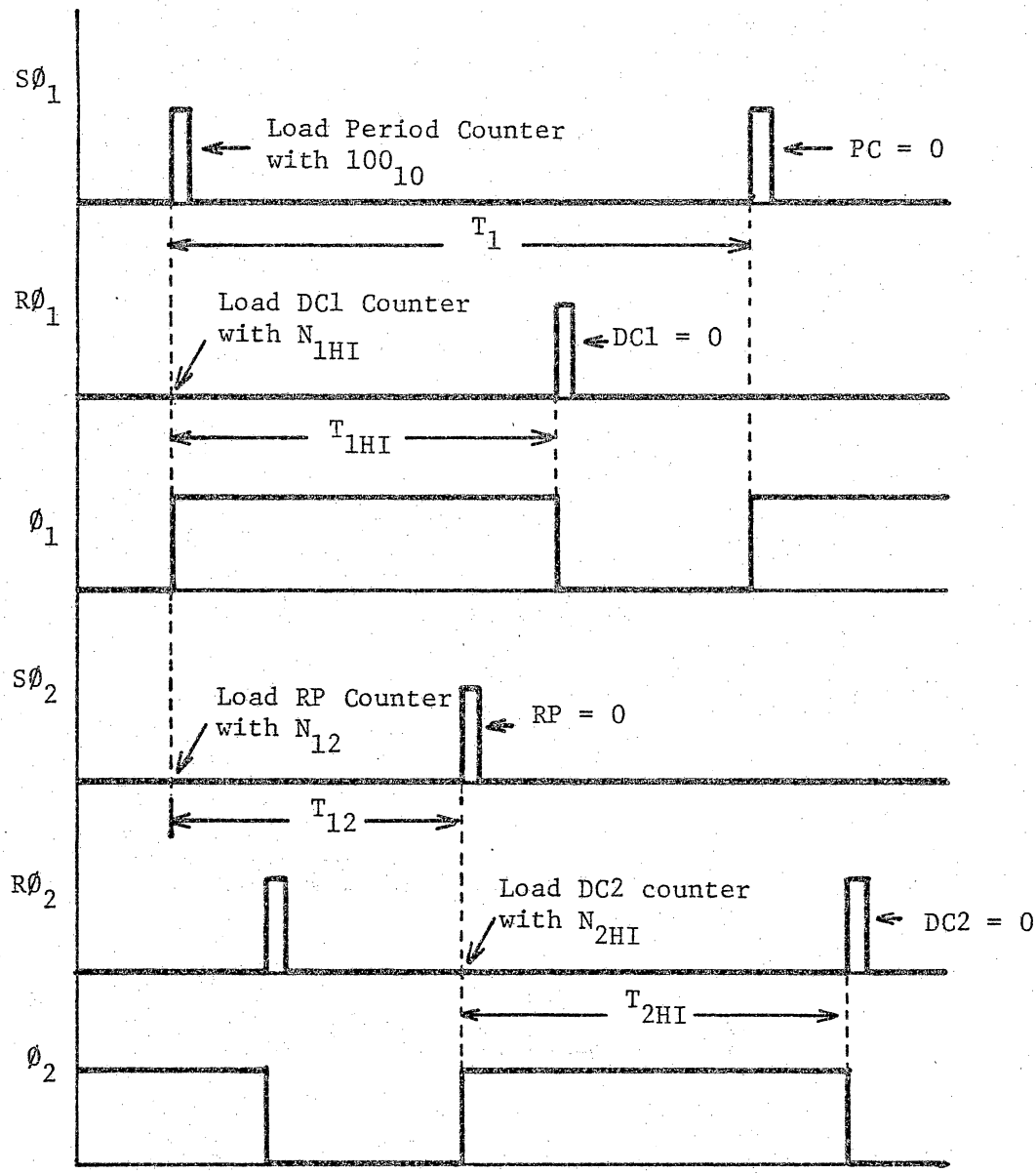


Figure A5-4. Timing diagram for the digital clock source.

Meanwhile, the RP counter is counting to zero. When it reaches zero, SØ2 goes high, setting FF2 and causing $\emptyset_2$ to go high. SØ2 also causes the DC2 counter to be loaded with $N_{2HI} = N_{1HI}$, and DC2 starts counting to zero. $R\emptyset_2$ goes high when DC2 reaches zero, resetting FF2, and causing $\emptyset_2$ to go low. The DC2 counter continues counting down until RØ2 goes high and $\emptyset_2$ remains low until SØ2 goes high.

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