

Low Power PMIC Design with Regulated Output Voltage and Maximum Power Point Tracking for Body Heat Energy Harvesting

Quinn Brogan

Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

Dong S. Ha, Chair
Qiang Li, Co-Chair
Kwang-Jin Koh

April 28, 2016
Blacksburg, Virginia

Keywords: Boost Converter, Energy Harvesting, Thermoelectric Generators, Ultralow
Power IC

Copyright 2016, Quinn L. Brogan

Low Power PMIC Design with Regulated Output Voltage and Maximum Power Point Tracking for Body Heat Energy Harvesting

Quinn L. Brogan

(ABSTRACT)

As wearable technology and wireless sensor nodes become more and more ubiquitous, the batteries required to power them have become more and more unappealing as they limit lifetime and scalability. Energy harvesting from body heat provides a solution to these limitations. Energy can be harvested from body heat using thermoelectric generators, or TEGs. TEGs provide a continuous, scalable, solid-state energy source ideal for wearable and wireless electronics and sensors. Unfortunately, current TEG technology produces low power (< 1 mW) at a very low voltage (20-90 mV) and require the load to be matched to the TEG internal resistance for maximum power transfer to occur. This thesis research proposes a power management integrated circuit (PMIC) that steps up ultralow voltages generated by TEGs to a regulated 3 V, while matching the internal resistance.

The proposed boost converter aims to harvest energy from body heat as efficiently and flexibly as possible by providing a regulated 3 V output that can be used by a variable load. A comparator-based burst mode operation affords the converter a high conversion ratio at high efficiency, while fractional open circuit voltage maximum power point tracking ensures that the controller can be used with a variety of TEGs and TEG setups. This control allows the converter to boost input voltages as low as 50 mV, while matching a range of TEG internal source resistances in one stage.

The controller was implemented in $0.25\ \mu\text{m}$ CMOS and taped out in February 2016. Since these fabricated chips will not be completed and delivered until May 2016, functionality has only been verified through simulation. Simulation results are promising and indicate that the peak overall efficiency is 81% and peak low voltage, low power efficiency is 73%. These results demonstrate the the proposed converter can achieve overall efficiencies comparable to current literature and low power efficiencies better than similar wide range converters in literature.

Low Power PMIC Design with Regulated Output Voltage and Maximum Power Point Tracking for Body Heat Energy Harvesting

Quinn L. Brogan

(GENERAL AUDIENCE ABSTRACT)

Technology is progressing to the point where wearable electronics can perform functions from healthcare (e.g. Fitbit, wireless health sensors) to social media (e.g. Apple watch). However, the wearable and overall lifetimes of these technologies are often dictated by the lifetime of the battery. Similarly, the battery size limits how small these electronics can become.

Energy harvesting refers to techniques that scavenge energy from the ambient surroundings or the human body itself. It is possible to use thermoelectric generators, or TEGs, to harvest energy from human body heat. Thus, energy harvesting provides a solution to the limitations of batteries for wearable devices. TEGs provide a continuous, scalable, solid-state energy source ideal for wearable and wireless electronics and sensors. Unfortunately, current TEG technology produces low power (< 1 mW) at a very low voltage (20-90 mV) and require the load to be matched to the TEG internal resistance for maximum power transfer. This thesis research proposes a power management integrated circuit (PMIC) that steps up ultralow voltages generated by TEGs to a regulated 3 V, while maximizing power transfer.

The proposed boost converter aims to harvest energy from body heat as efficiently and flexibly as possible by providing a regulated 3 V output that can be used by a variable load, such as a microprocessor or other electronics load. A comparator-based burst mode operation affords the converter a high conversion ratio at high efficiency, while fractional open circuit voltage maximum power point tracking ensures that the controller can be used at the maximum power point with a variety of TEGs and TEG setups.

The controller was sent out for fabrication in February 2016. Since these fabricated chips will not be completed and delivered until May 2016, functionality has only been verified through simulation. Simulation results are promising and indicate that the peak overall efficiency is 81% and peak low voltage, low power efficiency is 73%. These results demonstrate the the proposed converter can achieve overall efficiencies comparable to current literature and low power efficiencies better than similar wide range converters in literature.

Acknowledgments

First and foremost, I want to thank my principle advisor, Dr. Dong S. Ha, who guided me throughout my thesis work with his advice, experience, and knowledge. I would also like to thank Dr. Qiang Li for lending his help and expertise throughout my thesis.

I would like to thank the Electrical Engineering department at Virginia Tech for not only providing me this opportunity, but also providing funding through graduate assistant opportunities throughout my time here.

I would like to thank Texas Instruments for providing our lab access to their 0.25 μm CMOS technology and space on their lbc7 shuttle runs. I would particularly like to thank Dr. Na Kong for her invaluable support and time throughout the tapeout process with TI.

I would like to thank my past and present colleagues within the MICS lab: Brian Cassidy, Taylor Yeago, Thomas O'Connor, Zhao Gao, Liao Wu, Yudong Xu, Nan Chen, Ji Hoon Hyun, Yu Lin, and Erick Aponte. It has been a pleasure working with you all and thank you for your advice and support.

Thank you to all my friends from Virginia Tech for your encouragement and making both my undergraduate and graduate experiences well-rounded and unforgettable.

Special thanks goes to my brother, Connor Brogan, who has been a constant source of help and encouragement throughout my thesis work. I'm not sure how I could have made it here without your support.

Finally, I am extremely grateful to my parents, Mary Anne Quinlan and Jim Brogan, and my brother, Brendan Brogan, for your unconditional support and patience.

Contents

1	Introduction	1
1.1	Motivation	1
1.2	Design Challenges and Shortcomings of Thermoelectric Energy Harvesting from Body Heat	2
1.3	Contributions of Proposed Research	3
1.4	Organization of Thesis	3
2	Preliminaries	5
2.1	Introduction to Thermoelectric Energy Harvesting	5
2.1.1	Introduction to Thermoelectric Generators	5
2.1.2	Challenges of Thermoelectric Energy Harvesting from Body Heat	6
2.1.3	Survey of Commercially Available TEGs	8
2.2	PMC Design Approaches for Thermoelectric Energy Harvesting from Body Heat	8
2.2.1	Defining Efficiency for Energy Harvesting Systems	8
2.2.2	Maximum Power Point Tracking with TEGs: the Fractional Open Circuit Voltage Method	9
2.2.3	Cold Startup Techniques	10
2.2.4	Power Management: Boost Converter	11
2.3	Applicable Boost Converter Control Techniques	12
2.3.1	One Stage vs. Two Stage Approaches	12
2.3.2	Im’s Approach to a One Stage Boost Converter	13

2.3.3	Ahmed’s Approach to a One Stage Boost Converter	14
3	Proposed Converter	17
3.1	Specifications and Design Goals	17
3.2	Operation Details	18
3.2.1	Block Diagram	18
3.2.2	Burst Control Details	19
3.2.3	Input Voltage Control Details	20
3.3	Design of the Power Stage	21
3.3.1	Selection of Inductor, Input Capacitor, and Output Capacitor	21
3.3.2	Diode Selection	24
3.3.3	Power MOSFET and Gate Driver Design	24
3.4	Design of the Control Blocks	27
3.4.1	Comparator Design	27
3.4.2	Open Circuit Voltage Sampler	29
3.5	Layout	30
4	Simulation Results	31
4.1	Post Layout Simulation Results	31
4.1.1	Proposed Converter Control Operation Verification	32
4.1.2	Overall Efficiency	33
4.1.3	Converter Efficiency	35
4.1.4	MPPT Efficiency	36
4.1.5	Sampling Accuracy of OCV Sampler Block	37
4.2	Comparison with Other Works	38
5	Conclusion	39
5.1	Key Contributions	39
5.2	Future Improvements	40

Appendix A	41
References	43

List of Figures

1.1	Block diagram of basic energy harvesting system, illustrating required feedback loops.	2
2.1	Typical TEG with electric equivalent circuit from [4], ©2011 IEEE.	6
2.2	Graph of load power vs. resistance ratio of load to source $\left(\frac{R_L}{R_{TEG}}\right)$, with marked location of MPP.	7
2.3	Block diagram of thermoelectric energy harvesting system.	8
2.4	Illustration of steps in FOCV MPPT algorithm.	10
2.5	Boost converter with current sink load.	11
2.6	Block diagrams of different TEG energy harvesting system configurations. . .	13
2.7	Waveforms of Im's proposed comparator based MPPT boost converter control from [5], ©2012 IEEE.	14
2.8	Block and timing diagrams of Ahmed's burst mode control in [8].	15
3.1	Diagram of proposed converter illustrating key control blocks.	18
3.2	Schematic of proposed control scheme, with key signals highlighted.	19
3.3	Burst waveforms, with active and inactive periods marked.	19
3.4	Waveforms illustrating hysteretic input voltage control to achieve FOCV MPPT. .	20
3.5	Designation of DT_s , D_1T_s , and D_2T_s	21
3.6	Push-pull gate driver schematic.	26
3.7	V_{out} comparator schematic and function.	27
3.8	V_{in} comparator schematic and function.	28
3.9	Schematic of OCV sampler.	29

3.10	Timing diagram of OCV sampler control signals and delayed D control signal.	29
3.11	Final layout of PMIC, with relevant blocks highlighted.	30
4.1	Testbench used for post-layout simulations.	31
4.2	Converter waveforms at $V_{TEG} = 50, 500$ mV and $R_{TEG} = 8 \Omega$ of V_o (blue), I_L (purple), D (red), and V_{in} (orange).	32
4.3	Converter waveforms at $V_{TEG} = 100$ mV and $R_{TEG} = 1, 16 \Omega$ of V_o (blue), I_L (purple), D (red), and V_{in} (orange)	33
4.4	Overall efficiency vs. V_{TEG} for entire R_{TEG} range.	34
4.5	Overall efficiency vs. P_{MPP} for entire R_{TEG} range.	34
4.6	Converter efficiency for entire R_{TEG} and V_{TEG} ranges.	35
4.7	Power loss breakdown between two different TEG resistances at 100 mV.	36
4.8	Burst ePPT Efficiency for entire R_{TEG} and V_{TEG} ranges.	36
4.9	Failure of OCV sampling block at $V_{TEG} = 120$ mV and $R_{TEG} = 4 \Omega$.	37

List of Tables

- 2.1 Comparison of Commercially Available TEGs 8
- 3.1 Proposed Boost Converter Specifications and Goals 18
- 4.1 Comparison of Proposed Boost Converter with Prior Work 38

Chapter 1

Introduction

1.1 Motivation

As predicted by early science fiction, wearable electronics are becoming ubiquitous in modern society. These electronics range from fitness trackers to smart watches to ultra low power temperature and heartrate sensors and are all becoming interconnected by the Internet ofThings (IoT). It is predicted that by 2018, there will be 485 million wearable electronic devices shipped around the world [1]. However, these technologies face many obstacles, including communication bandwidth and small, efficient power management [2]. These electronics have, thus far, been powered by batteries that need to be recharged after a certain amount of wear-time and replaced at the end of their life. Thus, batteries not only inhibit lifetime, but also cost and scalability, making small sensor nodes larger than the electronics would require [3]. A solution to these problems would be an efficient, scalable, and continuous energy source, thus eliminating the need for battery recharging and replacement.

For wearable electronics, energy harvesting from motion, solar, and body heat has been proposed in the past to either charge the battery or power the devices [4, 5, 6, 7, 8, 9]. However, thermoelectric energy harvesting from body heat is the most continuous energy source available for wearable electronics: it does not depend on light level or movement, but rather merely contact with the body and the ambient temperature, both of which are inherent in wearable devices. This work focuses on creating a power management circuit (PMC) to harvest energy from body heat efficiently and create a stable voltage high enough to support various microelectronics devices.

1.2 Design Challenges and Shortcomings of Thermoelectric Energy Harvesting from Body Heat

Thermoelectric Energy Generators (TEGs) used to harvest energy from body heat provide a continuous and renewable source of energy for wearable electronics, but there are a few crucial issues that must be addressed when designing power management. First, TEGs generate a potential proportional to the temperature gradient across them. When harvesting energy from body heat, there is generally a low temperature differential (a few °C) available and thus the TEGs produce a low voltage, usually a few tens of mV. Furthermore, the power produced by the TEG is proportional to the square of the temperature difference, so TEGs used for harvesting from body heat also produce very low powers, generally less than 1 mW [4, 10, 8]. Lastly, TEGs are a nonideal energy source and, thus, the power supplied depends on load impedance. For a resistive source like TEGs, the load resistance must match the TEG's internal electrical resistance to provide maximum power. If these do not match, significantly less than maximum power is extracted, therefore harvesting energy very inefficiently.

Current research in thermoelectric energy harvesting focuses on the design of either the device side (investigating thermoelectric materials and properties, etc.) or the power management circuitry to address these challenges. Power management is particularly crucial for energy harvesting from body heat because the generated voltage is too low to be used to charge a battery or power microelectronics. Thus, PMC including either a charge pump or DC-DC switching converter is required to step up the voltage provided from TEGs.

The key challenge to developing power management techniques for stepping up these low voltages is delivering as much power to the load as possible, by both designing a low-loss step-up power converter and matching the input impedance. To dynamically match the input impedance and provide a regulated output, the power stage of the converter must be controlled by both an input and output feedback loop, as seen in Fig. 1.1.

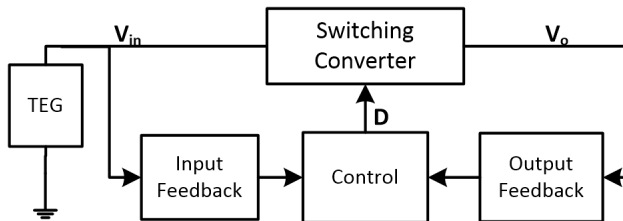


Figure 1.1: Block diagram of basic energy harvesting system, illustrating required feedback loops.

While matching a single stable input impedance with a low power boost converter can be achieved using any constant frequency control [4], matching a range of input impedances to make the converter more versatile can be more difficult as it requires an input and output

feedback loop to regulate input and output voltage. However, with traditional pulse width modulation techniques (PWM) it is not simple to control both the output and input voltage of the converter [5, 7]. Thus, much of previous research does not regulate the input voltage [8, 11] or uses two stages, which results in a lower overall efficiency [4, 6].

Lastly, since the power available is so low, the quiescent current consumed by the controller itself can have a large impact on the amount of power that is finally delivered to the load. Thus, it is crucial that the analog and digital controls of the power management integrated circuit (PMIC) be designed very carefully with regards to power consumption.

1.3 Contributions of Proposed Research

This research proposes a DC-DC converter control scheme to harvest energy from body heat for use by ultra-low power sensor nodes using a combination of burst control and fractional open circuit voltage (FOCV) maximum power point tracking (MPPT). The objective was to harvest the maximum energy available with an efficient power stage and a regulated output voltage to eliminate the need for a battery for ultralow power wearable sensors and devices. The proposed converter is fabricated in 0.25 μm CMOS technology. As the chips have not been delivered as of April 2016, only post-layout simulations are available for verification. However, simulation results have been positive. The key contributions are as follows.

First, the converter provides a regulated output voltage across a wide range of input voltages and resistances. This regulation is achieved by using a burst mode control. This voltage can be used directly by microelectronic devices.

Second, the converter uses a fractional open circuit voltage method to track the maximum power point. This, coupled with an efficient low frequency power stage, provides a high overall efficiency and maximizes power available to the load. MPPT also allows the converter to efficiently harvest from a variety of TEG arrays and setups, due to its ability to match a wide input impedance and voltage range.

Third, post-layout simulation results indicate that the quiescent current of the converter is approximately 10 μA , peak overall efficiency is 81%, and peak low power, low voltage efficiency is 73%. Thus, it presents a very efficient control scheme for wide input voltage ranges that performs as well or better than previous research in this field, as measured by converter and overall efficiency.

1.4 Organization of Thesis

The organization of the thesis is as follows. Chapter 2 provides background information on thermoelectric energy harvesting from body heat and prior research in boost converters for

this application. This background information includes TEG operation, energy harvesting challenges, and solutions to these challenges proposed by previous researchers. The details of the burst mode operation proposed in previous work is explored in-depth and the drawbacks are discussed. Chapter 3 describes the operation and design of the proposed boost converter, including details on the input and output voltage feedback mechanisms. Design of both the power stage and unique analog control components are discussed. Chapter 4 presents the post-layout simulation results verifying the converter operation and functionality and compares efficiency metrics with previous works. Lastly, Chapter 5 concludes the paper by reviewing the key contributions proposed and suggests possible directions for future research and improvement.

Chapter 2

Preliminaries

This chapter provides background information on previous research on thermoelectric energy harvesting and the state of current research activities on boost converters for energy harvesting applications. Section 2.1 provides background on how energy is harvested via thermoelectric generators (TEGs) from body heat and the challenges thereof. The following section, Section 2.2, details solutions to these challenges, such as the use of boost converters, cold startup techniques, and the necessity of Maximum Power Point Tracking (MPPT), as employed by the fractional open circuit voltage technique. Lastly, Section 2.3 discusses specific control strategies of boost converters relevant to this work.

2.1 Introduction to Thermoelectric Energy Harvesting

This section provides a brief introduction to thermoelectric energy generation and the challenges of harvesting energy from body heat with currently available TEGs.

2.1.1 Introduction to Thermoelectric Generators

A thermoelectric generator is a number of thermopiles connected in series or parallel. A thermopile, also called a thermocouple, pellet, or thermoelectric leg, is composed of an n-type material in series with a p-type material. When a temperature differential is applied to the thermopile, heat flows from the hotter to cooler side providing energy that allows free electrons and holes to move. Thus, an electric potential forms across the thermopile and, if a load is applied, current flows and power is generated [4]. This is called the Seebeck effect. When these thermopiles are connected in series, as shown in Fig. 2.1, a higher output voltage results. Similarly, in parallel, a higher output current results.

Since a TEG is several thermopiles arranged in parallel and/or series generating a single

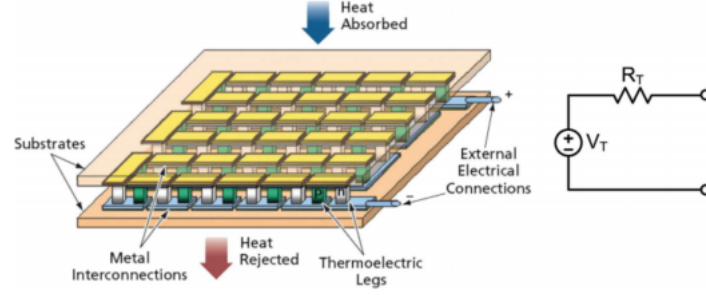


Figure 2.1: Typical TEG with electric equivalent circuit from [4], ©2011 IEEE.

potential, it can be modeled as a voltage source with an internal resistance based on the electrical resistance and connection of the thermopiles, as shown in Fig. 2.1. Depending on the series or parallel combination of the thermopiles, and the number and material of thermopiles, this resistance can range from less than 1Ω to several hundred. Furthermore, this resistance may vary with temperature, by about 10% per 10°C [12, 13].

The Seebeck coefficient, S , is used to relate the voltage generated across a given thermopile to the temperature difference across it, T . In other words, $V_T = S \cdot T$. S varies with device material and design; but given S and the number of series thermopiles in a device, N , the voltage generated by a TEG can be estimated as follows [4]:

$$V_{TEG} = N \cdot S \cdot T \quad (2.1)$$

To compare thermoelectric devices to one another, the thermoelectric figure of merit ZT is used, where T is still the temperature differential across the device. ZT is proportional to the ratio of electrical and thermal conductivities (σ and κ , respectively) such that $ZT = S^2 T \frac{\sigma}{\kappa}$. This figure of merit can be used to estimate the maximum power available using the following equation, where R_t is the thermal resistance at maximum power [10]:

$$P_{TEG,max} = \frac{ZT^2}{4R_t} \quad (2.2)$$

2.1.2 Challenges of Thermoelectric Energy Harvesting from Body Heat

While the human body is a very efficient machine, there are still large energy losses—almost entirely in the form of body heat. However, it has been shown that the temperature difference seen by a TEG against human skin and the ambient temperature depends on a number of factors, including where the TEG is located on the body and the skin's thermal resistance. Generally, the gradient is very small, in the realm of 1-3 $^\circ\text{C}$ [10].

As can be seen in Eqn. 2.1, the lower the temperature difference across a device, the lower the output voltage. Most TEGs used for energy harvesting from body heat are composed

of the thermoelectric material bismuth telluride, as this material offers higher thermal to electrical energy conversion efficiency at room temperature than most other thermoelectric materials. Generally, bismuth telluride devices with several series thermopiles can still only generate 25-30 mV/°C [4, 14]. Thus, using TEGs to harvest energy from body heat produces voltages too low to be used by standard electronics, such as microprocessors and sensors.

Using Eqn. 2.2, it can be seen that the lower the temperature differential, the exponentially less power available. Less power available means that the efficiency of the power management circuit is critical to harvest enough energy to be useful. Most commercially available TEGs, as covered in the next section, output considerably less than 1 mW to the load.

Lastly, as can be seen in the Fig. 2.1, TEGs are a nonideal energy source and, thus, the power supplied to a load depends on the load impedance. As the maximum power transfer theorem states, the load resistance must match the source resistance in order to provide maximum power. This is called the Maximum Power Point (MPP). Thus, to harvest maximum power the load resistance must equal R_{TEG} . This relationship is illustrated by the graph in Fig. 2.2, where it can be seen that close to maximum power ($> 95\%$) is harvested if the load resistance is above 70% and below 150% of the TEG resistance. Smaller load resistors deliver much less power and significantly higher load resistors also deliver much less than maximum power, thus harvesting energy very inefficiently. The maximum power the TEG can deliver to the load at the MPP is given by Eqn. 2.3.

$$P_{MPP} = \frac{V_{TEG}}{4R_{TEG}} \quad (2.3)$$

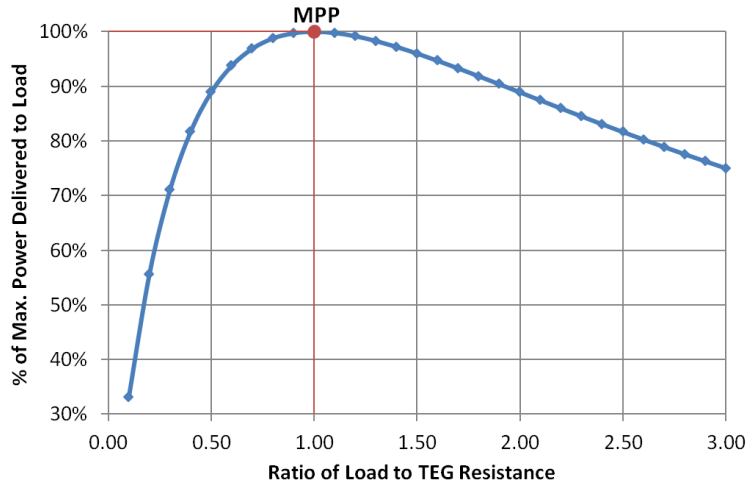


Figure 2.2: Graph of load power vs. resistance ratio of load to source $\left(\frac{R_L}{R_{TEG}}\right)$, with marked location of MPP.

2.1.3 Survey of Commercially Available TEGs

A survey of commercially available and soon to be available micro thermoelectric generators was conducted. The results of this survey is displayed in Table 2.1. It can be seen that at low temperature differences even the best performing TEGs produce less than 100 mV. It should also be noted that a variety of sizes and input resistances are currently available.

Table 2.1: Comparison of Commercially Available TEGs

Company	Size Dimensions [mm]	R_{TEG} [Ω]	V_{TEG} [mV] at $\Delta T = 2^\circ\text{C}$	P_{TEG} [μW] at $\Delta T = 2^\circ\text{C}$
Nextreme [15]	2.09 x 3.05	11	25	4.5
Micropelt [13]	3.3 x 2.45	210	46	5.04
TEC [16]	13.75 x 19.00	4.5	30	100
Phononic [17]	13.75 x 19.00	1.9	35	160
RMT, LTD [18]	16.00 x 16.00	3.13	100	1500
RMT, LTD [14]	18.00 x 18.00	1.65	90	2400

2.2 PMC Design Approaches for Thermoelectric Energy Harvesting from Body Heat

This section details previous research that has dealt with the challenges of thermoelectric energy harvesting from body heat, beginning with efficiency definitions. Then, the concept and application of Maximum Power Point Tracking is described. Next, techniques to step up the ultra-low TEG voltage at startup and during steady state are discussed.

2.2.1 Defining Efficiency for Energy Harvesting Systems

When discussing efficiency with an energy harvesting system, it may refer to several different things [19]. First, as can be seen in Fig. 2.3, an energy harvesting system is generally very simple: the transducer (TEG) is connected to some power conditioning circuit (boost converter) which then supplies the load (battery or electronics).

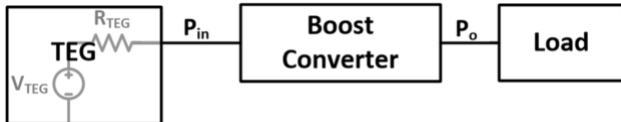


Figure 2.3: Block diagram of thermoelectric energy harvesting system.

The three definitions of efficiency that are relevant to this paper are converter efficiency, MPPT efficiency, and overall (also called end-to-end) efficiency. The converter efficiency is the efficiency for the power converter, generally a boost converter, and is given by Eqn. 2.4.

$$\eta_{converter} = \frac{P_o}{P_{in}} \quad (2.4)$$

The MPPT efficiency (Eqn. 2.5) evaluates how close to the MPP the system is at by dividing the power provided by the TEG to the converter by the maximum power available at the MPP, as given in Eqn. 2.3.

$$\eta_{MPPT} = \frac{P_{in}}{P_{MPP}} \quad (2.5)$$

The overall efficiency is the fraction of the maximum power delivered to the load, as can be seen in Eqn. 2.6. To truly compare how well a power management circuit works for energy harvesting, overall efficiency should be used [19].

$$\eta_{overall} = \frac{P_o}{P_{MPP}} \quad (2.6)$$

2.2.2 Maximum Power Point Tracking with TEGs: the Fractional Open Circuit Voltage Method

As described in Section 2.1.2, energy should be harvested at the MPP of the TEG. While the input resistance of a given TEG is relatively stable over the small temperature variations that would be seen in body heat energy harvesting applications, designing a power management circuit to only work with one input resistance is short-sighted. As can be seen in Table 2.1, the input resistance can vary significantly based on size and design. Further, resistances may vary from batch to batch depending on manufacturing variability. To account for this variability and increase the versatility of a power management circuit, Maximum Power Point Tracking (MPPT) should be employed.

There are many types of MPPT developed for different types of inputs (photovoltaic, piezoelectric, etc.) and applications, but one of the simplest is the Fractional Open Circuit Voltage Method (FOCV) [20]. This method works well for resistive sources and can ideally achieve 100% matching efficiency, with very low power dissipation. Since directly measuring input and a variable source resistance is often not feasible, this method achieves matching by maintaining the load voltage to some fraction of the source voltage.

For TEGs, the voltage at the load is as follows (where V_{TEG} is the open circuit TEG voltage):

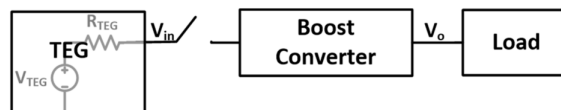
$$V_L = V_{TEG} \frac{R_L}{R_{TEG} + R_L} \quad (2.7)$$

For resistive sources like TEGs, the MPP occurs when $R_L = R_{TEG}$. Thus, the equation for load voltage can be simplified very simply:

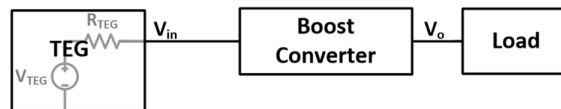
$$V_L = V_{TEG} \frac{R_{TEG}}{R_{TEG} + R_{TEG}} = 0.5V_{TEG} \quad (2.8)$$

Thus, the fractional open circuit voltage technique can be used to match the TEG very accurately if the load voltage is regulated to half the TEG voltage.

This achieved with two simple steps using FOCV MPPT. First, the source is disconnected from the PMC (see Fig. 2.4a). Now V_{in} is equal to V_{TEG} , or the “open circuit voltage.” This open circuit voltage is sampled and held to be used later. After the open circuit voltage is sampled, the PMC is reconnected, as in Fig. 2.4b. Now the PMC can continue delivering energy to the load. During this time period, the PMC is controlled such that V_{in} is now kept to some fraction of that sampled open circuit voltage; hence the name fractional open circuit voltage method. The open circuit voltage is periodically measured, such that the PMC can track any changes in the input.



(a) Step 1 of FOCV MPPT, illustrating disconnection of input.



(b) Step 2 of FOCV MPPT, illustrating reconnection of input.

Figure 2.4: Illustration of steps in FOCV MPPT algorithm.

2.2.3 Cold Startup Techniques

“Cold Startup” refers to starting up an analog or digital PMC with no external V_{cc} or precharged output voltage, as is this case in most energy harvesting applications. There is no consensus in the literature on what is the best method to cold startup from subthreshold voltages, such as those available from TEGs. Ramadass, in [4], proposes a mechanically assisted start up circuit that charges V_{cc} to the necessary voltage for the analog converter controller via a motion activated switch and boost converter. This method was able to achieve cold start from voltages as low as 35 mV, but does require an external switch and motion to activate the switch.

In contrast, Im proposes a transformer reuse circuit in [5]. The proposed circuit uses a boost converter where the inductance of the boost is the magnetizing inductance of a transformer. Noise is stepped up through a transformer to trigger a native MOSFET with a zero threshold voltage. This switch triggering connects and disconnects the input source with the transformer, which steps up the voltage and connects it to a resonant tank. The resonant tank slowly gains energy, and thus voltage amplitude, until the voltage is high enough for the converter controller to kick in [5]. While this technique is able to achieve startup from 40 mV, it has a few drawbacks: namely, it requires a transformer, which is larger than a single inductor and can contribute additional winding loss to the power stage, and a zero threshold voltage MOSFET, which is not always readily available in all CMOS technologies.

Other techniques achieve cold-startup by using an antenna attuned to ambient low power RF signals and a rectifier to charge the output of the boost converter [21, 6]. This technique has achieved success in previous research starting up boost converters with V_{in} as low as 30 mV, assuming an ambient -10 dBm RF signal is available, such as Wi-Fi.

2.2.4 Power Management: Boost Converter

As discussed previously, there are many ways that a circuit can be started from extremely low voltage; however, these are not the most power efficient techniques of stepping up DC voltages. The most power efficient technique to step a low DC voltage to a higher DC voltage is to use a DC-DC switching converter. While the boost and buck-boost topologies both work for this case, the boost is more convenient as its output is the same polarity as the input. The power stage of a boost converter is shown in Fig. 2.5. To use a boost converter for ultralow voltage, it is of course assumed that a supply voltage for the controller is available either via external battery or a low voltage startup technique, as discussed in the previous section.

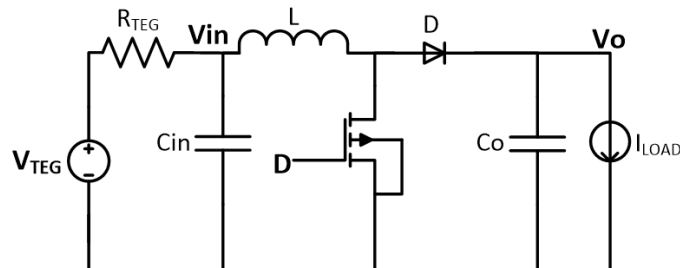


Figure 2.5: Boost converter with current sink load.

A boost converter works either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), as defined by the current through the inductor. DCM is when the inductor current falls and remains at 0 for a period of each switching cycle, whereas in CCM the inductor current is never allowed to remain at 0. The conversion ratio $\left(M = \frac{V_{out}}{V_{in}}\right)$ for CCM is independent of load and equal to $\frac{1}{1-D}$, where D is the duty cycle of the MOSFET switch. At light loads, DCM provides a higher conversion ratio (see Eqn. 2.9) and efficiency due to the period where neither the MOSFET or diode is conducting current [22].

$$M = \frac{1 + \sqrt{1 + \frac{4D^2 R_L}{2L f_{sw}}}}{2} \quad (2.9)$$

However, the efficiency of a boost converter falls as conversion ratio increases due to the increased duty cycle required, as can be seen in Eqn. 2.9. Since TEGs produce such low voltage, this can pose a challenge to efficient power management. The design solutions to these challenges, as proposed in recent literature, are detailed in the next section.

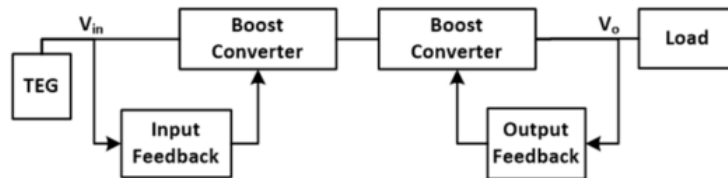
2.3 Applicable Boost Converter Control Techniques

This section details design approaches for using boost converters for thermoelectric energy harvesting from body heat. The first section details the advantages and disadvantages of one stage and two stage converters. The following two sections detail two successful one stage converters.

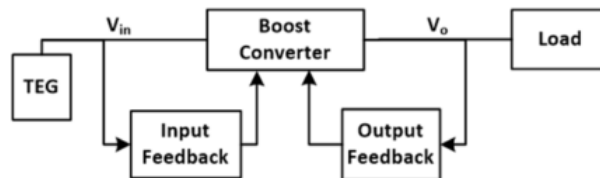
2.3.1 One Stage vs. Two Stage Approaches

There have been several techniques presented in previous research to design efficient boost converters to harvest energy from thermoelectric generators. As discussed previously, achieving high conversion ratio requires higher duty cycle, which leads to decreased efficiency. To decrease the conversion ratio required by each converter, some have proposed 2-stage converter solutions [4, 6]. As can be seen in Fig. 2.6a, the first stage controls the input voltage for MPPT and the second stage controls the output voltage. [4] achieves a peak overall efficiency of (60%). [6] has achieved a higher overall efficiency of 75%; however, this power converter is very efficient due to a low output voltage (0.5 V) and, thus, low conversion ratio, and also a limited operable power range. A two-stage solution requires high individual converter efficiency to achieve a high system efficiency.

As converter efficiency has improved, others have proposed high conversion ratio single stage converters. However, it is difficult to achieve high efficiencies while incorporating efficient MPPT (input feedback) and output voltage regulation in this ultra low power range (see Fig. 2.6b). Thus, some have opted to eschew MPPT to produce very efficient boost converters, reasoning that the losses from not harvesting at the maximum power point are made up for by losing less power in the power stage [11, 8]. These efforts have reported high peak converter efficiencies of 75% and 82%, respectively. However, the overall efficiency is significantly lower: overall efficiency is only 52% for [11], as estimated by [4]. [5] incorporates both input and output feedback loops into a single stage control and achieves a peak overall efficiency of 61%: the details of this design will be discussed further in the next section.



(a) Block diagram of two stage converter design, illustrating separate feedback loops.



(b) Block diagram of a one stage converter design with two feedback loops.

Figure 2.6: Block diagrams of different TEG energy harvesting system configurations.

2.3.2 Im's Approach to a One Stage Boost Converter

As previously mentioned, Im et.al. in [5] report a peak overall efficiency of 61% with a single stage converter that regulates both the input and output and could boost 40-300 mV up to 2 V. This section will detail how this was achieved and any drawbacks of the scheme.

Operation Details

Input and output voltage regulation is achieved in [5] by using a dual comparator scheme: the duty cycle for the MOSFET is the anded signal of an output voltage comparator and an input voltage comparator. The output voltage comparator goes high whenever V_o falls below some V_{ref} . The input voltage comparator applies FOCV MPPT by comparing V_{in} to $\frac{V_{TEG}}{2}$. When V_{in} rises above $\frac{V_{TEG}}{2}$, the duty cycle turns on until V_{in} falls below $\frac{V_{TEG}}{2}$, as can be seen in Fig. 2.7.

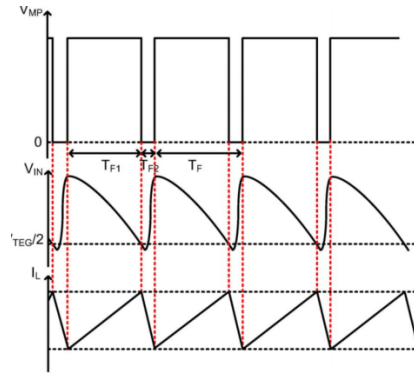


Figure 2.7: Waveforms of Im's proposed comparator based MPPT boost converter control from [5], ©2012 IEEE.

Drawbacks

The drawback of this design is that, as can be seen in Fig. 2.7, the converter may be working in CCM due to a large duty cycle, which leads to decreased efficiency at low powers. The reason the duty cycle may so high is because the frequency of switching is due to the RC delay time and inductance of the feedback loop: the off time TF_2 is only due to the RC delay of the comparator and is thus small. The amount the input voltage raises above the maximum power point is thus uncontrolled. Further, the converter operation is interrupted periodically to sample and hold the MPP reference voltage, $\frac{V_{TEG}}{2}$.

2.3.3 Ahmed's Approach to a One Stage Boost Converter

The approach used by K.Z. Ahmed in [8] was notable for its ability to regulate the output voltage while maintaining high efficiency and conversion ratio. It was able to boost input voltage as low as 12 mV to output voltages high as 3.3 V, with a peak efficiency of 82%. Ahmed's proposed control also provides a regulated output, that is efficient for a wide load range due to burst mode control.

Operation Details

Ahmed's approach uses a burst mode operation to maintain high converter efficiency, even if the load uses less than the maximum power available. The EN signal Fig. 2.8b is the output of a hysteretic comparator that compares the output voltage (V_{out}) with some reference voltage (V-REF). The EN signal goes high when V_{out} falls to V-REF. When EN goes high, a 98% duty cycle, 86 kHz oscillator is enabled. This oscillator provides the control signal to the power stage, thus controlling the inductor current (I-IND). The oscillator's high duty cycle allows both inductor current and output voltage to rise. When the output voltage rises above the hysteretic window of the comparator (i.e. V-REG+V-HYS), EN goes low. Thus, the oscillator turns off, the inductor dumps its energy into the load, and the power stage turns off. The output voltage then falls, until it reaches V-REF and the cycle starts again.

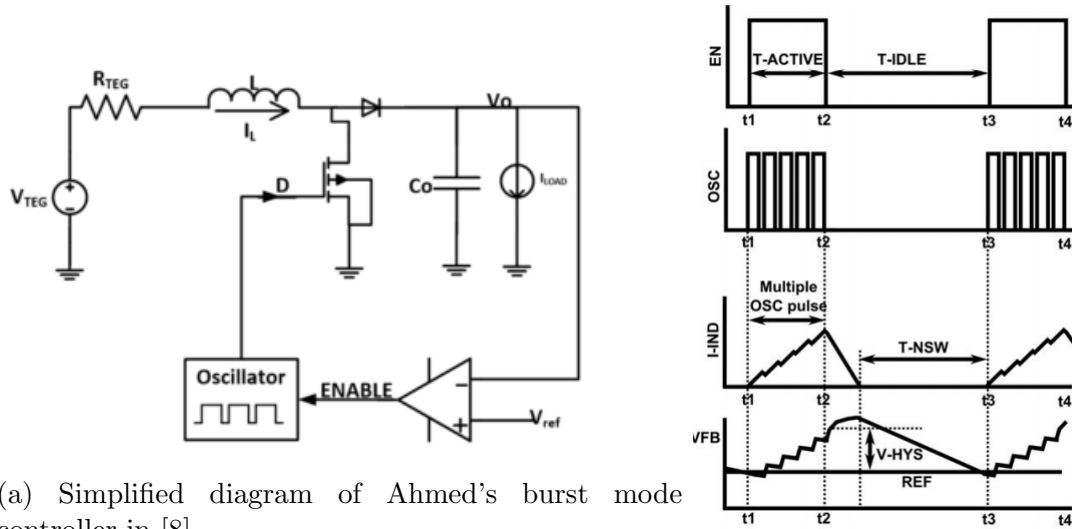


Figure 2.8: Block and timing diagrams of Ahmed's burst mode control in [8].

The burst operation regulates the output voltage to approximately V-REF, with a ripple to V-REF+V-HYS. The high converter efficiency is achievable by careful design of the controller and the large dead times (T-NSW in Fig. 2.8b) afforded by burst mode. The dead times increase for smaller output loads, thus increasing light load efficiency for variable loads. Further this dead time increases overall converter efficiency, while still maintaining a 50 mV ripple (which is small compared to high output voltages of 2-3 V).

Drawbacks

Ahmed's proposed controller relies entirely on output voltage feedback and a constant duty cycle and constant frequency oscillator. In other words, there is no MPPT. Ahmed tested his design with a low resistance TEG [15], but did not measure the maximum power and, thus, only reported converter efficiency. Using his reported efficiencies at different temperatures/voltages in his paper [8] and the datasheet of the TEG [15], it can be estimated that even when the converter efficiency is close to 70% at low voltage, the overall efficiency is approximately 40%. As reported earlier, two stage approaches or other lower converter-efficiency one stage approaches have been able to achieve much higher overall efficiency. It should also be noted that when the converter has a large dead time (i.e. load is small), much less than the maximum power is harvested. This may be acceptable in some applications where there is no need to harvest maximum energy, if the load requirement is much smaller than the maximum power producible by the TEG.

Chapter 3

Proposed Converter

The proposed power management integrated circuit (PMIC) for energy harvesting from human body heat should satisfy several requirements imposed by the characteristics of the energy harvester. It must boost the low input voltage to a voltage usable by microelectronics. This is achieved by adopting a boost converter topology. It also must be able to match the internal resistance of the thermoelectric generator (TEG). To match the input while regulating output voltage, fractional open circuit voltage MPPT and burst mode operation control techniques are adopted. This chapter describes the specifications, design goals, operation, and design of the proposed converter. Design of the converter is split into that of the power stage in Section 3.3 and the analog and digital control blocks in Section 3.4. Lastly, the layout of the chip is discussed.

3.1 Specifications and Design Goals

Based on the survey of TEGs (see Table 2.1), requirements for the input voltage, input resistance, and thus, maximum load power were set. The input resistance and input voltage requirements are high to accommodate several low resistance TEGs in series, so that the PMC can work with different energy harvesting system designs. The efficiency goals are based on the literature survey referenced in Section 2.3. Note that there are 2 efficiency goals. Since efficiency is expected to be higher at high input voltage/high load, a low-power, low-voltage efficiency goal is established as well. This will ensure that the design is competitive with narrow-range, low power converters. An output voltage of 3 V is chosen, as this is a usable voltage by ultra-low power MCU's [23, 24] and could easily be adjusted up 30% to 3.3 V for lithium ion battery applications. These design goals and specifications are summarized in Table 3.1.

Table 3.1: Proposed Boost Converter Specifications and Goals

Specification/Goal	Requirement
Input Voltage Range	70 - 500 mV
Input Resistance Range (for testing)	1 - 16 Ω
Output Voltage	3 V
Output Voltage Ripple	<3%
Maximum Load Power	10 mW
Maximum Overall Efficiency	>75%
Maximum Overall Efficiency for $V_{in} < 200$ mV and $P_{in} < 0.5$ mW	>65%

3.2 Operation Details

This section describes the proposed switching converter and its operation. The goal is to achieve high converter efficiency across a range of loads while boosting the input voltage and matching the input resistance. The proposed converter regulates both input and output voltage by using a burst mode operation and an input voltage control scheme. The first subsection looks at the overall control at a higher block diagram level. The second and third subsections detail how the output voltage and input voltage are controlled.

3.2.1 Block Diagram

The proposed converter uses a burst mode, as in Ahmed's work, to both control the output voltage, provide for a higher conversion ratio, and reduce light load efficiency for a variable load [8]. The converter is controlled during the burst period by a feedback loop that maintains the input voltage at the maximum power point. The general concept is illustrated below as a simplified block diagram in Fig. 3.1.

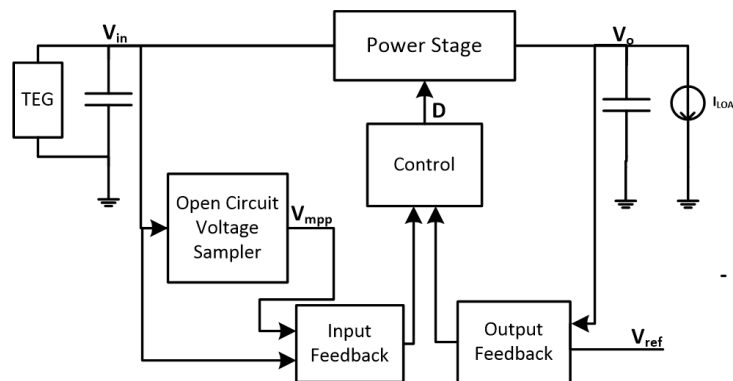


Figure 3.1: Diagram of proposed converter illustrating key control blocks.

Feedback from the output regulates when the converter enters an active (or burst) period such that the output voltage is maintained within a certain ripple of V_{ref} . The Open Circuit Voltage Sampler (OCV Sampler) block produces the input reference, V_{mpp} , by sampling the input voltage before the active period. During the active period, the on-time of the MOSFET in the power stage is modulated to regulate the input voltage within a ripple of V_{mpp} . The basic schematic of the controller can be seen in Fig. 3.2, with relevant signals color-coded to match their counterparts in future figures (Fig. 3.3 - Fig. 3.5).

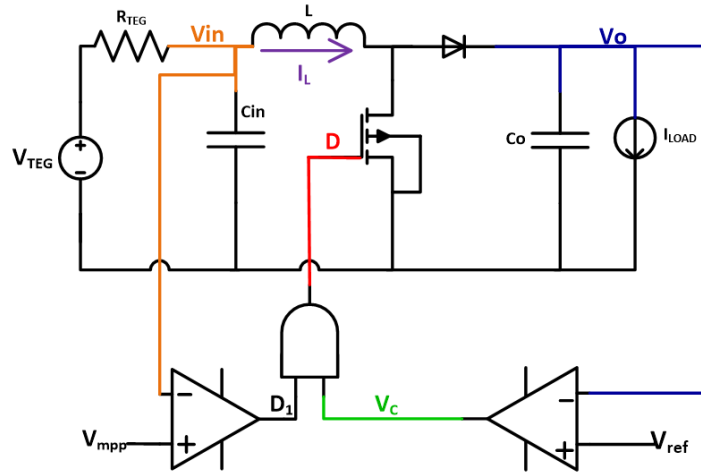


Figure 3.2: Schematic of proposed control scheme, with key signals highlighted.

3.2.2 Burst Control Details

As can be seen in the schematic in Fig. 3.2 and the output waveforms in Fig. 3.3, when V_{out} falls to V_{ref} , V_c goes high. This signals the start of an “active” period, when the converter is actively switching and the output voltage begins to rise. Due to hysteresis in the comparator, the signal V_c remains high until $V_{out} > V_{ref} + V_{hysteresis}$. Thus, the output voltage ripple is approximately equal to the hysteresis of the output comparator (designed to be 50 mV). The length of the active period depends on the control of the boost converter and the length of the inactive period depends entirely on load and the output capacitor size.

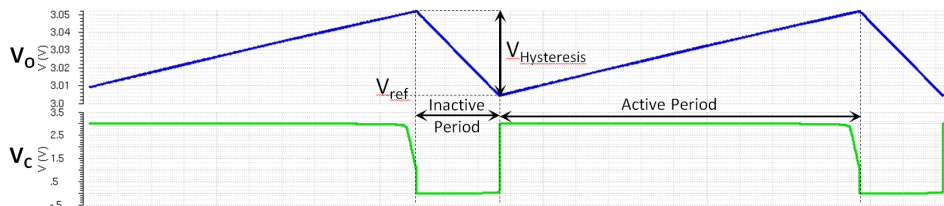


Figure 3.3: Burst waveforms, with active and inactive periods marked.

3.2.3 Input Voltage Control Details

The control of the power stage occurs during the active period; however, it uses information gained during the inactive period by sampling V_{in} to create V_{mpp} . Assuming the input capacitor has had time to fully charge during the inactive period, the input voltage to the converter, V_{in} , is equal to the open circuit voltage of the TEG at the start of the active period/end of the inactive period. It is at this time that the input voltage is used by the OCV block to sample and hold the maximum power point (approximately 50% the open circuit voltage, V_{TEG}). After this occurs, the active period begins.

During the active period, V_{in} is greater than V_{mpp} , so thus D_1 goes high (refer to Fig. 3.2). The power stage switch is controlled by $D = D_1 \cdot V_C$, so when D_1 goes high, the switch closes, and energy is transferred to the inductor (i.e. inductor current I_L begins to rise). Thus, the input voltage will begin to fall as the input is loaded. When V_{in} falls to V_{mpp} , the signal D_1 goes low and the switch opens. The inductor current I_L falls as the inductor supplies energy to the load and output capacitor and the output voltage increases. Due to the diode limiting current direction, the inductor current cannot fall below zero. Thus, when the inductor discharges all of its energy, the output capacitor must supply the load and the TEG begins to charge the input capacitor. Due to hysteresis in the input voltage comparator, D_1 remains low until V_{in} crosses the $V_{mpp} + V_{hysteresis}$ threshold. Then the cycle repeats, as can be seen in Fig. 3.4. It can be understood that with this control scheme, the input voltage is regulated to $V_{mpp} < V_{in} < V_{mpp} + V_{hysteresis}$. The proposed converter was designed such that this ripple was, at maximum, 40 mV.

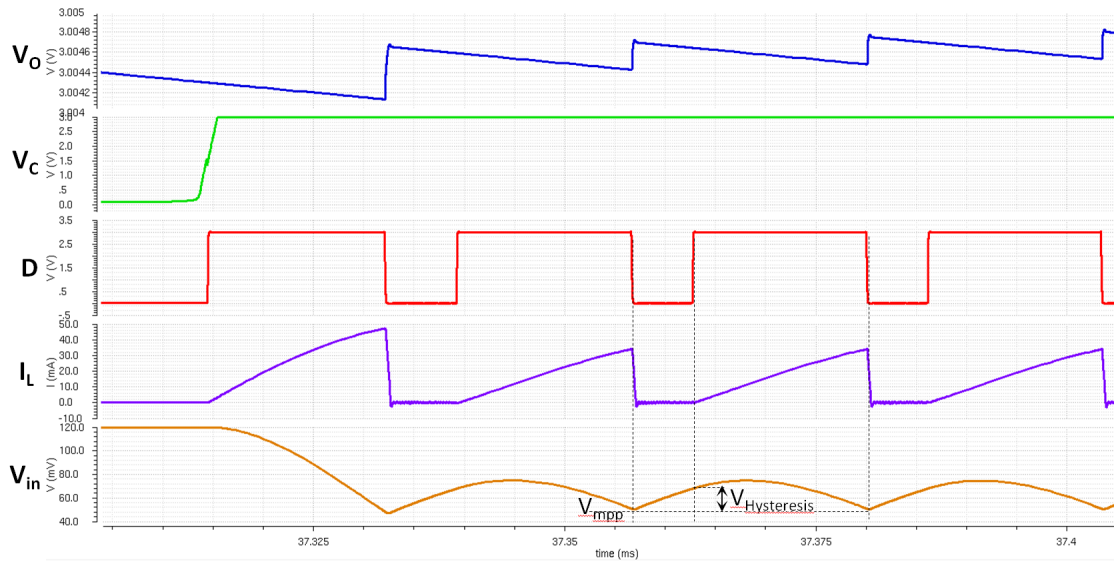


Figure 3.4: Waveforms illustrating hysteretic input voltage control to achieve FOCV MPPT.

3.3 Design of the Power Stage

Since the design of the converter relies on the relationship between the input voltage ripple and inductor current, the power stage components (input capacitor, inductor, output capacitor, diode, and Power MOSFET) must be selected very carefully for the converter to operate efficiently and across the required range of input resistances.

3.3.1 Selection of Inductor, Input Capacitor, and Output Capacitor

Importance of the lengths of DT_s , D_1T_s , and D_2T_s

For the proposed converter to work, the output voltage must be increasing during the active period. The output voltage slope is determined by the currents charging or discharging the output capacitor (inductor current and load current, respectively), the output capacitor size, and the length of the discharge and charge times. To design for this, a rough piecewise model was created to determine the discharge and charge times. First, the converter operation during the active period was split into three different modes: DT_s where the MOSFET is conducting and inductor current is rising; D_1T_s where inductor current is falling and the diode is conducting; and D_2T_s where the inductor current is zero. These three modes are illustrated in Fig. 3.5.

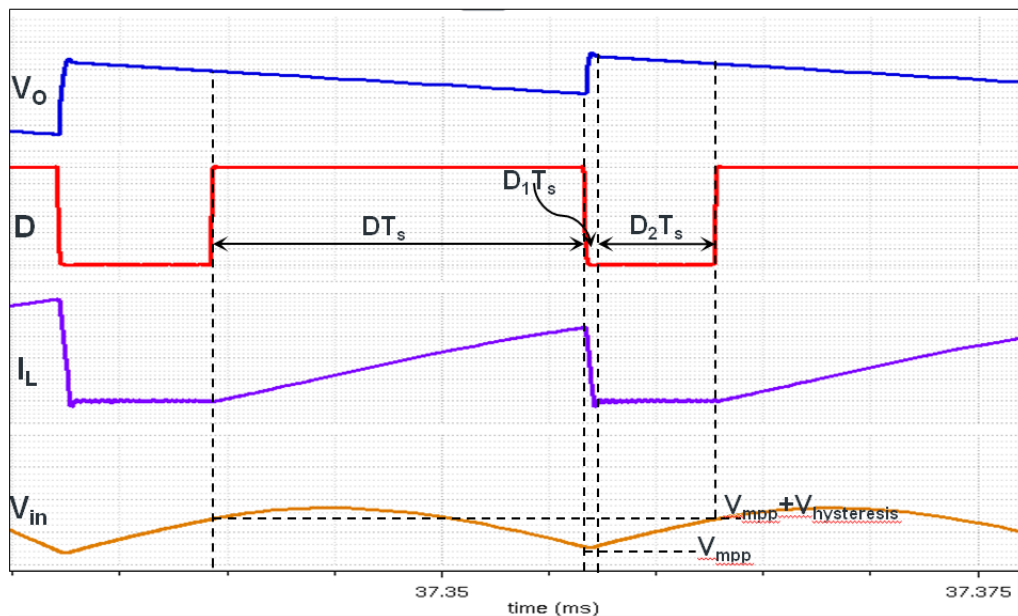


Figure 3.5: Designation of DT_s , D_1T_s , and D_2T_s .

As can be seen in Fig. 3.5, the output capacitor is only charged during D_1T_s , when the diode is conducting, and discharged during DT_s and D_2T_s . Thus, the output voltage ripple can be described as follows:

$$\text{Increasing } \Delta V_{out} = \frac{I_L}{C_{out}} D_1 T_s \quad (3.1a)$$

$$\text{Decreasing } \Delta V_{out} = \frac{I_o}{C_{out}} (DT_s + D_2 T_s) \quad (3.1b)$$

As said previously V_{out} must increase overall, meaning $I_L D_1 T_s > I_o (DT_s + D_2 T_s)$. Thus, the selection of the input capacitor and inductor must be made such that this is well satisfied. It should be obvious that the critical condition here is at heavier loads (which occur at small R_{TEG} or large V_{TEG}).

Derivation of calculations to estimate DT_s , D_1T_s , and D_2T_s

As explained in Section 3.2.3, DT_s starts when the input voltage is equal to the sampled $V_{mpp} + V_{hysteresis}$ and ends when the input voltage falls to V_{mpp} . During this time period, the MOSFET is shorted to ground and the inductor is charged by the TEG, forming a parallel RLC circuit between R_{TEG} , C_{in} , and L . It is assumed that $R_{TEG} \gg ESR_{C_{in}}$, the equivalent series resistance of the input capacitor (e.g. 5 m Ω). Thus, the $v_{in}(t)$ is governed by the second order differential equation:

$$v_{in}''(t) + \frac{\dot{v}_{in}}{C_{in}R_{TEG}} + \frac{v_{in}}{LC_{in}} = 0 \quad (3.2)$$

As this is a general second-order system, the solution may take one of three forms depending on whether it is an underdamped, overdamped, or critically damped system. DT_s can be found by setting the appropriate solution to equal to V_{mpp} . This can be done by using a number of methods; in this case MATLAB's `vpsolve` function was used (refer to Appendix A for source code used for solving the equations discussed in this section).

The length of D_1T_s is determined by how long it takes I_L to fall from its peak value to zero. The peak value can be found using the solution to Equation 3.2 (henceforth referred to as $v_{in,DT_s}(t)$) as follows:

$$I_{Lpk} = \frac{1}{L} \int_0^{DT_s} v_{in,DT_s}(t) dt \quad (3.3)$$

Once I_{Lpk} is calculated, D_1T_s can be found by multiplying the peak current by the slope of the current. The slope of the inductor current is $\frac{dI_L}{dt} = \frac{V_L}{L}$ where $V_L = V_o + V_D - v_{in}$ and $V_{in} = V_{mpp}$ (it is assumed that there is no change in the input voltage during the relatively short D_1T_s as supported by a less than 2% of V_{in} during simulation) and V_D is the forward

voltage drop across the diode. Thus D_1T_s can be found as follows:

$$D_1T_s = \frac{I_{Lpk}L}{V_o + V_D - V_{mpp}} \quad (3.4)$$

Similarly, during D_1T_s , the system is essentially a series RLC circuit, under the assumption that there is no change in the input voltage during D_1T_s (in simulation, this change is less than 2% of V_{in}) and $v_o(t) = V_o = 3\text{V}$ due to small output voltage ripple relative to 3 V (ripple is on the order of single mV and so is <5%). The inductor current can thus be modeled by the second order differential equation:

$$\ddot{i}_L(t) + \frac{\dot{i}_L R_{TEG}}{L} + \frac{i_L}{LC_{out}} = 0 \quad (3.5)$$

Comparatively, finding D_2T_s is very simple. During this mode, the inductor current is zero, so the output capacitor is discharging to the load and the TEG is charging the input capacitor. Again assuming no change in the input voltage during D_1T_s , then v_{in} at the beginning of this mode can be assumed to be V_{mpp} . Then the input voltage can be modeled as:

$$v_{in}(t) = (V_{TEG} - V_{mpp}) \left(1 - e^{\frac{-t}{R_{TEG}C_{in}}}\right) \quad (3.6)$$

Solving this for when $V_{in} = V_{mpp} + V_{hysteresis}$, yields:

$$D_2T_s = -R_{TEG}C_{in} \ln \left(1 - \frac{V_{mpp} + V_{hysteresis}}{V_{TEG} - V_{mpp}}\right) \quad (3.7)$$

It should be noted that while C_{in} , L , and C_{out} all have an effect on the timing of the circuit that the switching frequency ($DT_s + D_1T_s + D_2T_s$) depends mainly on R_{TEG} , C_{in} and L but not the value of C_{out} , the load, or input voltage. The reason that switching frequency depends little on the load current or C_{out} is because D_1T_s is the only time period that dependent on C_{out} and I_o and this period is significantly smaller than the two other time periods in practice because the inductor current falls much faster than it rises (there is a significantly higher potential across the inductor during discharge due to the high conversion ratio of the circuit). V_{in} does not affect significantly switching frequency because the ratio of V_{mpp} to V_{TEG} is constant.

Choosing C_{in} , L , and C_{out}

Using a MATLAB script (located in Appendix A) to estimate the results of Equation 3.1, the passive components of the power stage C_{in} , L , and C_{out} can be chosen such that the output voltage is rising over the entire burst mode. Furthermore, for best efficiency these components should be chosen such that the switching frequency over the entire resistance range is greater than 25 kHz (above the audible noise range for humans). It should also be taken into consideration that the length of deadtime between bursts is entirely decided by the size of C_{out} , so care should be taken such that this time is long enough for C_{in} to fully charge to V_{TEG} such that the open circuit voltage can be sampled. The final values used were: $L = 33 \mu\text{H}$, $C_{in} = 5 \mu\text{F}$, and $C_{out} = 2.2 \mu\text{F}$. To summarize the tradeoffs in choosing: the inductor size affects switching frequency and peak current, the input capacitor affects the burst period length by affecting the length of inactive period and how fast V_{out} rises during the active period, and the input capacitor affects the switching frequency and duty cycle.

3.3.2 Diode Selection

There is an external diode to allow current to flow to the output when the MOSFET is switched off during D_1T_s and to block current during D_2T_s . For best efficiency, a Schottky diode was chosen, so that there would be no reverse recovery switching losses. The lower the forward drop voltage, the lower the effective conversion ratio and, thus, the higher the efficiency. A lower forward voltage also means lower conduction losses ($P_{conduction,diode} = I_D V_D$), which also increases the overall converter efficiency. Thus, a BAS 40 device from Diodes, Incorporated was chosen, which can support up to 1 A of continuous current and has a forward voltage of 240 mV.

3.3.3 Power MOSFET and Gate Driver Design

MOSFET Losses

The switching elements of a power converter (i.e. MOSFET and diode) contribute to most of the losses of the system and thus must be designed very carefully. The losses of the MOSFET can be broken down into conduction, switching, gate charge, and output capacitance charge loss. These losses can be expressed as a function of both external factors and internal properties of the MOSFET. The external factors are the switching frequency f_{sw} , MOSFET drain current I_{drain} , duty cycle of the switching waveform D , and blocking voltage V_{off} .

For the proposed boost converter $I_{drain,rms} = I_o$, duty cycle is $DT_s f_{sw}$, and $V_{off} = V_o + V_D$, where V_D is the forward voltage of the external diode. The internal variables are the gate charge Q_g , output capacitance C_{oss} , and on resistance R_{dson} . From [22], the power losses can be estimated thus:

$$P_{conduction} = \frac{I_{Lpk}^2 R_{dson} D}{3} \quad (3.8a)$$

$$P_{gatecharge} = Q_G V_{gs} f_{sw} \quad (3.8b)$$

$$P_{sw} = \frac{f_{sw} V_{off} I_{Lpk} Q_{GD}}{2 I_{driver}} \quad (3.8c)$$

$$P_{outputcapacitance} = \frac{f_{sw} V_{off} C_{oss}}{2} \quad (3.8d)$$

The figure of merit (FOM) used to determine the relative performance of power MOSFETs is $FOM = Q_g R_{dson}$, where a lower figure of merit implies a better device. It should be noted that conduction losses are mainly due to the length of DT_s and peak inductor current. The other losses are all related to switching frequency and the various parasitic capacitances of the MOSFET. For instance, it can be seen that switching loss, P_{sw} is due to the switching delay when the MOSFET is not fully ON or OFF caused by the charging of the gate capacitance (represented by Q_g) by the gate driver (I_{driver}).

MOSFET Design

For this design, the MOSFET is integrated into the chip using the 7 V lateral diffused MOSFET available within TI 0.25 μm PDK LBC7. While this breakdown voltage is much higher than necessary considering the blocking voltage required is 3.24 V, it is the lowest breakdown voltage available in the PDK for lateral MOSFETs. A lateral MOSFET is chosen because it has the best possible figure of merit in the TI PDK [25]. The length and width of the MOSFET determine the gate charge, Q_g , and on resistance, R_{dson} , so the particular FOM will vary with MOSFET design. Increasing the size will result in larger capacitance, but smaller resistance and vice versa.

Since the switching frequency was purposefully kept low in the design, it is known that the conduction loss will dominate throughout the load range at low input resistance (when switching frequency is at its minimum). Using the MATLAB script, it was estimated that the switching frequency increases from 25 to 5 kHz, depending on input conditions (assuming 80% converter efficiency). Thus, the non-conduction losses will become more significant. A general rule of thumb is that switching and conduction losses should be equal at maximum frequency [22]. Since 50 kHz is still a relatively low frequency and the duty cycle is high due

to the large conversion ratio, this rule of thumb was reduced to a 40-60 split of conduction to other losses.

The MOSFET was thus designed to have 120 400 μm wide gate fingers with a length of 0.8 μm (minimum length for manufacturing purposes). This MOSFET consumed 21 μW due to conduction loss and 30 μW due to other losses (switching, gate charge, and output capacitance under pre-layout simulations at 40 kHz, with an 80% duty cycle and $I_D = 200\mu\text{A}$ (600 μA load). With a 20 kHz, 90 % duty cycle at the same I_D , conduction loss increased to 48 μW and only 3 μW due to other losses. This satisfied the design goal of keeping total loss constant and low across the frequency spectrum by using the a 60-40 split of conduction to other losses at a midway operating point.

Gate Driver Design

It should be mentioned that a gate driver is required to drive the MOSFET with high current to reduce switching losses (Equation 3.8c) and the output of the AND gate used to create the signal D (refer to Fig. 3.2). A basic push-pull gate driver consisting of two back to back inverters was created. The width of the second inverter is larger than that of the first to provide more current to the gate of the power MOSFET and reduce switching loss by quickly turning on and off the MOSFET. The trade-off is larger gate driver power consumption. The designed gate driver with W/L ratios is shown in Fig. 3.6.

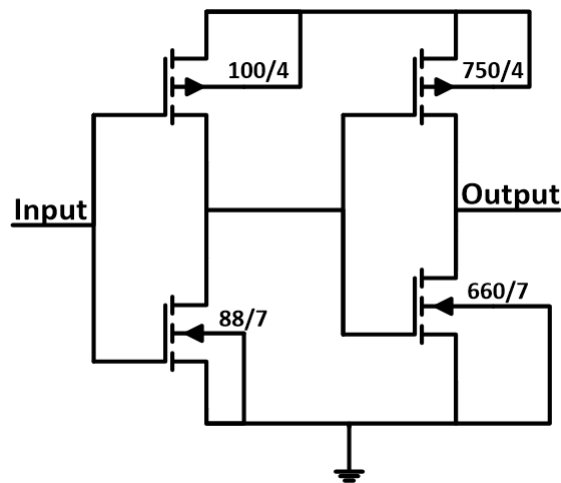


Figure 3.6: Push-pull gate driver schematic.

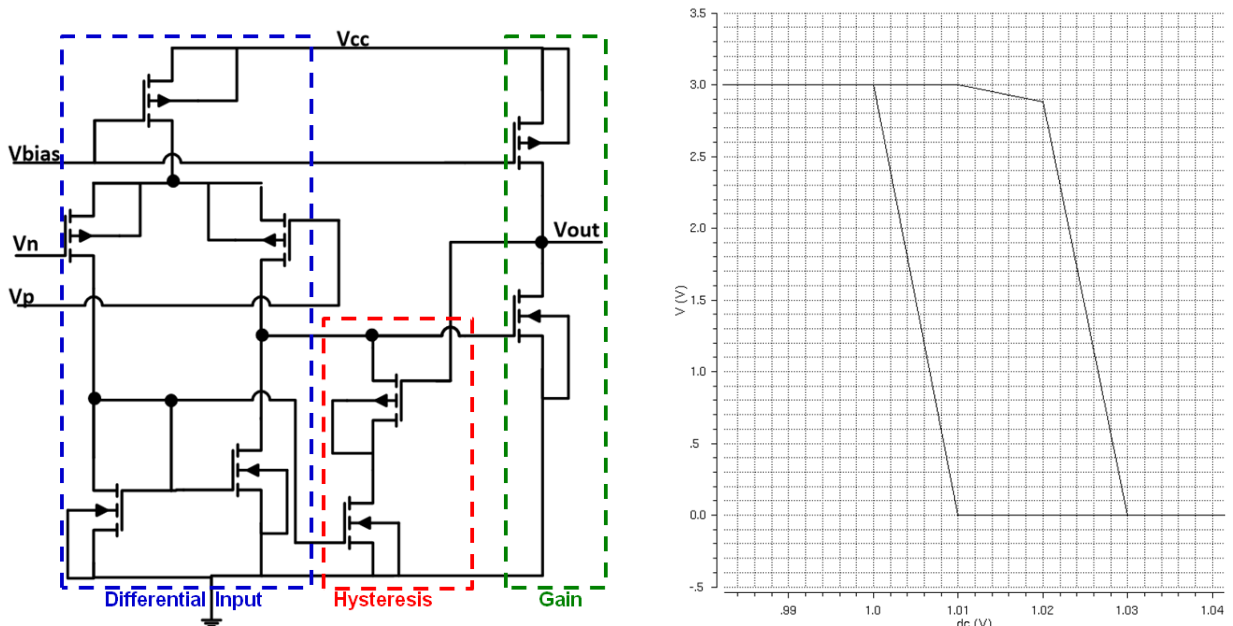
3.4 Design of the Control Blocks

This section details the design of the important unique control blocks: the low power comparators with hysteresis and the open circuit voltage sampler used to obtain V_{mpp} .

3.4.1 Comparator Design

The two comparators are critical to the proposed controller: the V_{out} comparator controls the burst of the converter and V_{in} controls D , or the switching of the power MOSFET. This control relies not only the function of the comparator, but also the size of its hysteresis. Furthermore, since the total power handled by the converter does not exceed 10 mW, it is also critical that these comparators consume as little power as possible.

Thus, a comparator design adapted from [8] is used to incorporate hysteresis with low power dissipation. This design is a simple differential input followed by an amplifier, with positive feedback providing one-sided hysteresis, as can be seen in Fig. 3.7a and Fig. 3.8a. Depending on the feedback loop, the hysteresis is either on the upper or lower edge. This simplifies the design and greatly reduces power consumption from the mW to the nW levels, compared to traditional three stage hysteretic comparator designs.

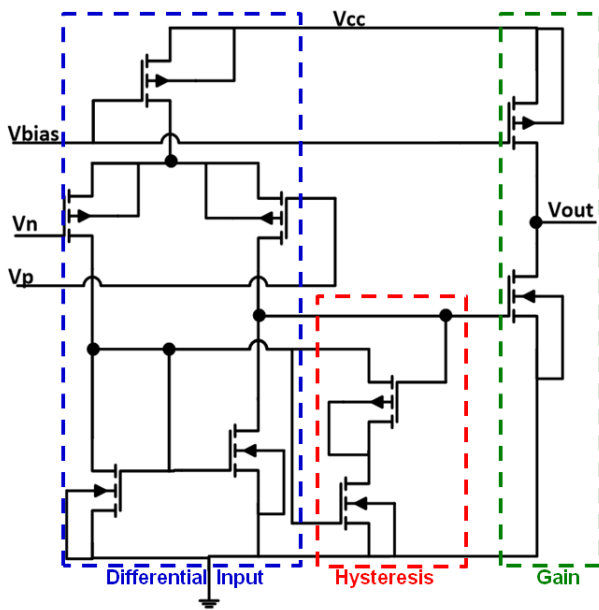


(a) V_{out} comparator design, with upper edge hysteresis. (b) DC Sweep of V_n , with $V_p = 1$ V.

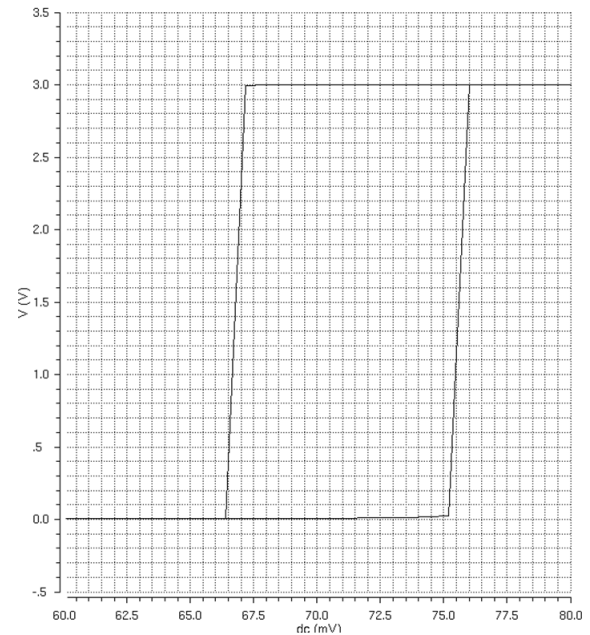
Figure 3.7: V_{out} comparator schematic and function.

Since the V_{out} comparator is being used to create a high output whenever V_{out} (negative differential input) falls to V_{ref} (positive differential input) and hold that signal until $V_{out} = V_{ref} + V_{hysteresis}$, the comparator is designed with hysteresis only on the upper side. This behavior is demonstrated in the simulation shown in Fig. 3.7b where the x-axis is the negative differential input and the positive differential input is 1 V. It can be seen the the output (y-axis) goes high at 1 V and stays high until the negative input has risen to 1.03 V, illustrating 30 mV hysteresis on the upper side.

Similarly, the V_{in} comparator needs to output low when V_{in} falls to V_{mpp} and remain low until V_{in} has risen an appropriate amount ($V_{hysteresis}$). This can be accomplished by having the differential input be $V_{in} - V_{mpp}$ and using hysteresis on the lower side, as illustrated in Fig. 3.8b. It can also be seen that at low input voltages, such as in Fig. 3.8b, there is a small 6 mV DC offset.



(a) V_{in} comparator, with lower edge hysteresis.



(b) DC Sweep of V_p , with $V_n = 65$ mV.

Figure 3.8: V_{in} comparator schematic and function.

3.4.2 Open Circuit Voltage Sampler

The open circuit voltage sampler (OCV) was designed to take store slightly less than half the open circuit voltage (since the stored voltage, V_{mpp} , would be the minimum V_{in} during the active period). The design is a basic sample and hold circuit and resistor-less capacitive divider, as based on a paper by [Liu]. It was designed with low capacitance on-chip capacitors to save space, but could still hold V_{mpp} within 10 mV for 20 ms. The design is shown in Fig. 3.9.

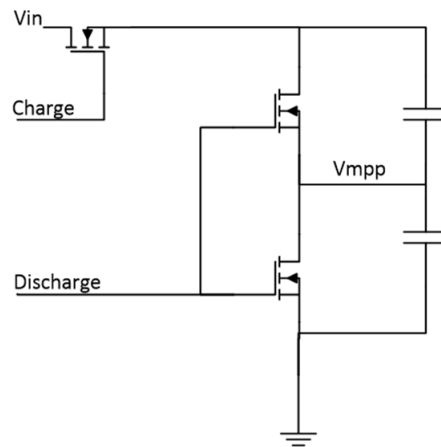


Figure 3.9: Schematic of OCV sampler.

As can be seen in Fig. 3.9, the signals that control the sampler are “Charge” and “Discharge”. These signals are based off the V_c burst control signal: V_c is actually about $50 \mu\text{s}$ delayed from the actual output of the V_{out} comparator, such that the charge and discharge of the OCV sampler can occur before the power stage begins switching. This is why it was imperative to choose an input capacitor small enough to allow even small V_{in} to raise to the open circuit voltage (V_{TEG}) during the smallest burst inactive periods. The timing of these signals is shown in Fig. 3.10 and the delays are created by using delayed inverters.

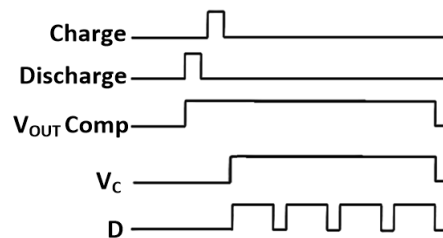


Figure 3.10: Timing diagram of OCV sampler control signals and delayed D control signal.

3.5 Layout

The proposed controller is implemented in $0.25\ \mu\text{m}$ CMOS, using the TI LBC7 PDK. The layout of the analog and digital control blocks and relevant references, along with the power stage MOSFET, is shown in Fig. 3.11. The entire chip size is $1.25\ \text{mm} \times 0.75\ \text{mm}$, mainly due to pad size (many pads were included for testing purposes, the actual chip would only need 4 pads). There is ESD protection circuitry included in the pad design, based on the design manual and [25]’s work. This design was completed and sent for fabrication in February 2016 and should be returned for testing in May/June 2016.

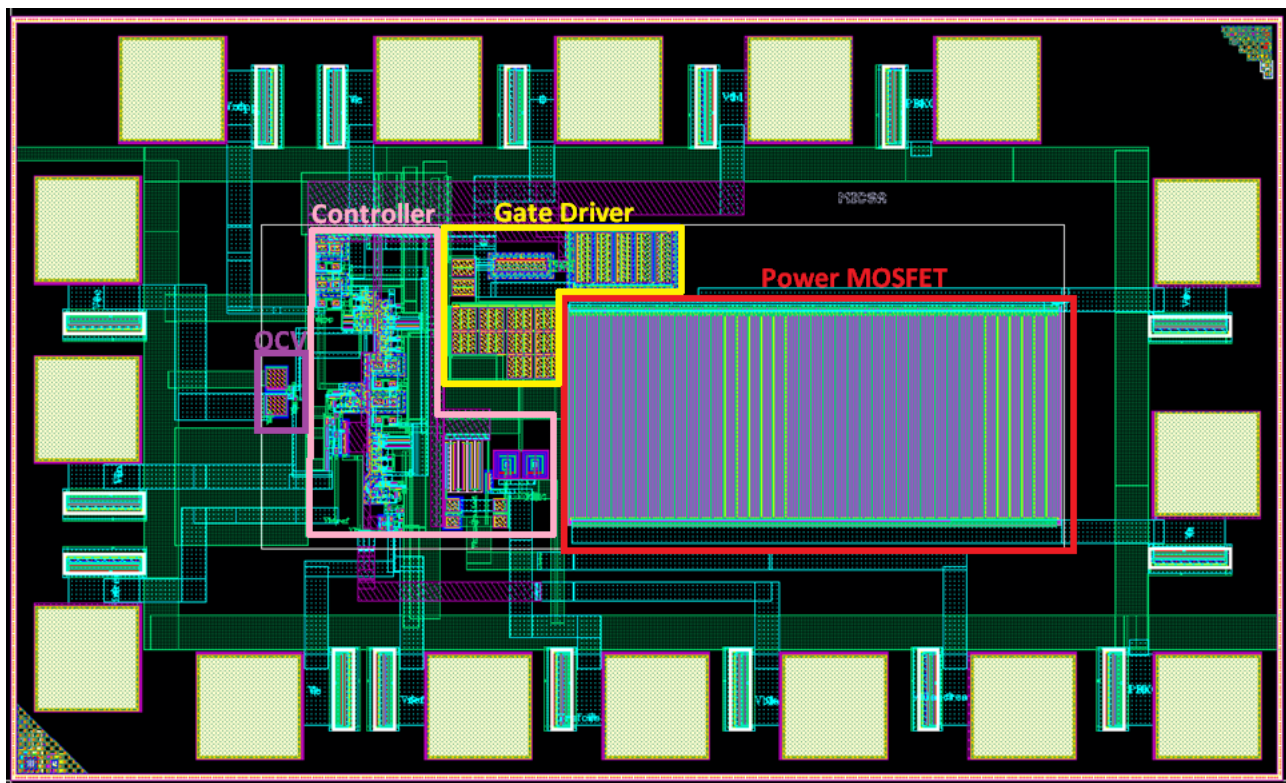


Figure 3.11: Final layout of PMIC, with relevant blocks highlighted.

Chapter 4

Simulation Results

This chapter describes the post-layout simulation results. Section 4.1 begins with confirmation of the operation of the proposed converter and then discusses benchmarks such as overall efficiency, converter efficiency, MPPT efficiency, and the sampling accuracy of the designed OCV sampler. These results are then compared with prior work in Section 4.2.

4.1 Post Layout Simulation Results

All results in this section are simulated using the final layout sent for tapeout in February 2016 (refer to Section 3.5) and the simulation testbench in Fig. 4.1. External components are assumed nonideal, so 5 mΩ ESR is added to the input and output capacitor and a SPICE model of the BAS40 diode, provided by Diodes, Incorporated, is used. The output capacitor is assumed to be precharged to 3.1 V (must be higher than maximum V_O , for converter to begin operating as no startup circuitry was incorporated in this design).

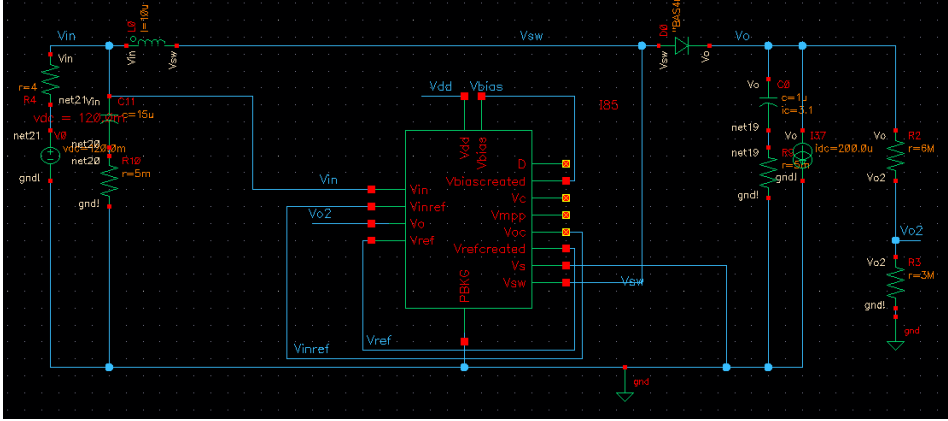


Figure 4.1: Testbench used for post-layout simulations.

4.1.1 Proposed Converter Control Operation Verification

This section details the verification of the converter control. Thus, an ideal voltage reference was used for V_{TEG} , which was varied from 50 mV to 500 mV (the entire input voltage range). It was found after tapeout (as detailed in section 4.1.5) that the designed on-chip OCV sampler did not work for long burst periods, so for consistency it was not used in any of the simulation results reported.

The voltage range, as explained in the beginning of the previous chapter, is 50 mV to 500 mV or the voltage at which $P_{MPP} = 10$ mW, whichever is greater. For example, the difference between operation at 50 mV and 500 mV at $R_{TEG} = 8 \Omega$ can be seen in Fig. 4.2, the converter appears stable and switches as expected, maintaining an output voltage of 3 V with a ripple of 55 mV. As anticipated, the burst length is much longer for higher conversion ratios (see Fig. 4.2b: the burst period when $V_{TEG} = 50$ mV is 80 ms, compared to just 0.35 ms at 500 mV). The figures are at the same time span to show more detail. Recall that the maximum power increases with TEG voltage (Eqn. 2.3), so thus switching frequency and duty cycle adjust accordingly. The switching frequency increases from 27 kHz to 56 kHz and the duty cycle increases from 0.37 to 0.69, as V_{TEG} increases from 50 mV to 500 mV. It should also be mentioned that input voltage ripple seems to vary slightly with input voltage (ripple ranging from 10 mV to 45 mV at 25 mV and 250 mV input, respectively).

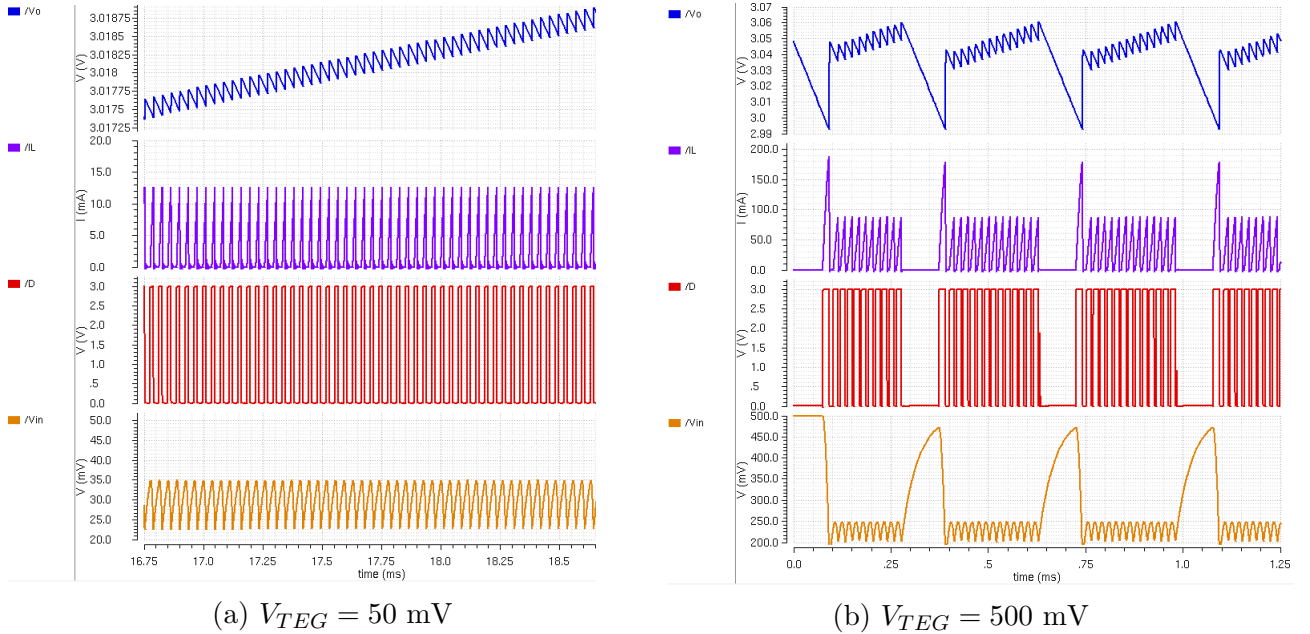


Figure 4.2: Converter waveforms at $V_{TEG} = 50, 500$ mV and $R_{TEG} = 8 \Omega$ of V_o (blue), I_L (purple), D (red), and V_{in} (orange).

The steady state waveforms of the converter were also verified across the R_{TEG} range (1-16 Ω). An example of the difference between an R_{TEG} of 1 Ω and 16 Ω , and thus power, is

displayed in Fig. 4.3. The power difference (P_{MPP}) is 2.5 mW and 156 μ W, respectively, as V_{TEG} is kept at 100 mV. It can be seen that, again, the duty cycle, frequency, burst cycle, etc. all varies between these two conditions. The burst period is 7.4 ms at 1 Ω and 40 ms at 16 Ω due to the increased load. The switching frequency is approximately (28 and 30 kHz, respectively); however the duty cycle is significantly higher at increased power. Interestingly, it can be seen that input resistance or increased power again affects the hysteresis of the input comparator by increasing the input ripple voltage from 10 mV to 40 mV.

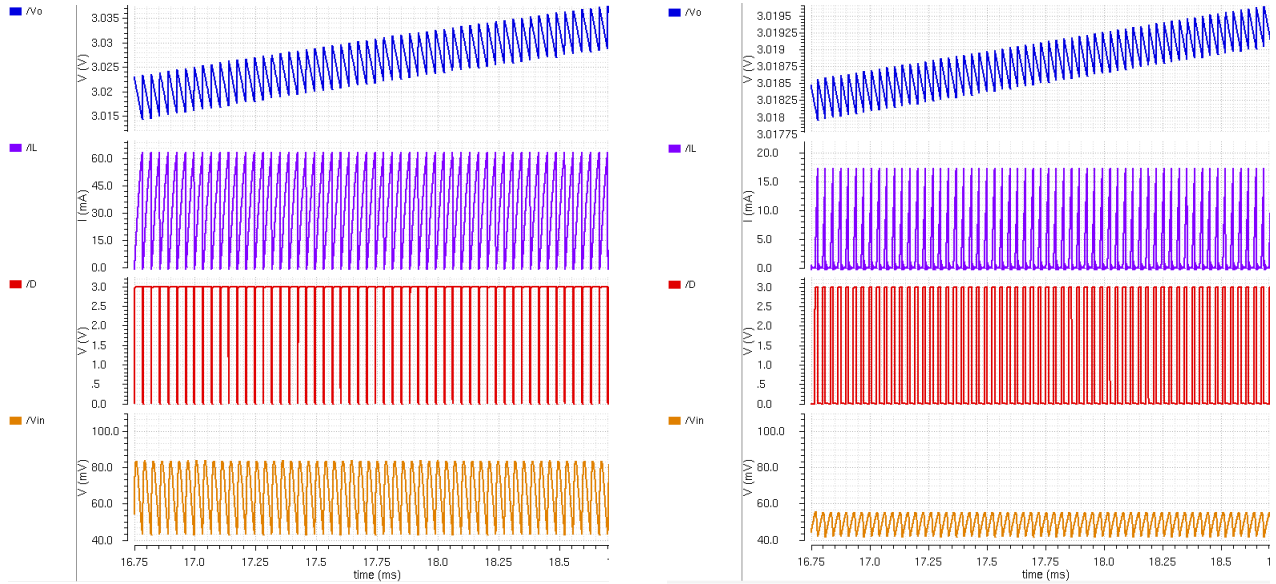
(a) $V_{TEG} = 1 \Omega$, $P_{MPP} = 2.5 \text{ mW}$ (b) $R_{TEG} = 16 \Omega$, $P_{MPP} = 156 \mu\text{W}$

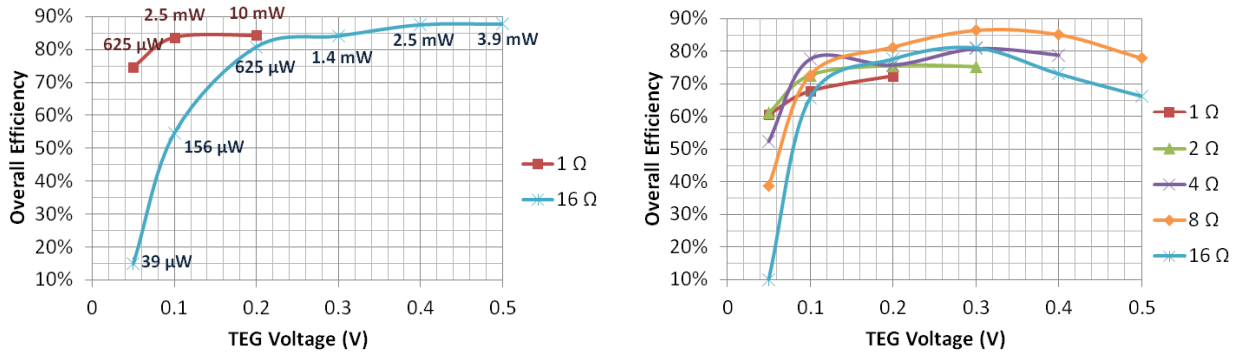
Figure 4.3: Converter waveforms at $V_{TEG} = 100 \text{ mV}$ and $R_{TEG} = 1, 16 \Omega$ of V_o (blue), I_L (purple), D (red), and V_{in} (orange)

4.1.2 Overall Efficiency

Since there are several variables that change (R_{TEG} , V_{TEG} , and thus P_{MPP}), several graphs will be described in this section to give the full picture of how converter efficiency varies. These graphs will be explained in depth within this section and then their format used again in the sections in converter and MPPT efficiency.

In Fig. 4.4, the graphs of overall efficiency vs. input voltage are displayed for several R_{TEG} (thus simulating various TEGs or TEG configurations at various temperature differences). Since the power can vary significantly at different R_{TEG} and V_{TEG} , Fig. 4.4a gives an idea of what the P_{MPP} , or the maximum power available to the system from the TEG, is at different V_{TEG} for the maximum and minimum input resistances; whereas Fig. 4.4b illustrates several

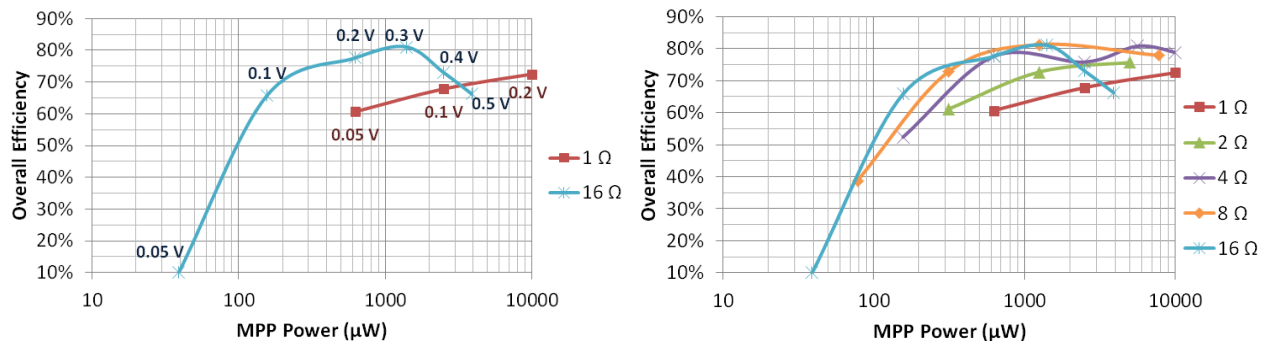
different resistance configurations at different input voltage. It can be seen that as input voltage increases, input power increases, and thus overall efficiency increases. The efficiency at the highest conversion ratio is the lowest for all resistances and particularly low at low resistance (and thus low power). For TEG voltages over 100 mV, the overall efficiency is greater than 60% for all resistances.



(a) Overall efficiency vs. V_{TEG} for selected R_{TEG} with power annotations. (b) Overall efficiency vs. V_{TEG} for selected R_{TEG} across entire range.

Figure 4.4: Overall efficiency vs. V_{TEG} for entire R_{TEG} range.

Fig. 4.5 displays this same data, but with the maximum power available from the TEG (P_{MPP}) as the x-axis. It should be noted that the overall efficiency peaks at mid-power range (see Fig. 4.5) for higher input resistances but peaks at maximum power for lower input resistances. The overall efficiency is over 60% for all resistance curves for $P_{MPP} > 300 \mu\text{W}$. From either of these two graphs it can be seen that the peak overall efficiency is 81% at several instances. Furthermore, the peak overall efficiency for $P_{MPP} < 500 \mu\text{W}$ and $V_{TEG} < 200 \text{ mV}$ is 73% at $R_{TEG} = 8 \Omega / V_{TEG} = 100 \text{ mV} / P_{MPP} = 313 \mu\text{W}$.

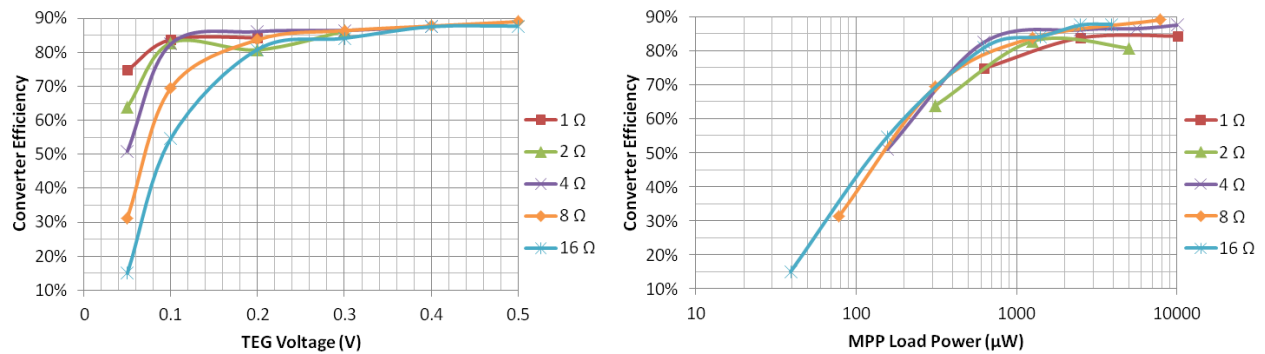


(a) Overall efficiency vs. P_{MPP} for selected R_{TEG} with annotated V_{TEG} . (b) Overall efficiency vs. P_{MPP} for selected R_{TEG} across entire range.

Figure 4.5: Overall efficiency vs. P_{MPP} for entire R_{TEG} range.

4.1.3 Converter Efficiency

The converter efficiency is the efficiency of the PMC without taking MPPT into account and is displayed in Fig. 4.6. Note that the data displayed in the graphs are the same, the x-axis has just changed such that the V_{TEG} trend can be separated from the P_{MPP} trend. It can be seen that the converter power is highest at conversion ratios above 10 ($V_{TEG} = 0.3$ V), regardless of input resistance (power). Similarly, for all input resistances, the converter efficiency is higher at higher powers.



(a) Converter efficiency vs. V_{TEG} for selected R_{TEG} across entire range. (b) Converter efficiency vs. P_{MPP} for selected R_{TEG} across entire range.

Figure 4.6: Converter efficiency for entire R_{TEG} and V_{TEG} ranges.

Fig. 4.7 presents the converter loss breakdown. This figure compares the difference in losses incurred at $V_{TEG} = 100$ mV between higher input resistance (less power) and smaller input resistance (more power). The diode is a prominent loss contributor in both cases; in fact, in all cases across the TEG voltage and resistance range, the diode contributed the most or second-most loss. The power MOSFET also contributes a large amount of loss; however, it can be seen that the loss is due to different things (on resistance vs. parasitic capacitance) depending on input conditions. This is because the MOSFET switches at 40 kHz with a 50% duty cycle at 8 Ω and 28 kHz with a 90% duty cycle at 1 Ω. Thus, the MOSFET conduction losses dominate at lower input resistance. The gate driver contributes a constant loss of 30 μW, which can become significant at lower powers. The controller loss (does not include gate driver) is the smallest. Simulated losses due to capacitor ESR were comparably insignificant (1 μW at 1 Ω) and thus are not shown.

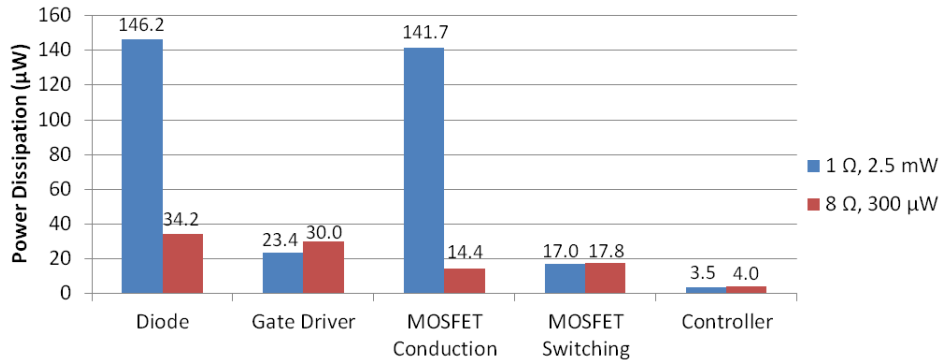
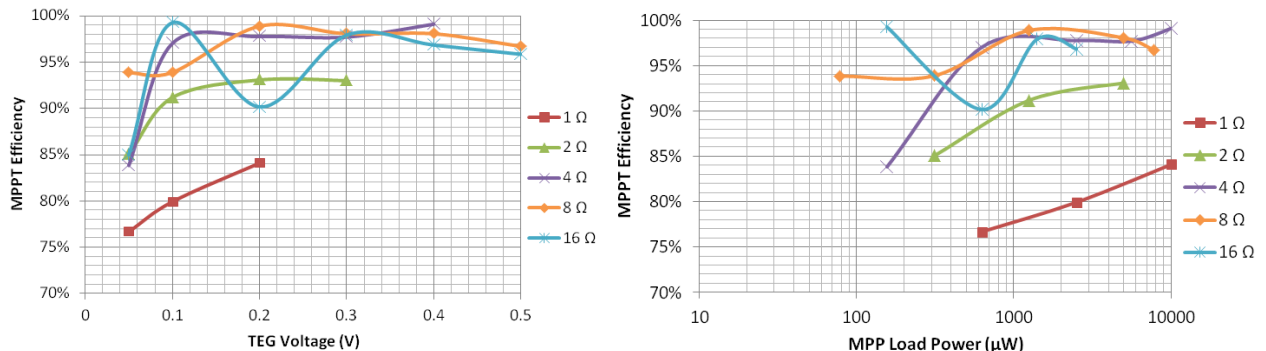


Figure 4.7: Power loss breakdown between two different TEG resistances at 100 mV.

4.1.4 MPPT Efficiency

As discussed in previous sections, the overall efficiency decreases at increased power but the converter efficiency does not. Thus, the overall efficiency must be decreasing due to not harvesting at the MPP. Fig. 4.8 shows the MPPT efficiency during the burst period (i.e. not including the inactive time in power calculations). However, it can be seen that the efficiency does not have any severely negative trends with input power. There is a trend with input resistance, though; as can be seen in Fig. 4.3, there is a higher ripple at higher input resistances, and thus, decreased matching efficiency. But for resistances above 1 Ω, it can be seen that the burst MPPT efficiency is high (above 90 % for $V_{TEG} > 100$ mV), meaning the input voltage feedback loop works well to match the input voltage to V_{MPP} .



(a) MPPT efficiency vs. V_{TEG} for selected R_{TEG} across entire range. (b) MPPT efficiency vs. P_{MPP} for selected R_{TEG} across entire range.

Figure 4.8: Burst ePPT Efficiency for entire R_{TEG} and V_{TEG} ranges.

Digging deeper into the data, it can be found that the reason the overall efficiency decreases at higher loads is actually very simple. The input capacitor needs to fully recharge to V_{TEG} during the inactive period; however, the inactive period is determined by output capacitor size and the load. When calculating overall efficiency, the largest load that still allows the

input capacitor to charge to 95% of V_{TEG} during the inactive period was used. Thus, at higher power (decreased inactive period) the maximum load current used was determined by the inactive period length, not the largest load that the converter could support (if given an external V_{MPP} reference). Thus, even if the matching efficiency during the burst is good (i.e., the input voltage feedback loop works well), the load will be smaller to increase the inactive period and thus reduce overall efficiency. This curve can be changed by redesigning the power stage and further reducing C_{in} ; however the f_{sw} would then increase, reducing converter efficiency. Since this design was aiming for a very flat curve, the tradeoff of decreased overall efficiency at higher input power for lower switching frequency (and thus higher converter efficiency) at low input powers was deemed acceptable.

4.1.5 Sampling Accuracy of OCV Sampler Block

It was found that the OCV sampling block did not act as expected at high input resistance and conversion ratio (longest burst periods). The voltage was divided down inaccurately and not held for the expected amount of time. For some input conditions, the converter is not able to operate with the taped out OCV sampling block connected at all, as can be seen in Fig. 4.9. Since V_{mpp} discharges too quickly, the switching frequency and duty cycle change during the active period as V_{mpp} changes. The duty cycle eventually becomes too large to maintain the output voltage. Unfortunately, this issue was not discovered until after the chip was sent off for manufacturing and thus, will also occur in testing. However, this block can be bypassed in testing to measure the operational functionality, overall efficiency, and matching accuracy at large input resistances. Future fabrications will move the OCV sampler's capacitors off-chip to allow for large capacitors and will use a resistive divider for more accurate sensing.

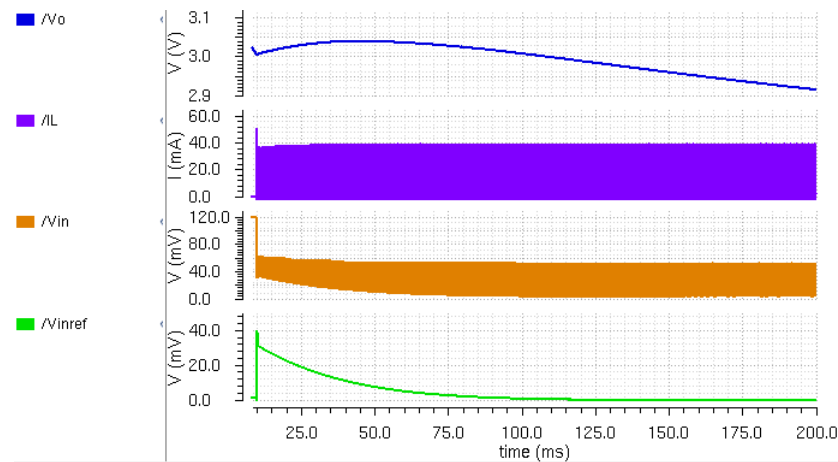


Figure 4.9: Failure of OCV sampling block at $V_{TEG} = 120$ mV and $R_{TEG} = 4 \Omega$.

4.2 Comparison with Other Works

Table 4.1 displays how this work compares to notable previous work in this area. It can be seen that the boost converter efficiency achieved in post-layout simulation is on-par with state of the field, particularly when the high conversion ratio (70 mV-3 V) and low input power (maximum 600 μ W) are taken into account. This work also uses the fractional open circuit voltage method to match the input resistance when the converter is extracting energy, ensuring maximum energy is extracted. Furthermore, the peak low power efficiency (less than 500 mW maximum power and 200 mV TEG voltage) is higher than other wide power range converters (e.g. Ahmed [8]), and on-par with narrower range and low conversion ratio converters, such as [6, 9].

Table 4.1: Comparison of Proposed Boost Converter with Prior Work

	Im [5]	Kim [7]	Liu [9]	Ahmed [8]	Zhang [6]	This Work
Minimum V_{in}	40 mV	70 mV	70 mV	12 mV	30 mV	70 mV
Output Voltage	2 V	3-5.8 V	1.8 V	0.66-3.3 V	0.5 V	3 V
Max. Output Power	2.7 mW	N/A	180 μ W	12 mW	150 μ W	600 μ W
Peak Efficiency	61%	72.2%	80%*	82%	74 %	81% *
Peak Low Power Efficiency	n/a	n/a	80%*	65%	74 %	73% *
MPPT	Yes	Yes	Yes	No	Yes	Yes
External V_{CC} required	No	Yes	Yes	No	No	Yes

*simulation only

Chapter 5

Conclusion

Energy harvesting from body heat using thermoelectric generators has the potential to provide energy savings to wearable systems and renewable energy for small sensor nodes. However, there are several key problems with this energy source, namely that it is a resistive voltage source that provides very low voltage at low power levels. This thesis research proposes an efficient boost converter controller to step up a range of low voltage with varying input resistance. The proposed controller consists of two hysteretic comparators that provide input voltage and output voltage feedback to provide maximum power point tracking and regulate the output to within 3% of 3 V. The controller has been taped out and post-layout simulations indicate good performance of most of the analog control blocks and a peak overall efficiency of 81%.

5.1 Key Contributions

The proposed boost converter provides several key contributions to the fields of ultralow power boost converters for thermoelectric energy harvesting. It utilizes burst mode and the fractional open circuit voltage method of MPPT to control both the input and output voltage. Using a simple control scheme and low power comparators, the input voltage is matched during harvesting within 2% while the controller has a quiescent current of less than 12 μA including the gate driver, and less than 2 μA excluding the gate driver. Due to the utilization of burst mode, the controller is able to boost input voltages as low as 50 mV to 3 V. A peak overall efficiency of 81% is expected, based on post-layout simulations. While prior works have achieved similarly high converter efficiencies (80 – 82%), they either did not include MPPT [8] or had a lower conversion ratio [9]. Furthermore, the converter works over a large voltage and power range and the simulated overall efficiency at low power and low voltage is 73%, which is higher than similarly high conversion ratio, wide range converters [5, 7, 8].

5.2 Future Improvements

There are several ways to continue and improve this work. As seen in Fig. 4.7, a large amount of loss is due to the external diode. To improve the converter efficiency, the proposed boost converter could be made synchronous by replacing the Schottky diode with a PMOS as in [11], [7], and [9]. This would increase controller complexity and power consumption, but the tradeoff with power stage efficiency may be worthwhile. Using a PMOS also decreases the peak inductor current as the voltage drop across the PMOS would be much less than the Schottky diode, thus effectively decreasing the conversion ratio. Reducing other converter losses or increasing MPPT accuracy would further increase overall efficiency.

Furthermore, now that the converter steady state control scheme has been established, incorporating a low voltage startup oscillation technique as in [5] or using a subthreshold voltage technique as in [8] would allow the circuit to start-up without a precharged output capacitor or operation without an external V_{CC} . This improvement would make the proposed converter more independent and thus a more attractive and viable candidate for thermoelectric energy harvesting.

These improvements are left for future research in ultralow power boost converters for energy harvesting, as well as low power analog electronics.

Appendix A

MATLAB code used for to estimate DT_s , D_1T_s , and D_2T_s for preliminary design purposes, as referenced in Section 3.3.1.

```
RTEG = 1;
Cin = 5e-6;
ESRCin = 0.005;
L = 33e-6;
VTEG = 120e-3;
Vmpp = VTEG*0.35;
dHys = 50e-3;
Vinmax = Vmpp+dHys;
Vd = 240e-3;
Vo = 3;
Co = 22e-6;
Io = 100e-6;
dVo = 50e-3;
Vomax = Vo+dVo;

%Solving for DTs
vin0 = Vinmax;
dvin0 = (VTEG-vin0)/((RTEG)*Cin);

alpha = 1/(2*(RTEG)*Cin);
wo = 1/(L*Cin)^0.5;
gamma = alpha/wo;
syms t

if gamma > 1
    a1 = wo*(-gamma + (gamma^2-1)^0.5);
    a2 = wo*(-gamma - (gamma^2-1)^0.5);
    A1 = vin0 - (dvin0-a1*vin0)/(a2-a1);
    A2 = (dvin0-a1*vin0)/(a2-a1);
    eqn = A1*exp(a1*t)+A2*exp(a2*t);
elseif gamma == 1
    d1 = -alpha;
    D1 = dvin0 + alpha*vin0;
    D2 = vin0;
```

```

    eqn = D1*t*exp(d1*t)+D2*exp(d1*t);
elseif gamma < 1
    b1 = -alpha;
    wd = (wo^2-alpha^2)^0.5;
    B1 = vin0;
    B2 = (dvin0 + alpha*vin0)/(wd);
    eqn = exp(b1*t)*(B1*cos(wd*t)+B2*sin(wd*t));
end

DTs = vpasolve(eqn == Vmpp,t, [0 0.001]);
DTs_us = double(DTs)*1e6

%Solving for D1Ts
%iL0 = 1/L integral(vin(t)) from 0 to DTs
DTs = double(DTs);
if gamma > 1
    IL0 = 1/L * (A1/a1*exp(a1*DTs)+A2/a2*exp(a2*DTs) - A1/a1-A2/a2);
elseif gamma == 1
    IL0 = 1/L * (exp(d1*DTs)/d1*(D1*DTs-D1/d1+D2) - D2+D1/d1);
elseif gamma < 1
    IL0 = 1/L*( exp(b1*DTs)*((B1*wd+B2*b1)*sin(wd*DTs)+(B1*b1-B2*wd) ...
    *cos(wd*DTs)) - B1*b1 +B2*wd)/(b1^2+wd^2);
end

D1Ts = IL0*L/(Vo+Vd-Vmpp);
D1Ts_us = D1Ts*1e6

%Solving for D2Ts
D2Ts = -RTEG*Cin*log(1-(Vinmax-Vmpp)/VTEG);
D2Ts_us = D2Ts*1e6

T_us = DTs_us+D1Ts_us+D2Ts_us
D = DTs_us/T_us
D_diode = D1Ts_us/T_us
fsw_kHz = 1/T_us*1000

ILpksw_mA = double(IL0*1000)

%Compare the hos much Vo rises and falls each MOSFET switching cycle
%Rise must be greater than fall to maintain Vo
Vorisesw_mV = (IL0)/Co * D1Ts * 1e3/2
Vofallsw_mV = Io/Co * (DTs+D2Ts) * 1e3
ratio = Vorisesw_mV/Vofallsw_mV

%Capacitor Charging & Discharging--compare burst dead time to time to OCV
t_CinChargetoOCV_ms = -RTEG*Cin*log(1-(VTEG-Vmpp)/(VTEG+Vmpp))*1000
t_deadTime_ms = -Vo*Co*log(Vo/Vomax)/Io*1000

```

Bibliography

- [1] B. T. Lynch, “Wearable Computing Devices, Like Apples iWatch, Will Exceed 485 Million Annual Shipments by 2018,” Online, ABI Research, Feb. 2013. [Online]. Available: <https://www.abiresearch.com/press/wearable-computing-devices-like-apples-iwatch-will/>
- [2] S. Hiremath, G. Yang, and K. Mankodiya, “Wearable internet of things: Concept, architectural components and promises for person-centered healthcare,” in *Wireless Mobile Communication and Healthcare (Mobihealth), 2014 EAI 4th International Conference on*, Nov 2014, pp. 304–307.
- [3] A. Klinefelter, N. E. Roberts, Y. Shakhsheer, P. Gonzalez, A. Shrivastava, A. Roy, K. Craig, M. Faisal, J. Boley, S. Oh, Y. Zhang, D. Akella, D. D. Wentzloff, and B. H. Calhoun, “21.3 a 6.45 μ w self-powered iot soc with integrated energy-harvesting power management and ulp asymmetric radios,” in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.
- [4] Y. K. Ramadass and A. P. Chandrakasan, “A battery-less thermoelectric energy harvesting interface circuit with 35 mv startup voltage,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan 2011.
- [5] J. P. Im, S. W. Wang, S. T. Ryu, and G. H. Cho, “A 40 mV Transformer-Reuse Self-Startup Boost Converter With MPPT Control for Thermoelectric Energy Harvesting,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3055–3067, Dec 2012.
- [6] Y. Zhang, F. Zhang, Y. Shakhsheer, J. D. Silver, A. Klinefelter, M. Nagaraju, J. Boley, J. Pandey, A. Shrivastava, E. J. Carlson, A. Wood, B. H. Calhoun, and B. P. Otis, “A batteryless 19 μ w mics/ism-band energy harvesting body sensor node soc for exg applications,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 199–213, Jan 2013.
- [7] J. Kim and C. Kim, “A DC-DC Boost Converter With Variation-Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications,” *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3827–3833, Aug 2013.

- [8] K. Z. Ahmed and S. Mukhopadhyay, "A Wide Conversion Ratio, Extended Input 3.5- μ A Boost Regulator With 82% Efficiency for Low-Voltage Energy Harvesting," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4776–4786, Sept 2014.
- [9] S. Liu, Y. Zhao, M. Zhao, H. Zhang, and X. Wu, "A burst-mode based boost converter harvesting photovoltaic energy for low power applications," in *Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on*, Aug 2014, pp. 49–52.
- [10] V. Leonov, "Thermoelectric energy harvesters for powering wearable sensors," in *Sensors, 2012 IEEE*, Oct 2012, pp. 1–4.
- [11] E. J. Carlson, K. Strunz, and B. P. Otis, "A 20 mV Input Boost Converter With Efficient Digital Control for Thermoelectric Energy Harvesting," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, April 2010.
- [12] "Thermoelectric Power Generating solutions: MD04-031-xxTEG," Online, RMT, LTD. [Online]. Available: http://www.rmtltd.ru/datasheets/Thermoelectric_Generators/1md04031_teg.pdf
- [13] "Thin Film Thermogenerator: MPG-D655 Preliminary Datasheet," Online, micropelt. [Online]. Available: http://micropelt.com/downloads/datasheet_mpg_d655.pdf
- [14] "Thermoelectric Power Generating solutions: MD10-111-xxTEG," Online, RMT, LTD. [Online]. Available: http://www.rmtltd.ru/datasheets/Thermoelectric_Generators/1md10111_teg.pdf
- [15] "eTEG HV56 Power generator," Online, Nextreme. [Online]. Available: http://www.mouser.com/ds/2/292/Nextreme_eTEG_HV56_Data_Sheet-3613.pdf
- [16] "TEG2-126LDTr," Online, TEC. [Online]. Available: <http://thermoelectric-generator.com/thermoelectric-lower-temperature-power-module-selections/>
- [17] "TEM12 Single Stage Thermoelectric Module," Phononic.
- [18] "Thermoelectric Power Generating solutions: MD06-127-xxTEG," Online, RMT, LTD. [Online]. Available: http://www.rmtltd.ru/datasheets/Thermoelectric_Generators/1md06127_teg.pdf
- [19] N. Kong and D. S. Ha, "Low-power design of a self-powered piezoelectric energy harvesting system with maximum power point tracking," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2298–2308, May 2012.
- [20] J. Ahmad, "A fractional open circuit voltage based maximum power point tracker for photovoltaic arrays," in *Software Technology and Engineering (ICSTE), 2010 2nd International Conference on*, vol. 1, Oct 2010, pp. V1–247–V1–250.

- [21] C. Wang, Z. Li, K. Zhao, and Q. Guo, "Efficient self-powered convertor with digitally controlled oscillator-based adaptive maximum power point tracking and rf kick-start for ultralow-voltage thermoelectric energy harvesting," *IET Circuits, Devices Systems*, vol. 10, no. 2, pp. 147–155, 2016.
- [22] B. T. Lynch, "Under the Hood of a DC/DC Boost Converter," TI Power Supply Design Seminar, pp. 3.1–3.26, 2008-2009.
- [23] "MSP432P401R (PREVIEW)," Online, TI. [Online]. Available: <http://www.ti.com/product/msp432p401r/datasheet>
- [24] "Ultra Low Power Microcontroller," Online, Ambiq Micro. [Online]. Available: <http://ambiqmicro.com/low-power-microcontroller>
- [25] Z. Gao, "A Two-Mode Buck Converter Toward High Efficiency for Entire Load Range for Low Power Applications," Master's thesis, Virginia Polytechnic Institute and State University, 2015.