Passive Balancing of Switching Transients between Paralleled SiC MOSFETs

Yincan Mao

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

Khai D. T. Ngo (Chair)
Rolando Burgos
Guo-Quan Lu
Dong S. Ha
Lei Zuo

December 12th, 2017
Blacksburg, Virginia

Keywords: paralleled SiC MOSFETs, dynamic balancing, passive compensation, magnetic coupling, modeling

Passive Balancing of Switching Transients between Paralleled SiC MOSFETs

Yincan Mao

Abstract

The SiC MOSFET has attracted interest due to its superior characteristics compared to its Si counterpart. Several SiC MOSFETs are usually paralleled to increase current capability, considering cost effectiveness and manufacturability. Current unbalance among the MOSFETs is a concern as it affects reliability. The two main causes are asymmetrical layout and parameter mismatch. The variation in parameters, unlike circuit or module layout, is unavoidable during production. Among all the parameters of MOSFET, the spreads in on-state resistance ($R_{ds(on)}$) and threshold voltage (V_{th}) are the major concerns during paralleling. The disparity in $R_{ds(on)}$ causes static current unbalance which is self-limited due to the positive temperature coefficient of $R_{ds(on)}$. Its influence is not investigated here. The threshold voltage V_{th} has a negative temperature coefficient, forcing the MOSFET with lower V_{th} to carry more current during switching transient. Paralleled MOSFETs are usually de-rated to guarantee safe operation. Balancing of peak currents during switching transient is the goal of this work.

Integration of current/voltage sensors into paralleled structure is difficult in real application. Complicated feedback loop design and separate gate drivers also need to be avoided in perspective of cost and volume. Passive balancing solutions are investigated in this dissertation. The inductors and resistors most effective in improving current sharing are identified by parametric analysis.

Their current balancing mechanisms are analyzed in circuit point of view. The design guidelines involving the magnitude of V_{th} mismatch, current rise time, and unbalance percentage are derived for the selection of passive components. The theory upholds well when substantial parasitics from device package and layout exist.

Several passive balancing structures are analyzed and compared in terms of current balancing capability, voltage stress, total switching loss, and switching loss difference. All of them can provide much better current and power balancing without increasing switching loss. Some of the them may increase the stress-inducing inductance, which can be reduced by negative magnetic coupling. Perfect coupling between power-source inductors would enable current matching without penalty on voltage stress.

Common-source inductance (L_{cm}) is effective in dynamic balancing, but at the expense of higher switching loss. It is not considered in power module application because Kelvin connection is normally applied. However, wire bond inside the package of discrete MOSFETs and part of the external leads are inevitable and add to L_{cm}. Peak-current and switching energy mismatches vary with operating conditions (including input voltage, input current, and switching speed). Design guidelines and procedures that are valid for wide operating range are provided for cases with and without L_{cm}.

This dissertation also models the switching energy and switching energy mismatch of paralleled MOSFETs. The influence of operating conditions, passive balancing components, layout and package parasitic inductances, nonlinear channel performance, and voltage dependent parasitic capacitors are included in the modeling process. The resulting high order system is simplified by reducing the number of passive components and number of devices without losing

accuracy. The influence of current balancing components and magnitude of threshold voltage mismatch on sharing are discussed based on modeling results.

In conclusion, this dissertation balances the transient currents between paralleled SiC MOSFETs automatically by inductance, resistance and magnetic coupling. This procedure is done utilizing one gate driver without current/voltage sensors and feedback loop. Those solutions work for both polarities of V_{th} mismatch and force balancing from the first current peak. Design guidelines involving the magnitude of V_{th} mismatch, current rise time, and maximum peak-current difference are derived to guide the choice of passive components. The detail design procedures are recommended to force currents to share over wide operating range. The aforementioned benefits are demonstrated by two paralleled SiC MOSFETs (C2M0160120D) tested at variant operating conditions. The difference of peak currents can be reduced below 5% of steady-state current in every switching transient. Switching energy mismatch percentage can be reduced by 6 times without increasing total switching energy.

Passive Balancing of Switching Transients between Paralleled SiC MOSFETs

Yincan Mao

General Audience Abstract

This research focuses on balancing currents between paralleled SiC MOSFETs. Several SiC MOSFETs are usually paralleled to increase current capability. Current unbalance among MOSFETs caused by variation in parameters is a concern as it affects reliability. Several passive balancing structures are proposed in this dissertation. All of them can provide much better current and power sharing without great scarification of other switching performance. Severity of unbalance varies with operating conditions (including input voltage, input current, and switching speed). Design guidelines and procedures that are valid for a wide operating range are provided. This dissertation also models the switching energy and switching energy mismatch of paralleled MOSFETs. The resulting high order system is simplified by reducing the number of passive components and number of devices without losing accuracy. More findings are discussed based on modeling results. The effectiveness of passive balancing methods are demonstrated by two paralleled SiC MOSFETs tested at variant operating conditions. The difference of peak currents can be reduced below 5% of steady-state current in every switching transient. Switching energy mismatch percentage can be reduced by 6 times without increasing total switching energy.

To My Family

And To Whom It May Concern

Acknowledgments

I would like to express the deepest appreciation to my advisor Dr. Khai D. T. Ngo, for his guidance, encouragement, support, and patience. I have been extremely lucky to have him as my supervisor during this journey of research. His profound knowledge, persistency, and rigorous attitude help me tackle lots of difficulties and challenges. I would like to thank him for opening the research door for me and guiding me along the research path. His patience and scientific advising are great fortunes for my research, career, and even my life. This dissertation would not have been written without his help and encouragement.

I am also grateful to my committee members Dr. Rolando Burgos, Dr. Guo-Quan Lu, Dr. Dong S. Ha, and Dr. Lei Zuo for their valuable comments and insightful suggestions.

I would like to thank my wonderful colleagues at CPES. It is my great honor to work with them. They are: Mr. Zichen Miao, Mr. Ting Ge, Mr. Lujie Zhang, Mr. Chien-An Chen, Dr. Yi Yan, Dr. Ming Lu, Dr. Milisav Danilovic, Dr. Zhemin Zhang, Dr. Han Cui, Dr. Jongwon Shin, Dr. Woochan Kim, Mr. Joseph Kozak, Mr. Xuebing Chen, Mr. Zhongsheng Cao, Dr. Zhengyang Liu, Dr. Xiucheng Huang, Dr. Dongbin Hou, Mr. Bin Li, Mr. Shishuo Zhao, Mr. Junjie Feng, Mr. Qiong Wang, Mr. Chao Fei, Mr. Jun Wang, Mr. Chi Li, Mr. Wei Zhang, Ms. Ye Tang, Mr. Jianghui Yu, Ms. Virginia Li, Ms. Niloofar Rashidimehrabadi, Mr. Shan Gao, Ms. Bingyao Sun, and Ms. Christina DiMarino.

My thanks also go to the wonderful CPES staff who are always willing to help me out: Mr. David Gilham, Mr. Igor Cvetkovic, Ms. Trish Rose, Ms. Teresa Shaw, Ms. Marianne Hawthorne, Ms. Linda Long, and Ms. Lauren Shutt.

Most importantly, I would like to my parents Suqiong Yin and Yuechun Mao, and my fiancé Jue Wang. It is their love that supports and encourages me to move forward during all these years.

I also want to thank Toyota Motor Engineering & Manufacturing - North America for providing financial support for this research.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

Nomenclature

V_{th}	Threshold voltage
$R_{ds(on)}$	On-state resistance
g_{fs}	Large signal transconductance
ΔV_{th}	Mismatch of threshold voltages
i_{ds}	Channel current of MOSFET
P	Instantaneous power loss

1.1 Background

Silicon Carbide (SiC), as a wide band gap (WBG) material, has attracted interest due to its superior performance as compared to silicon (Si) counterparts. It has ten-time breakdown field, three times thermal conductivity and a three-time band gap of silicon [1], [2]. With those properties, lower on-state resistance, higher blocking voltage, faster switching speed, and higher temperature operation can be achieved [3]-[6]. As a result, SiC based MOSFETs are suitable for applications such as aerospace [7], [8], oil drilling [9], transportation [10], [11], renewable energies [12] and some industry equipment [13]. More and more commercialized SiC MOSFETs are available on the market through intensive research done in this decade. Fig. 1-1 summarizes the available current ratings of SiC MOSFFETs from CREE for different blocking voltages [14]. The highest current rating available for a single MOSFET (either as bare die or packaged MOSFET) is less than 100 A (which is also the highest among products of other manufactures).

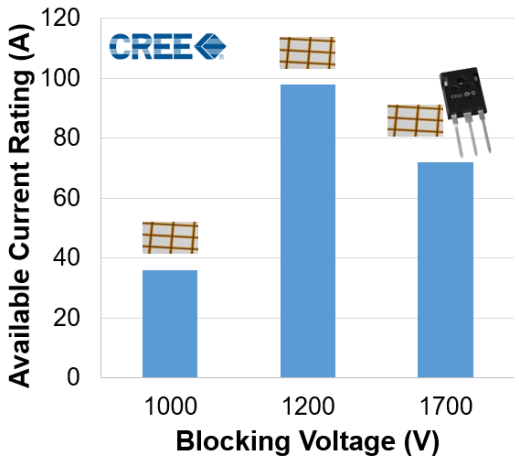


Fig. 1-1. Available current ratings of SiC MOSFETs (as bare die or packaged MOSFETs) for different blocking voltages [14].

Several hundreds or even higher current rating is required in medium-power and high-power applications. The most straightforward way to satisfy the demand is to produce high current rating MOSFETs. However, there are two challenges. Firstly, higher current rating means larger die area. Price increases exponentially with current rating [15]. Crystal defects will lead to lower manufacturing yield and raise costs [16]-[18]. Secondly, large die introduces more waste area on the wafer, which also results in extra cost [15]. Several SiC MOSFETs are usually parallel to increase current capability, considering cost effectiveness and manufacturability (as illustrated in Fig. 1-2) [15], [19]-[24]. Either bare dies or discrete MOSFETs can to be paralleled, as shown in Fig. 1-3. Paralleling discrete MOSFETs is simpler, more cost effective, and more flexible than paralleling bare die, especially for a small number of MOSFETs. However, the internal package of discrete MOSFETs leads to more parasitics (especially common-source inductances) and spaces. Paralleling bare dies requires more sophisticated design. One example is shown in Fig. 1-3 [15]. In this module, every switch is composed of two 80 A SiC MOSFETs. An additional 50 A junction

barrier Schottky (JBS) diode is connected in anti-parallel with MOSFET to bypass the internal body diode. The resulting current rating is 100 A.

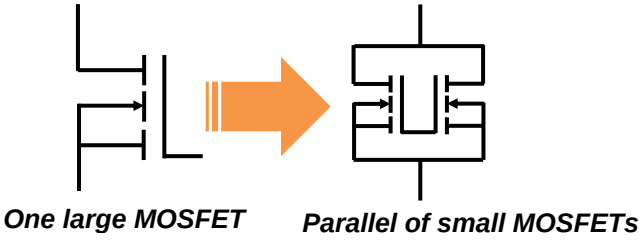


Fig. 1-2. Realization of an equivalent large die by paralleling MOSFETs with small die area.

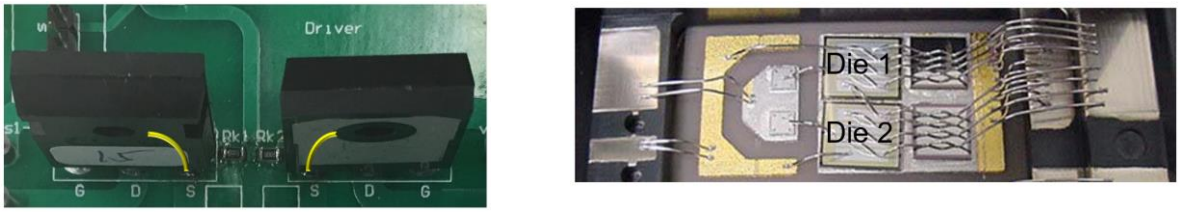


Fig. 1-3. (a) Paralleling of discrete SiC MOSFETs, and (b) internal view of a SiC power module with two SiC MOSFETs and two SiC JBS diodes per switch [15].

Paralleled MOSFETs cannot resemble a single one due to the unavoidable variation in MOSFET parameters during production. The variations in on-state resistance ($R_{ds(on)}$) and threshold voltage (V_{th}) cause imbalance during steady state and switching transients [25]-[30], respectively. The positive temperature coefficient of $R_{ds(on)}$ can help balance the currents [31], [32]. Its influence is not investigated here. The negative temperature coefficient of V_{th} (as shown in Fig. 1-4 [33]) tends to worsen the mismatch of currents [34]. Dynamic current imbalance can cause localized over-current and over-temperature. The reliability and lifetime of MOSFETs are adversely affected [35]-[38]. Current de-rating is required even with screened MOSFETs [39]. Fig.

1-5 (a) shows the variation of threshold voltage (V_{th}) within 30 samples measured in [24]. The highest and lowest values are 3.08 V and 2.48 V, respectively, resulting in 0.6 V difference. Larger variation is expected if more samples were measured. Fig. 1-5 (b) shows the comparison of transfer curves of two MOSFETs with different threshold voltages. According to the figure, MOSFET with smaller V_{th} has larger current share during dynamic region.

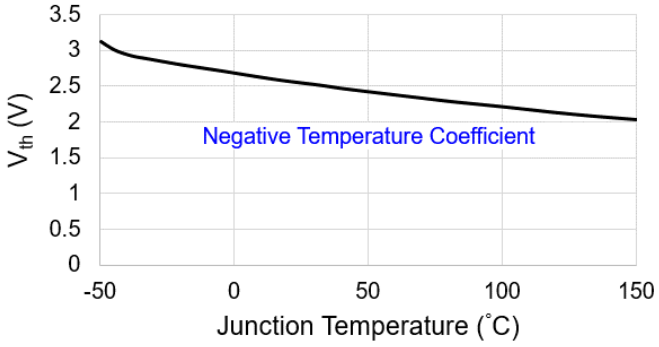
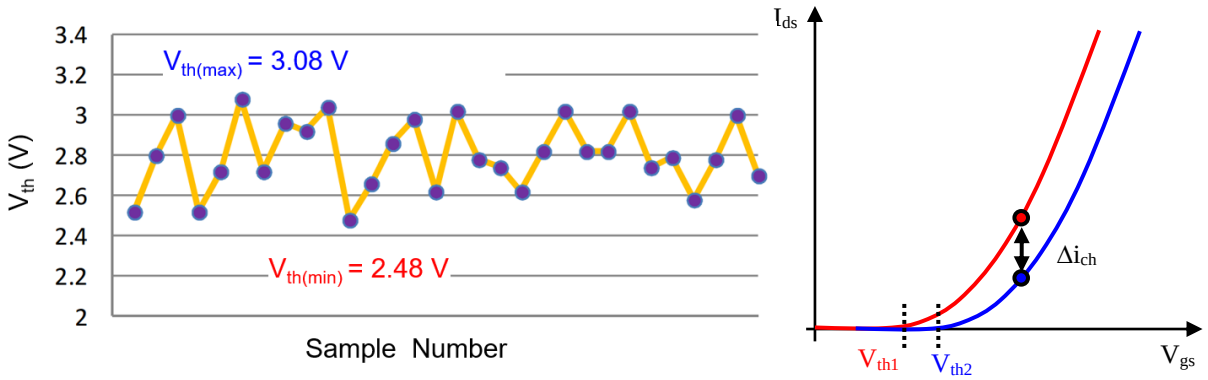


Fig. 1-4. Negative temperature coefficient of threshold voltage [33].



(a) **(b)**

Fig. 1-5. (a) Variation of threshold voltage (V_{th}) from sample to sample [24]; (b) transfer characteristics of MOSFETs with different threshold voltages.

Double-pulse tester is utilized for testing of switching transients. The schematic is shown in Fig. 1-6. Inductive load is modeled by a constant current source for simplicity. The high side

consists of a SiC Schottky diode with no reverse recovery. The low side is composed of two SiC MOSFETs with V_{th1} = 2.48 V and V_{th2} = 3.08.

The DPT tests two short pulses. The switching transients are captured at the first falling and rising edges at room temperature (with negligible change in junction temperatures). Simulation results of Fig. 1-6 are illustrated in Fig. 1-7. According to the waveforms, MOSFET M1 (which has a smaller V_{th}) carries higher current than M2 during both turn-on and turn-off switching transients. The current mismatch also leads to switching loss unbalance. The one consumes more power will have less lifetime and is the bottleneck of the paralleled structure [40]-[43].

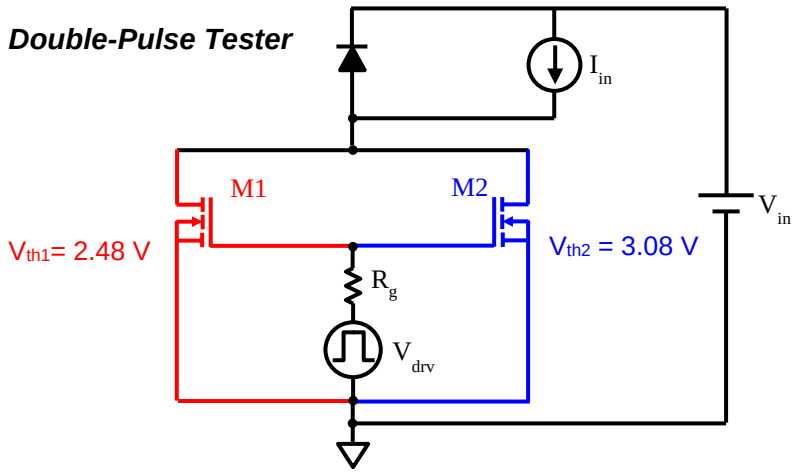


Fig. 1-6. Schematic of double-pulse tester for testing of switching transients. Low side is composed of two paralleled MOSFETs with different threshold voltages.

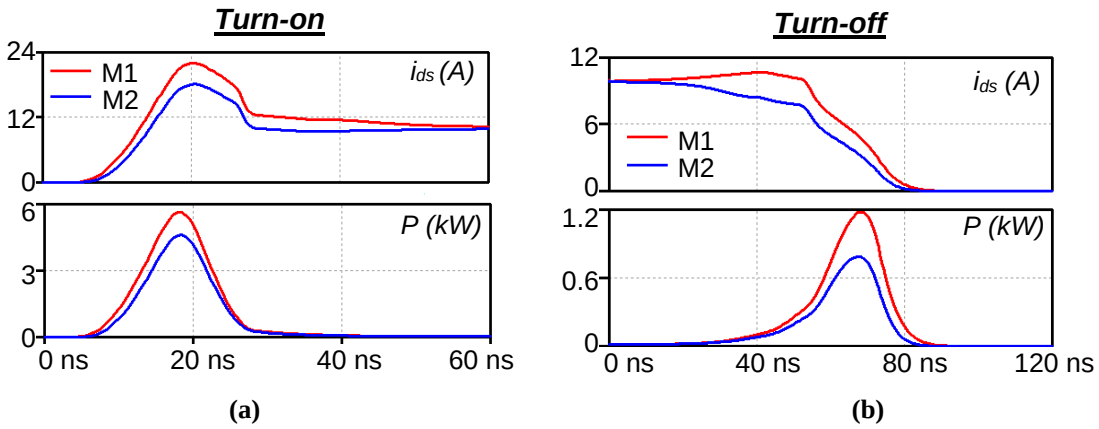


Fig. 1-7. Simulation results of Fig. 1-6. SPICE models of MOSFETs (C2M0160120D) and Schottky diode (CPW51200Z050B) are from Cree. (a) Drain-source currents and power losses during turn-on transients; (b) drain-source currents and power losses during turn-off transients

1.2 Research Motivations and Objectives

Current unbalance among MOSFETs is a concern as it affects reliability [44]-[48]. Paralleled MOSFETs are usually de-rated to guarantee safe operation [49]-[54], which means more MOSFETs need to be paralleled to achieve certain current capabilities. There are several drawbacks when more MOSFETs are paralleled. Firstly, the price of this parallel structure is increased, considering SiC MOSFET is much more expensive than Si counterparts [16]. Secondly, the volume is increased when more MOSFETs are paralleled. This may be a problem when power density is crucial [55]. Thirdly, an increase in the number of MOSFETs greatly aggregates the complexity of layout design. Either volume or layout parasitics or layout symmetry needs to be sacrificed.

The objective of this dissertation is to propose dynamic balancing solutions that can balance currents during switching transients without greatly increase the complexity, volume, and price of the original parallel structure. The desired balancing effect should be achieved without sacrificing

other switching characteristics, such as switching energy and voltage stress. The details are summarized in Fig. 1-8 and listed as follows.

- **Instant balancing** — Current balancing should be achieved within one switching cycle or instantaneously. This can promise good sharing in every switching transient. A double-pulse tester, which captures switching transients at the first falling and rising edges, can be utilized for demonstration.
- **No voltage and current sensors** — The price and size of sensors are important, especially for power module application. The current/voltage of every device should be sensed. The current/voltage of wire bond, instead of copper trace, needs to be sensed to obtain the switching information of a specific device. Internal current/voltage cannot be accessed for commercialized power modules. Current/voltage sensors must be embedded inside. In addition, current/voltage sensors need to have high bandwidth to be able to accurately measure the transient current/voltage. However, it is hard to obtain such sensors with the co-existing properties of high bandwidth, small size, and low price.
- **Current imbalance < 5%** — The quality of current sharing should be quantified instead of merely by observing. The current unbalance leads to switching loss difference between paralleled MOSFETs and results in unequal temperature distribution [55]. By approximating switching loss using piecewise linear model (which is not precise, but is convenient for approximation) [57], the mismatch of peak currents and the deviation in switching energies are around a similar value. Mismatch of peak currents below 5% of steady-state current is the goal of this dissertation. It also can be preferably a small number specified by the designer.
- **Single gate driver** — Different gate drivers potentially have different delay times, which also cause current mismatch during switching transients [58]. More functions are embedded into

the gate driver, especially for fast switching SiC MOSFET [59],[60]. Multiple gate drivers will increase the cost and volume of parallel structure.

- **Simple design guideline** — A design guideline is required for selection of current balancing components. The design guideline should be simple enough to reduce the design complexity and design cycle.
- **Simple implementation** — Complex digital computation module, delay time producing module and feedback loop module greatly increase the cost, volume, and difficulty in either implementation or integration. The power module has limited room available for extra circuit. Power density is also a concern when paralleling discrete MOSFETs. Complicated circuit structure should be avoided.
- **Both polarities of V_{th} mismatch** — Sorting threshold voltage for every die is time consuming for mass production. Normally, discrete MOSFETs or bare dies are randomly placed when been paralleled. The polarity of V_{th} mismatch is unknown. The balancing method should be able force good sharing in a bipolar way and work for both polarities of V_{th} mismatch. In other words, the balancing solution should be able to balance currents automatically.

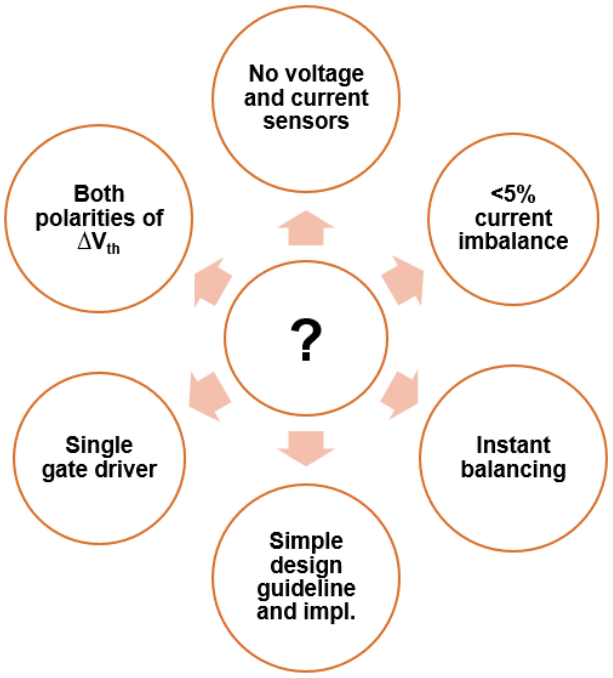


Fig. 1-8. Objectives of this research.

1.3 Existing Methods for Current Balancing

There are generally two kinds of method for compensation of current imbalance during switching transients. One is active compensation [35],[36],[39],[61]-[70]. For this method, current/voltage sensor for every device and feedback loop design are required to automatically modify the gate driving signals. The other one is passive compensation [71]. For this method, voltage/current sensors and feedback loop design are avoided. However, the automatic compensation becomes challenging. In this section, state of the art balancing solutions will be reviewed and compared according to the objectives listed in Fig. 1-8.

1.3.1 Active compensation

Active compensation is a popular method for balancing of switching transients, because it can automatically modify gate driving signals and work for both polarities of V_{th} mismatch.

One example is shown in Fig. 1-9 [67], where the imbalance information is extracted from the measured voltages across bond wires. According to this paper, voltage drops on bond wires will be different when current imbalance exists. Gate driving signals were shifted according to the delay time information extracted from the sensed voltages. Balanced currents were achieved after several cycles.

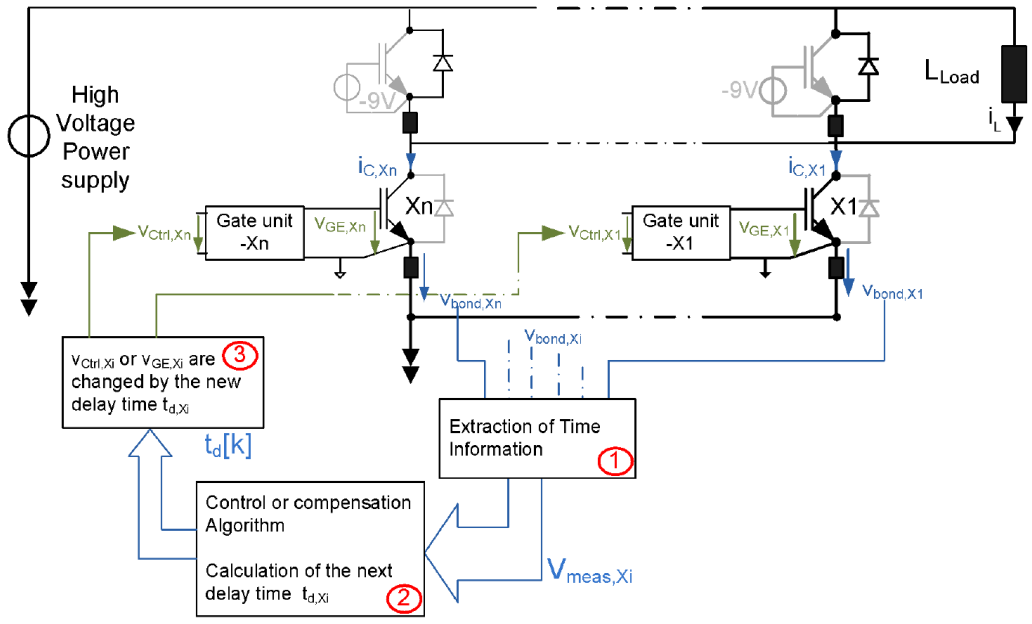


Fig. 1-9. Block diagram of the structure of automated delay time compensation for parallel connected IBGTs [67].

However, this method violates some of the objectives in Fig. 1-8. Firstly, this method needs voltage sensors. Wire bond is typically thin and short. Integration of voltage sensors is challenging. Secondly, multiple gate drivers are required to generate distinct delay times. Potential propagation delay between gate drivers will also cause current imbalance [72],[73]. Thirdly, the proposed compensation algorithm and feedback loop design are not easily integrated. A simple design

guideline is also hard to be derived. Furthermore, balancing was achieved by several steps/cycles to avoid over compensation, and the final unbalance was larger than 5% after multiple iterations.

Fig. 1-10 illustrates another example of active current balancing method for switching transients [35]. In this paper, current sensors instead of voltage sensors and analog feedback circuit instead of digital compensation algorithm are employed. Differential current transformer (CT) is utilized to measure the difference of currents. The feedback scheme is able to continuously adjust the delay time based on the sensed current difference. The peak currents are balanced after more than 10 cycles.

Similar to the previous method, this solution violates some of the objectives in Fig. 1-8. Firstly, this method needs a current sensor, which should have high bandwidth for accuracy. Secondly, multiple gate drivers are required to generate distinct delay times. Thirdly, the implementation and design guideline of this analog feedback loop design is complicated. Furthermore, this method cannot achieve balancing instantaneously. Desirable current sharing was achieved after several tens of switching cycles.

The currents in [39] were measured by Rogowski coils fabricated on a printed circuit board. The sensed rising/falling edges and peak values of the currents were fed to a FPGA and a DSP to adjust the gate driving signals, as shown in Fig. 1-11. A few cycles were required to balance the currents. Even though the current sensor has smaller size and less cost, multiple gate drivers and feedback loop design are still required. The response time is another concern.

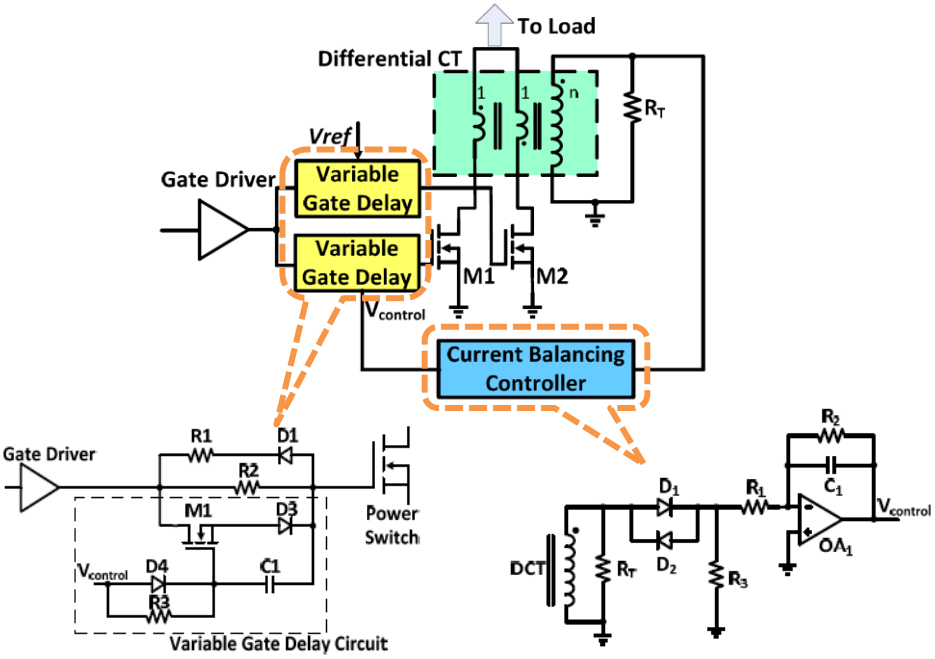
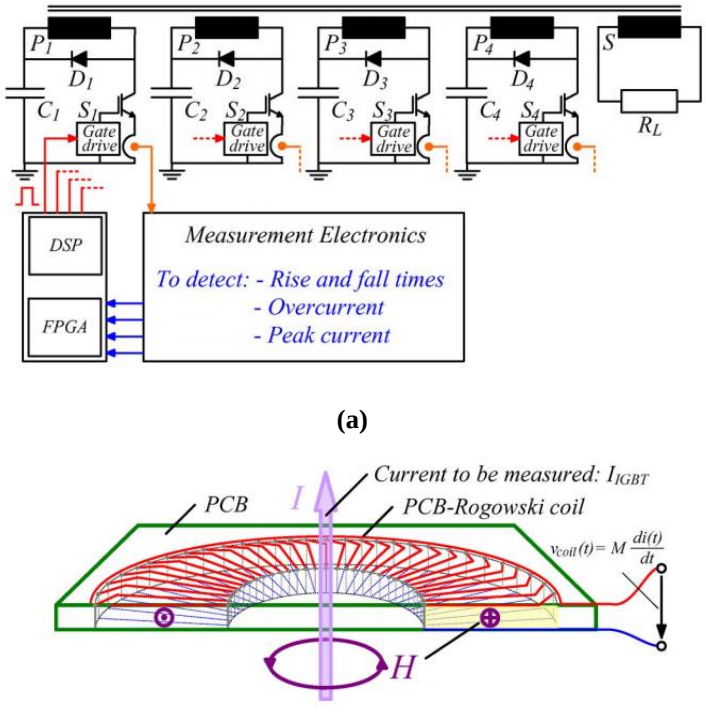


Fig. 1-10. Structure of active current balancing system in [35].



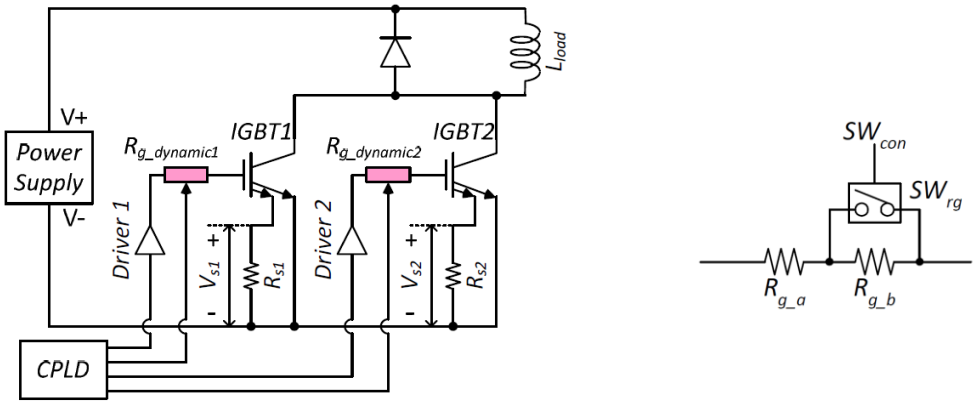
(a)

(b)

Fig. 1-11. (a) Schematic of active gate control, and (b) measuring principle with a PCB-Rogowski coil [39].

1.3.2 Passive compensation

Passive compensation is another way to balance currents during switching transients. One example is shown in Fig. 1-12 [71]. In this paper, a dynamic gate resistance is utilized to produce difference between delay times of parallel devices. According to Fig. 1-12(a), a dynamic gate resister ($R_{g\_dynamic}$) is added for every device. The topology of $R_{g\_dynamic}$ is shown in Fig. 1-12(b). It consists of two series connected resistance (R_{g_a} and R_{g_b}), one analog switching (SW_{rg}), and one digital control signal (SW_{con}). By turning SW_{rg} on and off, the equivalent gate resistance can be varied between R_{g_a} and (R_{g_a} + R_{g_b}). In other words, $R_{g\_dynamic}$ is a two-level resistor.



(a) **(b)**

Fig. 1-12. (a) Structure of dynamic gate resistance control; (b) topology of dynamic gate resistance [71].

The solution described in [71] can balance peak currents instantly at the expense of losing automatic compensation. Dynamic gate resistor $R_{g\_dynamic}$ can be controlled to increase or decrease the switching speed. However, the polarity and magnitude of V_{th} mismatch need to be known to determine the value of it. Two-level resistance is only suitable for one case. Another set of values is required when the severity of unbalance is changed. This method also requires multiple gate drivers and two extra control signals for every dynamic gate resistor. Furthermore, the final

balancing was not perfect because the design guideline for selection of passive components was not provided

The characteristics of state of the art dynamic current balancing solutions are summarized in Table 1-1.

Table 1-1. Summary of state of the art balancing methods

	Active compensation	Passive compensation
Instant balancing	×	✓
No voltage and current sensors	×	✓
Current imbalance <5%	×	×
Single gate driver	×	×
Simple design guideline and implementation	×	×
Both polarities of V_{th} mismatch	✓	×

1.4 Contributions of This Dissertation

The objective of this dissertation is to propose dynamic balancing solutions that can balance currents during switching transients without greatly increase the complexity, volume, and price of the original parallel structure. The aforementioned benefits can most probably be realized by passive balancing method according to the literature review in the previous section. Parasitic inductances are inevitable among paralleled switches. Their impact on dynamic current unbalance induced by V_{th} mismatch is investigated to identify the beneficial ones.

Fig. 1-13 illustrates the schematic of a Double-Pulse Tester (DPT) for testing of switching transients. The focal point is the paralleled M1 and M2 with $V_{th1} \neq V_{th2}$. The board and package inductances are assumed symmetric to exclude the unbalance caused by layout. The inductances on the same trace are lumped together and categorized as seven types in

This dissertation also models the switching energy and switching energy mismatch of paralleled MOSFETs. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs. The accuracy of the proposed model is experimentally verified over wide operating range. The influence of current balancing components and magnitude of threshold voltage mismatch on sharing are discussed based on modeling results.

Table 1-2. Inductances have current/power balancing capabilities are figured out through parametric analysis. They are common-source inductance (L_{cm}), power-source inductance (L_s), and drive-source inductance (L_k). Through the analysis of balancing mechanism, the drive-source resistance (R_k) and magnetic coupling between inductors are also found to be beneficial. Several passive balancing solutions are synthesized employing those passive components. All of them can satisfy the objectives in Fig. 1-8 as shown in Fig. 1-14.

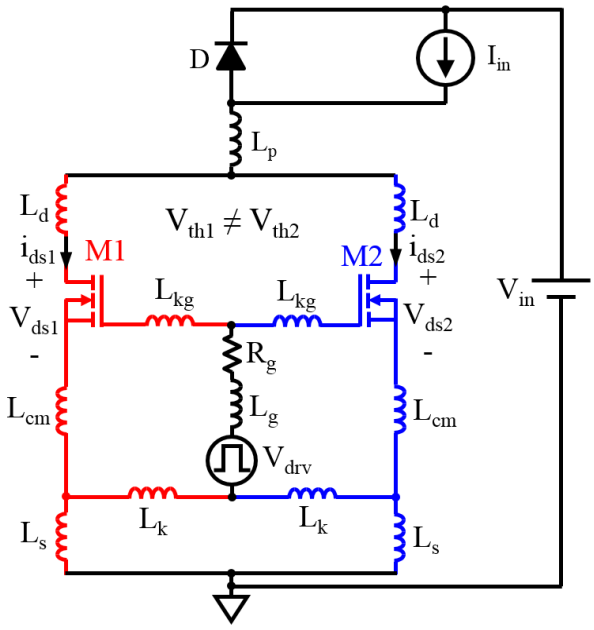


Fig. 1-13. Schematic of double-pulse tester with paralleled SiC MOSFETs.

This dissertation also models the switching energy and switching energy mismatch of paralleled MOSFETs. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs. The accuracy of the proposed model is experimentally verified over wide operating range. The influence of current balancing components and magnitude of threshold voltage mismatch on sharing are discussed based on modeling results.

Table 1-2. Parasitic inductances considered in Fig. 1-13

Symbol	Name
L_d	Drain inductance
L_s	Power-source inductance
L_p	Power-loop inductance
L_{cm}	Common-source inductance
L_{kg}	Drive-gate inductance
L_k	Drive-source inductance
L_g	Gate-drive inductance

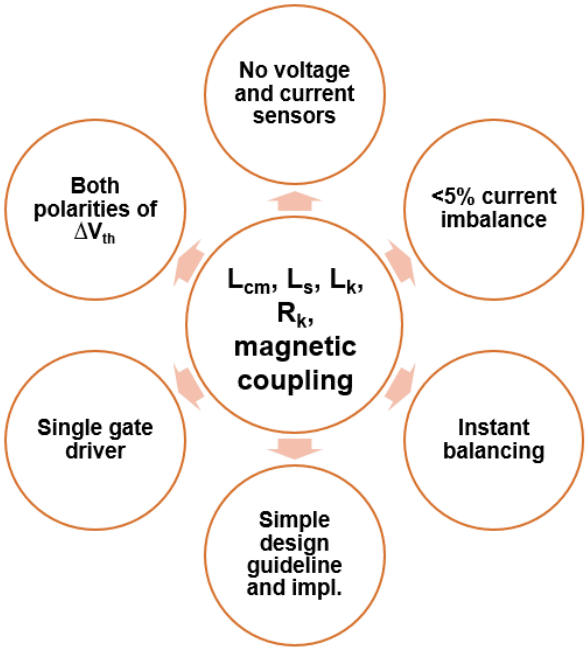


Fig. 1-14. Contribution of this dissertation.

In summary, the main contributions of this dissertation are:

- Transient currents between paralleled SiC MOSFETs are automatically balanced by inductance, resistance, and magnetic coupling using one gate driver, no sensors, and no feedback. Passive balancing solutions work for both polarities of V_{th} mismatch and force balancing from the first current peak.
- Design guidelines involving the magnitude of V_{th} mismatch, current rise time, and maximum peak-current difference are derived to guide the choice of passive components. The detail design procedures are recommended to force currents to share over wide operating range.
- Analytical model for switching energy and switching energy mismatch of paralleled MOSFETs are provided. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs without losing accuracy.

1.5 Dissertation Outline

This dissertation explores passive solutions to balance switching transients between paralleled SiC MOSFETs. The proposed dissertation outline is:

Chapter 1 Introduction

1.1 Background

1.2 Research Motivations and Objectives

1.3 Existing Methods for Current Balancing

1.4 Contributions of This Dissertation

1.5 Dissertation Outline

Chapter 2 Passive Balancing Solutions for Paralleling of Bare Dies

Nomenclature

V_{th}	Threshold voltage
L_d	Drain inductance
L_s	Power-source inductance
L_p	Power-loop inductance
L_{cm}	Common-source inductance
L_{kg}	Drive-gate inductance
L_k	Drive-source inductance
L_g	Gate-drive inductance
g_{fs}	Large signal transconductance
V_{in}	Input voltage of double-pulse tester
I_{in}	Input current of double-pulse tester
R_g	Gate resistor of double-pulse tester
i_{ds}	Channel current of MOSFET
v_{ds}	Drain-source voltage of MOSFET
v_{gs}	Gate-source voltage of MOSFET
i_{kg}	Gate charging current of MOSFET
E_{sw}	Switching energy
I_{pk}	Peak channel current
V_{pk}	Peak drain-source voltage

M Mutual inductance

2.1 Introduction

The state-of-art solutions balance transient currents by two categories of "active" compensation. One is with feedback loop and current/voltage sensors. The currents in [39] are measured by Rogowski coils fabricated on a printed circuit board. The sensed rising/falling edges and peak values of the currents are fed to a FPGA and a DSP to adjust the gate driving signals. A few cycles are required to balance the currents. The imbalance information in [67] is extracted from the measured voltages across the stray inductances. The feedback compensation varies the delay time of gate signals. Balanced currents are achieved after several cycles. The difference of currents is measured by a differential current transformer in [35]. The feedback scheme can continuously adjust the delay time based on the sensed current difference. The peak currents are balanced after more than 10 cycles. The other category of active compensation is without feedback loop. The two-level dynamic gate resistances indirectly control the delay time between gate drivers [71]. The peak currents can be balanced in one switching cycle. The asymmetry of threshold voltages needs to be known due to the loss of automatic compensation.

The objective of this chapter is to automatically limit the mismatch of peak currents in one switching cycle and by one gate driver without using current/voltage sensors and feedback loop. As the first step, the "parasitic" inductors most effective in improving current sharing are identified by parametric analysis. They are common-source inductance (L_{cm}), power-source inductance (L_s) and drive-source inductance (L_k). Then, findings in the previous parametric analysis are employed to synthesize several passive balancing topologies. The principle of forcing sharing is explained for each structure. Their respective design guidelines are also suggested for component selection.

Next, a passive balancing solution that utilizes drive-source resistors (R_k) and power-source inductors (L_s) is derived based on previous topologies. The effectiveness of all the aforementioned passive balancing techniques is verified by a prototype that, indeed, includes significant layout inductances in order to demonstrate the robustness. Finally, all the balancing structures are comprehensively compared, considering total switching energy, switching energy difference, peak-current difference, and voltage stress.

2.2 Parametric Analysis of Parasitic Inductances

Parasitic inductances are inevitable among paralleled switches. The question is whether those inductances will or will not influence imbalance. The impact of parasitic inductances on dynamic current unbalance induced by V_{th} mismatch is investigated in this section to identify the beneficial ones. Their influences on switching energy and voltage stress are also summarized for comprehensiveness.

Fig. 2-1 illustrates the schematic of a Double-Pulse Tester (DPT) for testing of switching transients. The focal point is the paralleled M1 and M2 with $V_{th1} \neq V_{th2}$. The layout and/or package inductances are assumed symmetric to exclude the unbalance caused by layout. The inductances on the same trace are lumped together and categorized as seven types in

This dissertation also models the switching energy and switching energy mismatch of paralleled MOSFETs. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs. The accuracy of the proposed model is experimentally verified over wide operating range. The influence of current balancing components and magnitude of threshold voltage mismatch on sharing are discussed based on modeling results.

Table 1-2. The inductive load is represented by I_{in}. The gate driver gives two short pulses. The turn-off and turn-on transients are captured at the end of the first pulse and the beginning of the second pulse, respectively.

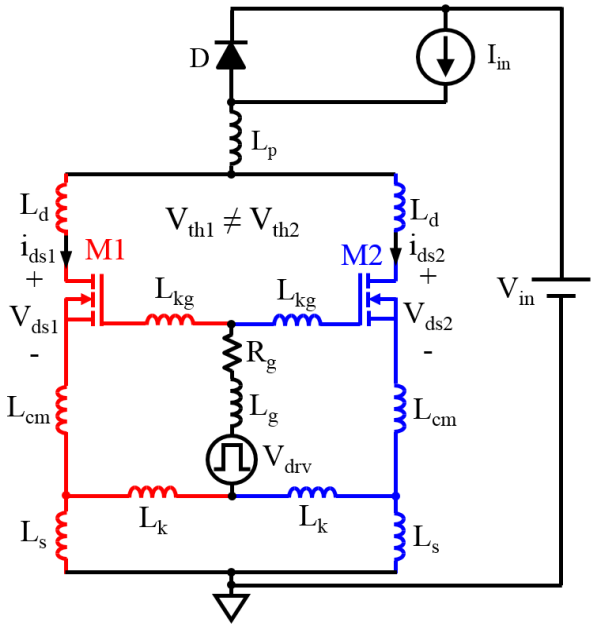


Fig. 2-1. Schematic of double-pulse tester with paralleled SiC MOSFETs.

Fig. 2-2 shows the procedure of parametric analysis. The parameters used in simulation are listed beside the corresponding steps. Measured worst-case mismatch of 2.48 V and 3.08 V in [24] were assigned to the paralleled MOSFETs. Operating conditions were V_{in} = 600 V, I_{in} = 20 A, and R_g = 10 Ω. The nominal inductance was 5 nH (instead of 0 nH) to account for the interaction among the seven inductances. Each inductance was swept in turn from 0 nH to 20 nH while the others were fixed at the nominal value. Switching loss (E_{sw}), peak drain-source current (I_{pk}), and peak drain-source voltage (V_{pk}) were recorded and post-processed to extract total switching loss, peak-current mismatch, and voltage stress. The normalized data are summarized in Fig. 2-3.

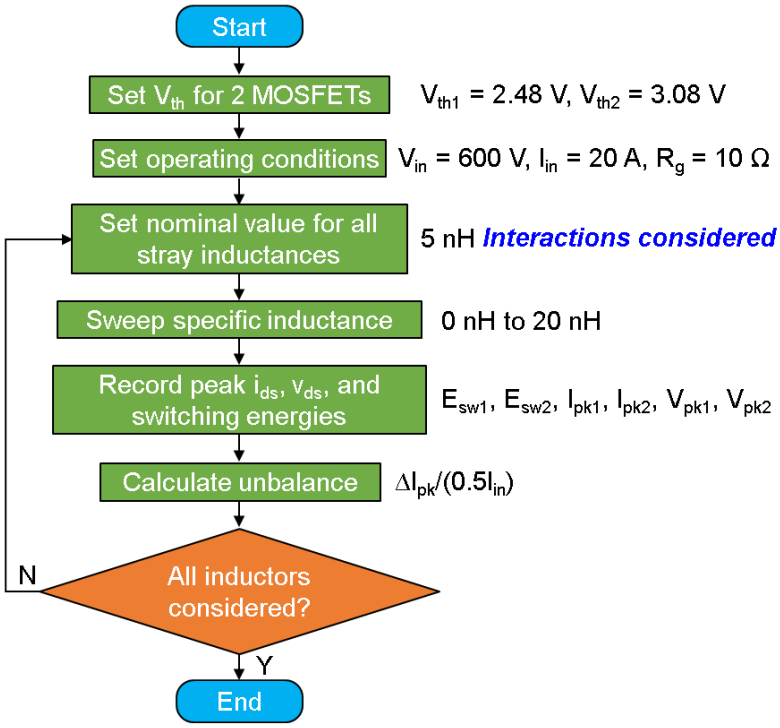


Fig. 2-2. Flow chart of parametric analysis to evaluate the influence of parasitic inductances on current sharing, voltage stress, and switching loss.

Simulations are performed at certain operating conditions, which are V_{in} = 600 V, I_{in} = 20 A, R_g = 10 Ω. In the simulations, inductances are swept from 0 nH to 20 nH to cover wide range. However, unit inductance has distinctive influence under different operating conditions. The base (L_{base}) for inductance normalization was identified from observations and the analyses in [74]-[76] to normalize the operating conditions. Voltage spike during turn-off transient increased with higher I_{in}. The voltage drops across inductors reduced with larger R_g thanks to slower switching speed. The over-voltage stress percentage was lessened by higher V_{in}. Lower quality factor (or higher damping) for the series resonant tank formed by the inductances and C_{oss} was resulted from larger output capacitance C_{oss}. Overall, the influence of the parasitic inductances was enhanced by higher input current and weakened by larger gate resistance, input voltage, and output capacitance. Thus,

the inductance is normalized to

$$L_{base} = \frac{C_{oss} R_g V_{in}}{I_{in}} = 14.1\,\text{nH} \tag{2-1}$$

where C_{oss} is from the C2M0160120D datasheet [33]. The normalized results under different operating conditions will be similar to Fig. 2-3 (with small variation) while following the procedure illustrated in Fig. 2-2 and correspondingly changing the nominal inductance and sweeping range base on (2-1).

The base inductance in (2-1) was derived from the performance of inductances on power commutation loop (L_p, L_d, and L_s). Because 0 to 1.2 normalized inductance (corresponding to 0 nH to 17 nH) covers the value that is typically created by gate loop, the same base was applied to gate-loop inductance (L_g, L_{kg}, and L_k) and common-source inductance (L_{cm}) for convenience. The L_{cm} inside some discrete MOSFETs is only approximately half of that range, but the trend of its influence is still clearly shown.

The peak-current mismatch in Fig. 2-3(a) is defined as

$$\text{current mismatch} = \frac{I_{pk1} - I_{pk2}}{I_{ss}} \times 100\% \tag{2-2}$$

where I_{pk1} and I_{pk2} are the peak currents of M1 and M2, respectively, and $I_{ss} = I_{in}/2$. Unbalance is reduced notably by L_{cm}, L_k, and L_s, and is mildly affected by the other inductances according to Fig. 2-3(a). Even though L_d seems equivalent to L_s in circuit point of view, inductance L_d is decoupled to gate and source terminals by C_{gd} and C_{ds}. The difference of their voltage drops can barely bias gate charging speed. The mismatch of gate currents is much smaller compared to drain-source currents and is normally trivial. The influence of L_{kg} is also negligible. Inductances L_{cm}, L_s,

and L_k are connected to source terminal. They are responsive to the difference between i_{ds1} and i_{ds2}. Even through most of the channel currents flow through the power commutation loop, inductances L_s and L_k are in parallel in differential point of view. If the common part of the currents in both branches is neglected and only the flowing of current difference is considered, part of the current difference will circulate in the loop formed by L_d, L_{cm}, and L_k and the remaining part will circulate in the loop formed by L_d, L_{cm}, and L_s. Voltage drops on the two L_k or two L_s will be different and bias the internal gate-source voltages. That is why L_k and L_s can help balance drain-source currents of paralleled MOSFETs.

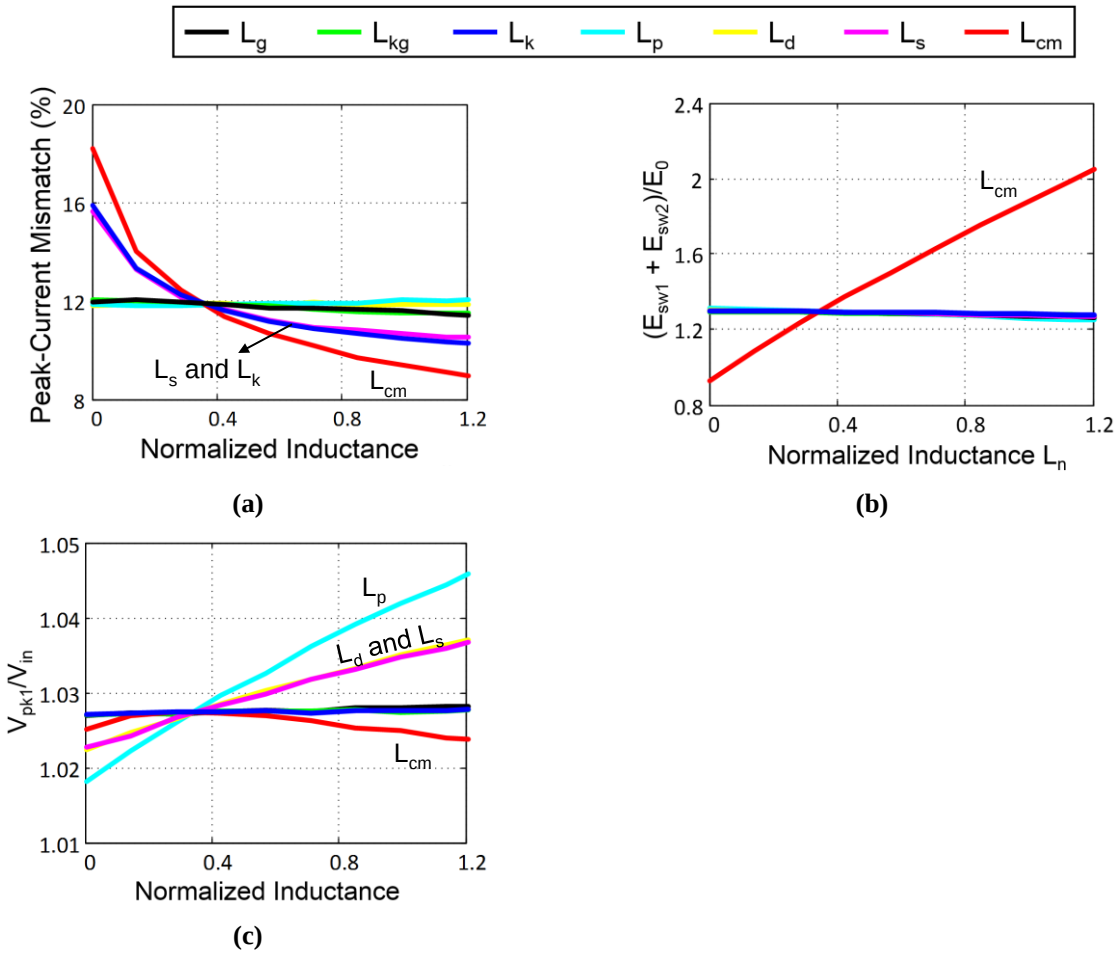


Fig. 2-3. Simulation results of Fig. 2-1 following Fig. 2-2 with SPICE models of MOSFETs (C2M0160120D) and Schottky diode (CPW51200Z050B) from Cree: (a) Peak-current mismatch, (b) switching loss, and (c) voltage stress of M1 versus inductance normalized to (2-1).

Fig. 2-3(b) shows the influence of inductances on normalized total switching energy, where E_{sw1} and E_{sw2} are the switching energies (including turn-on energy and turn-off energy) of M1 and M2, respectively; E_o is the total switching energy obtained when all inductances equal zero. Only L_{cm} increases switching loss dramatically as reported in [77] since it is a common inductance of gate loop and power loop and slows down the gate charging speed as shown in Fig. 2-4. During turn-on transient, a positive voltage drop on common-source inductance is induced by the positive current slew rate. This voltage drop will slow down the gate charging speed as L_{cm} is also on the gate charging path. Vice versa for turn-off transient. As a result, common-source inductance is better to be minimized to avoid extra loss.

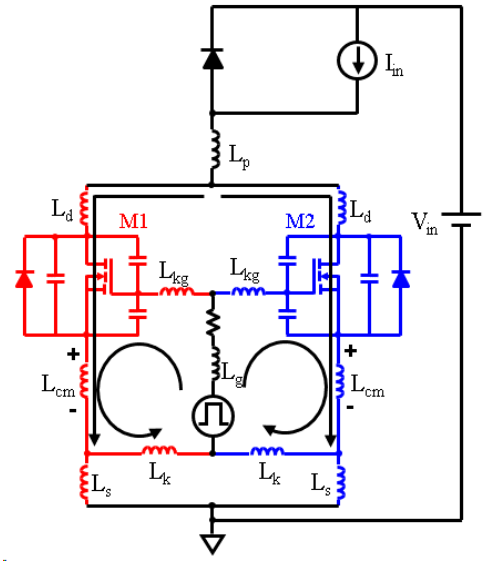


Fig. 2-4. Influence of L_{cm} on slowing down switching speed during turn-on transient.

Fig. 2-3(c) illustrates the influence of inductances on normalized voltage stress, where V_{pk1} is the peak of drain-source voltage of M1. (The voltage stress of M2 is similar.) According to the results, voltage stress is hardly affected by L_k, L_g, and L_{kg}. It increases with L_d, L_s, and L_p because

the negative voltages on those inductors add to V_{in} during turn-off transient. Inductance L_{cm} also lies on the power commutation loop. However, L_{cm} slows down switching speed, thus its corresponding trend is non-monotonic. Large L_{cm} might be beneficial for voltage stress.

A summary for the influences of parasitic inductances on total switching energy, voltage stress, and peak-current difference is shown in Table 2-1. The drive-source inductors L_k balance the currents without increasing switching loss and voltage stress. The power-source inductors L_s balance the currents, but also add voltage stress. The common-source inductance L_{cm} will not be increased intentionally (although it helps current balancing) because it greatly increases the switching loss.

Table 2-1. Summary of layout influences shown in Fig. 2-3

	L_d	L_s	L_p	L_{cm}	L_{kg}	L_k	L_g
Total switching energy $E_{sw1} + E_{sw2}$	-	-	-	↑	-	-	-
Voltage stress V_{ds}	↑	↑	↑	↓	-	-	-
Peak-current difference Δi_{pk}	-	↓	-	↓	-	↓	-

↑ denotes increase

↓ denotes decrease

- denotes no influence

2.3 Current Balancing Effects of Common-, Drive-, and Power-source Inductances

The inductances that can mitigate current imbalance have been figured out in the previous section. This section will provide a more sophisticated analysis in circuit point of view. The design guidelines involving the magnitude of V_{th} mismatch, current rise time, and unbalance percentage will be derived for the selectin of passive components. Because L_p, L_d, L_g, and L_{kg} have slight

impact on current, they are not included in the analysis for simplicity. The theory upholds well when parasitics are considered as shown in the later experimental verification, which has substantial parasitics from device package and copper traces.

The balancing structure with common-source inductances is depicted in Fig. 2-5. The DPT (double-pulse tester) is used for the testing of switching transients. The lower side is composed of two SiC MOSFETs with mismatched V_{th}, where V_{th1} and V_{th2} are threshold voltages of M1 and M2, respectively. Voltage v_{gs} is the internal gate-source voltage of MOSFET. Voltage V_{cm} is the voltage drop on common-source inductance. The upper side is a SiC Schottky Barrier Diode (SBD). The inductive load is modeled by a constant current source for simplicity.

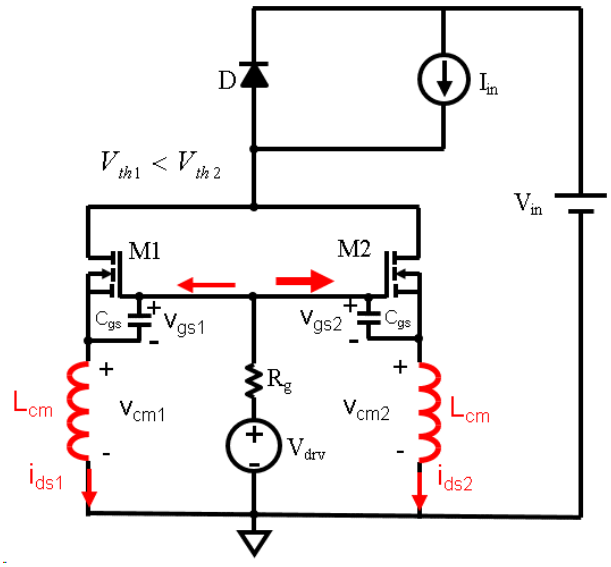


Fig. 2-5. Influence of Common-source inductance on biasing gate charging speed and improving dynamic sharing, as indicated by (2-10).

Because the channel current i_{ds} is much larger than the currents bypassed through parasitic capacitances during i_{ds} rising period [77], current flowing through the common-source inductance is approximated by i_{ds}, which can be modeled by a parabolic equation during saturation region:

$$i_{ds_j} = g_{fs}\left(v_{gs_j} - V_{th_j}\right)^2, v_{gs_j} > V_{th_j}, j = 1,2 \tag{2-3}$$

where V_{th1} and V_{th2} are the threshold voltages of M1 and M2, respectively. The large-signal transconductance g_{fs} is assumed to match for both MOSFETs [49].

If common-source inductances in Fig. 2-5 were removed, two gate-source capacitors would be in parallel. Voltages v_{gs1} and v_{gs2} are equal and can be expressed as

$$v_{gs1} = v_{gs2} = v_{gs} = V_{drv}\left[1 - e^{-\frac{t}{2C_{gs}R_g}}\right] \tag{2-4}$$

With the same v_{gs}, the MOSFET with smaller V_{th} carries larger current according to (2-3) and as illustrated in Fig. 2-6(a). The difference of drain-source currents can be obtained by differentiating (2-3):

$$\Delta i_{ds} = 2g_{fs}\left(v_{gs} - V_{th}\right)\left(\Delta v_{gs} - \Delta V_{th}\right), \quad v_{gs} > V_{th} \tag{2-5}$$

where

$$\Delta x = x_1 - x_2, \; x = 0.5\left(x_1 + x_2\right) \tag{2-6}$$

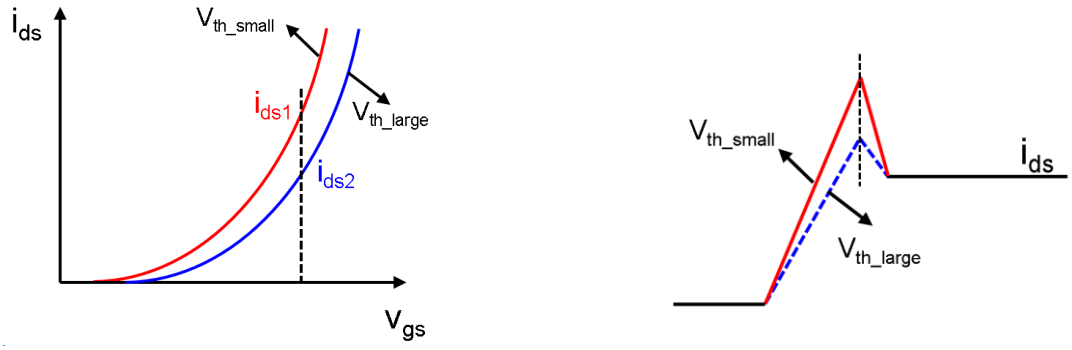
Equation (2-5) shows that the difference of drain-source currents is zero when

$$\Delta v_{gs} = \Delta V_{th} \tag{2-7}$$

By taking the derivative of (2-3), the current slew rates of both branches are given as

$$\frac{di_{ds_j}}{dt} = 2g_{fs}\frac{dv_{gs}}{dt}\left(v_{gs} - V_{th_j}\right) \tag{2-8}$$

According to above equation, the MOSFET with smaller threshold voltage also has a higher current slew rate, as shown in Fig. 2-6(b).



(a) **(b)**

Fig. 2-6. (a) Transfer characteristics of two MOSFETs with different threshold voltages. The dashed line indicates the currents of two MOSFETs when $v_{gs1} = v_{gs2}$. (b) Turn-on transient currents of two MOSFETs with mismatched threshold voltages.

When common-source inductances are inserted, the voltage drop V_{cm} for the MOSFET with smaller V_{th} will be larger:

$$V_{cm1} = L_{cm}\frac{di_{ds1}}{dt} > V_{cm2} = L_{cm}\frac{di_{ds2}}{dt} \tag{2-9}$$

If viewing V_{cm} as an effective voltage source, gate drive voltage V_{drv} in (2-4) should be replaced by (V_{drv} - V_{cm}) as

$$v_{gs_j} = \left(V_{drv} - V_{cm_j}\right)\left[1 - e^{-\frac{t}{2C_{gs}R_g}}\right] \tag{2-10}$$

Thus, the gate charging speed of M1 (which has a smaller V_{th}) is slower than that of M2 resulting in a smaller gate-source voltage. The difference of v_{gs1} and v_{gs2} can be obtained by Fig. 2-5 as

$$\Delta v_{gs} = -L_{cm} \frac{d\Delta i_{ds}}{dt} \tag{2-11}$$

Current imbalance during switching transient can be completely compensated if this v_{gs} difference equals V_{th} mismatch, as shown in Fig. 2-7

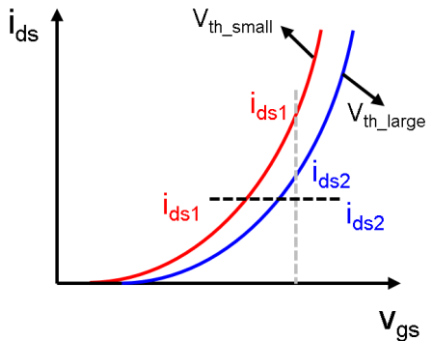


Fig. 2-7. Comparison of drain-source currents of two MOSFETs when $v_{gs1} = v_{gs2}$ (grey dashed line) and when L_{cm} is inserted, and balance is achieved (black dashed line).

The expression of Δi_{ds} is derived in (2-5). Substitution of $d\Delta i_{ds}/dt$ from (2-5) into (2-11) yields

$$\frac{d\Delta v_{gs}(t)}{dt} = \frac{2g_{fs}\frac{dv_{gs}(t)}{dt}\Delta V_{th} - \left(2g_{fs}\frac{dv_{gs}(t)}{dt} + \frac{1}{L_{cm}}\right)\Delta v_{gs}(t)}{2g_{fs}\left(v_{gs}(t) - V_{th}\right)}, v_{gs}(t) > V_{th} \tag{2-12}$$

The initial value of Δv_{gs} in (2-12) is zero as the gate driver charges the gate-source capacitances of M1 and M2 equally before the channels of MOSFETs turned on. Thus, the slew rate of Δv_{gs} is larger than zero when $\Delta V_{th} > 0$ and smaller than zero when $\Delta V_{th} < 0$. The maximum value of $\Delta v_{gs}(t)$ is achieved when the numerator of (2-12) reaches zero and is expressed as

$$\Delta v_{gsMax} = \lim_{d\Delta v_{gs}/dt \to 0} \Delta v_{gs} = \frac{1}{1 + \left(2g_{fs} \frac{dv_{gs}}{dt} \times L_{cm} \right)^{-1}} \Delta V_{th} \tag{2-13}$$

The voltage Δv_{gsMax} can be approximated by ΔV_{th} when $2g_{fs}L_{cm}\, dv_{gs}/dt >> 1$. The larger the L_{cm}, the better the balance effect.

According to (2-13), $|\Delta v_{gs}| \le |\Delta V_{th}|$. The maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ can be obtained by (2-11):

$$\max \left| i_{ds1(pk)} - i_{ds2(pk)} \right| = \frac{|\Delta V_{th}|}{L_{cm}} t_r \tag{2-14}$$

where t_r is the time for current rising from 0 to the peak, as illustrated in Fig. 2-8. The numerical model of t_r as a function of parasitic inductances and operating conditions is derived in Appendix A.

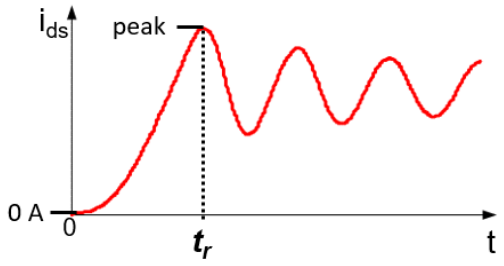


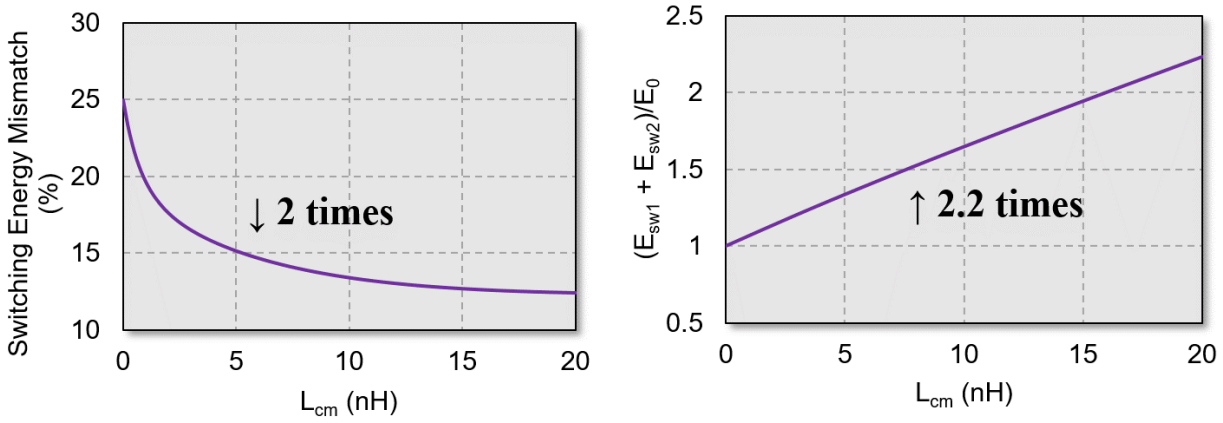
Fig. 2-8. Definition of t_r in (2-14).

Even though L_{cm} can balance transient currents by producing difference in gate-source voltages, the absolute gate-source voltages are reduced compared to the case without L_{cm} (as indicated by the dark line in Fig. 2-7). The general switching speed is slowed down and total

switching energy is increased. Fig. 2-9 Shows the simulation results of Fig. 2-5 with varying L_{cm}. The switching energy mismatch percentage is defined as

$$\text{Switching energy mismatch percentage} = \frac{E_{sw1} - E_{sw2}}{0.5(E_{sw1} + E_{sw2})} \times 100\% \tag{2-15}$$

According to the plots, switching energy mismatch is reduced by 2 times. However, total switching loss is increased by 2.2 times due to the slowed down switching speed (as demonstrated in (2-10)). To sum up, common-source inductance is effective in dynamic balancing, but at the expense of higher switching loss. Thus, common-source inductance is not preferred in real design.

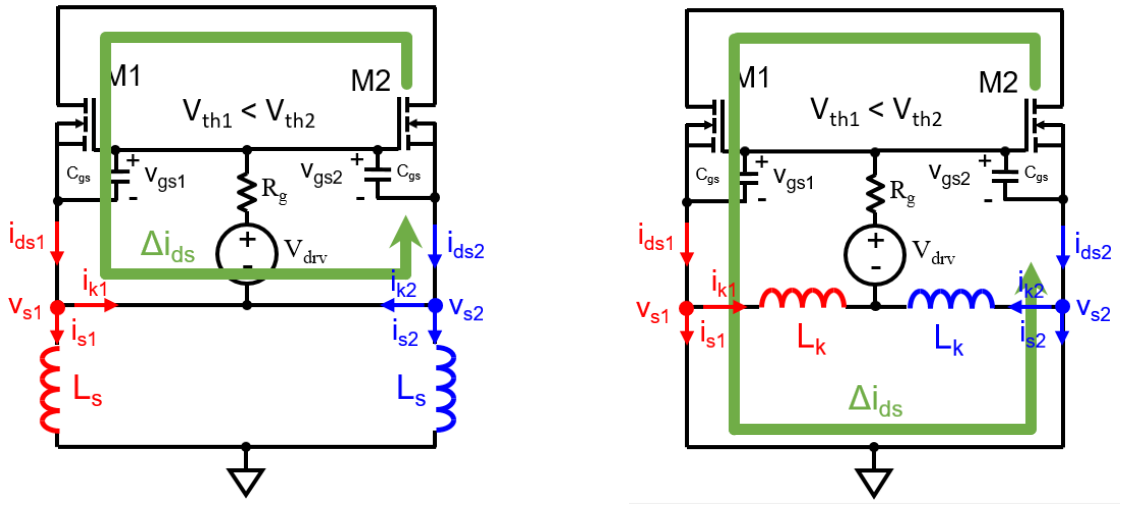


(a) **(b)**

Fig. 2-9. (a) Influence of L_{cm} on switching energy mismatch; (b) influence of L_{cm} on total switching loss. All the other inductances are set as 0 nH.

Except for L_{cm}, power-source inductance L_s and drive-source inductance L_k are also effective in current balancing, as illustrated by the parametric analysis shown in Fig. 2-3 and Table 2-1. Paralleling of two MOSFETs with L_s, and without L_{cm} and L_k, is shown in Fig. 2-10(a), where the threshold voltage of M1 is smaller than that of M2. For the structure shown in Fig. 2-10(a), two gate-source capacitors are directly paralleled even with L_s inserted. MOSFET M1 (which has a

smaller V_{th}) carries higher current than M2 according to Fig. 2-7. The impedance in power-source trance is much larger than drive-source trace due to the implementation of L_s. Current difference Δi_{ds} will circulate though drive-source paths (as indicated by the green arrow in Fig. 2-10(a)). Paralleling of two MOSFETs with L_k, and without L_{cm} and L_s, is shown in Fig. 2-10(b). Similar to Fig. 2-10(a), two gate-source capacitors are also directly paralleled even with L_k inserted. Mismatch in drain-source currents still exist and will circulate through power-source path.



(a) **(b)**

Fig. 2-10. (a) Paralleling of two MOSFETs with L_s and without L_{cm} and L_k. (b) Paralleling of two MOSFETs with L_k and without L_s and L_{cm}. The threshold voltage of M1 is smaller than that of M_2. The green arrows indicate the flow direction of drain-source current difference.

According to the above analysis, structure only with L_s or only with L_k is not an effective balancing solution. The parametric analysis in section 2.2 sets nominal inductance as 5 nH, instead of 0 nH, to account for the interaction among inductances. Power-source and drive-source inductances should be implemented simultaneously to be able to reduce the current mismatch in both power-source and drive-source branches. Structure with both L_s and L_k is shown in Fig. 2-11.

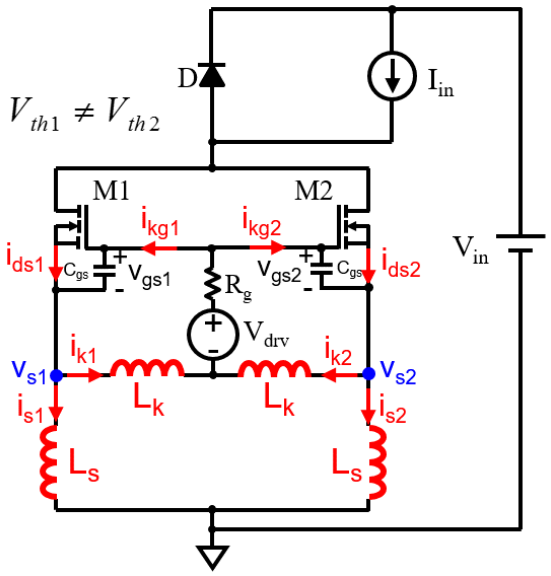


Fig. 2-11. Balancing effect of power-source and drive-source inductances during turn-on transient with mismatch in threshold voltages.

According to Fig. 2-6, lower V_{th} leads to higher current share and current slew rate. Voltages at V_{s1} and V_{s2} will be different when L_s and L_k are inserted. Similar to L_{cm}, MOSFET with lower threshold voltage will have higher potential at source terminal leading to a smaller gate-source voltage. Current imbalance during switching transient can be completely compensated if this v_{gs} difference equals V_{th} mismatch. To solve for the explicit expression of Δv_{gs}, KVL and KCL of Fig. 2-11 are constructed:

$$\begin{cases} \Delta v_{gs} = -L_s \dfrac{d\Delta i_s}{dt} \\ \Delta v_{gs} = -L_k \dfrac{d\Delta i_k}{dt} \\ \Delta i_{ds} \approx \Delta i_s + \Delta i_k \end{cases} \tag{2-16}$$

where Δ indicates the difference of two terms as defined in (2-6). Current i_s and i_k are currents flowing through power-source inductances and drive-source inductances, respectively. The

currents of C_{gs} and C_{ds} are approximated to be zero during i_{ds} rising interval to simplify the analysis [77].

Solving (2-16),

$$\Delta v_{gs} = -\frac{L_s L_k}{L_s + L_k}\frac{d\Delta i_{ds}}{dt} \tag{2-17}$$

where Δi_{ds} was derived in (2-6) and is repeated here for convenience:

$$\Delta i_{ds} = 2g_{fs}\left(v_{gs} - V_{th}\right)\left(\Delta v_{gs} - \Delta V_{th}\right), \quad v_{gs} > V_{th} \tag{2-18}$$

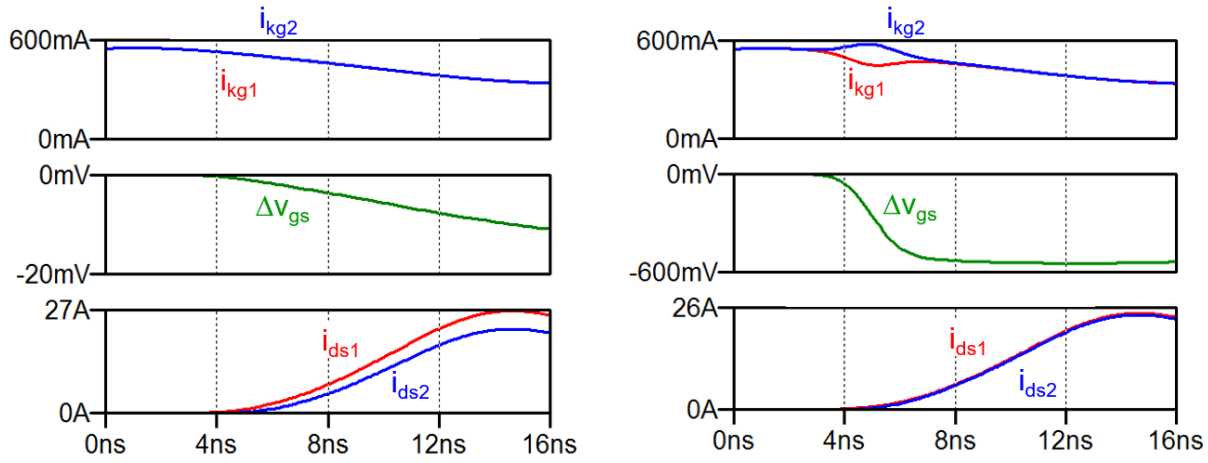
According to Fig. 2-6 and (2-17),

$$\Delta V_{th} < 0 \Rightarrow \frac{d\Delta i_{ds}}{dt} > 0 \Rightarrow \Delta v_{gs} < 0 \tag{2-19}$$

MOSFET with a smaller V_{th} has a smaller gate-source voltage, which means the mismatch in i_{ds} can be forced balanced. In addition, the coefficient of (2-17) is equal to the parallel inductance of L_s and L_k. If either of them is zero, there will be no balancing effect. Another way to interpret the parallel relationship between L_s and L_k is to analyze the circuit in differential point of view. Disregarding the common mode information, joints of two L_k and two L_s can be considered as shorted. Kelvin-source and power-source inductances are effectively paralleled in differential point of view.

Simulation results of Fig. 2-11 with and without L_k are shown in Fig. 2-12. When L_k = 0 nH, two gate-source capacitors are directly paralleled. Gate charging current i_{kg1} and i_{kg2} of M1 and M2 are equal, as shown in Fig. 2-12(a). MOSFET M1 (which has a smaller V_{th}) carries higher current than M2 because the difference of v_{gs} is negligible (as indicated by (2-17)). Both L_k and L_s

are inserted in Fig. 2-12(b). The voltage drops on L_s//L_k forces i_{kg1} to be smaller than i_{kg2} at the beginning of turn-on transient. Difference in gate-source voltages is built quickly to compensate threshold mismatch. The current unbalance in Fig. 2-12(a) is almost eliminated for the whole turn-on process.

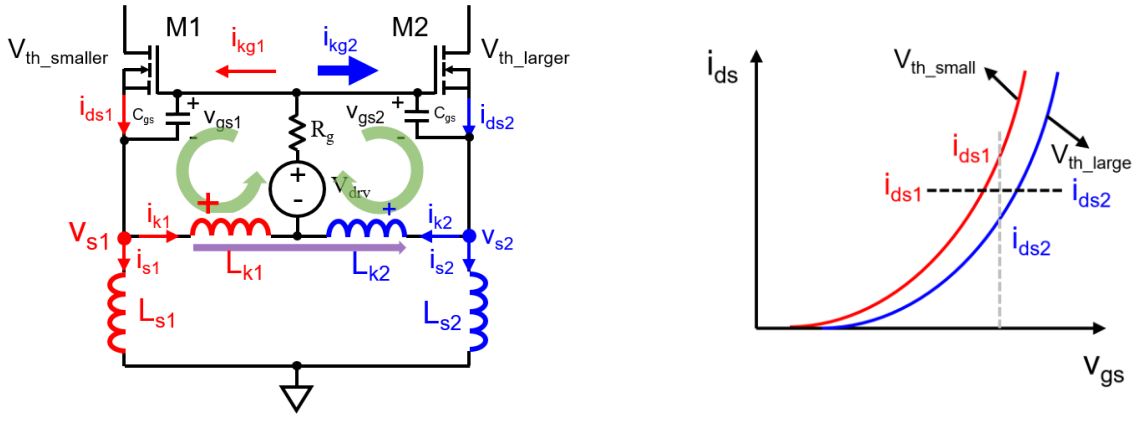


(a) **(b)**

Fig. 2-12. Simulation results of Fig. 2-11 (a) with L_k = 0 nH and L_s = 40 nH ; (b)) with L_k = 40 nH and L_s = 40 nH. The threshold voltages of M1 and M2 are 2.48 V and 3.08 V, respectively.

Unlike common-source inductance, neither L_s nor L_{ks} is shared by power loop and gate loop. Fig. 2-13(a) shows the flow of gate-driving currents in drive-source branches, where green arrow and purple arrow indicate the flow direction of common mode current and differential mode current, respectively. Inductance L_k//L_s creates voltage difference at V_{s1} and V_{s2} when mismatch in threshold voltages exists. This voltage difference forces current flowing from V_{s1} to V_{s2} through two drive-source inductors. For the situation shown in Fig. 2-13(a), current i_{k1} is increased and voltage drop on L_{k1} becomes larger. On the other hand, i_{k2} is decreased, which reduces the voltage drop on L_{k2}. Two gate-source voltages are bias without influencing the general switching speed. The Comparison of transfer curves between without balancing solution and with inserted L_s//L_k is

shown in Fig. 2-13(b), where grey line is when $v_{gs1} = v_{gs2}$ and black line is when L_s and L_k are inserted, and balance is achieved.



(a) **(b)**

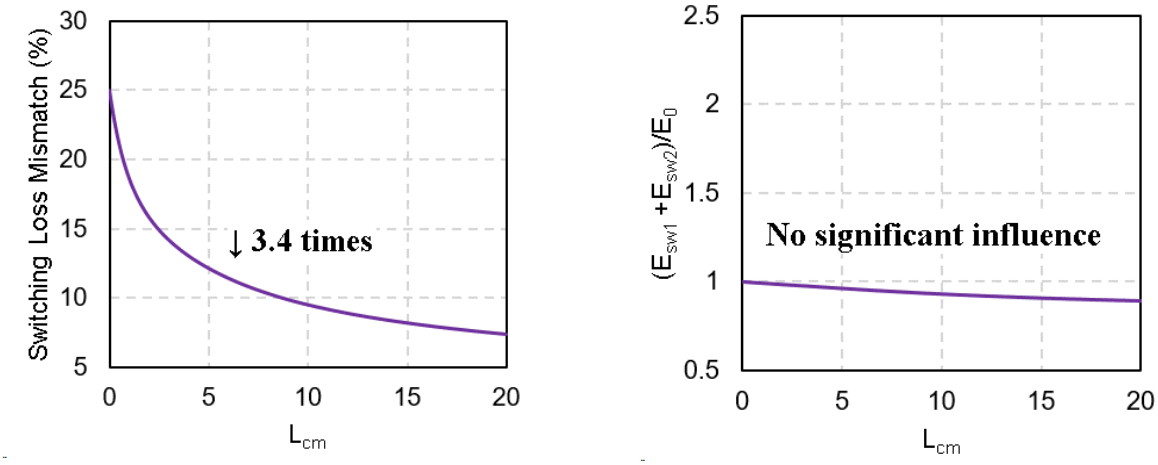
Fig. 2-13. (a) Flow of gate-driving currents in drive-source branches, where green arrow and purple arrow indicate the flow direction of common mode current and differential mode current, respectively. (b) Comparison of drain-source currents of two MOSFETs when $v_{gs1} = v_{gs2}$ (grey) and when L_s and L_k are inserted, and balance is achieved (black).

Fig. 2-14 shows the simulation results of Fig. 2-11 with varying $L_s//L_k$. The horizontal axis is normalized by base inductance defined in (2-1). With the increasing of $L_s//L_k$, switching loss mismatch is reduced by 3.4 times because of the current balancing effect, while total switching loss doesn't have significant change as illustrated in Fig. 2-13. To sum up, passive balancing structure of L_s and L_k can effectively improve dynamic sharing, without sacrificing switching loss.

Equation (2-17) demonstrates the effectiveness of L_k and L_s on current balancing, but cannot guide the selection of passive components. The derivative of Δi_{ds} in (2-17) can be obtained from (2-18) as

$$\frac{d\Delta i_{ds}}{dt} = 2g_{fs}\frac{dv_{gs}(t)}{dt}\left(\Delta v_{gs}(t) - \Delta V_{th}\right) + 2g_{fs}\frac{d\Delta v_{gs}(t)}{dt}\left(v_{gs}(t) - V_{th}\right) \tag{2-20}$$

where Δ indicates the difference of two terms ($\Delta x = x_1 - x_2$) and symbols without Δ denote the average of two terms ($x = 0.5\,(x_1 + x_2)$).



(a) **(b)**

Fig. 2-14. (a) Influence of $L_s//L_k$ on switching loss mismatch; (b) influence of $L_s//L_k$ on total switching loss. All the other inductances are set as 0 nH.

Substituting (2-20) into (2-17) and collecting terms:

$$\frac{d\Delta v_{gs}(t)}{dt} = \frac{2g_{fs}\frac{dv_{gs}(t)}{dt}\Delta V_{th} - \left(2g_{fs}\frac{dv_{gs}(t)}{dt} + \frac{1}{L_s // L_{ks}}\right)\Delta v_{gs}(t)}{2g_{fs}\left(v_{gs}(t) - V_{th}\right)},\ v_{gs}(t) > V_{th} \tag{2-21}$$

Gate driver charges C_{gs}s equally before the channels of MOSFETs are turned on (i.e., when $v_{gs}(t) \le V_{th}$). Set $t = 0$ when $v_{gs}(t) = V_{th}$. The initial value of Δv_{gs} is zero volt. According to (2-21), the slew rate of Δv_{gs} (which is the left side of (2-21)) is larger than zero when $\Delta V_{th} > 0$ and smaller than zero when $\Delta V_{th} < 0$ (as shown in Fig. 2-12(b)). The maximum value of $\Delta v_{gs}(t)$ is achieved when the numerator of (2-21) reaches zero and is expressed as

$$\Delta v_{gsMax} = \lim_{d\Delta v_{gs}/dt \to 0} \Delta v_{gs} = \frac{1}{1 + \frac{1}{2g_{fs}\frac{dv_{gs}}{dt} \times L_s // L_k}} \Delta V_{th} \tag{2-22}$$

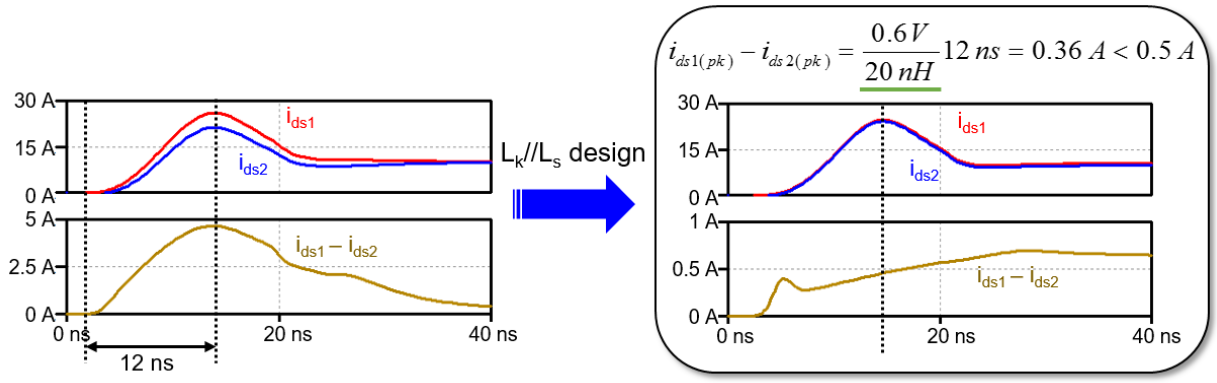
Voltage Δv_{gsMax} can be approximated by ΔV_{th} when $2g_{fs}\frac{dv_{gs}}{dt} \times L_s // L_k >> 1$. The larger the $L_s//L_k$, the better the balance effect.

According to (2-22), $\left|\Delta v_{gs}\right| \le \left|\Delta V_{th}\right|$. The maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ can be obtained by (2-17):

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{L_s // L_k} t_r \tag{2-23}$$

where t_r is time for current rising from 0 to the peak, as illustrated in Fig. 2-8. This equation predicts the maximum peak-current difference and is the worst-case design guideline for the selection of passive components.

Simulation verification of (2-23) is shown in Fig. 2-15, where threshold voltages of M1 and M2 are 2.48 V and 3.08 V, respectively. In Fig. 2-15(a), L_k is set as 0 nH. The effective balancing inductance $L_k//L_s$ equals zero. Currents of two paralleled MOSFETs are unbalanced during turn-on switching transient because of mismatched threshold voltages. In Fig. 2-15(b), $L_s//L_k$ is designed based on (2-23), where t_r = 12 ns is obtained from simulation in Fig. 2-15(a). The passive components are selected to limit the difference of peak currents below 0.5 A, which is 5% of steady-state value. Simulation results agree well with calculation. The resulting current mismatch is negligible. The worst-case design guideline in (2-23) has been demonstrated.



(a) **(b)**

Fig. 2-15. (a) Drain-source currents and current difference when L_k = 0 nH and L_s = 40 nH; (b) drain-source currents and current difference when L_k = 40 nH and L_s = 40 nH. All the other inductances are set as 0 nH.

2.4 Structure with Drive-Source Resistors and Power-Source Inductors for Slow Switching

The main reason of passive balancing effect is the voltage difference between nodes V_{s1} and V_{s2} according to the previous section. Three traces are joining at V_{s1} or V_{s2}. They are common-source trace, power-source trace, and kelvin-source trace. Any impedance on those traces should be able to produce difference between V_{s1} and V_{s2}. The passive balancing structures in Fig. 2-5 and Fig. 2-11 may be evolved by replacing inductance by capacitance or resistance. Some of those possible topologies are not suitable for practical application. The reasons are as follows. Capacitance has a DC blocking effect. Impedance on the common-source trace tends to intensely increase the switching loss. The resistance on the power-source trace resembles an extra on-state resistance and is not preferred. As a result, resistance on the drive-source trace (R_k) is the only new solution that can provide current-balancing effect without intensely increasing switching loss. The structure with power-source inductance (L_s) and drive-source resistance (R_k) is shown in Fig. 2-16 [78],[79]. The parasitics of package and layout are not included in the analysis for simplicity. The

DPT (double-pulse tester) is used for the testing of switching transients. The lower side is composed of two SiC MOSFETs with mismatched V_{th}, where V_{th1} and V_{th2} are threshold voltages of M1 and M2, respectively. The upper side is a SiC Schottky Barrier Diode (SBD). The inductive load is modeled by a constant current source.

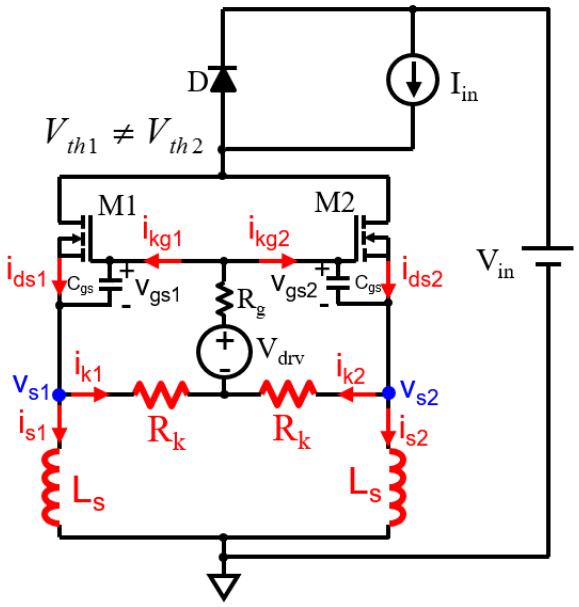


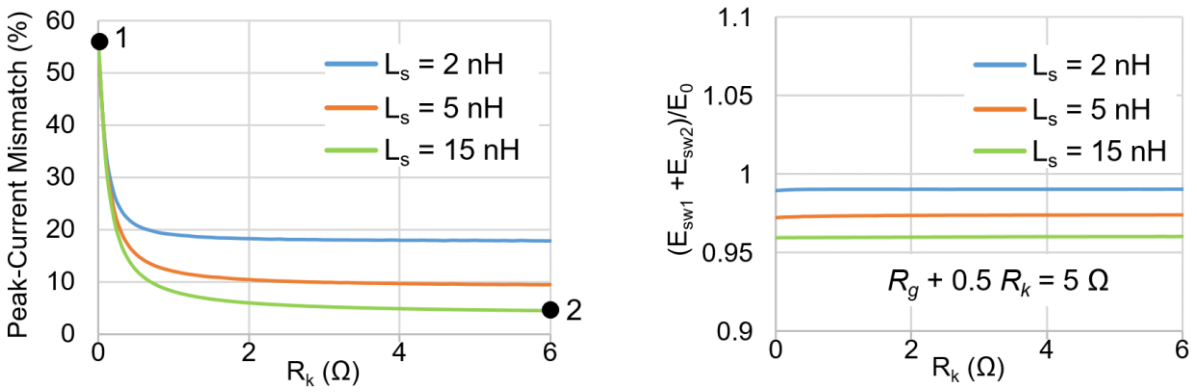
Fig. 2-16. Influence of power-source inductance (L_s) and drive-source resistance (R_k) on dynamic sharing, where lower side is paralleled SiC MOSFETs with mismatched V_{th} and upper side is SiC Schottky barrier diode.

The simulation results with varying R_k and L_s are shown in Fig. 2-17, where E_{sw1} and E_{sw2} are the switching losses (including turn-on loss and turn-off loss) of M1 and M2, respectively. Losses of bare dice are set as the normalizing factor. The mismatch of peak currents is defined as

$$\text{current} \quad \text{mismatch} = \frac{i_{pk1} - i_{pk2}}{I_{ss}} \times 100\% \tag{2-24}$$

where i_{pk1} and i_{pk2} are the peak currents of M1 and M2, respectively, and I_{ss} is the steady-state current of each MOSFET, namely half of I_{in}.

The current mismatch decreases with increasing L_s and R_k while the simulated total switching loss doesn't change significantly when (R_g + 0.5R_k) is kept constant according to Fig. 2-17. The simulation results of point 1 (R_k = 0 Ω and L_s = 15 nH) in Fig. 2-17(a) are shown in Fig. 2-18(a), and the corresponding flow of drain-source current difference is plotted in Fig. 2-19(a). When R_k = 0 Ω, two gate-source capacitors are directly paralleled (even with L_s inserted). Gate driving currents of M1 and M2 (i.e., i_{kg1} and i_{kg2}) charge the input capacitances of two MOSFETs at the same speed. MOSFET M1 (which has a smaller V_{th}) carries higher current than M2 according to Fig. 2-7. The measured peak current difference is 5.6 A. All the current difference will circulate though drive-source paths (as indicated by the green arrow in Fig. 2-19(a)) because the impedance of power-source trace is much larger than that of drive-source trace. Similarly, two gate-source capacitors are also directly paralleled and gate driving currents of M1 and M2 (i.e., i_{kg1} and i_{kg2}) charge the input capacitances of two MOSFETs at the same speed when L_s = 0 nH. The simulation results of Fig. 2-16 with R_k = 6 Ω and L_s = 0 nH are shown in Fig. 2-18(b), and the corresponding flow of drain-source current difference is plotted in Fig. 2-19(b). The measured peak current difference is 5.4 A. Different from the simulation in Fig. 2-18(a), all the current difference is circulating though power-source paths (as indicated by the green arrow in Fig. 2-19(b)), which have much smaller impedance.



(a) **(b)**

Fig. 2-17. Influence of R_k and L_s on (a) peak current mismatch and (b) normalized total switching loss, based on simulation of Fig. 2-16 with R_g + 0.5 R_k = 5 Ω, V_{in} = 600 V, I_{in} = 20 A, V_{th1} = 2.48 V, and V_{th2} = 3.08 V.

As a result, both L_s and R_k are necessary to control and limit the flowing of differential currents in drive-source trace and power-source trace. The simulation results of point 2 (R_k = 6 Ω and L_s = 15 nH) in Fig. 2-17(a) are shown in Fig. 2-18(c), and the corresponding flow of drain-source current difference is plotted in Fig. 2-19(c). According to Fig. 2-18(c), the gate driving current of M1(which has a smaller V_{th}) is smaller than that of M2 at the beginning of turn-on transient, which quickly produces a voltage difference between two gate-source capacitors to compensate the mismatch in threshold voltages. Current unbalance exists, however is damped, in both drive-source trace and power-source trace, resulting in more balanced drain-source currents.

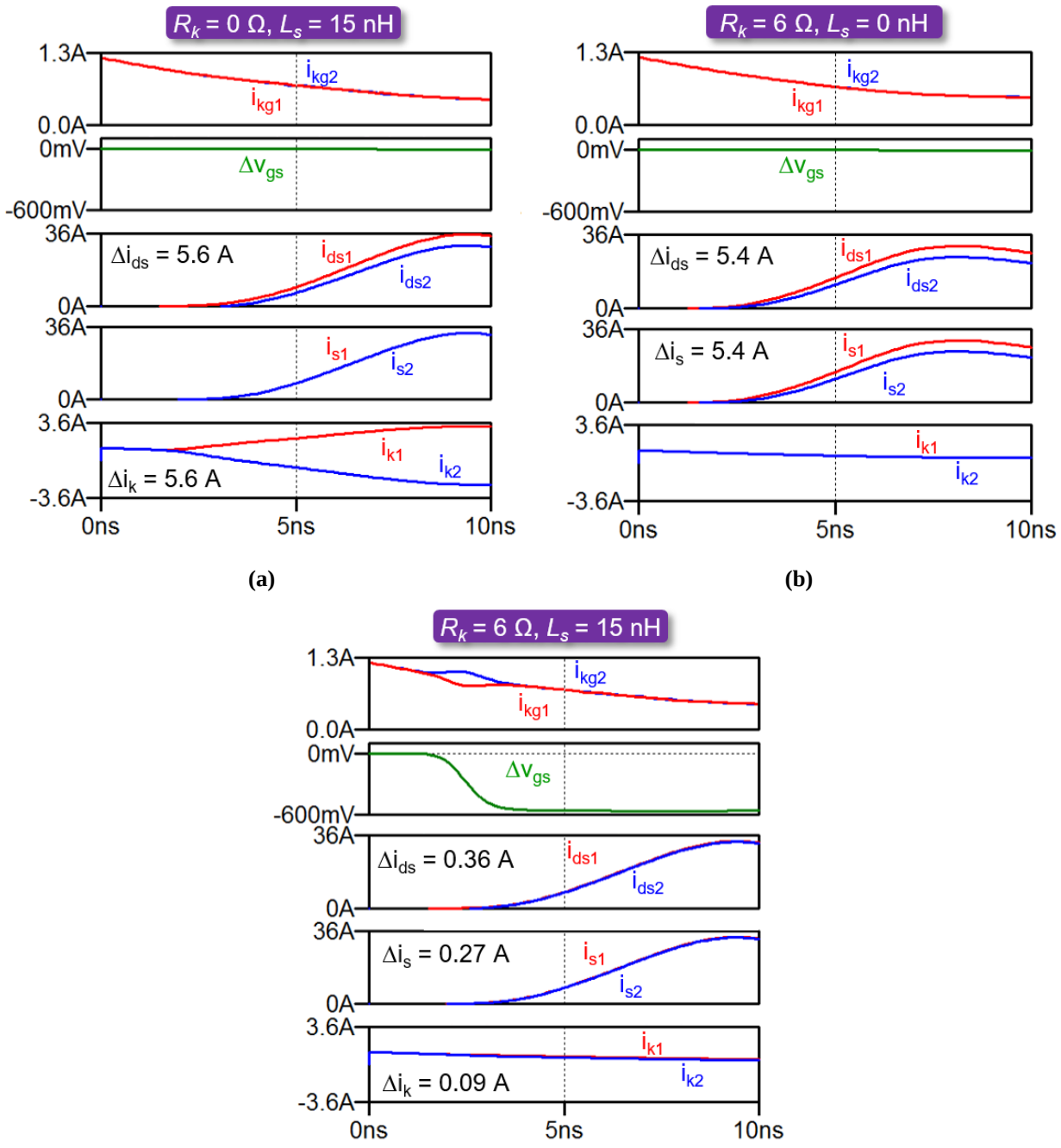


Fig. 2-18. Simulation results of Fig. 2-16 (a) with R_k = 0 Ω and L_s = 15 nH (design point 1 shown in Fig. 2-17); (b) with R_k = 6 Ω and L_s = 0 nH; (c) with R_k = 6 Ω and L_s = 15 nH (design point 2 shown in Fig. 2-17); The threshold voltages of M1 and M2 are 2.48 V and 3.08 V, respectively. The operating conditions are R_g + 0.5 R_k = 5 Ω, V_{in} = 600 V, I_{in} = 20 A, V_{th1} = 2.48 V, and V_{th2} = 3.08 V.

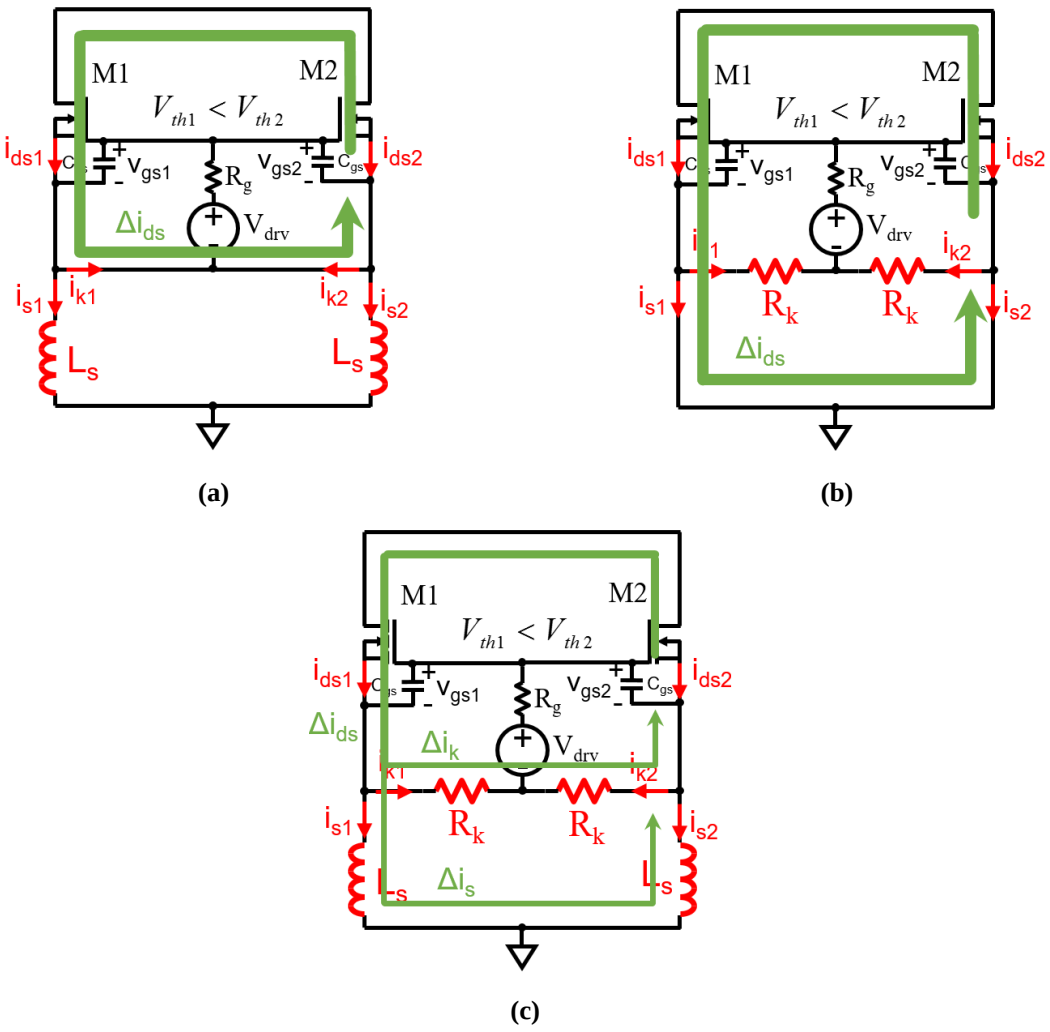


Fig. 2-19. Flow of drain-source current difference (a) when R_k = 0 Ω and $L_s \neq$ 0 nH, (b) when $R_k \neq$ 0 Ω and L_s = 0 nH, (c) when $R_k \neq$ 0 Ω and $L_s \neq$ 0 nH.

Fig. 2-17 demonstrates the effectiveness of R_k and L_s on current balancing. Design guideline for selection of passive components will be derived as follows.

Voltage Δv_{gs} can be produced by the difference between gate voltages (v_{g1} and v_{g2}) or between source voltages (v_{s1} and v_{s2}). Currents i_{kg1} and i_{kg2} are normally matched even with unequal drain-source currents, as shown in Fig. 2-18(a) and Fig. 2-18(b). The passive components on gate traces are not effective in current balancing and voltage difference between v_{g1} and v_{g2} is negligible.

Voltage Δv_{gs} approximately equals $-\Delta v_s$. This can also be demonstrated by simulation with gate inductance and/or resistance. The following analysis neglects the gate inductance and internal gate resistance to simplify the analysis.

Voltage potentials v_{s1} and v_{s2} are different with inserted L_s and R_k when i_{ds1} and i_{ds2} do not match. Voltage Δv_{gs} can be obtained by the loop containing C_{gs}s, L_ss and the loop containing C_{gs}s, R_ks:

$$\Delta v_{gs} = -L_s \frac{d\Delta i_s}{dt} \tag{2-25}$$

$$\Delta v_{gs} = -R_{ks} \Delta i_k \tag{2-26}$$

where Δi_s is the current difference of power-source inductances, and Δi_k is the current difference of drive-source resistances.

The currents through C_{gs} and C_{ds} are approximated to be zero during the i_{ds} rising interval to simplify the analysis [77]. Taking the difference of KCLs at node v_{s1} and v_{s2} in Fig. 2-16:

$$\Delta i_s + \Delta i_k \approx \Delta i_{ds} = 2g_{fs}\left(v_{gs} - V_{th}\right)\left(\Delta v_{gs} - \Delta V_{th}\right) \tag{2-27}$$

Substitution of $d\Delta i_s/dt$ from (2-25) and $d\Delta i_k/dt$ from (2-26) into the derivative of (2-27) yields

$$\frac{d\Delta v_{gs}(t)}{dt} = \frac{2g_{fs}\frac{dv_{gs}(t)}{dt}L_s\Delta V_{th} - \left(2g_{fs}\frac{dv_{gs}(t)}{dt}L_s + 1\right)\Delta v_{gs}(t)}{2g_{fs}\left(v_{gs}(t) - V_{th}\right)L_s + \frac{L_s}{R_k}} \tag{2-28}$$

The initial value of Δv_{gs} in (2-28) is zero as the gate driver charges the gate-source capacitances of M1 and M2 equally before the channels of MOSFETs is turned on. The slew rate

of Δv_{gs} is larger than zero when $\Delta V_{th} > 0$ and smaller than zero when $\Delta V_{th} < 0$ (as shown in Fig. 2-18(c)). The MOSFET with larger V_{th} has higher gate current. The maximum value of $\Delta v_{gs}(t)$ is achieved when the numerator of (2-28) reaches zero and is expressed as

$$\Delta v_{gsMax} = \frac{1}{1+\frac{1}{2g_{fs}L_s\, dv_{gs}/dt}}\Delta V_{th} \tag{2-29}$$

Voltage difference Δv_{gsMax} can be approximated by ΔV_{th} when $2g_{fs}L_s\, dv_{gs}/dt >> 1$. Dynamic balancing with unknown asymmetric V_{th} is obtained by utilizing a single gate driver.

Inductance L_s influences the steady state of $\Delta v_{gs}(t)$ according to (2-29), whereas resistance R_k affects the slew rate of Δv_{gs} according to (2-28). This resistance needs to be sufficiently large to allow $\Delta v_{gs}(t)$ to reach steady state before i_{ds} peaks.

According to (2-29), $|\Delta v_{gs}| \le |\Delta V_{th}|$. The maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ is obtained by (2-25)-(2-27):

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{|\Delta V_{th}|}{R_k} + \frac{|\Delta V_{th}|}{L_s}t_r \tag{2-30}$$

where t_r is the time for current rising from 0 to the peak.

The above equation consists of two terms. The first term shows the effect of R_k; the second term indicates the influence of L_s. To bound $|i_{ds1(pk)} - i_{ds2(pk)}|$ to $\varepsilon I_{in}/2$,

$$\frac{|\Delta V_{th}|}{R_k} + \frac{|\Delta V_{th}|}{L_s}t_r < \varepsilon\frac{I_{in}}{2} \tag{2-31}$$

where ε is preferably a small number (e.g., 5%) specified by the designer. The current unbalance

leads to switching loss difference between paralleled MOSFETs and results in unequal temperature distribution. By approximating switching loss using piecewise linear model (which is not precise, but convenient for approximation), the mismatch of peak currents and the deviation in switching energies are around a similar value. Mismatch of peak currents below 5% is the goal for the later experiment.

Fig. 2-20 shows the recommended design procedure for the passive balancing solution in Fig. 2-16, where texts on the left side show how to choose the corresponding values, and tests on the right sides are the values applied to the simulation verification in Fig. 2-21. Firstly, the maximum peak-current difference $\max|\Delta i_{ds(pk)}|$ is determined. Five percent of $0.5I_{in}$, which equals 0.5 A for the simulation in Fig. 2-21, is applied in this dissertation. Then, constants ΔV_{th} and t_r in design guideline (2-30) are obtained by datasheet, simulation, or measurement. For the simulation in Fig. 2-21, mismatch of threshold voltage between two paralleled MOSFETs is -0.6 V and current rise time t_r is 16 ns, which is obtained by the baseline simulation in Fig. 2-21(a). Finally, the design trajectory of R_k and L_s is achieved by (2-30), as plotted in Fig. 2-20(b). Any designs on and above this trajectory are able to limit peak-current difference below the predetermined $\max|\Delta i_{ds(pk)}|$ by increasing R_k and L_s. The value of L_s decreases quickly with the increase of R_k and stays almost constant when R_k is above 6 Ω. The design at the knee of this curve is selected to have moderate values for both L_s and R_k.

Simulation results of Fig. 2-16 before current balancing is shown in Fig. 2-21(a). The 0.6 V mismatch in V_{th} produces 4.6 A peak-current difference. Fig. 2-21(b) plots the simulation results after current balancing, where L_s and R_k are designed based on the procedure shown in Fig. 2-20. The measured current difference at the peak of i_{ds} is 0.47 A, which is smaller than the desired $\max|\Delta i_{ds(pk)}|$. Simulation results agree well with calculation. Current imbalance is almost

unnoticeable with the passive balancing method.

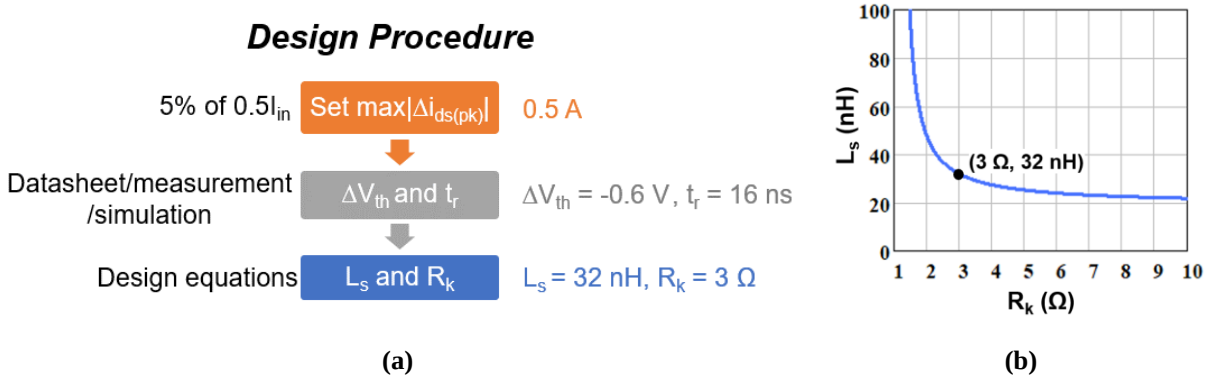


Fig. 2-20. (a) Design procedure of passive balancing solution in Fig. 2-16. (b) Design trajectory of L_s and R_k obtained from (2-30), where $\max|i_{ds1(pk)}-i_{ds2(pk)}| = 0.5$ A, $t_r = 16$ ns, and $\Delta V_{th} = -0.6$ V.

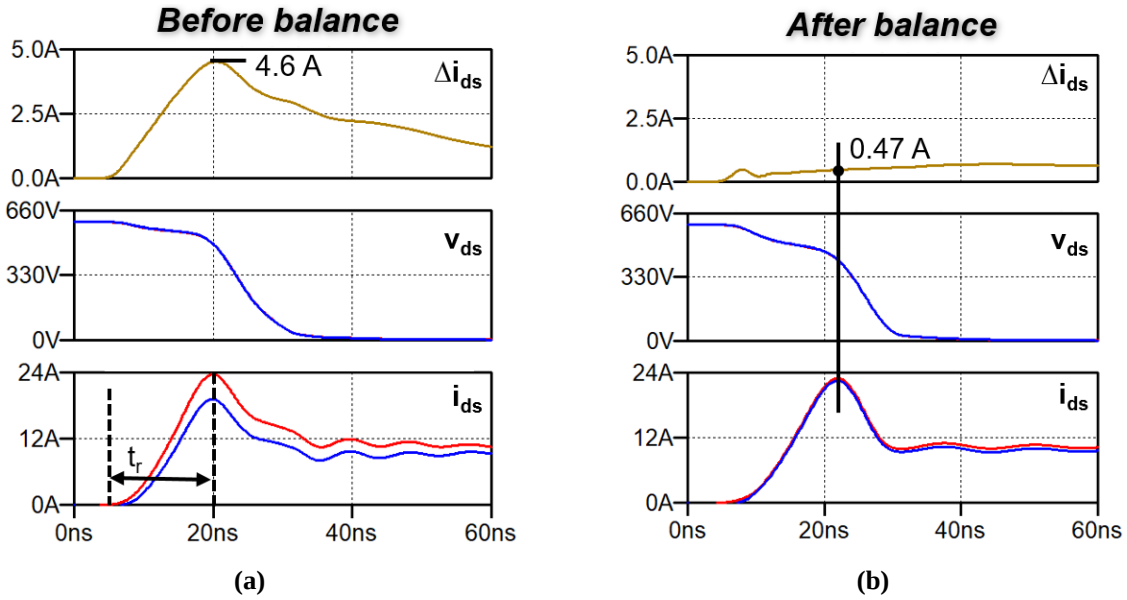


Fig. 2-21. Simulation results of Fig. 2-16 before current balancing and (b) after current balancing, where L_s and R_k are designed in Fig. 2-20. The operating conditions are $R_g + 0.5\,R_k = 15\,\Omega$, $V_{in} = 600$ V, $I_{in} = 20$ A, $V_{th1} = 2.48$ V, and $V_{th2} = 3.08$ V.

2.5 Reduction of Voltage Stress by Magnetic Coupling for Fast Switching

Power-source inductance can be designed to balance switching transients without increasing switching energy at the expense of producing extra voltage stress during turn-off transient, as shown in Fig. 2-22. This induced voltage drop on L_s may be only a small portion of input voltage and is not a problem if switching speed is not fast. Passive balancing structures introduced in the previous section can be directly applied. The extra voltage stress produced by the designed L_s should be reduced if the voltage across L_s will cause drain-source voltage exceeding the blocking voltage of MOSFET.

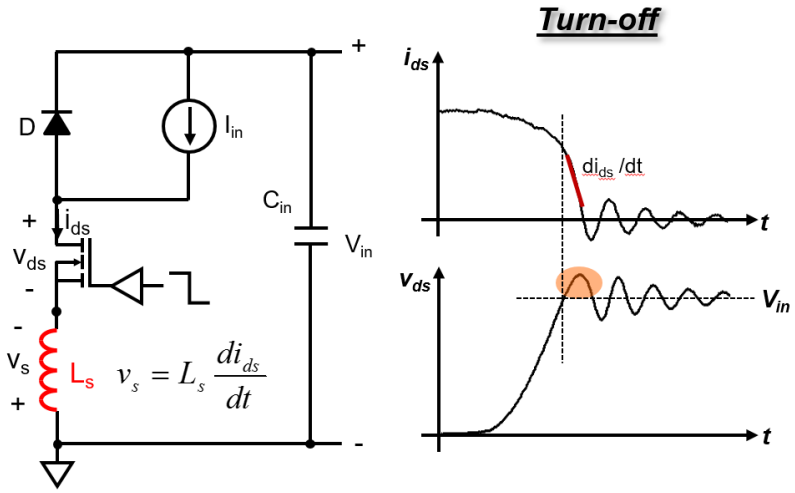


Fig. 2-22. Extra voltage stress produced by power-source inductance during turn-off transient.

Fig. 2-23 shows the enhancement of balancing effect by coupling of drive-source inductors and coupling of power-source inductors, which can reduce the extra voltage stress produced by L_s. Reasons are explained as follows.

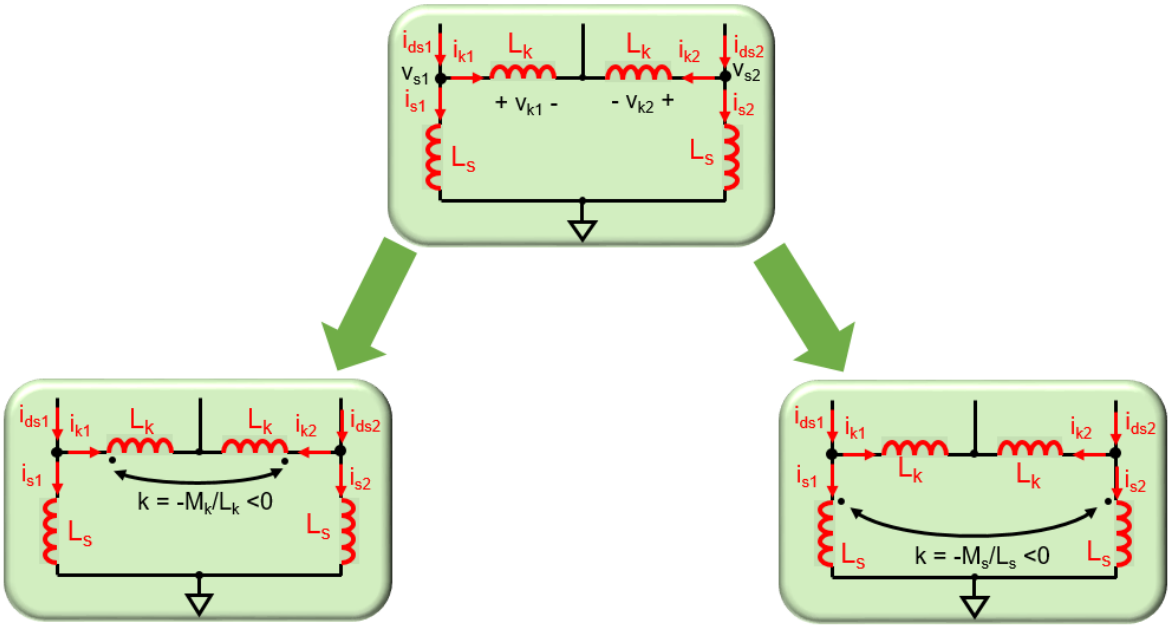


Fig. 2-23. Enhancement of balancing effect by coupling of drive-source inductors and coupling of power-source inductors.

According to the loop formed by power-source inductors and drive-source inductors,

$$v_{s1} - v_{s2} = v_{k1} - v_{k2} \tag{2-32}$$

With negatively coupled L_k (as shown in Fig. 2-23),

$$v'_{k1} = L_k \frac{di_{k1}}{dt} - M_k \frac{di_{k2}}{dt} \tag{2-33}$$

$$v'_{k2} = L_k \frac{di_{k2}}{dt} - M_k \frac{di_{k1}}{dt} \tag{2-34}$$

Substituting (2-33) and (2-34) into (2-32) yields

$$v'_{s1} - v'_{s2} = \frac{L_k + M_k}{L_k}\left(v_{s1} - v_{s2}\right) \tag{2-35}$$

Voltage difference at source terminals is increased by (1-k) times, where $k = - M_k/L_k < 0$. Because current balancing effect is provided by the mismatch between v_{s1} and v_{s2} (i.e. between v_{gs1} and v_{gs2}), less L_s is required for the same balancing performance resulting in less voltage stress.

Similarly, voltage difference between v_{s1} and v_{s2} can be increased by coupling power-source inductors. With negatively coupled L_s (as shown in Fig. 2-23),

$$v'_{s1} = L_s \frac{di_{s1}}{dt} - M_s \frac{di_{s2}}{dt} \tag{2-36}$$

$$v'_{s2} = L_s \frac{di_{s2}}{dt} - M_s \frac{di_{s1}}{dt} \tag{2-37}$$

From (2-36) and (2-37):

$$v'_{s1} - v'_{s2} = \frac{L_s + M_s}{L_s}\left(v_{s1} - v_{s2}\right) \tag{2-38}$$

Voltage difference at source terminals is increased by (1-k) times, where $k = - M_s/L_s < 0$. Less L_s is required for the same balancing performance resulting in less voltage stress.

2.5.1 Structure with Drive-Source Resistors and Coupled Power-Source Inductors

Power-source inductors balance currents, but also add voltage stress. They will be coupled to solve this problem. The passive balancing topology with drive-source resistors (R_k) and inversely- or negatively-coupled power-source inductors (L_{s1} and L_{s2}) is shown in Fig. 2-25(a). The four inductors that have minor influence on current mismatch according Fig. 2-3, as well as L_{cm}, are

excluded from further consideration.

The equivalent circuit of negatively-coupled inductors is shown in Fig. 2-24, where the coupled inductors are replaced by the series connection of (L + M) and -M (M > 0) [80]. Fig. 2-25(b) shows the equivalent circuit of Fig. 2-25(a) when applying Fig. 2-24 [81]. Comparing the structure with coupling (shown in Fig. 2-25(b)) to the structure without coupling (shown in Fig. 2-16), negative coupling enhances balancing by increasing the equivalent power-source inductance in the differential-mode path (indicated by the curved arrow) from L_s to ($L_s + M_s$). It decreases the voltage stress (as well as ringing, EMI, etc.) by decreasing the power-source inductance in the common-mode path (indicated by the straight arrow) from L_s to ($L_s + M_s - 2M_s$) = $L_s - M_s$.

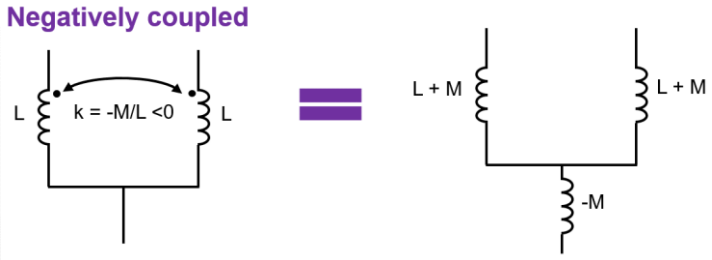


Fig. 2-24. Equivalent circuit of negatively-coupled inductors.

The difference Δi_{ds} between drain-source currents is driven toward zero in the presence of ΔV_{th} by driving the gates such that $v_{gs1} - v_{gs2} = \Delta v_{gs}$ approaches ΔV_{th}. The MOSFET current i_{ds} follows the saturation model as it rises from zero to the peak:

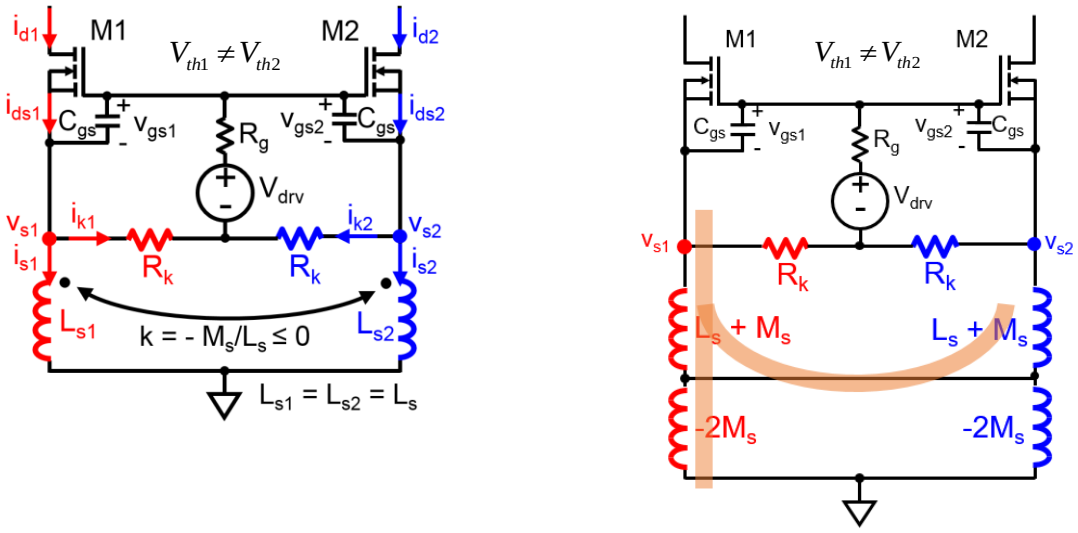
$$i_{ds_j} = g_{fs}\left(v_{gs_j} - V_{th_j}\right)^2, v_{gs_j} > V_{th_j}, j = 1,2 \qquad (2\text{-}39)$$

where V_{th1} and V_{th2} are the threshold voltages of M1 and M2, respectively. The large-signal transconductance g_{fs} is assumed to match for both MOSFETs. The current difference is thus

$$\Delta i_{ds} = 2g_{fs}\left(v_{gs} - V_{th}\right)\left(\Delta v_{gs} - \Delta V_{th}\right), \quad v_{gs} > V_{th} \tag{2-40}$$

where

$$\Delta x = x_1 - x_2,\ x = 0.5\left(x_1 + x_2\right) \tag{2-41}$$



(a) **(b)**

Fig. 2-25. (a) Passive topology employing negatively coupled power-source inductors ($L_{s1/2}$) and drive-source resistors (R_k) to balance peak currents; (b) equivalent circuit.

If $L_s = 0$ H or $R_k = 0\ \Omega$, $\Delta v_{gs} = 0$ V and the MOSFET with smaller V_{th} carries larger current as exemplified in Fig. 2-26, then L_s and R_k in Fig. 2-25(a) need to be non-zero so that $\Delta v_{gs} = -\Delta v_s$ has an opportunity to reach ΔV_{th} to equalize the drain currents

.

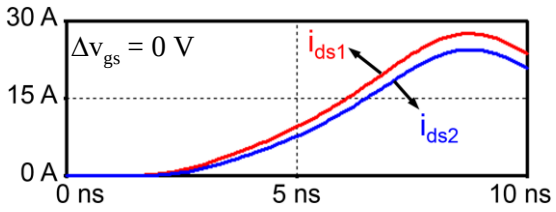


Fig. 2-26. Simulation results of Fig. 2-25(a) with R_g = 5 Ω, R_k = 0 Ω, L_s = 15 nH, k = 0, V_{th1} = 2.34 V, and V_{th2} = 2.78 V. SPICE models for MOSFETs [33] and diode [82] are from CREE.

The next four equations are dedicated toward proving that Δv_{gs} approaches ΔV_{th} with the help from L_s, M_s, and R_k. The simulated waveforms for $\Delta v_{gs}(t)$, $v_{gs1}(t)$, and $i_{ds1/2}(t)$ are plotted in Fig. 2-27 to offer insight and to identify approximations for the analysis. From Fig. 2-25 (b),

$$\Delta v_{gs} = -(L_s + M_s)\frac{d\Delta i_s}{dt} = -R_k \Delta i_k \tag{2-42}$$

If the currents through C_{gs} and C_{ds} are neglected while i_{ds} rises as suggested by [77], $i_{ds} \approx i_s + i_k$. Then,

$$\Delta i_{ds} \approx \Delta i_s + \Delta i_k \approx 2g_{fs}(v_{gs} - V_{th})(\Delta v_{gs} - \Delta V_{th}) \tag{2-43}$$

Substitution of $d\Delta i_s/dt$ and $d\Delta i_k/dt$ from (2-42) into the derivative of (2-43) yields the following approximation while i_{ds} rises:

$$\frac{d\Delta v_{gs}(t)}{dt} \approx -\frac{2g_{fs}\dfrac{dv_{gs}(t)}{dt}(L_s + M_s) + 1}{2g_{fs}(v_{gs}(t) - V_{th})(L_s + M_s) + \dfrac{L_s + M_s}{R_k}}\Delta v_{gs}(t) + \frac{2g_{fs}\dfrac{dv_{gs}(t)}{dt}(L_s + M_s)}{2g_{fs}(v_{gs}(t) - V_{th})(L_s + M_s) + \dfrac{L_s + M_s}{R_k}}\Delta V_{th}, \Delta v_{gs}(0) = 0 \tag{2-44}$$

Fig. 2-27 suggests that dv_{gs}/dt could be treated as a constant ($dv_{gs}/dt = m$) during the short transient of Δv_{gs}. The maximum Δv_{gs} is reached as $d\Delta v_{gs}/dt$ approaches zero:

$$\Delta v_{gsMax} = \lim_{d\Delta v_{gs}/dt \to 0} \Delta v_{gs} = \frac{1}{1+\left[2g_{fs}m\left(L_s + M_s\right)\right]^{-1}} \Delta V_{th} \tag{2-45}$$

The larger ($L_s + M_s$) is, the closer Δv_{gsMax} is to ΔV_{th}. Thus, the inequality

$$\left[2g_{fs}m\left(L_s + M_s\right)\right]^{-1} << 1 \tag{2-46}$$

enables $\Delta v_{gs} \rightarrow \Delta V_{th}$ and $\Delta i_{ds} \rightarrow 0$. This and the simulation waveforms in Fig. 2-27 prove the feasibility of dynamic balancing with unknown polarity of V_{th} difference and with one gate driver by the "current-balancing inductance" ($L_s + M_s$).

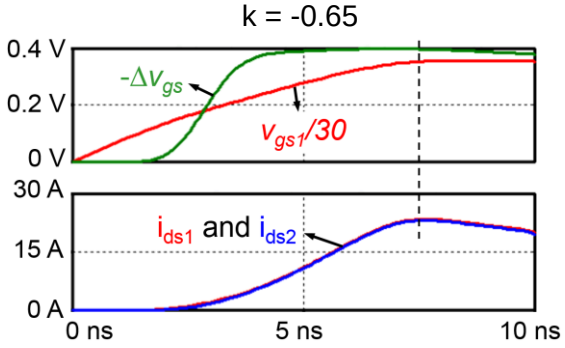


Fig. 2-27. Simulation results of Fig. 2-25(a) with $R_g + 0.5\ R_k = 5\ \Omega$, $V_{th1} = 2.34$ V, $V_{th2} = 2.78$ V, $L_s = 9.1$ nH, $M_s = 5.9$ nH, and $R_k = 5.6\ \Omega$.

The duration of the Δv_{gs} transient should be short so that Δv_{gs} could reach the desired value when i_{ds} peaks. With (2-46), (2-44) is simplified to

$$\frac{d\Delta v_{gs}(t)}{dt} \approx -\frac{2g_{fs}m}{2g_{fs}\left(v_{gs}(t)-V_{th}\right)+\dfrac{1}{R_k}}\left[\Delta v_{gs}(t)-\Delta V_{th}\right] \tag{2-47}$$

The theory presented in this sub-section has established that (L_s + M_s) influences the Δv_{gsMax} according to (2-45) and that R_k affects the "slew rate" of $\Delta v_{gs}(t)$ if (2-47) were a first-order differential equation. More details are illustrated by the parametric simulation in Fig. 2-28. Resistance R_k and inductance (L_s + M_s) should be designed together to achieve the required Δv_{gs} at i_{ds} peaks. If either of them is zero, the source terminals are shorted and there is no balancing effect (Δv_{gs} = 0 V). The circuit in Fig. 2-25(a) was simulated with the passive components swept, and the results are plotted in Fig. 2-29(a) to reinforce these points. Once R_k is designed properly (e.g., 2 Ω < R_k < R_{kmax}, where R_{kmax} is the maximum resistance specified by the designer), the mismatch percentage settles to a low level determined by (L_s + M_s). The case of L_s + M_s = 15 nH is detailed in Fig. 2-27.

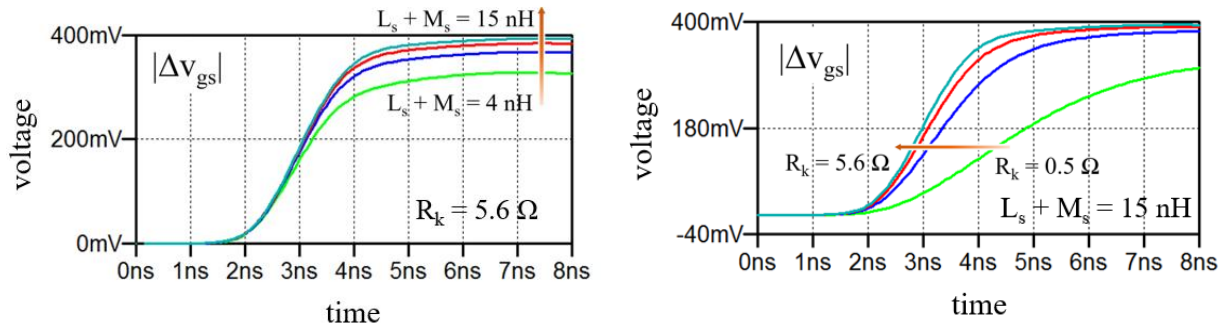
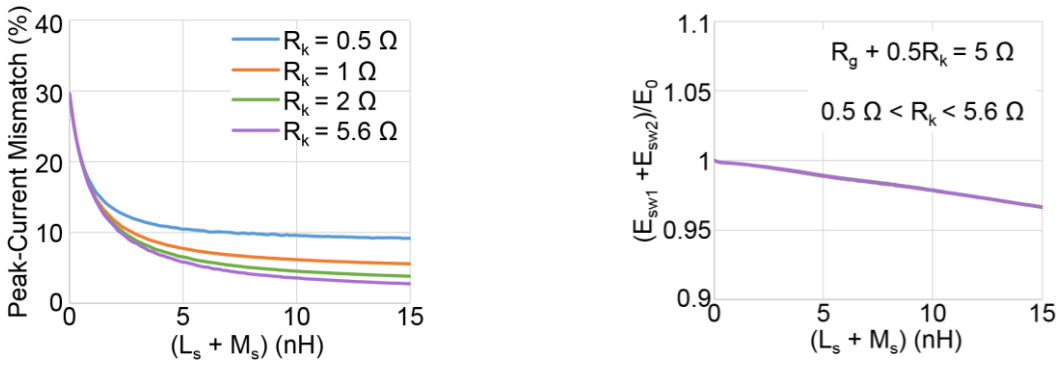


Fig. 2-28. (a) Influence of (L_s + M_s) on Δv_{gsMax}, where R_k = 5.6 Ω and (b) influence of R_k on slew rate of Δv_{gs}, where L_s + M_s = 15 nH



(a) **(b)**

Fig. 2-29. Simulation results of Fig. 2-25(a) with $R_g + 0.5R_k = 5\ \Omega$, $V_{in} = 300$ V, $I_{in} = 20$ A, $V_{th1} = 2.34$ V, $V_{th2} = 2.78$ V, and $k = -0.65$. (a) peak-current mismatch and (b) total switching energy with varying R_k and ($L_s + M_s$).

The voltage across a power-source inductance like L_{s1} (L_{s2}) in Fig. 2-25(a) is expected to increase the voltage stress on M1 (M2). Negative coupling of a fraction of the voltage across L_{s2} (L_{s1}) is leveraged to reduce the extra stress. Assuming the currents of M1 and M2 are balanced with the designed passive components, the additional voltage stress on M1 is

$$v_{s1} = L_s \frac{di_{s1}}{dt} - M_s \frac{d\left(i_{s2} = i_{s1} - \Delta i_s\right)}{dt} \approx \left(L_s - M_s\right)\frac{di_{s1}}{dt} \tag{2-48}$$

The inductance (L_s – M_s) is thus named “stress-inducing inductance”. Perfect coupling between L_{s1} and L_{s2} would enable current matching without penalty on voltage stress.

The influence of current balancing strategy on total switching energy is depicted in Fig. 2-29(b). The power-source inductance reduces the turn-on loss and increases the turn-off loss. The total switching energy doesn’t change significantly if (R_g + 0.5R_k) is kept constant [77],[113].

One comparison of switching transients without L_s and with coupled L_s is shown in Fig. 2-30. The drain inductance L_d and power-loop inductance L_p are included to make the voltage spike

visible. The current-balancing inductance and stress-inducing inductance are zero in Fig. 2-30(a). The mismatched V_{th} and uncompensated gate-source voltages lead to unbalanced currents. The voltage stress is introduced by L_d and L_p only. The simulation in Fig. 2-30(b) applies the current balancing solution with a coupling coefficient around -0.65. The switching transient are able to be balanced with an extra voltage stress of 8 V. The influences on di_{ds}/dt and switching energy are also negligible compared to Fig. 2-30(a). The case with L_p = 120 nH is also shown Fig. 2-30(b) as dashed lines to validate the ringing in the later experiment is caused by a large L_p instead of the current balancing scheme.

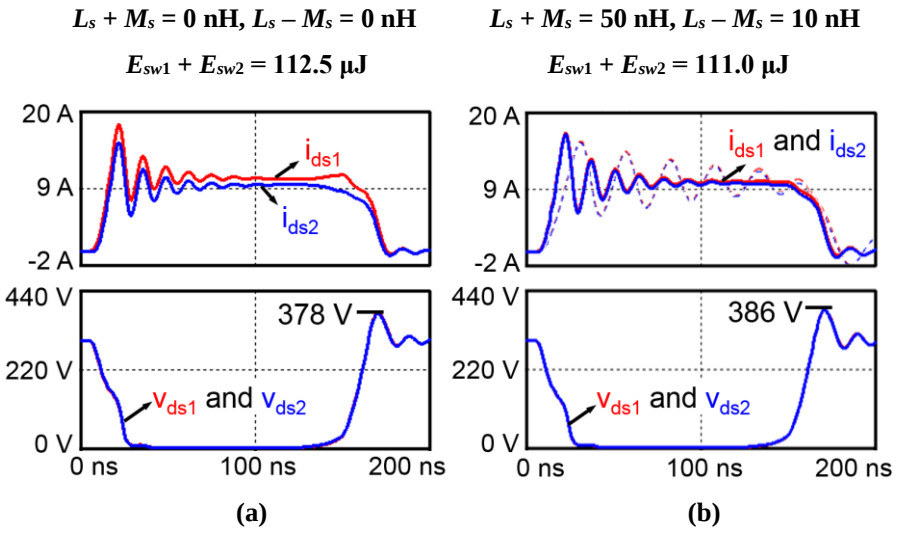


Fig. 2-30. Simulation results of Fig. 2-25(a) at V_{in} = 300 V, I_{in} = 20 A, $R_g + 0.5R_k$ = 20 Ω, L_d = 20 nH, L_p = 20 nH, V_{th1} = 2.34 V, and V_{th2} = 2.78 V: (a) L_s = 0 nH, M_s = 0 nH, and R_k = 5.6 Ω; (b) L_s = 30 nH, M_s = 20 nH, and R_k = 5.6 Ω (solid waveforms). The dashed waveforms correspond to the experimental results in the later section with L_p = 120 nH.

The effectiveness of R_k and L_s on current balancing has been analyzed. A design guideline is next suggested to facilitate their selection. According to (2-45), $|\Delta v_{gs}| \le |\Delta V_{th}|$. The maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ can be obtained from (2-42) and (2-43) as

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{R_k} + \frac{\left|\Delta V_{th}\right|}{L_s + M_s} t_r \tag{2-49}$$

where t_r is the time for current to rise from 0 to the peak value.

The above equation consists of two terms. The first term shows the effect of R_k; the second term indicates the influence of L_s and M_s. The required (L_s + M_s) is proportional with t_r because the slew rate m (= dv_{gs}/dt) in (2-45) decreases with t_r. To bound $|i_{ds1(pk)} - i_{ds2(pk)}|$ to $\varepsilon I_{in}/2$, the components should be selected such that

$$\frac{\left|\Delta V_{th}\right|}{R_k} + \frac{\left|\Delta V_{th}\right|}{L_s + M_s} t_r < \varepsilon \frac{I_{in}}{2} \tag{2-50}$$

where ε is preferably a small number (e.g., 5%) specified by the designer. The current unbalance leads to switching loss difference between paralleled MOSFETs and results in unequal temperature distribution [55]. By approximating switching loss using piecewise linear model (which is not precise, but convenient for approximation) [57], the mismatch of peak currents and the deviation in switching energies are around a similar value. Mismatch of peak currents below 5% is the goal for the later experiment.

Fig. 2-31 compares the design trajectories of (L_s – M_s) and R_k calculated by (2-49) with different mutual inductances. The vertical axis is stress-inducing inductance (L_s – M_s), instead of current-balancing inductance (L_s + M_s), to reveal the impact of negative magnetic coupling on the reduction of voltage stress. The other conditions employed are $\max|i_{ds1(pk)} - i_{ds2(pk)}|$ = 0.5 A, $|\Delta V_{th}|$ = 0.44 V, and t_r = 35 ns, which are the same as the situation in the later experiment. The obtained curves illustrate the possible designs that satisfy $\max|i_{ds1(pk)} - i_{ds2(pk)}|$ = 0.5 A. Less R_k and (L_s – M_s) are required with increased M_s for the same balancing effect. Perfect coupling between L_{s1} and L_{s2}

would enable current matching without penalty on voltage stress, i.e., $L_s - M_s = 0$ nH. Designs above those trajectories can provide even smaller $\max|i_{ds1(pk)} - i_{ds2(pk)}|$.

Fig. 2-32 shows the recommended design procedure for the passive balancing solution in Fig. 2-25, where texts on the left side show how to choose the corresponding values, and tests on the right sides are the values applied to the simulation verification in Fig. 2-33. Firstly, the maximum peak-current difference $\max|\Delta i_{ds(pk)}|$ is determined. Five percent of $0.5I_{in}$, which equals 0.5 A for the simulation in Fig. 2-33, is applied. Then, constants ΔV_{th} and t_r in design guideline (2-30) are obtained by datasheet, simulation, or measurement. For the simulation in Fig. 2-33, mismatch of threshold voltage between two paralleled MOSFETs is -0.6 V and current rise time t_r is 16 ns, which is obtained by the baseline simulation in Fig. 2-33(a). Next, the stress-inducing inductance ($L_s - M_s$) needs to be determined. Same ($L_s - M_s$) as baseline simulation is selected for the balancing topology for easy comparison. Finally, the design trajectory of R_k and L_s is achieved by (2-49), as plotted in Fig. 2-32(b). Any designs on and above this trajectory are able to limit peak-current difference below the predetermined $\max|\Delta i_{ds(pk)}|$. The value of L_s decreases quickly with the increase of R_k and stays almost constant when R_k is above 6 Ω. The design at the knee of this curve is selected to have moderate values for both L_s and R_k.

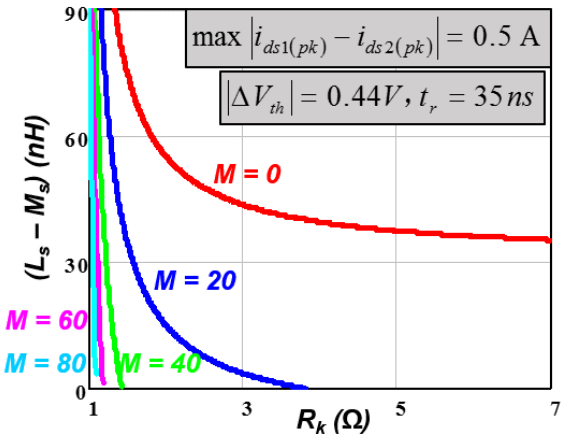
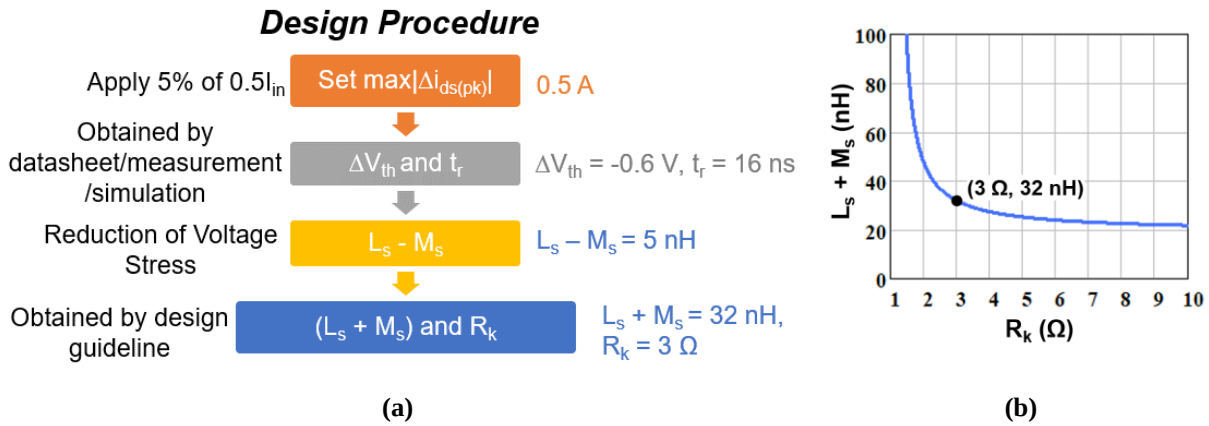


Fig. 2-31. Trajectories of (L_s – M_s) and R_k calculated by (2-49) with different mutual inductances.

Simulation results of Fig. 2-25 before current balancing are shown in Fig. 2-33(a). The 0.6 V mismatch in V_{th} produces 4.6 A peak-current difference. Fig. 2-33(b) plots the simulation results after current balancing, where (L_s + M_s), (L_s – M_s), and R_k are designed based on the procedure suggested in Fig. 2-32. The measured current difference at the peak of i_{ds} is 0.45 A, which is smaller than the desired max|$\Delta i_{ds(pk)}$| = 0.5 A as designed. The same voltage stress is maintained by negative coupling of power-source inductors.



(a) **(b)**

Fig. 2-32. (a) Design procedure of passive balancing solution in Fig. 2-25. (b) Design trajectory of (L_s + M_s) and R_k obtained from (2-49), where max|$i_{ds1(pk)}$-$i_{ds2(pk)}$| = 0.5 A, t_r = 16 ns, and ΔV_{th} = -0.6 V.

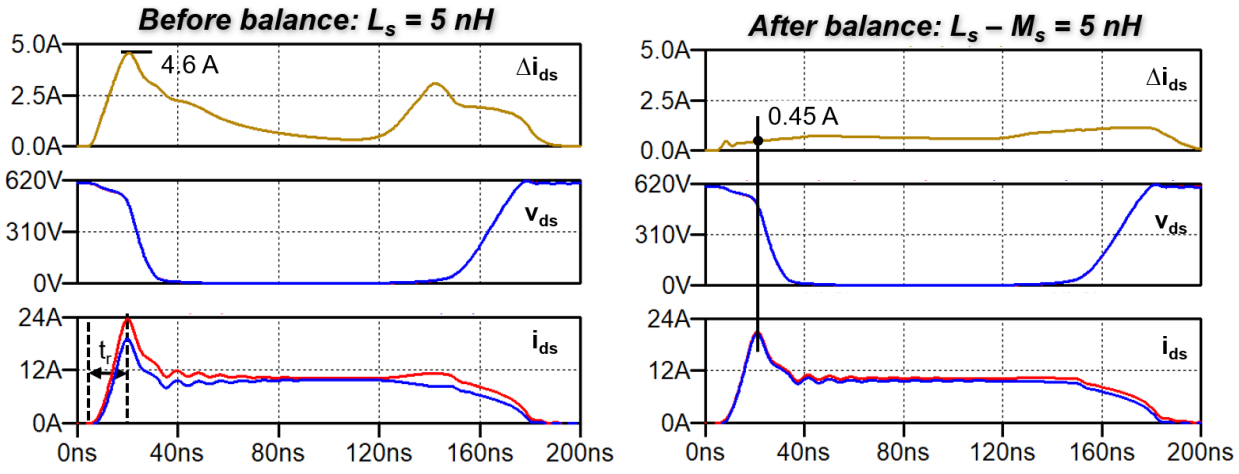


Fig. 2-33. Simulation results of Fig. 2-25 with V_{th1} = 2.48 V and V_{th2} = 3.08 V, (a) before current balancing and (b) after current balancing, where (L_s + M_s) and R_k are designed in Fig. 2-32. The operating conditions are R_g + 0.5 R_k = 15 Ω, V_{in} = 600 V, I_{in} = 20 A. Experimental validations over wide operating ranges are shown in Section 2.7.

2.5.2 Other Structures with Magnetic Coupling

The passive balancing topology with negatively coupled drive-source inductors and discrete power-source inductors is shown in Fig. 2-34(a). The corresponding equivalent circuit is shown in Fig. 2-34(b), where coupled inductors are replaced by the series connection of (L_k + M_k) and –M_k (M_k > 0). Comparing the structure with coupling (shown in Fig. 2-34(a)) to the structure without coupling (shown in in Fig. 2-11), negative coupling enhances balancing by increasing the equivalent drive-source inductance in the differential-mode path from L_k to (L_k + M_k) and reduces the terminal gate inductance by M_s. The change of terminal gate inductance can be neglected in the later analysis as it has slight influence on sharing, voltage stress, and switching loss, as shown in Table 2-1.

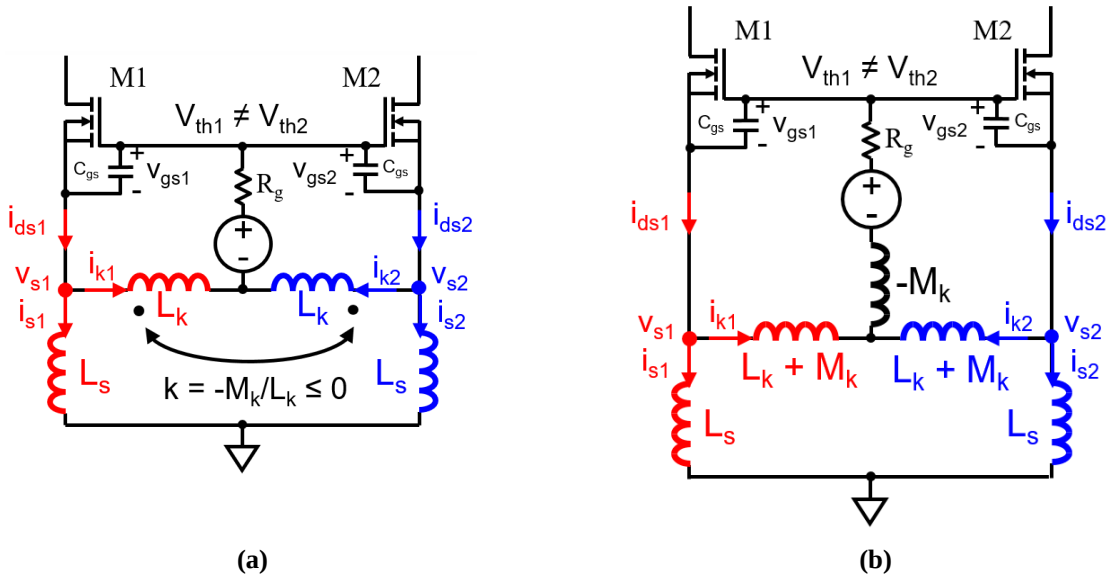


Fig. 2-34. (a) Passive topology employing negatively coupled drive-source inductors and discrete power-source inductors to balance peak currents; (b) equivalent circuit.

From the loop containing C_{gs}s, L_ss and the loop containing C_{gs}s, L_ks, voltage difference between v_{gs1} and v_{gs2} is given as

$$\Delta v_{gs} = -L_s\left(\frac{di_{s1}}{dt} - \frac{di_{s2}}{dt}\right) = -\left(L_k + M_k\right)\left(\frac{di_{k1}}{dt} - \frac{di_{k2}}{dt}\right) \tag{2-51}$$

Following the procedures in (2-16)-(2-23), the maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ can be obtained as

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{L_s \,//\left(L_k + M_k\right)} t_r \tag{2-52}$$

where t_r is the time for current to rise from 0 to the peak value.

Comparing (2-52) with (2-23), the effective drive-source inductance is increased by mutual inductance.

Fig. 2-35 compares the design trajectories of L_s and L_k calculated by (2-52) with different

mutual inductances. The other conditions employed are $\max|i_{ds1(pk)} - i_{ds2(pk)}| = 0.5$ A, $|\Delta V_{th}| = 0.44$ V, and $t_r = 35$ ns, which are the same as the situation in the later experiment. The obtained curves illustrate the possible designs that satisfy $\max|i_{ds1(pk)} - i_{ds2(pk)}| = 0.5$ A. Less L_k and L_s are required with increased M_s for the same balancing effect. Designs above those trajectories can provide even smaller $\max|i_{ds1(pk)} - i_{ds2(pk)}|$.

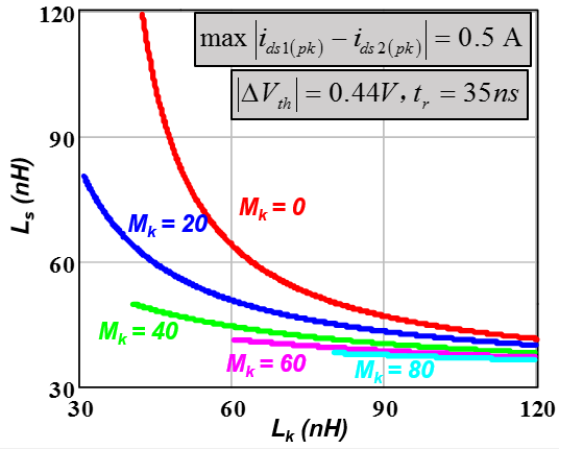


Fig. 2-35. Trajectories of L_s and L_k calculated by (2-52) with different mutual inductances.

Passive balancing topology with negatively coupled power-source inductors and discrete drive-source inductors is shown in Fig. 2-36(a). The corresponding equivalent circuit is shown in Fig. 2-36(b), where the coupled inductors are replaced by the series connection of $(L_s + M_s)$ and $-M_s$ ($M_s > 0$). Comparing the structure with coupling (shown in Fig. 2-36(a)) to the structure without coupling (shown in Fig. 2-11), negative coupling enhances balancing by increasing the equivalent power-source inductance in the differential-mode path from L_s to $(L_s + M_s)$ and reduces the voltage stress (as well as ringing, EMI, etc.) by decreasing the power-source inductance in the common-mode path from L_s to $(L_s + M_s - 2M_s) = L_s - M_s$.

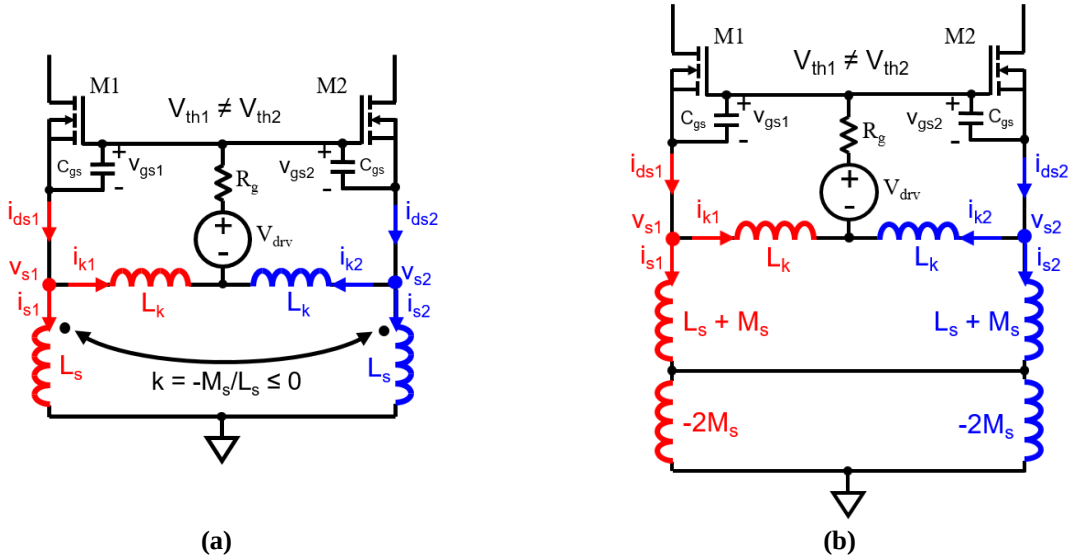


Fig. 2-36. (a) Passive topology employing negatively coupled power-source inductors and discrete drive-source inductors to balance peak currents; (b) equivalent circuit.

From the loop containing C_{gs}s, L_ss and the loop containing C_{gs}s, L_ks, voltage difference between v_{gs1} and v_{gs2} is given as

$$\Delta v_{gs} = -(L_s + M_s)\left(\frac{di_{s1}}{dt} - \frac{di_{s2}}{dt}\right) = -L_k\left(\frac{di_{k1}}{dt} - \frac{di_{k2}}{dt}\right) \tag{2-53}$$

Following the procedures in (2-16)-(2-23), the maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ can be obtained as

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{|\Delta V_{th}|}{(L_s + M_s)/\!/\, L_k} t_r \tag{2-54}$$

where t_r is the time for current to rise from 0 to the peak value.

Comparing (2-54) with (2-23), the effective power-source inductance is increased by mutual inductance.

Fig. 2-37 shows the design trajectories of (L_s – M_s) and L_k calculated by (2-54) with different mutual inductances. The vertical axis is stress-inducing inductance (L_s – M_s), instead of current-balancing inductance (L_s + M_s), to reveal the impact of negative magnetic coupling on the

reduction of voltage stress. The other conditions employed are max|$i_{ds1(pk)}$ - $i_{ds2(pk)}$| = 0.5 A, |ΔV_{th}| = 0.44 V, and t_r = 35 ns, which are the same as the situation in the later experiment. Those curves show the possible designs that satisfy max|$i_{ds1(pk)}$ - $i_{ds2(pk)}$| = 0.5 A. If even smaller max|$i_{ds1(pk)}$ - $i_{ds2(pk)}$| wants to be achieved, designs above the lines should be selected. According to Fig. 2-37, lines are shifted downward when mutual inductance is increased, which means negative coupling of L_s can reduce the required inductances. This passive balancing method won't produce an extra voltage stress if perfect coupling is achieved, i.e. $L_s - M_s = 0$ nH.

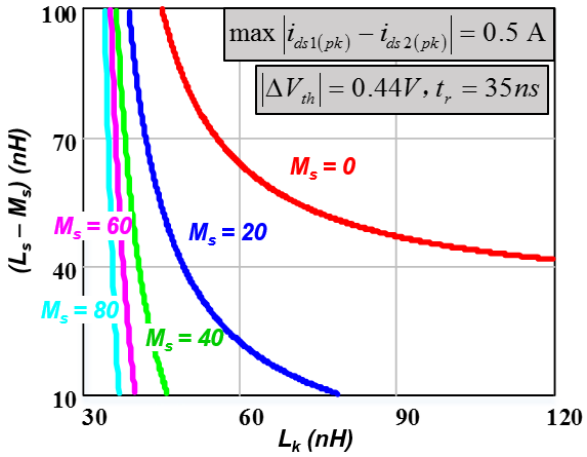


Fig. 2-37. Trajectories of ($L_s - M_s$) and L_k calculated by (2-54) with different mutual inductances.

2.6 Experimental Verification

In this section, the effectiveness of all the aforementioned passive balancing structures, including L_k//L_s, R_k//L_s, R_k//coupled L_s, coupled L_k//L_s, and L_k// coupled L_s, will be experimentally verified. The measurement methods of drain-source currents will be identified to obtain the mismatch of channel currents which could not be measured directly. Discrete and coupled inductors will be designed, manufactured, and measured to realize the passive solutions. The same hardware will be used for fair comparison of the baseline design and the balancing design.

2.6.1 Measurement of Drain-Source Currents

The measurement method of drain-source current needs to be determined before testing. The channel current of MOSFET cannot be measured directly. It can be approximated by source current i_s or drain current i_d, as shown in Fig. 2-39. The source current is usually measured because it is ground-referenced. Simple current sensor without isolation capability can be used. The sensing resistor [83],[84] and co-axial shunt [85],[86] are popular choices for accuracy. However, current imbalance may not appear in the measured i_{s1} and i_{s2} waveforms. One example is shown in Fig. 2-38, where the mismatch of channel currents caused by the difference in threshold voltages is clearly shown. Current Δi_{ds} is the sum of Δi_s and Δi_k. Most of the differential current flows though drive loop when L_k is much smaller than L_s, as depicted in Fig. 2-39. According to (2-17), ($V_{s1} - V_{s2}$) is determined by inductance $L_k//L_s$ and difference of channel current slew rates:

$$V_{s1} - V_{s2} = \frac{L_s L_k}{L_s + L_k}\left(\frac{di_{ds1}}{dt} - \frac{di_{ds2}}{dt}\right) \tag{2-55}$$

For the simulation in Fig. 2-38, L_k = 0.5 nH and L_s = 20 nH resulting in a minor difference between V_{s1} and V_{s2}. Based on (2-55), the difference between slew rates of source currents is given by

$$\frac{di_{s1}}{dt} - \frac{di_{s2}}{dt} = \frac{V_{s1} - V_{s2}}{L_s} = \frac{L_k}{L_s + L_k}\left(\frac{di_{ds1}}{dt} - \frac{di_{ds2}}{dt}\right) \tag{2-56}$$

According to (2-56), the difference of channel current slew rates is greatly weakened by small L_k and large L_s, leading to matched source currents. The differential current is flowing though drive-source inductances instead and circulating in the loop illustrated by Fig. 2-39. Another

example is shown in Fig. 2-18(a), where all the current difference will circulate though drive-source paths.

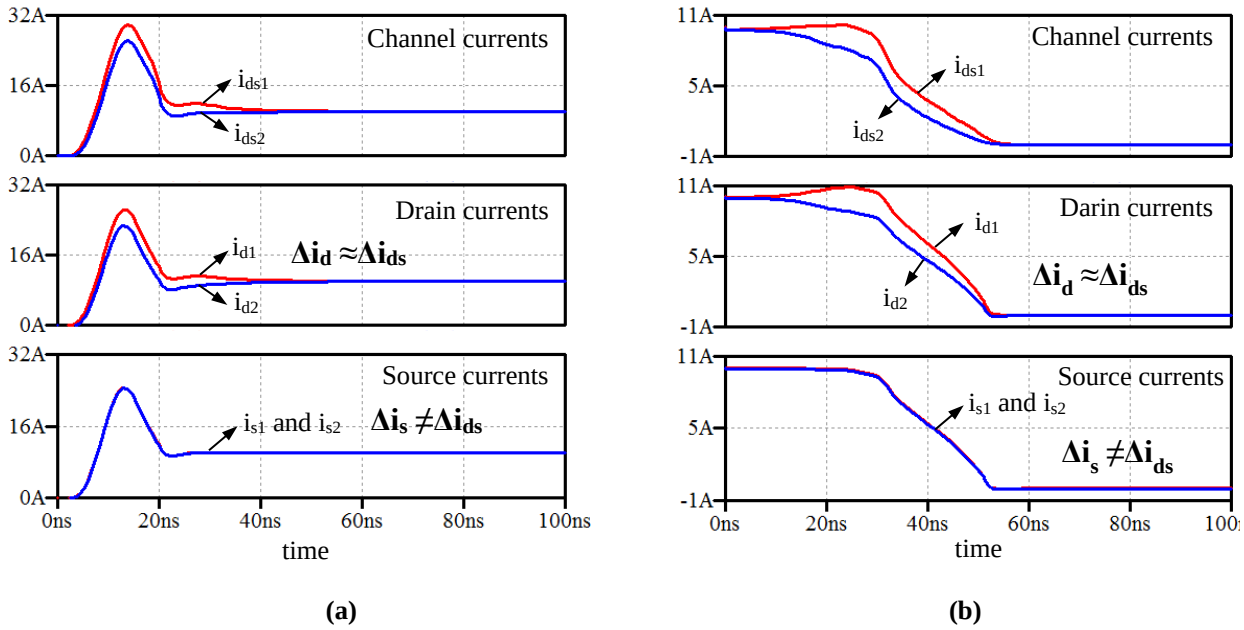


Fig. 2-38. Comparison of channel currents, drain currents and source currents (defined in Fig. 2-39) with L_k = 0.5 nH, L_s = 20 nH, and all the other inductances equal 0 nH. (a) Turn-on transient. (b) Turn-off transient.

However, similar imbalance is captured by drain currents. Absolute drain current is slightly smaller than channel current during turn-on transients and slightly larger than channel current during turn-off transients because of the displacement currents of parasitic inductances. However, current difference Δi_{ds} can be approximated by Δi_d thanks to the negligible difference of displacement currents from C_{ds} and C_{gd} between paralleled MOSFETs. The current rise time may be as small as 10 ns. The bandwidth of current probe should be higher than 100 MHz to accurately capture switching waveforms. The peak current may be as high as 25 A. The split core current probe (TCP0030A) [87] with 30 A dynamic range and 120 MHz bandwidth was used in the experiment.

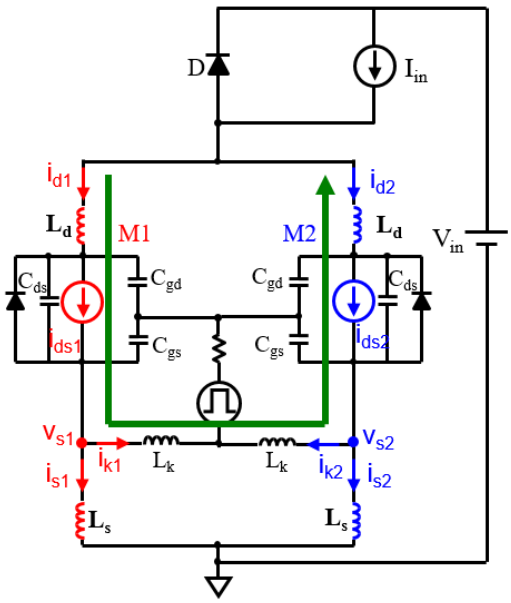


Fig. 2-39. Origin of measurement inaccuracy at source terminal.

Fig. 2-40 shows the layout of PCB for the measurement of drain-source currents. Two cutouts were designed around every drain trace for insertion of split core current probe, which provides isolation and has the capability of measuring DC current.

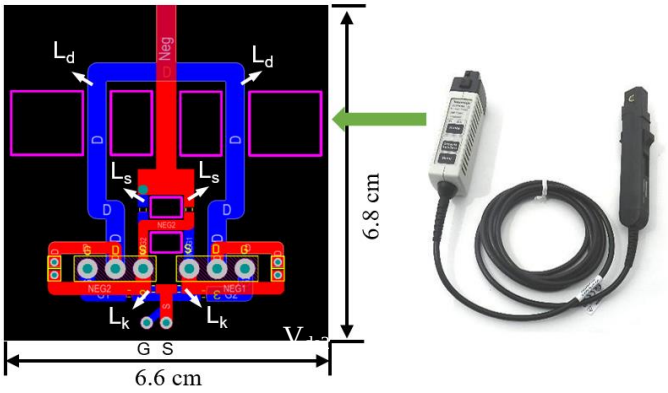


Fig. 2-40. Layout of PCB for measurement of drain currents.

Drain-source voltages are also measured for the calculation of switching energy. Specifications of probes (which have enough dynamic range and bandwidth) are summarized in Table 2-2. Propagation delays and DC offsets among those four probes are eliminated by a resistive load circuit before measurement to obtain accurate switching loss [89].

Table 2-2. Summary of probes utilized for measurement

Types	Models	Dynamic Range	Bandwidth	Rise time
Differential voltage probe	THDP0200 [88]	1500 V	200 MHz	< 1.8 ns
Split core current probe	TCP0030A [87]	30 A	120 MHz	< 2.92 ns

2.6.2 Baseline Test

Fig. 2-41 shows the double-pulse tester fabricated for the demonstration of dynamic balancing solutions. SiC MOSFETs were C2M0160120D rated at 1200 V, 19A, and 160 mΩ [33]. Their threshold voltages were found to be 2.34 V and 2.78 V by measurement set up described in [90]. The SiC diode was C4D20120A rated at 1200 V and 25.5 A [82]. Gate driver board was CRD-001 with 1700 V isolation voltage and 9 A peak output current [91]. The drain-source voltages were measured by differential voltage probe THDP0200. The 15.6 mm × 17.5 mm cutouts for insertion of two TCP0030A current probes add 26 nH to the drain inductance L_d and 120 nH (from copper traces and equivalent series inductances of dc-link capacitors) to the power-loop inductance L_p. Those parasitics were purposely not reduced to verify the performance of design guidelines under an awful layout. The ringings predicted in Fig. 2-30(b) (dashed waveforms) and measured in later experiments originate from these inductances, not from the balancing solutions. The same board was utilized for fair comparison of baseline and passive balancing solutions. The only difference was the designed parts. Openings on the power-source and drive-source traces were prepared for insertion of extra inductors or resistors. For baseline design, 0 Ω resistors were soldered to short

the openings. For verification of the passive balancing effect, inductors and/or resistors with designed values were inserted. Small L_k (1.89 nH based on Q3D simulation [92]) from the PCB layout ensured limited initial balancing effect. The impedance of drive source was dominated by inserted R_k or L_k.

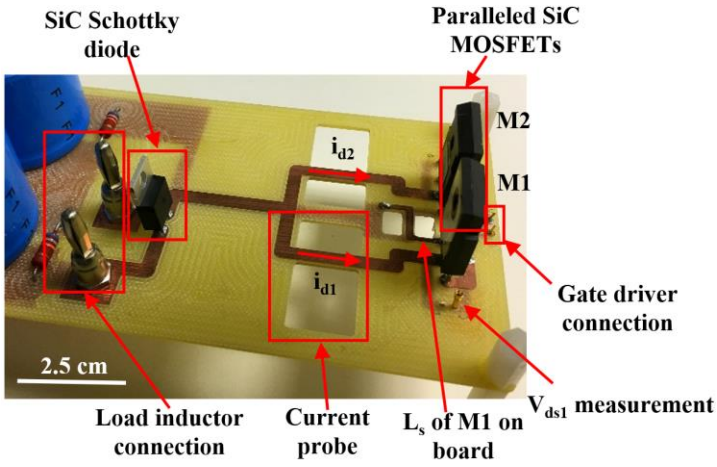


Fig. 2-41. Hardware for the demonstration of current balancing method.

The DPT tests two short pulses. The switching transients were captured at the first falling and rising edges at room temperature (with negligible change in junction temperatures). The experimental results of the baseline design are shown in Fig. 2-42. The corresponding on-board L_s and L_k (obtained by Q3D simulation) are illustrated in Table 2-3. The resulting effective current balancing inductance L_s // L_k is 3.4 nH, which is too small to achieve good sharing. The mismatch between the peak currents is 15.7 A – 14.2 A = 1.5 A, or 15% of the steady-state drain current. The voltage stress is 457 V. The current rise time t_r is 35 ns and will be used later for current balancing design. The large stray inductances associated with the expansion of layout for current measurement generate ringings that are not normally observed in a compact circuit board.

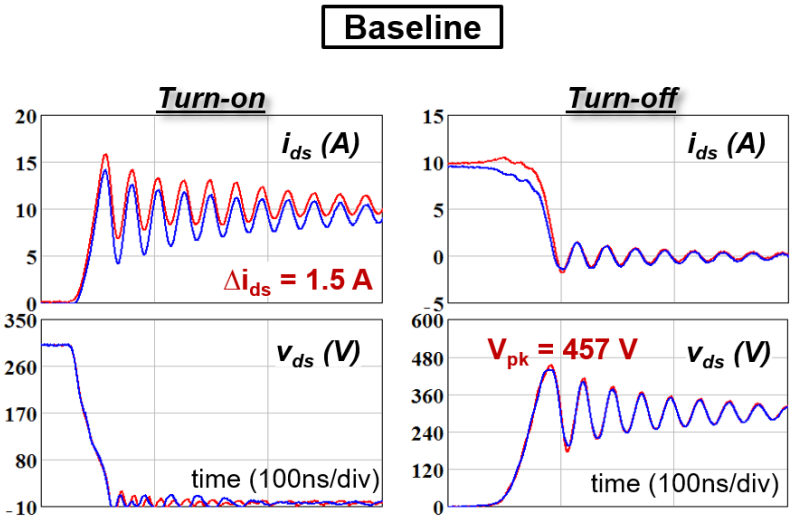


Fig. 2-42. Experimental results of baseline design (shown in Fig. 2-41 and Table 2-3) tested at V_{in} = 300 V, I_{in} = 20 A, $R_g + 0.5R_{ks}$ = 20 Ω, V_{th1} = 2.34 V, and V_{th2} = 2.78 V.

Table 2-3. Inductance and resistance on power- and drive-source traces for baseline test in Fig. 2-42

L_s (nH)	L_k (nH)	R_k (Ω)
11.5	1.89	0

2.6.3 Design and Fabrication of Discrete and Coupled Inductors

The discrete inductors employed in passive balancing structures are realized by small air-cored inductors. A photo of hardware for the verification of passive balancing structure L_s//L_k in Fig. 2-11 and passive balancing structure L_s//R_k in Fig. 2-16 is shown in Fig. 2-43. Small L_k (1.89 nH based on Q3D simulation) from the PCB layout ensures limited initial balancing effect. The drive-source impedance will be dominated by the inserted L_k or R_k. The same board is utilized for fair comparison of baseline and passive balancing solutions. The only difference is the designed parts: L_s, L_k, and/or R_k. Openings on the drive- and power-source traces are prepared for insertion of extra inductors or resistors. For baseline design, 0 Ω resistors are utilized to short the openings.

For verification of the passive balancing effect, small air-cored inductors and SMD resistors with designed values are inserted. In Fig. 2-43, two air-cored inductors with the same inductance are employed to increase the power-source inductance. One is placed on the top of the board, the other one is on the bottom and blocked by the board. Drive-source inductances/resistances are varied by air-cored inductors/surface mount resistors, which are also on the bottom of the board.

The comparison of L_s, L_k, and R_k for baseline design, passive balancing design $L_s//L_k$ in Fig. 2-11, and passive balancing design $L_s//R_k$ in Fig. 2-16 is shown in Table 2-4. Based on design guideline (2-23), the difference of peak currents can be bounded within 5% of $0.5I_{in}$ (namely 0.5 A) by designed $L_s//L_k$:

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{L_s // L_k} t_r = \frac{0.44V}{35.7\,nH} 35ns = 0.431A < 0.5\,A \tag{2-57}$$

Based on design guideline (2-30), the difference of peak currents can also be bounded within 5% of $0.5I_{in}$ (namely 0.5 A) by designed $L_s//R_k$:

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{R_k} + \frac{\left|\Delta V_{th}\right|}{L_s} t_r = \frac{0.44V}{5.6\,\Omega} + \frac{0.44V}{47nH} 35ns = 0.406\,A < 0.5\,A \tag{2-58}$$

where current rise time t_r = 35 ns is obtained by baseline test shown in Fig. 2-42 and ΔV_{th} = 0.44 V is achieved by measurements.

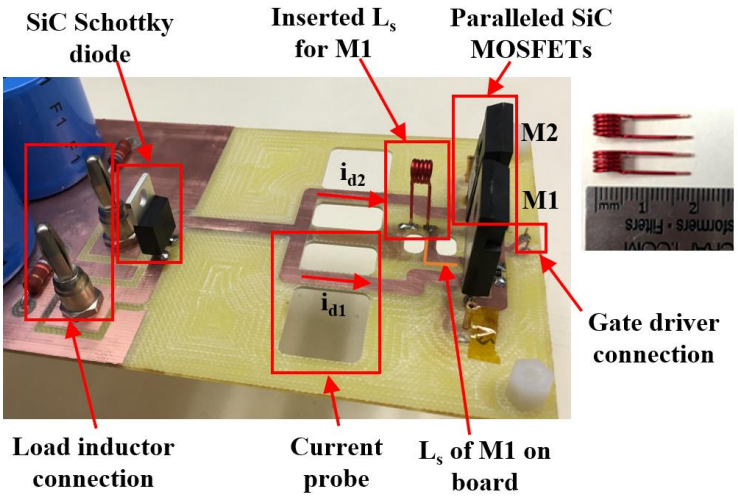


Fig. 2-43. Photo of hardware for the verification of passive balancing structure L_s//L_k in Fig. 2-11 and passive balancing structure L_s//R_k in Fig. 2-16. Air-cored inductors are utilized to change L_s and L_k. Surface mount resistors are utilized to change R_k.

Table 2-4. Comparison of L_s, L_k, and R_k for baseline design, passive balancing design L_s//L_k in Fig. 2-11, and passive balancing design L_s//R_k in Fig. 2-16

	Baseline	Balancing design in Fig. 2-11	Balancing design in Fig. 2-16
L_s (nH)	11.5	88.5	47.2
L_k (nH)	4.9	59.9	4.9
R_k (Ω)	0	0	5.6

A realization of negatively coupled inductors is shown in Fig. 2-44(a) using air core. Each inductor comprises a "solenoidal winding" and two "leads". The solenoidal windings were wound bifilarly since finite-element simulation suggested such a construction would yield $M_s \approx L_s$. Preliminary coil radius r, coil length l, and wire diameter d (all in inches), as well as the number of turns n, were selected using [93]

$$M_{sole} \approx L_{sole} \approx \frac{(r+0.5d)^2 n^2}{9(r+0.5d)+10l}\ \mu\text{H} \tag{2-59}$$

where coil radius r, coil length l, and wire diameter d are defined in Fig. 2-44(a).

The inductance L_{lead} of each lead was estimated from lead length l_{lead} (in meters) by [94]

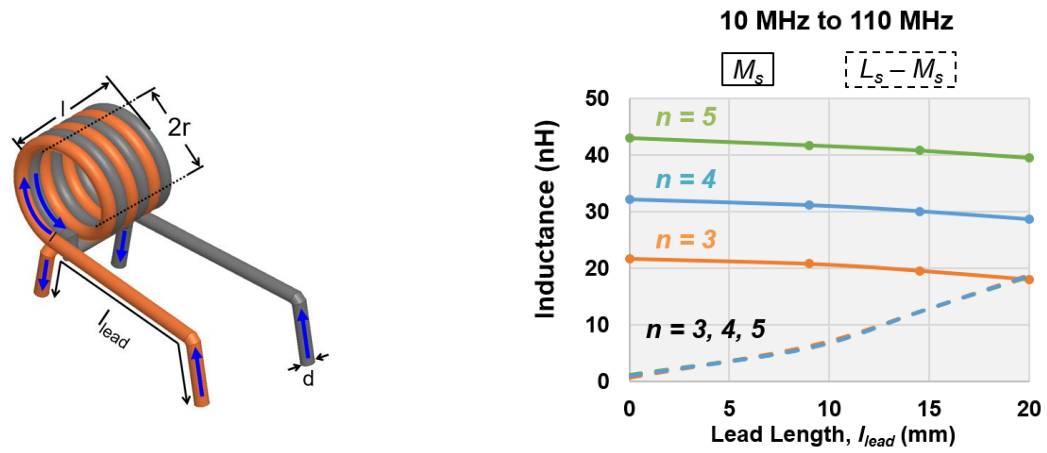
$$L_{lead} \approx 0.2 l_{lead}\left(\ln\frac{4l_{lead}}{d} - 0.75\right)\mu\text{H} \tag{2-60}$$

Preliminary inductances M_s and L_s - M_s were estimated from M_{sole} in (2-59) and L_{lead} in (2-60) by

$$M_s \approx M_{sole}, L_s - M_s \approx L_{lead} \tag{2-61}$$

The preliminary design of coupled inductors for passive balancing structure R_k//coupled L_s in Fig. 2-25 was iterated using finite-element simulation. The impacts of the number of solenoidal turns and the lead length on M_s and L_s - M_s are summarized in Fig. 2-44(b). Equations (2-59) and (2-60) yield M_s = 25 nH and L_s - M_s = 11 nH at low frequency for the design point and numbers shown in Fig. 2-44(a). The corresponding values from finite-element simulation were M_s = 19.8 nH and L_s – M_s = 12 nH between 10 MHz to 110 MHz. This design point yielded reasonable R_k to limit current mismatch below 5% and stress-inducing inductance which was comparable to the baseline test.

The drive-source resistance R_k was chosen according to (2-49). If the resulting R_k exceeds R_{kmax} specified by the designer, i.e., switching speed will be reduced even with R_g = 0 Ω, L_s + M_s needs be increased, e.g., by adding more turns.



(a) **(b)**

Fig. 2-44. (a) Air-cored negatively-coupled inductors with r = 1.9 mm, n = 3, and l_{lead} = 14.5 mm, and (b) mutual inductance M_s (>0) and stress-inducing inductance ($L_s - M_s$) for different turns number n and lead length l_{lead} simulated in the range of 10 MHz to 110 MHz with r = 1.9 mm.

Coupled inductors were made to demonstrate the passive balancing solution R_k//coupled L_s in Fig. 2-25 with k < 0. The photo of negatively-coupled inductors L_{s1} and L_{s2} is illustrated in Fig. 2-45. Two copper wires were wound and interleaved together. Terminal 1 and 3 are for L_{s1}; Terminal 2 and 4 are for L_{s2}. The arrows indicate the directions of currents during switching transient. The layout of power loop is shown in Fig. 2-46(a). The original power-source traces were replaced by coupled inductors. The photo of hardware with the negatively-coupled power-source inductors is shown in Fig. 2-46(b). The terminals of L_{s1} and L_{s2} in Fig. 2-45 were twisted and trimmed to fit the connections. The detail dimensions are shown in Fig. 2-44 (a).

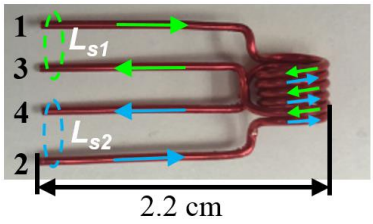
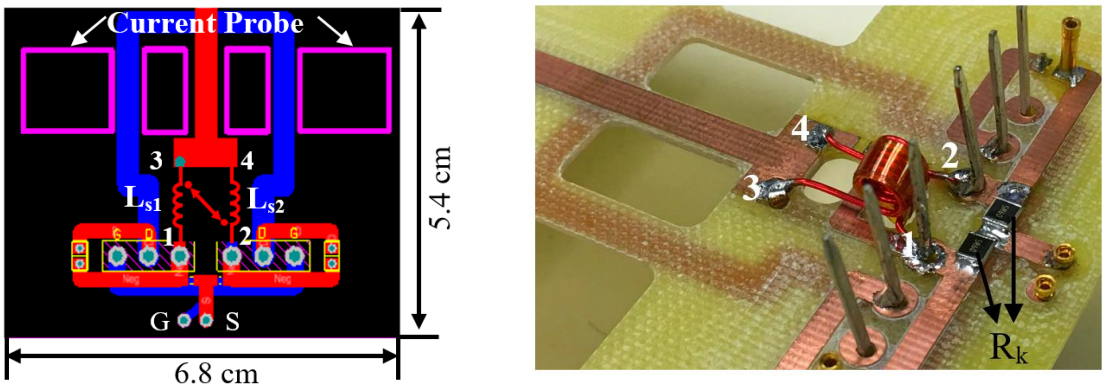


Fig. 2-45. Fabricated coupled inductors.

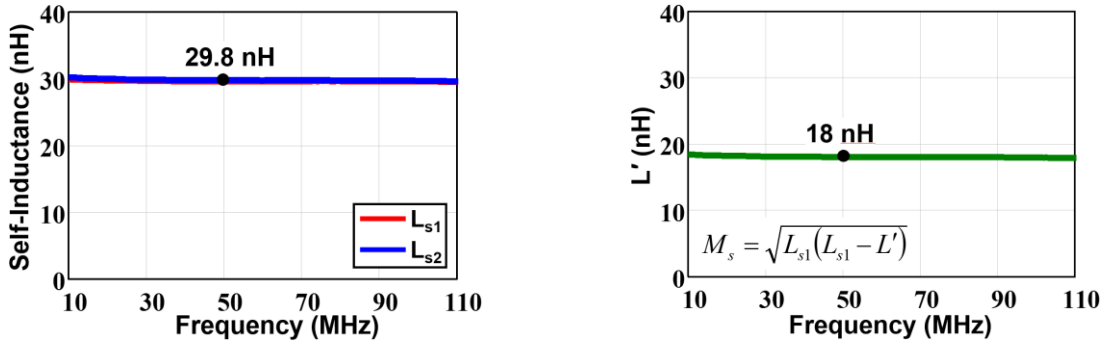


(a) **(b)**

Fig. 2-46. (a) Layout of power loop with inserted coupled power-source inductors; (b) photo of hardware inserted with the designed coupled power-source inductors and drive-source resistors for verification of passive balancing structure R_k//coupled L_s in Fig. 2-25.

The inductances of coupled inductors in Fig. 2-46(b) were measured by impedance analyzer and plotted in Fig. 2-47. The self-inductance which was measured by opening one port (e.g., 1 and 3) and measuring from the other one (e.g., 2 and 4) is shown in Fig. 2-47(a). The two self-inductances have similar values and don't change significantly between 10 MHz and 110 MHz, the practical range of ringing frequencies. The value at 50 MHz (which is the ringing frequency observed in the experiment) was used in the design. The measured intermediate inductance for the calculation of mutual inductance is shown in Fig. 2-47(b). It was measured by shorting one port and measuring from the other one. This curve is also stable between 10 MHz and 110 MHz. The mutual inductance is then calculated by $M_s = \sqrt{L_{s1}(L_{s1} - L')}$. The corresponding M_s and $L_s - M_s$

are 18.8 nH and 11 nH, respectively. They are close to the simulation shown in Fig. 2-44(b).



(a) **(b)**

Fig. 2-47. Measurement results of impedance analyzer over wide frequency range. (a) Measured self-inductances; (b) measured intermediate inductance for the calculation of mutual inductance.

The specific values of L_s, M_s, and R_k for passive balancing design coupled $L_s//R_k$ in Fig. 2-25 are shown in Table 2-5. The stress-inducing inductance (L_s – M_s) is 11 nH, which is close to baseline design. The same R_k = 5.6 Ω as passive balancing design $L_s//R_k$ was selected for convenient comparison between structures with and without magnetic coupling. According to (2-49), the difference of peak currents can be bounded within 5% of $0.5I_{in}$ (namely 0.5 A) by designed coupled $L_s//R_k$:

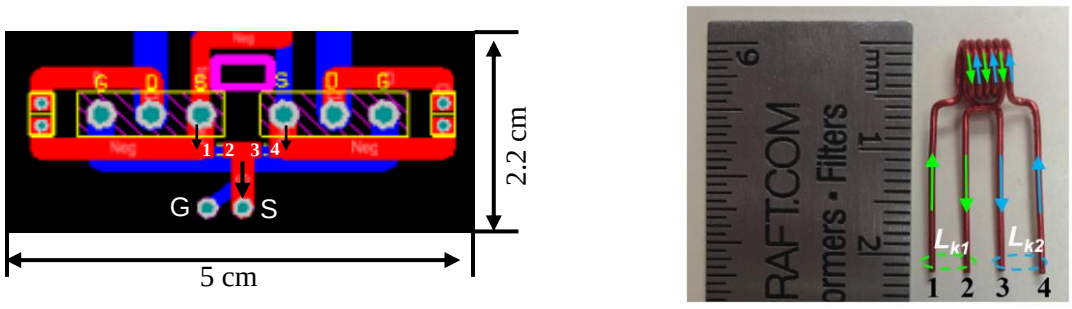
$$\begin{aligned}\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| &= \frac{V_{th2} - V_{th1}}{R_k} + \frac{V_{th2} - V_{th1}}{L_s + M_s} t_r \\ &= \frac{0.44V}{5.6\Omega} + \frac{0.44V}{48.6nH} 35ns = 0.395A < 0.5A\end{aligned} \tag{2-62}$$

where current rise time t_r = 35 ns is obtained by baseline test shown in Fig. 2-42 and ΔV_{th} = 0.44 V is achieved by measurements.

Table 2-5. Comparison of L_s, M_s, and R_k between baseline design and passive balancing design coupled L_s//R_k in Fig. 2-25

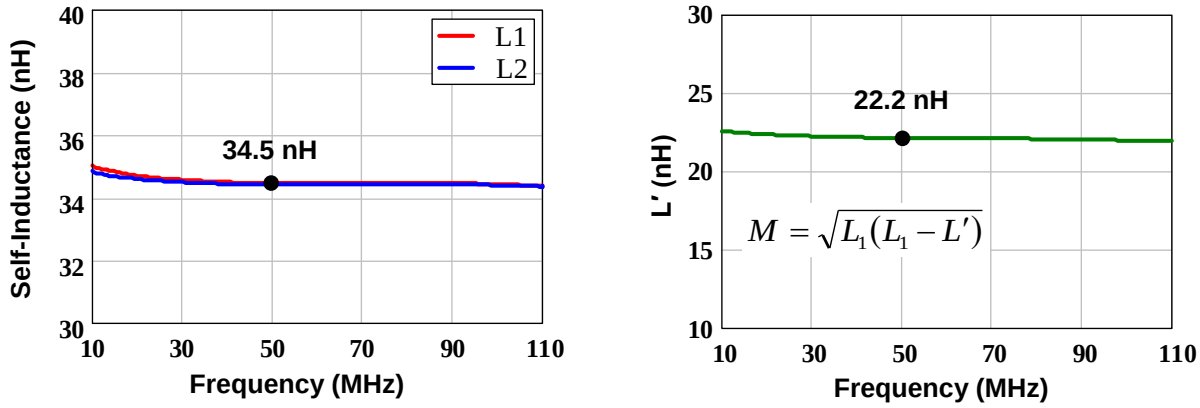
	Baseline	Balancing design in Fig. 2-25
L_s (nH)	11.5	29.8
M_s (nH)	0	18.8
R_k (Ω)	0	5.6

Following the same method, the coupled inductors for passive balancing structure L_s//coupled L_k in Fig. 2-34 was designed and manufactured. The layout of gate loop is shown in Fig. 2-48(a), where G" and "S" represent the ports for the connection of gate driver. Openings on drive-sources traces are purposely left for insertion of coupled inductors. The arrows indicate the directions of currents during turn-on transient. Fig. 2-48(b) shows the photo of designed negatively coupled inductors. The measurement results of impedance analyzer are plotted in Fig. 2-49. The two self-inductances have similar values and don't change significantly between 10 MHz and 110 MHz, the practical range of ringing frequencies. The value at 50 MHz (which is the ringing frequency observed in the experiment) was used in the design. The measured intermediate inductance for the calculation of mutual inductance is shown in Fig. 2-49(b). This curve is also stable between 10 MHz and 110 MHz. The mutual inductance is then calculated by $M_k = \sqrt{L_{k1}\left(L_{k1} - L'\right)}$.



(a) **(b)**

Fig. 2-48. (a) Layout of gate loop for insertion of coupled inductor; (b) photo of designed coupled inductors for passive balancing structure L_s//coupled L_k in Fig. 2-34.



(a) **(b)**

Fig. 2-49. Measurement results of impedance analyzer over wide frequency range. (a) Measured self-inductances; (b) measured intermediate inductance for calculation of mutual inductance.

According to Fig. 2-49 and Q3D simulation, the resulting L_k and M_k are calculated as

$$L_k = L_1 + L_{pcb} = 34.5 + 4.89 = 39.4\,nH \tag{2-63}$$

$$M_k = \sqrt{L_1(L_1 - L')} = 20.6\,nH \tag{2-64}$$

The specific values of L_s, L_k, and M_k for passive balancing design L_s//coupled L_k in Fig. 2-34 are shown in Table 2-6. The same L_s = 88.5 nH as balancing design L_s//L_k in Table 2-4 was selected for convenient comparison between structures with and without magnetic coupling. According to (2-52), the difference of peak currents can be bounded within 5% of $0.5I_{in}$ (namely 0.5 A) by designed L_s//coupled L_k:

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{V_{th2} - V_{th1}}{L_s // (L_k + M_k)} t_r = \frac{0.44V}{36nH} 35\,ns = 0.428\,A < 0.5\,A \tag{2-65}$$

where current rise time t_r = 35 ns is obtained by baseline test shown in Fig. 2-42 and ΔV_{th} = 0.44 V is achieved by measurements.

Table 2-6. Comparison of L_s, L_k, and M_k between baseline design and passive balancing design L_s//coupled L_k in Fig. 2-34

	Baseline	Balancing design in Fig. 2-34
L_s (nH)	11.5	88.5
L_k (nH)	4.9	39.4
M_k (nH)	0	20.6

The coupled inductors for passive balancing structure coupled L_s//L_k in Fig. 2-36 was designed and manufactured. The original power-source traces were replaced by coupled inductors as shown in Fig. 2-46(a). The photo of hardware inserted with the designed negatively-coupled power-source inductors is shown in Fig. 2-50. The inductances of coupled inductors were measured by impedance analyzer and plotted in Fig. 2-51. The two self-inductances have similar values and don't change significantly between 10 MHz and 110 MHz. The value at 50 MHz (which is the ringing frequency observed in the experiment) was used in the design. The measured intermediate inductance for the calculation of mutual inductance is shown in Fig. 2-51(b). This curve is also stable between 10 MHz and 110 MHz. The mutual inductance is then calculated by $M_s = \sqrt{L_{s1}(L_{s1} - L')}$.

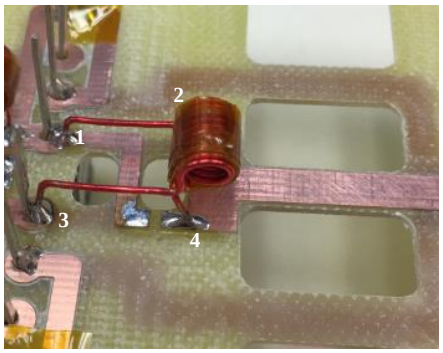
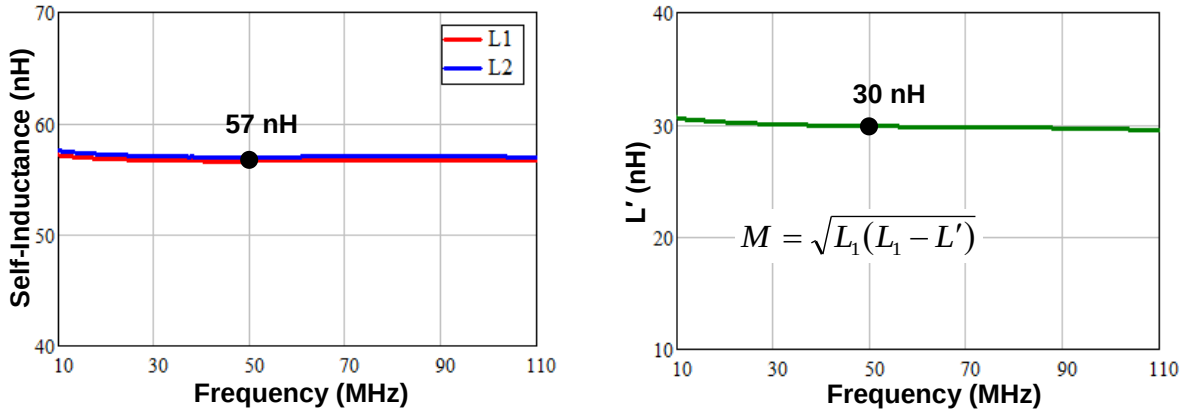


Fig. 2-50. Photo of hardware inserted with the designed coupled power-source inductors for verification of passive balancing structure coupled L_s//L_k in Fig. 2-36.



(a) **(b)**

Fig. 2-51. Measurement results of impedance analyzer over wide frequency range. (a) Measured self-inductances; (b) measured intermediate inductance for calculation of mutual inductance.

According to Fig. 2-51, the resulting L_s and M_s are calculated as

$$L_s = L_1 = L_2 = 57nH \tag{2-66}$$

$$M_s = \sqrt{L_1(L_1 - L')} = 39.3nH \tag{2-67}$$

The specific values of L_s, M_s, and L_k for passive balancing solution coupled L_s//L_k in Fig. 2-36 are shown in Table 2-7. The same L_k = 59.9 nH as balancing design L_s//L_k in Table 2-4 was selected for convenient comparison between structures with and without magnetic coupling. According to (2-54), the difference of peak currents can be bounded within 5% of $0.5I_{in}$ (namely 0.5 A) by designed coupled L_s// L_k:

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{V_{th2} - V_{th1}}{(L_s + M_s)// L_{ks}} t_r = \frac{0.44V}{37nH} 35ns = 0.416A < 0.5A \tag{2-68}$$

where current rise time t_r = 35 ns is obtained by baseline test shown in Fig. 2-42 and ΔV_{th} = 0.44 V is achieved by measurements.

Table 2-7. Comparison of L_s, M_s, and L_k between baseline design and passive balancing design coupled L_s//L_k in Fig. 2-36

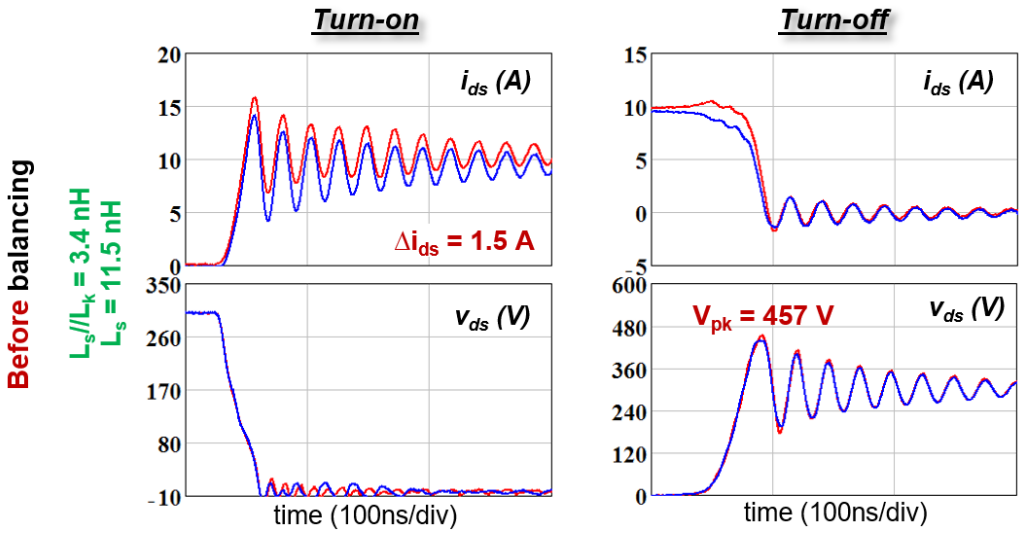
	Baseline	Balancing design in Fig. 2-36
L_s (nH)	11.5	57.0
M_s (nH)	0	39.3
L_k (nH)	4.9	59.9

2.6.4 Experimental Results

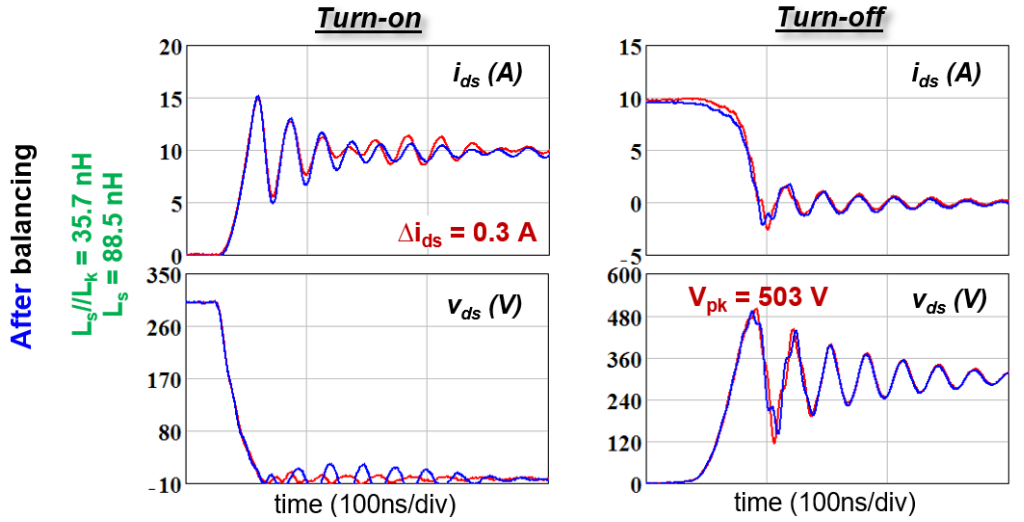
The same test board (shown in Fig. 2-41), MOSFETs (with V_{th1} = 2.34 V and V_{th2} = 2.48 V), and test conditions (i.e. V_{in} = 300 V, I_{in} = 20 A, R_g = 20 Ω) are employed for the baseline test in Fig. 2-42 and verification of passive balancing solutions shown in Fig. 2-11 (L_s//L_k), Fig. 2-16 (L_s//R_k), Fig. 2-25 (coupled L_s//R_k), Fig. 2-34 (L_s//coupled L_k), and Fig. 2-36 (coupled L_s//L_k) to achieve fair comparison among them. The only differences are the impedances on power-source and drive-source traces, as shown in Table 2-4, Table 2-5, Table 2-6, and Table 2-7. The prototype in Fig. 2-41 has relatively large power-loop inductance (around 120 nH from copper traces and ESLs of DC link capacitors) and drain inductance (around 26 nH) due to the accommodation of current probes. Those parasitics were not purposely reduced to verify the performance of design guidelines under an awful layout.

The Fig. 2-52 shows the comparison of test results between baseline design (shown in Fig. 2-52(a)) and passive balancing solution in Fig. 2-11 (L_s//L_k) (shown in Fig. 2-52(b)). The measured difference of peak currents is reduced from 1.5 A to 0.3 A. The desired current sharing (< 5% of steady-state drain current = 0.5 A) is obtained by a single gate driver from the first switching cycle as demonstrated by the double-pulse test which captures switching transients at the first falling and rising edges. The design guideline (2-23) upholds well when parasitics are considered. Much

better sharing is also achieved for the turn-off transient compared to the baseline shown in Fig. 2-52(a). The increased L_s doesn't worsen the ringing but increases the voltage stress during turn-off transient by 46 V.



(a)

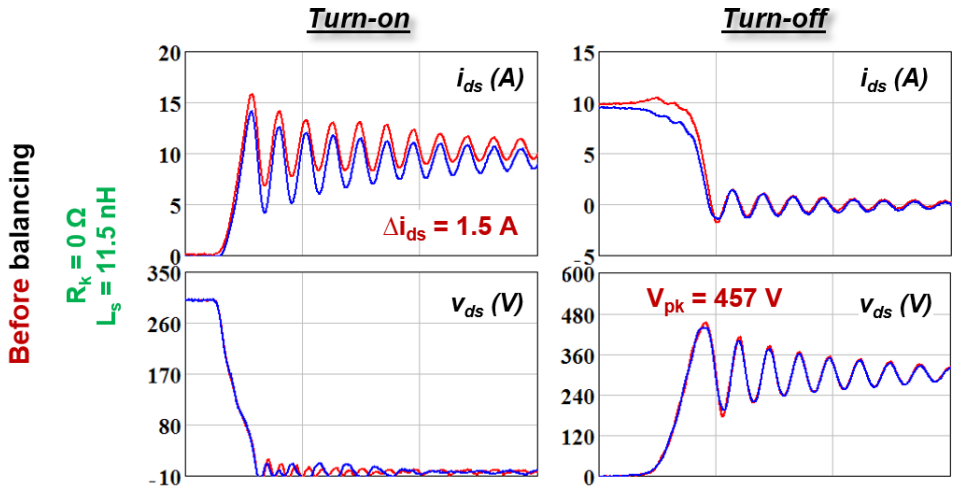


(b)

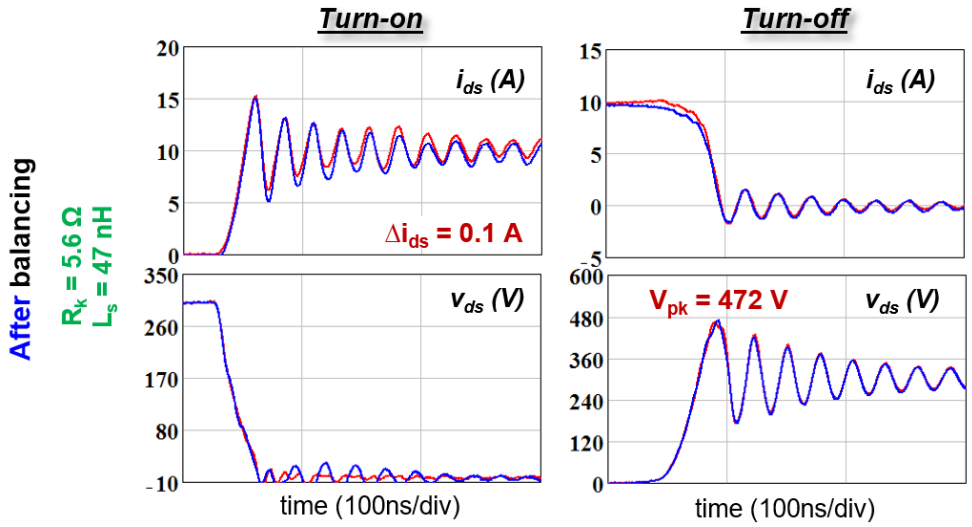
Fig. 2-52. Experimental verification of current balancing solution in Fig. 2-11 (L_s//L_k). (a) Switching transients of baseline design, and (b) switching transients with designed L_s and L_k. Test conditions are V_{in} = 300 V, I_{in} = 20 A, R_g = 20 Ω, V_{th1} = 2.34 V, and V_{th2} = 2.78 V. The passive components are shown in Table 2-4.

Fig. 2-53 shows the comparison of test results between baseline design and the passive balancing solution in Fig. 2-16 (L_s//R_k). The air-cored drive-source inductors employed in Fig. 2-52 are replaced by surface mount resistors. The corresponding L_s and R_k are illustrated in Table 2-4. According to the comparison, the measured difference of peak currents is reduced from 1.5 A to 0.1 A by a single gate driver from the first switching cycle. The effectiveness of design guideline (2-30) with the existence of parasitics is verified. Much better sharing is also achieved for the turn-off transient compared to the baseline shown in Fig. 2-53(a). The inserted L_s doesn't worsen the ringing but increases the voltage stress during turn-off transient by 15 V, which is smaller than Fig. 2-52(b) because less L_s is required for structure L_s//R_k.

Fig. 2-54 shows the comparison between design trajectory of solution L_k //L_s in Fig. 2-11 (blue line) and design trajectory of solution R_k //L_s in Fig. 2-16 (green line). The lower horizontal axis is L_k for structure L_k //L_s and the upper horizontal axis is R_k for structure R_k //L_s. The vertical axis is L_s, which is proportional with voltage stress. The two black dots show the design points of Fig. 2-52(b) and Fig. 2-53(b). According to the comparison, less L_s is required for structure R_k //L_s than L_k //L_s for the same balancing effect, resulting in a smaller voltage stress.



(a)



(b)

Fig. 2-53. Experimental verification of current balancing solution in Fig. 2-16 (L_s//R_k). (a) Switching transients of baseline design, and (b) switching transients with designed L_s and R_k. Test conditions are V_{in} = 300 V, I_{in} = 20 A, R_g = 20 Ω, V_{th1} = 2.34 V, and V_{th2} = 2.78 V. The passive components are shown in Table 2-4.

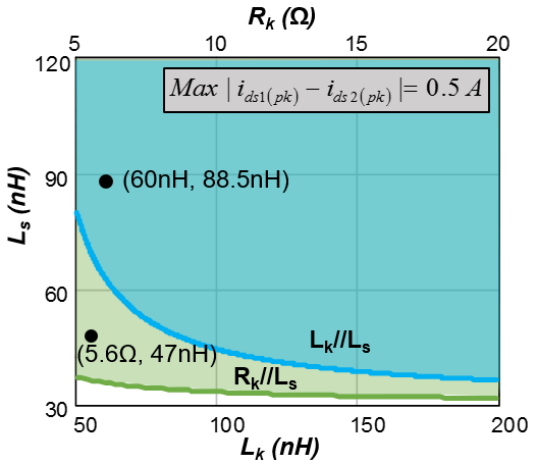


Fig. 2-54. Comparison between design trajectory of solution L_k//L_s (in Fig. 2-11) and design trajectory of solution R_k//L_s (in Fig. 2-16). The other conditions are $|\Delta V_{th}|$ = 0.44 V and t_r = 35 ns.

The Fig. 2-55 shows the comparison of test results between baseline design (shown in Fig. 2-55(a)) and passive balancing solution in Fig. 2-25 (coupled L_s//R_k) (shown in Fig. 2-55(b)). The air-cored discrete power-source inductors employed in Fig. 2-54 are replaced by negatively-

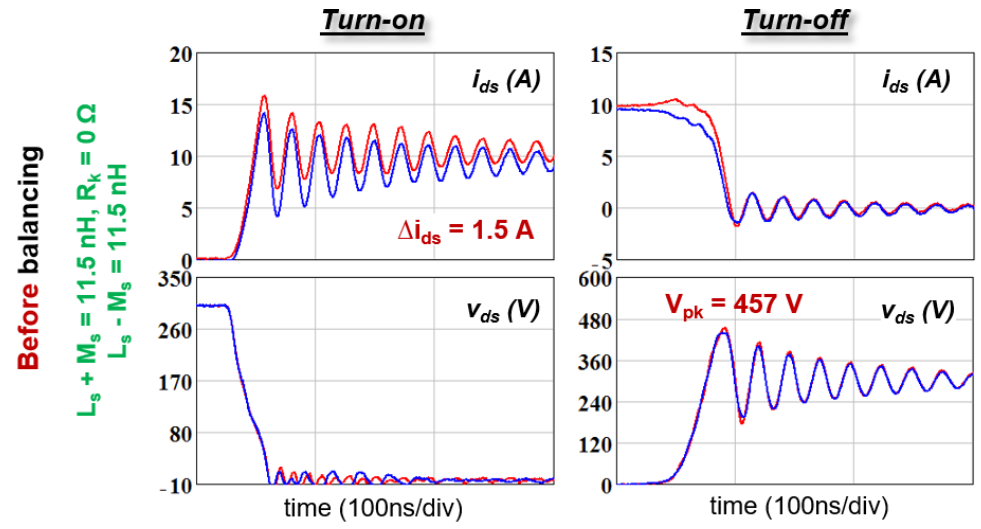
coupled power-source inductors (as shown in Fig. 2-46). The corresponding L_s, M_s, and R_k are designed by (2-49) and listed in Table 2-5.

Fig. 2-56 shows the trajectories of ($L_s - M_s$) and R_k calculated by (2-49) for different mutual inductances. The vertical axis is stress-inducing inductance ($L_s - M_s$), instead of current-balancing inductance ($L_s + M_s$), to reveal the impact of negative magnetic coupling on the reduction of voltage stress. The red dot and blue dot are design points of tests in Fig. 2-53 and Fig. 2-55, respectively. According to the comparison, less ($L_s - M_s$) is required for structure coupled $L_s//R_k$ than $L_s //R_k$ for the same balancing effect, resulting in a smaller voltage stress.

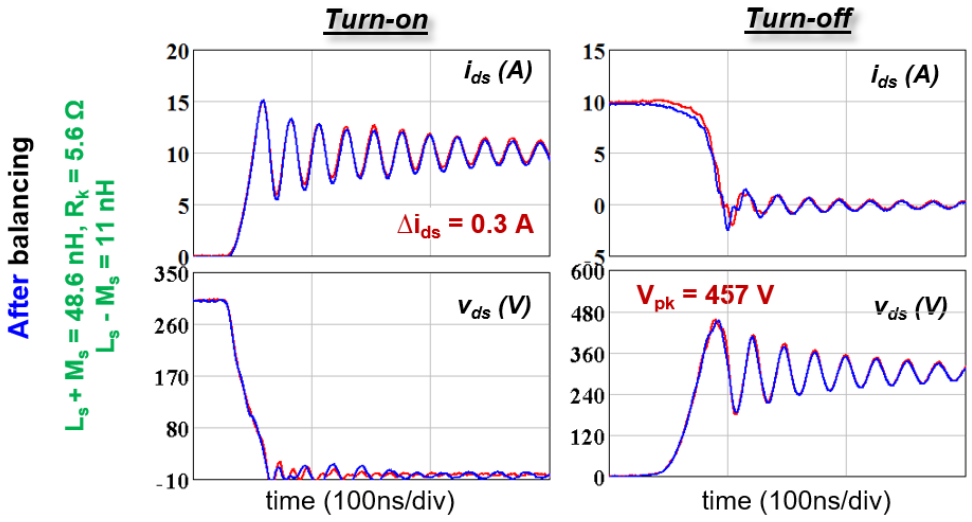
The tested switching transients with designed coupled L_s and R_k are shown in Fig. 2-55(b). The measured difference of peak currents is reduced from 1.5 A to 0.3 A. The desired current sharing (< 5% of steady-state drain current = 0.5 A) is obtained by a single gate driver from the first switching cycle as demonstrated by the double-pulse test which captures switching transients at the first falling and rising edges. The design guideline (2-49) upholds well when parasitics are considered. Much better sharing is also achieved for the turn-off transient compared to the baseline shown in Fig. 2-55(a). The same voltage stress as the baseline is achieved by the designed stress-inducing inductance ($L_s - M_s$). This inductance can be further reduced by trimming the lead length (as shown in Fig. 2-46).

A comprehensive comparison of test results shown in Fig. 2-55 is plotted in Fig. 2-57. The switching energies were calculated by the integration of instantaneous power ($i_{ds}*v_{ds}$) during turn-on and turn-off transients. The delays and DC offsets among two current probes and two voltage probes have been compensated to obtain accurate switching energy and energy difference. The

effectiveness of L_s, R_k, and M_s is demonstrated with negligible influence on total switching energy and voltage stress.



(a)



(b)

Fig. 2-55. Experimental verification of current balancing solution in Fig. 2-25 (coupled L_s//R_k). (a) Switching transients of baseline design, and (b) switching transients with designed coupled L_s and R_k. Test conditions are V_{in} = 300 V, I_{in} = 20 A, R_g = 20 Ω, V_{th1} = 2.34 V, and V_{th2} = 2.78 V. The passive components are shown in Table 2-5.

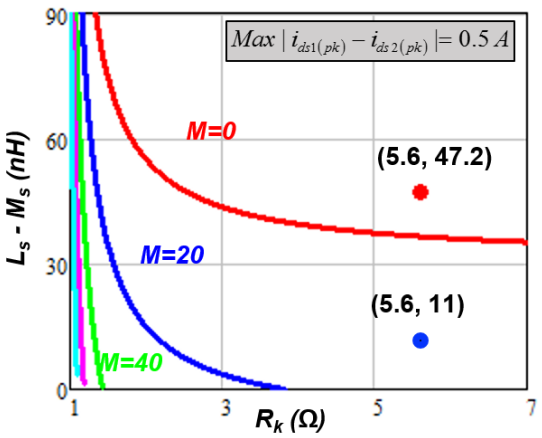


Fig. 2-56. Trajectories of (L_s – M_s) and R_k calculated by (2-49) for different mutual inductances. The red dot and blue dot are design points of tests in Fig. 2-53 and Fig. 2-55, respectively. The other conditions are max|$i_{ds1(pk)}$ - $i_{ds2(pk)}$| = 0.5 A, |ΔV_{th}| = 0.44 V, and t_r = 35 ns.

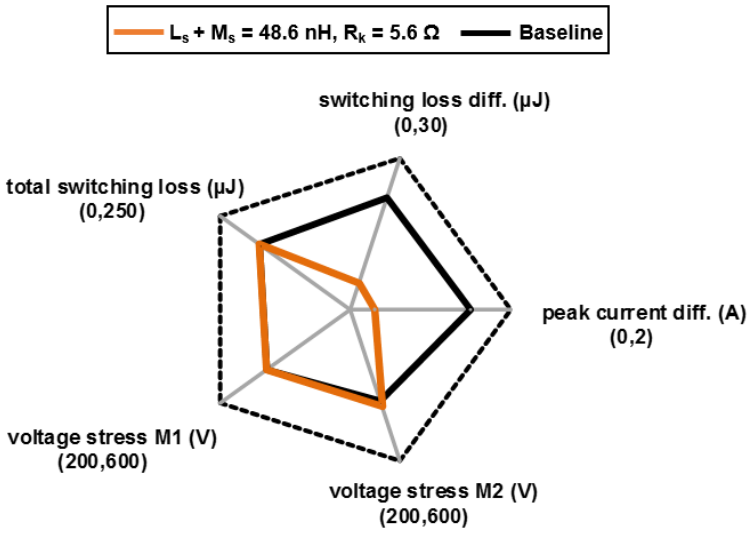
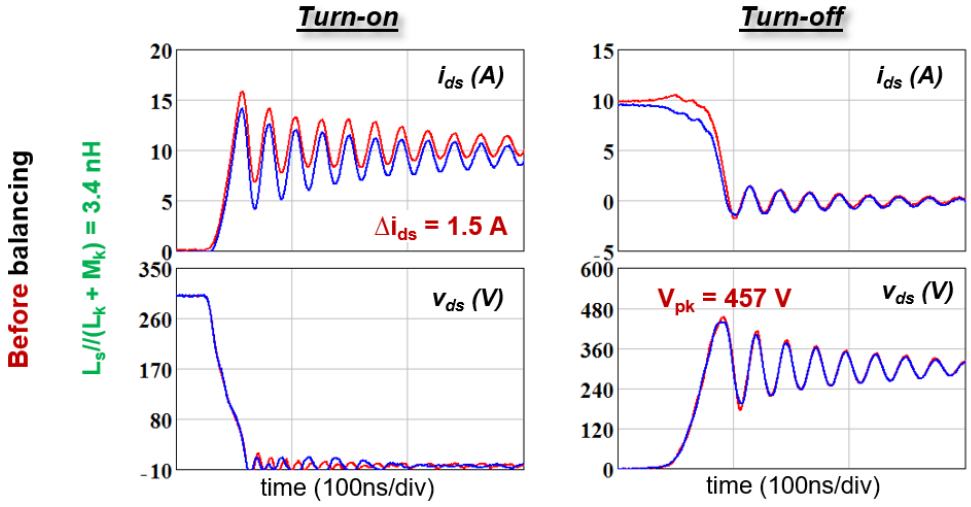


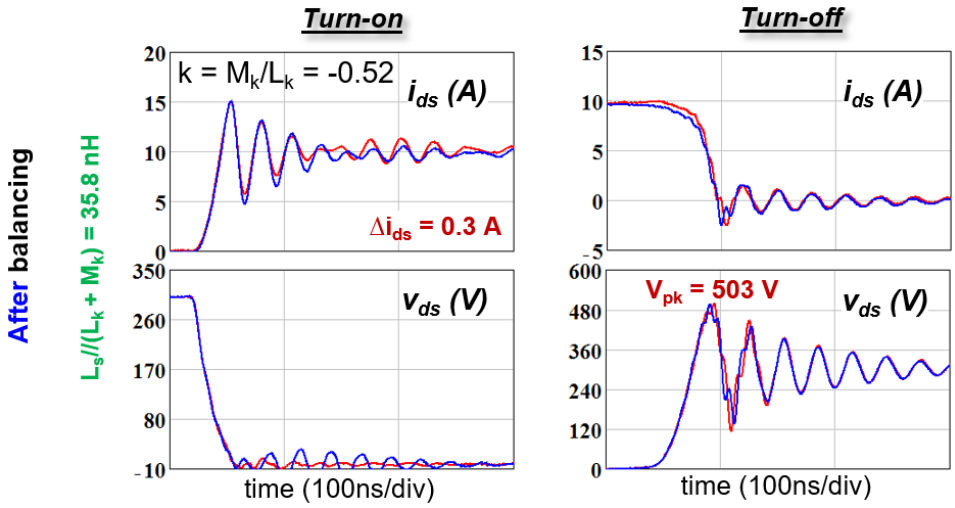
Fig. 2-57. Comprehensive comparison of test results shown in Fig. 2-55.

Fig. 2-58 shows the comparison of test results between baseline design (shown in Fig. 2-58(a)) and passive balancing solution in Fig. 2-34 (L_s//coupled L_k) (shown in Fig. 2-58(b)), where the discrete drive-source inductances used in Fig. 2-52(b) are replaced by coupled inductors (as shown in Fig. 2-48). The specific values are designed by (2-52) and listed in Table 2-6. According to Fig.

2-58, the measured difference of peak currents is reduced from 1.5 A to 0.3 A by a single gate driver from the first switching cycle. Much better sharing is also achieved for the turn-off transient. The effectiveness of design guideline (2-52) with the existence of parasitics is verified.



(a)



(b)

Fig. 2-58. Experimental verification of current balancing solution in Fig. 2-34 (L_s//coupled L_k). (a) Switching transients of baseline design, and (b) switching transients with designed L_s and coupled L_k. Test conditions are V_{in} = 300 V, I_{in} = 20 A, R_g = 20 Ω, V_{th1} = 2.34 V, and V_{th2} = 2.78 V. The passive components are shown in Table 2-6.

The design points of Fig. 2-52(b) (59.9, 88.5) and Fig. 2-58 (b) (39.4, 88.5) are also shown

Fig. 2-59. Less self-inductance L_k is required when two drive-source inductors are negatively coupled while keeping (L_k + M_k) the same. However, inductance on the drive loop has slight influence on sharing, voltage stress, and switching loss, as shown in Table 2-1. Test results in Fig. 2-52(b) and Fig. 2-58 (b) are very similar with each other since two designs have the same difference of peak currents and L_s. More comprehensive comparison is shown in Fig. 2-60 in terms of total switching loss, switching loss difference, peak current difference, and voltage stresses. Two lines exactly overlap with each other in the spider plot.

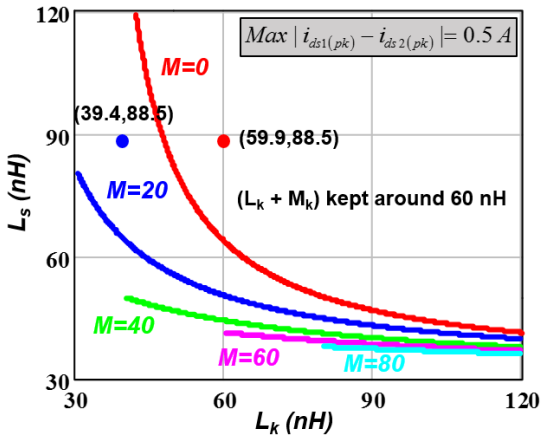


Fig. 2-59. Trajectories of L_s and L_k calculated by (2-52) for different mutual inductances. The red dot and blue dot are design points of tests in Fig. 2-52 and Fig. 2-58, respectively. The other conditions are $|\Delta V_{th}|$ = 0.44 V and t_r = 35 ns.

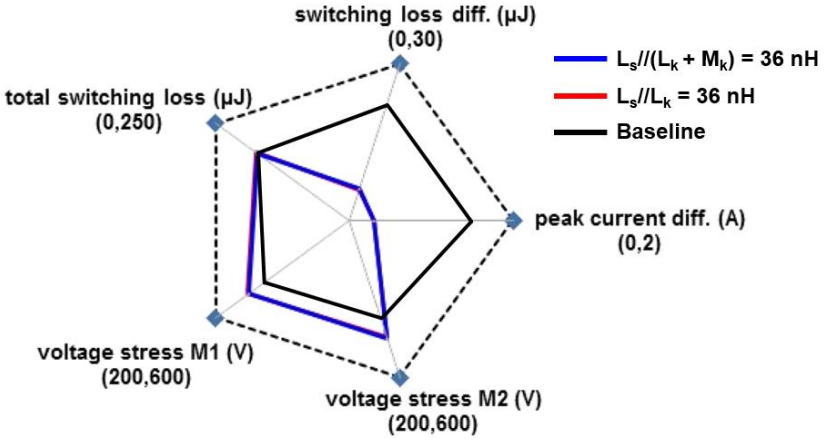


Fig. 2-60. Comprehensive comparison of test results shown in Fig. 2-52 and Fig. 2-58.

Even though Fig. 2-52(b) and Fig. 2-58 (b) show no difference between the two solutions, magnetic coupling can provide more design freedom. Fig. 2-61 illustrates another design of L_s//coupled L_k. Instead of moving horizontally (as the blue dot shown in Fig. 2-59), the design point is shifted vertically resulting in balanced current with less voltage stress.

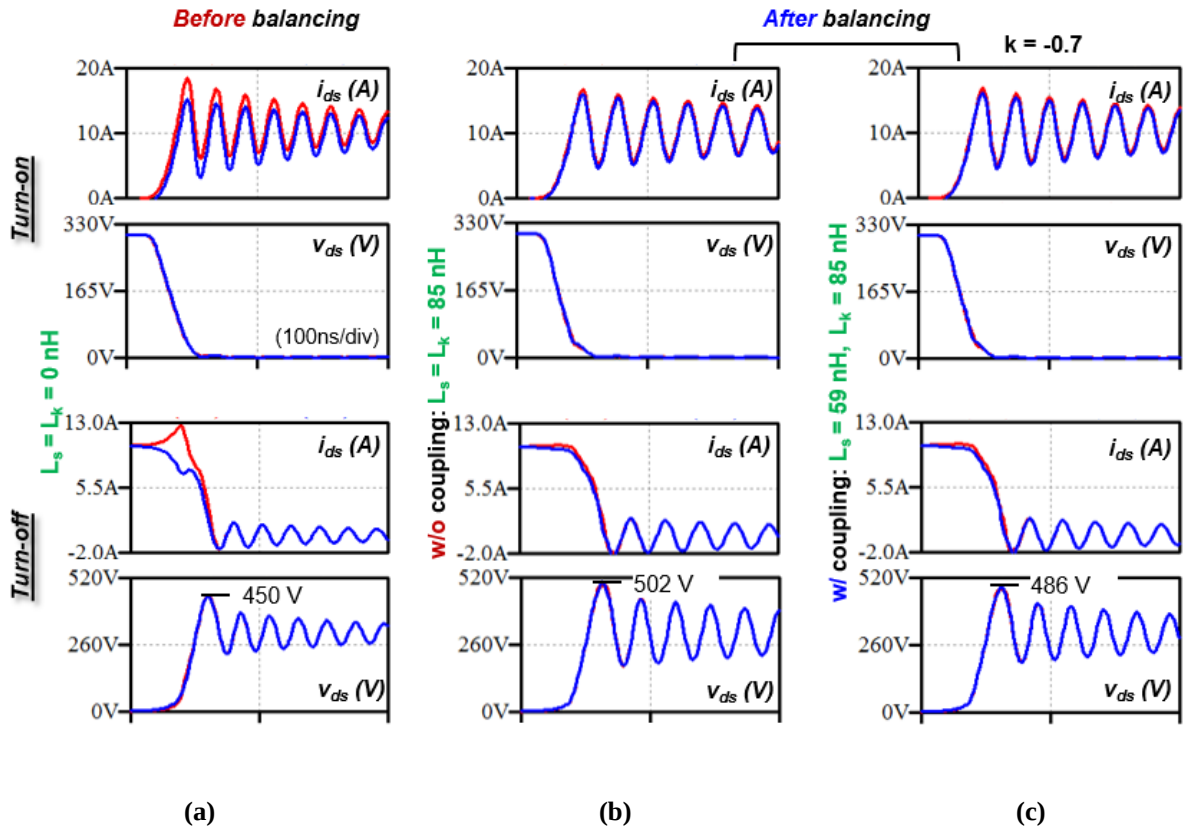
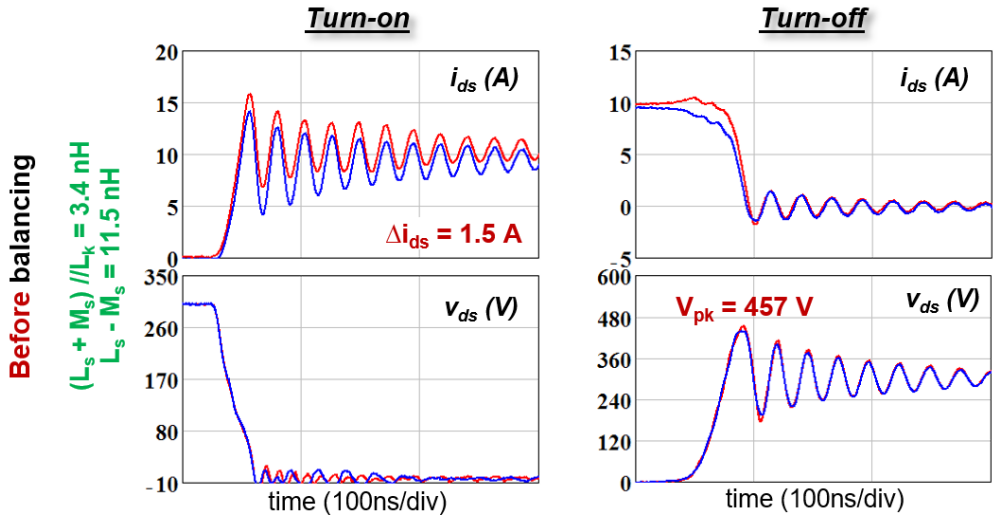


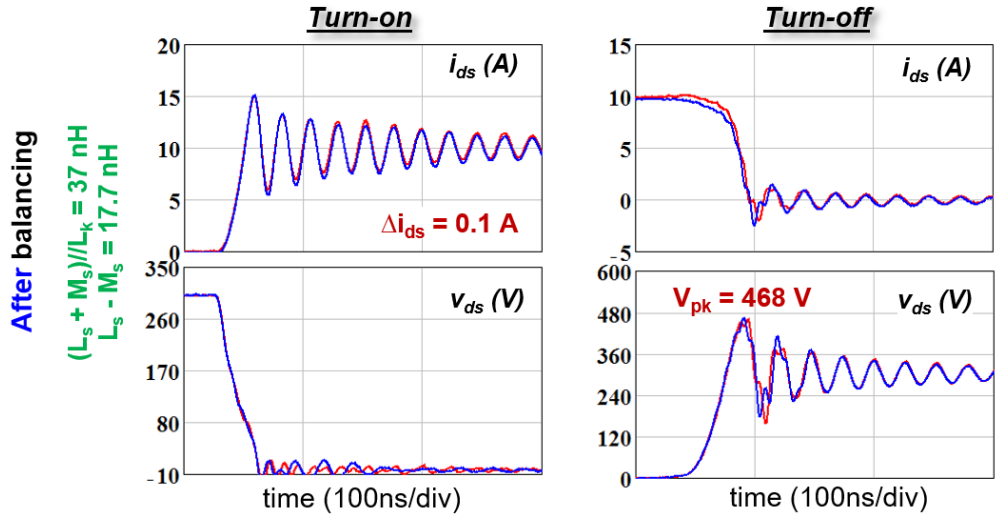
Fig. 2-61. Switching transients (a) before balancing ($L_s = L_k = 0$ nH); (b) after balancing without coupling ($L_s = L_k = 85$ nH); (c) after balancing with negatively-coupled L_k ($L_s = 59$ nH, $L_k = 85$ nH, $k = -0.7$).

Fig. 2-62 shows the comparison of test results between baseline design (shown in Fig. 2-62(a)) and passive balancing solution in Fig. 2-36 (coupled L_s//L_k) (shown in Fig. 2-62(b)), where the discrete power-source inductances used in Fig. 2-52(b) are replaced by coupled inductors (as shown in Fig. 2-50). The specific values are designed by (2-54) and listed in Table 2-7. According to Fig. 2-62, the measured difference of peak currents is reduced from 1.5 A to 0.1 A by a single

gate driver from the first switching cycle. Much better sharing is also achieved for the turn-off transient. The effectiveness of design guideline (2-54) with the existence of parasitics is verified.



(a)



(b)

Fig. 2-62. Experimental verification of current balancing solution in Fig. 2-36 (coupled $L_s//L_k$). (a) Switching transients of baseline design, and (b) switching transients with designed coupled L_s and L_k. Test conditions are V_{in} = 300 V, I_{in} = 20 A, R_g = 20 Ω, V_{th1} = 2.34 V, and V_{th2} = 2.78 V. The passive components are shown in Table 2-7.

The design points of Fig. 2-52(b) (59.9, 88.5) and Fig. 2-62(b) (59.9, 17.7) are also shown in

Fig. 2-63. According to the comparison, less stress-inducing inductance ($L_s - M_s$) is required when two power-source inductors are negatively coupled while keeping ($L_s + M_s$) the same, resulting in smaller voltage stress. More comprehensive comparison is shown in Fig. 2-64 in terms of total switching loss, switching loss difference, peak current difference, and voltage stresses. The effectiveness of L_s, M_s, and L_k is demonstrated with negligible influence on total switching energy and voltage stress.

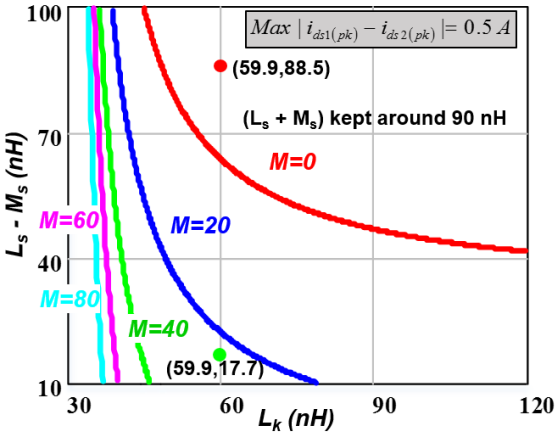


Fig. 2-63. Trajectories of ($L_s - M_s$) and L_k calculated by (2-54) for different mutual inductances. The red dot and green dot are design points of tests in Fig. 2-52 and Fig. 2-62Fig. 2-58, respectively. The other conditions are $|\Delta V_{th}|$ = 0.44 V and t_r = 35 ns.

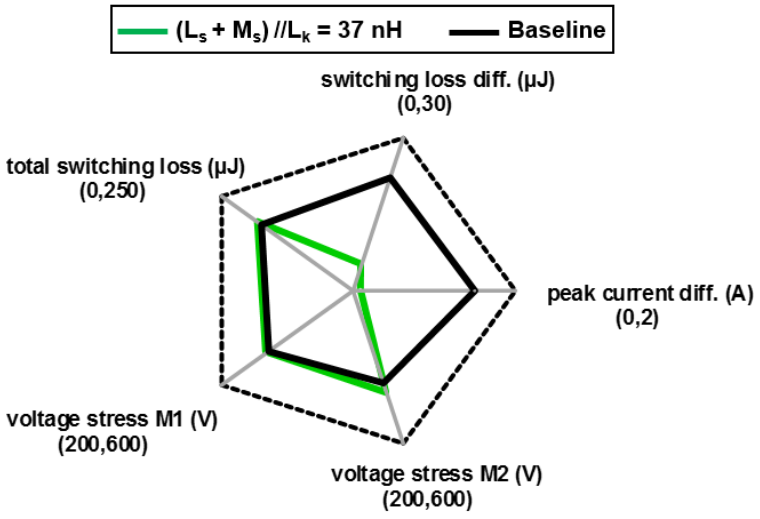


Fig. 2-64. Comprehensive comparison of test results shown in Fig. 2-62.

2.7 Effectiveness over A Wide Operating Range

The performance of current balancing solution was also investigated under different operating conditions (i.e., V_{in}, I_{in}, and R_g). The structure coupled L_s//R_k in Fig. 2-25 was employed in the tests. According to design guideline (2-49),

$$\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{R_k} + \frac{\left|\Delta V_{th}\right|}{L_s + M_s} t_r \tag{2-69}$$

Desired balancing performance for other operating conditions can be achieved with the same balancing designs (i.e., L_s, M_s, and R_k) and for the same MOSFETs (i.e., ΔV_{th}), if the resulting current rise time t_r is smaller than that of the conditions for which the passive components were designed.

The comparison of current rise time when one of I_{in}, V_{in}, and R_g is changed, while keeping the other conditions unchanged is shown in Fig. 2-65. Current rise time t_r rises with increasing input current I_{in} and gate resistance R_g, and droops a little with increasing input voltage V_{in}. This is also demonstrated in Appendix A. Thus, the designed L_s, M_s, and R_k for Fig. 2-55(b) should also provide balanced results under higher V_{in}, lower I_{in}, or lower R_g. The effectiveness of passive balancing solution over wide operating range is plotted in Fig. 2-66, where the dark blue region shows the effective area. The black dot shows the conditions that the passive components were designed for (as shown in Fig. 2-55(b)) and red dots are the conditions tested at for verification of effectiveness over the wide operating range.

The experimental results are shown in Fig. 2-67. Much better sharing was achieved for all the tests compared to the baseline shown in Fig. 2-42. The comparison of peak-current difference employing the same L_s, M_s, and R_k under different operating conditions are shown in Table 2-8.

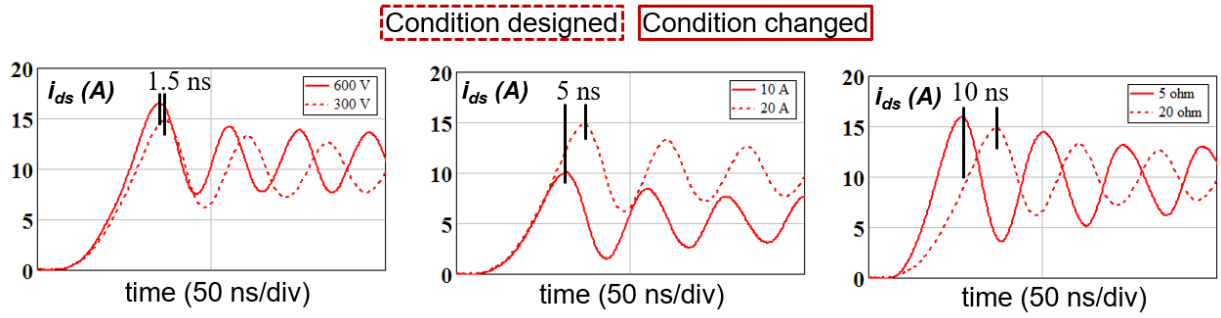


Fig. 2-65. Comparison of current rise time when one of I_{in}, V_{in}, and R_g is changed while keeping the other conditions the same.

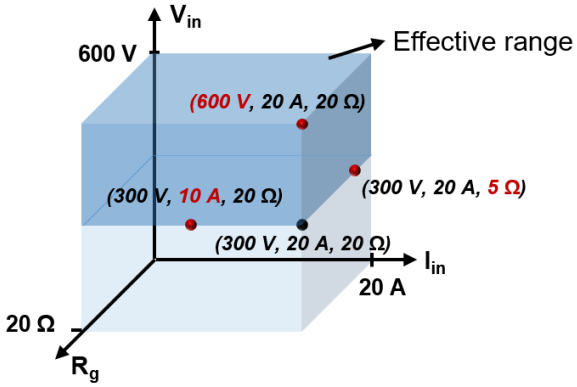
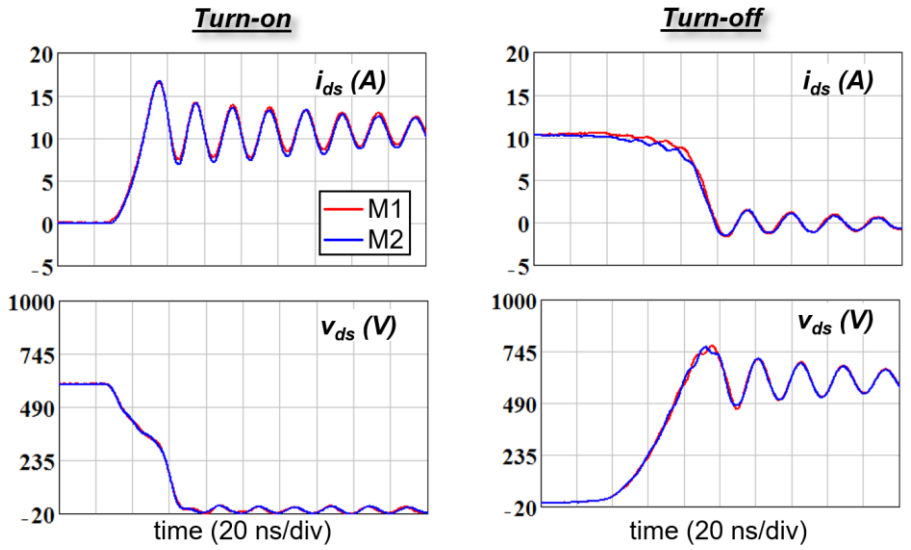
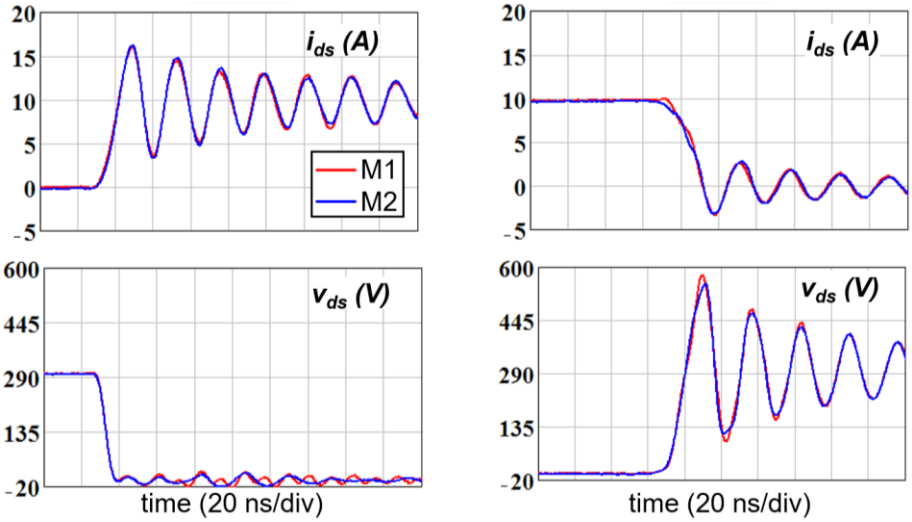


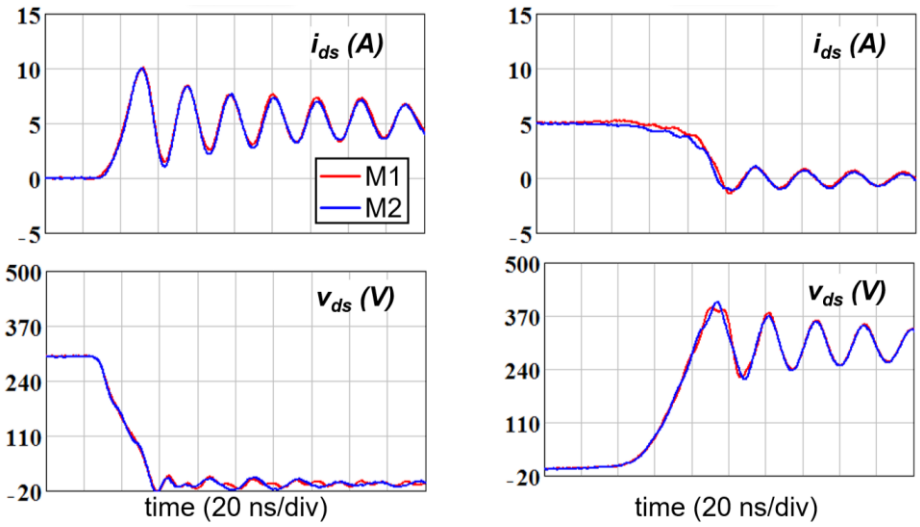
Fig. 2-66. Effectiveness of passive balancing solution over wide operating range, where black dot shows the conditions that passive components designed at. The dark blue region shows the effective range. The red dots are the conditions tested for verification, as shown in Fig. 2-67.


Turn-on
Turn-off
i_{ds} (A)
v_{ds} (V)
M1
M2
time (20 ns/div)

(a)


i_{ds} (A)
v_{ds} (V)
M1
M2
time (20 ns/div)

(b)



(c)

Fig. 2-67. Switching transients with balancing solution tested under (a) V_{in} = 600 V, I_{in} = 20 A, and $R_g + 0.5R_k$ = 20 Ω, (b) V_{in} = 300 V, I_{in} = 20 A, and $R_g + 0.5R_k$ = 5 Ω, and (c) V_{in} = 300 V, I_{in} = 10 A, and $R_g + 0.5R_k$ = 20 Ω for V_{th1} = 2.34 V and V_{th2} = 2.78 V.

Table 2-8. Comparison of peak-current difference employing the same L_s, M_s, and R_k under different operating conditions

Conditions	$\lvert i_{pk1(pk)} - i_{pk2(pk)} \rvert$ (A)
300 V, 20 A, 20 Ω	0.3
600 V, 20 A, 20 Ω	0.3
300 V, 10 A, 20 Ω	0
300 V, 20 A, 10 Ω	0.3

2.8 Comparison of Different Balancing Solutions

Five current balancing solutions are introduced in Section 2.3, Section 2.4, and Section2.5, as plotted in Fig. 2-68. They are named after structure characteristics. According to the experimental results shown in Fig. 2-52, Fig. 2-53, Fig. 2-58, Fig. 2-62, and Fig. 2-55, all of them can provide satisfying current sharing. Their corresponding design guidelines are summarized in Table 2-9. The upper bound of peak current difference can be controlled by the design of inductance, magnetic coupling, and resistance.

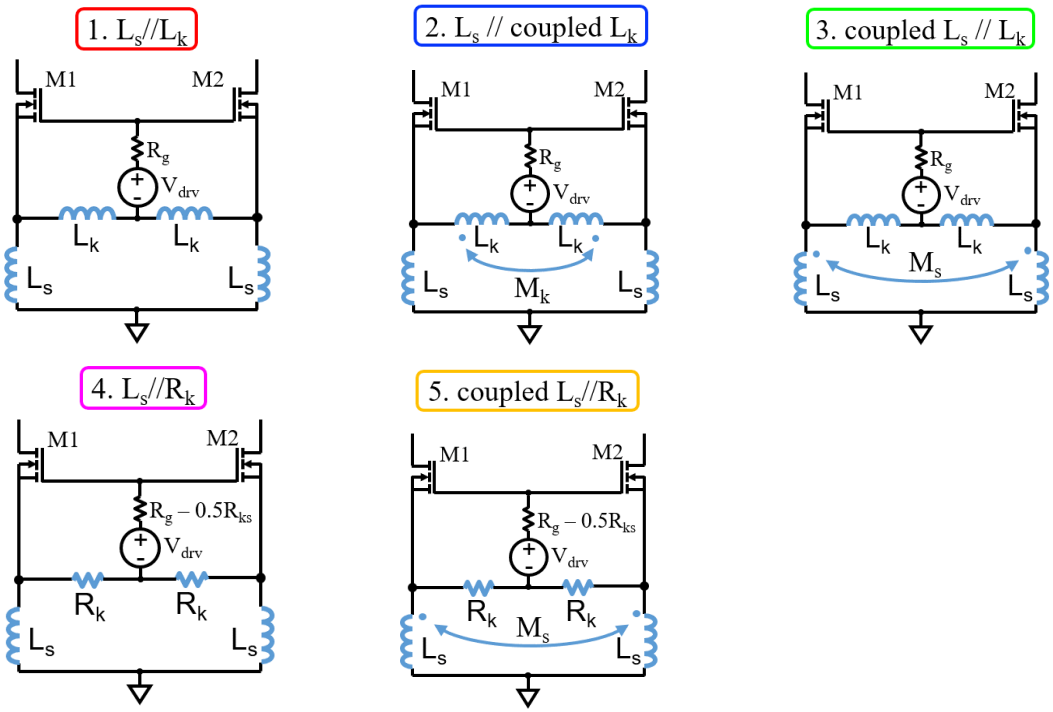


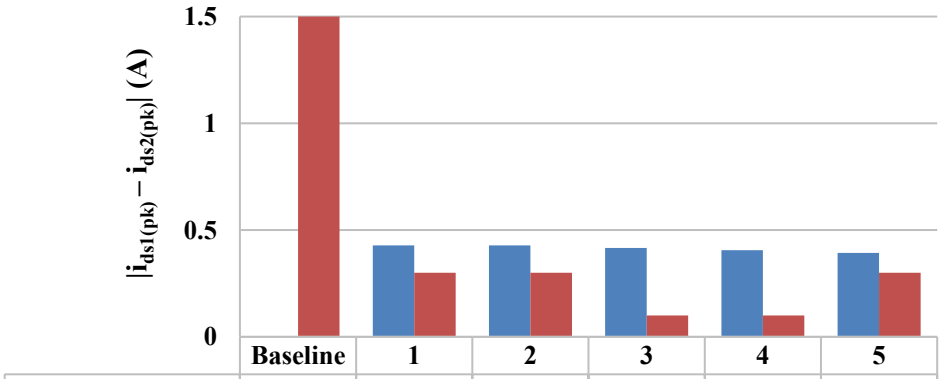
Fig. 2-68. Five current balancing solutions introduced in Section 2.3, Section 2.4, and Section2.5.

According to Table 2-9, the only difference among those design guidelines is the denominator. Current difference caused by V_{th} mismatch is directly damped by resistor R_k. Inductance reduces the increasing rate of current difference. Mutual inductance enhances balancing effect and adds to the corresponding self-inductance though negative coupling.

Table 2-9. Summary of design guidelines for different balancing solutions shown in Fig. 2-68

Configuration	$\text{Max}\lvert i_{ds1(pk)} - i_{ds2(pk)}\rvert$
1. L_s // L_k	$\frac{\lvert\Delta V_{th}\rvert}{L_s // L_k} t_r$
2. L_s //coupled L_k	$\frac{\lvert\Delta V_{th}\rvert}{L_s // (L_k + M_k)} t_r$
3. coupled L_s // L_k	$\frac{\lvert\Delta V_{th}\rvert}{(L_s + M_s) // L_k} t_r$
4. L_s // R_k	$\frac{\lvert\Delta V_{th}\rvert}{R_k} + \frac{\lvert\Delta V_{th}\rvert}{L_s} t_r$
4. coupled L_s // R_k	$\frac{\lvert\Delta V_{th}\rvert}{R_k} + \frac{\lvert\Delta V_{th}\rvert}{L_s + M_s} t_r$

Comparison between calculated and measured differences of peak currents is shown in Fig. 2-69, where numbers correspond to the structures in Fig. 2-68. The guidelines shown in Table 2-9 calculate the maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$. In other words, they are worst-case design guidelines. According to this figure, the measured differences of peak currents are well limited below 0.5 A, which are as expected. All the solutions have equal current balancing capability in current sharing point of view.



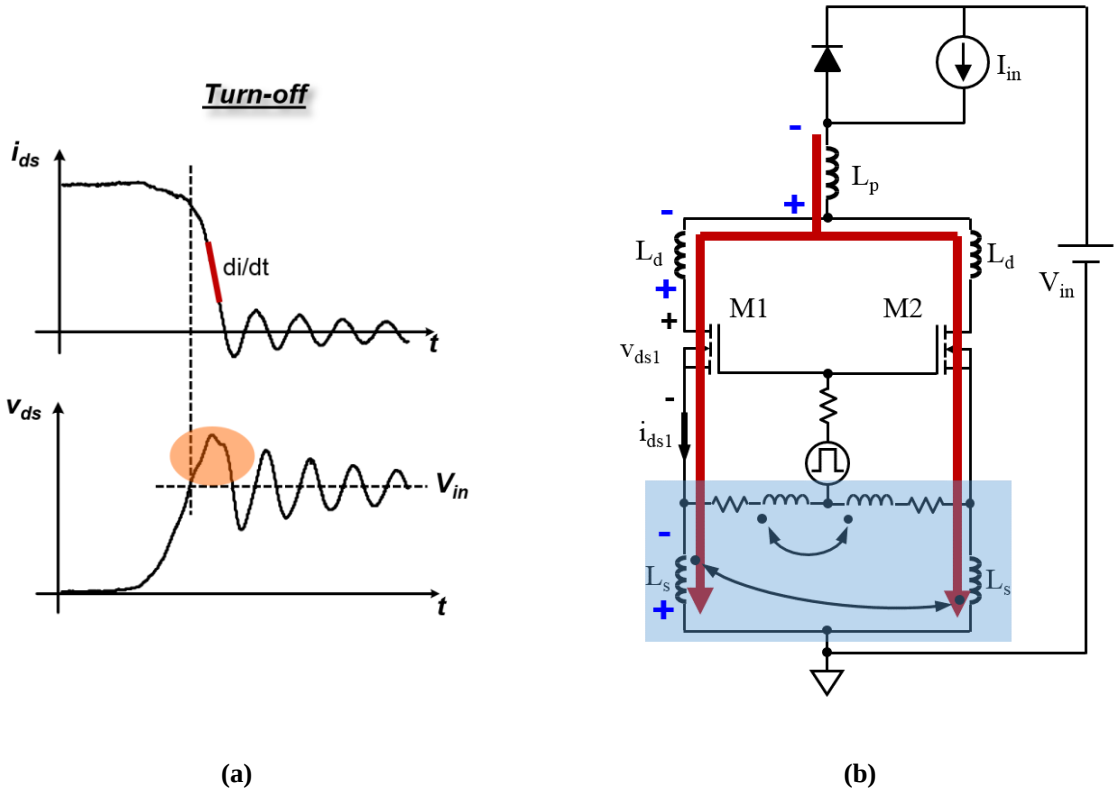
	Baseline	1	2	3	4	5
design (A)		0.428	0.428	0.416	0.406	0.393
Measurement (A)	1.5	0.3	0.3	0.1	0.1	0.3

Fig. 2-69. Comparison of peak current difference between calculation and measurement based on the experimental results shown in Fig. 2-52, Fig. 2-53, Fig. 2-58, Fig. 2-62, and Fig. 2-55.

Then, voltage stresses of different passive balancing solutions will be compared. The schematic in Fig. 2-70(b) includes all the parasitic inductances (except for L_{cm}) and lumps all the passive structures in Fig. 2-68 together, which are emphasized by the blue square. Negative current slew rate causes extra voltage stress during turn-off transient (as illustrated by the ellipse shown in Fig. 2-70(a)). According to Fig. 2-70(b), inductances contributing to this over-voltage are L_p, L_d, and L_s, among which, only L_s is varied by balancing design and is considered for the comparison. Assuming the currents of M1 and M2 are balanced with the designed passive components, the additional voltage stress on L_s is

$$v_s = (L_s - M_s)\frac{di_s}{dt} \tag{2-70}$$

where inductance (L_s – M_s) is named “stress-inducing inductance”.



(a) **(b)**

Fig. 2-70. (a) Voltage over-stress during turn-off transient; (b) influence of inductances on voltage stress.

Fig. 2-71 compares the design trajectories of different solutions calculated by design guidelines in Table 2-9, where current rise time t_r is 35 ns, V_{th} mismatch is 0.44 V, and maximum difference of peak currents is set as 0.5 A. The Y-axis plots the equivalent stress-inductance (L_s - M_s). The first X-axis plots the self-inductance of drive-source inductor and the secondary X-axis plots drive-source resistance. Mutual inductances for solutions with magnetic coupling are 20 nH to obtain fair comparison.

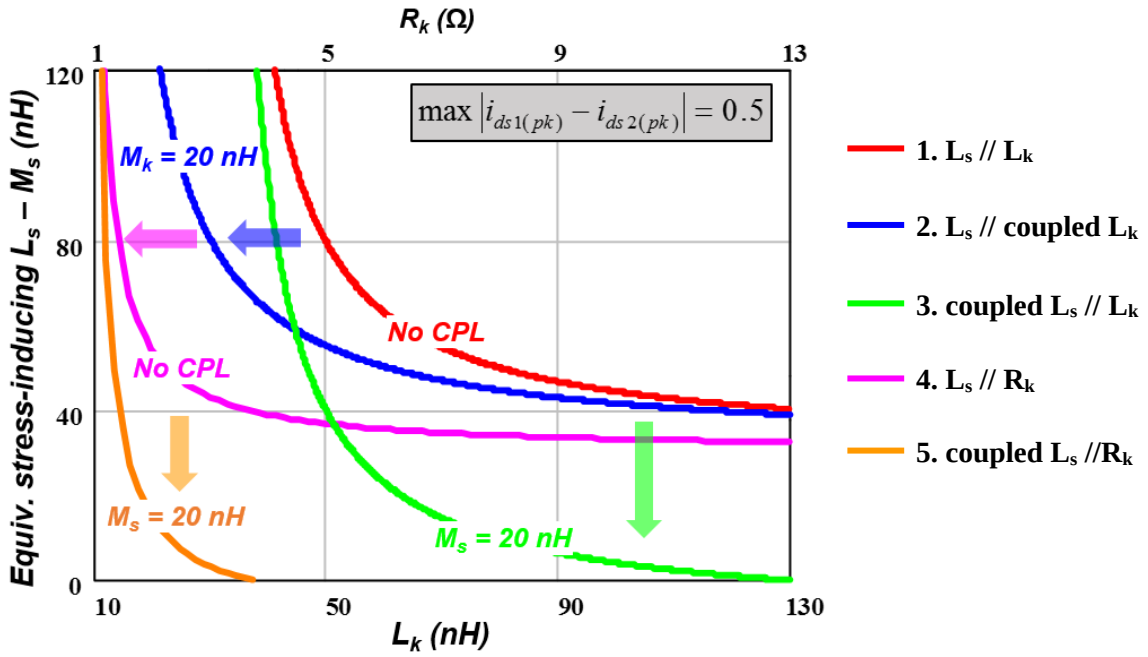


Fig. 2-71. Comparison of equivalent stress-inducing inductance (L_s – M_s) among different solutions. The other conditions are $|\Delta V_{th}|$ = 0.44 V and t_r = 35 ns.

According to the comparison among solutions 1, 2, and 3 shown in Fig. 2-71, magnetic coupling reduces the inductances required for the same balancing effect. The red curve (design trajectory without coupling) shifts to the left when the drive-source inductors L_k are negatively coupled and shifts downward when the power-source inductors L_s are negatively coupled. Trajectories will shift further away with tighter coupling, as depicted in Fig. 2-35 and Fig. 2-37.

Stress inducing inductance (L_s – M_s) can also be reduced by replacing drive-source inductance L_k by drive-source resistance R_k, as illustrated by the magenta curve in Fig. 2-71. This magenta curve (design trajectory without coupling) shifts downward when power-source inductors L_s are negatively coupled, as shown by the orange line. The third structure coupled L_s//L_k and the fifth structure coupled L_s//R_k provide the lest stress-inducing inductance among all the solutions and are preferred if voltage stress is a critical factor in the design process. Perfect coupling between

L_{s1} and L_{s2} would enable current matching without penalty on voltage stress.

Table 2-10. Summary of L_s, L_k, M_s, M_k, and R_k for different designs

	Baseline	L_s//L_k	L_s//coupled L_k	coupled L_s//L_k	L_s//R_k	coupled L_s//R_k
L_s (nH)	11.5	88.5	88.5	57.0	47.2	29.8
L_k (nH)	4.9	59.9	39.4	59.9	4.9	4.9
M_s (nH)	0	0	0	39.3	0	18.8
M_k (nH)	0	0	20.6	0	0	0
R_k (Ω)	0	0	0	0	5.6	5.6

Baseline design and five passive balancing designs (shown in Fig. 2-68) are tested at the same operating conditions utilizing the same board to ensure fair comparison. Table 2-10 summarizes the passive components L_s, L_k, M_s, M_k, and R_k applied in the experiments. Inductances L_s and L_k for baseline design are from PCB layout and are not purposely designed. The other five tests inserted extra discrete inductors, coupled inductors, or SMD resistors, which either dominated or bypassed the original power- and drive-source inductance on the PCB layout.

The design points in Table 2-10 are also depicted in Fig. 2-72, where the corresponding design trajectories are plotted with mutual-inductances (which are close to the values shown in Table 2-10) labeled. Some design margins are left in case of any uncontrollable factors influencing the experimental results. According to (2-70), points at higher positions will result in higher voltage stress. The measured V_{pk} for both paralleled MOSFETs are compared in Fig. 2-73. The results match well with the trend shown in Fig. 2-72. The fifth design (coupled L_s//R_k), which has the smallest equivalent stress-inducing inductance, achieves the smallest voltage stress. This value is the same as the baseline design because of the similar (L_s – M_s) (as shown in Table 2-10).

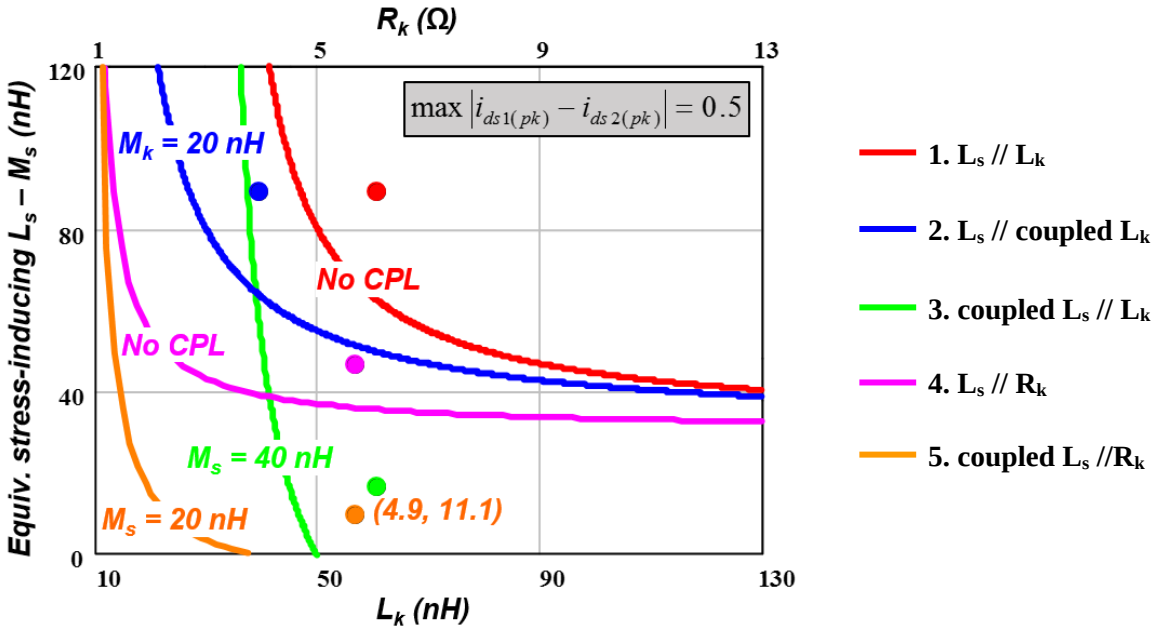
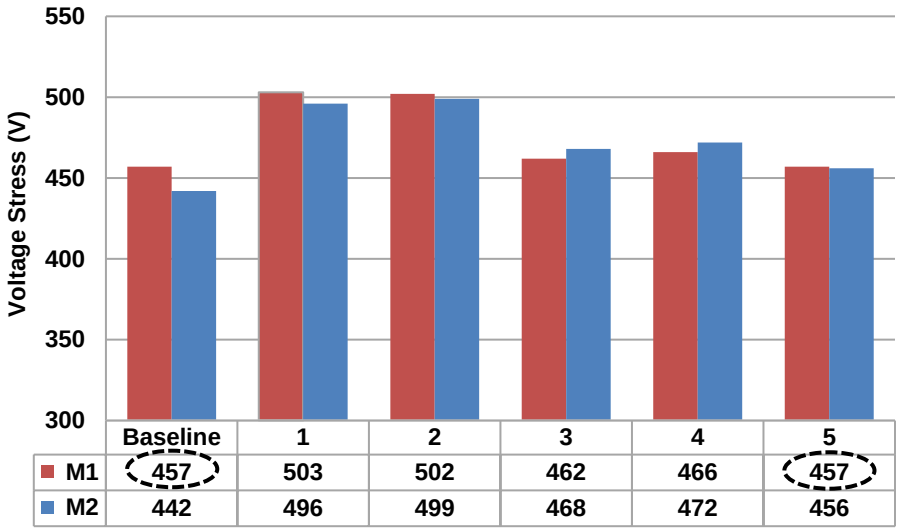


Fig. 2-72. Design points of experiments shown in Fig. 2-52, Fig. 2-53, Fig. 2-58, Fig. 2-62, and Fig. 2-55 for balancing of switching transients.



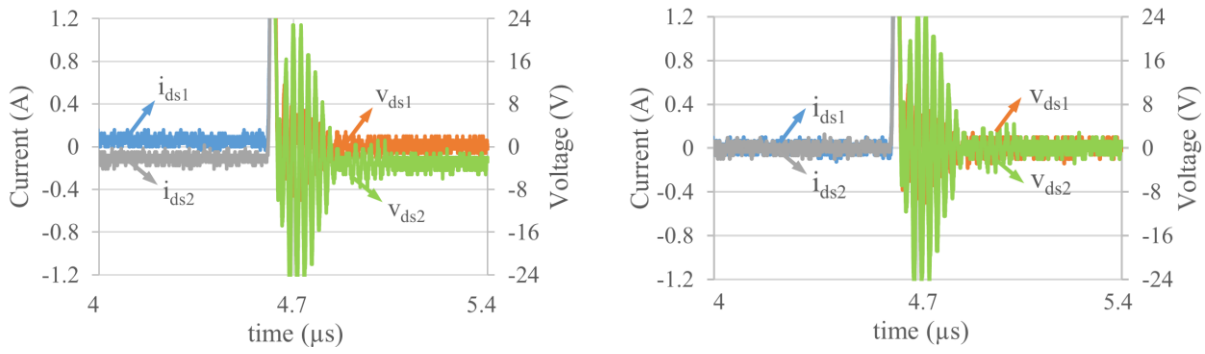
	Baseline	1	2	3	4	5
M1	457	503	502	462	466	457
M2	442	496	499	468	472	456

Fig. 2-73. Comparison of voltage stresses among different design points shown in Fig. 2-72.

Following, switching energies and switching energy differences will also be compared.

The switching energies were calculated by the integration of instantaneous power (i_{ds}*v_{ds}) during turn-on and turn-off transients. Two split core current probes and two differential voltage

probes were employed to measure drain-source currents and drain-source voltages, respectively. Probe specifications are shown in Table 2-2. The propagation delays among probes were compensated by a resistive load circuit to obtain accurate switching energy. Most of the DC offsets were removed by the probes built-in AutoZero routines to achieve accurate switching energy differences. However, small amounts of DC offsets and/or difference of DC offsets between current/voltage probes still exist even after running those routines, as shown in Fig. 2-74(a). Even though those DC offsets and DC offset differences are small (e.g. 0.2 A << 10 A, 4 V << 300 V), they will result in large errors in the calculated switching energy and switching energy difference. Waveforms after the elimination of DC offsets are shown in Fig. 2-74(b).



(a) **(b)**

Fig. 2-74. (a) Original measured currents and voltages with different DC offsets; (b) post-processed currents and voltages with zero DC offsets.

The comparison of the calculated switching energies and switching energy differences based on Fig. 2-74(a) and Fig. 2-74(b) are shown in Table 2-11, where E_{sw1} and E_{sw2} are the switching losses (including turn-on loss and turn-off loss) of M1 and M2, respectively. Based on the good

sharing illustrated in Fig. 2-52, switching loss difference of 5.96 µJ is more reasonable than 29.1 µJ. Elimination of DC offsets by post-processing is critical to achieve correct conclusion.

Table 2-11. Comparison of switching energies before and after the elimination of DC offsets

	E_{sw1}	E_{sw2}	$E_{sw1} - E_{sw2}$	$E_{sw1} + E_{sw2}$
Original (µJ)	100.77	71.67	29.10	172.44
Post-processed (µJ)	90.37	84.41	5.96	174.78

The comparisons of total switching losses and switching loss differences among different design points in Fig. 2-72 are shown in Fig. 2-75 and Fig. 2-76, respectively. The proposed passive balancing solutions didn't increase the total switching loss and reduced the switching loss difference between paralleled MOSFETs by around 4 times compared to the baseline design. The resulting differences of five solutions are similar with each other because all the designs are based on the same criteria, i.e. maintain difference of peak currents below and near 0.5 A. To sum up, passive balancing solutions shown in Fig. 2-68 can compensate V_{th} mismatch with negligible influence on total switching energy.

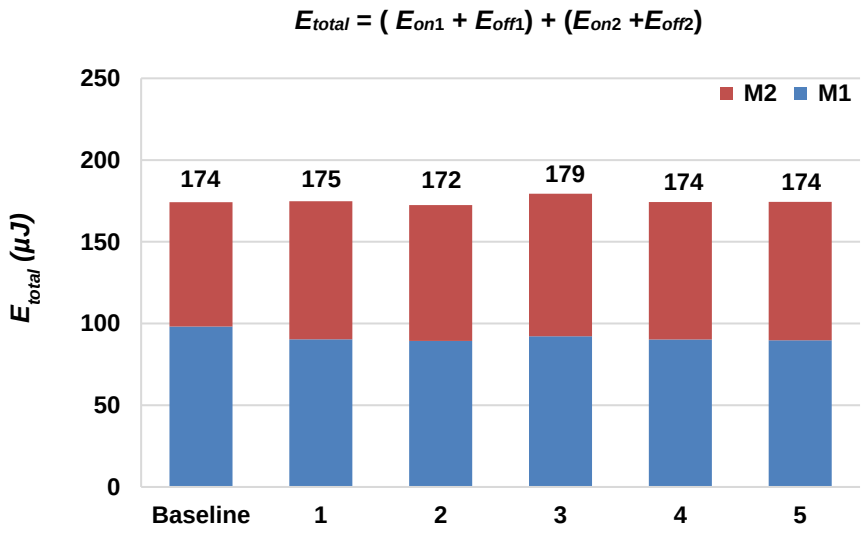


Fig. 2-75. Comparison of total switching energies among different design points shown in Fig. 2-72.

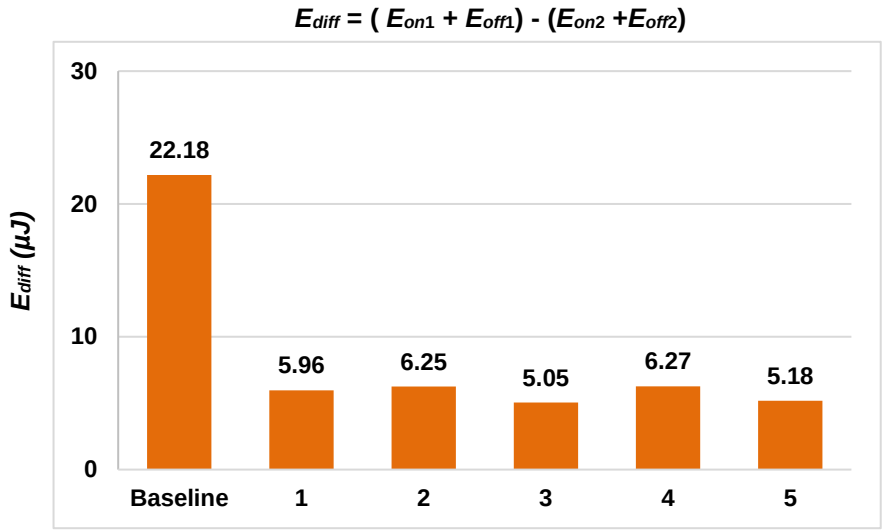


Fig. 2-76. Comparison of switching energy difference among different design points shown in Fig. 2-72.

The comprehensive comparisons of peak-current difference, voltage stress, switching loss difference, and total switching loss are summarized in Fig. 2-77. All of the designs can provide much better current and power balancing without increasing switching loss. Some of the them induce more voltage stress due to the increased stress-inducing inductance, which can be reduced by negative magnetic coupling.

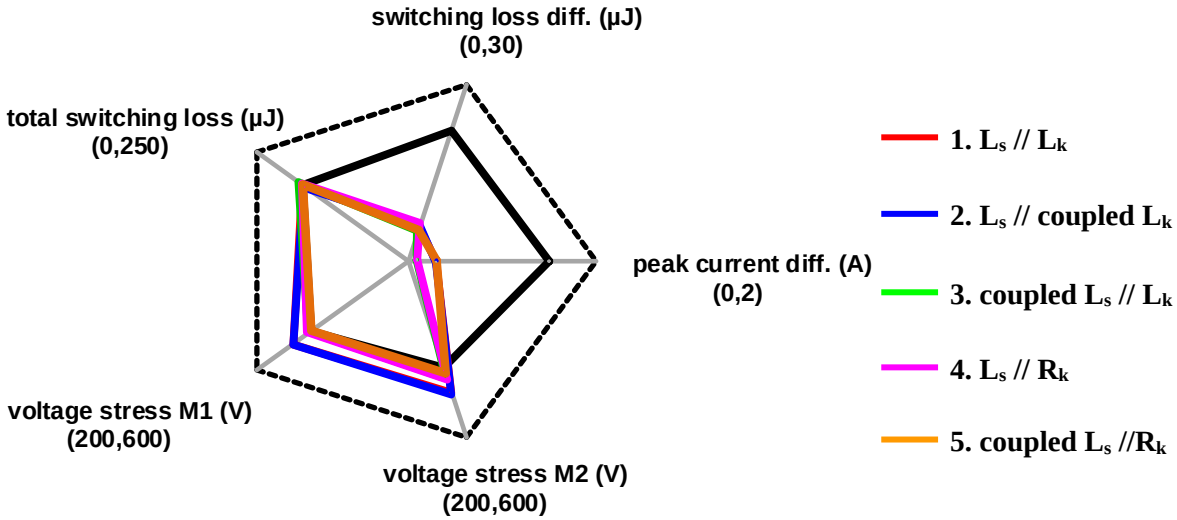


Fig. 2-77. Summary of comparison among different design points shown in Fig. 2-72.

The current balancing solutions in Fig. 2-68 do not require any sensors in practical applications. Parasitic inductance along the current commutation loop can be maintained at small levels after the elimination of current probe and/or addition of decoupling capacitor. The switching speed can be increased without introducing severe ringing, and less (L_s – M_s) than Fig. 2-71 is expected as shown in Fig. 2-78. Fig. 2-77 only compares one design for each solution. Several possible designs exist especially when mutual inductance exists. The appropriate structure and design point can be selected based on the convenience of realization and switching characteristics.

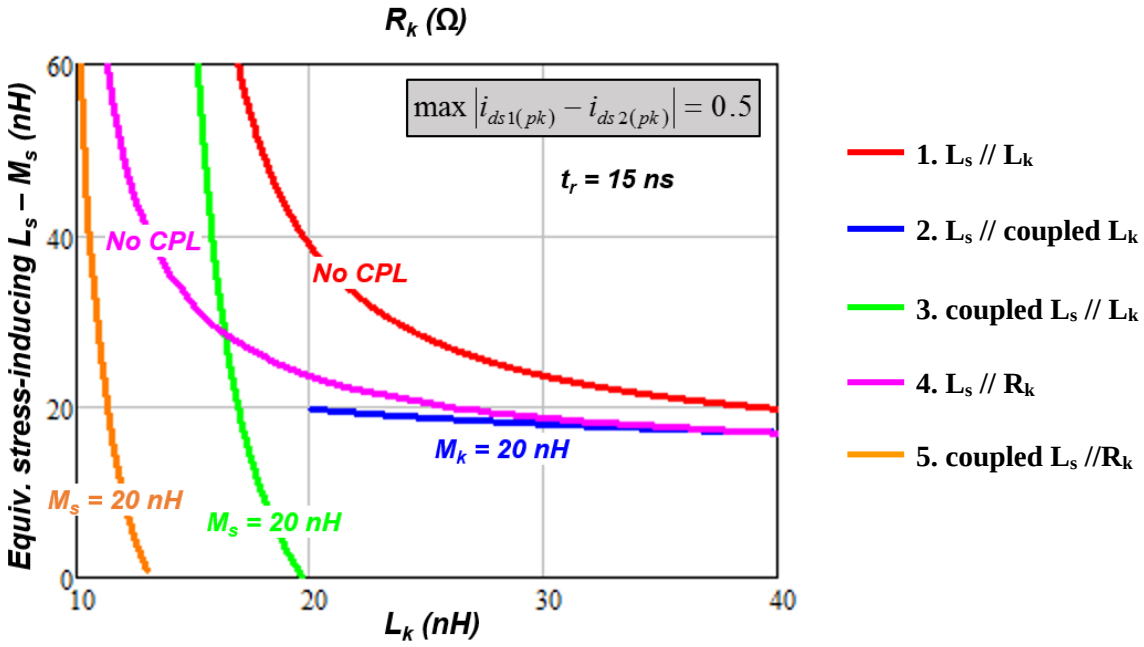


Fig. 2-78. Comparison of equivalent stress-inducing inductance (L_s – M_s) among different solutions. The other conditions are $|\Delta V_{th}|$ = 0.44 V and t_r = 15 ns.

2.9 Conclusion

Passive balancing solutions are investigated to balance the peak currents between paralleled MOSFETs caused by unequal threshold voltages. Current/voltage sensors, feedback loop, multiple gate drivers, and the knowledge of the polarity of V_{th} difference are not required. The difference

of peak currents can be limited to a predetermined percentage by inductances and/resistances without sacrificing the total switching loss. The aforementioned benefits were demonstrated by two paralleled SiC MOSFETs (C2M0160120D) tested over a wide operating range. The difference of peak currents can be reduced below 5% of steady-state current in every switching transient. The values of passive components were determined by the design guidelines involving threshold voltage mismatch, current rise time, and unbalance percentage. The ΔV_{th} may vary under continuous testing due to the different junction temperatures between MOSFETs and the negative temperature coefficient of V_{th}. The worst ΔV_{th} can be approximated by the temperature coefficient of V_{th} in the datasheet. For example, if the largest difference of temperatures allowed is 25°C, the ΔV_{th} of SiC MOSFETs C2M0160120D will increase around 0.25 V [33]. The R_k, L_s, L_k, M_k, or M_s can be calculated by design guidelines with the updated worst ΔV_{th}. This chapter did not cover the case of different junction temperatures. Further investigation could be undertaken in the future. The realization of coupled inductors with magnetic core can also be studied to further reduce the size and to manage the magnetic field when the calculated inductance is too large to be effectively realized by air-cored inductor. Very-high-frequency magnetic materials reported in [95],[96] can provide a permeability of 50 or above at tens of MHz and could be used to fabricate the inductor with magnetic core for current balancing. As only current difference is flowing through the negatively-coupled inductors, the size and loss of magnetic core are expected to be limited when the balancing solution is implemented. The methods shown in Fig. 2-68 can be extended to the case of more than two MOSFETs in parallel (as shown in Appendix B) because they don't need to consider the asymmetry of V_{th} and uses one gate driver. In practical realization, e.g., module fabrication, the $|\Delta V_{th}|$ can be replaced by the largest mismatch from the datasheet, and t_r can be approximated by simulation and/or datasheet for the worst-case design.

Chapter 3 Balancing Solutions for Paralleling of Discrete MOSFETs

Nomenclature

V_{th}	Threshold voltage
L_d	Drain inductance
L_s	Power-source inductance
L_p	Power-loop inductance
L_{cm}	Common-source inductance
L_{kg}	Drive-gate inductance
L_k	Drive-source inductance
L_g	Gate-drive inductance
g_{fs}	Large signal transconductance
V_{in}	Input voltage of double-pulse tester
I_{in}	Input current of double-pulse tester
R_g	Gate resistor of double-pulse tester
i_{ds}	Channel current of MOSFET
v_{ds}	Drain-source voltage of MOSFET
v_{gs}	Gate-source voltage of MOSFET
i_{kg}	Gate charging current of MOSFET
E_{sw}	Switching energy
I_{pk}	Peak channel current
V_{pk}	Peak drain-source voltage

M	Mutual inductance
r	Radius of air-cored coupled inductors
n	Number of turns
L_{insert}	Inserted inductance
L_{int}	Inductance inside package
L_{pcb}	Inductance from PCB layout

3.1 Introduction

The current rating of SiC MOSFET is not high enough for medium and high-power application. Discrete MOSFETs may need to be paralleled to increase the current capability. The uneven current distribution caused by threshold voltage mismatch will lead to different losses among paralleled MOSFETs and finally reduce the reliability and lifetime of parallel structure. According to the parametric analysis shown in Section 2.2, common-source inductance L_{cm}, drive-source inductance L_k, and power-source inductance L_s have current balancing effect. Inductance L_{cm} is not considered in Chapter 2 because common-source inductance is negligible in power module. However, the wire bond inside the package of discrete MOSFETs and part of the external leads are inevitable and will add to common-source inductance, as shown in Fig. 3-1. The drive-source inductances are also neglected in the analysis of Chapter 2 because the L_k on PCB layout were assumed to be small. The impedances on drive-source traces were dominated by the inserted inductors or resistors. In this chapter, all the balancing-effective passive components, including L_s, L_k, R_k, and L_{cm}, will be considered. A design guideline that is applicable to the paralleling of discrete MOSFETs will be derived to guide the choice of passive components. Parasitics that are not effective in current balancing, such as L_p, L_d and so on, are neglected during derivation to simplify the analysis. The detail design procedure of the passive balancing solution that is effective

over wide operating range is described. The accuracy design guideline and the effectiveness of worst case design over wide operating range are also experimentally verified.

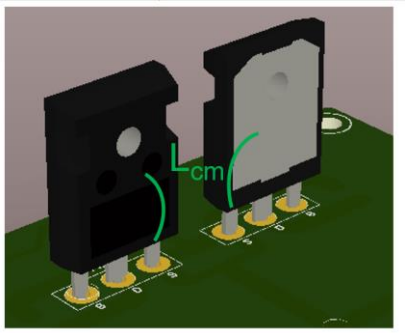


Fig. 3-1. Paralleling of discrete MOSFETs.

3.2 Passive Balancing Structure, Design Guideline, and Design Procedure

Five passive balancing methods were introduced in Chapter 2. All of the designs can provide much better current and power balancing without increasing switching loss. Some of the them induce more voltage stress due to the increased stress-inducing inductance, which can be reduced by negative magnetic coupling. Perfect coupling between L_{s1} and L_{s2} would enable current matching without penalty on voltage stress. Thus, structure with coupled L_s is analyzed, as shown in Fig. 3-2, which can also be reduced to the case without coupling by setting M_s = 0 nH. Both drive-source resistance R_k and drive-source inductance L_k are inserted in the drive-source path as they are both are effective in current balancing. Common-source inductance is inevitable in paralleling of discrete MOSFETs and helps current balancing. It is also included, however, will not be increased intentionally. The passive solution in Fig. 3-2 adds an extra L_k in drive-source path and an extra L_{cm} in the common-source path per switch compared to the passive solution shown in Fig. 2-25 (coupled L_s//R_k). Fig. 3-3(a) and Fig. 3-3(b) show the structures with an additional L_k and an addition L_{cm}, respectively. Their design guidelines will be derived first to

reveal the specific influences of L_k and L_{cm} on transient balancing.

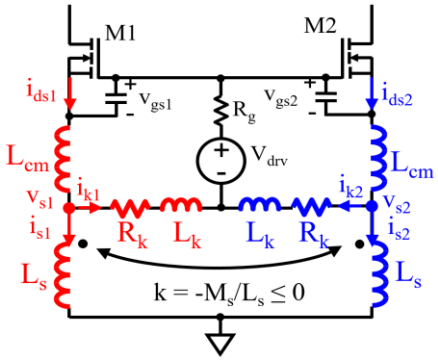


Fig. 3-2. Complete balancing solution with L_{cm}, R_k, L_k, and coupled L_s.

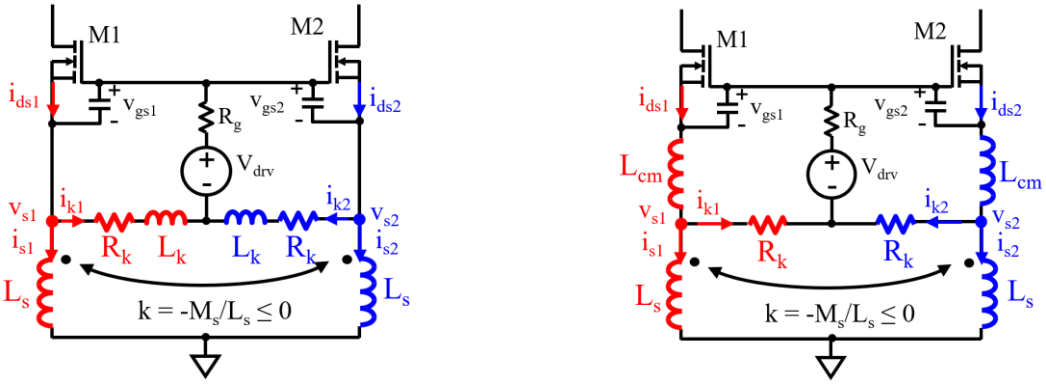


Fig. 3-3. (a) Balancing solution with R_k, L_k, and coupled L_s; (b) balancing solution with L_{cm}, R_k, and coupled L_s.

Firstly, the structure in Fig. 3-3(a) is analyzed.

The expression of Δi_{ds} was derived in (2-6) and is repeated here for reference:

$$\Delta i_{ds} = 2g_{fs}\left(v_{gs} - V_{th}\right)\left(\Delta v_{gs} - \Delta V_{th}\right), \quad v_{gs} > V_{th} \tag{3-1}$$

According to (2-18), a certain Δv_{gs} needs to be produced in order to balancing the mismatch of switching transients induced by ΔV_{th}. Based on KVLs of the loop formed by gate-source

capacitors, drive-source resistors, and drive-source inductors and the loop formed by gate-source capacitors and coupled power-source inductors:

$$\Delta v_{gs} = -(L_s + M_s)\frac{d\Delta i_s}{dt} = -R_k \Delta i_k - L_k \frac{d\Delta i_k}{dt} \tag{3-2}$$

where Δi_s is the current difference of power-source inductances and Δi_k is the current difference of drive-source resistances.

The currents bypassed through C_{gs} and C_{ds} can be neglected compared to i_{ds} when i_{ds} rises. Taking the difference of KCLs at nodes v_{s1} and v_{s2} in Fig. 3-3(a),

$$\Delta i_{ds} = \Delta i_s + \Delta i_k \tag{3-3}$$

where current difference Δi_k can be solved by (3-2) as

$$\Delta i_k = -\frac{1}{L_k} e^{-\frac{R_k}{L_k}t} \int e^{\frac{R_k}{L_k}t} \Delta v_{gs} dt \tag{3-4}$$

where initial condition $\Delta i_k (t = 0) = 0$ A is applied and $t = 0$ is when v_{gs} reaches V_{th}.

The derivatives of Δi_s and Δi_k can be obtained by (3-2) and (3-4), respectively as

$$\frac{d\Delta i_s}{dt} = -\frac{\Delta v_{gs}}{L_s + M_s} \tag{3-5}$$

$$\frac{d\Delta i_k}{dt} = \frac{R_k}{L_k^2} e^{-\frac{R_k}{L_k}t} \int e^{\frac{R_k}{L_k}t} \Delta v_{gs} dt - \frac{1}{L_k} \Delta v_{gs} \tag{3-6}$$

Substitution of (3-5), (3-6) and the derivative of (3-1) into the derivative (3-3) yields

$$\frac{d\Delta v_{gs}}{dt}=\frac{-\dfrac{\Delta v_{gs}}{L_s+M_s}+\dfrac{R_k}{L_k^2}e^{-\frac{R_k}{L_k}t}\int e^{\frac{R_k}{L_k}t}\Delta v_{gs}dt-\dfrac{1}{L_k}\Delta v_{gs}-2g_{fs}\left(\Delta v_{gs}-\Delta V_{th}\right)\dfrac{dv_{gs}}{dt}}{2g_{fs}\left(v_{gs}-V_{th}\right)},\ v_{gs}\geq V_{th} \tag{3-7}$$

When t = 0, the above equation is reduced to

$$\frac{d\Delta v_{gs}}{dt}\left(t=0\right)=\frac{g_{fs}\Delta V_{th}\dfrac{dv_{gs}}{dt}}{2g_{fs}\left(v_{gs}-V_{th}\right)},v_{gs}\geq V_{th} \tag{3-8}$$

The slew rate of Δv_{gs} is larger than zero when $\Delta V_{th} > 0$ and smaller than zero when $\Delta V_{th} < 0$. Voltage Δv_{gs} will rise until the maximum value is reached if $\Delta V_{th} > 0$. Vice versa for the case of $\Delta V_{th} < 0$.

Thus, the maximum value Δv_{gsMax} is achieved when $d\Delta v_{gs}/dt=0$, i.e.,

$$-\frac{\Delta v_{gsMax}}{L_s+M_s}+\frac{R_k}{L_k^2}e^{-\frac{R_k}{L_k}t_{@\Delta v_{gsMax}}}\int_0^{t_{@\Delta v_{gsMax}}}e^{\frac{R_k}{L_k}t}\Delta v_{gs}dt-\frac{1}{L_k}\Delta v_{gsMax}-2g_{fs}\left(\Delta v_{gsMax}-\Delta V_{th}\right)\frac{dv_{gs}}{dt} \tag{3-9}$$
$$=0$$

Rearrangement of (3-9) yields

$$\Delta v_{gsMax}=\frac{2g_{fs}\dfrac{dv_{gs}}{dt}\Delta V_{th}+\dfrac{R_k}{L_k^2}e^{-\frac{R_k}{L_k}t_{@\Delta v_{gsMax}}}\int_0^{t_{@\Delta v_{gsMax}}}e^{\frac{R_k}{L_k}t}\Delta v_{gs}dt}{\dfrac{1}{L_s+M_s}+\dfrac{1}{L_k}+2g_{fs}\dfrac{dv_{gs}}{dt}} \tag{3-10}$$

Voltage Δv_{gs} is generated to compensate ΔV_{th} and is smaller than 0 if $\Delta V_{th} < 0$. The second term in the denominator of (3-10) can be deduced as

$$\frac{R_k}{L_k^2} e^{-\frac{R_k}{L_k} t_{@\,\Delta v_{gsMax}}} \int_0^{t_{@\,\Delta v_{gsMax}}} e^{\frac{R_k}{L_k} t} \Delta v_{gs} dt \geq \frac{R_k}{L_k^2} \Delta v_{gsMax} e^{-\frac{R_k}{L_k} t_{@\,\Delta v_{gsMax}}} \int_0^{t_{@\,\Delta v_{gsMax}}} e^{\frac{R_k}{L_k} t} dt$$

$$= \frac{R_k}{L_k^2} \Delta v_{gsMax} e^{-\frac{R_k}{L_k} t_{@\,\Delta v_{gsMax}}} \left(\frac{L_k}{R_k} e^{\frac{R_k}{L_k} t_{@\,\Delta v_{gsMax}}} - \frac{L_k}{R_k} \right) \qquad (3\text{-}11)$$

$$\geq \frac{1}{L_k} \Delta v_{gsMax}$$

Apply (3-11) to (3-10),

$$\Delta v_{gsMax} \geq \frac{2 g_{fs} \frac{dv_{gs}}{dt} \Delta V_{th} + \frac{1}{L_k} \Delta v_{gsMax}}{\frac{1}{L_s + M_s} + \frac{1}{L_k} + 2 g_{fs} \frac{dv_{gs}}{dt}} \qquad (3\text{-}12)$$

Rearrangement of (3-12) yields

$$\Delta v_{gsMax} \geq \frac{1}{\left[2 g_{fs} \frac{dv_{gs}}{dt} \left(L_s + M_s \right) \right]^{-1} + 1} \Delta V_{th} \geq \Delta V_{th} \qquad (3\text{-}13)$$

The larger ($L_s + M_s$) is, the closer Δv_{gsMax} is to ΔV_{th}. Thus, the inequality

$$\left[2 g_{fs} \frac{dv_{gs}}{dt} \left(L_s + M_s \right) \right]^{-1} << 1 \qquad (3\text{-}14)$$

enables $\Delta v_{gs} \rightarrow \Delta V_{th}$ and $\Delta i_{ds} \rightarrow 0$.

Following the same procedure from (3-11) to (3-12), the maximum value of Δv_{gs} for $\Delta V_{th} > 0$ is

$$\Delta v_{gsMax} \le \frac{2g_{fs}\dfrac{dv_{gs}}{dt}}{\dfrac{1}{L_s+M_s}+2g_{fs}\dfrac{dv_{gs}}{dt}}\Delta V_{th} \le \Delta V_{th} \tag{3-15}$$

Combining (3-13) and (3-15) for both polarities of ΔV_{th} gives

$$\left|\Delta v_{gs}\right| \le \left|\Delta V_{th}\right| \tag{3-16}$$

Applying (3-16) to (3-2), inequalities for Δi_s and Δi_k can be solved. Substitution of those two inequalities to (3-3) yields

$$\left|\Delta i_{ds}\right| \le \frac{\left|\Delta V_{th}\right|}{R_k}\left(1-e^{-\frac{R_k}{L_k}t_r}\right)+\frac{\left|\Delta V_{th}\right|}{L_s+M_s}t_r \tag{3-17}$$

Thus, the maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ for the structure shown in Fig. 3-3(a) is

$$\max\left|\Delta i_{ds(pk)}\right| = \frac{\left|\Delta V_{th}\right|}{R_k}\left(1-e^{-\frac{R_k}{L_k}t_r}\right)+\frac{\left|\Delta V_{th}\right|}{L_s+M_s}t_r \tag{3-18}$$

where t_r is the time for current to rise from 0 to the peak value.

When $R_k = 0\ \Omega$ and $L_k \neq 0$ nH, guideline (3-18) reduces to

$$\lim_{R_k\to 0}\left(\max\left|\Delta i_{ds(pk)}\right|\right) = \frac{\left|\Delta V_{th}\right|}{L_k}t_r+\frac{\left|\Delta V_{th}\right|}{L_s+M_s}t_r \tag{3-19}$$

which is exactly the same as the design guideline of structure coupled $L_s//L_k$ shown in Fig. 2-68.

In most cases, term $e^{-\frac{R_k}{L_k}t_r}$ is much smaller than 1 and

$$1-e^{-\frac{R_k}{L_k}t_r} \approx 1 \tag{3-20}$$

For example, when $R_k = 2\ \Omega$, $L_k = 10$ nH, and $t_r = 20$ ns, term $e^{-\frac{R_k}{L_k}t_r} = 0.018 << 1$. The equation of maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ shown in (3-18) can be reduced to

$$\max\left|\Delta i_{ds(pk)}\right| \approx \frac{\left|\Delta V_{th}\right|}{R_k} + \frac{\left|\Delta V_{th}\right|}{L_s + M_s} t_r \tag{3-21}$$

The above equation consists of two terms. The first term ($|\Delta V_{th}|/R_k$) shows the effect of R_k and the second term ($|\Delta V_{th}|t_r/(L_s + M_s)$) indicates the influence of L_s and M_s. The design guideline for Fig. 3-3(a) is the same as the case without L_k, as shown in Table 2-9. In other words, the impedance of drive-source trace is dominated by R_k.

Then, the structure in Fig. 3-3(b) is analyzed.

Based on KVLs of the loop formed by gate-source capacitors, common-source inductors, and drive-source resistors and the loop formed by gate-source capacitors, common-source inductors, and coupled power-source inductors:

$$\Delta v_{gs} = -L_{cm}\frac{d\Delta i_{ds}}{dt} - \left(L_s + M_s\right)\frac{d\Delta i_s}{dt} = -L_{cm}\frac{d\Delta i_{ds}}{dt} - R_k \Delta i_k \tag{3-22}$$

Substitution of (3-3) into (3-22) yields

$$\Delta v_{gs} = -\left(L_{cm} + L_s + M_s\right)\frac{d\Delta i_s}{dt} - L_{cm}\frac{d\Delta i_k}{dt} = -L_{cm}\frac{d\Delta i_s}{dt} - L_{cm}\frac{d\Delta i_k}{dt} - R_k \Delta i_k \tag{3-23}$$

Rearrange (3-23):

$$\begin{cases} \dfrac{d\Delta i_k}{dt} + \dfrac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}\Delta i_k = -\dfrac{\Delta v_{gs}}{L_{cm}} \\ \dfrac{d\Delta i_s}{dt} = -\dfrac{L_{cm}}{L_{cm}+L_s+M_s}\dfrac{d\Delta i_k}{dt} - \dfrac{\Delta v_{gs}}{L_{cm}+L_s+M_s} \end{cases} \tag{3-24}$$

Solving the first equation of (3-24),

$$\Delta i_k = -\frac{1}{L_{cm}} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \int e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \Delta v_{gs} dt \tag{3-25}$$

where initial condition $\Delta i_k(t = 0) = 0$ is applied and t = 0 is when v_{gs} reaches V_{th}.

Taking the derivative of (3-25)

$$\frac{d\Delta i_k}{dt} = \frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}^2\left(L_s+M_s\right)} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \int e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \Delta v_{gs} dt - \frac{1}{L_{cm}} \Delta v_{gs} \tag{3-26}$$

Substitution of the second equation of (3-24) into the derivative of (3-3) yields

$$\frac{d\Delta i_{ds}}{dt} = \frac{L_s+M_s}{L_{cm}+L_s+M_s}\frac{d\Delta i_k}{dt} - \frac{\Delta v_{gs}}{L_{cm}+L_s+M_s} \tag{3-27}$$

The derivative of Δv_{gs} can be obtained by substituting (3-26) and the derivative of (3-1) into (3-27):

$$\frac{d\Delta v_{gs}}{dt} = \frac{\dfrac{R_k}{L_{cm}^2} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \int e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \Delta v_{gs} dt - \left[\dfrac{L_s+M_s}{L_{cm}\left(L_{cm}+L_s+M_s\right)} + \dfrac{1}{L_{cm}+L_s+M_s} + 2g_{fs}\dfrac{dv_{gs}}{dt}\right]\Delta v_{gs} + 2g_{fs}\Delta V_{th}\dfrac{dv_{gs}}{dt}}{2g_{fs}\left(v_{gs}-V_{th}\right)} \tag{3-28}$$

Similar to (3-7), the maximum value Δv_{gsMax} is reached when $d\Delta v_{gs}/dt=0$, i.e.,

$$\frac{R_k}{L_{cm}^2} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_{@\Delta v_{gsMax}}} \int_0^{@\Delta v_{gsMax}} e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \Delta v_{gs} dt$$
$$-\left[\frac{L_s+M_s}{L_{cm}\left(L_{cm}+L_s+M_s\right)}+\frac{1}{L_{cm}+L_s+M_s}+2g_{fs}\frac{dv_{gs}}{dt}\right]\Delta v_{gsMax}+2g_{fs}\Delta V_{th}\frac{dv_{gs}}{dt}=0 \quad (3\text{-}29)$$

Rearrangement of (3-29) yields,

$$\Delta v_{gsMax}=\frac{2g_{fs}\Delta V_{th}\frac{dv_{gs}}{dt}+\frac{R_k}{L_{cm}^2}e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_{@\Delta v_{gsMax}}}\int_0^{@\Delta v_{gsMax}}e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t}\Delta v_{gs}dt}{\frac{L_s+M_s}{L_{cm}\left(L_{cm}+L_s+M_s\right)}+\frac{1}{L_{cm}+L_s+M_s}+2g_{fs}\frac{dv_{gs}}{dt}} \quad (3\text{-}30)$$

Voltage Δv_{gs} is generated to compensate ΔV_{th} and is smaller than 0 if $\Delta V_{th} < 0$, which means $\Delta v_{gs} \geq \Delta v_{gsMax}$. The second term in the denominator of (3-30) can be deduced as

$$\begin{aligned}
&\frac{R_k}{L_{cm}^2} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_{@\Delta v_{gsMax}}} \int_0^{@\Delta v_{gsMax}} e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} \Delta v_{gs} dt \\
&\geq \frac{R_k}{L_{cm}^2}\Delta v_{gsMax} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_{@\Delta v_{gsMax}}} \int_0^{@\Delta v_{gsMax}} e^{\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t} dt \\
&= \frac{R_k}{L_{cm}^2}\Delta v_{gsMax} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_{@\Delta v_{gsMax}}} \left[\frac{L_{cm}\left(L_s+M_s\right)}{R_k\left(L_{cm}+L_s+M_s\right)} e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_{@\Delta v_{gsMax}}} - \frac{L_{cm}\left(L_s+M_s\right)}{R_k\left(L_{cm}+L_s+M_s\right)}\right] \\
&\geq \frac{L_s+M_s}{L_{cm}\left(L_{cm}+L_s+M_s\right)}\Delta v_{gsMax}
\end{aligned} \quad (3\text{-}31)$$

Apply (3-31) to (3-30),

$$\Delta v_{gsMax} \geq \frac{2g_{fs}\Delta V_{th}\frac{dv_{gs}}{dt}+\frac{L_s+M_s}{L_{cm}\left(L_{cm}+L_s+M_s\right)}\Delta v_{gsMax}}{\frac{L_s+M_s}{L_{cm}\left(L_{cm}+L_s+M_s\right)}+\frac{1}{L_{cm}+L_s+M_s}+2g_{fs}\frac{dv_{gs}}{dt}} \quad (3\text{-}32)$$

Rearrangement of (3-32) yields,

$$\Delta v_{gsMax} \geq \frac{1}{\left[2g_{fs}\frac{dv_{gs}}{dt}\left(L_{cm}+L_s+M\right)\right]^{-1}+1}\Delta V_{th} \geq \Delta V_{th} \tag{3-33}$$

The larger ($L_{cm} + L_s + M_s$) is, the closer Δv_{gsMax} is to ΔV_{th}. Thus, the inequality

$$\left[2g_{fs}\frac{dv_{gs}}{dt}\left(L_{cm}+L_s+M_s\right)\right]^{-1} << 1 \tag{3-34}$$

enables $\Delta v_{gs} \rightarrow \Delta V_{th}$ and $\Delta i_{ds} \rightarrow 0$.

Following the same procedure from (3-31) to (3-33), the maximum value of Δv_{gs} for $\Delta V_{th} > 0$ should satisfy

$$\Delta v_{gsMax} \leq \frac{2g_{fs}\frac{dv_{gs}}{dt}}{\frac{1}{L_{cm}+L_s+M_s}+2g_{fs}\frac{dv_{gs}}{dt}}\Delta V_{th} \leq \Delta V_{th} \tag{3-35}$$

Combining (3-33) and (3-35) for both polarities of ΔV_{th},

$$\left|\Delta v_{gs}\right| \leq \left|\Delta V_{th}\right| \tag{3-36}$$

The inequalities of Δi_s and Δi_k can be obtained by applying (3-36) to (3-24). Substitution of those two inequalities to (3-3) yields

$$\left|\Delta i_{ds}\right| \leq \frac{\left(L_s+M_s\right)^2\left|\Delta V_{th}\right|}{R_k\left(L_{cm}+L_s+M_s\right)^2}\left[1-e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_r}\right]+\frac{\left|\Delta V_{th}\right|}{L_{cm}+L_s+M_s}t_r \tag{3-37}$$

The maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ is

$$\max\left|\Delta i_{ds(pk)}\right| = \frac{\left(L_s + M_s\right)^2 \left|\Delta V_{th}\right|}{R_k \left(L_{cm} + L_s + M_s\right)^2}\left[1 - e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_r}\right] + \frac{\left|\Delta V_{th}\right|}{L_{cm} + L_s + M_s}t_r \tag{3-38}$$

Comparing (3-38) to (3-21), the effect of common-source inductance L_{cm} is coupled to both drive-source path and power-source path, as shown in Fig. 3-4. When L_{cm} = 0 nH, (3-28) reduces to

$$\lim_{L_{cm}\to 0}\left(\max\left|\Delta i_{ds(pk)}\right|\right) = \frac{\left|\Delta V_{th}\right|}{R_k} + \frac{\left|\Delta V_{th}\right|}{L_s + M_s}t_r \tag{3-39}$$

which is the same as the design guideline of structure coupled L_s//R_k shown in Fig. 2-68.

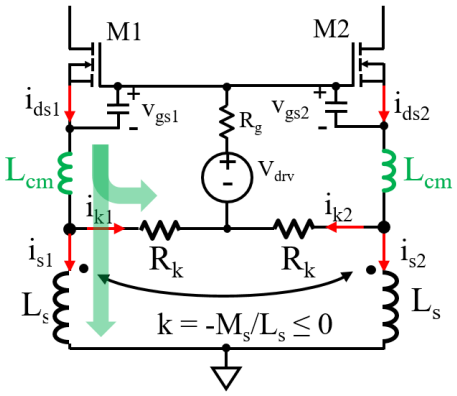


Fig. 3-4. Influence of common-source inductance L_{cm} is coupled to both drive-source path and power-source path.

Because L_k can be neglected when R_k is applied, the worst-case design guideline for the complete structure in Fig. 3-2 is

$$\max\left|\Delta i_{ds(pk)}\right| = \frac{\left(L_s + M_s\right)^2 \left|\Delta V_{th}\right|}{R_k \left(L_{cm} + L_s + M_s\right)^2}\left[1 - e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)}t_r}\right] + \frac{\left|\Delta V_{th}\right|}{L_{cm} + L_s + M_s}t_r \tag{3-40}$$

The design guideline (3-40) is demonstrated by two simulations shown in Fig. 3-5. Certain L_{cm} and coupled L_s exist in both cases. In Fig. 3-5(a), R_k is zero. Nodes v_{s1} and v_{s2} in Fig. 3-2 are shorted, which bypasses the balancing effect of coupled L_s. Voltage Δv_{gs}, which is only produced by L_{cm}, is not close to ΔV_{th} which results in 2.5 A peak-current difference. In Fig. 3-5(b), resistance R_k is design by (3-40) with $\max|\Delta i_{ds(pk)}| = 0.5$ A. The generated Δv_{gs} is still smaller than ΔV_{th} (as shown in (3-16) and (3-36)) but is very close to it. The measured Δi_{ds} is 0.46 A, which matches well with calculation and satisfies the design objective.

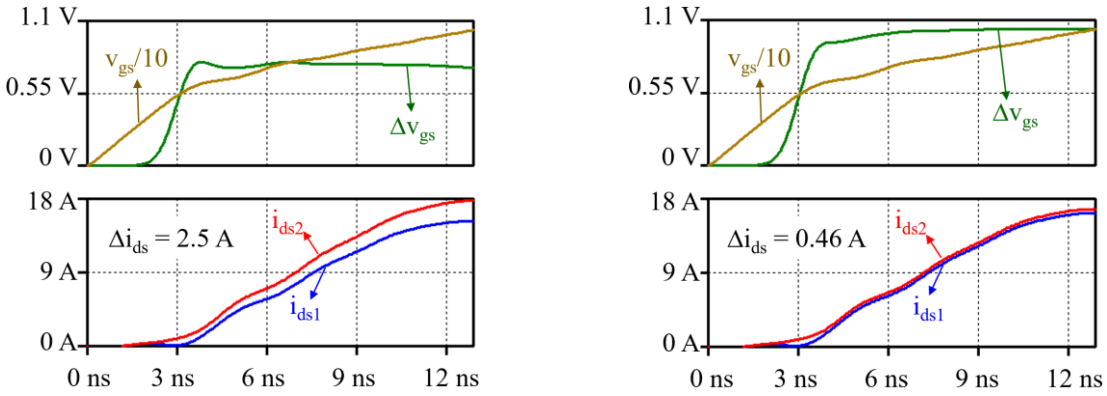


Fig. 3-5. Simulation results of Fig. 3-2 with L_{cm} = 4 nH, L_s = 30 nH, k = -0.8, L_k = 0, ΔV_{th} = 1.1 V, and (a) R_k = 0 Ω; (b) R_k = 4 Ω which is designed by (3-40) with t_r = 11.8 ns.

The influence of L_{cm}, $(L_s + M_s)$, and R_k on $\max|\Delta i_{ds(pk)}|$ can be plotted base on (3-40), as shown in Fig. 3-6. The other conditions employed are $|\Delta V_{th}| = 1.1$ V and $t_r = 16$ ns, which are the same as the situation in the later experiment. The $\max|\Delta i_{ds(pk)}|$ decreases with increasing L_{cm}, $(L_s + M_s)$, and R_k. The common-source inductance L_{cm} will not be increased intentionally (although it helps current balancing) because it greatly increases the switching loss (as shown in Fig. 2-3). Desired current balancing can be achieved by properly selecting the other passive values.

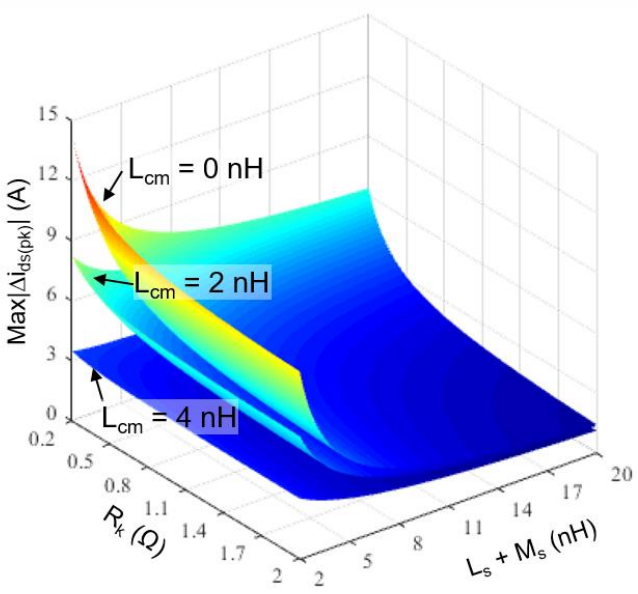


Fig. 3-6. Influence of L_{cm}, (L_s + M_s), and R_k on maximum peak-current difference, which is obtained by (3-40) when $|\Delta V_{th}|$ = 1.1 V and t_r = 16 ns.

Negative coupling of L_s not only enhances the balancing effect by adding an additional inductance M_s to self-inductance L_s, but also reduces the voltage stress induced by the passive balancing solution. Assuming the currents of M1 and M2 are balanced with the designed passive components, the additional voltage stress on M1 is

$$v_{s1} = L_s \frac{di_{s1}}{dt} - M_s \frac{d\left(i_{s2} = i_{s1} - \Delta i_s\right)}{dt} \approx \left(L_s - M_s\right)\frac{di_{s1}}{dt} \tag{3-41}$$

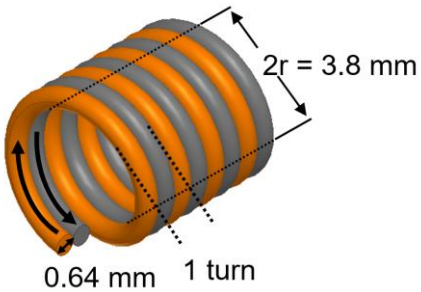
The inductance (L_s – M_s) is thus named “stress-inducing inductance”. Perfect coupling between two power-source inductors would enable current matching without penalty on voltage stress.

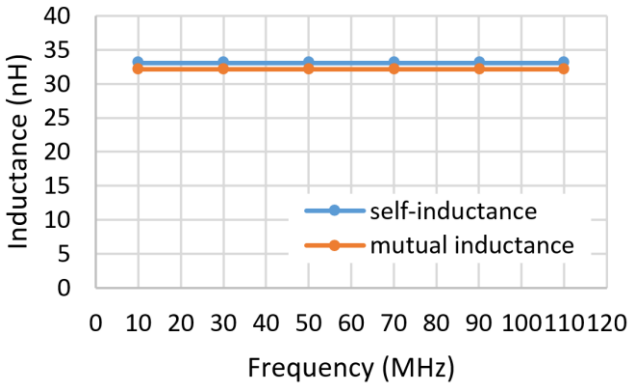
Air-cored coupled inductors were simulated, designed, and manufactured in Chapter 2. Each inductor comprises a “solenoidal winding” and two “leads”. The solenoidal windings were wound bifilarly since finite-element simulation suggested such a construction would yield $M_s \approx L_s$. The

inductance L_{lead} of each lead was estimated from lead length l_{lead}. Preliminary inductances M_s and L_s - M_s were estimated from M_{sole} in (2-59) and L_{lead} in (2-60) by

$$M_s \approx M_{sole}, L_s - M_s \approx L_{lead} \tag{3-42}$$

The stress-inducing inductance (L_s – M_s) in Chapter 2 was designed in order to be comparable with that of the baseline design. The lead length is minimized in this Chapter to alleviate the influence of the passive balancing solution (shown in Fig. 3-2) on voltage stress. A realization of negatively coupled inductors is shown in Fig. 3-7(a), which is wound bifilarly using copper wires. The Q3D simulation results in Fig. 3-7(b) suggest that both mutual and self-inductances are stable from 10 MHz for 110 MHz, which is wide enough to cover almost all possible ringing frequencies during switching transients. The coupling coefficient of this solenoid structure is close to -1. In real case, zero lead length is not practical. A little leads are required for soldering. Those extra leads will increase the leakage inductances and reduce the coupling coefficient. The resulting current-balancing inductance (L_s + M_s) will be a little larger according to (3-42), but should not deviate from the simulation shown in Fig. 3-7(b) too much if the leads are cut as short as possible.





(a) **(b)**

Fig. 3-7. (a) Air-cored negatively-coupled inductors with *r* = 1.9 mm and *n* = 4; (b) simulated self-inductance and mutual inductance by Q3D extractor from 10 MHz to 110 MHz.

Current balancing inductance ($L_s + M_s$) can be changed by varying the number of turns while keeping the radiuses of solenoid and winding wire the same. The simulation results are shown in Table 3-1. The coupling coefficients are close to -1 and the inductances are stable from 10 MHz for 110 MHz for all the cases.

Table 3-1. Simulation results of coupled inductors with different number of turns

f_s = 10 MHz to 110 MHz	n=2	n=3	n=4	n=5
Self-inductance (nH)	12.7	22.5	33.1	44.1
Mutual inductance (nH)	12.2	21.8	32.1	42.9
Coupling coefficient	-0.96	-0.97	-0.97	-0.97

With design guideline derived and the realization of coupled inductors determined, the design process of passive balancing solution in Fig. 3-2 is recommended in Fig. 3-8. The $\max|\Delta i_{ds(pk)}|$ should be determined first. Then, constants ΔV_{th}, t_r, and L_{cm} in design guideline (3-40) are obtained by datasheet, simulation, or measurement. Because the radiuses of solenoid and winding wire (which are illustrated in Fig. 3-7(b)) are kept the same, the achievable current-balancing inductances ($L_s + M_s$) are discrete series and are related to the number of turns, as listed in Table 3-1. Then, drive-source resistances R_k are calculated by (3-40) for different turns of coupled L_s. A proper combination of R_k and coupled L_s can be chosen based on the needs of designers. The value of R_k can be rounded for easier implementation. Next, the designed coupled L_s is manufactured and measured. The coupled inductors are not properly made and need to be tuned (for less lead length or more uniform windings) if the measured ($L_s + M_s$) deviates from the simulated result shown in Table 3-1 too much (for example, larger than 5 nH). Finally, the $\max|\Delta i_{ds(pk)}|$ is updated for the manufactured coupled inductors and the rounded R_k based on (3-40).

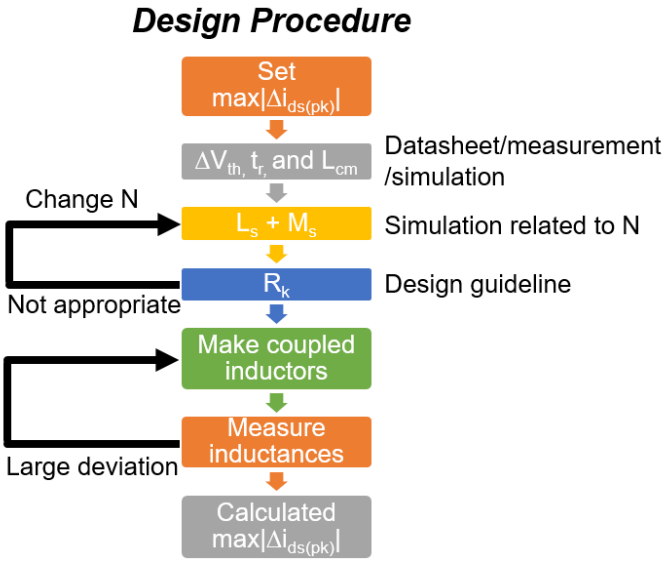


Fig. 3-8. Design procedure of passive balancing solution in Fig. 3-2.

3.3 Experimental Validation

Double pulse tester (DPT) was employed to test the switching transients of baseline design and worst-case design. The same test board was utilized for all the tests to ensure consistency. The only differences are the values of coupled L_s and R_k. The instant balancing capability of passive solution can be demonstrated because DPT only tests two short pulses. Common-source inductance L_{cm} is from MOSFET package and will not be increased intentionally because it greatly increases the switching loss.

3.3.1 Baseline Tests

Fig. 3-9 shows the prototype of the baseline design. The DUTs were two SiC MOSFETs (C2M0160120D) from Wolfspeed rated at 1200 V, 19 A, and 160 mΩ. Their threshold voltages were found to be 3.7 V and 4.8 V by measurements. The freewheeling SiC diode was C4D20120A from Wolfspeed rated at 1200 V and 54.5 A. Drain-source voltages and drain-source currents were

measured for the calculation of switching energy and peak-current difference. A differential voltage probe THDP0200, with enough dynamic range and bandwidth, was employed to measure v_{ds}. Power-source current difference Δi_s is smaller than drain-source current difference Δi_{ds} according to Fig. 2-38. Drain current difference Δi_d was measured to approximate Δi_{ds} instead due to the negligible difference of displacement currents from C_{ds} and C_{gd} between paralleled MOSFETs. Two TCP0030A current probes were utilized to measure drain currents and two cutouts were prepared for probe insertion. Openings for insertion of extra R_k and coupled L_s were shorted by jumpers in baseline design in order to reveal the currant mismatch induced by V_{th} variation.

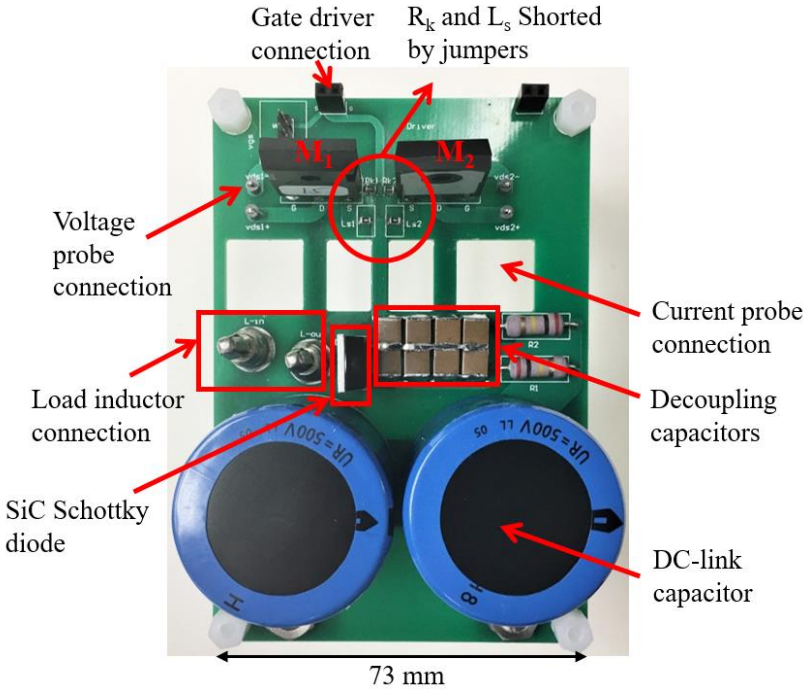


Fig. 3-9. Prototype for baseline test of current and switching energy unbalance.

Five passive parameters, i.e., L_s, M_s, L_{cm}, L_k, and R_k, are influencing the balancing performance of solution shown in Fig. 3-2. Some of them are from device package, some of them are from PCB layout, and some of them can be varied by the insertion of extra resistance or inductance. The determination of L_s, M_s, L_{cm}, L_k, and R_k are shown in Table 3-2, where subscript "int", "pcb", and "insert" denote parameters from internal package of devices, PCB layout, and externally inserted, respectively. The parasitic inductances from PCB layout are extracted by Q3D extractor. Parasitic inductances from package can be achieved by impedance analyzer. The inductances in datasheet over-estimate the values because only part of a lead is connected to the circuit. Between any of the three terminals of a MOSFET, a series resonant tank is formed, as shown in Fig. 3-10. With known capacitance at zero voltage, the sum of two of the three inductances can be calculated by the measured resonant frequency. Inductance L_{d_int}, L_{g_int}, and L_{s_int} can then be solved by three measurements between drain and gate, drain and source, and gate and source. Openings for insertion of extra R_k and coupled L_s were shorted by jumpers in the baseline design. Threshold voltage mismatch and parameters related to current balancing in baseline test are listed in Table 3-3.

Table 3-2. Determination of L_s, M_s, L_{cm}, L_k, and R_k shown in Fig. 3-2

R_k	L_s	M_s	L_k	L_{cm}
R_{k_insert}	$L_s = L_{s\_pcb} + L_{s\_insert}$	M_{s_insert}	L_{k_pcb}	L_{s_int}

Table 3-3. Threshold voltage mismatch and parameters related to current balancing in baseline test

ΔV_{th} (V)	R_k (Ω)	$L_s = L_{s\_pcb}$ (nH)	M_s (nH)	$L_k = L_{k\_pcb}$ (nH)	$L_{cm} = L_{s\_int}$ (nH)
-1.1	0	4.19	0	1.85	4.1

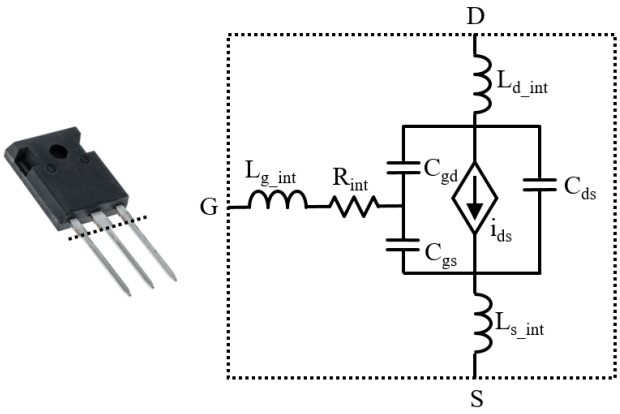


Fig. 3-10. Equivalent circuit of discrete MOSFET.

The waveforms of the baseline design tested at 600 V, 20 A, and 5 Ω are shown in Fig. 3-11. MOSFET M1 (which has a smaller threshold voltage) carries more current than M2 during both turn-on and turn-off switching transients. The measured peak-current difference is 3.26 A. The balancing effects of L_s, L_k, and L_{cm} in Table 3-3 are not strong enough to remove the mismatch between paralleled MOSFETs induced by -1.1 ΔV_{th}. In addition, current unbalance during turn-on switching transient cannot be damped quickly and will be transferred to on state, as shown by the turn-on waveforms in Fig. 3-11.

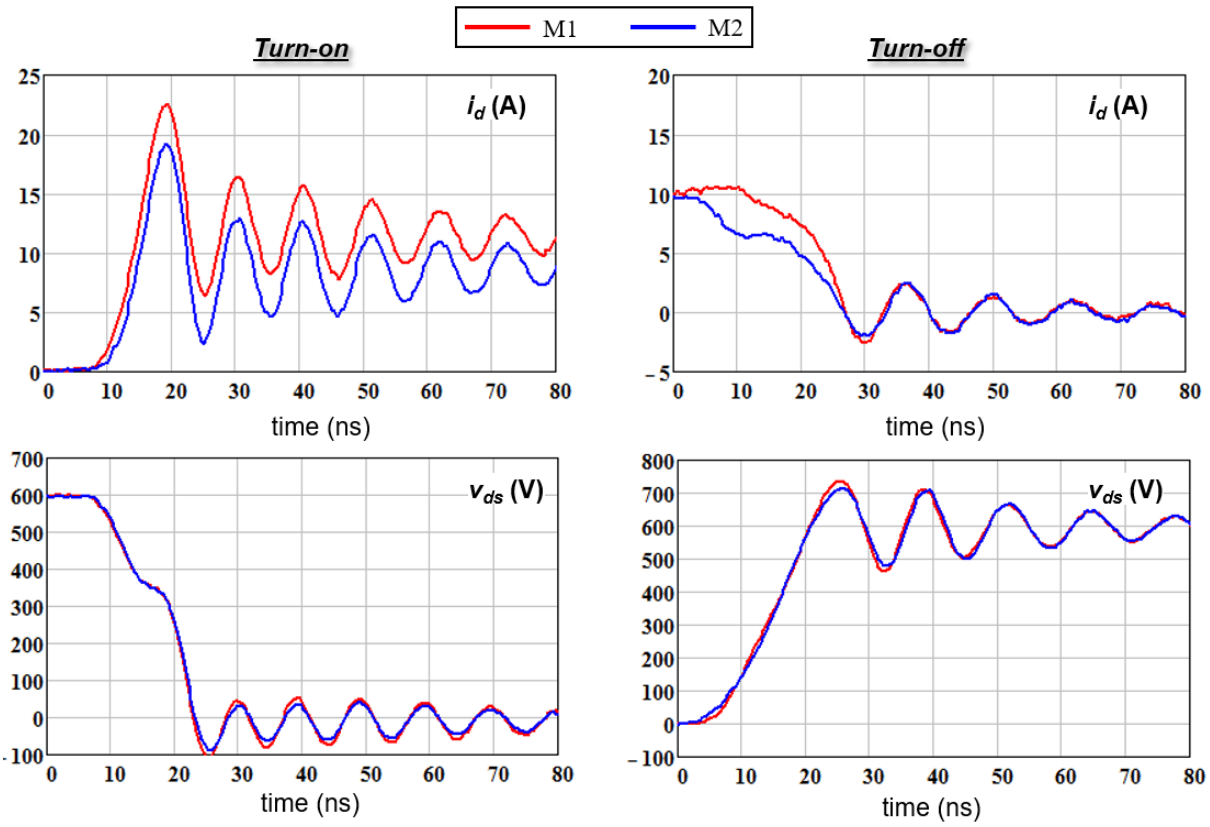


Fig. 3-11. Experimental switching transients of baseline test (with balancing parameters shown in Table 3-3). Test conditions are V_{in} = 600 V, I_{in} = 20 A, R_g = 5 Ω.

The baseline design was also tested under different operating conditions. The measured peak-current differences are shown in Fig. 3-12. According to the plot, ΔI_{pk} increases with I_{in} and stays almost the same for different switching speed when the balancing effect is slight. The calculated peak-current mismatch percentage ($\Delta I_{pk}/0.5I_{in}$) varies from 26% to 59%. More severe unbalance will be transferred to on state under higher I_{in} as ΔI_{pk} is larger. On the other hand, the current mismatch percentage is greater under smaller I_{in} and causes higher switching energy mismatch percentage.

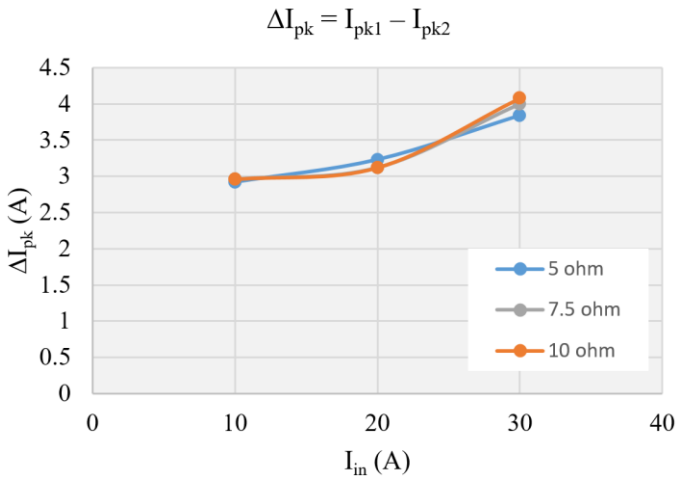
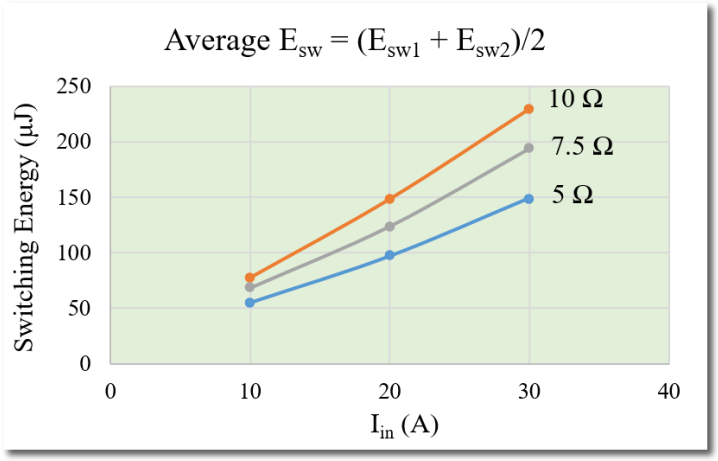
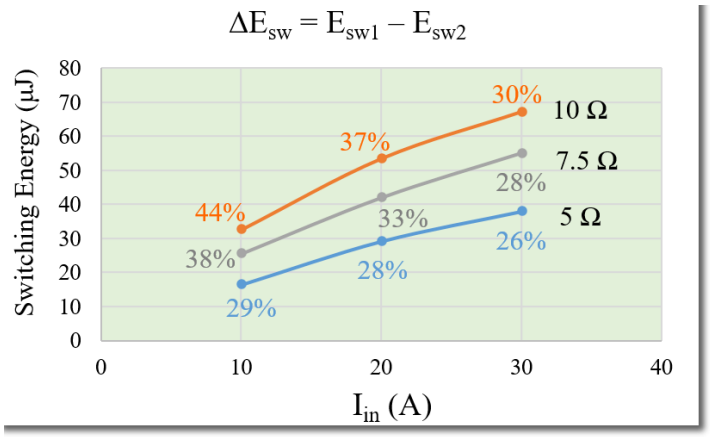


Fig. 3-12. Tested ΔI_{pk} under variant operating conditions with parameters shown in Table 3-3.

Average switching energies E_{sw} and switching energy mismatches ΔE_{sw}, under different operating conditions, are compared in Fig. 3-13. The switching energies were calculated by the integration of instantaneous power ($i_{ds}*v_{ds}$) during turn-on and turn-off transients. Even though drain currents were measured because channel currents cannot be directly sensed, it is important to note that the energy stored in output capacitance C_{oss} during turn-off transient will be dissipated in the channel during turn-on transient. The total switching energy E_{swj} ($E_{swj} = E_{swjon} + E_{swjoff}$, j=1, 2) won't be affected by the currents bypassed though parasitic capacitors. According to Fig. 3-13, average E_{sw} and ΔE_{sw} increase with input current I_{in} and external gate resistance R_g. The switching energy mismatch percentage is as high as 44% and increases with reducing I_{in}, which is consistent with previous analysis. Even though ΔI_{pk} are kept almost the same under different switching speeds (as shown in Fig. 3-12), the current and/or voltage rises and/or falls slower with larger R_g resulting in higher switching energy mismatch.



(a)



(b)

Fig. 3-13. Comparison of tested (a) average E_{sw} and (b) ΔE_{sw} (with mismatch percentage listed) under variant operating conditions for base line design. Parameters influencing current unbalance are shown in Table 3-3.

3.3.2 Worst-Case Design for A Wide Operating Range

As peak-current mismatch and switching energy mismatch vary with operating conditions, a worst-case design that is valid for wide operating range would be preferred. The only parameter that changes with operating conditions in the design guideline (3-40) is t_r, which increases with input current I_{in} and gate resistance R_g. This was proved by both simulations in Appendix A and experiments in Fig. 2-65. Among all the tests shown in Fig. 3-13, the turn-on transient under 30 A

and 10 Ω has the longest t_r, which is measured to be 16 ns. The passive balancing solution designed based on t_r = 16 ns should also be effective for other conditions, as demonstrated in the later experiments.

Following the design procedure shown in Fig. 3-8, the max|$\Delta i_{ds(pk)}$| = 0.5 A (5 % for 20 A I_{in}) was determined first. Then ΔV_{th} = -1.1 V, t_r = 16 nH, and L_{cm} = 4.1 nH were obtained by measurements. Based on the simulated inductances of coupled inductors in Table 3-1, the corresponding R_k can be solved from (3-40) for different turns of coupled L_s, as shown in Fig. 3-14. The value of R_k for N = 2 is not shown because no solution could be found. According to Fig. 3-14, the required R_k is reduced by more than 1 Ω when the number of turns increases from 3 to 4 and doesn't change too much when the number of turns increases from 4 turns to 5 turns. The design with N = 4 and R_k = 4 Ω was finally chosen as worst-case design.

The designed negatively-coupled inductors were manufactured as illustrated in Fig. 3-15(a). Two copper wires were wound and interleaved together. Terminal 1 and 2 are for L_s of M1; Terminal 3 and 4 are for L_s of M2. The arrows indicate the directions of currents during switching transients. The leads were cut short (as indicated by the straight line) to reduce the leakage inductance which tends to increase the voltage stress during turn-off transient as determined by (3-41). Fig. 3-15(b) shows the photo of hardware with designed coupled power-source inductors and resistors inserted. The inductances of coupled inductors in Fig. 3-15(a) were measured by impedance analyzer and plotted in Fig. 3-16. Fig. 3-16(a) illustrates the self-inductance which was measured by opening one port (e.g., 1 and 2) and measuring from the other one (e.g., 3 and 4). The two self-inductances have similar values and don't change significantly between 10 MHz and 110 MHz (which is the practical range of ringing frequencies) as predicted by simulation. The value at 90 MHz (which is the ringing frequency observed in the experiment) was used in the design. Fig.

3-16(b) plots the measured intermediate inductance for the calculation of mutual inductance. It was measured by shorting one port and measuring from the other one. The mutual inductance is then calculated by $M_s = \sqrt{L_{s1}(L_{s1} - L')}$. The flat curve of L' indicates that mutual inductance is also stable between 10 MHz and 110 MHz.

According to Fig. 3-16 and Q3D simulation, the resulting L_s and M_s are calculated as

$$L_s = L_1 + L_{s\_pcb} = 36.1 + 4.19 = 40.3\,nH \tag{3-43}$$

$$M_s = \sqrt{L_1(L_1 - L')} = 29.6\,nH \tag{3-44}$$

The passive current balancing components for worst case design are summarized in Table 3-4.

The measured (L_1 + M_s) is 65.7 nH and is close to the simulation shown in Table 3-1. Finally, max|$\Delta i_{ds(pk)}$| = 0.48 A was updated and calculated by (3-40).

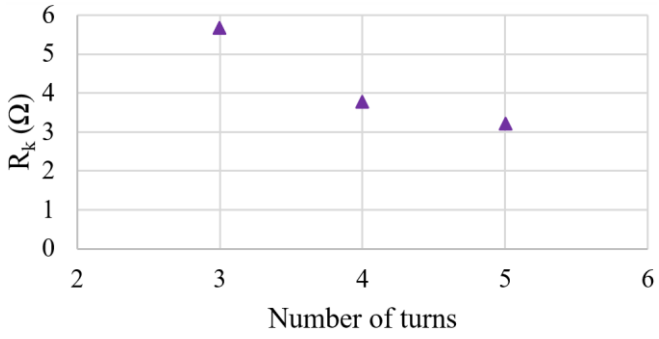
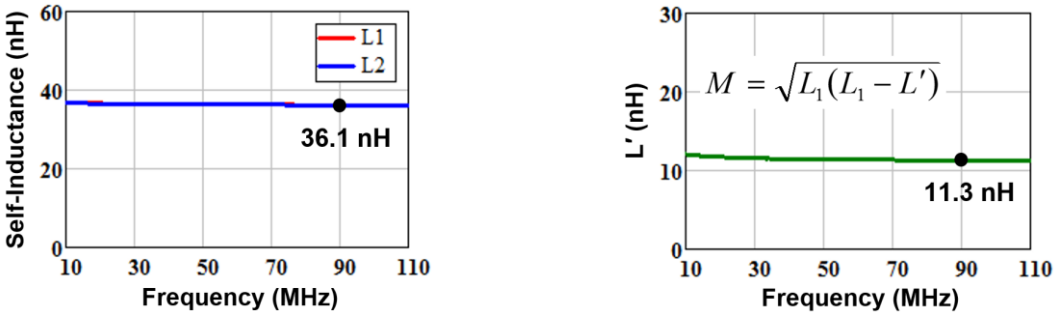


Fig. 3-14. Design of R_k based on design guideline (3-40) and simulation results of coupled inductors in Table 3-1. The other parameters are max|$\Delta i_{ds(pk)}$| = 0.5 A, t_r = 16 ns (from baseline design tested at V_{in} = 600 V, I_{in} = 30 A, R_g = 10 Ω), ΔV_{th} = -1.1 V, L_{s_pcb} = 4.19 nH, L_{k_pcb} = 1.85 nH, and L_{cm} = 4.1 nH.

(a) **(b)**

Fig. 3-15. (a) Fabricated coupled inductors, and (b) photo of hardware with designed coupled power-source inductors and resistors inserted.



(a) **(b)**

Fig. 3-16. (a) Measured self-inductances of coupled inductors, and (b) measured intermediate inductance for the calculation of mutual inductance.

Table 3-4. Threshold voltage mismatch and current balancing parameters in the tests of worst case design

ΔV_{th} (V)	R_k (Ω)	$L_s = L_1 + L_{s\_pcb}$ (nH)	M_s (nH)	$L_k = L_{k\_pcb}$ (nH)	$L_{cm} = L_{s\_int}$ (nH)
-1.1	4	40.3	29.9	1.85	4.1

The switching waveforms tested at 600 V, 20 A, and 5 Ω for current balancing design in Table 3-4 are shown in Fig. 3-17. The measured difference of peak currents is reduced from 3.26 A to 0.1 A. The desired current sharing ($|\Delta i_{ds(pk)}| < 0.5$ A) is obtained by a single gate driver from the first switching cycle as demonstrated by the double-pulse test which captures switching transients at the first falling and rising edges. Good sharing at the peak also prevents the mismatch during

switching transient being transferred to on state. Much better sharing is also achieved for turn-off transient compared to the baseline shown in Fig. 3-11.

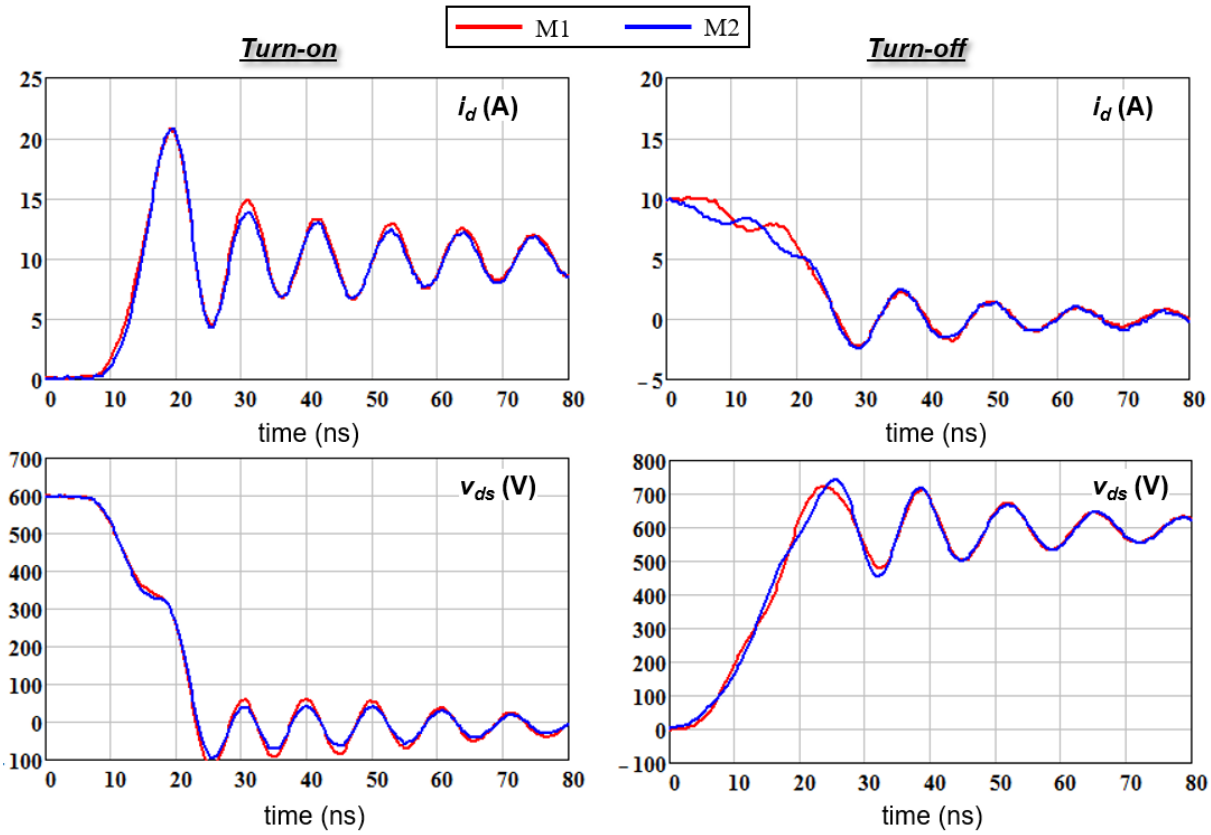
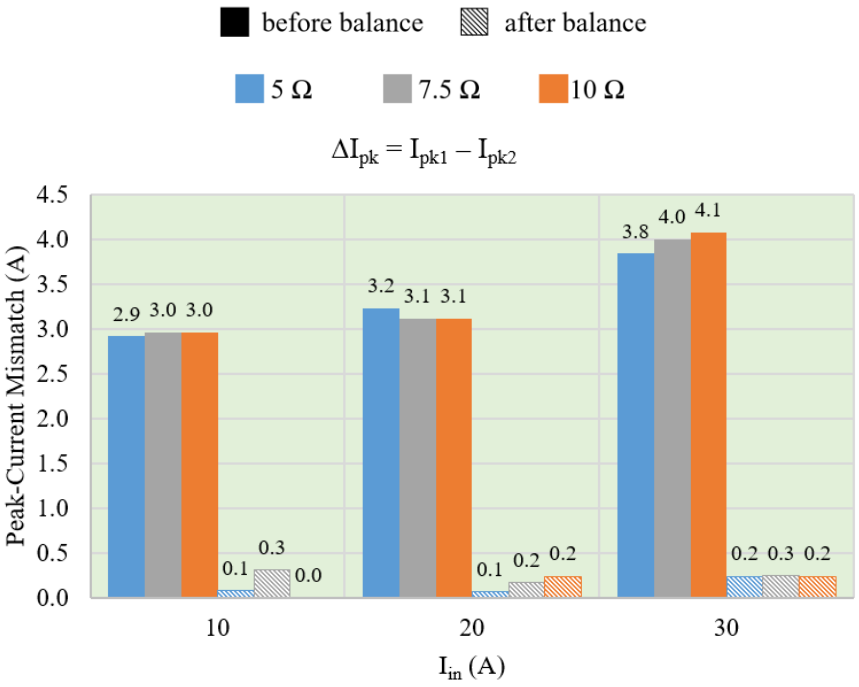


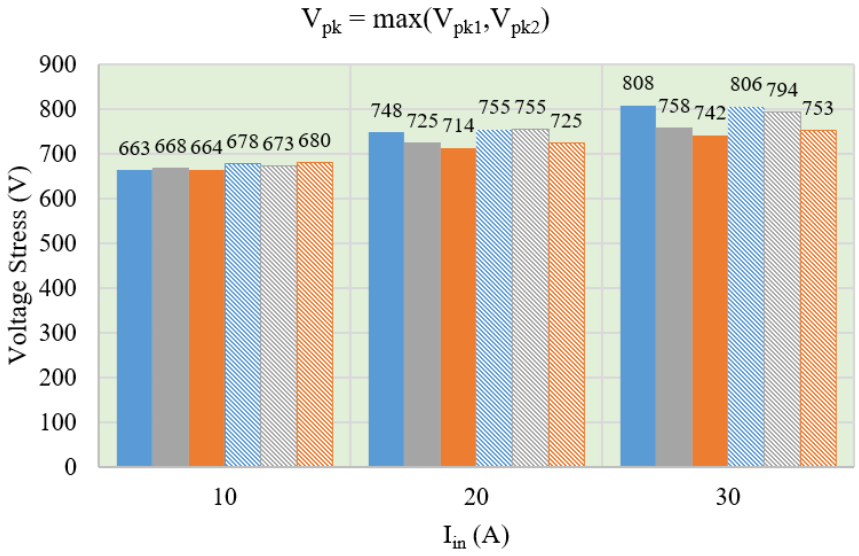
Fig. 3-17. Experimental switching transients of worst case balancing solution (with balancing parameters shown in Table 3-4). Test conditions are V_{in} = 600 V, I_{in} = 20 A, R_g = 5 Ω.

Tests at variant operating conditions were conducted to demonstrate the capability of providing forced sharing over wide operating range by one worst-case design. The comparison of peak-current mismatches between the baseline design (solid bars) and worst-case design (dashed bars) are shown in Fig. 3-18(a). According to the plots, peak-current differences could be reduced by 20 times and were below 0.5 A for all the operating conditions.

Comparison of turn-off voltage stresses between the baseline design (solid bars) and worst-case design (dashed bars) are shown in Fig. 3-18(b). With the exception of coupled L_s and R_k, the same board was employed for all the tests to keep layout and components the same for fair comparison. The increase in voltage spike, which is induced by the extra stress-inducing inductance from balancing design ($\Delta(L_s - M_s)$ = 6.2 nH), is almost negligible compared to input voltage (V_{in} = 600 V). In practical design, the unnecessary L_s (4.19 nH) on this prototype PCB can be eliminated. The extra stress inductance from balancing design can be reduced to 2 nH.



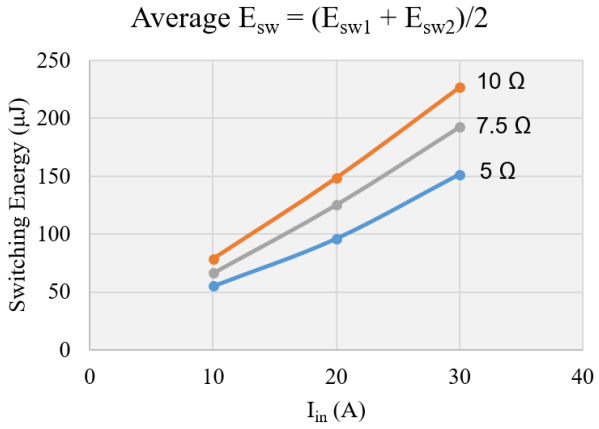
(a)



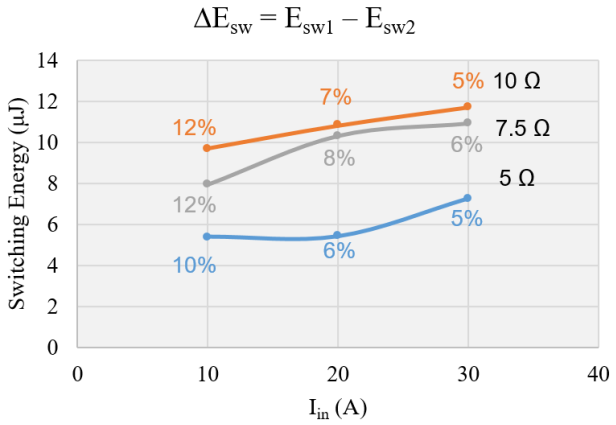
(b)

Fig. 3-18. (a) Comparison of peak-current difference before and after balance under variant operating conditions, and (b) comparison of peak drain-source voltage before and after balance under variant operating conditions.

Average switching energies E_{sw} and switching energy mismatches ΔE_{sw} under variant operating conditions for worst-case design are shown in Fig. 3-19. Average E_{sw} and ΔE_{sw} increased with input current I_{in} and external gate resistance R_g. The resulting switching energy mismatch percentage is as low as 5%.



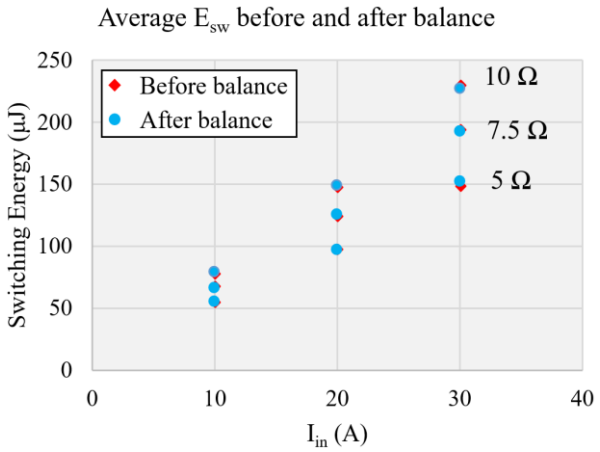
(a)



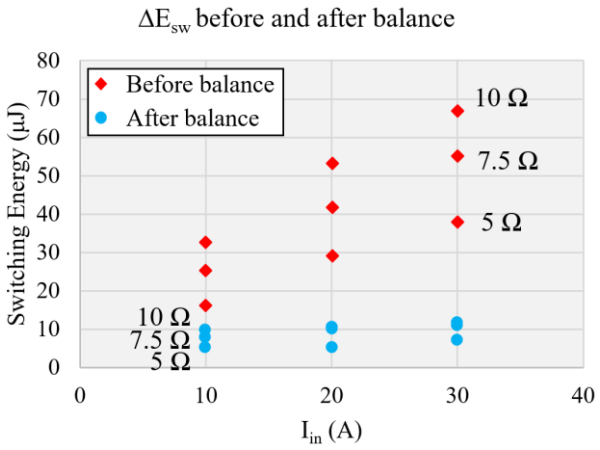
(b)

Fig. 3-19. Comparison of tested (a) average E_{sw} and (b) ΔE_{sw} (with mismatch percentage listed) under variant operating conditions for worst case design. Parameters influencing current sharing are shown in Table 3-4.

Fig. 3-20 compares the average switching energies and switching energy mismatches between baseline design (before balance) and worst-case design (after balance) in Table 3-4, which is valid for a wide operating range. According to the comparison, the proposed worst-case balancing design didn't increase the average switching energy and reduced the switching energy mismatch by 6 times compared to the baseline tests shown in Fig. 3-13(b).



(a)



(b)

Fig. 3-20. (a) Comparison of average E_{sw} before and after balance under variant operating conditions, and (b) comparison of ΔE_{sw} before and after balance under variant operating conditions.

3.4 Conclusion

A passive balancing solution is investigated to balance the peak currents caused by unequal threshold voltages between paralleled discrete SiC MOSFETs. All the balancing-effective passive components, including L_s, M_s, L_k, R_k, and L_{cm}, are considered. A design guideline involving the magnitude of V_{th} mismatch, current rise time, and maximum peak-current difference is derived to guide the choice of passive components. The detailed design procedure of the passive balancing solution in Fig. 3-2 is recommended to force currents to share over wide operating range. Current/voltage sensors, feedback loop, multiple gate drivers, and the knowledge of the polarity of V_{th} difference are not required. The difference of peak currents can be limited to a predetermined value by passive components without sacrificing the total switching loss and voltage stress. The accuracy of design guideline and the effectiveness of worst case design over wide operating range were demonstrated by two paralleled SiC MOSFETs (C2M0160120D) tested at variant operating conditions. The difference of peak currents was reduced by 20 times and below 0.5 A in every switching transient. The average switching energy was not increased. The switching energy

mismatch was reduced by 6 times. The increase in voltage spike was almost negligible compared to input voltage (V_{in} = 600 V). The methods shown in Fig. 3-2 can be extended to the case of more than two MOSFETs in parallel (as shown in Appendix B) because they don't need to consider the asymmetry of V_{th} and uses one gate driver.

Chapter 4 Modeling of Paralleled SiC MOSFETs with Mismatched Threshold Voltages

Nomenclature

V_{th}	Threshold voltage
L_d	Drain inductance
L_s	Power-source inductance
L_p	Power-loop inductance
L_{cm}	Common-source inductance
L_{kg}	Drive-gate inductance
L_k	Drive-source inductance
L_g	Gate-drive inductance
g_{fs}	Large signal transconductance
V_{in}	Input voltage of double-pulse tester
I_{in}	Input current of double-pulse tester
R_g	Gate resistor of double-pulse tester
i_{ds}	Channel current of MOSFET
v_{ds}	Drain-source voltage of MOSFET
v_{gs}	Gate-source voltage of MOSFET
i_{kg}	Gate charging current of MOSFET
E_{sw}	Switching energy
I_{pk}	Peak channel current
V_{pk}	Peak drain-source voltage

M	Mutual inductance
r	Radius of air-cored coupled inductors
n	Number of turns
L_{insert}	Inserted inductance
L_{int}	Inductance inside package
L_{pcb}	Inductance from PCB layout
C_{oss}, C_{iss}	Output capacitance and input capacitance of MOSFET
C_{gs}, C_{ds}, C_{gd}	Gate-source capacitance, drain-source capacitance, Miller capacitance
C_j	Junction capacitance of diode

4.1 Introduction

The peak currents between two paralleled SiC MOSFETs could differ significantly due to the mismatch in threshold voltages (V_{th}). Current unbalance among the MOSFETs leads to mismatched switching energies, which is a concern as it affects the reliability of the paralleled structure. Most of the studies on balancing of paralleled devices focus on current sharing [97]-[103]. The switching energy mismatch caused by V_{th} variation is seldom calculated due to the complex mathematics. The two key parameters to reveal the severances of unbalance are switching energy mismatch in (4-1) and switching energy mismatch percentage in (4-2).

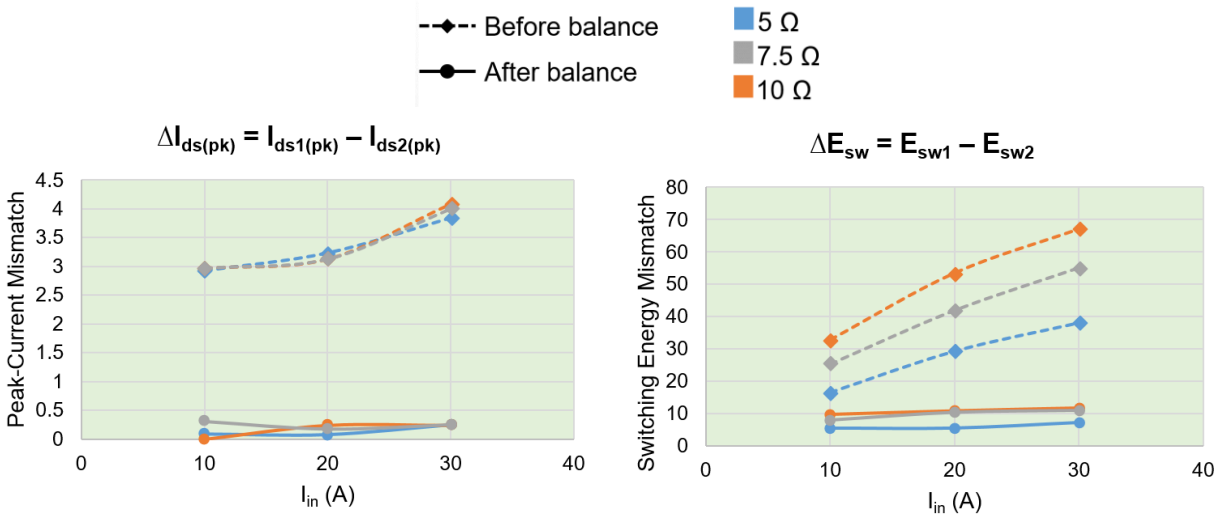
$$\Delta E_{sw} = E_{sw1} - E_{sw2} \tag{4-1}$$

$$Switching\ energy mismatch\ percentage = \frac{\Delta E_{sw}}{0.5\left(E_{sw1} + E_{sw2}\right)} \times 100\% \tag{4-2}$$

Switching energy mismatch ΔE_{sw} is not equal or proportional to peak-current mismatch $\Delta i_{ds(pk)}$ even though both can be reduced by passive balancing method. Fig. 4-1 shows the comparison of

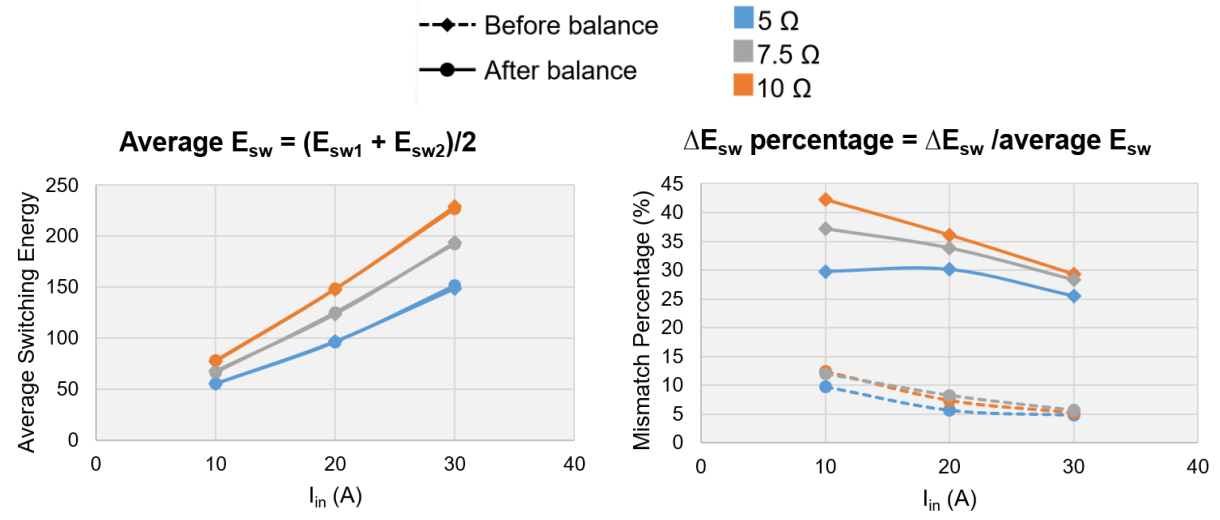
peak-current mismatch and switching energy mismatch before and after balance under variant operating conditions. Switching energy mismatch is influenced by switching speed with the same peak-current mismatch. Fig. 4-4 shows the comparison of average switching energy and switching energy mismatch percentage before and after balance under variant operating conditions. The average switching energy as a function of operating conditions also needs to be modeled to achieve the corresponding mismatch percentage.

Device modeling and circuit modeling are two necessary parts to achieve the accurate results of switching transients. For devices, the following needs to be modeled based on either measurement results or datasheet values: channel performance, parasitic inductors from package, and voltage dependent parasitic capacitors [104]-[110]. For circuits, all the layout parasitics need to be extracted and modeled. Common-source inductance L_{cm}, drive-source inductance L_k, drive-source resistance R_k, power-source inductance L_s, and mutual-inductance between power-source inductors have balancing effect according to the previous Chapters. All of them will be considered in the modeling process to accurately calculate the mismatch in switching energies. Other parasitic inductances exist in layout, i.e., power-loop inductance L_p, drain inductance L_d, drive-gate inductance L_{kg}, and gate inductance L_g, are also included for generality. The complete schematic is illustrated in Fig. 4-3, where inductances on the same trace are lumped together. The more parasitics considered, the more accurate will the model be, however, at the expense of more complex mathematics. The constructed model can't be solved in most of the times because of the order of system, especially when paralleled MOSFETs are considered. This Chapter will discuss how to model devices and how to simplify the mathematics of this high order system. The accuracy of the derived model will be experimentally demonstrated. The influence of L_{cm} and ΔV_{th} are also discussed based on modeling results.



(a) **(b)**

Fig. 4-1. (a) Comparison of peak-current mismatch and (b) comparison of switching energy mismatch before balance (with bassline design shown in Table 3-3) and after balance (with balancing design shown in Table 3-4) under variant operating conditions.



(a) **(b)**

Fig. 4-2. (a) Comparison of average switching energy and (b) comparison of switching energy mismatch percentage before balance (with bassline design shown in Table 3-3) and after balance (with balancing design shown in Table 3-4) under variant operating conditions.

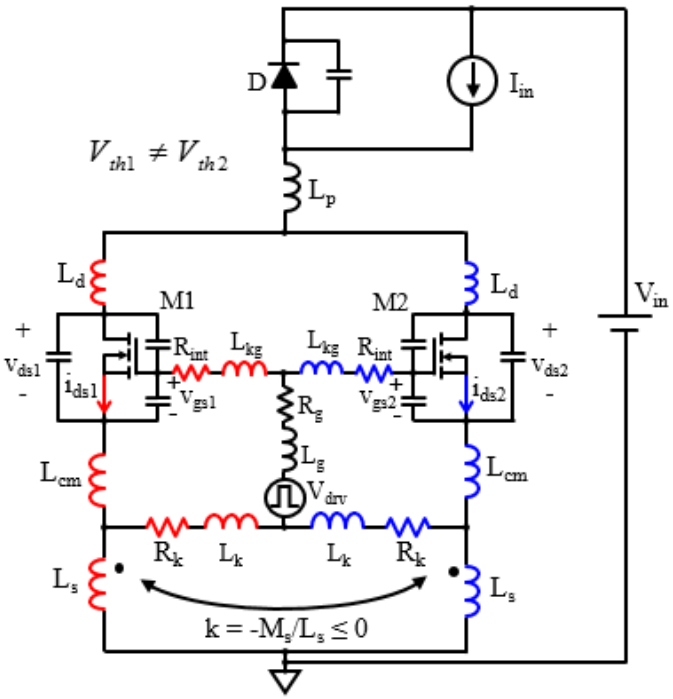


Fig. 4-3. Schematic with parasitic inductances and passive balancing components.

4.2 Modeling of Device Parameters

Two SiC MOSFETs (C2M0120160D from Wolfspeed) in To-247 package are paralleled and are the devices under test (DUTs). The freewheeling diode is SiC Schottky diode (C4D20120A from Wolfspeed) in TO-220 package. Both MOSFET and diode contain parasitic inductances and voltage dependent parasitic capacitors. Their equivalent circuits are shown in Fig. 4-4, where dashed lines indicate the positions soldered on the printed circuit board (PCB) and “int” denotes parameters inside the package of devices.

Two SiC MOSFETs with unequal threshold voltages are selected. Their measured transfer characteristics are shown in Fig. 4-5(a) by solid lines. During switching transient, the channel of SiC MOSFET can be modeled by

$$i_{ds_j} = g_{fs}\left(v_{gs_j} - V_{th_j}\right)^2, v_{gs_j} > V_{th_j}, j = 1,2 \tag{4-3}$$

where V_{th} is threshold voltage. Subscript j indicates the corresponding MOSFETs (M1 or M2). The large-signal transconductance g_{fs} is assumed to match for both MOSFETs.

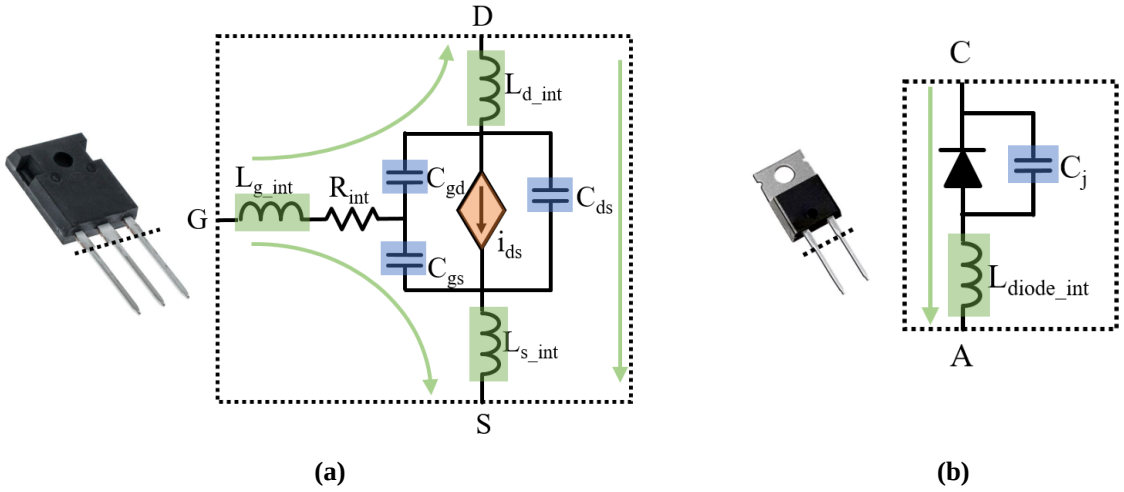


Fig. 4-4. (a) Equivalent circuit of discrete MOSFET, and (b) equivalent circuit of discrete diode.

The g_{fs} and V_{th} in (4-3) are solved using MATLAB by curve fitting. The results are listed in Table 4-1. Even though a power of 2.5 in (4-3) can make the fitting a little better, an integer power of 2 can greatly simplify mathematics without losing too much accuracy (the residual sum of square is only 2.05), especially in the high current region which is the most important range contributing to switching energy and current mismatch. According to Table 4-1, the threshold voltage mismatch ΔV_{th} between two MOSFETs is 1.1 and the large-signal transconductance g_{fs} is 0.57S/V when quadratic relationship is applied. The modeled transfer curves are plotted in Fig. 4-5(a) by dashed lines. Good matching between measurement and modeling is achieved.

The voltage dependent non-linear capacitors, including input capacitance C_{iss}, output capacitance C_{oss}, reverse transfer capacitance C_{rss}, and diode junction capacitance C_j, are modeled by

$$C = f(V) \tag{4-4}$$

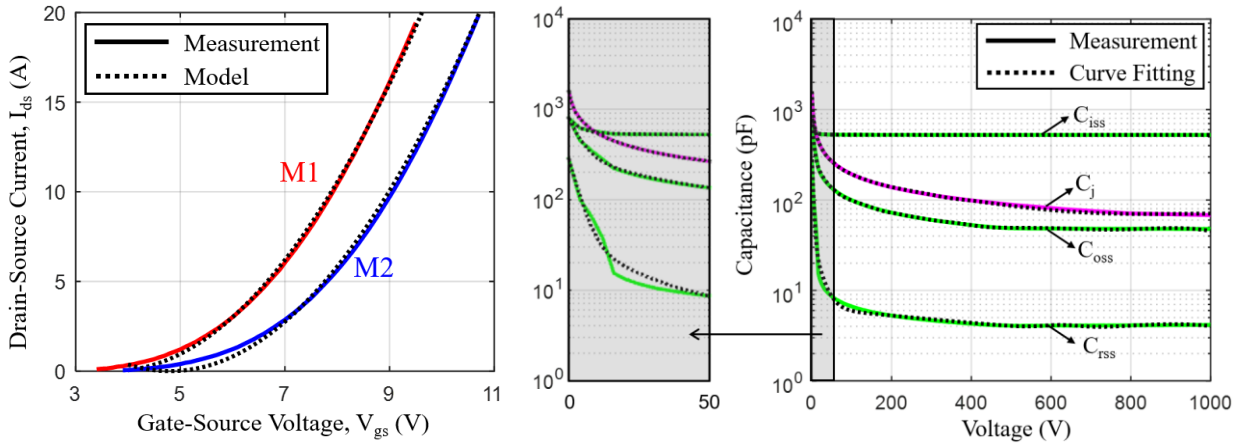
where V is drain-source voltage V_{ds} of MOSFET or reverse blocking voltage V_R of diode. Function f can be extracted by curve fitting using MATLAB (as shown in Appendix D) as

$$y = a_1 e^{-\left(\frac{x-b_1}{c_1}\right)^2} + \ldots + a_8 e^{-\left(\frac{x-b_8}{c_8}\right)^2} \tag{4-5}$$

where Gaussian model is applied because it provides the most accurate matching among all the curve fitting functions in MATLAB.

The comparisons between measurements (solid lines) and modeling results (dashed lines) are shown in Fig. 4-5(b). The fitted curves match well with measurements over wide voltage range. Good accuracy is also achieved near zero voltage, where capacitances change very fast.

Parasitic inductances from package are obtained by impedance measurement using impedance analyzer. The inductances provided in datasheet will over-estimate the values because only part of a lead is connected to the circuit. Between any two of the three terminals of a MOSFET, a series resonant tank is formed (as indicated by the green arrows in Fig. 4-4(a)). With known capacitances at zero voltage, the sum of any two of the three inductances (i.e., L_{d_int}, L_{g_int}, and L_{s_int}) can be calculated by the measured resonant frequencies. Inductance L_{d_int}, L_{g_int}, and L_{s_int} are then solved by three measurements between drain and gate, drain and source, and gate and source. Similar method is employed to measure L_{diode_int}. The results are shown in Table 4-1.



(a) **(b)**

Fig. 4-5. (a) Comparison of transfer curves obtained by measurement (solid lines) and model in (4-3) (dashed lines), and (b) comparison of parasitic capacitances C_{iss}, C_{oss}, C_{rss}, and C_j obtained by measurement (solid lines) and curve fitting (dashed lines).

Table 4-1. Extracted Parameters of MOSFET and Diode Shown in Fig. 4-4

V_{th1} (V)	V_{th2} (V)	g_{fs} (S/V)	R_{int} (Ω)	L_{d_int} (nH)	L_{g_int} (nH)	L_{s_int} (nH)	L_{diode_int} (nH)
3.7	4.8	0.57	6.5	1.5	4.3	4.1	6.3

4.3 Transforming Modeling of Paralleled MOSFETs to Single MOSFET

The goal of modeling is to solve for switching energy mismatch in (4-1) and switching energy mismatch percentage in (4-2). The complete schematic in Fig. 4-3 has 12 inductors, 7 non-linear capacitors, and 2 DUTs. The structure needs to be simplified to reduce the number of passive components and/or number of devices to simplify the solving process and mathematics. According to the parametric analysis in Fig. 2-3, impedance on the drive-gate trace has slight influence on balancing and switching energy. Thus, can be moved to terminal as shown in Fig. 4-6. However, switching energy calculation of circuit in Fig. 4-6 is still challenging. Fig. 4-6 will be further simplified by transforming the problem of two MOSFETs in parallel to a single MOSFET. Fewer

parasitics need to be considered and conventional modeling of one MOSFET can be applied. The details are as follows.

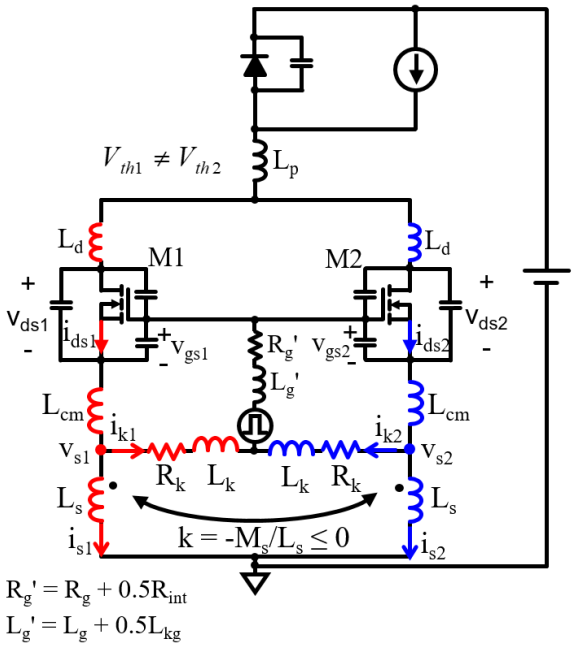


Fig. 4-6. Simplification of circuit shown in Fig. 4-3.

Switching energy is obtained by integration of instantaneous power, which can be expressed by

$$P_j = i_{ds_j} v_{ds_j}, \; j = 1,2 \tag{4-6}$$

where i_{ds} is drain-source current (or channel current), v_{ds} is drain-source voltage, subscript i denotes the corresponding variable of M1 or M2.

Switching energy difference can be obtained from (4-6) as

$$\Delta E_{sw} = \int \Delta P dt = \int \left(v_{ds} \Delta i_{ds} + \Delta v_{ds} i_{ds} \right) dt \tag{4-7}$$

where x denotes the average of two terms and Δx means the difference of two terms, namely,

$$\Delta x = x_1 - x_2, x = 0.5\left(x_1 + x_2 \right) \tag{4-8}$$

Similarly, Δi_{ds} in (4-7) can be derived from (4-3) as

$$\Delta i_{ds} = 2 g_{fs} \left(v_{gs} - V_{th} \right) \left(\Delta v_{gs} - \Delta V_{th} \right) = f\left(v_{gs}, \Delta v_{gs} \right) \tag{4-9}$$

which is a function of average of gate-source voltages v_{gs} and difference of gate-source voltages Δv_{gs}.

Voltage Δv_{ds} in (4-7) can be obtained by KVL of the loop formed by L_d, C_{ds}, and C_{gs}:

$$\Delta v_{ds} = \Delta v_{gs`} - L_d \frac{d\Delta i_{ds}}{dt} = f\left(v_{gs}, \Delta v_{gs} \right) \tag{4-10}$$

which also is a function of average of gate-source voltages v_{gs} and difference of gate-source voltages Δv_{gs}.

According to (4-9) and (4-10), both Δi_{ds} and Δv_{ds} are functions of Δv_{gs}, which is produced by passive balancing components including L_{cm}, R_k, L_k, and coupled L_s. From Fig. 4-6, equations can be constructed to solve for Δv_{gs}:

$$\begin{cases} \Delta v_{gs} = -L_{cm} \dfrac{d\Delta i_{ds}}{dt} - \left(L_s + M_s \right) \dfrac{d\Delta i_s}{dt} \\ \Delta v_{gs} = -L_{cm} \dfrac{d\Delta i_{ds}}{dt} - R_k \Delta i_k - L_k \dfrac{d\Delta i_k}{dt} \\ \Delta i_s + \Delta i_k \approx \Delta i_{ds} \\ \Delta i_{ds} = 2 g_{fs} \left(v_{gs} - V_{th} \right) \left(\Delta v_{gs} - \Delta V_{th} \right) \end{cases} \tag{4-11}$$

where currents through C_{gs} and C_{ds} are neglected while i_{ds} rises.

From (4-11), voltage Δv_{gs} can be solved as a function of v_{gs}:

$$\Delta v_{gs} = f\left(v_{gs}\right) \tag{4-12}$$

Explicit analytical expression of (4-12) is not convenient to use and hard to achieve. It will be solved numerically instead by MATLAB (as shown in Appendix D).

Substituting (4-9), (4-10), and (4-12) into (4-7), switching energy mismatch can be expressed by average variables, namely

$$\Delta E_{sw} = f\left(v_{ds}, i_{ds}, v_{gs}\right) \tag{4-13}$$

The total switching energy ($E_{sw1} + E_{sw2}$) is obtained by the integration of total instantaneous power ($P_1 + P_2$), which is constructed as

$$\begin{aligned} P_1 + P_2 &= i_{ds1} v_{ds1} + i_{ds2} v_{ds2} \\ &= 2 i_{ds} v_{ds} + \frac{1}{2} \Delta i_{ds} \Delta v_{ds} \end{aligned} \tag{4-14}$$

Assume

$$i_{ds} v_{ds} >> \frac{1}{4} \Delta i_{ds} \Delta v_{ds} \tag{4-15}$$

For example, when $\Delta i_{ds} = 0.5 i_{ds}$ and $\Delta v_{ds} = 0.5 v_{ds}$ (which shows every bad sharing), $0.25 \Delta i_{ds} \Delta v_{ds}$ equals $0.063 i_{ds} v_{ds}$, which is much smaller than the product of i_{ds} and v_{ds}.

Therefore,

$$\frac{E_{sw1} + E_{sw2}}{2} \approx \int i_{ds} v_{ds} dt \tag{4-16}$$

According to (4-13) and (4-16), both switching energy difference and average switching energy are functions of v_{ds}, i_{ds}, and v_{gs}. Only averages of variables need to be solved. The comparison of typical drain-source currents/voltages (dashed lines) and their averages (solid line) during turn-on transient is shown in Fig. 4-7. The averaged waveforms are very similar to the switching transients of a single MOSFET and can be obtained by the switching of a single chip if parasitics and operating conditions are properly modified, as shown in Fig. 4-8.

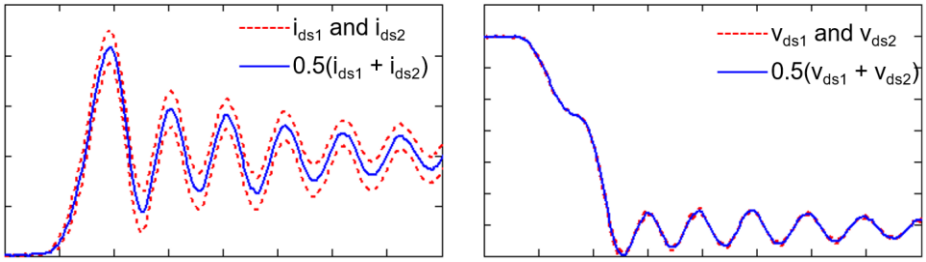


Fig. 4-7. Comparison of typical drain-source currents/voltages (dashed lines) and their averages (solid line) during turn-on transients.

The parasitics and operating conditions in Fig. 4-8 are derived as follows. The threshold voltage V_{th} in Fig. 4-8 is the average of V_{th1} and V_{th2} shown in Fig. 4-3. Common-source inductance L_{cm} is maintained, and the equivalent gate resistance is applied to achieve the same switching speed. Input current is cut by half for the switching of one chip. Diode junction capacitance is divided by 2 to achieve the same current spike. Gate inductance and power-loop inductance in Fig. 4-3 are lumped together to have the same ring frequency and voltage dropping/rising amount.

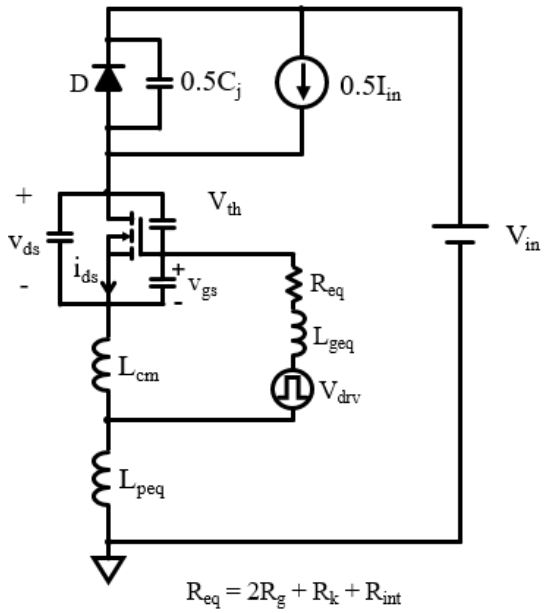


Fig. 4-8. Circuit for calculation of averages of variables in Fig. 4-3.

The capability of solving average variables by Fig. 4-8 can be demonstrated mathematically. The average of channel current i_{ds1} of M1 and channel current i_{ds2} of M2 is constructed and deduced as

$$\begin{aligned}
0.5(i_{ds1}+i_{ds2}) &= 0.5g_{fs}\left[(v_{gs1}-V_{th1})^2+(v_{gs2}-V_{th2})^2\right] \\
&= 0.5g_{fs}\left(v_{gs1}^2-2v_{gs1}V_{th1}+V_{th1}^2+v_{gs2}^2-2v_{gs2}V_{th2}+V_{th2}^2\right) \\
&= 0.5g_{fs}\left[\begin{array}{l}\dfrac{(v_{gs1}+v_{gs2})^2}{2}-(v_{gs1}+v_{gs2})(V_{th1}+V_{th2})+\dfrac{(V_{th1}+V_{th2})^2}{2} \\ +\dfrac{(v_{gs1}-v_{gs2})^2}{2}-(v_{gs1}-v_{gs2})(V_{th1}-V_{th2})+\dfrac{(V_{th1}-V_{th2})^2}{2}\end{array}\right] \\
&= g_{fs}\left(\frac{v_{gs1}+v_{gs2}}{2}-\frac{V_{th1}+V_{th2}}{2}\right)^2+g_{fs}\left(\frac{v_{gs1}-v_{gs2}}{2}-\frac{V_{th1}-V_{th2}}{2}\right)^2 \\
&= g_{fs}(v_{gs}-V_{th})^2+\frac{1}{4}g_{fs}(\Delta v_{gs}-\Delta V_{th})^2
\end{aligned} \tag{4-17}$$

where V_{th1} and V_{th2} are threshold voltages of M1 and M2, respectively. Threshold voltage V_{th} = $0.5(V_{th1} + V_{th2})$.

Because $\Delta v_{gs}\Delta V_{th} > 0$ and $\left|\Delta v_{gs}\right| < \left|\Delta V_{th}\right|$ (as demonstrated in Chapter 3),

$$\frac{1}{4} g_{fs}\left(\Delta v_{gs} - \Delta V_{th}\right)^2 \le \frac{1}{4} g_{fs}\Delta V_{th}^{\ 2} \tag{4-18}$$

In addition,

$$\frac{1}{4} g_{fs}\Delta V_{th}^{\ 2} << 0.5 I_{in} \tag{4-19}$$

For example, when I_{in} = 20 A, g_{fs} = 0.45 A/V^2, and $V_{th1} - V_{th2}$ = -0.6 V, $0.25 g_{fs}\Delta V_{th}^2$ = 0.041 A << $0.5 I_{in}$ = 10 A.

Thus,

$$i_{ds} = 0.5\left(i_{ds1} + i_{ds2}\right) \approx g_{fs}\left(v_{gs} - V_{th}\right)^2 \tag{4-20}$$

The average of i_{ds1} and i_{ds2} can be approximated by the channel current of one MOSFET with threshold voltage V_{th} = $0.5(V_{th1} + V_{th2})$. The average drain-source voltage v_{ds} and average gate-source voltage v_{gs} can also be achieved by switching of that MOSFET when power loop impedance and gate loop impedance are properly scaled.

The capability of solving average variables by Fig. 4-8 is also demonstrated by simulation. Fig. 4-9 compares the simulation results of two cases. Fig. 4-9(a) shows the average waveforms of M1 and M2 in Fig. 4-3 with V_{th1} = 2.48 V and V_{th2} = 3.08 V. Fig. 4-9(b) shows the waveforms obtained by Fig. 4-8 with V_{th} = 0.5(2.48 + 3.08) = 2.78 V. Two simulations lead to the exactly same results. The unknowns in (4-13) and (4-16) can be solve by Fig. 4-8.

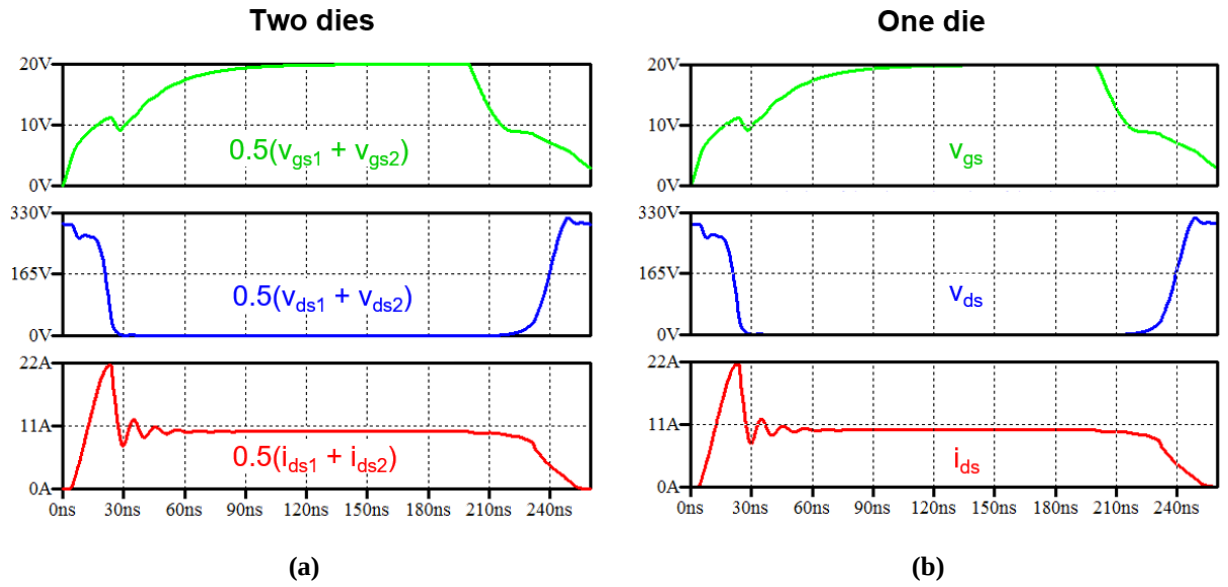


Fig. 4-9. (a) Simulation results of Fig. 4-3, and (b) simulation results of Fig. 4-8.

Modeling of a single MOSFET has been studied a lot [111]-[116] and is not the key purpose of this dissertation. The method described in [113] is employed because of the similar switching process and its excellent accuracy. The only difference is that the transfer characteristic in this dissertation is modeled by a quadratic equation with a constant transconductance instead of a linear equation with a non-linear transconductance. The details are shown in Appendix C.

4.4 Experimental Verification

Fig. 4-10 and Fig. 4-11 show the prototype of double pulse tester for experimental verification. The DUTs were two SiC MOSFETs (C2M0160120D) from Wolfspeed rated at 1200 V, 19 A, and 160 mΩ. Their threshold voltages were found to be 3.7 V and 4.8 V by measurements and modeling shown in Fig. 4-5. The freewheeling SiC diode was C4D20120A from Wolfspeed rated at 1200 V and 54.5 A. Differential voltage probe THDP0200 with enough dynamic range and bandwidth was employed to measure v_{ds}. Two TCP0030A current probes were utilized to measure drain currents and two cutouts were prepared for insertion of them. Power-source current

difference Δi_s is smaller than drain-source current difference Δi_{ds} according to Fig. 2-38. Drain current difference Δi_d was measured instead to approximate Δi_{ds} between paralleled MOSFETs thanks to the negligible difference of displacement currents from C_{ds} and C_{gd}. The switching energies were calculated by the integration of instantaneous power ($i_d * v_{ds}$) during turn-on and turn-off transients. Even though drain currents were measured because channel currents cannot be directly sensed, it is important to note that the energy stored in output capacitance C_{oss} during turn-off transient will be dissipated in the channel during turn-on transient. The total switching energy E_{swj} ($E_{swj} = E_{swjon} + E_{swjoff}$, j=1, 2) won't be affected by the currents bypassed though parasitic capacitors. Openings on the power-source and drive-source traces were prepared for insertion of extra inductors or resistors, as shown in Fig. 4-10. For baseline design, 0 Ω resistors were soldered to short the openings (as shown in Fig. 4-11) in order to reveal the switching energy mismatch induced by V_{th} variation.

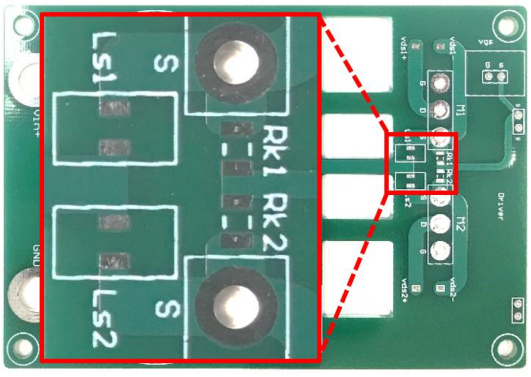


Fig. 4-10. Openings on power-source and drive-source traces for insertion of extra inductors or resistors.

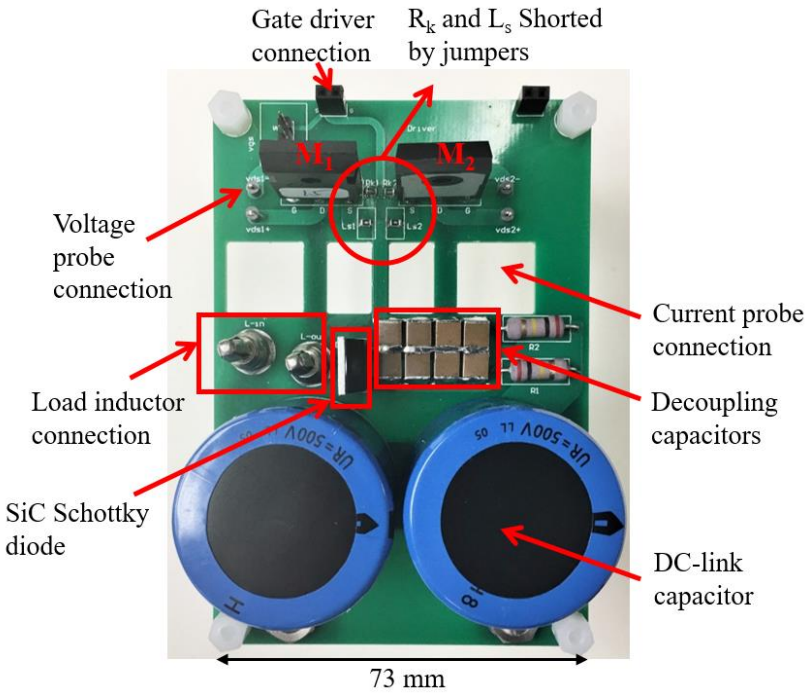


Fig. 4-11. Prototype for baseline test of current and switching energy unbalance.

To simplify the analysis, the inductances on the same trace are lumped together for the complete schematic shown in Fig. 4-3. The determination of corresponding values is illustrated in Table 4-2, where subscript "int", "pcb", and "insert" denote parameters from internal package of devices, PCB layout, and externally inserted, respectively. The devices have been modeled in Section 4.2. Inductances from the packages of MOSFET and diode are shown Table 4-1. The parasitic inductances from PCB layout are extracted by Q3D extractor as shown in Fig. 4-12. The results are listed in Table 4-3. The externally inserted component is an air-cored coupled inductor, which is employed to manipulate the passive balancing performance.

Table 4-2. Determination of parasitic inductances in Fig. 4-3.

L_p	L_d	L_{cm}	L_s	M_s	L_k	L_{kg}	L_g
$L_{p\_pcb} + L_{diode\_int}$	$L_{d\_pcb} + L_{d\_int}$	L_{s_int}	$L_s = L_{s\_pcb} + L_{s\_insert}$	M_{s_insert}	L_{k_pcb}	$L_{kg\_pcb} + L_{g\_int}$	L_{g_pcb}

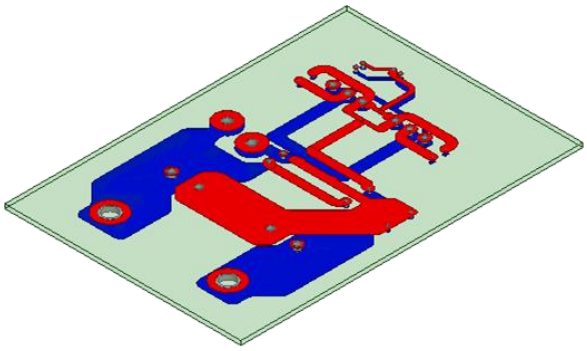


Fig. 4-12. Extraction of parasitic inductances from PCB layout by Q3D extractor.

Table 4-3. Parasitic Inductances of PCB Layout

L_{p_pcb} (nH)	L_{d_pcb} (nH)	L_{kg_pcb} (nH)	L_{g_pcb} (nH)	L_{k_pcb} (nH)	L_{s_pcb} (nH)
14.9	21.89	12.19	41.76	1.85	4.19

*L_{p_pcb} also includes the ESL of decoupling capacitor.

4.4.1 Model Verification Under Severe Unbalance

Balancing effective passive components are intentionally not added in the baseline design. The slight current balancing effect is from the inductances that exist in either layout or device package. The specific values are listed in Table 4-4. The waveforms of baseline design tested at 600 V, 20 A, and 5 Ω are shown in Fig. 3-11 and repeated in Fig. 4-13 for convenience. MOSFET M1 (which has a smaller threshold voltage) carries more current than M2 during both turn-on and turn-off switching transients. The measured peak-current difference is 3.26 A.

Table 4-4. Threshold Mismatch and Parameters Related to Current Balancing in Baseline Test

ΔV_{th} (V)	R_k (Ω)	$L_s = L_{s\_pcb}$ (nH)	M_s (nH)	$L_k = L_{k\_pcb}$ (nH)	$L_{cm} = L_{s\_int}$ (nH)
-1.1	0	4.19	0	1.85	4.1

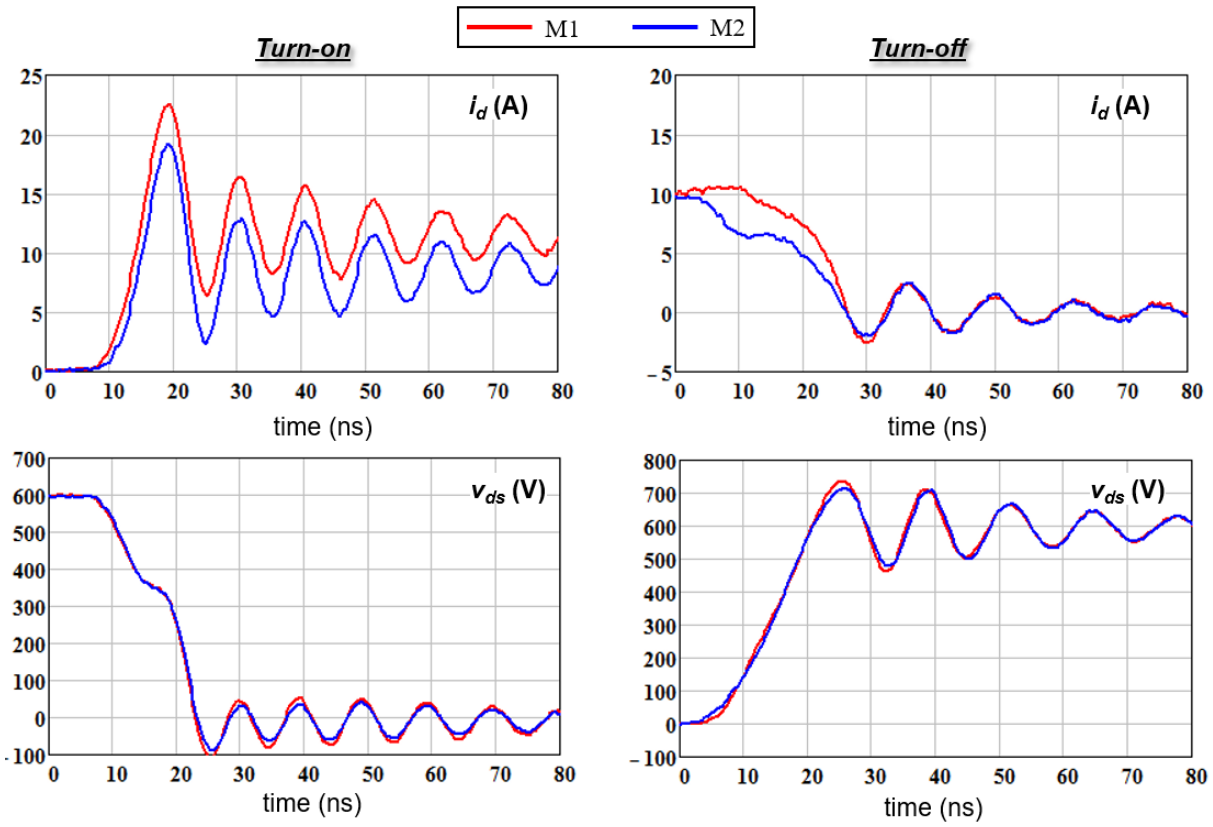


Fig. 4-13. Experimental switching transients of baseline test (with balancing parameters shown in Table 4-4). Test conditions are V_{in} = 600 V, I_{in} = 20 A, R_g = 5 Ω.

The average switching waveforms for baseline test are modeled by the circuit in Fig. 4-8 with parasitics and device parameters shown in Table 4-1-Table 4-4. Fig. 4-14 shows the comparisons between waveforms averaged from Fig. 4-13 (dashed lines) and the results calculated by the analytical model (solid lines). Good matching on slope, magnitude, and ringing frequency is achieved. Drain currents i_d (instead of channel currents i_{ch}) are compared because channel currents cannot be directly measured. Ringing in the measured v_{ds} during turn-on transient (after v_{ds} dropping to 0 V) is from the voltages on parasitic inductances inside the device package and the loading effect of voltage probes, which are much smaller than the internal v_{ds} of MOSFET when v_{ds} > 0 V because of the low equivalent frequency. The overlap loss in the channel is calculated

and compared. The ringing of v_{ds} during turn-on transient is not necessary for fair comparison, thus not intentionally modeled.

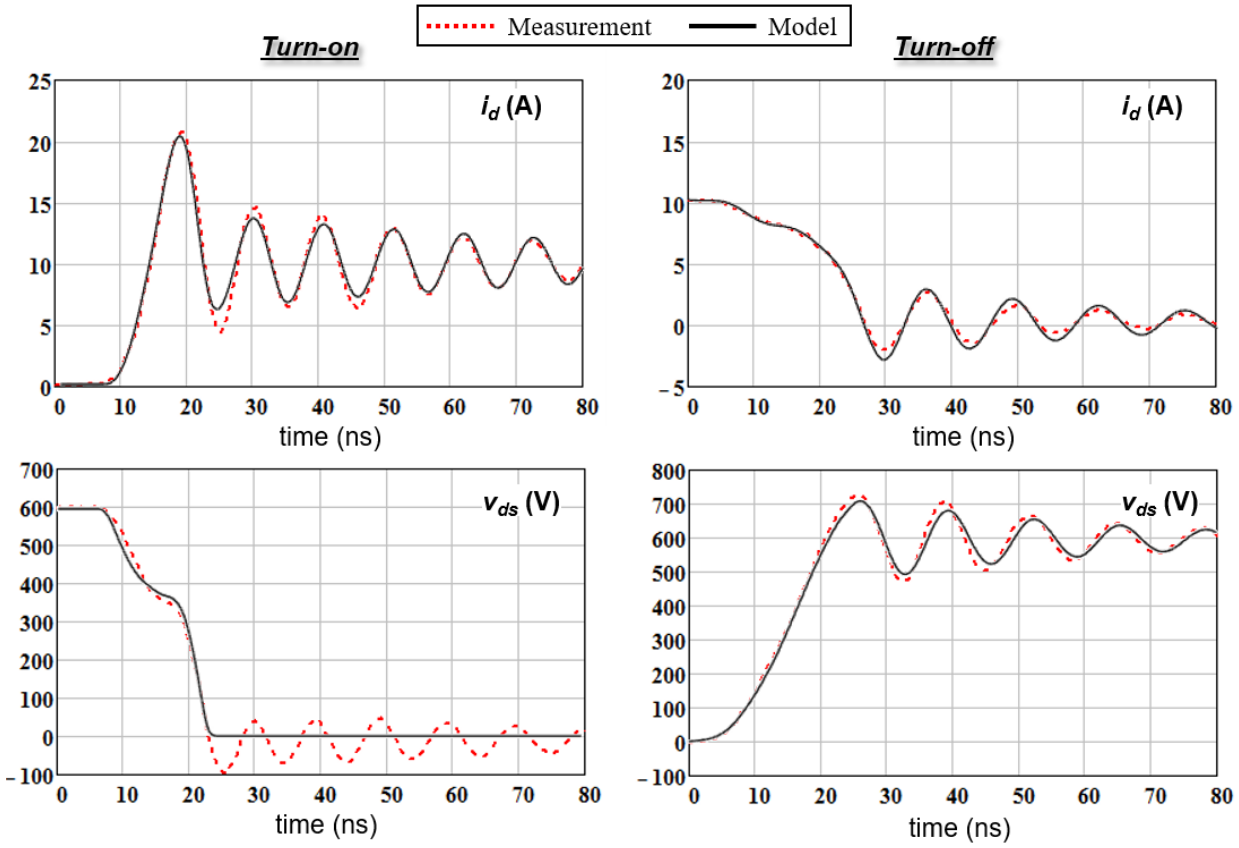


Fig. 4-14. Comparison of average waveforms obtained by model and experiment tested at V_{in} = 600 V, I_{in} = 20 A, R_g = 5 Ω (shown in Fig. 4-13).

Average switching energy E_{sw} and switching energy mismatch ΔE_{sw} are solved by applying the modeled average waveforms to (4-16) and (4-13), respectively. The channel current i_{ds} (or i_{ch}) and internal v_{ds} voltage are applied in the calculation. The overlap switching energy and switching energy difference in the channel are calculated as

$$\Delta E_{sw} = \int \Delta P dt = \int_{t(i_{ds}\ starts\ to\ rise)}^{t(v_{ds}=0)} \left(v_{ds}\Delta i_{ds} + \Delta v_{ds} i_{ds}\right) dt + \int_{t(v_{ds}\ starts\ to\ rise)}^{t(i_{ds}=0)} \left(v_{ds}\Delta i_{ds} + \Delta v_{ds} i_{ds}\right) dt \qquad (4\text{-}21)$$

$$\frac{E_{sw1} + E_{sw2}}{2} \approx \int i_{ds} v_{ds} dt = \int_{t(i_{ds}\ starts\ to\ rise)}^{t(v_{ds}=0)} i_{ds} v_{ds} dt + \int_{t(v_{ds}\ starts\ to\ rise)}^{t(i_{ds}=0)} i_{ds} v_{ds} dt \qquad (4\text{-}22)$$

The details are shown in Appendix D.

Drain currents and terminal drain-source voltages are employed in the calculation of switching losses of test results. The energy stored in output capacitance C_{oss} during turn-off transient will be dissipated in the channel during turn-on transient. The terminal v_{ds} measured by differential probe is approximately equal to the internal v_{ds}, because the voltages on parasitic inductances inside the device package and the loading effect of voltage probes are much smaller than the internal v_{ds} of MOSFET when $v_{ds} > 0$ V. Thus, The average of total switching energy $0.5(E_{sw1} + E_{sw2})$ and switching energy difference $(E_{sw1} - E_{sw2})$ (where $E_{swj} = E_{swjon} + E_{swjoff}$, j=1, 2) won't be affected and can be fairly modeled by (4-22) and (4-21).

Comparisons of tested (lines) and modeled (dots) average E_{sw} and ΔE_{sw} under variant operating conditions are illustrated in Fig. 4-15. The good agreement further validates the accuracy of the analytical model for paralleled MOSFETs. According to Fig. 4-15, average E_{sw} and ΔE_{sw} increase with input current I_{in} and external gate resistance R_g. The switching energy mismatch percentage is as high as 44% and increases with reducing I_{in}. Even though ΔI_{pk} are kept almost the same under different switching speed (as shown in Fig. 3-12), the current and/or voltage rise and/or fall slower with larger R_g resulting in a higher switching energy mismatch.

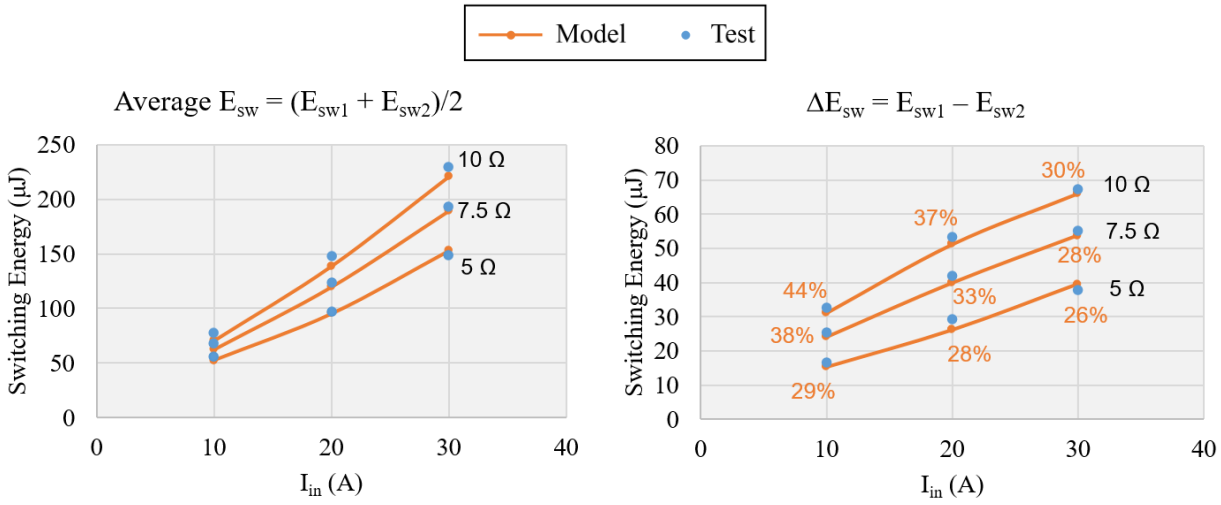


Fig. 4-15. Comparison of tested and modeled (a) average E_{sw} and (b) ΔE_{sw} (with mismatch percentage listed) under variant operating conditions for base line design. Parameters influencing current unbalance are in Table 4-4.

4.4.2 Model Verification Under Slight Unbalance

As peak-current mismatch and switching energy mismatch vary with operating conditions, a worst-case design that is valid for wide operating range would be preferred. The design procedure and prototype of passive balancing components are shown in Section 3.3.2. The specific values are listed in Table 4-5. The waveforms of current balancing design tested at 600 V, 20 A, and 5 Ω are shown in Fig. 3-17 and repeated in Fig. 4-13 for convenience. The measured difference of peak currents is reduced from 3.26 A to 0.1 A. The desired current sharing ($|\Delta i_{ds(pk)}| < 0.5$ A) is obtained by a single gate driver from the first switching cycle. Much better sharing is also achieved for turn-off transient compared to the baseline shown in Fig. 4-13.

Table 4-5. Threshold voltage mismatch and current balancing parameters in the tests of worst case design

ΔV_{th} (V)	R_k (Ω)	$L_s = L_1 + L_{s\_pcb}$ (nH)	M_s (nH)	$L_k = L_{k\_pcb}$ (nH)	$L_{cm} = L_{s\_int}$ (nH)
-1.1	4	40.3	29.9	1.85	4.1

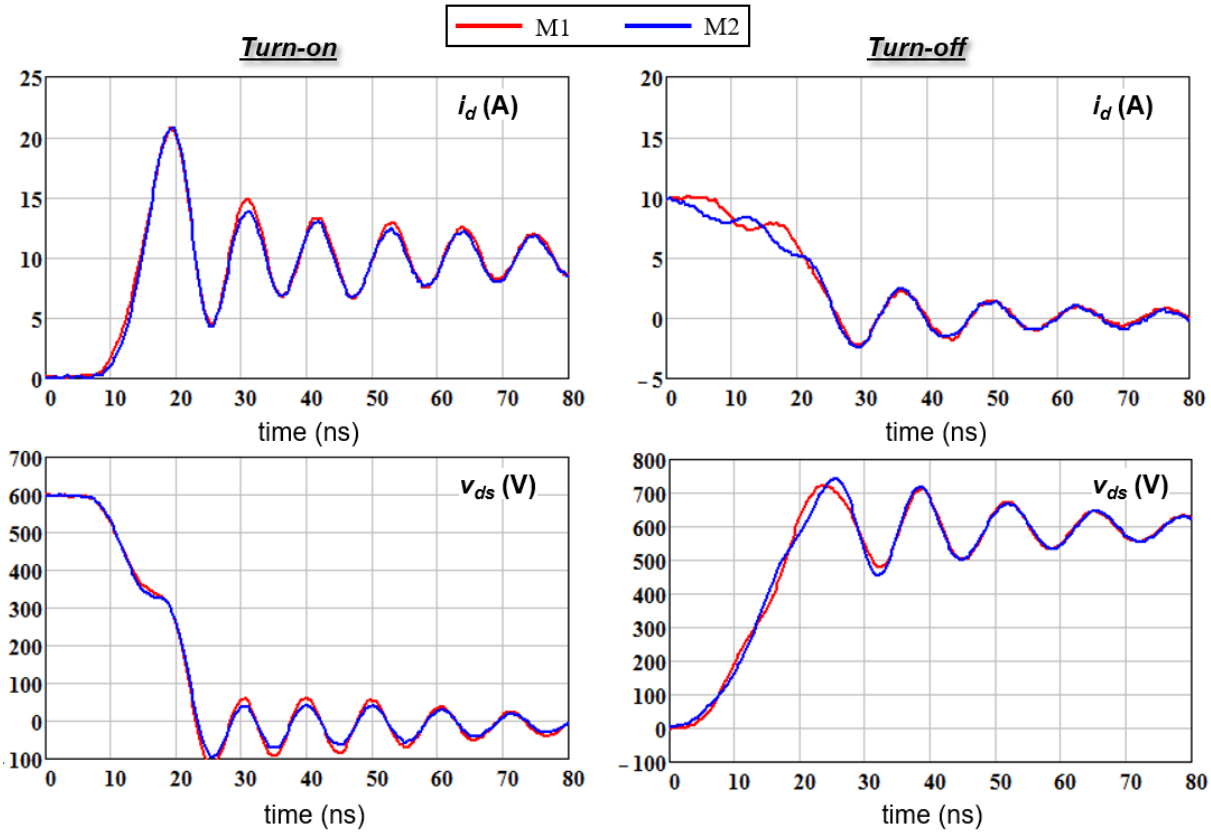


Fig. 4-16. Experimental switching transients of worst case balancing solution (with balancing parameters shown in Table 4-5). Test conditions are V_{in} = 600 V, I_{in} = 20 A, R_g = 5 Ω.

Comparisons between waveforms averaged from Fig. 4-16 (dashed lines) and the results calculated by analytical model (solid lines) are shown in Fig. 4-17. The average switching waveforms are modeled by Fig. 4-8 with parasitics and device parameters shown in Table 4-1- Table 4-3, and Table 4-5. Good matching on slope, magnitude, and ringing frequency is achieved. The ringing of v_{ds} during turn-on transient is not necessary for fair comparison, thus not intentionally modeled.

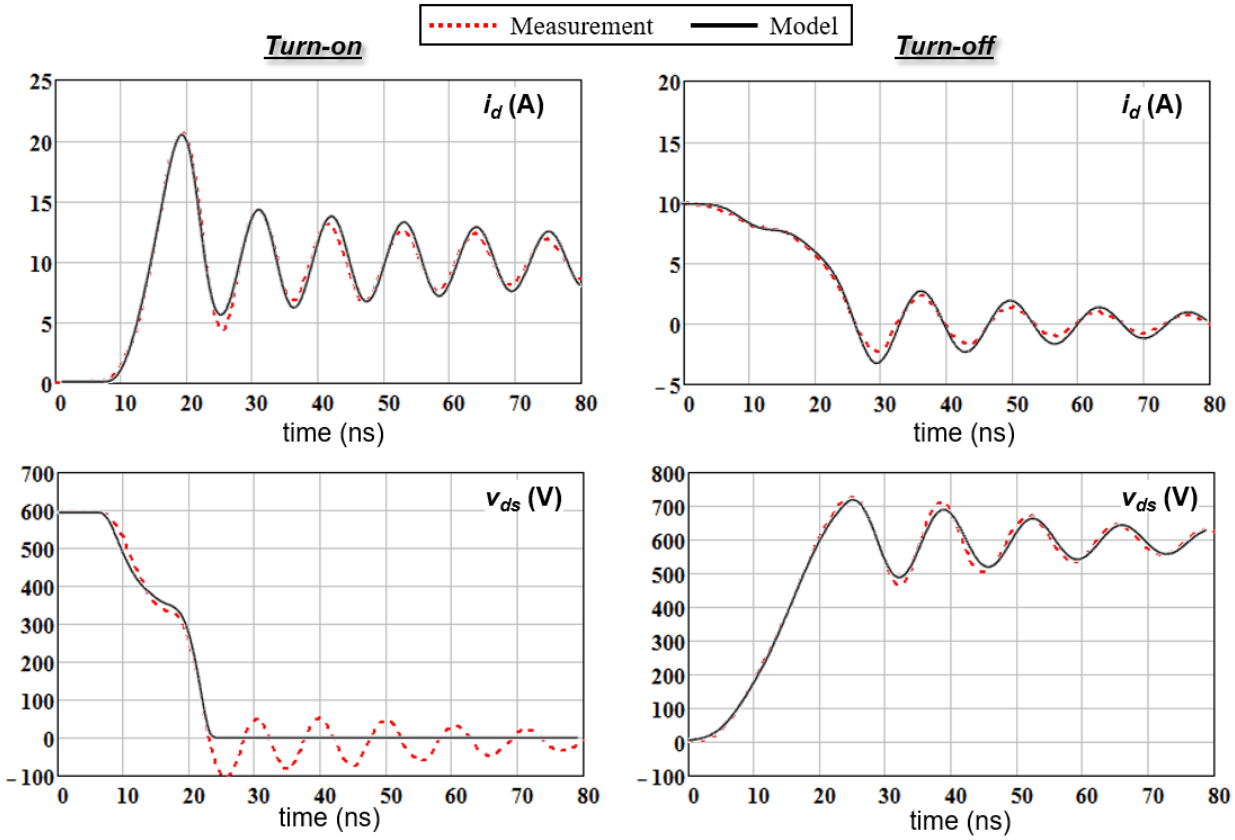
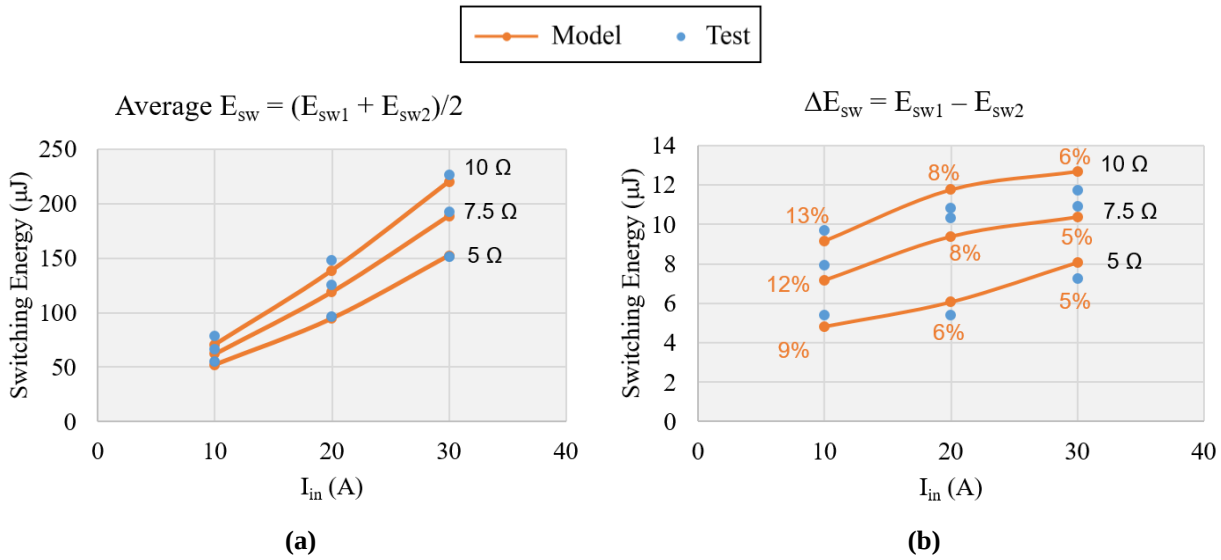


Fig. 4-17. Comparison of average waveforms obtained by model and experiment tested at V_{in} = 600 V, I_{in} = 20 A, R_g = 5 Ω (shown in Fig. 4-16).

Average switching energy E_{sw} and switching energy mismatch ΔE_{sw} under slight unbalance are solved by applying the modeled average waveforms to (4-16) and (4-13), respectively. The channel current i_{ds} (or i_{ch}) and internal v_{ds} voltage are utilized in the calculation. The overlap switching energy and switching energy difference in the channel are calculated as (4-22) and (4-21). The details are shown in Appendix D.

Drain currents and terminal drain-source voltages are employed for the calculation of switching losses of test results. The average of total switching energy $0.5(E_{sw1} + E_{sw2})$ and switching energy difference $(E_{sw1} - E_{sw2})$ (where $E_{swj} = E_{swjon} + E_{swjoff}$, j=1, 2) won't be affected and can be fairly modeled by (4-22) and (4-21).

Comparisons of tested (lines) and modeled (dots) average E_{sw} and ΔE_{sw} under variant operating conditions are illustrated in Fig. 4-18. The capability of balancing switching energies by passive method is accurately modeled. Switching energy mismatch percentage can be reduced by 5 times compared to Fig. 4-15.



(a) **(b)**

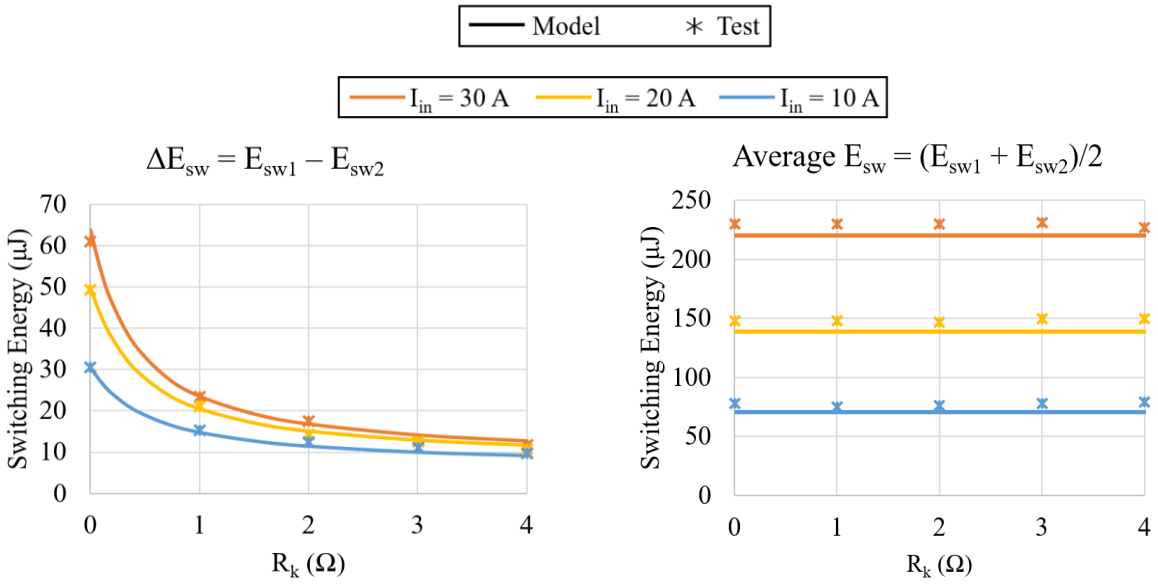
Fig. 4-18. Comparison of tested and modeled (a) average E_{sw} and (b) ΔE_{sw} (with mismatch percentage listed) under variant operating conditions for balanced design. Parameters influencing current sharing are in Table 4-5.

4.5 Discussions

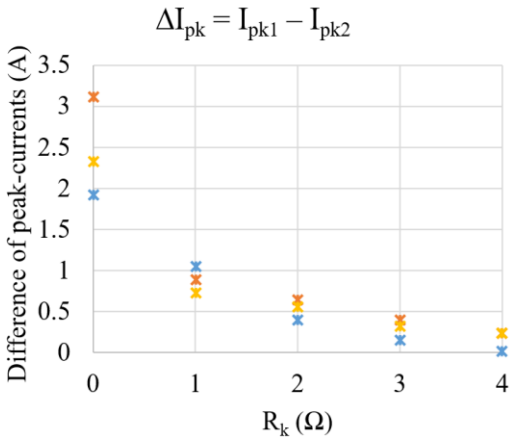
4.5.1 Influence of R_k and Coupled L_s on Balancing Effect

The drive-source resistance R_k and effective power-source inductance (L_s + M_s) were swept to investigate their respective influences on balancing and to demonstrate the accuracy of the analytical model over wide range.

Fig. 4-19 shows the comparison of switching energy differences, average switching energies, and peak-current differences between tested (star) and modeled (line) results under V_{in} = 600 V, $R_g + 0.5R_k = 10\ \Omega$, and I_{in} = 10A/20A/30A. The value of R_k was swept from 0 Ω to 4 Ω while keeping coupled L_s the same as the worst-case design in Table 4-5. When R_k = 0 Ω, the balancing effect of drive-source trace is provided by the drive-source inductance L_k = 1.85 nH, which is the first term in (3-19). The effective current balancing inductance from drive-source and power-source traces is $L_k//(L_s + M_s)$. The influence of $L_s + M_s$ = 70.2 nH is almost bypassed by the small L_k. The main balancing effect is offered by L_{cm} = 4.1 nH. With increased R_k, the current mismatch between drive-source traces is mitigated. The peak-current mismatch and switching energy mismatch gradually is reduced while keeping average switching energy constant. Good accuracy between model and experiment was achieved.



(a) **(b)**



(c)

Fig. 4-19. Influence of R_k on (a) switching energy difference, (b) average switching energy, and (c) peak-current difference based on modeled (line) and tested (star) results under V_{in} = 600V, R_g + 0.5 R_k =10 Ω, and changing I_{in}. The coupled power-source inductors are kept the same as the worst-case design shown in Table 4-5.

Mismatches of switching energies under different switching speeds are predicted by analytical model and shown in Fig. 4-20. A similar trend as Fig. 4-19(a) is observed. The only difference is the magnitude of ΔE_{sw}. The faster the switching speed, the smaller the switching energy mismatch will be, as demonstrated in Fig. 4-15(b) and Fig. 4-18(b). Even though the inserted coupled L_s is able to limit the current difference of power-source traces, a certain R_k is still required to reduce the current mismatch of drive-source traces. Otherwise, the difference of drain-source currents will bypass the coupled L_s and circulate from channels to drive sources.

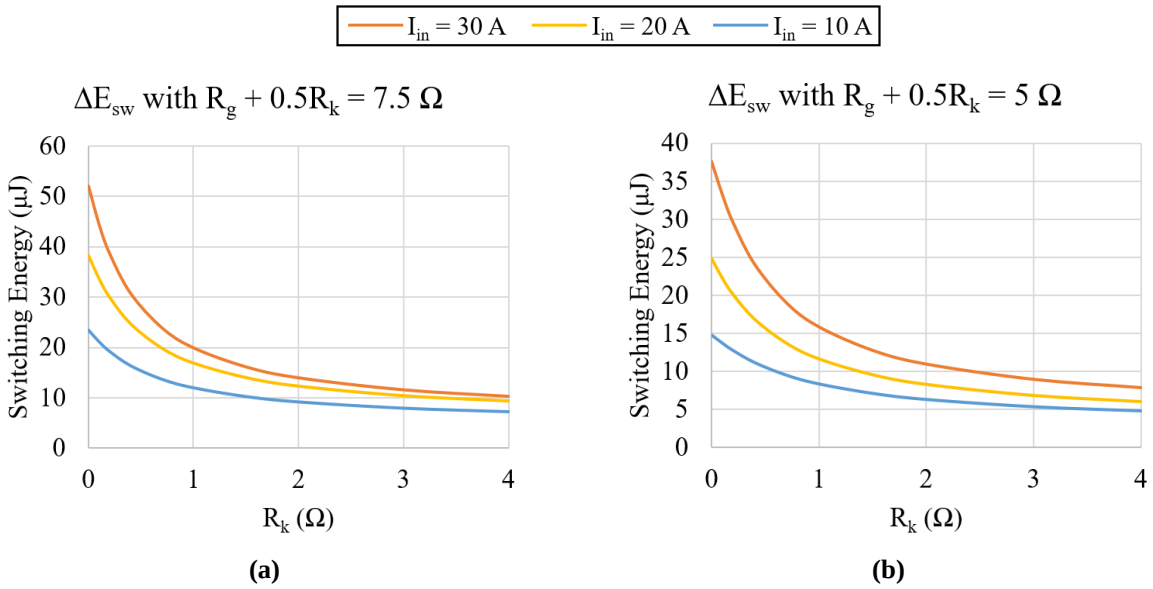


Fig. 4-20. Influence of R_k on transient balancing under different operating conditions based on modeling results. The coupled power-source inductors are kept the same as the worst case design shown in Table 4-5. (a) V_{in} = 600 V, R_g + 0.5 R_k = 7.5 Ω, and changing I_{in}; (b) V_{in} = 600 V, R_g + 0.5 R_k = 5 Ω, and changing I_{in}.

Fig. 4-22 shows the comparison of switching energy differences, average switching energies, and peak-current differences between tested (star) and modeled (line) results. The value of (L_s + M_s) is varied by changing the number of turns. The manufactured air-cored coupled inductors are shown in Fig. 4-21. Resistance R_k is kept the same as the worst-case design shown in Table 4-5. The operating conditions are V_{in} = 600 V, R_g + 0.5R_k = 10 Ω, and I_{in} = 10A/20A/30A. When N = 0 (openings on power-source traces are shorted by jumpers), the on-board (L_s + M_s) is only 4.19 nH. The second term in (3-21) dominates the max|$\Delta i_{ds(pk)}$|. Most of the channel current mismatch flows through power-source traces and the 4 Ω R_k is almost bypassed. The current mismatch between power-source traces can be mitigated by increased (L_s + M_s). Peak-current mismatch and switching energy mismatch gradually reduce while keeping average switching energy constant. Good accuracy between model and experiment was achieved.

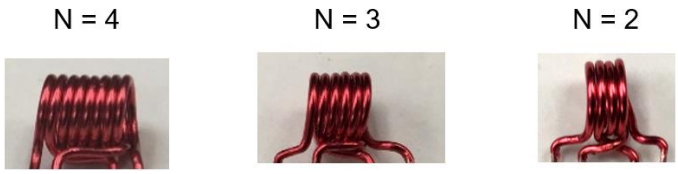


Fig. 4-21. Manufactured air-cored coupled inductors with different number of turns.

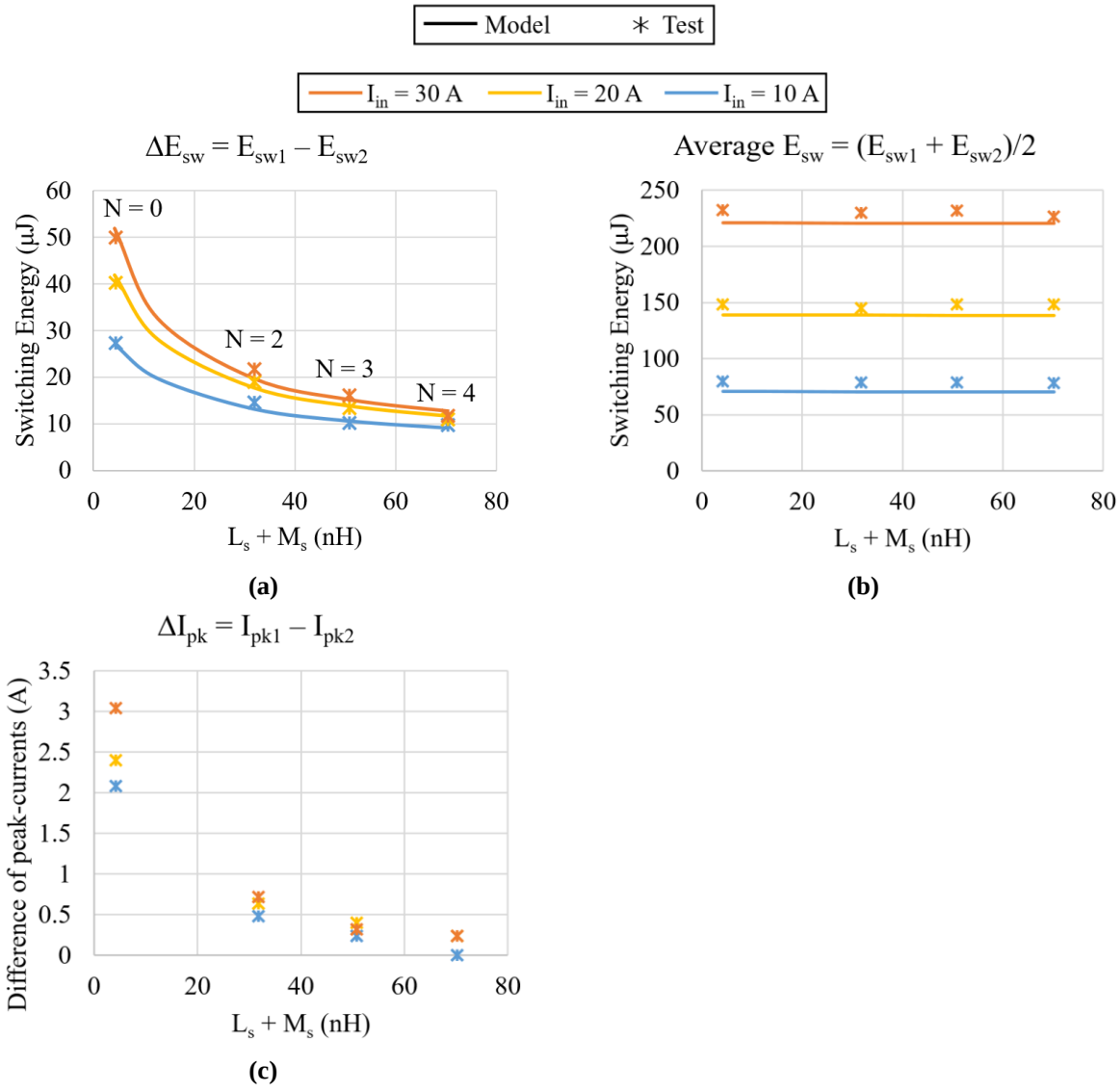


Fig. 4-22. Influence of coupled power-source inductors on (a) switching energy difference, (b) average switching energy, and (c) peak-current difference based on modeled (line) and tested (star) results under V_{in} = 600V, $R_g + 0.5\ R_k$ =10 Ω, and changing I_{in}. Resistance R_k is kept the same as the worst-case design in Table 4-5.

Switching energy mismatches with varying (L_s + M_s) under different switching speeds are obtained by analytical model and shown in Fig. 4-23. A aimilar trend as Fig. 4-22 is observed. The only difference is the magnitude of ΔE_{sw}. Even though the inserted R_k = 4 Ω is able to limit the current difference of drive-source traces, a certain (L_s + M_s) is still required to reduce the current mismatch of power-source traces. Otherwise, R_k will be partially bypassed in differential point of view and the induced ΔV_{gs} will not be large enough to compensate ΔV_{th}. According to Fig. 4-19 - Fig. 4-23, neither R_k nor coupled L_s can be ignored.

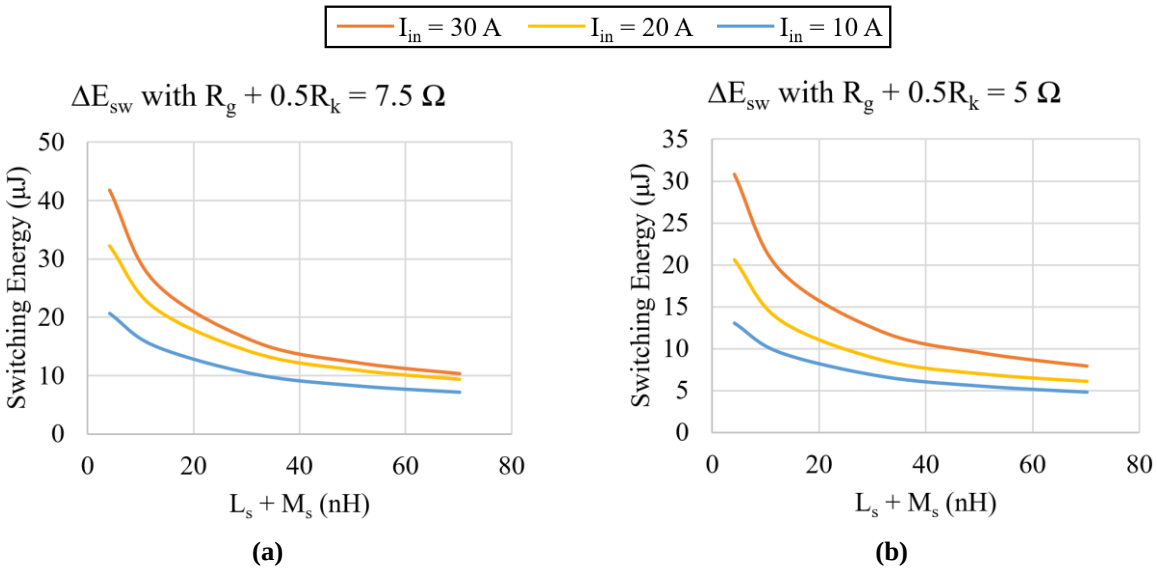


Fig. 4-23. Influence of coupled power-source inductors on transient balancing under different operating conditions based on modeling results. Resistance R_k is kept the same as the worst-case design in Table 4-5. (a) V_{in} = 600 V, R_g + 0.5 R_k = 7.5 Ω, and changing I_{in}; (b) V_{in} = 600 V, R_g + 0.5 R_k = 5 Ω, and changing I_{in}.

4.5.2 Influence of L_{cm} and ΔV_{th} on Sharing during Switching Transients

In the previous experiments, SiC MOSFETs in TO-247-3 package were tested. Common-source inductance from the bond wire inside MOSFET package is around 4.1 nH (as shown in Table 4-1). This inductance can be avoided if 4 terminal packaging is applied to discrete MOSFETs or if bare dies are paralleled inside the power module. Common-source inductance is shared by

gate loop and power loop. It will reduce switching speed and increase switching energy for both turn-on and turn-off transients. Inductance L_{cm} is preferred to be as small as possible to achieve better switching performance, however this will cause more severe unbalance according to (3-40) and Fig. 3-6. Comparisons of average switching energy and switching energy mismatch between with (solid lines) and without L_{cm} (dashed lines) are shown in Fig. 4-24. The results are obtained by analytical model described in Section 4.3. Layout parasitics and balancing parameters are the same as the baseline test, as shown in Table 4-1-Table 4-4. Input current and gate resistance are varying to cover a wide operating range. When L_{cm} = 0 nH, average switching energy is smaller, but switching energy mismatch is larger. Switching energy mismatch percentages are calculated based Fig. 4-24 and are shown in Fig. 4-25. Elimination of L_{cm} results in more than 10% increase of mismatch percentage for all the operating conditions. Implementation of passive balancing solution will be more crucial if L_{cm} is removed by Kelvin connection.

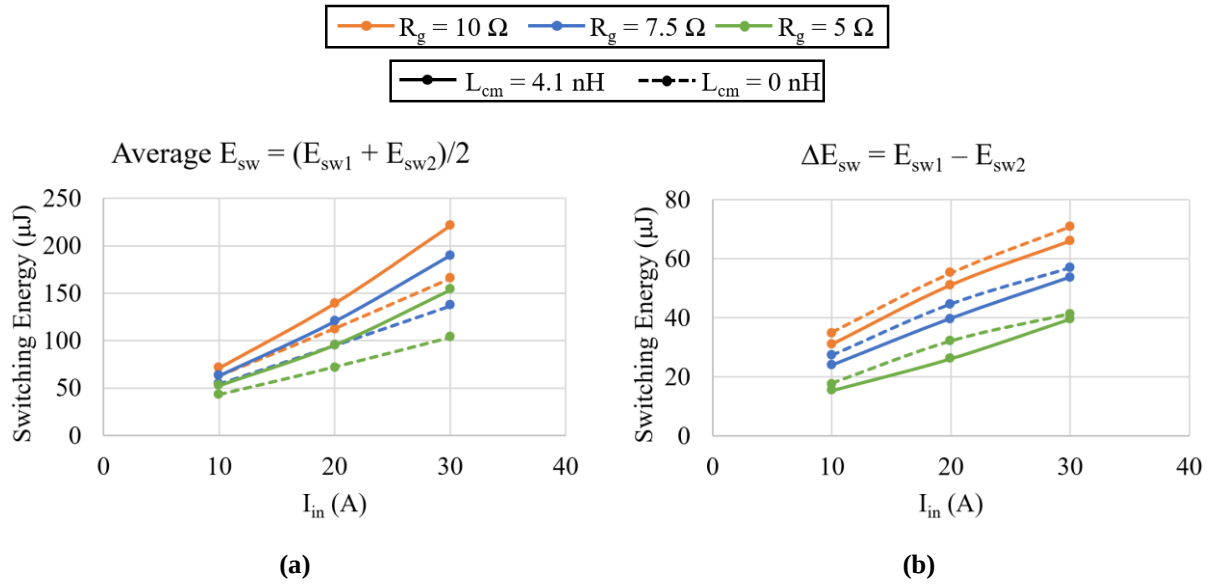


Fig. 4-24. Comparison of (a) average switching energy and (b) switching energy mismatch between with (solid line) and without (dashed line) L_{cm} under varying operating conditions.

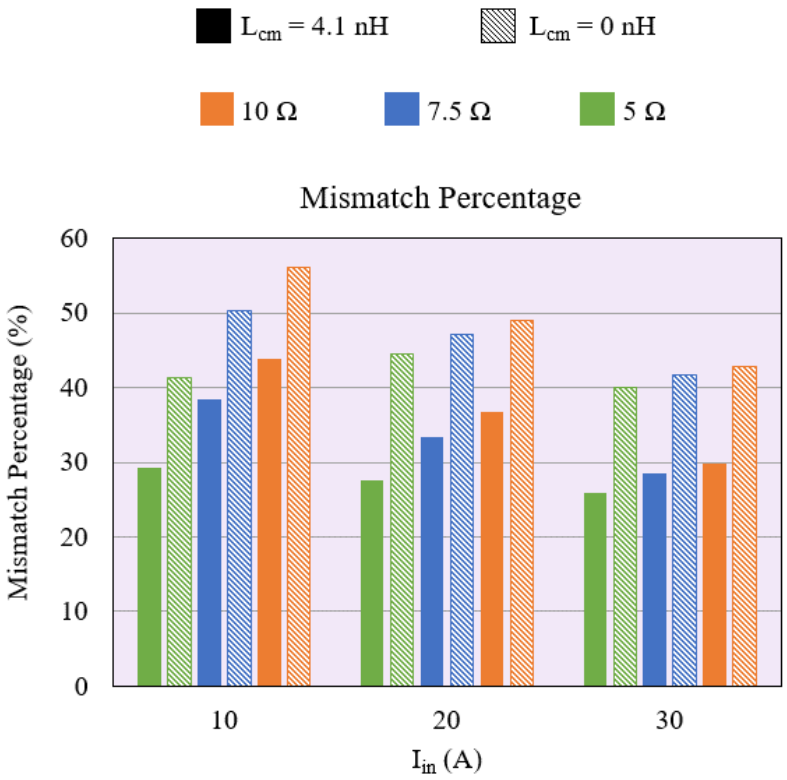


Fig. 4-25. Comparison of switching energy mismatch percentage with (solid pattern) and without (dashed pattern) L_{cm} under varying operating conditions.

Average switching energies, switching energy differences, and switching energy mismatch percentages with varying threshold voltage mismatch ΔV_{th} are obtained by analytical model and plotted in Fig. 4-26. The solid and dashed lines show the results when L_{cm} = 4.1 nH and L_{cm} = 0 nH, respectively. The operating conditions are V_{in} = 600V, I_{in} = 10 A, and R_g =10 Ω. According to Fig. 4-26, mismatch in V_{th} will not change the average switching energy, but deviate the switching energy of one MOSFET from the other in parallel. Switching energy difference is almost proportional to $|\Delta V_{th}|$. For L_{cm} = 4.1 nH, switching energy mismatch percentage is around 40% when ΔV_{th} = 1 V and is increased to around 70% when ΔV_{th} = 2 V. This tendency is more severe for L_{cm} = 0 nH, as shown in Fig. 4-26(c). Switching energy mismatch percentage is increased by 10% when ΔV_{th} = 1 V and is increase by 20% when ΔV_{th} = 2 V if L_{cm} is eliminated. Thus, passive

balancing solution is necessary if variation in threshold voltage exists, especially when Kelvin connection is applied.

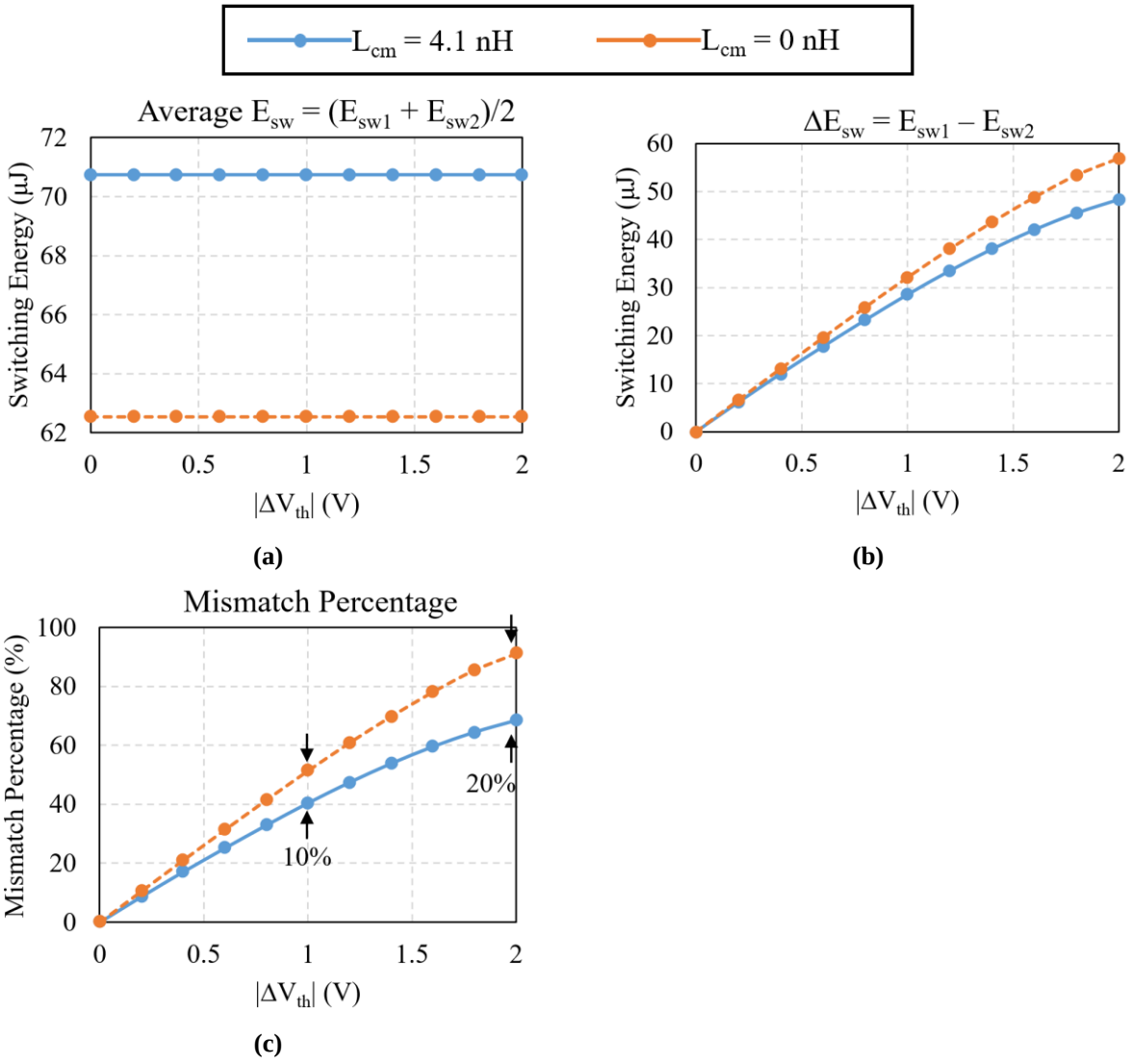


Fig. 4-26. Influence of threshold mismatch on (a) average switching energy, (b) switching energy mismatch, and (c) switching energy mismatch percentage based on modeled results with L_{cm} = 4.1 nH (solid lines) and L_{cm} = 0 nH (dashed lines). Operating conditions are V_{in} = 600V, I_{in} = 10 A, and R_g =10 Ω. The balancing parameters are L_{cm} = 4.1 nH, L_k = 1.85 nH, L_s = 4.19 nH, M_s = 0 nH, and R_k = 0 Ω.

4.6 Conclusion

The switching energy mismatch and switching energy mismatch percentage caused by V_{th} variation are modeled in this chapter. Switching energy mismatch ΔE_{sw} is not equal or proportional to peak-current mismatch $\Delta i_{ds(pk)}$ even though both can be reduced by passive balancing method. The influence of operating conditions, passive balancing components, layout and package parasitic inductances, nonlinear channel performance, and voltage dependent parasitic capacitors are included in the modeling process. The more parasitics considered, the more accurate the model will be, however, at the expense of more complex mathematics. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs. The accuracy of the derived model is experimentally verified under variant operating conditions and passive balancing designs. The average E_{sw} and ΔE_{sw} increase with input current I_{in} and external gate resistance R_g. The switching energy mismatch percentage is as high as 44%. The capability of balancing switching energies by passive method is accurately modeled. Switching energy mismatch percentage can be reduced by 5 times. The influence of L_{cm} and ΔV_{th} are also discussed based on modeling results. The mismatch in V_{th} will not change the average switching energy, but deviate the switching energy of one MOSFET from the other in parallel. Switching energy difference is almost proportional to $|\Delta V_{th}|$. This tendency is more severe if L_{cm} is eliminated. Passive balancing solution is necessary if variation in threshold voltage exists, especially when Kelvin connection is applied. The derived model also can be extended to the case of more than two MOSFETs in parallel (as shown in Appendix B).

Chapter 5 Conclusions and Future Work

5.1 Summary of Work

Passive balancing solutions are investigated to balance the peak currents between paralleled MOSFETs caused by unequal threshold voltages. Design guidelines involving the magnitude of V_{th} mismatch, current rise time, and maximum peak-current difference are derived to guide the choice of passive components. The detailed design procedures are recommended to force currents to share over wide operating range. Current/voltage sensors, feedback loop, multiple gate drivers, and the knowledge of the polarity of V_{th} difference are not required. The difference of peak currents can be limited to a predetermined percentage automatically by inductances and/resistances without sacrificing the total switching loss. The aforementioned benefits were demonstrated by two paralleled SiC MOSFETs (C2M0160120D) tested at variant operating conditions. The difference of peak currents can be reduced below 5% of steady-state current in every switching transient.

Several passive balancing structures are analyzed and compared. All of them can provide much better current and power balancing without increasing switching loss. Some of the them induce more voltage stress due to the increased stress-inducing inductance, which can be reduced by negative magnetic coupling. Perfect coupling between power-source inductors would enable current matching without penalty on voltage stress. Common-source inductance L_{cm} is not considered in power module application because it is negligible with Kelvin connection. However, the wire bond inside the package of discrete MOSFETs and part of the external leads are inevitable and add to L_{cm}. Common-source inductance is effective in dynamic balancing, but at the expense of higher switching loss. Design guidelines and procedures for cases with and without L_{cm} are provided and experimentally verified over wide operating range.

The switching energy mismatch and switching energy mismatch percentage caused by V_{th} variation are modeled. Switching energy mismatch ΔE_{sw} is not equal or proportional to peak-current mismatch $\Delta i_{ds(pk)}$ even though both of them can be reduced by passive balancing method. The influence of operating conditions, passive balancing components, layout and package parasitic inductances, nonlinear channel performance, and voltage dependent parasitic capacitors are included in the modeling process. The more parasitics considered, the more accurate the model will be, though it would be at the expense of more complex mathematics. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs. The accuracy of the derived model is experimentally verified under variant operating conditions and passive balancing designs. The average E_{sw} and ΔE_{sw} increase with input current I_{in} and external gate resistance R_g. The switching energy mismatch percentage is as high as 44%. The capability of balancing switching energies by passive method is accurately modeled. Switching energy mismatch percentage can be reduced by 6 times. The influence of L_{cm} and ΔV_{th} are also discussed based on modeling results. The mismatch in V_{th} will not change the average switching energy, but deviate the switching energy of one MOSFET from the other in parallel. Switching energy difference is almost proportional to $|\Delta V_{th}|$. This tendency is more severe if L_{cm} is eliminated. Passive balancing solution is necessary if variation in threshold voltage exists, especially when Kelvin connection is applied.

5.2 Future Work

The passive balancing solutions can be extended to the case of more than two MOSFETs in parallel because they don't need to consider the asymmetry of V_{th} and use one gate driver. In practical realization, e.g., module fabrication, the $|\Delta V_{th}|$ can be replaced by the largest mismatch from datasheet, and t_r can be approximated by simulation and/or datasheet for the worst-case

design. Preliminary mathematic analysis and simulation demonstration for three MOSFETs in parallel are provided in Appendix B. Experimental verification for paralleling of bare dice inside a power module and paralleling of discrete MOSFETs can be the future work.

The ΔV_{th} may vary under continuous testing due to the different junction temperatures between MOSFETs and the negative temperature coefficient of V_{th}. The worst ΔV_{th} can be approximated by the temperature coefficient of V_{th} in the datasheet. For example, if the largest difference of temperatures allowed is 25^{o}C, the ΔV_{th} of SiC MOSFETs C2M0160120D will increase around 0.25 V. The R_k, L_s, L_k, M_k, or M_s can be calculated by design guidelines with the updated worst ΔV_{th}. This dissertation does not cover the case of different junction temperatures, though further investigation could be given to that topic in future work.

The realization of coupled inductors with magnetic core can also be studied to further reduce the size and to manage the magnetic field when the calculated inductance is too large to be effectively realized by air-cored inductor. Very-high-frequency magnetic materials reported in [95],[96] can provide a permeability of 50 or above at tens of MHz and could be used to fabricate the inductor with magnetic core for current balancing. As only current difference is flowing through the negatively-coupled inductors, the size and loss of magnetic core are expected to be limited when the balancing solution is implemented.

Appendix A Numerical Model of t_r

This section derives current rise time t_r defined in Fig. 2-8. Because current rise time is related to parasitic inductances, devices under test, and operating conditions, the mathematics to achieve an analytical solution of t_r will be very complex. The final result either cannot be obtained or is too complex to be meaningful. Thus, a numerical method is employed in this section to derive the influence of parasitic inductances (listed in

This dissertation also models the switching energy and switching energy mismatch of paralleled MOSFETs. The resulting high order system is simplified by reducing the number of passive components and number of MOSFETs. The accuracy of the proposed model is experimentally verified over wide operating range. The influence of current balancing components and magnitude of threshold voltage mismatch on sharing are discussed based on modeling results.

Table 1-2) and operating conditions on t_r. The MOSFET under test is C2M0160120D from Wolfspeed. The simulation schematic is shown in Fig. A-1. The main purpose of this numerical model is to reveal the trend and significance of the impact of parasitic inductances and operating conditions on t_r, which can be referred to when applying passive balancing solutions. Similar procedures can be employed to derive the numerical model for other MOSFETs.

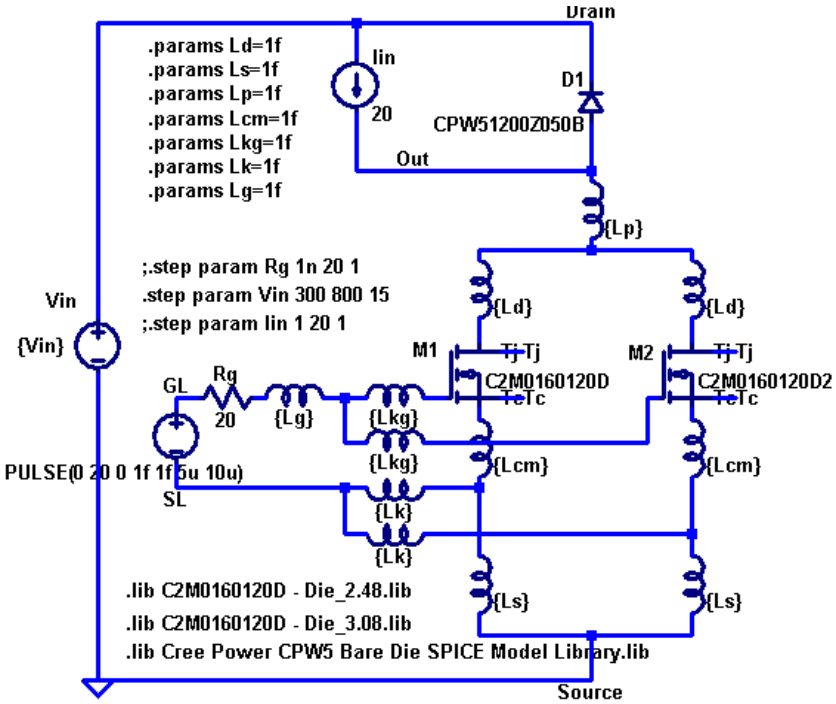


Fig. A-1. Schematic built in LTspice to simulate the influence of operating conditions and parasitic inductances on current rise time t_r.

The schematic in Fig. A-1 includes all the parasitic inductances that may exist in the circuit. The low side is composed of two MOSFETs in parallel. The threshold voltages of M1 and M2 are 2.48 V and 3.08 V, respectively. The values of parasitic inductances and operating conditions (including V_{in}, I_{in}, and R_g) can be swept. The corresponding current rise time will be recorded to achieve their influence.

Firstly, the numerical model of t_r as a function of operating conditions is derived. Parasitic inductances are not considered for now for simplicity. The change of current rise time with the variation of V_{in}, I_{in}, or R_g is shown in Fig. A-2 , where all the inductances are set as 0 nH. The corresponding current rise time is name as t_{r_die}, i.e., for bare die case. According to Fig. A-2, t_{r_die} increases linearly with I_{in} and R_g, and decreases linearly with V_{in}. The influences of I_{in} and R_g are more significant than V_{in}.

Since t_{r_die} is linearly dependent on operating conditions, it can be modeled by (A-1), where all the interactions among V_{in}, I_{in}, and R_g are considered.

$$t_{r\_die} = d_1 I_{in} + d_2 R_g + d_3 V_{in} + d_4 I_{in} R_g + d_5 I_{in} V_{in} + d_6 R_g V_{in} + d_7 I_{in} R_g V_{in} + d_8 \quad \text{(A-1)}$$

Because only three variables are included, and the relationship is simple, the statistic software JMP is utilized to solve the unknown coefficient d_1 to d_8. Twelve experiments are selected and designed by JMP to achieve the model, as shown in Fig. A-3. The calculated coefficients are listed in Table A-1.

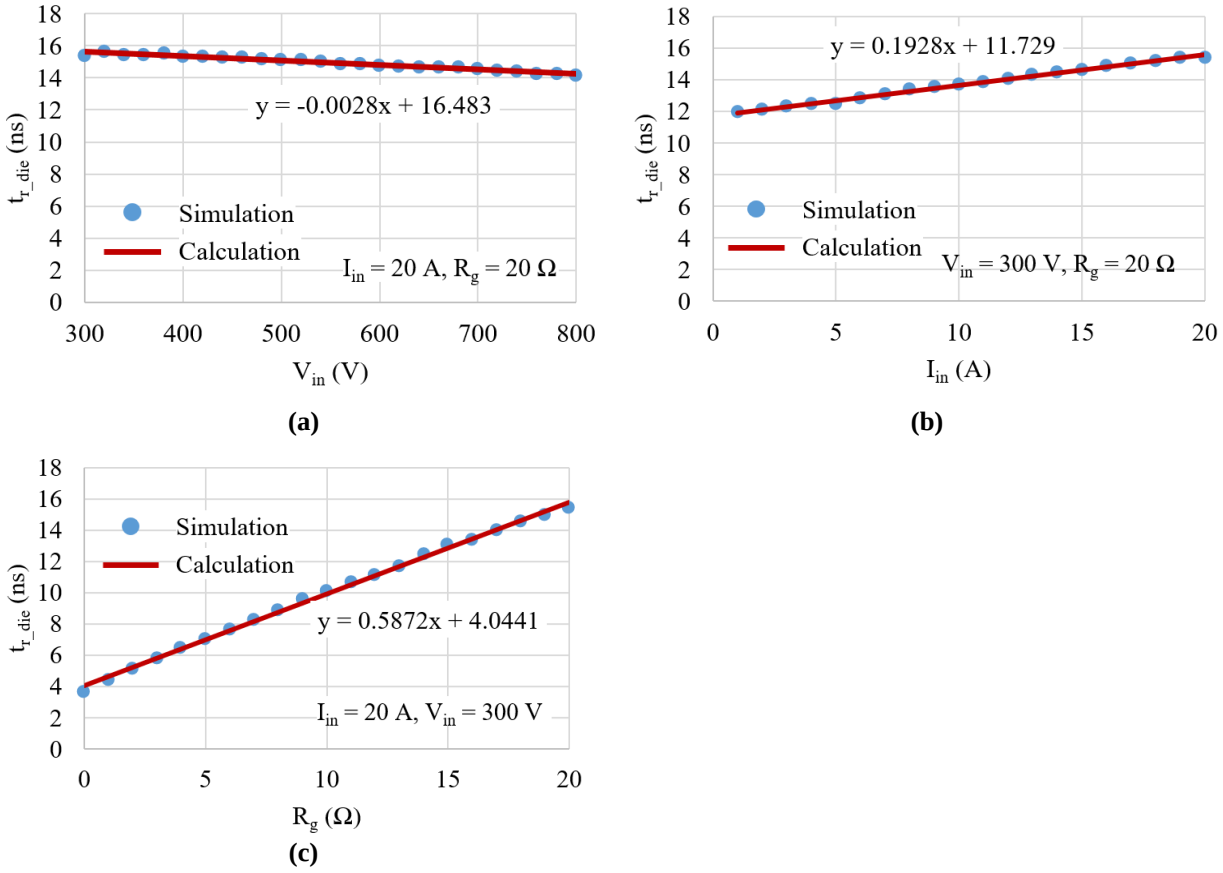


Fig. A-2. Simulation results of Fig. A-1 with all the inductances set as 0 nH. (a) Influence of V_{in} on t_r; (b) influence of I_{in} on t_r; (c) influence of R_g on t_r, where dots show simulation results and lines show the calculated results from linear functions.

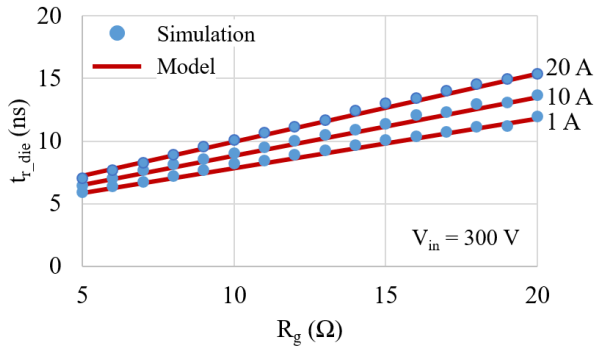
	Iin	Rg	Vin	tr
1	5	5	300	6.12424
2	5	5	800	5.94922
3	5	5	800	5.94922
4	5	20	300	12.53721
5	5	20	300	12.53721
6	5	20	800	12.16532
7	20	5	300	7.2107
8	20	5	300	7.2107
9	20	5	800	6.58918
10	20	20	300	15.39604
11	20	20	800	14.14393
12	20	20	800	14.14393

Fig. A-3. Modeling of t_r employing DOE (Design of Experiment) in JMP. The values of I_{in}, R_g, and V_{in} are determined by JMP. The values of t_r are simulated by Fig. A-1.

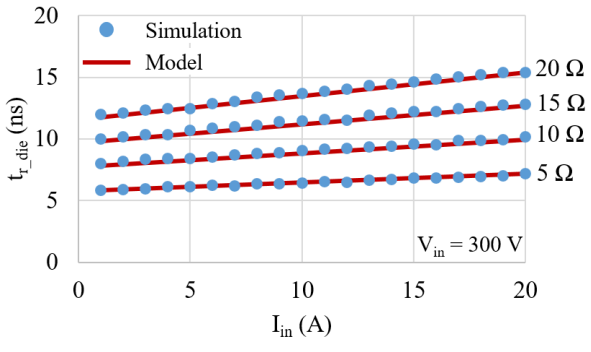
Table A-1. Coefficients of t_r in (A-1) obtained by JMP

d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8
0.045122	0.39024	-1.75×10^{-5}	9.03×10^{-3}	-4×10^{-5}	-7×10^{-6}	-3.9×10^{-6}	3.8266

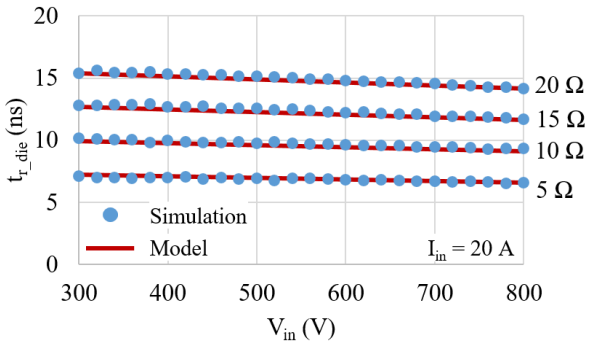
The accuracy of the model in (A-1) and Table A-1 is verified in Fig. A-4, where dots show the simulation results and lines show the modeled results. The input voltage V_{in}, input current I_{in}, and gate resistance R_g are swept over a wide range. Good accuracy is achieved for all the conditions.



(a)



(b)



(c)

Fig. A-4. Verification of t_r model in (A-1) and Table A-1, where dots show simulation results and lines show the modeled results. (a) Verification of model under varying R_g, V_{in} = 300 V, and I_{in} = 1 A, 10 A, 20A. (b) Verification of model under varying I_{in}, V_{in} = 300 V, and R_g = 5 Ω, 10 Ω, 15 Ω, 20 Ω. (c) Verification of model under varying V_{in}, I_{in} = 20 A, and R_g = 5 Ω, 10 Ω, 15 Ω, 20 Ω.

Next, the dependence of t_r on parasitic inductances is derived. The model of t_r as a function of inductances under one specific conditions (i.e., V_{in} = 300 V, I_{in} = 20 A, and R_g = 20 Ω) is analyzed first for simplicity. The interactions among inductances and operating conditions will be included and derived after that.

Fig. A-5(a) shows the simulation results of Fig. A-1 with variation of L_{cm}, L_p, or L_g, while the other inductances are set as 0 nH. According to Fig. A-5(a), current rise time increases with L_{cm}, L_p, and L_g. The influence of L_{cm} is most significant. The influence of L_g is the slightest and sometimes can be neglected. Quadratic equations are able be model the trends with high accuracy. Because L_d and L_s are also on power commutation loop (similar to L_p), the same quadratic model as L_p (shown in Fig. A-5(a)) can be employed for L_d and L_s by simply dividing the coefficients by 2, as demonstrated by Fig. A-5(b). A similar method can be employed for the models of L_{kg} and L_k.

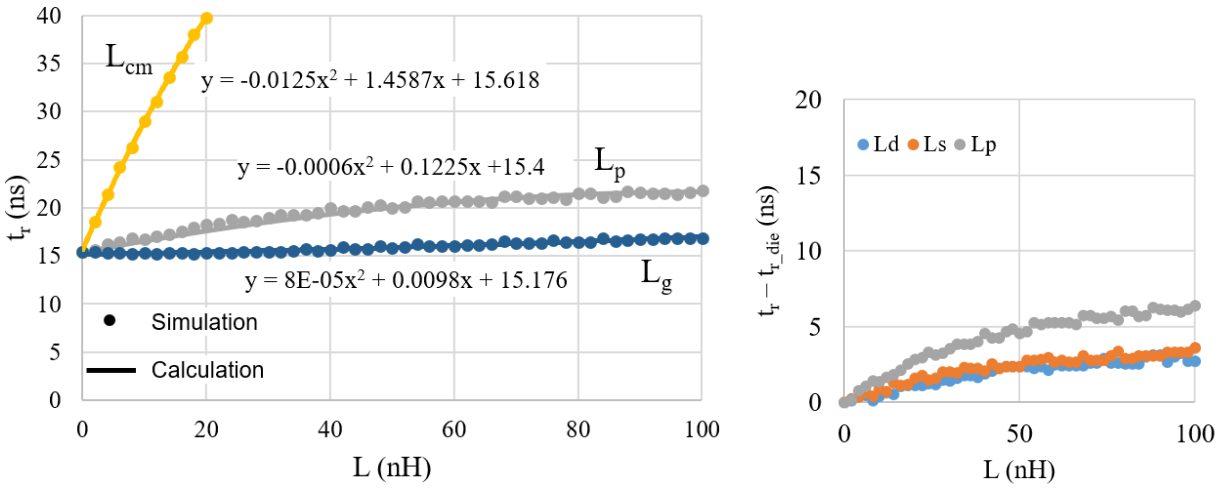


Fig. A-5. Simulation results of Fig. A-1 with variation of one inductance and the other inductances are set as 0 nH. The operating conditions are V_{in} = 300 V, I_{in} = 20 A, and R_g = 20 Ω. Dots show simulation results and lines show the calculated results from quadratic functions. (a) Influence of L_{cm}, L_p, and L_g on t_r, (b) influence of L_d, L_s and L_p on (t_r – t_{r_die}).

The model of t_r as a function of parasitic inductances can be represented as

$$\begin{aligned} t_r &= c_1 L_{cm}^2 + c_2 L_{cm} + c_3 \left(L_p^2\right)_{eq} + c_4 \left(L_p\right)_{eq} + c_5 \left(L_g^2\right)_{eq} + c_6 \left(L_g\right)_{eq} \\ &+ c_7 L_{cm}^2 \left(L_p^2\right)_{eq} + c_8 L_{cm}^2 \left(L_p\right)_{eq} + c_9 L_{cm} \left(L_p^2\right)_{eq} + c_{10} L_{cm} \left(L_p\right)_{eq} \\ &+ c_{11} L_{cm}^2 \left(L_g^2\right)_{eq} + c_{12} L_{cm}^2 \left(L_g\right)_{eq} + c_{13} L_{cm} \left(L_g^2\right)_{eq} + c_{14} L_{cm} \left(L_g\right)_{eq} \\ &+ t_{r\_die} \end{aligned} \tag{A-2}$$

where interactions between L_p and L_s, and between L_{cm} and L_g are considered. The interaction between L_p and L_g is neglected due to the slight influence of L_g and moderate influence of L_p on t_r. The equivalent inductances in (A-2) are defined as

$$\begin{aligned} \left(L_p^2\right)_{eq} &= L_p^2 + 0.5 L_s^2 + 0.5 L_d^2 \\ \left(L_p\right)_{eq} &= L_p + 0.5 L_s + 0.5 L_d \end{aligned} \tag{A-3}$$

$$\left(L_g^2\right)_{eq} = L_g^2 + 0.5L_k^2 + 0.5L_{kg}^2$$

$$\left(L_g\right)_{eq} = L_g + 0.5L_k + 0.5L_{kg}$$

Coefficients c_1 and c_2 for L_{cm} can be obtained by setting all the other inductances to be 0 nH. The results are shown in Fig. A-5(a). Similar method can be used to solve for c_3 to c_6. The values are listed in Table A-2.

Table A-2. Coefficients of c_1 to c_6 in (A-2) obtained from Fig. A-5 (a)

c_1	c_2	c_3	c_4	c_5	c_6
-0.0125	1.4587	-6×10^{-4}	0.1225	8×10^{-5}	9.8×10^{-3}

Then, coefficients c_7 to c_{10} will be solved by setting L_g as 0 nH. The term $\Delta t_{r\_Lg\,=\,0nH}$ is defined as

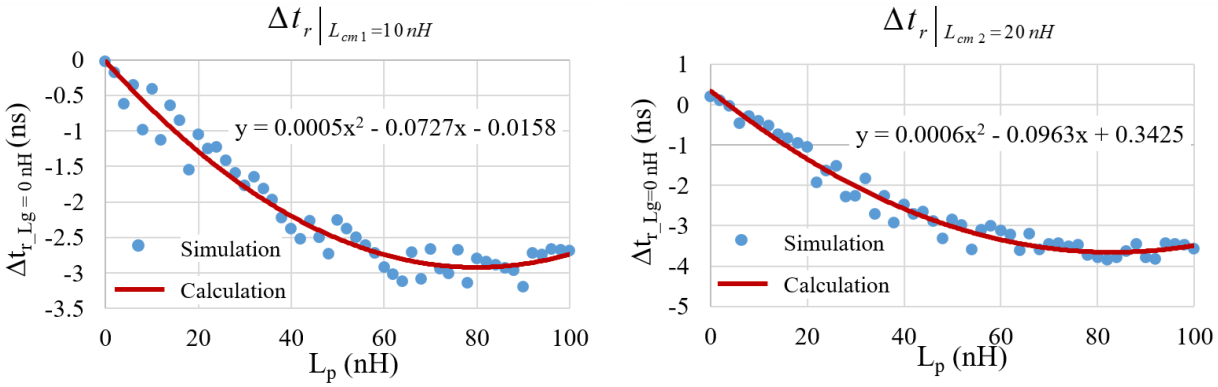
$$\begin{aligned}\Delta t_{r\_L_g=0nH} &= t_{r\_L_g=0nH} - \left(c_1L_{cm}^2 + c_2L_{cm} + c_3L_p^2 + c_4L_p + t_{r\_die}\right) \\ &= \left(c_7L_{cm}^2 + c_9L_{cm}\right)L_p^2 + \left(c_8L_{cm}^2 + c_{10}L_{cm}\right)L_p\end{aligned} \tag{A-4}$$

where $t_{r\_Lg\,=\,0nH}$ is the current rise time when L_g = 0 nH. Subscript "eq" is omitted thereafter for simplicity.

Equation (A-4) is reduced to a quadratic equation when L_{cm} is certain. Two sets of simulations are performed with L_{cm} = 10 nH and L_{cm} = 20 nH, respectively. The results are shown in Fig. A-6. The obtained $\Delta t_{r\_Lg\,=\,0nH}$ can be modeled by quadratic equations with good accuracy. Neglecting the small constant terms, coefficients c_7 to c_{10} can be solved by

$$\begin{cases} \left(c_7 L_{cm}^2 + c_9 L_{cm}\right)\Big|_{L_{cm}=10} = 0.0005 \\ \left(c_8 L_{cm}^2 + c_{10} L_{cm}\right)\Big|_{L_{cm}=10} = -0.0727 \end{cases} \qquad \begin{cases} \left(c_7 L_{cm}^2 + c_9 L_{cm}\right)\Big|_{L_{cm}=20} = 0.0006 \\ \left(c_8 L_{cm}^2 + c_{10} L_{cm}\right)\Big|_{L_{cm}=20} = -0.0963 \end{cases} \tag{A-5}$$

The solutions of (A-5) are shown in Table A-3



(a) **(b)**

Fig. A-6. (a) Modeling of $\Delta t_{r\_Lg\,=\,0\,nH}$ in (A-4) when L_{cm1} = 10 nH, and (b) modeling of $\Delta t_{r\_Lg\,=\,0\,nH}$ in (A-4) when L_{cm1} = 20 nH. The operating conditions are V_{in} = 300 V, I_{in} = 20 A, and R_g = 20 Ω.

Table A-3. Coefficients of c_7 to c_{10} in (A-2) obtained from (A-5)

c_7	c_8	c_9	c_{10}
-2×10^{-6}	2.455×10^{-4}	7×10^{-5}	-9.725×10^{-3}

Following the same method, coefficients c_{11} to c_{14} can be solved by setting L_p as 0 nH. The term $\Delta t_{r\_Lp\,=\,0nH}$ is defined as

$$\begin{aligned} \Delta t_{r\_L_p=0nH} &= t_{r\_L_p=0nH} - \left(c_1 L_{cm}^2 + c_2 L_{cm} + c_5 L_g^2 + c_6 L_g + t_{r\_die}\right) \\ &= \left(c_{11} L_{cm}^2 + c_{13} L_{cm}\right) L_g^2 + \left(c_{12} L_{cm}^2 + c_{14} L_{cm}\right) L_g \end{aligned} \tag{A-6}$$

where $t_{r\_Lp\,=\,0nH}$ is the current rise time when L_p = 0 nH.

Equation (A-6) is reduced to a quadratic equation when L_{cm} is certain. Two sets of simulations are performed with L_{cm} = 10 nH and L_{cm} = 20 nH, respectively. The results are shown in Fig. A-7. The obtained $\Delta t_{r\_Lp\,=\,0nH}$ can be modeled by quadratic equations with good accuracy. Neglecting the small constant terms, coefficients c_{11} to c_{14} can be solved by

$$\begin{cases} \left(c_{11}L_{cm}^2 + c_{13}L_{cm}\right)\Big|_{L_{cm}=10} = 0.0002 \\ \left(c_{12}L_{cm}^2 + c_{14}L_{cm}\right)\Big|_{L_{cm}=10} = -0.0463 \end{cases} \qquad \begin{cases} \left(c_{11}L_{cm}^2 + c_{13}L_{cm}\right)\Big|_{L_{cm}=20} = 0.0002 \\ \left(c_{12}L_{cm}^2 + c_{14}L_{cm}\right)\Big|_{L_{cm}=20} = -0.0535 \end{cases} \tag{A-7}$$

The solutions of (A-7) are shown in Table A-4.

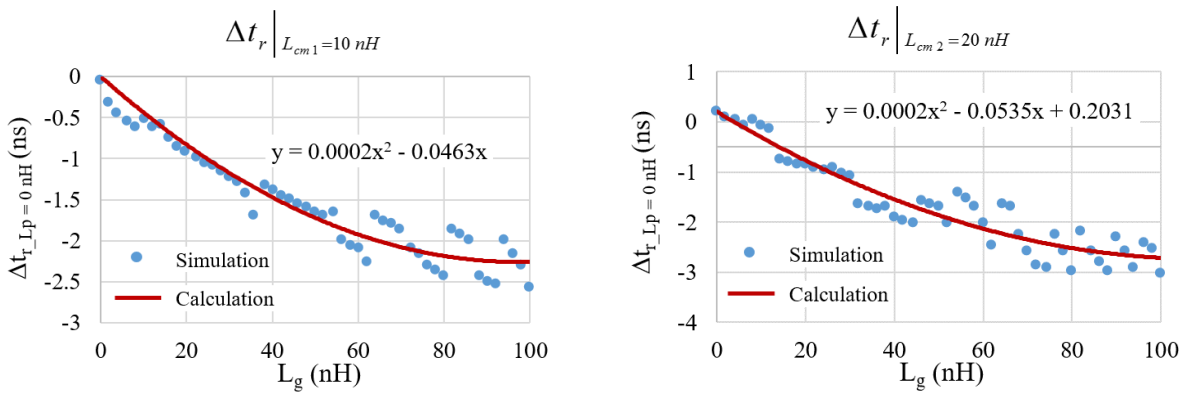


Fig. A-7. (a) Modeling of $\Delta t_{r\_Lg\,=\,0\,nH}$ in (A-4) when L_{cm1} = 10 nH, and (b) modeling of $\Delta t_{r\_Lg\,=\,0\,nH}$ in (A-4) when L_{cm1} = 20 nH. The operating conditions are V_{in} = 300 V, I_{in} = 20 A, and R_g = 20 Ω.

Table A-4. Coefficients of c_{11} to c_{14} in (A-2) obtained from (A-7)

c_{11}	c_{12}	c_{13}	c_{14}
-1×10^{-6}	1.955×10^{-4}	3×10^{-5}	-6.583×10^{-3}

The dependence of t_r on parasitic inductances under one specific conditions (i.e., V_{in} = 300 V, I_{in} = 20 A, and R_g = 20 Ω) has been obtained. The interactions among inductances and operating

conditions will be derived by expressing the coefficients of inductances (i.e., c_1 to c_{14}) as functions of operating conditions.

Fig. A-8 shows the simulation results of Fig. A-1 with variation of operating conditions when all the inductances are set as 5 nH. The linearity property as bare die case (shown in Fig. A-2) is maintained even with the consideration of parasitic inductances. Thus, the dependence of c_1 to c_{14} on V_{in}, I_{in}, and R_g should also be linear. Because V_{in} has minor influence on t_r, the interaction between V_{in} and inductance should also be slight and will not be included.

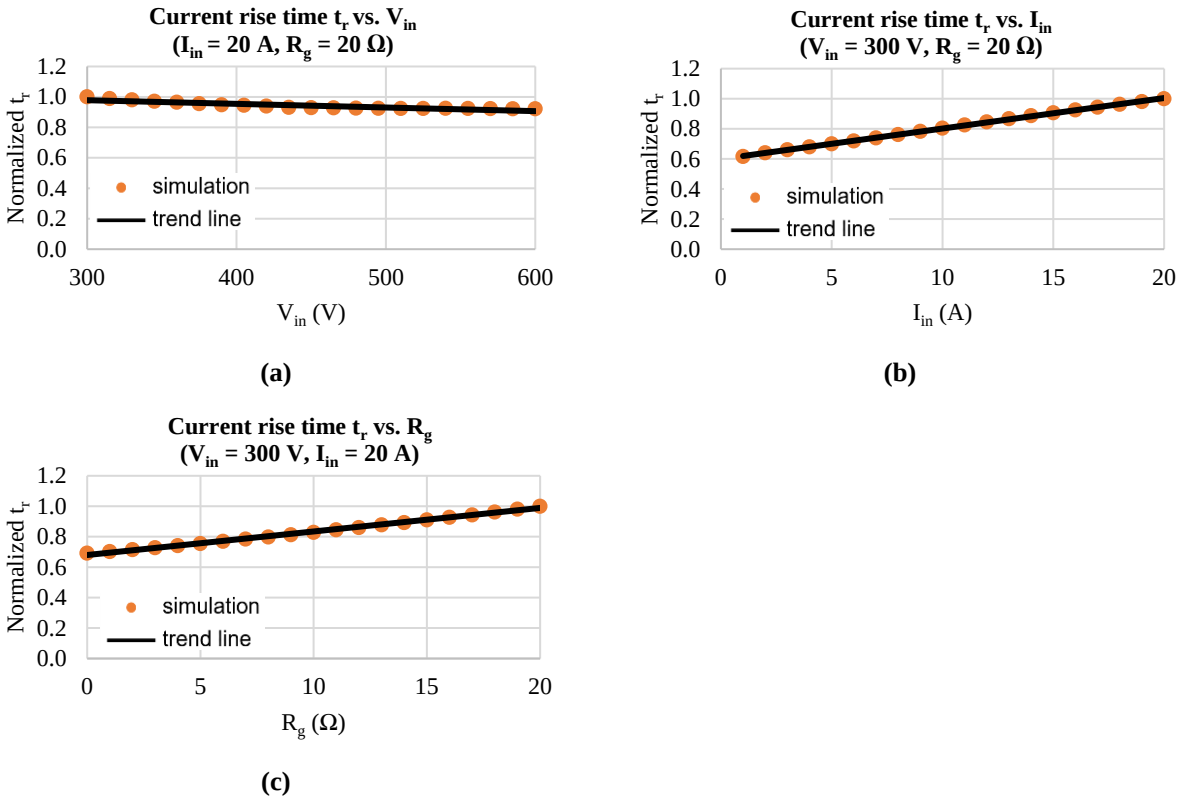


Fig. A-8. Simulation results of Fig. A-1 with all the inductances set as 5 nH. (a) Influence of V_{in} on t_r; (b) influence of I_{in} on t_r; (c) influence of R_g on t_r, where dots show simulation results and lines show the calculated results from linear functions.

Firstly, c_1 and c_2 as functions of I_{in} will be derived. The term $t_{r\_Lp=0nH,Lg=0nH}$ is defined as current rise time when $L_p = L_g = 0$ nH. With constant V_{in} and R_g, $t_{r\_Lp=0nH,Lg=0nH}$ can be expressed as

$$t_{r\_L_p=0nH,L_g=0nH}(I_{in}) = c_1(I_{in})L_{cm}^2 + c_2(I_{in})L_{cm} + t_{r\_die}(I_{in}) \quad \text{(A-8)}$$

where $c_1(I_{in})$ and $c_2(I_{in})$ are both linear functions.

Equation (A-8) reduces to a quadratic equation when I_{in} is certain. The difference of $t_{r\_Lp=0nH,Lg=0nH}$ when I_{in} = 20 A and $t_{r\_Lp=0nH,Lg=0nH}$ when I_{in} = 10 A is plotted in Fig. A-9. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω. According to the figure, this difference is linearly increasing with L_{cm}, which means c_1 is independent of I_{in}. Equation (A-8) can be re-written as

$$t_{r\_L_p=0nH,L_g=0nH}(I_{in}) = c_1 L_{cm}^2 + (b_1 + b_2 I_{in})L_{cm} + t_{r\_die} \quad \text{(A-9)}$$

where b_2 can be calculated based on the linear equation in Fig. A-9 as

$$b_2 = \frac{k_1}{I_{in1} - I_{in2}} = 0.04432 \quad \text{(A-10)}$$

Because c_2 in Table A-2 is calculated when I_{in} = 20 A, b_1 can be solved as

$$b_1 = c_2(I_{in1}) - b_2 I_{in1} = 0.572 \quad \text{(A-11)}$$

The interaction between I_{in} and L_{cm} shown in (A-9) to (A-11) is verified by varying L_{cm} and I_{in}, as shown in Fig. A-10. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω. According to the comparison, the numerical model in (A-9) matches well with simulation over wide current and inductance ranges.

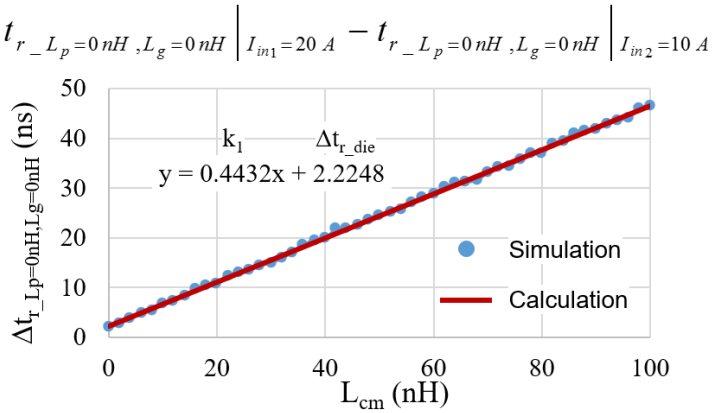


Fig. A-9. Modeling of interaction between I_{in} and L_{cm}. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω.

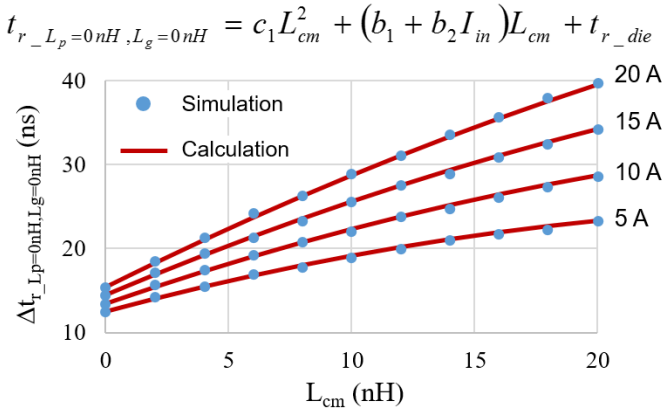


Fig. A-10. Verification of interaction between I_{in} and L_{cm} shown in (A-9) to (A-11) by varying L_{cm} and I_{in}. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω.

Following the same method, c_3 and c_4 as functions of I_{in} can be derived. The term $t_{r\_Lcm=0nH,Lg=0nH}$ is defined as current rise time when $L_{cm} = L_g = 0$ nH. With constant V_{in} and R_g, $t_{r\_Lcm=0nH,Lg=0nH}$ can be expressed as

$$t_{r\_L_{cm}=0nH,L_g=0nH}(I_{in}) = c_3(I_{in})L_p^2 + c_4(I_{in})L_p + t_{r\_die}(I_{in}) \quad \text{(A-12)}$$

where $c_3(I_{in})$ and $c_3(I_{in})$ are both linear functions.

Equation (A-12) reduces to a quadratic equation when I_{in} is certain. The difference of $t_{r\_Lcm=0nH,Lg=0nH}$ when I_{in} = 20 A and $t_{r\_Lcm=0nH,Lg=0nH}$ when I_{in} = 10 A is plotted in Fig. A-11. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω. According to the figure, this difference is linearly increasing with L_p, which means c_3 is independent of I_{in}. Equation (A-12) can be re-written as

$$t_{r\_L_{cm}=0nH,L_g=0nH}(I_{in}) = c_3 L_p^2 + (b_3 + b_4 I_{in}) L_p + t_{r\_die} \tag{A-13}$$

where b_4 can be calculated based on the linear equation in Fig. A-11 as

$$b_4 = \frac{k_2}{I_{in1} - I_{in2}} 0.00191 \tag{A-14}$$

Because c_4 in Table A-2 is calculated when I_{in} = 20 A, b_3 can be solved as

$$b_3 = c_4(I_{in1}) - b_4 I_{in1} = 0.0843 \tag{A-15}$$

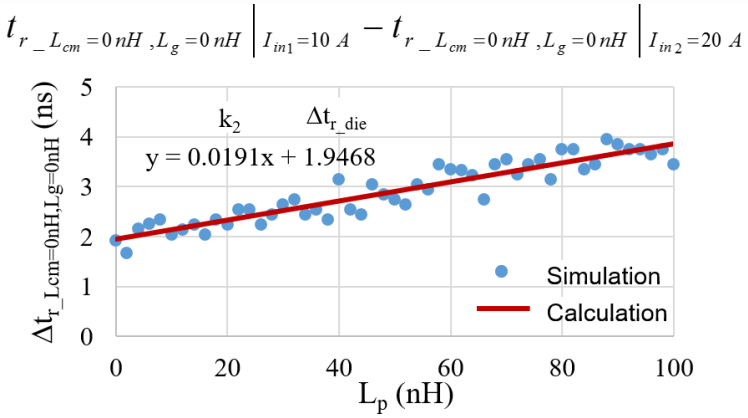


Fig. A-11. Modeling of interaction between I_{in} and L_p. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω.

The interaction between I_{in} and L_p shown in (A-13) to (A-15) is verified by varying L_p and I_{in}, as shown in Fig. A-12. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω. According to the comparison, the numerical model in (A-13) matches well with simulation over wide current and inductance ranges.

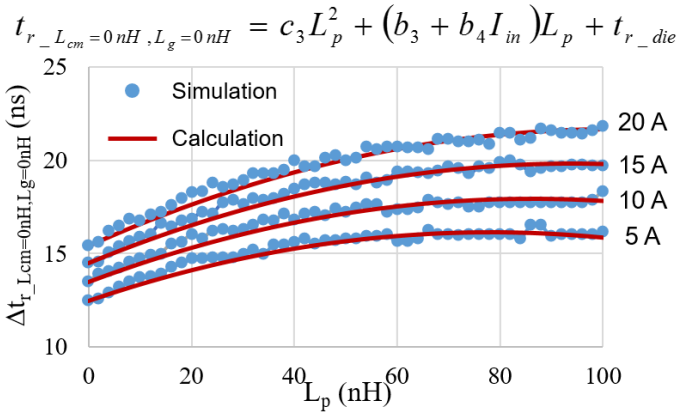


Fig. A-12. Verification of interaction between I_{in} and L_p shown in (A-13) to (A-15) by varying L_p and I_{in}. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω.

If both L_{cm} and L_p are not 0 nH, the interactions between them exist and their corresponding coefficients also depend on I_{in}. Because c_1 and c_3 are not related to I_{in} (as shown in (A-9) and (A-13)). The coefficients of interactions that include L^2_{cm} and L^2_p are also independent of I_{in}. Thus, term $t_{r\_Lg=0nH}$ can be expressed as

$$\begin{aligned} t_{r\_L_g=0nH} &= c_1L_{cm}^2 + (b_1 + b_2I_{in})L_{cm} + c_3L_p^2 + (b_3 + b_4I_{in})L_p \\ &+ c_7L_{cm}^2L_p^2 + c_8L_{cm}^2L_p + c_9L_{cm}L_p^2 + (b_5 + b_6I_{in})L_{cm}L_p \\ &+ t_{r\_die} \end{aligned} \tag{A-16}$$

where $t_{r\_Lg=0nH}$ is the current rise time when L_g = 0 nH with constant V_{in} and R_g

Considering the linear influence of I_{in} on current rise time (as shown in Fig. A-2 and Fig. A-8), the value of b_6 can be calculated as

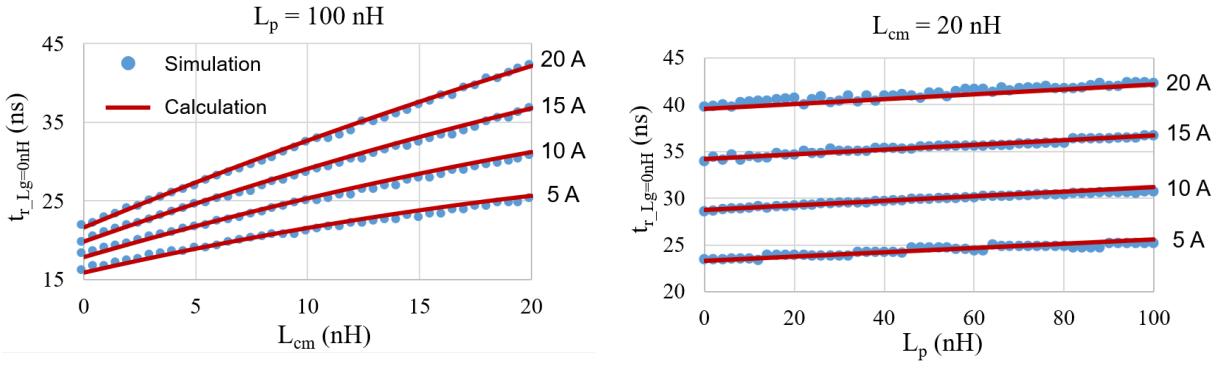
$$b_6 = -b_2 b_4 \text{ -}8.465\times10^{-5} \tag{A-17}$$

where negative sign is decided by the accuracy of model when compared with simulation.

Because $c_{10}(I_{in}) = b_5 + b_6 I_{in}$, b_5 can be solved as

$$b_5 = c_{10}(I_{in1}) - b_6 I_{in1} = \text{-}8.032\times10^{-3} \tag{A-18}$$

The model in (A-16) to (A-18) is verified by varying L_{cm} and I_{in} with L_p = 100 nH and by varying L_p and I_{in} with L_{cm} = 20 nH, as shown in Fig. A-13. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω. According to the comparison, the numerical model in (A-16) matches well with simulation over wide current and inductance ranges.



(a) **(b)**

Fig. A-13. Verification of (A-16) to (A-18) by (a)varying L_{cm} and I_{in} with L_p = 100 nH and (b) varying L_p and I_{in} with L_{cm} = 20 nH. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω.

The parametric simulation in Fig. A-5(a) shows that inductance L_g has minor influence on current rise time. The interaction between I_{in} and L_g should also be slight and doesn't need to be considered. The complete model of t_r as a function of I_{in}, L_{cm}, L_p, and L_g is

$$
\begin{aligned}
t_r(I_{in}) &= c_1 L_{cm}^2 + (b_1 + b_2 I_{in}) L_{cm} + c_3 L_p^2 + (b_3 + b_4 I_{in}) L_p + c_5 L_g^2 + c_6 L_g \\
&+ c_7 L_{cm}^2 L_p^2 + c_8 L_{cm}^2 L_p + c_9 L_{cm} L_p^2 + (b_5 + b_6 I_{in}) L_{cm} L_p \\
&+ c_{11} L_{cm}^2 L_g^2 + c_{12} L_{cm}^2 L_g + c_{13} L_{cm} L_g^2 + c_{14} L_{cm} L_g \\
&+ t_{r\_die}
\end{aligned}
\tag{A-19}
$$

Model (A-19) is verified in Fig. A-14 by varying L_{cm} and I_{in} with L_p = 100 nH and L_g = 100 nH. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω. According to the comparison, good matching between numerical model and simulation results is achieved over wide current and inductance ranges.

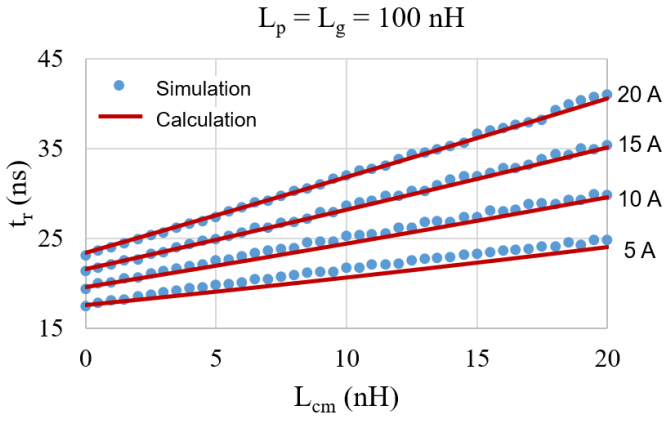


Fig. A-14. Verification of (A-19) by varying L_{cm} and I_{in} with L_p = 100 nH and L_g = 100 nH. The other operating conditions are V_{in} = 300 V and R_g = 20 Ω.

Next, coefficients as functions of R_g will be derived by setting V_{in} and I_{in} to be constant values.

The term $t_{r\_Lp=0nH,Lg=0nH}$ is defined as current rise time when L_p = L_g = 0 nH. The model of $t_{r\_Lp=0nH,Lg=0nH}$ as a function of I_{in} was derived in (A-8) and is repeated here for convenience.

$$
t_{r\_L_p=0nH,L_g=0nH}(I_{in}) = c_1 L_{cm}^2 + (b_1 + b_2 I_{in}) L_{cm} + t_{r\_die} \tag{A-20}
$$

Considering a varying R_g, $t_{r\_Lp=0nH,Lg=0nH}$ can be expressed as

$$t_{r\_L_p=0nH,L_g=0nH}(R_g) = c_1(R_g)L_{cm}^2 + [b_1(R_g) + b_2 I_{in}]L_{cm}L_{cm} + t_{r\_die}(R_g) \quad \text{(A-21)}$$

where $c_1(R_g)$ and $b_2(R_g)$ are both linear functions.

The difference of $t_{r\_Lp=0nH,Lg=0nH}$ when $R_g = 20\ \Omega$ and $t_{r\_Lp=0nH,Lg=0nH}$ when $R_g = 0\ \Omega$ is plotted in Fig. A-15. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A. According to the figure, the coefficients of L^3_{cm}, L^2_{cm}, and L_{cm} are affected by R_g. Term L^3_{cm} was not detected when $R_g = 20\ \Omega$ and will be considered from now on to be accurate for wide operating range. The revised model of $t_{r\_Lp=0nH,Lg=0nH}$ as a function of R_g is

$$t_{r\_L_p=0nH,L_g=0nH} = (a_1 + a_2 R_g)L_{cm}^3 + (a_3 + a_4 R_g)L_{cm}^2 + (a_5 + b_2 I_{in} + a_6 R_g)L_{cm} + t_{r\_die} \quad \text{(A-22)}$$

where a_2, a_4, and a_6 can be calculated based on the linear equations in Fig. A-15 as

$$a_2 = \frac{k_3}{R_{g1} - R_{g2}} = -4.5\times10^{-5}$$

$$a_4 = \frac{k_4}{R_{g1} - R_{g2}} = 0.001775 \quad \text{(A-23)}$$

$$a_6 = \frac{k_5}{R_{g1} - R_{g2}} = -0.024335$$

Equation (A-22) under V_{in1} = 300 V, I_{in1} = 20 A, and $R_{g1} = 20\ \Omega$ has been solved in Fig. A-5, (A-2), and Table A-2. Applying $a_1 + a_2 R_{g1} = 0$, $a_3 + a_4 R_{g1} = c_1$, and $a_5 + b_2 I_{in1} + a_6 R_{g1} = c_2$, a_1, a_3, and a_5 can be solved as

$$a_1 = -a_2 R_{g1} = 9\times10^{-4} \quad \text{(A-24)}$$

$$a_3 = c_1\left(I_{in1}, R_{g1}\right) - a_4 R_{g1} = \text{-}0.048$$

$$a_5 = c_2\left(I_{in1}, R_{g1}\right) - b_2 I_{in1} - a_6 R_{g1} = 1.0587$$

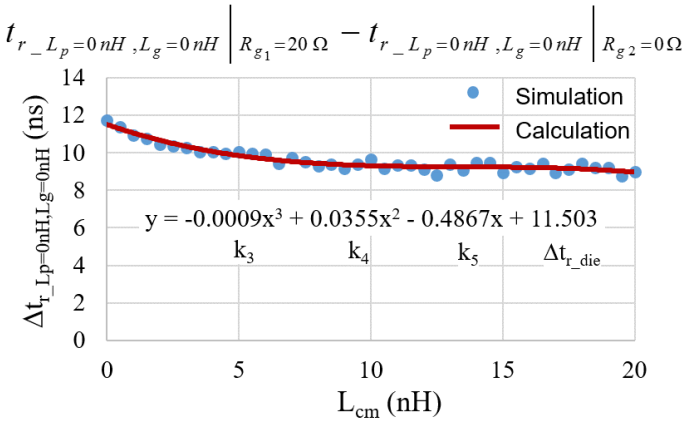


Fig. A-15. Modeling of interaction between R_g and L_{cm}. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A.

The interaction between R_g and L_{cm} shown in (A-22) to (A-24) is verified by varying L_{cm} and R_g, as shown in Fig. A-16. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A. According to the comparison, the numerical model in (A-22) matches well with simulation results over wide R_g and inductance ranges.

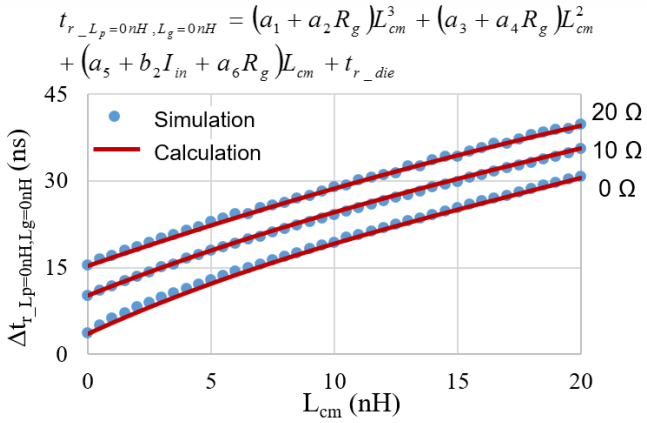


Fig. A-16. Verification of interaction between R_g and L_{cm} shown in (A-23) and (A-24) by varying L_{cm} and R_g. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A.

Following the same method, the model of $t_{r\_Lcm=0nH,Lg=0nH}$ as a function of R_g can be derived based on (A-13) and expressed as

$$t_{r\_L_{cm}=0nH,L_g=0nH}(R_g) = c_3(R_g)L_p^2 + [b_3(R_g) + b_4 I_{in}]L_p + t_{r\_die}(R_g) \quad \text{(A-25)}$$

where both $C_3(R_g)$ and $b_3(R_g)$ are linear functions.

The difference of $t_{r\_Lcm=0nH,Lg=0nH}$ when R_g = 20 Ω and $t_{r\_Lcm=0nH,Lg=0nH}$ when R_g = 0 Ω is plotted in Fig. A-17. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A. According to the figure, this difference is linearly increasing with L_p, which means c_3 is independent of R_g. Equation (A-25) can be re-written as

$$t_{r\_L_{cm}=0nH,L_g=0nH} = c_3 L_p^2 + (a_7 + b_4 I_{in} + a_8 R_g)L_p + t_{r\_die} \quad \text{(A-26)}$$

where a_8 can be calculated based on the linear equations in Fig. A-17 as

$$a_8 = \frac{k_6}{R_{g1} - R_{g2}} = 1.915 \times 10^{-3} \quad \text{(A-27)}$$

Equation (A-26) under V_{in1} = 300 V, I_{in1} = 20 A, and R_{g1} = 20 Ω has been solved in Fig. A-5, (A-2), and Table A-2. Applying $a_7 + b_4 I_{in1} + a_8 R_{g1} = c_4$, a_7 can be solved as

$$a_7 = c_4(I_{in1}, R_{g1}) - b_4 I_{in1} - a_8 R_{g1} = 0.046 \quad \text{(A-28)}$$

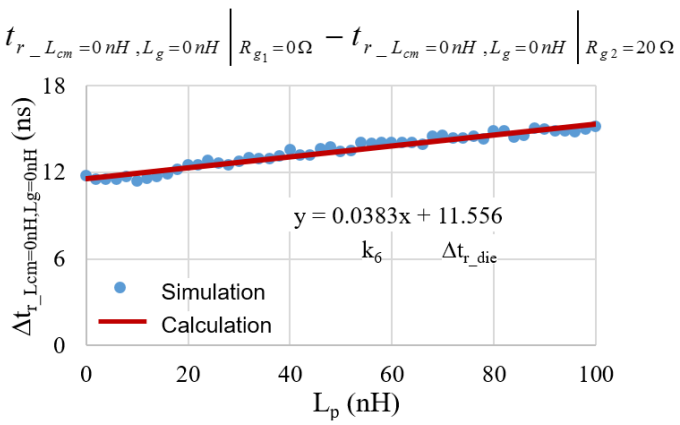


Fig. A-17. Modeling of interaction between R_g and L_p. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A.

The interaction between R_g and L_p shown in (A-26) and (A-27) is verified by varying L_p and R_g, as shown in Fig. A-16. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A. According to the comparison, the numerical model in (A-26) matches well with simulation results over wide R_g and inductance ranges.

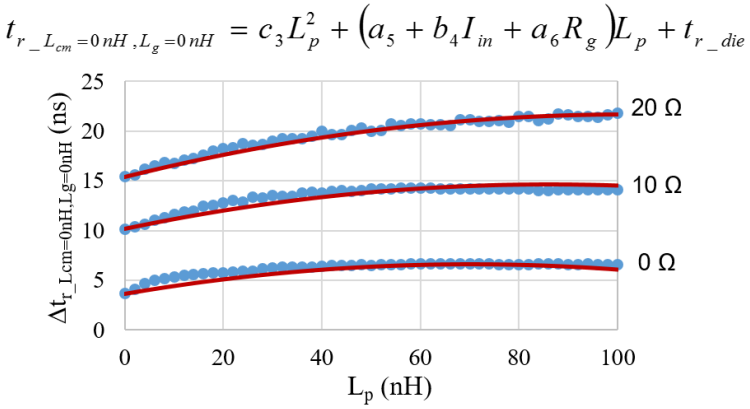


Fig. A-18. Verification of interaction between R_g and L_p shown in (A-26) and (A-27) by varying L_p and R_g. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A.

If both L_{cm} and L_p are not 0 nH, the interactions between them exist and their corresponding coefficients also depend on R_g. Because c_3 is not related to R_g (as shown in (A-26)). The

coefficients of interactions that include L^2_p are also independent of R_g. Thus, term $t_{r\_Lg=0nH}$ can be expressed as

$$\begin{aligned} t_{r\_L_g=0nH} &= \left(a_1 + a_2 R_g\right) L_{cm}^3 + \left(a_3 + a_4 R_g\right) L_{cm}^2 + \left(a_5 + b_2 I_{in} + a_6 R_g\right) L_{cm} + c_3 L_p^2 + \left(a_7 + b_4 I_{in} + a_8 R_g\right) L_p \\ &+ c_7 L_{cm}^2 L_p^2 + \left(a_9 + a_{10} R_g\right) L_{cm}^2 L_p + c_9 L_{cm} L_p^2 + \left(a_{11} + b_6 I_{in} + a_{12} R_g\right) L_{cm} L_p \\ &+ t_{r\_die} \end{aligned} \tag{A-29}$$

where $t_{r\_Lg=0nH}$ is the current rise time when L_g = 0 nH.

Considering the linear influence of R_g on current rise time (as shown in Fig. A-2 and Fig. A-8), the value of a_{10} and a_{12} can be calculated as

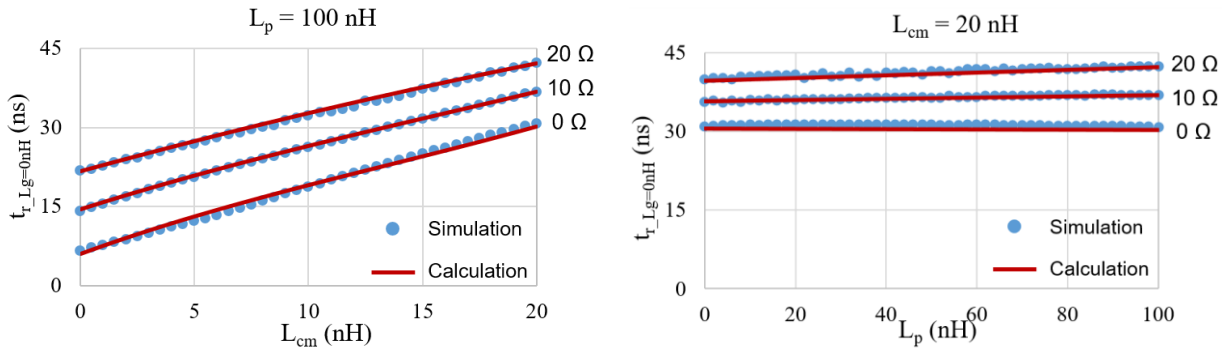
$$\begin{aligned} a_{10} &= -a_4 a_8 = -3.399\times10^{-6} \\ a_{12} &= -a_6 a_8 = 4.66\times10^{-5} \end{aligned} \tag{A-30}$$

where negative sign is decided by the accuracy of model when compared with simulation.

Because $c_8(R_{g1}) = a_9 + a_{10}R_{g1}$ and $b_5 = a_{11} + a_{12}R_{g1}$, a_9 and a_{11} can be solved as

$$\begin{aligned} a_9 &= c_8\left(R_{g1}\right) - a_{10} R_{g1} = 1.775\times10^{-4} \\ a_{11} &= b_5 - a_{12} R_{g1} = -8.964\times10^{-3} \end{aligned} \tag{A-31}$$

The model in (A-29) and (A-31) is verified by varying L_{cm} and R_g with L_p = 100 nH and by varying L_p and R_g with L_{cm} = 20 nH, as shown in Fig. A-19. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A. According to the comparison, the numerical model in (A-29) matches well with simulation over wide R_g and inductance ranges.



(a) **(b)**

Fig. A-19. Verification of (A-29) and (A-31) by (a)varying L_{cm} and R_g with L_p = 100 nH and (b) varying L_p and R_g with L_{cm} = 20nH. The other operating conditions are V_{in} = 300 V and I_{in} = 20 A.

Simulations in Fig. A-5(a), Fig. A-2, and Fig. A-8 show that inductance L_g and input voltage V_{in} have minor influences on current rise time. The interaction between operating conditions and L_g and the interaction between V_{in} and inductances should also be slight and doesn't need to be considered. Thus, the complete model of t_r as a function of R_g, I_{in}, L_{cm}, L_p, and L_g is

$$\begin{aligned} t_r = &\left(a_1 + a_2 R_g\right)L_{cm}^3 + \left(a_3 + a_4 R_g\right)L_{cm}^2 + \left(a_5 + b_2 I_{in} + a_6 R_g\right)L_{cm} \\ &+ c_3 L_p^2 + \left(a_7 + b_4 I_{in} + a_8 R_g\right)L_p \\ &+ c_5 L_g^2 + c_6 L_g \\ &+ c_7 L_{cm}^2 L_p^2 + \left(a_9 + a_{10} R_g\right)L_{cm}^2 L_p + c_9 L_{cm} L_p^2 + \left(a_{11} + b_6 I_{in} + a_{12} R_g\right)L_{cm} L_p \\ &+ c_{11} L_{cm}^2 L_g^2 + c_{12} L_{cm}^2 L_g + c_{13} L_{cm} L_g^2 + c_{14} L_{cm} L_g \\ &+ d_1 I_{in} + d_2 R_g + d_3 V_{in} + d_4 I_{in} R_g + d_5 I_{in} V_{in} + d_6 R_g V_{in} + d_7 I_{in} R_g V_{in} + d_8 \end{aligned} \tag{A-32}$$

where the values of coefficients are listed in Table A-5.

Equation (A-32) is the final complete model of this section. The whole modeling process employs 14 sweep simulations to obtain the unknown coefficients. This numerical model reveals the trend and significance of the impact of parasitic inductances and operating conditions on t_r,

which can be referred to when applying passive balancing solutions. Similar procedures can be employed to derive the numerical model for other MOSFETs.

Table A-5. Coefficients of t_r in (A-32)

a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8
9×10^{-4}	-4.5×10^{-5}	-0.048	0.001775	1.0587	-0.024335	0.046	1.915×10^{-3}
a_9	a_{10}	a_{11}	a_{12}	b_2	b_4	b_6	c_3
3.135×10^{-4}	-3.399×10^{-6}	-8.964×10^{-3}	4.66×10^{-5}	0.04432	0.00191	-8.465×10^{-5}	-6×10^{-4}
c_5	c_6	c_7	c_9	c_{11}	c_{12}	c_{13}	c_{14}
8×10^{-5}	9.8×10^{-3}	-2×10^{-6}	7×10^{-5}	-1×10^{-6}	1.955×10^{-4}	3×10^{-5}	-6.583×10^{-3}
d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8
0.045122	0.39024	-1.75×10^{-5}	9.03×10^{-3}	-4×10^{-5}	-7×10^{-6}	-3.9×10^{-6}	3.8266

Appendix B Extending Balancing Solutions to Three MOSFETs

The passive balancing structures shown in Chapter 2 (Fig. 2-68) are also applicable to the case with more than 2 power MOSFETs connected in parallel. The structure L_s//R_k (shown in Fig. 2-16) is simulated as an example.

Fig. B-1 shows the simulation schematic, where 3 power MOSFETs with different V_{th} are paralleled. All the parameters are kept the same except for R_k. When R_k = 0 Ω, three gate-source capacitors are directly paralleled (even with L_s inserted). Gate driving currents of M1, M2, and M3 charge the input capacitances of three MOSFETs at the same speed. MOSFET M1 (which has a smaller V_{th}) carries the highest current and M3 (which has a largest V_{th}) carries the lowest current, as shown in Fig. B-2(a). Fig. B-2(b) shows the simulated i_{ds} with R_k = 5 Ω (and L_s = 80 nH). Voltage difference between any two of the gate-source capacitors can be quickly produced to compensate the mismatch in threshold voltages. Current unbalances in both drive-source trace and power-source trace are damped, resulting in more balanced drain-source currents. Good current sharing among the 3 MOSFETs is achieved.

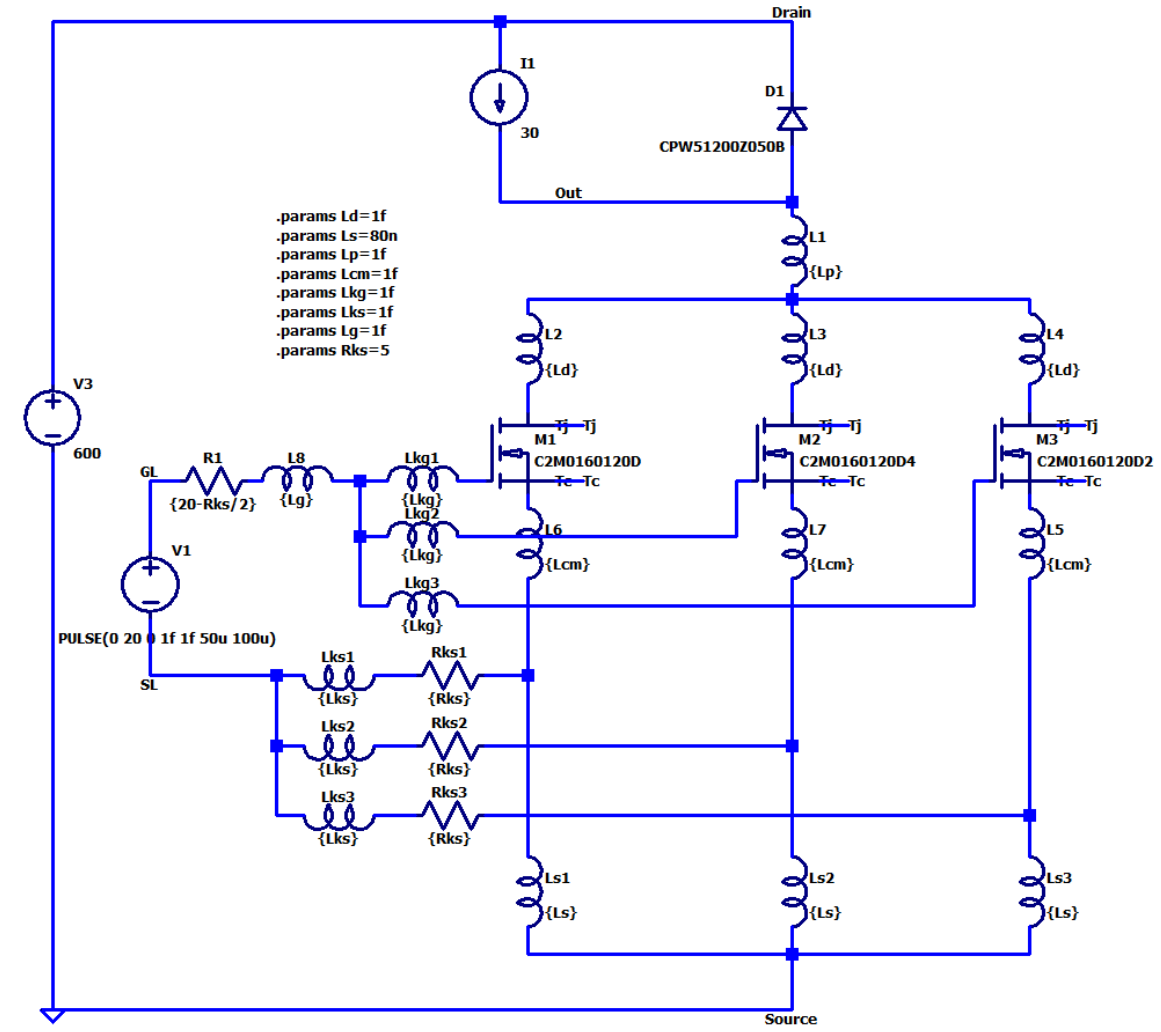


Fig. B-1. Simulation schematic of passive balancing structure L_s//R_k (shown in Fig. 2-16) with 3 MOSFETs in parallel. The threshold voltages of MOSFETs are V_{th1} = 2.48 V, V_{th2} = 2.68 V, and V_{th3} = 3.08 V.

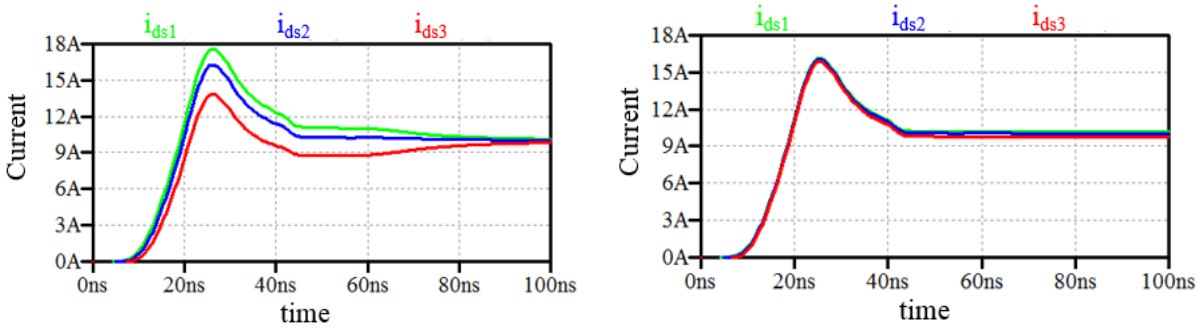


Fig. B-2. (a) Unbalanced drain-source currents without drive-source resistance R_k, and (b) balanced drain-source currents with designed R_k = 5 Ω.

The passive balancing structure shown in Chapter 3 (Fig. 3-2) is also applicable to the case with more than 2 power MOSFETs connected in parallel. Fig. B-3 shows the schematic of passive balancing solution with L_{cm}, R_k, and coupled L_s, where 3 power MOSFETs with different V_{th} are paralleled. Inductance L_k is not considered because the impedance of drive-source trace is dominated by R_k.

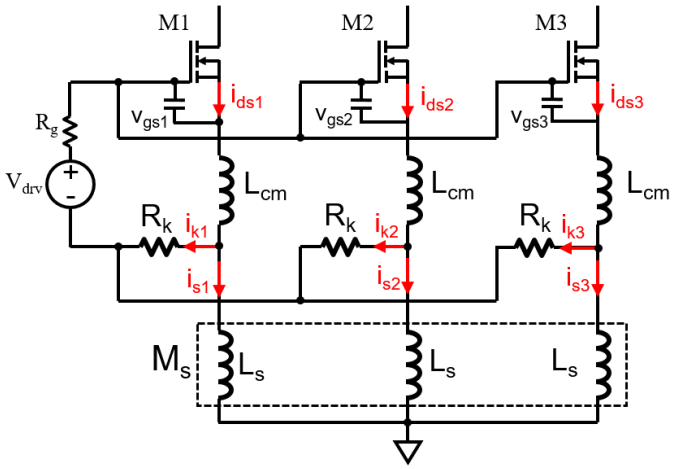


Fig. B-3. Passive balancing structure with 3 MOSFETs in parallel.

According to KCLs at source terminals,

$$i_{ds1} = i_{k1} + i_{s1} \quad i_{ds2} = i_{k2} + i_{s2} \quad i_{ds3} = i_{k3} + i_{s3} \tag{B-1}$$

where the currents bypassed through C_{gs} and C_{ds} are neglected compared to i_{ds} when i_{ds} rises.

Based on KVLs of the loops formed by gate-source capacitors, common-source inductors, and drive-source resistors,

$$v_{gs1} + L_{cm}\frac{di_{ds1}}{dt} + R_k i_{k1} = v_{gs2} + L_{cm}\frac{di_{ds2}}{dt} + R_k i_{k2} = v_{gs3} + L_{cm}\frac{di_{ds3}}{dt} + R_k i_{k3} \tag{B-2}$$

Based on KVLs of the loops formed by gate-source capacitors, common-source inductors, and coupled power-source inductors:

$$\begin{aligned} & v_{gs1} + L_{cm}\frac{di_{ds1}}{dt} + L_s\frac{di_{s1}}{dt} - M_s\frac{di_{s2}}{dt} - M_s\frac{di_{s3}}{dt} \\ &= v_{gs2} + L_{cm}\frac{di_{ds2}}{dt} - M_s\frac{di_{s1}}{dt} + L_s\frac{di_{s2}}{dt} - M_s\frac{di_{s3}}{dt} \\ &= v_{gs3} + L_{cm}\frac{di_{ds3}}{dt} - M_s\frac{di_{s1}}{dt} - M_s\frac{di_{s2}}{dt} + L_s\frac{di_{s3}}{dt} \end{aligned} \tag{B-3}$$

Define

$$\Delta x_{12} = x_1 - x_2 \tag{B-4}$$

where subscript denotes the corresponding MOSFET.

From (B-1),

$$\Delta i_{ds12} = \Delta i_{k12} + \Delta i_{s12} \tag{B-5}$$

From (B-2),

$$\Delta v_{gs12} = -L_{cm}\frac{d\Delta i_{ds12}}{dt} - R_k\Delta i_{k12} \tag{B-6}$$

From (B-3)

$$\Delta v_{gs12} = -L_{cm}\frac{d\Delta i_{ds12}}{dt} - \left(L_s + M_s\right)\frac{d\Delta i_{s12}}{dt} \tag{B-7}$$

Equations (B-1) to (B-3) are the same as the case of two MOSFETs in parallel (as shown in (3-3) and (3-22)). Following the steps from (3-22) to (3-38), the maximum $|i_{ds1(pk)} - i_{ds2(pk)}|$ is

$$\max\left|\Delta i_{ds12(pk)}\right| = \frac{\left(L_s + M_s\right)^2 \left|\Delta V_{th12}\right|}{R_k \left(L_{cm} + L_s + M_s\right)^2} \left[1 - e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)} t_r}\right] + \frac{\left|\Delta V_{th12}\right|}{L_{cm} + L_s + M_s} t_r \qquad \text{(B-8)}$$

Similarly, the maximum peak-current differences between M2 and M3, and between M1 and M3 are

$$\max\left|\Delta i_{ds23(pk)}\right| = \frac{\left(L_s + M_s\right)^2 \left|\Delta V_{th23}\right|}{R_k \left(L_{cm} + L_s + M_s\right)^2} \left[1 - e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)} t_r}\right] + \frac{\left|\Delta V_{th23}\right|}{L_{cm} + L_s + M_s} t_r \qquad \text{(B-9)}$$

$$\max\left|\Delta i_{ds13(pk)}\right| = \frac{\left(L_s + M_s\right)^2 \left|\Delta V_{th13}\right|}{R_k \left(L_{cm} + L_s + M_s\right)^2} \left[1 - e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)} t_r}\right] + \frac{\left|\Delta V_{th13}\right|}{L_{cm} + L_s + M_s} t_r \qquad \text{(B-10)}$$

Combining (B-8) to (B-10), the maximum peak-current difference among the three paralleled MOSFETs is

$$\max\left|\Delta i_{ds(pk)}\right| = \frac{\left(L_s + M_s\right)^2 \left|\Delta V_{th(\max)}\right|}{R_k \left(L_{cm} + L_s + M_s\right)^2} \left[1 - e^{-\frac{R_k\left(L_{cm}+L_s+M_s\right)}{L_{cm}\left(L_s+M_s\right)} t_r}\right] + \frac{\left|\Delta V_{th(\max)}\right|}{L_{cm} + L_s + M_s} t_r \qquad \text{(B-11)}$$

where $\Delta V_{th(max)} = \max(\Delta V_{th12}, \Delta V_{th23}, \Delta V_{th13})$

Current unbalance among three paralleled MOSFETs can be limited by properly selecting the values of passive balancing components based on (B-11).

The modeling method proposed in Chapter 4 also can be extended to the case of more than two MOSFETs in parallel. Modeling of three MOSFETs in parallel is analyzed as an example.

The structure of three MOSFETs in parallel can be reduced to two in parallel if the operating conditions and parasitic inductances are properly modified, as shown in Fig. B-4. The currents and voltages of M1 and M2 in both structures are the same no matter the threshold voltage of M3, as

demonstrated by simulations in Fig. B-5 and Fig. B-6. The switching energy and switching energy mismatch between M1 and M2 can be obtained by following the procedures in Chapter 4. Similar method can be applied to calculate the switching energy difference between M1 and M3 (or M2 and M3).

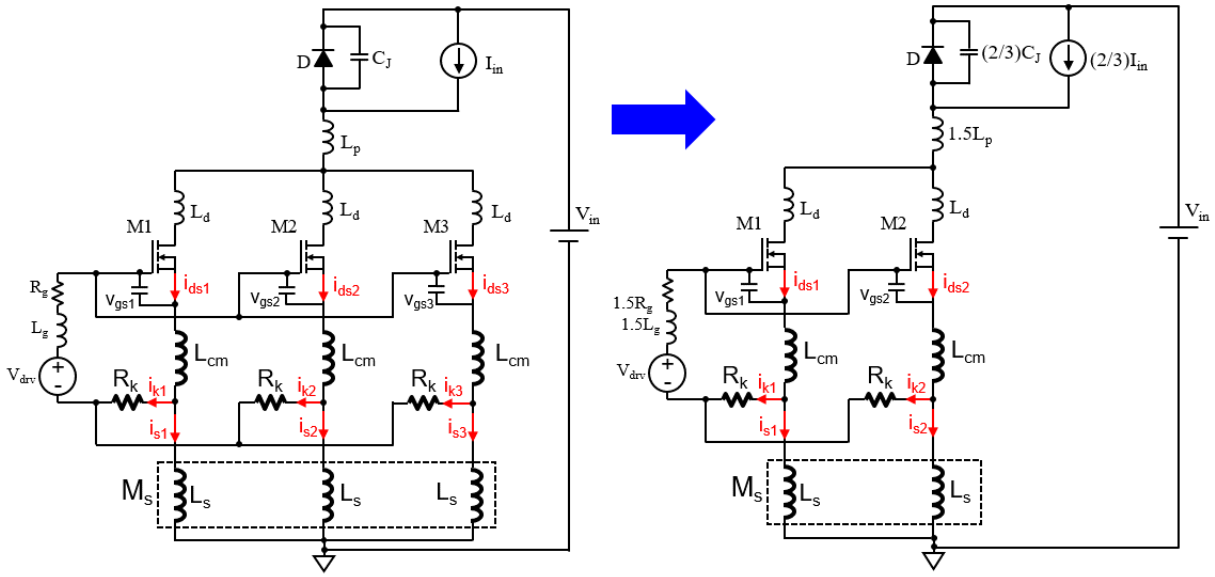


Fig. B-4. Reducing paralleling of three MOSFETs to paralleling of two MOSFETs.

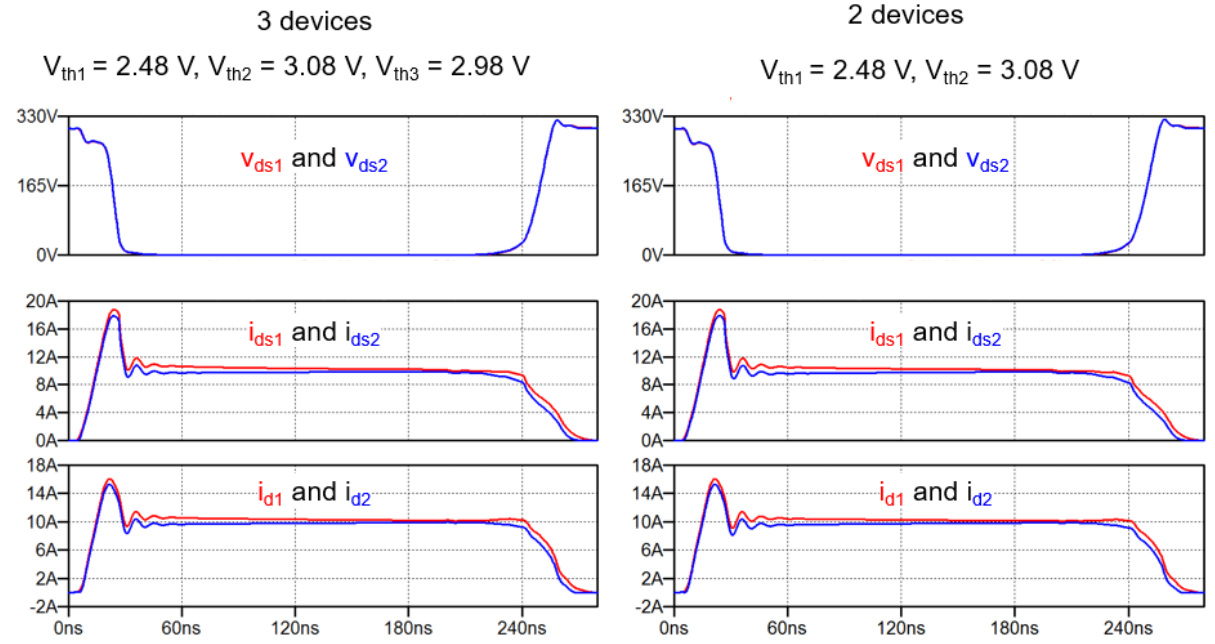


Fig. B-5. Simulation verification of Fig. B-4 with V_{th1} = 2.48 V, V_{th2} = 3.08 V, V_{th3} = 2.98 V.

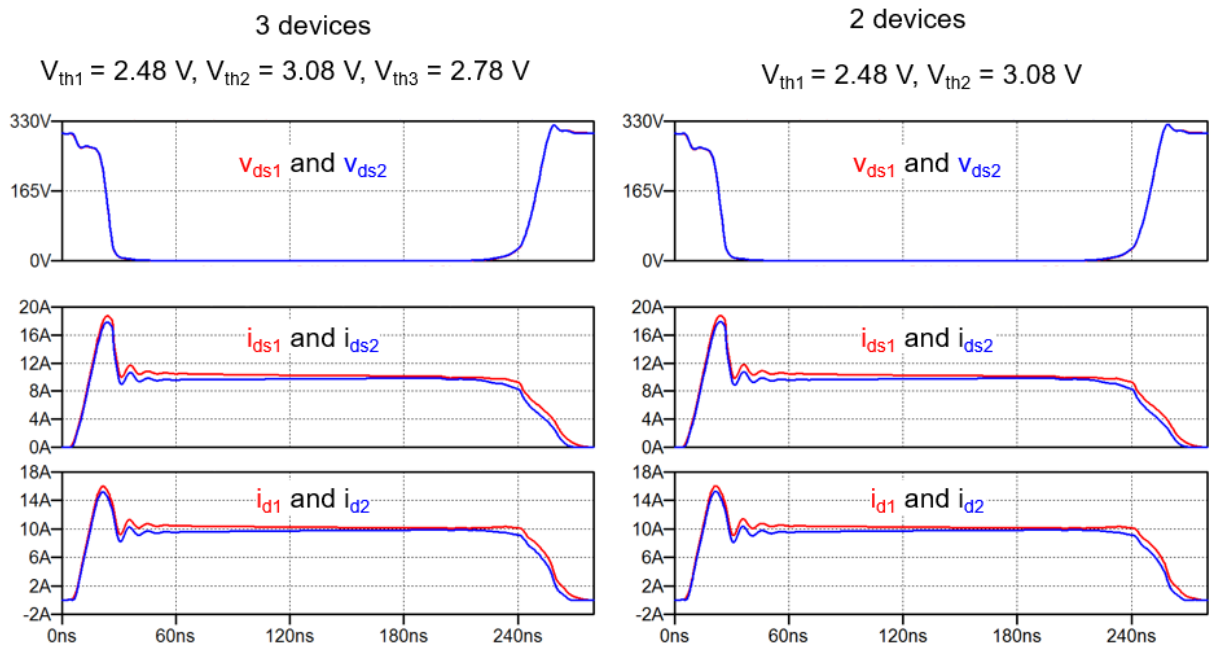


Fig. B-6. Simulation verification of Fig. B-4 with V_{th1} = 2.48 V, V_{th2} = 3.08 V, V_{th3} = 2.78 V.

Appendix C Analytical Model of Switching Transients for a Single MOSFET

C.1 Turn-On Transient

Six variables are modeled. They are channel current (i.e., drain-source current) i_{ch}, gate-source voltage v_{gs}, drain current i_d, drain-source voltage v_{ds}, diode voltage v_{diode}, and gate current i_g.

Stage I: delay period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-1.

The initial conditions of this stage are

$$i_{ch} = 0, v_{gs} = 0, i_d = 0, v_{ds} = V_{in}, v_{diode} = 0, i_g = 0. \quad \text{(C-1)}$$

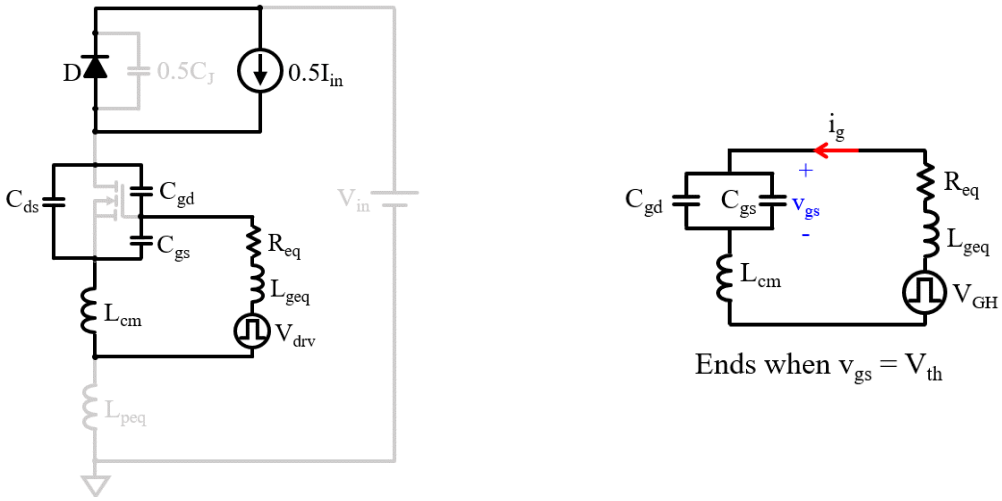


Fig. C-1. (a) Equivalent circuit during Stage I, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-1(b), the following equations are obtained:

$$
\begin{aligned}
i_g &= \left(C_{gs} + C_{gd}\right)\frac{dv_{gs}}{dt} \\
V_{GH} &= \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + R_{eq}i_g + v_{gs} \\
i_{ch} &= 0,\ i_d = 0, v_{ds} = V_{in}, v_{diode} = 0.
\end{aligned}
\tag{C-2}
$$

This stage ends when $v_{gs} = V_{th}$.

Stage II: current rising period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-2.

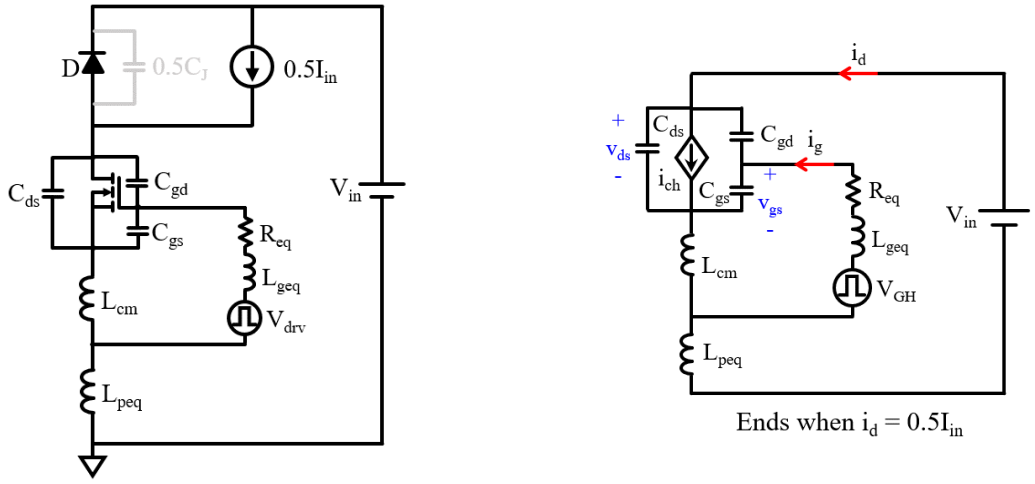


Fig. C-2. (a) Equivalent circuit during Stage II, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-2(b), the following equations are obtained:

$$
\begin{aligned}
i_{ch} &= g_{fs}\left(v_{gs} - V_{th}\right)^2 \\
i_d &= i_{ch} + \left(C_{ds} + C_{gd}\right)\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gs}}{dt} \\
V_{in} &= v_{ds} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} \\
V_{GH} &= R_{eq}i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
i_g &= C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
v_{diode} &= 0
\end{aligned}
\tag{C-3}
$$

This stage ends when $i_d = 0.5I_{in}$.

Stage III: voltage falling period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-3.

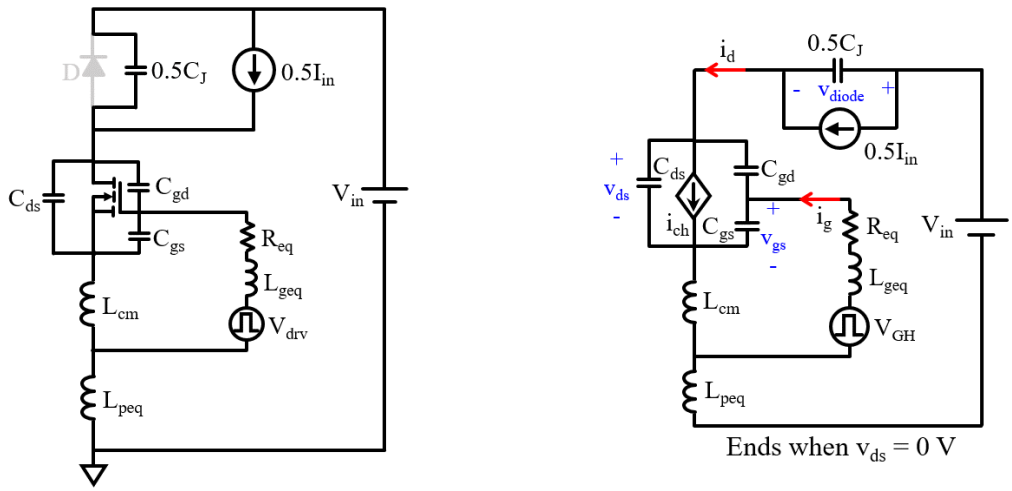


Fig. C-3. (a) Equivalent circuit during Stage III, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-3(b), the following equations are obtained:

$$
\begin{aligned}
i_{ch} &= g_{fs}\left(v_{gs} - V_{th}\right)^2 \\
i_d &= i_{ch} + \left(C_{ds} + C_{gd}\right)\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gs}}{dt} \\
V_{in} &= v_{ds} + v_{diode} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} \\
V_{GH} &= R_{eq}i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
i_g &= C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
i_d &= 0.5I_{in} + 0.5C_J\frac{dv_{diode}}{dt}
\end{aligned}
\qquad \text{(C-4)}
$$

This stage ends when $v_{ds} = 0$ V.

Stage IV: ringing period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-4.

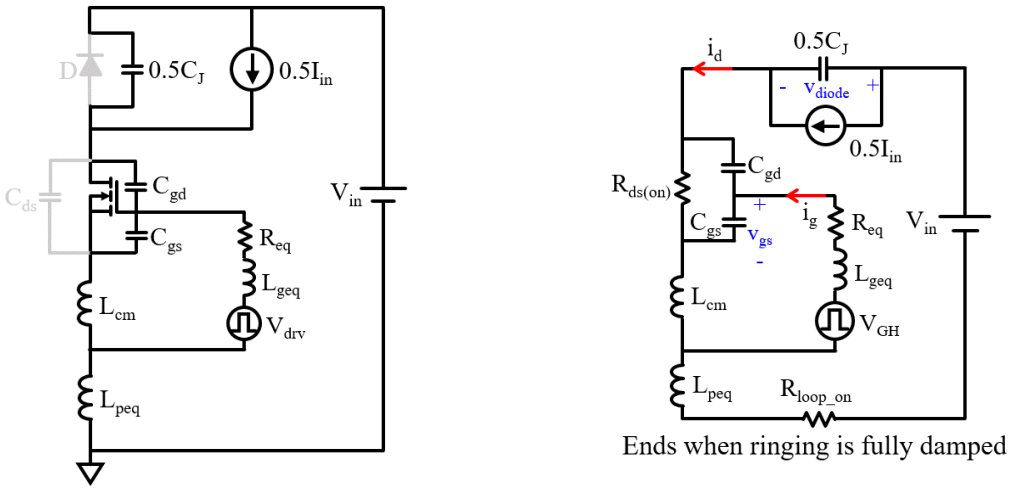


Fig. C-4. (a) Equivalent circuit during Stage IV, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-4(b), the following equations are obtained:

$$
\begin{aligned}
i_d &= 0.5I_{in} + 0.5C_J \frac{dv_{diode}}{dt} \\
V_{in} &= v_{diode} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} + R_{loop\_on} i_d \\
i_g &= \left(C_{gs} + C_{gd}\right)\frac{dv_{gs}}{dt} \\
V_{GH} &= R_{eq} i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
i_{ch} &= i_d \\
v_{ds} &= 0
\end{aligned}
\tag{C-5}
$$

where R_{loop_on} is the damping resistance of parasitic inductances.

This stage ends when ringing is fully damped.

The equations for Stage I – Stage IV can be solved by command ode45 in MATLAB, which requires equations to be written in the form of y′ = f(t, y), as shown in (C-6)-(C-9).

Stage I:

$$\begin{aligned}
&\frac{di_{ch}}{dt} = 0 \\
&\frac{dv_{gs}}{dt} = \frac{i_g}{C_{iss}} \\
&\frac{di_d}{dt} = 0 \\
&\frac{dv_{ds}}{dt} = 0 \\
&\frac{dv_{diode}}{dt} = 0 \\
&\frac{di_g}{dt} = \frac{V_{GH}}{L_{gate}} - \frac{1}{L_{gate}} v_{gs} - \frac{R_{eq}}{L_{gate}} i_g
\end{aligned} \tag{C-6}$$

Stage II:

$$\begin{aligned}
&\frac{di_{ch}}{dt} = -\frac{2C_{gd} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{2C_{gd} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{2C_{oss} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
&\frac{dv_{gs}}{dt} = -\frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{oss}}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
&\frac{di_d}{dt} = \frac{L_{gate}V_{in} - L_{cm}V_{GH}}{L_{gate}L_{loop} - L_{cm}^2} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} + \frac{R_{eq}L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} i_g \\
&\frac{dv_{ds}}{dt} = -\frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
&\frac{dv_{diode}}{dt} = 0 \\
&\frac{di_g}{dt} = \frac{L_{loop}V_{GH} - L_{cm}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} - \frac{L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} - \frac{R_{eq}L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} i_g
\end{aligned} \tag{C-7}$$

Stage III:

$$\begin{aligned}
\frac{di_{ch}}{dt} &= -\frac{2C_{gd}g_{fs}\left(v_{gs}-V_{th}\right)}{C_{iss}C_{oss}-C_{gd}^2}i_{ch}+\frac{2C_{gd}g_{fs}\left(v_{gs}-V_{th}\right)}{C_{iss}C_{oss}-C_{gd}^2}i_d+\frac{2C_{oss}g_{fs}\left(v_{gs}-V_{th}\right)}{C_{iss}C_{oss}-C_{gd}^2}i_g\\
\frac{dv_{gs}}{dt} &= -\frac{C_{gd}}{C_{iss}C_{oss}-C_{gd}^2}i_{ch}+\frac{C_{gd}}{C_{iss}C_{oss}-C_{gd}^2}i_d+\frac{C_{oss}}{C_{iss}C_{oss}-C_{gd}^2}i_g\\
\frac{di_d}{dt} &= \frac{L_{gate}V_{in}-L_{cm}V_{GH}}{L_{gate}L_{loop}-L_{cm}^2}+\frac{L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}v_{gs}-\frac{L_{gate}}{L_{gate}L_{loop}-L_{cm}^2}v_{ds}-\frac{L_{gate}}{L_{gate}L_{loop}-L_{cm}^2}v_{diode}+\frac{R_{eq}L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}i_g\\
\frac{dv_{ds}}{dt} &= -\frac{C_{iss}}{C_{iss}C_{oss}-C_{gd}^2}i_{ch}+\frac{C_{iss}}{C_{iss}C_{oss}-C_{gd}^2}i_d+\frac{C_{gd}}{C_{iss}C_{oss}-C_{gd}^2}i_g\\
\frac{dv_{diode}}{dt} &= -\frac{I_{in}}{C_J}+\frac{1}{0.5C_J}i_d\\
\frac{di_g}{dt} &= \frac{L_{loop}V_{GH}-L_{cm}V_{in}}{L_{gate}L_{loop}-L_{cm}^2}-\frac{L_{loop}}{L_{gate}L_{loop}-L_{cm}^2}v_{gs}+\frac{L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}v_{ds}+\frac{L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}v_{diode}-\frac{R_{eq}L_{loop}}{L_{gate}L_{loop}-L_{cm}^2}i_g
\end{aligned} \tag{C-8}$$

Stage IV:

$$\begin{aligned}
\frac{di_{ch}}{dt} &= \frac{L_{gate}V_{in}-L_{cm}V_{GH}}{L_{gate}L_{loop}-L_{cm}^2}+\frac{L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}v_{gs}-\frac{R_{loop_on}L_{gate}}{L_{gate}L_{loop}-L_{cm}^2}i_d-\frac{L_{gate}}{L_{gate}L_{loop}-L_{cm}^2}v_{diode}+\frac{R_{eq}L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}i_g\\
\frac{dv_{gs}}{dt} &= \frac{1}{C_{iss}}i_g\\
\frac{di_d}{dt} &= \frac{L_{gate}V_{in}-L_{cm}V_{GH}}{L_{gate}L_{loop}-L_{cm}^2}+\frac{L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}v_{gs}-\frac{R_{loop_on}L_{gate}}{L_{gate}L_{loop}-L_{cm}^2}i_d-\frac{L_{gate}}{L_{gate}L_{loop}-L_{cm}^2}v_{diode}+\frac{R_{eq}L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}i_g\\
\frac{dv_{ds}}{dt} &= 0\\
\frac{dv_{diode}}{dt} &= -\frac{I_{in}}{C_J}+\frac{1}{0.5C_J}i_d\\
\frac{di_g}{dt} &= \frac{L_{loop}V_{GH}-L_{cm}V_{in}}{L_{gate}L_{loop}-L_{cm}^2}-\frac{L_{loop}}{L_{gate}L_{loop}-L_{cm}^2}v_{gs}+\frac{R_{loop_on}L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}i_d+\frac{L_{cm}}{L_{gate}L_{loop}-L_{cm}^2}v_{diode}-\frac{R_{eq}L_{loop}}{L_{gate}L_{loop}-L_{cm}^2}i_g
\end{aligned} \tag{C-9}$$

where $L_{gate}=L_{geq}+L_{cm}, L_{loop}=L_{cm}+L_{peq}, C_{iss}=C_{gs}+C_{gd}, C_{oss}=C_{ds}+C_{gd}$.

C.2 Turn-Off Transient

Six variables are modeled. They are channel current (i.e., drain-source current) i_{ch}, gate-source voltage v_{gs}, drain current i_d, drain-source voltage v_{ds}, diode voltage v_{diode}, and gate current i_g.

Stage I: delay period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-5.

The initial conditions of this stage are

$$i_{ch} = 0.5I_{in}, v_{gs} = V_{GH}, i_d = 0.5I_{in}, v_{ds} = 0, v_{diode} = V_{in}, i_g = 0. \tag{C-10}$$

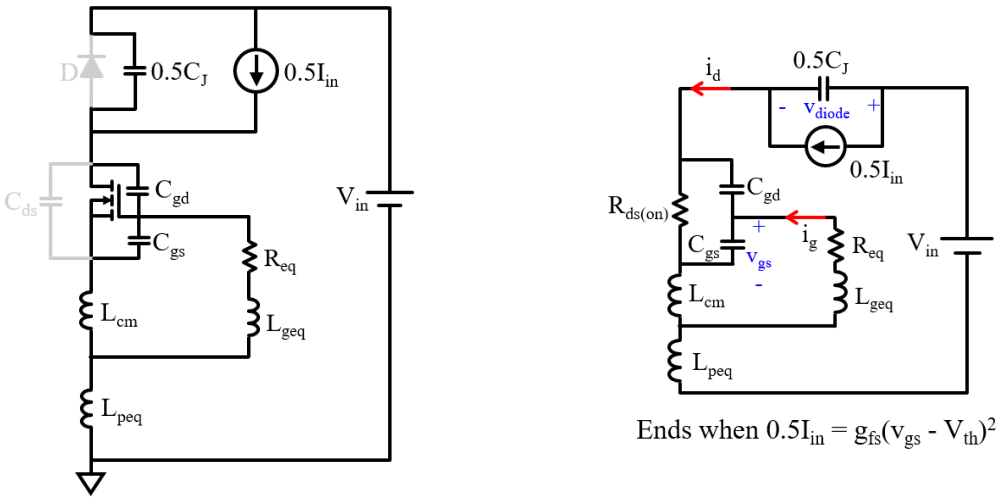


Fig. C-5. (a) Equivalent circuit during Stage I, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-5(b), the following equations are obtained:

$$\begin{aligned} i_g &= \left(C_{gs} + C_{gd}\right)\frac{dv_{gs}}{dt} \\ 0 &= R_{eq} i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} \\ i_d &= i_{ch} = 0.5I_{in}, v_{ds} = 0, v_{diode} = V_{in}. \end{aligned} \tag{C-11}$$

This stage ends when $0.5I_{in} = g_{fs}(v_{gs} - V_{th})^2$.

Stage II: voltage rising period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-6.

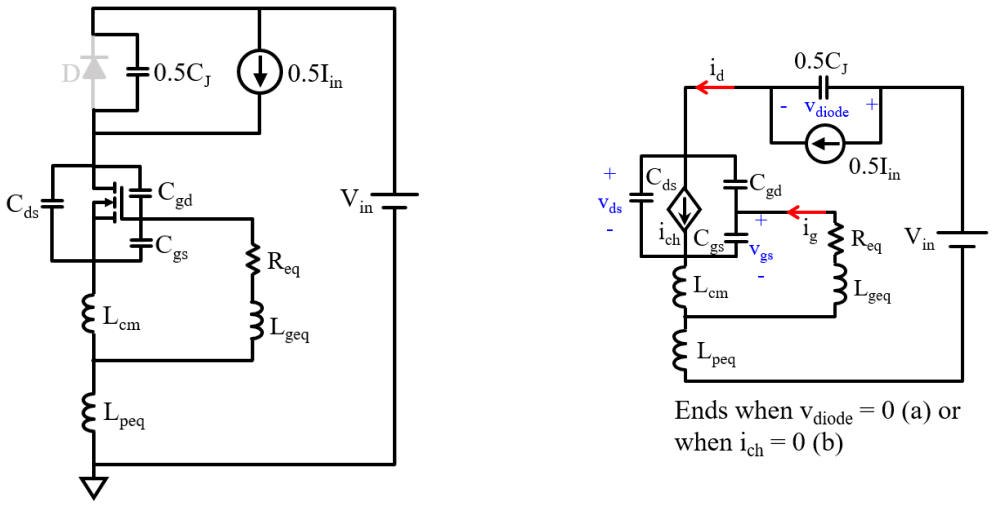


Fig. C-6. (a) Equivalent circuit during Stage II, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-6(b), the following equations are obtained:

$$
\begin{aligned}
i_{ch} &= g_{fs}\left(v_{gs} - V_{th}\right)^2 \\
i_d &= i_{ch} + \left(C_{ds} + C_{gd}\right)\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gs}}{dt} \\
V_{in} &= v_{ds} + v_{diode} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} \\
0 &= R_{eq} i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
i_g &= C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
i_d &= 0.5I_{in} + 0.5C_J\frac{dv_{diode}}{dt}
\end{aligned}
\qquad \text{(C-12)}
$$

This stage ends when v_{diode} = 0 V (a) or when i_{ch} = 0 A (b).

Stage III(a): current falling period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-7.

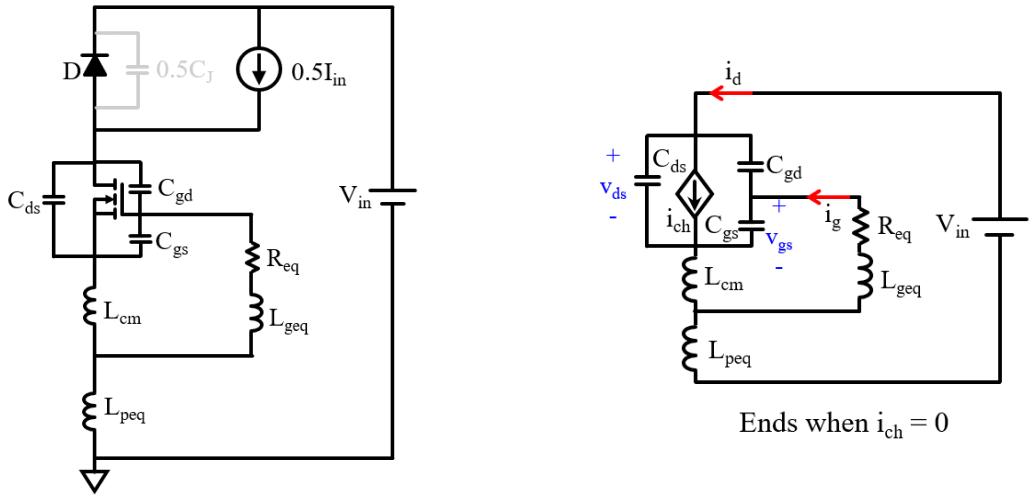


Fig. C-7. (a) Equivalent circuit during Stage III(a), and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-7(b), the following equations are obtained:

$$
\begin{aligned}
i_{ch} &= g_{fs}\left(v_{gs} - V_{th}\right)^2 \\
i_d &= i_{ch} + \left(C_{ds} + C_{gd}\right)\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gs}}{dt} \\
V_{in} &= v_{ds} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} \\
0 &= R_{eq}i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
i_g &= C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
v_{diode} &= 0
\end{aligned}
\qquad \text{(C-13)}
$$

This stage ends when $i_{ch} = 0$.

Stage III(b): remaining voltage rising period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-8.

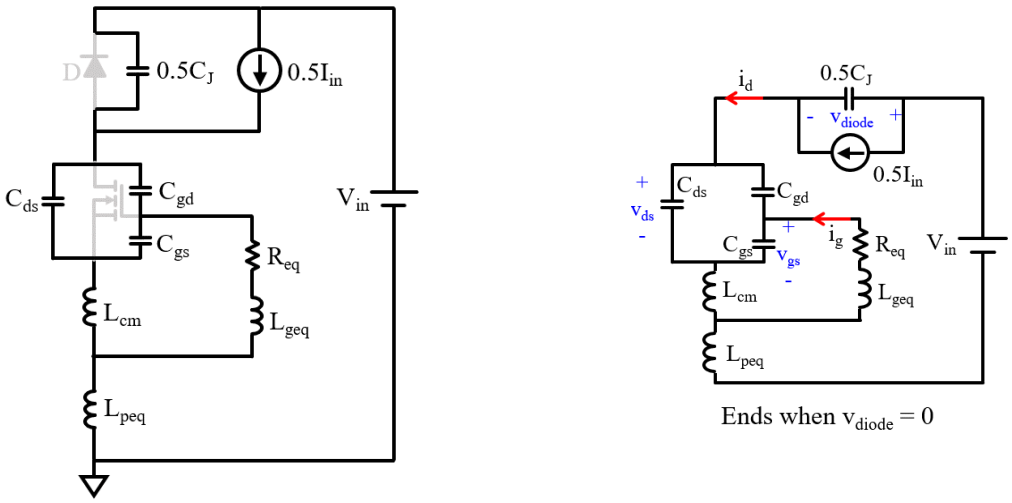


Fig. C-8. (a) Equivalent circuit during Stage III(b), and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-8(b), the following equations are obtained:

$$
\begin{aligned}
& i_{ch} = 0 \\
& i_d = \left(C_{ds} + C_{gd}\right)\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gs}}{dt} \\
& V_{in} = v_{ds} + v_{diode} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} \\
& 0 = R_{eq} i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
& i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
& i_d = 0.5 I_{in} + 0.5 C_J \frac{dv_{diode}}{dt}
\end{aligned}
\qquad \text{(C-14)}
$$

This stage ends when $v_{diode} = 0$.

Stage IV: ringing period.

The equivalent circuit and simplified equivalent circuit of this stage are shown in Fig. C-9.

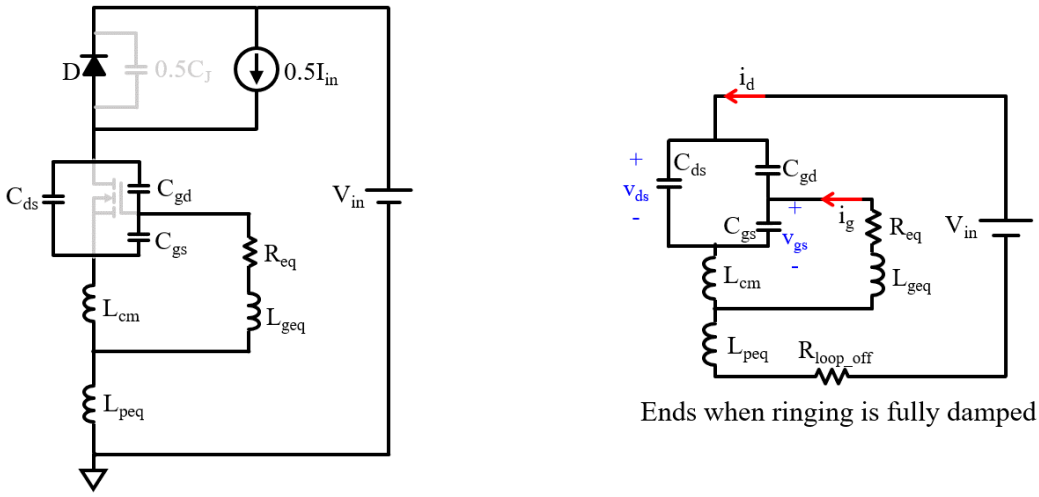


Fig. C-9. (a) Equivalent circuit during Stage IV, and (b) simplified equivalent circuit of (a).

From the circuit in Fig. C-9(b), the following equations are obtained:

$$
\begin{aligned}
i_d &= \left(C_{ds} + C_{gd}\right)\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gs}}{dt} \\
V_{in} &= v_{ds} + \left(L_{cm} + L_{peq}\right)\frac{di_d}{dt} + L_{cm}\frac{di_g}{dt} + R_{loop\_off} i_d \\
0 &= R_{eq} i_g + v_{gs} + \left(L_{geq} + L_{cm}\right)\frac{di_g}{dt} + L_{cm}\frac{di_d}{dt} \\
i_g &= C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
i_{ch} &= 0, v_{diode} = 0.
\end{aligned}
\tag{C-15}
$$

where R_{loop_off} is the damping resistance of parasitic inductances.

This stage ends when ringing is fully damped.

The equations for Stage I – Stage IV can be solved by command ode45 in MATLAB, which requires equations to be written in the form of y′ = f(t, y), as shown in (C-16)-(C-20).

Stage I:

$$\begin{aligned}
\frac{di_{ch}}{dt} &= 0 \\
\frac{dv_{gs}}{dt} &= \frac{1}{C_{iss}} i_g \\
\frac{di_d}{dt} &= 0 \\
\frac{dv_{ds}}{dt} &= 0 \\
\frac{dv_{diode}}{dt} &= 0 \\
\frac{di_g}{dt} &= -\frac{1}{L_{gate}} v_{gs} - \frac{R_{eq}}{L_{gate}} i_g
\end{aligned} \tag{C-16}$$

Stage II:

$$\begin{aligned}
\frac{di_{ch}}{dt} &= -\frac{2C_{gd} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{2C_{gd} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{2C_{oss} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
\frac{dv_{gs}}{dt} &= -\frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{oss}}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
\frac{di_d}{dt} &= \frac{L_{gate}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{diode} + \frac{R_{eq}L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} i_g \\
\frac{dv_{ds}}{dt} &= -\frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
\frac{dv_{diode}}{dt} &= -\frac{I_{in}}{C_J} + \frac{1}{0.5C_J} i_d \\
\frac{di_g}{dt} &= \frac{-L_{cm}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} - \frac{L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{diode} - \frac{R_{eq}L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} i_g
\end{aligned} \tag{C-17}$$

Stage III(a):

$$\begin{aligned}
\frac{di_{ch}}{dt} &= -\frac{2C_{gd} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{2C_{gd} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{2C_{oss} g_{fs}\left(v_{gs} - V_{th}\right)}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
\frac{dv_{gs}}{dt} &= -\frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{oss}}{C_{iss}C_{oss} - C_{gd}^2} i_g \\
\frac{di_d}{dt} &= \frac{L_{gate}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} + \frac{R_{eq}L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} i_g
\end{aligned} \tag{C-18}$$

$$\frac{dv_{ds}}{dt} = -\frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_{ch} + \frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_g$$

$$\frac{dv_{diode}}{dt} = 0$$

$$\frac{di_g}{dt} = \frac{-L_{cm}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} - \frac{L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} - \frac{R_{eq}L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} i_g$$

Stage III(b):

$$\frac{di_{ch}}{dt} = 0$$

$$\frac{dv_{gs}}{dt} = \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{oss}}{C_{iss}C_{oss} - C_{gd}^2} i_g$$

$$\frac{di_d}{dt} = \frac{L_{gate}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{diode} + \frac{R_{eq}L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} i_g \quad \text{(C-19)}$$

$$\frac{dv_{ds}}{dt} = \frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_g$$

$$\frac{dv_{diode}}{dt} = -\frac{I_{in}}{C_J} + \frac{1}{0.5C_J} i_d$$

$$\frac{di_g}{dt} = -\frac{L_{cm}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} - \frac{L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{diode} - \frac{R_{eq}L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} i_g$$

Stage IV:

$$\frac{di_{ch}}{dt} = 0$$

$$\frac{dv_{gs}}{dt} = \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{oss}}{C_{iss}C_{oss} - C_{gd}^2} i_g$$

$$\frac{di_d}{dt} = \frac{L_{gate}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} - \frac{R_{loop\_off}L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} i_d - \frac{L_{gate}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} + \frac{R_{eq}L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} i_g \quad \text{(C-20)}$$

$$\frac{dv_{ds}}{dt} = \frac{C_{iss}}{C_{iss}C_{oss} - C_{gd}^2} i_d + \frac{C_{gd}}{C_{iss}C_{oss} - C_{gd}^2} i_g$$

$$\frac{dv_{diode}}{dt} = 0$$

$$\frac{di_g}{dt} = \frac{-L_{cm}V_{in}}{L_{gate}L_{loop} - L_{cm}^2} - \frac{L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} v_{gs} + \frac{R_{loop\_off}L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} i_d + \frac{L_{cm}}{L_{gate}L_{loop} - L_{cm}^2} v_{ds} - \frac{R_{eq}L_{loop}}{L_{gate}L_{loop} - L_{cm}^2} i_g$$

where $L_{gate} = L_{geq} + L_{cm}, L_{loop} = L_{cm} + L_{peq}, C_{iss} = C_{gs} + C_{gd}, C_{oss} = C_{ds} + C_{gd}$.

Appendix D Matlab Code for Calculation of Switching Energy

D.1 Matlab Code for Turn-On Transient

```
%-------------------------------------------------------------------------%
%///////////////// analytical model for mismatched MOSFETs ////////////////%
%-------------------------------------------------------------------------%
%                   1.difference of turn-on energies                      %
%                   2.average of turn-on energies                         %
%                   3.switching waveforms of single switch                %
%                   4.waveforms of variable difference                    %
%                   5.MOSFET model verification: cap and transfer         %
%-------------------------------------------------------------------------%


function switching_loss_turn_on

%-------------------------------------------------------------------------%
%                    parameters and operating conditions                  %
%----------------- same gfs, different Vth for 3 MOSFETs -----------------%
%-------------------------------------------------------------------------%
% unit
p=1*10^-12; % unit
n=1*10^-9; % unit

% balancing solution
L_k=1.85*n;
R_k=4;
L_s=(36.1+4.19)*n;
M_s=29.9*n;

%R_k=0;
%L_s=4.19*n;
%M_s=0;

% operating conditions
V_in=600;
I_in=20;
R_g=10.1;
R_int=6.5;
R_eq=2*R_g+R_k+R_int+1.6; % Rint considered; Req=2Rg+Rk+Rint
                          % impedance of gate driver is 0.8

V_GH=20; % gate high voltage
```

```
% parasitics
L_cm=4.1*n;
%L_cm=0;
L_p=18.2*n;
L_d=21.39*n;
L_gate=60*n+L_cm+40*n; % Lgate=Lgeq+Lcm; Lgeq=2Lg+Lkg;
L_loop=2*L_p+L_d+L_s-M_s+L_cm+6*n+2*n; % Lloop=Lpeq+Lcm; Lpeq=2Lp+Ld+Ls-Ms
R_loop_on=2; % 20A
% transfer characteristics
g_fs=0.57; % equivalent transconductance
V_th=4.25; % averaged Vth
delta_V_th=-1.1; % delta vth
%delta_V_th=-2;

%-------------------------------------------------------------------------%
%                 curve fitting of C_gd, C_ds, and C_J                    %
%                              Unit: pF                                   %
%-------------------------------------------------------------------------%
%---------------  data:   denote the data from measurement -------------%
%---------------  C_gs:   C_gs=520pF                       -------------%
%---------------  C_gd:   function of C_gd --> C_gd(x)     -------------%
%---------------  C_ds:   function of C_ds --> C_ds(x)     -------------%
%---------------  C_J:    function of C_J --> C_J(x)       -------------%
%-------------------------------------------------------------------------%

C_gs=520*10^-12; % Cgs=520pF

% read data
filename='capacitance';

xlrange1='BD6:BD46'; % Voltage of CJ
xlrange2='BP6:BP46'; % CJ

xlrange3='A6:A256'; % Voltage of Crss
xlrange4='AN6:AN256'; % Crss

xlrange5='A6:A256'; % Voltage of Cds
xlrange6='AM6:AM256'; % Cds


DataCap_J_V=xlsread(filename,xlrange1); % Voltage of CJ
DataCap_J=xlsread(filename,xlrange2); % CJ

DataCap_rss_V=xlsread(filename,xlrange3); % Voltage of Crss
DataCap_rss=xlsread(filename,xlrange4); % Crss

DataCap_ds_V=xlsread(filename,xlrange5); % Voltage of Cds
DataCap_ds=xlsread(filename,xlrange6); % Cds

% Curve fitting:
% Cgs is 520pF;
    C_J=fit(DataCap_J_V,DataCap_J,'gauss8'); % extract FUNCTION of C_J
    C_gd=fit(DataCap_rss_V,DataCap_rss,'gauss8'); % extract FUNCTION of C_gd
    C_ds=fit(DataCap_ds_V,DataCap_ds,'gauss8'); % extract FUNCTION of C_ds
```

```
%-------------------------------------------------------------------------%
%                      solving equations of single switch                 %
%-------------------------------------------------------------------------%
%---------------------- time:   vector of time      --------------------%
%---------------------- var:    matrix of variables --------------------%
%---------------------- t_step: time step           --------------------%
%---------------------- m_1:    index for stageI    --------------------%
%---------------------- m_2:    index for stageII&stageIII -------------%
%---------------------- m_3:    index for stageIV   --------------------%
%-------------------------------------------------------------------------%

t_step=100*p; % time step 100 ps-->can be changed based on speed and accuracy

% define time interval for the first iteration
t_ini=0; % initial time
t_end=t_step; % end time
t_extend=t_end+t_step; % dummy time for ode45
        % x1  x2  x3 x4  x5     x6
        % ich vgs id vds vdiode ig
var_ini=[0 0 0 V_in 0 0]; % initial values of turn-on transition
m_1=1; % index
var(m_1,:)=var_ini; % solution register
time(m_1)=t_ini; % time register
%-------------------------------------------------------------------------%
%                             solving stageI                              %
%-------------------------------------------------------------------------%
while var(m_1,2)<V_th % period ends condition
    [T,X]=ode45(@stageI,[t_ini t_end t_extend],var_ini); % solve one point
    % update index and initial values
    m_1=m_1+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_1,:)=var_ini;
    time(m_1)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end
%-------------------------------------------------------------------------%
%                            solving stageII                              %
%-------------------------------------------------------------------------%
m_2=m_1;
while var(m_2,3)<0.5*I_in % period ends condition
    [T,X]=ode45(@stageII,[t_ini t_end t_extend],var_ini); % solve one point
    % update index and initial values
    m_2=m_2+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_2,:)=var_ini;
    time(m_2)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
```

```
end
%-------------------------------------------------------------------------%
%                           solving stageIII                              %
%-------------------------------------------------------------------------%
while var(m_2,4)>6 % period ends condition; vds=0 is more accurate
    [T,X]=ode45(@stageIII,[t_ini t_end t_extend],var_ini);% solve one point
    % update index and initial values
    m_2=m_2+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_2,:)=var_ini;
    time(m_2)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end
%-------------------------------------------------------------------------%
%                           solving stageIV                               %
%-------------------------------------------------------------------------%
%-------------------------- linear region --------------------------------%
%-------------------------------------------------------------------------%
m_3=m_2;
var_ini=var_ini(2:6);
while t_end<100*n % total time is set to 100ns
    [T,X]=ode45(@stageIV,[t_ini t_end t_extend],var_ini);% solve one point
    % update index and initial values
    m_3=m_3+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_3,:)=[var_ini(2),var_ini(1:5)];
    time(m_3)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end

% extract waveforms
i_ch=var(:,1);
v_gs=var(:,2);
i_d=var(:,3);
v_ds=var(:,4);
power=i_ch.*v_ds;
%-------------------------------------------------------------------------%



%-------------------------------------------------------------------------%
%                         average of turn-on energy                       %
%-------------------------------------------------------------------------%
%---------------------- E_on: turn-on switching loss ---------------------%
%------------ vds goes to zero; no need to consider ringing ------------%
%-------------------------------- unit: J --------------------------------%
%-------------------------------------------------------------------------%
E_on=trapz(time(1:m_2),power(1:m_2)); % stage I to III
```

```
%-------------------------------------------------------------------------%
%                       difference of turn-on energy                      %
%-------------------------------------------------------------------------%
%------------------------ delta_ich solved by ode ------------------------%
%----------- delta_vgs and delta_vds solved by algebraic relation -------%
%-------------------- calculation performed before linear ----------------%
%-------------------------------- unit: J --------------------------------%
%-------------------------------------------------------------------------%

num=1;
% variable difference is zero during index=1:m_1 (stageI: delay period)
while num<m_1
    var_diff(num,:)=[0 0];
    time_diff(num)=time(num);
    num=num+1;
end

dex=m_1; % initial is the last point of stageI
% time interval for one point
t_ini=time(m_1); % initial time
t_end=t_ini+t_step; % end time
t_extend=t_end+t_step; % dummy time for ode45

            % x1         x2
            % delta_i_ch delta_i_s
var_diff_ini=[0 0];
var_diff(dex,:)=var_diff_ini; % variable register
time_diff(dex)=t_ini; % time register
while m_1-1<dex && dex<m_2 % cover stageII and stageIII
    [T,X]=ode45(@(t,x) func_diff_ich(t,x,v_gs(dex)),...
        [t_ini t_end t_extend],var_diff_ini);% solve one point
    %update index and initial values
    dex=dex+1;
    var_diff_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var_diff(dex,:)=var_diff_ini;
    time_diff(dex)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end

% extract delta_ich
delta_i_ch=var_diff(:,1);
i_pk=max(delta_i_ch);
% during stageI delta=0; num=m_1
delta_v_gs(1:num)=zeros(num,1);
delta_v_ds(1:num)=zeros(num,1);
delta_power(1:num)=zeros(num,1);
```

```
% calculation of delta_vgs, delta_vds, and delta_power during stageII & III
num=num+1;
while num<dex+1
    delta_v_gs(num)=delta_i_ch(num)/(2*g_fs*(v_gs(num)-V_th))+delta_V_th;
    delta_v_ds(num)=delta_v_gs(num)-L_d*(delta_i_ch(num)...
        -delta_i_ch(num-1))/t_step;
    delta_power(num)=v_ds(num)*delta_i_ch(num)+delta_v_ds(num)*i_ch(num);
    num=num+1;
end

delta_E_on=trapz(time_diff,delta_power);



%-------------------------------------------------------------------------%
%                  describing equations for each stage                    %
%-------------------------------------------------------------------------%
%---------------------------- x1 --> ich    ------------------------------%
%---------------------------- x2 --> vgs    ------------------------------%
%---------------------------- x3 --> id     ------------------------------%
%---------------------------- x4 --> vds    ------------------------------%
%---------------------------- x5 --> vdiode ------------------------------%
%---------------------------- x6 --> ig     ------------------------------%
%-------------------------------------------------------------------------%


%-------------------------------------------------------------------------%
%                         equations of stageI                             %
%-------------------------------------------------------------------------%
    % stage I: delay period
    function dxdt=stageI(t,x)
        dxdt=zeros(6,1); % a column vector

        dxdt(1)=0;
        dxdt(2)=x(6)/(C_gs+C_gd(x(4)-x(2))*p);
        dxdt(3)=0;
        dxdt(4)=0;
        dxdt(5)=0;
        dxdt(6)=V_GH/L_gate-1/L_gate*x(2)-R_eq/L_gate*x(6);
    end
%-------------------------------------------------------------------------%
%                         equations of stageII                            %
%-------------------------------------------------------------------------%
    % stage II: current rising period
    function dxdt=stageII(t,x)
        dxdt=zeros(6,1); % a column vector

        C_g=C_gd(x(4)-x(2))*p+1.5*p+6*p; % simplified notation of C_gd
        C_iss=C_g+C_gs;
        C_oss=C_g+C_ds(x(4))*p;
        den1=C_iss*C_oss-C_g^2; % denominator type 1
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=-2*C_g*g_fs*(x(2)-V_th)/den1*x(1)+...
            2*C_g*g_fs*(x(2)-V_th)/den1*x(3)...
```

```
            +2*C_oss*g_fs*(x(2)-V_th)/den1*x(6);
        dxdt(2)=-C_g/den1*x(1)+C_g/den1*x(3)+C_oss/den1*x(6);
        dxdt(3)=(L_gate*V_in-L_cm*V_GH)/den2+L_cm/den2*x(2)...
            -L_gate/den2*x(4)+R_eq*L_cm/den2*x(6);
        dxdt(4)=-C_iss/den1*x(1)+C_iss/den1*x(3)+C_g/den1*x(6);
        dxdt(5)=0;
        dxdt(6)=(L_loop*V_GH-L_cm*V_in)/den2-L_loop/den2*x(2)...
            +L_cm/den2*x(4)-(R_eq)*L_loop/den2*x(6);
    end
%-------------------------------------------------------------------------%
%                         equations of stageIII                           %
%-------------------------------------------------------------------------%
    % stage III: voltage falling period
    function dxdt=stageIII(t,x)
        dxdt=zeros(6,1); % a column vector

        C_g=C_gd(x(4)-x(2))*p+1.5*p+1*p; % simplified notation of C_gd

        C_iss=C_g+C_gs;
        C_oss=C_g+C_ds(x(4))*p;
        C_diode=C_J(x(5))*p; % simplified notation of C_J
        den1=C_iss*C_oss-C_g^2; % denominator type 1
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=-2*C_g*g_fs*(x(2)-V_th)/den1*x(1)...
            +2*C_g*g_fs*(x(2)-V_th)/den1*x(3)...
            +2*C_oss*g_fs*(x(2)-V_th)/den1*x(6);
        dxdt(2)=-C_g/den1*x(1)+C_g/den1*x(3)+C_oss/den1*x(6);
        dxdt(3)=(L_gate*V_in-L_cm*V_GH)/den2+L_cm/den2*x(2)...
            -L_gate/den2*x(4)-L_gate/den2*x(5)+R_eq*L_cm/den2*x(6);
        dxdt(4)=-C_iss/den1*x(1)+C_iss/den1*x(3)+C_g/den1*x(6);
        dxdt(5)=-I_in/C_diode+1/(0.5*C_diode)*x(3);
        dxdt(6)=(L_loop*V_GH-L_cm*V_in)/den2-L_loop/den2*x(2)...
            +L_cm/den2*x(4)+L_cm/den2*x(5)-R_eq*L_loop/den2*x(6);
    end
%-------------------------------------------------------------------------%
%                         equations of stageIV                            %
%-------------------------------------------------------------------------%
    % stage IV: ringing period
    function dxdt=stageIV(t,x)
        dxdt=zeros(5,1); % a column vector

        C_g=C_gd(x(3)-x(1))*p+1.5*p+1*p; % simplified notation of C_gd; avoid
vgd<0.
        C_iss=C_g+C_gs;
        C_diode=C_J(x(4))*p; % simplified notation of C_J
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=1/C_iss*x(5);
        dxdt(2)=(L_gate*V_in-L_cm*V_GH)/den2+L_cm/den2*x(1)...
            -R_loop_on*L_gate/den2*x(2)-L_gate/den2*x(4)...
            +R_eq*L_cm/den2*x(5);
        dxdt(3)=0;
        dxdt(4)=-I_in/C_diode+1/(0.5*C_diode)*x(2);
        dxdt(5)=(L_loop*V_GH-L_cm*V_in)/den2-L_loop/den2*x(1)...
            +R_loop_on*L_cm/den2*x(2)+L_cm/den2*x(4)-R_eq*L_loop/den2*x(5);
```

```
    end


%-------------------------------------------------------------------------%
%               describing equations for variable difference              %
%-------------------------------------------------------------------------%
%--------------------------- x1 --> delta_ich ----------------------------%
%--------------------------- x2 --> delta_is  ----------------------------%
%-------------------------------------------------------------------------%
function dxdt=func_diff_ich(t,x,v_point) % v_point is v_gs value

    dxdt=zeros(2,1);

    den1=(L_s+M_s)*L_k+(L_s+M_s+L_k)*L_cm;
    dxdt(1)=-(L_s+M_s+L_k)/den1*delta_V_th...
        -((L_s+M_s+L_k)/(2*g_fs*(v_point-V_th))+(L_s+M_s)*R_k)/den1*x(1)...
        +R_k*(L_s+M_s)/den1*x(2);
    dxdt(2)=-L_k/den1*delta_V_th...
        -(L_k/(2*g_fs*(v_point-V_th))-R_k*L_cm)/den1*x(1)...
        -R_k*L_cm/den1*x(2);
end
%-------------------------------------------------------------------------%
%                                pop up menu                              %
%-------------------------------------------------------------------------%
i=0;
while i<5
% pop up main menu
i=input(['Please enter the number:',...
    '\n1.difference of turn-on energies',...
    '\n2.average of turn-on energies',...
    '\n3.switching waveforms of single switch',...
    '\n4.waveforms of variable difference',...
    '\n5.MOSFET model verification: cap and transfer',...
    '\n6.exit\n\n']);

if i==1,
    delta_E_on
end

if i==2,
    E_on
end

if i==3,
%-------------------------------------------------------------------------%
%                   plotting waveforms of single switch                   %
%-------------------------------------------------------------------------%
%------------------------ i_d:   drain current        -------------------%
%------------------------ v_ds:  drain-source voltage -------------------%
%------------------------ i_ch:  channel current      -------------------%
%------------------------ v_gs:  gate-source voltage  -------------------%
%------------------------ power: instantaneous power  -------------------%
%------------------------ time:  ns                   -------------------%
%--------- vgs won't match because of channel length modulation ---------%
```

```
%-------------------------------------------------------------------------%

figure('position',[0,0,1000,1000])

% id
subplot(3,2,1)
plot(time/n,i_d,'k','linewidth',1); grid on;
xlabel('time (ns)');
ylabel('Drain Current, i_d (A)');
axis([0 80 0 25])

% vds
subplot(3,2,2)
plot(time/n,v_ds,'k','linewidth',1); grid on;
xlabel('time (ns)');
ylabel('Drain-Source Voltage, v_d_s (V)');
axis([0 80 -100 700])

% ich
subplot(3,2,3)
plot(time/n,i_ch,'k','linewidth',1); grid on;
xlabel('time (ns)');
ylabel('Channel Current, i_c_h (A)');

% vgs
subplot(3,2,4)
plot(time/n,v_gs,'k','linewidth',1); grid on;
xlabel('time (ns)');
ylabel('Gate-Source Voltage, v_g_s (V)');

% power
subplot(3,2,5)
plot(time/n,power,'k','linewidth',2); grid on;
xlabel('time (ns)');
ylabel('Power Loss, p (W)');

end

if i==4,
%-------------------------------------------------------------------------%
%                  plotting waveforms variable difference                 %
%-------------------------------------------------------------------------%
%----------------- delta_i_ch:  channel current diff.      --------------%
%----------------- delta_v_gs:  gate-source voltage diff.  --------------%
%----------------- delta_v_ds:  drain-source voltage diff. --------------%
%----------------- delta_power: power loss diff.           --------------%
%----------------- time:  ns                               --------------%
%-------------------------------------------------------------------------%

figure('position',[0,0,1800,1000])

% delta_ich
subplot(2,2,1)
plot(time_diff/n,delta_i_ch,'linewidth',2);
xlabel('time (ns)')
```

```
ylabel('\Deltai_c_h (A)');

% delta_vgs
subplot(2,2,2)
plot(time_diff/n,delta_v_gs,'linewidth',2);
xlabel('time (ns)')
ylabel('\Deltav_g_s (V)');

%delta_vds
subplot(2,2,3)
plot(time_diff/n,delta_v_ds,'linewidth',2);
xlabel('time (ns)')
ylabel('\Deltav_d_s (V)');

%delta_power
subplot(2,2,4)
plot(time_diff/n,delta_power,'linewidth',2);
xlabel('time (ns)')
ylabel('\Deltap (W)');

end

if i==5
%-------------------------------------------------------------------------%
%                  MOSFET model verification: cap and transfer             %
%-------------------------------------------------------------------------%
%-------------------- C_rss: reverse transfer capacitance ---------------%
%-------------------- C_oss: output capacitance           ---------------%
%-------------------- C_iss: input capacitance            ---------------%
%-------------------- C_J: diode junction capacitance     ---------------%
%-------------------- transfer characteristic             ---------------%
%-------------------------------------------------------------------------%

% cap model verification

xlrange7='A6:A256'; % Voltage of Coss
xlrange8='AL6:AL256'; % Coss

xlrange9='A6:A256'; %voltage of Ciss
xlrange10='AP6:AP256'; %voltage of Ciss

DataCap_oss_V=xlsread(filename,xlrange7); % Voltage of Coss
DataCap_oss=xlsread(filename,xlrange8); % Coss

DataCap_iss_V=xlsread(filename,xlrange9); % Voltage of Ciss
DataCap_iss=xlsread(filename,xlrange10); % Ciss

figure('position',[0,0,800,700])
% linear scale can make the matching look better
% if the voltage spike<1kV, the voltage range can be smaller--> better
% matching

volt=(-10:0.1:1000)';
% C_rss
```

```
subplot(2,2,1)
semilogy(DataCap_rss_V,DataCap_rss,'b',volt,C_gd(volt),'r','linewidth',2); %
dash line
legend('data','fitted curve'); title('C_r_s_s'); grid on% is also good

% C_oss
subplot(2,2,2)
semilogy(DataCap_oss_V,DataCap_oss,'b',volt,C_ds(volt)+C_gd(volt),'r','linewi
dth',2);
legend('data','fitted curve'); title('C_o_s_s'); grid on

% C_iss
subplot(2,2,3)
Cap_iss=520+C_gd(volt);
semilogy(DataCap_iss_V,DataCap_iss,'b',volt,Cap_iss,'r','linewidth',2);
legend('data','fitted curve'); title('C_i_s_s'); grid on

% C_J
subplot(2,2,4)
semilogx(DataCap_J_V,DataCap_J,'b',volt,C_J(volt),'r','linewidth',2);
legend('data','fitted curve'); title('C_J'); grid on

% transfer curve
figure
% read data
filename2='Matched transfer characteristics';
rangexdata='A4:A105'; % range of vgs
rangeydata='B4:B105'; % range of ids

xdata=xlsread(filename2,rangexdata); % vgs
ydata=xlsread(filename2,rangeydata); % ids

v=3.5:0.05:11;
i=g_fs*(v-V_th).^2*(1+lamda*20);% gfs(vgs-vth)^2*(1+lamda*vds). Valid when
vgs>vth.
plot(xdata,ydata,'b',v,i,':k','LineWidth',2)

% figure property
hleg=legend('Measurement','Model');
set(hleg,'Location','NorthWest');
title('Transfer Characteristic')
xlabel('Gate-Source Voltage, V_G_S (V)');
ylabel('Drain-Source Current, I_D_S (A)');
set(gca,'xlim',[3 11],'Xtick',(3:2:11),'ylim',[0 20]);grid on

end
end
return

end
```

D.2 Matlab Code for Turn-Off Transient

```
%-------------------------------------------------------------------------%
%///////////////// analytical model for mismatched MOSFETs ////////////////%
%-------------------------------------------------------------------------%
%                   1.difference of turn-off energies                     %
%                   2.average of turn-off energies                        %
%                   3.switching waveforms of single switch                %
%                   4.waveforms of variable difference                    %
%                   5.MOSFET model verification: cap and transfer         %
%-------------------------------------------------------------------------%


function switching_loss_turn_off

%-------------------------------------------------------------------------%
%                    parameters and operating conditions                  %
%----------------- same gfs, different Vth for 3 MOSFETs -----------------%
%-------------------------------------------------------------------------%
% unit
p=1*10^-12; % unit
n=1*10^-9; % unit

% balancing solution
L_k=1.85*n;
R_k=4;
L_s=(36.1+4.19)*n;
M_s=29.9*n;

%R_k=0;
%L_s=4.19*n;
%M_s=0;

% operating conditions
V_in=600;
I_in=20;
R_g=10.1;
R_int=6.5;
R_eq=2*R_g+R_k+R_int+1.6; % Rint considered; Req=2Rg+Rk+Rint
                          % impedance of gate driver is 0.8

V_GH=20; % gate high voltage

% parasitics
L_cm=4.1*n;
%L_cm=0;
L_p=18.2*n;
L_d=21.39*n;
L_gate=60*n+L_cm+40*n; % Lgate=Lgeq+Lcm; Lgeq=2Lg+Lkg;
L_loop=2*L_p+L_d+L_s-M_s+L_cm+6*n+2*n; % Lloop=Lpeq+Lcm; Lpeq=2Lp+Ld+Ls-Ms
R_loop_off=4; % damping resistance during ringing period (tuned value)

% transfer characteristics
g_fs=0.57; % equivalent transconductance
```

```
V_th=4.25; % averaged Vth
delta_V_th=-1.1; % delta vth
%delta_V_th=-2;

%-------------------------------------------------------------------------%
%                  curve fitting of C_gd, C_ds, and C_J                   %
%                               Unit: pF                                  %
%-------------------------------------------------------------------------%
%---------------  data:   denote the data from measurement -------------%
%---------------  C_gs:   C_gs=520pF                       -------------%
%---------------  C_gd:   function of C_gd --> C_gd(x)     -------------%
%---------------  C_ds:   function of C_ds --> C_ds(x)     -------------%
%---------------  C_J:    function of C_J --> C_J(x)       -------------%
%-------------------------------------------------------------------------%

C_gs=520*10^-12; % Cgs=520pF

% read data
filename='capacitance';

xlrange1='BD6:BD46'; % Voltage of CJ
xlrange2='BP6:BP46'; % CJ

xlrange3='A6:A256'; % Voltage of Crss
xlrange4='AN6:AN256'; % Crss

xlrange5='A6:A256'; % Voltage of Cds
xlrange6='AM6:AM256'; % Cds

DataCap_J_V=xlsread(filename,xlrange1); % Voltage of CJ
DataCap_J=xlsread(filename,xlrange2); % CJ

DataCap_rss_V=xlsread(filename,xlrange3); % Voltage of Crss
DataCap_rss=xlsread(filename,xlrange4); % Crss

DataCap_ds_V=xlsread(filename,xlrange5); % Voltage of Cds
DataCap_ds=xlsread(filename,xlrange6); % Cds

% Curve fitting:
% Cgs is 520pF;
    C_J=fit(DataCap_J_V,DataCap_J,'gauss8'); % extract FUNCTION of C_J
    C_gd=fit(DataCap_rss_V,DataCap_rss,'gauss8'); % extract FUNCTION of C_gd
    C_ds=fit(DataCap_ds_V,DataCap_ds,'gauss8'); % extract FUNCTION of C_ds

%-------------------------------------------------------------------------%
%                     solving equations of single switch                  %
%-------------------------------------------------------------------------%
%----------------------- time:   vector of time      --------------------%
%----------------------- var:    matrix of variables --------------------%
%----------------------- t_step: time step           --------------------%
%----------------------- m_1:    index for stageI    --------------------%
%----------------------- m_2:    index for stageII&stageIII -------------%
%----------------------- m_3:    index for stageIV   --------------------%
%-------------------------------------------------------------------------%
```

```
t_step=100*p; % time step 100 ps-->can be changed based on speed and accuracy

% define time interval for the first iteration
t_ini=0; % initial time
t_end=t_step; % end time
t_extend=t_end+t_step; % dummy time for ode45
        % x1  x2  x3 x4  x5     x6
        % ich vgs id vds vdiode ig
var_ini=[0.5*I_in V_GH 0.5*I_in 0 V_in 0]; % initial values of turn-off
transition
m_1=1; % index
var(m_1,:)=var_ini; % solution register
time(m_1)=t_ini; % time register
%-------------------------------------------------------------------------%
%                             solving stageI                              %
%-------------------------------------------------------------------------%
%-------------------------- linear region --------------------------------%
%-------------------------------------------------------------------------%
while g_fs*(var(m_1,2)-V_th)^2>0.5*I_in % period ends condition
    [T,X]=ode45(@stageI,[t_ini t_end t_extend],var_ini); % solve one point
    % update index and initial values
    m_1=m_1+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_1,:)=var_ini;
    time(m_1)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end
%-------------------------------------------------------------------------%
%                            solving stageII                              %
%-------------------------------------------------------------------------%
m_2=m_1;
while var(m_2,5)>0 % period ends condition(a): v_diode=0.
    [T,X]=ode45(@stageII,[t_ini t_end t_extend],var_ini); % solve one point
    % update index and initial values
    m_2=m_2+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_2,:)=var_ini;
    time(m_2)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end


%-------------------------------------------------------------------------%
%                            solving stageIII                             %
%-------------------------------------------------------------------------%
%------------------------------- 2 cases ---------------------------------%
%-------------------------------------------------------------------------%
```

```
% case of stageIII(a)
if var(m_2,1)>0
    while var(m_2,2)>V_th % period ends condition: vgs=Vth, i.e.,ich=0.
    [T,X]=ode45(@stageIIIa,[t_ini t_end t_extend],var_ini);% solve one point
    % update index and initial values
    m_2=m_2+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_2,:)=var_ini;
    time(m_2)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
    end

% case of stageIII(b)
else
    % resolving stageII
    % reset initial conditions
    m_2=m_1;
    t_ini=time(m_1);
    t_end=t_ini+t_step;
    t_extend=t_end+t_step;
    var_ini=var(m_1,:);

    while var(m_2,2)>V_th % period ends condition(b): vgs=Vth, i.e.,ich=0.
    [T,X]=ode45(@stageII,[t_ini t_end t_extend],var_ini); % solve one point
    % update index and initial values
    m_2=m_2+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_2,:)=var_ini;
    time(m_2)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
    end

    while var(m_2,5)>0 % period ends condition(a): v_diode=0.
    [T,X]=ode45(@stageIIIb,[t_ini t_end t_extend],var_ini);% solve one point
    % update index and initial values
    m_2=m_2+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_2,:)=var_ini;
    time(m_2)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
    end
end
```

```
%-------------------------------------------------------------------------%
%                            solving stageIV                              %
%-------------------------------------------------------------------------%
m_3=m_2;
while t_end<120*n % total time is set to 120ns
    [T,X]=ode45(@stageIV,[t_ini t_end t_extend],var_ini);% solve one point
    % update index and initial values
    m_3=m_3+1;
    var_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var(m_3,:)=var_ini;
    time(m_3)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end

% extract waveforms
i_ch=var(:,1);
v_gs=var(:,2);
i_d=var(:,3);
v_ds=var(:,4);
power=i_ch.*v_ds;
%-------------------------------------------------------------------------%




%-------------------------------------------------------------------------%
%                          average of turn-off energy                     %
%-------------------------------------------------------------------------%
%---------------------- E_off: turn-off switching loss -------------------%
%--------------------------------- unit: J -------------------------------%
%-------------------------------------------------------------------------%
E_off=trapz(time(1:(m_2)),power(1:(m_2)));
% include stage I to III



%-------------------------------------------------------------------------%
%                        difference of turn-off energy                    %
%-------------------------------------------------------------------------%
%------------------------- delta_ich solved by ode -----------------------%
%----------- delta_vgs and delta_vds solved by algebraic relation --------%
%--------- calculation performed during stage II and stage III-----------%
%--------------------------------- unit: J -------------------------------%
%-------------------------------------------------------------------------%

num=1;
% variable difference is zero during index=1:m_1 (stageI: delay period)
while num<m_1
    var_diff(num,:)=[0 0];
    time_diff(num)=time(num);
```

```
    num=num+1;
end

dex=m_1; % initial is the last point of stageI
% time interval for one point
t_ini=time(m_1); % initial time
t_end=t_ini+t_step; % end time
t_extend=t_end+t_step; % dummy time for ode45

            % x1         x2
            % delta_i_ch delta_i_s
var_diff_ini=[0 0];
var_diff(dex,:)=var_diff_ini; % variable register
time_diff(dex)=t_ini; % time register
while m_1-1<dex && dex<m_2 % cover stageII and stageIII
    [T,X]=ode45(@(t,x) func_diff_ich(t,x,v_gs(dex)),...
        [t_ini t_end t_extend],var_diff_ini);% solve one point
    %update index and initial values
    dex=dex+1;
    var_diff_ini=X(2,:);
    t_ini=t_ini+t_step;
    % update registers
    var_diff(dex,:)=var_diff_ini;
    time_diff(dex)=t_ini;
    % update time to be solved the next iteration
    t_end=t_end+t_step;
    t_extend=t_extend+t_step;
end

% extract delta_ich
delta_i_ch=var_diff(:,1);
% during stageI delta=0; num=m_1
delta_v_gs(1:num)=zeros(num,1);
delta_v_ds(1:num)=zeros(num,1);
delta_power(1:num)=zeros(num,1);

% calculation of delta_vgs, delta_vds, and delta_power during stageII & III
num=num+1;
while num<dex+1 % num<m_2+1
    delta_v_gs(num)=delta_i_ch(num)/(2*g_fs*(v_gs(num)-V_th))+delta_V_th;
    delta_v_ds(num)=delta_v_gs(num)-L_d*(delta_i_ch(num)...
        -delta_i_ch(num-1))/t_step;
    if (2*i_ch(num)-delta_i_ch(num))/2>0
       delta_power(num)=v_ds(num)*delta_i_ch(num)+delta_v_ds(num)*i_ch(num);
    else
       %delta_power(num)=2*i_ch(num)*v_ds(num);
       delta_power(num)=2*i_ch(num)*v_ds(num);
    end
    num=num+1;
end

delta_E_off=trapz(time_diff,delta_power);
```

```
%-------------------------------------------------------------------------%
%                  describing equations for each stage                    %
%-------------------------------------------------------------------------%
%---------------------------- x1 --> ich    ------------------------------%
%---------------------------- x2 --> vgs    ------------------------------%
%---------------------------- x3 --> id     ------------------------------%
%---------------------------- x4 --> vds    ------------------------------%
%---------------------------- x5 --> vdiode ------------------------------%
%---------------------------- x6 --> ig     ------------------------------%
%-------------------------------------------------------------------------%


%-------------------------------------------------------------------------%
%                         equations of stageI                             %
%-------------------------------------------------------------------------%
%--------------------------- linear region -------------------------------%
%-------------------------------------------------------------------------%
    % stage I: delay period
    function dxdt=stageI(t,x)
        dxdt=zeros(6,1); % a column vector
        if x(4)>x(2)
            C_g=C_gd(x(4)-x(2))*p+2.5*p; % simplified notation of C_gd
        else
            C_g=C_gd(0)*p+2.5*p;
        end
        C_iss=C_g+C_gs;

        dxdt(1)=0;
        dxdt(2)=1/C_iss*x(6);
        dxdt(3)=0;
        dxdt(4)=0;
        dxdt(5)=0;
        dxdt(6)=-1/L_gate*x(2)-R_eq/L_gate*x(6);
    end
%-------------------------------------------------------------------------%
%                         equations of stageII                            %
%-------------------------------------------------------------------------%
    % stage II: voltage rising period
    function dxdt=stageII(t,x)
        dxdt=zeros(6,1); % a column vector
        if x(4)>x(2)
            C_g=C_gd(x(4)-x(2))*p+3*p; % simplified notation of C_gd
        else
            C_g=C_gd(0)*p+2.5*p;
        end
        if x(4)<400
             C_iss=C_g+C_gs+1.5*n; % 5 ohm
        else
             C_iss=C_g+C_gs;
        end
        C_oss=C_g+C_ds(x(4))*p;
        C_diode=C_J(x(5))*p; % simplified notation of C_J
        den1=C_iss*C_oss-C_g^2; % denominator type 1
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=-2*C_g*g_fs*(x(2)-V_th)/den1*x(1)...
```

```
            +2*C_g*g_fs*(x(2)-V_th)/den1*x(3)...
            +2*C_oss*g_fs*(x(2)-V_th)/den1*x(6);
        dxdt(2)=-C_g/den1*x(1)+C_g/den1*x(3)+C_oss/den1*x(6);
        dxdt(3)=(L_gate*V_in)/den2+L_cm/den2*x(2)...
            -L_gate/den2*x(4)-L_gate/den2*x(5)+R_eq*L_cm/den2*x(6);
        dxdt(4)=-C_iss/den1*x(1)+C_iss/den1*x(3)+C_g/den1*x(6);
        dxdt(5)=-I_in/C_diode+1/(0.5*C_diode)*x(3);
        dxdt(6)=(-L_cm*V_in)/den2-L_loop/den2*x(2)...
            +L_cm/den2*x(4)+L_cm/den2*x(5)-R_eq*L_loop/den2*x(6);
    end
%-------------------------------------------------------------------------%
%                    equations of stageIII (a) and (b)                    %
%-------------------------------------------------------------------------%
    % stage III(a): current falling period
    function dxdt=stageIIIa(t,x)
        dxdt=zeros(6,1); % a column vector
        if x(4)>x(2)
            C_g=C_gd(x(4)-x(2))*p-4*p; % simplified notation of C_gd 5 ohm
        else
            C_g=C_gd(0)*p;
        end
        C_iss=C_g+C_gs;
        C_oss=C_g+C_ds(x(4))*p+20*p; % 5ohm
        den1=C_iss*C_oss-C_g^2; % denominator type 1
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=-2*C_g*g_fs*(x(2)-V_th)/den1*x(1)+...
            2*C_g*g_fs*(x(2)-V_th)/den1*x(3)...
            +2*C_oss*g_fs*(x(2)-V_th)/den1*x(6);
        dxdt(2)=-C_g/den1*x(1)+C_g/den1*x(3)+C_oss/den1*x(6);
        dxdt(3)=(L_gate*V_in)/den2+L_cm/den2*x(2)...
            -L_gate/den2*x(4)+R_eq*L_cm/den2*x(6);
        dxdt(4)=-C_iss/den1*x(1)+C_iss/den1*x(3)+C_g/den1*x(6);
        dxdt(5)=0;
        dxdt(6)=(-L_cm*V_in)/den2-L_loop/den2*x(2)...
            +L_cm/den2*x(4)-R_eq*L_loop/den2*x(6);
    end

    % stage III(b): remaining voltage rising period
    function dxdt=stageIIIb(t,x)
        dxdt=zeros(6,1); % a column vector
        if x(4)>x(2)
            C_g=C_gd(x(4)-x(2))*p; % simplified notation of C_gd
        else
            C_g=C_gd(0)*p;
        end
        C_iss=C_g+C_gs;
        C_oss=C_g+C_ds(x(4))*p;
        C_diode=C_J(x(5))*p; % simplified notation of C_J
        den1=C_iss*C_oss-C_g^2; % denominator type 1
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=0;
        dxdt(2)=C_g/den1*x(3)+C_oss/den1*x(6);
        dxdt(3)=(L_gate*V_in)/den2+L_cm/den2*x(2)...
            -L_gate/den2*x(4)-L_gate/den2*x(5)+R_eq*L_cm/den2*x(6);
```

```
        dxdt(4)=C_iss/den1*x(3)+C_g/den1*x(6);
        dxdt(5)=-I_in/C_diode+1/(0.5*C_diode)*x(3);
        dxdt(6)=(-L_cm*V_in)/den2-L_loop/den2*x(2)...
            +L_cm/den2*x(4)+L_cm/den2*x(5)-R_eq*L_loop/den2*x(6);
    end
%-------------------------------------------------------------------------%
%                         equations of stageIV                            %
%-------------------------------------------------------------------------%
    % stage IV: ringing period
    function dxdt=stageIV(t,x)
        dxdt=zeros(6,1); % a column vector
        C_g=C_gd(x(4)-x(2))*p+10*p; % simplified notation of C_gd
        C_iss=C_g+C_gs;
        C_oss=C_g+C_ds(x(4))*p;
        den1=C_iss*C_oss-C_g^2; % denominator type 1
        den2=L_gate*L_loop-L_cm^2; % denominator type 2

        dxdt(1)=0;
        dxdt(2)=C_g/den1*x(3)+C_oss/den1*x(6);
        dxdt(3)=(L_gate*V_in)/den2+L_cm/den2*x(2)...
            -R_loop_off*L_gate/den2*x(3)-L_gate/den2*x(4)...
            +R_eq*L_cm/den2*x(6);
        dxdt(4)=C_iss/den1*x(3)+C_g/den1*x(6);
        dxdt(5)=0;
        dxdt(6)=(-L_cm*V_in)/den2-L_loop/den2*x(2)...
            +R_loop_off*L_cm/den2*x(3)+L_cm/den2*x(4)-R_eq*L_loop/den2*x(6);
    end



%-------------------------------------------------------------------------%
%               describing equations for variable difference              %
%-------------------------------------------------------------------------%
%--------------------------- x1 --> delta_ich ----------------------------%
%--------------------------- x2 --> delta_is  ----------------------------%
%-------------------------------------------------------------------------%
function dxdt=func_diff_ich(t,x,v_point) % v_point is v_gs value

    dxdt=zeros(2,1);

    den1=(L_s+M_s)*L_k+(L_s+M_s+L_k)*L_cm;
    dxdt(1)=-(L_s+M_s+L_k)/den1*delta_V_th...
        -((L_s+M_s+L_k)/(2*g_fs*(v_point-V_th))+(L_s+M_s)*R_k)/den1*x(1)...
        +R_k*(L_s+M_s)/den1*x(2);
    dxdt(2)=-L_k/den1*delta_V_th...
        -(L_k/(2*g_fs*(v_point-V_th))-R_k*L_cm)/den1*x(1)...
        -R_k*L_cm/den1*x(2);
end



%-------------------------------------------------------------------------%
%                               pop up menu                               %
%-------------------------------------------------------------------------%
i=0;
```

```
while i<5
% pop up main menu
i=input(['Please enter the number:',...
    '\n1.difference of turn-off energies',...
    '\n2.average of turn-off energies',...
    '\n3.switching waveforms of single switch',...
    '\n4.waveforms of variable difference',...
    '\n5.MOSFET model verification: cap and transfer',...
    '\n6.exit\n\n']);

if i==1,
    delta_E_off
end

if i==2,
    E_off
end

if i==3,
%-------------------------------------------------------------------------%
%                    plotting waveforms of single switch                  %
%-------------------------------------------------------------------------%
%------------------------- i_d:   drain current        ------------------%
%------------------------- v_ds:  drain-source voltage ------------------%
%------------------------- i_ch:  channel current      ------------------%
%------------------------- v_gs:  gate-source voltage  ------------------%
%------------------------- power: instantaneous power  ------------------%
%------------------------- time:  ns                   ------------------%
%-------------------------------------------------------------------------%

figure('position',[0,0,1110,265])

% id
subplot(3,2,1)
plot(time/n,i_d,'k','linewidth',1);grid on;
xlabel('time (ns)');
ylabel('Drain Current, i_d (A)');
axis([20 100 -5 20])


% vds
subplot(3,2,2)
plot(time/n,v_ds,'k','linewidth',1);grid on;
xlabel('time (ns)');
ylabel('Drain-Source Voltage, v_d_s (V)');
axis([20 100 -100 800])


% ich
subplot(3,2,3)
plot(time/n,i_ch,'linewidth',2);
xlabel('time (ns)');
ylabel('Channel Current, i_c_h (A)');
axis([20 120 -5 20])
```

```
% vgs
subplot(3,2,4)
plot(time/n,v_gs,'linewidth',2);
xlabel('time (ns)');
ylabel('Gate-Source Voltage, v_g_s (V)');

% power
subplot(3,2,5)
plot(time/n,power,'linewidth',2);
xlabel('time (ns)');
ylabel('Power Loss, p (W)');

end

if i==4,
%-------------------------------------------------------------------------%
%                     plotting waveforms variable difference               %
%-------------------------------------------------------------------------%
%----------------- delta_i_ch:  channel current diff.      --------------%
%----------------- delta_v_gs:  gate-source voltage diff.  --------------%
%----------------- delta_v_ds:  drain-source voltage diff. --------------%
%----------------- delta_power: power loss diff.           --------------%
%----------------- time:  ns                               --------------%
%-------------------------------------------------------------------------%

figure('position',[0,0,1400,600])

% delta_ich
subplot(2,2,1)
plot(time_diff/n,delta_i_ch,'linewidth',2);
xlabel('time (ns)');
ylabel('\Deltai_c_h (A)');

% delta_vgs
subplot(2,2,2)
plot(time_diff/n,delta_v_gs,'linewidth',2);
xlabel('time (ns)');
ylabel('\Deltav_g_s (V)');

%delta_vds
subplot(2,2,3)
plot(time_diff/n,delta_v_ds,'linewidth',2);
xlabel('time (ns)');
ylabel('\Deltav_d_s (V)');

%delta_power
subplot(2,2,4)
plot(time_diff/n,delta_power,'linewidth',2);
xlabel('time (ns)');
ylabel('\Deltap (W)');

end

if i==5
```

```
%-------------------------------------------------------------------------%
%                 MOSFET model verification: cap and transfer             %
%-------------------------------------------------------------------------%
%-------------------- C_rss: reverse transfer capacitance ---------------%
%-------------------- C_oss: output capacitance           ---------------%
%-------------------- C_iss: input capacitance            ---------------%
%-------------------- C_J: diode junction capacitance     ---------------%
%-------------------- transfer characteristic             ---------------%
%-------------------------------------------------------------------------%

% cap model verification

xlrange7='A6:A256'; % Voltage of Coss
xlrange8='AL6:AL256'; % Coss

xlrange9='A6:A256'; %voltage of Ciss
xlrange10='AP6:AP256'; %voltage of Ciss

DataCap_oss_V=xlsread(filename,xlrange7); % Voltage of Coss
DataCap_oss=xlsread(filename,xlrange8); % Coss

DataCap_iss_V=xlsread(filename,xlrange9); % Voltage of Ciss
DataCap_iss=xlsread(filename,xlrange10); % Ciss

figure('position',[0,0,800,700])
% linear scale can make the matching look better
% if the voltage spike<1kV, the voltage range can be smaller--> better
% matching

volt=(-10:0.1:1000)';
% C_rss
subplot(2,2,1)
semilogy(DataCap_rss_V,DataCap_rss,'b',volt,C_gd(volt),'r','linewidth',2); %
dash line
legend('data','fitted curve'); title('C_r_s_s'); grid on% is also good

% C_oss
subplot(2,2,2)
semilogy(DataCap_oss_V,DataCap_oss,'b',volt,C_ds(volt)+C_gd(volt),'r','linewi
dth',2);
legend('data','fitted curve'); title('C_o_s_s'); grid on

% C_iss
subplot(2,2,3)
Cap_iss=520+C_gd(volt);
semilogy(DataCap_iss_V,DataCap_iss,'b',volt,Cap_iss,'r','linewidth',2);
legend('data','fitted curve'); title('C_i_s_s'); grid on

% C_J
subplot(2,2,4)
semilogx(DataCap_J_V,DataCap_J,'b',volt,C_J(volt),'r','linewidth',2);
legend('data','fitted curve'); title('C_J'); grid on

% transfer curve
figure
```

```
% read data
filename2='Matched transfer characteristics';
rangexdata='A4:A105'; % range of vgs
rangeydata='B4:B105'; % range of ids

xdata=xlsread(filename2,rangexdata); % vgs
ydata=xlsread(filename2,rangeydata); % ids

v=3.5:0.05:11;
i=g_fs*(v-V_th).^2*(1+lamda*20);% gfs(vgs-vth)^2*(1+lamda*vds). Valid when
vgs>vth.
plot(xdata,ydata,'b',v,i,':k','LineWidth',2)

% figure property
hleg=legend('Measurement','Model');
set(hleg,'Location','NorthWest');
title('Transfer Characteristic')
xlabel('Gate-Source Voltage, V_G_S (V)');
ylabel('Drain-Source Current, I_D_S (A)');
set(gca,'xlim',[3 11],'Xtick',(3:2:11),'ylim',[0 20]);grid on

end
end
return

end
```

Appendix E Sensitivity Analysis

The balancing solution shown in Fig. 2-25 is analyzed as an example. Similar method can be applied to other structures.

Fig. E-1(a) shows the circuit with variation in drive-source resistance R_k.

According the design guideline shown in (2-49),

$$\frac{\partial \max\left|i_{ds1(pk)} - i_{ds2(pk)}\right|}{\partial R_k} = -\frac{\left|\Delta V_{th}\right|}{R_k^{\,2}} \tag{E-1}$$

Define $\Delta R_k = \alpha R_{k0}$. The variation of $\max|i_{ds1(pk)}\text{-}i_{ds2(pk)}|$ caused by ΔR_k is

$$\frac{\left.\frac{\partial \max\left|i_{ds1(pk)} - i_{ds2(pk)}\right|}{\partial R_k}\right|_{R_{k0}} \Delta R_k}{\max\left|i_{ds1(pk)} - i_{ds2(pk)}\right|_0} = \frac{\left.-\frac{\left|\Delta V_{th}\right|}{R_k^{\,2}}\right|_{R_{k0}} \alpha R_{k0}}{\frac{\left|\Delta V_{th}\right|}{R_{k0}} + \frac{\left|\Delta V_{th}\right|}{L_{s0} + M_{s0}} t_r} = \frac{-\alpha}{1 + \frac{R_{k0} t_r}{L_{s0} + M_{s0}}} \tag{E-2}$$

According to (E-2), the variation of R_k won't be amplified. For example, if $\max|i_{ds1(pk)}\text{-}i_{ds2(pk)}|$ = 0.5 A, the 10% variation in R_k will only cause less than 0.05 A difference in $\max|i_{ds1(pk)}\text{-}i_{ds2(pk)}|$. The current balancing solution is not sensitive to the variation of R_k. This is also demonstrated by simulation shown in Fig. E-2(a).

Similar analysis is applied to coupled L_s. Fig. E-1(b) shows the circuit with variation in coupled power-source inductance L_s.

According the design guideline shown in (2-49),

$$\frac{\partial \max\left|i_{ds1(pk)}-i_{ds2(pk)}\right|}{\partial\left(L_s+M_s\right)}=-\frac{\left|\Delta V_{th}\right|t_r}{\left(L_s+M_s\right)^2} \tag{E-3}$$

Define $\Delta\left(L_s+M_s\right)=\alpha\left(L_{s0}+M_{s0}\right)$. The variation of max|$i_{ds1(pk)}$-$i_{ds2(pk)}$| caused by ($\Delta L_s + \Delta M_s$) is

$$\frac{\left.\frac{\partial \max\left|i_{ds1(pk)}-i_{ds2(pk)}\right|}{\partial\left(L_s+M_s\right)}\right|_{L_{s0}+M_{s0}}\Delta\left(L_s+M_s\right)}{\max\left|i_{ds1(pk)}-i_{ds2(pk)}\right|_0}=\frac{-\left.\frac{\left|\Delta V_{th}\right|t_r}{\left(L_s+M_s\right)^2}\right|_{L_{s0}+M_{s0}}\alpha\left(L_{s0}+M_{s0}\right)}{\frac{\left|\Delta V_{th}\right|}{R_{k0}}+\frac{\left|\Delta V_{th}\right|}{L_{s0}+M_{s0}}t_r}=\frac{-\alpha}{1+\frac{L_{s0}+M_{s0}}{R_{k0}t_r}} \tag{E-4}$$

According to (E-4), the variation of ($L_s + M_s$) won't be amplified. For example, if max|$i_{ds1(pk)}$-$i_{ds2(pk)}$| = 0.5 A, the 10% variation in ($L_s + M_s$) will only cause less than 0.05 A difference in max|$i_{ds1(pk)}$-$i_{ds2(pk)}$|. The current balancing solution is not sensitive to the variation of ($L_s + M_s$). This is also demonstrated by simulation shown in Fig. E-2(b).

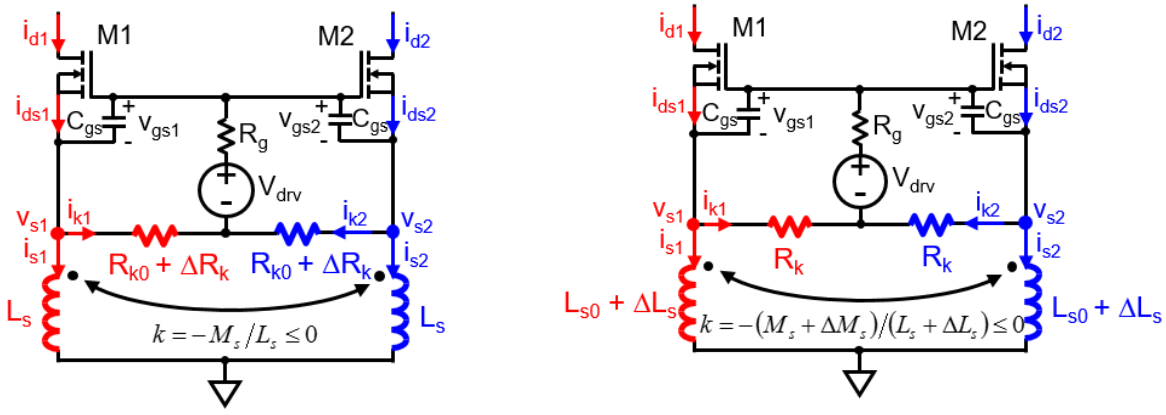


Fig. E-1. (a) Variation exists in drive-source resistance R_k. (b) Variation exists in coupled power-source inductance L_s.

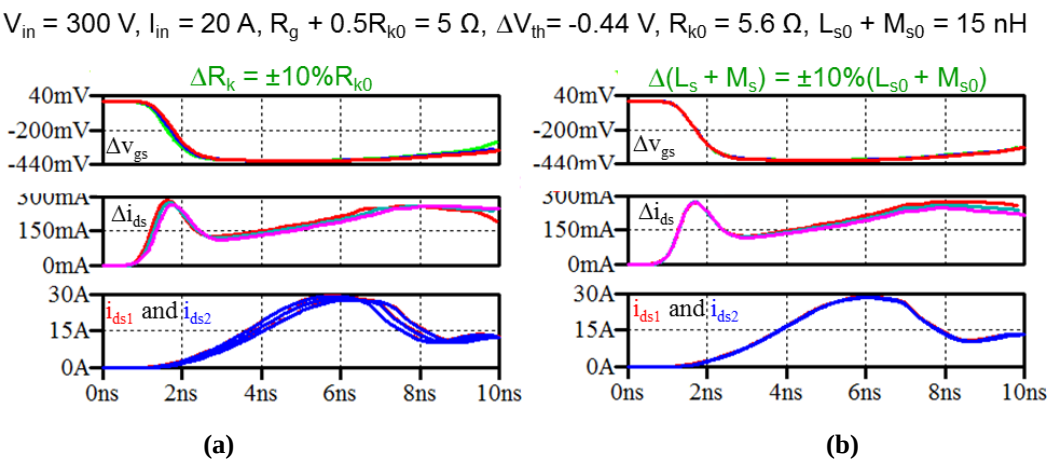


Fig. E-2. (a) Influence of variation in drive-source resistance R_k on current balancing effect. (b) Influence of variation in coupled power-source inductance L_s on current balancing effect.

Appendix F Directory of Raw Files

The original simulation files, Matlab code, Excel files, Mathcad files, test results, etc. in this dissertation can be found at the //ADFS directories as shown in Table A-5.

Table F-1. Directory of raw files

Figure or Table	Type	Directory (\\adfs\projects\Khai Ngo\yincanMao\Dissertation files\simulations\)
Fig. 1-7	LTspice	Fig. 1-7
Fig. 2-3	LTspice Excel	Fig. 2-3
Fig. 2-9	LTspice Excel	Fig. 2-9
Fig. 2-12	LTspice	Fig 2-12
Fig. 2-14	LTspice Excel	Fig. 2-14
Fig. 2-15	LTspice	Fig. 2-15
Fig. 2-17	LTspice Excel	Fig. 2-17
Fig. 2-18	LTspice	Fig. 2-18
Fig. 2-21	LTspice	Fig. 2-21
Fig. 2-26	LTspice	Fig. 2-26
Fig. 2-27	LTspice	Fig. 2-27
Fig. 2-28	LTspice	Fig. 2-28
Fig. 2-29	LTspice Excel	Fig. 2-29
Fig. 2-30	LTspice	Fig. 2-30
Fig. 2-33	LTspice	Fig. 2-33
Fig. 2-38	LTspice Excel	Fig. 2-38
Fig. 2-43	Mathcad	Fig. 2-42
Fig. 2-44	Excel	Fig. 2-44
Fig. 2-52	Mathcad TXT	Fig. 2-52
Fig. 2-53	Mathcad TXT	Fig. 2-53
Fig. 2-55	Mathcad	Fig. 2-55

	TXT	
Fig. 2-58	Mathcad TXT	Fig. 2-58
Fig. 2-62	Mathcad TXT	Fig. 2-62
Fig. 2-67	Mathcad TXT Excel	Fig. 2-67
Fig. 3-5	LTspice	Fig. 3-5
Fig. 3-6	Matlab	Fig. 3-6
Fig. 3-7	Ansys Q3D	Fig. 3-7
Fig. 4-5	Excel Matlab	Fig. 4-5
Fig. 4-9	LTspice	Fig. 4-9
Fig. 4-15	Excel	Fig. 4-15
Fig. 4-18	Excel	Fig. 4-18
Fig. 4-19	Excel	Fig. 4-19
Fig. 4-22	Excel	Fig. 4-22
Fig. 4-26	Excel	Fig. 4-26
Fig. 4-4, Fig. 4-15, Fig. 4-17, Fig. 4-18, Fig. 4-20, Fig. 4-23, Fig. 4-24, Fig. 4-26	Excel Matlab	Matlab for loss calculation
Fig. 2-35, Fig. 2-37, Fig. 2-54, Fig. 2-56, Fig. 2-59, Fig. 2-63, Fig. 2-71, Fig. 2-72, Fig. 2-78	Mathcad	Drawing of trajectories
All Figures and Tables in Chapter 2 related to Experiment	Mathcad TXT	Test data for Chapter 2
All Figures and Tables in Chapter 3 and Chapter 4 related to parasitic extraction	Ansys Q3D Excel	Extraction of parasitics of devices and layout
All Figures and Tables in Chapter 3 and Chapter 4 related to Experiment	Mathcad TXT Excel	Test results for Chapter 3&4

References

[1] A. Elasser, T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," in *Proc. of the IEEE*, vol. 90, no. 6, Jun. 2002, pp. 969-986.

[2] Rohm Semiconductor, "SiC Power Devices and modules," *Application Note*.

[3] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning and S. H. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," in *IEEE Trans. on Power Electron.*, vol. 22, no. 2, pp. 353-363, March 2007.

[4] Z. Chen, D. Boroyevich and J. Li, "Behavioral comparison of Si and SiC power MOSFETs for high-frequency applications," *Appl. Power Electron. Conf. and Expo. (APEC), 2013 Twenty-Eighth Annu. IEEE*, Long Beach, CA, USA, 2013, pp. 2453-2460.

[5] T. Matsukawa, H. Chikaraishi, Y. Sato and R. Shimada, "Basic study on conductive characteristics of SiC power device for its application to AC/DC converter," in *IEEE Trans. on Appl. Superconductivity*, vol. 14, no. 2, pp. 690-692, June 2004.

[6] J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," in *IEEE Trans. on Ind. Electron.*, vol. 58, no. 7, pp. 2872-2882, July 2011.

[7] K. Shenai, "Silicon carbide power converters for next generation aerospace electronics applications," *National Aerospace and Electron. Conf., 2000. NAECON 2000. Proc. of the IEEE 2000*, Dayton, OH, 2000, pp. 516-523.

[8] T. Funaki *et al*., "Power Convers. With SiC Devices at Extremely High Ambient Temperatures," in *IEEE Trans. on Power Electron.*, vol. 22, no. 4, pp. 1321-1329, July 2007.

[9] N. A. Riza, A. Arain and F. Perez, "Harsh environments minimally invasive optical sensor using free-space targeted single-crystal silicon carbide," in *IEEE Sensors Journal*, vol. 6, no. 3, pp. 672-685, June 2006.

[10] H. Zhang, L. M. Tolbert and B. Ozpineci, "Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles," in *IEEE Trans. on Industry Applications*, vol. 47, no. 2, pp. 912-921, March-April 2011.

[11] D. Han, J. Noppakunkajorn and B. Sarlioglu, "Comprehensive Efficiency, Weight, and Volume Comparison of SiC- and Si-Based Bidirectional DC–DC Converters for Hybrid

Electric Vehicles," in *IEEE Trans. on Vehicular Technology*, vol. 63, no. 7, pp. 3001-3010, Sept. 2014.

[12] Y. Hinata, M. Horio, Y. Ikeda, R. Yamada and Y. Takahashi, "Full SiC power module with advanced structure and its solar inverter application," *Appl. Power Electron. Conf. and Expo. (APEC), 2013 Twenty-Eighth Annu. IEEE*, Long Beach, CA, 2013, pp. 604-607.

[13] J. Jordan *et al*., "A Comparative Performance Study of a 1200 V Si and SiC MOSFET Intrinsic Diode on an Induction Heating Inverter," in *IEEE Trans. on Power Electron.*, vol. 29, no. 5, pp. 2550-2562, May 2014.

[14] CREE, *SiC MOSFETs*. [Online]. Available: https://www.wolfspeed.com/power/products/sic-mosfets

[15] J. Richmond, M. Das, S. Leslie, A. Agarwal, B. Hull and J. Palmour, "Roadmap for megawatt class power switch modules utilizing large area silicon carbide MOSFETs and JBS diodes," *Energy Convers. Congr. and Expo., 2009. ECCE 2009. IEEE*, San Jose, CA, 2009, pp. 106-111.

[16] P. Friedrichs, "Silicon carbide power devices - status and upcoming challenges," *Power Electron. and Applications, 2007 European Conf. on*, Aalborg, 2007, pp. 1-11.

[17] J. Rabkowski, D. Peftitsis, M. Zdanowski and H. P. Nee, "A 6kW, 200kHz boost converter with parallel-connected SiC bipolar transistors," *Appl. Power Electron. Conf. and Expo. (APEC), 2013 Twenty-Eighth Annu. IEEE*, Long Beach, CA, 2013, pp. 1991-1998.

[18] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy and H. P. Nee, "Challenges regarding parallel-connection of SiC JFETs," *Power Electron. and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conf. on*, Jeju, 2011, pp. 1095-1101.

[19] J. Fabre and P. Ladoux, "Parallel connection of SiC MOSFET modules for future use in traction converters," *2015 Int. Conf. on Elect. Syst. for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, Aachen, 2015, pp. 1-6.

[20] J. Fabre and P. Ladoux, "Parallel Connection of 1200-V/100-A SiC-MOSFET Half-Bridge Modules," in *IEEE Trans. on Ind. Applicat.*, vol. 52, no. 2, pp. 1669-1676, March-April 2016.

[21] R. A. Wood and T. E. Salem, "Evaluation of a 1200-V, 800-A All-SiC Dual Module," in *IEEE Trans. on Power Electron.*, vol. 26, no. 9, pp. 2504-2511, Sept. 2011.

[22] S. Musumeci, R. Pagano, A. Raciti, F. Frisina and M. Melito, “Parallel strings of IGBTs in short circuit transients: analysis of the parameter influence and experimental behavior,” *IECON 02 Ind. Electron. Society, IEEE 2002 28th Annu. Conf.*, 2002, pp. 555-560, vol. 1.

[23] Hua Yang, Wen Xuhui, Gu Lingyun, Wang Li and Zhao Feng, “Investigation of parallel connection of IGBTs,” *Electrical Machines and Systems, 2005. ICEMS 2005. Proc. of the Eighth International Conf. on*, 2005, pp. 833-835 Vol. 1.

[24] W. Gangyao, J. Mookken, J. Rice and M. Schupbach, “Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications,” *Appl. Power Electron. Conf. and Expo. (APEC), 2014 Twenty-Ninth Annu. IEEE*, Fort Worth, TX, 2014, pp. 1478-1483.

[25] R. Letor, “Static and dynamic behavior of paralleled IGBTs,” in *IEEE Trans. on Industry Applications*, vol. 28, no. 2, pp. 395-402, Mar/Apr 1992.

[26] H. Miyazaki, H. Fukumoto, S. Sugiyama, M. Tachikawa and N. Azusawa, “Neutral-point-clamped inverter with parallel driving of IGBTs for industrial applications,” in *IEEE Trans. on Ind. Applicat.*, vol. 36, no. 1, pp. 146-151, Jan/Feb 2000.

[27] SIEMENS, “Connecting IGBTs in Parallel,” *Application Note*.

[28] International Rectifier, “Paralleling of Power MOSFETs for Higher Power Output,” *Application Note*.

[29] Infineon, “Parallel Operation of Power MOSFETs,” *Application Note*.

[30] F. Chimento, A. Raciti, A. Cannone, S. Musumeci and A. Gaito, “Parallel connection of super-junction MOSFETs in a PFC application,” *Energy Convers. Congr. and Expo., 2009. ECCE 2009. IEEE*, San Jose, CA, 2009, pp. 3776-3783.

[31] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy and H. P. Nee, “Challenges regarding parallel-connection of SiC JFETs,” *Power Electron. and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conf. on*, Jeju, 2011, pp. 1095-1101.

[32] M. Chinthavali, P. Ning, Y. Cui and L. M. Tolbert, “Investigation on the parallel operation of discrete SiC BJTs and JFETs,” *Appl. Power Electron. Conf. and Expo. (APEC), 2011 Twenty-Sixth Annu. IEEE*, Fort Worth, TX, 2011, pp. 1076-1083.

[33] CREE, *C2M0160120D datasheet*. [Online]. Available: http://www.wolfspeed.com/media/downloads/169/C2M0160120D.pdf.

[34] Advanced Power Technology, “Parallel Connection of IGBT and MOSFET Power Modules,” *Application Note*.

[35] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock and F. Wang, “Active current balancing for parallel-connected silicon carbide MOSFETs,” *Energy Convers. Congr. and Expo. (ECCE), 2013 IEEE*, Denver, CO, 2013, pp. 1563-1569.

[36] Yang Xue, Junjie Lu, Zhiqiang Wang, L. M. Tolbert, B. J. Blalock and F. Wang, “Active compensation of current unbalance in paralleled silicon carbide MOSFETs,” *Appl. Power Electron. Conf. and Expo. (APEC), 2014 Twenty-Ninth Annu. IEEE*, Fort Worth, TX, 2014, pp. 1471-1477.

[37] A. Castellazzi, “Experimental characterization and modelling of high-voltage IGBT modules off-state thermal instability,” *Power Electron. and Applicat., 2009. EPE '09. 13th European Conf. on*, Barcelona, 2009, pp. 1-9.

[38] J. Hu, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran and P. A. Mawby, "The Effect of Electrothermal Nonuniformities on Parallel Connected SiC Power Devices Under Unclamped and Clamped Inductive Switching," in *IEEE Trans. on Power Electron.*, vol. 31, no. 6, pp. 4526-4535, June 2016.

[39] D. Bortis, J. Biela and J. W. Kolar, “Active Gate Control for Current Balancing of Parallel-Connected IGBT Modules in Solid-State Modulators,” in *IEEE Trans. on Plasma Science*, vol. 36, no. 5, pp. 2632-2637, Oct. 2008.

[40] T. Lopez and R. Elferich, “Static paralleling of power MOSFETs in thermal equilibrium,” *Appl. Power Electron. Conf. and Expo., 2006. APEC '06. Twenty-First Annu. IEEE*, 2006, pp. 841-847.

[41] M. Tencer, J. S. Moss and T. Zapach, “Arrhenius average temperature: the effective temperature for non-fatigue wearout and long term reliability in variable thermal conditions and climates,” in *IEEE Trans. on Components and Packaging Technologies*, vol. 27, no. 3, pp. 602-607, Sept. 2004.

[42] Alpha and Omega Semiconductor, “Power Semiconductor Reliability Handbook,” *Application Note*.

[43] Lulu Wang, Bo Gao and Lixin Wang, "A study of the Au-Al bonding lifetime for MOSFET devices," *Physical and Failure Analysis of Integrated Circuits (IPFA), 2015 IEEE 22nd International Symposium on the*, Hsinchu, 2015, pp. 366-369.

[44] B. Gutsmann, P. Mourick and D. Silber, "Exact inductive parasitic extraction for analysis of IGBT parallel switching including DCB-backside eddy currents," *Power Electron. Specialists Conf., 2000. PESC 00. 2000 IEEE 31st Annu.*, Galway, 2000, pp. 1291-1295, vol. 3.

[45] T. Lopez and R. Elferich, "Current Sharing of Paralleled Power MOSFETs at PWM Operation," *Power Electron. Specialists Conf., 2006. PESC '06. 37th IEEE*, Jeju, 2006, pp. 1-7.

[46] C. Martin, J. L. Schanen, J. M. Guichon and R. Pasterczyk, "Analysis of Electromagnetic Coupling and Current Distribution Inside a Power Module," in *IEEE Trans. on Industry Applicat.*, vol. 43, no. 4, pp. 893-901, July-Aug. 2007.

[47] A. Müsing, G. Ortiz and J. W. Kolar, "Optimization of the current distribution in press-pack high power IGBT modules," *Power Electron. Conf. (IPEC), 2010 International*, Sapporo, 2010, pp. 1139-1146.

[48] R. Alvarez, K. Fink and S. Bernet, "Simulation and experimental investigation of parallel connected IGBTs," *Ind. Technology (ICIT), 2010 IEEE International Conf. on*, Vi a del Mar, 2010, pp. 824-831.

[49] Helong Li *et al*., "Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs," in *IEEE Trans. on Power Electron.*, vol. 31, no. 1, pp. 621-634, Jan. 2016.

[50] D. P. Sadik, J. Colmenares, D. Peftitsis, J. K. Lim, J. Rabkowski and H. P. Nee, "Experimental investigations of static and transient current sharing of parallel-connected silicon carbide MOSFETs," *Power Electron. and Applicat. (EPE), 2013 15th European Conf. on*, Lille, 2013, pp. 1-10.

[51] C. Keller and Y. Tadros, "Are paralleled IGBT modules or paralleled IGBT inverters the better choice?," *Power Electron. and Applicat., 1993., Fifth European Conf. on*, Brighton, 1993, pp. 1-6, vol. 5.

[52] P. R. Palmer and J. C. Joyce, “Current redistribution in multi-chip IGBT modules under various gate drive conditions,” *Power Electron. and Variable Speed Drives, 1998. Seventh International Conf. on (Conf. Publ. No. 456)*, London, 1998, pp. 246-251.

[53] Mitsubishi Electric, “Using IGBT Module,” *Application Note.*

[54] P. O. Jeannin, J. L. Schanen and E. Clavel, “Original cabling conditions to insure balanced current during switching transitions between paralleled semiconductors,” *Industry Applicat. Conf., 1999. Thirty-Fourth IAS Annu. Meeting. Conf. Record of the 1999 IEEE*, Phoenix, AZ, 1999, pp. 1757-1764, vol. 3.

[55] B. Whitaker *et al.*, “High-temperature SiC power module with integrated SiC gate drivers for future high-density power electronics applications,” *Wide Bandgap Power Devices and Applicat. (WiPDA), 2014 IEEE Workshop on*, Knoxville, TN, 2014, pp. 36-40.

[56] J. Rabkowski, D. Peftitsis and H. P. Nee, “Silicon Carbide Power Transistors: A New Era in Power Electronics Is Initiated,” in *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17-26, Jun. 2012.

[57] Yuancheng Ren, Ming Xu, Jinghai Zhou and F. C. Lee, “Analytical loss model of power MOSFET,” in *IEEE Trans. on Power Electron.*, vol. 21, no. 2, pp. 310-319, March 2006.

[58] M. Sasaki, H. Nishio, W. T. Ng, “Dynamic gate resistance control for current balancing in parallel connected IGBTs,” in *IEEE Appl. Power Electron. Conf. and Expo.* (APEC), Mar., 2013, pp. 244-249.

[59] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang and B. J. Blalock, “Design and Performance Evaluation of Overcurrent Protection Schemes for Silicon Carbide (SiC) Power MOSFETs,” in *IEEE Trans. on Ind. Electron.*, vol. 61, no. 10, pp. 5570-5581, Oct. 2014.

[60] P. Anthony, N. McNeill and D. Holliday, "High-speed resonant gate driver with controlled peak gate voltage for silicon carbide MOSFETs," *2012 IEEE Energy Convers. Congr. and Expo. (ECCE)*, Raleigh, NC, 2012, pp. 2961-2968.

[61] P. Hofer, N. Karrer and C. Gerster, “Paralleling intelligent IGBT power modules with active gate-controlled current balancing,” *Power Electron. Specialists Conf., 1996. PESC '96 Record., 27th Annu. IEEE*, Baveno, 1996, pp. 1312-1316, vol. 2.

[62] Jiann-Fuh Chen, Jiunn-Nan Lin and Tsu-Hua Ai, "The techniques of the serial and paralleled IGBTs," *Ind. Electron., Control, and Instrumentation, 1996., Proc. of the 1996 IEEE IECON 22nd International Conf. on*, Taipei, 1996, pp. 999-1004 vol.2.

[63] P. Hofer-Noser and N. Karrer, "Monitoring of paralleled IGBT/diode modules," in *IEEE Trans. on Power Electron.*, vol. 14, no. 3, pp. 438-444, May 1999.

[64] J.J. Nelson and G. Venkataramanan, "Active Gate Control for Parallel Operation of IGBT Devices," Center Power Electron. Syst. Seminar, Virginia Tech., pp. 471-477, April 2002.

[65] D. Bortis, J. Biela and J. W. Kolar, "Active gate control for current balancing in parallel connected IGBT modules in solid state modulators," *Pulsed Power Conf., 2007 16th IEEE International*, Albuquerque, NM, 2007, pp. 1323-1326.

[66] D. Bortis, P. Steiner, J. Biela and J. W. Kolar, "Double-stage gate drive circuit for parallel connected IGBT modules," in *IEEE Trans. on Dielectrics and Electrical Insulation*, vol. 16, no. 4, pp. 1020-1027, August 2009.

[67] R. Alvarez and S. Bernet, "A new delay time compensation principle for parallel connected IGBTs," *Energy Convers. Congr. and Expo. (ECCE), 2011 IEEE*, Phoenix, AZ, 2011, pp. 3000-3007.

[68] Chuck Wong and K. Priest, "Current sharing for paralleled IGBTs using statistics method," *Industry Applicat. Conf., 1996. Thirty-First IAS Annu. Meeting, IAS '96., Conf. Record of the 1996 IEEE*, San Diego, CA, 1996, pp. 1418-1424, vol. 3.

[69] Y. Lobsiger, D. Bortis and J. W. Kolar, "Decentralized active gate control for current balancing of parallel connected IGBT modules," *Power Electron. and Applicat. (EPE 2011), Proc. of the 2011-14th European Conf. on*, Birmingham, 2011, pp. 1-10.

[70] R. Alvarez and S. Bernet, "Sinusoidal current operation of delay time compensation for parallel connected IGBTs," *Energy Convers. Congr. and Expo. (ECCE), 2012 IEEE*, Raleigh, NC, 2012, pp. 3942-3949.

[71] M. Sasaki, H. Nishio and W. T. Ng, "Dynamic gate resistance control for current balancing in parallel connected IGBTs," *Appl. Power Electron. Conf. and Expo. (APEC), 2013 Twenty-Eighth Annu. IEEE*, Long Beach, CA, USA, 2013, pp. 244-249.

[72] J. J. Nelson, G. Venkataramanan and B. C. Beihoff, “Investigation of parallel operation of IGBTs,” *Industry Applicat. Conf., 2002. 37th IAS Annu. Meeting. Conf. Record of the*, Pittsburgh, PA, USA, 2002, pp. 2585-259, 1 vol. 4.

[73] Y. F. Wu, “Paralleling high-speed GaN power HEMTs for quadrupled power output,” *Appl. Power Electron. Conf. and Expo. (APEC), 2013 Twenty-Eighth Annu. IEEE*, Long Beach, CA, 2013, pp. 211-214.

[74] W. Teulings, J. L. Schanen and J. Roudet, “MOSFET switching behaviour under influence of PCB stray inductance,” *Ind. Applicat. Conf.*, San Diego, CA, 1996, pp. 1449-1453.

[75] Y. Xiao, H. Shah, T. P. Chow and R. J. Gutmann, “Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics,” *Appl. Power Electron. Conf. and Expo. (APEC)*, 2004, pp. 516-521.

[76] Z. Chen, D. Boroyevich, P. Mattavelli and K. Ngo, “A frequency-domain study on the effect of DC-link decoupling capacitors,” *2013 IEEE Energy Convers. Congr. and Expo. (ECCE)*, Denver, CO, 2013, pp. 1886-1893.

[77] J. Wang, H. S. h. Chung and R. T. h. Li, “Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance,” in *IEEE Trans. on Power Electron.*, vol. 28, no. 1, pp. 573-590, Jan. 2013.

[78] Y. Mao, Z. Miao, K. D. T. Ngo and C. M. Wang, “Balancing of peak currents between paralleled SiC MOSFETs by source impedances,” *2017 IEEE Appl. Power Electron. Conf. and Expo. (APEC)*, Tampa, FL, 2017, pp. 800-803.

[79] Y. Mao, Z. Miao, C. M. Wang and K. D. T. Ngo, “Passive Balancing of Peak Currents Between Paralleled MOSFETs With Unequal Threshold Voltages,” in *IEEE Trans. on Power Electron.*, vol. 32, no. 5, pp. 3273-3277, May 2017.

[80] P. Wong, Q. Wu, P. Xu, B. Yang and F. C. Lee, “Investigating coupling inductors in the interleaving QSW VRM,” *Appl. Power Electron. Conf. and Expo. (APEC)*, New Orleans, LA, 2000, pp. 973-978.

[81] Y. Mao, Z. Miao, C. M. Wang and K. D. T. Ngo, "Balancing of Peak Currents Between Paralleled SiC MOSFETs by Drive-Source Resistors and Coupled Power-Source Inductors," in *IEEE Trans. on Ind. Electron.*, vol. 64, no. 10, pp. 8334-8343, Oct. 2017.

[82] CREE, *C4D20120A datasheet*. [Online]. Available: http://www.wolfspeed.com/media/downloads/85/C4D20120A.pdf.

[83] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," *2011 IEEE Energy Convers. Congr. and Expo.*, Phoenix, AZ, 2011, pp. 2681-2688.

[84] J. C. Hernandez, L. P. Petersen, M. A. E. Andersen and N. H. Petersen, "Ultrafast switching superjunction MOSFETs for single phase PFC applications," *Appl. Power Electron. Conf. and Expo. (APEC), 2014 Twenty-Ninth Annu. IEEE*, Fort Worth, TX, 2014, pp. 143-149.

[85] J. A. Ferreira, W. A. Cronje and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits," in *IEEE Trans. on Power Electron.*, vol. 10, no. 1, pp. 32-37, Jan 1995.

[86] Z. Liu, X. Huang, F. C. Lee and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," in *IEEE Trans. on Power Electron.*, vol. 29, no. 4, pp. 1977-1985, April 2014.

[87] Tektronix, *TCP0030A datasheet*. [Online]. Available: http://www.tek.com/datasheet/tcp0030a-ac-dc-current-probe-datasheet.

[88] Tektronix, *THDP0200 datasheet*. [Online]. Available: http://www.tek.com/sites/tek.com/files/media/media/resources/TMDP-THDP-P5200A-High-Voltage-Differential-Probe-Datasheet-51W1119511.pdf

[89] Zheyu Zhang *et al*., "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," *Appl. Power Electron. Conf. and Expo. (APEC), 2014 Twenty-Ninth Annu. IEEE*, Fort Worth, TX, 2014, pp. 2534-2541.

[90] M. Khatib, J. Zheng, K. D. T. Ngo, and G. Q. Lu, "Power Cycling and Measurement of Thermal Impedance to Determine Reliability of IGBT Modules" in *Proc. of CPES Annu. Power Electron. Conf.*, Blacksburg, VA, 2013.

[91] CREE, *CRD-001 datasheet*. [Online]. Available: http://www.wolfspeed.com/crd001.

[92] Ansys, *Q3D extractor*. [Online]. Available: http://www.ansys.com/Products/Electronics/ANSYS-Q3D-Extractor.

[93] H. A. Wheeler, "Simple Inductance Formulas for Radio Coils," in *Proc. of the Inst. of Radio Engineers*, vol. 16, no. 10, pp. 1398-1400, Oct. 1928.

[94] E. B. Rosa, “The self and mutual inductances of liner conductors”, Bull. Bur. Standards, vol. 4, no. 2, pp. 301-344, 1908.

[95] A. J. Hanson, J. A. Belk, S. Lim, C. R. Sullivan, D. J. Perreault, “Measurements and performance factor comparisons of magnetic materials at high frequency,” *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7909-7925, Nov. 2016.

[96] D. B. Hou, F. C. Lee, Q. Li, “Very high frequency integrated voltage regulator for small portable devices,” in *Porc. IEEE Energy Convers. Congr. Expo. (ECCE),* Sept. 2016, pp. 1-7.

[97] Y. Zhong, X. Wen, W. Sun, W. Su and J. Meng, “A novel IGBT package to reduce current imbalance with pinfin baseplate,” *Energy Convers. Congr. and Expo. (ECCE), 2013 IEEE,* Denver, CO, 2013, pp. 268-272.

[98] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock and F. Wang, “A compact planar Rogowski coil current sensor for active current balancing of parallel-connected Silicon Carbide MOSFETs,” *Energy Convers. Congr. and Expo. (ECCE), 2014 IEEE,* Pittsburgh, PA, 2014, pp. 4685-4690.

[99] H. Li, S. Munk-Nielsen, C. Pham and S. Bęczkowski, “Circuit mismatch influence on performance of paralleling silicon carbide MOSFETs,” *Power Electron. and Applicat. (EPE'14-ECCE Europe), 2014 16th European Conf. on,* Lappeenranta, 2014, pp. 1-8.

[100] H. Li, S. Beczkowski, S. Munk-Nielsen, R. Maheshwari and T. Franke, “Circuit mismatch and current coupling effect influence on paralleling SiC MOSFETs in multichip power modules,” *PCIM Europe 2015; International Exhibition and Conf. for Power Electron., Intelligent Motion, Renewable Energy and Energy Management; Proc. of,* Nuremberg, Germany, 2015, pp. 1-8.

[101] D. Reusch and J. Strydom, “Effectively paralleling gallium nitride transistors for high current and high frequency applications,” *Appl. Power Electron. Conf. and Expo. (APEC), 2015 IEEE*, Charlotte, NC, 2015, pp. 745-751.

[102] D. Reusch and J. Strydom, “Improving Performance of High Speed GaN Transistors Operating in Parallel for High Current Applications,” *PCIM Europe 2014; International Exhibition and Conf. for Power Electron., Intelligent Motion, Renewable Energy and Energy Management; Proc. of,* Nuremberg, Germany, 2014, pp. 1-8.

[103] Z. Wang, Y. Wu, J. Honea and L. Zhou, “Paralleling GaN HEMTs for diode-free bridge power converters,” *Appl. Power Electron. Conf. and Expo. (APEC), 2015 IEEE*, Charlotte, NC, 2015, pp. 752-758.

[104] Texas Instruments, “Estimating MOSFET Parameters from the Data Sheet,” *Application Note*.

[105] Infineon, “MOSFET Power Losses Calculation Using the Datasheet Parameters,” *Application Note*.

[106] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar and J. S. Zúniga, “An Insight into the Switching Process of Power MOSFETs: An Improved Analytical Losses Model,” in *IEEE Trans. on Power Electron.*, vol. 25, no. 6, pp. 1626-1640, June 2010.

[107] N. Mohan, T. Undeland, andW. Robbins, *Power Electrononics—Converters, Applications and Design*, 2nd ed. New York: Wiley, 1995.

[108] U. Drofenik, A. Müsing and J. W. Kolar, “Voltage-dependent capacitors in power electronic multi-domain simulations,” *Power Electron. Conf. (IPEC), 2010 International*, Sapporo, 2010, pp. 643-650.

[109] On Semiconductor, “Characterizing the dynamic output capacitance of a MOSFET,” *Application Note.*

[110] T. Heckel and L. Frey, “A novel charge based SPICE model for nonlinear device capacitances,” *Wide Bandgap Power Devices and Applicat. (WiPDA), 2015 IEEE 3rd Workshop on*, Blacksburg, VA, 2015, pp. 141-146.

[111] I. Castro *et al*., “Analytical Switching Loss Model for Superjunction MOSFET With Capacitive Nonlinearities and Displacement Currents for DC–DC Power Converters,” in *IEEE Trans. on Power Electron.*, vol. 31, no. 3, pp. 2485-2495, March 2016.

[112] B. Gutsmann, P. Mourick and D. Silber, “Exact inductive parasitic extraction for analysis of IGBT parallel switching including DCB-backside eddy currents,” *2000 IEEE 31st Annu. Power Electron. Specialists Conf. Proc. (Cat. No.00CH37018)*, Galway, 2000, pp. 1291-1295 vol.3.

[113] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng and W. Chen, "An Analytical Switching Process Model of Low-Voltage eGaN HEMTs for Loss Calculation," in *IEEE Trans. on Power Electron.*, vol. 31, no. 1, pp. 635-647, Jan. 2016.

[114] M. Orabi and A. Shawky, "Proposed Switching Losses Model for Integrated Point-of-Load Synchronous Buck Converters," in *IEEE Trans. on Power Electron.*, vol. 30, no. 9, pp. 5136-5150, Sept. 2015.

[115] X. Huang, Q. Li, Z. Liu and F. C. Lee, "Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration," in *IEEE Trans. on Power Electron.*, vol. 29, no. 5, pp. 2208-2219, May 2014.

[116] J. Fu, Z. Zhang, Y. F. Liu and P. C. Sen, "MOSFET Switching Loss Model and Optimal Design of a Current Source Driver Considering the Current Diversion Problem," in *IEEE Trans. on Power Electron.*, vol. 27, no. 2, pp. 998-1012, Feb. 2012.