

# Millimeter-Wave Harmonically-Tuned Silicon Power Amplifiers for High Efficiency

Seyed Yahya Mortazavi

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Kwang-Jin Koh, Chair  
Dong. S. Ha  
Sanjay Raman  
R. Michael Buehrer  
Vinh Nguyen

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## ABSTRACT

This research utilizes the Class  $F^{-1}$  harmonic tuning approach to improve the power efficiency and power added efficiency (PAE) of the silicon power amplifiers (PAs) at mm-wave frequency bands. This work tunes the 2<sup>nd</sup> and 3<sup>rd</sup> harmonic components of voltage and current waveform over active device to improve the efficiency of the PA. The potentials and limitations of the class- $F^{-1}$  technique in achieving a high PAE at microwave and higher frequencies, especially for integrated PAs based on silicon process have been analyzed. To demonstrate effectiveness of the Class- $F^{-1}$  approach a multi-resonance 6<sup>th</sup> order load network is proposed which achieves 50% power added efficiency with 18dBm output power at 24GHz. By optimizing this network for 38GHz, based on the loss of passive components, PAE of 38.5% achieved. The design methodology developed for this network and extensive small signal, large signal, and linearity performance of both PAs presented. To further improve power efficiency of Class  $F^{-1}$  PAs, coupled inductor based harmonic tuning load network proposed. The load network, utilizes coupled inductors to enhance quality factor of the inductors and make wide bandwidth high impedance at 2<sup>nd</sup> harmonic and very low impedance at 3<sup>rd</sup> harmonic, which improves both efficiency and efficiency bandwidth. By using this load network and optimizing for 28GHz, 2-stage PA implemented with PAE~42% with 16.5dBm output power. As frequency increases to >30 GHz, the complexity of load network degrades the power efficiency improvement of the Class- $F^{-1}$  PAs. A simple  $\lambda/4$  transformer based load network proposed to tackle this issue and achieve high power efficiency. Using this load network, PAs implemented with exceptional PAE performance of 43% at 41 GHz and 23% 94 GHz with output power of 18 dBm and 11 dBm, respectively. To increase peak PAE bandwidth of PA, a simple LC-based multi-resonance network proposed which provides in band mode transition from Continuous-Class- $F^{-1}$  to Continuous-Class-F. The PA operated at Continuous-Class- $F^{-1}$  mode at low signal frequency band and Continuous-Class-F mode at high signal frequency band. By using mode-transition, PAE > 36.5% achieved over 25% fractional bandwidth (25 GHz~31 GHz).

In summary, this research presents different harmonic tuning load networks for Class  $F^{-1}$  operation to address different issues and improve efficiency of mm-wave silicon PAs.

To my dear parents and my lovely wife Shirin

## Attribution

This dissertation is composed of an introduction, five main chapters and a conclusion. The main chapters are published in four conference papers and either have or will be submitted to archival journals for separate publication. Chapter three is published in a journal paper.

**Dr. Kwang-Jin Koh**, Ph.D., Assistant Professor in department of Electrical and computer Engineering (ECE), Virginia Tech, Served as the committee chair and provided advice on the works presented in each chapter. Dr. Koh is a coauthor on each and all of the papers.

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# 1 Introduction

## 1.1 Motivation

A wide spectrum of applications like mobile internet, home networking, gaming, and multimedia streaming have motivated the exponential growth of data traffic in wireless communication systems. Fig. 1-1 shows the growth of the data traffic since 2010 and the predictions till 2030 [1]. The 25-50% growth of data traffic is expected to continue annually till 2030 and beyond due to the demand for more connected devices like the Internet of Things, vehicle-to-vehicle (V2V) communications, and wearable devices, and more value added services like e-health, ultra-high definition video streaming, virtual reality, and smart cars. The limited available spectrum at microwave frequencies below 10GHz draws attentions to millimeter wave (mm-wave) bands: the local multipoint distribution service (LMDS) at 28-30 GHz and 38-40GHz, the unlicensed band at 57-66 GHz, 71-76 GHz, 81-86 GHz, and 92-95 GHz [2]. Therefore, moving to mm-wave frequencies allows for larger bandwidth allocations to each user and thus higher data transfer rates. Moreover, by expanding the channel bandwidths beyond the present 20 MHz channels used by 4G customers, the data capacity will greatly increase while the latency for digital

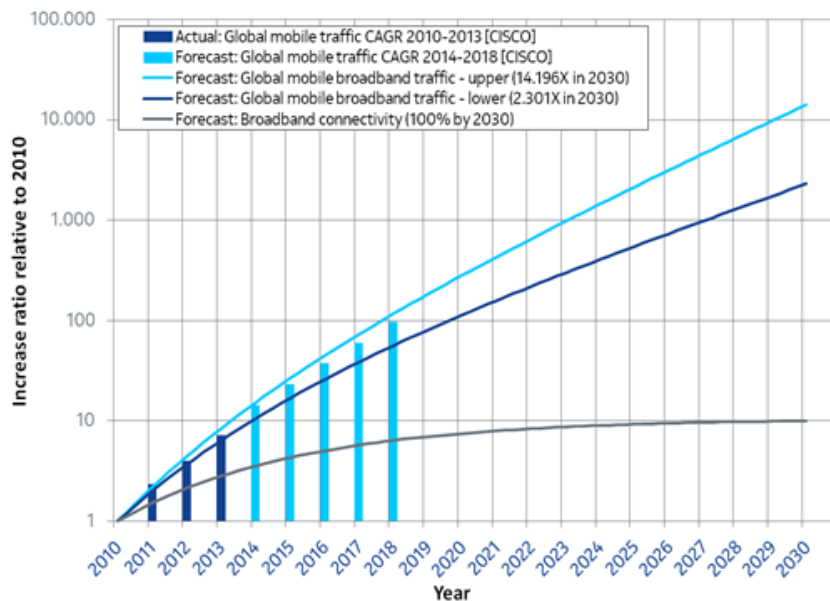


Fig. 1-1 The growth of data traffic since 2010 and predictions till 2030 [1].



traffic is decreased, thus supporting much better internet-based access and applications that require minimal latency [3]. Massive densification of mm-wave small cells deployed underlying the macrocells as WLANs or WPANs are also a promising solution for the extreme capacity enhancement for the exploding future data traffic growth. With huge bandwidth, cells are able to provide the multi-gigabit rates, and wideband multimedia applications [4].

The trend toward mm-wave wireless communication has opened up a challenging opportunities of mm-wave integrated circuit design. Microwave and mm-wave integrated circuits have been traditionally designed using III-V semiconductor technologies, such as GaAs and InP. The III-V compounds have superior performance compared with silicon devices due to their higher electron mobility and higher breakdown voltage. They also provide low-loss substrates, high quality metal layers, and through-substrate vias, all of which support high-performance passive networks, and high thermal conductivity [5]. Nonetheless, there is a large demand for silicon integrated circuits at mm-wave mainly because silicon promises higher levels of integration which is an effective way to reduce size and end user cost. Integrating RF front-end blocks with digital base-band processing modules reduces the area and the number of packages, and hence reduces cost. Also, silicon process has superior yield for mass production compared with III-V technologies which reduces the total cost of a product.

Silicon devices have extraordinary performance for low-power digital circuits at baseband, however, it is challenging to design high performance RF/mm-wave front-end blocks mainly due to low device speed (i.e.  $f_T = 200\sim 350$  GHz). Recently, by using submicron scaled CMOS technology nodes (e.g. 65nm/45nm SOI CMOS) or 130nm/90nm SiGe BiCMOS, most of the building blocks of mm-wave transceiver successfully integrated into silicon technology [6]-[7]. Nevertheless, the power amplifier (PA) is often implemented as a stand-alone module in expensive process like GaAs HBT. In addition to device speed, the low power handling of silicon devices is another challenge of designing high performance PAs in silicon. The PA is the last block in transmitter chain and needs to deliver tens to hundreds of milliwatts to a fixed load and most of the power dissipation in a wireless products is in the PA. Therefore, PA power efficiency is a key point for power consumption of the wireless transceiver. In addition, since a significant portion of the DC power is dissipated as heat, low power efficiency of the PA raises serious thermal issues and increases thermal handling and cooling costs in the transceiver.

Fig. 1-2 shows the efficiency performance and output power of the state-of-the-art mm-wave silicon PAs. So far, for unit PA peak PAE ~35% with  $P_{out}$  ~16-23 dBm is reported in the literature. Due to lower speed of silicon devices, they suffer from low power gain and need high driving power which reduces overall power efficiency of the transmitter. Also, the break down voltage of CMOS/BiCMOS silicon devices is in the range of 1V~5V, which is very low compared to III-V devices (~>40V). Therefore, generating high out power in silicon devices is challenging. To increase output power and achieve wattlevel silicon PAs power combining techniques using PA arrays are inevitable. However, power combining networks with lossy passives at mm-wave have 70%~85% efficiency degradation and, as Fig. 1-2 shows, the projected efficiency performance for wattlevel PAs is 15-28%. Therefore, the power efficiency of the unit PA with 15~20 dBm output power becomes crucial to achieve overall high power efficiency.

The primary goal of this research is to investigate harmonic tuning approach for design of high efficiency silicon PAs at mm-wave bands for communication applications and imaging systems.

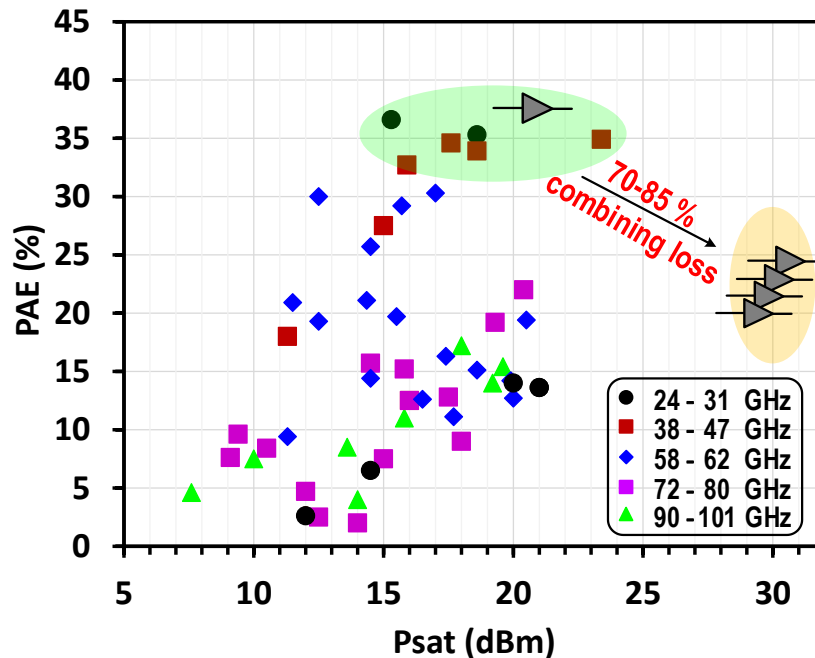


Fig. 1-2 Efficiency and output power of the mm-wave silicon PAs with performance projection for watt-level PAs.

## 1.2 Problem statement

The primary goal of this research is to investigate harmonic tuning approach and propose effective load networks to improve power efficiency of the mm-wave silicon PAs communication applications and imaging systems. This work explores harmonic tuning approach to shape voltage and current waveforms over power device, reduce the power dissipation, and improve the power efficiency and power added efficiency of the PA. Therefore, the load network should effectively manipulate the harmonic contents of the power device while providing optimum load at fundamental frequency. At mm-wave frequencies, designing such a load is very challenging due to the unwanted capacitive and inductive coupling between different nodes and lines. As operating frequency increases in mm-wave regime, very detailed and careful electro-magnetic modeling and simulations are required to capture all parasitic capacitances and inductances especially at the harmonic bands. The design of load network both at fundamental and harmonic bands plays a key role in the performance of the PA. The load network should absorb the parasitics in fundamental and harmonic frequency bands, especially at output node of the power device.

Silicon substrate is conductive in modern integrated circuits (typical substrate resistivity  $\sim 10\text{-}\Omega\cdot\text{cm}$  for bulk processes). This conductivity causes energy loss due to magnetically induced eddy currents. Passive devices also suffer from energy loss due to their finite conductivity. The ohmic energy loss can be significantly more important at mm-waves because of the small skin depth. As operating frequency increases in mm-wave bands, the low quality of the passives, especially at harmonic bands, degrades the effectiveness of the complex load networks. Therefore, the load network should be very simple yet effective to shape the waveforms and improve power efficiency of the PA.

Another issue which should be addressed is that the harmonic tuning PAs have low efficiency bandwidth. The bandwidth of the harmonic load limits the efficiency bandwidth of the PAs. Wide-bandwidth tuning of the harmonics increases the complexity of the load network, therefore, increasing the efficiency bandwidth becomes more challenging at mm-wave PAs.

This work investigates Class-F<sup>-1</sup> mode operation with 2<sup>nd</sup> and 3<sup>rd</sup> harmonic tuning for silicon mm-wave PAs. This work studies the limiting factors of power efficiency of Class-F<sup>-1</sup> for silicon mm-wave PAs and proposes different load networks to address the above-mentioned problems.

The design methodology and analysis of the proposed load networks are presented and verified with implementation and measured results at different mm-wave frequencies.

### 1.3 Contributions of this research and Organization of the dissertation

This research is the first work addressing the challenges and limitations of the high efficiency Class-F<sup>-1</sup> PAs for mm-wave silicon technology using 0.13  $\mu\text{m}$  SiGe BiCMOS. This work proposes different load networks to mitigate these challenges for integrated Class-F<sup>-1</sup> PAs and present implementations with highest power efficiency performances reported so far: PAE= 50% @ 24 GHz, PAE = 43% @ 41 GHz, and PAE = 23% @ 94 GHz. The design methodology and detailed analysis of the proposed load networks presented and verified with implementation and measured results.

Key contributions of this research are as following:

1. The limitations and challenges of the Class-F<sup>-1</sup> harmonic tuning approach for mm-wave silicon PAs addressed and a multi-resonance LC-load network proposed for Class-F<sup>-1</sup> PA as a proof of concept for viability of achieving high power efficiency beyond state-of-the-art silicon PAs. The design methodology and detailed analysis presented and verified with PA implementation at 24 GHz (PAE = 50%,  $P_{\text{sat}} = 18$  dBm) and 38 GHz (PAE = 38.5%,  $P_{\text{sat}} = 16.5$  dBm).
2. To address the issues of low quality factor of the passives in the load network, a Q-enhancement method proposed for Class-F<sup>-1</sup> based on coupled inductors. The design methodology and analysis presented and verified with PA implementation at 28 GHz (PAE = 42%,  $P_{\text{sat}} = 16.5$  dBm).
3. To mitigate power efficiency degradation in Class-F<sup>-1</sup> PAs due to low-quality passives at high mm-wave frequencies, a simplified load network is proposed based on  $\lambda/4$ -transformer. The design methodology and analysis presented and verified with PA implementation at 40 GHz (PAE = 43%,  $P_{\text{sat}} = 18$  dBm) and 94 GHz (PAE = 23%,  $P_{\text{sat}} = 11$  dBm).

4. To increase efficiency bandwidth of harmonically tuned PA, a multi-resonance LC-based load network proposed with in band mode transition from Continuous Class-F<sup>-1</sup> to Continuous Class-F to achieve wide efficiency bandwidth. The design methodology and analysis presented and verified with PA implementation at 28 GHz (PAE > 39% @ 25-31 GHz, P<sub>sat</sub> = 17.2 dBm).

The outline of this dissertation is as follows:

In chapter 2, the performance merits of PA and different classes are introduced. This chapter discusses the shortcoming of different classes of PAs for achieving high efficiency at mm-wave bands with silicon technology. Chapter 3 discusses the efficiency limiting factors in Class-F<sup>-1</sup> PAs, especially for integrated PAs based on silicon technologies. Specifically, the efficiency degradation by a finite number of harmonics control, knee voltage, limited breakdown voltage, and finite losses from passive networks on PAE have been analyzed with supporting mathematical models. This chapter presents details on the design methodology of the proposed load network for a low-loss bi-harmonic impedance termination for an optimal Class-F<sup>-1</sup> operation. Chapter 4 presents the proposed Class-F<sup>-1</sup> load network with Q-enhancement method to improve the PAE by utilizing harmonic tuning despite low-quality passives at mm-wave. Design methodology of the proposed load network is also disclosed in detail. A simple and effective load network based on  $\lambda/4$ -transformer proposed in chapter 5 for >40 GHz mm-wave bands. The measurement results presented and discussed for two implemented PAs at 40 GHz and 94 GHz. Chapter 6 presents the proposed load network with in band transition from Continuous-Class-F<sup>-1</sup> to Continuous-Class-F operation mode for mm-wave bands. This mode transition increases the efficiency bandwidth while high PAE is achieved by harmonic tuning all over the signal band. Chapter 7 summarizes and concludes this research and suggest future works.



## 2 Technical Background

### 2.1 The merits for measuring efficiency performance of PAs

The PA is the most power hungry building block in wireless transceiver. Power Efficiency (called collector efficiency) and Power Added Efficiency (PAE) are main measures of efficiency of the power amplifier. The Power Efficiency (PE) defined as:

$$\eta_c = PE = \frac{P_{out}}{P_{DC}} \quad (2 - 1)$$

PE shows how much power is consumed from DC power supply,  $P_{DC}$ , when PA converts DC power to RF power and delivers it to the output load,  $P_{out}$ . The other metric, PAE, measures the efficiency of the PA for the portion of RF power that PA contributes to the total power,  $P_{out}-P_{in}$ , delivered to the load. PAE is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (2 - 2)$$

The PAE can be expressed in terms of PE and gain of the PA,  $G$ , as:

$$PAE = PE \cdot \left(1 - \frac{1}{G}\right) \quad (2 - 3)$$

The PAE and PE are approximately same for amplifiers with high gain,  $\sim G > 10\text{dB}$ . For PAs with low gain, the PAE is better measure of efficiency performance compared to PE.

For cascade two-stage PAs, the total PAE can be expressed as:

$$\frac{1}{PAE_{total}} = \left( \frac{1}{PE_{output}} + \frac{1}{PE_{driving} \cdot G_{output}} \right) \cdot \left( 1 - \frac{1}{G_{output} \cdot G_{driving}} \right) \quad (2 - 4)$$

which shows the PE of the last stage is the most dominant term in total PE and total PAE and as we go back to the driving stages the power gain of proceeding stages relaxes the PE requirements.

PA linearity is another important performance metric for PAs, particularly critical for PAs amplifying spectrally efficient complex modulated such as high-order quadrature amplitude

modulation (QAM) signals. To characterize the linearity of the PA when amplifying a modulated input signal, both in-band and out-of-band performance should be evaluated. For in-band linearity performance, error vector magnitude (EVM) of the constellation of the output signal is measured. EVM is a measure of the deviations in constellation of the output signal from ideal constellation points which are due to The PA nonlinearities and defined as:

$$EVM = \sqrt{\frac{\sum_{i=1}^N \Delta I_i^2 + \Delta Q_i^2}{\sum_{i=1}^N |V|_i^2}} \Big|_{\%} \quad (2 - 5)$$

the signal vector and error vector is demonstrated in Fig. 2-1 (a).

Moreover, nonlinear PA behavior also distorts the constellation trajectories and generate undesired intermodulation tones. These out-of-band distortions may lead to spectral regrowth of the transmitted signal, violate the spectrum mask compliance, and eventually result in link fratricide in highly dense electromagnetic environment. The out-of-band nonlinearity of the PA is measure based on the signal leakage power, mainly due to spectral regrowth, to the adjacent channels as:

$$ACPR = 10 \log \left( \frac{P_{adj}}{P_{ref}} \right) \Big|_{dB} \quad (2 - 4)$$

Adjacent Channel Power Ratio (ACPR) is shown in Fig. 2-1 (b).

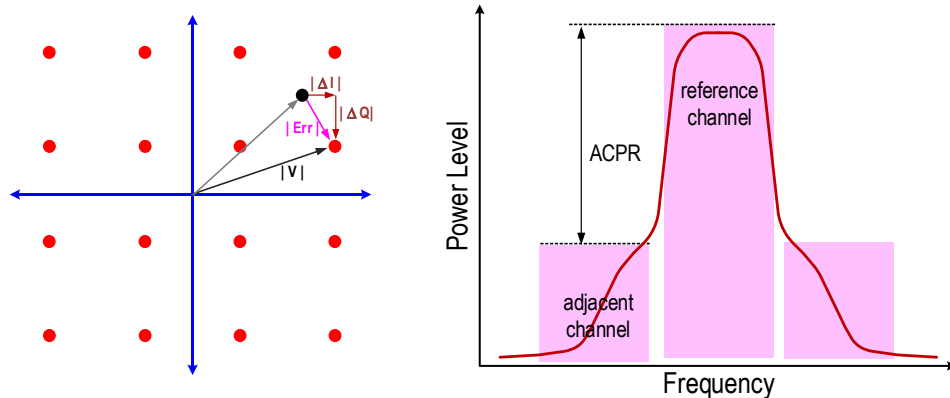


Fig. 2-1 Efficiency and output power of the mm-wave silicon PAs with performance projection for watt-level PAs.



## 2.2 Classes of PAs

The PAs can be classified to two main categories based on operation of the active device: linear PAs and switching PAs. In the linear PAs the active device works as transconductance,  $g_m$ , and provides current gain. In the switching PAs, the active device works as switch and by providing a high current path to a DC source to charge/discharge the load and amplifies the input signal. In this section different classes of linear and switching amplifiers will be introduced.

### 2.2.1 Linear power amplifiers (Class A/AB/ B)

In linear PAs the transistor operates as a current source with transconductance of  $g_m$ . Linear PAs are also classified based on conducting time of the active device in one cycle of input signal, called conduction angle. The PA operates in Class-A if the device is conducting current all the time (conduction angle =  $2\pi$ -rad). Class-A is the most linear PA and the least efficient one. Fig. 2-2 (a) shows the voltage and current waveforms for Class-A PA. The maximum voltage swing is  $V_{dd} - V_{knee}$  and the maximum current swing is equal to DC bias. Therefore, the peak output power is [7]:

$$P_{out,max}^A = \frac{1}{2} \cdot I_{ac,max} \cdot V_{ac,max} = \frac{1}{2} \cdot I_{DC} \cdot (V_{dd} - V_{knee}) \quad (2 - 5)$$

the PE of the Class-A PA is then derived as [3]:

$$PE = \frac{P_{out,max}^A}{P_{DC}} = \frac{\frac{1}{2} \cdot I_{DC} \cdot (V_{dd} - V_{knee})}{I_{DC} \cdot V_{dd}} \approx 50\% \quad (2 - 6)$$

In the Class-A amplifier, the active device dissipates half of the DC power provided by the supply voltage. To improve the efficiency of the PA, the overlapped region of non-zero voltage and current waveform should reduce to decrease the DC power consumption. This is achieved by appropriate biasing and reducing the conduction time of PA (conduction angle <  $2\pi$ -rad). When the active device conducts the current for less than the time period of the input signal, both fundamental and DC component of the current waveform decrease but the DC component decreases more than the fundamental. Therefore, the efficiency of the PA increases at the cost of reducing output power. In Class-B PAs, the device conducts the current for the half of time period of the input signal (conduction angle =  $\pi$ -rad) and the power efficiency is ~79%. In addition to

lower output power and thus gain compared to Class A, the linearity of Class B is also lower than Class A. To improve linearity of Class B, the conduction angle could be increased to be between  $\pi$  (Class B) and  $2\pi$  (Class A) which is called Class AB with PE in the range of ~79% to 50% depending on conduction angle. The PE of Class AB is expressed as a function of conduction angle as [9]:

$$PE = \frac{P_{out,max}^{AB}}{P_{DC}} = \frac{\frac{1}{2} \cdot I_{DC} \cdot (V_{dd} - V_{Knee})}{I_{DC} \cdot V_{dd}} \cdot \frac{\alpha - \sin(\alpha)}{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)} \quad (2 - 7)$$

where  $\alpha$  is conduction angle of the PA. Fig.2-2 (b) shows the Class B current and voltage waveforms.

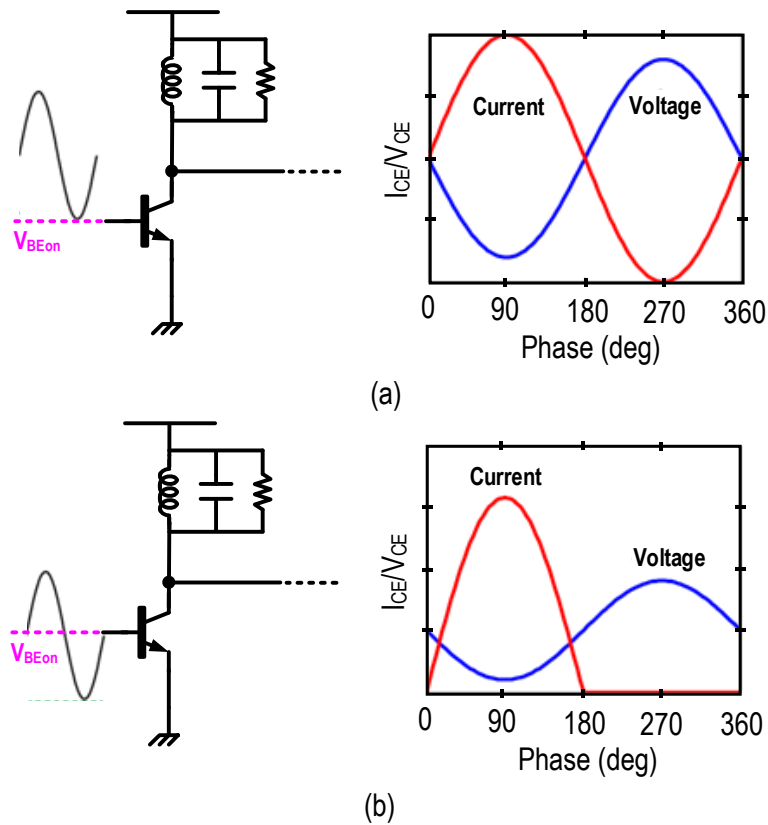


Fig. 2-2 Voltage and current waveforms for linear PAs: (a) Class-A, (b) Class-B.

## 2.2.2 Switching power amplifiers (Class D/E)

In switching amplifiers, the power transistor works as switch in either triode region or cut-off region. The most basic switching amplifier is Class-D PA. Fig. 2-3 (a) shows the schematic and current and voltage waveform for Class-D switching PA. The series LC filters the fundamental frequency to deliver the power to load. As shown in Fig. 2-3 (a) the voltage and current waveforms are non-overlapping and the PE  $\sim 100\%$  is achievable in theory. Implementing Class D PA is limited to low frequency ranges due to parasitic capacitor at the collector (drain) node of the transistor. The Class E switching PAs absorb the output parasitic capacitance in the load network while the current and voltage waveforms are non-overlapping as shown in Fig. 2-3 (b). When the switch is off, the current following into the drain is zero while the drain voltage is non-zero. The voltage waveform becomes zero right before the switch turns on and remains zero until the switch turns off. This is called zero voltage switching (ZVS) which avoids the switching loss on the output capacitor when the switch turns on. Fig. 2-3 (b) shows the current and voltage waveforms for Class E PA.

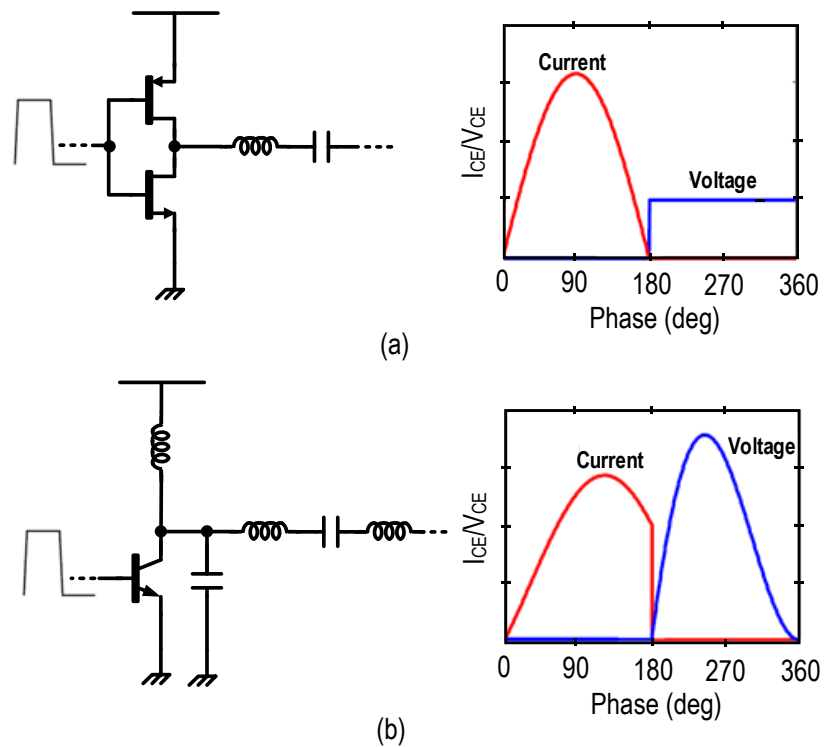


Fig. 2-3 Voltage and current waveforms for switching PAs: (a) Class-D, (b) Class-E

## 2.3 Harmonic tuned power amplifiers: Class F<sup>-1</sup>/Class F

By tuning harmonic load of Class AB/B PAs it is possible to make non-overlapped current and voltage waveforms over power transistor and achieve PE ~ 100%. This approach is utilized in Class F<sup>-1</sup> and Class F PAs. Fig. 2-4 shows the harmonic tuning load and time-domain current and voltage waveforms. In Class F<sup>-1</sup> PA, all odd harmonics are terminated with short circuit and all even harmonics are terminated with open circuit. Therefore, as Fig. 2-4 shows, the current waveform is rectangular odd harmonic-rich and voltage waveform is half-sinusoidal harmonic-rich and current and voltage waveforms are non-overlapped and PE~100%. Class F is dual of Class F<sup>-1</sup> where the current waveform is half-sinusoidal and voltage waveform is rectangular. The odd harmonics are terminated to with open circuit load and even harmonics are terminated with short circuit load. To achieve PE~100% in Class F<sup>-1</sup> and Class F, all harmonics should be terminated appropriately, however, this needs complex load network and practically the loss of passive components degrades the efficiency. Table I shows the achievable PE with controlling up to 5<sup>th</sup> harmonic. In mm-wave frequency bands, the complexity of the load becomes more critical and the PE becomes limited to ~90% by controlling 2<sup>nd</sup> and 3<sup>rd</sup> [10].

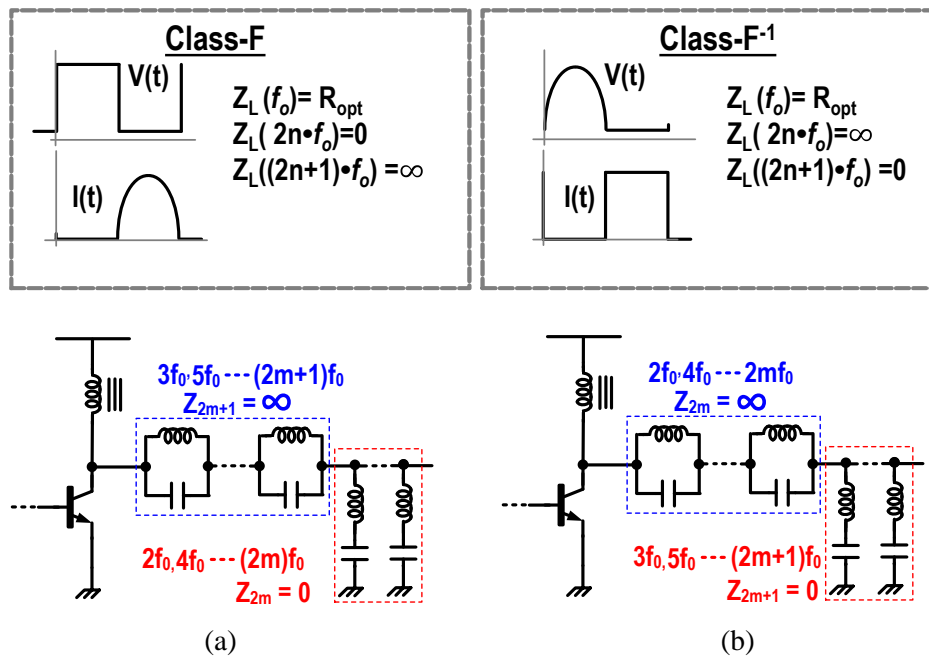


Fig. 2-4 Voltage and current waveforms for Class F and Class F<sup>-1</sup>PA with conceptual schematic for Class F<sup>-1</sup> PA.

Table 2-1: Peak achievable Power Efficiency (PE) using different harmonic tuning

Class	Harmonic control	PE (%)
B	-	78.5
F <sup>-1</sup>	2 <sup>nd</sup> & 3 <sup>rd</sup>	90
F <sup>-1</sup>	2 <sup>nd</sup> , 3 <sup>rd</sup> , & 4 <sup>th</sup>	95.5
F	2 <sup>nd</sup> & 3 <sup>rd</sup>	90.7
F	2 <sup>nd</sup> , 3 <sup>rd</sup> , 4 <sup>th</sup> & 5 <sup>th</sup>	92

## 2.4 Mm-wave Silicon Power Amplifiers

At mm-wave bands the operating frequency of the PA is a fraction of the silicon device speed ( $f_T/f_{MAX}$ ), which limits the gain of the device. Also, at this high frequencies, the parasitics of the transistor interconnects and wiring drastically affect the operation of the circuit and need careful design and layout considerations. Therefore, to avoid complex load network, most of the PAs in mm-wave are Class-AB. The load network matches the optimum load at collector node to the output 50- $\Omega$  load and relies on the big parasitic capacitor of the output node (collector) of the large power device for shorting harmonic loads to ground. Regarding low power gain of silicon devices, even though the Class-B biasing point provides peak power efficiency, it is not an optimum biasing for peak PAE due to low power gain. In Class-AB PAs, based on the required efficiency and linearity, the biasing point of the device is chosen the biasing spectrum between Class-A and Class-B with optimum efficiency and power gain to achieve high PAE. To further improve efficiency at mm-wave silicon PAs, Continuous-Class-AB mode is utilized at 28 GHz [11]. Fig. 2-5 (a) shows the PA with Continuous-Class-AB load at the output stage. By tuning harmonic components the PA achieves peak PAE ~35% at 28GHz.

Class E PAs with peak PAE ~ 35% are reported at Q-band (41 GHz) [12], shown in Fig. 2-5 (b). The Class E power amplifiers are not suitable for transceivers with linear modulations. However, for applications like car radars at mm-wave, where linearity is not a concern, Class-E switching PAs could be used. High efficiency Class E PAs are also utilized in RF DAC PA structures [13].

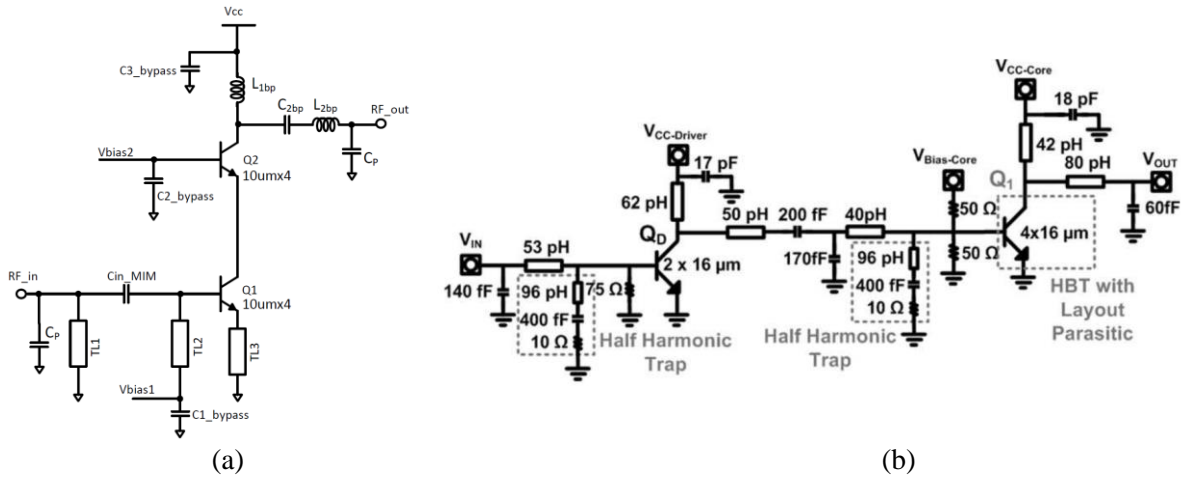


Fig. 2-5 mm-wave PAs with highest power efficiency, so far, : (a) continuous Class-A [11], (b) switching Class-E [12].

## 2.5 Harmonic tuning PA at mm-wave

Harmonic tuning approach can be utilized to improve the PAE performance of linear silicon PAs. In [6] harmonic tuning for Continuous-Class-AB is presented. However, the main goal for Continuous-Class-AB operation mode is to provide wider efficiency bandwidth rather than higher efficiency compared with Class-AB/B PAs [14] and the peak achieved efficiency follows the trend of Class-AB PAs.

Both Class-F<sup>-1</sup> and Class-F operation modes are promising for improving the PAE of the linear PAs near output 1-dB compression point ( $OP_{1dB}$ ) by tuning harmonic components. From Table 2-1, by tuning up to 3<sup>rd</sup> harmonic the achievable peak power efficiency is ~90% before circuit non-ideal effects.

Assuming up to 3<sup>rd</sup> harmonic control Fig. 2-6 (a) and Fig. 2-6 (b) shows the ideal current and voltage time-domain waveforms for Class-F<sup>-1</sup> and Class-F PAs with the same fundamental components which results in a same output power from both PAs. The waveforms are also normalized to their peak value which are limited to the break-down voltage and peak  $f_T$  current density of the power device for the voltage waveforms and current waveform, respectively. Regarding the harmonic load impedances, the normalized rectangular waveform corresponds to

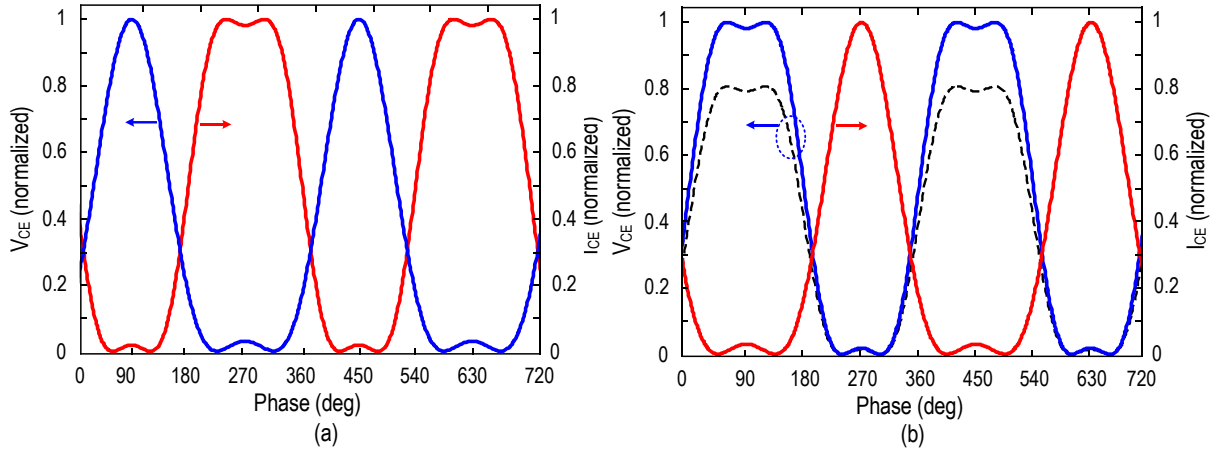
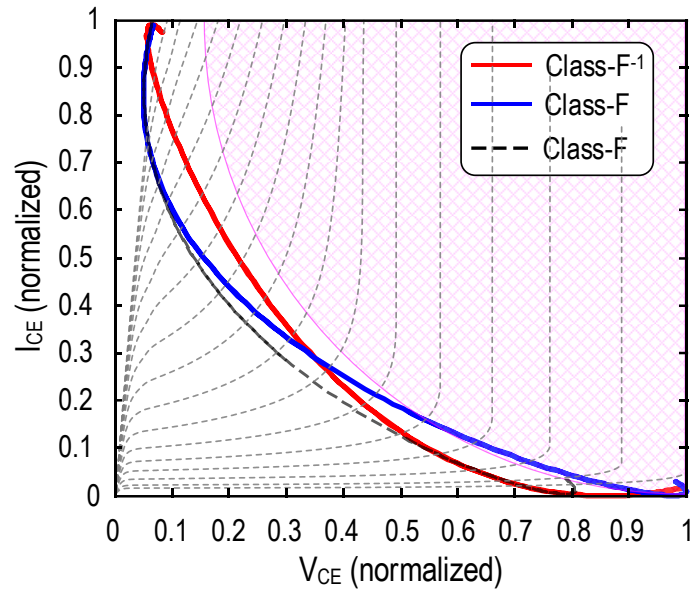


Fig. 2-6 Voltage and current waveforms for an ideal Class-F and Class-F<sup>-1</sup>PA, normalized to the break-down voltage (5.9 V) and peak current (95 mA): (a) waveforms for Class-F-1, (b) waveforms for Class-F.

current waveform for Class-F<sup>-1</sup> and voltage waveform for Class-F. The half-sinusoidal waveform corresponds to the voltage waveform for Class-F<sup>-1</sup> and current waveform for Class-F. The peak efficiency of both PAs are same since the overlap of the waveforms are same which results in equal power dissipation. Therefore, the Class-F<sup>-1</sup> and Class-F PAs ideally have same large signal performance. However, practical implementation should consider device voltage-current limits and low-quality passives for choosing the best architecture to achieve high efficiency performance at mm-wave.

Fig. 2-7 shows the ac-loadline of the Class-F<sup>-1</sup> and Class F PAs, typical  $V_{knee} = 0.4$  V is considered for both PAs based on simulations. The DC current-voltage (I-V) curves of the HBT transistor in 0.13  $\mu$ m BiCMOS are also normalized to peak current and breakdown voltage based on GF PDK simulation results. The red hatched area shows the device breakdown region which should not be crossed by ac-loadline of the PAs due to reliability issues. As Fig. 2-7 shows, when  $V_{CE} > 0.5 \cdot V_{Breakdown}$  the ac-loadline is in the breakdown region while the Class-F<sup>-1</sup> PA is always operating in the safe region. In order to have Class-F PA operating in reliable region the voltage swing should be scaled down. The dashed black line shows the voltage waveform and ac-loadline for a Class-F PA when the voltage swing is scaled down by a factor of 0.8 and so does the peak voltage. Therefore, the peak achievable output power reduce by  $\sim 1$  dB. The power efficiency reduces as well since practically the knee voltage does not change with voltage scaling and thus becomes greater fraction of the fundamental voltage component after voltage scaling.



(c)

Fig. 2-7 Ac- load line of the Class-F<sup>-1</sup> and Class-F PAs corresponding to the voltage and current waveforms of Fig. 2-5

At mm-wave frequencies the quality factor of the passive components is another limiting factor for achieving peak PAE. As frequency increases, the quality factor of the passive components reduces due to skin effect and substrate coupling. Therefore, providing high impedance ( $>2.5R_{OPT}$ ) becomes more challenging as frequency increases. Providing proper high impedance is critical for shaping voltage waveform and achieving high efficiency performance. In Class-F<sup>-1</sup> PA, the load network should provide high impedance at 2<sup>nd</sup> harmonic while in Class-F the 3<sup>rd</sup> harmonic load should be high impedance. Therefore, practically at mm-wave frequencies it is less challenging to provide proper harmonic termination for Class-F<sup>-1</sup> and achieve high efficiency compared with Class-F PAs.

## 2.6 Summary

This chapter gives an overview of the different classes of power amplifiers and the major efficiency and linearity metrics of the PAs. The state-of-the-art mm-wave SiGe BiCMOS PAs reported in literature are introduced. This chapter also compares the Class-F and Class-F<sup>-1</sup> harmonic tuning approaches considering the gain and load limitations at mm-wave frequencies..



# 3 High efficiency mm-wave Class F<sup>-1</sup> PA with LC harmonic tuning load

## 3.1 Introduction

Harmonically tuned amplifier topologies, classified as class-F and inverse class-F (F<sup>-1</sup>), are widely investigated to achieve a high power efficiency in high frequency power amplifiers (PAs) [8]-[10], [15]-[17]. In ideal class-F PAs, by terminating all odd and even harmonic impedances to be open-circuit and short-circuit, respectively, the PAs can shape a *rectangular* voltage and *half-sinusoid* current waveform at the collector (or drain) output. The circuit duality allows interchanging of the even and odd harmonics impedances, inverting the collector voltage and current waveform in ideal class-F<sup>-1</sup> PAs. Both architectures enable non-overlapped zero-voltage or zero-current switching. This completely eliminates the spectral power of any harmonic components, and thus leads to 100% power conversion efficiency from a DC supply to a fundamental radio frequency (RF) signal by a generator [16].

At high frequencies, the authentic circuit impedance control for the class-F or class-F<sup>-1</sup> waveform shaping is often opted for up to the 3<sup>rd</sup> harmonic of a fundamental frequency because higher than the 3<sup>rd</sup>-order harmonic impedance control may not be easy, nor be practical in terms of size and loss [15]-[16]. Prior state-of-the-art class-F or class-F<sup>-1</sup> PAs with the bi-harmonic (2<sup>nd</sup> and 3<sup>rd</sup> harmonic) impedance tuning exhibit outstanding power-added-efficiency (PAE) over 70% [18]-[22]. However, major design efforts have been focused on discrete PAs at RF by leveraging a packaged high-power transistor such as LDMOS FET or GaN HEMT [21], [22], or GaAs based MMIC implementation at microwave frequencies [7]. So far, little research effort has been exerted for realizing harmonically tuned integrated PAs in the silicon process. This is partly because for highly efficient integrated silicon PAs at RF, the class-F or class-F<sup>-1</sup> topology may not be an optimal choice over other switching-mode PAs due to the difficulty in realizing a high-Q LC resonance load network; a high passive component loss will sacrifice the power efficiency substantially and PAE improvement by the class-F or class-F<sup>-1</sup> topology may not be prominent at RF.

However, the passive component loss, mainly inductor loss, becomes smaller at microwave and higher frequencies thanks to the scale down of the passive components size. This provides a good opportunity of implementing low-loss and compact high-Q LC resonators for an optimal harmonic impedance modulation for the integrated class-F or class-F<sup>-1</sup> PAs. The class-F<sup>-1</sup> technique is particularly more attractive and effective than the class-F technique in achieving a high PAE at microwave and mm-Wave bands. This is because developing a high impedance at a 2<sup>nd</sup>-harmonic band will be much more robust to parasitic effects and less vulnerable to passive components Qs than at a 3<sup>rd</sup>-harmonic band at such high frequencies.

In this work, two class-F<sup>-1</sup> PAs employing a multi-resonance LC harmonic filter are designed at 24 GHz and 38 GHz in a SiGe BiCMOS technology to explore potentials and limitations of the harmonic tuning technique in achieving a high PAE at microwave and mm-Wave bands. The PAs produce 50-70 mW output power on a 50-Ω load at saturation, and achieve 50% and close to 40% PAEs at 24 GHz and 38 GHz, respectively, some of the highest PAEs reported so far in integrated PAs in both silicon and III-V technologies. The saturated output power has been defined optimally and maximally to the extent that a power transistor can sustain the output power without suffering breakdown, and at the same time, maintain a high  $f_T$  ( $> 180$  GHz) in the given 0.13-μm SiGe BiCMOS technology. Namely, the  $P_{sat}$  is the outcome of a compromise between the output power and device speed, which is an ingrained tradeoff in silicon technologies. Larger output power could be produced by aggregating the output power with configuring a PA array utilizing the proposed designs as a unit PA cell.

### 3.2 Inverse Class-F Power Efficiency Limiting Factors

Let  $i_{fund}$  and  $v_{fund}$  be peak magnitudes of fundamental current and voltage components at a generator output, then collector (or drain) efficiency will be

$$\eta_c = \frac{1}{2} \left( \frac{i_{fund}}{I_{DC}} \right) \left( \frac{v_{fund}}{V_{DC}} \right). \quad (3 - 1)$$

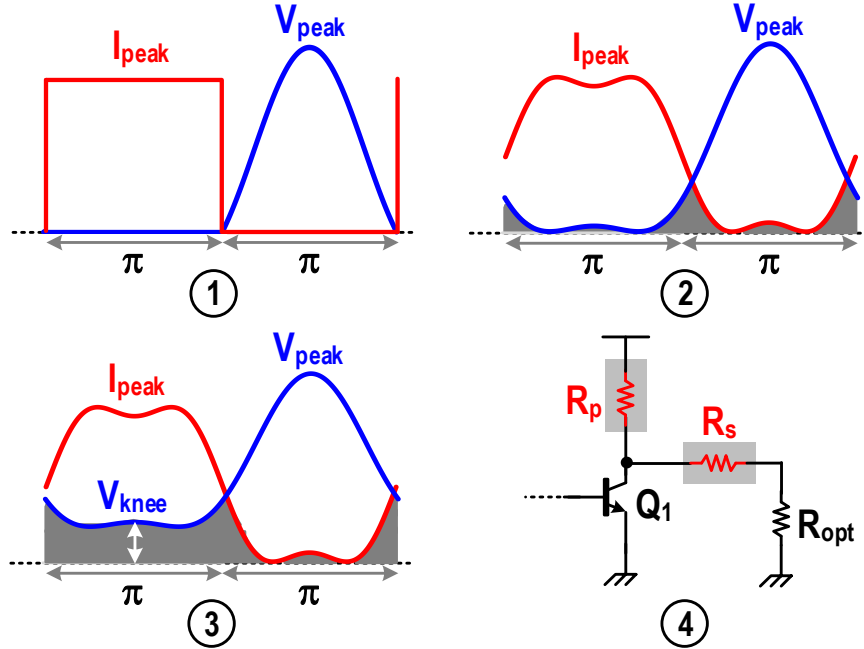


Fig. 3-1. PAE limiting factors in the inverse class-F PAs: ①-ideal non-overlapped inverse class-F V/I waveforms; ②-finite number of harmonic impedance control; ③-finite knee voltage in the power transistor; and ④-finite resistive losses from parallel resonance load ( $R_p$ ) and series resonance load ( $R_s$ ) at  $f_0$ .

$V_{DC}$  and  $I_{DC}$  are DC voltage and current, respectively. In ideal non-overlapped rectangular current and half-sinusoidal voltage waveforms, shown in Fig. 3-1①,  $i_{fund}/I_{DC} = 4/\pi$  and  $v_{fund}/V_{DC} = \pi/2$ , resulting in 100%  $\eta_c$ .

### 3.2.1 Finite Number of Harmonics Control

In reality, only finite number of harmonics will be present at the generator load due to the band limiting nature of a passive load, causing nontrivial collector voltage and current overlap in Fig. 3-1②, where the generator dissipates an active power. When restricting the harmonics control up to the 3<sup>rd</sup> of a fundamental frequency, the following class-F<sup>-1</sup> collector voltage and current polynomials have been suggested for the maximum efficiency [16]:

$$v_{CE}(\theta) = V_{DC} \left( 1 - \sqrt{2} \cos\theta + \frac{1}{2} \cos 2\theta \right) \quad (2-3)$$

and

$$i_{CE}(\theta) = I_{DC} \left( 1 - \frac{2}{\sqrt{3}} \cos\theta + \frac{1}{3\sqrt{3}} \cos 3\theta \right) \quad (3-3)$$

, which results in

$$\eta_{c,max} = \frac{1}{2} \left( \frac{i_{fund}}{I_{DC}} \right) \left( \frac{v_{fund}}{V_{DC}} \right) = \frac{1}{2} \times \frac{2}{\sqrt{3}} \times \sqrt{2} = 0.816. \quad (3-4)$$

### 3.2.2 Finite Knee Voltage, $V_{knee}$

The efficiency will be decreased further because of the finite knee voltage of a power transistor ( $Q_1$ ),  $V_{knee}$  in Fig. 3-1(3). To investigate the  $V_{knee}$  effect on the efficiency, let's redefine the collector voltage as

$$v_{CE}(\theta) = V_{DC} - v_{fund} \cos \theta + v_{2nd} \cos 2\theta, \quad (3-5)$$

where  $v_{2nd}$  is peak magnitude of the 2<sup>nd</sup> harmonic component of the collector voltage waveform. In the half-sinusoid voltage, the minimum of (3-5) needs to be  $V_{knee}$  and at the minimum points should be flat for a maximum flatness during the half cycle, imposing the signal condition of  $v_{CE,min} = v_{CE}(\theta_o) = V_{knee}$  and  $\partial v_{CE}(\theta)/\partial \theta = 0$  at  $\theta = \theta_o$ .  $\theta_o$  is the angle where the collector voltage reaches its minimum value. This enforces the following relationships:

$$V_{DC} - v_{fund} \cos \theta_o + v_{2nd} \cos 2\theta_o = V_{knee} \quad (3-6)$$

and

$$\frac{\partial v_{CE}(\theta)}{\partial \theta} = 0 \text{ at } \theta = \theta_o \text{ } (-\pi \leq \theta_o \leq \pi) \Rightarrow \begin{cases} \cos \theta_o = \frac{v_{fund}}{4v_{2nd}}, \text{ if } \frac{v_{2nd}}{v_{fund}} > \frac{1}{4} \\ \theta_o = 0, \text{ if } \frac{v_{2nd}}{v_{fund}} < \frac{1}{4} \end{cases}. \quad (3-7)$$

Plugging (3-7) into (3-6) gives

$$\frac{v_{fund}}{V_{DC}} = \begin{cases} \left( 1 - \frac{V_{knee}}{V_{DC}} \right) \left( \frac{v_{2nd}}{v_{fund}} + \frac{v_{fund}}{8v_{2nd}} \right)^{-1}, \text{ if } \frac{v_{2nd}}{v_{fund}} > \frac{1}{4} \\ \left( 1 - \frac{V_{knee}}{V_{DC}} \right) \left( 1 - \frac{v_{2nd}}{v_{fund}} \right)^{-1}, \text{ if } \frac{v_{2nd}}{v_{fund}} < \frac{1}{4} \end{cases}. \quad (3-8)$$

Consequently,  $\eta_c$  will be

$$\eta_c = \frac{1}{2} \times \frac{2}{\sqrt{3}} \times \begin{cases} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \left(\frac{v_{2nd}}{v_{fund}} + \frac{v_{fund}}{8v_{2nd}}\right)^{-1}, & \text{if } \frac{v_{2nd}}{v_{fund}} > \frac{1}{4} \\ \left(1 - \frac{V_{knee}}{V_{DC}}\right) \left(1 - \frac{v_{2nd}}{v_{fund}}\right)^{-1}, & \text{if } \frac{v_{2nd}}{v_{fund}} < \frac{1}{4} \end{cases} \quad (3-9)$$

In (3-9), the maximum efficiency happens when  $v_{2nd}/v_{fund} = 1/2\sqrt{2} \cong 0.354$ , and is given by

$$\eta_{c,max} = 0.816 \times \left(1 - \frac{V_{knee}}{V_{DC}}\right). \quad (3-10)$$

The optimal collector voltage waveform including the knee voltage will be

$$v_{CE}(\theta) = V_{DC} \left\{ 1 - \sqrt{2} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \cos\theta + \frac{1}{2} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \cos 2\theta \right\}. \quad (3-11)$$

Apparently, when  $V_{knee} = 0$  (3-11) will be reduced to (3-2).  $V_{DC}$  depends on output power and is limited strictly by a device breakdown voltage ( $V_{BK}$ ) which is relatively low and traded with speed in the silicon process. Thus, the efficiency could be restricted severely by the knee voltage in high frequency silicon power amplifiers, particularly when the output power level is not high. For instance, if  $V_{DC}=2.3$  V and  $V_{knee}=0.4$  V, then theoretical maximum collector efficiency would be limited to around 67.4%.

### 3.2.3 Transistor Breakdown Voltage, $V_{BK}$

More complete expression on the collector efficiency can be derived when the maximum output signal is bounded by a breakdown voltage as following. In (3-5), the maximum happens when  $\theta = \pm\pi$  but is capped to  $V_{BK}$ , conditioning

$$v_{CE,max} = V_{DC} + v_{fund} + v_{2nd} = V_{BK}, \quad (3-12)$$

which can be processed further as

$$V_{DC} + v_{fund} + v_{2nd} - V_{knee} = V_{BK} - V_{knee}$$

$$\rightarrow 1 - \frac{V_{knee}}{V_{DC}} = \frac{\frac{V_{BK}}{V_{DC}} \cdot \left(1 - \frac{V_{knee}}{V_{BK}}\right)}{1 + \left(1 + \frac{v_{2nd}}{v_{fund}}\right) \left(\frac{\frac{v_{fund}}{V_{DC}}}{1 - \frac{V_{knee}}{V_{DC}}}\right)}. \quad (3-13)$$

Since at the maximum  $\eta_c$   $v_{2nd}/v_{fund} = 1/2\sqrt{2}$  and  $v_{fund}/V_{DC} = \sqrt{2} \cdot (1 - V_{knee}/V_{DC})$ , (3-13) is simplified to

$$1 - \frac{V_{knee}}{V_{DC}} = \frac{1}{1.5 + \sqrt{2}} \times \frac{V_{BK}}{V_{DC}} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right) \cong 0.343 \times \frac{V_{BK}}{V_{DC}} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right). \quad (3-14)$$

The substitution of (3-14) into (3-10) leads to

$$\eta_{c,max} = 0.28 \times \frac{V_{BK}}{V_{DC}} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right). \quad (15)$$

In continuing the previous example, when  $V_{BK}=5.9$  V,  $V_{DC}=2.3$  V, and  $V_{knee}=0.4$  V,  $\eta_{c,max}$  becomes 67%, a slight decrease compared with the unbounded case. Fig. 3-2 shows  $\eta_c$  versus  $v_{2nd}/v_{fund}$  in two cases: a solid line for the ideal case ( $V_{knee}=0$  and  $V_{BK}=\infty$ ) and a dot-line for a realistic case in this work ( $V_{knee}=0.4$  V and  $V_{BK}=5.9$  V). In this example, the peak voltage magnitude,  $V_{peak}$  in Fig. 1, is  $\sim 5.9$  V from (3-11).

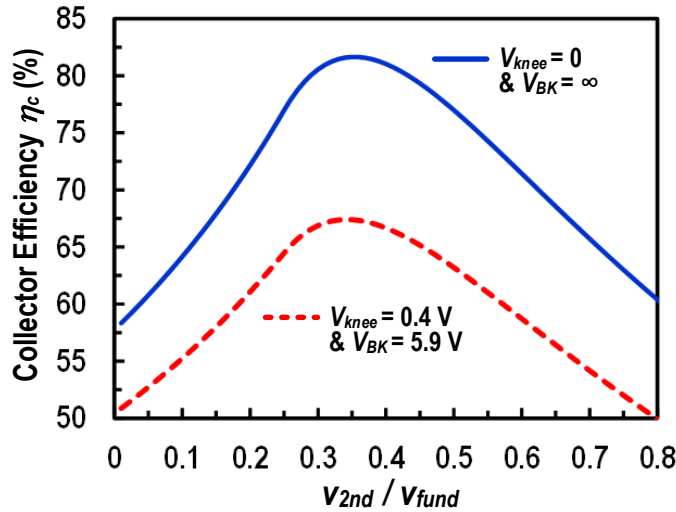


Fig. 3-2. Collector efficiency ( $\eta_c$ ) versus  $v_{2nd}/v_{fund}$ .

### 3.2.4 Resistive Losses from Passive Load Network

So far, it has been assumed that the class-F<sup>-1</sup> passive load network is ideal with no loss from the load. This could be a valid assumption in discrete PA designs on a printed-circuit board, where extremely high Q off-the-shelf Ls and Cs would be readily available. However in integrated PAs, particularly in the silicon process, the passive load suffers from substantial loss because of a limited Q from the integrated passive components. In Fig. 3-1④,  $R_p$  and  $R_s$  represent equivalent loss resistances at a fundamental frequency from the parallel and series loads, respectively.  $R_{opt}$  is an optimum PA load. The resistor network divides collector current and voltage, dissipates DC power, and thus causes RF fundamental power loss ( $P_{loss}$ ) which can be expressed as

$$P_{loss} = \underbrace{\left( \frac{R_p}{R_p + R_s + R_{opt}} \right)}_{\text{current loss}} \cdot \underbrace{\left( \frac{R_{opt}}{R_s + R_{opt}} \right)}_{\text{voltage loss}}. \quad (3 - 16)$$

$P_{loss}$  is factored out by the current and voltage losses. When including this power loss, the peak collector efficiency in (3-15) will decrease to  $\eta_{c,max} \times P_{loss}$ .

In fact, the loss factors in (3-16) disclose a tradeoff in choosing  $R_{opt}$  to desensitize the impact of the passive components losses on the efficiency: namely, to minimize the current loss smaller  $R_{opt}$  is desirable, whereas larger  $R_{opt}$  is preferable in order to desensitize the effect of  $R_s$  on the voltage loss. The sensitivity of  $\eta_{c,max}$  on  $R_p$  can be evaluated systematically by a sensitivity function given as

$$S_{R_p}^{\eta_{c,max}} = \frac{R_p}{\eta_{c,max}} \times \frac{\partial \eta_{c,max}}{\partial R_p} = \left( 1 + \frac{R_p}{R_s + R_{opt}} \right)^{-1}. \quad (3 - 17)$$

Similarly, the sensitivity of  $\eta_{c,max}$  on  $R_s$  can be appreciated by

$$S_{R_s}^{\eta_{c,max}} = \frac{R_s}{\eta_{c,max}} \times \frac{\partial \eta_{c,max}}{\partial R_s} = - \left( 1 + \frac{R_{opt}}{R_s} \right)^{-1} \quad (3 - 18)$$

where negative sign manifests degradation of  $\eta_{c,max}$  with the increase of  $R_s$ . In general supply (or breakdown) voltage constraint silicon power amplifiers,  $R_{opt}$  tends to be small, typically ranging ~1's  $\Omega$  to ~10's  $\Omega$ , while  $R_p$  could be an order of magnitude higher than  $R_{opt}$ . When an output

impedance matching network is incorporated, the matching network loss could be noticeable and  $R_s$  could be comparable to  $R_{opt}$ . This implies that the efficiency degradation may be highly sensitive to  $R_s$ . For instance, if  $R_{opt}=20\ \Omega$  and  $R_s=5\ \Omega$ , then  $S_{RS}^{\eta_c, max} = -0.2$  from (3-18), claiming another efficiency reduction by 20% even if  $R_p$  is infinite. In this work, we choose  $R_{opt}=50\ \Omega$  to eliminate the impedance matching loss and thus to minimize the loss ( $R_s$ ) in the series signal path. This confines the maximum achievable output power for efficiency, revealing the tradeoff between output power and efficiency in a supply constraint integrated silicon PA.

### 3.2.5 Other Non-Idealities

A number of other non-idealities could affect the efficiency further. First, any deviation from the  $180^\circ$  conduction angle may alter the collector efficiency. This, however, does not necessarily degrade PAE since biasing slightly larger than *ideal* class-B, so-called *deep* class-AB biasing, will improve the power gain, resulting in a better PAE. In fact, due to the difficulty in defining an *exact* class-B bias point in practical designs, a common tactic for searching optimum bias point is to push the power transistor biasing gradually from a class-AB point toward *close enough* to a class-B operation while securing adequate gain, not to sacrifice the PAE in simulations.

Second, non-open 2<sup>nd</sup> harmonic impedance or non-zero 3<sup>rd</sup> harmonic impedance will spawn finite 2<sup>nd</sup> harmonic current and 3<sup>rd</sup> harmonic voltage spectrum, respectively, causing extra DC power dissipation by the generator and sacrificing efficiency thereof. Particularly, the non-ideal magnitude of 2<sup>nd</sup> harmonic impedance may result in a suboptimal  $v_{2m}/v_{1m}$  in (3-9), waning the achievable maximum efficiency lower than the  $\eta_{c, max}$  in (3-10).

Finally, for the sake of simplicity the order of controlled harmonics is limited up to a third order. However, higher-order harmonics could be load-pulled depending on the frequency response of a load network. If higher-order even or odd harmonics are present exclusively in the voltage or current waveform, not both, it could improve the waveform flatness and thus enhance efficiency. For instance, because of a natural low reactance by the parasitic load capacitance at high order harmonic frequencies in class-F<sup>-1</sup> PAs, the 5<sup>th</sup>-order harmonic current is often notable, as can be seen in section IV. When including the 5<sup>th</sup> harmonic current, [16] has suggested following numerical polynomial for the maximally flat current waveform:



$$i_{CE}(\theta) \cong I_{DC}(1 - 1.207 \cdot \cos\theta + 0.28 \cdot \cos3\theta - 0.073 \cdot \cos5\theta). \quad (3 - 19)$$

This increases the ratio of  $i_{fund}/I_{DC}$  from  $2/\sqrt{3} \cong 1.155$  in (3-3) to 1.207, and thereby enhances the  $\eta_{c,max}$  from 67% to 70% when taking into account a 5.9 V  $V_{BK}$  and 0.4 V  $V_{knee}$  in the previous example ( $V_{DC}=2.3$  V). However, if the higher order harmonics are present commonly in the collector voltage and current, it could create an active harmonic power. This will impair efficiency although the impairment may not be conspicuous due to a smallness of the higher-order harmonic power compared with the fundamental signal power.

### 3.3 Inverse Class-F Load Network

#### 3.3.1 Multi-Resonance Parallel Load

Fig. 3-3 (a) shows a multi-resonance load network driven by a frequency-dependent nonlinear current source emulating the power amplifiers output current.  $C_L$  represents the PA's output load capacitance including the generator's output parasitic capacitance and is presumed to have no frequency dependency. The LC tanks can be replaced equivalently with frequency-dependent inductors,  $L_{eq1}(\omega)$  in (3-20) and  $L_{eq2}(\omega)$  in (3-21), of which the inductance varies widely from a positive to a negative (or capacitive), depending on the operation frequency.

$$L_{eq1}(\omega) = \frac{L_1}{1 - (\omega/\omega_{o1})^2}, \text{ where } \omega_{o1} = 1/\sqrt{L_1 C_1}. \quad (3 - 20)$$

$$L_{eq2}(\omega) = \frac{L_2}{1 - (\omega/\omega_{o2})^2}, \text{ where } \omega_{o2} = 1/\sqrt{L_2 C_2}. \quad (3 - 21)$$

Explicit harmonic control is limited up to the 3<sup>rd</sup> harmonic of a fundamental frequency ( $\omega_o$ ) and the PA current is approximated to a nonlinear current, dependent on  $\omega_o$ ,  $2\omega_o$ , and  $3\omega_o$  in Fig. 3-3. Suppose that the local resonance frequencies by the  $L_1$ - $C_1$  tank ( $\omega_{o1}$ ) and  $L_2$ - $C_2$  tank ( $\omega_{o2}$ ) satisfy that  $\omega_o < \omega_{o1} < 2\omega_o < \omega_{o2} < 3\omega_o$ . Then, the equivalent circuits at  $\omega_o$ ,  $2\omega_o$ , and  $3\omega_o$  can be reconfigured as shown in Fig. 3-3 (b), (c), and (d), respectively.

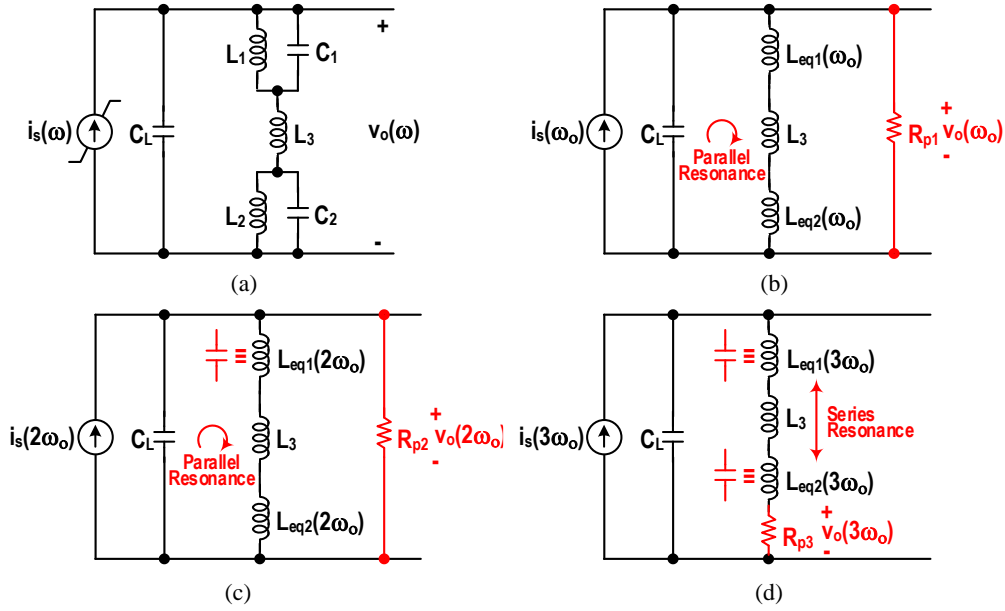


Fig. 3-3. (a) Multi-resonance parallel LC load network driven by a nonlinear current source emulating power amplifier output current, (b) equivalent load networks with a finite loss ( $R_{p1}$ ) at fundamental frequency ( $\omega_0$ ), (c) equivalent load networks with a finite loss ( $R_{p2}$ ) at 2<sup>nd</sup> harmonic ( $2\omega_0$ ), and (d) equivalent load networks with finite loss ( $R_{p3}$ ) at 3<sup>rd</sup> harmonic ( $3\omega_0$ ).

For an inverse Class-F operation, the choice of the passive components shall satisfy the following design equations:

$$L_{eq1}(\omega_0) + L_{eq2}(\omega_0) + L_3 = 1/(\omega_0^2 C_L), \quad (3-22)$$

$$L_{eq1}(2\omega_0) + L_{eq2}(2\omega_0) + L_3 = 1/(4\omega_0^2 C_L), \quad (3-23)$$

$$L_{eq1}(3\omega_0) + L_{eq2}(3\omega_0) + L_3 = 0. \quad (3-24)$$

(3-22) and (3-23) express the parallel resonances at  $\omega_0$  and  $2\omega_0$  in Fig. 3-3 (b) and (c), respectively. (3-24) indicates series resonance in the inductor branch in Fig. 3-3 (d). In Fig. 3-3,  $R_{p1}$  and  $R_{p2}$  represent effective tank losses after the resonances at  $\omega_0$  and  $2\omega_0$ .  $R_{p3}$  expresses a series loss in the series resonance path. For a given technology, different combinations of  $L_s$  and  $C_s$  will give different tank losses. The best practice for determining the optimum component set will be to choose the component combinations causing a power loss minimally in the passive networks.

This can be achieved by the following optimization process. First, for a given  $\omega_0$  we choose a particular set of  $\{\omega_{01}, \omega_{02}\}$  subjected to  $\omega_0 < \omega_{01} < 2\omega_0 < \omega_{02} < 3\omega_0$ . Then, using (3-22)-(3-24) we determine a components set of  $\{L_1, L_2, L_3, C_1, C_2\}$  and characterize corresponding  $R_{p1}$ ,  $R_{p2}$ , and  $R_{p3}$  through EM simulations. By sweeping  $\{\omega_{01}, \omega_{02}\}$  two dimensionally and repeating the loss

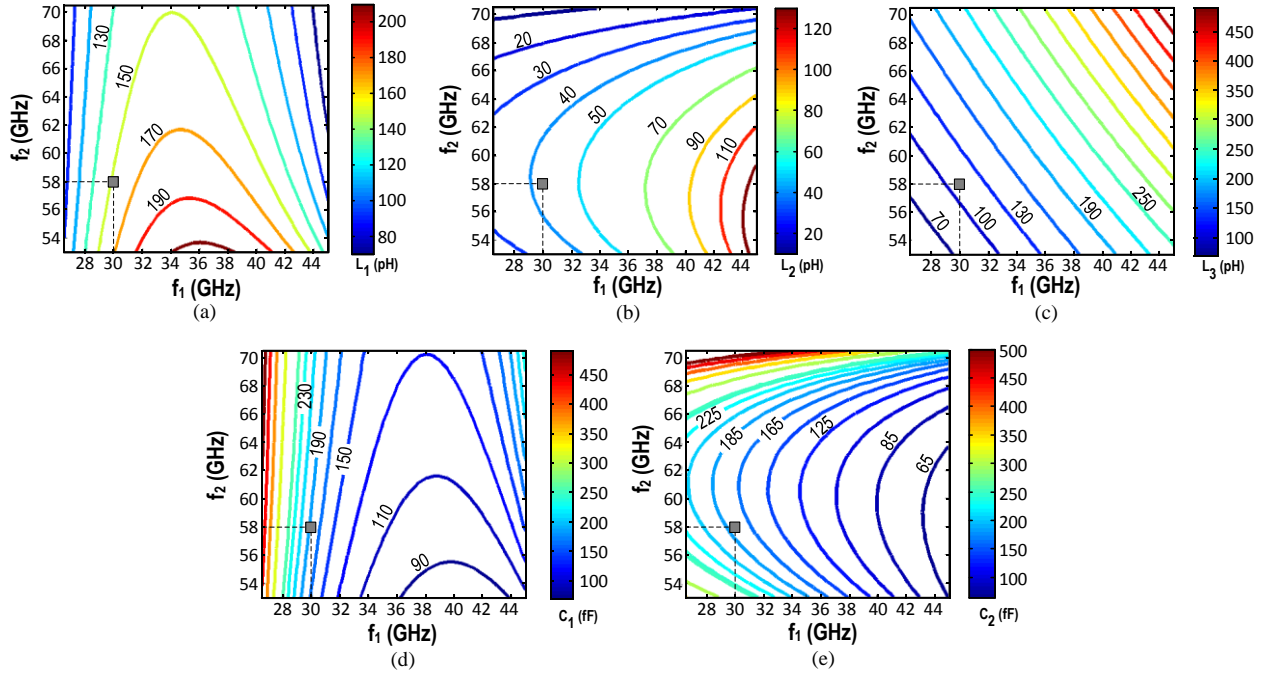


Fig. 3-4. Contour plots of the passive L and C components values as the function of  $\{f_1, f_2\}$  satisfying the equations of (23)-(25): (a)  $L_1$  (pH), (b)  $L_2$  (pH), (c)  $L_3$  (pH), (d)  $C_1$  (fF), and (e)  $C_2$  (fF).

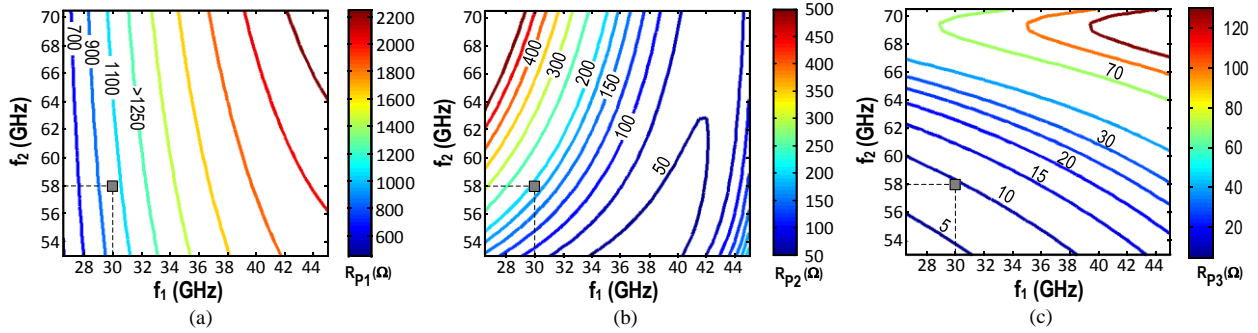


Fig. 3-5. Contour plots of equivalent loss resistances when  $\{L_1, L_2, L_3, C_1, C_2\}$  vary as in Fig. 3-4: (a)  $R_{P1}$ , (b)  $R_{P2}$ , and (c)  $R_{P3}$  in Fig. 3, respectively. The rectangular dot is the design point chosen in this work, i.e.  $f_1=30$  GHz and  $f_2=58$  GHz.

characterization for each components set, contour plots of the loss resistances can be obtained, and optimum design window for a minimum tank loss can be found graphically.

Fig. 3-4 and Fig. 3-5 illustrate this design process. Fig. 3-4 plots all possible combinations of  $\{L_1, L_2, L_3, C_1, C_2\}$  by sweeping  $f_{o1}$  ( $=\omega_{o1}/2\pi$ ) and  $f_{o2}$  ( $=\omega_{o2}/2\pi$ ). For 24 GHz PA, the range of  $f_o$  is  $23 \text{ GHz} < f_o < 25 \text{ GHz}$ , requiring two dimensional frequency sweeping of  $26 \text{ GHz} < f_{o1} < 47 \text{ GHz}$  and  $55 \text{ GHz} < f_{o2} < 72 \text{ GHz}$ .  $C_L$  is around 60-65 fF (*see next section*). Under the  $f_{o1}$  and  $f_{o2}$  sweepings, the ranges of the passive components are found by applying (22)-(24):  $80 \text{ pH} < L_1 <$

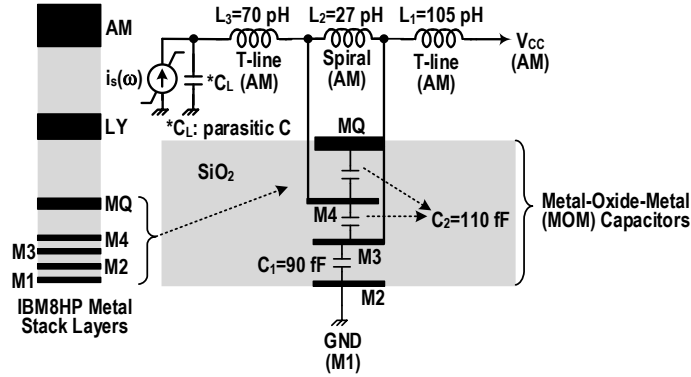


Fig. 3-6. IBM8HP SiGe BiCMOS process metal stack layers [26] and Implementation of the parallel multi-resonance load network for 38 GHz PA.

200 pH (Fig. 3-4 (a));  $10 \text{ pH} < L_2 < 120 \text{ pH}$  (Fig. 3-4 (b));  $15 \text{ pH} < L_3 < 200 \text{ pH}$  (Fig. 3-4 (c));  $40 \text{ fF} < C_1 < 200 \text{ fF}$  (Fig. 3-4 (d)); and  $50 \text{ fF} < C_2 < 500 \text{ fF}$  (Fig. 3-4 (e)).

In these variations of the passive components, typical on-chip spiral inductors' Q is 18 at the  $f_0$ -band, 21 at the  $2f_0$ -band, and 24 at the  $3f_0$ -band according to EM modeling. For T-line inductors, Q is  $\sim 35$  for all bands. The Q of MIM capacitors is typically 35 at the  $f_0$ -band, and diminishes to 25 at the  $2f_0$ -band and 12 at the  $3f_0$ -band. These component Qs are applied to estimate  $R_{P1}$ ,  $R_{P2}$ , and  $R_{P3}$  in first order. Fig. 3-5 shows the contour plot of  $R_{P1}$ ,  $R_{P2}$ , and  $R_{P3}$  versus  $\{f_1, f_2\}$ . As mentioned, a  $50\text{-}\Omega$  has been chosen for the PA's optimum load and the optimum design window are selected by the following criteria:  $R_{P1} > 20 \cdot R_{\text{opt}}$  ( $1 \text{ k}\Omega$ ),  $R_{P2} > 3 \cdot R_{\text{opt}}$  ( $150 \text{ }\Omega$ ), and  $R_{P3} < 0.2 \cdot R_{\text{opt}}$  ( $10 \text{ }\Omega$ ). The grey dots in Fig. 3-5 show the design point applied in this work, resulting in  $f_{o1}=30 \text{ GHz}$  and  $f_{o2}=58 \text{ GHz}$  and  $\{L_1, L_2, L_3, C_1, C_2\} = \{153 \text{ pH}, 43 \text{ pH}, 111 \text{ pH}, 184 \text{ fF}, 175 \text{ fF}\}$ .

The same optimization strategy has been applied for 38 GHz PA design ( $C_L=60 \text{ fF}$ ), resulting in  $\{f_{o1}, f_{o2}\}=\{50 \text{ GHz}, 90 \text{ GHz}\}$  and  $\{L_1, L_2, L_3, C_1, C_2\} = \{105 \text{ pH}, 27 \text{ pH}, 70 \text{ pH}, 90 \text{ fF}, 110 \text{ fF}\}$ . One particular distinction for the 38 GHz PA is that the MIM capacitors given in the library models suffer from a low Q at the target mm-Wave bands. So, as illustrated in Fig. 3-6, the MOM capacitors are custom made, utilizing BEOL lower metal layers and silicon dioxide as a dielectric to guarantee at least  $Q \sim 80$  at a fundamental frequency and  $Q > 20$  up to a 3<sup>rd</sup> harmonic band over 100 GHz. After setting the passive component values, full EM simulations have been conducted for a fine optimization and extraction of more exact loss resistances.

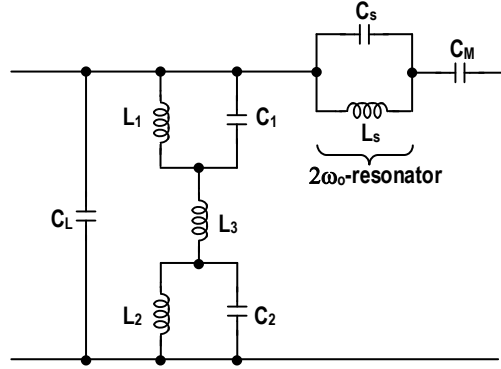


Fig. 3-7. Complete inverse Class-F load network by adding a series dual resonance network. The  $L_s$ - $C_s$  tank resonates at the  $2\omega_0$  band and at  $\omega_0$  band the effective inductance from the  $L_s$ - $C_s$  tank will be resonated with the  $C_M$ .

### 3.3.2 Dual-Resonance Series Load

Fig. 3-7 completes the inverse class-F load network by cascading a dual resonance series LC resonator with the multi-resonance parallel load described in the previous section. The role of the series network is obvious:  $L_s$ - $C_s$  tank resonates at  $2\omega_0$ , isolating a PA load from the generator at the second harmonic band to maintain a high impedance at the generator's collector node. At a  $\omega_0$ -band, the  $2\omega_0$ -resonator becomes inductive ( $\sim 4/3 \cdot L_s$ ) which is resonated out in series with  $C_M$ , enabling the PA to fully deliver an active power to the PA's optimum load. As in the parallel load, to minimize the loss in the series path, the choice of the passive component needs an iterative optimization. For a high Q, the  $L_s$ - $C_s$  tank is implemented with the custom-made MOM capacitor as illustrated in Fig. 3-6.

TABLE 3-1 and TABLE 3-2 summarize the optimized passive component values and major parasitic resistances characterized with EM simulations including output RF pad. With eliminating output impedance matching circuit and by a careful optimization, the effective  $R_s$  is suppressed to below  $2 \Omega$  at 24 GHz and below  $3 \Omega$  at 38 GHz.  $R_{p1}$  is 1 k $\Omega$  and 0.9 k $\Omega$  at 24 GHz and 38 GHz, respectively. From (3-16), the  $P_{loss}$  is estimated to 0.914 at 24 GHz and 0.891 at 38 GHz. Thus, in continuing the previous example ( $V_{BK} = 5.9 V$ ,  $V_{knee} = 0.4 V$ , and  $V_{DC} = 2.3 V$ ) with assuming the bi-harmonic control, the maximum achievable collector efficiency can be estimated as

$$\eta_{c,max} = 67\% \times P_{loss} = 61.2\% @24 \text{ GHz and } 59.7\% @38 \text{ GHz.} \quad (3 - 25)$$

TABLE 3-1. Summary of the passive values of the class-F<sup>-1</sup> load network

	C <sub>1</sub> (fF)	L <sub>1</sub> (pH)	L <sub>2</sub> (pH)	L <sub>3</sub> (pH)	C <sub>1</sub> (fF)	C <sub>2</sub> (fF)	L <sub>s</sub> (pH)	C <sub>s</sub> (fF)
24 GHz PA	65	153	43	111	184	175	108	100
38 GHz PA	60	105	27	70	90	110	70	65

TABLE 3-2. Summary of the equivalent parasitic resistances

	R <sub>p1</sub> (Ω) @f <sub>0</sub>	R <sub>p2</sub> (Ω) @2f <sub>0</sub>	R <sub>p3</sub> (Ω) @3f <sub>0</sub>	R <sub>s</sub> (Ω) @f <sub>0</sub>	R <sub>s</sub> (Ω) @2f <sub>0</sub>
24 GHz PA	1000	240	5	2	480
38 GHz PA	900	200	6	3	420

The  $\eta_{c,max}$  increases by a few % when the current waveform contains an ideal 5<sup>th</sup> harmonic content in (3-19), resulting in

$$\eta_{c,max} = 70\% \times P_{loss} = 64\% @24 \text{ GHz and } 62.4\% @38 \text{ GHz.} \quad (3 - 26)$$

It is important to guarantee the validity of the passive components models up to at least the 3<sup>rd</sup> harmonics of the design frequencies for the integrity of the 2<sup>nd</sup> and 3<sup>rd</sup> harmonics impedance control. For this, individual passive components are modeled with 2-port S-parameters valid up to ~240 GHz using the EM field solver.

### 3.4 Two-Stage Class-F<sup>-1</sup> Power Amplifier Design

Fig. 3-8 shows the proposed two-stage 24 GHz power amplifier comprised of a class-AB driving amplifier followed by an inverse class-F output PA which adopts the harmonically tuned load described in the previous section. Target saturated output power ( $P_{sat}$ ) is in the range of 50-70 mW, a compromise for the best PAE performance. The design step is first to design the output stage to produce the required  $P_{sat}$  with a maximum possible PAE. Then, based on a saturated power gain, the class-AB driver is designed to deliver an optimum inter-stage driving power to the output stage, followed by the design of an inter-stage matching network that concurrently meets an optimum power matching between the driver and the output PA with a maximum PAE in the driver stage as well.

#### 3.4.1 Inverse Class-F Output Power Amplifier

##### 3.4.1.1 Circuit Design

To produce 17-18 dBm of 1-dB compressed output power ( $OP_{-1dB}$ ) on 50-Ω  $R_{opt}$ , the required fundamental peak voltage swing is 2.3-2.4 V. In order to meet the peak swing requirement after

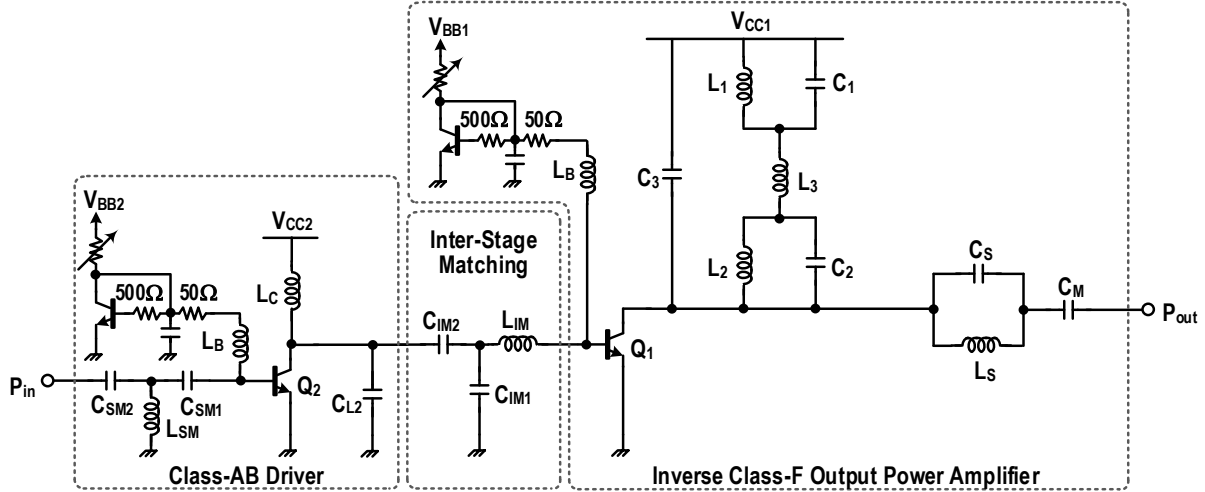


Fig. 3-8. Schematic of the 2-stage power amplifier, cascade of Class-AB driver followed by inverse Class-F output stage. Inter-stage matching is applied to achieve an optimum power delivery to the PA with a maximum PAE in the driver.

taking 400-450 mV  $V_{knee}$  into account, the optimum supply voltage,  $V_{DC}$  from (3-11), is in the range of 2.3-2.4 V ( $V_{CC1}$  in Fig. 3-8). This will create a maximum of about 5.9 V of sinusoidal peaking at the collector of  $Q_1$ . In the given 0.13- $\mu\text{m}$  SiGe BiCMOS technology, the  $BV_{CEO}$  of a SiGe HBT is 1.8 V. However, in practical circuit designs the base node will not be open but terminated with a finite resistance by a DC bias network which provides a discharging path from the base to ground, preventing the base charge accumulation and thus avoiding the early collector impact ionization [27], [27]. Realistically, in such circumstance the breakdown voltage of the transistor would be limited by  $BV_{CBO}$ . The  $BV_{CBO}$  of the given SiGe HBT technology is 6 V [26], relieving the reliability issue when developing the target  $P_{sat}$  over the 50- $\Omega$  load.

In Fig. 3-8, the base of  $Q_1$  ( $l_e=2\times 16.5\ \mu\text{m}$  for 24 GHz,  $l_e=2\times 14.5\ \mu\text{m}$  38 GHz) is biased at  $\sim 0.83$  V ( $V_{BB1}$ ), conducting  $\sim 8$  mA of quiescent collector current and pushing  $Q_1$  into a deep class-AB point when driven by 0 dBm input power ( $P_{in}$ ). The size of  $Q_1$  is optimized to have a current density of  $J_c=1.4$  mA/ $\mu\text{m}$  to achieve a peak 180 GHz  $f_T$  at 15 dBm OP-1dB ( $I_{DC}=40$  mA). This maintains  $\sim 9.5$  dB power gain ( $G_p$ ) at 24 GHz and 7 dB  $G_p$  at 38 GHz until the output reaches 1-dB gain compression point. The base bias path provides  $< 150\ \Omega$  of DC resistance to prevent the early collector breakdown. The  $\sim 0.5$  nH of  $L_B$  is realized by a narrow or meandered transmission line for a small form factor (*see chip photographs in Section V*) and isolates the bias circuit from  $Q_1$  in AC-wise. Therefore, the bias circuit causes negligible loading to the amplifier. Once establishing the  $Q_1$  size and bias conditions ( $V_{CC1}=2.3$  V), a series of DC, AC load lines and load

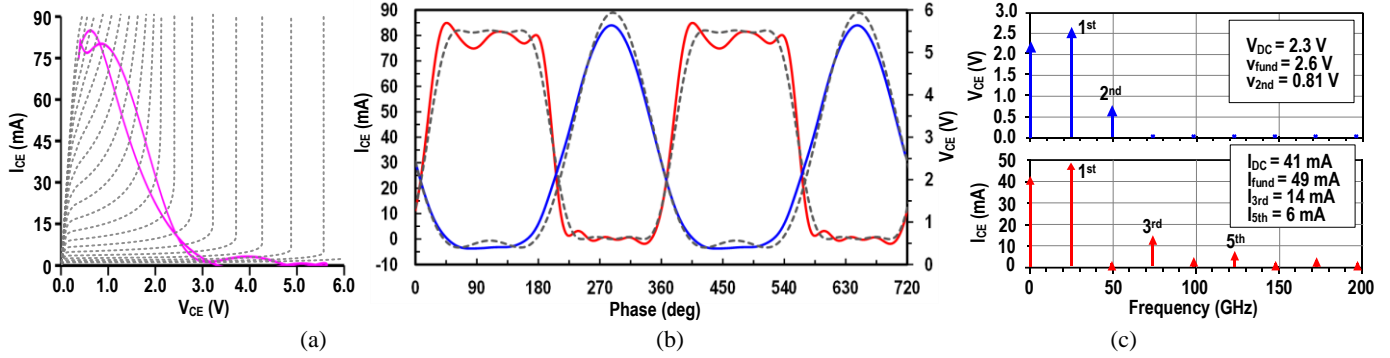


Fig. 3-9. Time domain simulation results for 24 GHz PA at  $P_{out}=18$  dBm ( $OP_{-1dB}$ ): (a) AC load line, (b) collector voltage and current waveforms, and (c) spectrum of the collector voltage and current. In the time domain V-I waveforms, dot lines are ideal class-F<sup>-1</sup> waveforms based on (3-20) and (3-11) for the current and voltage, respectively, where  $V_{knee}=0.4$  V.

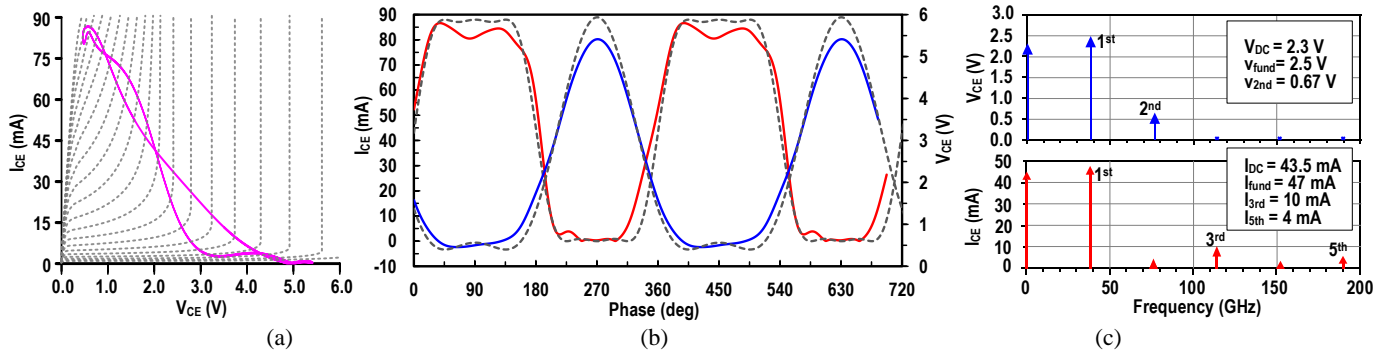


Fig. 3-10. Time domain simulation results for 38 GHz PA at  $P_{out}=17.5$  dBm ( $OP_{-1dB}$ ): (a) AC load line, (b) collector voltage and current waveforms, and (c) spectrum of the collector voltage and current. In the time domain V-I waveforms, dot lines are ideal class-F<sup>-1</sup> waveforms based on (3-20) and (3-11) for the current and voltage, respectively, where  $V_{knee}=0.4$  V.

pull simulations are conducted, which estimates  $\sim 800 \Omega$  of the transistor's large signal output resistance and 60-65 fF of parasitic output load capacitance ( $C_3$ ). About 15 fF of parasitic capacitance stemmed from the layout interconnects are modeled using an EM field solver [29] and absorbed into  $C_3$  in Fig. 3-8.

### 3.4.1.2 Time-domain Simulation Waveform Analysis

The CAD simulation results on the AC load lines at the output stage collector node, time-domain V-I waveforms, and corresponding spectrum analyses are shown in Fig. 3-9 and Fig. 3-10 for 24 GHz and 38 GHz PAs, respectively. In the simulations, the output power is 18 dBm for 24 GHz PA and 17.5 dBm for 38 GHz PA. In the time domain waveforms in Fig. 3-9 (b) and Fig. 3-10 (b), dot lines are ideal current and voltage waveforms based on (3-19) and (3-11), respectively, where  $V_{knee} \approx 0.4$  V. In the current spectra, analyzed in Fig. 3-9 (c) and Fig. 3-10 (c), due to a natural short-like capacitive impedance contributed by the PA load at high-order harmonic frequencies, non-negligible 5<sup>th</sup> harmonic current spectra is observed for both PAs. This enhances the transition



sharpness of the current switching, shaping better rectangular waveform which is fairly well matched with the ideal curves, and thus improving  $\eta_c$ . Note that this is a unique benefit in class-F<sup>1</sup> PAs, since in class-F PAs it requires a large impedance at the 5<sup>th</sup> harmonic frequency to shape similar quality rectangular voltage waveform, which will be much more challenging task than creating a low impedance because of increasing passive component loss at higher order harmonic bands.

The native low reactance effectively terminates the voltage spectra that are higher than the 2<sup>nd</sup> harmonic, shaping the  $2\omega_0$  induced half-sinusoidal voltage peaking. The  $v_{2nd}/v_{fund}$  is ~0.29 at 24 GHz and 0.26 at 38 GHz, while the optimal value is ~0.354 based on the analysis in (3-9), which causes about 0.4-0.5 V smaller peaking than the ideal 5.9 V<sub>peak</sub>. From the spectrum analyses,  $\eta_c=67.5\%$  at 24 GHz and  $\eta_c=58.7\%$  at 38 GHz at the collector node of each PA. The efficiency is, however, decreased on the 50- $\Omega$  R<sub>opt</sub> due to the power loss caused by a finite Q of the load network. When considering  $P_{loss}=0.914$  at 24 GHz and 0.891 at 38 GHz, the net collector efficiency becomes  $\eta_c=61.7\%$  at 24 GHz and  $\eta_c=52.3\%$  at 38 GHz. Compared with the theoretical estimation in (3-26), the simulation result at 24 GHz is only 2.3% less than the theoretical value. Because of the finite unity current gain frequency ( $f_T$ ), the current driving capability ( $g_m$ ) of the power transistor becomes smaller as the frequency increases. Further, because of lower 2<sup>nd</sup> harmonic impedance, the 2<sup>nd</sup> harmonic voltage is smaller at 38 GHz in Fig 10 than at 24 GHz in Fig. 3-9. These claim more DC power at 38 GHz than at 24 GHz to develop similar P<sub>out</sub> and harmonic voltage and current contents, diminishing the collector efficiency and thus widening the error from a theoretical maximum: the  $\eta_c$  at 38 GHz is about 10% lower than the theoretical value.

Since the power gain is 9.5 dB at 24 GHz and 7 dB at 38 GHz, the PAE will be 56% and 42% at 24 GHz and 38 GHz, respectively, which agrees well with the load-pull simulation results shown in Fig. 3-11. Apparently, the limited power gain due to insufficient  $f_T$  or  $f_{max}$  of the silicon transistor reduces the PAE substantially from the collector efficiency, causing about 6% and 10% efficiency reduction from the  $\eta_{c,max}$  at 24 GHz and 38 GHz, respectively.

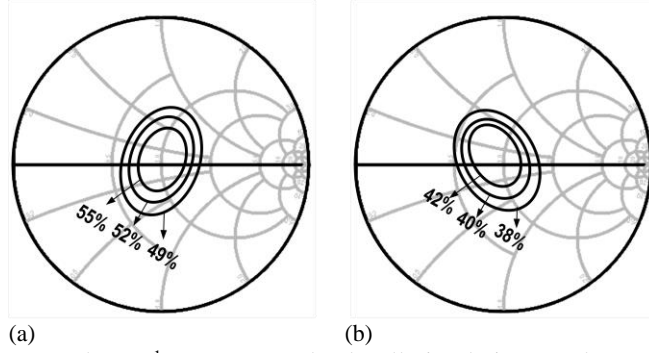


Fig. 3-11. Output class-F<sup>-1</sup> stages PAE load-pull simulation results: (a) 24 GHz PA (output stage gain: 9.5 dB and  $\eta_c=61\%$  on  $50\text{-}\Omega R_{opt}$ ) and (b) at 38 GHz PA (output stage gain: 7 dB and  $\eta_c=51.5\%$  on  $50\text{-}\Omega R_{opt}$ ).

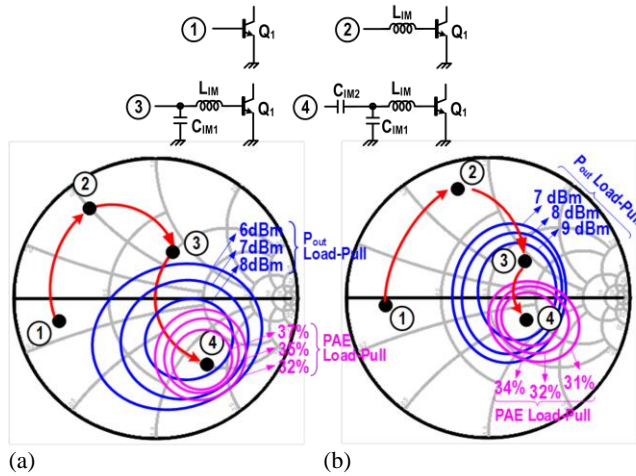


Fig. 3-12. Load-pulls ( $P_{out}$  and PAE) design of the interstage impedance matching network to achieve an optimum interstage power delivery with a maximum PAE in the class-AB driver: (a) 24 GHz PA (inter-stage gain: 9.5 dB and  $\eta_c=41.5\%$ ) and (b) 38 GHz PA (inter-stage gain: 8 dB and  $\eta_c=40\%$ )

### 3.4.2 Class-AB Driving Amplifier

The tuned common-emitter driver in Fig. 8 is biased at a class-AB point ( $V_{BB2}=0.83\text{ V}$  and  $I_{CE,Q2}=3.2\text{ mA}$ ). The size ( $l_e=10\text{ }\mu\text{m}$  for 24 GHz PA,  $l_e=16\text{ }\mu\text{m}$  for 38 GHz PA) and supply voltage ( $V_{CC2}=2\text{ V}$  for 24 GHz PA,  $V_{CC2}=1.5\text{ V}$  for 38 GHz PA) of  $Q_2$  are optimized to drive the output power stage to saturation when the driver output power reaches near 1-dB compression point (7 dBm @24 GHz PA, 8 dBm @38 GHz PA), resulting in a high PAE (37% @ 24GHz PA, 34% @38 GHz PA) from the driver. Input is matched to  $50\text{ }\Omega$  using T-network composed of the transmission (T)-line inductor  $L_{SM}$  and MIM capacitors,  $C_{SM1}$  and  $C_{SM2}$ . The T-line inductor  $L_C$  resonates out

TABLE 3-3. Summary of the passive values in the driving stages

	Input Matching			Driver Load		Inter-Stage Matching		
	C <sub>SM1</sub> (fF)	C <sub>SM2</sub> (fF)	L <sub>SM</sub> (pH)	L <sub>c</sub> (pH)	C <sub>L2</sub> (fF)	L <sub>IM</sub> (pH)	C <sub>IM1</sub> (fF)	C <sub>IM2</sub> (fF)
24 GHz PA	105	170	223	350	32	165	115	51
38 GHz PA	90	130	150	220	38	130	100	60

only a portion of C<sub>L2</sub> to provide a capacitive impedance at  $\omega_0$ , which is necessary to achieve simultaneous matching for both optimum output power and maximum efficiency. In Fig. 3-12 the impedance locus on the Smith Chart which is dependent on the inter-stage matching elements is illustrated in a step-by-step manner.

In the inter-stage matching network formed by the T-line inductor L<sub>IM</sub> and MIM capacitors, C<sub>IM1</sub> and C<sub>IM2</sub>, in Fig. 3-8, L<sub>IM</sub> and C<sub>IM1</sub> establish an optimum power matching. This matching network transforms the small impedance seen from the base of Q<sub>1</sub> in Fig. 3-12 ① to an optimum power impedance point in Fig. 3-12 ③, thus driving the PA output stage with > 8-9 dBm of inter-stage power. In order to achieve the highest possible PAE in the driver, C<sub>IM2</sub> is cascaded to move the impedance matching point further to the overlapped capacitive region in Fig. 3-12 ④ where the peak P<sub>out</sub> and PAE contours form a common impedance area. This allows the driver stage to achieve both optimum power matching and a maximum inter-stage PAE concurrently. TABLE 3-3 summarizes the passive component values in the driving stage. The inter-stage PAE load-pull simulations are conducted at the driver's output 1-dB gain compression point where the power gain of the driver is 10 dB and 8.5 dB at 24 GHz and 38 GHz, respectively.

After cascading the driver and output stages, the overall gain at OP<sub>-1dB</sub> point is 19 dB,  $\eta_c=53\%$ , and PAE=51% at 24 GHz in simulations. At 38 GHz, the simulated 1-dB compressed gain =15 dB,  $\eta_c=41.5\%$ , and PAE=39%. The input impedance matching bandwidth for S<sub>11</sub><-10 dB is 20-30 GHz for 24 GHz PA, and 30-50 GHz for 38 GHz PA. Fig. 3-13 presents the P<sub>out</sub> and PAE simulation results of the 24 GHz 2-stage PA over the temperature variations when the PA is biased with a constant current mirror. The saturated output power decreases from 18.5 dBm to 17 dBm by increasing the temperature from -20 °C to 120 °C (Fig. 3-13 (a)). This is mainly due to the degradation of the current gain  $\beta$  (or f<sub>T</sub>) of HBTs over the temperature increase, which results in degradation in peak PAE from 52% at -20 °C to 47% at 120 °C in Fig. 3-13 (b). In summary, when the temperature changes in the range of -20~120 °C, there is  $\pm 0.5$  dB variation in output power and  $\pm 3\%$  variation in peak PAE compared with the nominal values at the room temperature (27 °C).

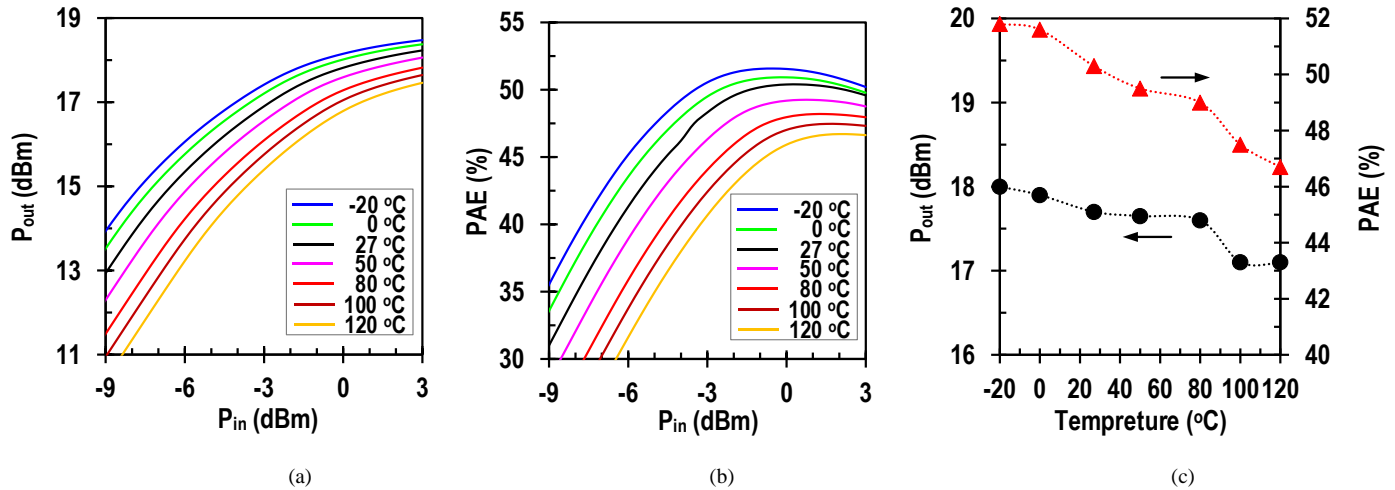


Fig. 3-13. Simulation results for temperature variation effects on the large signal performance of the 24 GHz PA: (a) output power, (b) PAE, and (c) output power and PAE versus temperature for input power levels of -9, -6, -3, 0, and 3 dBm.

### 3.4.3 Experimental Results

The PAs are fabricated in IBM8HP 0.13  $\mu\text{m}$  SiGe BiCMOS process ( $f_T/f_{max}$ =180/220 GHz) and Fig. 3-14 shows the die photographs of the PAs. The PA size is  $0.6 \times 0.95 \text{ mm}^2$  for 24 GHz PA (Fig. 3-14(a)) and  $0.55 \times 0.93 \text{ mm}^2$  for 38 GHz PA (Fig. 3-14(b)), including all pads. On-wafer small-signal S-parameter measurements are performed after SOLT calibrations. For large signal measurements, the PAs input power is sampled using a directional coupler and the sampled input and PA output powers are evaluated using R&S power sensors and power meters. RF cable loss is characterized and de-embedded carefully over the operational frequency range. The PAs are stable over all measured frequencies.

Modulated signals are also applied to the PAs to characterize in-band and out-of-band linearity performances. The R&S signal source SMW200A provides the PAs with 23-bit pseudo random binary sequence with an arbitrary digital modulation at a carrier frequency variable of up to 40 GHz. In the measurements the maximum modulated signal bandwidth is limited by the equipment. After a raised cosine filtering with 0.2 roll-off factor the maximum available bandwidth is 8.4 MHz. The PAs input signal is modulated using various modulation schemes having different peak-to-average power ratio (PAPR) including QAM, 8-PSK, 16-QAM, 64-QAM, and 128-QAM, which result in the bit-rate of 14, 21, 28, 42, and 49 Mbps, respectively. The PA output is fed to the R&S spectrum analyzer, FSW67, to evaluate EVM and ACPR, and corresponding average

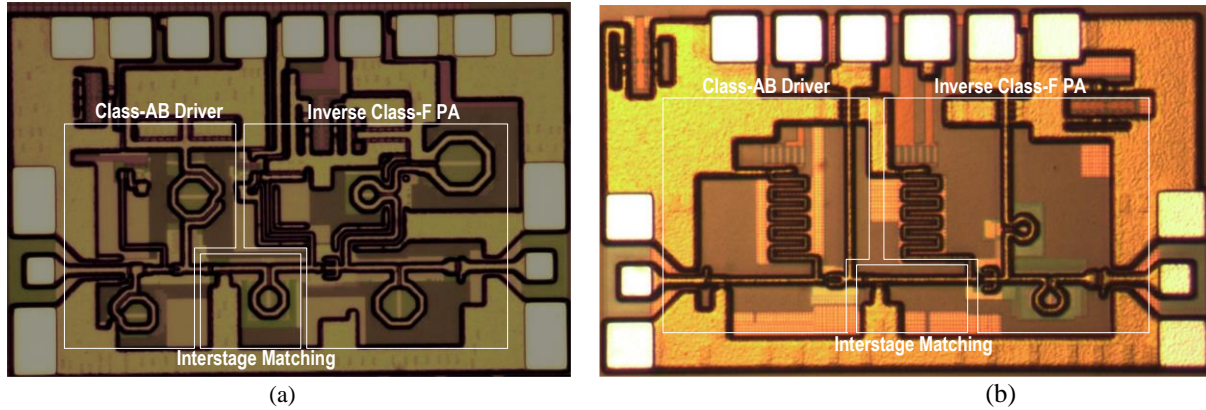


Fig. 3-14. Chip photographs: (a) 24 GHz PA (size:  $0.55 \times 0.93 \text{ mm}^2$ ) and (b) 38 GHz PA (size:  $0.55 \times 0.93 \text{ mm}^2$  including pads).

output power ( $P_{\text{out,ave}}$ ) and average power efficiency of the modulate signals. The EVM of the signal source itself is less than 0.9% (-41 dB) for all different modulation schemes at 20-40 GHz. In the PAs testing, ACPR is measured at 8 MHz offset from the carrier center frequency.

### 3.4.3.1 24 GHz Inverse Class-F PA Measurement Results

Fig. 3-15 shows the small signal and large signal measurement results with biasing  $V_{CC1}/V_{CC2}=2.3/2 \text{ V}$  and  $I_{CE1}/I_{CE2}=11.5/2 \text{ mA}$ .  $S_{11} < -10 \text{ dB}$  @ 22.5-36.5 GHz,  $S_{22} < -10 \text{ dB}$  @ 15-28 GHz, and  $S_{21}=19\text{-}22 \text{ dB}$  @ 21.5-27.2 GHz (Fig. 3-15 (a)). Fig. 3-15 (b) shows the large signal power measurement results at 24 GHz. The PA achieves peak 50% PAE at 17 dBm  $P_{\text{out}}$ . The measured  $P_{\text{sat}}$  is 18 dBm and  $OP_{-1\text{dB}}$  is 16 dBm. The compressed power gain at the peak PAE is around 19 dB, well matched with the simulation result. The measured PAE at the 6-dB back-off from the  $OP_{-1\text{dB}}$  is 22.5%, exhibiting a high PAE at the linear mode as well. To characterize the frequency response of the power efficiency, the PAE is measured over 22-27 GHz. The measurement results of peak PAE and corresponding output power versus frequency is disclosed in Fig. 3-15 (c). The PAE is higher than 45% over the range of 23.5-25.5 GHz with  $\sim 17.5 \text{ dBm}$  of corresponding output power. The trend of measured frequency response of the PAE is well aligned with simulation curve with only 1-2.5% error around the peak PAE point. The PAE is also measured by sweeping the supply voltage of the output stage from 1.2-2.4 V at 24 GHz to characterize the supply dependency of the PAE, and the results are shown in Fig. 3-15 (d). The PA can maintain higher than 45% of peak PAE over 0.9 V supply variations from 1.5-2.4 V, while the output power corresponding to the peak efficiency increases from 14 dBm to 17.5 dBm as the supply voltage increases.

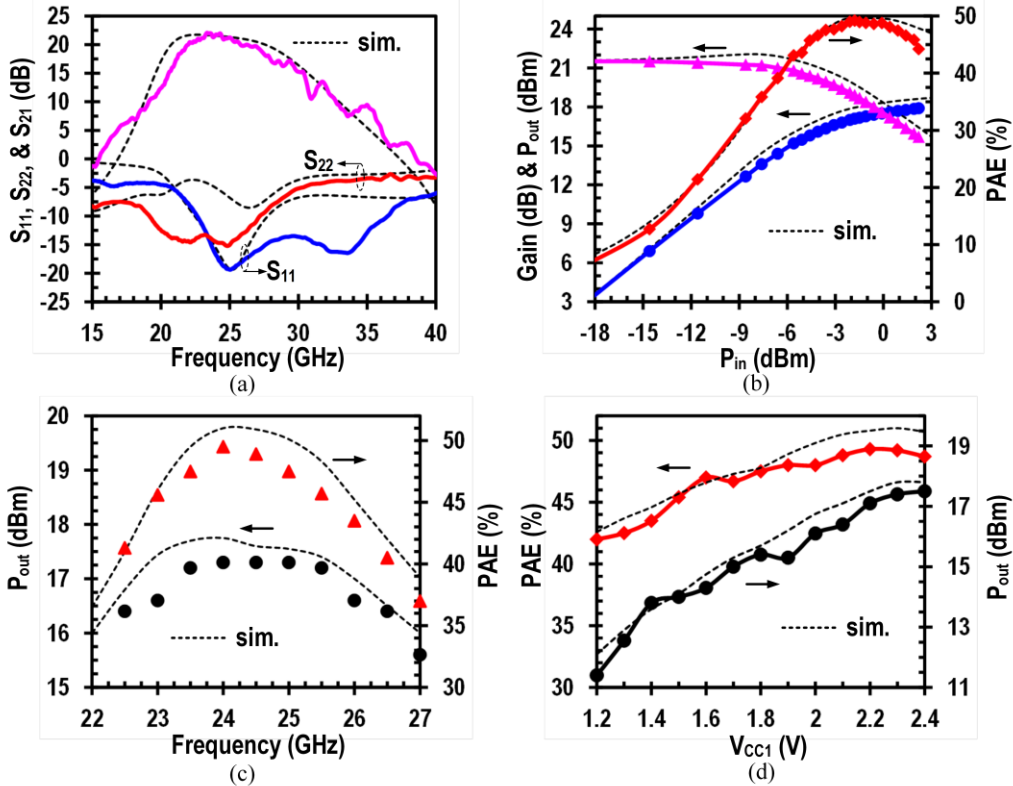


Fig. 3-15. 24 GHz PA measured performances: (a) gain, input and output matching, (b) power gain, output power, and PAE versus input power, (c) peak PAE and corresponding output power versus frequency, and (d) peak PAE and corresponding output power versus supply voltage of the output stage.

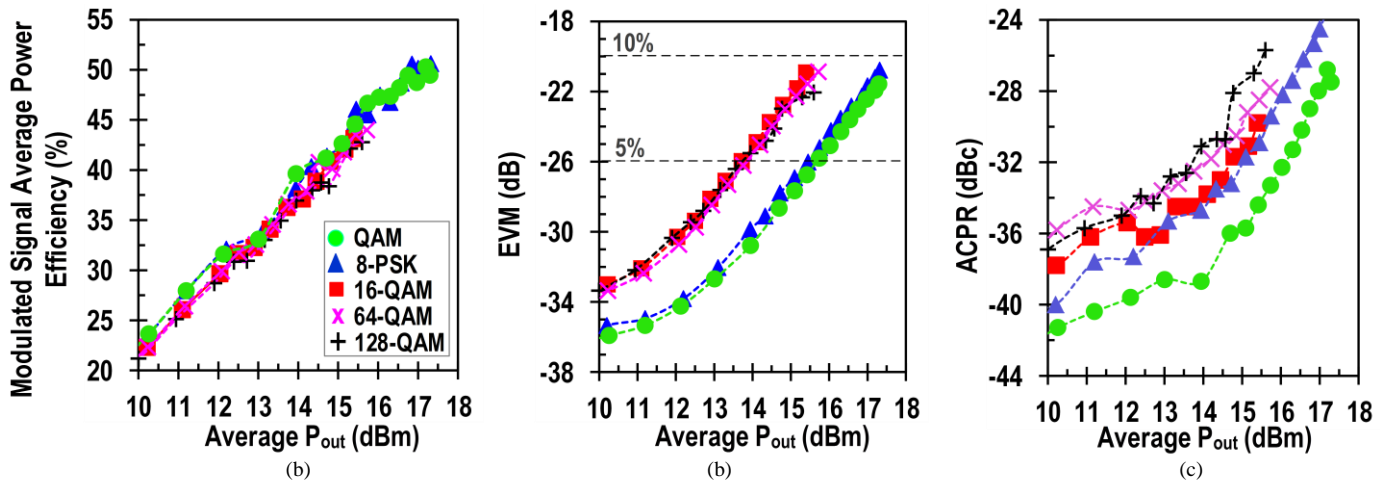


Fig. 3-16. 24 GHz PA measured modulation power efficiency, EVM, and ACPR versus average output power at 24 GHz for different modulation platforms: (a) power efficiency, (b) EVM, and (c) ACPR at 8 MHz offset bands. ACPR is presented in absolute magnitude scale.

The modulation test results for different modulation schemes are summarized in Fig. 3-16. The center frequency of the modulation signal is 24 GHz. Obviously, the average power efficiency is proportional to the  $P_{out,ave}$  and exceeds 50% when the  $P_{out,ave}$  increases over 17 dBm in Fig. 3-16 (a). This shows a good correlation with the monotone test in Fig. 3-15 (b). The measured EVM is

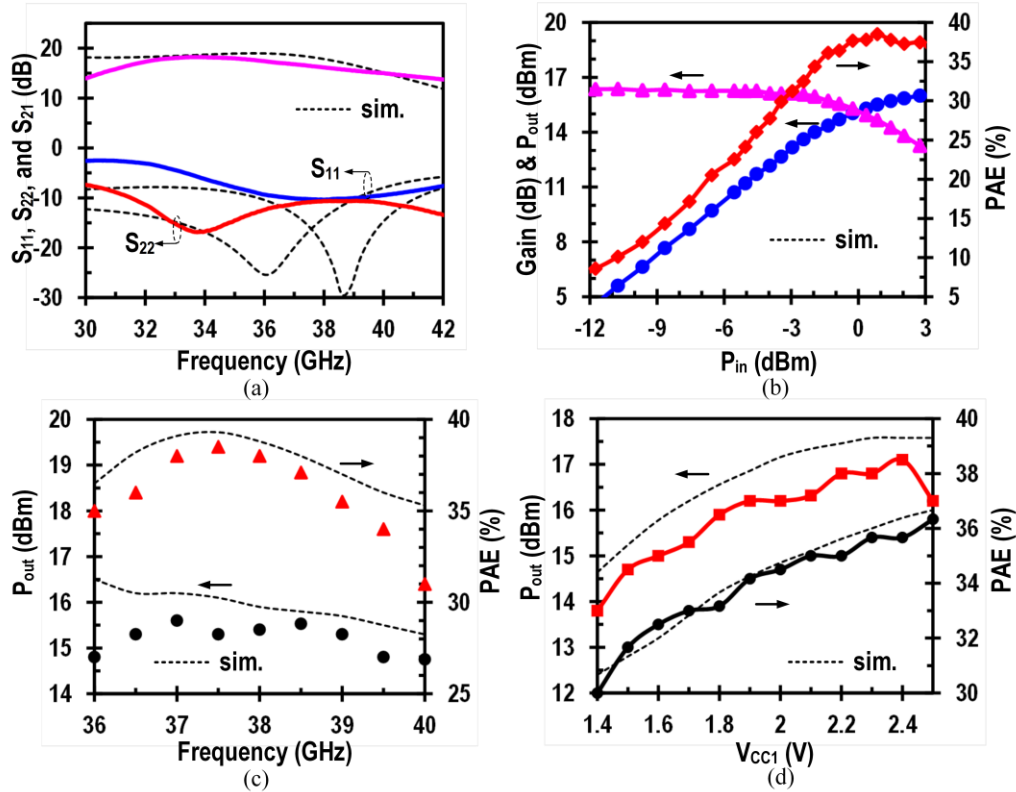


Fig. 3-17. 38 GHz PA measured performances: (a) gain, input and output matching, (b) power gain, output power, and PAE versus input power, (c) peak PAE and corresponding output power versus frequency, and (d) peak PAE and corresponding output power versus supply voltage of the output stage.

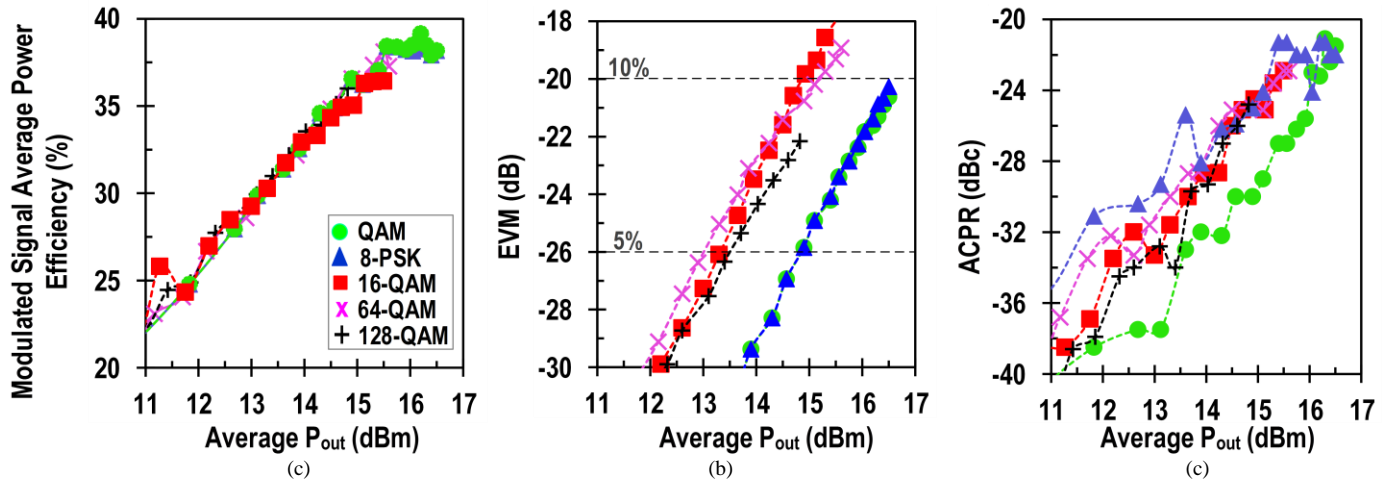


Fig. 3-18. 38 GHz PA measured modulation power efficiency, EVM, and ACPR versus average output power at 38 GHz for different modulation platforms: (a) power efficiency, (b) EVM, and (c) ACPR at 8 MHz offset bands. ACPR is presented in absolute magnitude scale.

plotted in dB scale for better contrast. The QAM and 8-PSK are the least PAPR modulation formats and exhibit the best power efficiency for a given EVM: the  $P_{out,ave}$  corresponding to 5% EVM is around 16 dBm for both QAM and 8-PSK in Fig. 3-16 (b). At 5% EVM the PA achieves 47.3% of modulation power efficiency in Fig. 3-16 (a) with  $< -35$  dBc ACPR in Fig. 3-16 (c). For 16-

64-, and 128-QAM signals, the range of  $P_{out,ave}$  for <5% EVM (-26 dB) is 13-13.5 dBm, and the corresponding average power efficiency is around 30-32% with <-32 dBc of ACPR.

### 3.4.3.2 38 GHz Inverse Class-F PA Measurement Results

For the 38 GHz PA, Fig. 3-17 (a) and Fig. 3-17 (b) show measured small-signal and large-signal characteristics with a nominal class-AB biasing of  $V_{CC1}/V_{CC2}=2.4/1.5$  V,  $I_{CC1}/I_{CC2}=8/4$  mA:  $S_{11}<-10$  dB,  $S_{22}<-10$  dB, and  $S_{21}=15-17$  dB over 36-40 GHz (Fig. 3-17 (a)). At 38 GHz with the class-AB biasing, the PA achieves peak PAE of 38.5% with corresponding 15.5 dBm  $P_{out}$ , 15 dBm  $OP_{-1dB}$ , and 17 dBm  $P_{sat}$  in Fig. 3-17 (b). The measured PAE at the 6-dB back-off from the  $OP_{-1dB}$  is 19%. The saturated power gain at the  $OP_{-1dB}$  is 15 dB as expected in the design section. The PAE is > 35% over 36-39 GHz in Fig. 3-17 (c) and over 1.5-2.5 V supply voltage variation in Fig. 3-17 (d), manifesting the PAE robustness to the frequency and supply variations. The PAE discrepancy between the measurement and the simulation is < 2% at 37-39 GHz.

As seen in the modulation test results summarized in Fig. 3-18, the average modulation signal power efficiency reaches around 38-39% when  $P_{out,ave}$  exceeds 15.5 dBm. The average PAE in Fig. 3-18 (a) is well matched with the PAE result in Fig. 3-17 (b). The  $P_{out,ave}$  for < 5% EVM is around 15 dBm and 13.5 dBm for QPSK/8-PSK and 16/64/128-QAM signals, respectively, in Fig. 3-18 (b). When the  $P_{out,ave}$  is capped for <5% EVM, the average power efficiency is ~36% for QPSK/8-PSK with -26~-27 dBc ACPR in Fig. 3-18 (c). The efficiency decreases to 30-32% with <-32 dB ACPR when the high spectral-efficiency modulation schemes of 16/64/128-QAM signals are applied to the PA.

Fig. 3-19 compares the PAE of recent microwave and mm-Wave silicon PAs more graphically and reveals a trend line of diminishing PAE as operational frequency increases. This demonstrates a common tradeoff between power-added efficiency and speed in silicon PAs. While recent PAs based on class-F or class-F<sup>-1</sup> technique demonstrate outstanding PAE performance over other high efficiency techniques, the proposed class-F<sup>-1</sup> PA adopting a high-order multi-resonance harmonic filter load achieves one of best power efficiency at each frequency band. The measured PAEs are even higher than or comparable to those of recent III-V PAs in Table 3-4.



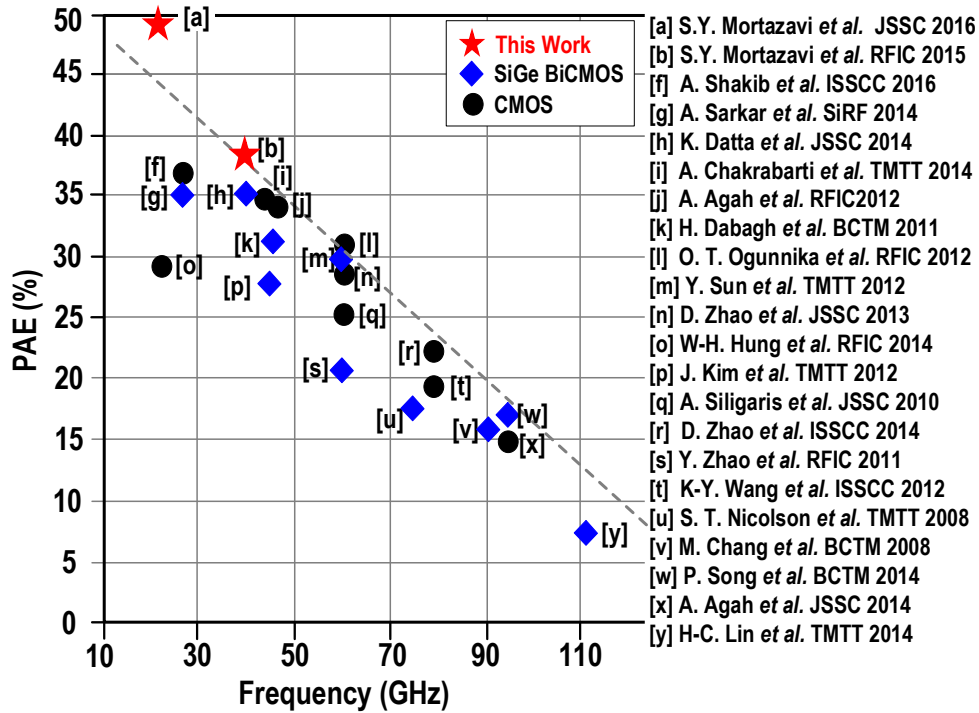


Fig. 3-19. PAE performance of the mm-wave silicon PAs

### 3.5 Summary

This chapter fully discusses the potentials and limitations of the class-F<sup>-1</sup> technique in achieving a high PAE at microwave and higher frequencies, especially for integrated PAs based on silicon process; the impact of a finite number of harmonics control, knee voltage, limited breakdown voltage, and finite losses from passive components on the PAE has been analyzed. In order to shape better class-F<sup>-1</sup> voltage and current waveforms, the PAs adopt multi-resonance parallel and series loads that modulate the load impedance cooperatively to pull the PAs with an optimal impedance which is variable depending on fundamental, even, and odd harmonic bands. Two integrated silicon inverse class-F PAs are successfully implemented and demonstrated at microwave and mm-Wave frequencies. PAs achieved overall 50% peak PAE at 24 GHz and 38.5% PAE at 38 GHz, some of the highest PAEs in the integrated PAs reported so far for both silicon and III-V technologies. Certainly, the PAs can process an ultrahigh speed modulation signal with a high efficiency since the signal bandwidth for power gain, impedance matching, and PAE is greater than several GHz, thus suitable for the application of the next generation high-speed wireless communications.



# 4 Harmonic load modulators for mm-wave Class-F<sup>-1</sup> PA

## 4.1 Introduction

Millimeter (mm)-Wave communication at 28 GHz is gaining growing attention for fifth-generation (5G) cellular networks to accommodate explosive demands on higher data-rate in wireless communications. While no firm 5G mobile standard is emerged yet, directional antennas and beam-forming arrays prove to be essential for a maximum channel capacity at the mm-Wave band for both base stations and mobile devices [3]. In the beam-forming phased array for the 5G mobile terminals, the required transmit output power per array element would be moderate, typically 50-60 mW (17-18 dBm) of a compressed output power ( $P_{\text{out}}$ ) per unit power amplifier (PA) [2]-[4]. The high power-added-efficiency (PAE) in the unit PA is critical to curb the system power down to a required low power level, likely less than 1 Watt, and thus for the phased array system platform to be more realistic in the mobile units.

In generic solid-state amplifiers, the power efficiency is directly traded with the circuit linearity which is another crucial PA's performance figure to support a high spectral efficiency required by the future 5G wireless standardization. For better linearity, a classical approach is to operate the PA with significant backoff from its saturation point. With being biased practically at a higher than nominal class-B point to achieve a higher gain and thus better PAE at mm-Wave, the harmonically tuned amplifiers, e.g. class-F or inverse class-F (F<sup>-1</sup>) PAs, can degenerate to a class-AB mode at a power backoff mode and possibly can support the linearity requirement [31]. In fact, in the silicon based class-F<sup>-1</sup> PAs, the output power transistor starts to produce visible nonlinear harmonic currents at near the 1-dB gain compression power level and generates distinguishable half-sinusoid voltage and quasi-rectangular current waveforms at their collector nodes. When the PAs operate at a linear (or power backoff) mode well below the gain compression point, their operation is in a class-AB mode. Compared with the class-F PAs, in the class-F<sup>-1</sup> PAs the odd harmonic impedances are terminated to short at a generator output node, which makes the class-F<sup>-1</sup> PAs less vulnerable to the odd-harmonics induced intermodulation distortion.

This paper is an extension of the short communication of [5] where the inverse class-F operation of a harmonically tuned load based on the coupled inductors is described qualitatively. A comprehensive quantitative analysis and analytical design equations are provided in this paper. For mm-Wave class-F<sup>-1</sup> PAs, the impedance control at higher than the 3<sup>rd</sup>-harmonic of a signal frequency would be cumbersome. In practical designs, sustaining a high impedance at a 2<sup>nd</sup>-harmonic band is crucial to shape minimally overlapped collector voltage and current waveforms at saturation. Compared to the prior class-F<sup>-1</sup> implementations, a coupled harmonic impedance control by the magnetically coupled coils can maintain a high impedance over a wider 2<sup>nd</sup>-harmonic band. Furthermore, by leveraging mutual resistance, the quality factor of the inductors can be enhanced. This will decrease the power loss in the passive networks and thus increase the PA's PAE.

Since specific 5G bandwidth standard is not yet available in the vicinity of 28 GHz, in this class-F<sup>-1</sup> PA implementation, the design frequency band is set rather judgmentally to around 28~29 GHz. The coupled coils promote a dual-resonance at the 2<sup>nd</sup>-harmonic band for better class-F<sup>-1</sup> waveform shaping. The peak PAE in the output stage when the PA is compressed and operates in the class-F<sup>-1</sup> mode ( $P_{\text{out}}=15\text{-}17$  dBm) is 45%, one of the best PAEs reported so far at the Ka-band. The overall PAE, however, is degraded to 42% when the PA is preceded by a class-AB driver. When the output power is backed off by 6 dB from the 1-dB gain compression point, whereby the overall 2-stage PA operates in a class-AB mode, the measured PAE is 20%, still far better than other recent state-of-the-art silicon PAs when compared with similar power backoff [32]-[37]. The error vector magnitude (EVM) tests exhibit that the PA's EVM is less than 2% with QAM and 8-PSK signals and less than 5% with 16-QAM, 64-QAM, and 128-QAM signals at the 6 dB power backoff mode, confirming that the PA operates in a linear class-AB mode.

## 4.2 Mutual Impedance Modulation

In the magnetically coupled inductors shown in Fig. 4-1, the net voltages in the primary and secondary inductors are a linear superposition of self- and mutually-induced voltages given as

$$\begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} j\omega L_1 + R_{s1} & j\omega M \\ j\omega M & j\omega L_2 + R_{s2} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}. \quad (4 - 1)$$

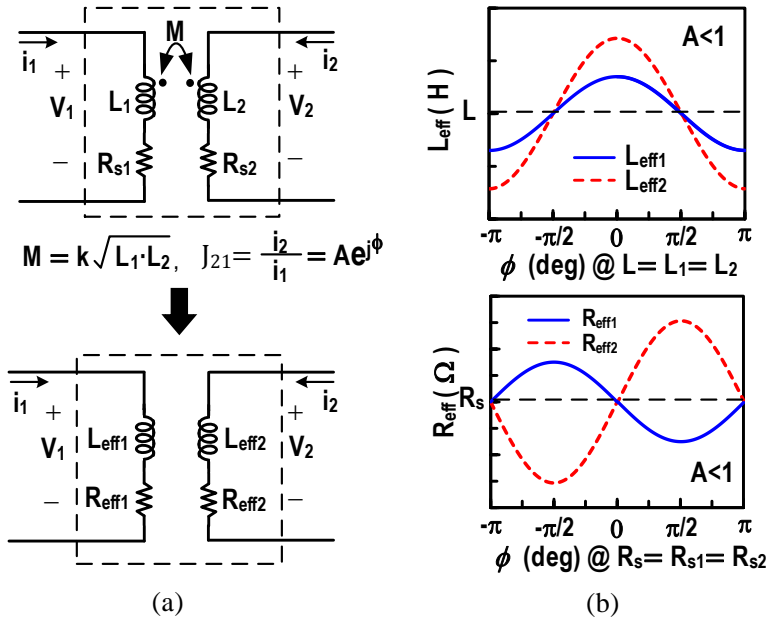


Fig. 4-1. Alternation of effective inductance and resistance in coupled inductors with primary/secondary current ratio.

$L_1$  and  $L_2$  are self-inductances of the primary and secondary inductors, respectively.  $M$  is a mutual inductance between the coils, expressed as  $M = k\sqrt{L_1 L_2}$  where  $k$  ( $0 \leq k \leq 1$ ) is a coupling coefficient.  $v_{1,2}$  and  $i_{1,2}$  are peak values.  $R_{s1}$  and  $R_{s2}$  model a finite quality factor ( $Q$ ) of the coupled inductors. By defining the ratio of the secondary current to the primary current as

$$J_{21} \triangleq i_2/i_1 = Ae^{j\phi} = A(\cos\phi + j\sin\phi). \quad (4-2)$$

where  $A$  is the magnitude of the current ratio and  $\phi$  is its phase,  $v_1$  and  $v_2$  can be found as

$$v_1 = \{j\omega(L_1 + MA \cdot \cos\phi) + R_{s1} - \omega MA \cdot \sin\phi\}i_1. \quad (4-3a)$$

and

$$v_2 = \{j\omega(L_2 + M/A \cdot \cos\phi) + R_{s2} + \omega M/A \cdot \sin\phi\}i_2. \quad (4-3b)$$

Therefore, the effective inductances and resistances of the primary and secondary inductors are

$$L_{eff1} = \text{Im}(v_1/i_1)/\omega = L_1 + MA \cdot \cos\phi, \quad (4-4a)$$

$$L_{eff2} = \text{Im}(v_2/i_2)/\omega = L_2 + \frac{M}{A} \cdot \cos\phi, \quad (4-4b)$$

$$R_{eff1} = \text{Re}(v_1/i_1) = R_{s1} - \omega MA \cdot \sin\phi, \quad (4-4c)$$

and

$$R_{eff2} = Re(v_2/i_2) = R_{s2} + \frac{\omega M}{A} \cdot \sin\phi, \quad (4 - 4a)$$

$J_{21}$  is a frequency-dependent parameter and the effective mutual inductance ( $L_{eff1,2}$ ) and mutual resistance ( $R_{eff1,2}$ ) are functions of the magnitude and phase  $J_{21}$ .

Fig. 4-1 (b) shows the effective inductance and resistance of the primary and secondary inductors when  $A < 1$  and  $\phi$  varies over  $-\pi$  to  $\pi$ . If the primary and secondary currents are in phase (e.g.  $\phi = 0$ ), their magnetic fluxes are constructive, effectively increasing  $L_{eff1}$  and  $L_{eff2}$  with no mutual resistance. This enhances the quality factor of the inductors. However, the induction of out-of-phase currents (e.g.  $\phi = \pm\pi$ ) between the coupled coils diminishes magnetic flux linkage, reducing the inductances of the coils whereby Q is lowered. For a perfect orthogonal current excitation (e.g.  $\phi = \pm\pi/2$ ), the magnetic coupling will not happen and there is only active power and corresponding energy exchange between the primary and secondary inductors; that is, from (4-2), (4-4c), and (4-4d),  $i_1^2 \omega M A \cdot \sin\phi/2 = i_2^2 \omega M/A \cdot \sin\phi/2$ , manifesting that when  $0 < \phi < \pi$ , any power loss caused by the positive mutual resistance of  $\omega M/A \cdot \sin\phi$  in (4-4d) will be replenished by the negative mutual resistance of  $-\omega M A \cdot \sin\phi$  in (4-4c), and vice versa when  $\pi < \phi < 2\pi$ . The real active power is only dissipated by the intrinsic physical resistances,  $R_{s1}$  and  $R_{s2}$ . The total power loss in the coupled coils is  $1/2 \cdot (i_1^2 R_{s1} + i_2^2 R_{s2})$  which is constant over the  $\phi$  variation.

In a general case of exciting arbitrarily phased currents in the coupled coils, the *in-phase* current component alters the mutual flux and modulates the mutual inductance, whereas the *quadrature* component modifies the effective coil resistances by inflecting the mutual resistance. Therefore, the impedance of a coupled inductor can be varied dramatically by controlling  $A$  and  $\phi$ ; From (4a) and (4b), when  $\phi = \pm\pi$ ,  $L_{eff}$  even becomes negative or capacitive at the primary if  $A > L_1/M$ , or at the secondary if  $A < M/L_2$ . Utilizing the coupled-inductor based LC resonator, the magnitude and phase of  $J_{21}$  can be controlled capably over the signal's harmonic bands to create optimal harmonic-dependent impedances for an inverse class-F operation.

### 4.3 High Quality-Factor Coupled Inductors Design

When designing magnetically coupled lines in the planar IC technology, the tradeoff between the coupling coefficient and loss comes into play. Namely, for a tight coupling ( $k > 0.5$ ) a broadside coupling is often preferred to an edge coupling. This, however, suffers from more loss due to a higher ohmic resistance from a lower metal layer. A low loss passive design is of prime concern for a high power efficiency. Therefore, to attain a high quality factor at both primary and secondary sides, the inductors are coupled utilizing the edge coupling in this work; two inductors are implemented side by side using the top metal layer with a low sheet resistance thanks to the excessive thickness compared to other lower metal layers. The widths of the inductors are also optimized in electromagnetic (EM) field simulations using the Sonnet Software [29] to reduce the ohmic loss while yielding required inductances.

In the planar coupled lines, the induced current tends to crowd at the edge toward the neighboring line at high frequencies. This effectively increases the metal sheet resistance and degrades Q. To distribute current more evenly on the metal plate, a sandwich structure is used as illustrated in Fig. 4-2 (a) where the secondary inductor is enclosed by the primary inductor [38]. This structure not only improves the quality factor but also achieves a close coupling of  $k \sim 0.5$  despite relatively far spacing ( $5 \mu\text{m}$ ) between the top metal layers required by a design rule. EM simulations are conducted on the various lengths (or inner diameters) of the coupled lines for realizing the inductances ranging 60-to-120 pH which are widely chosen at mm-Wave. It is found

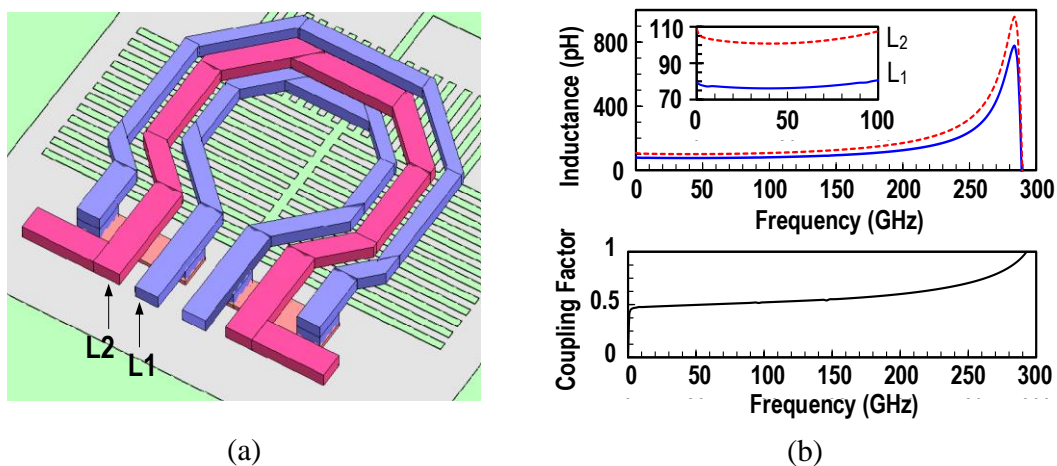


Fig. 4-2. Layout and EM simulation results for coupled inductance

that the inductance of the enclosed inductor (secondary) is 1.2~1.5 times larger than that of the outer inductor (primary) because of the layout asymmetry.

In practice for the initial numerical design of a PA load network, it can therefore be assumed reasonably that  $L_2 \approx 1.3L_1$  and the mutual coupling can be approximated to  $M = k\sqrt{L_1L_2} \approx 0.6L_1$ . The initial load design is then followed by a fine characterization and calibration of the passive components through EM modeling including layout parasitic inductances and capacitances. Fig. 4-2 (b) shows the frequency responses of the self-inductances and the coupling factor of the optimized coupled inductors for the class-F<sup>-1</sup> PA in this work. The self-resonance occurs near 280 GHz.  $L_1$  and  $L_2$  are typically 75 pH and 100 pH, respectively, which are fairly constant over the frequencies; less than 1% variation at the frequency band of interest from 28 GHz (fundamental) to around 84 GHz (3<sup>rd</sup> harmonic). The coupling factor is 0.5 with less than 1% variation up to the 3<sup>rd</sup> harmonic band. TABLE I summarizes ohmic resistances of  $L_1$  and  $L_2$  at the fundamental ( $\omega_0$ ), the 2<sup>nd</sup> harmonic ( $2\omega_0$ ), and the 3<sup>rd</sup> harmonic ( $3\omega_0$ ) frequencies, respectively.

#### 4.4 Coupled Inductors based Class-F<sup>-1</sup> Load

Fig. 4-3 shows the proposed inverse class-F load network employing the coupled coils. The load network is comprised of a parallel of  $Z_S$ , the impedance of series signal path to the 50- $\Omega$  output load, and  $Z_P$ , the impedance of parallel path which includes a total parasitic capacitance ( $C_3$ ) at the collector node of the PA. By coupling the two inductors  $L_1$  and  $L_2$ ,  $Z_S$  and  $Z_P$  become dependent on each other. This allows a coupled impedance control by  $L_1$  and  $L_2$  to provide desirable frequency-dependent inductances to the primary and secondary paths for generating an

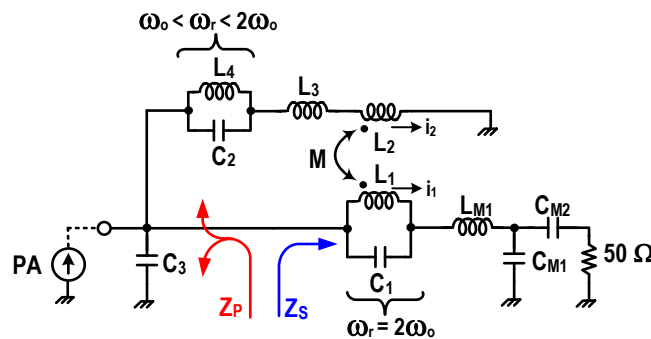


Fig. 4-3. The proposed load network with coupled coils for Class-F<sup>-1</sup> PA



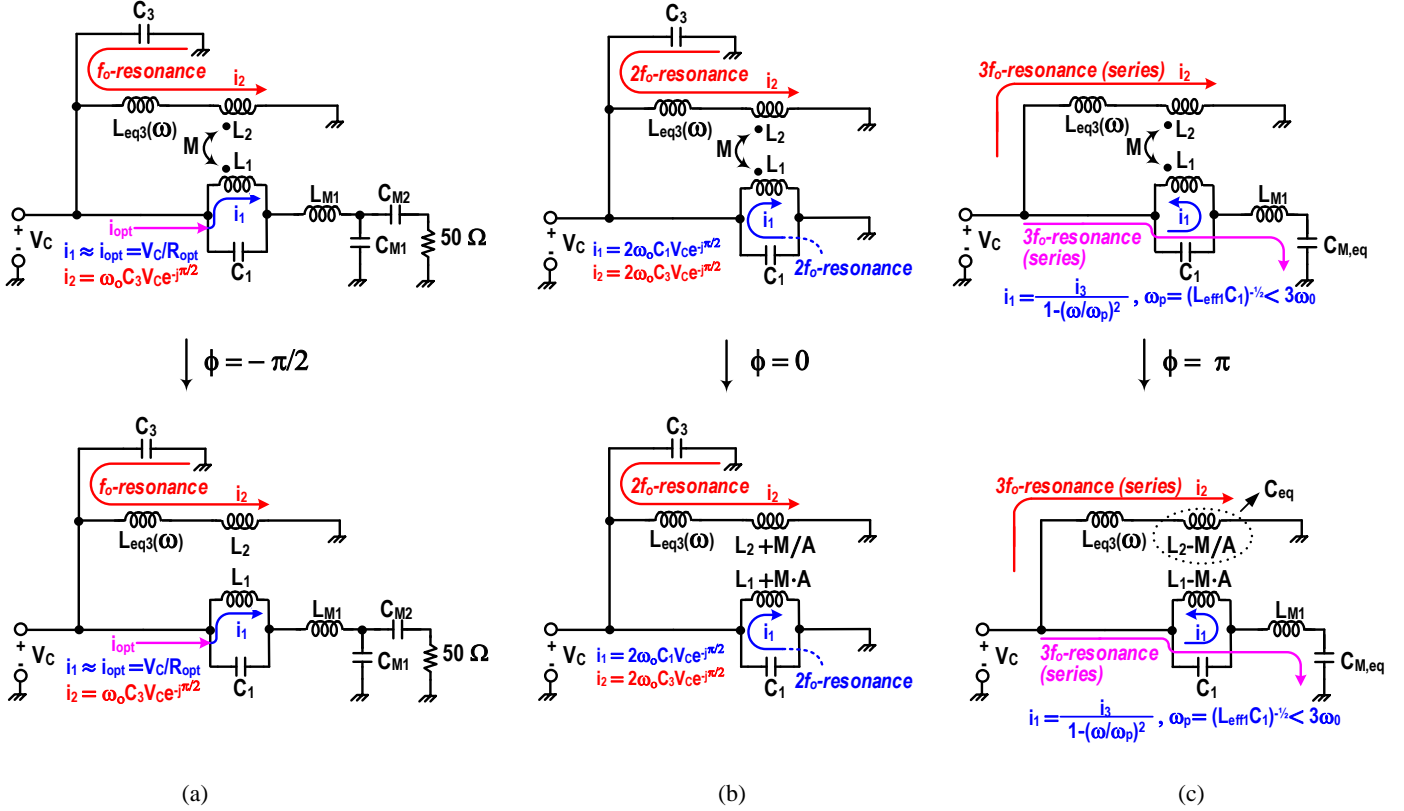


Fig. 4-4. Operation and equivalent circuit of the load network at different frequency bands (a) fundamental frequency band with no coupling, (b) 2<sup>nd</sup>-harmonic band with in-phase coupling, (c) 3<sup>rd</sup>-harmonic band with out-of-phase coupling.

optimum resistance at the  $\omega_0$ -band (28 GHz), a high impedance at the  $2\omega_0$ -band (56 GHz), and a low impedance at the  $3\omega_0$ -band (84 GHz).

### I. Impedance Modulation @ $\omega_0$ -band

Fig. 4-4 (a) shows the equivalent load network at the  $\omega_0$ -band. The series of  $L_4$ - $C_2$  resonator ( $\omega_0 < \omega_r < 2\omega_0$ ) and  $L_3$  in Fig. 4-3 can be modeled equivalently with a frequency-dependent nonlinear inductance  $L_{eq3}(\omega)$  expressed as

$$L_{eq3}(\omega) = L_3 + \frac{L_4}{1 - \left(\frac{\omega}{\omega_r}\right)^2}, \quad \text{where } \omega_r = \frac{1}{\sqrt{L_4 C_2}}. \quad (4-5)$$

The series network comprised of  $L_1$ ,  $C_1$ ,  $L_{M1}$ , and  $C_{M1,2}$  matches the 50- $\Omega$  load to an optimum load ( $R_{opt}$ ). Thus, the optimum current,  $i_{opt}$  ( $=v_c/R_{opt}$ ) flowing to the series network is in-phase with the collector voltage  $v_c$ . The current in the primary inductor  $L_1$  is

$$i_1 = \frac{i_{opt}}{1 - \omega_o^2 L_{eff1} C_1} = \frac{v_c}{R_{opt}} \cdot \frac{1}{1 - \omega_o^2 L_{eff1} C_1}. \quad (4 - 6)$$

In (6), the  $L_{eff1}$ - $C_1$  tank is set to resonate at the  $2\omega_o$ -band, resulting in  $\omega_o^2 L_{eff1} C_1 < 1/4$  at the  $\omega_o$ -band. The primary inductor current  $i_1$  is in phase with  $v_c$ . In the parallel path, the series inductance of  $L_{eq3} + L_{eff2}$  resonates out  $C_3$  and provides a high impedance at the  $\omega_o$ -band so that most of the fundamental current is delivered to  $R_{opt}$ . The secondary inductor current is

$$i_2 = \frac{v_c}{j\omega_o \{L_{eq3}(\omega_o) + L_{eff2}\}} = -j\omega_o C_3 v_c. \quad (4 - 7)$$

Subsequently,  $J_{21}$  becomes

$$J_{21} = \underbrace{\left( \frac{\omega_o C_3}{R_{opt}} \cdot \frac{1}{1 - \omega_o^2 L_{eff1} C_1} \right)}_A e^{-j\frac{\pi}{2}}. \quad (4 - 8)$$

The coupled inductor currents are orthogonal ( $\phi = -\pi/2$ ). This nullifies the magnetic coupling effect at the signal band and the effective inductances at the primary and secondary paths do not change: i.e.,  $L_{eff1} = L_1$  and  $L_{eff2} = L_2$  in (6)-(8). It is worthwhile to mention that from (4-4c), because  $\phi = -\pi/2$  the mutual resistance is additive and increases the net resistance of the primary inductor ( $R_{eff1}$ ) by  $\omega_o M A$ . While this seemingly incurs an additional power dissipation via the added resistance, it does not cause any actual power loss. This is because the negative mutual resistance in the secondary path behaves as a current source and will feed the equal power back to the primary signal path, compensating the power loss, as discussed in the previous section. CAD simulations confirm that there is no power loss from the collector node to the 50- $\Omega$  load by the mutual resistances and no stability issues arise.

## II. Impedance Modulation @ $2\omega_o$ -band

The equivalent load network at the  $2\omega_o$ -band is shown in Fig. 4-4 (b). In the series path,  $L_{eff1}$  resonates  $C_1$ . This provides a high impedance and almost all 2<sup>nd</sup> harmonic voltage drops on the resonator. Therefore, the series load is simplified by the  $L_1$ - $C_1$  tank. By applying KVL around the coupled inductors, the voltage drop over the secondary inductor can be found as

$$v_2 \approx v_1 - j\omega L_{eq3}(\omega) i_2. \quad (4 - 9)$$

From (4-1) and (4-9),  $J_{21}$  becomes

$$J_{21} = \frac{L_1 - M}{L_2 - M + L_{eq3}(\omega)}. \quad (4-10)$$

By carefully setting  $L_3$  and  $L_4$  in (4-5), it is possible to make  $L_{eq3}(\omega)$  inductive at the  $2\omega_0$ -band. This results in the in-phase current induction in the coupled coils ( $\phi=0$ ). Since from (4-4a) and (4-4b)  $L_{eff1} > L_1$  and  $L_{eff2} > L_2$ , the quality factor of the coupled inductors will be enhanced. At the exact  $2\omega_0$  frequency, where  $L_{eff2}$  resonates out  $C_3$ , the current ratio in (4-10) is simplified to

$$J_{21} = C_3/C_1 @\omega = 2\omega_0. \quad (4-11)$$

This leads the effective primary and secondary inductances at the  $2\omega_0$  frequency to be

$$L_{eff1} = L_1 + M \left( \frac{L_1 - M}{L_2 - M + L_{eq3}(\omega)} \right) = L_1 + M \cdot C_3/C_1 @\omega = 2\omega_0, \quad (4-12a)$$

and

$$L_{eff2} = L_2 + M \left( \frac{L_1 - M}{L_2 - M + L_{eq3}(\omega)} \right)^{-1} = L_2 + M \cdot C_1/C_3 @\omega = 2\omega_0. \quad (4-12b)$$

It is desirable that the 2<sup>nd</sup> harmonic-trap  $L_1$ - $C_1$  tank keeps high impedance over the entire 2<sup>nd</sup> harmonic band so that the sinusoidal voltage peaking at the collector node is better shaped over the required bandwidth. This can be achieved by the frequency dependent  $L_{eff1}$  in (4-12a). Namely, since  $L_{eq3}(\omega)$  increases over the frequency at the  $2\omega_0$ -band,  $L_{eff1}$  decreases as the frequency increases. This can sustain a resonance over the entire 2<sup>nd</sup> harmonic band, with a fixed  $C_1$ , allowing a high impedance over the required harmonic bandwidth.

### III. Impedance Modulation @ $3\omega_0$ -band

Fig. 4-4 (c) shows the equivalent load circuit at the  $3\omega_0$ -band. The network comprised of  $C_{M1}$ ,  $C_{M2}$ , and 50- $\Omega$  load can be equivalently lumped as a low Q capacitance,  $C_{M,eq}$ , due to the 50  $\Omega$  loading. Thus, the series path composed of  $L_{M1}$ ,  $C_{M1}$ ,  $C_{M2}$ , and 50- $\Omega$  load in Fig. 4-3 is approximated to the series of  $L_{M1}$  and  $C_{M,eq}$  in Fig. 4-4 (c), which is then modeled as an equivalent nonlinear inductance  $L_{eq4}(\omega)$  expressed as

$$L_{eq4}(\omega) \approx L_{M1} - \frac{1}{\omega^2 C_{M,eq}}. \quad (4-13)$$

Further, at the 3<sup>rd</sup>-harmonic band a capacitive impedance will be dominant in the L<sub>1</sub>-C<sub>1</sub> tank, which can resonate  $L_{eq4}(\omega)$ . By applying KVL around the coupled inductors in Fig. 4-4 (c), it can be found that

$$v_2 = v_1 + j\omega L_{eq4}(\omega)i_3 - j\omega L_{eq3}(\omega)i_2. \quad (4-14)$$

Meanwhile, by applying KCL at the L<sub>1</sub>-C<sub>1</sub> tank node, we get

$$i_3 = j\omega C_1 v_1 + i_1. \quad (4-15)$$

Plugging (4-15) into (4-14) results in

$$v_2 = v_1 \left( 1 - \frac{\omega^2}{\omega_x^2} \right) + j\omega L_{eq4}(\omega)i_1 - j\omega L_{eq3}(\omega)i_2, \quad \text{where } \omega_x = \frac{1}{\sqrt{L_{eq4}(\omega)C_1}}. \quad (4-16)$$

Subsequently, by applying (4-16) into (4-1)  $J_{21}$  can be found as

$$J_{21} = \underbrace{\left( \frac{L_1 \left( \frac{\omega^2}{\omega_x^2} - 1 \right) + M + L_{eq4}(\omega)}{L_2 + M \left( \frac{\omega^2}{\omega_x^2} - 1 \right) + L_{eq3}(\omega)} \right)}_A e^{j\pi}. \quad (4-17)$$

The primary inductor current  $i_1$  induces an out-of-phase current  $i_2$  in the secondary inductor, resulting in  $\phi=\pi$ . As seen in the next section, we carefully optimize the passive reactive elements such that  $0 < A < M/L_2$  at the 3<sup>rd</sup>-harmonic band. Therefore, from (4-4b) the effective secondary inductance,  $L_{eff2}$ , becomes negative (or capacitive) and can resonate  $L_{eq3}(\omega)$  at the  $3\omega_o$  frequency. Now, both the series path and the parallel path make series resonance. This will short the 3<sup>rd</sup>-harmonic collector current to the ground and thereby can shape a 3<sup>rd</sup>-harmonic-rich quasi-rectangular current waveform at the collector node. The passive components values of the load network optimized for 28 GHz operation are disclosed in the following section.

## 4.5 Inverse Class-F Power Amplifier Design

Fig. 4-5 shows the schematic of the proposed 28-GHz 2-satge PA, which is the cascade of a class-AB driver and a class-F<sup>-1</sup> power stage adopting the proposed load network. As for an overall

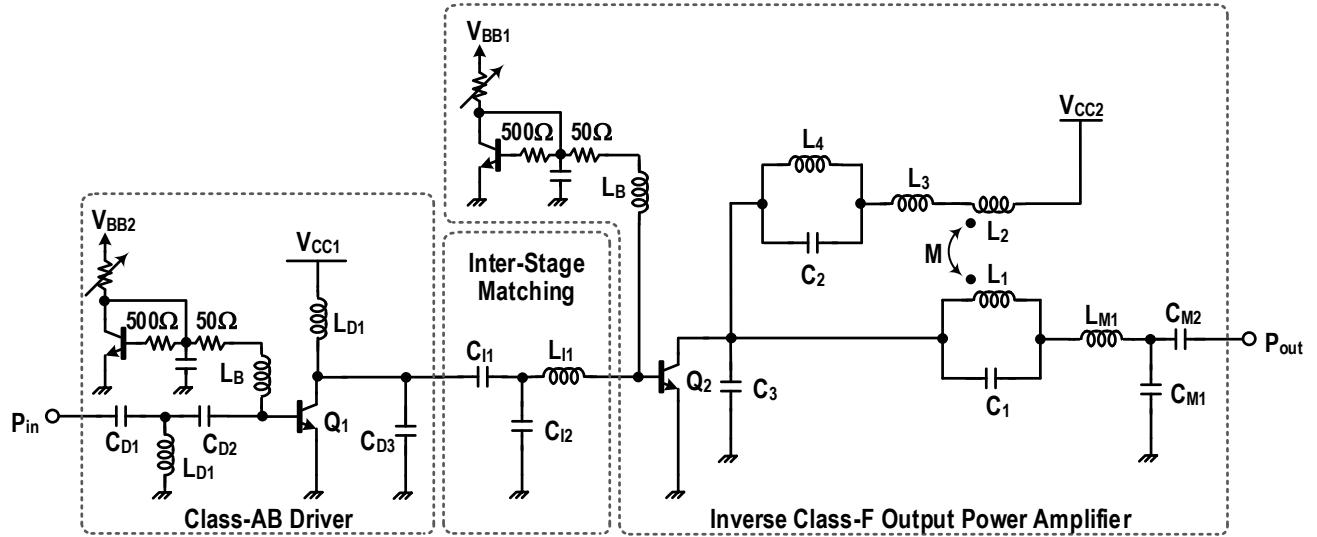


Fig. 4-5. Schematic of the 2-stage power amplifier, cascade of Class-AB driver followed by Inverse Class-F output stage. Inter-stage matching is applied to achieve an optimum power delivery to the PA with a maximum PAE in the driver

system overview, the maximum saturated output power ( $P_{\text{sat}}$ ) at the output stage is set to 17-18 dBm at 28 GHz, which is about 2 dB higher than the output 1-dB gain compression power ( $OP_{1\text{dB}}$ ). At such power level, the saturated power gain ( $G_{p,\text{sat}}$ ) at the output stage is about 6-7 dB. The output power level is moderate since the PA is intended to be integrated as a unit PA in the array configuration, either in the PA array or in the phased array system platform, to produce a higher aggregated output power required by the system specification. The class-AB driver is designed to produce 10 dBm  $P_{\text{sat}}$  with 10-11 dB  $G_{p,\text{sat}}$ , resulting in overall 17-18 dB  $G_{p,\text{sat}}$  for the 2-stage PA. This requires about 1 mW input power to deliver the required 50-60 mW of the saturated output power to the 50- $\Omega$  load.

#### 4.5.1 Inverse Class-F Output-Stage Amplifier

##### I. $R_{\text{opt}}$ and Device Sizing

In the output stage design, the first step is to choose an optimum resistance  $R_{\text{opt}}$ , which involves rather complicated tradeoffs for mm-Wave integrated PAs, particularly for silicon PAs based on a harmonic impedance tuning architecture. In the silicon PAs, a smaller  $R_{\text{opt}}$  is often preferable for containing transistor reliability issues under the constraint of the supply voltage ceiling capped by the device breakdown voltage, for a given maximum power level. The smaller  $R_{\text{opt}}$ , however, necessitates a larger DC current, requiring a larger transistor size to meet an

optimum current density for a high  $f_T$ . The larger device size, in turn, will add more stray capacitances sprouted by intrinsic or extrinsic device and layout parasitics, limiting the device speed and therefore restricting the achievable power gain and PAE at mm-Wave.

Furthermore, similar to the requirement on the harmonic impedance magnitude in the class-F PAs depicted in [16], for noticeable half-sinusoid collector voltage and quasi-rectangular current waveforms, the load impedance should be several times (typically three times at least) greater and smaller than the fundamental impedance at the 2<sup>nd</sup>- and the 3<sup>rd</sup>-harmonic bands, respectively. In the silicon IC process, due to the finite passive components  $Q_s$ , the achievable maximum impedance for emulating an open circuit is typically on the order of several 100's ohm at the 2<sup>nd</sup>-harmonic band. Similarly, the effective short circuit impedance will be limited to several 1's ohm at the 3<sup>rd</sup>-harmonic band. In this design  $R_{opt}$  is set to around 40-45  $\Omega$  to guarantee at least better than 4-5 times of impedance contrast between at the fundamental and at the harmonic bands for a distinctive inverse class-F waveform shaping. After setting  $R_{opt}$ , the emitter length of  $Q_2$  is optimized to  $l_e=2\times 13 \mu\text{m}$  where the current density becomes an optimum of 1.4 mA/ $\mu\text{m}$  from 2.3 V supply voltage, achieving a peak  $f_T$  of 180 GHz when the output power reaches 15 dBm OP<sub>-1dB</sub>. This maximizes power gain and thus PAE at the saturated output power level for the given 0.13- $\mu\text{m}$  SiGe BiCMOS process.

## II. Estimation of Large-Signal Collector Capacitance

To design the load network, it needs to determine the collector node parasitic capacitance  $C_3$  first under the presence of the compressed output signal. For this, with the blindness of a large-signal transistor model, one practical way to estimate the large-signal capacitance is relying on a harmonic loadpull simulation. As seen in Fig. 4-6 (a), the existence of  $C_3$  makes the optimum load for peak PAE to be purely inductive at the  $2\omega_0$  frequency and the optimum inductance is the conjugation of the  $C_3$  impedance. From the 2<sup>nd</sup>-harmonic loadpull simulation conducted at the OP<sub>-1dB</sub> output power level, it is found that  $Z_{opt}\approx j44-j47 \Omega @2\omega_0$  ( $2\pi\cdot 56$  Grps), which corresponds to  $C_3 \approx 60\sim 65$  fF. This requires effective inductance of 495~540 pH at 28 GHz and 124~135 pH at 56 GHz from the load network for resonating  $C_3$ . It is easily confirmed that by adding a fictitious  $C_x \approx -65$  fF in parallel with  $C_3$  at the collector node, the optimum impedance point moves to an ideal open position in the Smith chart as shown in Fig. 4-6 (b). The transistor layout interconnects after the EM modeling are included in the loadpull simulations. Apparently, it is seen that the peak

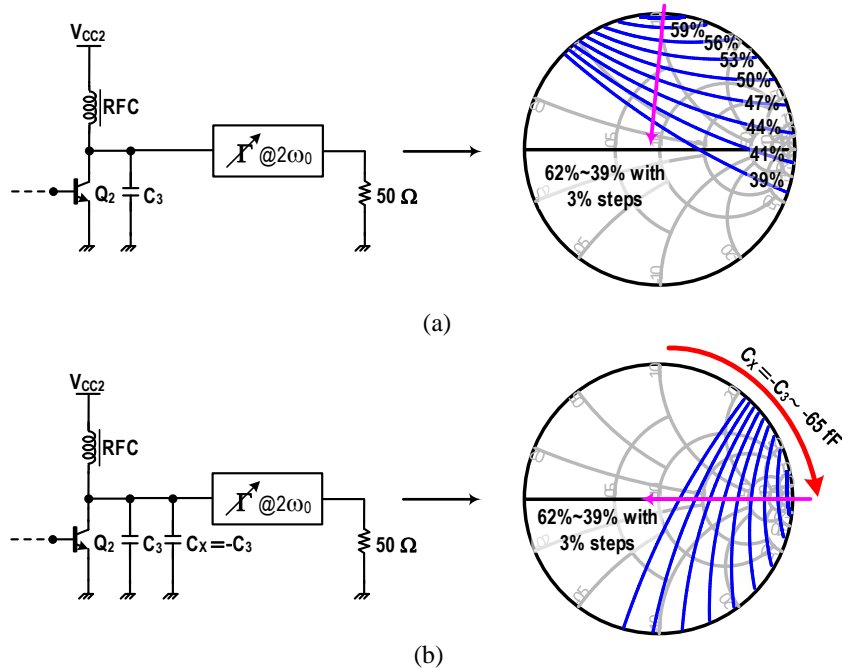


Fig. 4-6. 2<sup>nd</sup> harmonic load pull simulation for estimation of the large signal collector capacitor with  $P_{out} = 17$  dBm at 28 GHz: (a) 2<sup>nd</sup> harmonic load pull simulation set up time-domain waveforms, and PAE contours on 2<sup>nd</sup> harmonic impedance locus, (c) PAE contours when collector capacitor ( $C_3$ ) is neutralized with  $C_x = -C_3$ .

achievable PAE reduces as the second harmonic load becomes lossy and moves inside the Smith chart because of an active power dissipation at the  $2\omega_0$  frequency.

### III. Harmonically Tuned Load Design

The passive component design starts with finding  $L_1$  based on the assumptions of  $L_2 \approx 1.3L_1$  and  $M \approx 0.6L_1$ , which are made in *Section II*. By setting  $A=|i_2/i_1|=C_3/C_1=1$  in (4-11) (e.g.  $C_1=65$  fF),  $L_{eff1}=L_1+M=1.6L_1$  and  $L_{eff2}=L_2+M=1.46L_2$ , effectively enhancing the quality factors by 60% and 46% in the primary ( $L_1$ ) and the secondary ( $L_2$ ) inductors, respectively, at the 2<sup>nd</sup>-harmonic band ( $\phi=0$ ). This Q enhancement is desirable to create a higher 2<sup>nd</sup>-harmonic impedance for better voltage peaking. The required  $L_1$  can be found by the following  $2\omega_0$  resonance condition,

$$\frac{1}{\sqrt{L_{eff1}C_1}} = \frac{1}{\sqrt{1.6L_1C_1}} = 2\omega_0. \quad (4-18)$$

which gives  $L_1=77$  pH. Consequently,  $L_2=1.3L_1=100$  pH and  $M=0.6L_1=46$  pH. After completing the final layout, about 5 fF of parasitic layout capacitance is added to  $C_1$ , which

decreases the required inductances. As disclosed in *Section II*, the final EM optimized values including parasitic layout inductances and capacitances are  $L_1=75$  pH,  $L_2=103$  pH, and  $M=42$  pH.

In the parallel path, the resonance conditions at the  $\omega_0$  and  $2\omega_0$  frequencies establish the following design equations,

$$L_2 + \underbrace{\left( L_3 + \frac{L_4}{1 - (\omega_0/\omega_r)^2} \right)}_{L_{eq3}(\omega_0) \text{ in (5)}} = \frac{1}{C_3 \cdot \omega_0^2}. \quad (4-19)$$

and

$$\underbrace{\left( L_2 + M/A \right)}_{L_{eff2} @ 2\omega_0} + \underbrace{\left( L_3 + \frac{L_4}{1 - (2\omega_0/\omega_r)^2} \right)}_{L_{eq3}(2\omega_0) \text{ in (5)}} = \frac{1}{C_3 \cdot (2\omega_0)^2}. \quad (4-20)$$

where  $L_2$  and  $M$  are known, and  $A$  is set to 1 @  $2\omega_0$  ( $2\pi \cdot 56$  Grps). For a specific  $\omega_r$ , using (4-19) and (4-20) a set of  $\{L_3, L_4, C_2\}$  is determined. Then, for a given solution set of  $\{L_3, L_4, C_2\}$ , the frequency-dependent inductances of  $L_{eff1}$  and  $L_{eff2}$  can be found from (4-12a) and (4-12b) at the  $2\omega_0$ -band. Amongst viable solutions, the optimum set of  $\{L_3, L_4, C_2\}$ , and therefore  $L_{eff1}$  and  $L_{eff2}$ , can be determined graphically-

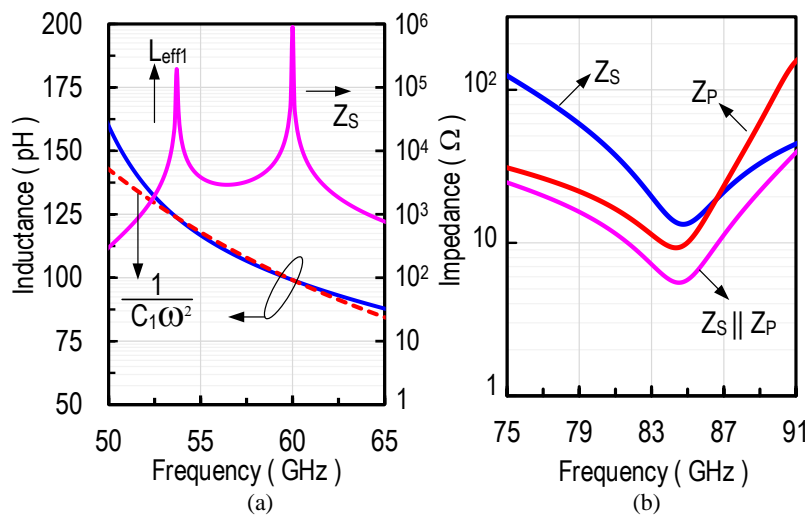


Fig. 4-7. (a) Effective inductance ( $L_{eff1}$ ) and required inductance  $[1/(C_1\omega^2)]$  for  $2f_0$ -resonance, and resonant tank impedance ( $Z_S$ ), (b) series ( $Z_S$ ), parallel ( $Z_P$ ) and total impedance ( $Z_S \parallel Z_P$ ) at  $3f_0$ -band.



The ideal  $L_{eff1}$  to completely resonate out  $C_1$  in the  $L_1$ - $C_1$  tank must be  $1/(C_1\omega^2)$  which is displayed as a dotted line in Fig. 4-7 (a). The  $L_{eff1}$  locus for  $\omega_r=2\pi\cdot 35$  Grps best fits with the ideal  $L_{eff1}$  trajectory until well above the  $2\omega_0$  frequency, roughly 56-to-60 GHz. When  $\omega_r=2\pi\cdot 35$  Grps ( $\sim 1.25\omega_0$ ), the optimized passive values are  $L_3=62$  pH,  $L_4=133$  pH, and  $C_2=156$  fF. Because of the frequency tracking capability of  $L_{eff1}$  the  $L_1$ - $C_1$  tank can sustain a high impedance resonance mode over a wideband in the vicinity of the 2<sup>nd</sup>-harmonic frequency. For instance, in Fig 4-7 (b) when  $\omega_r=2\pi\cdot 35$  Grps dual resonances occur at 56 GHz and 60 GHz and it keeps the series path impedance ( $Z_s$ ) greater than 3-4 k $\Omega$  in between the resonances. While  $Z_s$  eventually decreases to 700-800  $\Omega$  range when including finite component Qs and layout parasitic effects, this effectively traps the 2<sup>nd</sup> harmonic PA current and makes an open circuit from the PA collector to the 50- $\Omega$  load at the  $2\omega_0$ -band. The parallel path ( $Z_p$ ) also resonates at 56 GHz and maintains greater than 500  $\Omega$  ( $> 10R_{opt}$ ) at  $56\pm 1$  GHz, and better than 200  $\Omega$  ( $> 4R_{opt}$ ) over  $56\pm 2$  GHz range, suitable for the intended class-F<sup>-1</sup> operation at the center of 28 GHz with about 1 GHz of RF bandwidth coverage.

The finding of  $L_{M1}$  and  $C_{M,eq}$  in Fig. 4-4 (c) requires a numerical analysis at the 3<sup>rd</sup>-harmonic band. Based on the prior setting of the passive components,  $L_{eq3}(\omega)$  in (4-5) becomes 34 pH at  $\omega = 3\omega_0$ . This necessitates  $L_{eff2} = L_2 - M/A = -34$  pH and subsequently  $J_{21} = 0.31e^{j\pi}$  for the series resonance in the parallel path ( $Z_p$ ) at the 3<sup>rd</sup>-harmonic frequency, bolstering that  $i_1$  and  $i_2$  are anti-phase ( $\phi=\pi$ ). Consequently, the effective inductance at the primary side is  $L_{eff1} = L_1 - MA \approx 64$  pH. For the series resonance in the series path ( $Z_s$ ), the following design equation can be made at the  $3\omega_0$  frequency,

$$L_{eq4}(3\omega_0) = -\frac{L_{eff1}}{1 - 9\omega_0^2 L_{eff1} C_1} = L_{M1} - \frac{1}{9\omega_0^2 C_{M,eq}} = 269 \text{ pH}. \quad (4 - 21)$$

Using (4-21) and considering the optimum matching requirement and parasitic interconnect effects at the fundamental frequency, it is determined that  $L_{M1}=325$  pH and  $C_{M,eq}=64$  fF ( $C_{M1}=15$  fF and  $C_{M2}=75$  fF). The impedance simulation results at the  $3\omega_0$  frequency band, 84-to-89 GHz, in Fig. 4-7 (c) shows the operation: after the series resonance in each path ( $Z_p$  &  $Z_s$ ). TABLE II summarizes the final optimized passive components. All inductors are custom made and verified using the Sonnet EM solver.  $L_3$  and  $L_{M1}$  are implemented utilizing line inductors including the

layout interconnect lines.  $L_4$  is a single-turn spiral inductor. After completing layout, the EM simulations show about  $200\text{-}250\ \Omega$  ( $> 4R_{\text{opt}}$ ) range of the 2<sup>nd</sup>-harmonic impedance at 55-58 GHz and  $8\text{-}12\ \Omega$  ( $< \frac{1}{4}R_{\text{opt}}$ ) range of the 3<sup>rd</sup>-harmonic impedance at 82-90 GHz.

#### IV. Waveform, Load-Line and PAE Simulation Results

Fig. 8 (a) shows the simulated collector current and voltage waveforms at 28 GHz when the PA output power at the  $Q_2$  collector node is around 17 dBm ( $OP_{-1\text{dB}}$ ). The dotted lines are ideal maximally flat class-F<sup>-1</sup> voltage and current waveforms based on the following equations [16]:

$$v_{CE}(\theta) = V_{DC} \left( 1 - \sqrt{2} \cos\theta + \frac{1}{2} \cos 2\theta \right) \quad (4 - 22)$$

and

$$i_{CE}(\theta) \cong I_{DC} (1 - 1.207 \cdot \cos\theta + 0.28 \cdot \cos 3\theta - 0.073 \cdot \cos 5\theta). \quad (4 - 23)$$

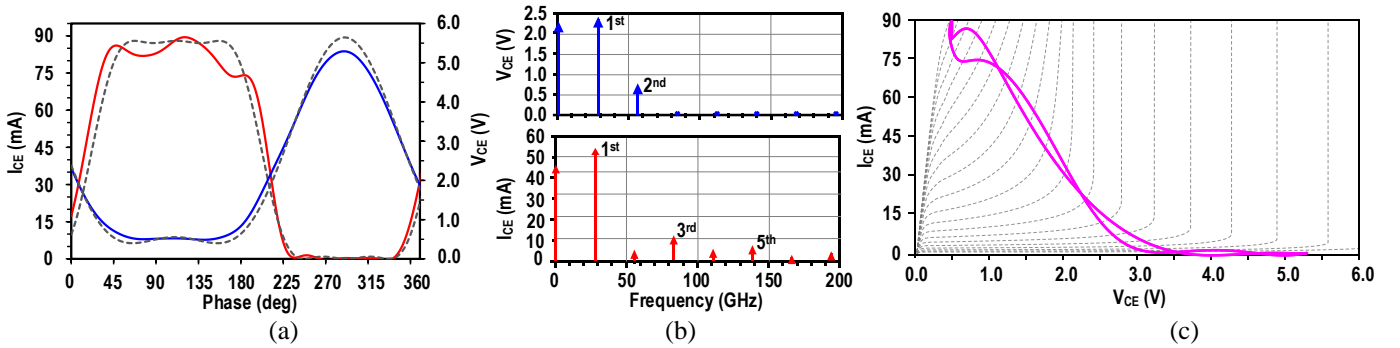


Fig. 4-8. Simulated collector current and voltage waveforms at 28 GHz at  $OP_{1\text{dB}} = 18$  dBm: (a) time-domain waveforms, (b) harmonic components:  $V_{DC} = 2.3$  V,  $V_{\text{fund}} = 2.4$  V,  $V_{2\text{nd}} = 0.7$  V, and  $I_{DC} = 46$  mA,  $I_{\text{fund}} = 52$  mA,  $I_{3\text{rd}} = 11$  mA,  $I_{5\text{th}} = 4.8$  mA, (c) AC load-line.

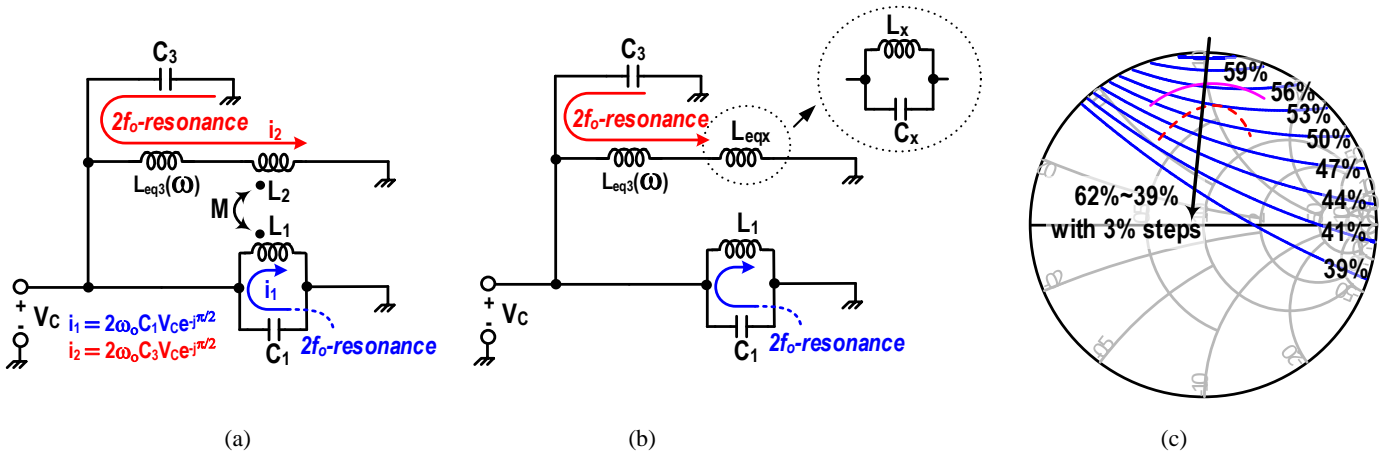


Fig. 4-9. Comparison of achievable peak PAE in the proposed load and conventional LC-based load at  $2\omega_0$ -band: (a) equivalent load network at  $2\omega_0$ -band for c, (b) peak PAE contours after loadpull simulation for 2<sup>nd</sup> harmonic load for proposed inductor based load (pink solid line) and conventional load (dot red line).

The transistor knee voltage is around 0.5 V. Fig. 4-8 (b) shows major harmonic spectra of the waveforms. The signatures of the class-F<sup>-1</sup> waveform are clearly observable: half-sinusoidal voltage peaking bred by the 2<sup>nd</sup>-harmonic voltage spectrum and quasi-rectangular current waveform shaped mainly by the visible 3<sup>rd</sup>- and 5<sup>th</sup>-harmonic current spectra in Fig. 4-8 (b). The transistor is biased at a class-AB point ( $V_{BE}=0.83$  V), which is appreciable in the ac load-line shown in Fig. 4-8 (c). The simulated PAE at the output of the collector is near 58% which, however, reduces to 48% at the 50- $\Omega$  load because of  $\sim 0.8$  dB power loss incurred by the finite passive component  $Q_s$  at the fundamental signal band.

Fig. 4-9 illustrates the PAE advantage of the proposed coupled-inductor based load over conventional LC loads. The 2<sup>nd</sup>-harmonic load-pull contours, conducted under the presence of the OP<sub>-1dB</sub> output power, show peak PAEs at different level of the 2<sup>nd</sup>-harmonic impedance. On top of that are the solid-pink and dashed-red lines which respectively show the 2<sup>nd</sup>-harmonic impedance traces from 54 GHz to 60 GHz for the proposed load and conventional LC load. In the comparative simulations, both networks achieve peak PAE at 28 GHz where the 2<sup>nd</sup>-harmonic impedance maximizes. However, the coupled-inductor based load achieves 2-8% better and more flat PAE than the conventional network over the  $2\omega_0$  frequency range, revealing more robust PAE tolerance to the operation frequency. This is mainly due to the Q enhancement effect in both the primary and secondary inductors and, at the same time, a wider high-impedance at the  $2\omega_0$ -band in the primary inductor. Note that a high-Q and a wide bandwidth are physically incompatible. In the proposed load, however, because of the frequency-dependent inductance modulated by the coupled-inductors, it is possible to implement both high-Q and wideband the 2<sup>nd</sup>-harmonic trapping LC resonator in the signal path for better PAE performance, as depicted in Fig. 4-7 (b).

#### 4.5.2 Class AB Driving Amplifier and Inter-Stage Matching

In the driver, the T-network composed of the T-line inductor  $L_{D1}$  (180 pH) and the MIM capacitors,  $C_{D1}$  (93f fF) and  $C_{D2}$  (143 fF) matches the input to 50  $\Omega$  over 27-31 GHz. The size and bias point of  $Q_1$  ( $l_e=16$   $\mu\text{m}$ ) and  $V_{CC1}$  (2 V) are optimally set to drive the output stage into saturation when the driver output power is near 9 dBm OP<sub>-1dB</sub>. As seen in Fig. 4-10, the load-pull simulations

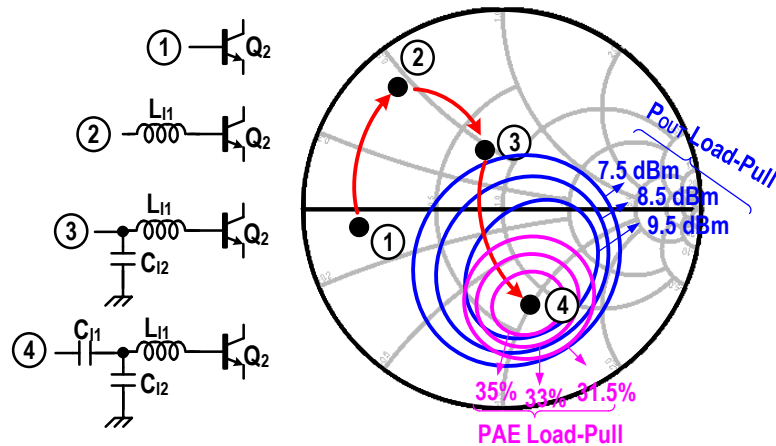


Fig. 4-10. Load-pull design of the inter-stage matching network.

reveal that the optimum inter-stage impedance to achieve  $>9$  dBm driver output power with  $> 35\%$  driver PAE is capacitive ( $34-j51 \Omega$ ). Therefore,  $L_{D1}$  (220 pH) in Fig. 4-5 resonates out only a portion of  $C_{D3}$  to provide the optimum capacitive impedance. A step-by-step approach to match a low input impedance of  $Q_2$  to the optimum inter-stage impedance is illustrated in Fig. 4-10. Design values are  $L_{11}=145$  pH,  $C_{11}=67$  fF, and  $C_{12}=153$  fF. After cascading the driver, overall 2-stage PA's PAE is 44% at 28 GHz in simulations.

### 4.5.3 Experimental Results

The PA is fabricated in IBM8HP 0.13  $\mu\text{m}$  SiGe BiCMOS process ( $f_T/f_{\text{max}}=180/220$  GHz). Fig. 4-11 shows the PA die photograph and its size is  $0.55 \times 0.93 \text{ mm}^2$  including all pads. The PA's small-signal performance is measured on-wafer after SOLT calibration. No instability is observed. Fig. 4-12 (a) shows the measurement and simulation results of S-parameters at the same class-AB bias points as simulations ( $V_{CC1}/V_{CC2}=2/2.4$  V and  $I_{CC1}/I_{CC2}=3/10$  mA):  $S_{11}<-10$  dB,  $S_{22}<-10$  dB and  $S_{21}=19.5\text{-}21.5$  dB over 27-29 GHz.

For the large-signal performance measurement, the PA's input power is sampled using a directional coupler. Then, the sampled input power and PA's output power are measured using R&S power sensors and power meter. RF cable losses are carefully characterized and de-embedded over the operational frequency range. Fig. 4-12 (b) shows the large-signal measurement results at 28 GHz. In general, the measured results are in good agreement with simulation data which is plotted in dotted lines. The measured  $P_{\text{sat}}$  is 16.5 dBm and  $OP_{-1\text{dB}}$  point is 15 dBm, which

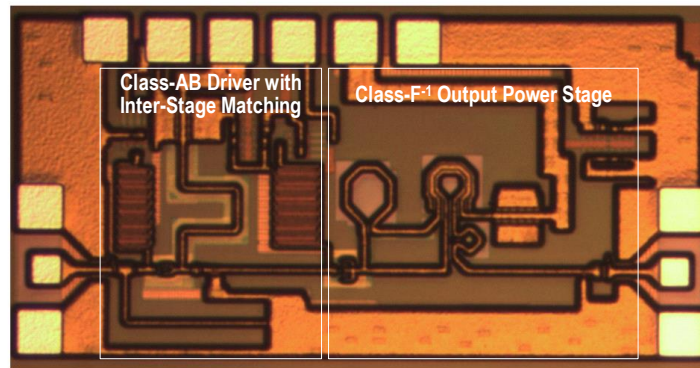


Fig. 4-11. Chip photograph (size: 0.55×0.96 mm<sup>2</sup>).

is about 1.5-2 dB less than the simulations. When  $P_{out}=15$  dBm, the output stage operates in class- $F^{-1}$  mode and the measure peak PAE is 42%. The PAE of the output stage itself can be as high as 45% when the class-AB PAE is de-embedded. The measured gain error from the simulation is around 1.5 dB, which causes about 2-3% PAE reduction of the simulation value. When  $P_{out}$  is backed off by 6 dB from the 15 dBm  $OP_{-1dB}$ , the PA operates in a class-AB mode and the measured PAE is 20%.

To characterize the frequency dependency of the efficiency, the PAE has been measured over 26-31 GHz and results are shown in Fig. 4-12 (c). The PAE is higher than 40% at 27.8-29.3 GHz and higher than 38% at 26.7-30.8 GHz with  $\sim 15.5$  dBm of corresponding output power. Fig. 4-12 (d) shows the measured PAE with varying the output stage's supply voltage from 1.3 V to 2.5 V at 28 GHz to characterize the supply dependency of the PAE. The PA can maintain higher than 40% of peak PAE over 2-2.5 V supply variations and the corresponding  $P_{out}$  is greater than 15 dBm, revealing the PAE robustness to the supply variation.

In order to characterize in-band and out-of-band linearity performances, modulated signals have been applied to the PA. The R&S signal source SMW200A provides the PA with 23-bit pseudo random binary sequence with arbitrary digital modulation at the carrier frequency up to 40 GHz. The PA output is fed to the R&S spectrum analyzer, FSW67, to evaluate EVM, ACPR, and corresponding average output power ( $P_{out,ave}$ ) and average power efficiency ( $PAE_{ave}$ ) of the modulated signals. The maximum modulated signal bandwidth from the available equipment is 8.4 MHz. The measurements have been performed for various modulation schemes, including QAM, 8-PSK, 16-QAM, 64-QAM, and 128-QAM modulation formats.

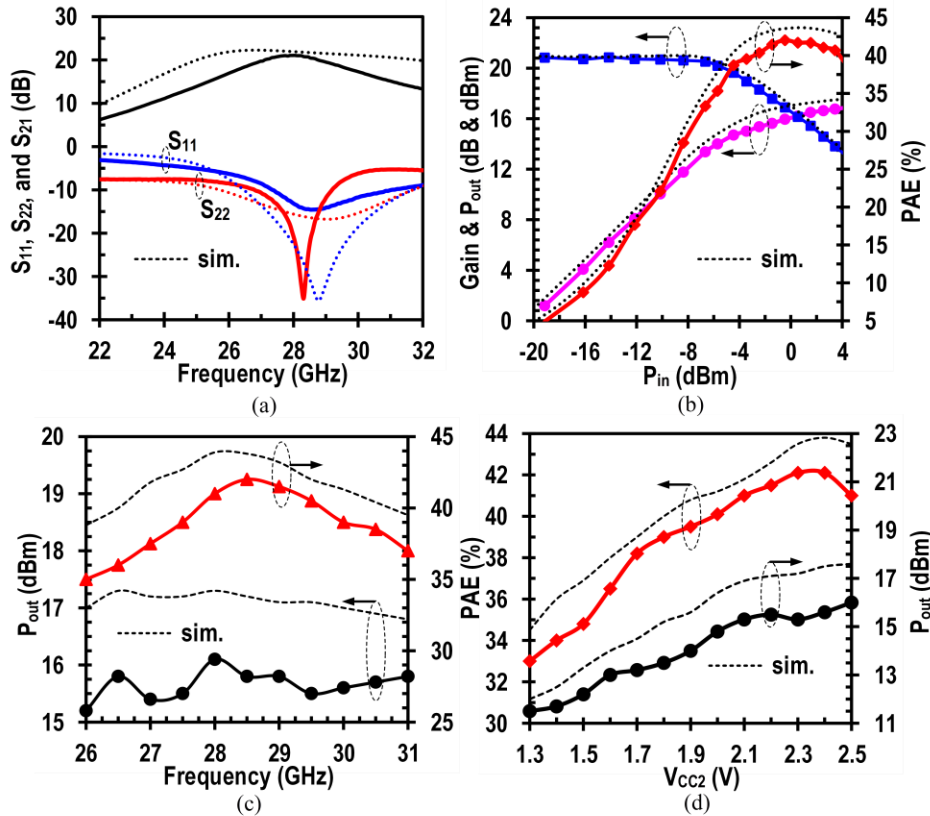


Fig. 4-12. Measured performances of the PA: (a) gain, input and output matching, (b) power gain, output power, and PAE versus input power, (c) peak PAE and corresponding output power versus frequency, and (d) peak PAE and corresponding output power versus supply voltage of the output stage.

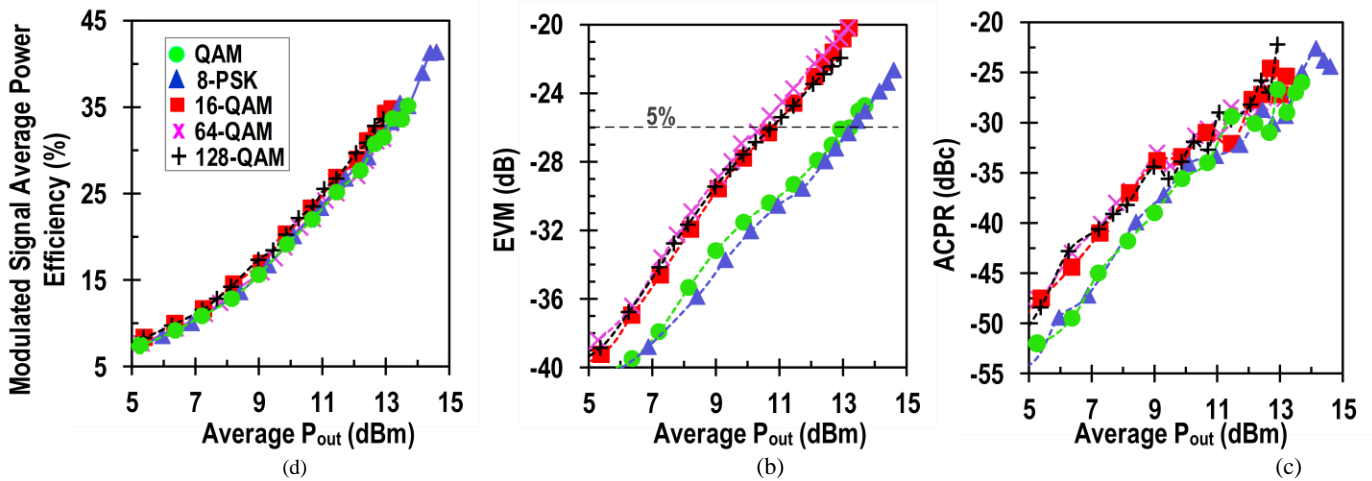


Fig. 4-13. The measured modulation power efficiency, EVM, and ACPR versus average output power at 28 GHz for different modulation schemes: (a) power efficiency, (b) EVM, and (c) ACPR at 8 MHz offset bands. ACPR is presented in absolute magnitude scale.

Fig. 4-13 (a) shows the measured EVMs for different modulation schemes versus  $P_{\text{out,ave}}$ . For the QPSK and 8-PSK signals, the EVM becomes -26 dB (5%) when  $P_{\text{out,ave}}$  reaches 13 dBm. For the 16/64/128-QAM signals the peak-to-average-power-ratio (PAPR) is typically about 3 dB higher than that of the QPSK/8-PSK signals. Therefore, for the 16/64/128-QAM signals, the measured  $P_{\text{out,ave}}$  resulting in 5% EVM is around 10 dBm, 3dB smaller than that of the QPSK/8-PSK signals. Fig. 4-13 (b) shows measured ACPR at  $\pm 8$  MHz offset from the carrier center. Typically, the ACPR is  $< -22$  dBc near the 15 dBm  $OP_{-1\text{dB}}$ . Fig. 4-13 (c) shows the measured  $PAE_{\text{ave}}$  of the PA. Apparently, the QAM and 8-PSK signals exhibit the best power efficiency for a given EVM: at the  $P_{\text{out,ave}}$  corresponding to 5% EVM the QAM/8-PSK signals achieve  $\sim 32.5\%$  modulated power efficiency while for the 16/64/128-QAM signals the  $PAE_{\text{ave}}$  corresponding to 5% EVM is  $\sim 20\%$ . The measured  $PAE_{\text{ave}}$  reaches 42% when  $P_{\text{out,ave}}$  approaches 15 dBm, matches well with results in Fig. 4-12 (b).

It should be noted that the measurement modulation signal bandwidth is limited mainly by the test equipment. The PA's impedance matching, gain, and efficiency bandwidth are on the order of several GHz range and therefore it can certainly process multi-Gbps high-speed input signal. For instance, from Fig. 4-12, the input and output VSWR are better than 2:1, and gain variation is less than 1 dB from the peak 20.5 dB over the 1 GHz of instantaneous bandwidth from 28 GHz to 29 GHz. The PAE variation is also less than 2%. Since the 1 GHz bandwidth is relatively small fraction of the carrier frequency (less than 4% of fractional bandwidth), the PA can maintain the modulation signal performance over the bandwidth.

## 4.6 Summary

This chapter presents a unique coupled-inductor based harmonic impedance modulator that terminates the 2<sup>nd</sup>- and 3<sup>rd</sup>-harmonic impedances appropriately for an optimal inverse class-F operation. An inverse class-F power amplifier driven by a class-AB preamplifier, implemented in 0.13- $\mu\text{m}$  SiGe BiCMOS process. The class-F<sup>-1</sup> PA employs At saturation mode, the PA operates in a class-F<sup>-1</sup> mode and achieves 42 % peak PAE at 28 GHz with 15 dBm  $OP_{-1\text{dB}}$  output power. At power backoff mode, typically 6-dB backoff from the 15 dBm  $OP_{-1\text{dB}}$  power, the PA operates in a class-AB mode and the measured PAE can reach to 20%, one of the best performances reported so far in silicon based PAs. The coupled inductors can be integrated compactly at mm-Wave,

claiming no particular area penalty but providing powerful harmonic impedance control, promising for a high efficiency at mm-Wave.

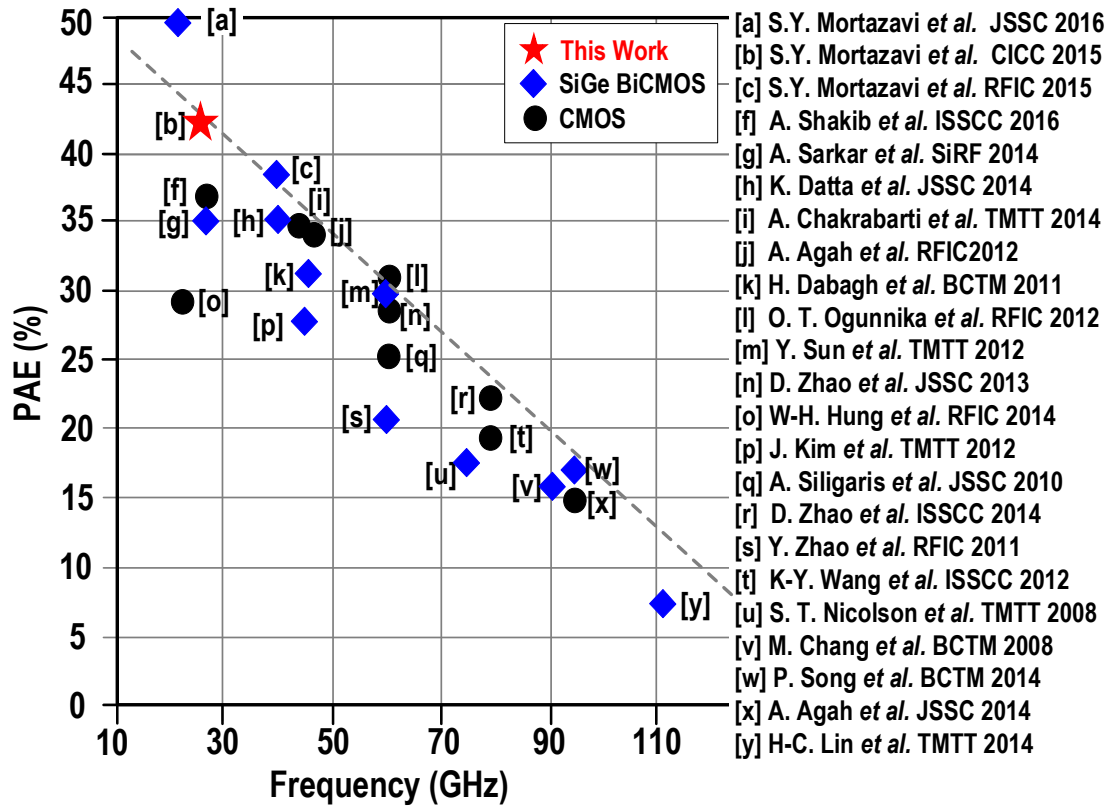


Fig. 4-14. PAE performance of the mm-wave silicon PAs





# 5 $\lambda/4$ -Transformer Based Harmonic Load Modulation at mm-wave

## 5.1 Introduction

A complex high-order LC filter can be utilized to terminate 2<sup>nd</sup>/3<sup>rd</sup>-harmonic impedances effectively, shaping highly efficient collector waveforms up to microwave frequencies. However, at mm-Wave the complexity sacrifices efficiency since the passive losses bounded by the filter complexity become exacerbated with acceleration of frequency over 30GHz. This paper presents Class-F<sup>-1</sup> PA employing more compact  $\lambda/4$ -transformer based impedance modulator that explicitly terminates 2<sup>nd</sup> harmonic impedance only and relies on native low capacitive reactance to short all other higher-order harmonics. This reduces filter complexity substantially and loss thereof, exceeding PAE over 40% at 39.5-42GHz with 43% peak PAE and 38% of 3dB-back-off PAE at 40.5GHz.

## 5.2 $\lambda/4$ -Transformer Based Harmonic Tuning for mm-Wave PAs

### 5.2.1 2-stage Q-band Class-F<sup>-1</sup> PA

The 2-stage PA in Fig.5-1 is a cascade of two modularized PAs hinged on identical Class-F<sup>-1</sup> amplifier topology adopting  $\lambda/4$  transmission-line (T-line) based harmonic filter. The maximal saturation output power ( $P_{sat1}$ ) in the output stage is 18dBm with 6dB power gain ( $G_{P1}$ ), developing < 5.5V peak voltage swing on the 50 $\Omega$   $R_{opt1}$  from 2.4V supply voltage and yet assuring the transistor reliability ( $BV_{CBO}=5.5V$ ). The generator  $Q_1$  ( $A_e=27.6 \times 0.12 \mu m^2$ ) is biased at a class-AB point ( $V_{BEQ1}=0.84V$ ,  $I_{CEQ1}=10mA$ ) and sized for an optimal *rms*-current density of 11.7mA/ $\mu m^2$  for  $f_T \geq 180GHz$  at the fundamental frequency ( $f_o$ ) of 39-42GHz when the output power reaches to a compression point ( $OP_{-1dB}=16dBm$ ). The driver supply voltage, and size and bias of  $Q_2$  are scaled properly to produce 12dBm driving power in saturation with 8dB power gain on 55 $\Omega$   $R_{opt2}$ . The T-type input matching network composed of  $L_{SM}$ ,  $C_{SM1}$ , and  $C_{SM2}$  transforms a

low base node impedance of  $Q_{1,2}$ , typically  $<10\Omega$ , to the  $R_{opt2}$  and  $R_s$  in the output and driving stage, respectively (Fig.5-1).

### 5.2.2 $\lambda/4$ -Transformer Based Harmonic Load Modulation

The harmonic-dependent impedance inversion in the  $\lambda/4$ -transformer plays a central role in modulating the filter impedance, formalized by  $L_P$ ,  $C_P$ ,  $L_{S1,2}$  and  $C_S$  in Fig. 3-1, dynamically in frequency domain to shape optimal Class-F<sup>-1</sup> waveforms. At the  $f_o$ -band, due to the open-circuit impedance by the  $\lambda/4$ -line the harmonic filter becomes a 4<sup>th</sup>-order shunt ( $L_P$ - $C_P$ )–series ( $L_S$ - $C_S$ ) dual  $f_o$ -resonator, providing a transparent fundamental current path from the generators to the optimum loads. However, at the  $2f_o$ -band (78-84GHz) the  $\lambda/4$ -line becomes short and isolates the PA from the load. This transforms the filter capably into a 2<sup>nd</sup>-order  $2f_o$ -resonator composed of  $L_P//L_{S1}$  and  $C_P$ , loading the generator with a high impedance at the  $2f_o$  frequencies for a sinusoidal voltage peaking. Finally, the 3<sup>rd</sup> ( $3f_o$ ) and higher order harmonics ( $>117$ GHz) will be filtered out

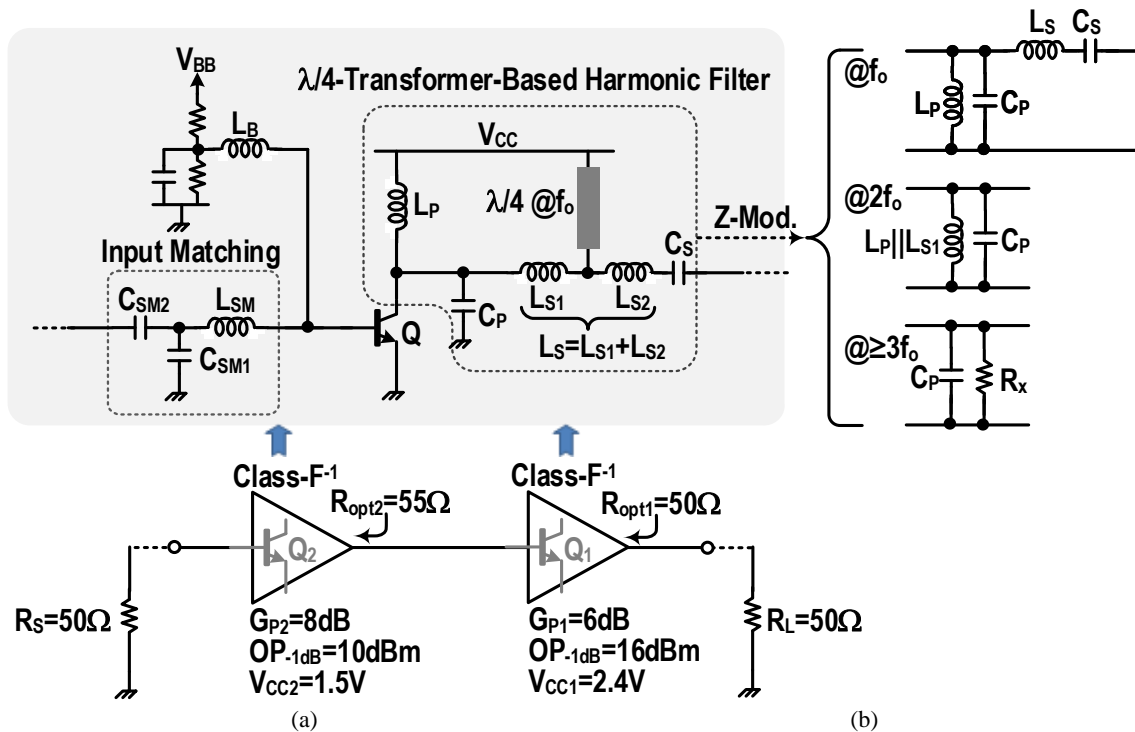


Fig. 5-1: 2-stage 39-42GHz power amplifier: cascade of two Class-F<sup>-1</sup> PAs employing  $\lambda/4$  T-line based harmonic filter.

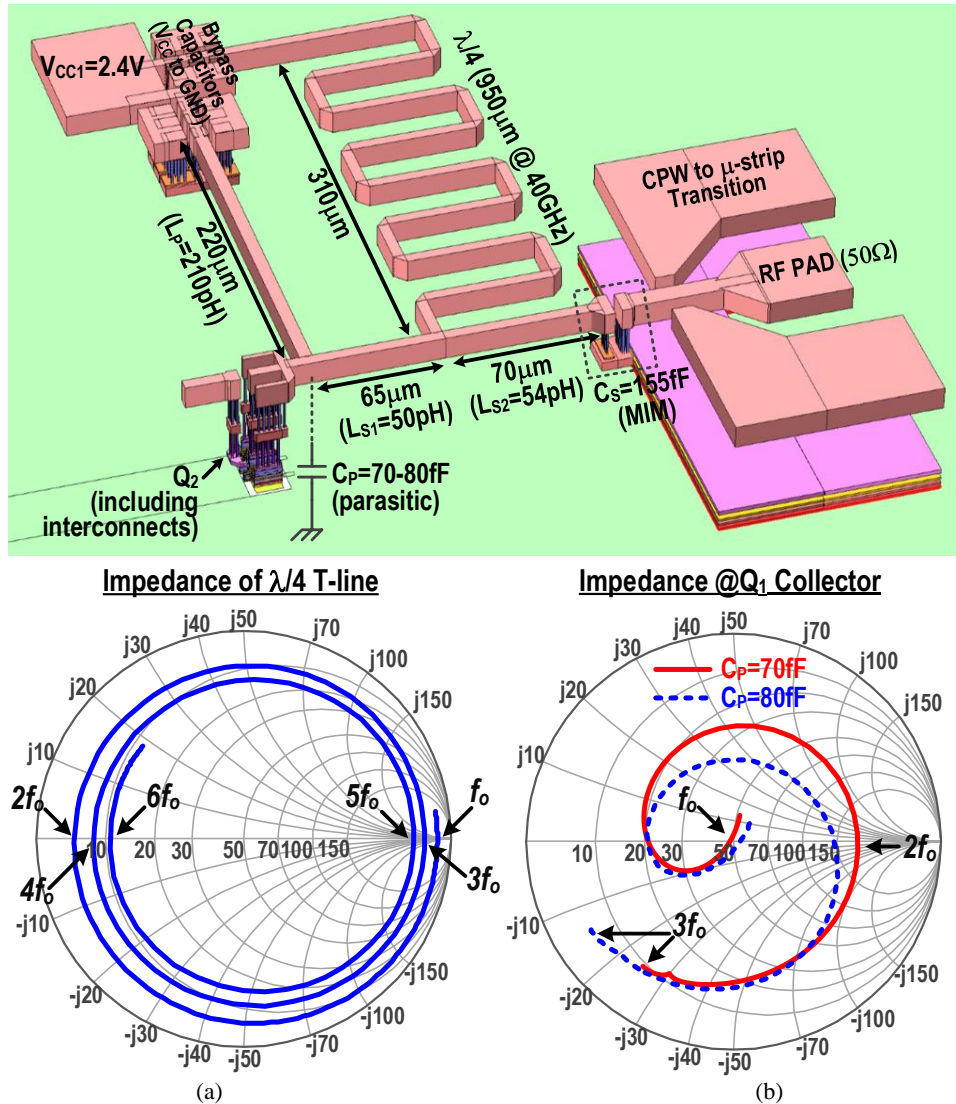


Fig. 5-2: Layout details of the Class-F<sup>-1</sup> output stage (upper) and EM simulation result of the impedance locus of the  $\lambda/4$  transformer (bottom-left) and total impedance seen at the  $Q_1$  collector after completing the load network including the RF pad (bottom-right):  $f_o=39\text{-}42\text{GHz}$ ,  $2f_o=78\text{-}84\text{GHz}$ , and  $3f_o=117\text{-}126\text{GHz}$ .

via a low capacitive impedance ( $Z_{3f_o}$ ) formed by the  $C_p$  in parallel with parasitic resistance  $R_x$  contributed by the finite  $Q$  of the inductors and output resistance of  $Q_{1,2}$ , allowing to shape a 3<sup>rd</sup>-harmonic-rich current peaking. The  $C_p$  is comprised of the transistors intrinsic capacitance plus layout interconnect parasitic, approximately lumped to 70-80fF resulting in  $|Z_{3f_o}| \leq 1/3 \cdot R_{opt}$  at 120GHz; the small reactance causes non-ideal phase shift in the 3<sup>rd</sup>-harmonic voltage and current but negligible impact on the PAE thanks to the relatively small contribution to the overall collector

waveforms. The details on the circuit layout of the output stage for full electromagnetic-wave (EM) simulations are illustrated in Fig. 5-2. The passive component values in the driver are similar but tuned up to accommodate slight different parasitic effect due to the different transistor size. The  $\lambda/4$  ( $l=0.95\text{mm}$  @40GHz)-transformer can be integrated compactly by meandering the line pattern. In fact, the  $L_{S1}$  (50pH) and  $L_{S2}$  (54pH) are single microstrip T-line inductor ( $L_S$ ) and the  $\lambda/4$ -line taps the signal approximately in the middle point of the  $L_S$  to realize a smaller inductor for the  $2f_0$ -resonance. Due to losses in the T-line, the impedance locus of the  $\lambda/4$ -line spirals inward in the Smith-Chart as frequency increases but still upholds the input impedance ( $Z_o^2/Z_L$ ) of  $>1.5\text{k}\Omega$  ( $30 \cdot R_{opt1}$ ) @ $f_0$ ,  $<5\Omega$  ( $0.1 \cdot R_{opt1}$ ) @ $2f_0$ , and  $>700\Omega$  ( $14 \cdot R_{opt1}$ ) @ $3f_0$  by setting the  $\lambda/4$ -line characteristic impedance ( $Z_o$ ) to  $72\Omega$  (Width= $7\mu\text{m}$ ), realizing virtual open/short terminations for the three major harmonics at the bands of interest. The relatively simple and low-order harmonic filter but achieving equal harmonic load modulation as in [18],[20], allows compact integration of the filter within  $\sim 0.15 \times 0.3\text{mm}^2$ , less subject to the loss incurred by layout parasitic or components Q. The EM characterization at the  $Q_1$  collector node after including all passives, interconnects, and RF pad verifies the load impedance transition from the optimum  $50\Omega$  at the  $f_0$ -band, to a high  $150\text{--}200\Omega$  at the  $2f_0$ -band, and to a low  $(5-j15\Omega) \sim (10-j25\Omega)$  at the  $3f_0$ -band, over the nonlinear  $C_P$  drift from  $70\text{fF}$  to  $80\text{fF}$  depending on  $P_{out}$  and harmonic frequencies in Fig.5-2.

In the SPECTRE periodic-steady-state simulation results at  $41\text{GHz}$  shown in Fig.5-3, due to the harmonic load modulation, the 3<sup>rd</sup>-harmonic becomes dominant in the collector current waveforms, introducing the 3<sup>rd</sup>-harmonic induced current peaking, clearly observable as  $P_{out}$  excels  $15\text{dBm}$  in Fig.5-3 (a)①. The current peaking in turn discharges the collector node further, flattening the voltage waveforms in the first-half period. When  $P_{out}$  approaches to  $16\text{dBm}$  ( $OP_{-1\text{dB}}$ ), the 3<sup>rd</sup> harmonic current starts to saturate in Fig.5-3 (a)②, compressing the current waveform. However, as the PA being saturated it produces required 2<sup>nd</sup>-harmonic voltage spectrum that keeps growing as  $P_{out}$  increases in Fig.5-3 (a)③ and inaugurates prominent sinusoidal peaking in the second half period of the voltage waveform. The voltage is unbounded until it reaches a soft breakdown point of around  $5.5\text{V}$  when  $P_{out}=18\text{dBm}$ . The load-pull analyses of driver and output stage confirm  $42\%$  PAE with  $>11\text{dBm}$   $P_{out}$  on the  $55\Omega$   $R_{opt2}$  in the driver, and  $46\%$  PAE with  $18\text{dBm}$   $P_{out}$  on the  $50\Omega$   $R_{opt1}$  in the output PA, resulting in  $>45\%$  cascade PAE at  $41\text{GHz}$  in simulations (Fig.5-3 (b)).

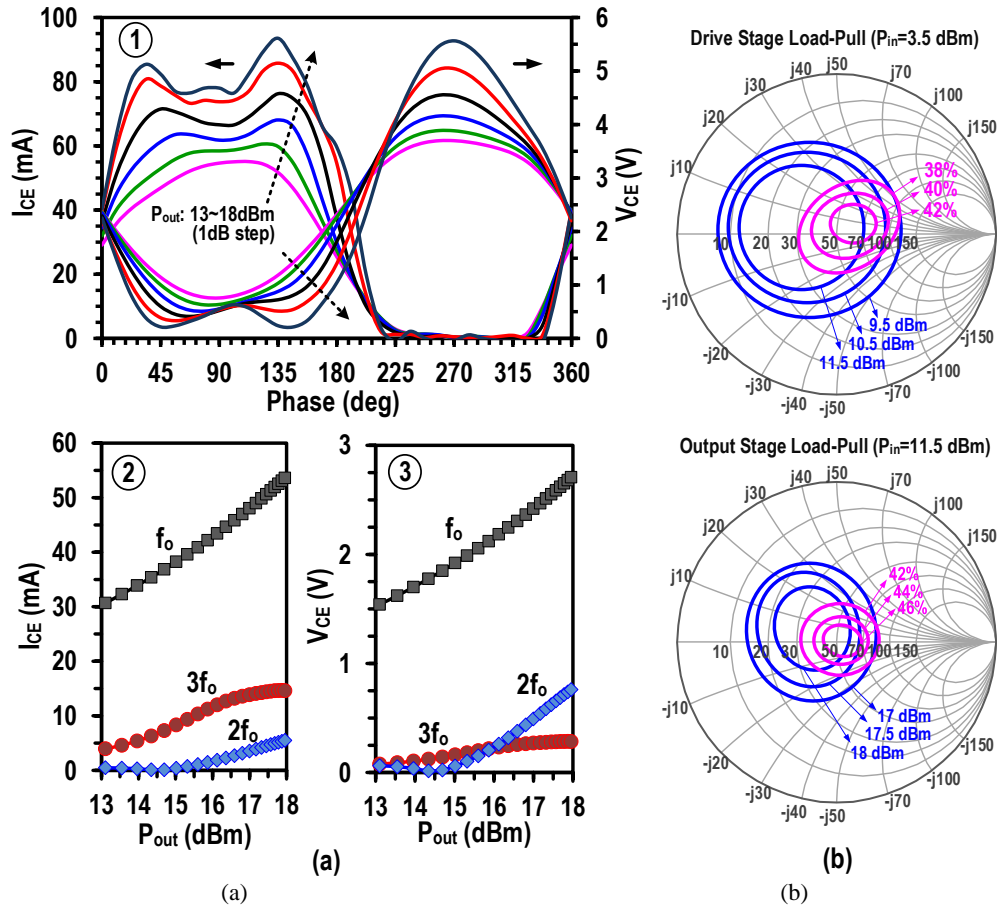


Fig. 5-3: SPECTRE simulation results: (a) ① simulated time-domain collector waveforms at 41GHz ( $f_0$ ), ② spectrum growth of  $f_0$ ,  $2f_0$ , and  $3f_0$  as  $P_{out}$  increases in the collector current ( $I_{CE}$ ), and ③ spectrum growth of  $f_0$ ,  $2f_0$ , and  $3f_0$  as  $P_{out}$  increases in the collector voltage ( $V_{CE}$ ); and (b) load-pull simulation results in the driver stage (upper) and in the output stage (lower).

### 5.2.3 Measurement Results

Fig. 5-4 shows the die photo of the PA implemented in 0.13  $\mu\text{m}$  SiGe BiCMOS technology. The PA occupies  $0.95 \times 0.6 \text{ mm}^2$  including pads. The small-signal performance of the PA is measured through on-wafer testing after standard SOLT calibration with biasing  $Q_{1,2}$  in Class-AB regions ( $V_{CC1}/V_{CC2}=2.4/1.5\text{V}$ ,  $I_{CE1}/I_{CE2}=10/5\text{mA}$ ) and the results are:  $S_{11} < -10\text{dB}$  @36-42GHz,  $S_{22} < -10\text{dB}$  @28-41GHz and  $S_{21}=16\text{-}22\text{dB}$  @36-42GHz (Fig.5-5①). For large-signal characterization, output power and sampled input power are fed to a dual-channel power meter and cable loss is calibrated out carefully at each measurement frequency. At 40.5GHz the peak

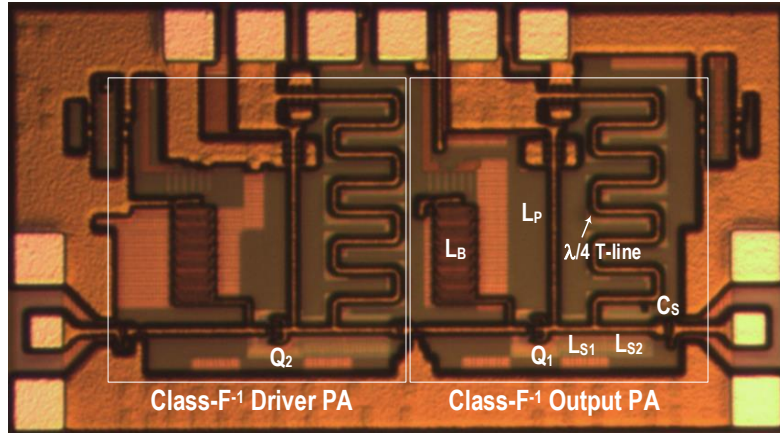


Fig. 5-4: The 2-stage Class<sup>-1</sup> PA chip photograph (chip size: 1.08x0.58mm<sup>2</sup> w/i pads, 0.8x0.45mm<sup>2</sup> w/o pad).

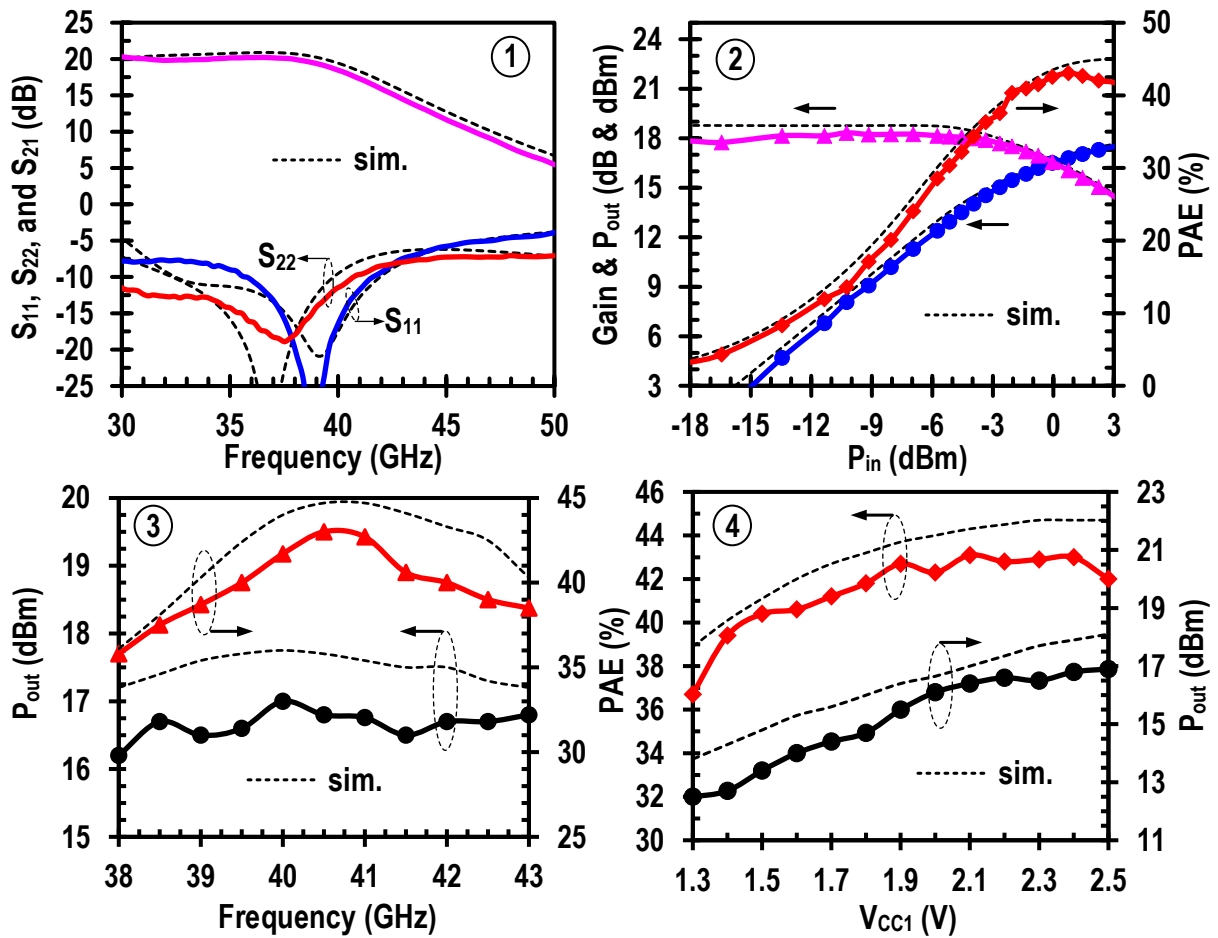


Fig. 5-5: Simulated (dot lines) and measured (*single-tone*) PA performances: ① gain, input and output matching ( $V_{CC1}=2.4V$ ,  $I_{CE}=10mA$ ), ② gain,  $P_{out}$ , and corresponding PAE versus  $P_{in}$  at 40.5GHz ( $V_{CC1}=2.4V$ ,  $I_{CE}=10mA$ ), ③ peak PAE and corresponding  $P_{out}$  versus frequency ( $V_{CC1}=2.4V$ ,  $I_{CE}=10mA$ ), and ④ peak PAE and corresponding  $P_{out}$  versus supply voltage at 40.5GHz

PAE reaches 43% with corresponding 16.5dBm  $P_{out}$ , and measured  $OP_{-1dB}$  and  $P_{sat}$  are 16dBm and 18dBm, respectively. When 3dB and 6dB back-off, the PAE is 38% and 28%, respectively (Fig.5-5②). The measured PAE is >40% @39.5-42GHz with 16.5-17dBm  $P_{out}$  (Fig.5-5③). While  $P_{out}$  decreases monotonically as the supply ( $V_{CC1}$ ) decrease, the PA sustains > 40% PAE over the 1.5-2.5V  $V_{CC1}$ , manifesting a robustness of the PAE to the supply variations (Fig.5-5④). The PA is characterized further by exciting modulated signals at 40GHz of which BW (8.4MHz) is limited by the R&S signal source (SMW200A). As a typical result in 64QAM (PAPR: 3.7dB) case, when the average  $P_{out}$  ( $P_{out,ave}$ ) increases to 13dBm its peak power passes the  $OP_{-1dB}$  and the constellation EVM becomes >5% in Fig.5-6①. Further increase of  $P_{out,ave}$  to 16dBm saturates the PA more and

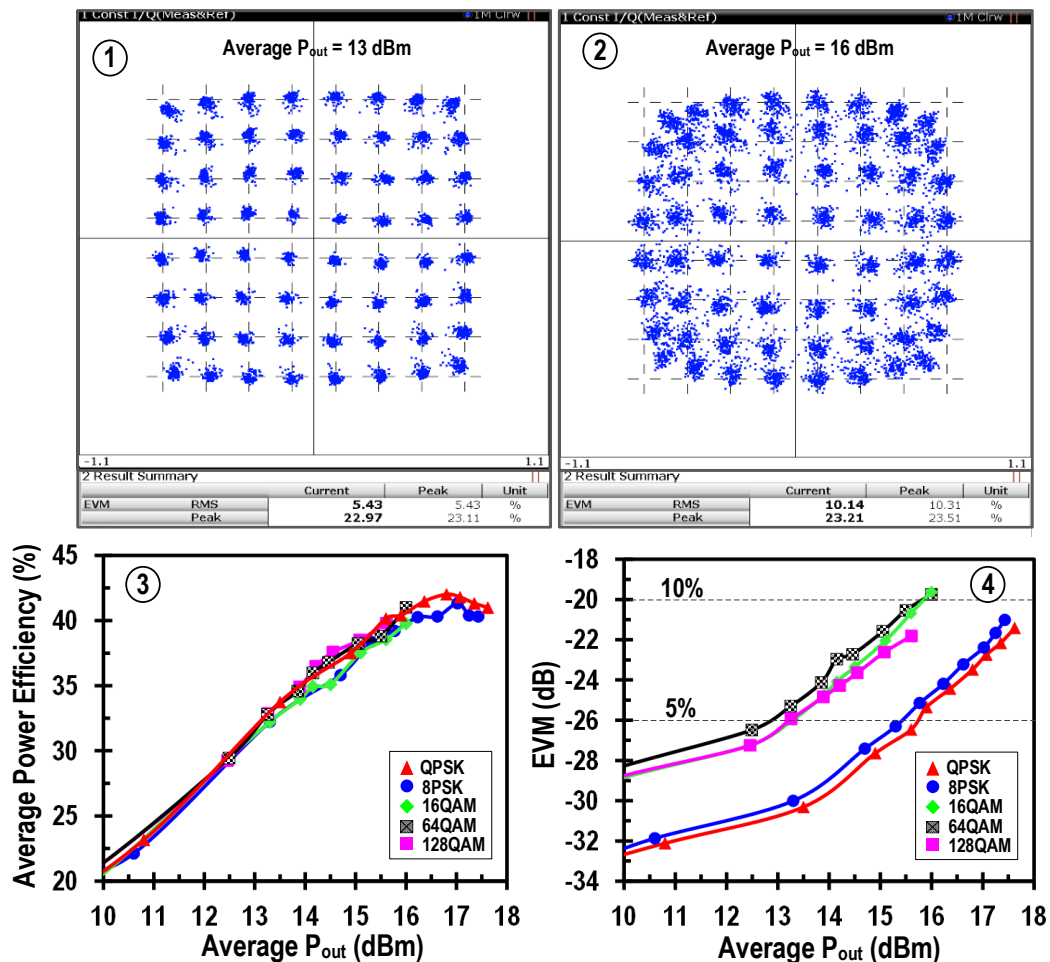


Fig. 5-6 Modulation (BW=8.4MHz with raised cosine filtering, roll-off factor: 0.2) test results for QPSK, 8PSK, 16QAM, 64QAM, and 128QAM formats at 40GHz: ① typical 64QAM constellation @ $P_{out,ave}$ =13dBm, ② typical 64QAM constellation @ $P_{out,ave}$ =16dBm, ③ modulated signal average power efficiency, and ④ EVM versus average output power.



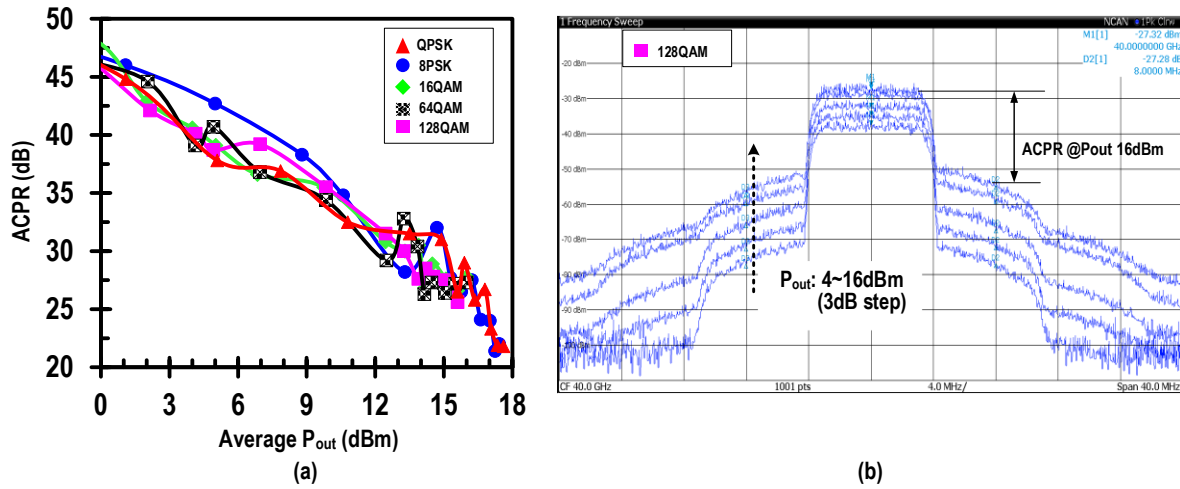


Fig. 5-7: Out-of-band linearity measurement results of the modulated input signal (a) ACPR (@8MHz offset) versus average output power, (b) Typical example of spectral regrowth for 128QAM modulated signal at 40GHz at different output power levels.

the average modulated signal power efficiency ( $PE_{ave}$ ) surpasses 40% at the cost of 10.1% EVM (Fig.5-6(2)). For the constant amplitude modulations (QPSK/8PSK) the peak  $PE_{ave}$  is 42-43% in Fig.5-6(3), well matched with the monotone case in Fig.5-6(3). The 5% EVM crossover happens when the peak power reaches to the  $OP_{-1\text{dB}}$  in each modulation scheme in Fig.5-6(4): the maximum  $P_{out,ave}$  for  $\leq 5\%$  EVM is  $\sim 15.5\text{dBm}$  for QPSK/8PSK; 13-13.5dBm for 16QAM (PAPR: 2.6dB) and 128QAM (PAPR: 3.2dB); and 12.5-13dBm for 64QAM. When the  $P_{out,ave}$  is capped for  $\leq 5\%$  EVM, the maximum  $PE_{ave}$  is 40-41% for QPSK/8PSK and 32-35% for 16/64/128QAM signals, and ACPR measured at  $\pm 8\text{MHz}$  offset is better than 25dB for all the modulations as shown in Fig. 5-7. In comparison, while recent Class- $F^{-1}$  PAs exhibit consistent efficiency improvement over other techniques, the PAE enhancement by the  $\lambda/4$ -line based harmonic filter is outstanding at Q-band, on a par with state-of-the-art III-V.

#### 5.2.4 3-stage W-band Class- $F^{-1}$ PA

To verify the effectiveness of the proposed simplified load network a 3-stage PA is also implemented at 94 GHz. Fig.5-8 (a) shows the schematic of the PA. Due to low power gain of the output stage, to achieve high PAE, the PA uses Class  $F^{-1}$  for output stage and first driving stage. The efficiency requirements of the second Class AB driving stage relaxes due to power gain of

proceeding stages. The saturation output power of the 3-stage is 12dBm with 9dB power gain, optimized for wavefer-sacle phased array transceivers []. The  $Q_{2,3}$  ( $A_e=16 \times 0.12 \mu\text{m}^2$ ) and  $Q_1$  ( $A_e=8 \times 0.12 \mu\text{m}^2$ ) are biased at a Class-AB point and sized for an optimal *rms*-current density of  $11.7 \text{mA}/\mu\text{m}^2$  for  $f_T \geq 180 \text{GHz}$  at the fundamental frequency ( $f_0$ ) of 90-100GHz when the output power reaches  $OP_{-1\text{dB}}=10\text{dBm}$ . The intersatge matching is designed and optimized to achieve peak PAE. The  $\lambda/4$  ( $l \sim 0.39 \text{mm}$  @94GHz)-transformer with the characteristic impedance ( $Z_0$ ) of  $72\Omega$  (Width= $7\mu\text{m}$ ), is integrated by meandering the line pattern. The  $L_{S1}$  (30pH) and  $L_{S2}$  (42pH) are also adopted to new device size and operating frequency.

Fig. 5-8 (b) shows the die photo of the PA implemented in  $0.13 \mu\text{m}$  SiGe BiCMOS technology. The PA occupies  $1.32 \times 0.56 \text{mm}^2$  including pads. The small-signal performance of the PA is The small-signal performance of the PA is measured through on-wafer testing after standard SOLT calibration with biasing  $Q_{1,2}$  in Class-AB regions ( $V_{CC1}/V_{CC2}/V_{CC3}=1.5/1.7/2\text{V}$ ,

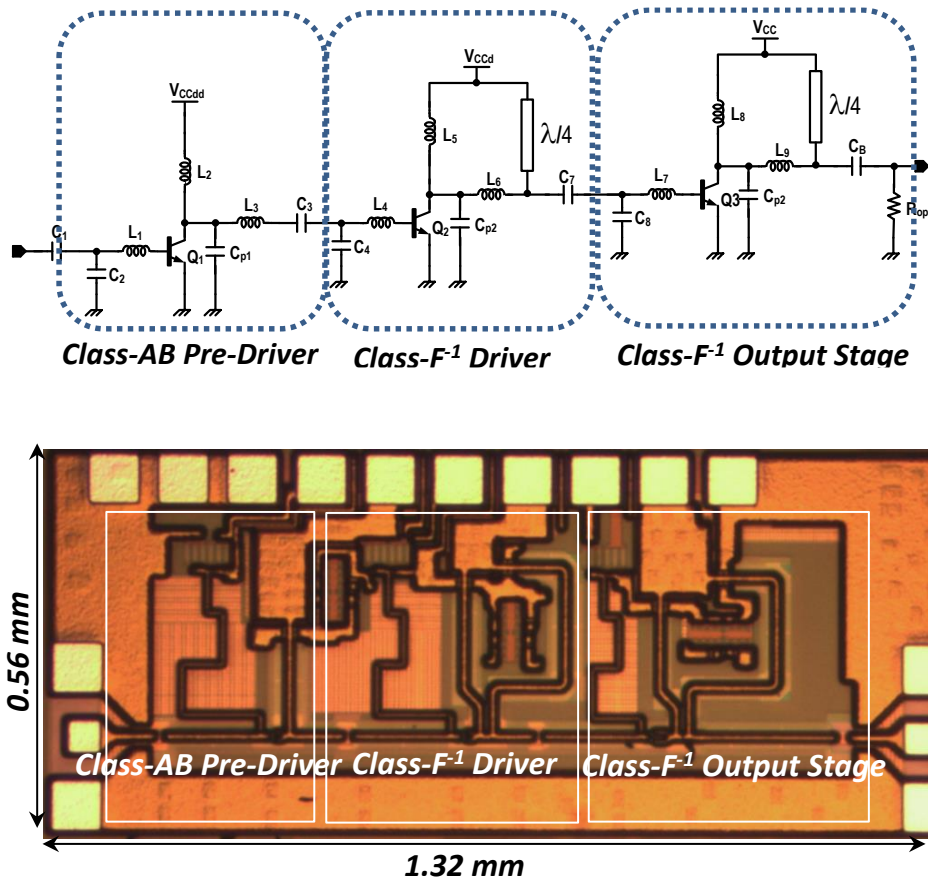


Fig. 5-8: Schematic and chip phot of 3-stage 94GHz PA

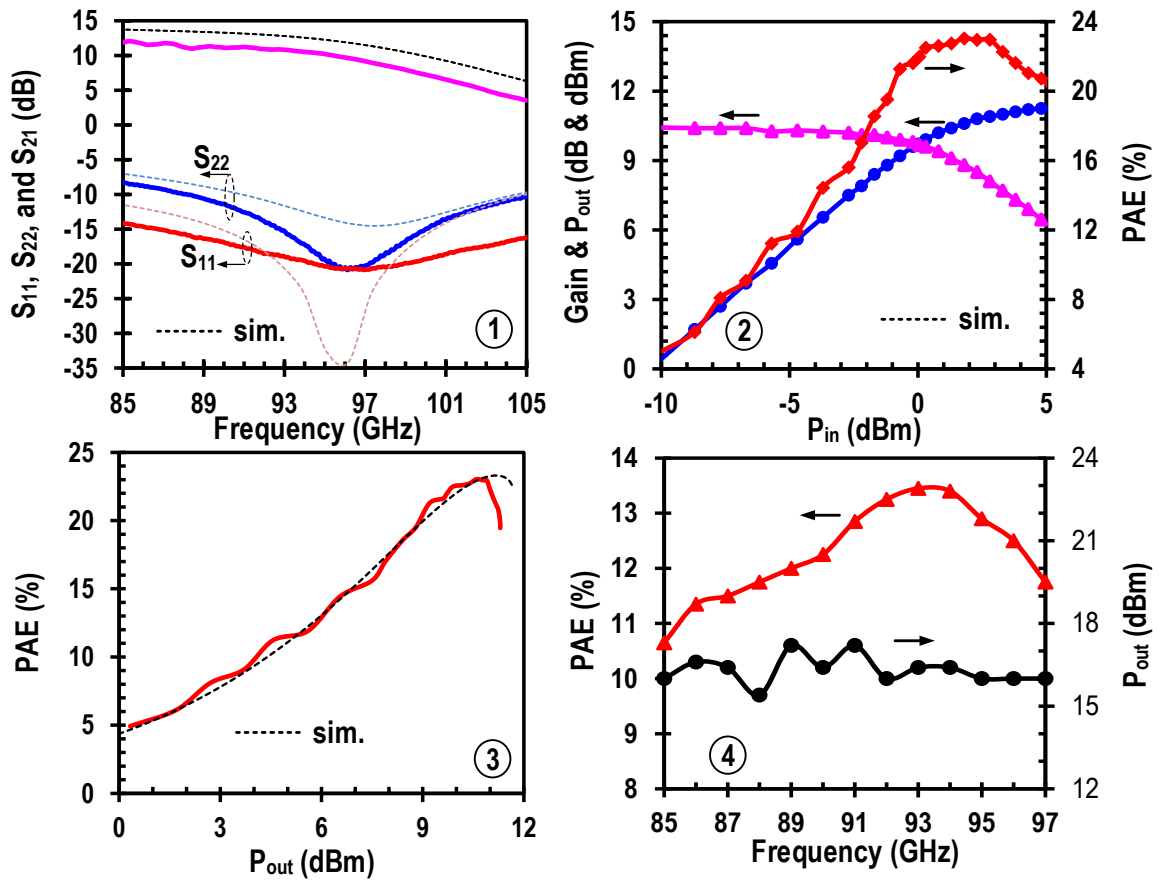


Fig. 5-9: Simulated (dot lines) and measured (*single-tone*) PA performances: ① gain, input and output matching, ② gain, P<sub>out</sub>, and corresponding PAE versus P<sub>in</sub> at 94GHz, ③ peak PAE versus P<sub>out</sub> at 94GHz, and ④ peak PAE and corresponding P<sub>out</sub> versus frequency

I<sub>CE1</sub>/I<sub>CE2</sub>/I<sub>CE3</sub>=3/4/6 mA) and the results are: S<sub>11</sub><-10dB @89-105GHz, S<sub>22</sub><-10dB @85-105GHz and S<sub>21</sub>=8-12dB @85-98GHz (Fig.5-9①). At 94GHz the peak PAE reaches 23% with corresponding 10dBm P<sub>out</sub>, and measured OP<sub>-1dB</sub> and P<sub>sat</sub> are 10.5dBm and 11.5dBm, respectively (Fig.5-9②). When 3dB and 6dB back-off, the PAE is 15% and 8%, respectively (Fig.5-9③). The measured PAE is >20% @90-96.5GHz with 10dBm P<sub>out</sub> (Fig.5-9④).

### 5.3 Summary

In this chapter a simplified load networks for harmonic tuning Class F<sup>-1</sup> PA presented for >30 GHz wave bands. As frequency increases in mm-wave bands, due to loss of passive components the power efficiency of the LC-based 6<sup>th</sup> order harmonic load degrades. To extend the Class F<sup>-1</sup> PA to high mm-wave frequencies, a simplified λ/4-transformer based harmonic tuning load

presented in this chapter. The load provides high-impedance at 2<sup>nd</sup> harmonic while for providing low impedance at 3<sup>rd</sup> harmonic relies on parasitic capacitors at collector node. Q-band 38~42 GHz and W-band 88-108 GHz Class F<sup>-1</sup> PA implemented to verify effectiveness of this load which achieve the peak PAE 43% and 23% at respectively. Fig. 5-10 shows the PAE performance of the PAs.

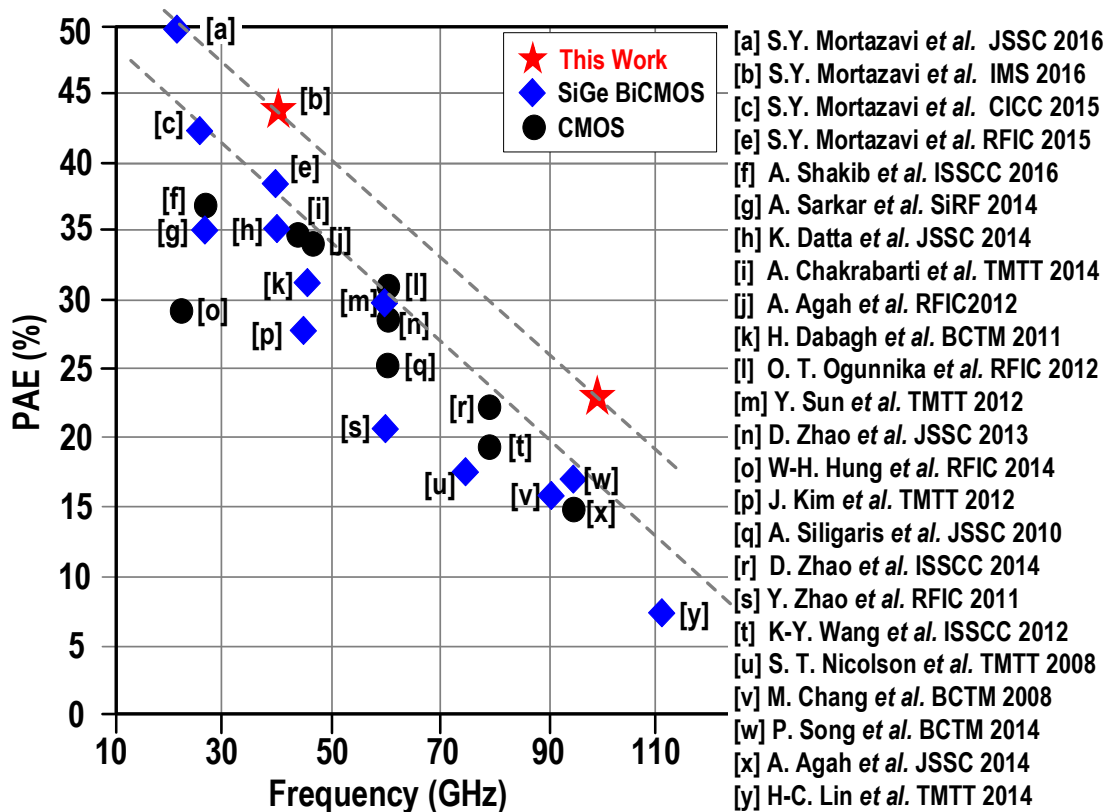


Fig. 5-10. PAE performance of the mm-wave silicon PAs



# 6 Wide Efficiency Bandwidth PA With in-band Class F<sup>-1</sup>/F Mode Transition

## 6.1 Introduction

This work presents a high-efficient class-F<sup>-1</sup>/F PA in 0.13μm SiGe BiCMOS achieving 39.3-40.7% PAE over 25-30 GHz, 40.7% of peak PAE at 27GHz corresponding to 52.7% of collector efficiency. In the PA, integrated on-chip passive load networks operates cooperatively to shape the load impedance for an in-band mode transition from class-F<sup>-1</sup> to class-F so as to maintain greater than 36.3% over the entire operation band (24-31GHz, 25.5% of fractional bandwidth).

## 6.2 Continuous mode Class-F<sup>-1</sup> and Class-F PAs

### 6.2.1 Class-F<sup>-1</sup> and Class F PAs

Controlling up to 3<sup>rd</sup> harmonic component in Class-F<sup>-1</sup> and Class-F PAs the current waveform of amplifier is expressed as [8]:

$$i_{F^{-1}}(\theta) = i_{1mF^{-1}} \cdot (i_{oF^{-1}} - \text{Cos}\theta + i_{3F^{-1}}\text{Cos}3\theta), \quad (6 - 1a)$$

and,

$$i_F(\theta) = i_{1mF} \cdot (i_{oF} - \text{Cos}\theta + i_{2F}\text{Cos}2\theta). \quad (6 - 1b)$$

where  $i_{oF^{-1}}$  and  $i_{oF}$  are DC current component normalized to fundamental current component, and  $i_{3F^{-1}}$  and  $i_{2F}$  are 3<sup>rd</sup> and 2<sup>nd</sup> harmonic current components normalized to fundamental current component for Class-F<sup>-1</sup> and Class-F, respectively. The harmonic components are determined by the conduction angle of the transistor and the harmonic load network. By changing the DC bias from Class-A bias point to Class-B bias point the conduction angle reduces from  $2\pi$  to  $\pi$  and harmonic components become stronger. In Class-F<sup>-1</sup> and Class-F PAs, the harmonic contents of the voltage waveform are tuned to make half-sinusoidal waveform and rectangular, respectively. For peak efficiency, the voltage waveforms normalized to dc are expressed as [8]:

$$v_{F^{-1}}(\theta) = v_{1mF^{-1}} \cdot \left( \frac{1}{\sqrt{2}} - \cos\theta + \frac{1}{2\sqrt{2}} \cos 2\theta \right), \quad (6 - 2a)$$

and,

$$v_F(\theta) = v_{1mF} \cdot \left( \frac{\sqrt{3}}{2} - \cos\theta + \frac{1}{6} \cos 3\theta \right). \quad (6 - 2b)$$

which result in ~90% power efficiency for class B bias point.

### 6.2.2 Continuous mode Class-F<sup>-1</sup> and Class-F PAs

Continuous-Class-F<sup>-1</sup> (CCF<sup>-1</sup>) and Continuous-Class-F (CCF) PAs extend the design space of Class-F<sup>-1</sup> and Class-F PAs by eliminating the need for open circuit and short circuit conditions at second harmonic load compared with Class-F<sup>-1</sup> and Class-F PAs [14], [38]-[40]. To eliminate open-circuit or short-circuit load condition at 2<sup>nd</sup> harmonic, both current and voltage waveforms should have non-zero 2<sup>nd</sup> harmonic components. Therefore, rectangular waveform of a core Class-F<sup>-1</sup> or Class-F PA is multiplied to a modulation function to make non-zero 2<sup>nd</sup> harmonic component in CCF<sup>-1</sup> or CCF PA. The modulated rectangular waveform in continuous mode operation is expressed as:

$$i_{CCF^{-1}}(\theta) = i_{F^{-1}}(\theta) \cdot f_{mod}(\theta). \quad (6 - 3a)$$

and:

$$v_{CCF}(\theta) = v_F(\theta) \cdot f_{mod}(\theta). \quad (6 - 3b)$$

where  $i_{F^{-1}}(\theta)$  is the current waveform of the core Class-F<sup>-1</sup> PA expressed in (6-1a), and  $v_F(\theta)$  is voltage waveform of the core Class-F PA expressed in (6-2b). The modulation function is defined as [4]:

$$f_{mod}(\theta) = (1 - \gamma \sin\theta) \cdot (1 - \alpha \cos\theta). \quad (6 - 4)$$

where both  $\gamma$  and  $\alpha$  are in the range of (-1, 1) since (6-3a) and (6-3b) should be non-zero to avoid efficiency degradation and nonlinearity. The first term in (4) is orthogonal to both current and voltage waveforms of the Class-F<sup>-1</sup> and Class-F PAs. Therefore, modulating the rectangular waveform with this term does not result in DC power consumption, thus maintains the efficiency

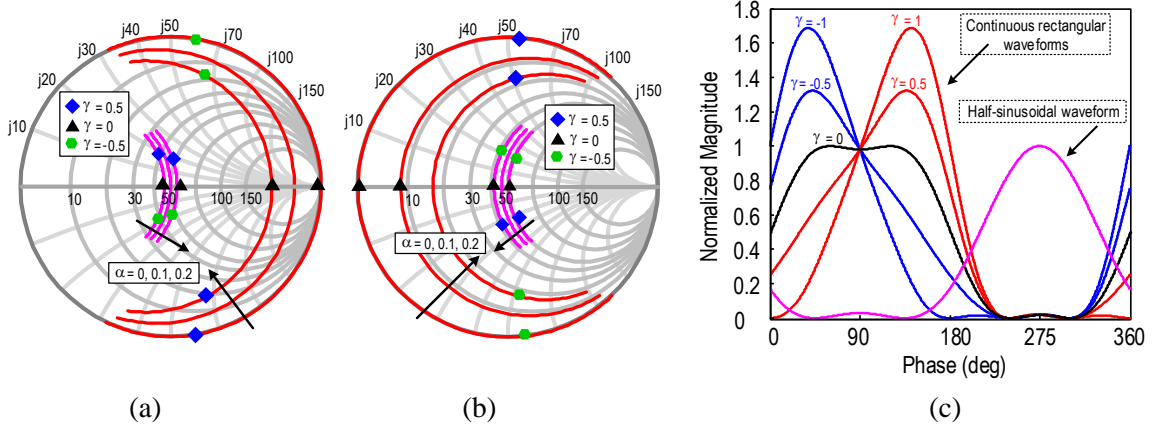


Fig. 6-1. Fundamental and 2<sup>nd</sup> harmonic load network for CF<sup>-1</sup> and CF operation mode for  $\theta_0 = 180$  (class B bias point),  $-1 < \gamma < 1$ , for  $\alpha = 0$  and  $\alpha = 0.2$

performance of the base Class-F<sup>-1</sup>/Class-F PA in continuous operating modes of CCF<sup>-1</sup>/CCF. This term adds imaginary part to the fundamental and 2<sup>nd</sup> harmonic load depending on  $\gamma$ . However, by changing  $\gamma$  the 2<sup>nd</sup> harmonic load is pure imaginary and only moves on the edge of the Smith-Chart[] as shown in the Fig. 6-1 (a) and Fig. 6-1 (b) with  $\alpha = 0$ . To include the effect of the loss of the passive components in the load network and expand the design space in the Smith chart, the second term in (4) is included in modulation function [38]. This term adds real part to 2<sup>nd</sup> harmonic load and brings it inside the Smith-chart (shown in the Fig. 6-1 (a) and Fig. 6-1 (b) with  $\alpha \neq 0$ ) at the cost of efficiency degradation.

Using (2) and (3) the fundamental and 2<sup>nd</sup> harmonic admittance of the load network for the CCF<sup>-1</sup> are expressed as:

$$Y_{1CCF^{-1}} = \frac{(1 - \alpha i_{oF^{-1}})}{R_{OPT-F^{-1}}} + j\gamma_{CCF^{-1}} \frac{(-i_{oF^{-1}} + \frac{\alpha}{4} + \frac{\alpha}{4} i_{3F^{-1}})}{R_{OPT-F^{-1}}}, \quad (6-5a)$$

and:

$$Y_{2CCF^{-1}} = \frac{\alpha\sqrt{2}(1 - i_{3F^{-1}})}{R_{OPT-F^{-1}}} + j\gamma_{CCF^{-1}} \frac{\sqrt{2}(-\alpha i_{oF^{-1}} + 1 + i_{3F^{-1}})}{R_{OPT-F^{-1}}}. \quad (6-5b)$$

where  $R_{OPT-F^{-1}}$  ( $= v_{1mF^{-1}}/i_{1mF^{-1}}$ ) is the optimum load for the core Class-F<sup>-1</sup> PA. For CCF PA, the harmonic admittances are:

$$Z_{1CCF} = \left[ \left( 1 - \frac{\sqrt{3}}{2} \alpha \right) - j\gamma_{CCF} \left( \frac{\sqrt{3}}{2} - \frac{7\alpha}{24} \right) \right] \cdot R_{OPT-F}, \quad (6-6a)$$



and:

$$Z_{2CCF} = \left[ \frac{5\alpha}{12i_{2F}} - jY_{CCF} \frac{(\alpha - \frac{7}{6})}{2i_{2F}} \right] \cdot R_{OPT-F} \quad (6-6b)$$

$R_{OPT-F}$  ( $= v_{1mF}/i_{1mF}$ ) is the optimum load for the core Class-F PA. Fig. 6-1 (a) and Fig. 6-1 (b) shows the design space for  $CCF^{-1}$  and CCF for  $-1 \leq \gamma \leq 1$  when  $\alpha = 0, 0.1, \text{ and } 0.2$ . As  $\alpha$  increases 2nd harmonic load moves from the edge to the inside of Smith chart. For a constant  $\alpha$ , only imaginary part of both the fundamental and 2nd harmonic loads change proportional to  $\gamma$ . Therefore, for a constant  $\alpha$ , as  $\gamma$  changes the design space is mapped to a line in a surface defined by imaginary part of fundamental and 2nd harmonic loads. The slope of the line is determined by  $\alpha$  and the harmonic components. For the  $CCF^{-1}$  PA the slope of the line is expressed based on (6-5) as:

$$B21R_{CCF^{-1}} = \frac{\sqrt{2}(-\alpha i_{oF^{-1}} + 1 + i_{3F^{-1}})}{-i_{oF^{-1}} + \frac{\alpha}{4}(1 + i_{3F^{-1}})} \Bigg|_{\alpha=0} = -\frac{\sqrt{2}(1 + i_{3F^{-1}})}{i_{oF^{-1}}}. \quad (6-7)$$

and for CCF PA based on (6-7) as:

$$X21R_{CCF} = \frac{\frac{7}{6} - \alpha}{(\sqrt{3} - \frac{7\alpha}{12})i_{2F}} \Bigg|_{\alpha=0} = -\frac{7}{6\sqrt{3}i_{2F}}. \quad (6-8)$$

$B21R_{CCF^{-1}}$  and  $X21R_{CCF}$  are function of  $\alpha$  and conduction angle. Fig. 6-2 shows the design space for  $0 < \alpha < 0.2$  at Class-B biasing point. Each line corresponds to a specific  $\alpha$  and thus power efficiency. The line corresponding to  $\alpha = 0$  has the peak power efficiency 91% for  $CCF^{-1}$  and 89% for CCF mode operations, same as the base Class-F<sup>-1</sup> and Class-F PAs. As  $\alpha$  increases the slope of the line changes and efficiency decreases, shown in Fig.2. The Efficiency is calculated in terms of  $\alpha$  using (1) and (4) as:

$$PE_{CCF^{-1}} = \frac{1}{2} \cdot \frac{\sqrt{2}(1 - \alpha i_{oF^{-1}})}{i_{oF^{-1}} - \frac{\alpha}{2}}. \quad (6-9)$$

and:

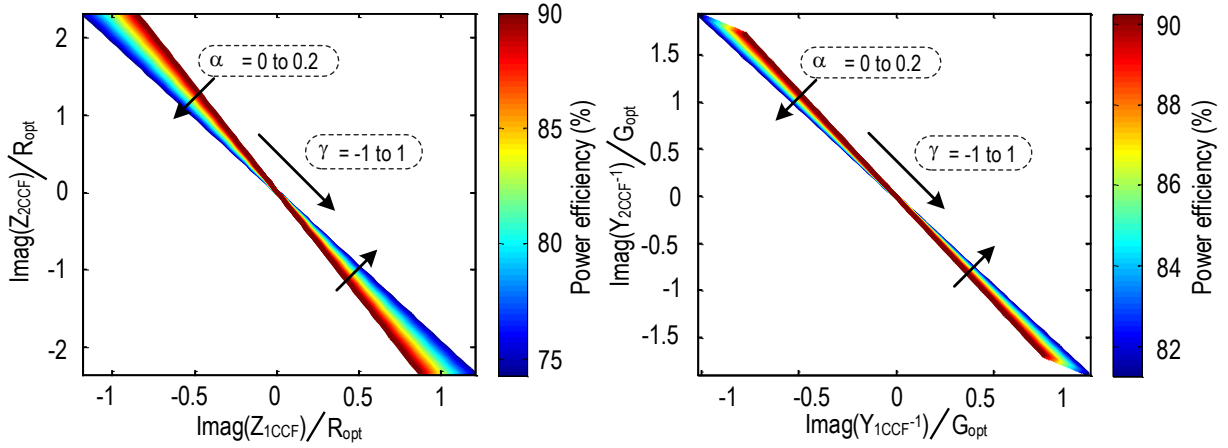


Fig. 6-2. Design space and Power efficiency for design space for continuous Class F and continuous Class F<sup>-1</sup>  $-1 < \gamma < 1$ , and  $0 < \alpha < 0.2$

$$PE_{CCF} = \frac{1}{2} \cdot \frac{1}{i_{oF}} \cdot \frac{\frac{2}{\sqrt{3}} - \alpha}{1 - \frac{\alpha}{2} \cdot \frac{2}{\sqrt{3}}} \quad (6-10)$$

where  $i_{oF^{-1}}$  and  $i_{oF}$  are respectively the normalized DC current components of the base Class-F<sup>-1</sup> and Class-F PAs of CCF<sup>-1</sup> and CCF PAs. As Fig. 6-2 shows, to reduce power efficiency degradation and get advantages of harmonic tuning for efficiency,  $\alpha$  should be in the range of  $0 \leq \alpha \leq 0.2$ .

### 6.2.3 In band transition from CCF<sup>-1</sup> to CCF for efficiency bandwidth

The impedance alternation in the load network for CCF<sup>-1</sup> to CCF operation mode transition is conceptually shown in Fig. 6-3. At low signal band,  $\omega_{oL}$ , PA operates in CCF<sup>-1</sup> mode and the peak power efficiency is same as base Class-F<sup>-1</sup> PA. As frequency increases, with transition in fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonic loads, at high signal band,  $\omega_{oH}$ , the PA operates in CCF mode. As Fig. 6-3 shows, assuming  $\alpha = 0$ , when the operation frequency increases over  $\omega_{oL}$ -band, the fundamental load impedance moves over constant conductance circle of  $\frac{1}{R_{OPT-F^{-1}}}$  and accordingly the load at 2nd harmonic band changes in respect to (6-5). The optimum load for CCF-1 operation with  $\alpha=0$  for  $-1 \leq \gamma_{CCF^{-1}} \leq 1$  is:

$$R_{OPT-CCF^{-1}} = \frac{1}{\text{real}(Y_{1CCF^{-1}})} = \frac{1}{Y_{1CCF^{-1}} \Big|_{\gamma_{CCF^{-1}}=0}} = R_{OPT-F^{-1}}.$$

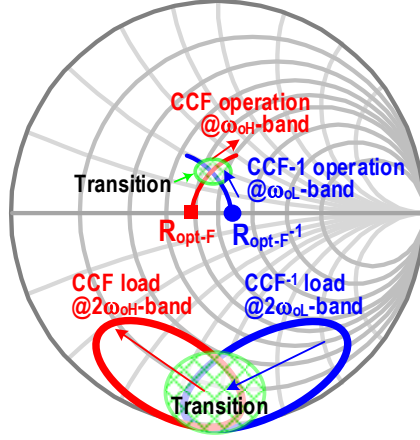


Fig. 6-3 Fundamental and 2<sup>nd</sup> harmonic load network for CCF<sup>-1</sup> and CCF operation mode for  $\theta_0 = 180$  (class B bias point),  $-1 < \gamma < 1$ , for  $\alpha = 0$  and  $\alpha = 0.2$

In the CCF operation mode in  $\omega_{oH}$ -band, when the operation frequency increases, the fundamental load impedance moves over constant resistance circle of  $R_{OPT-F}$  while the load at 2<sup>nd</sup> harmonic band changes with respect to (6-7). The optimum load for CCF is the resistance of the fundamental frequency load expressed as:

$$R_{OPT-CCF} = \text{real}(Z_{1CCF}) = Z_{1CCF}|_{\gamma_{CCF}=0} = R_{OPT-F}.$$

At transition bands, to provide optimum load at fundamental frequency for both CCF<sup>-1</sup> and CCF modes and maintain high efficiency performance the  $\gamma_{CCF^{-1}}$  should be set to have  $R_{CCF^{-1}}=R_{OPT-CCF}$  where  $R_{CCF^{-1}}$  is expressed as:

$$R_{OPT-F} = \frac{R_{OPT-F^{-1}}}{1 + (\gamma_{CCF^{-1}} \cdot i_{OF^{-1}})^2}.$$

Moreover, the load at 2<sup>nd</sup> harmonic should meet requirements for both design spaces  $B21R_{CCF^{-1}}$  and  $X21R_{CCF}$  which limits the conduction angle. At the transition region, the operation mode is either CCF<sup>-1</sup> or CCF depending on the 3<sup>rd</sup> harmonic load network and thus current and voltage harmonic components.

### 6.3 multi-resonance LC load for in-band CCF<sup>-1</sup>/CCF transition

Fig. 6-4 (a) shows the proposed load network for a PA with mode transition from CCF<sup>-1</sup> to CCF. The multi-resonance LC load network provides optimum inductive load at  $\omega_o$ -band with

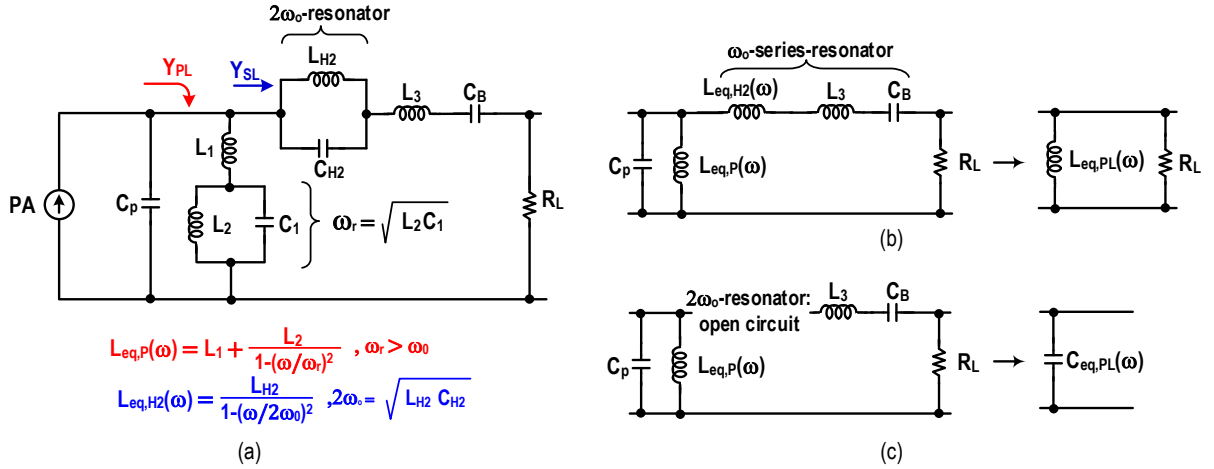


Fig. 6-4 (a) Proposed load network for  $CF^{-1}/CF$  mode transition, (b) equivalent inductive load at  $\omega_0$ -band, (c) equivalent capacitive load at  $2\omega_0$ -band

corresponding capacitive impedance at  $2\omega_0$ -band, and low impedance to high impedance transition at  $3\omega_0$ -band. The  $L_1$ ,  $L_2$ ,  $C_1$  and  $C_P$  form a multi-resonance parallel load ( $Y_{PL}$ ), and  $L_{H2}$ ,  $C_{H2}$ ,  $L_3$ ,  $C_B$ , and load resistance  $R_L$  comprise a series load ( $Y_{SL}$ ). The  $C_P$  is the collector node total capacitance which includes the layout parasitics.

Fig. 6-4 (b) and Fig. 6-4 (c) show the equivalent load network at  $\omega_0$ -band and  $2\omega_0$ -band. The  $Y_{PL}$  is an LC-tank composed of  $C_P$  and  $L_{eq,P}(\omega)$ . The  $L_{eq,P}(\omega)$  is equivalent inductance of  $L_1$  and  $L_2$ - $C_1$  tank expressed as:

$$L_{eq,P}(\omega) = L_1 + \frac{L_2}{1 - \left(\frac{\omega}{\omega_r}\right)^2}, \quad \text{where } \omega_r = \frac{1}{\sqrt{L_2 C_1}}. \quad (6 - 12)$$

The resonance frequency of  $L_{eq,P}(\omega)$ - $C_P$  is set to around midpoint between the  $\omega_0$ -band and the  $2\omega_0$ -band.  $Y_{PL}$  provides inductive load for the  $\omega_0$ -band and capacitive load for the  $2\omega_0$ -band, Fig. 6-4 (b) and Fig. 6-4 (c). At  $\omega_0$ ,  $C_B$ ,  $L_3$ , and the effective  $L_{H2}$ - $C_{H2}$  tank inductance make series resonance and  $Y_{SL}$  is conductive and near  $1/R_L$ . Therefore load admittance seen by active device at  $\omega_0$  can be expressed as:

$$Y_1 = \frac{1}{R_L} + j \frac{1 - \omega_0^2 L_{eq,P}(\omega_0) C_P}{\omega_0 L_{eq,P}(\omega_0)}. \quad (6 - 13)$$

At  $2\omega_0$ -band the series path is open circuit due to resonance of the parallel  $L_{H2}$ - $C_{H2}$  tank, Fig. 6-4 (c), and the load admittance is expressed as:

$$Y_2 = j \frac{1 - 4\omega_0^2 L_{eq,P}(2\omega_0) C_P}{2\omega_0 L_{eq,P}(2\omega_0)}. \quad (6 - 14)$$

with  $R_L = R_{OPT-F^{-1}}$ , for CCF<sup>-1</sup> operation, the load admittance at  $\omega_0$  and  $2\omega_0$  frequencies should lay on the design space defined by (6-7a) which is expressed as:

$$B21R_{CCF^{-1}} = \frac{\frac{1 - 4\omega_0^2 L_{eq,P}(2\omega_0) C_P}{2\omega_0 L_{eq,P}(2\omega_0)}}{\frac{1 - \omega_0^2 L_{eq,P}(\omega_0) C_P}{\omega_0 L_{eq,P}(\omega_0)}} = -\frac{\sqrt{2}(1 + i_{3F^{-1}})}{i_{oF^{-1}}}. \quad (6 - 15)$$

at the end of the  $\omega_0$ -band, called  $\omega_{oH}$ , to change the operation mode to the CCF, the load at  $\omega_{oH}$  and  $2\omega_{oH}$  should meet (8a). This condition can be expressed based on (6-13) and (6-14) as:

$$X21R_{CCF} = -\frac{\left(\frac{1}{R_L}\right)^2 + \left(\frac{1 - \omega_{oH}^2 L_{eq,P}(\omega_{oH}) C_P}{\omega_{oH} L_{eq,P}(\omega_{oH})}\right)^2}{\left(\frac{1 - \omega_{oH}^2 L_{eq,P}(\omega_{oH}) C_P}{\omega_{oH} L_{eq,P}(\omega_{oH})}\right) \cdot \left(\frac{1 - 4\omega_{oH}^2 L_{eq,P}(2\omega_{oH}) C_P}{2\omega_{oH} L_{eq,P}(2\omega_{oH})}\right)} = -\frac{7}{6\sqrt{3}i_{2F}}. \quad (6 - 16)$$

Over 3<sup>rd</sup> harmonic frequencies, the impedance change of the  $L_2$ - $C_1$  tank plays a key role in modulating the load impedance and hence mode transition from CCF<sup>-1</sup> to CCF. At the center of the 3rd-harmonic band, the dominant impedance of the  $L_2$ - $C_1$  tank is capacitive which resonates with  $L_1$  making an impedance null at  $3\omega_0$ -band. If frequency increased further after passing the series resonance, the  $Z_{PL}$  becomes inductive, and makes a parallel resonance with  $C_P$  creating an impedance peak at the edge of the 3rd-harmonic band,  $3\omega_{oH}$ . This can be expressed as:

$$L_{eq,P}(3\omega_0) = 0. \quad (6 - 17)$$

and:

$$L_{eq,P}(3\omega_{oH}) C_P \cdot 9\omega_{oH}^2 = 1. \quad (6 - 18)$$

By meeting these conditions, the load network provides low-to-high impedance transition at  $3\omega_0$ -band, required for mode transition from CCF<sup>-1</sup> to CCF. Replacing (6-12) in (6-17) and (6-18)  $L_{eq,P}(\omega)$  is expressed as:

$$L_{eq,P}(\omega) = \frac{1}{C_P \cdot 9\omega_{oH}^2} \cdot \frac{\left(1 - \frac{1 - \left(\frac{3\omega_o}{\omega_r}\right)^2}{1 - \left(\frac{\omega}{\omega_r}\right)^2}\right)}{\left(1 - \frac{1 - \left(\frac{3\omega_o}{\omega_r}\right)^2}{1 - \left(\frac{3\omega_{oH}}{\omega_r}\right)^2}\right)}. \quad (6-19)$$

For a desired  $\omega_o$ -band, (6-15)-(6-18) should be used to set  $\omega_{oH}$  and  $\omega_r$  so that the load network meets the CFF<sup>-1</sup> and CFF operation modes over  $\omega_o$ -,  $2\omega_o$ -, and  $3\omega_o$ -bands. For the specific  $\omega_o$ ,  $\omega_{oH}$  and  $\omega_r$ , the values of parallel path passive components  $\{L_1, L_2, C_1\}$  determine from (6-17) and (6-18).

## 6.4 CCF<sup>-1</sup>/CCF mode transition power amplifier Design

Fig. 6-5 shows the schematic of the PA with proposed load at 27-30 GHz band. The operation mode is CFF<sup>-1</sup> for 27-29 GHz and changes to CFF mode at the end of the band. The bias path provides less than 300Ω seen from the base of Q1, which increases effective collector-emitter breakdown voltage over 5V (BVCEO=1.8V, BVCBO=5.9V), allowing 2.2V supply voltage (V<sub>CC</sub>) with a safe margin. The C<sub>M</sub> (178fF), L<sub>M</sub> (170pH) and C<sub>PI</sub> (660fF) constitute π-matching network and provides S11 better than -10 dB over 23-31GHz. The CM absorbs about 18fF of input pad

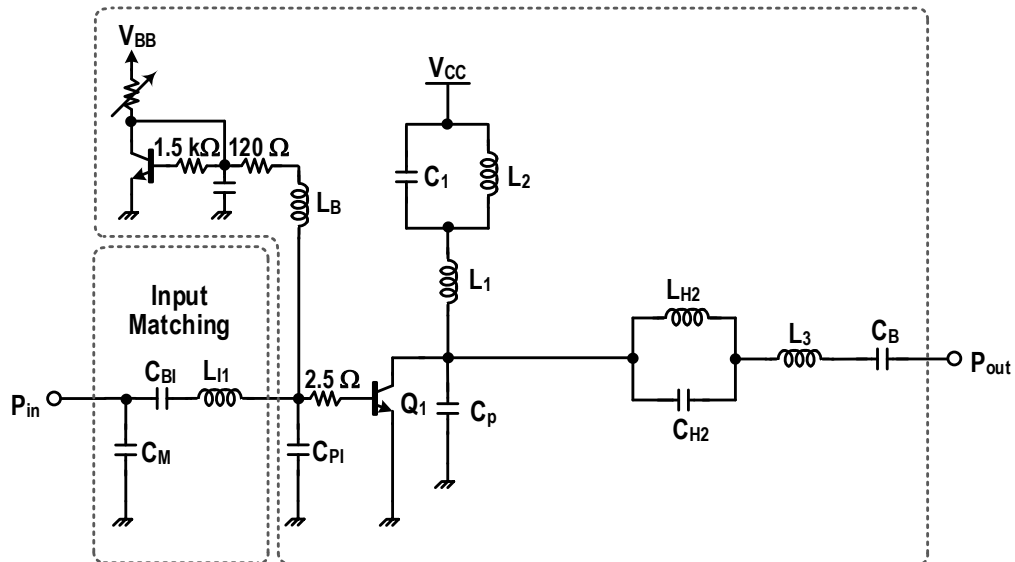


Fig. 6-5 Schematic of the wide efficiency bandwidth power amplifier with in band Continuous-Class-F<sup>-1</sup>/Continuous-Class-F mode transition

capacitance and  $C_{PI}$  includes  $C_{\pi}$  and miller capacitance of  $C_{bc}$  of Q1. Interconnects are characterized with the Sonnet EM-field solver and absorbed in the passive networks. A small resistor of  $2.5\Omega$  is in series with Q1 to guarantee stability on all frequencies. The Q1 (emitter area= $27.6 \times 0.12 \mu\text{m}^2$ ) is sized for peak- $fT$  current density ( $11.5 \text{mA}/\mu\text{m}^2$ ) with respect to the rms current at target  $P_{\text{sat}}$  (50mW).

### 6.4.1 Load network design

Design of the load network starts with extracting the harmonic contents of the collector current when operating in Class- $F^{-1}$  and Class-F modes as a core for continuous operation mode. Based on (6-5) and (6-6), the harmonic components of the collector current determine the required harmonic load for CCF $^{-1}$  and CCF modes at  $\omega_0$ -band and  $2\omega_0$ -band. Multi harmonic loadpull simulations at output 1-dB gain compression power level performed to determine the current and voltage harmonic contents. Fig. 6-6 shows the collector waveform and harmonic contents of a Class- $F^{-1}$  PA at 27 GHz with 16 dBm output power and a Class-F PA at 30 GHz with 15 dBm output power both with  $R_{\text{OPT}}=50\text{-}\Omega$ . In Class-F PA, due to rectangular voltage waveform, the collector voltage level is high in the voltage-current overlapped region where the voltage level is

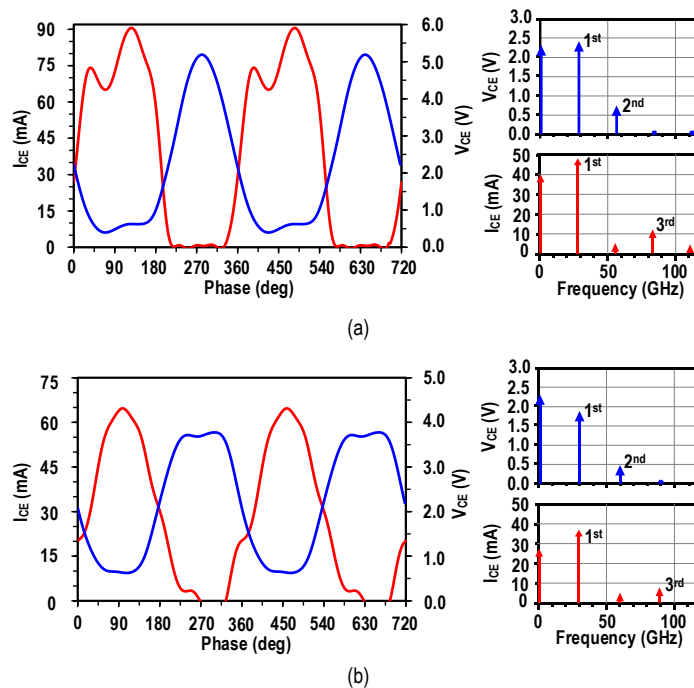


Fig. 6-6. Voltage and current time waveforms and harmonic contents of the core PA: (a) Class- $F^{-1}$  PA @ 27 GHz with  $P_{\text{out}}=16$  dBm, and (b) Class-F PA @ 30 GHz with  $P_{\text{out}}=15$  dBm

Table 6-1. Harmonic contents of core Class-F<sup>-1</sup> and Class-F PAs

PAs			
Class-F <sup>-1</sup>	dc	2 <sup>nd</sup>	3 <sup>rd</sup>
I <sub>CE</sub> Harmonics	0.83	-	0.25
V <sub>CE</sub> Harmonics	0.71	0.32	-
Class-F			
Class-F	dc	2 <sup>nd</sup>	3 <sup>rd</sup>
I <sub>CE</sub> Harmonics	0.81	0.2	-
V <sub>CE</sub> Harmonics	0.9	-	0.14

>2.5 V. Therefore, the voltage and current swing is highly limited by the breakdown voltage. The Table I summarizes the normalized harmonic components. Using Table 6-1, from (6-7a) and (6-8a),  $B21R_{CCF^{-1}} = -1.8$  at 27 GHz and  $X21R_{CCF} = -2.8$  at 30GHz when  $\alpha = 0$ . With  $R_L = R_{OPT,F^{-1}} = 50 \Omega$ ,  $\omega_0 = 2\pi \cdot 27$  Gprs, and  $2\omega_0 = 2\pi \cdot 54$  Gprs, solving (6-15)-(6-18) determines that the  $\omega_{0H} = 2\pi \cdot 30$  Gprs and  $\omega_f = 2\pi \cdot 58$  Gprs, which results in:  $\{L_1 = 192 \text{ pH}, L_2 = 183 \text{ pH}, C_1 = 41 \text{ fF}\}$ . At  $2\omega_0$ -band the  $L_{H2}$ - $C_{H2}$  tank is open circuit and the load is only determined by parallel path from (6-14). The value of components in the series path are optimized to provide the optimum load based on (6-5) and (6-6) for CCF<sup>-1</sup> and CCF operation all over  $\omega_0$ -band:  $\{L_{H2} = 135 \text{ pH}, L_3 = 118 \text{ pH}, C_{H2} = 50 \text{ fF}, C_B = 147 \text{ fF}\}$ .

#### 6.4.2 Simulation results

The load network is implemented with standard spiral inductors and MIM capacitors and used in the design after electromagnetic (EM) modeling. The interconnect inductances of parallel and series paths are absorbed in  $L_1$  and  $L_3$ . For inductors the quality factor is  $\sim 22$  over all bands, while the quality factor of MIM capacitors degrades from  $\sim 50$  at  $\omega_0$ -band to  $\sim 30$  at  $2\omega_0$ -band and  $\sim 12$  at  $3\omega_0$ -band. Due to low quality factor of the passive components, as shown in Fig. 6-7 (a) with solid blue line, the load at  $2\omega_0$ -band moves inside the Smith-Chart. The dashed lines in Fig. 6-7 (a) show the load impedance from (6-5) and (6-6) for CCF<sup>-1</sup> and CCF modes with  $\alpha \sim 0.13$  and Table 6-1. The proposed load network is well matched required impedances from (6-5) and (6-6). The PA operates in CCF<sup>-1</sup> mode at 26-28.5 GHz band with  $\gamma_{CCF^{-1}} \sim 0.4-0.6$ . Fig 6-7 (b) shows the load network on the design space described by (6-7), which is a line with slope of  $B21R_{CCF^{-1}} \sim -1.8$  with  $0.1 < \alpha < 0.15$ . The load network is within the theoretical design space for CCF<sup>-1</sup> mode operation. The operation of the PA changes to CCF mode at 29-30 GHz with  $\gamma_{CCF} \sim -0.45- -0.25$ . Fig 6-7 (c) shows the load network on the design space described by (6-8), a line with slope of



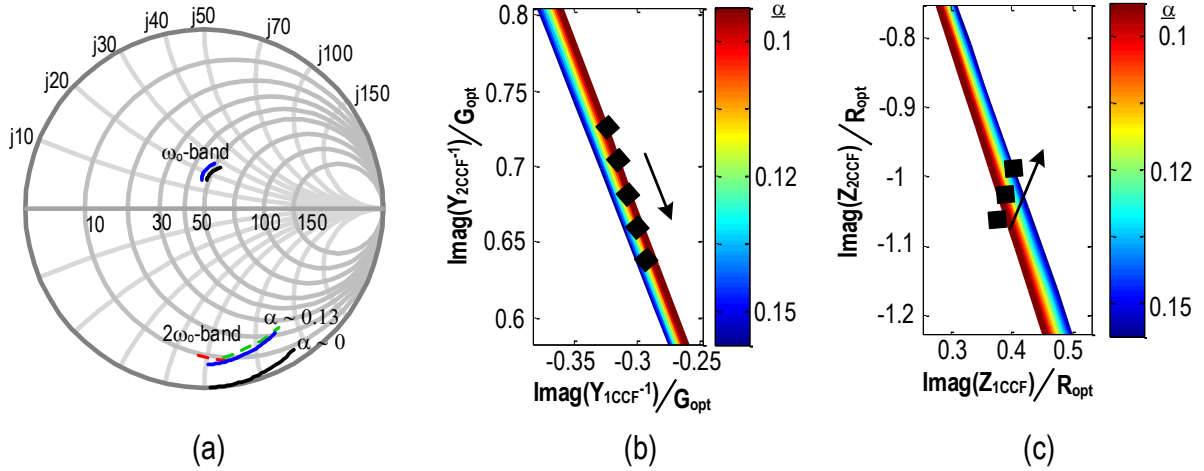


Fig. 6-7. Proposed load network with  $CCF^{-1}/CCF$  mode operation: (a) proposed load impedance at  $\omega_0$ -band and  $2\omega_0$ -band with lossless passives (solid black line)/EM modeled passives (Blue solid line), and ideal  $CCF^{-1}/CCF$  loads from (6-5) and (6-6) with  $\alpha \approx 0.13$  dashed lines, (b) proposed load network (black dots) in  $\omega_0$ -band = 26~28.5 GHz on the  $CCF^{-1}$  design space with  $B21R_{CCF^{-1}} \sim -1.8$  with  $0.1 < \alpha < 0.15$ , (c) proposed load network (black dots) in  $\omega_0$ -band = 29~30 GHz on the  $CCF^{-1}$  design space with  $X21R_{CCF} \sim -2.8$  with  $0.1 < \alpha < 0.15$ .

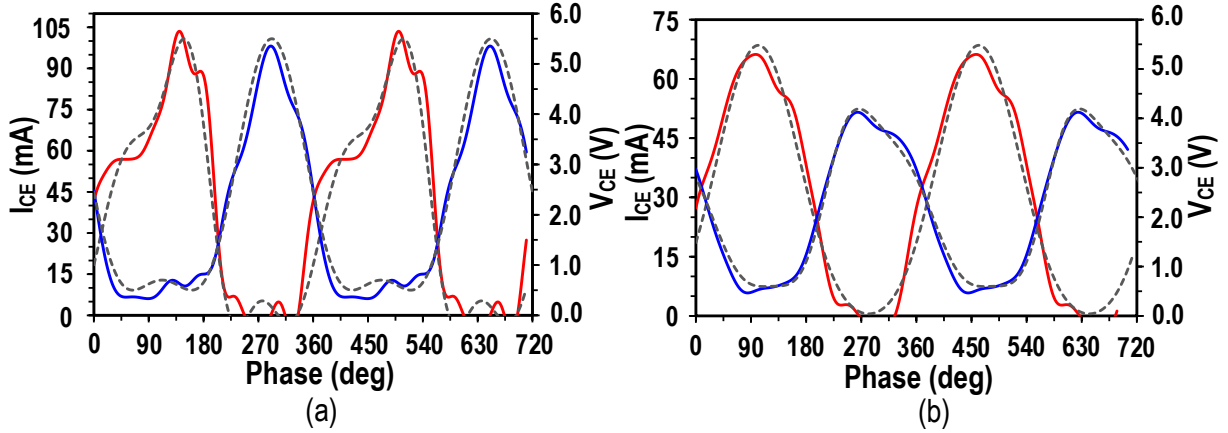


Fig. 6-8. Simulated (solid lines) and theoretical (dot lines) collector voltage and current waveforms for (a)  $CCF^{-1}$  mode @ 27 GHz with  $P_{out} = 16$  dBm, (b) CCF mode @ 30 GHz with  $P_{out} = 15$  dBm,.

$X21R_{CCF} \sim -2.8$  with  $0.1 < \alpha < 0.15$ . The load network is in well agreement with the theoretical design space for CCF mode operation. Fig. 6-8 (a) and Fig. 6-8 (b) show the simulated collector voltage and current waveforms at 27 GHz and 30 GHz with output power level of 16 dBm and 15 dBm, respectively. The solid lines show the simulated waveforms and the dashed lines are calculated based on (6-1)-(6-4), by using Table 6-1,  $\gamma_{CCF^{-1}} = 0.4$ ,  $\gamma_{CCF} = -0.25$ , and  $\alpha \approx 0.13$ . At 27 GHz in Fig. 6-8 (a), while the voltage waveform is half-sinusoidal, the current waveform is shaped with 2nd harmonic current and PA operates in  $CCF^{-1}$  mode. At 30 GHz, the current waveform is

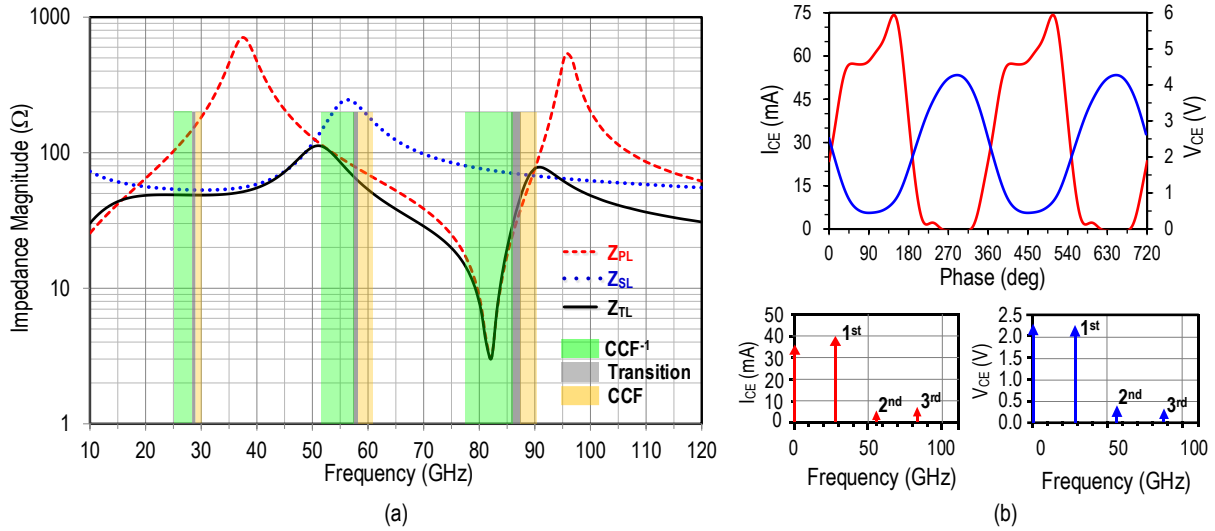


Fig. 6-9 Transition operation mode: (a) load impedance over transition frequencies (gray highlight), (b) collector current and voltage time waveforms and harmonic components at 28.5 GHz with  $P_{out}= 15.5$  dBm.

2nd harmonic-rich sinusoidal while in the voltage waveform is well matched CCF mode waveform.

At 27 GHz, the peak power efficiency based on theoretical waveforms is  $\sim 75\%$ , when  $\alpha \approx 0$ , considering knee voltage and breakdown voltage limitations [26]. The low-quality factor of passive components at  $2\omega_0$ -band,  $\alpha \approx 13$ , degrades the power efficiency to 70%. In addition, the low-quality factor of passives results in 0.9 dB loss at  $\omega_0$ -band which reduces the peak efficiency to  $\sim 65\%$ . At 30GHz, the breakdown voltage limits maximum swing and the peak efficiency based on theoretical waveforms is  $\sim 68\%$  when  $\alpha \approx 0$ . The peak efficiency reduces to 60% due to the loss at  $2\omega_0$ -band and total of  $\sim 50\%$  after the 1 dB loss at  $\omega_0$ -band.

There is a transition region from  $CCF^{-1}$  to CCF mode  $\sim 28.5$ -29 GHz, shown in Fig. 6-9. In this region the fundamental and 2<sup>nd</sup> harmonic loads are matched with both  $CCF^{-1}$  and CCF mode and the operations is determined with low or high impedance condition in 3<sup>rd</sup> harmonic load. Fig. 10 (b) shows the collector waveforms and harmonic components at  $P_{-1dB}= 15.5$  dBm. In this region the 3<sup>rd</sup> harmonic load impedance ( $|Z|=30\text{-}\Omega$  at 85.5 GHz) is still less than 2<sup>nd</sup> harmonic load impedance ( $|Z|=65\text{-}\Omega$  at 57 GHz). Therefore, collector current is 3<sup>rd</sup> harmonic rich with  $CCF^{-1}$  peaking. However, voltage waveform is still 2<sup>nd</sup> harmonic-rich half-sinusoidal. The 3<sup>rd</sup> harmonic component in voltage waveform misshapes the voltage level and increases the overlap between

voltage and current waveforms. This reduces the simulated peak PAE to 50% with lossless load and 43% with implemented load at 15.5 dBm output power.

### 6.4.3 Implementation and Measurement results

The PA die photograph is shown in Fig. 6-10. The PA is characterized with on-wafer testing using GSG probes for RF signal transitions after SOLT calibration. The small-signal S-parameter measurement with a class-AB biasing ( $V_{CC}=2.2V$ ,  $I_{CE}=9mA$ ) shows that  $S_{11}<-10dB$  @22.5-32GHz,  $S_{22}<-10dB$  @15-33GHz and  $S_{21}=9-10.8dB$  @24-31GHz, Fig. 6-11 (b). The measured k-factor is greater than 1 and the PA is stable over all measured frequencies. For large signal measurements, a signal generator followed by an amplifier provides high-power input signals to the PA, and the input and output power of the DUT are sampled using directional couplers and measured by a dual-channel power meter. Typical measured cable loss is 1.5-2 dB at 24-31GHz, which is de-embedded from the measured output power. Fig. 6-11 (a) shows measured PAEs, collector efficiencies, output powers and power gains. At 27GHz with the class-AB biasing, the PA achieves peak PAE of 40.7%, equivalent to 52.7% of collector efficiency, with corresponding output power of 16.5dBm,  $OP_{-1dB}$  of 15dBm, and  $P_{sat}$  of 17.1dBm. The peak PAE is greater than 36.3% over 24-31GHz and 39.3-40.7% PAE is maintained over 25-30GHz. The output power at the peak PAE ranges 15.3-16.2dBm at 24-31GHz, Fig. 6-12 (a). The PAE is also measured for different supply voltages at 27GHz and is better than 40% over the  $V_{CC}$  range of 1.4-2.3V, Fig. 6-

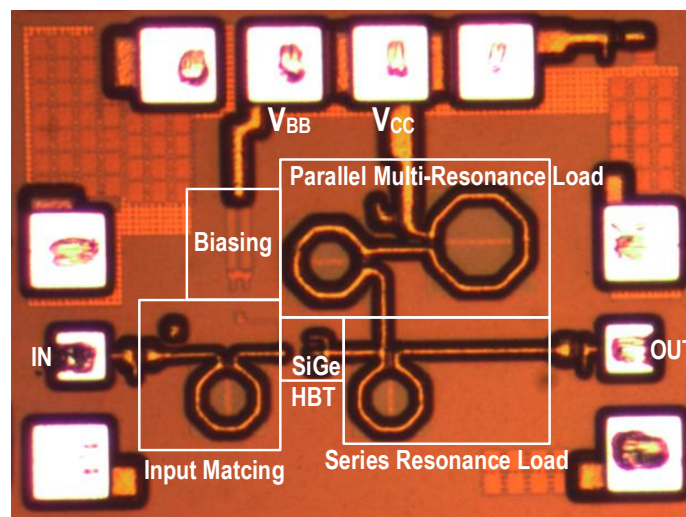


Fig. 6-10: The PA chip photograph (chip size:0.6x0.45mm<sup>2</sup> w/i pads, 0.48x0.3mm<sup>2</sup> w/o pad).

12 (b). It is notable that the measured linear-mode PAE at 6dB-back-off from the  $P_{\text{sat}}$  is 26% (Fig.6-11 (a)), still comparable to the peak PAE of the state-of-the-art silicon designs. Without pad the PA occupies only  $0.48 \times 0.3 \text{mm}^2$ , conducive for further integration into a large PA array for a higher  $P_{\text{out}}$ .

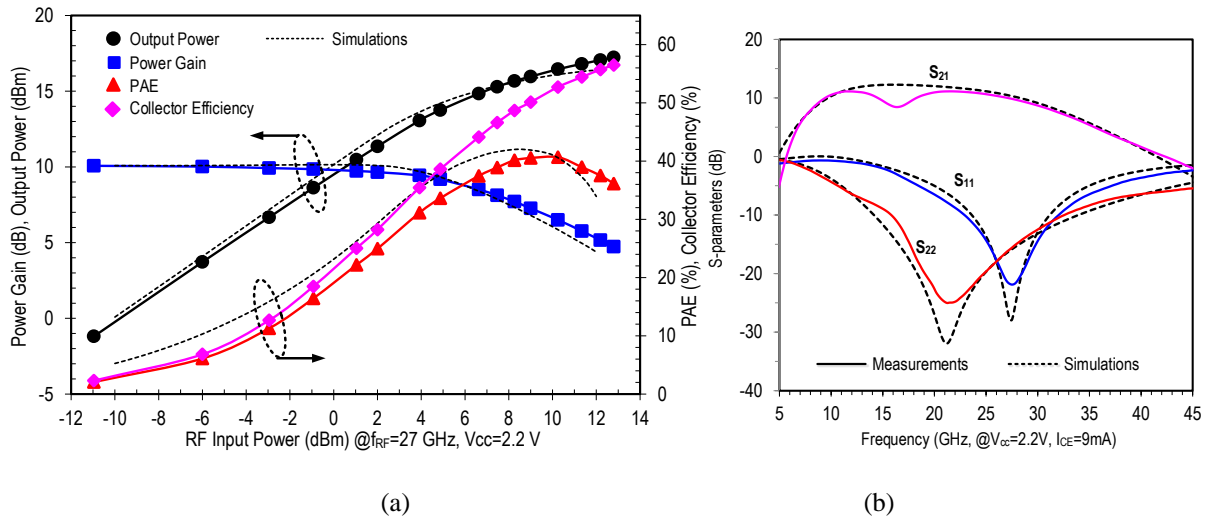


Fig. 6-11: Simulated and measured performance of the PA: (a)  $P_{\text{out}}$ , power gain, PAE, and collector efficiency at 27GHz, (b) small signal SP.

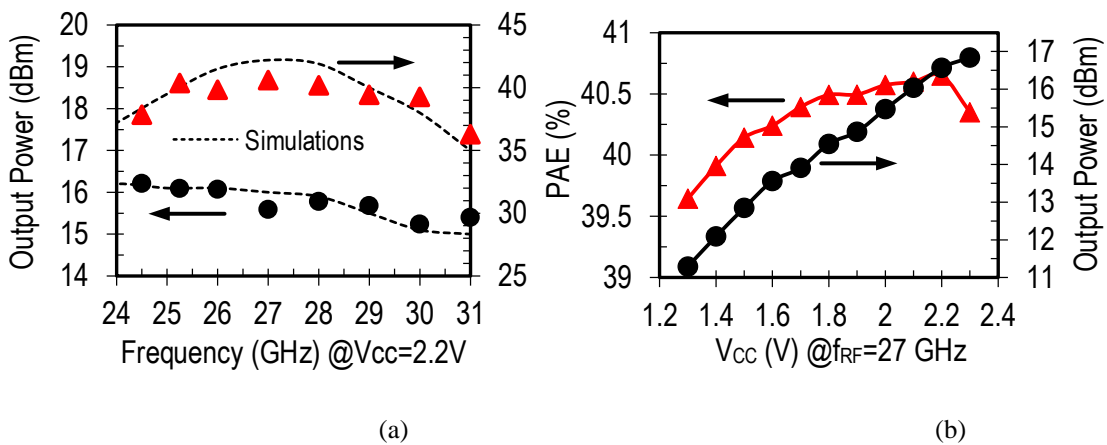


Fig. 6-12: The large signal performance of PA: (a) peak PAE and corresponding  $P_{\text{out}}$  over signal frequency band, (b) peak PAE and corresponding  $P_{\text{out}}$  for different supply voltages at 27GHz.

## 6.5 Summary

This chapter presents a simple LC-based multi-resonance network proposed which provides in band mode transition from Continuous-Class-F<sup>-1</sup> to Continuous-Class-F to increase peak PAE bandwidth of PA. The PA operated at Continuous-Class-F<sup>-1</sup> mode at low signal frequency band and Continuous-Class-F mode at high signal frequency band. The design steps and analysis presented for the PA. By using mode-transition, PAE > 36.5% achieved over 25% fractional bandwidth (25 GHz~31 GHz).

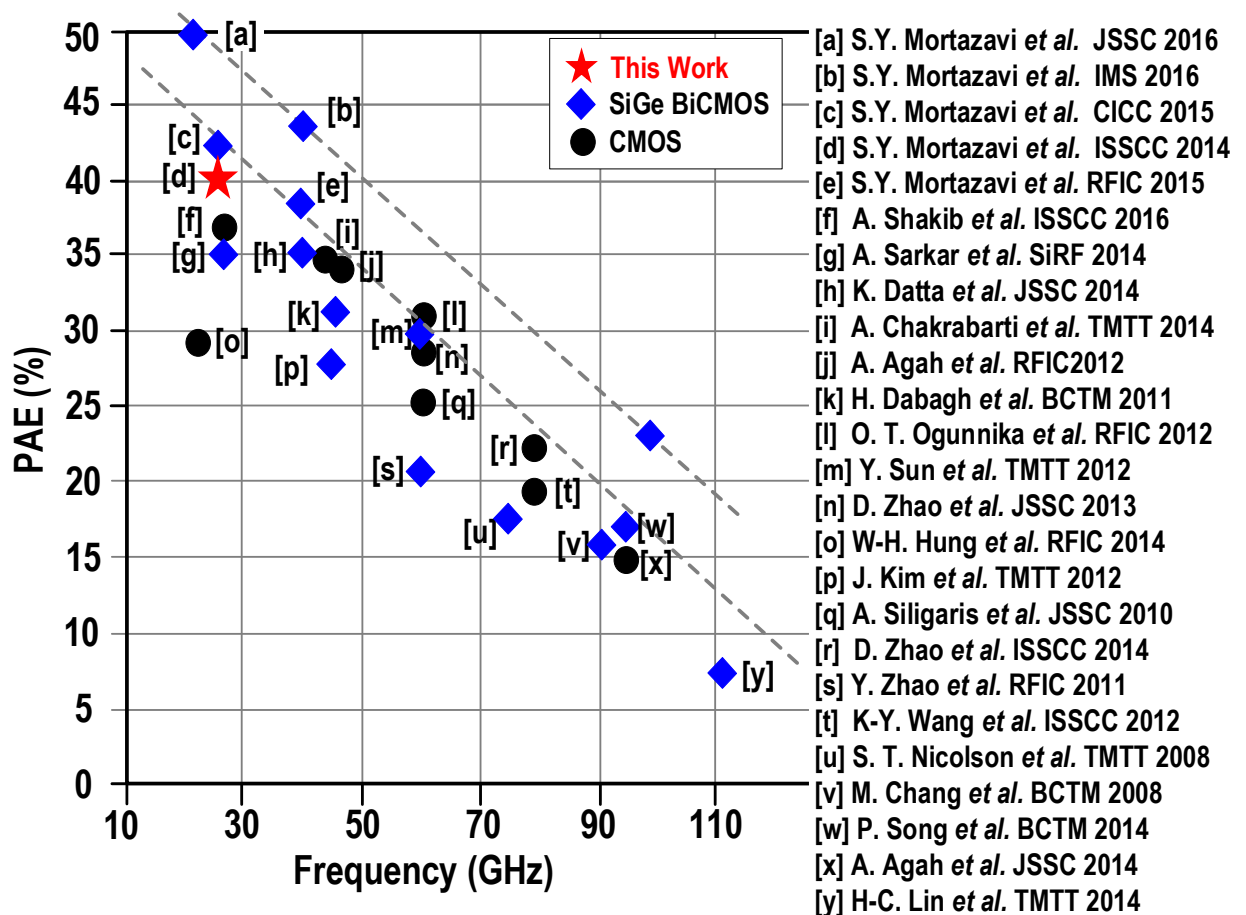


Fig. 6-13. PAE performance of the mm-wave silicon PAs



# 7 Conclusion

## 7.1 Summary and conclusion

The exploding growth of data traffic in wireless systems draws attention to unlicensed mm-wave frequency bands. However, designing high-performance circuit and systems with low-cost silicon devices is challenging. Low device speed (low  $f_T/f_{MAX}$ ) is main limiting factor for RF front-end building blocks of the transceivers. In addition to low device speed, power amplifiers in silicon technologies suffer from low break-down voltage. This reduces the peak power and power efficiency of the power amplifier and thus drastically increases the power consumption of the transceiver.

In this research, for the first time, we are utilizing Class  $F^{-1}$  harmonic tuning approach to improve the power efficiency and power added efficiency of the silicon PAs at mm-wave frequency bands. In Class  $F^{-1}$  PAs, the even harmonic loads are open circuit ( $Z_{2n} = \infty$ ) and odd harmonic loads are short circuit ( $Z_{2n+1} = 0$ ). Therefore, the harmonic components shape the waveforms to make non-overlapped rectangular current and half sinusoidal voltage waveforms. This research utilizes 2<sup>nd</sup> and 3<sup>rd</sup> harmonic tuning for improving efficiency of the PA. The potentials and limitations of the class- $F^{-1}$  technique in achieving a high PAE at microwave and higher frequencies, especially for integrated PAs based on silicon process; the impact of a finite number of harmonics control, knee voltage, limited breakdown voltage, and finite losses from passive components on the PAE has been analyzed.

To demonstrate effectiveness of the Class- $F^{-1}$  approach a multi-resonance 6<sup>th</sup> order load network is proposed which achieves 50% power added efficiency with 18dBm output power at 24GHz. By optimizing this network for 38GHz, based on the loss of passive components, PAE of 38.5% achieved. The design methodology developed for this network and extensive small signal, large signal, and linearity performance of both PAs presented in chapter 3.

To further improve power efficiency of Class  $F^{-1}$  PAs, coupled inductor based harmonic tuning load network proposed. The load network, utilizes coupled inductors to enhance quality factor of the inductors and make wide bandwidth high impedance at 2<sup>nd</sup> harmonic and very low impedance at 3<sup>rd</sup> harmonic, which improves both efficiency and efficiency bandwidth. By using

this load network and optimizing for 28GHz, 2-stage PA implemented with PAE~42% with 16.5dBm output power. This is presented in chapter 4.

As frequency increases to >30 GHz, the complexity of load network degrades the power efficiency improvement of the Class-F<sup>-1</sup> PAs. In chapter 5, a simple  $\lambda/4$  transformer based load network proposed to tackle this issue and achieve high power efficiency. The load provides optimum load at fundamental and high impedance at 2<sup>nd</sup> harmonic frequency band. To provide low impedance at 3<sup>rd</sup> harmonic band, the load network relies on parasitic capacitance at the output node of the power transistor. Using this load network, PAs implemented with exceptional PAE performance of 43% at 41 GHz and 23% 94 GHz with output power of 18 dBm and 11 dBm, respectively.

Harmonic tuned PAs suffer from narrow efficiency bandwidth mainly due to narrow-band 2<sup>nd</sup> harmonic tuning load network. To increase peak PAE bandwidth of PA, a simple LC-based multi-resonance network proposed which provides in band mode transition from Continuous-Class-F<sup>-1</sup> to Continuous-Class-F. The PA operated at Continuous-Class-F<sup>-1</sup> mode at low signal frequency band and Continuous-Class-F mode at high signal frequency band. By using mode-transition, PAE > 36.5% achieved over 25% fractional bandwidth (25 GHz~31 GHz). This design presented in chapter 6.

In summary, this research presents different harmonic tuning load networks for Class F<sup>-1</sup> operation to address different issues and improve efficiency of mm-wave silicon PAs. Table 7-1, Fig. 7-1, and Fig. 7-2 compare the PAE performance of the proposed harmonically tuned PAs with state-of-the-art silicon PAs.

Table 7-1. State-of-the-art silicon PAs

Authors	Freq.(GHz)	PAE (%)	P <sub>sat</sub> (dBm)	OP <sub>-1dB</sub> (dBm)	Gain (dB)	Size (mm <sup>2</sup> )	Supply (V)	Technology	Feature
<b>JSSC 2016</b>	24	50	18	16	21	0.6	2.3	0.13 $\mu$ m SiGe	2-stage Class-F <sup>-1</sup>
<b>RFIC 2015</b>	38	38.5	16.5	15	18.5	0.5	2.4	0.13 $\mu$ m SiGe	2-stage Class-F <sup>-1</sup>
<b>IMS 2016</b>	41	43	18	16.5	20.	0.64	2.4	0.13 $\mu$ m SiGe	2-stage Class-F <sup>-1</sup>
	94	23	12	9.5	10.5	0.72	2.	0.13 $\mu$ m SiGe	3-stage Class-F <sup>-1</sup>
<b>CICC 2015</b>	28	42	17.1	15	21.2	0.49	2.4	0.13 $\mu$ m SiGe	2-stage Class-F <sup>-1</sup>
<b>ISSCC 2014</b>	28	40.7	17.1	15	10.3	0.27	2.2	0.13 $\mu$ m SiGe	1-stage Class-F <sup>-1</sup>
ISSCC 2014	28	40.7	17.1	15	10.3	0.27	2.2	0.13 $\mu$ m SiGe	1-stage Class-F <sup>-1</sup>
SIRF 2014	28	35.3	18.6	15.5	15.3	0.43	3.6	0.13 $\mu$ m SiGe	2-stage Class-F <sup>-1</sup>
BCTM 2011	37.5	26.2	14.8	NA	5.6	0.74	2.5	0.13 $\mu$ m SiGe	2-Stage Class-B
JSSC 2014	41	36	18.1	NA	21.2	0.49	2.4	0.13 $\mu$ m SiGe	1-stage Class-E
RFIC 2012	42.5	34.4	18.6	17.5	9.5	0.3	2.7	45 nm SOI CMOS	3-stack Class-AB
RFIC 2012	24	29	18	NA	NA	0.91	1.2	65 nm CMOS	2-stage Class-AB
IMS 2012	24	24	19	15.7	19	0.4	3.6	0.18 $\mu$ m CMOS	2-stage Class-AB
RFIC 2014	18	41.4	15.9	13.3	11	0.62	2	45 nm SOI CMOS	Cascode Class-E



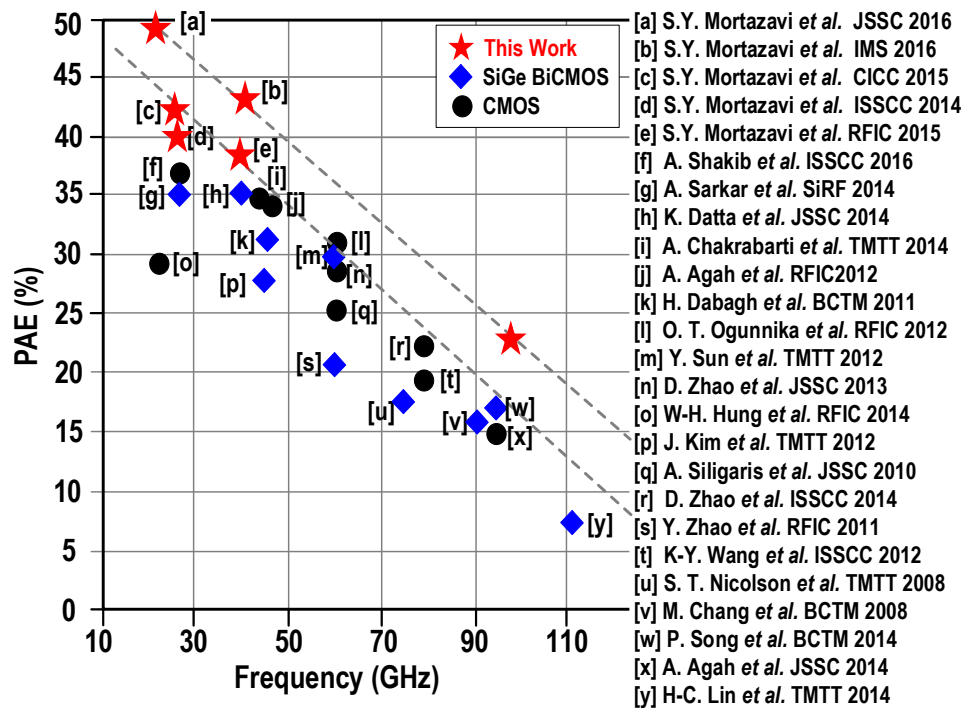


Fig. 7-1: PAE performance versus frequency comparison for mm-wave silicon PAs.

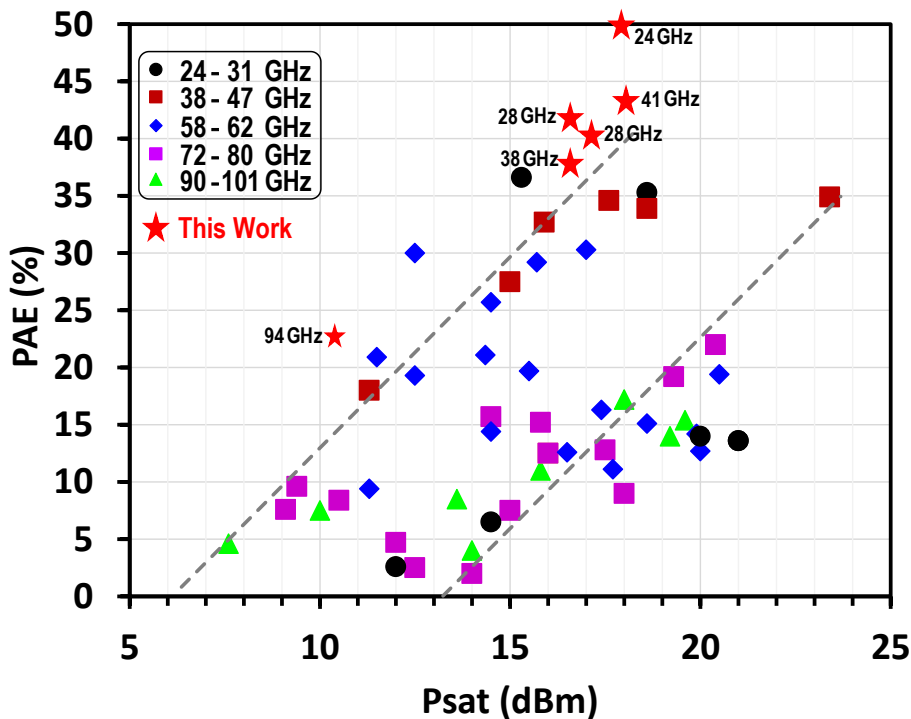


Fig. 7-2: PAE versus  $P_{sat}$  performance comparison for mm-wave silicon PAs.

## 7.2 Contributions

This research is the first work addressing the challenges and limitations of the high efficiency Class-F<sup>-1</sup> PAs for mm-wave silicon technology using 0.13  $\mu\text{m}$  SiGe BiCMOS. Key contributions of this research are as following:

1. The limitations and challenges of the Class-F<sup>-1</sup> harmonic tuning approach for mm-wave silicon PAs addressed and a multi-resonance LC-load network proposed for Class-F<sup>-1</sup> PA as a proof of concept for viability of achieving high power efficiency beyond state-of-the-art silicon PAs. The design methodology and detailed analysis presented and verified with PA implementation at 24 GHz (PAE = 50%,  $P_{\text{sat}} = 18$  dBm) and 38 GHz (PAE = 38.5%,  $P_{\text{sat}} = 16.5$  dBm).
2. To address the issues of low quality factor of the passives in the load network, a Q-enhancement method proposed for Class-F<sup>-1</sup> based on coupled inductors. The design methodology and analysis presented and verified with PA implementation at 28 GHz (PAE = 42%,  $P_{\text{sat}} = 16.5$  dBm).
3. To mitigate power efficiency degradation in Class-F<sup>-1</sup> PAs due to low-quality passives at high mm-wave frequencies, a simplified load network is proposed based on  $\lambda/4$ -transformer. The design methodology and analysis presented and verified with PA implementation at 40 GHz (PAE = 43%,  $P_{\text{sat}} = 18$  dBm) and 94 GHz (PAE = 23%,  $P_{\text{sat}} = 11$  dBm).
4. To increase efficiency bandwidth of harmonically tuned PA, a multi-resonance LC-based load network proposed with in band mode transition from Continuous Class-F<sup>-1</sup> to Continuous Class-F to achieve wide efficiency bandwidth. The design methodology and analysis presented and verified with PA implementation at 28 GHz (PAE > 39% @ 25-31 GHz,  $P_{\text{sat}} = 17.2$  dBm).

### 7.3 Future research direction

This work demonstrates the feasibility of the Class-F<sup>-1</sup> harmonic tuning approach for mm-wave silicon PAs. Further improving power efficiency using different techniques input harmonic termination, or harmonic injection at mm-wave would be a natural extension of this work, yet quite challenging due to tight complexity-efficiency trade-off at mm-wave bands. Another extension of this work would be investigating the power efficiency improvement at back-off powers based on envelope tracking and supply modulation techniques and integrating with proposed PAs for mm-wave applications.

Investigating harmonic tuning approach for mm-wave stacked silicon PAs would increase the power efficiency and output power of the unit PA and be a big step toward wattlevel (>30 dBm) high efficiency mm-wave silicon PAs. Shaping the waveforms of the inter-stack devices in presence of parasitics would be the main challenge for this approach at mm-wave.

Even though the main focus of this research is improving power efficiency, the linearity enhancement is also vital for advanced wireless communication systems. Investigating the effect of different harmonic tuning techniques on PA linearity and output power would be a complementary study. Investigating and developing wideband linearization techniques near output compression point where the peak power efficiency) would be a challenging and practical future work.

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