Modeling and Electrical Characterization of Ohmic Contacts on n-type GaN

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ABSTRACT

As the current requirements of power devices are moving towards high frequency, high efficiency and high-power density, Silicon-based devices are reaching its limits which are instigating the need to move towards new materials. Gallium Nitride (GaN) has the potential to meet the growing demands due to the wide band-gap nature which leads to various enhanced material properties like, higher operational temperature, smaller dimensions, faster operation and efficient performance. The metal contacts on semiconductors are essential as the interface properties affect the semiconductor performance and device operation. The low resistance ohmic contacts for n-GaN have been well established while most p-GaN devices have still high contact resistivity. Significant work has not been found that focuses on software-based modeling of the device to analyze the contact resistance and implement methods to reduce the contact resistivity. Understanding the interface physics in n-GaN devices using simulations can help in understanding the contacts on p-GaN and eventually reduce its metal contact resistivity.

In this work, modeling of the metal-semiconductor interface along with the effect of a heavily doped layer under the metal contact is presented. The extent of reduction in contact resistivity due to different doping and thickness of n^{++} layer is presented with simulations. These results have been verified by the growth of device based on simulation results and reduction in contact resistivity has been observed. The effect of different TLM pattern along with different annealing conditions is presented in the work.

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GENERAL AUDIENCE ABSTRACT

Technology has become part and parcel of the life of humans which is slowing gearing towards Automation, Internet of Things (IoT). The hardware for this is being provided by semiconductor silicon for a very long time. However, the demand is moving towards smaller size and better performance. Silicon material has reached its limitations in terms of dimension scaling and performance enhancement. A quest for new material has led to Gallium Nitride (GaN) which has the potential to provide enhanced properties like higher operational temperature, smaller dimensions, faster operation and efficient performance. Metal contact on the semiconductor is essential as these contacts provide the external connection. The contact characteristic of the metal-semiconductor interface is evaluated by contact resistance. It is expected that contact has linear IV characteristics (ohmic contact) and low contact resistance to avoid perturbing the semiconductor performance in devices.

There are metals which can provide ohmic contacts for n-GaN but they offer low contact resistance only on annealing. These contact characteristics are studied by simulating the metal-semiconductor interface by replicating the thermionic and tunneling effects at the junction by physics-based device modeling. It is essential to reduce the contact resistivity for better interface properties which can be provided by a heavily doped (n^{++}) layer under the metal layer. The effect of various doping and thickness of n^{++} layer is presented in this research work. Devices were grown based on simulation results and the extent of reduction in contact resistivity due to the n^{++} layer is documented in this research. This reduction in contact resistivity can aid in a significant reduction in power dissipation in the devices which could lead to efficient device operation.

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1 Introduction

The world is growing at a fast pace and moving towards automation due to the humungous advancement in technology over the past few years. This progress has been possible because of the growth of the semiconductor materials. The demand for the advancing technology is to be able to get smaller devices (occupy smaller area) and operate faster (high operation frequency).
Silicon has been the dominant semiconductor in use for a majority of the purpose for a very long time. However, Silicon-based devices are reaching its limit in terms of frequency, temperature and dimension scaling.
According to Moore's law, the number of transistors in an integrated circuit doubles every two years. Moore's law based on Silicon has reached its limit in terms of material properties. In the past few years, the number of transistors per chip has almost begun to reduce while the achievable clock frequency has saturated for quite some time now[1]. The clock frequency determines the speed of operation for a device. The maximum achievable switching frequency is determined by the tradeoff between frequency and switching loss. This reduction in the number of transistors per chip and saturating clock frequency validates that the silicon material properties have reached its limits and it is necessary to move on to other materials which can continue Moore's law further.
In order to keep Moore's law active, researchers are moving towards new materials which could provide the better material properties than Silicon. The research has been propelling towards wide band-gap materials like Silicon Carbide, Gallium Arsenide, and Gallium Nitride (GaN).

1.1 Properties of Wide Band-Gap Semiconductors

Wide band-gap (WBG) semiconductors are the semiconductor with large band gap typically greater than 2eV[2]. The wide band-gap of the semiconductor material offers various advantages. Due to the large band-gap, the device of WBG semiconductors can operate at much higher operational conditions like higher voltages, current, temperature, and higher frequency than devices based on typical semiconductors. WBG semiconductors can also withstand much higher critical electric field. The much higher operational frequency of WBG semiconductors is due to the high free electron velocity in WBG semiconductors. The higher voltage and current

achievable by WBG semiconductors lead to a much higher power density of WBG semiconductor devices. These devices have high breakdown voltage as a large electric field is needed to create breakdown through impact ionization or phonon scattering as the device has large band-gap.

The various wideband gap materials available are Silicon Carbide (SiC), Aluminum Nitride (AlN), Gallium Nitride(GaN), Boron Nitride (BN) etc., The material of interest for this research is Gallium Nitride (GaN) which has a band-gap of 3.4 eV which is much higher than Silicon (1.2 eV band-gap). The properties of GaN material is shown in TABLE 1-1.

The most preferred type of GaN crystal is the Wurtzite structure which allows spontaneous polarization of the GaN material [2]. This polarization effect causes polar surfaces which have higher sheet carrier density. The direct band-gap nature of GaN leads to the fact that the momentum of electrons and holes are same in the conduction band and valence band.

TABLE 1-1. Property of Gallium Nitride[3].

Property	**Gallium Nitride**
Crystal Structure	Wurtzite
Type (Direct /Indirect)	Direct Band-gap devices
Band-gap (eV)	3.425
Electron affinity (eV)	4.1
Electron Mobility (cm^2/V-s)	1500
Hole Mobility (cm^2/V-s)	30
Intrinsic carrier concentration (cm^{-3})	1.9×10^{-10}
Electron effective mass m_e^*	0.2 m_o
Hole effective mass m_{hh}^*	1.0 m_o
Effective DOS at CB edge (cm^{-3})	2.3×10^{18}
Effective DOS at VB edge (cm^{-3})	1.8×10^{19}
Dielectric constant	8.9
Breakdown field (V cm^{-1})	5×10^6
Electron Diffusion coefficient (cm^2s^{-1})	25
Hole Diffusion coefficient (cm^2s^{-1})	5

The polarization nature of GaN has an advantage which improves the properties of GaN devices. When AlGaN layer is grown on top of GaN, polarization nature of the two layers leads to the formation of the 2-Dimesional Electron Gas (2DEG) [4]. This 2DEG layer has a very high mobility which reduces the on-resistance. On-resistance is defined as the resistance offered by the semiconductor bulk through which ideally current flows inside the semiconductor device. The entire voltage drop measured across the GaN device upon application of voltage is caused due to the on-resistance offered by the MOSFET. This low on-resistance of GaN is utilized to make High Electron Mobility Transistors (HEMT) which provides superior performance compared to Silicon MOSFETs.

GaN-based devices have much smaller feature size than Silicon counterparts for the same operational conditions. The small size of GaN devices reduces the area occupied leading to higher power density and provides smaller conduction path in the devices leading to lower on-resistance. GaN devices offer lower capacitance due to the smaller area occupied by GaN devices. This smaller capacitance reduces the switching times (on-time and off-time) which causes lower switching losses of GaN devices. The high electron mobility of GaN lowers the on resistance of GaN FETs which still reduces the conduction losses. The reduction in conduction loss and switching loss causes a net reduction in the losses of GaN devices. Hence, the GaN devices operate at high efficiency at higher frequency

1.2 GaN vs. Si vs. SiC

Silicon is the most predominantly used well-established semiconductor for commercial purposes. Wide band-gap materials like Silicon Carbide and Gallium Nitride is gradually beginning to replace Silicon due to the exceptional material properties and their prospective superior performance. The comparison between the material properties of Si, SiC and GaN are provided in TABLE 1-2.

TABLE 1-2. Comparison of properties of Si, SiC, and GaN.

Properties	**Silicon (Si)**	**Silicon Carbide (SiC)**	**Gallium Nitride (GaN)**
Band-gap(eV)	1.12	3.26	3.4
Electric field critical (MV/cm)	0.23	2.2	3.0
Thermal conductivity (W/cm^2 K)	1.5	5	1.3
Electron Mobility (cm^2/V-s)	1400	950	800/1700
Saturated electron drift velocity (cm/s)	1.0×10^7	2×10^7	2.5×10^7
Permittivity	11.9	9.7	8.9
BFOM [5] with respect to Si	1	500	1300/2700

$$\text{BFOM} = \varepsilon_s \mu_n {E_C}^3 \tag{1-1}$$

Baliga Figure of Merit (BFOM) is calculated as shown in Eq.(1-1). SiC and GaN have wider band-gap as discussed before. The wide band gap devices have a much higher critical field which is 10 times the critical field of Si. The permittivity of GaN is smaller than Si and SiC. The electron mobility of SiC is much smaller than Si or GaN. The mobility of GaN material is smaller. However, 2DEG layer gives much higher electron mobility which contributes to the reduction of conduction losses. The thermal conductivity of SiC is much higher than Si or GaN. Hence, SiC is preferred for operation at a much higher power and high temperature than GaN devices. The high efficiency of GaN devices implies that it has lower power losses or lesser heat to be dissipated. Hence, lower thermal conductivity does not create a major issue for GaN-based devices. Baliga Figure of merit is calculated using Eq. (1-1). GaN material has higher critical electric field and higher mobility which contributes to GaN with much higher BFOM than Si or SiC. Hence according to BFOM, GaN material is much better compared to Silicon Carbide. Thus, this research focuses on GaN material and its contact resistance properties.

1.3 Application of GaN devices

As discussed before, the wide band-gap of GaN enables its use in high power, high-temperature applications. GaN is a suitable candidate for lasers. It has widespread application in the production of blue laser which is being used in Blu-ray technology for faster writing and retrieving of the data into storage devices.

GaN HEMT devices based on 2-DEG formation offers higher efficiency operation. This enables GaN devices to be used for radio applications as well huge energy conversion purpose at power grids. The high-efficiency operation of GaN devices at high power allows it to be utilized in military applications.

1.4 Significance of contact resistance in semiconductor devices

By definition, contact resistance refers to the resistance offered by the electrical leads instead of the actual material in scrutiny. The electrical leads for semiconductor are provided by the metals deposited on top of it. Unlike two metal interfaces, metal-semiconductor interface does not have negligible resistance. Appropriate metal needs to be selected to provide good contact. When a voltage is applied to two metal contacts, the major contributors to voltage drop are two metal contacts, semiconductor, and two metal-semiconductor interfaces. Metals are very good conductors and hence, the contribution is negligible. In order to have an efficient metal-semiconductor contact, it is necessary that the contribution of resistance at metal-semiconductor interface should be as small as possible so that major voltage drop occurs across the semiconductor and help in characterizing semiconductor performance than being perturbed by the metal interface.

From a circuit point of view, contact resistance contributes to on-resistance of the device which further increases the conduction losses in the circuit. Excessive heat can be generated at the metal contacts in case of high contact resistance which could damage the contact. Hence, the contact resistance is a very important parameter for device characterization as well utilization of device in the circuit. It is necessary to ensure that the contact resistance is low enough to prevent the hindrance caused by the metal in characterizing the semiconductor.

1.5 Different types of Device Modeling

Computer simulations are hugely appreciated as they save a lot of time and money compared to actual device growth and fabrication. It also gives a complete insight into the device performance and characteristics. Computer Aided Design (CAD) provides the opportunity to simulate multiple conditions which require a tedious process to achieve practically. There are different types of modeling available for the devices. The most predominant modeling methods are physics driven modeling and compact modeling.

Physics-driven models are based on the physics of the device technology. These models are based on structure, material properties, and device physics. Physical modeling is based on mathematical equations that describe the physics governing the operation of the device. Physics-based modeling can be used to obtain I-V characteristics, C-V characteristics, Breakdown characteristics, and various device level performance parameters.

Compact models are generally used to provide equivalent circuit models for devices using active and passive circuit components like resistor, capacitor, current or voltage sources. These models are developed based on measurement of device characteristic based on testing results or results obtained from physics-based modeling. Compact models do not deal with the basics physics of the device operation. These models are further used for circuit design using high-level simulators like SPICE simulators. Compact models are less extensive than Physics-driven models in order to make them compatible with circuit simulators.

Physics-based models consume more time as they focus on physics. However, they are more accurate in determining the effect of contact resistance which is the main focus of my research. Hence, physics driven device modeling of the metal-semiconductor interface is chosen for my research work which motivates me to use Sentaurus TCAD to model the contact resistance of the devices.

1.6 Literature Review

The study of providing good contacts to semiconductors has been prevalent for a long time[7][8]. III-V semiconductors had begun to get attention from the late 1970s[9]. Hence, metal contacts on these materials have been studied extensively since then. The contact resistance at the ohmic

contacts is expected to be around 10^{-5} to 10^{-6} Ω-cm^2 so that the contact resistance does not affect the device performance[10]. The barrier height is expected to be low in order to have a good ohmic contact at the metal-semiconductor interface. There were many methods to obtain low metal-semiconductor contact resistances namely metal with low work-function, heavily doped layer under contact, graded hetero-junction approach, non-alloyed short period super-lattice structure (SPS), increasing density of recombination centers at the interface, etc. [11]. The concept of the heavily doped layer under the metal contact to provide low contact resistance was also known as the high-low junctions[12]. A shallow layer of a heavily doped semiconductor with the thickness equal to the depletion width at metal n-type semiconductor interface provides good ohmic contact. Any further enlargement of the layer thickness does not contribute much to the reduction in contact resistivity[13]. The contact resistivity at high-low barriers is proposed to consist of two significant contributors, namely tunneling at the metal-n^+ interface and thermionic at the high-low interface[14]. Hence, the barrier at the n^+n interface needs to be considered especially when the heavy doping is more than critical doping of the semiconductor.

The wide band-gap semiconductors have band-gap around 2-4 eV which makes the metal to have huge work-function in order to get low barrier height. Ohmic contact on wide band-gap semiconductors can be achieved through another current transport mechanism namely, tunneling of current at the metal-semiconductor interface with high barrier height[8].

The extensive survey of various ohmic contacts to Gallium Nitride materials has been provided in [15]. Ohmic contacts on n-type GaN material due to Al contacts were studied in 1993. The metal deposited on the semiconductor layer is annealed to provide better ohmic contact behavior. However, [16] observed that annealing of the Al/n-GaN interface at 575°C for 10min increased the contact resistance by 50%. It was concluded that the annealing process leads to the formation of interface layer made with AlN. The annealed contacts on n-GaN material provided contact resistivity of about 10^{-7}Ω-cm^2[16].

Bilayer metallization of Ti/Al is one of the predominant methods for providing contact on n-GaN. In [17], it was observed that annealing of single metallization contacts gave higher specific contact resistivity than two layer metallization. [17] also reported that annealing of bilayer metallization at 900°C for the 30s reduced the contact resistance of $8x10^{-6}$ Ω-cm^2. At the same annealing temperature of 900°C, it was observed that the specific contact resistance keeps reducing till a certain time and then it starts increasing. This shows that there exists an optimum

time for certain annealing temperature which would lead to least possible specific contact resistivity. They proposed that the Ti metal layer on annealing leads to the formation of TiN by reaction of Ti and GaN layer. The formation of TiN could deplete the GaN surface layer of N atoms at the surface leading to the formation of n^{++} layer which leads to electron tunneling at the interface of metal-semiconductor. The TiN has another advantage of lower contact resistivity as the conductivity of the TiN is 1.3 times higher than Ti.

In [18], the nature of Ti/GaN interface was studied reported that the annealing temperatures below 850°C did not have any significant contribution to contact resistance. However, temperature above 900°C had a significant contribution to the reduction in specific resistivity which is due to the critical temperature for formation of TiN at the Ti GaN interface was around 900- 950°C. Wu.et.al reported that low contact resistance of $3x10^{-6}$ Ω-cm^2 was achieved due to annealing at a higher temperature.

There was a report of low resistance n-type Ohmic contact with a different metallization structure Ti/Al/Cr/Mo/Au[19]. This metallization structure provides low resistance smooth contact surface with contact resistivity of 1.1 x 10^{-6} Ω-cm^2 after annealing at 875°C and also maintains the low contact resistivity during storage at 200°C with Nitrogen flow. They proposed that the robustness of the metal contact is due to the layers of Cr and Mo which suppress the alloy formation in the contact stacks and Cr plays a major role in achieving low contact resistivity.

The low contact resistance metallization for p-GaN has always been a major research interest due to unavailability of metals of high work-function to provide an ohmic contact. The focus of research has been shifted since then onto the surface layers of metal and semiconductor in contact to understand the physics and then eventually reduce the contact resistance. There was a report on the analysis of the surface layers of GaN and metal work-functions[20]. It was concluded that the GaN surface grown using MOCVD (Metal Organic Chemical Vapor Deposition) has a contamination layer on the surface made of GaO_x and absorbed carbon. This layer was only partially removed on treatment with HF solution which did not result in any significant change in electrical properties of the material. Ohmic contacts to p-type GaN has been found get better by controlling the residual carbon impurity during the growth of the material[21]. They have reported a low contact resistance to p-GaN of 6.8 x 10^{-5} Ω-cm^2.

2 Theoretical Background

Semiconductor devices need electrical leads to provide an interface for external periphery. These leads are generally made of metals as they are good conductors of electricity. Hence, it is necessary to fabricate metals on semiconductors to be able to access semiconductors from outside. It is essential to understand the mechanisms of metal–semiconductor interface as that could affect the performance of semiconductor studied through the metal contacts. This metal-semiconductor junction could result in either rectifying or ohmic interface depending on the nature of the metal and semiconductor layer beneath it. Rectifying metal-semiconductor is called Schottky barriers. Ohmic interfaces are called ohmic contacts. Ohmic contacts are the preferred type of contact on semiconductors for providing electrical connection to the semiconductor.

The contact is characterized by the contact resistivity which gives an estimate of the resistance offered to the current flow at the metal-semiconductor junction. The resistance at the interface is important as it affects the performance as well as the parameters extracted using the metal contacts. This contact resistivity is defined as the rate of change in voltage with respect to current density as voltage approaches zero as given by Eq. (2-1).

$$\rho_c = \left(\frac{\partial V}{\partial J}\right)\Big|_{V \to 0} \tag{2-1}$$

As the technology has been progressing towards smaller size, efficient operation and better performance, it has become increasingly important to characterize the contact resistance. As the device keeps getting smaller, the resistance contributed by semiconductor keeps reducing and the metal-semiconductor interface resistance becomes more significant. It is necessary to reduce the resistance at the contact to avoid excessive heat generation due to resistance at the metal-semiconductor interface. Excessive heat generation at metal-semiconductor interface could wear off metal deposited on semiconductor and ruin the electrical contact to the semiconductor.

2.1 Metal-Semiconductor Interface

It is necessary to understand the physics at the metal-semiconductor interface in order to interpret the cause of contact resistance. This can be studied using energy band diagram at the interface of metal and semiconductor. The parameters used in defining the performance of the interface are as follows.

φ_s	-	work-function of the semiconductor	-	E_{VAC} - E_{Fs}
φ_m	-	work-function of the metal	-	E_{VAC} - E_{Fm}
χ	-	electron affinity of the semiconductor	-	E_{VAC} - E_C
E_g	-	Band-gap of the semiconductor	-	E_C – E_V
Ref	-	Reference Energy level - Vaccum	-	E_{VAC}

Vacuum energy level is the reference level which is used to compare the energy of metal and semiconductor. Work-function is the energy difference between the vacuum and the Fermi energy level. Electron affinity is defined as the energy needed for the electron at the bottom of the conduction band to reach the vacuum energy level. The band gap is the energy difference between the top of the valence band to bottom of the conduction band. The energy band diagram of the metal and semiconductor before putting into contact is shown in the Fig. 2-1.

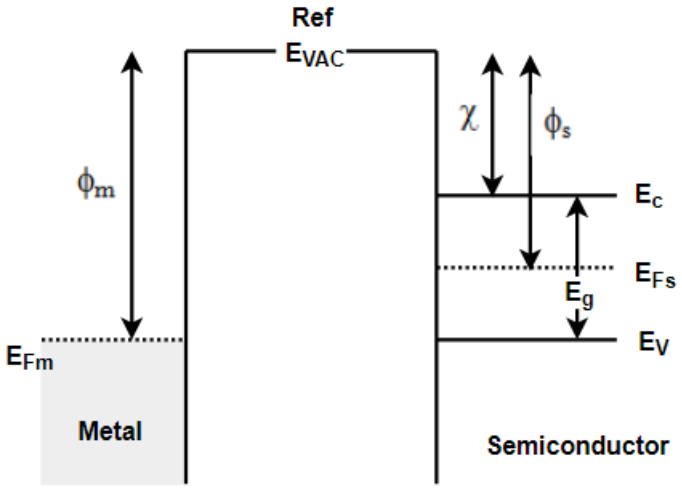

Fig. 2-1. Metal and n-type Semiconductor before putting into contact.

When the metal and semiconductor are brought into intimate contact the energy levels get rearranged such that the Fermi levels on metal and semiconductor line up. Due to the rearrangement of energy levels, the energy barrier is created at the interface. Barrier height is defined as the height (energy difference) the electrons have to cross through for traveling between metal and semiconductor. Barrier Height is the difference between the work-function of metal and electron affinity of the semiconductor. Due to the rearrangement of energy levels, the conduction band in the n-type semiconductor is pulled down and the change in the energy level gives rise to the development of voltage at the interface which is called Built-in voltage. Barrier height is given by Eq.(2-2). Built-in voltage is given by Eq. (2-3).

$$\varphi_B = \varphi_M - \chi \tag{2-2}$$

$$V_{bi} = \varphi_m - \varphi_s \tag{2-3}$$

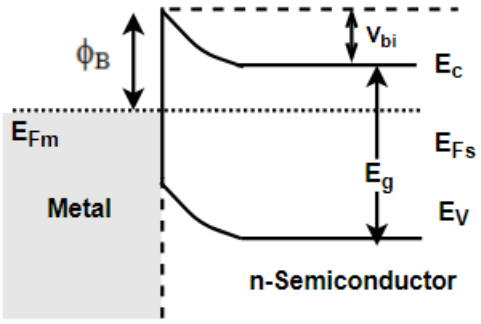

Fig. 2-2. Metal- n-type Semiconductor put into intimate contact.

From Fig. 2-2, band bending occurs at the interface of metal and semiconductor. This region is the depletion region in the semiconductor. It is assumed that the metal has charged in the form of sheet charge while the charge in the semiconductor is spread through the depletion region. This region of charge in semiconductor gives rise to the electric field and further potential in the region which is the built-in voltage. On applying the full-depletion analysis at the interface, the width of the depletion region can be calculated. The depletion width at the interface of metal and semiconductor is given by Eq. (2-4).

$$x_d = \sqrt{\frac{2\varepsilon_s(V_{bi} - V_a)}{qN_d}} \tag{2-4}$$

2.1.1 Types of Contact – Ohmic contact and Schottky contact

The metal and semiconductor, when put into contact, can give rise to either ohmic contact or Schottky contact. Ohmic contacts are the most preferred contact as this allows the current to flow in both directions. Schottky contacts allow the flow of current only in one direction. In Schottky contact, when a reverse bias voltage is applied between metal and semiconductor contact, then current flow is negligible which prohibits current flow at the contact when a positive bias is applied to the semiconductor with respect to metal.

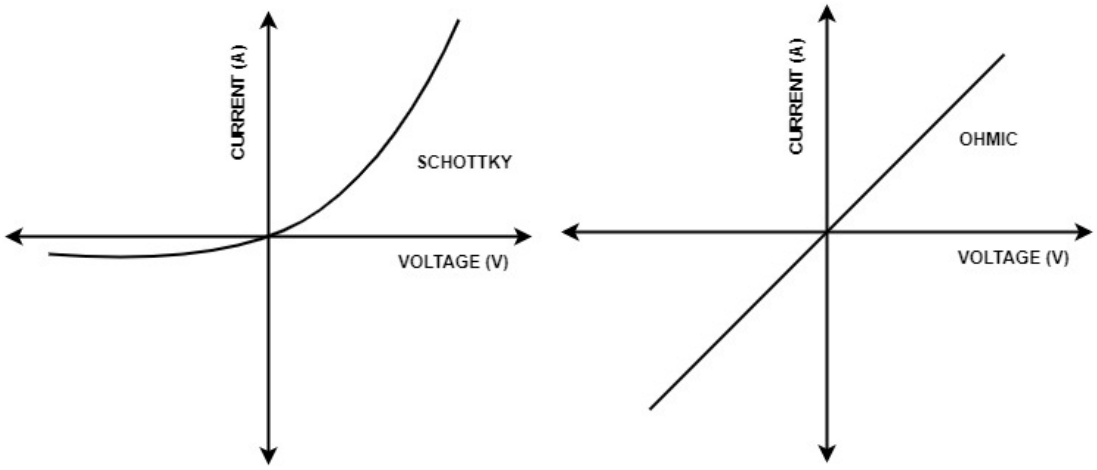

Fig. 2-3. Schottky and Ohmic Contact IV curve.

I-V characteristics of ohmic and Schottky contact are shown in Fig. 2-3. The exponential characteristics of the schottky contact can be described as shown in Eq. (2-5). The linear curve of ohmic contact is shown in Eq. (2-6).

$$I = I_s \left[exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{2-5}$$

Where I_s = saturation current and N= ideality factor

$$I = \frac{V}{R} \tag{2-6}$$

Where R= Resistance offered to current flow.

A metal contact on the semiconductor is expected to provide an electrical connection which can conduct current under all voltage conditions. Thus, it is necessary for the contact to be ohmic contact so that performance of semiconductor is unaffected by the limitation of current at the metal-semiconductor interface. The comparison of the work-function of metal and semiconductor to obtain ohmic and Schottky contact for n-type and p-type semiconductor is provided in TABLE 2-1.

TABLE 2-1. Ohmic and Schottky contact condition.

Contact	**Ohmic**	**Schottky**
Barrier Height	low	High
n-type semiconductor	$\phi_M < \phi_S$	$\phi_M > \phi_S$
p-type semiconductor	$\phi_M > \phi_S$	$\phi_M < \phi_S$

2.2 Current Conduction Mechanism at Metal-Semiconductor Interface

The current flow at the metal-semiconductor interface could be due to thermionic emission or field emission or the combination of both. The idea about the possible current conduction mechanism can be obtained based on characteristic energy level E_{00} given by Eq. (2-7).

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{K_s \varepsilon_0 m^*_{tun}}} = 1.86 \text{ x } 10^{-11}\sqrt{\frac{N}{K_s\left(m^*_{tun}/m\right)}} \tag{2-7}$$

Where N is doping density, m^*_{tun} is tunneling effective mass, m is the free electron mass. The conduction mechanism is determined based on the comparison between characteristic energy E_{00} and thermal energy kT.

$kT \gg E_{00}$ Thermionic Emission

$kT \approx E_{00}$ Thermionic Field Emission

$kT \ll E_{00}$ Field Emission

The characteristic energy, thermal energy is plotted against the doping density in Fig. 2-5. As, the doping increases, E_{00} keeps increasing and the conduction mechanism shifts from thermionic emission to thermionic field emission and later to field emission.

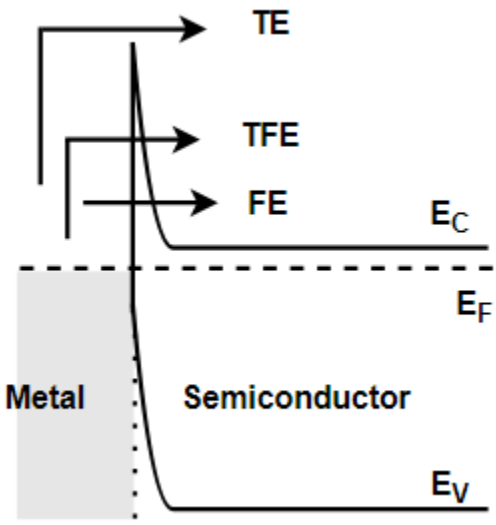

Fig. 2-4. Different Current Conduction Mechanisms at the metal-semiconductor interface.

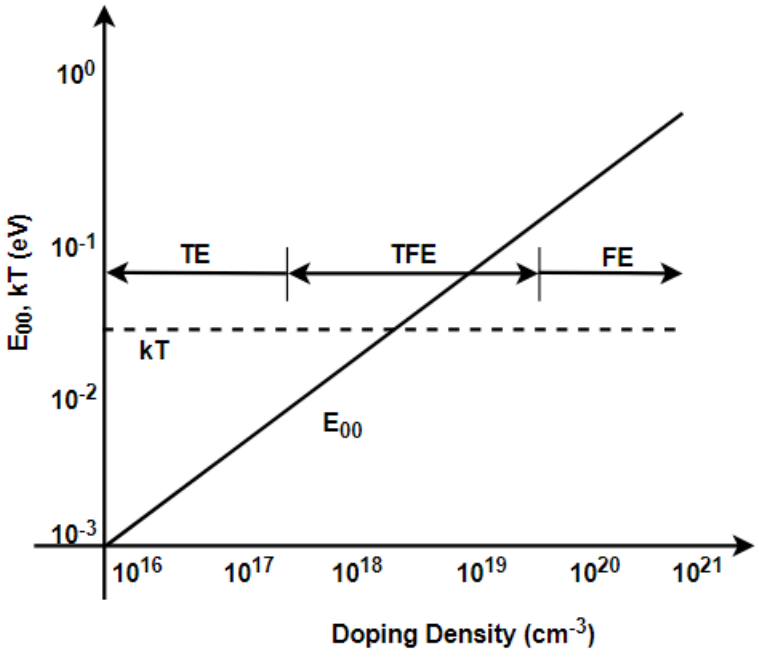

Fig. 2-5. E_{00} and kT as function of doping density for Silicon with m_{tun}/ m= 0.3 at 300 K [10].

2.2.1 Thermionic Emission

Thermionic emission is a major current transport process at the metal-semiconductor junction. Metal is a conductor of electricity and hence no diffusion current can flow from the metal as electrons are freely available for conduction in metal. Thermionic emission is a majority carrier current process which occurs at a junction when the electrons have energy high enough to exceed the barrier at the metal-semiconductor interface. Hence, thermionic current occurs only when the barrier height is low enough for sufficient electrons to jump across the barrier. The current density flow due to the thermionic emission is given by Eq. (2-8).

$$J = A^{*}T^{2}exp\left(-\frac{q\varphi_{B}}{kT}\right)\left[exp\left(\frac{qV}{kT}\right)-1\right] \tag{2-8}$$

A^{*} is the Richardson constant

$$A^{*} = \frac{4\pi qk^{2}m^{*}}{h^{3}} = 120\left(\frac{m^{*}}{m}\right)A/cm^{2}\cdot K^{2} \tag{2-9}$$

Where, V = applied voltage, T= absolute temperature, ϕ_B is the barrier height, m is the free electron mass, m* is the effective electron mass. This equation shows that as the barrier height increases, the current keeps reducing exponentially. The contact resistivity is given by Eq.(2-10).

$$\rho_{c} = \left(\frac{k_{B}}{qA^{*}T}\right)exp\left(\frac{q\varphi_{Bn}}{k_{B}T}\right) \tag{2-10}$$

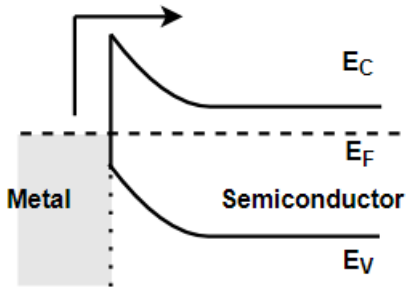

Fig. 2-6. Thermionic conduction mechanism.

2.2.2 Thermionic Field Emission

At medium doping cases, the conduction between metal and semiconductor takes place through partial thermionic and partial field emission between metal and semiconductor. Thermionic Field emission occurs when the electrons do not have enough energy to rise across the entire barrier and transfer from metal to semiconductors. The electrons have sufficient energy to rise to certain energy level where the depletion width is thin enough so that the electrons can tunnel through the barrier at that energy level. Hence, thermionic energy is utilized to raise the electrons to higher energy level and then tunneling takes place to conduct electrons from the metal to semiconductor. As this current transport process includes the combination of thermionic emission and tunneling, it is called thermionic field emission.

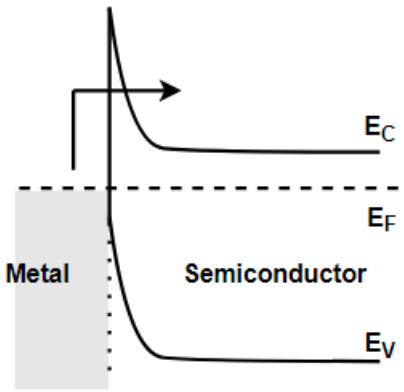

Fig. 2-7. Thermionic field conduction mechanism.

2.2.3 Field Emission

The field emission is the dominant current transfer phenomenon at the metal-semiconductor interface in a highly doped semiconductor. When the barrier between the metal and semiconductor is very thin, the current can tunnel from metal to semiconductor. The probability of the current tunneling depends on various factors like doping, barrier height. Tunneling phenomenon is caused mainly by the large electric field at the interfaces with a large barrier.

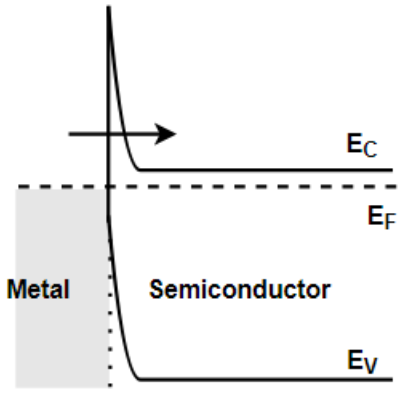

Fig. 2-8. Field emission conduction mechanism.

The contact resistivity or specific contact resistance for field emission process is given by [11]. It can be seen in the Eq. (2-12), that contact resistance depends inversely on the square root of doping concentration. Hence it proves that the contact resistance reduces as the doping of the semiconductor increases.

$$R_c \sim exp\left[\left(\frac{2\varphi_B}{\hbar}\right)\sqrt{\frac{\varepsilon_0 \varepsilon_s m^*}{N_D}}\right] \tag{2-11}$$

$$R_c \propto exp\left[\frac{K}{\sqrt{N_D}}\right] \tag{2-12}$$

The tunneling process is a quantum mechanical tunneling process which is a major current transport mechanism at the metal-semiconductor junction in highly doped semiconductors. This field emission called Fowler-Nordheim tunneling occurs when there is a huge electric field at the barrier. The tunneling current equation is derived based on the time-independent Schrodinger equation given by Eq. (2-13) where $\psi(x)$ is the potential wave function. WKB (Wigner, Kramers, Brillouin) Approximation is used for solving the equation to obtain the tunneling probability for a triangular barrier[22]. The tunneling probability of the electrons between metal and semiconductor is given by Θ which is given by Eq. (2-14).

$$\frac{\hbar^2}{2m^*}\cdot\frac{d^2\psi}{dx^2}+V(x)\psi=E\psi \tag{2-13}$$

$$\Theta = exp\left(-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_B^{3/2}}{\mathrm{E}}\right) \tag{2-14}$$

E- electric field is given by

$$\mathrm{E}=\frac{\varphi_B}{L}$$

The tunneling current is given by Eq. (2-15).

$$J_n = qv_R n\Theta \tag{2-15}$$

Θ is the tunneling probability, v_R is the Richardson velocity, n is the density of electrons.

2.3 Contact Resistivity

The quality of the metal-semiconductor interface is determined by the contact resistivity at the metal-semiconductor junction. This contact resistivity is highly important with regards to the performance of semiconductor when provided with an external connection. This contact resistivity is given by the Eq. (2-16).

$$\rho_c = R_{sh} * {L_t}^2 \tag{2-16}$$

The contact resistivity at metal-semiconductor interface under different current conduction mechanisms are shown in Eq. (2-17).

$$\rho_c = \begin{cases} \left(\frac{k_B}{qA^*T}\right) exp\left(\frac{q\varphi_{Bn}}{k_B T}\right) - TE \\ C_1\left(\frac{k_B}{qA^*T}\right) exp\left(\frac{q\varphi_B}{E_0}\right) - TFE \\ C_2\left(\frac{k_B}{qA^*T}\right) exp\left(\frac{q\varphi_B}{E_{00}}\right) - FE \end{cases} \quad (2\text{-}17)$$

Where,

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{K_s \varepsilon_0 m^*_{tun}}}$$

$$E_0 = E_{00} coth\left(\frac{E_{00}}{k_B T}\right) \quad (2\text{-}18)$$

$$C_1, C_2 = f(N_D, T, \varphi_B)$$

It can be seen that the contact resistivity during the thermionic field emission depends on energy E_0 which is a function of E_{00}. The simplified contact resistivity in case of field emission is given by E_{00} which depends inversely on doping concentration. Hence, at higher doping cases, field emission reduces the contact resistivity.

2.4 Transfer Length Method (TLM)

TLM (transfer length method) method is based on the variation of Total Resistance vs. Spacing between the contacts. The basic metal-semiconductor interface could be represented as equivalent resistance model as shown in the Fig. 2-10. In-order to obtain the relationship between the total resistance and spacing between the metal contacts, the lateral device structure with metal is studied first. The same concept is projected to the vertical structure of the device where the voltage is applied across the semiconductor between the top and the bottom metal electrode. The thickness of the semiconductor layer is varied to obtain different spacing between the contacts and further obtain a TLM plot. The structure and equivalent resistance model of the vertical device are shown in Fig. 2-11.

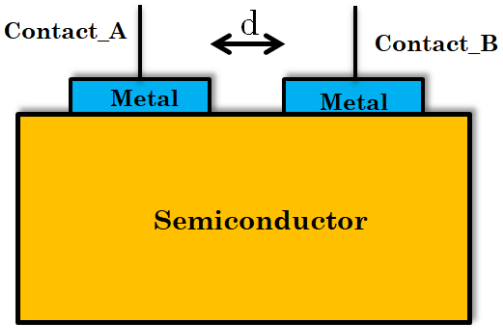

Fig. 2-9. Metal-semiconductor contact in simpler case.

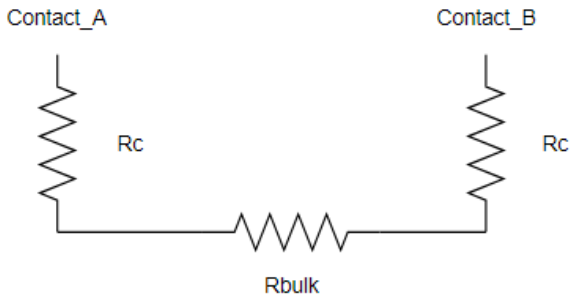

Fig. 2-10. Equivalent resistance based model of the structure.

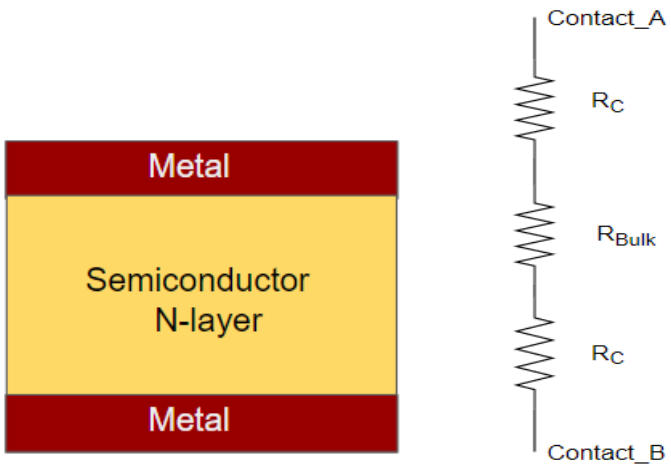

Fig. 2-11. Vertical semiconductor structure and equivalent resistance model.

The total resistance between the contacts A and B can be written as

$$R_T = 2R_C + R_{bulk} \tag{2-19}$$

R_c is the contact resistance at the interface of metal-semiconductor. R_{bulk} is the semiconductor resistance offered by the bulk of the device. The bulk resistance of the semiconductor can be written in terms of sheet resistivity as Eq. (2-20).

$$R_{bulk} = \rho_s * d/Z \tag{2-20}$$

Where ρ_s is the sheet resistivity, d is the spacing between the metal contacts (in lateral structure), Z is the thickness of the semiconductor where the current flow. The total resistance can be written as Eq. (2-21).

$$R_T = 2R_C + \frac{\rho_s}{Z} d \tag{2-21}$$

Hence, the total resistance can be plotted as a function of spacing (d). It has an intercept of twice the contact resistance while slope represents the bulk resistivity. The plot R_T vs. d is obtained as shown in the Fig. 2-12.

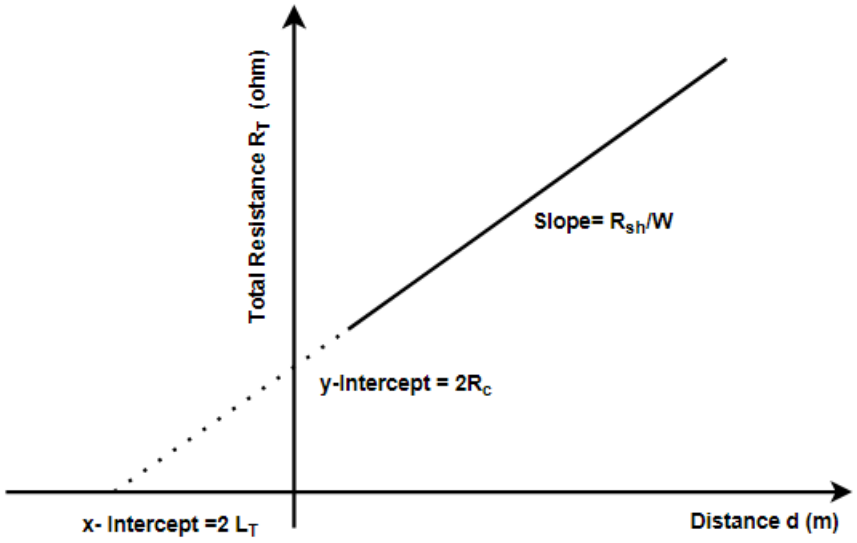

Fig. 2-12. TLM plot of R_T vs. d.

The parameter extracted from the x-intercept of TLM plot is a characteristic contact parameter called transfer length. Transfer length is defined as the effective length needed for the current to transfer from the metal to semiconductor. When a voltage is applied across the metal contacts fabricated on top of semiconductor, the current does not take the entire cross section to enter the semiconductor from the metal. It takes a very small fraction to enter the semiconductor from the metal which is called the transfer length. This transfer length plays a major factor in determining the contact resistivity at the metal-semiconductor interface.

2.4.1 Linear TLM (L-TLM)

The linear structure of TLM as seen from the top-view of metal-semiconductor interface is seen in the Fig. 2-13.

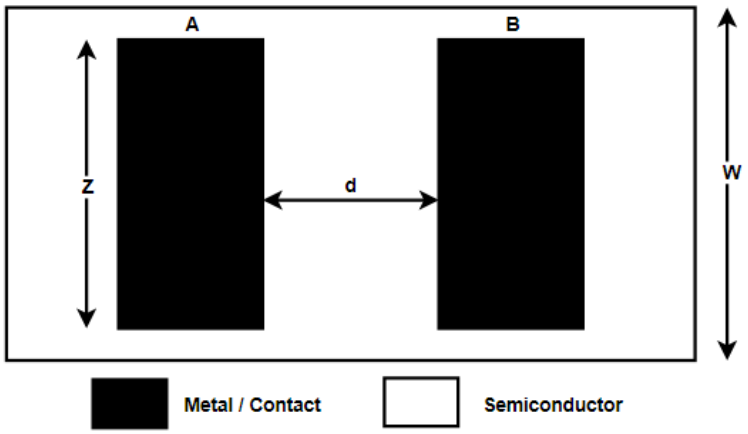

Fig. 2-13. Simple LTLM structure (top-view).

Z is defined as the dimension of the metal deposited on the semiconductor while W is the actual dimension of the semiconductor. The TLM mask in case of LTLM is shown in Fig. 2-14. It can be seen that the spacing between the metal contacts is gradually increased. The current is applied between two consequent metal contacts and voltage drop is measured across the contacts. I-V curves are plotted to obtain the total resistance between the metal contacts.

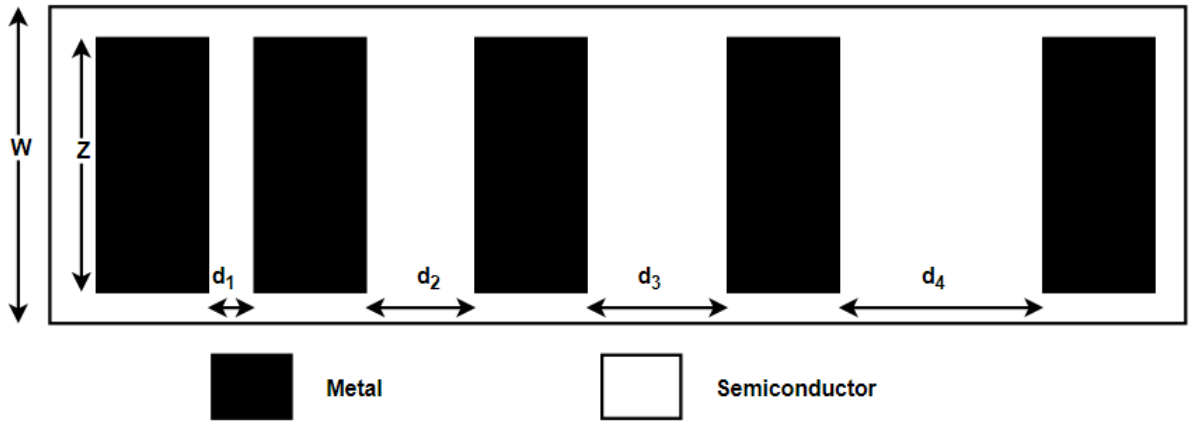

Fig. 2-14. Linear TLM mask deposited on the layer under consideration.

One main assumption with the LTLM is that the metal contact length is much more than the transfer length of the devices. Also, $\delta = W - Z$ is very small compared to Z.

$$V(x) = \frac{I\sqrt{R_{sh}\rho_c}\cdot\cosh\left[L - x/L_T\right]}{Z\sinh\left(L/L_T\right)} \tag{2-22}$$

Where V(x)- Voltage as a function of distance. L = rectangular contact pad length; Z= contact width; I= current flowing into the contact

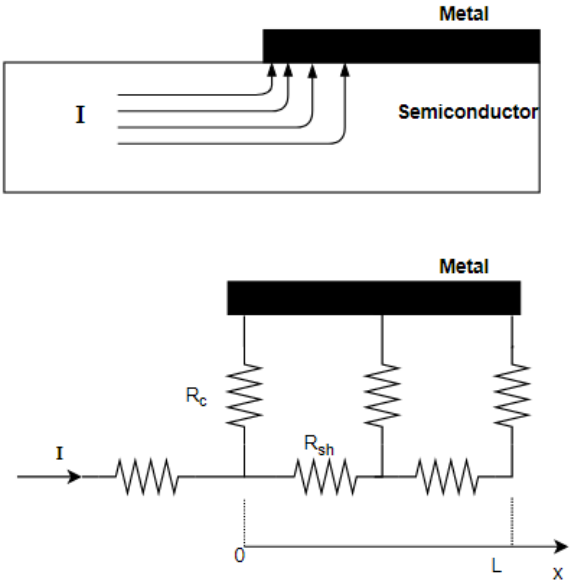

Fig. 2-15. M-S interface with current contours and equivalent resistance model.

The sharp corners in metals could lead to current crowding when current is applied between two metal contacts. It is highly essential to provide electrical isolation between the metal contacts as currents could instead flow through surface instead of flowing through the bulk of the semiconductor leading to incorrect results.

2.4.2 Circular TLM (C-TLM)

Circular TLM has metals deposited on the semiconductor with circular gap or spacing between the metal contacts. This annular spacing between metal contacts provides isolation by default and does not require the additional etching process as required by LTLM. These circular spacing between the metal contacts ensures that the spacing between the metal contacts remains the same irrespective of the mutual spacing of the metal electrodes for measuring the voltage drop. The Circular TLM structure is shown Fig. 2-16.

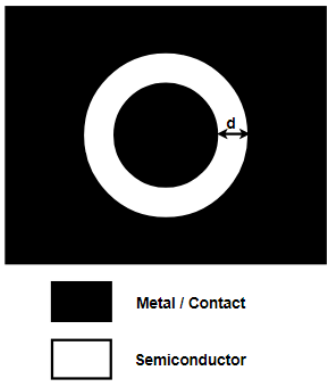

Fig. 2-16. Simple CTLM structure.

The equation of Circular TLM is obtained using Marlow and Das pattern[23]. The equation for CTLM is derived in detail in Appendix A: Derivation of Equation of CTLM and Correction Factor. Various parameters used in this derivation are listed as follows.

ρ_c- specific contact resistivity

Rsk – beneath sheet resistance

x- radius of a contact element of width dx.

V(x) – voltage drop across contact interface at x

The simplified equation for the CTLM is given in as Eq. (2-23).

$$\nabla^2 V - k^2 \cdot V = 0 \tag{2-23}$$

Where,

$$k^2 = \frac{1}{{L_t}^2} = \frac{R_{sh}}{\rho_c} \tag{2-24}$$

$$L_t = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{2-25}$$

The parameter transfer length is defined as the square root of contact resistance per sheet resistance. The transfer length is the effective length which more than 63% of current transfers from metal to semiconductor or semiconductor to metal. The solution to this equation under the condition that the inner radius (r_1) of the concentric circle of CTLM is much larger compared to spacing is given by Eq. (2-26). This equation looks similar to the total resistance from LTLM.

$$R_T = \frac{R_{sh}}{Z}[d + 2L_T] \tag{2-26}$$
$$Z = 2\pi r_1$$

The assumption of spacing being much larger than the radius of the inner circle may not be true for all conditions. Hence, we introduce a correction factor that could be applied in cases where the assumption becomes invalid. Derivation of the correction factor for CTLM is as follows[24].

$$R_T = \frac{R_{sh}}{2\pi}\left[ln\frac{r_1 + d}{r_1} + L_T\left(\frac{1}{r_1 + d} + \frac{1}{r_1}\right)\right] \tag{2-27}$$

$$R_T = \frac{R_{sh}}{2\pi r_1}[d + 2L_T] \cdot C \tag{2-28}$$

$$C = \frac{r_1}{d} \cdot ln\frac{r_1 + d}{r_1} \tag{2-29}$$

The Fig. 2-17 shows the effect of the correction factor on TLM plot of (R_T vs d). When the correction factor is avoided, the line is not linear and trying to fit these points on a straight line could skew the results extracted from the plot. The corrected data plot gives a good straight line with well-fit points which show that the importance of correction factor in the extraction of parameters.

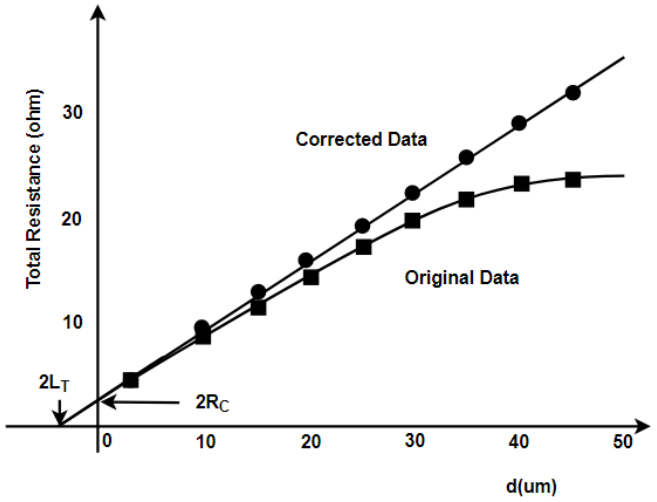

Fig. 2-17. Effect of Correction Factor in TLM Fit [25].

2.4.3 Comparison of LTLM vs. CTLM

The advantages and disadvantages of LTLM and CTLM are compared in TABLE 2-2.

TABLE 2-2. Pros and Cons of LTLM and CTLM.

	LTLM	**CTLM**
Pros	Simpler Mask Design	Isolation created due to the mesa structure
	no correction factors involved	No current crowding or lateral current flows
Cons	When Z<W, lateral currents can flow on semiconductor surface and current crowding can occur at edges of metal deposited	Correction factor needs to be considered while TLM plot (Total Resistance Vs. Spacing)
	Additional mesa etching step is highly essential during fabrication of TLM structure to provide isolation between deposited metal contacts	

2.5 Effect of substrate on Contact resistivity

Presence of substrate under the actual semiconductor layer is inevitable due to various reasons. The bulk of Gallium Nitride is very expensive which leads to the use of sapphire or silicon as the bulk layer. Foreign bulk layers create the presence of intermediate layers in between bulk and semiconductor layer to avoid the dislocation densities or irregular growth of the semiconductor on the actual semiconductor layer under consideration. The basic structure of the device with substrate layer below it is shown in the Fig. 2-18. The equivalent resistor structure is given in Fig. 2-19.

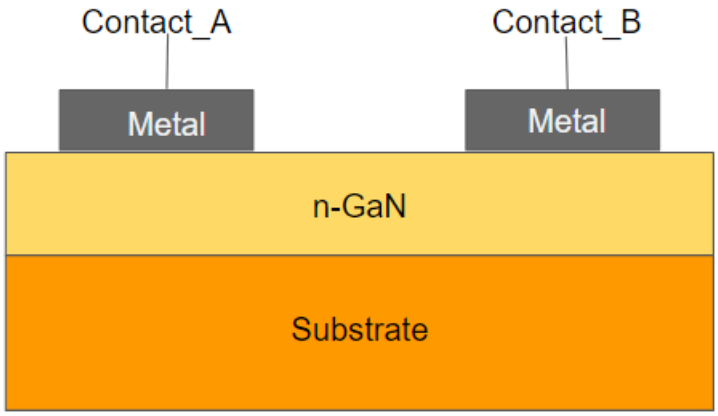

Fig. 2-18. Structure of the device with the Substrate layer below it.

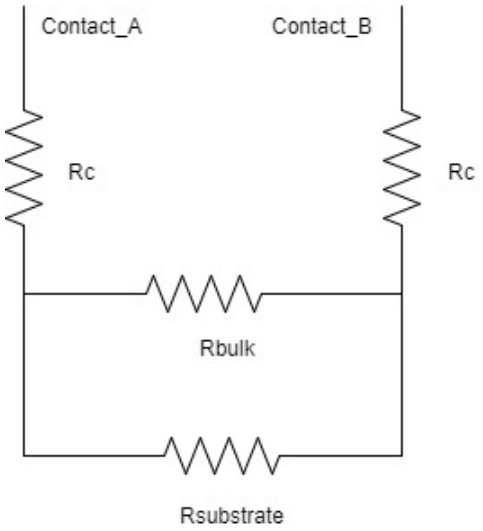

Fig. 2-19. Equivalent Resistor model for the semiconductor-substrate with the metal layer.

The equivalent of the semiconductor layer resistance is given by the R_{bulk} while the substrate resistance is given by $R_{substrate}$. If the resistance of the bulk layer is comparable to the resistance of the substrate, then it contributes significantly to the slope of the obtained TLM figure. Hence, substrate resistance contribution should be taken into consideration. The contact resistance is still the resistance contribution of the metal-semiconductor interface.

$$R_T = 2R_C + R_{bulk\_eff} \tag{2-30}$$

$$R_{bulk\_eff} = R_{bulk} || R_{substrate} \tag{2-31}$$

The contribution from the resistance from the substrate can be avoided only in the cases when the substrate is insulating, or it is huge resistance material that could avoid any current flow through it.

2.6 Effect of Heavily doped layer on Contact resistivity

A heavily doped layer between metal and semiconductor layer causes the lowering of the conduction band Energy diagram as shown in Fig. 2-20.

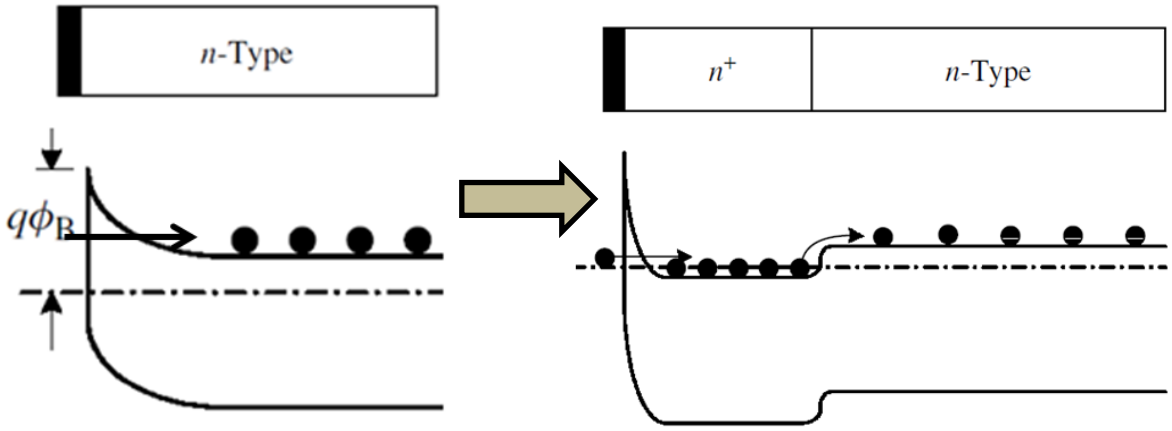

Fig. 2-20. Effect of a Heavily doped semiconductor layer on energy band diagram at M-S interface[25].

The tunneling barrier becomes thin which leads to the tunneling of more electrons through metal-semiconductor. This excessive current flow at M-S junction leads to lower contact resistance. The heavily doped layer at the interface would make the contact modified ohmic contact whose IV curve looks like Fig. 2-21.[22]

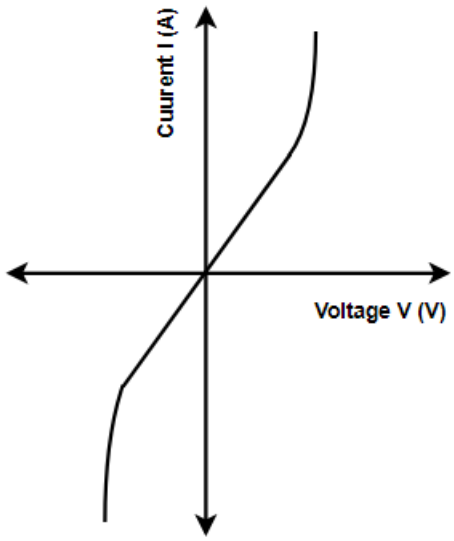

Fig. 2-21. Modified IV curve due to $n^{+}n$ layer.

3 Basics of Simulation in Sentaurus

Simulation of semiconductor devices before actual growth and fabrication has various advantages in terms of saving time and cost involved. Modeling of the devices gives a perspective into the possible errors that could occur after the device is grown. For materials like GaN which are very expensive, modeling provides an opportunity to implement numerous ideas which a researcher gets and verify the validity of the ideas. Device simulation is highly essential in aiding designers to optimize device designs before putting into production

Sentaurus Technology Computer Aided Design (TCAD) software package is provided by Synopsys, Inc. Sentaurus allows simulation of a variety of semiconductors like Si, SiC, GaAs, GaN, insulators like SiO_2, metals and various other materials. The simulations can be performed in 1D, 2D or 3D. This software can provide electrical, thermal, and optical characteristics of the device.

3.1 Simulation Outline

Sentaurus has a different set of tools for various purposes. Various tools provided by Sentaurus that are used in my simulations are

1. Sentaurus Structure Editor
2. Sentaurus Mesh
3. Sentaurus Device
4. Sentaurus Visual

Sentaurus Workbench (SWB) is the framework offered by Synopsys which provides easier access to tools provided by Sentaurus. It is the user interface screen where input commands could be provided to various tools and enable automatic simulation groups. This screen which is shown in Fig. 3-1 also provides an opportunity to vary the value of the parameters used in the simulation tools. SWB also provides a list of example files provided by Synopsys for user reference.

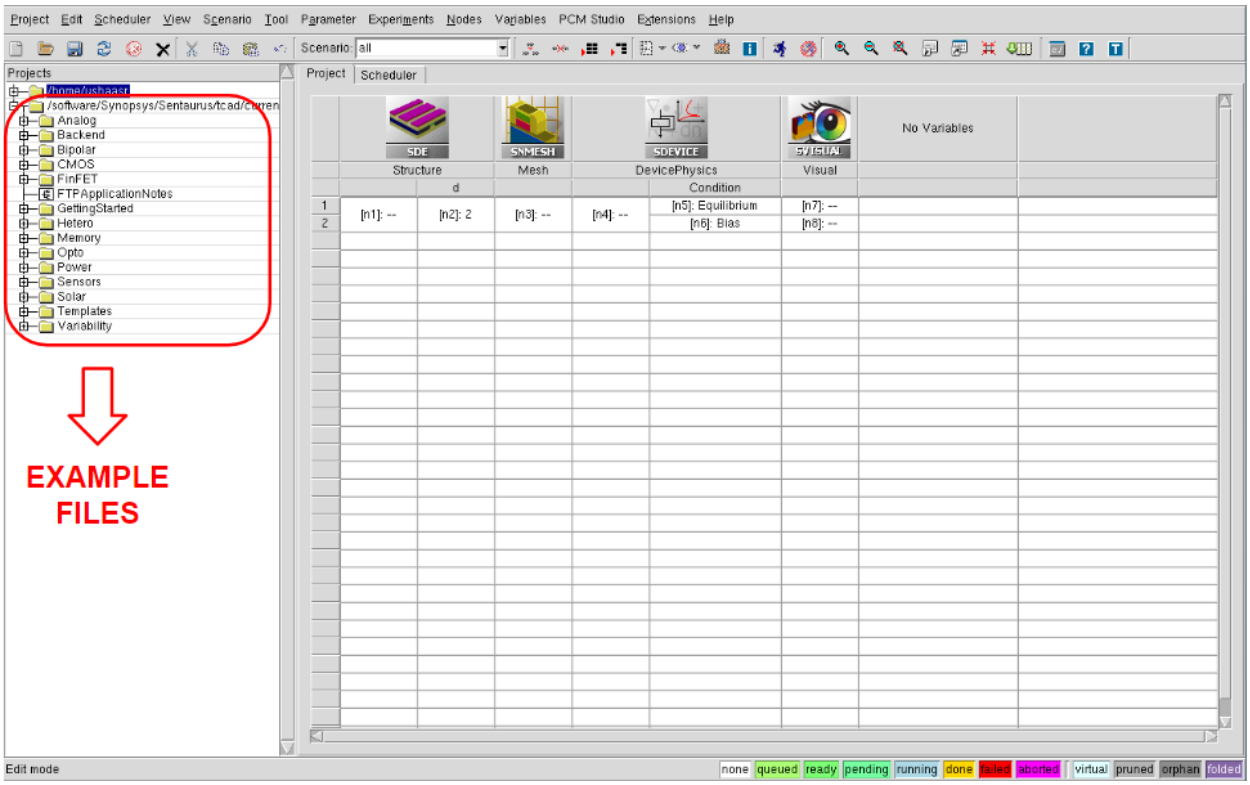

Fig. 3-1 Sentaurus Workbench View.

3.1.1 Sentaurus Structure Editor

Sentaurus Structure Editor (SSE) [26] is the first tool used in the course of simulation where the basic geometry of the device is defined. SSE can be used as a command-based input file or boundary file where the device can be constructed using drop down options. SSE includes the doping profile of the device, location of the metal contacts. This tool also offers the option to define the mesh of the device instead of using the separate mesh tool.

3.1.2 Sentaurus Mesh

The mesh definition is highly important in any software simulation as it defines the accuracy of the simulation results. Thinner mesh is needed in areas where there is a possibility of abrupt variation of electrical parameters like the interface of metal–semiconductor or at the interface of any two layers. At the same time, thinner meshes means that the basic equations are solved at lot more points than the case of denser meshes which means that the simulation time is much more

in case of thinner meshes. Hence, the size of the mesh is defined based on the tradeoff between the time taken for simulation and the need for thinner mesh. Thin meshes are defined at the metal–semiconductor interface and the region between the metal contacts in lateral device simulations.

3.1.3 Sentaurus Device

Sentaurus Device [27] is the heart of the entire simulation as it defines the major parameters of the device like physics inside the device, contact conditions, ramping conditions for the electrical study of the device, and for defining of the parameter of materials. It consists of various sections namely File, Electrode, Physics, Math, Solve, plot section. It also includes Parameter file.

File – This provides an option to list out the required input and output files of the simulations. It provides the option of declaring the mixed circuit simulation files, newton plots to study in case of errors, and various other plot and parameter files.

Electrode – This section allows the user to define the contact type (Ohmic or Schottky), initial voltage conditions, and resistance at the contacts. It also allows the option to define the barrier height in case of Schottky contacts.

Physics – This is the segment where the physics inside the bulk or the interfaces are initiated. The various physics that were included in the simulation were mobility models, recombination models, tunneling, thermionic current, trapping in devices. The major concern for the metal-semiconductor junction current is given by thermionic and tunneling current at the interface of M-S which is dealt in detail in the upcoming sections.

Math- Sentaurus solves the transport equations in an iterative manner to obtain the intended electrical conditions. Math section defines the number of iterations, convergence error limits, and the degree of accuracy of simulations.

Solve- This section is responsible for defining the equations that need to be solved in the devices along with the ramping conditions of the electrical quantities. The equations used in the simulations are Poisson equations for electrons and holes. The Poisson equation is solved for the electrostatic potential.

Plot – Here is where the list of the solution variables that need to be saved to an output file is specified. The solution variables include the electric field, electrostatic potential, Mobility, current density, tunneling, etc.

Parameter File – This file is defined in SD which includes the parameter definition for materials which are not available by default in Sentaurus. The parameter file includes the parameter values of various specifications related to the material used in the simulation. The excitation energy of the impurities can also be defined in the parameter file. The parameter file for Gallium Nitride is given in Appendix B [28].

3.1.4 Sentaurus Visual

Sentaurus Visual [29] is an important part of the simulation as it helps in visualizing the device. It can be used to view the characteristics and various parameters of the device like electric field, current density contours. The Sentaurus visual figures provide a good insight into the operation of the device. I-V characteristics obtained from Visual are used majorly in the TLM parameter extraction in the research work. Sentaurus Visual also has an option to extract parameters from the plots like small-signal resistance, conductance, threshold voltage, etc.

3.2 Physics involved in Sentaurus

Sentaurus gives the flexibility to define the physics inside the device of the semiconductor. The Poisson equations are the basic equations for semiconductor modeling. These equations are derived from the Boltzmann transport equation. The electrostatic potential is solved using Poisson equation which is given by Eq. (3-1).

$$\nabla \cdot \left(\varepsilon \nabla \varphi + \vec{P}\right) = -q(p - n + N_D - N_A) - \rho_{trap} \tag{3-1}$$

Where ε is the electrical permittivity, $\vec{P}$ is the ferroelectric polarization, *n* and *p* are the electron and hole densities, N_D is the donor concentration, N_A is the acceptor concentration and $\rho_{trap}$is the charge density contributed by traps and fixed charges. Polarization effect can be neglected in the simulations as we do not consider the effect of polarization for the metal-semiconductor interface.

Sentaurus provides different current transport models [27] namely Drift-Diffusion model, Thermodynamics, Hydrodynamics, and Monte-Carlo. The transport models are written in the form of continuity equation shown in Eq. (3-2) and Eq. (3-3).

$$\nabla \overrightarrow{J_n} = qR_{net,n} + q\frac{\partial n}{\partial t} \tag{3-2}$$

$$-\nabla \overrightarrow{J_p} = qR_{net,p} + q\frac{\partial p}{\partial t} \tag{3-3}$$

$R_{net,n}, R_{net,p}$ are the electron and hole net recombination rate. $\overrightarrow{J_n}$, $\overrightarrow{J_p}$ are the electron and hole current density. N and p are the electron and hole density respectively.

By default, Sentaurus uses drift-diffusion model as the current transport model. Drift-Diffusion model consists of current due to two components namely drift and diffusion. The basic current density equation can be written in terms of drift and diffusion terms are shown in Eq. (3-4) and Eq. (3-5).

$$\overrightarrow{J_n} = -qn\mu_n \vec{\nabla}\varphi + qD_n \vec{\nabla} n \tag{3-4}$$

$$\overrightarrow{J_p} = -qp\mu_p \vec{\nabla}\varphi - qpD_p \vec{\nabla} p \tag{3-5}$$

The current density equations for electrons and holes are modified by Sentaurus to provide a more accurate version which is given by Eq. (3-6) and Eq. (3-7).

$$\overrightarrow{J_n} = \mu_n(n\nabla E_c - 1.5nkT\nabla ln m_n) + D_n(\nabla n - n\nabla ln\, \gamma_n) \tag{3-6}$$

$$\overrightarrow{J_p} = \mu_p(\mathrm{p}\nabla E_v - 1.5pkT\nabla lnm_p) + D_p(\nabla p - p\nabla ln\,\gamma_p) \quad (3\text{-}7)$$

Where, μ_n, μ_p are mobility of electrons and holes respectively; m_n, m_p are the effective mass of electron and holes; γ represents the Boltzmann statistics. Diffusion constants are given by Eq. (3-8).

$$D_n = kT\mu_n;\ D_p = kT\mu_p \quad (3\text{-}8)$$

3.2.1 Mobility dependence on Doping

Sentaurus offers different mobility models based on doping namely, Masetti, Arora and various other combinations. The mobility model used for the simulation purposes is the default model of Masetti. The mobility dependent on doping is given by the Eq. (3-9). The equation consists of various parameters likeμ_{min1}, μ_{min2}, μ_1, P_c, C_r are defined for the material GaN in the parameter file.

$$\mu_{dop} = \mu_{min1}exp\left(-\frac{P_c}{N_{A,0}+N_{D,0}}\right) + \frac{\mu_{const}-\mu_{min2}}{1+\left(\left(N_{A,0}+N_{D,0}\right)/C_r\right)^{\alpha}} - \frac{\mu_1}{1+\left(C_s/\left(N_{A,0}+N_{D,0}\right)\right)^{\beta}} \quad (3\text{-}9)$$

3.2.2 Tunneling

Since the metal-semiconductor contact resistance depends hugely on the tunneling phenomenon, it is important to completely understand the tunneling as defined by Sentaurus to make use of it as much as it can be close to reality.

Sentaurus sees tunneling through models called NLM (non-local models) which defines various tunneling parameters. The NLM models can be defined based on region or material defined in the device or it can be defined based on the reference surface. These NLM models are the most versatile tunneling models which can handle tunneling through Schottky contacts or hetero-structures and gate leakage through insulators.

The tunneling model is based on WKB Tunneling which is based on the computation of position and energy based on WKB approximation and further obtains the tunneling probability. This

probability is used to further compute the electrons that could flow between the barrier and further compute the current that could flow.

NLM models offer the option to decide the various parameters like length till which tunneling can take place, the interface where the tunneling needs to be considered, permeation length which defines the length till which the non-local lines need to be defined to check the probability of tunneling to occur.

3.2.3 Thermionic Emission Current

The current transport process at a hetero-junction is dominated by the thermionic current instead of typical drift and diffusion. It is defined with keyword Thermionic in the physics definition at the interface of metal and semiconductor. When there is a hetero-interface between two materials (say 1 and 2), the current density is given by Eq. (3-10) and Eq. (3-11).

$$J_n = a_n q \left[v_{n,2} n_2 - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 exp\left(-\frac{E_c}{kT}\right) \right] \tag{3-10}$$

$$v_{n,i} = \sqrt{\frac{kT}{2\pi m_{n,i}}} \tag{3-11}$$

Where, $v_{n,i}$ – emission velocity in material i, m is the effective mass of electrons.

4 Results and Discussions

This chapter deals with the simulations results and testing results conducted by me during the course of this research work. The simulations are performed in Sentaurus TCAD provided by Synopsys, Inc. The Gallium Nitride (GaN) based simulations were implemented to get a better understanding of the electrical properties internal to the devices which could help improve the performance of the semiconductor. The simulations are used to obtain the IV characteristics of the device. This data is further analyzed using MATLAB and Excel. The n-GaN samples grown at Virginia Tech are tested using Keithley 2400 source meter and four-point auto-prober setup. The IV characteristics of the samples are analyzed using the LabView and Excel.

4.1 Sentaurus Simulation Vertical Structure

The simulations are started with a simple vertical device structure with metal on top and bottom of the semiconductor device. The vertical device structure is shown in Fig. 4-1. The dimensions of the structure are listed in TABLE 4-1. The mesh inside the device is shown in Fig. 4-2. The interface between metal and semiconductor is the major region of interest. Hence, a very minute mesh is defined at the interface which is shown in Fig. 4-2. The size of the mesh is a major determining factor in simulations. Finer mesh provides accurate results but takes a long simulation time. Hence, the size of the mesh is determined by the tradeoff between the simulation time and simulation accuracy.

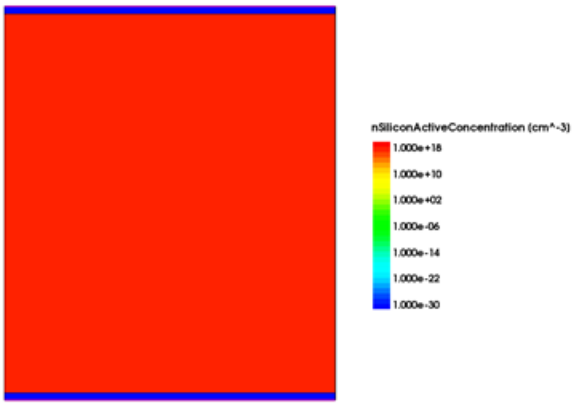

Fig. 4-1. Vertical Structure of the n-GaN device.

TABLE 4-1. Dimension of vertical n-GaN.

Doping (cm^{-3})	1e18
X	4 um
Thickness	5,9,13,17,21,25 um

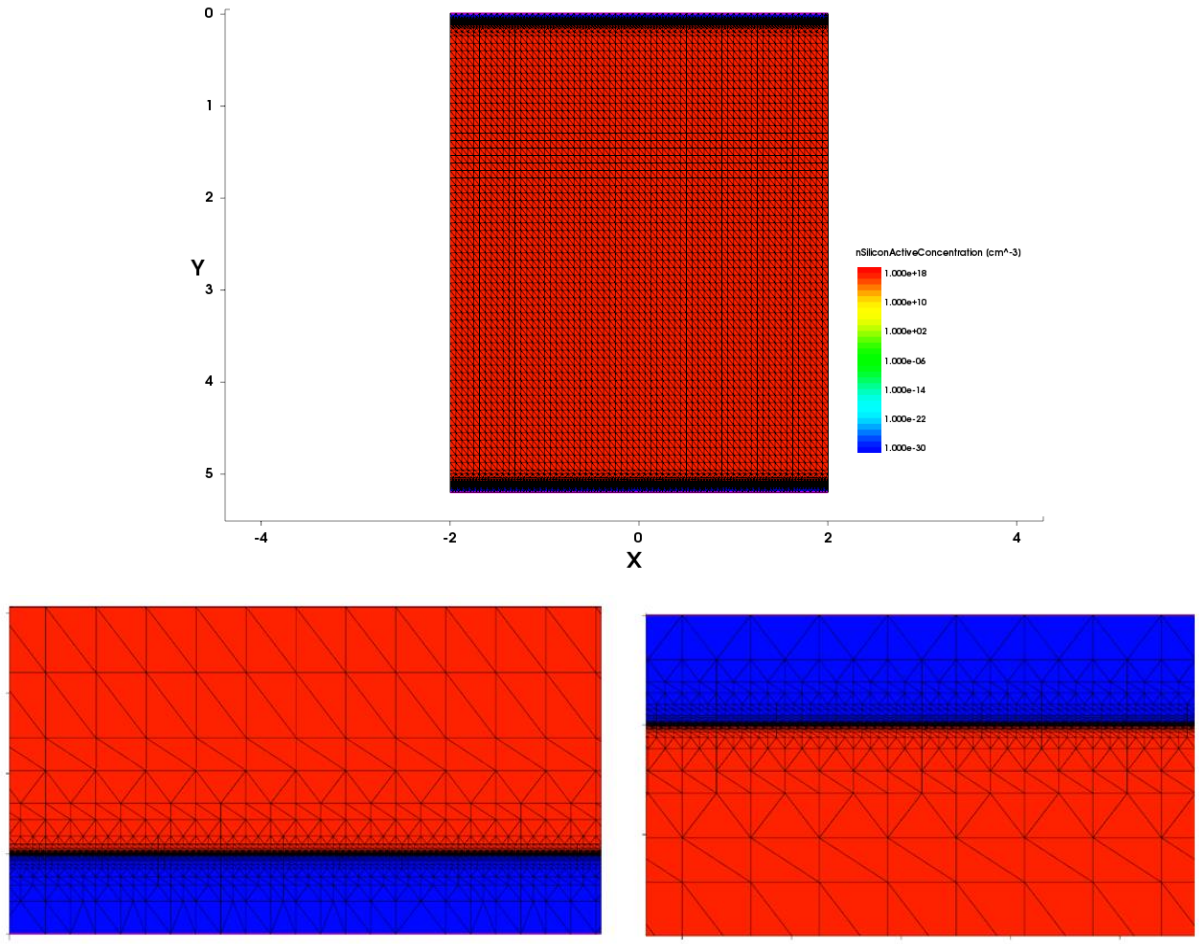

Fig. 4-2. n-GaN device with mesh defined inside metal and GaN along with zoomed version at interfaces.

4.1.1 Basic vertical GaN simulation

The TLM pattern is obtained by plotting the IV curves by plotting the total resistance vs. spacing between the metal contacts. In a vertical GaN structure, as the metal contacts are present on either side of the semiconductor, the thickness of the semiconductor is varied in terms of 5,

9,13,17,21 and 25um. These different well spread thickness values are used to obtain the total resistance points to obtain the TLM plot. The IV characteristic of the sample is shown in Fig. 4-4. The energy band-diagram for the vertical semiconductor with a metal of work-function of 4.3 is shown in Fig. 4-3.

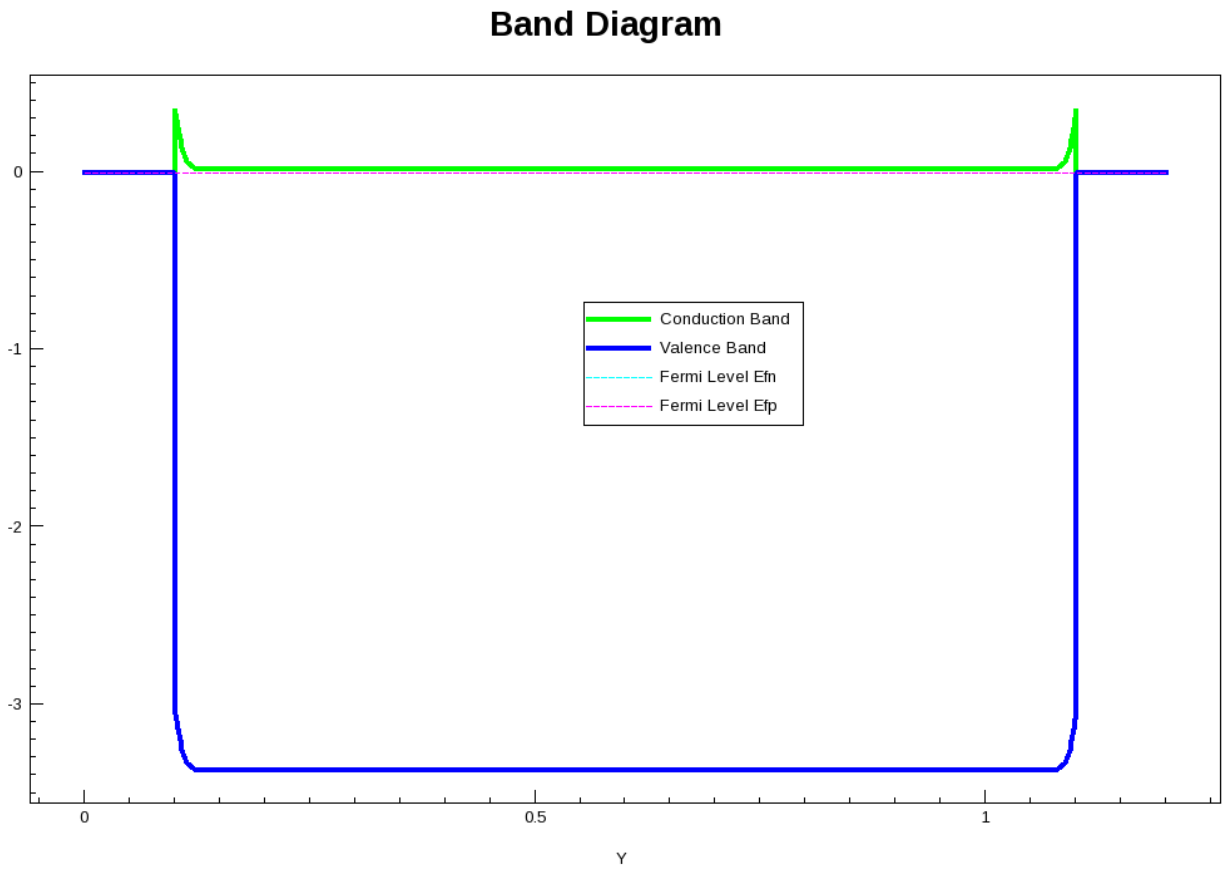

Fig. 4-3. Energy Band Diagram of Vertical n-GaN with metal work-function 4.3.

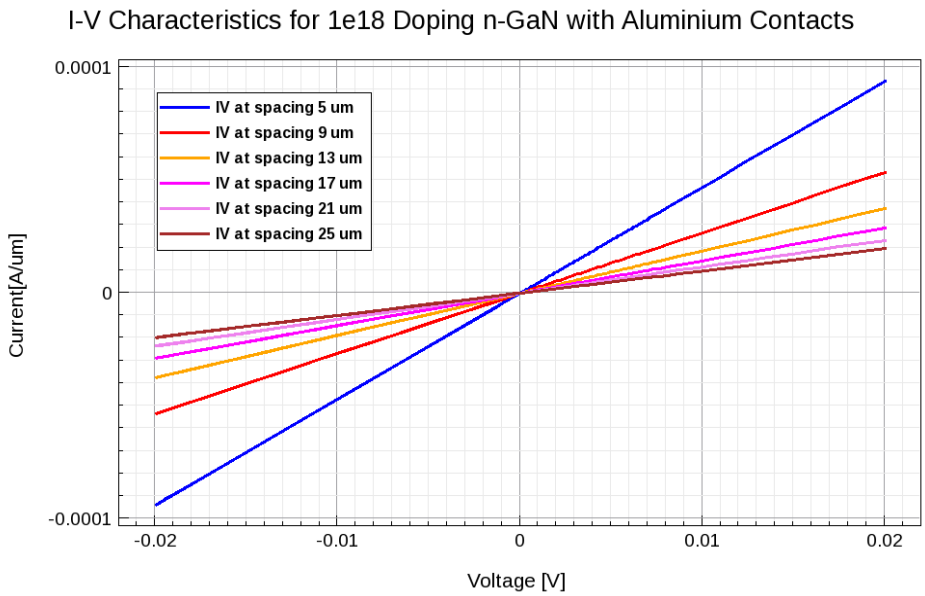

Fig. 4-4. IV characteristics of 1e18 n-GaN with Al contacts.

I-V characteristics of the n-type GaN with a metal having work-function of 4.5 and variable n doping are shown in Fig. 4-5. As, the doping increases, the Schottky metal contact becomes an ohmic contact. The specific resistance for various doping conditions for metal with work-function of 4.5 is shown in TABLE 4-2. It can be noticed that the specific resistance keeps reducing on increasing the doping of n-type GaN. As the doping of semiconductor keeps increasing, the tunneling probability keeps increasing and current flows from metal to semiconductor through field emission. Hence, reduced specific resistance is observed with doping increase.

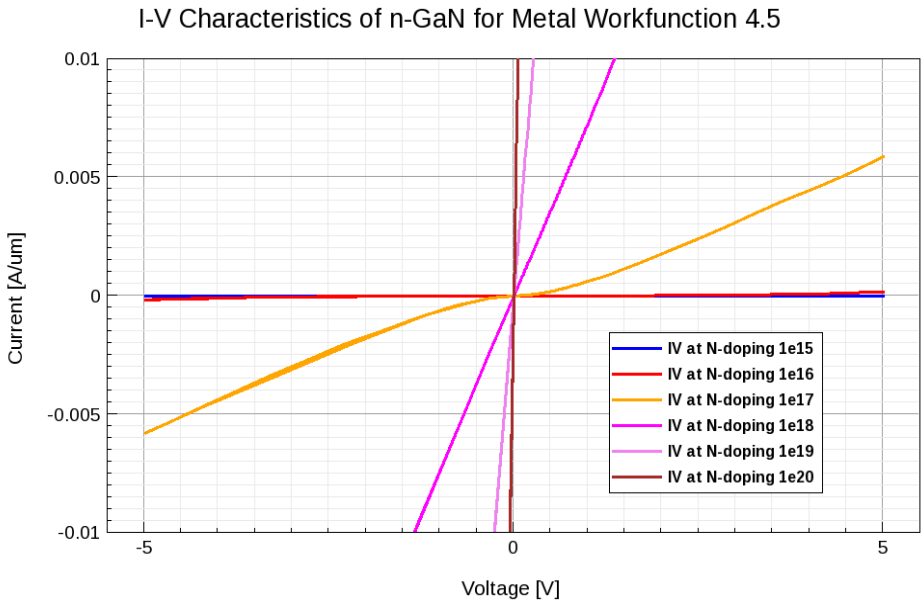

Fig. 4-5. IV characteristics of n-GaN with metal work-function 4.5.

TABLE 4-2. Specific Resistance of vertical n-GaN under different doping.

Doping	Specific Resistance (Ω-cm^2)
1e15	2679701.365
1e16	120753.600
1e17	1011.577
1e18	133.955
1e19	26.375
1e20	5.366

4.1.2 TLM extraction and validation

The TLM plot is the R_T vs. d is obtained by first obtaining the various TLM points (Resistances for each spacing condition) is shown in TABLE 4-3. The TLM plot is shown in Fig. 4-6.

TABLE 4-3. Total Resistance of vertical n-GaN under different spacing.

Spacing (um)	Total Resistance (Ω)
5	853.147
9	1496.107
13	2138.704
17	2777.722
21	3418.652
25	4066.661

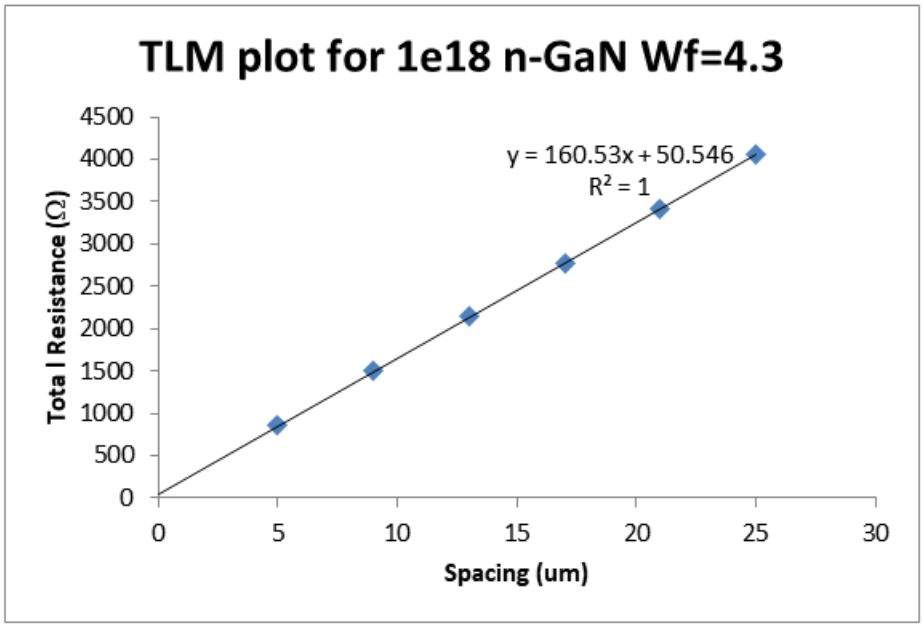

Fig. 4-6. TLM plot for n-GaN of 1e18 with metal work-function 4.3.

The parameters can be extracted from the linear fit of the points in TLM plot. The y-intercept gives the contact resistance. The slope represents the sheet resistance per unit width of the device. The calculated value of sheet resistance can be verified using hand calculation using the formula given in Eq. (4-1). The parameters extracted for the doping of 1e18 for mobility of 389 cm^2/V-s. The extracted parameters are listed in TABLE 4-4. Since the simulated structure is vertical, the concept of transfer length does not play a role here as current tends to occupy the entire cross section to flow between the metal contacts.

$$\rho = \frac{1}{q\mu N_d} \tag{4-1}$$

TABLE 4-4. Extracted Parameters from TLM plot.

Contact Resistance (Ω)	25.273
Sheet Resistance (Ω)	160.53
Bulk Resistivity (Ω-cm)	0.016046
Calculated Bulk Resistivity (Ω-cm)	0.016053

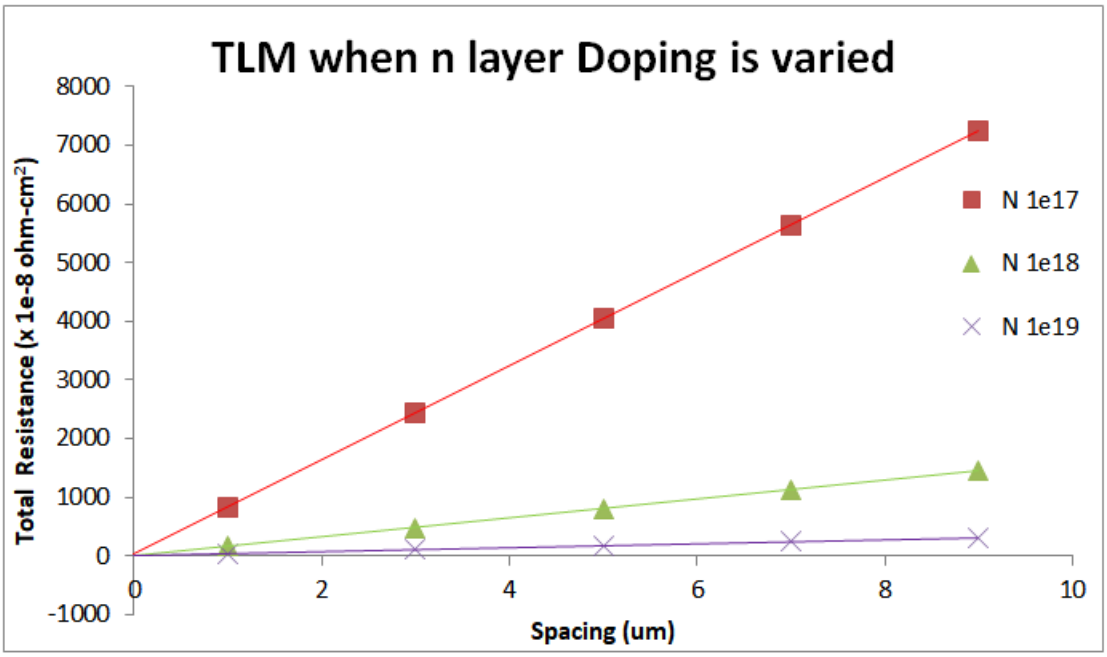

Fig. 4-7.TLM plot when n-GaN doping varied as 1e17, 1e18, and 1e19.

4.1.3 TLM simulation for different metal barrier height

The increase in metal work-function above the electron affinity leads to increase in barrier height at the metal-semiconductor interface. Hence, as the metal on n-GaN increases above 4.2, barrier height increases. As the barrier height increases, the metal contact becomes schottky as it becomes difficult for the current to flow across the barrier. Hence, IV curves become schottky curves as the barrier height increases. The conversion of ohmic IV curves into schottky curves can be seen in Fig. 4-8.

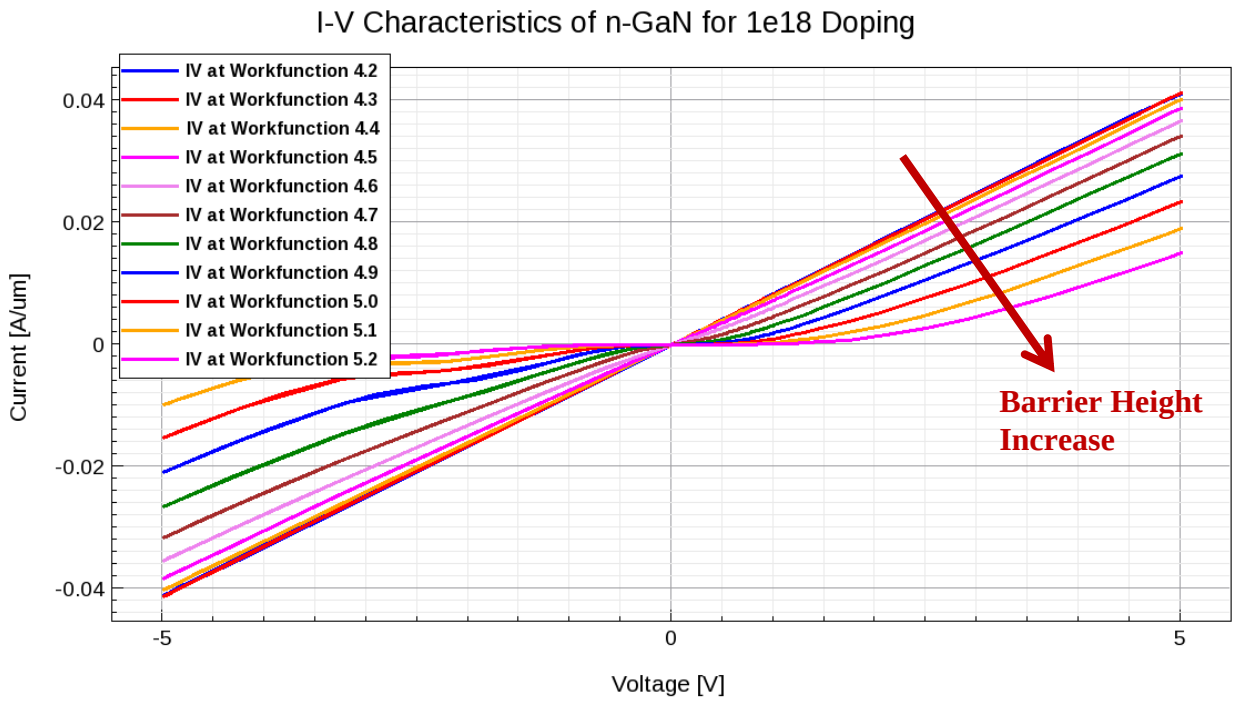

Fig. 4-8. IV characteristics of n-GaN in contact with metals of different work-functions.

4.2 Lateral Semiconductor structure

Most of the practical devices are in the lateral structure. The basic lateral structure is very large with small contacts on top of the semiconductor. The basic structure of the lateral device is shown in Fig. 4-9. The structural dimensions of the device are shown in TABLE 4-5.

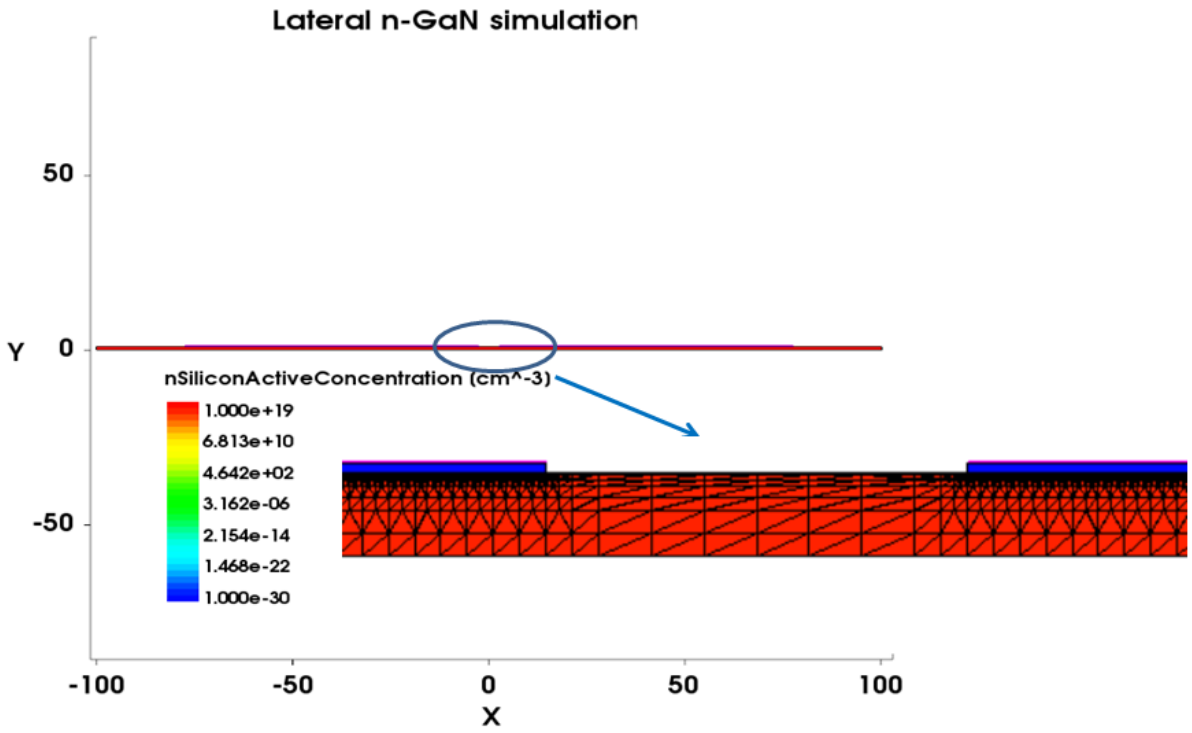

Fig. 4-9. Structure of lateral n-GaN structure.

TABLE 4-5. Lateral n-GaN dimensions and specifications.

X	200
Metal Thickness	100nm
Semiconductor Thickness	1um
Metal Contact length	75 um
N doping (cm^{-3})	1e19
Spacing between Contacts (um)	5,9,13,17,21,25
Metal Work-function	4.3 (Ti/Al/Ni/Ag)

4.2.1 Basic GaN simulation

Basic simulation of a lateral n-GaN device of 1e19 cm^{-3} doping is conducted. Linear IV characteristics are observed as the doping is high and barrier height is very less (Work-

function=4.3). The IV characteristics for different spacing are shown in Fig. 4-10. The contact resistances for different doping conditions and various spacing are listed in TABLE 4-6.

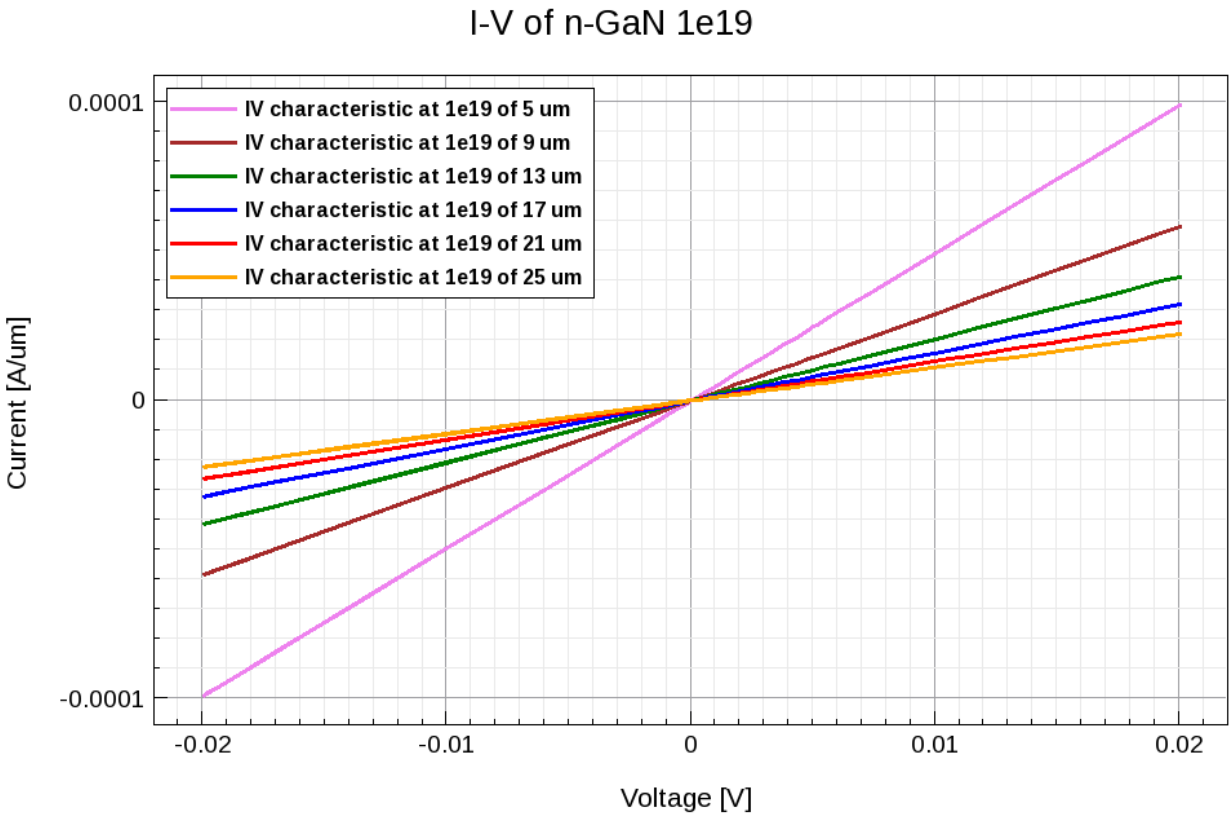

Fig. 4-10. IV characteristics of n-GaN of Doping 1e19 with work-function 4.3.

TABLE 4-6. Total Resistance for TLM plot under different doping conditions.

d	**1e16**	**1e17**	**1e18**	**1e19**
5	31786.025	4691.077	927.211	201.987
9	53536.934	7885.869	1570.101	342.657
13	75134.692	11059.683	2208.062	482.196
17	96811.433	14244.525	2848.668	622.349
21	118431.531	17421.925	3487.432	762.066
25	140078.115	20603.38	4127.147	902.008

TLM plot for these various doping conditions is shown in Fig. 4-11. It can be observed that as the doping increases, mobility decreases. However, the decrease in mobility is much less than the increase in doping which leads to a rapid reduction in sheet resistance with the increase in doping of the semiconductor. Hence, it can be observed in TLM plot that as the doping of n-GaN increases, the slope of the plot reduces as slope represents the sheet resistances.

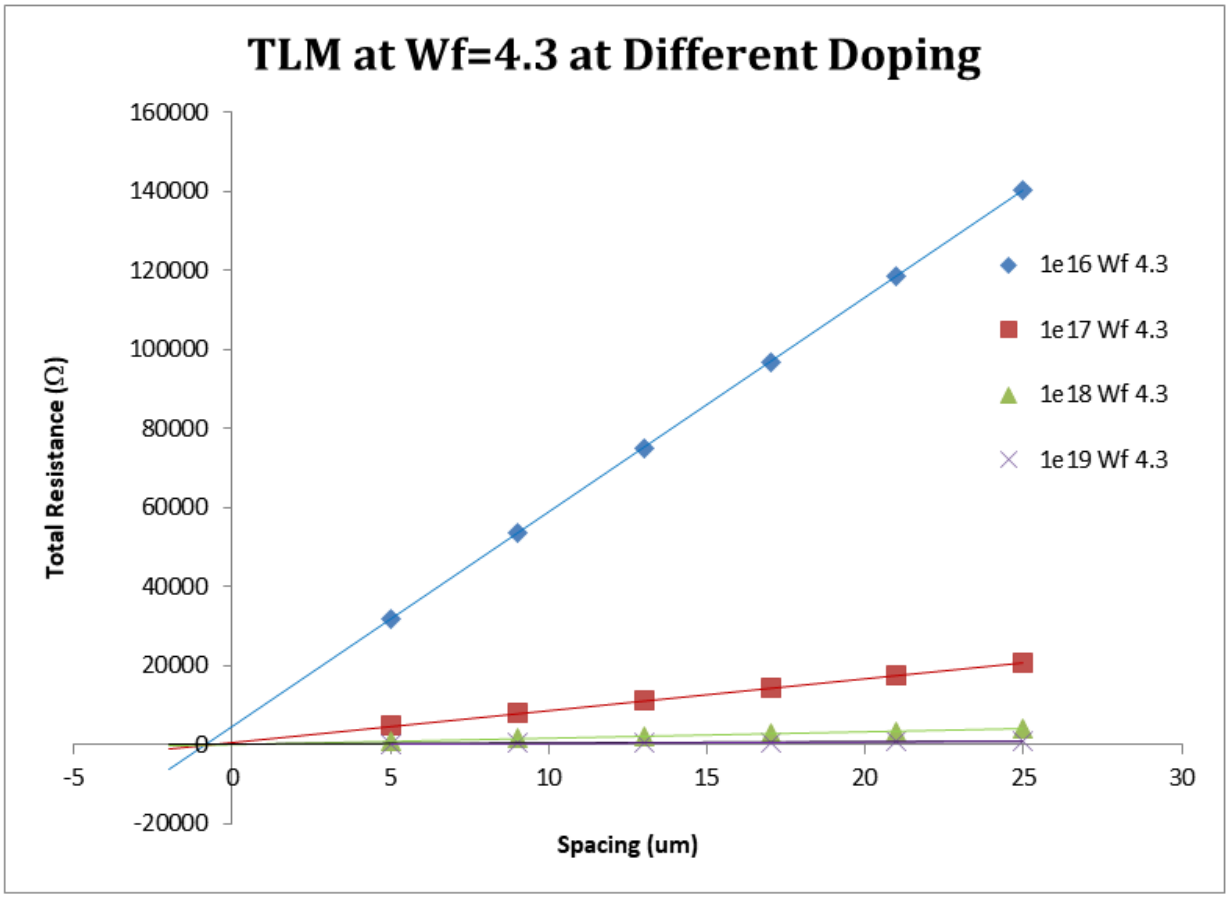

Fig. 4-11. TLM plot of lateral n-GaN with Wok-function 4.3 at different doping.

TABLE 4-7. TLM fit parameters along with extracted parameters for different doping.

Doping	**1e16**	**1e17**	**1e18**	**1e19**
TLM Linear Fit				
Slope	5412.998979	795.3895	159.9449	34.98918
Intercept	4768.174488	720.2345	128.9308	27.37282
R^2	0.999999305	0.999999	0.999999	0.999999
Electrical Properties				
Sheet Resistance (Ω)	5412.998979	795.3895	159.9449	34.98918
Contact Resistance (Ω)	2384.087244	360.1173	64.46537	13.68641
Bulk Resistivity (Ω-cm)	0.541299898	0.079539	0.015994	0.003499
Transfer Length (um)	0.440437409	0.452756	0.403048	0.391161
Contact Resistivity (Ω-cm^2)	1.05004E-05	1.63E-06	2.6E-07	5.35E-08

Parameters extracted from the lateral structure for various doping conditions are shown in TABLE 4-7. It includes the linear fit parameters of the various doping conditions along with the extracted electrical parameters. R-squared or R^2 value is a measure of how good the linear fit parameters are to the actual data point. A really good fit line has R^2 =1. The parameter transfer length is the x-intercept of the TLM plot. This transfer length is the effective length taken by the current to flow from metal to semiconductor or vice versa. Contact resistivity is calculated from transfer length and sheet resistance.

The current density contours under different doping conditions are shown in Fig. 4-12. It can be seen that the current density of the metal contacts keeps increasing as the doping increases. The transfer length can be also noted in the structures as the highest current density is occupying only a small fraction of the total metal contact on the semiconductor in all doping conditions.

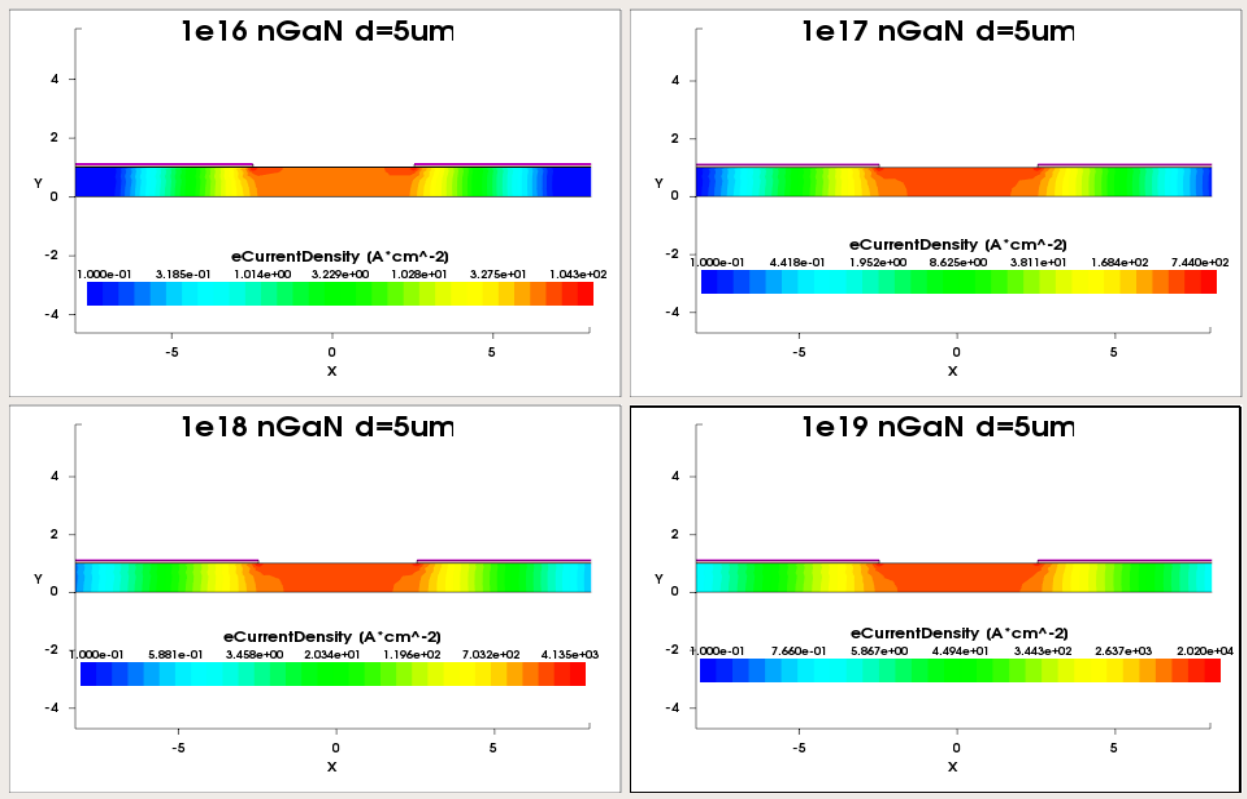

Fig. 4-12. Current Density contours for Different Doping of n-GaN.

4.2.2 N^{++} layer under the contact and throughout bulk

A heavily doped layer is placed under the metal contact to provide better ohmic contacts to the metal-semiconductor interface. This heavily doped layer can be deposited in two methods- One namely, the heavily doped layer is grown only under the metal contacts, or the heavily doped layer can be deposited throughout the semiconductor layer. The structure of both the cases of n^{++} layer under contact and throughout bulk layer is shown in Fig. 4-13. The current density for n layer doping of 1e17 cm^{-3} and n^{++} concentration of 1e20 cm^{-3} is shown for both the cases of n^{++} is shown in Fig. 4-14 and Fig. 4-15.

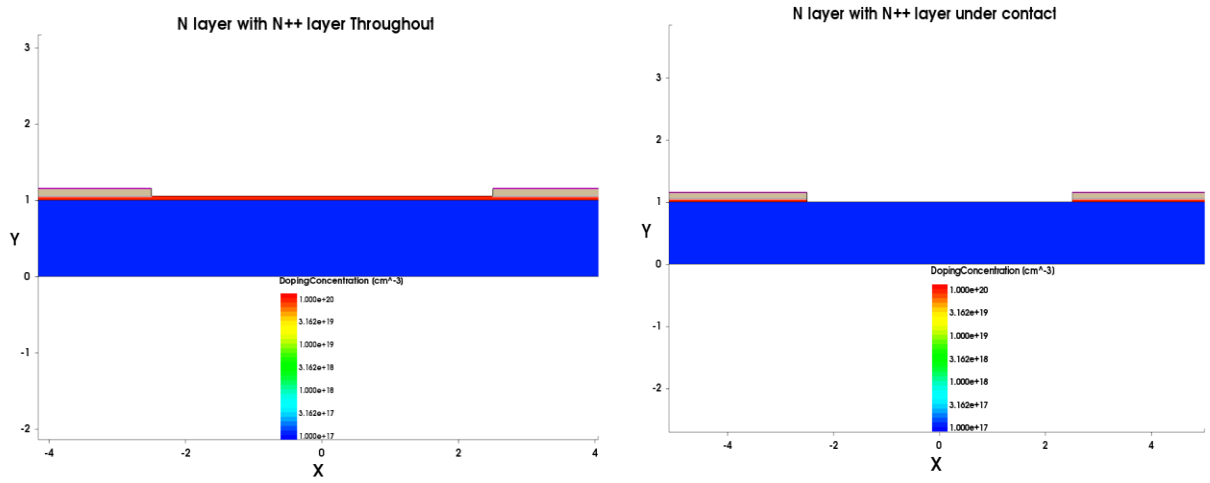

Fig. 4-13. Structure of lateral n-GaN with n^{++} layer throughout bulk and just under metal contact.

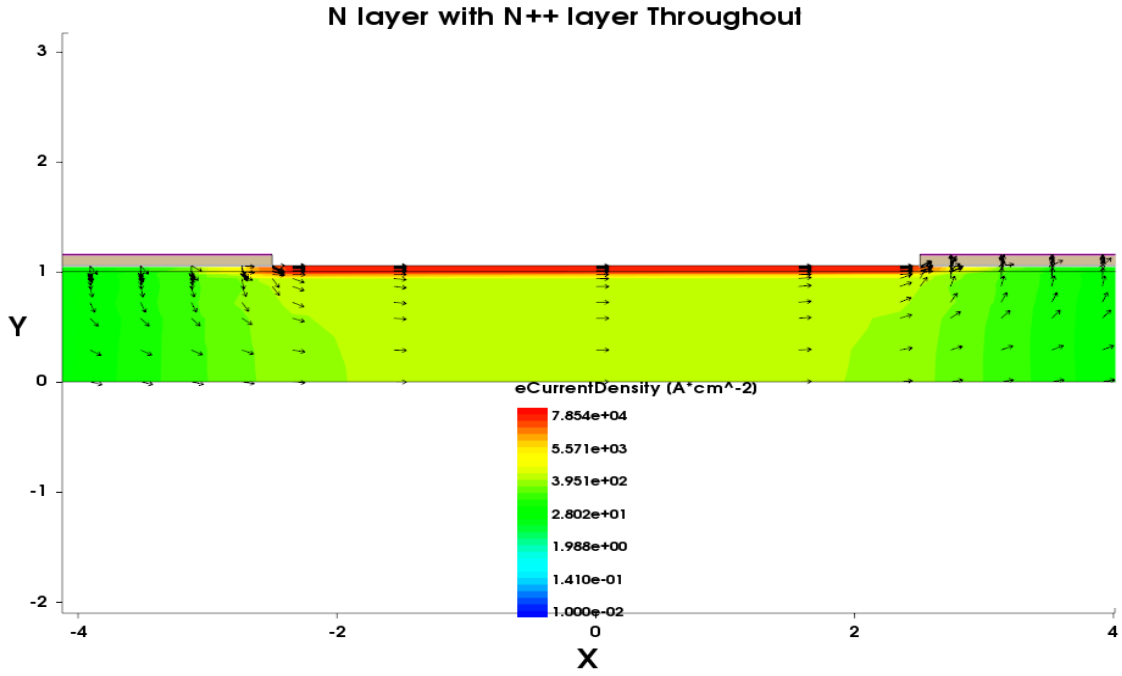

Fig. 4-14. Current Density contour with n-GaN 1e17 with n^{++} 1e20 cm^{-3} of 54nm thickness.

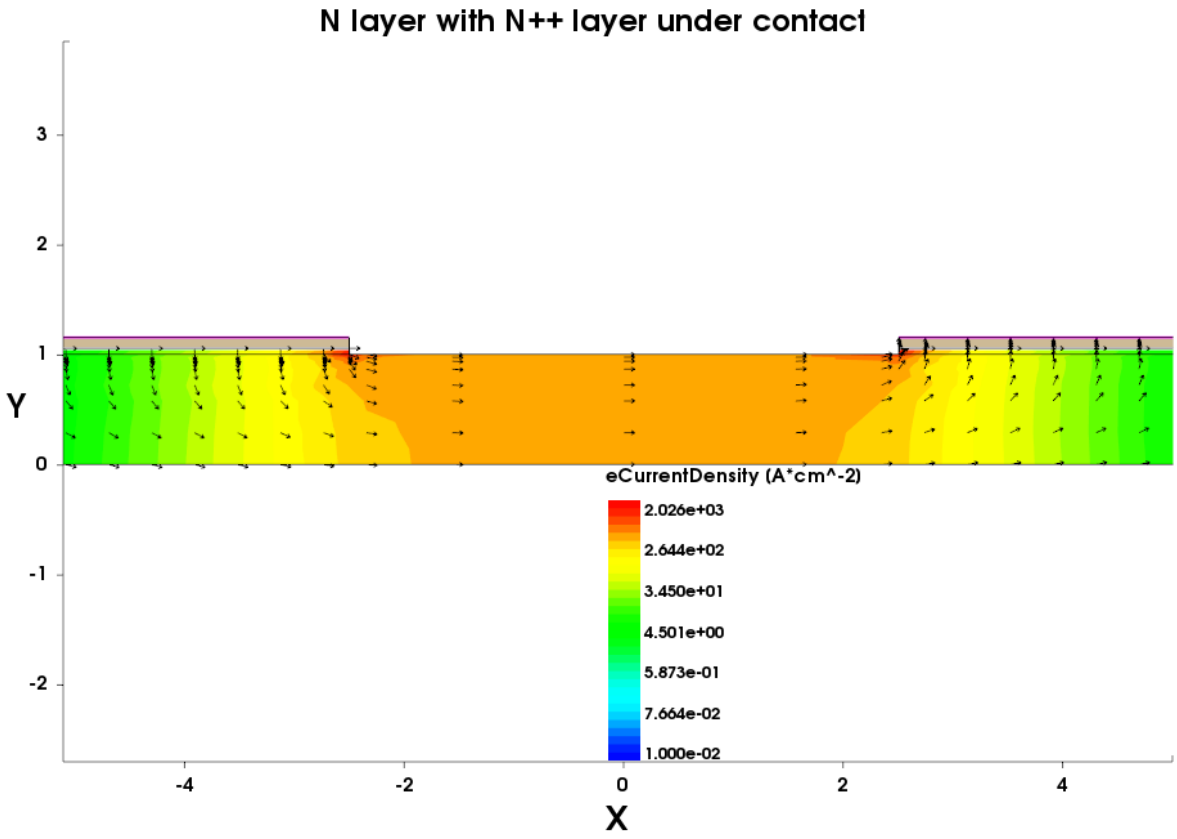

Fig. 4-15. Current Density contour with n^{++} 1e20 cm^{-3} with 54nm thickness under metal contact.

The thickness and the doping of the n^{++} layer are varied to study the effect of properties of n^{++} layer. The thickness of n^{++} layer is varied as 2nm, 6nm, 18nm, and 54nm. The electron current density for the condition when n^{++} layer is present throughout the bulk is plotted for the n layer of doping 1e17 with n^{++} layer of 1e20 and variable thickness as shown in Fig. 4-16. The metal-semiconductor interface is zoomed in the Fig. 4-17. It can be noticed that when the thickness of n^{++} layer is 54 nm, the entire current tends to flow through the n^{++} layer as it offers the lowest resistivity for the current flow. The arrows in the electron current density contour represent the direction of current flow. The electron current density for the condition when n^{++} layer is present just under the metal contact is plotted in Fig. 4-18.

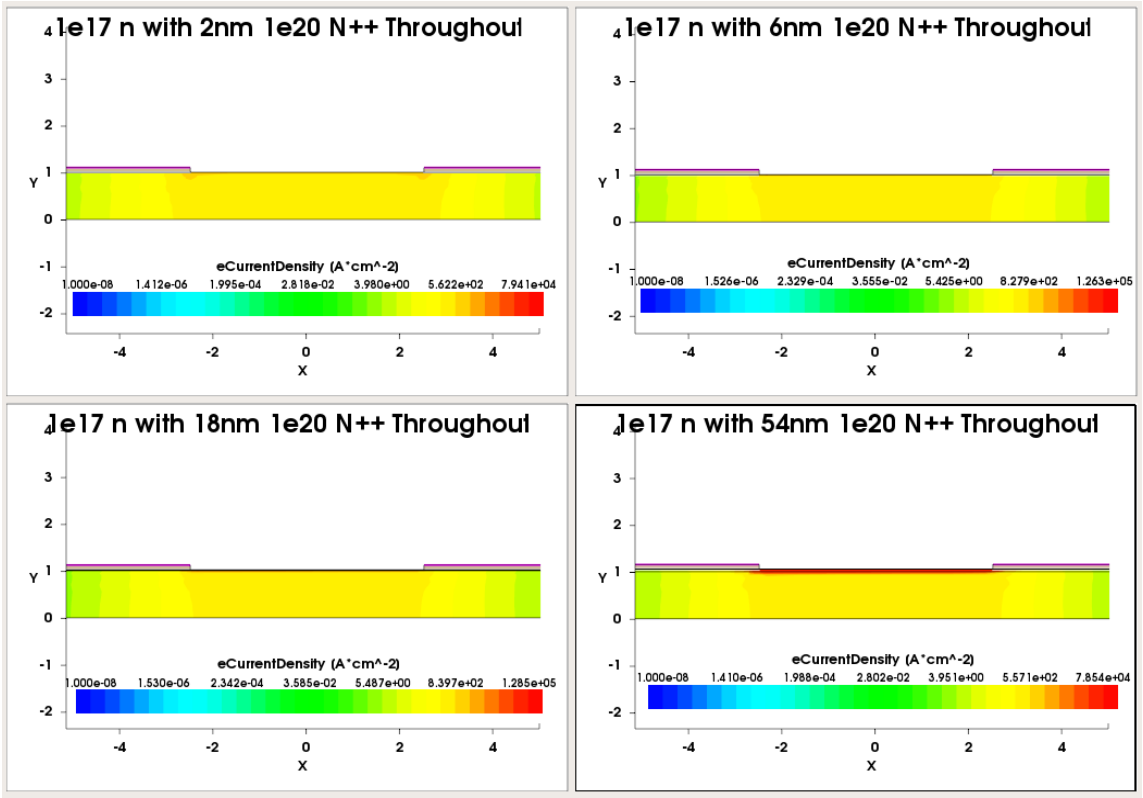

Fig. 4-16. Current Density contour with n^{++} of different thickness throughout bulk.

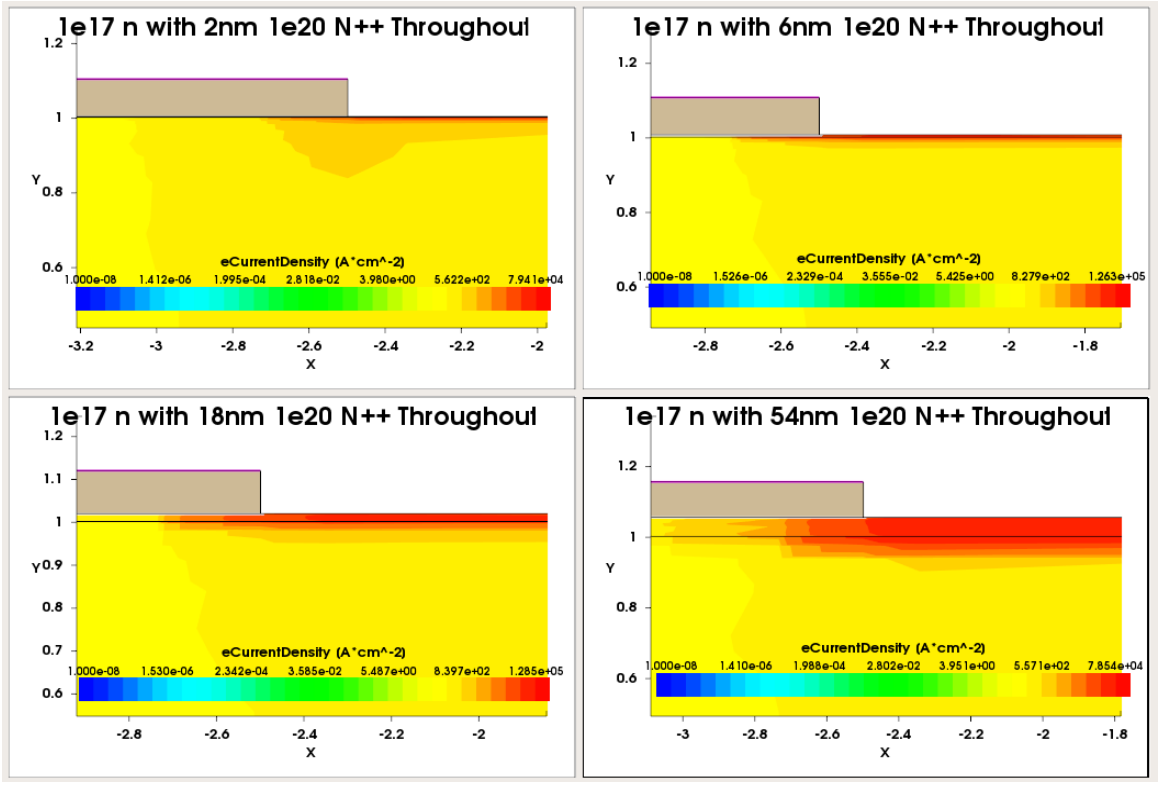

Fig. 4-17. Zoomed version of current density in n^{++} layer for different thickness.

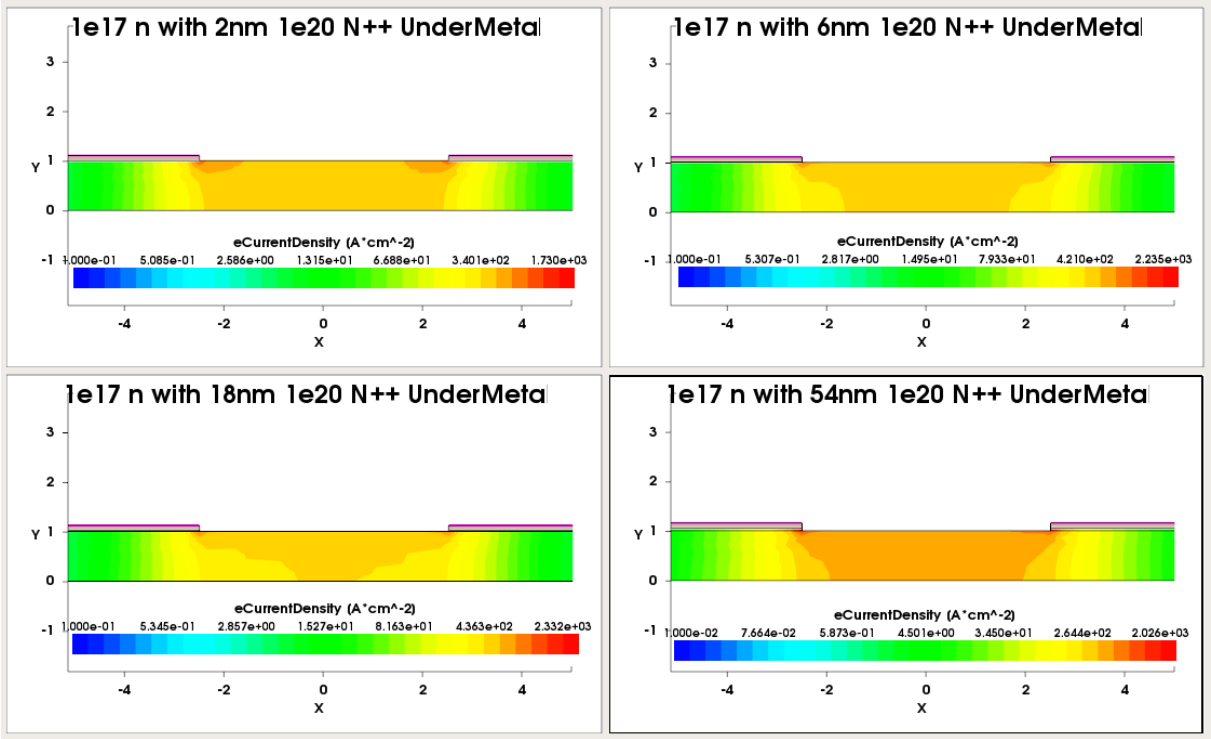

Fig. 4-18. Current Density contour with n^{++} of different thickness under the metal.

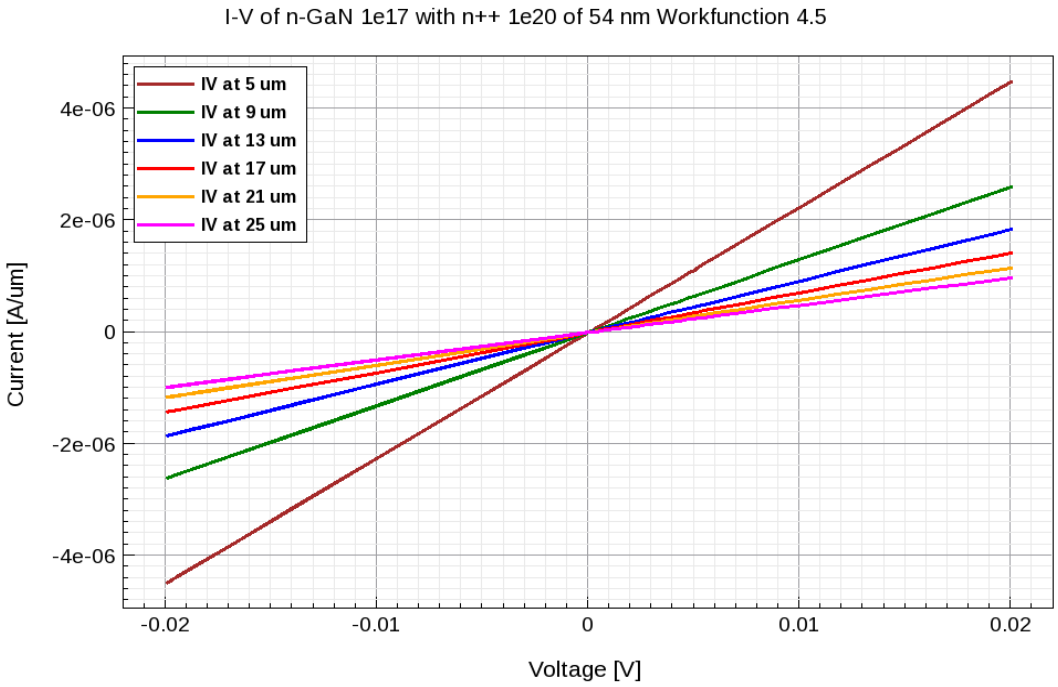

Fig. 4-19. IV curves of n-GaN 1e17 with n^{++} of 1e20 with 54nm just under metal contact.

I-V characteristics of the effect of the n^{++} layer for different cases are shown in Fig. 4-19 and Fig. 4-20. It can be observed from I-V curves that when the n^{++} layer is present throughout the bulk layer, more current tends to flow across the metal-semiconductor interface than when the n^{++} layer is just under the metal contact.

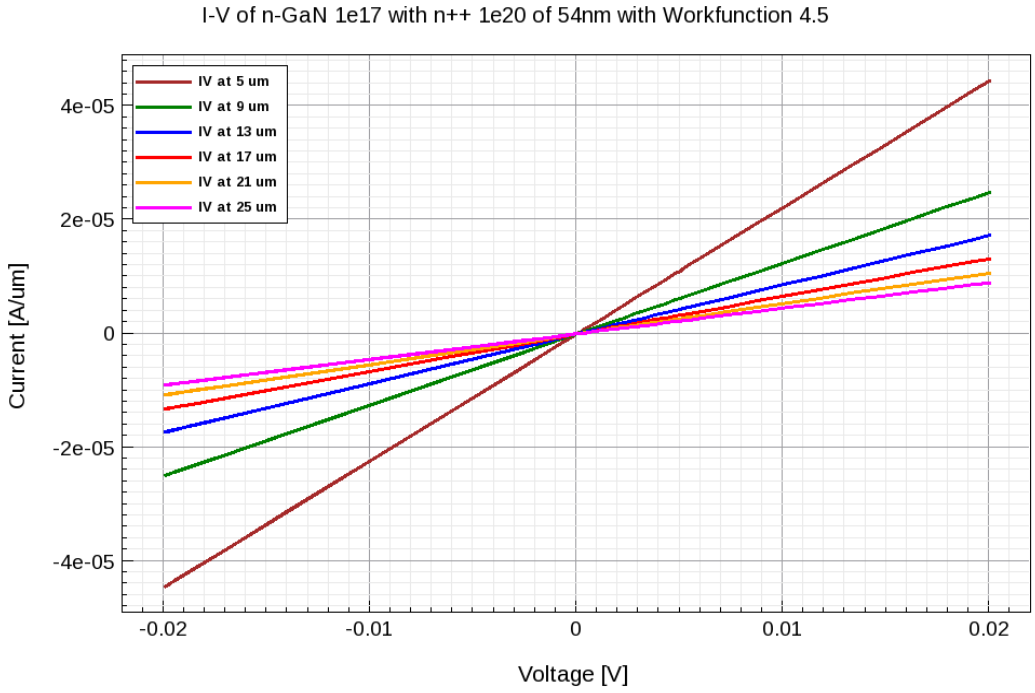

Fig. 4-20. IV curve of n-GaN 1e17 with n^{++} 1e20 54nm throughout the bulk layer.

The effect of various thicknesses and doping of n^{++} layer under both the cases of n^{++} layer (just under metal and throughout the bulk) is listed in TABLE 4-8. It can be observed that the contact resistivity is much when the n^{++} layer is present throughout the bulk. When the n^{++} layer is present throughout the top of the bulk semiconductor, a major part of the current tends to flow through n^{++} layer without entering n-layer since n^{++} layer provides low resistance path. This current flow through n^{++} layer causes a significant reduction in transfer length needed for current flow. It can be observed that the reduction in contact resistivity has almost saturated after 18nm thickness for various doping of n^{++} layers.

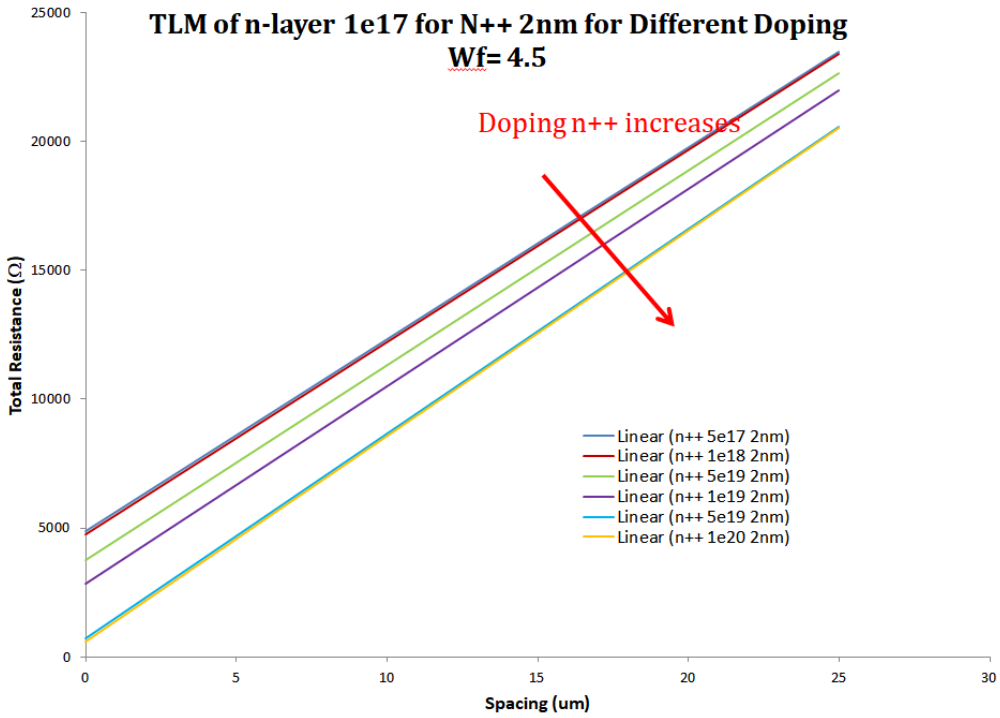

Fig. 4-21. TLM curve of n-GaN 1e17 with n^{++} 2nm just under metal with different doping.

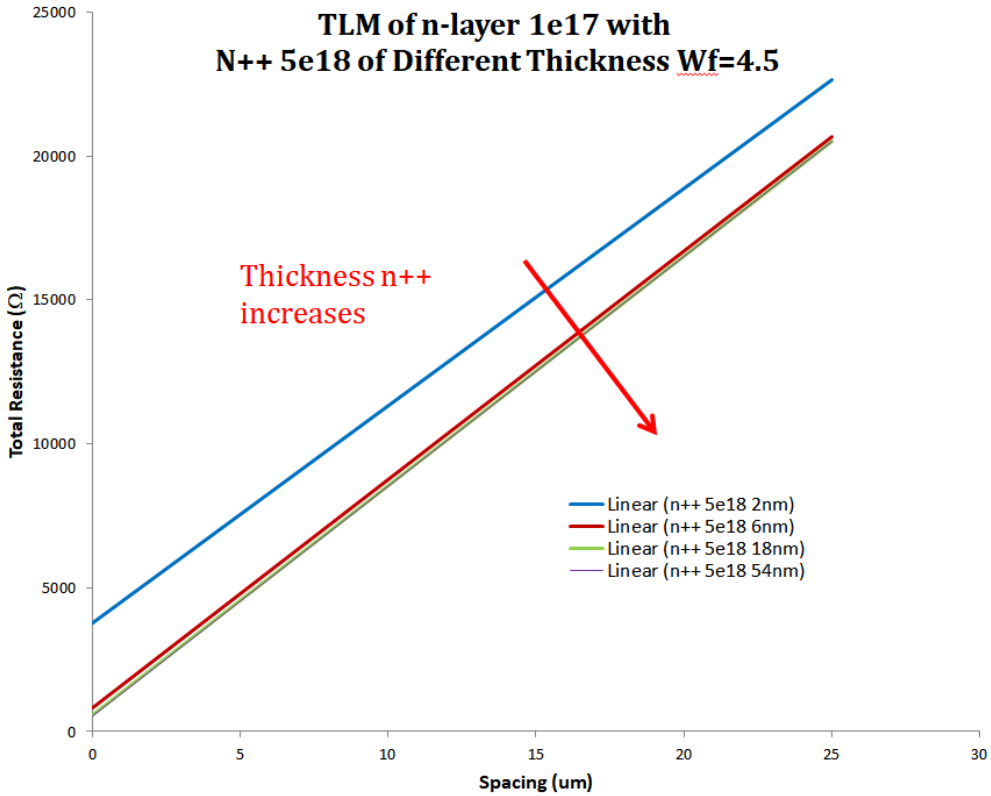

Fig. 4-22. TLM curve of n-GaN 1e17 with n^{++} 5e18 just under metal with different thickness.

TABLE 4-8. n-GaN with 1e17 doping contact resistivity with different doping and thickness of n^{++} layer with metal work-function of 4.5.

N^{++} ONLY UNDER METAL						
Dop/Thick (nm)	**5.00E+17**	**1.00E+18**	**5.00E+18**	**1.00E+19**	**5.00E+19**	**1.00E+20**
2	8.07E-05	7.60E-05	4.71E-05	2.64E-05	1.59E-06	1.06E-06
6	5.05E-05	3.04E-05	2.10E-06	1.17E-06	9.33E-07	9.10E-07
18	8.04E-06	2.30E-06	1.04E-06	9.88E-07	9.25E-07	9.04E-07
54	2.56E-06	1.75E-06	9.91E-07	9.01E-07	7.71E-07	7.30E-07
N^{++} THROUGHOUT THE BULK						
Dop/Thick (nm)	**5.00E+17**	**1.00E+18**	**5.00E+18**	**1.00E+19**	**5.00E+19**	**1.00E+20**
2	7.67E-05	7.31E-05	4.96E-05	3.07E-05	2.59E-06	1.04E-06
6	5.43E-05	3.52E-05	2.80E-06	1.22E-06	6.40E-07	5.57E-07
18	8.61E-06	2.07E-06	5.48E-07	3.60E-07	1.17E-07	7.01E-08
54	2.90E-06	9.39E-07	1.30E-07	5.26E-08	4.44E-09	1.42E-09

The contact resistivity for n layer of 1e18 doping concentration is shown in TABLE 4-9. It can be observed from both the tables that significant contribution in the reduction of contact resistivity is observed when the thickness is more than 18nm and the ratio of the doping concentration of n^{++} with n layer is more than 100. It is seen that when n^{++} is present throughout the bulk layer, contact resistivity reduces by a large margin than just under contact. The plot of contact resistivity with thickness at different doping conditions is shown in Fig. 4-23. The contact resistivity variation with doping at different thickness is shown in Fig. 4-24.

TABLE 4-9. n-GaN with 1e18 doping contact resistivity with different doping and thickness of n^{++} layer with metal work-function of 4.5.

N^{++} ONLY UNDER METAL				
Dop/Thick (nm)	**5.00E+18**	**1.00E+19**	**5.00E+19**	**1.00E+20**
2	4.23E-07	3.80E-07	2.58E-07	2.54E-07
6	2.87E-07	2.74E-07	2.26E-07	2.21E-07
18	2.66E-07	2.46E-07	2.26E-07	2.21E-07
54	2.97E-07	2.55E-07	2.05E-07	1.91E-07
N^{++} THROUGHOUT THE BULK				
Dop/Thick (nm)	**5.00E+18**	**1.00E+19**	**5.00E+19**	**1.00E+20**
2	5.10E-07	4.53E-07	2.81E-07	2.47E-07
6	3.12E-07	2.64E-07	1.88E-07	1.61E-07
18	2.20E-07	1.80E-07	9.40E-08	6.16E-08
54	1.56E-07	1.01E-07	2.47E-08	1.05E-08

Hence, the sheet resistance offered by the bulk is significantly affected as current tends to flow through the n^{++} layer. The purpose of n^{++} layer is to just reduce the contact resistance without affecting the bulk current flow path, it is suggestible to implement heavy doped region only under the metal contact.

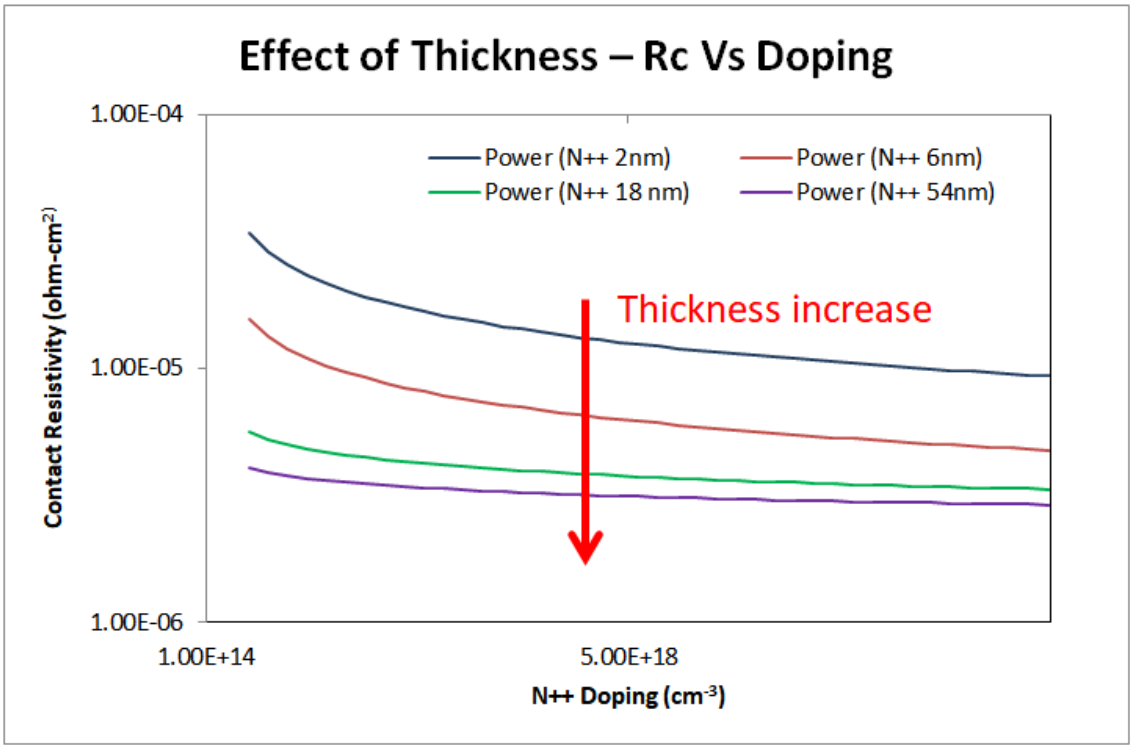

Fig. 4-23. Contact Resistivity vs. Doping at different thickness of n^{++} layer.

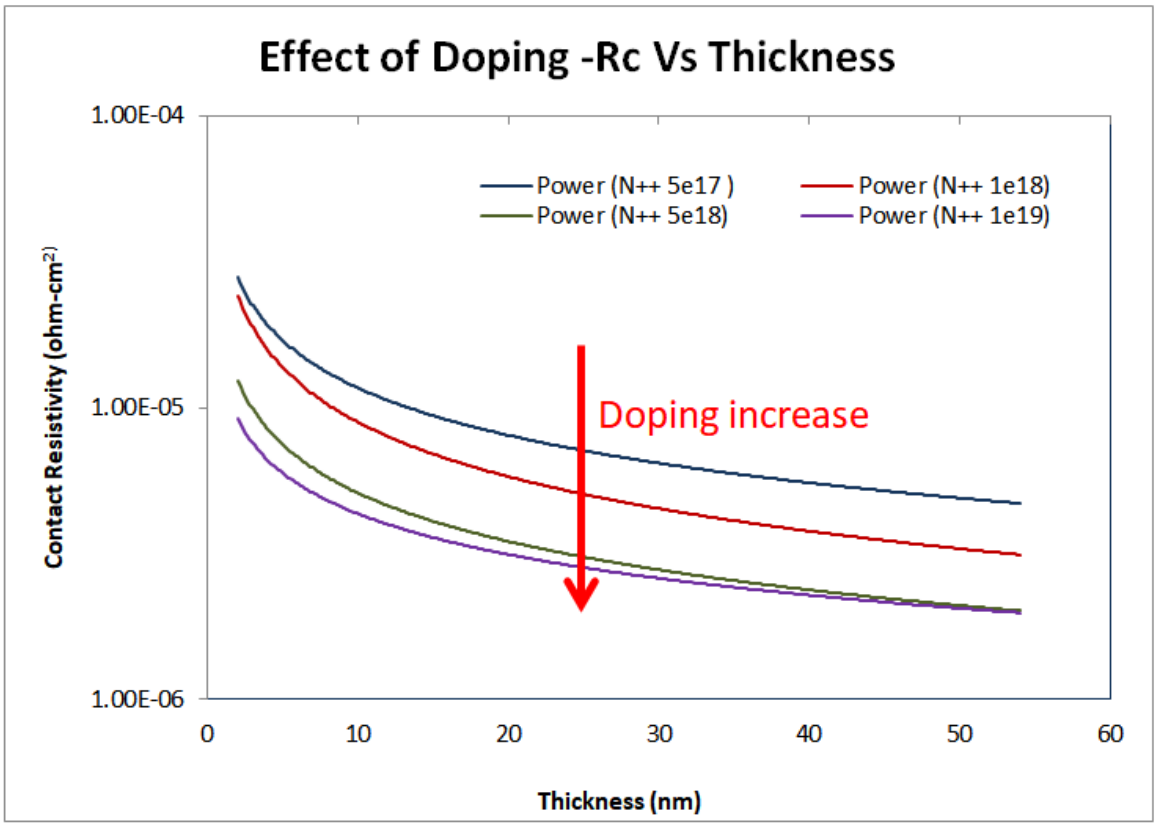

Fig. 4-24. Contact Resistivity vs. Thickness at different doping of n^{++} layer.

4.2.2.1 Application of n^{++} layer

The presence of heavily doped semiconductor layer under the metal makes the contact more ohmic as discussed in the previous section. Hence, the presence of this layer can help in making a schottky contact into an ohmic contact. When the barrier height at the metal-semiconductor junction is very high, thermionic current reduces as enough electrons do not have the energy to cross such high barrier height. However, the presence of heavily doped layer helps in electron tunneling at the junction which increases with increase in doping of the layer under the metal contact.

Simulations were performed for the Nickel metal (Work-function=5.2eV) which has a huge barrier height of 1.0eV with a heavily doped semiconductor layer and variable thickness to study the conversion of schottky contact into ohmic contact. The semiconductor with doping of 1e17 cm^{-3} with a metal of work-function 5.2 is studied. The observed behavior of the metal-semiconductor interface with different thickness and doping of this layer is given in TABLE 4-10. It can be seen that 2nm thickness of n^{++} does not have major effect while for 6nm thick n^{++} layer when doping exceeds 5e19 cm^{-3}, contact becomes ohmic. Ohmic behavior is observed for doping greater than 5e18 cm^{-3} for 18nm thick layer while for a 54nm thick layer, doping of more than 2e18 cm^{-3} makes the contact ohmic.

TABLE 4-10. Different thickness and doping of n^{++} layer and behavior of the metal contact.

N^{++} Thickness	**N^{++} Doping**	**Behavior**	
		Schottky	Ohmic
2 nm	5e17 – 1e20	✓	
6 nm	Doping <5e19	✓	
	Doping > 5e19		✓
18 nm	Doping < 5e18	✓	
	Doping >5e18		✓
54nm	Doping < 2e18	✓	
	Doping > 2e18		✓

4.2.3 Effect of presence of substrate

The structure of the n-GaN device with a substrate is shown in Fig. 4-25. The structure of the device and properties of the structure is shown in TABLE 4-11. The substrate is varied with three different cases- insulating substrate (intrinsically doped GaN), template layer of GaN (doped 1e16 cm^{-3} with low mobility).

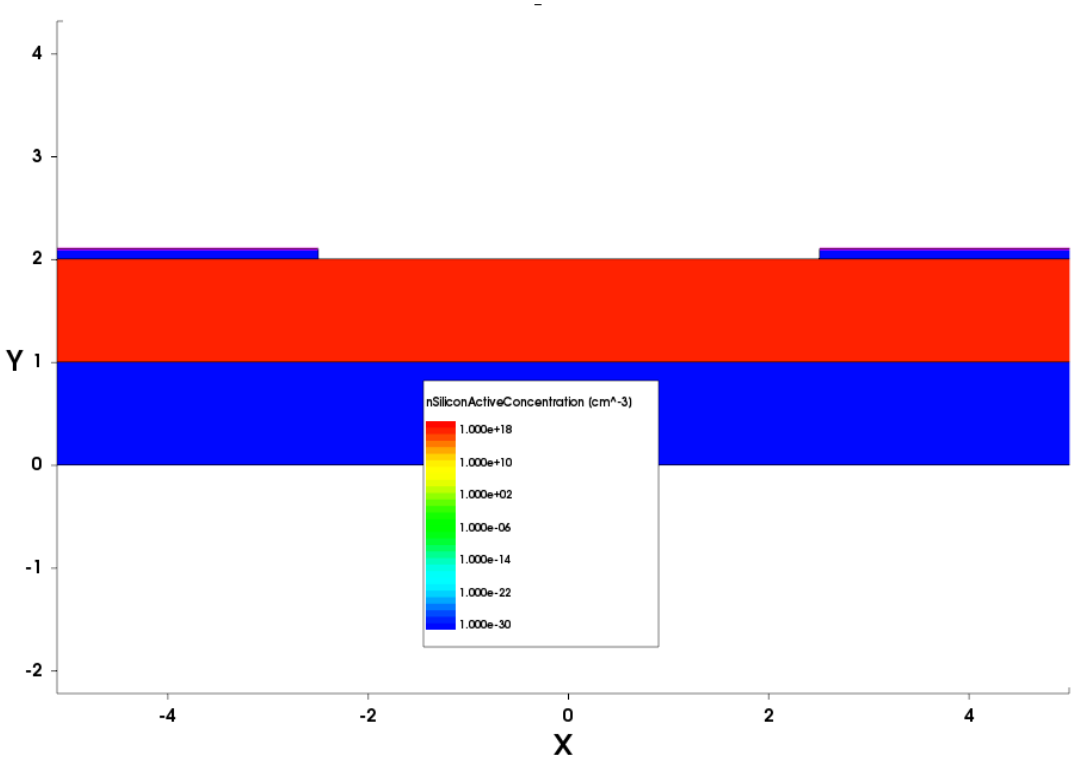

Fig. 4-25. Structure of device with lateral n-GaN with the substrate.

TABLE 4-11. Dimensions of lateral n-GaN with the substrate.

X	200 um
Metal Contact Dimension	75 um
Thickness n-layer	1 um
Thickness Substrate	1 um
metal thickness	100 nm
N Doping	1e17 cm^{-3}
Metal Work-function	4.5

The insulating substrate is considered first. The current density effect on n-GaN with an insulating substrate is shown in Fig. 4-26. The current density effect of conducting substrate with low mobility is shown in Fig. 4-27 and Fig. 4-28. The IV characteristics of all three cases are shown in Fig. 4-29, Fig. 4-30 and Fig. 4-31.

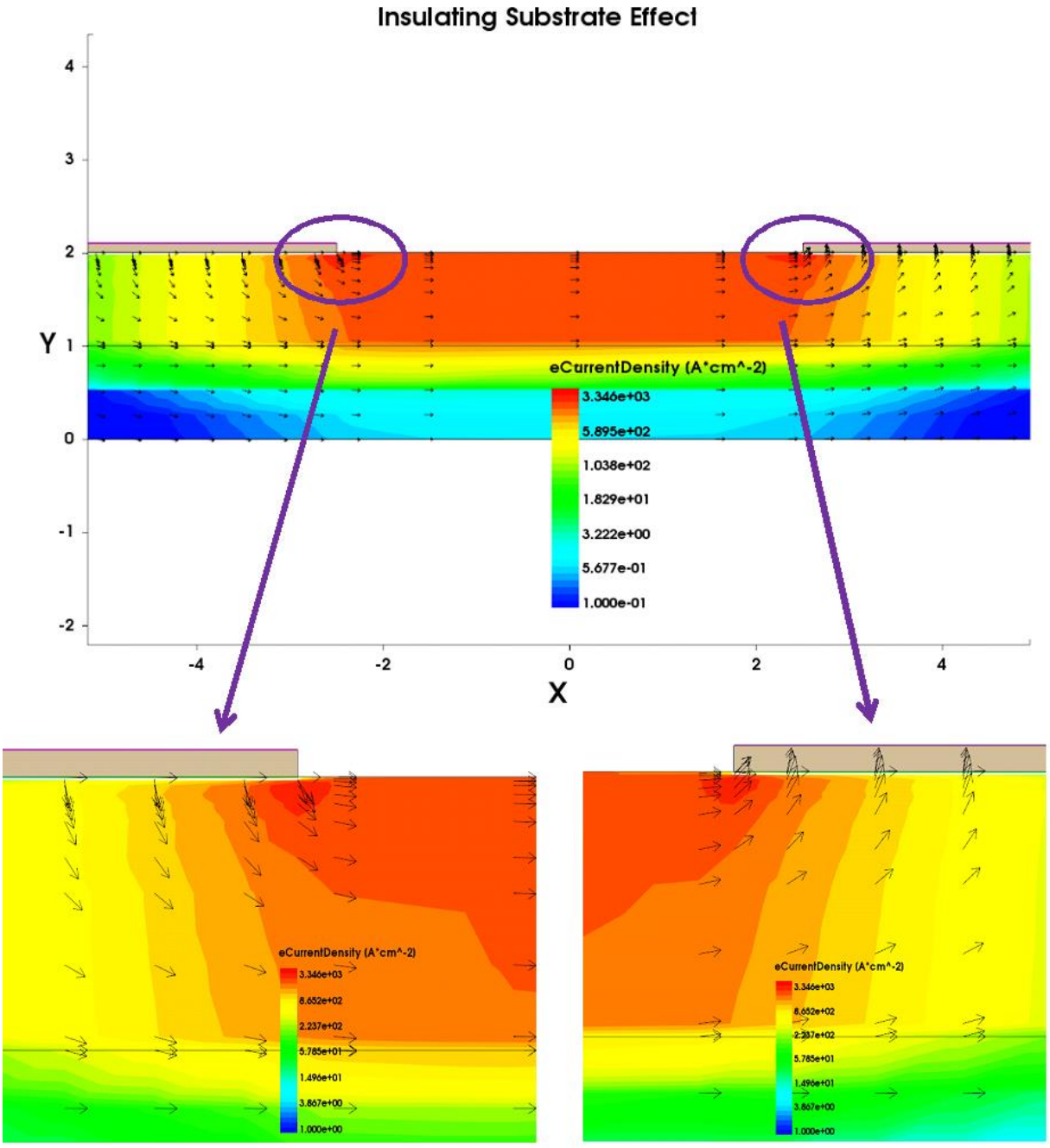

Fig. 4-26. Current Density contour in n-GaN with an insulating (Sapphire) substrate.

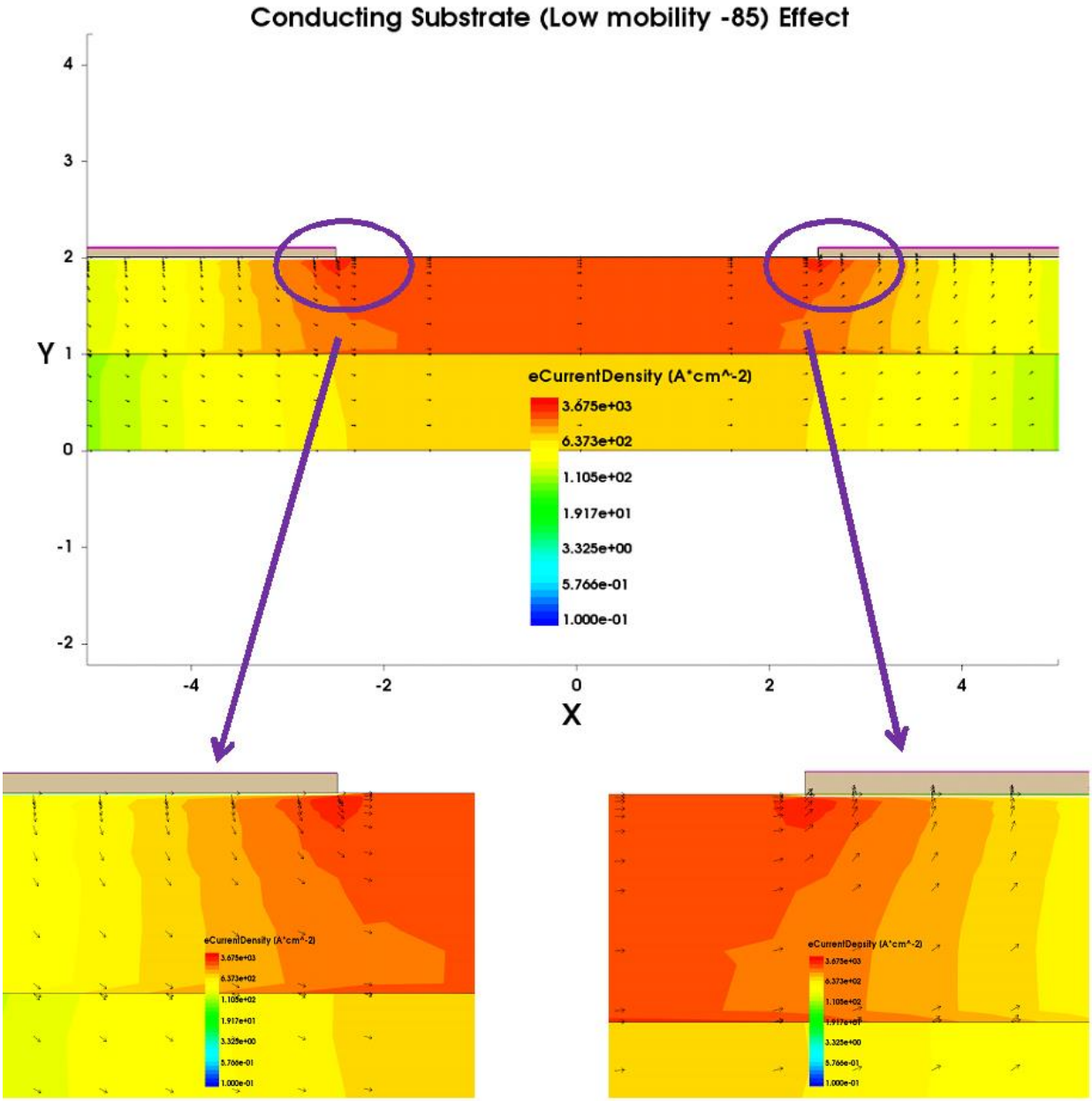

Fig. 4-27. Current Density contour in n-GaN with low mobility (85cm^2/Vs) conducting GaN substrate.

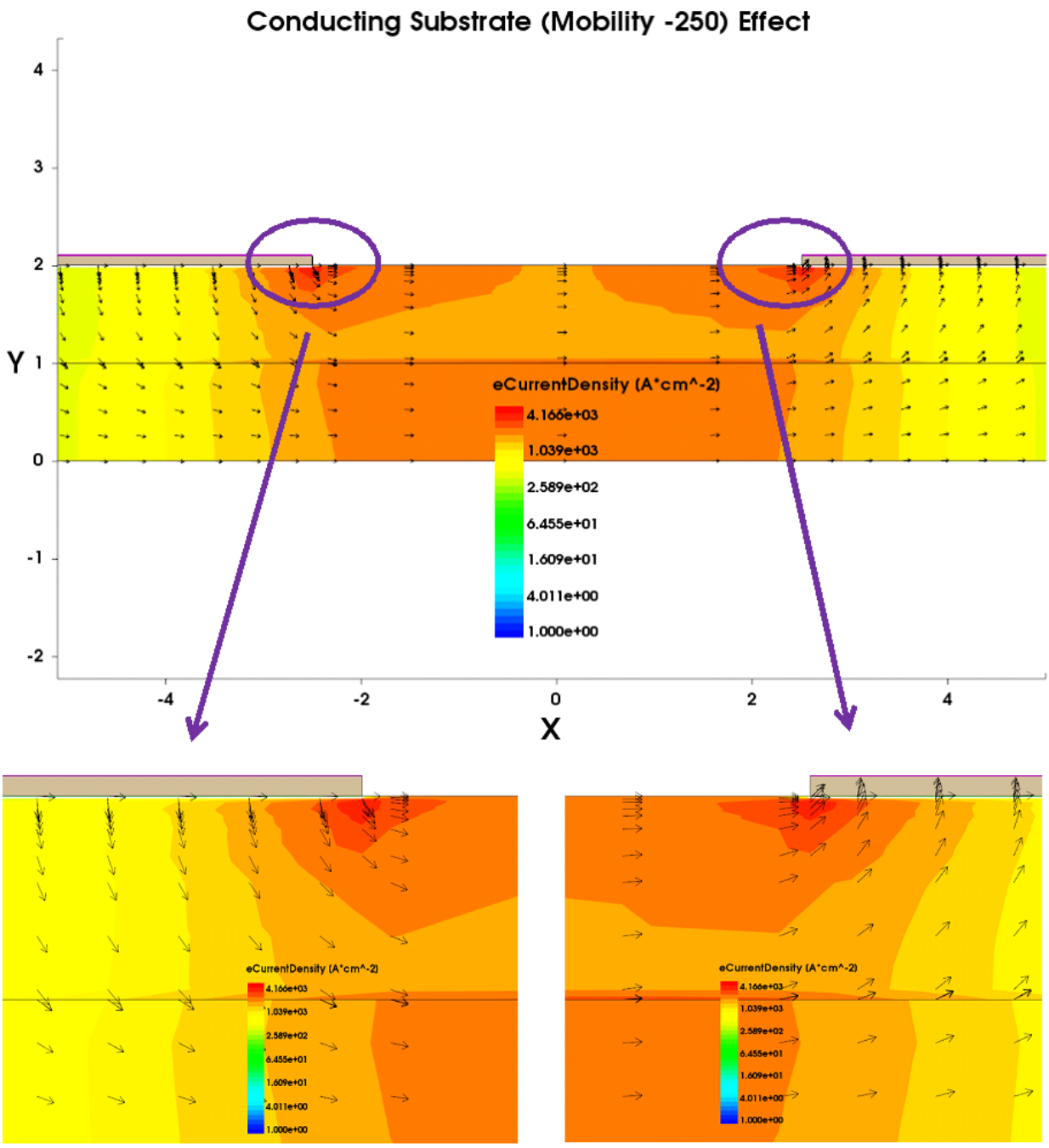

Fig. 4-28. Current Density contour in n-GaN with conducting low mobility (250cm^2/Vs) substrate.

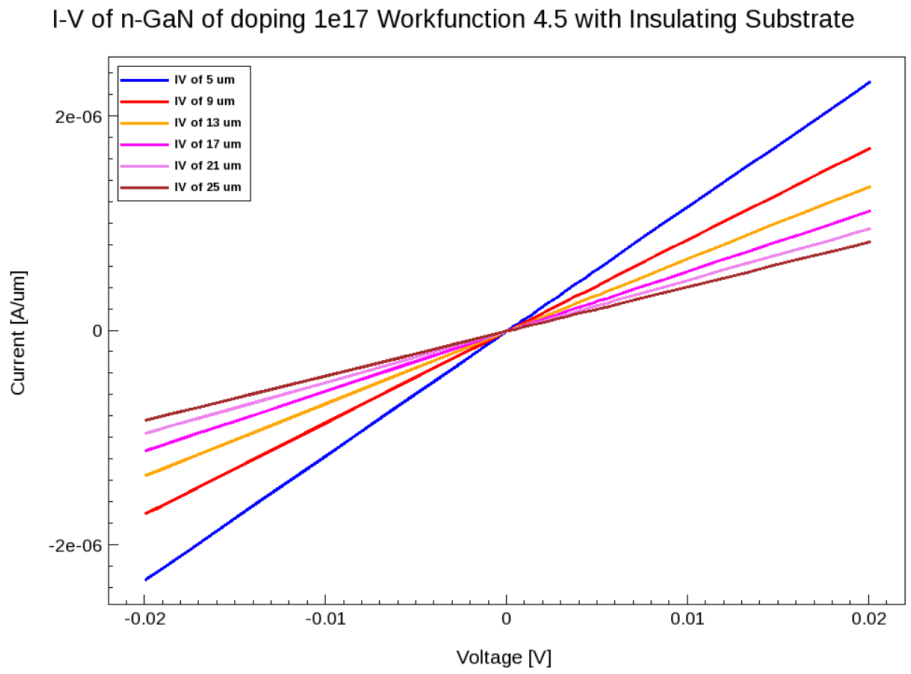

Fig. 4-29. IV curve of n-GaN with an insulating substrate.

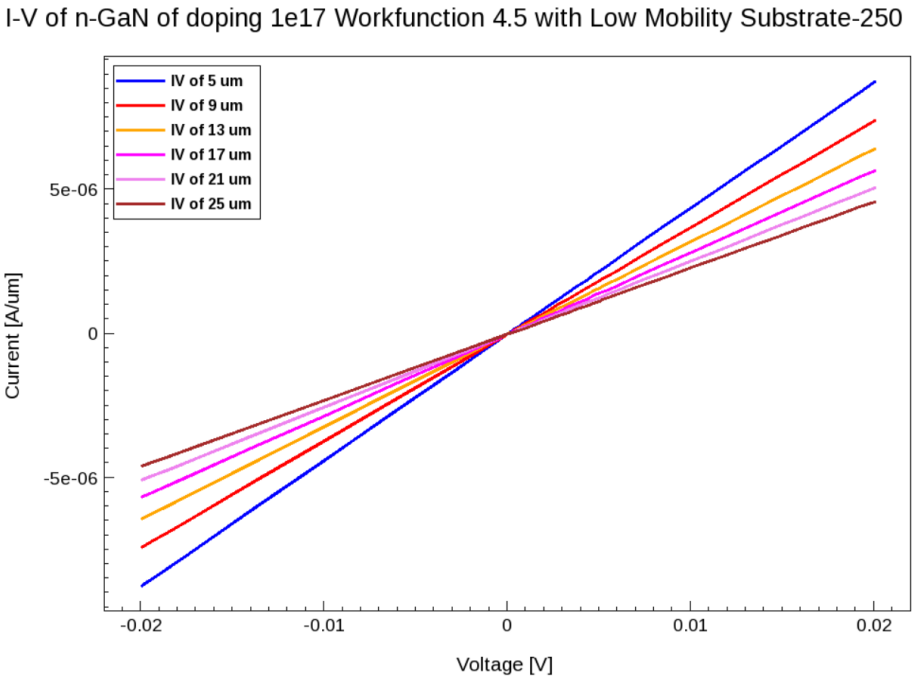

Fig. 4-30. IV curve of n-GaN with low mobility (250cm^2/Vs) GaN substrate.

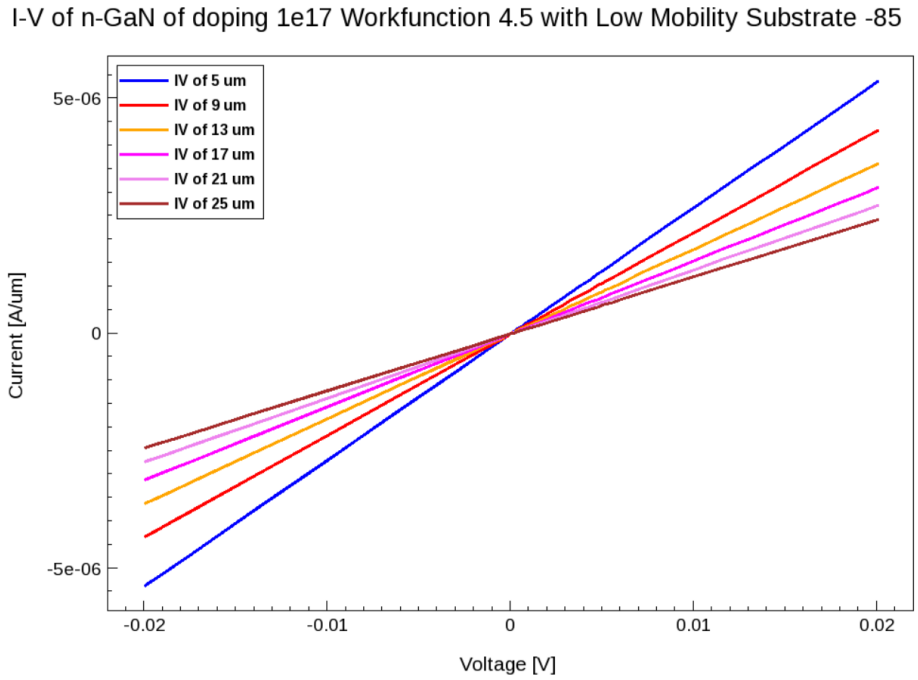

Fig. 4-31. IV curve of n-GaN with low mobility substrate (85 cm^2/Vs).

TABLE 4-12. Effect of different substrates on contact and sheet resistivity.

Bulk Doping	**Type of Substrate**	**Contact Resistivity (Ω-cm^2)**	**Bulk Resistivity Simulation(Ω-cm)**	**Bulk Resistivity Calculated(Ω-cm)**
1e17	No Substrate	7.07e-05	0.07953	0.0799
	Insulating Substrate	7.28e-05	0.0775	0.0799
	GaN substrate (μ=85 cm^2/V-s)	7.48e-05	0.0226	0.025289
	GaN substrate (μ=250 cm^2/V-s)	7.56e-05	0.0103	0.01079
1e18	No Substrate	5.31-07	0.01595	0.01599
	Insulating Substrate	6.04e-07	0.0151	0.01599
	GaN substrate (μ=85 cm^2/V-s)	7.81e-07	0.0109	0.01117
	GaN substrate (μ=250 cm^2/V-s)	9.97e-07	0.006958	0.00699

The effect of different substrates on contact resistivity and sheet resistivity are shown in TABLE 4-12. The sheet resistance has calculated using the concept discussed in Chapter 2 section 2.5 regarding the effect of substrate layer on sheet resistance calculation.

4.2.4 Effect of traps

The traps are one of the major reasons for conversion of a schottky contact into an ohmic contact due to the possibility of the trap to trap tunneling at the metal-semiconductor interface. The presence of traps converts the schottky contact into conducting ohmic contact as shown in Fig. 4-32. The IV characteristics are shown on the log scale for better understanding the effect of traps in Fig. 4-33.

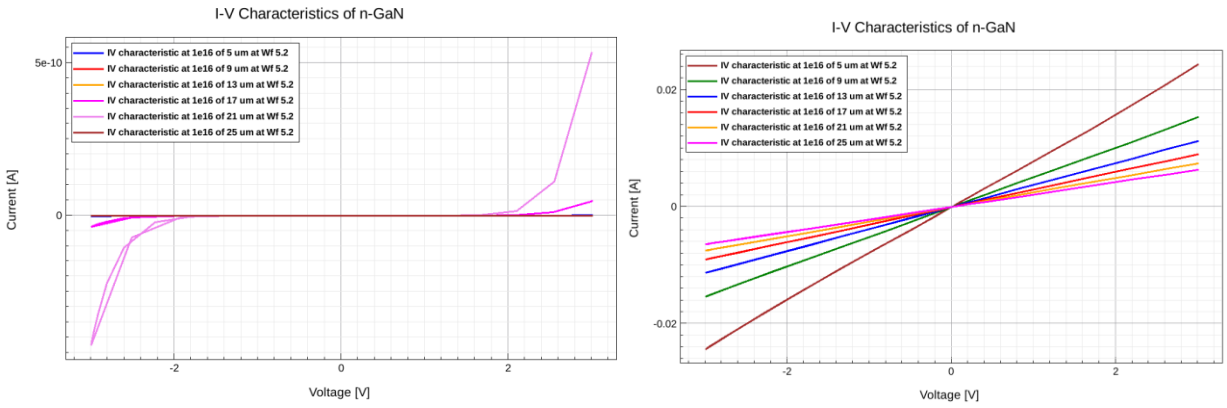

Fig. 4-32. Conversion of Schottky metal contact into ohmic contact due to the presence of traps.

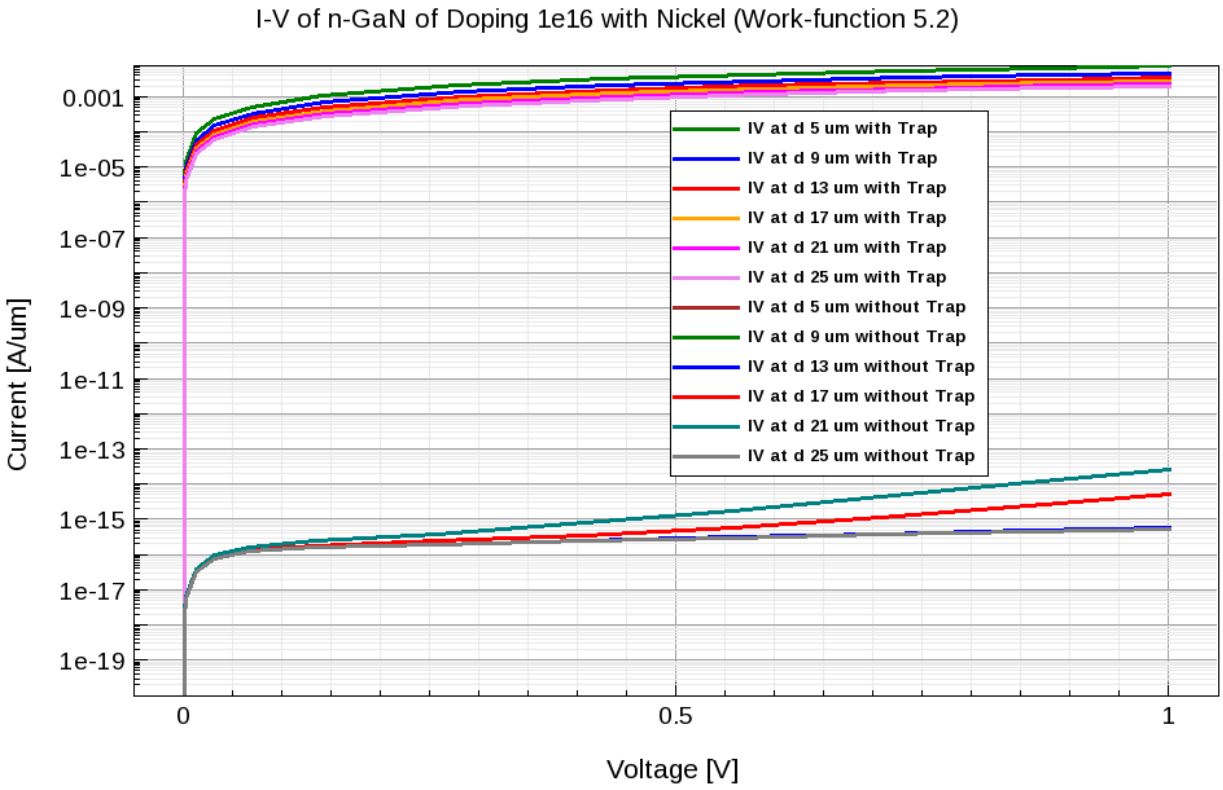

Fig. 4-33. Effect of traps on making schottky contact to ohmic contact.

4.3 Testing Results

4.3.1 Experimental setup

The Gallium Nitride devices are grown at Virginia Tech lab using MOCVD (Metal-Organic Chemical Vapor Deposition) process. The growth of GaN is through the combination of TMGa Trimethyl Gallium $(CH_3)_3Ga$ and Ammonia (NH_3). The TLM fabrication procedure is performed at Virginia tech MicrON lab. Metallization stack of Ti/Al/Ni/Ag is deposited for providing ohmic contacts on n-type GaN. Ti metal has low work-function which leads to low barrier height and hence expected ohmic contact on n-type GaN device.

The electrical characterization of the device is performed to study the TLM plot for all devices to study the contact characteristics. IV curves are obtained to calculate the total resistance for plotting the TLM plot. Four-point probe method is used for obtaining the IV curves. Two external probes are used to apply the current across the device while the two internal probes are

used to measure the voltage using the voltmeter. This four-point probe method is more advantageous compared to the two-point probe method. The probe resistance also contributes to the voltage drop in two-point probe as the application of current and voltage measurement is done using the probes.

The testing of the devices is performed using source meter Keithley 2400 along with four probe point method. The current range is varied from -1mA to 1mA with voltage compliance of ±20V. The measurement is done using an auto-prober setup which is controlled using LabView.

4.3.2 Comparison between basic n-GaN simulation

The devices are grown at Virginia Tech. The typical structure of the device is shown in Fig. 4-34. The Metal is made of the metallization structure Ti/Al/Ni/Ag for the n-GaN device. The UID layer is the unintentionally doped layer of GaN which grown above the substrate to prevent any growth defects penetrating into the bulk of the GaN device from the substrate. This UID layer is generally doped around 1e16 cm^{-3} and has a very low mobility of around 100cm^2/V-s as it filled with a lot of defects and impurities. Substrate layer could be made of wither Sapphire (Al_2O_3) or bulk Gallium Nitride. The most commonly used substrate in sapphire as bulk GaN is very expensive. Sapphire substrate is an insulating substrate. The growth condition of various devices is shown in TABLE 4-13.

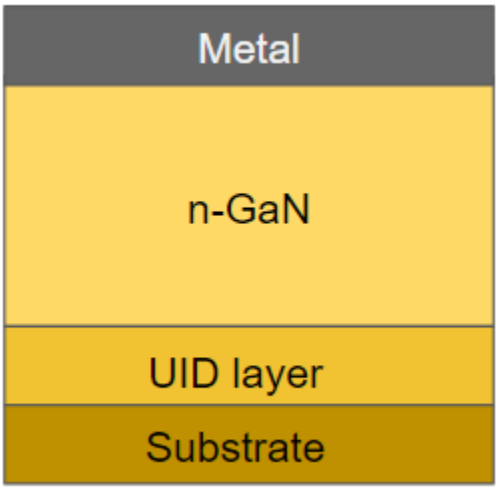

Fig. 4-34. Structure of practical device tested in the lab.

TABLE 4-13. Growth conditions of various samples used for testing.

Device Name/ Properties	**16063011**	**16070711**	**16080721**	**16080811**
N Doping (cm^{-3})	3.85E+18	1.12E+17	8.46E+18	1.53E+19
Thickness of n layer (um)	2.04	1.92	2.15	2.187
TMGa flow (mol/min)	6.26e-5	6.26e-5	1.88e-4	1.88e-4
SiH_4 flow (mol/min)	5.69e-9	7.11e-11	3.66e-8	5.575e-8

TABLE 4-14. Extracted parameters from testing and simulation (ideal) conditions.

Device	**Property**	**Simulation (Ideal)**	**Experimental**
16063011	Transfer Length (um)	0.920982	5.2929
	Sheet Resistance (Ω)	27.4409	33.66211
	Contact Resistivity (Ω-cm^2)	2.53e-7	9.43e-6
16070711	Transfer Length (um)	0.91295	4.549896
	Sheet Resistance (Ω)	330.6327	294.8209
	Contact Resistivity (Ω-cm^2)	3.02e-6	6.1e-5
16080721	Transfer Length (um)	1.014249	9.793277
	Sheet Resistance (Ω)	16.71407	16.48085
	Contact Resistivity (Ω-cm^2)	1.7e-7	1.58e-5
16080811	Transfer Length (um)	1.013012	7.926098
	Sheet Resistance (Ω)	10.88021	13.82679
	Contact Resistivity (Ω-cm^2)	1.1e-7	8.69e-6

The extracted parameters for the simulated and actual devices are listed in TABLE 4-14. It can be observed that the experimental contact resistivity is much higher than the simulated values. This is mainly due to the reason that the simulations are the ideal conditions which do not consider any surface defects or recombination centers. The samples are annealed in either N_2 or Ar to provide a better interface between metal and semiconductor. These annealing conditions lead to reaction at the interface of metal and semiconductor as reported in [17]. The calculated and experimentally obtained sheet resistances are same which shows the validity of the model. The discrepancies between the simulations and actual devices could be attributed to the defects, traps and surface impurities which are accounted in the simulations.

4.3.3 Comparison of n^{++} layer under the device

A new set of devices were grown with n^{++} layer under the metal contact for testing the effect of the heavily doped layer under the metal with structure without the n^{++} layer. The etching process is performed to study the effect of surface roughness on contact resistivity. Linear TLM is performed on these samples to compare the testing of the practical devices with simulations. The Circular TLM was also performed on these devices to compare the results of CTLM with LTLM. The CTLM and LTLM mask had spacing of 7, 10,13,16,20 and 25 um which were used to obtain the TLM plot. The annealing conditions were also varied to study the effect of annealing on contact resistivity. The device 17112711 has just n layer before and after etching as shown in Fig. 4-35. The device 17112721 has the n^{++} layer between the metal and semiconductor as shown in Fig. 4-36.

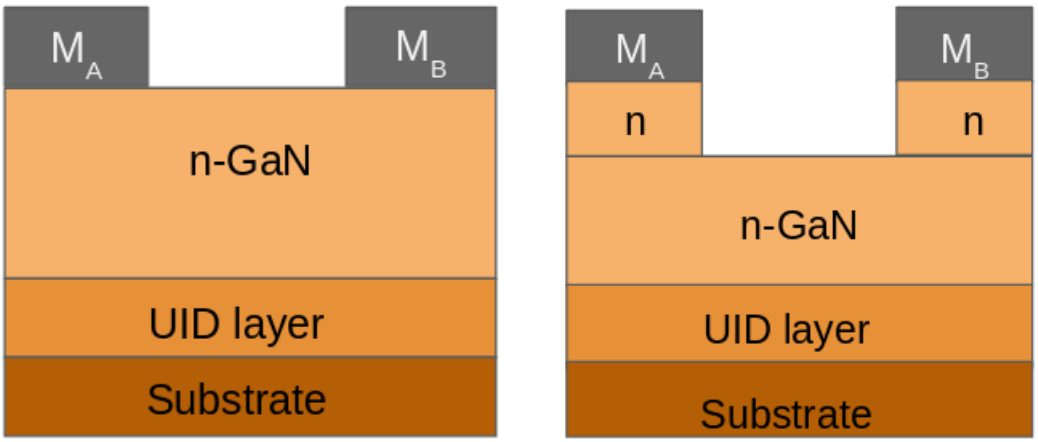

Fig. 4-35. GaN 17112711 Device structure before etching and after etching.

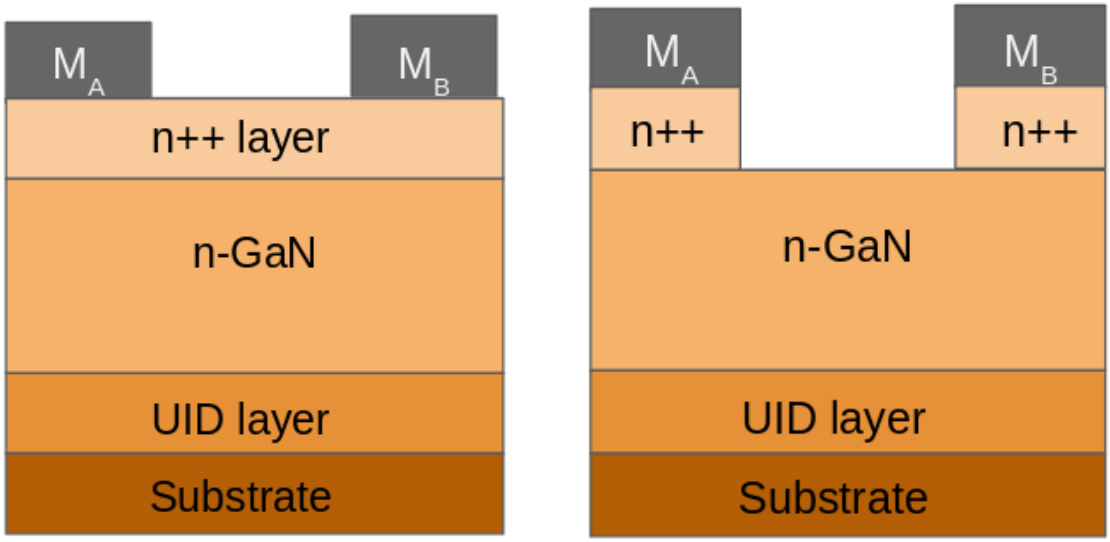

Fig. 4-36. GaN 17112721 Device structure before and after etching.

All the samples were subjected to both LTLM and CTLM testing to compare the results obtained from both testing methods. The sample of the same device is annealed at two different temperatures 300°C and 900°C in N_2 for 5 min to study the effect of annealing temperature on contact resistivity. These samples were etched in RIE to remove the n^{++} layer present throughout the bulk layer. The structure of the device is shown in TABLE 4-15. It also includes the conditions subjected to each device.

TABLE 4-15. Structure and Specifications of Devices 17112711 and 17112721.

Device Name/ Properties	17112711 - K	17112711 - M	17112721- H	17112721 - J
N Doping (cm^{-3})	1E+18	1E+18	1E+18	1E+18
Thickness of n layer (um)	1.0	1.0	1.0	1.0
N^{++} Doping (cm^{-3})	-	-	1.9E+19	1.9E+19
Thickness of n layer (um)	-	-	0.02	0.02
Annealing Temp (°C)	300	900	300	900
Annealing time	5 min	5 min	5 min	5 min

The samples were tested under three different conditions namely,

1. As-Deposited
2. After Annealing (300°C or 900°C)
3. After Etching

The sample with just n layer (1e18) provides schottky contact with As-Deposited metallization of Ti/Al/Ni/Ag. The samples are subjected to both linear and circular TLM. The mask used for depositing both circular and linear TLM patterns is shown in Fig. 4-37.

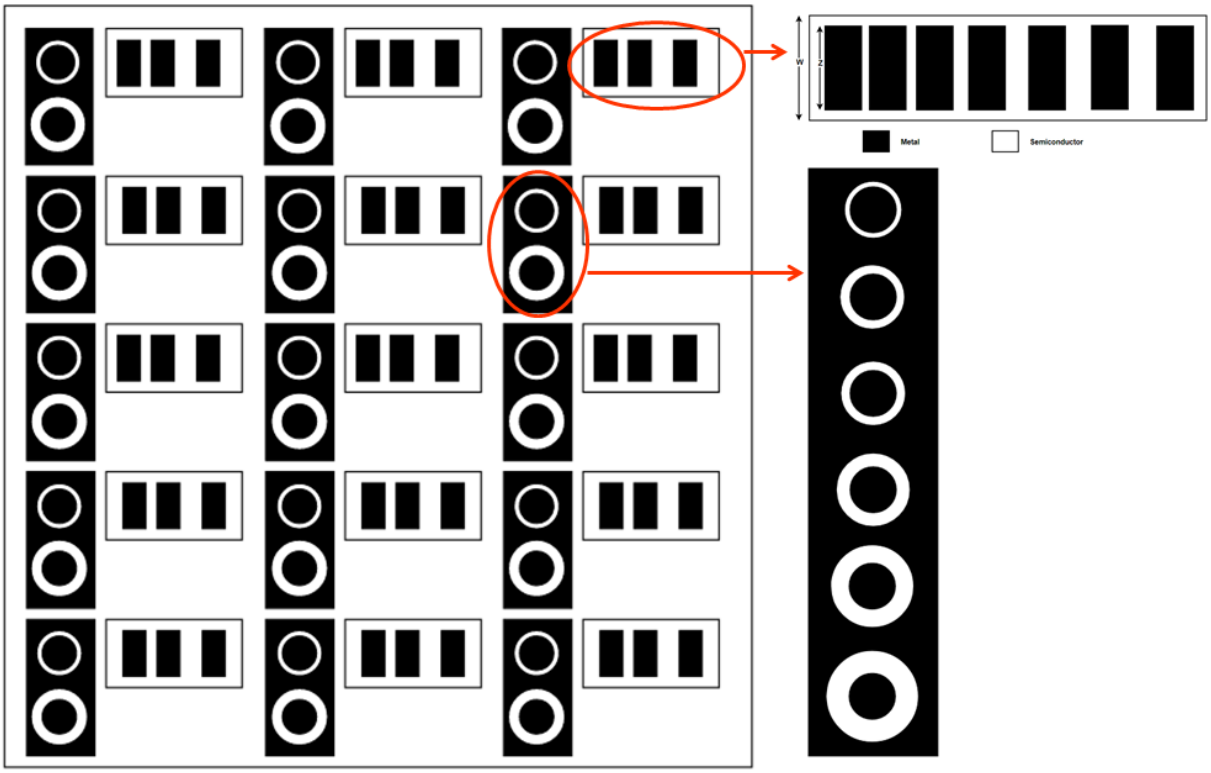

Fig. 4-37. Mask used for depositing both CTLM and LTLM on the devices.

The linear TLM IV curve is shown in Fig. 4-39. The circular TLM IV curve is shown in Fig. 4-40. It can be observed that IV curves from linear TLM are symmetric on both sides while the circular TLM looks linear in positive voltage range and looks schottky in negative voltage range. The symmetric nature of LTLM IV curve is due to the equal cross section area of metal contact pads where the voltage is applied. The asymmetric nature of CTLM IV curve is mainly due to the different contact area of the metal pads. The inner circular contact area is much smaller compared to the contact area outside the concentric circle. The contacts can be represented as schottky diode in parallel with resistance as shown in Fig. 4-38. The metal contact area of inner circle is much smaller causing higher resistance than outer metal contact which has much lower contact resistance.

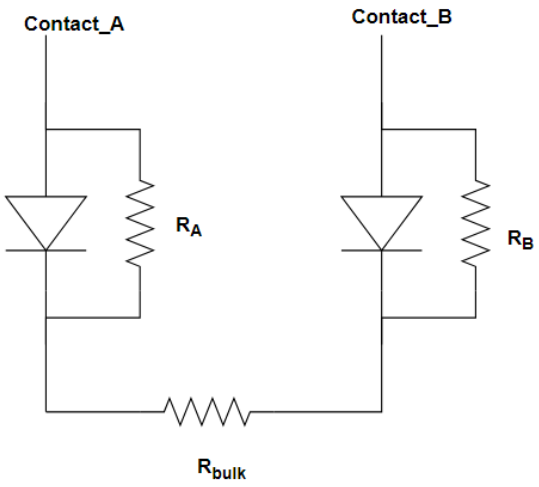

Fig. 4-38. Equivalent electrical circuit for two metal-semiconductor contact.

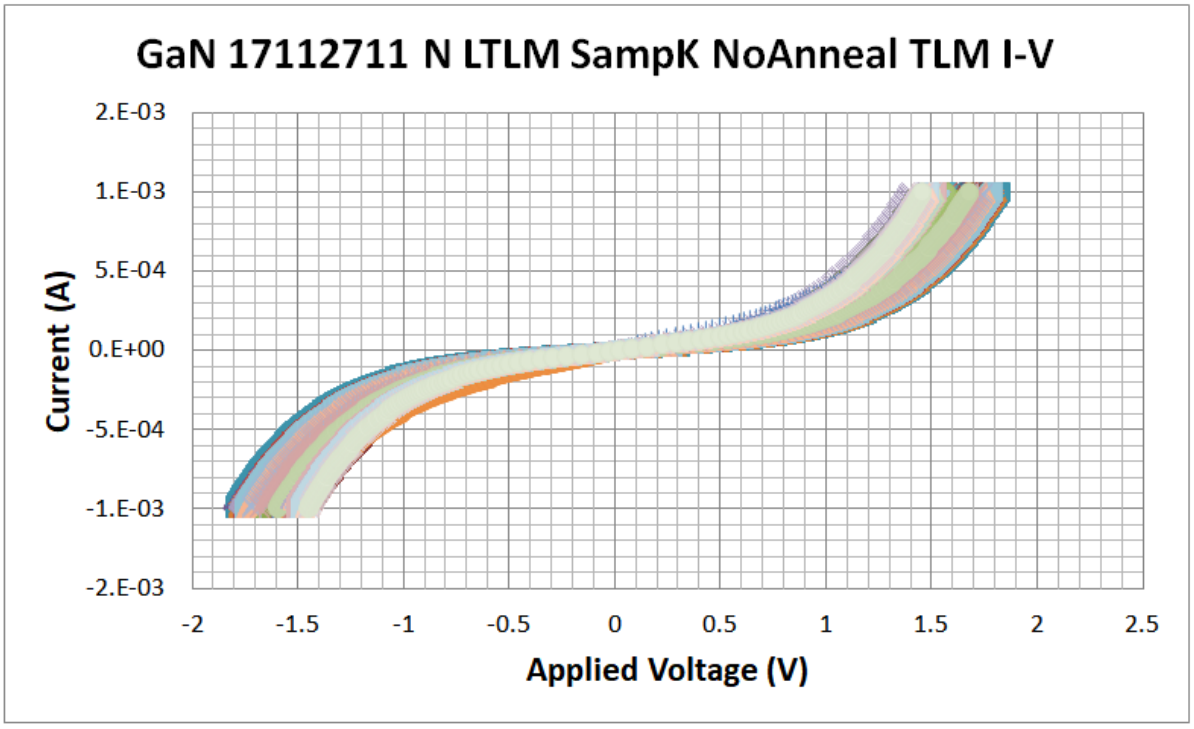

Fig. 4-39. IV of GaN 17112711 n-GaN Linear TLM of As-Deposited sample.

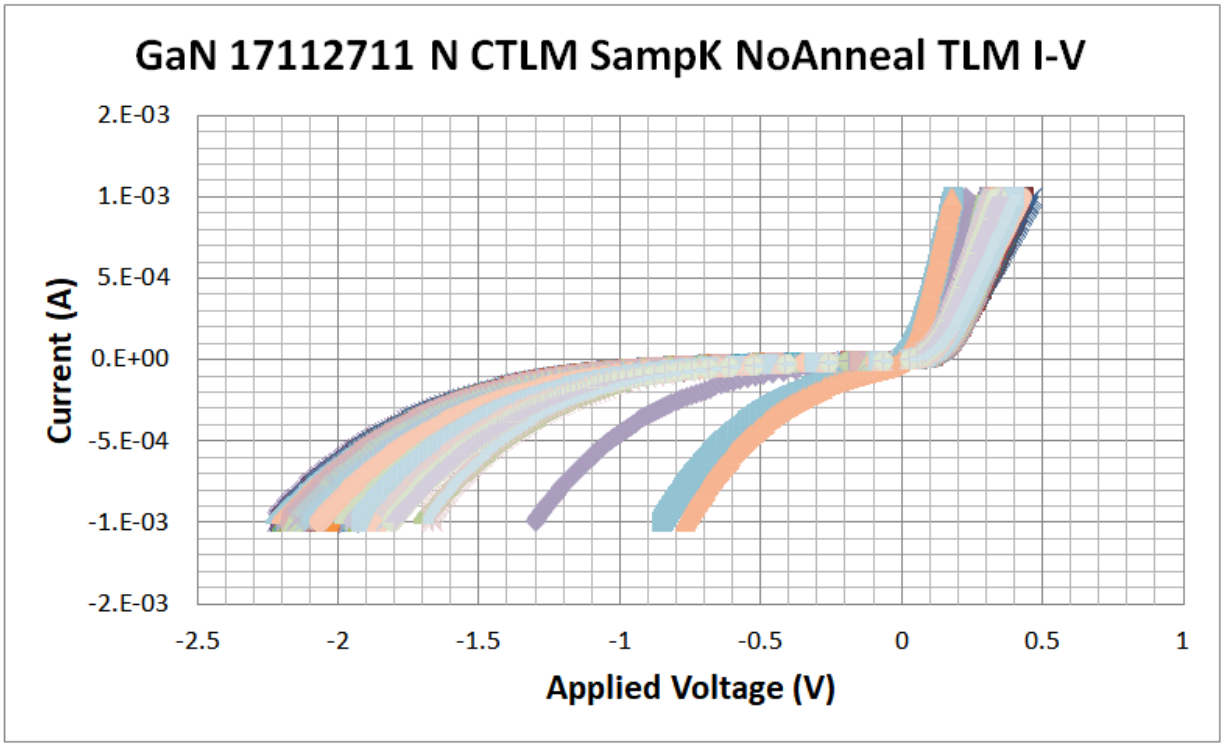

Fig. 4-40. IV of GaN 17112711 n-GaN Circular TLM of As-Deposited sample.

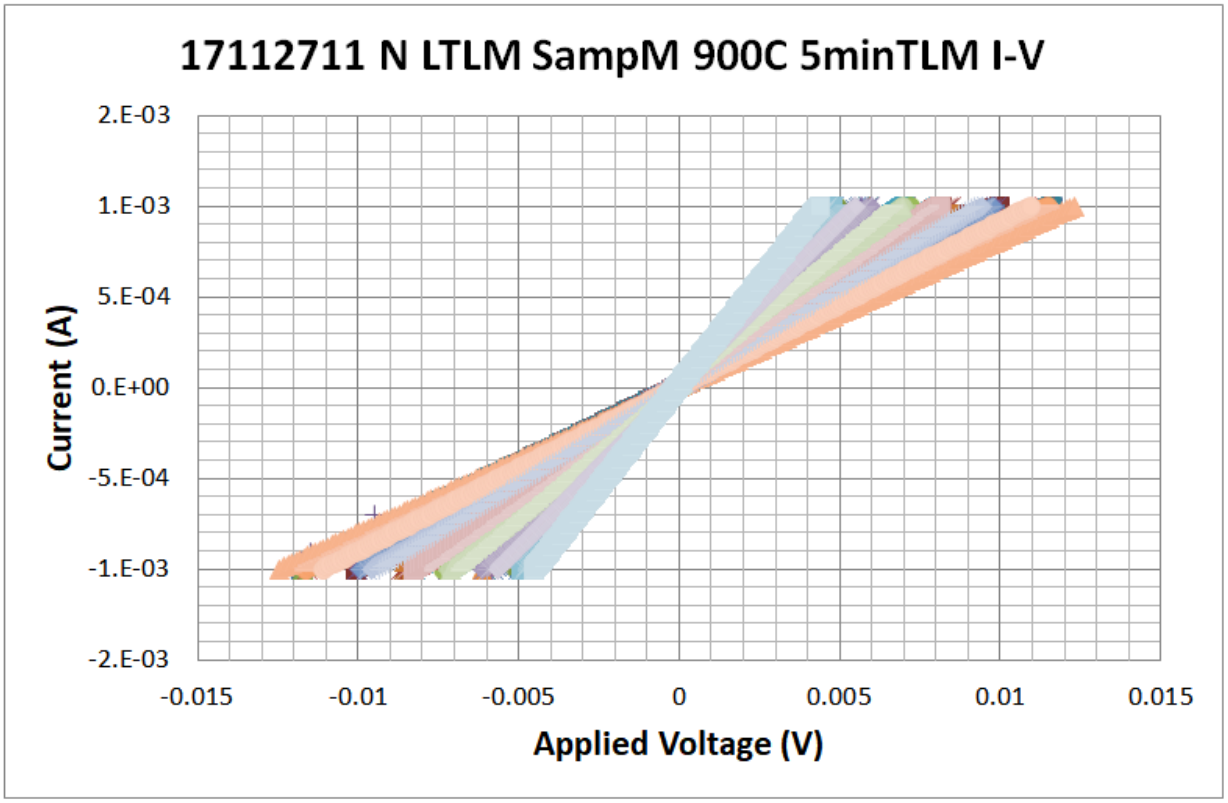

Fig. 4-41. IV of 17112711 n-GaN Linear TLM of annealing at 900°C in N_2 for 5min.

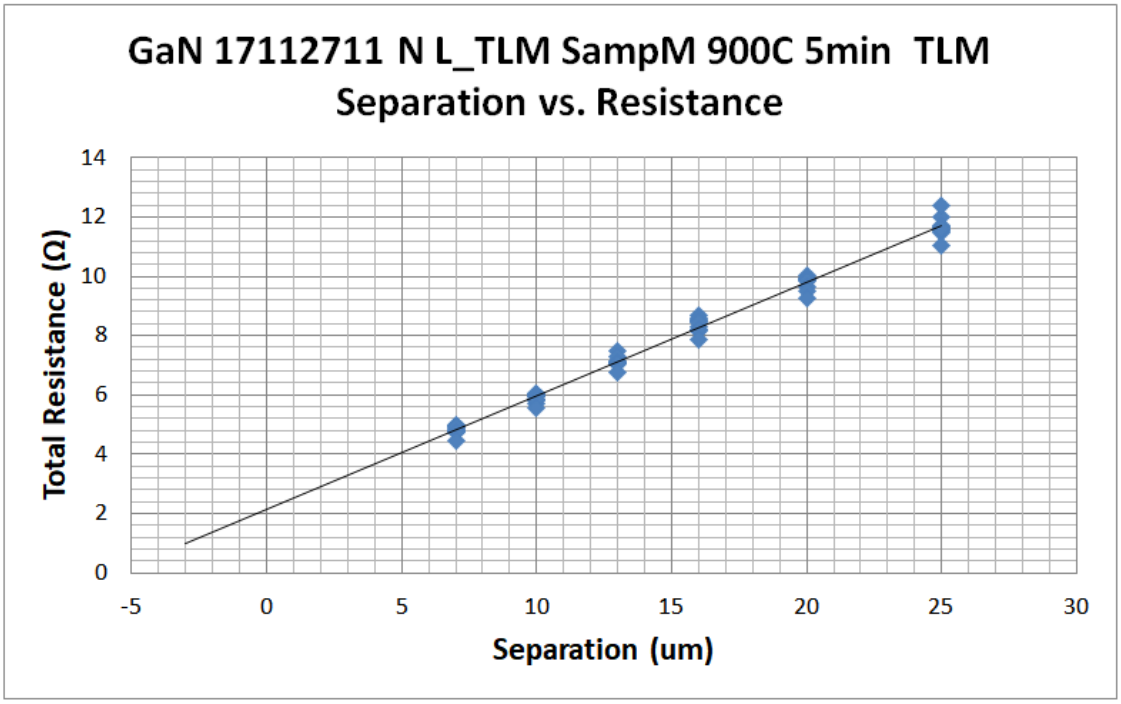

Fig. 4-42. TLM plot of 17112711 n-GaN Linear TLM Annealed at 900°C in N_2 for 5min.

The schottky contacts of the sample 17112711 were annealed at 900°C in N_2 for 5 min. These schottky IV curves became ohmic IV which can be seen in Fig. 4-41. These ohmic curves were used to obtain the total resistance for the different spacing conditions. The resistance was obtained from the IV curves and TLM plot is obtained as shown in Fig. 4-42. Annealing at 900°C has led to the reaction of Ti with GaN surface which makes the contact ohmic.

The samples of 17112721 had a n^{++} layer under the metal contact. These provided ohmic contact with As-Deposited samples due to the heavy doping of n^{++} layer. The IV curves of these samples can be seen in Fig. 4-43. The TLM curve for these linear samples can be seen in Fig. 4-44. These seem to well spread around the linear fit line.

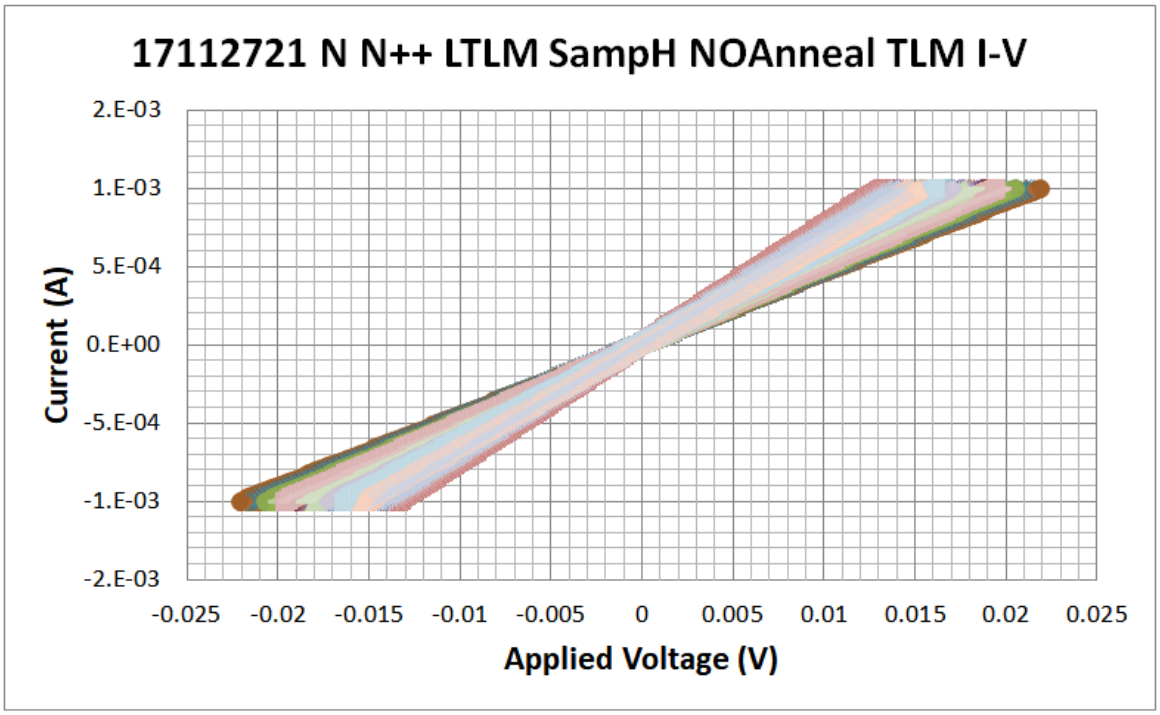

Fig. 4-43. IV of 17112721 n-GaN with n^{++} Linear TLM of As-Deposited sample.

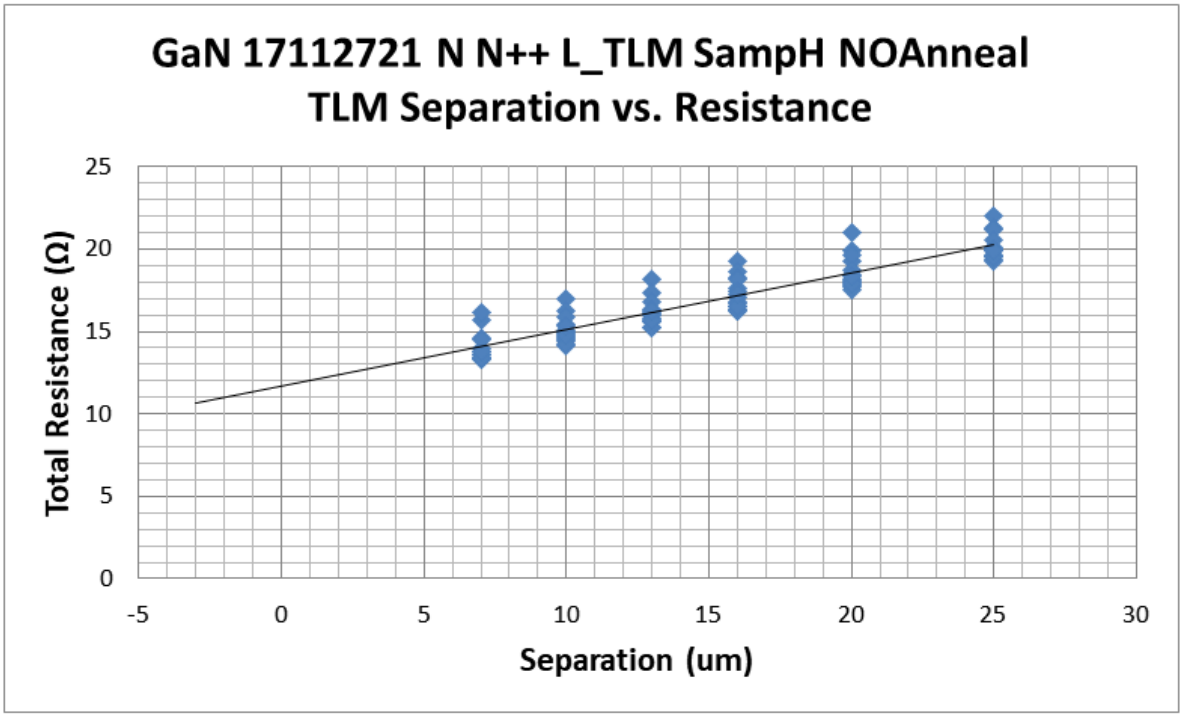

Fig. 4-44. TLM plot of 17112721 n-GaN with n^{++} Linear TLM of As-Deposited sample.

These samples were annealed were at 900°C and 300°C to check the effect of different annealing conditions. The IV curves of annealed samples at 300°C and 900°C are seen in Fig. 4-45 and Fig. 4-47 respectively. TLM plot for the annealing conditions at 300°C and 900°C can be seen in Fig. 4-46 and Fig. 4-48. It can be observed that the sample annealed at 300°C and 900°C both appear to be linear making it ohmic contacts. However, from the TLM plot, it can be inferred that the sample annealed at 300°C has become worse compared to As-Deposited sample while the sample annealed at 900°C seems to have become better and the points on the TLM graph are much closer validating that all contacts seem to be similar. The TLM plot of samples annealed at 300C have points well spread out and the slope of the TLM plot which should represent the sheet resistance of the device is much higher than the expected value which shows the invalidity of the points obtained from IV curves of samples annealed at 300°C. Hence, the samples need to be annealed at 900°C which is sufficient for the formation of TiN at the interface of Ti and GaN.

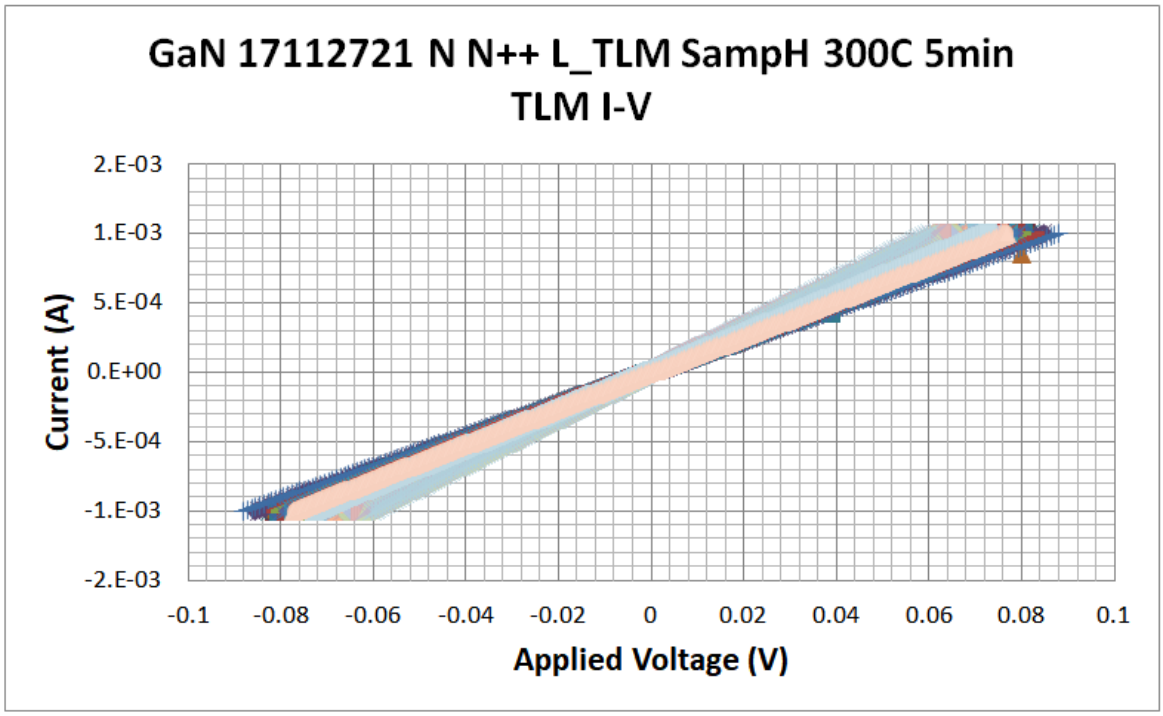

Fig. 4-45. IV of 17112721 n-GaN with n^{++} Linear TLM of annealing at 300°C in N_2 for 5min.

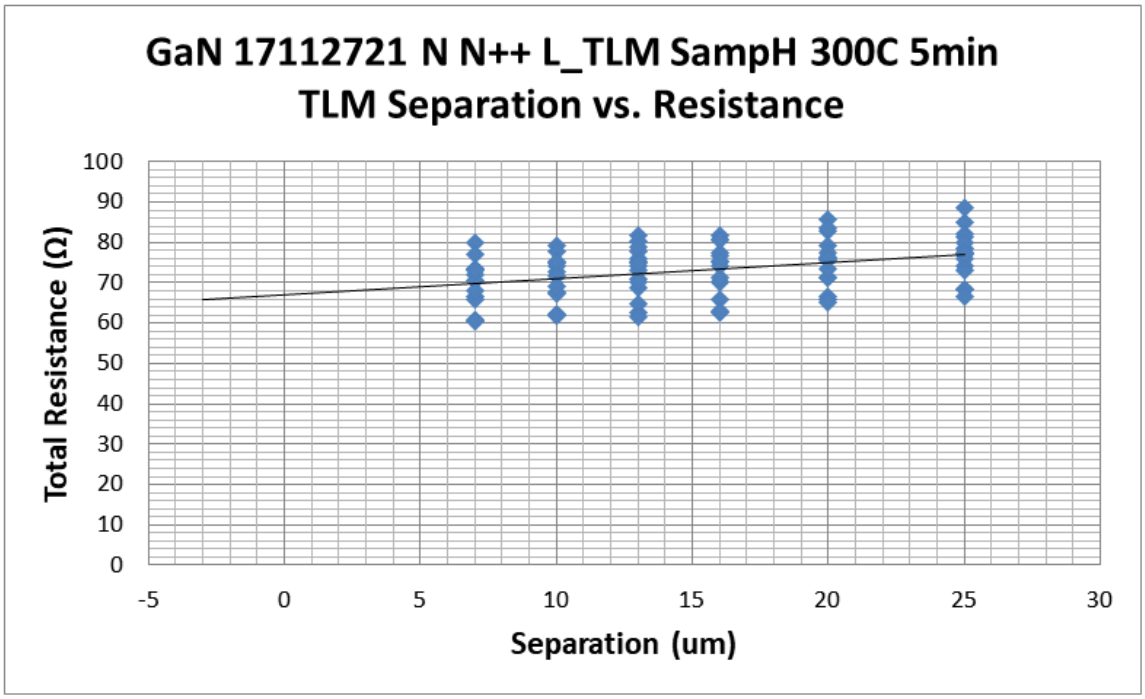

Fig. 4-46. TLM plot of 17112721 n-GaN with n^{++} Linear TLM Annealed at 300°C in N_2 for 5min.

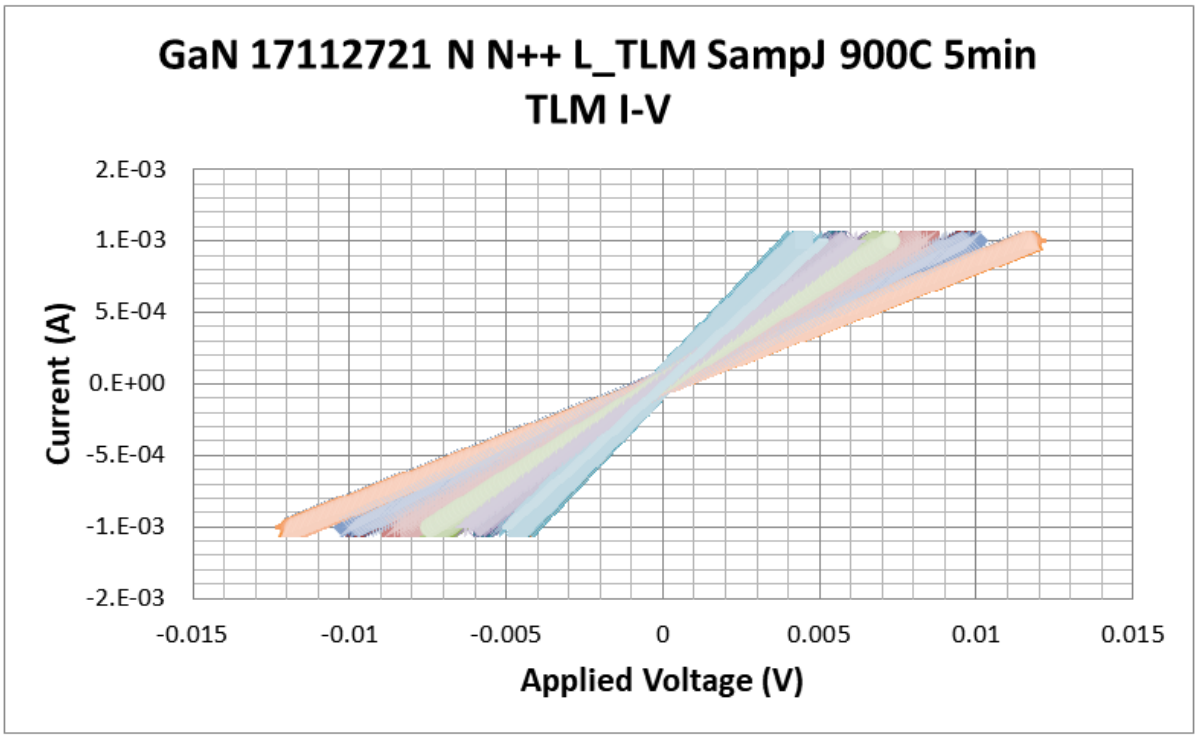

Fig. 4-47. IV of 17112721 n-GaN with n^{++} Linear TLM Annealed at 900°C in N_2 for 5min.

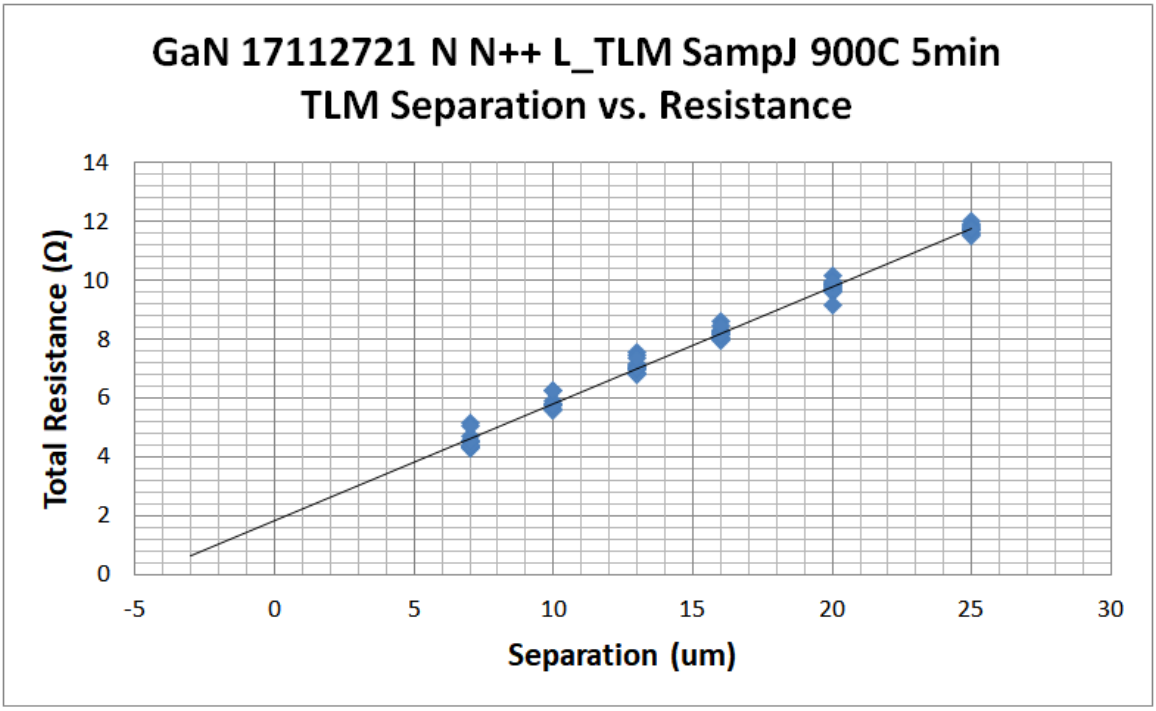

Fig. 4-48. TLM plot of 17112721 n-GaN with n^{++} Linear TLM Annealed at 900°C in N_2 for 5min.

The samples were etched after annealing to remove the n^{++} layer present in between the metal layer. The annealing was performed in RIE (Reactive Ion Etching) where etching is performed by the combination of BCl_3 and O_2. It was observed that the Ag silver present at the top of metallization has a reaction with the Chlorine leading to the etching of the top metal layer. Hence, Ag layer could be avoided in case etching needs to be carried out after the metallization process. The IV curve of n^{++} sample after etching is shown in Fig. 4-49. The TLM plot for these IV curves is shown in Fig. 4-50. It can be perceived that TLM points are more spread out than they were before etching. This shows that etching leads to certain surface impurities or defects that cause the spreading of the points in TLM curve.

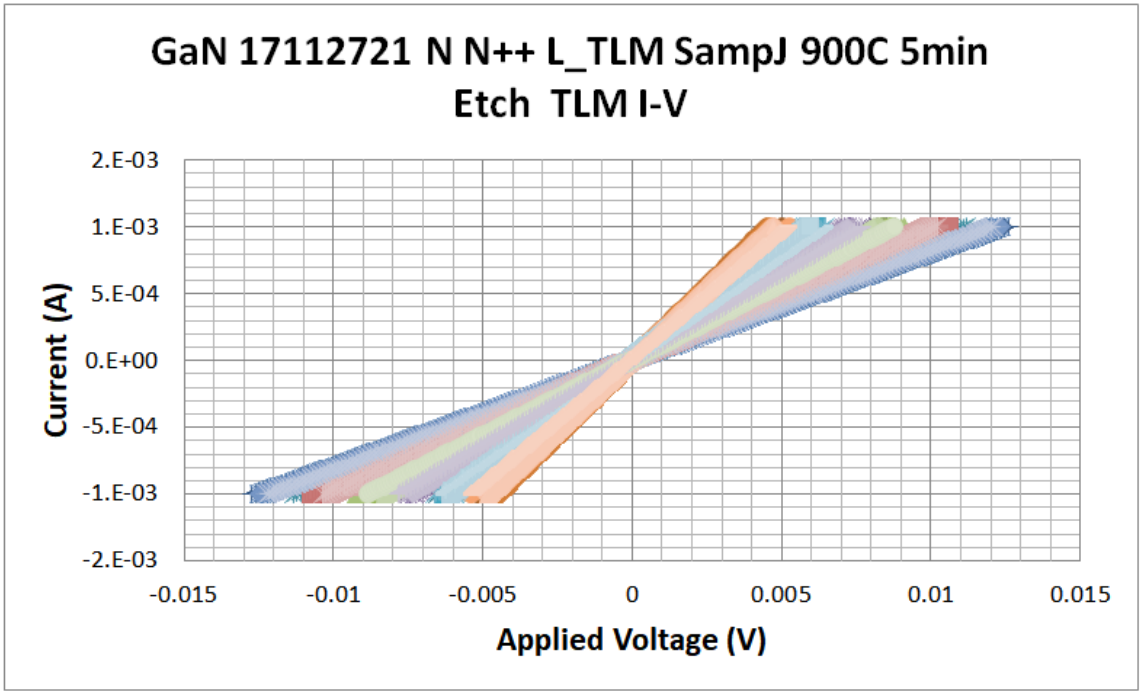

Fig. 4-49. IV of Linear TLM of 17112721 n-GaN with etched n^{++} layer Annealed at 900°C in N_2 for 5min.

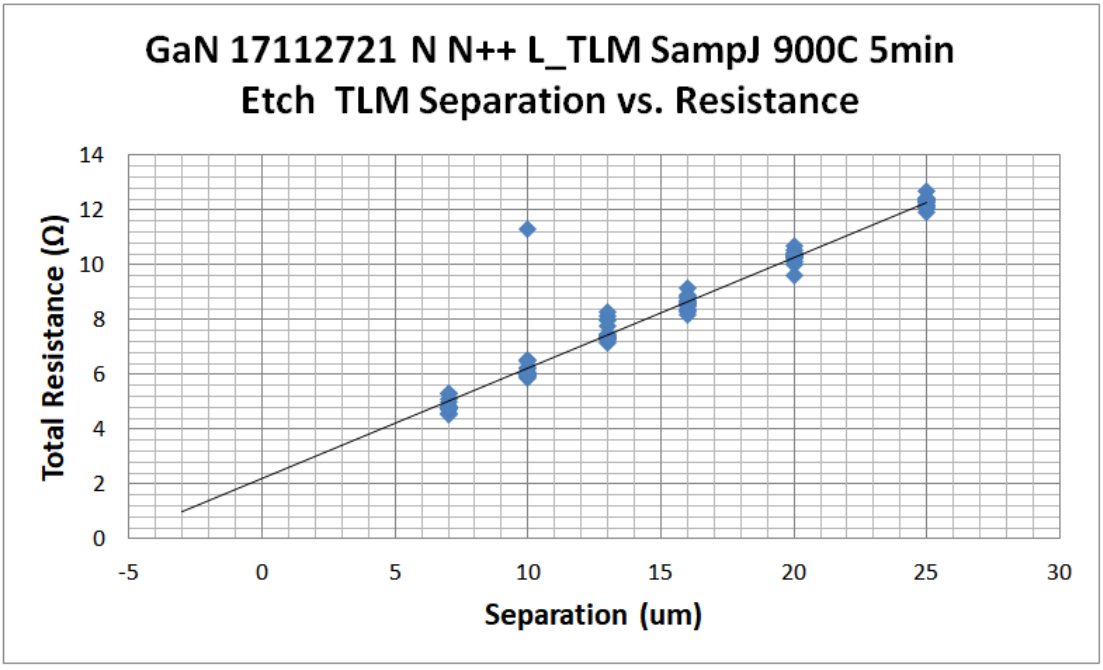

Fig. 4-50. TLM plot of Linear TLM of 17112721 n-GaN with etched n^{++} layer Annealed at 900°C in N_2 for 5min.

The parameters for Circular TLM pattern and linear TLM pattern are listed in TABLE 4-16 and TABLE 4-17 respectively. The sample without any values written in the table represents the non-linear IV curves or schottky metal contact. The R-squared value in the table represents the statistical measure of the closeness of the fit parameters to the actual data points. It can be observed that all ohmic contacts which have linear IV curves have a really good linear fit as the R^2 values are almost close to 0.99.

The table also includes the sheet resistance calculated using formula. It can be observed that the theoretical sheet resistance matches well with the parameters of CTLM than LTLM. This could be due to various reasons. LTLM fabrication has an etching step where the semiconductor is etched around the TLM pattern area in order to avoid the current spreading around the metal contact area. The LTLM pattern also has sharp rectangular corners which could cause current crowding at the edges leading to irregular current flow between the metal pads. In CTLM the current is applied between the concentric circles which do not have sharp edges for current crowding and the additional step is not necessary.

It can be verified from the fit parameters that the presence of n^{++} layer reduces the contact resistivity. Annealing at 900°C makes the contact better while annealing at 300°C makes the contact worse. It can be seen that etching of the samples has increased the contact resistivity by a slight bit which could be due to the surface roughening. The contact resistivity of CTLM is slightly less than LTLM which could be due to the current crowding factors which were discussed before.

TABLE 4-16. Circular TLM parameters extracted from practical device.

CTLM	Id	Fabrication Condition	Contact Resistance (Ω)	Transfer Length (um)	Sheet Resistance (Ω)	Theoretical Sheet Resistance (Ω)	Contact Resistivity (Ω-cm^2)	R^2
17112711	K	As-Deposited 300°C in N_2 5min	-	-	-	-	-	-
	M	As-Deposited	101.1265	76.96551	619.1699	160.0563	3.667E-02	0.996227
		900°C in N_2 5min	0.841661	2.523315	157.4682		1.01E-05	0.997785
		900°C in N_2 5min Etch	1.114313	3.248971	162.6004	166.7254	1.74E-05	0.99352
17112721	H	As-Deposited	4.897556	14.76676	159.9262	150.0528	3.47E-04	0.996291
		300°C in N_2 5min	45.94528	95.69186	226.2596		2.07E-02	0.989424
		300°C in N_2 5min Etch	44.12918	44.21674	470.3057	169.9897	9.20E-03	0.921774
	J	As-Deposited	4.481235	12.66569	167.655	150.0528	2.69E-04	0.996272
		900°C in N_2 5min	0.547838	1.488577	173.429		3.84E-06	0.996256
		900°C in N_2 5min Etch	0.60545	1.598271	178.5128	169.9897	4.56E-06	0.998327

TABLE 4-17. Linear TLM values extracted from the practical device.

LTLM	Id	Fabrication Condition	Contact Resistance (Ω)	Transfer Length (um)	Sheet Resistance (Ω)	Theoretical Sheet Resistance (Ω)	Contact Resistivity (Ω-cm^2)	R^2
17112711	K	As-Deposited 300°C in N_2 5min	-	-	-	-	-	-
	M	As-Deposited	2251.26	76.41137	11490.32	160.0563	6.7E-01	0.748204
		900°C in N_2 5min	1.057003	2.756948	149.868		1.14E-05	0.998295
		900°C in N_2 5min Etch	1.308929	3.388247	152.2958	166.7254	1.78E-05	0.996556
17112721	H	As-Deposited	5.709145	16.11483	139.4182	150.0528	3.60E-04	0.999134
		300°C in N_2 5min	34.26456	86.74261	155.0587		1.16E-02	0.994441
		300°C in N_2 5min Etch	34.83184	64.51282	210.5693	169.9897	8.76E-03	0.998042
	J	As-Deposited	5.441392	14.02848	152.3703	150.0528	2.98E-04	0.998498
		900°C in N_2 5min	0.905884	2.287368	155.402		8.39E-06	0.998904
		900°C in N_2 5min Etch	0.832471	1.914803	169.5545	169.9897	6.22E-06	0.998588

5 Summary and Conclusions

5.1 Summary

This research work focuses mainly on modeling the metal-semiconductor interface in Sentaurus TCAD and characterization of contacts on n-type GaN devices. The simulation has been performed to compare the contact resistance of the devices (experimental results) with the simulation. Effect of reducing the contact resistivity due to the presence of a heavily doped semiconductor (n^{++}) layer under the metal contact has been studied in this work. The simulations have been conducted for different thickness and doping of n^{++} layer. Based on the simulation results and requirement of reduction in contact resistivity, particular doping condition and thickness has been chosen for testing it practically.

It was observed from simulations that 20nm thick layer of n^{++} helped reduce the contact resistivity to a greater extent than n^{++} layer of any higher thickness. A practical device with bulk semiconductor doping of 1e18 cm^{-3} was grown with n^{++} layer of 1.2e19 cm^{-3} of 20nm thickness was grown. This device was provided with ohmic contact with metallization structure of Ti/Al/Ni/Ag. It was observed that this thin layer of n^{++} reduced the contact resistivity from 3.67e-2 Ω-cm^2 to 2.7e-4 Ω-cm^2 without annealing. Hence, when the metal is As-Deposited, the contact resistivity reduces by an order of 2. However, on annealing at 900°C, the contact resistivity of bulk layer decreased rapidly to 1.01e-5 Ω-cm^2. The n^{++} layer device had a contact resistivity of 3.84e-6 Ω-cm^2. It was also observed annealing at 300°C lead to much higher contact resistivity. The structure with n^{++} layer had a contact resistivity of 2.07e-2 Ω-cm^2 which is much higher than the case when annealing was not performed with a value of 2.69e-4 Ω-cm^2. Appropriate annealing temperatures and annealing conditions could result in significant reduction in contact resistivity which could lead to significant reduction of voltage drop and power loss at the interface.

It was also observed that the etching of surface had negligible effect on contact resistivity at the interface. Etching of the surface had caused the contact resistivity to very slightly increase from 1.01e-5 Ω-cm^2 to 1.74e-5 Ω-cm^2 for bulk layer while for the structure with n^{++}, it changed from 3.84e-6 Ω-cm^2 to 4.56e-6 Ω-cm^2 which is a very small increase.

5.2 Conclusions

There is not significant research work available which focuses on modeling of the metal contacts on semiconductor to reduce contact resistivity as most of the device modeling research assumes the contacts to be ohmic with negligible or predefined small contact resistance. This however neglects the characteristics of the metal-semiconductor interface. The current work focuses on the metal-semiconductor interface with focus on physics at interface and provides a better understanding of the contact parameters. The presence of a heavily doped layer at metal-semiconductor interface for making the metal contact ohmic is a well-established concept in semiconductors. However, notable research has not been published which focuses on this concept for Gallium Nitride devices. Hence this research work focuses on the modeling of the metal-semiconductor interface understanding the physics involved at the interface and trying to reduce the contact resistivity for n-type GaN devices.

It was noted that the n^{++} layer needs to be grown only under the metal contact to avoid perturbing the sheet resistance of the device as the purpose of the heavily doped layer is to just reduce the contact resistance and also there could be gate terminal between the metal contacts as in MOSFET where it is not possible to have this heavily doped layer in between the metal contacts of source and drain. Simulation results showed that the thickness of the n^{++} layer when increased beyond certain limit did not further reduce the contact resistivity which could be due to the fact when the thickness of n^{++} is extended beyond the depletion width at the interface of the metal-semiconductor junction no significant reduction in resistivity is observed. It was also noted that higher the ratio of the doping of n^{++} layer compared to the bulk of the semiconductor, higher is the amount of reduction in contact resistivity which is due to better current tunneling at heavier doping of the n^{++} layer.

As discussed before, it was observed that the annealing conditions play a major role in the reduction of the contact resistivity. At annealing temperatures around 900°C, [17] it has been reported that Ti layer reacts with GaN to form the intermediate layer of TiN which leads to the reduction in contact resistivity. This validates the results observed from testing that annealing the devices at 900°C made the devices better while annealing temperature of 300°C made the device worse. Etching of the devices showed that the contact parameters were unaffected which can be

attributed to the fact that surface damage to semiconductor or surface impurities does not affect the interface of the metal and semiconductor.

From the perspective of fabrication, CTLM is easier to fabricate as LTLM needs additional etching step and a metallization process for that. The testing results also helped in concluding that the CTLM pattern gives a better characterization of the device than LTLM pattern which was inferred based on the calculated sheet resistances. Hence, it is much better to use CTLM for characterization of the contacts.

Hence, it can be concluded that the presence of heavily doped layer under the metal contact with doping more than 10 times bulk doping along with the thickness of around 20 nm (as the layer is heavily doped, it can have smaller depletion width) could reduce the contact resistivity by an order of 2 when metal contacts are not annealed. However, annealing leads to significant reduction of contact resistivity. Contact resistivity reduces by a factor of 2 or more under annealed conditions.

Hence, the presence of this additional n++ layer makes the metal contact ohmic without thermal treatment and improves the contact properties namely contact resistivity even after thermal treatment.

5.3 Future Work

GaN p-n junction diodes are not yet commercialized due to the major problem of very high contact resistivity of p-GaN. GaN being a wide band-gap semiconductor needs a metal with work-function of 7.5eV to provide ohmic contact on p-type GaN which does not exist. The most predominantly used metal contact for p-GaN is Palladium (Pd) with work-function of 5.8 eV. Experimentally it has been observed that annealing of Pd contacts at a temperature around 700-900°C in gases like N_2 or Argon converts the schottky contacts into ohmic contacts. These annealed contacts have high contact resistivity in the order of milliohms which leads to significant voltage drops or power loss. Hence, it is not advisable to use such contacts for commercial purposes. Attempts are being made to figure out ways to reduce the contact resistivity for p-GaN. Modeling of the metal-semiconductor interface along with better understanding of the physics of annealing could help in figuring out solutions so that the contact resistivity of p-type GaN contacts could be reduced to the order to 1e-5 to 1e-6 like contact to n-

type GaN. This would provide immense help in developing GaN p-n diodes that could provide very high blocking voltages and power density compared to silicon Devices. These low resistance contacts on p-GaN could lead to even better utilization of GaN material.

This work can be further extended into various steps as follows

1. Understanding the effect of annealing and interface chemical reaction at annealing temperatures at metal contacts.
2. Modeling of traps and surface impurities in TCAD Sentaurus.
3. Using TCAD Sentaurus Process which can simulate the growth and fabrication conditions to have a much closer perspective to the actual growth instead of using Structure Editor for getting the device structure.
4. Simulations of the structure can be carried in 3 dimensions for better accuracy (which need super-computers).
5. Modeling of surface recombination centers, trap densities at interface and bulk of the semiconductor to better understand the practical device.

The work can be further extended into analysis of the contact impedance parameters like capacitance and inductance instead of just contact resistivity. As the device keep getting smaller and smaller, the effect of the reactive parameters on the device operation is increasing and it needs to be studied as well to help improve the switching properties of the devices as well.

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Appendix A: Derivation of Equation of CTLM and Correction Factor

The equation of Circular TLM is obtained using Marlow and Das pattern[30]. The equation for CTLM is derived to understand the parameters[31]. The derivation of CTLM is conducted to obtain the total resistance between thee metal contacts as function of spacing of metal contacts.

$$R_T = f(d) \tag{1}$$

Various parameters used in this derivation are

ρ_c- Specific contact resistivity

Rsk – beneath sheet resistance

x- Radius of a contact element of width dx.

V(x) – voltage drop across contact interface at x

I(x) – Current beneath the contact at x

The current gradient occurs across the contact of the metal-semiconductor interface. The current gradient is given by conductance element which is given by $\frac{2\pi x * dx}{\rho_c}$

$$\frac{di}{dx} = \frac{2\pi x V(x)}{\rho_c} \tag{2}$$

As the majority of the voltage drop occurs across the bulk of the semiconductor layer,

$$\frac{dV}{dx} = \frac{R_{sh} i(x)}{2\pi x} \tag{3}$$

The series resistance element is given by $\frac{R_{sk} * dx}{2\pi x}$. Combining the two equations to eliminate the current term i(x),

$$di = \frac{V(x)}{\rho_c / 2\pi x dx};\ dV = \frac{R_{sh} dx}{2\pi x} * i(x)$$

$$\frac{d}{dx}\left[\frac{2\pi x}{R_{sh}} * \frac{dV}{dx}\right] = \frac{2\pi V(x) \cdot x}{\rho_c}$$

$$\frac{d}{dx}\left[\frac{x}{R_{sh}} * \frac{dV}{dx}\right] = \frac{Vr}{\rho_c}$$

$$x * \frac{d^2V}{dx^2} + \frac{dV}{dx} = \frac{R_{sh}Vr}{\rho_c}$$

$$\frac{d^2V}{dx^2} + \frac{1}{x}\frac{dV}{dx} - \frac{V}{{L_t}^2} = 0 \tag{4}$$

$$L_t = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{5}$$

The parameter transfer length is defined as the square root of contact resistance per sheet resistance. The transfer length is the effective length which more than 63% of current transfers from metal to semiconductor or semiconductor to metal. The radius of the contact element is a large quantity. Hence, the second term with x in the denominator can be neglected as it contributed very less to the differential. The equation can be simplified as Eq. (6).

$$\nabla^2 V - k^2 \cdot V = 0 \tag{6}$$

Where,

$$k^2 = \frac{1}{{L_t}^2} = \frac{R_{sh}}{\rho_c} \tag{7}$$

Based on the mathematical equation the solution to this equation is given by

$$V(x) = C_1 I_0(kx) + C_2 K_0(kx)$$

Where I_0 and K_0 are Bessel functions of n-th order

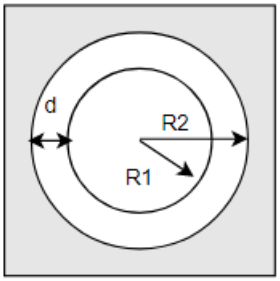

Fig. A-1. Simplified CTLM model based on Marlow and Das.

$$\Delta V = \frac{i_0 R_{sh}}{2\pi}\left[ln\frac{r_2}{r_1} + \frac{L_T}{r_1}\cdot\frac{I_0\left({}^{r_1}/_{L_T}\right)}{I_1\left({}^{r_1}/_{L_T}\right)} + \frac{L_T}{r_2}\cdot\frac{K_0\left({}^{r_2}/_{L_T}\right)}{K_1\left({}^{r_2}/_{L_T}\right)}\right] \quad (8)$$

Where,

r_1- Radius of inner circle

r_2- Radius of outer circle

i_0- Constant current applied between the metal contacts

ΔV- Voltage difference between the metal contacts under consideration

Hence, total resistance is given by

$$R_T = \frac{\Delta V}{i_0} = \frac{R_{sh}}{2\pi}\left[ln\frac{r_2}{r_1} + \frac{L_T}{r_1}\cdot\frac{I_0\left({}^{r_1}/_{L_T}\right)}{I_1\left({}^{r_1}/_{L_T}\right)} + \frac{L_T}{r_2}\cdot\frac{K_0\left({}^{r_2}/_{L_T}\right)}{K_1\left({}^{r_2}/_{L_T}\right)}\right] \quad (9)$$

In cases where,

$${}^{r_1}/_{L_T} \geq 4 \;\&\; {}^{r_2}/_{L_T} \geq 4$$

$\frac{I_0}{I_1}$ and $\frac{K_0}{K_1}$ are unity

Hence,

$$R_T = \frac{R_{sh}}{2\pi}\left[ln\frac{r_2}{r_1} + L_T\left(\frac{1}{r_1} + \frac{1}{r_2}\right)\right] \quad (10)$$

Rewriting,

$$R_T = \frac{R_{sh}}{2\pi}\left[ln\frac{r_1 + d}{r_1} + L_T\left(\frac{1}{r_1 + d} + \frac{1}{r_1}\right)\right] \quad (11)$$

Where, d – distance of the spacing between the two concentric circles

When, $r_1, r_2 \gg d$, Equation becomes

$$R_T = \frac{R_{sh}}{Z}[d + 2L_T] \quad (12)$$

Where,

$$Z = 2\pi r_1$$

And equation becomes similar to LTLM total resistance equation.

The assumption of spacing being much larger than the radius of the inner circle may not be true for all conditions. Hence, we introduce a correction factor that could be applied in cases where the assumption becomes invalid. Derivation of the correction factor for CTLM is as follows[24].

$$R_T = \frac{R_{sh}}{2\pi}\left[ln\frac{r_1 + d}{r_1} + L_T\left(\frac{1}{r_1 + d} + \frac{1}{r_1}\right)\right] \quad (13)$$

$$R_T = \frac{R_{sh}}{2\pi r_1}[d + 2L_T] \cdot C \quad (14)$$

Where,

$$C = \frac{r_1}{d} \cdot ln\frac{r_1 + d}{r_1} \quad (15)$$

Appendix B: GaN Parameter File

```
************************** Dielectric Constant: *************************
*************************************************************************
Epsilon
{                   epsilon = 8.9 # [1]      }
Epsilon_aniso
{                   epsilon = 10.4 # [1]     }

************************** Lattice Heat Capacity: ************************
*************************************************************************
LatticeHeatCapacity
{
        * lumped electron-hole-lattice heat capacity
        * cv() = cv + cv_b * T + cv_c * T^2 + cv_d * T^3
                cv = 3.0 # [J/(K cm^3)]
                cv_b = 0.0000e+00 # [J/(K^2 cm^3)]
                cv_c = 0.0000e+00 # [J/(K^3 cm^3)]
                cv_d = 0.0000e+00 # [J/(K^4 cm^3)]
}

************************** Thermal Conductivity: *************************
*************************************************************************
Kappa
{
        * Lattice thermal conductivity
                Formula = 1
        * Formula = 1:
        * kappa() = kappa + kappa_b * T + kappa_c * T^2

                kappa = 1.3 # [W/(K cm)]
                kappa_b = 0.0000e+00 # [W/(K^2 cm)]
                kappa_c = 0.0000e+00 # [W/(K^3 cm)]
```

```
}

****************************** Hydro Parameters *************************
*********************************************************************
EnergyFlux
{
        * Coefficient in front of the energy flux equation
        * energy_flux_coef=0.6 corresponds to Stratton model

                energy_flux_coef_ele = 0.6 # [1]
                energy_flux_coef_hol = 0.6 # [1]
}

ThermalDiffusion
{
        * Thermal diffusion factor (0 <= td <= 1)
        * td=0. corresponds to Stratton model

                td_n = 0.0000e+00 # [1]
                td_p = 0.0000e+00 # [1]
}

HeatFlux
{
        * Heat flux factor (0 <= hf <= 1)
        * Heat flux plays some role in the vertical reach of hot carriers.
        * The values of hf below are NOT calibrated

                hf_n = 1.0 # [1]
                hf_p = 1.0 # [1]
}

AvalancheFactors
```

```
{
        * Coefficientss for avalanche generation with hydro
        * Factors n_l_f, p_l_f for energy relaxation length in the expressions
        * for effective electric field for avalanche generation
        * eEeff = eEeff / n_l_f ( or b = b*n_l_f )
        * hEeff = hEeff / p_l_f ( or b = b*p_l_f )
        * Additional coefficients n_gamma, p_gamma, n_delta, p_delta

                n_l_f = 0.8 # [1]
                p_l_f = 0.8 # [1]
                n_gamma = 0.0000e+00 # [1]
                p_gamma = 0.0000e+00 # [1]
                n_delta = 0.0000e+00 # [1]
                p_delta = 0.0000e+00 # [1]
}

**************************** Bandgap ***********************************
************************************************************************
Bandgap
{
        * Eg = Eg0 + alpha Tpar2 / (beta + Tpar) - alpha T2 / (beta + T)
        * Parameter 'Tpar' specifies the value of lattice
        * temperature, at which parameters below are defined
        * Chi0 is electron affinity.

                Chi0 = 4.1 # [eV]
                Bgn2Chi = 0.5 # [1]
                Eg0 = 3.47 # [eV]
                alpha = 9.39e-04 # [eV K^-1]
                beta = 772 # [K]
                Tpar = 0.0000e+00 # [K]
}

eDOSMass
```

```
{
        * For effective mass specificatition Formula1 (me approximation):
        * or Formula2 (Nc300) can be used :
        Formula = 2 # [1]
        * Formula2:
        * me/m0 = (Nc300/2.540e19)2/3
        * Nc(T) = Nc300 * (T/300)3/2

                Nc300 = 2.3e18 # [cm-3]
        * mass=0.222*mo
}

hDOSMass
{
        * For effective mass specificatition Formula1 (mh approximation):
        * or Formula2 (Nv300) can be used :
        Formula = 2 # [1]
        * Formula2:
        * mh/m0 = (Nv300/2.540e19)2/3
        * Nv(T) = Nv300 * (T/300)3/2

                Nv300 = 4.6e19 # [cm-3]
        *mass=1.0*mo
}

*****************************************************************************
* Doping
*****************************************************************************
***************************** Mobility Models: ***************************
        * mu_lowfield^(-1) = mu_dop(mu_max)^(-1) + mu_Enorm^(-1) + mu_cc^(-1)
        * Variable = electron value , hole value
        # [units]
*****************************************************************************
ConstantMobility:
```

```
{
        * mu_const = mumax (T/T0)^(-Exponent)

                mumax = 1500 ,170 # [cm2/(Vs)]
                Exponent = 1 ,5.0 # [1]
                mutunnel        = 0.05,                                 0.05
}
DopingDependence:
{
        * For doping dependent mobility model three formulas
        * can be used. Formula1 is based on Masetti et al. approximation.
        * Formula2 uses approximation, suggested by Arora.
        formula = 1 ,1 # [1]
        * If formula=1, model suggested by Masetti et al. is used:
        * mu_dop = mumin1 exp(-Pc/N) + (mu_const - mumin2)/(1+(N/Cr)^alpha)
        * - mu1/(1+(Cs/N)^beta)
        * with mu_const from ConstantMobility

                mumin1 = 85,33                          # [cm2/Vs]
                mumin2 = 75,0.00E+00                            # [cm2/Vs]
                mu1 = 50,20                     # [cm2/Vs]
                Pc = 6.50E+15,5.00E+15                          # [cm3]
                Cr = 9.50E+16,8.00E+16                          # [cm3]
                Cs = 7.20E+19,8.00E+20                          # [cm3]
                alpha = 0.55, 0.55                      # [1]
                beta = 0.75,0.7                         # [1]

        * If formula=2, model suggested by Arora is used:
        ***** Not Callibrated *****
        ***** Parameters Below are for InN *****
        * mu_dop = muminA + mudA/(1.+(N/N00)^AA),
        * where muminA=Ar_mumin*(T/T0)^Ar_alm; mudA = Ar_mud*(T/T0)^Ar_ald
        * N is net doping
        * N00=Ar_N0*(T/T0)^Ar_alN; AA = Ar_a*(T/T0)^Ar_ala
```

```
}

HighFieldDependence:
{
        * Caughey-Thomas model:
        * mu_highfield = mu_lowfield / ( 1 + (mu_lowfield E / vsat)^beta )1/beta
        * beta = beta0 (T/T0)^betaexp.

                beta0 = 0.9 ,0.8 # [1]
                betaexp = 0.0000e+00 ,0.0000e+00 # [1]

        * Smoothing parameter for HydroHighField Caughey-Thomas model:
        * if Tl < Tc < (1+K_dT)*Tl, then smoothing between low field mobility
        * and HydroHighField mobility is used.

                K_dT = 0.01 ,0.01 # [1]

        * Transferred-Electron Effect:
        * mu_highfield = (mu_lowfield+(vsat/E)*(E/E0_TrEf)4)/(1+(E/E0_TrEf)4)

                E0_TrEf = 1.5000e+05 ,1.5000e+05 # [1]
                Ksmooth_TrEf = 1 ,1 # [1]

        * For vsat either Formula1 or Formula2 can be used.
                Vsat_Formula = 2 ,2 # [1]

        * Formula2 for saturation velocity:
        * vsat = A_vsat - B_vsat*(T/T0)
        * (Parameter Vsat_Formula has to be equal to 2):
        * Obs: experiments seem to confirm a lower vsat for the 2D electron gas than bulk
                A_vsat = 2.6e7 ,2.6e+07 # [1]
                B_vsat = 0 , 0 # [1]
                vsat_min = 5.000e+05 ,5.000e+05 # [1]
```

```
}

****************** Recombination/Generation Models: **********************
* Variable = electron value , hole value
# [unit]
*******************************************************************************
Scharfetter * relation and trap level for SRH recombination:
{
        * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma
        * tau(T) = tau * ( (T/300)^Talpha ) (TempDep)
        * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)

                taumin = 0.0000e+00 ,0.0000e+00 # [s]
                taumax = 1.0000e-11 ,1.0000e-11 # [s]
                Nref = 1.0000e+16 ,1.0000e+16 # [cm^(-3)]
                gamma = 1 ,1 # [1]
                Talpha = -1.5000e+00 ,-1.5000e+00 # [1]
                Tcoeff = 2.55 ,2.55 # [1]
                Etrap = 0.0000e+00 # [eV]
}
vanOverstraetendeMan * Impact Ionization:
{
        * G_impact = alpha_n n v_drift_n + alpha_p p v_drift_p
        * with alpha = gamma a exp(-b gamma/E) for E<E0 (low) and E>E0 (high)
        * with gamma = tanh(hbarOmega/(2kT0)) / tanh(hbarOmega/(2kT))

                a(low) = 1.143e+07 ,1.3400e+08 # [1/cm]
                a(high) = 1.143e+07 ,1.3400e+08 # [1/cm]
                b(low) = 3.4e+07 ,2.0300e+07 # [V/cm]
                b(high) = 3.4e+07 ,2.0300e+07 # [V/cm]
                E0 = 4.0000e+05 ,4.0000e+05 # [V/cm]
                hbarOmega = 0.035 ,0.035 # [eV]
}
```

```
QuantumPotentialParameters
{
        * gamma: weighting factor for quantum potential
        * theta: weight for quadratic term
        * xi: weight for quasi Fermi potential
        * eta: weight for electrostatic potential

                gamma = 1.41,1.4 # [1]
                theta = 0.5 ,0.5 # [1]
                xi = 1 ,1 # [1]
                eta = 1 ,1 # [1]
}

Auger * coefficients:
{
        * R_Auger = ( C_n n + C_p p ) ( n p - ni_eff^2)
        * with C_n,p = (A + B (T/T0) + C (T/T0)^2) (1 + H exp(-{n,p}/N0))

                A = 1.0000e-30 ,1.0000e-30 # [cm^6/s]
                B = 0.0000e+00 ,0.0000e+00 # [cm^6/s]
                C = 0.0000e+00 ,0.0000e+00 # [cm^6/s]
                H = 0.0000e+00 ,0.0000e+00 # [1]
                N0 = 1.0000e+18 ,1.0000e+18 # [cm^(-3)]
}

RadiativeRecombination * coefficients:
{
        * R_Radiative = C (n p - ni_eff^2)

                C = 1.1000e-8 # [cm^3/s]
}
BarrierTunneling
{
        mt = 0.01, 0.026
```

```
        g = 1 , 1
}
HurkxTrapAssistedTunneling
{
        mt = 0.5, 0.5
}

***************************************************
*Ionization
***************************************************
Ionization
      {
      NaCrit          =       9.0000e+17
      NdCrit          =       9.0000e+17

                  Species ("nSiliconActiveConcentration") {

            E_0         =      0.100
            alpha       =      2.50e-08
            g           =     2.0
            Xsec        =      1.0000e-12
                                        }
          Species ("PDopantActiveConcentration") {
            E_0         =      0.326
            alpha       =      0
            g           =     4.0
            Xsec        =      1.0000e-12
                                }
                      }
```

Appendix C: Device Structure File

```
(sde:clear)

;Defining the parameters of device dimensions
;Device is supposed to be symmetric on either side. Hence, half of the actual x dimension is defined in X. Y, Z axis zero is the right bottom corner. X=0 is assumed at the center

(define X 100)
(define Hna @t_n@)
(define Hb @t_b@)
(define He @t_epi@)
(define thick 75)
;This thickness means the thickness of contact which i assumed as 75um
(define Hm 0.1)
;(define HAl 0.1)
;(define HNi 0.05)
;(define HAg 0.15)
(define Hn (+ Hna Hb))
(define Hf (+ Hn He))
(define d  (/ @d@ 2))
(define Hft (+ Hf Hm))
;(define Hfta (+ Hft HAl))
;(define HfNi (+ Hfta HNi))
;(define Htot (+ HfNi HAg))

;Defining the doping quantities of device
(define Ndop @Ndop@)
(define Epidop @Epidop@)
(define Bdop @Bulkdop@)

; Creating the main structure of the device
```

```
(define bulk (sdegeo:create-rectangle (position (- 0 X) 0.0 0.0 )  (position X Hb 0.0 ) "GaN" "GaNbulk" ))
(define nlayer (sdegeo:create-rectangle (position (- 0 X) Hb 0.0 )  (position X Hn 0.0 ) "GaN" "nGaN" ))
(define epilayer1 (sdegeo:create-rectangle (position (- 0 d) Hn 0.0 )  (position (- 0 (+ d thick)) Hf 0.0 ) "GaN" "EpiGaN_A" ))
(define epilayer2 (sdegeo:create-rectangle (position d Hn 0.0 )  (position (+ d thick) Hf 0.0 ) "GaN" "EpiGaN_B" ))
(define M1 (sdegeo:create-rectangle (position (- 0 d) Hf 0.0 )  (position (- 0 (+ d thick)) Hft 0.0 ) "Metal" "M_A" ))
(define M2 (sdegeo:create-rectangle (position d Hf 0.0 )  (position (+ d thick) Hft 0.0 ) "Metal" "M_B" ))


;Defining the contact name and colors

(sdegeo:define-contact-set "Contact_A" 4.0  (color:rgb 1.0 0.0 0.0 ) "##" )
(sdegeo:define-contact-set "Contact_B" 4.0  (color:rgb 0.0 0.0 1.0 ) "##" )

;Defining the locations of contacts

(sdegeo:define-2d-contact (find-edge-id (position (- 0 (+ d (/ thick 2))) Hft 0.0)) "Contact_A" )
(sdegeo:define-2d-contact (find-edge-id (position (+ d (/ thick 2)) Hft 0.0)) "Contact_B" )


;Defining the doping profile
(sdedr:define-constant-profile "Ndoping" "nSiliconActiveConcentration" Ndop)
(sdedr:define-constant-profile-region "Place.Ndop" "Ndoping" "nGaN")

;Defining the doping of the bulk layer
(sdedr:define-constant-profile "Bdoping" "nSiliconActiveConcentration" Bdop)
(sdedr:define-constant-profile-region "Place.Bdop" "Bdoping" "GaNbulk")

; Defining the Epi doping
```

```
(sedr:define-constant-profile "Epidoping" "nSiliconActiveConcentration" Epidop)
(sedr:define-constant-profile-region "Place.EpidopA" "Epidoping" "EpiGaN_A")
(sedr:define-constant-profile-region "Place.EpidopB" "Epidoping" "EpiGaN_B")

;Defining the mesh
(sedr:define-refinement-size "Global"
 2.0 0.5 1.0
 0.05 0.05 0.1)
(sedr:define-refinement-material "Place.GaN" "Global" "GaN" )

(sedr:define-refinement-size "Epimesh"
 2.0 0.05 1.0
 0.05 0.0001 0.1)
(sedr:define-refinement-region "Place.EpiGaNA" "Epimesh" "EpiGaN_A" )
(sedr:define-refinement-region "Place.EpiGaNB" "Epimesh" "EpiGaN_B" )

(sedr:define-refinement-size "Metals"
 1.0 0.05 0.5
 0.01 0.001 0.1)
(sedr:define-refinement-material "Place.M" "Metals" "Metal" )

;Fine tuning the mesh at the interface
(sedr:define-body-interface-refwin (list epilayer1 M1) "RW1")
(sedr:define-body-interface-refwin (list epilayer2 M2) "RW2")
(sedr:define-refinement-size "RDef_1"
0.5  0.01 0.1
0.0001 0.00001 0.05)
(sedr:define-refinement-placement "RPl_1" "RDef_1" "RW1")
(sedr:define-refinement-placement "RPl_2" "RDef_1" "RW2")

;Meshing the device
(sde:build-mesh "snmesh" "" "n@node@_msh")
```

Appendix D: Device Physics File

```
File{
        Grid ="@tdr@"
        Plot="@tdrdat@"
        Parameter= "@parameter@"
        Current= "@plot@"
}

Electrode{
        {name= "Contact_A" Voltage=0.0  }
        {name= "Contact_B" Voltage=0.0  }
        }

Physics{
        Mobility(DopingDep)
        Thermionic
        Fermi
        EffectiveIntrinsicDensity( oldSlotboom  )
        Recombination(                  SRH Radiative                   )
        eBarrierTunneling "NLM"
        }
Physics(MaterialInterface="GaN/Metal")
        { Schottky
        eThermionic
                }

Math {
NonLocal "NLM"
( MaterialInterface="GaN/Metal"  Length=1e-5  Digits=4 EnergyResolution=0.001          )
  ExtendedPrecision
  Digits=8
  RHSmin=1e-8
```

```
  Extrapolate
  RelErrControl
  Iterations=30
  Notdamped=100
  NewtonPlot ( Error MinError   Residual       )
  AcceptNewtonParameter (
          -RhsAndUpdateConvergence * enable 'RHS OR Update' convergence
          RhsMin = 1.e-5 * RHS converged if 'RHS < RhsMin'
          UpdateScale = 1.e-2 * scale actual update error
          )
   }

Math(material="GaN") {
BreakCriteria { CurrentDensity(maxval=5e4) }
}

Plot {
  eDensity hDensity  Doping
  eCurrent/Vector
  eCurrentDensity hCurrentDensity
  hCurrent
  ElectricField/Vector
  eEnormal hEnormal
  eQuasiFermi hQuasiFermi
  BuiltinPotential
  ConductionBandEnergy ValenceBandEnergy
  Potential Doping SpaceCharge  SRH Auger
  AvalancheGeneration
  eMobility hMobility
  DonorConcentration AcceptorConcentration
  eVelocity hVelocity
  eBarrierTunneling hBarrierTunneling
}
```

```
Solve {
          Coupled(Iterations=100){ Poisson }
          Coupled{ Poisson Electron Hole }

   #if @<[string compare Condition "Equilibrium"] == 0>@
            Coupled(Iterations=100){ Poisson }
            Coupled{ Poisson Electron Hole }

#elif @<[string compare Condition "Full_Bias"] == 0>@

  Quasistationary(
     InitialStep=1e-2  Increment= 2.0 Minstep=1e-6 MaxStep=0.2
     Goal{ Name="Contact_A" Voltage= -0.02 }
   ){ Coupled{ Poisson Electron Hole }  }

  Quasistationary(
     InitialStep=0.01 Increment= 2.0  Minstep=1e-6 MaxStep=0.2
     Goal{ Name="Contact_A" Voltage= 0.0 }
   ){ Coupled{ Poisson Electron Hole }  }

  Quasistationary(
     InitialStep=0.001 Increment= 1.5   Minstep=1e-6 MaxStep=0.1
     Goal{ Name="Contact_A" Voltage= 0.005}
    * AcceptNewtonParameter ( ReferenceStep = 5.e-4 )
   ){ Coupled{ Poisson Electron Hole }  }

   Quasistationary(
     InitialStep=1e-2 Increment= 1.5  Minstep=1e-6 MaxStep=0.1
     Goal{ Name="Contact_A" Voltage= 0.02 }
     ){ Coupled{ Poisson Electron Hole }  }
#endif
}
```

Appendix E: Device IV File

```
#-----------------------------------------------------------------------#
lib::SetInfoDef 1
#-----------------------------------------------------------------------#
set N     @node@
set i     @node:index@
set Ndop @N_doping@
set nt @thick_n@
set Mtl @Metal@
set Xn @Xn@
set Wf @Workfunc@

#- Automatic alternating color assignment tied to node index
#-----------------------------------------------------------------------#


#if @<[string compare Condition "Equilibrium"] == 0>@

#load_file @tdrdat@ -name n($N)_des.tdr

set COLORS  [list green blue red orange magenta violet brown]
set NCOLORS [llength $COLORS]
set color   [lindex  $COLORS [expr $i%$NCOLORS]]

# Load TDR file.
set mydata2D [load_file @tdrdat@ -name n($N)_des.tdr]
# Create new plot.
set myplot2D [create_plot -dataset $mydata2D]
# Create 1D cutline normal to x-axis at point x=1.0
create_cutline -plot $myplot2D -type x -at 0.0
select_plots Plot_1
set_band_diagram Plot_1
```

```
#elif @<[string compare Condition "Full_Bias"] == 0>@


set COLORS  [list green blue red orange magenta violet brown]
set NCOLORS [llength $COLORS]
set color   [lindex  $COLORS [expr $i%$NCOLORS]]

if {[lsearch [list_plots] Plot_IV] == -1} {
        create_plot -1d -name Plot_IV
        set_plot_prop -title "J-V Characteristics" -title_font_size 20
}
select_plots Plot_IV


set_axis_prop -axis y -title {CurrentDensity [A/cm2]} \
        -title_font_size 16 -scale_font_size 14 -type linear
set_axis_prop -axis x -title {Voltage [V]} \
        -title_font_size 16 -scale_font_size 14 -type linear

load_file @plot@ -name PLT($N)
set_legend_prop -font_size 12 -location top_left -font_att bold

create_variable -name CurrentDens -dataset PLT($N) -function "(<Contact_A
TotalCurrent:PLT($N)>)*1e8/$Xn"
create_variable -name Jext -dataset PLT($N) -function "(<CurrentDens:PLT($N)>)*1e-8"

create_curve -name IV($N) -dataset PLT($N) \
        -axisX "Contact_A OuterVoltage" -axisY "CurrentDens"
set_curve_prop IV($N) -label "JV at n $nt um at $Ndop for Workfunction $Wf" \
        -color $color -line_style solid -line_width 3
set_axis_prop -plot Plot_IV -axis y -min -1000 -min_fixed
set_axis_prop -plot Plot_IV -axis y -max 1000 -max_fixed
```

```
#- Storing variables in Tcl lists for parameter extraction
#-------------------------------------------------------------------------#

set Vs [get_variable_data "Contact_A OuterVoltage" -dataset PLT($N)]
set Js [get_variable_data Jext -dataset PLT($N)]

ext::RemoveDuplicates -out RVI -x $Vs -y $Js
set Vss $RVI(X)
set Jss $RVI(Y)

ext::ExtractRdiff -out Rsp -name "out" -v $Vss -i $Jss -vo 0.0001

#endif
```