Full Bridge LLC Converter Secondary Architecture Study for Photovoltaic Application

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ABSTRACT

The increasing global energy demand calls for attention on renewable energy development. Among the available technology, the photovoltaic (PV) panels is a popular solution. Thus, targeted Power Conditioning Systems (PCSs) are drawing increased attention in research. Microconverter is one of the PCS that can support versatile applications in various power line architectures. This work focuses on the comparison of circuit secondary side architectures for LLC converter for microconverter application.

As the research foundation, general characteristic of solar energy and PV panel operation are introduced for the understanding of the needs. Previous works are referenced and compared for advantages and limitation. Base on conventional secondary resonant full bridge LLC converter, the two sub-topologies of different secondary rectification network: active, full bridge secondary and active voltage doubler output end LLC converter are presented in detail. The main operating principle is also described in mathematical formula with the corresponding cycle-by-cycle operation to ensure the functional equality before proceeding to performance comparison.

Circuit efficiency analysis is conducted on the main power stage and the key components with frequency consideration. The hardware circuit achieved the designed function while the overall hardware efficiency result agrees with analysis. In implementation, the transformer is costume built for the system pacification. Another part is the parasitic effect analysis. At a high operating frequency and to achieve very high-frequency operation, parasitic effect need to be fully understood and considered as it may have the dominating effect on the system.

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GENERAL AUDIENCE ABSTRACT

With the increasing demand for electric energy in today's world while the traditional natural energy recourses such as coals running towards depletion, renewable energy sources become an important alternative. Among them, solar energy is an option with easy access and convenient utilization. The photovoltaic (PV) panel requires matching Power Conditioning Systems (PCS) for connection and adaptation. Microconverter is one of the PCS that can support versatile applications in various power line architectures. This work focuses on different sub-circuitry for PV application under LLC converter category, which is a popular and effective solution for renewable energy dc-dc power conversion.

First, the research background is studied, which lays the ground for the utilization of LLC converter for PV application. Then the topology under study is presented in detail. In this work, the foundation of variation is based on secondary resonant full bridge LLC converter. For verification of functionality, the step-by-step operational breakdown are listed for the two verification proposed of different secondary topology. The efficiency analysis and performance verification are conducted on the given circuitry. Then the analog testing board is built and tested while the result agrees with the analysis.

A few additional topics regarding detail of the system is discussed at more length. One is the magnetic component design, which is the key part for stable and efficient system operation; another is the parasitic effect, as at such high frequency and efficiency range, the parasitic effect become significant for the circuit performance.

To my parents:

Ziyu Yan

Jie Chen

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Chapter 1

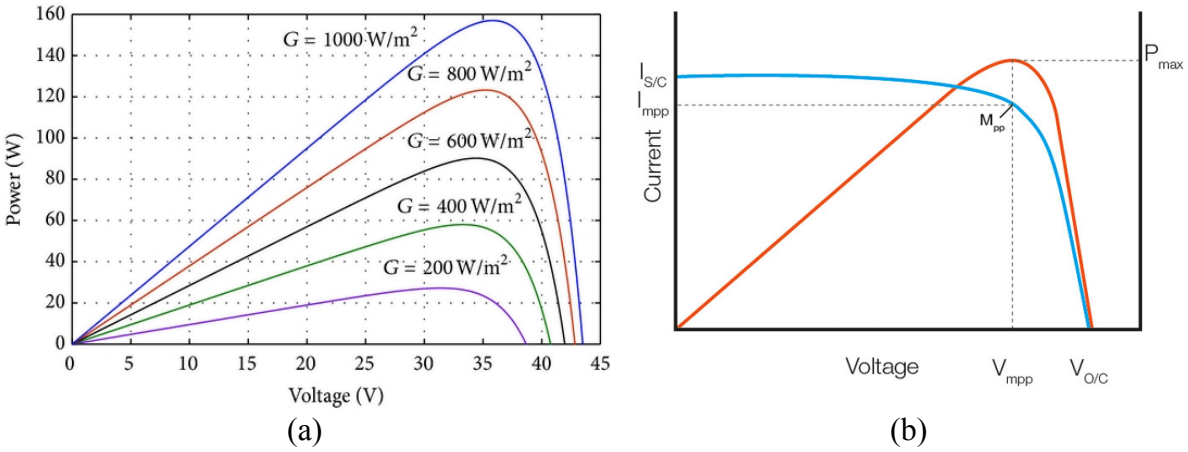
Introduction

1.1 General Background

In recent years, the required global energy production has been growing exponentially. In modern society, one main form of utilized energy is in electricity. According to the United Nations statistic, the total production was approximately 20 million gigawatt-hours in electricity in 2014. Moreover, the annual data are continuously growing. [1] Traditionally, the majority of the electricity is produced through fuel sources. With the increasing power consumption globally and the promotion of sustainable development, renewable energy has become an important sector for electricity production. [2] Among the available technology, solar energy conversion, or Photovoltaic (PV) devices proves as an efficient approach.[3] It has become one of the fastest growing renewable energy sources. Thus power regulating solution targeting this specific application is in urgent need.

In practices, Power Conditioning Systems (PCSs) and delivery paths are needed to utilized solar energy. With PV panels, the collected energy will be uploaded to the utility grid through a power delivery architecture. In this system, power electronic converters are in place to ensure compatibility and system performance. The output of PV panel needs to match to the voltage that is used for the next stage while the Maximum Power Point

Tracking (MPPT) function need to be performed. For voltage conversion, the transmission line usually adapts a relatively higher voltage to alleviated loss on the pass while a different bus voltage may also be used for standalone application. [5] The MPPT is necessary for PV application due to the output characteristic of PV panels. [4] Figure 1.1 present the general relation between output power, output current and output voltage for PV panel. Depending on model, units and environment condition, the parameters has different numerical value while the general correlation trend remains the same. In order for the most energy to be delivered to the grid and utilized, the implemented PCSs need to ensure the PV panels are operating in the voltage that allowed maximum power output.



(a) (b)

Figure 1.1. Characteristic for PV Panels (a) Single panel output demonstration for certain model (b) P-V and I-V Curve for PV panel and Maximum Power Point

Depends on the leveling structure for the above functions, there are different architecture for the PV power conditional system been proposed and implemented over the years. [5] In central or string structure, PV panels are connected in series to provide higher voltage while an inverter is placed either on the end of all or each string to inverting the dc

output of PV panels to the needed ac power supply. In these cases, MPPT is implemented for the string or the entire system as a whole.

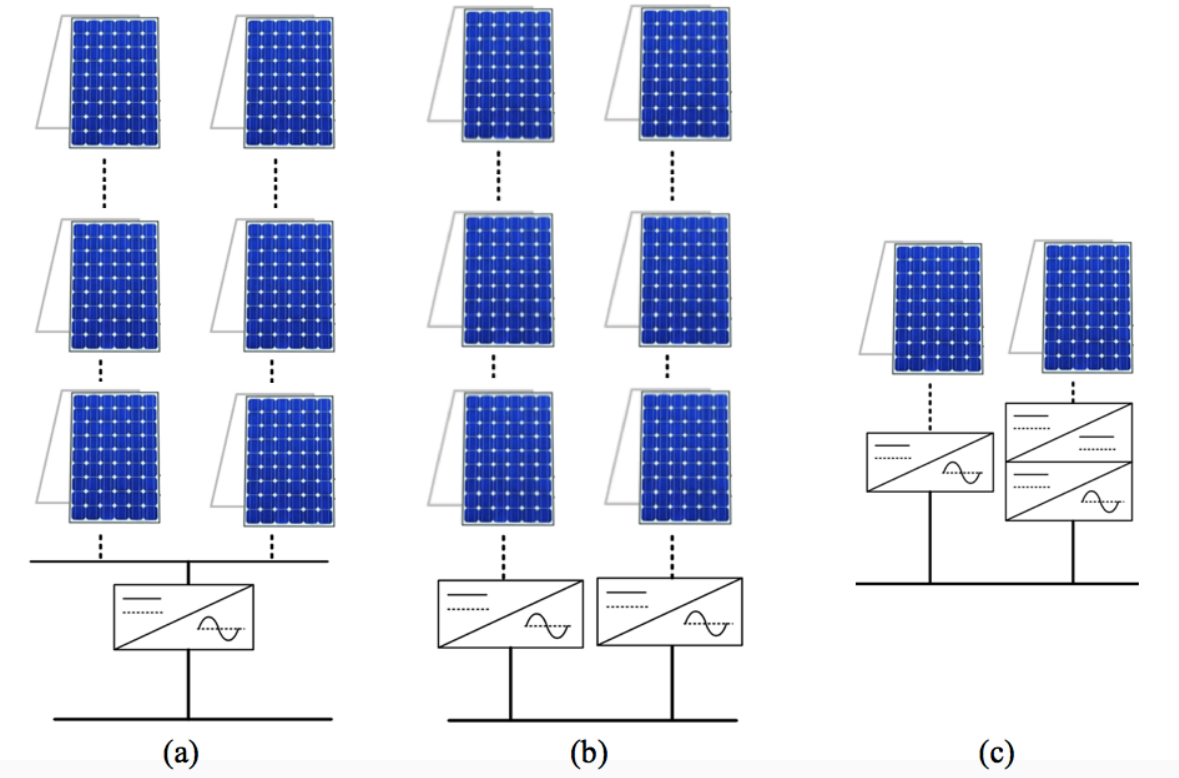


Figure 1.2. PV System Architecture (a) Central (b) String (c) Modular.

The series connection of PV panels has the disadvantage of mismatch power loss between panels.[6] When there are any differences exist between operation condition of individual panels, the string MPPT does not provide the optimized operating point for each panel. Moreover, when faulty operation occurs on one or multiple panels, the entire string might shut down due to the series connection. Therefore, modularized PCS is introduced, which allows every PV panel to be connected to the line individually. Within this category, there are also different solutions. Microinverter is a single stage solution that directly

changes the dc output to the ac value used on the line. Then there is the two-stage solution. The output of each PV panel firstly goes through a dc-dc converter to boost the energy up to the bus voltage level. Then an inverter stage directly follows if it is an ac bus, or a string inverter may be installed before connecting to the grid if dc bus architecture is used.

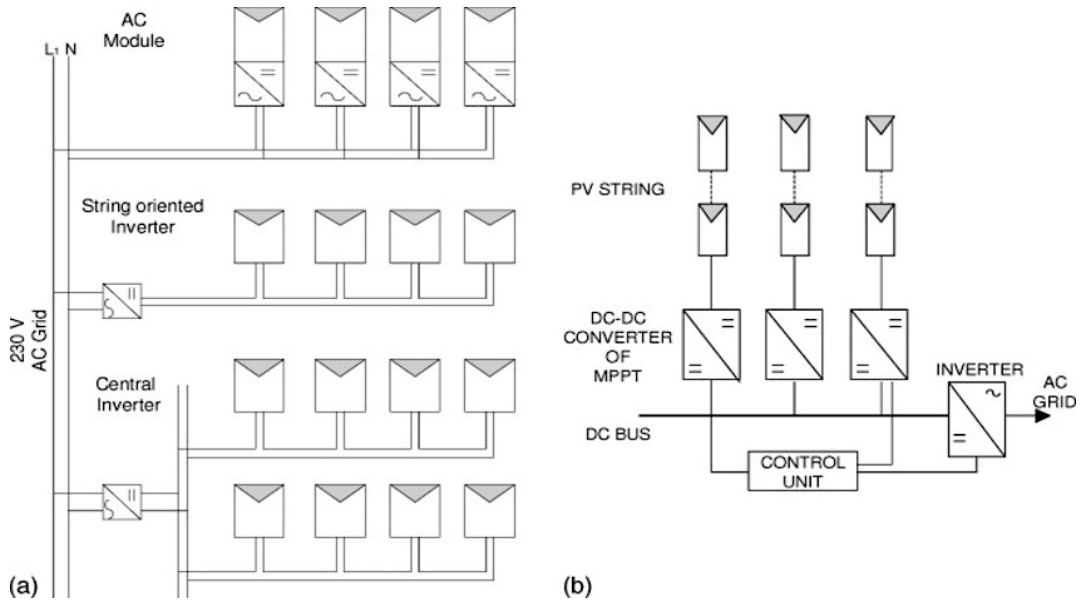


Figure 1.3. PV System Architecture (a) ac grid-based structure (b) dc bus connection.

There are multiple advantages of modularized architecture. Primarily it provides flexibility in control and operation. Each panel is controlled by a microconverter separately which provides targeted power conversion and optimization. This also provides simplified system installation as the individual panel does not necessarily to be the same model, while mix-source system is also achievable.[7] As long as the transmission bus is in place, additional units can always be added later on, which provides ease for easy customization. From the MPPT function perspective, correlated maximum power can always be extracted from each panel and the shaded units will have minimum effect on system performance.[8]

Overall, such system will be more robust for individual unit failure while also allow best unit optimization. However, such layout also requires more power conversion devices in the architecture, which leads to cost consideration. Still, the modular solution is preferred due to its apparent superiority in performance.

One essential component for achieving modular operation is the microconverter, which is the dc-dc power conversion device that is mounted on each panel for its separated control and conversion. Such unit needs to meet several expectations: high voltage conversion ratio, high efficiency, compact and autonomous. The first requirement is due to the large difference between PV panel output and the transmission line voltage. Currently, most panels have the maximum output voltage of under 65 V while the maximum power point operation voltage is at 35 V or lower. [9] On the other hand, the common dc bus voltage is 380 V. Therefore, the implemented devices need to provide the large ratio of voltage boost to ensure compatibility. For energy harvesting system such as PV, its goal is to generate most power in its lifespan with minimum initial cost. Here efficiency requires the system has high overall efficiency through operating condition, while the hardware cost for the microconverter need to be acceptable for individual panel implementation due to both financial and environmental consideration. To fully utilize the benefit of modular architecture, the ideal device should be able to be easily installed with each panel and requires minimal effort for its daily maintenance. These standards are adopted in this thesis to evaluate a given microconverter system.

1.2 Previous work

Since the initial introduction of modular architecture of PV arrays, there have been vast studies on the power electronic devices within the PCS. One approach is targeted towards utility line connection. Such modular PV PCS device is the microinverter, and it was intensely focused on previously when renewable energy source is mostly grid based. However, as the cost and technology of renewable energy become more readily accessible, and the desire and motivation for implementing renewable energy increase under the guideline of sustainable development, the structure of PV panel --- dc bus --- line/load has become more popular as it offers more flexibility for the system structure. To perfect the function while improving performance, different designs have been proposed for this application. These designs can be categorized into two groups of topology: PWM converter and resonant type converter.

The most common PWM topology for microconverter application is the flyback converter. It provides voltage step-up conversion and isolation, while has a relatively simple structure and control. [10] Other topologies includes isolated boost, buck-boost and etc. have also been explored as methods for PV dc-dc power conditioning.[11] However, PWM type of converter in such implementation usually suffers from compromised efficiency due to switch losses while incorporating galvanic isolation limits the choice and simplicity of the system.

To achieve very high efficiency while maintaining a compact structure, resonant converter has become a popular solution. It provides natural soft switching with proper design, and the architecture includes incorporated transformer which also serves as the galvanic isolation.

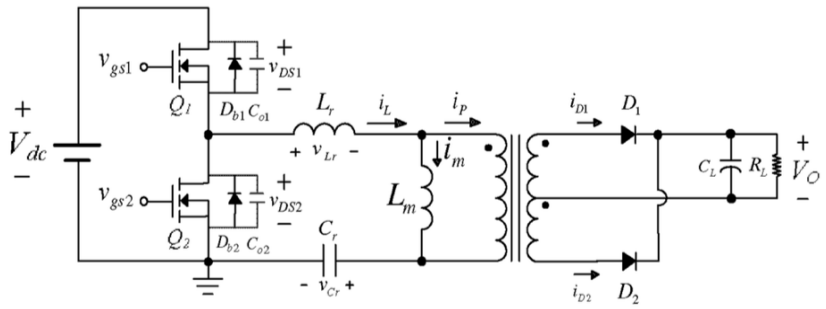


Figure 1.4. The circuit of Standard LLC Converter.

Within resonant converter family, LLC converter is favored especially for its very high efficiency while maintain some range of regulation capacity. Extensive study has been conducted for the detailed architecture, system performance and control for LLC topology. Hsieh and Hsu illustrated the synchronous rectification operation of common LLC in detail[12]; then some proposed LLC variations utilize full bridge front-end rectification structure for improved controllability [13]–[15]; Kim, D. *et al.* proposed a solution of increasing input range by adding auxiliary LC loop[16] while AC switch has also been added to provide more APWM mode of operation and improve operation range [17]; Chub *et al.* reconfigured a buck-boost stage to extend the input voltage range[18]. All of the above study improved functionality of traditional LLC resonant converter by extending operational range and providing more control methods. However, above solutions requires additional devices and loops, while still are nonideal for microconverter application. Then secondary rectification is modified for targeted application: usage of current doubler is explored for server application [19], and voltage-doubler are suggested as secondary architecture for voltage step-up LLC application [20]–[22]. The later studies cooperated several design aspects specifically for microconverter application.

Also, works have also been presented for LLC converter system analysis. Soft-switching realization is studied in detail to fully utilize the advantage of resonant converter characteristic[23], [24]; Varies control method are suggested for improved system function[17], [25], [26]; design procedure is introduced for specific system optimization goal [15], [27], [28]. Some work specifically looked into certain detail parasitic effect [29]–[31]; while others address the phenomenon under a general setting [19], [32]–[34]. These study provided insight for LLC optimization in certain scope yet targeted analyze for full-bridge LLC converter for microconverter application.

1.3 Study goal and thesis outline

In this paper, the performance differences of secondary architecture for LLC converter in PV microconverter application is studied in detail. For comparison, the topologies under discussion should meet the same requirement:

1) All systems can achieve the same function of wide input range operation. The input range for PV panel is considered as from 15 to 65 Volt while the output is at 380 V for dc bus. All topology need to be able to achieve the same range of controllability.
2) The system can provide the high ratio of voltage step-up with galvanic isolation while maintaining a similar level of system complexity.

The above standards are to ensure the same engineering functionality and class rating. Then for performance comparison, following points are evaluated:

1) System efficiency. The primary goal for system optimization for this application is to improve overall efficiency. When other differences are within tolerance, higher efficiency is to be expected
2) Device stress. This will contribute to system lifespan and reliability.
3) Device number and cost. One disadvantage of implementing modular PV system is the increased installation cost from the additional PCS devices. Thus it is crucial to control the hardware cost to improve its competitively on the market.

In this paper, the topic is addressed in the following structure:

Chapter 1. addresses the application background and research history. The general information for PV architecture and its PCS is provided, then more detail for previous work in microconverter study is discussed for its focus and pros and cons.

Chapter 2. introduces the topologies under discussion and analysis the system structure and operation stage. This is to ensure same functionality for fair performance evaluation.

Chapter 3. focuses on the efficiency analysis for the given system. A general numerical estimation is conducted, and the key parameters are pointed out for accuracy. This section also covers the verification and test results. System performance is compared with minimum changes on hardware implementation to eliminate interference.

Chapter 4. address the magnetic design and optimization. For the LLC converters under discussion, magnetic components are the crucial part of system optimization for which customized design is required.

Chapter 5. specifically discusses the parasitic effect within the system. While the traditional LLC converter optimization is rather straightforward, the performance is highly relative to the non-ideality from the actual hardware. This is especially true for the system utilizing Wide-Band-Gap devices. Thus in this section, a few parasitic related phenomenon is further explored.

Chapter 6. concludes this paper and points out the future work direction.

Chapter 2

Full Bridge LLC Secondary Topologies

2.1 Introduction of Topologies

As stated in the previous chapter, there has been some work introduced previous for microconverter application. Especially, LLC converter has been widely adopted for renewable energy source power conversion. For this specific application, there has been some targeted design providing the needed wide operating range potential.

One of the proposed topology that utilizing resonant converter and improved the rectification networks to adapt to the high voltage conversion ratio needed for this application. For a improved operating range, full-bridge rectification network is used for the front end while voltage doubler is implemented for the output end [35]. This design required fewer turns ratio for the transformer and maintained the soft-switching advantage of the LLC converter when operates higher than the resonant frequency.

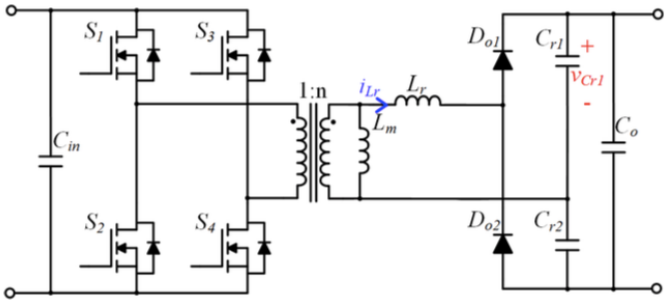


Figure 2.1. Full Bridge LLC Converter with Voltage Doubler at Secondary Side[35].

However, the above design has its limitation, as the operating range is restricted due to the passive switching components which lack controllability. Thus with fixed frequency operation, additional bidirectional ac switch is required for extended operational range, which partially defeats the purpose of reducing the component number by using voltage doubler.

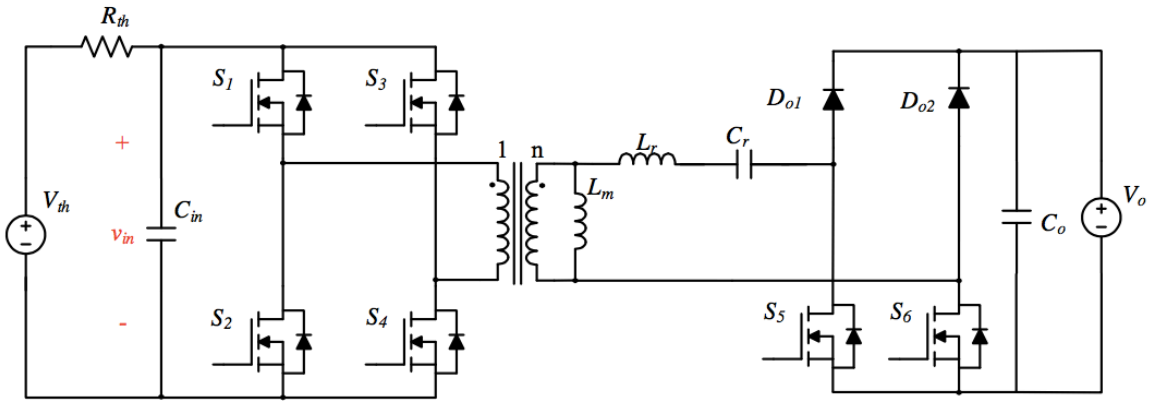


Figure 2.2. Full Bridge LLC Converter with Full Bridge Secondary.

Another approach is to use full bridge rectification on the secondary side[36]. While more switch component is required, device stress is reduced thus allows lower loss on each device. Such structure can also improve the control magnetism by partially using active switches on the secondary side, which would allow more complex functions of the system.[37] Thus the extended operating range at fix frequency point can be achieved with no additional device cost.

In this paper, further modifications of the above topologies are listed while the main work focuses on the comparison of their performances. As can be seen from the schematic, the secondary architecture still partially relays on passive switch component which limits

the controllability while introduces energy loss created by diode voltage drop and reverse recovery loss. By changing all diode on the secondary side of power stage to FET and perform diode emulation, the system is expected to provide the same function during Synchronize Rectification (SR) operation while loss should be reduced. Also, GaN FETs are used for all the active devices in this research. This allows faster switching operation and avoids reverse recovery loss. Related parasitic issue is then addressed in this work.

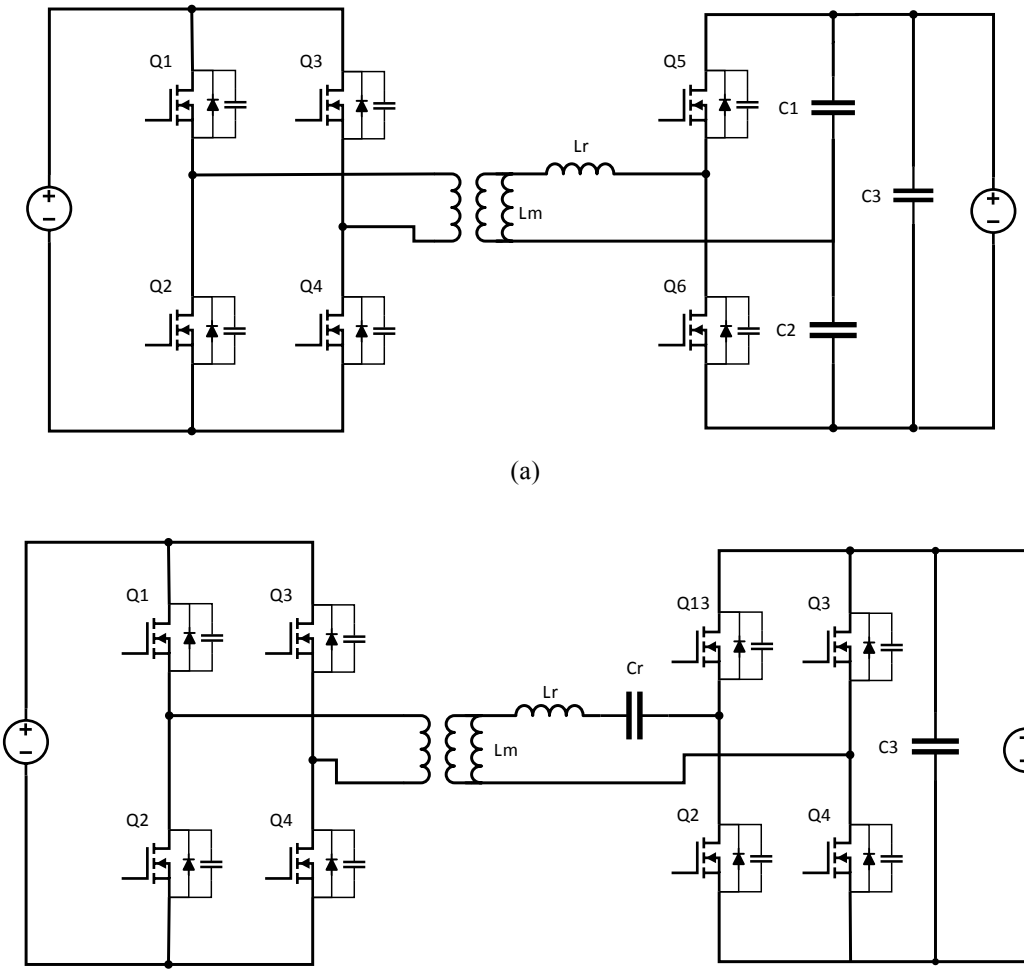


Figure 2.3. Topologies under Study: (a) Full Bridge LLC converter with Active Voltage Doubler Secondary; (b) Full Bridge LLC Converter with Active Full Bridge Secondary Topology.

As shown in above figure, the studied circuits require same or fewer number of devices for maintaining the same functionality of the system. For nominal point operation, the secondary switches perform diode emulation, which maintains the same function with the advantage of no diode voltage drop. Also, soft-switching will be ensured for the secondary side as the deadtime can and should be carefully toned for the secondary as well as primary side. The detailed operation will be analyzed step by step later in this chapter. For the convenience of discussion, the topology reflected in Figure 2.3. (a) will be referred as Active Half Bridge Secondary LLC or Half Bridge topology and will be marked with HB subscript for the parameters, and the circuit in (b) will be referred as Active Full Bridge Secondary LLC, or Full Bridge topology and will be marked with FB subscript for the parameters.

2.2 Operation Analysis for Active Half Bridge Secondary LLC

The Active Half Bridge Secondary LLC is derived from the full bridge LLC topology using voltage doubler. To maintaining functionality and optimizing performance, the primary and secondary devices operate in synchronize rectification mode operation.

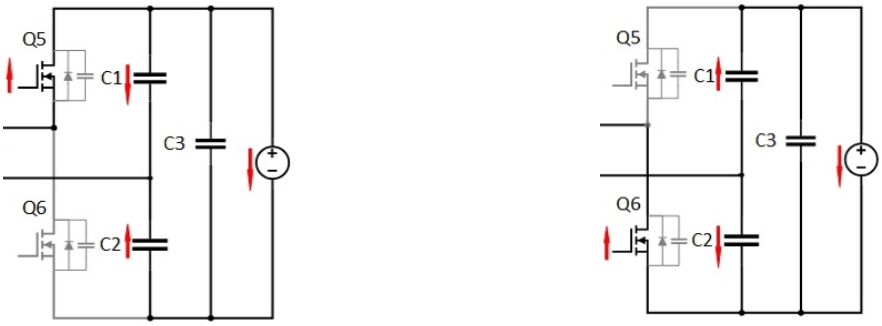


Figure 2.4. Secondary Active Voltage Doubler Operation (a) During C1 Charging; (b) During C2 Discharging.

In this topology, the capacitors in the secondary half-bridge rectification network also serve as the capacitance of resonant tank. As demonstrated in Figure 2.4., during operation, the two capacitor C_{r1} and C_{r2} are in parallel equivalently while one of the capacitor current conducting through the load. Therefore the angular frequency and angular displacement can be defined in (2-1) and (2-2).

$$\omega_r = \frac{1}{\sqrt{L_r(C_{r1} + C_{r2})}} \tag{2-1}$$

$$\theta = \omega_r \cdot t \tag{2-2}$$

As the secondary switching devices Q5 and Q6 and primary devices Q1 through Q4 are separately controlled, the deadtimes are separately set for the required discharging time are different for the two groups of devices. The secondary devices are higher voltage and lower current rated compared with primary; while the primary devices are rated for high current with low voltage tolerance. The different nature of the devices also brings the different value of parasitic capacitances, which cause asymmetry during discharges: The primary and secondary devices take different time to discharge. This creates additional stages during operation. However, as will be discussed in the later chapter, though there are methods to synchronize the discharging time, there is no obvious benefit from such control. The step by step operation and corresponding time-stamped waveform demonstration are in Figure 2.6 and Figure 2.6 and is analyzed below.

Stage 1 [time interval $t_o < t < t_1$, figure (a)**]** At beginning of this interval, the resonant inductor (or inductance) current L_r is at zero while the voltage across C_{r1} is at its minimum. The initial condition can be described by

$$i_{Lr}(t_o) = 0 \tag{2-3}$$

$$v_{Cr1}(t_o) = \frac{V_o}{2} - \Delta v_{Cr} \tag{2-4}$$

Here the maximum voltage variance for a signal resonant capacitor in this topology can be determined by output profile and switching frequency, as

$$\Delta v_{Cr} = \frac{P_o T_s}{4 V_o C_r} \tag{2-5}$$

Note that there is $v_{Cr1}(t) + v_{Cr2}(t) = V_o$ for any time during the switching cycle while the average value is at half of load voltage for any one of them.

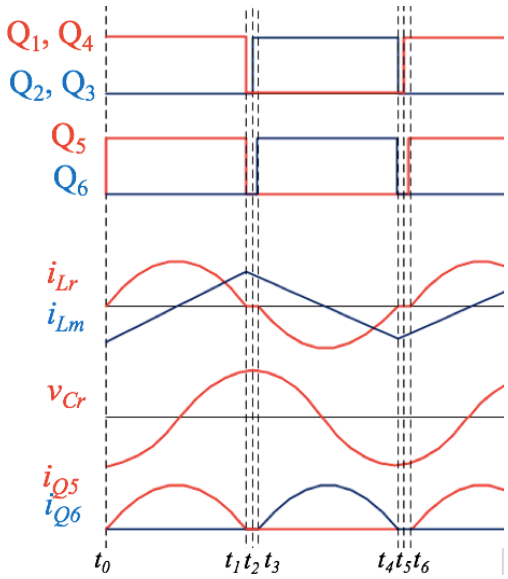
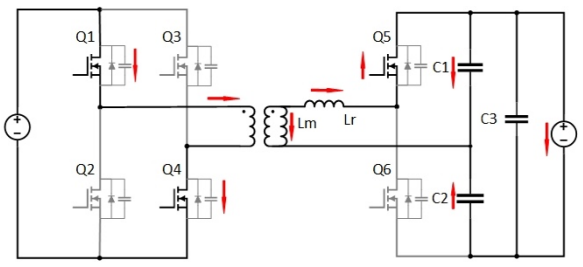
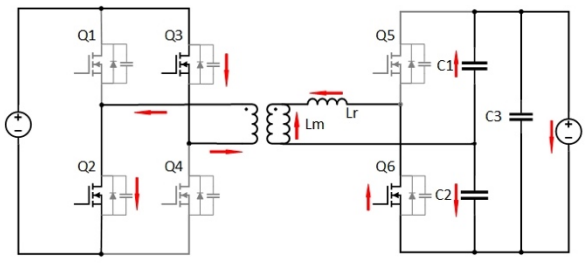


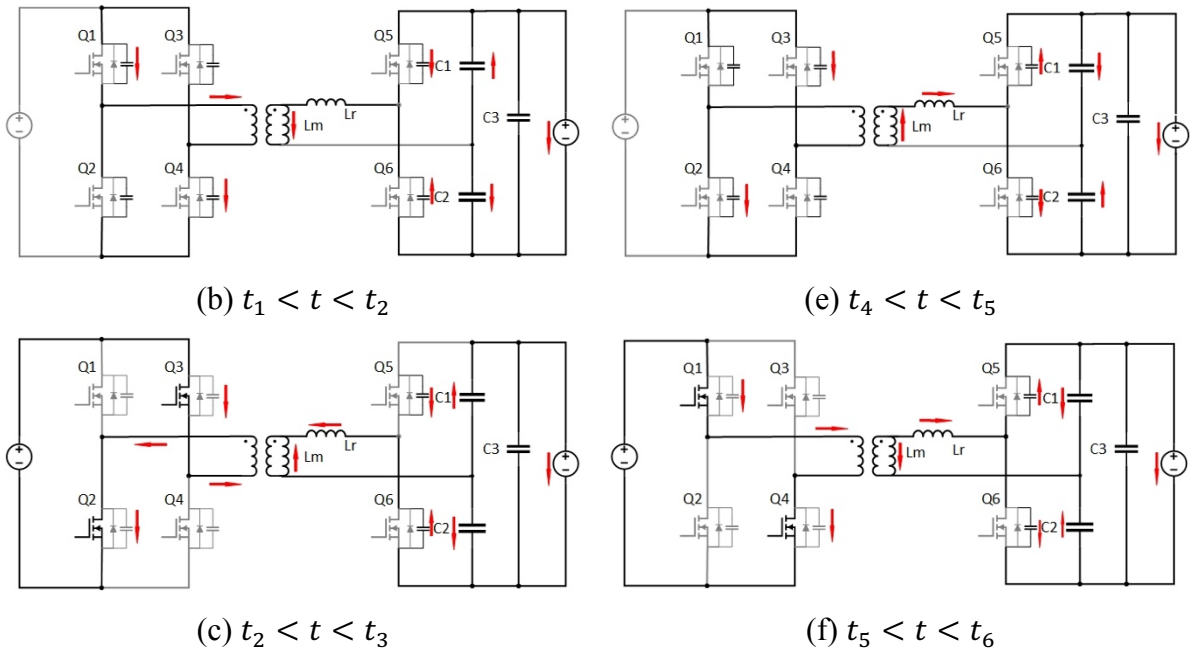
Figure 2.5. Operating waveform demonstration for the half-bridge case.



(a) $t_o < t < t_1$



(d) $t_3 < t < t_4$



(b) $t_1 < t < t_2$ (e) $t_4 < t < t_5$

(c) $t_2 < t < t_3$ (f) $t_5 < t < t_6$

Figure 2.6. Stage operation Analysis for Active Half Bridge LLC Converter

At moment t_o, the primary side switch Q1 and Q4 turns on while at the same time Q5 turns on. The source is directly connected to the transformer primary side. Thus the voltage across transformer primary side is the input voltage V_{in}; and the voltage of n times the input voltage is applied to the secondary side, where n is the transformer secondary to primary turns ratio. The resonant inductance L_r resonate with capacitor C_{r1} and C_{r2} in parallel configuration and the resonant current can be described as

$$i_{Lr}(t) = \frac{V_1}{Z_r} \cdot \sin\left(\pi - \omega(t - t_o)\right) \tag{2-6}$$

Here V_1 is the voltage across resonant inductor and is described in (2-7) below.

$$V_1 = nV_{in} - \left(\frac{V_o}{2} - \Delta v_{Cr}\right) \tag{2-7}$$

Where Z_r is the resonant tank impedance and is calculated in (2-8).

$$Z_r = \sqrt{\frac{L_r}{(C_{r1} + C_{r2})}} \tag{2-8}$$

Since the system operates in synchronize rectification, the switching frequency is equal to the resonant frequency.

$$f_{sw} = \frac{\omega_r}{2\pi} = \frac{1}{2\pi\sqrt{L_r(C_{r1} + C_{r2})}} \tag{2-9}$$

Thus during this period, the inductor current resonant through a complete half cycle. The system directly transfers energy from source to the output through this entire stage.

Also, the magnetizing current is charging up during this stage. At moment t_o, the inductor current is at its minimum value as in (2-10) and linearly increases to its peak value by the end of this cycle. This process is described in the time domain function (2-11) below.

$$i_{Lm}(t_0) = -\frac{nV_o}{4L_m f_{sw}} \tag{2-10}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{nV_o}{L_m}(t - t_o) \tag{2-11}$$

At the end of this stage, the resonant current reaches zero while there is no current through the secondary devices, while only magnetizing current is conducting through the primary side. Thus, Q5 can be turned off at its natural commutate point. This will allow the Zero Current Switching for Q5 at t_1. And at this time the current through Q1 and Q4 are also relatively small.

Stage 2 [time interval $t_1 < t < t_2$, figure (b)**]** At moment t_1, secondary switch Q5 turns off at ZCS and primary side switch Q1 and Q4 turns off at near ZVS. The system

enters Zero Voltage Switching (ZVS) discharging period. This stage lasts as long as it takes for primary devices to fully discharge, which is a very brief section compared with switching cycle. As discussed in the last stage, at this time the magnetizing current i_{Lm} has been charged to its peak value. Since the time interval is very short, the magnetizing inductance can be considered as a current source with the value of peak magnetizing current.

$$i_{Lm}(t) = \frac{nV_o}{4L_m f_{sw}}, \qquad t_1 < t < t_2 \tag{2-12}$$

During this stage, this magnetizing current charges and discharges device on both primary and secondary side as shown in figure X. The red arrow marks the path and direction of current through devices. On the primary side, device output capacitance C_{oss} for Q1 and Q4 are been charged while and voltage charge across Q2 and Q3's output parasitic capacitance are been discharged. This will allow Q2 and Q3 later been turned on at zero voltage and achieve soft switching.

Once the C_{oss} of primary side device fully discharges, the current will conduct through the body diode, which are have high energy loss due to the large body diode voltage drop of GaN devices. To eliminate this power dissipation, the charged devices Q2 and Q3 are to be turned on when the voltage across output capacitances reach zero, and system moves to the next stage.

Stage 3 [time interval $t_2 < t < t_3$, figure (c)**]** At the moment t_3, primary devices Q2 and Q3 are turned on. However, the secondary device is not necessarily fully discharged at the same period of time. Thus during this stage, the secondary device continuously

discharges while the primary has been connected to the source. The voltage applied to the primary side of the transformer is reversed for the next half cycle: the voltage value across the transformer winding is the negative of input voltage. And the voltage across transformer secondary winding is $-nV_{in}$, which means the inductor current direction is reversed compare with stage 1. However, the current direction is the same as the last stage.

During this period, the magnetizing current has already started decreasing as it is been reversely charged. As

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{nV_o}{L_m}(t - t_2) \tag{2-13}$$

This stage finishes at the moment that Q6 is fully discharged. Similar to the situate for primary side device discharging, the secondary side circuit will start conducting through the body diode of Q6, which creates additional loss with its body diode. Thus for optimized performance, Q6 is to be turned on at the moment the voltage across device reaches zero. This stage ends.

Stage 4 [time interval $t_3 < t < t_4$, figure (d)**]** At moment t_3, Q6 on the secondary side is turned on. The input is connected to the output during this period of time and the system starts its energy conduction for the other half cycle. The operation during this period are similar to that of stage 1. Only the voltage across transformer is negative and the current through resonant inductor is in the reversed direction. The input source is applied to the primary side of transformer through Q2 and Q3 and the voltage of $-nV_{in}$ is at the secondary side of the transformer as of the last stage. However, as Q6 is now turned on, the load is connected to the rest of circuit through Q6 and C1. During this stage, resonant

inductance L_r resonants with capacitor C_{r1} in parallel with C_{r2} through load current. The resonant current through C_{r1} discharges it and the voltage across C_{r1} decreases during this stage, as described in

$$v_{Cr1}(t) = nV_{in} - r\cos\big(\omega(t - t_3)\big) \tag{2-14}$$

At this stage, current though L_r is the resonant current that conducts energy from source to load, where the current value is

$$i_{Lr}(t) = -\frac{V_1}{Z_r} \cdot \sin\big(\pi - \omega(t - t_o)\big) \tag{2-15}$$

Compare (2-6) and (2-15), this stage is the negative half cycle of stage 1 and the behavior is in symmetry with the positive half-cycle in stage 1. During this period, the current in the tank finishes a complete half cycle and reaches zero at t_4. Thus soft switching again can be achieved for the secondary device turn off. And the current in the primary device is only is value of magnetizing current at this time.

For L_m, the voltage is negative across the magnetizing inductance and remain constant. Thus the magnetizing current decreases linearly though this period. At t_4, the current though primary device Q2 and Q3 are the absolute value of the magnetizing current for primary side, which is at its minimum value. There is the following function for this time period.

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{nV_o}{L_m}(t - t_2) \tag{2-16}$$

Stage 5 [time interval $t_4 < t < t_5$, figure (e)**]** At t_4, secondary device Q6 turns off at zero current and primary device Q2 and Q3 turns off at low current, as no resonant current

is conducting and only magnetizing current exist. Similar to that of stage 2, both primary and secondary devices start to charge and discharge the output parasitic capacitances. Note that as no resonant current is circulating at this point, the secondary current direction is dominated by magnetizing current. The L_m can be considered as a current sources and are shared by both primary and secondary side. During this brief period, magnetizing current can be approximated as a fixed value and is at the minimum point.

$$i_{Lm}(t) = \frac{nV_o}{4L_m f_{sw}}, \qquad t_1 < t < t_2 \tag{2-17}$$

This stage ends when the voltage across Q1 and Q4 has reduced to zero and soft turn on can be achieved.

Stage 6 [time interval $t_5 < t < t_6$, figure (f)**]** At moment t_6, primary side devices Q1 and Q4 turns on and connects the input voltage in positive direction across the transformer primary side. As the secondary devices are both off at this moment, this voltage will force resonant inductor current to discharge Q5. Once Q5 is fully discharged, this stage ends.

During this period, the magnetizing current already starts to be charged as a positive voltage is applied. There is the minimum value for i_{Lm} at moment t_5 before positive voltage is applied.

$$i_{Lm}(t_5) = -\frac{nV_o}{4L_m f_{sw}} \tag{2-18}$$

When the voltage across Q5 reaches zero, the devices can be turned on at ZVS when this stage finishes. Thus the next cycle can begin from stage 1.

2.3 Operation Analysis for Active Full Bridge Secondary LLC

For full bridge secondary LLC, an active full bridge rectification network is used at the secondary output end after the resonant tank. The step by step analysis shows similar operation with its half bridge secondary counterpart. For this topology, rectification network is separated from the resonant tank. While there are more active switches in this topology, the control design and circuit operation in a certain way are simpler.

As there is a separate resonant tank, the resonant capacitor can be a single device or a capacitor network located directly after the resonant inductance. Here we can treat this capacitance as a whole and its value C_r satisfies:

$$f_{sw} = \frac{\omega_r}{2\pi} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2-19}$$

For this resonant tank, there is the angular frequency as (2-20) and impedance (2-21).

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{2-20}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2-21}$$

Similar to that of the half-bridge case, the primary and secondary devices have different ratings, thus also completely different parasitic value. While for the conducting periods during a duty cycle the front end and secondary full bridges operate in synchronize, the discharging behavior during deadtime differs. For the Full Bridge secondary topology, the total parasitic from the system consideration is Q5, Q7 in series and Q6, Q8 in series,

then the two branch are in parallel, as demonstrated in X. Thus the equivalent $C_{sec,oss}$ equals to the value of a single device.

Figure 2.7. Secondary Active Full Bridge Secondary Device Discharging Operation (a) During Q5 Charging; (b) During Q5 Discharging.

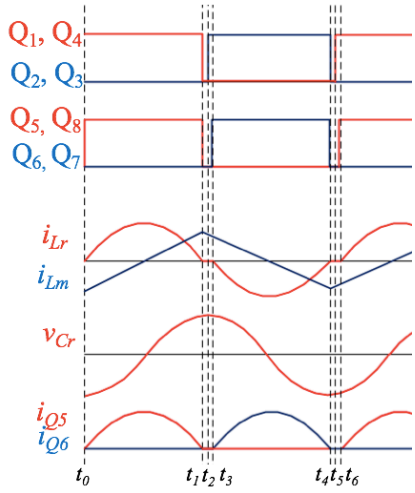


Figure 2.8. Operating waveform demonstration for full bridge case.

Stage 1 [time interval $t_o < t < t_1$, figure (a)**]** This stage is the first period for energy conduction between source and load. In this stage, the primary side switch Q1 and Q4 is on while at the moment t_o secondary switch Q5 and Q8 turns on. At beginning of this interval,

the resonant inductor (or inductance) current L_r is at zero while the voltage across C_r is at its minimum. The initial condition can be described by

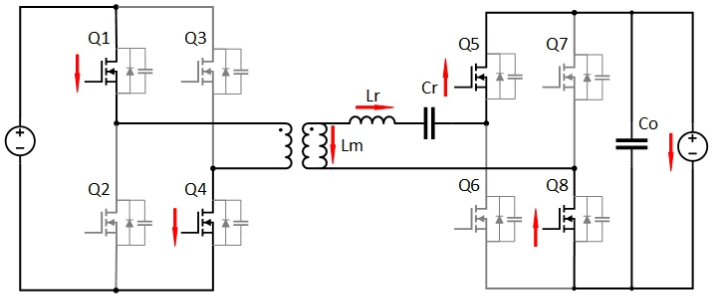
$$i_{Lr}(t_o) = 0 \tag{2-22}$$

$$v_{Cr}(t_o) = -\Delta v_{Cr} \tag{2-23}$$

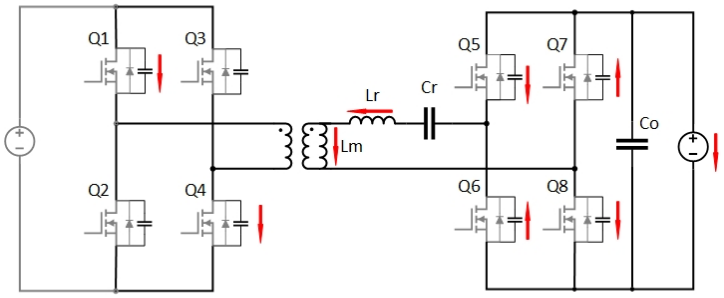
Here the maximum voltage variance for the resonant capacitor is the same as the case in half bridge topology, as

$$\Delta v_{Cr} = \frac{P_o T_s}{4 V_o C_r} \tag{2-24}$$

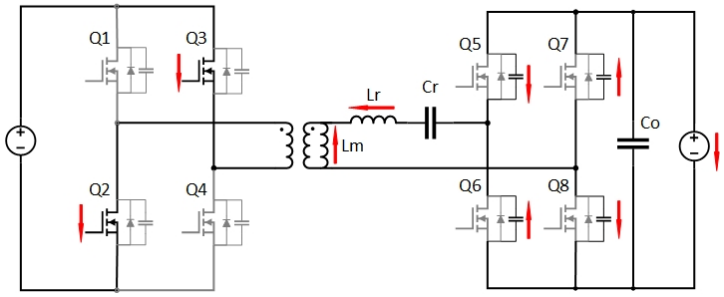
When the source is directly connected to the transformer primary side, input voltage V_{in} is applied across transformer primary side; and the voltage of n times the input voltage is at the secondary side. Here n is the transformer secondary to primary turns ratio for full bridge configuration.



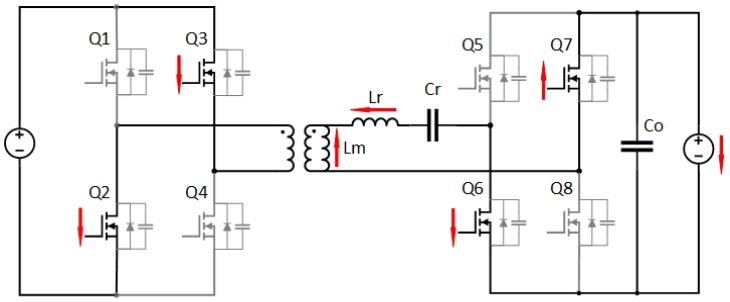
(a) $t_o < t < t_1$



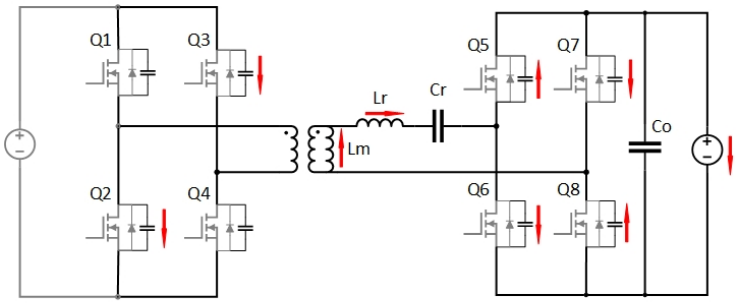
(b) $t_1 < t < t_2$



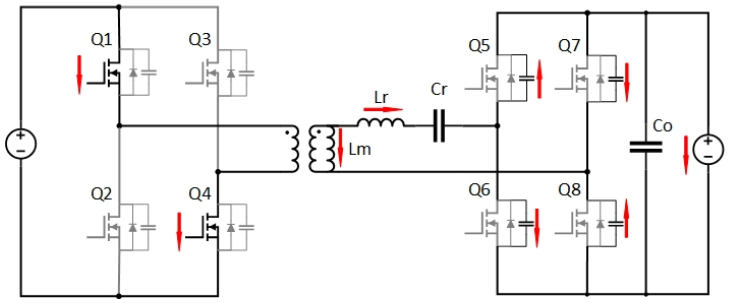
(c) $t_2 < t < t_3$



(d) $t_3 < t < t_4$



(e) $t_4 < t < t_5$



(f) $t_5 < t < t_6$

Figure 2.9. Stage operation Analysis for Active Full Bridge LLC Converter

During this stage, resonant inductance L_r resonate with C_r for a complete half cycle and the resonant current can be described as

$$i_{Lr}(t) = \frac{V_r}{Z_r} \cdot \sin\left(\pi - \omega(t - t_o)\right) \tag{2-25}$$

Where Z_r is the resonant tank impedance and is calculated in (2-24). Here V_r is the voltage across resonant inductor. Ideally it equals to the voltage ripple of the resonant capacitor, as the transformer turns ratio is designed that the voltage on the secondary side is the designated output voltage.

$$V_r = \Delta v_{Cr} \tag{2-26}$$

In reality, there is a slight difference due to difficulty in transformer partial turns and voltage loss on the devices. The actual voltage ripple is described in below.

$$V_r = nV_{in} - V_o + \Delta v_{Cr} \tag{2-27}$$

The system is designed to operate in synchronize rectification, which requires the switching frequency be equal to the resonant frequency. For this stage, the time length a half resonant cycle and allows the current to reach to zero at the end of the stage.

$$t_1 - t_0 = \frac{1}{2f_r} = \frac{1}{2} \cdot 2\pi\sqrt{L_r C_r} \tag{2-28}$$

Thus during this period, the inductor current resonant through a complete half cycle. The system directly transfers energy from source to the output through this entire stage.

Also, the magnetizing current is being charged during this stage. The current increases from its minimum value since the moment primary conducts the input to transformer primary and it linearly increases to its peak value by the end of this cycle. This process is described in the time domain function (2-11) below.

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{nV_o}{L_m}(t - t_o) \quad (2\text{-}29)$$

At the end of this stage, the resonant current reaches zero and there is no current through the secondary devices, while only magnetizing current is conducting through the primary side. Thus, Q5 and Q7 can be turned off at zero current point. Thus the turn-off for secondary devices is considered lossless. For the primary side, the turn-off is at the peak magnetizing current value. While this creates energy loss, the magnetizing current is necessary for the discharging period in the next stage and ultimately achieves soft turn-on. For GaN devices, turn-off loss at such small current is significantly smaller compared with a hard turn-on loss.

Stage 2 [time interval $t_1 < t < t_2$, figure (b)**]** At moment t_1, secondary switch Q5 and Q8 turn off at ZCS and primary side switch Q1 and Q4 turns off at near ZCS. With all primary device turned off, the input side is no longer connected with the rest of circuit. The primary side of transformer is not clamped by the input voltage, allowing the magnetizing current start discharging the primary and secondary devices. The purpose of this stage is to fully discharge the primary device and ensure zero voltage across Q2 and Q3 by the end of this stage, preparing for ZVS turn on of these devices.

As the voltage across transformer primary side has been removed, magnetizing inductance is no longer been charged. Since the time interval is very short, the magnetizing inductance can be considered as a current source with the value of peak magnetizing current.

$$i_{Lm}(t) = \frac{nV_o}{4L_m f_{sw}}, \qquad t_1 < t < t_2 \tag{2-30}$$

During this stage, this magnetizing current charges and discharges device on both primary and secondary side as shown in Figure 2.9. (b). The red arrow marks the path and direction of current through devices. On the primary side, device output capacitance C_{oss} for Q1 and Q4 are been charged while and voltage charge across Q2 and Q3's output parasitic capacitance are been discharged. At the same time, magnetizing current are also assisting the discharging of secondary side device. The equivalent discharging model is shown in Figure X. Since current sharing exist between primary and secondary side, the discharging process for primary C_{oss} are nonlinear. This phenomenon will be discussing further in later chapter.

Once the voltage across Q2 and Q3 is dropped to zero and C_{oss} of primary side device fully discharges, Q2 and Q3 are to be turned on to avoid conduction through the body diode. Thus this marks the end of this stage.

Stage 3 [time interval $t_2 < t < t_3$, figure (c)**]** At the moment t_3, primary devices Q2 and Q3 are turned on with ZVS. At this time, secondary device C_{oss} are not necessarily fully discharges. Thus during this stage, the secondary device continuously discharges while the primary has been connected to the source. Once Q2 and Q3 is turned on, the transformer primary side across voltage reverses polarity: the voltage value across the transformer winding is the negative of input voltage. And the voltage across transformer

secondary winding is $-nV_{in}$ now. This will reverse the current direction in the resonant tank: inductor current direction is reversed compare with stage 1; this current is actually in the same direction as the secondary discharging current during deadtime.

During this period, the magnetizing inductance is being reversely charged and the magnetizing current start to decrease from its peak value. As

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{nV_o}{L_m}(t - t_2) \tag{2-31}$$

During this stage, the secondary device discharging is no longer assisted by magnetizing current solely. Inductance current i_{Lr} will ensure secondary device been fully discharged quickly. Similar to the situate for half-bridge discharging case and also the the case for primary device, the secondary side circuit will start conducting through the body diode once its C_{oss} if fully discharged, which creates additional loss with its body diode voltage drop. Thus for optimized performance, Q6 and Q7 is to be turned on at the moment the voltage across device reaches zero. This stage ends as soon as voltage across Q6 and Q7 has reached zero.

Stage 4 [time interval $t_3 < t < t_4$, figure (d)**]** As now the voltage across Q6 and Q7 has dropped to zero, these two device turns on at t_3. Through Q2 and Q3 on the primary side and Q6 and Q7 on the secondary side, the system is conducting energy from source to the load. The operation during this stage is the negative asymmetric of that in stage 1. The input voltage is applied to the transformer winding with reversed polarity and the voltage of $-nV_{in}$ is observed across the secondary side of the transformer during this time interval. The resonant inductance resonant with the resonant capacitor and resonant tank resonate

another complete half cycle. There is resonant inductor current formula (2-31) and resonant capacitor voltage described as (2-30).

$$v_{Cr}(t) = -V_r \cos\big(\omega(t - t_3)\big) \tag{2-32}$$

At this stage, current though L_r is the negative half cycle of a complete resonant period. Also this period lasts half the resonant cycle, which allow the current value reaches zero by the end of this stage.

$$i_{Lr}(t) = -\frac{V_r}{Z_r} \cdot \sin\big(\omega(t - t_3)\big) \tag{2-33}$$

At moment t_4, the current in the resonant tank is at zero. Thus soft switching again can be achieved for the secondary device turn off. And the current in the primary device is only is value of magnetizing current at this time. At t_4, the current though primary device Q2 and Q3 are the absolute value of the magnetizing current for primary side, which is at its minimum value.

For L_m, there is the negative voltage of nV_o across the magnetizing inductance this entire stage. Thus the magnetizing current decreases linearly though this period. There is the following time domain function (2-32) for this time period.

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{nV_o}{L_m}(t - t_3) \tag{2-34}$$

Stage 5 [time interval $t_4 < t < t_5$, figure (e)**]** At moment t_4, Q2, Q3 and Q6 and Q7 turns off at the same time. There is full soft switching for the secondary side and partial ZCS for the primary: secondary device Q6 and Q7 turns off at ZCS and primary device Q2 and Q3 turns off at low current, as no resonant current is conducting and only magnetizing

current exist. Once primary rectification network enters deadtime, transformer also no longer been clapped by input and magnetizing inductance is no longer been charged. For this period, the magnetizing current can be considered as a current source with constant value.

$$i_{Lm}(t) = -\frac{nV_o}{4L_m f_{sw}}, \qquad t_4 < t < t_5 \tag{2-35}$$

The magnetizing current charges Q1 and Q4 primarily while also charge Q5 and Q8 in the secondary. Note that the secondary charging and discharging happens simultaneously. The voltage across each leg in the full bridge is constant and of that of the load voltage. However, the purpose of this stage is to ensure soft switching of the primary side during turn on. Thus this stage ends as soon as the voltage across Q1 and Q4 has reduced to zero and soft turn on can be achieved.

Stage 6 [time interval $t_5 < t < t_6$, figure (f)**]** At moment t_6, primary side devices Q1 and Q4 turns on with ZVS. The positive input voltage is directly applied across the transformer primary side. All the secondary devices remain turned off for this stage until Q5 and Q8 are fully discharged. At this time the transformer is connected to the input and, the secondary positive transformer voltage will force discharge Q5 and Q8. Note that though Q5 and Q8 are identical devices, slight differences for parasitic value may still exist with asymmetrical in layout and individual inconsistence of the device. Thus in actual design it is necessary to monitor the device voltage separately to ensure full ZVS to be achieved on with the upper and lower device. Once voltage in the junction capacitance for Q5 and Q8 has both reached zero, this stage ends.

During this period, the magnetizing current already starts to be charged as a positive voltage is applied. There is the minimum value for i_{Lm} at moment t_5 before positive voltage is applied.

$$i_{Lm}(\mathrm{t}) = -\frac{nV_o}{4L_m f_{sw}} + \frac{nV_o}{4L_m}(t - t_5) \tag{2-36}$$

When the voltage across Q5 reaches zero, the devices can be turned on at ZVS when this stage finishes. Thus the next cycle can begin from stage 1.

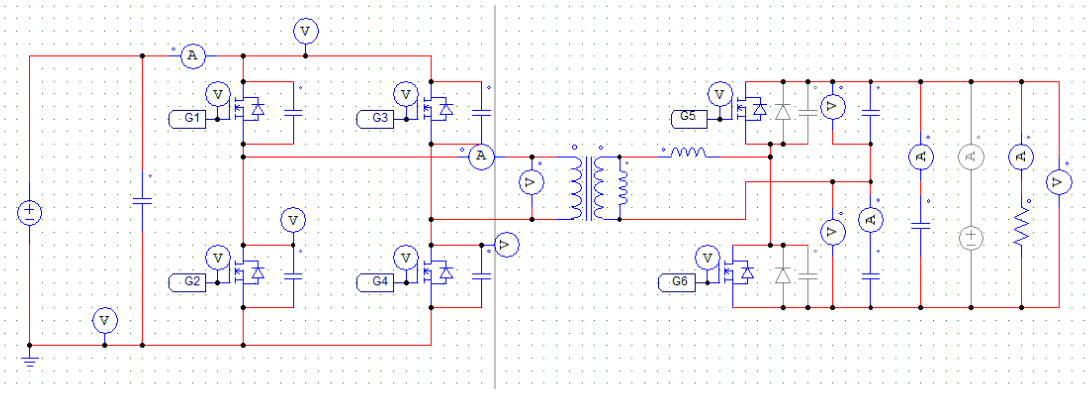
2.4 Simulation

To approve the functionality, software simulation is performed for the two topology. The platform used is Psim 11.0 running psim simulation. The parameter used for simulation are as follow.

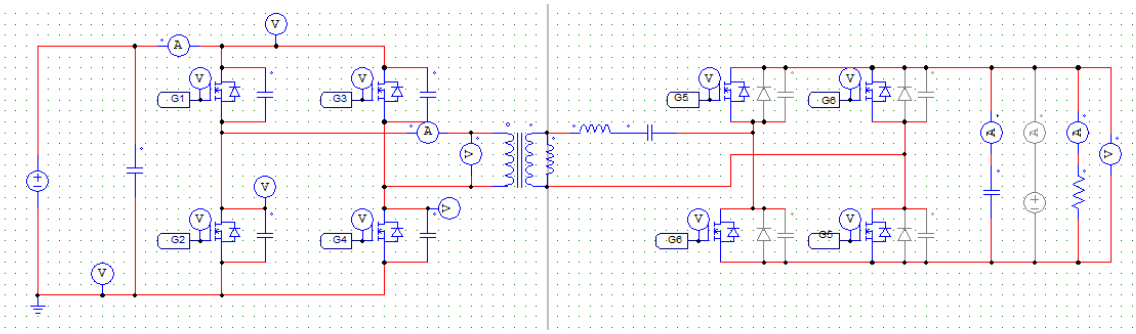
Table 2.1. Parameters used for the simulation circuit.

Parameters	Half-Bridge	Full-Bridge	Unit
L_m	0.75	0.65	mH
L_{lk}	40.6	40.6	μH
C_r	33	33	nF
Resonant Frequency	137.5	137.5	*kHz*
Switching Frequency	140	140	*kHz*
Transformer Turns Ratio	4:22	4:44	---

The constructed simulation circuit is demonstrated in following figures.



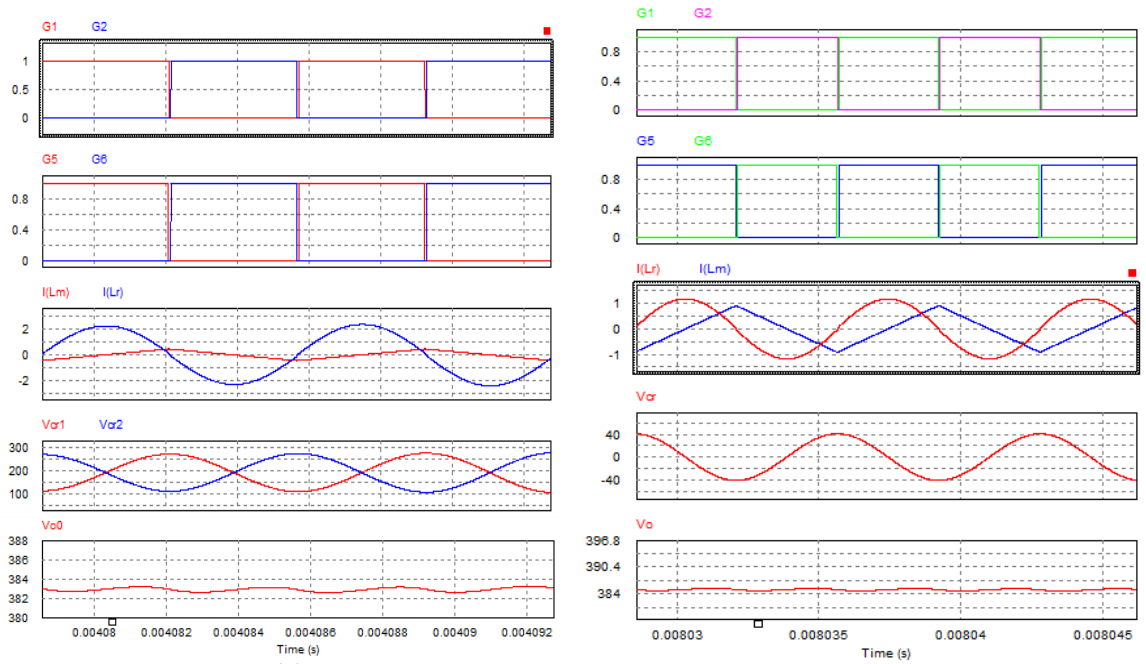
(a)



(b)

Figure 2.10. Simulation circuit for (a) Half-bridge Case; (b) Full-bridge Case.

Run simulation with the same specification: input 35 V and load of 300 W. Both circuit reaches stability and operates as anticipated SR operation. Plot monitored parameters and there are following waveforms. The simulation results are presented in Figure 2.11. It can be seen that the waveforms match that of the analysis from previous sections.



(a) (b)

Figure 2.11. Simulation waveform for (a) Half-bridge Case; (b) Full-bridge Case.

2.5 Extension of Operation

In addition to the synchronize rectification operation, above discussed active switch LLC converter has the capability of extending the operational range at fixed frequency through PWM control of primary and secondary rectification network. Some previous work has introduced such operation mode on similar circuitry. However, by using active rectification network, the same function can be achieved without additional device requirement. As PWM control method of LLC converter is not the focus of this work, only the principle operation concept is briefly covered in this subsection to approve equal functionality of the topology under comparison.

For PV microconverter, there is the need of MPPT, which requires the converter to be able to operate over a same wide range of input voltage both above and below the nominal

operating frequency. These require the ability of “buck” and “boost” operation of the resonant converter when operating at fixed-frequency. For the active secondary LLC converters discussed in this paper, these functions can be achieved through the front and secondary rectification network without the requirement of additional devices.

When the input voltage is higher than the designed nominal point, the converters can utilize the full-bridge front end to buck down the average voltage value before reaches the LLC converter transformer primary side. The function is achieved through the phase shift operation between the two leg of the full bridge. Control for the primary devices is illustrated Figure 2.12.

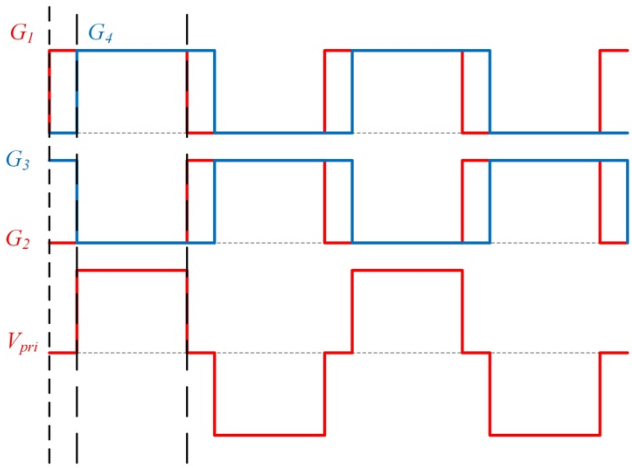


Figure 2.12. Primary Gate Operation for Input Voltage Higher than Nominal.

The boost operation is used when the actual input voltage is lower than the nominal voltage. In this case, the converter needs to further increase the secondary voltage value in addition to the ratio adjustment of the transformer. Referencing the operation of traditional PWM boost converter, this can be achieved by shorting the secondary and allow the

inductor current to be charged up. Specifically, the active voltage doubler or full bridge on the output end is used to short the transformer secondary side. The realization is different for the studied circuits.

For the Full Bridge topology, the boost operation is achieved by shorting across the entire secondary resonant tank to shorting transformer secondary side, as illustrated in Figure 2.13. The two conducting pass demonstrated are identical for performance. However, as such switching is not full soft-switching as the case of SR, one recommendation is to alternate the paths. This helps with dividing the heat generation, which alleviates thermal stress; while it also avoids overstressing one pair of the devices and causing unbalance wearing down, ultimately improve the unit lifespan.

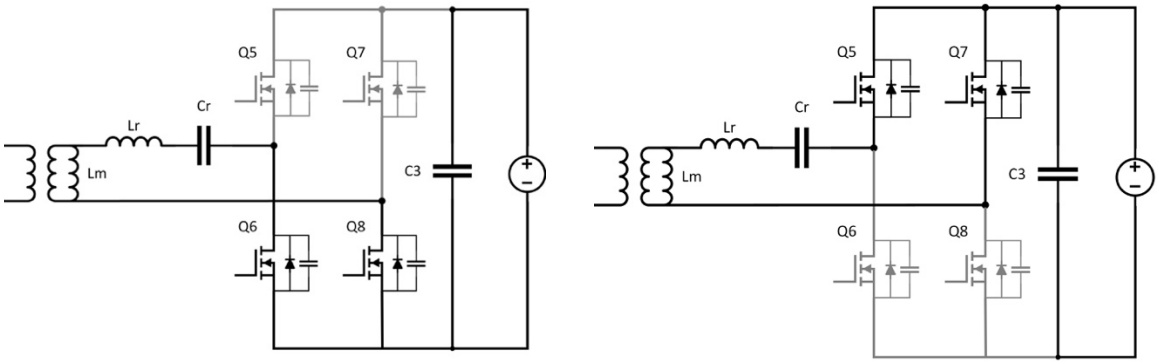


Figure 2.13. Secondary Active Full Bridge Secondary Device Boost Operation (a) Conducting through Q6 and Q8; (b) Conducting through Q5 and Q7.

For the Active Half Bridge topology, only one switch is turned on to shorting the resonant inductor. When the system is in boost operation mode, the opposite switch on the secondary HB needs to be forcedly turned on compared with SR in Stage 1 and 4. The circuit behavior is illustrated in Figure 2.14. below. For stage 1, Q6 instead of Q5 is turned

on at the t0. At this time, the inductor current direction is clamped by the voltage across the transformer. Thus the current will be forced to go through Q6 and C2, shorting the secondary of the transformer and allows the inductance to be directly charged. Similar behavior happens during stage 4: by turning on Q5 at the beginning of the stage, the transformer can be shorted through the pass of Q5 and C1. Boost operation is achieved.

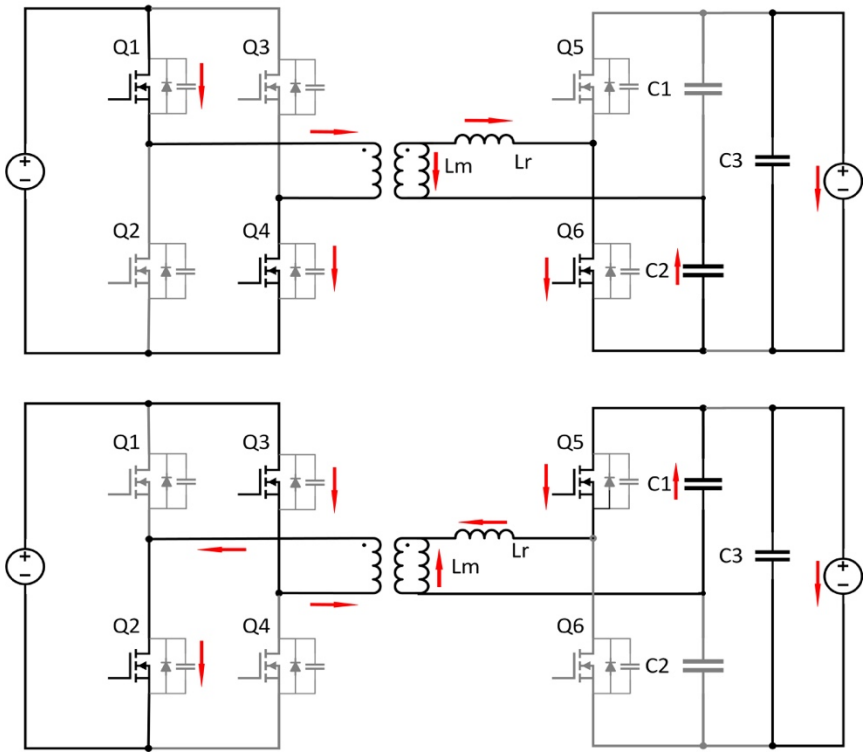


Figure 2.14. Boost Operation for Active Half Bridge Secondary Topology.

From previous analysis, it can be seen that the two secondary topologies have the potential of a same range of operation. All primary and secondary devices are active and separated control is required. Considering the complexity of operation and amount of devices, the same model of digital control devices can be used for both circuit operational control. This means auxiliary power assumption for control module in the circuit will be

similar in these circuits. Thus the comparison of the studied topologies should focus on the efficiency and device stress, which is the subject of the next chapter.

Chapter 3

Efficiency Analysis and Performance Comparison

3.1 Circuitry Analysis

In this section, several performance parameters are evaluated for the topology under study. As discussed in the previous chapter, the listed two circuits are able to provide the same function. Thus in the main part of this chapter, performance comparison focuses on the efficiency analysis. This section will discuss the losses on the circuit while magnetic component will be addressed separately in the next sub-section.

As stated in the introduction, this work focuses on the nominal point operation, specifically the operation of SR mode. The SR operation is the optimized operational point and at which the circuits under comparison, though have a different structure, operate in a similar manner. While in the more complicated operational modes the system performance depends on a lot of variables and becomes hard for a fair comparison.

Before loss analysis, firstly the system parameters are defined. With given input voltage at nominal input point V_{in} and output voltage V_o, the current in the circuitry is determined by the operating load, or the output power P_o. The transformer turns ratio is

determined base on nominal operating parameters and the system topology. For LLC with Full Bridge secondary, the transformer turns ratio are

$$\frac{1}{n_{FB}} = \frac{V_{in}}{V_o} \tag{3-1}$$

While for the Active Half Bridge Secondary LLC, due to the characteristic of the voltage doubler structure on the secondary, the turns ratio becomes half of the full bridge secondary case. There is

$$\frac{1}{n_{HB}} = \frac{V_{in}}{2 \cdot V_o} \tag{3-2}$$

Then the current in the circuitry can be determined. Note that for energy power calculation, the current parameters are in the Root Mean Square (RMS) value. For the studied converter, the ideal operating current waveform is in sinusoidal. Thus there are following relation between its peak value, the average value, and RMS value.

$$I_{AVG} = \frac{2}{\pi} I_{peak} \tag{3-3}$$

$$I_{rms} = \frac{1}{\sqrt{2}} I_{peak} \tag{3-4}$$

The current on the circuit secondary side can be described as the following equation.

$$I_{sec,FB} = \frac{P_o}{V_o} \tag{3-5}$$

$$I_{sec,HB} = 2\frac{P_o}{V_o} \tag{3-6}$$

Note that while the transformer turns ratio can be reduced to half utilizing voltage double, the current on the secondary is doubled.

Then the RMS current value used for device loss calculation can be de calculated.

$$I_{sec,rms} = \frac{\pi\, I_{sec}}{2\sqrt{2}} \tag{3-7}$$

Acquiring primary side current is more complicated as there is magnetizing current involved, which is determined by in the magnetizing inductance value of the transformer and its turns ratio, system switching frequency and voltage.

$$I_{Lm,rms} = \frac{nV_o}{4\sqrt{3}L_m f_{sw}} \tag{3-8}$$

Then the total primary side current value can be calculated.

$$I_{pri,rms} = \sqrt{(n \cdot I_{sec,rms})^2 + {I_{Lm,rms}}^2} \tag{3-9}$$

3.2 Power Stage Loss Estimation

Here the power stage loss refers to the losses on the power devices, specifically the active switches in the primary and secondary rectification network.

From the operation analysis in chapter 2, we have the following parameter waveform. On the primary side, there is equivalently two devices conducting throughout the switching cycle, as one pare of switch Q1 and Q4 conduct for the positive cycle and the other pair conduct for the negative half cycle.

$$P_{pri,cond} = 2{I_{pri,rms}}^2 R_{ds(on)} \tag{3-10}$$

The system utilizes LLC converter for its soft-switching advantage. However, there is one switching loss cannot be avoided: the primary device turn-off loss. Due to the magnetizing current, there is the peak value magnetizing current conducting through the primary when the conducting pair of devices switches off. Such turn-off loss has been studied extensively for LLC resonant converters. However, with the utilization of GaN devices, there still lacks sufficient data for approximation. The very fast switching speed makes it difficult for the switching loss estimation, and the device performance becomes dominated by the parasitic. A few modeling and estimation data are provided be manufactures and research facilities while some unexpected phenomenon has been reported by users and academia [38]–[42]. The estimation used here is proposed for similar circuitry and operation condition, and have the comparison data for both Si and GaN devices which validates the accuracy of the method [43]. The method takes consideration of magnetizing inductance, the junction capacitance of the device and the turn off speed of the device. The final formula that is adapted for this application is

$$P_{pri,off} = \frac{n^2 {V_o}^2 {T_f}^2 T_s}{C_{pri,Coss} {L_m}^2} \tag{3-11}$$

Here the T_f represents current full time. Note here the considered turn-off loss only limits to the discharging of device output capacitance. The body diode reverse conduction loss can be avoided with careful deadtime design and there is no reverse recovery charge for GaN FET devices. With the GaN FET very fast current fall at turn-off, the turn-off loss is relatively small. This is one of the reason that LLC is used in this application: the lossy

turn-on can be avoided by the Zero Voltage Switching (ZVS) turn-on when system operates below resonant frequency.

Also, complete soft switching is achieved for the secondary devices as analyzed in the previous chapter. Thus for the secondary side, the only device loss comes from the conduction loss during on-time in theory. For the half-bridge design, it equivalent to one device conducting through the switching cycle; while for fall bridge, the equivalent device number is two, similar to the full bridge rectification situation on the primary side. There is

$$P_{HB,sec,cond} = {I_{sec,rms}}^2 R_{ds(on),sec} \tag{3-12}$$

$$P_{FB,sec,cond} = 2{I_{sec,rms}}^2 R_{ds(on),sec} \tag{3-13}$$

The total device loss for the system can be expressed as:

$$P_{pri,off} = P_{pri,cond} + P_{pri,off} + P_{sec,cond} \tag{3-14}$$

3.3 Losses on the Magnetic Component

One of the major loss for the designed LLC converter comes from the magnetic components. For the compactness of the system, ideally, LLC converter can utilize the leakage inductance L_{lk} of the transformer to provide the inductance of the resonant tank. In reality, the transformer leakage inductance may not able to provide sufficient inductance for optimized system performance due to physical restriction or efficiency compromise. This section focus on the loss estimation for gapped transformer with good coupling, while magnetic optimization will be discussed more extensively in later chapter.

Firstly, consider the case without an external inductor. For the transformer, the loss model consists of core loss and copper loss. The core loss depends on the core material, size and the peak flux density. The core material is selected base on the required operating range and frequency while the choice in size and shape considers more on the efficiency. Given the selected core, the flux density can be calculated base on designed turns.

$$\Delta B = \frac{V_{in}}{4 \cdot nA_e f_{SW}} \tag{3-15}$$

With the given material, per volume core material loss can be read from core datasheet. In this application, a formula is extracted through data fitting for the specific core material and provider [44]. The selected 3C95 core is rated for optimized performance in this design's frequency and flux density range, while temperature variance is smooth. The per volume loss can be approximated as:

$$P_{core} = 92.16 \cdot f^{1.045} \Delta B^{2.44} C_T \tag{3-16}$$

Where C_T is the temperature coefficient that can be calculated as $C_T = 1.33236 - 7.94\times10^{-3} \cdot T + 4.6\times10^{-5} \cdot T^2$, where T is the temperature in Celsius degress.

For the conduction loss, the ac conductance in Litz wire needs to be studied. For high-frequency applications, Litz wire is used to reduce ac loss caused by skin effect. A properly design and selected Litz wire should be able to minimize conduction loss while mitigate the internal proximity effect by properly arranging the strands. Here is the formula provided by new England technology for accurate dc and ac conduction loss calculation [45].

$$R_{dc} = \frac{R_s \cdot 1.015^{N_B} \cdot 1.025^{N_C}}{N_S} \tag{3-17}$$

Here the R_s is the per length dc resistance for each strands of the litz wire, N_B is the number of bunching operation and N_C is the number of cabling operation with in the litz wire structure. N_S is the number of strands within the wire. All of the above parameter should be able to be acquired from the Litz wire data sheet, while noticing the unites need to corresponding through the calculation. Then the ac to dc resistive ratio is calculated basing on several factors considering ac effects

$$\frac{R_{ac}}{R_{dc}} = H + K\left(\frac{N_S \cdot D_1}{D_0}\right)^2 G \tag{3-18}$$

Here G is the eddy-current basis factor that can be calculated as $G = \left(\frac{D_1 \cdot \sqrt{f_{SW}}}{10.44}\right)^4$, where D_1 is the diameter of individual strand copper.[45] H is the individual strand ac to dc resistance ratio, which can be determined by individual strand gauge; K is a constant based on the total strands number; and D_0 is the diameter of the finished wire over strands. This formula considered the extensive factor of the complicated litz wire internal structure and accurately describes the conduction loss in the single wire. Again note the unites during calculation as the constant are developed using a specific unite system.

With above formula, the wire loss can be calculated depending on the wire type and wire length. Primary wire and secondary wire should be considered separately; conduction loss is calculated using the RMS current value on each side.

$$P_{copper} = {I_{rms}}^2 R_{ac,total} \tag{3-19}$$

The $R_{ac,total}$ here represent the ac resistance of the actual length of wire; and for accuracy of calculation, a one-inch solid copper conductor ac resistance is added-in to simulate the connection terminal of the Litz wire to the board.

3.4 System Comparison and Verification

For verification, circuit boards are built for analog testing. In accordance with the intended application, both the half-bridge and full-bridge system perform dc-dc power conversion that bridges the voltage ratio between PV panel and dc-bus for transmission. The output is 380 V constant and input is at the 35 V nominal output voltage for PV panels. The power level for the systems under discussion are both 300 W. For the benefit of comparison, the tested half-bridge and full-bridge circuits are modified using the same board and the adjustment is minimal. Also, both circuits use the same switching devices in the primary and secondary rectification network accordingly. The devices and specification for the analog circuitry are as follow.

Table 3.1. Device Model and Power Stage Specification

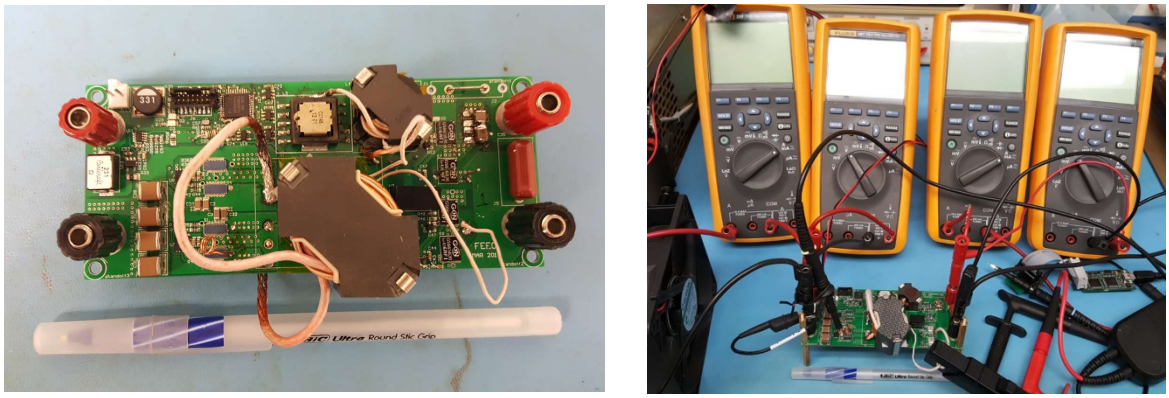
Item/Parameter	Specification
Input Voltage	30 V
Output Voltage	380 V
Power	300 W
Switching Frequency	140 kHz
Primary Device	EPC 2021
Secondary Device	GS66502S

As discussed in the previous subsection of this chapter, there is a few differences in the circuitry power stage behavior under same operation point for the full-bridge and half-bridge topology, especially at the secondary side. Thus the operational parameter and the resonant tank design has some variation between the two topologies under discussion. Table. 3.2. here listed the value of these parameters.

Table 3.2. Circuit Parameter Comparison and Values

Parameters	Half-Bridge	Full-Bridge	Unit
L_m	0.66	0.60	mH
L_{lk}	41.45	42.62	μH
C_r	33	34	nF
Resonant Frequency	136	132	kHz
Switching Frequency	140	140	kHz
Transformer Turns Ratio	4:22	4:44	---

The goal here is to ensure the maximum similarity during operation for the given two topologies. As can be seen in Table 3.2., the resonant frequency is set to approximately same value through the selection of the tank component. The resonant tank is consisted of a resonant capacitance and also an inductance component, which including the leakage inductance and the external resonant inductor if used. As the transformer requires different turns ratio, the associated parameters present large difference in value. Thus the external inductor helps to maintain the structure of the resonant tank. Still, the secondary structural differences and the parasitic introduces brings about the difference in system performance. It will be discussed in a more detailed manner through later chapter.



(a) (b)

Figure 3.1. (a) Full-Bridge prototype; (b) Half-Bridge modification with testing set up.

Here is the hardware testing result for system verification. Figure 3.2. presented the operation waveform under optimized operational point. The system switching frequency is designed to very close with the resonant frequency. Thus DCM conduction mode is minimized for efficiency consideration.

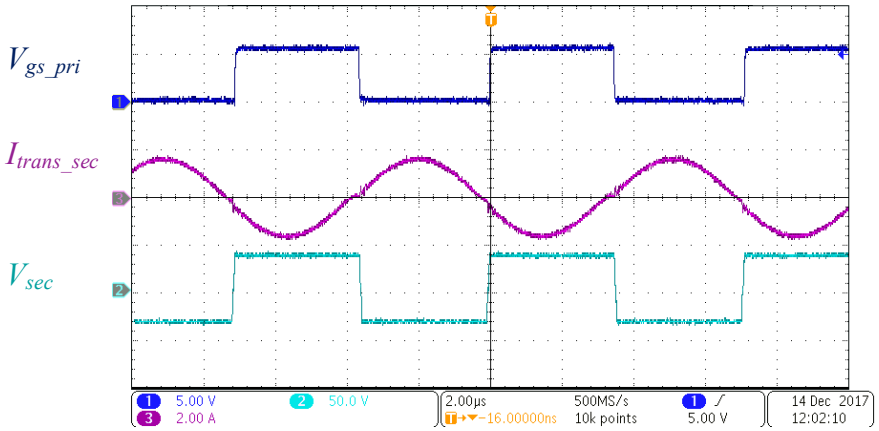
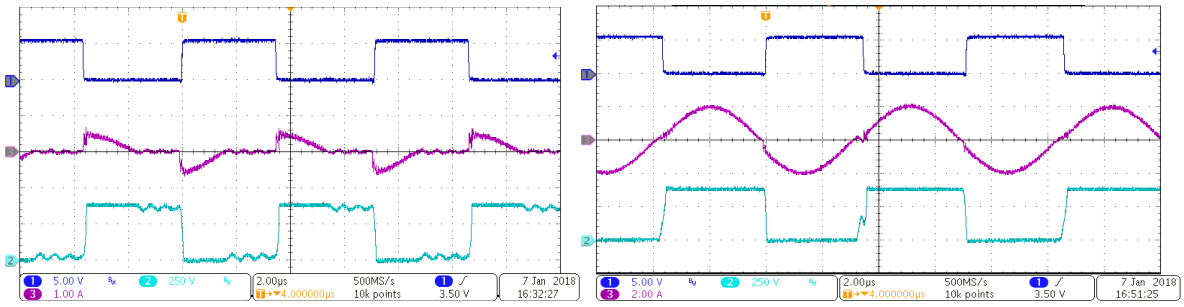


Figure 3.2. Operation Waveform for Half-Bridge under 200W Load.



(a) (b)

Figure 3.3. Additional Operation Waveform for Half-Bridge Topology: (a) under light load (b) under full load.

For full bridge topology, operation waveform is similar. The optimize operational point waveforms are presented in Figure 3.4. There are a few differences: as previously analyzed, the secondary current in full-bridge topology is half of the full-bridge case; and

due to the slight difference of resonant frequency in hardware setting, the DCM period is more noticeable under same switching frequency.

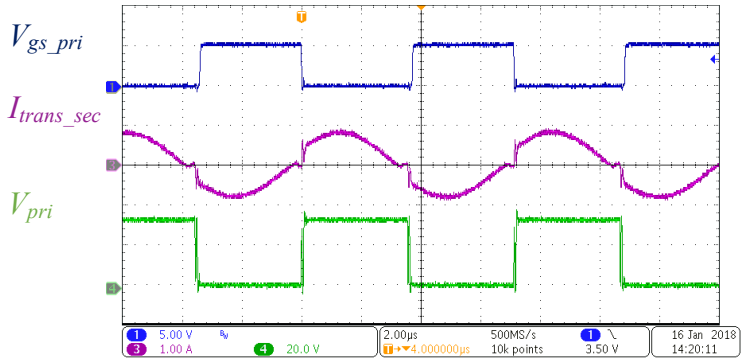
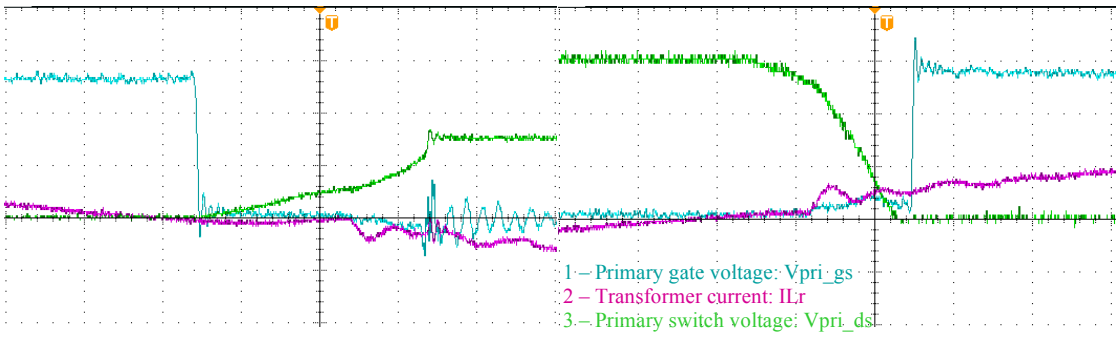


Figure 3.4. Operation Waveform for Full-Bridge under 200W Load.

One key factor for ensuring efficiency optimization is the full soft switching for LLC converters. For LLC converter operates at lower frequency than the resonant frequency, ZCS is a given. Also, deadtime is designed then toned for minimum yet sufficient discharging.



(a) (b)

Figure 3.5. Soft switching verification of primary side: (a) ZCS of primary devices; (b) ZVS of primary devices.

With full soft switching, then efficiency evaluation is performed for the system. Power loss is calculated for different load condition with the same operating point for both full bridge and half bridge converter accordingly.

Before analyzing the differences and consider possible causes, detail loss breakdown are shown for some of the key efficiency points, as seen in Table 3.3. It is also true that the testing efficiency also varies between testing sections as the environmental condition changes.

Table 3.3. Estimation of each loss category and comparison with measured efficiency at different load point using half-bridge case.

	200 W	**300 W**
Primary Current	7.646 A	10.49 A
Secondary Current	1.169 A	1.754 A
Primary Conduction Loss	0.350 W	0.661 W
Primary Switching Loss	0.215 W	0.215 W
Secondary Conduction Loss	0.41 W	0.98 W
Transformer Core Loss	0.49 W	0.49 W
Transformer Winding Loss	0.378 W	0.755 W
Inductor Loss	0.350 W	0.407 W
TOTAL LOSS	2.181 W	3.437 W
ESTIMATED EFFICIENCY	98.90 %	98.87%
MEASURED EFFICIENCY	98.78%	98.72%

Estimation for each category is calculated using formula listed in this chapter. Detailed calculation result for each category is listed in Table 3.3. Estimation of each loss

category and comparison with measured efficiency at different load point using half-bridge case. This helps to understand the main contribution for the system loss.

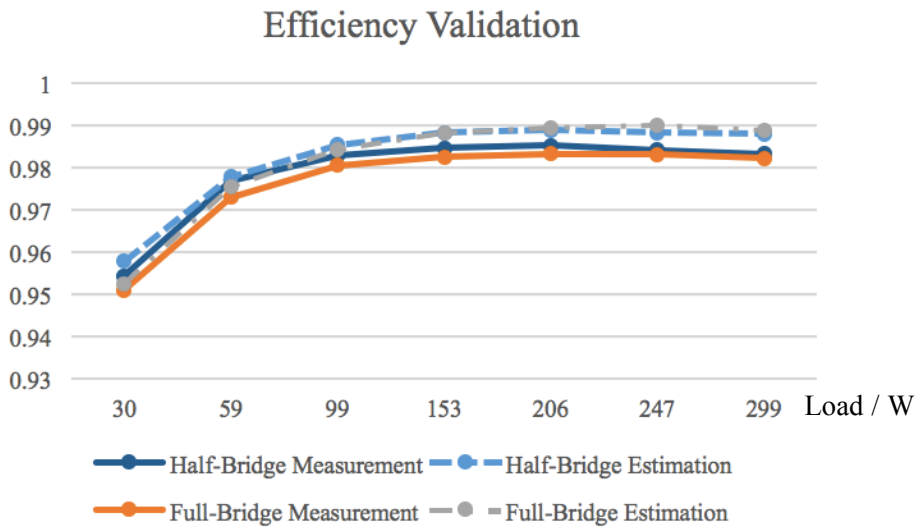


Figure 3.6. Efficiency across load range comparison for Half-Bridge Topology

As can be seen from above figure, the efficiency estimation shows similar value and same trend while the load condition changes. There exists some stable margin between the theoretical value and the actual testing.

From table and figure above we can see the efficiency estimation is very close to the tested result. The differences most likely contributed by the following area:

1) The complicated dynamic conducting resistance for GaN switches. Unlike traditional silicon MOSFET, the $R_{ds(on)}$ has been noticed to have a dynamic characteristic during the operation. The resistance can be several times larger during switching time than that during stable conduction.

2) Unclear switching loss characteristic of GaN devices. In addition to the advantage of faster switching and no-loss recovery, the GaN devices also have its cons with switching control as a stricter driving voltage is required. Also, the internal nonlinear switching model is still immature for accurate performance description.
3) Difficulty in calculating higher frequency ringing ac loss. As can observe from the above waveforms, there exists higher frequency ringing in the conducting current waveform. The ringing amplitude is minimum. Thus the effect on current RMS value is relatively small. However, high-frequency Litz wire ac resistance can be magnitudes higher than that of its dc value. Thus the resistance loss becomes more prominent than desire.

During different sections of testing, a change in testing efficiency result is also noticed at similar testing point. The main factor here is the temperature of operation. Several circuit components are rather sensitive to its operating temperature: the ferrite core loss increases when the core is at cool ambient environment rather than the designed operating temperature; while the conducting resistance of switching devices increases when temperature rise. Another part that brings difficulties to efficiency estimation is that the operating loss of one part may affect other elements on the board. The most significant case is the magnetic component: the higher copper loss at heavy load situation introduces heat to the wire, which warms up the core and changes the core operating character. Such interaction is too complicated to be considered in a numerical calculation, while the impact is prominent.

Chapter 4

Magnetic Optimization

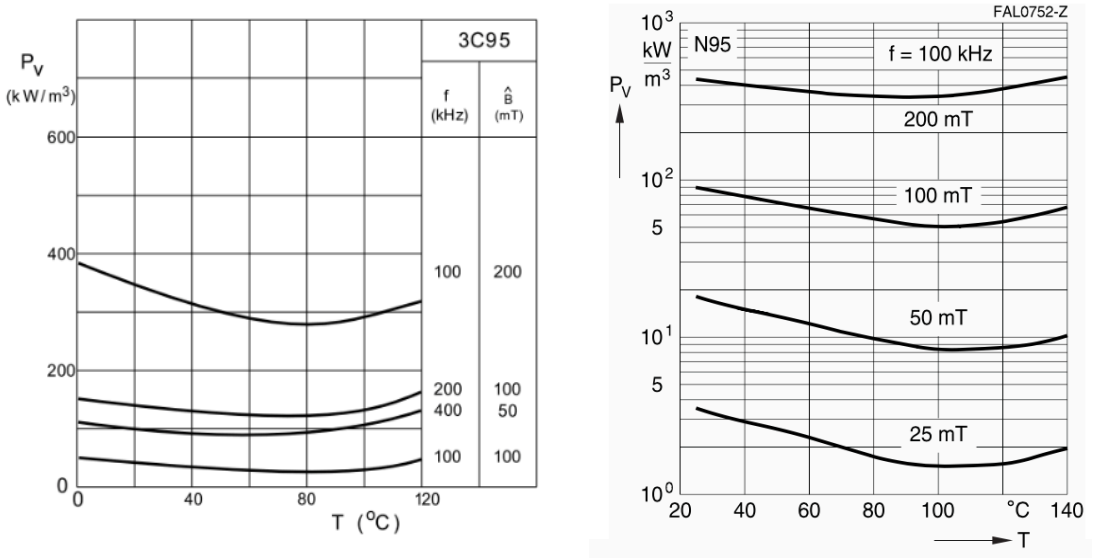
4.1 Transformer Overview

The soft switching LLC converter multi-tasks the transformer: it serves as galvanic isolation with a certain voltage transforming ratio, provides resonant inductance with the leakage inductance and also assists soft-switching with the magnetizing inductance. However, to balancing all the parameter while maintaining high-efficiency performance requires dedicated design of such magnetic component.

The transformer turns ratio is decided by the required voltage conversion as LLC have fixed conversion ratio under fixed-frequency operation. Equation (3-1) and (3-2) presented the calculation formula, while the required ratio is different for the half-bridge and full-bridge case. Duo the characteristic for the active voltage-doubler as secondary rectification architecture, the turns ratio for half-bridge topology is half of that for the full-bridge case.

With that, first consider core selection for the transformer design, which includes the determination of material and size/shape. For core material, the affecting factors are operating frequency and temperature. As previously listed, the operating frequency is listed at 140 kHz. It is set with consideration of efficiency and potential EMI noise. The application for the topology under discussion is PV optimizer, which is usually mounted

under the PV panel on roof-top or open space with direct sunlight. This means the ambient temperature can be relatively high. Adding in the temperature rise during operation, each component of the system needs to be able to stand 60°C to 90°C while being effective in operation. Here the transformer is optimized around 70°C temperature. There are a few ferrite materials for this frequency and temperature range.



(a) (b)

Figure 4.1. Power loss density for specific flux density and frequency combination through temperature range for (a) 3C95 core material; (b) N95 Core material.

Then consider the core shape and size. For this part, parameters involved in the power stage need to be considered. Primarily is the magnetizing inductance, which provides the magnetizing current for discharging during soft switching. There is a relation between the magnetizing current peak value and magnetizing inductance of transformer as listed in (3-8). The value of L_m relates to the turns number and core shape.

$$L_m = \frac{\mu N^2 A_e}{l_m} \tag{4-1}$$

In (4-1), μ is the material permeability for the selected core material, A_e is the effective area and l_m is the effective magnetic loop length. In actual application, the available turns number is limited by the allowed profile as it limits the core dimensions and the window area. Then the magnetizing inductance value is tuned by changing the air-gap of transformer, which changes the equivalent permeability.

The main design consideration here is the core loss. Equation (3-15) and (3-16) describes the relation between operating parameter, peak flux density and per-volume core loss. From the core selection point of angle, the main factors are the effective area and loop length. Generally, the desired core should have a relatively large effective area A_e yet small loop length l_m. With the same flex density, such core would generate less energy loss on the ferrite; and to achieve the same magnetic current, smaller air gap is required, which in turn reduces friendging effect. With above consideration, two core of a similar class is selected for comparison.

Table 4.1. Core Parameters for Comparable Model/Shape.

Parameters	RM14/ILP Core	PQ 32/30 Core
Material	N95	3C95
Effective Length l_m	50.9 mm	55.9 mm
Effective Volume V_e	10230 mm^3	9440 mm^3
Effective Area A_e	201 mm^2	169 mm^2
Core Factor ($\Sigma l/A$)	0.25 mm^{-1}	0.331 mm^{-1}

Then consider winding design. Here the selected wire is Litz wire for its advantage in reduced high-frequency ac loss. For Litz wire, there are two parameters to be determined: the string gauge, which is selected base on the frequency of the conducting current; and the total equivalent gauge, or the number of string included, which is decided by the current value. For the hundred kHz range frequency operation, the suitable Litz wire substring should be #42 and above. In resonant converter here is the potential for higher frequency noise, especially on the secondary side. Thus the wire used for implementation is higher rated: #46 Litz wire is used for transformer winding.

Table 4.2. Comparison between Different Core Configuration and System Efficiency at 200 W load.

	PQ32/20	**RM14**	**RM14**	**RM14**
Turns Ratio	3: 19	3: 19	3: 19	4: 25
Interleave	No	No	Yes	Yes
Gap	3 mil	2 mil	2 mil	3 mil
L_m	1.9 mH	0.5 mH	0.5 mH	2.1 mH
L_{lk}	9 μH	7.97 μH	4.63 μH	6.34 μH
Winding Loss	0.3 W	0.3 W	0.3 W	0.38 W
Core Loss	1.4 W	1.04 W	1.04 W	0.61 W
Efficiency	98.16%	98.23%	98.37%	98.49%

Table 4.2. presents the efficiency improvement with each change of optimization. By changing core type, the core loss reduction contributes to improved system efficiency; interleaving the wire reduces the coupling loss. Then while window area allows, changing turns number to reduce peak core flux density can further reduce core loss. Overall, optimization of the transformer design improved the system efficiency by 0.3 %.

The overall transformer design and the corresponding parameter is listed in the following table.

Table 4.3. Final Transformer Parameters.

Parameters	Half-Bridge	Full-Bridge
Core	RM14/ILP	RM14/ILP
Primary Wire	Litz #44/14	Litz #44/14
Secondary Wire	Litz 330*#46	Litz 175*#46
Primary Turns Number	4	4
Secondary Turns Number	22	44
Air Gap	3 mil	5 mil
Interleave	Yes	Yes

The final core selection is based on efficiency superiority. The RM14 core has a very low ratio of effective length to effective area, which reduces flex density when transformer design remains the same. In turn, the per volume loss is smaller while maintaining the same flux density. Also, the window profile is sufficient and effective for the required wire and turns requirement.

Also, there are a few differences between the half-bridge and full-bridge design. Besides the different turns ratio, the full-bridge transformer utilizes a smaller magnetic inductance, creating a larger magnetic current during operation. This is to match the relatively higher secondary device junction capacitance of discharging.

4.2 External Inductor and Other Issue

While it is convenient to use solely the leakage inductance from the transformer as the resonant tank inductance, the leakage inductance value may not be sufficient for the resonant tank design. For the performance of the resonant tank, the total inductance L_r and

resonant capacitance C_r need to be proportional for the benefit of quality factor. There are methods to increase the leakage inductor from the same transformer turns. However, it significantly increases loss on the transformer as it requires purposely creates poor coupling between the primary and secondary winding. Thus such approach is not appropriate in this application as it defeats the purpose of efficient system design. In this case, internal inductor is also included and its added to the total resonant inductance value.

The external inductor is constructed using the same core material and Litz wire as the transformer secondary winding. The core used is RM9 for the small footprint and low profile. While it is sufficient for creating the inductance value required. Table 4.4. listed the design parameter for the external inductor in use for the design.

Table 4.4. External Inductor Design Parameters.

Item/Parameter	Specification
Core	RM9/ILP
Material	3C95
Wire	330*#46
Gap	5 mil
Inductance	33.6 μH

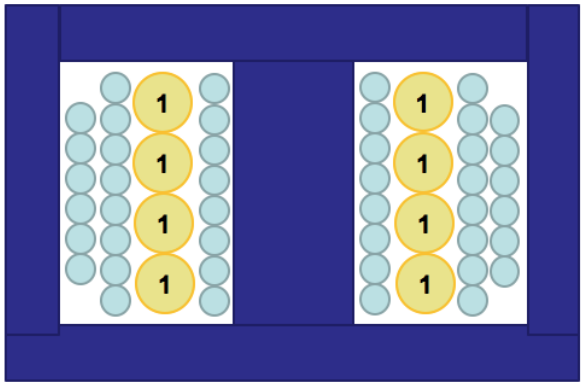
Another issue introduced by the transformer design is the winding capacitance. As there is a voltage drop between each turn of the transformer winding, it creates a small capacitance in between. In total, this incidental parasitic can be modeled as a capacitor across the transformer winding terminal. As been noted in some previous work, its value is affected by the turns number and winding structure of the transformer. Usually the parasitic is in a few to tens of pF level.

While its effect on the circuit performance is analyzed in the next chapter, the principle here is to reduce this value to as low as possible. Here are a few principles for reducing winding parasitic and its effect:

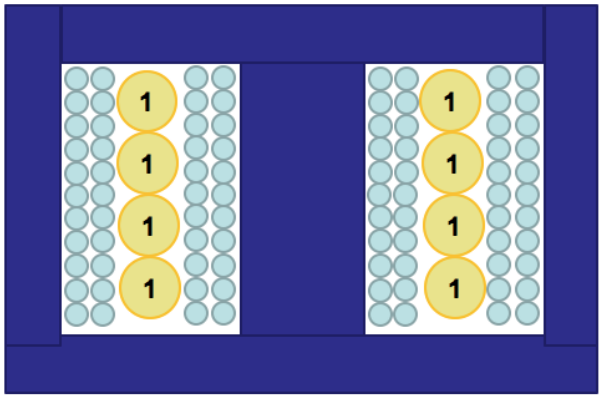
1) Increasing distance between layers of winding. The capacitance value is in reverse proportion to the separation between conductive. Thus by increase the layer separation, especially between layers of same side winding, the capacitance created can be reduced.
2) Separate layers of winding from the same transforming side. This falls under the same principle of the previous point. By interleaving the primary and secondary winding, the distance between windings of the same side significantly increase. In turn, winding capacitance between the two terminal of the same side is reduced.
3) Avoiding adjacent winding with large ordinal number jump. For the same side winding, the voltage differences between each consecutive ordinal winding are approximately uniform. The charge in the same winding capacitance is in square ratio to the voltage difference.

$$W_{stored} = C \cdot V^2 \tag{4-2}$$

As previous stated, the closest winding turns creates the largest parasitic capacitance. Thus by limiting the ordinal jump between the adjacent wires, the circulating energy created by the parasitic capacitance can be reduced.



(a)



(b)

Figure 4.2. Transformer configuration for: (a) half-bridge secondary; (b) full-bridge secondary.

In reality, the structure of winding and the allowed separation is limited by the core window room, wire size and standardized manufacturing consideration. The cross-section for the winding structure is demonstrated in Figure 4.2. For the full-bridge secondary LLC transformer design, separation layer of Kapton tape is used in between each layer of wires to reduce the parasitic capacitance.

4.3 Summary

Overall, the magnetic design for full-bridge secondary topology is more complicated than that of the half-bridge secondary LLC. Both cases need external inductor for sufficient resonant inductance value, whose design is rather straightforward. The main challenge remains with the transformer design. Given the same design specification, full-bridge transformer requires twice of the turns number on the secondary side. The large turns number of secondary winding creates a large parasitic on the transformer that cannot be avoided. The same reason also causes issues with physical limitations of wire window area and winding structure for manufacturing.

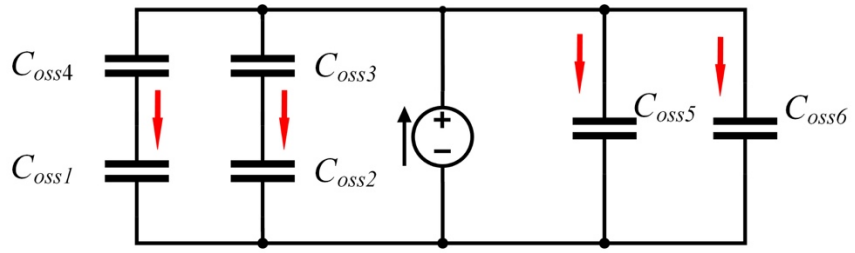
From efficiency and performance perspective, half-bridge transformer also has the advantage. The fewer turns of secondary winding means shorter conducting distance and less copper resistance. Considering the operating of the entire system, though full-bridge topology has half of the secondary current value, the loss from the secondary wire is still larger for this case. Another consideration is the related issues caused by the larger parasitic. Firstly, a larger magnetizing current needs to be generated for sufficiency discharging to ensure ZVS. Then the parasitic itself also causes ringing, which is at a higher frequency range. Thus higher frequency ac conduction loss becomes an issue for the transformer and external inductor winding.

Chapter 5

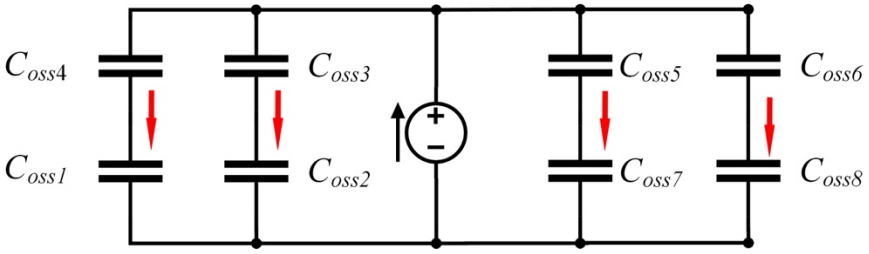
Secondary Parasitic Effects

5.1 LLC Soft-Switching Requirement

One goal of LLC converter is to achieve soft-switching for both the primary and secondary devices. However, as was stated in the circuit operation analyze, the magnetizing current that assisting the ZVS discharges the FET junction capacitances of primary and secondary side simultaneously. This current sharing creates difficulty in transformer magnetizing inductance design and deadtime tuning for both primary and secondary devices.



(a)



(b)

Figure 5.1. Equivalent Discharging Circuit During Stage 5: (a) Half-Bridge Secondary Architecture (b) Full-Bridge Architecture.

The discharging behavior during stage 5 in circuit analysis is demonstrated in Figure 5.1. For the discharging phase in stage 2, the equivalent circuit is the same only with reversed current direction. Thus in hardware implementation, instead of considering only the discharging of primary device junction capacitance, both the primary and secondary total equivalent junction capacitances need to be considered. Most of the existing works consider the issue with a static approach: the magnetizing current discharges the total value of primary and secondary parasitic capacitance. Under this condition, the estimated magnetizing current is:

$$I_{Lm} = \left(C_{pri} + C_{sec}\right) \cdot \frac{2V_{in}}{t_d} \tag{5-1}$$

However, in reality, the deadtime length and the magnetizing current value cannot be arbitrarily chosen. The discharging current during deadtime is not a constant value. Rather, the current shows an oscillation between the resonant inductor and primary and secondary parasitic capacitances. To demonstrate, the deadtime current waveform under purposefully extended deadtime is shown in Figure 5.2.

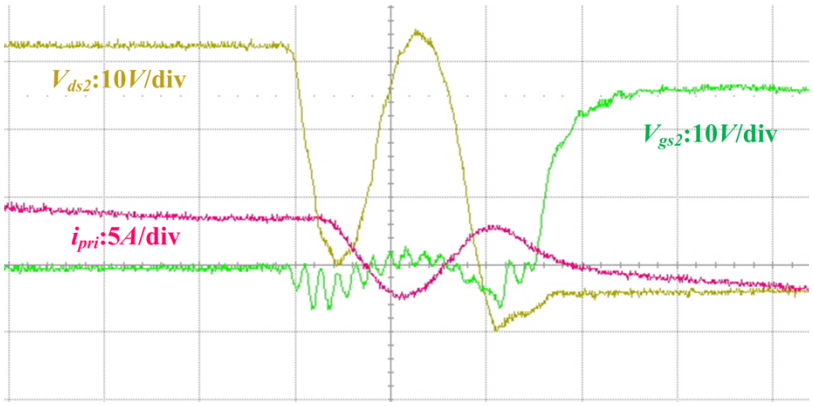


Figure 5.2. Primary Side Waveform during Extended Deadtime.

From above figure, it is easy to see there can be multiple appropriate deadtime lengths existing for the ZVS of primary and secondary time. However, longer deadtime means reduced energy conducting period. This means the effective energy transmission through the system is done in shorter period of time during operation. The increased current RMS value decreases efficiency. Also, the ringing during deadtime creates circulating energy, which also potentially compromises efficiency. Thus, it is desired to have sufficient discharging current to allow the primary device junction capacitances to be fully discharged before the oscillation on junction voltage happens.

5.2 Additional Parasitic Effect

The ideal operation of LLC offers ZVS with clean sinusoid current waveforms. However, the parasitics in the circuit and component are unavoidable in reality. These non-idealities create distortion and ripple during operation. One of such parasitic is the transformer winding parasitic capacitance mentioned in the previous chapters.

At the switching moment of each half cycle, the voltage across transformer secondary side winding capacitance need to flip direction, while the current on the leakage inductance and inductor continuous conducting. Thus the discharging process causes circulating energy in the circuitry, which resonants with the leakage inductance of the transformer and introduces ringing in transformer current.

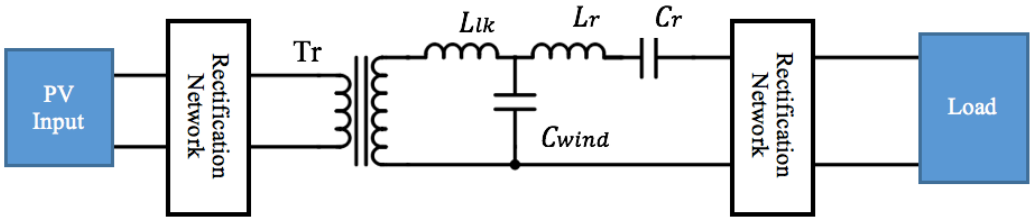
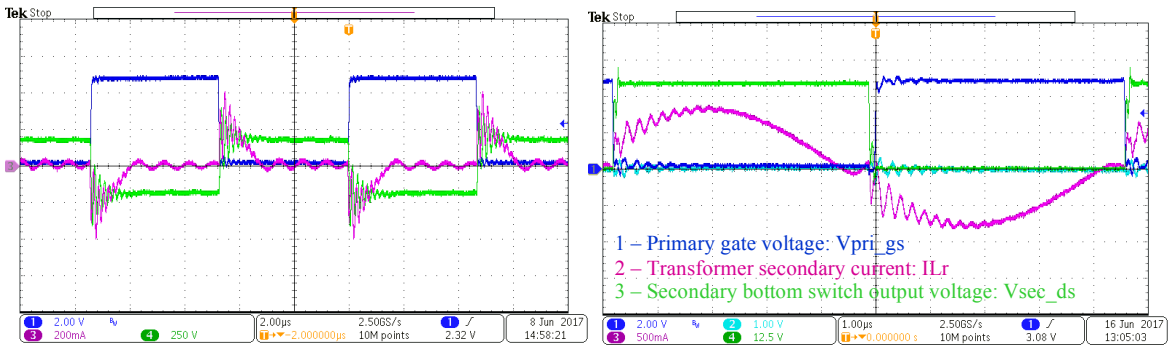


Figure 5.3. Circuit Model Considering Transformer Winding Capacitance.

Such distortion becomes especially prominent with the high turns ratio in this application, as the reflected capacitance in the non-isolated equivalent circuit become larger, thus creating more significant impact. Here the sample waveform is demonstrated using full bridge case.



(a) (b)

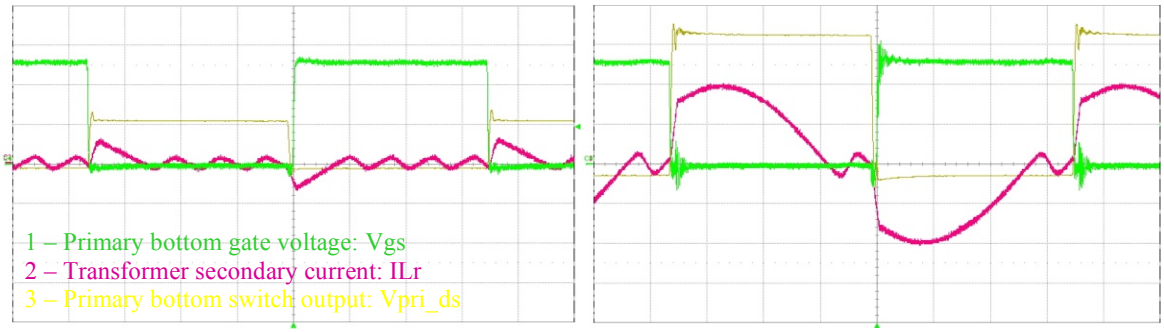
Figure 5.4. Ringing on the resonant current waveform under (a) Light load condition; (b) Heavy load condition.

This also verifies the previous analysis. In this specific testing, the winding capacitance on the secondary side is measured to be 17.2 pF while the secondary leakage inductance is 24 μH. According to previous analysis, there should be ringing at frequency

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{5-2}$$

With above parameters, the ringing frequency is expected to be around 7 MHz. The ripple on the resonant current happens as soon as the secondary voltage flips, and the ringing frequency is measured at 7.4 MHz.

Then to solve this issue, the straightforward approach is to increase transformer leakage inductance and decrease winding capacitance. This can increase ripple frequency and also increase the loop impedance thus allow the ringing to be damped out faster. However, such solution cannot fully resolve the issue as the circulating energy are still created at each half switching cycle. Also, the ability to change those parameters can be limited due to circuit function requirement or physic limitation. One simple solution is removing the external inductor and fully utilizing the leakage inductance for the resonant tank.

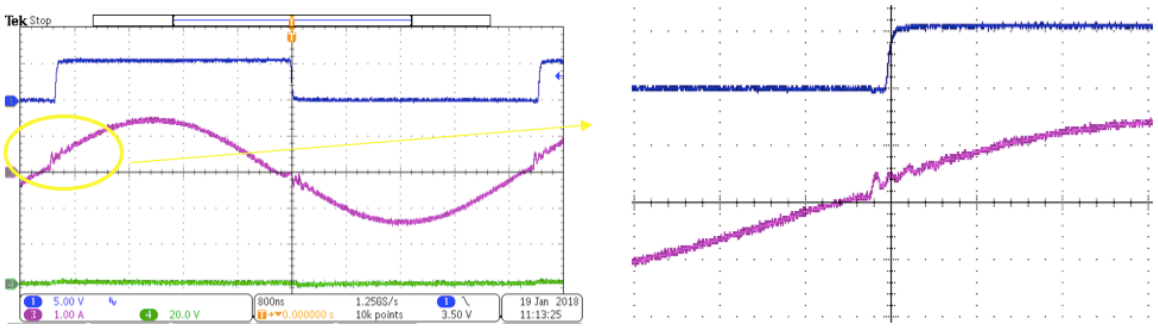


(a) (b)

Figure 5.5. Improved Testing Waveform (a) Light Load Condition (b) Heavy Load Condition

However, this solution might not be appropriate for all LLC board design. As previously have stated, the inductance value that is required in this work cannot be satisfied by leakage inductance alone. Thus the phenomenon can only be alleviated with other methods. The winding capacitance can be controlled with proper winding structure

configuration listed in the previous chapter. Also, increase Q factor of the resonant tank can help the ringing to be damped out faster, thus have less effect on the current waveform.



(a) (b)

Figure 5.6. Winding parasitic effect for Half-Bridge secondary topology (a) current ringing (b) zoom in of switching time.

From this perspective, the half-bridge also has the advantage. As fewer turns are needed for the transformer secondary winding, the parasitic winding capacitance is significantly less than that of the full bridge topology with same resonant tank design. As can be seen in Figure 5.6., the current ringing at switching moment, though still exists, has much smaller amplitude and are damped out faster. Thus relatively clean current waveform can be achieved with the use of external inductor for the half-bridge secondary topology.

Chapter 6

Conclusion and Future Work

6.1 Conclusion of Work

PV microconverter is an application that is drawing increasing attention as the solar energy harvest becoming increasingly popular and accessible. Rather than the basic functionality, optimization and efficiency are required for the power conditioning system for PV panels. Modularized solution and compatibility for different power system structures with inclusion of PV is demanded by the market. One favored topology for the application is LLC converter for the dc-dc power conversion from PV panel to dc power bus voltage. While the LLC converter has been studied and utilized for a long time and vast of work has been done, the topology needs to be optimized for specific application requirement. Two sub-structures of LLC secondary design of similar functionality have drawn the attention during exploration of the better performance among the alternative solutions.

This work focuses on the comparison of the two different secondary resonant tank and rectification network structures: (1) active full-bridge secondary rectification with resonant tank on the secondary side, and (2) active half-bridge voltage doubler rectification incorporating resonant tank on the secondary side. The two structures are studied fromtheoretical and actual performance perspective and compared in several aspects.

Firstly, the operation of the circuit is analyzed in detail. For both converters, the step-by-step operation breakdown is conducted. From the system level, the two circuits go through similar stages of performance: resonance conducting and separate primary and secondary deadtime control to achieve soft switching. In circuit structure, secondary operating method and parameter are different and brings related advantage and issue for performance and efficiency. From the discreet device point of view, the same maneuver is achieved with different device control, especially on the secondary device switching control. The discharging of secondary device junction capacitance requires different control method during deadtime. Also, further control method for extended system functionality is briefly explored. In this part, the purpose is to prove the equivalence of the two circuits in functionality. It is the foundation for later study, as the performance and efficiency comparison relies on the assumption that the circuits under study are compatible with this application.

Then the focus is on the performance and efficiency comparison between the two systems. Loss model is provided for all major components of the circuit. Analog circuit testing is also included in this section for verification and hardware performance comparison. While the estimation and hardware verification agrees in general, explanations for the difference are provided and supported by the phenomena observed during testing. One detail is the hardware testing in this work also incorporating the GaN devices, which the device performance model is yet to be perfected from vast study and performance data collection.

Remaining part of the work focuses on detail optimization for transformer and alleviation of parasitic effect. Parasitic components not only cause energy losses, but also create potential difficulty for effective system design. The key component of optimization in this section is the transformer. The transformer is the largest component in the physical profile and the crucial component for efficiency. Reducing the loss of the transformer itself and its associated parasitic components require design optimization and some design tradeoff. While the parameters can be calculated, some structural decisions need to be made based on physical constraint.

Overall, active voltage doubler implementation has the superior performance in the SR operation for high ratio voltage boost LLC converter. It provides very high efficiency of operation even for resonant converter operation. The hardware implementation requires less number of devices while still able to achieve all operation functionality through control. The voltage doubler also has the advantage of easier transformer design and introduces less parasitic in the process. This, in turn, further promotes the efficiency advantage.

6.2 Future Work

Though the purpose of this work is to provide comprehensive performance comparison for the given two topologies under study, further work can be done to improve efficiency with detailed modeling and system behavior, especially under dynamic operation.

The circuit utilizes GaN devices which brings difficulty in estimation of switch performance. Extended research work is yet to be done with GaN devices behavior modeling. It will help engineer better anticipate the device performance and provide appropriate operating condition and control signal for optimized performance. For such study, it is especially important to establish quantitative modeling method that is supported by hardware testing verification.

On a similar note, field simulation and systematic study of the entire the magnetic component, specifically the transformer can be done for further verification. Another explanation provided in this work to fill the discrepancy of estimation and measured efficiency difference is the fringing effect and inter-winding proximity effect. Both problems require the input of the 3D transformer structure with the core material and considering the interaction. High calculating power finite element analysis is the method for closest accurate description. Also, the ac loss estimation incorporating ringing component in the circuitry would also benefit the further accurate consideration of this topic. Ahough all above factors together only affect a small portion of the total loss, as the efficiency being further pushed to a higher level, the accuracy in detail becomes crucial for further optimization.

Reference

[1] Statistics Division, “2014 Energy Statistics Yearbook,” New York, USA, 2017.

[2] United Nations Development Programme, “UNDP Sustainable Development Goals,” 2017. [Online]. Available: http://www.undp.org/content/undp/en/home/sustainable-development-goals/goal-7-affordable-and-clean-energy.html. [Accessed: 04-Nov-2017].

[3] REN21, *Renewables 2017: global status report*, vol. 72, no. October 2016. 2017.

[4] D. A. R. Wati, “Maximum Power Point Tracking of Photovoltaic Systems Using Simple Interval Type-2 Fuzzy Logic Controller based on Hill Climbing Algorithm,” in *2016 International Seminar on Intelligent Technology and Its Application*, 2016, pp. 687–692.

[5] Y. Huang, F. Z. Peng, J. Wang, and D. Yoo, “Survey of the Power Conditioning System for PV Power Generation,” in *Power Electronics Specialists Conference*, 2006.

[6] C. Chen and Y. Chen, “Analysis of the Series-Connected Distributed Maximum Power Point Tracking PV System,” in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 3083–3088.

[7] C. Chen, S. Member, C. Liao, S. Member, and K. Chen, “Modeling and Controller Design of a Semi - Isolated Multi - Input Converter for Hybrid PV / Wind Power Charger System,” vol. 8993, no. c, pp. 4843–4853, 2014.

[8] C. W. Chen, K. H. Chen, and Y. M. Chen, “Modeling and controller design of an autonomous PV module for DMPPT PV systems,” *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4723–4732, 2014.

[9] Fraunhofer Institute for Solar Energy System, “Photovoltanic Reports,” 2017.

[10] G. Spiazzi, D. Tagliavia, and S. Spampinato, “DC-DC flyback converters in the critical conduction mode: a re-examination,” *Conf. Rec. 2000 IEEE Ind. Appl. Conf. Thirty-Fifth IAS Annu. Meet. World Conf. Ind. Appl. Electr. Energy (Cat. No.00CH37129)*, vol. 4, pp. 2426–2432, 2000.

[11] R. K. Hester, C. Thornton, S. Dhople, Z. Zhao, N. Sridhar, and D. Freeman, “High efficiency wide load range buck/boost/bridge photovoltaic microconverter,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2011, pp. 309–313.

[12] G. C. Hsieh, C. Y. Tsai, and W. L. Hsu, “Synchronous rectification LLC series-resonant converter,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2007, vol. 2, pp. 1003–1009.

[13] J. H. Kim, C. E. Kim, J. K. Kim, J. B. Lee, and G. W. Moon, “Analysis on Load-Adaptive Phase-Shift Control for High Efficiency Full-Bridge LLC Resonant Converter under Light-Load Conditions,” *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4942–4955, 2016.

[14] M. Joung, H. Kim, and J. Baek, “Dynamic analysis and optimal design of high efficiency full bridge LLC resonant converter for server power system,” in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 1292–1297.

[15] N. Azura, S. Iqbal, and S. Taib, “LLC resonant DC-DC converter for high voltage applications,” *2014 IEEE Conf. Energy Conversion, CENCON 2014*, no. 1, pp. 90–95, 2014.

[16] D. Kim, S. Moon, C. Yeon, and G. Moon, “LLC Resonant Converter with High Voltage Gain using Auxiliary Resonant Circuit,” *IEEE Trans. Power Electron.*, vol.

31, no. 10, pp. 6901–6909, 2016.

[17] X. Sun, X. Li, Y. Shen, B. Wang, and X. Guo, “Dual-Bridge LLC Resonant Converter with Fixed-Frequency PWM Control for Wide Input Applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 69–80, 2017.

[18] A. Chub, D. Vinnikov, R. Kosenko, and E. Liivik, “Wide Input Voltage Range Photovoltaic Microconverter with Reconfigurable Buck-Boost Switching Stage,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5974–5983, 2017.

[19] D. H. Lee, J. Y. Shin, S. S. Hwang, B. K. Lim, and H. W. Kim, “Analysis of the efficiency characteristics of an LLC resonant converter having a current doubler rectification circuit,” in *2015 18th International Conference on Electrical Machines and Systems, ICEMS 2015*, 2016, vol. 1, pp. 480–484.

[20] H. Gui, Z. Zhang, X. He, and Y. Liu, “A High Voltage-Gain LLC Micro-Converter with High Efficiency in Wide Input Range for PV Applications,” in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 637–642.

[21] X. Z. L. Z. R. B. J.-S. Lai, “A High-Efficiency Hybrid Resonant Microconverter for Photovoltaic Generation Systems,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3684–3695, 2017.

[22] G. Oriti, A. L. Julian, and T. D. Bailey, “PV power conditioning system with LLC resonant converter in DCM,” *2014 IEEE Energy Convers. Congr. Expo.*, no. Ccm, pp. 4262–4268, 2014.

[23] B. Gu, C. Lin, B. Chen, J. Dominic, and J. J. Lai, “Zero-Voltage-Switching PWM Resonant Full-Bridge Converter With Minimized Circulating Losses and Minimal Voltage Stresses of Bridge Rectifiers for Electric Vehicle Battery Chargers,” *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4657–4667, 2013.

[24] U. KUNDU, K. Yenduri, and P. Sensarma, “Accurate ZVS Analysis for Magnetic Design and Efficiency Improvement of Full Bridge LLC Resonant Converter,” *IEEE Trans. Power Electron.*, vol. 8993, no. c, pp. 1–1, 2016.

[25] J. Kim, J. Han, and J. Lai, “APWM adapted half-bridge LLC converter with voltage doubler rectifier for improving light load efficiency,” *Electron. Lett.*, vol. 53, no. 5, pp. 2–3, 2017.

[26] X. Zhao *et al.*, “A High-efficiency Hybrid Series Resonant DC-DC Converter with Boost Converter as Secondary for Photovoltaic Applications,” in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5462–5467.

[27] Q. Wang, X. Zhang, and R. Burgos, “Design Considerations for a High Efficiency 3 kW LLC Resonant DC / DC Transformer,” in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5454–5461.

[28] N. Shafiei, M. Ordonez, S. R. Cove, M. Craciun, and C. Botting, “Accurate Modeling and Design of LLC Resonant Converter with Planar Transformers,” in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5468–5473.

[29] R. Ren, S. Liu, J. Wang, and F. Zhang, “High frequency LLC DC-transformer based on GaN devices and the dead time optimization,” in *Proceedings - 2014 International Power Electronics and Application Conference and Exposition, IEEE PEAC 2014*, 2014, pp. 462–467.

[30] N. Wang, H. Jia, M. Tian, Z. Li, G. Xu, and X. Yang, “Impact of Transformer Stray Capacitance on the Conduction Loss in a GaN-Based LLC,” in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, 2017, pp. 1334–1338.

[31] X. Zhao, L. Zhang, Q. Ma, and J. S. Lai, “Modeling and control of a wide-input

hybrid resonant microconverter for photovoltaic applications," *2016 Asian Conf. Energy, Power Transp. Electrif. ACEPT 2016*, 2017.

[32] R.-L. Lin and L.-H. Huang, "Efficiency Improvement on LLC Resonant Converter Using Integrated LCLC Resonant Transformer," *IEEE Trans. Ind. Appl.*, vol. PP, no. 99, pp. 1–8, 2017.

[33] M. Jami, R. Beiranvand, M. Mohamadian, and M. Ghasemi, "Optimization the LLC Resonant Converter for Achieving Maximum Efficiency at a Predetermined Load Value," in *The 6th International Power Electronics Drive Systems and Technologies Conference (PEDSTC2015)*, 2015, no. February, pp. 3–4.

[34] Y. Jeong and G. Moon, "Analysis on Half-Bridge LLC Resonant Converter by Using Variable Inductance for High Efficiency and Power Density Server Power Supply," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 170–177.

[35] T. Labella and J. S. Lai, "A hybrid resonant converter utilizing a bidirectional GaN AC switch for high-efficiency PV applications," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3468–3475, 2014.

[36] X. Zhao, L. Zhang, R. Born, and J. S. Lai, "A High-Efficiency Hybrid Resonant Converter with Wide-Input Regulation for Photovoltaic Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3684–3695, 2017.

[37] X. Zhao, L. Zhang, R. Born, and J. S. Lai, "Output capacitance effect on the voltage gain in the high step-up series resonant converter," *2015 IEEE 2nd Int. Futur. Energy Electron. Conf. IFEEC 2015*, pp. 6–10, 2015.

[38] B. Cougo, H. Schneider, J. Brandelero, and T. Meynard, "Accurate switching energy estimation of parallel eGaN FETs for modern aircraft applications," *1st IEEE Work. Wide Bandgap Power Devices Appl. WiPDA 2013 - Proc.*, pp. 108–111, 2013.

[39] L. C. Murillo Carrasco and A. J. Forsyth, “Energy analysis and performance evaluation of GaN cascode switches in an inverter leg configuration,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2015–May, no. May, pp. 2424–2431, 2015.

[40] K. Wang, M. Tian, H. Li, F. Zhang, X. Yang, and L. Wang, “An improved switching loss model for a 650V enhancement-mode GaN transistor,” *2016 IEEE 2nd Annu. South. Power Electron. Conf. SPEC 2016*, p. 159DUMMY, 2016.

[41] B. Hu *et al.*, “Device loss comparison of GaN device based LLC, dual active bridge and phase shift quasi switched capacitor circuit,” *ECCE 2016 - IEEE Energy Convers. Congr. Expo. Proc.*, pp. 1–7, 2016.

[42] S. Park and J. Rivas-Davila, “Power loss of GaN transistor reverse diodes in a high frequency high voltage resonant rectifier,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 1942–1945, 2017.

[43] W. Zhang *et al.*, “Evaluation and comparison of silicon and gallium nitride power transistors in LLC resonant converter,” *2012 IEEE Energy Convers. Congr. Expo.*, pp. 1362–1366, 2012.

[44] Ferroxcube, “3C95-3C97 Data Leaflet,” 2011.

[45] New England Wire Technologies, “Litz Wire Technical Inofrmation,” 2003.