DESIGNING FET BASED MULTIPLE VALUED LOGIC CIRCUITS

by

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(ABSTRACT)

The thesis presents an analysis of FET based Multiple Valued Logic circuits. The circuit analysis program SPICE2 was used to analyze these circuits. A description of device modelling as done by SPICE2 is included in the beginning of the thesis. Techniques to implement MVL circuits using simple threshold circuits as building blocks are outlined. The two principal methods of achieving different switching voltages, namely, changing the device threshold and the device transconductance, for these threshold circuits are discussed. A comparative study of these two methods from theritical and practical viewpoint is included. Several MOSFET based MVL circuits are developed and an explanation of their operation is also given.

ACKNOWLEDGEMENTS

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CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter I

INTRODUCTION

1.1 BACKGROUND

During the past decade, semiconductor technology has made many advances. In a matter of few years, fabrication technology has advanced from small scale integration (SSI) to large scale integration (LSI). This technology is at present on the threshold of stepping into very large scale integration (VLSI). VLSI will enable a manufacturer to pack large amount of computing power on a single chip by placing close to a million devices on it.

When such high levels of integration are used to pack many circuits on a small chip area, several physical constraints exert significant influence on the circuit design. Two of these are :

1. Intra-chip wiring, and
2. Inter-chip connections.

According to a study by Dao [1] 70% of the chip area is consumed by wiring (metal and poly) as compared to 10% by active devices (transistors- FETs and BJTs) and 20% by passive isolation (oxides,dielectrics) [1]. This underlines the need for developing techniques that can reduce the chip area used for interconnect wiring.

With an increase in the number of devices on a single chip the designer will be hard pressed to find means of enabling these devices to interact with devices on other chips. An efficient mechanism must be provided for communication between chips in order to make effective use of having more devices on a single chip.

It is in the light of these technological advances and underlying constraints that the study of multiple valued logic is undertaken.

Classically, the design and implementation of digital systems has been based on the binary number system. The transistor gave further impetus to the use of binary system because it could be conveniently switched on and off to realize binary states. Consequently, the art of circuit and system design using binary logic developed so rapidly that the idea of developing non-binary system was practically non-existant. Semiconductor technology constraints made it more difficult for the non-binary systen to make a headway. This is because to realize a non-binary system it was important that the manufacturers have an advanced fabrication facility that can achieve close tolerances (eg ion-implantation techniques).

In addition to these factors that inhibited the growth of non-binary system, reduced noise immunity was another draw-

back of non-binary systems. The existing levels of operation were further broken down to accomodate the operation of systems having more than two stable states. This lowered the margins for interference due to noise.

1.2 DEVELOPMENTS IN MULTIPLE VALUED LOGIC.

Recently, the research in the field of non-binary logic has increased. People have been exploring possibilities of expanding from a binary logic system to a one having more than two states and what will henceforth be called Multiple Valued Logic (MVL). Several researchers laid the foundations for MVL by developing mathematical tools to analyze MVL designs. These are outlined by Givone and Allen in [2] and by Vranesic, Lee and Smith in [3]. Further research work yielded even more efficient algorithms and techniques to design and optimize MVL circuits [4], [5] and [6]. Supported by the mathematical base, researchers began the exploring circuits that can function as MVL gates and memories. In a short period of time many ideas surfaced that lent credibility to MVL. MVL circuits were designed and tested for various devices. Dao, Pugsley and Silio, and Singh and Armstrong designed bipolar circuits [7], [8], [9]. Russell, Dao, and Tront and Givone gave MOSFET/MESFET circuits [10], [11], [12] and the CCD based circuits were de-

veloped by Kerkhoff and Tervoert. This research work aims at developing more FET based circuits that can function as MVL gates and memories.

1.3 ADVANTAGES OF MVL.

MVL presented the researchers with very important advantages which are described by Vranesic in [14]. MVL systems hold promise of reducing the system wiring complexity. Since more information can be transferred over an MVL path, fewer wires will be needed, requiring fewer pins on the IC package. This can be seen by considering the following : the area of an LSI chip increases in proportion to the chip perimeter. Since information transferred to the chip by connecting pins increases linearly with the chip perimeter, it can concluded that the perimeter, and therefore the number of pins, becomes a limiting factor in the information processed rather than the chip area itself. Thus, it can be seen that a mechanism for increasing the information transferred per pin, even at possible cost of moderate increase in circuit complexity, has potential of increasing the information processing capability per unit area. Consequently, there would be immediate application of such a device to volume and weight constrained systems. In this way MVL can help in reducing the intra-chip wiring and would also provide more cost effective communication between IC's.

The other aspect of computer architechture in which MVL can be of value is in increasing the efficiency of storage of digital information. It is perceived that MVL will reduce the cost per information stored for read/write memories and will also significantly reduce the cost of ROM's.

1.4 DESCRIPTION OF CHAPTERS IN THE THESIS.

This thesis deals with investigating the suitability of field effect devices (MOSFETs and MESFETs) in implementing MVL.

The circuit analysis program SPICE2 was used extensively during the research. It is therefore essential that the element models that SPICE2 uses be understood very clearly before proceeding any further. Chapter II is a description of the element models used to characterize the MVL devices. It gives details about how SPICE2 models MOSFET and also outlines the changes that are incorporated to obtain a MESFET model.

Chapter III includes details on the threshold circuits that were used as building blocks to configure MVL circuits. Description of both MOSFET and MESFET threshold circuit is included in this chapter.

Chapter IV shows how the threshold circuits can be manipulated to implement MVL circuits. It gives details about

variations in parameters that are made to achieve MVL characteristics.

Chapter V gives a discussion of several MVL circuits. Starting from the threshold circuit, implementation of memories, literal gates, logic gates etc., is discussed in the chapter.

The final chapter, chapter VI, is devoted to conclusions and future directions for possible research. It outlines the advantages of configured MVL circuits to the equivalent binary ones. It lays directions in which future research can continue and introduces several ideas that can help in implementing more MVL circuits like EPROM's.

Chapter II

DESCRIPTION OF SPICE2 MODELS

Electronic circuit design requires an accurate method of assesing circuit performance. Simple circuits can be tested on 'breadboards', but the design of integrated circuits poses an entirely different problem. For such highly complex circuits, it will be very advantageous to use computer programs for analysis. SPICE2 is one of the several successful circuit simulation program that are currently available [17]. It has grown immensely in popularity and is applicable to a large variety of circuit simulation problems.

For carrying out the simulation of circuits having active devices, SPICE2 uses different models to characterize the behaviour of these devices. The aim of this chapter is to present the details of these models for MOSFETs[15]. Slight changes were made to the JFET model of SPICE2 so as to model a GaAs MESFET. These have been outlined towards the end of the chapter. The version of SPICE used for this research was SPICE2E.2.

2.1 ANALYTICAL VS. EMPIRICAL MODELS.

SPICE2 has two models to characterize a MOSFET device :

1. The Analytical Model
2. The Empirical Model

These two models can be used seperately or in various combinations. The analytical model relies heavily on processing parameters to predict the electrical characteristics of the device. The designer specifies values for doping concentration, surface state density, etc. and the program calculates values for threshold voltage, drain current, etc. The accuracy of the model depends on the appropriateness of the mathematical formulation and the accuracy of the input data.

The empirical model simulates the electrical characteristics of the MOS transistors by using parameters based on measured operational characteristics. The accuracy of the model is based on the ability of the designer to match the electrical characteristics of the component in question with the model parameters available.

One or a combination of both models is used depending on the parameters specified by the user. In some cases, if certain physical parameters are specified, the analytical model will be used over-riding the empirical values specified by user. In other cases, some empirical model parameters will

over-ride analytical values if both are specified. Finally, in absence of parameters the model resorts to default values. The default values have been chosen to produce a computable model. They are not necessarily representative of a particilar device. A complete list of these parameters and it's details are given in [15] and a few of them have been included in the appendix for illustration purpose.

2.2 MOSFET EQUIVALENT CIRCUIT.

Fig. 1 gives an equivalent circuit of a MOSFET that is used by SPICE2 for analysis. This model is applicable for any insulated-gate FET (IGFET). Polarities shown are for an n-channel device. For a p-channel device, the polarities of the five terminal voltages (VGS, VGD, VDS, VBS, and VBD), the two substrate junctions, and the non-linear current sources Id are reversed. The substrate node is labelled B (for bulk) to avoid confusion with source node. The ohmic resistances of the drain and source regions of the device are modeled by two linear resistances rd and rs.

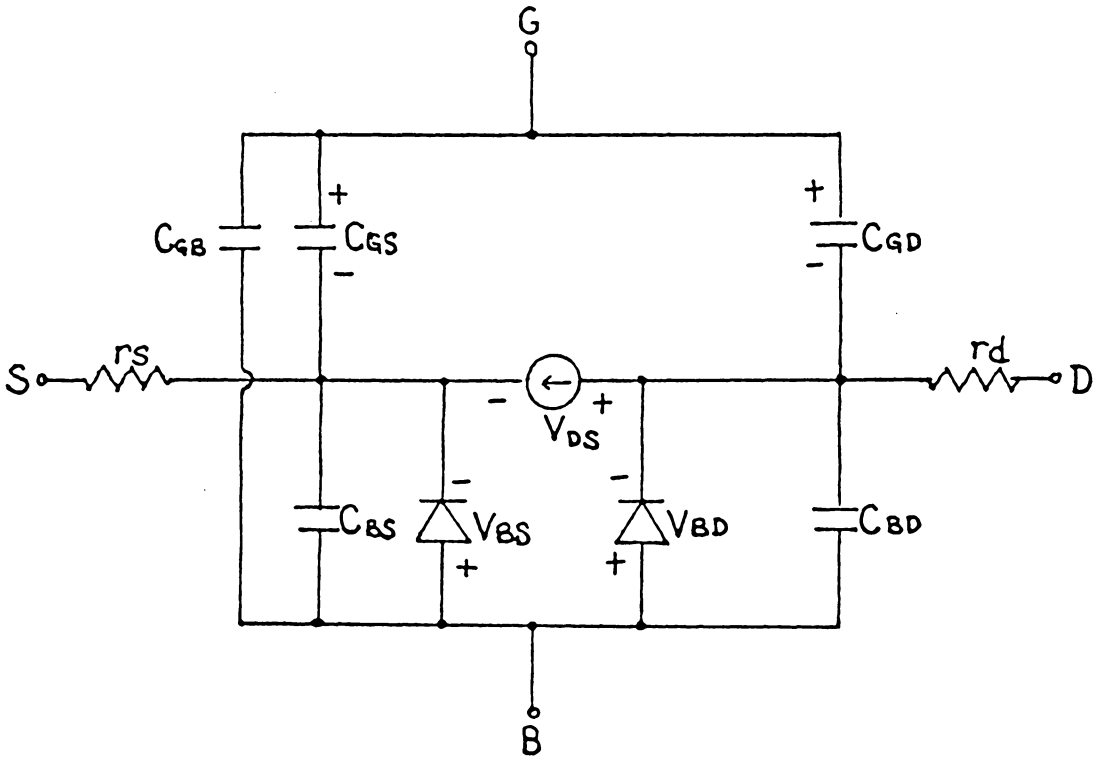

Figure 1: MOSFET Equivalent Circuit.

2.3 MODEL PARAMETER DEFINITIONS.

The following section gives an outline of several very significant parameters of a MOSFET. As mentioned previously some parameters are solely used with analytical model while others are used with the empirical models.

2.3.1 VTO - Threshold Voltage.

When VTO is specified, then SPICE2 uses the empirical model. However if the doping concentration of the substrate, NSUB, is specified, the analytical model overrides the empirical model and then SPICE2 uses the analytical model.

VTO is calculated from the relation :

$$V_{TO} = V_{FB} + 2\phi_F + \frac{2\sqrt{q\varepsilon_{si}N_{SUB}\phi_F}}{C_{ox}} \qquad 2.3.1.$$

where

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_{ox}}$$

$$\phi_{ms} = \phi_m - \phi_{so} - \frac{E_g}{2q} - \phi_F$$

= Metal Semiconductor Work-Function.

ϕ_m = Metal Gate Work Function (3.2V).

ϕ_{so} = Si-SiO_2 Work Function (3.25V).

E_g = Silicon Band Gap.

$$\phi_F = \frac{kT}{q} \ln\left[\frac{N_{sub}}{n_i}\right]$$

N_{SUB} = Substrate Doping Concentration.

n_i = Intrinsic Doping Concentration.

$Q_{ss} = N_{ss} * q$ = Oxide Charge.

$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}$ = Oxide Capacitance/Area.

There are several parameters which directly influence the VTO, and significant among these are NSUB, NSS, and TOX. While carrying out a parameter variation study in a later chapter, the changes that these parameters bring about in the threshold voltage will be examined.

2.3.2 Kp - Intrinsic Transconductance.

The intrinsic transconductance is calculated using the relation

$$K_p = \mu_o C_{ox} = \mu_o \frac{\varepsilon_{ox}}{T_{ox}}$$

where

μ_o = Carrier Mobility.

ε_{ox} = Permittivity of Oxide.

T_{ox} = Thickness of Oxide.

A specified value overrides any calculation or default value in either model. To use the analytical model the user should specify the mobility u and Tox, the oxide thickness, and leave Kp out of parameter list. To arrive at the k-factor of a MOSFET the Kp is used as follow :

$$k = k_p . \frac{W}{L}$$

where W and L, the length and width of the gate, are specified by the user.

2.3.3 Gamma - Bulk Threshold Parameter.

According to Ihantola's equation for drain current [16] the coefficient term accounting for substrate bias effect is gamma. Analytically gamma can be written as :

$$\text{Gamma} = \frac{2}{3} \frac{\sqrt{2\varepsilon_{si} q N_{SUB}}}{C_{ox}}$$

where

ε_{si} = Permittivity of Silicon.
q = Electronic Charge.
N_{SUB} = Substrate Doping Concentration.
C_{ox} = $\frac{\varepsilon_{ox}}{T_{ox}}$ is Oxide Capacitance per Area

If gamma is maintained small (<1) it is easier to follow the changes in Id with respect to VDS. If gamma is allowed to be large (>20) the influence it exerts on the drain current is not easily predictable.

Gamma is not directly specified by the user. While using the analytical model, SPICE2 calculates it from the parameters specified.

2.3.4 RD and RS - Drain and Source Ohmic Resistances.

The value for these resistances can be specified for either model but when none is specified both are defaulted to zero for both models.

2.3.5 CGS and CGD - Source and Drain Overlap Capcitances.

The gate-source and gate-drain capacitances, CGS and CGD, can be specified for both empirical and analytical model. When specified, these capacitances should be specified as farad per cm of channel width since SPICE2 multiplies that quantity by width of channel to determine total capacitance.

2.3.6 TOX - Oxide Thickness.

The gate oxide thickness, TOX, may be specified for either the empirical or the analytical model. When no value is specified SPICE2 uses default values for the models of 1000 A for the analytical model, and infinity for empirical model. The value of infinity is set by defaulting COX to zero. In the latter case, substrate bias effects, weak inversion effects, and varible mobility effects are eliminated.

2.3.7 XJ - Metallurgical Junction Depth.

This may be specified for either of the models and the default value is zero. The value of XJ is used to calculate the effective channel length. The effective channel length is used in all calculations requiring the width-to-length ratio. This ratio directly affects the transconductance parameter and therefore the switching characteristics of a circuit.

2.3.8 NSUB - Effective Substrate Doping Concentration.

The substrate doping concentration should be specified only when an analytical model is desired. In case NSUB is specified the analytical model will override the empirical model. The value of the threshold voltage is calculated using the equation given in 2.3.1.

2.3.9

NSS - Effective Surface State Density.

The effective surface state density, NSS, should be specified if the analytical model is to be used. In the analytical model the threshold voltage is calculated using the equation given in 2.3.1.

2.4 DRAIN CURRENT CALCULATIONS.

Once SPICE2 has all the information needed it goes ahead and calculates the drain current for the MOSFET using the following relations:

$$i_D = \begin{cases} 0 & v_{GS}-V_T < 0 \\ k(v_{GS}-V_T)^2 & 0 < v_{GS}-V_T < v_{DS} \\ kv_{DS}[2(v_{GS}-V_T)-v_{DS}] & 0 < v_{DS} < v_{GS}-v_T \end{cases}$$

where $K = Kp(W/L)$

VT is given in 2.3.1.

2.5 IMPLEMENTATION OF A MESFET MODEL ON SPICE2.

2.5.1 Introduction to a MESFET.

A MESFET can be thought of as a modified version of a JFET. The depletion of the channel in a JFET can be accomplished by the use of a reverse-biased schottky barrier instead of a p-n junction. The resulting device is called a MESFET, indicating that a metal-semiconductor junction is used. This device is useful in high speed digital or microwave circuit, where simplicity of Schottky barriers allows fabrication to close geometrical tolerences. For this reason this thesis investigates the suitability of a MESFET for implementing MVL circuits.

MESFETs have been designed with Silicon as well as with Gallium Arsenide. GaAs devices are of particular interest because of their high speed of operation [18]. In addition GaAs MESFETs exhibit high saturation current, low ON resistances, and low parasitic capacitance in monolithic IC's.

2.5.2 MESFET Modelling.

A number of MESFET models can be found in the literature [19], [20], [21]. The model proposed by Curtice is of particular interest because it can be used in the design of integrated circuits and is in a simplified form so that it can be easily incorporated in SPICE2.

The JFET model available in SPICE2 forms the basis of MESFET model given by Curtice [21]. However, JFET model has several deficiencies when used to model MESFETs. The model is in error with regard to drain-current voltage relationships below current saturation. Furthermore, electron transit time effects under the gate are omitted in the JFET device.

Figure 2 shows a simple MESFET equivalent circuit that can be used with a circuit analysis program. In this figure the non-linear elements of the circuit are:

$$i_D = I_D(v_{GS}, v_{DS}, t)$$

$$C_{GS} = C_{GS}(v_{GS})$$

The drain-current expressions for the JFET model used in SPICE2 are as follows:

$$i_D = \begin{cases} 0 & v_{GS}-V_T < 0 \\ \beta(v_{GS}-V_T)^2 & 0 < v_{GS}-V_T < v_{DS} \\ \beta v_{DS}[2(v_{GS}-V_T)-v_{DS}] & 0 < v_{DS} < v_{GS}-V_T \end{cases}$$

To get accurate drain current relationships for a MESFET, Curtice suggests that a hyperbolic tangent function be in-

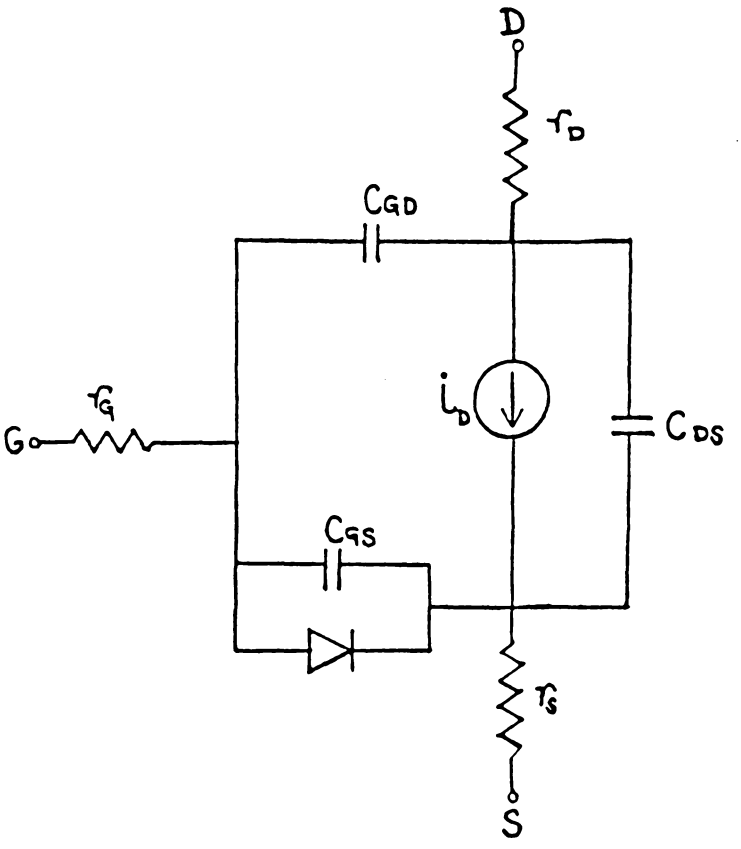

Figure 2: A MESFET Equivalent Circuit.

corporated into the equations of the JFET. Consequently, the drain current equations for a MESFET are given as follows:

$$i_D = \begin{cases} 0 & v_{GS}-V_T < 0 \\ \beta(v_{GS}-V_T)^2 & 0 < v_{GS}-v_T < v_{DS} \\ \beta(V_{GS}-V_T)^2 \tanh(\alpha V_{DS}) & 0 < v_{DS} < v_{GS}-V_T \end{cases}$$

These equations were experimentally verified by matching a set of data developed in [21]. This is the most significant change that needs to be made in order to perform a DC analysis of MESEFT circuits using SPICE2.

Other changes in the JFET model that need to be made in order to perform AC and transient analysis are:

1. Inclusion of transit time effects.
2. Accurate evaluation of gate capacitances.
3. Evaluation of 'Non-Electronic' drain-gate and source-gate capacitances.
4. Evaluation of circuit parameters.

These are explained extremely well in [19].

The changes for the drain current relations in the non-saturation were incorporated in the SPICE2 model by modifying the FET subroutine. Instead of the equation for an FET

the one for a MESFET was substituted and the program was run for a sample MESFET circuit.

Chapter III

SWITCHING CHARACTERISTICS OF THRESHOLD CIRCUITS.

3.1 DESCRIPTION OF THE THRESHOLD CIRCUIT.

The threshold circuits described here form the basic building blocks from which the more complex MVL circuits can be configured. For both, MOSFET and MESFET based circuits, the threshold circuit is the standard two transistor inverter. The transfer characteristics of these inverter circuits are described here in detail. Based on the dc characteristics of this circuit a scheme for implementing MVL circuits will be developed.

3.1.1 MOSFET Threshold Circuit.

Shown in Fig. 3 is MOSFET inverter which is the threshold circuit for MOSFET based MVL circuits.

Transistor TL is an n-channel depletion-mode load while TS is an n-channel enhancement mode switching transistor. Operating TL in the depletion mode eliminates the need for a second power supply. Moreover, when TL is in saturation it supplies constant current facilitating faster switching. VTS and VTL are the threshold voltages of the respective transistors while KS and KL are the transconductance parame-

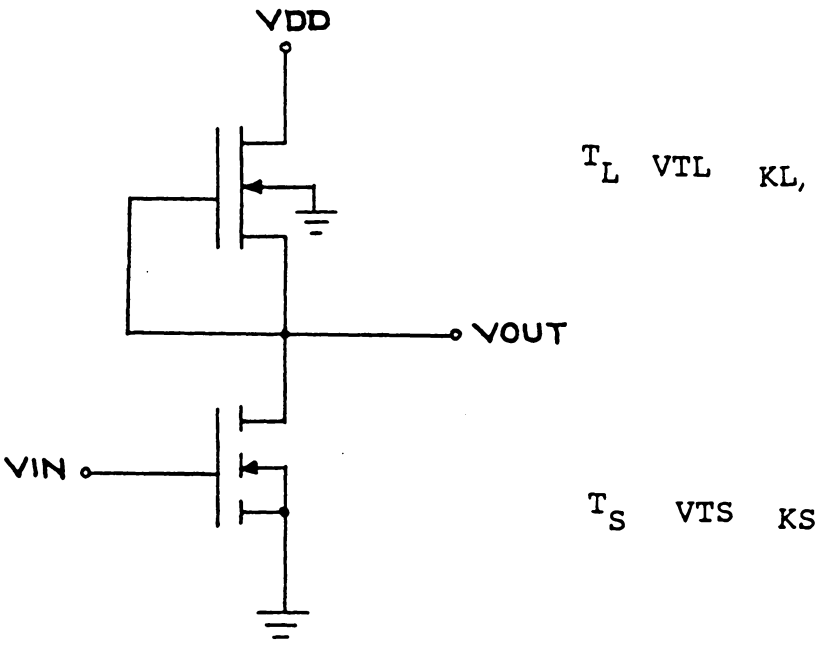

Figure 3: A MOSFET Threshold Circuit.

ters for each. The equations relating VIN and VOUT for the threshold circuits are developed below.

For a MOSFET the drain current, i_D, as a function of gate-source and drain-source voltages is given by the following equations :

For transistor T_S :

$$v_{GS} = v_{IN}$$

$$v_{DS} = v_{OUT}$$

Cutoff :

$$i_{DS} = 0 \quad \text{for} \quad v_{GS}-V_T < 0$$

$$\text{or} \quad v_{GS} < V_T$$

Non-saturation :

$$i_{DS} = K_S v_{DS}(2(v_{GS}-V_{TS})-v_{DS})$$

$$= K_S v_{OUT}(2(v_{IN}-v_{OUT})-v_{OUT}) \qquad 4$$

Transistor T_S is in non-saturation for

$$v_{DS} < v_{GS}-V_{TS}$$

$$v_{OUT} < v_{IN}-V_{TS}$$

Saturation :

$$i_{DS} = K_S(v_{GS}-V_{TS})^2$$

$$= K_S(v_{IN}-V_{TS})^2 \qquad 3$$

Transistor T_S is in saturation for

$$v_{DS} > v_{GS}-V_{TS}$$

$$v_{OUT} > v_{IN}-V_{TS}$$

For transistor T_L :

$$v_{GS} = 0$$

$$v_{DS} = V_{DD}-v_{OUT}$$

Non-saturation :

$$i_{DL} = K_L v_{DS}(2(v_{GS}-V_{TL})-v_{DS})$$

$$= K_L(V_{DD}-v_{OUT})(2(-V_{TL})-V_{DD}+v_{OUT})$$

$$= K_L(V_{DD}-v_{OUT})(v_{OUT}-V_{DD}-2V_{TL}) \quad 1$$

Transistor T_L is in non-saturation for

$$v_{DS} < v_{GS} -V_{TL}$$

$$\text{or} \quad V_{DD}-v_{OUT} < -V_{TL}$$

$$\text{or} \quad v_{OUT} < V_{DD} +V_{TL}$$

Saturation :

$$i_{DL} = K_L(v_{GS}-V_{TL})^2$$

$$= K_L V_{TL}^2 \quad 2$$

Transistor T_L is in saturation for

$$v_{DS} > v_{GS} - V_{TL}$$

$$v_{DD} - v_{OUT} > -V_{TL}$$

$$v_{OUT} > V_{DD} + V_{TL}$$

Equation (1) through (4) can be used to explain the different regions of the transfer characteristics shown in Fig. 4.

In the region AB, TL is in non-saturation and TS is in saturation giving:

$$(i_{DL})\text{non-sat.} = (i_{DS})\text{sat.}$$

Using (1) and (3), we get

$$K_L(v_{DD}-v_{OUT})(v_{OUT}-v_{DD}-2V_{TL}) = K_S(v_{IN}-v_{TS})^2$$

which can be written as

$$v_{OUT}^2 - 2v_{OUT}(v_{DD}+V_{TL}) - (v_{DD}(v_{DD}+2V_{TL}) + K_S/K_L(v_{IN}-V_{TS})^2$$

Solving this gives, VOUT in terms of VIN

$$v_{OUT} = (-b + \sqrt{b^2-4ac})/2$$

where

$$b = -2(V_{DD}-V_{TL})$$

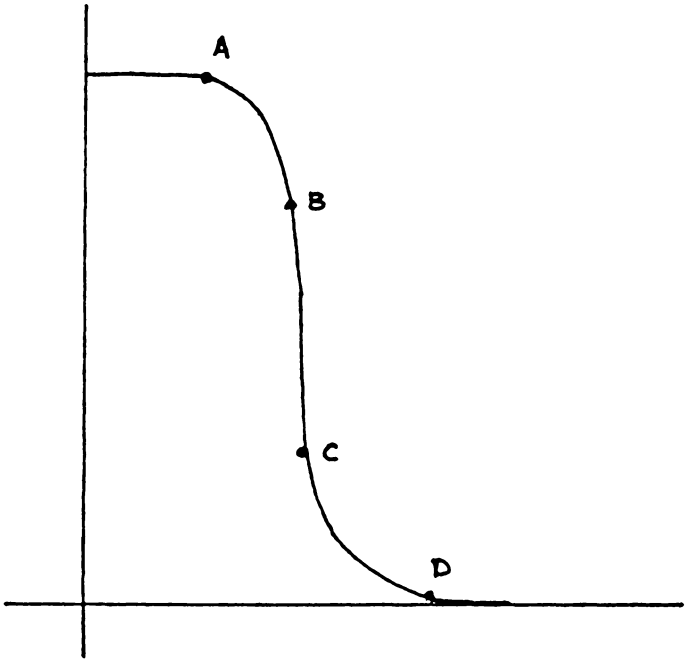

Figure 4: Transfer Characteristics Of An Inverter.

$$c = (V_{DD}(V_{DD}+2V_{TL})+K_S/K_L(v_{IN}-V_{TS})^2$$

In the region BC, TL is in saturation and TS is in saturation giving:

$$(i_{DL})\text{sat.} = (i_{DS})\text{sat.}$$

Using (2) and ( ), we get

$$K_L V_{TL}^2 = K_S(v_{IN}-V_{TS})^2$$

Solving for VIN:

$$v_{IN} = -\sqrt{(K_L\ K_S)}.V_{TL}+V_{TS} = v_{SW}$$

We define this value of the input voltage, VIN, as the switching voltage (VSW) for this circuit configuration. Voltage VSW is taken to be the input voltage at which the output voltage changes from "high" level to "low" level.

In the region CD, TL is in saturation and TS is in non-saturation giving:

$$(i_{DL})\text{sat.} = (i_{DS})\text{non-sat.}$$

Using (1) and (4), we get

$$K_L V_{TL}^2 = K_S v_{OUT}(2(v_{IN}-V_{TS})-v_{OUT})$$

which can be written as

$$v_{OUT}^2 - 2v_{OUT}(v_{IN}-V_{TS}) + K_L\ K_S V_{TL}^2 = 0$$

Solving for VOUT in terms of VIN gives

$$v_{OUT} = (-b+\sqrt{b^2-4c})/2$$

where

$$b = -2(v_{IN}-V_{TS})$$

$$c = (K_L/K_S)V_{TL}^2$$

With these equations and given KL, KS, VTL, VTS, it is possible to generate curves for the transfer characteristics of a particular inverter circuit. The changes that can be made in several physical parameters of the devices in order to vary the transfer characteristics are discussed in the next chapter. This change of the physical parameters from one transistor type to another forms the basis of the methods employed to get MVL behaviour in FET circuits.

3.1.2 MESFET Threshold Circuit.

Shown in Fig. 5 is the MESFET inverter which is the basic building block for MESFET based MVL circuits. A MESFET threshold circuit analysis can be carried along lines similar to that of MOSFETS. However, in non-saturation region the MESFET behaviour is different than that of the MOSFET. The drain current there is given by [19] and is reproduced here.

$$i_D(v_{GS}, v_{DS}) = \beta(v_{GS}+V_T)^2(1+\lambda v_{DS})\tanh(\alpha v_{DS})$$

where β is the transconductance parameter.
α is a constant depending on the device.
λ is channel length modulation parameter.

Therefore, the complete set of simplified equations for a MESFET is as follows:

$$i_D = \begin{cases} 0 & v_{GS}-V_T < 0 \\ \beta(v_{GS}-V_T)^2 & 0 < v_{GS}-v_T < v_{DS} \\ \beta(V_{GS}-V_T)^2\tanh(\alpha V_{DS}) & 0 < v_{DS} < v_{GS}-v_T \end{cases}$$

An analysis, similar to that for the MOSFETS, yields the following relations for the threshold circuit of Fig. 5.

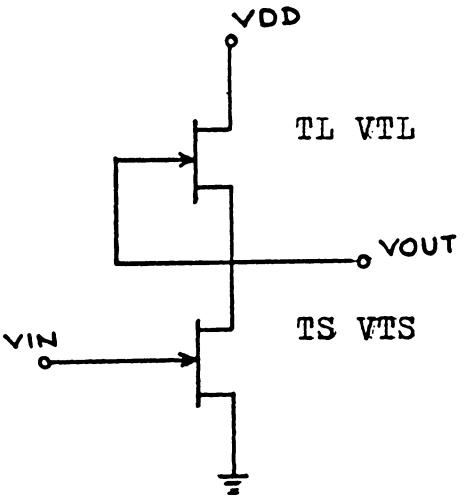

Figure 5: A MESFET Threshold Circuit.

Refering to the Fig. 4 the regions of operation for the transfer characteristics obey these equations.

Region AB

$$v_{OUT} = V_{DD} - \frac{1}{\alpha}.\tanh^{-1}\left|\frac{\beta_S(v_{IN}-V_{TS})^2}{\beta_L V_{TL}^2}\right|$$

Region BC

$$v_{IN} = -\sqrt{\frac{\beta_L}{\beta_S}}V_{TL} + V_{TS} = v_{SW} \text{ (Switching Voltage)}$$

Region CD

$$v_{OUT} = \frac{1}{\alpha}.\tanh^{-1}\left|\frac{\beta_L V_{TL}^2}{\beta_S(v_{IN}-V_{TS})^2}\right|$$

Using the equations for the MOSFETs and the MESFETs typical dc switching characteristics were plotted for the test circuits of Fig.3 and Fig. 5 and they are shown in Fig. 6. As can be seen the MESFET circuit displays excellent transfer characteristics, and as in the case of MOSFET inverter the switching voltages for these characteristics can be manipulated by changing several physical parameters of the switching devices. Two of these parameters that can be changed to get different switching voltages are the threshold voltage and the transconductance. These techniques are investigated in the next chapter.

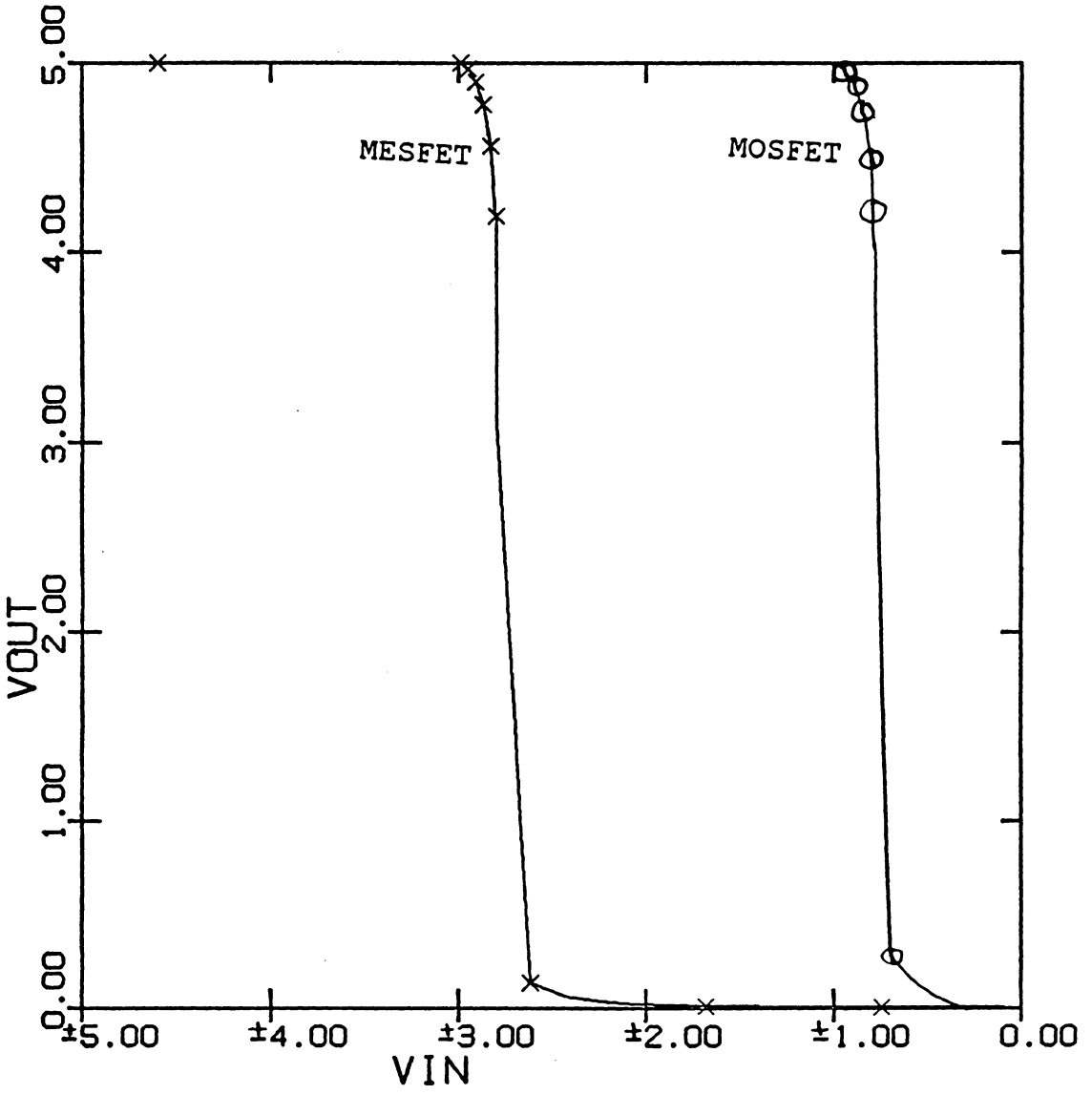

Figure 6: Switching Characteristics For The Test Circuits.

As conclusion to this chapter, a dicussion on the logic bandwidths, for an MVL is presented. This gives an introduction to the next chapter that concerns parameter variation study to achieve MVL behaviour.

The underlying idea of an MVL circuit (eg. a literal gate) is illustrated by the schematic of Fig. 7. A typical MVL circuit is configured from a number of subcircuits. The threshold circuit discussed in the previous section is one type of a subcircuit. In order to realize an MVL behaviour it would be necessary that the subcircuits recognize a particular value of input voltage and then place a corresponding voltage on the output line. Therefore, the subcircuit Sa, in Fig. 7 recognizes the input voltage, VINA, and an output voltage, VOA, is realized. Similarly, subcircuit, Sb, recognizes VINB and the corresponding output voltage is VOB. An identical explanation can be given for VOC and VOD.

The threshold circuits discussed in the previous sections can be made to recognize a particular input voltage by setting its switching to this input voltage. In this way, when the input voltage crosses the fixed switching voltage the inverter changes states. This would either place a 'high' voltage or a 'low' voltage on the output as the case may be. Instead of designating a single input voltage as a particu-

lar logic level, it is necessary that a band of voltages around the switching voltage be recognized as the same logic level. This is essential to provide noise margins for the overall MVL circuit. A definition for the logic voltage bandwidth in an MVL circuit can be give as follows:

DEFINITION : Logic voltage bandwidth of an MVL circuit is the width of voltage values around a particular logic level that are associated with the same logic level.

EXAMPLE : A four-valued MVL circuit has sub-circuits that have switching voltages of 0.5V, 1.5V, and 2.5V. This definition of logic bandwidths is illustrated in Fig. 8. A small band around the switching voltage is left as dead-band and a voltage in this band is not desirable. This is to accomodate changes in the switching voltages of the sub-circuits resulting from inaccurate manufacturing. This also provides a margin for output corrupted by noise. Shown in Fig. 8 is a schematic that illustrates these bands. Input voltages below 0.2V are realized as logic 0. Therefore, the nominal logic 0 voltage can be corrupted to 0.2 by noise and still be recognized as logic 0. Similarly, logic 1 can lie between 0.8V and 1.2V and is recognized as logic 1. If the voltage falls within the dead band, that is more than 0.2V is added by noise, then the threshold device may not recognize the

level correctly. As shown in Fig. 8 this dead band is 0.6V wide.

These bandwidths should be taken into consideration every time a decision is to be made regarding the switching voltages of the subcircuits.

A very small bandwidth is undesirable because it decreases the noise margin of the overall circuit. A large bandwidth, though desirable from the noise margin point of view, is not possible to realize because of the physical constraints of the devices like threshold voltages, area of the chip, doping concentrations etc. The subcircuits therefore have to be fabricated such that a desirable bandwidth is achieved when the overall MVL circuit is configured.

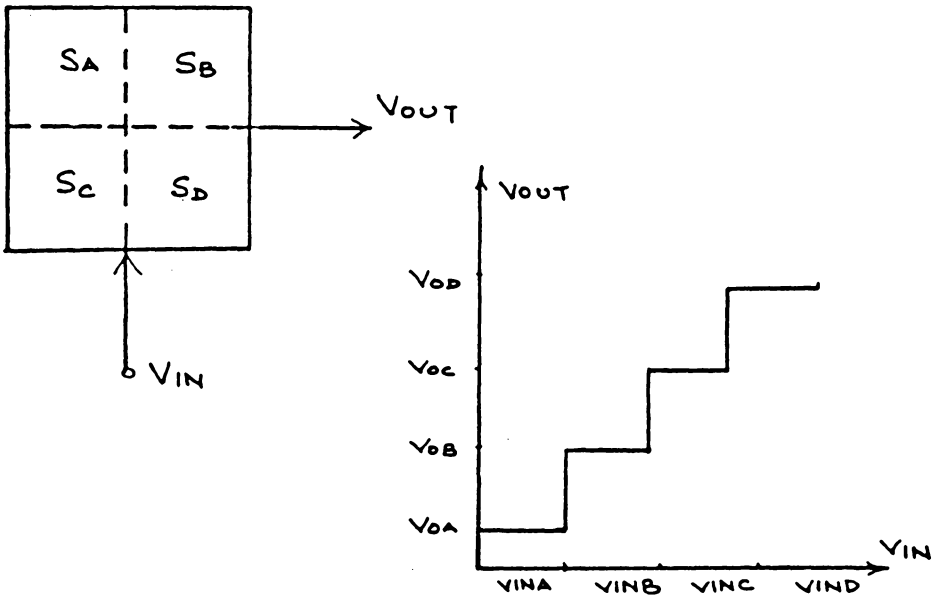

Figure 7: Characteristics of an MVL circuit.

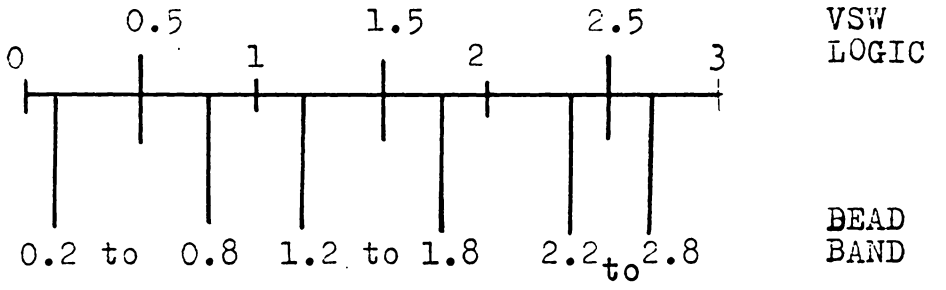

Figure 8: Illustrations of bandwidths, dead-band, and VSW.

Chapter IV

ADJUSTING THRESHOLD TO PRODUCE MVL BEHAVIOUR.

This chapter outlines the different ways in which the threshold of an individual sub-circuit can be changed. This change in the switching characteristics of the sub-circuits is necessary to implement MVL circuits. There are two important device parameters that directly affect the switching voltage of an inverter. These are: 1) The threshold voltage of the device, VT, and 2) K - factor of the MOSFET (beta for a MESFET). These two parameters can be changed by manipulating several physical parameters of the device to produce the desired switching voltage. A complete discussion of the ways in which physical parameters like substrate doping concentration, gate dimensions, etc. change the switching voltage is included in this chapter.

4.1 SETTING THE SWITCHING THRESHOLD FOR A MOSFET SUBCIRCUIT.

The switching voltage of an inverter can be changed very easily by changing the threshold voltage of the devices. It is, therefore, necessary to determine ways of changing the threshold voltage of a MOSFET. This threshold voltage was described in Chapter 2 and the equation is reproduced here.

$$V_{TO} = V_{FB} + 2\phi_F + \frac{2\sqrt{q\varepsilon_{si}N_{SUB}\phi_F}}{C_{ox}}$$

Equation 4.1 indicates that the physical parameters which can be manipulated in order to change VTO are:

1. NSS : Effective Surface State Density.
2. TOX : Oxide Thickness.
3. NSUB : Substrate Doping Concentration.

Figures 9 and 10 illustrate the dependence of the threshold voltage on two of these parameters namely, NSS and TOX. The switching voltage for a MOSFET inverter was derived in section 3.1.1. as:

$$V_{SW} = - (KL/KS).V_{TL} + V_{TS}$$

In order that the switching voltage be dependent on the threshold voltage alone, the ratio of the K-factors is made very small. Therefore, if KL << KS, then

$$(KL/KS).V_{TL} << V_{TS}$$

$$V_{SW} \simeq V_{TS}$$

In this way, VSW can be directly controlled by setting VTS to the required values. Figures 11 and 12 illustrate a set of different switching curves obtained by varying NSS

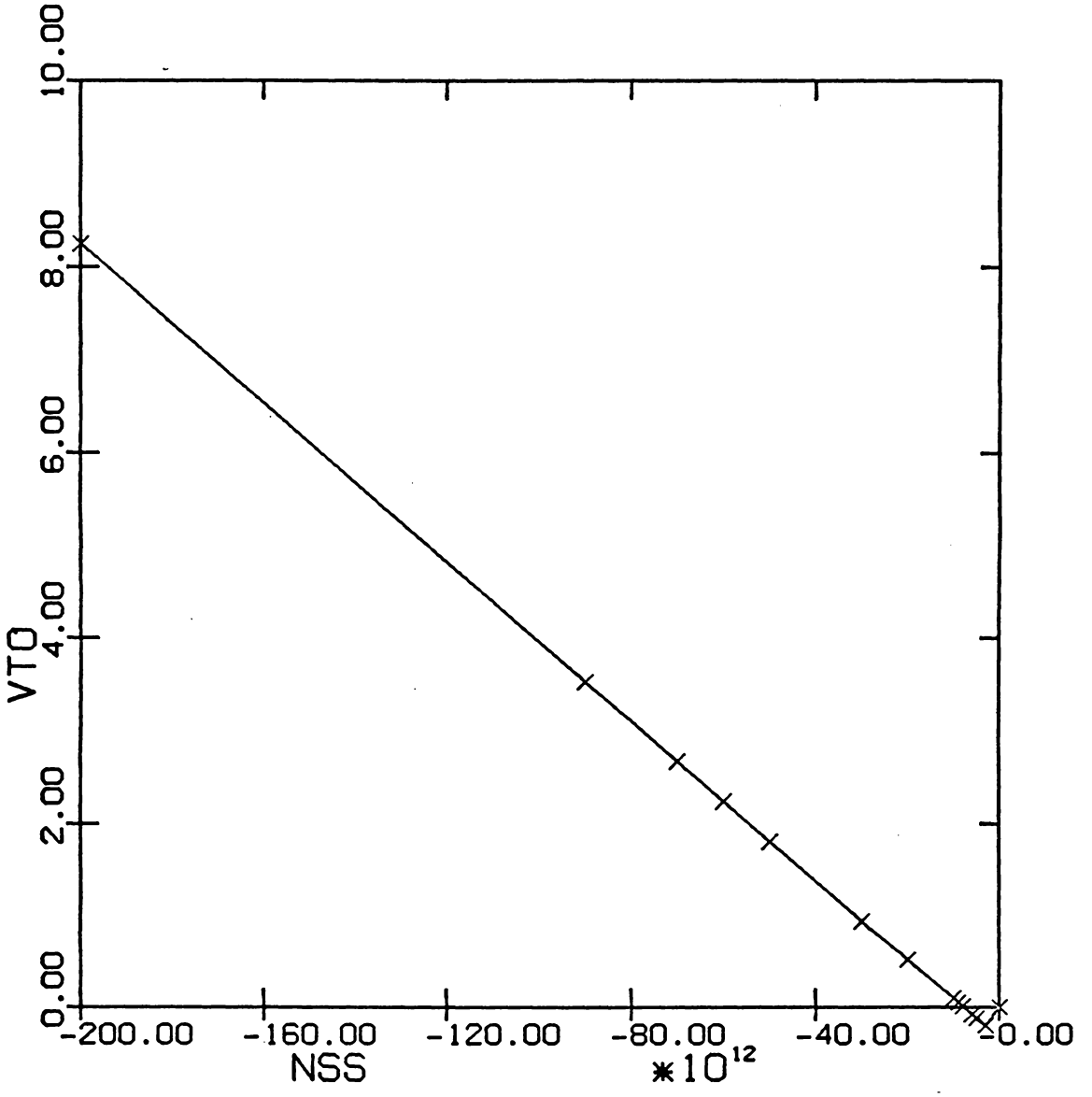

Figure 9: Threshold Voltage vs. NSS. TOX = 95E-9m, NSUB = 8 14/m

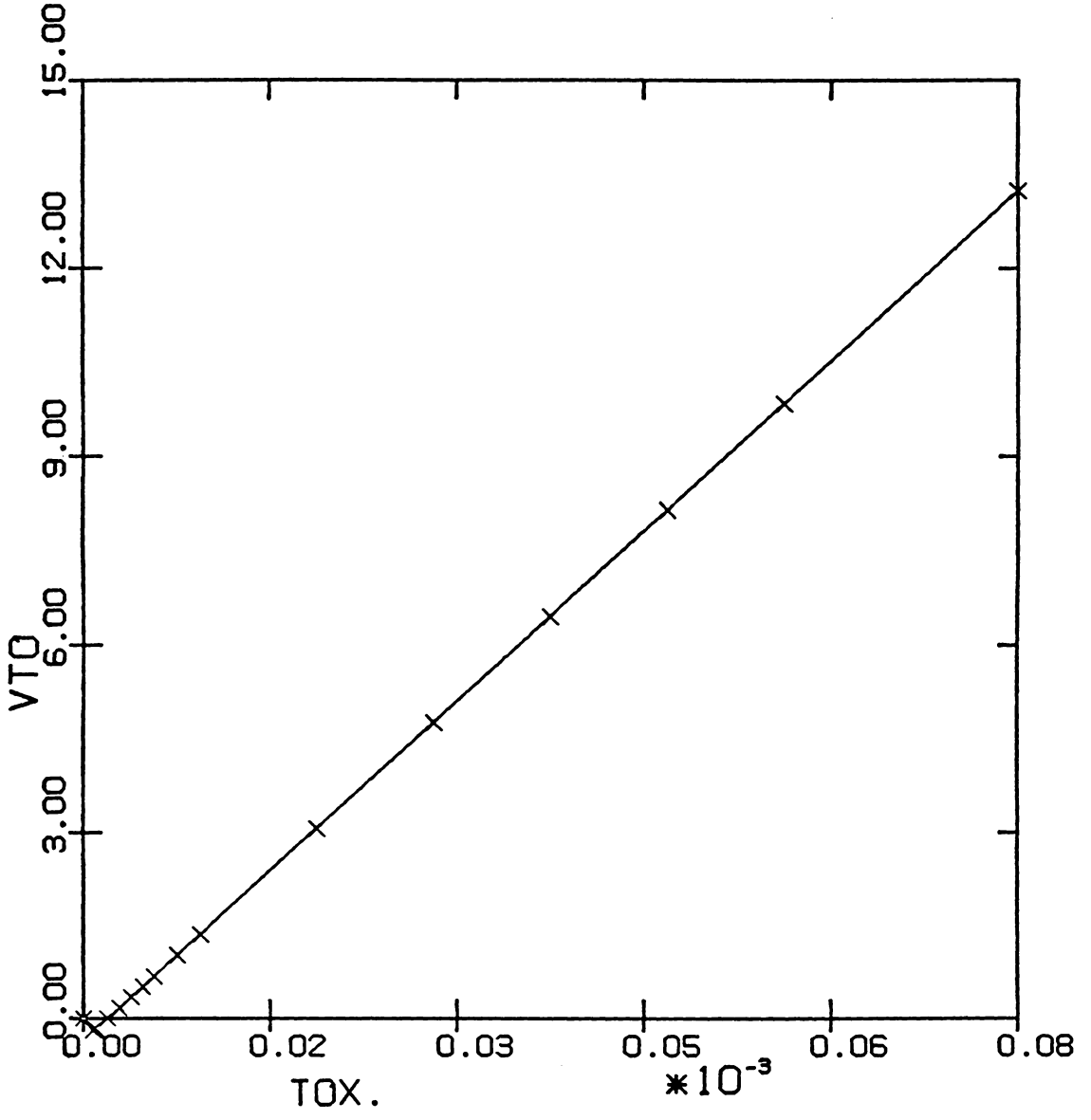

Figure 10: Threshold Voltage vs. TOX. NSS =-5 11/m , NSUB =8E14/m

and TOX. These curves were obtained using SPICE2 to analyse the MOSFET inverter. The parameters were specified and SPICE2 calculated the VTO for each case using its internal analytical model. It is seen from these curves that this technique of obtaining different switching voltages is very effective.

Unfortunately, setting VSW by the control of NSS, TOX and NSUB presents a difficult problem since the threshold voltage is a complex function of these parameters. In addition, the individual physical parameters must be controlled to absolute tolerances which can present arduous problem. It is generally found that, it is easier to hold the ratio of parameters to within a certain tolerance than to bring a single parameter to within a given tolerance.

Examining Eq. 4.2, it can be seen that it is possible to control VSW by fixing the value of threshold voltages and adjusting the ratio of the transconductance factor K. In this way tolerence errors in the adjusted parameters (K's) will cancel out.

$$K = \frac{\mu_o \varepsilon_{ox}}{T_{ox}} \cdot \frac{W}{L}$$

Thus, K can be changed by varying the dimensions of the gate and by varying the oxide thickness. The dimensions are

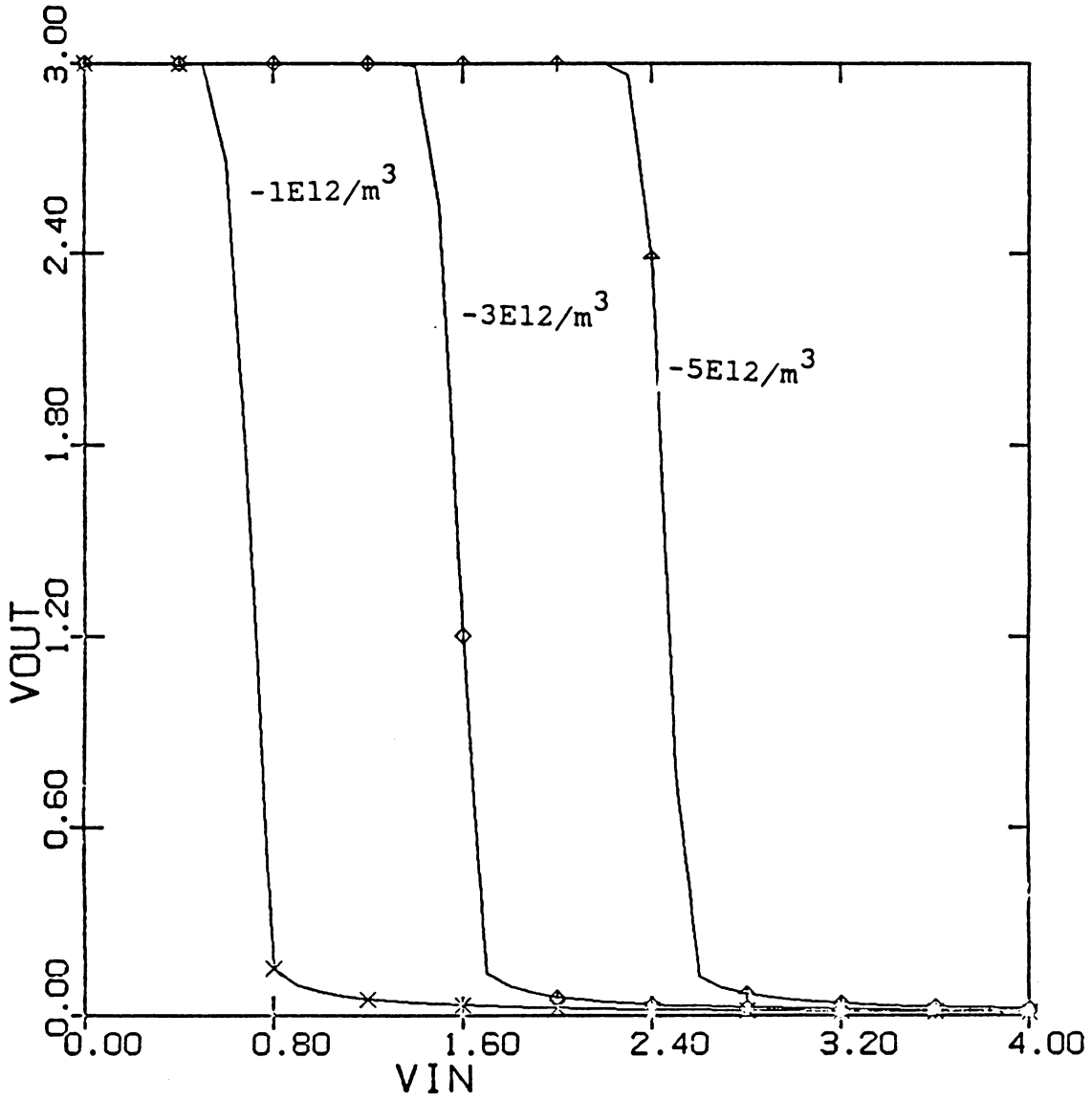

Figure 11: Switching curves for changing NSS. TOX = 95E-9m, NSUB =8E14/m

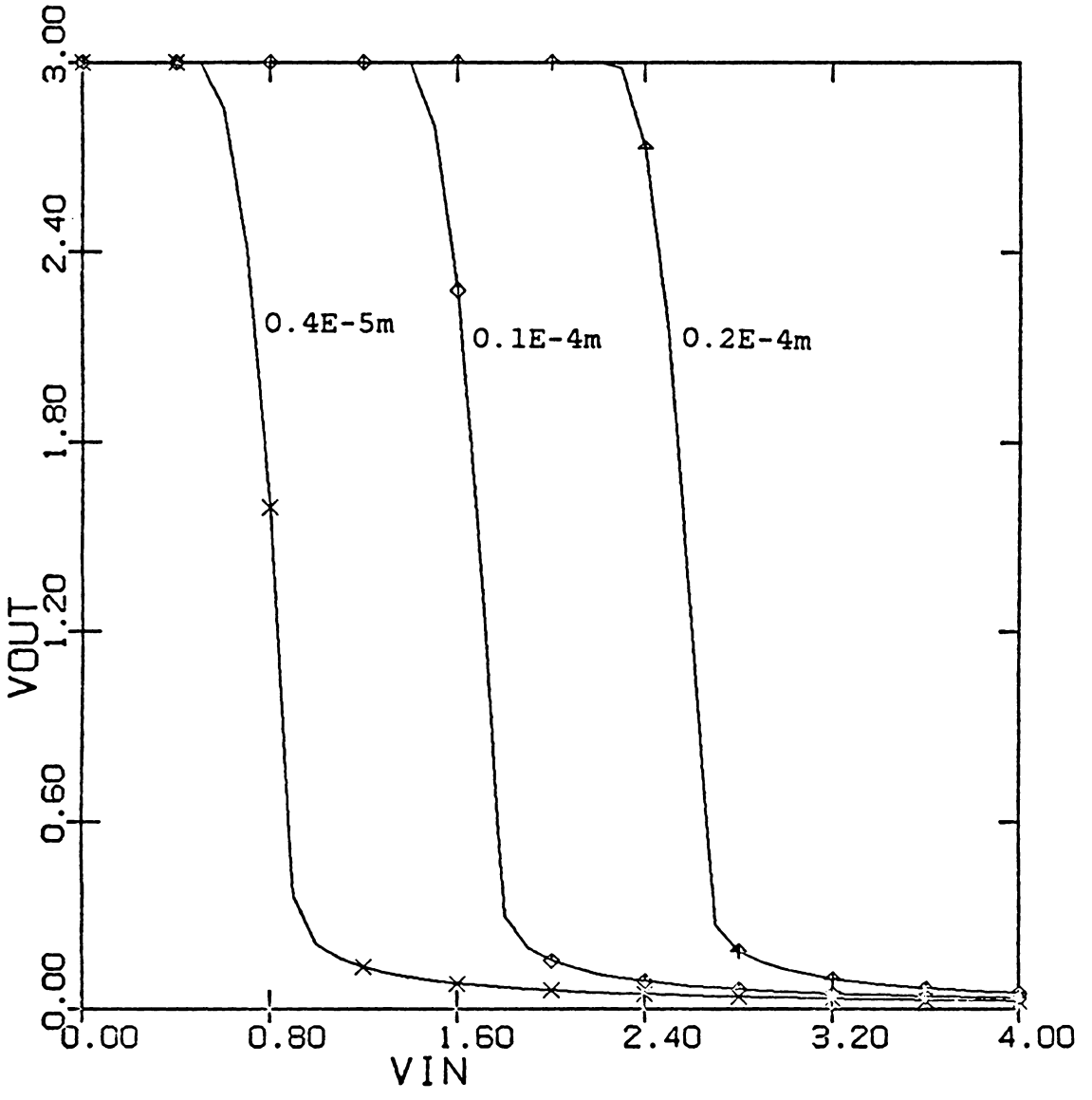

Figure 12: Switching curves for changing TOX. NSS =-5E14/m
NSUB =8E14/m

illustrated in Fig. 13. The oxide thickness will be held constant since changing TOX would effect the threshold voltage and this is undesirable.

Assuming TOXL = TOXS, we get

$$\frac{K_L}{K_S} = \frac{W_L \cdot L_S}{W_S \cdot L_L}$$

Therefore, the K-factor can be changed in the following ways:

1. Let WS = WL and change LL and LS.
2. Let LL = LS and change WS and WL.
3. Change L and W for both transistors.

In the fabrication process, it is desired that constraints on the dimensions be minimized. It would be desirable to make as few changes in W and L as possible. For example if we keep W fixed for both TL and TS then L can be varied by changing the spread of the gate material over the diffused area. This is illustrated by Fig. 14. In this way, K-factor can be changed directly by changing L as given by this relation where C is the proportionality constant.

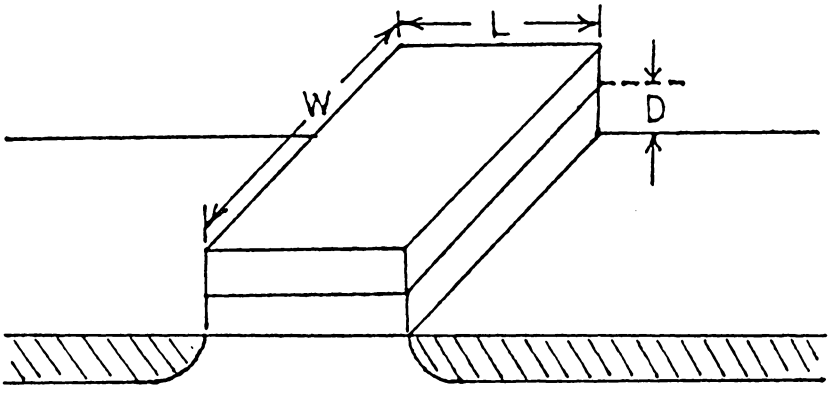

Figure 13: Schematic Illustrating The Gate Dimensions

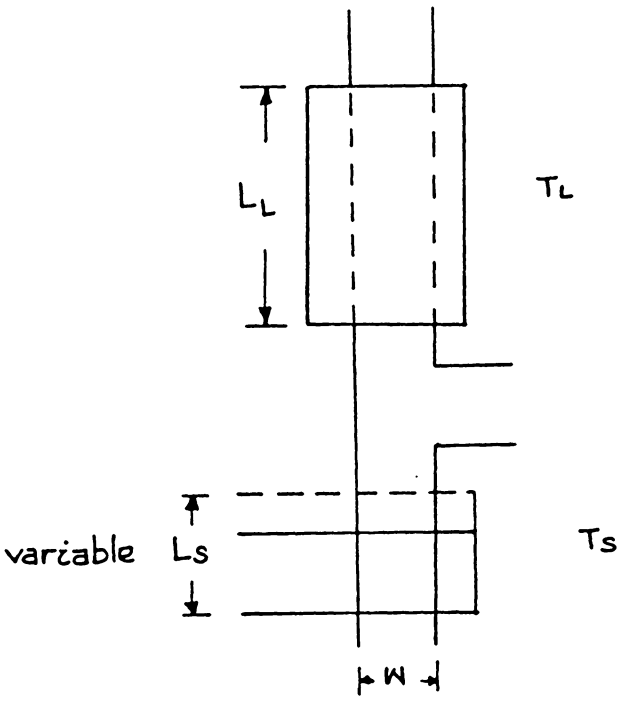

Figure 14: An inverter structure with same W but different L

Examining Eq. 4.2 it is seen that changing L to get different K-factors provides a reasonable technique for obtaining different switching voltages. Selecting this ratio to be physical parameter which sets the value of VSW for a particular switching pair is very advantageous in terms of meeting required tolerances. Considering that LL and LS are usually defined within the same physical processing step, any discrepency which affects the length of one device will have the same effect on the other. For example, if the length LS is off by -10%, then the length LL will also be off by -10%. This variance in the value for LL and LS will not affect the ratio LL/LS and thus the target value for VSW will still be obtained.

Figure 15 shows a plot of VSW vs the ratio of K-factors for different values of threshold voltages. These curves provide a means for determining the KL/KS ratio necessary for obtaining a particular VSW using a VTS, VTL pair.

Consider the following example of a four valued logic system. The logic levels for this system are say, 0, 1, 2, and 3 volts. For such a system, it may be desirable that the switching voltages VSW are 0.7, 1.5, and 2.5 volts for various threshold subcircuits of an MVL gate. Table 1 gives the bandwidths associated with these logic levels. This gives a logic bandwidth of approximately 0.4V that is sufficient for

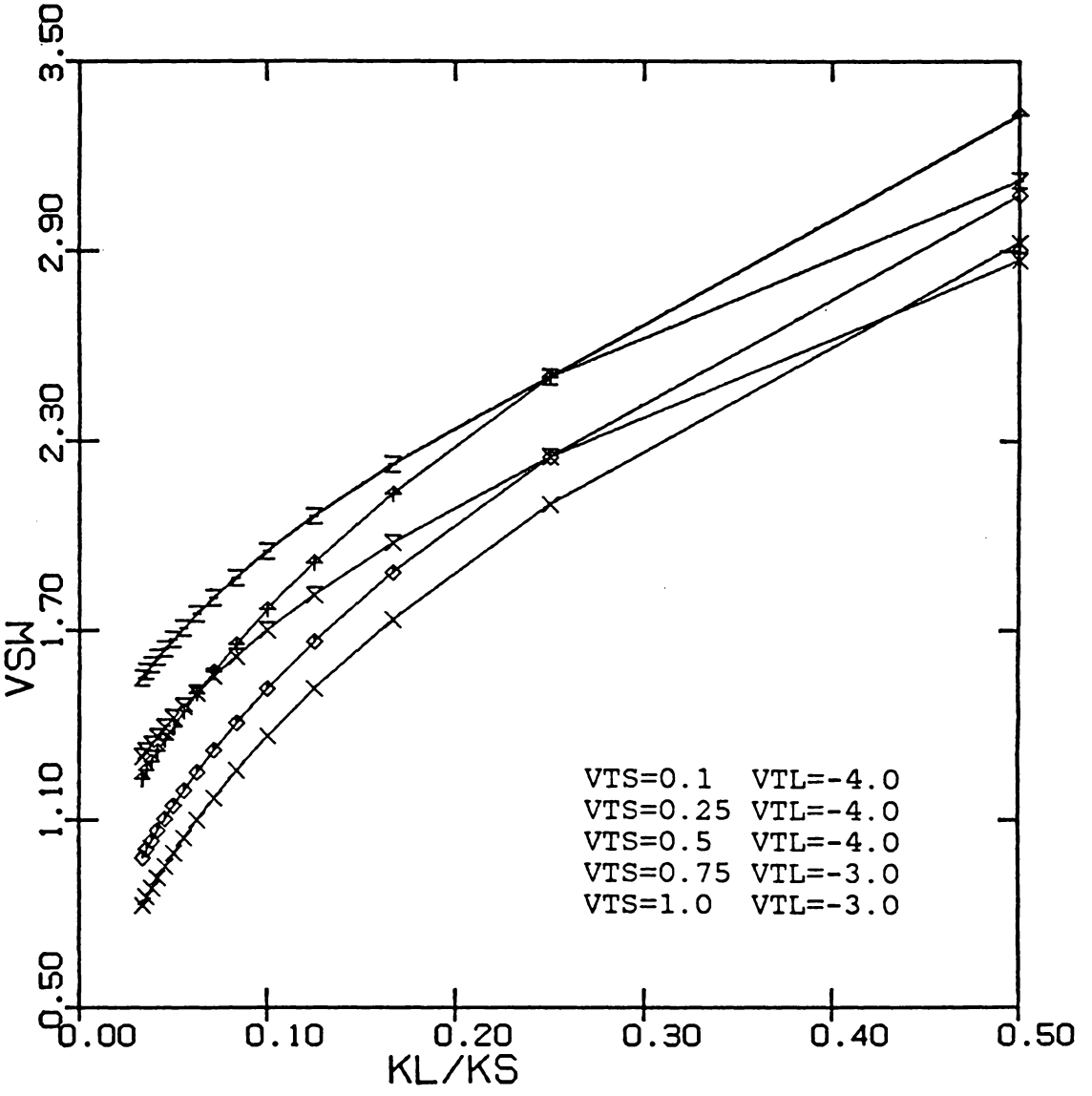

Figure 15: VSW vs K-factors

this system. From Fig. 15, using the curve for VTS = 0.25V and VTL = -4.0V, the ratio of W and L can be obtained and the values of W and L that meet this ratio are given in Table 2.

This table gives some values of LL and LS that will provide the desired ratios of K-factors that were obtained from Fig 15. Note that these are only two sets of the large number of values for LS and LL that will provide the disired VSW. These values were selected because they are practical to implement.

Figure 16 shows the dc switching curves that meet the target values of switching voltages described in the previous example. These curves are calculated by SPICE2 for specified threshold voltage and the ratio of K-factors obtained by adjusting the dimensions of the gates.

It may be required to change W for the transistor in addition to changing L to achieve the given ratio of K-factors. This is done to keep the dimensions of the gate from exceeding the requirements of LSI technology. However, it is desirable to keep W constant.

It can be seen from Fig. 16 that as the ratio, KL/KS, approaches unity the transition is not sharp. In some circuits, KL/KS would have to to be small to get the best performance.

TABLE 1

Logic levels and associated banwidths.

Output Voltage Of The Circuit	Logic Level
0.0-0.7V	0
0.7-1.5V	1
1.5-2.5V	2
2.5 and above	3

TABLE 2

Selected values of W and L for the desired threshold voltage.

Desired VSW	LS	LL (μ)
0.7	3	96
1.5	3	30
2.5	3	6

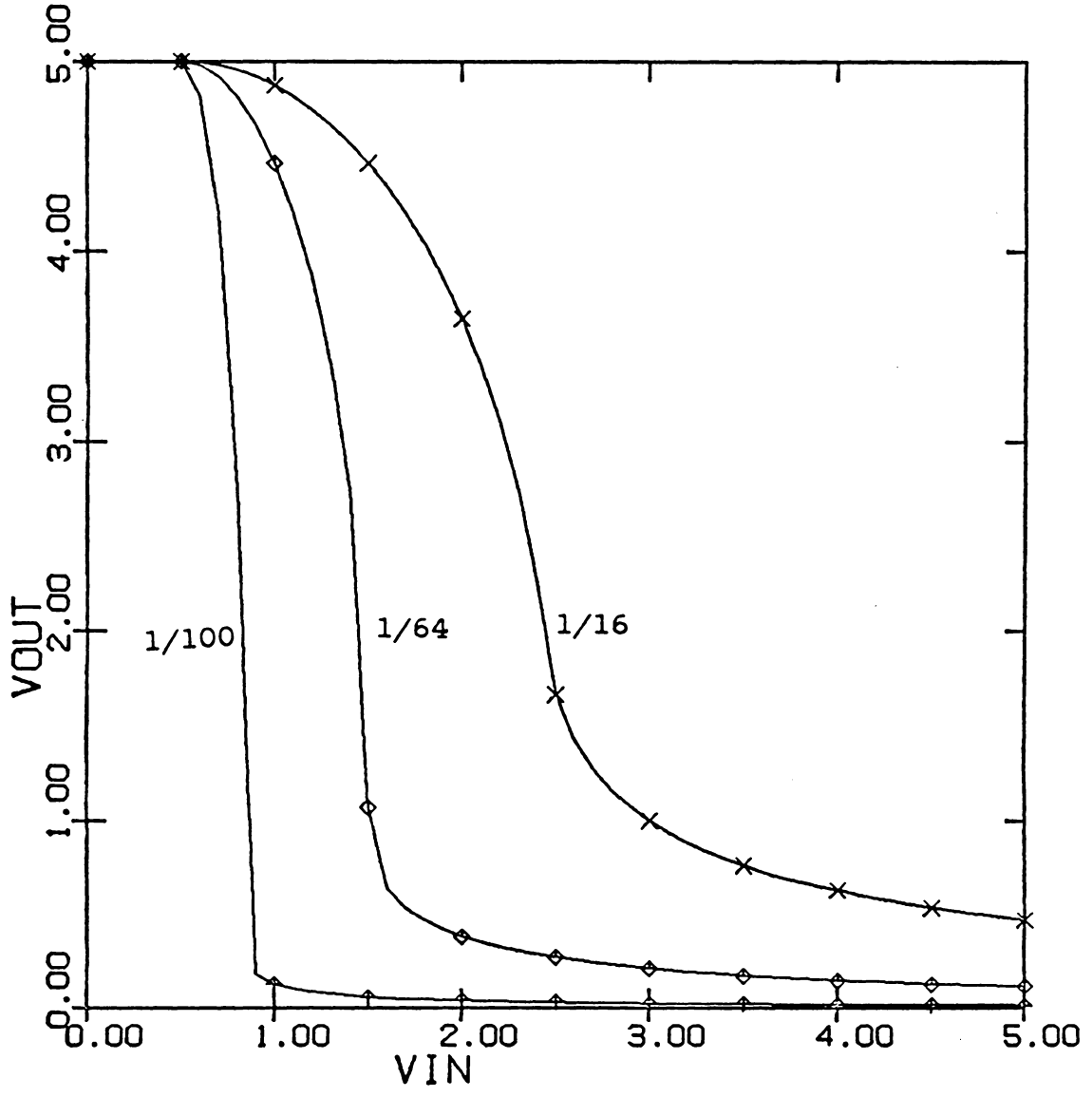

Figure 16: Switching Curves For Changing KL/KS Ratio

4.2 SETTING THE SWITCHING THRESHOLD FOR A MESFET.

Setting the switching threshold for a MESFET suubcircuit is performed in a manner similar to that of a MOSFET subcircuit. However, for M SFET the expressions for the threshold voltage and the transconductance, beta, are different than that of the MOSFET.

The switching voltage for a MESFET inverter is given by the following equation:

$$V_{SW} = -\sqrt{(\beta_L/\beta_S)}.V_{TL} + V_{TS}$$

In order that different sub-circuits have different switching voltages, changes have to be made in the threshold voltages or the betas of the various transistors.

The threshold voltage for a MESFET is given by the following expression:

$$V_T = -\frac{qN_Da^2}{2\varepsilon}$$

where ND is the channel doping concentration.

a is the channel thickness.

q is the electronic charge.

ε is the semiconductor permittivity.

It is seen from this equation that the threshold voltage can be changed by setting the dopant concentration or the channel depth. Changes in switching voltage due to changes in either of these two parameters are illuatrated in Figs. 17 and 18.

Changing the channel depth is a very difficult proposition because the threshold is a function of the square of the channel depth a. Therefore, any error in the fabrication of the channel will result in a much larger error in the value of the threshold voltage. Even changing the doping concentration, ND, is not a very easy task because controlling a single parameter within absolute tolerance is difficult. Therefore, following the arguments stated for the case of the MOSFET inverter it is much more practical to change the beta ratios of the devices to achieve different switching voltages.

An approximate relation of the beta to other physical parameters (gate dimensions) is given as:

$$\beta = \frac{2\varepsilon W}{3La}$$

where ε is semiconductor permittivity.

W is the gate width.

L is the gate length.

a is the channel depth.

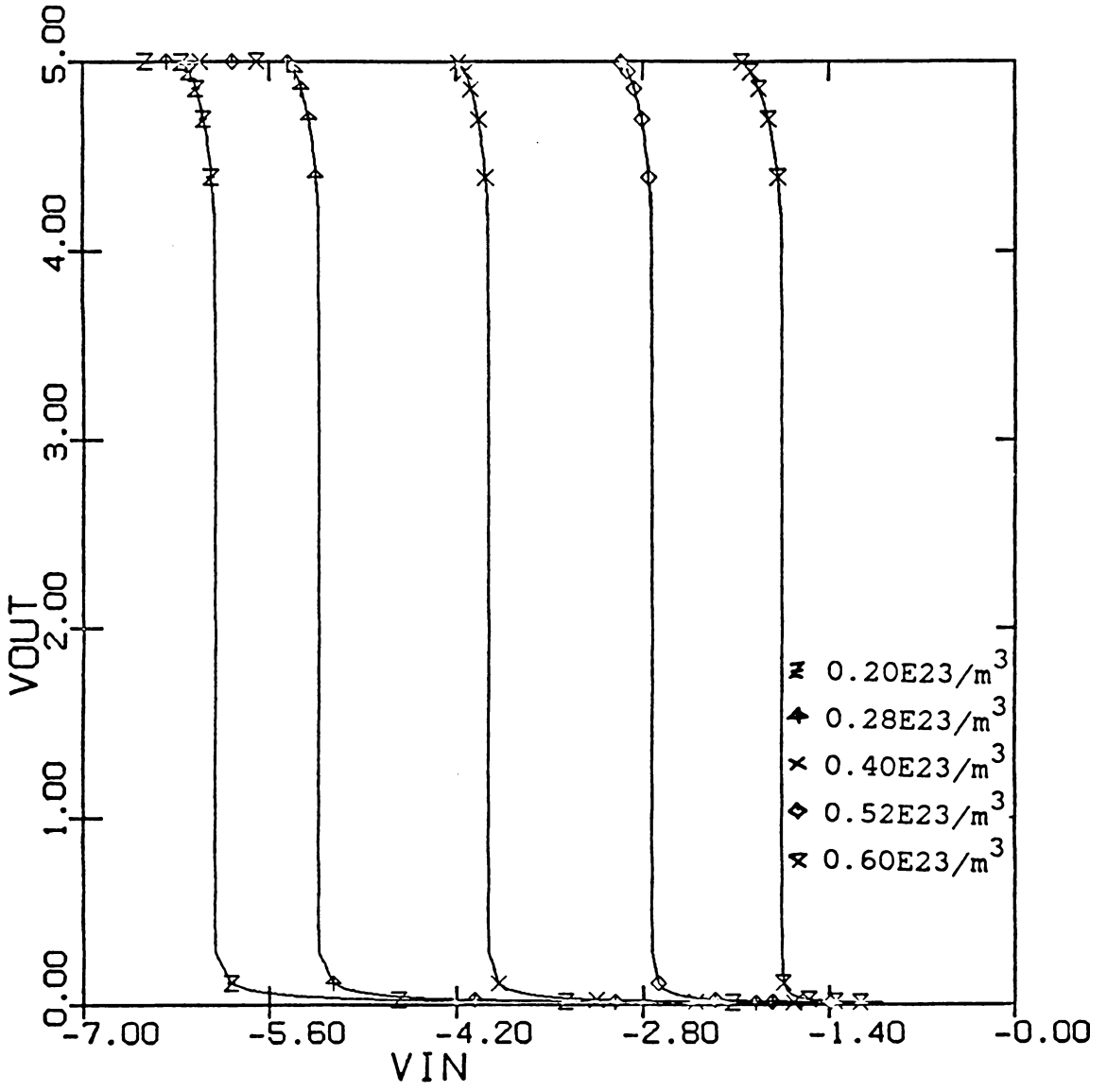

Figure 17: Switching curves for different ND in a MESFET circuit

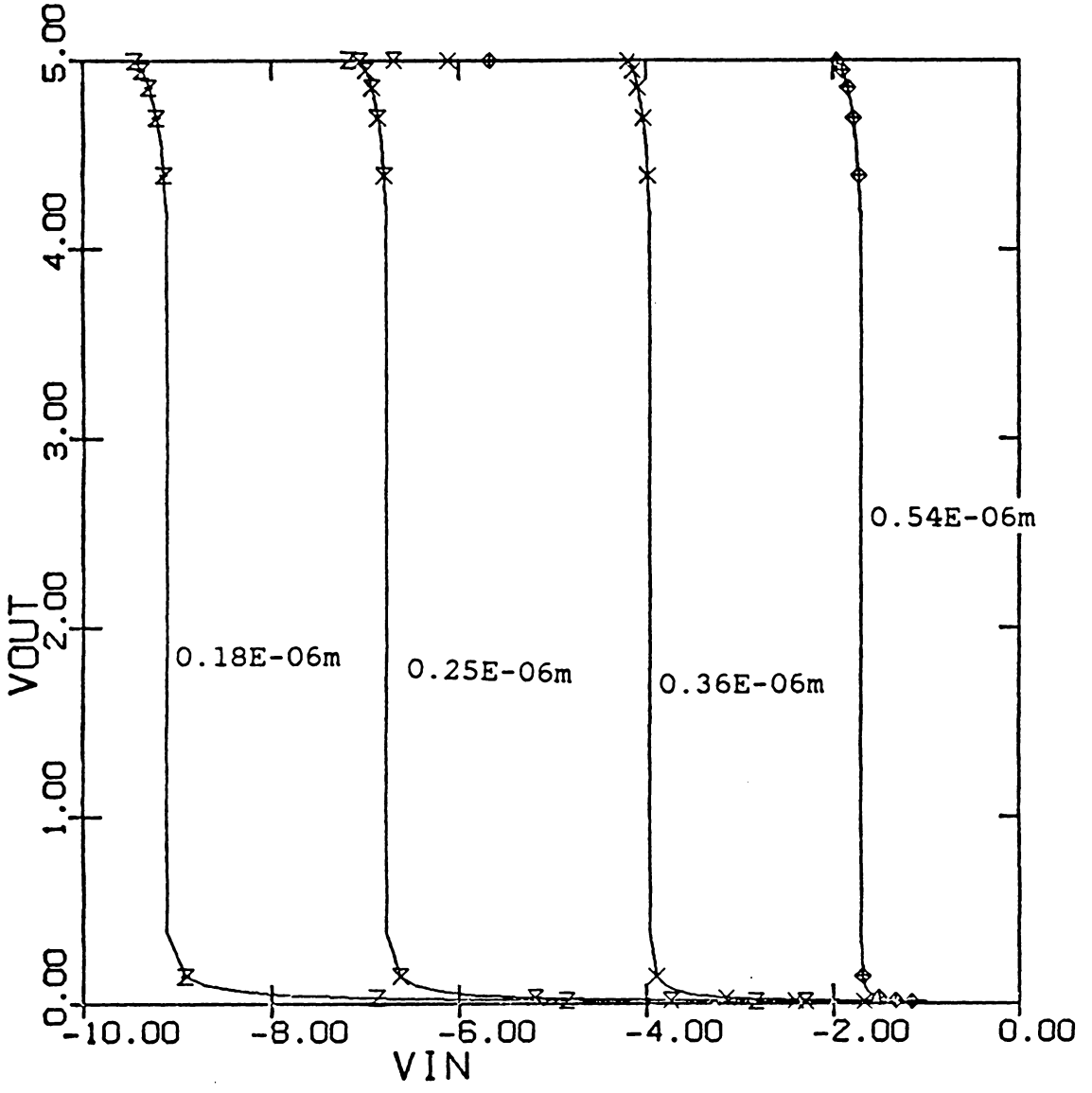

Figure 18: Switching curves for different a In a MESFET circuit.

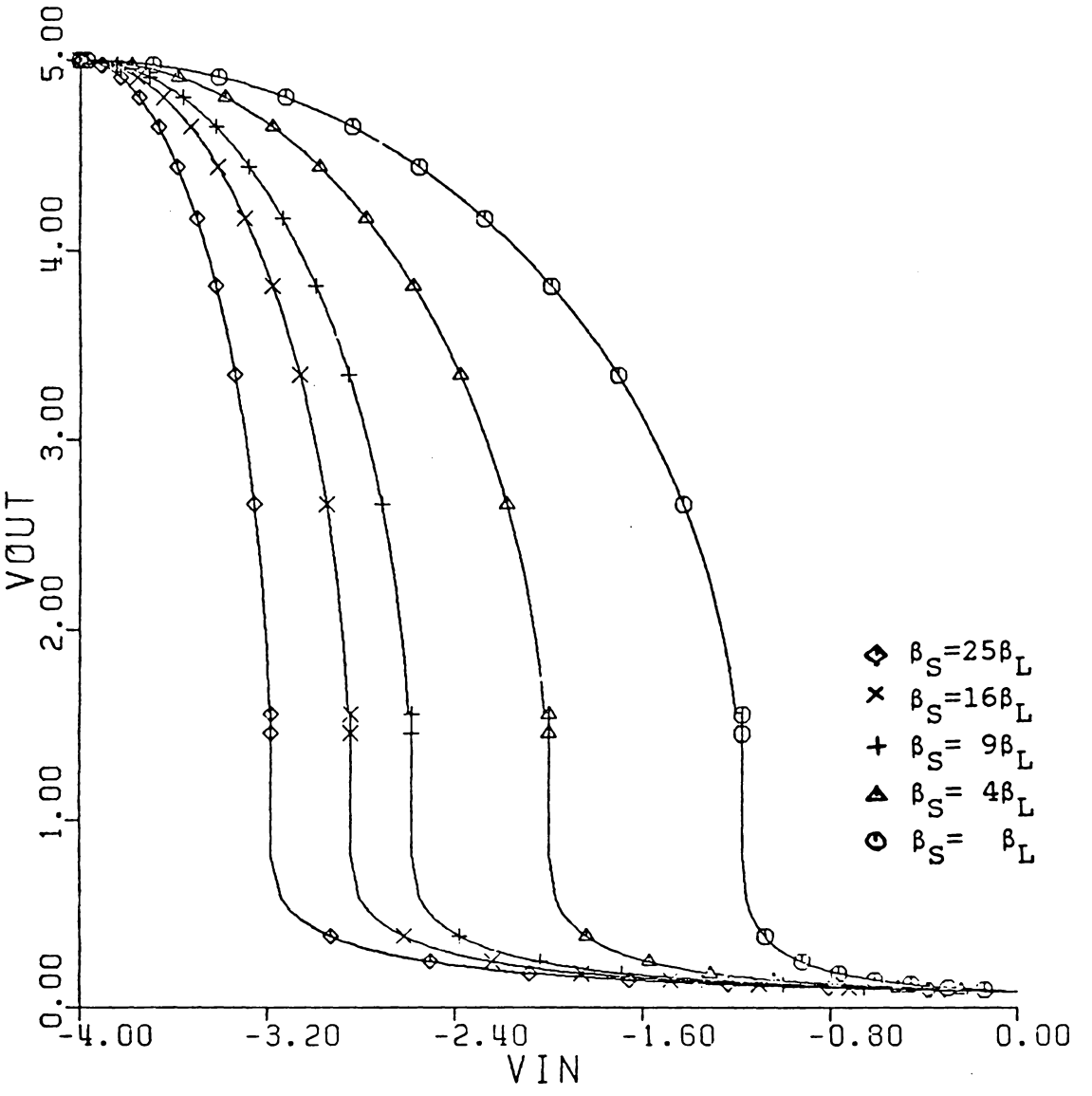

Figure 19: DC transfer char. of MESFET inverters with different KL/KS ratio.

This equation shows that it is possible to change beta by changing the length and width of the gate. Fig. 19 is a plot of a family of dc transfer characteristics of the threshold circuit. Each curve in this plot has a different WL/WS ratio.

As in case with MOSFET based MVL circuits, MESFET circuits do not display fast response if the ratio of transconductances approaches unity. Therefore, even though changing the ratios may be an easier way to achieve MVL behaviour, yet in some applications, it might be necessary to change the threshold voltage in order to vary switching voltage.

4.3 VARIATION IN SWTCHING THRESHOLD DUE TO FABRICATION ERRORS.

It has been stated previously that fabrication technology is not is not developed to an extent where it can provide precise doping or dimensions in an integrated circuit. This section includes graphs that illustrate the change in switching threshold caused by deviation of device parameters from actual values.

The next chapter is a discussion of several MVL circuits. The MVL behaviour in these circuits was obtained by manipulating the ratio of transconductances of the devices.

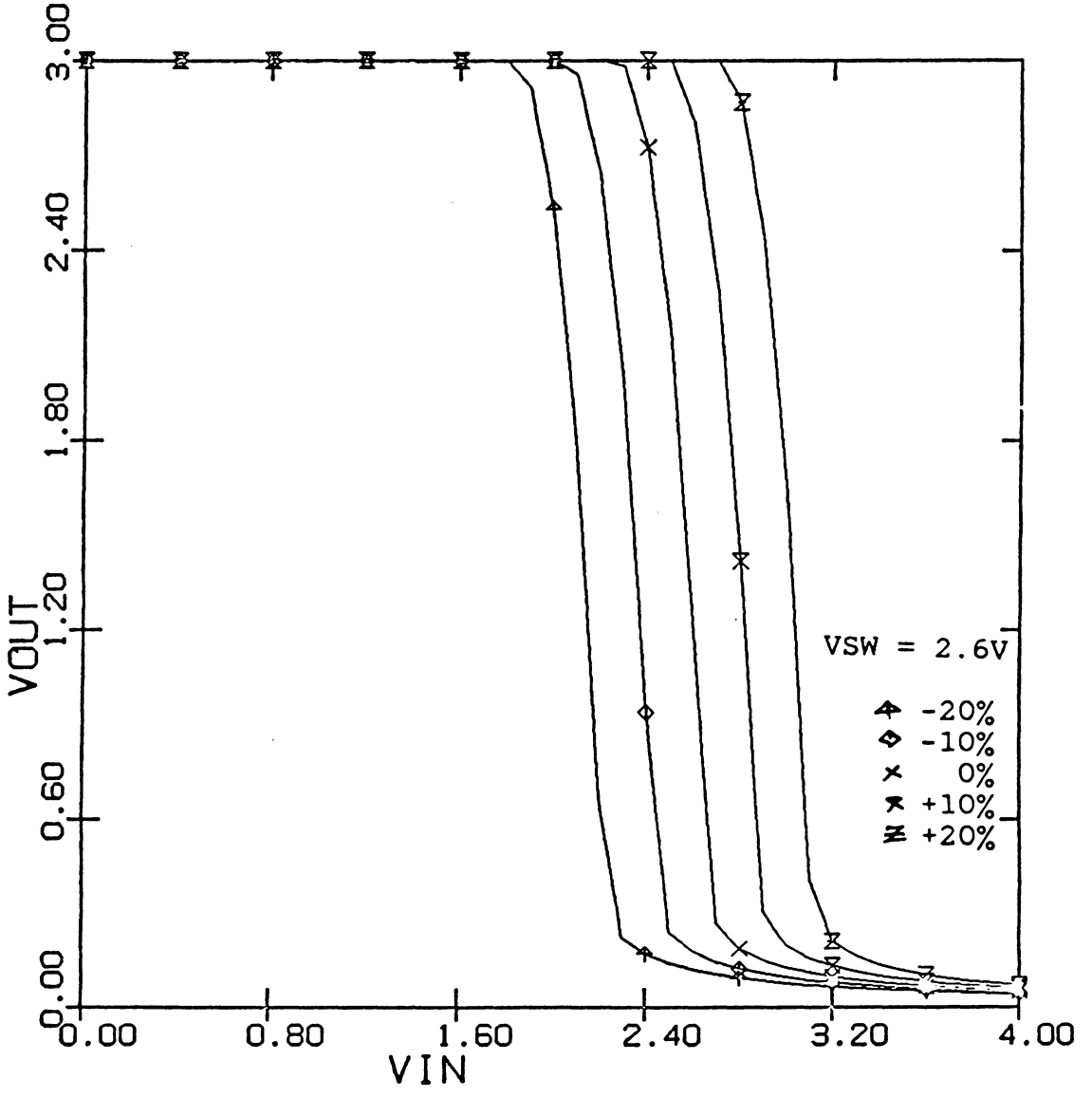

Figure 20: Graphs for percentage change in the value of NSS for a MOSFET.

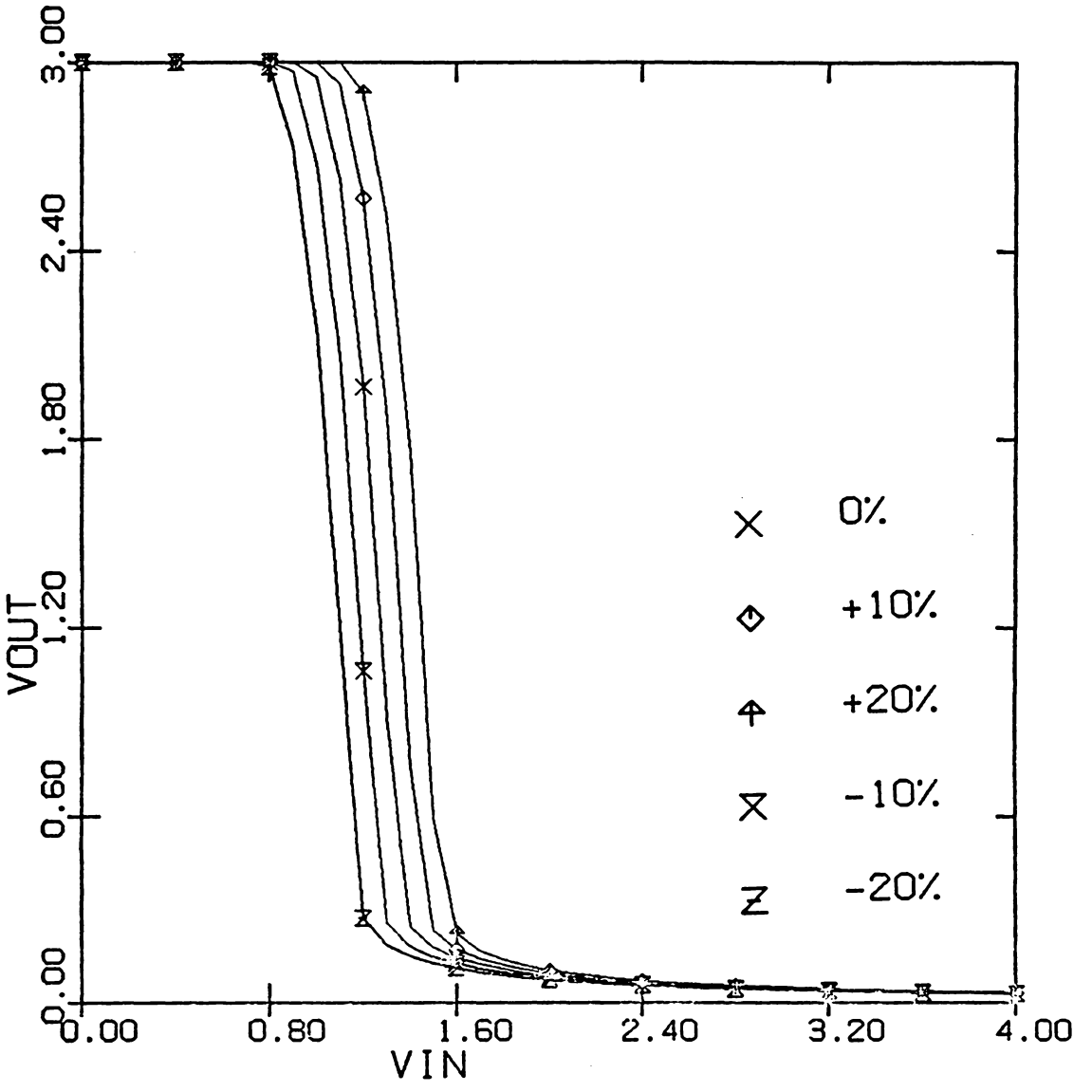

Figure 20:

Graphs For Percentage Change In The Value Of NSS For a MOSFET.

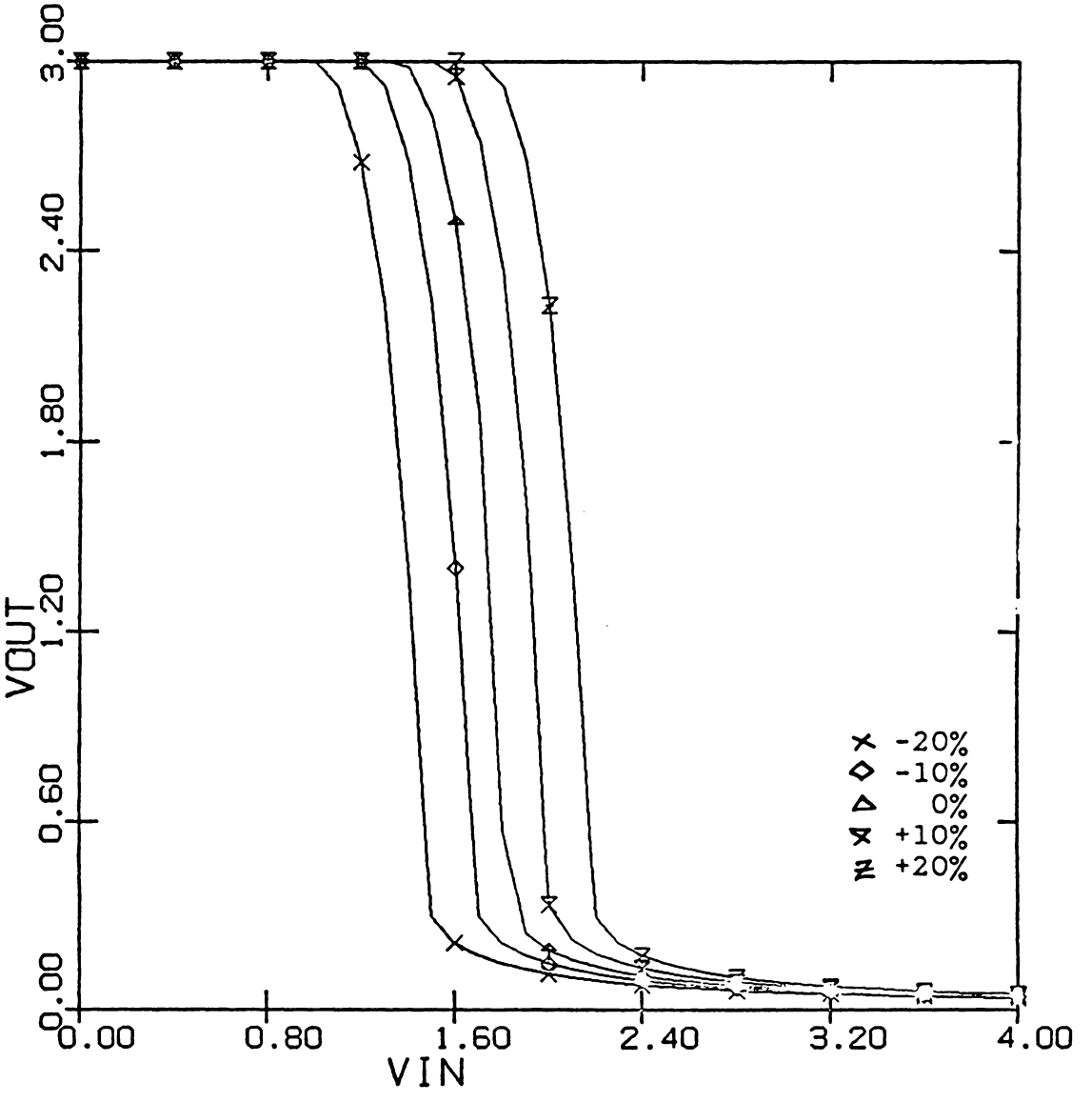

Figure 22: Graphs for percentage change in the value of TOX for a MOSFET.

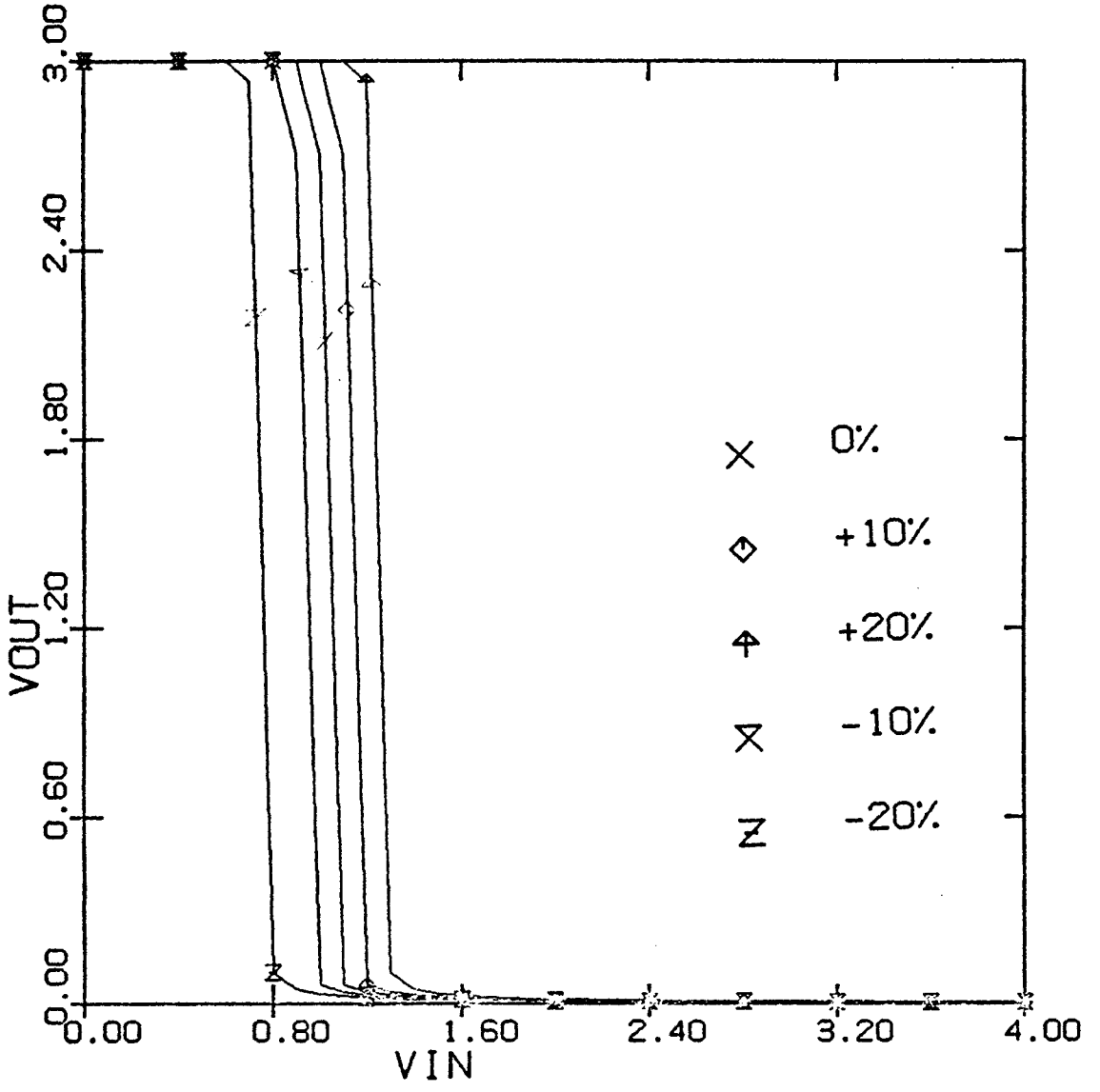

Figure 21:

Graphs For Percentage Change In The Value Of
For a MOSFET.

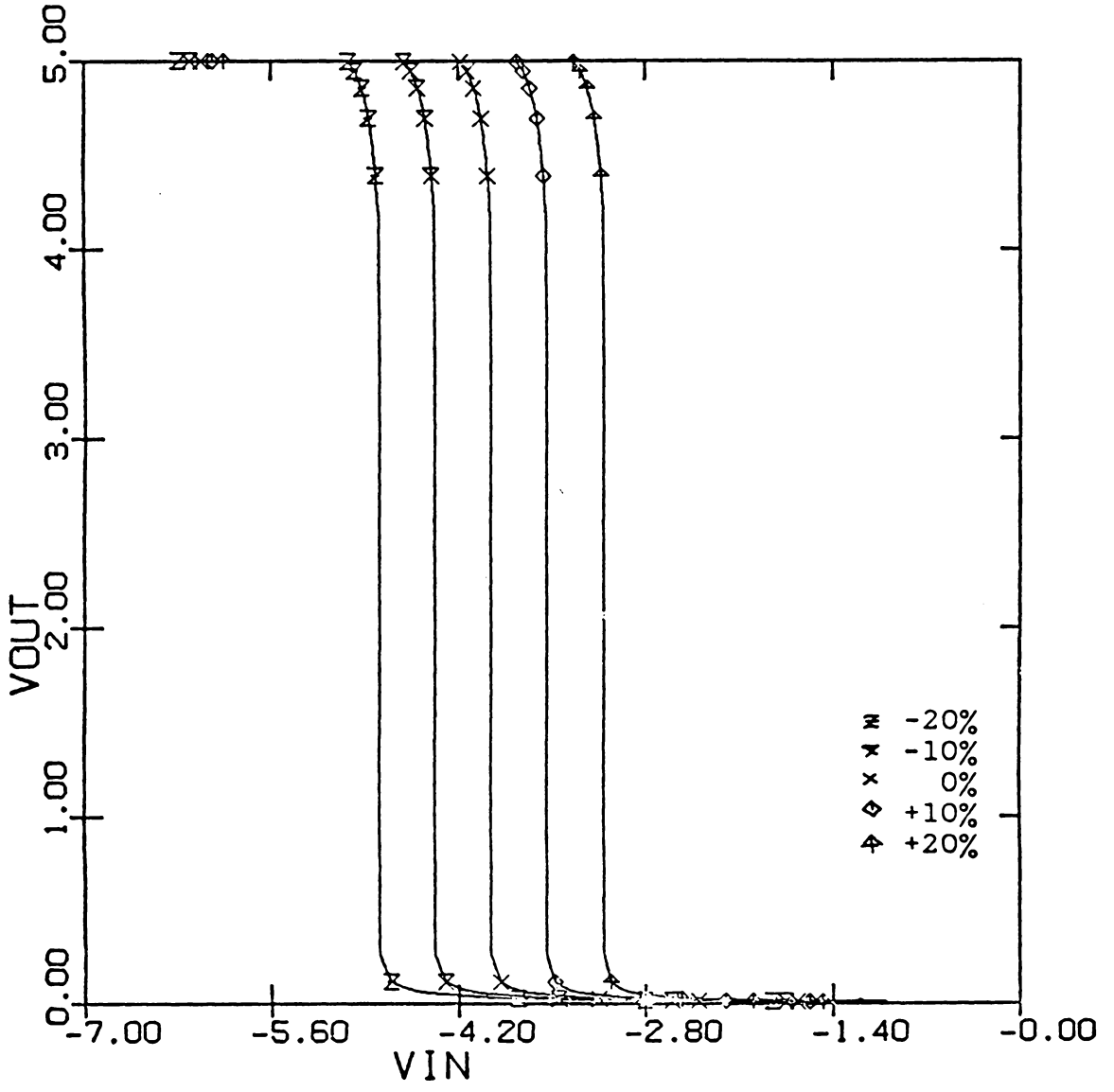

Figure 24: Graphs for percentage change in the value of ND for a MESFET.

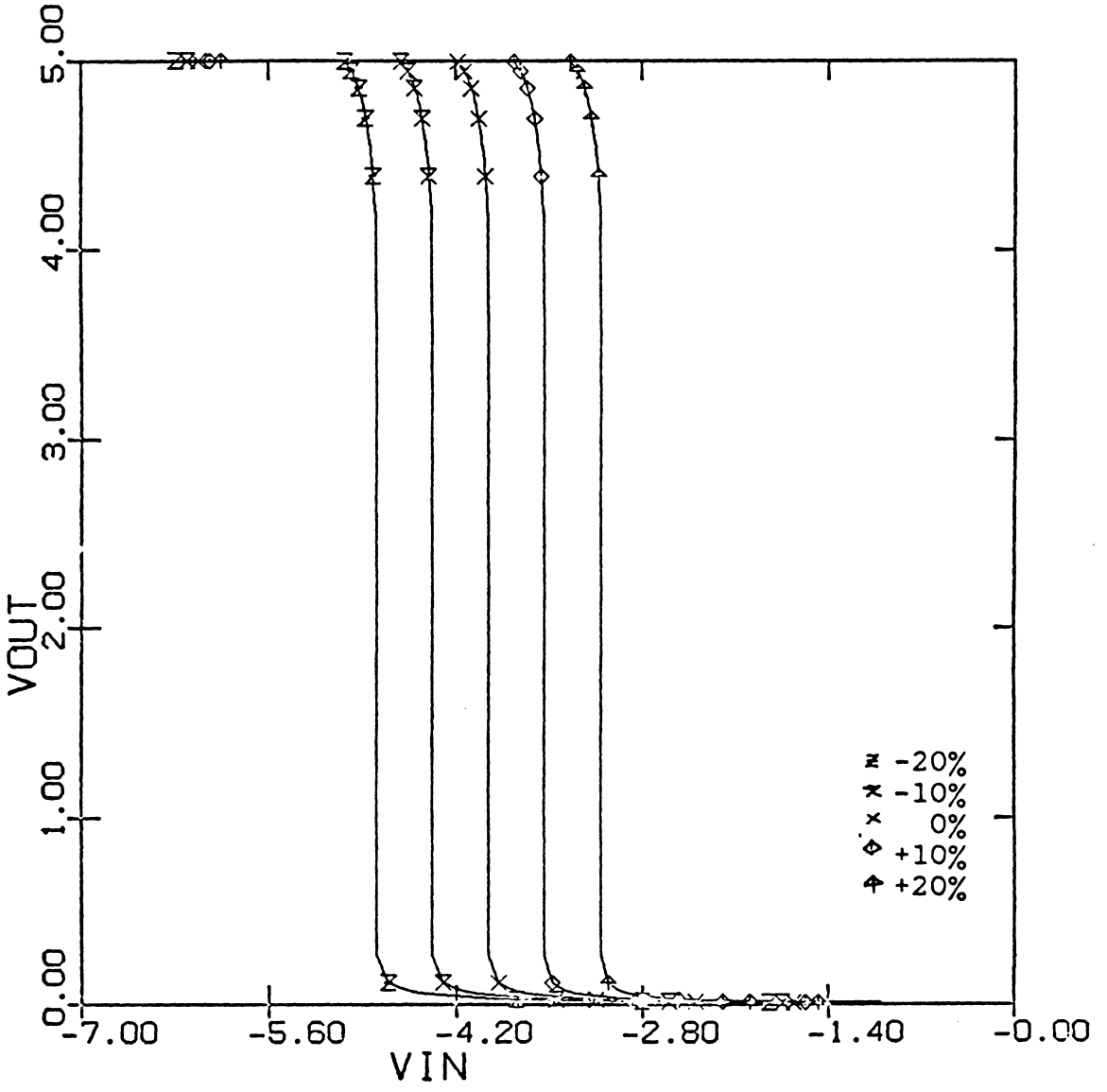

Figure 25: Graphs for percentage change in the value Of a for a MESFET.

Figures 20 through 25 indicate that, even though the switching voltage changes with a change in these physical parameters, yet it still remains within the bandwidth of the system.

For example, a 10% deviation in the value of NSS and TOX, would change VSW by approximately 0.3V which is still in the dead band as illustrated in Fig. 8. Hence, it is possible to achieve MVL behavior by changing the threshold voltage.

Chapter V

MVL CIRCUIT DESIGN.

In the last chapter, techniques to obtain MVL behaviour in FET based circuits, were discussed. The basis for MVL behaviour in FET based circuits are the circuit building blocks, or the sub-circuits , comprised of transistor pairs. One transistor acts as a switching transistor while the other acts as an active load device. Each pair has a different switching characteristic. The switching characteristics can be altered by changing some physical parameters of the devices. In the previous chapter, it was argued that, from a practical viewpoint changing a single parameter, and therefore, changing the threshold voltage was a difficult proposition. It was shown that, it is possible to change the switching voltage of a sub-circuit by changing the ratio of transconductance parameters.

In section 5.1 and 5.2, an attempt is made to develop MVL circuits that are based on the above principle of using the K-ratio to set the switching threshold. The circuits developed using MOSFETS are:

1. LITERAL Gate.
2. Read-Only Memory Cell.
3. NOT(MIN) and NOT(MAX) Gate

Designs for MOSFET NOT(MIN) and NOT(MAX) gates are given in section 5.3. These designs are an examples where the K-ratio design principal cannot be applied. These circuits would help to lay the basis for the development of even more complex MVL circuits.

5.1 LITERAL GATE.

5.1.1 Theoretical Background.

The MVL algebra as proposed by Allen and Givone [4] introduces the idea of a literal gate. A literal gate can be defined as follows:

$$\text{LITERAL}(A,a,b) = A^{a,b} = \begin{cases} m-1 & a \leq A \leq b \\ 0 & \text{otherwise} \end{cases}$$

where A is the logic variable.

a,b are constants such that

a and b in are the range (0,1,2..m-1)

and $a \leq b$.

m is the radix of the system.

Shown in Fig. 26 are the characteristics of a literal gate in a 4-valued system. Literal gates are of importance because they are unary operators needed for completeness in the Allen-Givone algebra. It will also be shown later how they can be used to in memory circit design.

Using the definition of a literal function and a 4-valued system wherein the logic level zero corresponds to 0V, logic 1 corresponds to 1V etc., the output of the literal gate would be:

For a gate $X^{a,b}$

$$VOUT = 3 \quad a \leq VIN \leq b$$

$$= 0 \quad \text{otherwise.}$$

The circuit for the literal gate shown in Fig. 27 meets these requirements. The dc transfer characteristics as simulated by SPICE2 fore the literal gate, $X^{1,1}$, are shown in Fig. 26. The output is 'high' for a band of input voltages. It can be seen that the high state covers the appropriate range of input voltages and is thus sufficient to cause appropriate changes in the circuit elements that are connected to the literal gate.

The description of the literal gate circuit is as follows: refering to Fig. 27 it is seen that the complete circuit consists of four threshold circuits. The inverter I1 has a switching voltage of 0.8V and the inverter I2 has a switching voltage of 1.2V. Inverter I3 and I4 have no constraints with regards to the switching voltage as they are used for the purpose of binary inversion only, whereas, I1 and I2 are used to sense the multi-valued input voltage levels.

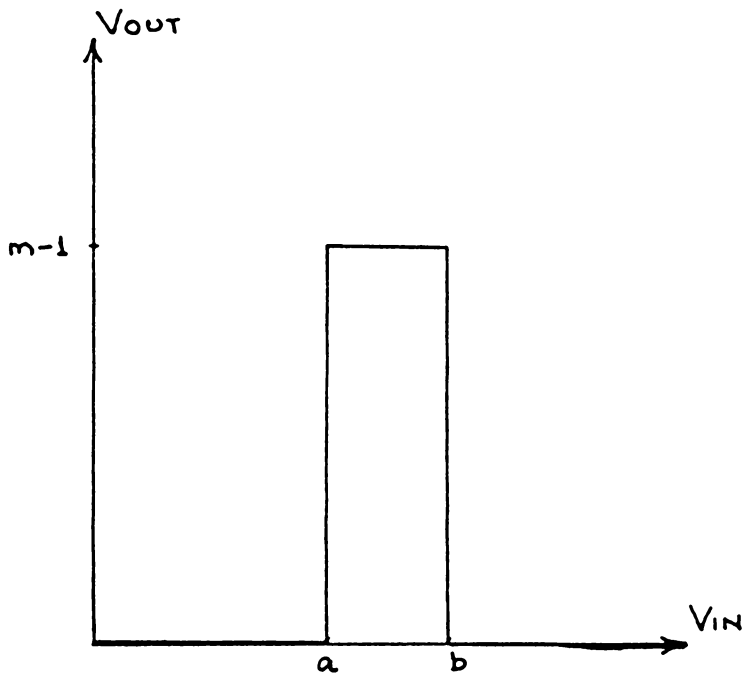

Figure 26: The DC characteristics of a LITERAL gate.

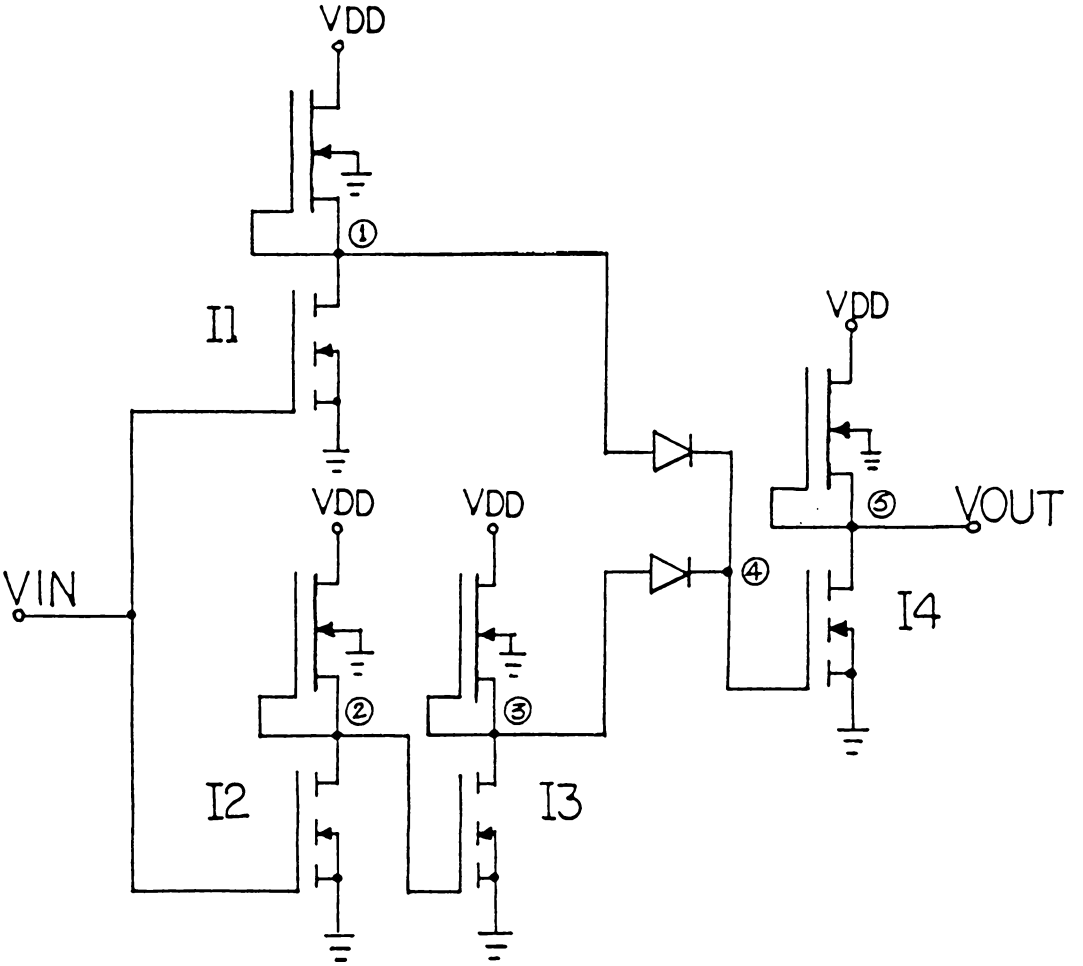

Figure 27: Circuit diagram of a LITERAL gate.

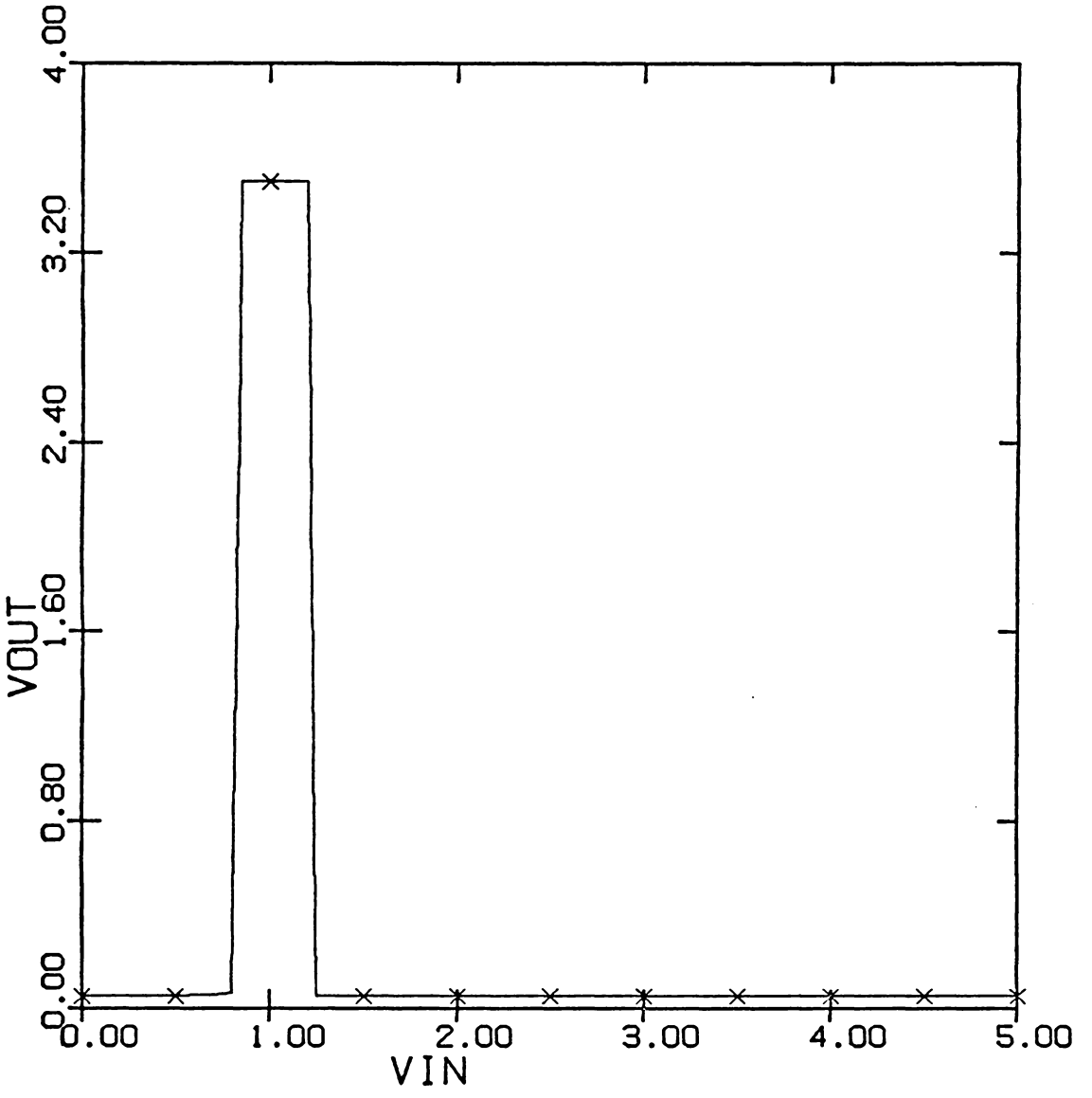

Figure 28: DC transfer characteristics of the LITERAL gate of Fig. 2.

Suppose the input voltage is at zero volts and it starts to rise. As the input crosses 0.8V, V(1) changes from logic 3 to logic 0 level as in Fig. 29(a). V(2) goes from logic 3 to logic 0 level when the input rises above 1.2V, as in Fig. 29(b). I3 invertes V(2), and this is shown in Fig. 27(c). The diode pair senses the maximum of V(1) and V(3) and places it on node 4. In effect the diode pair performs point by point addition of the incoming voltages. Inverter I4 inverts the voltage, V(4), and Fig. 29(e) shows the output of the literal gate.

The output is centered at VIN=1V. The width of the band of input voltages over which VOUT is logic 3 can be changed by changing the switching voltage of inverters I1 and I2. The switching voltages of these inverters are varied by changing the K-ratio of the devices. The threshold voltages, once determined, were maintained constant for all devices. The values of VTS, VTL and the K-ratios are shown in Table 3.

The same literal gate can also be implemented using MESFETs. Literal gates for a five-valued system have been developed by Tront and Givone [12], one of which is reproduced here in Fig. 30.

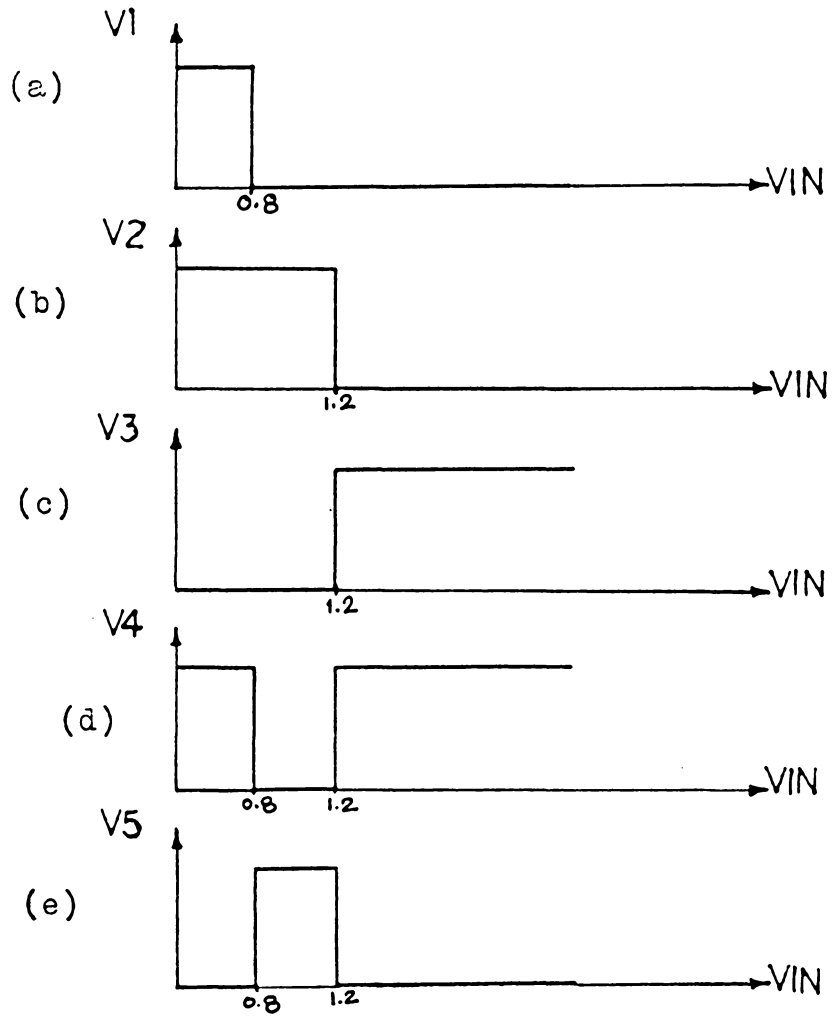

Figure 29: Waveforms of voltages at different nodes of the LITERAL gate.

TABLE 3

Threshold Voltages and K-Ratios for the Literal Gate.

	VTS	VTL	K-RATIO	VSW
INVERTER 1	0.6	-2.0	100	0.8
INVERTER 2	0.6	-2.0	9	1.2
INVERTER 3	0.6	-2.0	100	0.8
INVERTER 4	0.6	-2.0	100	0.8

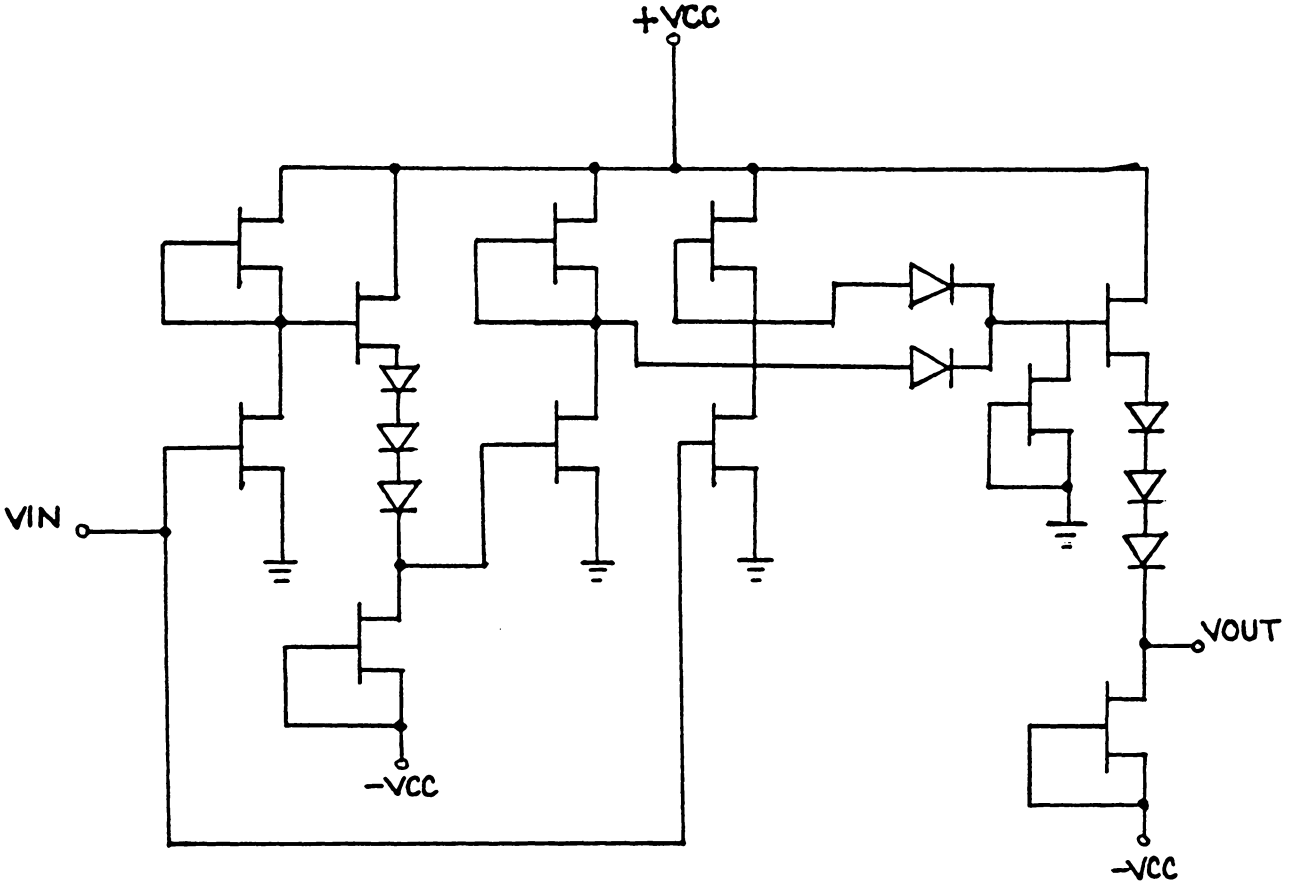

Figure 30: A MESFET based five-valued LITERAL gate.

5.2 READ-ONLY MEMORY CELL.

The following section introduces the idea of implementing a set of basic MVL read-only memory cells. The basic building block in the design is again the threshold circuit described in Chapter 3.

The memory cell uses literal gates, described in the last section, as address selectors. In effect, the literal gate functions as a selector which places a 'high' voltage on one of the lines going to the memory cell. In order to select a memory cell for readout, both the column-select and the row-select must be 'high'. Values are stored in each cell by connecting an appropriate pull up voltage for the cell.

The setup of the memory cell is shown in Fig. 31. In this figure the cell blocks, B1, B2, B3 and B4, are comprised of transistor pairs. These transistors pairs are turned on by the enabling signals from the literal gates as shown in Fig. 32. Also shown in Fig. 32, is the way in which the transistor pairs are connected inside each block. The working of this memory cell is explained in the following example:

EXAMPLE: Let VROW = 1V.

and VCOL = 2V.

$$\text{VROW} = 1\text{V implies } \text{VOUT}(\overset{0,0}{XU}) = \text{VOUT}(\overset{2,2}{XU}) = \text{VOUT}(\overset{3,3}{XU})$$

$= 0V.$

and $VOUT(^{1,1}XU) = 3V.$

$VOUT(^{1,1}XU) = 3V$ enables block B2.

VCOL = 2V implies $VOUT(^{0,0}XL) = VOUT(^{1,1}XL)$

$= VOUT(^{3,3}XL)$

$= 0V.$

and $VOUT(^{2,2}XL) = 3V.$

$VOUT(^{2,2}XL) = 3V$ turns on QL2(Fig. 9)

From 1 and 2 it is seen that for this case

VOUT = VDD(QU2,QL2 pair)

In this way depending on the value of the voltages, VROW and VCOL one of the sixteen pairs is enabled and VOUT is the corresponding VDD. It is possible to fix the value of this VDD at the masking step during fabrication of the circuit. The values of VTS, VTL, KS/KL are as follows:

VTS=0.5V VTL=0.5V KL/KS=0.1

The VSW for the literal gates are selected in a manne similar to those of section 5.1. Typical values for the VTs and K-ratio for one type of literal gate can be found in Table 3.

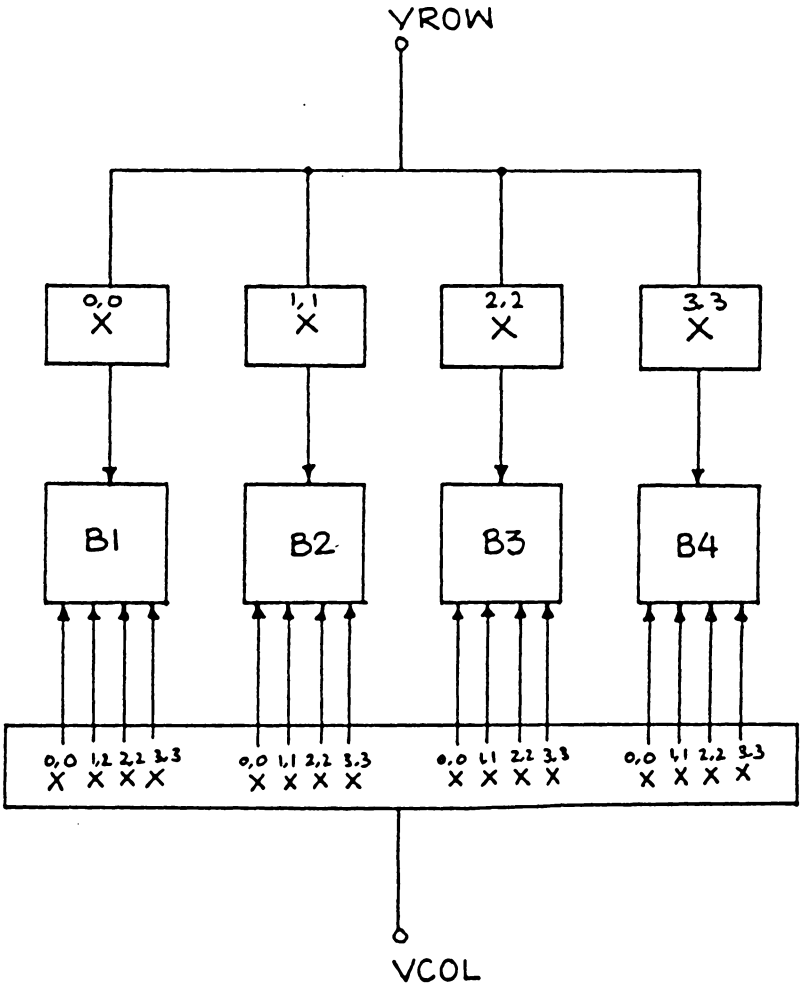

Figure 31: Setup of the memory cell.

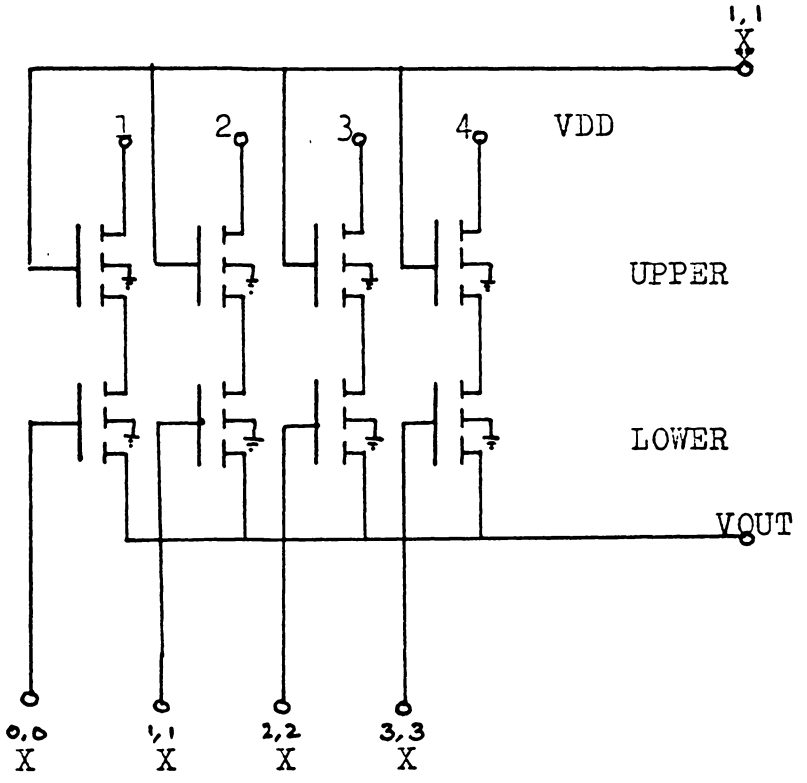

Figure 32: Circuit Diagram Of The Memory Block.

5.3 FOUR-VALUED NOT(MIN) GATE.

The threshold circuit discussed in detail in previous chapters is used here to configure an MVL logic gate. The logic function implemented, and it's truth table is given in Table 4.

It will be in order at this point to give a definition of the complementary function.

DEFENITION: Let A be a logic variable whose range of value is (0,1,2,..m).

Then,

$$COMP(A)=\bar{A}=(m-1)-A$$

Shown in Fig. 33 is the figure for the logic gate and the explanation of how it works is as follows:

The complete logic function is implemented using a number of different threshold circuits which were described in Chapter 3. The circuit consists of two identical parts, one correspoinding to each input. The switching voltage of each threshold circuit is set to a predetermined value and these are indicated in Fig.33. Further, every threshold circuit in each of the two halves are tied to a different supply. This allows each of the sub-circuits to be pulled up to different voltage which is essentially the complement of the logic level which the threshold circit is detecting.

TABLE 4

Truth table for the logic function $\overline{\text{MIN}}(A,B)$.

$Y = \overline{\text{MIN}}(A,B)$

A	B	Y
0	0	3
0	1	3
0	2	3
0	3	3
1	0	3
1	1	2
1	2	2
1	3	2
2	0	3
2	1	2
2	3	1
3	0	3
3	1	2
3	2	1
3	3	3

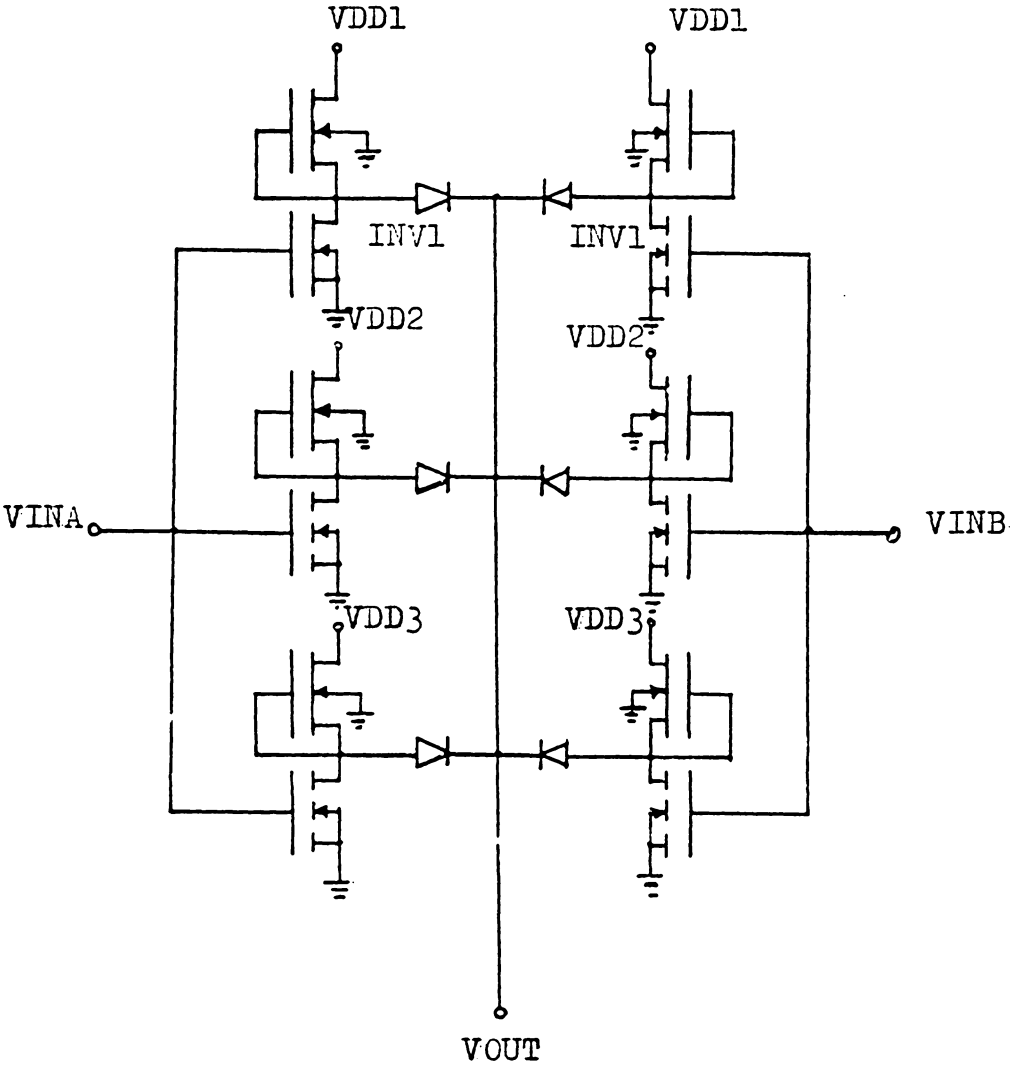

Figure 33: Circuit diagram of the logic gate $\overline{\text{MIN}}(A,B)$.

For input voltags, VINA and VINB, the threshold circuits, having a VSW less than the input voltage,will produce an output of zero. But the circuits that do not switch place their pull-up voltage onto the anode of their respective diode. The diode having the highest voltage is forward biased and this voltage is realized on the output of the logic gate. The following example further facilitates the understanding of the logic gate.

EXAMPLE: VINA = 2V.

VINB = 3V.

MIN(A,B) = MIN(2,3)

=COM(2)

=1.

For VINA = 2V, A1 and A2 switch.

or VOUT(A1)=VOUT(A2)=0V

and VOUT(A3)=VDD(A3)=1V.

For VINB = 3V, B1,B2, and B3 switch.

or VOUT(B1,B2,B3)=0V.

Therefore, anodes of diodes D1, D2, D4, D5, and D6 are at 0V and the anode of D3 is at 1V. Diode D3 is forward biased and VOUT=1V=MIN(A,B).

When attempting to set the VSW for each of the threshold subcircits of the NOT(MIN) gate, it was found that the principle of using K-ratio to select VSW was no longer feasible.

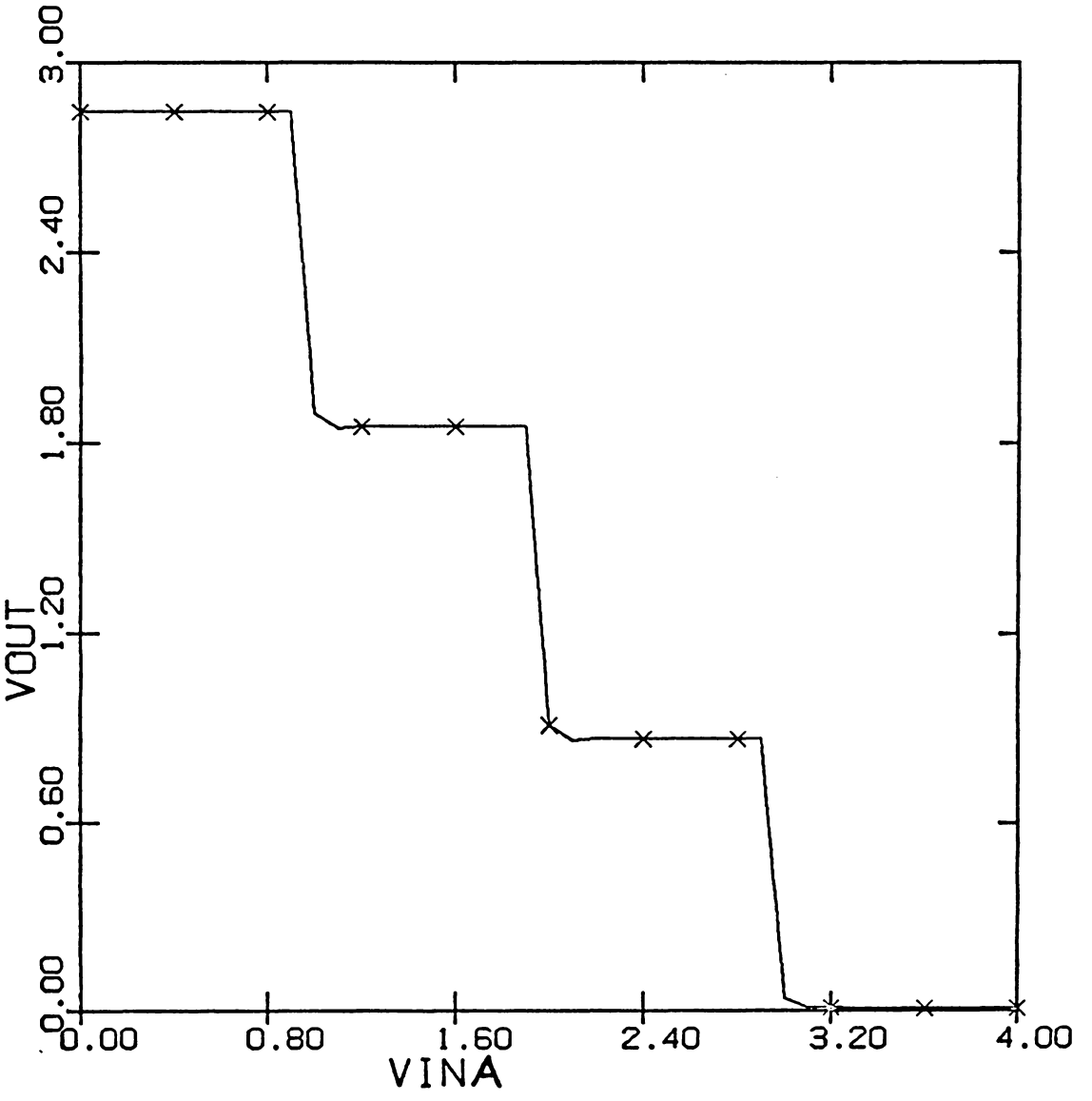

Figure 34: DC Transfer Charateristics For The Logic Gate MIN(A,B).

The required K-ratios and VT's went beyond reasonable technological limits. Instead the VSW's were set by choosing KL/KS to be small and choosing an appropriate VTS in order to obtain the necessary VSW. The values for the KS and the VTS for this gate are shown in Table 4.

Given in Fig. 34 is the dc transfer characteristics of this logic gate as calculated by SPICE2. In this figure VINB=3V, and VINA is increased from 0V to 3V.

Table 6 and Fig. 35 illustrate the implementation of NOT(MAX) gate. The principle of operation is similar to that of the NOT(MIN) gate.

In this chapter emphasis was mainly laid on implementing MOSFET based circuits. These circuits can be very easily realised using MESFETs. But in case of MESFET based circuits a voltage level shifter block would be needed to make these circuits input/output compatible. A variety of MESFET based circuits have been suggested by Tront in [22].

TABLE 5

Values of VTS, VTL, and KL/KS for the NOT(MIN) gate.

	VTS	VTS	KL/KS
INVERTER 1	0.9V	-1.0V	0.01
INVERTER 2	1.9V	-1.0V	0.01
INVERTER 3	2.9V	-1.0V	0.01

TABLE 6

Truth Table for a NOT(MAX) Gate.

Y = NOT(MAX)(A,B)

A	B	Y
0	0	3
0	1	2
0	2	1
0	3	0
1	0	2
1	1	2
1	2	1
1	3	0
2	0	1
2	1	1
2	2	1
2	3	0
3	0	0
3	1	0
3	2	0
3	3	0

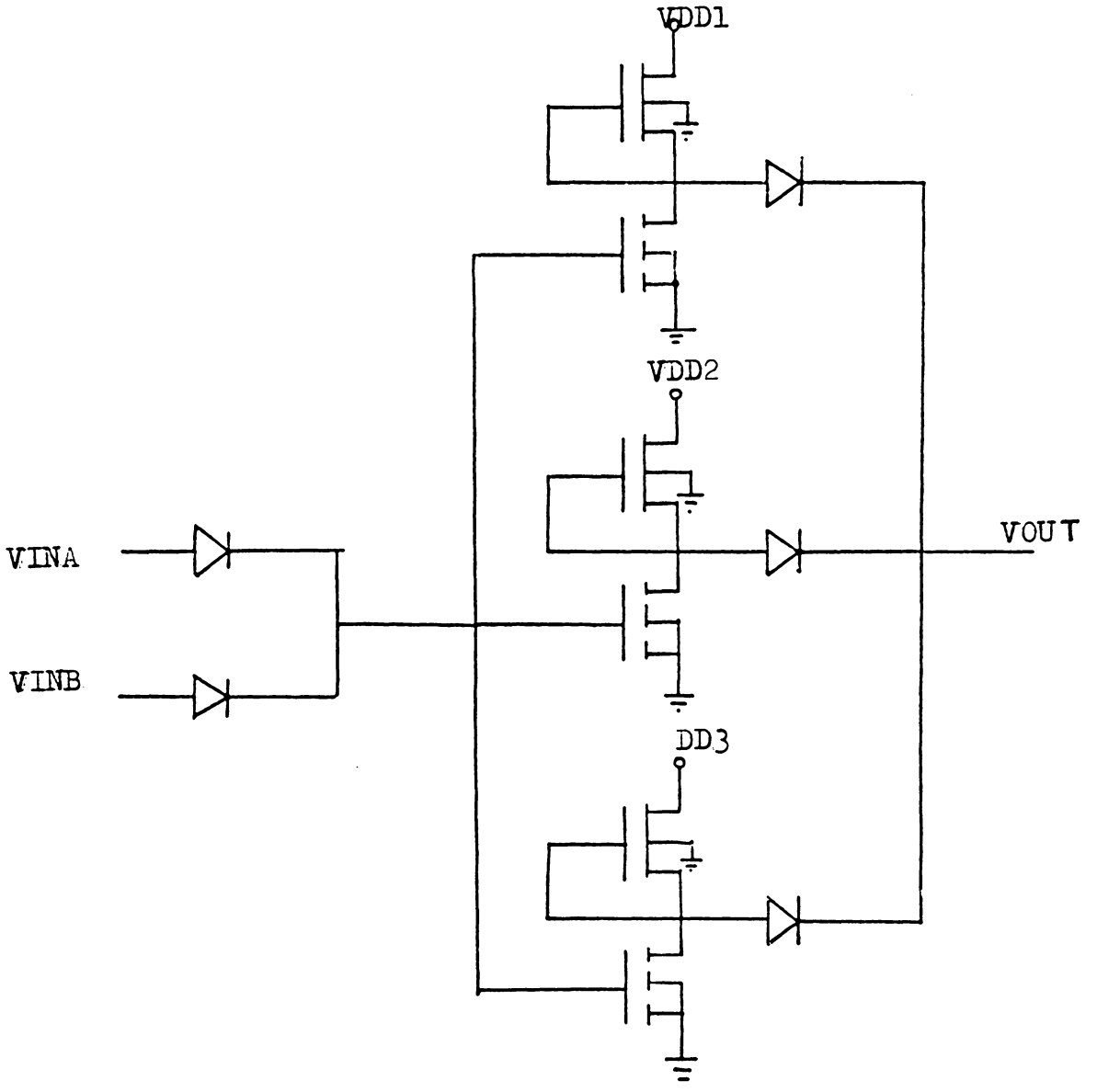

Figure 35: Circuit diagram of the $\overline{\text{MAX}}(A,B)$ gate.

Chapter VI

CONCLUSIONS AND AREAS FOR FURTHER RESEARCH.

This chapter aims at summing up the main aspects of the thesis. A comparison of the two ways of changing switching threshold is given and also included is a comparative study of binary and MVL read-only memory cell. Towards the end of the chapter, some directions for further research are outlined.

6.1 CONCLUSIONS.

It was stated that, with the nature of fabrication technology available these days it would be difficult to vary any single parameter of the device without getting possible processing tolerance errors. It is much easier to vary ratio of parameters in order to cancel any effects due to change in parameter values. But even this technique could fail to provide favourable results because the threshold voltage could still change and this will alter the value of switching threshold voltage. Therefore, it would certainly be more desirable that the threshold voltage rather than the transconductance be used to change the switching threshold.

Further, LSI technology has made rapid developments in the past years. It is very possible that future developments

will lead to very accurate fabricating processes. Under such circumstances it would be possible to consider changing switching voltages by changing the threshold voltage. Therefore, in future, it is possible that more powerful methods of changing switching threshold will be developed. This would provide a great impetus to the application of FETs in MVL circuits.

The ROM cell described in section 5.3 is an initial step towards implementing MVL memory elements using MOSFETs. In the cell described, 16 memory locations can be addressed, each location containing a 4-valued data bit. A binary cell with the same function would require 16, 2-bit words. This would give 16 addressable locations, each location containing one of four values. If a binary cell is assumed to be implemented using a single transistor (the most elementary form of ROM cell) then 32 transistors are used for both MVL as well as binary cells.

In the decoder section of the MVL cell there are eight literal gates comprising 8 transistors each, giving an overall count of 64 transistors. To address 16 locations for the binary case, a 4-to-16 decoder would be needed which can be implemented using sixteen four input AND gates, four inverters, and an OR gate. This would give a total count of 90 transistors. Therefore, MVL has a slight edge where the

number of transistors are concerned. But the main importance of the MVL cell would be realized by the fewer interconnection on the chip. In addition, the circuit complexity is reduced and as larger memory cells are configured the advantages of the MVL cell will be more pronounced.

6.2 AREAS FOR FURTHER RESEARCH.

The ROM cell described in section 5.3 can be extended to a programmable ROM. This would require that the user be able to select a value for the VDD for each pair in the memory block. This can be achieved by selecting the VDD through an array of switches, each switch providing contact to one supply voltage.

The Erasable-Programmable ROM marketed by INTEL corporation [23] is another area where MVL can be effectively realized. The memory cell has a transistor consisting of a buried or a floating gate. The charge on this gate determines the conductance of the channel. Erasure is achieved by energising the electrons on the floating gate by exposure to UV light. MVL behaviour can be obtained by changing the dimensions of the floating gate and thereby change the conductance of the channel. A detailed description of the floating gate transistor is given by Wada in [24], and by Kahng and Sze in [25].

Stark Moses, of INTEL Corporation, has introduced the idea of storing two bits per ROM cell using MOSFETs [26]. His approach is to manipulate the impedance of the channel and having sense circuits to know the amount current flowing through the device and thereby establishing the level inside the cell. This area could also be explored more in connection with using FETs in MVL.

In addition, MVL RAM design is another field where a good amount of work could be done. An efficient RAM would help in getting closer to realising the aim of building a complete MVL computer system

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Appendix A

MOSFET MODEL PARAMETERS

NAME	PARAMETER	DEFAULT	TYPICAL	UNITS
PHI	Surface Potential at Strong Inversion	0.6	0.65	V
PB	Bulk Junction Potential	0.8	0.87	V
JS	Bulk Junction Reverse Saturation Current Per M**2 of Junction Area.	1.0E-04	1.0E-04	A/M**2
NFS	Effective Fast Surface State Density	0.0	1.0E10	/CM**2
KF	Flicker Noise Coefficient	0.0	1.0E-26	
TPS	Type of Polysilicon: +1 (-1) for Opposite (Same) as Substrate.			
LD	Lateral Diffusion Coeff.	0.8	0.8	

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