Power Electronics Design Methodologies with Parametric and Model-Form Uncertainty Quantification

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(ABSTRACT)

Modeling and simulation have become fully ingrained into the set of design and development tools that are broadly used in the field of power electronics. To state simply, they represent the fastest and safest way to study a circuit or system, thus aiding in the research, design, diagnosis, and debugging phases of power converter development. Advances in computing technologies have also enabled the ability to conduct reliability and production yield analyses to ensure that the system performance can meet given requirements despite the presence of inevitable manufacturing variability and variations in the operating conditions. However, the trustworthiness of all the model-based design techniques depends entirely on the accuracy of the simulation models used, which, thus far, has not yet been fully considered. Prior to this research, heuristic safety factors were used to compensate for deviation of real system performance from the predictions made using modeling and simulation. This approach resulted invariably in a more conservative design process.

In this research, a modeling and design approach with parametric and model-form uncertainty quantification is formulated to bridge the modeling and simulation accuracy and reliance gaps that have hindered the full exploitation of model-based design techniques. Prior to this research, a few design approaches were developed to account for variability in the design process; these approaches have not shown the capability to be applicable to complex systems. This research, however, demonstrates that the implementation of the proposed modeling approach is able to handle complex power converters and systems. A systematic study for developing a simplified testbed for uncertainty quantification analysis is introduced accordingly. For illustrative purposes, the proposed modeling approach is applied to the swi
-tching model of a modular multilevel converter to improve the existing modeling practice and validate the model used in the design of this large-scale power converter.

The proposed modeling and design methodology is also extended to design optimization, where a robust multi-objective design and optimization approach with parametric and model-form uncertainty quantification is proposed. A sensitivity index is defined accordingly as a quantitative measure of system design robustness, with regards to manufacturing variability and modeling inaccuracies in the design of systems with multiple performance functions. The optimum design solution is realized by exploring the Pareto Front of the enhanced performance space, where the model-form error associated with each design is used to modify the estimated performance measures. The parametric sensitivity of each design point is also considered to discern between cases and help identify the most parametrically-robust of the Pareto-optimal design solutions.

To demonstrate the benefits of incorporating uncertainty quantification analysis into the design optimization from a more practical standpoint, a Vienna-type rectifier is used as a case study to compare the theoretical analysis with a comprehensive experimental validation. This research shows that the model-form error and sensitivity of each design point can potentially change the performance space and the resultant Pareto Front. As a result, ignoring these main sources of uncertainty in the design will result in incorrect decision-making and the choice of a design that is not an optimum design solution in practice.
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To my uncle

Dr. Mehdi Ashraf-Khorassani
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Chapter 1

Introduction

This chapter presents the motivations and objectives of this work. It introduces the background and the applications of modeling and simulation in power electronics. A review of the state-of-the-art model-based design and multi-objective optimization techniques for power electronic converters and systems is provided, with a focus on the design evaluation for product development. Challenges in the modeling and design optimization of power converters are discussed, followed by the scope of research and the dissertation outline.

1.1 Background

1.1.1 Power Electronics Modeling

Modeling and simulation are used throughout the power electronics field on a broad range of circuits and applications and have become fully ingrained into the set of design and development tools used daily by power electronics practitioners [49]. The method simply represents the fastest and safest way to study a circuit or system, aiding in the research, de-
sign, diagnosis, and debugging development phases of a power converter. As such, modeling and simulation play the most critical role in this burgeoning industry.

As the power processing capabilities of power electronics evolve, ever more complex power converters and systems are being developed with inherent behaviors and operating states that cannot be easily or confidently predicted. This scenario has further emphasized the design and simulation practice previously described in the first paragraph. The modular multilevel converter (MMC) is an example of a large-scale and complex system [2]; for the whole converter to function properly, tens or hundreds of thousands of individual circuits; including gate drivers, sensors, controllers, protection devices, and power processing modules must operate exactly as planned. In this case, isolating errors in the finished product can be very difficult. As a result, developers have become increasingly reliant on varied design and simulation software tools that allow them to simulate and monitor different subsystems under a variety of operating conditions. These tools also allow developers to conduct whole-system simulations that help them understand the converters operation and dynamics [27, 68, 75]. Without these software tools, the development of systems such as the MMC would be extremely challenging; perhaps impossible.

As opposed to simulation models in other technical fields, however, power converter simulation models are used simultaneously with laboratory prototypes, as simulation in and of itself has not been relied upon as a true substitute for experimental results [28]. Although in many cases testing a real-world system can be prohibitively expensive or sometimes impossible, simulations are either not utilized or results are not fully relied upon, so experiments are often carried out using scaled-down laboratory prototypes. A generator fault in a real power plant is an example of a very expensive, and nearly impossible, experiment to conduct [101]. Studying the stability of numerous grid-connected converters represents another challenging experiment, typically investigated by testing scaled-down system prototypes [97]. The ex-
1.1. Background

The content of this practice is such that, in some cases, full hardware replicas are built, e.g., in the development of electrical systems for space applications. Simulation is relegated accordingly and used to fine-tune the design of the control system and power stage, or to explore new phenomena arising from the hardware tests, thereby aiding overall in the risk mitigation strategy in place.

1.1.2 Model-Based Design Techniques

Advances in computing technologies over the past few decades have set the stage for a major step forward in modeling and simulation. Reduction in computation times in power circuit simulation, in particular, has made it practical to use simulation environments to conduct numerical design of experiments. This, in turn, has enabled reliability and production yield analyses to be conducted to ensure that the system performance can meet the given requirements in the presence of inevitable manufacturing variability, as well as variations in operating conditions [36, 91, 99].

In mass production, for instance, model-based design techniques, such as design for six sigma (DFSS) and worst-case analysis, along with hardware prototyping, have become necessary to evaluate the design robustness under extreme thermal and mechanical conditions, as well as variations in circuit component values and operating conditions. DFSS is the extension of the quality control technology called Six Sigma developed by Motorola and General Electric (GE) [69]. This methodology is an effective approach that addresses many of the problems that cause failures when a new product is launched in multiple industries. DFSS has become a robust design approach generally used to develop products that feature customer needs with very low defect levels [99, 102]. Monte Carlo simulation is the main step in these design techniques, which takes into consideration nearly all possible value com-
binations of the uncertain parameters. In worst-case analysis, on the other hand, statistical analysis is carried out by taking a certain number of different combinations of values of the parameters in question, an analysis that has become a crucial step in circuit design [23].

1.1.3 Multi-objective Design Optimization

The critical role of power electronics as an enabling technology has been realized over the past two decades, and significant effort has been dedicated to the development of road mapping in this field [8, 63, 88]. In these efforts, after an analysis of the state-of-the-art technology, a strategy is worked out to overcome technological barriers to achieve predetermined goals. A set of performance indices is defined accordingly, enabling the strategy to be implemented in a quantitative plan of action with measurable goals, e.g., cost, efficiency, reliability, weight, size, and power density.

The rising demand for improvement in the performance of power converters and systems has initiated a development trend toward design optimization. Early implementations of power converter optimizations were limited to optimization with respect to a single performance index [70, 96]. Nevertheless, almost every realistic design problem is multi-objective in nature, which involves simultaneous optimization of various conflicting performance functions as follows.

Given the constant demand for higher power density in many application areas, lower system volume provides a smaller surface for power dissipation which emphasizes the need for high-efficiency systems. As a result, the energy efficiency has become one of the most important performance measures in the design of power electronic converters. In the long term, the reliability of power electronic systems should be considered to comply with more stringent constraints on safety and availability in various applications. Cost is also a key
1.1. Background

performance measure to confirm the economic feasibility of the power electronic products [10]. Further, to ensure the market success of a new product, it should become available to the market in the right time frame, which makes time to market a critical measure to consider. Therefore, the performance of the system must be analyzed in a multi-dimensional performance space to realize the optimum solution among all possible feasible designs.

It is worth noting that physical, thermal, and electrical constraints for a feasible design should be defined according to the intended application area. The design of power converter systems is thus a multi-domain procedure too, which considers thermal and mechanical effects and limitations as well as electric and magnetic characteristics of active and passive power components.

The multi-objective optimization of power converters based on multi-dimensional performance space and the resultant Pareto Front is proposed in [39]. Pareto Front defines the boundary of the feasible performance space. This concept has been carried out in multi-objective design optimization (MDO) of power electronics converters to realize the performance limit relationship as well as determining the final optimum design point.

Furthermore, the effect of a change in the technology base of an improvement on the target performance is also realized through MDO. Therefore, optimization can be employed in the reverse direction to determine the most effective change in technology, i.e., to serve as the basis for a technology road-mapping process. Moreover, different system concepts, e.g., circuit topologies, control procedures, modulation schemes, etc. can be evaluated and directly compared with regards to achievable performance in the form of their associated Pareto Front [39].

Figure 1.1 illustrates the effects of the technology improvements on the achievable performance in the design optimization of power converters. The fundamental trends for the
development of power electronics converters are shown in Fig. 1.1a, indicating the achievable performance using the state-of-the-art technologies. As mentioned above, the performance indices considered in the design of power converters are mutually coupled, e.g., high power densities imply high frequencies, which potentially lead to a reduction in efficiency due to fundamental barriers and technology constraints. As a result, there is a constant demand for new semiconductor technologies, new circuit topologies, and modulation schemes, etc. to eliminate these barriers and provide new options for system optimization. These limits are realized through mathematical modeling and subsequent multi-objective optimization of converter systems. Figure 1.1b shows the performance trends over time. As technology improves and innovation occurs, there will be more options available in design optimization which will allow for all requirements to be met simultaneously (see Fig. 1.1c) [11].

1.2 Research Motivation and Objectives

Given that the accuracy of simulation results is typically not well-defined or is simply unknown, the role of modeling and simulation in power electronics has been more design-oriented. The trustworthiness of all the model-based design techniques, however, depends
1.2. Research Motivation and Objectives

entirely on the accuracy of the simulation models used, which has not yet been fully considered. In general, only viewgraph simulation and experimental waveforms are superimposed or compared side-by-side to determine the validity of a model. If the comparison is satisfactory from a qualitative standpoint, the designer is able to conduct other studies with the sole purpose of understanding or characterizing a physical phenomenon observed in the hardware prototype. As a result, pure simulation studies are, for the most part, limited to the initial stages of a design process, as any results obtained rely fully on the experience and knowledge of the designer. Heuristic safety factors are used to compensate for the uncertainties that are causing the possible deviation of real system performance from the predictions made using modeling and simulation [18]. This approach invariably results in a more conservative design process.

On the other hand, MDO is also a model-based approach that is susceptible to the shortcomings of current modeling and simulation practices. Despite the inevitable tolerance associated with different system parameters due to manufacturing variability as well as variations in the operating conditions, these sources of uncertainty have not been considered in the presented computation within MDO. Whereas, the impact of these tolerances could potentially change the performance space and the resultant Pareto Front. In a few cases, the effects of the component tolerances on the performance of the system are investigated after selecting the final design, e.g., in [9] the particular, the combination of component values that lead to the worst-case condition was determined to ensure feasibility of the selected design in the presence of manufacturing variability.

Also, in all previous works discussing MDO in power electronics, it is assumed that the mathematical models available for design optimization adequately model the system performance and tradeoffs of interest for the problem. However, this assumption is, in principle, not valid as no model is perfect. Modeling inaccuracy introduces an additional
source of variability in the design of power converters and systems.

Other disciplines have overcome the limitations in modeling and simulation described with the aid of formulated mathematical frameworks and procedures for the verification, validation, and uncertainty quantification (VV&UQ) of models [3, 65, 66]. A VV&UQ approach for power electronics converters was shown in [52, 72] to identify the most important steps that merit additional studies. To this end, this research has strived to formulate a modeling process with uncertainty quantification to bridge the modeling and simulation accuracy and reliance gaps. The absence of technique to bridge these gaps has hindered the full exploitation of model-based design techniques that ultimately pursue a reduced level of dependence on experimental results as well as an empowered role of modeling and simulation in the design and decision-making processes.

In general, there are two potential sources of uncertainty in model-based design techniques: parametric uncertainty (PU), which results from manufacturing variability, and model-form uncertainty (MFU), which results from the inherent inaccuracies of the models used. Although DFSS and worst-case analysis have accounted for PU as a means of improving the design process, MFU has not been considered thus far in product development.

Accordingly, a model-based design methodology with both PU and MFU quantification would represent a desirable alternative to the design of power electronics converters and systems, which is the main proposal of this research. This type of design approach would expectedly yield less conservative and more dependable designs. The proposed modeling framework in this approach can quantify the deviation of the real system performance from predictions made using modeling and simulation. This capability is attained by the proper identification, characterization, and quantification of the different, and often numerous sources of uncertainty. It should be noted that this technique does not require any additional resources other than those required for DFSS. Yet, the utilization of this tech-
nique will effectively eliminate the need for heuristic safety factors, yielding quantifiably more precise designs that are capable of truly maximizing the power processing capability of the devices at hand.

Modeling and design with uncertainty quantification is then extended to multi-objective design and optimization. In this research, a new approach for MDO with parametric and model-form uncertainty quantification (MDO with P&MF-UQ) is also proposed to include system design robustness considerations with regards to manufacturing variability and modeling inaccuracies in the design of power converters with multiple performance functions.

1.3 Dissertation Outline and Summary of Contributions

Accounting for the issues mentioned in the review of the existing literature on the modeling and design optimization of power electronics converters and systems, a new modeling approach is proposed in this dissertation, and a design optimization methodology with uncertainty quantification is developed, accordingly. The main aspects of the proposed modeling and design optimization approach will be addressed in this dissertation.

Chapter 2 presents an enhanced modeling framework for the design of power electronics converters and systems. This methodology provides the means to assess and quantify the predictive accuracy of power converter models, a capability that is attained by the proper identification, characterization, and quantification of the different, and often numerous, sources of uncertainty in the modeling and simulation process. For illustrative purposes, an in-depth example is presented using a power electronics building block (PEBB) as the modeling testbed. This example demonstrates how, through this formal modeling procedure
– and taking into consideration the uncertainties in the system – the model in question can predict the variable of interest within a known range with a given level of confidence, without requiring heuristic safety factors. This predicted range can be used as the required design margin when the selected output is a design variable, evincing the inherent potential of having a less conservative and more reliable power converter using the design methodology with uncertainty quantification.

Chapter 3 discusses the sensitivity analysis (SA) techniques. SA results are ultimately used to guide the modeling effort and minimize the number of uncertain parameters in estimating parametric uncertainty especially in the case of large-scale power electronics converters and systems. SA results also indicate which input uncertainties would most merit additional study in the uncertainty quantification (UQ) analysis. In this chapter, a review of the state-of-the-art techniques in the sensitivity analysis is provided, with a special focus on the numerical approaches, followed by the sensitivity analysis of an MMC. The switching model of an MMC is used as a case study to evaluate the techniques introduced in this chapter, where the sensitivity of two selected system response quantities (SRQs) to parametric uncertainties are studied. In this work, both local and global techniques are presented, and their advantages and drawbacks are discussed. A comparison is finally made between applied methods to identify the most efficient technique for SA of a complex power converter.

Chapter 4 discusses the main limitations in applying UQ analysis to large-scale power converters and systems. The MMC is used as a case study to demonstrates that the implementation of the proposed modeling approach in Chapter 2 can also handle complex power converters and systems. The enhanced modeling framework is then used to improve the modeling practice used in the design of an MMC. The effect of increasing the number of PEBBs in each arm on the estimated total uncertainty, and thus the predictive capability of the MMC simulation models for medium- and high-voltage applications is studied. A
1.3. Dissertation Outline and Summary of Contributions

Simulation model and a hardware prototype with up to two PEBBs per arm are used to estimate the uncertainty due to parameter variations and modeling inaccuracies in different model outputs. The result unveils an interesting feature of MMCs. Although the potential sources of uncertainty increase by adding more PEBBs in each arm, the total uncertainty associated with the final prediction remains the same or decreases, depending on the model output. A simplified testbed for UQ analysis of an MMC is developed accordingly. This simplified testbed is used to quantify the model-form uncertainty at multiple low power conditions and the results are used to build a regression model to predict the minimum required margin at the full-power condition. Therefore, any possible failures in the converter can be predicted ahead of time without any physical damages and the design can be improved in later iterations.

Chapter 5 proposes a multi-objective design and optimization technique with parametric and model-form uncertainty quantification (MDO with P&MF-UQ). A brief mathematical background of the MDO is provided followed by a complete mathematical formulation of MDO with P&MF-UQ. In this approach, a sensitivity index is formulated as a new performance measure which is defined as a quantitative measure of system design robustness in the presence of both parametric and model-form uncertainties. The sensitivity index would consequently provide a comprehensive design criterion to enable the selection of the most robust Pareto-optimal solution. Challenges for including systematic parametric and model-form uncertainty quantification analysis into the design and optimization process are also discussed.

Chapter 6 demonstrates the benefits of incorporating UQ analysis into the MDO from a more practical standpoint. The Vienna-type rectifier is used as a case study to compare the theoretical analysis with a comprehensive experimental validation. A thorough mathematical modeling and design optimization of the converter system and its components
concerning efficiency and power density within given size limitations and operational requirements (electromagnetic interference (EMI), power quality, temperature) are provided. MDO with built-in P&MF-UQ is then used to design a robust free-convection cooled Vienna-type rectifier with an input EMI filter. The final optimum design is realized by exploring the system Pareto Front of the enhanced performance space, where the model-form error associated with each design is used to modify the estimated performance measures, and parametric sensitivity of each design point is used to discern between cases and help identify the most parametrically-robust of the Pareto-optimal solutions. This research shows that the model-form error and sensitivity of each design point could potentially change the performance space and resultant Pareto Front for which the results of conventional MDO are illustrated as well. As a result, ignoring these main sources of uncertainty in the design will result in incorrect decision making and choosing a design that is not optimized in practice.

The last chapter summarizes the work and discusses the future works that could be undertaken to continue and enhance this research.
Chapter 2

Modeling and Design with Uncertainty Quantification

2.1 Introduction

There are two main sources of uncertainty associated with the outcome of any model-based design technique: parametric uncertainty (PU), which results from manufacturing variability, and model-form uncertainty (MFU), which results from the inherent inaccuracies of the models used [77]. In the past few decades, design for Six Sigma (DFSS) and worst-case analysis have accounted for PU as a means of improving the design process [23, 99]. Whereas, MFU has not been considered thus far in product development. The trustworthiness of all the model-based design techniques, however, depends entirely on the accuracy of the simulation models used, which has not yet been fully considered. Hence, heuristic design margins and safety factors are often used to compensate for the possible deviation of real system performance from the predictions made using modeling and simulation [18], resulting invariably in a more conservative design approach.
Accordingly, a model-based design methodology with both PU and MFU quantification would represent a desirable alternative to the design of power electronics converters and systems [56], which is the main proposal of this chapter. This type of design approach would expectedly yield less conservative and more dependable designs. To this end, the proposed modeling framework in this chapter quantifies the deviation of the real system performance from predictions made using modeling and simulation, a capability that is attained by the proper identification, characterization, and quantification of the different, and often numerous, sources of uncertainty. It should be noted that this technique does not require any additional resources other than those required for DFSS yet will effectively eliminate the need for heuristic design margins yielding quantifiably more precise designs capable of truly maximizing the power processing capability of the devices at hand.

The following sections will discuss in detail the implementation of this enhanced modeling framework. To this end, and with the intent to clearly illustrate the methodology developed, this chapter utilizes the modeling of a power electronics building block (PEBB) used in a modular power converter, assessing the capability of the model to predict the peak dc bus voltage and peak arm current of the PEBB, both variables that ultimately determine the voltage and current rating and stress of the PEBB. A 15 kW three-phase PEBB-based modular power converter hardware prototype and its corresponding switching model developed in Matlab-Simulink, are used for this purpose.

### 2.2 Enhanced Modeling Framework

Figure 2.1 displays an overview of the framework developed to implement the proposed modeling methodology, illustrating each of the steps in the process. These steps include planning and prioritization, modeling, verification, validation, uncertainty quantification,
2.2. Enhanced Modeling Framework

Figure 2.1: Modeling framework with parametric and model-form uncertainty quantification (P&MF-UQ).

and documentation. A key advantage of this inherently iterative framework is that the model is evaluated at each step, with updates applied as needed. From a power electronics perspective, the most relevant steps are validation and uncertainty quantification since they represent the main differentiator with respect to the present simulation practice. They also yield the results required to enable the prediction of variables of interest with known quantified uncertainty. More importantly, they formalize the modeling process, bridging
the simulation accuracy and reliance gaps that have hindered the full exploitation of this computer-aided design tool in the field. A detailed discussion of the required steps for completing this framework is provided in this section with the focus on validation and uncertainty quantification sections.

2.2.1 Planning and Prioritization

The purpose of the planning and prioritization step is to define the specifications and objectives of the design at hand. The planning aspect of the process is a set of routine questions which are necessary to answer before getting started and is summarized in the following steps [65]:

1. Specification description of the application of interest.

2. Specification of the application domain for the system.

3. Specification of the environments that the system could be exposed to.

4. Identification of important scenarios for each of the specified environments.

5. Specification of the system and its surroundings.

6. Specification of the system response quantities (SRQs) of interest.

7. Specification of product yield requirements for each SRQ of interest.

Prioritization, on the other hand, deals with the most important SRQs in the environment related to the phenomena under study. In this step, a table is generated, namely a phenomena identification and ranking table (PIRT), in order to prioritize the SRQs [1]; modular power converters and large power systems could accordingly make use of it to identify the SRQs needed for the study.
2.2.2 Modeling

The core of any design process is modeling. Given a very complicated system that has been developed, analyzing a system without a model is nearly impossible. Modeling seeks to answer the question of how to build the model of a given physical phenomenon, as well as to address how much to trust an existing model of the reality under study. This modeling step comprises two phases: first, building the conceptual model based on the information from planning and prioritization, and second, implementing or computerizing the conceptual model [67].

The resultant model is then subject to the verification and validation processes. If the models fail to be verified or validated, it must be updated as illustrated by the flow diagram in Fig. 2.1. In general, it is understood that using the simplest model of sufficient accuracy in the verification and validation processes will minimize the effort needed.

2.2.3 Verification

Since differential-equation-based models rarely yield exact solutions for practical problems, approximate numerical solutions must be used. Accordingly, there are a number of sources of uncertainty associated with these numerical approximations. These sources of uncertainty include round-off error, statistical sampling error, iterative error, discretization error, and simple coding mistakes [77]. As a result, the verification process is formulated to separately address solution verification and code verification.

Code verification is the process by which the use of consistent and convergent numerical algorithms is ensured when solving the mathematical model as well as ensuring that no coding mistakes are present in the software being used. Therefore, code verification requires a deep understanding of the software being used and, specifically, of its numerical engine.
The actual test is outside the scope of this research, but the reader is referred to [76] for a detailed description. Since software used in power electronics, such as MATLAB and Saber do not allow much control, the code, in this case, is assumed to have passed the order of accuracy test.

Solution verification addresses the uncertainties that occur due to numerical approximations. Since the governing differential equations are solved using Simulink (ode45 solver), the uncertainty due to the identified numerical approximations is assumed to be small in relation to the other relevant sources of uncertainty; this is typically the case when simulating power electronics converters and systems [1, 72]. In general, and regardless of the selected solver, running simulations using a finer grid reduces discretization error, which is typically considered as the main source of uncertainty due to numerical approximations. However, when lower computational cost is a criterion, running simulations using a coarser grid is required. In that case, the discretization error needs to be estimated using techniques discussed in [76].

Finally, as part of the verification process, any specific requirements laid out during the planning and prioritization stage need be checked to determine if the model is qualified. If the simulation results meet the code and solution requirements, then the model is verified and ready to go through the validation process. If not, either the computerized model or the conceptual model need to be updated.

2.2.4 Validation

The goal of validation is to assess the prediction capabilities of a model. This involves the quantitative comparison between simulation and experimental results obtained with the model in question and the respective hardware prototype. This comparison is not based
2.2. Enhanced Modeling Framework

on viewgraphs or some form of error calculation between waveforms as is often done when conducting circuit simulations. It requires extreme care since it is made between two nondeterministic values. Specifically, simulation and experimental results are nondeterministic due to the sources of uncertainty present, which arise due to the lack of knowledge in the system and inherent variations – such as manufacturing variability, measurement errors, and variations in boundary conditions. The main steps in the validation process are described hereinafter.

2.2.4.1 Experimental Results

Validation experiments require the experimental system to be well characterized in order to include all sources of uncertainty in the validation study and to prevent the under- or over-estimation of parametric uncertainties. Although, in essence, the validation process between the simulation and experimental counterparts should be blind [65], in power electronics, simulations and experiments are typically conducted by the same specialist, who should decide the model inputs and SRQs to be measured, while also determining the input parameters, the initial and boundary conditions, and estimating the uncertainty of the parameters in question.

There are always uncertainties associated with the experimental results obtained due to measurement errors. Therefore, it is recommended to have replicated experimental measurements of the desired SRQ to estimate the measurement uncertainty.

2.2.4.2 Simulation Results

The SRQs obtained through simulation are necessary to quantitatively assess the model accuracy and to estimate the PU, they are also the main purpose of the modeling and simula-
tion process. Due to the lack of knowledge in the system parameters (epistemic uncertainty), or inherent variations such as manufacturing variability, and variations in boundary conditions (aleatory uncertainty), the input parameters of the model, which are the simulation inputs, are usually nondeterministic. Accordingly, instead of a single deterministic simulation, an ensemble of simulations is needed to predict the uncertainty of the SRQ in question. The following steps provide guidance on how to perform this nondeterministic simulation:

1. Uncertainty Identification: all potential sources of uncertainties in the model input parameters should be identified. In addition, all aspects of the model, including the system parameters, should be classified either as deterministic or uncertain. Deterministic aspects are not taken into consideration any further.

2. Sensitivity Analysis: One important concept in the nondeterministic simulation is what is known as the curse of dimensionality, which refers to the increase in the number of samples needed as the number of uncertain parameters increases [16]. Specifically, sensitivity analysis reduces the input parameters to those that significantly affect the SRQ, so that those that do not have a big effect can be fixed at their nominal values and be excluded from the non-deterministic simulation. This concept, will be further discussed later in Chapter 3.

3. Uncertainty Characterization: This step classifies each uncertainty as epistemic, aleatory, or a mixture of aleatory and epistemic, assigning the corresponding mathematical structure to the parameters involved. The numerical values of all parameters in the resultant mathematical structures are then determined. In the case of an epistemic uncertainty, the parameter is characterized by an interval with determined upper and lower limits. If it is aleatory, the parameter is characterized by a cumulative distribution function (CDF) with its associated parameters.
4. Uncertainty Propagation: In this chapter, it is assumed that all model input uncertainties are aleatory, in which case Monte-Carlo (MC) sampling can be used to sample from the distributions of the model input parameters and runs numerous simulations to generate a sequence of SRQs [62].

2.2.4.3 Validation Metric

The ultimate goal of the validation process is to quantitatively assess the ability of the model to predict a well-characterized physical system or process. The validation metric is a methodology used to measure the disagreement between the simulation and experimental results, where different criteria can be used [65].

If only aleatory uncertainties (due to randomness) are present in the model inputs, then propagating these uncertainties through the model produces a CDF of the SRQ. Experimental measurements are then used to construct an empirical CDF of the SRQ. The enclosed region between these two CDFs is referred to as the area validation metric $d$ [77]. Equation (2.1) is used to calculate the area validation metric as follows:

\[
d(F, S_n) = \int_{-\infty}^{+\infty} |F(x) - S_n(x)|dx,
\]

where $x$ is the selected SRQ, $F(x)$ is the CDF from the simulation results, and $S_n(x)$ is the CDF from the experimental results, which is a function of the number of replicated measurements ($n$). It should be noted that the area validation metric represents an epistemic uncertainty since additional experiments and model improvements can be conducted to reduce it. This epistemic uncertainty is commonly referred to as MFU and has the same unit as the selected SRQ. Finally, $d$ is applied symmetrically to both sides of the CDF from simulation results, which tends to provide a conservative estimate of the MFU.
Figure 2.2: Modified area validation metric example.

An alternative type of validation metric is known as the modified area validation metric (MAVM), which separately tracks the regions between two CDFs. Specifically, where the experimental values are larger than the simulation values, it is referred to as $d^+$, and where the experimental values are smaller than the simulation values, as $d^-$ [90]. This is shown in Fig. 2.2.

In this case, the MFU is given by the following interval:

$$[F(x) - F_s d^-, F(x) + F_s d^+]$$

(2.2)

where $F_s$ is a factor of safety, which represents the most important advantage of MAVM as it accounts for the uncertainties resulting from measurement errors. Equation (2.3) has been adapted from [90] to calculate the desired safety factor, which is a function of the number of replicated experiments, $N_{exp}$, where additionally $F_1 = 1.25$, and $F_0 = 4$. 
2.2. Enhanced Modeling Framework

\( F_s(N_{exp}) = F_1 + \frac{1.2(F_0 - F_1)}{\sqrt{N_{exp}}} \) \hspace{1cm} (2.3)

As seen in (2.3), the number of replicated experimental measurements should be as high as possible to reduce the factor of safety and decrease the conservativeness of the validation metric. In addition to MFU, the MAVM also provides an estimate of model-form error (MF error), which can be calculated as below:

\[ \epsilon_{MF} = F_s d^- - F_s d^+ \] \hspace{1cm} (2.4)

2.2.5 Uncertainty Quantification (UQ)

The uncertainty quantification (UQ) step incorporates the concepts and results discussed in the previous sections into a simple framework to estimate the total uncertainty – mainly PU and MFU – in modeling and simulation. The framework for UQ is described below.

2.2.5.1 Parametric Uncertainty (PU) Estimation

After identifying the uncertainties, characterizing and propagating the model input uncertainty through the model with enough number of samples, the CDF of the SRQ of interest is assumed to be the best simulation result that reflects the model input uncertainty. The shape of the CDF depends on the uncertainty of the model inputs, which is also called PU.
2.2.5.2 Model-Form Uncertainty (MFU) Estimation

The calculated MAVM provides an estimate of the MFU. As noted above, the calculated MAVM uses the same units as the SRQ, which provides a quantitative comparison between the simulation and experimental results. The calculated $F_s d^+$ and $F_s d$ are applied to the right and left hand side of the CDF from the simulation results, respectively. This generates a probability box, aka p-box, without any probability or likelihood associated with the different locations within the p-box [4]; rather, it represents the family of all possible distributions that fit within its bounds.

2.2.5.3 Total Uncertainty Determination

The p-box displays all the possible sources of uncertainty in the scientific computing process. It should be noted that no probability distribution is associated within the p-box, as its shape is determined by aleatory uncertainty (PU), and its width is associated with epistemic uncertainty (MFU and uncertainty due to the numerical approximations).

Further, as mentioned previously, the MFU is epistemic; therefore, it can be represented by an interval with specified width. PU, on the other hand, is aleatory in nature, and as such, cannot be represented by an interval. To estimate the total uncertainty in the final prediction of the SRQ, an arbitrary interval-valued probability, e.g. a capability index of two-sigma (95 % level of confidence), should be selected. The SRQ is then expected to be within the upper and lower bounds, which are intervals themselves. In the end, the minimum value of the lower bound and the maximum value of the upper bound are selected to determine the final value of the estimated total uncertainty.
2.2.6 Model Updating

In general, the resultant p-box from the uncertainty quantification step may be large. Typically though, most of the uncertainties are epistemic, which means that more information about the components and system will help reduce it. This might lead to changing the assumptions used at the conceptual modeling stage, and also at the computational modeling stage, which are recommended and necessary steps to update the model in pursuit of a reduced total uncertainty. Additionally, a better characterization of the model input parameters during the validation experiment will also aid in reducing the resultant p-box.

2.3 Case Study: Power Electronics Building Block

This section presents the modeling of a PEBB to illustrate the enhanced modeling approach to be used in the design methodology with uncertainty quantification. The concept of PEBB as a universal power processor is the integration of fundamental components such as power devices, gate drives, minimum required passive components as well as control schemes [21, 22]. Figure 2.3 shows the circuit schematic of the silicon-carbide (SiC)-based PEBB in question, a power module potentially used in multiple applications in medium- and high voltage dc systems, ship power systems, and medium-voltage motor drives [35, 93]. In this chapter, the PEBB in question is part of a modular power converter for medium-voltage applications. The switching-level simulation is chosen as an example as it plays an important role in the converter design process and it is typically used to predict various aspects of the converter operation, including the estimation of voltage and current switching ripple, the sizing and design of energy storage and filter passive components, the prediction of its power quality, as well as its transient response, among others.
Chapter 2. Modeling and Design with Uncertainty Quantification

2.3.1 Planning and Prioritization

In this example, the system under consideration is shown in Fig. 2.4, which includes a three-phase modular inverter with its ac output filter, a dc power source, and an ac load. The operating environment is defined as normal, pertaining primarily to the ambient temperature used of 25 °C. The peak dc bus voltage and peak arm current of the PEBB are chosen as SRQs to avoid any unnecessary complexities in the formulation of the modeling approach. In this case, the model accuracy and credibility is assessed solely in the operating space where
2.3. Case Study: Power Electronics Building Block

Experimental data is available. However, using the same modeling approach, the calculated uncertainty can be extrapolated to a region where experimental data is not available. This enables the prediction of the SRQ in cases where the conduction of experiments could be impossible or very costly from an operational and/or financial standpoint.

2.3.2 Modeling

The switching model of the system under study is developed in MATLAB-Simulink. For the modulation scheme, a phase-shifted carrier modulation technique is used. As the PEBBs of this converter are modulated independently, the voltage balancing of the capacitors is achieved by adjusting the reference signal of each PEBB. A complete description of mathematical modeling, modulation implementation, and control scheme of the modular power converter used in this section is provided in Appendix A.

2.3.3 Validation

In the case of limited availability of hardware units, such as in this example, the measurement is limited to a single hardware unit. The experimental measurements are, therefore, not a fair representation of MC simulation results for estimating MFU. In such cases, the model input parameters should be measured directly from hardware and used in the simulation, so any difference between simulation and experimental results would be due to the model structure (i.e., MFU). The experimental setup used in the validation process comprises a three-phase modular inverter operating at 300 V dc bus, 76 V ac rms, 8 A rms, 60 Hz output frequency, and 100 kHz switching frequency, its ac output filter, and a three-phase resistive bank as the load in the setup. The complete description of the hardware setup in this example is provided in Appendix B. Figure 2.5 shows the experimental waveforms.
Chapter 2. Modeling and Design with Uncertainty Quantification

Figure 2.5: Multiple experimental waveforms: a PEBB dc bus voltage of upper arm $v_u$, an upper arm current $i_u$, a PEBB dc bus voltage of lower arm $v_l$, a lower arm current $i_l$, an ac (load) current $i_{ac}$, and a circulating current $i_{circ}$. SRQs of interest: a peak dc bus voltage $v_{pk_bus}$ and a peak arm current $i_{pk_arm}$.

Figure 2.6: CDFs of the PEBB (a) peak dc bus voltage and (b) peak arm current from simulation and experiment indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).
Using all available information, the values of the different hardware parameters and their tolerances were determined, i.e., the model input parameters (Table 2.1). The experimental setup is assumed to be well-characterized and, therefore, includes all possible sources of uncertainty in the validation process. The instrumentation used in the validation process should be as accurate as possible to decrease measurement errors. The uncertainty identified by the latter is mitigated, regardless of using the MAVM with its factor of safety, which
requires the use of as many as possible replicate measurements to achieve less uncertainty.

Figure 2.6 shows the superimposed CDF curves of the simulation and experimental results. In this figure, replicated experimental measurements are provided to take into account the measurement uncertainty. Similarly, using the measured input parameters of PEBBs, the CDF from simulation results was obtained, which is a single deterministic value. The resultant MFU for peak dc bus voltage and peak arm current of the PEBB is 20.11 V and 2.29 A.

The main advantage of this methodology is that even if some aspect of the actual hardware is missing in the model, it will be characterized as an epistemic uncertainty and will be included in the final result. Therefore, an incomplete model still results in a reliable modeling and simulation outcome with a larger interval as a penalty.

2.3.4 Uncertainty Quantification

The PU is estimated using nondeterministic simulations, while the MFU is estimated through validation, using a validation metric.

In this example, PU estimation is made only in the presence of aleatory uncertainties. Herein, the stratified MC sampling technique, also known as Latin hypercube sampling (LHS) [100], is preferred and used with 500 samples per parameter, propagating the uncertainties through the model when simulating the converter. Figures 2.7a and 2.7b show the CDF of the PEBB peak dc bus voltage and peak arm current obtained from this analysis.

It is important to note that although the input dc bus voltage and the ac load represent an epistemic uncertainty, these parameters were not considered as uncertain parameters in the analysis in question. For this analysis, they were fixed at their worst-case condition, given that higher dc voltage or higher load current will trigger the protection circuit; this
allows for focus on the design of the system with the given specification.

The calculated MAVM provides an estimate of the MFU. As noted previously, the calculated MAVM uses the same units as the SRQ, which provides a quantitative comparison between the simulation and experimental results. The calculated $F_{sd}^+$ and $F_{sd}^-$ are applied to the right and left-hand side of the CDF from the simulation results, respectively. As illustrated in Fig. 2.8, this generates a p-box.

To estimate the total uncertainty in the final prediction of the SRQ, an arbitrary interval-value probability, in this example, a capability index of two sigma (95% level of confidence) is selected. The final SRQ will therefore be within the blue-dashed line, and the total uncertainty is estimated as shown in Fig. 2.8a. Additionally, with a 95% probability, the CDF from any number of replicated experimental measurements will fall within the p-box, which will result in 308,000 PEVB units out of a million to have a peak dc bus voltage outside of this predicted range. To reduce the number of defects in new product development using the design methodology with PU and MFU quantification, a capability index of six sigma can be used in a given industry, which would result in only 3.4 defects per million. Following the same procedure, the final p-box of the peak arm current of the PEVB is generated and

![Figure 2.8: P-box of the PEVB (a) peak dc bus voltage and (b) peak arm current.](image)
shown in Fig. 2.8b.

2.3.5 Model Updating

As illustrated in Fig. 2.8, a significant portion of the total uncertainty in the system is epistemic, which is inherently due to the structure or form of the model. If knowledge is added to the modeling process, the total uncertainty and the width of the resultant p-box can be reduced. Regarding the model itself, the assumptions made during the modeling process can be reconsidered, which would lead to an updated structure and the opportunity to characterize the model input parameters in more detail. This would also aid in the uncertainty reduction effort, if desired.

2.4 Conclusion

In this chapter, a model-based design technique with uncertainty quantification for power electronics converters and systems was proposed. An enhanced modeling framework with parametric and model-from uncertainty quantification was identified and defined. An example addressing the modeling and design of a PEBB was then presented using the peak dc bus voltage and peak arm current of the PEBB as design variables, and thus, SRQs of interest in the modeling framework. The latter was then successfully applied to estimate the required margin in predicting the nominal voltage and current rating of the semiconductor devices of the PEBB. Specifically, it was shown how the model in question could predict the voltage and current to be within 307.4 – 336.4 V and 8.4 – 11.6 A, respectively. These predictions were made by taking into consideration the uncertainties of system parameters, model form, and measurements at two sigma capability index, evincing the inherent potential
of this methodology regarding the use of simulation results without heuristic safety factors in the product development.

Although the simulation output was predicted for an operating condition where experimental data was available, this approach is often used to predict the converter performance where there is no experimental data available, as the MFU can be calculated and extrapolated to such operating regions. Chapter 4 will address this specific topic, further supporting the use of this modeling and simulation framework.
Chapter 3

Sensitivity Analysis

3.1 Introduction

There is a distinction between models used to understand a law and models used to predict the behavior of a system given a presumably understood law [79]. The latter requires more precision, and the model used for designing a converter falls within this group. In the case of a large-scale system, developing such a model, that is capable of predicting the system behavior with an acceptable level of accuracy, poses additional challenges due to the large number of components that need to be modeled as well as their parameters required to be specified. The design specifications such as semiconductor voltage and current stress, output power, line-to-line voltage, maximum temperature and power quality in such systems are, accordingly, functions of many variables. These variables are associated with different types of uncertainties caused by a variety of factors, i.e. modeling errors, unknown modeling parameters, and manufacturing variabilities.

As discussed in Chapter 2, effects of the aforementioned uncertainties on the design
specifications need to be studied through a uncertainty quantification (UQ) analysis. Due to recent advances in computing power, parametric UQ (P-UQ) analyses have in fact become a critical step in the design of power electronics converters. In these analyses, the effect of parameter tolerances on system performance is estimated by carrying out nondeterministic simulations using Monte-Carlo (MC) sampling techniques.

One important concept in nondeterministic simulations is what is known as the curse of dimensionality, which refers to the increase in the number of samples needed as the number of uncertain parameters increases resulting in an increase in the number of model evaluations required in performing MC simulations. This, in effect, is the main limitation in applying UQ-based design techniques, such as the design with P&MF-UQ and DFSS, to large-scale power converters and systems. For instance, in the case of modular multilevel converter (MMC) for medium- and high-voltage applications [28] for which each arm consists of tens and hundreds of PEBBs connected in series or parallel, performing P-UQ analysis would become extremely expensive or nearly impossible in terms of computational costs. These costs are due to the considerable number of uncertain model input parameters such as those associated with semiconductor devices, dc-capacitor banks, arm inductors, etc.

Despite these limitations, the necessity of P-UQ analysis for a more robust and less conservative design cannot be disregarded. The resultant ranges from P-UQ analyses are valuable; they represent the component-to-component variability in a real system and changes in the operating conditions resulting in the requirement of design margins. In other words, the ranges from P-UQ analyses represent our knowledge or lack of it with regards to system parameters and its operating conditions. The results of these studies can be used to make informed design decisions and evaluate system performance in extreme thermal and electrical conditions in the presence of manufacturing variability.

To this end and with the intend to minimize computational costs, sensitivity analysis
is used to apportion the uncertainty of model output into different sources of uncertainty in the model input parameters which enables identifying critical parameters in a P-UQ analysis [78]. Sensitivity analysis is hence the key to reducing the uncertain parameters to those contributing the most to the uncertainty of the selected system response quantities (SRQs) under study. This analysis can serve several useful purposes in the economy of modeling, i.e., uncover technical errors in the model, identify critical regions in the space of the inputs, establish priorities for research, simplify models, and defend against falsifications of the analysis [79].

This chapter examines methods to calculate the sensitivity of a system output to parametric uncertainties using the MMC as an example of a large-scale power converter. In Section 3.2, sensitivity analysis methods are introduced. These methods are then applied to an MMC in Section 3.4 to determine the importance of MMC model input uncertainties in P-UQ analysis concerning two system outputs – namely peak dc bus voltage and peak arm current of PEBBs in an MMC. The results are finally used to minimize the number of uncertain parameters in predicting the effects of the tolerances on the system performance.

### 3.2 Sensitivity Analysis Techniques

Sensitivity analysis (SA) identifies the key parameters whose tolerances contribute the most to the uncertainty of the intended output. It will, in turn, instruct the analysts to the relative importance of the inputs in terms of determining the uncertainty associated with the selected output. There are various approaches for performing SA on numerical and analytical models. This chapter focuses on quantitative approaches.

SA techniques can be roughly classified into two main groups: global SA (GSA) and local SA (LSA) [78, 79]. This section presents a range of methods for performing sensitivity
analyses from both local and global techniques. In all methods presented in this section, uncertainty ranges, different in principle for each parameter, are the input for the analysis.

In the following, the model under investigation is described by a function that is \( y = f(x) \), where the input \( (x = [x_1, x_2, \ldots, x_n]) \) is a point inside an n-dimensional input space, and \( y \) is a scalar output.

### 3.2.1 Local Sensitivity

Local sensitivities provide a basic method to quickly calculate sensitivities. This form of SA, which is in the form of model output partial derivatives, is a straightforward implementation of the sensitivity concept. This measure tells how sensitive the output is to a perturbation of the input. This is customarily obtained by computing system derivatives such as,

\[
S_i = \left| \left( \frac{\partial y}{\partial x_i} \right)_{x_i=x^*} \right|,
\]

where \( x_i \) is the \( i^{th} \) input factor, \( S_i \) is the sensitivity measure of the \( x_i \), \( y \) is the output of interest, \( x^* \) is the vector of nominal values for input factors, and \( x_{-i} \) is the vector of all input factors except for the \( i^{th} \) factor. As shown in (3.1), in local sensitivity, one parameter is being examined at different points, and its effect is observed on a particular output, while the other parameter values are fixed at their nominal values.

If factors are uncertain within a known or hypothesized range, the sensitivity could then be multiplied by the associated uncertainty range. This corrects for cases where the uncertain slope is high, but the uncertain range is very small, resulting in a reduced effect on the output [29]. Furthermore, if a measure independent of the units used for \( x_i \) as well
as $y$ is needed, the equation below as the local sensitivity index can be used,

$$S_{x_i} = \left| \left( \frac{\sigma x_i^*}{y^*} \right) \cdot \left( \frac{\partial y}{\partial x_i} \right)_{x_i=x_i^*} \right|,$$

where $\sigma x_i$ is the standard deviation of the $x_i$ that is the uncertainty analysis input, in the sense that $\sigma x_i$ comes from the available knowledge of $x_i$, and $y^*$ is the value taken by $y$ when all input factors are fixed at their nominal value. Equation (3.2) gives us a fair measurement of an output sensitivity with respect to different model inputs. The percentage of the reduction in output uncertainty due to fixing parameter $x_i$ is finally calculated using the equation below:

$$P_{r_{x_i}} = \frac{S_{x_i}}{\sum_{k=1}^{n} S_{x_i}}$$

(3.3)

An obvious consequence of the local sensitivity is that the analyst will remain ignorant of the possible higher-order interaction effects on the uncertainty level of the model output. The other drawback to this approach is that it assumes that measured local sensitivity is indicative of the variation over the full range of uncertain inputs and that this variation is constant over the entire uncertain range. Overall, although the derivative-based approach has the advantage of being very efficient in terms of computing time, due to its mentioned inherent limitations, it is deficient when the model is nonlinear regarding the input/output relationship.
3.2 Sensitivity Analysis Techniques

3.2.2 Global Sensitivity

GSA overcomes the limitations of the local sensitivity approach discussed in the previous section. This method focuses on the output uncertainty over the entire range of values of the input parameters and unlike LSA does not specify the input to be $x = x^*$. Therefore, global sensitivity indices should be regarded as a tool for studying the mathematical model rather than its specified solution. A particular class of GSA techniques is explored in this section that is based on analysis of variance (ANOVA). Variance-based methods have a long history in sensitivity analysis. A comprehensive review of ANOVA-based SA techniques is presented in [34].

As more computing resources became available, ANOVA-based methods, as a form of the global sensitivity approach, have become popular. There are different options for variance-based methods [78]. In this work, the factor prioritization has been selected as the ultimate goal is to rank different parameters based on their contribution to the estimation of uncertainty associated with the final output. This method is based on calculation of the conditional variance of the model output by fixing certain parameter(s) on their nominal values. This approach is equivalent to calculating the expected reduction in the variance of the model output when these parameters are fixed at their nominal values. These conditional variances are usually obtained by averaging over the possible values of the fixed parameter(s).

The general ANOVA formulation for the calculation of the complete Sobol indices is provided in [85]. This section however focuses on two main metrics introduced by Sobol which are provided by the outcome of ANOVA analysis. These two metrics are the first-order index and the total index, which have been proven to be sufficient for studying the effect of parameters on output uncertainty when including not only first order effect but also the interaction between parameters [33].
3.2.2.1 First-Order Index

A variance-based first-order effect for an input factor can be written as

\[ V_{x_i} [E_{x_{-i}} (y|x_i)] , \]  

(3.4)

where the meaning of the inner expectation operator \(E_{x_{-i}}(.)\) in (3.4) is that the mean of \(y\) is taken over all possible values of \(x_{-i}\) while keeping \(x_i\) fixed. The outer variance \(V_{x_i}(.)\) is taken over all possible values of \(x_i\). In other words, (3.4) measures the expected reduction in the variance of output that would be obtained by fixing input factor \(x_i\) at its nominal value. The associated sensitivity measure, which is the first-order index \(S_i\), is calculated using the equation below:

\[ S_i = \frac{V_{x_i} [E_{x_{-i}} (y|x_i)]}{V(y)} , \]  

(3.5)

where \(V(y)\) is the variance of the output when all the input factors are changing.

As shown above \(V_{x_i} [E_{x_{-i}} (y|x_i)]\), the numerator of (3.5), measures the first-order (main) effect of \(x_i\) on the model output that is the fractional contribution of \(x_i\) to the \(V(y)\). In addition, due to the known identity:

\[ V_{x_i} [E_{x_{-i}} (y|x_i)] + E_{x_i} [V_{x_{-i}} (y|x_i)] = V(y) , \]  

(3.6)

\(E_{x_i} [V_{x_{-i}} (y|x_i)]\) is called the residual. Thus according to (3.6) and (3.5), \(S_i\) varies between zero and \(V(y)\) and is therefore a normalized index. The first-order index value is also equivalent to the expected percentage reduction in the variance due to main effects only.

As the first-order index of a parameter approaches zero, the relative parameter becomes
less important in determining the uncertainty of the output of interest and can be fixed at any given point within its range. As it approaches one, it becomes more important to include the parameter’s variation in the model. The first-order index is, therefore, a proper instrument to use for setting factor prioritization.

3.2.2.2 Total-Effect Index

The total effect metric ($S_{Ti}$) measures the contribution to the output variance from an input, including not only the main effect, but also any uncertainty caused by higher-order interactions between the given parameter and all other uncertain parameters. This is the primary metric of interest in UQ studies as it indicates fixing what input will provide the greatest reduction in output variance. This measure provides a more accurate measure of a parameters importance and can be calculated using the equation below

$$S_{Ti} = 1 - \frac{V_{X_{\sim i}}[E_{x_i}(y|x_{\sim i})]}{V(y)} = \frac{E_{x_{\sim i}}[V_{x_i}(y|x_{\sim i})]}{V(y)},$$

where the meaning of the variance operator ($V_{x_i}(.)$) is that the variance of $y$ is taken over all possible values of $x_i$ while keeping $x_{\sim i}$ fixed. The outer mean operator ($E_{x_{\sim i}}(.)$) is taken over all possible values of $x_{\sim i}$, and $S_{Ti}$ measures the total effect index of $x_i$, i.e., first and higher order effects (interactions) of factor $x_i$.

In (3.7), $E_{x_{\sim i}}[V_{x_i}(y|x_{\sim i})]$ is the expected variance that would be left if all factors but $x_i$ could be fixed. Accordingly and due to (3.6), $V_{x_{\sim i}}[E_{x_i}(y|x_{\sim i})]$ is the expected reduction in variance that would be obtained if $x_i$ could be fixed. One way to visualize this result is to consider that the term $V_{x_{\sim i}}[E_{x_i}(y|x_{\sim i})]/V(y)$ in (3.7) is the first order effect of $x_{\sim i}$. Therefore, $V(Y)$ minus this term must give the contribution of all terms in the variance decomposition which includes $x_i$. Finally, $S_{Ti}$ itself provides a measure of the percentage of the reduction in output uncertainty due to fixing parameter $x_i$. 

3.2.2.3 Monte Carlo (MC)-Based $S_i$ and $S_{Ti}$ Estimators

The main advantage of using (3.5) and (3.7) is their applicability to both non-orthogonal and orthogonal input spaces. To compute sensitivity indices using these formulas, the number of model evaluations strictly depends upon the number of uncertain parameters. Moreover, according to (3.5) and (3.7), two computation loops are required to calculate first- and total-effect indices. For instance, in (3.5), an inner MC loop is required to compute $E_{x_{\sim i}} (y|x_i)$ and an outer loop is required to apply the variance operator to obtain $V_{x_i} [E_{x_{\sim i}} (y|x_i)]$.

In the case of orthogonal input space, however, the computations could be much more accelerated. In this section, MC-based estimators are provided to compute both $S_i$ and $S_{Ti}$ for an orthogonal input space simultaneously without requiring a separate set of model evaluations for each index.

It is known that the equation below is preferred when calculating the variance:

$$V(y) = E(y^2) - E^2(y)$$

Using (3.8), the numerator in (3.5) can be rewritten as:

$$V_{x_i} [E_{x_{\sim i}} (y|x_i)] = \int E^2_{x_{\sim i}} (y|x_i) dx_i - (\int E_{x_{\sim i}} (y|x_i) dx_i)^2$$

The latter term in (3.9) is clearly $(E(y))^2 \equiv f_0^2$ and the former term can be written as:

$$\int E^2_{x_{\sim i}} (y|x_i) dx_i = \int \left( \int \cdots \int f(x_1, x_2, ..., x_i, ..., x_k) dx_{\sim i} dx'_{\sim i} \right) dx_i$$

$$= \int \cdots \int f(x_1, x_2, ..., x_i, ..., x_k) dx dx'_{\sim i},$$

(3.10)
where the derived term in (3.10) is the expected value of the function $f(x_1, x_2, ..., x_i, ..., x_k)$ $f(x'_1, x'_2, ..., x_i, ..., x'_k)$ over $2k - 1$ variables which are $x_i, x_2, ..., x_k, x'_1, x'_2, ..., x_i, ..., x'_k$. The integral in (3.10) can be calculated using MC simulation; it can therefore be described as a finite sum as below:

\[
\int E_{x_i}(y|x_i)dx_i = \frac{1}{N} \sum_{j=1}^{N} f(A)_j f(B_A)_j,
\]

where, $A$ and $B$ are two $K \times N$ independent sampling matrices; $K$ is the number of uncertain parameters and $N$ is the number of samples taken from each parameter; $a_{ij}$ and $b_{ij}$ are the elements of matrix $A$ and $B$, respectively. In matrix $A_B^{(i)} (B_A^{(i)})$ all the columns are from $A(B)$ except for the $i^{th}$ column which is from $B(A)$. As seen within the product $f(A)_j f(B_A^{(i)})_j$ the arguments $B$ and $A_B^{(i)}$ have in common the coordinate $x_i$ as in (3.10). Moving from $(B)_j$ to $(A_B^{(i)})_j$ is equivalent to a step along $x_\sim i$. Equivalent MC-based estimator for $S_i$ is therefore derived as below:

\[
S_i = \frac{1}{N} \sum_{j=1}^{N} f(A)_j f(B_A^{(i)})_j - f_0^2 V(y)
\]

Following the same procedure, similarly a MC-based estimator for $S_{Ti}$ is developed as below:

\[
S_{Ti} = 1 - \frac{1}{N} \sum_{j=1}^{N} f(A)_j f(A_B^{(i)})_j + f_0^2 V(y)
\]

As seen, to compute both $S_i$ and $S_{Ti}$ for the $k$ input factors the triplet matrices $A, B, B_A^{(i)}$ or $B, A, A_B^{(i)}$ are required. Several approaches have been proposed based on the MC-estimator to further minimize the computational cost by improving the convergence rate. Alternative formulas proposed by Jansen [80] have proved to be the most efficient approaches for estimating $S_i$ and $S_{Ti}$ with minimum errors compared to other methods [33, 85]. The calculation
efficiency is further improved when quasi-random sampling technique, also known as Sobol sampling, is used which imposes the minimum required samples relative to other MC sampling approaches. Matrices $A$ and $B$ are hence generated from a quasi-random sequence of size $N \times 2K$. As a result, the points of matrix $A$, and hence $A_B^{(i)}$ are better distributed than the points of $B$ and $B_A^{(i)}$. This is due to the algorithm used in Sobol sampling. The method based on $A,A_B^{(i)}$ is therefore often superior to $B,B_A^{(i)}$ and it is used in this work.

Finally, alternative formulas known as Jansen estimators for $S_i$ and $S_{Ti}$ are used in this works and are given as below.

\[
S_i = \frac{V(y) - \frac{1}{2N} \sum_{j=1}^{N} f(B)_{j} f(A_B^{(i)})_{j}}{V(y)} \quad (3.14)
\]

\[
S_{Ti} = \frac{\frac{1}{2N} \sum_{j=1}^{N} (f(A)_{j} - f(A_B^{(i)})_{j})^2}{V(y)} \quad (3.15)
\]
3.3 Case Study: Modular Multilevel Converter (MMC)

The MMC has become a preferred choice for medium-voltage applications as it has several advantages when compared with two-level voltage source converters [17, 44, 45]. Advantages of the MMC such as excellent harmonic performance, distributed energy storage, and near ideal current and voltage scalability also make this converter the most promising converter technology for high-voltage direct-current (HVDC) transmission systems [7, 30, 46, 84]. Power cells in an MMC – a full-bridge or half-bridge circuit – can be configured as a PEBB. PEBB as a concept to construct modular converters, was originally proposed by Office of Naval Research in 1997. Over the past two decades, PEBB-based modular converters have gained increased attention due to their minimal maintenance cost, easy assembly and production [21, 35, 93].

Figure 3.1: Circuit configuration of the modular multilevel converter (MMC).
Figure 3.1 shows the circuit configuration of a three-phase PEBB-based MMC. Each phase of the converter consists of two arms, the upper and the lower. Each arm comprises a large number of series-connected PEBBs. In this chapter, as shown in Fig. 3.1, the PEBB is configured as a full-bridge, not the conventional half-bridge, due to its several advantages such as four-quadrant operation, fault handling capability, and small impact when a fewer PEBBs are used in each arm in medium-voltage applications, as opposed to hundreds in the HVDC applications.

Several aspects of MMCs such as modulation implementation, control algorithm, and component selection require crucial insight and understanding of converter’s operation and dynamics. At early design stages modeling and simulation, as a set of design and development tools, provide valuable perspectives on these topics. Further on in the process and prior to mass production, the converter design also needs to be ensured via model-based reliability and production yield analysis where UQ analysis is performed. MMC models thus need to be developed based on their application whether they are used to understand the MMC principle and fine-tune design of controllers, or whether they are intended to be used to predict the MMC’s design specifications. For the latter purpose, a more detailed model is required. The detailed model should take into account the distribution or range of parameters that are critical in predicting the intended design specification. To this end, SA is required to determine the most important model input parameters that need to be specified accurately in predicting the intended MMC design specification in the context of UQ analysis.

In this work, high switching frequency high power SiC-based PEBBs are used which has shown to be a promising replacement of conventional Si IBGT-based PEBBs for implementing MMCs [35, 93]. This is mainly due the recent advancements in the development of SiC MOSFET with low switching losses and high switching speed that enable high switching frequency, which improves the overall power density of the PEBB [59]. This would however
raise concern regarding safe operation of the device. In this chapter, peak dc bus voltage and peak arm current of the PEBB are selected as the intended SRQs as they are the two main variables in determining the peak voltage and current stress of the device in MMCs to ensure the safe operation of semiconductor devices.

### 3.4 SA Results and Discussion

This section examines the use of sensitivity studies by LSA and GSA in determining the most influential uncertain model input parameters in the UQ analysis of an MMC. The peak dc bus voltage and peak arm current of the PEBB are selected as the intended SRQs. SA is performed on the switching model of an MMC developed in MATLAB-simulink (See Appendix A). In this scenario, MMC with two PEBBs per arm is selected to investigate the possible interaction among PEBBs in each arm. A three-phase ac resistive load and an ac filter are connected to the ac side of this converter. The input dc source, feeding the converter, is connected to the dc side. Table 3.1 summarizes the system specifications and Fig. 3.2 shows the time-domain simulation results.

This section also focuses on the uncertainties due to manufacturing variability. The uncertain parameters in this example are the same as those described in Chapter 2 (See

<table>
<thead>
<tr>
<th>Table 3.1: System specification.</th>
</tr>
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<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Rated power [kW]</td>
</tr>
<tr>
<td>DC-bus voltage [V]</td>
</tr>
<tr>
<td>Load current [A]</td>
</tr>
<tr>
<td>Switching frequency [kHz]</td>
</tr>
</tbody>
</table>
Since the operating principles in all three phases are identical and independent from each other, both global and local analyses were performed on phase $A$, and similar results are expected from the two other phases. Additionally, in complex systems such as MMCs,
which can be presented in a hierarchical structure, the sensitivity analysis could also be carried out at different levels, including sub-system (PEBB) and system levels. Based on PEBB-level analysis, non-influential parameters are accordingly fixed at their nominal values when performing system-level analysis.

To eliminate any possible sampling error in the calculated first-order and total indices, GSA is performed with different sample sizes to ensure the calculated index has converged to its final value. Figures 3.3, 3.4, 3.5, and 3.6 show computed PEBB-level first-order and total indices of uncertain parameters for the peak dc bus voltage and peak arm current with different sample sizes, i.e. \{10, 50, 100, 500, 1000, 5000, 10000, 20000\}. First-order and total indices of PEBB parameters in the case of dc bus voltage are almost the same; this indicates that for this specific SRQ there is no higher order interaction between PEBB parameters. However, in the case of peak arm current, these two sensitivity indices are not the same for all parameters and higher order interaction appears to be significant for dc capacitance \(C\), dc capacitor equivalent series resistance (ESR) \(R_C\), arm inductance \(L_{arm}\), arm inductor ESR \(R_{Larm}\), and drain-source on-state resistance of MOSFET \(R_{on}\).

Similar studies were conducted for MMC without a circulating current controller, and results are summarized in Table 3.2. Once the circulating current controller is disabled, the main effect of the arm inductor on the peak arm current increases significantly which indicates that in addition to the discussed benefits brought by circulating current controller and its necessity in Appendix A, it also helps decrease the sensitivity of the system to parameters variations.

At system-level analysis, all the parameters with a total index lower than 0.1 from PEBB level analysis are fixed at their nominal values and the rest remain as uncertain variables. Figures 3.7, 3.8, 3.9, and 3.10 show computed system-level first-order and total indices of the uncertain parameters regarding the PEBB peak dc bus voltage and peak arm current.
Table 3.2: First-order and total effects of PEBB uncertain parameters on the PEBB peak arm current with and without circulating current controller.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$S_i$</th>
<th></th>
<th>$S_T$</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>w circ</td>
<td>wo circ</td>
<td>w circ</td>
<td>wo circ</td>
</tr>
<tr>
<td>DC capacitance</td>
<td>0.83</td>
<td>0.55</td>
<td>0.99</td>
<td>0.74</td>
</tr>
<tr>
<td>DC capacitor ESR</td>
<td>0</td>
<td>0</td>
<td>0.12</td>
<td>0.10</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>0</td>
<td>0.27</td>
<td>0.16</td>
<td>0.43</td>
</tr>
<tr>
<td>Arm inductor ESR</td>
<td>0</td>
<td>0</td>
<td>0.10</td>
<td>0.10</td>
</tr>
<tr>
<td>MOSFET on-state resistance</td>
<td>0</td>
<td>0</td>
<td>0.13</td>
<td>0.13</td>
</tr>
</tbody>
</table>

with different sample sizes, i.e. \{10, 50, 100, 200, 2000, 4000\}. First-order and total indices of MMC parameters in the case of dc bus voltage are almost the same. However, in the case of peak arm current, higher order interaction appears to be significant dc capacitance ($C$) and ac inductance ($L_{ac}$).

According to SA of the MMC, the only critical input parameter for UQ analysis of a PEBB peak dc bus voltage is its dc capacitance value; the rest of the parameters could be fixed at their nominal values. Whereas for peak arm current, in addition to the ac inductor, all the dc capacitance values of the PEBBs in the same phase leg are equally important and should be included in the UQ analysis.

LSA is also performed in this example. Table 3.3 summarizes both local and global SA results. For this particular example, the results appear to be qualitatively similar; the methods agree on which of the parameters the system response is most sensitive to. However, only the total index for each parameter provides an accurate estimate of the expected uncertainty reduction in the SRQ, if the parameter could be fixed. This is due to the fact
that LSA and first-order effect both fail to identify the higher-order effects as expected. In certain situations, these differences could lead to significant errors in the sensitivities.

On the other hand, the computational costs in terms of the number of required model evaluations for LSA is $2^K$, whereas for GSA is $N(K + 2)$ where $N$ and $K$ are the minimum required number of MC samples and number of uncertain parameters, respectively. It is worth noting that the minimum required samples ($N$) vary depending on the selected sampling algorithm and the number of uncertain parameters in the study.

To summarize, the SA method used must be chosen carefully with consideration given to the assumptions made in each model. The first factor that should be taken into account is the nonlinearity of the model. In cases where the system can be safely treated as linear, LSA results can be used. In cases where the system is nonlinear, or the linearity is not clear, then GSA must be conducted. If the system under study has a low number of uncertainties, then first-order and total-effect indices could be used to estimate the overall sensitivity.

Estimating both indices will also identify the available interaction between parameters. In cases with a huge number of uncertain parameters, performing SA analysis in a hierarchical manner helps reduce the computational cost. In addition, initial studies can be performed using LSA or other lower-cost, but less-accurate, global sensitivity analysis such as scatter plot analysis [29]. Later on, more intense studies that utilize more accurate algorithms can be conducted to estimate uncertainty reduction percentage for the key parameters.
Figure 3.3: Subsystem-level GSA results for peak dc bus voltage: first-order index estimates versus the number of samples in the MC simulation with seven uncertain inputs.
Figure 3.4: Subsystem-level GSA results for peak dc bus voltage: total index estimates versus the number of samples in the MC simulation with seven uncertain inputs.
Figure 3.5: Subsystem-level GSA results for peak arm current: first-order index estimates versus the number of samples in the MC simulation with seven uncertain inputs.
Figure 3.6: Subsystem-level GSA results for peak arm current: total index estimates versus the number of samples in the MC simulation with seven uncertain inputs.
Figure 3.7: System-level GSA results for peak dc bus voltage: first-order index estimates versus the number of samples in the MC simulation with six uncertain inputs.

Figure 3.8: System-level GSA results for peak dc bus voltage: total index estimates versus the number of samples in the MC simulation with six uncertain inputs.
Figure 3.9: System-level GSA results for peak arm current: first-order index estimates versus the number of samples in the MC simulation with twenty-two uncertain inputs.
Figure 3.10: System-level GSA results for peak arm current: total index estimates versus the number of samples in the MC simulation with twenty-two uncertain inputs.
### Table 3.3: Summary of sensitivity analysis results for peak dc bus voltage (SRQ$_1$) and peak arm current (SRQ$_2$).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SRQ$_1$</th>
<th></th>
<th>SRQ$_2$</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{i}$</td>
<td>$S_{i}$</td>
<td>$S_{Ti}$</td>
<td>$P_{i}$</td>
</tr>
<tr>
<td>Arm inductance, $L_{arm}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.16</td>
</tr>
<tr>
<td>Arm parasitic resistance, $R_{arm}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.06</td>
</tr>
<tr>
<td>dc-link capacitance, $C_{dc}$</td>
<td>0.99</td>
<td>0.99</td>
<td>1</td>
<td>0.73</td>
</tr>
<tr>
<td>dc-link parasitic resistance, $R_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.02</td>
</tr>
<tr>
<td>MOSFET on resistance, $R_{ds}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.05</td>
</tr>
<tr>
<td>Diode forward voltage, $V_f$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Diode on resistance, $R_d$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>System level</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PEBB1 Arm inductance, $L_{arm}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.04</td>
</tr>
<tr>
<td>PEBB1 dc-link capacitance, $C_{dc}$</td>
<td>0.85</td>
<td>0.99</td>
<td>0.99</td>
<td>0.19</td>
</tr>
<tr>
<td>PEBB2 Arm inductance, $L_{arm}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.04</td>
</tr>
<tr>
<td>PEBB2 dc-link capacitance, $C_{dc}$</td>
<td>0.04</td>
<td>0</td>
<td>0</td>
<td>0.17</td>
</tr>
<tr>
<td>PEBB3 Arm inductance, $L_{arm}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.05</td>
</tr>
<tr>
<td>PEBB3 dc-link capacitance, $C_{dc}$</td>
<td>0.03</td>
<td>0</td>
<td>0</td>
<td>0.17</td>
</tr>
<tr>
<td>PEBB4 Arm inductance, $L_{arm}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.06</td>
</tr>
<tr>
<td>PEBB4 dc-link capacitance, $C_{dc}$</td>
<td>0.03</td>
<td>0</td>
<td>0</td>
<td>0.21</td>
</tr>
<tr>
<td>AC inductance, $L_{ac}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.24</td>
</tr>
</tbody>
</table>
3.5 Conclusion

In this chapter, sensitivity analysis was presented to guide the modeling effort and minimize the number of uncertain parameters in estimating PU, particularly in the case of large-scale power electronics converters and systems. Furthermore, SA results indicated which input uncertainties would most merit additional study in the UQ analysis. In this work, methods from both local and global approaches were presented and their advantages and drawbacks were discussed. The switching model of an MMC was used as a case study to evaluate the techniques discussed in this chapter, where the sensitivity of two selected SRQs to parametric uncertainties was studied. It was also shown that performing SA in a hierarchical manner could help reduce the computational costs of the GSA significantly for large-scale power converters.

As shown in this chapter, in the case of the MMC and for certain SRQs, the number of key uncertain parameters is a function of the number of PEBBs in each arm of an MMC. As a result, as more PEBBs are added in the arm of an MMC, P-UQ analysis become computationally more expensive and ultimately impossible to conduct; alternative approaches for UQ analysis of complex power converters is further discussed in Chapter 4.

Finally, a comparison was made between applied methods to identify the most efficient technique for sensitivity analysis of a complex power converter. It was shown that, although GSA has significantly higher computational costs, for nonlinear systems with a manageable number of uncertainties, in particular, GSA is recommended over LSA due to the trustworthiness of its results regardless of the type of model under study.
Chapter 4

Regression-Based Uncertainty Quantification Analysis

4.1 Introduction

As discussed in Chapter 2, design with P&MF-UQ aims at quantifying all sources of uncertainty in the modeling and simulation of a power converter for which experimental results for MF-UQ and nondeterministic simulation results for P-UQ are obtained. For large-scale power converters and systems, however, estimating PU and MFU requires a significant computational effort and hardware prototyping. As a result, UQ analysis, as a key step in the design with P&MF-UQ, could potentially apply limitations concerning feasibility; these limitations are briefly discussed in the following.

There are two main factors affecting the computational cost of a nondeterministic simulation: the number of model evaluations required and the fidelity of the model. As discussed in Chapter 3, the first factor is a function of the number of uncertain model input parameters
where SA results are used to minimize the number of uncertain parameters and the number of required model evaluation accordingly. The latter, however, depends on the level of accuracy required in the context where the model is used. As the required accuracy increases, higher fidelity models would be of more interest resulting in higher computational costs. As an example, in the switching model of an MMC for medium-voltage drives or HVDC applications [13, 28], there are tens to thousands of PEBBs connected in series; as more PEBBs are added in each arm, the computational cost per model evaluation increases significantly due to the huge number of PEBBs that are modeled, thereby increasing the overall computation cost per model evaluation. This increase is in addition to the increase in the number of required model evaluations, discussed earlier in Chapter 3, leading to another challenge in P-UQ.

In comparison, with regards to MF-UQ, when it comes to large-scale power converters and systems, testing the complete converter at its rated power could be prohibitively expensive, or sometimes impossible at the early design stage due to safety considerations or physical constraints (equipment, facilities, etc.). Experiments are often carried out using scaled-down laboratory prototypes to complete the modeling effort. For instance, to measure the accuracy of the MMC model, MF-UQ requires conducting a full power validation experiment on the hardware prototype of the MMC with the actual number of the PEBBs. Whereas, the hardware prototype with a limited number of power modules is usually available at early design stages to run low-power validation experiments [28]. As a result, MF-UQ at the full-rated power lacks experimental results.

In this chapter, MMC as an example of a large-scale system is used to present a systematic study for developing a simplified testbed for UQ analysis. In Section 4.2, the enhanced modeling framework is used to explore the effects of adding more series-connected PEBBs per arm on the design of the MMC concerning two main design variables – namely peak dc
bus voltage and peak arm current of the PEBB. A simplified testbed is derived accordingly for conducting MC simulations and low-power validation experiments to estimate PU and MFU, respectively. This simplified testbed enables validating certain aspects of the design with less computational cost and hardware prototyping. In Section 4.3, low-power validation experiments with a limited operating area, combined with modeling and simulation are finally used to predict the actual behavior of the converter at its full-rated power, where the MFU is extrapolated using a regression-based MFU predictor. Section 4.4 provides concluding remarks.

4.2 Simplified Validation Testbed

The ultimate goal of this section is to improve the existing modeling practice used in the design of an MMC by using the P&MF-UQ approach. Due to several challenges of validating an MMC model used in the design of this converter, this section investigates the possibility of validating a PEBB model instead. This would be done so that the corresponding model, with the gained confidence in its simulation results, can be used in the design of the MMC.

In order to develop a simplified testbed for model validation of PEBB in the design of an MMC, the relationship between total uncertainty associated with the SRQs of interest and the number of PEBBs per arm needs to be investigated [55, 57]. To this end, the effects of adding more PEBBs per arm on the PU and MFU associated with SRQs are studied separately.
4.2.1 Parametric Uncertainty

The PU of the selected SRQs is estimated for three cases where the number of PEBBs per arm increases incrementally. The modulation implementation and control system are presented in Appendix A. All the model input parameters that are subject to variability are identified as the uncertain input parameters. These uncertainties are mainly due to the manufacturing tolerance, and natural material variability. A mathematical structure is then assigned to each of these uncertain parameters based on the type of uncertainty. In this case, the uncertain parameters are characterized by a normal distribution with a specific mean and standard deviation which is equal to the nominal value and one-third of the tolerance of each uncertain input parameter, respectively. Table 2.1 summarizes the circuit parameters for the MC simulations.

According to SA results from Chapter 3, the uncertain input parameters are first reduced to those whose tolerances contribute the most to the PU of the SRQs of interest, and those that do not have a big effect are fixed at their nominal values. In addition, as three phases of the MMC are independent of one another, the PU of the peak dc bus voltage and the peak arm current of each PEBB can be estimated by propagating only the model input uncertainties of the PEBBs in the same phase. The parameters of the other two phases can be fixed at their nominal values, resulting in a significant reduction of the number of uncertain parameters. As all input uncertainties are classified as aleatory, Latin Hypercube sampling (LHS) [100] is used to sample from the distributions of the model input parameters to generate a sequence of SRQs.

Figure 4.1 shows the resultant CDF of the peak dc-bus voltage and peak arm current of one of the PEBBs in the phase-leg of an MMC. It should be noted that due to the current ripple reduction as a result of having more PEBBs in each arm, the nominal peak arm
current decreases as more PEBBs are connected in series. The resultant CDF of the peak arm current for all cases is therefore normalized with respect to its mean nominal value for each case.

As shown in Fig. 4.1a, the peak dc-bus voltage of any PEBB is independent of the number of series-connected PEBBs in each arm. When there is peak arm current, however, as shown in Fig. 4.1b, the distribution will be affected as more PEBBs are connected in series.

A two-sigma capability index is finally used to demonstrate the PU in the peak dc bus voltage of the PEBB and the peak arm current. Table 4.3 summarizes the corresponding PU for each of the cases with a 95 % level of confidence. This result unveils an interesting feature of the MMC; the PU of the peak arm current will decrease as more PEBBs are added in series to scale up the voltage for different applications. The PU of the peak dc bus voltage of each PEBB, on the other hand, remains the same.
4.2.2 Model-Form Uncertainty

As the three phase-legs in an MMC are fully decoupled, the validation experiment can be conducted on a half-bridge based on the MMC. Due to the limited number of PEBBs available, scaled-down validation experiments are conducted for two cases: a phase-leg with one PEBB per arm, and a phase-leg with two PEBBs per arm. Figure 4.2 shows the system configuration used for validation experiments. In the validation experiment set-up, for both cases, a second phase-leg (PEBB 5 and PEBB 6 in Fig. 4.2) is used for the midpoint connection. The modulation implementation and control system is the same as the one presented in Appendix A. Tables 4.1 and 4.2 summarize the circuit parameters and phase-leg specifications for the down-scaled validation experiments. The experiments were carried out under the condition of 180V-1kW and 360V-2kW for phase-leg with one and two PEBBs per arm, respectively. Figures 4.3a and 4.3b show the experimental waveforms indicating the SRQs.

Figure 4.2: Experimental circuit for: (a) Case 1: 1 PEBB/arm and, (b) Case 2: 2 PEBBs/arm.
Figure 4.3: Multiple experimental waveforms of the phase-leg with (a) 1 PEBB per arm and (b) 2 PEBBs per arm: A PEBB dc bus voltage of upper arm $v_u$, an upper arm current $i_u$, a PEBB dc bus voltage of lower arm $v_l$, a lower arm current $i_l$, an ac (load) current $i_{ac}$, and a circulating current $i_{circ}$. SRQs of interest: A peak dc bus voltage $v_{pk\_bus}$ and a peak arm current $i_{pk\_arm}$. 
In this case, the experimental measurements are limited to a single hardware unit for each of the cases shown in Fig. 4.2. Although the replicated experimental measurements are provided to take into account the uncertainty due to measurement errors, the empirical CDF is not representing the CDF from simulation results shown in Fig. 4.1. A proper replication of the CDF shown in Fig. 4.1 requires multiple experimental units available. Therefore, a single simulation using the measured value of all parameters of the PEBBs is used to calculate the MFU. Figure 4.4 shows the CDF from simulation and experiment representing the peak dc bus voltage of the PEBB (PEBB 1), and the peak arm current (upper arm) for both cases. The enclosed region between each pair of CDFs from simulation and experiment is then estimated where $d^-$ and $d^+$ are calculated separately.

Table 4.3 summarizes the estimated MFU associated with the predictive capability of the model in predicting the PEBB peak dc bus voltage and peak arm current as evidenced by the validation assessment on the available data for both cases. The MFU of the peak dc bus voltage of the PEBB is the same for both cases. However, the MFU of the peak arm current decreases when the number of PEBBs in each arm is increased to two.

![Figure 4.4: CDFs of the PEBB (a) peak dc bus voltage and (b) peak arm current from simulation and experiment.](image-url)
### 4.2. Simplified Validation Testbed

Table 4.1: PEBB specification.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-bus voltage [V]</td>
<td>180</td>
</tr>
<tr>
<td>Arm current [A]</td>
<td>5.7</td>
</tr>
<tr>
<td>Arm inductance [mH]</td>
<td>1</td>
</tr>
<tr>
<td>DC capacitance [µF]</td>
<td>210</td>
</tr>
<tr>
<td>Switching frequency [kHz]</td>
<td>100</td>
</tr>
</tbody>
</table>

Table 4.2: Phase-leg specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of PEBB(s) per arm</td>
<td>1</td>
</tr>
<tr>
<td>Load apparent power [W]</td>
<td>1000</td>
</tr>
<tr>
<td>DC link voltage [V]</td>
<td>180</td>
</tr>
<tr>
<td>Line frequency [Hz]</td>
<td>60</td>
</tr>
<tr>
<td>AC line current [A]</td>
<td>10</td>
</tr>
<tr>
<td>AC inductance [mH]</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Table 4.3: Calculated parametric and model-form uncertainties for two cases: Case 1 is 1 PEBB per arm, and Case 2 is 2 PEBBs per arm.

<table>
<thead>
<tr>
<th>SRQ</th>
<th>PU</th>
<th>MFU</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Case 1</td>
<td>Case 2</td>
</tr>
<tr>
<td>$v_{up1}$ [V]</td>
<td>8.4</td>
<td>8.4</td>
</tr>
<tr>
<td>$i_{up}$ [A]</td>
<td>1.6</td>
<td>1.3</td>
</tr>
</tbody>
</table>
4.2.3 Total Uncertainty and Discussion

The sum of the estimated MFU and PU, based on the two-sigma capability index, is the total uncertainty in modeling and simulation of the MMC with a 95% level of confidence. The total uncertainty is the expected amount of variation in the system performance from predictions made from modeling and simulation results. Figure 4.5 shows the total uncertainty associated with the predictive capability of the model in predicting the PEBB peak dc bus voltage and peak arm current.

As shown in Fig. 4.5, the PU and MFU for peak dc bus voltage of each PEBB is the same for both cases studied in this work. The total uncertainty associated with the final prediction of this SRQ is thus independent of the number of series-connected PEBB in each arm of the MMC. Therefore, the estimated range for a phase leg with one PEBB per arm could be used as the estimated uncertainty for the case of a three-phase MMC with more PEBBs per arm.

However, when there is peak arm current, the PU and MFU will be affected as more PEBBs are connected in series. A regression-based model could be developed to predict the

![Figure 4.5: Total uncertainty associated with the final prediction of: (a) maximum dc capacitor voltage of the PEBB, and (b) peak arm current.](image-url)
PU of the MMC with more PEBBs per arm. On the other hand, the estimated PU of the peak arm current of a single phase-leg with one PEBB per arm can be used as the upper bound for the final prediction of this SRQ in other cases that have more series-connected PEBBs.

Based on the analysis given in this section, in the design of MMC, having more PEBBs in each arm does not necessarily require a greater margin for the selected design variables of interest. A single phase-leg with one PEBB per arm can therefore be used as a simplified testbed for model validation in the design of an MMC without adding any further uncertainties in the modeling and simulation. Accordingly, the heuristic safety factors in the design of MMC can be replaced by the estimated total uncertainty at the full-rated power for the selected design variables using the simplified testbed. This may result in further minimizing the design margins and improvements, while the safe operation of the converter is ensured via the gained confidence in the predictive proficiency of MMC simulation models.

4.3 Regression-Based Design Margin Estimation

In a design with P&MF-UQ, the minimum required design margin is determined based on the estimated total uncertainty at the full-rated power of a power converter or system. Consider a case where testing the PEBBs developed for simplified testbed at their full-rated power is not possible. PU can still be estimated using MC simulation at the full-power condition using a simplified testbed. Whereas, estimating the MFU is limited to a narrow operating range; and the comparison between simulation and experimental results at full-rated power lacks the actual experimental results. In this case, since the application domain is outside of the validation domain, an extrapolation procedure must be used using a regression model for MFU estimation in the application domain [53]. Finally, MFU is based directly on
what has been observed in the prediction performance of the model at low-power validation experiments.

4.3.1 Design of Experiments

An essential step in developing a regression model is data collection where a design of experiments (DOE) can be used. DOE is a systematic approach for collecting data used in statistical analysis; some of the designs are full factorial, fractional factorial, central composite, one factor, etc. [60].

The validity of the predictions made outside of validation domain depends on the quality of the conducted DOE. In this work, full factorial DOE with two factors is applied to evaluate the interaction effect among factors as well as their individual main effect on the accuracy of the model. The first factor is the input dc voltage and the second one is the load rms current. These two are the primary means of changing the power level of validation experiments. Each factor has four levels, where $v_{in,dc} = \{150, 200, 250, 300\}$ [V] and $i_{L,rms} = \{3.4, 4.2, 5.7, 8.4\}$ [A]; thus the total number of sixteen treatment combinations are studied in this section.

The hardware prototype described in Appendix B is configured as an MMC with one PEBB per arm. Validation experiments are conducted on the simplified testbed developed in the previous section at a total number of sixteen different operating points. Fig 4.6 shows the operational waveforms under different operating conditions with 300 V dc input voltage, similar waveforms are captured for other twelve cases as well.
Figure 4.6: Experimental waveforms of the conducted DOE at 300 V dc bus voltage: a PEBB dc bus voltage of upper arm $v_u$, an upper arm current $i_u$, a PEBB dc bus voltage of lower arm $v_l$, a lower arm current $i_l$, an ac (load) current $i_{ac}$, and a circulating current $i_{circ}$. SRQs of interest: A peak dc bus voltage $v_{pk,us}$ and a peak arm current $i_{pk,arm}$.
4.3.2 Model-Form Uncertainty Quantification

In this section, the modeling accuracy is evaluated at sixteen different operating points. At each operating condition, the MFU of the peak dc bus voltage and peak arm current of PEBB is calculated using the twenty-four measured data and simulation results. Figures 4.7 and 4.8 show the superimposed CDF curves of peak dc bus voltage and peak arm current from the simulation and experimental results for operating conditions with 300V dc input voltage. Following the same approach, $d^+$ and $d^-$ of the peak dc bus voltage and peak arm current are calculated for rest of the operating conditions using the measured data and simulation results.

4.3.3 Model-Form Error Prediction

The next step is to develop a model that makes MFU predictions for any possible operating condition. The MFUs calculated in the previous section then need to be extrapolated to the full-power condition using the developed predictive model. The predicted MFU is hence based directly on what has been observed in the prediction performance of the model at low-power validation experiments.

It should be noted, as discussed in Chapter 2, that estimating MFU requires multiple hardware replicates. In this specific example and due to the lack of hardware replicates, MF error is used for evaluating modeling accuracy. Therefore, extrapolated MF error at full-power condition will be later used to generate the final p-box. In the case of multiple hardware units, however, $d^-$ and $d^+$ should be extrapolated separately and used to generate the final P-box.
Figure 4.7: CDFs of PEBB 1 peak dc bus voltage from simulation and experiment under different operating conditions at 300 V dc bus voltage indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).
Figure 4.8: CDFs of PEBB 1 peak arm current from simulation and experiment under different operating conditions at 300 V dc bus voltage indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).
In this section, two different approaches are used for developing a regression-based predictive model: multiple linear regression and Gaussian Process regression (Appendix C). Each method is discussed in the following.

4.3.3.1 Multiple Linear Regression

Multiple linear regression is perhaps one of the most commonly used and relatively easy-to-build models among various parametric methods that have been developed for predictive modeling [61]. In this model, dependent variables are expressed as a function of the predictor variables. In this section, the calculated MF errors are regressed against the input voltage and load current. The method of least squares is then used to estimate the regression coefficients so that the sum of the squares of the differences between the observations and the straight line, known as the residuals, is minimized.

The major assumptions that are implicitly made in linear regression analysis are as follow:

- the residuals are normally distributed,
- the residuals have zero mean,
- the residuals have constant variance,
- the residuals are uncorrelated.

These are the basic requirements in a regression analysis to ensure regression model adequacy. The validity of these assumptions, however, need to be considered. If any of these assumptions are violated, the linear regression model is not valid to be used for making predictions.
In this work, data transformation is used to modify the regression model built to have an error term normally and independently distributed with mean zero and constant variance. The resulting regression models for peak dc bus voltage and peak arm current are shown below:

\[
MFU_V(v_{in}, i_L) = 0.078 - 0.0001 v_{in} - 0.002 i_L \tag{4.1}
\]

\[
MFU_I(v_{in}, i_L) = -\frac{42.88}{v_{in}} + \frac{0.90}{i_L} + 203.9 \left( \frac{1}{v_{in}} - 0.004 \right) \left( \frac{1}{i_L} - 0.20 \right) \tag{4.2}
\]

Figure 4.9 shows the estimated MF error associated with peak dc bus voltage and peak arm current using the developed MLR model against the dc input voltage and load rms current. The 95 % prediction interval (PI) for the value of the area metric at the regulatory conditions is also depicted.

Figure 4.9: Mean of the estimated MF error (blue plane) using MLR and its 95 % PI (yellow planes) as a function of load rms current and dc input voltage for (a) peak dc bus voltage and (b) peak arm current; red points indicate the training data points.
The experimental result at a higher power is obtained to evaluate the predictive capability of the regression model. If the measured MFU falls within the predicted range, MLR model is validated to be sufficiently accurate for making predictions at higher power conditions. The predicted range for MF error of peak dc bus voltage and peak arm current at $P = 13$ kW using 4.1 and 4.2 is $-6.92 \% \sim 4.90\%$ and $-5.04 \% \sim 8.24\%$. The calculated MF error of these SRQs from the actual measurements at this operating point is $4.21\%$ for voltage and $1.21\%$ for current, which are within the predicted range for peak dc bus voltage and peak arm current, respectively.

Finally, using the regression-based model, the estimated MFU at full-rated power, i.e. $1$ kV dc bus voltage and $12.8$ A rms load current is $-27.22 \% \sim 11.61\%$ and $1.6 \% \sim 18.36\%$ for peak dc bus voltage and peak arm current, respectively.

### 4.3.3.2 Gaussian Process Regression

Gaussian Process (GP) regression is a simple nonparametric nonlinear regression tool which is widely used in various application areas; it is an alternative for parametric regression tools [73]. This method gives a prior probability to every possible function, where higher probabilities are given to functions that are considered to be more likely. This prior distribution is then conditioned on the training dataset and a posterior distribution is finally derived over all possible functions. A complete discussion on GP regression tools is provided in Appendix C; following the same procedure, a GP regression is developed for peak dc bus voltage and peak arm current using the sixteen training data points, i.e. sixteen estimated model-form uncertainties. Equation (4.3) denotes the GP regression model specified by its mean and covariance functions that are $m(x)$ and $k(x, x')$, respectively.
\begin{equation}
MFU(x) \sim GP(m(x), k(x, x')),
\end{equation}

where $x$ is the vector of operating conditions at which the MFU needs to be estimated, $x'$ is the vector of training dataset that is the operating conditions at which MFU is available. The covariance function specifies the covariance between pairs of outputs as a function of the inputs. Among possible options for the covariance function, squared exponential covariance function is selected due to the smooth function behavior that is expected for the MF error over different operating conditions. The associated hyper parameters with the covariance function are calculated using maximum likelihood.

The training dataset, in this case, is considered to be noisy due to inevitable measurement errors. As a result, the error bound would not be zero at the training data points but has a minimum value. Moving away from the training data points, the error bound increases. More training data points are thus required to reduce the error bound associated with the estimated MF errors.

GP finally defines a posterior distribution over all possible functions conditioned on the training dataset. A 95% prediction interval is selected to calculate an error bound for the predicted MFUs. Fig 4.10 shows the mean response of the estimated MFU associated with peak dc bus voltage and peak arm current against the dc input voltage and load rms current using the developed GP model, where the 95% prediction interval for the value of the area metric at the regulatory conditions is also shown.

Similar to MLR, the predicted range for MF error of peak dc bus voltage and peak arm current at $P = 13$ kW is estimated to be $1.77\% \sim 6.57\%$ and $-31.23\% \sim 15.02\%$ which encompass the MF errors from actual measurements. Finally, using the GP regression model, the MFU at full-rated power, i.e. 1000 V dc bus voltage and 12.8 A rms load current
Figure 4.10: Mean of the estimated MF error (blue plane) using GP and its 95 \% PI (yellow planes) as a function of load rms current and dc input voltage for (a) peak dc bus voltage and (b) peak arm current; red points indicate the training data points.

would be 1.65 \% \sim 6.49 \% and -42.97 \% \sim 30.05 \% for peak dc bus voltage and peak arm current, respectively.

4.3.4 Final Design Margin

To estimate the final design margin, the upper bound from the prediction intervals using GP at 1000 V dc input voltage and 12.8 A rms load current is used as the estimated MF error. Figure 4.11 shows the prediction distribution, representing the input uncertainty, with a parallel distribution displaced by the predicted MF error at full-power condition. The p-box represents a reasonable estimate of the combined input and model-form uncertainty associated with the predictive capability of the model as evidenced by the validation assessment on the available data at low-power condition. The interval-valued probability of 95 \% is finally used to demonstrate the total uncertainty in the peak dc-bus voltage and peak arm current. Specifically, the model in question predicts the voltage and current to be within 1050 V \sim 1077 V and 17.2 A \sim 25.1 A, respectively, by taking into consideration the uncertainties of
system parameters, model form, and measurements, at two sigma capability index, evincing the inherent potential of using this predicted range as a design margin without requiring heuristic safety factors.

4.4 Conclusion

In this chapter, the enhanced modeling framework with parametric and model-form uncertainty quantification was used to improve the existing modeling practice and to validate the model used in the design of an MMC as an example of a complex power converter. To this end, the main limitations in applying UQ-based design techniques to large-scale power converters and systems in general was discussed. The effect of increasing the number of PEBBs in each arm on the estimated total uncertainty, and thus the predictive capability of the MMC simulation models for medium- and high-voltage applications was then investigated. A simulation model and a hardware prototype with up to two PEBBs per arm were used accordingly to estimate the uncertainty due to parameter variations and modeling
4.4. Conclusion

inaccuracies in different model outputs – namely the peak dc bus voltage and the peak arm current of PEBB. The result reveals an interesting feature of MMCs: although the potential sources of uncertainty increase by adding more PEBBs in each arm, the total uncertainty associated with the final prediction remains the same or decreases, depending on the model output.

Accordingly, a simplified testbed for UQ analysis and model validation of the PEBB in the design of an MMC was developed. This simplified testbed was used to conduct MC simulation to estimate PU. It was also used to conduct scaled-down validation experiments to quantify the MFU at multiple low power conditions; these results were used to build a regression model and ultimately predict the minimum required margin at the full-power condition. Therefore, any possible failures in the converter is predicted ahead of time without any physical damages and the design can be improved in later iterations. Following the same strategy, a simplified testbed for model validation of any other complex power system can be investigated for use in UQ-based design approaches without introducing any further uncertainties in the modeling and simulation.
Chapter 5

Design Optimization with Uncertainty Quantification

5.1 Introduction

A multi-objective design and optimization (MDO) approach in the field of power electronics was first developed within the framework of a road-mapping initiative that the European Center for Power Electronics (ECPE) started in 2003 [40]; since then, this approach has been applied for the realization of ultra-compact ultra-efficient power converters [9, 39, 70, 94, 95, 96].

Despite the inevitable tolerance associated with different system parameters, as well as variations in the operating conditions, uncertainties have not been considered in the presented computations within the MDO. As a result, their effect on the performance space and the resultant Pareto Front has been neglected. The impact of these uncertainties on the predicted system performance measures, however, could potentially change the performance
space and the resultant Pareto Front. In a few cases, the effects of the component tolerance on system performance are investigated after selecting the final design; e.g., the particular combination of component values that lead to the worst-case condition is determined to ensure feasibility of the selected design in the presence of manufacturing variability [9].

Also, in all previous works discussing MDO in power electronics, it is assumed that the mathematical models available for design optimization adequately model the system performance and make tradeoffs in interest for the problem. However, this assumption is, in principle, not valid because no model is perfect. Modeling inaccuracy introduces an additional source of variability in the design of power converters and systems. Therefore, depending on the accuracy of the model for the selected design, actual performance of the final converter could vary from the predicted performance ascertained using MDO approach.

This chapter proposes a new method for MDO with parametric and model-form uncertainty quantification (MDO with P&MF-UQ) that includes robustness considerations with regards to manufacturing variability as well as modeling inaccuracies in the design of power converters with multiple performance functions. Challenges for including systematic P&MF-UQ analysis into the design and optimization process are also discussed.

This chapter is organized as follows. Section 5.2 provides a brief mathematical background of the MDO, in which the design process in general and the subsequent evaluation of the systems are first illustrated and shown in abstract form as the mathematical mapping of a design space into a system performance space. Following, the multi-objective optimization of this mapping is discussed. In Section 5.3, the general system design flow is modified to incorporate UQ analysis into the optimization framework. Section 5.4 develops a new performance vector indicating design robustness. Section 5.5 develops the proposed optimization formulations with P&MF-UQ and discusses some practical implementation difficulties. Section 5.5 provides concluding remarks.
Chapter 5. Design Optimization with Uncertainty Quantification

5.2 Multi-Objective Design Optimization (MDO)

Circuit topology, modulation scheme, control parameters, magnetic core type, and core size are a few examples of the many design variables present in the design of power electronic systems and converters. Design variables are a group of system parameters in the design of power converters which are determined by designers. These variables are selected based on the available library and within given lower and upper bounds (for continuous variables) or from a limited number of options (for discrete design variables). Each design variable is then assigned a coordinate axis forming an $n$-dimensional design space where $n$ is the number of design variables.

Generally, in the design of power converters and systems, for each point in the design space, the behavioral model is run based on the given system specifications. All required information for the design of components, i.e., voltage and current waveforms, are extracted from simulation results, and appropriate passive and active devices, magnetic components, wires, etc. are selected accordingly. Besides design variables, the rest of the system parameters need to be determined such that side conditions defined by system specification or

Figure 5.1: Representation of the multi-objective design and optimization (MDO): mapping a multi-dimensional design space into a multi-dimensional performance space to determine the Pareto Front.
a minimum performance requirement are fulfilled. These parameters are called non-design system parameters; they are not directly controlled by the designer and are a function of system specifications and design parameters. These parameters are realized through the system design flow for each design iteration to ensure system functionality and operational requirements.

According to the specified design criteria, required component models are also developed to predict the intended system behavior and selected performance measures. Performance measures (e.g., efficiency, size, cost, weight, etc.) are the indices that need to be maximized or minimized (depending on the MDO formulation) through a design process. These objectives are a function of design variables as well as non-design system parameters. Each performance
index is then assigned a coordinate axis forming an $m$-dimensional performance space where $m$ is the number of performance indices.

By calculating all desired performance indices for a point in the design space through the general system design flow, the corresponding design can be represented with a point in the $m$-dimensional performance space. This procedure is iterated until all combinations of design variables (all the points in the design space) are swept with corresponding side conditions to ensure feasibility of the designs in the performance space.

Hence, overall, the $n$-dimensional design space is mapped into the $m$-dimensional performance space (see Fig. 5.1); a general system design flow in the design of power converters is shown in Fig. 5.2, which includes a behavioral model of the power converter, component library, and component models. A switching model, for instance, is a behavioral model, as all information for selecting each component can be extracted from its simulation results. Loss, size, and cost models, on the other hand, are examples of component models, which are developed to predict the intended performance measures.

A typical mathematical formulation for mapping the design space into a performance space in the multi-objective design can be given as follows:

$$\mathbf{x} \rightarrow \mathbf{J}(\mathbf{x}, \mathbf{p})$$

(5.1)

where $\mathbf{x}$ is the vector of design variables ($\mathbf{x} = [x_1, x_2, ..., x_n]$), $\mathbf{p}$ is the vector of non-design system parameters ($\mathbf{p} = [p_1, p_2, ..., p_m]$), $\mathbf{J}$ is the vector of primary performance indices ($\mathbf{J} = [J_1, J_2, ..., J_k]$), and $n$, $m$, and $k$ are the number of design variables, non-design system parameters and performance indices, respectively.

Within the scope of design optimization, the final step is to find the optimum design solution that maximizes the performance vector ($\mathbf{J}(\mathbf{x}, \mathbf{p})$) while satisfying constraints. A
5.2. Multi-Objective Design Optimization (MDO)

A typical mathematical formulation of the MDO can be written as follows:

\[
\text{max } J(x, p, )
\]

\[\text{such that (s.t.) } g(x, p) \leq 0,\]

\[h(x, p) = 0, \text{ and}\]

\[x_{LB} \leq x \leq x_{UB},\]

where \(x_{LB}\) and \(x_{UB}\) are the vector of lower and upper bounds for the vector of design variables, respectively. Functions \(g(\cdot, \cdot)\) and \(h(\cdot, \cdot)\) are side conditions describing the inner converter function, the system requirements or specifications, and minimum required values of other performance indices to ensure feasibility of the designs.

The optimum design solution is finally realized by exploring the Pareto Front that is the boundary of the feasible performance space. Many approaches have been studied to construct the Pareto Front [37]. Among these studies, the weighted sum [50], goal programming [12], constraint-based methods [51], and genetic algorithm [14] are more popular; these methods are briefly discussed in the following.

The weighted sum method assigns weights for each objective (performance function) based on the relative preferences among objectives and combines the multiple objectives into a single objective. The Pareto Front is then achieved by trying different weights for the individual objectives and performing the optimization multiple times. The goal programming approach treats each objective through an equivalent constraint and introduces detrimental deviations for each of the goals. The objective is to minimize the weighted sum of the detrimental deviations. In constraint-based methods, one of the objective functions is selected as the only objective, and the remaining objective functions are treated as con-
Chapter 5. Design Optimization with Uncertainty Quantification

The Pareto Front can be obtained by systematically varying the constraint bounds. Similarly, multiple optimizations need to be implemented. The genetic algorithm-based approach globally searches for feasible solutions, compares and ranks them based on objectives and constraints, and selects the non-dominated solutions.

As described, the first three approaches convert the multi-objective optimization problem into a single objective problem to be solved with optimization algorithms. These approaches are therefore more efficient compared to the genetic algorithm, but are more likely to result in suboptimal solutions, especially in high-dimensional performance spaces. In contrast, in genetic algorithms the entire Pareto set is obtained using multi-objective genetic algorithms, which will always result in a global optimum solution but also requires more function evaluations. The optimization algorithm must hence be selected based on the problem setting.

Due to the limited number of objectives in this work, the weighted sum approach is used. The Pareto Front is realized using the following algorithm:

\[
\sum w_i J_i(x, p) \rightarrow Max; \quad \sum w_i = 1,
\]

where \(w_i\) is the weighting factor for the \(i^{th}\) performance index. The maximum performance vector for all possible value combinations of weighting factors would be the resultant Pareto Front (shown in Fig. 5.1). Therefore, the MDO results in a set of Pareto-optimal solutions in the performance space. Considering a two-dimensional performance space, for any point on the Pareto Front, an increase in one performance index is only possible with a decrease in the other performance index. The final design point is ultimately selected from Pareto-optimal design solutions and is based on the compromise between individual optimization goals.
5.3 Modified System Design Flow

As described in the previous section, design optimization of a converter is generally done using the nominal values of all component parameters. However, in the real system, there is a tolerance associated with the different parameters of each component; these variations are mainly due to manufacturing variability. One of the approaches for solving MDO in the presence of PU is the probabilistic approach, where UQ is incorporated into in the optimization formulation.

As discussed in Chapter 2, the uncertainty due to physical variability in the system properties and surrounding is often irreducible and is commonly represented by probability distributions. If an uncertain design variable or non-design system parameter can be described using a combination of data points or an interval, then the principle of likelihood can be used to construct a probability distribution \( f_X(x) \). Assume the type of distribution (normal, lognormal, uniform, etc.) of \( x \) is known and let \( L \) denote the distribution parameters. Then the probability density function (PDF) of \( x \) is denoted by \( f_X(x|L) \). Note that this density function is conditional on the choice of parameters, and hence these parameters (\( L \)) need to be estimated using the available evidence.

To account for parametric uncertainty, the system design flow must be modified accordingly, as the input parameters are no longer considered deterministic. As a result, optimization under PU requires an extra loop of computation, i.e., parametric uncertainty quantification (P-UQ), in each system design iteration. Nondeterministic simulation can be employed to propagate the uncertainties throughout the model to estimate the variability in the model outputs, such as performance indices and constraint functions. Therefore, at each design iteration, the output distributions and probabilities of satisfying constraint thresholds need to be evaluated given the design variable values.
Figure 5.3: System design flow with built-in parametric uncertainty quantification (P-UQ).

Among nondeterministic simulation approaches, MC simulation takes into consideration almost all possible value combinations of the uncertain parameters. Therefore, MC-based nondeterministic optimization formulation often suffers from the intensive computational effort required. In a worst-case analysis, however, statistical analysis is carried out by considering a certain number of different combinations of values of the parameters in question. Hence, to reduce the computational effort for MDO with P-UQ, in the case of analytical models, for which the explicit solution to the model is available, the worst-case analysis is conducted to estimate the variability in the model output. In the case of numerical models, however, MC sampling must be used to propagate uncertainties throughout the model and
5.4. New Performance Vector

estimate the variability in the model output.

Figure 5.3 illustrates the flow diagram summarizing the system design process with built-in P-UQ. As seen, there are two types of models in the general system design process: behavioral model and component models. Since the governing differential equations of power electronics behavioral models rarely yield exact solutions for practical problems, approximate numerical solutions must be used. Component models, on the other hand, are usually analytical models and have a closed form solution. Therefore, to incorporate P-UQ analysis, quasi-random MC simulation and worst-case analysis are incorporated into behavioral models and component models, respectively.

5.4 New Performance Vector

In the modified system design flow, multiple simulations must be conducted for each point in the design space. As a result, in each design iteration, instead of a single value for each performance measure, multiple values are generated to reflect the effect of manufacturing variability on the predicted performance indices. A PDF of uncertain performance measures can then be denoted by $f_{j}(j|L)$, which is conditioned on the choice of parameters; these parameters (mean, standard deviation, etc.) need to be estimated using the resultant data points from the nondeterministic simulation.

Accordingly, for the design of a power converter to be optimized under PU, two goals must be formulated mathematically: first is maximizing the mean of the performance functions and the second is minimizing the variation of the performance functions, which is usually modeled by its variance or standard deviation. In other words, each performance function is now represented as two corresponding objectives in the MDO with P-UQ formulation. These two objectives should be achieved simultaneously to ensure performance
robustness and optimality. This will increase the set of objectives from \( k \) objectives to \( 2k \) as below.

\[
\begin{align*}
\max & \mu_J(x, x_d, p, p_d) \\
\min & \sigma^2_J(x, x_d, p, p_d)
\end{align*}
\] (5.6)

\[
\begin{align*}
x_{dLB} \leq x_d \leq x_{dUB} \\
p_{dLB} \leq p_d \leq p_{dUB}
\end{align*}
\] (5.7)

In (5.6) and (5.7), \( \mu_J \) and \( \sigma^2_J \) are the mean and variance vectors of performance functions, \( x_{dUB}, x_{dLB}, x_{UB}, \) and \( x_{LB} \) are the vectors of upper and lower bounds on the deterministic and nondeterministic design parameters; \( p_{dUB}, p_{dLB}, p_{UB}, \) and \( p_{LB} \) are the vectors of upper and lower bounds on the deterministic and nondeterministic non-design system parameters; and \( \mu_x, \sigma^2_x, \mu_p, \) and \( \sigma^2_p \) are the mean and variance vectors of uncertain design and non-design system parameters, respectively.

Since each performance function is represented as two objectives, the MDO formulation can quickly become intractable even with a small number of them. In addition, a large number of objective functions in such problems causes an inability to graphically visualize the Pareto set to understand tradeoffs introduced by design robustness considerations. Thus, the main drawback of such methods is that they become burdensome to solve as the number of performance functions increases [48, 64, 81, 86].

A new approach has been proposed [71] that tackles both robustness and optimality using the joint probability density function of all the performance functions. The MDO problem is hence reduced to a two-dimensional optimization problem regardless of the num-
ber of objectives. However, this approach cannot be readily visualized and interpreted. Such a representation lacks any information regarding the tradeoff between different performance measures, whereas this information is typically expected to aid in decision-making for MDO problems.

In the formulation proposed in this work, the sensitivity index is first defined for the performance function to provide a measure of robustness for each primary performance index in the presence of PU. The aggregated function of individual sensitivity indices, herein after referred to as total sensitivity, is then used as an additional performance measure in the MDO formulation. This new performance measure represents the total sensitivity of the design with regards to PU. Such a representation takes into account the manufacturing variability in the decision-making by minimizing a scalar quantity irrespective of the number of performance functions.

In this work, equation (5.8) is first used to calculate the sensitivity index for each performance measure:

$$S_i = \frac{3\sigma_{j_i}(x, x_d, p, p_d))}{\mu_{j_i}(x, x_d, p, p_d)}$$

(5.8)

where $\sigma_{j_i}$ and $\mu_{j_i}$ are the standard deviation and mean value of the $i^{th}$ performance index, and $S_i$ is the resultant sensitivity index of the $i^{th}$ performance measure. As shown in equation (5.8), to calculate sensitivity indices, the tolerance of each performance index is normalized with respect to its mean value to avoid scaling issues when aggregating the sensitivity indices; this can occur when the variances of the performance functions are of largely disparate magnitudes.

The individual sensitivity indices are finally aggregated using weight-based methods by expressing preferences between objectives using weights; this results in a total sensitivity index for each design point. The weightings of the individual performance indices deter-
mine the compromise between the individual optimization goals. The total sensitivity index ($S_T$) is hence calculated based on the compromise between individual performance measures according to the optimization goals as below:

$$S_T = \sum w_i S_i; \quad \sum w_i = 1$$  \hspace{1cm} (5.9)

The new performance vector is finally expressed as below:

$$\max \mu_J(x, x_d, p, p_d)$$

$$\min S_T$$  \hspace{1cm} (5.10)

In the proposed MDO formulation, the final performance space will have an additional performance index, which is the total sensitivity. As shown in Fig. 5.4, in the new performance space, the tradeoffs can be easily visualized using the aggregated sensitivity index of the performance functions. As the total sensitivity of a design approaches zero, the design would be more robust in the presence of manufacturing variability. An alternative design with a lower sensitivity index should hence be selected as the final optimum design. Conse-

Figure 5.4: Representation of the multi-objective design and optimization with uncertainty quantification (MDO with UQ): mapping a multi-dimensional design space into an enhanced multi-dimensional performance space with sensitivity index to determine the Pareto Front.
5.5. MDO with Built-in P&MF-UQ

Figure 5.5: Performance trends over time: introducing sensitivity as the measure of system design robustness.

sequently, total sensitivity can potentially be used as a measure of system design robustness to evaluate performance trends in the field of power electronics (Fig. 5.5).

5.5 MDO with Built-in P&MF-UQ

The previous section described how MDO with design robustness considerations could be accomplished by adding a PU-Q loop in the system design flow and modifying the performance vector accordingly. In this work, however, besides performance robustness, feasibility robustness is also considered; this is concerned with ensuring that the constraints are adequately fulfilled under uncertainty. Similar to performance objectives, as a result of incorporating UQ analysis, the constraint functions in the new MDO formulation are also modified to account for the effects of PU as below:

\[
\text{s.t. } \begin{align*}
Prob(g(x, x_d, p, p_d) \leq 0) & \geq P_{\text{target}}, \text{ and} \\
Prob(h(x, x_d, p, p_d) = 0) & \geq P_{\text{target}},
\end{align*}
\] (5.11)
where $P_{\text{target}}$ is determined based on the intended level of confidence. For instance, if $P_{\text{target}} = 100\%$ is selected then the constraints should be satisfied under the entire range of the resultant distribution, setting a more stringent requirement for the optimization.

Although $S_T$ is calculated for the nominal operating condition, the operating conditions are subject to variability such as load and source variation, and changes in the temperature. To ensure feasibility of the design under uncertainty, in practice, for a design point to be included in the final performance space, it should satisfy the constraints under the worst-case condition. MDO constraints are therefore modified as below:

\[
\begin{align*}
\text{s.t.} & \quad \text{Prob}(g(s_{\text{wc}}, x, x_d, p, p_d) \leq 0) \geq P_{\text{target}}, \quad \text{and} \\
& \quad \text{Prob}(h(s_{\text{wc}}, x, x_d, p, p_d) = 0) \geq P_{\text{target}},
\end{align*}
\]

(5.12)

where $s_{\text{wc}}$ is the vector of variables defining operating conditions at the worst-case conditions.

The credibility of the selected design point, in the end, relies entirely on the accuracy of the simulation models used in the process; this has not been considered in the MDO formulation thus far. In the next step, MF-UQ should be incorporated in the MDO to estimate the error due to MFU for all the points in the performance space.

For practical purposes, a reduced number of points in the performance space are selected based on a DOE. A validation metric is then used to calculate the MF error for the selected design points. These measured MF errors are called training data points ($\theta = \{x_d, \epsilon_{MF_{jn}}\}^D_{d=1}$, where $D$ is the number of selected points for model validation). Next, an interpolation procedure must be used for the estimation of MF error for the entire performance space. Finally, MF error is based directly on what has been observed in the prediction performance of the training dataset.

Many linear and nonlinear regression tools are available for predictive modeling, which
tries to find the best fit for the training dataset. The best fit is ultimately used to make predictions. In this work, however, GP is used, where the training dataset is used to train an algorithm to estimate the MF error where there is no data available (See Appendix C). A GP model is finally developed to determine the MF error of all design cases in the performance space based on validation results of the selected design points as below:

$$\epsilon_{MF_{ji}}(x) \sim GP(m(x), k(x', x')),$$

(5.13)

where $m(x)$ and $k(x', x')$ are mean and covariance functions, $x$ is the vector of design variables
corresponding to a feasible design in the performance space, and $\mathbf{x}'$ is the vector of training dataset that are the combinations of design variables for which MF error is available.

Primary MDO objectives are modified accordingly. Sensitivity indices need to be modified, too, based on the calculated MF error as below:

$$S_i' = \frac{3\sigma_j(s_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d)}{\mu_j(s_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d) - \epsilon_{MF_j}(s_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d)},$$

(5.14)

where $s_{nom}$ is the vector of variables defining operating conditions at the nominal condition.

The new total sensitivity index ($S_T'$) is then calculated as follows.

$$S_T' = \sum w_i S_i'; \quad \sum w_i = 1$$

(5.15)

Finally, the mathematical description of MDO with P&MF-UQ is given below:

$$\max(\mu_J(s_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d) - \epsilon_{MF}(s_{nom}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d))$$

$$\min S_T'$$

$$s.t. \quad \text{Prob}(g(s_{wc}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d) \leq 0) \geq P_{target}$$

$$\text{Prob}(h(s_{wc}, \mathbf{x}, \mathbf{x}_d, \mathbf{p}, \mathbf{p}_d) = 0) \geq P_{target}$$

$$\mathbf{x}_{dLB} \leq \mathbf{x}_d \leq \mathbf{x}_{dUB}$$

$$\mathbf{p}_{dLB} \leq \mathbf{p}_d \leq \mathbf{p}_{dUB}$$

$$\mathbf{x}_{LB} + 3\sigma^2_{x_{LB}} \leq \mu_{x} \leq \mathbf{x}_{UB} - 3\sigma^2_{x_{LB}}$$

$$\mathbf{p}_{LB} + 3\sigma^2_{p_{LB}} \leq \mu_{p} \leq \mathbf{p}_{UB} - 3\sigma^2_{p_{LB}}$$

(5.18)

It should be noted that, as discussed in Chapter 2, there are in fact three types of uncertainty sources that need to be considered in the design optimization under uncertainty:
5.6. Conclusion

The review of MDO application and its critical role in the field of power electronics was discussed in this chapter. The conventional MDO problems in this field involve deterministic evaluation of primary performance measures in which the nominal value of each performance function is optimized. Discussion on available MDO methods with robustness considerations in other technical fields was provided. The existing MDO problems with design robustness considerations involve nondeterministic simulations in which the variance vector of performance functions is minimized at the same time as maximizing the mean performance vector. As the number of performance functions increases, such formulations tend to have a large number of objective functions, which poses challenges in aggregating, solving, and visualizing the objectives.

In this chapter, a new design optimization approach was proposed to quantify and formulate design robustness with regards to manufacturing variability and modeling inaccuracy in the design problems with multiple performance functions. In this approach, the total sensitivity was introduced as a new performance measure, which is the weighted sum of...
of normalized standard deviation of primary performance indices. This scalar value represents robustness of the primary performance functions that are modified according to the estimated MF errors. To this end, a modified system design flow was illustrated to integrate UQ analysis into the MDO. Regardless of the number of performance objectives considered, the proposed formulation can reduce a generic $2k$-dimensional MDO problem into a $(k + 1)$-dimensional problem, while ensuring that design robustness considerations are addressed jointly for all objectives, and that constraints are adequately fulfilled under uncertainty. The effectiveness of the proposed method has been illustrated; due to the reduced number of objectives, it becomes more intuitive to apply preferences to optimality and robustness considerations and visualize the tradeoffs.

In Chapter 6, an example is presented for further investigations; a comprehensive design optimization of a Vienna-type rectifier with two primary performance functions – namely loss and size – is carried out to illustrate the proposed MDO with P&MF-UQ.
Chapter 6

Multi-Objective Design Optimization
of a Vienna-Type Rectifier

6.1 Introduction

In the development of power electronics systems for More Electric Aircraft (MEA) [19, 98] the power density and efficiency have been a primary concern [25, 94]. The Pareto Front concept has thus been carried out in the multi-objective design and optimization of these power converters to realize the performance limit based on the available degrees of freedom and to ultimately determine the final optimum design [40]. The main contribution of this chapter is to present the benefits of incorporating UQ analysis into the MDO, the methodology proposed in Chapter 5, from a more practical standpoint. For illustrative purposes, the Vienna-type rectifier, a popular topology for implementing ac-dc mains interface in MEA, is used as a case study to compare the theoretical analysis with a comprehensive experimental validation.
To this end, a thorough mathematical modeling and design optimization of the converter system and its components, in terms of efficiency and power density within given size limitations and operational requirements (electromagnetic interference (EMI), power quality, temperature), are shown in Sections 6.2 - 6.5. Key specifications, design variables, procedures, and models involved in the design and optimization are presented. The MDO with built-in P&MF-UQ is then used in Section 6.6 to design a robust free-convection-cooled Vienna-type rectifier with an input EMI filter. In Section 6.7, the modified trade-off limit curve (Pareto Front) of the enhanced multi-dimensional performance space, i.e., loss-size-sensitivity, is determined. Performance indices and key design variables of the selected optimum design based on conventional MDO, MDO with P-UQ, and MDO with P&MF-UQ is provided and compared in Section 6.8. Section 6.9 provides concluding remarks.

### 6.2 System Specifications and Requirements

The power electronics supply of high-power systems from the three-phase ac mains in MEA applications is usually carried out in two stages: The mains ac voltage is first converted into a dc voltage, which is then adapted to the load voltage by a dc-dc converter with galvanic isolation [26, 98]. This chapter focuses on design optimization of the ac-dc converter in the first stage.

Ac-dc converters are roughly categorized into two main groups: unidirectional and bidirectional. Due to the missing on-board storage element in MEA applications, energy feedback into the main is not allowed [11]. Therefore, only unidirectional front ends are considered for this stage. Unidirectional rectifier systems can further be divided into passive systems (e.g., three-phase diode bridge), hybrid systems (e.g., diode bridge with third harmonic injection), and active systems (e.g., pulse-width modulated (PWM) three-phase rectifiers) [38].
In aerospace applications, to select a suitable three-phase rectifier topology, several criteria should be considered [24] as summarized below:

- sinusoidal input currents (less than 5% total harmonics distortion (THD)),
- ohmic fundamental mains behavior (power factor (PF) = 1),
- controlled dc output voltage,
- unidirectional power flow with capability of reactive power compensation,
- simple circuit topology featuring phase and bridge symmetry,
- simple modulation and control schemes, and
- possibility to achieve high efficiency and high power density.

Considering these criteria, three-phase active PWM rectifiers are well suited for implementing ac-dc power converters, as they feature superior performance in comparison with other unidirectional topology candidates in terms of efficiency, input-current quality, and weight [26].

Figure 6.1 shows the system configuration of a three-phase active ac-dc converter in which a three-phase active front end (AFE) converts three-phase ac input voltage into regulated dc voltage while providing the power-factor correction (PFC) function. In this work,
a Vienna-type rectifier is selected as the targeted topology for implementing the AFE rectifier due to its high efficiency as compared with other topology candidates; this will be further discussed later in this chapter. Additionally, an input EMI filter is added between the three-phase source and the converter to bring the converter into compliance with the EMI standard.

The primary objective of this work is to optimize the design of a local converter card (shown in Fig. 6.1) with regards to design robustness, efficiency, and power density, while addressing combined power quality, EMI, and thermal requirements. An aircraft variable-frequency ac power bus feeds the converter and output power should provide 345 V dc voltage. The converter will be designed for the maximum tenable power rating within the given constraints of volume \((8.3 \times 7.26 \times 1 \text{ in}^3)\) and total loss \((30 \text{ W})\) under specified operating conditions. To avoid any active cooling in the converter, an efficiency of greater than 98 % is required. The maximum allowable loss should be considered for the worst-case condition. Therefore, the maximum desired loss at nominal power is limited to lower values. Given the minimum required efficiency to achieve free-convection-cooled design and the required margin for allocated loss in the worst-case condition, the maximum attainable power rating of the converter is set to approximately 1.25 kW. The system specifications and operating conditions of the converter are summarized in Table 6.1.

In summary, according to MDO objectives, the primary performance indices in this work are loss and size of the converter. The final converter should also comply with the DO-160 standard for EMI and power quality (PQ) (see Figs. 6.3 and 6.2). These specifications set the limitations in the converter design optimization, as described in the next section.
Table 6.1: Summary of system specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal output power $P_{out}$</td>
<td>1.25 kW</td>
</tr>
<tr>
<td>Line-to-line rms input voltage $V_{ac}$</td>
<td>115 V ± 10%</td>
</tr>
<tr>
<td>Nominal output DC voltage $V_o$</td>
<td>345 V</td>
</tr>
<tr>
<td>Line frequency $f_o$</td>
<td>360 Hz ~ 800 Hz</td>
</tr>
<tr>
<td>Operation temperature $T_a$</td>
<td>-40 °C ~ 70 °C</td>
</tr>
</tbody>
</table>

Figure 6.2: Maximum limit (percentage of fundamental component) for low-frequency harmonics, i.e., up to the 40th harmonic order, based on the DO-160 standard.

Figure 6.3: Conducted emission limits based on the DO-160 standard.
6.3 Converter Design Considerations

In the design of power converters, a circuit topology and its associated modulation and control schemes must be selected, and the component values and control parameters should be determined in such a way that system specifications and regulations are fulfilled. For rectifiers, in particular, the system must deliver the required output power in a defined range of input voltage; the switching-frequency ripple of the output voltage must be limited to an upper limit; the correction of the output voltage after a load step must take place in a defined maximum time; and the regulations regarding EMI emissions and PQ must be satisfied. Additionally, minimum requirements regarding system performance, i.e. maximum allowed loss and size, must be fulfilled. Selection of the components must be made in such a way that materials limits, such as the maximum junction temperature of the power semiconductors, the maximum flux density of the magnetic materials, and the maximum current loading of filter capacitors, do not exceed their limits.

Accordingly, design of a converter is comprised of several steps, including topology selection, input/output filter design, modulation implementation, implementations of passive devices, selection of semiconductor devices, and design of the control system; each of these steps is discussed in the following sections, in which key design variables are identified and described.

6.3.1 Topology Selection

As discussed before, three-phase active PWM rectifiers are preferred for implementing ac-dc power converters, due to their high efficiency and high input-current quality compared to other topology candidates [38].
6.3. Converter Design Considerations

Although conventional two-level boost rectifiers have become dominant in the industry, if higher efficiency is required, three-level converters present a better solution. Three-level converters have a lower switching voltage, thus allowing the use of switches with lower blocking voltage which usually present lower on-resistance and higher junction capacitance, resulting in lower loss and higher efficiency. Three-level rectifiers also have the advantage of an improved current-waveform quality compared with two-level rectifiers [105].

The most renowned three-level implementation of a three-phase active PWM rectifier is the Vienna-type rectifier. The main advantage of this topology is its high reliability due to the impossibility of shoot-through failure modes. Although the forward-voltage drops of the diodes in this rectifier result in high conduction losses, the development of SiC Schottky diodes with high blocking voltage and, ideally, no reverse-recovery current has eliminated this source of loss and has further improved the efficiency of this converter [95].

The circuit schematic of the selected topology is shown in Fig. 6.4, in which a Vienna-type rectifier converts three-phase variable-frequency ac input voltage into regulated dc voltage while providing the PFC function. Among various phase-leg configurations, the one used

![Circuit schematic of the Vienna-type rectifier.](image-url)
in this work features the highest efficiency [11]. For active switches, Vienna-type rectifiers require four-quadrant switches to block voltage and conduct current in both directions. Two MOSFETs are hence connected in a common source configuration in this topology. There is also an input EMI filter added to the three-phase converter to make the converter comply with EMI and power-quality standards, which will be further discussed in Section 6.3.7.

6.3.2 Operation Principle

To better understand the design procedure, the operation principle of the Vienna-type rectifier is briefly discussed in this section. The Vienna-type rectifier is a current-commutated converter, meaning the devices participating in commutation are determined by current direction. As described in (6.1), the rectifier input terminals are clamped to positive ($V_o/2$), negative ($-V_o/2$), or the neutral-point ($M$) voltage rail depending on the input-current direction and the state of the corresponding switches:

$$v_{j'M} = \begin{cases} 
\frac{V_o}{2}\text{sign}(i_j) & \text{for } s_j = 0 \\
0 & \text{for } s_j = 1 
\end{cases}, \quad (6.1)$$

where $i_j$ is the phase current, $v_{j'M}$ is the input rectifier voltage of $j$-phase referred to the middle point $M$ ($j \in \{a, b, c\}$).

It is worth noting that in three-phase PWM rectifiers, in general, there is no connection between the star point of the supplying mains ($K$) and the center point of the output DC voltage $M$ (see Fig. 6.4). As a result, only the differences between phase voltages formed at the input of the rectifier ($v_{j'K}$) and the mains voltages ($v_{jK}$) influence the formation of the phase currents in the mains as below:
Therefore, the zero-sequence voltage between $K$ and $M$ can adopt any value; its waveform shape depends on the selected modulation strategy. This enables the possibility of implementing high-performance modulation strategies (see Section 6.3.3).

6.3.3 Modulation Scheme

Continuous pulse-width modulation (CPWM) and discontinuous pulse-width modulation (DPWM) are two modulation-scheme candidates for ac-dc active converters [41].

In DPWM, sinusoidal currents are formed by switching only two rectifier phase legs while the third phase leg is clamped to an output voltage bus, which results in reduced switching events. Additionally, the phase-clamping intervals occur around the peaks of the respective phase current to further minimize switching loss, where the selected phase changes in a cyclic manner over one period of the mains. As a result, where there is a constant switching of the power devices, DPWM has lower switching losses compared to CPWM [70]. For a defined value of allowable switching loss, this allows an increase in the effective switching frequency for DPWM, which is the main advantage of DPWM over CPWM.

The possibility of increasing the effective switching frequency will lead to significant reduction of the rms value of current harmonics in the mains, especially for high values of the modulation index [42]. Therefore, DPWM has a lower ripple of phase current in the mains. In addition, it is known that the cut-off frequency of the EMI filter should be considerably lower than the switching frequency. Increasing the switching frequency thus enables pushing the cut-off frequency to higher values and accordingly reducing the size of
the input EMI filter.

However, DPWM lacks the flexibility of choosing a redundant vector, which will result in poorer harmonic performance compared to CPWM. This situation is even more significant at lower modulation-index values, and results in a dominant third harmonic in the neutral-point current. This current flows into the parallel connection of the output capacitors, and the implementation of neutral-point voltage control may introduce further switching transitions. Therefore, to maintain the same level of third-harmonic voltage ripple as in CPWM, an increase of output capacitance value is required; this, in effect, results in a reduction in power density.

Although requirements such as the hold-up time may dominate over the mentioned increase in the DC capacitor, given the design requirements in this work (see Section 6.2), CPWM is selected as the modulation scheme to achieve a higher-power-density design. In CPWM, the ripple of the phase current in the mains is influenced by the distribution of redundant switching states. In the development of space-vector PWM (SVPWM), the zero space vector positions are left undefined and there is an opportunity to explore possible harmonic benefits by manipulating the placement of zero pulses [31]. In this work, center-aligned SVM is used; the active space-vector is centered in each half carrier period and the remaining zero space-vector time is split equally, such that the redundant vector occurs at the first and last positions of the switching sequence. This will essentially improve the input-current quality to better comply with PQ standards.

6.3.4 Control Algorithm

The controller architecture implemented in this work, with the primary purpose of controlling the three-phase input current and dc bus voltage of the Vienna-type rectifier is
6.3. Converter Design Considerations

shown in Fig. 6.5. The overall control algorithm is described in the following paragraphs.

The mains’ three-phase voltage and current and the dc bus voltage are sensed with a sampling frequency that is the same as the switching frequency. The sensed input voltage is fed to the phase-locked loop (PLL) to determine the angle of the input-voltage vector in the $\alpha\beta$ frame. This angle is used to convert the sensed current signal from the $abc$ frame into the $dq$ frame. The current controller is implemented in the $dq$ frame using PI compensators, for which the reference signal for the $q$ component is set to zero to achieve unity PF and the reference signal for the $d$ component is generated by the outer voltage-control loop. The voltage controller is also implemented using a PI compensator and the reference voltage is set to be the required nominal output voltage. The outputs of the current-control loop are finally fed to the modulator, in which the turn-on time and turn-off time for each switch in

Figure 6.5: Control architecture and power stage of the Vienna-type rectifier.
the next switching cycle are generated.

To further improve the quality of input power, two special feed-forward loops are added to the control architecture – namely, turn-off delay and $\theta_{rec}$ compensation loops [11]. The turn-off delay compensation loop is required to compensate for the turn-off delay caused by charging the output capacitors of the MOSFET during its turn-off period. All the charge consumed by the output capacitor of a device is provided by the line current. Therefore, when the line current is small, charging output capacitors of the MOSFET may last for a long time and result in false modulation and distorted input current. The addition of a feed-forward loop resolves this problem where the total compensated time is calculated by examining the turn-off voltage waveforms using phase-current and gate-falling times. The $\theta_{rec}$ compensation loop is also used to avoid false modulation caused by the change in phase-current polarity. To avoid false modulation, the location of the current vector should always be known to the modulator. A feedforward loop is thus added to calculate the angle between the current and voltage vectors.

Another control loop discussed in the literature is the control of the neutral-point voltage. The neutral-point-balancing control strategies are based on the same degree of freedom used to implement the current controller. However, in this work, the effect of adding voltage balancing was not significant; an acceptable balancing was achieved without adding further complexity to the controller. Therefore, no voltage-balancing controller was used in the final testing of the converter.

6.3.5 Switching Frequency

A relatively high switching frequency is required to obtain a low design volume of magnetic components to further increase the power density in the design of power electronic
systems. However, high switching frequency results in an increase in frequency-dependent losses (e.g., switching loss, skin and proximity effect loss, etc.), and hence a relatively low-efficiency design will be achieved. As a result, if the switching frequency is increased above a certain limit, the volume of the cooling system finally dominates, and the output-power density will be reduced. Thus, to maintain an efficiency of less than 98 % to avoid any active cooling, and according to preliminary calculations, the maximum switching frequency in this design is limited to 92 kHz.

Minimum switching frequency, on the other hand, is determined according to the DO-160 PQ standard. This PQ standard has limitations up to 40\textsuperscript{th}-order harmonics; given the frequency range for the mains (360 Hz $\sim$ 800 Hz), this would limit the minimum switching frequency to values higher than 32 kHz.

### 6.3.6 Boost Inductance

The boost inductance will affect low-frequency current harmonics, which are critical to meeting the PQ standard. For the selected boost-inductance value, therefore, the PQ must be checked to ensure compliance with the standard. The boost-inductance value must also increase with the reciprocal of the switching frequency to retain a relatively low switching-frequency ripple in the input current. Given the maximum and minimum allowable switching frequencies in this design (see Section 6.3.5), the final range for boost-inductance value in this design is 210 $\mu$H- 450 $\mu$H.

### 6.3.7 DM EMI Filter

A CLCL structure has been selected as the differential mode (DM) EMI filter configuration per phase [94]. In this configuration, a damping resistor is also added in series with
the DM capacitor to damp unwanted current noise in the power-quality standard band (up to 32 kHz) that is caused by filter resonance.

The DM filter capacitance value is selected based on the reactive power constraint and rectifier functionality described in the following. For a Vienna-type rectifier, the angle between phase-leg current and voltage should be low enough to ensure correct modulation; this requirement places limitations on the total allowed filter capacitance. The angle limit (\(\theta_{\text{lim}}\)) is given by (6.3):

\[
\theta_{\text{lim}} = |\arcsin\left(\frac{1}{\sqrt{3M}} - \frac{\pi}{6}\right)| = 0.124 \text{ rad}, \quad (6.3)
\]

where \(M\) is the modulation index and is defined as \(2V_{\text{ac,pk}}/V_o\). Assuming unity power factor is achieved at the input terminals, this limits the angle between the filter’s reactive power and the converter’s active power, as follows:

\[
\arcsin\left(\frac{Q_f}{P_o}\right) < \theta_{\text{lim}}, \quad (6.4)
\]

\[
\arcsin\left(\frac{|Q_f|}{P_o}\right) \approx \arcsin\left(\frac{2\pi f_{\text{in}} L_f f_{\text{in,rms}}^2 - 2\pi f_{\text{in}} C_f V_{\text{in,rms}}^2}{I_{\text{in,rms}} V_{\text{in,rms}}^2}\right) < \theta_{\text{lim}}, \quad (6.5)
\]

where \(L_f\) is the total inductance and \(C_f\) is the total capacitance per phase. Based on (6.5), the total allowed filter capacitance is related to the input frequency, active power, and total filter inductance. However, the second term in (6.5) is dominant in determining the phase angle between the filter’s reactive power and the converter’s active power. Therefore, changes in the total inductance value will not significantly affect this angle. In this design, the minimum required capacitance is estimated such that the correct modulation is guaranteed under half load with 800 Hz input frequency. The minimum required \(C_{DM}\) is estimated to
be 0.22 $\mu F$. Finally, the 0.22 $\mu F$ EPCOS MKT film capacitor is selected.

The minimum required DM filter inductance is then calculated based on EMI constraints as follows. For a given operating condition, the output-voltage spectrum of each phase leg (referred to as $v'_a$, $v'_b$, and $v'_c$) can be calculated using the Matlab Simulink simulation model or analytical models, i.e., by applying double Fourier transformation to the modulator reference and carrier. A limited range of possible damping resistor values is defined accordingly to ensure that the design complies with the PQ standard. With the voltage spectrum calculated, and the filter capacitance and damping resistance selected, DM inductance can be derived based on the EMI standards using the DM model (shown in Fig. 6.6), in which DM source voltage magnitude is calculated as below:

$$V_{DM, source} = v'_a - \frac{v'_a + v'_b + v'_c}{3}$$

6.3.8 DC Output Capacitance

The dc bus capacitance value ($C_o$ in Fig. 6.4) is determined by the output power. This capacitor is also selected such that the voltage rise on the dc bus capacitors at sudden load
drops (i.e., full load to no load) will not exceed the voltage limit of either the capacitor or the semiconductor devices. Also, for overall power density, the design volume of the output capacitor is considered.

Furthermore, as discussed in Section 6.3.2, the neutral voltage ripple is influenced by input frequency and the modulation index. Depending on the selected modulation scheme, third-order harmonics can be found on neutral-point voltage, which will result in $(6k \pm 1)^{th}$-order harmonics in input current, where $k \in \{1, 2, \ldots\}$. As such, for a Vienna-type rectifier, which is a three-level converter, the low-frequency ripple on the two dc bus capacitors, which is known as the neutral-point ripple, may influence the input-power quality. As a result, the dc bus capacitance should be large enough to ensure compliance with the power-quality standard. In this design, 15 $\mu F$ EPCOS MKP film capacitors are selected.

### 6.3.9 Magnetic Cores

A core material and core geometry must be selected for magnetic components, i.e., the DM and boost inductors. In this work, other aspects of the inductor design, such as realization of airgap length, number of turns, winding arrangements, winding cross-section or copper foil, etc., are specified later as non-design system parameters through the system design flow.

For boost and DM filtering inductor implementation, Ferroxcube 3C95 ferrite cores (effective volume: $5470 \ mm^3 \sim 52600 \ mm^3$), and Magnetics Inc. MPP iron-powder cores (effective volume: $960 \ mm^3 \sim 10600 \ mm^3$) are considered; these have relatively lower cost compared to amorphous materials.
6.3.10 Semiconductor Devices

The total loss in a Vienna-type rectifier is dominated by the conduction and switching losses of the power semiconductors. Hence at a given switching frequency, a possibility of maximizing the efficiency appears through the optimum choice of power semiconductor devices. Power semiconductors or semiconductor modules are available from semiconductor manufacturers in prefabricated packages for various application areas. The design is thus limited to the selection of options available from appropriate semiconductor devices which in this case are MOSFET and diode as follows.

MOSFETs with lower on-resistance have higher junction capacitance, which result in higher switching losses. The on-resistance of the MOSFETs is therefore a critical parameter in determining loss and is used as a design variable to select device candidates. In this work, 250 V Si MOSFETs with 20 mΩ and 60 mΩ on-resistance from Infineon are selected (IPB200N25N G3 and IPB600N25N G3).

The loss generated by diodes is not limited to conduction loss, as they will also generate switching losses due to charging and discharging of their junction capacitors. To achieve maximum efficiency, diodes should be carefully selected with consideration given to their influence on both conduction loss and switching loss. Diodes with larger current capability have higher junction capacitance values that generate more loss. Therefore, current capability is used as a design variable to select diode candidates. In this work, 650 V SiC Schottky diodes with 16 A and 20 A current rating from CREE are selected (IDH20G65C5 and IDH16G65C5).


6.4 Design Variables

In this section, a sweeping program is executed to find all possible value combinations of system-design variables to determine the final design space. It is worth noting that although certain design variables, such as AFE topology, EMI filter structure, modulation scheme, and control parameters, have been predetermined, any of these variables could have been realized through an MDO process with the penalty of higher computational cost.

The design procedure described in this work is based on the systematic approach for designing the ac-dc converter presented in a previous work [94]. This procedure starts with the definition of converter specifications and standards (see Section 6.1). Following, the switching-frequency and boost-inductance values are selected from the available range, after which the voltage spectrum can be derived from switching-model simulation results using the center-aligned SVM modulation scheme. Damping resistance is then selected from the available options. The minimum required DM inductance of the converter is then calculated as described in Section 6.3.7.

At the end of each iteration, PQ requirements are checked for up to the 40\textsuperscript{th} harmonic of the input current as well as EMI requirements for 150 kHz up to 10 MHz. It is worth noting that EMI and PQ requirements are checked at the worst-case condition, which is 100 V ac input voltage and 800 Hz input line frequency. This will ensure functionality of the converter over the entire range of operating conditions.

If both standards are met, then the values of the design variables are stored. In the preliminary design process shown in Fig. 6.7, only the system design parameters are swept. Semiconductors, core size, and core type are component-level design variables, which are added to the final design vector. This would result in a 9-dimensional design space comprised of the following design variables: MOSFET, Diode, $F_{sw}$, DM inductor-core type, DM
Standards and specifications

\[i=0, j=0, k=0\]

- \(i = i + 1\)
  - Select \(i^{th}\) switching frequency
  - \(j = j + 1\)
    - Select \(j^{th}\) boost inductance \((L_B)\)
    - \(k = k + 1\)
      - Extract voltage spectrum
      - Select \(k^{th}\) damping resistance \((R_{\text{damp}})\)
      - Calculate DM capacitance \((C_{\text{DM}})\) and DM inductance \((L_{\text{DM}})\)

- Power Quality met?
  - No
    - Store \([F_{\text{sw}}, L_B, R_{\text{damp}}, L_{\text{DM}}, C_{\text{DM}}]\)
  - Yes
    - End

- \(K = l?\)
  - No
    - \(j = m?\)
      - No
        - \(k = l?\)
          - No
            - \(i = i + 1\)
          - Yes
            - \(j = j + 1\)
        - Yes
          - \(k = k + 1\)
      - Yes
        - \(i = i + 1\)
    - Yes
      - \(j = j + 1\)
  - Yes
    - \(k = k + 1\)

Figure 6.7: System under investigation: a three-phase AC/DC converter.
inductor-core size, $L_{\text{boost}}$, boost inductor-core type, boost inductor-core size, and $R_{\text{damp}}$. The specified range for design variables and the value for design constants and non-design system parameters are summarized as follows:

- topology: Vienna-type rectifier,
- modulation scheme: center-aligned SVM,
- control parameters: determined based on Section 6.3.4,
- switching frequency ($F_{\text{sw}}$): 60 kHz - 92 kHz,
- boost inductance ($L_{\text{boost}}$): 210 $\mu$H - 510 $\mu$H,
- boost inductor-core type: Ferrite and iron powder,
- boost inductor-core size: 5470 $mm^3$ $\sim$ 52600 $mm^3$ for ferrite cores, and 960 $mm^3$ $\sim$ 10600 $mm^3$ for iron-powder cores,
- damping resistance ($R_{\text{damp}}$): 0.5, 1, 2, and 4 $\Omega$,
- DM capacitance ($C_{\text{DM}}$): 0.22 $\mu F$,
- DM inductance ($L_{\text{DM}}$): determined according to 6.3.7,
- DM inductor-core type: ferrite and iron powder,
- DM inductor-core size: 5470 $mm^3$ $\sim$ 52600 $mm^3$ for ferrite cores, and 960 $mm^3$ $\sim$ 10600 $mm^3$ for iron-powder cores,
- output capacitance ($C_{\omega}$): 15 $\mu F$,
- MOSFET: IPB200N25N G3 and IPB600N25N G3 , and
diode: IDH20G65C5 and IDH16G65C5.

It is worth noting that the rest of non-design system parameters, such as the number of turns and air-gap length for DM and boost inductors, are calculated separately for each design point to complete the design process of the converter.

6.5 Performance Indices

According to the primary goal of the optimization process, loss and size of the power converter need to be calculated at each design point. The required models for calculating loss and size have thus been implemented in the system-design flow. All of the circuit operation information required by loss and size calculation models (e.g., current through devices, flux density change in inductor cores, etc.) is captured by the switching model of a Vienna-type rectifier, which is implemented in Matlab Simulink (see Fig. 6.8). Loss and size models are described in the following.

![Figure 6.8: Switching model of the Vienna-type rectifier.](image-url)
6.5.1 Loss Model

The losses in a Vienna-type rectifier result mainly from its semiconductor devices and inductors. In this work, corresponding models for the conduction and switching losses of semiconductor devices, as well as the magnetic core and winding losses of inductors, have been developed and implemented in the system design flow [74, 83, 89]. Notably auxiliary circuits, including DSPs, provide a fixed amount of loss that is not dependent on the operating point of output power, and thus these circuits are not included in the loss model.

Many of the parameters used in loss models are temperature dependent. On the other hand, thermal considerations are one of the constraints in the MDO of the Vienna-type rectifier. As a result, estimating the temperature rise of a component is required and thermal models need to be implemented, mainly for those components that contribute significantly to the total loss of the converter (e.g., diode, MOSFET, and boost inductor). Consequently, an accurate estimate of model input parameters will be provided while ensuring that the temperature of a component is not exceeding its maximum limit.

6.5.1.1 Conduction Loss

Conduction loss is directly related to the resistance of the conductor and the rms current flowing through the conductor. The rms current in a specific component can be calculated mathematically or from simulations. MOSFETs, diodes, DM and boost inductors contribute significantly to the conduction losses of the converter.

MOSFET conduction loss is a function of its drain-to-source resistance during the on-stage as well as the rms current flowing through its channel. The diode conduction loss is also a function of its conduction characteristics and the current flowing through it.
MOSFET on-resistance and diode conduction characteristics are highly temperature dependent. Figure 6.9 shows the thermal model used for the diode and MOSFET, where $R_{\text{thJC}}$ and $R_{\text{thCA}}$ are the thermal resistance from junction to case and from case to ambient, respectively. This model is used to estimate the actual conduction characteristics according to the temperature.

Similarly, the winding conduction loss of each inductor can be calculated using the dc winding resistance and the rms value of the current flowing through the inductor. The conduction loss of each damping resistor is also calculated using its resistance value and the rms value of the current flowing through the resistor. It should be noted that the effect of the temperature on the conduction loss of inductors and damping resistors are assumed to be negligible.

In this work, the conduction loss due to the remaining resistive components, including PCB traces, cables, magnetic contactors, fuses, damping resistors and discharge resistors at the dc link, is assumed to be negligible.
6.5.1.2 Switching Loss

Switching of MOSFETs is a highly nonlinear procedure. In this work, the piecewise linear model for predicting the switching loss of the MOSFET is used [95]. This model is briefly discussed in this section to identify the parameters that should be included in the UQ analysis described later in Section 6.6. It should be noted that the total switching loss is calculated, including the driving loss and the efficiency of the auxiliary circuit that provides this energy.

The equivalent circuit model used in this section is shown in Fig. 6.10. The expected waveforms during the turn-on procedure are shown in Fig. 6.11. In this model, instead of non-linear capacitances, the gate charges of the MOSFET are used to calculate the turn-on and turn-off time due to the consistency of the charges in a wide voltage range. The common source inductors \(L_s\) and the loss caused by charging the diode during its turn-off (when turning on the switch) are considered.

There are four intervals in a switching procedure. The driving circuits, the parasitics

![Figure 6.10: Circuit for MOSFET switching loss calculation.](image-url)
and, most importantly, the gate charge dominating the interval determine the duration of each interval. The turn-on procedure is described as follows.

Interval 1: Gate-to-source voltage (gate voltage) $V_{gs}$ increases from zero to threshold voltage $V_{th}$. The gate charge that needs to be provided by the driver is $Q_{th}$. There is no switching loss from this interval.

Interval 2: Gate voltage $V_{gs}$ increases from $V_{th}$ to $V_{pl}$, (plateau voltage of the MOSFET). At the same time, the drain-to-source current rises to load current $I_{load}$. Gate charge during this interval (provided by the gate driver) is $Q_{gs1}$. The duration of this interval $t_r$ is given by:

$$t_r = \frac{2R_g(Q_{gs1} + \frac{L_sI_{load}}{R_g})}{2V_{dr} - V_{th} - V_{pl}}$$

(6.7)

where $R_g$ is the gate resistor, $L_s$ is the common source inductance, $I_{load}$ is the load current and $V_{dr}$ is the gate driver output voltage.

Interval 3: Gate voltage $V_{gs}$ stays at $V_{pl}$, due to the Miller effect. The drain-to-source voltage begins to drop. The total charge required by the Miller capacitor is $Q_{gd}$, which can
be found in the datasheet. Based on the analysis, the output current of gate driver $I_{gate,P3}$ during this interval is given by:

$$I_{gate,P3} = \frac{V_{dr} - V_{pl}}{R_g}$$  \hspace{1cm} (6.8)

The duration of this interval is given by:

$$t_f = \frac{Q_{gd} R_g}{V_{dr} - V_{pl}}$$  \hspace{1cm} (6.9)

It should be noted that the diode is also being charged during this interval, and the current charging the diode junction capacitor will flow through the MOSFET channel causing additional loss. The current charging the diode junction capacitor $I_{diode}$ during this interval can be expressed as:

$$I_{diode} = \frac{Q_{diode}}{t_f}$$  \hspace{1cm} (6.10)

where $Q_{diode}$ is the total capacitive charge of the junction capacitor of the fast diodes, which can be found in the datasheet of the diode. The resulting capacitive charge-loss energy ($E_{cap}$) is derived as below:

$$E_{cap} = \frac{1}{2} Q_{diode} V_{out}$$  \hspace{1cm} (6.11)

where $V_{out}$ is the dc bus voltage.

Interval 4: Gate voltage $V_{gs}$ continues to rise, resulting in further reduction of the MOSFET drain-to-source on-resistance. There is no switching loss in this interval; the device is considered to be fully on after this interval.
Accordingly, the turn-on loss energy in this switching is given by:

\[
E_{\text{on}} = \frac{1}{2} V_{\text{out}} I_{\text{load}} (t_r + t_f) + \frac{1}{2} Q_{\text{diode}} V_{\text{out}} \tag{6.12}
\]

Therefore, different load currents may lead to different levels of turn-on energy. Thus, the relationship between \(E_{\text{on}}\) and load current may be determined. Together with simulation, from which the turn-on current at any turn-on instant is modeled, the turn-on loss of the MOSFETs is calculated mathematically. The turn-off of the MOSFET is similar to its turn-on process, thus a similar equation is derived for turn-off loss energy.

### 6.5.1.3 Core Loss

The Steinmetz equation is used for core loss calculation. Theoretically, the flux density in the inductor is proportional to the input current; i.e., with the knowledge of the input current, the magnetization change of the inductor core and accordingly core loss can be calculated using the behavioral model and core characteristics given in the datasheet.

In the case of iron-powder cores, (6.13) is used for estimating core loss (in watts):

\[
P_{\text{core}} = K f_{\text{sw}}^\beta \left( \frac{n \Delta I}{2L_e} \mu_e \times 10^3 \right) \alpha V_e \times 10^{-6} , \tag{6.13}
\]

where \(K\) is the core loss constant, \(f_{\text{sw}}\) is the switching frequency, \(n\) is the number of turns, \(\Delta I\) is the magnitude of the current ripple, \(L_e\) and \(V_e\) are effective length and volume of the core, respectively, \(\mu_e\) is the effective permeability at the dc bias, and \(\alpha\) and \(\beta\) are constants determined by curve fitting.

Equation (6.14) is used for estimating core loss (in watts) for ferrite cores:
\[ P_{\text{core}} = 30.42 f_{\text{sw}}^{1.62} (B_{\text{max}} \frac{\Delta I}{2I_{\text{max}}} )^{2.77} V_e \times 10^{-6}, \] (6.14)

where \( B_{\text{max}} \) is the maximum flux density of the core, and \( I_{\text{max}} \) is the peak current.

Dissipation of the heat generated by the conductor and core losses is influenced by many factors. This means there is no simple way to precisely predict temperature rise. The temperature change in the selected ferrite cores is assumed to be insignificant given their large surface areas. The following equation gives a useful approximation for a component in still air and is used for estimating the temperature change in iron powder cores:

\[ \Delta T(\degree C) = \left( \frac{\text{Total losses (mW)}}{\text{Component Surface Area (cm}^2\text{)}} \right)^{0.833} \] (6.15)

It should be noted that in this work, due to the attained low switching-frequency ripple in the input current, the estimated core losses are small. In addition, skin and proximity-effect losses are assumed to be negligible with the use of Litz wire [87]. The dominant losses in both DM and boost inductors are thus conduction losses which can be dissipated via natural convection without the use of explicit cooling devices. The temperature rise for inductors is thus assumed to be insignificant compared to semiconductor devices.

### 6.5.2 Size Model

According to size constraints defined in Section 6.2, the height of all components is limited to 1 in. On the other hand, it is assumed that no inductors, capacitors, or semiconductor devices are placed over other devices. The total space occupied by each device is hence calculated by the multiplication of its footprint area and the height limit. Thus, in this optimization, the footprint area is taken as the performance index representing the size
of the converter.

The dimension for each component is extracted from the available library, and the footprint area is calculated accordingly. The footprint area of the final converter is the sum of the calculated footprint areas for all components. Whereas in the final prototype, there will be free spaces between components due to the minimum required clearance distance, smooth airflow, and non-optimum placements of the components. As a result, the size of the realized hardware is expected to be greater than the estimated value based on the component size models. This increase in the final converters size is assumed to increase linearly as the footprint area increases; and hence footprint area is considered as a fair index for comparing size of the designs.

### 6.6 System Design Flow with UQ

In this section, the design of a Vienna-type rectifier is represented as a mathematical mapping of the design space derived in Section 6.4 into the performance space using the models developed in Section 6.5.

To this end, through the conventional system-design flow for each point in the multi-dimensional design space, the switching model of the Vienna-type rectifier is run using the parameter values corresponding to the selected design point. The required information for selecting system components, such as operation parameters (e.g., rms/average current flowing through components), and component values (e.g., boost inductance, DM inductance, and damping resistance), with constraints of system operational requirements (temperature, EMI standard, and PQ standard) is extracted from simulation results of the behavioral model. All active and passive components are then designed and optimized based on the values given by the selected point in the design space, behavioral simulation results, and commercially
available components. Loss and size models are then used to calculate values of performance indices.

At the end of the optimization procedure, total loss and size are calculated at each design point, mapping the multi-dimensional design space into the two-dimensional performance space. Figure 6.12 shows the resultant feasible performance space derived from the MDO of the 1.25 kW Vienna-type rectifier using the information from the database, switching model of the converter, and component models.

The main benefit of projecting many converter designs into the multi-dimensional performance space is that it makes an easier comparison of the trade-off between multiple performance indices and allows for clear decision making. As shown in Fig. 6.12, the Pareto Front of the Vienna-type rectifier is then determined (indicated by the red stars). For the design points on the Pareto Front, a decrease in the loss is only possible with an increase in the size, and no design exists that would offer the same size with a lower loss.

The final design point is finally selected based on the compromise between individual optimization goals; the selected Pareto-optimal design point based on the conventional MDO
(MDO without UQ) features 21.58 in$^2$ total footprint area and 14.02 W loss.

It should be noted that there are tens of other Pareto-optimal design points available with predicted performances quite similar to the selected design. In the next section, an enhanced performance space with the sensitivity index is used to discern between cases and to help identify the design that is the most parametrically robust among the Pareto-optimal solutions. Further, the feasibility of the design at worst-case condition is checked as an additional MDO constraint.

### 6.6.1 Parametric Uncertainty

The switching model of the Vienna-type rectifier, as a behavioral model, is used to predict the behavior of a power converter to extract the required information for design and optimization of all active and passive components. Since the governing differential equations of such behavioral models rarely yield exact solutions for practical problems, approximate numerical solutions must be used. Loss and size models, on the other hand, are analytical models and have a closed-form solution. Therefore, to incorporate P-UQ analysis, quasi-random MC simulation and WC analysis are incorporated into the switching model of the Vienna-type rectifier and loss/size models of components, respectively.

Through the system design flow with P-UQ (see Fig. 5.3), for each point in the multi-dimensional design space, the switching model of the Vienna-type rectifier is run using the parameter values corresponding to the selected design point. Similar to the conventional approach, key design variables of the Vienna-type rectifier are identified and swept. With design variables selected, values of passive components are calculated based on simulation and analytical models to address EMI and PQ requirements.

However, in the modified system design flow, in addition to the nominal value for a
nondeterministic parameter, its associated tolerance is also required. A complete list of uncertain input parameters, i.e., nondeterministic design and non-design system parameters for behavioral and component models of the Vienna-type rectifier, is provided in Appendix D.

To predict primary performance measures in the system design flow with P-UQ, multiple simulations must be conducted for each point in the design space. As a result, instead of a single value for each performance measure, multiple values are generated that reflect the effects of manufacturing variability on the predicted performance indices. According to the number of uncertain parameters in the conducted MC simulation, the minimum required resolution for the MC output is set to 500 data points that are then used in WC analysis to estimate mean, upper, and lower boundaries for each performance measure.

The estimated upper, lower, and mean distributions are then used to estimate the required parameters ($L$) for defining a PDF ($f_j(j|L)$) for each performance measure. Based on the estimated parameters in this work, the resultant estimated loss and size values corresponding to each design point have lognormal and normal distributions (see Figs. 6.13a and

![CDF of the fitted distribution for: (a) loss, and (b) size (footprint area) of a design based on MC and WC analyses.](image)
6.6. **System Design Flow with UQ**

6.13b) with an associated PDF derived as (6.16) and (6.17), respectively.

\[
\text{Loss} \sim \text{Lognormal}(e^{(\mu + \sigma^2)}, e^{(2\mu + \sigma^2)}(e^{\sigma^2} - 1)) \\
\text{Footprint area} \sim \text{Normal}(\mu, \sigma^2)
\]

The sensitivity index for each performance measure is then calculated based on the derived distribution of each performance index using (5.8). The total sensitivity index is ultimately calculated using (5.9), where \(w_1 = 0.9\) and \(w_2 = 0.1\) are weighting factors for loss and size, respectively. The total sensitivity index is hence calculated based on the compromise between the sensitivity of loss and size with regards to manufacturing variability.

As discussed in Chapter 5, when the total sensitivity index of a design point approaches zero, the corresponding design would be more robust in the presence of manufacturing variability. The sensitivity index introduced in Chapter 5 is therefore utilized to help identify the most robust Pareto-optimal design solution [58].

It should be noted, although the total sensitivity of a design is calculated under nominal operating conditions (25 °C ambient temperature, 115 V ac voltage, and 100 Ω resistive load), to ensure the feasibility of the designs realized in the performance space the constraints must be fulfilled under the worst-case condition; that is 70 °C ambient temperature, 100 V ac voltage, and 95 Ω resistive load.

This procedure is iterated for all the points in the design space. In the end, a high-density performance space is mapped from the design space to a 3D performance space. Figure 6.14 illustrates the enhanced performance space resulting from MDO with P-UQ, with the sensitivity index as the third performance index. The parametric sensitivity of each
design point provides a comprehensive design criterion to enable the selection of the most robust Pareto-optimal solution. Therefore, an alternative design with lower sensitivity index should be selected as the final optimum design. Additionally, as a result of modifying the constraints and adding a third performance measure in MDO with P-UQ, there is a 32 % reduction in the number of feasible design points and a 2,200 % increase in the number of Pareto-optimal solutions in the performance space shown in Fig. 6.14 as compared to the two-dimensional performance space shown in Fig. 6.12. The total sensitivity index of the Pareto-optimal design points shown in Fig. 6.14 ranges from 17.3 % to 74 %; this range is limited to 17.3 % - 50 % for the Pareto-optimal solutions.

The total sensitivity of the preselected optimum design based on the conventional MDO approach is 49.7 %, i.e. the estimated loss using the exact parameters of 95 % of the hardware units built based on this design ranges from 8.97 W to 22.90 W. As a result of including P-UQ in the MDO, alternative designs with quite similar primary performance measures but relatively lower sensitivity compared to the preselected optimum design are realized in the

![Figure 6.14: Enhanced performance space of the Vienna-type rectifier indicating loss-size-sensitivity Pareto front under 1.25 kW rated power and the Pareto-optimal design solutions indicated by red stars: (a) top view, and (b) bottom view.](image)
performance space (Fig. 6.14). Finally, the most robust Pareto-optimal design with 30.6 \% parametric sensitivity, 21.5 in² total footprint area, and 14.10 W loss is selected.

The converters built based on the selected robust Pareto-optimal design are expected to have the least variability in their performance measures (e.g., less variability in the measured loss and size) and the best overall performance compared with the ones built based on the rest of the Pareto-optimal design solutions. According to the estimated loss and sensitivity index, 95 \% of the converters built based on this design would have a loss within 11.29 W and 20.00 W. However, this conclusion cannot be trusted, as its validity fully relies on the accuracy of modeling and simulation results, which have not yet been considered. This realization will be addressed in the following sections.

6.6.2 Model-Form Uncertainty

To validate the analytical and numerical models used in the MDO framework, and to estimate the error due to model-form uncertainty for all the points in the performance space, hardware demonstrations of a limited number of design points are presented with measurement results indicating the actual loss and size of the selected design points. Given the acceptable accuracy of the size models used in the design process and their low weighting factor in the optimization, MF error is only calculated for loss models.

In this section, to begin, DOE is conducted to determine different value combinations of design variables that should be studied for accuracy assessment of loss models. In this work, two hardware prototypes are built and tested for each design to evaluate the accuracy of the models used in the MDO framework. This testing is specifically in regards to their accuracy in the prediction of primary performance measures and to ensure that the design meets qualification testing standard constraints. A GP regression model is then developed
to estimate the MF error of all design cases in the performance space based on validation results of the selected design points.

### 6.6.2.1 Design of Experiments

MOSFET, diode, boost inductor, DM inductor, and damping resistors are the components considered in the total loss calculation of the Vienna-type rectifier. There are several design variables associated with these five components that are loss-model input parameters as well; i.e., switching frequency, boost-inductance value, boost-core size, boost-core type, DM-core type, DM-core size, MOSFET on-resistance, and diode current rating. In this section a DOE is conducted to study the effect of these design variables on the MF error.

To minimize the number of variables in the DOE, the components are first ranked based on their contribution to the total converter loss. Those with an insignificant contribution to the total loss can be ignored in the DOE, as their effect on the changes in the MF error over the entire performance space is perhaps insignificant. It should be noted that the contribution of each component to the total loss is not the same for all points in the performance space. To evaluate the importance of a component regarding loss calculation, its maximum contribution over the whole performance space is used for the comparison. Figure 6.15 shows the maximum contribution of each component to the total converter loss, indicating loss breakdown for each component.

The analysis of loss distribution shows that the boost inductor is the most important component to be considered in the DOE as it contributes up to 70% to the total loss in the Vienna-type rectifier. MOSFETs and diodes each contribute more than half, about 60%, to the total loss individually. DM inductors and damping resistors, however, are excluded from DOE due to their low contribution to the converter loss. Finally, those design
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variables associated with boost inductor, MOSFET, and diode are considered as variables in the conducted DOE.

To further minimize the number of design variables and their range in the DOE, the values of each design variable for the feasible design points in the performance space, especially for the Pareto-optimal solutions and their nearby design points, hereinafter referred to as the critical region, need to be studied. In fact, for a better decision-making, design solutions in the critical region require a precise estimate of their associated MF error as they are more likely to be selected as the final design. Therefore, the selected values of each design variable in the DOE must focus on its value in this region. Figs. 6.16 - 6.21 show the color-coded performance space with P-UQ and the resultant Pareto front; the color of each design point in the performance space indicates the value of the selected design variable for the design corresponding to that specific point.

As shown in Fig. 6.16, the switching frequency of feasible design points ranges from 60 kHz to 86 kHz. The frequency range of the critical design points, however, is more focused on lower values.
Figure 6.16: Enhanced (a) performance space, and (b) Pareto Front of the Vienna-type rectifier; the color of each design point indicates the switching frequency of its associated design.

Figure 6.17: Enhanced (a) performance space, and (b) Pareto Front of the Vienna-type rectifier; the color of each design point indicates the diode used in its associated design and identifies the total sensitivity value of the design.
Figure 6.18: Enhanced (a) performance space, and (b) Pareto Front of the Vienna-type rectifier; the color of each design point indicates the MOSFET used in its associated design and identifies the total sensitivity value of the design.

Figure 6.19: Enhanced (a) performance space, and (b) Pareto Front of the Vienna-type rectifier; the color of each design point indicates the boost inductance value of its associated design.
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Figure 6.20: Enhanced (a) performance space, and (b) Pareto Front of the Vienna-type rectifier; the color of each design point indicates the type of core used in its associated design and identifies the total sensitivity of the design.

Figure 6.21: Enhanced (a) performance space, and (b) Pareto Front of the Vienna-type rectifier; the color of each design point indicates the size of the core used in its associated design and identifies the total sensitivity range of the design.
As seen in Fig. 6.17, both diode candidates are used in the design points of the critical region. With regards to the MOSFET, as illustrated in Fig. 6.18, although the 200N25N3 device is dominant in the critical region, due to the critical role of MOSFET in determining the total loss of the converter, the MOSFET selection option will remain as a variable in the DOE.

According to Fig. 6.19, boost inductance value of the design points in the critical region are more focused on higher values. In addition, in the critical region, very few design points have been implemented using a powder core. Over 85% of the points on the Pareto front are, in fact, based on the use of a ferrite core (see Fig. 6.20). The conducted DOE is thus limited to designs with ferrite cores. Also, as shown in Fig. 6.21, the design points using cores with an effective volume of 5470 $mm^3$ and 52600 $mm^3$ will result in points toward extreme loss or size values in the performance space, which are not desired among Pareto-optimal design solutions. Therefore, the conducted DOE will be limited to those core sizes with an effective volume of 9440 $mm^3$ and 25800 $mm^3$.

In summary, the following design variables and their respective levels have been selected for the DOE:

- diode: 16G65C5 (1) and 20G65C5 (2),
- MOSFET: 200N25N3 (1) and 600N25N3 (2),
- switching frequency: 64 kHz and 76 kHz,
- boost inductance value: 410 $\mu H$ and 450 $\mu H$, and
- core size: ferrite cores with 25800 $mm^3$ and 9440 $mm^3$ effective volume.

It is assumed that for the same operating condition, the losses generated by different components in the Vienna-type rectifier are independent of one another, i.e., the parameters
used in estimating the loss of a component are not affected by the design variables associated with other components. In other words, the dissipated loss of a component will not affect the loss generated by the rest of the components. As a result, it is assumed that there is no interaction between design variables regarding the accuracy of the total loss of the converter.

Four one-factor DOEs are thus conducted to study the main effects of MOSFET on-state resistance, diode current rating, core size, and inductance value on the accuracy of the estimated loss (see Design 1a - 3a, 5a, and 6a in Table 6.2).

It should be noted that in the PCB layout of the final converter, semiconductor devices are placed close to one another. The temperature rise for diodes (MOSFETs) might be affected by the dissipated heat by MOSFETs (diodes); as a result, the temperature-dependent parameters of the diodes (MOSFETs) and their generated losses might get affected. This may violate the assumption made earlier regarding independence of estimated loss for components from one another. To verify the assumption, another case is also tested, in which both diode and MOSFET devices are changed compared to any of the first three designs.
conducted above (see Design 4a in Table 6.2).

Switching frequency affects the estimated loss of all critical components. As a result, for each of the selected designs, the switching frequency is varied and the results are obtained to investigate the effects of switching-frequency value on the accuracy of estimated loss for each component (see Design 1b - 6b in Table 6.2).

In summary, twelve different validation experiments need to be conducted, each of which correspond to a unique design point in the performance space. Table 6.2 summarizes the selected design points. It is worth noting that the primary design points (Designs 1a - 6a) are selected from feasible designs in the performance space. Also, to have a fair comparison, these primary designs have been selected in such a way that, except for the DOE variables, the remaining design and non-design system parameters of the converter are quite similar in all six designs.

6.6.2.2 Validation Experiments

This section presents testing results, and the performance evaluation of hardware prototypes replicates built for twelve preselected design points. Figures 6.22, 6.23, and 6.24 show hardware prototypes built based on Design 1-4, 5, and 6, respectively.

Experimental waveforms at nominal output power with different input-line frequencies are shown in Figs. 6.25 - 6.30 for all six designs (at 64 kHz switching frequency). All the waveforms presented in this section show that the designed Vienna-type rectifiers function properly with different input-line frequencies. No significant voltage overshoot is observed. The input current is well shaped and the dc bus voltage is stabilized as well.
Figure 6.22: Converter card hardware prototype based on Designs 1-4: (a) without CM filter (Prototype 1) and (b) with CM filter (Prototype 2).

Figure 6.23: Converter card hardware prototype based on Designs 5: (a) without CM filter (Prototype 1) and (b) with CM filter (Prototype 2).

Figure 6.24: Converter card hardware prototype based on Designs 6: (a) without CM filter (Prototype 1) and (b) with CM filter (Prototype 2).
Figure 6.25: Experimental waveforms of the operation of Design 1a converter prototype with (a) 360 Hz, and (b) 800 Hz line frequency. $I_a$ is the input current of phase $A$, $V_a$ is the input phase to neutral voltage of phase $A$, $V_{am}$ is the phase-leg output voltage (voltage at point $A$ referred to neutral point $M$), $V_{dcp}$ is the voltage across upper capacitor of the dc bus.
Figure 6.26: Experimental waveforms of the operation of Design 2a converter prototype with (a) 360 Hz, and (b) 800 Hz line frequency. $I_a$ is the input current of phase $A$, $V_a$ is the input phase to neutral voltage of phase $A$, $V_{am}$ is the phase-leg output voltage (voltage at point $A$ referred to neutral point $M$), $V_{dcp}$ is the voltage across upper capacitor of the dc bus.
Figure 6.27: Experimental waveforms of the operation of Design 3a converter prototype with (a) 360 Hz, and (b) 800 Hz line frequency. $I_a$ is the input current of phase $A$, $V_a$ is the input phase to neutral voltage of phase $A$, $V_{am}$ is the phase-leg output voltage (voltage at point $A$ referred to neutral point $M$), $V_{dcp}$ is the voltage across upper capacitor of the dc bus.
Figure 6.28: Experimental waveforms of the operation of Design 4a converter prototype with (a) 360 Hz, and (b) 800 Hz line frequency. $I_a$ is the input current of phase $A$, $V_a$ is the input phase to neutral voltage of phase $A$, $V_{am}$ is the phase-leg output voltage (voltage at point $A$ referred to neutral point $M$), $V_{dcp}$ is the voltage across upper capacitor of the dc bus.
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Figure 6.29: Experimental waveforms of the operation of Design 5a converter prototype with (a) 360 Hz, and (b) 800 Hz line frequency. $I_A$ is the input current of phase $A$, $V_a$ is the input phase to neutral voltage of phase $A$, $V_{am}$ is the phase-leg output voltage (voltage at point $A$ referred to neutral point $M$), $V_{dcp}$ is the voltage across upper capacitor of the dc bus.
Figure 6.30: Experimental waveforms of the operation of Design 6a converter prototype with (a) 360 Hz, and (b) 800 Hz line frequency. $I_a$ is the input current of phase $A$, $V_a$ is the input phase to neutral voltage of phase $A$, $V_{am}$ is the phase-leg output voltage (voltage at point $A$ referred to neutral point $M$), $V_{dcp}$ is the voltage across upper capacitor of the dc bus.
The input current is measured and analyzed to evaluate input power quality. The phase A current in the tests is measured by a Tektronics TCP0030 current probe, and the spectrum is calculated by MATLAB. The input-current spectrums within the power-quality standard range (from the 2nd-order harmonic up to the 40th-order harmonic), with 360 Hz and 800 Hz input frequency, for all six designs are shown in Figs. 6.31 - 6.42. As shown, there is no significant violation with regards to power quality in either the 360 Hz or the 800 Hz line-frequency case for any of the six design points.

Figure 6.31: Input-current harmonics of Design 1a with 360 Hz input frequency.

Figure 6.32: Input-current harmonics of Design 1a with 800 Hz input frequency.
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Figure 6.33: Input-current harmonics of Design 2a with 360 Hz input frequency.

Figure 6.34: Input-current harmonics of Design 2a with 800 Hz input frequency.

Figure 6.35: Input-current harmonics of Design 3a with 360 Hz input frequency.
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Figure 6.36: Input-current harmonics of Design 3a with 800 Hz input frequency.

Figure 6.37: Input-current harmonics of Design 4a with 360 Hz input frequency.

Figure 6.38: Input-current harmonics of Design 4a with 800 Hz input frequency.
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Figure 6.39: Input-current harmonics of Design 5a with 360 Hz input frequency.

Figure 6.40: Input-current harmonics of Design 5a with 800 Hz input frequency.

Figure 6.41: Input-current harmonics of Design 6a with 360 Hz input frequency.
Tests have also been conducted to evaluate the EMI performance of the converters. The converter-grounding arrangement for EMI measurement is shown in Fig. 6.43. In tests for EMI measurement, the converter is connected to the line-impedance-stabilization-network (LISN) that is required by all conducted emissions standards. Due to the possible variation in the external networks that depend on the application, a fixed network is defined by the standards that must be used for evaluating the EMC compliance of the electronic products. LISN is a line-filter that has a 50 Ω input impedance looking from the converter side. It isolates the AC mains from the converter under test and hence enables accurate measurement of EMI noise [6]. The termination is chosen to be 50 Ω in order to match the 50 Ω port of a spectrum analyzer (or an EMC receiver) which is used for measuring the EMI noise.

The input currents are measured by an ETS-Lindgren 95510-1 current probe and are captured by an Agilent E7402A EMC analyzer. All measurements are taken under full-load operation, 400 Hz input frequency and 115 V AC input voltage. The measured input DM current spectrum of both prototypes for all six designs and EMI standards are shown in Figs. 6.44 - 6.49. As shown, by adding a common mode (CM) filter in Prototype 2, the DM noise is effectively attenuated due to the cross-coupling between CM and DM noise,
Table 6.3: Summary of the CM filter design for the Vienna-type rectifier.

<table>
<thead>
<tr>
<th>Component</th>
<th>Design parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM choke</td>
<td></td>
</tr>
<tr>
<td>Inductance value ((\mu H))</td>
<td>230</td>
</tr>
<tr>
<td>Core part number</td>
<td>Vac T60006-L2015-W865</td>
</tr>
<tr>
<td>Windings</td>
<td>9 turns of AWG 19</td>
</tr>
<tr>
<td>CM capacitors</td>
<td></td>
</tr>
<tr>
<td>Capacitance value ((nF))</td>
<td>10</td>
</tr>
<tr>
<td>Component</td>
<td>EPCOS 32911</td>
</tr>
<tr>
<td>(R_{CMdamp} (\Omega))</td>
<td>1</td>
</tr>
</tbody>
</table>

which is identified as mixed-mode noise [104]. The mixed-mode noise occurs due to circuit asymmetry caused by the tolerance of components, and can be attenuated by adding a CM filter. The design of the CM filter is summarized in Table 6.3.

In all six designs, however, with and without CM filters, line-current noise complies with the standard within the conducted EMI frequency range (150 kHz \(\sim\) 30 MHz); this validates the design of the input EMI filter.

![Grounding arrangement for EMI measurement setup.](image)
6.6. System Design Flow with UQ

Figure 6.44: Input current spectrum for Design 1a (Prototype 1&2) and EMI standard.

Figure 6.45: Input current spectrum for Design 2a (Prototype 1&2) and EMI standard.

Figure 6.46: Input current spectrum for Design 3a (Prototype 1&2) and EMI standard.
Figure 6.47: Input current spectrum for Design 4a (Prototype 1&2) and EMI standard.

Figure 6.48: Input current spectrum for Design 5a (Prototype 1&2) and EMI standard.

Figure 6.49: Input current spectrum for Design 6a (Prototype 1&2) and EMI standard.
The temperature is measured by an FLIR E40 thermal camera to evaluate the thermal performance of the converter prototype. The thermal graphics of the converter prototypes under full-load operation, when the temperature of all devices have reached steady state, are shown in Figs. 6.50 - 6.55. According to the recorded temperature for all designs at nominal output power and at lab ambient temperature without active cooling, the hottest spot appears on the diode. In all scenarios, the case temperatures of the diodes and MOSFETs remain below their maximum temperature limit (175 °C), and thus, safe operation of the devices is verified.

If the ambient temperature is higher, e.g., 70 °C, assuming the loss of the device is kept the same, a 45 °C increase in junction temperature is expected. This results in over 150 °C junction temperature, which is marginal for safe operation. However, the surface temperatures of other components such as boost inductors, DM inductors, and filter capacitors are far below their limits.
Figure 6.50: Temperature distribution of the converter Prototype 1 (a) based on (b) Design 1a and (c) Design 1b; Prototype 2 (d) based on (e) Design 1a and (f) Design 1b.
Figure 6.51: Temperature distribution of the converter Prototype 1 (a) based on (b) Design 2a and (c) Design 2b; Prototype 2 (d) based on (e) Design 2a and (f) Design 2b.
Figure 6.52: Temperature distribution of the converter Prototype 1 (a) based on (b) Design 3a and (c) Design 3b; Prototype 2 (d) based on (e) Design 3a and (f) Design 3b.
Figure 6.53: Temperature distribution of the converter Prototype 1 (a) based on (b) Design 4a and (c) Design 4b; Prototype 2(d) based on (e) Design 4a and (f) Design 4b.
Figure 6.54: Temperature distribution of the converter Prototype 1 (a) based on (b) Design 5a and (c) Design 5b; Prototype 2 (d) based on (e) Design 5a and (f) Design 5b.
Figure 6.55: Temperature distribution of the converter Prototype 1 (a) based on (b) Design 6a and (c) Design 6b; Prototype 2 (d) based on (e) Design 6a and (f) Design 6b.
Finally, for efficiency measurements, input and output power are measured by a Yokogawa PZ4000 power analyzer. All tests are conducted with about 1.25 kW input power, 115 V ac input voltage, and 400 Hz input-line frequency. For each design, efficiency measurements are done on two different hardware prototypes. In each run, the efficiency data was recorded for 15 cycles at steady state when the temperature of all the devices reached steady state (after 30 minutes of full-load operation) for a period of 90 seconds. The mean value of those measurements is then used as the recorded efficiency. This measurement was repeated in another run for each prototype. Figs. 6.56 - 6.61 show the CDF from the measured efficiency for Designs 1(a, b) - 6(a, b) at nominal output-power.

Figure 6.56: CDFs of measured efficiency for Designs 1a and 1b.

Figure 6.57: CDFs of measured efficiency for Designs 2a and 2b.
Figure 6.58: CDFs of measured efficiency for Designs 3a and 3b.

Figure 6.59: CDFs of measured efficiency for Designs 4a and 4b.

Figure 6.60: CDFs of measured efficiency for Designs 5a and 5b.
6.6.2.3 Modified Area Validation Metric

In this section, the CDF from experimental measurements (Section 6.6.2.2), together with the CDF from simulation results (Section 6.6.1), are used to estimate the MF error associated with each design point. MAVM is used for this purpose where $d^-$ and $d^+$ are calculated for each design. The MF error ($\epsilon_{MF}$) is then calculated using the equation below.

$$\epsilon_{MF} = d^+ - d^- \quad (6.18)$$

The calculated MF error is then normalized with respect to the mean value of the loss distribution obtained from simulation results:

$$\epsilon_{MFnorm} = \frac{\epsilon_{MF}}{\mu_{Loss}} \times 100 \quad (6.19)$$

This value indicates the percentage of MF error at each design point.
The CDF from experiment and simulation results indicating $d^{-}$ and $d^{+}$ for all twelve validation experiments are shown in Figs. 6.62 - 6.67. The normalized MF error for all twelve design points is also summarized in Table 6.4.

Figure 6.62: CDFs of the total loss from simulation and experiment for (a) Design 1a and (b) Design 1b indicating MFU ($d^{-}$, blue-shaded region, and $d^{+}$, red-shaded region).

Figure 6.63: CDFs of the total loss from simulation and experiment for (a) Design 2a and (b) Design 2b indicating MFU ($d^{-}$, blue-shaded region, and $d^{+}$, red-shaded region).
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Figure 6.64: CDFs of the total loss from simulation and experiment for (a) Design 3a and (b) Design 3b indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).

Figure 6.65: CDFs of the total loss from simulation and experiment for (a) Design 4a and (b) Design 4b indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).
Figure 6.66: CDFs of the total loss from simulation and experiment for (a) Design 5a and (b) Design 5b indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).

Figure 6.67: CDFs of the total loss from simulation and experiment for (a) Design 6a and (b) Design 6b indicating MFU ($d^-$, blue-shaded region, and $d^+$, red-shaded region).
Chapter 6. Multi-Objective Design Optimization of a Vienna-Type Rectifier

Table 6.4: Calculated MF error for the training dataset.

<table>
<thead>
<tr>
<th>Design</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>a</td>
<td>b</td>
<td>a</td>
<td>b</td>
<td>a</td>
<td>b</td>
</tr>
<tr>
<td>$\epsilon_{MF_{norm}}$ (%)</td>
<td>10.03</td>
<td>8.460</td>
<td>7.480</td>
<td>6.380</td>
<td>11.40</td>
<td>9.910</td>
</tr>
<tr>
<td>$\epsilon_{MF}$ (W)</td>
<td>1.592</td>
<td>1.418</td>
<td>1.193</td>
<td>1.069</td>
<td>1.948</td>
<td>1.823</td>
</tr>
</tbody>
</table>

It should be noted that to use one factor DOE, it was assumed that the estimated losses of components are independent of one another. If the assumption is valid, then the MF error for Design 4 should be able to be calculated based on Design 1, 2, and 3. To this end, the MF error for Design 4 is estimated based on the measured MF error for Designs 1, 2, and 3, as follows:

$$
\epsilon_{MF_{norm4}} = \epsilon_{MF_{norm1}} + \Delta \epsilon_{MF}(Diode_{1,2}) + \Delta \epsilon_{MF}(MOSFET_{1,2}) \\
= \epsilon_{MF_{norm1}} + (\epsilon_{MF_{norm2}} - \epsilon_{MF_{norm1}}) + (\epsilon_{MF_{norm3}} - \epsilon_{MF_{norm1}})
$$

According to MF error of Design 1, 2, and 3, the MF error for Designs 4a and 4b is estimated to be 1.5488 W (8.85 %) and 1.4749 W (7.89 %), respectively, which match the measured values directly from Design 4. This verifies the assumption made in Section 6.6.2.1.

As seen, overall, the MF error is significant, and for most of the cases the model is underestimating the total converter loss. However, its percentage varies depending on the value combinations of design parameters. The observed trend in the measured MF errors reveals that the MF error is perhaps due to the poor thermal model used in the MDO framework. In other words, as the expected temperature-rise for a design increases/decreases,
the thermal model fails to provide an accurate estimate of the expected change in parameter values. This result will be further discussed in Section 6.8. Also, the contribution of auxiliary circuit components to the total losses and the traces in the PCB board were not considered in the design, which would also result in underestimating the loss.

6.6.2.4 Gaussian Process Regression

The training data set in this case contains five variables, of which the diode and MOS-FET are categorical variables, and switching frequency, boost inductance value, and boost inductor-core size are numerical variables. As discussed in Chapter 5, a GP regression model needs to be built to estimate an MF error for all design points in the performance space based on validation results of the selected design points, as follows:

\[ \epsilon_{MF_{\text{norm}}}(\mathbf{x}) \sim GP(m(\mathbf{x}), k(\mathbf{x}, \mathbf{x}')), \]  

(6.21)

where \( \mathbf{x} \) is the vector of a feasible design points in the performance space, and \( \mathbf{x}' \) is the vector of training dataset. Following the procedure described in Appendix C, parameters for estimating mean and covariance functions are estimated using the training dataset. GP finally defines a posterior distribution over all possible functions conditioned on the training dataset. A 95 % prediction interval is selected to calculate an error bound for the estimated MF errors. In this case, the training dataset is considered to be noisy due to inevitable measurement errors. As a result, the error bound would not be zero at the training data points but has its minimum value. Moving away from the training data points, the error bound increases. More training data points are hence required to reduce the error bound associated with the estimated MF errors.

To provide an insight into the relationship between estimated MF error using GP and
design variables, for a given diode and MOSFET, predicted MF error versus the boost inductance value and boost core size for two different switching frequencies, predicted MF error versus the switching frequency and boost inductance value for two different core sizes; the predicted MF error versus the switching frequency and boost core size for two different boost inductance values are shown in Figs. 6.68, 6.69, and 6.70, respectively. To better demonstrate the aforementioned effect of not having enough training data points, the MF error versus core size and inductance value is also plotted for a given diode and MOSFET in cases where no training data is available. For the last plot, it is indicated that the error bound is overall greater than the error bound in similar plots shown in Fig 6.71.

Figure 6.68: Mean of the estimated MF error (blue plane) and its 95% PI (yellow planes) versus boost inductor-core size and boost inductance value for MOSFET 600N25N3, diode 20G65C5, at (a) 64 kHz and (b) 76 kHz; red points indicate the training data points.
Figure 6.69: Mean of the estimated MF error (blue plane) and its 95% PI (yellow planes) versus switching frequency and inductance value for MOSFET 600N25N3, diode 20G65C5, and (a) 9440 $mm^3$ boost inductor-core size and (b) 25800 $mm^3$ boost inductor-core size; red points indicate the training data points.

Figure 6.70: Mean of the estimated MF error (blue plane) and its 95% PI (yellow planes) versus switching frequency and boost core size for MOSFET 600N25N3, diode 20G65C5, and (a) 410 $\mu H$ boost inductance value and (b) 450 $\mu H$ boost inductance value; red points indicate the training data points.
The estimated loss and total sensitivity of each point in the performance space is finally modified using (5.16) and (5.15). Figure 6.72 illustrates the modified performance space and the realized Pareto Front.

As seen, by adding the MF error, the final performance space and the resultant Pareto Front are changed compared to those obtained by the MDO with P-UQ. According to the results from validation experiments, the estimated loss for the selected optimum design solution based on MDO with P-UQ was actually incorrect by around 2 W. After correcting the loss models by adding the error term to them, so that the models now match the experiments, the preselected optimum design point based on MDO with P-UQ is outperformed by another design, which was not previously realized as a Pareto-optimal solution. A new design is hence selected that features 17 W loss and a footprint area of 12.2 in\(^2\). This design is found to have better performance overall as compared to the optimum designs that were selected based on conventional MDO and MDO with P-UQ. Table 6.5 summarizes the actual
performance measure of the selected optimum design based on the conventional MDO, MDO with P-UQ, and MDO with P&MF-UQ.

As mentioned in Chapter 5, MF error affects constraint conditions as well; as a result, in the new performance space the number of feasible designs is reduced by 20%. The number of Pareto-optimal designs is also increased by 15%. It should be noted that not all the Pareto-optimal designs from the MDO with P-UQ approach are among the new Pareto-optimal design solutions. This further emphasizes the necessity of including P&MF-UQ analysis in the MDO, as without considering these sources of uncertainty, an incorrect non-optimum design solution might get selected.

Despite all the long-term benefits of incorporating UQ into the MDO, the main drawback of this approach is its initial high cost regarding both computation and hardware prototyping. In this case, the computational cost for the MDO with UQ is 442 core hours. Whereas this value for the MDO without UQ is 0.63 core hour.

Figure 6.72: Enhanced performance space and the resultant Pareto Front for the Vienna-type rectifier, where the red colormap corresponds to MDO with P-UQ and the blue colormap corresponds to MDO with P&MF-UQ.
6.8 Discussion

Table 6.6 summarizes the key design variables of the selected optimum designs based on the conventional MDO, MDO with PU-Q and MDO with P&MF-UQ. This section discusses how incorporating P-UQ and MF-UQ analyses into the MDO results in realizing a different set of design variable values in the final optimum design solution.

According to simulation results, the estimated loss for Diode 1 is slightly higher than that of Diode 2, and MOSFET 2 is expected to have significantly higher loss compared to MOSFET 1. Therefore, in the MDO without UQ, MOSFET 1 and Diode 2 are selected as the semiconductor devices to minimize the total converter loss. It should be noted that, since the MOSFET and diode selection in this case does not affect the size of the converter, no compromise between loss and size needs to be made in the selection of semiconductor devices. The switching frequency, boost inductor core size, and boost inductance values are, however, selected based on a compromise between loss and size.
In the design with P-UQ, it is found that the design becomes less sensitive to tolerances by simultaneously decreasing the switching frequency and increasing the boost inductance value. Therefore, in the selected optimum design solution based on MDO with P-UQ the switching frequency is reduced to 64 kHz and the inductance value is increased to 410 $\mu$H. In this case, MOSFET 2 is selected, which slightly increases the nominal loss of the converter, resulting in a decrease in the sensitivity of the design. The effective loss of this design, however, i.e., the product of sensitivity index and nominal loss, is lower than what occurs in the design that was selected based on the conventional MDO. In other words, the selected design based on P-UQ has a better performance overall as compared to the design that was selected based on the conventional MDO.

Finally, according to validation experiments and estimated MF errors, it is found that the developed converter loss model is not accurate; it is, in fact, off by about 2 W on average over the performance space. Specifically, it is found that the actual loss of Diode 1 is significantly lower than Diode 2. Therefore, in the new optimum design, Diode 1 is selected. In addition, according to validation experiments, the actual loss difference between MOSFET 1 and MOSFET 2 is less than the predicted values from simulation results; in reality, MOSFET 2 will not cause any significant increase in the nominal loss of the converter. Therefore, in the final design, MOSFET 2 remains as the selected device to maintain low sensitivity index without a significant increase in the nominal loss. According to validation experiments, it is also shown that for the same core size, increasing the inductance value will, in fact, significantly increase core and conduction losses. Therefore, there is a compromise between design sensitivity and the converter loss, which should be considered when increasing the inductance value. As a result, in the final design selection, the inductance value is reduced to 390 $\mu$H, which allows the nominal loss to be reduced with a slight increase in the sensitivity index, as compared to the design selected based on MDO with P-UQ.
Notably, from the MF error estimated for six design cases, it can be concluded that the thermal model needs to be improved, as there is a relationship between the expected temperature rise and the calculated error. For the boost inductor, in particular, it can be concluded that the thermal model performs poorly. When comparing the MF error for Designs 5 and 1, it can be seen that once a smaller core is selected (although it has been assumed that all cores are large enough to dissipate the thermal loss), the temperature rise is in fact significant and has affected the temperature-dependent parameters and total loss accordingly.

Table 6.5: Performance measures of the selected optimum design based on conventional MDO, MDO with P-UQ, and MDO with P&MF-UQ.

<table>
<thead>
<tr>
<th>MDO approach</th>
<th>Without UQ</th>
<th>With P-UQ</th>
<th>With P&amp;MF-UQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (inch²)</td>
<td>21.58</td>
<td>21.58</td>
<td>21.58</td>
</tr>
<tr>
<td>Loss (W)</td>
<td>14.02</td>
<td>14.10</td>
<td>14.14</td>
</tr>
<tr>
<td>$S_T$ (%)</td>
<td>49.70</td>
<td>30.6</td>
<td>31.18</td>
</tr>
<tr>
<td>Loss' (W)</td>
<td>15.94</td>
<td>15.65</td>
<td>15.17</td>
</tr>
<tr>
<td>$S_T'$ (%)</td>
<td>43.71</td>
<td>27.84</td>
<td>29.10</td>
</tr>
</tbody>
</table>
Table 6.6: Key design variables of the selected optimum design based on conventional MDO, MDO with P-UQ, and MDO with P&MF-UQ.

<table>
<thead>
<tr>
<th>Design</th>
<th>Without UQ</th>
<th>With P-UQ</th>
<th>With P&amp;MF-UQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>MOSFET</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Boost inductor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductance value ($\mu H$)</td>
<td>330</td>
<td>410</td>
<td>390</td>
</tr>
<tr>
<td>Core size ($mm^3$)</td>
<td>25800</td>
<td>25800</td>
<td>25800</td>
</tr>
<tr>
<td>Airgap length ($mm$)</td>
<td>0.54</td>
<td>0.64</td>
<td>0.62</td>
</tr>
<tr>
<td>Number of turns</td>
<td>21</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>DM inductor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductance value ($\mu H$)</td>
<td>24.4</td>
<td>25.5</td>
<td>26.1</td>
</tr>
<tr>
<td>Core size ($No$)</td>
<td>19</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>Airgap length ($mm$)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Number of turns</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Damping resistor ($\Omega$)</td>
<td>1</td>
<td>0.5</td>
<td>2</td>
</tr>
<tr>
<td>Switching frequency (kHz)</td>
<td>68</td>
<td>64</td>
<td>64</td>
</tr>
</tbody>
</table>
6.9 Conclusion

In this chapter, MDO with P&MF-UQ was applied to the design optimization of a Vienna-type rectifier, with regards to its primary performance measures, i.e., loss and size, and the total sensitivity, while considering specific design constraints, operation requirements, and modeling inaccuracies. The total sensitivity in this approach is an aggregated measure of robustness for performance indices. Therefore, minimizing the total sensitivity results in minimization of loss and size variations individually, while favoring loss due its higher weighting factor.

The final optimum design was realized by exploring the system sensitivity-loss-size Pareto Front of the enhanced performance space, where the MF error associated with each design was used to modify the estimated performance measures; the parametric sensitivity of each design point was used to discern between cases and to help identify the most parametrically robust of the Pareto-optimal solutions. For comparison purposes, the results of the traditional formulation and MDO with P-UQ were also illustrated.

An advantage of including P&MF-UQ in the design is that even when the model used in the MDO is not accurate, this approach quantifies the inaccuracy of the model and modifies the performance space accordingly to select the actual optimal design solution. MF estimation will also provide insights into any fidelity improvements needed in the model to reduce the uncertainty for future design iterations.

The main conclusion drawn from the results provided in this chapter is that the MF error and sensitivity of each design point could potentially change the performance space and its resultant Pareto Front. Thus, ignoring these main sources of uncertainty in the design will result in wrong decision-making and could potentially lead to choosing a design that is not optimum in practice.
Chapter 7

Conclusions and Future Work

Modeling and simulation are essential tools in the analysis, design, and optimization of power electronics converters and systems. Advances in computing power over the past few decades have set the stage for a major step forward in modeling and simulation. Reduction in power circuit simulation computation times, in particular, has made it practical to use simulation environments to conduct a numerical design of experiments. This, in turn, has enabled the conduction of reliability and production yield analyses to assess design robustness for a certain period of time and in the presence of parameters tolerances. The trustworthiness of all the model-based design techniques, however, depends entirely on the accuracy of the simulation models used, which has not been fully considered thus far.

Accordingly, this research has strived to formulate a modeling process with uncertainty quantification (UQ) to bridge the modeling and simulation accuracy and reliance gaps that have hindered the full exploitation of model-based design techniques. This modeling framework ultimately pursues a reduced level of dependence on experimental results, as well as to empower the role of modeling and simulation results in the design and decision-making processes. The proposed modeling framework is able to quantify the deviation of the real
system performance from predictions made using modeling and simulation, a capability that is attained by the proper identification, characterization, and quantification of the different, and often numerous, sources of uncertainty. There are, in fact, two main sources of uncertainty in the modeling and simulation of power converters that are addressed through this framework: parametric uncertainty, which results from manufacturing variability, and model-form uncertainty, which results from the inherent inaccuracies of the models used.

A design methodology with parametric and model-form uncertainty (design with P&MF-UQ) is proposed accordingly, representing a desirable alternative to the design of power electronics converters and systems. Unlike other model-based design techniques, this approach considers modeling inaccuracies as well as the parameter tolerances in determining the required design margin. This type of design approach would expectedly yield less conservative and more dependable designs without requiring any additional resources, yet will effectively eliminate the need for heuristic safety factors yielding quantifiably more precise designs, capable of truly maximizing the power-processing capability of the devices at hand. Design with P&MF-UQ is applied to the modeling of a power electronics building block (PEBB) used in a modular power converter; the results obtained fully evince the extent of the capabilities attained by the proposed modeling framework in the design of power electronics converters and systems. In this study, the variations in system input parameters was limited to aleatory uncertainty. In the future, additional computation loops can be added to the UQ analysis to propagate epistemic uncertainties throughout the model instead of fixing them under the worst-case condition. The significant gains in a design should also be demonstrated, such that modeling and design with P&MF-UQ can be systematically applied to new designs.

The presented work demonstrates that the implementation of the proposed modeling approach can also handle complex power converters and systems. The approach requires
only the development of a simplified testbed for UQ analysis without introducing any additional uncertainties. To demonstrate its feasibility, this modeling approach is applied to the switching model of a PEBB-based modular multilevel converter (MMC) as an example of a complex power converter. Sensitivity analysis is first conducted to minimize the number of uncertain parameters. The relationship between the different sources of uncertainties and the number of PEBBs in each arm is then investigated, and a phase-leg with one PEBB per arm is introduced as a simplified testbed for UQ analysis of an MMC. The enhanced modeling framework with P&MF-UQ was, in fact, able to improve the existing modeling practice and to validate the model used in the design of an MMC. Accordingly, a simplified testbed for UQ analysis and model validation of the PEBB in the design of an MMC was developed. In the future, similar studies should be conducted for systems with a non-orthogonal uncertain input space, where Monte Carlo sampling and sensitivity analysis studies pose additional challenges.

The methodology is then extended to multi-objective design and optimization. This research also proposes a robust multi-objective design and optimization approach with parametric and model-form uncertainty quantification (MDO with P&MF-UQ) in which the sensitivity index is formulated as a new performance measure. The sensitivity index is defined as a quantitative measure of system design robustness in the presence of both parametric and model-form uncertainties which consequently will provide a comprehensive design criterion to enable the selection of the most robust Pareto-optimal design solution. A complete mathematical formulation of this design optimization technique is provided. Application of the proposed formulation is not limited to power electronic converters and can potentially be applied to ordinary differential equation (ODE)-based models in any other application areas. Similar to MDO analysis, reliability studies are also based on model-based techniques which suffer from the same limitations in the previous modeling and simulation practice. In
the future, similar studies can be conducted to improve the existing reliability frameworks in the field of power electronics.

Finally, to demonstrate the benefits of incorporating UQ analysis in MDO from a more practical standpoint, the Vienna-type rectifier is used as a case study to compare the theoretical analysis with a comprehensive experimental validation. The final optimum design is realized by exploring the Pareto Front of the enhanced performance space of the system, where the model-form error associated with each design is used to modify the estimated performance measures, and parametric sensitivity of each design point is used to discern between cases and to help identify the most parametrically-robust of the Pareto-optimal solutions. This research shows that the model-form error and sensitivity of each design point can potentially change the performance space and resultant Pareto Front for which the results of conventional MDO are illustrated. As a result, ignoring these main sources of uncertainty in the design will result in wrong decision making and in the choosing of a design that is not optimized in practice. It is also shown how model-form error estimation would also provide insight into any fidelity improvements needed in the model to reduce the uncertainty in the next iterations of a design. In the future, the feasibility of the proposed MDO approach should be explored in the case of complex systems where employing surrogate models may become necessary.
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Appendices
Appendix A

Mathematical Modeling and Control of the MMC

A.1 Mathematical Modeling

The equivalent circuit of one phase of an MMC, shown in Fig. A.1, is used for the analysis provided in this section; the other two phases have a similar behavior. The following equations can be obtained by Kirchhoff’s voltage law (KVL):

\[
\frac{1}{2} V_{dc} = u_{upj} + R_{up} i_{upj} + L_{upj} \frac{di_{upj}}{dt} + u_{oj}, \tag{A.1}
\]

\[
\frac{1}{2} V_{dc} = u_{lwj} + R_{lw} i_{lwj} + L_{lwj} \frac{di_{lwj}}{dt} - u_{oj}, \tag{A.2}
\]

where \( u_{oj} \) is the output voltage of phase \( j \) \((j \in \{a, b, c\})\), \( i_{oj} \) is the phase current, \( V_{dc} \) is the dc link voltage; \( u_{upj}, i_{upj}, u_{lwj}, \) and \( i_{lwj} \) represent the voltages and currents of the upper and lower arms; \( R_{up}, R_{lw}, L_{up}, \) and \( L_{lw} \) are the resistances and inductances of the upper and
lower arms, respectively. Therefore, the expression for output voltage can be derived as

\[ u_{oj} = \frac{1}{2}(u_{twj} - u_{upj}) \]  \hspace{1cm} (A.3)

Furthermore, \( i_{Zj} \) is defined as the circulating current along the \( j \)-phase and based on the definition, it only circulates in-between phase-legs without flowing to the dc bus or the ac line. The circulating current along the \( j \)-phase can be given by

\[ i_{circj} = \frac{1}{2}(i_{upj} - i_{twj}) \]  \hspace{1cm} (A.4)

Finally, the arm currents can be expressed in terms of the circulating current and the phase current as follows.

\[ i_{upj} = i_{circj} + \frac{1}{2}(i_{oj}) \]  \hspace{1cm} (A.5)

\[ i_{twj} = i_{circj} - \frac{1}{2}(i_{oj}) \]  \hspace{1cm} (A.6)
A.2 Modulation Implementation

The phase-shifted carrier modulation technique, shown in Fig. A.2, is used in this work, where the $N$ triangular carriers of upper/lower arms ($C_{u1}, C_{u2}, ..., C_{uN}$ for the upper arm, and $C_{w1}, C_{w2}, ..., C_{wN}$ for the lower arm) are shifted by $\pi/N$ incrementally to achieve the best harmonic cancellation [32]. Accordingly, each PEBB is assigned with a specific reference signal and a triangular carrier, such that all PEBBs have the same switching frequency and the semiconductor stress is evenly distributed. The switching pulses of each PEBB are generated by comparing the reference signals with the corresponding carrier wave. The reference signals of the upper and lower PEBBs are given by

$$u_{ref1_{lwj}}(i) = \frac{3V_{dc}}{4} + \frac{MV_{dc}}{4} \cos(\omega_o t + \phi_j) + \Delta u_{ref lwj}(i), \quad (A.7)$$

$$u_{ref2_{lwj}}(i) = \frac{V_{dc}}{4} + \frac{MV_{dc}}{4} \cos(\omega_o t + \phi_j + \pi) - \Delta u_{ref lwj}(i), \quad (A.8)$$

$$u_{ref1_{upj}}(i) = \frac{3V_{dc}}{4} + \frac{MV_{dc}}{4} \cos(\omega_o t + \phi_j + \pi) + \Delta u_{ref lwj}(i), \quad (A.9)$$

$$u_{ref2_{upj}}(i) = \frac{V_{dc}}{4} + \frac{MV_{dc}}{4} \cos(\omega_o t + \phi_j) - \Delta u_{ref lwj}(i), \quad (A.10)$$

where $M(0 \leq M \leq 1)$ is the modulation index, $\omega_o$ is the angular frequency of the output ac voltage, $\phi_j$ is the phase angle, and $\Delta u_{ref lwj}(i)$ and $\Delta u_{ref lwj}(i)$ are the reference adjustments, which are obtained by the voltage balancing control method discussed later in Section A.3.

It should be noted that the difference between the phase angle of the triangular carrier in the lower and upper arms, known as displacement angle denoted by $\theta$ in Fig. A.2, has a significant impact on the harmonic features of the output voltage and the circulating current. According to the double Fourier series analysis, the harmonics of the circulating current will be minimized when the displacement angle is $\pi/N$ and 0 degrees for the converter with odd
A.3 Control Scheme

As the PEBBs of the MMC are modulated independently, the voltage balancing of the capacitors can be achieved by adjusting the reference signal of each PEBB. The complete block diagram of the capacitor voltage balancing method is shown in Fig. A.3. The controller used in this section is adapted from [27] and is composed of an averaging controller together with a voltage balancing block.

As shown in Fig. A.3a, the balancing controller balances individual PEBB voltages with respect to their reference value. Whereas the averaging controller (Fig. A.3b) forces the $j$-phase average voltage ($\bar{v}_{cj}$) to follow its command ($v^*_c$). An ac circulating current control
loop (a proportional-resonant (PR) controller [82]) with the reference of zero, is also added to the balancing controller to suppress the second order harmonics of the circulation current with minimum effect on the original system performance. Finally, based on the averaging and balancing controller commands, the reference adjustments of each PEBB used in (A.7)-(A.10), are calculated as below:

\[
\Delta u_{ref1_upj}(i) = v_{Aj}^* + v_{Bj}^*(i) \quad (A.11)
\]

\[
\Delta u_{ref1_lwj}(i) = v_{Aj}^* + v_{Bj}^*(i) \quad (A.12)
\]
Appendix B

Hardware Prototype of the MMC

Figure B.1 depicts one of the six PEBB units built where the PEBB planar dc bus structure, film capacitor bank, gate-driver units with high-EMI immunity, and dual-purpose differential and common-mode inductors are observed. Each PEBB has a power rating of 7.5 kW and a dc bus voltage rating of 1 kV.

Given the dc bus voltage and arm current rating, the CAS300M17BM2 SiC MOSFET half-bridge modules from Cree are selected due to their superior performance in fast switching speed, low switching loss, and high operating temperature. Fast switching speed enables an increase of the switching frequency and, accordingly, the design of a high-power density PEBB. To this end, the gate driver in this prototype is particularly designed for the maximum driving speed, and 100 V/ns dv/dt noise immunity, as well as fast and effective short-circuit protection to accommodate the high switching frequency design of the PEBB [92].

According to the maximum allowed voltage ripple on PEBB dc bus voltage, the minimum required capacitance is calculated such that the safe operation of a power electronic device and the functionality of the converter is assured [5, 106]. The voltage rating of the
Appendix B. Hardware Prototype of the MMC

The capacitor bank should be at least 1.7 kV to guarantee the safe operation during the transient. The current rating of the capacitor bank should be at least 30 A based on converter specifications. Finally, two Cornell Dubilier Electronics (CDE) 420 uF capacitors rated at 900 V dc and 75 A are connected in series to meet the requirements.

The role of the arm inductors in the MMC is to suppress any high-frequency components of the arm currents caused by differences in upper and lower arm voltages. In addition, there are resonance frequencies associated with intrinsic even order harmonics (mainly second and fourth order harmonics) of the circulating current [103]. Hence, the arm inductance value needs to be far away from the corresponding inductance to the resonance points. To minimize the size of the arm inductors, the ac filter inductor is added to the ac side, and the circulating current suppression control is used. The arm inductance and ac inductance are designed to be 1 \( mH \) and 1.5 \( mH \). As shown in Fig. B.1, the arm inductance is distributed between two ac terminals for common-mode considerations. Due to their high saturation flux density (1.56 T), amorphous cores, AMCC 630 and AMCC 1000 are used to build the arm and ac
Figure B.2: MMC hardware prototype (a) front view (b) back view.
Appendix B. Hardware Prototype of the MMC

inductors, respectively. The number of turns and air gap length for arm and ac inductors are calculated as 38 turns - 5.4 mm and 40 turns - 4.3 mm, respectively [20].

The primary role of the dc planar busbar in a PEBB is to achieve series or parallel configuration of the capacitors and to link the dc capacitor bank and power modules. Planar busbar has shown to be an effective technology to reduce the interconnection inductance, improve thermal performance, and achieve a compact PEBB design [54]. Achieving a low stray inductance is, in fact, extremely important in the design of a SiC-based PEBB. Because of the high-speed switching transients, a large stray inductance in the PEBB may cause excessive transient voltage overshoots across the MOSFETs, resulting in increased power loss and high voltage stress that may result in exceeding the MOSFET safe operating range.

There are two main types of layers in the construction of the busbar; the conductor layer and the insulation layer. An additional layer is also added as the outer layer to improve the mechanical strength of the busbar.

Conductor material selection is critical in meeting electrical performance and mechanical rigidity requirements. Copper is selected as the conductor due to its excellent electrical conductivity as well as its mechanical strength. The dimensions of the copper plates and the size of the holes are determined by the overall layout of the busbar. However, the minimum clearance distances and the thickness of the conductive layer are determined by voltage and current ratings of the busbar, respectively. Based on the specification of the PEBB and busbar, a standard copper sheet with thickness of 1.27 mm is selected and a 5 mm clearance distance is used in the design of the busbar.

There are several types of insulation materials that could be used in manufacturing busbars. In this design, Kapton tape is used due to its excellent dielectric strength. The minimum thickness of the insulation layers is determined by the dielectric strength of the
insulation material and the voltage rating of the busbar. The thickness of the Kapton tape used in this busbar is 0.025 mm.

An additional outer layer is added to the busbar to increase its mechanical strength. For this busbar, flame-retardant multipurpose garolite (G-10/FR4) is used for its excellent impact strength. Since this outer layer will not affect the stray inductance of the busbar, it can be made thick enough to provide sufficient mechanical strength for the application. Finally, epoxy adhesive is used to bond the layers of the busbar together.

The final structure of the busbar is shown in Fig. B.3 with a focus on the structure near a hole for positive terminal connection. It should be noted that a decoupling capacitor is also connected at the terminal of the switching device to further decrease the interconnection inductance. The final loop inductance from Q3D simulation and measurement is 11.91 nH and 12.82 nH, respectively.

To ensure that all of the components in the converter operate below their maximum rated temperature, the thermal model of the converter is developed. According to the simulation results, switching devices are the largest contributors to the total loss of the converter. Wakefield-Vette 511-6U heat sink is selected due to its low thermal resistance and compact size. A fan is also used to provide enough air flow to achieve forced convection for the heat sink. Using the thermal resistance provided by the datasheets, the maximum junction temperature of the switching device is about 70 °C, which is much lower than the
maximum rated value (150 °C).

According to the aforementioned control method in Appendix A, 16 sensing feedback channels are required, comprised of 6 PEBB capacitor voltages, 6 arm currents, 3 ac bus voltages, and 1 dc bus voltage. The LEM LF 205-S/SP3 current sensor is used to sense the arm current and can be observed in Fig. B.1. The LEM LV 25- P/SP5 voltage sensor is used to sense all of the voltages and can be observed on the sensor board in Fig. B.2. The rest of the required signals for the control of the MMC, such as the circulating currents, ac currents, and average PEBB capacitor voltages can be calculated using the measured value of the 16 sensed signals.

The sensing information is then transferred to a central controller. The central controller features a Texas Instruments TMS320C28343 Delfino Microcontroller (MCU) and a Lattice LCMX02-4000HC Complex Programmable Logic Device (CPLD) to process the control calculation tasks described in Section A.3. The central controller finally generates twelve pairs of complementary gate signals with 400 ns of deadtime. Twenty-four gate signals are grouped in such a way that each group of four gate signals are intended for the switching devices of one PEBB. Six groups of gate signals are finally sent to the PEBBs through six optical fiber interface boards.
Appendix C

Gaussian Process

There are several linear and nonlinear regression approaches for estimating a system behavior. In most of the cases, there is a set of observed data which can be used to train a function to estimate the system response when no data is available. These observations are called the training data. The goal of regression problems is hence to apply a statistical learning method to the training data to estimate an unknown function.

There are different classifications proposed for regression problems. Most statistical learning methods for this task can be characterized as either parametric or non-parametric which are also referred to as classical or Bayesian approaches, respectively.

The parametric (classical) regression is the most common approach to regression problems and has been used in a variety of application areas. A comprehensive discussion on different parametric regression settings and their implementation is provided in [61]. Parametric methods basically try to find the best fit for a system response. The best fit is ultimately used to make predictions for cases where there system output is not available. As such, parametric approaches involve a two-step model-based approach. First, a series of
assumptions about the functional form of model \( f(.) \) are made, i.e., determine if \( f(.) \) is
linear, quadratic, cubic, polynomial, etc. Once the form of the \( f(.) \) is selected, the problem
of estimating \( f(.) \) is greatly simplified; instead of having to determine an entirely arbitrary
multi-dimensional \( f(.) \), one only needs to estimate parameters associated with the selected
form, known as coefficients, using the training data for which different settings can be used.
The most common approach for estimating the coefficients is referred to as least squares, in
which the coefficients are estimated such that the sum of squared errors is minimized.

Non-parametric methods, on the other hand, do not make explicit assumptions about
the functional form of \( f(.) \); instead, they seek an estimate of \( f(.) \) that gets as close to the
data points as possible without being too rough. In other words, these approaches do not
attempt to identify best fit models of the data. Instead, they compute a posterior distribution
over models. These distributions provide a useful way to quantify the uncertainty in model
estimates and to exploit knowledge of this uncertainty to make more robust predictions on
new test points.

It should be noted that in the case of parametric models, developing complex models
with large number of terms can lead to a phenomenon known as overfitting the data, which
essentially means that models follow the errors, or noise, too closely. Another potential
disadvantage of the parametric approach is the possibility that the selected model is very
different from the true unknown form of \( f(.) \). If the chosen model is too far from the true \( f(.) \),
then any estimate using that model will be poor. Non-parametric approaches completely
avoid these dangers, since essentially no assumption about the form of \( f(.) \) is made. Such
approaches can, in fact, have a major advantage over parametric approaches. By avoiding
the assumption of a particular functional form for \( f(.) \), they have the potential to accurately
fit a wider range of possible shapes for \( f(.) \). Alternately, non-parametric approaches suffer
from a major disadvantage; since they do not reduce the problem of estimating \( f(.) \) to a
small number of parameters, a very large number of observations is required to obtain an accurate estimate for $f(.)$.

This appendix focuses only on the Kernel-based fully Bayesian regression approach known as Gaussian Process (GP) regression, which can be applied in many application areas as it provides a flexible nonparametric regression tool for solving a wide range of problems [15, 47, 73]. Simply put, GP can be used as a prior to random functions; using Bayes law, a posterior distribution on $f(.)$ is ultimately calculated conditioned on the training dataset. This appendix does not go into detail to understand the fundamentals of GP. Instead, the concept and implementation are shown through mathematics and the framework is explained simply and ready to be applied.

GP is a very generic term meaning that any finite collection of observations have a jointly or multivariate normal distribution (MVN); that, in turn, interprets that mean function ($\mu(x)$) and covariance function ($\sum(x, x')$) are the only factors that need to be specified when working with this tool. GPs are, in fact, uniquely determined by their means and covariances.

The majority of the effort in the Gaussian process modeling is in developing the covariance structure where the covariance is defined as a function of distance. Starting with a very simple example, we will define a covariance structure that is a function of Euclidean distance as below:

$$\text{Cov}(Y(x), Y(x')) = \sum(x, x') = \exp\{-||x - x'||\}, \quad (C.1)$$

where output at two different input locations $x$ and $x'$ are modeled as $Y(x)$ and $Y(x')$. According to (C.1), the covariance between two locations decays exponentially as the two input locations become farther apart in the input space, i.e., the covariance matrix is inversely
related to distance. In this specification, if $x$ and $x'$ are the same then the covariance is 1, meaning that they are perfectly correlated.

It is worth noting that a valid covariance matrix ($\Sigma_n$) for MVN, which is based on evaluating $\Sigma(x_i, x_j)$ on pairs of $x_1, x_2, ..., x_n$, must be positive definite as shown below:

$$x^T \Sigma_n x > 0 \quad \text{for all } x > 0$$ (C.2)

Any other functions of distance or other covariance functions can therefore be selected as long as the resulting covariance matrix is a positive definite.

For a selected covariance matrix, random data can be generated following a smooth relationship as

$$Y \sim \mathcal{N}(0, \Sigma_n)$$ (C.3)

A finite realization of a random function under a GP prior with a particular covariance structure can be generated using (C.3) that is $Y(x) \sim \mathcal{GP}(\mu, \Sigma_n)$. In (C.3) since the scale of the covariance is 1, data generated is within [-2,2] with a 95% probability. Also, due to the covariance structure, there will be lots of bumps in the $x$-range that are a result of the covariance structure that determines that short distances are highly correlated, and long distances are essentially uncorrelated. The resultant function, however, is extremely smooth because the covariance function is indefinitely differentiable. The mean of this MVN is assumed to be zero. However, this is not a drastic limitation and can be easily modified; since the mean of the posterior process is not confined to zero.

In the next step, we want to limit the data realization by introducing a set of predefined function values that is the training data set ($D_n$). Following that step, the goal is to determine
the random function realizations that could explain the given training dataset, which is equivalent to the conditional distribution of $Y(x)$ that is a posterior distribution denoted by $Y(x)|D_n$.

Deriving a predictive distribution is a simple application of conditional distributions from a joint MVN. If an $N$-dimensional random vector $x$ is partitioned as

$$x = \begin{pmatrix} x_1 \\ x_2 \end{pmatrix}, \quad (C.4)$$

where $x_1$ and $x_2$ are $q \times 1$ and $(N - q) \times 1$ matrices, respectively, then $\mu$ and $\Sigma_n$ can be partitioned as below:

$$\mu = \begin{pmatrix} \mu_1 \\ \mu_2 \end{pmatrix}, \quad (C.5)$$

$$\Sigma_n = \begin{pmatrix} \Sigma_{11} & \Sigma_{12} \\ \Sigma_{21} & \Sigma_{22} \end{pmatrix}, \quad (C.6)$$

where dimensions of $\mu_1$ and $\mu_2$ are $q \times 1$ and $(N - q) \times 1$. Also $\Sigma_{11}$, $\Sigma_{12}$, $\Sigma_{21}$, and $\Sigma_{22}$ are $q \times q$, $q \times (N - q)$, $(N - q) \times q$, and $(N - q) \times (N - q)$ matrices, respectively.

The distribution of $x_1$ conditional on $x_2$ is $x_1|x_2 \sim N_q(\bar{\mu}, \bar{\Sigma})$, where

$$\bar{\mu} = \mu_1 + \Sigma_{12} \Sigma_{22}^{-1}(x_2 - \mu_2), \quad (C.7)$$

$$\bar{\Sigma} = \Sigma_{11} - \Sigma_{12} \Sigma_{22}^{-1} \Sigma_{21}, \quad (C.8)$$
According to (C.7) and (C.8), conditioning upon $x_2$ decreases the variance of $x_1$ compared to its marginal variance ($\Sigma_{11}$); this will also alter the mean. However, the amount by which the mean and variance are changing does not depend on the value of $x_2$.

Now consider $Y(.)$ with $n' + n$ points; the last $n$ observations are from the training data set ($Y_n$). $Y_n$ ($n \times 1$) and $Y(X)$ ($n' \times 1$) have a joint MVN distribution with mean zero and covariance function $\Sigma(x,x')$. The mean and covariance structure are partitioned as follows.

$$\mu = \begin{pmatrix} Y(X) \\ Y_n \end{pmatrix}$$  \hspace{1cm} (C.9)

$$\Sigma = \begin{pmatrix} \Sigma(X,X) & \Sigma(X,X_n) \\ \Sigma(X_n,X) & \Sigma_n \end{pmatrix}$$  \hspace{1cm} (C.10)

It should be noted that $\Sigma(X,X_n) = \Sigma(X_n,X)^T$. The conditional results for the MVN give us the following predictive distribution:

$$Y(X)|D_n \sim \mathcal{N}(\mu(X), \Sigma(X)),$$  \hspace{1cm} (C.11)

where

$$\mu(X) = \Sigma(X,X_n)\Sigma_n^{-1}Y_n$$  \hspace{1cm} (C.12)

$$\Sigma(X) = \Sigma(X,X) - \Sigma(X,X_n)\Sigma_n^{-1}\Sigma(X,X_n)^T$$  \hspace{1cm} (C.13)

According to (C.13) and the fact that $\Sigma(X,X_n)\Sigma_n^{-1}\Sigma(X,X_n)^T$ is a positive definite
value, $\Sigma(X)$ is lower than $\Sigma(X, X)$. This means $Y_n$ has added knowledge to the algorithm and reduced its variance by an amount which is a function of the distance between $X$ and $X_n$ and does not depend on the value of $Y_n$. Also, the predictive standard deviation is the highest at locations that are farther from the $x_i$ values in the training dataset meaning that the extrapolations too far outside the training data range cannot be relied upon. However their behavior is predictable.

According to (C.13) and the fact that $\Sigma(X, X_n)\Sigma_n^{-1}\Sigma(X, X_n)^T$ is a positive definite value, $\Sigma(X)$ is lower than $\Sigma(X, X)$. This means $Y_n$ is added knowledge to the algorithm and reduces its variance by an amount which is a function of the distance between $X$ and $X_n$ and does not depend on the value of $Y_n$. Also, the predictive standard deviation is the highest at locations that are farther from the $x_i$ values in the training dataset meaning that the extrapolations too far outside the training data range cannot be relied upon. However their behavior is predictable.

So far the amplitude of the function was limited to $[-2,2]$. However, the amplitude of the function is not known in advance and should not be limited to a certain value. Besides, training dataset was assumed to be deterministic. Whereas, in the real cases, the training data set is often noisy. Also, in a multi-dimensional input space, the correlation does not decay uniformly in all directions. To take into account the mentioned considerations, the GP needs to be modified using hyperparameters. The impact of hyperparameters on the overall estimation is more of a fine tuning which is described as follows.

To modify the prior to have random functions which have amplitudes greater than two a scale parameter is introduced, $\tau^2$, which is defined as

$$\Sigma_n = \tau^2 \mathcal{C}_n$$ (C.14)
where $C$ is basically the same as $\Sigma$ meaning that is a correlation function with all previous properties; it only modifies the covariance definition to accommodate scale. There are several approaches available to estimate $\tau^2$ such as the method of moments, likelihood, cross-validation and etc. In this work, likelihood-based methods have been used which can be easily generalized to higher dimensional parameter spaces. In this method, given the data-generating process as below:

$$Y \sim \mathcal{N}(0, \tau^2 C_n) \quad (C.15)$$

the MVN PDF is written as

$$L \equiv L(\tau^2, C) = (2\pi \tau^2)^{-\frac{n}{2}} |C_n|^{-\frac{1}{2}} \exp\left\{-\frac{1}{2\tau^2} Y_n^T C_n^{-1} Y_n\right\} \quad (C.16)$$

the logarithm of (C.16) is finally derived as below:

$$l = \log L = -\frac{n}{2} \log 2\pi - \frac{n}{2} \log \tau^2 - \frac{1}{2} \log |C_n| - \frac{1}{2\tau^2} Y_n^T C_n^{-1} Y_n \quad (C.17)$$

To maximize the likelihood with respect to $\tau^2$, (C.17) needs to be differentiated and solved as follows:

$$\tau^2 = \frac{Y_n^T C_n^{-1} Y_n}{n} \quad (C.18)$$

The predictive equations are modified accordingly:

$$Y(X)|D_n \sim \mathcal{N}_{n'}(\mu(X), \Sigma(X)) \quad (C.19)$$

where
\[ \mu(X) = C(X, X_n)C_n^{-1}Y_n \] 

\[ \Sigma(X) = \tau^2[C(X, X) - C(X, X_n)C_n^{-1}C(X, X_n)^T] \] 

According to (C.20) and (C.30), \( \tau^2 \), which is a function \( Y_n \) values, will only affect the predictive variance and not the predictive mean.

To take into account the effects of noise, another hyperparameters is introduced, \( g \), to determine the size of discontinuity as \( x \) gets closer to \( x' \). This effect is realized as below:

\[ K(x, x') = C(x, x') + g\delta_{x,x'} \]  

\[ \delta_{x,x'} \] is the Kronecker delta function. Note that \( g \) is only added when indices of \( x \) are the same. Equation (C.22) is therefore modified as below:

\[ K(x_i, x_j) = \begin{cases} 
C(x_i, x_j) & \text{when } i \neq j, \\
C(x_i, x_j) + g & \text{when } i = j.
\end{cases} \]  

The data-generating function is accordingly modified as below:

\[ Y \sim \mathcal{N}_n(0, \tau^2(C_n + gI_n)) \]  

Parameter \( g \) is also estimated using the likelihood-based method. However in this case, unlike \( \tau^2 \), there is no closed form solution and maximizing \( l(g) \) should be done numerically.

As a result of introducing noise, unlike previous cases, the error bar at training data location
will not be zero.

In the last step, the correlation decay needs to be modified. Consider the following generalization of the covariance function:

\[ C_\theta(x, x') = \exp\left\{-\frac{||x - x'||}{\theta}\right\} \]  

(C.25)

where the correlation function is indexed by the scalar hyperparameter \( \theta \), called the characteristic length scale. Nevertheless, the correlation does not necessarily decay uniformly in all input directions. Equation (C.25) is therefore modified as below:

\[ C_\theta(x, x') = \exp\left\{-\sum_{k=1}^{m} \frac{(x_k - x'_k)^2}{\theta_k}\right\} \]  

(C.26)

where vectorized lengthscale parameter \( \theta = (\theta_1, ..., \theta_m) \) is used. The corresponding correlation function is called the separable or anisotropic Gaussian. Similar to \( g \), \( \theta \) is also calculated numerically using the likelihood-based approach. The data-generating function is therefore modified as below:

\[ Y \sim \mathcal{N}_n(0, \tau^2(C_n + gI_n)) \]  

(C.27)

Finally, the GP can be derived as below:

\[ Y(X)|D_n \sim \mathcal{N}_n' (\mu(X), \Sigma(X)) \]  

(C.28)

where:

\[ \mu(X) = C(X, X_n)C_n^{-1}Y_n \]  

(C.29)
\[ \Sigma(X) = \tau^2 [C_\theta(X, X) - C_\theta(X, X_n) C_n^{-1} C_\theta(X, X_n)^T + g I_n] \] (C.30)

As discussed, \( \tau^2 \), \( g \), and \( \theta \) in (C.29) and (C.30) are hyperparameters required to fine tune the GP, and their values are estimated numerically or analytically based on the training dataset.
Appendix D

List of Uncertain Parameters

A list of uncertain input parameters for numerical and analytical models used in Chapter 6 is provided in this appendix.

D.1 Switching Model

The uncertain input parameters of the switching model are listed below:

1. DM 1 inductance, $L_{DM1}$
2. DM 2 inductance, $L_{DM2}$
3. DM 1 capacitance, $C_{DM1}$
4. DM 2 capacitance, $C_{DM2}$
5. DM 1 damping resistance, $R_{damp1}$
6. DM 2 damping resistance, $R_{damp2}$
D.2. Loss Model

D.2.1 Switching Loss

The uncertain input parameters of the switching-loss model are summarized as below:

1. Capacitance stored energy of diode, $E_{oss}$
2. Capacitance stored energy of MOSFET, $E_{oss}$
3. Gate to source charge, $Q_{gs}$
4. Gate to drain charge, $Q_{gd}$
5. Gate charge total, $Q_g$
6. Gate threshold voltage, $V_{th}$
7. Gate plateau voltage, $V_{pl}$
8. Gate resistance, $R_g$
9. Driver on-state voltage, $V_{dr-on}$
10. Driver off-state voltage, $V_{dr-off}$
11. MOSFET stray inductance, $L_s$
D.2.2 Conduction Loss

The uncertain input parameters of the conduction loss model are summarized as below:

1. Diode conduction characteristics $V_F$ and $R_t$

2. Drain-source on-state resistance of MOSFET, $R_{DS(on)}$

3. Winding resistance, $R_{wire}$

D.2.3 Core Loss

The uncertain input parameters of the core loss model are summarized as below:

1. Core dimensions,

2. Core loss constant, $K$

3. Initial permeability of the core, $A_L$

4. Effective core volume, $V_e$

5. Effective core surface, $A_e$

6. Effective core length, $L_e$

7. Core window area, $W_A$

8. Core window perimeter, $W_P$
D.3  Thermal model

The uncertain input parameters of the thermal model are summarized as below:

1. Diode junction-case thermal resistance, $R_{th,JC}$

2. Diode junction-ambient thermal resistance, $R_{th,JA}$

3. MOSFET junction-case thermal resistance, $R_{th,JC}$

4. MOSFET junction-ambient thermal resistance, $R_{th,JA}$

D.4  Size Model

Dimensions of Ferrite cores, iron powder cores, and semiconductor devices are all uncertain within the given range in the datasheet of each component.