Optimization of LLC Resonant Converters: State-trajectory Control and PCB based Magnetics

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Abstract

With the fast development of information technology (IT) industry, the demand and market volume for off-line power supplies keeps increasing, especially those for desktop, flat-panel TV, telecommunication, computer server and datacenter. An off-line power supply normally consists of electromagnetic interference (EMI) filter, power factor correction (PFC) circuit and isolated DC/DC converter. Isolated DC/DC converter provides input to output isolation and output voltage regulation for off-line power supply. It occupies more than half of the volume in an off-line power supply, so isolated DC/DC converter is the key aspect to improve the overall performance and reduce the total cost for off-line power supply. On the other hand, of all the power supplies for industrial applications, those for the data center servers are the most performance driven, energy and cost conscious due to the large electricity consumption. The total power consumption of today’s data centers is becoming noticeable. In 2014, data centers in the U.S. consumed an estimated 70 billion kWh, representing about 1.8% of total U.S. electricity consumption. Moreover, with the increase in cloud computing and big data, energy use of data centers is expected to continue rapidly increasing in the near future. Isolated DC/DC converters in datacenters are required to provide low-voltage high-current output and fast transient response, and those requirements make the design of isolated DC/DC converters even more difficult.
The LLC resonant converters have been widely used as the DC-DC converter in off-line power supplies and datacenters due to its high efficiency and hold-up capability. With the property of zero-voltage-switching (ZVS) for the primary switches and zero-current-switching (ZCS) for the secondary synchronous rectifiers (SRs), using LLC converters can also reduce electromagnetic interference. Almost all the high-end offline power supplies employs LLC converters as the DC/DC converter.

But there are three major challenges in LLC converters. Firstly, the control characteristics of the LLC resonant converters are complex due to the dynamics of the resonant tank. The state-trajectory analysis and control is a powerful tool to solve this challenge, but it requires high-performance digital controller together with analog control circuitry. This dissertation proposes a method to implement state-trajectory control with a low-cost microcontroller (MCU). And further efforts have been made to integrate all the state-trajectory control function into one MCU for high-frequency LLC converters, including start-up and short-circuit protection, fast transient response, light load efficiency improvement and SR driving.

Secondly, most power supplies in IT industry are required to provide low-voltage high-current output, but the transformer is very bulky and it is very challenging to design due to large conduction losses. By pushing switching frequency up to MHz with gallium nitride (GaN) devices, the magnetics can be integrated into printed circuit board (PCB) windings. This dissertation proposes a novel matrix transformer structure and its design methodology, to integrate four elemental transformers into one magnetic core with much reduced winding loss and core loss. On the other hand, to suppress the CM noise, shielding layers can automatically be inserted into the PCB windings between the primary and secondary windings in the fabrication process. A novel shielding technique is proposed to utilize half of the shielding as the primary winding, which not
only suppresses CM noise, but also improves the efficiency. The proposed transformer design and shielding technique is applied to an 800W 400V/12V LLC converter design. Peak efficiency of 97.7%, power density of 900W/inch³ and CM noise reduction of 30dB are achieved.

Thirdly, the LLC converters have sinusoidal current shape due to the nature of resonance, which has larger root mean square (RMS) of current, as well as larger conduction loss, compared to pulse width modulation (PWM) converter. This extra conduction loss compared to PWM converter is considered circulating energy in resonant converter. Three-phase interleaved LLC converters can reduce the circulating energy by inter-connecting the three phases in certain way, but it suffer from bulky and numerous magnetic components. This dissertation proposed a novel magnetic structure to integrated three inductors and three transformers into one magnetic core. By pushing switching frequency up to 1MHz, all the magnetics can be implemented with 4-layer PCB winding. Additional 2-layer shielding can be integrated to reduce CM noise. A 1MHz 3kW 400V/48V three-phase LLC converter with proposed magnetic structure is designed, and peak efficiency of 97.5% and power density of 600W/inch³ are achieved.

This dissertation solves the challenges in analysis, digital control, magnetic design and EMI in high-frequency DC/DC converters in off-line power supplies and datacenters. With the academic contribution in this dissertation, GaN devices can be successfully applied to high-frequency DC/DC converters with MHz switching frequency to achieve high efficiency, high power density, simplified but high-performance digital control and automatic manufacturing. The cost will be reduced and the performance will be improved significantly.
With the fast development of information technology (IT) industry, the demand and market volume for off-line power supplies keeps increasing, especially those for desktop, flat-panel TV, telecommunication, computer server and datacenter. The total power consumption of today’s data centers is becoming noticeable. Moreover, with the increase in cloud computing and big data, energy use of data centers is expected to continue rapidly increasing in the near future. The efficiency of off-line power supplies is very critical for the whole human society in order to reduce the total electricity consumption. And the cost is also a key driving force for the development of novel technology in off-line power supplies due to the large market volume.

An off-line power supply normally consists of electromagnetic interference (EMI) filter, power factor correction (PFC) circuit and isolated DC/DC converter. Isolated DC/DC converter occupies more than half of the volume in an off-line power supply and takes the most control responsibilities, so isolated DC/DC converter is the key aspect to improve the overall performance and reduce the total cost for off-line power supply. Among all the DC/DC converter topologies, the LLC resonant converters have been most widely used as the DC/DC converter due to its high efficiency and hold-up capability.

But there are three major challenges in LLC converters. Firstly, the control characteristics are very complex due to the dynamics of the resonant tank. To achieve good control performance,
very complex and expensive digital controller has to be employed. Secondly, the magnetic components are very bulky, and it is expensive to manufacture them. Thirdly, there is circulating energy in LLC converters due to the nature of resonance, which increases the total loss.

To solve these challenges, this dissertation proposes to implement a special control method, state-trajectory control, with a low-cost microcontroller (MCU). All the control functions can be integrated into one simple, low-cost MCU to replace the previous complex and expensive controller. By pushing switching frequency up to MHz with next generation power devices, this dissertation proposes a novel magnetics structure that can be integrated into printed circuit board (PCB) windings to achieve low-cost and automatic manufacturing. Furthermore, this dissertation employs three-phase interleaved LLC converters topology to reduce the circulating energy, and proposed a novel magnetic structure to integrated three inductors and three transformers into one magnetic core with simple 4-layer PCB winding. All the proposed technologies have been verified on hardware prototypes, and significant improvements over industrial state-of-art designs have been demonstrated.

To sum up, this dissertation solves the challenges in analysis, digital control, magnetic design and EMI in DC/DC converters for off-line power supplies. With the academic contribution in this dissertation, the cost can be reduced due to the simplified control and automatic manufactured magnetics, and the efficiency can be improved with proper utilization of next generation power devices. This dissertation will improve future DC/DC converter for IT industrial in the three most important aspects of efficiency, power density and cost.
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Chapter 1. Introduction

1.1. DC/DC converter in off-line power supplies

With the fast development of information technology (IT) industry, the demand and market volume for off-line power supplies keeps increasing, especially those for desktop, flat-panel TV, telecommunication, computer server and datacenter, as shown in Fig. 1.1(a). An off-line power supply normally consists of electromagnetic interference (EMI) filter, power factor correction (PFC) circuit and isolated DC/DC converter, as shown in Fig. 1.1(b). Most IT equipment requires isolated low-voltage high-current output and fast transient response. Isolated DC/DC converter needs to meet several rigid requirements, such as input to output isolation, output voltage regulation, short-circuit protection, load condition monitor, and communication with central controller. Besides these requirements, the design of high-output-current DC/DC converter is very challenging due to large conduction loss.

![Applications and Architecture of Off-Line Power Supplies](image)

Fig. 1.1. Applications and architecture of off-line power supplies.
In a standard off-line power supply as shown in Fig. 1.2, the DC/DC converter normally occupies more than half of the total volume, so DC/DC converter is the key aspect to improve the overall performance and reduce the total cost for off-line power supplies. Present DC/DC converter, operating at 50 - 100 kHz, requires bulky and expensive magnetic components. And it is difficult to optimize these magnetics due to large conduction loss. On the other hand, it is very challenging to design the control system for DC/DC converter due to many rigid requirements.

![An example of off-line power supply.](image)

Fig. 1.2. An example of off-line power supply.

Of all the power supplies for industrial applications, those for the data center servers are the most performance driven, energy and cost conscious due to the large electricity consumption. The total power consumption of today’s data centers is becoming noticeable. In 2014, data centers in the U.S. consumed an estimated 70 billion kWh, representing about 1.8% of total U.S. electricity consumption [1]. Moreover, with the increase in cloud computing and big data, energy use of data centers is expected to continue rapidly increasing in the near future. The current practice of data center power architecture is illustrated in Fig. 1.3(a), where all major processor/memory devices are powered from a 12V bus. The i^2R loss for a 12V bus is excessive, and there are many energy conversion stages, which reduces the total system efficiency. To mitigate the heavy bus-bar loss and reduce energy conversion stages in the power distribution path, industry leaders such as Google, Facebook, Cisco and IBM are already implementing a new data center design with a
higher voltage distribution bus, such as 48V or 400V instead of 12V [2]-[6]. Power architecture with 48V bus, shown in Fig. 1.3(b), is advantageous than the current design practice with the elimination of online UPS and cables and harness. Recently, the International Electronics Manufacturing Initiative (iNEMI) at the behest of IBM and other server manufacturers undertook a project to develop an industry standard for DC/DC converters [7], whose specifications are shown in Table 1.1. This converter is used to step down 380V directly to 12V and is placed directly on the motherboard. This new power architecture with 400V bus, shown in Fig. 1.3(c), is deemed superior to the current practice with 12V bus.

(a) Current architecture with 12V bus.

(b) Alternative architecture with 48V bus.

(c) Future architecture with 400V bus.

Fig. 1.3. Comparison of data center power architectures.
### Table 1.1. Specifications of DC/DC Converter Required by iNEMI

<table>
<thead>
<tr>
<th>Item</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>360Vdc</td>
<td>380Vdc</td>
<td>400Vdc</td>
</tr>
<tr>
<td>Efficiency</td>
<td>92%@10% load</td>
<td>96%@full load</td>
<td>97%@50% load</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>11.60Vdc</td>
<td>12.00Vdc</td>
<td>12.60Vdc</td>
</tr>
<tr>
<td>Output Current</td>
<td>0A</td>
<td>62.5A</td>
<td></td>
</tr>
<tr>
<td>packaging</td>
<td>DOSA Quarter Brick Form Factor</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Isolated high-output-current DC/DC converters are critical for off-line power supplies and future data center power architecture. Present DC/DC converters, operating at 50-100 kHz with a power density less than 50W/in³, cannot fulfill the increasing requirement. The trend for off-line power supplies and datacenters is the pursuit of higher efficiency and higher power density. The LLC resonant converters are suitable for both high-efficiency and high-power-density design [8]-[12]. The LLC converters can achieve ZVS for zero to full load range with a low turn-off current for the primary switches, and at the same time, ZCS for the synchronous rectifiers (SRs). Such soft-switching properties also reduce electromagnetic interference [12]. In comparison with soft-switching PWM converters, LLC converters can achieve a higher switching frequency with better efficiency, resulting in a higher power density and lower total cost [9][11]. Almost all the high-end off-line power supplies are employing LLC converter as the isolated DC/DC converter.

By pushing switching frequency 10 times higher with GaN devices, the power density can be significantly increased to meet the trend in future datacenter power supplies. However, there would be several key challenges: (1) how to achieve high-performance control for the high-frequency LLC converter in a cost-effective way; (2) how to design and optimized the high-frequency high-
output-current transformer design; (3) how to reduce circulating energy in LLC converters and further integrate magnetics when several phases of LLC converter are paralleled. These challenges will be discussed in detail as follows.

1.2. Challenges in control of high-frequency LLC converters

The control of the resonant converter has always been a challenge due to the dynamics of the resonant tank. For the PWM converter, since the natural frequency of the output filter is much lower than the switching frequency, the state-space average method is good enough to provide an accurate small-signal model. For the resonant converter, since the natural frequency of the resonant tank is close to the switching frequency, the average method will eliminate the information of switching frequency, thus cannot predict the dynamic performance. Many approaches have been tried to describe the control characteristics and improve the transient response of the resonant converters. The control schemes for most of these approaches can be generalized as Fig. 1.4. There is an inner loop sensing the resonant tank information. And there is an outer loop to regulate the output voltage. The outputs of the two loops are compared to generate the primary driving signal.

Fig. 1.4. Generalized control scheme for the LLC resonant converters

Among those approaches, the frequency control is the simplest and most commonly used. Since the average model does not work for the resonant converter. The describing function [13]
and the multi-frequency averaging [14] are used to derive the small-signal model for the frequency control, but they require extensive computation work. The simulation-based method [15] provides an alternative solution, but it also requires extensive time to cover all the operation range. Recently, the simplified equivalent circuit models for the series resonant converters (SRC) [16] and the LLC converters [17] have been developed to help simplify the analysis of the small-signal model while at the same time still maintain a good accuracy. However, all of the results from these work shows that the transfer function is quite complex under different operating points due to the nature of the variable frequency control for the resonant converters. Thus the simply frequency control with a linear compensator cannot achieve a high bandwidth, as well as a fast transient response.

The current-mode control [18] or charge-mode control [19][20] have been proposed to improve the transient response of the resonant converter. The variation of the control-to-output transfer function of the current-mode control under the different operating points is smaller than that of the frequency control due to the additional feedback from the resonant tank. However, the implementation of this approach is quite complex, requiring additional sensing circuits, as well as logic circuits, to control the switching instants of the primary-side switches. On the other hand, it is shown that the current-mode control for the SRC has an inherent stability issue; and capacitor-voltage control or charge-mode may decrease the unstable range with careful designs, but cannot eliminate stability issue [21][22]. The stability issue of the current-mode control or the charge-mode control for the LLC converters needs to be further investigated.

Different from the small-signal approaches, the state-trajectory analysis and control can better describe and analyze the behavior of the resonant tank. It is first applied to the SRC [21][22]. By sensing all the state variables and processing them in the controller, the optimal trajectory control (OTC) for the SRC can control the resonant tank to follow the desired trajectory exactly,
while at the expense of complexity [23]. The simplified optimal trajectory control (SOTC) for the LLC converters was proposed to simplify the OTC, while at the same time still maintain a good transient response [24]. The state-trajectory analysis and control for the LLC converters was also extended to the burst mode for light load efficiency improvement [25], and soft start-up [26]. However, it is worth noting that even the SOTC has demonstrated a simplified control scheme, a very fast controller, such as FPGA in the demonstration, is still required to achieve these control functions. The controller at such a high cost is not practical for the industrial applications, such as power supplies for server or telecom.

The digital controllers are gradually taking the place of the analog controllers in the control of the LLC converters [27][28][29], and will become the future trend for the power management [30]. Among the digital controllers, the cost-effective microcontrollers (MCUs) are preferred in the industrial applications. Recently, some progress has been made to achieve MCU based SOTC control to integrate all the state-trajectory control functions into one MCU for a 130kHz LLC converter [31], as shown in Fig. 1.5. However, the digital control for high-frequency LLC converters is still very challenging, since the impact of digital delay is becoming more significant for high-frequency operation. And how to achieve SOTC control for high-frequency LLC converters with low-cost MCU has not been solved yet.

Fig. 1.5. MCU based simplified optimal trajectory control (SOTC) for LLC converters
1.3. Challenges in transformers design for high-output-current LLC converters

For applications that require low-voltage and high-current outputs, such as computer servers, there are several important design considerations for the LLC converters, take 1kW 12V output server power supply as an example: 4-8 SRs should be paralleled to reduce secondary conduction loss caused by a huge output current (> 80A) as illustrated in Fig. 1.6(a). This makes it difficult to achieve both static and dynamic current sharing. There will be large termination losses since AC currents must flow through common termination points between the transformer and the SRs, which is marked using red dots in Fig. 1.6(a). It is difficult to place the large number of SRs close to the terminations, since it will result in large leakage inductances and winding losses at the secondary windings. Such an LLC converter design will suffer large winding losses and termination loss. On the other hand, the transformer normally uses litz wires as the primary winding and copper foils as the secondary winding, which is very bulky, labor-intensive and expensive. The prototype of such LLC converter design, as shown in Fig. 1.6(b), has large volume and requires complex manufacturing process.

![Schematics and Prototype](image)

(a) Schematics. (b) Prototype.

Fig. 1.6. State-of-art LLC converters.
A matrix transformer with a PCB winding can be adopted to solve the challenges in conventional LLC converter designs, as shown in Fig. 1.7(a). The conventional single core structure was divided into a four-core structure. The primary current for the four elemental transformers is the same due to a series connection. The secondary current is perfectly balanced and the large secondary current is evenly distributed to different SRs. The matrix transformer in Fig. 1.7(b) can be formed by using four sets of identical UI-cores. The primary winding winds one pillar of each core as shown in Fig. 1.7(a), where only the primary winding is shown for simplicity. The matrix transformer in Fig. 1.7(a) has an increased core loss with 4 sets of UI-cores compared to the transformer in Fig. 1.6(a) with only one ER-core. The structure can be simplified by means of flux cancellation [36][37], but multiple cores are still employed, which is complex for the manufacturing. Matrix transformer with PCB windings can be automatically manufactured, but the fully interleaved PCB windings will lead to large distributed inter-winding capacitors and, hence, a large CM noise current. The shielding technique is considered an effective method to suppress CM noise for the planar transformers and has been successfully demonstrated in [38][39]. Specifically for a 4-layer PCB winding matrix transformer, shielding could be achieved by simply placing two shielding layers in between primary and secondary windings.

(a) Schematics. (b) Transformer structure.

Fig. 1.7. LLC converter with matrix transformers.
When using matrix transformer for high-output-current applications, the core number, as well as volume and core loss, will increase. Increasing switching frequency can reduce core volume significantly, and further magnetic integration is necessary to reduce the core number, but this requires high-frequency transformer loss model and integrated matrix transformer structure. Shielding technique is necessary for PCB winding transformers, but shielding layers will introduce extra eddy current loss and reduce the total efficiency. Further improvement on shielding technique is required to achieve CM noise reduction, while at the same time improving efficiency.

1.4. Challenges in three-phase interleaved LLC converters

The LLC converters have sinusoidal current shape due to the nature of resonance, which has larger root mean square (RMS) of current, as well as larger conduction loss, compared to pulse width modulation (PWM) converter. An example of primary current in single-phase LLC converter and PWM converter is shown in Fig. 1.8, in which the magnetizing current is set to zero for clear comparison. This extra conduction loss in single-phase LLC converter compared to PWM converter is considered circulating energy in resonant converter.

![Comparison of primary current in single-phase LLC converter and PWM converter.](image)

Fig. 1.8. Comparison of primary current in single-phase LLC converter and PWM converter.

To get the benefit of soft-switching in resonant converters, while at the same time reducing circulating energy, three-phase interleaved LLC converter, as shown in Fig. 1.9(a), can be
employed. Three-phase LLC converters can reduce circulating energy and achieve automatic current sharing by interconnecting the three phases in certain ways, including connecting the primary sides to a common Y-node (Y-primary) [84], connecting the secondary sides to a common Y-node (Y-secondary) [85], and employing a delta-connect resonant capacitor network (∆-Cr network) for primary sides [86]. Furthermore, the primary and secondary RMS current can be reduced due to interaction between three phases [84]-[86], as show in Fig. 1.9(b), in which the magnetizing current is set to zero for clear comparison. The current in three-phase LLC converter is quite close to PWM converter.

(a) Schematics.

(b) Comparison of primary current with single-phase LLC converter.

Fig. 1.9. Three-phase interleaved LLC converter.
But three-phase LLC converter requires three inductors and three transformers. If three individual inductors and three individual transformers are employed, the volume, cost and complexity will increase a lot. Therefore, magnetic integration is necessary for application of three-phase LLC converters. But present DC/DC converters, operating at 50-100 kHz with a power density less than 50W/in³, require large bobbins and hand-wound windings, the integrated magnetic is still large and hard to manufacture. The trend for off-line power supplies is the pursuit of higher efficiency and higher power density. Three-phase LLC converters are beneficial for reducing circulating energy, but it is very challenging to design suitable magnetics.

1.5. Dissertation outline

As discussed in this chapter, LLC converter is widely used as isolated DC/DC converter in off-line power supplies, and high-frequency operation is necessary to meet the trend of future offline power supplies and future datacenter architecture due to the high power density and low cost. But it is very challenging to control and design high-frequency DC/DC converters. The LLC resonant converters are suitable for both high-efficiency and high-power-density designs [8]-[12]. Digital control is necessary for IT industry, but the impact of digital delay is becoming more significant in high-frequency operation. Matrix transformer is necessary to achieve high efficiency for high-output-current applications, but it requires multiple cores and there is large CM noise. Three-phase interleaved LLC converters can reduce circulating energy, but using three inductors and three transformers increases the volume and complexity significantly. To solve these challenges in the high-frequency DC/DC converter. This dissertation is organized as follows.

Chapter 2 investigates the limitations of SOTC control for high-frequency LLC converters, and proposes methods to extend the SOTC control to the high-frequency LLC converters with low-
cost MCU. All the necessary control functions for LLC converters in datacenter power supplies are integrated into one MCU, including: soft start-up [32], fast transient response [33], burst mode for light-load efficiency improvement [34] and adaptive SR driving [35].

Chapter 3 investigates the state-of-art matrix transformer designs, and proposes an optimal design methodology. Due to the challenge of multiple cores in matrix transformer, further magnetic integration is proposed to integrate all the elemental transformers into one magnetic component, and efficiency is also improved at the same time [93]. On the other hand, this chapter develops the inter-winding capacitance and CM noise model for the matrix transformers, and comes up with a novel shielding technique for the matrix transformer which can not only reduce CM noise significantly, but also further improve efficiency [94]. Besides, chapter 3 proposes a method to dynamically control the bus voltage of two-stage VRM with LLC converter as the bus converter to further improve the light load efficiency [75].

Chapter 4 investigates the state-of-art three-phase interleaved LLC converters, and proposes a structure suitable for high-frequency application. By pushing $f_s$ of three-phase LLC converter up to MHz with GaN devices, this chapter further proposes an integrated magnetics structure integrate three inductors and three transformers into one magnetic core with 4-layer PCB winding and additional 2-layer shielding. Design optimization methodology is also presented. Compared to the state-of-art three-phase LLC converters, the proposed high-frequency three-phase LLC converter has the benefit of high efficiency, high power density, low CM noise and good manufacturability.

Conclusions and future work are given in Chapter 5.
Chapter 2.  State-trajectory Control for High-frequency LLC Converters

The optimal trajectory control (OTC) proposed in [23] employs a control scheme that senses all the state variables and process them in the controller to calculate the real-time trajectory. The control scheme is shown in Fig. 2.1, in which, the input voltage $V_{IN}$, the current $i_{Lr}$ for the resonant inductor $L_r$, the sum or difference of the voltage $V_{Cr}$ for the resonant capacitor $C_r$ and the output voltage $V_O$ are sensed. The radius of the real-time calculated trajectory for high-side switch $R_1$ or that for low-side switch $R_2$ is compared with a reference radius $R_{ref}$ to determine the switching instant.

Fig. 2.1. Control scheme for the Optimal Trajectory Control (OTC)

The control law for the OTC can be explained on the state-plane, which is drawn with x-axis of the normalized resonant voltage $V_{CrN}$, and y-axis of the normalized resonant current $i_{LrN}$. In the
state-plane, the voltages are normalized with the voltage factor $V_{IN}$, and the currents are normalized with the current factor $V_{IN}/\sqrt{Lr/Cr}$. Fig. 2.2 presents two examples of transient response of OTC for SRC. In Fig. 2.2(a) for load step-up, the converter works at light load with a control reference of $R_{ref1}$ at the beginning. The reference controls the radius of the trajectory when the active switches are conducting. If the control reference changes from $R_{ref1}$ to $R_{ref2}$, the converter is able to change from the light load trajectory to the heavy load trajectory within one step by controlling the turn-on instant of Q1 switch, which is marked as green trajectory in Fig. 2.2(a). The same principle applies to load step-down in Fig. 2.2(b). The converter is able to change from the heavy load with a reference of $R_{ref1}$ to the light load with a reference of $R_{ref2}$ within one step.

![Diagram](image)

(a) Load step-up  
(b) Load step-down

Fig. 2.2. Transient response of OTC for SRC

Although the OTC demonstrated the optimal transient performance, it has not been widely adopted due to the complex implementation and the requirement of high-performance controller. To simplify the complex implementation, the simplified optimal trajectory control (SOTC) for LLC converter is proposed in [24], whose control scheme is shown in Fig. 2.3. Instead of sensing all the state variables in OTC, the SOTC senses the load current and output voltage to estimate the state trajectory of the resonant tank. When load transient happens, the SOTC would predict the
optimal response of the primary driving signals based on the sensed load current and modify the primary driving signals accordingly. And in steady state, the linear compensator would regulate the output voltage and eliminate the steady state error. By doing this, the SOTC is able to achieve the fast transient response and optimal trajectory of the resonant tank, which is quite similar to that of the OTC.

![Control scheme of the simplified optimal trajectory control (SOTC)](image)

**Fig. 2.3.** Control scheme of the simplified optimal trajectory control (SOTC)

Because sensing the load current is quite a common practice and widely adopted in power supplies for the IT industry due to the power management requirements, the SOTC increases little system complexity compared with the conventional linear control. Although the SOTC predicts the response based on the known resonant tank parameters, it is shown that the SOTC for LLC converter is robust to the sensing or parameter tolerance by simulation in [24]. This is because that when load steps up, the controller always needs to increase the primary switch on-time to extend the energy in the resonant tank, and when load steps down, the controller always needs to decrease the primary switch on-time to shrink the energy in the resonant tank. So the SOTC is beneficial to improve the transient performance even tolerance exists. Fig. 2.4 shows the transient response of SOTC for LLC converter, where the red trajectory represents the heavy load steady state, the black trajectory represents the light load steady state, the green trajectory represents SOTC for transient,
and the blue trajectory represents the closed-loop regulation. The controller calculates the response of the primary switches immediately after the load transient and settles the resonant tank to the vicinity of steady state. Then the linear compensator would eliminate the steady state error.

![Diagram](image)

(a) Load step-up

(b) Load step-down

*Fig. 2.4. Transient response of SOTC for LLC converter*

Despite the simplified control scheme, the SOTC still requires very high-speed ADC and high-performance digital controller to make the converter response within half switching period after the load transient. While such expensive ADC and digital controller is not practical for commercial power supplies. On the other hand, most LLC converters are employed as the isolated bus converters, and the di/dt of the load transient is not as fast as those for the CPU voltage regulators. It is very meaningful to investigate how to implement the SOTC for fast transient response with low-cost microcontrollers, which are widely used in the control of commercial power supplies; and furthermore, investigate how to apply SOTC to high-frequency LLC converters. In commercial power supply products, different control functions can be further integrated into the digital controller to reduce the system cost. Further research need to be conducted to integrate soft start-up, burst mode for light load efficiency and SR driving into the MCU.
2.1. Fast transient response

Different from previous state-trajectory control method [23], the Simplified Optimal Trajectory Control (SOTC) proposed in [24] calculates the trajectory based on only the output voltage and the load current, rather than the resonant current and/or the resonant voltage. This is because the steady-state trajectory is determined by the output voltage and the load current under certain input voltage range, regardless of the switching frequency.

Fig. 2.5 is an example of the state-trajectory for the LLC converters operating at around the resonant frequency. The x-axis is the normalized resonant current, and the y-axis is the normalized resonant voltage. The current normalizing factor is \( V_{in}/\sqrt{L_r/C_r} \), and the voltage normalizing factor is \( V_{in} \). Firstly, the centers of the trajectory are determined by the output voltage. When the high-side switch is on, the voltage across the resonant tank is \( V_{in} - nV_o \), which is \( O_1(1 - nV_{oN}, 0) \) in the state-plane. When the low-side switch is on, the voltage across the resonant tank is \( nV_o \), which is \( O_2(nV_{oN}, 0) \) in the state-plane. The radius \( R \) of the trajectory is determined by the load current. Take switching frequency at around the resonant frequency as an example, \( R \) is expressed as

\[
R = \frac{\sqrt{2}I_{LR,RMS}}{V_{in}/\sqrt{L_r/C_r}} \quad (2.1)
\]

In which, \( I_{LR,RMS} \) is the RMS value of the resonant current, expressed as:

\[
I_{LR,RMS} = \frac{1}{4\sqrt{2}} \sqrt{\frac{n^4V_o^2T_r^2}{L_m^2} + 4\pi^2 \left(\frac{I_{load}}{n}\right)^2} \quad (2.2)
\]
Fig. 2.5. State-trajectory of the LLC converters operating at around the resonant frequency

2.1.1. Digital implementation of fast transient response

To achieve SOTC with low-cost digital controller, [31] simplified the real-time calculation of SOTC for the digital controllers and proposed method to implement SOTC with low-cost MCUs. Since the digital delay is a key factor impacting the transient performance, the sampling and the calculation is allocated within one switching cycle to optimize the transient response. Fig. 2.6 is an example of sampling and calculation during the load step-up with SOTC.

Fig. 2.6. Sampling and calculation during the load step-up with SOTC

For the SOTC implemented by MCU, there is still a maximum switching frequency limitation caused by the digital delay. Take TI’s digital controller TMS320F28027 as an example, the total
digital delay is 7.2us, which means that the maximum switching frequency suitable for SOTC is 140kHz. If we want to further increase this maximum switching frequency limitation, the digital delay of SOTC must be reduced.

To reduce the digital delay of SOTC, firstly, the sampling and the calculation is re-allocated as shown in Fig. 2.7. The A/D for the output voltage finishes before the beginning of the present switching cycle, and then the PI calculation starts at the beginning of the present switching cycle since the PI calculation only needs the output voltage. At the same time of the PI calculation, the load current is sampled and converted, and then the SOTC calculation follows immediately after the PI calculation. With this improvement, the digital delay consists of only calculation. With digital controller TMS320F28027, the digital delay is reduced to 6.7us, and the maximum switching frequency suitable for SOTC is increased to 150kHz.

![Fig. 2.7. Improve implementation of SOTC by re-allocating sampling and calculation](image)

The second step to reduce the digital delay is to use the look-up table for the SOTC calculation instead of the real-time calculation. In the previous implementation, the equations for $\Delta T_{UP}$ in the load step-up and $\Delta T_{DOWN}$ in the load step-down are expressed below, which is derived in [24]:

$$
\Delta T_{UP} = \frac{L_m (I_{[k]} - I_{[k-1]})}{nV_{in}}
$$

(2.3)
\[ \Delta T_{DOWN} = -\left(1 - \sqrt{\frac{I_{[k]}}{I_{[k-1]}}} \right) \cdot \frac{T}{4} \] (2.4)

The real-time calculation can be replaced by the look-up table to reduce the calculation time. Take a 500kHz LLC converter as an example, the look-up table is shown in Fig. 2.8. It is 3-dimenion table, with x-axis of the (k-1)th sampling, y-axis of the kth sampling, and z-axis of the \( \Delta T \).

![Look-up table for SOTC calculation of a 500kHz LLC converter](image)

The result from the look-up table is the same with that from the real-time calculation, but the required CPU cycles for the calculation is reduced from around 400 CPU cycles to around 240 CPU cycles. And the table consists of only 121 integers, which is around 3% RAM space of TMS320F28027. With the look-up table, the digital delay is reduced to 4us, and the maximum switching frequency suitable for SOTC is increased to 250kHz. Although the evaluations above are based on given controller, the same analogy applies to the other digital controllers. The implementation of SOTC is improved by optimizing the sampling points and using the look-up table to reduce the calculation time. With these improvements and taking TMS320F28027 as an example, the maximum switching frequency suitable for SOTC is improved from 140kHz to
250kH. But there is still a limitation if we want to further push the switching frequency with given controller.

### 2.1.2. Fast transient response for high-frequency LLC converters

Although the implementation of SOTC is optimized and improved, there is still maximum switching frequency limitation with given controller. Multi-step SOTC is proposed to further push this maximum switching frequency limitation with given controller. The concept of SOTC is to settle the resonant tank within 2-step, which is the optimal way to settle 3 resonant elements: resonant inductor $L_r$, resonant capacitor $C_r$ and magnetizing inductor $L_m$ in the LLC converters. However, due to this 2-step limitation, the maximum switching frequency with given controller is also limited. If we want to further push this maximum switching frequency limitation, the 2-step solution is not suitable any more. Instead of trying to achieve the optimal performance, Multi-step SOTC can be used to settle the resonant tank within more than 2 steps as shown in Fig. 2.9. The number $m$ of steps in Multi-step SOTC is determined by the speed of the digital controller and the switching frequency of the power stage. For example, 2-step SOTC with TMS320F28027 is suitable for a switching frequency of up to 250kHz; then 4-step SOTC with the same controller would be suitable for a switching frequency of up to 500kHz; the same analogy applies to the cases with more steps.

Even Multi-step SOTC uses more steps to settle the resonant tank; it can still achieve the benefit of SOTC, which means there is very small oscillation in the resonant tank during the load transient. This is because Multi-step SOTC is still much faster than the linear regulator, and the resonant tank is first settled to around the final steady state; then the linear regulator takes very little effort to eliminate the steady state error. For given high frequency power stage and low-cost digital controller, the benefit of SOTC can still be achieved by using Multi-step SOTC.
Fig. 2.9. Proposed Multi-step SOTC

Fig. 2.10 shows the implementation of 6-step SOTC. The output voltage and the load current are sampled every third switching cycle. After the load transient happens, the controller would have 3 switching cycles (equivalent to 6 steps) to accommodate the calculation time. Then the controller uses 6-step to settle the resonant tank. So the same controller can be applied to the higher switching frequency with Multi-step SOTC compared with the case using 2-step SOTC.

Fig. 2.10. Implementation of 6-step SOTC
The $\Delta T_{UP}$ for load step-up and $\Delta T_{D}$ for load step-down in a multi-step SOTC are derived in [33] and expressed below, assuming the SOTC control loop is executed every $(N+1)^{th}$ switching cycle ($N = 1, 2, 3$):

$$\Delta T_{UP} = \frac{L \cdot (I_{Load}[k] - I_{Load}[k-1])}{(N+1) \cdot n \cdot V_{IN}}$$

$$\Delta T_{D} = \left(1 - \frac{2^{(N+1)}}{\sqrt{I_{Load}[k]}}\right) \cdot \frac{T_{Q}}{4}$$

### 2.1.3. Experimental results

The proposed control for the high-frequency LLC converters are implemented by a 60MHz MCU TMS320F28027, and verified on a 1kW 400V/12V 500kHz LLC converter, whose parameters are listed in Table 2.1. This high-frequency LLC converter is designed based on the matrix transformer for LLC converters in [36]. The prototype and the efficiency curve are shown in Fig. 2.11. The LLC converter has a power density of 207W/inch$^3$, a peak efficiency of 95.1%, and an output capacitor of 3mF.

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant Frequency $f_0$</td>
<td>500kHz</td>
</tr>
<tr>
<td>Dead Time</td>
<td>180ns</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>16:1</td>
</tr>
<tr>
<td>Primary devices</td>
<td>IPW60R099P6</td>
</tr>
<tr>
<td>Secondary devices</td>
<td>BSC010N04LS</td>
</tr>
<tr>
<td>Primary Driver</td>
<td>ADuM4223</td>
</tr>
<tr>
<td>Secondary Drivers</td>
<td>FAN3122</td>
</tr>
<tr>
<td>Resonant Capacitor</td>
<td>22nF</td>
</tr>
<tr>
<td>Resonant Inductance</td>
<td>4.5uH</td>
</tr>
<tr>
<td>Magnetizing Inductance</td>
<td>21.6uH</td>
</tr>
</tbody>
</table>
Fig. 2.11. MCU-controlled 1kW 400V/12V 500kHz LLC Converter.

The experimental results of the load step-up from 40A to 80A and the load step-down from 80A to 40A are shown in Fig. 2.12. The overshoot for both the load step-up and the load step-down are very small, and there is almost no oscillation in the resonant tank during the load transient.

Fig. 2.12. Experiments of multi-step SOTC for load transient

In this section, the Simplified Optimal Trajectory Control (SOTC) is investigated and improved to push the maximum switching frequency limitation for given controller, and SOTC can be implemented by the low-cost controllers to achieve the fast load transient response. Then
the Multi-step Simplified Optimal Trajectory Control (SOTC) is proposed to further push the maximum switching frequency limitation, which calculates the trajectory based on only the output voltage and the load current, and settles the resonant tank within multi steps. With Multi-step SOTC, the low-cost controllers can be used to control the high frequency LLC converters with the state-trajectory control. The number of steps in Multi-step SOTC is determined by the speed of the controllers and the switching frequency of the LLC converters. Experimental results are demonstrated on a 500kHz 1kW 400V/12V LLC converter with 60MHz MCU (TMS320F28027). Fast load transient response is achieved by using 6-step SOTC.

2.2. Soft start-up

Start-up is the most critical process in the control of the LLC converters. There can be very large resonant current $i_{Lr}$ and resonant voltage $V_{Cr}$ stresses during start-up if the process is not well controlled. To limit these stresses, $f_S$ during start-up must be increased to be above the resonant frequency $f_0$ during start-up. The control strategy of most controllers are as follows: the controllers set an initial $f_S$ for start-up, then decreases $f_S$ linearly or exponentially; if $i_{Lr}$ exceeds the limit, the controllers increase $f_S$ abruptly and then decrease $f_S$ gradually again. If the initial $f_S$ for start-up is not high enough, there will be very large stresses. Fig. 2.13 shows the start-up of a commercial controller with an initial $f_S$ of $1.5f_0$ [40]. The controller keeps the $f_S$ of $1.5f_0$ for some time, and then gradually decreases $f_S$ to $f_0$. In this example, the maximum $i_{Lr}$ stress is four times as large as the full-load steady-state stress, and the maximum resonant voltage $V_{Cr}$ stress is twice as large as the full-load steady-state stress. Even when the initial $f_S$ is high enough, it is still very difficult to avoid large stresses during the start-up process. Fig. 2.14 shows the start-up of a commercial controller with an initial $f_S$ of $5f_0$ [41]. Since the initial $f_S$ is very high, $i_{Lr}$ and $V_{Cr}$ stresses are small.
However, during the start-up process, the controller decreases $f_S$ too fast, and large stresses still occur, which trigger the over-current protection. The controller then abruptly increases $f_S$ to limit the stresses. It takes a long time to start-up and there are still large stresses during start-up.

(a) Experimental waveforms.  
(b) $f_S$ trajectory on the gain curve.

Fig. 2.13. Start-up of a commercial controller with an initial $f_S$ of 1.5$f_O$.

(a) Experimental waveforms.  
(b) $f_S$ trajectory on the gain curve.

Fig. 2.14. Start-up of a commercial controller with an initial $f_S$ of 5$f_O$.

Optimal trajectory control (OTC) for soft start-up is first proposed in [26]. The whole start-up process is divided into three stages, as illustrated in Fig. 2.15. Stage 1 sets an asymmetrical current-limiting band, $+I_{maxN}$ and $-I_{LmN}$ (the suffix N means normalized), to settle $V_{Cr}$ to half of input voltage $V_{in}$ (for half-bridge primary configuration). Stage 2 sets a symmetrical current-limiting band, $+I_{maxN}$ and $-I_{maxN}$, to optimize the energy delivery. Stage 3 decreases $f_S$ gradually until $V_O$
reaches steady state, which is 12V in this case. OTC for soft start-up is based on the graphical state-trajectory analysis of the resonant tank. Hence it can minimize the resonant tank stresses and optimize the energy delivery, thus ensuring a safe start-up process in a very fast manner. Fig. 2.16 shows the simulation result of OTC for soft start-up. The parameters for the LLC converter are: resonant inductor $L_r = 55uH$, resonant capacitor $C_r = 24nF$, and magnetizing inductor $L_m = 280uH$. The simulation result shows that $i_{Lr}$ stress during the whole start-up process is only a little bit larger than that of the full-load steady-state. The $f_S$ trajectory of start-up on the gain curve is very smooth. It is obvious that OTC for soft start-up is advantageous over other control methods.

Fig. 2.15. Optimal trajectory control (OTC) for soft start-up.

Fig. 2.16. Simulation of OTC for soft start-up.
2.2.1. Digital implementation of soft start-up

Since OTC for soft start-up has advantages over other control methods and low-cost MCUs are the preferred controllers in industrial applications, it is worthwhile to implement OTC for soft start-up using low-cost MCUs. However, there are still technical challenges if an MCU is employed directly to implement OTC for soft start-up due to the large stresses caused by digital delay. To better illustrate the impact of digital delay, a 60MHz MCU TMS320F28027 is selected as an example for the following analysis, which is a popular low-cost MCU and widely used in telecom and server power supplies. All the required state variables are sensed through the ADC and processed by the CPU, as shown in Fig. 2.17(a). If the MCU senses $i_{Lr}$ and compares it with $I_{maxN}$, there would be a digital delay of at least 0.8us. The impact of this 0.8us digital delay will cause very large $i_{Lr}$ stress in Stage 1, as shown in the shaded areas of Fig. 2.17(b), where the dashed line represents the desired trajectory and the solid line represents the actual trajectory with digital delay. Since the initial $f_S$ for start-up should be very high, even a very small digital delay will cause a large $i_{Lr}$ stress. Specifically, the 0.8us digital delay will cause twice as large as the full-load current stress for a 130kHz LLC converter and more than three times the full-load current stress for a 500kHz LLC converter.

(a) System scheme.  
(b) Trajectory of Stage 1 with digital delay.

Fig. 2.17. Implementing OTC for soft start-up by MCU directly.
It is clear that further effort need to be spent on reducing the impact of digital delay so that soft start-up, as well as short-circuit protection, can be implemented with the low-cost MCUs. The following sections present analysis and propose methods to solve these challenges.

To solve the challenges caused by digital delay in ADC and calculation, MCU-based implementation with look-up tables is proposed, as shown in Fig. 2.18, which only requires sensing $V_o$. The table in Fig. 2.18 is based on the parameters of a 130kHz 300W LLC converter. The start-up process is as follows: when $V_{in}$ reaches around 400V, the MCU will begin the soft start-up process; in Stage 1, the MCU generates the pre-calculated $\Delta T_1, \Delta T_2 \ldots \Delta T_n$ consequently; in Stage 2, the MCU senses $V_o$ and controls $f_S$ based on the pre-calculated $f_S$ vs. $V_o$ table; then in Stage 3, the MCU decreases $f_S$ gradually until $V_o = 12V$, which is the same as OTC for soft start-up. Detailed derivation for the tables appears below.

![Digital implementation with look-up tables for 130kHz LLC converter.](image)

In Stage 1, $V_o$ is considered to be approximately 0V because the output capacitor is very large and there are only a few switching pulses in Stage 1. The initial condition is: $V_{cr} = 0$ and $i_{Lr} = 0$ because there is no energy in the resonant tank before start-up. The trajectories to calculate $\Delta T_1$ and $\Delta T_2$ are shown in Fig. 2.19. And $\Delta T_1$ and $\Delta T_2$ are calculated using the following equations,
where $\omega_o = 1/\sqrt{L_r \cdot C_r}$. The values for $\Delta T_1, \Delta T_2 ... \Delta T_n$ are calculated step by step until it comes to the step at which $V_{Cr}$ comes into the region around $V_{in}/2$, which is the last switching action in Stage 1.

\[
\alpha_1 = \sin^{-1}(I_{maxN}/\rho_1) \\
\Delta T_1 = \alpha_1/\omega_o \\
\alpha_2 = \sin^{-1}(I_{maxN}/\rho_2) + \sin^{-1}(I_{lmN}/\rho_2) \\
\Delta T_2 = \alpha_2/\omega_o
\]

In Stage 2, $f_S$ can be determined based on the pre-calculated $f_S$ vs. $V_O$ table. This is because for a given $V_{in}$ and $V_O$, $f_S$ can be determined based on the $i_{Lr}$ stress requirements when operating at above $f_O$. During start-up, $V_{in}$ and $V_O$ can be considered to be constant within several switching cycles because there is a large input capacitor for the hold-up time and a large output capacitor for the load transient. Under these conditions, the corresponding $f_S$ can be obtained for different values of $V_O$ to guarantee $i_{Lr}$ is within $I_{max}$ under the nominal input voltage $V_{in,nom}$ based on the corresponding trajectory shown in Fig. 2.20. The switching period is then calculated as below to derive the $f_S$ vs. $V_O$ table for Stage 2, which then linearized piece-wise and stored in the MCU.

\[
\alpha = \sin^{-1}(I_{maxN}/\rho_1); \beta = \sin^{-1}(I_{maxN}/\rho_2) \\
T_S = 2(\alpha + \beta)/\omega_o
\]

Stage 3 for this method is the same as that of the OTC for soft start-up, just decreasing $f_S$ gradually until $V_O = 12V$ and then merging with closed-loop control.
In this method, the $\Delta T$ table and the $f_S$ vs. $V_O$ table are calculated based on $V_{in,nom}$ and given $L_r$ and $C_r$ values, because different tables based on $V_{in}$ will increase the memory requirement, and on-line measurement of $L_r$ and $C_r$ is not practical. Thus the impact of variation of $V_{in}$ and the tolerance of $L_r$ and $C_r$ need to be considered under such conditions. The impact of variation of $V_{in}$ is analyzed as follows: $I_{max}$ is determined using $V_{in,nom}$. The tables are calculated based on $I_{maxN}$ as expressed below. The same tables are applied under different $V_{in}$ conditions, then the relationship between current stress $I_{stress}$ and $V_{in}$ is expressed below, which shows clearly that $I_{stress}$ is proportional to $V_{in}$. Since $V_{in}$ is normally within a certain range ($\pm 5\%$), the variation of $I_{stress}$ is also very small.
\[
I_{\text{max}N} = \frac{I_{\text{max}}}{\sqrt{V_{\text{in, nom}}/C/\sqrt{L}}}
\]  
\[
I_{\text{Stress}}(V_{\text{in}}) = I_{\text{max}N} \cdot \frac{V_{\text{in}}}{\sqrt{L}/C}
\]

The impact of the tolerance of \( L_r \) and \( C_r \) is estimated by simulation, as shown in Fig. 2.21. The start-up conditions are \( V_{\text{in}} = 390 \text{V} \) and \( \text{load} = 25 \text{A} \) (full-load). The table is calculated based on \( L_r = 60 \text{uH} \) and \( C_r = 24 \text{nF} \). Fig. 2.21(a) shows the case without tolerance, and \( I_{\text{stress}} = 3.60 \text{A} \) compared to the full-load steady-state current stress of around 3A. Fig. 2.21(b) shows the case with +5\% tolerance for both \( L_r \) and \( C_r \), and the \( I_{\text{stress}} = 3.40 \text{A} \), which is around 6\% less than the nominal case. Fig. 2.21(c) is the case with -5\% tolerance for both \( L_r \) and \( C_r \), and the \( I_{\text{stress}} = 3.91 \text{A} \), which is around 9\% higher than the nominal case. So the impact of the tolerance of \( L_r \) and \( C_r \) is small, because ±5\% tolerance will result in less than 9\% current stress variation.

![Simulation of proposed method for soft start-up with \( L_r, C_r \) tolerance for 130kHz LLC converter](image)

Fig. 2.21. Simulation of proposed method for soft start-up with \( L_r, C_r \) tolerance for 130kHz LLC converter

This method is applicable to different load conditions because even under different loads, the output can still be considered as a constant voltage source within several switching cycles. The load conditions have an impact on the duration of the whole start-up process, but will not have an impact on \( i_{L_r} \) stress. While the table is derived for given power stage parameters and \( V_{\text{in}} \), it is still
suitable for a given $V_{in}$ range and is sufficiently robust for the tolerance of the resonant tank. It is worth noting that the parasitic has little impact on the proposed start-up using the $f_s$ vs. $V_o$ table due to the following reasons: for LLC converters, parasitic may have large impact on the input/output gain at very light load conditions, but it has very little effect on the input/output gain at the heavy load conditions; the proposed start-up controls the LLC converter with a current limiting band slightly larger than the full-load current stress, which means that during the whole start-up process, the converter’s operation is always equivalent to heavy load conditions; so the small error caused by the parasitic will only have very little impact on $i_L$ majorly determined by the $f_s$ vs. $V_o$ table during the start-up process. It is recommended to leave +20% margin for $I_{max}$, so that the impact of parasitic and tolerance for start-up can be compensated to guarantee the converter can start-up under any conditions.

2.2.2. Soft start-up for high-frequency LLC converters

The state-trajectory control is basically a cycle-by-cycle control, which means that the control cycle should be based on the switching cycle of the power stage, so that the controller can record the status of the resonant tank and integrate other state-trajectory control functions [32][33][34][35]. In the proposed implementation with look-up tables, the switching times are controlled by the CPU of the MCU. Hence there is a limitation in $f_s$ with a given performance of the CPU if the control cycle is set to be equal to the switching cycle. The 60MHz MCU TMS320F28027 selected in this section is normally used to control the LLC converter with an $f_o$ of around 70kHz - 130kHz. The analysis below investigates how to use this MCU for the LLC converter with an $f_o$ above 500kHz. The control system is programmed to fully utilize the controller resource. When the system is reset, the MCU generates $\Delta T_1, \Delta T_2 ... \Delta T_n$ subsequently for Stage 1. Since the code is optimized with the system initialization, it actually takes only a few
CPU cycles (around 25 CPU cycles) to execute Stage 1 for each control cycle. In Stage 2, the MCU senses $V_o$ through ADC and refers to the $f_S$ vs. $V_o$ table to determine $f_S$ for Stage 2, which takes around 130 CPU cycles to execute once. In Stage 3, it takes a few more CPU cycles than Stage 2 (around 180 CPU cycles to execute once) because the MCU needs to gradually merge with the closed-loop control.

The switching instants for Stage 1 is shown in Table 2.2. These analyses are based on a 130kHz 300W LLC converter with $L_n \approx 5$, as referred to above, and a 500kHz 1kW LLC converter with $L_r = 4.5uH$, $C_r = 22nF$, and $L_m = 22uH$. The same methodology applies to the design of different power stages. 25 CPU cycles in a 60MHz MCU is equivalent to 418ns, so there is enough time for the MCU to update the PWM module, even for a 500kHz LLC converter.

<table>
<thead>
<tr>
<th>Time interval</th>
<th>130kHz LLC converter</th>
<th>500kHz LLC converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta T_1$</td>
<td>808ns</td>
<td>210ns</td>
</tr>
<tr>
<td>$\Delta T_2$</td>
<td>2096ns</td>
<td>544ns</td>
</tr>
<tr>
<td>$\Delta T_1 + \Delta T_2 (f_S)$</td>
<td>2904ns (344kHz)</td>
<td>754ns (1.33MHz)</td>
</tr>
<tr>
<td>$\Delta T_3$</td>
<td>1163ns</td>
<td>302ns</td>
</tr>
<tr>
<td>$\Delta T_4$</td>
<td>1646ns</td>
<td>428ns</td>
</tr>
<tr>
<td>$\Delta T_3 + \Delta T_4 (f_S)$</td>
<td>2809ns (356kHz)</td>
<td>730ns (1.37MHz)</td>
</tr>
</tbody>
</table>

Since the maximum start-up frequency $f_{S_{\text{max}}}$ of Stage 2 is much higher than that of Stage 3, and it takes many more CPU cycles for Stage 2 than Stage 1, the limitation for the soft start-up is the beginning of Stage 2. To ensure that there is enough time for the MCU to update PWM, which takes around 130 CPU cycles, the PWM module can be configured to be updated every $n^{th}$ switching cycle ($n = 1, 2, 3 \ldots$). Then $f_{S_{\text{max}}}$ must satisfy:
\[ \frac{n}{f_{S, \text{max}}} > \frac{130}{60 \text{MHz}} \]  

(2.15)

The summary for \(f_{S, \text{max}}\) under different PWM updating speeds is listed in Table 2.3, and the graph of \(f_S\) vs. \(V_o\) for the 130kHz LLC converter and the 500kHz LLC converter is shown in Fig. 2.22. For the 130kHz LLC converter, the maximum \(f_S\) is around 300kHz, so the PWM can be updated every switching cycle. For the 500kHz LLC converter, the maximum \(f_S\) is around 1.1MHz, so the PWM is updated every 3\(^{rd}\) switching cycle.

Fig. 2.23 provides a comparison between PWM updating speeds of every switching cycle and every 3\(^{rd}\) switching cycle. For both cases, the sampling and A/D is at the end of the previous control cycle, and the calculation, which includes looking up the \(f_S\) vs. \(V_o\) table and PWM update, starts at the beginning of each control cycle. A comparison has been made to verify \(V_o\) variation for different PWM updating speeds as shown in Fig. 2.24. The simulation is based on the 500kHz LLC converter referred above with an output capacitor of 3mF and under 80A constant-current load. Slower updating speed will increase \(V_o\) variation, but due to the long start-up process, \(V_o\) variation between two consecutive PWM updates is still very smaller compared to nominal \(V_o\), for example, the worst case is 70mV, which is equivalent to around 0.6\% of nominal \(V_o\).

<table>
<thead>
<tr>
<th>PWM updating speed</th>
<th>(f_{S, \text{max}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Every switching cycle</td>
<td>460kHz</td>
</tr>
<tr>
<td>Every 2(^{nd}) switching cycle</td>
<td>920kHz</td>
</tr>
<tr>
<td>Every 3(^{rd}) switching cycle</td>
<td>1.38MHz</td>
</tr>
</tbody>
</table>

Table 2.3. \(F_{S, \text{MAX}}\) under Different PWM Updating Speeds
Fig. 2.22. $f_s$ vs. $V_O$ for 400V/12V 130kHz and 500kHz LLC converters.

(a) Every switching cycle.  
(b) Every 3rd switching cycle.

Fig. 2.23. Comparison between different PWM updating speeds.

Fig. 2.24. Comparison of $V_O$ variation under different PWM updating speeds
If $f_s$ is further pushed to even higher, then either a higher-performance MCU or a slower PWM update speed is needed. And $V_o$ variation within one control cycle can be analyzed accordingly to guarantee that the proposed start-up is still valid for given parameters.

2.2.3. Experimental results

The proposed soft start-up is verified on the 500kHz LLC converter in Fig. 2.11, which has a full-load steady-state $i_{Lr}$ stress of around 10A. Considering the impact of $V_{in}$ variation and resonant tank tolerance, both of which contributes 10\% $i_{Lr}$ stress variation, 14A current stress is selected as the current limiting band for calculating the $f_s$ vs. $V_o$ table to ensure that the converter is able to start-up under any conditions. The experimental results of soft start-up with different resistive loads under $V_{in} = 385V$ are shown in Fig. 2.25. Since the LLC converter works like a constant current source with the proposed control method during start-up, $i_{Lr}$ stress for both cases are the same. Most of the output current charges the output capacitor while the rest is dissipated by the load, so it takes a little bit longer to finish the start-up process for the 0.178Ω load conditions.

(a) Load = 0.35Ω (40% load). (b) Load = 0.178Ω (80% load).

Fig. 2.25. Soft start-up under different resistive loads with $V_{in} = 385V$. 
This section provides an investigation of optimal trajectory control (OTC) for soft start-up and the limitations of its MCU implementation. Digital delay has a significant impact on the stresses during start-up if directly employing the concept of OTC for soft start-up. An MCU-based implementation with look-up tables is proposed to overcome this challenge, which only requires sensing the output voltage. The look-up tables for different stages in the soft start-up are derived based on the concept of OTC for soft start-up and the state-plane analysis. The proposed method is then extended to high-frequency LLC converters without increasing the cost for the controllers. The method is proven by theoretical analysis and simulation to be robust enough to handle input voltage variations and resonant tank tolerances.

2.3. Short-circuit protection

Short-circuit protection is very critical for front-end converters, especially when parallel operation is required. The converter is required to provide different output characteristics according to the load conditions: the converter should provide constant \( V_o \) from no load to full-load condition; if the load exceeds full-load power, the converter should be able to operate at constant power or constant current mode; furthermore, if \( V_o \) is shorted by a very small impedance under fault condition, the converter should be able to not only protect itself when \( V_o \) is shorted, but also start-up again after the short-circuit condition is removed. The transient from constant voltage mode to constant power mode or constant current mode is relatively slow, and its control can be inherently achieved by controlling \( f_s \) according to the \( f_s \) vs. \( V_o \) table in Section III since \( V_o \) drops slowly and \( V_o \) variation is very small within two consecutive control cycles for the digital controller, meaning that the impact of digital delay is very small. As a comparison, under the protection mode, i.e. \( V_o \) is shorted by a very small impedance, \( V_o \) drops abruptly and it cannot be
considered as stable over several switching cycles. Digital delay in the controller would have a significant impact since $V_o$ may change greatly within two consecutive control cycles. And this effect will become more severe for the high-frequency LLC converters with low-cost digital controllers. It is of great meaning to investigate the impact of digital delay on the response of the converter under such abrupt short-circuit condition caused by a very small impedance, and figure out methods to minimize digital delay impact.

2.3.1. Impact of digital delay on short-circuit protection

The protection under short-circuit is normally tested by shorting $V_o$ using a wire directly. The converter is tested as illustrated in Fig. 2.26; when $V_o$ is shorted during the normal operation, the converter should be able to limit its stresses; and when the short-circuit condition is removed, the converter should be able to build up $V_o$ again. It is worth noting that although Fig. 2.26 is a conceptual drawing, a converter satisfying the requirement in Fig. 2.26 is able to handle a varieties of real conditions, for example, a short-circuit could happen, then disappear and then appear again. This is because if the converter is able to handle the transient between normal operation to short-circuit, it can handle the repetitive short-circuit conditions.

The analysis regarding digital delay impact is verified by simulation as shown in Fig. 2.27, in which $V_o$ is shorted by a 10mΩ resistor during full-load steady-state operation. Fig. 2.27(a) is the case without digital delay, which shows little $i_{Lr}$ stress increase compared to full-load stress after short-circuit occurs. Fig. 2.27(b) is the case with a digital delay of three switching cycles, which shows a significant $i_{Lr}$ stress increase of up to three times the full-load current stress after short-circuit occurs.
Fig. 2.26. Short-circuit protection test procedure.

Fig. 2.27. Simulation of short-circuit protection using $f_s$ vs. $V_o$ table for 500kHz LLC converter.

Overcoming the limitations caused by digital delay in short-circuit protection using the $f_s$ vs. $V_o$ table requires either a very fast digital controller or a very huge output capacitor. A very fast digital controller may limit digital delay to a certain range that would minimize the digital delay impact but would also increase the cost significantly. A huge output capacitor may help slow down $V_o$ drop when short-circuit occurs, but in order to limit the stress, the required capacitance would be much larger than the industrial practice, resulting in a larger footprint as well as a higher cost.
2.3.2. Proposed method for short-circuit protection

To solve this challenge in the short-circuit protection for the high-frequency LLC converters with low-cost digital controllers, this section proposes a protection method based on load current $i_{\text{Load}}$ that can be easily combined with the proposed soft start-up presented in Section III. Fig. 2.28 shows the proposed control scheme combining soft start-up and short-circuit protection. $V_o$ is sensed for soft start-up, and $i_{\text{Load}}$ is sensed to provide a fast response to short-circuit. Sensing $i_{\text{Load}}$ is quite a common practice in power supplies for the IT industry due to the power management requirements. Advanced control methods such as SOTC already includes $i_{\text{Load}}$ in the control system to achieve the benefit of fast transient response. The proposed control scheme is quite similar to that of SOTC, and thus both methods can be integrated into the same digital controller without increasing the cost or adding an auxiliary circuit.

Fig. 2.28. Proposed control scheme for soft start-up and short-circuit protection.

The basic control principle of the proposed short-circuit protection is illustrated in Fig. 2.29. During normal operation, the controller senses $V_o$ and converts it through A/D for closed-loop control. Meanwhile, the controller senses $i_{\text{Load}}$ and compares it with the pre-set over-current threshold. This comparison function could be implemented by the integrated comparator peripheral within the digital controller or by an external comparator to minimize digital delay.
When $V_O$ is shorted, there would be a huge current drawn from the output capacitor, which would trigger short-circuit protection, and then the controller would set $f_S$ to the pre-determined short-circuit switching frequency $f_S_{short}$ to minimize the stresses. During the short-circuit conditions, the controller keeps monitoring $V_O$ and compares it with a recover threshold. When the short-circuit condition is removed, $V_O$ will increase gradually and the controller will begin the soft start-up process when $V_O$ reaches the recovery threshold. The proposed short-circuit protection method is verified by simulation, as shown in Fig. 2.30. When $V_O$ is shorted by a 10mΩ resistor during full-load steady-state operation, the controller is able to respond very quickly to limit $i_{Lr}$ stress.

![Diagram illustrating the proposed short-circuit protection method.](image)

**Fig. 2.29.** Illustration of the proposed short-circuit protection method.

![Simulation of proposed short-circuit protection for 500kHz LLC converter.](image)

**Fig. 2.30.** Simulation of proposed short-circuit protection for 500kHz LLC converter.
Another important consideration for the short-circuit protection is to limit the system thermal stress. In order to not increase the cost for heat dissipation, the total loss under short-circuit conditions should be kept below the total loss under full-load condition in normal operation. Loss analysis under short-circuit condition has been made for the 1kW 500kHz 400V/12V LLC converter. The primary is a half-bridge configuration, and the secondary consists of four sets of outputs. The total losses with different $f_{S\_short}$ under short-circuit condition are shown in Fig. 2.31. The $f_{S\_short}$ is selected as 1.6MHz to fulfill the system thermal requirements.

![Loss vs. $f_{S\_short}$ under short-circuit for 500kHz LLC converter](image)

Fig. 2.31. Total loss vs. $f_{S\_short}$ under short-circuit for 500kHz LLC converter.

### 2.3.3. Experimental results

The experimental results of the proposed short-circuit protection and its recovery are shown in Fig. 2.32. The short-circuit condition is emulated by the short-circuit function of the electronic load, and the total short-circuit resistance is around 10mΩ ~ 20mΩ. In Fig. 2.32(a), the converter operates in the normal condition with 40A load at the beginning. When short-circuit occurs, $V_O$ drops to almost 0V and the converter is able to limit $i_L$ stress immediately. In Fig. 2.32(b), when short-circuit is removed, $V_O$ starts rising; after $V_O$ meets the recover threshold, the converter begins the soft start-up process and builds up $V_O$ gradually to 12V.
(a) Protection.  

(b) Recovery.

Fig. 2.32. Short-circuit protection and recovery.

The experimental results of using “hiccup” mode to reduce the thermal stress during short-circuit conditions are shown in Fig. 2.33. In this case, the converter operates with an $f_s$ of 1.6MHz for around 6ms, and stops for around 24ms. The converter would repeat this process until the short-circuit condition is removed and the converter would recovery to normal operation.

Fig. 2.33. “Hiccup” mode to reduce thermal stress during short-circuit condition

Based on the concept of simplified optimal trajectory control (SOTC), a short-circuit protection method is proposed that senses the load current to minimize the impact of digital delay. The total loss during the short-circuit condition under different switching frequencies is analyzed,
and guidelines are provided to select a suitable switching frequency for short circuit. “Hiccup” mode is employed to further reduce the thermal stress. The proposed soft start-up and short-circuit protection have a control scheme which is similar to that of SOTC, and thus they are suitable for integration with other SOTC control functions.

2.4. Burst mode for light load efficiency improvement

Burst mode is widely used to improve the light load efficiency of the LLC converters. The concept of burst mode is to switch the converter between ON and OFF mode. During the burst-ON time, the converter runs at the efficiency-optimal point. While during the burst-OFF time, the converter is shut down and there is no energy delivered to the load. The average power of the whole burst period equals to the power required by the load so that the output voltage is stabilized around the reference. The comparison of the conventional frequency control and the burst mode control is shown in Fig. 2.34.

![Diagram](image)

(a) Frequency control

(b) Burst mode control

Fig. 2.34. Comparison of frequency control and burst mode control
The burst mode on-time is defined as $T_{\text{burst}}$, and off-time defined as $T_{\text{off}}$. $P_{\text{OPT}}$ is the power delivered to the secondary side during the burst on-time. Then the burst duty cycle $D_{\text{burst}}$ and the average power $P_{\text{average}}$ for burst mode are expressed as below:

$$D_{\text{Burst}} = \frac{T_{\text{Burst}}}{T_{\text{Burst}} + T_{\text{off}}}$$  \hspace{1cm} (2.16)

$$P_{\text{Average}} = P_{\text{OPT}} \cdot D_{\text{Burst}}$$  \hspace{1cm} (2.17)

Ideally, burst mode can boost the light efficiency to the optimal efficiency by settling the resonant tank to the efficiency-optimal state during the burst-ON time. However, it is challenging to control the resonant converters during the burst on-time due the complex control characteristics caused by the dynamics of the resonant tank.

The previous burst mode control methods cannot fix to the highest-efficiency status during the burst on-time since the switching frequency during the burst on-time is controlled by the compensator rather than optimized for the resonant tank, and the output voltage ripple is very large. To solve this problem, Optimal Trajectory Control (OTC) of burst mode for LLC converter uses the fixed 3-pulse pattern for the burst on-time and constant burst-on time implementation for the closed-loop control. Fig. 2.35 is the illustration of the fixed 3-pulse pattern in OTC for burst mode with time-domain waveforms in Fig. 2.35(a) and corresponding state-trajectory in Fig. 2.35(b). In the fixed 3-pulse pattern, the first pulse settles the resonant tank from the burst mode initial point to the highest-efficiency load trajectory; then the second and the third pulse would follow the highest-efficiency load trajectory; after the third pulse, all the switches are turned off, and the state-trajectory comes to the burst mode initial point after a little oscillation cause by the energy in the magnetizing inductor.
With the calculation in [25], the length of the first pulse is normally around \( \frac{1}{4} T_0 \), in which \( T_0 \) is the resonant period. The length of the first pulse may have some variation for different power stage designs. Since the second and the third pulse follow the highest-efficiency load trajectory, both their lengths are around the half of the resonant period. The third pulse may be a little bit smaller than the half of the resonant period in order to settle the resonant tank to the burst mode initial point, but it can still be treated approximately as the half of the resonant period in the following analysis.

2.4.1. **Digital implementation of burst mode**

An example of digital implementation of OTC for burst mode based on MCU (TMS320F28027) is shown in Fig. 2.36. The basic control scheme is constant burst-on time control. When the output voltage is below the reference, which is 12V in this example, the controller would...
generate the fixed 3-pulse pattern. After that, there would a 1us blanking time to avoid the noise from the oscillation. Then the controller would sample the output voltage, compare it with the reference and determine whether updating PWM for the next burst on-time. The control loop in the off-time is executed every 2us. The sampling includes the load current for system power management and the control loop includes over-current monitor and transition to normal operation.

![Diagram](image)

Fig. 2.36. Digital implementation of OTC for burst mode

The off-time in the constant on-time control is variable and dependent on the load condition. When the load becomes lighter, the off-time is increased so that the average power is decreased. When the load becomes heavier, the off-time decreases. While the on-times for different load conditions are always the same to ensure the small output voltage ripple.

For the digital implementation of OTC for burst mode, there would be a minimum off-time limitation, an example of which based on MCU (TMS320F28027) is shown in Fig. 2.37. The case with the minimum off-time happens when the first sampling of the output voltage, which is just after the 1us blanking time, is equal to or below the reference. The first control loop execution after the 1us blanking time is the sampling and the A/D conversion of the output voltage and the load current. The second control loop updates PWM for the burst on-time. The first pulse of the 3-
pulse pattern is also classified as off-time in the following analysis, since the first pulse is used to settle the resonant tank and there is no energy delivered to the secondary side within the first pulse.

![Diagram](image)

**Fig. 2.37. Minimum off-time limitation in the digital implementation of OTC for burst mode**

Deriving from the analysis above, the minimum off-time consists of 1us blanking time, twice execution of the control loop, and the first pulse of the fixed 3-pulse pattern. And the on-time is the later 2 pulses in the fixed 3-pulse pattern. Corresponding to the minimum off-time, the maximum burst duty cycle and the maximum average power is expressed as below

$$D_{\text{Burst\_max}} = \frac{T_{\text{Burst}}}{T_{\text{Burst}} + T_{\text{off\_min}}} = \frac{T_o}{\frac{5}{4}T_o + 5us} \quad (2.18)$$

$$P_{\text{Average\_max}} = P_{\text{OPT}} \cdot D_{\text{Burst\_max}} \quad (2.19)$$

With the equation for the maximum burst duty cycle $D_{\text{Burst\_max}}$, the relationship between $D_{\text{Burst\_max}}$ and the resonant frequency $f_o$ is shown in Fig. 2.38. In which $D_{\text{Burst\_max}}$ for a 130kHz LLC converter and a 500kHz LLC converter is marked for comparison. The resonant frequency is normally selected below 130kHz for the commercial products, which means that the $D_{\text{Burst\_max}}$ will be large than 50% and there will enough burst mode operation range.
However, when the switching frequency is pushed higher, for example 500kHz, the $D_{\text{Burst\_max}}$ decreases to 26.7% and there would be a problem in the burst mode operation range if the burst on-time is still the fixed 3-pulse pattern. Fig. 2.39 takes the 500kHz LLC converter as an example. The peak efficiency is at 60% load condition. With a maximum burst duty cycle $D_{\text{Burst\_max}}$ of 26.7%, the maximum average power $P_{\text{average\_max\_1}}$ is only 16% load condition. So the burst mode can be applied from no load to only 16% load condition.

Fig. 2.39. Expected efficiency curve of OTC for burst mode with fixed 3-pulse pattern on a 500kHz LLC converter
2.4.2. Multi-step burst mode for high-frequency LLC converters

When the OTC for burst mode of the LLC converters is implemented by the digital controllers, there is always the limitation of the maximum burst duty cycle caused by the digital delay and the fixed 3-pulse pattern. For given controller, the higher the switching frequency of the LLC converters, the smaller this maximum burst duty cycle is. Corresponding to the maximum burst duty cycle and the burst on-power, the burst mode operation range is limited by the maximum average power. To solve this problem, the multi-step Simplified Optimal Trajectory Control (SOTC) for burst mode is proposed below. Fig. 2.40 is the comparison of burst modes with different $T_{Burst}$ under same $T_{off, min}$. For the burst mode with 5-pulse pattern, the first pulse is still used to settle the resonant tank, which is the same as the first pulse of the 3-pulse pattern. The following 4 pulses follow the highest-efficiency load trajectory, and they are the same as the later 2 pulses in the 3-pulse pattern. Since the minimum off-time are the same for both cases and the burst on-time of the 5-pulse pattern is larger, the maximum burst duty cycle of the 5-pulse pattern is larger, resulting in a larger maximum average power.

![Diagram](image)

(a) 3-pulse switching pattern  
(b) 5-pulse switching pattern

Fig. 2.40. Comparison of burst modes with different $T_{Burst}$ under same $T_{off, min}$

Following the concept of increasing the burst on-time, the SOTC for burst mode with adaptive multi-step is proposed, as illustrated in Fig. 2.41. The first pulse is always the same as that in the fixed 3-pulse pattern in OTC for burst mode, in order to settle the burst on-power to the highest-
efficiency point. The pulses following the first pulse always have the length of around half the resonant period. The number of the pulses can be selected as 3, 5, 7, and 9 … depending on the load condition.

Fig. 2.41. Concept of SOTC for burst mode with adaptive multi-step

Take a 500kHz LLC converter as an example, the table of pulse number, $T_{\text{Burst}}$, $D_{\text{Burst\_max}}$ and $P_{\text{Average\_max}}$ is shown in Table 2.4. For different load condition, the pulse number can be selected according to $P_{\text{Average\_max}}$.

Table 2.4. Relationship between pulse number and $P_{\text{AVE\_max}}$ for a 500kHz LLC Converter

<table>
<thead>
<tr>
<th>Pulse #</th>
<th>3</th>
<th>5</th>
<th>7</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{Burst}}$</td>
<td>2us</td>
<td>4us</td>
<td>6us</td>
<td>8us</td>
</tr>
<tr>
<td>$D_{\text{Burst_max}}$</td>
<td>26.7%</td>
<td>42.1%</td>
<td>52.2%</td>
<td>59.3%</td>
</tr>
<tr>
<td>$P_{\text{Average_max}}$</td>
<td>16.0% $\cdot P_{\text{Full}}$</td>
<td>25.3% $\cdot P_{\text{Full}}$</td>
<td>31.3% $\cdot P_{\text{Full}}$</td>
<td>35.6% $\cdot P_{\text{Full}}$</td>
</tr>
</tbody>
</table>

The expected efficiency curve of the proposed SOTC for burst mode with adaptive multi-step on a 500kHz LLC converter is illustrated in Fig. 2.42. The 3-pulse pattern is used from no load to 16% load; the 5-pulse pattern is used from 16% load to 25.3% load; the 7-pulse pattern is used
from 25.3% load to 31.3% load; and the same analogy applies until the load reaches the highest-efficiency point in the ideal case. Since the pulse number is dependent on the load condition, the output voltage ripple is still very small at very light load condition with the 3-pulse pattern, and has very little variations as the pulse number increases due to the increased load current.

![Efficiency Curve](image)

**Fig. 2.42.** Expected efficiency curve of the proposed SOTC for burst mode with adaptive multi-step on a 500kHz LLC converter

### 2.4.3. Experimental results

The waveforms of the proposed SOTC for burst mode with adaptive multi-step are shown in Fig. 2.43, including: the 3-pulse pattern @ load = 4A; the 5-pulse pattern @ load = 12A; and the 7-pulse pattern @ load = 18A. It is shown clearly that the resonant current fixes to the same power level during the burst on-time and the output voltage ripple has very small variations under different conditions.
Fig. 2.43. Waveforms of the proposed SOTC for burst mode with adaptive multi-step.

The efficiency curve of the proposed SOTC for burst mode with adaptive multi-step is shown in Fig. 2.44. The efficiency curves of the normal operation and the state-of-art burst mode are also drawn as comparison. The efficiency curves show that the light load efficiency improvement of the proposed SOTC for burst mode with adaptive multi-step is significant. The converter enters burst mode when load condition is below 26% load. And it can achieve 92.5% efficiency at 10% load and 91.8% efficiency at 2.4% load.
There are some differences between the experimental efficiency curve and the expected ideal efficiency curve; the reasons include: the first pulse is hard switching turn-on; the energy in the first pulse is circulating energy and there is no power delivered to the secondary side within the first pulse; the oscillation between \( L_r, L_m \) and \( C_{oss} \) after the last pulse turn-off will induce extra loss.

In this section, the Optimal Trajectory Control (OTC) for burst mode of the LLC converters is investigated and its limitation in the high frequency LLC converters with the digital implementation is explained in detail. The burst operation range is limited when applied to the high frequency LLC converters due to the small minimum off-time caused by the digital delay and the small burst on-time caused by the high switching frequency. To solve this challenge, the Simplified Optimal Trajectory Control (SOTC) for burst mode with adaptive multi-step is proposed. The proposed burst mode with adaptive multi-step adjusts the pulse number for the burst on-time based on the load condition to extend the burst operation range.
2.5. Adaptive SR driving

The SR driving scheme is quite challenging due to the discrepancy between the primary driving signal and the SR driving signal, especially under high $f_s$. Key waveforms with desired SR driving signal under different $f_s$ are shown in Fig. 2.45, including Q1 gate signal $V_{gs,Q1}$, resonant current $i_{Lr}$, magnetizing current $i_{Lm}$, transformer secondary current $i_{SEC}$, SR2 gate signal $V_{gs,SR}$. If $f_s$ is below the resonant frequency $f_o$, the SR on-time $T_2$ is smaller than the primary switch on-time $T_1$; if $f_s$ is above $f_o$, $T_2$ is larger than $T_1$; if $f_s$ is equal to $f_o$, $T_2$ is equal to $T_1$. Besides, $T_2$ is also dependent on the load condition. So the primary driving signal cannot be applied directly to the SRs. In addition, deviation from the desired SR driving will cause efficiency drop due to a large forward conduction voltage in the body diode. This problem becomes more severe at high $f_s$ since a small deviation occupies a large portion of the duty cycle.

![Fig. 2.45. Key waveforms with desired SR driving under different $f_s$](image)

To figure out an SR driving scheme suitable for low-cost digital implementation, different SR driving schemes are investigated in this section. Current sensing based SR driving schemes [42][43][44], induce a large loss and are hardly ever used. Most of the SR driving schemes nowadays are based on sensing $V_{dc,SR}$, which does not induce extra loss. The commercialized SR driving smart ICs can work as independent driving circuit at the secondary side and do not require
primary control signals [45][46][47]. These smart ICs work in the following principle as shown in Fig. 2.46(a): at the beginning, the SR is in the off-state; when there is a body diode conduction, it results in a large forward voltage drop in $V_{ds_{SR}}$, which is compared with the turn-on threshold voltage $V_{th_{on}}$; if the $V_{ds_{SR}}$ is larger than $V_{th_{on}}$, the SR driving IC turns on the SR; in the LLC converters, during the SR on-time, the current in SR $i_{SR}$ will, first increase and then decrease to zero; as the current approaches zero, $V_{ds_{SR}}$ also becomes very small, which is compared with the turn-off threshold voltage $V_{th_{off}}$ to determine when to turn off the SR. However, the accuracy of the SR driving schemes in the second category is highly affected by the SR package. The actual SR on-time is shorter than the expected value and there is a related duty-cycle loss due to the inevitable package inductance of the SRs, as shown in Fig. 2.46(b). This problem is extremely severe in high-frequency applications since even a very small package inductance can induce a large phase leading in $V_{ds_{SR}}$. A compensation network can be connected to the sensed terminals to solve this problem [48], but it is very complex and also impacted by the tolerance of the compensation network.

![Waveforms of smart IC based SR driving](image.png)

(a) Without parasitic inductance  
(b) With parasitic inductance

Fig. 2.46. Waveforms of smart IC based SR driving

Adaptive SR driving can solve the issue of an extra body diode conduction in a smart IC based SR driving when operating at high $f_s$ by detecting the body diode conduction after SR turn-off [49][50][51]. The turn-on of the SR can be synchronized with the primary driving signal under
different conditions as shown in Fig. 2.47, however the turn-off tuning mechanisms are different. The control scheme and waveforms of the adaptive SR driving scheme [49] are shown in Fig. 2.47. The $V_{ds_{SR}}$ is detected and compared with a threshold voltage $V_{th}$. The output of the comparator is connected to the input of a linear compensator. The control signal of the linear compensator is connected to the positive input of the pulse-width modulation (PWM) generator, and a triangular waveform generated from the primary driving signal is connected to the negative input of the PWM generator. If the body diode conduction is detected, i.e. $V_{ds_{SR}}$ is larger than $V_{th}$ for some time, the compensator output will increase, so as the SR on-time $T_2$. If no body diode conduction is detected, the compensator will decrease $T_2$ accordingly. The final steady state will have the minimum body diode conduction. There would be two major limitations if this SR driving scheme is integrated within the cost-effective digital controllers. The first limitation is that it requires a linear compensator, which would either require the additional circuit or occupy a lot of CPU resources. The second limitation is that since the negative input of the PWM generator is the primary driving signal, $T_2$ cannot be large than the corresponding $T_1$, which is not suitable when $f_S$ is above $f_0$.

Fig. 2.47. Adaptive SR driving scheme using a linear compensator
The control scheme and flowchart of the adaptive SR driving scheme using digital tuning [50] are shown in Fig. 2.48. The turn-on of the SRs in the LLC converters is synchronized with the primary switches. $V_{ds_{-}SR}$ is sensed just at the falling edge of $V_{gs_{-}SR}$ and compared to $V_{th}$. The output of the comparator indicates if there is a body diode conduction. The digital SR controller would increase or decrease the SR duty cycle by $\Delta D$ accordingly for the next switching cycle. The SR duty cycle will approach the optimal condition step-by-step, and finally be stabilized around the optimal condition. Reference [51] uses similar adaptive SR driving concepts and integrates this function into an IC chip, but this IC is dedicated to digital controller UCD3138A and requires complex communication protocol with the digital controller.

(a) Control scheme  
(b) Control flowchart

Fig. 2.48. Adaptive SR driving scheme using digital tuning

The limitation with these SR driving schemes is that they require complex algorithm and comparing the $V_{ds_{-}SR}$ to $V_{th}$ just at the falling edge of $V_{gs_{-}SR}$. The implementation of this function requires either an FPGA controller or an additional logic circuit as demonstrated in [50][51], which cannot be integrated within the cost-effective digital controllers. Further efforts need to be spent on integrating adaptive SR driving into low-cost digital controllers. How to guarantee safe SR operation during a fast transient response has also not been addressed yet. Furthermore, when
applied to high-frequency LLC converters, tuning the SR on-time every switching cycle in the digital controller will greatly increase the CPU utilization and consume much more auxiliary power. The following presents how to solve these issues with a low-cost digital controller.

### 2.5.1. Digital implementation of adaptive SR driving

The adaptive SR driving scheme can be integrated within the digital controllers by using ripple detection, whose control scheme is shown in Fig. 2.49. The $V_{ds,SR}$ is sensed and compared with $V_{th}$ to detect body diode conduction, and the output of the comparator $V_{CMP}$ is connected to the ripple detection function of the digital controller, i.e. the external interrupt of the MCU, based on which the on-time of SR is tuned accordingly. Since the adaptive SR driving scheme is integrated within the digital controller, the primary driving signal can be used to synchronize the turn-on of SR and control the enable/disable of the ripple detection.

![Fig. 2.49. Integrating adaptive SR driving in the low-cost digital controller](image)

The control mechanism of the integrated adaptive SR driving is shown in Fig. 2.50. Since there is a small body diode conduction period at the SR turn-on moment, only the ripple at $V_{CMP}$ in the shaded area will be detected by controlling the enable/disable of the ripple detection based on the primary driving signal. The ripple detection is enabled at the middle of the primary switch
on-time, and disabled after SR turn-off. In Fig. 2.50, at the beginning, there is large body diode conduction, the controller increases $T_2$ by $\Delta T$, which is the minimum resolution of the digital controller; and this process continues until no ripple at $V_{CMP}$ in the shaded area is detected; then the controller decreases $T_2$ by $\Delta T$. In the steady state, the SR on-time will jitter between the condition with no body diode conduction and that with a very small body diode conduction as shown in the two conditions at the bottom of Fig. 2.50. It is optimal for the adaptive SR driving to jitter between these two conditions; otherwise, if the SR on-time stays in the condition with no body diode conduction, when $f_S$ increases, the adaptive SR driving cannot reduce the SR on-time accordingly.

![Control mechanism of integrated adaptive SR driving schemes](image)

Fig. 2.50. Control mechanism of integrated adaptive SR driving schemes

The CPU utilization can be estimated when integrating the adaptive SR driving into the digital controller. Take a 60MHz MCU TMS320F28027 as an example. It takes 10 CPU cycles to enable or disable the ripple detection, and around 30 CPU cycles to modify SR on-time for the next switching cycle when there is ripple detected and the interrupt in the MCU is triggered, as shown
in Fig. 2.51. So the total adds up to a maximum of 50 CPU cycles within one switching cycle to implement such an adaptive SR driving scheme. The CPU utilization for SR driving $\eta_{SR}$ is calculated as follows:

$$m_{total} = \frac{f_{clock}}{f_s}$$  \hspace{1cm} (2.20)

$$\eta_{SR} = \frac{m_{SR}}{m_{total}}$$  \hspace{1cm} (2.21)

Where $f_{clock}$ is the clock frequency of the digital controller, $m_{total}$ is the total CPU cycles within one switching cycle, and $m_{SR}$ is the required CPU cycles for adaptive SR driving within one switching cycle, specifically, $m_{SR} = 50$ when integrating the SR driving scheme into TMS320F28027. To control a 100kHz LLC converter with a 60MHz MCU ($m_{total} = 600$), the adaptive SR driving takes around 8.3% CPU utilization. When using 8.3% CPU utilization for the SR driving, the digital controller still has enough resources for the closed-loop control and auxiliary functions. However, when this method is applied to high-frequency LLC converters, the CPU utilization for the SR driving would increase dramatically. For example, if the SR driving is applied to a 500kHz LLC converter with a 60MHz MCU ($m_{total} = 120$), it would take 42% CPU utilization, which means that most of the time, the CPU is occupied by SR driving and has little spare time for the closed-loop control and auxiliary functions.

Fig. 2.51. CPU utilization with the integrated adaptive SR driving scheme
2.5.2. **Adaptive SR driving for high-frequency LLC converters**

To achieve effective control performance for high-frequency LLC converters with the cost-effective digital controller, the control loop can be executed every several switching cycles. Specifically, to solve the challenge of the SR driving for high-frequency LLC converters, an adaptive SR driving scheme using a ripple counter is proposed. The control scheme is shown in Fig. 2.52. A ripple counter is added between the comparator and the digital controller, which can help the digital controller to tune the SR on-time every several switching cycles.

![Proposed integrated adaptive SR driving for high-frequency LLC converters](image)

Fig. 2.52. Proposed integrated adaptive SR driving for high-frequency LLC converters

By using the ripple counter, the proposed method can tune the SR on-time every \((N+1)^{th}\) switching cycle \((N = 1, 2, 3\ldots)\). The turn-on time of the SRs is still synchronized with the primary switches, so there is always a very small duration of body diode conduction at the turn-on moment. The proposed method counts the ripples at \(V_{\text{CMP}}\) to determine if there is extra body diode conduction after the SR turn-off in the following principles: the controller clears the ripple counter in the first switching cycle after SR turn-on; then the controller reads the ripple counter in the \((N+1)^{th}\) switching cycle after SR turn-on. If the output is ‘2n’, it means that there is the body diode
conduction after the SR turn-off. Otherwise, there is no body diode conduction. Fig. 2.53 is an example in which the SR on-time is tuned every 3\(^{\text{rd}}\) switching cycle.

(a) There is body diode conduction after SR turn-off

(b) No body diode conduction after SR turn-off

Fig. 2.53. Detecting body diode conduction every 3\(^{\text{rd}}\) switching cycle

An example of a tuning process for the proposed adaptive SR driving is shown in Fig. 2.54, in which the SR on-time is tuned every second switching cycle. At the beginning, there is a large body diode conduction after the SR turn-off, and the ripple counter indicates two ripples in the detection window. So the controller keeps increasing the SR on-time. Every two switching cycles, the SR on-time is increased by $\Delta T$, which continues until when the ripple counter indicates that there is only one ripple. Then the controller decreases the SR on-time by $\Delta T$. In the next two switching cycles, there are two ripples again. Thus, the SR on-time is tuned step-by-step to eliminate the body diode conduction, and finally it’s around the optimal point.
On the one hand, with the proposed adaptive SR driving method the CPU utilization for high-frequency LLC converters can be reduced effectively by reducing the SR on-time tuning speed with minimum auxiliary circuits and components. On the other hand, by eliminating the external interrupt in the MCU with the ripple counter, it takes less than 20 CPU cycles to execute the proposed adaptive SR driving every digital control cycle, meaning \( m_{SR} < 20 \) in this case. Reducing the control speed is quite a common practice when using low-cost digital controllers to control high-frequency converters. When tuning the SR on-time every \((N+1)^{th}\) switching cycle \((N = 1, 2, 3 \ldots)\), the total CPU cycles within one digital control cycle \(m_{total}\) becomes as follows:

\[
m_{total} = (N + 1) \cdot \frac{f_{\text{clock}}}{f_s}
\]  

(2.22)

Compared with the method in Fig. 2.49, the proposed method for high-frequency LLC converters can increase \(m_{total}\) by \(N+1\) times and reduce \(m_{SR}\) from 50 to 20. When applying the proposed SR driving scheme to a 500kHz LLC converter with a 60MHz MCU by tuning the SR on-time every third switching cycle \((m_{total} = 360)\), the CPU utilization for SR driving is reduced to less than 6%, compared to 42% CPU utilization with the method in Fig. 2.49 by tuning the SR
on-time every switching cycle. Furthermore, by reducing the SR on-time tuning speed, the SR driving control and the closed-loop control can be updated synchronously, and the SR on-time can be modified accordingly during fast transient response to guarantee safe operation.

Under fast load transient, $f_s$ may change very fast and the SR driving needs to be handled properly. When $f_s$ suddenly decreases under load step-up as shown in Fig. 2.55, the primary on-time increases from $T_1[k]$ to $T_1[k+1] + \Delta T_{UP}$, where the change from $T_1[k]$ to $T_1[k+1]$ is determined by linear regulator based on $V_o$ regulation and $\Delta T_{UP}$ is determined by SOTC calculation based on sensed load current. In such a case, if the SR on-time is also increased from $T_2[k]$ to $T_2[k+1] + \Delta T_{UP}$ as shown in Fig. 2.55(a), $i_{Lr}$ would cross $i_{Lm}$ as the shaded area and there would be a negative current going through SRs, inducing extra losses. The proper SR on-time $T_2$ after load step-up is shown in Fig. 2.55(b), which is determined by the tuning process, i.e. $T_2$ is increased by $\Delta T$ if there is body diode conduction in current switching cycle and decreased by $\Delta T$ if not, and expressed as below:

$$
T_2 = T_2[k + 1] = \begin{cases} 
T_2[k] + \Delta T, & \text{if } V_{CMP} = 1 \\
T_2[k] - \Delta T, & \text{if } V_{CMP} = 0
\end{cases}
$$

(a) SR on-time increases with primary on-time
When $f_S$ suddenly increases under load step-down as shown in Fig. 2.56, the primary on-time increases from $T_1[k]$ to $T_1[k+1] - \Delta T_D$, in which the change from $T_1[k]$ to $T_1[k+1]$ is also determined by linear regulator based on $V_o$ regulation and $\Delta T_D$ is determined by SOTC calculation based on load transient. In addition, the change of the SR on-time from $T_2[k]$ to $T_2[k+1]$ is determined by the tuning process and explained in equation (6). If there is no further modification and protection mechanism of SR on-time, there is a potential shoot-through condition as shown in Fig. 2.56(a), and the shoot-through conditions are highlighted in the shaded area. To prevent shoot-through, the SR on-time $T_2$ is modified accordingly as shown in Fig. 2.56(b), following the principle below:

$$
T_2 = \begin{cases} 
T_2[k+1] - \Delta T_D, & \text{if load step - down} \\
T_2[k+1], & \text{if load step - up}
\end{cases} 
$$

(a) SR on-time remains the same

Fig. 2.55. SR driving signal during load step-up
The proposed adaptive SR driving can be integrated with a multi-step SOTC by synchronizing the adaptive SR driving with the SOTC control, meaning that the SR on-time and primary $f_S$ are updated simultaneously. During load transient response, the SR on-time is modified accordingly. An example is shown in Fig. 2.57, in which the SR on-time and primary $f_S$ are updated every second switching cycle.

Based on the aforementioned techniques, the proposed adaptive SR driving can be integrated with closed-loop control for high-frequency LLC converters. For a given low-cost microcontroller, the digital
delay including closed-loop control and adaptive SR driving is evaluated, and then the PWM updating speed for the primary switches and SRs is chosen accordingly to accommodate the digital delay and maximize the response speed.

2.5.3. Experimental results

The tuning process of the proposed adaptive SR driving scheme on the 500kHz LLC converter is shown in Fig. 2.58. The initial SR on-time is relatively small, and the body diode conduction time is large. The proposed adaptive SR driving tunes the SR on-time step-by-step until finally the body diode conduction is around the minimum point.

![Fig. 2.58. Tuning process of proposed SR driving](image)

The proposed adaptive SR driving scheme under load step-up from 40A to 70A is shown in Fig. 2.59. It is shown that envelop of $i_{Lr}$ increases from light load condition to heavy load condition very fast with SOTC control; the SR body-diode conduction before the load transient is around the minimum, increases slightly during the transient, and converges to the minimum immediately after the transient.
The efficiency curve of the 500kHz LLC converter with and without the proposed adaptive SR driving scheme is shown in Fig. 2.60. The proposed adaptive SR driving can improve efficiency by around 0.3%.

SRs are important for high output current LLC converters in order to reduce the secondary conduction loss. Different SR driving schemes are investigated and their limitations and digital
implementation are discussed in detail. The adaptive SR driving is suitable to be integrated with a closed-loop control into a digital controller, but it will require a much higher-cost digital controllers when applied to high-frequency LLC converters. To solve this challenge, firstly, the adaptive SR driving based on the ripple detection is proposed to integrate the SR driving into a low-cost digital controller without auxiliary circuits; then it is proposed to extend this method to high-frequency LLC converters by adding a ripple counter. By tuning the SR on-time every several switching cycles, the proposed method can reduce the CPU utilization for SR driving effectively, and thus be implemented by the low-cost digital controllers.

A very important issue for adaptive SR driving is how to cooperate with the closed-loop control during fast transient response to guarantee that the SR driving signals are in safe conditions. This section discusses the proper response of SR driving when embedded into a closed-loop control during a fast transient response. By synchronizing the PWM update of an adaptive SR and the closed-loop control, guidelines on how to modify the SR on-time accordingly are provided in this section. The proposed method is verified on a 1kW 500kHz 400V/12V LLC converter with a 60MHz MCU and a ripple counter. Compared with the other SR driving schemes, the proposed method is suitable to be embedded into digital controller, while at the same time, minimizing the CPU utilization and extra components.

2.6. Conclusions

After integrating all the control functions, including closed-loop control, start-up and short-circuit protection, burst mode, and proposed SR driving, the utilization of MCU resources are shown in Fig. 2.61. The whole program takes around 3.5k ram space. The control loop is executed every third switching cycle and the maximum CPU utilization is around 90%, which happens
during start-up and burst mode. The controller only needs to sense $V_o$ and the load current. The ePWM1 module is used to drive the primary switches. The ePWM2 module is used for the start-of-conversion of the analog-to-digital converter (ADC) and the ePWM3/4 modules are used to drive the SRs. Four general-purpose input/outputs (GPIOs) are needed for the proposed adaptive SR driving control, two of which are used to clear the ripple counter and the other two are used to read the output of the ripple counter.

![Utilization of MCU resources](image)

**Fig. 2.61. Utilization of MCU resources**

By minimizing utilization of controller CPU and resources, the proposed SOTC control is able to control high-frequency LLC converters with a low-cost MCU. Fast transient response, low current and voltage stresses, and good light load efficiency are demonstrated. The proposed control provides a high-performance and low-cost solutions to solve the challenges in the control of high-frequency LLC converters.
Chapter 3. Matrix Transformers for High-output-current LLC converters

The design of isolated high output current DC/DC converters is very challenging due to the large conduction losses from SR devices and transformer windings, as well as the huge AC termination loss when connecting SRs and secondary windings. To reduce the primary AC winding loss, a hybrid transformer structure, including litz wires primary winding and PCB secondary winding, are employed; to reduce the secondary termination loss, the SRs and output capacitors are mounted on the same PCB layer of the secondary winding [53][54]. Although such a structure in [53][54] can help reduce conduction loss and termination loss, it is too complex for manufacturing and mass production. The matrix transformer can help increase the output current capability by distributing the secondary current with multiple cores [55][56]. The concept of flux cancelation is proposed to reduce core size and loss [57], but the transformer is implemented with a very expensive 12-layer PCB, which also has large distributed inter-winding capacitance and, hence, large CM noise current for high input voltage applications. One alternative solution over the 12-layer PCB is to use a simple four-layer PCB to implement a matrix transformer for a 380V/12V LLC converter and integrate SRs and output capacitors as part of the secondary winding in order to eliminate AC termination loss [36]. When using four-layer PCB windings, two shielding layers could be placed in between primary and secondary windings. Each shielding layer is connected to the primary ground. Therefore the CM noise current can only circulate in the primary side [39]. The 380V/12V LLC converter design is further optimized with a design optimization procedure, and a peak efficiency of around 97% is demonstrated [37]. But these
designs still have the problem of complex structure with multiple cores and there is room for efficiency improvement. Further efforts need to be spent on the design, optimization and magnetic integration of matrix transformer in order to improve both efficiency and power density.

For applications that require low-voltage and high-current outputs, such as computer servers, there are several important design considerations for the LLC converter: (1) The SR devices have limited current capability due to packaging and thermal constrain. For server applications, one should consider paralleling 4-8 SRs to reduce conduction loss as illustrated in Fig. 3.1(a). Both static and dynamic current sharing, when paralleling a large number of SRs, are difficult to achieve. (2) The large sum of high frequency and high di/dt AC currents must flow through common termination points between the transformer and the SRs, which is marked using red dots in Fig. 3.1(a). This will result in large termination losses. (3) It is difficult to place the large number of SRs close to the termination, which will result in large leakage inductances at the transformer’s secondary windings, as well as large winding losses. Such LLC converter design, even though it has a lower core loss, will suffer large winding losses and termination loss. On the other hand, the transformer in commercial power supplies normally uses litz wires as the primary winding and copper foils as the secondary winding. This is very bulky, labor-intensive and expensive.

3.1. Planar matrix transformer with PCB winding

A planar transformer with PCB winding can be adopted to achieve automatic manufacturing and high power density. The matrix transformer, which is defined as an array of elemental transformers inter-wired to form a single transformer, can be employed to evenly distribute the large secondary current to different SRs [55]. An LLC converter with a matrix transformer is shown in Fig. 3.1(b). The traditional single core structure was divided into a four-core structure,
with the primary windings in series and the secondary windings in parallel. Since the primary current for the four elemental transformers is the same due to a series connection, the secondary current is perfectly balanced.

(a) With conventional transformer. \hspace{1cm} (b) With matrix transformer.

Fig. 3.1. LLC converters with different transformers structure

The matrix transformer in Fig. 3.1(b) can be formed by using four sets of identical UI-cores. The primary winding winds one pillar of each core as shown in Fig. 3.2(a), where only the primary winding layer is shown for simplicity. The matrix transformer in Fig. 3.2(a) has an increased core loss with 4 sets of UI-cores compared to the transformer in Fig. 3.1(a) with only one ER-core. To reduce the core size, as well as core loss in Fig. 3.2(a), the primary winding can be modified as shown in Fig. 3.2 (b) to achieve flux cancellation.

(a) Original matrix transformer. \hspace{1cm} (b) Matrix transformer with flux cancellation.

Fig. 3.2. Primary winding pattern for matrix transformer.
The termination points are very critical for efficiency. With a 12-layer PCB as the transformer windings, vias have to be used to connect the secondary winding and the SRs, which would cause extra losses since all the AC current would go through these vias. It is proposed in [36] to integrate the SRs and output capacitors into the secondary winding as shown in Fig. 3.3(a) and employ a simple four-layer PCB winding as shown in Fig. 3.3(b), where the top and bottom layers are two sets of secondary windings for center-tap structure and the middle two layers are the primary windings. With this approach, the termination points, where all currents are summed, occur on the DC side, thus, there would be no AC termination loss. Transformer winding losses are significantly reduced as are the leakage inductances.

(a) Top view.  
(b) Cross-sectional view.

Fig. 3.3. Four-layer PCB winding transformer with integrated SRs and output capacitors.

A design optimization procedure is then provided in [37], and the number of cores is doubled as well as the number of SRs to reduce the winding losses and SRs’ conduction loss. References [36][37] provide two designs of 1kW 380V/12V LLC converters with matrix transformer operating at 1MHz, whose efficiency curves are shown in Fig. 3.4. From the design in [36] to the design in [37], the peak efficiency is improved from 95.5% to 97.1%, with the same power density of around 700W/in$^3$. 

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Despite all the efforts, the LLC converters with matrix transformer still have some challenges to overcome and require further efficiency improvement. To achieve a high output current, multiple cores are still used even with flux cancellation, which is complex for the manufacturing. Further magnetic integration is indispensable to overcome this challenge. Furthermore, to replace the present DC/DC converters operating at 50-100 kHz, further efficiency improvement for the high frequency DC/DC converters is required. The following sections will present a detailed design methodology and a novel matrix transformer structure to overcome the design challenge.

3.1.1. Proposed optimal design methodology

To improve the design of planar matrix transformer, a transformer loss model and design methodology are proposed in this section. According to Table 1.1, the DC/DC converter should step down 380V directly to 12V with 62.5A output and comply with quarter-brick form factor. To leave some margin, 67A output current is selected, which is equivalent to around 800W at 12V output, as the full-load condition to optimize the transformer design. To handle such large output current, four sets of outputs, meaning four elemental transformers, are selected for one LLC converter in the following analysis. Since the total primary to secondary transformer turn ratio is

Fig. 3.4. Efficiency improvement of LLC converter with matrix transformer.
16:1:1 for half-bridge primary configuration, each elemental transformer has a turn ratio of 4:1:1. By using four-layer PCB winding structure, in each elemental transformer, the primary winding has two PCB layers and each layer has two turns.

To make a fair comparison with the previous design practices [36][37], 1MHz is chosen as the switching frequency to illustrate the proposed design methodology and considerations in the high-frequency matrix transformer design for LLC converter in this section. For different design considerations, the switching frequency could be change accordingly to make a better tradeoff between power density and efficiency. It is proposed to use a round core pillar for each elemental transformer to further reduce the winding losses instead of a rectangular core pillar. A comparison of current distribution in the secondary winding between rectangular core pillar and round core pillar is shown in Fig. 3.5. Both cases have the same effective area $Ae$ of 44mm$^2$ and footprint of 325mm$^2$. The length of the current path for secondary winding with rectangular core pillar is around 46mm considering the curvature effect caused the four round edges [37], and that with round core pillar is 41mm. So the winding loss can be reduced effectively by using the round core pillars.

(a) With rectangular core pillar. (b) With round core pillar.

Fig. 3.5. Comparison of current distribution in secondary winding.
To develop an optimal design methodology for planar matrix transformer, the winding loss for round core pillar is calculated as follows: the primary and secondary windings could be simplified as shown in Fig. 3.6 to develop the winding loss model. Since there is almost no current distribution at the four edges of the winding due to the high switching frequency, the four edges of the winding are ignored.

![Fig. 3.6. Model for calculating winding resistance.](image)

The analytical expressions of the secondary DC winding resistance winding $R_{Sec,DC}$, and the primary DC winding resistance for inner turn $R_{1,DC}$, outer turn $R_{2,DC}$ and two turns in total $R_{Pri,DC}$ are expressed a follows:

\[
R_{Sec,DC} = \frac{\rho \cdot 2\pi}{h} \cdot \frac{1}{\ln R - \ln r} \tag{3.1}
\]

\[
R_{1,DC}(x) = \frac{\rho \cdot 2\pi}{h} \cdot \frac{1}{\ln x - \ln r} \tag{3.2}
\]

\[
R_{2,DC}(x) = \frac{\rho \cdot 2\pi}{h} \cdot \frac{1}{\ln R - \ln x} \tag{3.3}
\]

\[
R_{Pri,DC}(x) = R_{1}(x) + R_{2}(x) \tag{3.4}
\]

In conventional transformer design with litz wires as the primary winding, the winding width of each turn is the same since it is not practical to use different litz wires for each turn. However, equal winding width for each turn is not actually the optimal design for a planar transformer and...
it is very easy to change the winding width without any extra cost when using the PCB winding. To select the proper winding width for the inner turn and outer turn of the primary winding, let:

\[ \frac{d}{dx} R_{pri,DC}(x) = 0 \quad (3.5) \]

Solve the equation above and get:

\[ x = \sqrt{R \cdot r} \quad (3.6) \]

If the result in equation (6) is taken back into equation (2) and (3), it is found that the total winding resistance is minimum when the resistances for the inner and outer turn are the same. This conclusion is also true for n-turn conditions, which can be derived through mathematical induction. Under the optimal winding width condition, the total \( R_{pri,DC} \) for the case with n turns in one layer is expressed as follows:

\[ R_{pri,DC} = \frac{\rho \cdot 2\pi \cdot n^2}{h \cdot ln R - ln r} \quad (3.7) \]

The ratio \( \eta_{opt} \) of winding resistance with optimal width over that with even width is plotted in Fig. 3.7. For the design in this section, the turn number per layer is 2, and the ratio of \( R/r \) is around 2.5, which would result in around 5% winding loss reduction with the optimal winding width.

\[ \eta_{opt} \]

\[ \text{Turns number per layer} \]

Fig. 3.7. Winding resistance reduction with optimal winding width.
With the expression of DC winding resistance, the AC resistance could be easily derived using the eddy current model in [58], in which the AC resistance coefficient $F_R$ is described as:

$$F_R = M' + \frac{(m^2-1)}{3} D'$$  \hspace{1cm} (3.8)

Where $M'$ and $D'$ are the real parts of $M$ and $D$, respectively; and $M = \alpha h \coth(\alpha h)$, $D = 2\alpha h \tanh(\alpha h/2)$, $\alpha = \sqrt{j\omega \mu_0 \eta/\rho}$, $\eta = N_l a/b$. $m$ is number of layers in a winding porting; $\omega$ is angular frequency; $h$ is winding copper thickness; $N_l$ is number of turns per layer; $a$ is total winding area width; and $b$ is winding width for each turn. With the AC winding resistance coefficient, the AC resistance for secondary winding and primary winding with the interleaving structure show in Fig. 3.3 for one elemental transformer, are expressed as follows:

$$R_{Sec,AC} = F_{R,Sec} \cdot R_{Sec,DC} = (F_{R,Sec} \cdot \frac{\rho \cdot 2\pi}{h}) \cdot \frac{1}{\ln R - \ln r}$$  \hspace{1cm} (3.9)

$$R_{Pri,AC} = F_{R,Pri} \cdot R_{Pri,DC} = (F_{R,Pri} \cdot \frac{\rho \cdot 2\pi}{h}) \cdot \frac{2^4}{\ln R - \ln r}$$  \hspace{1cm} (3.10)

Since in this case, the window area is fully utilized, meaning $\eta \approx 1$. The terms in the parentheses of equations above is only dependent on switching frequency, copper thickness $h$ and interleaving structure. The terms are defined as follows, and plotted in Fig. 3.8 for a switching frequency of 1MHz, which shows that the optimal copper thickness for primary is 2oz, and that for secondary is 3oz.

$$H_{Sec}(h) = F_{R,Sec} \cdot \frac{\rho \cdot 2\pi}{h}$$  \hspace{1cm} (3.11)

$$H_{Pri}(h) = F_{R,Pri} \cdot \frac{\rho \cdot 2\pi}{h}$$  \hspace{1cm} (3.12)
Different magnetic materials suitable for this application are tested and core loss measurement results under 1MHz excitation are shown in Fig. 3.9. Among them, ML91 is selected for the following analysis since it has the lowest core loss. The core loss $P_{\text{Core}}$ can be calculated based on core loss density $P_V$ and core volume $V_{\text{Core}}$ using:

$$P_{\text{Core}} = P_V \cdot V_{\text{Core}}$$  \hspace{1cm} (3.13)

Based on the aforementioned winding loss model and core loss model, the transformer total loss versus core radius $r$ as x-axis and secondary winding width $c$ as y-axis could be plotted as shown in Fig. 3.10 with four elemental transformers and under full-load condition. In Fig. 3.10,
the numbers in the colored solid lines are the total transformer loss; the black dash line represents all the combinations of \( r \) and \( c \) for given footprint; the tangential points (marked using red dots) between the black dash lines and colored solid lines are the optimal design points for the given footprint.

![Diagram of transformer total loss vs. core radius and winding width](image)

Fig. 3.10. Transformer total loss vs. core radius \( r \) and winding width \( c \) for round core pillar.

To make a comparison with rectangular core pillars, the transformer total loss versus dimension variable \( a \) as x-axis and secondary winding width \( c \) as y-axis could be plotted as shown in Fig. 3.11 with four elemental transformers and under full-load condition. Since elemental transformer with rectangular core pillar has three dimension variables, including \( a, c \) and \( Ae \); core loss density is fixed to 600kW/m\(^3\), so \( Ae \) is also fixed, to derive Fig. 3.11. In Fig. 3.11, the numbers in the colored solid lines are the total transformer loss; the black dash line represents all the combinations of \( a \) and \( c \) for given footprint; the tangential points (marked using red dots) between the black dash lines and colored solid lines are the optimal design points for the given footprint. Different core loss density value are swept later to get the optimal design point for different core density.
When all the optimal design points are swept for a given footprint range, the minimum transformer loss versus the footprint for a matrix transformer with round core pillars and rectangular core pillars is plotted in Fig. 3.12, which shows that although the two cases have similar core losses, the matrix transformer with round core pillars has more reduced winding losses. To fit into a quarter-brick form factor, 1150mm$^2$ footprint is selected for the transformer, which means around 1.7W loss reduction with the round core pillars.
3.1.2. Proposed matrix transformer structure

To overcome the challenge of multiple cores and further improve efficiency, two matrix transformer structures, both of which can integrate four elemental transformers into one magnetic core, are proposed as follows, and comparison between them has been made.

The original matrix transformer with flux cancellation is shown in Fig. 3.13. Four elemental transformers are integrated into two magnetic cores. Only the primary winding layer is shown for simplicity. Magnetic Core 1 has two pillars numbered as 1 and 2, and magnetic Core 2 has another two pillars numbered as 3 and 4. There is a flux of $\Phi_B$ from Pillar 1 to Pillar 2, and another flux of $\Phi_B$ from Pillar 3 to Pillar 4.

![Diagram of original matrix transformer with flux cancellation](image)

Fig. 3.13. The original matrix transformer with flux cancellation.

The proposed matrix transformer Structure 1 is derived as follows: Core 2 in Fig. 3.13 is moved just below Core 1 as shown in Fig. 3.14(a); now there are still two magnetic cores in Fig. 3.14(a); then the magnetic plates for the two cores are replaced by the integrated plates as shown in Fig. 3.14(b) to integrate the two magnetic components into one. With the proposed Structure 1, although the flux pattern and core loss remains the same as the original two-core structure, the challenge of multiple cores in previous designs has been overcome.
The proposed matrix transformer Structure 2 with reduced flux density is derived as follows: Core 2 in Fig. 3.13 is moved just below Core 1, and then rotated by 180° as shown in Fig. 3.15(a); now there are still two magnetic cores in Fig. 3.15(a) and the flux pattern remains the same as the that in Fig. 3.13; then the magnetic plates for the two cores are replaced by the integrated plates as shown in Fig. 3.15(b) to integrate the two magnetic components into one. With the proposed Structure 2, although the flux within the pillars remains the same, the flux density in the magnetic plates is reduced by half. This is very beneficial for high frequency ferrite materials since the core loss is a considerable portion in the total loss and is mainly determined by the flux density. Take ML91 as an example, the core loss is approximately proportional to the cubic of the flux density according to the measurement results shown in Fig. 3.9.
The flux distribution of two proposed matrix transformer structures are compared by simulation as shown in Fig. 3.16. Two structures have identical geometry for the magnetic core, but different winding arrangements as described in Fig. 3.14 and Fig. 3.15. Since the proposed Structure 2 has a more evenly distributed flux, the core loss is reduced by around 40% compared to Structure 1 according to the simulation results.
Both of the 2 proposed matrix transformer structures consist of four identical elemental transformers, so their winding losses are close. However, the proposed Structure 2 has a significantly reduced core loss due to a better arrangement of the four elemental transformers. Furthermore, since the four elemental transformers are coupled in the proposed Structure 2, it is more robust to the tolerance between the four elemental transformers. Overall, Structure 2 is considered superior to Structure 1 due to lower core loss and more robustness. Fig. 3.17 is the schematics of LLC converter with proposed matrix transformer.

Fig. 3.17. Schematics of LLC converter with proposed matrix transformer

The detailed winding arrangement for the proposed matrix transformer Structure 2 is illustrated in Fig. 3.18, where the yellow arrows indicate current direction in the positive current cycle. The top layer (Layer 1) and bottom layer (Layer 4) are the secondary windings. SRs and output capacitors are integrated into the secondary windings to eliminate AC termination loss. No vias are needed to connect the secondary PCB layers due to the simple four-layer PCB winding implementation. The middle two layers (Layer 2 and Layer 3) are the primary windings. Although the primary windings are connected through vias, the vias related loss is relatively small since the primary current is small. Another benefit of this winding structure is that the two primary terminals, as shown in Fig. 3.18(b), are very close to each other, which means there is negligible leakage
inductance and termination loss related to the primary terminals. Although the proposed design employs buried vias, the overall PCB cost is still lower than the 12-layer PCB implementation in [57], and inter-winding capacitance has been reduced a lot with four-layer PCB winding.

![Diagram of winding arrangement for the proposed matrix transformer Structure 2.](image)

(a) Layer 1 for secondary. (b) Layer 2 for primary. (c) Layer 3 for primary. (d) Layer 4 for secondary.

Fig. 3.18. Winding arrangement for the proposed matrix transformer Structure 2.

The proposed Structure 2 can be improved to further reduce the core loss without sacrificing power density. Fig. 3.19(a) shows the 3D view of the original Structure 2, including the flux distribution on the surface of the integrated magnetic core. Since the SRs and output capacitors are on the two edges of the PCB windings and there are no components on the other two edges; the top and bottom magnetic plates can be expanded to the other two edges of the PCB windings as
shown in Fig. 3.19(b). By doing this, the flux density in the magnetic plates can be further reduced, so is the core loss. The improved Structure 2 has the same dimension and power density as that of the original one, but the core loss is further reduced by around 30% according to the simulation results.

![Diagram](image1)

(a) Before improvement.  
(b) After improvement.

Fig. 3.19. Improvement of proposed Structure 2 to further reduce core loss.

There are four sets of SRs with the proposed matrix transformer structure. Three candidate 30V SR devices are compared by plotting the total SR loss, including driving loss and conduction loss, versus output power in Fig. 3.20 under ideal gate driving signals. The loss of EPC2023 and BSC0500NSI are close, while the later one is preferred due to the following reasons: the reverse drain-source conduction characteristics of BSC0500NSI with inherent body-diode is much better than EPC2023, which has no body-diode; the drain-source on-state resistance $R_{ds(on)}$ of BSC0500NSI has smaller variation under different junction temperature, for example, 30% $R_{ds(on)}$ increase for BSC0500NSI compared to 50% $R_{ds(on)}$ increase for EPC2023, both under the condition of junction temperature rising from 25°C to 100°C; BSC0500NSI has larger drain pads with SuperSO8 package, as well as better thermal characteristics [59][60].
Based on the proposed design methodology and matrix transformer structure, the LLC converter is designed and the specifications are shown in Table 3.1. The leakage inductance of the matrix transformer is used as the resonant inductance, which is 312nH. The resonant capacitor is selected accordingly as 71nF to make the resonant frequency 1MHz. The magnetizing inductance and dead time are optimized according to the optimal design methodology in [10]. In this design, the air gap is around 0.2mm to achieve a magnetizing inductance of 25uH. The distance between the winding and the air gap is 2.5 times of the air gap thickness. So the fringing effect caused by the air gap is negligible in this case.

**Table 3.1. Specifications of the Proposed LLC Converter**

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant Frequency</td>
<td>1MHz</td>
</tr>
<tr>
<td>Dead Time</td>
<td>90ns</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>16:1</td>
</tr>
<tr>
<td>Primary devices</td>
<td>PGA26E08</td>
</tr>
<tr>
<td>Secondary devices</td>
<td>BSC0500NSI</td>
</tr>
<tr>
<td>Primary Driver</td>
<td>Si8273</td>
</tr>
<tr>
<td>Secondary Drivers</td>
<td>FAN3122</td>
</tr>
<tr>
<td>Resonant Capacitor</td>
<td>71nF</td>
</tr>
<tr>
<td>Resonant Inductance</td>
<td>312nH</td>
</tr>
<tr>
<td>Magnetizing Inductance</td>
<td>25uH</td>
</tr>
</tbody>
</table>
The converter works as a DC transformer with a fixed switching frequency at the resonant frequency, which helps maximize the efficiency and simplify the control. The experimental results are presented below.

3.1.3. Experimental results

The 1MHz 800W 380V/12V LLC converter prototype with the proposed matrix transformer is shown in Fig. 3.21. It has the same footprint as a quarter-brick, but a much smaller height of 0.27inch, compared to the height of 0.50inch for quarter-brick. An output power of 800W at such a dimension is equivalent to a power density of around 900W/inch³.

![Magnetic components](image1.png)

(a) Magnetic components.

![Prototype Without top plate](image2.png)

(b) Prototype Without top plate.

![Fully-assembled prototype](image3.png)

(c) Fully-assembled prototype.

Fig. 3.21. 1MHz 800W 380V/12V LLC converter prototype.

The experimental waveforms under full-load and light load (10% load) conditions are shown in Fig. 3.22. Here, it shows that ZVS for both the primary and secondary switches under both full-load and light-load conditions can be achieved. The experimental waveforms of the drain-source voltage for SRs $V_{ds,SR}$ of four elemental transformers are shown in Fig. 3.23. The $V_{ds,SR}$ waveforms for four SRs are quite symmetrical and overlap each other very well, which means that there is
almost no tolerance for the four elemental transformers. Moreover, there is no ringing in the $V_{ds_{SR}}$ due to the minimum secondary leakage.

![Experimental waveforms of $V_{ds_{SR}}$ for 4 elemental transformers.](image)

(a) Full-load. (b) Light-load (10% load).

Fig. 3.22. Experimental waveforms.

![Experimental waveforms of $V_{ds_{SR}}$ for 4 elemental transformers.](image)

Fig. 3.23. Experimental waveforms of $V_{ds_{SR}}$ for 4 elemental transformers.

The measured efficiency curve of the proposed LLC converter is shown in Fig. 3.24. The efficiency curves of the two designs in [36][37] and requirement of iNEMI are also listed as a comparison. The proposed LLC converter has a peak efficiency of 97.6%, a full-load efficiency of 97.2% and a light-load (10% load) efficiency of 93.0%. The efficiency of the proposed LLC converter is much higher than the requirement of iNEMI and state-of-the-art high-frequency LLC converters. Fig. 3.25 provides the thermal test results of the proposed LLC converter under full-load condition, 25°C ambient temperature and 200 LFM (Linear Feet per Minute) fan speed. The
highest temperature is 71.2°C and occurs on the primary devices. Both the primary and secondary devices operate within the safe temperature range. The proposed design has good thermal performance due to the high-efficiency design and a higher surface area to volume ratio by using planar magnetic cores compared to the conventional magnetic cores. The planar magnetics are more efficient to conduct heat and lead to low temperature rises compared with conventional wire-wound components [61].

![Graph showing efficiency vs output power]

**Fig. 3.24.** Measured efficiency.

(a) Test setup.  
(b) Thermal image.

**Fig. 3.25.** Thermal test.

To compare the proposed design with the two designs in [36][37], loss breakdown under full-load condition is analyzed as shown in Fig. 3.26. The improvement of the proposed LLC converter
is analyzed as follows: the loss reduction in the primary devices is mainly achieved with the improvement of the GaN devices; the core loss reduction in the transformer is significant with the proposed matrix transformer; the winding losses are reduced with the improved PCB winding arrangement and the proposed optimal design methodology; better tradeoff between conduction loss and driving loss of the SRs has been made.

![Loss breakdown comparison](image)

**Fig. 3.26.** Loss breakdown comparison.

Compared to the previous high-frequency LLC converter designs, the proposed design in this section can achieve the highest efficiency and power density, with an additional benefit of all elemental transformers integrated into one magnetic core. Although the proposed design uses 1MHz as the switching frequency, it could be further increased to make a better tradeoff between efficiency and power density. The currently available ferrite material (ML91) is good for 1MHz to 3MHz, and the 600V GaN devices and 30V Si devices can both operate at above 1MHz. However, it is worth noting that maintaining a safe case temperature is important if a higher switching frequency is chosen, which can be achieved with a higher efficiency by using more layers of PCB winding or a better heat dissipation condition.
3.1.4. Conclusions

The matrix transformers for high output current LLC converter are investigated. To improve the current design practice, a high-frequency transformer loss model is developed and a detailed design methodology is proposed. To overcome the challenge of multiple cores, a novel matrix transformer structure is proposed to integrate four elemental transformers into one magnetic core and utilized a simple four-layer PCB as the windings. The proposed design can utilize flux cancellation and reduce flux density in the magnetic plates to reduce core loss; and integrate SRs and output capacitors into the secondary winding to minimize leakage and termination loss. The core loss with the proposed matrix transformer is reduced by more than half compared to the state-of-art matrix transformer technique. The proposed matrix transformer is superior to the state-of-the-art due to the much reduced core loss, simple four-layer PCB windings and integrated magnetic structure.

By pushing switching frequency up to MHz with GaN devices, the proposed matrix transformer can demonstrate the impact of GaN in such important issues as efficiency, power density and manufacturability. With the academic contribution provided in this section, we can design a converter with 10 times, or even 20 times in switching frequency, comparing to the current practice using silicon devices. Finally, a 1MHz 380V/12V 800W LLC converter with GaN devices using the proposed matrix transformer structure is demonstrated. The prototype fits in quarter-brick footprint and achieves a peak efficiency of 97.6% and a power density of 900W/inch$^3$.

3.2. A novel shielding techniques

The aforementioned LLC converter design with a PCB winding matrix transformer demonstrates a peak efficiency of 97.6% and a power density of 900W/inch$^3$ with 1MHz switching
frequency, in which high efficiency and high power density are achieved with a simple 4-layer PCB winding. Such a design with the ability to be automatically manufactured is superior to the conventional LLC converter designs with its bulky, hand-made transformer. But the matrix transformer has fully interleaved PCB windings which lead to large distributed inter-winding capacitors and, hence, a large CM noise current. Passive cancellation approaches or balance techniques can be employed to reduce the CM noise, but they require additional passive components and the tolerance in the components and circuit highly impacts the cancellation or balancing effect, meaning that in mass production, the CM noise reduction effect is limited. The shielding technique is considered an effective method to suppress CM noise for the planar transformers and has been successfully demonstrated in [38][39]. Specifically for a 4-layer PCB winding matrix transformer, shielding could be achieved by simply placing two shielding layers in between primary and secondary windings. Fig. 3.27 illustrates the matrix transformer structure with shielding. Each shielding layer is connected to the primary ground. Therefore the CM noise current can only circulate in the primary side. The shielding layers are made identical to the secondary windings, both are single-turn windings. Therefore, there is zero potential difference between the shielding winding and the secondary winding, thus, causing no CM current. To predict the CM noise for the matrix transformers, the inter-winding capacitance and CM noise model are developed below.
3.2.1. Analysis of interwinding capacitance and CM noise

For low-voltage, high-current output applications, the LLC converter will employ a half-bridge primary and center-tapped secondary as shown in Fig. 3.28(a), in which there are four voltage pulsation nodes with a high $dv/dt$, including: the half-bridge switching node voltage $V_{SW}$, voltage applied to transformer primary winding $V_{Pri}$, drain-source voltages of two SRs $V_{SR1}$ and $V_{SR2}$. In this case, the leakage inductance of the transformer is utilized as the resonant inductance, otherwise, $V_{Pri}$ would be connected to the right terminal of the resonant inductor $Lr$. The CM noise coupling path can be simplified as shown in Fig. 3.28(b). $C_{PS}$ is the inter-winding capacitance between the primary and secondary windings, which is very large for planar transformers with PCB windings due to the large winding area and limited distance between primary and secondary windings. $C_{AG}$ is the parasitic capacitance between the half-bridge switching node and the primary ground, which is normally much smaller than $C_{PS}$, and it is very hard to measure the exact value of its capacitance. $V_{SR1}$ and $V_{SR2}$ are complementary with the same magnitude and 180° phase difference, meaning that the CM noises generated by these two $dv/dt$ nodes cancel each other. So there is no CM noise...
generated from the secondary side. To sum up, $C_{PS}$ dominates the coupling path for the CM noise, and the CM noise spectrum can be predicted by analyzing the CM noise current through $C_{PS}$.

![Schematics.](image1)

![CM noise sources and coupling paths.](image2)

Fig. 3.28. Simplified CM noise model for LLC converter.

To develop the CM noise model for the matrix transformers, the model for a single transformer is first developed as shown in Fig. 3.29. In the distributed model as shown in Fig. 3.29(a), in which the voltage of the two nodes for primary winding are defined as $V_A$ and $V_B$; the secondary winding has two complementary voltage nodes with $V_C$ and $-V_C$. Since the net CM noise current generated from the secondary side is zero due to two complementary voltage excitation, the lumped CM noise model can be described as shown in Fig. 3.29(b).

![Distributed model.](image3)

![Lumped model.](image4)

Fig. 3.29. CM noise current model for a single transformer.

For high output current applications, since the core cross-section areas are small and winding width is large in order to reduce the winding losses, it can be assumed that the primary winding is approximately spiral and uniformly distributed. To derive the analytic expression of $C_{lump}$ from the
distributed model in Fig. 3.29(a), it is defined that primary winding has a length of \( L \), the CM noise current \( \Delta i_{CM}(x) \) through the primary winding at position \( x \) with a length of \( \Delta x \) is expressed in (3.14). By integrating all the CM noise along the primary winding, the total CM current \( i_{CM} \) can be derived with (3.15).

\[
\Delta i_{CM}(x) = \Delta C(x) \cdot V'(x) = \frac{C_{PS}}{L} \cdot \Delta x \cdot \left( V_B' + \frac{V_A' - V_B'}{L} \cdot x \right) \quad (3.14)
\]

\[
i_{CM} = \sum \Delta i_{CM}(x) = \int_0^L \frac{C_{PS}}{L} \cdot \left( V_B' + \frac{V_A' - V_B'}{L} \cdot x \right) \cdot dx = C_{PS} \cdot \frac{V_A' + V_B'}{2} \quad (3.15)
\]

The distributed model in Fig. 3.29(a) can be lumped as shown in Fig. 3.29(b), then the CM current can be expressed by (3.16). By equating (3.15) and (3.16), \( C_{lump} \) can be expressed by (3.17).

\[
i_{CM} = C_{lump} \cdot V_A' \quad (3.16)
\]

\[
C_{lump} = \frac{1}{2} C_{PS} \cdot \left( 1 + \frac{V_B'}{V_A'} \right) \quad (3.17)
\]

The aforementioned matrix transformer in consists of 4 elemental transformers, and each elemental transformer has a different pulsation voltage at the nodes of the primary winding as shown in Fig. 3.30(a). With (3.17), the lumped inter-winding capacitance for each elemental transformer can be derived, then the lumped matrix transformer model is shown in Fig. 3.30(b). The total CM current \( i_{CM,T} \) is the sum of all the CM current through each elemental transformer, as expressed in (3.18).

\[
i_{CM,T} = \frac{C_{PS} V_{Prt}'}{2} + \frac{3C_{PS} V_{Prt}'}{4} + \frac{5C_{PS} V_{Prt}'}{6} + \frac{7C_{PS} V_{Prt}'}{8} = 2C_{PS} \cdot V_{Prt}' \quad (3.18)
\]
For the LLC converter, the magnetizing current is employed to achieve ZVS. Since the magnetizing inductance is very large, the magnetizing current can be considered a constant current source during the dead time. Thus, a constant current source is charging and discharging the junction capacitance of the two primary MOSFETs. The waveforms of \( V_{Pri} \) and \( i_{CM,T} \) are shown in Fig. 3.31. It should be noted that the \( dv/dt \) of \( V_{Pri} \) is assumed to be approximately constant during the dead time since the parallel of two junction capacitances is modeled as linear capacitances. The magnitude of the CM current \( i_{CM\_mag} \) during dead time is expressed in (3.19). By applying Fourier transform, the total CM current \( i_{CM\_T} \) is expressed in (3.20). Then the EMI spectrum can be calculated from the noise voltages picked up by LISN as expressed in (3.21).

\[
i_{CM\_mag} = 2C_{PS} \cdot \frac{V_{IN}}{T_{dead}} \tag{3.19}
\]

\[
i_{CM\_T}(t) = i_{CM\_mag} \cdot 4T_{dead} \sum_{n=1,3,5...}^{\infty} \frac{\sin(n \cdot \pi \cdot \frac{T_{dead}}{T_S})}{n \cdot \pi \cdot \frac{T_{dead}}{T_S}} \sin \left( \frac{2n \cdot \pi}{T_S} t \right) \tag{3.20}
\]

\[
V_{CM\_T}(t) = i_{CM\_T}(t) \cdot R_{LSIN} \tag{3.21}
\]
To verify the derived CM noise model, the predicted and measured CM noise spectra of the aforementioned design are plotted in Fig. 3.32. It can be observed that the derived model matches the experimental results up to 7MHz, with some discrepancies caused by other CM noise coupling paths not included in the model. Although at high frequency range, the model does not fit the experimental result very well, it does not impact the EMI filter design since the magnitude at fundamental frequency determines the corner frequency of the filter. To obtain a more accurate result for a higher frequency range, parasitic inductances, the nonlinear characteristics of MOSFET junction capacitances and other factors, should be considered in the model. On the other hand, it is worth noting that for LLC converters, the voltage pulsation is caused by the magnetizing current, which is load-independent, so the spectrum under a full-load condition is good enough to represent the worst case.
With the aforementioned CM noise model, the noise spectra of the LLC converters with a PCB winding matrix transformer can be predicted. Due to the large inter-winding capacitance, such a design normally cannot meet the requirement of EMI standards. Additional efforts are required to suppress the CM noise, but the traditional methods either require additional components, have complex structure or decrease efficiency for the whole load range. To solve these challenges, a novel shielding technique is proposed below.

### 3.2.2. Proposed shielding technique

The shielding technique in [39] is achieved by simply placing two shielding layers in between primary and secondary windings. In a fully interleaved transformer, the space between the primary and secondary winding has the highest magnetomotive force (MMF); when placing the PCB layers as shielding into this space, there would be an eddy current induced in the shielding layers. Decreasing the thickness of the shielding layers can limit the eddy current loss, however, due to the cost concern, the thinnest copper thickness is 0.5oz for standard PCB manufacturing. It has been demonstrated that using 0.5oz copper thickness as shielding layers can achieve 20dB CM noise attenuation, but at cost of 0.2% efficiency decrease [39].

In order to get the benefit of CM noise attenuation without simultaneously sacrificing the efficiency, this section proposes to utilize half of the shielding as the primary windings as shown in Fig. 3.33. It is defined that the voltage excitation applied to the primary windings is $V_{Pri}$, then the floating nodes of Shielding #2, #4, #6, #8 have a voltage potential of $+V_{Sh} = V_{Pri}/16$, while the floating nodes of Shielding #1, #3, #5, #7 have a voltage potential of $-V_{Sh}$. By connecting all the floating nodes of Shielding #2, #4, #6, #8 to a common node $S$, which is marked as green dot in Fig. 3.33, a parallel connection of these shielding serves as one additional turn for the primary winding. Doing this does not impact the function of shielding, since the voltage potential on the
shielding in Fig. 3.33 remains the same as the secondary windings. So there is zero potential difference between the shielding winding and the secondary winding, thus, no CM current. Although the voltage potential on the primary winding is increased by $+V_{sh}$, the CM noise current induced by the primary windings still circulates in the primary side since the shielding is connected to the primary ground.

![Fig. 3.33. Schematics of matrix transformer with the proposed shielding.](image)

When utilizing half of the shielding as one additional turn for the primary winding, the equivalent primary to secondary turn ratio is changed from 16:1 to 17:1. By doing so, the primary current is reduced by 5.9% for a given output voltage and current, which can help reduce the primary MOSFET conduction loss by 11%. The reduction of winding losses needs to be verified by the finite element analysis (FEA). In server applications, the turn ratio for most transformer designs of the LLC converter is between 16:1 and 18:1 \[54][62][63]. When using a matrix transformer consisting of 4 elemental transformers, the turn ratio must be 16:1 since it can only be an integer multiplied by 4. But with the proposal shielding, the turn ratio can be 17:1 by using the shielding as an additional turn.
The PCB winding implementation of the proposed shielding is shown in Fig. 3.34. The ground connection and voltage pulsation for the secondary windings are also included. The shielding is made identical to the secondary windings. To achieve the proposed shielding structure, the windings for the shielding have to be connected through additional PCB traces around the output terminals to the primary ground and node S, which would increase the footprint, cause interference between the primary windings and output terminals, and thus increase CM noise.

(a) Layer 1 for secondary.  
(b) Layer 2 for shielding.

To solve this problem, the shielding layout can be rotated by 270˚ as shown in Fig. 3.35, while still achieving the same effect. The top of Fig. 3.35 shows the shielding at Layer 5 and the secondary winding at Layer 6 for elemental transformer #1. Two terminals of secondary windings

Fig. 3.34. PCB winding implementation of the proposed shielding.
are marked as $A$ and $B$, and those of shielding are marked as $A'$ and $B'$. $B$ is connected to the secondary ground and $B'$ is connected to primary ground. The windings can be stretched along the $x$-axis to map the voltage potential at each point on the windings to the $U$-$x$ coordinate at the bottom of Fig. 3.35. In Fig. 3.35(a), since the secondary winding and shielding are identical, the voltage potentials of both at the same position on the $x$-axis are identical, so the two curves on the $U$-$x$ coordinate overlap each other, and have $U = V_{SR}$ at $x = 0$ and $U = 0$ at $x = L$. In Fig. 3.35(b), the secondary winding remains the same, while the shielding is rotated by 270°. Then the shielding has $U = \frac{3}{4}V_{SR}$ at $x = 0$ and $x = L$. Since the shielding has an opening between terminals $A'$ and $B'$, the shielding has $U = 0$ on the left edge of $x = \frac{3}{4}L$ and $U = V_{SR}$ on the right edge of $x = \frac{3}{4}L$. It can be seen from Fig. 3.35(b) that there is a displacement current circulating from the secondary winding to the shielding and then back to the secondary winding, so the net CM current between the secondary winding and shielding is still zero although the shielding is rotated by 270°. Similarly, it can be further proven that the net current is zero even when the shielding is rotated by an arbitrary angle.

(a) Shielding identical to secondary winding.  (b) Shielding rotated by 270°.

Fig. 3.35. Voltage potential on secondary windings and shielding.
By rotating the shielding, the two terminals of the shielding can converge at the center of the matrix transformer as shown in Fig. 3.36. Then the ground terminals for the shielding can be connected through the PCB trace from the center to the middle of the left edge, so that the PCB trace for the primary does not occupy the output terminals on the top and bottom edges.

![Diagrams showing rotation of shielding](image)

(a) Layer 2.  
(b) Layer 5.

Fig. 3.36. Rotating the shielding.

The PCB winding implementation can be completed by including the traces to connect node S, as shown in Fig. 3.37. Vias are also needed for the connection between the primary windings and the shielding. With the proposed PCB winding implementation, all the windings and the connection are limited to within the footprint of the matrix transformer. Although vias are added for the connection between shielding, the vias related loss is relatively small since the primary current is less than 5A and distributed to 4 sets of shielding.
To verify the winding loss reduction with the proposed shielding, the FEA simulation result is shown in Fig. 3.38, in which the windings are idealized by eliminating vias and termination. The Secondary 1 is set to be conducting a secondary current. The termination and vias effects are analyzed with the method mentioned in [36][37]. The proposed shielding doesn’t impact the secondary winding loss, but reduces the primary winding loss significantly. Overall, the proposed shielding can reduce the total winding loss by 4%.

Fig. 3.37. PCB winding implementation of the proposed rotated shielding.
(b) With shielding.

Fig. 3.38. Winding loss simulation.

The 1MHz 800W 400V/12V LLC converter prototype with the proposed matrix transformer and shielding is shown in Fig. 3.39. It has the same footprint as a quarter-brick, but a much smaller height of 0.27inch, compared to the height of 0.50inch for a quarter-brick. An output power of 800W at such a dimension is equivalent to a power density of around 900W/inch$^3$. Adding the proposed shielding does not increase the volume of the LLC converter. The prototype maintains the same power density as the design without shielding.

(a) Prototype without top plate.  (b) Fully-assembled prototype.

Fig. 3.39. 1MHz 800W 400V/12V LLC converter prototype with proposed shielding.
3.2.3. Experimental results

The experimental waveforms under the full-load condition are shown in Fig. 3.40. Here, it shows that ZVS for both the primary and secondary switches can be achieved. Moreover, there is no ringing in the $V_{ds_{SR}}$ due to the minimum secondary leakage.

![Fig. 3.40. Experimental waveforms under the full-load condition.](image)

Fig. 3.40. Experimental waveforms under the full-load condition.

Fig. 3.41 shows the measured CM noise spectrums of the proposed LLC converter. The red curve is the design without shielding and the blue curve is the design with the proposed shielding. The proposed shielding can attenuate the CM noise by around 30dB, and such attenuation is effective in all frequency spectrums of interest up to 30MHz. A conventional CM choke cannot achieve such a good attenuation at very high-frequency range due to its parasitic capacitance.

![Fig. 3.41. Measured CM noise spectrums.](image)
The measured efficiency curve of the proposed LLC converter is shown in Fig. 3.42. Compared to the design without shielding, the proposed shielding can improve the full-load efficiency from 97.2% to 97.4% and improve the peak efficiency from 97.6% to 97.7%. It has a slightly lower light load efficiency since the conduction loss is not dominant at the light load condition while there is extra eddy current loss on the shielding which is not serving as the primary windings.

Fig. 3.42. Measured efficiency.

Fig. 3.43 provides the thermal test results of the proposed LLC converter under the full-load condition, 25°C ambient temperature and 200 LFM (Linear Feet per Minute) fan speed. The proposed design has better thermal behavior due to a higher efficiency, improved layout and two more copper layers to dissipate the heat compared to the design without shielding.
Loss breakdown for the designs with and without shielding under full-load condition is analyzed as shown in Fig. 3.44. The design with proposed shielding has the following improvement: the primary MOSFET conduction loss reduction is achieved with a smaller primary current due to a higher turn ratio; the primary winding loss reduction is achieved as analyzed by the FEA simulation in Section IV; the SR conduction loss reduction is achieved due to a lower junction temperature, thus a lower on-resistance; more output capacitors are placed to reduce the output current ripple related loss.
3.2.4. Conclusions

For high output current LLC converters, the planar matrix transformers with PCB windings are advantageous over the conventional transformer designs because of its high efficiency and high power density. However, it suffers from a large inter-winding capacitance of the PCB windings, which causes a large CM noise. This is more severe when GaN device is applied because it has a higher $dv/dt$ than its Si counterpart. To predict the CM noise spectrum for the matrix transformers, a model for the inter-winding capacitance has been developed. Shielding is an effective method to attenuate the CM noise in all frequency spectrums of interest, and it is more suitable for PCB windings since it can automatically be embedded in the fabrication process. But shielding will cause extra losses and decrease efficiency.

A novel shielding structure is proposed to utilize half of the shielding as the primary winding while still maintaining the benefit of the CM noise attenuation. Shielding is supposed to be identical to the secondary windings, while it is proven in this section that the proposed shielding
can be rotated to simplify the PCB traces for connection and minimize interference between the primary traces and the output terminals. The proposed shielding is verified by experiments on 1MHz 800W 400V/12V LLC converters. The proposed shielding can attenuate the CM noise by around 30dB, effective in all frequency range; improve the full-load efficiency from 97.2% to 97.4% and improve the peak efficiency from 97.6% to 97.7%.

3.3. Dynamic bus voltage control for 2-stage 48V VRM

A very popular power architecture for the data centers is the 48V distribution bus with 48V/1.8V VRM on the motherboard. The two-stage 48V-12V-1.8V VRM is widely adopted in such applications. The LLC converter is the preferred choice for the first conversion stage [8][10] since it provides the isolated 12V output efficiently. The multi-phase Voltage Regulator (VR), then, takes the 12V and converts it to 1.8V. Fig. 3.45 is an example of two-stage VRM in such configuration.

![Fig. 3.45. Structure of two-stage 48V-12V-1.8V VRM](image)

Due to the importance of light load efficiency, many efforts have been made to improve the light load efficiency of the Buck VR [64][65][66][67][68]. Several control approaches, which utilize the duty cycle signal to improve the efficiency at light load, are proposed in [64]. A load
adaptive VR, called adaptive FET modulation, has been proposed in [65], which achieves high efficiency that extends to light and heavy load regions. Adaptive ON-time control and a novel nonlinear inductor are proposed to improve discontinuous-current-mode efficiency [66]. Different synchronous rectifier (SR) self-drive methods are employed in [67], which allow the SR driver voltage to be lowered from the input voltage $V_{IN}$ to an optimized voltage so that the overall efficiency is improved. A two-stage 12V VR and related advanced control schemes to improve light-load efficiency have been proposed in [68] by reducing the $V_{IN}$ for the second stage.

In order to maximize its efficiency due to a fixed switching frequency $f_s$, the LLC DCX stage is mostly used as unregulated. Topology change is employed in many applications to deal with very wide input-voltage and/or output-voltage ranges [69][70][71][72]. By changing the topology, the gain of the converter is changed effectively so that $f_s$ range is still narrow and efficiency can be improved. However, if the topology transitions in [69] are made abruptly the result will be large stresses in the resonant tank during the transitions. Topology transitions in [70][71] are achieved by stopping and restarting the circuit, which requires a large output capacitance to reduce the output voltage $V_O$ variations. The improved control method proposed in [72] maintains a tight regulation of $V_O$ with reduced stresses in the resonant tank. However, the transition takes a long time and the ZVS for 2 switches is lost during the transition period.

The benefit from the efforts to improve either the DCX stage or the VR stage, as mentioned above is quite limited for the two-stage VRM. This section proposes a two-stage 48V-12V/6V-1.8V VRM, which can change the primary side of the LLC DCX dynamically in the light load condition from FB configuration into HB configuration, so that the output of the LLC DCX can be changed from 12V to 6V, which increases the overall light load efficiency significantly due to reduced core loss of the LLC DCX and the reduced switching loss of the multi-phase VR.
Moreover, to achieve a fast transition of the bus voltage between 12V and 6V, the minimum capacitance for the intermediate bus $V_{O, LLC}$ is properly selected and the Optimal Trajectory Control (OTC) for transition between FB and HB is proposed. Experiments demonstrate the fast transient response and a more than 10% light load efficiency improvement.

### 3.3.1. Design and evaluation of two-stage 48V VRM

For the two-stage VRM structure, the LLC resonant converter is deemed the most desired topology for the first stage because of its high efficiency and high power density. The LLC converter can achieve ZVS for the primary devices and ZCS for the secondary SRs. These features are not only beneficial for achieving a higher efficiency but also for lowering EMI noises. Multi-phase Buck converter is the most widely used as the second stage due to small current ripple and ability to achieve high-bandwidth design.

For applications that require low-voltage, high-current outputs, such as computer servers, there are several important design considerations for the LLC converter with 12V output: 1) the state-of-the-art SRs are best operated with 10-15A. One should consider paralleling SRs to reduce conduction loss. Both static and dynamic current sharing, when paralleling a large number of SRs, are difficult to achieve. 2) The large sum of high frequency and high $di/dt$ AC currents must flow through a common termination point between the transformer and the SRs. This can result in large termination losses. 3) The large leakage inductances at the transformer secondary-side windings result in large winding losses.

A matrix transformer structure proposed in [57] has demonstrated superior benefits over the conventional design. The schematics of the LLC converter with matrix transformers is shown in Fig. 3.46(a). Since the primary current for all the transformers are the same, the secondary current
is perfectly balanced. The matrix transformer structure integrates 2 transformers into 1 UI core to reduce the core loss and achieve high power density as shown in Fig. 3.46(b). The transformer is implemented by 12-layer PCB winding. By integrating the SRs and output caps in the secondary windings, the termination point, where all currents are summed, occurs on the DC side, thus causing no termination loss. Transformer winding losses are significantly reduced, as are the leakage inductances.

![Schematics](image1)

(a) Schematics

![Transformer structure](image2)

(b) Transformer structure

Fig. 3.46. LLC converter with matrix transformers

Based on the techniques referred above, a 240W 48V/12V LLC DCX prototype has been designed. The detailed specifications is shown in Table 3.2. The prototype is shown in Fig. 3.47(a), which has a dimension of $20mm \times 31mm$ and a thickness of $8mm$. By pushing the $f_s$ up to 1.6MHz, a power density of 860W/in$^3$ is achieved. The standard driving circuit using LM5113 for GaN devices recommended by EPC is employed for both the primary side and the secondary side with a turn-on resistance of $5\Omega$ and a turn-off resistance of $0\Omega$. Since the control is on the secondary side, IL611 isolators are placed between the driving signals and the primary drivers. The efficiency of the LLC DCX is measured under nominal $V_{IN}$ with different load condition. High efficiency is demonstrated with a peak efficiency of over 97%, as shown in Fig. 3.47(b).
Table 3.2. Specification of the LLC DCX

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency ($f_s$)</td>
<td>1.6MHz</td>
</tr>
<tr>
<td>Dead Time</td>
<td>66ns</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>4:1</td>
</tr>
<tr>
<td>Primary devices</td>
<td>EPC2021</td>
</tr>
<tr>
<td>Secondary devices</td>
<td>EPC2030</td>
</tr>
<tr>
<td>Drivers</td>
<td>LM5113</td>
</tr>
<tr>
<td>Isolator</td>
<td>IL611</td>
</tr>
<tr>
<td>Resonant Capacitor</td>
<td>330nF</td>
</tr>
<tr>
<td>Resonant Inductance</td>
<td>21nH</td>
</tr>
<tr>
<td>Magnetizing Inductance</td>
<td>2.9uH</td>
</tr>
</tbody>
</table>

Fig. 3.47. Prototype and efficiency of 240W 1.6MHz 48V/12V LLC DCX

For the second stage of the 48V-1.8V VRM, the industrial practice uses DrMOS as the switches for the multi-phase Buck converter. 3 candidates DrMOS, including TDA21231 from Infineon, SiC620R from VISHAY and CSD95378 from Texas Instruments, have been evaluated for the 12V/1.8V VR. The efficiency of the 3 candidates are measured under the same condition,
with an $f_s$ of 1MHz and an inductor of 200nH. Fig. 3.48(a) is the evaluation board for TDA21231 and SiC620R, both of which have the same package, and Fig. 3.48(b) is for CSD95378. The measured efficiency is shown in Fig. 3.49, and TDA23231 is selected because it has demonstrated the highest efficiency.

![Evaluation boards for Candidates DrMOS](image)

(a) TDA21231 and SiC620R  
(b) CSD95378

**Fig. 3.48. Evaluation boards for Candidates DrMOS**

![Measured efficiency of candidates DrMOS](image)

**Fig. 3.49. Measured efficiency of candidates DrMOS**

In the VR application, the CPU can provide the load transient information to the VR controller, which is called Power State Indicate (PSI) [73]. When the CPU enters the light load condition, the PSI indicates the load step down simultaneously. So the VRM enters a phase shedding mode to improve the light load efficiency. When the CPU enters the heavy load condition, the PSI indicates
this 3.3us ahead of the load transient, so the VR controller has some time to recover the power stage from the phase shedding mode. The recommended cutoff frequency for PSI is between 1kHz to 10kHz. The principle of PSI is shown in Fig. 3.50.

![Fig. 3.50. Principle of PSI signal](image)

The light load efficiency improvement for a two-stage structure with phase shedding mode is evaluated as shown in Fig. 3.51. In the light load range, the red dotted line is the case without phase shedding and the blue solid line is the case with phase shedding. There is some improvement with the phase shedding, but it’s insignificant and further improvement is necessary. Since the CPUs are constantly operating between the sleep-mode and the wake-up-mode, and most of the time in the sleep-mode. It is of great meaning to further improve the light load efficiency, and this

![Fig. 3.51. Measured light load efficiency improvement with phase shedding](image)
section proposes a method using dynamic bus voltage control, which benefits the light load efficiency of both the LLC DCX and the multi-phase VR.

3.3.2. Proposed light-load efficiency improvement

Reducing the intermediate bus voltage $V_{O_{LLC}}$ is helpful to further improve the light load efficiency due to the reduced core loss for LLC DCX and the reduced switching loss for multi-phase Buck converter. To operate an LLC DCX with an input-output gain much smaller than 1 is, however, not without significant technical challenges, for two reasons. One reason is that the LLC DCX has been proven to be optimal for efficiency when operating at the resonant frequency $f_o$. Suppose the resonant converter is designed and optimized for a 12V output. An LLC DCX normally uses the leakage inductance of the transformer as the resonant inductor, which is very small, so it has a rather flat gain characteristic around $f_o$. To reduce $V_{O_{LLC}}$, it would require a significant drift away from the optimal operating point. This significant drift away which would render itself with a rather poor efficiency. The second reason is that the resonant converter is very difficult to control its dynamics with sufficient speed and a short settling time to match the dynamic power demand from the CPUs, in order to improve its light load efficiency.

To solve the first challenge, this section proposes to change the LLC DCX from the FB configuration into the HB configuration dynamically at the light load condition. By doing this dynamic configuration change, the LLC DCX is still able to operate at $f_o$, while the input-output gain is reduced by half and $V_{O_{LLC}}$ is changed from 12V to 6V. To achieve the FB configuration as shown in Fig. 3.52(a), the Q3 switch needs to be synchronized with Q1, and the Q4 switch needs to be synchronized with Q2. To achieve the HB configuration as shown in Fig. 3.52(b), the Q3 switch needs to be kept on all the time, and the Q4 switch needs to be kept off all the time.
The configuration change is based on the PSI signal as shown in Fig. 3.53. When PSI indicates the load step down, the DCX enters the HB configuration to change $V_{O_{LLC}}$ into 6V. When the PSI indicates the load step-up, the DCX enters FB configuration and settles $V_{O_{LLC}}$ into 12V within 3.3us. By doing this, we are able to reduce the voltage*second of transformer by half for the DCX and reduce the switching loss for the POL at the light load condition. Both are dominant losses for the light load condition.

The efficiency with the proposed method is measured and the result is shown in Fig. 3.54. With the proposed method, the light load efficiency for both the LLC DCX and the multi-phase VR are greatly improved, resulting in a significant improvement in the overall light load efficiency.
The concern on the second challenge with this method is how to achieve the fast transient requirement of the CPU. The intermediate bus capacitor \( C_{O\_LLC} \) determines the transient response of \( V_{O\_LLC} \). When the PSI requires the transition from the light load condition to the heavy load condition the LLC DCX must be able to charge \( C_{O\_LLC} \) from 6V to 12V. To limit the output current of the LLC DCX \( I_{O\_LLC} \) within 2 times the nominal output current \( I_{Full} \), we can derive the expression for the range of \( C_{O\_LLC} \) as below, where \( I_{IN\_VR} \) is the input current for the VR, which is very small at the light load condition. In this case, 18uF cap is chosen as \( C_{O\_LLC} \) considering the transient requirement.

\[
\Delta t = \frac{C_{O\_LLC} \Delta V}{I_{O\_LLC} - I_{IN\_VR}} = \frac{C_{O\_LLC} \Delta V}{2I_{Full} - I_{IN\_VR}} < 3.3\mu s 
\] (3.22)
The light load efficiency improvement with the HB configuration has demonstrated superior performance as shown above, however, the control for the transient is quite a challenge due to the dynamics of the resonant converters. To better understand the operation of the LLC converter, the state-trajectory is used to describe the operation of the resonant tank, which is drawn with the x-axis of normalized resonant voltage (normalizing factor = $V_{IN}$) and the y-axis of normalized resonant current (normalizing factor = $V_{IN}/\sqrt{L_r/C_r}$). The time-domain waveforms and corresponding state-trajectory of the FB configuration under the heavy load condition and the HB configuration under the light load condition in the steady state is shown in Fig. 3.55. In the HB configuration, there is a $V_{IN}/2$ DC bias in the resonant cap, compared with no DC bias for the FB configuration. The conventional control method cannot handle such a large energy change in a fast manner with limited stresses.

Fig. 3.55. Waveforms and state-trajectory of FB and HB configurations
3.3.3. **Fast transient response from half-bridge to full-bridge**

The state trajectory control [21][22][23], in essence, controls the instantaneous energy of the resonant tank on a cycle-by-cycle basis. It has been applied to the LLC converters to achieve different control functions [24][25][26]. And the control is further simplified and applied to the high frequency LLC converters by a microcontroller [31][32][33][34]. Based on the same concept, the OTC for fast transient between FB and HB is proposed in this section to solve the second challenge: the fast transient response in the light load efficiency improvement for CPU VRM. The proposed OTC from HB to FB employs similar concepts used in the start-up mentioned in [32]. The whole process is divided into 3 stages and the control law is explained as follows.

Stage 1 uses an asymmetrical current limiting band to settle the resonant tank from the HB steady state to around the origin (0, 0), which is the shaded area shown in Fig. 3.56(a). When the controller receives the PSI signal for transition, Q2 and Q4 are turned on, and the trajectory goes down until it touches the negative current band; then Q1 and Q3 are turned on, and the trajectory goes up, until it touches x-axis; then Q2 and Q4 are turned on again. This process continues until the DC bias is settle to around 0V. Stage 2 uses a symmetrical current limiting band to optimize the energy delivery as shown in Fig. 3.56(b). When the trajectory touches the positive current limiting band, Q2 and Q4 are turned on; and when the trajectory touches the negative current limiting band, Q1 and Q3 are turned on. $V_{O, LLC}$ is built up gradually in Stage 2. Stage 2 ends when $V_{Cr} \approx V_{in} - nV_{O, LLC}$ at the switching instant as highlighted in the shaded area in Fig. 3.56(b), after which, the switching instants cannot be determined by the current limiting band. Based on such mechanism, the converter operates with an optimal frequency at given $V_{O, LLC}$ condition, such that the delivered energy is maximized under given stress requirement. Stage 3 simply decreases $f_S$
gradually to $f_0$, whose trajectory is shown in Fig. 3.56(c). The details about the theories and the implementation of the control method for these 3 stages can be referred in [32].

Fig. 3.56. State-trajectory illustration of OTC from HB to FB

The OTC in this section is implemented by digital controller using the method in [32]. Briefly speaking, the switching pulses in Stage 1 and $f_s$ in Stage 2 and Stage 3 is determined based on $V_{O, LLC}$. The control system is programmed to operate as follows: when the controller receives the PSI signal for transition from the CPU, the controller would generate switching pulses subsequently for Stage 1; then controller senses $V_{O, LLC}$ and determine $f_s$ accordingly for Stage 2;
in Stage 3, the controller simply decrease $f_S$ gradually to $f_O$. Take Stage 2 as an example to explain how $f_S$ for given $V_{O, LLC}$ can be calculated based on the trajectory in Fig. 3.57, ($V_{oN}$ in Fig. 3.57 means normalized $V_{O, LLC}$):

Fig. 3.57. Calculating $f_S$ for given $V_{O, LLC}$

The switching period $T_S$ is then calculated as follows:

$$\alpha = \sin^{-1}\left(\frac{l_{maxN}}{\rho_1}\right); \quad \beta = \sin^{-1}\left(\frac{l_{maxN}}{\rho_2}\right)$$

(3.23)

$$T_S = \frac{2(\alpha + \beta)}{\omega_o}$$

(3.24)

A simplified control scheme for the OTC employed in this section is shown in Fig. 3.58. The OTC in the digital controller can be achieved using either real-time calculation or look-up table. The transient speed from HB to FB can be easily controlled by adjusting the current limiting band and/or $C_{O, LLC}$. A larger current limiting band always means a faster transient response, while at the same time, a smaller design margin. A current limiting band equivalent to 2 times full load RMS current stress is selected in this section considering the tradeoff between the transient response speed required by CPU and the design margin acceptable for most designs.
A simulation model has been built with a current limiting band of 2 times the full load RMS current stress and a $C_{O, LLC}$ of 18uF; the proposed control method is verified as shown in Fig. 3.59. The whole process is limited within 3.3us, which can satisfy the transient requirement of PSI. From the state-trajectory, it shows that both the current and voltage stresses are limited within the given range, which insures that the converter will operate safely under such high transient speed.

![Diagram of OTC control scheme](image)

**Fig. 3.58. Simplified control scheme of the proposed OTC**

(a) Time-domain waveforms  
(b) State-trajectory

**Fig. 3.59. Simulation of the proposed OTC for transient from HB to FB**
It might be a concern that during the transition from HB to FB, there may be some unbalanced DC-bias in the magnetizing current. While it is not a problem here due to the following reasons: the period of each switching instant is quite a short time in Stage 1, meaning that little fluctuation in the DC-bias of the magnetizing current will be induced; even there is a little fluctuation, the converter is switching in a symmetrical way in Stage 2 and Stage 3, which is similar to the optimal frequency control, such that the any unbalance in the DC-bias will diminish very soon. This phenomenon can be observed in Fig. 3.59(a), the DC-bias of the magnetizing current is always around zero during the transition.

3.3.4. Fast transient response from full-bridge to half-bridge

A simple way to solve the transient from FB to HB, i.e. $V_{O, LLC}$ decreases from 12V to 6V, is to rely on the load current to discharge $C_{O, LLC}$. However, the load condition is already very light when the LLC DCX needs to switch to HB. By using a 20A CPU current as an example, we see that it’s equivalent to a 4A current discharges $C_{O, LLC}$, which would take more than 30us as shown in Fig. 3.61. It takes too long for the transition which is not acceptable. A smarter idea is to recycle the energy in $C_{O, LLC}$ back to the 48V source.

![Fig. 3.60. Transient from FB to HB with load current to discharge $C_{O, LLC}$](image)
To recycle the energy in $C_{O,LLC}$ back to the 48V input source, we need to operate the LLC in reverse. Fig. 3.61 is the schematics of the LLC reverse operation in HB configuration. Q3 is always on and Q4 is always off in order to achieve HB configuration. Q1 and Q2 operate as SRs and can achieve ZCS. S1 and S2 operate as active switches and can achieve ZVS. The energy flows in reverse from $V_{O, LLC}$ to $V_{IN}$.

Fig. 3.61. Schematics of reversely operating LLC in HB configuration

Fig. 3.62 is an example of the LLC reverse operation in HB configuration with $V_{IN} = 48V$, $V_{O, LLC} = 9V$ and $f_s > f_0$. From $t_0$ to $t_1$, S1 is in on-state and the resonant current is negative and goes back to the 48V source through Q1 and Q3. S2 is turned-on at $t_1$, and the resonant current is still negative and goes back to source from $t_1$ to $t_2$. From $t_2$ to $t_3$, S2 is in on-state and the resonant current becomes positive and circulates through Q2 and Q3. S1 is turned-on at $t_3$ and the resonant current circulates through Q2 and Q3 from $t_3$ to $t_4$.

Fig. 3.62. Reverse operation of LLC at above $f_0$
The equivalent load for the HB reverse operation can be derived, as shown below using half of $V_{IN}$ divided by 2 times the current delivered back to the source, so as the characteristic impedance:

$$R_{eq} = \frac{V_{IN}/2}{2I_{in}} = \frac{R_{IN}}{4}$$  \hspace{1cm} (3.25)

$$Q_{eq} = \frac{\sqrt{L_r/C_r}}{R_{eq}}$$  \hspace{1cm} (3.26)

Fig. 3.63 is the gain curves of reversely operating LLC with y-axis of $nV_{O, LLC}/V_{IN}$. The LLC should operate at above $f_{o}$ to achieve ZVS for the active switches. To recycle the energy back to the 48V source $V_{IN}$, the LLC should decrease $f_S$ gradually so that the gain is reduced from 1 to 0.5.

Fig. 3.63. Gain curves of reversely operating LLC converter

With the LLC reverse operation, the transient from FB to HB can be accelerated. The OTC for transient from FB to HB is proposed below. The whole process is divided into 3 stages and the control law is explained as follows.

The control law for Stage 1 is to extend the on-time for switch Q1, Q3 from $t_0$ to $t_1$ until $V_{Cr} \approx V_{in}/2$, which means the trajectory enters the shaded area as shown in Fig. 3.64(a). Then Q2 and Q4 are conducting from $t_1$ to $t_2$ until the trajectory comes to around (0.5, 0). Stage 2 uses a current limiting band to optimize the reverse energy flow in HB configuration as shown in Fig. 3.64(b). S1 and S2 are active switches in Stage 2. When the trajectory touches the positive current limiting
band, S1 is turned on; and when the trajectory touches the negative current limiting band, S2 is turned on. The $V_O$ decreases gradually in Stage 2. Stage 2 ends when $V_{Cr} \approx V_{in} - nV_{O, LLC}$ at the switching instant as highlighted in the shaded area in Fig. 3.64(b), after which, the switching instants cannot be determined by the current limiting band. Stage 3 simply decreases $f_s$ gradually to $f_o$ and the LLC DCX will merge to HB configuration as shown in Fig. 3.64(c).

Fig. 3.64. State-trajectory illustration of OTC from FB to HB

The details about OTC implementation is similar to that in Section IV. The transient speed from FB to HB can also be easily controlled by adjusting the current limiting band or $C_{O, LLC}$. The proposed control method is verified on the same simulation model mentioned in Section IV. The result is shown in Fig. 3.65. The whole process is around 4us, which can satisfy the cutoff frequency requirement of PSI. From the state-trajectory, it shows that both the current and voltage stresses are limited within the given range.
Stage 1 of the transition from FB to HB involves a period of charging the magnetizing inductor as shown in Fig. 3.64(a) from $t_0$ to $t_1$. The magnetizing current reaches the peak at $t_1$, while immediately discharged to zero afterwards. This peaks magnetizing current will not cause a potential saturation problem for the magnetizing inductance in most cases, since the DC/DC transformers are normally designed based on efficiency consideration, which means that the saturation flux of the core would be much higher than the peak flux during the transition.

### 3.3.5 Experimental results

The proposed OTC for fast transient between FB and HB is verified on the hardware prototype mentioned in Section II. An 18uF cap is selected for $C_{O, LLC}$. The control is implemented by digital controller TMS320F28335 based on the implementation method proposed in [31][32][33][34].

FB under full load (20A) condition is tested as shown in Fig. 3.66(a). ZVS is achieved for the primary switches with a dead time of around 66ns. HB under light load (4A) condition is tested as
shown in Fig. 3.66(b). Since voltage*second of the transformer is reduced by half, so as the peak of the magnetizing current, the dead time for HB is doubled to ensure ZVS for the primary switches.

![Image](https://via.placeholder.com/150)

(a) FB under full load (20A)  
(b) HB under light load (4A)

**Fig. 3.66. Experiments of FB and HB stable operation**

It is worth noting that to maintain stable HB operation, magnetically-coupled gate drivers, such as driving transformers, are not proper since the Q3 switch is required to be kept on. A bootstrap driving IC combined with digital isolator is recommended in this application, which is also deemed to be the most suitable driving circuit for high frequency GaN applications [74]. Bootstrap driving IC LM5113 and isolator IL611 are employed in the experiments in this section.

The transient from FB to HB with the load current to discharge $C_{O, LLC}$ is tested as shown in Fig. 3.67. Since the PSI will provide a transient signal simultaneously when the transient from heavy load to light load happens, the controller settles $V_{O, LLC}$ under the light load condition, which is equivalent to a maximum light load current for the LLC DCX of 4A. It takes around 40us for the transient, which is far away from the CPU transient requirement.
Fig. 3.67. Experiment of FB to HB with load current to discharge $C_{O, LLC}$

The transient from HB to FB with the proposed OTC is tested as shown in Fig. 3.68(a). It is tested under the worst case with the maximum light load current for the LLC DCX of 4A, which is sufficient to verify the concept. Since the PSI signal will provide the transient signal 3.3us ahead of the transient from light load to heavy load, the controller has 3.3us to settle the $V_{O, LLC}$, during which the maximum load condition is 4A. Under other load conditions, the transient will be even faster while the current stress is still within the current limiting band as discussed in Section IV.

The transient from FB to HB with the proposed OTC is tested under 4A load current as shown in Fig. 3.68(b). With the help of reverse operation, the transient process is accelerated by 8 times compared to Fig. 3.67, and it takes only 5us to finish the transient, during which the current stress is still within the current limiting band as discussed in Section V.
The experimental results have demonstrated that, by employing the proposed method, the transient from HB to FB takes less than 3.3us, which satisfies the CPU transient requirement. And the transient from FB to HB with the proposed method takes around 5us, which satisfies 10 kHz cutoff frequency for PSI. In both cases, the resonant current stress is always limited within the current limiting band and the transient of the $V_{O, LLC}$ is very smooth.

### 3.3.6. Conclusions

In this section, a two-stage 48V-12V-1.8V VRM structure that focuses on server and data center applications is investigated. The LLC resonant converter is deemed the most desired topology for the first stage because of its high efficiency and high power density with ZVS for the primary devices and ZCS for the secondary SRs. A 240W 48V-12V LLC DCX prototype has been designed using a matrix transformer structure and the PCB windings. A power density of 860W/in$^3$ and a peak efficiency of over 97% is demonstrated under a 1.6MHz switching frequency. Three DrMOS candidates have been evaluated for 12V-1.8V VR under the same conditions, and the one with the best performance has been used in the analysis in this section.
A novel 48V-12V/6V-1.8V VRM has been proposed, which can improve the light load efficiency significantly due to the reduced core loss of the LLC DCX and the reduced switching loss of the multi-phase VR. More than 10% light load efficiency improvement is achieved. The Optimal Trajectory Control (OTC) for fast transient between full-bridge configuration (48V-12V-1.8V) and half-bridge configuration (48V-6V-1.8V) has been proposed to meet the fast transient requirement from the CPU. Experimental results of the proposed OTC have been demonstrated on the 1.6MHz LLC DCX with proper selection of the intermediate bus capacitance. The transient from half-bridge configuration for light load to full-bridge configuration for heavy load is achieved within 3.3us and 2 times resonant current stress. The transient from full-bridge configuration to half-bridge configuration is achieved at around 5us, also within 2 times the resonant current stress.
Chapter 4. High-frequency Three-phase Interleaved LLC Converters

The AC/12V PSU for datacenter architecture is normally designed to have 1kW output power [78]. While those for datacenter architecture with 48V bus and telecom power supplies are normally designed to have 3kW output. To increase the output power, full-bridge configuration can be employed instead of half-bridge for the primary side [79], but output current and voltage ripples are also increased. Different two-phase interleaved LLC converter has been proposed in [80]-[83], but all two-phase interleaved LLC converters require additional switches, components, and control algorithm to achieve current sharing, which increases system cost and decreases efficiency.

Three-phase interleaved LLC converter, as shown in Fig. 4.1, can achieve automatic current sharing by interconnecting the three phases in certain ways, including connecting the primary sides to a common Y-node (Y-primary) [84], connecting the secondary sides to a common Y-node (Y-secondary) [85], and employing a delta-connect resonant capacitor network (∆-Cr network) for primary sides [86]. Furthermore, the primary and secondary RMS current can be reduced due to interaction between three phases [84]-[86], and three inductors and three transformers can be integrated into one magnetic component [86]. Other three-phase interleaved LLC converters are presented in [87][88], but they both requires additional balancing transformer. To sum up, three-phase interleaved LLC converter is considered as a superior candidate for 3kW 400V/48V DC/DC converter with the benefits of automatic current sharing, reduced RMS current and integrated magnetics.
If three individual inductors and three individual transformers are employed in three-phase LLC converter, the volume and cost will increase a lot. Therefore, magnetic integration is necessary for application of three-phase LLC converter. But present DC/DC converters, operating at 50-100 kHz with a power density less than 50W/in\(^3\), require large bobbins and hand-wound windings, the integrated magnetic is still large and hard to manufacture. The trend for datacenters or distributed power systems is the pursuit of higher efficiency and higher power density. The fast development of wide bandgap devices and novel magnetic materials provides opportunities to push \(f_s\) higher [89][90]. MHz LLC converters with GaN devices have been designed for different applications and significantly improved power density has been demonstrated [36][37][57]. Digital control systems for high-frequency LLC converters have also been demonstrated [33][34][35][75][91][92]. When \(f_s\) is pushed around MHz, PCB winding can be employed to achieve high efficiency, high power density and automatic manufacturing [78]. 12-layer PCB and concept of flux cancelation are employed to reduce transformer size and losses [57], but 12-layer PCB is expensive and has large inter-winding capacitance. An alternative solution is to use a simple four-layer PCB to implement the transformer and integrate SRs and output capacitors as part of the secondary winding to eliminate AC termination loss [36][37]. When using four-layer PCB windings, two shielding layers could be placed in between primary and secondary windings.
Each shielding layer is connected to the primary ground. Therefore, the CM noise current can only circulate in the primary side [39]. The high-frequency transformer is further improved by integrating four transformers into one magnetic core [93], and applying a novel shielding technique [94].

### 4.1. Investigation of three-phase interleaved LLC converters

Three-phase interleaved LLC converters is first proposed in [84] to interconnect the primary sides to a common Y-node as shown in Fig. 4.2(a). With such a topology, simply interleaving the primary switches with 120° phase shift will provide automatic current sharing between phases even there is tolerance in the resonant tanks of each phase. Another topology of three-phase LLC converter is proposed in [85] to connect the secondary sides to a common Y-node, as shown in Fig. 4.2(b). The average voltage of secondary common Y-node is half of output voltage $V_O$, so that the effect secondary Y-node is same as that of voltage doubler structure in secondary side.

![Fig. 4.2. Three-phase LLC converter topologies.](image)

The three phases in both topologies in Fig. 4.2 can interact with each other through the voltage fluctuation at either primary Y-node or secondary Y-node [84][85]. Such interaction can help reduce the RMS current in both primary side and secondary side as shown in Fig. 4.3, in which
\(i_{Lr\_1ph}\) is the resonant current of single-phase LLC converter with 1kW output power and \(i_{Lr\_3ph}\) is that of three-phase LLC converter with 1kW output power for each phase. It is shown that the peak current, as well as the RMS current of \(i_{Lr\_3ph}\) are reduced compared to those of \(i_{Lr\_1ph}\), so that three-phase interleaved LLC converter will result in a smaller conduction loss.

![Graph showing comparison between single-phase and three-phase LLC converter currents.](image)

Fig. 4.3. Comparison between resonant current of single-phase and three-phase LLC converter.

Another three-phase interleaved LLC converter topology connects the primary sides to a delta-connected resonant capacitor network (\(\Delta\)-Cr network) [86], as shown in Fig. 4.4(a). The operation of \(\Delta\)-Cr network is equivalent to Y-primary or Y-secondary, however, the required capacitance of each resonant capacitor \(C_r\) in \(\Delta\)-Cr network is just one third of that in Y-primary. And since both terminals of each resonant capacitor are connected to switching nodes, there is no DC bias in the resonant tank. The simulated time-domain waveforms in Fig. 4.4(b) shows that the resonant current of \(\Delta\)-Cr network \(i_{Lr\_\Delta}\) is the same at that of Y-primary \(i_{Lr\_Y}\), and the resonant voltage of \(\Delta\)-Cr network \(V_{Cr\_\Delta}\) has no DC bias, but with a larger amplitude compared to that of Y-primary \(V_{Cr\_Y}\).
(a) Topology.            (b) Time-domain waveforms.

Fig. 4.4. Three-phase interleaved LLC converter with Δ-Cr network.

When employing three-phase interleaved LLC converter, the three inductors and three transformers can be integrated into one three-phase inductor and one three-phase transformer, as shown in Fig. 4.5(a). An integrated magnetic structure is proposed in [86] to stack the three-phase inductor on top of the three-phase transformer so that all the magnetic components are integrated into one. Each of the three core legs in the middle represents either an inductor or a transformer, and the two outer legs are for magnetic shield. Such a structure, although can reduce the volume of magnetic components, is very complex to manufacture.

(a) Before integration.            (b) After integration.

Fig. 4.5. Integrated magnetic structure for three-phase LLC converter.

Based on the previous analysis, the three-phase interleaved LLC converters have the benefit of reduced input and output current ripples, reduced conduction losses due to lower RMS current,
and opportunities to integrate magnetics. The state-of-art three-phase interleaved LLC converters, operating at around 100kHz, require bulky magnetics components, which are very complex and difficult to manufacture. To solve this challenge, by pushing $f_S$ up to MHz, the size of magnetic components can be reduced significantly, and the windings can be integrated into simply 4-layer PCB windings with additional 2-layer shielding. The following sections will present proposed magnetic integration for high-frequency three-phase LLC converter and its optimization process.

4.2. Proposed magnetic integration for high-frequency three-phase LLC converters

Based on the analysis of previous three-phase LLC topologies, it is proposed in this paper to use Δ-Cr network for the primary and full-bridge structure for the secondary, as shown in Fig. 4.6. Using Δ-Cr network can eliminate DC bias in the resonant capacitors $C_r$, and the required capacitance is reduced to 1/3. The benefit of full-bridge secondary, concept of proposed integrated magnetic structure and shielding implementation (the yellow winding in Fig. 4.6) will be introduced in this section.

Fig. 4.6. Proposed three-phase LLC converter with Δ-Cr network primary and full-bridge secondary.
Three different secondary structures are compared in Fig. 4.7 and Table 4.1 based on EPC GaN devices. The half-bridge structure employs a turns ratio of 8:1 since it has a voltage doubler effect, and transformer voltage*second is $0.5 \cdot V_o/f_S$; however, the AC current path is very long, and two EPC2029 GaN devices need to be paralleled as SR to handle larger RMS current (33.0A for full load at resonant frequency $f_o$). The center-tap secondary has a smaller SR current stress (16.5A for full load at $f_o$) and smaller AC current loop, but has a larger SR voltage stress and requires two sets of secondary windings for each phase. Full-bridge secondary has same SR current stress as center-tap secondary and same SR voltage stress as half-bridge secondary, small AC current loop, and requires only one set of secondary winding for each phase. Although Full-bridge secondary requires 12 SR devices, it is selected in this paper due to efficiency consideration.

(a) Half-bridge secondary. (b) Center-tap secondary. (c) Full-bridge secondary.

Fig. 4.7. Comparison of secondary structures.

<table>
<thead>
<tr>
<th>Secondary structure</th>
<th>Half-bridge</th>
<th>Center-tap</th>
<th>Full-bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR voltage stress</td>
<td>$V_o$</td>
<td>$2 \cdot V_o$</td>
<td>$V_o$</td>
</tr>
<tr>
<td>SR current stress</td>
<td>33.0A</td>
<td>16.5A</td>
<td>16.5A</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>8:1</td>
<td>4:1</td>
<td>4:1</td>
</tr>
<tr>
<td>Voltage*second</td>
<td>$0.5 \cdot V_o/f_S$</td>
<td>$V_o/f_S$</td>
<td>$V_o/f_S$</td>
</tr>
</tbody>
</table>
When $f_s$ is pushed up to MHz, planar transformer with simple PCB windings can be employed as shown in Fig. 4.8. Each core leg represents one transformer for one phase. Since the primary and secondary windings are perfectly interleaved, the transformer leakage inductance for this structure is minimized.

(a) Top view with simplified windings.  
(b) Magnetic cores.

Fig. 4.8. Three-phase planar transformer.

To achieve certain regulation capability, the inductance of resonant inductor $L_r$ must be properly designed [10]. The leakage inductance of a perfectly interleaved transformer is not large enough to meet requirement. To achieve controllable leakage inductance in the transformer, a novel integrated magnetic structure is proposed in this paper as shown in Fig. 4.9. For each phase, a non-interleaving area between primary and secondary windings are created, and an addition core leg is inserted in order to control the amount of leakage inductance. In the propose structure in Fig. 4.9, the bottom three core legs are for transformers, and the top three are for inductors. By controlling the effective areas for transformers $A_{e,M}$ and inductors $A_{e,K}$, and air gaps for transformers $l_{g,M}$ and inductors $l_{g,K}$, the ratio $L_N$ between magnetizing inductance $L_m$ and $L_r$ can be controlled for certain three-phase LLC converter design as expressed in (4.1).

$$L_N = \frac{L_m}{L_r} = \frac{A_{e,m}/l_{g,k}}{A_{e,r}/l_{g,r}}$$  \hspace{1cm} (4.1)
When employing perfectly interleaved PCB windings, there would be very large inter-winding capacitance between the primary and secondary windings. Since the primary side employs half-bridge structure, high $dv/dt$ in the primary switching node would induce large common-mode (CM) current from the primary side to the secondary side, as shown in Fig. 4.10. The secondary side employs full-bridge structure and $dv/dt$ at the two switching nodes are complementary with the same magnitude and 180° phase difference, so these two $dv/dt$ nodes cancel each other and there is no CM noise generated from the secondary side.

The shielding technique is an effective method to suppress CM noise. It is achieved by inserting shielding layers in between the primary and the secondary windings \[39][94] as shown
in Fig. 4.11. Each shielding layer is connected to the primary ground. Therefore the CM noise current induced by the primary winding will flow to the shielding and circulate back to the primary ground. The shielding layers are made identical to the secondary windings, both are single-turn windings, so they have the same voltage potential distribution. Therefore, even there is a parasitic capacitance between the shielding layers and the secondary windings, there is no CM current between them since the voltage potential difference across this parasitic capacitance is zero.

Fig. 4.11. Shielding eliminates CM current in three-phase LLC converter with PCB winding transformer.

Fig. 4.12 shows the voltage distribution on secondary winding and shielding for one phase of the proposed transformer, and the primary winding is not included for simplicity. Two terminals of secondary windings are marked as $A$ and $B$, and those of shielding are marked as $A'$ and $B'$. The center parts of two shielding layers are connected to primary ground. The windings can be stretched along the $x$-axis to map the voltage potential at each point on the windings to the $U$-$x$ coordinate at the right side of Fig. 4.12. Since the secondary winding and shielding are identical, the voltage potentials of both at the same position on the $x$-axis are identical, so the two curves on the $U$-$x$ coordinate overlap each other, and have $U = V$ at $x = 0$ and $U = -V$ at $x = L$. 
Based on the proposed magnetic structure and shielding, the PCB winding and shielding implementation is shown in Fig. 4.13. Since the windings for three phases are identical, only the windings for one phase is shown for simplicity.

Fig. 4.13. PCB winding and shielding implementation for one phase of the proposed integrated magnetic structure.
4.3. Optimization of proposed magnetic structure for three-phase LLC converters

In order to optimize the proposed magnetic structure, this section provides an optimization process. Different magnetic materials suitable for this application are measured using the core loss measurement technique in [95] and core loss measurement results under 1MHz excitation are shown in Fig. 4.14. Among them, ML91 is selected for the following analysis since it has the lowest core loss. The core loss $P_{\text{Core}}$ can be calculated based on core loss density $P_V$ and core volume $V_{\text{Core}}$ using:

$$P_{\text{Core}} = P_V \cdot V_{\text{Core}}$$ (4.2)

![Core loss measurement under 1MHz excitation.](image)

Fig. 4.14. Core loss measurement under 1MHz excitation.

The transformer core loss can be calculated using (2), and transformer winding losses can be calculated using the method in [93][58]. Then the transformer total loss under full-load condition versus transformer core leg length $a$ as x-axis and secondary winding width $c$ as y-axis could be plotted as shown in Fig. 4.15. Since the transformer has three dimension variables, $a$, $c$ and $Ae$, $Ae$ is fixed to 250mm$^2$ to derive Fig. 4.15, in which, the numbers in the colored solid lines are the total transformer loss; the black dash line represents all the combinations of $a$ and $c$ for given footprint.
of one phase; the tangential points (marked using blue dots) between the black dash lines and colored solid lines are the optimal design points for given $Ae$.

![Diagram of Transformer Optimization](image)

**Fig. 4.15.** Transformer optimization with given $Ae$ of 250mm$^2$.

With the optimal design points derived from Fig. 4.15, the relationship between transformer loss and footprint can be derived. Furthermore, different $Ae$ (corresponding to different $P_V$ value) are swept to get the optimal $P_V$ for different footprint as shown in Fig. 4.16. It is clear that for smaller footprint, the optimal $Ae$ is smaller and corresponding $P_V$ is larger. The shielded area will be selected as the design region for this paper.
In front-end converter for server and telecom power supplies, 600V or 650V devices are employed for power factor correction circuit (PFC) and primary side of DC/DC converter. The output of PFC, i.e. the input of three-phase LLC converter, are normally regulated to be 400V; in such case, the three-phase LLC converter needs to have an output-to-input voltage gain range of 0.8 to 1.2 as shown in Fig. 4.17(a). The 48V batteries normally have a nominal voltage of around 53.5V; in order to make three-phase LLC converter have a reduced gain range and operate at unit gain point for nominal output, the input of three-phase LLC converter can be regulated to have a range of 400V to 440V by controlling the output of PFC, as shown in Fig. 4.17(b).

Fig. 4.16. Transformer minimum loss vs. footprint under different $P_V$

(a) Fixed input voltage of 400V.  
(b) Variable input voltage of 400V to 440V.

Fig. 4.17. Output-to-input voltage gain of three-phase LLC converter.
Base on such a gain range, the parameters of LLC converter can be designed following the methodology in [10]. The simulated gain curves and operation range is shown in Fig. 4.18. The $L_m$ is selected to be 25uH and $L_r$ is selected to be 2.5uH. The full-load $f_S$ range for 40V to 60V output range is 0.7 to 1.5 times $f_o$. When the load is very light, it will require very high $f_S$ to get a low $V_o$. This is not desirable, but can be solved with burst mode [34].

![Fig. 4.18. Gain curves and operation range.](image)

After optimizing the transformer design, the width $b$ of magnetic structure and winding width $c$ are determined. Then the inductor can be optimized for certain $L_r$ value by sweeping inductor core leg length $a_l$. Then the inductor loss vs. footprint can be plotted as shown in Fig. 4.19.
Based on the proposed integrated magnetic structure and design methodology, the three-phase interleaved LLC converter is designed and the specifications are shown in Table 4.2. In this design, the air gap is around 0.2mm to achieve a magnetizing inductance of 25uH. The distance between the winding and the air gap is 5 times of the air gap length. So the fringing effect caused by the air gap is negligible in this case.

Table 4.2 Specifications of the Proposed Three-phase LLC Converter

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant Frequency</td>
<td>1MHz</td>
</tr>
<tr>
<td>Dead Time</td>
<td>60ns</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>4:1</td>
</tr>
<tr>
<td>Primary devices</td>
<td>PGA26E07BA</td>
</tr>
<tr>
<td>Secondary devices</td>
<td>ECP2029</td>
</tr>
<tr>
<td>Primary Driver</td>
<td>Si8273GBD</td>
</tr>
<tr>
<td>Secondary Drivers</td>
<td>LM5113</td>
</tr>
<tr>
<td>Resonant Capacitor</td>
<td>3nF</td>
</tr>
<tr>
<td>Resonant Inductance</td>
<td>2.5uH</td>
</tr>
<tr>
<td>Magnetizing Inductance</td>
<td>25uH</td>
</tr>
</tbody>
</table>
4.4. Experimental results

The 1MHz 3kW 400V/48V LLC converter prototype with the proposed integrated magnetic structure is shown in Fig. 4.20. It has a length of around 71mm, a width of around 55mm, and a height of less than 17.7mm. An output power of 3kW at such a dimension is equivalent to a power density of around 600W/inch$^3$.

(a) Prototype Without top magnetic plate.  
(b) Fully-assembled prototype.

Fig. 4.20. 1MHz 3kW 400V/48V LLC converter prototype.

The experimental waveforms of drain-source voltage for primary low-side switch of phase B $V_{ds,Q2B}$, drain-source voltage for one SR of phase B $V_{ds,SR2B}$, resonant current for three phases $i_{Lr_A}$, $i_{Lr_B}$, $i_{Lr_C}$, under full-load and light-load (20% load) conditions are shown in Fig. 4.21. Here, it shows that ZVS for both the primary and secondary switches under both full-load and light-load conditions can be achieved. Moreover, there is no ringing in the drain-source voltage for SR due to the minimum secondary leakage. The resonant current of three phases have almost identical shape, but with 120° phase shift.
The measured efficiency curve of the proposed three-phase interleaved LLC converter is shown in Fig. 4.22. The proposed LLC converter has a peak efficiency of 97.6%, a full-load efficiency of 97.2% and a light-load (10% load) efficiency of 93.0%.

Full-load loss breakdown for the proposed three-phase LLC converter has been made, as shown in Fig. 4.23.
4.5. Conclusions

The LLC converter is very popular as DC/DC converter in server and telecom applications due to its high efficiency and high power density. Three-phase interleaved LLC converter can have additional benefits of increased output power, reduced input and output current ripples, and automatic current sharing between phases. But three-phase LLC converter suffers from numerous magnetic components. By pushing switching frequency up to MHz with GaN devices, the size of magnetics can be significantly reduced. This paper proposes a novel magnetic structure that can integrate three inductors and three transformers into one magnetic core. Furthermore, all the magnetics can be implemented with 4-layer PCB winding under MHz switching frequency, and additional 2-layer shielding can be integrated to reduce CM noise. The proposed three-phase LLC converter employs delta-connected resonant capacitor network in primary side to achieve
automatic current sharing and full-bridge secondary side due to high-frequency operation. Design optimization process is also provided for the proposed magnetic structure.

The proposed three-phase interleaved LLC converter with integrated magnetics can demonstrate the impact of GaN in such important issues as efficiency, power density and manufacturability. With the academic contribution of this paper, we can design a converter with more than 10 times higher in switching frequency and power density, while at the same time maintaining a higher efficiency, compared to the current practice using silicon devices. A 1MHz 3kW 400V/48V three-phase LLC converter with proposed magnetic structure is designed, and a peak efficiency of 97.5% and power density of 600W/inch^3 are achieved.
Chapter 5. Conclusions and Future Work

5.1. Conclusions

With the fast development of information technology (IT) industry, the demand and market volume for off-line power supplies keeps increasing, especially those for desktop, flat-panel TV, telecommunication, computer server and datacenter. Isolated DC/DC converter is very critical for off-line power supplies and datacenter power architecture, since it occupies more than half of the volume in off-line power supplies and takes responsibility for most control functions. LLC resonant converter dominates the isolated DC/DC converter in IT industry. It has the advantages of ZVS for primary switching, low turn-off current, ZCS for SRs, and easy magnetic integration. Almost all the high-end off-line power supplies are using LLC converter as the isolated DC/DC converter.

But there are several challenges in the control and design of LLC converters. The control of LLC converter is very difficult due to the dynamics of resonant tank. Simplified optimal trajectory control (SOTC) is an effective method to control LLC converter, but it requires high-performance FPGA and analog controller. On the other hand, present LLC converter, operating at around 100kHz, has bulky and labor-intensive magnetic components. By pushing switching frequency higher, the LLC converter volume can be shrunk significantly and the magnetic can be integrated into PCB to achieve automatic manufacturing.

To achieve this goal, the dissertation proposes microcontroller (MCU) based SOTC for high-frequency LLC converters. The impact of digital delay on each control function is analyzed and methods to minimize the impact are proposed. By fully utilizing the controller resources, all the
required control functions can be integrated into a low-cost MCU, including: fast transient response, soft start-up and short-circuit protection, burst mode for light load efficiency improvement, and adaptive SR driving. The experimental results demonstrate significantly improved control performance for a 500kHz LLC converter with a 60MHz MCU.

By using GaN devices and novel magnetic materials to push the switching frequency much higher, the transformer can be integrated into PCB winding. But for high-output-current applications, either PCB with a large number of layers or multiple cores should be employed to handle large output current. This dissertation proposes an integrated matrix transformer structure to integrated four elemental transformers into one magnetic core with four-layer PCB windings, and a novel shielding technique to reduce CM noise and improve efficiency by inserting additional two shielding layers. An optimal design methodology and CM noise model are also provided. A 1MHz 800W 400V/12V LLC converter prototype with the proposed design has been demonstrated: the peak efficiency is 97.7%, which is close to or even higher than the best commercial products, and the power density is 900W/\text{inch}^3, which is ten times higher than the state-of-art designs.

To further improve the LLC converter, three-phase interleaved LLC converter can be employed to reduce the inherent circulating energy in the resonant tank, as well as conduction losses, by connecting the three phases in certain way. Furthermore, three-phase LLC converter increases output power and reduces input and output current ripples. This dissertation proposes a novel integrated magnetic structure along with its optimization methodology, to integrated three inductors and three transformers into one magnetic core with four-layer PCB winding and two-layer shielding. A 1MHz 3kW 400V/48V LLC converter prototype with the proposed design has been demonstrated: the power density is 600W/\text{inch}^3, which is much higher than the state-of-art designs, the peak efficiency is 97.5%, which is very good but can be further improved.
In today’s power electronics products, quality and reliability are given. Great emphases are placed on high efficiency, high power density and low cost. Present LLC converter designs, operating at around 100kHz, suffer from complex control system with poor dynamics, bulky magnetics with labor-intensive contents, and large volume with inferior efficiency. Pushing switching frequency much higher with GaN devices is an effective way to reduce the volume and cost, but it is very challenging to handle the control and magnetic components.

With the academic contributions in this dissertation, the control system can be simplified into a low-cost MCU based digital control system with significantly improved transient behavior; the volume of magnetic components can be reduced significantly and further integrated into PCB winding; the circulating energy, and input and output current ripples can be reduced with three-phase interleaved LLC converter, which requires only one magnetic component by using the proposed structure. Issues related to control, efficiency, power density, cost, reliability and manufacturability of high-frequency LLC converter are all addressed properly in this dissertation.

5.2. Future Work

This dissertation analyzes the MCU based SOTC control for high-frequency LLC converters with a resonant frequency up to 500kHz. Although methods to increase the switching frequency limitation have been provided, further efforts need to be spend on trade off between converter switching frequency and transient behavior for given MCU. On the other hand, this dissertation uses the low-cost MCU to demonstrate the proposed SOTC control, but how to select proper controller for given transient requirement has not been investigated.

Since most off-line power supplies in IT industries are only required to provide a small output voltage range, this dissertation optimizes LLC converter for given operating point. But for
application that requires battery to be connected directly to the input or output of LLC converter, such as telecom or electric vehicles, the LLC converter should be able to operate at a wide input or output voltage range to cover the battery voltage range. Further efforts need to be spend on investigating how to optimize LLC converter design for a wide operation range.

On the other hand, since the switching frequency of LLC converter is modulated to change the input to output gain, the switching frequency range may be very wide if the required gain range is wide, especially under light load condition. This brings challenges related to control and magnetic design if the maximum switching frequency is very high. There have been some control methods to reduce the switching frequency range, but they all suffers from extra components and efficiency drop. How to get a wide gain range under a narrow switching frequency range should be investigated for these applications.

The three-phase LLC converter has the benefits of reduced circulating energy and magnetic integration with the proposed structure, but the control for three-phase LLC converter has not been investigated yet. It is meaningful to investigate how to analyze three-phase LLC converter with state-plane, and how to control three-phase LLC converter to achieve fast transient response, soft start-up and burst mode for light load efficiency improvement.
Reference


