Switching-Cycle Control and Sensing Techniques for High-Density SiC-Based Modular Converters

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ABSTRACT

Nowadays high power density has become an emerging need for the medium-voltage (MV) high-power converters in applications of power distribution systems in urban areas and transportation carriers like ship, airplane, and so forth. The limited footprint or space resource cost such immensely high price that introducing expensive advanced equipment to save space becomes a cost-effective option. To this end, replacing conventional Si IGBT with the superior SiC MOSFET to elevate the power density of MV modular converters has been defined as the concentration of this research work.

As the modular multilevel converter (MMC) is the most typical modular converter for high power applications, the research topic is narrowed down to study the SiC MOSFET-based MMC. Fundamentals of the MMC is firstly investigated by introducing a proposed state-space switching model, followed by unveiling all possible operation scenarios of the MMC. The lower-frequency energy fluctuation

on passive components of the MMC is interpreted and prior-art approaches to overcome it are presented.

By scrutinizing the converter's switching states, a new switching-cycle control (SCC) approach is proposed to balance the capacitor energy within one switching cycle is explored. An open-loop model-predictive method is leveraged to study the behavior of the SCC, and then a hybrid-current-mode (HCM) approach to realize the closed-loop SCC on hardware is proposed and verified in simulation.

In order to achieve the hybrid-current-mode SCC (HCM-SCC), a high-performance Rogowski switch-current sensor (RSCS) is proposed and developed. As sensing the switching current is a critical necessity for HCM-SCC, the RSCS is designed to meet all the requirement for the control purposes. A PCB-embedded shielding design is proposed to improve the sensor accuracy under high dv/dt noises caused by the rapid switching transients of SiC MOSFET.

The overall system and control validations have been conducted on a high-power MMC prototype. The basic unit of the MMC prototype is a SiC Power Electronics Building Block (PEBB) rated at 1 kV DC bus voltage. Owing to the proposed SCC, the PEBB development has achieved high power density with considerable reduction of passive component size. Finally, experimental results exhibit the excellent performance of the RSCS and the HCM-SCC.

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GENERAL AUDIENCE ABSTRACT

Electricity is the fastest-growing type of end-use energy consumption in the world, and its generation and usage trends are changing. Hence, the power electronics that control the flow and conversion of electrical energy are an important research area. As a typical example, the modular multilevel converter (MMC) is a popular voltage-source converter for high-voltage dc electric transmission systems (VSC-HVDC). The MMC features in excellent voltage scalability that fits various HVDC transmission projects. Though, the huge passive energy storage components of the MMC remains a hurdle to improve its power density.

On the other hand, wide-bandgap (WBG) power semiconductors are enabling power electronics to meet higher power density and efficiency, and have thus begun appearing in commercial products, such as traction and solar inverters. Silicon-carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET), as one type of WBG devices, is able to switch higher voltages faster and with lower losses than existing semiconductor technologies will drastically reduce the size,

weight, and complexity of medium-voltage and high-voltage systems. However, these devices also bring new challenges for designers.

The objective of this research work is to develop a new control approach that takes advantage of the merits of the SiC MOSFET to reduce the passive components of the MMC. In order to achieve that, a switching-state model of the MMC, a closed-loop hybrid-current-mode switching-cycle control (HCM-SCC) method, a Rogowski switch-current sensor (RSCS), and a SiC-based power electronics building block (PEBB) have been developed. Analytical and experimental results show that the new control approach is able to reduce the capacitance by 93%, inductance by 74%, and semiconductor losses by 11% at the same time, and thus to improve the power density of the MMC power stage by a factor of 23X.

To My Grandfather:

Tingliang Guan

For his inspiration

Also to My Parents:

My father: Feiyue Wang
My mother: Xuejuan Guan

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Chapter.1 Introduction

1.1 Background

Power electronics building blocks (PEBB), as a least replaceable unit (LRU) to construct modular converters, was originally proposed by the Office of Naval Research in 1997 [A.1] . A PEBB was defined as a universal power processor and a systematic approach, featuring modular configurations, scalable voltage, and current ratings, as well as low inventory and maintenance cost [A.2] -[A.4] . The converters that are constructed by PEBBs are termed modular converters. In the past two decades, numerous commercial modular converter products in medium-voltage (MV) and high-voltage (HV) applications have been developed [A.5] -[A.8] , adopting PEBB-based power stage architecture. Those PEBBs are connected in series, parallel, or multi-phase configurations to scale up the voltage or current ratings of modular converters.

A major part of modular converters is multilevel converters. They were invented to realize MV and HV power conversion where the DC bus voltage is multiple times higher than the limited device voltage ratings, while direct stacking devices are intentionally avoided [A.9] [A.10] . Typical commercial multilevel topologies include neutral-point clamped 3-level (NPC-3L) [A.9], flying capacitors (FC) [A.9], active neutral-point clamped 5-level (ANPC-5L) [A.8] , cascaded H-bridge (CHB) for motor drives [A.11] and

for static synchronous compensators (STATCOM) [A.12] , and the modular multilevel converters (MMC) [A.13] .

The PEBB unit of an NPC-3L modular converter is a phase leg of NPC-3L, and the PEBB for ANPC-5L and FC topologies are usually configured the same way. In this setting, a DC source generated by the front end of the converter feeds those PEBBs at their DC terminals via a DC-link bus [A.10] . The AC terminals of the PEBBs can be paralleled or interleaved to extend the converter output current capability by single-, three- or multi-phase [A.14] configurations. The PEBB unit of a CHB modular converter is typically an H-bridge. For active power processing such as motor drive applications, each PEBB requires a DC source supplied by a multi-pulse transformer and corresponding rectifiers. The transformer has a maximum secondary winding number constrained by manufacturing techniques. Therefore, in higher voltage applications where more voltage levels are needed, the cascaded H-bridge can be replaced by a cascaded NPC-3L, FC, or other multilevel topologies. On the other hand, for reactive power processing, the DC sources for PEBBs are dispensable such as a STATCOM.

The abovementioned multilevel converters cannot process active power unless separated DC sources are fed to their PEBBs, which are actually generated by certain transformers or isolated power supplies that have limited voltage ratings. As a result, the scalability of those multilevel converters is limited. Nonetheless, the MMC PEBBs do not rely on separated DC sources at their DC terminals to enable active power processing. This feature enables MMC to have nearly unlimited scalability by stacking PEBBs. To this end,

the MMC converter has been used in voltage source converter (VSC)-based high-voltage direct current (HVDC) transmission station in recent years. In 2014, the world-first multi-terminal HVDC scheme entered in service, built from Barkeryd to Hurva in southern Sweden by Alstom. This particular HVDC scheme consists of two parallel links, each of 720 MW capacity, operating at a DC voltage of ±300 kV, with more than 300 IGBT-based PEBBs in series [A.15] . MMC's complete modularity and scalability has drawn a huge attention from both the academia and the industry and became one of the hottest research topics in the past 10 years. Researchers would like to explore the inherent essence of this topology and how it can be applied in the fields other than HVDC transmission links. [A.16] compares the CHB, ANPC-5L, and MMC for motor drives rated at 4.16-13.8 kV voltage range, concluding that the MMC has high efficiency and is a good fit for the fan, blower, and pump drives. Siemens has developed induction machine drive product SINAMICS SM120 CM based on Si IGBT and the MMC topology, rated at 3.3-7.2 kV and 4-13.3 MVA [A.17] .

Today, the necessity for higher power density and lower weight is increasing rapidly. Typical MV applications for high power density include motor drive for underground mining, medium voltage direct current (MVDC) distribution system in an urban area [A.18] and electrical ships [A.19] , and MV wind turbine converters [A.20] . All of them share a common feature of the extremely high cost of footprint or space. If the advancement of new technologies is able to elevate the power density of the converters in those applications, the deducted cost for system accommodation is much higher than the incremental cost of more advanced equipment. For instance, if the land cost density is more

than \$10,000 USD/m^2, and the advanced semiconductor device brings an incremental cost density \$4,000 USD/m^2 compared to the conventional one while reducing the converter size by half at the same power rating. Then the total cost can be saved by 30% for a converter footprint reduction from 10 m^2 to 5 m^2. In the history, the power density improvement was usually brought by the commercialization of superior power semiconductor devices, and recently the booming wide-bandgap (WBG) semiconductor devices that are leading a power-density evolution. In consequence, it can be foreseen that SiC MOSFET, as one type of MV WBG devices, is a promising cost-effective alternative to replace Si IGBTs in MV limited-space applications.

SiC MOSFETs with the same ratings are able to switch more than 5x faster switching speed and consume 5x less switching loss than the Si IGBTs at similar ratings. Theoretically, the passive capacitor and inductor sizes can be reduced to 1/5 of original values, but unfortunately, this can scarcely happen because of two major obstacles. First, for certain converter topologies (e.g. single-phase inverter/rectifier) the energy storage in passive components is determined by the fundamental frequency and its harmonics, other than the switching frequency. Increasing switching frequency contributes very little to the passive component size reduction. Second, the device switching losses are scaled up with the switching frequency, so the thermal limit does not allow the SiC MOSFETs to really switch 10x more frequently than Si IGBT.

According to all the analysis above, research on the SiC MOSFET-based MMC converter was selected as the major concentration of this dissertation. The objective is to

investigate and tackle the major problems that a SiC MOSFET-based MMC has, aiming to take good advantage of SiC MOSFETs and to really boost the power density of the MMC by a large scale in MV limited-space applications. In order to better understand the nature of the MMC converter topology, a literature review of the modeling, modulation and control of the MMC has been conducted. The review summarizes the fundamentals and limitations of the MMC topology, and also reveals major problems and existing solutions.

1.2 Review of the Modular Multilevel Converter

The circuit diagram of the MMC is shown in **Figure 1-1**. It was originally developed for HVDC transmission and currently has been increasingly considered for MV industrial and grid applications owing to its great features of high modularity, good voltage scalability, and the capability to operate in a direct-to-line mode without a dedicated transformer [A.13] [A.21] -[A.23] . The topology of the MMC has been modified since its invention. The original version comprises half-bridge modules without inductors in the phase-leg arms [A.13] . It is able to output sinusoidal voltage with low total harmonic distortion by using the appropriate control approach. However, the inrush currents in arms were significant during transient when switching the modules. To resolve this problem, additional inductors are inserted in series with the modules on each arm [A.24] , which provided the MMC with the capability to limit and control the arm currents.

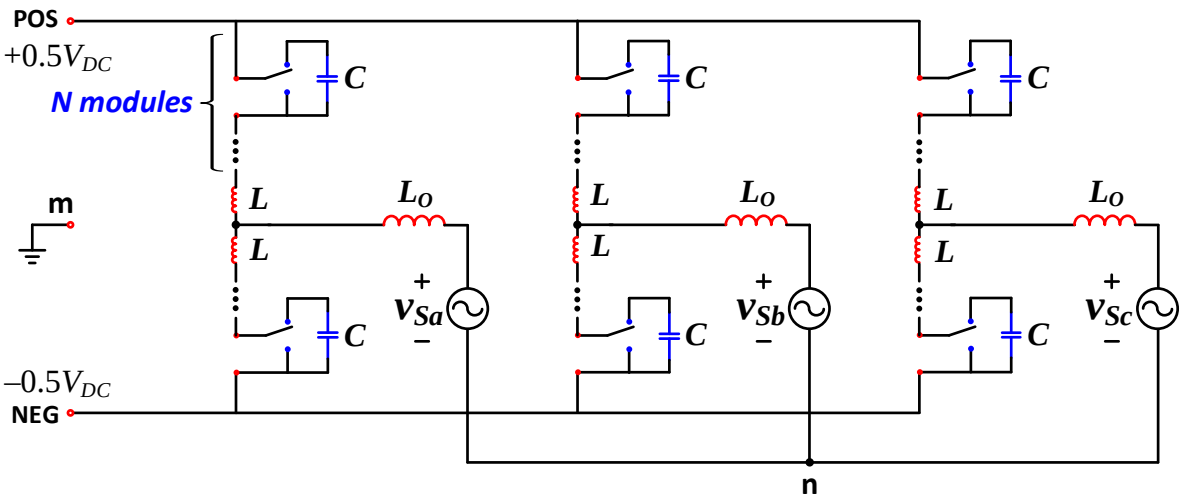


Figure 1-1 Circuit topology of the modular multilevel converter (MMC)

1.2.1 Review of MMC Modeling

Because of the absence of arm inductors and module capacitors being treated as selectable DC sources [A.13] [A.21] [A.22] , the voltage from the phase to the DC mid-point is assumed as a controlled voltage source as shown in **Figure 1-2**. The arm voltages are in the shape of staircases that consist of a DC component, a sinusoidal component at the fundamental frequency and its harmonics. If the number of modules is as large as 300, for instance, the high-frequency harmonics will be trivial. Hence, it can be assumed that the arm voltages are composed of a fixed DC-component and a sinusoidal component controlled by the duty cycles.

Later, in order to control and limit the arm current, an inductor is inserted into each arm in series with the modules [A.24] . This modification in the circuit also changes the MMC's model as shown in **Figure 1-3** where the terminal voltage of the series-connected modules are still regarded as a controlled voltage source [A.25] -[A.30] . The above two models are only valid on the basis of two assumptions. Firstly, the capacitance in each module is large enough to emulate a DC voltage source. Secondly, the number of modules needs to be large enough so that the harmonics components of the controlled voltage source can be regarded as trivial.

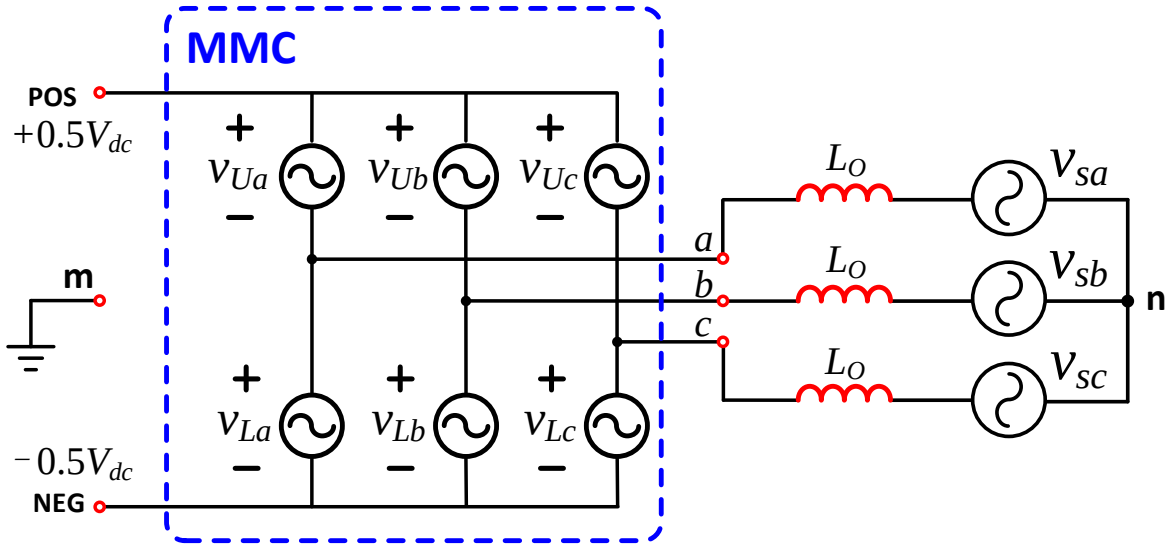


Figure 1-2 Original equivalent circuit

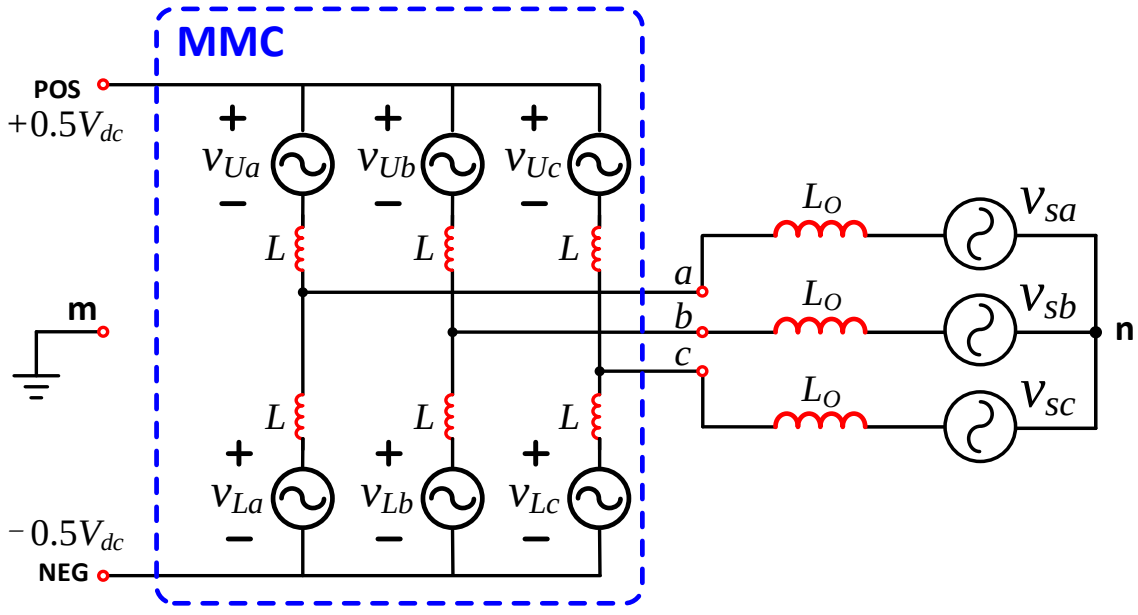


Figure 1-3 Equivalent circuit including arm inductors

Although these two models are very straightforward and easy to use in controller design, nevertheless, they still contain drawbacks and limitations. First, all modules have to be treated as one in the model, and then the terminal behaviors of a single module are veiled. Secondly, only line frequency behavior can be derived using the model, which means the explicit expression for the phenomena such as circulating current cannot be derived. Thirdly, the capacitor dynamics and their coupling effects to arm current are lost. Finally, other possible operation modes cannot be observed in this model.

Another model shown in **Figure 1-4** is analogous to the previous one. The difference lies in the assumption that this model regards each arm as a nonlinear capacitor with time-variant sinusoidal capacitance, while the capacitor voltages are still controlled voltage sources. In dealing with the dynamics of the capacitors in this model, total capacitor energy in one arm is usually calculated to control the arm capacitor voltage. The sum energy of the upper and lower arm is regulated to control the power delivery to load, whereas the difference in energy between them is controlled to balance the voltage between the upper and lower arms, respectively [A.31] -[A.34] . The expression for the total capacitor ripple can be derived in this model [A.38] [A.39] .

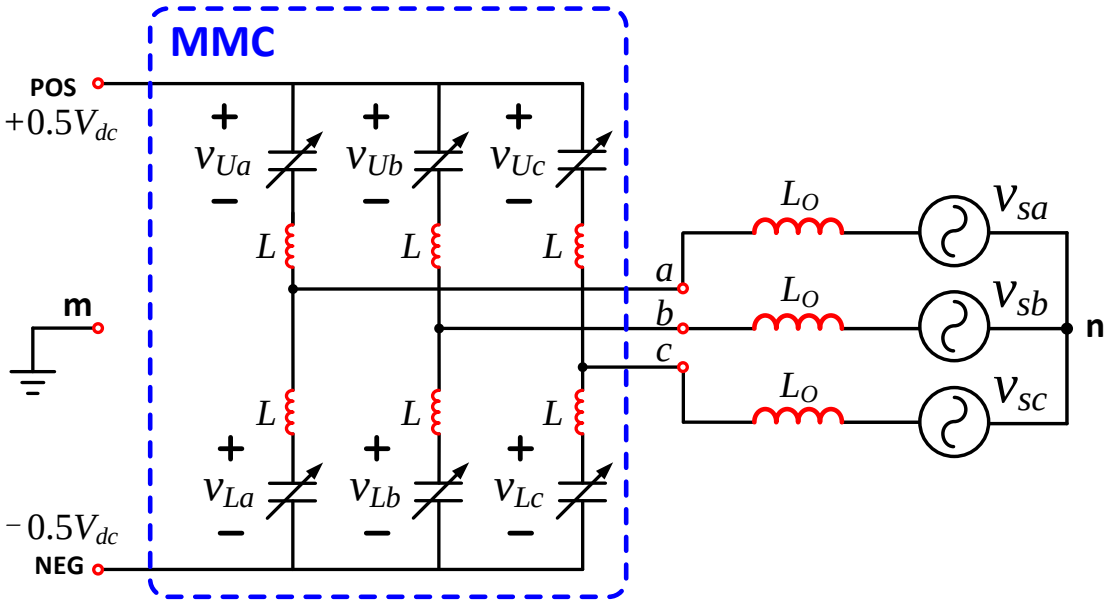


Figure 1-4 Equivalent circuits with nonlinear arm capacitors

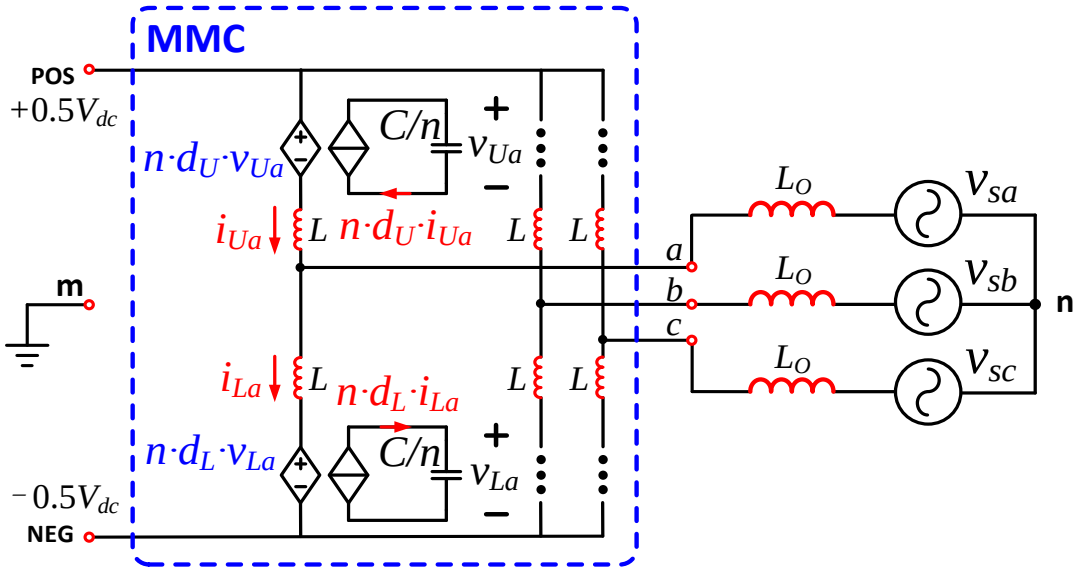


Figure 1-5 Equivalent circuits of averaged PWM-switch model

Recently, various pulse-width modulation approaches were implemented on the MMC, and thus the modules operated at a switching frequency much higher than the line frequency. In this manner, the MMC's model can be refined to be more accurate to an averaged PWM-switch model [A.35] -[A.37] . Due to the identical duty cycle references for all the modules in the same arm, they have the same coefficient of the controlled sources after averaging the switching frequency components. In this case, they will be equivalent to one single module as shown in **Figure 1-5**. The explicit expression for the circulating current [A.40] can be derived in this model.

Compared to the previous three models, this model includes additional information on single capacitors provided that the switching frequency is high enough for the equivalency of averaging and that all the module parameters and modulation commands are the same to every module. One limitation of the PWM-switch model is that the voltage and current behaviors of an individual module cannot be differentiated from the others in the given model as all of them appear to be identical. The other is that the circuit behaviors at switching frequency are still hidden.

On the basis of the averaged PWM-switch model, a further simplification has been made to obtain a three-phase coupling model in [A.41] [A.42] , shown in **Figure 1-6**. This model facilitates the prediction on dynamic characteristics like transfer function and input impedance by circuit derivation. The accuracy in estimating the small-signal DC-terminal impedance of the MMC turns out to be well presented in [A.41] . This model analyzes the effects of the DC and AC components of the duty cycle, illustrating that the DC component

transfers energy from/to the DC terminal to/from module capacitors, whereas the latter transfers energy from/to module capacitors to/from the AC terminal. In addition to the presumptions made in the model of **Figure 1-6**, this model further assumes that all the module capacitors in all the arms share the identical steady-state and dynamic behaviors. Similar to other models, this model is also limited to observing the real performance of a capacitor in each individual module and exploring other possible operation modes.

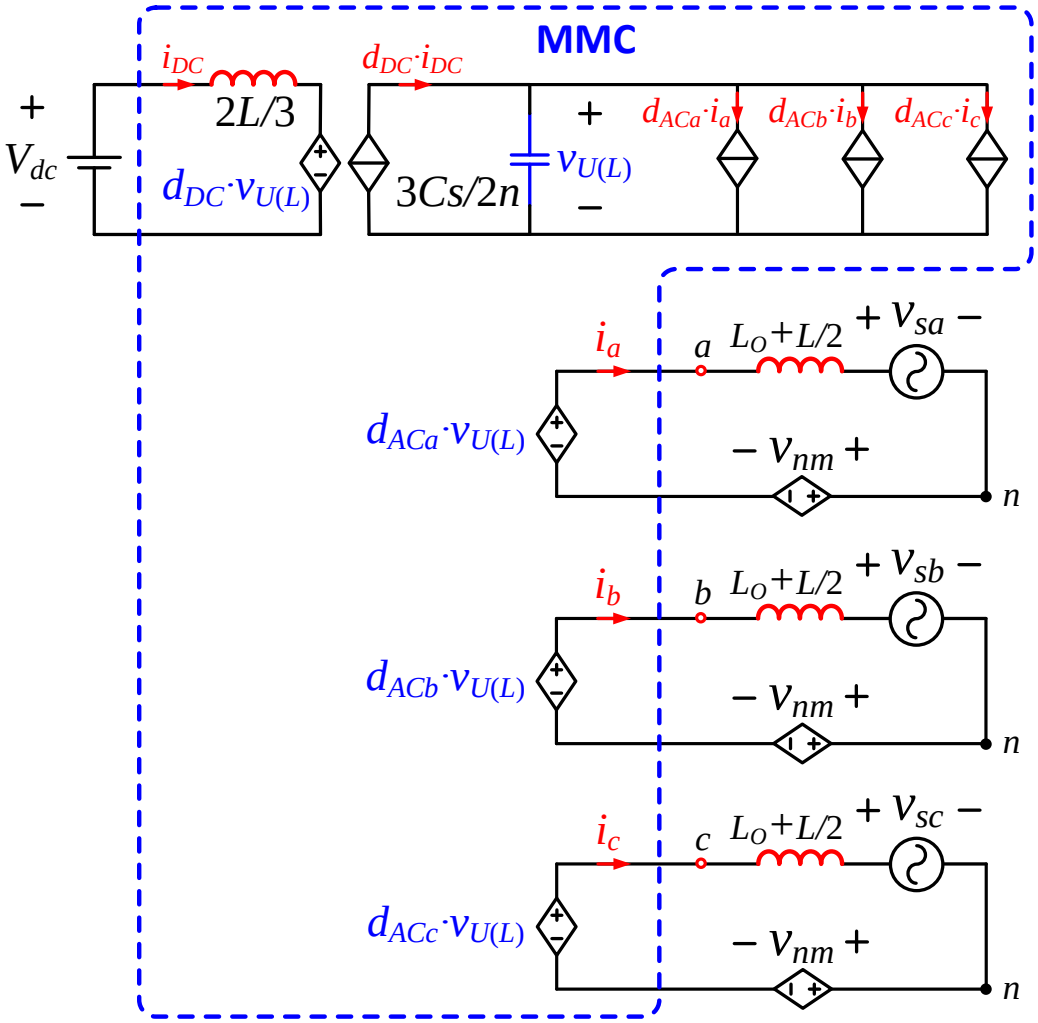


Figure 1-6 Equivalent circuit with nonlinear arm capacitors

Since all the above-mentioned models are averaged to be analyzed based on the DC or sinusoidal components in the time domain, naturally, all those components can also be transformed to the frequency domain to obtain a phasor model for the MMC. From the state-space equations point of view, [A.43] demonstrates how to use the Fourier series to get the dynamic phasor model of the MMC from a time domain state-space model. From the equivalent circuit perspective, [A.36] presents the AC and DC controlled sources for an average PWM-switch model in **Figure 1-5**. Notice that in any kind of phasor model of the MMC, the high order frequency components are omitted for the sake of simplicity.

State-space equations can be derived corresponding to all the aforementioned models, holding the difference in the selection of state variables. For the original model in **Figure 1-2**, there are five independent loops in the circuit but it has only three phase inductors that can be designated as state variables. This implies that only three KVL loops are valid for the state-space model of the equivalent circuit, and the two arm voltage sources in each phase-leg are independent of each other. No state-space model has been established so far for this circuit model as it is too ideal to be of practical value.

For the circuit model in **Figure 1-3**, there are totally nine inductors that can be chosen as state variables of a circuit with five independent loops. Therefore, the selection of states can be tricky in controlling the MMC. In [A.44] , four arm currents and one DC current are selected to be state variables, which is ambiguous for converter control because the arm currents are not the states that need to be controlled directly. Since there are no capacitors in the equivalent circuit, the coupling between the inductor currents and

capacitor voltages cannot be presented by the state-space equations. Therefore, it is not possible to control the capacitor voltage in the circuit precisely and it's inaccurate for the current control. Later in [A.30] [A.45] , the expression of the phase current, DC current and circulating current are derived such that the characteristics of the featured current variables of the MMC are illustrated with respect to the controlled voltage sources. By sharing the same problem with [A.44] -- losing the capacitor information, the state-space model in [A.30] [A.45] is still limited in controlling the capacitor voltage and inductor current.

For the circuit model in **Figure 1-4**, the time-variant capacitance of module capacitors vastly complicates the state-space model, and the linear system theory is not even applicable. Therefore, the stored capacitor energy instead of its voltage, is usually used to control the capacitor voltage indirectly [A.41] -[A.44] . For the circuit model in **Figure 1-5**, capacitor voltages are the states in the state-space model so that their dynamics and coupling effect to inductor currents can be analyzed, although the equivalent single capacitor cannot represent the behavior of all capacitors in the arm. However, selecting the arm current to be states has the same problem as [A.44] which was previously discussed. For the circuit model in **Figure 1-6**, further assumptions are made so that in the state-space model there is only one equation for capacitor voltage reflecting total capacitor characteristics. The model also reduces the number of current states to four.

All the above state-space models are average models based on various assumptions. A state-space switching model has been built for the MMC [A.46] . Similarly, since it is

the five arm currents that are selected to be current state variables, the model is too ambiguous for the analysis of the circuital behavior and the control.

1.2.2 Review of MMC Modulation

(a) Space-Vector Modulation (SVM)

In the first paper where the SVM was mentioned to be a possible modulation scheme [A.13] . But in later high voltage applications, the MMC consists of too many modules to be modulated by SVM because of the complex vector calculation and selection, for instance as many as 200 in HVDC application. Therefore, the staircase modulation and PWM modulations are implemented in practical applications.

(b) Staircase Modulation

In staircase modulation that renders low switching frequencies, the power devices generally switch on and off twice during one cycle of line voltage, to minimize the switching losses in high power applications. Then a staircase waveform will be generated, following a sinusoidal envelope [A.47] . As long as the staircase pattern is determined, the way to shape the pattern by switching the modules can simply follow the description in [A.48] .

There are two ways to calculate the switching time and level to form a staircase pattern in the staircase modulation, the selective harmonic elimination modulation, and nearest level modulation. In [A.25] the staircase modulation with selective harmonic elimination pulse-width modulation (SHEPWM) technique is suggested to be used for the MMC modulation. The switching angles of all steps of the staircase are calculated by

solving the harmonic equations with associated modulation index and harmonic elimination requirement. By this approach, lower order harmonics which have relatively high magnitudes can be eliminated, and hence the total harmonic distortion (THD) of the AC voltage of the MMC is reduced. Normally the switching angle tables are pre-calculated and stored in the memory off-line to save the computation resources, but both of the number and scale of the tables will be too large when it comes to hundreds of voltage levels and a wide range of modulation indexes.

It is not realizable to calculation the switching angles for every modulation indexes in advance. The switching tables can only be calculated for limited numbers of modulation indexes, such that the THD may not be optimized for certain operation voltage. Therefore, an on-line switching-angles calculator is proposed for the MMC modulation [A.49] . In this technique, reducing the THD of the voltage is targeted through the instantaneous comparison between the pure-sinusoidal voltage reference and the voltage signal synthesized using Fourier analysis. The error from the comparison is used to update the switching angles in the direction for the error to be eliminated using the least-mean-squares method [A.49] . But this approach is still complicated for a large number of voltage levels.

Compared to the SHE technique, the nearest level modulation (NLM) is much simpler and more applicable for the applications with large amount of modules, which simply selects the output voltage level nearest to the reference. To obtain the switching patterns the voltage reference is multiplied by the number of positive voltage levels n, then apply the round function to find the required output voltage level [A.50] . The relationship

between the THD and sampling frequency, number of modules and the modulation index value can be found in [A.51] .

(c) Carrier-Based Pulse-Width Modulation (CBPWM)

Because of the approximation nature of round function used in nearest level modulation, the voltage level selection at each sampling period always contains error. To address this problem, a modulation approach based on the nearest level modulation is proposed to achieve a PWM pattern without carriers [A.52] . Only one module is operating at PWM mode in each switching cycle and then the average value of the AC voltage will be equal to that of the reference at this switching cycle. This approach reduces the THD at the cost of a little more switching losses, which is quite effective when the module number is relatively low.

Traditional level-shifted and phase-shifted multicarrier based PWM which are widely used in other multilevel converters can be applied as well in the modulation of the MMC, shown in **Figure 1-7**. In [A.53] , implementation and harmonic comparisons of those PWM modulations have been elaborated in details and all the associated waveforms are given. The phase-shifted PWM turns out to have the lowest THD but the most switching events, namely the highest switching losses.

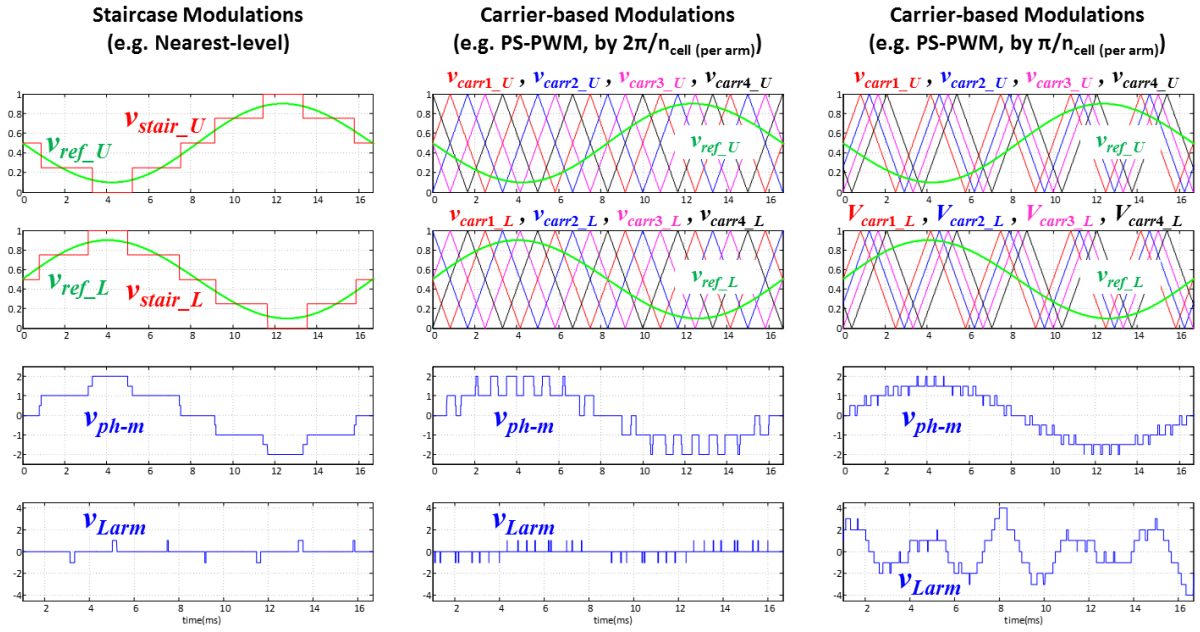


Figure 1-7 Different types of modulations

1.2.3 Review of MMC Control

(a) The balancing controls of capacitor voltages in arm

The cause of the voltage imbalance between modules is fundamentally the charge imbalance due to different current value and time duration when the capacitor of an on-state module is conducting [A.13] . In order to achieve module voltage balance, the specific balancing approaches are different for various modulation techniques.

For the staircase modulation, all the modules in one arm are equivalent to each other, so any module can be selected to be inserted to form a specific voltage level. This feature renders two criteria to select the ON-state modules of each arm: 1) capacitor voltages and 2) sign of the arm currents [A.52] . The basic solution, named sorting algorithm, is to insert the module with lowest average capacitor voltages in ascending order into the arm when the arm current is charging the capacitors, and conversely, to insert the module with highest average capacitor voltages in descending order into the arm when the arm current is discharging the capacitors [A.13] . A balance can be achieved within a line cycle using this approach. If one module works in PWM mode without carriers as suggested in [A.52] , this PWM module is defined as the module in ascending order following those ON-state modules when the arm current is charging the capacitors. And reversely, this PWM module is defined as the module in descending order following those ON-state modules when the arm current is discharging the capacitors.

Based on the above-mentioned sorting algorithm, an optimized capacitor voltage balancing control is proposed in [A.48] to avoid unnecessary switching actions, thus to

reduce switching losses. The method is to set up overvoltage and under-voltage thresholds and to change the states of modules that are over the threshold while maintaining the states of modules within the threshold to reduce switching actions. It is realized by adjusting the measured module capacitor voltages before the sorting process.

For the level-shifted carrier based PWM, the trigger signals generated by the comparison between the modulation reference and the multi-carriers need to be sorted before given to the device gates [A.54] . As long as the modulator generates the voltage level reference, the same sorting approaches can be applied as mentioned in using staircase modulation.

For the phase-shifted carrier based PWM, all the modules are basically self-contained and balanced in line period. But due to the parameter variation and signal delays the module voltage imbalance still exists in practical applications. The soring algorithm is still applicable following the same idea as the level-shifted case, that is, to sort the modules after the voltage level references are generated [A.55] . This method is even extended to other modular multilevel converters with module topologies as 3L-NPC, 3L-FC, 3L-NPP, and so forth [A.56] . It is noticed that all the aforementioned voltage balancing control approaches are based on a centralized control system. For distributed control system, the closed-loop control on capacitor voltage which slight adjust the modulation index for individual modules is applicable only for the phase-shifted carrier based PWM [A.57] - [A.59] .

(b) The controls of circulating current

The circulating currents are the currents that flow only in between phase-legs, without flowing to DC or AC terminals. They are induced by harmonic ripples on module capacitors [A.60] , and is mathematically proved to contain only even order harmonics [A.61] . Circulating currents can bring about additional conduction loss and instability risks, so it should be well suppressed or controlled depending on application purposes. The steady-state expression of the circulating currents are derived in [A.40] [A.60] based on the parameters of the converter, which can be used for arm inductor design and variable frequency analysis.

In [A.60] the closed-loop control of circulating current in d-q frame is proposed. Additional three-phase 2nd-order harmonic voltages obtained from a closed-loop PI controller are added to the arm voltage commands to compensate the 2nd-order harmonic voltage ripple on the module capacitors. Similar approach using PI controller in abc coordinates is carried out in [A.62] . To better counteract the other even order harmonics in the circulating current, a P & PR controller is proposed in [A.63] , which largely increase the open-loop gain at even order harmonic frequencies to minimize the magnitudes of those harmonic components. Differed from the abovementioned approaches in manipulating the arm voltage commands, an approach to generate 2nd-order harmonic by adjusting the pulse width in SHE staircase modulation is proposed in [A.61] , where a PI controller is also used.

(c) The converter control

The control algorithms of the MMC varies from one application to another, however, basically the phase current or voltage control of it does not differ a lot from that of the regular VSI. One type of control solution is introduced in [A.31] to control the arm energy. In [A.57] [A.64] -[A.67] , Akagi gives the control algorithms in application of STATCOM and motor drive [A.38] .

Summarizing the control approaches in most of papers, the basic control diagram is shown in **Figure 1-9**. The decoupled voltage or current controller is used for regular three-phase AC/DC or DC/AC control in d-q coordinates. The circulating current controller is used to minimize the amplitude of 2nd order harmonic in normal operation to decrease the conduction loss. Both of the output of the two controller works together to generate the output voltage command. Knowing that the capacitor voltage balancing algorithm has to be implemented phase by phase because the MMC is intrinsically a single-phase converter, the voltage command is transformed back to abc frame. Finally with appropriate modulation approach described in Section III, the outputs with closed-loop control are obtained.

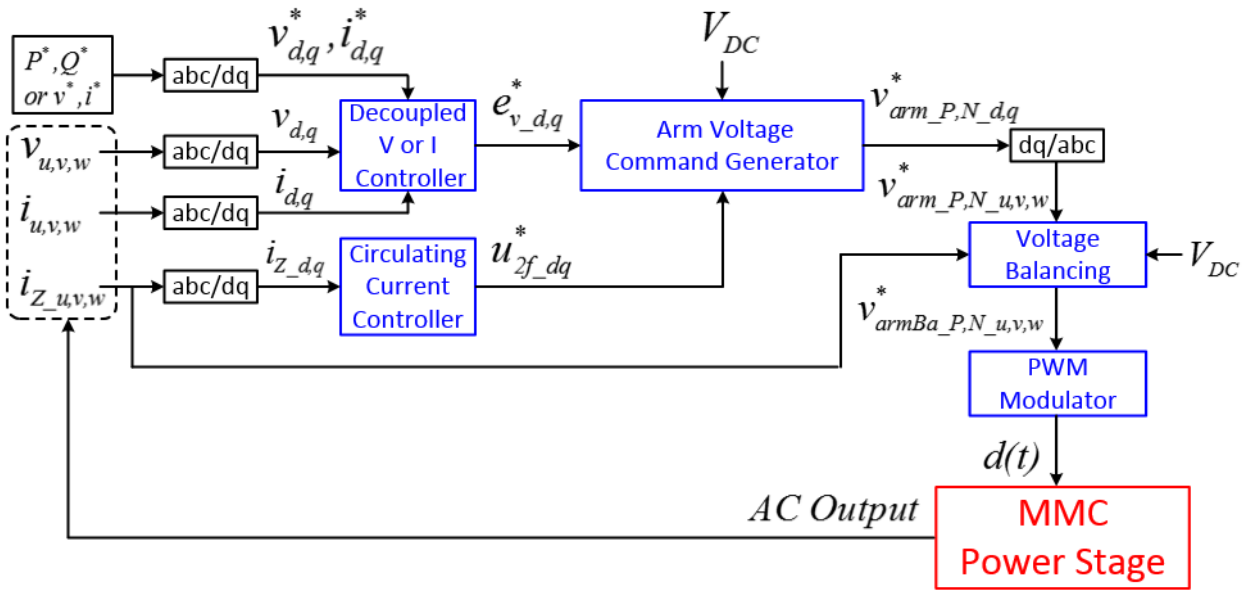


Figure 1-8 Control diagram of MMC

A comparison between four different types of control algorithm in the same application has been made in [A.67] . The features that are considered in trade-off include: the dynamic performance, the complexity of hardware, and the consumed communication resources. A closed-loop control with open-loop balancing is verified to have the fair performance by occupying smallest resources among the four.

As the MMC is essentially a single-phase converter, there will be fundamental or harmonic currents flowing through the module capacitors which bring about the capacitor ripple voltages. The analytic formulas between the capacitor ripple voltages, line frequency and load currents indicate that the ripple voltages are proportional to load current and inversely proportional to the line frequency [A.38] . Accordingly, this ripple voltages are comparatively much larger than that in the three-phase converter which force the MMC to be designed with much larger module capacitance to meet the ripple ratio requirement at rated frequency operations. Furthermore, in variable frequency motor drive applications where the operation frequency is varying from 50/60Hz to 0Hz, the capacitor ripple voltage will be tremendously increased which both the capacitor and the power devices cannot withstand. This phenomenon becomes worst for the constant load applications where the load current is still high for lower frequency operations. Conclusively speaking, the described feature of the MMC makes the converter operated with large capacitance, and prevents it from being applied in variable frequency applications.

Korn proposed a way to modulate the arm current by injecting high frequency circulating current and common mode voltage [A.69] [A.70] . In this paper, the capacitor

margin is maintained sufficient in a so-called “low frequency mode” that is activated when the line frequency is below 0.3 p.u. The penalty of this approach is that the arm current is very high such that the conduction loss of switching devices is vastly increased. Antonopoulos has similar conclusions on this type of approach, and also shows a constant full torque operation of driving a motor with MMC from zero to rated speed by means of sectional control strategy [A.71] . In those conditions when the capacitor voltage ripple is largely increased, Ilves proposed a way to align the peak of capacitor ripple with the peak of applicable voltage limit, by injecting circulating current with calculated amplitude and phase-shift [A.72] .

1.2.4 Summary of the Review

The-state-of-art MMC models are categorized on the basis of different assumptions and simplification. Most of these models are steady-state, whether sinusoidal or phasor-based, or are assumed that the module capacitors are DC voltage sources. Some models based on switching functions are transformed into average models immediately, thus the intrinsic nature of the converter might not be fully understood. Those average models show their simplicity and effectiveness in the averaged control and balancing loop design within the scope defined in the literature. However, the fundamental circuit behavior cannot be easily observed to the extent that possible operating modes could easily be veiled, and other effects such as the coupling between arm inductors and module capacitors are lost. The other switching models not selecting appropriate state variables still offer very limited help with interpreting the behaviors of the MMC. To this end, in Chapter 2, a state-space

switching model for MMC that is derived mathematically without any assumptions made from other previous models is proposed, which enables the observation on the circuit behaviors from a fundamental point of view.

Regarding the MMC modulation approaches, almost all the conventional modulation methods for multilevel converters can be applied to each of the MMC PEBBs. Except for the SHPWM, all the other modulation methods are carrier-based and the device switching events are determined by the comparison between the carriers and the generated modulation references. To some extent, those modulation methods limit possible operation modes of the MMC. In Chapter 3, the peak-current mode control that use the device peak current to determine the switching event has been proposed. This approach is applied to realize the switching-cycle control proposed in the same chapter.

In terms of the MMC control approaches, most of the prior-art efforts focus on the capacitor voltage balancing and circulating current control. The essence of the previous control proposals is to manage the energy exchange between arm inductor and PEBB capacitors at a controllable frequency. This can be done by playing with circulating current injection of various harmonic components that are much lower than the switching frequency. In this dissertation, it is proposed to control the circulating current at switching frequency, which will be described thoroughly in Chapter 3.

1.3 Research Motivations and Objectives

1.3.1 Motivations

The literature review has revealed that the MMC under conventional operation modes has both of the two problems described in Section 1.1. First, the MMC is essentially a single-phase converter whose PEBB capacitor energy is mainly coupled with the current flowing through one phase leg. Second, the MMC is usually operated in the CCM mode, where semiconductor switches consume hard turn-on and turn-off losses so that the current that SiC MOSFET modules can take is limited. It is highly motivated to solve the two issues to dramatically increase the power density of MMC. Therefore, the author attempts to develop new operation schemes of the MMC and to build an MV SiC-based MMC prototype for validation.

On the other hand, most of the previous control algorithm in literature was validated in simulations or on a highly scaled-down SiC-based prototype. The control system hardware configurations in those setups are also simplified. Under those "ideal" circumstances, the control signal integrity, noise susceptibility and communication latency cannot be fully represented as in a practical control system. Accordingly, it is also highly motivated to build an MV high-power (e.g. 100 kW) SiC MOSFET-based PEBB prototype where the control algorithm, parasitics impact, EMI susceptibility and thermal management can also be evaluated. Furthermore, an MMC can be constructed based upon that high-power SiC PEBB for the converter-level hardware and control validation.

1.3.2 Objective converter

Despite that the MMC is able to cover very high voltage (±300 kV) applications (e.g. HVDC), due to the limit of lab resources, the number of the MMC PEBBs will not go as high as hundreds in the HVDC applications. The maximum converter DC bus voltage under design in research work is 10 kV, which can fit 4.16~6 kV line-to-line voltage. Wolfspeed 1.7 kV, 225 A SiC MOSFET module is selected as the major power semiconductor device as it is one the most mature commercial products with the highest voltage and current rating in recent years (3.3 kV, 6.5 kV and 10 kV SiC MOSFETs are still in the engineering prototype stage). To fit the device voltage rating, the PEBB DC bus voltage is around 800~1200 V, and there will be at most 10 PEBBs per arm. As demonstrated in **Figure 1-9**, the PEBB topology is a basic H-bridge converter with the maximum delivery of 100 kW with the selected SiC MOSFET. The three-phase MMC converter is rated at 6 kV DC bus, 4.16 kV line-to-line RMS voltage, 150 A phase current, and 1 MVA apparent power.

To simplify the analysis and to better understand the fundamentals of the MMC topology, the research mainly focuses on a simplified MMC. In addition, cost and laboratory resource is limited to afford a number of 100 kW SiC PEBB, so an MMC converter with single PEBB per arm and single phase leg is built. Study on the case of multiple PEBBs per arm will be the prospective work in the future.

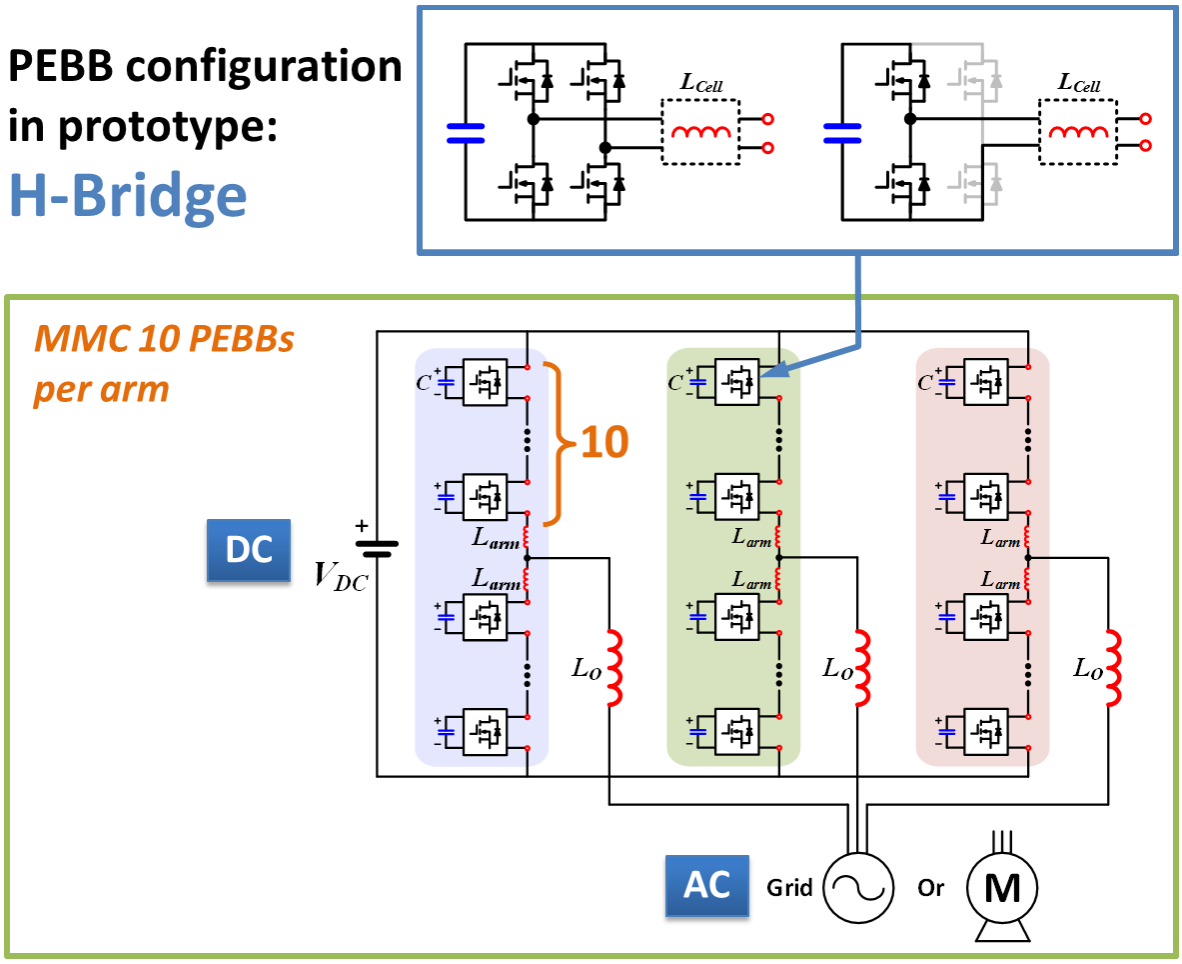


Figure 1-9 Target application in this research work (10 H-bridge PEBBs per arm)

1.3.3 Challenges

The major challenge of this research work is to investigate a band new control method to address the abovementioned two issues. In order to realize switching-cycle-based control and sensing techniques, the time sequence and latency of every signal stage (e.g. fiber optics, logic ICs, A/D converters) should be well considered and calculated in the control margin.

As the experimental validation will be conducted on a high-power prototype, the MMC converter will be pushed toward very extreme conditions in the high-power test. There also exist some other challenges closely related to the high voltage and high current, the extreme switching speed, and the switching-cycle based control.

On one hand, MV high-power power converter has a huge amount of energy storage components. The high voltage and large current can cause severe explosion or burning if any failure happens. Therefore, a very comprehensive fault protection should be designed bottom-up, from device level to the converter system level. At the device level, accurate and fast Short-circuit protection, overvoltage protection, and over-temperature protection should be properly established. At PEBB level, the auxiliary control and gate driver power should be designed robust, and any pre-charge/discharge of the energy storage components (e.g. capacitors) should be working.

On the other hand, by pushing the switching speed of the SiC MOSFET to obtain minimum switching losses, large dv/dt and di/dt noises will be generated that will likely cause susceptibility issues and malfunction of the converter. To overcome that, proper EMI

filter, noise suppression, and propagation path control should be carefully designed in the auxiliary power system, gate drivers and control hardware.

1.4 Dissertation Outlines

In chapter 1, a comprehensive literature review of the MMC modeling, modulation, and control techniques is conducted. The advantages and disadvantages of different models and modulations are compared and evaluated. According to the review conclusions, a potential and promising research area that has never been considered before is found. Then the research motivations and possible application areas are discussed. Last part of this chapter identifies the design objective and challenges. (Related publications [P11])

In Chapter 2, the state-space switching model and average model of the MMC will be presented in the first place. This switching-function based model unveils the very nature of the MMC converter, through which all the possible operation modes can be discovered. Afterward, the switching-cycle-average model is derived from the switching model. The passive energy fluctuation of fundamental-frequency in the MMC is also interpreted in this chapter, and meanwhile, the fact that boosting the switching frequency does not really help increase the power density is explained. (Related publications [P1] [P12])

In chapter 3, by carefully investigating the full switching states, the new SCC is proposed. This chapter elaborates all the fundamentals, parameter design, and application conditions and limitations of the new control method. Closed-loop HCM-SCC is proposed that combines the SCC with a practical realization method for industrial applications. (Related publications [P7] [P8] [P10])

In chapter 4, in order to make the peak-current mode doable for high power applications, a PCB-based RSCS is proposed and designed. It cannot only realize the peak-current-mode control but also protect the SiC MOSFET from Short-circuit events. The switching-current sensor is designed for very high bandwidth, large di/dt, fast response and good accuracy, and also very small profile as it is integrated with the gate driver. The performance of the RSCS has been validated in experiments. (Related publications [P4] [P6])

In chapter 6, the design of Power Electronics Building Block (PEBB) is presented. The design includes the power stage, gate drivers, optical-fiber-based digital control system, mechanical layout, and thermal management. The PEBB is designed to ensure excellent switching performance of the SiC MOSFET, and specifically for very high dv/dt immunity. (Related publications [P3] [P5] [P18] [P19])

In chapter 7, the designed PEBB is validated by experiments with both conventional and proposed HCM-SCC approach. The test results demonstrate the efficiency and power density improvement.

Finally, in chapter 8, the conclusions and future research topics potentially continued from this dissertation are presented.

Chapter.2 State-Space Switching Model and Average Model of MMC

2.1 Introduction

According to the MMC modeling review in the previous chapter, the state-of-the-art MMC models have been developed according to different assumptions and simplifications. Most of these models are steady-state, whether sinusoidal, phasor-based or are assumed that the module capacitors are DC voltage sources. Some models based on switching functions are transformed into average models immediately, thus the intrinsic nature of the converter might not be fully understood. Those average models show their simplicity and effectiveness in the averaged control and balancing loop design within the scope defined in the literature. However, the fundamental circuit behavior cannot be easily observed to the extent that possible operating modes could easily be veiled, and other effects such as the coupling between arm inductors and module capacitors are lost. The other switching models not selecting appropriate state variables still offer very limited help with interpreting the behaviors of the MMC. To this end, this chapter proposes a state-space switching model for MMC that is derived mathematically without any assumptions made from other previous models, which enables the observation on the circuit behaviors from a fundamental point of view.

The proposed switching model serves three purposes. Firstly, an average model of the MMC will be developed based on the switching model, which sets a foundation for understanding the conventional operation behavior of the MMC. Secondly, the switching model unveils unused switching states that can be applied to balance capacitor voltages in a novel manner, which will be introduced in later chapters. Finally, the switching model functions as a critical element of a model-predictive control (MPC) method that will be applied to explore the behavior the MMC operating under the new operation mode.

2.2 State-Space Switching Model

2.2.1 State-Space Modeling

The derivation of the MMC state-space model begins with a minimum MMC configuration. The topology is shown in **Figure 2-1** with only one module in each arm, where all the model variables are given. Note that the model assumes respectively that the two arm inductance L are identical, and the same ac line inductance L_O. The module capacitance values will be modeled individually as shown later. The inductor currents and capacitor voltages are normally selected as "states" to derive the state-space model for converter control. The current-voltage characteristics of those two types of components are in accordance with the typical form of a state equation. Considering that five independent KVL equations for the circuit, i_{Ua}, i_{La}, i_{Ub}, i_{Lb}, and i_{Uc} can be selected as initial state variables that are independent to each other. The DC current, phase current and circulating current are three of the most featured currents of the MMC, which reflect its fundamental

circuit characteristics that need to be controlled during the operation. Thus it would be very helpful to transform those initial state variables into another set of independent states in terms of DC current, phase current and circulating current.

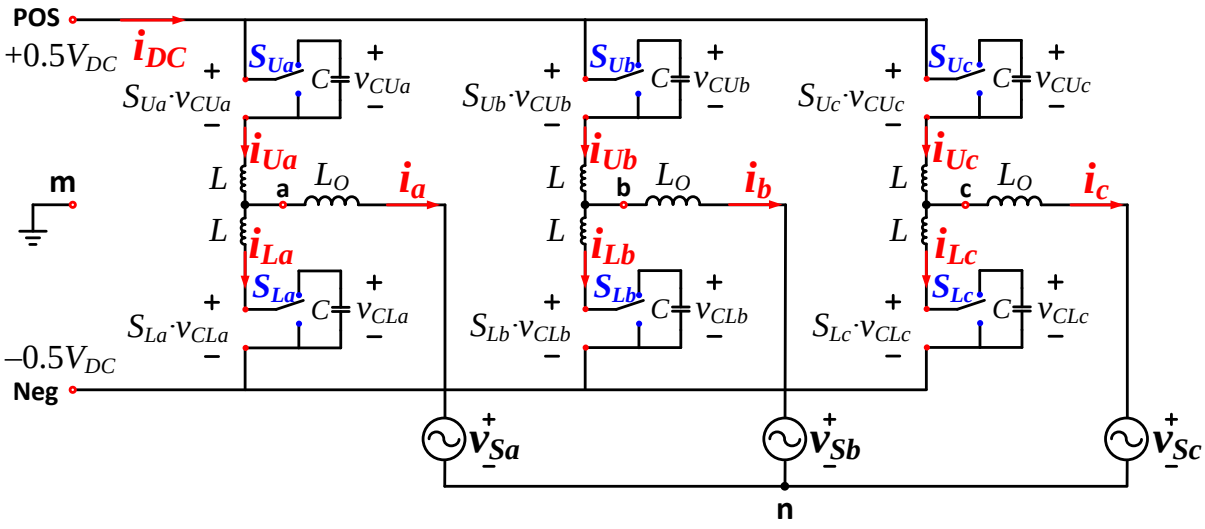


Figure 2-1 Equivalent circuit of three-phase MMC with one module per arm

S_{Ux} and S_{Lx} are the switching functions of the single-pole-double-throw (SPDT) switches that can be either '1' or '0', where x is a phase identifier, given by (2-1). For simplicity, "x=*a*, *b*, or *c*" will be omitted in all the equations that contain x.

(2-1) $$S_{U(L)x} = \begin{cases} 1 & \text{when switched to the upper pole} \\ 0 & \text{when switched to the lower pole} \end{cases}$$

By making an intermediate state variable transform as (2-2) and (2-3), equations of the sum current and phase current can be derived from those arm current variables. Firstly, the sum current equation is given as (2-4), and its equivalent flowing path is shown in **Figure 2-2**. The sum currents are very important intermediate state variables that can help derive DC current and phase current equations.

(2-2) $$i_{sum} = i_{Ux} + i_{Lx}$$

(2-3) $$i_x = i_{Ux} - i_{Lx}$$

(2-4) $$\frac{d}{dt}\frac{i_{sumx}}{2} = \frac{V_{dc} - (S_{Ux}v_{CUx} + S_{Lx}v_{CLx})}{2L}$$

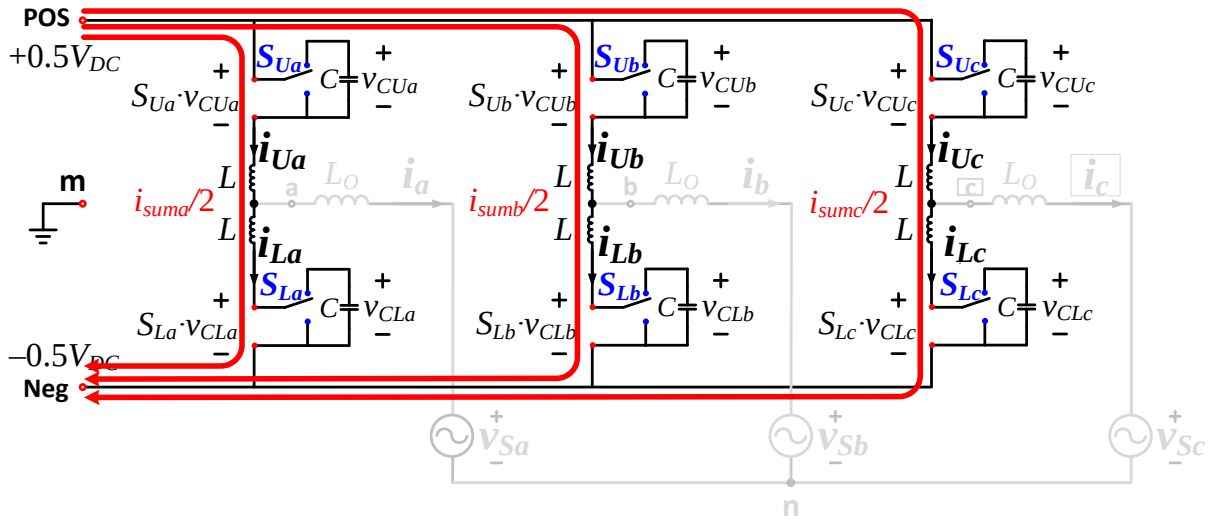


Figure 2-2 Sum current equation derivation

The DC current equation can be derived using KVL in the intersection between the three-phase and the DC bus, given by (2-5) because (2-6) is always valid by KCL.

(2-5) $$i_{DC} = \sum_{x=a,b,c} i_{Ux} = \frac{1}{2} \sum_{x=a,b,c} \left(i_{sumx} + i_x \right) = \frac{1}{2} \sum_{x=a,b,c} i_{sumx}$$

(2-6) $$\sum_{x=a,b,c} i_x = i_a + i_b + i_c = 0$$

The common-mode voltage between the AC neutral to the DC mid-point, the v_{nm_1}, is expressed by (2-7) and then the AC phase current equations are given by (2-8).

(2-7) $$v_{nm\_1} = \frac{1}{6} \sum_{x=a,b,c} \left(S_{Lx} v_{CLx} - S_{Ux} v_{CUx} \right)$$

(2-8) $$\frac{d}{dt} i_x = \frac{(S_{Lx} v_{CLx} - S_{Ux} v_{CUx}) - 2v_{nm} - 2v_{Sx}}{2L_O + L}$$

Based on the definition of circulating currents, they only circulate between phase-leg without flowing to the DC bus or the AC line. Therefore, the equations of circulating currents can be derived by solving the circuit in **Figure 2-3**, given by (2-9).

(2-9) $$\frac{d}{dt} i_{cirx} = \frac{1}{6L} \left[\begin{array}{l} \sum_{x=a,b,c} \left(S_{Lx} v_{CLx} + S_{Ux} v_{CUx} \right) \\ -3(S_{Ux} v_{CUx} + S_{Lx} v_{CLx}) \end{array} \right]$$

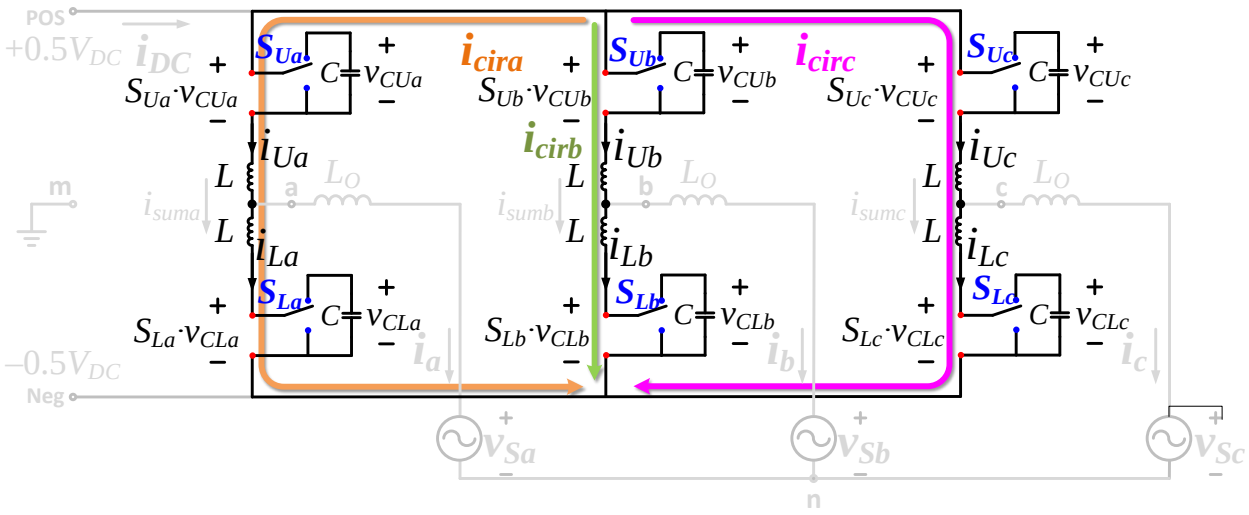


Figure 2-3 Circulating current equations derivation

The similarity between (2-4) and (2-9) can be observed by comparing them to each other, then a secondary state-variable transformation is made based on the relationship between the circulating current and sum current equations, given by (2-10), if considering a reasonable assumption that the initial states of all the currents flowing in the converter system are zero.

(2-10)
$$i_{cirx} = \frac{1}{6}\left(3i_{sumx} - \sum_{x=a,b,c} i_{sumx}\right)$$

Finally, the full-rank current equations for the state-space model are derived as the following (2-11), which has five independent equations:

(2-11)
$$\begin{cases} \dfrac{d}{dt}i_{dc} = \dfrac{1}{2L}\left[3V_{dc} - \sum\limits_{x=a,b,c}(S_{Ux}v_{CUx} + S_{Lx}v_{CLx})\right] \\ \dfrac{d}{dt}i_{a} = \dfrac{1}{L_O + L/2}\begin{bmatrix}(S_{La}v_{CLa} - S_{Ua}v_{CUa})/2 \\ -v_{Sa} - v_{nm\_1}\end{bmatrix} \\ \dfrac{d}{dt}i_{b} = \dfrac{1}{L_O + L/2}\begin{bmatrix}(S_{Lb}v_{CLb} - S_{Ub}v_{CUb})/2 \\ -v_{Sb} - v_{nm\_1}\end{bmatrix} \\ \dfrac{d}{dt}i_{cira} = \dfrac{1}{6L}\begin{bmatrix}\sum\limits_{x=a,b,c}\left(S_{Lx}v_{CLx} + S_{Ux}v_{CUx}\right) \\ -3(S_{Ua}v_{CUa} + S_{La}v_{CLa})\end{bmatrix} \\ \dfrac{d}{dt}i_{cirb} = \dfrac{1}{6L}\begin{bmatrix}\sum\limits_{x=a,b,c}\left(S_{Lx}v_{CLx} + S_{Ux}v_{CUx}\right) \\ -3(S_{Ub}v_{CUb} + S_{Lb}v_{CLb})\end{bmatrix} \end{cases}$$

where v_{nm_1} is defined the same as (2-7). The two-step state variable transforms are summarized by (2-12),

$$\begin{bmatrix} i_{DC} \\ i_a \\ i_b \\ i_{cira} \\ i_{cirb} \end{bmatrix} = \mathbf{T_2} \begin{bmatrix} i_a \\ i_b \\ i_{suma} \\ i_{sumb} \\ i_{sumc} \end{bmatrix} = \mathbf{T_2}\mathbf{T_1} \begin{bmatrix} i_{Ua} \\ i_{Ub} \\ i_{La} \\ i_{Lb} \\ i_{Uc} \end{bmatrix} \tag{2-12}$$

where

$$\mathbf{T_1} = \begin{bmatrix} 1 & 1 & -1 & -1 & 2 \\ 1 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

$$\mathbf{T_2} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1/3 & -1/6 & -1/6 \\ 0 & 0 & -1/6 & 1/3 & -1/6 \\ 0 & 0 & 1/2 & 1/2 & 1/2 \end{bmatrix}$$

Note that both $\mathbf{T_1}$ and $\mathbf{T_2}$ are linear and invertible matrices, which means that both steps of the transformation are linear and full-rank. Inversely, the expression for the original inductor currents with new variables can be derived by inverting the transition matrix, given by (2-13)

$$\begin{cases} i_{Ux} = i_{dc}/3 + i_x/2 + i_{cirx} \\ i_{Lx} = i_{dc}/3 - i_x/2 + i_{cirx} \end{cases} \tag{2-13}$$

Finally, the state equations for module capacitors are given by (2-14) and (2-15).

(2-14) $$\frac{d}{dt}v_{CUx} = \frac{1}{C}S_{Ux}i_{Ux}$$

(2-15) $$\frac{d}{dt}v_{CLx} = \frac{1}{C}S_{Lx}i_{Lx}$$

In (2-14) and (2-15), the individual module capacitance value C_{Ux} and C_{Lx} are defined, which shows that this model is able to capture the individual dynamics of each of its intrinsic state variables. Regardless, the model can be simplified in case all capacitors are assumed to be identical in which case a simple "*C*" is used. Further, the model can be easily extended to the multilevel case with *n* modules per arm as shown in (2-16) ~ (2-19), with the assumed phase symmetry for the three-phase variables and voltage sources. All the analysis in Section IV is based on the *n*-module-per-arm model.

(2-16)

$$\begin{cases} \frac{d}{dt}i_{DC} = \frac{1}{2L}\left[3V_{DC} - \sum_{x=a,b,c}\sum_{i=1}^{n}(S_{Uxi}v_{CUxi} + S_{Lxi}v_{CLxi})\right] \\ \frac{d}{dt}i_{a} = \frac{1}{L_O + L/2}\left[\sum_{i=1}^{n}(S_{Lai}v_{CLai} - S_{Uai}v_{CUai})/2 - v_{Sa} - v_{nm}\right] \\ \frac{d}{dt}i_{b} = \frac{1}{L_O + L/2}\left[\sum_{i=1}^{n}(S_{Lbi}v_{CLbi} - S_{Ubi}v_{CUbi})/2 - v_{Sb} - v_{nm}\right] \\ \frac{d}{dt}i_{cira} = \frac{1}{6L}\left[\sum_{x=a,b,c}\sum_{i=1}^{n}(S_{Uxi}v_{CUxi} + S_{Lxi}v_{CLxi}) - 3\sum_{i=1}^{n}(S_{Uai}v_{CUai} + S_{Lai}v_{CLai})\right] \\ \frac{d}{dt}i_{cirb} = \frac{1}{6L}\left[\sum_{x=a,b,c}\sum_{i=1}^{n}(S_{Uxi}v_{CUxi} + S_{Lxi}v_{CLxi}) - 3\sum_{i=1}^{n}(S_{Ubi}v_{CUbi} + S_{Lbi}v_{CLbi})\right] \end{cases}$$

(2-17) $$\frac{d}{dt}v_{CUxi} = \frac{1}{C}S_{Uxi}i_{Ux},\ i = 1,\ldots,n$$

(2-18) $$\frac{d}{dt}v_{CLxi} = \frac{1}{C}S_{Lxi}i_{Lx},\ i = 1,\ldots,n$$

(2-19) $$v_{nm\_n} = \frac{1}{6}\sum_{x=a,b,c}\sum_{i=1}^{n}(S_{xiL}v_{xiL} - S_{xiU}v_{xiU})$$

2.2.2 State-Space Switching Model Verification

In order to prove the correctness of the proposed switching-cycle mathematical model, the simulation of a switching model in Matlab Simulink® is conducted for comparison. Specifically, two-module-per-arm MMC (N=2) operating waveforms are generated by both the mathematical and the switching models. In order to simulate the proposed model, the differential equations of the state-space model (2-16) ~ (2-19) are discretized into the difference equations (2-20) using a Euler approximation. A time-step of ΔT = 1 μs was used to make sure the approximation is accurate enough. The respective switching functions of the converter modules were generated by comparing the triangular carriers and sinusoidal functions. All the initial values of the state variables were set to zero.

(2-20)

$$
\begin{cases}
i_{DC}(k)=\dfrac{1}{2L}\left[3V_{DC}-\sum\limits_{x=a,b,c}\sum\limits_{i=1}^{n}\left[S_{Uxi}(k-1)v_{Uxi}(k-1)+S_{Lxi}(k-1)v_{Lxi}(k-1)\right]\right]\cdot\Delta T+i_{DC}(k-1)\\
i_{a}(k)=\dfrac{1}{L/2}\left[\sum\limits_{i=1}^{n}\left(S_{Lai}(k-1)v_{Lai}(k-1)-S_{Uai}(k-1)v_{Uai}(k-1)\right)\Big/2-v_{Sa}(k-1)-v_{nm}(k-1)\right]\cdot\Delta T+i_{a}(k-1)\\
i_{b}(k)=\dfrac{1}{L/2}\left[\sum\limits_{i=1}^{n}\left(S_{Lbi}(k-1)v_{Lbi}(k-1)-S_{Ubi}(k-1)v_{Ubi}(k-1)\right)\Big/2-v_{Sb}(k-1)-v_{nm}(k-1)\right]\cdot\Delta T+i_{b}(k-1)\\
i_{cira}(k)=\dfrac{1}{6L}\left[\begin{array}{l}\sum\limits_{x=a,b,c}\sum\limits_{i=1}^{n}\left(S_{Lxi}(k-1)v_{CLxi}(k-1)+S_{Uxi}(k-1)v_{CUxi}(k-1)\right)\\ \quad-3\sum\limits_{i=1}^{n}\left(S_{Uai}(k-1)v_{CUai}(k-1)+S_{Lai}(k-1)v_{CLai}(k-1)\right)\end{array}\right]\cdot\Delta T+i_{cira}(k-1)\\
i_{cirb}(k)=\dfrac{1}{6L}\left[\begin{array}{l}\sum\limits_{x=a,b,c}\sum\limits_{i=1}^{n}\left(S_{Lx}(k-1)v_{CLx}(k-1)+S_{Ux}(k-1)v_{CUx}(k-1)\right)\\ \quad-3\sum\limits_{i=1}^{n}\left(S_{Ub}(k-1)v_{CUb}(k-1)+S_{Lb}(k-1)v_{CLb}(k-1)\right)\end{array}\right]\cdot\Delta T+i_{cirb}(k-1)\\
v_{CUxi}(k)=\dfrac{1}{C}S_{Uxi}(k-1)v_{CUxi}(k-1)\cdot\Delta T+v_{CUxi}(k-1),\ x=a,b,c,\ i=1,\cdots,n\\
v_{CLxi}(k)=\dfrac{1}{C}S_{Lxi}(k-1)v_{CLxi}(k-1)\cdot\Delta T+v_{CLxi}(k-1),\ x=a,b,c,\ i=1,\cdots,n\\
v_{nm\_n}(k)=\dfrac{1}{6}\sum\limits_{x=a,b,c}\sum\limits_{i=1}^{n}\left[S_{Lxi}(k-1)v_{CLxi}(k-1)-S_{Uxi}(k-1)v_{CUxi}(k-1)\right]
\end{cases}
$$

On the other hand, a switching model has been built in Simulink® where the voltage sources, active and passive components are taken from the SimPowerSystem library. For a fair comparison, ideal switches, inductors, and capacitors with no parasitic parameters as well as ideal voltage sources are used. Any controller delays are not included in the model. In the simulation setup, "Discrete-Tustin" and "ode23tb" solver was selected with a sampling time T_S = 1 μs. The switching functions were generated by the comparison between "triangle" and "sine wave" blocks whose magnitudes, frequencies and phase angles are the same as those used in the mathematical model. All the initial values of the inductor currents and capacitor voltages were set to be zero as well. The comparison result is shown on the top view graphs in **Figure 2-4** ~ **Figure 2-7**, on which the perfect match between the two models is shown. This indicates that the mathematical derivation of the proposed model is correct and the proposed model is accurate to represent all the behavior of the MMC converter without losing any information of the converter. Consequently, any further analysis, modeling and controller design of the converter can be carried out using the proposed model without losing information.

Specifically, the analysis on the MMC circuit can be carried out by observing the equations of the state-space switching model. The DC current is controlled by the addition of all the switching functions in the circuit if considering that the ripples of all capacitors are relatively small. The waveforms shown in **Figure 2-4** illustrate the relationships between them.

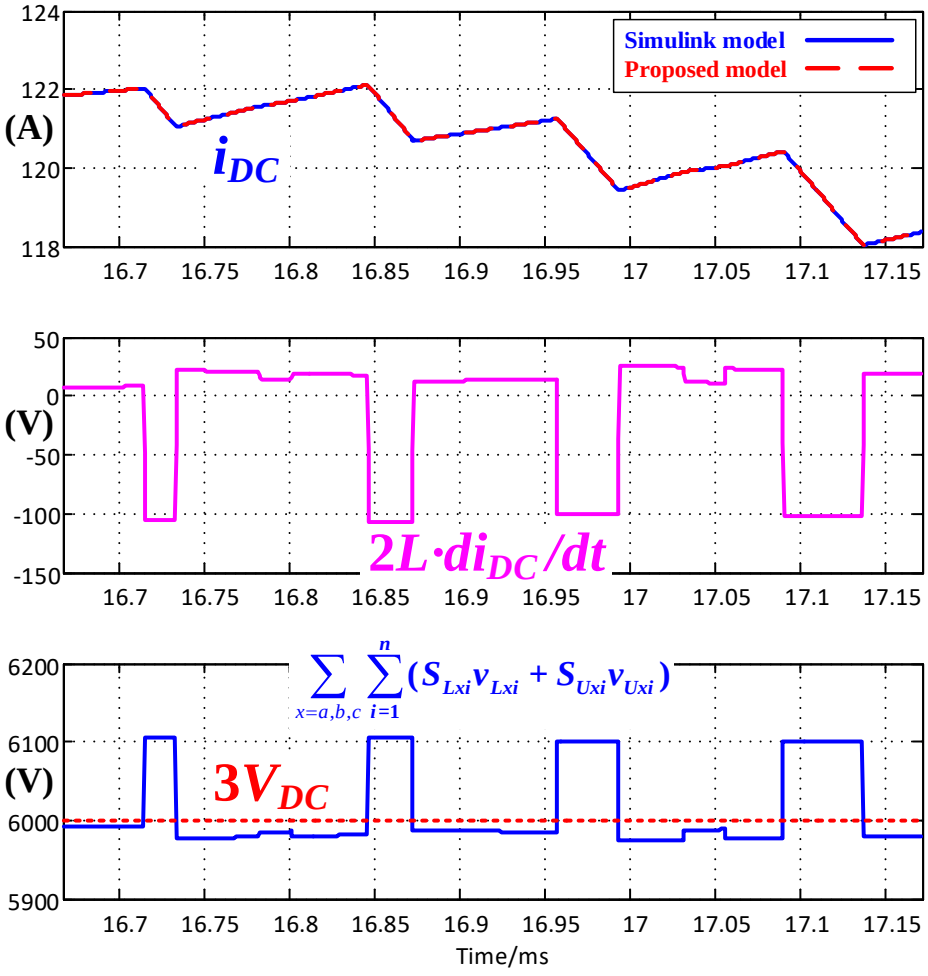


Figure 2-4 Waveforms for DC current equation

From the derivation of (2-21) in Section III, if the arm inductance is required to be minimized, the restriction for the switching function follows (2-22) which has to be satisfied for each phase, otherwise, the DC current will go to infinity. (2-22) shows the relations between the averaged capacitor voltages and the switching functions in one phase.

(2-21) $$\frac{d}{dt}i_{DC} = \frac{1}{2L}\left[3V_{DC} - \sum_{x=a,b,c}\sum_{i=1}^{n}(S_{Uxi}v_{Uxi} + S_{Lxi}v_{Lxi})\right]$$

(2-22) $$\sum_{i=1}^{n}(S_{Uxi}\overline{v}_{Uxi} + S_{Lxi}\overline{v}_{Lxi}) = V_{dc}$$

If all the capacitor voltages are well balanced, (2-23) is valid, and then (2-24) is necessary at every switching period for minimal arm inductance where the DC current will be quite smooth without any spikes. Thus the insertion index, or both the reference and carrier waveforms in PWM modulator, need to be designed carefully in terms of the different modulation schemes applied.

(2-23) $$\overline{v}_{Uxi} = \overline{v}_{Lxi} = V_{dc}/n$$

(2-24) $$\sum_{i=1}^{n}(S_{Uxi} + S_{Lxi}) = n$$

In order to obtain more voltage levels, certain modulation schemes allow for the occurrence of (2-25) where the two arm inductors will block the voltage of one module capacitor from time to time. Thus the arm inductance has to be much larger than the case with switching restriction of (2-24), otherwise large current spikes will occur on the DC current. The polarity of the averaged across voltage on inductors is alternating at thrice the

line frequency.

$$\sum_{i=1}^{n}(S_{Uxi}+S_{Lxi})=n\pm 1 \qquad \textbf{(2-25)}$$

For the phase current equation in (2-26), the two arm inductors are paralleled from the line-side perspective. The variables waveforms are shown in **Figure 2-5**, which illustrates the connections between them. The equation (2-26) dominates the control of the phase current. Assuming n=2, the v_{diff} value of (2-27) could be "three-levels" as $+V_{dc}/2$, 0, $-V_{dc}/2$ on the restriction of (2-24). However, on the restriction of (2-25), the value of (2-27) could be "five-levels" as $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$.

$$\frac{d}{dt}i_x=\frac{1}{L_O+L/2}\left[\sum_{i=1}^{n}(S_{Lxi}v_{Lxi}-S_{Uxi}v_{Uxi})/2-v_{Sx}-v_{nm}\right] \qquad \textbf{(2-26)}$$

$$v_{diff}=\sum_{i=1}^{n}(S_{Lxi}v_{Lxi}-S_{Uxi}v_{Uxi})/2 \qquad \textbf{(2-27)}$$

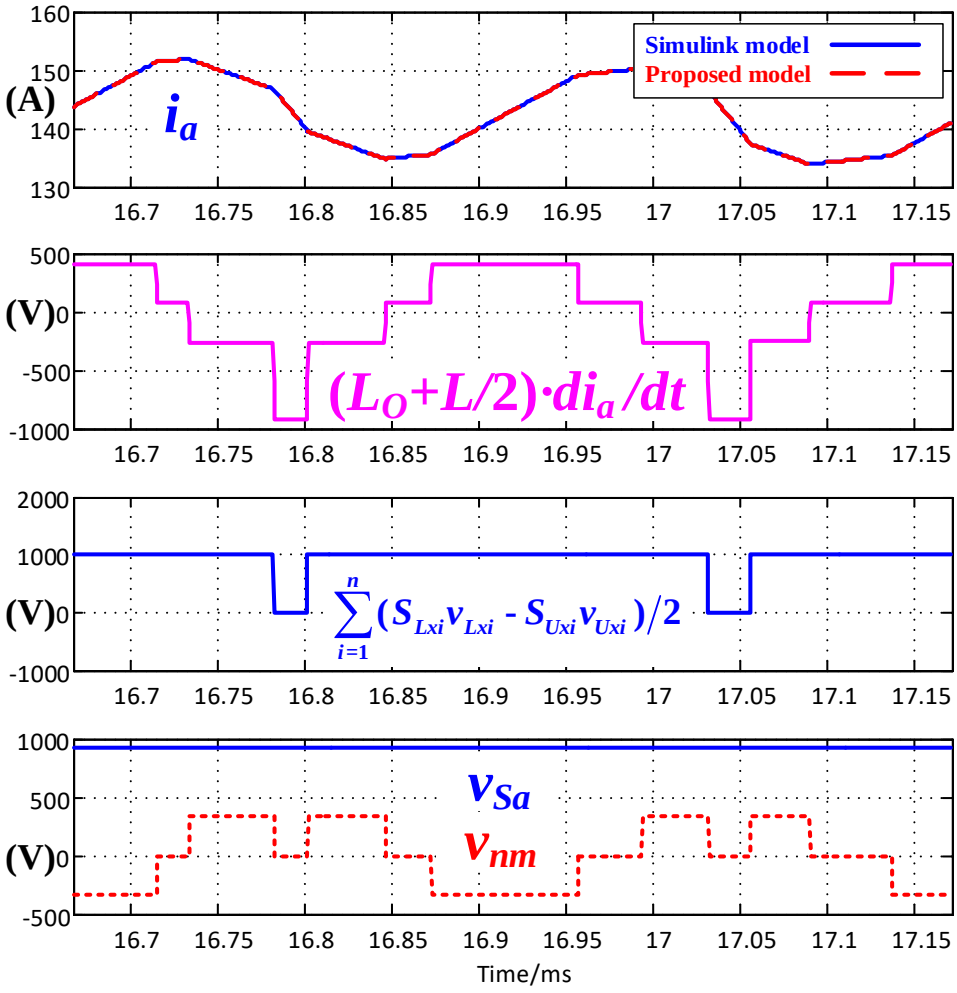


Figure 2-5 Waveforms for line current equation

If a sequence of switching functions from one switch cycle to another are controlled so that (2-27) follows a sinusoidal averaged value at line frequency, the phase current will be controlled to be sinusoidal with an amplitude determined by L_O+L/2, the equivalent line inductance.

The zero-sequence neutral-to-mid voltage equation in (2-28) is the arithmetic mean of the three-phase voltage commands controlled by all the switches. The amplitude of v_{nm_n} is smaller and its pulse duration is also shorter compared to (2-29) since the three-phase symmetry leads to nearly no impact on the phase current. v_{nm_n} averagely alternates at 3rd-order line frequency. The waveforms are shown in **Figure 2-6** that illustrates the relations between them.

(2-28)
$$v_{nm\_n} = \frac{1}{6}\sum_{x=a,b,c}\sum_{i=1}^{n}(S_{Lxi}v_{Lxi} - S_{Uxi}v_{Uxi})$$

(2-29)
$$\frac{d}{dt}i_{cirx} = \frac{1}{6L}\left[\sum_{x=a,b,c}\sum_{i=1}^{n}(S_{Uxi}v_{Uxi} + S_{Lxi}v_{Lxi}) - 3\sum_{i=1}^{n}(S_{Uxi}v_{Uxi} + S_{Lxi}v_{Lxi})\right]$$

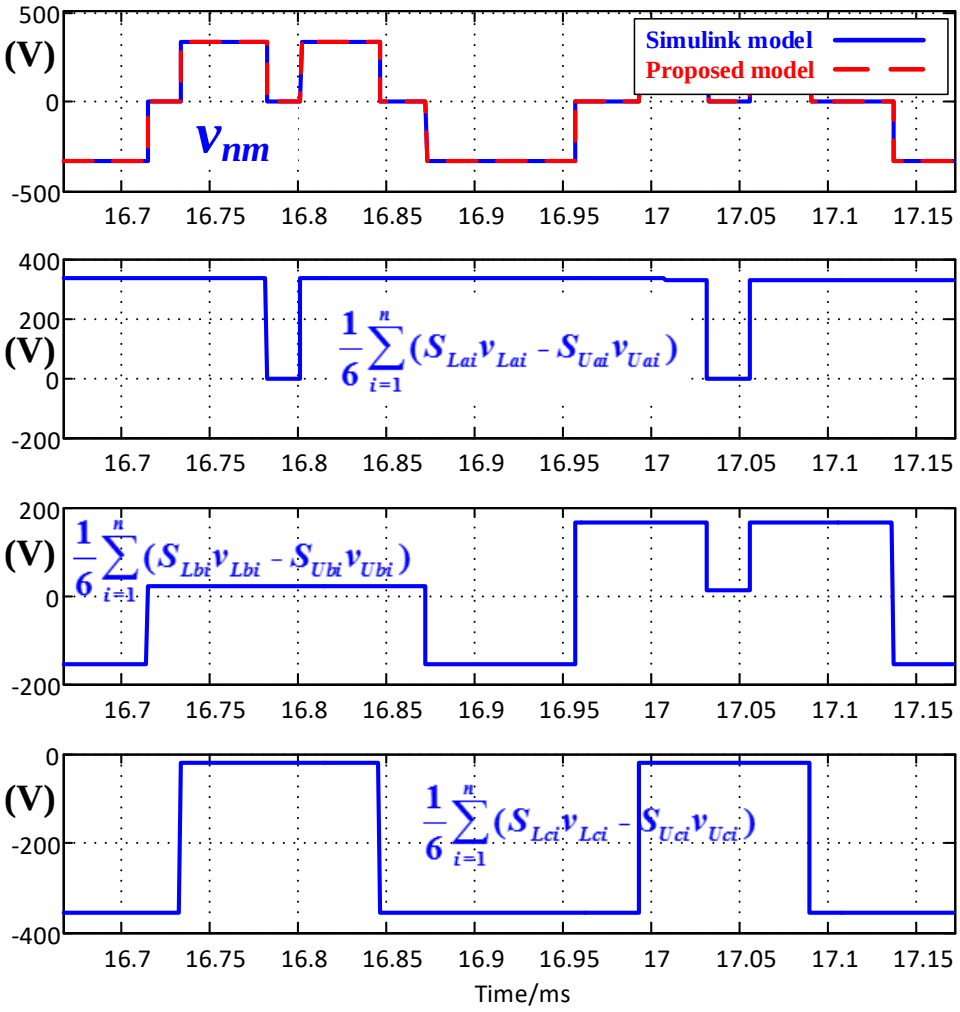


Figure 2-6 Waveforms for neutral voltage equation

The circulating current related variable waveforms and the relations between them are shown in **Figure 2-7**. For the circulating current equation in (2-29), assuming that the restriction for switching functions follows (2-24), then ideally the right-hand side of (2-29) is equal to zero at every switching period if all the capacitor voltage is constant. In this case, no circulating current will be observed during the operation of the three-phase symmetric system. Considering the capacitor ripple, the circulating current will consist of a harmonic current with 2nd-order and above frequency as described in [B.1] .

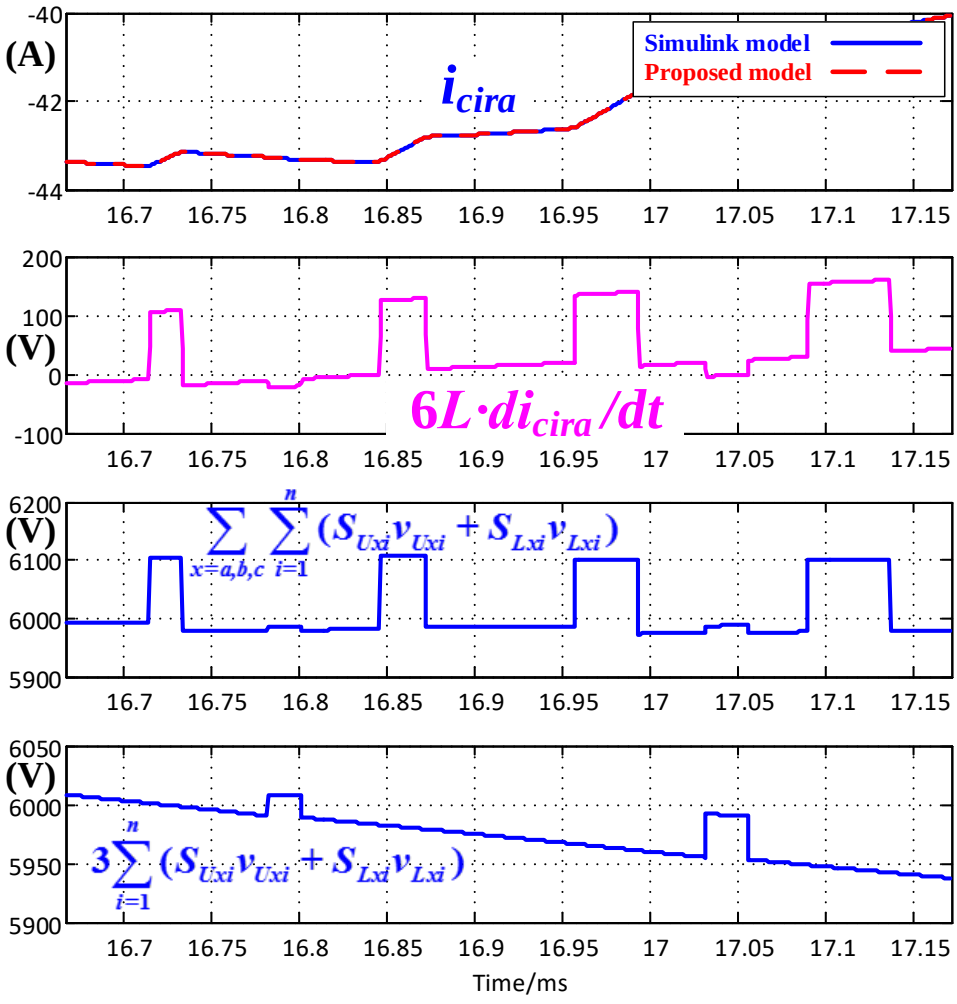


Figure 2-7 Waveforms for circulating current equation.

The module capacitor equation, for instance, the upper module equation (2-30), reflects the cause for the capacitor voltage ripple. The capacitor voltage can be changed only when S_{Uxi}=1. The amplitude and frequency of current i_{Ux} determine the ripple amplitude and the frequency of v_{Ux}.

(2-30) $$\frac{d}{dt}v_{Uxi} = \frac{1}{C_{Uxi}}S_{Uxi}i_{Ux}$$

(2-31) $$i_{Ux} = i_{dc}/3 + i_x/2 + i_{cirx}$$

In (31), the current i_{DC} must have a positive DC offset when the MMC is delivering active power from DC to AC, so the on-time duration of S_{Uxi} when i_{Ux}>0 has to be shorter than that of S_{Uxi} when i_{Ux}<0, otherwise the capacitor ampere·second balance cannot be achieved within the line cycle. Note that among those currents in (2-31) only i_x is the one that must follow certain reference to deliver/absorb energy to/from the AC line side. The current i_{DC} and i_{cirx} could be regarded as degrees of freedom to control the instant current flowing through module capacitors, which affords a possibility to achieve ampere·second balance for capacitors in a switching cycle. The restrictions of the sum of the switching functions of the upper and lower arms include but are not limited to (2-24) and (2-25) such that more switching states could be used for capacitor voltage control.

2.3 Average Model and MMC Analysis Based on It

Conventionally, the switching model of MMC is not used directly, instead, the average model is more commonly applied for closed-loop regulator design. The switching-

cycle averaged value of all the time-domain variables are defined the same way as (2-32), where the DC current is shown as an example.

(2-32) $$\overline{i_{DC}} = \frac{1}{T_{SW}} \int_0^{T_{SW}} i_{DC}(t)\,dt$$

Then the switching-cycle average model is derived as (2-33) ~ (2-37), assuming that all averaged capacitance values of all the modules are the same. An arithmetic mean value i_{MEAN} that equals to half of the sum current is defined as (2-33)

(2-33) $$\overline{i_{MEANx}} = \frac{\overline{i_{sumx}}}{2} = \frac{\overline{i_{Ux}} + \overline{i_{Lx}}}{2}$$

(2-34)
$$\begin{cases} \frac{d}{dt}\overline{i_{DC}} = \frac{1}{2L}\left[3V_{DC} - N \cdot \sum_{x=a,b,c}(d_{Ux}\overline{v_{CUx}} + d_{Lx}\overline{v_{CLx}})\right] \\ \frac{d}{dt}\overline{i_a} = \frac{1}{L_O + L/2}\left[N \cdot (d_{La}\overline{v_{CLa}} - d_{Ua}\overline{v_{CUa}})/2 - \overline{v_{Sa}} - \overline{v_{nm}}\right] \\ \frac{d}{dt}\overline{i_b} = \frac{1}{L_O + L/2}\left[N \cdot (d_{Lb}\overline{v_{CLb}} - d_{Ub}\overline{v_{CUb}})/2 - \overline{v_{Sb}} - \overline{v_{nm}}\right] \\ \frac{d}{dt}\overline{i_{cira}} = \frac{N}{6L}\left[\sum_{x=a,b,c}(d_{Ux}\overline{v_{CUx}} + d_{Lx}\overline{v_{CLx}}) - 3(d_{Ua}\overline{v_{CUa}} + d_{La}\overline{v_{CLa}})\right] \\ \frac{d}{dt}\overline{i_{cirb}} = \frac{N}{6L}\left[\sum_{x=a,b,c}(d_{Ux}\overline{v_{CUx}} + d_{Lx}\overline{v_{CLx}}) - 3(d_{Ub}\overline{v_{CUb}} + d_{Lb}\overline{v_{CLb}})\right] \end{cases}$$

(2-35) $$\frac{d}{dt}\overline{v_{CUx}} = \frac{1}{C} S_{Ux}\overline{i_{Ux}},\ x = a,b,c$$

(2-36) $$\frac{d}{dt}\overline{v_{CLx}} = \frac{1}{C} S_{Lx}\overline{i_{Lx}},\ x = a,b,c$$

(2-37) $$\overline{v_{nm\_n}} = \frac{N}{6} \sum_{x=a,b,c} (d_{Lx} v_{CLx} - d_{Ux} v_{CUx})$$

With the averaged mode, the duty cycles, voltage sources and phase current can be assumed sinusoidal, then the averaged operation behavior of the MMC can be studied. In the MMC, the mean current represents the active power supplied from the DC source. When the mean current is controlled as a DC value eliminating all the AC components [B.2] -[B.24] , the waveform of the critical variables in the MMC is shown in **Figure 2-8**. The upper arm current i_U have mainly the fundamental component, and thus the capacitor energy P_{CU} and voltage ripples v_{CU} have fundamental and second order harmonics.

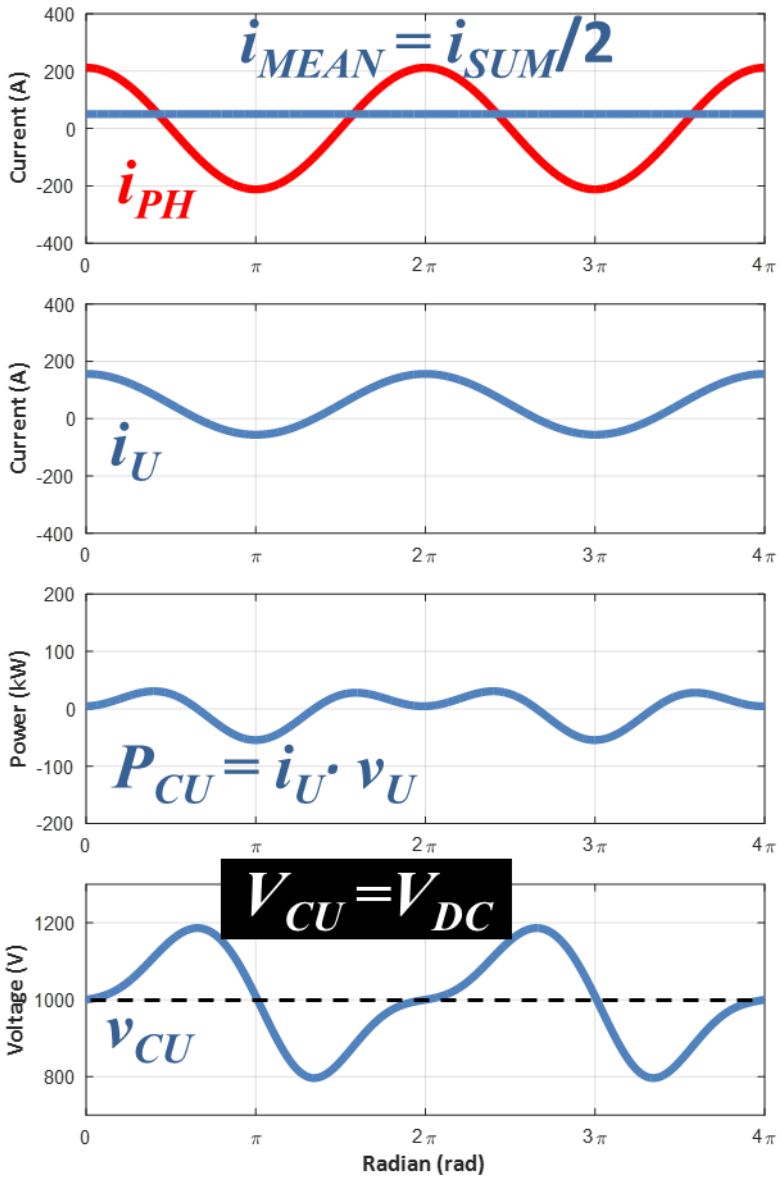


Figure 2-8 MMC Waveforms when mean current is DC.

If the mean current is injected with AC components, the active power supplied from the DC source remains constant. Therefore, the AC components provides a degree of freedom by which the capacitor energy fluctuation can be manipulated. In [B.25] [B.26] , the mean current is controlled as a DC plus 2nd-order harmonic. The MMC behavior under this operation mode is shown as **Figure 2-9**. By this way the capacitor energy P_{CU} and voltage ripples v_{CU} have lower ripple magnitude, and their harmonic spectrums is changed.

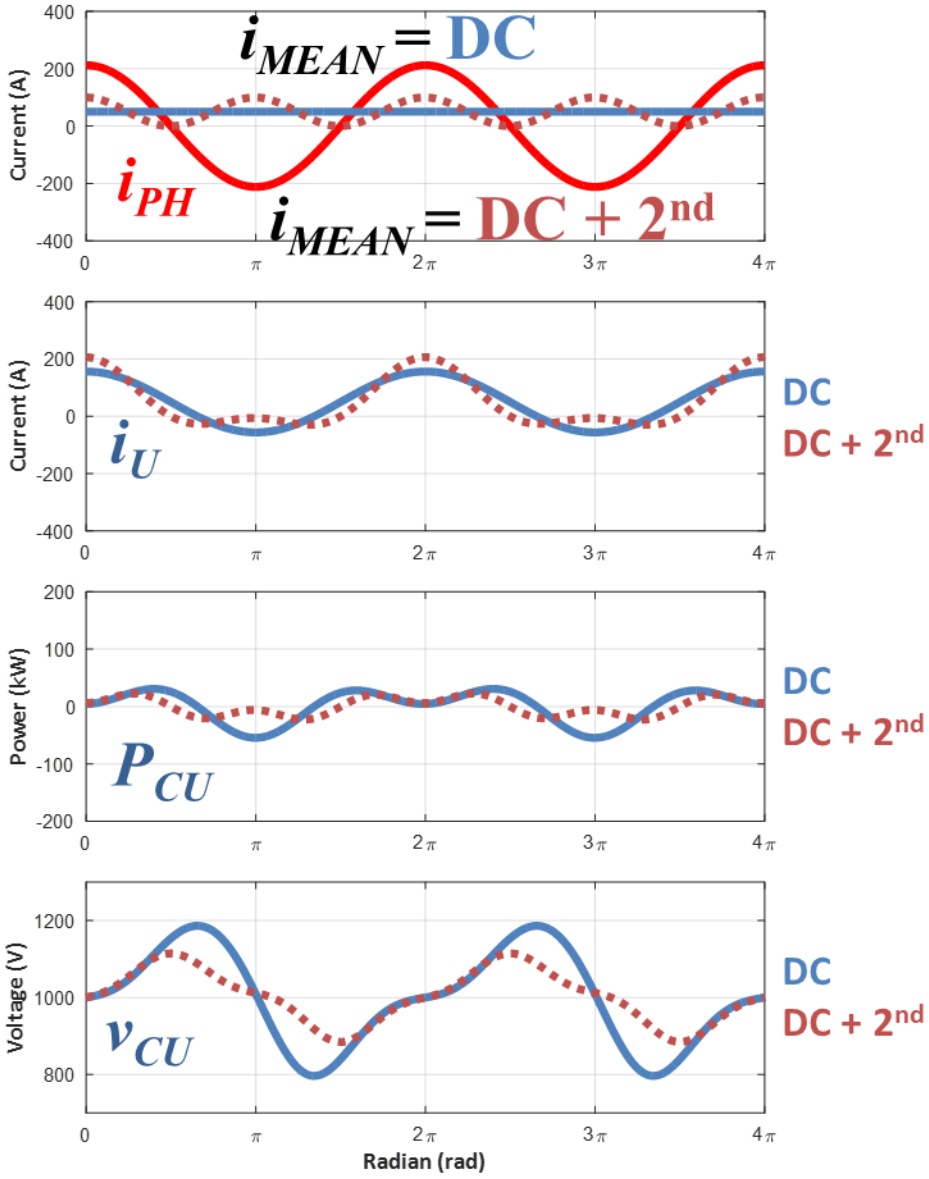


Figure 2-9 MMC Waveforms when mean current is DC+2nd harmonic.

Because of the abovementioned MMC operation fundamentals, the module capacitance has to be very large to suppress the low-frequency voltage ripple. The MMC capacitance design with conventional controls has been discussed in a number of references [B.27] . Plus, a typical math expression in (2-38) shows the capacitor voltage ripple is proportional to phase current RMS value, and inversely proportional to the fundamental frequency and module capacitance. This again implies the critical issue of the MMC that it cannot operate at a very low fundamental frequency or at DC-DC mode (f_0 = 0 Hz) by conventional controls.

(2-38) $$v_{CU(L)\_AC} \propto \frac{I_{PH}}{f_0 \cdot C}$$

The capacitor voltage ripple versus fundamental frequency is shown in **Figure 2-10**, at 1 kV DC bus voltage, 150 A phase current, and the capacitance value is 500 μF. With DC mean current, at 60 Hz, the ripple peak is 1.2 kV, which becomes 1.1 kV with 2nd-order mean current injection. When the fundamental frequency decreases, the capacitor voltage ripple becomes unacceptably large and the capacitance has to be enlarged, although the 500 μF capacitor size already dominates the module volume. An actual example shown in **Figure 2-11** indicates that in the industrial HVDC converter module the capacitor volume is a critical problem.

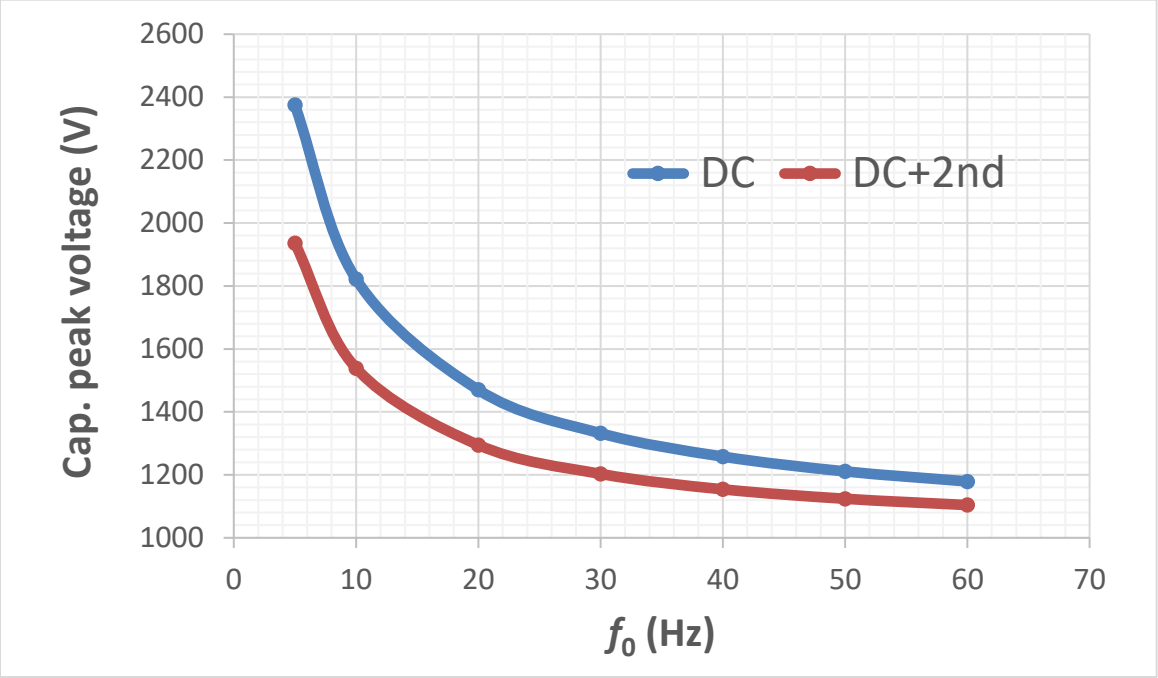


Figure 2-10 MMC capacitance voltage ripple peak versus fundamental frequency.

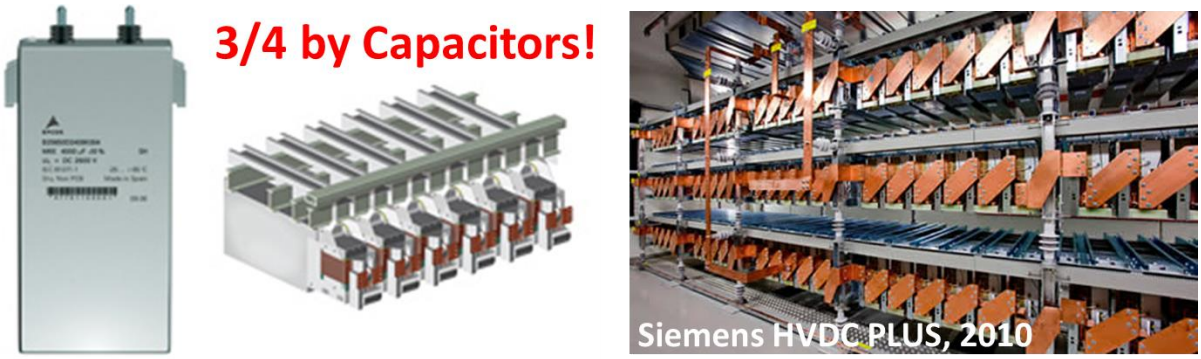


Figure 2-11 HVDC Plus modules where the capacitor volume dominates.

Since the AC components of the mean current can be manipulated in any form, another previous practice that the mean current is controlled as a DC plus 2nd-order plus high-frequency harmonics is proposed in [B.28] . This method is dedicated to the occasions when the fundamental frequency is below 30 Hz, and the injected high frequency is higher than 6th order. An example of the MMC behavior under this operation mode is shown in **Figure 2-12**. The injection frequency is set equal to 20 times of the fundamental frequency. By this way, the capacitor energy P_{CU} and voltage v_{CU} ripples magnitudes are further reduced, which contains trivial fundamental frequency component. Other similar harmonic injection approaches inspired by the method in [B.28] has been published in [B.29] -[B.35] .

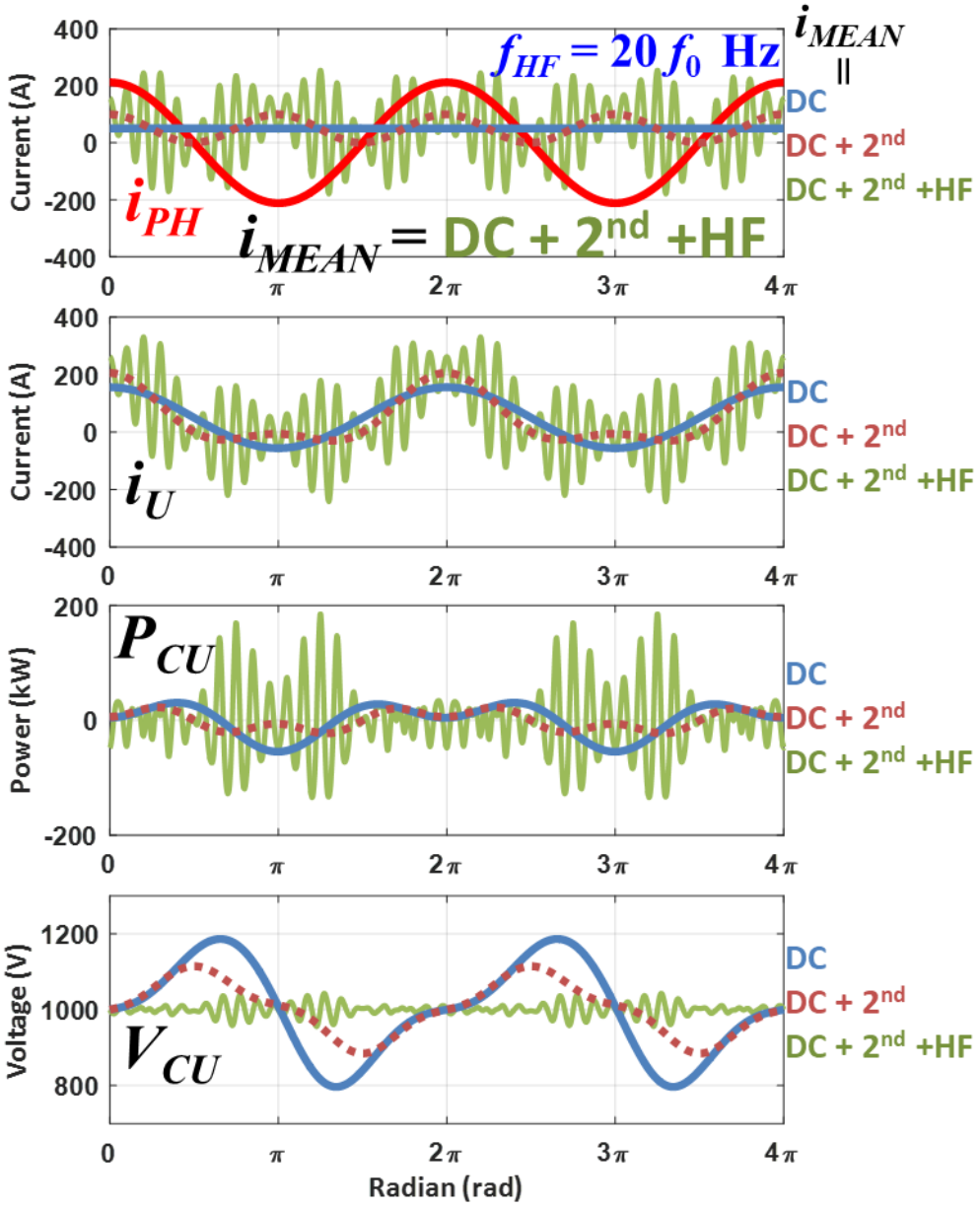


Figure 2-12 MMC Waveforms when mean current is DC+2nd+HF harmonics.

To fully understand the behaviors of the abovementioned three different operation modes of the MMC, a harmonic spectrum comparison has been conducted in **Figure 2-13**. i_{MEAN}, i_U, P_{CU} and voltage v_{CU} ripple are four variables being compared. The mean current i_{MEAN} has been regulated as in Case (a) "DC" (blue bar), Case (b) "DC+2nd harmonic" (red bar), or Case (c) "DC+2nd harmonic + high frequency" (green bar), respectively. In the first row, the high-frequency components of the green bars dominate the root mean square value, at the odd side-band of the injection frequency. They are 17th, 19th, 21st, and 23rd harmonic of the fundamental frequency 60 Hz. Upper arm current i_U contains all the mean current information, and hence it contains similar harmonic spectrum as i_{MEAN}. Because of the harmonic cancellation effect brought by the high-frequency injection, upper capacitor charging energy P_{CU} at the 3rd row does not have low-frequency component. Instead, its frequency concentrates on the 20th frequency and its side-band frequencies, where the capacitor impedance is very low. Consequently, in Case (c) those frequency components on the capacitor voltage are insignificant at the 4th row of the figure. On the contrary, in Case (a) and (b) the 1st-, 2nd-, and 3rd-order harmonics dominate the capacitor voltage ripple.

The upper limit of the injected high-frequency harmonics is the switching frequency in a switching power converter. The next chapter investigates the performance when the harmonic injection frequency reaches the upper limit, that is, the switching frequency.

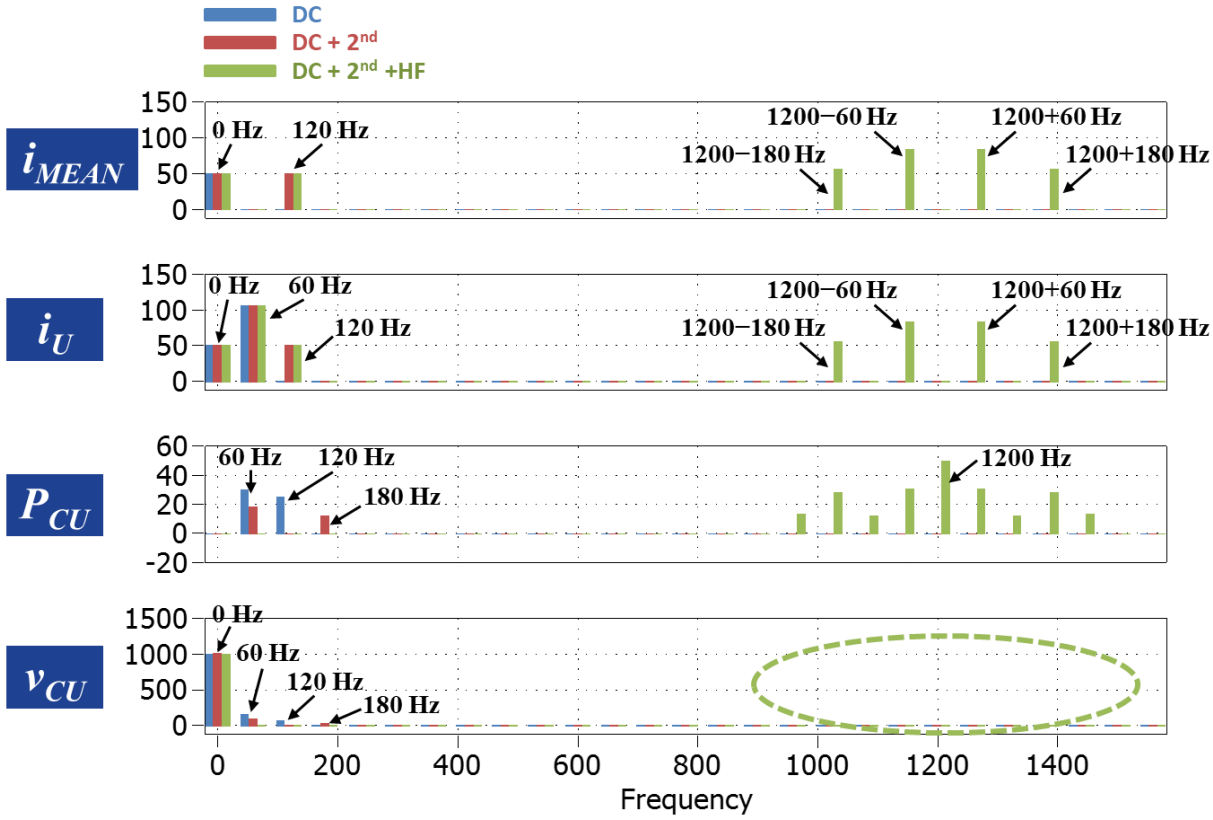


Figure 2-13 Harmonic spectrum comparison in different mean current patterns.

Chapter.3 Hybrid-Current Mode Switching-Cycle Control of MMC

3.1 Introduction

This chapter introduces a novel control approach that was inspired by the developed state-space switching model in Chapter 2. In the model, the capacitor voltage of a particular module at a given switching period is found to be determined by the phase current, mean current, and the switching functions. To decouple the capacitor voltages from the fundamental frequency and its harmonics, the extreme approach is to balance them at one switching period, named switching-cycle control (SCC). A similar concept of this proposal in the history is the “one-cycle control (OCC)” or “charge control” that was proposed in 1991 [C.1] -[C.5] . Implementing the OCC, the capacitor charging will be stopped when the capacitor voltage has reached a referenced value, achieving the capacitor voltage balancing within each switching cycle. The kernel philosophy of the SCC proposed in this chapter is also to balance the module capacitor voltage at each switching cycle. The OCC requires high-accuracy, high-bandwidth continuous sampling of the instant capacitor voltage values, which can be easily achieved in low-voltage DC-DC converters. Yet, it is unrealistic for the MV converters controller to sense a few volts on top of 1 kV offset voltage of module capacitors by a high-bandwidth isolated digital sensor. Another indirect means to control the capacitor voltage is to control the peak value of the inductor current

that charges the capacitors, which was widely recognized as the Peak-Current-Mode (PCM) control. Accordingly, PCM was implemented to regulate the arm current that charge and discharge the module capacitors. Combining the PCM and average-current-mode (ACM) that regulates the phase current, a hybrid-current-mode (HCM) control method is proposed to regulate all the state variables in the MMC.

3.2 Switching-Cycle Control

3.2.1 MMC Switching-Cycle Operation Fundamentals

Again, the topology configuration of the single-module-per-arm MMC is shown in **Figure 3-1**, where the module model in the dashed blue box is simplified into three elements, a capacitor represents the DC-link capacitor bank C, an SPDT switch S_U (S_L) that reflects the half-bridge configuration, and a lumped inductor L represents the total differential-mode and cable inductance. The upper module and the lower module are connected jointly at "PH" to form an MMC phase leg. "PH" is then connected to a large phase inductor L_O, a voltage source v_S, and then the middle point of the DC source voltage "m". This is a very basic single-phase MMC topology with only one module on the MMC arm.

The upper arm current that flows into the module AC terminal is defined as i_U, and the lower arm current is i_L. The phase current flowing through the phase inductor is i_{PH}. The upper capacitor voltage is v_{CU}, and the lower one is v_{CL}. The phase current i_{PH} is found to follow (3-1). The arithmetic mean value i_{MEAN} is still defined as (3-2)

(3-1) $$i_{PH} = i_U - i_L$$

(3-2) $$i_{MEAN} = \frac{i_U + i_L}{2}$$

An arithmetic mean value i_{MEAN} of the upper and lower arm current is defined as (3-2). Similarly, i_U and i_L can be expressed by i_{PH} and i_{MEAN} as (3-3) and (3-4).

(3-3) $$i_U = i_{MEAN} + \frac{i_{PH}}{2}$$

(3-4) $$i_L = i_{MEAN} - \frac{i_{PH}}{2}$$

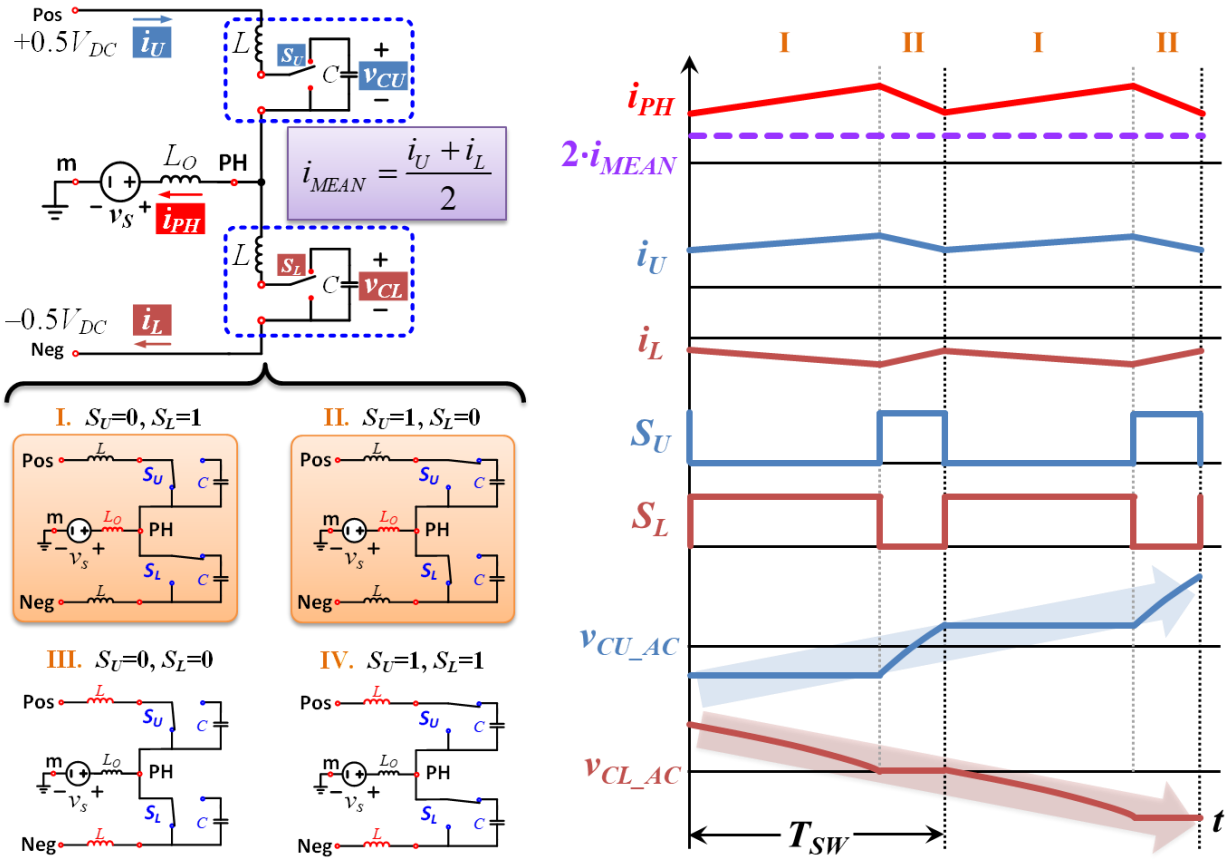


Figure 3-1 Fundamentals of the baisc MMC, by conventional controls

The phase current i_{PH} is determined by the load demand. The averaged value of i_{MEAN} represents the active power supplied from the DC source V_{DC}, which should balance the input and output active power. However, the AC component of i_{MEAN} is a degree of freedom that is controlled but meanwhile not affecting the phase current. i_U and i_L are calculated according to i_{MEAN} and i_{PH} values. The two capacitor dynamics are expressed as (3-5) and (3-6).

(3-5) $$\frac{dv_{CU}}{dt} = \frac{S_U}{C}\left(i_{MEAN} + \frac{i_{PH}}{2}\right)$$

(3-6) $$\frac{dv_{CL}}{dt} = \frac{S_L}{C}\left(i_{MEAN} - \frac{i_{PH}}{2}\right)$$

Where S_U and S_L are binary values defined as (3-7).

(3-7) $$S_{U(L)} = \begin{cases} 1, & \text{when SPDT is on the top throw} \\ 0, & \text{when SPDT is on the bottom throw} \end{cases}$$

When v_{CU} and v_{CL} are not bypassed, their dynamics are decided by i_{MEAN} and i_{PH}.

There are totally 4 states I, II, III, and IV as shown in the bottom-left circuits in Figure 9-2. In State I, S_U=0, and S_L=1, and the terminal "PH" voltage nearly equals to the positive DC bus. The right-hand side waveforms show that i_{PH} is controlled to increase, but the i_{MEAN} current almost does not change because the lower capacitor voltage V_{CL_DC} equals to the V_{DC}. i_U and i_L follow the trajectory that is defined by (3-3) and (3-4). The AC component of upper capacitor voltage V_{CU_AC} does not change as the upper capacitor is bypassed. As a contrast, the lower V_{CL_AC} is discharged as i_L is a negative value.

At the second stage of the waveforms where State II (S_U=1, and S_L=0) is applied, similar behaviors have been revealed that i_{PH} is controlled to decrease, and i_{MEAN} does not change because V_{CU_DC} equals to V_{DC}. V_{CL_AC} stays as it is since the lower capacitor is bypassed, while the upper capacitor AC components V_{CU_AC} increases.

The analysis reveals that State I and II are the key working states that regulate the phase inductor current i_{PH} to have a switching-cycle averaged value that meets the load demands. The phase inductor current demand could be a constant value in DC-DC operations (when v_S is a DC source), or a sinusoidal AC value at 60 Hz or other fundamental frequency in DC-AC operations (when v_S is an AC source), etc. The regulation is realized by controlling the duty cycle of S_U and S_L, and casting the State I and II alternatingly. During the two consecutive switching cycles in the figure, the upper and lower capacitor voltages are drifting towards unipolar directions. If the averaged i_{PH} is a DC value, the two capacitor voltages will drift away. If the i_{PH} is an AC value, the two capacitor voltages will drift and come back to complete a fundamental cycle.

However, the other two states, State III and IV, demonstrate complete different behaviors. In State III, S_U=0, S_L=0, the total across voltage on the two module inductors 2L equals to the DC bus voltage, so i_{MEAN} rises at a slope rate determined by V_{DC}/(2L), while the effect on the phase current is negligible. Conventionally, in order to avoid a large peak of i_{MEAN}, total arm inductance has to be much larger than the module inductance L when i_{MEAN} takes across voltage V_{DC}/2. In other cases such as the **Figure 3-2**, state III and IV are avoided to prevent sudden changes of i_{MEAN}. The AC ripple of i_{MEAN} is usually generated

by the capacitor voltage ripples at State I and II, rather than the influence from State III and IV.

Because of those MMC operation fundamentals, the module capacitance has to be designed very large to suppress the low-frequency ripple, which verifies the critical issue as discussed based on (3-8) in the previous chapter.

(3-8) $$v_{CU(L)\_AC} \propto \frac{I_{PH}}{f_0 \cdot C}$$

3.2.2 Proposal of Switching-Cycle Control

In order to resolve those issues, a new control approach named switching-cycle control (SCC) has been proposed. The vital concept is to take full advantage of the State III and IV that has been neglected in conventional control methods. The operation waveform is shown in **Figure 3-2**, where small total arm inductance is needed for fast control of i_{MEAN}. Between State I and State II, State IV is inserted, when $-V_{DC}/(2L)$ lead to a quick drop of the i_{MEAN}. i_U and i_L also drop accordingly until i_L reaches a negative peak value. The negative part of i_L discharges v_{CL_AC} to the initial value at the beginning of the switching period. On the other hand, v_{CU_AC} is charged by i_U during State IV where i_U is positive, and then discharged to the initial value by i_U during State II where i_U is negative. Finally, at State III the i_{MEAN} rises quickly by the effect of $V_{DC}/(2L)$, and i_U and i_L are reset back to the initial value. The phase current i_{PH} is still controlled to make sure its switching-cycle averaged value follows the load demand, despite that a small portion of the effective control time has been taken by State and IV and III.

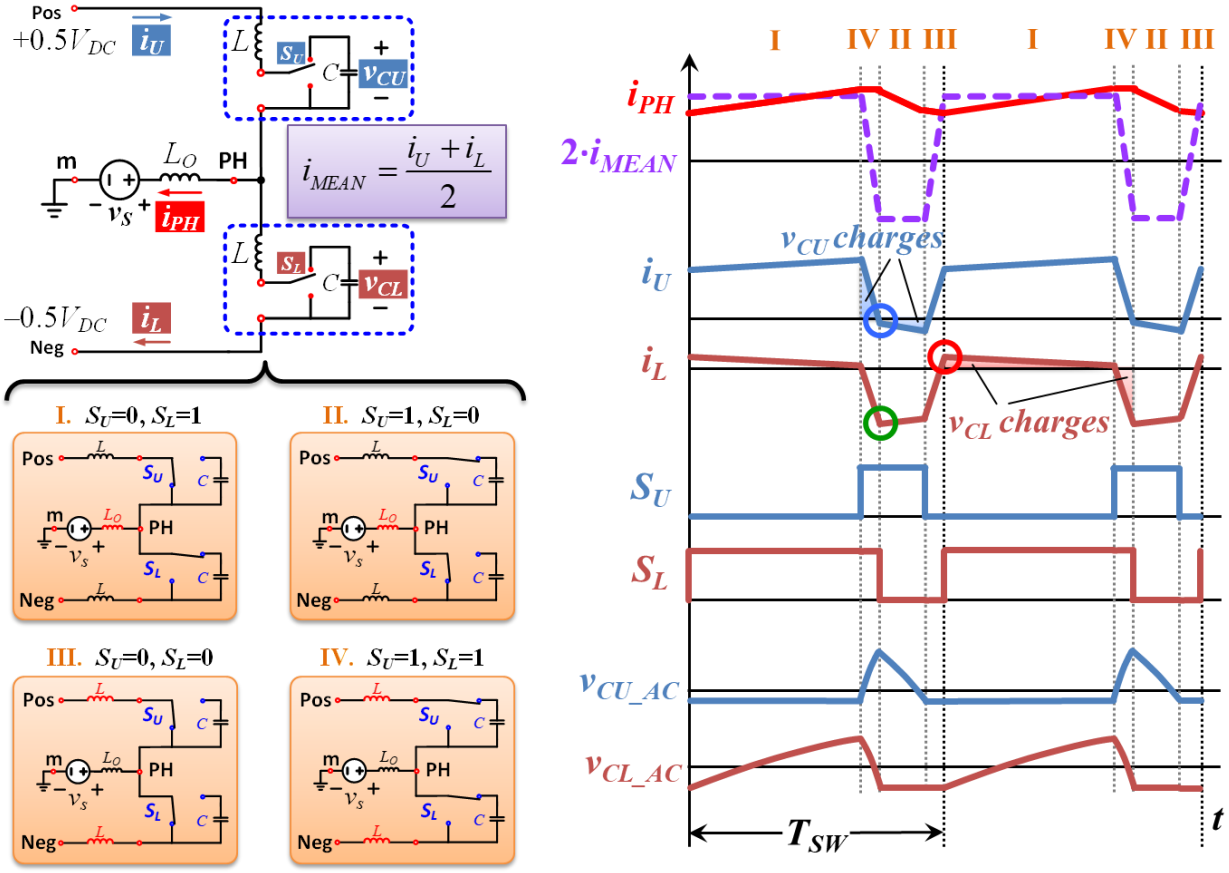


Figure 3-2 Fundamentals of single-PEBB MMC, by switching-cycle control

As the polarity of the arm currents i_U and i_L are changing every switching cycle, zero-voltage switching (ZVS) turn-on of every SiC MOSFET is realized. **Figure 3-3** shows the single-phase MMC with upper MOSFET S_{1U} and S_{2U}, and lower MOSFET S_{1L} and S_{2L}. Their drain-source voltage V_{DS1U}, V_{DS2U}, V_{DS1L}, and V_{DS2L} have been discharged to zero by the two arm currents before the rising edge of their gate command g_{S1U}, g_{S1U}, g_{S1L} and g_{S1L}. Therefore, zero turn-on losses are expected, which is very desirable for SiC MOSFETs.

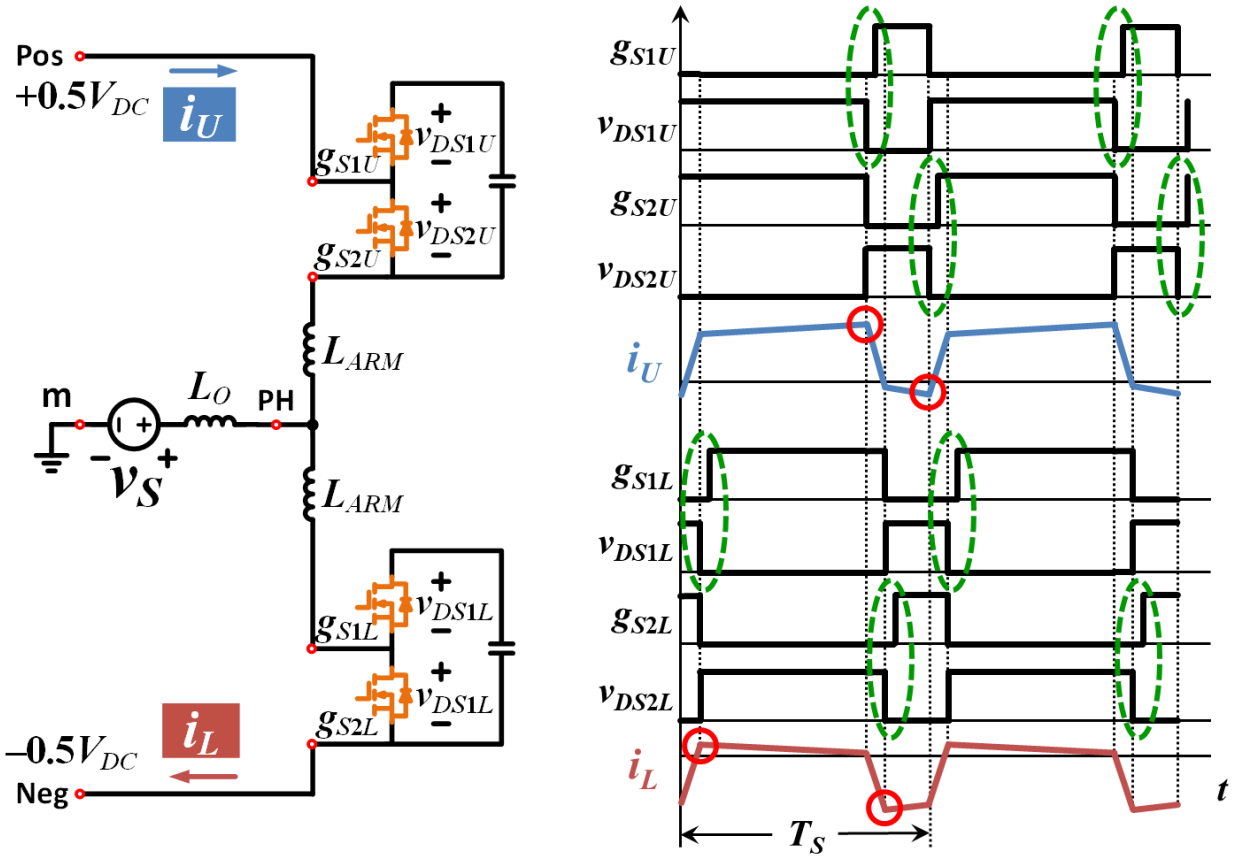


Figure 3-3 ZVS turn-on of all the four SiC MOSFETs in SCC

3.2.3 Extension of Switching-Cycle Control to multiple PEBBs

The SCC can be extended to the situations when the phase current is negative by inserting state IV instead of III before state I, and similarly putting state III before state II. It can also be directly extended to the three-phase case if a common DC-link capacitor is in the circuit for all three phases. All the mean currents needed in the SCC for the three phases will be provided by the DC-link capacitor. When the situation comes to multi-module per arms, a simply extended method of the SCC is proposed in **Figure 3-4**, taking a two-module-per-arm case as an example. The method is still to introduce the states that can quickly change the arm currents such that the capacitor voltages can be brought to the reference at the next time interval. Assuming again that the phase current is in its positive half cycle, short delays are introduced at every edge of the two lower module switches. If a proper delay is placed at "*a*" on S_{L1}, then the capacitor voltage of v_{CL2} can resonate back to the reference voltage where an arrow of "*a*" is point toward. Afterward, the capacitor voltage v_{CL2} can stay at the reference voltage when the capacitor is bypassed. Similar mechanisms work well with the delays where "*b*", "*c*" and "*d*" are labeled.

As observed from the **Figure 3-4**, the initial values of capacitor voltages are no longer at the reference because the capacitor voltages will be influenced by the arm current when it is attempting to balance the other capacitor voltages. In order to analyze the resonant interactions among the multiple capacitors and the two arm inductors in one phase-leg, mathematical solutions are required.

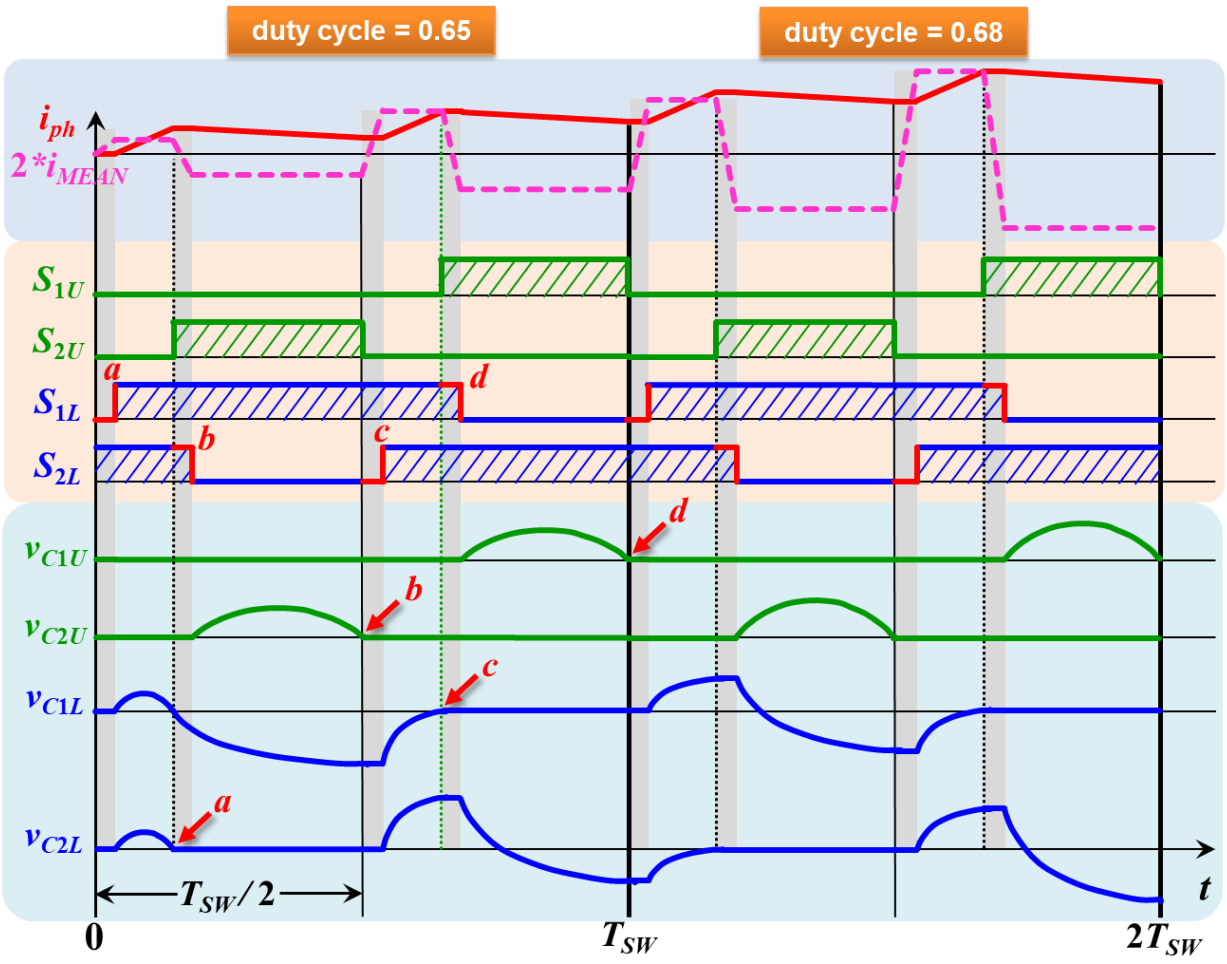


Figure 3-4 The Switching-Cycle Control in two-module-per-arm case

3.3 Open-Loop Simulation: Model-Predictive Switching Cycle Control

3.3.1 Resonant behavior analysis

The most important part of the SCC is how to determine the arm current or the mean current that need to be charged during State IV and III, so that the capacitor voltage can be balanced during State I and II. In State I and II of the SCC control mode, the arm inductors, phase inductor, and the module capacitors are resonating which determines the end value of the capacitor voltage, with given initial values including the mean current and capacitor voltage. Therefore, understanding the resonant behavior is one way to calculate the charging values of mean current during State VI and III.

By re-organizing the state space equations with more detailed voltage source information of a single-phase, single-module MMC, the inductor current and arm voltage state equations are given. **Figure 3-5** shows State I when S_U=0 and S_L=1, where the arm voltages v_U and v_L are defined as (3-9). Accordingly, the state equations become (3-10), in which all the variables are instantaneous functions of time without any averaging operations.

(3-9) $$v_U = S_U \cdot v_{CU},\ v_L = S_L \cdot v_{CL}$$

(3-10)

$$\frac{d}{dt}\begin{bmatrix} i_U \\ i_L \\ v_U \\ v_L \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\dfrac{1}{L_2} \\ 0 & 0 & 0 & -\dfrac{1}{L_1} \\ 0 & 0 & 0 & 0 \\ 0 & \dfrac{1}{C} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_U \\ i_L \\ v_U \\ v_L \end{bmatrix} + \begin{bmatrix} \dfrac{0.5V_{dc}}{L} - \dfrac{V_S \sin\left(\omega_0 t + 2\pi \cdot k/CR\right)}{2L_O + L} \\ \dfrac{0.5V_{dc}}{L} + \dfrac{V_S \sin\left(\omega_0 t + 2\pi \cdot k/CR\right)}{2L_O + L} \\ 0 \\ 0 \end{bmatrix}$$

CR is carrier ration, $k = 0, 1, 2, \ldots, CR\text{-}1$.

Similarly, referring to **Figure 3-6**, the state question for State II is derived as (3-11)

(3-11)

$$\frac{d}{dt}\begin{bmatrix} i_U \\ i_L \\ v_U \\ v_L \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{1}{L_1} & 0 \\ 0 & 0 & -\dfrac{1}{L_2} & 0 \\ \dfrac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_U \\ i_L \\ v_U \\ v_L \end{bmatrix} + \begin{bmatrix} \dfrac{0.5V_{dc}}{L} - \dfrac{V_S \sin\left(\omega_0 t + 2\pi \cdot k/CR\right)}{2L_O + L} \\ \dfrac{0.5V_{dc}}{L} + \dfrac{V_S \sin\left(\omega_0 t + 2\pi \cdot k/CR\right)}{2L_O + L} \\ 0 \\ 0 \end{bmatrix}$$

CR is carrier ration, $k = 0, 1, 2, \ldots, CR\text{-}1$.

By solving (3-10) and (3-11), the time-domain responses of capacitors voltages and arm currents can be derived.

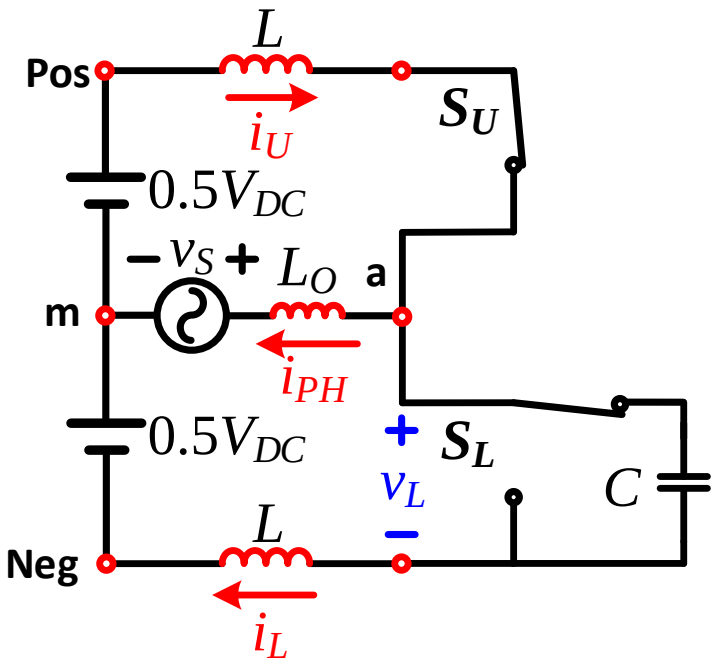


Figure 3-5 Single-phase single-module MMC Topology during State I

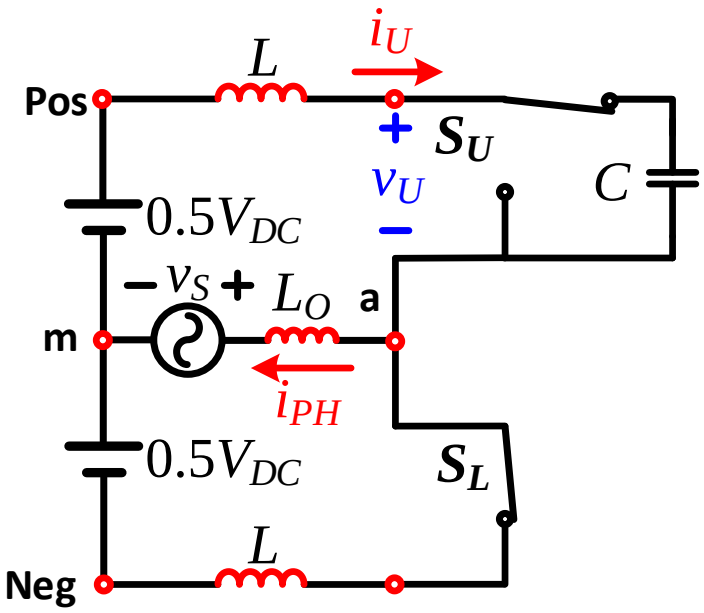


Figure 3-6 Single-phase single-module MMC Topology during State II

This approach can be extended to calculate all the state variables when the module number N is larger than 1. At a given switching cycle, in the switching states where no fast mean current occurs, the number of modules that are connected or bypassed has been predestined, so the N_U and N_L are given according to (3-12). Then the voltage state variables are defined in (3-13).

(3-12) $$N_U = \sum_{i=1}^{N} S_{Ui},\ N_L = \sum_{i=1}^{N} S_{Li}$$

(3-13) $$v_U = \sum_{i=1}^{N} S_{Ui} \cdot v_{CUi},\ v_L = \sum_{i=1}^{N} S_{Li} \cdot v_{CLi}$$

(3-14) $$\frac{1}{C_U} = \frac{N_U}{C},\ \frac{1}{C_L} = \frac{N_L}{C}$$

(3-15) $$L_1 = \frac{L\left(2L_O + L\right)}{L_O + L},\ L_2 = \frac{L\left(2L_O + L\right)}{L_O}$$

With expressions of (3-14) and (3-15), the state equations are in (3-16).

(3-16) $$\frac{d}{dt}\begin{bmatrix} i_U \\ i_L \\ v_U \\ v_L \end{bmatrix} = \mathbf{A}\begin{bmatrix} i_U \\ i_L \\ v_U \\ v_L \end{bmatrix} + \begin{bmatrix} \frac{0.5V_{dc}}{L} - \frac{V_S \sin\left(\omega_0 t + 2\pi \cdot k/CR\right)}{2L_O + L} \\ \frac{0.5V_{dc}}{L} + \frac{V_S \sin\left(\omega_0 t + 2\pi \cdot k/CR\right)}{2L_O + L} \\ 0 \\ 0 \end{bmatrix}$$

where the matrix A is determined by whether N_U or N_L equals to zero as defined in **Figure 3-7**. A two-module-per-arm example is shown to illustrate the categorization.

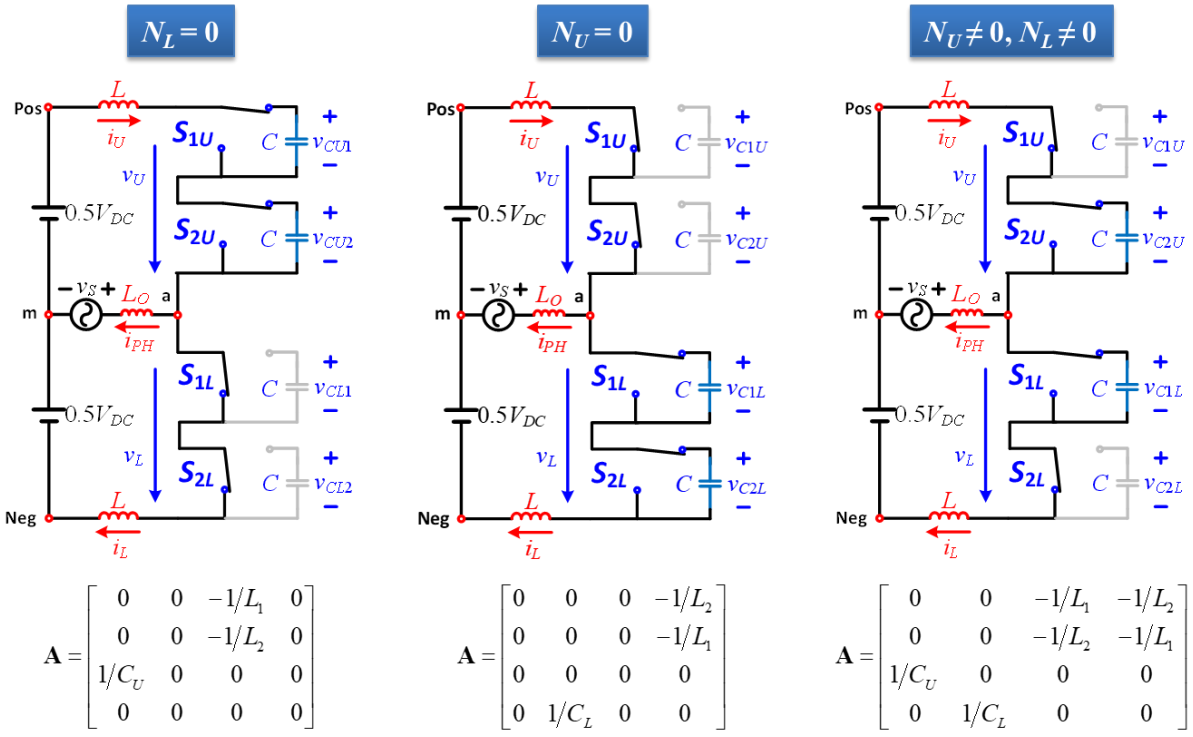


Figure 3-7 Matrix A definition

The solution of state equation (3-16) is shown in (3-19) and (3-20), where the two arm currents i_U and i_L are given. The approximation of the two resonant frequencies ω_{r1} and ω_{r2} are shown in (3-17) and (3-18), indicating the physical meaning of the resonant behavior of capacitors and inductors. The comparatively faster resonance in (3-17), that is, between the series of the two equivalent arm capacitors and the series of the two arm inductors, determines the basic behaviors of the circuit, where the lower frequency resonance and the fundamental component in (3-18) have minor but not negligible impact on the time-domain response.

With the derived two arm current expressions, any capacitor voltage response can be calculated during the time interval by capacitor charging equations. They can be used to solve the initial arm current value that is needed to balance the capacitor voltages. Meanwhile, when the control is trying to balance one capacitor, the impact that the other capacitors that are influenced can also be derived.

(3-17)

$$\omega_{r1} = \sqrt{\frac{C_U + C_L}{2C_U C_L L_1} + \frac{\sqrt{C_L{}^2 L_2{}^2 + 4C_U C_L L_1{}^2 - 2C_U C_L L_2{}^2 + C_U{}^2 L_2{}^2}}{2C_U C_L L_1 L_2}}$$

$$\approx \sqrt{\frac{1}{2L}\left(\frac{1}{C_U} + \frac{1}{C_L}\right)}$$

(3-18)

$$\omega_{r2} = \sqrt{\frac{C_U + C_L}{2C_U C_L L_1} - \frac{\sqrt{C_L{}^2 L_2{}^2 + 4C_U C_L L_1{}^2 - 2C_U C_L L_2{}^2 + C_U{}^2 L_2{}^2}}{2C_U C_L L_1 L_2}}$$

$$\approx \sqrt{\frac{1}{4L_O}\left(\frac{1}{C_U} + \frac{1}{C_L}\right)}$$

(3-19)

$$
\begin{aligned}
i_U = &\left(\begin{array}{l}\dfrac{\omega_0 V_S \cos(2\pi\cdot k/CR)}{(\omega_{r1}^{\ 2}-\omega_0^{\ 2})(2L_O+L)}\left(\dfrac{1}{2}+\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}-\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ +\dfrac{I_{U0}}{2}+\dfrac{(C_L-C_U)I_{U0}}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}+\dfrac{I_{L0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\end{array}\right)\cdot\cos(\omega_{r1}t)+\left(\begin{array}{l}\dfrac{\omega_0 V_S \cos(2\pi\cdot k/CR)}{(\omega_{r2}^{\ 2}-\omega_0^{\ 2})(2L_O+L)}\left(\dfrac{1}{2}-\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}+\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ +\dfrac{I_{U0}}{2}-\dfrac{(C_L-C_U)I_{U0}}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}-\dfrac{I_{L0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\end{array}\right)\cdot\cos(\omega_{r2}t)\\
&\left(\begin{array}{l}-\dfrac{0.5V_{dc}}{\omega_{r1}L}\left(\dfrac{1}{2}+\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}+\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ -\dfrac{\omega_{r1}V_S\sin(2\pi\cdot k/CR)}{(\omega_{r1}^{\ 2}-\omega_0^{\ 2})(2L_O+L)}\left(-\dfrac{1}{2}-\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}+\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ -\dfrac{\omega_{r1}C_UV_{U0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_1}+\dfrac{\omega_{r1}V_{L0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})L_2}+\dfrac{\omega_{r1}^{\ 3}C_UV_{U0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})}\end{array}\right)\cdot\sin(\omega_{r1}t)-\left(\begin{array}{l}-\dfrac{0.5V_{dc}}{\omega_{r2}L}\left(\dfrac{1}{2}-\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}-\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ -\dfrac{\omega_{r2}V_S\sin(2\pi\cdot k/CR)}{(\omega_{r2}^{\ 2}-\omega_0^{\ 2})(2L_O+L)}\left(-\dfrac{1}{2}+\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}-\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ +\dfrac{\omega_{r2}C_UV_{U0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_1}-\dfrac{\omega_{r2}V_{L0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})L_2}-\dfrac{\omega_{r2}^{\ 3}C_UV_{U0}}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})}\end{array}\right)\cdot\sin(\omega_{r2}t)\\
&+\frac{\omega_0 V_S}{(2L_O+L)}\left(\begin{array}{l}\left(\dfrac{1}{\omega_{r1}^{\ 2}-\omega_0^{\ 2}}\right)\left(-\dfrac{1}{2}-\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}+\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\\ +\left(\dfrac{1}{\omega_{r2}^{\ 2}-\omega_0^{\ 2}}\right)\left(-\dfrac{1}{2}+\dfrac{(C_L-C_U)}{2(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_UC_LL_1}-\dfrac{1}{(\omega_{r1}^{\ 2}-\omega_{r2}^{\ 2})C_LL_2}\right)\end{array}\right)\cdot\cos(\omega_0 t+2\pi\cdot k/CR)
\end{aligned}
$$

(3-20)

$$
i_L = \left(\begin{array}{l}
\left(\begin{array}{l} \dfrac{\omega_0 V_S \cos(2\pi \cdot k/CR)}{(\omega_{r1}^{\ 2} - \omega_0^{\ 2})(2L_O + L)} \left(-\dfrac{1}{2} - \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} + \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ + \dfrac{I_{L0}}{2} + \dfrac{(C_U - C_L) I_{L0}}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} + \dfrac{I_{U0}}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \end{array} \right) \cdot \cos(\omega_{r1} t) + \\
\left(\begin{array}{l} \dfrac{\omega_0 V_S \cos(2\pi \cdot k/CR)}{(\omega_{r2}^{\ 2} - \omega_0^{\ 2})(2L_O + L)} \left(-\dfrac{1}{2} + \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} - \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ + \dfrac{I_{L0}}{2} - \dfrac{(C_U - C_L) I_{L0}}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} - \dfrac{I_{U0}}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \end{array} \right) \cdot \cos(\omega_{r2} t) \\
\left(\begin{array}{l} -\dfrac{0.5 V_{dc}}{\omega_{r1} L} \left(\dfrac{1}{2} + \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} + \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ - \dfrac{\omega_{r1} V_S \sin(2\pi \cdot k/CR)}{(\omega_{r1}^{\ 2} - \omega_0^{\ 2})(2L_O + L)} \left(\dfrac{1}{2} + \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} - \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ + \dfrac{\omega_{r1} V_{U0}}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) L_2} + \dfrac{\omega_{r1} C_L V_{L0}}{2} - \dfrac{\omega_{r1} (C_L - C_U) V_{L0}}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_1} \end{array} \right) \cdot \sin(\omega_{r1} t) - \\
\left(\begin{array}{l} -\dfrac{0.5 V_{dc}}{\omega_{r2} L} \left(\dfrac{1}{2} - \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} - \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ - \dfrac{\omega_{r2} V_S \sin(2\pi \cdot k/CR)}{(\omega_{r2}^{\ 2} - \omega_0^{\ 2})(2L_O + L)} \left(\dfrac{1}{2} - \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} + \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ - \dfrac{\omega_{r2} V_{U0}}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) L_2} + \dfrac{\omega_{r2} C_L V_{L0}}{2} + \dfrac{\omega_{r2} (C_L - C_U) V_{L0}}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_1} \end{array} \right) \cdot \sin(\omega_{r2} t) \\
+ \dfrac{\omega_0 V_S}{(2L_O + L)} \left(\begin{array}{l} \left(\dfrac{1}{\omega_{r1}^{\ 2} - \omega_0^{\ 2}} \right) \left(\dfrac{1}{2} + \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} - \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \\ + \left(\dfrac{1}{\omega_{r2}^{\ 2} - \omega_0^{\ 2}} \right) \left(\dfrac{1}{2} - \dfrac{(C_U - C_L)}{2(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U C_L L_1} + \dfrac{1}{(\omega_{r1}^{\ 2} - \omega_{r2}^{\ 2}) C_U L_2} \right) \end{array} \right) \cdot \cos(\omega_0 t + 2\pi \cdot k/CR)
\end{array} \right)
$$

3.3.2 Model-predictive control

It is well known that there always exists one/half switching-cycle delay in the digital control system depending on how frequent the modulator reference is updated. This fundamentally restrains the application of the SCC. For instance, in a one-cycle delay control system, because the state variables value are sampled at the beginning of T_{SW1}, and will be used for the control at T_{SW2}, referred to **Figure 3-8**. In order to address this issue, the prediction of the state variables' dynamics is necessary for the SCC. Therefore, the Model-Predictive Switching-Cycle Control (MP-SCC) is applied, and it comprises two steps.

Firstly, the state variable values at the end of T_{SW1} is calculated based on the data sampled at the beginning of T_{SW1} and the time duration of each switching scenarios given at the previous cycle, by using either the given time-domain solutions (3-19) and (3-20), or the differential state-space switching model (D-SSSM) with Euler Approximation in (2-20). The D-SSSM given for the three-phase MMC is an accurate model derived with KCL and KVL, as long as the iteration step is sufficiently short. In the comparison of the two prediction approaches, the three-phase D-SSSM is more accurate as it considers the circulating interactions between the three phases and the common mode voltage between the neutral and the DC middle point. However, despite the approximations, the single-phase time-domain solution (3-19) and (3-20) is sufficiently correct for the state variable prediction and saves a large amount of the computation efforts.

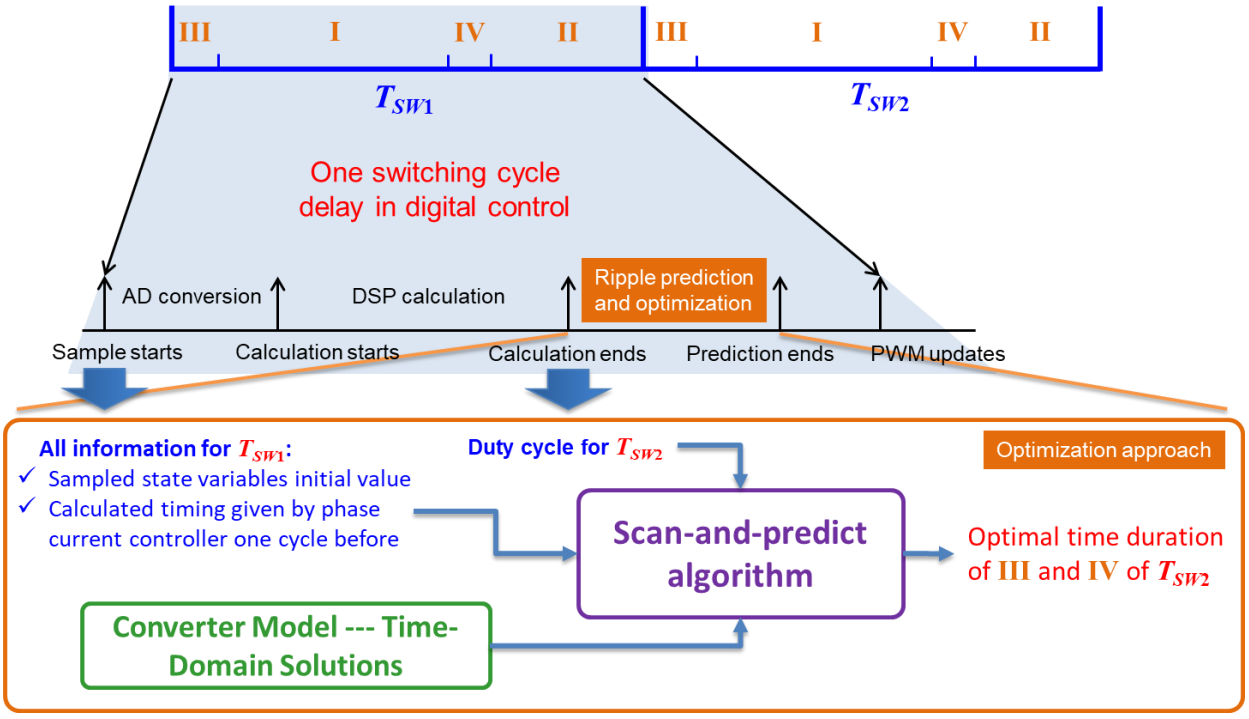


Figure 3-8 Principle of the model-predictive switching-cycle control

The second step is to determine the time duration of all the switching scenarios, for instance, the State III, I, IV and II. The try-and-error method is borrowed for the prediction of the best solution. With the existence of the outer averaged phase-current loop, the duty cycle after delay compensation is already obtained for the cycle T_{SW2}. So the original time duration of State I and II in conventional control method can be calculated. Then as the time for the State III and IV are both short delays limited within 15 μs due to the very small arm inductance, 1 μs time step is set to scan for the best State III. Using the time-domain solutions, the capacitor voltage v_L at the end of State III can be calculated. By trying different lengthes of State III, the optimal time for that meet the criteria that $(v_L\text{-}V_{Lref})^2$ reaches its minimum value, and then the length of State III and the modified length of State I against its original value are determined. Afterward, all the state variable values at the end of State I by the time-domain solutions, which will be used for the next prediction of time interval State IV. Finally, the similar approach can be implemented for obtaining the optimal length of State IV to achieve the minimum $(v_U\text{-}V_{Uref})^2$ value. The detailed flow chart of the MP-SCC is shown in **Figure 3-9**.

Need to notice that due to the insertion of State III and IV, the originally calculated duty cycles could be slightly changed, and thus proper compensation need to be made after the time durations of State III and IV are determined. As they are very short, the duty cycle only needs to be slightly changed before it is given to the modulator, which has very little change in the state variable responses since their resonant frequencies are much longer than the time length of State III and IV.

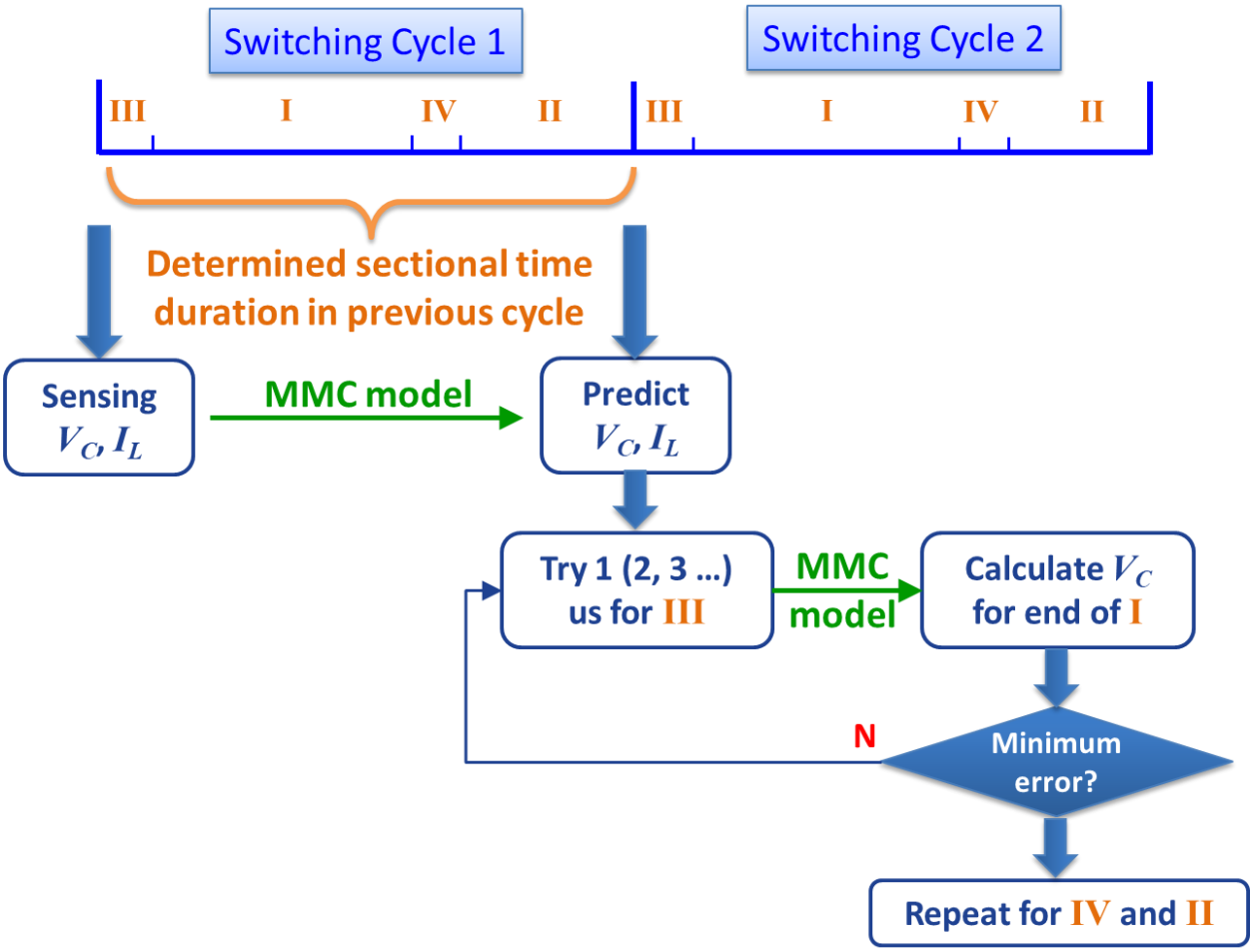


Figure 3-9 Principle of model-predictive switching-cycle control

The parameters of the simulation example are shown in **Table 3-1**. The simulation results for the 60 Hz line frequency case are shown in **Figure 3-10**. The line current is controlled to follow the current requirement as specified. There are quite a number of intermediate voltages levels (±500V, ±1500V) caused by the newly used states, shown on the line-to-line voltage v_{ab} waveform. In the SCC the duty cycle is still maintained as it was originally required for the averaged line current control, and thus there is actually no low order harmonic distortions on the line-to-line voltage. Therefore, there is no low-frequency distortion occurring on the phase current as shown at the top of the figures. The sum current are controlled to indirectly regulate the cell capacitor voltages to ensure that at the end of each switching cycle the capacitor voltage will go back to the reference voltage, 1 kV in this case. **Figure 3-11** demonstrates that the SCC nearly eliminates the dependency on the line frequency to balance the cell capacitor voltages when the line frequency is 1 Hz. The capacitor voltage ripples are almost the same as the 60 Hz case, and there are actually no low order harmonic distortions on the line-to-line voltage either. As observed in the specification, the capacitance value is 400 μF and the arm inductance value is 20 μH, which is significantly reduced compared to the conventional case where 4 mF capacitance and 1 mH arm inductance are needed to achieve the same capacitor voltage ripples.

Although the simulation demonstrates the effectiveness of MP-SCC, it relies on accurate converter model including parasitics, accurate sampling time, and an extremely powerful computation unit. This solution is suitable for the analysis of the operational behavior of SCC, but not friendly for a practical hardware test.

Table 3-1 Converter Specifications in Simulations

Property	Value
Apparent power	200 kVA
Power factor	Unity
Line-to-line grid voltage	1140 V
Line current	150 A
DC-bus voltage	2000 V
Module count per arm	2
Module DC-link voltage	1000 V
Module DC-link voltage ripple	-50 V ~ +50 V
Capacitance in each module	500 μF
Arm inductance	20 μH
Line inductance	2000 μH
Line frequency	60 Hz and 1 Hz
Switching frequency	2 kHz

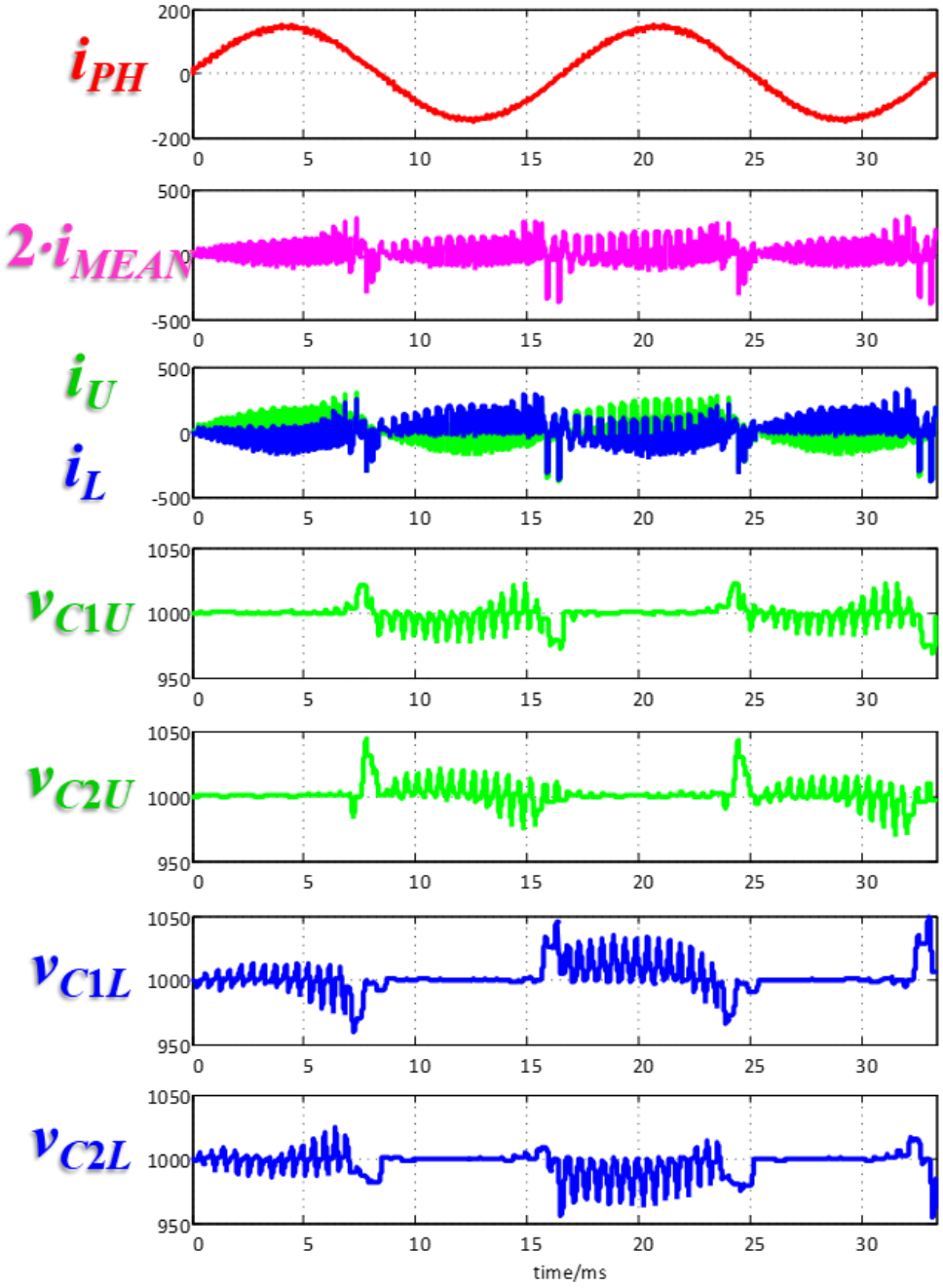


Figure 3-10 Simulation waveforms of two-module-per-arm MMC with MP-SCC, f_0=60 Hz

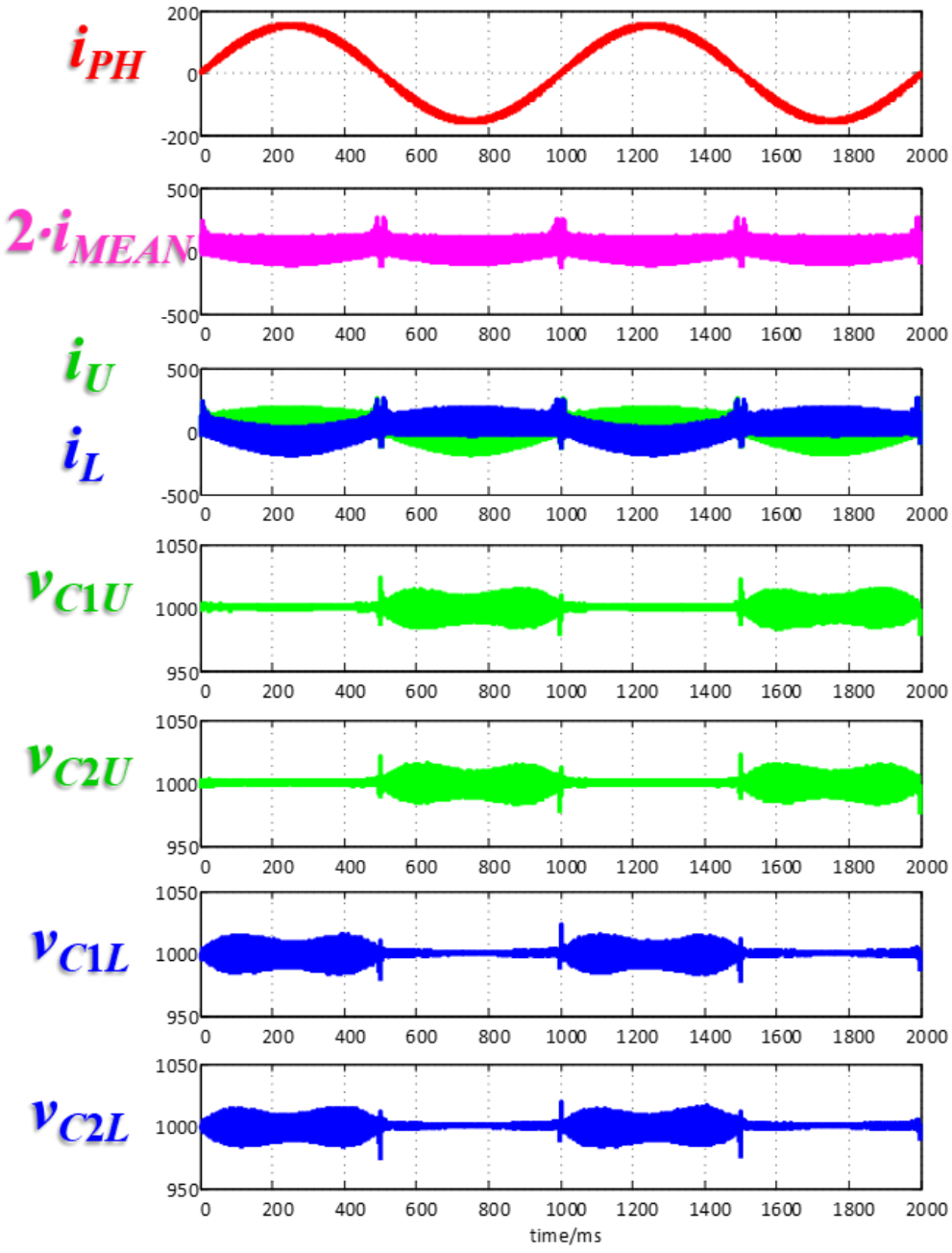


Figure 3-11 Simulation waveforms of two-module-per-arm MMC with MP-SCC, f_0=1 Hz

3.4 Closed-Loop Realization: Hybrid-Current-Mode Switching-Cycle Control

3.4.1 Fundamentals

The most critical step of the SCC is how to determine the time length of State IV and III in every switching period to balance the two capacitor voltage. As marked on i_U in **Figure 3-2**, the positive and negative charges accumulated in the blue area should be equal to zero so that v_{CU_AC} is balanced within this switching period. The start time of State IV is the rising edge of S_U. The end time is the turning point of i_U in the blue circle, which is also aligned with the turning point of i_L in the green circle, as well as the falling edge of S_L. Assuming the rising edge of S_U is pre-set, if the falling edge of S_L comes later, the turning point of i_L in the green circle (and of i_U in the blue circle) becomes more negative, and then the v_{CU_AC} is discharged more than charged in that period. On the contrary, if the falling edge of S_L comes earlier, v_{CU_AC} will be increased.

Similarly, the positive and negative charges accumulated in the red area should be equal to zero so that v_{CL_AC} is balanced within this switching period. The start time of State III is the falling edge of S_U. The end time is the turning point of i_L in the red circle, aligned with the rising edge of S_L. Assuming the falling edge of S_U is pre-set, if the rising edge of S_L comes later, the turning point of i_L becomes more positive, and then the v_{CL_AC} is charged more than discharged. At the end of this switching cycle, v_{CL_AC} will be increased. If the rising edge of S_L comes earlier, v_{CL_AC} will be decreased.

Based on the SCC behaviors, when the rising and falling edge of S_U is pre-set, it is natural to use the turning points in green and red circles to determine the falling and rising edge of S_L, respectively. Furthermore, the duty cycle of S_U controls the switching-cycle averaged value of phase current i_{PH}. Longer "low" time of S_U increases the averaged i_{PH}, and longer "high" time decrease the averaged i_{PH}. Accordingly, the block diagram of a closed-loop SCC realization is proposed in **Figure 3-12**. Two controller units are applied for the upper and lower module, respectively.

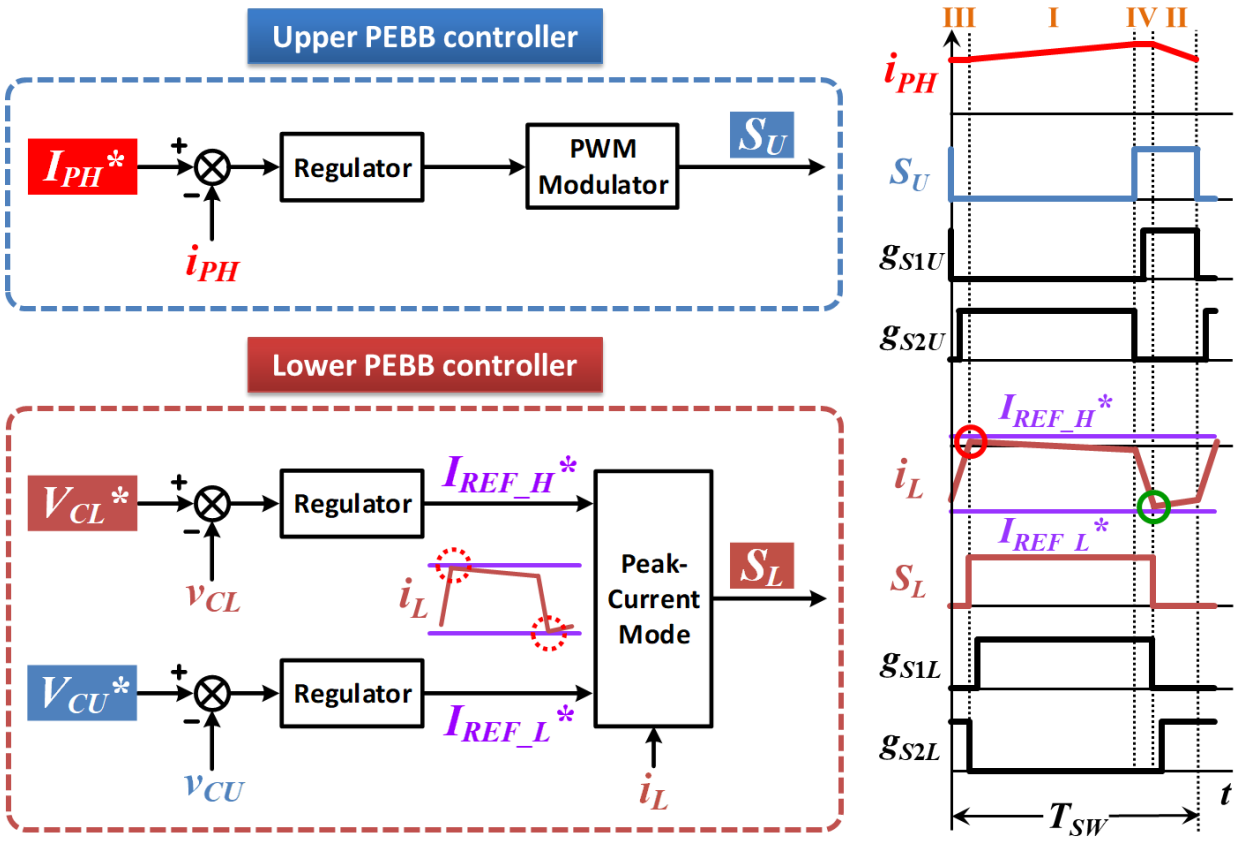


Figure 3-12 Control block diagram of the closed-loop HCM-SCC

The upper module is responsible for regulating the averaged phase current. The phase current error $I_{PH}^{*}-i_{PH}$ signal is fed to a regulator that generates a modulation reference. The reference is given to a pulse-width modulator that generates S_U. After a logic inverter and dead-time generators, the gate signals g_{S1U} and g_{S2U} are generated and sent to the half-bridge gate driver board. This mechanism is the conventional average-current-mode (ACM) control.

The lower module is responsible for regulating the upper and lower averaged capacitor voltages. The averaged voltage error $V_{CL}^{*}-v_{CL}$ of the lower capacitor at the outer loop is fed to a regulator that generates a high reference current $I_{REF\_H}^{*}$ for the inner loop. The averaged voltage error $V_{CU}^{*}-v_{CU}$ of the upper capacitor at the outer loop is fed to a regulator that generates a low reference current $I_{REF\_L}^{*}$ for the inner loop. The two current boundaries define a band area that limits the lower arm current i_L. As soon as i_L touches $I_{REF\_H}^{*}$, S_L generates a rising edge to transit the switching states from III to I with a turning point, which is realized by giving g_{S2L} a "turn-off" command. As soon as i_L touches $I_{REF\_L}^{*}$, S_L generates a falling edge to transit the switching states from IV to II with a turning point, which is realized by giving g_{S1L} a "turn-off" command. The rising edges g_{S1L} and g_{S2L} are produced by dead-time generators. This "compare and turn-off" mechanism of the inner current loop is conventionally named peak-current-mode (PCM) control.

As this closed-loop SCC realization combines the conventional ACM and PCM controls for the upper and lower arms, respectively, it is named hybrid-current-mode switching-cycle control (HCM-SCC). Three strong correlations built the foundation of

HCM-SCC. First of all, the averaged phase current i_{PH} has a strong negative correlation with the upper duty cycle d_U (averaged value of S_U). Secondly, the averaged lower capacitor voltage v_{CL} has a strong positive correlation with the high reference current I_{REF_H}*. The third one is that average voltage v_{CU} of the upper capacitor has a strong positive correlation with the low reference current I_{REF_L}*. However, some weak coupling between the two voltage loops may have potential influences on the control performance. According to **Figure 3-2**, v_{CL} has a weak positive correlation with the low reference current I_{REF_L}*, and v_{CU} has a weak positive correlation with the low reference current I_{REF_H}*. Unfortunately, small-signal modeling and stability analysis on HCM-SCC has not been conducted in this research, those effects will be studied in the future work.

Due to the fact that the di/dt rate of i_L is very high during State III and IV, overcurrent can occur when the two reference current I_{REF_H}* and I_{REF_L}* are not calculated correctly resulting in the PCM comparison failure. Therefore, limiters are necessary to prevent overcurrent from happening. A reference current limiter and a State-III/IV time limiter, are placed in the controller software. Each reference current has one maximum and one minimum values, and the time for State III/ IV has one maximum value, too. In practice, the way to measure the time duration of State III/ IV is critical. As S_L is generated based on S_U, it must be ensured that the PCM controller is informed of S_U from the ACM controller, so that a time counter can start from the rising and falling edge of S_U, and activate PCM control forcedly as soon as the time duration reaches the maximum value.

3.4.2 Simulation results

The steady-state DC-DC mode simulation result is shown in **Figure 3-13**. The converter is operating at 1 kV DC bus voltage, 150 A phase current, 21 kHz switching frequency. The passive parameters are 50 μH PEBB capacitance, 5 μH arm inductance, and 250 μH phase inductance. The two arm currents i_U and i_L are pulsating at the switching frequency. The capacitor charging power P_{CU} and P_{CL} reach their peaks at State III and IV. The capacitor voltage v_{CU} and v_{CL} are balanced every switching cycle.

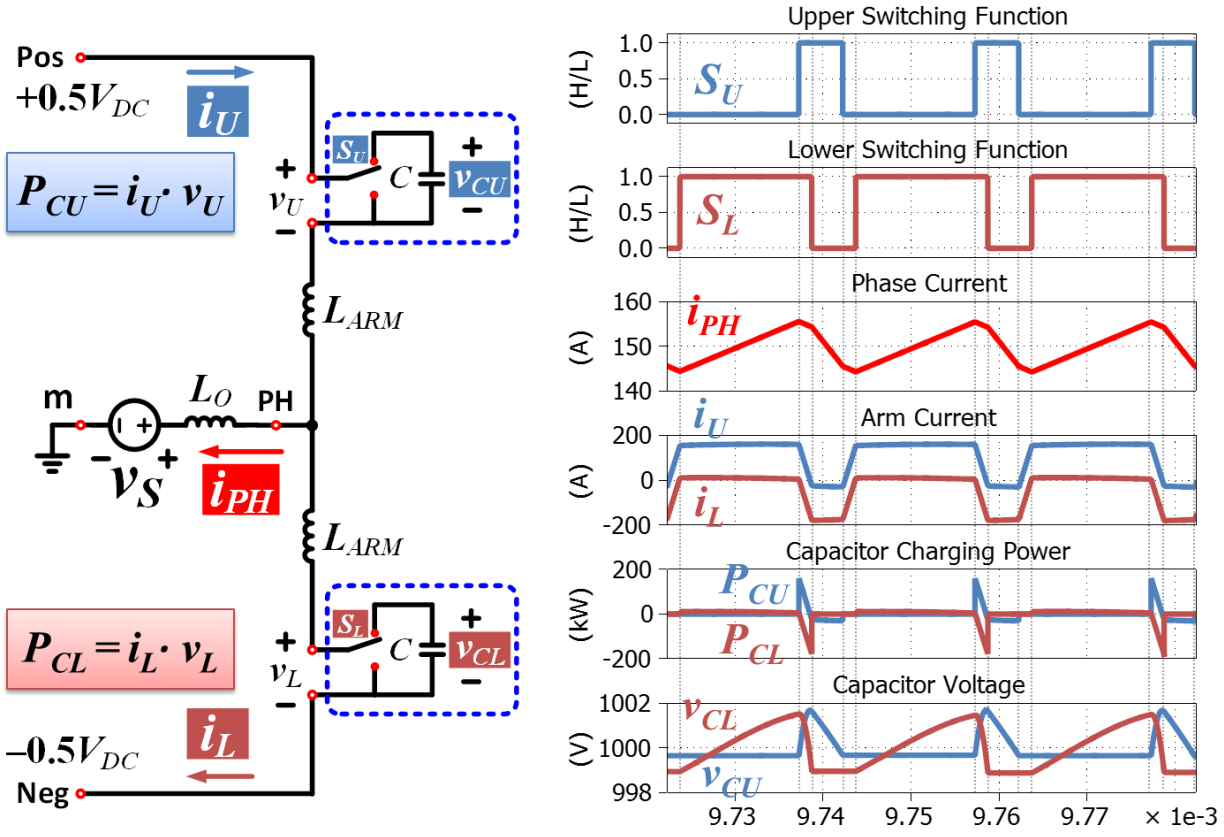


Figure 3-13 Simulation results of the steady-state HCM-SCC in DC-DC mode

The start-up simulation result is shown in **Figure 3-14**. The phase current i_{PH} is regulated by the closed-loop HCM-SCC, and the capacitor voltage is also well controlled. The start-up dynamic time is about 4 ms and the overshoots are within the safety range of components.

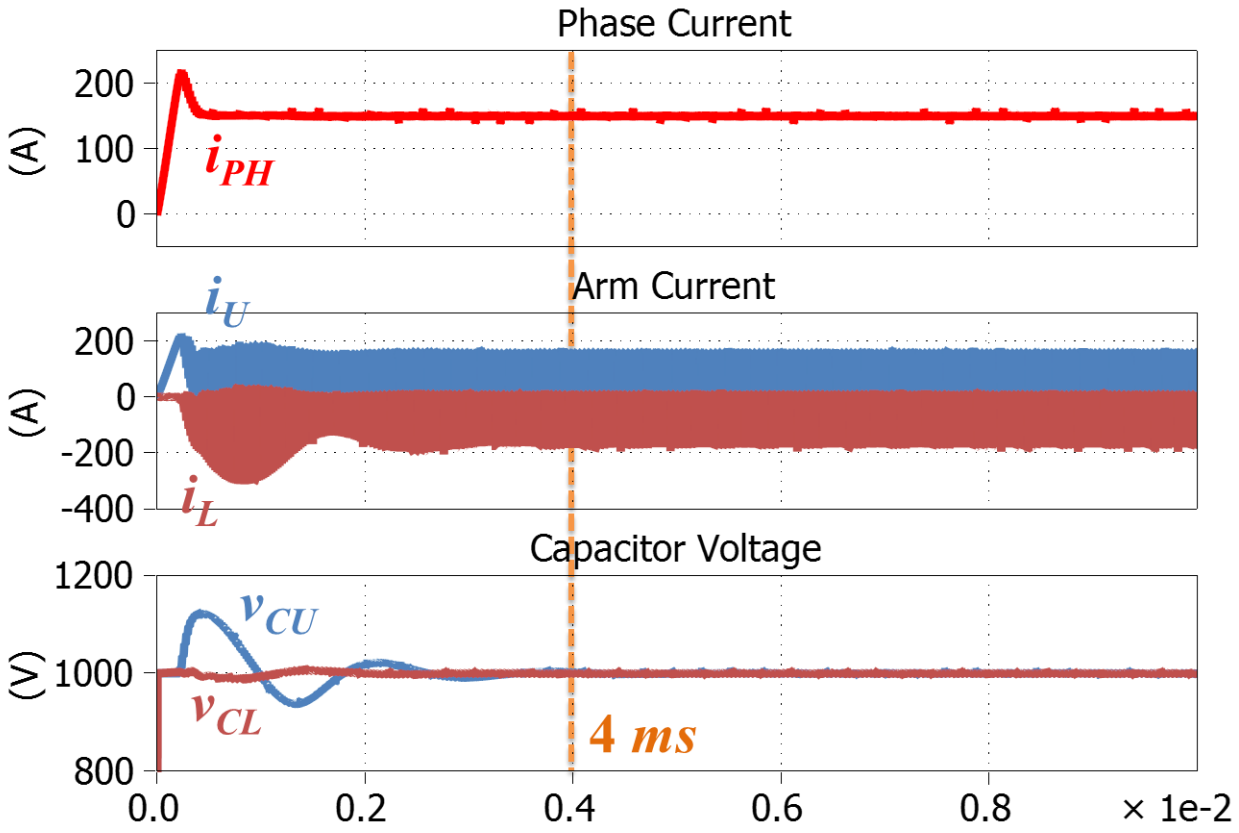


Figure 3-14 Simulation result of the start-up dynamics of HCM-SCC in DC-DC mode

The steady-state DC-AC mode simulation result is shown in **Figure 3-15** and **Figure 3-16**. The average value of phase current i_{PH} is following the current reference i_{PH_REF}. The two arm currents i_U and i_L are pulsating at the switching frequency. The capacitor voltage v_{CU} and v_{CL} are still balanced by cycles with observable errors, which demonstrates a trivial portion of the fundamental frequency component.

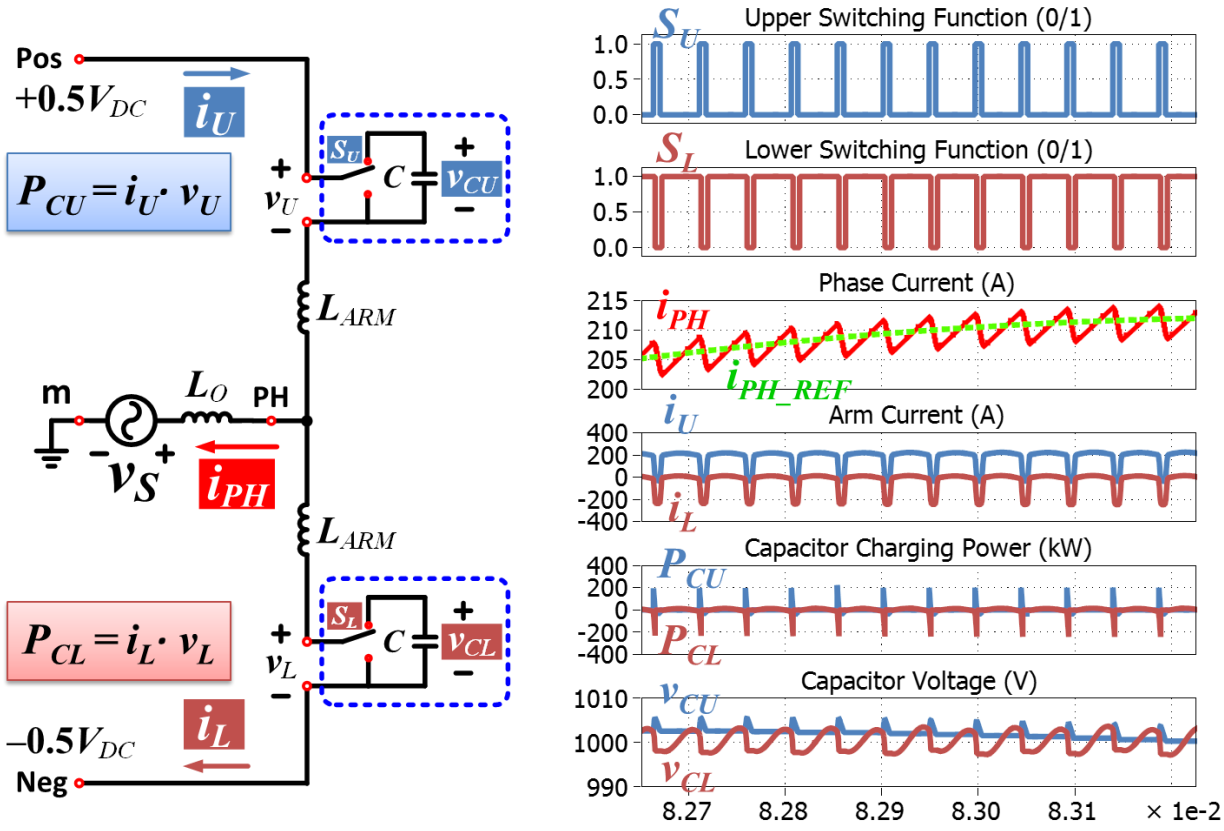


Figure 3-15 Simulation result of the steady-state HCM-SCC in DC-AC mode

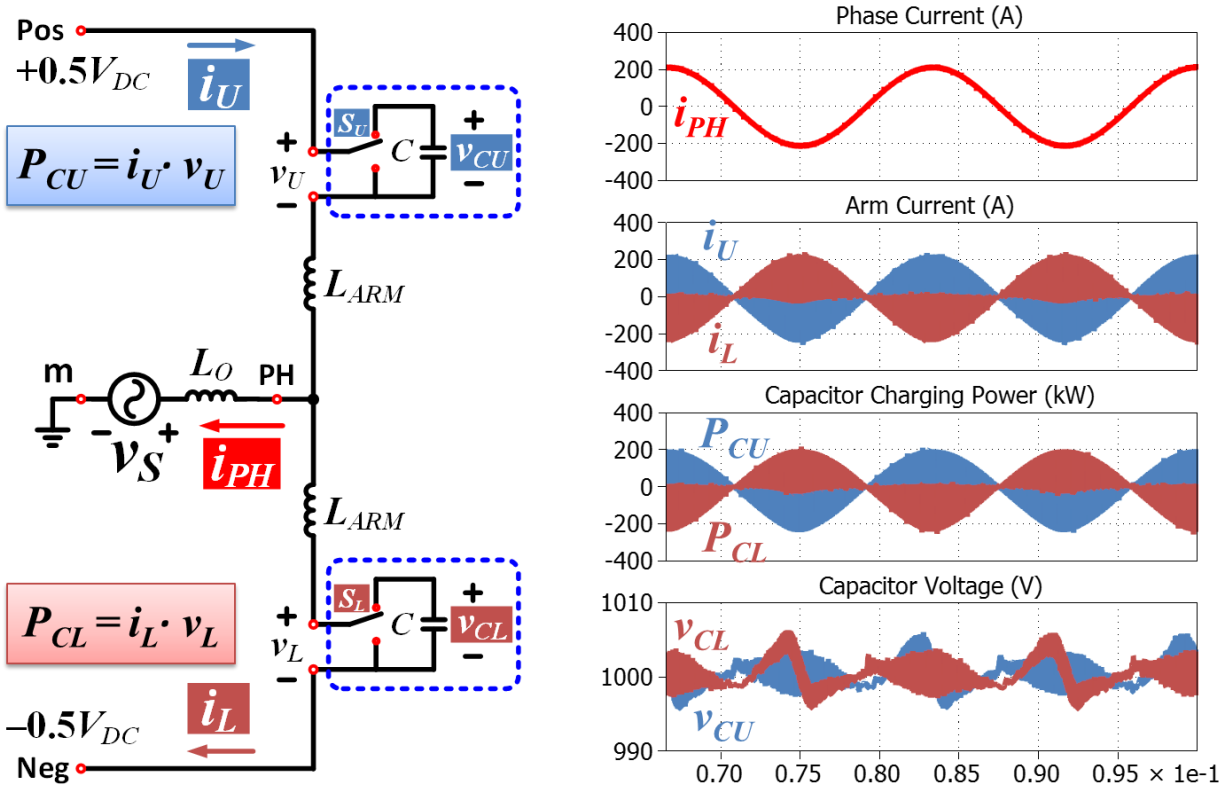


Figure 3-16 Simulation result of the steady-state HCM-SCC in DC-AC mode

The harmonic spectrums of critical variables in the HCM-SCC DC-AC operation mode are given in **Figure 3-17**. The switching frequency of 21 kHz is 350th-order harmonics of the fundamental frequency 60 Hz. In the spectrum of switching functions S_U and S_L, the 0 Hz component equals to 0.5, and 60 Hz and 350th-order harmonic have been observed. Phase current i_{PH} contains primarily 60 Hz component and negligible 350th-order harmonic. The arm current i_U and i_L contain not only low-frequency components (0 Hz, 60 Hz, 120 Hz) but also the side-band of the switching frequency at (350±1)th and (350±3)th. Accordingly, the product of S_U and i_U cancel out the low-frequency part, so the capacitor voltages are dominated by 0 Hz components.

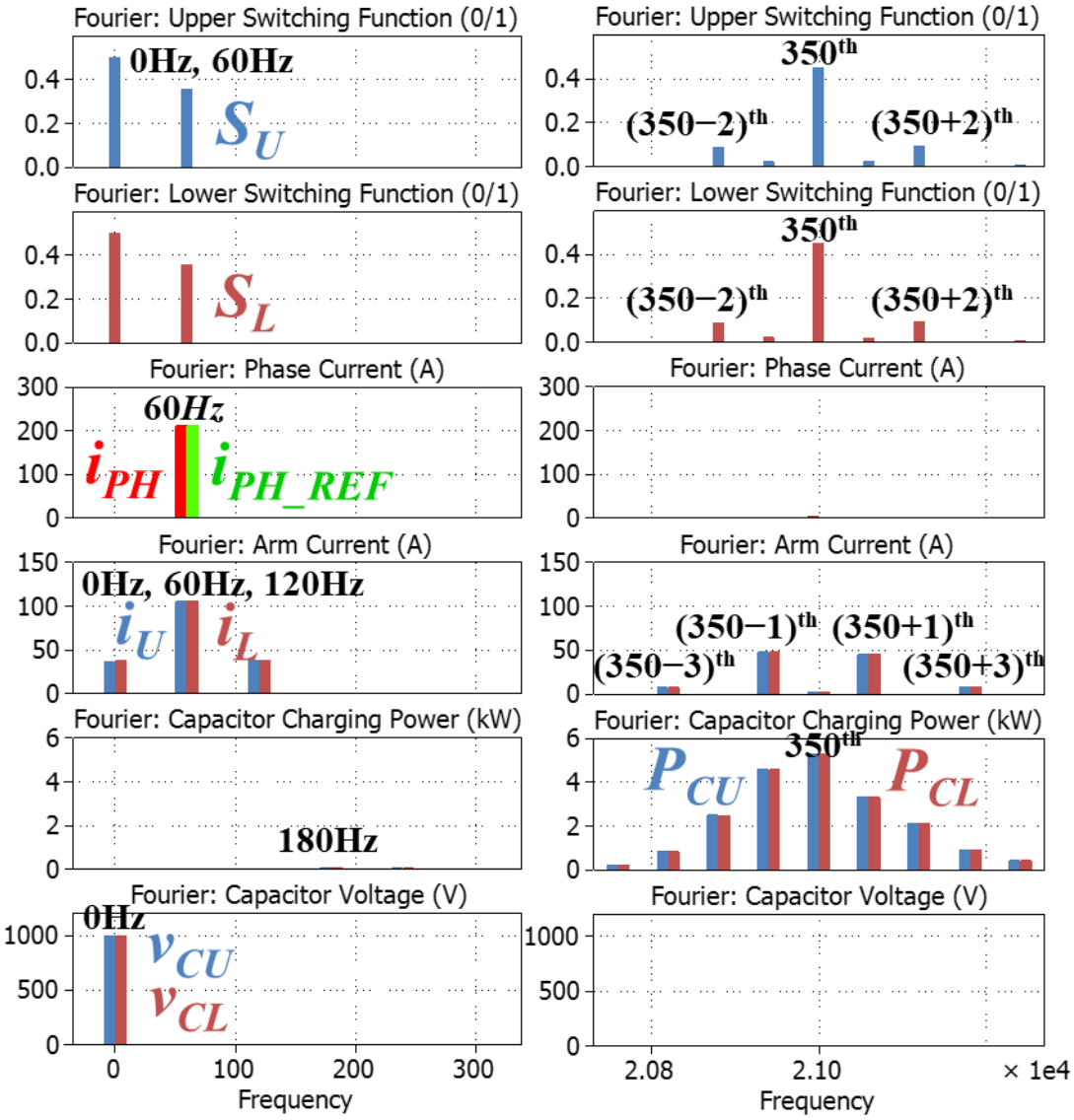


Figure 3-17 Harmonic spectrums of the HCM-SCC simulation in the DC-AC mode

3.5 Power Component Density Comparison

A comparative study regarding passive components and device losses of the half-bridge PEBB-based MMC has been carried out. The selected control method in comparison is the 2^{nd}-order injection, (2^{nd}+60^{th})-order injection and the SCC. **Figure 3-18** shows that SCC has the largest capacitor voltage ripple reduction. **Figure 3-19** illustrates that the arm inductance can be reduced greatly in the (2^{nd}+60^{th})-order injection and SCC modes. Instead, the phase inductance is still necessary for load regulation. **Figure 3-20** tells that the high-frequency injection solution can bring tremendous conduction loss of the devices compared to the 2^{nd}-order injection. The SCC brings more conduction loss as well, but by eliminating the turn-on loss it gives an overall semiconductor loss reduction by 10%.

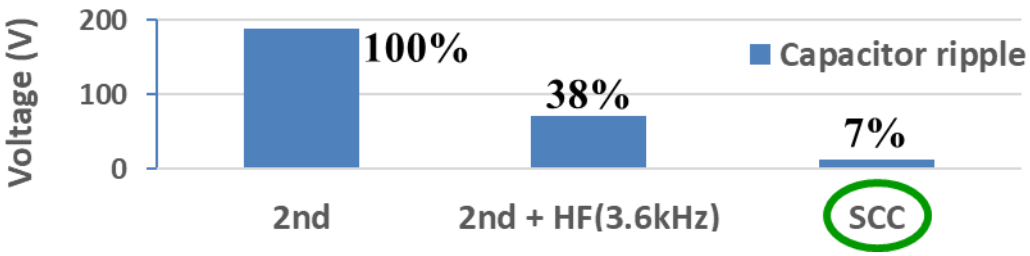


Figure 3-18 Capacitor voltage ripple comparison

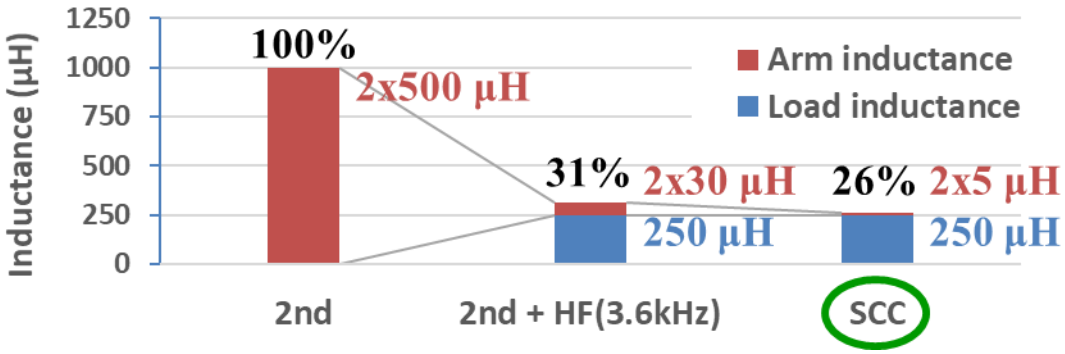


Figure 3-19 Arm and phase (load) inductance comparison

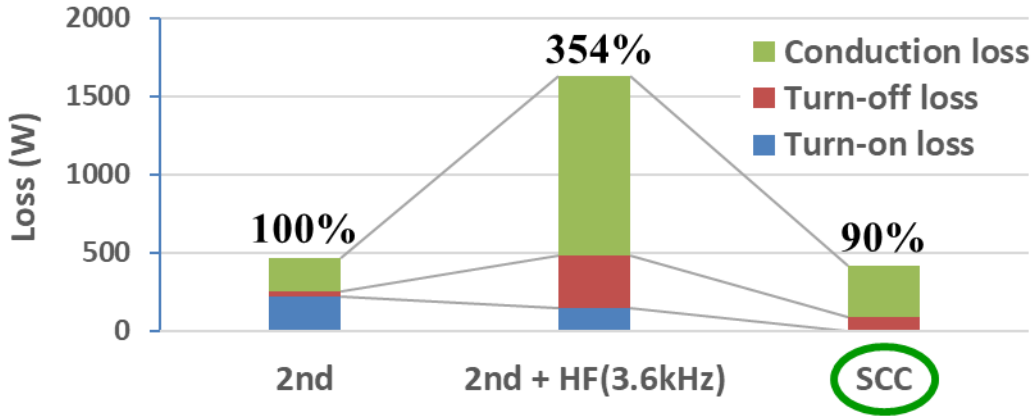


Figure 3-20 SiC MOSFET losses comparison

As specified in Chapter 1, the objective MV modular converter is the 4.16 kV, 150 A (1 MVA), 3-phase MMC built by PEBB1000, a universal power electronics module that will be introduced in the next chapter. In four different operation modes, the required the passive component, device type, and device ampacity are compared in **Figure 3-21**.

In Column 1, Si IGBTs are applied and switch at 2 kHz, while in Column 2 SiC MOSFETs are applied and switch at 20 kHz. Both cases operate with 120 Hz harmonic injection. By using SiC MOSFET at the high switching frequency, the arm inductance is reduced from 5 mH to 500 μH. Assuming that the volume of total inductors and capacitors are similar, the power component density can be improved to 1.8 p.u.

In Column 3, SiC MOSFETs are used and the 3.6 kHz injection is applied to reduce the capacitor volume. The capacitor bank outside the PEBB1000s and the arm inductors are eliminated, but the current ampacity of the device is reduced to 28.2% because of the huge conduction loss. As a result, the total power component density is only increased to 1.4 p.u.

In Column 4, SiC MOSFETs are used and the SCC is applied to reduce the capacitor volume. An assumption has been made in this case the SCC can scale up to 10 PEBBs per arm without de-rating. In this way, the capacitor bank, the arm inductors are removed, and meanwhile, the ampacity is increased by 11% as the total device loss is reduced to 90%. Consequently, the power component density is augmented to 23.1 p.u.

MMC	120 Hz injection with Si IGBT (f_{sw} = 2 kHz)	120 Hz injection with SiC MOSFET (f_{sw} = 20 kHz)	3.6 kHz injection with SiC MOSFET (f_{sw} = 20 kHz)	SwF injection (SCC) with SiC MOSFET (f_{sw} = 20 kHz)
PEBB	PEBB X 60	PEBB X 60	PEBB X 60	PEBB X 60
Low-freq. caps	1600 V, 450 µF  X 60	1600 V, 450 µF  X 60	-	-
Addit. arm inductor	300A 5 mH  X 6	300A 500 µH  X 6	-	-
Phase inductor	-	-	300A 250 µH  X 3	300A 250 µH  X 3
Power compo-nent density	Capacitor: 100 % Inductor: 100 % Ampacity: 100 % Density: 1.0 p.u.	Capacitor: 100 % Inductor: 10 % Ampacity: 100 % Density: 1.8 p.u.	Capacitor: 38 % Inductor: 3.1 % Ampacity: 28.2 % Density: 1.4 p.u.	Capacitor: 7 % Inductor: 2.6 % Ampacity: 111 % Density: 23.1 p.u.

Figure 3-21 MMC power component density comparison

Chapter.4 PCB-Imbedded Rogowski Switch Current Sensor

4.1 Introduction

The proposed HCM-SCC requires accurate analog information of one arm current to turn off the corresponding switches. However, in high power applications, this is unrealistic because no commercial high-density current sensor is available to achieve both hundreds-of-ampere magnitude and megahertz bandwidth. Alternative means to realize the HCM-SCC is to use the switch current instead of the inductor current. According to that, this chapter introduces a high-density integrated switch-current sensor based on Rogowski coils, named Rogowski switch-current sensor (RSCS). Eventually, it serves not only the control sensor but also a short-circuit detector for fast and reliable SiC MOSFET protections.

4.2 Motivation, Specifications, and Fundamentals

4.2.1 Motivation

Short-circuit protection is one of the most critical functionalities that prevents semiconductor switches from breakdown or explosion upon phase-leg shoot-through. It is even more critical in MV high-power application as the components are expensive and high-energy explosion is catastrophic. The conventional solution for Si IGBT protection is

the DeSaturation (DeSat) that takes advantage of the device output characteristics [D.1] - [D.7] . The blue curve in

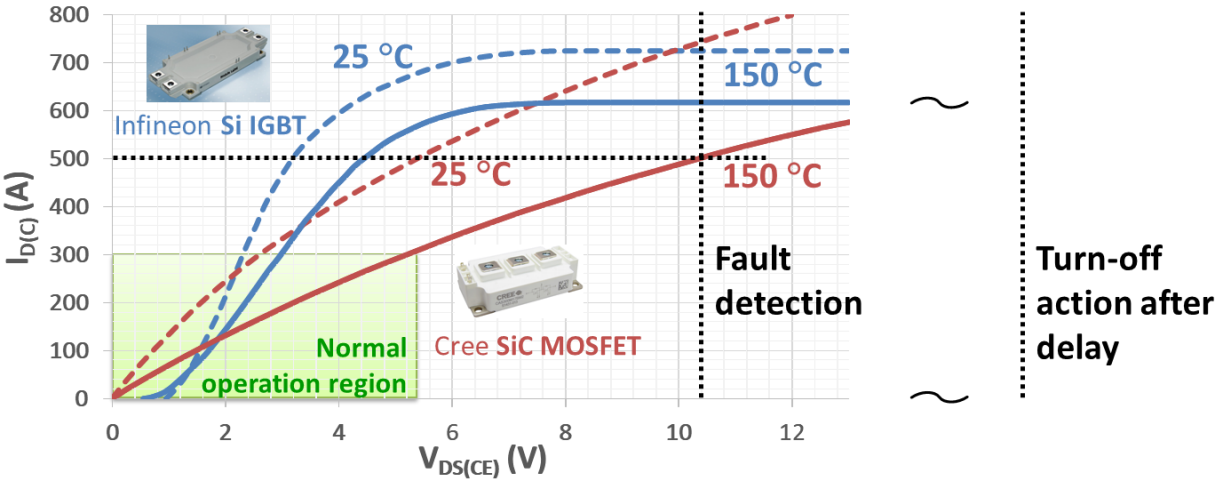


Figure 4-1 is the output characteristics of a commercial Si IGBT FF225R17ME4 rated at 1700 V and 225 A (@100°C) [D.8] . In the normal operation (saturation) region, the device collector-emitter voltage V_{CE} varies in a small range while the collector current IC changes in a wide range. As soon as short-circuit happens, the device operation state deviates from the saturation region and moves across a "hard" knee point. It then enters the linear region where IC hardly increases, and V_{CE} rises dramatically. This feature makes sensing V_{CE} a very simple and reliable technique for Si IGBT short-circuit detection. It also works well with varying junction temperature as the Si IGBT output characteristics are not strongly temperature-dependent, as shown in the comparison between the 25°C and 150°C blue curves.

The DeSat protection usually responses within several microseconds, primarily because it requires the DeSat circuitry to kick in until the V_{CE} drops low enough when the device is fully turned on. The time span between the gate signal turning on and V_{CE} dropping to almost zero is called the "blanking time" [D.9] [D.10] . The blanking time is produced by an RC low-pass filter. It works jointly with reaction circuit to cause a total delay between the time when I_C reaches a threshold value and the time when I_C starts to drop. The delay sets a minimum response time of the DeSat protection. This is labeled as t_d in

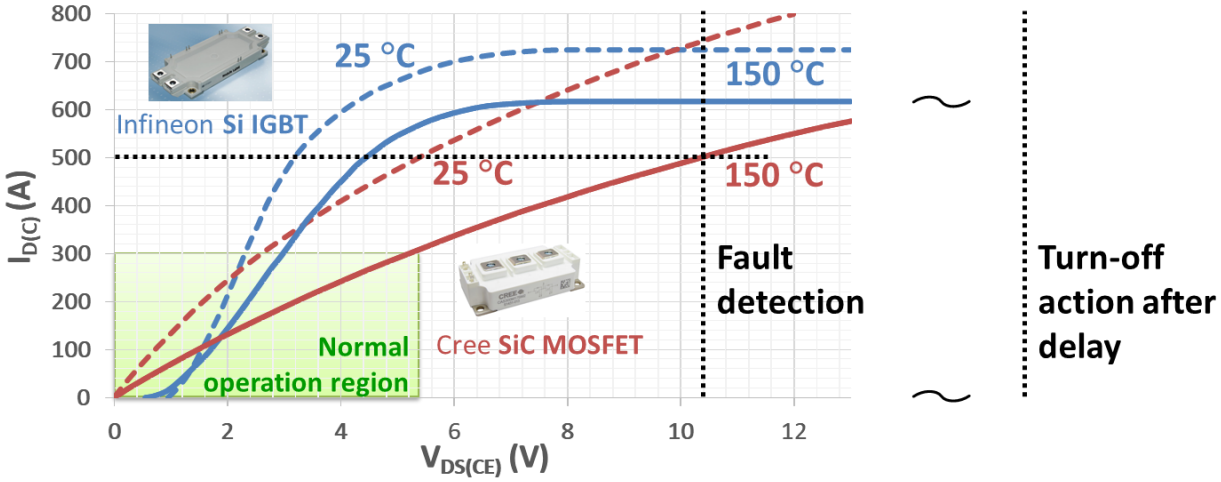


Figure 4-1, where the time-domain IGBT short-circuit curve is blue. Fortunately, most of the commercial Si IGBTs are designed to withstand the short-circuit current for 10~15 μs, which is long enough for the device to safely shut down.

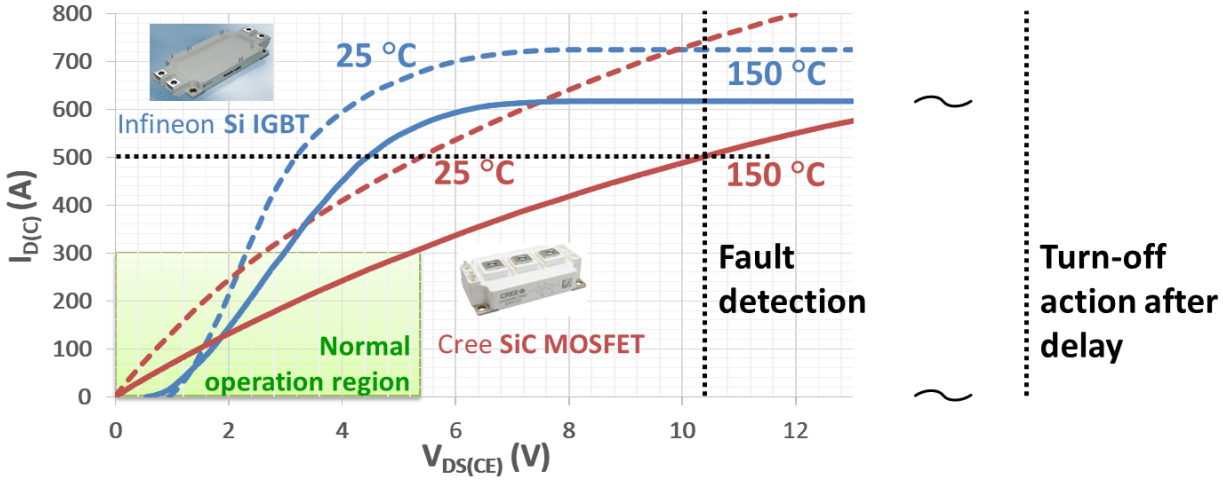


Figure 4-1 Output characteristics comparison: Si IGBT vs. SiC MOSFET

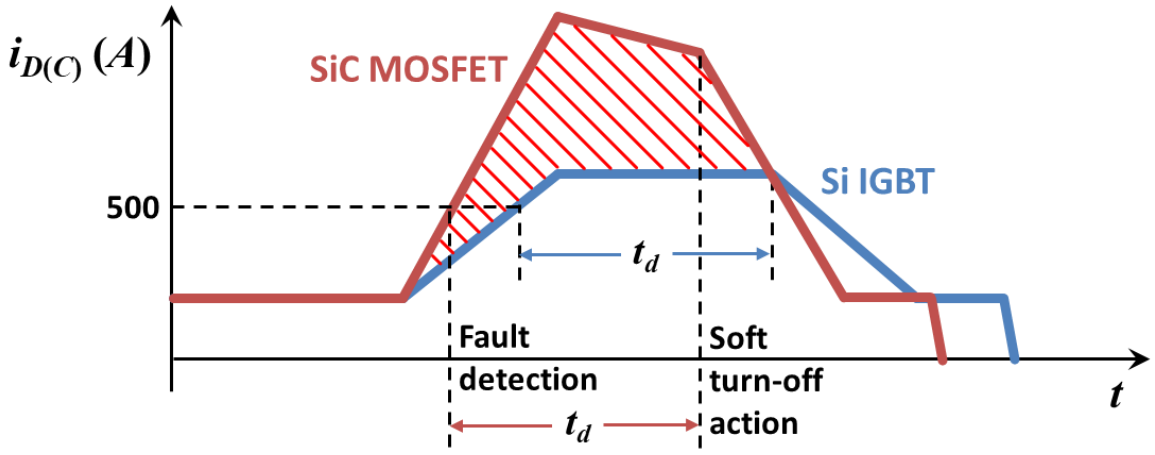


Figure 4-2 Short-circuit current comparison: Si IGBT vs. SiC MOSFET

The output characteristics of the SiC MOSFET are much "softer" in the wider current region [D.11] . **Figure 4-2** shows that the drain current I_D keeps rising even when the drain-source voltage V_{DS} is at high values. For this reason, the peak short-circuit current, as well as the accumulated short-circuit energy on the SiC MOSFET, are extensively higher than the Si IGBTs. Accordingly, most of commercial SiC MOSFETs cannot survive under a long response delay time. On the other hands, output characteristics of SiC MOSFETs have almost 50% difference between 25°C and 150°C as shown in

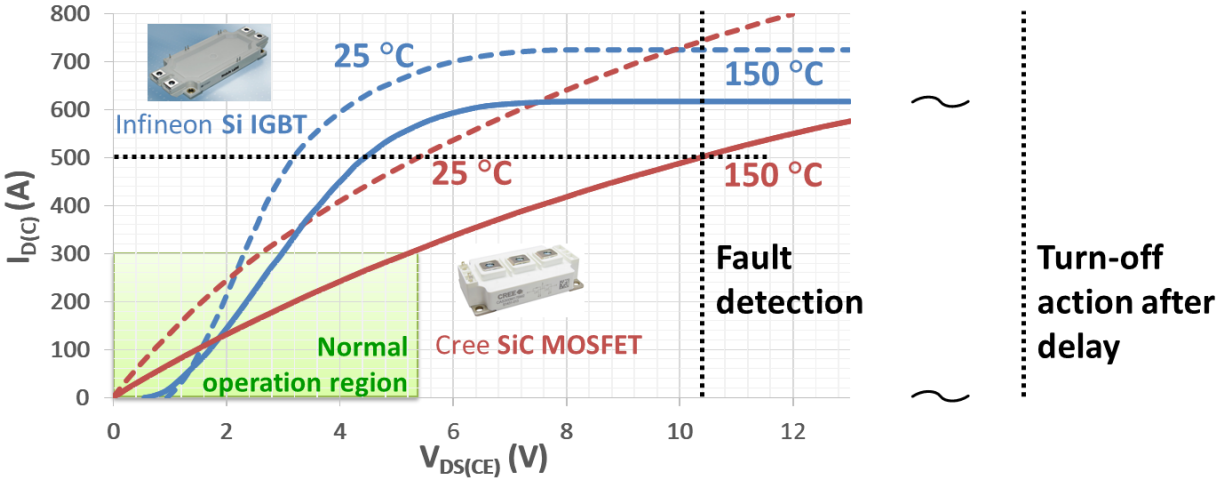


Figure 4-1. This behavior indicates that short-circuit current threshold varies distinctively if using V_{DS}-based current sensing method. Consequently, if the DeSat still serves as a short-circuit protection approach, very precise is required for tuning blanking time and the threshold value under different operation conditions.

Alternative switch-current sensing methods have been investigated for short-circuit protection. It is required to have high sensing magnitude, high bandwidth, low response

delay, high noise immunity, and fair accuracy. A Rogowski switch-current sensor (RSCS) is featured in all those characteristics. It was used as a switch-current detection method for motor drive phase-current sensing as early as 1990s when the main power devices were Si IGBTs [D.12] . It has also been used for current sharing of paralleled IGBTs and demonstrated quite good performance [D.13] . However, the switch-current sensor was not widely implemented for Si IGBT short-circuit protection as the DeSat is simpler and more cost-effective. In this research work, Rogowski switching-current sensor (RSCS) is designed for both short-circuit protection and current control.

4.2.2 Specifications

The different current sensor specifications for the two purposes regarding the selected SiC MOSFET module are shown in **Figure 4-3**, where the parameter comparison with 6 dimensions of range, response delay, bandwidth (BW), accuracy, *di/dt*, and sensor density, are given. Short-circuit protection requires the highest sensing range. The high BW, *di*/*dt*, and short response delay are also necessary to achieve fast protection. However, protection sensor can tolerate 10% error in practical applications. The sensor for current control requires higher accuracy than the protection but allows for lower performance on other dimensions. The current probe for testing and validation, as a contrast, requires the highest performances in almost all the respects but high sensor density, because it never comes with a converter product. A commercial Rogowski probe usually has a value of 20 A/inch^3, which is too low to be integrated within any power converters. It is required to

design the sensor for a high-density integration of 1000 A/inch^3 so that high converter power density can be achieved.

Merging the requirement for both the short-circuit protection and converter current control, the specifications of the RSCS are defined in **Figure 4-4**. Compared to the commercial current probe, the RSCS is able to be integrated into a gate driver board by sacrificing a small portion of the performance in response delay, BW, accuracy, and *di*/*dt*.

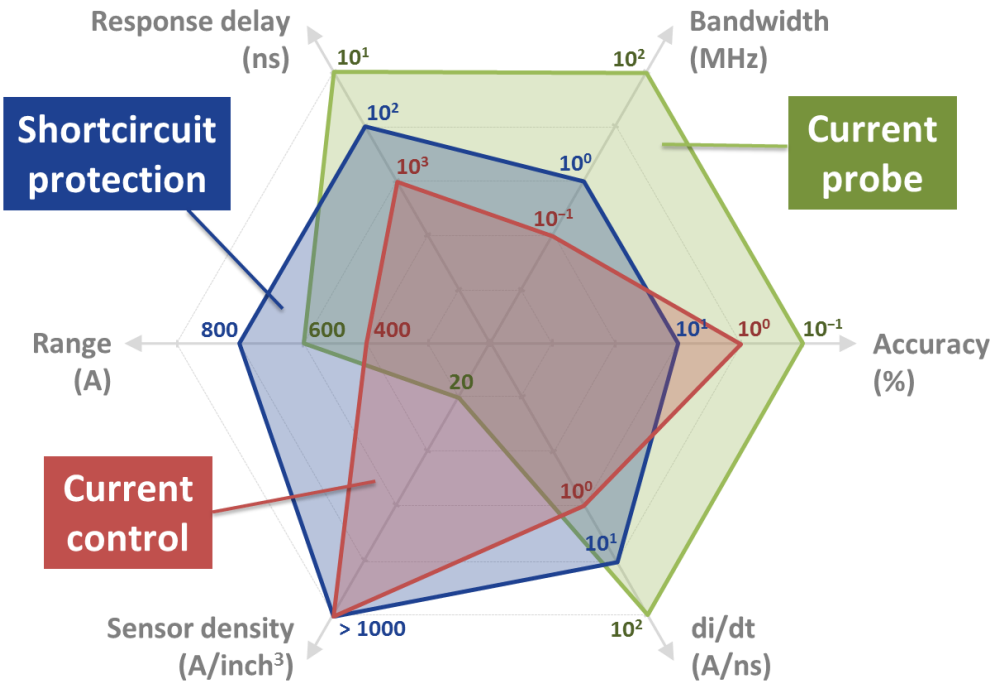


Figure 4-3 Current sensing requirements for different applications

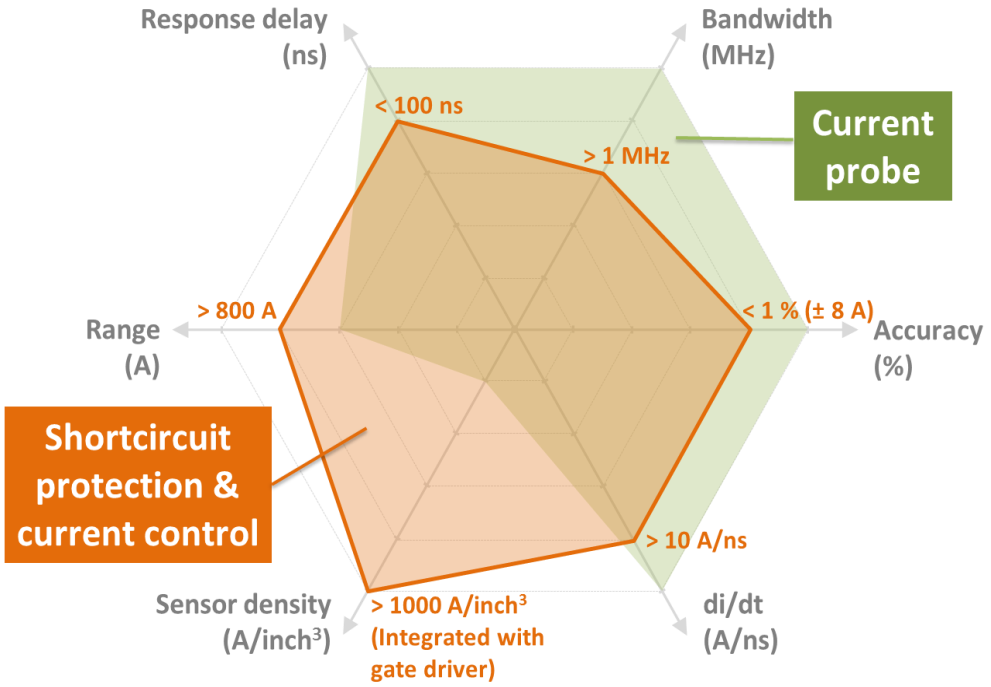


Figure 4-4 Specifications of the Rogowski switch-current sensor

4.2.3 Fundamentals

The switch current sensor essentially comprises a Rogowski coil and an integrator. **Figure 4-5** shows that the Rogowski coil serves as a differentiator that generates the *di*/*dt* value of the sensed current, scaled by a factor of the mutual inductance *M* between the sensed conductor and the Rogowski coil. The integrator then converts the *di*/*dt* information back to the sensed current. Passive and active integrators are alternatives, and they both have problems with insufficient low-frequency gain. The passive integrator is basically an RC filter. In the Bode plot of the passive integrator shown in **Figure 4-6**, the total transfer gain is a band-pass filter in orange. The lower limit f_{BW_L} is the cut-off frequency of the passive integrator, and higher limit f_{BW_L} is the self-resonant frequency caused by the Rogowski-coils self-inductance and its equivalent parasitic capacitance (EPC). On the other hand, the total transfer gain of the active filter in green is also equivalent to a band-pass filter, as shown in the Bode plot **Figure 4-7**. However, the lower limit f_{BW_L} is due to the non-ideal cut-off frequency of the operational amplifier when configured as an active integrator. Naturally, the active integrator is a better option because the low-frequency gain is critical for a current control sensor of higher bandwidth. Nevertheless, the sensor still cannot sense any DC signal at steady state. As shown in **Figure 4-5**, the output of active integrator V_{INT_OUT} (green) drifts away along with the time. To resolve this issue, a switch-cycle-based reset switching is placed across the integration capacitor. It resets the sensor output to zero when the SiC MOSFET is not conducting current. As the initial value of the integrator output is set zero at every switching period, the reset circuit guarantees that the

sensor output always follows the sensed switch current, and the sensor output in time-domain becomes the blue waveform in **Figure 4-5**. The frequency-domain transfer gain is depicted by the blue curve in **Figure 4-7**. The ideal transfer gain from the sensed current to the sensor output voltage is given in (4-1),

$$\textbf{(4-1)} \qquad v_{INT\_OUT}(f) = G_{RSCS} \cdot i_D(f) = \frac{M}{R_i C_f} i_D(f)$$

where the M is the mutual inductance, R_i is the integration resistance and C_f is the integration capacitance.

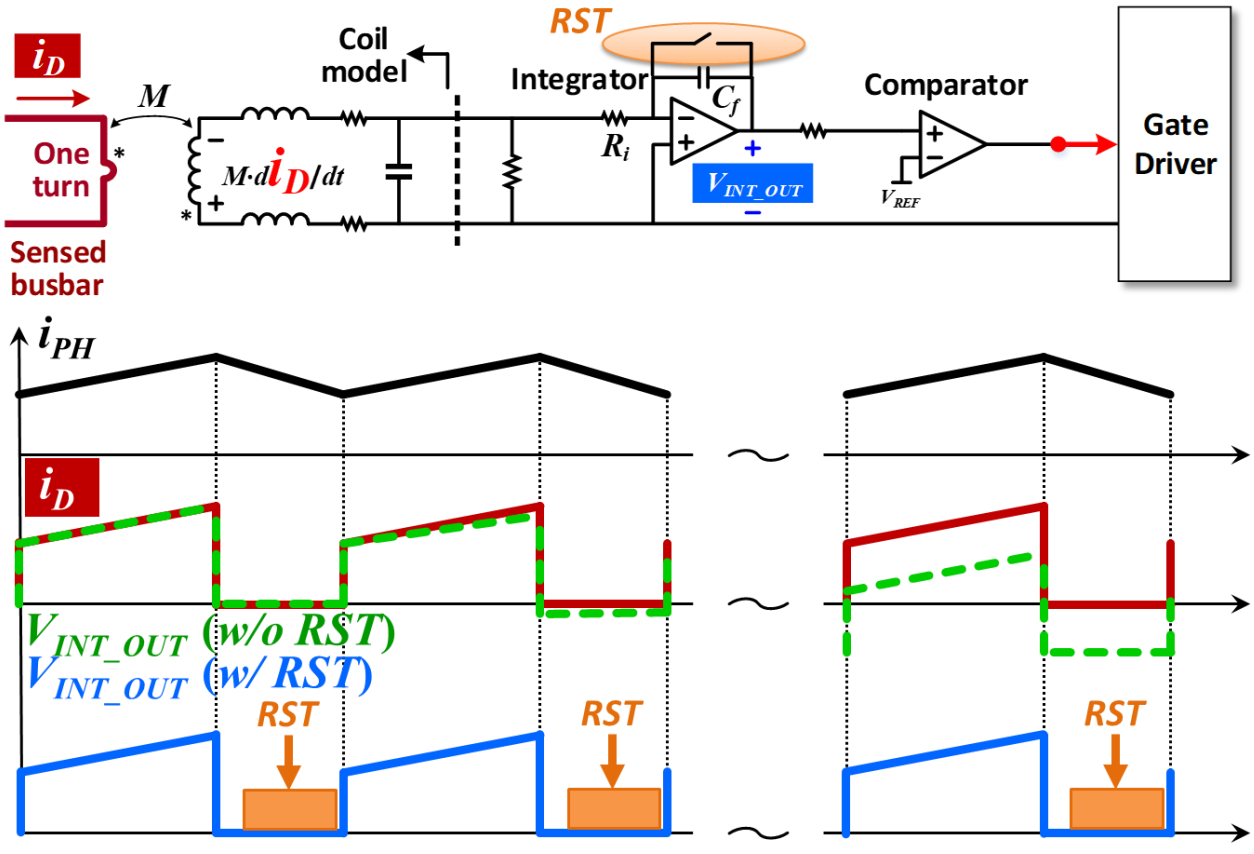


Figure 4-5 Current sensing requirements for different applications

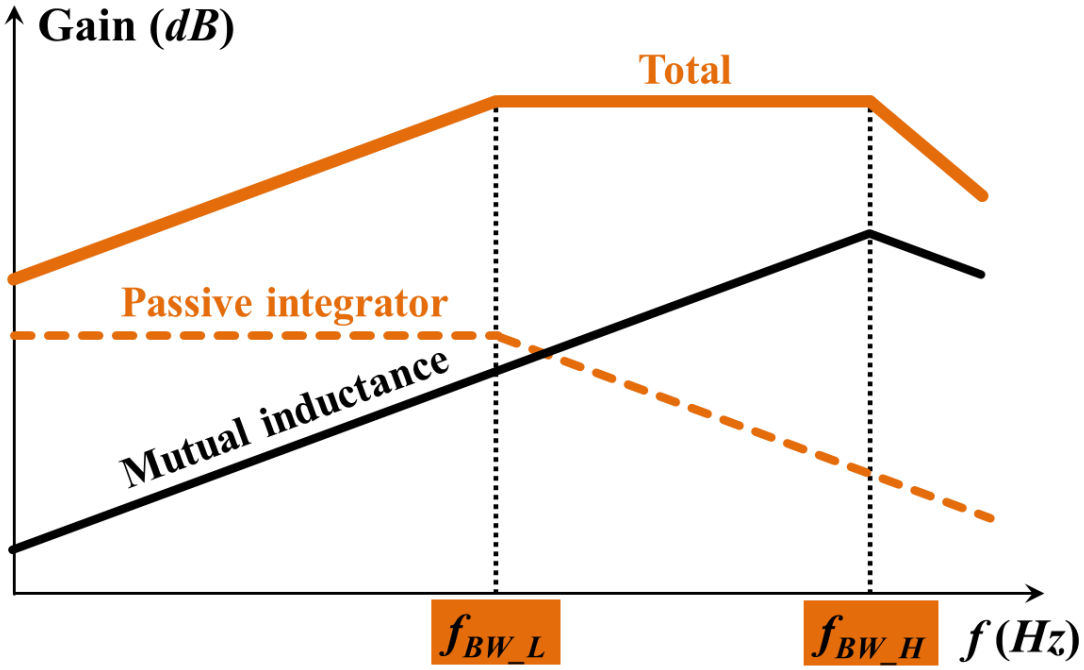


Figure 4-6 Passive integrator gains

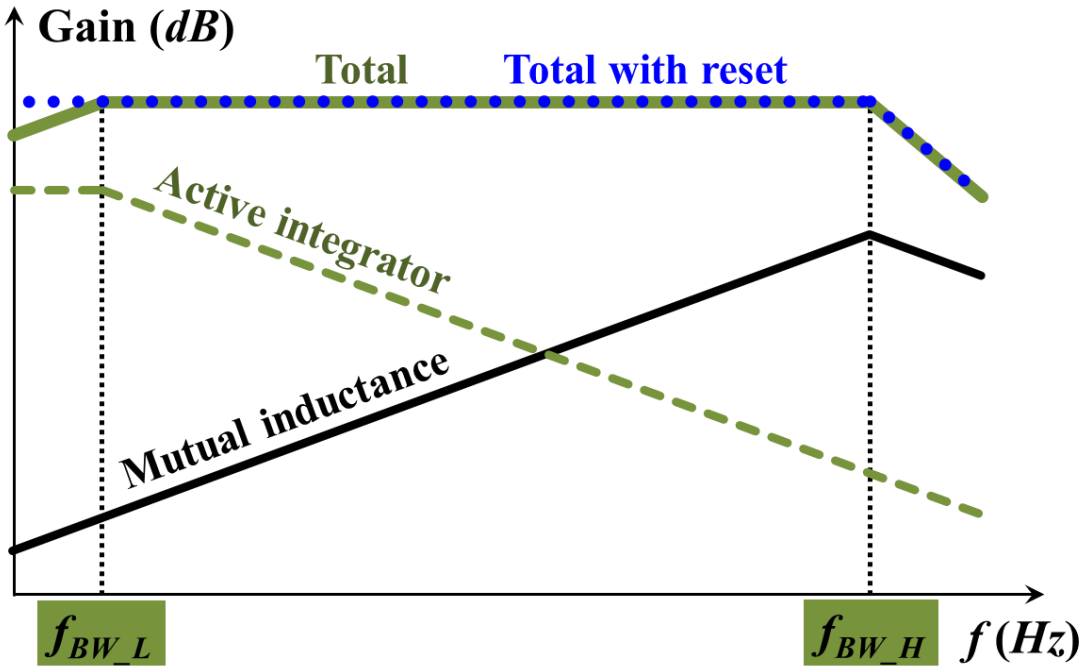


Figure 4-7 Active integrator gains

4.3 Rogowski Switch-Current Sensor Design

4.3.1 PCB-Embedded Rogowski Coil Design

The Rogowski coil requires auxiliary windings to compensate its one-turn effect, otherwise, it is very sensitive to the flux going along the coil center (shown as the blue line in **Figure 4-8**). The most widely-used structure is the single return trace crossing along the center of the winding center (different from the coil center), shown as the dashed red trace in **Figure 4-8**. In an ideal design, the sensed conductor should be going along the center line of the coil, so that the flux it generates will be uniformly coupled by all the windings. It is very difficult to be ensured because of the primary-side conductor shape and assembly tolerance. To overcome this issue, uniform winding distance and high turn number are required. On the other hand, in order to increase the sensitivity of the sensor as well as the signal-to-noise ratio, the mutual inductance M should also be as high as possible. Accordingly, 152 turns of windings have been designed by an effort to maximize the turn number on PCB without high-cost manufacturing process. The winding height is limited by the PCB thickness and is designed as 2 mm. The winding width is limited by the terminal positions of the device packaging and insulation clearance and is designed to be 1 mm. The final PCB layout of the RSCS winding is shown in **Figure 4-9**.

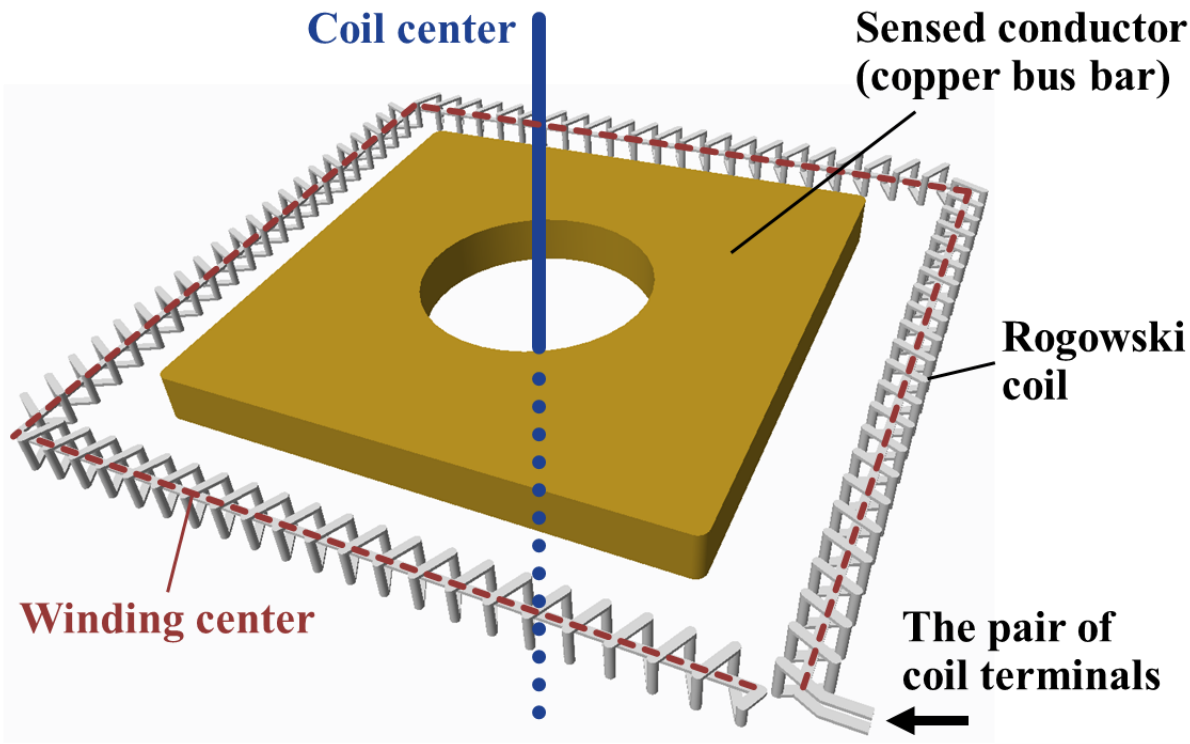


Figure 4-8 Rogowski coil conceptual structure

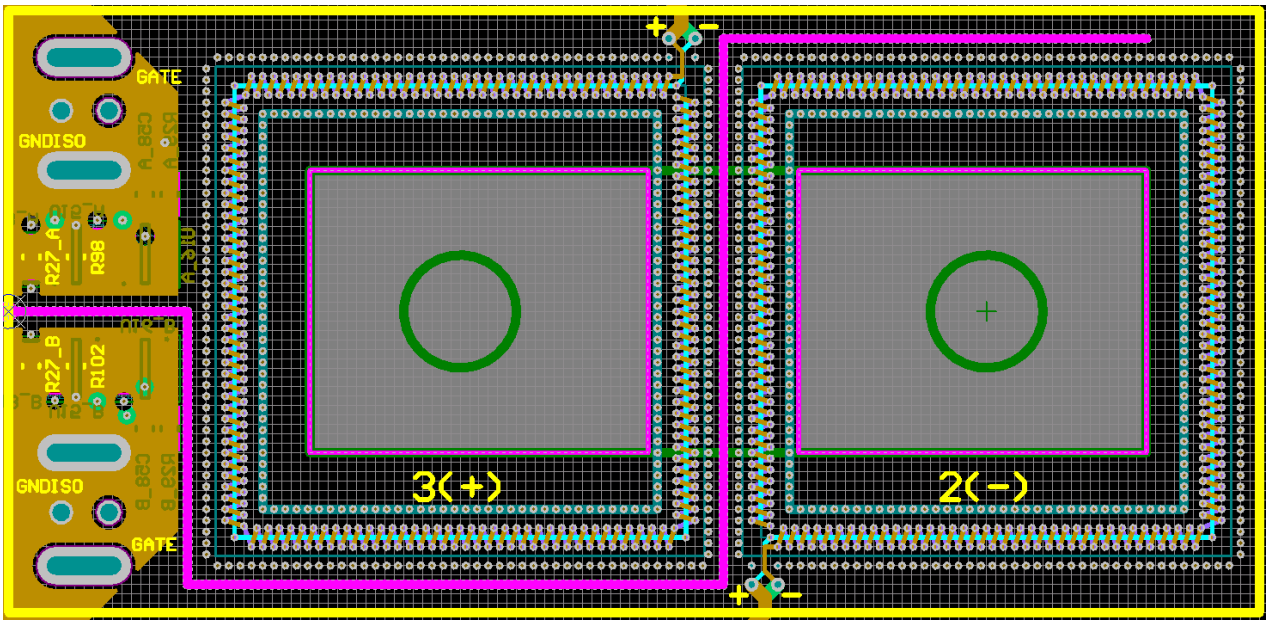


Figure 4-9 RSCS wingding layout

4.3.2 PCB-Embedded Shielding Design

As shown in **Figure 4-10**, the sensed conductor of the high-side SiC MOSFET is sitting on a jumping voltage potential, referred to the ground of the high-side RSCS signal processing circuits. The signal processing circuits include a high-BW integrator, a fast comparator for protection, an ADC for current sampling and a DAC and comparator for peak-current-mode (PCM) control. All of them are very sensitive to noises. Therefore, a high dv/dt rate caused by the switching of the SiC MOSFET can easily induce a CM current that is injected to the sensing circuitry in the yellow shade via the parasitic coupling capacitance C_{CP}. The C_{CP} is estimated to be 2 pF in Q3D simulations. If the dv/dt rate of v_{DS} rises as high as 30 V/ns, 60 mA CM noise current can be induced at megahertz. The noise spikes on the Rogowski winding self-inductance and other PCB traces are significant at this high-frequency range.

To overcome this problem, PCB-based shielding layers have been proposed. The green line inserted between the primary and secondary sides of the Rogowski coil in **Figure 4-11** illustrates the effect of the shielding layers. The direct coupling capacitance between the sensed bus-bar and the Rogowski coil is greatly attenuated, and C_{CP} is divided into two parts C_{CP1} and C_{CP2}. As the shielding layers are connected to the source of the SiC MOSFET, C_{CP1} is still subjected to the dv/dt, and the CM noise currents will flow through the shielding layers back to the MOSFET source. C_{CP2} is not subjected to the dv/dt, and thus no CM noise currents will be injected to the RSCS signal processing circuitry. However, the shielding layers introduce penalties as well. C_{CP2} will be equivalently added

to the EPC of the windings C_S, which decreases high-frequency BW f_{BW_H}. Negative effects have been modeled and measured by impedance analyzer and will be shown in later sections.

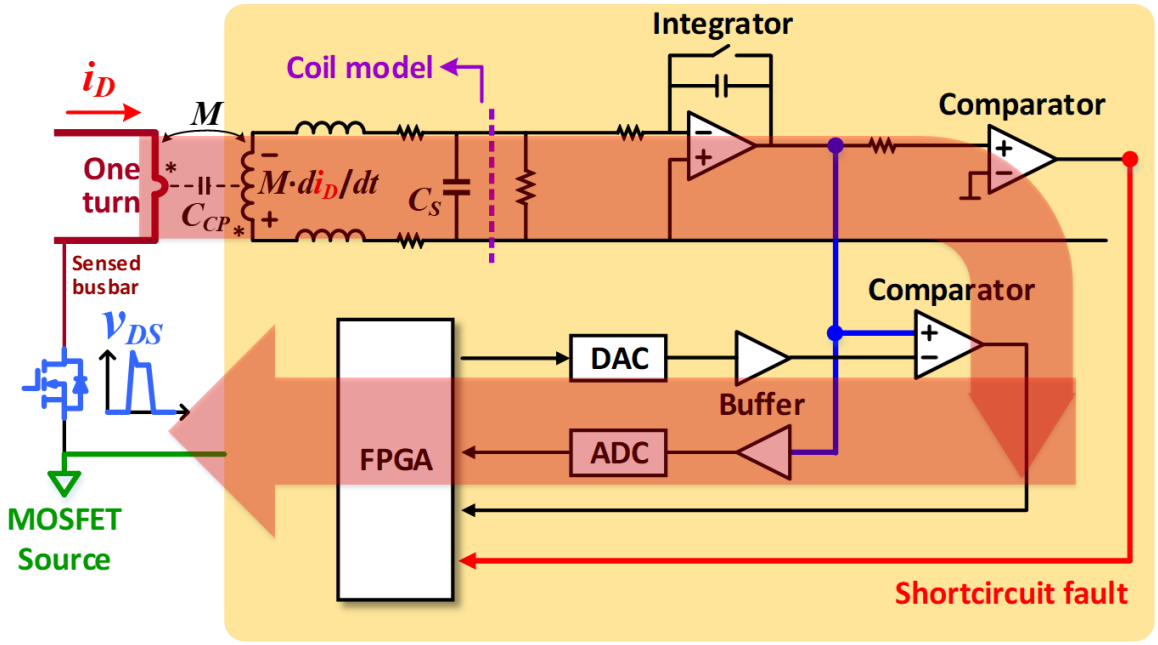


Figure 4-10 CM noise issue of the high-side RSCS caused by *dv/dt*

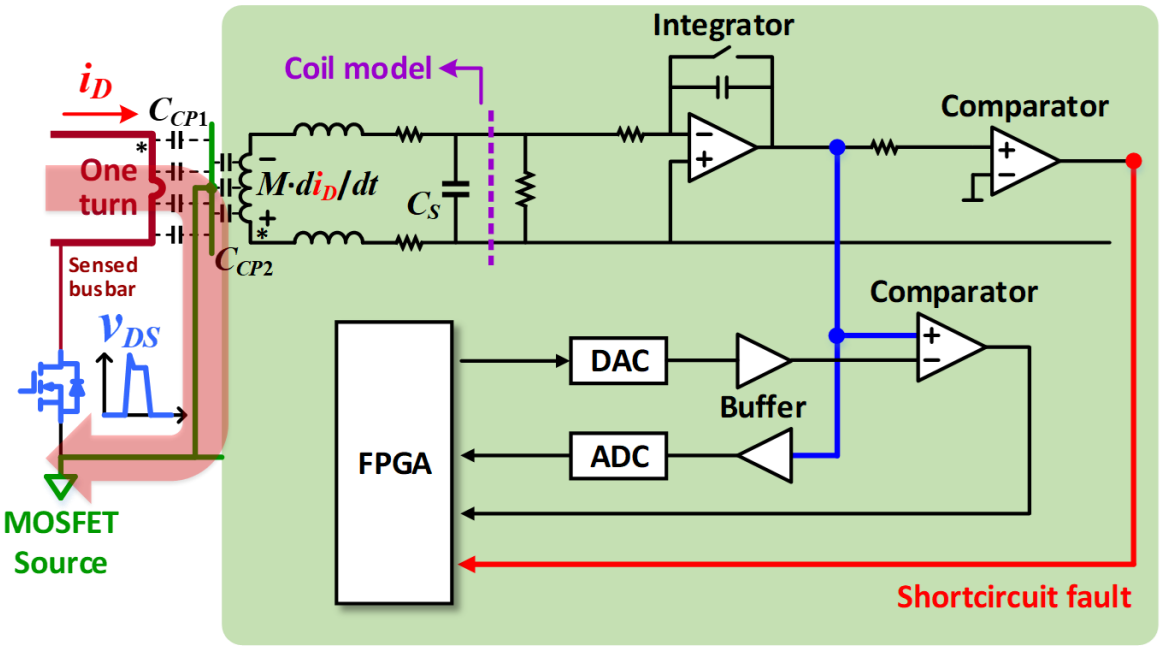


Figure 4-11 Shielding layers to bypass the CM noise current

Figure 4-12 shows that the RCSC windings and shielding layers are designed on a 6-layer PCB. The internal 4 layers are used to construct the windings by traces and vias, and the shielding is placed on the top and bottom layers. As the shielding is only designed to screen the electric field instead of the magnetic field that dominates the mutual inductance *M*, the top and bottom shielding traces are connected only at a single common junction. The final PCB layout of the RSCS winding and shielding design is shown in **Figure 4-13**.

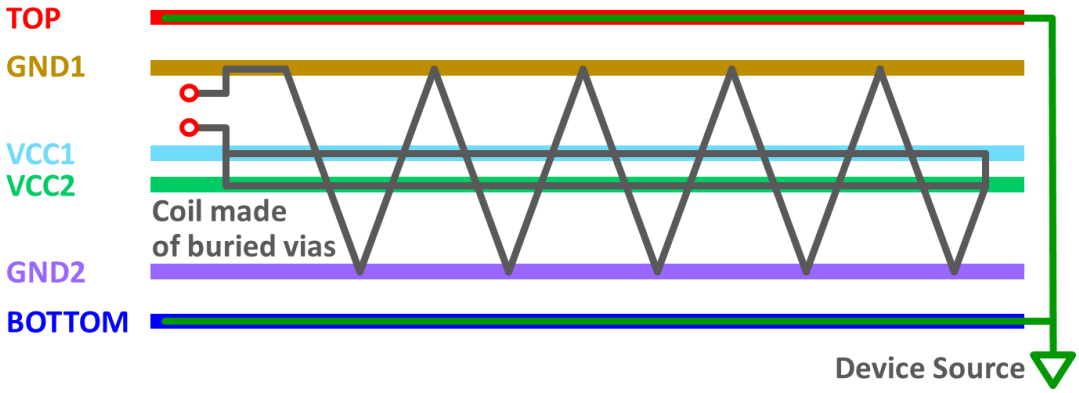


Figure 4-12 RSCS layer design on a 6-layer PCB

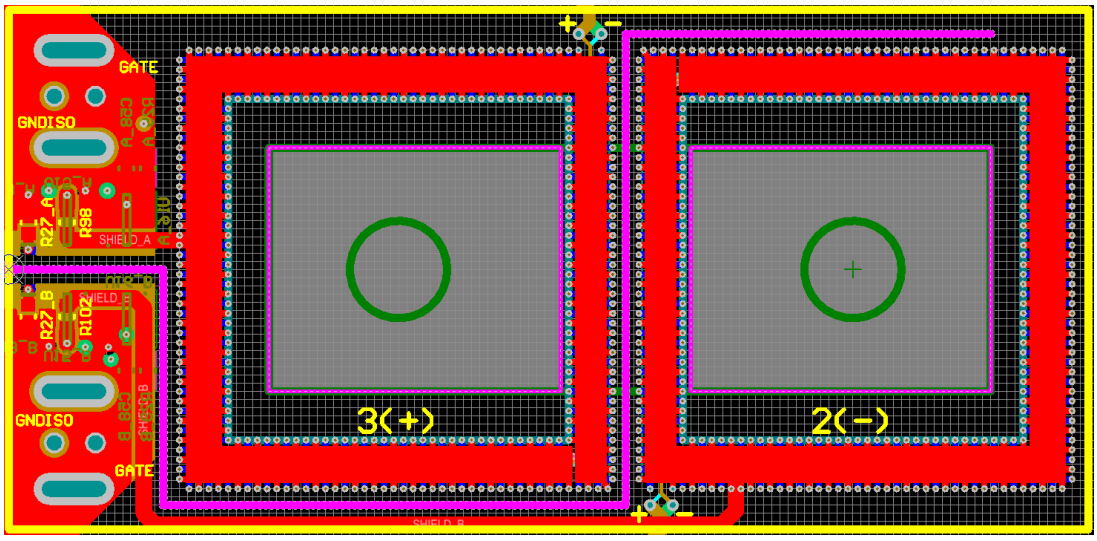


Figure 4-13 RSCS wingding layout adding shielding layers

4.3.3 Integrator Design

Despite that the active integrator has shown superior performance than the passive integrator, the non-ideal behavior of the former one still prevents the RSCS from fully reflecting the device current. The left figure in **Figure 4-14** shows the non-ideal model of an operational amplifier (OpAmp) based active integrator. First of all, there always exists a large feedback resistor R_f in parallel with the integration capacitor C_f. R_f is a critical value that partially determines the closed-loop DC gain of the integrator, which is usually integrated inside the OpAmp IC package with a value of a few mega-Ohms. **Figure 4-15** shows both the ideal and the practical RSCS output voltage, where the switching-cycle reset is enabled at 500 ns after the MOSFET is turned off. The reset is released before the MOSFET is turned on again. Since C_f is paralleled with R_f, the voltage across C_f will be slowly discharged and the V_{INT_OUT} becomes the blue waveform. If C_f is a few micro-Farads, then the discharge time constant is at the milliseconds range. Accordingly, if the switching frequency is as low as 1 kHz, then the steady-state drift will be significant and the RSCS sensor accuracy will drop. Regarding the SiC MOSFET applications, the switching frequency is mostly designed higher than 20 kHz to mitigate acoustic noises, which is very suitable for the RSCS fundamentals and limitations.

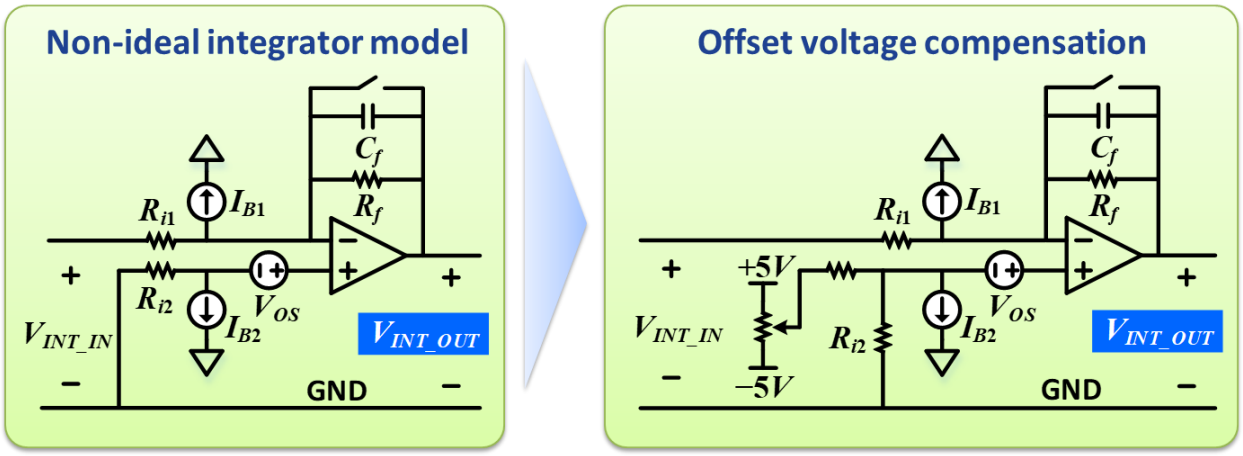


Figure 4-14 Non-ideal integrator model and offset compensation

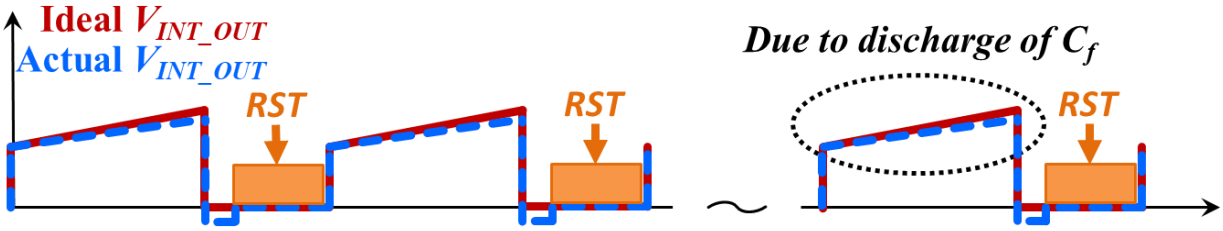


Figure 4-15 Non-ideal integrator model and offset compensation

4.3.4 Prototype

The fabricated RSCS integrated with the gate driver board is mounted on top of the SiC MOSFET module as shown in **Figure 4-16**. The connection screw of the module for positive and negative DC buses are aligned with the two center points of two coils, respectively. The actual currents are carried by the terminal bus bars coming out of the module. On the surface of the PCB, the top-layer shielding layout can be observed.

From the other view of the gate driver in **Figure 4-17**, most of the critical components including power supplies, a driver IC, an FPGA, and signal processing circuits of the RSCS is presented. The signal processor only takes a small piece of the area of the driver board where all the functionalities described in **Figure 4-11** have been integrated. It provides the gate driver with high-level intelligence for advanced sensing and control techniques.

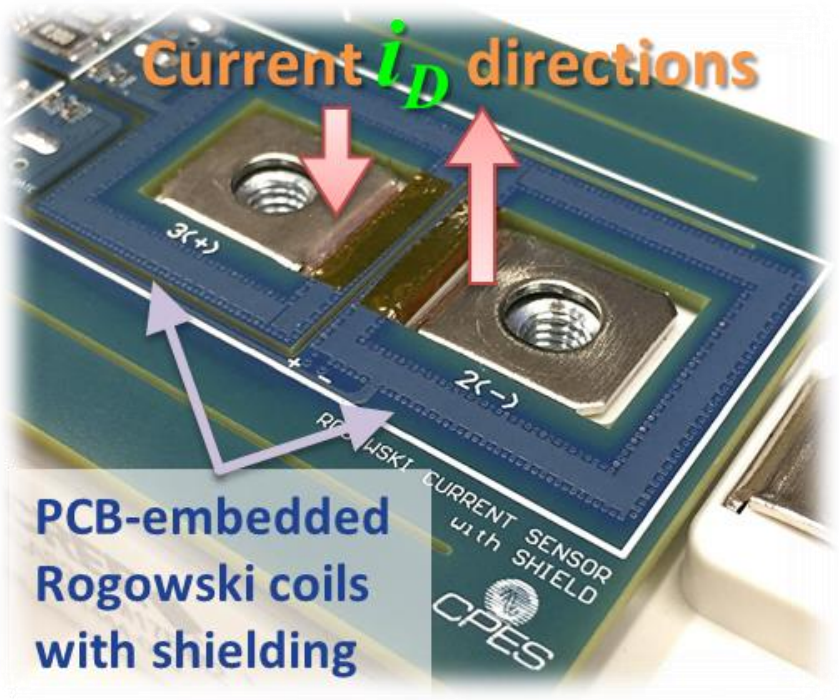


Figure 4-16 Rogowski coil prototype

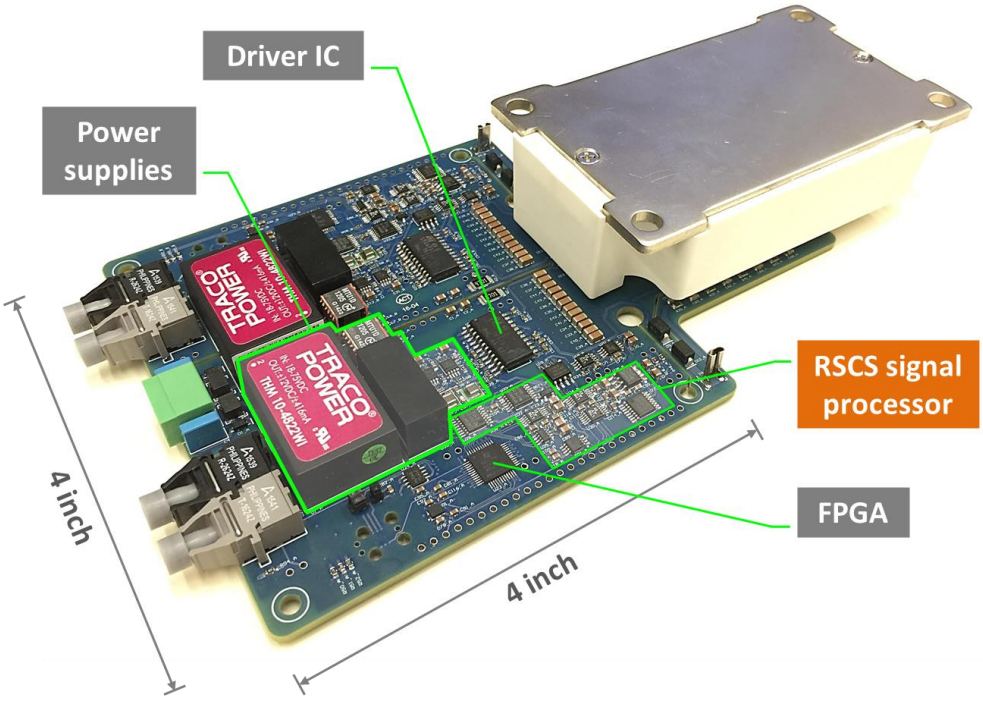
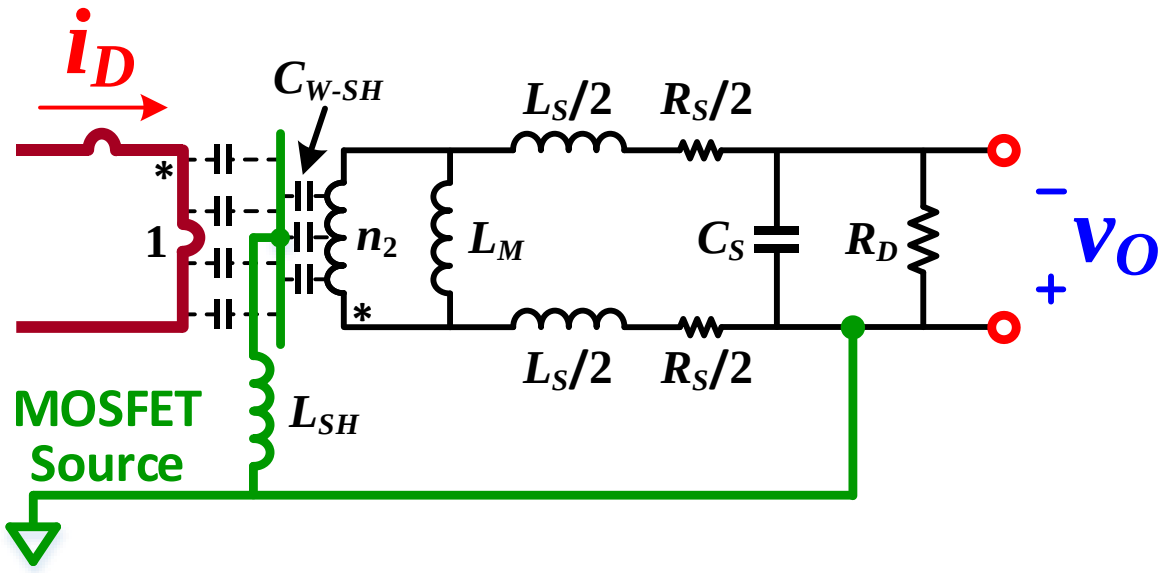


Figure 4-17 Gate driver prototype

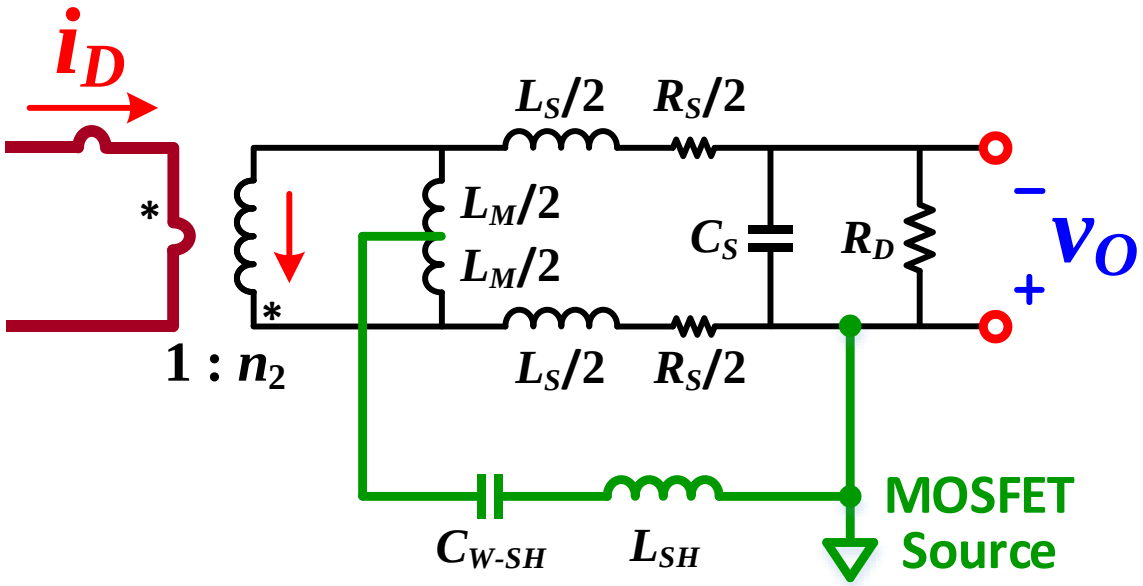
4.4 Rogowski Switch Current Sensor Validation

4.4.1 Modeling of Rogowski coils and Shielding

The circuit model of the fabricated Rogowski coil of the RSCS including the shielding parasitics is shown in **Figure 4-18(a)**. The primary side is assumed to be an ideal current excitation regardless of the influence from the RSCS, so the primary side leakage inductance is not considered. n_2 is the Rogowski winding number. L_M is the magnetizing inductance of the coil. L_S is secondary-side leakage inductance. R_S is the winding resistance. C_S is the EPC of the windings. R_D is at the coil terminals serving as a damping resistor. L_{SH} is the trace inductance from the shielding to the ground. $C_{W\text{-}SH}$ is the winding-to-shielding parasitic capacitance, which is equivalently added to C_S. Therefore, it is reasonable to model $C_{W\text{-}SH}$ as a lumped capacitor. The simplified equivalent circuit model in **Figure 4-18(b)**, where $C_{W\text{-}SH}$ is connected to the middle of the magnetizing inductance L_M. The parameters of this model have been derived using an impedance analyzer and a set of double-pulse test data by a few steps. The model has been validated by the measurement of various configurations.



(a)



(b)

Figure 4-18 Equivalent circuit model of the Rogowski coil, with shield

First of all, the equivalent circuit can be simplified by disconnecting the trace from shielding to ground. By this configuration, the equivalent circuit model is simplified as **Figure 4-19**. The mutual inductance is calculated using (4-2) derived from (4-1) based on a test data. I_{D_NOM} is the nominal sensed current, and $V_{INT\_OUT\_NOM}$ is the nominal output voltage according to a designed transfer gain G_{RSCS} of 5 mΩ. R_{i1} and C_f are the actual fine-tuned values in the schematic in **Figure 4-14**, which ensure the required transfer gain in experiments. Then the secondary-side magnetizing inductance L_M is calculated based on (4-3)

(4-2) $$M = \frac{v_{INT\_OUT\_NOM}}{i_{D\_NOM}} R_{i1} C_f$$

(4-3) $$L_M = n_2 M$$

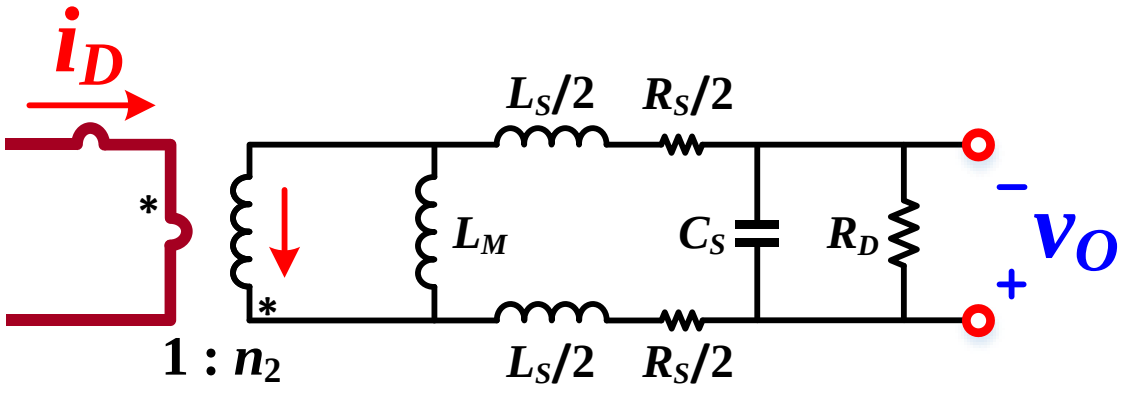


Figure 4-19 Equivalent circuit model of the Rogowski coil, without shield

The first step of impedance measurement is to derive L_S, R_S, and C_S. The damping resistor R_D and the primary-side bus-bar are both configured as open-circuit. Therefore, the equivalent circuit is simplified as the **Figure 4-20**. The measurement is conducted via the two red terminals, and the frequency-domain impedance curve is shown as the right side. Below 100 kHz, the impedance represents the R_S value. Between 1 MHz and 40 MHz, the impedance is almost a straight line because the L_S impedance is dominant. The resonant frequency f_{RES1} is determined by the L_S and C_S, so the EPC value can be calculated by (4-4)

(4-4)
$$C_S = \frac{1}{4\pi^2 f_{RES1} L_S}$$

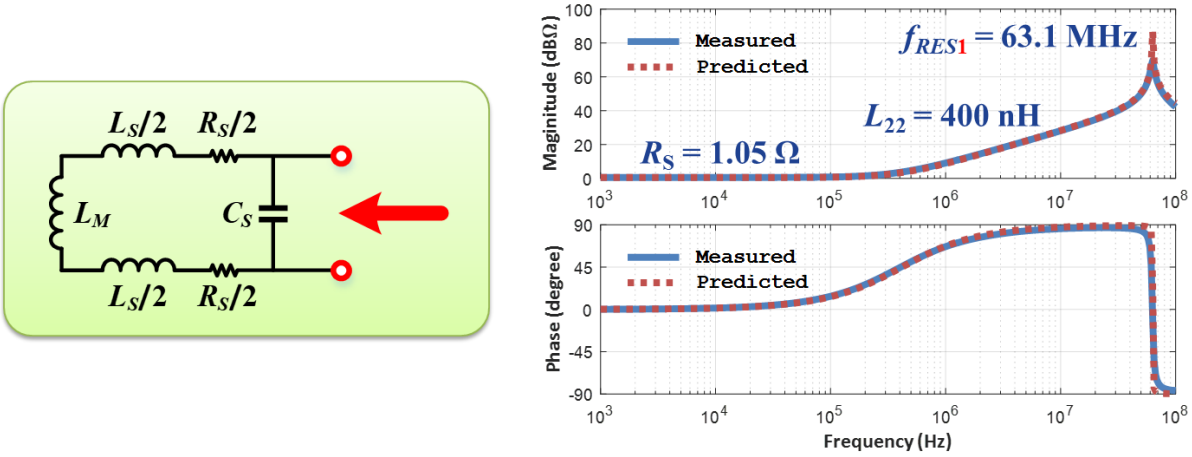


Figure 4-20 Impedance measurement of the Rogowski coil, without shielding, Step 1

The second step of impedance measurement is to derive $C_{W\text{-}SH}$ and L_{SH}. The two output terminals of the windings are shorted, and the shielding layers are connected to the ground. The measurement is conducted via the two red terminals in **Figure 4-21**. The impedance curve shows that below 40 MHz the characteristics are dominated by $C_{W\text{-}SH}$, and it is calculated according to the slope. The resonant frequency f_{RES2} is determined by the L_{SH}, L_S, L_M, and C_S, so the L_{SH} value can be calculated by (4-5)

$$L_{SH} = \frac{1}{4\pi^2 f_{RES2} C_S} - \frac{L_S + L_M}{4} \tag{4-5}$$

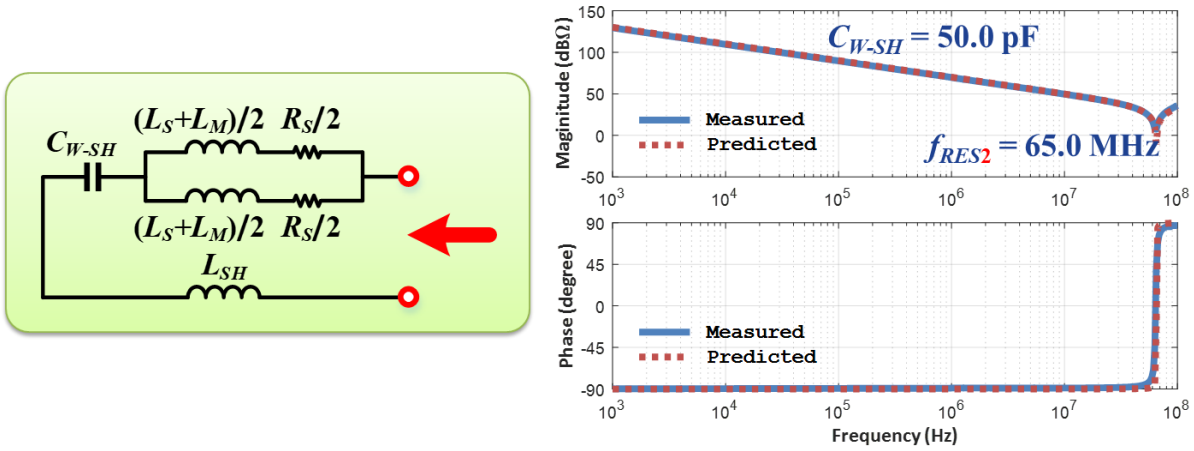


Figure 4-21 Impedance measurement of the Rogowski coil, with shielding, Step 2

This calculation is based on the aforementioned assumption that $C_{W\text{-}SH}$ is connected to the middle of the magnetizing inductance L_M, splitting it into half and half. In order to validate this assumption, another measurement has been conducted. The terminal configurations are modified again. One of the winding terminals is connected jointly with the shielding ground, and the other winding terminal remains open-circuit. Accordingly, the equivalent circuit is modified as shown in **Figure 4-22**. Since all the parameters have already been derived in previous steps, the derived model is compared with the measured model. The results show that the two impedance matches very well below 70 MHz. The first resonant frequency f_{RES1} at 63.1 MHz still exist in this setup, while f_{RES2} is no longer observed. A new resonant frequency f_{RES3} at 42.8 MHz is generated.

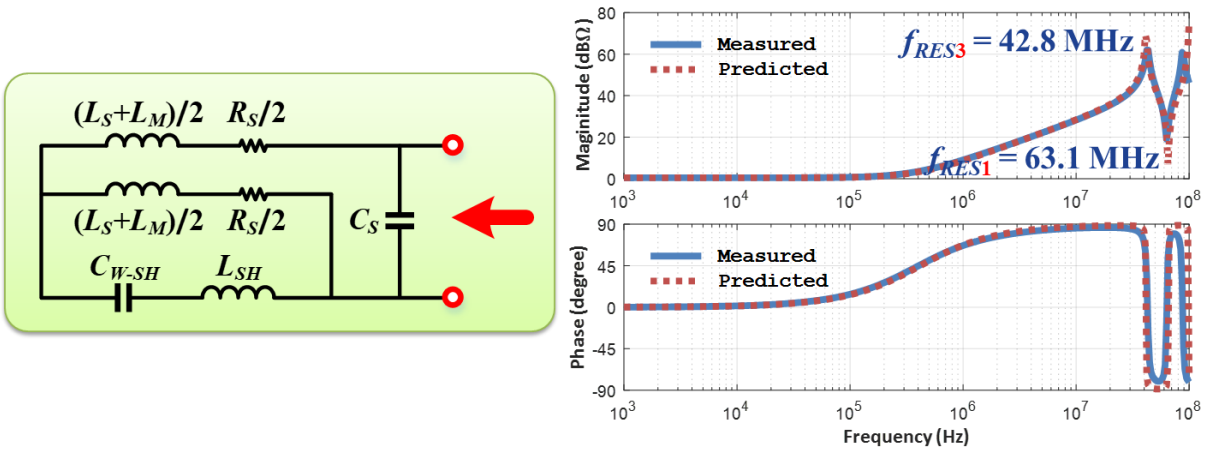
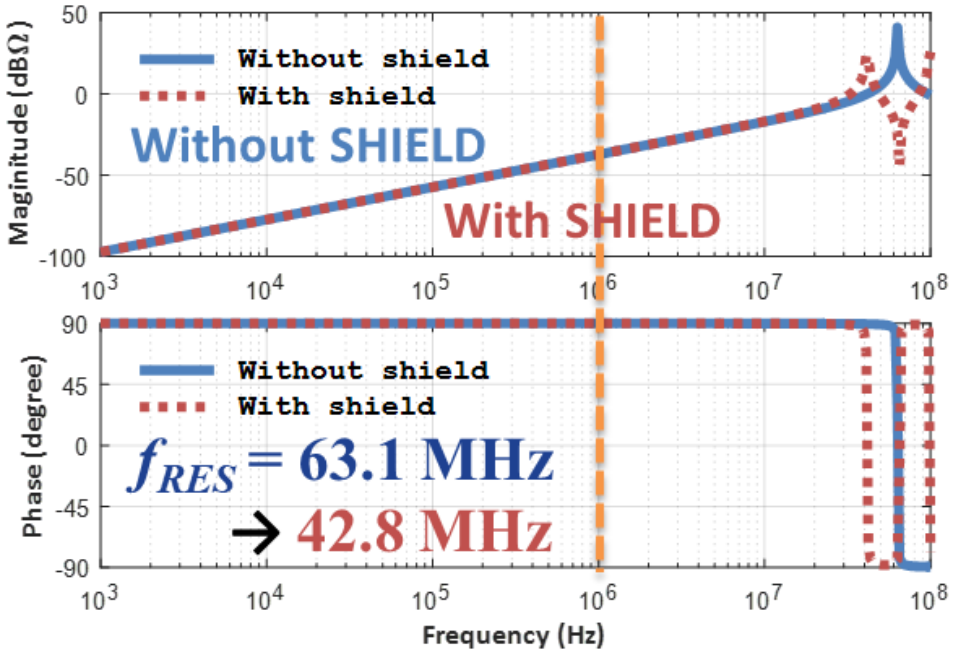


Figure 4-22 Impedance measurement of the Rogowski coil, for model validation, Step 3

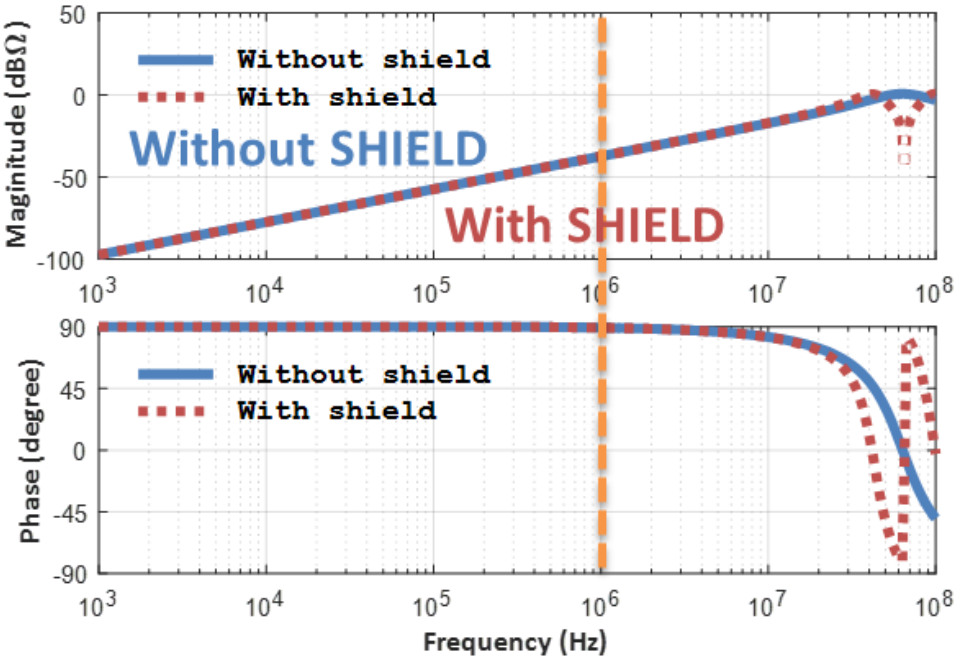
By those steps of impedance measurement, the parameters have been fully derived. Plus, the results prove that the assumption that the lumped capacitor $C_{W\text{-}SH}$ is connected to the middle of the L_M is correct, otherwise, the two impedance in **Figure 4-22** would not match. All the parameters are given in **Table 4-1**. Finally, the equivalent circuit model of the Rogowski coils is derived as **Figure 4-23(a)**. The shielding of Rogowski coils reduces the winding resonant frequency from 63.1 MHz to 42.8 MHz. At 1 MHz, defined by the specifications, the Rogowski coils have very good inductive characteristics. The effect of damping resistance R_D has also been compared. **Figure 4-23(b)** shows that if R_D is set to 100 Ω, the resonant quality factor can be attenuated very well. In practical applications, integration resistor R_{i1} actually serves as the damping resistance.

Table 4-1 Validated RSCS Parameters

Parameter	Value	Parameter	Value
G_{RSCS}	5 mΩ	$C_{W\text{-}SH}$	50.0 pF
n_2	152 turn	L_{SH}	20.0 nH
M	2.51 nH	f_{RES1}	63.1 MHz
L_M	382 nH	f_{RES2}	60.0 MHz
L_S	18.0 nH	f_{RES3}	42.8 MHz
R_S	1.05 Ω	R_{i1}	125 Ω
C_S	15.9 pF	C_f	4.0 nF



(a)



(b)

Figure 4-23 Transfer gain of the PCB-embedded Rogowski coils

4.4.2 Experimental Validation

(a) RSCS input-output performance

Figure 4-25 and **Figure 4-26** shows the RSCS performance at a 5-pulse test, with SiC MOSFET drain current up to 460A and DC bus voltage being 1 kV. The waveforms are labeled on the related schematics in **Figure 4-24**. The SiC MOSFETs are switching at hard commutations, and thus 16 MHz ringing is observed on both the drain current and the drain-source voltage. In **Figure 4-25**, the yellow sensor output v_{SEN_PRT} is designed for overcurrent/short-circuit protection purpose. Its steady-state magnitude matches the Rogowski probe CWT-3B waveform in orange accurately. The ringing magnitude has been partly attenuated with an RC filter to prevent false protection at hard turn-on transients. In **Figure 4-26**, the blue waveform v_{SEN_CTRL} has been further filtered by a two-stage RC filter. All the switching ringings have almost been eliminated to allow this signal suitable for current-mode control purposes. The sensing error is measured less than 2% at the steady state.

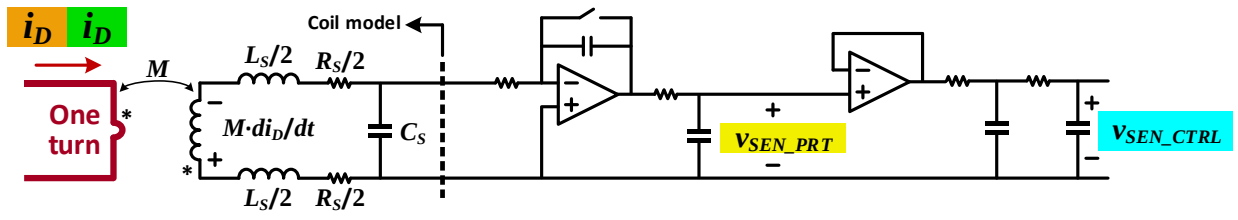


Figure 4-24 Schematics for RSCS input-output performance test

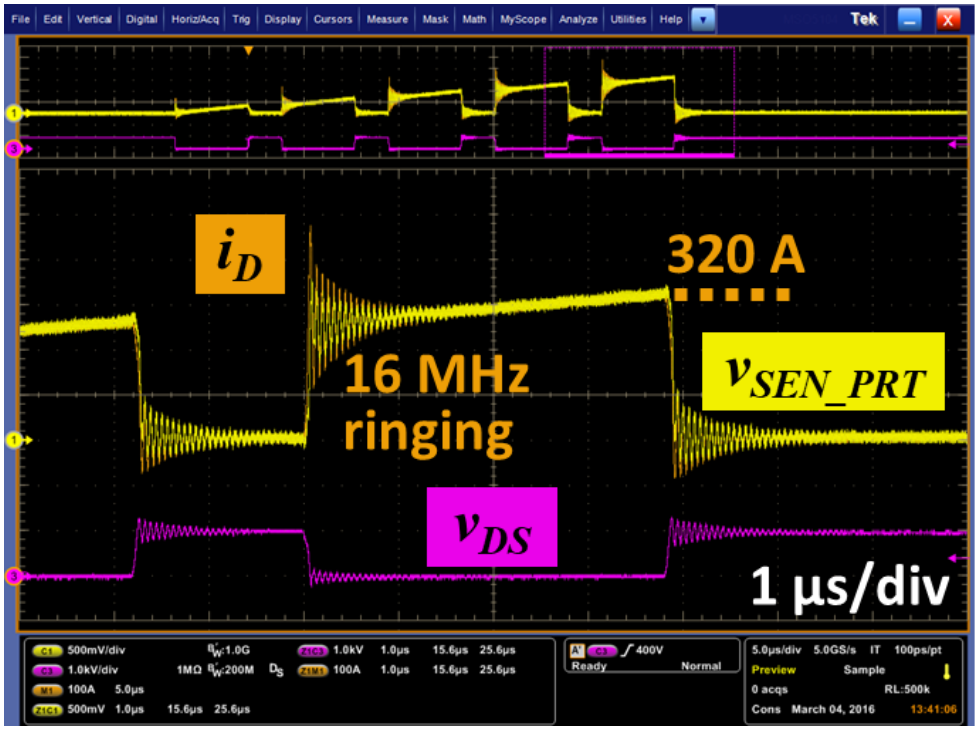


Figure 4-25 RSCS output signal for protection

Figure 4-26 RSCS output signal for current control

(b) RSCS overcurrent/short-circuit test performance

The performance of the RSCS for overcurrent and short-circuit protection has been validated in experiments. The functional block diagram in **Figure 4-27** shows that the RSCS output (RC filters and offset compensation is not drawn) has been given to a high-speed comparator that sets the protection threshold value V_{th}. The output of the comparator notifies the gate driver IC of the overcurrent incident via a low-delay digital isolator. The driver IC STMicro STGAP1AS provides a "SENSE" pin to enable current-based overcurrent protection functionalities, where the output of the digital isolator feeds to. As soon as the overcurrent protection is triggered, two options are provided by the STGAP1AS to shut down the SiC MOSFET. One of them is the "hard protection", shown in **Figure 4-28**. In a single-pulse test, the overcurrent threshold is set as 500 A, corresponding to a V_{th} value of 2.5 V. By placing 1 kV DC bus voltage to a 2 μH load inductor L_O. The inductor current rises to 500 A in 1 μs, and then the protection is triggered. It is observed that the latency between detection and current dropping is about 195 ns, and then it takes about 80 ns for the current to reach zero. The overvoltage peak value at this quick shutdown is about 400 V. The other mechanism is the "soft protection", shown in **Figure 4-29**. A "two-level turn-off" shutdown process is activated in this test, where the value of intermediate voltage is 7 V, and the duration is 750 ns (both are the minimum setup constrained by STGAP1AS). It is observed that the time duration between the detection and the current dropping is about 470 ns, and then it takes about 500 ns to reduce the current to 180 A corresponding to the 7 V gate voltage. This causes a first voltage peak on v_{DS} of 1.1 kV. After that, it takes 50 ns for the current to drop to zero, then a second turn-off voltage peak of 1.05 kV is induced.

By the comparison, the soft protection is more desirable as it is able to limit the turn-off voltage overshoot, which is very critical in real short-circuit protections.

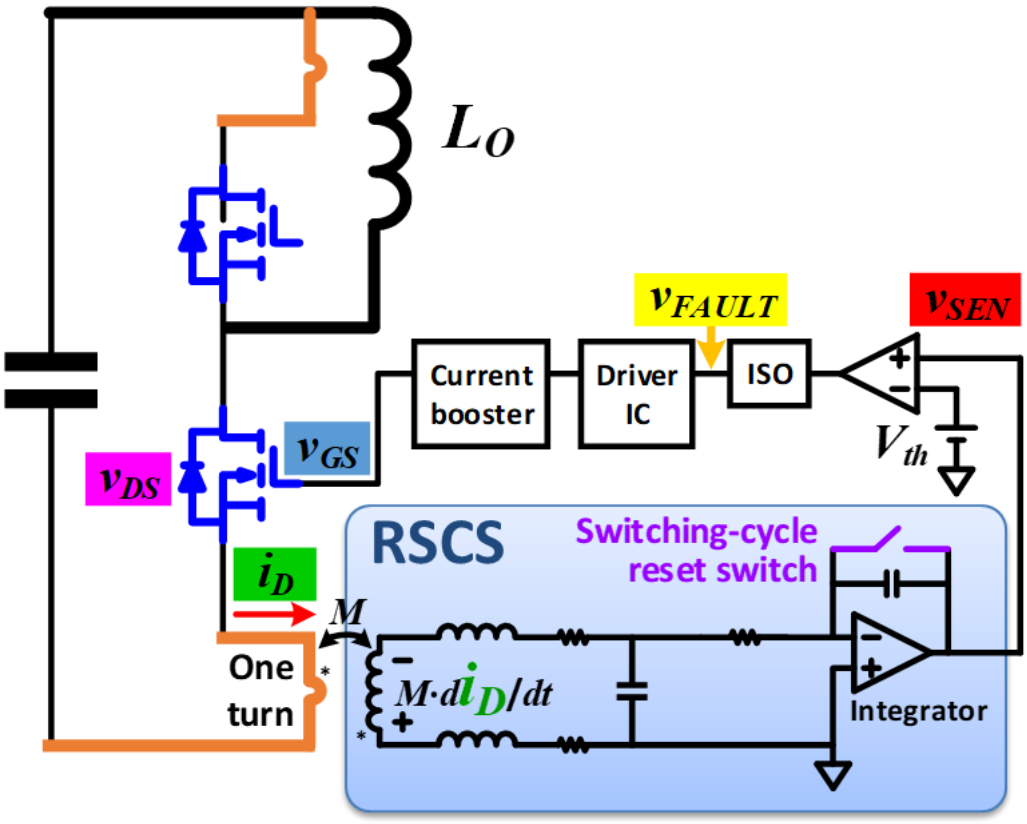


Figure 4-27 RSCS functional block diagram for overcurrent protection

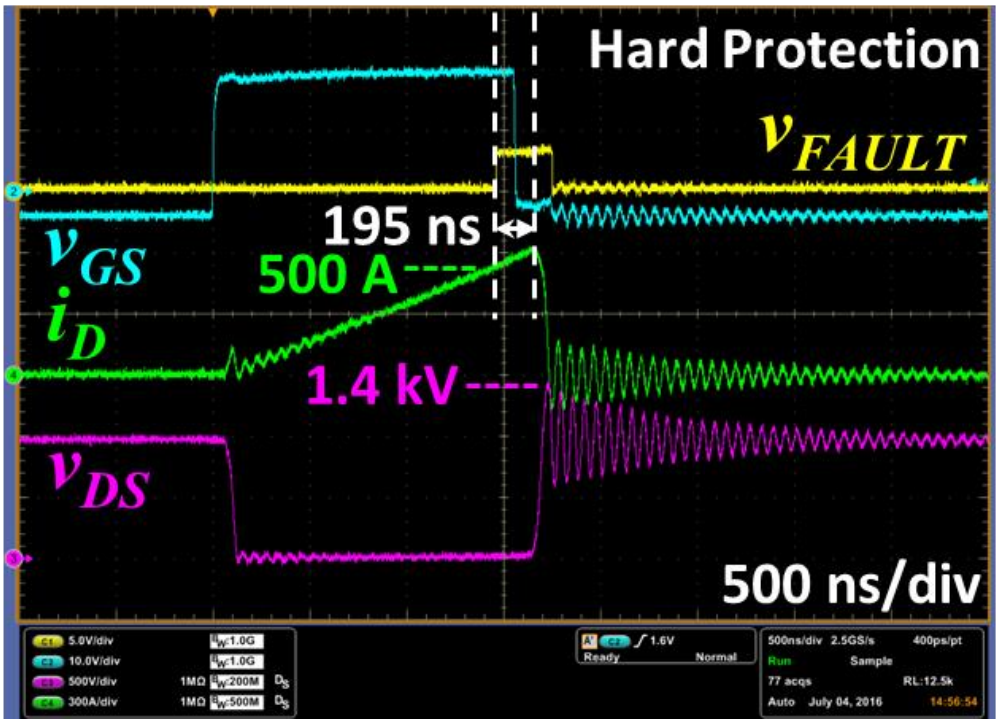


Figure 4-28 RSCS overcurrent protection behavior at hard turn-off

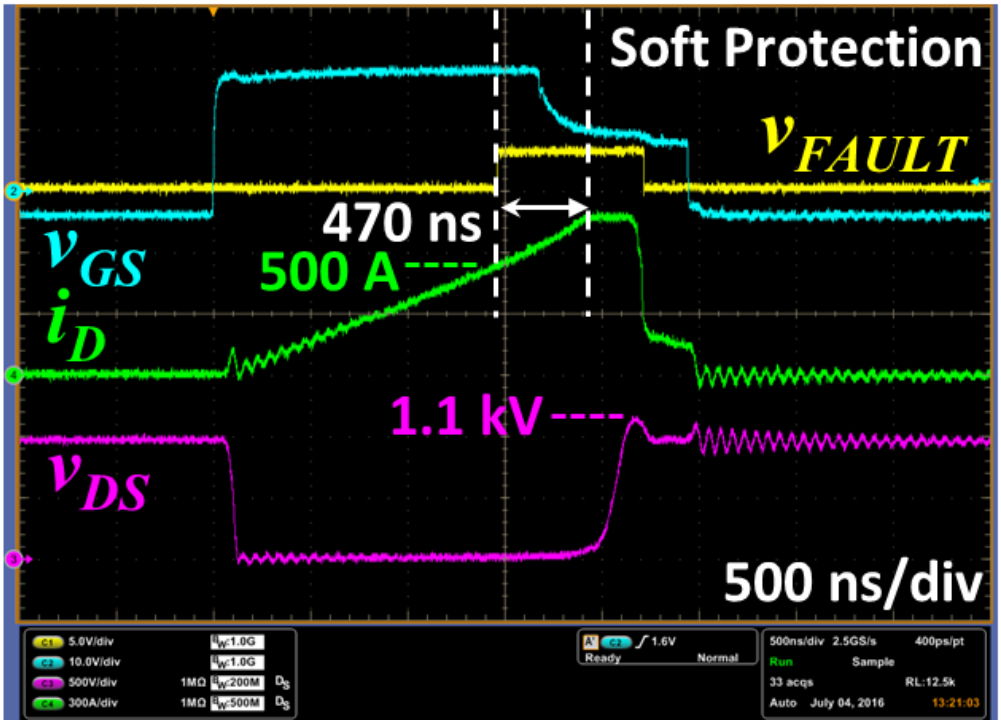


Figure 4-29 RSCS overcurrent protection behavior at soft turn-off

The real Short-circuit test is conducted as well to further assess the RSCS performance refer to **Figure 4-30**. **Figure 4-31** shows the short-circuit incident as soon as the high-side MOSFET is turned on after the low-side MOSFET has been on for 1.5 μs. The threshold of this test is set to be 800 A, corresponding to a V_{th} value of 4 V. At 600 V DC bus voltage, the short-circuit current reaches the threshold within 86 ns, and then it takes 540 ns for the current to drop below 300 A. After 520 ns, the MOSFET is completely off. Because of the fast and soft protection, the 5 kA short-circuit current is safely turned off, with voltage overshoot of only 136 V. This test has been repeated for more than 50 times without damaging the SiC MOSFET module. It is noted that beyond 800 A, the RSCS output voltage v_{SEN} is distorted because the integration OpAmps starts to saturate and enters an abnormal state. Fortunately, the shut-down-and-restart process of the converter after a short-circuit gives the OpAmp enough time to recover.

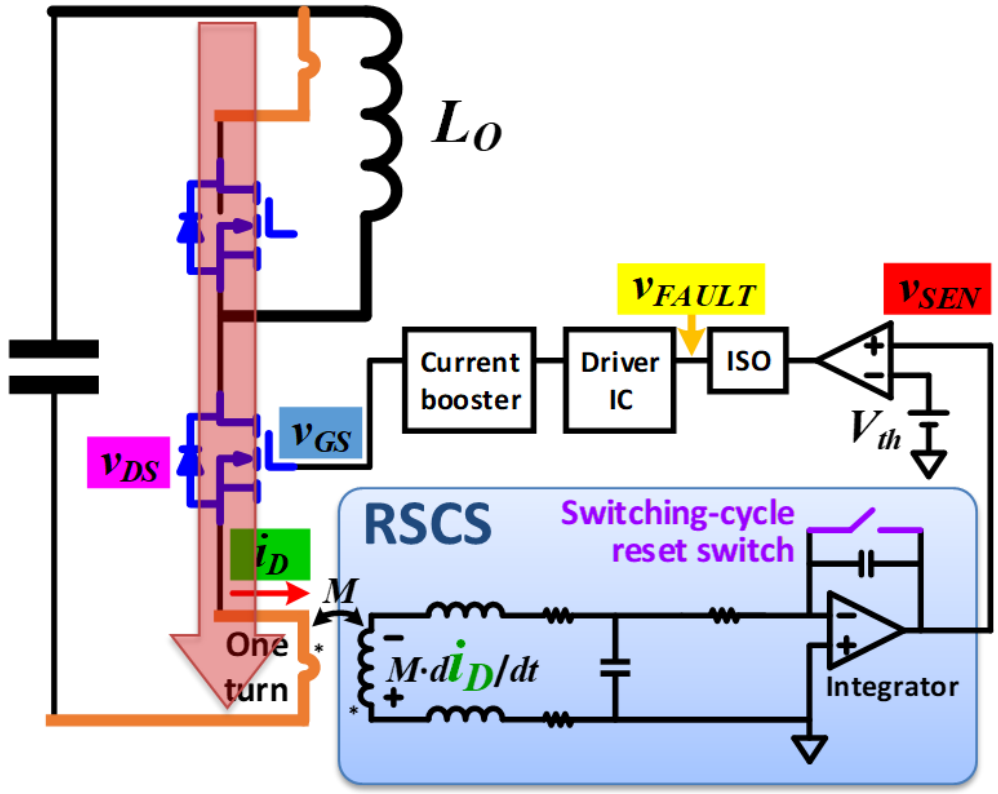


Figure 4-30 RSCS functional block diagram for short-circuit protection

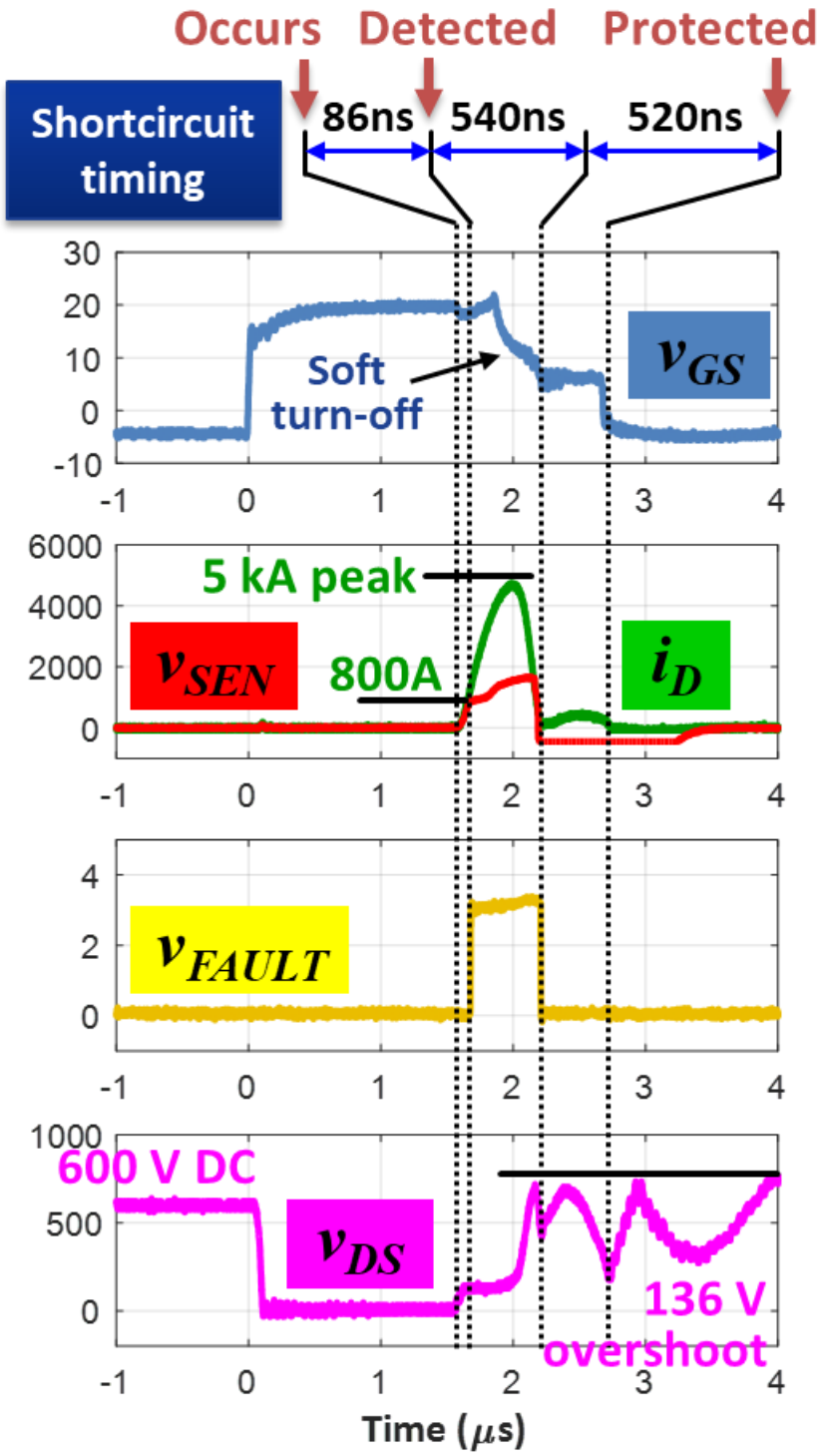


Figure 4-31 RSCS Short-circuit protection behavior at soft turn-off

(c) RSCS for current mode control

The RSCS is also designed to serve as the converter control sensor because the switch currents already carry full information of the phase-leg current. The functional block diagram for current control is shown in **Figure 4-32**. **Figure 4-33** shows the continuous operation of a half-bridge converter running in quasi-square-wave (QSW) DC-DC mode. The switching frequency is 100 kHz (switching period of 10 μs) and the duty cycle is 0.5. The load inductor L_O is 5 μH, and the DC bus voltage is raised to 600 V. In this operation mode, the device current rises from the −150 A to 150 A during the 5 μs conduction time. In **Figure 4-33**, the sensor output V_{SEN_CTRL} shows a very good agreement with the green device current measured by commercial CWT-3B, with proper filtering of switching ringing, shown in the right-top figure. As the peak value of the device current is accurately captured, the RSCS is an excellent candidate for PCM control

Regarding digital signal sampling, the sensor output is converted to digital signals by an ADC at a sampling frequency of 2 MHz. The date is sent to the FPGA via an SPI link to fulfill any control purposes. The FPGA also generates a comparator reference via a DAC, which offers the turn-off references for PCM control. **Figure 4-34** shows that the *ADC_SCLK* and *ADC_SDO* are very clean even at the switching transient. The transmitted binary digital data is collected and calculated to decimal values at the higher-level controller side, which is reconstructed with delay compensation in **Figure 4-35**. The results show that the transmitted digital data matches very well with the original current probe signal.

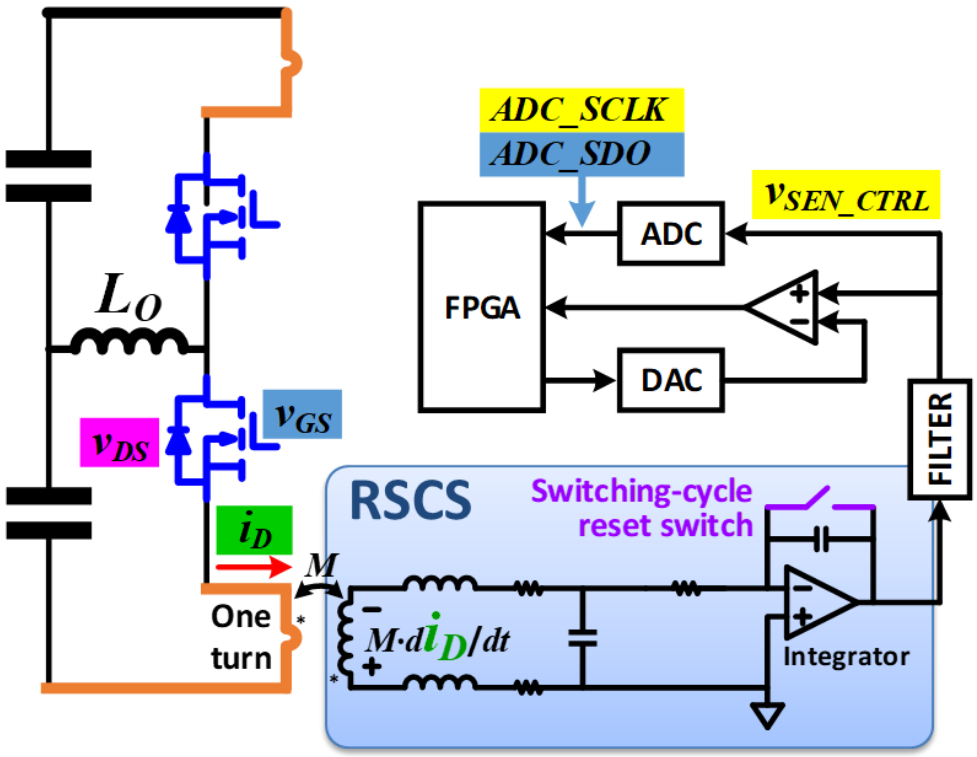


Figure 4-32 RSCS functional block diagram for current control

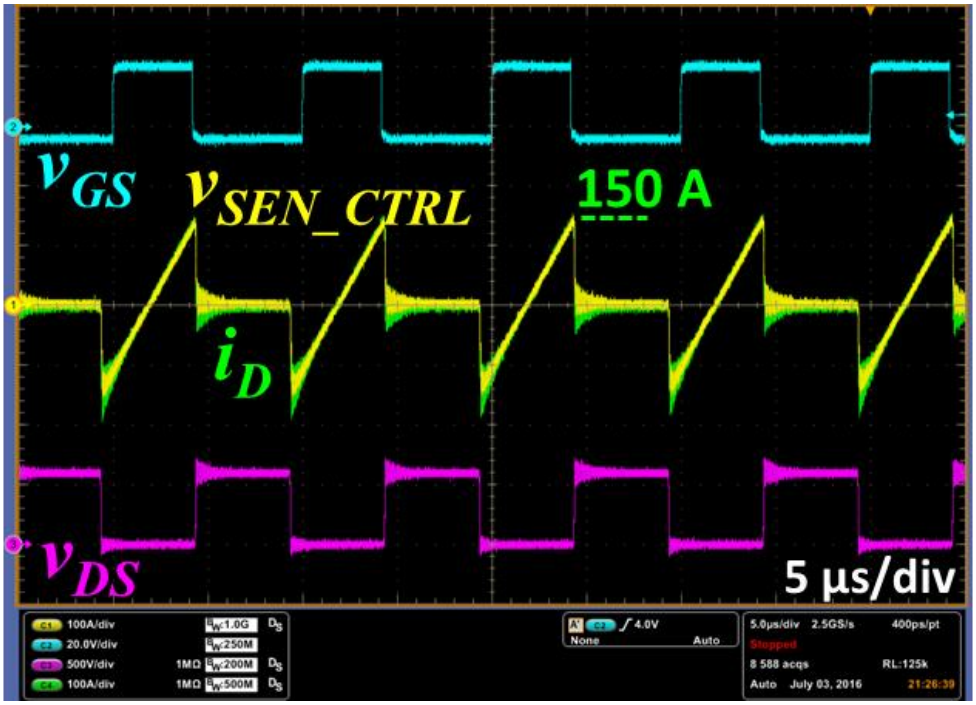


Figure 4-33 RSCS output at quasi-square-wave operation mode

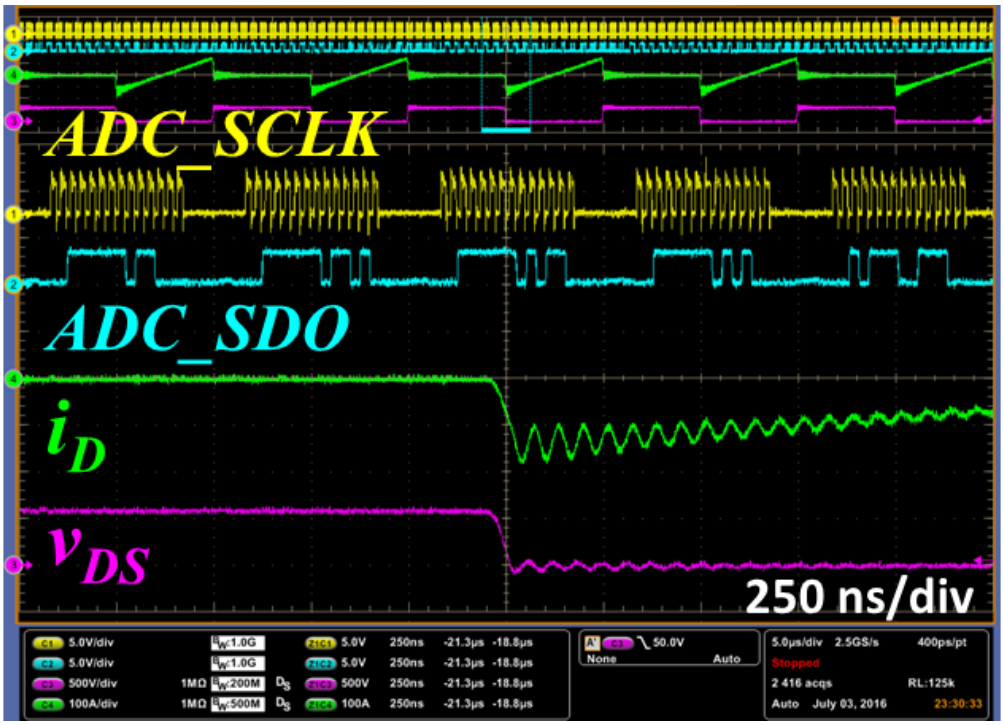


Figure 4-34 ADC output converted from RSCS output

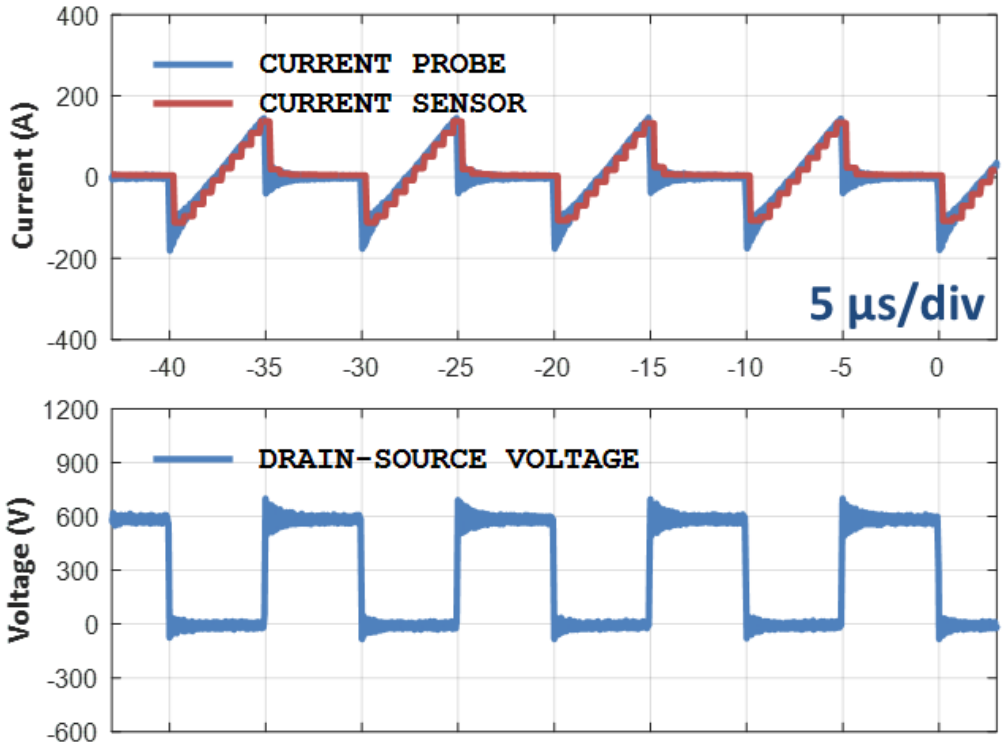


Figure 4-35 Reconstructed decimal switch current signal

Chapter.5 SiC-based Power Electronics Building Block Design

5.1 Introduction

One of the most important features of the MMC converter is the full scalability. The power module of MMC can be stacked in series or parallel to scale up the voltage and current ratings of the MMC. This concept was proposed and termed power electronics building blocks (PEBBs) in 1997 [E.1] -[E.4] . As specified in Chapter 1, the objective MMC converter is based on a PEBB module rated at 1 kV, termed as PEBB1000 in this thesis. It serves as a hardware platform to validate the HCM-SCC control approach.

The power stage of the PEBB1000 is a full-bridge circuit, built by Wolfspeed 1.7 kV SiC MOSFET modules CAS300M17BM2. As the SiC MOSFET modules are able to switch 5x faster than Si IGBTs at the same voltage and current ratings, the passive component size should be accordingly reduced by a similar factor. However, in high power applications, the power density is not only constrained by the passive component size but also influenced by the control/driving system, insulation clearance, and creepage, etc. Therefore, the high-density design is a comprehensive study that requires inter-discipline expertise such as electrical, thermal, mechanical and insulation techniques. In addition, according to previous test experiences on SiC-based converters, the common-mode and

differential-mode noises aroused by the high *dv*/*dt* and *di*/*dt* rate have demonstrated strong interferences with the converter control and auxiliary system. Abnormal behaviors and false protections occur now and then without being explicitly understood. Under this background, resolving noise issues and developing working components for the PEBB1000 become the first priority and the basic foundation. On top of that, efforts have been made to minimize the size of each critical component.

The critical components in the PEBB1000 are shown in **Figure 5-1**. This chapter basically focuses on the SiC MOSFET selection and characterization, laminated DC bus-bar, passive components including capacitors and inductors, gate drivers, an auxiliary power supply, isolated digital sensors and a PEBB controller.

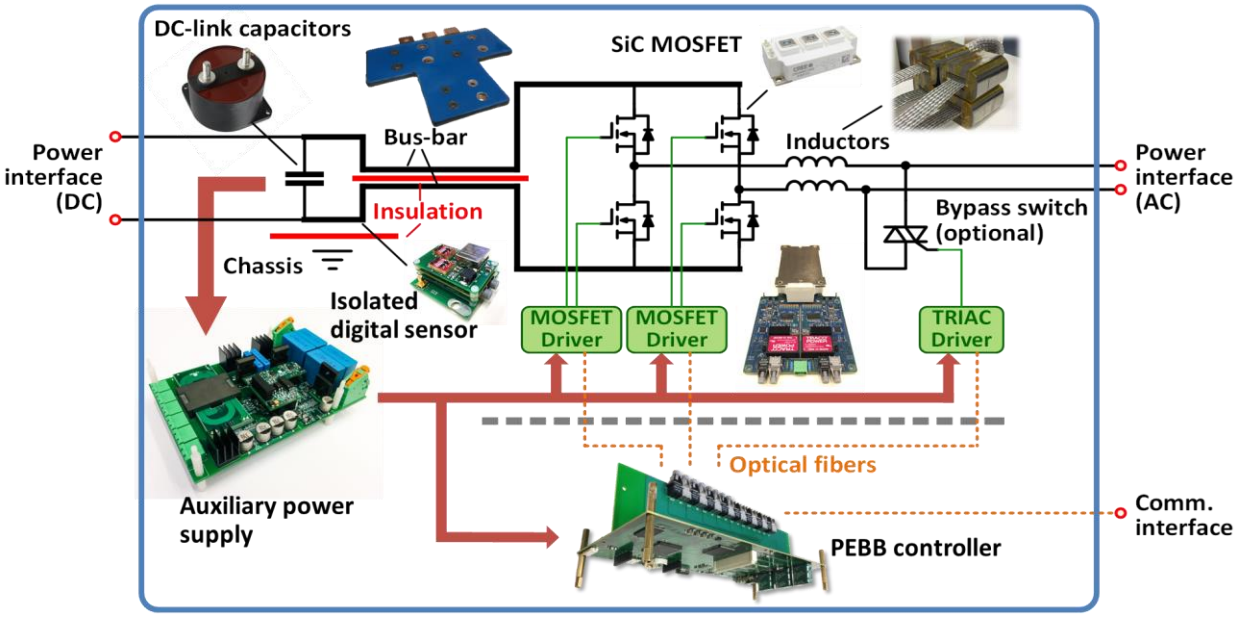


Figure 5-1 Critical components of PEBB1000

5.2 Power Stage Design

5.2.1 DC Bus Design

The DC bus design includes the DC capacitor and the laminated bus-bar design. The DC capacitance value is determined by several operation modes, and possible extension has been reserved. The mid-point of the DC bus is selected as the local PEBB ground to minimize the overall PEBB voltage stress. The laminated bus-bar is designed for low stray inductance and symmetric geometry to balance the common-mode (CM) impedance along the DC bus.

(a) DC Capacitance

Since the PEBB1000 is designed as a universal power processor, it should be able to operate in different applications. One type of application category is the operation mode when the DC capacitor has only a switching-frequency ripple, for instance, the Buck mode. For all this type of operations, the minimum capacitance value is calculated as (5-1).

(5-1)
$$C_{DC} = \frac{I_{MAX}}{10\% \cdot V_{DC} \cdot f_{SW\_MIN}} = \frac{150\sqrt{2}}{10\% \cdot 1000 \cdot 40 \cdot 10^3} = 53\mu F$$

f_{SW_MIN} is the minimum switching frequency 40 kHz, I_{MAX} is the phase current amplitude, V_{DC} is the nominal DC link voltage, and the 10% is the allowable peak-to-peak capacitor voltage ripple within a switching cycle.

The other type of application category is the operation mode when the DC capacitor has not only a switching-frequency ripple but also line-frequency harmonic ripples, for instance, the single-phase inverter mode. For this type of operations, the required

capacitance is usually at least 10x higher than the previous case and is highly dependent on the control schemes for low-frequency ripple reduction. Consequently, the DC-link interface should be reserved on the mechanical layout to retain the possibility of DC capacitance extension.

In addition, the mid-point of the DC bus is connected to the chassis. The impedance from the mid-point to the positive/negative DC bus should be low at high frequencies so that the DC-link capacitors can serve as a pair of CM Y-capacitors that prevent the CM current flowing out of the DC terminals. In that regard, the DC-link capacitor bank should be designed in the form of "series and parallel". Finally, 2x2 off-the-shelf film capacitor AVX FFVS6B0586K have been selected to construct the DC link. Each capacitor is rated at 800 V, 58 μF, and 83 A. The total DC-bus capacitor bank differential-mode (DM) rating of capacitors is 1600 V, 58 μF, and 166 A, whereas the CM rating is 800 V, 232 μF, and 332 A.

(b) Laminated bus-bar

The role of the PEBB laminated bus-bar is to link the half-bridge device modules and the capacitor bank. In addition, the bus-bar is used to achieve series or parallel association of the dc capacitors in the capacitor bank. A basic solution is to use a simple copper sheet to connect the components. Even if a copper sheet is less inductive than conventional wires, the stray inductance is still too high with respect to the large current variations of power electronics. The main drawback of using a simple copper sheet is a large current unbalance between the different access points in addition to its large stray

inductance. Although machining apertures in the sheet is a solution to compensate this unbalance, the aperture results in an increase in partial inductance. The multi-layer laminated bus-bar is an alternative solution which results in decreased stray inductance by taking advantage of the large coupling between the sheets.

For most power electronics circuits, there are a high number of power switches and dc bus capacitors. Even considering just the capacitor bank of a PEBB for high-power applications, the bus-bar usually requires more than two layers. The PEBB1000 shown in **Figure 5-1** requires a three-layer bus-bar to enable the series-parallel configuration of the dc capacitors and to ensure there is a link between two half-bridges and the capacitor bank.

The final constructed SiC-based H-bridge PEBB including the bus-bar, capacitor bank, and gate drives with integrated Rogowski current sensor for short circuit protection is shown in Fig. 6. Note that the experimental results for one half-bridge of the PEBB are shown in this paper, and the results for the other bridge are similar due to the PEBB's symmetry. More design considerations and details can be found in [E.5] .

5.2.2 AC Inductor Design

The highest current-changing rate at the PEBB terminal is the switching-cycle control (SCC) operation mode when PEBB1000 is configured for as a Modular Multilevel Converter (MMC). Under this operation mode, the terminal current is demanded to change from its positive peak to negative peak within 20% of the minimum switching period, calculated as (5-2).

(5-2) $$L_{PEBB} = \frac{V_{DC} \cdot 20\%}{2 \cdot I_{MAX} f_{SW\_MAX}} = \frac{1000 \cdot 0.2}{2 \cdot 150\sqrt{2} \cdot 100 \cdot 10^3} = 4.7\mu H$$

Considering the power cable stray inductance, the DM inductance value is designed as 4 μH. In order to have a symmetric design, the DM inductor is split into two identical parts connected to the two phase-legs of the full bridge. Each inductance value is 2 μH, and take a maximum current of 300 A defined by the PEBB specifications. It is noted that this is a high-current small-inductance inductor, which is usually realized by an air-core or single-turn structure. The former one has low power density and its adjacent flux usually causes noise issues. The latter one has high power density, enclosed flux loop, and is highly manufacturing-friendly as the thick copper bus-bar can be easily assembled through the core windows. Accordingly, the single-turn structure has been selected.

The next steps are to select proper core material, size, number and air gap length, to optimize the inductor loss and size. The inductance design equation is

(5-3) $$L_{PEBB} = \frac{\mu_0 A_C n^2}{l_g}$$

where μ_0 is the permeability constant $4\pi \cdot 10^{-7}$ H·m^{-1}, A_C is the core area, n is the turn number "1", l_g is the air gap length. The maximum flux density in operation expressed as (2-11) should be around half of the saturation flux density B_{SAT} of the core material.

(5-4) $$B_{MAX} = \frac{n\mu_0 I_{MAX}}{l_g}$$

The two equations infer that for a given core material and inductance value L_{PEBB}, larger core area A_C leads to larger air gap length l_g, then the flux density can be reduced to decrease core loss density and avoid saturation. In this case, larger A_C means bigger cores or larger number of cores are used to construct the single-turn inductor, paying the penalty of increased volume and weight. Two series of magnetic material, the Metaglas® AMCC and the FINEMET® F3CC, has been investigated for the inductor design. Metaglas® AMCC is one type of Amorphous metal with saturation flux density B_{SAT} of 1.56 T. FINEMET® F3CC is a type of Nanocrystalline material with B_{SAT} of 1.23 T.

Nine types of cores with different size has been investigated and the needed number, volume, and weight have been calculated accordingly. The number of cores must be an odd integer because of the symmetric layout requirement. Finally, the AMCC-8 and F3CC0008 have been selected and compared. 6 pairs of them give the 2 μH for one phase leg, and totally 12 pairs of cores are needed for two phase-legs. In a validation test, **Figure 5-3** shows that the loss of AMCC-8 DM inductor was out of the PEBB's cooling capability

with the temperature rising above 150°C in 10 minutes. As a comparison, **Figure 5-4** shows that under the same condition, the temperature of F3CC0008 DM inductor stays at 105°C. Finally, the F3CC0008 has been selected to build the DM inductor, and the structure is as shown in **Figure 5-2**.

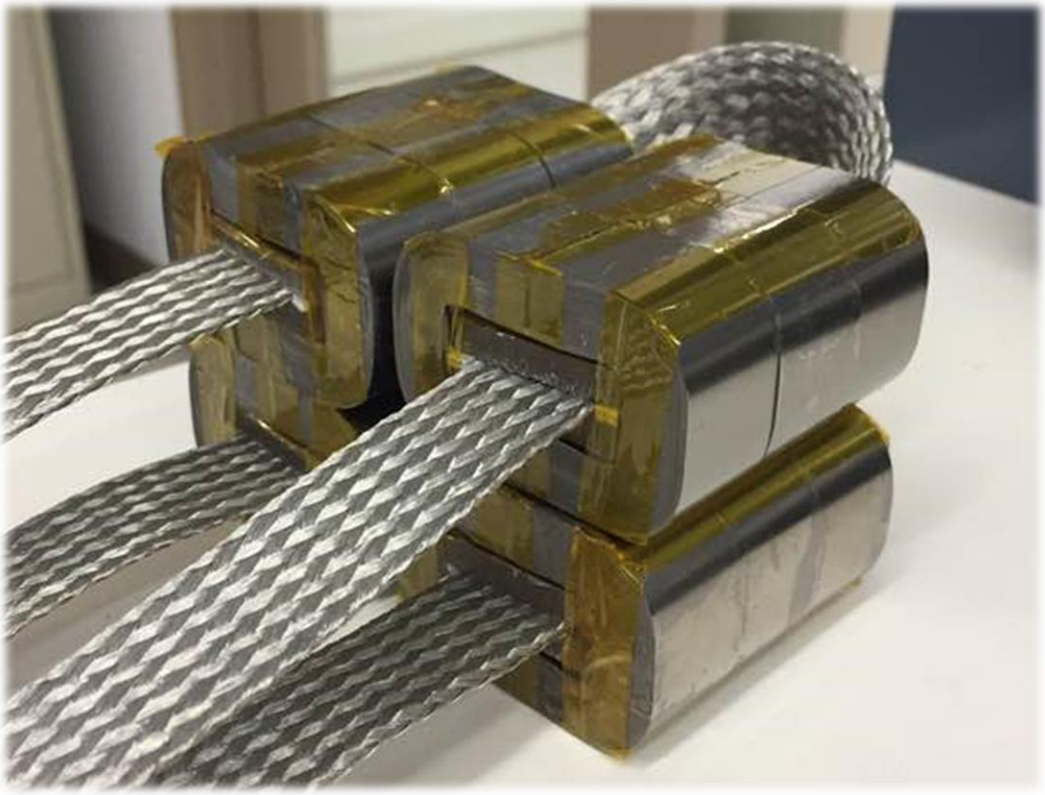


Figure 5-2 Final PEBB inductor prototype

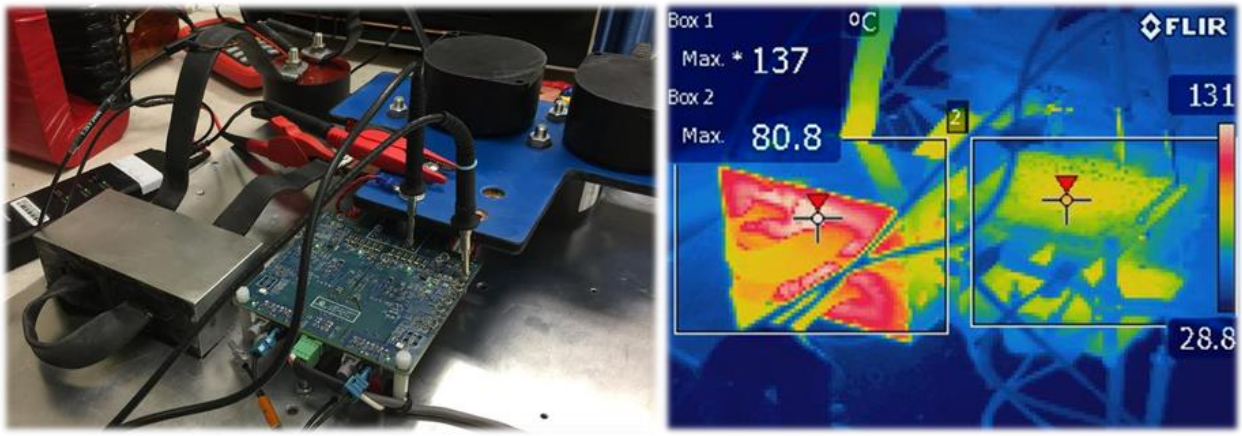


Figure 5-3 Amorphou core inductor: 137°C @100kHz, 300A p-p
10 min with water cooling

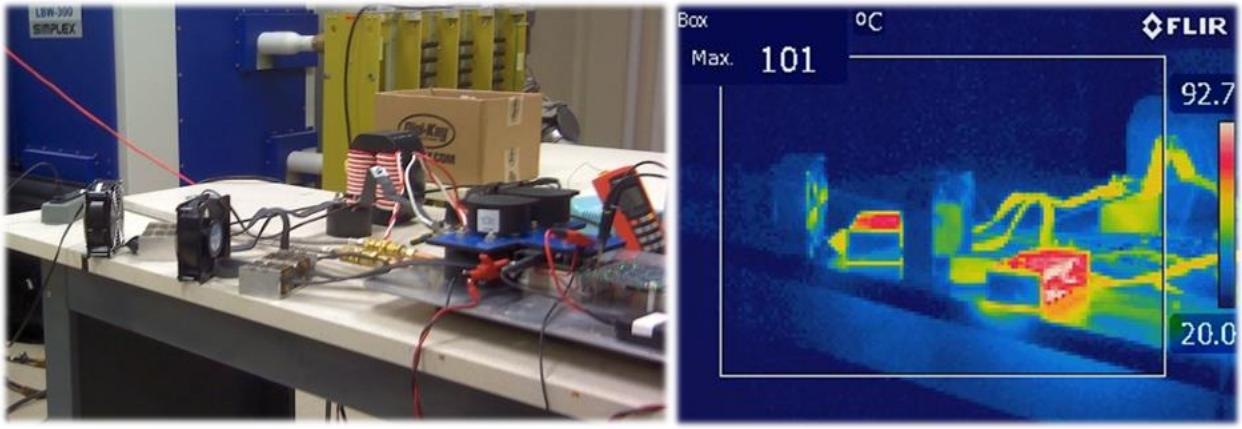


Figure 5-4 Nanocrystalline core inductor: 101°C @100kHz, 300A p-p
30 min with air cooling

5.3 Gate Driver Design

SiC MOSFET as a wide-bandgap device has superior performance for its high breakdown electric field, low on-state resistance, fast switching speed and high working temperature [E.8] . Their high switching speed and low switching loss can boost the switching frequency by a factor of more than 5x, which significantly reduces bulky passive component size in most applications. The overall system cost is comparable to or even lower than conventional Si-based designs due to the reduced material cost. Further, the cost of SiC MOSFETs is also gradually dropping by years due to their growing yield rate. Therefore, SiC MOSFET is of great potential in medium-voltage (MV) high power applications as a substitution of Si IGBTs. A well-performed gate driver with sufficient protections plays a critical role to ensure excellent performance of SiC MOSFET modules. The driver is required to have features such as low propagation delay, high driving current, good dv/dt immunity, and effective protections with correct detection and fast response. According to those requirements, the specifications of the gate driver is given in **Table 5-1**.

For the 1.2 kV IGBTs, a number of commercial driver ICs has been well developed with sufficient isolation rating and protection functionalities. Those driver ICs are fast enough to drive 1.2 kV SiC MOSFETs, and some commercial driver boards have been designed based on the ICs. When it comes to 1.7 kV or higher rated device voltage, the isolation strength of the driver ICs becomes insufficient. In commercial designs, fiber-optic cables or pulse transformers are used to realize isolation for signal propagation channels, while isolated power supply for power channels. The non-idea isolations usually come

along with input/output parasitic capacitance, which is a low impedance path for high-frequency common-mode noises. The CM current magnitude is determined by the switching-transient dv/dt, and the frequency by the transient slope time. A well-designed power architecture is able to attenuate the CM noise going through the sensitive circuity on the gate driver board, in order to avoid malfunction or false triggering. Therefore, first of all, the different power/signal architectures have been studied based on the system parasitics model, followed by detailed circuit designs including driver IC selection, current booster, soft turn-off, and active Miller-clamp. A solution of self-balanced paralleled current booster has been proposed not only to meet the driving current requirement but also to enable the two-level soft turn-off upon short-circuit. A circuit for active Miller-clamp has been proposed to solve a threshold issue limited by the driver IC. A Rogowski switch-current sensor (RSCS) is embedded within the gate driver PCB as described in Chapter 4.

Table 5-1 SiC MOSFET Datasheet Parameters

Property	Value
Objective SiC MOSFET	CAS300M17BM2 (Wolfspeed)
Device voltage rating	1700 V
Device current rating	225 A @T_C=90°C
Gate charge required	1076 nC
Device Package	62 mm
Maximum switching frequency	100 kHz
Maximum Propagation delays	100 ns
Maximum Propagation distortion	20 ns
Driving voltage	+20 V / −4 V
Maximum gate driving current	30 A

	Functionalities	Under-voltage lockout; Short-circuit protection; soft turn-off; active Miller-clamp

5.3.1 Power/Signal Architecture Design

Isolation of the gate drive is critical when high dv/dt rate and short transient time are involved. The maximum switching transient of the selected device can be as high as 30 V/ns, and the dominant transient frequency is around 10~100 MHz. A good isolation design ensures reliable continuous operation of the SiC converters without wrong gating pulse, false triggering of protection, or other malfunctions. Accordingly, different isolated power/signal architectures are compared to evaluate the noise behaviors within the critical frequency range.

The study of power/signal architectures begins with the equivalent circuit diagram in **Figure 5-5**. This is the most widely used architecture where the signal isolation and power isolation are in parallel and both of them take isolation voltages. In the figure, the common-mode (CM) model of an isolated two-channel gate driver for a half-bridge converter is shown. In the model, only power/ground path of the circuit matters to the propagation of CM current as they are of the lowest impedance. The power and ground traces are usually regarded as short-circuited at a frequency above 1 MHz because there are always tens of micro-Farads decoupling capacitance across each other. As a result, one single line with a “rectangular impedance” symbol of impedance is used to represent the path of power/ground impedance in parallel. This trace impedance is generally very small with only a few nano-henries inductance and milliohms resistance. As far as a CM choke

is concerned, an "inductor" symbol is used to represent the CM choke model (including the equivalent parasitic capacitance of the CM choke). It usually has much larger impedance than the trace impedance at high-frequency range. When an isolation barrier is included in the model, a "capacitor" symbol is applied to represent the input-output parasitic capacitance of the physical isolation barrier, which gives a high impedance at the low-frequency range. The three impedance types of the power/ground trace, CM choke and input-output capacitor at a wide frequency range are shown in **Figure 5-6**. By playing with the three impedances, it is possible to design different CM impedance for the gate driver architecture.

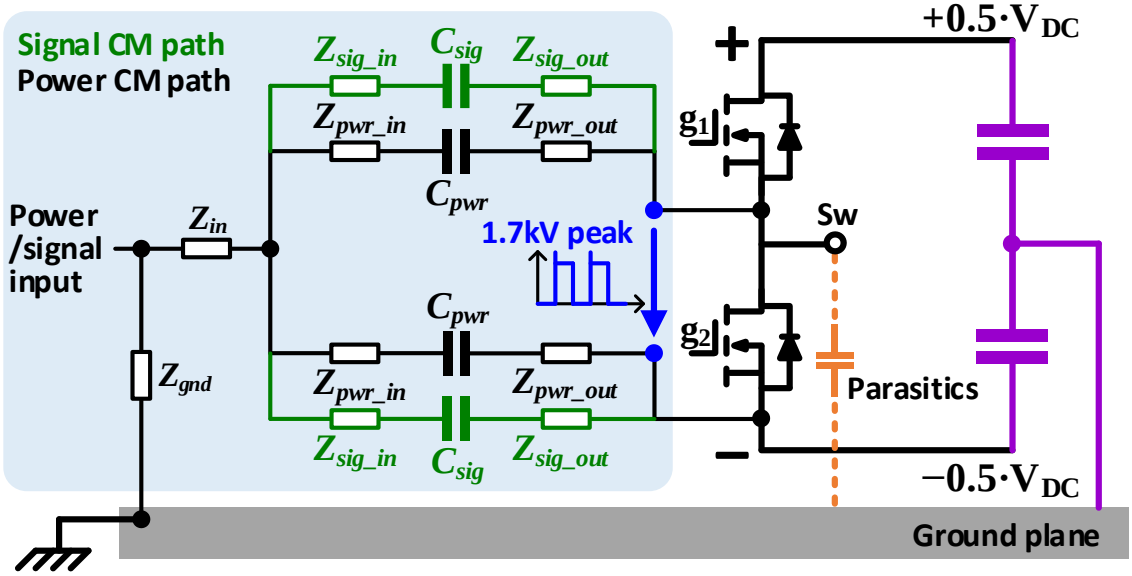


Figure 5-5 DC analysis of the gate driver model

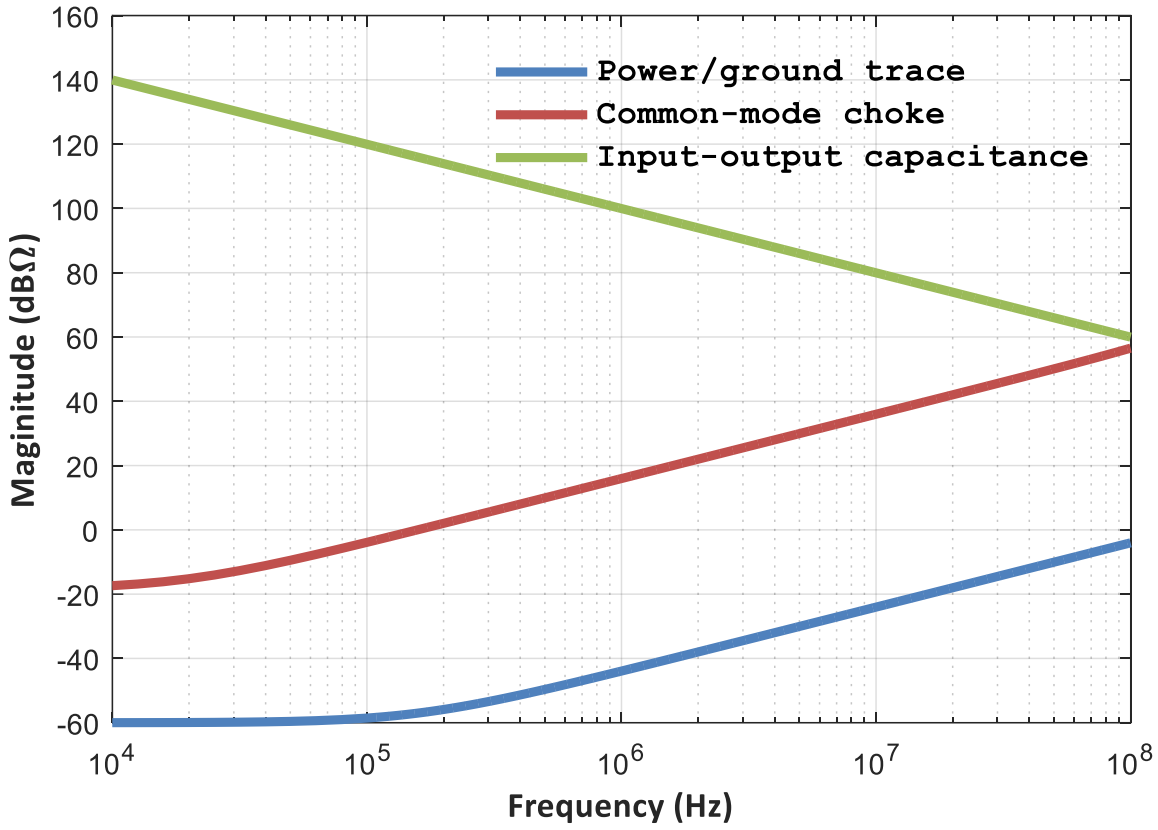


Figure 5-6 Impedance comparison between the three elements of CM model

The gate driver located in the blue shade in **Figure 5-5** is connected to the two source terminals of the two main SiC switches via two lines. The differential voltage across the two source terminals are jumping from zero to a turn-off voltage peak of the bottom device because of the switching behavior, which forms the CM noise source from the power stage to the gate driver network. To the left side of the CM noise source, trace impedance Z_{sig_out}, isolation capacitance C_{sig} and trace impedance Z_{sig_in} construct the CM propagation path along the signal channel. It is noted that Z_{sig_in} and Z_{sig_out} are both dominated by the ground for signal channel. Similarly, Z_{pwr_out}, C_{pwr} and Z_{pwr_in} the CM propagation path along the power channel. Z_{sig_in} and Z_{pwr_in} are connected to a common junction because they share the same control ground in the end. It is the same for the Z_{sig_out} and Z_{pwr_out} because they refer to the same device source potential. The two Z_{sig_in} and two Z_{pwr_in} are connected jointly through an input impedance Z_{in} to the gate driver input and then connected to the system ground via a grounding impedance Z_{gnd}. This is the most widely used isolation architecture to drive commercial Si IGBT and SiC MOSFET half-bridge modules. Further, the middle point of the DC-link capacitor bank is connected to the ground chassis to minimize the overall converter system voltage stress. On the basis of the given model, DC and AC analysis of the design has been carried out to evaluate the CM noise propagation behavior.

(a) DC and Low-Frequency AC Analysis

The DC analysis indicates the static voltage stress over the gate driver isolation barriers. In the DC model of **Figure 5-7**, the trace impedance becomes short-circuited and

the parasitic capacitors are open-circuited. The DC-bus capacitors are treated as constant voltage sources. Under this condition, the low-side isolation barrier takes half of the DC-bus voltage stress $0.5 \cdot V_{dc}$. The switching-node averaged voltage is $D \cdot V_{dc}$, where D is the averaged value of the top switch duty cycle $d(t)$. Accordingly, the high-side isolation barrier will take $(D-0.5) \cdot V_{dc}$ static voltage stress. For a DC-AC system, if the D value is 0.5, the high-side static voltage stress becomes zero. A similar concept applies for low-frequency (e.g. 60Hz and 120Hz) switching-node voltage as well because it is still valid to assume negligible parasitics. The low-side isolation barrier voltage is $0.5 \cdot V_{dc}$ and the high-side one is $(d(\omega t)-0.5) \cdot V_{dc}$, where ω is the fundamental frequency or its low-order harmonics.

In summary, for DC and low-frequency component of the switching voltage, the low-side isolation barrier takes half of the DC-bus voltage, and the high-side will take zero DC stress and low-frequency AC components. Those quasi-static voltage stresses must be considered when designing insulation strength of isolation components such as driver IC, optocoupler or digital isolator, nonetheless, they don't generate high-magnitude CM noises because of the very low frequency.

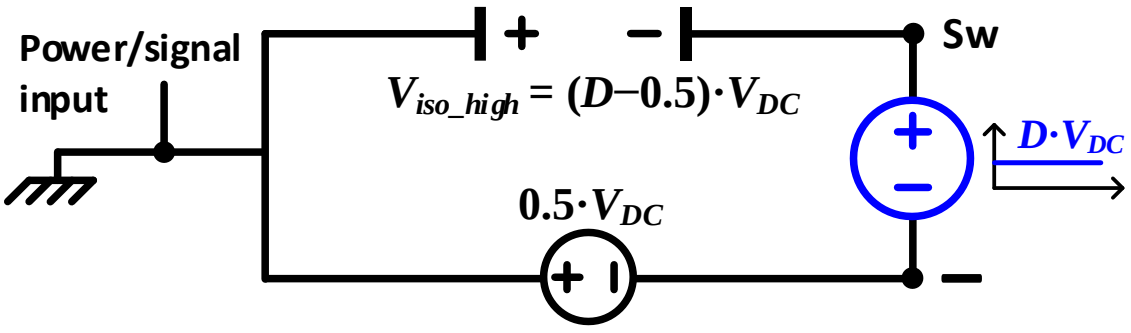


Figure 5-7 DC and low-frequency AC CM model of the gate driver circuit

(b) High-Frequency AC Analysis

The high-frequency AC analysis in this section talks about the switching frequency and the rising- and falling-edge frequency at switching transients. For the SiC MOSFET modules, the high-frequency range of the switching-node noise source v_{NS} is from 10 kHz to 100 MHz, so parasitics of components and connections must be modeled. As shown in **Figure 5-8**, the DC capacitor C_{DC} of 232 μF in the CM model is 4 times of the DM DC-bus capacitance value in **Figure 5-5**. The stray impedance of grounding cable Z_{gnd1} is estimated to include 50 nH inductance and 1 mΩ resistance, that connects the DC capacitor C_{DC}. The SiC MOSFET packaging (switching node to base plate) capacitance C_{para} is 0.2 nF, and from the base plate to the grounding point there is grounding impedance Z_{gnd2} that includes 20 nH inductance and 0.5 mΩ resistance. All the power/ground trace impedances Z_{sig_in}, Z_{sig_out}, Z_{pwr_in}, Z_{pwr_out}, and Z_{in} on the gate driver board are estimated to be 1 nH and 1 mΩ. The grounding network impedance Z_{gnd_net} mentioned in Figure 3-1 is specified here to be a paralleled RC circuit constructed by Y capacitor and grounding resistors. The Y capacitor C_{gnd_net} of 0.2 μF bypasses the CM current generated by the noise source v_{NS} to the ground plane instead of going back to the front-end auxiliary power supply via power input. The resistor R_{gnd_net} of 50 kOhm offers a static voltage potential at the input side for low frequency. The most critical values are the isolation capacitance C_{sig} and C_{pwr}, which are determined by the actual commercial component part. Most of the off-the-shelf signal isolators have C_{sig} value of 1~2 pF, and among commercial isolated power supplies higher than 6 W, the C_{pwr} is around 10~20 pF. Since the purpose of this analysis is for a comparative study of different architectures, the absolute value of a single device does not

influence the comparison results as long as they are in a reasonable range. Therefore, the C_{sig} is set to be 1.6 pF according to the measured capacitance of a commercial gate driver IC STMicro STGAP1AS, and the C_{pwr} is 17 pF according to the value of an off-the-shelf isolated power supply THM 10-4822WI. Based on the given CM model of the gate driver and corresponding power stage, the high-frequency AC response is studied at a range from 10 kHz to 100 MHz. The lower limit is set because most SiC MOSFETs switch at above 10 kHz. The upper limit is set at 100 MHz because frequency beyond that value almost touches the radiated frequency (RF) range, where the above-mentioned equivalent circuit model is no longer valid.

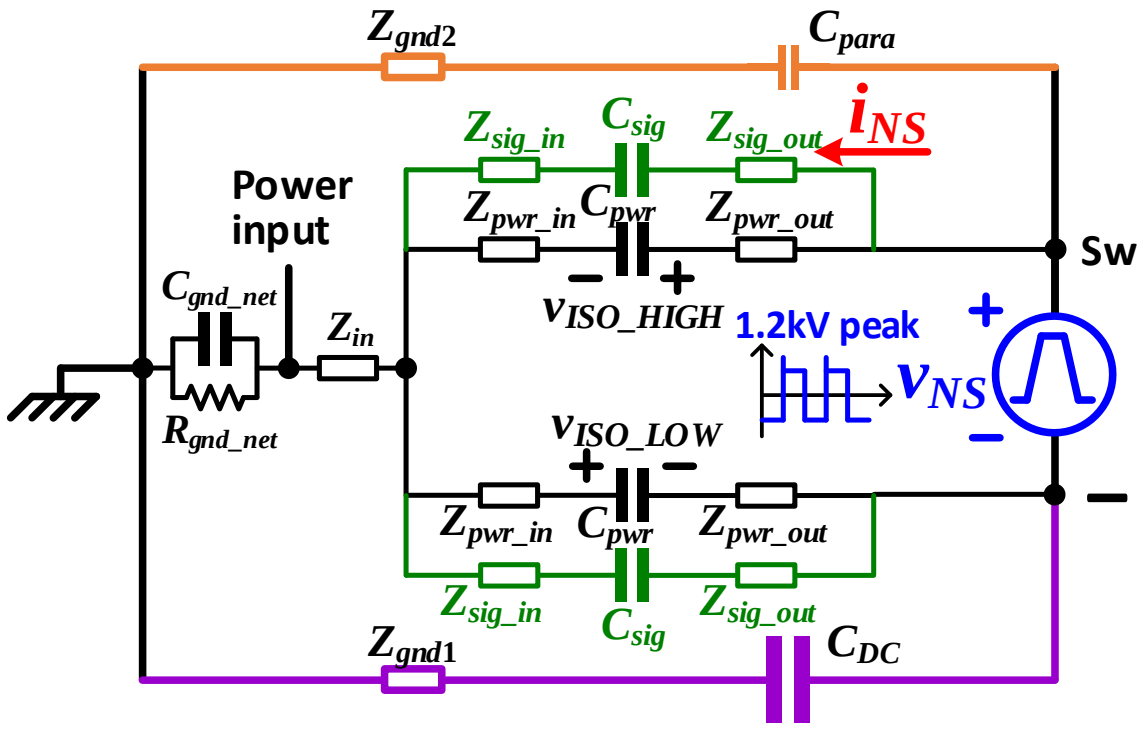


Figure 5-8 High-frequency AC CM equivalent model of the gate driver circuit

First of all, the high-side and low-side isolation stresses are compared using the ratio of the power supply isolation voltage v_{ISO_HIGH} (v_{ISO_LOW}) to the noise source v_{NS}. **Figure 5-9** shows that the high-side v_{ISO_HIGH}/v_{NS} almost equal to "1" (0 dB) below 30 MHz and reaches the peak at the series resonant frequency around 60 MHz (constructed by the loop of the noise source, high- and low-side isolation capacitor, and trace inductance). On the contrary, the low-side v_{ISO_LOW}/v_{NS} is nearly a trivial value of −60 dB below 4 MHz. In combination with the previous DC and low-frequency analysis, below 30 MHz the low-side isolation barrier takes only half of the DC voltage (500 V), and the high-side will take almost all the AC components of the switching-node noise source v_{NS}. Accordingly, the turn-off voltage spike should also be taken into consideration, and the low-side noise stress can be as high as 1200 V peak considering the 1.7 kV device limit. At frequency above 30 MHz, the series resonance effect kicks in and dramatically increases both the high- and low-side voltage stress. Therefore, the power supply isolation capacitor and trace inductance should be designed as small as possible to push the series resonance higher than the switch transient frequency to avoid series resonance.

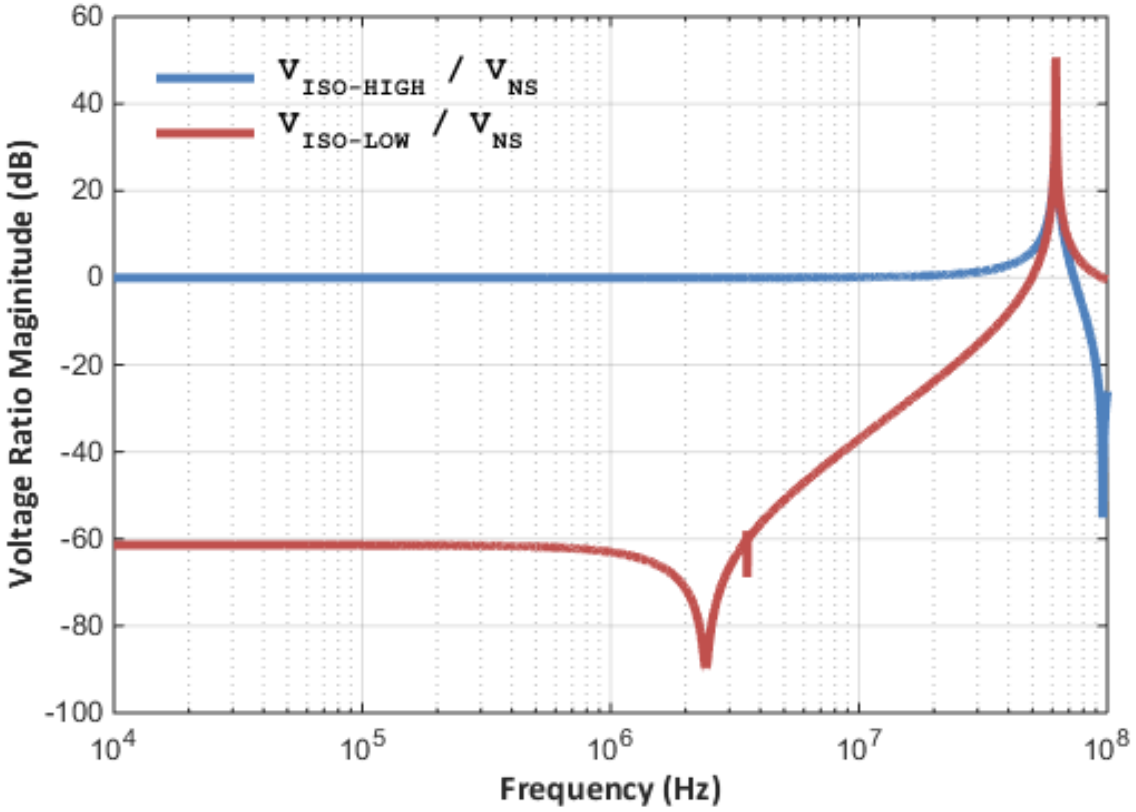


Figure 5-9 AC voltage distribution between the high-side and low-side isolations

Secondly, according to the analysis, the high-frequency noise voltage generates CM currents that flow through the high-side signal isolator and isolated power supply. The normal functioning of those components is guaranteed on their maximum dv/dt immunity in datasheets by proper component selection, however, CM noise current still results in voltage ringing and spikes on the ground/power trance impedances Z_{sig_in}, Z_{sig_out}, Z_{pwr_in}, Z_{pwr_out}, and Z_{in}. The negative effects on the Z_{pwr_in} and Z_{pwr_out} are generally not significant because the power supply input and output differential voltage is usually no less than 15 V, and sufficient amount of decoupling capacitors help suppress the spike voltage. On the contrary, the noise ringing and spikes on Z_{sig_in}, Z_{sig_out}, and Z_{in} will cause severe disturbances on the signal processing as most of the high-speed logic units use 3.3 V or 1.2 V power and their logic threshold is even lower. False triggering and protection are prone to occur by a 0.5 V voltage spike. Plus, those signals cannot be processed with large filters due to undesired signal propagation delays.

In order to mitigate the noise ringing on the primary side signal path, and to increase the voltage rating of the signal isolator, fiber-optic transceivers are widely used in medium-voltage applications. Fiber-optic cables can take hundreds of kilo-volts insulation stress while providing almost zero coupling capacitance. **Figure 5-10** shows the equivalent circuit of the power architecture when the fiber-optic transceivers are used. An open-circuit bar (half of a capacitor symbol) replaces the signal path capacitor C_{sig}, where the CM noise current cannot flow through. However, the secondary-side CM impedance Z_{sig_out} still exist as certain signal conditioning circuit still exist to process the fiber-optic transceiver signals. The secondary-side logic signals can still be subjected to CM noise currents.

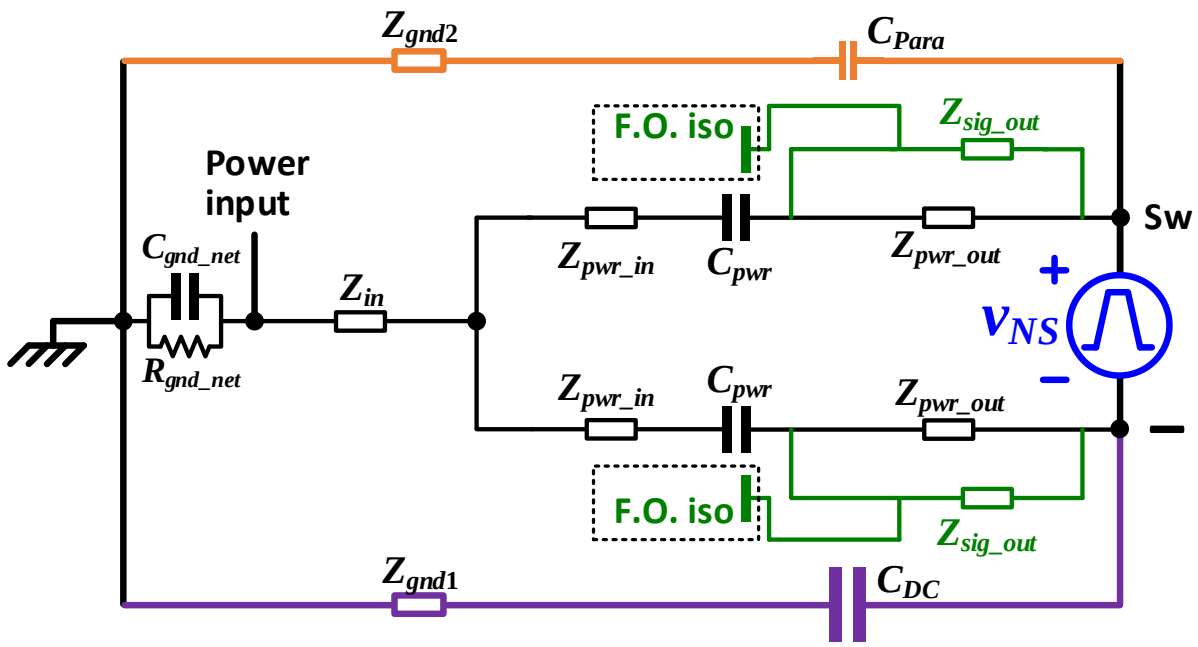


Figure 5-10 CM equivalent model of improved power architecture using fiber-optic transceivers

As mentioned before, the secondary-side signal path CM impedance Z_{sig_out} is determined by the power/ground traces for the signal path, which is provided by a 3.3 V logic power supply. The secondary-side power impedance Z_{pwr_out} is determined by the power/ground traces of a 24 V power supply. The two grounds are connected jointly at common points, the device source terminals. Basically, Z_{sig_out} and Z_{pwr_out} share the total secondary-side CM current. If the CM impedance Z_{sig_out} is intentionally designed much higher than Z_{pwr_out}, very few CM current will flow through Z_{sig_out} to generate noises. Generally speaking, there are two ways to increase the total impedance of the path along with Z_{sig_out}. One is to insert an additional signal isolator with parasitic capacitance C_{IC} as shown in **Figure 5-11**, and the other is to insert a CM choke L_{chk_out} as shown in **Figure 5-12**. The isolation capacitance is actually provided by a digital isolator or an isolated gate driver IC. The CM choke is practically inserted at the power lines of 3.3 V logic power supply instead of the logic signal line, to make sure the signal propagation will not be delayed. The architectures in **Figure 5-8**, **Figure 5-11** and **Figure 5-12** are compared in **Figure 5-13**, where the comparison variable is the admittance Y_{NS} as a function of frequency f, given by

$$Y_{NS}(f) = \frac{i_{NS}(f)}{v_{NS}(f)} \tag{5-5}$$

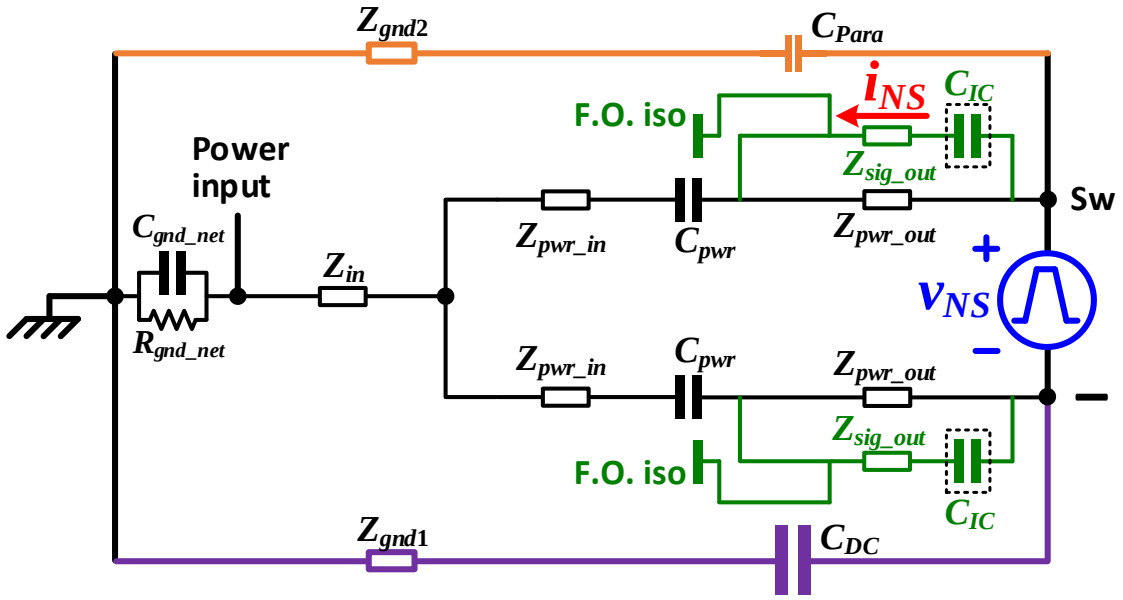


Figure 5-11 CM equivalent model of improved power architecture using fiber-optic transceivers and additional signal isolators

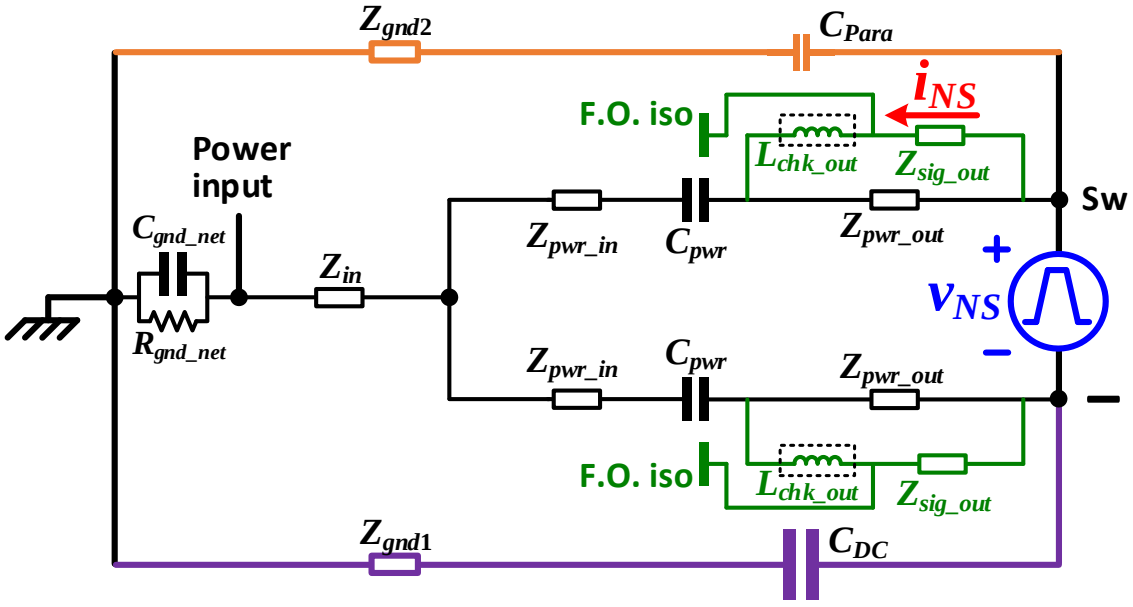


Figure 5-12 CM equivalent model of improved power architecture using fiber-optic transceivers and CM chokes

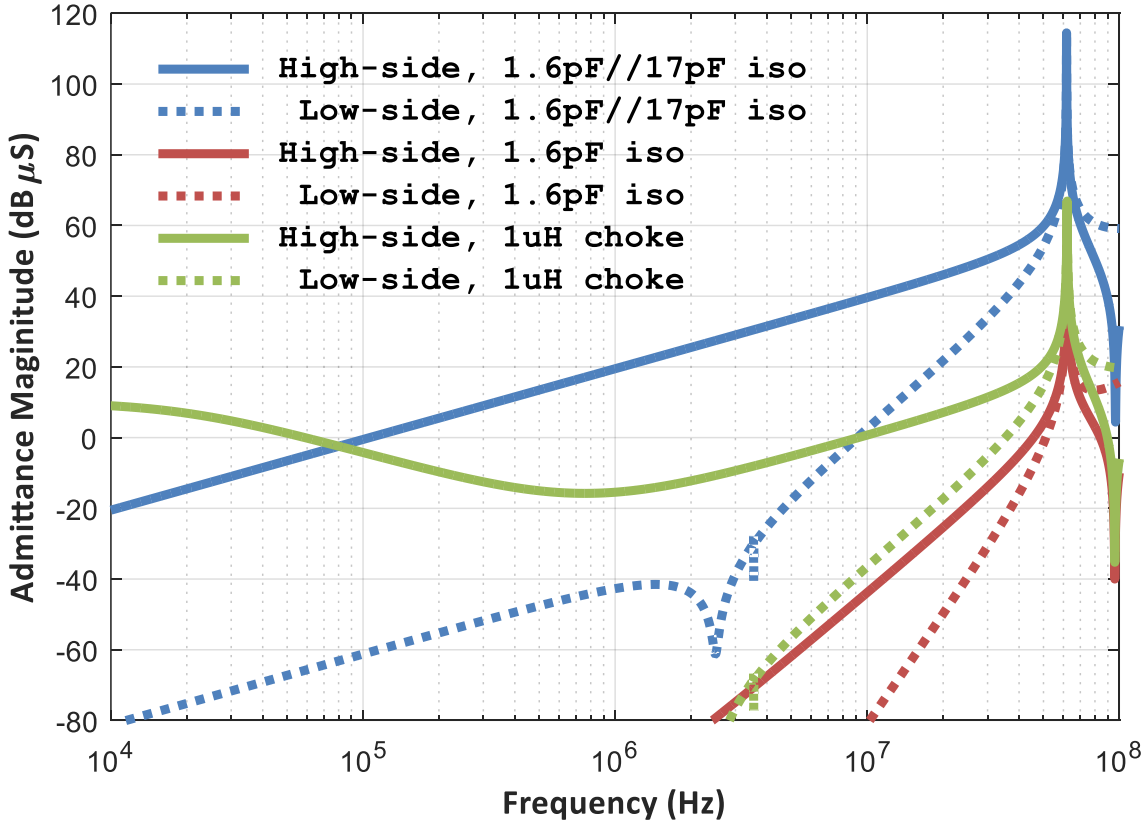


Figure 5-13 Comparison between noise-immunity solutions for signal path

where $i_{NS}(f)$ is the CM noise current flowing through the Z_{sig_out} of high-side and low-side channels (in the figures only the high-side i_{NS} is labeled). Therefore, in **Figure 5-13** there are totally 6 curves to represent the admittance $Y_{NS}(f)$ of 6 cases. Legend "1.6pF//17pF iso" corresponds to **Figure 5-8** where C_{IC} is 1.6 pF and C_{pwr} is 17 pF. Legend "1.6pF iso" corresponds to **Figure 5-11** where C_{IC} is 1.6 pF. Legend "1μH choke" corresponds to **Figure 5-12** where L_{chk_out} is 1 μH. From the results, all the high-side admittance (solid lines) is much higher than the low-side (dashed lines) ones below the resonant frequency at around 60 MHz, which is in accordance with the results in **Figure 5-9** where the high-frequency noise voltage concentrates on the high-side, generating higher CM noise currents that flow through the high-side trace impedances. The comparison result shows that the solution of "1.6 pF iso" give the best result where Y_{NS} is minimum at a wide frequency range.

One question will be raised that whether adding both the isolation capacitor and the CM choke can further reduce Y_{NS}. Therefore, another comparison is studied between the architectures in **Figure 5-11** and **Figure 5-14**. The results in **Figure 5-15** show that the two designs have almost no difference because the resonant frequency of L_{chk_out} and C_{IC} is 126 MHz beyond the design region 100 MHz. The capacitance C_{IC} still dominates the impedance of the Z_{sig_out} path. If L_{chk_out} is higher, the LC series resonant circuit will take effect so that the total Z_{sig_out} path impedance will dramatically drop and the admittance Y_{NS} will increase. In consequence, adding a CM choke L_{chk_out} in series with the additional signal isolator C_{IC} makes it even worse than adding only the signal isolator C_{IC}.

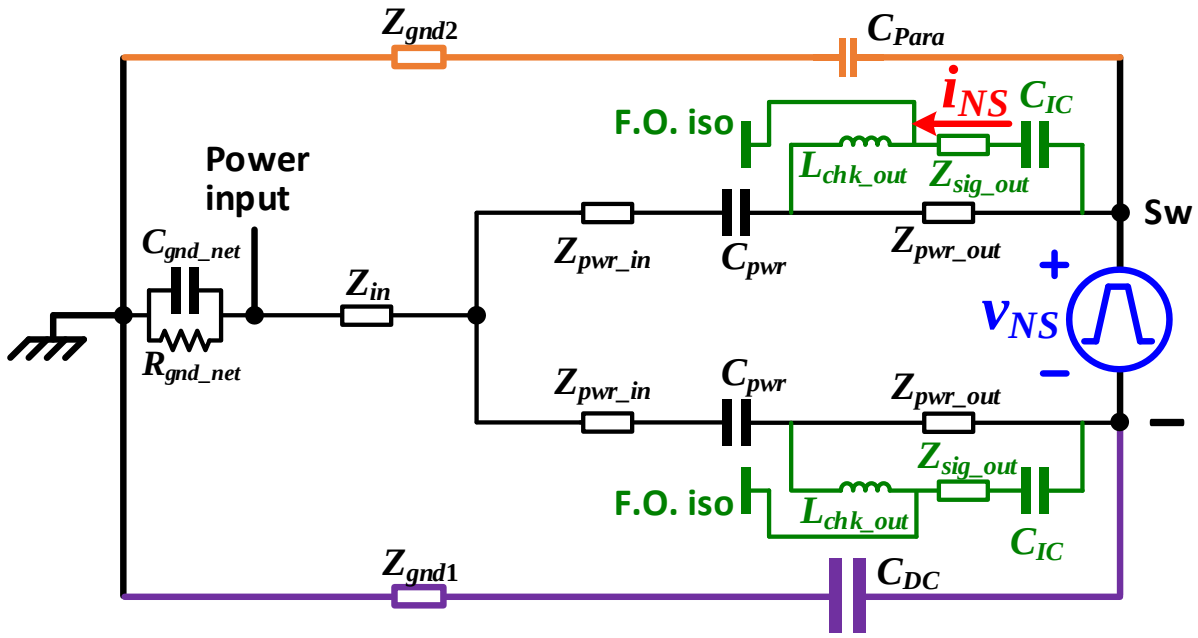


Figure 5-14 CM equivalent model of improved power architecture using fiber-optic transceivers, additional signal isolators and CM chokes

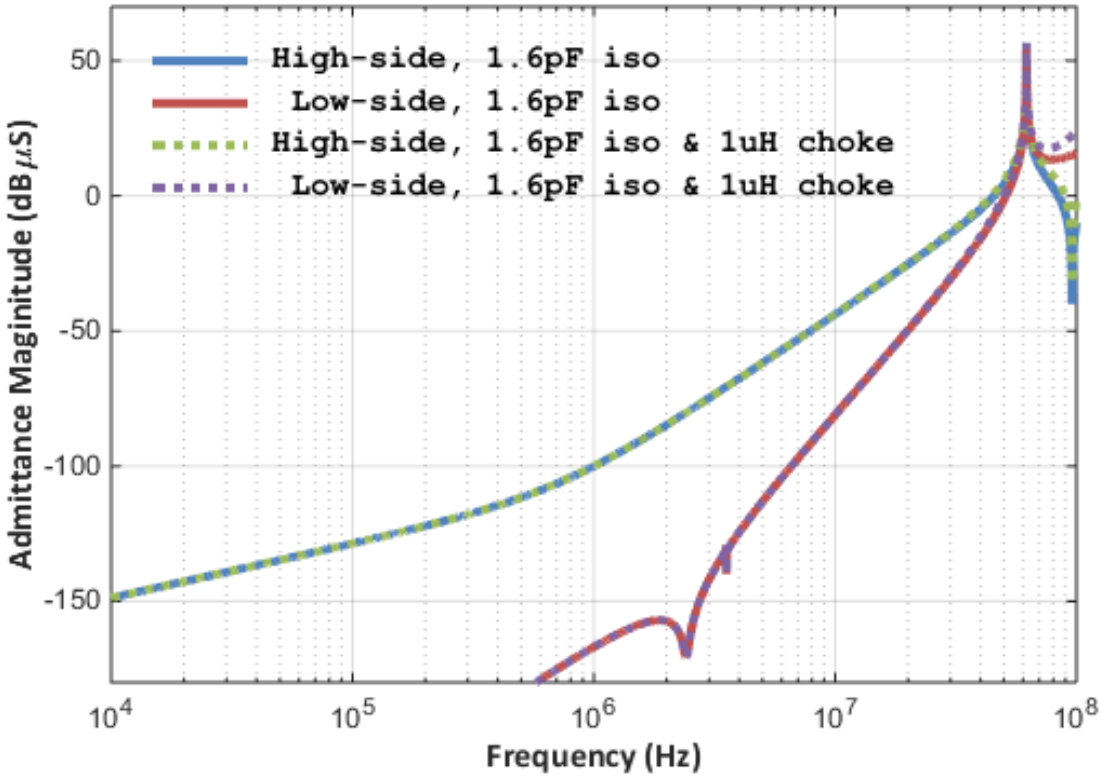


Figure 5-15 Comparison to decide if CM choke is needed for the signal path

On the basis of design in **Figure 5-11**, further study has been conducted to investigate the effect of CM chokes at the power input. Two designs at the power input have been made for comparison. The design in **Figure 5-16** adds two 1 μH chokes L_{chk_pwrin} at the two power channels, respectively. The other design in **Figure 5-17** is to add a single 1 μH chokes L_{chk_in} at the common power input. Concluded from the frequency-domain comparison in **Figure 5-18**, the admittance Y_{NS} is not reduced significantly, but two more resonant frequencies are created at around 20~30 MHz. This may result in more CM noise current. Accordingly, CM chokes for the power path are not recommended.

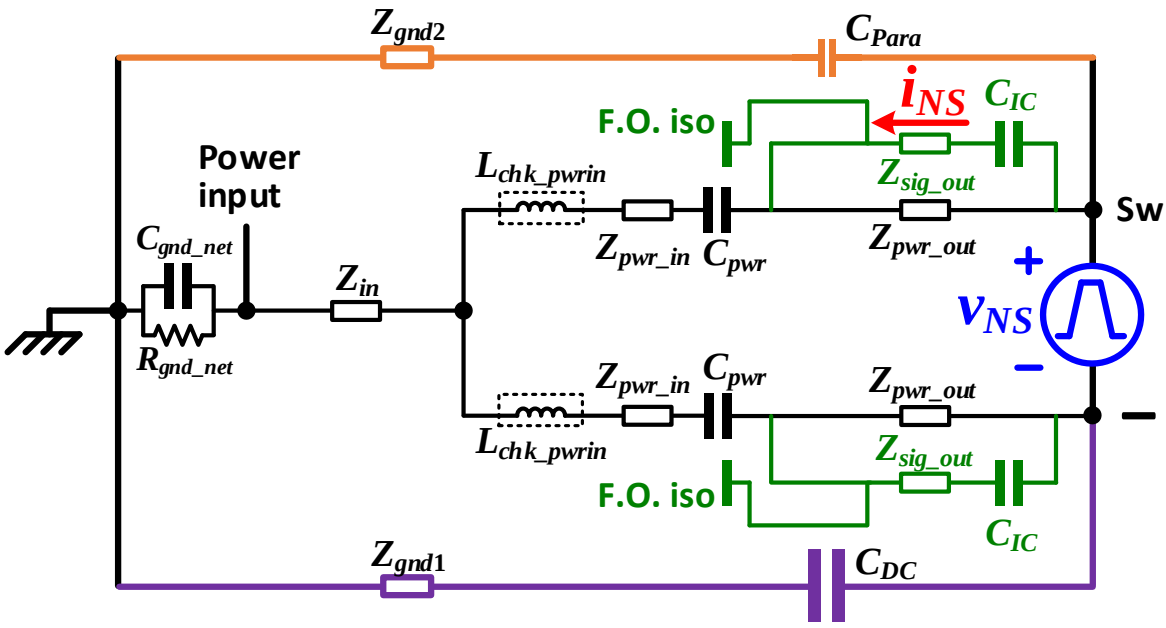


Figure 5-16 CM equivalent model of improved power architecture with separated CM chokes at two power channels

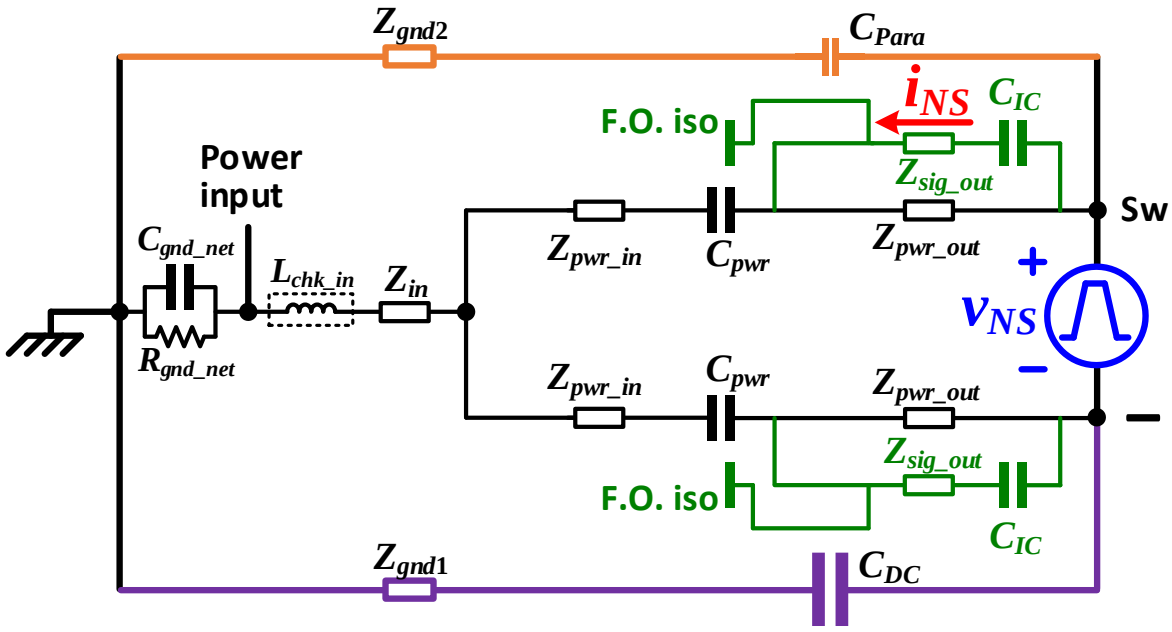


Figure 5-17 CM equivalent model of improved power architecture with single CM choke at the common power input

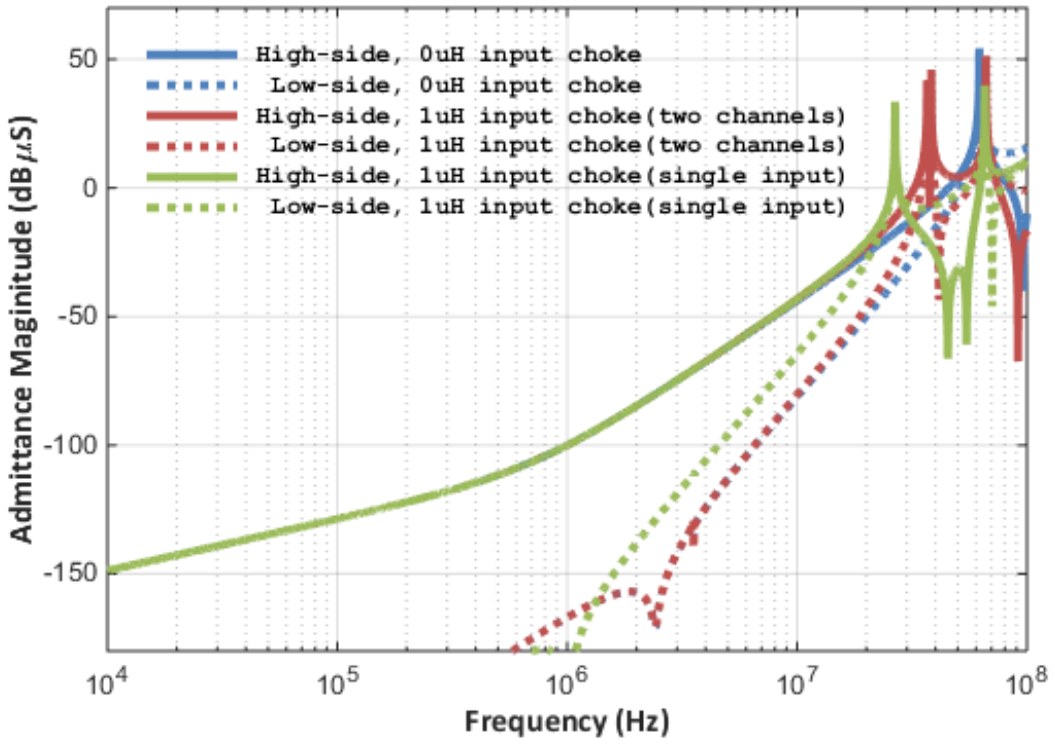


Figure 5-18 Comparison of CM choke designs at the power input

From the comprehensive study of the CM model of gate driver architecture, using fiber-optic isolation is able to improve CM noise immunity of sensitive circuitry with proper mismatched CM impedance design. The high capacitive impedance is preferred than the inductive impedance as the former one has better performance within low-frequency range. As long as a capacitive isolation is already applied, it is not recommended to add CM chokes in series with the isolation as it generates undesirable resonant peak hitting the noise source frequencies. Plus, the CM chokes only contribute to noise reduction at 10 times of the resonant frequency, which requires the CM choke to have very large value, trivial EPC, and the resonant frequency should be very carefully designed. Eventually, the gate driver power architecture is designed as shown in **Figure 5-19**, corresponding to the equivalent CM model in **Figure 5-11**. An isolated power supply Traco THM 10-4822WI with 17 pF input-output capacitance converts the auxiliary bus voltage 48 V to 24 V (+20V, −4V) to drive the MOSFET. The 24 V is converted to 3.3 V, 1.2 V, and ±5 V for logic and signal processing circuits by a second logic power supply, especially powering the primary input side of the gate driver IC with 1.6 pF input-output capacitance. As this capacitance dominates the CM noise propagation path, the isolation capacitance of the logic power supply is not critical. A non-isolated power supply also works with a well-planned PCB layout. In this design, the CM voltage stresses on both the logic power supply and the driver IC are negligible, and no CM chokes are necessary.

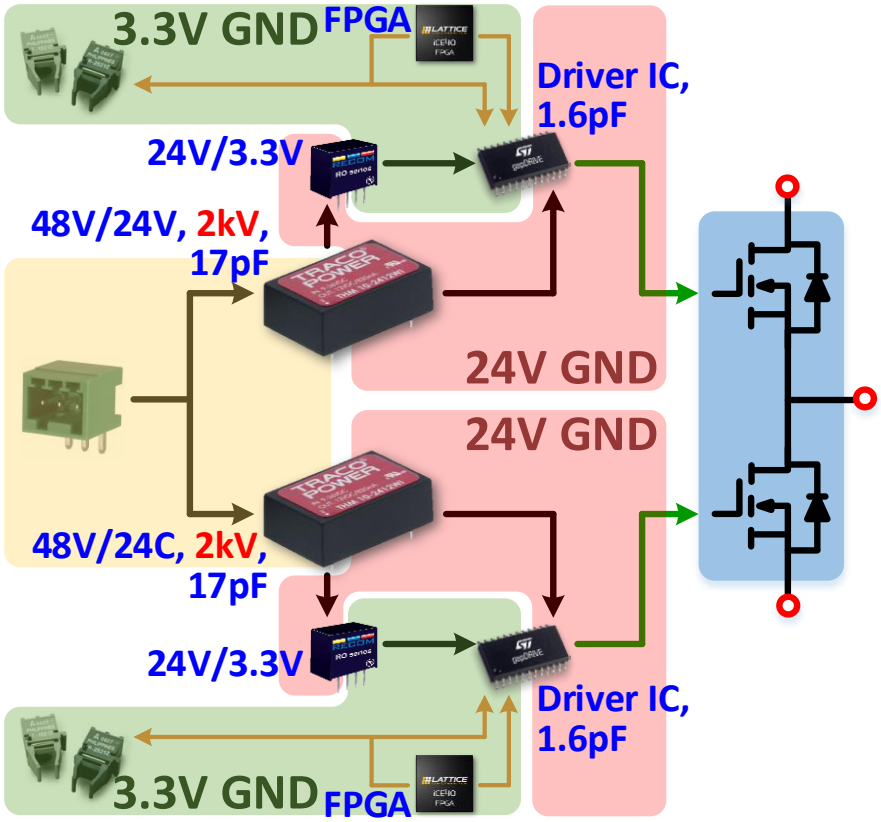


Figure 5-19 Designed power architecture for the gate driver

5.3.2 Driver IC Selection

Based on the critical specifications, eight gate driver IC candidates from various manufacturers have been screened for comparison. In **Table 5-2**, the values are collected from public manufacturer datasheets. In the column of "Propagation", "(d)" means "delays" and the first number indicates the turn-on delay while the second indicates the turn-off delay. "(r/f)" means rise/fall time corresponding to the two numbers in the row, respectively. In the column of "UVLO", the "+ number" indicates the positive threshold voltage where the under-voltage lockout will be triggered if the positive supply voltage drops. Similarly, the "− number" represents the negative threshold value. In the column of "DeSat", the first value means the maximum configurable threshold voltage of desaturation, and the second indicates the response time. In the column of "STO", the aforementioned two types of soft turn-off mechanisms are labeled if provided. In the column of "AMC", the threshold value of the gate voltage to enable the low-impedance active Miller-clamp are presented. "N/A" means the functionality is not offered by the IC. After a compressive comparison, the driver STGAP1AS demonstrates the best performance in the first four characteristics. The only shortcoming is that its AMC threshold voltage is almost the same as the device gate threshold, so an improved AMC circuit has been proposed for this concern. In the following sections, the circuit design based on STGAP1AS is presented.

Table 5-2 COMPARISON OF GATE DRIVER IC CANDIDATES

Manufacturer	Part number	Critical Functionalities				
		Propagation	UVLO	DeSat	STO	AMC
Avago	ACPL-332J	(d) 180 ns, 180 ns (r/f) 50 ns, 50 ns	+ 10.3 V	(th) 6.5 V, (r) 300 ns	LRTO	V_{EE} + 2.0 V
Avago	HCPL-316J	(d) 300 ns, 320 ns (r/f) 100 ns, 100 ns	+ 11.1 V	(th) 7.0 V, (r) 300 ns	LRTO	N/A
Fairchild	FOD8318	(d) 300 ns, 250 ns (r/f) 34 ns, 34 ns	+ 10.0 V	(th) 7.0 V, (r) 850 ns	LRTO	V_{EE} + 2.2 V
Toshiba	TLP5214	(d) 85 ns, 90 ns (r/f) 32 ns, 18 ns	+ 10.3 V	(th) 6.5 V, (r) 180 ns	LRTO	V_{EE} + 3.0 V
Infineon	1ED020I12	(d) 170 ns, 165 ns (r/f) 30 ns, 50 ns	+ 11.0 V	(th) 9.0 V, (r) 350 ns	2LTO	V_{EE} + 2.1 V
On Semi	MC33153	(d) 80 ns, 120 ns (r/f) 17 ns, 17 ns	+ 11.0 V	(th) 6.5 V, (r) 300 ns	N/A	N/A
ROHM	BM6102FV-C	(d) 150 ns, 150 ns (r/f) 50 ns, 50 ns	+ 11.5 V	(th) 10 V, (r) 3250 ns	2LTO	V_{EE} + 2 V
STMicro	STGAP1AS	(d) 100 ns, 100 ns (r/f) 25 ns, 25 ns	+ 13.0 V − 2.0 V	(th) 10 V, (r) 100 ns	2LTO	GND + 2 V

5.3.3 Current Booster Design

The internal gate resistance of the SiC MOSFET module is 3.3 Ω per switching position of the half bridge. If it is driven by a 24 V power supply, the maximum driving current is 7.3 A. The MOSFET-based output buffer stage of STGAP1AS has 1 Ω internal conduction resistance, and then the driving current is limited to 5.6 A. However, the driver IC has maximum pulse current limit of 5 A at 25°C ambient temperature. So, more than 1 Ω external gate resistor is needed, but the SiC MOSFET switching speed will be limited. To this end, external current boosters are necessary to boost switching speed and thus reduce switching losses.

Typically, the current booster is a pair of push-pull MOSFETs or bipolar transistors. As the conduction of a MOSFET is equivalent to a resistor, there is always voltage drop on the on-resistance of the MOSFET-based boosters. If the on-resistance is 0.5 Ω, the voltage drop across it can be as high as 3.15 V assuming a total gate resistance of 3.8 (3.3+0.5) Ω and driving current of 6.3 A. In this case, the on-resistance will slow down the driving speed and take about 15% of the total driving loss. Then extra heatsinks for the MOSFETs that take more space on the driver boards become necessary for the current boosters. Nonetheless, the losses on the BJT-based current booster are trivial because the bipolar transistors have lower voltage drops of around 0.1~0.7 V from part to part.

The current booster should also be able to work together with the STO functionality. For the type of LRTO, the input capacitance of the current booster need to be increased. However, the normal switching process will also be delayed by hundreds of nanoseconds,

which is undesirable for high-frequency applications. For the type of 2LTO, the current booster should be able to transfer the intermediate voltage level following the driver IC output, which can be only achieved by BJT-based current boosters. In addition, BJT-based current boosters can be easily paralleled via gate resistors for excellent current sharing. Finally, BJT-based current boosters are selected. Available commercial BJT-based current boosters can drive up to 10 A peak current. To design for enough margin, three the current booster are paralleled as shown in **Figure 5-20**. This design has a natural closed-loop to balance the output currents of three boosters. When one of the boosters delivers higher current, the voltage drop on R_{G_EXT} increases so that the voltage drop across the base resistor R_b decreases and the base current decreases. Because of the transfer characteristics of the BJTs, the transistor emitter current is reduced. **Figure 5-21** shows the well-balanced driving current of the three paralleled current boosters at switching transient. The yellow waveform is the gate to source voltage as labeled, and the blue, magenta and green waveforms are the three voltage across R_{G_EXT} that represent the driving current of three channels.

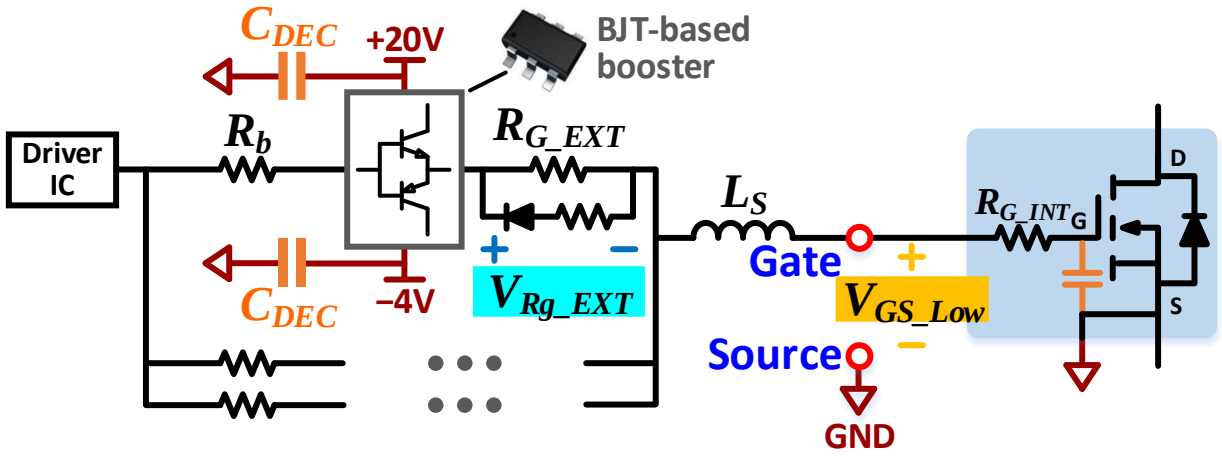


Figure 5-20 Schematics of the self-balanced paralleled current boosters

Figure 5-21 Current sharing of three paralleled current boosters

In terms of the PCB layout, for each one of the three driving channels, the gate resistor, and the decoupling capacitors are designed back-to-back at the top and bottom PCB layers. Hence, the current boosters, gate resistors, and decoupling capacitors enclose a very small loop of a quite small parasitic inductance. A cross-section view of the PCB layout is shown in **Figure 5-22**. The paralleled current boosters lead to a further reduced driving loop inductance by paralleling the three driving channels on a wider driving-current distribution area. The actual gate loop impedance of the populated PCB has been measured with impedance analyzer Agilent 4294A. The measurement cables have been calibrated and the driving-loop impedance is characterized by shorting the current boosters with zero-ohm resistance. **Figure 5-23** shows the measurement results of the turn-on loop and turn-off loop, respectively. Both of them demonstrate an LCR series resonant performance. The decoupling capacitor impedance is shown at frequencies lower than 100 kHz, matching the soldered value of 60 μF. At resonant frequency around 70 kHz, the resistance impedances are read as 0.03 Ω and 0.015 Ω, which correspond the populated total resistance of 3 paralleled 0.1 Ω for the turn-on loop, and 6 paralleled 0.1 Ω for the turn-off loop. The loop inductance impedance is represented at frequencies above 10 MHz, giving 1.20 nH for the turn-on loop and 1.07 nH for the turn-off loop, respectively.

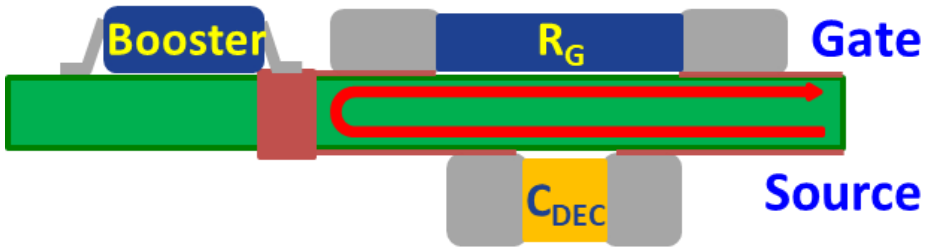


Figure 5-22 Schematics of the self-balanced paralleled current boosters

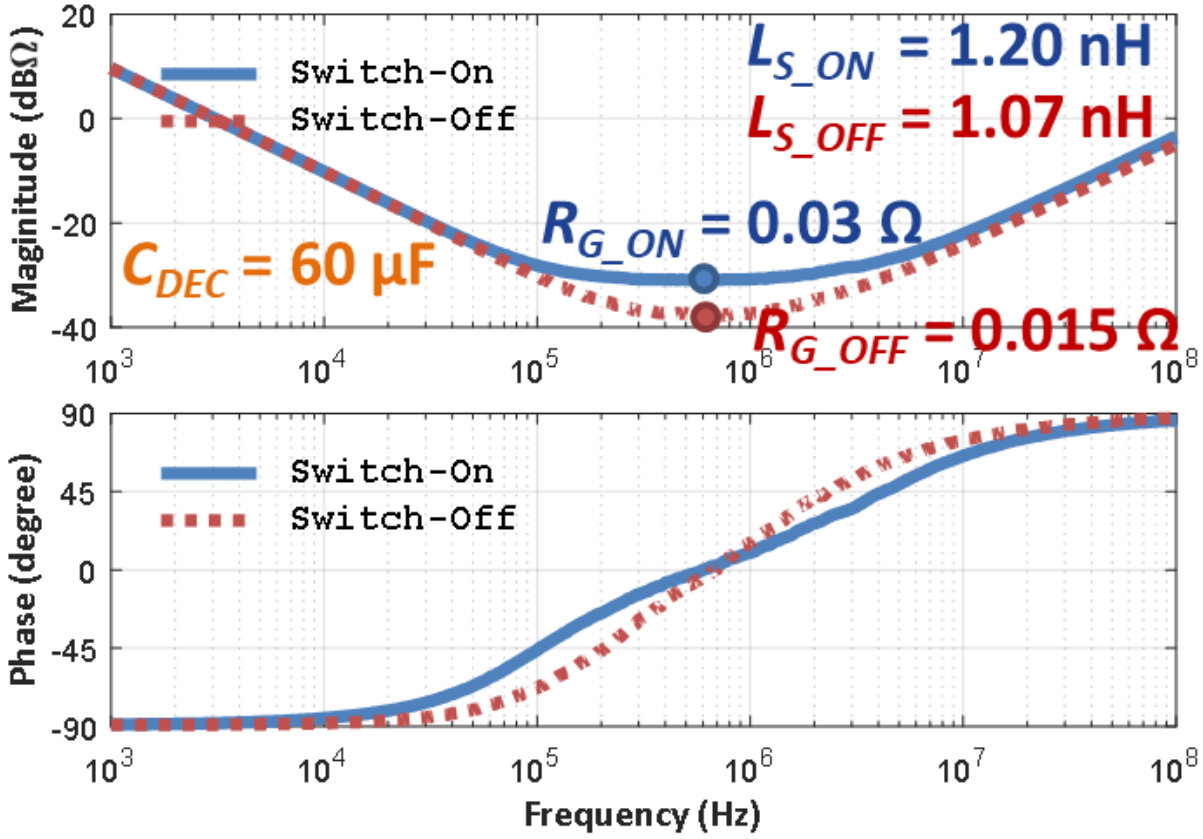


Figure 5-23 Current sharing of three paralleled current boosters

5.3.4 Soft Turn-Off

The gate voltage controls the drain current of the SiC MOSFET according to its transfer characteristics. The intermediate gate voltage in 2LTO should be designed to a value that ensures the drain current is within the normal operating range. In this manner, the turn-off voltage overshoot will not exceed device rating at the second turn-off transient at normal turn-off speed. The duration of this intermediate gate voltage should be long enough for the drain current to drop to the normal-operation current value. The datasheet only gives the transfer characteristics at one drain-source voltage, however, in practical application, the drain-source voltage varies with the drain current at the turn-off process. This makes it very difficult to pre-calculate the proper design value, and thus the better way to determine the intermediate gate voltage is by trial and error. **Figure 5-24** shows an overcurrent protection using the STO at the time scale of 500 ns/div. The protection is activated at 400 A. The intermediate gate voltage is finally designed as 7 V and the time span for the current to drop is about 500 ns.

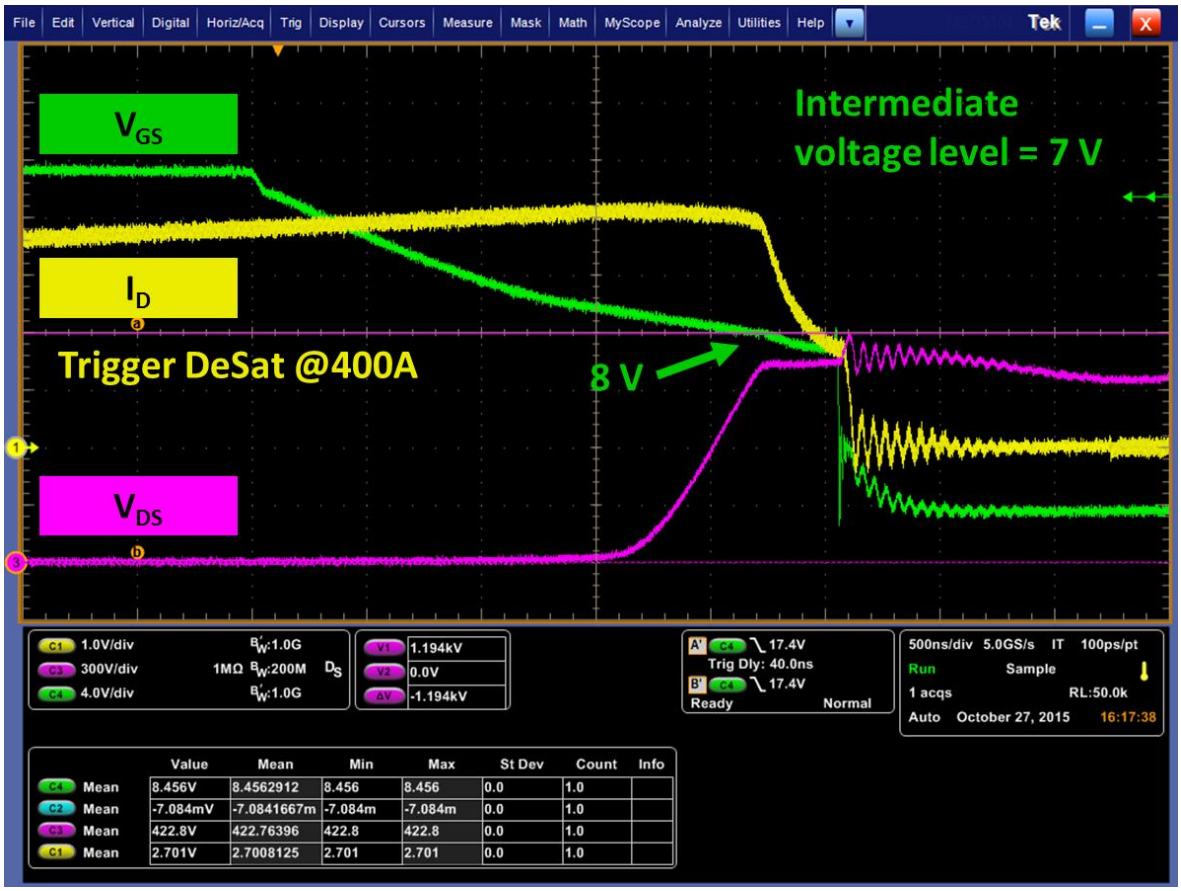


Figure 5-24 Test waveform of Soft Turn-Off

5.3.5 Active Miller Clamp Design

The AMC schematics are shown in **Figure 5-25**. In order to minimize the total impedance of the Miller-clamp loop and to boost the sink current capability, a PNP transistor T_{MC} is added and placed adjacent to the gate pins in actual layout. A concern that the AMC threshold the driver is almost the same as the device gate threshold voltage of 2 V can result in early activation of AMC before the SiC MOSFET is fully turned off. To address that issue, a capacitor C_{MC} is added to form a delay circuit together with the sensing resistor R_{MC}. The detection of gate voltage will be delayed to make sure that the actual gate voltage has dropped low enough to completely cut off the SiC MOSFET channel earlier than the AMC is triggered.

The experimental results of the low-side gate waveforms when the high-side MOSFET is turned on with the AMC activated are shown in **Figure 5-26**. The maximum dv/dt rate is −20 V/ns. The peak value on low-side gate voltage V_{GS_LOW} is −0.92 V, not reaching the turn-on threshold voltage of 2 V. **Figure 5-27** shows the high-side switch turned-off waveform when the maximum dv/dt rate is 14 V/ns. The valley value on the low-side gate is −6.7 V, without reaching the negative gate voltage limit of −10V.

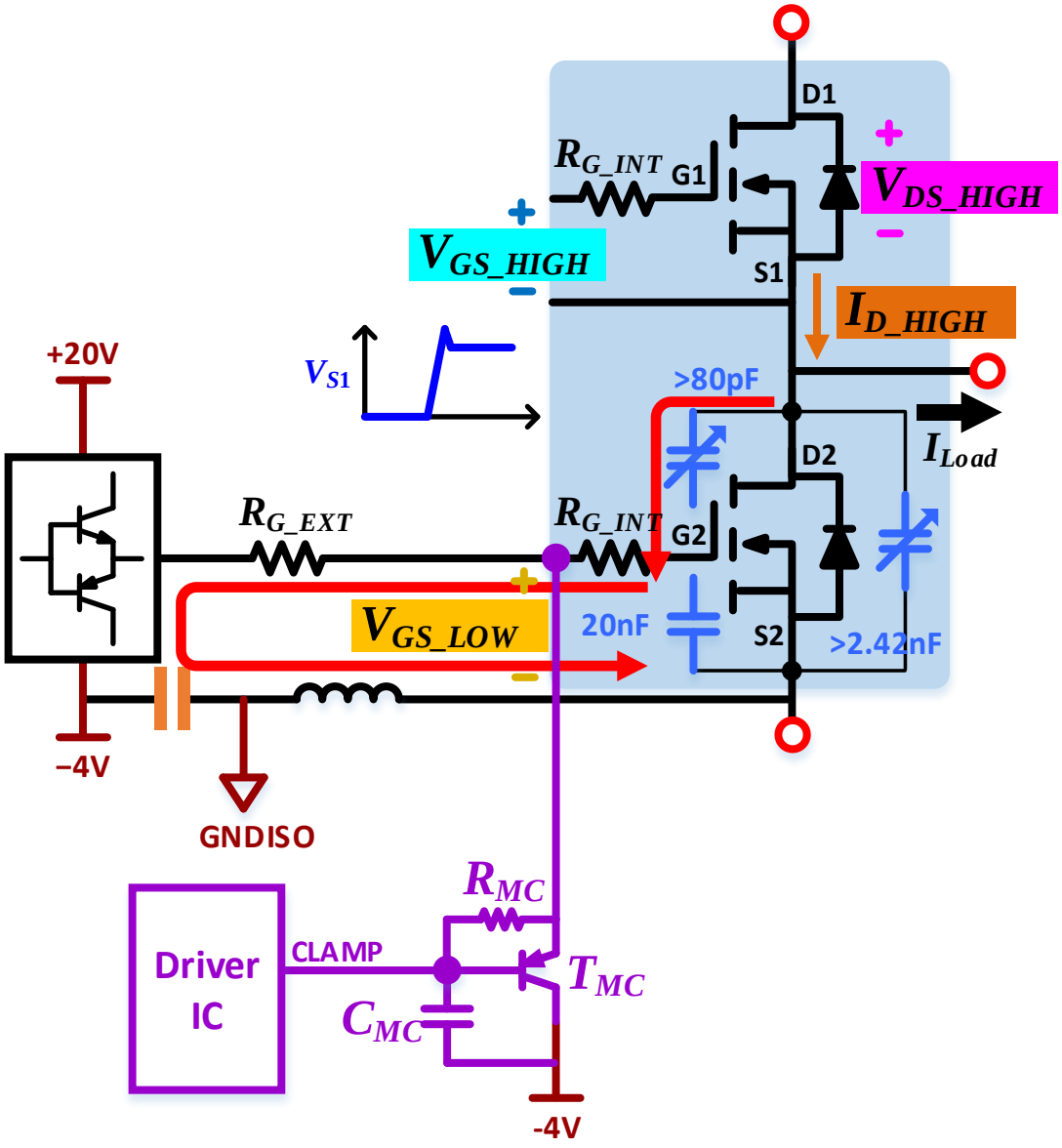


Figure 5-25 Schematics of the Active Miller Clamp

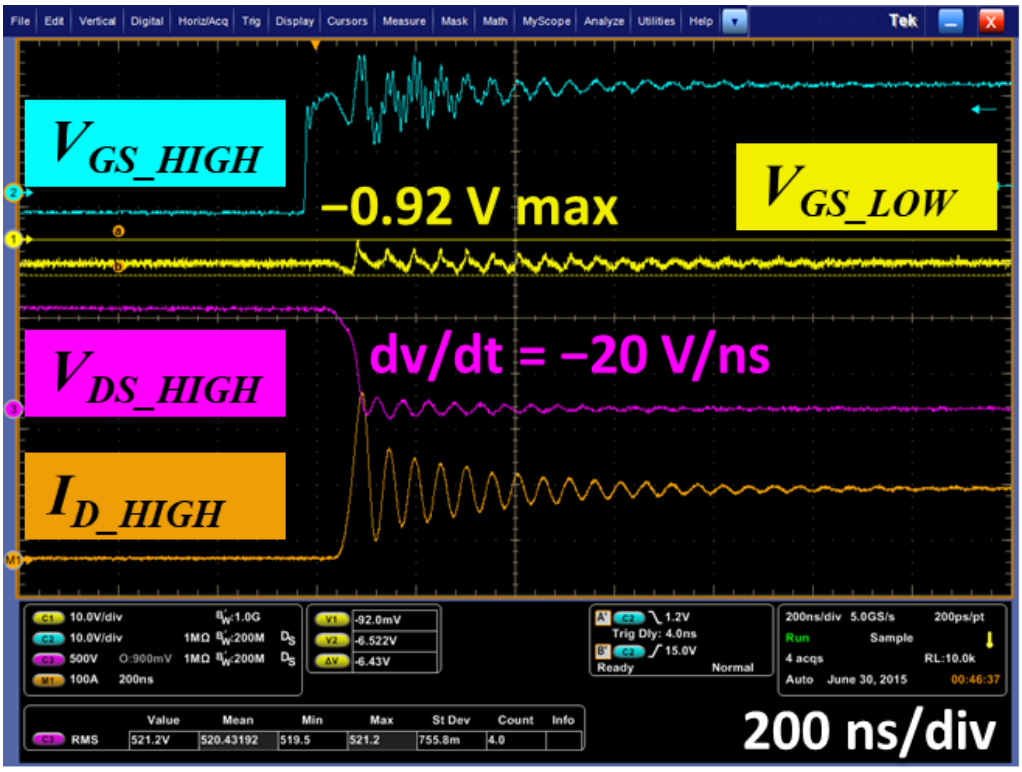


Figure 5-26 Test waveform of the cross-talk issue at turn-on

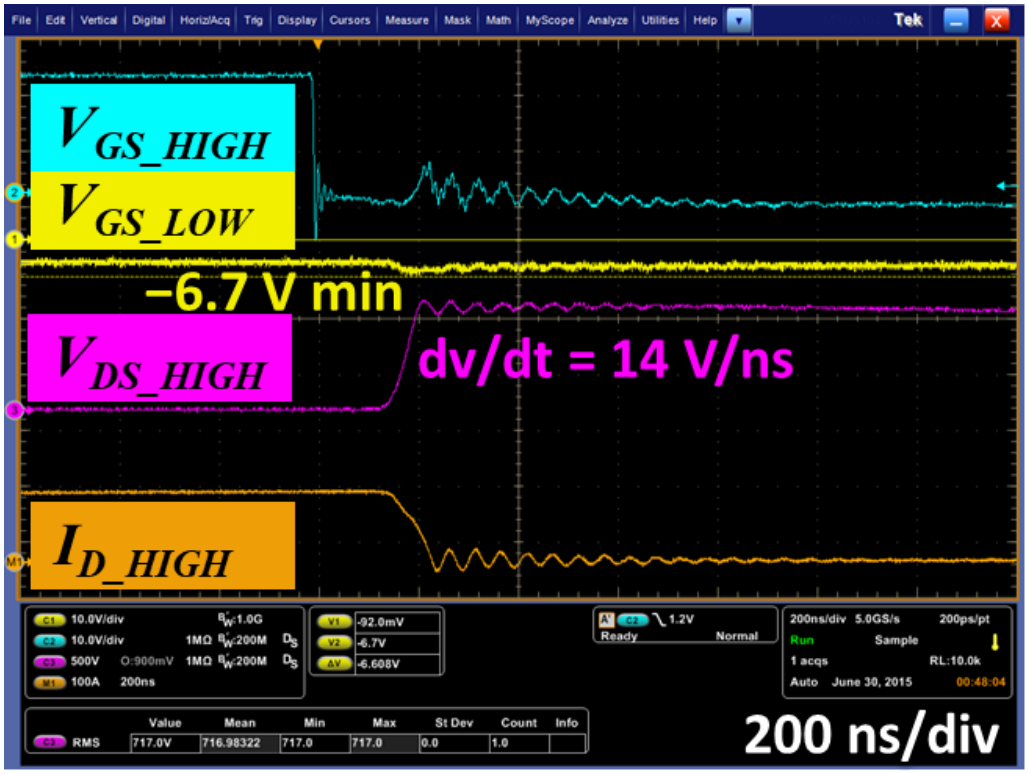


Figure 5-27 Test waveform of the cross-talk issue at turn-off

5.3.6 Switch-Voltage Sensor Design

The semiconductor switch voltage is a critical sensing information that can be used for DC-bus voltage sensing, zero-voltage switching (ZVS) detection, dead-time compensation, overvoltage alert and voltage balancing for directly stacked devices. The BW for those sensing purposes usually varies depending on the amount of switching ringing that has to be filtered. For instance, the overvoltage alert usually senses the very peak of the turn-off ringing, so it requires a BW that is high enough to cover the ringing frequency. On the contrary, the switching ringing is not desirable for device voltage balancing as the spikes will give wrong sensing results of the off-stage drain-source voltages. To meet those different needs, therefore, a sensor that has a constant gain up to the ringing frequency is first needed, based on which filters can be places for different applications.

The conventional resistor voltage divider (RVD) is not appropriate in this design work. As shown in the top schematics in **Figure 5-28**, the RVD comprises high-voltage high-resistance R_1 (usually by multiple resistors in series) and low-voltage low-resistance R_2. The output V_{RVD} usually feeds a voltage follower. The trace parasitic to ground capacitance and OpAmp input capacitance C_{in} can hardly reach less than 10 pF, which equivalently forms a low-pass filter with R_2. The cutoff frequency (BW) of this filter is $f_{RVD} = 1/(2\pi \cdot R_2 \cdot C_{in})$. If it is necessary to measure 16 MHz voltage ringing, f_{RVD} need to be no less than 80 MHz (5x), then R_2 should be no higher than 195 Ω. For a reasonable sensor gain, R_1 is around 60 kΩ, with power consumption of 17 W under 1 kV DC bus voltage. To this end, RVD is extensively bulky and lossy for this type of sensor applications.

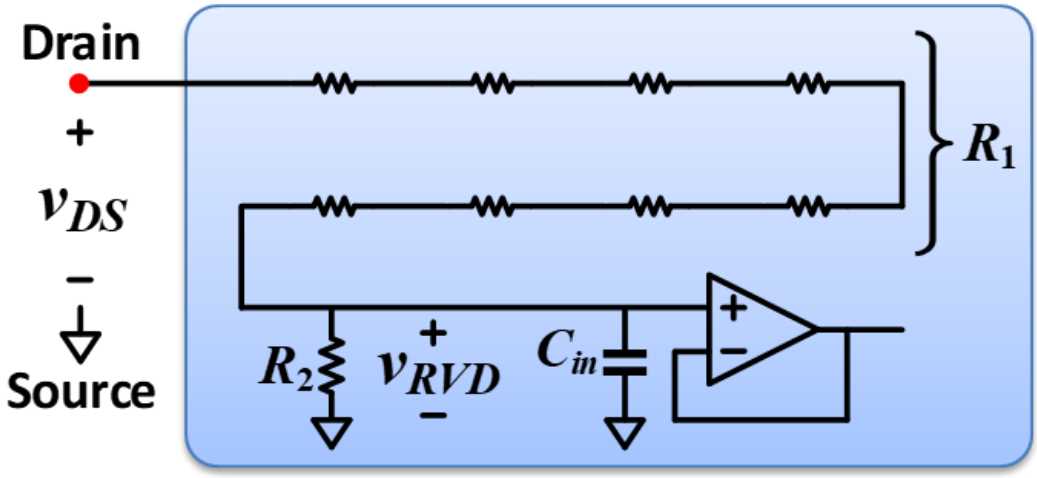


Figure 5-28 Resistor voltage divider (RVD) schematics

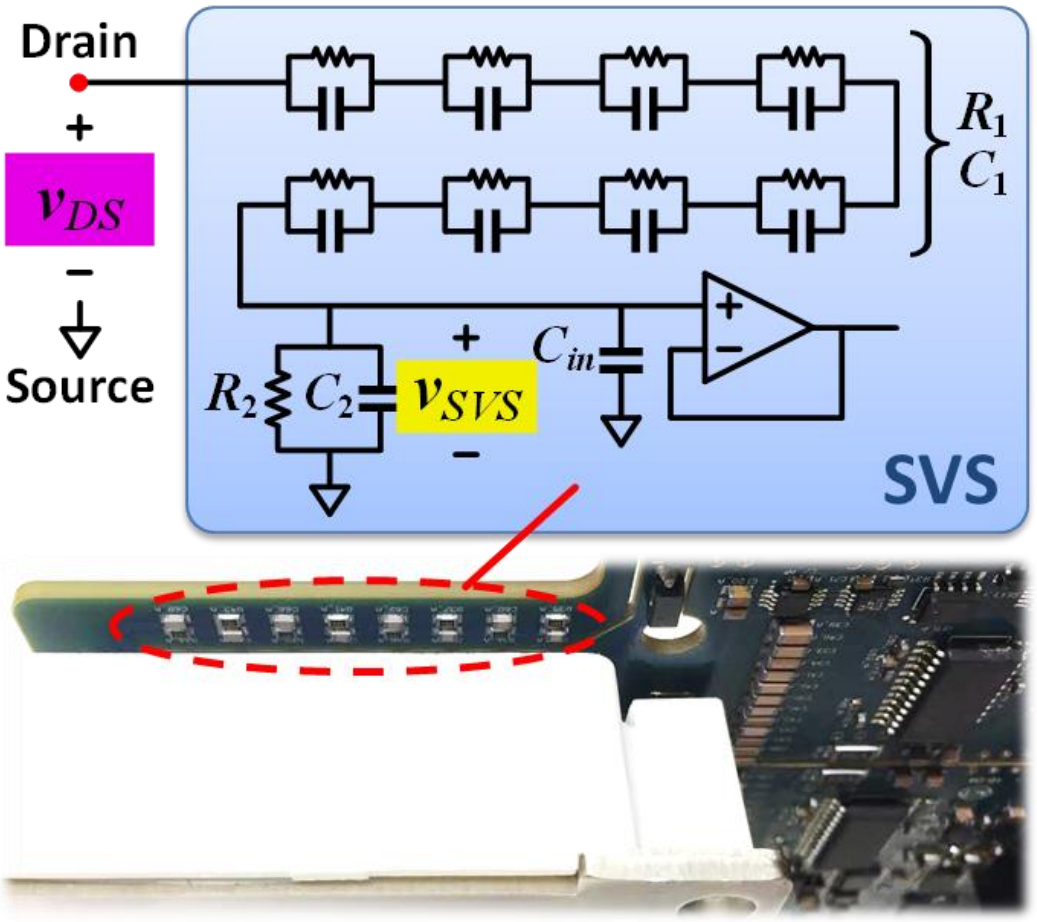


Figure 5-29 Switch voltage sensor (SVS) schematics

An SVS has been integrated to address the issue. **Figure 5-29** shows a capacitors divider paralleled with the conventional RVD, and they share the same transfer gain G_{SVS} as in (5-6). As C_2>>C_{in}, the impact from parasitic capacitance becomes negligible. The finalized parameters are given in **Table 5-3**, which shows that the loss on SVS is less than 1 W.

(5-6)
$$G_{SVS} = \frac{v_{SVS}}{v_{DS}} = \frac{R_2}{R_1 + R_2} = \frac{1/\ j\omega C_2}{1/\ j\omega C_1 + 1/\ j\omega C_2} = \frac{C_1}{C_1 + C_2}$$

Table 5-3 SVS Parameters

Parameter	Value	Parameter	Value
G_{SVS}	3.24 mΩ (1500V~4.86V)	*SVS loss*	0.83 W
R_1	1.2 MΩ (8 in series)	C_1	1.625 pF (8 in series)
R_2	3.9 kΩ	C_2	0.5 nF

Figure 5-30 shows the experimental waveforms acquired in a 1 kV quasi-square-wave test, where the v_{SVS} and v_{DS} demonstrate excellent agreement. The ZVS behavior can be simply detected as v_{DS} has already dropped to zero before v_{GS} becomes high. **Figure 5-31** shows the waveforms of a 1 kV DPT test, $v_{SVS,}$ and v_{DS} have the same envelope of ringing and the peak values are captured correctly.

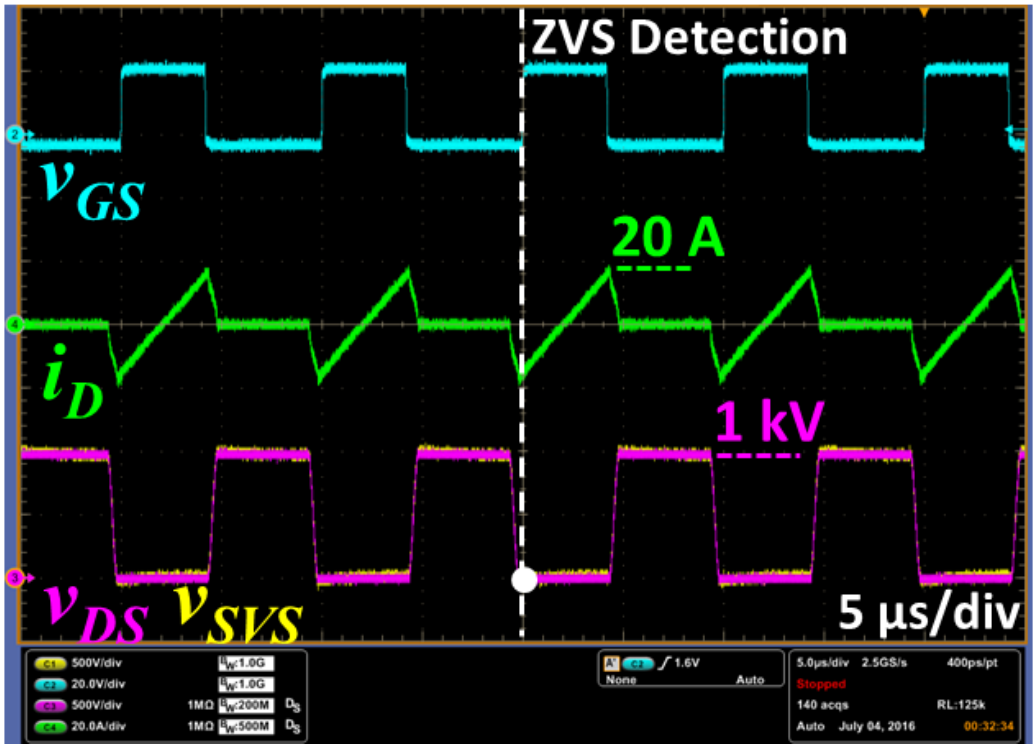


Figure 5-30 SVS performance in QSW test

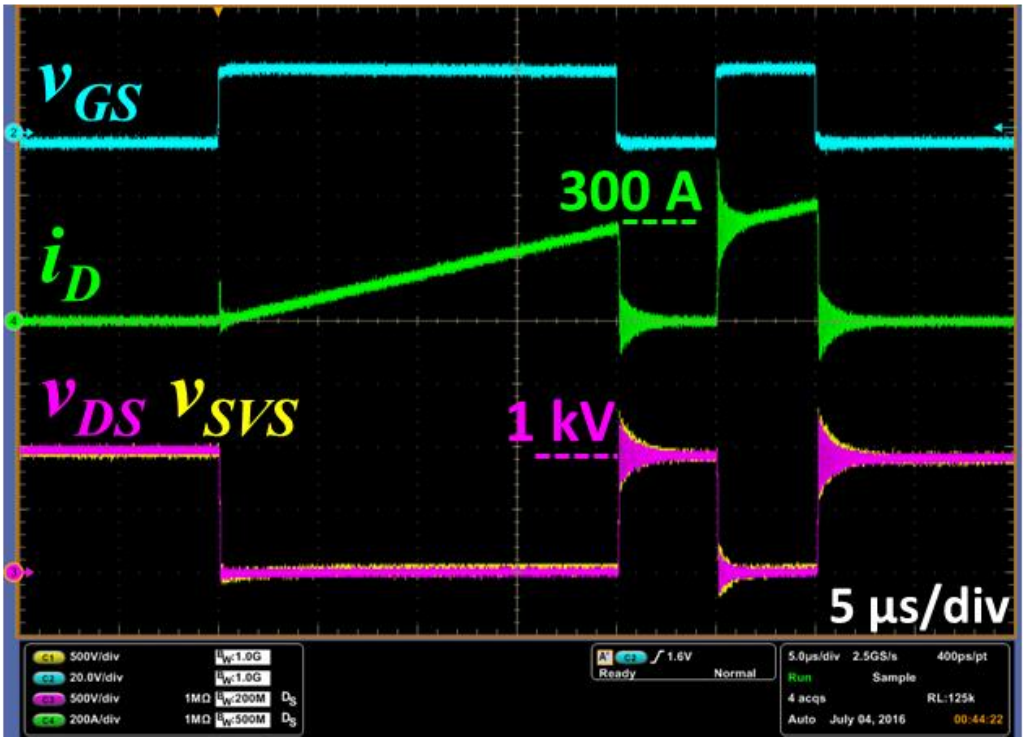


Figure 5-31 SVS performance in DPT test

The transfer gain of the designed SVS is shown in **Figure 5-32**, which is a constant value from DC to 100 MHz. However, with the same resistance and parasitic capacitance (10 pF), the cutoff frequency of RVD can only reach 4 MHz (−3 dB), and the valid frequency of designed gain is around 800 kHz.

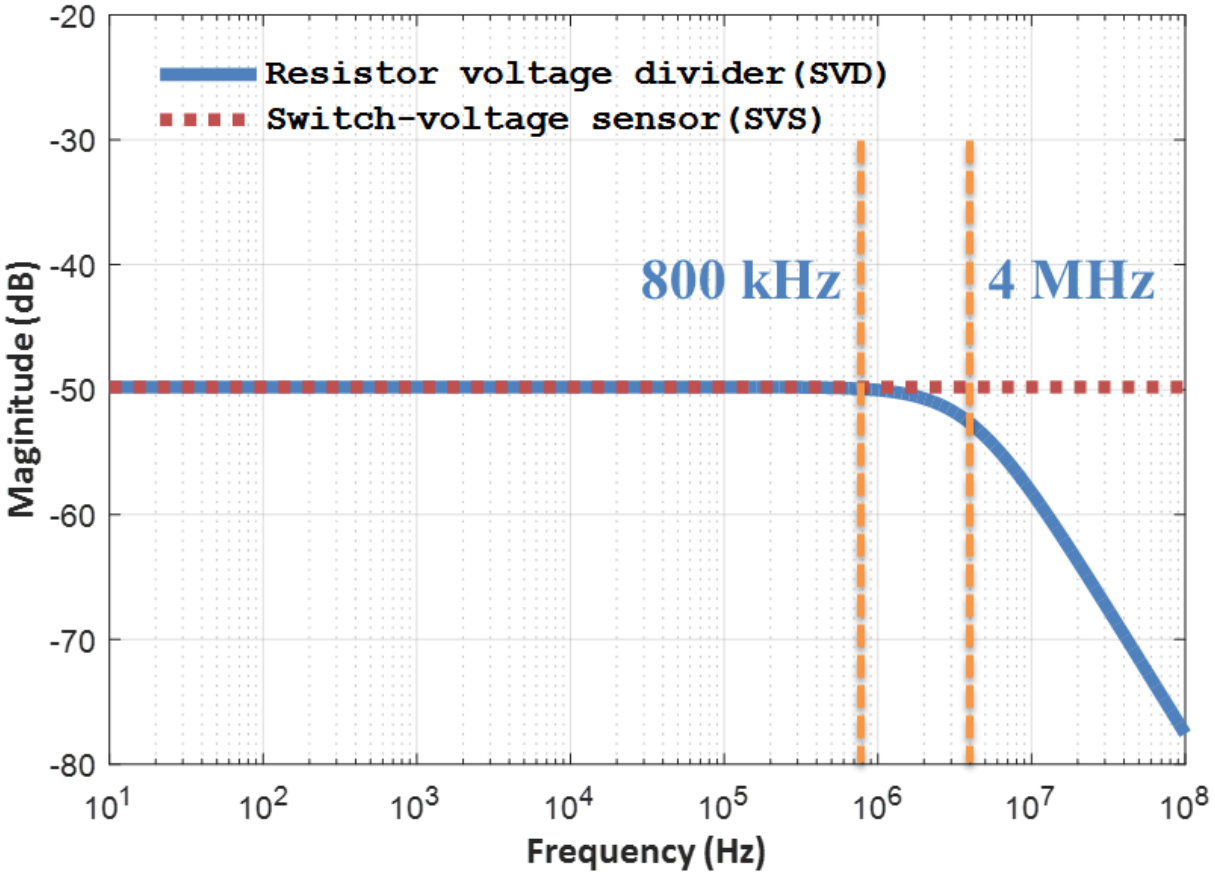


Figure 5-32 RVD and SVS transfer gain

5.4 PEBB System Integration

The work of this section is primarily contributed by other team members of an ONR PEBB1000 project. Hence, only considerations, objective and results are presented in this section. The design details can be found in the project report and corresponding references published by the team members. In the end, the test result of the integrated PEBB unit is shown.

5.4.1 Auxiliary power supply

Figure 5-33 shows an architecture for the auxiliary power solution that takes energy from a grid-fed low-voltage external source and isolation is mandatory. The primary-side is fed from the utility sources, and the secondary-side supplies a 48 V auxiliary DC bus, where the gate drivers, PEBB controller, and sensors are powered from. It has been mentioned that the PEBB is the LRU for stacking and paralleling connections to meet higher voltage and current demands. Accordingly, as shown in the right-hand side picture of **Figure 5-33**, the power supply that feeds the PEBB1000 sitting at higher potential have to block higher isolation voltages. For n number of PEBBs connected in series, and the power supply must have an isolation strength of the maximum $n \cdot V_{ISO}$. This value can rise as high as hundreds of kilovolts, and thus the isolation and insulation design are quite challenging.

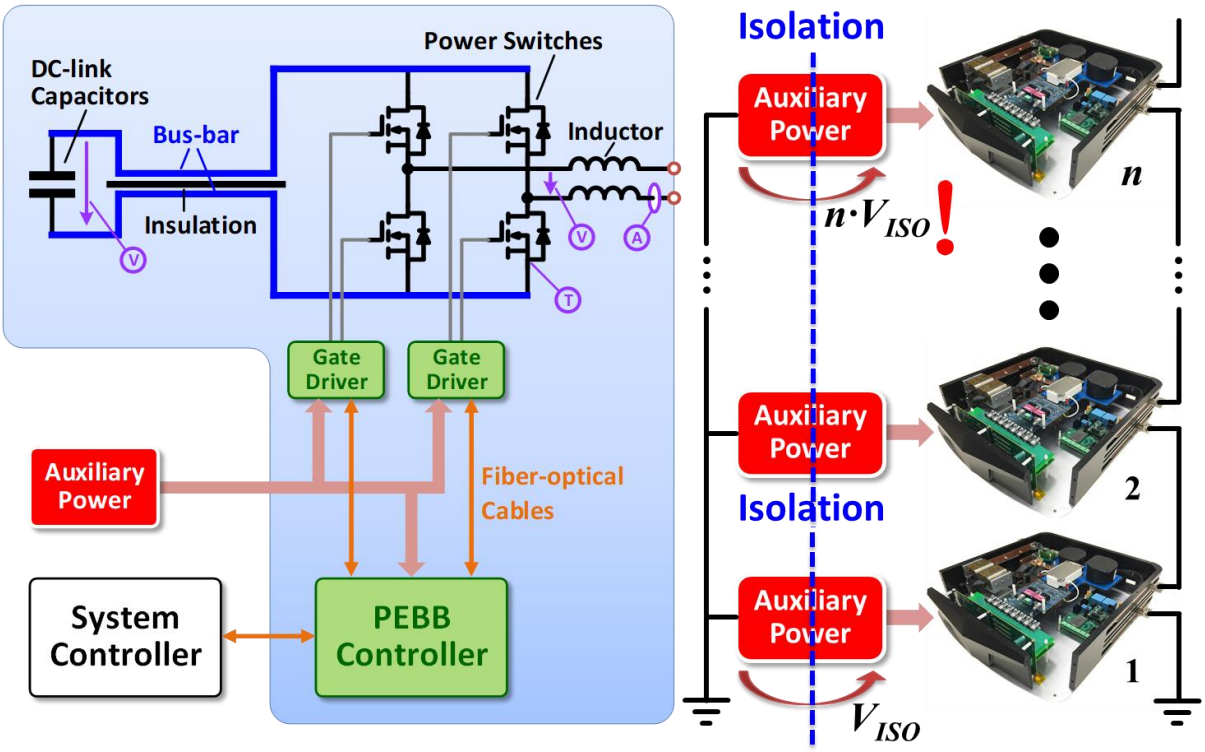


Figure 5-33 Auxiliary power for PEBB-based converters: from low-voltage external source

Another alternative option is the DC-bus-fed power supply that can avoid such extremely high isolation and insulation voltage requirements. The input to the primary side of the auxiliary power supply is from the local PEBB DC bus, and the secondary-side output feeds the gate drivers, controller, and sensors. **Figure 5-34** shows this architecture, where the maximum isolation/insulation stress is the DC bus voltage up to 1.2 kV. However, the most critical drawback of this architecture is that the power supply cannot start working until the DC bus voltage reach a "wake-up" threshold value. The SiC MOSFETs have to take the voltage with the absence of the gate driver, control, and sensor power. It requires additional particular circuit on the gate driver to ensure the safety of SiC MOSFETs under this circumstance. In the meantime, the wake-up voltage should be as low as possible. In this design, the threshold has been minimized as 230 V.

The design, prototyping, and testing have been conducted by Dr. Gabriele Rizzoli, a visiting scholar from the University of Bologna and a team member of the PEBB project. The two-switch flyback circuit has eventually been selected as a result of topology trade-off. The prototype is shown in **Figure 5-35**, with input voltage from 230 V to 1.2 kV and output voltage regulated at 48 V. More design considerations and details can be found in [E.6] .

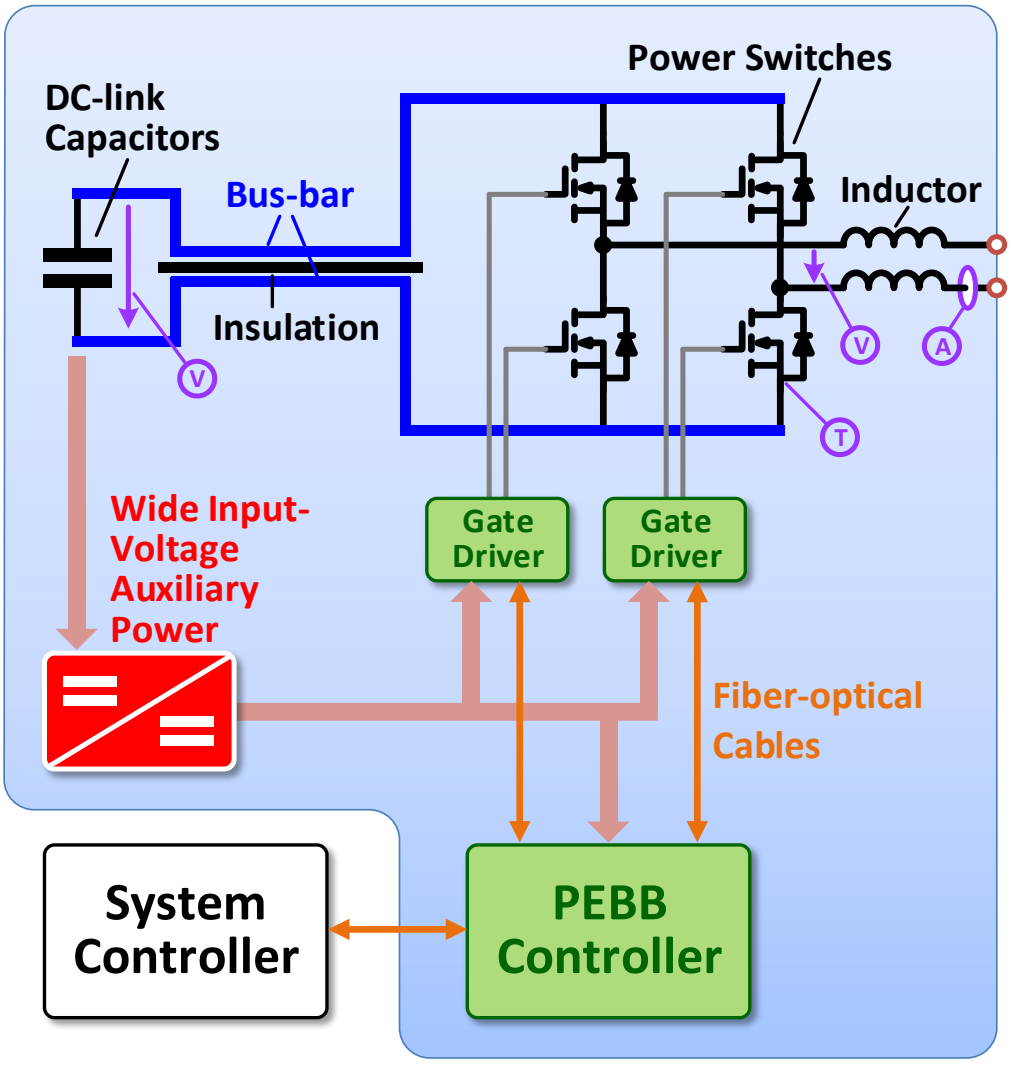


Figure 5-34 Auxiliary power for PEBB-based converters: from PEBB DC bus

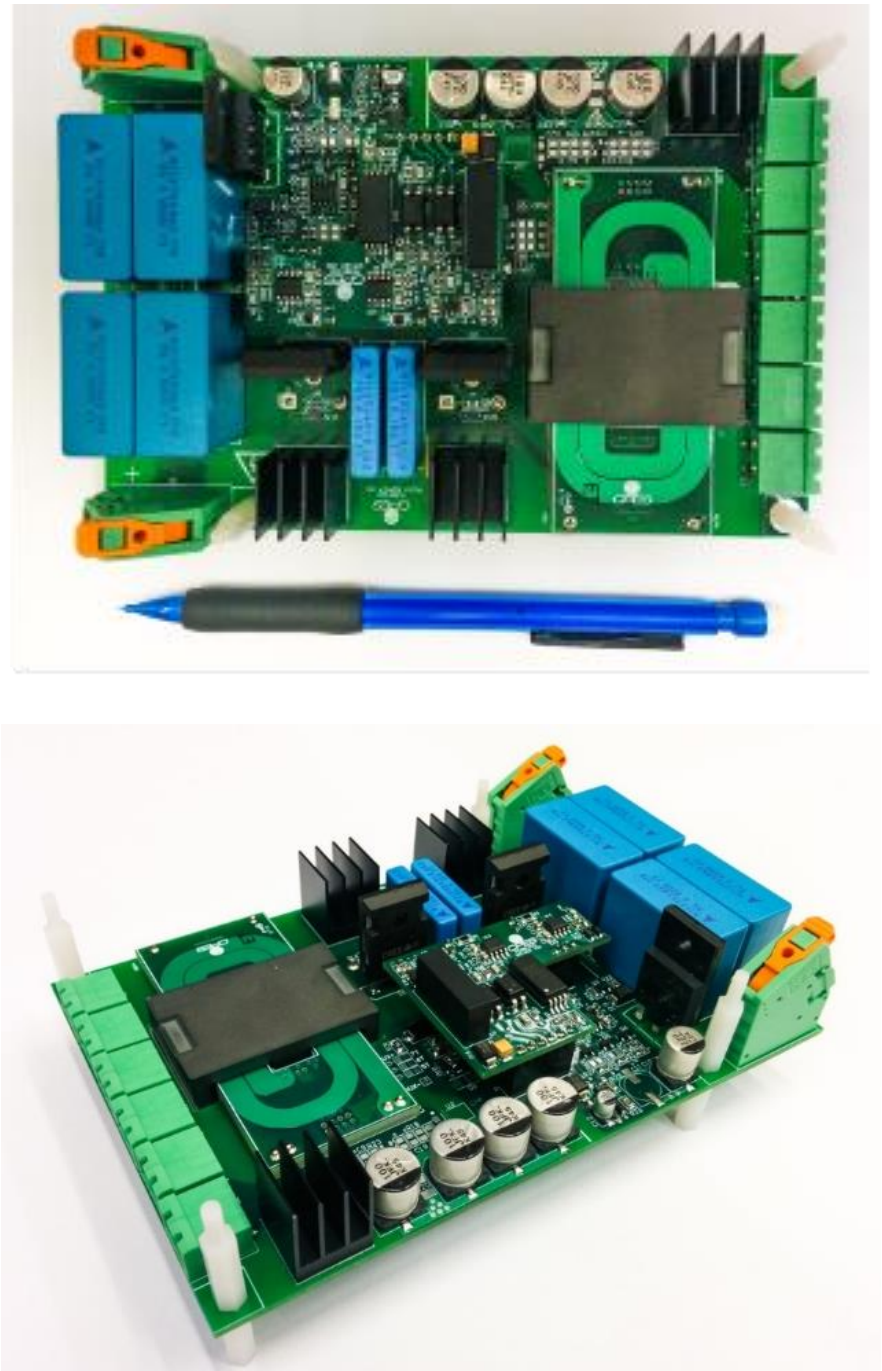


Figure 5-35 Auxiliary power supply prototype

5.4.2 Optical-fiber-based digital control system

A high-noise-immunity control and sensing system is the "brain" of a power converter. The PEBB should be smart enough to construct converters of different topologies and to fulfill different application profile. Therefore, information of voltage, current, and temperature at different locations of the power stage needs to be collected and transmitted to the PEBB controller for control regulations and health monitoring. This section introduces the design of an isolated digital sensor (IDS) and a digital controller developed by Dr. Zhiyu Shen.

The configurable IDS is able to sense current, voltage and temperature and finish A/D conversion locally at where it is installed, and then transmits digital signals to the digital controller. The IDS hardware is designed in a structure of stacking four PCB layers, shown in **Figure 5-36**. They are the interface layer, the signal conditioning layer, the digital signal processing layer, and the power supply layer. The interface layer has three design variants to fit the measure of current, voltage and temperature, respectively. The signal conditioning layer is basically the analog filters and instrumentation amplifiers that assures accurate and noise-free analog signals fed to the ADC. The digital processor layer consists of an ADC, an FPGA and a pair of optical transceivers. They are mainly responsible for digital signal sampling, encoding/decoding, and communications. The four layers of PCB are stacked in the sequence as the photo shows. The overall profile of the IDS is about 0.5 $inch^3$.

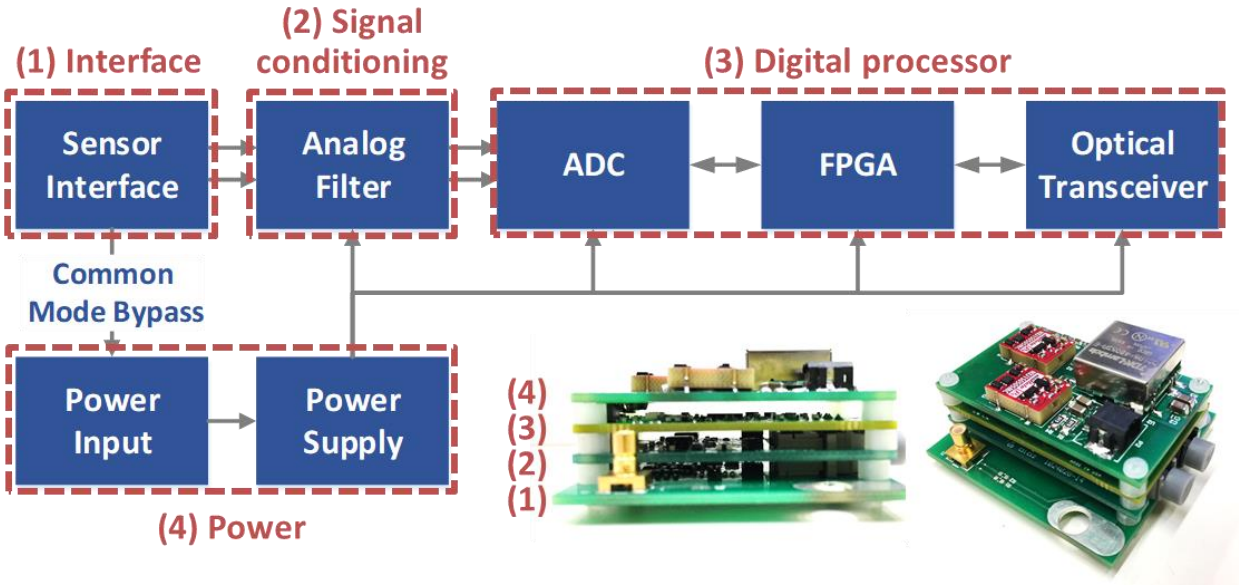


Figure 5-36 PCB stacking layout of the IDS

The PEBB digital control system is partitioned as shown in **Figure 5-37**. The local controller is built as conventional digital power converter controllers of an MCU-and-FPGA-based architecture. A communication interface (CNI) card can be plugged into the main controller, which connects to the MCU external memory bus. It provides necessary functions to form a distributed communication network.

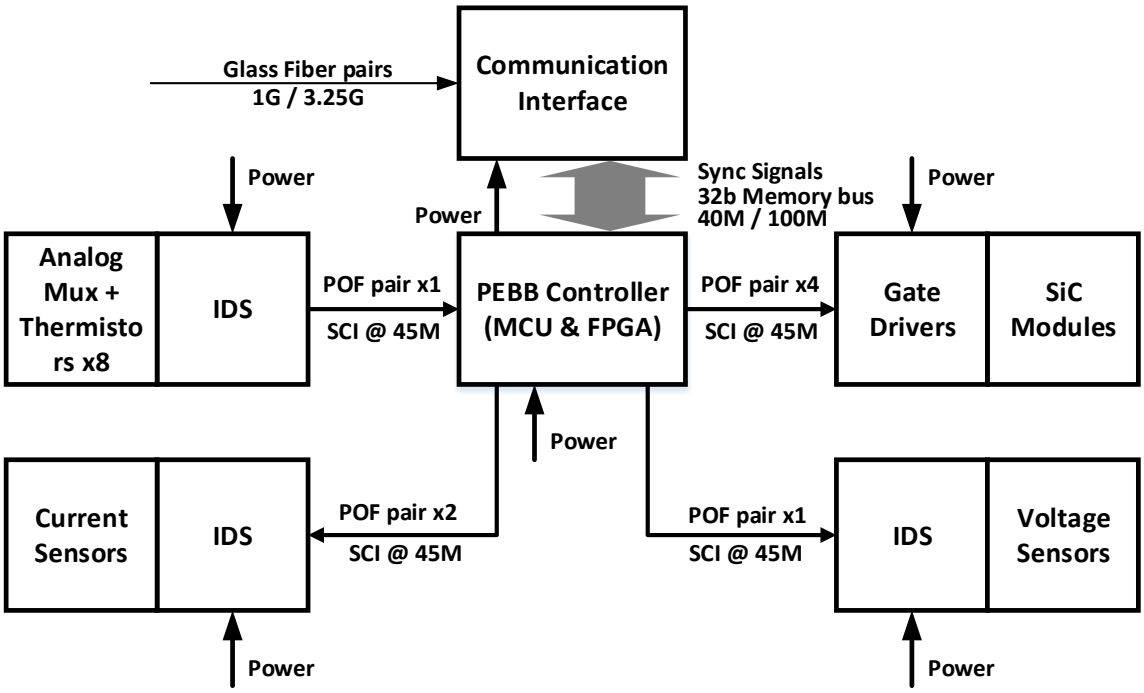


Figure 5-37 PEBB control system hardware partition

The main controller talks to all the peripherals such as the IDS and gate drivers via optical fiber connections, as shown in **Figure 5-38**. The fiber connection provides sufficient insulation and isolation strength that is able to function normally under high dv/dt noises generated by SiC MOSFETs. In this way, the main controller PCB set has only one single CM electrical connection point, the power supply. It eliminates CM noise propagation loops to avoid malfunction issues in the control circuit.

In the PEBB, plastic optical fiber (POF) is used due to their lower cost and smaller footprint. However, their speed is relatively slow, so a "star" connection with the PEBB controller as the center/master is used. It also simplifies the synchronization process between different IDS and drivers. The driver receives either PWM gating signals or communication data according to the application demands. The delay variation over the short fiber link is negligible. More design details and communication protocols have been elaborated in [E.7] .

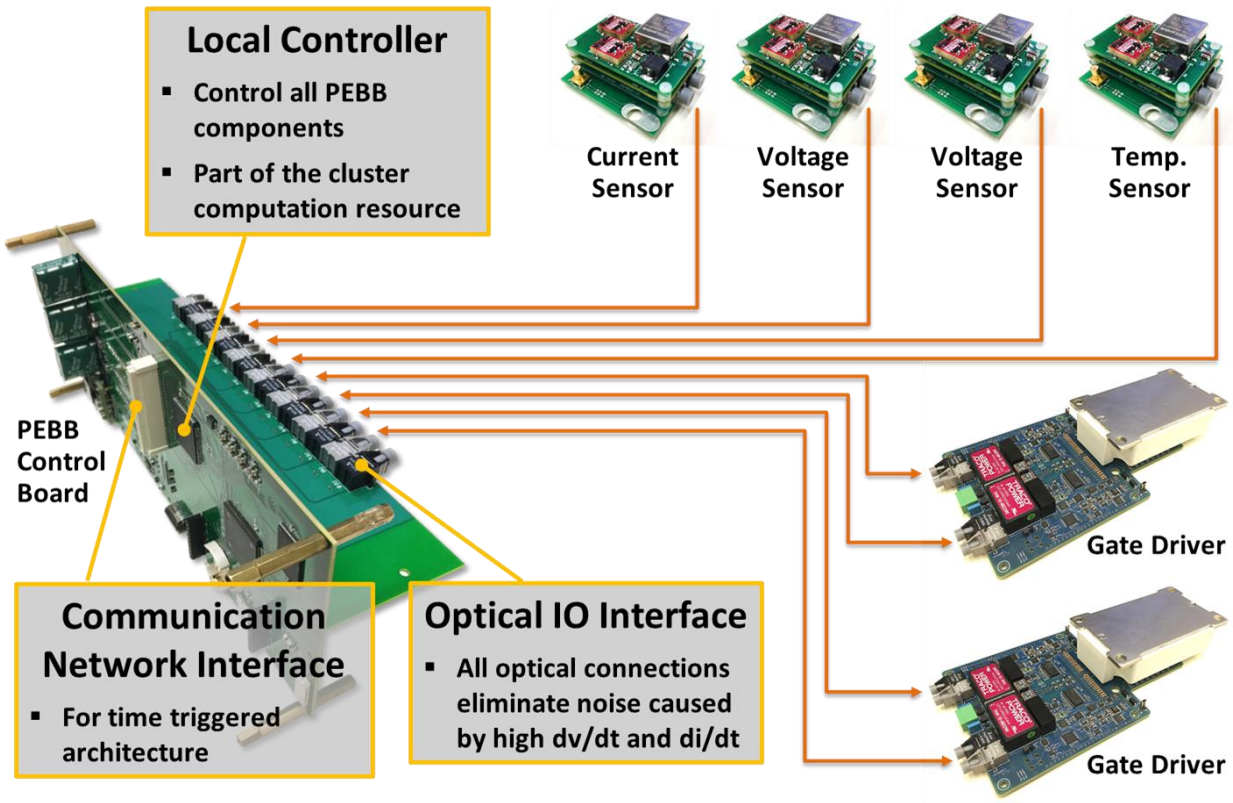


Figure 5-38 POF-based PEBB control system and local control board

5.4.3 System integration and PEBB test

The final assembly of the PEBB is shown in **Figure 5-39**. The power stage is completely symmetric from top to bottom such that the parasitics are symmetric. The two SiC MOSFET modules terminals are facing at each other, and their baseplates are facing to the top and bottom separately so a double-side cooling approach can be implemented. The two module baseplates are mounted to PEBB baseplates with thermal grease in between. The PEBB baseplates are the two cooling interfaces of the PEBB. Either air-cooled heat-sinks or water-cooled cold plates can be mounted on the base plates to dissipate the heat. The power stage interfaces are at the left side (AC) and right side (DC), with two copper blades that can slide into copper clips mounted on the cabinet (**Figure 5-40**). The interface for optical fiber connections is at the back side, and the front of the PEBB is for human-machine interfaces. By this design, the PEBB can be installed or replaces by plug-and-play that is highly friendly for maintenance.

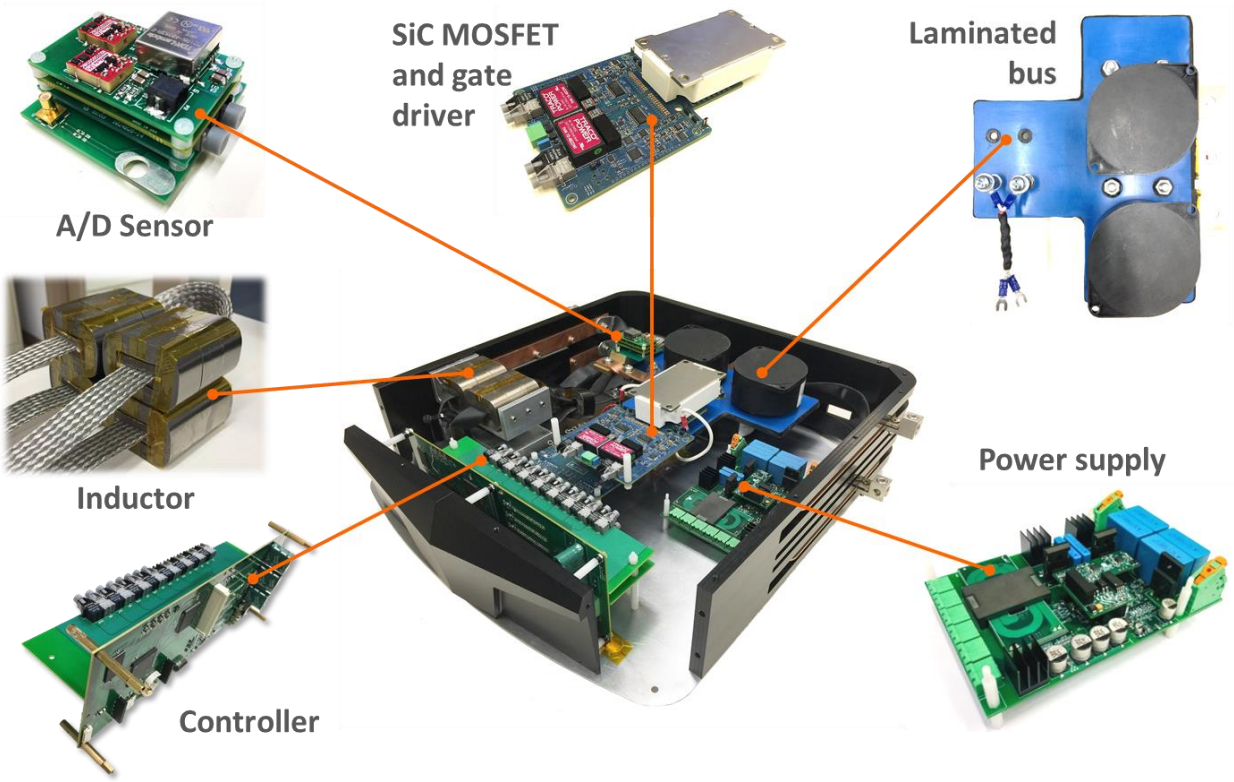


Figure 5-39 PEBB mechanical layout

Figure 5-40 PEBB interfaces

Various tests have been conducted in different converter test platforms and measurement systems to validate component behaviors. The double-pulse test and multiple-pulse test, and quasi-square wave test on one phase-leg for the gate driver, RSCS, SVS, and IDS evaluation. After the PEBB1000 has been fully assembled, an H-bridge DC-DC test with external load inductor, capacitor and resistors have been carried out.

The test platform configurations are shown in **Figure 5-41**. A 1 kV, 100 kW isolated DC source Magna-Power TQ1000-100/480 has been used to convert the 480 V AC from the grid to 1 kV DC. The DC source is supplying the PEBB1000 DC bus via a CM choke, in case that the high-frequency CM current trips the protection of the DC source. The PEBB DC bus voltage is raised to the nominal 1 kV. The gate signals given to the two phase-legs are complementary, so the H-bridge switching node V_{PH} sees ±1 kV voltages. The duty cycle for the Phase-A low-side switch is 0.65. The PEBB AC terminal current reaches the maximum value of 305 A, as defined by the PEBB1000 specifications in Chapter I. Other test parameters are shown in **Table 5-4**.

Table 5-4 H-Bridge Test Parameters

Parameter	Value	Parameter	Value
f_{SW}	100 kHz	V_O	300 V
T_{SW}	10 μs	I_O	260 A
V_{DC}	1 kV	L_O	45 μH
D_{A2}	0.65	C_O	200 μF
P_O	78 kW	R_O	1.15 Ω

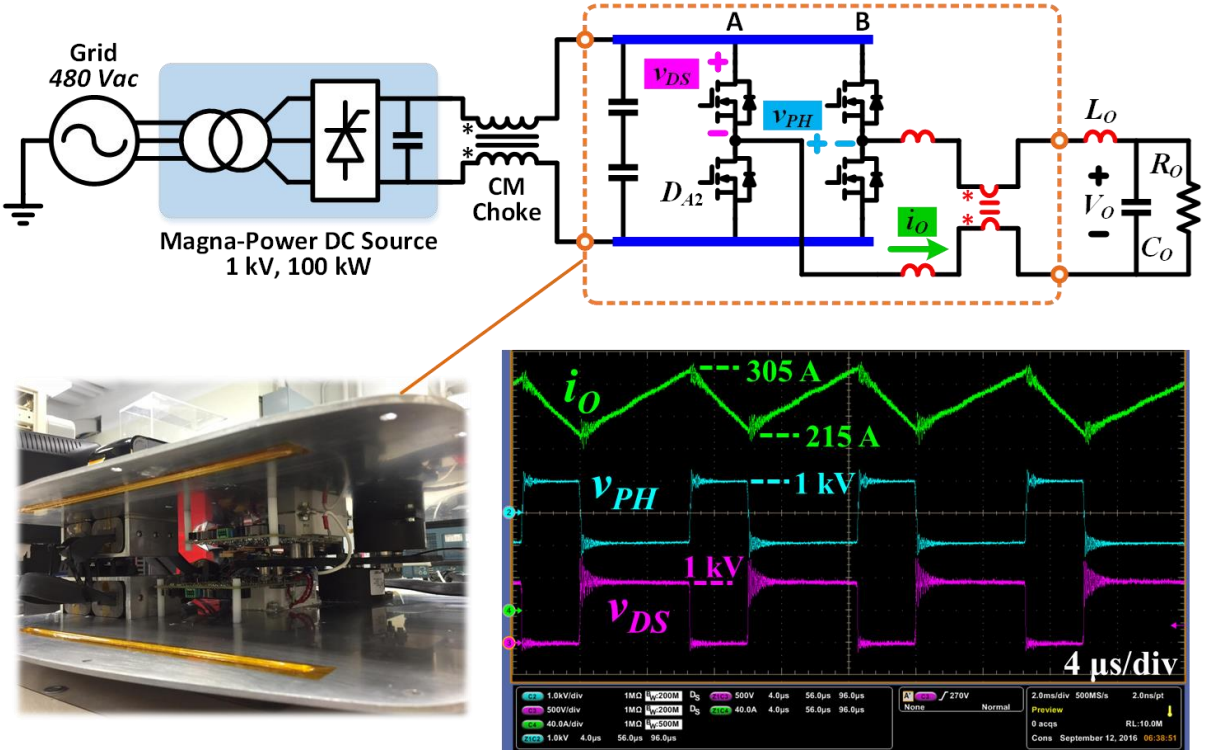


Figure 5-41 H-bridge DC-DC test, current i_O=305 A peak

Chapter.6 Hardware Realization of Closed-Loop HCM-SCC

6.1 Introduction

In Chapter 4, the SCC for MMC capacitor voltage balancing has been proposed and validated with simulations. In Chapter 5, a 100 kW SiC MOSFET-based PEBB1000 has been developed. In this Chapter, the SCC is validated in a single-phase two-module MMC converter constructed with the PEBB1000 prototypes.

6.2 Current Sensing Techniques

The biggest challenge in the HCM-SCC is the accurate high-BW sensing of the high-amplitude lower arm current i_L. The amplitude of i_L can be as high as the PEBB terminal current 300 A, and it contains rich components of DC, fundamental frequency, switching frequency, and other higher frequencies. The only commercial sensor to measure i_L is to use a high-power coaxial shunt resistor, which has huge size and weight, and very high cost. If the i_L sensing is not available, the switch current i_{S1L} and i_{S2L} can also serve for the HCM-SCC. **Figure 6-1** illustrates the fundamentals of this alternative approach. The red circles indicate that g_{S2L} is given a turn-off command when i_L touches I_{REF_H}*, which can also be achieved as soon as i_{S2L} touches I_{REF_H}*. Similarly, the blue circles indicate that g_{S1L} is given a turn-off command when i_L touches I_{REF_L}*, which can also be achieved as

soon as $-i_{S1L}$ touches I_{REF_L}*. Consequently, the objective of sensing i_L becomes sensing $-i_{S1L}$ and i_{S2L}.

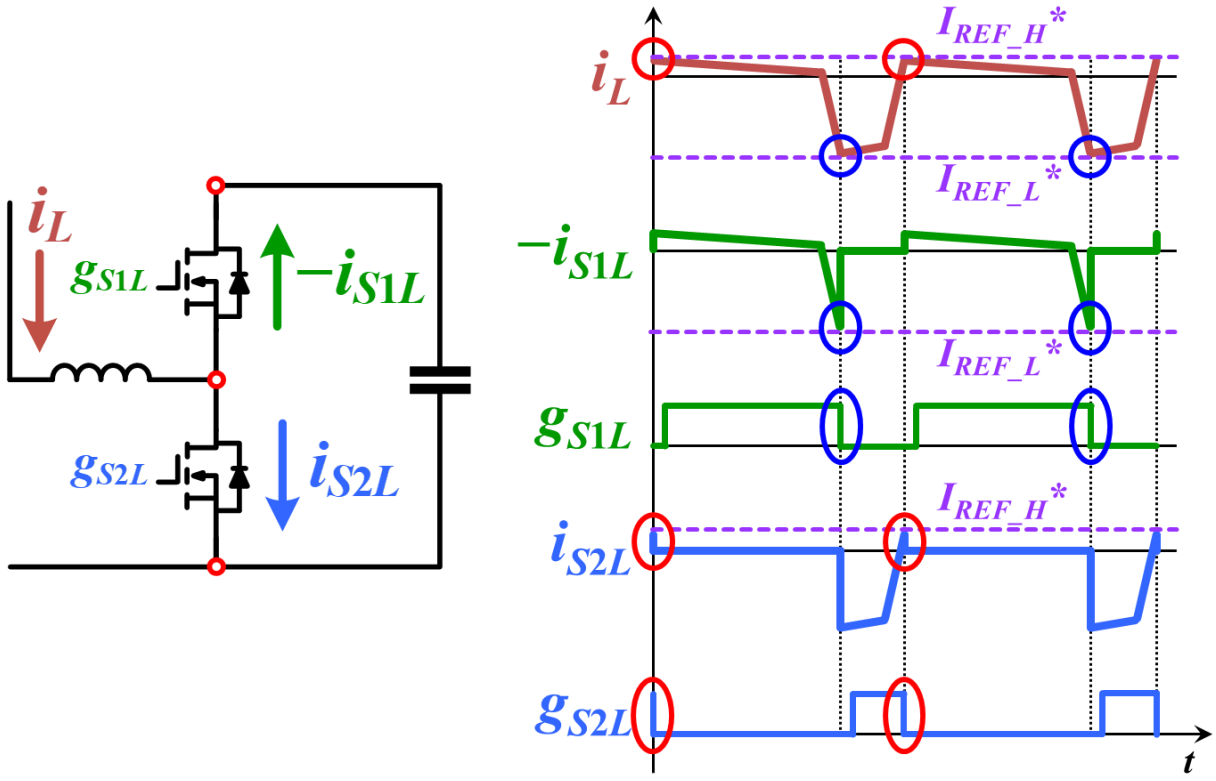


Figure 6-1 HCM-SCC using i_L, or using $-i_{S1L}$ and i_{S2L}

The RSCS is the solution that has already been proposed and validated in Chapter 4. The test has been conducted under a central control system for the purpose of simplicity, so another sets of RSCS board have been designed just for the control purpose. They are not integrated together with the gate driver. The sensed two switch-current signals $-i_{S1L}$ and i_{S2L} are directly given back to the PEBB controller. **Figure 6-2** shows the hardware implementation of the RSCS sensing system. The Rogowski coil board has been assembled on top of the SiC MOSFET module. The signals are transmitted to the signal processing board via two coaxial cables. The signal processing board is directly plugged into the analog sockets on the PEBB control board.

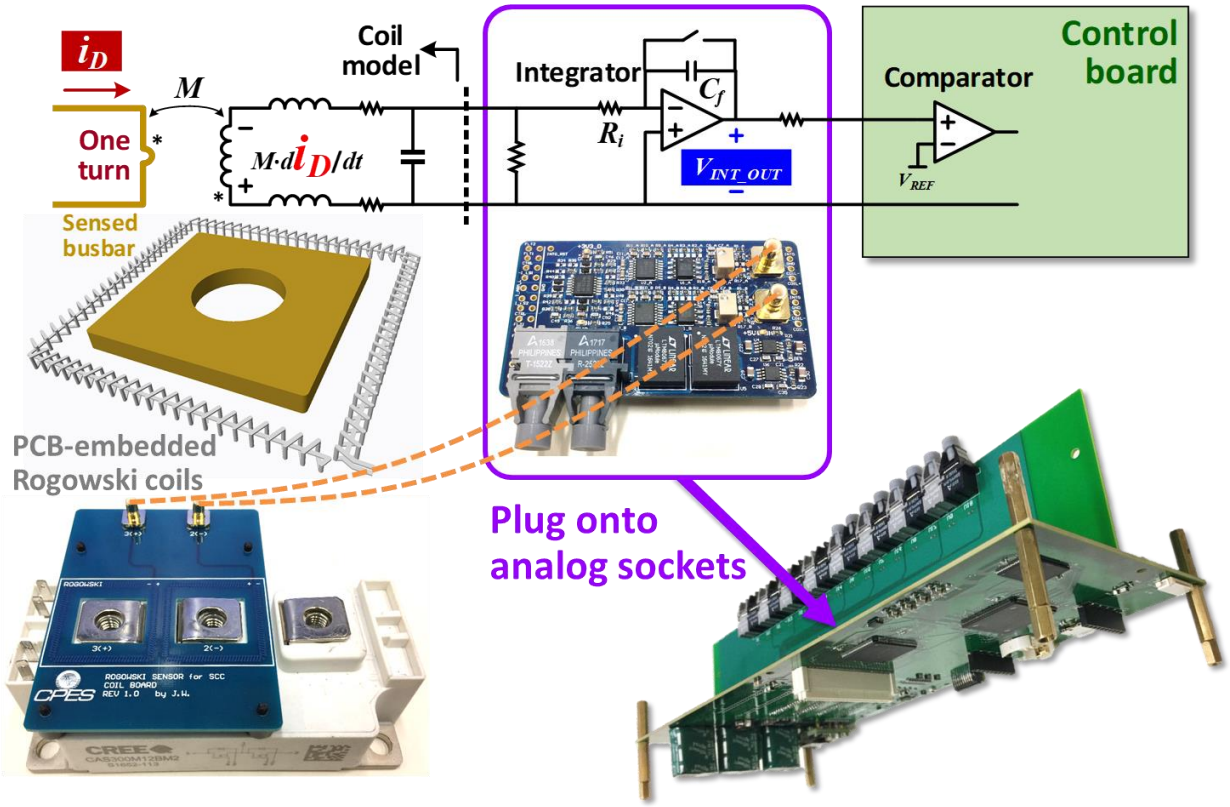


Figure 6-2 Hardware implementation of RSCS sensing system for HCM-SCC

6.3 Hardware Implementation

6.3.1 Closed-Loop HCM-SCC Architecture with Hardware

The hardware implementation of HCM-SCC is shown in **Figure 6-3**. The MMC topology is configured as a modular multilevel Buck converter (MMBC) where the average value of i_{PH} is DC. All the other arm current and capacitor voltage characteristics are similar same as the MMC. A precharge switch and resistor are designed at the positive DC bus. A load switch is connected between the phase-leg and the load inductor L_O to isolate the load during precharge. The two PEBB capacitor voltages are initially charged alternatingly to 95% of the nominal value by the 1 kΩ precharge resistor Ohmite TGHHV1K00JE within 300 ms. As soon as the precharge is completed, the MMBC quits the "precharge mode" by closing the precharge switch and the load switch, and then enters "normal operation mode".

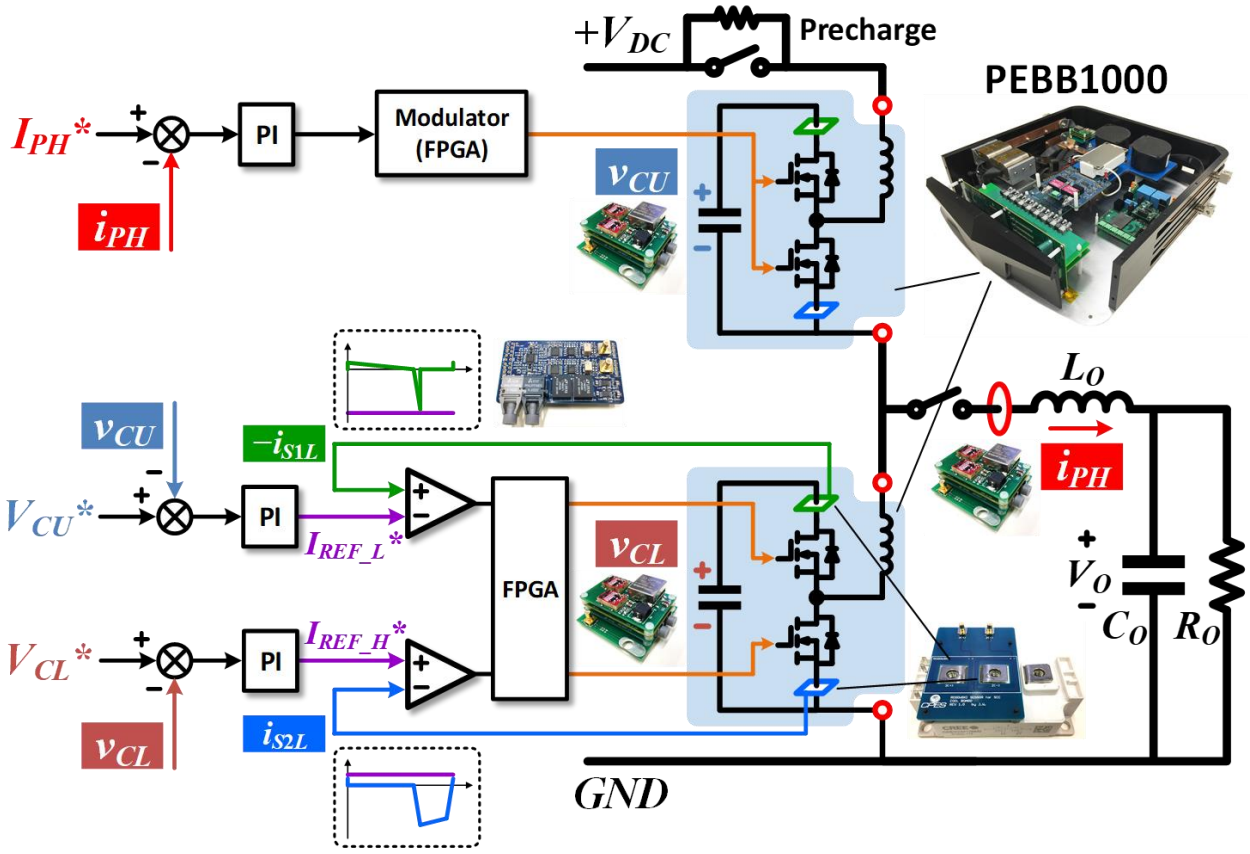


Figure 6-3 Hardware implementation of HCM-SCC

The phase current error is fed to a PI regulator in the DSP on the main control board. The regulator output sends a modulation reference to the FPGA via a parallel communication bus to generate gate commands to the half-bridge of the upper PEBB. The upper and lower capacitor voltage errors are fed to two PI regulators in the DPS. The two regulator outputs then generate the two reference currents I_{REF_H}* and I_{REF_L}* for PCM comparators at the DSP I/O. PCM feedback current $-i_{S1L}$ and i_{S2L} are from the RSCS with added level-shifters to fit the analog input specifications of the DSP I/O. The output of the comparators are also given to the FPGA on the main control board, which then generates the gate commands to the half-bridge of the lower PEBB.

The averaged phase current i_{PH} and averaged capacitor voltage v_{CU} and v_{CL} are sensed by the isolated digital sensors (IDS) that have been described in Chapter 5. The sampling command and data transmission are accomplished between the main FPGA on the main control board and the FPGA on the IDS, via a pair of plastic fibers at a sampling frequency of 2 MHz. For the switching frequency of 40 kHz, there are 50 sample points in each switching period. In the SCC operations, the ripple of i_{PH}, v_{CU} and v_{CL} are not in triangular patterns, and thus the sample point in the peak of triangular carrier waveforms does not accurately represent the average current or voltage values anymore. Therefore, the main FPGA sends all those sampled data to the DSP via the parallel communication bus, and the averaged i_{PH}, $v_{CU,}$ and v_{CL} of one switching cycle are then calculated in the DSP.

From the illustration of the hardware implementation of HCM-SCC, it is noted that the duties of the DSP and the FPGA on the main control board are well allocated. The DSP is in charge of operation mode management, parameter configurations, closed-loop regulator computation, PCM comparison and current limiters. The FPGA is responsible for data sampling, PWM modulation, dead-time generation, PCM gate command generation, State-III/IV time limiter, and fault protection. The DSP and FPGA talk to each other via the high-speed parallel communication bus. In this central control system for two PEBBs, the FPGA on the main control board contains the gate information of both upper and lower PEBBs, so the synchronization and timing of all the gate commands can be accomplished simply and effectively. If the distributed control system is applied in the future, the synchronization and data exchange between the multiple main FPGAs in multiple PEBBs become quite challenging and critical.

6.3.2 Test Platform Construction

The test platform for experimental validation of HCM-SCC is shown in **Figure 6-4**. The mechanical locations of the upper and lower PEBB1000 LRUs plugged into a white rack are corresponding to the MMBC topology configurations. Two IDS voltage sensors are installed inside the two PEBBs, respectively. One IDS current sensor is installed next to the load inductor. The Rogowski coil board with two coils are mounted on top of the gate driver board inside the lower PEBB. The Rogowski coil outputs are transmitted via two SMB connectors and coaxial cables to the Rogowski signal processing board, which is plugged onto the main control board. The fiber-optic interface board mounted vertically

on the main control board, transceives digital signals to/from the gate drivers and IDS sensors via plastic optical cables.

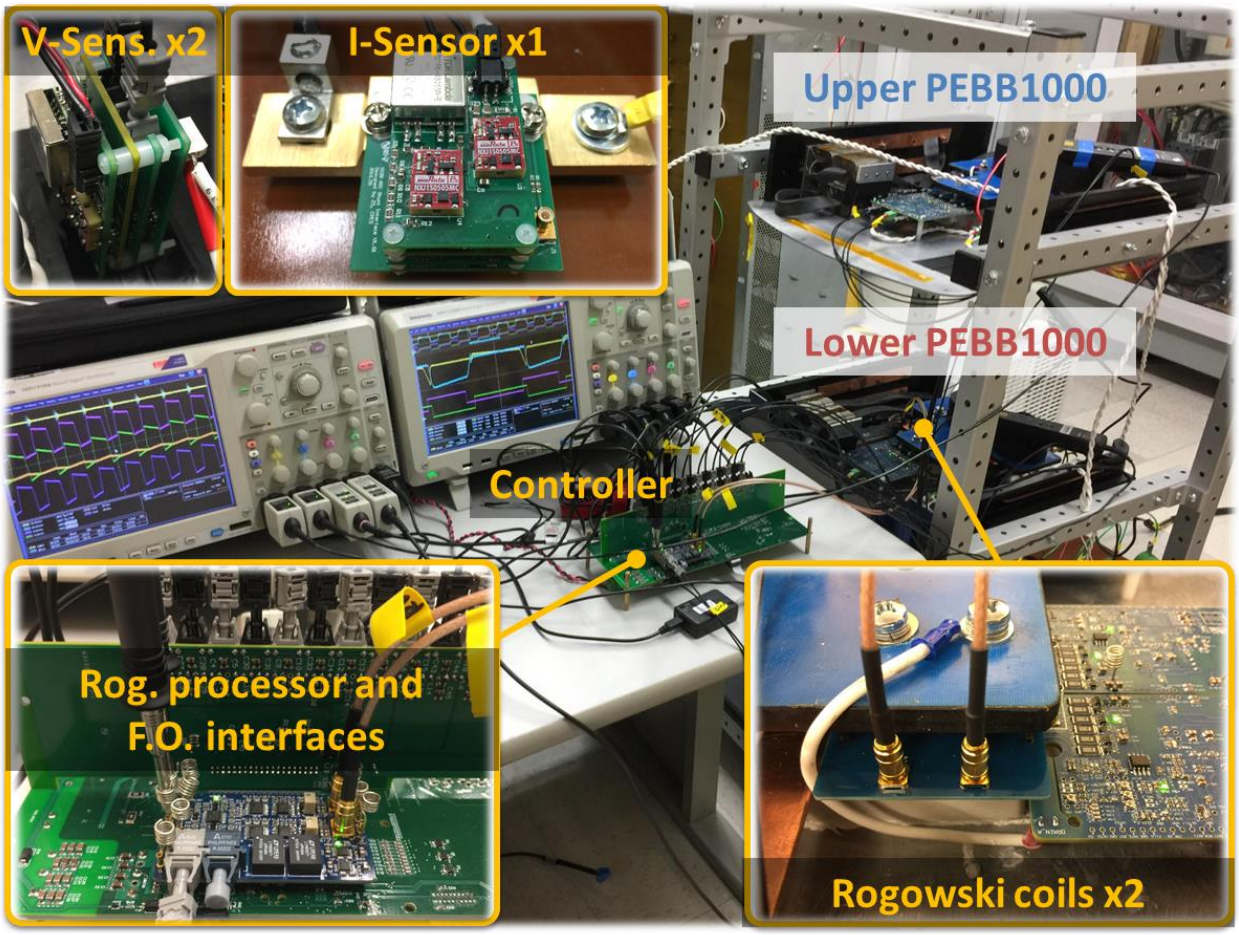


Figure 6-4 Test platform for experimental validation of HCM-SCC

6.3.3 Experimental Validation

The MMBC test parameters are shown in **Table 6-1**. The switching frequency is 40 kHz, DC bus voltage is 500 V and the output current is 50 A. The duty cycle command to the upper PEBB half-bridge is 0.62, while the effective output duty cycle is 0.57. The difference is caused by the use of State III and IV. The capacitor voltage PI parameters K_{P_Vcap} and K_{I_Vcap}, and phase current PI parameter K_{P_Iph} and K_{I_Iph} are also shown in the table. **Figure 6-5** shows the test waveforms at the given setup. It is observed that the capacitor voltages scale is 100 V/div, v_{CU} and v_{CL} are controlled steadily at 500 V, with excellent balancing at every switching cycle without drifting. The switching-frequency ripple is trivial, with only 40 V peak-to-peak parasitic ringing observed at around 5 MHz due to the ESL and bus-bar inductance of the series DC-link capacitors. The phase current i_{PH} has about 8 A switching frequency ripple, and four switching states on it are observed. The two arm current i_U and i_L and mean current i_{MEAN} are operating at the SCC mode, whose dominant frequency component is at 40 kHz.

Table 6-1 Component and Control Parameters in MMBC Test with HCM-SCC

Parameter	Value	Parameter	Value
f_{SW}	40 kHz	L_O	600 μH
T_{SW}	25 μs	C_O	50 μF
V_{DC}	500 V	R_O	5.7 Ω
D_{S1U}	0.62	K_{P_Vcap}	0.01
D_{EFF}	0.57	K_{I_Vcap}	5
V_O	285 V	K_{P_Iph}	0.01
I_O	50 A	K_{I_Iph}	0.5
P_O	14.25 kW	η	99%

The bottom waveforms of **Figure 6-5**, the switch current $-i_{S1L}$ and i_{S2L} on the RSCS signal processing board are shown. A plus operation between them is done by the oscilloscope, giving

(6-1) $$i_{L\_SEN} = i_{S2L} + (-i_{S1L})$$

The waveform of i_{L_SEN} and i_L are almost identical except a small portion of the peak value that has been filtered by the sensor processing circuit. The results validate that the switch currents sensed by RSCS are accurate enough for analog PCM control approach.

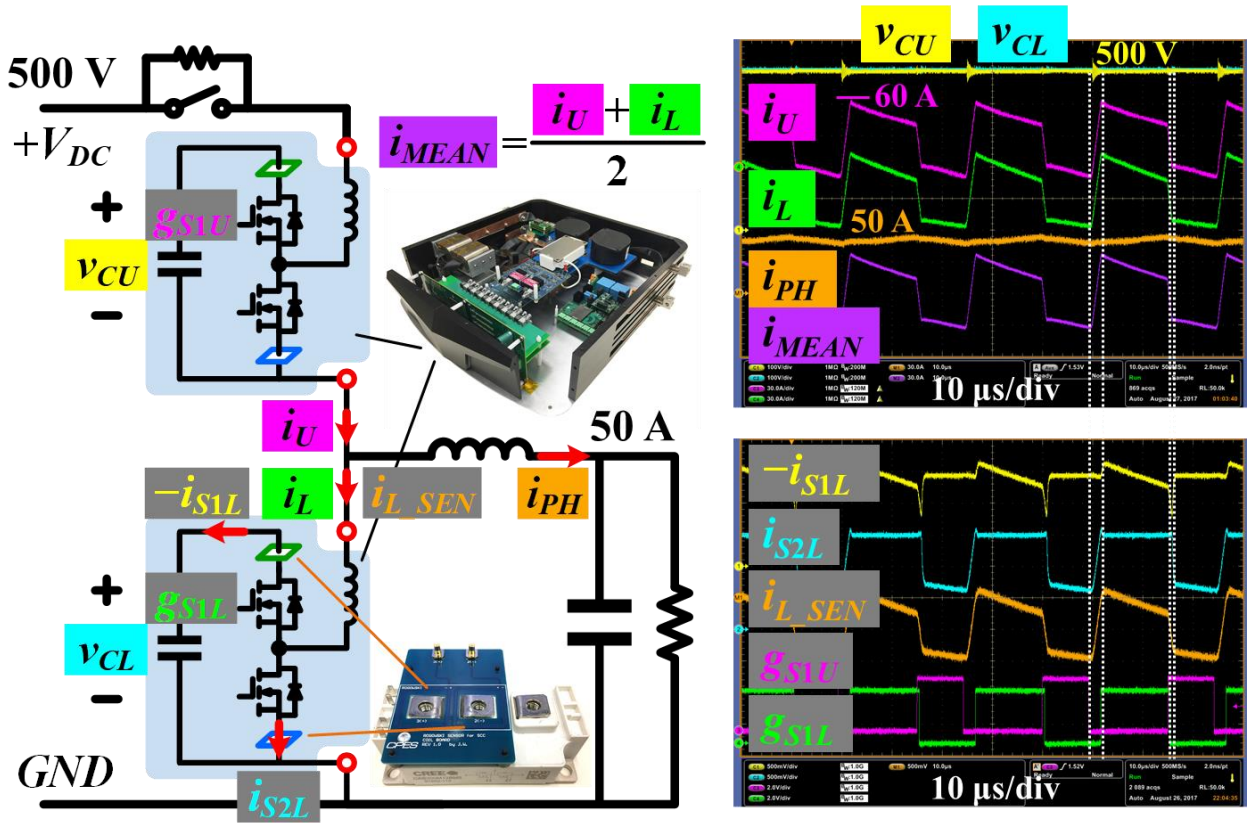


Figure 6-5 Experimental results of HCM-SCC

Figure 6-6 shows the ZVS turn-on behavior of all the four switches. The signal signals g_{S1U}, g_{S2U}, g_{S1L} and g_{S2L} are the gate commands sent from the main controller FPGA, rather than the real gate terminals on the gate driver board. There is about 200 ns total delays between the FPGA commands and the gate-source voltages. Therefore, all the actual gate-source voltages are fired after the drain-source voltage V_{DS1U}, V_{DS2U}, V_{DS1L} and V_{DS2L} are discharged by the arm currents. No device turn-on voltage ringing is observed in the waveforms.

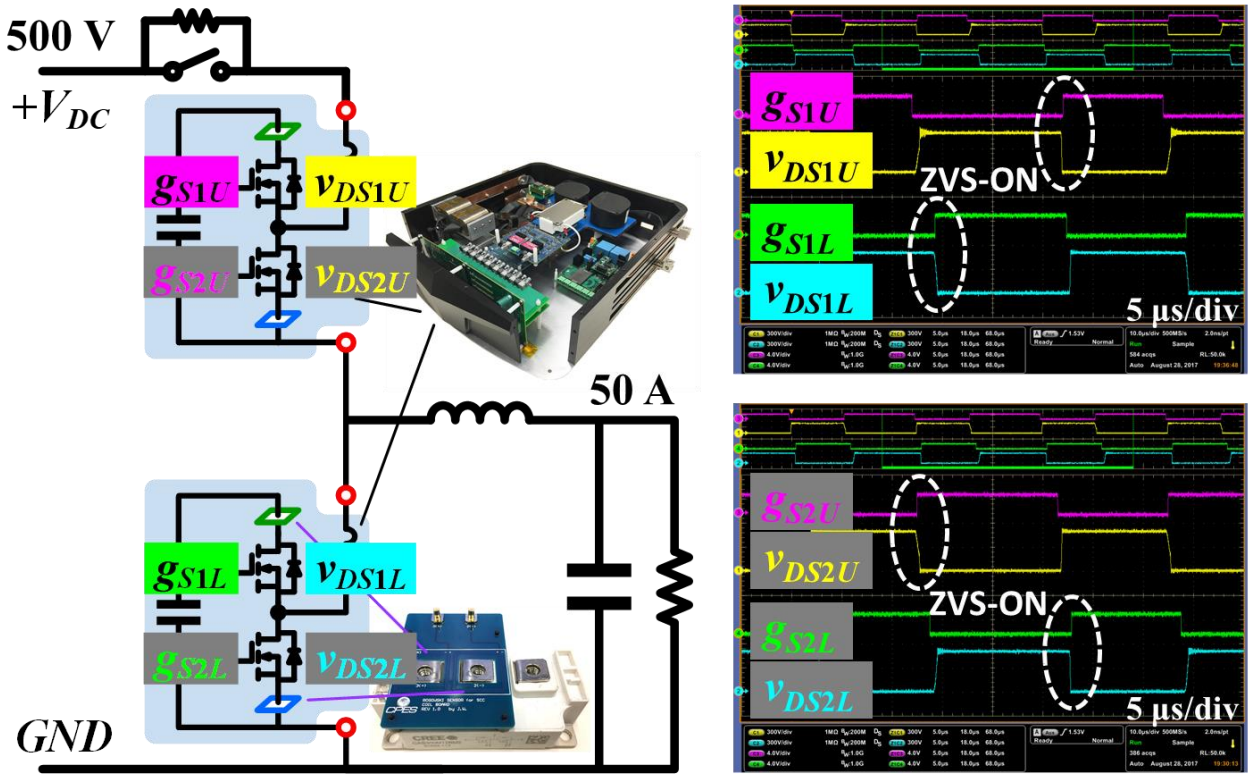


Figure 6-6 ZVS behavior of HCM-SCC

A phase current step-down test has been conducted to assess the dynamic behavior of the closed-loop HCM-SCC control with the given PI parameters. The phase current reference step from 50 A to 40 A is generated in the DSP controller. **Figure 6-7** shows the three control objectives: phase current i_{PH}, upper capacitor voltage AC component v_{CU_AC}, and lower capacitor AC component v_{CL_AC}. The phase current reaches steady state in about 100 ms with no overshoot. The capacitor voltage DC components are at 500 V. The upper capacitor presents a dynamic overshoot voltage about 4 V, and the high-frequency parasitic ringing peak of 12 V at 5 MHz due to the operation mode transient. The lower capacitor presents a dynamic undershoot voltage about 10 V. All the control objectives reach steady states within 400 ms. Overall speaking, the capacitor voltage dynamics behaviors contain trivial transients less than 2.4% of the nominal values.

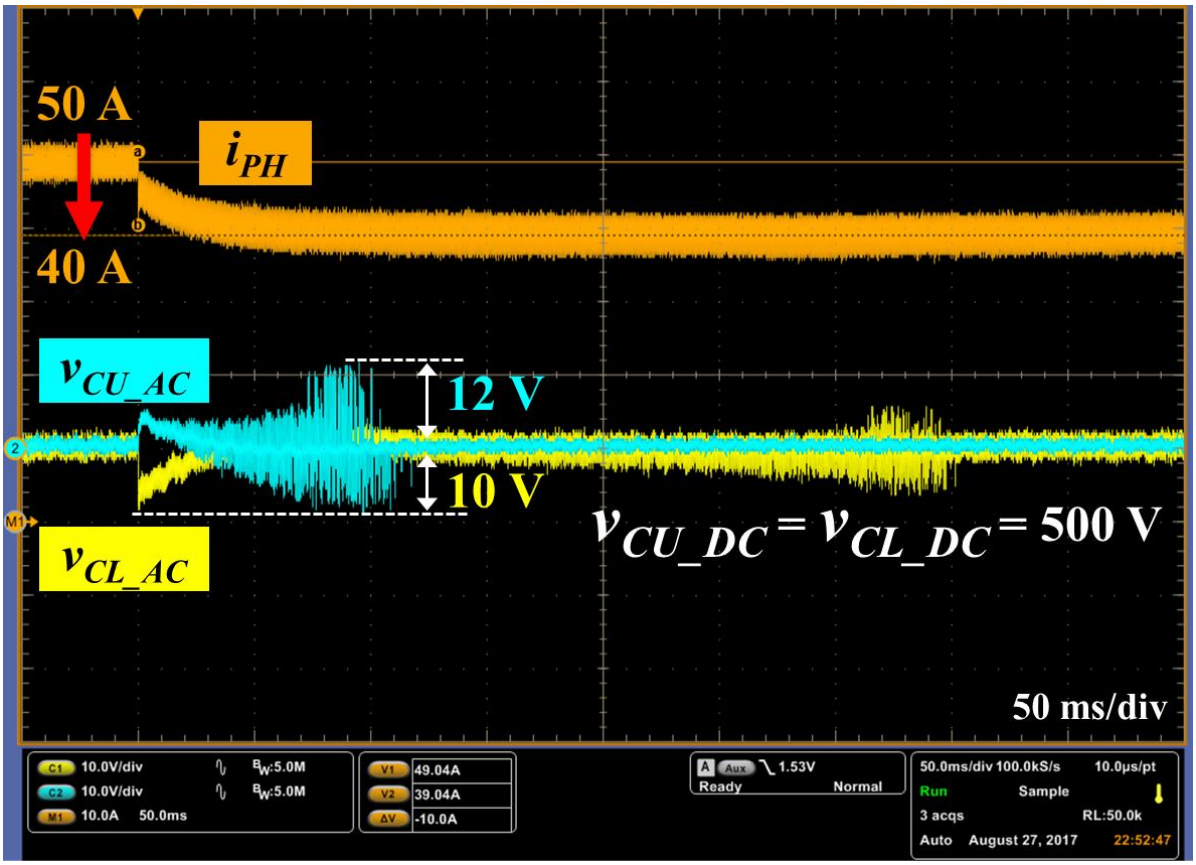


Figure 6-7 Closed-loop dynamic behavior: phase current steps from 50 A to 40 A

Chapter.7 Summary and Future Topics

This dissertation presents high-frequency control and sensing techniques that are used to reduce the passive components size and active device loss of the SiC-based modular multilevel converter (MMC). The proposed switching-cycle control (SCC) modulates the arm current to switching frequency, and thus capacitor voltages are balanced in every switching cycle. The polarity change of the arm current every switching cycle also enables zero-voltage switching (ZVS) behavior of all the SiC MOSFETs, which nearly eliminate the turn-on losses. In order to realize closed-loop SCC, the hybrid-current-mode switching cycle control (HCM-SCC) has been proposed that directly regulates the load current and capacitor voltages.

The HCM-SCC relies on high-amplitude, high-bandwidth, and high-accuracy switch current sensors. This is realized by a proposed Rogowski switch-current sensor (RSCS) developed for SiC MOSFET modules. In addition to the current control, the RSCS also serves as a great short-circuit detector that is suitable for the SiC MOSFET protections.

A power electronics building block with 1 kV DC bus voltage (PEBB1000) has been developed based on SiC MOSFET modules. The design of gate driving, sensing, and control system for high-dv/dt-rate environment is accomplished. The proposed HCM-SCC and RSCS have been validated on the PEBB1000-based converter prototype.

As the SCC and HCM-SCC are proposed and validated for the first time, a lot more work can be done for better understanding the essence and limit of the new control scheme.

On the SCC, future research topics are as follows,

- Small signal modeling of the SCC and HCM-SCC for MCC-type converters.
- Closed-loop realization of SCC for MCC-type converters with more than one PEBB per arm.
- Multi-objective optimization of the MCC-type converters that use the SCC control scheme.
- SCC on a de-centralized control system for converters with a large number of PEBBs.

On the smart gate driver, future research topics are as follows,

- Integrating all necessary sensors on the gate driver board for converter control and protection.
- Smarter gate drivers with device health monitoring and failure diagnostics.

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