Design of a 15MW Solid-State Linear Transformer Driver for Gas Switch Triggering Applications

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Abstract

Field-reversed configuration (FRC) research and pulsed high-energy experiments are in a need of an upgrade. Studying nuclear fusion and obtaining high energy yields for flash x-ray radiography using plasma or particles can be made easier through faster switches. One newly emerging technology is called the Linear Transformer Driver (LTD). These switches are becoming more commonly used in the solid-state domain. While gas spark gap switches can supply high power, they cannot be turned off when engaged. Solid-state switches on the other hand can, and when integrated into the LTD topology, these switches can operate like their spark gap peers. Even better, solid-state switches can be switched in the sub-nanosecond regime with minimal jitter. With the advent of solid-state LTD technology, fast rise-time high energy applications in nuclear science and plasma physics experiments are possible. This has led to the design and development of a 30kV and 500A solid-state LTD. The designed LTD can achieve a rise-time under 10ns and has a high potential to achieve less than 1ns jitter. This thesis details every aspect of the LTD design process. A novel code has been developed to estimate the feasibility of a variety of solid-state switches and costs. This feasibility code has been shown to have a good correlation with real life prices that it models. A new detailed LTD model has been made as well and shows a strong correlation with other LTD models. The new model also shows voltage transient spiking of the pulsed waveform attributed by the primary inductance of the LTD. Overall, the design tools gathered and made in this thesis will help any engineer developing a solid-state LTD for their application.

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- Dr. Ryusuke Hasegawa

When trying to figure out the type of copper to use, along with the continuous quotes I needed to collect for the transformer of the LTD, I was fortunate enough to have an excellent sales representative from Cadi Company, Inc. quickly get back the needed quotes and tolerances. Her name is Liza Beyer and she definitely has made designing my LTD a lot easier.

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Chapter 1

Introduction

The Magnetized Shock Experiment (MSX) at Los Alamos National Laboratory (LANL) investigates the physics of magnetized shocks in plasmas.

The laboratory is able to make their experiment work by employing the use of field-reversed configuration (FRC) technology. The FRC allows the experiment to achieve high energy by accelerating the plasma into a magnetic mirror. [18]

FRC technology is not only for MSX, it can also be employed to generate nuclear fusion energy, and theoretically can be used to make a propulsion source for space vehicles that have an efficiency of 80%. This 80% number is significantly larger than other pulsed power propulsion sources that can only achieve 50%. This 80% however is only possible with the advent of new solid-state technologies. [18]

The electrical switches used to provide pulsed power for MSX at LANL is presently done using inefficient technologies. The spark gaps being used have large amount of triggering jitter. In order to do more effective experiments requires to have switches with a jitter of under 1ns and a rise time of under 10ns. [18]

Novel pulsed power technological approaches such as the Linear Transformer Driver (LTD) are becoming better understood and can be employed to solve the inefficiency problem at

MSX. LANL is presently looking into employing solid-state LTDs to drive efficient custom-made spark gaps that will drive the FRC at MSX.

1.1 Purpose and Goals

This thesis focuses on the development of a 15MW solid-state LTD. The new spark gap being developed for LANL will be documented in another thesis. Work being done on the spark gap shows that to power one of them required 30A of current and ideally a voltage of 30kV. The first goal of this thesis is to make the LTD achieve 30kV output. The second goal relates with cutting down on costs, as the LTD should be able to power multiple spark gaps, hence the current requirement is set at 500A. The third goal is that the LTD should achieve a rise time of under 10ns, and a jitter of less than 1ns to be a viable switch. The pulse-length does not matter once the LTD reaches its maximum voltage, hence power requirements on materials being used can be relaxed. Finally, the last goal is to keep the LTD compact, and must be within a three foot by one foot diameter enclosure. Present technology has opened up the possibility in achieving these specifications.

1.2 Structure of Thesis

This thesis is organized by first discussing the background and the concepts behind the Linear Transformer Drivers in Chapter 2. A survey on related work is provided in Chapter 3. I then conducted a feasibility study to optimize the components to be used in a Linear Transformer Driver for my application in Chapter 4. In Chapter 5 I delve into the engineering of each aspect of the Linear Transformer Driver to be built. The expected simulated performance of my Linear Transformer Driver and models can be seen in Chapter 6. Finally, in Chapter 7 I offer my conclusions and suggestions for future work.

Chapter 2

Background

This chapter discusses the history of the Linear Transformer Driver and what defines a LTD. Next, this chapter goes into a brief summary of available solid-state technologies. This is necessary in order to have an understanding of the solid-state engineering work that is discussed throughout this thesis. Finally, the chapter finishes up with the differences between the conventional transformer core and its model and the pulsed power core and its model.

2.1 Linear Transformer Driver

In the 1980s, a new pulsed power switch was developed called the Linear Transformer Driver. This was founded at the Institute of High Current Electronics in Tomsk, Russia. The LTD is a great improvement over older Marx generator pulsed power switches. The Marx generator is a bank of capacitors, where they are charged in parallel at a low voltage, then connected in series to achieve higher voltages. As can be thought of, the individual switches connecting each of the capacitors in series adds jitter that makes it challenging to bring down to the sub-nanosecond range.

2.1.1 Summary of the Physics Behind the LTD

The LTD replaces Marx generators, while greatly enhancing switch performance. However, it is not just the enhanced performance, but the ability to take smaller switches such as solid-states and use them relatively easily in a high-voltage line. This is due to the physical make-up of the LTD. To make it easier to understand, a graphic showing a single stage of the LTD can be seen in Figure 2.1 below.

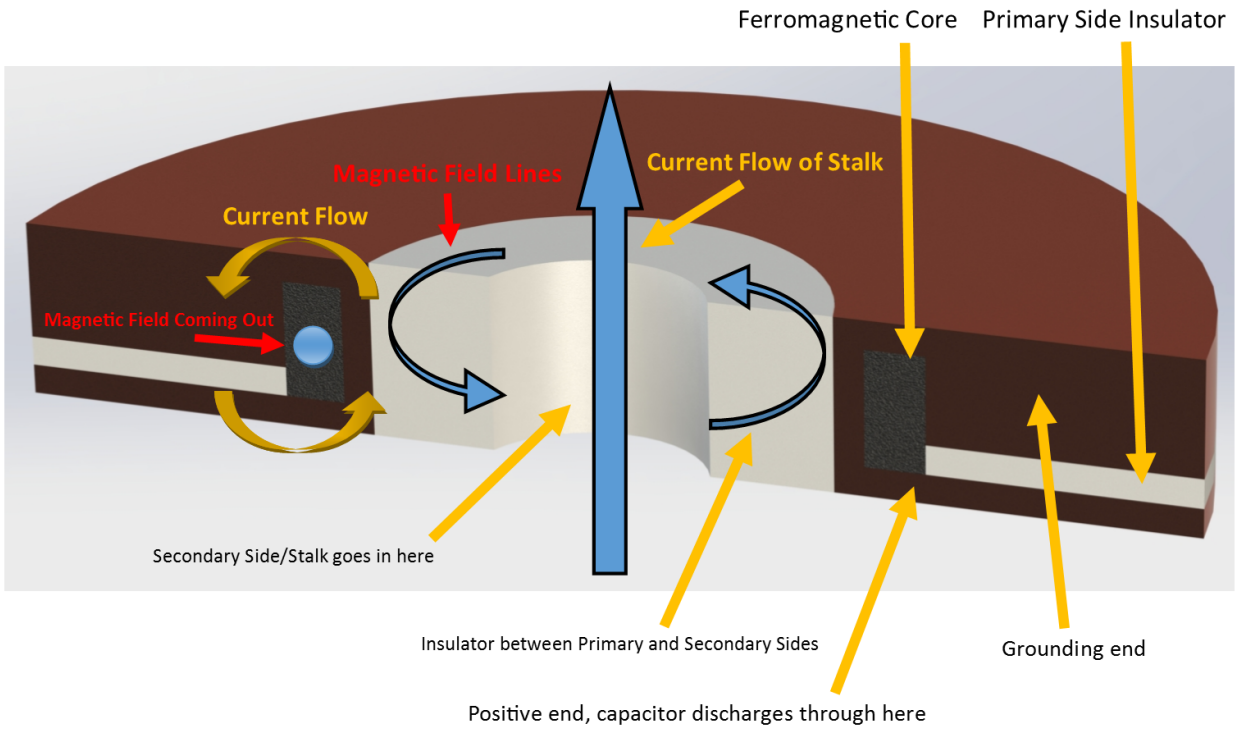


Figure 2.1: Cross-sectional cut view of the physics in a single LTD stage

From the graphic, a LTD stage is surrounded radially by switches. These can be gas switches or solid-state switches. Each switch is connected with its own capacitor charged up to the voltage that LTD stage is rated for. Then, the switches are closed and current runs poloidally around a ferromagnetic core that is in the shape of a toroid. This toroid is going around a center electrode. In LTD terminology, this center electrode is called the stalk. For directly sending energy to another device, it can be a long metal rod. It could also be a hollow

cylinder that holds a vacuum to send electrons through. Regardless, the magnetic field forms radially around the stalk. Using Biot-Savart's law, it is then known that the induced current runs perpendicular to the curl of the magnetic field. In this case, along the length of the stalk. The direction in which this induced current goes is determined by which side of the LTD stage the current enters. Notice from the graphic that there are no coils. This is because LTDs are a 1:1 turn-ratio. Voltage is isolated in this configuration, however the current the stalk experiences is also the current that the switches surrounding the LTD stage experience. Since all the switches surrounding the LTD stage are in parallel, the number of switches needed is the total output current divided by the current rating of each switch or $N_{switches} = \frac{I_{out}}{I_{switch}}$. [19]

To zoom out how the induced current affects the resulting voltage in a LTD system, another graphic is included in Figure 2.2 below.

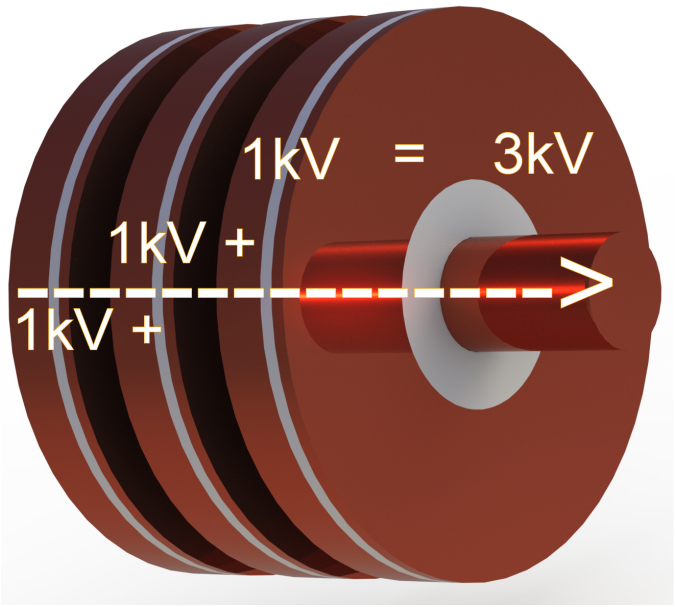


Figure 2.2: Multiple LTD stages stacked to show the effects of voltage adding

Each stage will in theory add their voltage to the resulting output voltage of the entire LTD. The resulting voltage can be the number of stages multiplied by the voltage of each stage or $V_{out} = N_{stage}\ V_{stage}$. [17] Realistically, there are losses that come from the magnetic core

being used, materials surrounding the core, and switching losses. Thus, additional stages should be added to compensate for the losses.

2.1.2 Defining the LTD

To fully define what exactly a LTD is, a helpful graphic is shown in Figure 2.3 below comparing LTDs to two other types of inductive adders.

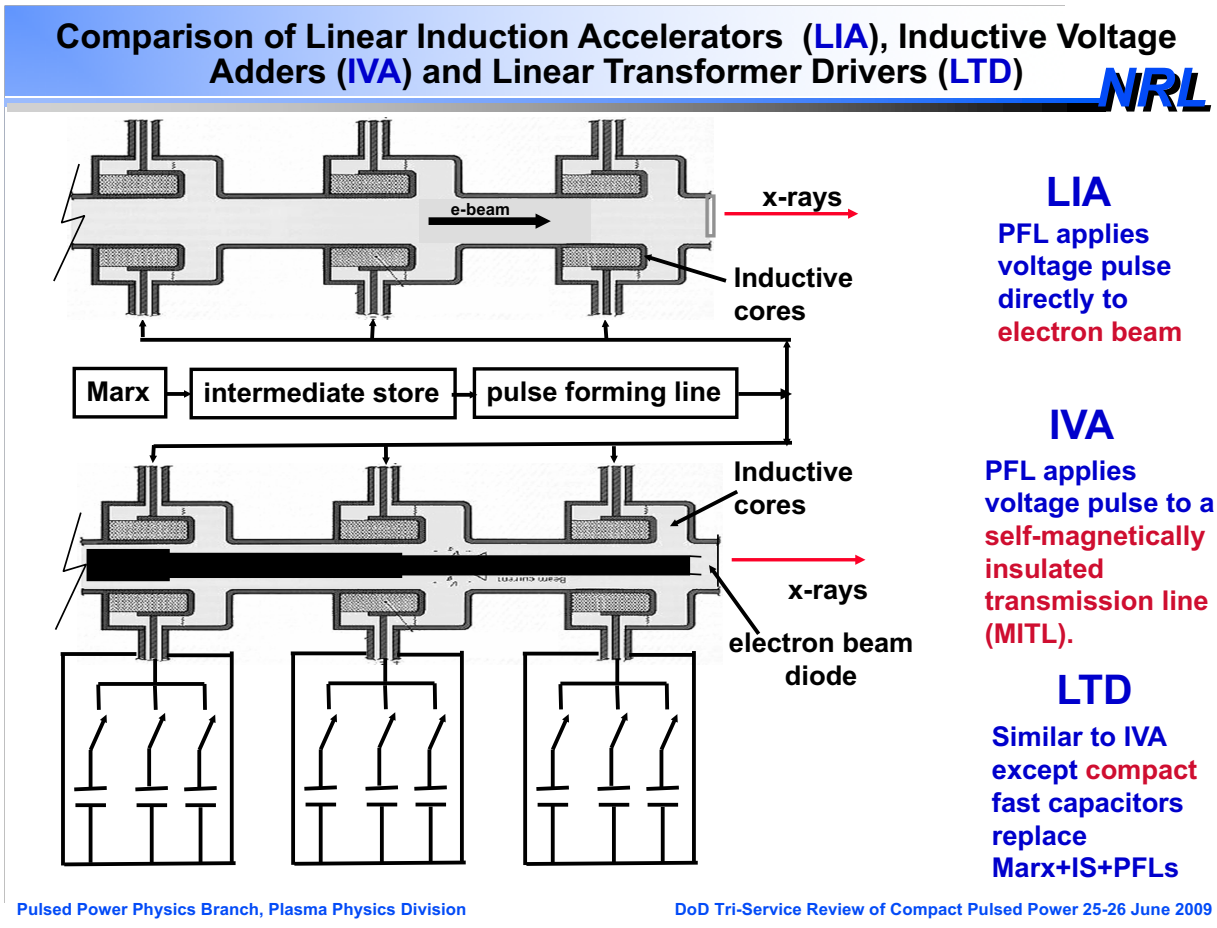


Figure 2.3: Comparison chart of LIA, IVA, and LTD. Image from Cooperstein. Made in June 2009. [24]

The first graphic on the top of the chart shows a linear induction accelerator (LIA) config-

uration. A Marx generator or a pulse forming line (PFL) sends a pulse into each individual stage of the LIA. This energy is then applied directly to an electron beam that is going axially down the stages.

The next graphic on the bottom of the chart is for both inductive voltage adders (IVAs) and LTDs. This is where the definitions can get blurred after a review of multiple LTD papers. There are some authors who argue a LTD is not a good definition because of the 1:1 transformer ratio. It is not transforming any voltage, but it can be argued that the transformer effect is still occurring due to the voltage isolation. According to this chart that has been given recognition amongst the professionals in the pulsed power community, there is a major difference between the operation of IVAs and LTDs. In an IVA, a Marx generator or pulse forming line can still be used and are auxiliary to the transformer stages, just like with LIA. However, unlike the LIA, the IVA sends the pulse into a self-magnetically insulated transmission line (MITL). The LTD does exactly what the IVA does, except that the pulsed power supply is not auxiliary, but surrounding the MITL in each stage. This makes LTDs compact, and replaces the need for Marx generators, intermediate storage, and pulse forming lines. [24]

2.2 Solid-State Technology Review

As stated in the introduction, an overview of the available solid-state switches are needed to have a firm understanding of the content in this thesis. I would like to note that there are numerous solid-state devices in existence. In this thesis, only the solid-state devices that have been thoroughly research (numerous academic publications and company white papers), easy to get in stock from commercial vendors, and can be viable for a LTD device to support the MSX are brought up.

This section is a brief overview of the following solid-state technologies: Power Metal-Oxide

Semiconductor Field-Effect Transistor (PMOSFET), Silicon Carbide MOSFET (SiC MOSFET), Gallium Nitride MOSFET (GaN MOSFET), Gallium Arsenide MOSFET (GaAs MOSFET), Insulated-Gate Bipolar Transistor (IGBT), Pressed-Packed IGBT (PPIGBT), and finally the Silicon-Controlled Rectifier (SCR).

Another type of solid-state switch, called the bipolar-junction transistor (BJT) will not be discussed in this thesis due to its use in current amplification. In comparison, MOSFETs are excellent in voltage amplification. Voltage amplification is needed for my specific LTD application in order to reach 30kV, and MOSFETs are capable enough to supply 500A when in parallel. Some MOSFETs can provide 500A in series, but drawbacks occur in both lower voltage output and slower rise time.

2.2.1 PMOSFET

The power MOSFET is the same structure as a typical MOSFET, with the difference being that the power MOSFET can operate at higher voltages and currents. These devices can operate in the sub-nanosecond regime as well.

In Figure 2.4 below, the internal structure of a MOSFET is shown.

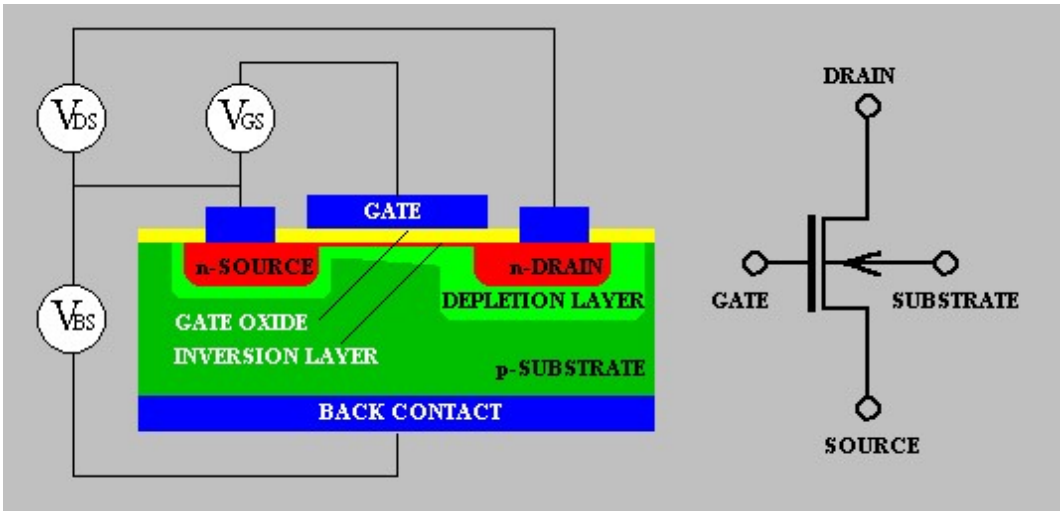


Figure 2.4: Internal structure of a MOSFET. Image from B. Zeghbroeck. Made in 1997. [62]

As can be seen in the figure, there are three pins: gate, drain, and source. When a voltage is applied to the gate, it creates a current path between the n-drain and n-source pins. This current path is known as the inversion layer. What is unique about the MOSFET versus the BJT is that it requires no current to operate at the gate.

There are two types of MOSFETs, n-type and p-type. For the purpose of the LTD I designed, I am using n-type since the MOSFET will have its source tied to ground. In p-type, the source is tied to the positive rail-voltage. Operating a p-type MOSFET requires additional switching circuitry to operate. The two types can either operate in enhancement-mode or depletion-mode. MOSFETs are commonly used in enhancement-mode where if no voltage is applied to the gate-source, there is no conduction between the drain-source. For depletion-mode, the MOSFET is normally conducting between the drain-source when no gate-source voltage is applied.

Hybrid-Pi Model and the Miller Effect

While on the topic about the fundamentals behind power MOSFETs, it is worth bringing up the hybrid-pi model. In Figure 2.5 below, a hybrid-pi model at high-frequencies is shown.

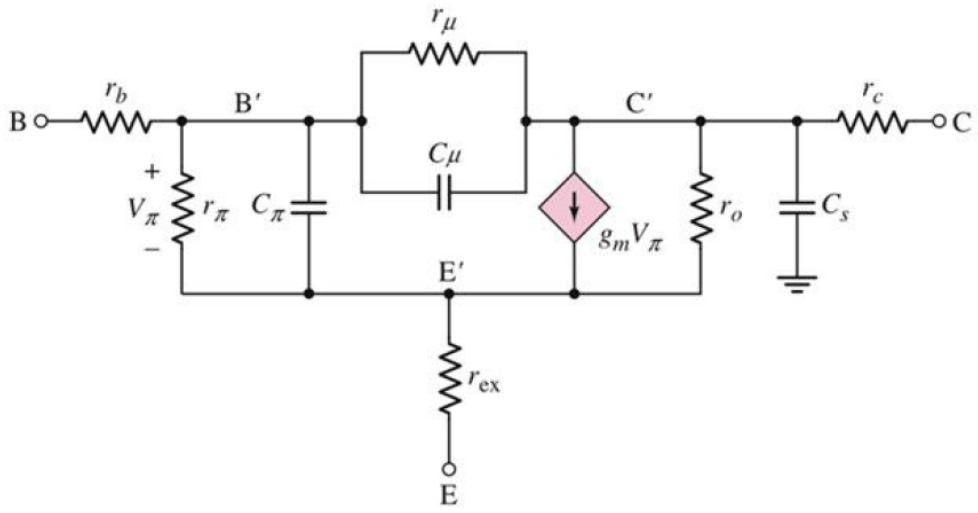


Figure 2.5: Hybrid-Pi model. Image from M. Agah. Made in October 2016. [14]

This hybrid-pi model is useful for both MOSFETs and BJTs. In the MOSFET case, the r_π resistor is removed to model the flow of no current between gate and source. Also, where it has B, is G for gate. Where it has E is S for source. Finally, where it has C is D for drain. The only symbols not seen in this model are inductance values that can model the inductance of the MOSFET pin leads. [14]

The hybrid-pi model is crucial when needing to understand the frequency response of the switch under test. In order to simplify the model, the Miller effect can be used to move the Cu value from gate-drain to gate-source and drain-source. The Miller effect states that $C1 = Cu \times (1 - Av)$ and $C2 = Cu \times (1 - \frac{1}{Av})$. It can be assumed that Av or gain is going to be much greater than one. This now simplifies the effect to $C1 = -Cu * Av$ and $C2 = Cu$. C1 in this case is not really negative, simply take the magnitude of the

value calculated. Understanding how the Miller effect works is important in understanding where the capacitance values come from in datasheets. Fortunately, there is no need to calculate the Miller effect as usually input capacitance and the output capacitances are given. [14]

Parasitic Oscillations

Now that the Miller effect has been brought up, it can be understood that all solid-state switches can exhibit a phenomena called parasitic oscillation at high frequencies. This is unavoidable for the LTD application since pulses are usually square waves. The Fourier-series of a square wave is made up of numerous harmonic frequencies that go across a wide-spectrum. This means that the resonant frequency has a high possibility of being hit by a square wave pulse. The RLC resonance frequency is $f_r = \frac{1}{2 \times \pi \times \sqrt{LC}}$. [59] Both the inductance and the capacitance going into the gate of a MOSFET can create a parasitic oscillation that can affect switching performance. This resonance can be easily seen by using an oscilloscope at the gate. By finding the resonant frequency, one could then find a suitable method in eliminating the frequency. In terms of fast switching MOSFETs, it is not feasible to use a large gate resistance to dampen the resonance. Instead, a device called a ferrite bead can eliminate the specified frequency, while passing through all other frequencies. Think of a ferrite bead as a frequency-dependent resistor. [29]

Having knowledge about the Miller effect and parasitic oscillations are pertinent for each solid-state switch being described in this section.

2.2.2 SiC MOSFET

The SiC MOSFET operates exactly like the power MOSFET, except it now also contains a silicon carbide substrate layer. This material exhibits a stronger voltage standoff, while

maintaining the properties of a normal MOSFET. This solid-state switch can operate in sub-nanosecond pulses as well, while providing voltages over 1.7kV.

The internal structure of a SiC MOSFET is discussed here. It will be explained in a later chapter about the specific SiC MOSFET I am using for the LTD application. It is of note that the best SiC MOSFET package is a 7L DPAK where the SiC MOSFET is in a vertical configuration. An example of a vertical SiC MOSFET structure is shown in Figure 2.6 below.

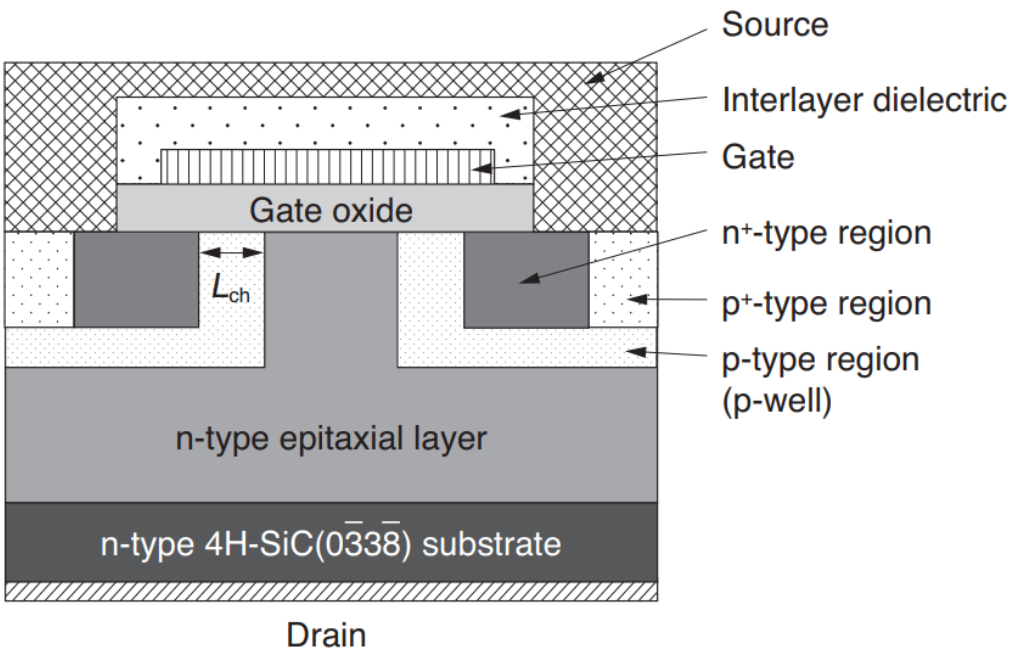


Figure 2.6: Internal structure of a SiC MOSFET. Image from T. Toru Hiyoshi. et al. Made in October 2013. [39]

The figure here for the SiC MOSFET is different from the one described for the power MOSFET, but works the same. In the power MOSFET section, the topology was for a lateral configuration where all pins are on the same side. In the vertical configuration being described here, the n-drain is underneath the p-type layer. The n-source doped regions are both above the p-type layer. It is more common to see vertical MOSFET configurations

when operating at higher voltages.

2.2.3 GaN MOSFET

GaN MOSFETs as with SiC MOSFETs, work the same way as regular MOSFETs. The difference is the additional doping of gallium nitride. This material gives faster switching speed than SiC MOSFET and MOSFETs in general. However, after a review of the commercial market, GaNs are not yet capable of achieving high voltages and currents. However, this does not rule out their use in a LTD, since they could be excellent MOSFET drivers to drive larger gate-source voltages.

In Figure 2.7 below, the internal structure of a GaN MOSFET is shown. Note, that this internal structure of a GaN MOSFET also contains silicon.

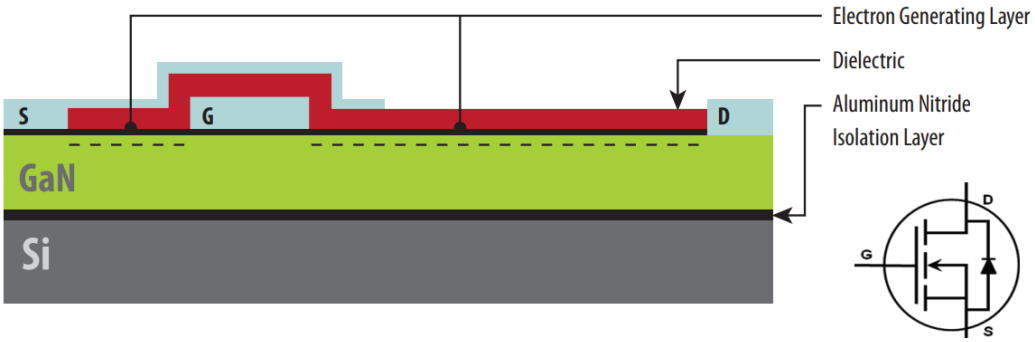


Figure 2.7: Internal structure of a GaN MOSFET. Image from D. Johan Strydom. et al. Made in 2017. [57]

As seen before with the other MOSFET topologies, the gate will open up a conductive channel between the drain and source when voltage is applied. The difference is again with the added gallium nitride layer that provides faster electron mobility.

2.2.4 GaAs MOSFET

GaAs MOSFET operates the same as a normal MOSFET, but unlike all the other ones discussed, it is severely lower in its output power. However, the use of gallium arsenide gives this MOSFET superior switching speeds, into the picoseconds regime. After a search on commercial websites, GaAs is usually not made to drive voltages over 3.3V. This is a common TTL voltage for GHz frequency applications. Despite being 3.3V, the GaAs MOSFET is still an incredibly useful device to amplify low voltage levels in the RF regime.

In Figure 2.8 below, the internal structure of a GaAs MOSFET is shown.

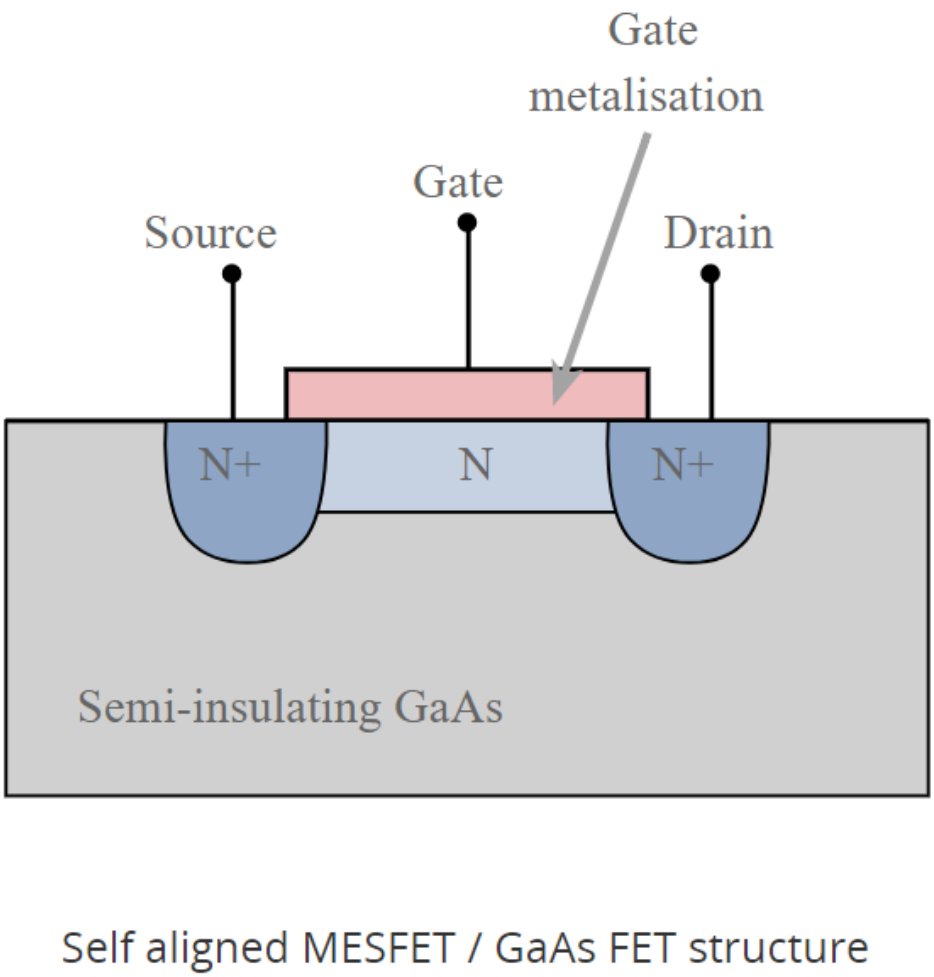


Figure 2.8: Internal structure of a GaAs MOSFET. Image from electronicsnotes website. Made in 2016. [31]

In this figure, the GaAs is acting as the p-layer. Unfortunately, due to the low operating voltage, the GaAs MOSFET could only be used in amplifying a low powered switching pulse sent to a LTD stage in order to turn-on a MOSFET driver.

2.2.5 Insulated-Gate Bipolar Transistor (IGBT)

The IGBT can be thought of as a hybrid between the Bipolar Junction Transistor (BJT) and MOSFET technologies. It is able to sustain high voltage and high currents. Even better, it is able to do this without latching as the SCR does. The only down side is that the minority charges stored inside the IGBT after pulsing a voltage must be removed in order to turn it off. The speed at which they recombine in the IGBT determines the fall time. In terms of their rise times, IGBTs are definitely getting faster over the years, but their commercial rise times are still only around 50ns for their fastest models. This will be seen in the next chapter where a range of switches have been cataloged. For FRC applications, this may not be the best option for me to use when the rise time requirement is under 10ns.

Due to the inherent structure of the IGBT, it will be worth mentioning the history of this device. Unlike MOSFETs that have a type of metal on the gate, and the usual FET architecture underneath, the IGBT can vary with how many layers it has and its architecture. Also, in terms of its operation, the IGBT is both voltage and current activated unlike the MOSFET that only requires voltage. This means when paralleling the IGBT, it is more difficult due to the need to ensure the same exact current reaches each gate at the same time. Otherwise, one IGBT may experience over-current and become damaged before the other IGBTs kick in to support it. This can cause system failure.

From the research done, there are eight generations of the IGBT. Generation eight is technically the Press-Packed IGBT which will be discussed in its own subsection. In 1968, a scientist named Yamagami in Japan invented the concept of the IGBT. In 1978, B.W. Scharf and J.D. Plummer experimentally shown a working IGBT by using a lateral four layer SCR. In 1979, B. Javant Baliga made a vertical IGBT device. In 1980, Hans W. Becke and Carl F. Wheatley made a power MOSFET with an anode region for a patent. This placed into theory an IGBT that has no thyristor action nor any latch-up. In 1983, the

IGBT became commercialized. Generation one of the IGBT was made. This was more of a proof-of-concept since it was prone to latch-up failure. In 1984, A. Nakagawa achieved suppression of parasitic thyristor action and non-latch up IGBT. Thus a little bit later, generation two was designed and greatly improved the latch-up issue. This now gave us the modern IGBT. In 1995, generation three of the IGBT came up and began to rival the switching speeds of present MOSFETs. Its ruggedness was excellent, tolerant of overloads, and included the use of Punch-Through (PT) technology. This included an additional N+ layer in the IGBT. See Figure 2.9 below for internal structure.

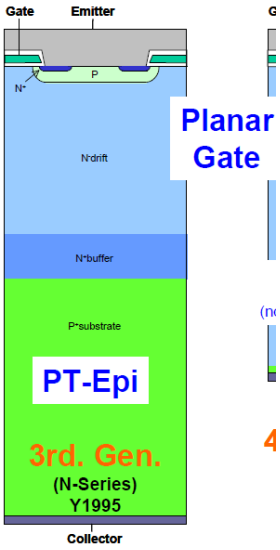


Figure 2.9: Internal structure of a generation three IGBT. Image from eFront runners. Made in 2011. [30]

In 1998, the use of Non-Punch Through (NPT) technology came out in generation four. See Figure 2.10 below for internal structure.

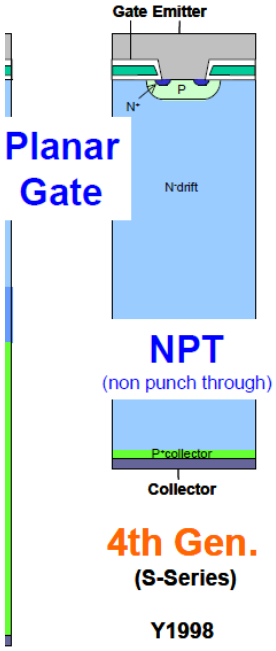


Figure 2.10: Internal structure of a generation four IGBT. Image from A. Gorgerino. Made in July 2012. [38]

There are slight nuances between using PT and NPT IGBTs, where PT helps to accelerate the recombination of minority charges with the additional N+ layer, thus shortens fall time. In 2002, generation five IGBTs began to roll out using a new technology called trench-field stop. The thickness of the IGBT was reduced and the cell-density was increased. However, the voltage coming out of the IGBT was reduced, but current capability was increased in this generation. The trench-field stop expanded the gates down into the N-drift layer. Also, for this generation of IGBTs, the N+ layers surround the outside sides of the gates and the P layer was in between the gates. See Figure 2.11 below for internal structure.

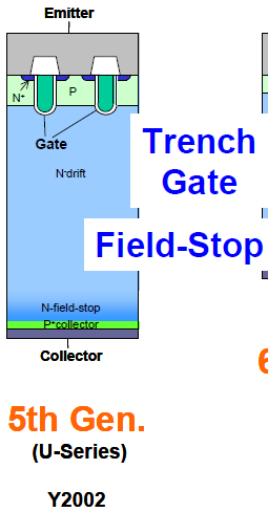


Figure 2.11: Internal structure of a generation five IGBT. Image from A. Gorgerino. Made in July 2012. [38]

Next, in 2007, generation six IGBTs were available using a more advanced trench-field stop technology. The IGBT acted like generation five, but in a smaller package. See Figure 2.12 below for internal structure.

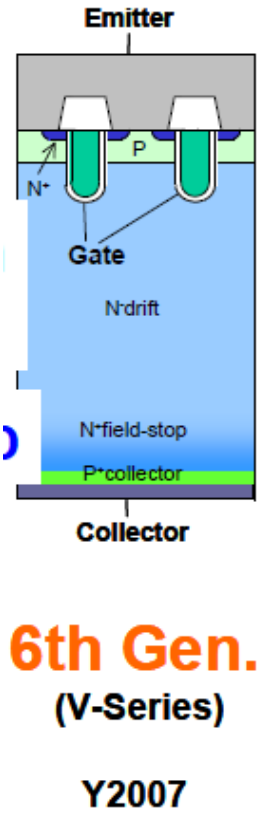


Figure 2.12: Internal structure of a generation six IGBT. Image from A. Gorgerino. Made in July 2012. [38]

In 2012, an even smaller IGBT was available in generation seven. This is where voltage capabilities are becoming significant for IGBTs from generation four, and an increase in current output from generation six. For driving PWM motors, this IGBT also increased their efficiency. See Figure 2.13 below for internal structure.

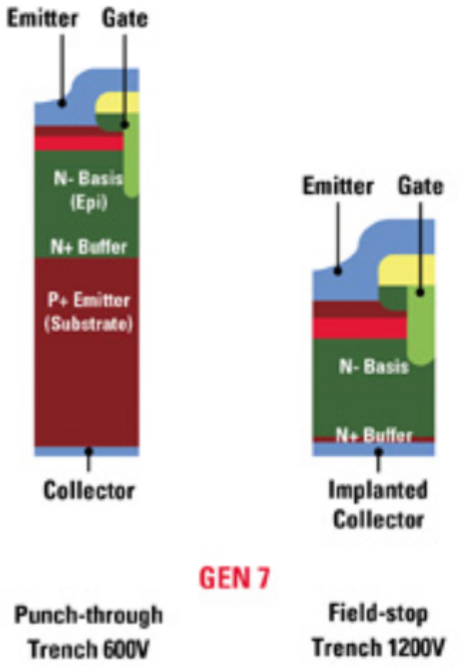


Figure 2.13: Internal structure of a generation seven IGBT. Image from A. Gorgerino. Made in July 2012. [38]

Finally of note are generation eight IGBTs, where IXYS developed hokey-puck sized IGBTs that can handle greatly higher voltages and currents. This will be discussed in the following subsection as their performance is much different from traditional IGBTs.

2.2.6 PPIGBT

The PPIGBT is called pressed-pack for a reason. It uses compression instead of wires to put numerous IGBTs in parallel to avoid much power loss. This gives this switch a superior performance in high voltage and current. In fact, this is the only solid-state switch in the market with the ability to be turned on and off with the highest power output in a compact package. The PPIGBTs from IXYS can have voltages up to 6.5kV and pulsed currents possibly up to 10kA. These solid-state switches do not come cheap as they can go up to $6,500 a unit. The superior output voltages and currents do come at a cost as the rise time

is around one microsecond for present PPIGBTs.

In Figure 2.14 below, the internal structure of a PPIGBT is shown.

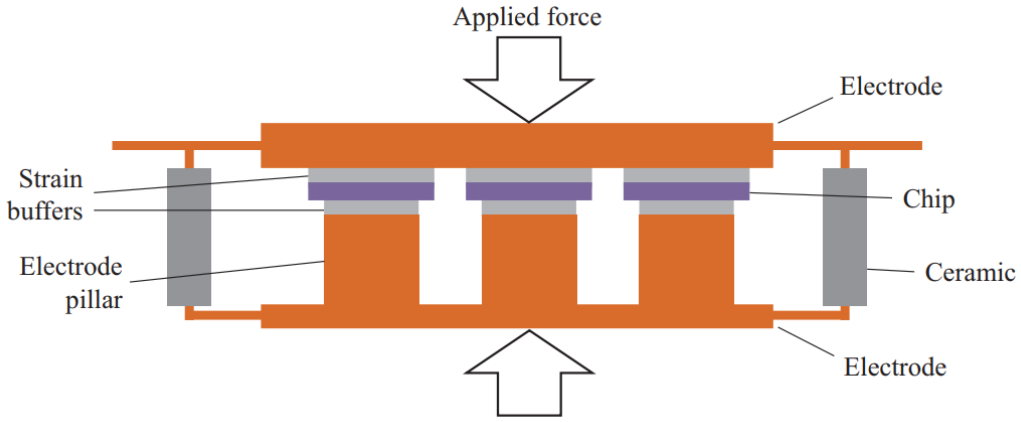


Figure 2.14: Internal structure of a PPIGBT. Image from A. Robin Simpson. et al. Made in September 2017. [56]

The PPIGBT uses the IGBT topology for each of its individual chips, however this method puts a number of them in parallel to increase their power output. It can be seen in the figure that compression is used to keep the chips secure, and a strain buffer is used to prevent the chips from breaking. A ceramic is used as an insulator around the package.

2.2.7 SCR

The SCR can also be known as a thyristor; both are solid-state switches. A gas switch equivalent is known as a thyratron. All these switches have high voltage and current outputs, but cannot be turned off until the running current is back to zero. This makes the SCR not preferable in a LTD application that needs to have a controlled output pulse, but for applications that need much higher power than I am designing may consider their use.

In Figure 2.15 below, the internal structure of a SCR is shown.

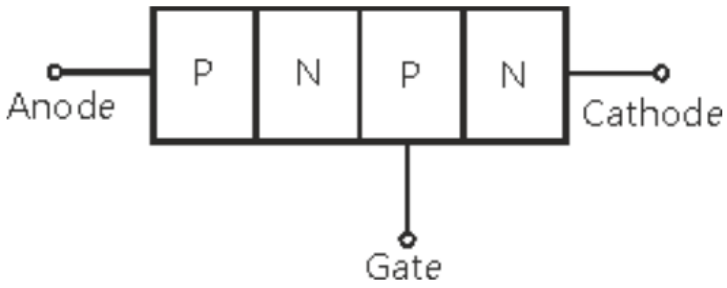


Figure 2.15: Internal structure of a SCR. Image from I. Poole. Made in 2018. [54]

The SCR contains four doping layers, P-N-P-N. By applying a voltage to the p-layer, a conductive passage is made between the anode and cathode. However, as can be seen, there is no way to remove charges that are inserted into the p-layer once current is running.

In Figure 2.16 below, the internal structure of a SCR in a semiconductor format is shown.

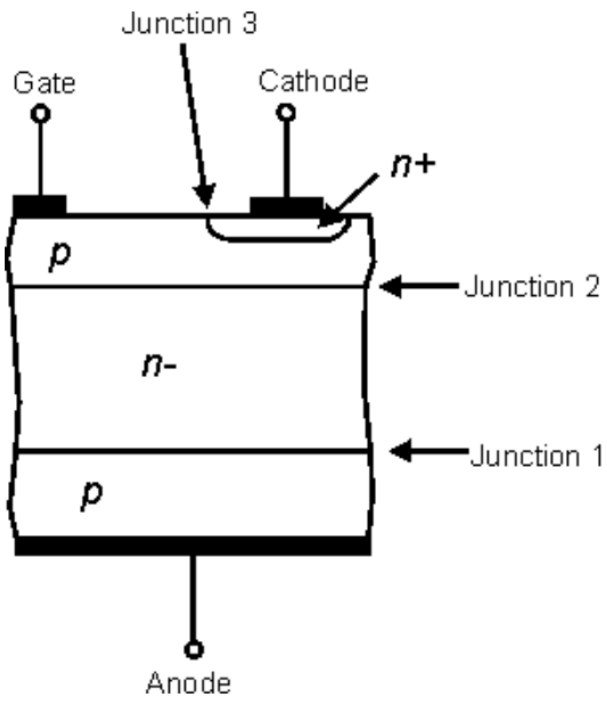


Figure 2.16: Internal structure of a SCR in a semiconductor format. Image from I. Poole. Made in 2018. [54]

As with the previous figure, this version of a SCR also contains the four doping layers.

Overall, SCRs are high-powered devices, but their lack of turn-off control makes them unsuitable for my specific LTD application. They are viable in applications that already use gas switches and need a solid-state equivalent and should not be discounted for future LTD use.

2.3 Spark Gap Switch Review

Spark gap switches are a form of thyratrons. Their fundamentals are simple, but their control systems can become fairly complex. A spark gap consists of two parallel metal plates,

where they are separated by an air gap. This gap is filled with a dielectric gas to a needed pressure in order to create a standoff between the anode and the cathode plates. Usually, an ignition switch creates a spark in the dielectric filled gas to create a conductive channel between the plates. As soon as this happens, the spark gap will run the current till it is out. There is no way to turn off a spark gap, however these switches have the highest power output of any type available.

An example of a spark gap switch can be seen in Figure 2.17 below.

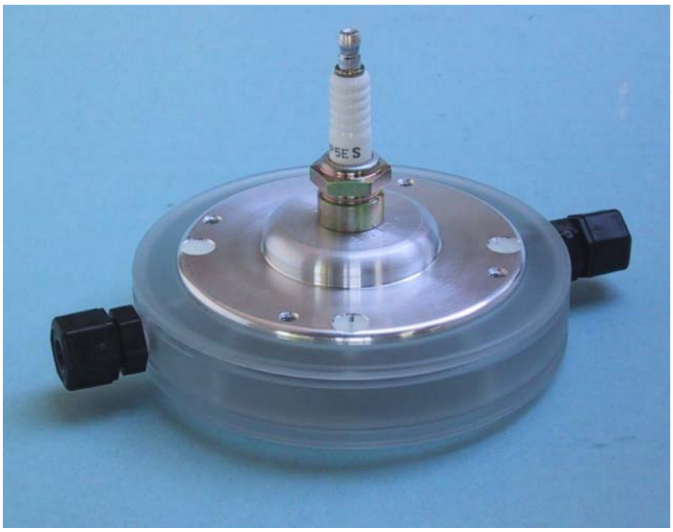


Figure 2.17: Example photo of a spark gap switch. Image from R.E. Beverly III and Associates. Made in December 2017. [10]

There are disadvantages with spark gaps compared to solid-state switches. First, there must be a running supply of pressurized gas to keep them running. Second, the use of a gas discharge also means spark gaps will degrade over time and must be taken out of operation for maintenance. Third, they are not as small as solid-state switches. Due to the plasma discharge in the gap, they cannot achieve the low amount jitter solid-state can provide, and their rise time would not be as good as a solid-state. This also makes modeling a spark gap more complex as well. However disadvantages aside, spark gap switches are cheap for the

amount of power they can supply.

There are multiple ways to ignite the gas in a spark gap. Besides the usual method in using a trigatron or ignition switch, one can also use the following: passive, field-distortion, laser, and surface discharge. [10]

2.4 Pulsed Power Transformer Fundamentals

The transformer core in a LTD operates a bit differently from a conventional transformer core. The most noticeable difference is that the H-field does not affect a pulsed power core, rather the volt-second rating is what matters. The volt-second rating stems from the B-field of a transformer's B-H curve. This section will walk through in detail about the differences between the LTD transformer core and conventional transformer cores, along with the different parameters that affect a LTD core's performance, and a brief look into whether an air core would be useful for my LTD design.

2.4.1 Conventional Transformer Model

The conventional transformer relates closely with pulsed power transformers. In terms of LTDs, there is a difference in terms of the stacking effect that LTDs have on the output voltage, but nevertheless, they contain the same basic building blocks as conventional transformers. There are a few discrepancies to point out, these being: the frequency response of a pulsed power signal versus a constant sinusoidal frequency power signal, hysteresis effects, temperature effects, and physical core manufacturing effects. [22] The conventional transformer model can be seen in Figure 2.18.

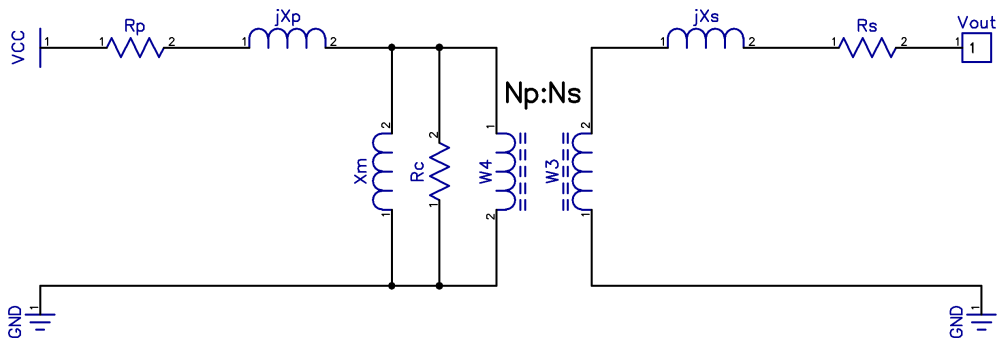


Figure 2.18: Schematic diagram of transformer model

A conventional transformer has reactive components Xp, Xs, and Xm. At a constant single frequency, there is a single value for all the reactive components. [22] However, in pulsed power, it is a Fourier series of different sinusoidal frequencies that go through the transformer. This makes approximating the resistance much harder. However, in the LTD method, the 1:1 turn-ratio helps to eliminate a little bit of the complexity of a conventional transformer model by removing the coils. The secondary load impedance can then be reflected over to the primary without any changes. [17]

LTD Transformer Model

The LTD takes advantage of the voltage isolation between transformers to stack up the voltage on the secondary end. To model this, the transformer windings can be removed. In a Department of Energy paper, all these secondary impedances and the primary inductances can be used to determine the load impedance that best matches the source impedance. [63] This explanation however, does not contribute to a detailed LTD transformer model and will not be covered in this thesis. Nevertheless, it is good to know that there is a simple formula for calculating a matching load impedance.

The hardest term to model for a pulsed power transformer is the Rc element. The Rc element

is modeled by a resistor and represents eddy current losses and heat losses in a transformer core. While hysteresis curves are available for all cores, manufacturers do not test their cores at the levels cutting-edge research may use them for. For example, manufacturers typically display BH curves conducted at single hertz to kilohertz frequencies. The frequencies that present research in pulsed power cores to generate high energy are in the order of 100s of MHz. Thus, conventional BH curves makes it tricky to estimate how the output pulse fairs as it goes through the transformer. For conventional transformer applications, the typical 60Hz frequency being used are in the datasheets of these cores. It is then possible to use the calculated current coming through the primary winding to get an H-field. This can then be used to determine the B-field from the BH curve. The total area of the BH curve can then be calculated to determine core losses. However, this is not the case for nanosecond rise time pulsed power applications such as used in the LTD. One work-around would be to model the entire LTD, and do a sweep of the Rc value to determine the sensitivity the transformer has with varying hysteresis, frequency, and temperature losses. This can help when selecting cores that are similar to each other. [21] An example LTSpice model and Rc sensitivity analysis is included in Figure 2.19 below for one stage of a LTD.

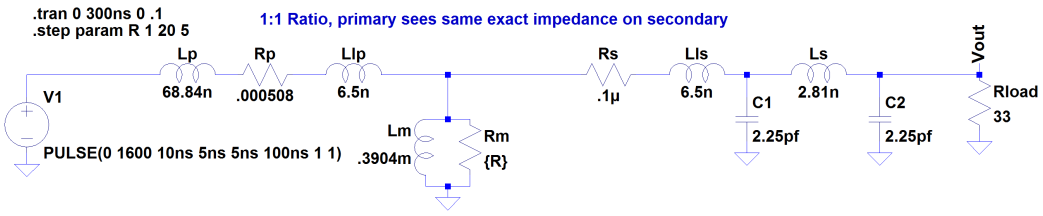


Figure 2.19: LTSpice model for conducting Rc sensitivity analysis

This figure above uses the LTD transformer model and contains a variable resistor Rc to program varying levels of resistance. The changes in Rc are determined through trial and error. By figuring out the Rc range of values that cause varying pulse shapes to occur, one can then focus the sensitivity analysis around those values of Rc to have a reasonable number of waveforms to compare on a single plot. This plot can be seen in Figure 2.20 below.

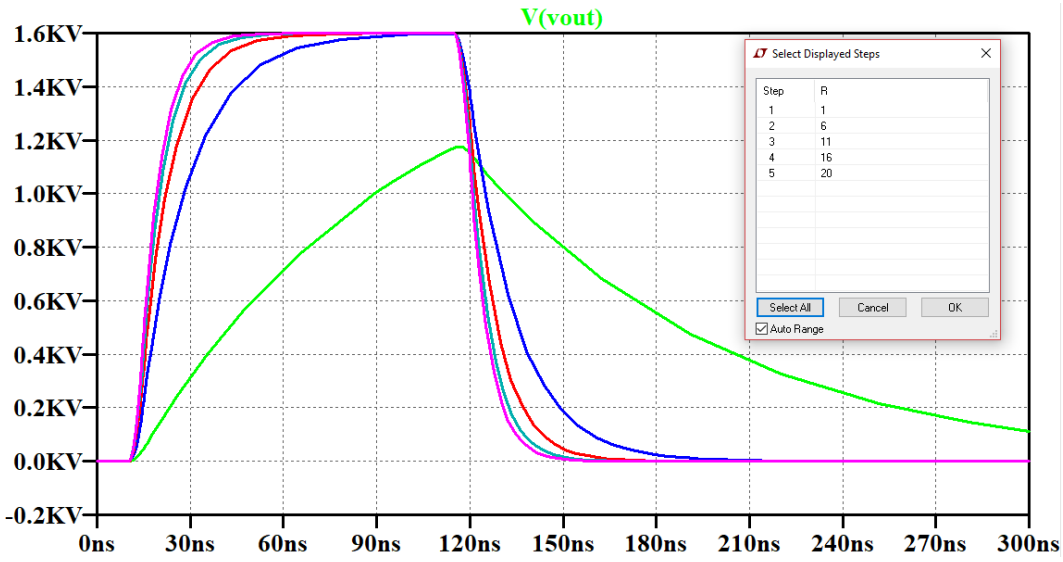


Figure 2.20: Output waveforms generated using varying values of Rc

As can be noted from the figure above, this analysis is useful for determining the threshold where small changes in Rc can have a major effect on the pulse's output.

Another work-around in estimating Rc is mentioned in a Physical Review Special Topics - Accelerators and Beams paper. [47] Knowing that the amount of eddy currents generated causes Rc, the skin depth will play a role in getting the Rc value. Keep in mind, this Rc value is dynamic due to the changing frequencies going through the core. However, in the paper, they mentioned that the static hysteresis curve and the voltage pulse are rectangular for the purposes of calculating Rc. This then implies that $\frac{dB}{dt}$ is nearly constant throughout the transformer core. The equation is then $R_c = k * \frac{pS}{\delta^2 * l}$. The specific resistance of the core or p will play a part in this formula. The constant S is the total cross sectional area of the material in the core. The next constant l is the total length of the core or the circumference for a toroidal core. Finally, δ is the thickness of the core's lamination. k is the dimensionless coefficient for this case is either 8 or 12. These are values found from two others papers mentioned in this source.

To complete the LTD model from the conventional transformer model, parasitic capacitance needs to be added onto the secondary end of the transformer. This is because the secondary rod acts as a transmission line, and especially at high frequencies, any small amount of capacitance can have an effect on the pulse. Also, the skin-effect will cause varying inductances and resistances that will be experienced at each frequency. The most important frequency to model will be the rise time frequency for the LTD case. Optimizing the design for this frequency, will mean that the other frequencies will pass through easier, however keep in mind that the frequency of the main pulse length will need to travel through a thicker piece of metal. It is ideal to make the piece of metal that the pulse is going through optically-flat in order to mitigate attenuation of the signal since even a 100ns pulse length will only penetrate a few micrometers into a conductor. All of this can be modeled into the Rc, Rp, Rs, Lp, Lstalk, Llp, Lls, Lm, Cstalk, and Rload impedances, with most of these values coming from the conventional transformer model, which can be seen in Figure 2.21.

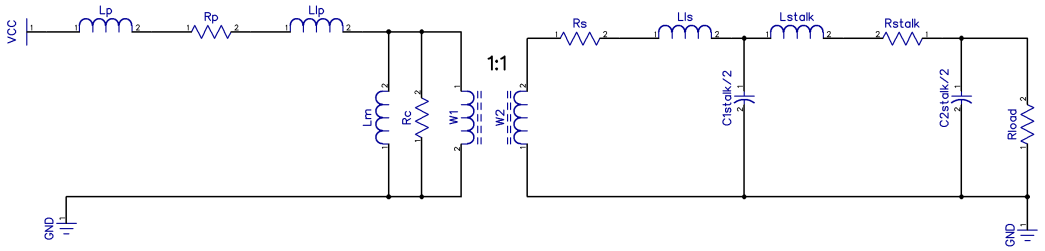


Figure 2.21: Schematic diagram of pulse transformer model

From the model, the circuit elements are: Rc being the core losses, Rp being the primary resistance, Rs being the secondary resistance, Lp being the primary inductance, Lstalk being the secondary inductance, Llp being the primary leakage inductance, Lls being the secondary inductance, Lm being the core magnetizing inductance, Cstalk being the secondary capacitance, and Rload being the resistance of the load.

2.4.2 Considerations When Choosing a Pulsed Power Transformer Core

When looking for a pulsed power transformer core, these areas should be considered: the permeability of the core, its maximum magnetic field swing, the manufacturing process used to make the core, its frequency considerations, and finally its temperature considerations. These are important because it is critical to optimize the integrity of the pulse, and little details such as the processing of the core may not be as important in conventional transformers.

Permeability

To start off, the permeability of the core needs to be able to handle the frequencies of a pulse. If using a normal iron ferrite core, the relative permeability will be about $5,000$. For this iron ferrite core, at high frequencies into the hundreds of megahertz range, its permeability will drop. The squareness ratio is the ratio of the remnant flux density over the magnetic flux density at the magnetic field of one Oersted or for this case 79.58 amperes per meter. This can be seen as $\frac{B_r}{B_1}$. For the best high frequency response, it is ideal to have to have a ratio value as close to one as possible. This is because after the field strength decreases, the magnetic field is still engaged and will continue supplying the pulse to the secondary. The squareness ratio also becomes affected in some core materials due to the geometry of a core. [61] Metglas, a state-of-the-art amorphous metal alloy can be affected if the inner diameter is too small. A smaller inner diameter can cause a drop in remnant flux density, which in turn drops the squareness ratio. Also of note, having a better frequency response will also result in a better core resistance. For the purpose of LTDs, the frequency response affects the efficiency of the transformer only. According to Dr. Jiang, the rise time is not necessarily affected by the transformer core. [43]

Maximum Magnetic Field Swing

Second, the maximum magnetic field swing determines the cross-sectional area size of a core according to Faradays law $V = \frac{-N*\delta B*Ae}{\delta t}$. Modifying this formula it looks like, $Ae = \frac{3 \times V \times \Delta t \times N}{\Delta B \times PF}$. Ae is the cross-sectional area, Δt is the pulse-length, V is the maximum voltage being put through, ΔB is the maximum magnetic field swing, PF is the packing-factor of the core, and three is used as a factor of safety to prevent core saturation. [19] Preferably, the larger the magnetic field that can be used, the smaller and cheaper the core can be. It is worth noting that packing-factor is defined in multiple ways across core manufacturing sites, but it is simply a percentage that defines how much core material and lamination material is used. The higher the packing-factor, the more core material that is available. Typical packing-factor values are around 75 percent.

There is some ambiguity in academia regarding the use of Faraday's law in determining the cross-sectional area of the core. Typical transformer core design requires that the H-field be used to come up with the required B-field, and find the cross-sectional area from there. However, due to a very high frequency operation and a short pulse length, only the saturation level of the B-field is required for the core design from a BH curve. It is understood that the H-field changes drastically as frequency is ramped up, and the coerciveness of the core changes. However, in the academic realm, there are no publicly available papers explaining this physics in detail, and all the LTD papers do not go into any details regarding the H-field. At high frequencies, the H-field can become non-linear and start to show complex attributes, along with the permeability of the core. This can cause the H-field to lag the B-field, and is a possible explanation about why H-fields order of magnitudes higher than what is shown on the BH curve can still be used in a pulsed power core without saturating it. It is of note that the BH curve is frequency depedent. [65]

Manufacturing Process

Next, the manufacturing process of the core can determine the overall structure of the core, and even how well it can dissipate temperature. For doing pulsed power cores, this becomes crucial if trying to make a core as small as possible. Depending on the material, a core may have a limit in how small its thickness can be. It may be possible that a small thickness is possible, but at the cost of additional structural material such as epoxy. [61] This can cause the primary and the secondary windings to be further away from the core itself. This in turn, can affect leakage inductance.

Frequency Response of the Core

Another aspect is the frequency of the core. A good rule of thumb is that the higher the permeability, the better it would be at handling higher frequencies. Unfortunately, manufacturers usually do not have data sheets regarding MHz frequency losses. The engineer would need to test the core to be absolutely sure it meets their specifications. [21] However, optimizing the other parameters as described above can ensure the best possible rise time for a pulsed power transformer.

Temperature Considerations of the Core

After everything has been considered, the temperature requirement of the core can be looked at. If multiple repetitions are needed, there needs to be a way for the core to transfer heat. If the core is fragile and needs to be coated in epoxy to keep it structurally sound, than it would not be useful for high repetition applications where the heat does not have enough time to escape. [61] However, for single pulse applications, as long as eddy currents are kept to a minimum, heat would not be a problem.

Transformer Solid-Core Versus Air-Core

When determining whether a solid-core or an air-core should be used, first look at the pulse length of the application. The voltage-second restraint of a core should be considered. If the application requires a time scale that is higher than the voltage-second rating of a core material, than it will need to be used in an air-core configuration. For a few applications, an air-core may not be the best option, and thus a larger magnetic core should be used. This is due to the mutual flux linkage between cores. [42] If the core geometry, such as in a Linear Transformer Driver is inherently low in leakage flux, than an air core could be a viable option for specific applications. The magnetic operation of a single stage inside a Linear Transformer Driver can be seen in Figure 2.1.

Figure 2.1 shows that the current is poloidal around the magnetic core, which in turn induces a field that is radially circulating around the secondary rod or the stalk. Current is then induced into the stalk through the Biot-Savart law, and the direction determined by the right hand rule and Lenzs law. The Biot-Savart law states that the magnetic field is $B = \frac{u_0 * i}{2 * \pi * r}$. [35] Maxwell-Faraday equation using Faradays law of induction shows that in integral form $\oint\limits_{\partial \sum} E \cdot \mathrm{d}l \ = \ - \frac{d}{dt} \iint\limits_{\sum} B \cdot \mathrm{d}S$ and in differential form $\nabla \ X \ \mathrm{E} \ = \ - \frac{\delta B}{\delta t}$. [2] These formulas show that the closed voltage induced into the secondary is determined by the change of magnetic field. The strength of the magnetic field does not matter since voltage considers the entire surface area of which the magnetic field goes through. However, this considers that the magnetic field is orthogonal to the surface area of which it passes, and leakage flux may not have its magnetic field orthogonally go through the surface area in which the main magnetic flux runs through. However, to make a point about the efficiency of using an air-core versus a solid-core pulsed power transformer in a LTD configuration, the flux linkage between the primary and secondary windings is relatively strong. Keep in mind that with high frequencies, even a small leakage flux can have an an impact on the rise time of a pulse, and thus one cannot assume a perfect flux linkage is occurring. A good approximation to figure out the efficiency of an air-core transformer is to look at the k-factor. In this case $k = \frac{M}{\sqrt{L_1 L_2}}$and be-

cause the windings can be thought of as being tightly wound on-top of each magnetically the mutual inductance can be approximated as $M = \frac{u_0 u_r N_1 N_2 A}{l}$. Since the LTD is a 1:1 ratio, the self-inductance of both the primary and secondary coils can be thought of as the inductance of a toroid$L1 = \frac{u_0 u_r N_1^2 A}{l}$. Both windings will have differing areas and lengths. [9] For an air core, the inductance is important to get a specified output voltage, where $V = L\frac{di}{dt}$. The rate of change can help induce a higher voltage, but also a higher inductance can help as well.

For a small LTD system, the inductance of the primary and secondary windings may not be large enough to pulse through a desired voltage. However, if the LTD system requires a long-pulse length, and can be larger in size, than an air-core is feasible. Keep in mind, if the inductance in an air-core is not large enough, much higher current must be passed through the switches of a LTD in order to achieve the voltage output level of the transformer. [42] Overall, the size required to operate with an air-core means it will not be a viable option when designing a LTD that needs to be compact.

Chapter 3

Related Work

The LTD is considered new in the realm of the research world, due to a limited number of publications available. This chapter will focus on LTDs that are made and published. An emphasize of this review will be on the solid-state LTD papers. The physics between a gas switch and solid-state switch LTD are the same. The only differences are the rise times and the complications gas switches bring in with their auxiliary systems required to run them.

3.1 Basu 22kV Solid-State LTD

The title of this paper is called "Development of 22kV, 1kHz Rep-Rated Solid-State Pulser Based on Linear Transformer Driver Topology." It was written by S. Basu et. al. The authors wrote the paper at the Accelerator and Pulse Power Division, Bhabha Atomic Research Center in Visakhapatnam, India. This was written in 2008.

Out of a lot of the LTD papers found, this is one of the best papers in putting LTD mechanics in layman's terms. Three engineers, Basu, Sahoo, and Rajawat at the Accelerator Pulse Power Division, Bhabha Atomic Research Centre in Visakhapatnam, India developed a large

LTD using solid-state switches. What is unique about their design is how they utilized easy to access consumer goods and no extra bells and whistles in their design versus the expensive builds that U.S. national laboratories go for.

The authors made useful definitions for the makeup of a LTD. They refer to a gate driver, solid-state switch, and capacitor bundle as a brick. The brick can be seen in Figure 3.1 below.

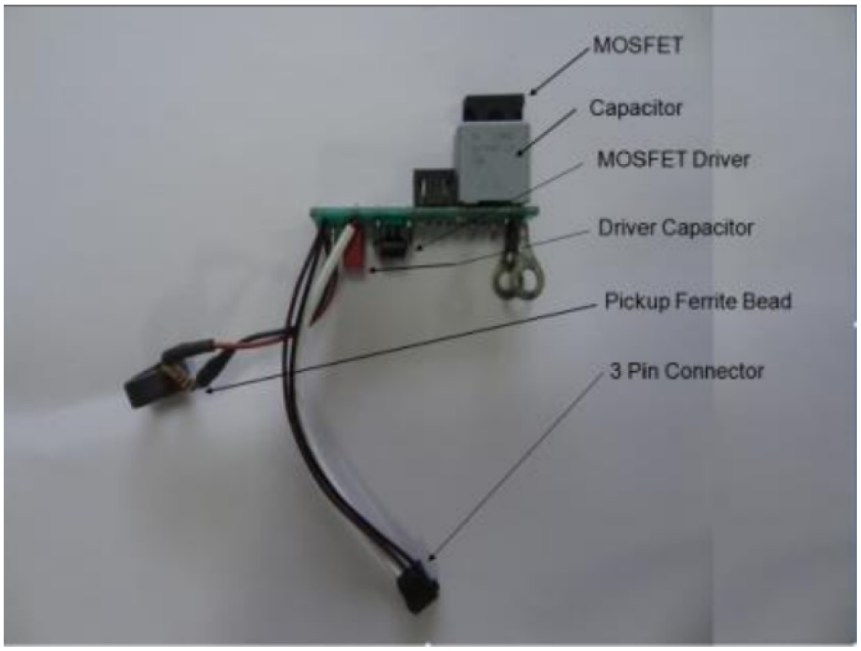


Figure 3.1: Makeup of a brick in the 22kV LTD. Image from S.S. Basu. et al. Made in 2014. [17]

What is nice about the brick designed here is the use of affordable PCB board. As will be discussed in the next sections reviewing other LTDs, a small PCB board is a design that can be bought for a few dollars versus the large custom-made ring PCB designs. However, there is a drawback as wires must be used to make all of the connections. This is susceptible to noise.

Notice towards the bottom left of Figure 3.1 that the authors made use of a component called a pickup ferrite bead. A wire is passed through the middle of the ferrite bead and provide the logic input to the brick. The authors did not go into further detail about inductive pickup, however it appears the wire going through multiple ferrite beads helps to slow down current entering bricks that have less resistance than other bricks, thus helping to equalize the impedance amongst the bricks. Another graphic from the paper is shown in Figure 3.2 below showing a full stage of their LTD.

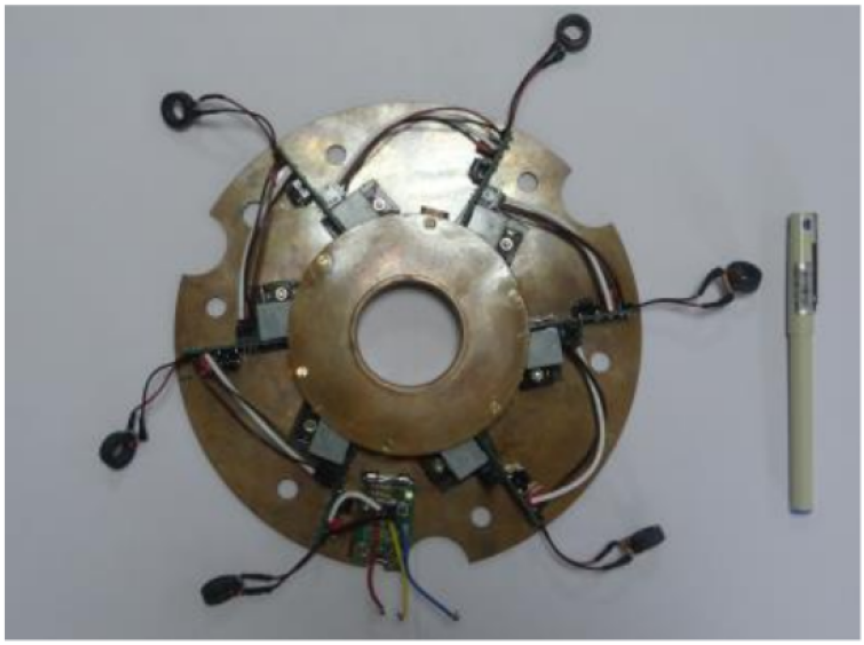


Figure 3.2: Makeup of a stage in the 22kV LTD. Image from S.S. Basu. et al. Made in 2014. [17]

It is easier to see now that a wire running inside all the ferrite beads can provide a cheap and reliable logic input to the bricks. In Figure 3.3 below, the author shows the make-up of a single module stacking five stages.

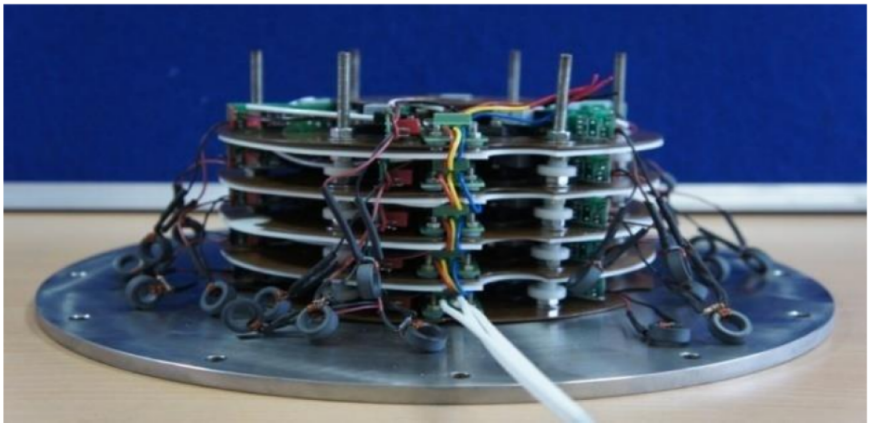


Figure 3.3: Makeup of a module in the 22kV LTD. Image from S.S. Basu. et al. Made in 2014. [17]

It is apparent that the module makes use of a single side to supply all the power inputs to the stages. The ferrite beads are arranged in such a way that they all are laying at the same height around the module. This makes it easier to insert a logic wire. These modules are then stacked to make a total of forty stages in the authors' LTD. This can be seen in Figure 3.4 below.

Figure 3.4: Makeup of the 22kV LTD. Image from S.S. Basu. et al. Made in 2014. [17]

It can be seen at the input side of the LTD that there are power cables and logic boards. The boards are utilized at each module. Looking closer, there are fiber optic cables going to each of these modules to provide a logic input from a control unit. It is unknown from the paper how the fiber pulse is made. This is important considering using multiple fiber optic transmitters could cause additional jitter versus a pulse that is split from a central transmitter. The authors modeled their LTD with the following schematic seen in Figure 3.5 below.

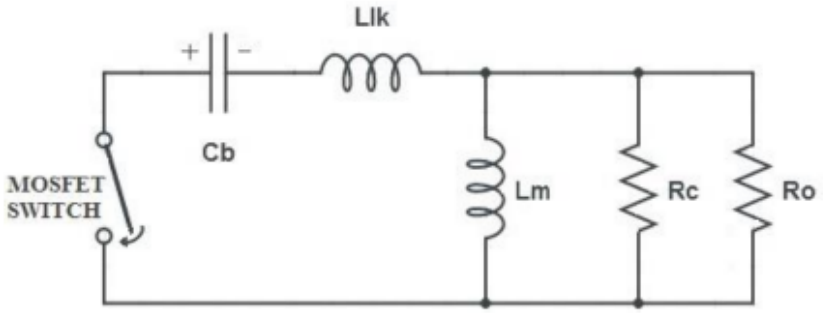


Figure 3.5: LTD circuit model. Image from S.S. Basu. et al. Made in 2014. [17]

This is a fairly simple model, and for the purposes of the LTD I designed, not sufficient for considering all LTD parameters. However, it is a simple model that can get a designer in the ballpark of their LTD output. In terms of the pulse shape after triggering the MOSFETs, the LTD output can be seen in Figure 3.6 below.

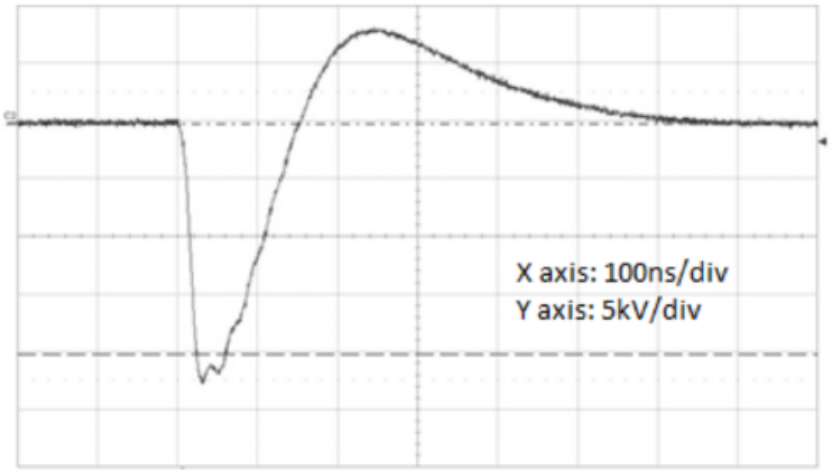


Figure 3.6: 100 ohm load at a 22kV output. Image from S.S. Basu. et al. Made in 2014. [17]

The output shows a fairly intact pulse from the LTD with a little bit of oscillation at the falling edge. For the parts used in the design of this LTD, this is an excellent response. However, the rise time of this LTD longer than 10ns. Some inspiration can come from this

design, but other LTDs must be referenced in order to come up with a LTD that can perform at under 10ns rise time.

The authors did provide information about the jitter performance of their LTD. This can be seen in Figure 3.7 below.

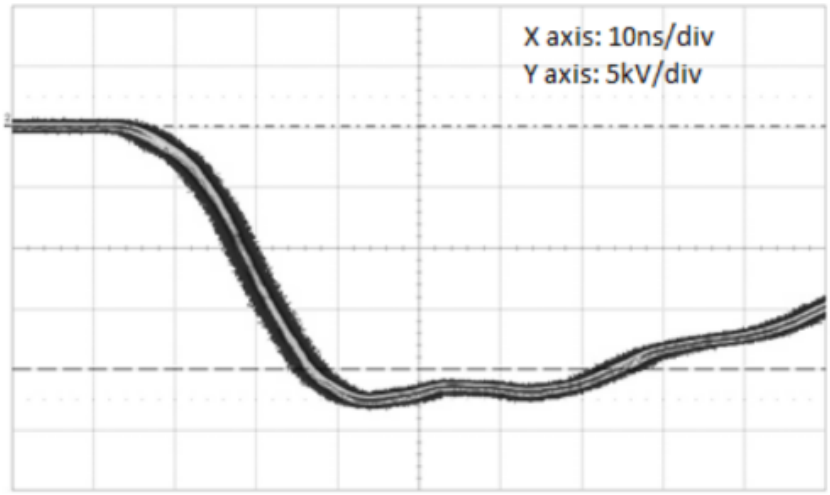


Figure 3.7: Temporal jitter is 5ns at 22kV output. Image from S.S. Basu. et al. Made in 2014. [17]

Using cheap PCB boards and long wires across the LTD stages, the 5ns jitter seen in this pulse output is good. This is promising as making a LTD with better switching performance, board design, and a more precise logic input can get me down to my goal of <1ns jitter.

Overall, the performance of this 22kV LTD is remarkable considering the use of individually packaged bricks and multiple optic fiber inputs going into the LTD. As a baseline, it is looking promising to achieve a rise time of less than 10ns and a <1ns jitter without needing much more specialized circuitry.

3.2 LLE-LLNL 10kV Solid-State LTD

The title of this paper is "A Solid-State, Inductive-Adder, 10-kV Pulse Generator for Driving Large-Aperture Pockels Cells." It was written by Wade Bittle. He wrote this paper at the Laboratory for Laser Energetics in Rochester, New York. This LTD was built for the Large-Aperture Pockel Cells at Lawrence Livermore National Laboratory. This was written in 2012.

In an overall summary, this paper does a good job in explaining the entire mechanics of the LTD from sending the firing signal to resetting the transformer cores after each pulse. However, while the high-level overview is good, the explanation of the transformer physics is poor. A lot of time was spent trying to decipher where the numbers came from. However, I discuss the useful aspects that can be learned from this paper.

The specifications for this LTD is similar to the one I designed. The authors who wrote this paper also designed for under a less than 10ns rise time and less than 200-ps rms jitter. The only downside however is that their output voltage is 10kV, unlike my specifications that must be at least 30kV. Thus, the parts used in this LTD will most likely not be useful in achieving the same timing specifications with my LTD.

The paper starts out with a high-level topology of a LTD. This topology is consistent with other papers found during the research phase of this thesis. The topology can be seen in Figure 3.8 below.

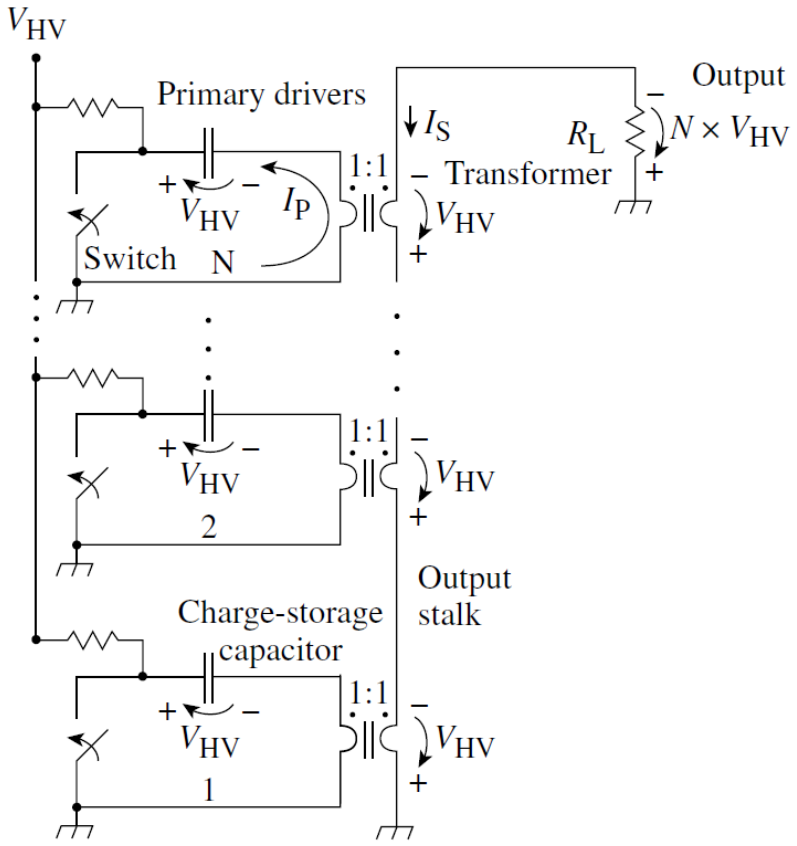


Figure 3.8: High-level LTD topology. Image from W. Bittle. Made in 2012. [19]

From what can be seen in this figure, stages are stacked along the secondary line. The ground of each stage on is mutual.

In a higher-level topology, the authors of this paper explained the triggering process to output a pulse in the LTD. This can be seen in Figure 3.9 below.

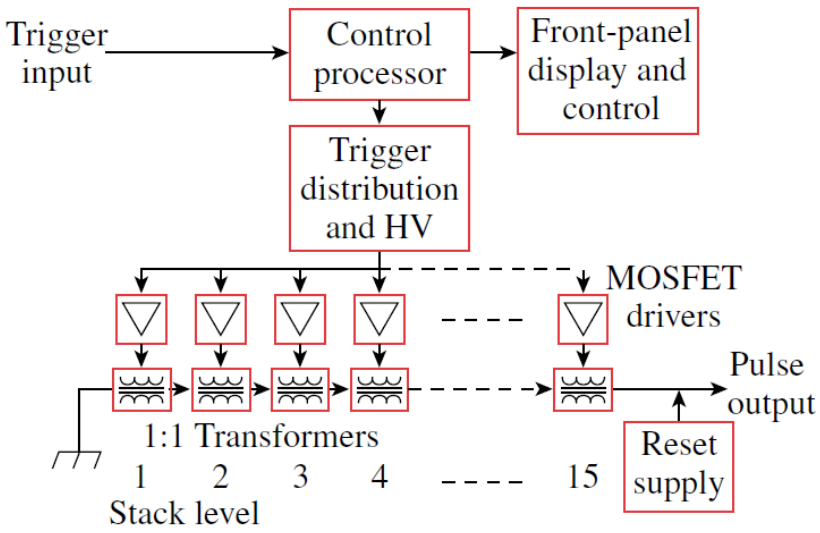


Figure 3.9: Higher-level LTD topology. Image from W. Bittle. Made in 2012. [19]

From what can be seen here, there is a central unit to output a logic pulse, that eventually feeds into MOSFET drivers that switch the MOSFETs. It is clear here that MOSFET drivers are an important piece in solid-state LTDs.

Next, the paper then goes into the transformer design. In Figure 3.10 below, it can be seen that the authors are using two disks. One of each disk that goes onto each side of a PCB board in between them. This is a nice and elegant design in making a modular LTD.

Figure 3.10: LTD transformer design. Image from W. Bittle. Made in 2012. [19]

After this figure, the authors then go into the material of the transformer core used and how the dimensions were designed. This is where the paper begins to become confusing to read. The authors used Metglas 2601SA1 as their transformer core. Unfortunately this core material is not found online anymore and its exact specifications cannot be found. What to take from this though is that Metglas is one of the best materials to look into for high-frequency applications since the authors are using this to get under a 10ns rise time. They then go into finding the cross-sectional area of the transformer core. Using a rearranged formula from Faraday's law, they used $A_e = \frac{3 \times V \times \Delta \times t}{\Delta \times B_{sat} \times PF}$. The constant three is the factor of safety for preventing saturation of the transformer core. The V is the maximum voltage swing the core will experience. $\Delta\ t$ is the pulse length. $\Delta \times B_{sat}$ is the flux density swing of the transformer core. Finally, PF is the packing-factor which is a ratio of how much core material is within an area when pressed with a material that keeps the lamination together.

For finding the magnetizing inductance, the authors used the following formula $L = \frac{\mu_0 \times \mu_r \times N^2 \times A_e}{l_e}$. This is taking the inductance of a toroid. l_e is the effective magnetic path length and can be defined as $2\ \pi\ r$. It is of note that the A_e found in the Faraday's formula is also used in this inductance formula. In the case of a LTD, N^2 is simply one due to no turns of wire used. The issue this paper runs into is not defining what they used for μ_r since their core material specification is not specified.

The paper then goes into the need to reset the transformer core after each pulse, and to find the DC current needed to reset the core. There is not much more explanation except using the B-H curve to figure this out. The physics and details in finding the current to reset the LTD cores will be explained in the engineering chapter.

The authors then go into more detail by providing a schematic of an individual primary drive circuit. This can be seen in Figure 3.11 below.

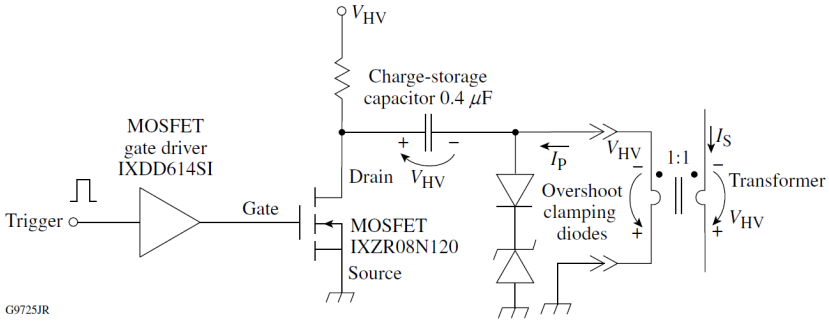


Figure 3.11: LTD individual MOSFET driving circuit. Image from W. Bittle. Made in 2012. [19]

This circuit shows that Transient Voltage Suppressors (TVS) diodes are needed to help protect the MOSFET. The MOSFET and driver model numbers are provided here as well.

In terms of a PCB board, the authors used a square geometry and arranged the solid-state switches around the circumference of the transformer. It can be seen that they are using a ring of metal on the PCB to be the contact to the transformer. This board can be seen in Figure 3.12 below.

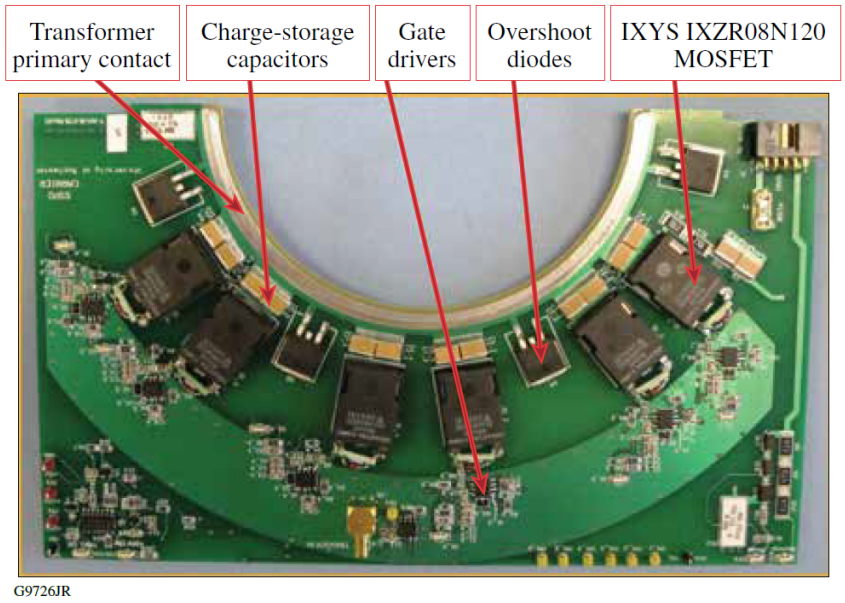


Figure 3.12: LTD PCB stage half. Image from W. Bittle. Made in 2012. [19]

The author then shows a photo of the overall LTD that contains all the PCB boards. This can be seen in the Figure 3.13 below.

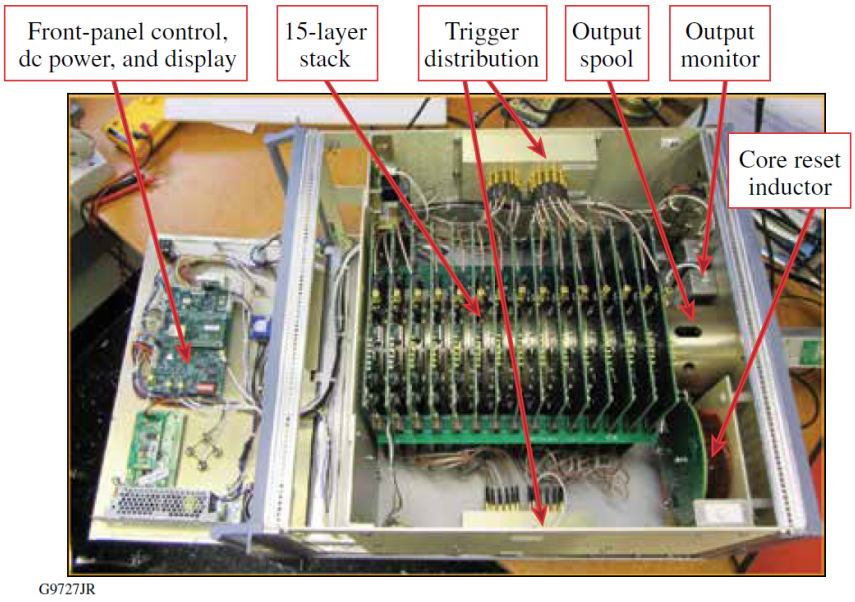
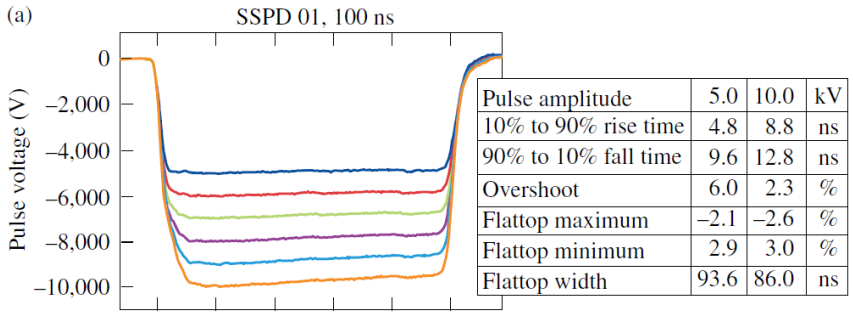


Figure 3.13: Full LTD assembly. Image from W. Bittle. Made in 2012. [19]

It is of great notice that the authors utilize coaxial cables to provide the triggering pulse to each of the stages. They are all of equal length. The LTD's output can be seen in Figure 3.14 below showing that it does indeed achieve the target specifications mentioned earlier.

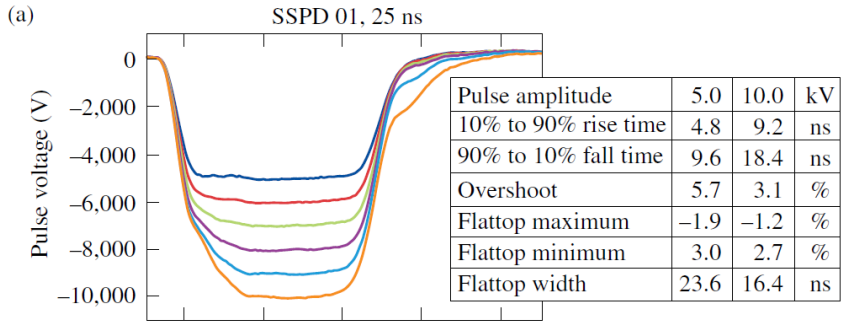


Pulse amplitude	5.0	10.0	kV
10% to 90% rise time	4.8	8.8	ns
90% to 10% fall time	9.6	12.8	ns
Overshoot	6.0	2.3	%
Flattop maximum	–2.1	–2.6	%
Flattop minimum	2.9	3.0	%
Flattop width	93.6	86.0	ns

Figure 3.14: LLNL-LLE LTD output pulses. Image from W. Bittle. Made in 2012. [19]

Note that the pulse length is 100ns. The LTD experiences a bit of drooping at 10kV, but otherwise the rise time is 8.8ns. This rise time may seem to be a great value, however this is for 10kV. For my LTD, 30kV is needed, thus improvements will need to be made to ensure it does not go over 10ns.

When the pulse length is shortened to 25ns, the rise time severely degrades. This can be seen in the Figure 3.15 below.



Pulse amplitude	5.0	10.0	kV
10% to 90% rise time	4.8	9.2	ns
90% to 10% fall time	9.6	18.4	ns
Overshoot	5.7	3.1	%
Flattop maximum	–1.9	–1.2	%
Flattop minimum	3.0	2.7	%
Flattop width	23.6	16.4	ns

Figure 3.15: LLNL-LLE output pulse anomaly. Image from W. Bittle. Made in 2012. [19]

The authors are not sure where this issue comes from, however a bit of an investigation was

done during this thesis to make a hypothesis of where it could come from. Professionals in the field are sure that the transformer core would not be the problem, as the type of transformer core would only increase the efficiency of the pulse. I then looked into the MOSFET driver being used, and it becomes apparent that this device is the reason why the rise time degrades with a shorter pulse length. The rise time of this driver is typically 25ns. [8] This means that a pulse length shorter than the rise time of the driver being used will experience severe performance issues. The jitter between all of the stages will also be severe, hence why the rise time of the overall LTD will experience a longer time. Individual stage data is not available in this paper. It is possible that the author did overdrive the MOSFET driver to operate faster, but going from 25ns to under 10ns still requires a decent amount of current to over drive the driver fast enough. The coaxial transmission lines going into each stage could provide another source of jitter. The lengths of these coaxial cables were not provided in the paper. Coaxial cables usually have GHz bandwidth, whereas the 25ns rise time driver appears to be the most likely barrier in achieving switch synchronization. However, another possible source for the degraded pulse when operating at a faster pulse length could be the transformer core itself. At higher frequencies, eddy currents become more pronounced and thus add more power loss to the transformer. Metglas may be hitting its operational limit with a faster pulse.

Overall, some useful LTD design formulas have been found in this paper, and a high-level overview of how to make a LTD work.

3.3 LLNL Solid-State LTD System Level Topology

The title of this paper is "A High Current, High Voltage Solid-State Pulse Generator For the NIF Plasma Electrode Pockels Cell." It was written by P.A. Arnold and et al. The authors wrote this paper at Lawrence Livermore National Laboratory in Livermore, California. This

was written in 2007.

This is a short paper, but nicely lays out the entire system level controls for a solid-state LTD. In terms of the performance of this LTD, it operates in the microsecond rise time range, therefore its design is not going to be the same in my LTD. However, there is a useful bit of information regarding how LLNL inserts their LTD stages into the transformer core. They use a method called the Ball-Spring approach. From another source, I looked into what this approach entails and found a useful graphic in Figure 3.16 below.

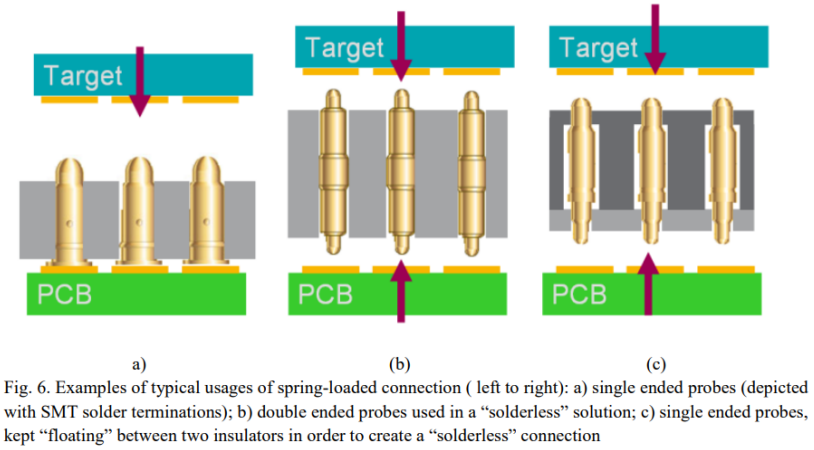


Figure 3.16: Graphic showing the three types of ball spring approaches. Image from R. Don Marx. et al. [50]

Approach letter "a" would be the most useful in my design as it has one of the main components contain the ball spring, meaning it only needs to be slid into the other component to form a good contact.

In Figure 3.17 below, a system level graphic from the LLNL paper can be seen.

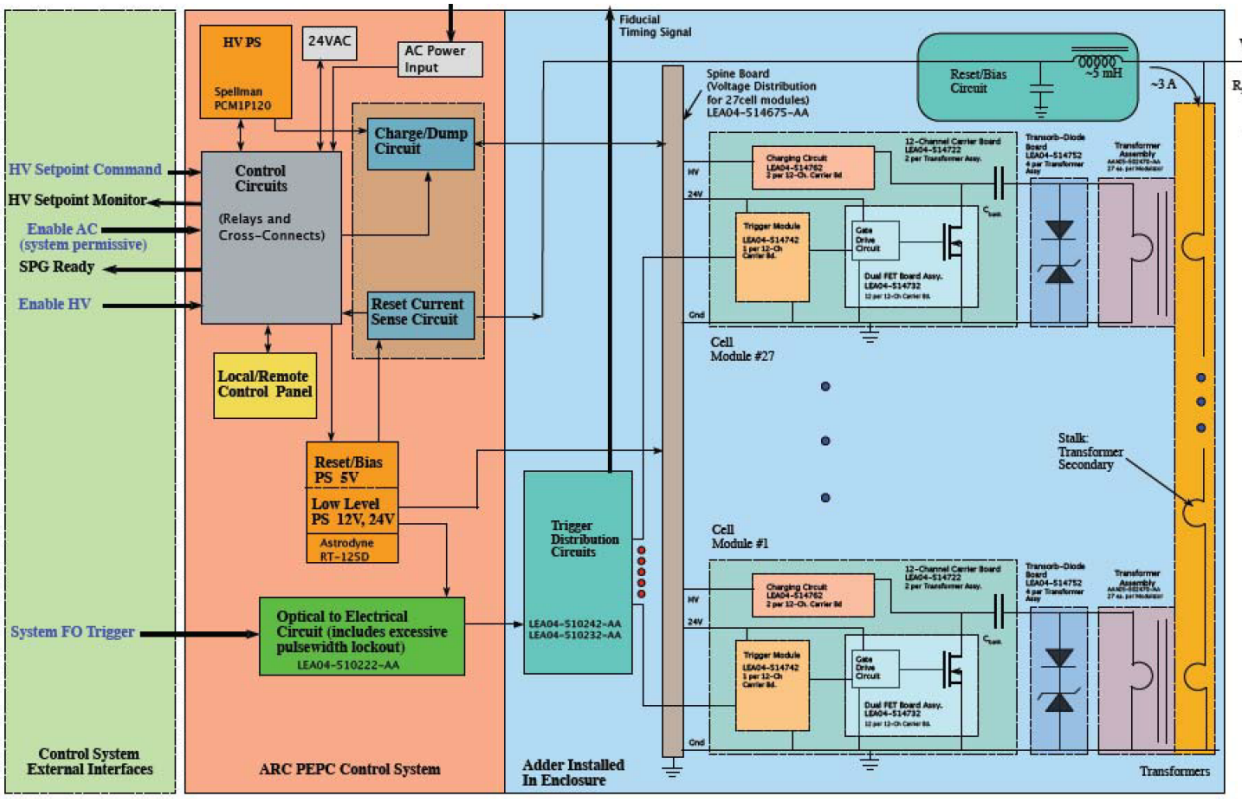


Figure 3.17: System level graphic in operating a solid-state LTD. Image from P.A. Arnold. et al. Image made in 2007. [15]

There are clearly a lot of control systems being used for this LTD. It is of notice that the top-left section is the control for running the high-voltage power supply, along with a way to charge and dump energy. Towards the bottom-right, the main logic signal is sent to the LTD over fiber optics. In this version, the optical signal is then transferred into electrical, then distributed amongst all the stages. The parts of real interest are the resetbias circuit on the top-right and the TVS diode being used for each stage. The bias circuit is used to supply a reverse current flow into the transformer secondary in order to reset the magnetization of the transformer cores. The inductor there is used to act as a low pass filter in order to prevent the main LTD pulse from going into the bias circuit. The authors did note that they could not find any appreciable resetting of the magnetic cores between bursts of pulses. They had

to take seconds in between resets for it to occur properly.

The TVS diode is used to prevent high voltage spikes that can damage the LTD electronics that can occur from inductance in the circuit. If damages to the LTD do occur, the authors incorporated LEDs that turn on if parts are damaged in order to help technicians fix the issue.

In summary, this paper provides a quick overview about how to control the major components in a LTD, along with how to easily plug in the LTD to the transformer core.

3.4 Jiang Solid-State LTD

The title of this paper is "Pulsed Power Generation by Solid-State LTD." It was written by Weihua Jiang and et al. The authors wrote this paper at Nagaoka University of Technology in Nagaoka, Japan. The paper was written in 2014.

While American, Indian, and Russian LTD publications are easily seen online, Japan is also developing more sophisticated solid-state LTDs. Dr. Jiang has been developing a LTD that can pulse out custom waveforms by varying when each individual stage turns on. If a load does not require the LTD's maximum voltage output, then it is possible to pulse each individual stage in a sequence to create high-frequency pulses. In the future, he is looking into technology to allow the LTD to self-calibrate all of its stages in order to take away stage jitter.

The best part about this paper is the voltage requirement this LTD is designed to operate in. The output voltage is 30kV and a maximum output current of 240A. The rise time however is around 30-40ns. The output pulse can be seen in Figure 3.18 below.

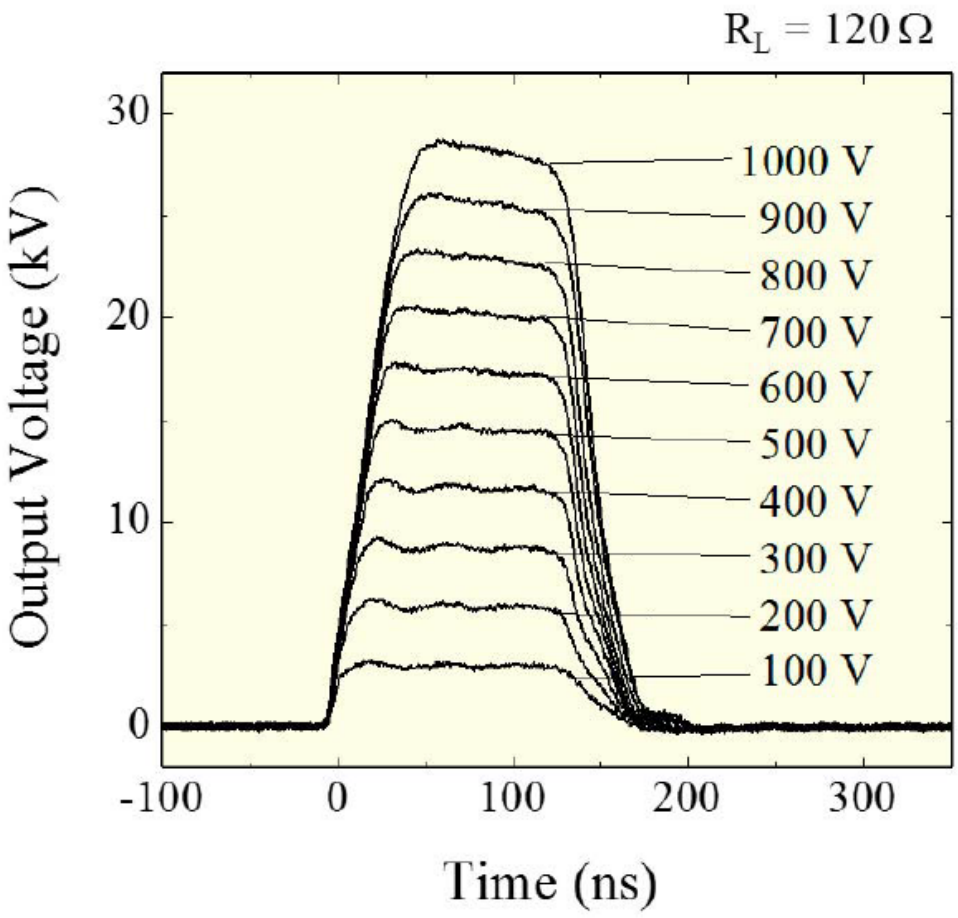


Figure 3.18: Output pulses using varying voltage levels on the load. Image from H. Weihua Jiang. et al. Image made in November 2014. [44]

The output pulses appear to be clean, without oscillations. However, the rise times do not go under 10ns. It is of note that the author was not focusing on a fast rise time LTD, but focusing on the concept of individually controlling stages.

There are useful pictures provided that show the design of the LTD in this paper. In Figure 3.19 below, a single LTD stage can be seen.

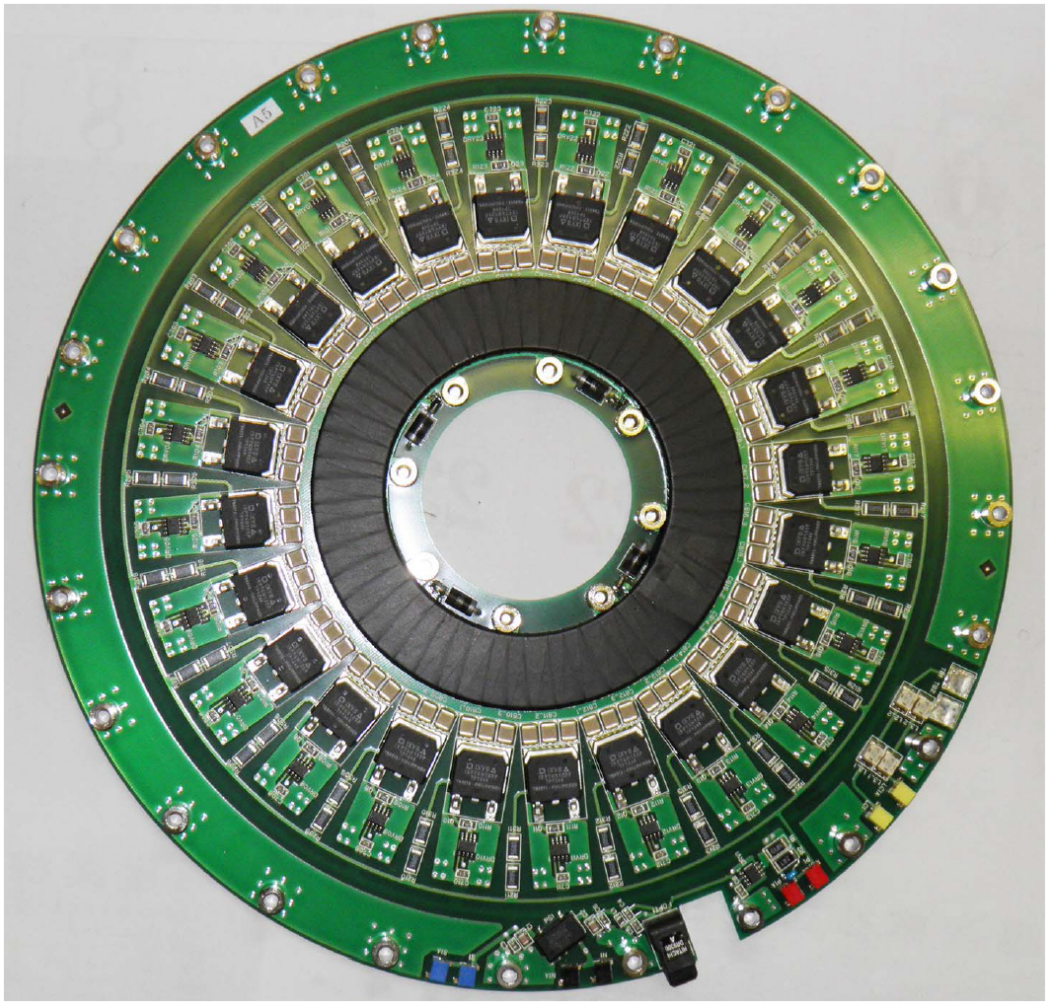


Figure 3.19: Single stage of Dr. Jiang's LTD. Image from H. Weihua Jiang. et al. Image made in November 2014. [44]

Useful design methods of note are the HV line running in a circumference around the MOSFETs, then coming in through their side. Unlike in the Livermore LTD that uses ball springs to secure the PCB to LTD in a plug-and-play setup, Dr. Jiang's LTD routes all of the positive channels across all the stages along the secondary stalk, then returns on the outside of all the stages. The picture in Figure 3.20 below shows a better view in how the stages stack and the ground return columns can be seen.

Figure 3.20: 30 Stages of Dr. Jiang's LTD. Image from H. Weihua Jiang. et al. Image made in November 2014. [44]

This method is effective in creating a compact LTD, however unlike the Livermore LTDs, there is no way to easily replace broken stages without removing multiple nuts. Also, unlike the Livermore LTDs, having a single circular PCB per a stage is better in reducing the length of the overall LTD. Thus, reducing the overall rise time as the pulse travels through the transmission line. Having an additional metal plate on the other side of the PCB increases the overall length, thus increasing the overall rise time.

Overall, the results from Dr. Jiang's LTD are promising since using better quality switches

and drivers can allow the LTD to achieve <10ns risetimes.

3.5 Leckbee SNL 7-MV LTD

This paper is useful in seeing details about the makeup of a LTD stage. Also, this is a gas-switch design and it would be useful to compare the differences between gas-switch LTDs and solid-state LTDs. The LTD in this paper is a 7 megavolt output for flash x-ray radiography applications. In Figure 3.21 below, a single-stage of this LTD can be seen.

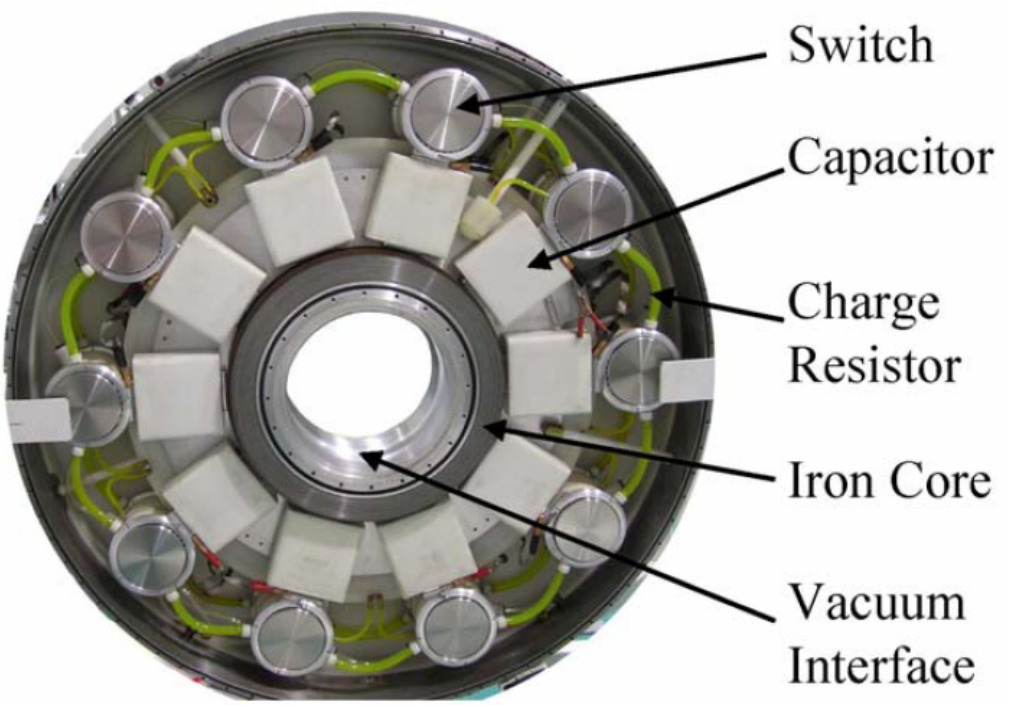


Figure 3.21: Single stage of the 7-MV LTD. Image from B. Joshua Leckbee. et al. Image made in 2008. [48]

Unlike what can be seen from the photos in the solid-state LTD papers, this photo clearly shows where all of the different parts in a stage are. In terms of the differences between a

gas-switch and solid-state switch design LTD, they both use a similar control structure, but keep in mind the auxiliary gas systems needed to use spark gaps. The output pulse from a single stage can be seen in Figure 3.22 below.

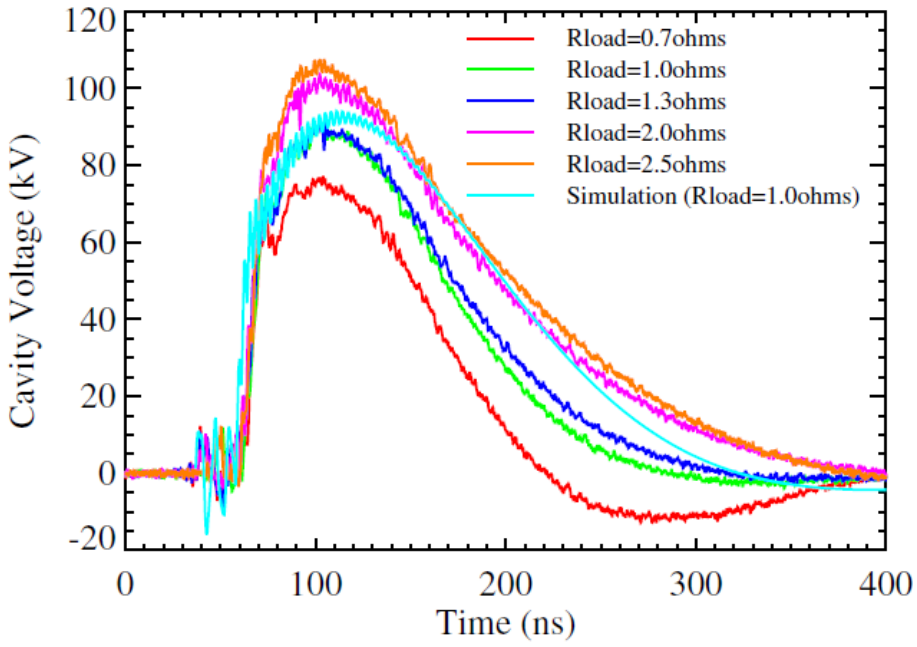


Figure 3.22: Single stage pulsed power output. Image from B. Joshua Leckbee. et al. Image made in 2008. [48]

The pulse shape here is a sinusoidal response. This is different when compared to solid-state LTDs that can sustain a square-wave type response. This is also due to the fact that gas-powered switches cannot be turned off on command, thus care must be taken in order to create a critically or overdamped response to prevent oscillations.

3.6 Liang 500kA LTD

The title of this paper is "Design of the 500kA Linear Transformer Driver Stage." It was written by Tianxue Liang and et al. The authors wrote this paper at the State Key Labo-

ratory of Environment Simulation and Effect for Intense Pulsed Radiation in the Northwest Institute of Nuclear Technology, located in China. The paper was written in 2013.

This LTD is another gas-switch LTD, with some useful design details. The author added in two equations that can be used to find the magnetic-core loss and excitation inductance.

The magnetic-core resistance loss of the LTD can be calculated by $R_c = \frac{8 \times p \times S}{\delta^2 \times l}$. Where p is the resistivity of the magnetic core and δ is the thickness of the core's lamination. The excitation inductance can be calculated by $L = \frac{U_r \times U_0 \times S \times k_t}{l}$. Where k_t is the packing factor and l is the average circumference of the magnetic cores. [49] Keep in mind, that these values are simple to calculate when using data that are given in data sheets, however when working with MHz frequency pulses, this data may not be available and one cannot assume that resistivity and permeability are linear in order to extrapolate the given data.

A single-stage of the LTD being designed in this paper can be seen in Figure 3.23 below.

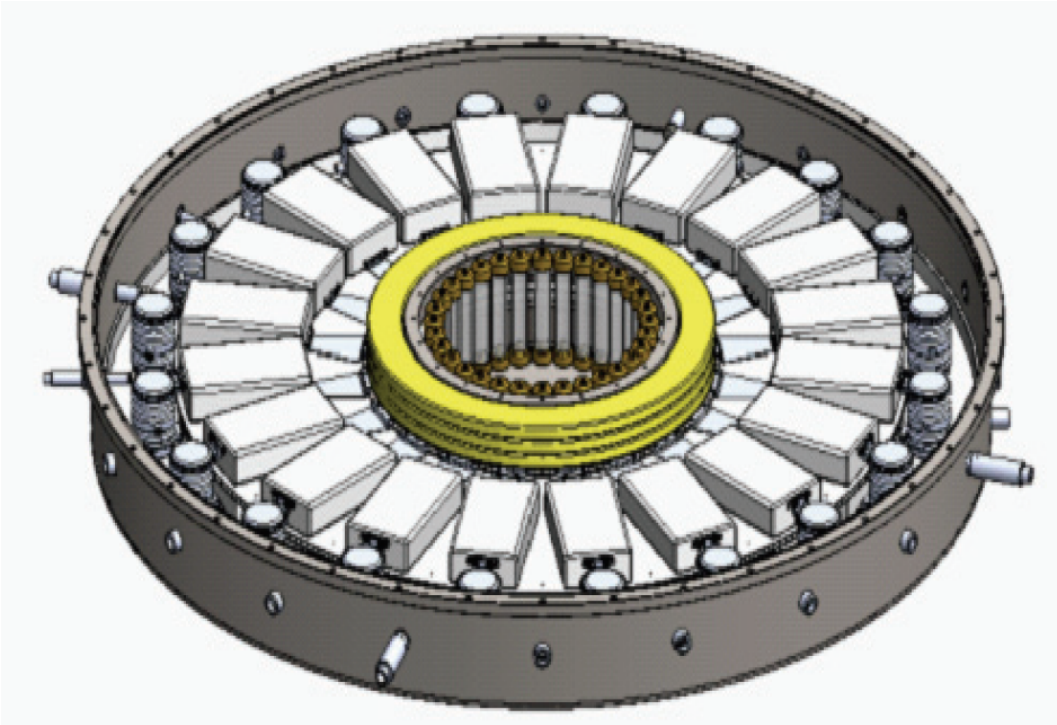


Figure 3.23: Graphic of a 500kA and 150ns LTD stage. Image from F. Tianxue Liang. et al. Image made in 2013. [49]

It can be seen that the LTD design is similar to the Sandia LTD and all LTDs in general.

3.7 Wang DARHT-II LTD

The title of this paper is "Modeling of An Inductive Adder Kicker Pulser for DARHT-II." It was written by L. Wang and et al. The authors wrote this paper at Lawrence Livermore National Laboratory in Livermore, California. No year is provided by this paper, but looking at the sources used, it was written after 1999.

Another Livermore LTD, this paper provides useful design equations in determining the stalk parameters and a lump LTD model for use in simulation.

The paper provides a LTD model that can be seen in Figure 3.24 below.

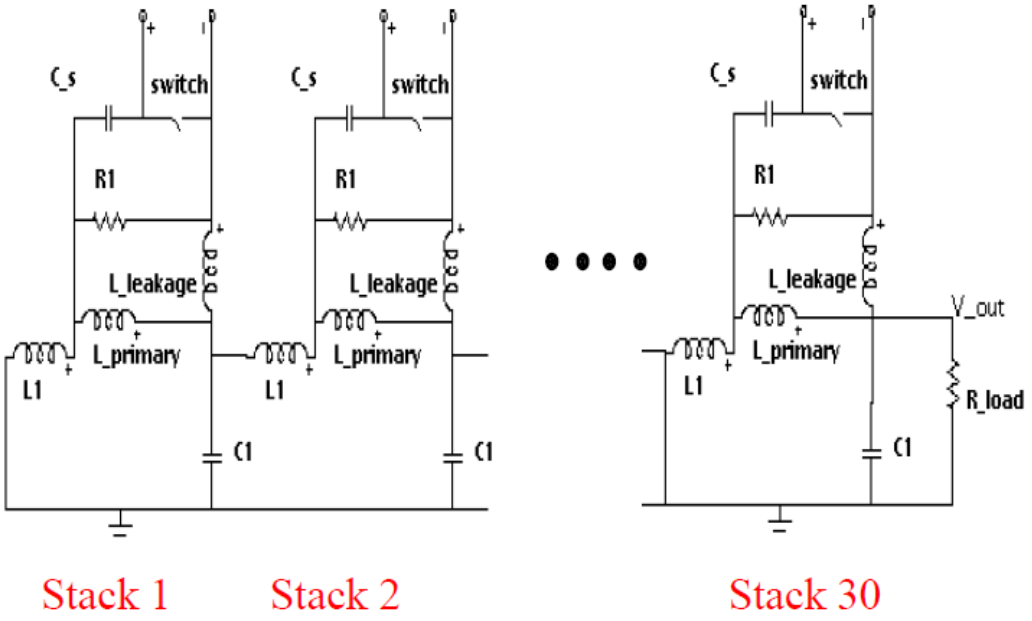


Figure 3.24: LTD circuit model that can be used for simulations. Image from G.L. Wang. et al. [60]

C_s in the model is the capacitor paired with the switch. $R1$ is the resistance on the primary. $L_{leakage}$ is the leakage inductance of the transformer and $L_{primary}$ is the primary inductance. $L1$ and $C1$ are the inductance and capacitance per stage length. To find $L1$, the equation is $L1 = \frac{u_0 \times h \times ln\frac{b}{a}}{2 \times \pi}$. To find $C1$, the equation is $C1 = \frac{2 \times \pi \times e_0 \times h}{ln\frac{b}{a}}$. The impedance of the stalk is found by $Z = \sqrt{\frac{L1}{C1}}$. It is important to match the stalk impedance with the load impedance to avoid a decrease in performance. [60]

The LTD model shown in this paper was useful when designing the overall LTD model simulation.

3.8 Stygar Two Petawatt LTD

The title of this paper is "Conceptual Designs of Two Petawatt-Class Pulsed-Power Accelerators for High-Energy-Density-Physics Experiments." It was written by W. A. Stygar and et al. The authors wrote this paper across all over the United States, but the system is to be built at Sandia National Laboratory in Albuquerque, New Mexico. It was written in 2015.

This paper is worth mentioning as it gives an excellent design overview of a large scale LTD system and the physics behind it. This paper does not use solid-state switches, but nevertheless, the physical equations brought up can be of use for my LTD. The authors of this paper also made some incredible CAD visuals that help to show the details inside the LTD.

In Figure 3.25 below, a high-level view of the two-petawatt pulsar device can be seen.

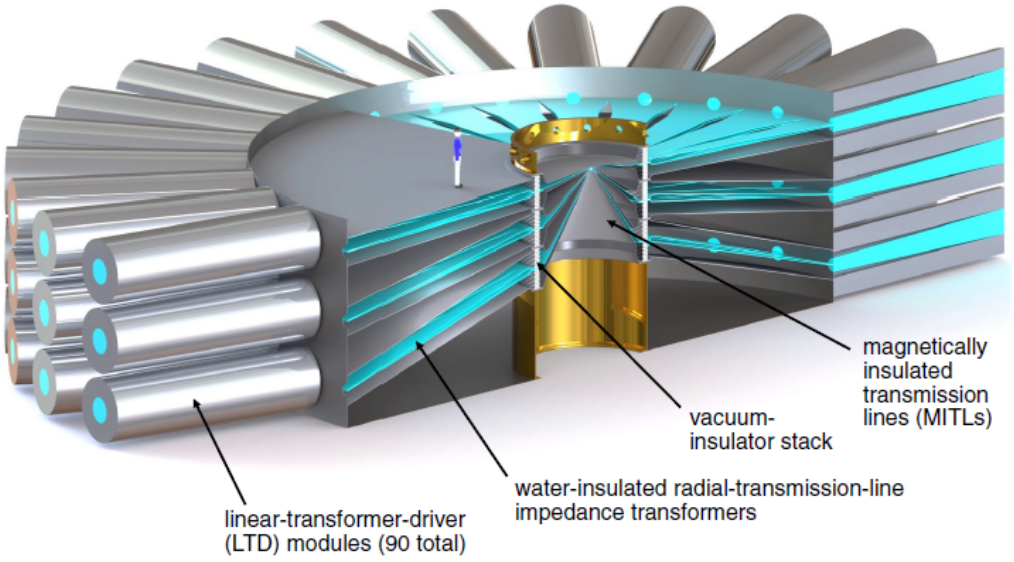


Figure 3.25: Graphic of the Z-300 accelerator where the placement of LTDs can be seen. Image from T. W. Stygar. et al. Image made in 2015. [58]

LTDs are used to supply the pulsed power along the perimeter of the main system. This graphic is also a great concept to see published since it means LTDs are now being used to

power the next state-of-the-art pulsed power facilities.

In Figure 3.26 below, a cross-sectional view of a single LTD can be seen.

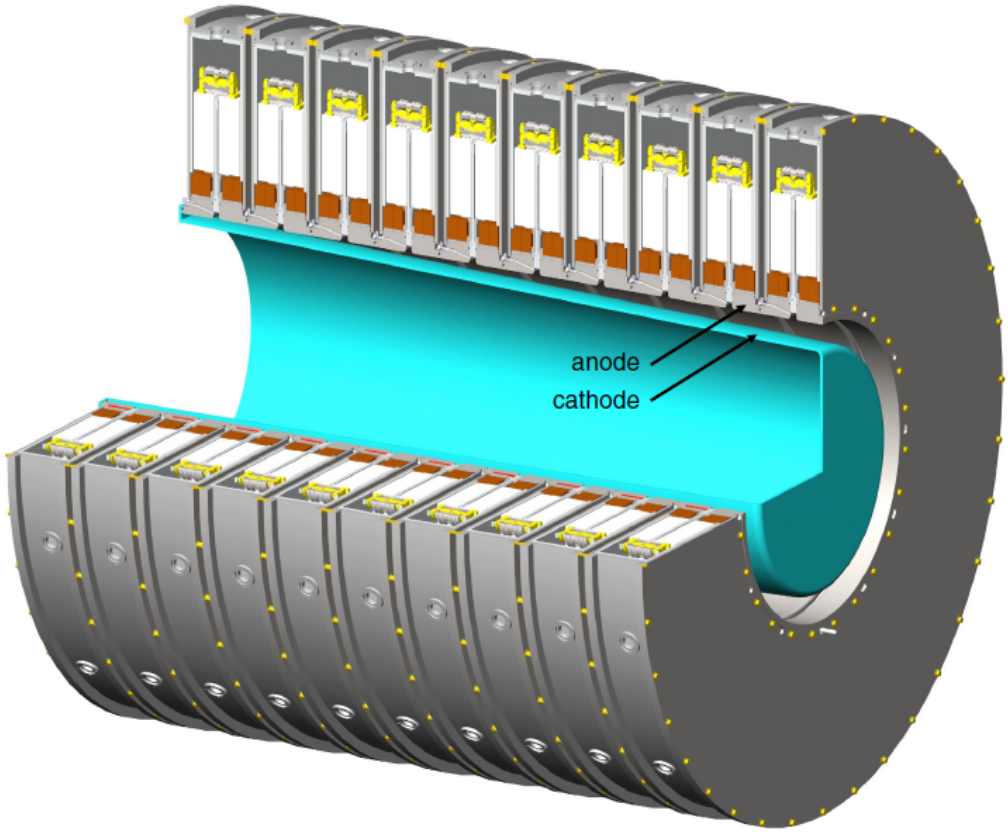


Figure 3.26: Cut view of one LTD module for the Z-300 accelerator. Image from T. W. Stygar. et al. Image made in 2015. [58]

As consistent with the previously mentioned LTD papers in this chapter, there are stages stacked along a transmission line. The insulation for this line is water. A gas switch is moving energy from the two capacitors connected to it in series.

In Figure 3.27 below, a closer look at a single LTD stage can be seen.

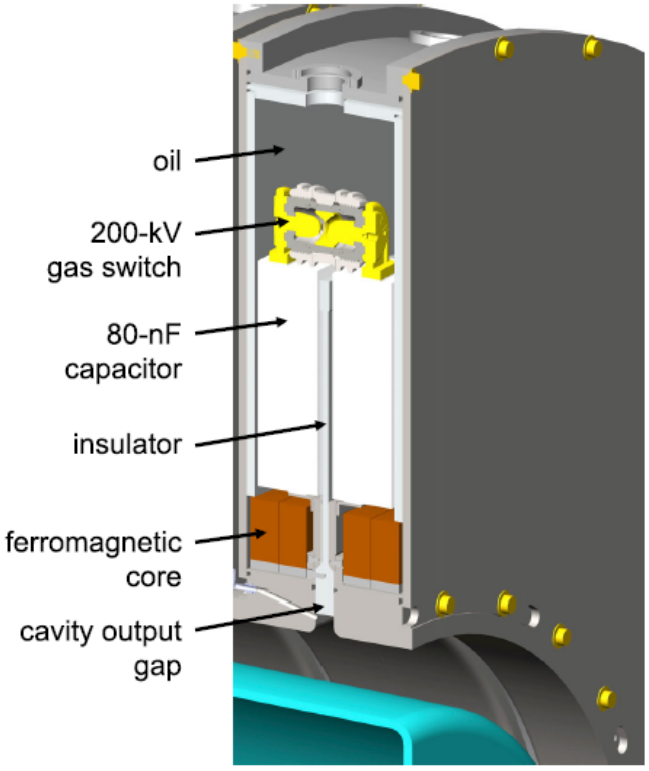


Figure 3.27: Cut view of one LTD stage for the Z-300 accelerator. Image from T. W. Stygar. et al. Image made in 2015. [58]

Due to the high power being used in this LTD, the authors of this paper have used oil to insulate the components within the stage. The Metglas core being used is Metglas 2605CO. This is significant for me since I am going to use this same material for my LTD. Looking a little further, a formula has been provided in finding the shunt resistance of the cores.

The formula for the shunt resistance is as follows: $R_{cores}(t) = \frac{2S(\mu\mu_0\rho_{cores})^{\frac{1}{2}}}{\pi^{\frac{3}{2}}\ r_{cores}\ \delta\ t^{\frac{1}{2}}}$. [58] The variables in the formula are explained as by the authors in the list below.

S is the total cross-sectional area of the transformer core

μ is the effective relative permeability of the transformer core

μ_0 is the permeability of free space

ρ_{cores} is the resistivity of the transformer core

r_{cores} is the radius of the centroid of the core material

δ is the thickness of the Metglas tape used in making the core

When knowing the exact constants to use, this formula can be well used. However, the authors in the paper did acknowledge that assumptions have to be made since both the permeability and the resistance of the cores are time dependent. An assumption that can be used is if the shunt resistance of the cores is much greater than the impedance of all parallel bricks within the stage, then both shunt resistance and permeability of the core become insensitive to each other. Finding the permeability of the core at a specified time of the pulse can give a useful shunt resistance, say at the point where the pulse reaches its peak power.

Overall, this paper delves deep into the shunt resistance of a transformer core compared to other works out there. The high resolution graphics help paint a better picture of the makeup of a LTD stage. However, these designs are meant for high powered gas switches, and my design is a bit different by using solid-state switches.

Chapter 4

Feasibility Study

In order to be able to best select a solid-state technology to be used in the LTD, a feasibility study was done to determine which one will have the lowest cost. On top of low cost, the study selected which solid-state switch would be able to achieve the target specifications. Another integral part of the LTD are the capacitors paired to each solid-state switch. This was also modeled to build a better sense of how much the overall LTD will cost. It is also important to model not only the target specifications, but also a range of different voltages, currents, and energy levels to determine future viability for additional uses. The LTD is modular in nature, and it is possible to switch out PCB boards and add additional stages to change it according to new needs.

It is of note that based upon the given specifications for the LTD to be made already, that some capacitor and switching technologies could be ruled out right away, however this feasibility study is also looking at how much better different technologies are compared to each other. For example, comparing a spark gap switch's performance to a SiC MOSFET. The algorithm developed for this model can also be used for future LTD designs.

This section will be split in the following ways: modeling approach and goals, high-level flow charts of MATLAB algorithm, solid-state switches to compare, capacitor technologies to compare, and the results of the MATLAB model.

4.1 Modeling Approach and Goals

The goal of the modeling code to be developed is to get a comprehensive overview of how the LTD would look like using each different switching technology. It is important to compare costs, weight, size, capacitor technologies, and outputs that work with given parameters that the user sets. It is the goal that this modeling software can be used not just for developing the LTD being made for this thesis, but for all future LTDs. The user would only need to change switch parameter inputs and algorithm variables to compare the right switching technologies for their LTD.

The switches that will be used for this feasibility study will be ones that will relate closely or even meet the specifications set for the LTD to be designed. This is dependent on the switching technology, as some that will be analyzed cannot meet all the target specifications. As a control, spark gap switches will also be studied to compare the advantages and disadvantages solid-state technologies have over gas switches.

There are three outputs that have been made for this model.

1. Switch comparison table that compares all switches at a single specified set of target specifications.
2. Logarithmic surface plot that compares all switches against a range of voltage and current points and shows the cost of the LTD at each of those points as a color.
3. Logarithmic surface plot that compares all capacitor technologies against a range of

voltage and current points and shows the cost of the LTD at each of those points as a color.

To go into further detail, the user will first see a table that will neatly summarize the cost of the LTD, its weight in grams, its circumference in mm, its depth in inches, the number of stages needed, and the capacitance for each individual capacitor needed in the LTD. An example output can be seen below in Figure 4.1.

	Switch_Cost	Switch_Weight	Switch_Circumference	Switch_Depth	Switch_Stages	Switch_Capacitance
IGBT	4288	5721.7	96.78	11.5	23	2.0708e-06
Power MOSFET	22276	8739.9	258.08	15	30	1.0058e-06
Spark Gap	3511.5	44211	127	5	1	7.6734e-06
PPIGBT	17934	12856	100	30	10	5.4718e-06
SIC	9277.1	12047	397.02	11.5	23	3.6238e-07

Figure 4.1: Example output of MATLAB algorithm in a table comparison

The user will next see a surface plot comparing all of the switching technologies and outputting the cost in logarithmic scale across a range of voltage and current points. The algorithm will select the cheapest capacitor technology when coming up with the cost for each point. The user will also notice non-colored (black) regions of the surface plot. This means that those sets of points have either went over the cost threshold the user set, the energy level in the capacitors used deplete too quickly for the LTD to even have a viable output, or the rise time exceeded the rise time threshold set by the user. The user will also see the load impedance attribute in the title of the plots. An example output showing one of the subplots and without the logarithmic cost scale can be seen below in Figure 4.2. This specific example plot output shows the overall cost of the LTD for a IGBT switch for varying voltages and currents. As costs are not being analyzed in showing this example output, in general the more yellow the color is, the more expensive the LTD becomes. The more greener and bluer the color is, the cheaper the LTD becomes. This applies to both the switch and capacitor surface plots.

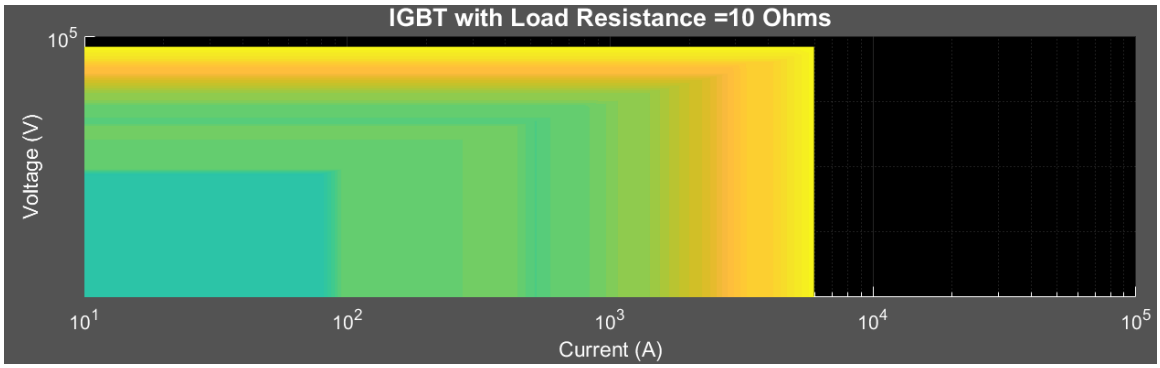


Figure 4.2: Example output of MATLAB algorithm in a surface plot switch comparison with coloring representing varying overall LTD costs

Finally, the user will see a surface plot comparing all of the capacitor technologies with an output similar to the surface plot comparing all of the switching technologies. The algorithm will select the cheapest switching technology for each set of points when calculating the cost of the LTD. This is useful for showing what capacitor technology is viable under what set of specifications. An example output showing one of the subplots and without the logarithmic cost scale can be seen below in Figure 4.3. This specific example plot output shows the overall cost of the LTD for a film capacitor for varying voltages and currents.

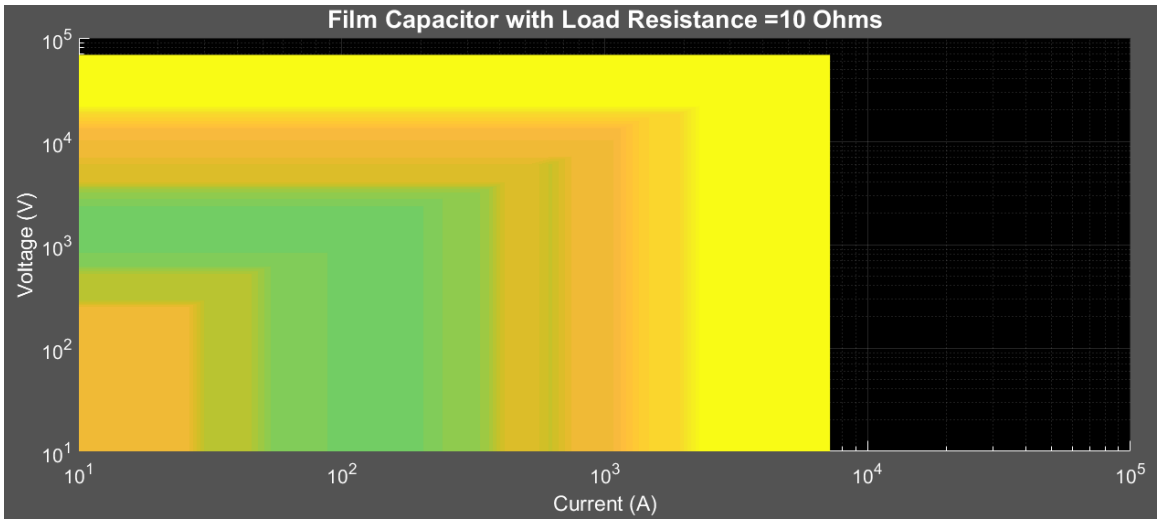


Figure 4.3: Example output of MATLAB algorithm in a surface plot capacitor comparison with coloring representing varying overall LTD costs

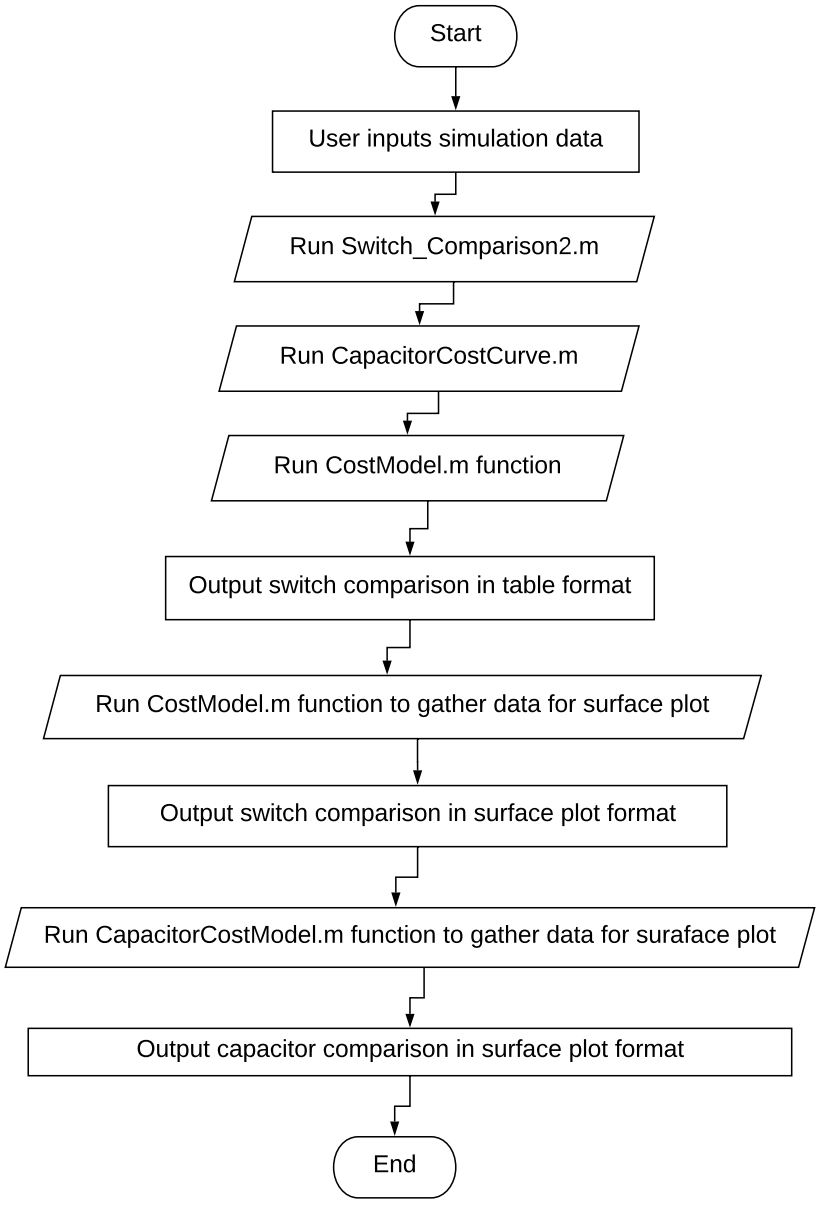
Overall, the user will get a good sense of how they would want to go about designing their LTD. The best switch can be selected, along with the most cost effective capacitor technology.

4.2 High-Level Flow Charts of MATLAB Algorithm

In this section, I give a quick overview of the operation of the MATLAB model at a high-level. This means how the different functions interact with each other in the main function, and quick flow chart going over the operations in the other functions. For an explanation of how the code works, please see appendix .6.

4.2.1 Function Interaction Flow Chart

A flow chart is shown on how the MATLAB algorithm operates in terms of how the main function is pulling the different MATLAB functions to create the outputs needed. The flow chart can be seen in the page below.


Start
User inputs simulation data
Run Switch_Comparison2.m
Run CapacitorCostCurve.m
Run CostModel.m function
Output switch comparison in table format
Run CostModel.m function to gather data for surface plot
Output switch comparison in surface plot format
Run CapacitorCostModel.m function to gather data for suraface plot
Output capacitor comparison in surface plot format
End

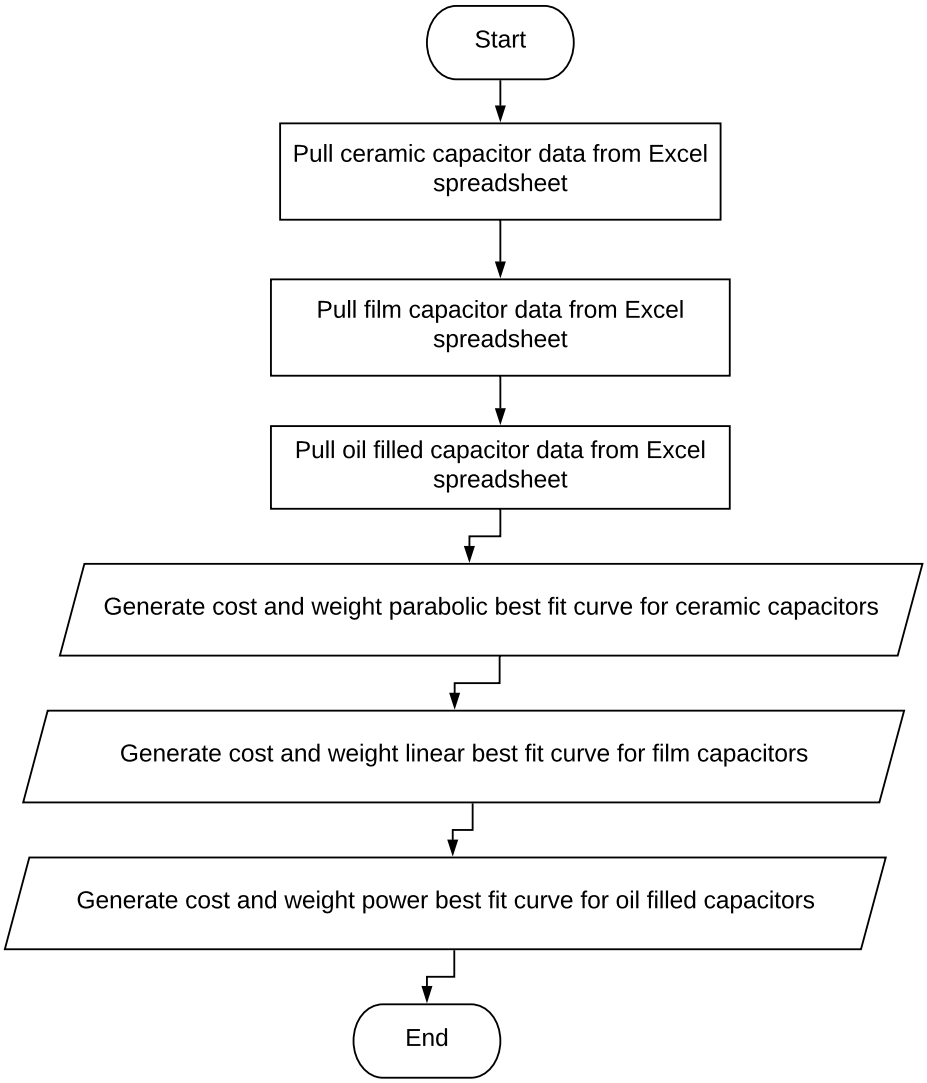
In the flow chart, it is of notice that there are four MATLAB files being used. In Table 4.1 below, there is an explanation of what each of these files does.

MATLAB Function	**Description**
Switch_Comparison2.m	Utilizes the other three MATLAB files to generate three readable outputs for the user
CapacitorCostCurve.m	Uses a Microsoft Excel file filled with capacitor data to generate capacitor cost curves and weight curves
CostModel.m	Uses five user specified switches and generates a LTD model for each of them
CapacitorCostModel.m	Uses three user specified capacitor technologies and generates a LTD model for each of them

Table 4.1: Table summarizing the purpose of each MATLAB function

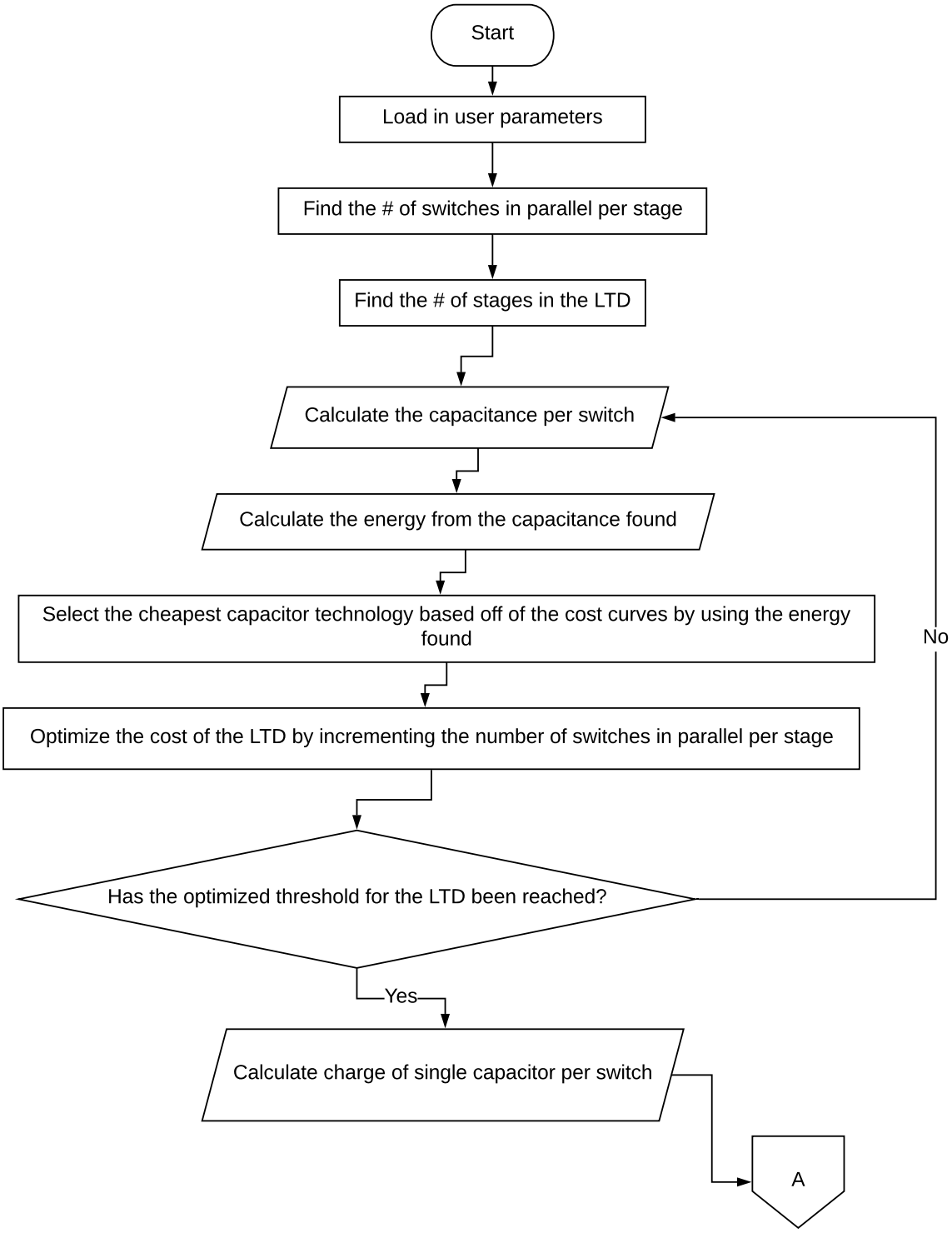
This finishes the high-level overview of how the functions are being pulled up by Switch_Comparison2 during the operation of the feasibility study code. Next, this section discusses at a high-level of how the three data collection or creation functions operate.

4.2.2 Capacitor Cost Curve Function Flow Chart

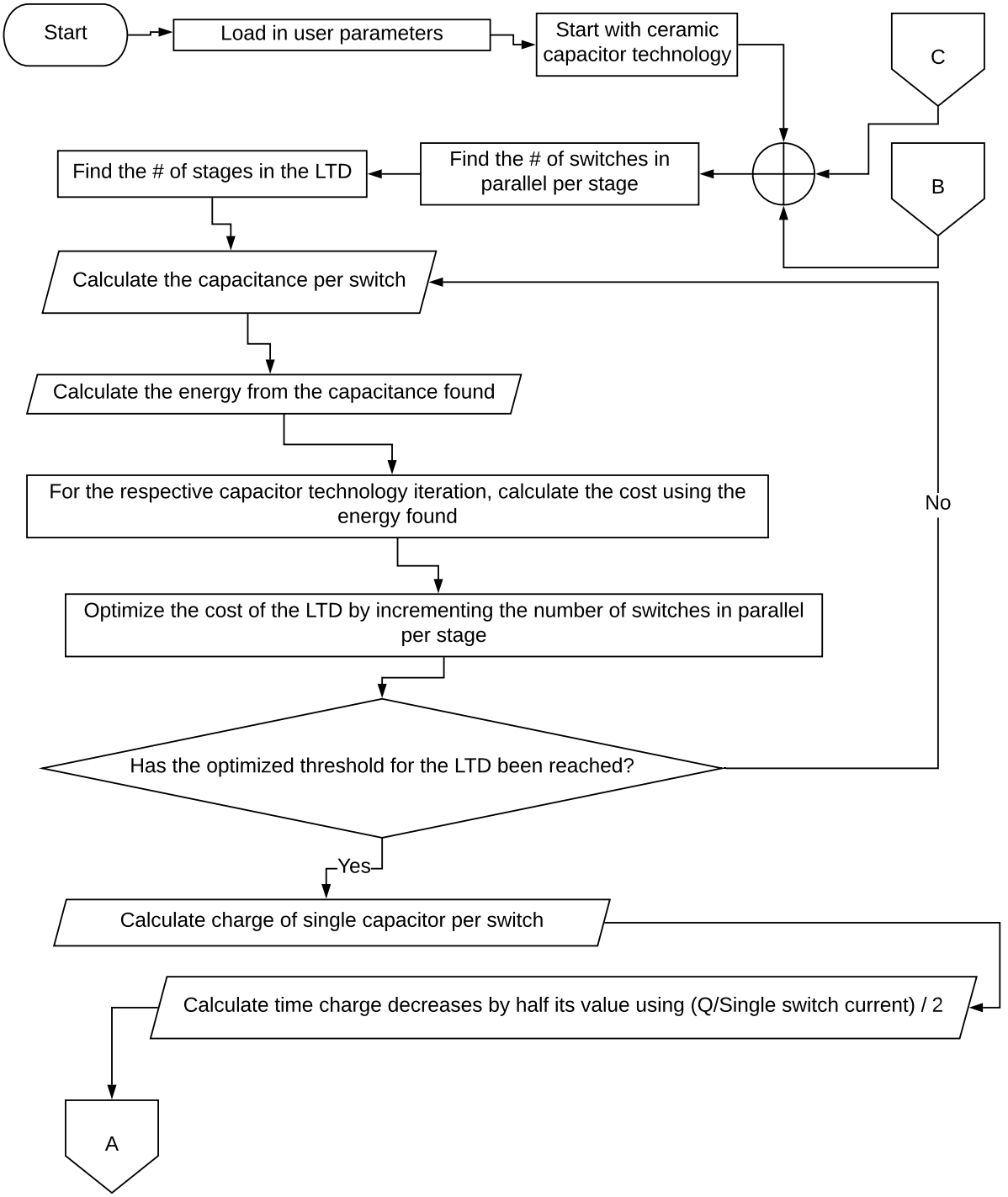


4.2.3 Switch Cost Model Function Flow Chart

There is of note here that the distance between LTD stages is not changing based upon the voltage per stage. For the purposes of this modeling, this is not necessary due to the ability of an engineer to use various forms of dielectrics to keep stages close together. If an air insulated LTD is absolutely necessary no matter the stage voltage, then this model will not satisfy a proper representation of that LTD. This is because if LTD stages are not close together, it begins to lose its coaxial properties which is an assumption in calculating its transmission line effects. This in turn affects the rise time output of the model. Not to mention, if LTD stages are not near each other, the risk of EMI affecting the switching performance increases as there is no natural coaxial shielding against EMI. This is why the model will not be pushing LTD stages further apart from each other as feasibility becomes questionable.


Start
Load in user parameters
Find the # of switches in parallel per stage
Find the # of stages in the LTD
Calculate the capacitance per switch
Calculate the energy from the capacitance found
Select the cheapest capacitor technology based off of the cost curves by using the energy found
Optimize the cost of the LTD by incrementing the number of switches in parallel per stage
Has the optimized threshold for the LTD been reached?
No
Yes
Calculate charge of single capacitor per switch
A

4.2.4 Capacitor Cost Model Function Flow Chart



4.3 Switches to Compare

This MATLAB model will consider five switches and will have the ability to compare each switch. Again, there are other switching technologies that can be added, however these switches have been ruled out already in having any feasibility for my LTD design purposes. It is of note that these switches could easily be added into the code in the future by changing switch parameters for any switch in the code.

This section will be organized into two sub-sections, one discussing about the control switch to compare. This will be a spark gap switch, which is the conventional technology in pulsed power applications. Then the next sub-section will go over the four viable solid-state switches used in pulsed power. The switches in here have decent rise times, the ability to operate over 50V, can sustain a timed pulse (not an impulse), and are non-latching.

4.3.1 Spark Gap Switch as the Control

The spark gap switch to be used in the modeling program is from R.E. Beverly III and Associates. The company is from Ohio and specializes in developing spark gap switches. They provide ample documentation on their switches which is one of the reasons why their switch is going to be used in this study.

The name of their switch model is called SG-101BM. This is their cheapest and smallest switch available. Keep in mind, that one of the goals of this thesis is to design a compact LTD. Using a larger spark gap switch will take me away from this goal. Even more convenient, there is already a SG-101BM being used at Virginia Tech to get accurate parameter data.

In terms of circuitry cost to drive the spark gap switch, the ignition trigger will be considered.

The switching parameters to be used in the model are below:

- Voltage Rating: 38kV
- Pulsed Current Rating: 100kA
- Breakdown Delay: <250ns
- Switch Width: 127mm
- Switch Weight: 3,628.74g
- Switch Cost: $695
- Switch Triggering Circuitry Cost: $1,495

Solid-State Switches

The four solid-state switches to be used in the model are the following: PMOSFET, SiC MOSFET, IGBT, and PPIGBT. The chosen switches will be discussed in these subsections. Keep in mind that IGBT technologies inherently have longer rise times that can go into the sub-microseconds, however are good to compare nevertheless due to their high voltage and current ratings. They may be useful in a slower rise time application.

Power MOSFET The best power MOSFET switch for this LTD application is called the IXZR08N120B-00 from IXYS. The switch is expensive at $40.59 a switch, however compared to other NMOS MOSFET technologies, its current and voltage maximums are superior. Thus, it would save more money by using less stages in a LTD than using much lower voltage rated MOSFETs. This is also important as less LTD stages means a more compact LTD,

helping to achieve the compactness goal.

The switching parameters to be used in the model are below:

- Voltage Rating: 1.2kV
- Pulsed Current Rating: 40A
- Rise Time: 5ns
- Switch Width: 16.13mm
- Switch Weight: 3.5g
- Switch Cost: $40.59
- Switch Triggering Circuitry Cost: $2.05

SiC MOSFET The SiC MOSFET switch chosen for this model is called the C2M1000170J from CREE. It is cheap at $5.87 a switch and has a great voltage rating.

The switching parameters to be used in the model are below:

- Voltage Rating: 1.7kV
- Pulsed Current Rating: 15A
- Rise Time: 4.8ns
- Switch Width: 10.180mm
- Switch Weight: 1.6g
- Switch Cost: $5.87
- Switch Triggering Circuitry Cost: $2.05

IGBT While high voltage IGBTs typically have a switching performance near 100ns, there is one that was found that can compete with SiC MOSFETs. This IGBT is called IXYH16N170C and its rise time is only 19ns. This is impressive for this technology considering that this IGBT can do 1.7kV and 100A pulsed. Now, 19ns may seem to already be not feasible for the LTD to be designed, however if the IGBT was used in cascode, it is possible its rise time could be cut close to an order of magnitude. This will keep it under 10ns, thus can be an actual competitor against other solid-state switches. This comes at a cost of being a little larger and requiring two switches. For the sake of simplicity, the total cost of this IGBT will be multiplied by two in order to account for the extra cost in putting it into a cascode arrangement.

It is important to realize that IGBTs have to be driven a bit differently than MOSFETs as they are both current and voltage activated. The driver used for the IGBT can be the same as for the MOSFET, but with different considerations in terms of the current output.

The switching parameters to be used in the model are below:

- Voltage Rating: 1.7kV
- Pulsed Current Rating: 100A
- Rise Time: 19ns or approximately 2ns for cascode
- Switch Width: 16.13mm
- Switch Weight: 6g
- Switch Cost: $9.71 per unit or $19.62 for cascode
- Switch Triggering Circuitry Cost: $2.05

Pressed-Packed IGBT Due to the intense nature of PPIGBTs, their rise time will most likely not go under 10ns, even in cascode. Since they are expensive and not small, these would not work well in cascode for the LTD application being made. However, it is worth exploring this family of switches that can mostly get near the target specifications. In the future, this technology could improve its rise time and potentially be a viable product.

The requirements to drive the PPIGBT are impressive, it operates like a normal IGBT. The voltage and current capabilities are high enough that this IGBT can rival other switching technologies, however the microsecond rise times make this less useful for nanosecond applications.

The PPIGBT selected for this study is called the T0340VB45Gfrom IXYS.

The switching parameters to be used in the model are below:

- Voltage Rating: 4.5kV
- Pulsed Current Rating: 2.06kA
- Rise Time: 3.2us
- Switch Width: 100mm
- Switch Weight: 650g
- Switch Cost: $1,700
- Switch Triggering Circuitry Cost: $2.05

4.4 Capacitor Technologies to Compare

Three capacitor technologies that are widely used will be considered in this study. The following being: ceramic, film, and oil filled capacitors. In order to efficiently model these capacitors in the MATLAB algorithm, their trends associated with their energy stored versus cost will be used. There are further complexities associated with choosing the right capacitor, as different technologies can have a larger internal inductance which can make them worse for higher frequency applications. However, for the purpose of this study, just comparing how many dollars it will takes to supply a level of energy will suffice as a good estimate. In order to make the estimate even better, it is known that different brand names of manufacturers will sell the same product for a higher price. These products are not considered in this study in order to make it easier to form a trend of capacitors with similar pricing. Adding the overpriced capacitors will throw out any possible trend and will most likely not be used by an engineer trying to cut down on costs.

I also want to point out that the cost outputs for the capacitor plots may not exactly match up with the switch plots. After investigation of the cause, this is because of the logarithm point function used to generate the surface plots. For the capacitor plots, the maximum point values used as the input to the capacitor modeling function may be a little higher or lower compared to the point used in the switching model. To further verify, I forced in point values into the capacitor modeling code and the feasible points show much better correlation to the maximum points of the switch models.

4.4.1 Ceramic Capacitors

Ceramic capacitor values across varying energy levels can be seen in Table 4.2 below.

Digikey Part Number	**Price ($)**	**Weight (g)**	**Voltage (V)**	**Capacitance (F)**	**Energy J**	**Package Size**
587-1335-1-ND	0.34	0.01	630	2.20E-08	4.37E-03	1206
445-8883-1-ND	0.37	0.004	250	1.00E-07	3.13E-03	805
709-1028-1-ND	0.31	0.01	500	2.20E-08	2.75E-03	1206
709-1031-1-ND	0.24	0.01	1.00E+03	4.70E-09	2.35E-03	1206
709-1036-1-ND	0.14	0.01	2.00E+03	1.00E-09	2.00E-03	1206
445-2291-1-ND	0.3	0.01	630	1.00E-08	1.98E-03	1206
490-3512-1-ND	0.24	0.01	630	1.00E-08	1.98E-03	1206
399-6741-1-ND	0.29	0.004	500	1.00E-08	1.25E-03	805
445-2281-1-ND	0.22	0.004	250	2.20E-08	6.88E-04	805
445-2344-1-ND	0.4	0.01	630	2.20E-09	4.37E-04	1206
399-6744-1-ND	0.36	0.01	630	2.20E-09	4.37E-04	1206
399-7062-1-ND	0.35	0.004	1.00E+03	1.00E-11	5.00E-06	805
478-10475-6-ND	0.49	0.004	200	3.90E-11	7.80E-07	805
478-3844-1-ND	0.32	0.004	200	2.70E-11	5.40E-07	805
478-10484-1-ND	0.44	0.004	200	9.20E-12	1.84E-07	805
478-10273-1-ND	0.32	0.002	200	6.20E-12	1.24E-07	603
478-3849-1-ND	0.44	0.004	200	4.70E-12	9.40E-08	805
478-3846-1-ND	0.35	0.004	200	3.30E-12	6.60E-08	805

Table 4.2: Ceramic Capacitor Information Table

From this data, a fitted trend-line can be applied, which can be seen in the Figure 4.4 below.

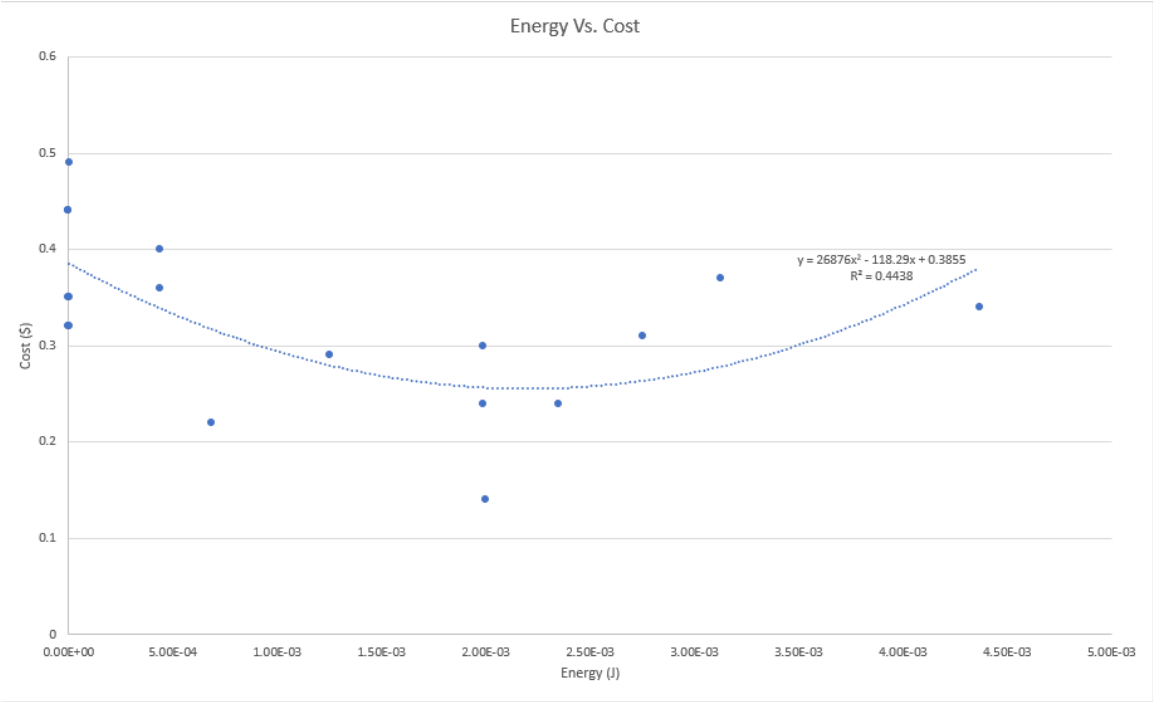


Figure 4.4: Polynomial fitted curve of energy versus cost of ceramic capacitors

Due to the variation of prices, the R^2 value of this curve is only .4438, which is a loosely fitted trend. However, it must be pointed out that the other trend lines have a worse R^2 value. The polynomial fit also is convenient since it allows the model to not come up with a negative cost value as it goes into lower energy levels. Even better, the curve shows a sweet spot that ceramic capacitors are the most viable to use.

4.4.2 Film Capacitors

Film capacitor values across varying energy levels can be seen in Table 4.3 below.

Digikey Part Number	**Price ($)**	**Weight (g)**	**Voltage (V)**	**Capacitance (F)**	**Energy J**
495-5037-1-ND	0.85	1	1500	4.70E-09	5.29E-03
PCF1426CT-ND	0.94	1	400	1.00E-08	8.00E-04
399-5419-ND	0.63	1	1250	1.00E-08	7.81E-03
PCF1430CT-ND	1.12	1	400	2.20E-08	1.76E-03
PCF1434CT-ND	1.4	1	400	4.70E-08	3.76E-03
EF2104-ND	0.29	1	250	1.00E-07	3.13E-03
BC1575-ND	1.4	3	1000	1.00E-07	5.00E-02
P14196-ND	0.62	1	450	1.50E-07	1.52E-02
399-5869-ND	0.65	3.59	630	4.70E-07	9.33E-02
399-11705-ND	1.41	10	630	1.00E-06	1.98E-01
399-5431-ND	2.83	0.275	760	1.00E-06	2.89E-01
495-4482-ND	3.98	50	1100	2.00E-06	1.21E+00
PCF1611-ND	0.86	50	450	2.20E-06	2.23E-01
399-5890-ND	1.45	0.030	560	2.20E-06	3.45E-01
B32774D1305K000-ND	4.32	50	1300	3.00E-06	2.54E+00
495-4832-ND	4.32	50	1100	5.00E-06	3.03E+00
495-3930-ND	6.13	50	1300	5.00E-06	4.23E+00
495-3934-ND	5.76	50	1100	7.00E-06	4.24E+00

Table 4.3: Film Capacitor Information Table

From this data, a fitted trend-line can be applied, which can be seen in the Figure 4.5 below.

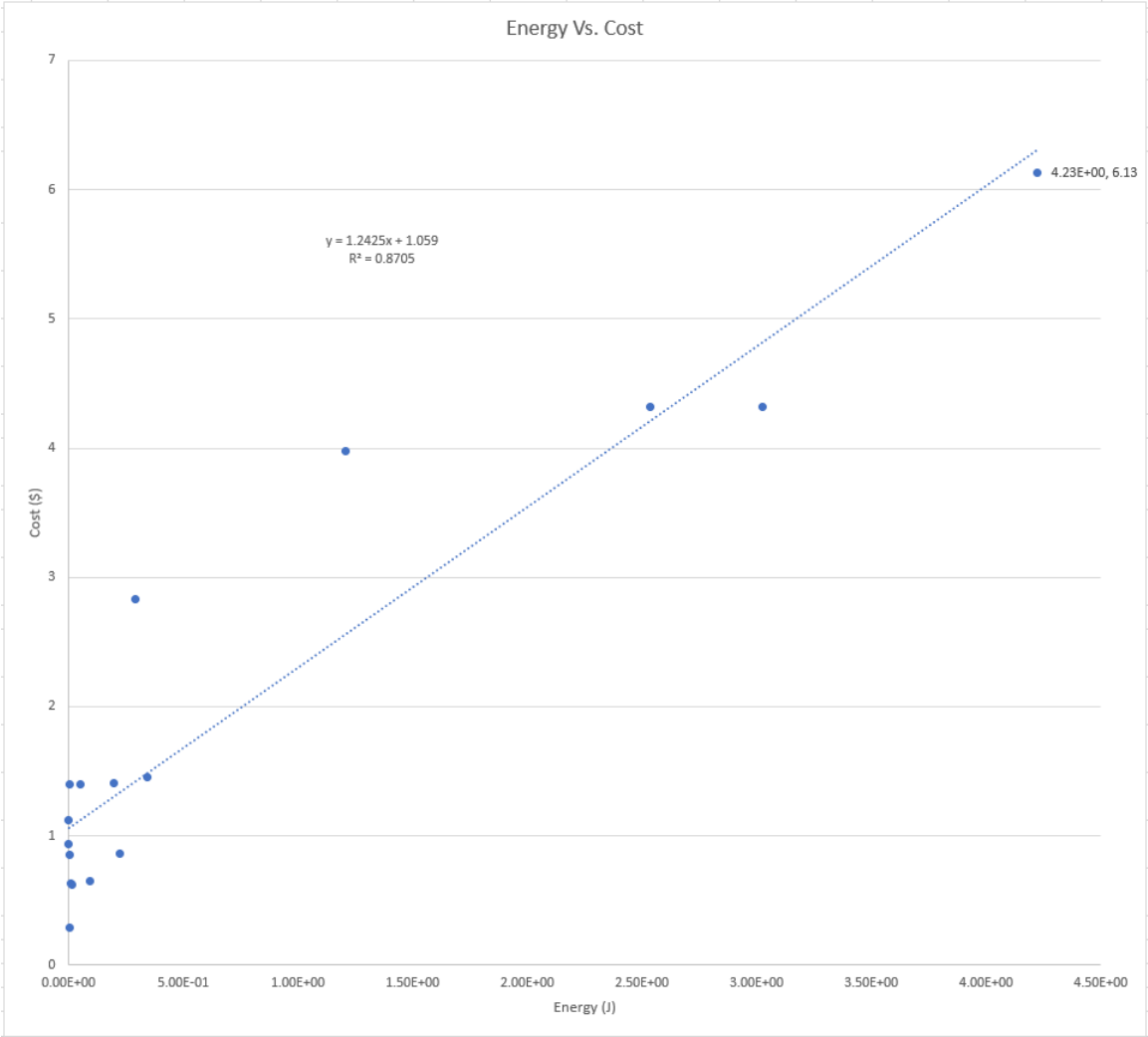


Figure 4.5: Linear fitted curve of energy versus cost of film capacitors

The R^2 value is .871 which is a good trend. In the search for parts, there were less film capacitors in the higher energy levels to choose from.

4.4.3 Oil Filled Capacitors

This capacitor technology is the most difficult to find good pricing for due to limited availability to consumers, and the fact that vendors require quotes for new oil filled capacitors.

Quotes make it hard to reliably find a trend with data, however a surplus site sells a range of oil filled capacitors and this data will be used for the purpose of the feasibility study as a good comparison. It should also be of note that using used capacitors will be much cheaper than newer ones, but their costs are still going to be high and their cost trends would remain similar.

From the site surplus sales, the following data has been collected in Table 4.4 below.

Price ($)	**Weight (g)**	**Voltage (V)**	**Capacitance (F)**	**Energy J**
225	1043.26	35000	3.00E-08	1.84E+01
1995	141974	15000	2.25E-04	2.53E+04
525	35380.2	50000	3.07E-07	3.84E+02
1895	53888.893	22000	5.20E-05	1.26E+04
1200	48589.958	25000	1.40E-05	4.38E+03
395	6350.29	4000	1.00E-05	8.00E+01

Table 4.4: Oil Filled Capacitor Information Table

A quick view from the Microsoft Excel plot comparing the energy versus cost of this capacitor technology gives the following curve in Figure 4.6 below.

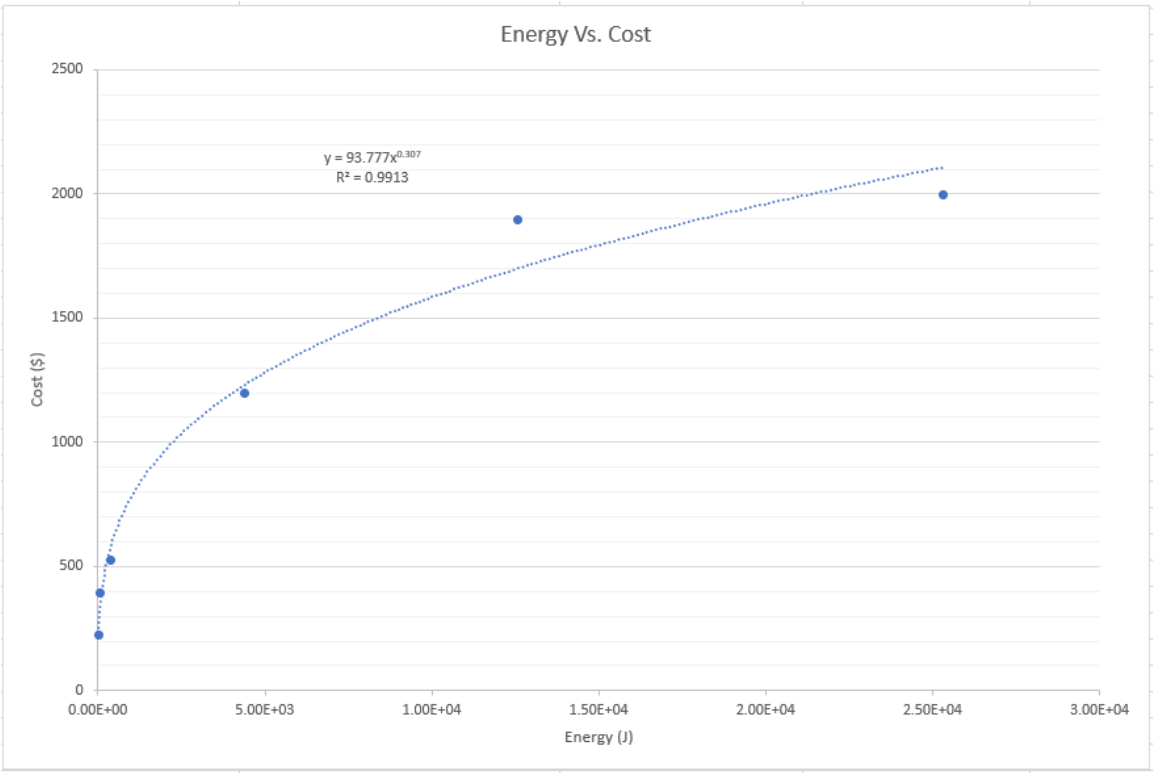


Figure 4.6: Power fitted curve of energy versus cost of oil filled capacitors

The R^2 value of this power fitted curve is .99 which shows a strong correlation. This is good considering the difficulty in finding useful oil filled capacitors from the surplus store.

In terms of getting a curve for comparing the amount of weight in grams that an oil filled capacitor is expected to have with a corresponding energy level, the following plot for this data can be seen below in Figure 4.7.

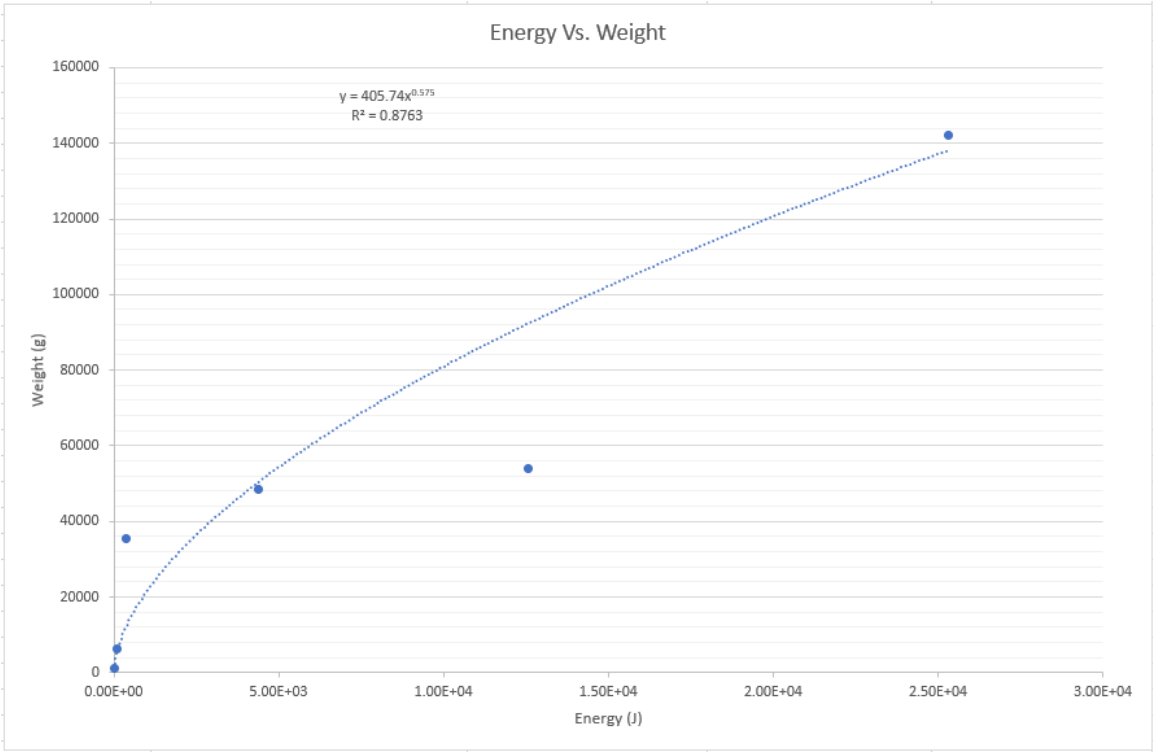


Figure 4.7: Power fitted curve of energy versus weight of oil filled capacitors

This power fitted curve shows a R^2 value of .88 which is still an okay correlation.

Overall, oil filled capacitors follow a power fitted curve where they are cost-prohibitive at low energy levels and start to level out in costs as the energy level increases.

4.5 MATLAB Model Results

This section will go over two models, one for getting modeling data of all the switches, and another that will have more stringent budget and rise time thresholds for actual use. The first part will show the feasibility of each technology, and the second part will show what technologies are even possible to use for my LTD application.

4.5.1 Overall Switching Comparison Results

For the first model of the LTD I am going to build, the following design parameters are listed in Table 4.5 below:

Parameter	**Value**
Voltage Output	30kV
Current Output	500A
Load Impedance	60 ohm
Energy Output	10kJ
Cost Threshold	$1,000,000
Rise Time Threshold	100,000s

Table 4.5: Table of user LTD parameter values

Note, that the cost threshold is set to $1,000,000 which is the maximum cost a government agency may want to pay for this technology and the rise time is set to 100,000 seconds to allow for modeling of the slower switches. The energy output is set to 10kJ to ensure that there is enough energy to have adequate results for all the switching technologies. In the next chapter, the total energy output will be different due to the output pulse of the LTD needing to only be an impulse at the minimum. The pulse length does not need to be extended. Also, the dielectric material category being used for the LTD will be polymide, which contains materials such as Kapton. A low-grade polymide will be used which has a dielectric strength of 3,400 Volts per Mil. For the purposes of comparison, it is assumed that polymides have a similar permittivity, which for Kapton is 3.4.

Now, the following modeling code parameters are listed in the Table 4.6 below:

Parameter	**Value**
Upper Limit of Logarithm Bound	10^5
Lower Limit of Logarithm Bound	10^1
Percent Voltage Rating	95%
Percent Current Rating	95%
Percent Stage Current Rating	110%
Logic Stage	1
PCTthres	90%
PCTthres2	5%
Tolerance Constant	0.01

Table 4.6: Table of user code performance values

Note that for my purposes, the logic stage is set to one and logic cost has been set to $30.64 for each switch. This will be discussed further in another chapter, but it has been found that a fiber optic connection to each individual stage will bring out the best switching performance. The logic cost is only considering the cost of a single mode fiber optic receiver. This is the most expensive component for the logic entry in a LTD stage, thus will still work for the model.

The switches and capacitors discussed in the last sections have been loaded into the LTD modeling code.

Comparison of Different Switching Technologies

The surface plots below will show the dollar value in logarithmic scale for each pair of voltage and current parameters comparing different switching technologies. Since the output pulse length is not of concern, energy does not need to be plotted as it will be a constant. The

main parameters of interest are the voltage output which will help drive a spark gap switch faster from the LTD and the current which will help drive more switches from one LTD. Also of note is the load impedance. If the voltage becomes high enough, the user defined current of 500A will not be used, and the program will change over to the voltage over load impedance current if it is greater than the user defined current of 500A.

The PMOSFET surface plot can be seen in Figure 4.8 below.

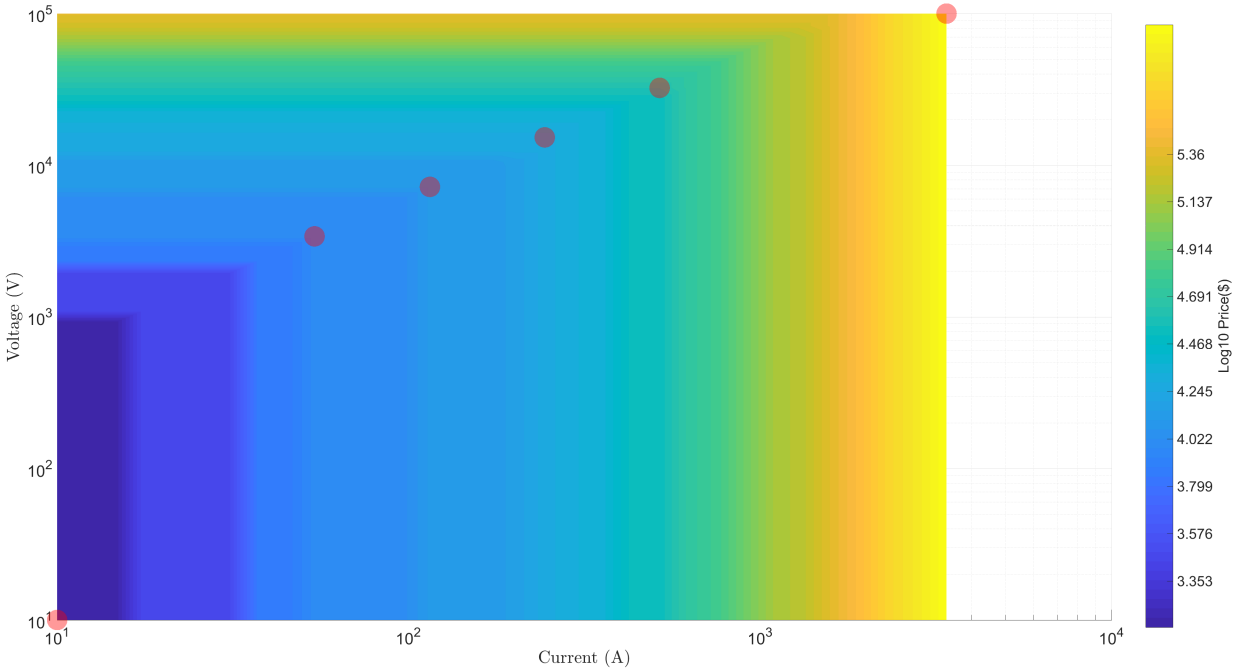


Figure 4.8: PMOSFET surface plot at 60 Ω load resistance

From the surface plot, a table of values can be made highlighting the different points. The maximum and minimum points will be used, along with the target specification voltage of 30kV and 500A. Different percentages of the target specification values will be used as well. Using varying percentages of the target specification will be useful in revealing any trends in the overall pricing. Sometimes the pricing could be a linear trend, but other times it could get more expensive the lower the voltages and currents. These trends come from the

capacitor technologies used for each point, which as can be read from the previous sections, may not be linear. The data points collected in the table would give a good representation of how each switching and capacitor technology compares to each other.

The values from the PMOSFET surface plot can be seen in Table 4.7 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	100,000	5,964	931,108
∼Target Spec Point	32,370	518	39,719
1/2 Target Spec Point	15,260	244	18,323
1/4 Target Spec Point	7,197	115	13,152
1/8 Target Spec Point	3,393	54	9,931
Minimum Point	10	10	1,365

Table 4.7: Table of PMOSFET test values from the surface plot for model 1

The SiC MOSFET surface plot can be seen in Figure 4.9

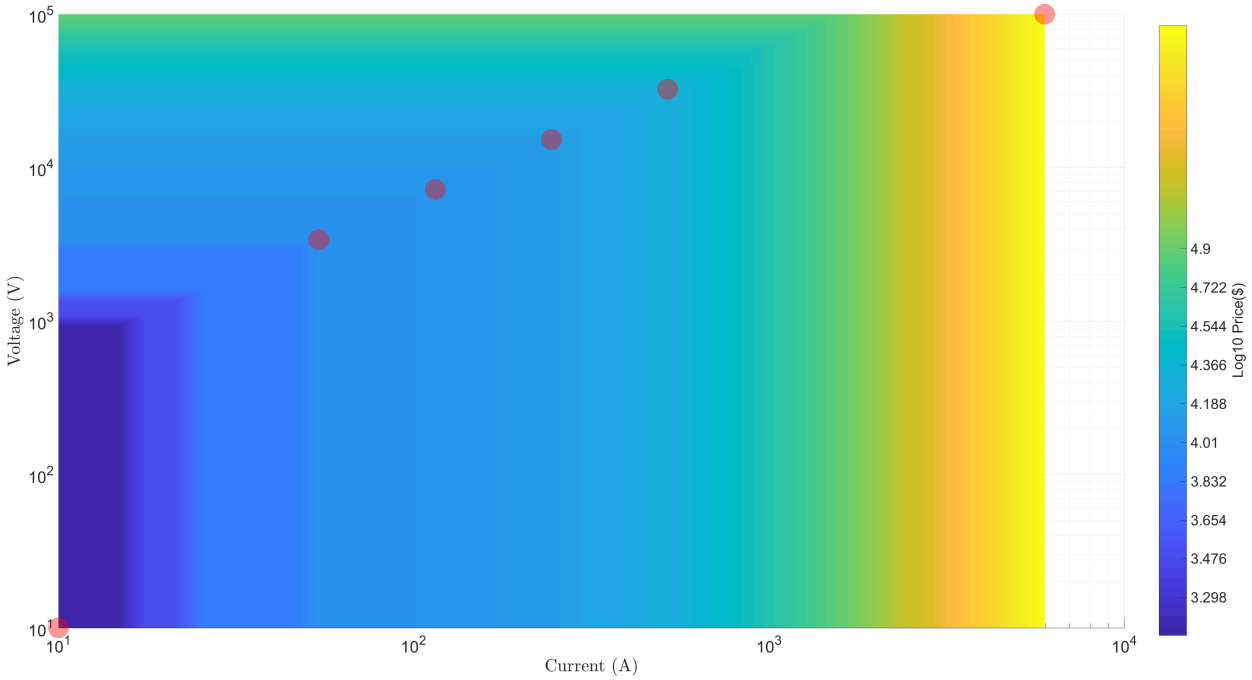


Figure 4.9: SiC MOSFET surface plot at 60 Ω load resistance

A table of values from the SiC MOSFET surface plot can be seen in Table 4.8 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	100,000	5,964	843,335
∼Target Spec Point	32,370	518	20,417
1/2 Target Spec Point	15,260	244	13,152
1/4 Target Spec Point	7,197	115	11,561
1/8 Target Spec Point	3,393	54	10,495
Minimum Point	10	10	1,330

Table 4.8: Table of SiC MOSFET test values from the surface plot for model 1

The IGBT surface plot can be seen in Figure 4.10 below.

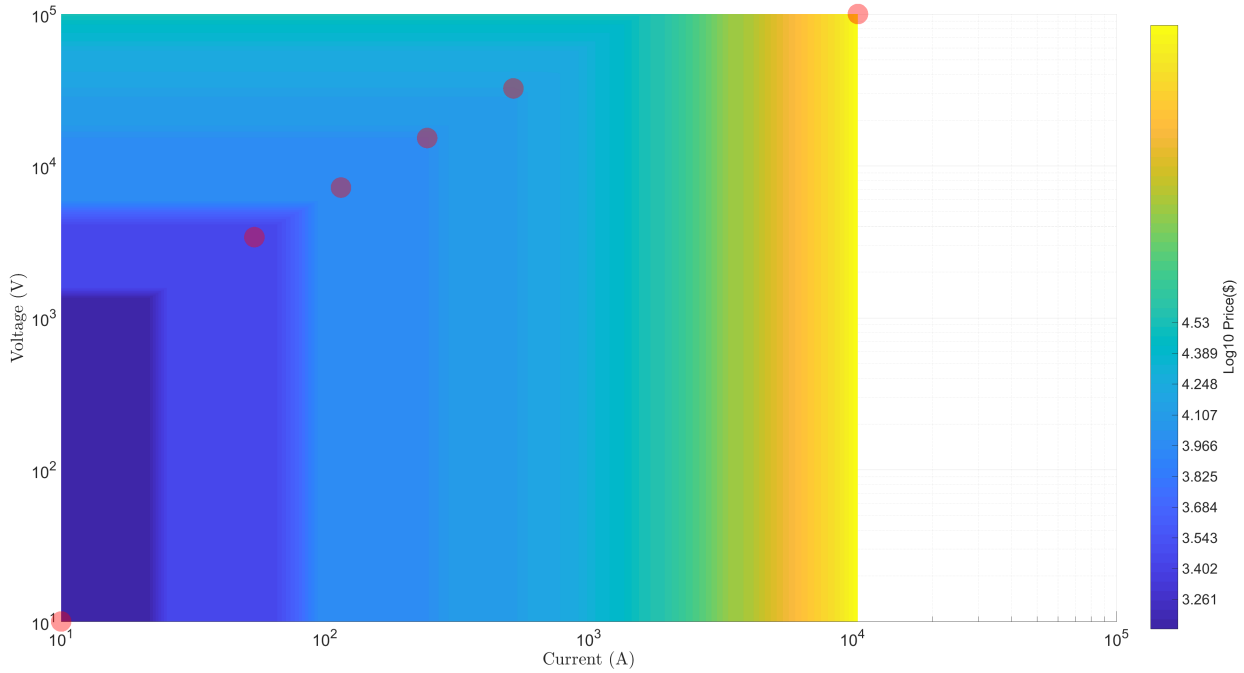


Figure 4.10: IGBT surface plot at 60 Ω load resistance

A table of values from the IGBT surface plot can be seen in Table 4.9 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	100,000	10,480	106,660
∼Target Spec Point	32,370	518	14,521
1/2 Target Spec Point	15,260	244	9,705
1/4 Target Spec Point	7,197	115	9,376
1/8 Target Spec Point	3,393	54	2,904
Minimum Point	10	10	1,334

Table 4.9: Table of IGBT test values from the surface plot for model 1

The PPIGBT surface plot can be seen in Figure 4.11 below.

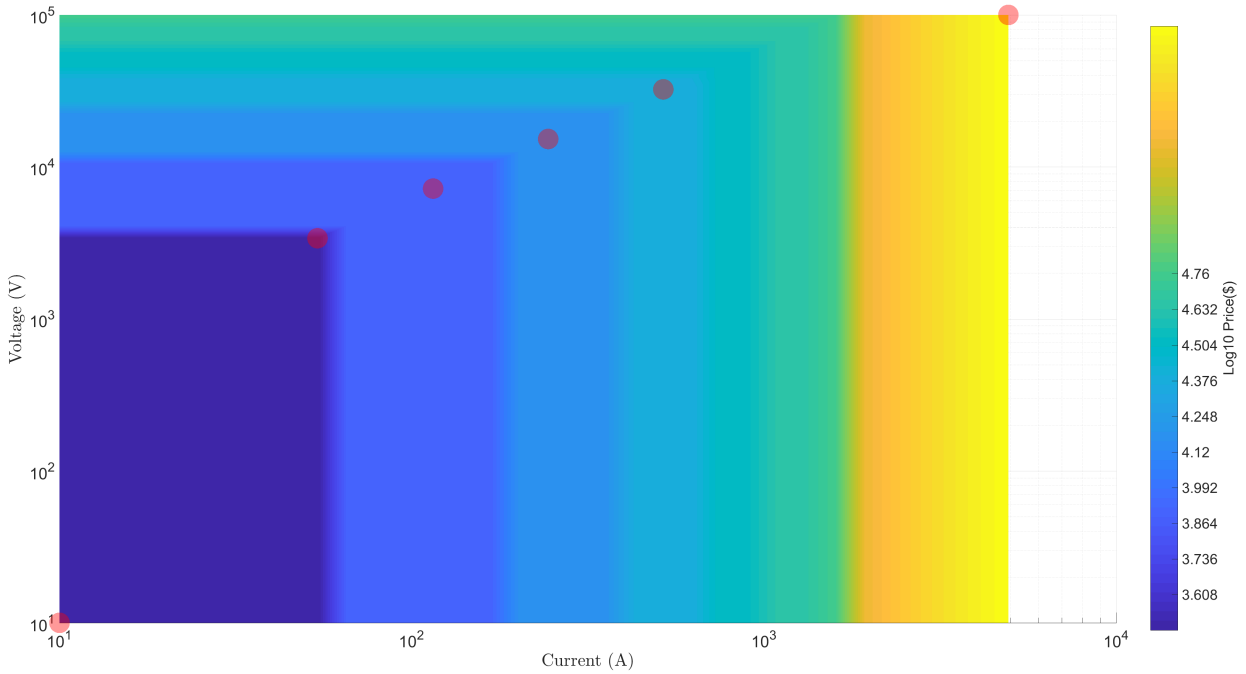


Figure 4.11: PPIGBT surface plot at 60 Ω load resistance

A table of values from the PPIGBT surface plot can be seen in Table 4.10 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	100,000	4,942	445,656
∼Target Spec Point	32,370	518	23,281
1/2 Target Spec Point	15,260	244	14,894
1/4 Target Spec Point	7,197	115	7,980
1/8 Target Spec Point	3,393	54	3,027
Minimum Point	10	10	3,027

Table 4.10: Table of PPIGBT test values from the surface plot for model 1

The spark gap surface plot can be seen in Figure 4.12 below.

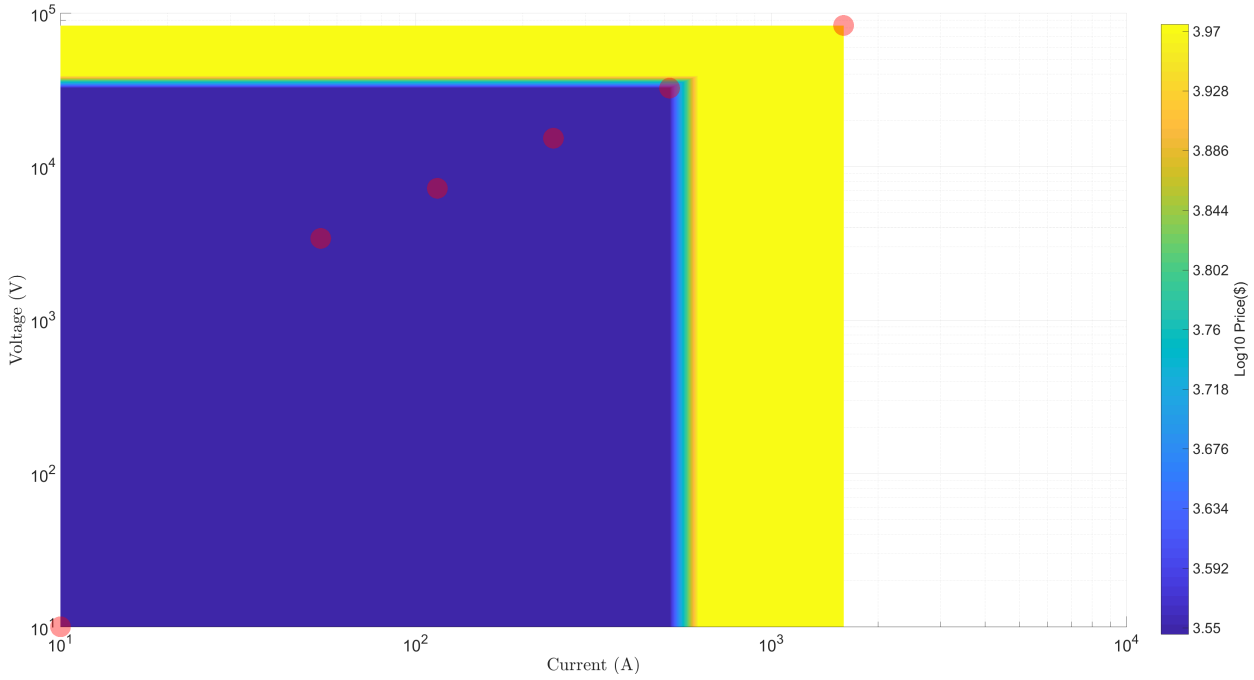


Figure 4.12: Spark gap surface plot at 60 Ω load resistance

A table of values from the spark gap surface plot can be seen in Table 4.11 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	82,860	1,600	9,441
∼Target Spec Point	32,370	518	3,508
1/2 Target Spec Point	15,260	244	3,508
1/4 Target Spec Point	7,197	115	3,508
1/8 Target Spec Point	3,393	54	3,508
Minimum Point	10	10	3,508

Table 4.11: Table of spark gap test values from the surface plot for model 1

Overall, clear price trends can be seen amongst all the switches. The spark gap switch is the cheapest switch by far, however as will be seen in the next sections, its rise time will make it

not feasible for the 10ns rise time requirement. Also, the spark gap switch and the PPIGBT can do far voltages and currents than provided by the surface plot. The 10kJ energy level used for this study would not provide for enough energy to allow the switches to get larger voltage and current values. As all the switches being compared are reaching the target specification values, there is no need to increase the energy level for this study. When comparing the solid-state switches, the PMOSFET is the most expensive at the target specification value. The SiC MOSFET is a little more than half of the cost of the PMOSFET at the same value. The IGBT is about half the amount of the SiC MOSFET. The PPIGBT is in between the price of using SiC MOSFETs and IGBTs. If my selection based upon solid-state switch technology was based upon costs, the IGBT would be the superior switch.

Comparison of Different Capacitor Technologies

The surface plots below will show the dollar value in logarithmic scale for each pair of voltage and current parameters comparing different capacitor technologies. The costs include the capacitor technology cost with the cheapest feasible switch.

The ceramic capacitor surface plot can be seen in Figure 4.13 below.

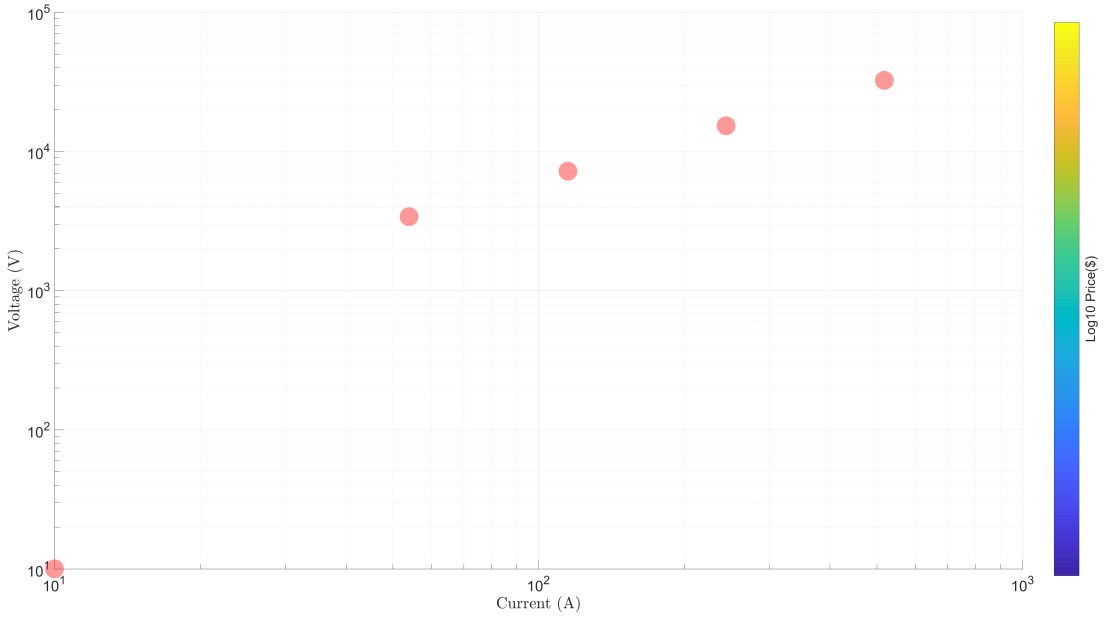


Figure 4.13: Ceramic capacitor surface plot at 60 Ω load resistance

A table of values using the same points as in the switching technology comparison section can be seen for the ceramic capacitor in Table 4.12 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	NaN	NaN	NaN
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	NaN	NaN	NaN
1/4 Target Spec Point	NaN	NaN	NaN
1/8 Target Spec Point	NaN	NaN	NaN
Minimum Point	NaN	NaN	NaN

Table 4.12: Table of ceramic capacitor test values from the surface plot for model 1

The film capacitor surface plot can be seen in Figure 4.14 below.

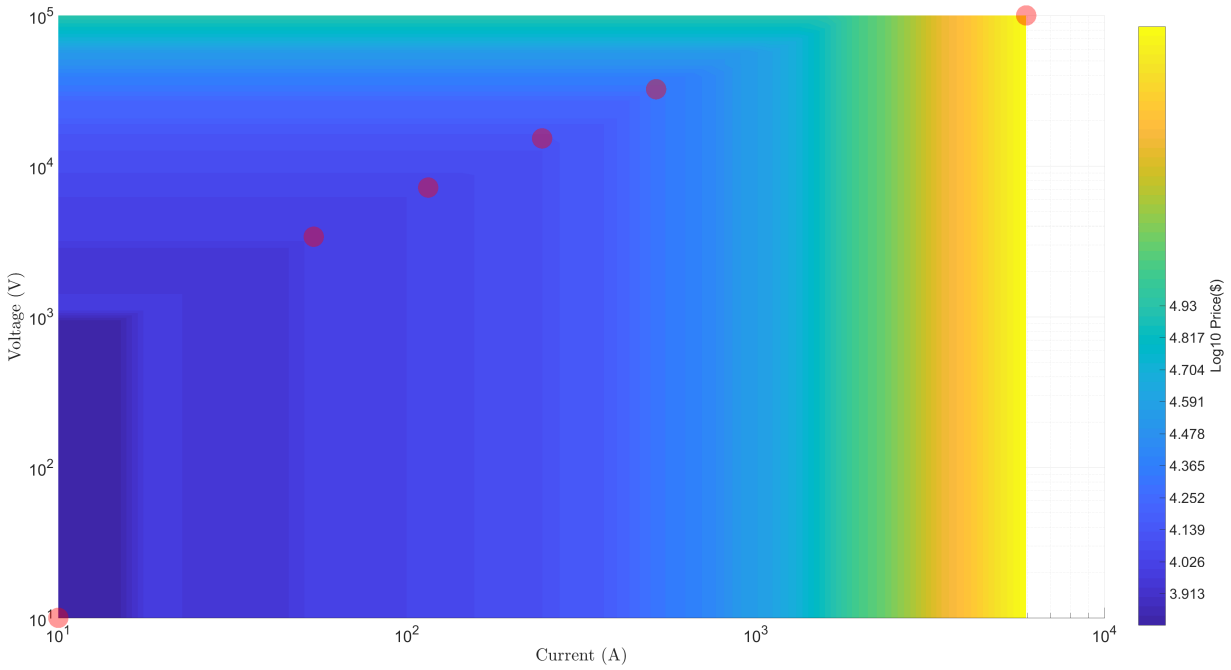


Figure 4.14: Film capacitor surface plot at 60 Ω load resistance

A table of values for the film capacitor can be seen in Table 4.13 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	100,000	5,964	824,138
∼Target Spec Point	32,370	518	20,701
1/2 Target Spec Point	15,260	244	13,243
1/4 Target Spec Point	7,197	115	11,455
1/8 Target Spec Point	3,393	54	10,520
Minimum Point	10	115	6,339

Table 4.13: Table of film capacitor test values from the surface plot for model 1

The oil filled capacitor surface plot can be seen in Figure 4.15 below.

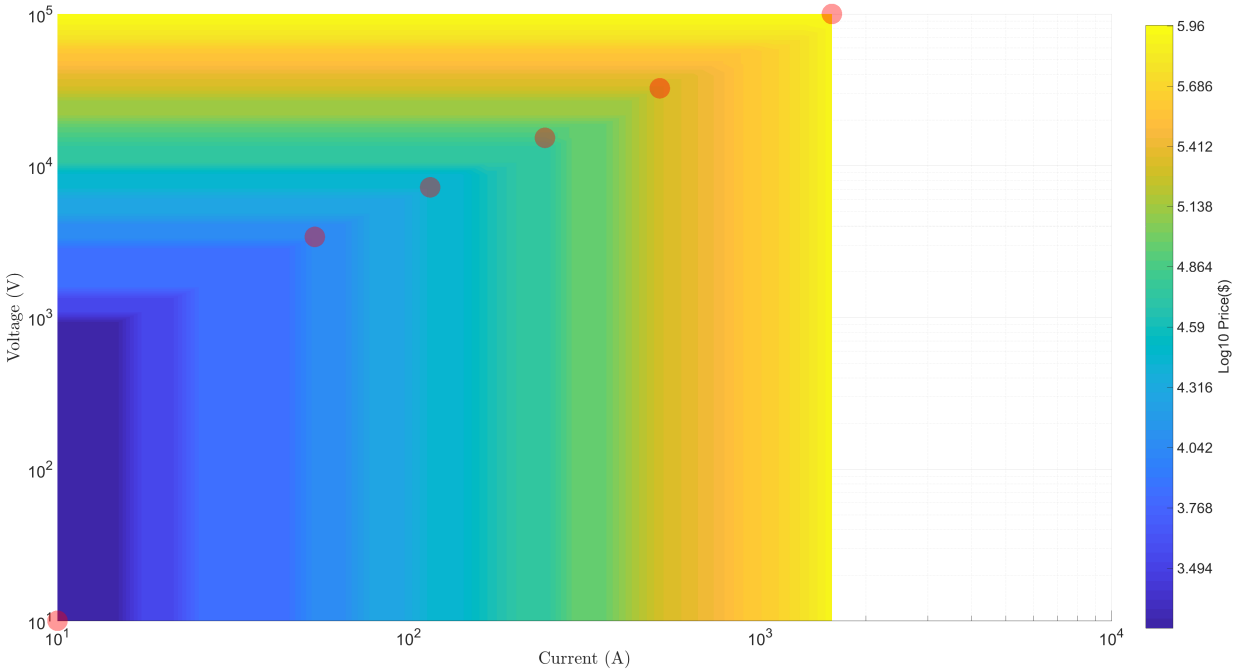


Figure 4.15: Oil filled capacitor surface plot at 60 Ω load resistance

A table of values for the oil filled capacitor can be seen in Table 4.14 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	100,000	1,600	918,333
∼Target Spec Point	32,370	518	204,644
1/2 Target Spec Point	15,260	244	70,146
1/4 Target Spec Point	7,197	115	27,416
1/8 Target Spec Point	3,393	54	11,668
Minimum Point	10	115	1,667

Table 4.14: Table of oil filled capacitor test values from the surface plot for model 1

Clear differences can be seen amongst all the capacitor technologies. At 10kJ, the ceramic

capacitor has a narrow region of feasibility. I have checked the code by lowering the energy level used, and the region of feasibility for the ceramic capacitor does increase. This makes sense as the cost of the ceramic capacitor is a parabolic model and has sharp price increases when deviating away from its optimal energy level. The film capacitor is greatly cheaper than the ceramic capacitor, and even cheaper than the oil filled capacitor. This makes the film capacitor the best choice for low energy output applications. If I were to increase the energy level to 1MJ, then I would be saying the same for the oil filled capacitor due to how its price eventually plateaus as the energy goes up.

4.5.2 LTD Specification Comparison Results

For the second model, the stringent LTD design specifications have been added in by making the rise time threshold 10ns and the budget $100,000. This value will be explained further in the next chapter, but in order to meet the sizing requirements, I must use ceramic capacitors as film capacitors are too large. This meant cutting the energy output down to approximately 7J to be feasible. The parameters loaded into the model can be seen in Table 4.15 below.

Parameter	**Value**
Voltage Output	30kV
Current Output	500A
Load Impedance	60 ohm
Energy Output	7J
Cost Threshold	$100,000
Rise Time Threshold	10ns

Table 4.15: Table of user LTD parameters

Now, the following modeling code parameters are listed in Table 4.16 below:

Parameter	**Value**
Upper Limit of Logarithm Bound	10^4
Lower Limit of Logarithm Bound	10^1
Percent Voltage Rating	95%
Percent Current Rating	95%
Percent Stage Current Rating	110%
Logic Stage	1
PCTthres	90%
PCTthres2	5%
Tolerance Constant	0.01

Table 4.16: Table of user code performance parameters

Comparison of Different Switching Technologies

The resulting surface plots are shown below. The first being the PMOSFET surface plot which can be seen in Figure 4.16 below.

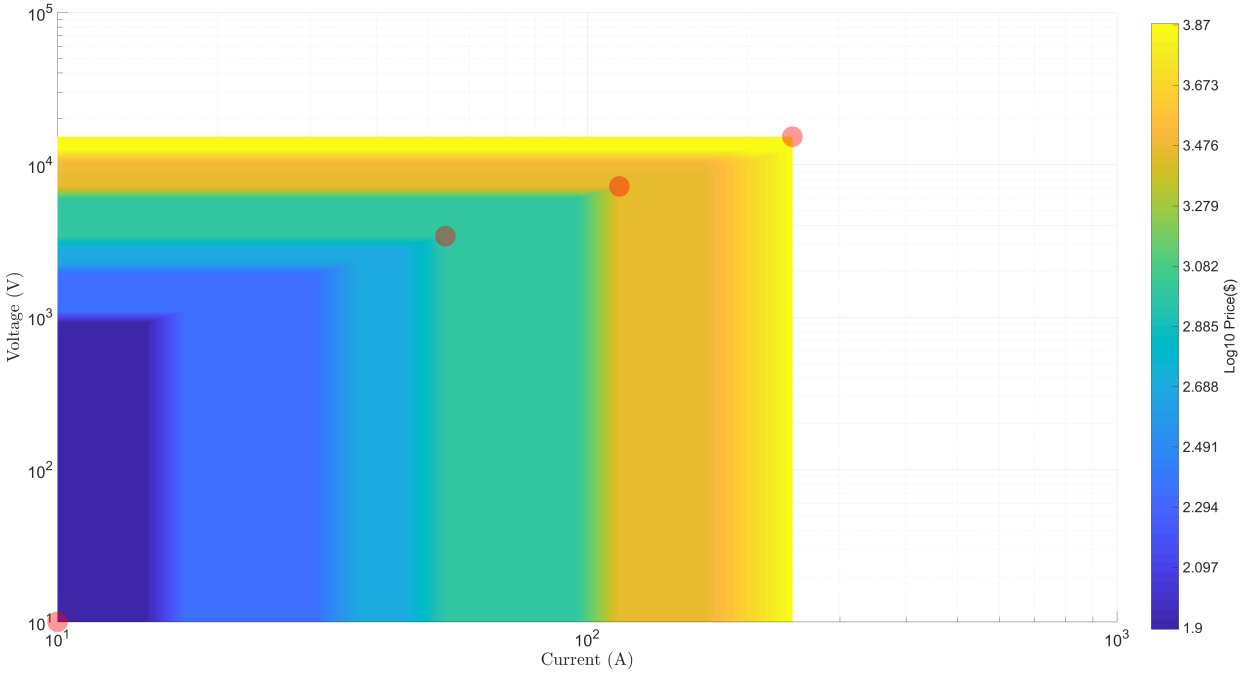


Figure 4.16: PMOSFET surface plot at 60 Ω load resistance

A table of values from the PMOSFET surface plot can be seen in Table 4.17 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	15,260	244	7,499
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	15,260	244	7,499
1/4 Target Spec Point	7,197	115	2,938
1/8 Target Spec Point	3,393	54	977
Minimum Point	10	10	79

Table 4.17: Table of PMOSFET test values from the surface plot for model 2

The SiC MOSFET surface plot can be seen in Figure 4.17 below.

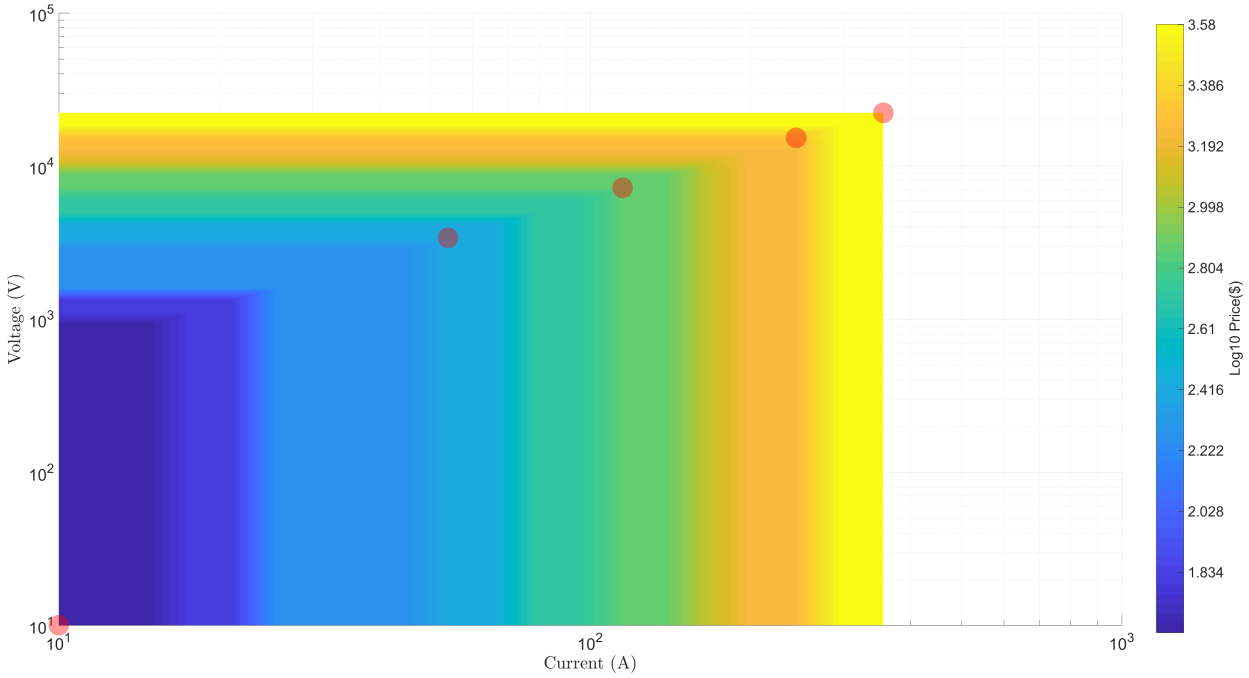


Figure 4.17: SiC MOSFET surface plot at 60 Ω load resistance

A table of values from the SiC MOSFET surface plot can be seen in Table 4.18 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	22,230	356	3,811
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	15,260	244	1,928
1/4 Target Spec Point	7,197	115	731
1/8 Target Spec Point	3,393	54	261
Minimum Point	10	10	44

Table 4.18: Table of SiC MOSFET test values from the surface plot for model 2

The IGBT surface plot can be seen in Figure 4.18 below.

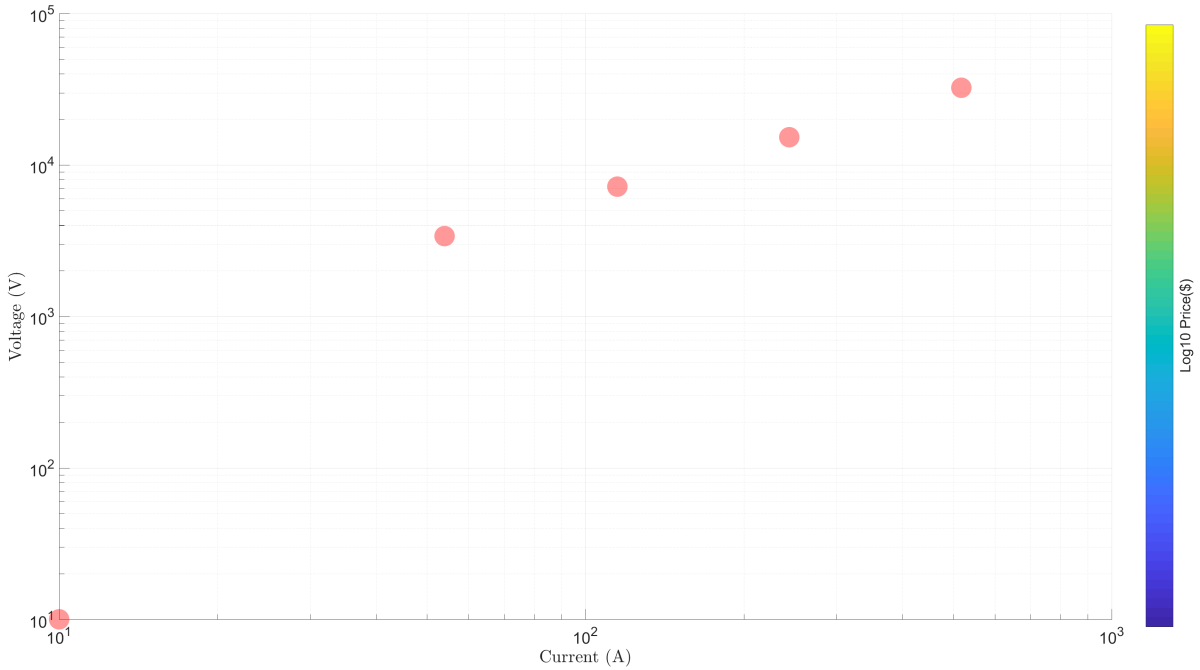


Figure 4.18: IGBT surface plot at 60 Ω load resistance

A table of values from the IGBT surface plot can be seen in Table 4.19 below. Note, that the IGBT is not feasible for the specifications set due to its rise time being just above 10ns. The use of over driving and cascoding topology could make it feasible, thus I should not rule out the IGBT completely.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	NaN	NaN	NaN
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	NaN	NaN	NaN
1/4 Target Spec Point	NaN	NaN	NaN
1/8 Target Spec Point	NaN	NaN	NaN
Minimum Point	NaN	NaN	NaN

Table 4.19: Table of IGBT test values from the surface plot for model 2

The PPIGBT surface plot can be seen in Figure 4.19 below.

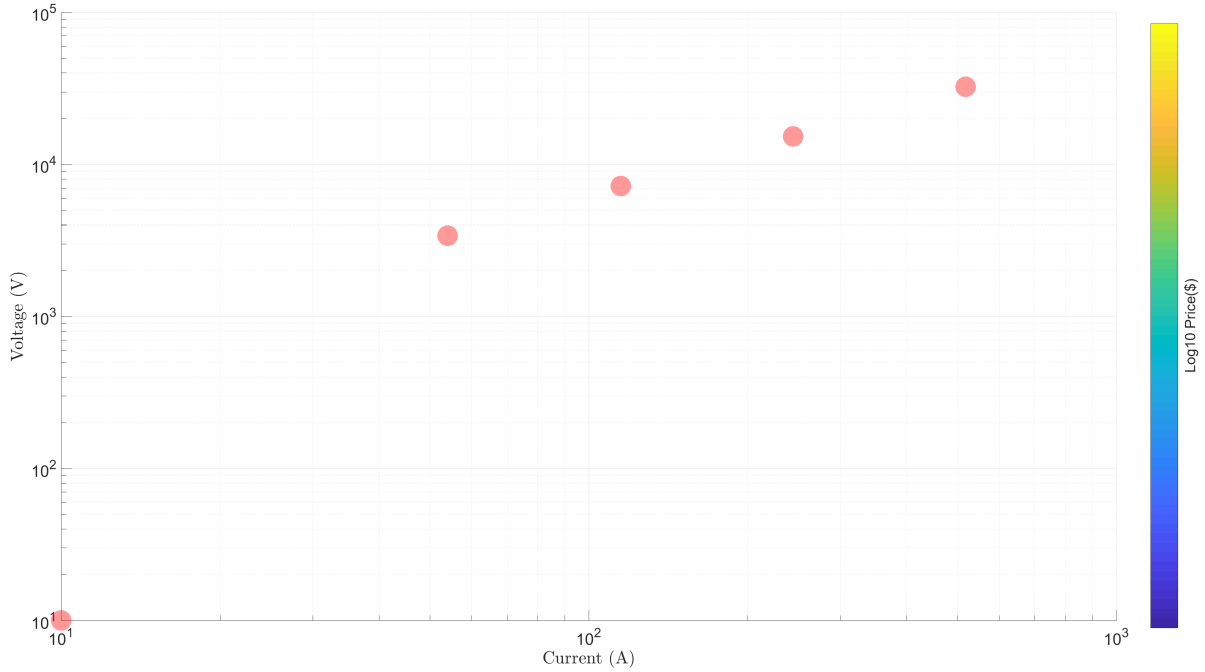


Figure 4.19: PPIGBT surface plot at 60 Ω load resistance

A table of values from the PPIGBT surface plot can be seen in Table 4.20 below. Note, that the PPIGBT is not feasible for the specifications set due to its long rise time.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	NaN	NaN	NaN
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	NaN	NaN	NaN
1/4 Target Spec Point	NaN	NaN	NaN
1/8 Target Spec Point	NaN	NaN	NaN
Minimum Point	NaN	NaN	NaN

Table 4.20: Table of PPIGBT test values from the surface plot for model 2

The spark gap surface plot can be seen in Figure 4.20 below.

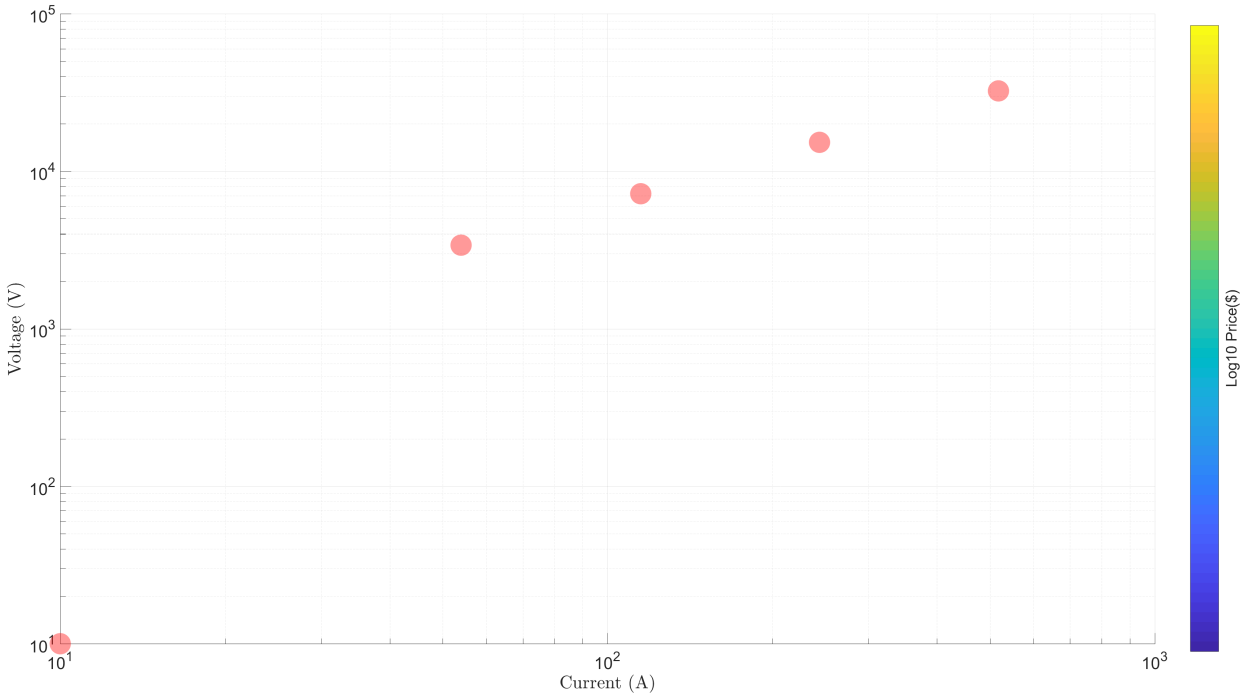


Figure 4.20: Spark gap surface plot at 60 Ω load resistance

A table of values from the spark gap surface plot can be seen in Table 4.21 below. Note,

that the spark gap is not feasible for the specifications set due to its long rise time.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	NaN	NaN	NaN
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	NaN	NaN	NaN
1/4 Target Spec Point	NaN	NaN	NaN
1/8 Target Spec Point	NaN	NaN	NaN
Minimum Point	NaN	NaN	NaN

Table 4.21: Table of spark gap test values from the surface plot for model 2

As can be seen, only the PMOSFET and the SiC MOSFET with their stated rise time parameters in their specification sheets can meet the 10ns rise time requirement. The SiC MOSFET is still cheaper than the PMOSFET. However, the maximum voltage attained is 22.23kV with 356A current. This is a little bit under the needed value for the target specification. Thus, with no changes, no solid-state technology exists in the commercial market that can fulfill my target specifications without over driving the gate or using topologies such as cascoding. Decreasing the length of the LTD can also help bring in more voltage, however ergonomics must be considered when going to make LTD stages right next to each other. It is possible to make the stages closer together, however this will come at a loss in being able to service the LTD without removing all the components. Also, the thinner the stages, the less mechanical options that are available in containing the transformer core and keeping the PCB all together. Making the transformer core thinner is also not advised since the Metglas manufacturer informed me that it would make the core too fragile, thus risky to use.

Comparison of Different Capacitor Technologies

The capacitor surface plots for this second model can be seen in this section. The ceramic capacitor surface plot can be seen in Figure 4.21 below.

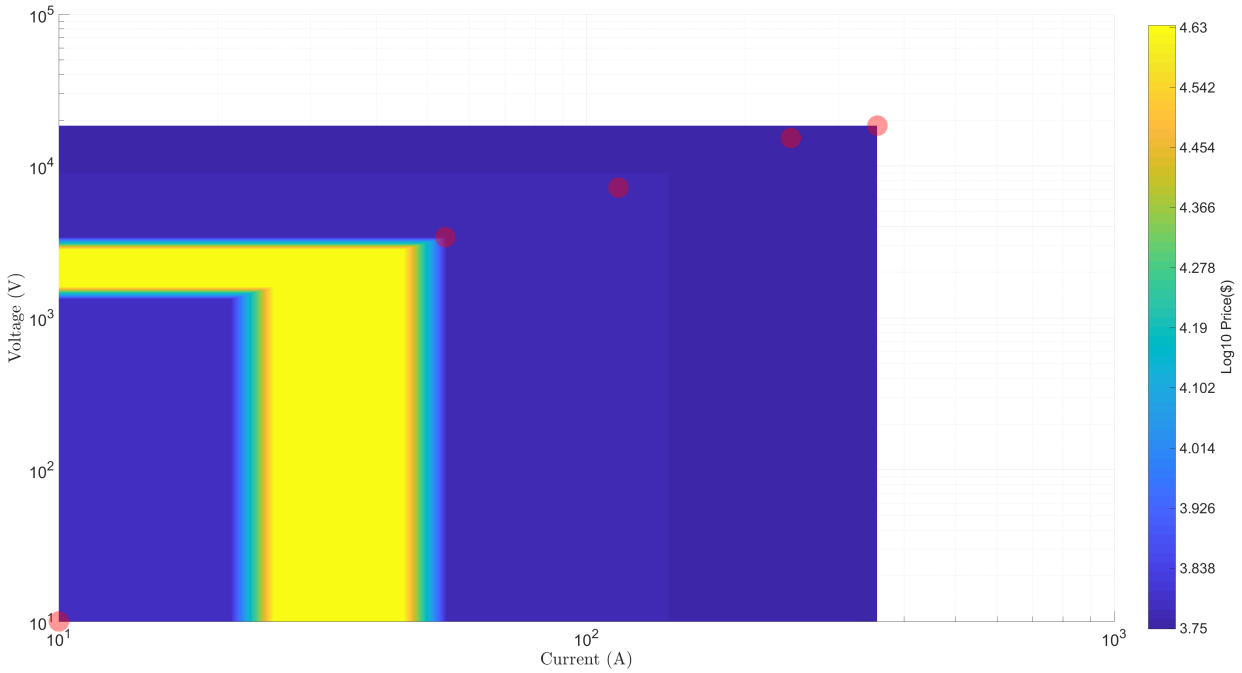


Figure 4.21: Ceramic capacitor surface plot at 60 Ω load resistance

A table of values from the ceramic capacitor surface plot can be seen in Table 4.22 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	18,420	356	5,610
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	15,260	244	5,610
1/4 Target Spec Point	7,197	115	5,808
1/8 Target Spec Point	3,393	54	5,902
Minimum Point	10	10	6,152

Table 4.22: Table of ceramic capacitor test values from the surface plot for model 2

The film capacitor surface plot can be seen in Figure 4.22 below.

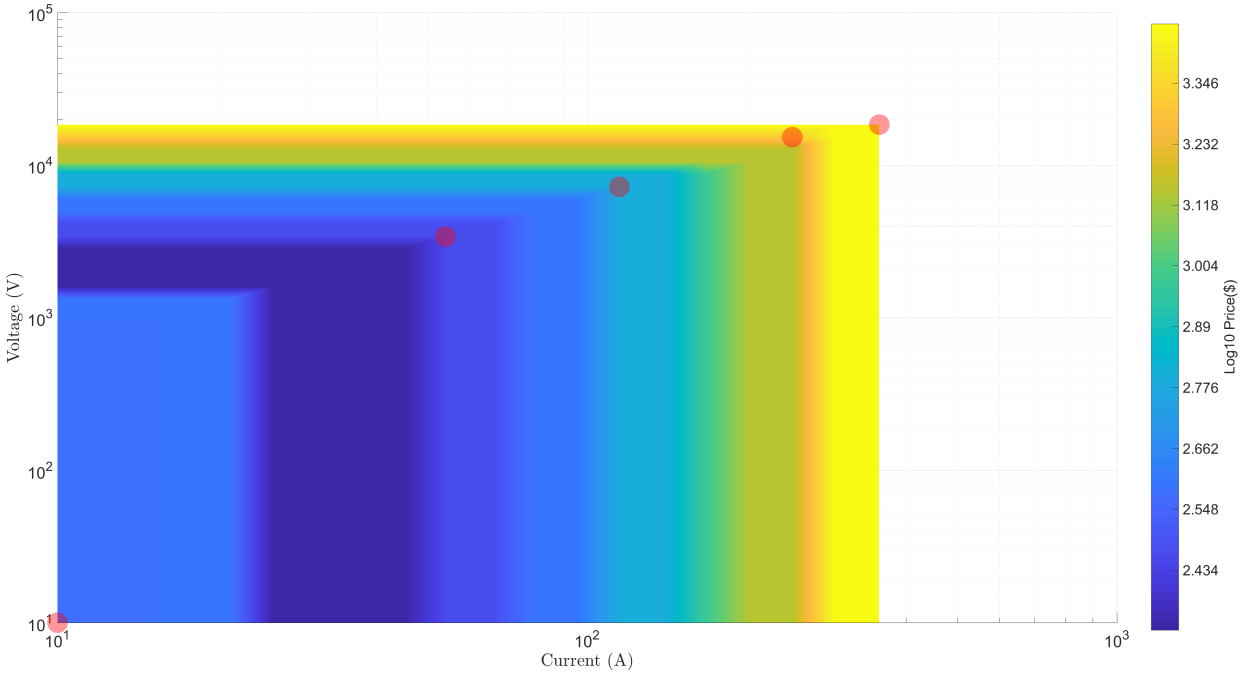


Figure 4.22: Film capacitor surface plot at 60 Ω load resistance

A table of values from the film capacitor surface plot can be seen in Table 4.23 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	18,420	356	2,864
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	15,260	244	2,056
1/4 Target Spec Point	7,197	115	608
1/8 Target Spec Point	3,393	54	292
Minimum Point	10	10	381

Table 4.23: Table of film capacitor test values from the surface plot for model 2

The oil filled capacitor surface plot can be seen in Figure 4.23 below.

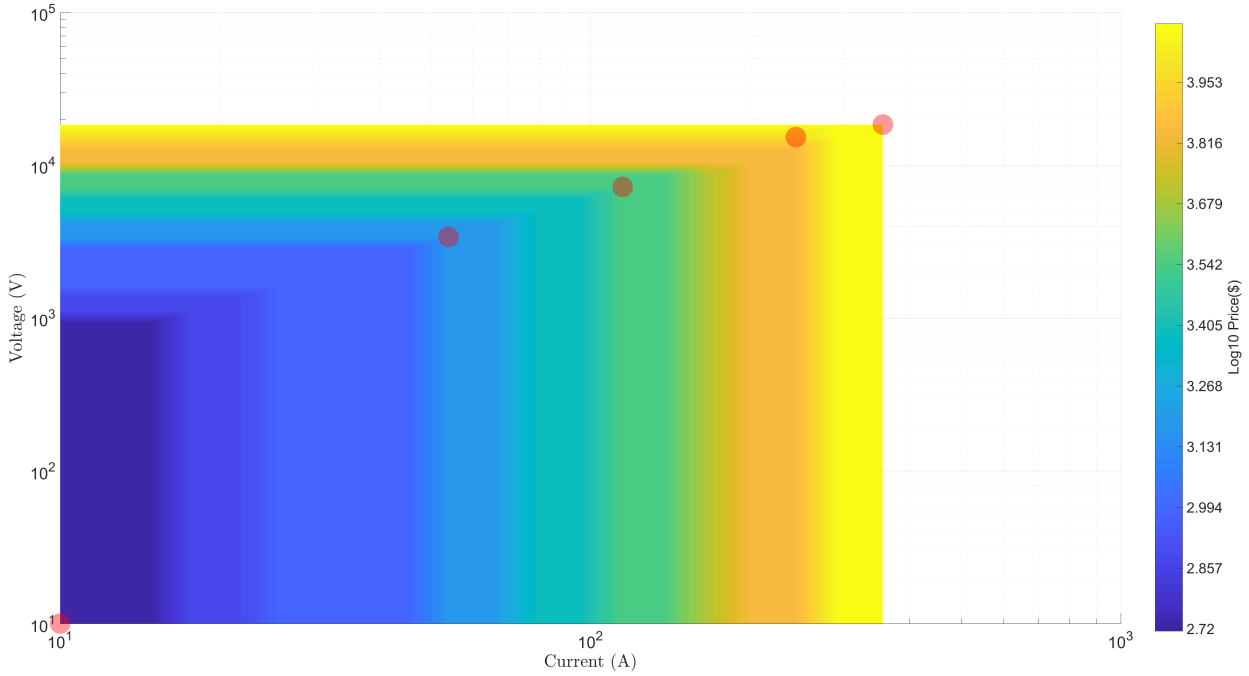


Figure 4.23: Oil filled capacitor surface plot at 60 Ω load resistance

A table of values from the oil filled capacitor surface plot can be seen in Table 4.24 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	18,420	356	50,350
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	15,260	244	40,832
1/4 Target Spec Point	7,197	115	16,181
1/8 Target Spec Point	3,393	54	8,453
Minimum Point	10	115	1,667

Table 4.24: Table of oil filled test values from the surface plot for model 2

Keep in mind that no switch has achieved the target specifications, thus the capacitor surface plots would not as well. However, clear comparisons can be made. The oil filled capacitor is not feasible at all for my LTD application due to a cost of $50,350 at only 18.42kV. The film capacitor is still feasible due to its cost of $2,864 at 18.42kV. It is important to keep in mind the size of the film capacitor, and in the market, these capacitors are around an inch in length for a 2kV rated capacitor. Thus, they would not work for my compact application. This is also why the energy level has been dropped down to 7J since ceramic capacitors need to be used. When looking at ceramic capacitors, their cost is at $5,610 at 18.42kV. They are about double the cost of film, but are necessary in order to keep my LTD compact. The cost of the ceramic film is still relatively cheap since I am keeping the entire LTD cost under $100,000 overall.

4.5.3 LTD With Over-Driven Switches Specification Comparison Results

This section will compare different switching technologies when the solid-state switches are over-driven with current. Cascode will not be considered in this comparison. Simply, each

solid-state switch except the PPIGBT (due to an already large rise time) will have their rise time reduced down to 1ns.

A table of user LTD parameter values can be seen in Table 4.25 below.

Parameter	**Value**
Voltage Output	30kV
Current Output	500A
Load Impedance	60 ohm
Energy Output	7J
Cost Threshold	$100,000
Rise Time Threshold	10ns

Table 4.25: Table of user LTD parameter values

The following modeling code parameters are listed in Table 4.26 below:

Parameter	**Value**
Upper Limit of Logarithm Bound	10^5
Lower Limit of Logarithm Bound	10^4
Percent Voltage Rating	95%
Percent Current Rating	95%
Percent Stage Current Rating	110%
Logic Stage	1
PCTthres	90%
PCTthres2	5%
Tolerance Constant	0.01

Table 4.26: Table of user code performance parameters values

Comparison of Different Switching Technologies

As was seen in the LTD specification surface plots, the PPIGBT and spark gap would not have a rise time anywhere near the rise time that we need and have no feasible points on the plots. Thus, they will not appear in this section.

The PMOSFET surface plot can be seen in Figure 4.24 below.

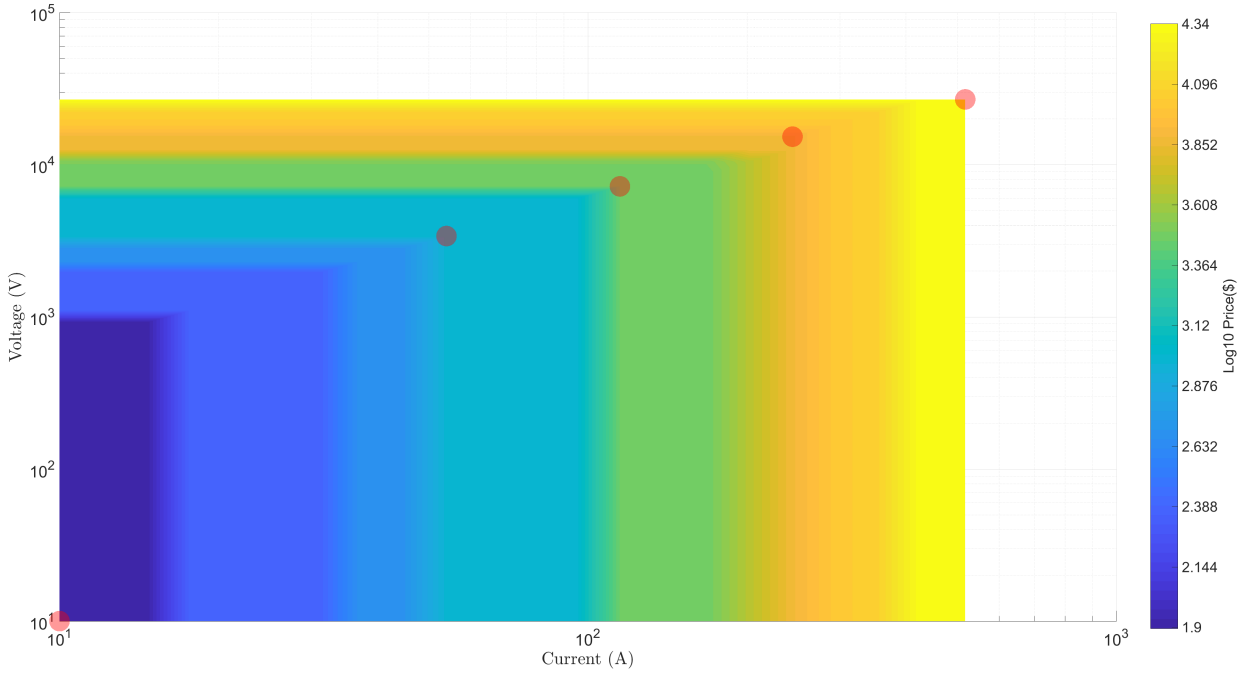


Figure 4.24: PMOSFET surface plot at 60 Ω load resistance

The table of values generated from the PMOSFET surface plot can be seen in Table 4.27 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	26,830	518	21,928
∼Target Spec Point	NaN	NaN	NaN
1/2 Target Spec Point	15,260	244	7,499
1/4 Target Spec Point	7,197	115	2,938
1/8 Target Spec Point	3,393	54	977
Minimum Point	10	10	79

Table 4.27: Table of PMOSFET test values from the surface plot for model 3

The SiC MOSFET surface plot can be seen in Figure 4.25 below.

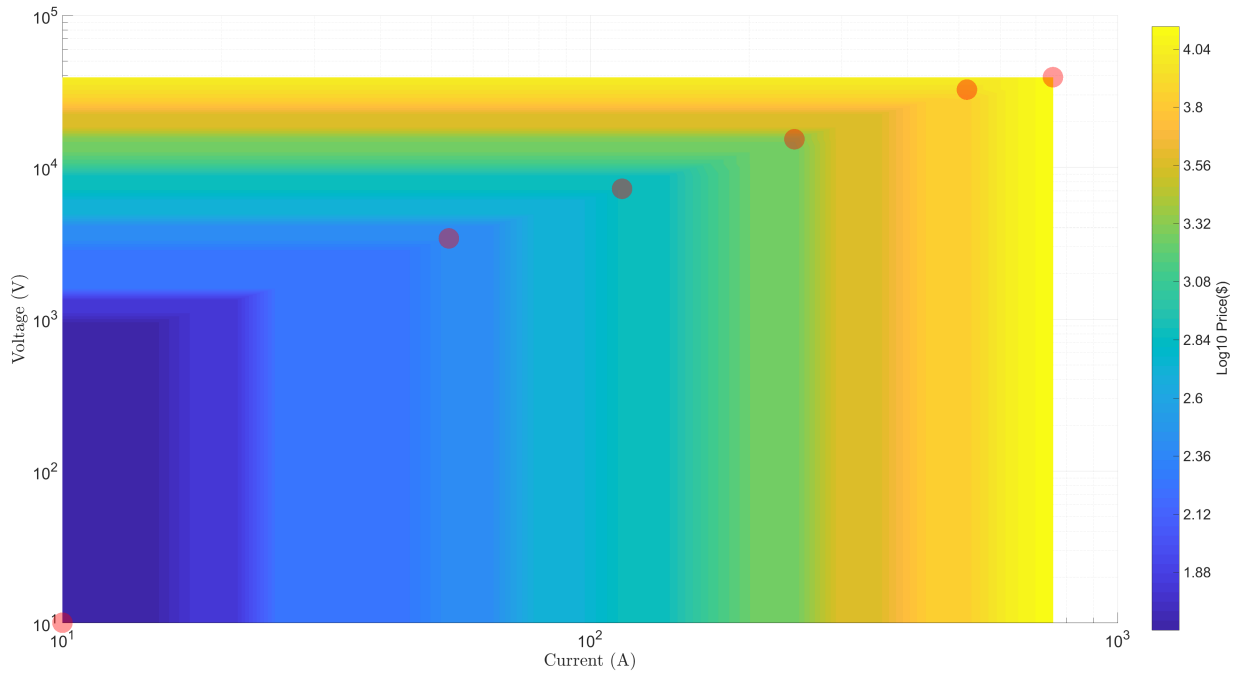


Figure 4.25: SiC MOSFET surface plot at 60 Ω load resistance

The table of values generated from the SiC MOSFET surface plot can be seen in Table 4.28 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	39,070	754	13,583
∼Target Spec Point	32,370	518	8,750
1/2 Target Spec Point	15,260	244	1,928
1/4 Target Spec Point	7,197	115	731
1/8 Target Spec Point	3,393	54	261
Minimum Point	10	10	44

Table 4.28: Table of SiC MOSFET test values from the surface plot for model 3

The IGBT surface plot can be seen in Figure 4.26 below.

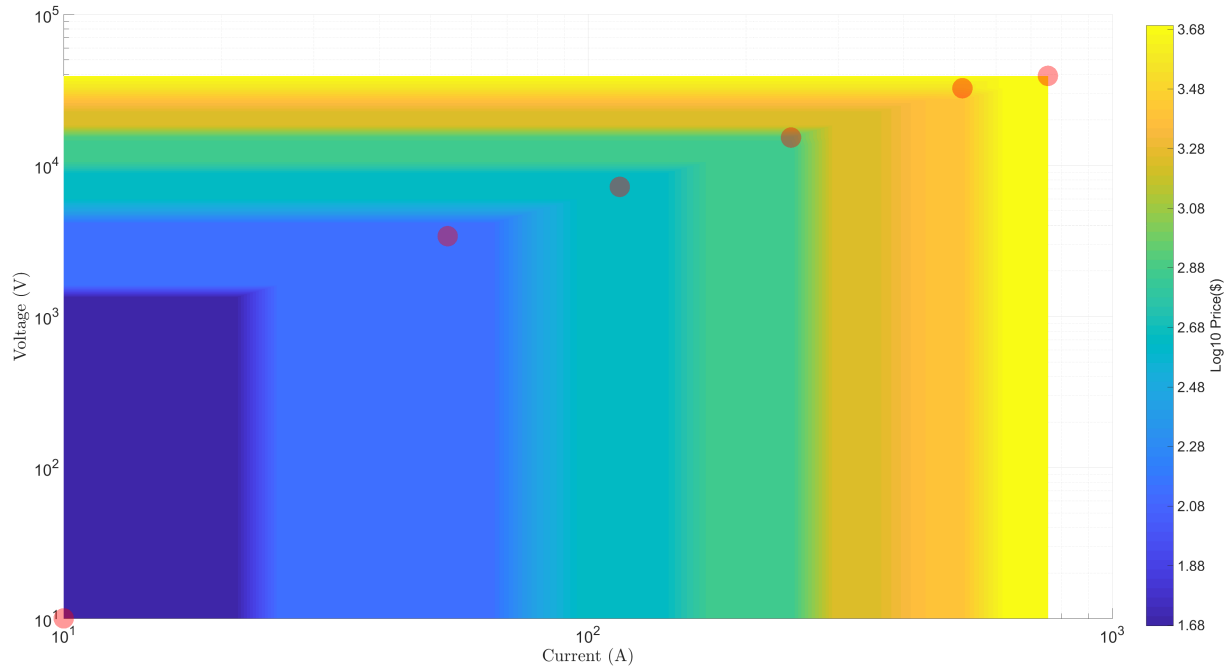


Figure 4.26: IGBT surface plot at 60 Ω load resistance

The table of values generated from the IGBT surface plot can be seen in Table 4.29 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	39,070	754	4,931
∼Target Spec Point	32,370	518	3,664
1/2 Target Spec Point	15,260	244	767
1/4 Target Spec Point	7,197	115	421
1/8 Target Spec Point	3,393	54	135
Minimum Point	10	10	48

Table 4.29: Table of IGBT test values from the surface plot for model 3

It can be seen that the IGBT would be the cheapest switch overall at ,664 at the target specification. The SiC MOSFET comes at $8,750 and the PMOSFET comes at $21,928 but does not even reach target specifications. The PMOSFET can only go up to 26.83kV, which is quite close to the needed value. However, even if there are ways to make the PMOSFET a little bit faster, its cost is still more than double the cost of the SiC MOSFET. At a 1ns rise time for both the SiC MOSFET and IGBT switches, they can reach up to 39.07kV. This is good, since even if the switches cannot get down to 1ns, they can still reach the 30kV goal. The SiC MOSFET is about more than double the cost of the IGBT, however keep in mind that to over drive the IGBT would be a much harder task than only using a few nanosecond drop to the stated rise time of the SiC MOSFET. Also, the IGBT is harder to parallel since its gate requires current, unlike the MOSFET. Thus, for my LTD I am using the SiC MOSFET. The $8,750 is not unreasonable either.

Comparison of Different Capacitor Technologies

All three capacitor technologies will be listed again in this modeling test.

The surface plot for the ceramic capacitor technology can be seen in Figure 4.27 below.

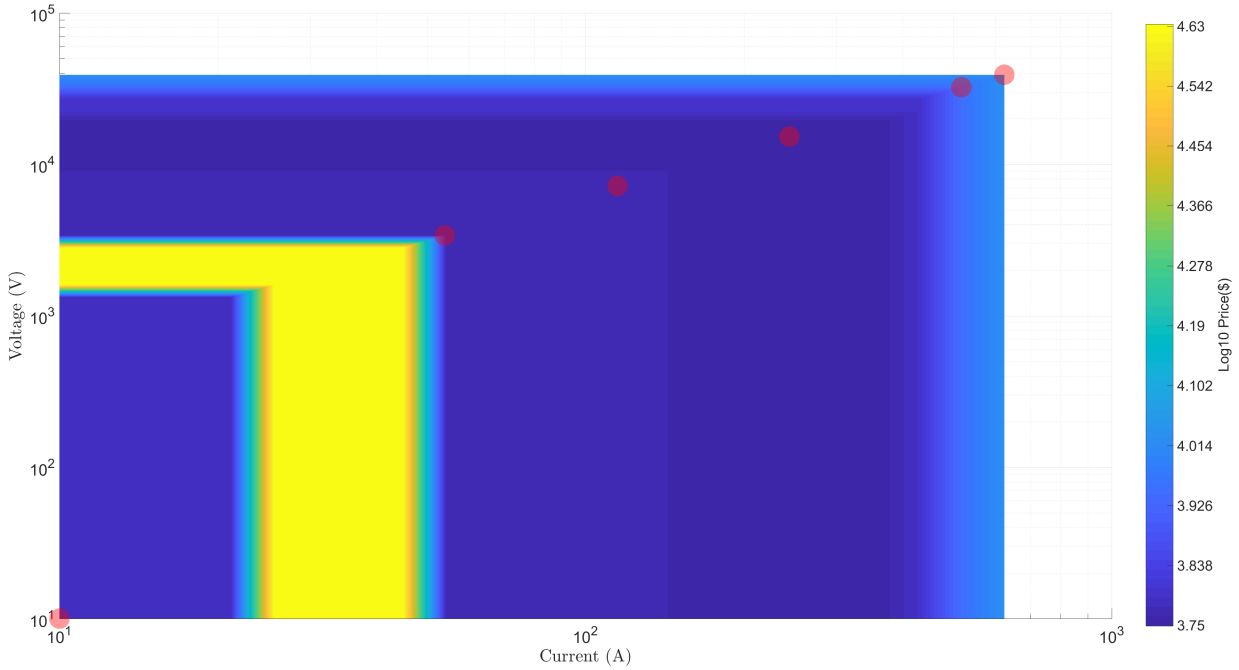


Figure 4.27: Ceramic capacitor surface plot at 60 Ω load resistance

The surface plot table of values for the ceramic capacitor technology can be seen in Table 4.30 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	39,070	625	10,666
∼Target Spec Point	32,370	518	8,810
1/2 Target Spec Point	15,260	244	5,610
1/4 Target Spec Point	7,197	115	5,808
1/8 Target Spec Point	3,393	54	5,902
Minimum Point	10	10	6,152

Table 4.30: Table of ceramic capacitor test values from the surface plot for model 3

The surface plot for the film capacitor technology can be seen in Figure 4.28 below.

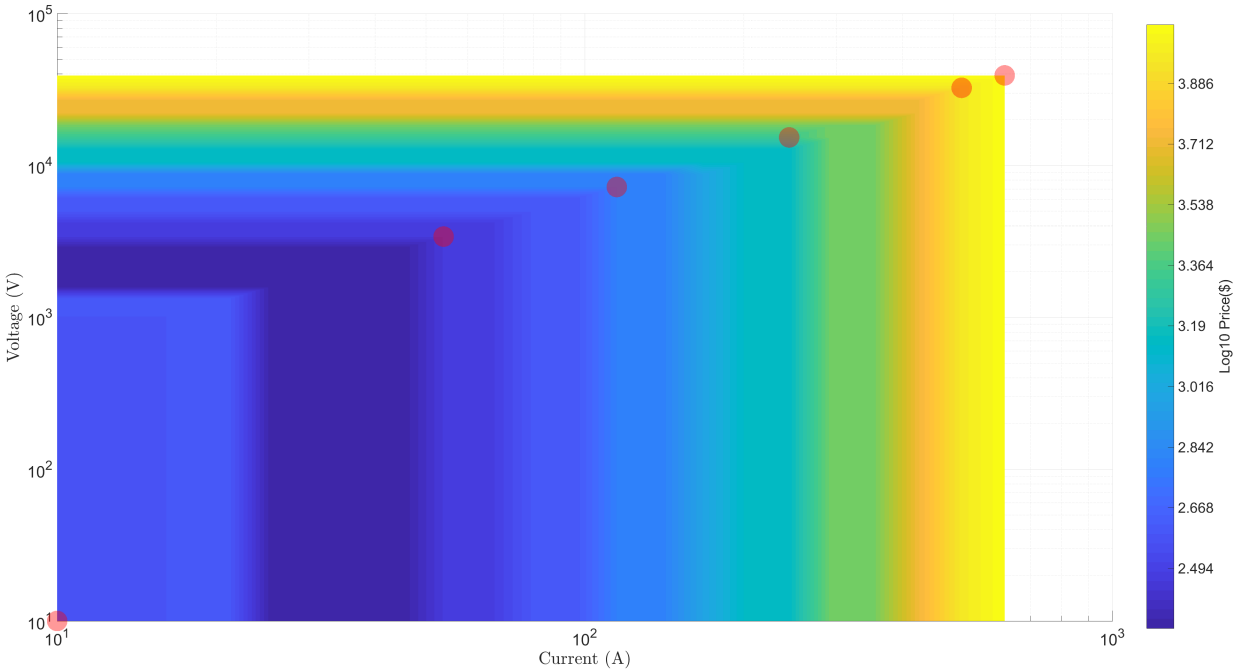


Figure 4.28: Film capacitor surface plot at 60 Ω load resistance

The table of values from the surface plot for the film capacitor technology can be seen in Table 4.31 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	39,070	625	11,350
∼Target Spec Point	32,370	518	9,078
1/2 Target Spec Point	15,260	244	2,056
1/4 Target Spec Point	7,197	115	608
1/8 Target Spec Point	3,393	54	292
Minimum Point	10	10	381

Table 4.31: Table of film capacitor test values from the surface plot for model 3

The surface plot for the oil filled capacitor technology can be seen in Figure 4.29 below.

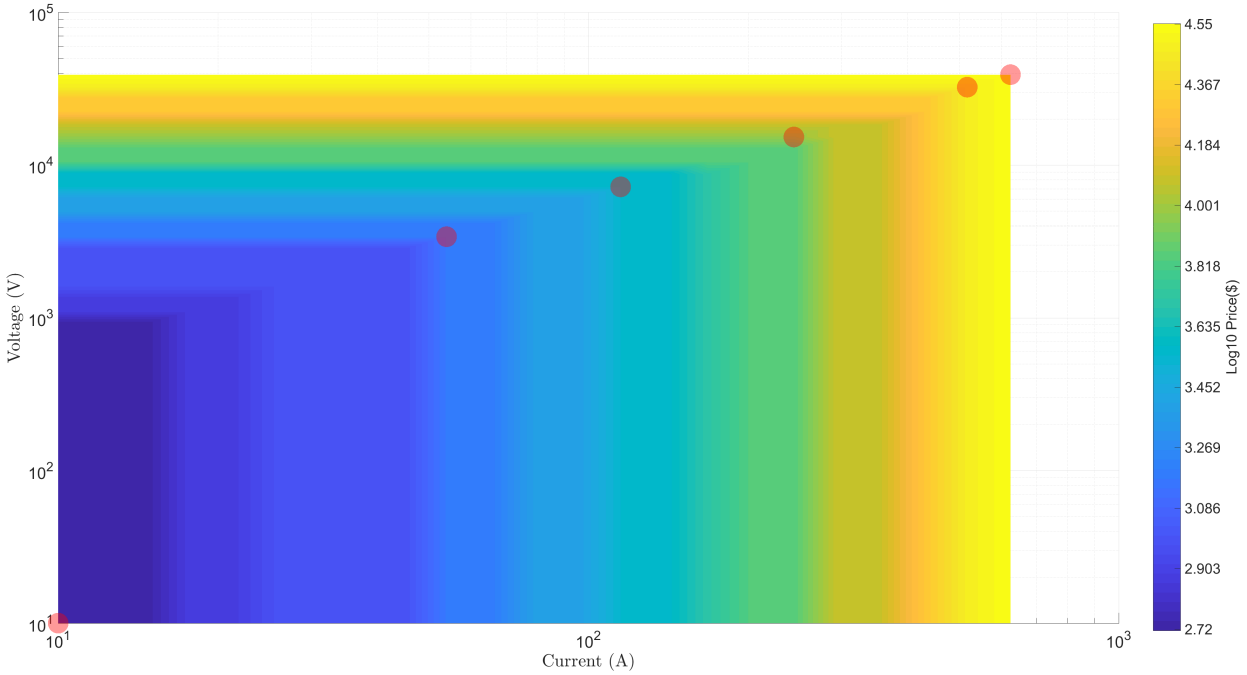


Figure 4.29: Oil capacitor surface plot at 60 Ω load resistance

The table of values from the surface plot for the oil filled capacitor technology can be seen in Table 4.32 below.

Test Point	**Voltage (V)**	**Current (A)**	**Cost ($)**
Maximum Point	39,070	625	35,563
∼Target Spec Point	32,370	518	29,854
1/2 Target Spec Point	15,260	244	9,397
1/4 Target Spec Point	7,197	115	3,532
1/8 Target Spec Point	3,393	54	1,535
Minimum Point	10	10	519

Table 4.32: Table of oil filled capacitor test values from the surface plot for model 3

From all of these plots, at 7J energy output, the ceramic capacitor technology is cheapest at the target specification point. Not to mention, ceramic capacitors are more compact in general compared to film capacitors. The ceramic capacitor LTD is expected to cost around $8,810. This is near the cost of the SiC MOSFET. The film capacitor comes at around $9,078 and the oil filled capacitor comes at a large $29,854. It is of observation that the capacitor cost for the ceramic capacitor is now cheaper than the film capacitor since the last model. This is also because of the parabolic trend the ceramic capacitor, thus at the higher voltage levels the ceramic capacitor costs become cheaper as the cost trend reaches its optimal point, whereas the film capacitor will continue to become more expensive with its linear trend.

4.6 Future Improvements to MATLAB Model

While this MATLAB model works well, it can be taken to additional levels in future versions. The following improvements can be made to this code:

1. Take away repetitive code and use additional for loops and arrays to ease changes to the model.

2. Utilize a Microsoft Excel spreadsheet to load in switch parameter information.

3. Take the Microsoft Excel spreadsheet to load in switch parameter information a step further by having the code model each switch row by row instead of the five switches being compared now. The model will need to add more variables in its functions to allow for passing through switch technology name and other parameters that must be added to each plot.

4. Add in the ability to model every part of the LTD by adding in transformer core and material information. Note, that this means not adding in a cost curve for a range of transformer cores, but by selecting a desired core and test it against all the models. This can then help in getting an even better value of the LTD rise time since

the stalk material, transformer winding material, and transformer core material are known. There is a complication as the desired transformer core will need to have a cost curve that must be provided by the company selling the core for various diameters and cross-sectional areas. Thus, unless a LTD being designed will be in the millions of dollars and it is crucial to find every potential area to cut costs, there is not a great need to add this function.

Chapter 5

Engineering the LTD

In this chapter I go through the design process in making a solid-state LTD. The design process begins by starting with the selection of the solid-state switch and its driver. Next, I then go into the transformer selection and its design. This section is written in much detail since I have noticed a lack of additional detail regarding pulsed power transformer design across all publicly available papers specifically for LTDs such as complete steps and explanations. After the transformer section, I then put together a rough estimate of how much the LTD is expected to cost, and its size.

Continuing through this chapter, I then go into detail about the fiber optic design to carry the trigger signal from the user to the LTD. I then take everything I have found from the previous sections and start putting together the LTD stage. Next, I then go into the fiber optic TTL to MOSFET driver circuitry, then from MOSFET driver circuitry to the solid-state switch, how to route the HV line, and PCB design techniques.

After the fine details in the circuitry, I then figure out the design of the stalk and the rest of the components needed to put all the stages together. Then, I put this design within an

enclosure. Finally, I show a 3D CAD model to give a visual representation of what the LTD is expected to look like.

5.1 Selecting Solid-State Switch and Driver

This section is broken up into two major areas, one looking into the solid-state switch to be used and the second looking at the technology drives the chosen solid-state switch.

5.1.1 Solid-State Switch Selection

A solid-state switch in my LTD will ideally need a high voltage rating, at least over 1kV to keep the number of stages low. The ideal switch would also have a decent current rating, with at least 20A and over to be viable. From the previous chapter, the best technology to use in my application would be the SiC MOSFET based on datasheet specifications. The manufacturing number of the SiC MOSFET is C2M1000170J by CREE. From low voltage testing $\leq$50V, I have determined that this SiC MOSFET can do at least 14.1A. At rated voltage, I expect the current capacity to be well over 20A, but I assumed for my purposes that it can safely handle 20A for designing the LTD. Oscilloscope data from the SiC MOSFET testing can be seen in Figure 5.1 below.

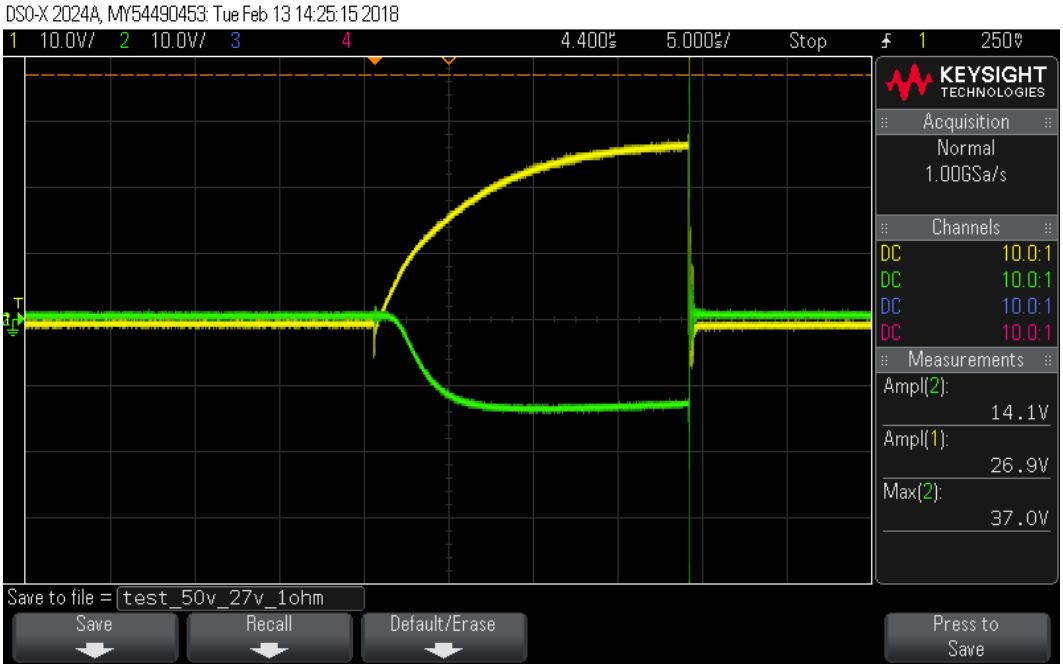


Figure 5.1: C2M1000170J current test with 27Vgs, capacitor at 50V, and 1Ω load resistance. Yellow trace (top trace) is gate voltage and green trace (bottom trace) is the MOSFET's drain voltage drop.

This oscilloscope data helps to show that I can get at least 14.1A at a low voltage load. The SiC MOSFET also sustained no damage from this test as well. Additionally, this test was operate using a low drive current to the SiC MOSFET, thus the rise time appears to be slow.

It is noted that if the SiC MOSFET switch operates at the rise time the specification sheet stated, it would not achieve my goal of 30kV and 500A in under 10ns. High currents at the MOSFET's gate can allow the switch to operate faster than what the data sheet gives out. This is because the gate capacitance of the MOSFET will be able to charge faster. There are two topology based designs that can help make a MOSFET operate with a higher voltage or a higher bandwidth. I discussed the possibility in using cascade to increase the voltage limit and cascode for increasing the bandwidth. Should over driving the MOSFET be inadequate in physical testing, these are two methods that can be used, however these will increase the

complexity of the system.

Cascading Research

One of the challenges in a LTD is getting the highest voltage as possible to operate per stage without destroying the switch being used. This is important as higher voltage will mean less stages, thus a better possibility in getting a rise time under 10ns as each stage adds a bit more time to the propagation of the pulse. An idea was played around by arranging a given MOSFET switch in a cascading topology. By pairing a capacitor to the gate of each MOSFET, and arranging the MOSFETs' source to each drain in series, the maximum voltage can stack. This has its disadvantages as the capacitors paired to each MOSFET have to be discharged safely as well after use. In Figure 5.2 below, an example of a cascading configuration of MOSFETs can be seen.

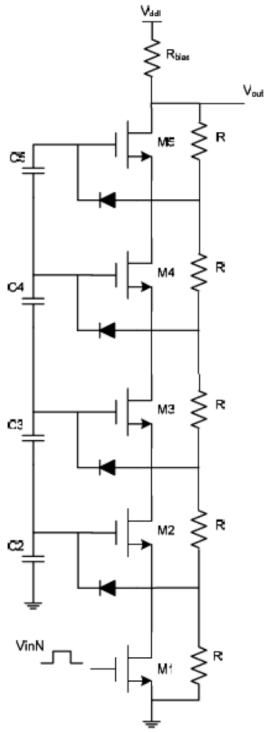


Figure 5.2: Five stage NMOS stack. Image from H. Jennifer Founds. et al. [36]

This five MOSFET stack configuration is one of a few other types of cascading topologies, however this topology is the simplest in terms of parts needed. A brief walk-through of how to derive the parts from the paper will be discussed. [36]

The resistor network used in the cascading case is determined by the following formula: $V_{draink} = \frac{k\ R}{5\ R+R_{bias}}\ V_{dd}$. Where k is the stage number of the NMOS in the cascoding setting. R_{bias} must be an order of magnitude lower than 5 R in order for the cascade to operate properly. The gate voltage in its off state can be seen as: $V_{gsk} = -V_{diode}$. Using these values, it is possible to solve for each individual capacitor by using the unit capacitance. This formula is: $C_{unit} = C_p\ (\frac{V_{drain2}}{V_{gs}+V_{diode}} - \frac{C_2+2\ C_p}{C_2+C_p})^{-1}$. From Figure 5.2, C_{unit} applies to the last NMOS in the cascade stack, or M5. Each additional NMOS under has its respective capacitor set to $k\ \times\ C_{unit}$. Where k in this case is the number of NMOSs away from M5. This can apply to any amount of stacking as well.

At the end of this research, cascading is a neat concept, however it increases the size of a LTD due to the linear configuration of the MOSFETs. With a goal in achieving less than a foot diameter LTD, cascading would not help. The other concern is complexity and rise time. Trying to find capacitance values on the market that will achieve the needed fine-tuned capacitance values derived from the calculations is challenging as well.

Cascoding Research

Should a problem come up where the rise time of the chosen solid-state switch is not fast enough, another MOSFET topology can be used. This is called cascoding where two MOSFETs are needed to carry the pulse. The first MOSFET operates normally, but the second MOSFET has its source connected to the first MOSFET's drain. The second MOSFET's gate is connected to ground, and its drain is attached to the output. The advantage of arranging MOSFETs in this way is higher bandwidth. This is because the second MOSFET

helps to bring down the Miller effect by lowering the gain of the first MOSFET, thus lowering the internal capacitance of the MOSFETs themselves. This in turn decreases the rise time of the MOSFET being used. An example of a cascode circuit can be seen below in Figure 5.3. [16]

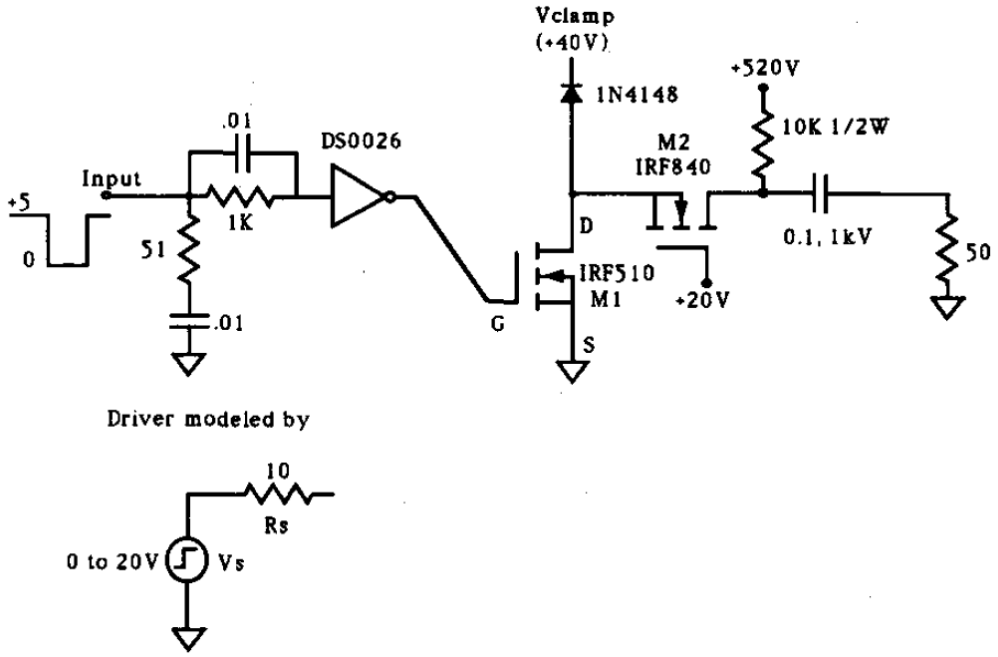


Figure 5.3: Example of a cascode MOSFET circuit. Image from R. J. Baker. et al. Image made in May 1992. [16]

The cascode topology is not complex, however it does require using additional electronics, which in turn increases price. The footprint of the circuit increases as well, which will make it harder to achieve the LTD size requirement. In a future design of a LTD where faster rise times are needed, this topology can be used. In the Baker paper, the author achieved a rise time improvement by an order of magnitude.

5.1.2 Driver Design and Selection

In the search for optimal drivers for operating a SiC MOSFET at its fullest potential, I found that there does not exist any driver capable of achieving the rise times and voltages required at stated specifications on their data sheets. Drivers have been found that have fast rise times of under 5ns, but their voltages only go up to 18V max. They are excellent in taking an input logic signal and putting out the right gate driving pulse. Usually, drivers have two pins, one for inverting and one for non-inverting configuration. This makes them easy to prototype with.

In order to get around this barrier, I decided to use a MOSFET as an intermediary between the MOSFET driver and SiC MOSFET. The MOSFET found can achieve the 30V output needed, with a fall-time of less than 2.7ns. Fall-time is being used here because a common-source NMOS amplifier inverts the signal, thus it would be the falling edge that switches the state of the SiC MOSFET. The MOSFET's manufacturing number is DMN6140L7 by Diodes Incorporated.

First, I needed to find out how much current is needed to drive the SiC MOSFET to a possible 1ns rise time. Knowing the total capacitance of the line between the MOSFET to the SiC MOSFET is needed for the calculation. The input capacitance of the SiC MOSFET is 200pF. The output capacitance of the MOSFET is 18pF.

I thought it may be a good idea to implement a TVS diode to protect the rest of the driver circuitry before the SiC MOSFET gate. To check feasibility, I looked at a TVS diode with manufacturing number 824551221 by Wurth Electronics Incorporated. The manufacturer does not give a capacitance directly, but in Figure 5.4 below, I can determine its amount.

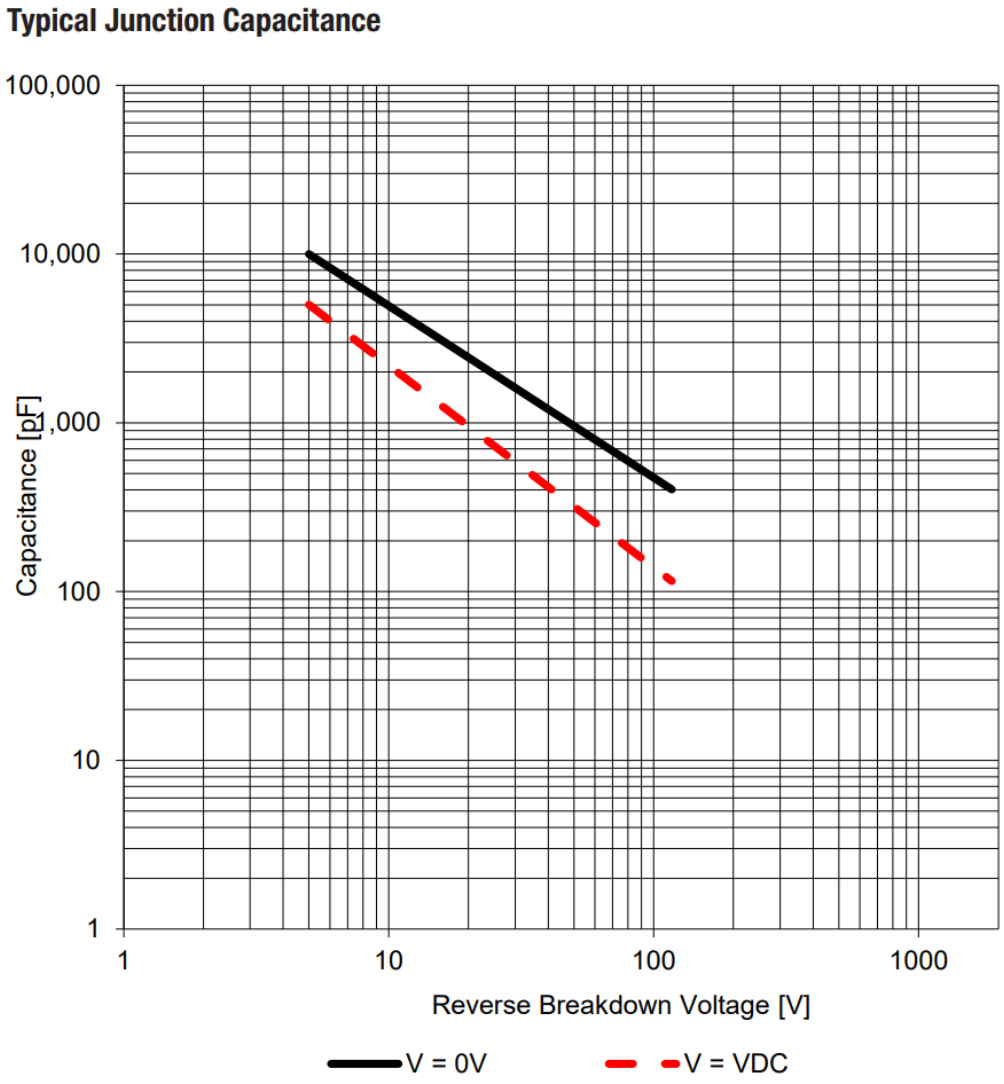


Figure 5.4: Capacitance plot for the TVS Diode. Image made by Wurth Electronics. [4]

I know the TVS diode from the data sheet has a reverse breakdown voltage of 25.65V. This means the capacitance would be 2,000pF. Unfortunately, this is too high of a capacitance to have a feasible current that can be pulsed to the SiC MOSFET's gate. Other TVS diodes with similar breakdown and clamping voltages are not much better in their capacitance. It would be best to apply a TVS diode at the drain of the SiC MOSFET where there is a much greater current that would be less affected by this device. It is important that the TVS diode used have a quick reaction time in order to help prevent damage from transients.

Table 5.1 below summarizes and totals the capacitance of the line.

Part	**Capacitance (pF)**
Sic MOSFET	200
MOSFET	18
Total Capacitance	218

Table 5.1: Total capacitance along the SiC MOSFET gate line

Knowing the capacitance data, I calculated the current required to operate the SiC MOSFET. The charge equation $Q = C \times V$ derived from the capacitance equation $C = \frac{Q}{V}$ is used to get the total charge that needs to be moved. [37] If maximum gate voltage to be used is 25V, then $Q = 218pF \times 25V$. The value of Q is then 5.45×10^{-9} coulombs. Then, using the equation $Q = I \times t$ where t is 1ns. [12] The current would then be 5.45 amps. To make it easier,I rounded this number up to 6A, which also leaves a little room in case of defects in any of the MOSFETs that could increase their capacitance.

Next, I calculated the value of the resistor to be used to supply the current into the drain of the intermediary MOSFET and into the gate of the SiC MOSFET. If the maximum gate supply voltage to be used is 25V and the needed current is 6A, then using ohm's law $V = IR$, the resistance would be 4.2Ω.

Using this newly found data, I looked at the MOSFET gatesource curves in Figure 5.5 below.

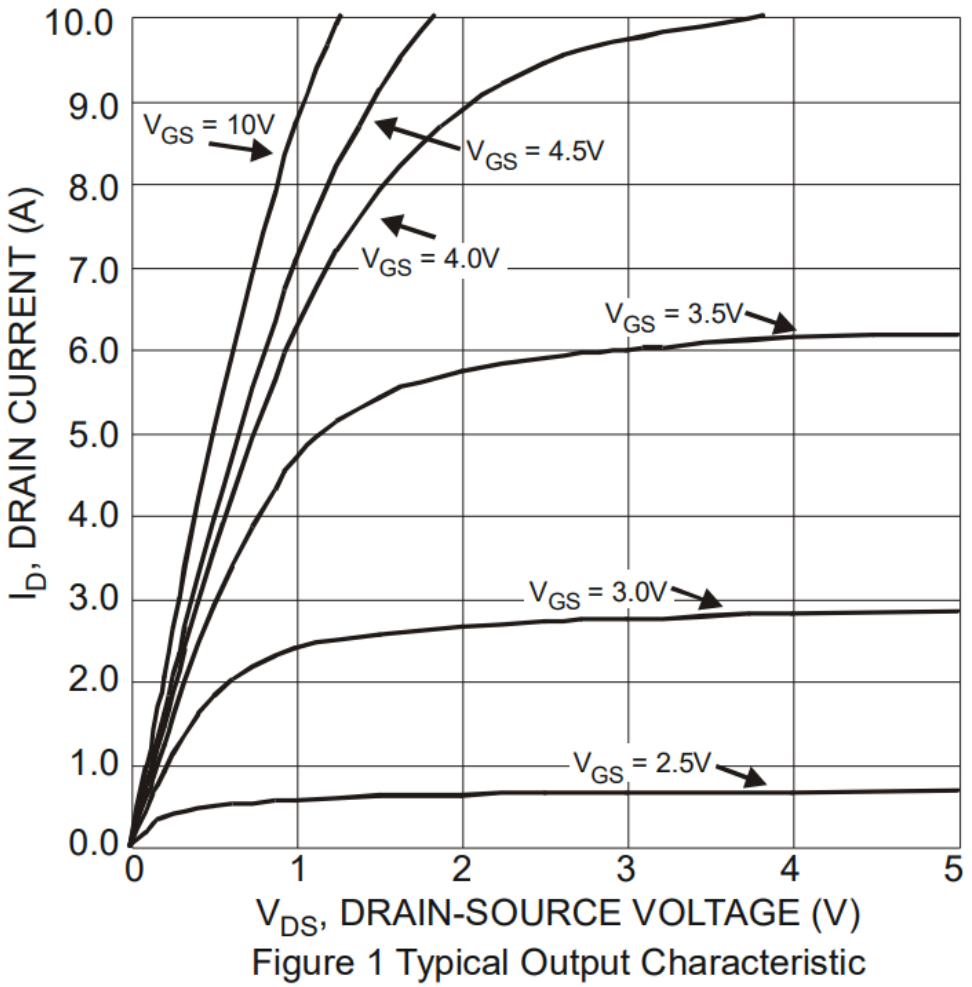


Figure 5.5: Intermediary MOSFET gate-source curves. Image from Diodes Incorporated. [3]

If the drain-source voltage is going up to 25V, the MOSFET operates in the linear region. To start conducting at 6A, the MOSFET needs a gate-source voltage of 3.5V. This value is important to figure out the rise time between the MOSFET driver and the intermediary MOSFET.

It is important to note that the MOSFET has a continuous current limit. For my purposes, 6A would destroy the MOSFET if kept on continuously. To solve this issue, another power MOSFET located at the output of the power supply that is giving the voltage to the drain

of the MOSFET can turn on right before firing the LTD. Then, the MOSFET immediately turns off in the microsecond regime. From the datasheet, the MOSFET's safe operation area can be seen in Figure 5.6 below.

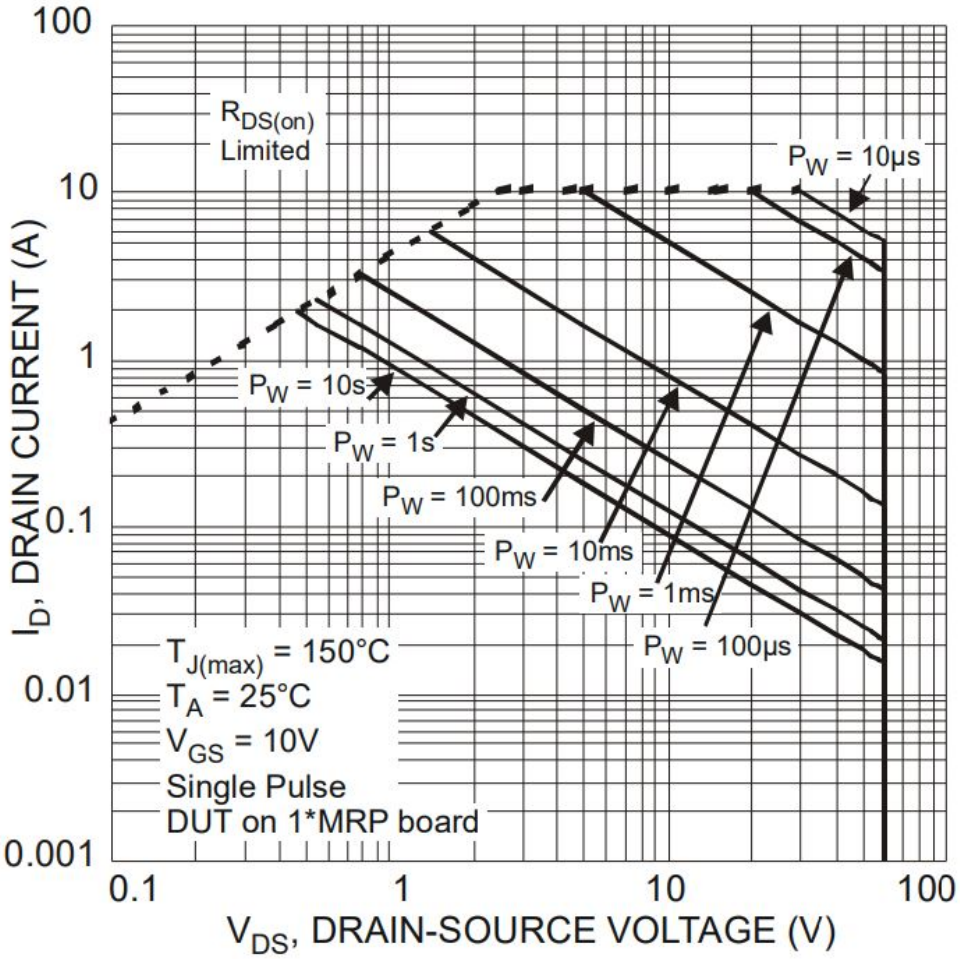


Figure 5.6: Intermediary MOSFET safe operating area plot. Image from Diodes Incorporated. [3]

At 6A and an expected drain-source voltage of 25V, the chart shows that the MOSFET can be powered for no more than 100 μ s. Thus, the power MOSFET turning the 25V power supply on and off will only pulse no more than 100 μ s intervals.

Now that I have figured out the driver design between the MOSFET and the SiC MOSFET, I then characterize what is occurring between the MOSFET driver and the intermediary MOSFET. This is to check that I am getting an acceptable rise time in this stage of the driver circuitry. TI does not give a capacitance nor a capacitance plot for their driver, however they do list the expected rise time for given a load capacitance at a specified driver voltage. The lowest load capacitance available is 1,000pF and its rise time is 3ns and fall-time is 2ns. This means any load capacitance lower than 1,000pF will perform faster than 3ns or 2ns respectively. TI also provides the sink and source current, which would be 7.6A and 4.5A respectively. The input capacitance of the intermediary MOSFET is 315pF.

To find the amount of time it will take to turn-on the MOSFET, the drive voltage to have the MOSFET conduct at its needed current is 3.5V. The source-current is 4.5A. This means the Q is 1.1025×10^{-9}C. This means the time to propagate the pulse to start conducting the MOSFET at the needed 6A current is 0.245ns. To find the amount of time it takes to turn-off the MOSFET from full conduction, I know the voltage would be 12V. The sink current of the MOSFET driver is 7.6A. This means the Q is 3.78×10^{-9}C. The fall-time for the MOSFET is 0.497ns. Both rise and fall times are well under the 1ns jitter requirement.

Effect of Ferrite Beads

In order to help take down the effects of noise while switching the SiC MOSFET, ferrite beads are being used to help mitigate the effects of EMIs and parasitic oscillation. A ferrite bead can be thought of as a frequency dependent resistor, allowing the use of a lower gate driving resistor to dampen out oscillations that occur in the signal. The oscillations can come from the inherent RLC connection that occurs when sending a square wave into the circuit. The resistance of the line, inductance of the line leads, and the parasitic capacitance of the solid-state device can create a RLC resonance. The square wave is a Fourier series of numerous frequencies and thus will usually have one element of the signal be the same as

the resonant frequency of the RLC connection. Thus, accounting for parasitic oscillation is crucial when trying to achieve a clean pulse shape. From my initial SiC MOSFET test, I have noticed an oscillation frequency near 40MHz. From my ferrite bead search, it became challenging to find a ferrite bead that can attenuate the desired frequency while handling the current going through it.

In Figure 5.7 below, frequency curves can be seen for the ferrite bead that I selected.

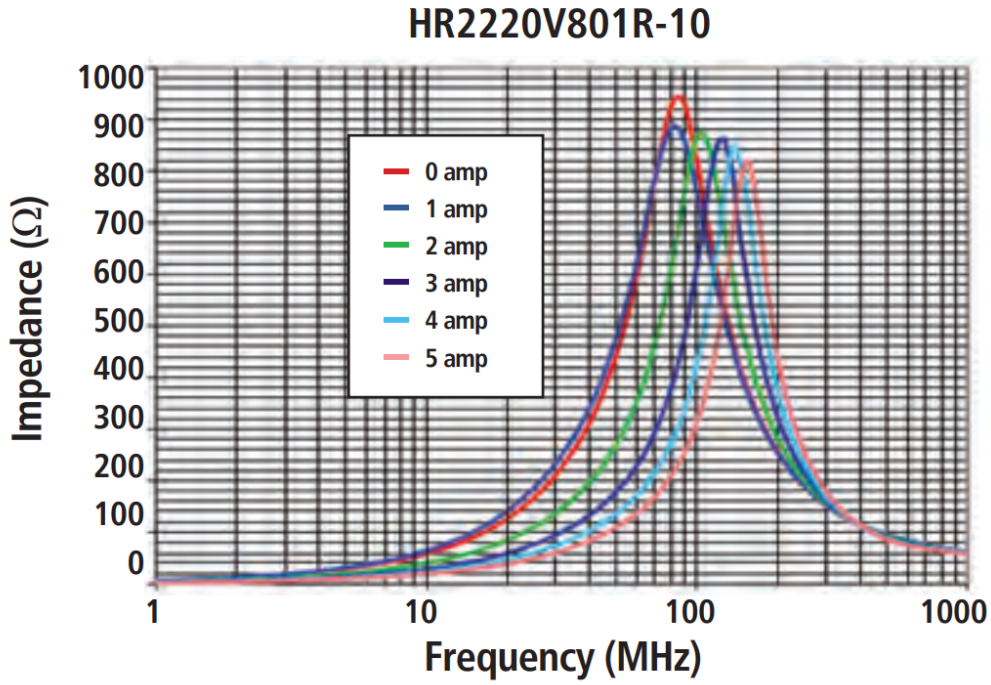


Figure 5.7: HR2220V801R-10 ferrite bead impedance versus frequency plot. Image from Laird. [1]

The ferrite bead is rated at 8A. Since my current being used to drive the SiC MOSFET is 6A, the ferrite bead's real curves on the plots will be shifted to the left. Ideally, ferrite beads are operated in a derated state in order to achieve the desired curve performance.

To demonstrate the effect of the ferrite beads, multiple figures are shown below, each one using a different number of ferrite beads. These tests are meant to demonstrate the effect of saturation of ferrite beads, and the importance in paralleling enough of them to get a desired pulse. These tests are first using a low current ferrite bead at a 500mA rating. The last test with four ferrite beads included a ferrite bead in parallel with an 8A rating which has a frequency plot as seen in Figure 5.7 above.

Figure 5.8 below shows no ferrite beads being used during the pulse.

Figure 5.8: Control test using no ferrite beads, green trace line (positive square pulse waveform) represents SiC MOSFET output voltage.

It can be seen that around a 40MHz oscillation is being made. At higher voltages these oscillations will become large enough to rapidly trigger the SiC MOSFET on and off, which can damage the switch. To study the effect that a ferrite bead provides, a small 500mA ferrite bead was placed in series to the gate of the SiC MOSFET. This can be seen in Figure 5.9 below.

Figure 5.9: One ferrite bead being used, green trace (top waveform) represents SiC MOSFET output voltage

It can be seen that the oscillation has been attenuated, but also a range of other useful frequencies used to make a square wave pulse. The output pulse has been severely attenuated and lost its squareness. This is a demonstration that saturating a ferrite bead changes its frequency curves. In the next test in Figure 5.10 below, an additional ferrite bead was added in parallel.

Figure 5.10: Two ferrite beads being used, green trace (top waveform) represents SiC MOSFET output voltage

It can be seen that by increasing the current capacity of the ferrite beads, that the pulse fidelity becomes better while dampening the parasitic oscillation. The next test adds an additional ferrite bead in parallel that can be seen in Figure 5.11 below.

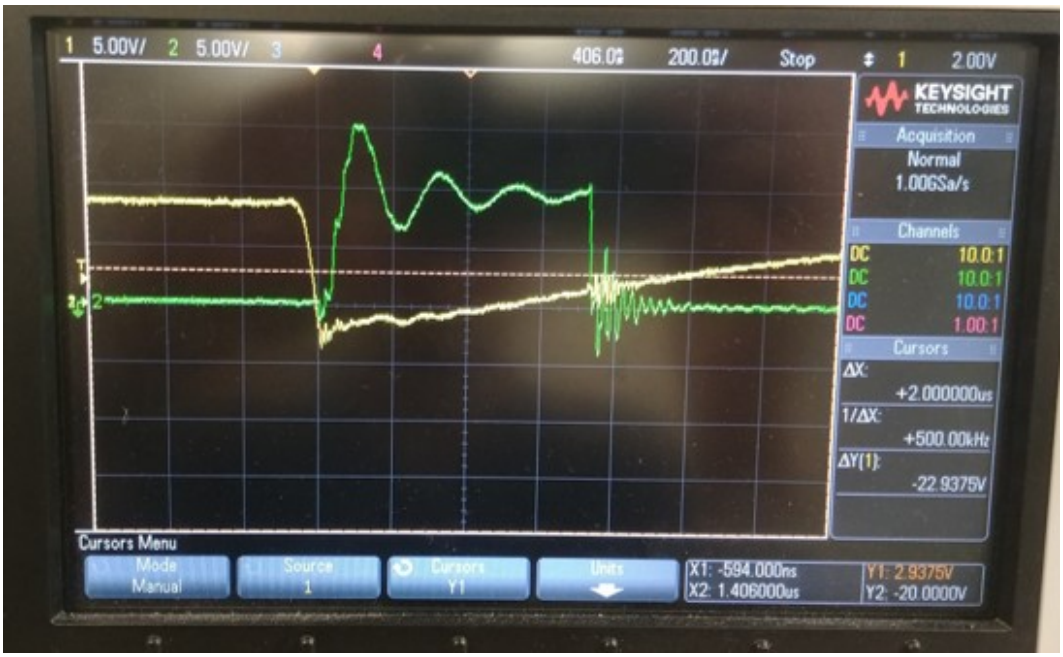


Figure 5.11: Three ferrite beads being used, green trace (top waveform) represents SiC MOSFET output voltage

Now a square wave pulse is starting to form. Note, that there is a pattern between each of these tests as each ferrite bead added places in another sinusoidal waveform that helps to make the pulse more square. The final test adds a fourth ferrite bead, this time rated at 8A in parallel with the rest. This can be seen in Figure 5.12 below.

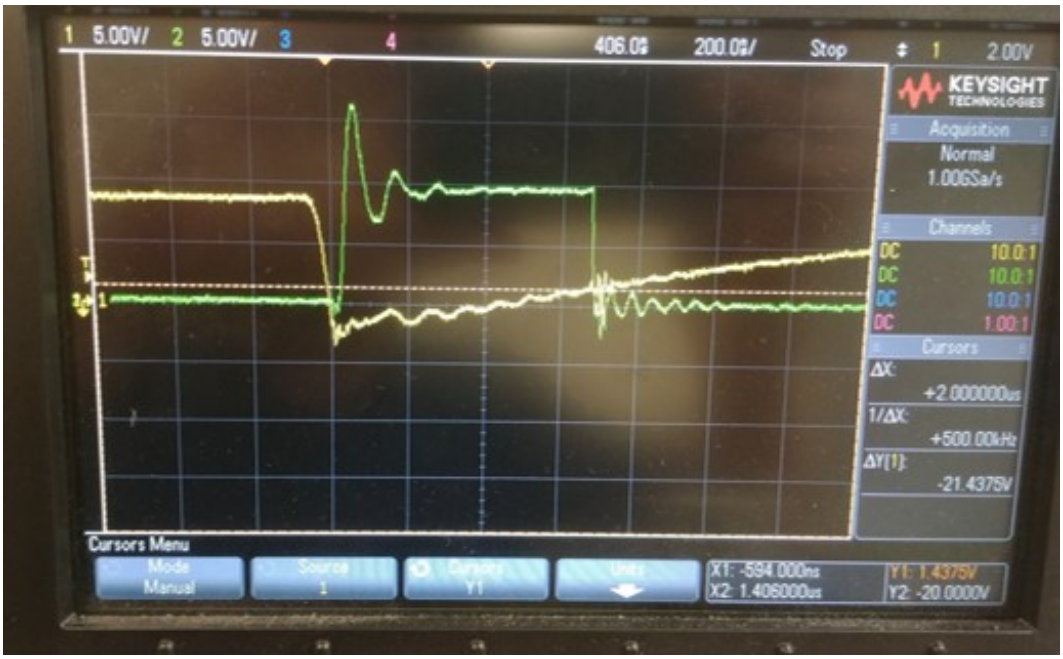


Figure 5.12: Four ferrite beads being used, green trace (top waveform) represents SiC MOSFET output voltage

From this test, I can see that the square wave has been fully formed, and the parasitic oscillation frequency has been heavily dampened. This is because the frequency plots have shifted more towards the right and stopped attenuating the needed frequencies to keep the square wave pulse while starting to remove the oscillation frequency. Also of note, ferrite beads are inductors and a larger transient voltage is observed at the rising edge of the pulse. Care must be taken to avoid the transient from damaging the SiC MOSFET. Adding a TVS diode before the gate is not recommended either due to how its internal capacitance will slow down the rise time of the SiC MOSFET switch.

For my LTD design, I have determined that it would be best to use three HR2220V801R-10 8A ferrite beads at the SiC MOSFET gate which gives me a total current rating of 24A. This is well over double the current that will be driving the SiC MOSFET, thus would not attenuate the square wave.

5.2 Selecting and Designing the Transformer Core

I used the formulas that have been discussed in the background chapter for pulsed power transformer cores. This section will begin with a search for the best transformer core for my LTD application and then go into how I found the dimensions for the core.

5.2.1 Transformer Core Search

From the related work chapter, it has been noted that Metglas is the best transformer core material to use for fast rise time LTD applications. Other materials may work such as iron, but they risk higher power loss and potential to distort the rise time of the pulse due to not being effective at high frequencies.

A quick look at their website explains how their product is made, "The key to Metglas Inc.s proprietary manufacturing process is the rapid-solidification of molten alloy at a rate of approximately one million degrees Celsius per second." They also included a graphic giving a high level overview of their process. This can be seen in Figure 5.13 below.

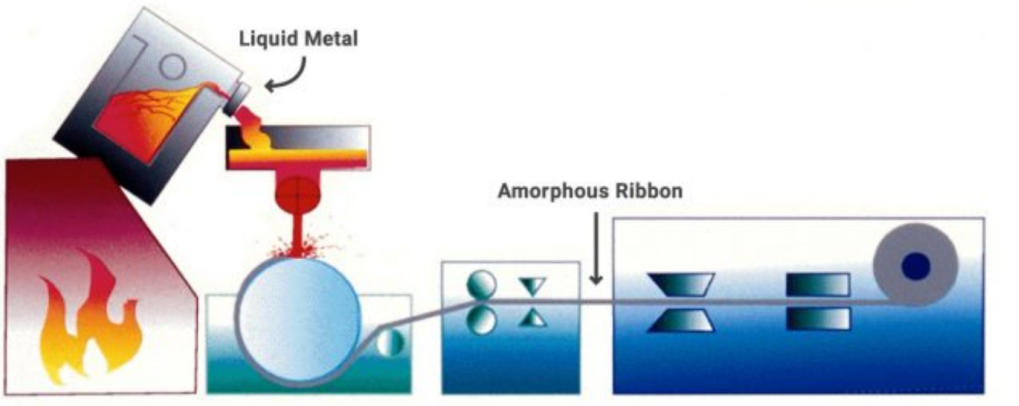


Figure 5.13: Metglas's manufacturing process graphic. Image credit: Metglas Inc. [52]

From their explanation and graphic, Metglas is able to take alloys and turn them into amorphous metals. This type of metal displays a random structure of atoms within the

material. Having this random structure allows it to achieve much higher permeability than anything else in the market. Where the usual relative permeability of a ferrite-core such as iron is 5,000, Metglas can achieve well over 300,000. [52]

The following alloys are available from the company: 2605CO, 2705M, 2605SA1, 2605HB1M, 2605S3A, 2705M, 2714A, and 2826MB. Table 5.2 and Table 5.3 below both show pertinent differences between all of the alloys. One of the differences which may not be familiar by readers would be the magnetostriction parameter, which is how much the material physically moves while being magnetized. This can cause core losses in the form of friction and heat. The lamination factor parameter is the same as the packing factor. For the purpose of the LTD I designed, I only care about the annealed properties of each material.

Alloy	**Metal Based**	**Max DC Permeability (Annealed)**	**Saturation Induction (T)**	**Electrical Resistivity** ($\mu\ Ohm - cm$)
2605CO	Iron	400,000	1.8	123
2705M	Cobalt	600,000	0.75	136
2605SA1	Iron	600,000	1.56	130
2605HB1M	Iron	600,000	1.63	120
2605S3A	Iron	35,000	1.41	138
2705M	Cobalt	600,000	0.77	136
2714A	Cobalt	1,000,000	0.57	142
2826MB	Iron Nickle	800,000	0.88	138

Table 5.2: Table #1 of Metglas alloys

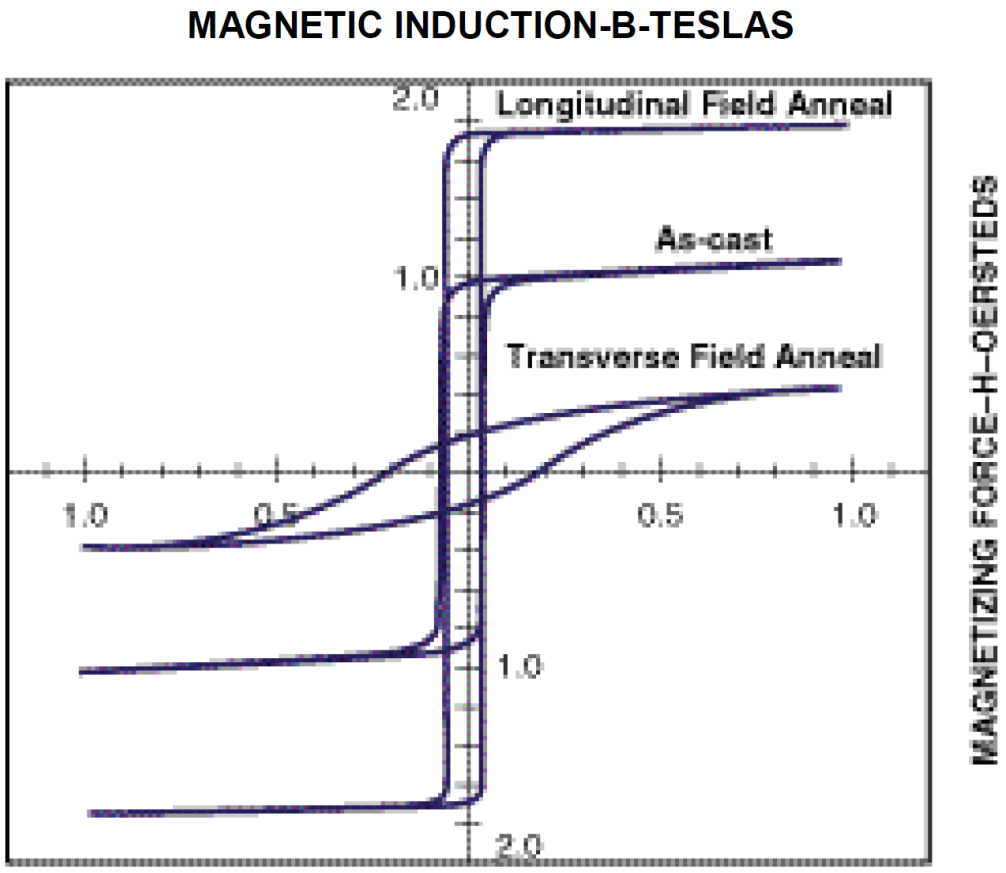
Alloy	**Thickness** (μ**m**)	**Lamination Factor** (%)	**Magnetostriction** (**x**10^{-6})
2605CO	N/A	>75	35
2705M	N/A	>75	<1
2605SA1	25	>84	27
2605HB1M	25	>84	27
2605S3A	18	>75	20
2705M	22	>75	<0.5
2714A	15	>75	<0.5
2826MB	29	>75	12

Table 5.3: Table #2 of Metglas alloys continued

5.2.2 Metglas Transformer Core Specifications

The chosen core as recommended by Metglas for my LTD application is the 2605CO core. It is Metglas's flagship core in having the best performance at the highest frequencies as possible. However, I still expect there to be some loss in power as the pulse goes through. This core also has an excellent squareness ratio, meaning the integrity of the pulse would not be as affected as with a normal iron ferrite core. The B-H curve for this core can be seen in Figure 5.14 below.

Figure 5.14: Metglas 2605CO B-H curve. Magnetic induction B-Tesla is y-axis and magnetizing force H-Oersteds is x-axis. Image credit Metglas Inc. Image made in 2009. [51]



The core that I used is the longitudinal field anneal. It is apparent that the squareness ratio is excellent. However, it can also be noticed that it does not take much H-field to saturate the core. As discussed in the previous section about the physics behind pulsed power cores, this is not an issue.

The physical and magnetic properties of 2605C0 can be seen in Table 5.4 below.

Property	**Value**
Lamination Factor	>75%
Continuous Service Temp.	125
Saturation Induction (T)	1.8
Maximum D.C. Permeability (μ)	400,000
Electrical Resistivity (μ-cm)	123

Table 5.4: Physical and magnetic properties of 2605CO

While working with a Metglas engineer, I was provided with the raw data of their B-H curve test to help get better transformer core information. This can be seen in appendix 0.7. For the design of this transformer core, a factor of safety of three will be used. This means the operational area of the transformer core will usually reach a third of its saturation level or 0.6T.

In Figure 5.15 below, the raw BH curve can be seen for the Metglas material. The data points can be seen in a table in the appendix.

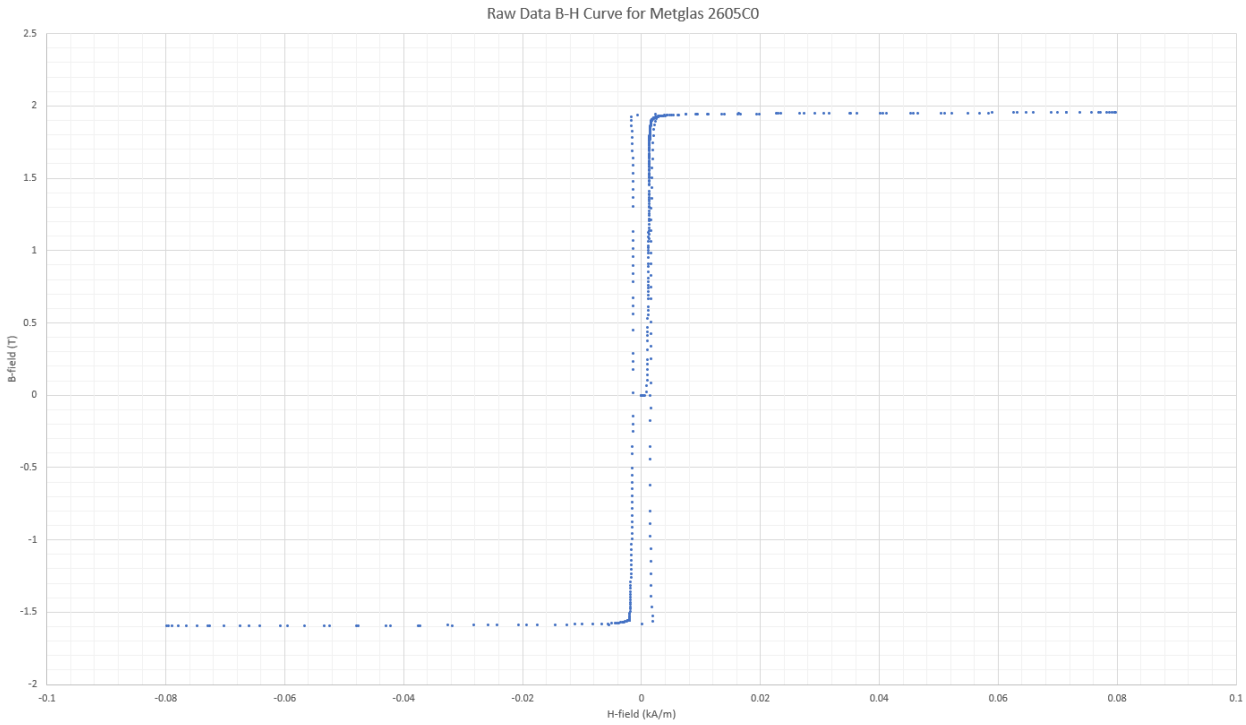


Figure 5.15: B-H curve for Metglas 2605C0 from raw data

A useful parameter to get out of this curve is the squareness ratio, where the closer the ratio is to one, the better the fidelity of the pulse. The squareness ratio is given by the following formula: $\frac{B_r}{B_m}$. Where B_r is the flux density when no magnetic force is applied after saturation. B_m is the maximum flux density. B_r from the B-H curve provided by the company is 1.936 and B_m is 1.954. This yields a squareness ratio of 0.99. This value is nearly one which means the pulse fidelity would be intact as the pulse propagates through the transformer.

The important parameters to get from all of this information is that the maximum field density swing or $\Delta\ B$ is 1.8T and the expected relative permeability will be 334,561. The permeability came from looking at the second increasing of the H-field. This is because the first time the H-field increases in a virgin core, the B-H curve is different. The second passing yields a H-field of 1.59Am and a B-field of 0.6688T. Using the formula $B = u\ H$, the total permeability is found to be 0.420208. Dividing out by 4 π 10^-7 gives out the relative

permeability.

Transformer Core Design for LTD

For me to use the Metglas core, I need to find the cross-sectional area to prevent saturation. I used this formula $Ae = \frac{3 \times V \times \Delta t \times N}{\Delta B \times PF}$ to find the value. V in this case would be 1.6kV. N would be one since their is only a single turn winding on the primary. would be 100ns as the maximum pulse width. would be 1.8T using just the positive cycle of the B-H curve. The packing-factor of the Metglas core being used is 75%. Plugging all these values in yields $0.000356m^2$ for the cross-sectional area of the core.

When discussing how thin the Metglas core could be, Metglas' engineer recommended to not go less than 0.25 inches. The engineer also recommended to make the inner radius as large as possible to better the core's properties. I decided that to make the foot diameter requirement, a transformer core that is no larger than 7 inches outer diameter would suffice. $0.25^{'}$ is equivalent to 6.35mm. Using the area of a rectangle $Area = Length \times Width$, the width needed to get the cross-sectional area required would be 0.0561 meters or 2.21 inches. Keep in mind this value in a torus is a radius. The radius of a 7 inch outer diameter is 3.5 inches. Subtracting 2.21 inches from 3.5 comes out to 1.3 inches for the inner radius. This means the inner diameter of the Metglas core is 2.6 inches.

The dimensions that were determined are shown below. It will be of note that a mandrel had to be used in order to keep the core together, these dimensions are also annotated.

- Inner Metglas Diameter: $2.6^{''}$
- Outer Metglas Diameter: $7.0 \pm 0.020^{''}$
- Metglas Height: $0.25^{''}$

- Mandrel Height: $0.394 \pm 0.010''$
- Mandrel Inner Diameter: $2.36 \pm 0.010''$

Orthographic drawing of the transformer core can be seen in appendix .1.

5.2.3 Transformer Core Renderings

The following renderings were made using the design dimensions of the transformer core being used.

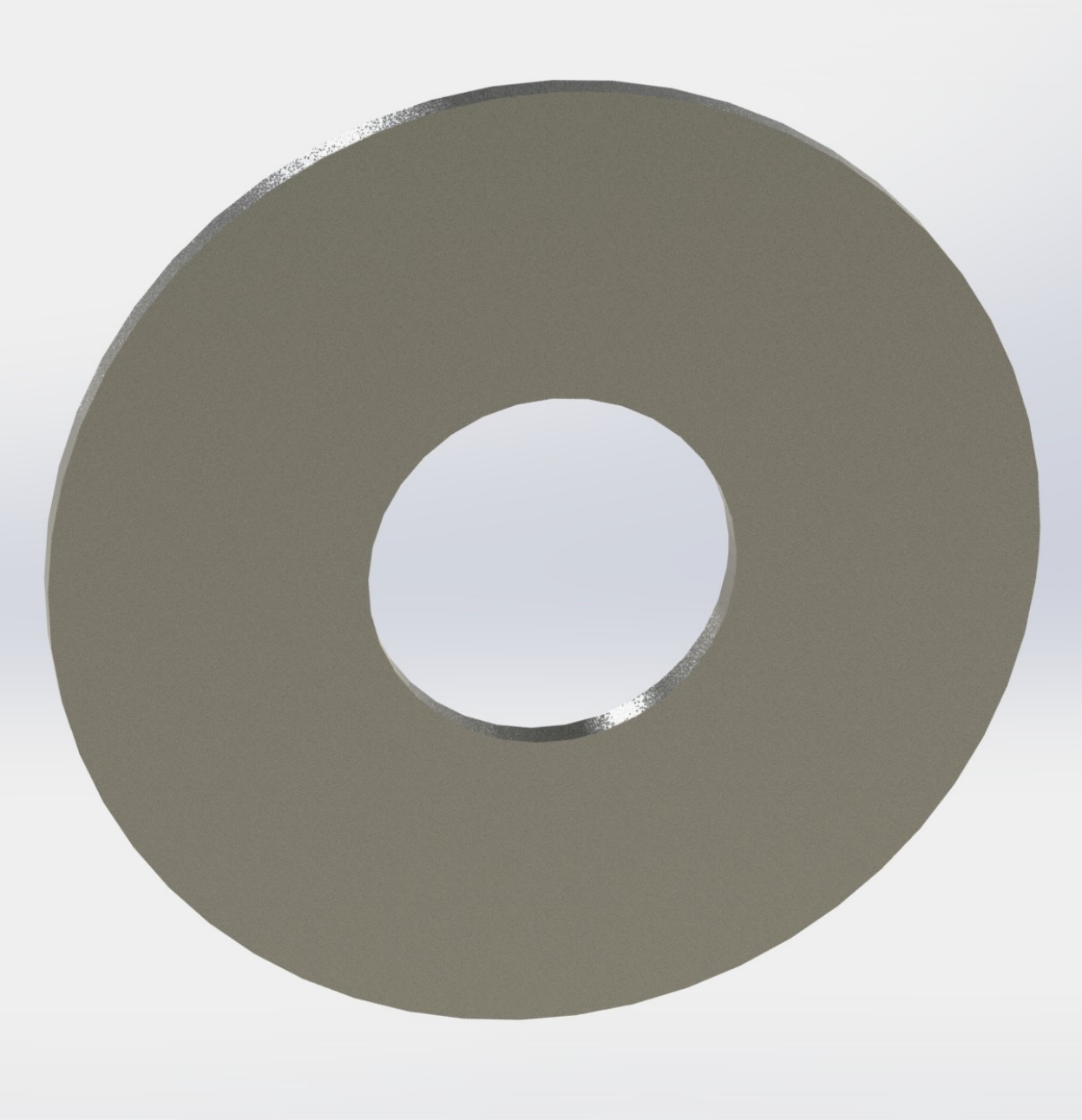


Figure 5.16: Metglas material only in the transformer core

Figure 5.17: Metglas material with mandrel in the transformer core

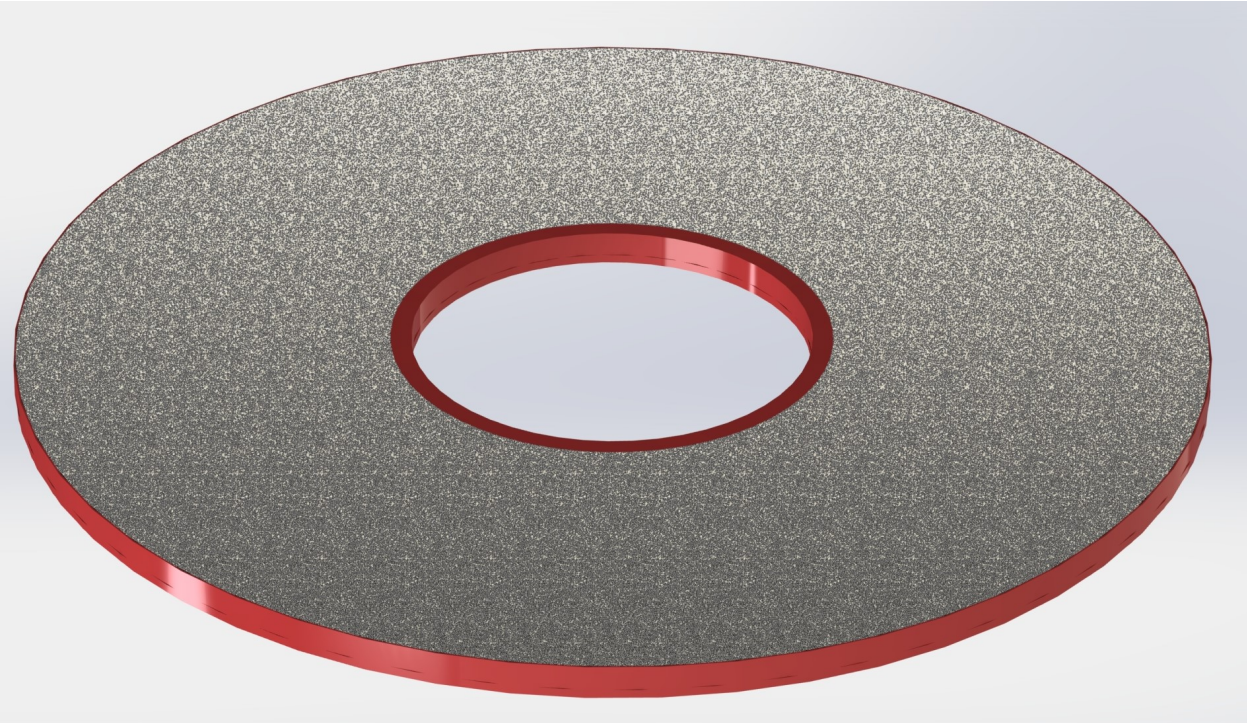


Figure 5.18: Cross-sectional view from the top face of the transformer core

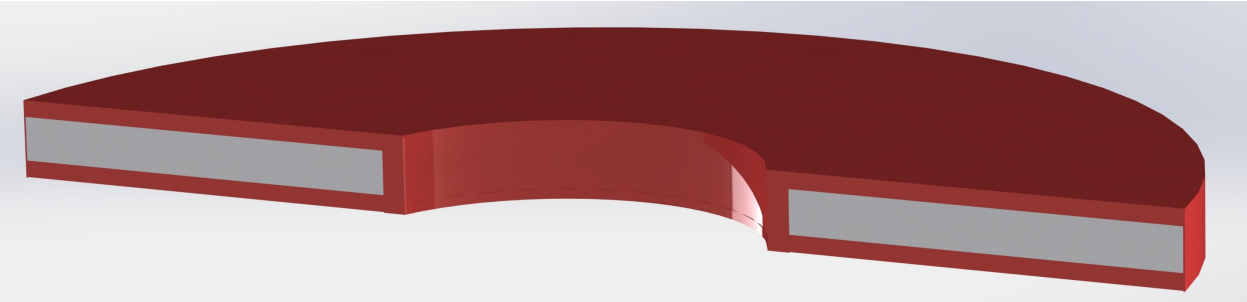


Figure 5.19: Cross-section view from the side of the transformer core

5.3 Transformer Core Primary Winding Design

In this section, I designed a primary winding that encases the transformer core. It is important that the conductive casing is as thin as possible, but still thick enough to allow the ability in making the LTD modular and easy to maintain. Using inspiration from Dr. Jiang's

LTD and the LLE-LLNL LTD, I came up with a hybrid LTD winding that allows for the ability to easily maintain the LTD, while keeping the stage as thin as possible. There would only be one copper disk on top of the Metglas core, which would be screwed into the PCB. The PCB will act as the ground return path for the transformer core.

The best conductive material to use in this LTD application would be C18200chromium copper. This alloy has a good compromise between high conductivity with 85% IACS of copper and the strength of the added chromium. The mixture allows for easy machining, since pure copper is too soft. The machining needed for my transformer winding is also made to be simple, thus I would not need a harder alloy. [7]

An excellent company to buy C18200 from is the Cadi Company Incorporation. The following dimensions are shown below.

- Outer C18200 Diameter: $7.54'' + 0.060''$
- C18200 Height: $0.56'' + 0.035''$

The next subsection is going to show the orthographic drawing of the chromium copper disk.

5.3.1 Primary Winding Copper Plate

An orthographic drawing of the primary winding plate can be seen in appendix .2.

A rendering of the primary winding plate is shown in Figure 5.20 below.

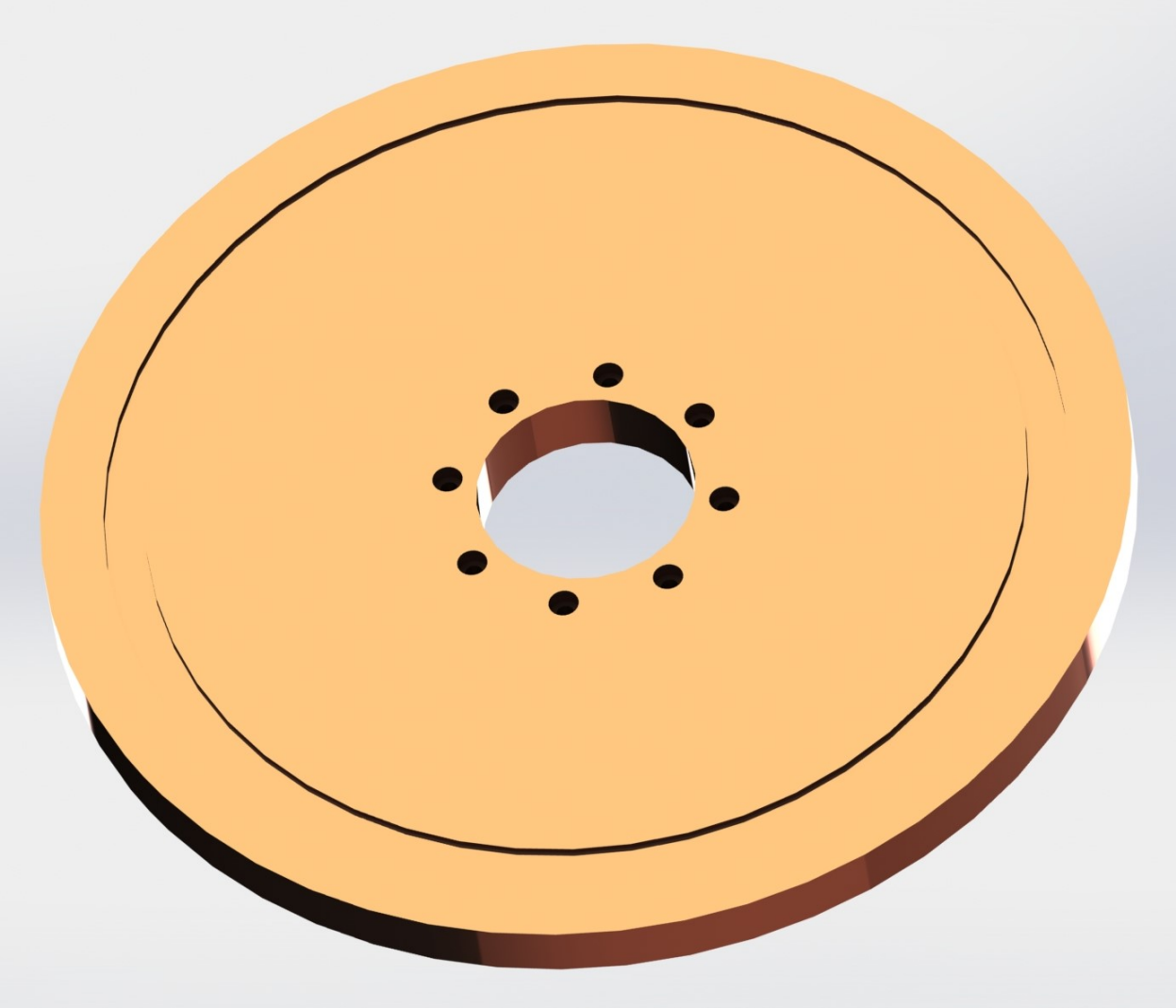


Figure 5.20: View of the primary winding plate

Of note is that on the other side of the primary plate, there are no cuts since the spacing between stages will be done by using a snap-in technique. There would be no need for spacers.

5.3.2 PCB Design

The PCB board needs to be able to mount on the primary disk winding. Non-magnetic brass screws will be used to secure the connections. In order to have enough room to mount electronics onto the PCB, the overall diameter needs to be $12^{''}$. This means the overall diameter of the LTD will be more than one foot, but only slightly. The orthographic drawing for the PCB design can be seen in appendix .3.

A rendering of the PCB board can be seen in Figure 5.21 below.

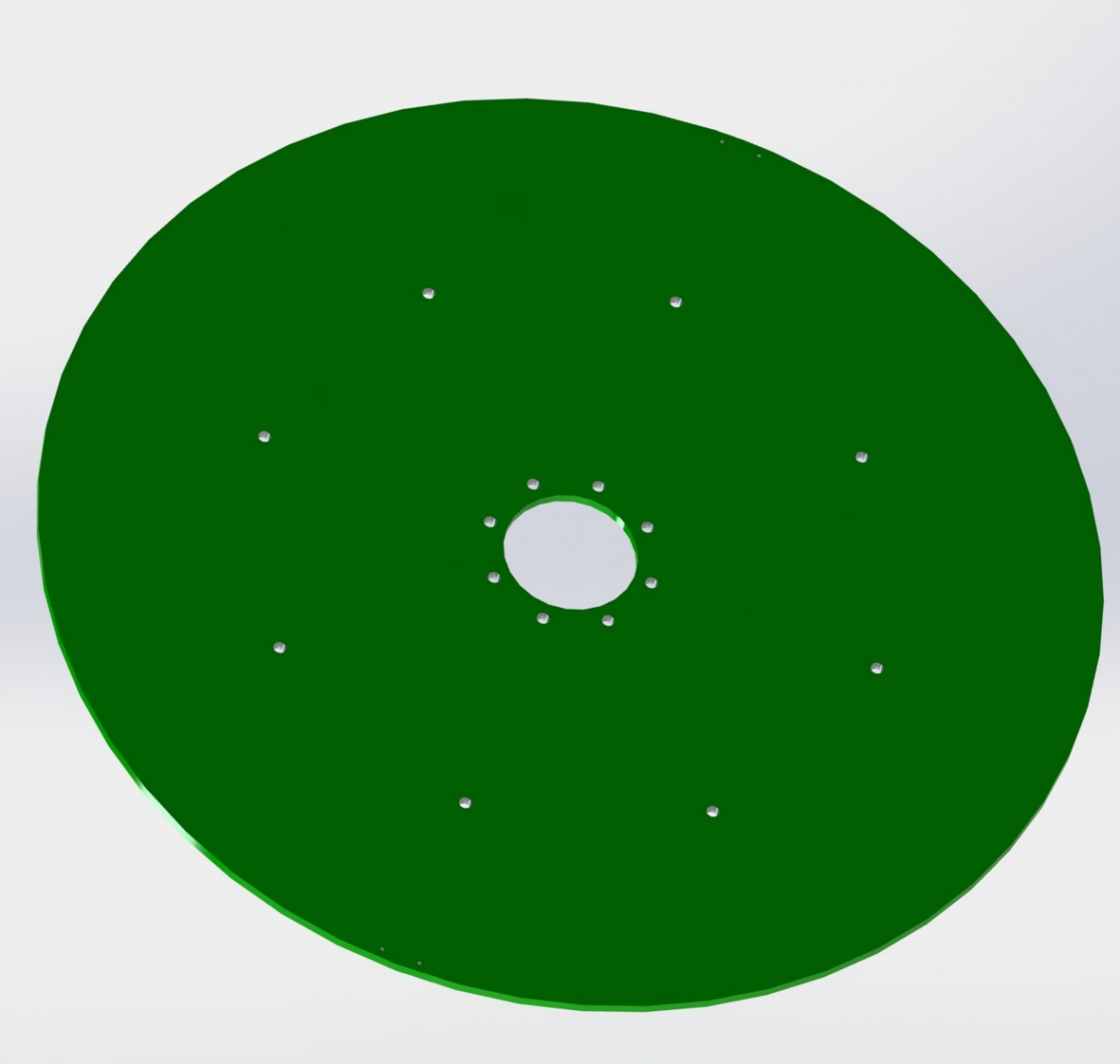


Figure 5.21: PCB rendering showing mounting holes to the primary copper disk

5.3.3 LTD Transformer Stage Assembly

A rendering of the entire LTD transformer stage be seen in Figure 5.22 below.

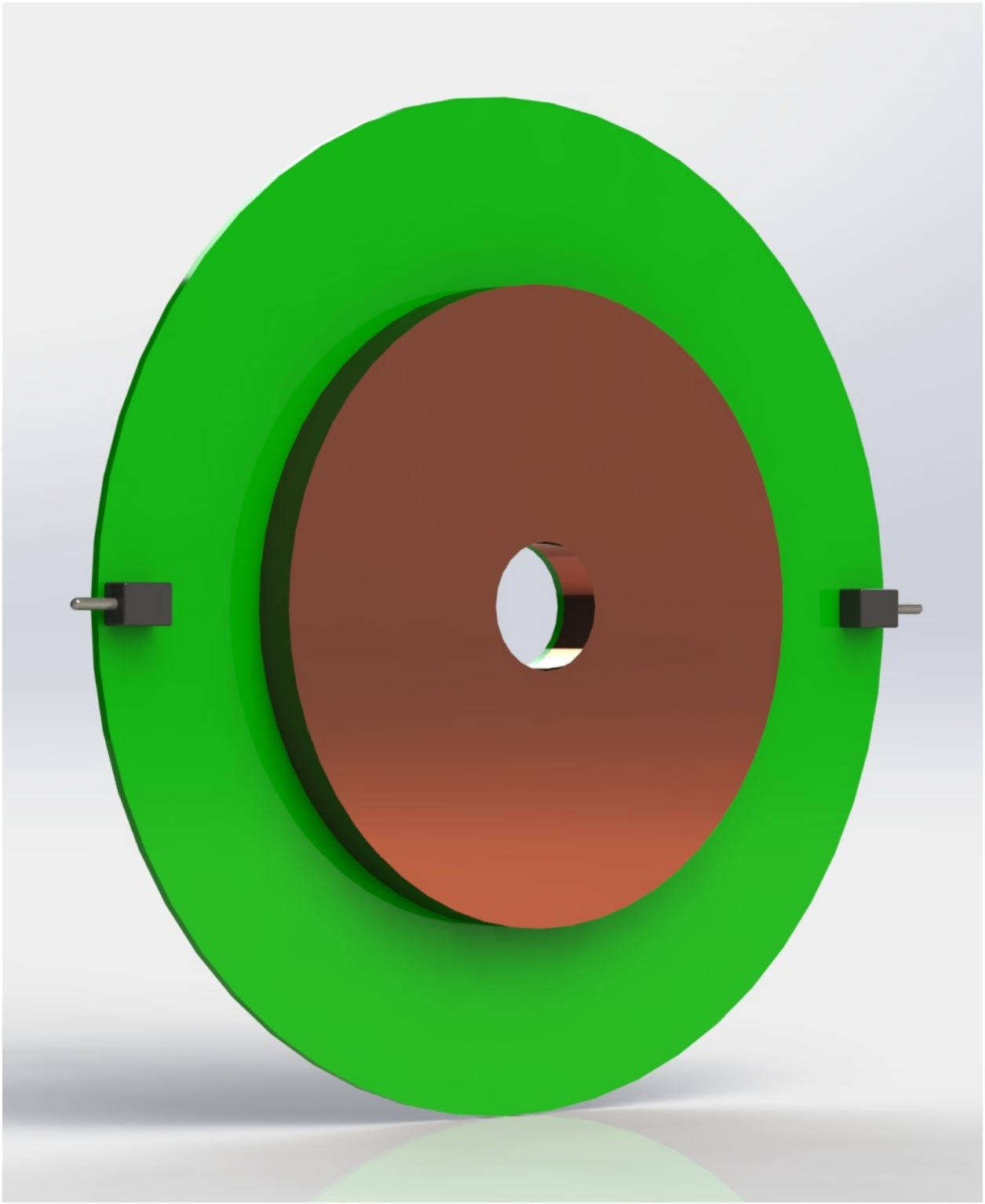


Figure 5.22: LTD stage top rendering

The other side of the LTD transformer stage be seen in Figure 5.23 below.

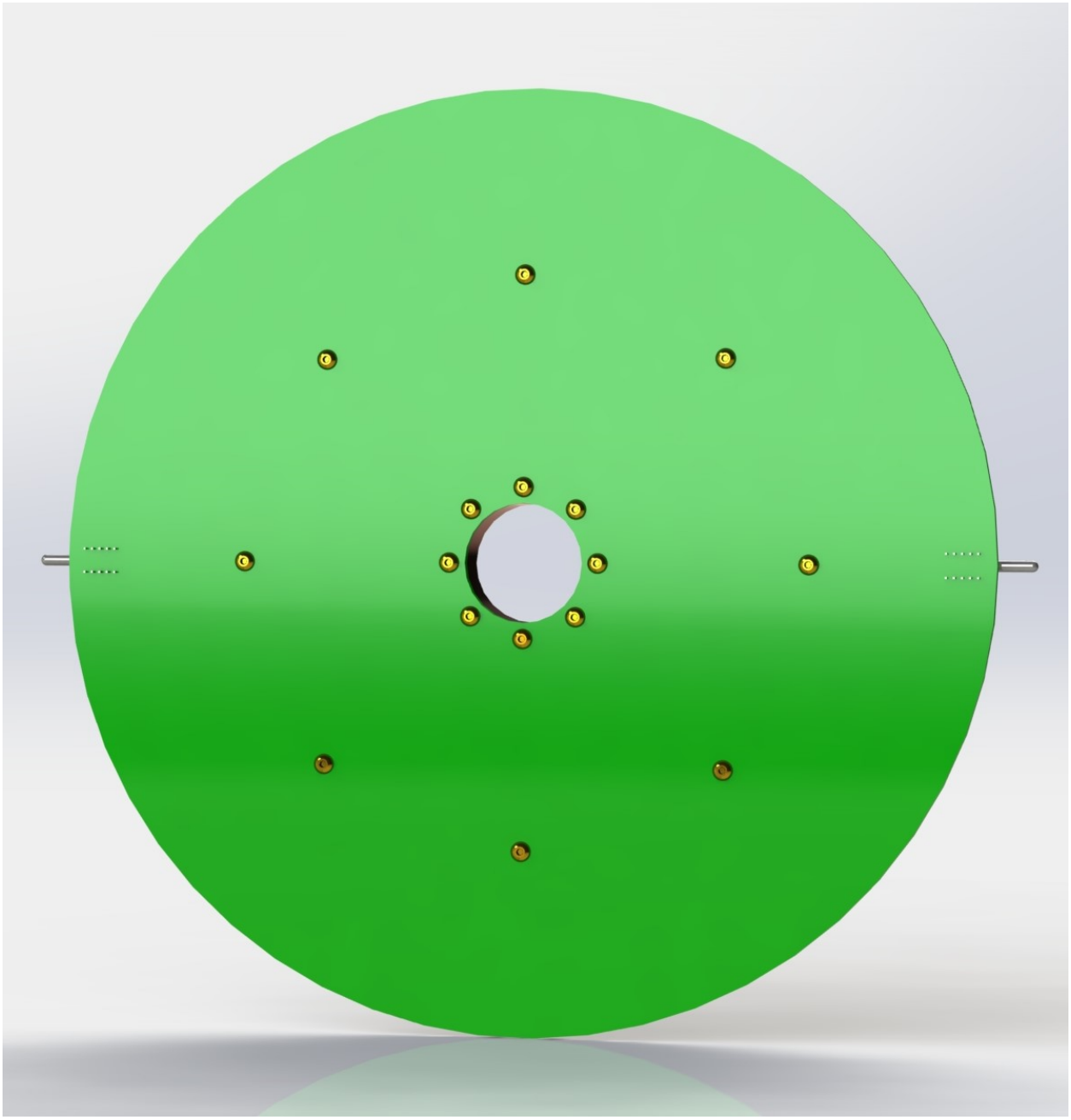


Figure 5.23: LTD stage bottom rendering

5.4 Determining Estimated Size and Cost of LTD

Running the MATLAB feasibility study program to get the estimated size and cost of the LTD yields the following values that can be seen in Table 5.5 below. In this program, I am using the energy level 7.92J with the capacitor that I found. This is slightly different from the feasibility study chapter of 7J. This value comes from finding a ceramic capacitor capable of supporting up to 2kV, and a 2200pF ceramic capacitor was found that has a small enough size to be useful while not costing a lot. The model number is C1210C222KGRACAUTO and the manufacturer is Kemet. I can use four of these capacitors in parallel to increase the energy output. Thus, 8.8nF multiplied by an estimated 30 solid-state switches a stage across 23 stages is where the energy value of 7.92J comes from. I use four capacitors instead of one in order to maintain an even flow of current around the entire circumference of the transformer core.

Parameter	**Values**
LTD Cost	$6,918
Stages	23
Parallel Switches Per a Stage	30

Table 5.5: Estimated Cost of LTD from MATLAB program

It is important to note from this table that the cost is only considering the price of switches, capacitors, and some driver circuitry. With this in mind, the LTD only costs approximately $7,000, which is reasonable. Keep in mind this estimate is not considering bulk pricing of all the items.

5.5 Fiber Optic Signal to LTD Stages from Central TTL Input

The initial signal that gets sent to the LTD to trigger all the stages is the most important step in achieving minimum jitter, thus decreasing the rise time of the LTD due to be synchronization between solid-state switches. As is discussed in the related work chapter, there are two different ways in going about sending the control signal to the LTD. One is using equal length coaxial cable to each of the LTD stages. The other is using a fiber optic cable to each stage.

After a discussion with professionals in the LTD field, it has been noted that fiber optics will help to ensure the best possible performance. Fiber is immune to EMIs that can be emitted by the pulse and is not effected by the transmission line effects that coaxial can experience. The other issue with using coaxial cable is the difficulty to ensure that the same level of current is passing through all of the lines.

In this section I start from where the triggering pulse is made and go down to the fiber optic receiver. The triggering pulse is made by a DG645 from Stanford Research Systems. The cost for one of these units is $4,295. Four LTDs could be reliably triggered by this unit with picosecond resolution. Later down the road, it would be possible to calibrate paralleling of LTDs to lessen jitter into an experimental apparatus. The DG645 can easily be programmed using serial communication. The voltage output of this unit can be programmed up to 5V.

A BNC connector would be used to connect the triggering signal to a fiber optic transmitter unit. This is where it is critical to choose the right fiber optic cable. To bring it back, there are two types of fiber optic cables that can be used: singlemode and multimode. Singlemode fiber is usually more expensive than multimode, but has superior performance due to low

dispersion. As is in the name, single-mode fiber cannot use a range of frequencies, thus it needs to be operated by a laser. Multimode fiber is used for any LED transmitter as it can take the range of frequencies from an LED and send it to the receiver. However, there will be dispersion, which will look like a bell-shape curve. This will cause jitter related issues when considering that this signal will be split in 23 ways to trigger each stage. Thus, it has been decided that singlemode fiber would be the best technology to use, and as will be seen, the price is not expensive.

First, a fiber optic splitter will be needed. From Fibermart, a 1x24 FBT splitter can be found for $95. It is small and easy to use. A picture of it can be seen in Figure 5.24 below.

Figure 5.24: Image of the 1×24 fiber optic splitter. Image from Fibermart. [34]

There are two main connector types that can be used angled physical contact (APC) or ultra physical contact (UPC). APC uses a 8-degree cut to lessen reflected light at the end of the fiber from traveling directly back to the transmitter. This is known as return loss. This can

help lessen error in more sensitive applications. UPC meanwhile is simply a straight cut and reflected light will come directly back to the transmitter. In Figure 5.25 below, the difference between APC versus UPC can be seen. [25]

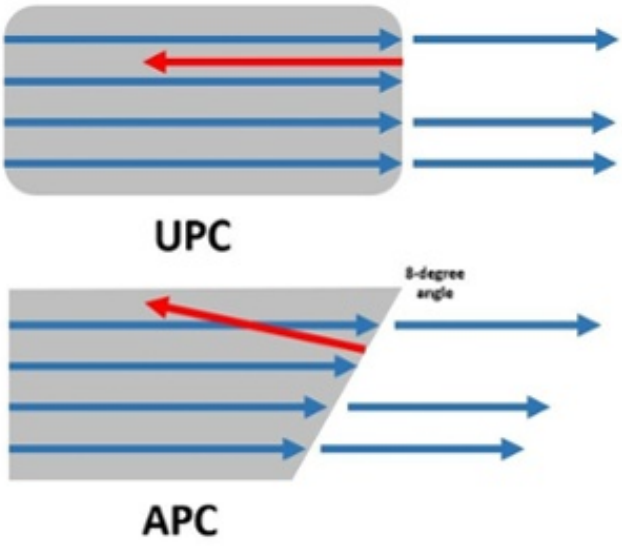


Figure 5.25: Physical difference and reflection effects of UPC versus APC. Image from D. Crawford. Image made in August 2014. [25]

For this LTD, using APC fiber optics will help to lower jitter. The fiber optic splitter will also use single-mode in order to mitigate the effects of dispersion.

A fiber optic receiver on Digikey can be bought for $27.50 a piece. It has a 200VW gain and a recommended output voltage of 3.3V. The receiver also has a 3dB bandwidth of 7GHz, which is well under a 1ns rise time. To easily use the already available 1x24 fiber optic splitter, the power output of a transmitting laser diode will be split in 24 ways. The goal is to directly power a MOSFET driver to drive all of the MOSFET drivers in a stage. The LM5134BMF MOSFET driver has a high-logic value threshold input voltage of 2.4V. Dividing 2.4V by the 200VW gain leads to a 0.012W laser signal into the receiver unit. Multiplying this value by 24 comes out to be 288mW. This means a fiber optic laser diode must be capable of

supplying at least 288mW in order to trigger all of the stages.

A photo of this receiver can be seen in Figure 5.26 below.

Figure 5.26: Photo of fiber optic receiver. Image from Digikey. [27]

This fiber optic receiver can use at maximum a 5V supply. The receiver is connected to a flexible wire and can be bent at a 90 degree angle. The circuitry to make use of this signal will be discussed in the next section.

As was discussed, a laser will be needed in order to operate a singlemode fiber. For $2,740 on SemiNex Laser Diodes a low power 1310nm single-mode laser can be bought. The laser's model number is 14BF-104. A picture of this laser can be seen in Figure 5.27 below.

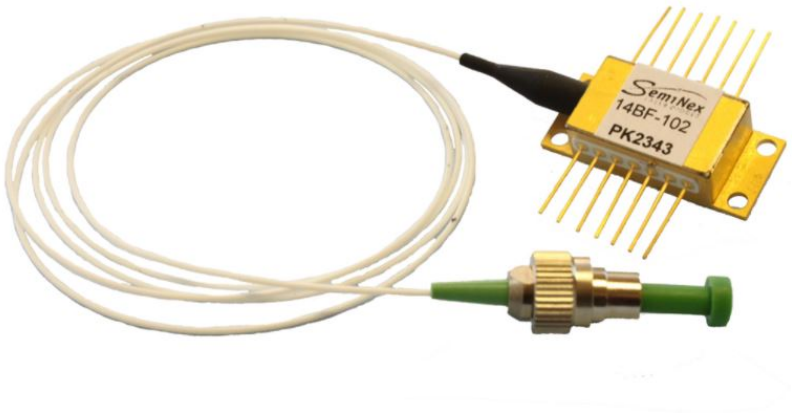


Figure 5.27: Photo of fiber optic transmitter. Image from SemiNex. [11]

In Figure 5.28 below, a graphic of the pin configuration for the laser diode can be seen.

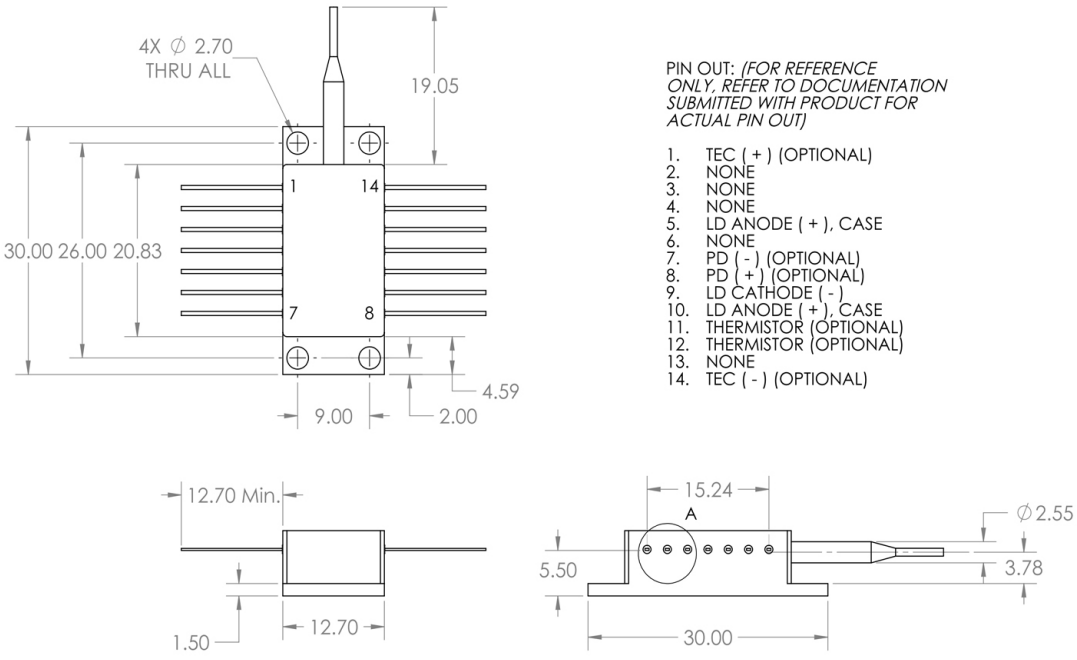


Figure 5.28: Pin configuration of 14BF-104 laser diode. Image from SemiNex. [11]

For the model number I am considering, thermoelectric cooling (TEC) will be included. This is useful to keep the laser operating at the temperature I would want. Even more useful, the laser's wavelength can be adjusted by changing its temperature. From the manufacturer, this can be changed by 0.55nm per degree Celsius. [28]

Pins 5, 9, and 10 are going to be connected to the DG645.

5.6 Design of LTD Stage

This section goes over the complete design of a LTD stage. Diagrams are shown to explain the high-level concepts, then eventually go into schematic diagrams. What is not fully shown is the full PCB board as it will be part of future work. However, a PCB design going into one brick is shown.

5.6.1 Fiber Optic TTL to Driver Circuitry

As designed in the last section, the fiber optic receiver has its output directly connected to the TI MOSFET driver in order to trigger all of the MOSFET drivers on the stage.

A functional block diagram in Figure 5.29 below shows the connections between all of the components.

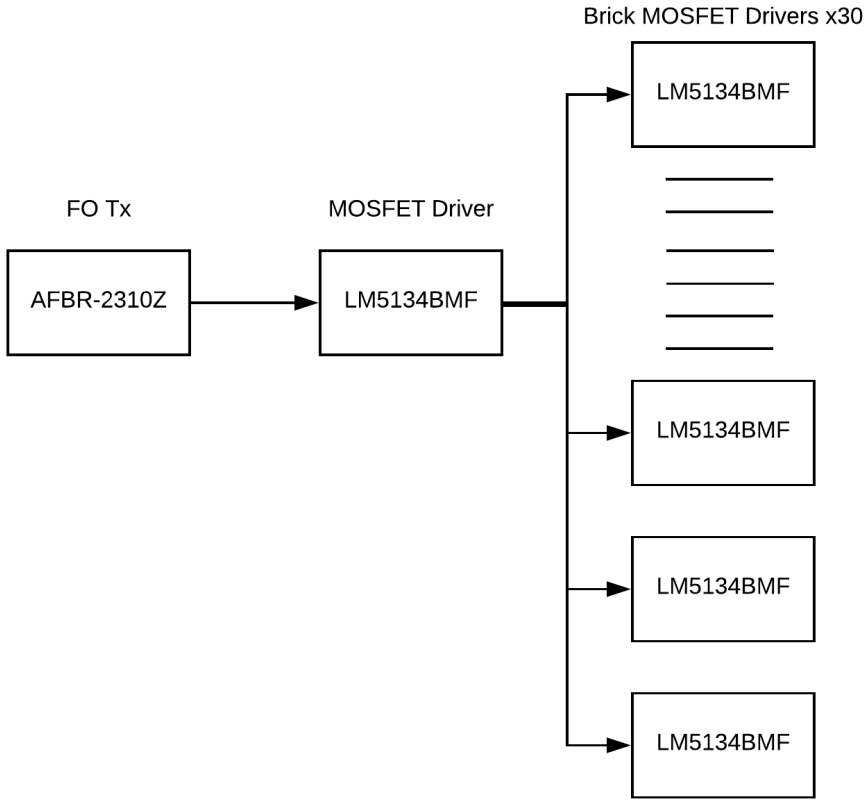


Figure 5.29: Functional block diagram of fiber optic Rx to drivers

5.6.2 Driver Circuitry to Solid-State Switch

The driver circuitry to solid-state switch being used to pulse the signal into the LTD is a critical aspect in terms of running the solid-state switch at its optimal performance while achieving minimum jitter. Emphasize will be placed on keeping all driver circuitry as close to each other as possible to the solid-state switch.

The TI MOSFET driver will supply a TTL signal to an intermediary GaN MOSFET. This will then supply a sufficient gate-source voltage to the SiC MOSFET.

A functional block diagram in Figure 5.31 below shows the connections between all of the components.

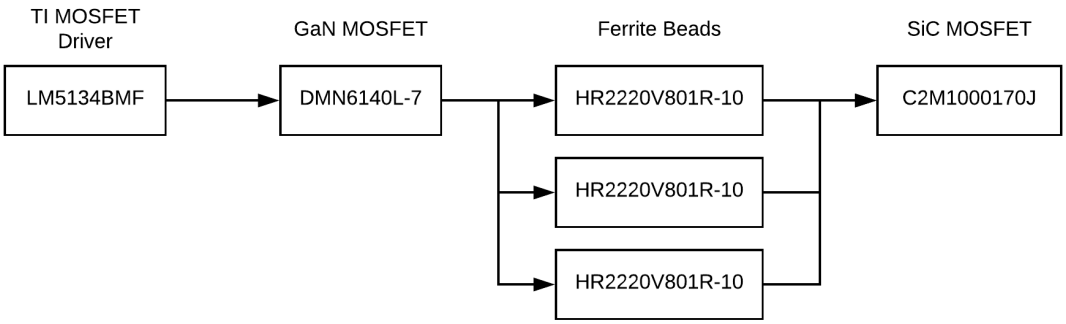


Figure 5.30: Functional block diagram of fiber optic Rx to drivers

After the SiC MOSFET, there would be TVS diodes to prevent voltage transients from destroying the circuit.

5.6.3 LTD Stage Schematic Diagram

For the brevity of this paper, only one full brick is used in the schematic as all bricks are connected to the main MOSFET driver the same way in parallel to each other. The schematic diagram can be seen in appendix .4.

LTD Stage Schematic Bill of Materials

A schematic label key and bill of materials can be seen in Table 5.6 below. Keep in mind this bill of materials is only considering the stage fiber optic receiver circuitry with a single brick. The parts for all additional bricks are the same. In the next chapter, the full bill of

materials will be shown.

Schematic Label	Part Type	Value	Case Type	Distributor	Manufacturing Number	Cost
C2,C3	Capacitor	1nF	0805	Digikey	C0805C102J5HACAUTO	$0.18
C1,C4,C7	Capacitor	0.1uF/100nF	0805	Digikey	C0805C104J5RACTU	$0.18
C5,C6,C8,C9	Capacitor	2.2nF	1210	Digikey	C1210C222KGRACAUTO	$1.10
L1	Inductor	15nH	0805	Digikey	HK212515NJ-T	$0.22
L2,L3,L4	Ferrite Bead	Spec Sheet	2220	Digikey	HR2220V801R-10	$2.02
Q1	SiC MOSFET	1.7kV	TO-263-7	Digikey	C2M1000170J-ND	$5.87
Q2	GaN MOSFET	60V	SOT-23	Digikey	DMN6140L-7	$0.45
R1	Resistor	8.2ohm - 0.5W	0805	Digikey	ERJ-6DQJ8R2V	$0.23
R2	Resistor	3.9 ohm - 0.5W	1210	Digikey	CRCW12103R90JNEA	$0.24
R3	Resistor	10kohm - 0.5W	1210	Digikey	ERJ-14YJ103U	$0.16
U1	FO Receiver	3.3V	Module	Digikey	AFBR-2310Z	30.64
U2,U3	MOSFET Driver	Single Driver	SOT-23-6	Digikey	LM5134BMF/NOPB	$1.60
U4	Phoenix Header	4-Terminal	Module	Digikey	1803293	$1.63
U5	High Voltage Header	3kV Rating	Module	Mouser	MDF51K-2P-12DSA(20)	$0.56
U4	Phoenix Plug	4-Terminal	Module	Digikey	1803594	$4.54
U5	High Voltage Plug	3kV Rating	Module	Mouser	MDF51-2S-12C	$0.31

Table 5.6: Bill of Materials for single LTD stage with a single brick

LTD Stage Schematic Diagram With Low Fiber Power

Some research has been done in looking at the possibility in using a low powered fiber optic transmitter. This is possible, however it comes with quite a bit of complicated circuitry to amplify the fiber optic receiver signal. There is a Texas Instrument comparator capable of operating in the picosecond timescale. This device is called the LMH7322.

A schematic utilizing this comparator can be seen below. Note, that this circuit is untested and potentially minor changes would be needed in the final design if this were to be used. This schematic can be seen in appendix .5.

The LMH7322 has an output that does not rest at zero volts when at a logic low. This means inserting a DC offset on the output to pull it down to zero. Then amplifying the logic

high value through a MOSFET. The MOSFET will amplify the 0.4V coming into the gate to a voltage level usable by the TI MOSFET driver. The current limiting resistor R13 needs to be set to a value that allows enough current to flow to all 30 brick MOSFET drivers in order to switch them at rated speeds.

There is one section that has not been designed in this schematic, which is adding in the +5V and 3.5V offset voltage source. It would be easiest to add a DC-DC converter that can take +12V and turn it into a 3.5V source and another DC-DC converter that can turn it into a +5V source. This in turns lowers the complexity of the power supply systems that feed into the LTD overall.

LTD Stage Schematic Low Fiber Power Bill of Materials

A schematic label key and bill of materials can be seen in Table 5.7 below. Just as with the previous BOM, this one only considers one brick.

Schematic Label	Part Type	Value	Case Type	Distributor	Manufacturing Number	Cost
C2,C3	Capacitor	1nF	0805	Digikey	C0805C102J5HACAUTO	$0.18
C1, C7	Capacitor	0.1uF/100nF	0805	Digikey	C0805C104J5RACTU	$0.18
C5, C8	Capacitor	10uF	1210	Digikey	EMK325BJ106KN-T	$0.38
C4, C6	Capacitor	10nF	1210	Digikey	CL32C113JBHNNNE	$0.55
C9, C10, C11, C12	Capacitor	2.2nF	1210	Digikey	C1210C222KGRACAUTO	$1.10
L1	Inductor	15nH	0805	Digikey	HK212515NJ-T	$0.22
L2,L3,L4	Ferrite Bead	Spec Sheet	2220	Digikey	HR2220V801R-10	$2.02
Q1	SiC MOSFET	1.7kV	TO-263-7	Digikey	C2M1000170J-ND	$5.87
R1	Resistor	8.2ohm - 0.5W	0805	Digikey	ERJ-6DQJ8R2V	$0.23
R2	Resistor	3.9 ohm - 0.5W	1210	Digikey	CRCW12103R90JNEA	$0.24
R3, R4, R7, R12	Resistor	10kohm - 0.5W	1210	Digikey	ERJ-14YJ103U	$0.16
R5	Resistor	2.5kohm - 0.5W	1210	Digikey	ERJ-14NF2491U	$0.25
R6	Resistor	10ohm - 0.5W	1210	Digikey	ERJ-14YJ100U	$0.16
R8, R9	Resistor	5kohm - 0.5W	1210	Digikey	ERJ-14NF4991U	$0.25
R10, R11	Resistor	270ohm - 0.5W	1210	Digikey	ERJ-14YJ271U	$0.16
R13	Resistor	TBD	1210	Digikey	TBD	
U1	FO Receiver	3.3V	Module	Digikey	AFBR-2310Z	30.64
U2	MOSFET Driver	Single Driver	SOT-23-6	Digikey	LM5134BMF/NOPB	$1.60
U3	GaN MOSFET	60V	SOT-23	Digikey	DMN6140L-7	$0.45
U4	Phoenix Header	4-Terminal	Module	Digikey	1803293	$1.63
U7	High Voltage Header	3kV Rating	Module	Mouser	MDF51K-2P-12DSA(20)	$0.56
U4	Phoenix Plug	4-Terminal	Module	Digikey	1803594	$4.54
U7	High Voltage Plug	3kV Rating	Module	Mouser	MDF51-2S-12C	$0.31
U5	Comparator	700ps speed	24-WQFN (4x4)	Digikey	LMH7322SQ/NOPB	$9.35
U6	MOSFET	Vgs-th = 0.3V	SOT-23-3	Digikey	DMG2302UK-7	$0.45

Table 5.7: Bill of Materials for single LTD stage using low power fiber with a single brick

5.6.4 High-Voltage Routing Considerations

For the PCB design, a high-voltage line needs to be routed in a circumference around the MOSFET drivers, and remain only on the top layer of the PCB. Dr. Jiang's LTD from the literature review chapter is taken as inspiration in how to route a high-voltage PCB line.

5.6.5 PCB Board Design

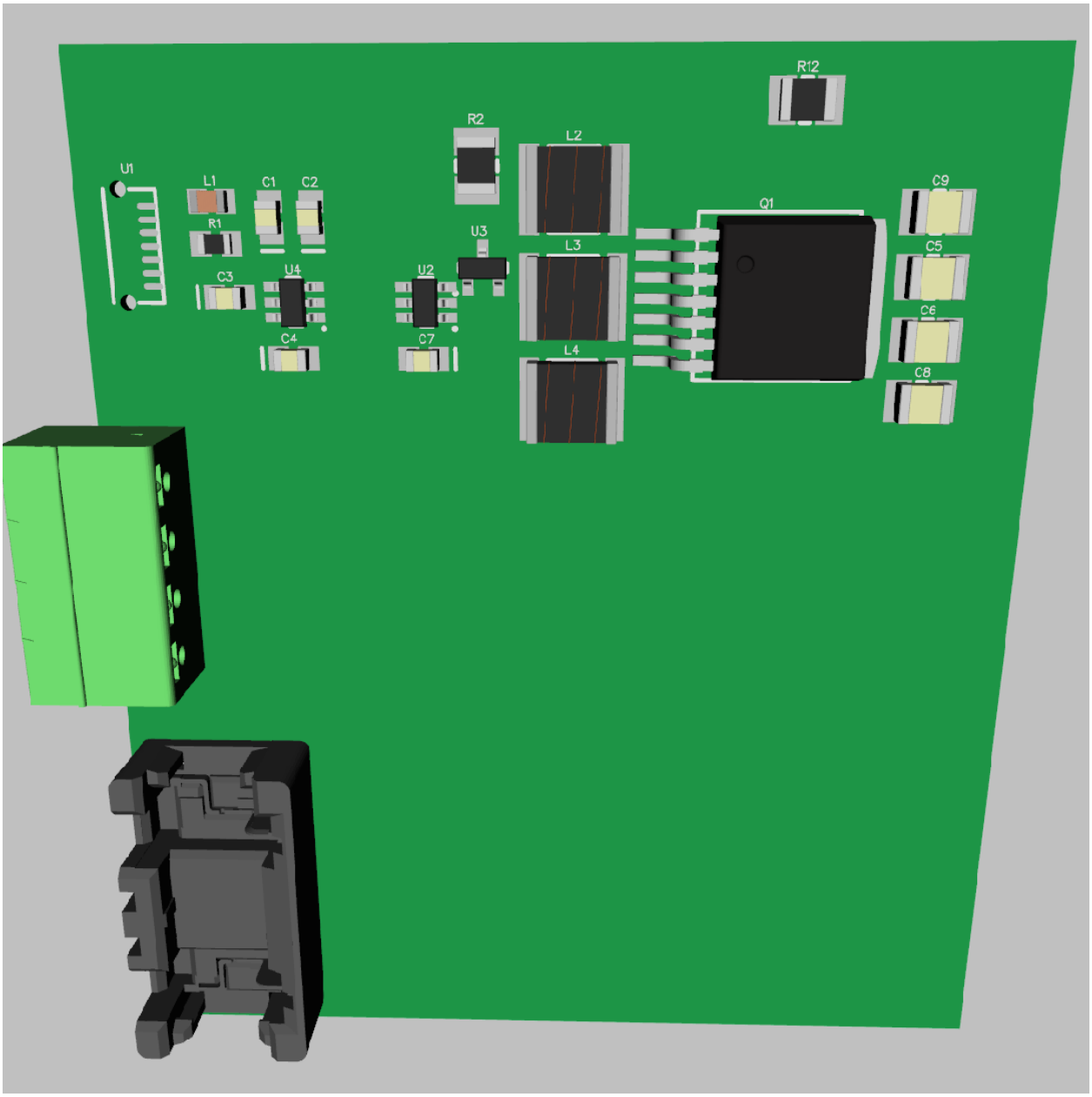


Figure 5.31: 3D model showing LTD stage inputs and a single brick

EMI Optimization

Should EMI become an issue in the LTD for the MOSFET drivers, it is possible to add additional shielding around them. However, due to the coaxial nature of the LTD, I do not expect a considerable amount of EMI that can affect the switching. Referencing other solid-state LTDs, no additional EMI shielding has been placed around the MOSFET drivers.

5.7 Design of LTD Stalk and Enclosure

This section goes into detail about the transformer's secondary winding, also known as the stalk. Both the metal used to make the stalk and the dielectric surrounding it will be brought up. After this, the section goes into the design of a custom enclosure.

5.7.1 LTD Stalk

The LTD stalk is the secondary winding or in this case a long rod that goes through all of the LTD stages. To get the length of the stalk needed, each LTD stage is $0.7''$ in height. Each stage must have enough air gap in order to standoff 1.7kV. The dielectric strength of air is 3kV/mm. [40] It would be good to have a factor of safety of three in between stages due to transients that could occur. This means the total standoff voltage needs to be at least 5.1kV, thus a 2mm or a $0.0787''$ gap will suffice. There will be 23 stages, thus $Stalk_{length} = (Stage_{height} + Stage_{gap}) * N_{stages}$. This comes out to be $17.91''$ in length. Keeping the LTD as short as possible will help to lower the rise time of the output pulse.

Dielectric Surrounding Stalk

A dielectric surrounding the stalk needs to be able to standoff at least 30kV which is the expected max voltage. It also needs to have a low permittivity in order to have the least

amount of capacitance as possible on the transmission line.

One such material is Polyvinyl Chloride (PVC). Its dielectric strength can be seen in Figure 5.32 below.

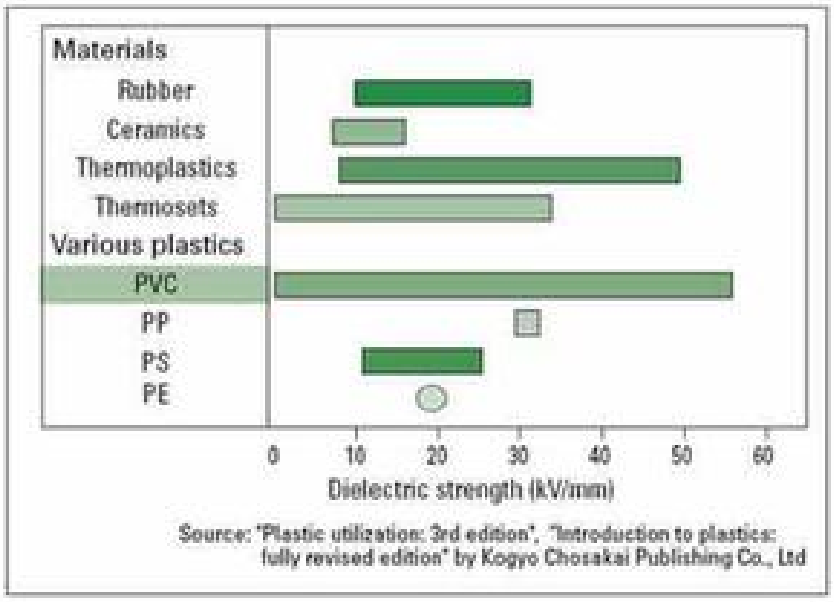


Figure 5.32: Table of dielectric strength ranges in kV/mm. Image from PVC website.[55]

As can be seen from the table, PVC has the capability of reaching about 55 kV/mm. This means I would need 1mm thickness of PVC to have almost a factor of safety of two. I also want to consider that the thinner the dielectric, the less capacitance that can be stored, and the closer the secondary can be to the primary winding.

Another material that could be used is Kapton. Its dielectric strength is 3,900 Volts per 5mil. [26] This means with a safety factor of two or 60kV standoff, Kapton just needs to be approximately 15mil. For ease of manufacturing, a 5mil thick sheet can be used and rolled up three times. This is enough distance as well to prevent tracking within the Kapton layers. With such a small thickness of 15mil or 0.381mm, Kapton is superior to PVC that requires

at least 1mm thickness. This will help optimize the LTD's rises time from the capacitive transmission line effects.

Stalk

For the outer diameter of the stalk, it cannot exceed $1.54''$. The stalk is small enough that a solid piece of copper can be used, but it can also be hollow due to the skin effect. I have determined that the length of the stalk should be $23''$ in order to contain all the LTD stages and have enough length to rest on $0.5''$ thick aluminum supports. From the Cadi Company, I can use a C10100 copper alloy rod which has a high purity of copper of 99.99% for $164.50. [41]

LTD Stage Standoffs

With each LTD stage being able to snap into place along the enclosure, there is no need for standoffs between stages. The air gap will remain to be 2mm in between stages.

5.7.2 LTD Enclosure

I have decided that a rectangular enclosure would work best for my LTD. This is because finding a circular aluminum enclosure becomes expensive at the diameter I am looking for. I also need to consider spacing between the PCB board and the side of the enclosure in order to route fiber optic cables and wires. Thus, I would need an enclosure that is 14 by 14 inches. This is a little above what I originally wanted, but this would ensure that I have safety, good wire organization, and ease of maintainability.

5.8 Design of the Rogowski Coil

In order to be able to measure the current coming out of the LTD and the shape of the pulse, a rogowski coil must be made. This device takes the derivative of the current and turns it into a voltage. From there, an integrator must be used to recover the original current signal. A coaxial cable can be used to create one. Using the formula $V = -K_1\ N\ A\ \frac{di}{dt}$ the output voltage of the rogwoski coil can be found. I know that the maximum current coming out of the LTD will be around 500A. The time it takes for it to reach 500A would be near 10ns. This can give me $\frac{di}{dt}$, which would be $50\ \times\ 10^9$. K_1 is the permeability of a vacuum or $4\ \pi\ 10^{-7}$. N is the number of turns per unit length or $\frac{N}{l_e}$. The l_e in this case would be the circumference of the rogowski coil or $2\ \pi\ r$. A is the average area per turn, which is the cross-sectional area the dielectric in the coaxial cable covers. Ideally, the rogowski coil should output between 5V-10V to be read by a DAQ. An excellent coaxial that is small and cheap to buy is RG-58. Its magnetic permeability can be assumed to be near that of air. Using a specially made MATLAB code to quickly find the output voltage value, the following parameters for the rogowski coil are written below.

- Coaxial Cable Type: RG-58
- Coaxial Cable Inner Conductor Diameter: $0.032''$
- Coaxial Cable Dielectric Diameter: $0.116''$
- Coil Radius: $3.0''$
- Number of Turns: 10
- Output Voltage: 9V

The code used to gather these parameter values can be seen in appendix **??**. The rogowski coil would have a radius of $3.0''$ which means when holding the coaxial cable, it would make

a circle of a six inch diameter with ten windings. In order to create the rogowski coil, the outer dielectric and outer conductor need to be stripped off a total of $41.34''$, while keeping an extra $0.25''$ of outer conductor to be soldered to the inner conductor winding back. Then the inner dielectric needs to be stripped off a total of $22.49''$ to expose the inner conductor. Finally, wrap the inner conductor with equal spacing back to where the exposed outer conductor is, then solder together. In order to prevent arcing between the rogowski coil and the LTD bus output, a semi-clear silicon rubber tube can be used. It is still possible to see the rogowski coil through the tube, which is good to see if anything is broken should the coil stop working. The length of tubing would be about $24''$. Kapton tape can then be used to prevent arcing between the silicon rubber and coaxial cable gaps. After all this is finished, add a crimped BNC connector at the end of the RG-58 cable.

5.8.1 DAQ to Measure the Rogowski Coil Signal

Since the rise time of the LTD is expected to be near 10ns. The frequency would be 100MHz. Using the Nyquist criteria, the DAQ being used would need to be able to handle 200MHz or 200MSs. Unfortunately this is an incredible fast sampling speed for DAQ technologies. National Instruments sells a DAQ capable of reaching this sampling speed called the PXI-5124. It is $8,289.90$ with 12-bit resolution. The cost is cut in half per a LTD considering it has two analog input channels. The filtering technology this DAQ is capable of must be turned off in order to reach 200MSs. Using the 1Minput, the DAQ is capable of going up to a 20Vpk-pk input. In order to house the PXI-5124, a PXI chassis capable of supporting at least 400MSs is needed to allow for the full operation of two channels. Thus, a PXIe-1078 can be used at a price of $2,406.60$. This chassis is capable of supporting up to three PXI cards and has a bandwidth of 1.75GBs, which is capable of supporting three PXI-5124 cards and all of their available channels at once. PXI technology can be integrated easily into LabVIEW.

5.8.2 Data Architecture When Saving DAQ Data

A proven data architecture for laboratories is .HDF5 which stands for Hierarchical Data Format. It is a simple to understand, and incredibly fast format. Both LabVIEW and MATLAB support the file type. In the .pdf below, a quick summary of how HDF5 works at a high-level is shown.

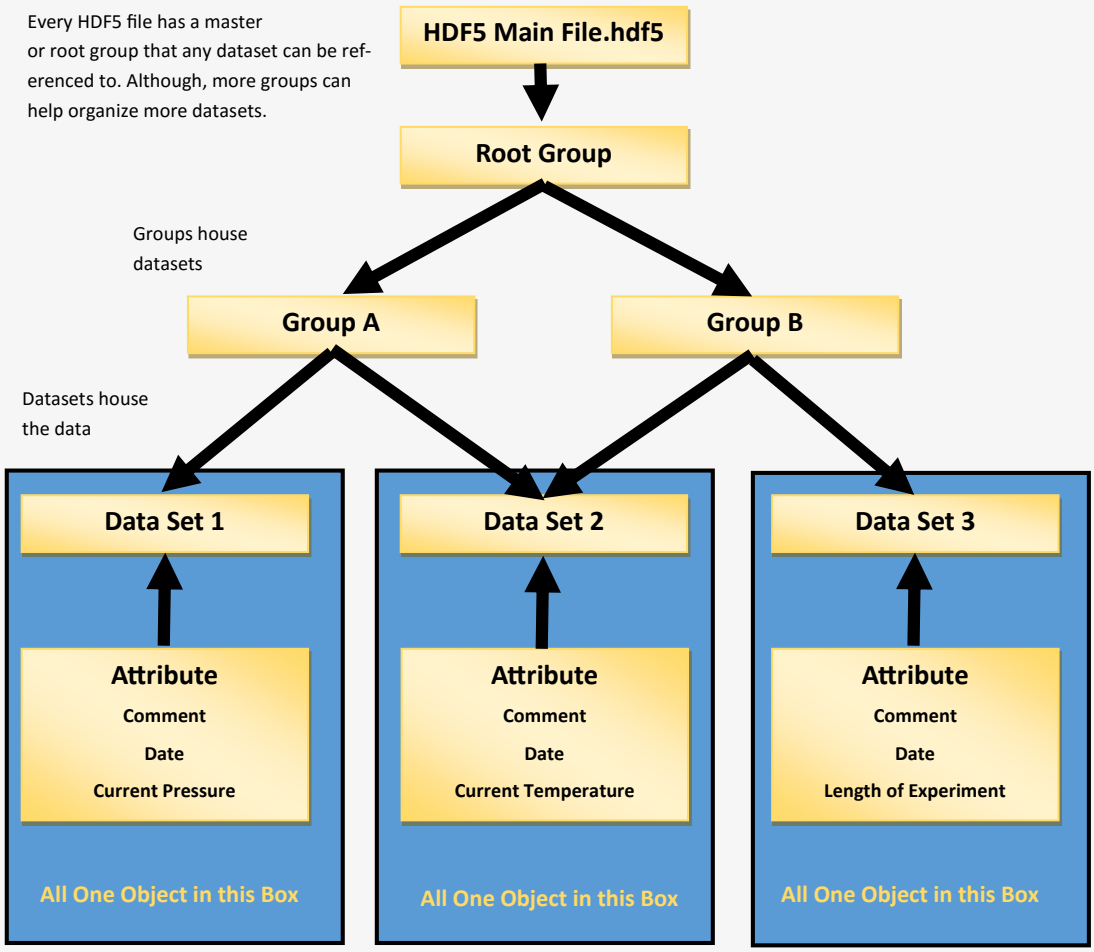
*Can be multiple paths linked to same object

HDF5 is a file architecture that can contain massive amounts of data in one file. It can also keep data from experiments organized.

Created By: Michael Sherburne

9/19/2016

Every HDF5 file has a master or root group that any dataset can be referenced to. Although, more groups can help organize more datasets.



Attributes are “metadata” for a dataset, adds in context. They are part of the dataset and can only be accessed when a dataset is opened.

As can be seen in the block diagram, .HDF5 can pack a lot of information into a single file. Even better, saving data and unpacking data from .HDF5 is fast as it is intended to save terabytes of data at once.

5.9 Full 3D Model of LTD

After putting everything discussed in this chapter together, a full 3D rendering of the LTD can be seen in Figure 5.33 below.

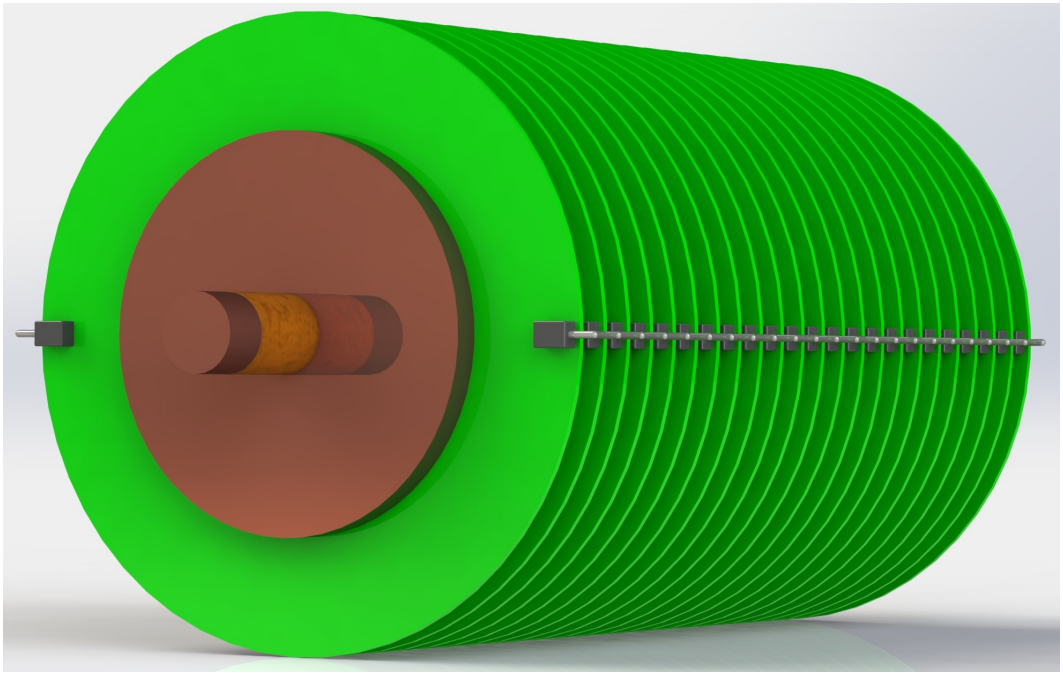


Figure 5.33: LTD 23 Stage rendering front view

A side view can be seen in Figure 5.34 below.

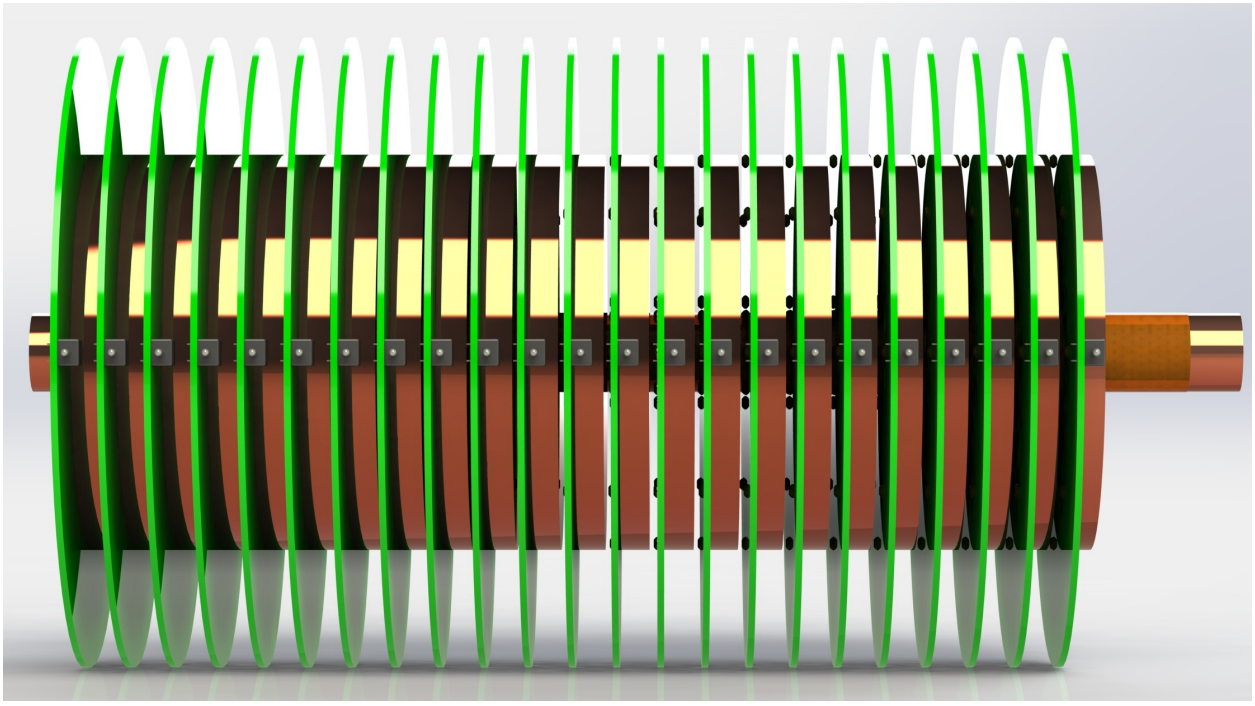


Figure 5.34: LTD 23 Stage rendering side view

The enclosure and snapping mechanisms added to the 23 stages can be seen in the rendering in Figure 5.35 below.

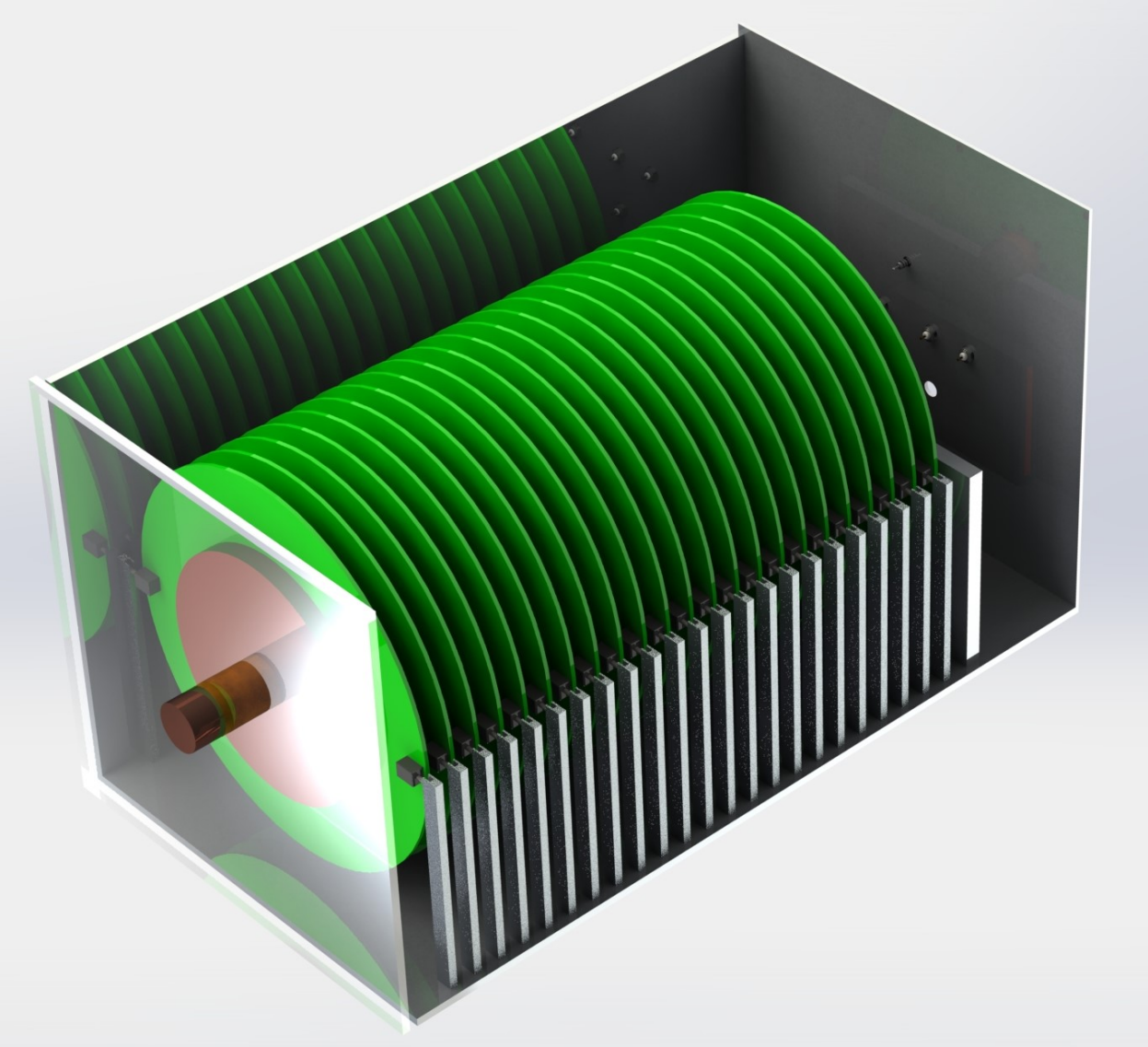


Figure 5.35: Front view of LTD 23 stage in enclosure with sides cut off

From the back side, all the connection points will be used to route the power supplies to the LTD. This can be seen in Figure 5.36 below.

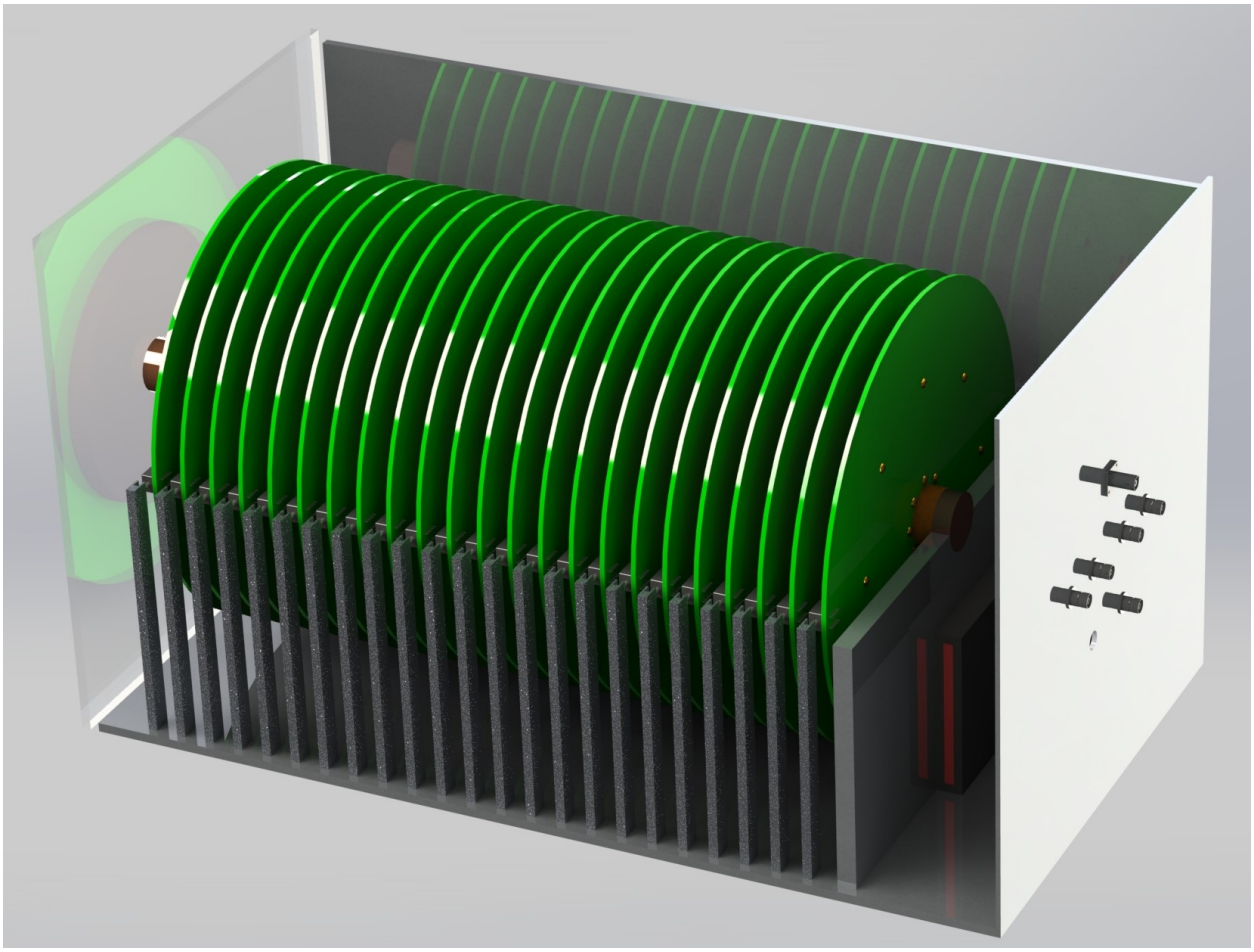


Figure 5.36: Back view of LTD 23 stage in enclosure with sides cut off

Another view of the LTD can be seen from the top in Figure 5.37 below.

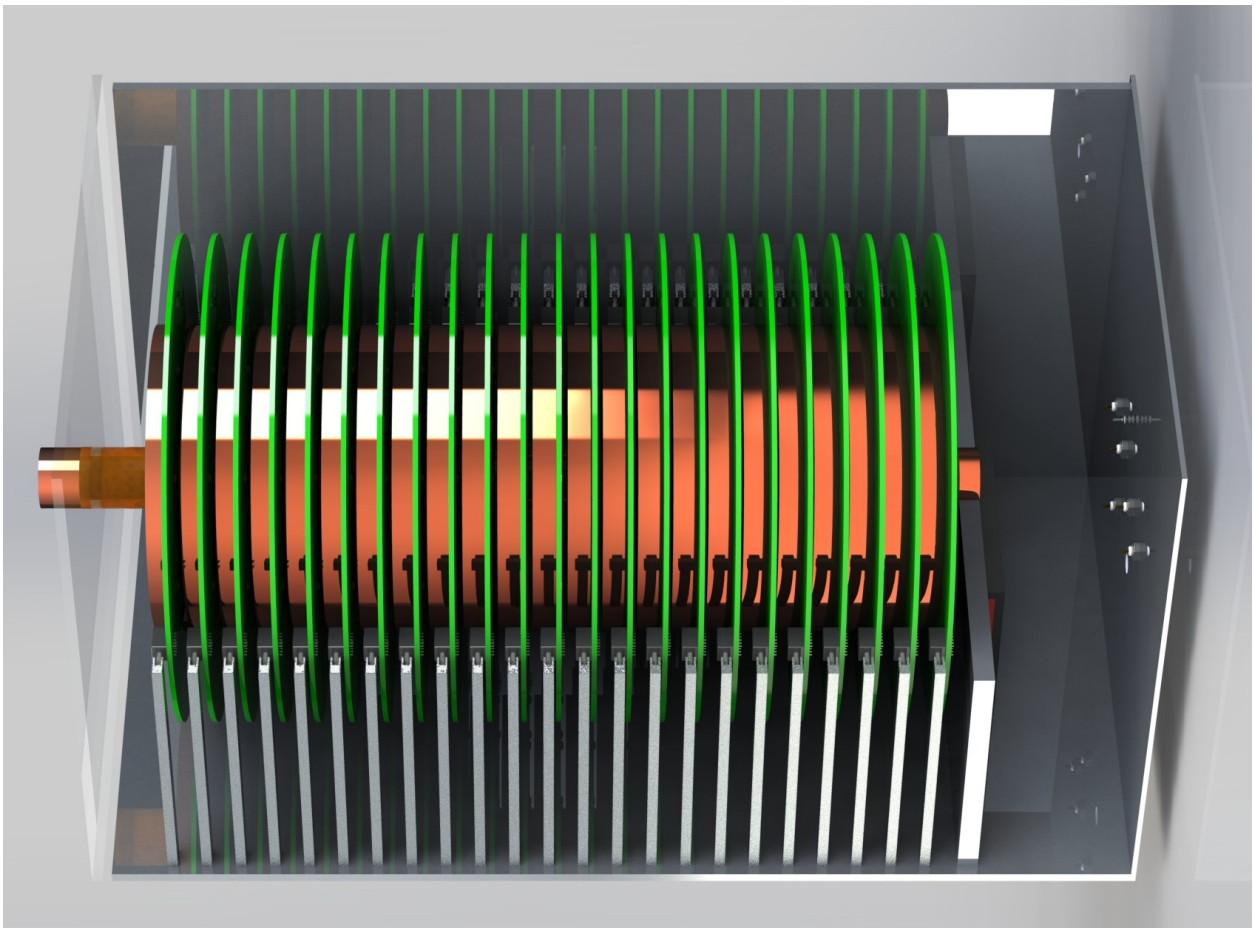


Figure 5.37: Top side view of LTD 23 stage in enclosure with sides cut off

5.10 Low Pass Filter Inductor for Transformer Core Reset

What will not be in the 3D modeling is the low pass filter inductor that routes a reverse DC current through the LTD stages in order to reset the transformer cores. In general it would set towards the front end of the LTD. The H-field needed to reset the core is 1.47Am. I can determine the DC current needed by rearranging the H-field formula from Biot-Savart's law which is $H = \frac{N\ I}{l_e}$. The circumference of the copper rod is $0.1229m$. The number of windings

is one. Thus, the required current to reset the cores is 0.181A. The low pass filter inductor needs to be able to hold off the full load of 30kV and 500A. The DC resistance of the copper rod that the DC current is going through is $8.2\mu\Omega$. This resistance is negligible, thus I can determine a resistor to be in series in order to supply the current. Using a 12V power supply already within the LTD system, the needed resistance is about 67Ω. The power dissipation is about $2.2W$. A chassis mount resistor that can be used is the HSA2568RJ for $3.06. The low pass inductor will need to be custom made from a manufacturer in order to be safely used.

5.11 Implementation Chapter Remarks

In this chapter I discussed how to design an entire solid-state LTD from selecting the switches and drivers, determining the transformer core to use, and to figuring out the spacing between stages. I evaluated through simulations and pricing out all the components of the LTD in the next chapter.

Chapter 6

Simulation of LTD

In this chapter I evaluated how my designed LTD compares against the target specifications. I chosen a two methods which are LTSpice simulations and looking at the logistics in making the LTD along with its costs. Ideally, I would like the LTD to have under a 10ns rise time, have a 500A output, a 30kV output, within a three foot by one foot diameter footprint, and have a reasonable cost, preferably under $100,000. Note, until I have the actual LTD made, jitter and EMI performance would not be testable.

6.1 Methods

The two methods to be used are LTSpice simulation with calculations and the logistics and costs. These two methods show the feasibility of our LTD design and models. Physical testing of the LTD will be seen in future publications. The results of these tests will be shown in the next section.

6.1.1 LTSpice Simulation

In this test, I used two LTD simulation models. One of them coming from a published paper, and another using a more in-depth model. A comparison was made between the two models and if the more in-depth model operates as expected, then it would be used for determining the performance of the LTD. Only one stage for each model will be simulated. This is because the computational software available to me is not able to test multiple stages in a way that I can finish this thesis in the limited time I have. However, this does not mean I cannot determine the expected rise time of the LTD reliably. A useful formula in calculation the LTD's overall rise time was used to act as a check and a way to tune the models. This equation is $T_R = 2\ N\ \sqrt{(L_K + L_1)\ C_1}$. [64]

Gathering Values for LTSpice Simulations

Both the detailed LTD model referenced in the background chapter in Figure 2.21 and the Brookhaven National Laboratory simplified LTD model share a few values. Additional values are also worked out here for the detailed model.

First, assumptions were made regarding the physical hardware being used. It is assumed that the MOSFET drivers being used can be over driven to operate faster than their stated rise times in their data sheet. It can also be assumed that the SiC MOSFET can also operate slightly faster than stated in its data sheet. From the MATLAB feasibility study, it was shown that the SiC MOSFET needed to run with at least a 1ns rise time in order to meet target specifications. Thus, the assumption is that instead of using the stated 4.8ns rise time in the data sheet, the SiC MOSFET can operate at 1ns rise time. This is reasonable, and does encourage future work in fully characterizing this new generation of SiC MOSFET technology.

Next, the total capacitance per a stage was calculated. Since each brick consists of four 2.2nF capacitors, and there are thirty bricks in parallel to each other per a stage. There is a total of 264nF per a stage.

Going along, I determined the transformer core parameters. The core's magnetizing inductance can be approximated using the inductance of a toroid formula. This equation is $L = \frac{\mu\ N^2\ A}{2\ \pi\ r}$. A is the cross-sectional area of the toroid, in this case from the implementation chapter, this value is $0.000356m^2$. [53] The radius of the winding is $3.5''$ which is $0.0889m$. The number of windings for a LTD transformer is one. The permeability as found in the implementation chapter is 0.420208. Plugging these values into the equation $L = \frac{0.420208\ *1^2\ *0.000356}{2\ \pi\ *0.0889}$ yields a $2.678mH$ magnetizing inductance. An additional assumption is going to be made for the purposes of this thesis. The leakage inductance is assumed to be extremely small and for purposes of modeling at 1pH for both the primary and secondary. This assumption is helped by the fact that the LTD is nearly coaxial in nature, with small gaps in between each stage. A physical test in the future will need to be conducted in order to properly characterize this parameter. The final transformer parameter to model is the Rm variable or core loss resistance. The lower this value, the more loss a core has. From the Stygar paper in the literature review, I know that $R_{cores}(t) = \frac{2S(\mu\mu_0\rho_{cores})^{\frac{1}{2}}}{\pi^{\frac{3}{2}}\ r_{cores}\ \delta\ t^{\frac{1}{2}}}$. [58] This formula only works for specific points. I assumed that the relative permeability of the transformer core is at its maximum which is 334,561. r_{cores} or the radius of the core is $0.0889m$. δ or the thickness of the Metglas tape is $2.3\ \times\ 10^{-5}m$ according to the Stygar paper using the same Metglas material. ρ_{cores} or the resistivity of the transformer core is $1.23\ \times\ 10^{-6}\Omega - m$. S or the total cross-sectional area of the core is again $0.000356m^2$. The time t will be taken at 100ns. Plugging in all these values together yields a Rm value of 142.32Ω resistance. Keep in mind that Rm is time dependent, meaning as relative permeability changes, the transformer shunt resistance will go from a lower value to the maximum value of 142.32Ω.

Moving along, the inductance and capacitance or L1 and C1 values per a stage length was determined. Since the LTD is assumed to be nearly the same as a coaxial transmission line, the coaxial transmission formulas were used. The inductance per unit length in a coaxial line is $L = \frac{\mu}{2\ \pi}\ \ln\ \frac{D}{d}$. The capacitance per unit length in a coaxial line is $C = \frac{2\ \pi\ \epsilon}{\ln\ \frac{b}{a}}$. The parameter b is the outer radius of the dielectric and the parameter a is the radius diameter of the dielectric. From the implementation chapter, the dielectric to be used is Kapton HN film. The thickness of the dielectric is $0.000127m$ for 5 mil. Since the dielectric strength is 3.9kV per mil, there needs to be at least three layers in order to get a safety of factor of two. [6] Also of concern is tracking distance along the wrapping. At 30kV, there needs to be at least three inches of wrapping before the copper is exposed in order to prevent arcing. Taking the circumference of the copper rod of 1.5 inch diameter yields 4.71 inches, which meets the criteria with just one wrap.

The outer radius of the dielectric film is $0.0192405m$ and the inner radius is $0.01905m$. The relative permittivity of Kapton at 5 mil is 3.5 and the relative permeability is assumed to be one due to being non-magnetic. [6] It is of note that Kapton is a type of polymide material, which helped in the search for its values. The length of the stage, in this case, the thickness of the stage with the air gap included is $0.84''$ or $0.0213m$. Putting all these values together in their respective formulas yields 42.4pH for L1 and 417pF for C1.

In the transmission line, it is important to know the AC resistance. The maximum frequency can be assumed to be related to the rise time of 10ns. The frequency in this case would be 100MHz. Note, that I want to optimize the LTD to pass through this frequency in order to reach its rise time. This means for the purpose of modeling, 100MHz is the only frequency I need to get a good estimate on circuit parameters. The diameter of the stalk is $1.5''$ or $0.0381m$. The unit length is still $0.0213m$. The material is pure copper. Plugging these values into an AC resistance calculator, the AC resistance of the stalk per unit length is $0.79m\ \Omega$. [5] For the AC resistance on the primary winding, I know that the circumference

of the winding is $0.5586m$, which would be the width of a theoretical rectangular metal bar. The distance the pulse travels through both sides around the transformer core is near $0.23622m$. The thickness the pulse travels through is between $0.42''$ and $0.06''$. The average would be $0.24''$ and in meters would be $0.006223m$. Plugging these values into an online calculator, the AC resistance of the primary winding is $0.545m\ \Omega$. [32]

For the primary inductance, imagine taking the circumference of the copper plate and like with finding the AC resistance, turning it into a rectangular bar. Then, chop the bar up into wires. It is then possible to treat its inductance like a straight wire parallel to the ground plane with one end grounded. All the wire inductances would be added in parallel. This would give me a close approximation. The PCB board already contains a ground plane and works nicely to this assumption. A visual aid of how this approximation works can be seen in Figure 6.1 below.

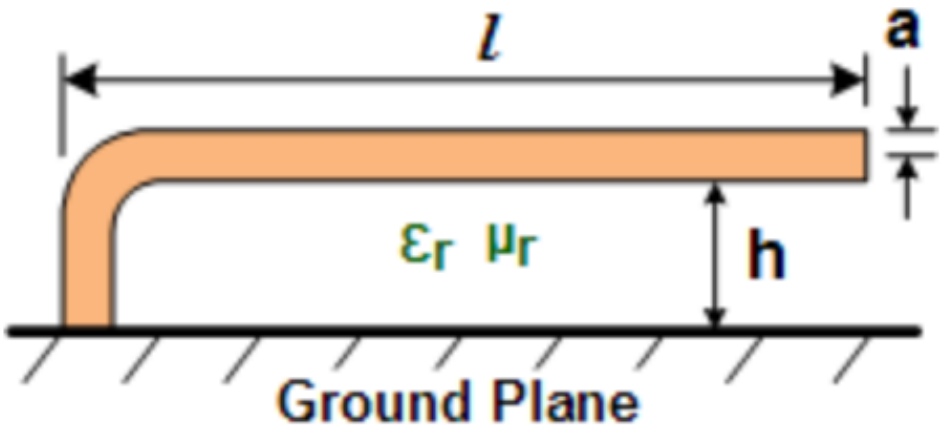


Figure 6.1: Visual aid showing where inductance parameters occur in straight wire over ground plane approximation. Image from K. Blattenberger. Image made in 2018. [20]

The wire diameter can be treated like how I solved for the AC resistance of the copper plate. The average diameter being $0.006223m$. The height of this wire above this plane needs to

account for how thick the Metglas core assembly is. This would be 0.49 inches or $0.012446m$. The height in the calculation goes from the center point of the wire to the top of the ground plane. This means the calculation height to plug into the calculator is $0.0155575m$. The length of this wire would be the radius of the copper disk which is 3.77 inches. This turns out to be $0.095758m$.

Finally, in order to complete the inductance calculation, the relative permeability must be considered between the wire and the ground plane. In this case that space is filled with the Metglas transformer core. I also employed a sanity check to the numbers. If the relative permeability is assumed to be one, then the inductance is 43.9nH. If the maximum relative permeability is 334,561 from the Metglas core, then the inductance is 14.7mH. [13] It is important to understand that the transformer core's relative permeability changes over time from one to the maximum value expected. If I was to use the 14.7mH in our simulation, then the output does not even reach 1A. From the papers referenced in the literature review chapter, the solid-state LTDs employing copper disks are able quickly rise to their full output in nanoseconds. Thus, for modeling purposes, it may be best to assume that the Metglas core does not apply in this primary inductance calculation. The core is already used when finding the magnetization inductance. Thus, I assumed that the relative permeability for my case is one. This is of course not perfect, but a rough assumption and requires future work to determine the effective relative permeability at high frequencies using the Metglas core.

From here, I paralleled out the inductance value found for one wire. The total number of wires that can be made from the rectangular block is 87.92 wires. Paralleling 43.9nH 87.92 times equates to 0.50nH. Please note, that I am hypothesizing that the permeability of the Metglas core does not have an effect on this specific inductance, and will need physical testing of a LTD stage to verify. It is possible that due to the permeability being a function of time, that the transformer cores do not have an effect at high frequencies, as seen from the other solid-state LTDs being able to achieve 10ns rise times.

For the simplified model, the parallel resistance is modeled as 50 Ω for the purposes of this simulation.

In Table 6.1 below, all simulation parameters are shown.

Parameter	**Value**	**Units**
Switch Rise Time	1	ns
Stage Capacitance	264	nF
Magnetizing Inductance	2.678	mH
Magnetizing Resistance	142.32	Ω
Primary Leakage Inductance	1	pF
Secondary Leakage Inductance	1	pF
L1 Inductance Per Stage Length	42.4	pH
C1 Capacitance Per Stage Length	417	pF
R1 AC Resistance Per Stage Length	0.790	$m\ \Omega$
Primary Resistance	0.545	$m\ \Omega$
Primary Inductance	0.50	nH

Table 6.1: Simulation model parameters from design LTD

To tune the outputs of the simulation results, a few key LTD parameters are calculated in a overall LTD rise time formula. In this case the equation will go like this, $T_R = 2 \times 23 \sqrt{(1 \times 10^{-12} + 42.4 \times 10^{-12})\ 417 \times 10^{-12}}$. This equates to a 6.188ns rise time based off of the transmission line. The total rise time would be 7.188ns assuming that the SiC MOSFET can achieve a 1ns rise time. If using the stated rise time given in the specification sheet for the SiC MOSFET of 4.8ns, then the total rise time would be 11.988ns. These values show that it is possible to get near a 10ns rise time with normal specifications. However, to guarantee under 10ns would require over driving the SiC MOSFET faster than its normal operation, which is feasible.

For one stage, I would use the formula $T_R = 2 \times 1\sqrt{(1 \times 10^{-12} + 42.4 \times 10^{-12})\ 417 \times 10^{-12}}$. This equates to a 0.2691ns rise time, or 1.2691ns rise time with the over driven SiC MOSFET switching speed. This is approximately a 2.14 Ω when tuning the simplified model to this rise time for one stage. This load resistor value will be used in both models.

Detailed LTD Model Simulation In Figure 6.2 below, a schematic used for the LTSpice simulation of the detailed model can be seen.

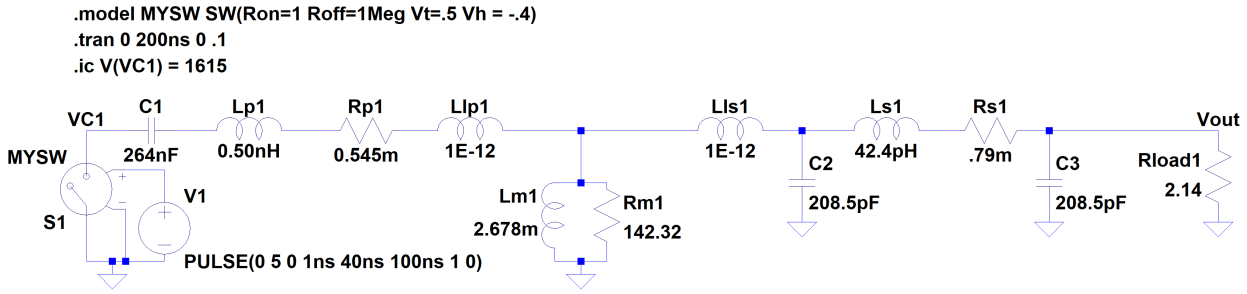


Figure 6.2: Detailed LTD model LTSpice schematic

Brookhaven Simplified LTD Model Simulation In Figure 6.3 below, a schematic used for the LTSpice simulation of the simplified model can be seen.

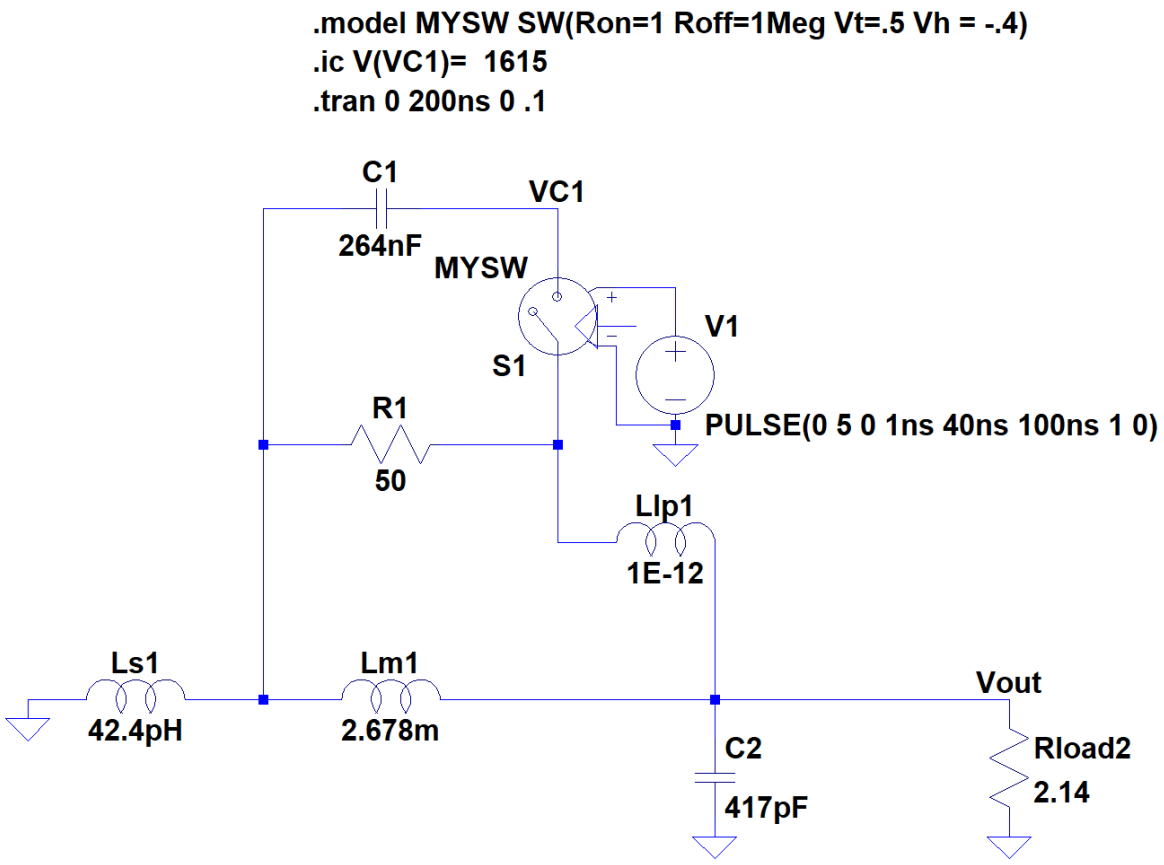


Figure 6.3: Simplified LTD model LTSpice schematic

6.1.2 Logistics and Costs

This section formulated a Bill of Materials (BOM) for all components needed to complete a single LTD, including diagnostic equipment. For the purpose of this thesis, it is assumed that standard power supplies are on hand, thus these will not be included in the BOM.

The lead times for parts that have this data available will also be accounted for in the BOM. If depending on a single supplier and distributor to keep the parts for the LTD going, how much time would I need to wait if stock runs out? The parts that could go out of stock

could be bought from a different distributor and manufacturer without needing to change values. Specialized parts such as the Metglas transformer cores do not have workarounds to avoid the lead time.

If the costs are over $100,000 for all components including DAQs, then the LTD may not be feasible for our specific application. It is of note that multiple LTDs can run off of one DAQ, which can lower the price per LTD. This single LTD pricing will be evaluated if the $100,000 threshold is reached to further evaluate feasibility.

The BOM for the LTD can be seen in both Table 6.2 and Table 6.3 below.

Table 6.2: BOM Part One

Part Type	**Manufacturing Number**	**Number Needed**	**Bulk Price Each**
Capacitor	C1210C222KGRACAUTO	2760	$ 0.40
Main MOSFET	C2M1000170J	690	$ 5.11
Intermediary MOSFET	DMN6140L-7	690	$ 0.11
MOSFET Driver	LM5134BMF/NOPB	713	$ 0.95
Fiber Optic Rx	AFBR-2310Z	23	$ 27.08
Fiber Optic Tx Laser	14BF-104	1	$ 2,740.00
Fiber Optic Splitter	FM-SM-124ABSD	1	$ 95.00
Metglas Cores		23	$ 395.00
Chromium Copper Disks		23	$ 109.00
Kapton Insulation Rod	5mil thick	1	$ 1.00
Copper Rod		1	$ 164.50
Transformer Screw	97715A103	368	$ 0.39
Bypass Capacitor	C0805C104J5RACTU	737	$ 0.04
Intermediary MOSFET Resistor	CRCW12103R90JNEA	690	$ 0.08
Fiber Optic Rx Resistor	ERJ-6DQJ8R2V	23	$ 0.20
Fiber Optic Rx Inductor	HK212515NJ-T	23	$ 0.19
Fiber Optic Rx Capacitor #1	C0805C102J5HACAUTO	23	$ 0.13
Fiber Optic Rx Capacitor #2	C0805C104J5RACTU	23	$ 0.13
PCB Board		23	$ 1,000.00
Ferrite Beads	HR2220V801R-10	2070	$ 0.90
Digital Delay Generator	DG645	1	$ 4,295.00
RG-58 Wire	C1166.21.01	2	$ 27.42

Sillicon Rubber Tubing	51135K25	2	$ 1.57
MHV Terminal HV	000-27000	1	$ 19.15
BNC Connector	31-221-RFX	4	$ 2.08
Crimp BNC Male Connector	5-1634500-3	9	$ 2.05
Aluminum Side Plates	25x13.5x.25	2	$ 40.05
Aluminum End Plates	14x14x.25	2	$ 25.84
Aluminum Top/Bottom Plates	25x14x.25	2	$ 40.05
Aluminum Stalk Support	13.5x6.75x.5	1	$ 16.79
Aluminum Clip Stands	5/8x7x.25	46	$ 1.58
End Plate Screws	92196A271	1	$ 10.34
Single Mode Fiber	F-SMF-28-C-3FCA	1	$ 74.00
Splice Wire Terminals	https://goo.gl/Cm1fnx	2	$ 10.39
4-Terminal Header	1803293	23	$ 1.56
4-Terminal Plug	1803594	23	$ 4.35
Red Hook-Up Wire 22AWG	1569-22-1-0500-004-1-TS	1	$ 10.71
Black Hook-Up Wire 22AWG	1569-22-1-0500-001-1-TS	1	$ 10.71
White Hook-Up Wire 22AWG	1569-22-1-0500-002-1-TS	1	$ 10.71
Yellow Hook-Up Wire 22AWG	1569-22-1-0500-003-1-TS	1	$ 10.71
HV Terminal Header	MDF51K-2P-12DSA(20)	23	$ 0.45
HV Terminal Plug	MDF51-2S-12C	23	$ 0.23
HV Power Supply	V6A3P30	1	$ 645.00
DAQ Unit	PXI-5124	1	$ 8,289.90
PXI Chassis	PXIe-1078	1	$ 2,406.60
Power to Board Pin	6643281-1	46	$ 7.52
Chassis Mount Resistor	HSA2568RJ	1	$ 3.06

Table 6.3: BOM Part Two

Part Type	**Total Cost**	**Supplier/Distributor**	**Lead Time If Unavailable (weeks)**
Capacitor	$ 1,099.14	Digikey	31
Main MOSFET	$ 3,525.90	Digikey	26
Intermediary MOSFET	$ 74.34	Digikey	20
MOSFET Driver	$ 678.58	Digikey	6
Fiber Optic Rx	$ 622.73	Digikey	8
Fiber Optic Tx Laser	$ 2,740.00	Seminex	10
Fiber Optic Splitter	$ 95.00	Fibermart	
Metglas Cores	$ 9,085.00	Metglas	12

Chromium Copper Disks	$ 2,507.00	Cadi Company	1
Kapton Insulation Rod	$ 250.00	American Durafilm Co.	0.43
Copper Rod	$ 164.50	Cadi Company	0.5
Transformer Screw	$ 142.20	McMaster-Carr	
Bypass Capacitor	$ 25.90	Digikey	22
Intermediary MOSFET Resistor	$ 53.82	Digikey	
Fiber Optic Rx Resistor	$ 4.55	Digikey	42
Fiber Optic Rx Inductor	$ 4.46	Digikey	7
Fiber Optic Rx Capacitor #1	$ 2.90	Digikey	21
Fiber Optic Rx Capacitor #2	$ 2.97	Digikey	22
PCB Board	$ 23,000.00	Advanced Circuits	
Ferrite Beads	$ 1,868.03	Digikey	8
Digital Delay Generator	$ 4,295.00	Stanford Research Systems	
RG-58 Wire	$ 54.84	Digikey	
Sillicon Rubber Tubing	$ 3.14	McMaster-Carr	
MHV Terminal HV	$ 19.15	Digikey	4
BNC Connector	$ 8.32	Digikey	10
Crimp BNC Male Connector	$ 18.45	Digikey	14
Aluminum Side Plates	$ 80.10	Midwest Steel and Aluminum	
Aluminum End Plates	$ 51.68	Midwest Steel and Aluminum	
Aluminum Top/Bottom Plates	$ 80.10	Midwest Steel and Aluminum	
Aluminum Stalk Support	$ 16.79	Midwest Steel and Aluminum	
Aluminum Clip Stands	$ 72.68	McMaster-Carr	
End Plate Screws	$ 10.34	McMaster-Carr	
Single Mode Fiber	$ 74.00	Newport	
Splice Wire Terminals	$ 20.78	Amazon	
4-Terminal Header	$ 35.97	Digikey	6
4-Terminal Plug	$ 99.98	Digikey	4
Red Hook-Up Wire 22AWG	$ 10.71	Digikey	
Black Hook-Up Wire 22AWG	$ 10.71	Digikey	
White Hook-Up Wire 22AWG	$ 10.71	Digikey	
Yellow Hook-Up Wire 22AWG	$ 10.71	Digikey	
HV Terminal Header	$ 10.35	Mouser	
HV Terminal Plug	$ 5.27	Mouser	
HV Power Supply	$ 645.00	Spellman	8
DAQ Unit	$ 8,289.90	National Instruments	
PXI Chassis	$ 2,406.60	National Instruments	
Power to Board Pin	$ 345.92		

Chassis Mount Resistor	$ 3.06	Digikey	

6.2 Results

This section shows the results of all the testing methods in the form of plots, tables, and analysis.

6.2.1 LTSpice Simulation Results

From the simulation results, the detailed simulation model created within this thesis correlates closely with the simplified model. Keep in mind I am only comparing one stage, not all 23 stages.

An overlayed view of both outputs can be seen in Figure 6.4 below.

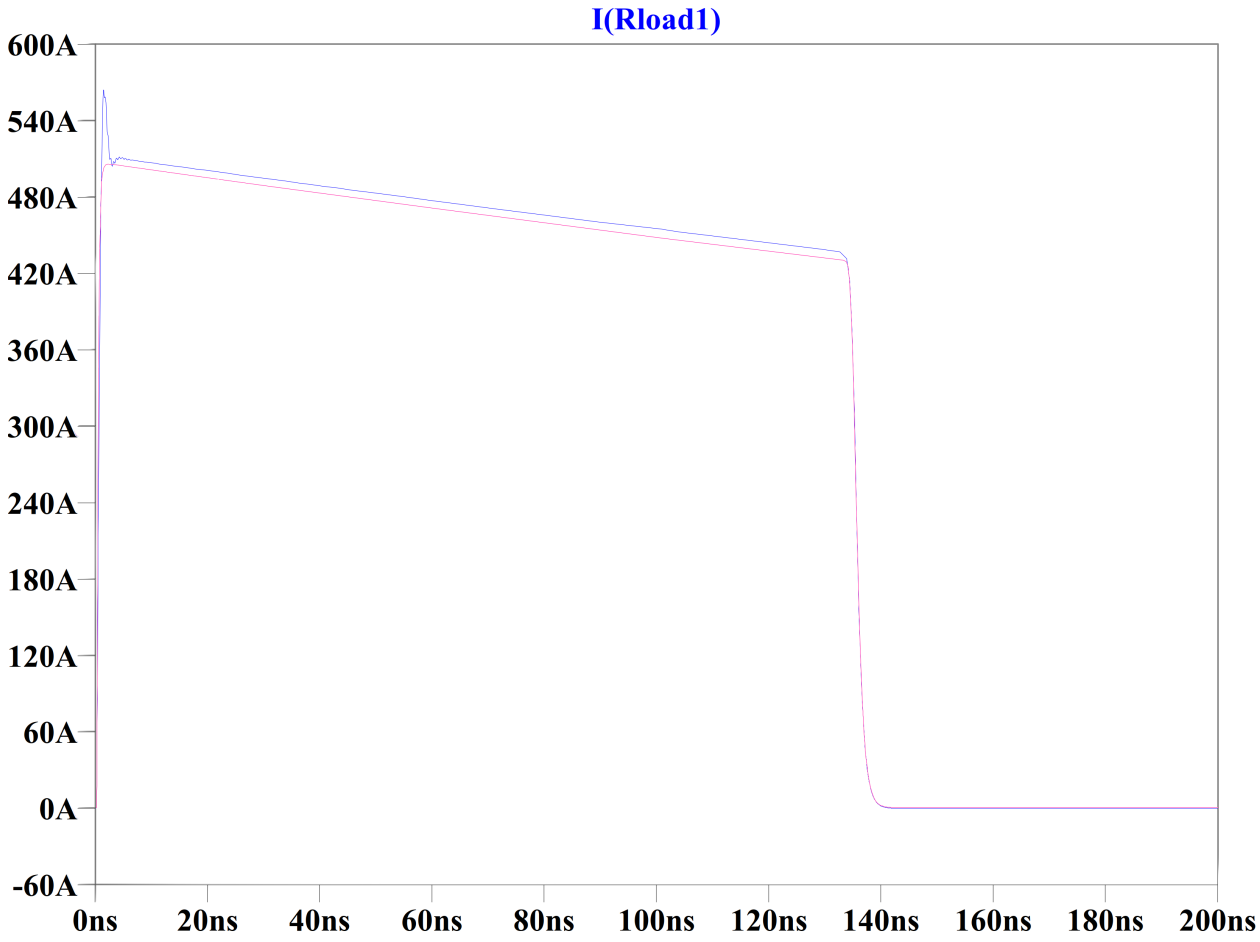


Figure 6.4: Detailed LTD model LTSpice output with both outputs overlayed

The blue line is the detailed simulation output and the red line is the simplified simulation output. It can be seen that the detailed simulation developed in this thesis closely correlates with the simplified model. From observation between the two models, I would select the detailed model that was designed in this thesis. The transient spike when the LTD turns on gives a better view of how the pulse is forming.

In terms of testing the performance when all 23 stages are stacked. From the previous section where I calculated the LTD rise time, my LTD design can achieve a 30kV and 500A pulse in under a 10ns rise time when over driving the SiC MOSFET.

Detailed LTD Model Simulation Output

In Figure 6.5 below, the output of the detailed LTSpice model can be seen.

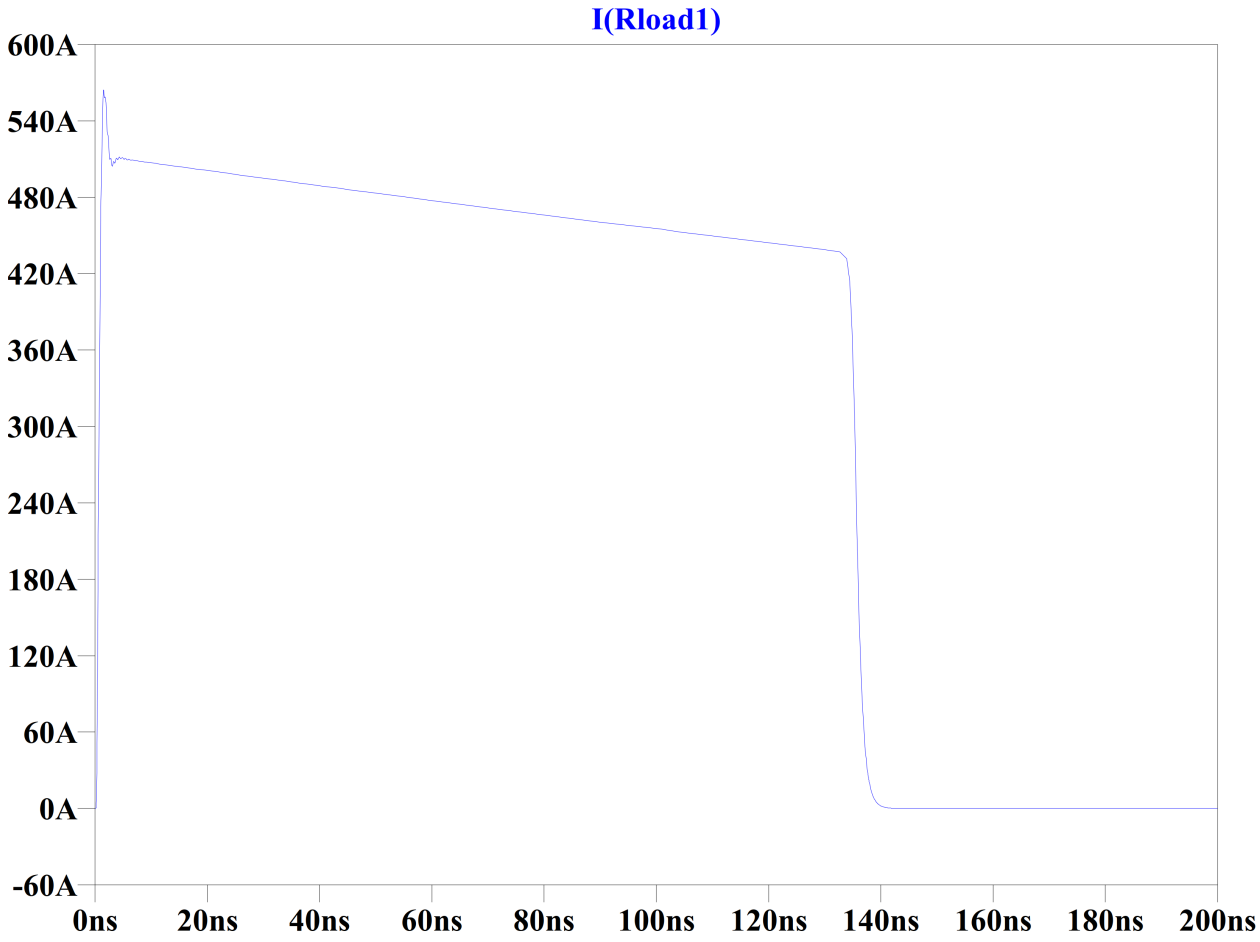


Figure 6.5: Detailed LTD model LTSpice output

From the figure above, it can be seen that the transient voltage is apparent when the LTD is switched on. This extra data from the detailed simulation may be useful when selecting a transient voltage suppressor.

Brookhaven Simplified LTD Model Simulation Output

In Figure 6.6 below, the output of the simplified LTSpice model can be seen.

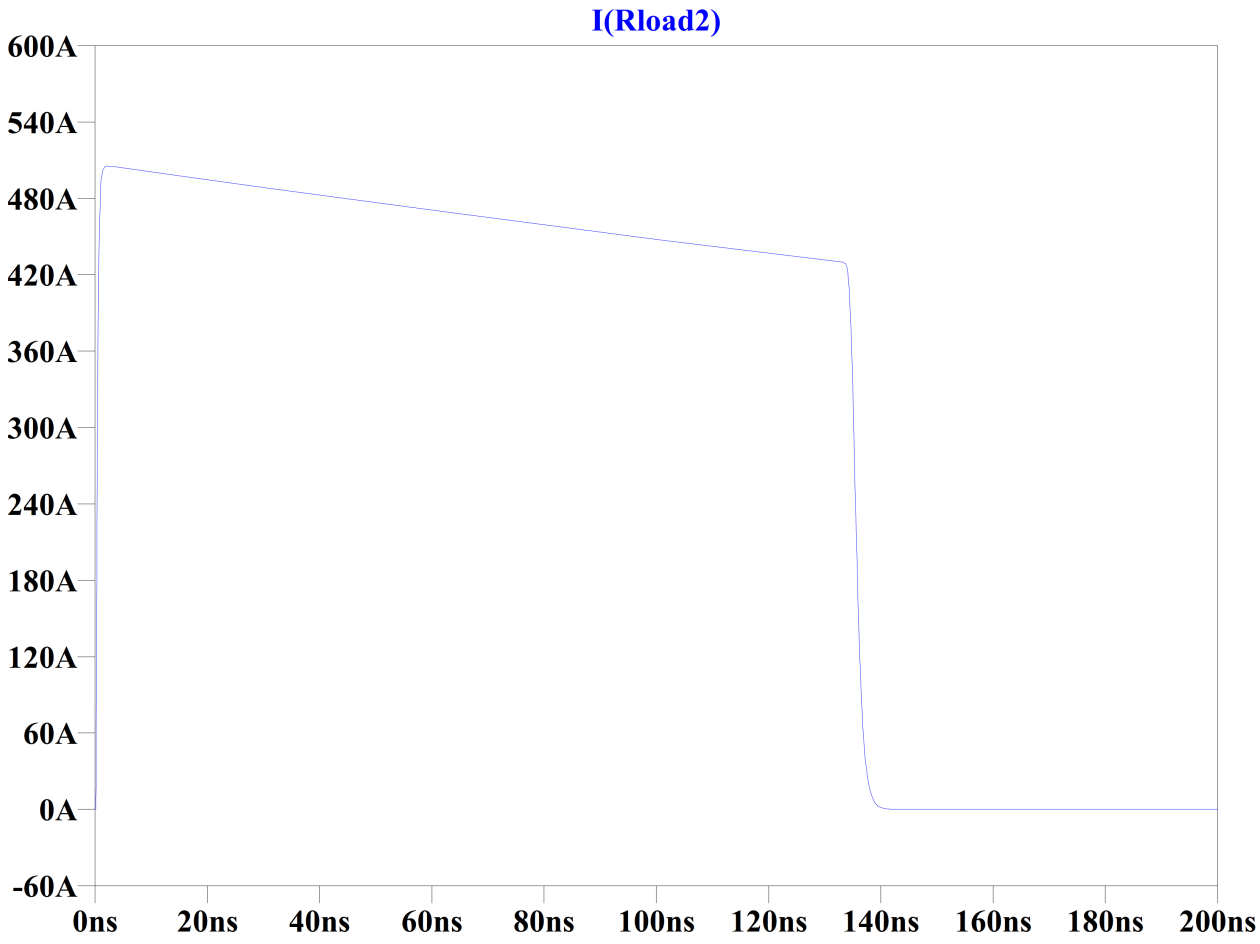


Figure 6.6: Simplified LTD model LTSpice output

From the figure above, it can be seen that the output from the simplified model is an ideal case. There are no other perturbations nor transients that can be seen. However, the simplicity of the model does make it useful when needing to do a quick test of a LTD design.

6.2.2 Evaluation of the Logistics and Costs of the LTD

Without buying any DAQ equipment, the LTD would cost a little above $\$51,940.77$ without machining costs added. If buying the DAQs as well, the total cost would be $\$62,637.27$. According to colleagues who are aware of switching equipment with similar specifications in

the field, this price is about the same range, erring on the cheaper side. However, despite costs, the jitter in this system will be much lower than conventional methods.

In terms of constructing the LTD, the longest lead time is with the construction of the Metglas transformer cores at 12 weeks. However, if any of the smaller components are not available, then it could be almost half a year to get the electronics. The good news however is whenever a manufacturer stops making a device, or a supplier stops selling a device, another one of the same specifications can be found. Metglas is the most specialized material in this BOM. Should Metglas go out of business, there would need to be a redesign of the LTD as the transformer core would have different properties. This is an unlikely case as Metglas is used for many high performance devices. All in all, our suppliers for the LTD are reliable and the lead times are reasonable for a graduate student to construct and test the system.

Comparing the MATLAB Cost Estimate

In my designed LTD, I have considered bulk pricing. The MATLAB feasibility study model used non-bulk pricing for the switches and logic systems. Bulk pricing would need to be considered for the capacitors, otherwise I would get an exorbitantly high price. There is a note about the accuracy of the surface plots, I used a logarithmic scale to keep computations down to a minimum to do a quick high-level design check. This means the exact pricing is going to be a little different from the ones appearing on the surface plots. From doing the model three modeling from the feasibility study section and using the table output, I get $6,918.76 at the 30kV and 500A target specification. Notice that from the surface plots the closest number to the target specification is 32,370V and 517.9A. This changes the pricing significantly enough to get $8,790.23 or a 21% deviation. Therefore, the surface plots should only be used as guidelines in design decisions when comparing technologies, but not the actual cost of the LTD.

To ensure that the table output was accurate, I entered in the voltage and current points that the surface plot gave out and inserted them back into the program. This yielded a value of $8,780.30. Practically the same value since there was some error due to significant figures from the points inserted back into the program. Thus, when comparing the accuracy of the programs output, I used the table output, not the surface plot output.

Using this knowledge, the cost of the SiC MOSFET and its intermediary MOSFET pair would be around $7.92. Total cost would be $5,464.80. The fiber optic receiver would cost $30.64 a device, or $704.72 for all 23 stages. Using the 2.2nF capacitors and having four per a brick would yield 2,760 capacitors. If I did not use bulk pricing, the cost would be $3,036. This would make the total cost to be around $9,205.52 which is way off of the $6,918 modeled in MATLAB, not to mention too much cost to be expected for small capacitors. If considering the bulk pricing, Digikey only shows quotes for up to 1,000 units at $0.40 each. At 2,760 units, it is possible lower the price per a capacitor. For now, let us use $0.40 per a capacitor. This would make the overall cost to $7,274. Not that far off from the modeled price of $6,918. Keep in mind the total cost would be lower since the quote does not go up to the number of capacitors I was using. The total error was about 5%.

Now, let us consider that I was to use a single capacitor per a brick, thus the capacitance would be around 8.8nF. The nearest capacitor that can do this would be the 1812GC822KAZ1A from AVX Corporation. It has a capacitance of 8.2nF. If using non-bulk pricing, the cost of the capacitors would be $759 versus bulk pricing would be $317.40. The total cost of the LTD stage would be $6,929 using non-bulk pricing versus $6,486.92 using bulk pricing. The percent error of using non-bulk pricing is 0.15% versus bulk pricing percent error would be 6.23%.

The MATLAB model can work as a good estimate. I can learn from this analysis that the capacitor pricing of the MATLAB model was considered at bulk pricing if paralleling capacitors. If using single capacitors, I should use non-bulk pricing if I wanted to get an accurate match. Of observation, the percent error for single capacitors is 0.15% above the intended value, versus paralleling capacitors makes it 5% over the intended value. This makes sense as paralleling capacitors means additional capacitors that increases the cost overall. This is useful to know when trying to get a better estimate from the MATLAB model. Add 5% from the cost if paralleling or add 0.15% using a single capacitor per brick respectively

Chapter 7

Conclusion and Future Work

For this thesis, I have provided the background to what a LTD is, a quick summary of available LTDs out in the academic world, and a thorough design and analysis of my LTD system. The LTD I have designed is at best expected to achieve a 7.2ns rise time and at worst a 12ns rise time with at least a 30kV and 500A output. This LTD is slightly larger than my original intentions of keeping the diameter within one foot. However, at 14 inches, this is still useful for the FRC application that the LTD is intended to be used for, while being serviceable. My LTD does exceed the standard in being under three feet in length. From the tip of the copper stalk to the back of the enclosure, it turns out to be 26.88 inches with ample space to route wiring and fiber. The jitter is expected to be under 1ns due to the use of single-mode fiber being powered by a laser diode. The limiting factor in achieving the <1ns jitter are the MOSFET drivers should they operate slower than intended. These need to be physically tested at their over-driven state to confirm for sure that they can allow for minimal jitter.

The PCB design for my LTD could not be created in this thesis due to limited design resources. It is best to hand over this work to a professional PCB technician. Especially to a technician familiar with high-frequency PCB design. However, the schematic diagram has

been made to run the LTD stages.

The one limiting factor in the accuracy of my calculations is the complex permeability of the Metglas transformer core at high-frequencies. There are some publications online that go over high-frequency transformers, but none directly related to the work I am doing, other than going over the fundamental transformer theories. The present solid-state LTD publications out there do not go into further detail regarding the transformer core design equations in terms of finding the primary winding inductance. This is certainly future work that will be in future publications from myself. Understanding how the complex permeability specifically affects the LTD transformer core will give researchers and engineers better tools in calculating the inductance within the transformer. I have also been going off of an assumption that power losses from the Metglas core will not be debilitating to the output pulse since other LTDs have been using Metglas cores. I have accounted for losses by designing my LTD with additional stages. Physical testing will also need to occur to determine how much power is being transferred over to the stalk.

7.1 Author's Contributions to the LTD Field

As far as this author is aware of, this thesis is the most comprehensive publicly available design document for other researchers and engineers to reference in the solid-state LTD field. It is intended that this thesis allows an electrical engineer with a good background in electronics and transformers to be able to design any LTD of their choosing when going along the process I took in my work.

Below is a list of contributions that I have provided to the solid-state LTD pulsed power field.

- A detailed thesis going step-by-step in the design process

- The creation of a novel modeling code in MATLAB to quickly make high-level design decision when making a LTD
- The formulation of a new detailed LTD model and verifying its feasibility
  - The formulation of an inductance approximation for the primary winding side of the transformer stage
  - Used the straight wire over ground plane with one end grounded inductance approximation
  - Took the toroidal core and straightened it into a rectangular slab
  - Divided the rectangular slab into numerous wires for the induction approximation
  - Assumed a low effective relative permeability in the medium between the copper and the PCB
  - Induction approximation showed transient voltage spike in simulation, which is more realistic than the basic LTD models available as TVS diodes are needed in each LTD design

7.2 Future Work

The following list below will highlight the additional research and work I believe is necessary to ensure my LTD is working as designed.

- Finish detailed design work for the LTD enclosure
  - Add in screws and threads
  - Add clamping mechanism to secure back end of stalk
- Finish selecting a low pass filter inductor for the reverse DC current that resets the transformer cores

- Carefully find a TVS diode that will clamp the output voltage of each LTD stage
  - The time it takes for the TVS diode to clamp is crucial in preventing damage to the SiC MOSFET
- Acquire all items in the LTD BOM for a single LTD stage and test
- Check and make any necessary changes to the detailed LTD model with the single stage test
- Make any design changes as needed should the single stage LTD not perform as expected
- Acquire remaining items for the full LTD system
- Conduct tests of the LTD and create simulation models according to the data
- Optimize MATLAB modeling code to quickly test new switches, different types of plots, and many switches at a time
- Fully gather and understand the high-frequency physics affecting the permeability in the transformer cores to better design LTD transformer cores

In addition, the high-frequency transformer work for the LTD is ongoing. While Metglas is an excellent transformer in terms of its saturation induction threshold, it is inherently going to have noticeable losses at high frequencies. This core may just work well enough for my application as it has done for other solid-state LTD applications. In transformers, core losses are due to eddy currents. A graphical example of eddy currents can be seen in Figure 7.1 below.

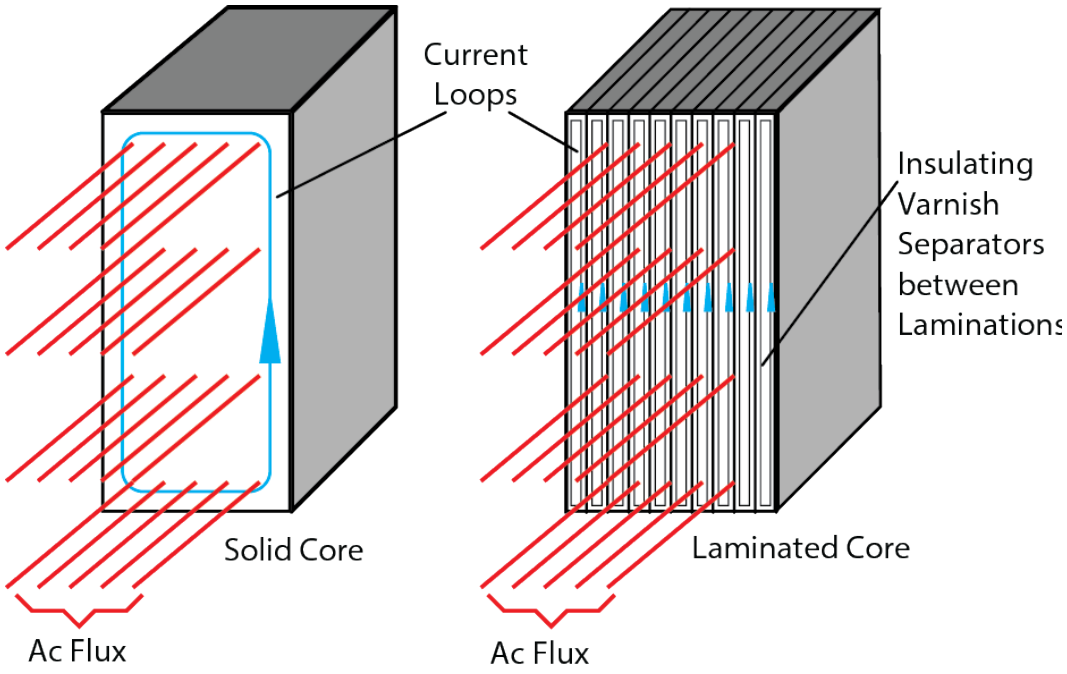


Figure 7.1: Graphic comparing non-laminated core to a laminated core and the effect of eddy currents. Image from J. Johnson. Image made in September 2014. [45]

It is common to see laminations in transformer cores to lower eddy currents as this results in smaller loops within a smaller cross-sectional area. There is a general equation to determine eddy current losses: $P_e = k_{ec} \times \frac{A_c}{\rho_c} \times (f\ B_m)^2$. Where k_{ec} is the waveform coefficient, A_c is the cross-sectional area, ρ_c is the electrical resistivity of the core, f is the frequency, and B_m is the amplitude of the magnetic flux density. [46] By confining the eddy currents to a smaller area, the power losses are smaller, hence the use of laminations reduce these losses. It is not enough to have smaller cross-sectional areas, but also a high electrical resistivity to lower eddy current losses.

There are other technologies to consider, however being expensive. These are nanocrystalline, powdered cores, and ferrofluids. These materials make it possible to make thinner laminations than possible with Metglas. However, the saturation induction is the tradeoff with these cores. Nanocrystalline cores can achieve thinner laminations than normal ferrites,

and can achieve high saturation magnetic flux densities of 1.2-1.5T. Of note however is that nanocrystalline cores have a lower electrical resistivity than amorphous alloys, thus have a lower workable frequency range. Powdered cores typically have a saturation magnetic flux density of 0.5-1.3T, but they have a much higher ρ_c than normal iron cores. [46] Ferrofluids are very new to the academic field. A company called FerroTec creates ferrofluids. They sell a product called EMG series dry magnetic nanoparticles that shows potential to be used in transformer cores. It is a dry particle base with a size of 10nm. According to their website, they exhibit no hysteresis, which is exciting as this means these particles exhibit no hysteresis losses. [33]

It would be useful to compare powdered cores, amorphous cores, and ferrofluids in a LTD solid-state transformer. Comparing their prices, ease of manufacturing, size, and power efficiency would be useful data to collect.

In addition, to model the complex permeability of these new cores such as the Metglas 2605CO is not trivial. An interesting find is the complex permittivity spectrum. As an application goes into very high frequencies, the conventional dipole movement in a transformer material changes. It eventually goes from spinning dipoles, to moving atoms, then at the highest of frequencies, only the electrons move. [23] I am hypothesizing that in terms of permeability, as frequencies go into the MHz to GHz range, that the dipoles begin to not respond as they normally would at lower frequencies. They may still spin a little, but the atomic spin starts to become more of an effect in terms of a material's magnetization. Complex permeability may help gather the effective permeability of a medium. However, better understanding of the dipole and atomic spinning within the transformer cores being examined would help further understanding on how the inductance and core losses are affected. Specifically, at high frequency transformer cores related to the LTD. My future research goal would be to model the dipole spin in detail of different high-frequency core materials, and use Finite Element Analysis to model the magnetic field.

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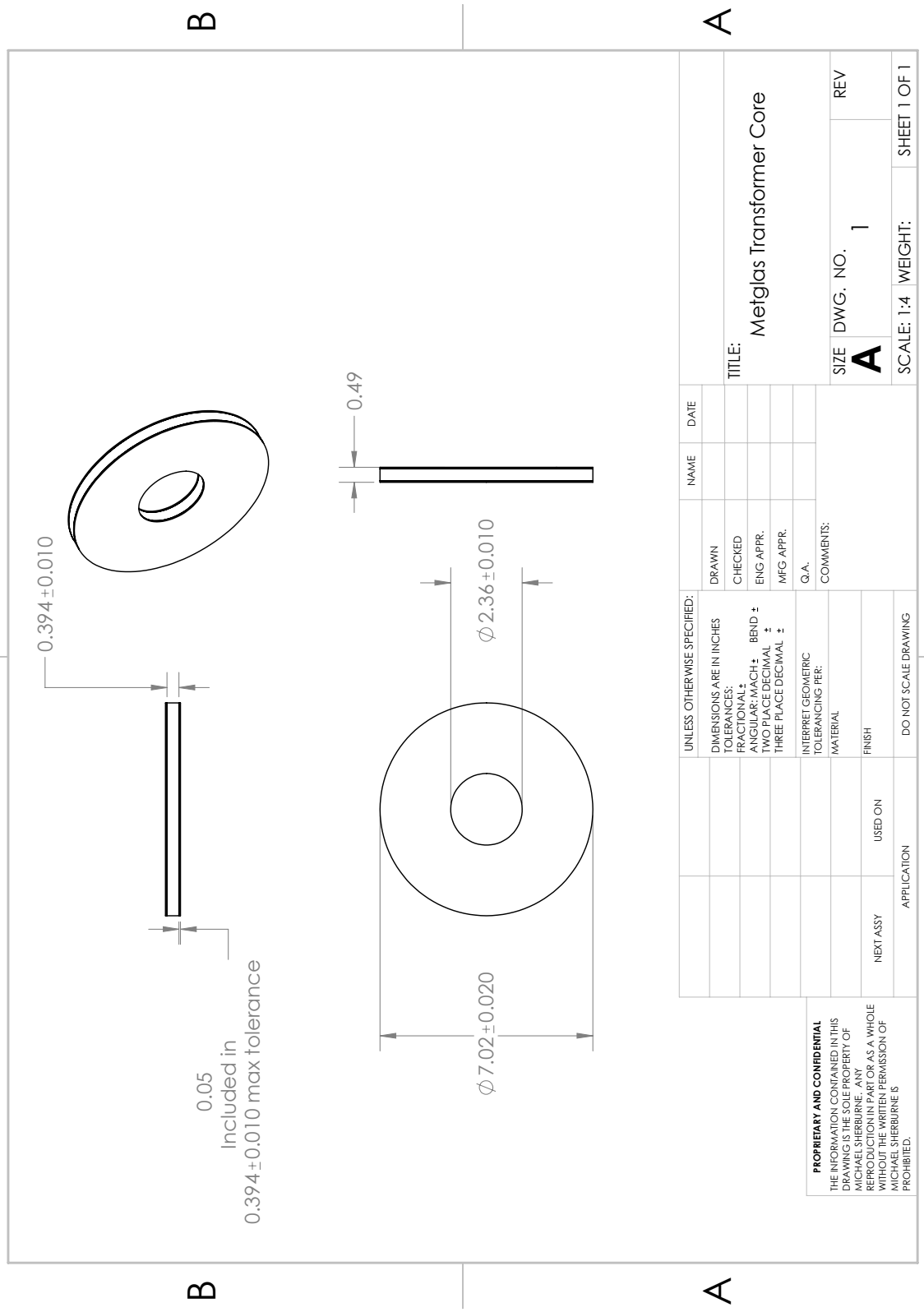
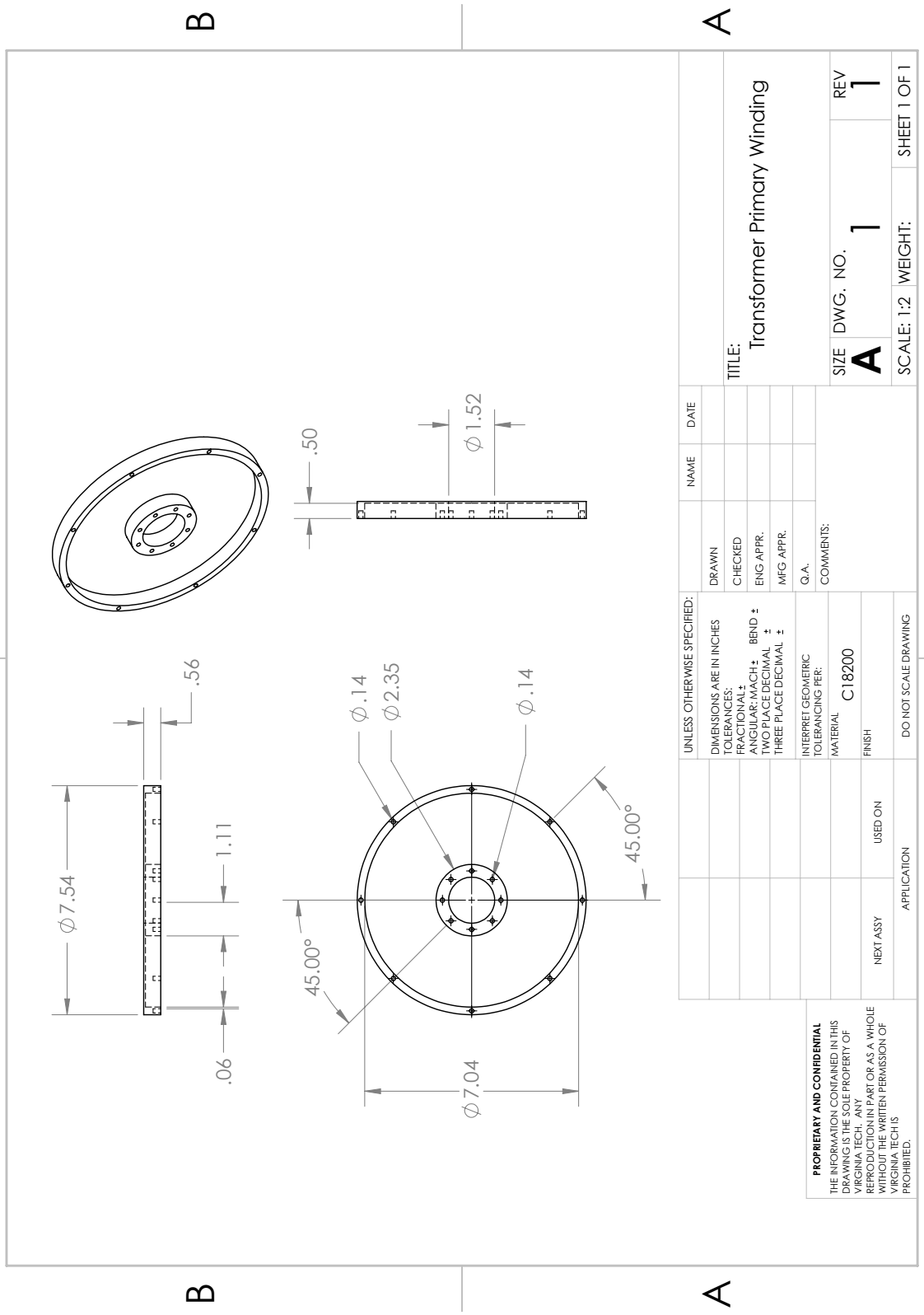
Appendices

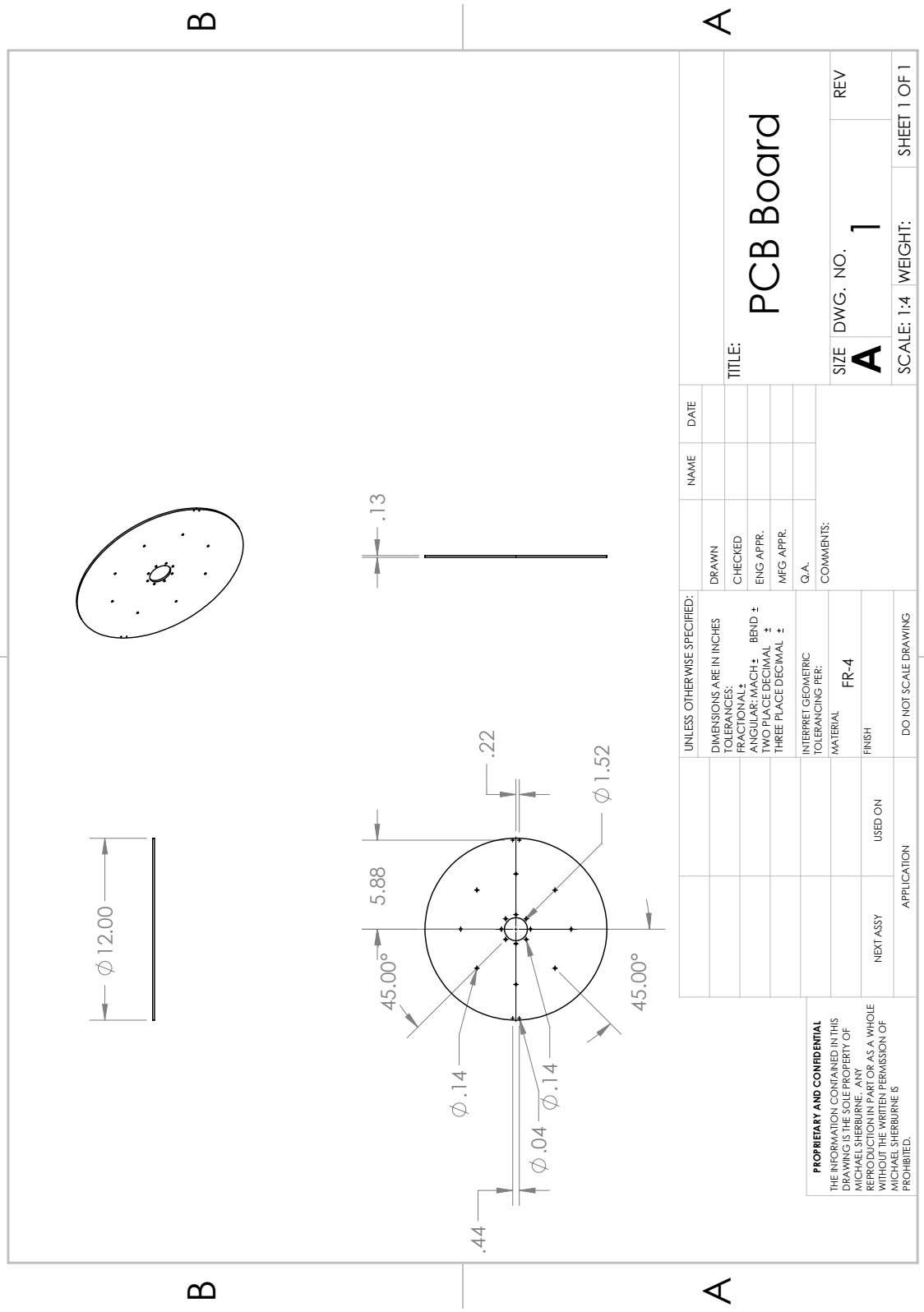
.1 Orthographic Drawing of Transformer Core



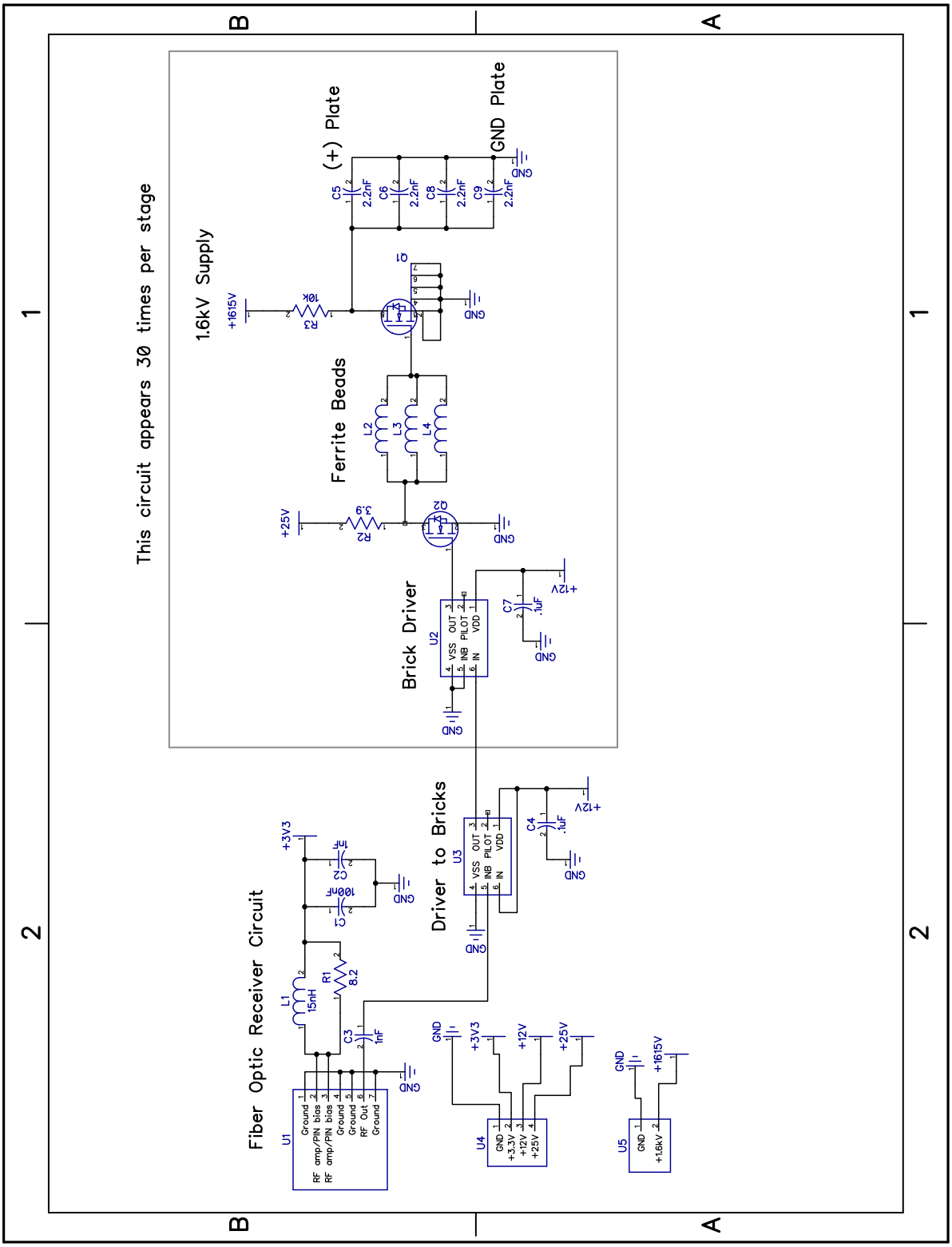
.2 Orthographic Drawing of Primary Winding Plate



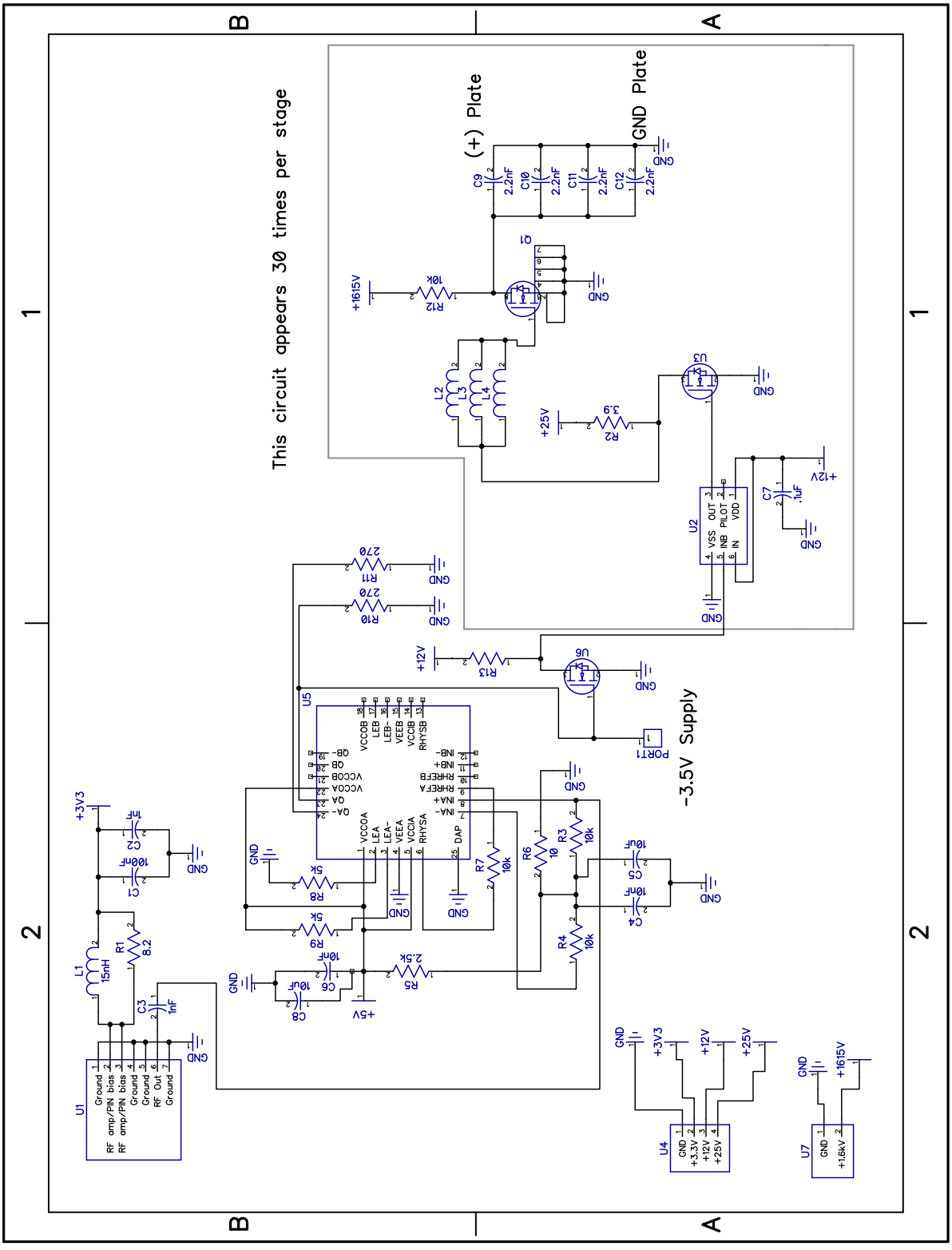
.3 Orthographic Drawing of PCB Stage



.4 Schematic Drawing of LTD Stage Circuit



.5 Schematic Drawing of LTD Stage Circuit With Low Fiber Power



.6 MATLAB Algorithm

The code developed for this modeling software is over 3,800 lines. The number of calculations required can easily eat up a powerful workstation's processing capabilities. Iterations of modeling prototypes were made to bring down the computation time from hours to minutes.

This section will be broken down into the following subsections: loading user parameters, user code settings, finding the number of switches in parallel, finding the number of stages, finding the capacitor to be used, testing the viability of the LTD model, packaging data between functions, creating a readable output for the user, and finally a flow chart to summarize the operation of the code.

.6.1 Loading User Parameters

The user has the ability in the main MATLAB function to set the requirements for the following: current, voltage, energy, rise time, and cost. When running the program, the code will take all the values and send them to the functions comparing different switching technologies and different capacitor technologies.

.6.2 User Code Settings

The modeling software is customizable friendly and allows the user to adjust the LTD's specifications, making the model more accurate, and making the model calculate faster but at the cost of less accuracy.

We now look at the following section of code below.

```
1 SIC_Core_Thickness = 0.021336; %Meters
2 SIC_RiseTime = 1E-9; %seconds
```

```
3
4  %Embedded Parameters (User can change this at any time)
5  %These parameters are to ensure a safety margin when calculating pricing
6  %Each stage in the LTD is increased by 10% of rated current for safety
7  %margin
8  Percent_Voltage_Rating = 95; %Percentage
9  Percent_Current_Rating = 95; %Percentage
10 Percent_Stage_Current_Rating = 110; %Percentage
11 Logic_Stage = 1; %every # stages, insert logic circuit
12
13 %Convert percentage values to actual decimal values
```

The user has the ability to set the maximum voltage and current the switch being used in the LTD will endure. It is good practice to derate switches as to prolong their life, and to not accidentally go over their limits. In this instance, the voltage setting is 95% of the max voltage the switch is rated at. The current setting is 95% of the max current the switch is rated at. It is also of note that the user can type in the full percentage, not as a decimal as the code will take care of that next. The stage current rating works the opposite as the switch current rating. It is also good practice to increase the current rating of a stage in case of a higher surge current or if needing a little extra current to operate a load. This will add additional switches in parallel from the target LTD output current. In this case, the stage is rated for 10% over the target LTD output current. The Logic Stage parameter is for adding in the cost of a logic unit every number of stages. For instance, if a driver unit that takes a main pulse logic signal from the user's control computer can reliably trigger a number of stages at once versus needing a logic unit for every stage, this program can do that. In this case, a logic unit is added every 12 stages and that cost is added to the total cost of the LTD.

The next set of parameters the user can change are for making the calculations run faster or slower, and either less accurately or more accurately respectively.

```
Percent_Current_Rating = Percent_Current_Rating/100;
Percent_Stage_Current_Rating = Percent_Stage_Current_Rating/100;

%Model Speed Tuning (Higher number = faster speed, but lower resolution)
%PCT means percent
PCTthres = 90;
ToleranceConstant = 0.01;
```

The first PCTthres constant that the user can change is for changing the threshold the program will use when stepping to its target number of switches in parallel and number of stages. This was designed in order to save computational power when figuring out the LTD costs at high currents and voltages. At low voltages and currents, the program can simply step by one till it reaches its goal without taking much time. However, say the voltage to be analyzed is 100MV, then stepping by one stage will take a while. Instead, for every step, the program will increase its step size by one until it reaches a certain threshold of the target value. That threshold is what PCTthres is. For the example code, the program will keep increasing its step size till it reaches 90% of the target voltage for example. Then after that, it will start to decrease its step size till it reaches its goal. We would like to call this the acceleration and deceleration algorithm. Without this algorithm, the computational time would take hours. It now only takes minutes.

Taking this a step further, it has been noticed that the cost of a LTD can go down by adding additional stages or more switches in parallel if the energy level is large enough. This is because adding more stages or switches in parallel will decreases the amount of energy each capacitor will have to store to achieve the target energy output. As will be noticed in later sections about the capacitor cost curves, decreasing the amount of energy stored in a capacitor will usually result in a cheaper capacitor.

After finding the number of stages, the program will begin adding more stages or switches in

parallel depending on how the user programed the code. The tolerance constant plays a role in calibrating the program to decrease the amount cost needs to change before confirming the LTD's cost has been optimized. The calibration is based off of the number of stages. For instance, if there are ten LTD stages, there is more computational room to add more stages or switches in parallel to get closer to a smaller cost. However, if the LTD has for instance a thousand stages, then the program may take hours before getting within .1% change between adding LTD stages or the number of switches in parallel. The tolerance constant will increase the percentage directly with the number of stages. This means with that thousand stage example, its percentage off the optimized value would be 10% to get a value in a reasonable amount of time. The program is constantly comparing the new value with the previous to get a percentage change of cost to compare with the tolerance value. The PCTthres2 also plays a role in this algorithm as it is another acceleration and deceleration algorithm to help expedite the process in zeroing down to the optimized LTD. If the target percent change is to be 5% in this case, then the program will increase its step size in either the number of stages or the number of switches to be added in parallel. Once it reaches the 5% threshold, then it will decrease its step size. Note, that this threshold is not the same as the tolerance value. The threshold is to help move the model along to get near enough to the tolerance value that will imply an optimized LTD.

0.6.3 Finding the Number of Switches in Parallel

In this subsection, and in the following subsections, the previously mentioned acceleration and deceleration algorithm is used. However, we will not bring this up again due to the previous subsection explaining its function in detail.

The program will first find the number of switches that need to be in parallel given the user's inputs. First, the maximum current must be found. The program will figure this out by dividing voltage from load impedance and comparing this to the current parameter the user

set in the input function. It is possible that a user wants a current output that is lower than the voltage divided by load impedance gives out in current. The code can correct for this automatically by choosing the higher current value. This is useful since the user does not need to do an additional calculation in figuring out the current output if they just want to base the current output from a known voltage output and load impedance.

The program at this section of code will consider the derating of the switch and begin to step the number of switches in parallel till it reaches the desired current for a single LTD stage. The acceleration and deceleration algorithm helps to speed up the computational process.

0.6.4 Finding the Number of Stages

This subsection is similar to the previous, except instead of finding how many switches in parallel are needed per a stage, it will now find the number of stages needed for the entire LTD.

The program uses the total current in the output of the LTD to figure out the number of stages. By stacking the LTD stages, each stage adds its respective voltage output. It is then possible to divide this voltage output by the known load impedance to get the current output. Thus, just like in the previous section in matching the current output for parallel switches, the code can do the same here for stages. As before, the acceleration and deceleration algorithm helps to speed up the processing.

0.6.5 Finding the Capacitor to be Used

This section of code has proven to be a little tricky to implement reliably. In the first round of code prototyping, the capacitance was stepped, but this caused a huge drain on computational resources. Instead, it was found that by simply rearranging the energy equation

for capacitors which is $E = \frac{1}{2} * C * V^2$, that the capacitance value needed can be instantly found. The following formula was used, $C = \frac{2\ E}{N_{switches}\ N_{stages}\ (V_{out}\ \%VR)^2}$. This formula adds three additional variables, one being %VR which is the percent of the total voltage rating the user wants to run the LTD stage at, the next being the inverse of the number of switches in parallel per a stage, and finally multiplying by the number of stages that the LTD has. This is to allow finding the capacitance needed per a switch.

From here, the program then finds the total energy contained in the single capacitor paired with its switch. This is simply using the previously mentioned energy equation for capacitors. The reasoning in finding the energy for the capacitor, is so that it can be used in the cost and weight curves found for each capacitor technology. The code will go ahead and get the cost data from all three capacitor technologies being used. Then choose the cheapest one. For the weight values, if the weight of a capacitor is under 0.006g, then it will default to 0.006 since that is the smallest capacitor package that can be used.

The code will now package all this data found in the previous subsections and get an initial cost of the LTD. It will now go into the optimization algorithm which has already been discussed in the User Code Settings subsection. After going through optimization, the LTD model is now prepared to be used in the next section of code, which is testing its viability in a LTD application.

0.6.6 Testing the Viability of the LTD Model

In order to provide the most useful model possible, the code will run a test concerning the rise time of the switch compared to the fall time of the capacitor being used. The code first uses the formula $Q = C * V_{switch}$ where Vswitch is the derated voltage for the application. The charge of the capacitor is found by calculation. Then it is possible to now find how long the charge depletes by using the derated current of a single switch. The following formula

is now used, $Q_{time} = \frac{\frac{Q}{I_{switch}}}{2}$. With the newly found time it takes to discharge half of the stored charge, this now can be compared with the rise time of the total LTD.

Now note, it is impossible to get an exact rise time of the LTD in a model without considering all the materials being used along the transmission of the pulse. To get a useful model, a similar solid-state LTD from LLNL and its model was used. This can be seen in the code below.

```
1
2  end
3  %************************************************************************
4  %Calculate Charge/Current of the Capacitor
5  Q = CAP*Single_IGBT_Voltage_Total;
6  Qtime = (Q/Single_IGBT_Current_Total)/2;
7
8  %Calculate Rise Time of LTD
9  %Calculate Rise Time of LTD
10 b = (IGBT_Size/(10^3) * IGBT_Number_Parallel)/(2*pi); %from circumference
11 %to radius
12 a = ((IGBT_Size/(10^3) * IGBT_Number_Parallel)/(2*pi))-...
```

This will now get a useful rise time of the entire LTD. If the rise time of the LTD is longer than the time it takes to deplete half of the charge in the capacitor, or is longer than the desired rise time the user set in the input of the code, then the program will fail the model as seen in the code below.

```
1      *InsulationSafetyFactor); %radius,
2  %stalk radius begins 5mm away from transformer radius
3  h = IGBT_Core_Thickness;
4  L1 = ((4*pi*10^(-7))*h*log(b/a))/(2*pi);
```

```
5 C1 = (2*pi*8.85E-12*h*INSULATIONer)/(log(b/a));
```

This failure will be noted as a one. If the rise time does work, then it will be noted as a zero. The program will use this data when creating surface plots of different parameter values. The goal is to show a failure by leaving that point on the plot black, and rest colored.

The LTD model is now officially ready to be packaged back to the main function and plotted to the user.

0.6.7 Packaging Data Between Functions

This section of code is simply packing the found data from the LTD model, and inserting it in the proper form back through the function.

0.6.8 Creating a Readable Output for the User

The user will receive three types of outputs in this version of the MATLAB modeling code. First, generating a table view of values. For our purposes we wanted to determine the LTD cost, its weight in grams, the circumference in mm, its depth in inches, the number of stages needed, and the capacitance of each individual capacitor used per a switch. Second, a surface plot that compares all switching technologies against two changing LTD parameter input values to gather total cost. Third and finally, another surface plot that compares all capacitor technologies against two changing LTD parameter values to total cost. These surface plots will make it easy for a user to determine which technology should be chosen for the application at hand. Voltage can be plotted with current, energy to current, voltage to energy, etc. for whatever the user needs. For our purposes, we wanted to plot voltage on the y-axis and current on the x-axis to see what our LTD output limits would be. Energy output in our case is not important, thus we did not need to also compare energy values to

another dependent variable.

Table View of LTD Switch Comparisons

An example output can be seen in Figure 3 below.

	Switch_Cost	Switch_Weight	Switch_Circumference	Switch_Depth	Switch_Stages	Switch_Capacitance
IGBT	4288	5721.7	96.78	11.5	23	2.0708e-06
Power MOSFET	22276	8739.9	258.08	15	30	1.0058e-06
Spark Gap	3511.5	44211	127	5	1	7.6734e-06
PPIGBT	17934	12856	100	30	10	5.4718e-06
SIC	9277.1	12047	397.02	11.5	23	3.6238e-07

Figure 2: Table view output from the MATLAB modeling code

Surface Plot View of LTD Switch Comparisons

An example output of one of the switch plots without its logarithmic scale can be seen in Figure 4 below.

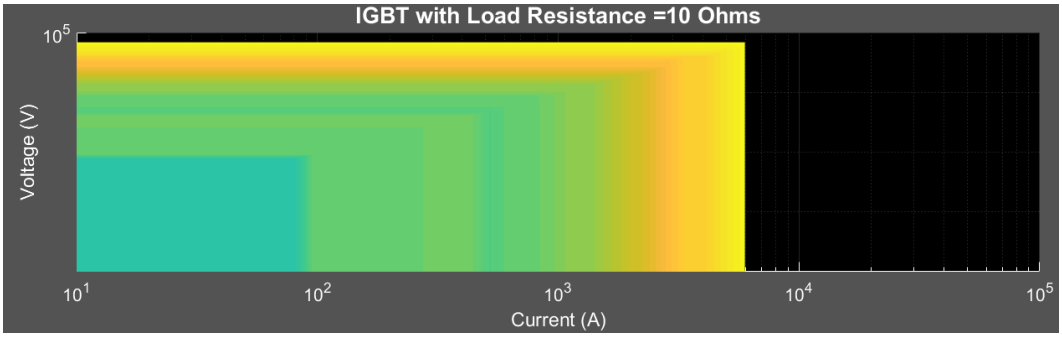


Figure 3: Switch surface plot output from the MATLAB modeling code

Surface Plot View of LTD Capacitor Technology Comparisons

An example output of one of the capacitor plots without its logarithmic scale can be seen in Figure 4 below.

Figure 4: Capacitor surface plot view output from the MATLAB modeling code

The only difference that the capacitor modeling code uses is a feasibility and cost effectiveness algorithm at the end of its sequence. For every point on the plot, the code models all switches being compared, then selects the cheapest one, but also the one that is feasible for that capacitor technology. We have noticed without the addition of the feasibility algorithm, the code only took the cheapest switching technology, which in turn caused many of our plots to return no values. By sorting first by feasibility, then selecting the cheapest switch, we are now getting useful plots.

0.7 Metglas 2605C0 Raw Data Table of BH Curve

Table 1: BH curve data table for Metglas 2605C0

H-Field(kA/m)	**B-Field(T)**
-5.4883E-06	6.9E-09
1.09765E-05	-1.38E-08
2.19531E-05	-2.76E-08
4.39062E-05	-5.52E-08

5.48827E-05	-0.000000069
7.68358E-05	-9.66E-08
9.87889E-05	-1.241E-07
0.000104277	-0.000000131
0.000131719	-1.655E-07
0.000148183	-1.862E-07
0.000164648	-2.069E-07
0.000186601	-2.345E-07
0.000197578	-2.483E-07
0.000219531	2.37456E-05
0.000554316	0.000503753
0.000828729	0.021474114
0.000911053	0.065000837
0.000949471	0.1059333
0.000976913	0.143454735
0.000987889	0.179030455
0.000993377	0.213621303
0.001004354	0.247659651
0.00101533	0.314198991
0.001020819	0.378744559
0.001031795	0.410212614
0.001037284	0.441128184
0.00104826	0.471347126
0.001059237	0.529671137
0.001070213	0.557776193
0.001075701	0.585256698
0.00108119	0.612208733

0.001092166	0.66474358
0.001097655	0.690134222
0.001103143	0.71480422
0.001119608	0.738969755
0.001114119	0.762414675
0.001130584	0.785547289
0.001136072	0.807959273
0.001147049	0.851077721
0.001158026	0.892058262
0.001163514	0.911611697
0.001179979	0.949469445
0.001185467	0.985165279
0.001190955	1.002484721
0.001196443	1.019059499
0.001201932	1.035418084
0.00120742	1.066597889
0.001218397	1.081515182
0.001212908	1.096096195
0.001218397	1.110629152
0.001212908	1.125114079
0.001223885	1.139478879
0.001229373	1.153531407
0.00124035	1.180483434
0.001245838	1.206090268
0.001251326	1.218341189
0.001256814	1.24169001
0.001251326	1.252884002

0.001262303	1.275320001
0.001267791	1.296651021
0.001273279	1.306812078
0.001278768	1.326293448
0.001284256	1.344381576
0.001289744	1.353005261
0.001295232	1.369507975
0.001289744	1.385266038
0.001295232	1.393217124
0.001300721	1.408494744
0.001295232	1.452622113
0.001311697	1.459972649
0.001317185	1.479189784
0.001311697	1.485483404
0.001306209	1.504244146
0.001311697	1.510729924
0.001322674	1.52317301
0.001317185	1.529178373
0.001322674	1.534919488
0.001328162	1.551494265
0.001322674	1.556442686
0.001317185	1.561703386
0.001328162	1.578638478
0.001322674	1.583658963
0.001328162	1.594060234
0.00133365	1.60402912
0.001339139	1.612772912

0.00133365	1.617216883
0.001339139	1.621348562
0.001344627	1.636986504
0.001339139	1.64085396
0.001344627	1.64467336
0.001339139	1.651975881
0.001344627	1.65577126
0.001339139	1.659470566
0.001344627	1.663049752
0.001339139	1.666676995
0.001344627	1.670304223
0.001350115	1.691707308
0.001344627	1.69499825
0.001350115	1.698409286
0.001344627	1.701676207
0.001350115	1.704847029
0.001355603	1.7078497
0.001350115	1.710684235
0.001355603	1.713614843
0.001361092	1.727018792
0.001355603	1.731799063
0.00136658	1.738909391
0.001361092	1.741071327
0.00136658	1.743161184
0.001361092	1.745275077
0.00136658	1.759615862
0.001361092	1.763579404

0.00136658	1.765573176
0.001361092	1.767590982
0.001372068	1.769392576
0.00136658	1.771146147
0.001372068	1.772803618
0.00136658	1.774557189
0.001372068	1.776238682
0.00136658	1.777728018
0.001372068	1.782844575
0.001361092	1.784478046
0.001372068	1.785991382
0.00136658	1.787384631
0.001372068	1.788946017
0.00136658	1.791828595
0.001383045	1.793486053
0.00139951	1.795407747
0.001415974	1.797593676
0.001426951	1.800043848
0.001421463	1.802878383
0.001426951	1.809027861
0.001421463	1.811886418
0.001426951	1.81488909
0.001421463	1.817747646
0.001432439	1.820389989
0.001426951	1.822768118
0.001432439	1.824906018
0.001426951	1.829398032

0.001432439	1.831559953
0.001437927	1.833433617
0.001443416	1.836772589
0.001437927	1.838382031
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