Resonant Cross-Commutated Dc-Dc Regulators
with Omni-Coupled Inductors

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Abstract

High-frequency noise at the switched node is a common issue in the hard-switched buck converters for point-of-load (POL) applications, such as telecommunications, network systems, FPGA, and ASIC. When the gallium-nitride (GaN) transistors are employed in those converters for higher efficiency and higher power density, the noise is more severe, due to a fast switching speed. Conventional quasi-square-wave (QSW) zero-voltage-switching (ZVS) buck converters have a clean switched node, but the switches and inductors must sustain very high current stresses. To overcome the high-stress limitation, a resonant cross-commutated (RCC) converter is put forward in this work. The basic premise is to inject the resonant current generated from one phase of two interleaved converters into the switched node of the other phase to turn on the active switch at zero voltage over a wide load range, and to turn off the synchronous switch at near-zero current at the rated load. The objective of this dissertation is to study the RCC topology, apply it in a two-phase buck converter, and achieve low noise, while maintaining efficiency, power density, and transient performance.

Closed-form analytical formulas of four switched states in a resonant cross-commutated buck (rccBuck) converter were derived to understand its operating principles. The complex fourth-order circuit was solved by decomposing it into two second-order circuit modes. The current to discharge the parasitic capacitor of the MOSFET was calculated by using a state-plane trajectory. The method of state-space representation was employed to calculate the inductor RMS current,
MOSFET turn-off current, and voltage stresses. The expectations were validated by three rccBuck converters switched at 2 MHz with 12 V input, 3.3 V at 20 A output, and peak efficiencies of 93.6%, 93.6%, and 93.3%. The discrepancy between the measured and modeled instantaneous state variables was less than 2%. When the rccBuck converter operates at discontinuous voltage mode (DVM), the active switch is turned off with near-zero current. The relevant ringing is also addressed.

The magnetic design for an rccBuck converter is challenging as a result of the significant ac and dc fluxes in resonant and output inductors. Commercial one-turn inductors with a full utilization of the winding window area are limited in this application due to the significant core loss and ac winding loss. The one-turn inductor with a certain space between the winding and gap was suggested in this work to reduce the ac resistance. The core loss densities and bias-related reliabilities of MHz magnetic materials were also surveyed. The core loss for an irregular voltage waveform was modeled by the equivalent elliptical loop (EEL) method. The ac winding loss was modeled by calculating the magnetic field strengths on the top surface of the winding. Four one-turn inductors were fabricated for a 12 V to 1.2 V rccBuck converter switched at 2 and 2.5 MHz. The designed one-turn inductors demonstrated a 2.1% higher efficiency at 20 A output, and 50% smaller total magnetic volume, than the commercial inductors with similar inductances, in the same rccBuck converter.

Four inductors in the rccBuck converter can be coupled into a single twisted E-E core to lower the part count, minimize the mismatch between the two phases, reduce dc flux density, and improve power density. The inductors L_{ra} and L_{ob} have in-phase voltages. The inductors L_{ra} and L_{rb} have interleaved voltages. Four windings with mixed in-phase and interleaved relationships then comprise Omni-coupled inductors (OCI). The steady-state current was modeled by the
decomposition of the common-mode (CM) voltage and differential-mode (DM) voltage. The PCB winding in the OCI simplifies the fabrication work and reduces the module height. The compact twisted E-E core achieves negative inter-couplings that are not available for conventional E-E cores. The self-inductances, coupling coefficients, and core loss were calculated from the reluctance network with errors less than 8%, 10%, and 11%, respectively. A 3.3 V GaN-based rccBuck converter with OCI was fabricated and achieved a 57% magnetic volume reduction and a 0.5% efficiency rise, compared to an rccBuck converter with discrete one-turn inductors.

The dynamic property of the rccBuck converter was studied by using the average-behavior model. The feedback design of an rccBuck converter is more difficult than that of a buck converter, due to an additional L-C tank and an additional right-half-plane zero. A modified type-III compensator that offers 100 kHz bandwidth and 56° phase margin was suggested. The load transient response of this rccBuck regulator is comparable to that of a buck regulator with the same output capacitance and closed-loop bandwidth. An input filter could be employed in a buck converter to mitigate the high-frequency noise, but was verified by simulation to have 60% lower bandwidth, three times larger $C_o$, and doubled settling time during a load transient, compared to the rccBuck converter with the same EMI spectrum.
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Ting Ge

General Audience Abstract

The switching noise in a hard-switched point-of-load (POL) converter may result in false turn on, electromagnetic interference issues, or even device breakdown. A resonant cross-commutated buck (rccBuck) converter operates with low noise since all MOSFETs are turned on with zero voltage within a wide load range. A state-space model was developed to calculate the voltage gain, voltage stresses, and current stresses. Design guidelines for the rccBuck converter operating at continuous voltage mode or discontinuous voltage mode are provided. The design methodology of a one-turn inductor with significant ac and dc fluxes is given. Four fabricated one-turn inductors achieved 2.1% higher efficiency and 50% smaller total magnetic volume than the commercial inductors in the same rccBuck converter. The Omni-coupled inductors (OCI), composed of a twisted E-E core and PCB windings, further improve power density and efficiency. The core loss and inductances were modeled from a complex reluctance network. According to the loss-volume Pareto fronts, the total inductor loss was minimized within a smaller volume than that of discrete inductors. The expectations were validated by an OCI-based rccBuck converter switched at 2 MHz with 12 V input, 3.3 V at 20 A output, and peak efficiency of 96.2%. The small-signal model with a good accuracy up to half switching frequency was developed based on the averaged equivalent circuit. The transient performance of an rccBuck regulator is comparable to that of a second-order buck regulator with the same switching frequency, output capacitance, and closed-loop bandwidth.
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Chapter 1 Introduction

Nomenclature

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<th>Symbol</th>
<th>Description</th>
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<td>( C_{oss} )</td>
<td>Output capacitance of MOSFET</td>
</tr>
<tr>
<td>( D, d, ) and ( \hat{d} )</td>
<td>Dc, instantaneous, and small-signal duty ratio</td>
</tr>
<tr>
<td>( f_s )</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>( G_{vd} )</td>
<td>Control-to-output transfer function</td>
</tr>
<tr>
<td>( i_d )</td>
<td>Channel current of MOSFET</td>
</tr>
<tr>
<td>( L_{loop} )</td>
<td>Parasitic inductance in a power switching loop</td>
</tr>
<tr>
<td>( R_{gate} )</td>
<td>Gate resistance</td>
</tr>
<tr>
<td>( v_{ds} )</td>
<td>Drain-to-source voltage of MOSFET</td>
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The applications, topologies, footprint, and efficiencies of point-of-load (POL) power modules are surveyed in this chapter. Most commercial POL converters are hard-switched and have a turn-on noise related to high-di/dt. Even with the state-of-the-art PCB layout, the high di/dt still exists and causes a 40% voltage overshoot. Conventional zero-voltage-switching (ZVS) buck converters have zero di/dt, but their high current stress and high core loss outweigh their benefits of low noise and low switching loss. The resonant cross-commutated (RCC) converter is a promising topology that achieves ZVS with acceptable current stresses. Coupled inductors could be applied in RCC converters to shrink the volume; therefore, general coupled inductors are surveyed and classified according to their energy-transfer component, energy-storage type, and phase relationship. The concept of Omni-coupled inductors (OCI) is then presented. Improving the dynamic response is another objective for POL converters. The small-signal modeling methods for a dc-dc converter are introduced by using the example of a buck converter. Their availabilities
for modeling the RCC converters are discussed. The contributions and outline of this dissertation are given at the end of this chapter. The related simulation files are given in Appendix F.

1.1 Survey of Point-of-Load Power Modules

Point-of-Load (POL) converters solve the challenges of high current demands and low noise margins, required by high-performance semiconductors such as microcontrollers or ASICs, by placing individual power supply regulators close to their point of use [1]. The applications of POL converters include CPU core, memory, telecommunications, networking systems, FPGA, DSP, automotive infotainment, etc. The specifications of their $V_{in}$, $V_o$, and $I_o$ are summarized in Table 1-1. The challenges of the conventional CPU voltage regulator (VR) are low output voltage ($< 2$ V) and high output current ($> 20$ A per phase). The POL converters for telecom/network/FPGA/ASIC applications have a medium step-down ratio and medium output current, compared with other POL applications. Power MOSFETs, gate drivers, controllers, and passive components are usually integrated into a power module to lower the part count, improve reliability, and reduce cost. The next-generation CPU VR needs to step down from a typical 48 V $V_{in}$ to a $V_o$ lower than 2.5 V with $I_o > 30$ A for each phase. Achieving such a high step-down ratio while maintaining high efficiency and high power-density, is challenging. Several single-stage, two-stage, and input-series-output-parallel topologies were developed in recent years to deal with the high step-down ratio [2]–[6]. The applications of automotive infotainment and advanced driver-assistance systems (ADAS) require converters to have wide $V_{in}$ and wide $V_o$. Meanwhile, their electromagnetic interference (EMI) should satisfy the strict CISPR-25 standard [7]. Because of this requirement, a high switching frequency ($\geq 2$ MHz) for avoiding the interaction with the radio frequency, as well as soft switching for low noise, are preferred.
Table 1-1. Specifications of existing POL converters

<table>
<thead>
<tr>
<th>Applications</th>
<th>$V_{in}$ (V)</th>
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<tr>
<td>Conventional CPU VR</td>
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</tr>
<tr>
<td>Next-Generation CPU VR</td>
<td>40 – 54</td>
<td>0.5 – 2.5</td>
<td>30 – 120</td>
<td>[2]–[6]</td>
</tr>
<tr>
<td>Automotive Infotainment and ADAS</td>
<td>3.6 – 40</td>
<td>1.1 – 20</td>
<td>2 – 5</td>
<td>[17]–[18]</td>
</tr>
</tbody>
</table>

This dissertation is focused on a general-purpose POL converter with a typical 12 V input and 1.2 – 3.3 V output. The output current is 20 A, and the switching frequency is around 2 MHz. The research goal is to realize low noise by zero-voltage switching, and to maintain high efficiency, small size, and fast transient response. The POL converters with a high step-down ratio and wide $V_{in}$ range for the next-generation CPU VR and automotive applications, are not considered in this work.

![Diagram](image-url)

Fig. 1-1. (a) Two-phase buck converter and (b) series-capacitor buck converter with extended duty ratio and 50% voltage stress reduction for $M_{1a}$ and $M_{2a/b}$.

The multi-phase interleaved buck converter is commonly used for POL applications due to its high current capability, low output current ripple, and high efficiency [19]–[21]. In order to reduce the voltage stress, increase the efficiency, and improve the dynamic response, the two-phase buck converter in Fig. 1-1(a) is modified to a series-capacitor buck (SCBuck) converter in Fig. 1-1(b).
The voltage across $C_s$ is half of the input voltage. Switched node voltages $v_{swa}$ and $v_{swb}$ are also reduced to half $V_{in}$. According to $\bar{v}_{swa} = \bar{v}_{swb} = V_0$, the duty ratio $D$ is doubled to maintain the same $V_o$, namely, $V_o/V_{in} = D/2$.

The SCBuck converter has many advantages. The voltage stresses of $M_{1a, 2a, 2b}$ are reduced to half $V_{in}$. The MOSFETs, having a better figure of merit (FOM), could be used to improve the efficiency. The volt-second of the output inductor is reduced; thus, the inductor size is smaller. The output capacitance is reduced due to the extended duty ratio and a better current-ripple cancelling effect. The dc current of $L_{oa}$ and $L_{ob}$ is balanced automatically due to the charge balance of $C_s$.

However, the disadvantages of the SCBuck converter should be noted. The $M_{2a}$ has a high current stress since it conducts $(i_{Loa} + i_{Lob})$ when $M_{1b}$ is on and $M_{1a}$ is off. The phase shedding method for improving the light-load efficiency is not feasible, as a result of asymmetric phases. The maximum voltage gain is limited by 0.25. As a result, the SCBuck converter is not available for POL applications with 3.3 V output.

The output current, inductor type, total volume, and maximum efficiency of the state-of-the-art power modules switched at 2 MHz and 1.2 V output, are summarized in Table 1-2. The buck converter in [26] using a monolithic half-bridge GaN module, has the highest efficiency. The SCBuck converter in [23] using a Si MOSFET has the minimum size and maximum power density. If the GaN FET and integrated magnetic structure, e.g., PCB inductor or LTCC substrate, were applied in the SCBuck converter, the efficiency and power density could be further improved. Notice that all the power modules in Table 1-2 are hard switched and thus may have the high-frequency noise discussed in Section 1.2.
Table 1-2. Surveyed switches, rated current, inductors, volumes, and efficiencies of the hard-switched converters with state-of-the-art efficiencies at \( V_{in} = 12 \) V, \( V_o = 1.2 \) V, and \( f_s = 2 \) MHz, for conventional CPU applications in Table 1-1.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Topology</th>
<th>Switches</th>
<th>Phase #</th>
<th>Rated ( I_o ) (A)</th>
<th>Inductor Package</th>
<th>Volume ( (\text{mm}^3) )</th>
<th>Maximum Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>[24]</td>
<td>Buck</td>
<td>Si (CSD97370)</td>
<td>1</td>
<td>20</td>
<td>PCB inductor</td>
<td>12×20×4</td>
<td>85.1%</td>
</tr>
<tr>
<td>[25]</td>
<td>Buck</td>
<td>GaN (IR)</td>
<td>1</td>
<td>20</td>
<td>LTCC substrate</td>
<td>15×21×3</td>
<td>86.0%</td>
</tr>
<tr>
<td>[26]</td>
<td>Buck</td>
<td>GaN (EPC2100)</td>
<td>1</td>
<td>20</td>
<td>Discrete L</td>
<td>18×23×6</td>
<td>87.6%</td>
</tr>
<tr>
<td>[22]</td>
<td>SCBuck</td>
<td>Si (CSD16411Q3)</td>
<td>2</td>
<td>10</td>
<td>Discrete L</td>
<td>13×30×4</td>
<td>86.1%</td>
</tr>
<tr>
<td>[23]</td>
<td>SCBuck</td>
<td>Si (TPS54A20)</td>
<td>2</td>
<td>10</td>
<td>Discrete L</td>
<td>10×16×2</td>
<td>87.1%</td>
</tr>
</tbody>
</table>

The SCBuck converter is not available for 3.3 V POL applications, and most of the commercial products with that \( V_o \), employ the buck converter. The switching frequency is usually below 1 MHz, as shown in Fig. 1-2. The Murata product has the highest nominal-load efficiency, 92.5% at 20 A, due to a low switching frequency and large core size. The MPS converter has the highest light-load efficiency since it operates at a pulse-skipping mode with a reduced switching frequency at light load.

![Efficiency graph](image)

Fig. 1-2. Surveyed efficiencies of the commercial power modules in [13]–[16] at \( V_{in} = 12 \) V and \( V_o = 3.3 \) V.
One objective of this work is to realize ZVS and low noise for POL converters. The efficiency and size are expected to be maintained by using the low-stress ZVS topology, GaN FETs, low-loss magnetic material, and coupled inductors. A higher switching frequency, e.g., 2 MHz, could reduce the inductor size and improve the transient response.

1.2 High-Frequency Noise in Hard-Switched POL Converters

Conventional hard-switched POL converters have the high-frequency switching noise, which is related to the turn on speed and switching loop layout. This section analyzes the high di/dt problem of GaN and Si FETs, and then surveys a state-of-the-art layout for minimizing the power loop inductance.

The schematic of a buck converter with an ideal layout is shown in Fig. 1-3(a). The input capacitor is assumed with zero equivalent series inductance (ESL), and the total switching loop inductance is zero. The switching waveforms were simulated by using the LTspice models of commercial half-bridge modules.

![Fig. 1-3. (a) Buck converter with ideal layout/package and zero switching-loop inductance. (b) Realistic buck converter with parasitic switching-loop inductance.](image)

Both GaN and Si switches have high di/dt at the turn-on transition period according to the simulated drain current waveforms in Fig. 1-4. This high di/dt in the GaN-based converter is
caused by the high $dv/dt$ on the $C_{oss}$ of the synchronous switch [27]. The high $di/dt$ in the Si-based converter is caused by the reverse recovery effect of the synchronous switch [28].

![Simulated gate voltages and drain current of M1 in Fig. 1-3(a) for (a) EPC2100 [29] and (b) CSD86360Q5D [30] with $R_{gate} = 2 \, \Omega$ and $L_o = 150 \, nH$. Current spike is more severe for GaN FET.](image)

The turn-on peak current is higher than the turn-off current in Fig. 1-4; thus, the turn-on noise is more severe than the turn-off noise. If the turn-off $di/dt$ exceeds the turn-on $di/dt$ when the output current or inductor current ripple is very high, the turn-off ringing is more severe.

The switching speed could be slowed by a larger gate resistance ($R_{gate}$). This method reduces the current spike but induces higher switching loss [31]. The switching energy and turn-on current spike were simulated by sweeping the $R_{gate}$ from 0.5 $\Omega$ to 2.5 $\Omega$. The active switch and synchronous switch had the same $R_{gate}$ in the simulation. The dead time was tuned manually to achieve the minimum switching loss. Both turn-on energy $E_{on}$ and turn-off energy $E_{off}$ of the active switch increase with $R_{gate}$ as shown in Fig. 1-5(a). The Si MOSFET has higher $E_{on}$ and $E_{off}$ because of the higher output capacitance ($C_{oss}$) and slower switching speed. The GaN FET with a negligible turn-off loss is more suitable for the ZVS operation since the ZVS converter usually has high turn-off current.
Fig. 1-5. Simulated (a) turn-on energy, turn-off energy, and (b) peak turn-on current of active switches in Fig. 1-3 versus gate resistance at $V_{in} = 12$ V, $I_o = 20$ A, $V_o = 1.2$ V, $f_s = 2$ MHz, and $L_o = 150$ nH. GaN switch has a smaller switching energy but higher current spike. $R_{gate}$ reduces current spike but increases loss.

The $R_{gate}$ can reduce the current spike effectively, as demonstrated in Fig. 1-5(b). However, higher $R_{gate}$ causes higher switching loss, especially the turn-off loss of Si MOSFET, as shown in Fig. 1-5(a). The higher peak current of the GaN FET is a result from the faster switching speed. The high $di/dt$ and the parasitic inductances in Fig. 1-3(b) may induce severe voltage overshoot at the switched node, false turn on, electromagnetic interference noise, or even device breakdown [32]–[35]. In order to avoid those issues, the parasitic inductances should be minimized. There are three critical kinds of parasitic inductances that have a significant impact on the switching performance of a converter: the common source inductance $L_{cs}$, the power loop inductance $L_{loop}$, and the driver loop inductance $L_g$. Both the MOSFET package and PCB layout will contribute to the parasitic inductances. The GaN manufactures have used advanced packages such as the GaNPX, PQFN, and land grid array (LGA) to reduce the parasitic inductances to a very low level [36]–[38]. The gate driver is very close to the GaN FET to minimize the driving-loop inductance [43]. The state-of-the-art package for the Si MOSFET uses the DrMOS structure, in which the high-side and low-side MOSFETs, as well as the drivers, are co-packaged as one chip [39]–[41]. The driving-loop inductance is then minimized. The stacked die package introduced in [41], allows
the high-side and low-side MOSFET dice to be stacked directly, instead of being connected by wire bonding, further reducing the parasitic inductances. Since the package inductance and diving-loop inductance have been minimized, this section only focuses on the power stage layout to minimize the power loop inductance.

Some guidelines of the power loop PCB layout for the POL converters are given in [42]–[45]. The state-of-the-art Si-based power module has a lateral switching-loop layout, as shown in Fig. 1-6(a) and (d). The MOSFET and $C_{in}$ are on the top layer, and an extra shielding layer is placed on the second layer, to cancel the flux generated by the power loop. The power loop inductance of this lateral layout is 0.5 nH, extracted from the finite-element simulation tool, Q3D.

![Layout 1](image1)

![Layout 2](image2)

![Layout 3](image3)

Fig. 1-6. Surveyed (a) half-bridge MOSFET module [42], (b) discrete GaN FETs [43], and (c) half-bridge GaN module [29]. (d) is the horizontal power loop of (a); (e) and (f) are vertical power loops of (b) and (c), respectively. Half-bridge GaN module achieves the minimum $L_{loop}$.

The GaN FET with a LGA package prefers the vertical layout since the adjacent top and second layers in Fig. 1-6(e) and (f) offer a smaller loop area. The width of the copper layer is much
larger than its thickness, thus the effective area that the high-frequency current flows through, is much larger. The equivalent loop inductance of a vertical layout is then lower than that of a lateral layout. The footprint of the monolithic half-bridge GaN module is smaller than that of the discrete GaN FETs. The loop inductance for the monolithic GaN is 0.15 nH (Fig. 1-6(c)), lower than that of the discrete GaN, 0.4 nH (Fig. 1-6(b)).

The vertical layout for the discrete-GaN-based POL converter was systematically analyzed in [45]. The concept of the multi-loop layout was introduced and implemented on three examples in Fig. 1-7. The simulated loop inductances of those cases, the split capacitor layout, parallel capacitor layout, and the double-sided layout, are 0.2 nH, 0.23 nH, and 0.1 nH, respectively. All of them are lower than the original vertical layout in Fig. 1-6(b) and (e). Additionally, the thermal performance is improved since the distance between the switches is increased. It should be pointed out that blind vias are used in the double-sided layout in Fig. 1-7(c), which will add some additional costs.

![Fig. 1-7. Surveyed layout with the minimum power-loop inductances for discrete GaN FETs in Fig. 1-6(b): (a) split capacitor layout, (b) parallel capacitor layout, and (c) double-sided layout [45].](image)

Compared with discrete FETs, the monolithic half-bridge modules are more suitable for POL...
applications since they save space, improve efficiency, simplify the layout design, and lower system costs. The simulated voltage peaks of $v_{sw}$ versus $L_{loop}$ for buck converters, with monolithic half-bridge Si and GaN modules, are shown in Fig. 1-8(a). The state-of-the-art layouts in Fig. 1-6 correspond to 1.6 $V_{in}$ for the GaN FET and 1.75 $V_{in}$ for the Si MOSFET at $I_o = 20$ A. The voltage spike is reduced dramatically at light load, e.g., $I_o < 2.5$ A for the GaN FET, as shown in Fig. 1-8(b). This is a result from the partial-ZVS of the active switch. The Si converter has a narrower partial-ZVS range than the GaN converter because of a larger $C_{oss}$. If ZVS could be achieved for an entire load range, the voltage spike could be reduced significantly. The $V_{sw}$-peak droop is caused by the voltage drop of active switch. The $R_{ds(on)}$ of the active switch is 3.7 $\Omega$ for the Si module and 8 $\Omega$ for the GaN module; thus, the $V_{sw}$-peak droop for the GaN module is more significant.

![Graph](image)

Fig. 1-8. (a) Simulated peak voltages of $v_{sw}$ versus loop inductance, for the Si and GaN converters in Fig. 1-4 at $V_{in} = 12$ V, $V_o = 1.2$ V, $I_o = 20$ A, $f_s = 2$ MHz, and $R_{gate} = 2$ $\Omega$. GaN FET has a smaller $L_{loop}$ and lower $v_{sw}$ spike. (b) Simulated peak voltages of $v_{sw}$ are almost independent of load current for state-of-the-art layouts marked by the symbol $\bigcirc$ in (a). The peak voltages are reduced at light load thanks to partial-ZVS.

The commercial buck converter [29] with a monolithic half-bridge GaN module and state-of-the-art layout in Fig. 1-6(c) was tested. The measured $v_{sw}$ and conducted EMI spectrum at $I_o = 20$ A are shown in Fig. 1-9. The voltage overshoot is 44% of $V_{in}$, and the noise in 40–300 MHz
range is significant. The measured overshoot is slightly lower than the simulated one in Fig. 1-8(a) because more damping (higher trace resistance) and temperature effects exist in the experiment.

![Graph showing measured and simulated overshoot with explanation](image)

Fig. 1-9. (a) Measured $v_{sw}$ peak voltage agrees with the simulated one in Fig. 1-8(a) with 8% discrepancy. (b) Measured conducted-EMI noise is significant in 30 – 150 MHz for the two-phase GaN-based buck converters with the layout in Fig. 1-6(c), operating at $V_{in} = 12$ V, $V_o = 1.2$ V, $C_{in} = C_o = 47$ μF, $L_o = 230$ nH, $I_o = 10$ A per phase, and $f_s = 2$ MHz.

The conclusion is given, based on the above analysis, simulation, and experiment. The high turn-on $di/dt$ and parasitic loop inductance would cause severe voltage ringing and EMI noise. Even with the state-of-the-art layout ($L_{loop} = 0.15$ nH), the voltage overshoot for the monolithic half-bridge GaN FET is 44%. In order to overcome this high-frequency noise, the root cause, high $di/dt$, should be avoided. A large $R_g$ could limit the $di/dt$ but increase the loss by ~30%. The ZVS operation for the entire load range is a potential method to solve the high turn-on $di/dt$. This is introduced in Section 1.3.

### 1.3 Two-Phase Zero-Voltage Switching (ZVS) Converters

Conventional hard-switched buck converters can be retrofitted to realize ZVS. The large output inductors could be replaced by smaller ones as shown in Fig. 1-10(a). The current ripple is very high for each phase but has a cancelling effect on the output due to the interleaved phases [19]. The inductor operates under a critical mode at the nominal load. The negative current of $i_{Loa}$
in Fig. 1-11(a) discharges the $C_{\text{oss}}$ of $M_{1a}$ in Fig. 1-10(a) when $M_{2a}$ is turned off. The $v_{\text{ds1a}}$ decreases to zero before the $M_{1a}$ is turned on. Conventional POL converters have no such negative current for ZVS because the inductor current ripple is around 30% of the dc current.

Fig. 1-10. (a) Two-phase quasi-square-wave (QSW) ZVS buck converter needs two inductors with high current ripples; (b) self-assisted ZVS buck converter needs only one inductor with high current ripple [46].

The simulated voltage waveforms when ZVS is realized are shown in Fig. 1-11(b). The active switch $M_{1a}$ and synchronous switch $M_{2a}$ are softly commutated. The body diode of $M_{2a}$ is always off, and $M_{1a}$ has no turn-on current spike. The voltage at the switch node $v_{\text{sw}}$ has no significant voltage overshoot, even with a certain parasitic power loop inductance. Furthermore, the turn-on loss is eliminated because the $v_{\text{ds}}$ and $i_{d}$ have no crossover interval, and the $C_{\text{oss}}$ is softly discharged.

Fig. 1-11. The negative current of (a) $i_{\text{Loa}}$ discharges the $C_{\text{oss}}$ of buck converter in Fig. 1-10(a) to achieve (b) ZVS and low noise at $V_{\text{in}} = 12$ V, $V_{o} = 1.2$ V, $I_{o} = 20$ A, $f_{s} = 2$ MHz, and $L_{\text{loop}} = 0.15$ nH (Fig. 1-3).
The inductors of the two-phase QSW-ZVS buck converter in Fig. 1-10(a) need to handle significant dc and ac fluxes. Both L_{oa} and L_{ob} are subjected to a high core loss. The modified two-phase converter, the self-assisted buck converter in Fig. 1-10(b), utilizes an auxiliary ac-coupled inductor connected between the two switch nodes to achieve ZVS [46]. The peak-to-peak current of the auxiliary inductor L_s is similar to that of L_{oa/b} in Fig. 1-10(a). Since L_s has no dc current, the magnetic design is easier than that for Fig. 1-10(a). Another benefit of the self-assisted ZVS topology is the output voltage ripple could be reduced since the filter inductors L_{oa/b} have small current ripples.

The synchronous MOSFET RMS current of the self-assisted ZVS buck converter is much higher than that of a normal QSW ZVS buck converter, as compared in Fig. 1-12. This is a result from the significant plateau of i_{dM2a}, which happens when both active switches are turned off. Two converters have the same RMS current of i_{dM1a} because their current waveforms of i_{dM1a} are the same.

![Fig. 1-12. The RMS current of i_{dM2a} in (a) two-phase QSW ZVS buck converter is smaller than that in (b) self-assisted ZVS buck converter (Fig. 1-10). The operating conditions are given in Fig. 1-11.](image)

The simulated RMS current for the above ZVS converters, versus the load current, is shown in Fig. 1-13. The normalized RMS current increases dramatically at light load since the current ripple is almost independent of the load current with a fixed switching frequency. The synchronous
switch of the self-assisted ZVS buck converter has a higher RMS current under all load conditions, as a result of the plateau effect. The high RMS current at light load would reduce the converter efficiency significantly. Increasing the switching frequency is a potential method to reduce that RMS current and the related conduction loss.

A Buck converter can achieve ZVS by using quasi-resonant conversion (QRC), multi-resonant conversion (MRC), quasi-square-wave (QSW), or zero-voltage-transition (ZVT) [47]–[50]. The QSW buck converters have the lowest voltage stress and lowest MOSFET count. Two-phase QSW-ZVS buck converters are reviewed in this section. They have low noise and negligible voltage overshoot at the switched nodes. The self-assisted ZVS buck converter is not suitable for POL applications because of the plateau current. The RMS current of the MOSFETs is much higher than that of a hard-switched buck converter, which may outweigh the benefits of low noise and low switching loss. New topologies with a lower current stress, as well as ZVS, are needed. The magnetic design is another challenge since the inductors need to cope with significant dc and ac fluxes for ZVS.

Fig. 1-13. Two ZVS buck converters in Fig. 1-12 have the same RMS current of (a) active switch. The self-assisted ZVS buck converter has higher RMS current of (b) synchronous switch due to the plateau region.
1.4 Applications, Classification, and Synthesis of Coupled Inductors

Multiple inductors or transformers in a single- or multi-phase power converter could be coupled into a single magnetic core to improve power density, efficiency, and dynamic performance. Such inductors with at least two coupled windings and one shared core, are called coupled inductors. The functionality of coupled inductors includes steady-state current ripple reduction, dynamic response improvement, diode reverse-recovery alleviation, soft switching realization, high step-up/down gain conversion, multi-output conversion, and single-stage PFC realization [51]. This section classifies the coupled inductors based on their energy-transfer component, energy-storage type, and voltage relationships. The in-phase coupled inductors and interleaved coupled inductors are introduced by using the examples of the Cuk converter and buck converter, respectively. The concept of Omni-coupled inductors is then put forward, as this concept has already been used in many existing topologies. Finally, some important features of the Omni-coupled inductors are summarized.

1.4.1 Classification of Coupled Inductors

Coupled inductors can be classified from several perspectives. From a phase relationship perspective, coupled inductors can be classified as in-phase inductors or interleaved inductors. The primary and secondary windings of an in-phase coupled inductor have positively or negatively in-phase voltages. The interleaved coupled inductor usually exists in multi-phase interleaved converters. In terms of connectivity between primary and secondary sides, coupled inductors could be classified as an isolated type or non-isolated type. Coupled inductors can also be classified by application type [51]. However, all of the external observations, e.g., phase relationship, isolation type, and application type, are not enough to clearly distinguish any two coupled inductors. Two
more intrinsic properties of coupled inductors, energy transfer and energy storage, should also be taken into account. Based on those two properties, a general classification of the coupled inductors is then possible.

A commonly used equivalent circuit model of coupled inductors is shown in Fig. 1-14. The mutual inductor M, leakage inductors \( L_{lk1/2} \), or both, may need to transfer energy when used in a converter. According to the component that transfers energy, there are three basic types of coupled inductors: the mutual based coupled inductor, the leakage based coupled inductor, and the all-magnetic based coupled inductor.

The method to determine which component transfers energy is given below. If the converter cannot work with zero leakage inductance (i.e., infinity current ripple or zero output voltage), the coupled inductor is leakage based. The leakage inductor must transfer energy. If the converter cannot work with zero mutual inductance, the coupled inductor is mutual based. The mutual inductor then must transfer energy. If the mutual and leakage inductors are both needed to transfer energy, the coupled inductor is based on mutual and leakage inductors. For example, the Flyback converter cannot work if the mutual inductance is zero. Thus, the Flyback coupled inductor is mutual based. The Cuk and buck converter, with negative coupled inductors, can work if the mutual inductance is zero but cannot work if the leakage inductance is zero. Therefore, the coupled inductors in the Cuk and buck converters are leakage based. The same process is applied for the
coupled inductors in the three-switch buck in [60] and Fly-buck converter in [62]. They are based on mutual and leakage inductors because both their mutual and leakage inductors need to transfer energy. The other existing coupled inductors are classified in Table 1-3.

### Table 1-3. Classification of coupled inductors

<table>
<thead>
<tr>
<th>Energy transferred by</th>
<th>Mutual inductor (L&lt;sub&gt;mutual&lt;/sub&gt;)</th>
<th>Leakage inductor (L&lt;sub&gt;leakage&lt;/sub&gt;)</th>
<th>L&lt;sub&gt;mutual&lt;/sub&gt; and L&lt;sub&gt;leakage&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Winding voltages</td>
<td>In-phase</td>
<td>In-phase and interleaved</td>
<td>In-phase</td>
</tr>
<tr>
<td>Current in L&lt;sub&gt;mutual&lt;/sub&gt;</td>
<td></td>
<td>Boost-Flyback with OCI [54], Boost-Push-pull with OCI [55]</td>
<td>Buck with positively-coupled L</td>
</tr>
<tr>
<td>DC</td>
<td>DC</td>
<td>Flyback [52], Tapped-L buck [53]</td>
<td>Fly-buck [62]</td>
</tr>
<tr>
<td>AC</td>
<td>DC</td>
<td>Cuk [56], Sepic [57]</td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td>DC &amp; AC</td>
<td>Buck with negatively-coupled L [58]</td>
<td></td>
</tr>
<tr>
<td>AC</td>
<td>AC</td>
<td>Three-switch buck [60], [61]</td>
<td></td>
</tr>
<tr>
<td>DC &amp; AC</td>
<td>DC &amp; AC</td>
<td>Phase-shifted Forward-Flyback with OCI [66], Multi-phase LLC with OCI [67]</td>
<td></td>
</tr>
<tr>
<td>Isolated Cuk with OCI [59]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Six-switch buck with potential OCI [63]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Another classification is based on the energy-storage type in mutual and leakage inductors. If the mutual and leakage inductors have dc current, they are dc type; otherwise, they are ac type. For example, dc current exists in the mutual and leakage inductors of the Flyback converter. Hence, its mutual and leakage inductors are dc type. For the half-bridge (HB) or full-bridge (FB) based resonant converters, there is no dc component in the mutual inductor and leakage inductor; thus, they have ac mutual inductor and ac leakage inductor. The conventional line transformer is also a
type of ac mutual and ac leakage inductor. Some converters may have multiple mutual inductors. Some of those inductors have dc currents, and the others have ac currents. The mutual inductors then have both dc and ac currents, e.g., Isolated Cuk converter in [59].

Coupled inductors could be further classified by looking at the relationship between $v_{L1}$ and $v_{L2}$ in Fig. 1-14. If the inductor has only two windings, e.g., the Cuk inductor and two-phase buck inductor, the winding voltages have two possible phase relations, in phase and interleaving. If the inductor has more than two coupled windings, e.g., the Boost-Flyback converter in [54], the winding voltages may have mixed phase relations, namely, both in phase and interleaving.

This dissertation is focused on the topology of the resonant cross-commutated buck (rccBuck) converter with coupled inductors. That coupled inductor is leakage based since the current ripple will be infinity if the leakage inductance is zero. The mutual inductors of $L_{rafb}$ and $L_{oaob}$ have no dc current, and the $L_{raob}$ and $L_{rbou}$ have dc current. All leakage inductors have dc current. Another feature of this coupled inductor is the presence of mixed phase relations. The $L_{ra}$ and $L_{rb}$ have interleaved voltages, while the $L_{ra}$ and $L_{ob}$ have in-phase voltages.

### 1.4.2 Interleaved Coupled Inductors

The interleaved coupled inductor is usually applied in multi-phase converters. It is exemplified in a buck converter with the schematic shown in Fig. 1-15(a). Since two windings are interleaved, the inductor voltages have a $180^\circ$ phase shift. The inductor current waveform has four slopes in a switching cycle, as shown in Fig. 1-15(b). Slope 1 determines the steady-state current ripple, and slopes 2 and 4 determine the transient current speed [68].
If only the fundamental component is considered, the sinusoidal inductor voltages are calculated by

\[
\begin{bmatrix}
    V_{Loa} \\
    V_{Lob}
\end{bmatrix} =
\begin{bmatrix}
    L & K_{oaob}L \\
    K_{oaob}L & L
\end{bmatrix}
\begin{bmatrix}
    \frac{di_{Loa}}{dt} \\
    \frac{di_{Lob}}{dt}
\end{bmatrix}
= L
\begin{bmatrix}
    1 & K_{oaob} \\
    K_{oaob} & 1
\end{bmatrix}
\begin{bmatrix}
    \frac{di_{Loa}}{dt} \\
    \frac{di_{Lob}}{dt}
\end{bmatrix}
\]

(1-1)

where \( K_{oaob} \) is the coupling coefficient of \( L_{oa} \) and \( L_{ob} \); \( L = L_{oa} = L_{ob} \) is the self-inductance.

The inductor voltage for one phase is obtained by

\[
V_{Loa} = L(1 - K_{oaob}) \frac{di_{Loa}}{dt}
\]

(1-2)

The equivalent inductance for one phase is \((1-K_{oaob}) L\). A negative coupling is required to increase the equivalent inductance and reduce the current ripple. The real voltage waveforms in Fig. 1-15(b) yield the presence of higher-order harmonics. The odd harmonics always have an 180° phase shift, but the even harmonics are always in phase. The equivalent inductance calculated by (1-1) is only valid for the odd harmonics. For the even harmonics, the equivalent inductance is \((1 + K_{oaob}) L\). If \( K_{oaob} \) is -1, the inductance for the even harmonics would be zero; thus, a tight coupling should be avoided. Under dynamics, \( M_{1a} \) and \( M_{1b} \) are turned on or turned off at the same time. The voltages
of two windings are in phase, and the equivalent inductance under a transient is then determined by \((1 + K_{oaob}) L\), lower than the equivalent inductance of the steady state, \((1 - K_{oaob}) L\). The transient performance could be improved without sacrificing the steady-state inductance.

If all harmonics are considered, the equivalent inductance at the steady state is given by [68]

\[
L_{eq} = \frac{V_{Loppf_s}}{I_{Lopp}D} = \frac{1 - K^2_{oaob}}{1 + \frac{D}{D'} K_{oaob}} L
\]

(1-3)

where \(V_{Lopp}, I_{Lopp},\) and \(D\) are defined in Fig. 1-15(b). When \(D = 0.5\), the even harmonic is zero and \(L_{eq} = (1 - K_{oaob}) L\) agrees with the equivalent inductance for odd harmonics in (1-2).

### 1.4.3 In-Phase Coupled Inductors

The in-phase coupled inductor is introduced by using the example of the Cuk converter with the schematic shown in Fig. 1-16(a). This converter has one phase but two inductors, one input inductor \(L_i\) and one output inductor \(L_o\). The capacitor \(C_{dc}\) blocks the dc voltage, \(V_{in} - V_o\). When \(M_1\) is off and \(M_2\) is on, the voltages across \(L_i\) and \(L_o\) are the same, \(V_o\). When \(M_1\) is on and \(M_2\) is off, the inductor voltages are also the same, \(V_{in}\). Hence, two inductors have the same voltage waveforms and current ripples all the time, as shown in Fig. 1-16(b).

Current ripples of \(L_i\) and \(L_o\) are calculated by

\[
\begin{bmatrix}
V_{Li} \\
V_{Lo}
\end{bmatrix} =
\begin{bmatrix}
L_i & K_{lo}\sqrt{L_i L_o} \\
K_{lo}\sqrt{L_i L_o} & L_o
\end{bmatrix}
\begin{bmatrix}
\frac{di_{Li}}{dt} \\
\frac{di_{Lo}}{dt}
\end{bmatrix}
\]

(1-4)

where \(K_{lo}\) is the coupling coefficient between \(L_i\) and \(L_o\). Let \(M = K_{lo}\sqrt{L_i L_o}\). The equivalent inductances of \(L_i\) and \(L_o\) are obtained by
\[ L_{eqi} = \frac{V_{Lipp} f_s}{I_{Lipp} D} = L_i + \frac{M(M - L_i)}{M - L_o} = L_i + L_i \frac{K_{io}^2 \sqrt{L_o/L_i} - K_{io}}{K_{io} - \sqrt{L_o/L_i}} \]
\[ L_{eqo} = \frac{V_{Lopp} f_s}{I_{Lopp} D} = L_o + \frac{M(M - L_o)}{M - L_i} = L_o + L_o \frac{K_{io}^2 \sqrt{L_i/L_o} - K_{io}}{K_{io} - \sqrt{L_i/L_o}} \]

There are two approaches to design the coupled inductors in the Cuk converter: the balanced design with \( L_i = L_o = M \) and the zero-ripple design with \( L_i > L_o = M \) or \( L_o > L_i = M \). In the balanced design, the equivalent inductances are two times self-inductances in (1-5), having the benefits of reduced core size and winding loss. The equivalent inductance \( L_{eqi} \) or \( L_{eqo} \) in the unbalanced design is infinite, having the benefit of zero input or output current ripple.

The equivalent inductance of the interleaved coupled inductor is dependent upon duty ratio \( D \), while that of the balanced in-phase coupled inductor is independent of \( D \). They are compared in Fig. 1-17. The equivalent inductance of the in-phase case increases linearly with \( |K| \), and the maximum \( L_{eqi}/L_s \) is 2 at \( |K| = 1 \). The equivalent inductance of the interleaved case has a peak when \( D \) is high, e.g., \( D = 0.4 \). It decreases with \( |K| \) monotonically when \( D \) is low, e.g., \( D = 0.1 \). From the transient response point of view, the interleaved coupled inductor is better since it achieves lower transient inductance while maintaining the steady-state inductance. The principle to design the in-phase and interleaved couplings is then clear: the in-phase coupling should be designed as high as...
possible to minimize the magnetic volume, and the interleaved coupling should be designed at the peak (if possible) or satisfy the transient requirement.

![Graph showing normalized steady-state equivalent inductance of the balanced in-phase coupled inductor in comparison to the interleaved coupled inductor.](image)

Fig. 1-17. Normalized steady-state equivalent inductance of the balanced in-phase coupled inductor in (1-5) is higher than that of the interleaved coupled inductor in (1-3).

1.4.4 Existing Omni-Coupled Inductors

The coupled inductors with at least three windings and multiple functionalities (e.g., mixed in-phase and interleaving operations, mixed filters and transformers, etc.) are termed the Omni-coupled inductors. The Omni-coupled inductors naturally have the benefits from the discrete coupled inductors: flux-cancelling effect, reduced self-inductance, small core size, and fast transient response.

An example of the mutual-based Omni-coupled inductors is the Boost-Flyback converter, as shown in Fig. 1-18(a). The boost converter and Flyback converter operate with interleaved voltages (Fig. 1-18(b)). The boost inductor and Flyback transformer share the same E-E core (Fig. 1-18(c)). The boost inductor uses the center leg, and the Flyback transformer uses the side legs. With the phase shift operation and flux-cancelling effect, the peak flux density is reduced by
about 45% [54].

Fig. 1-18. (a) Schematic and (b) typical waveforms of the Boost-Flyback converter [54]. (c) The Omni-coupled inductors comprise three windings and a E-E core.

The inductors in six-switch buck converter introduced in [63] have the potential of being Omni-coupled inductors. The schematic of this converter is shown in Fig. 1-19(a). The four inductors have not been integrated to a single core in [63]. The $L_{ra}$ and $L_{oa}$ formed coupled inductors; the $L_{rb}$ and $L_{ob}$ formed another coupled inductor. However, those four inductors could be integrated to a single core to form Omni-coupled inductors since the voltages $v_{ra}$ and $v_{rb}$ have an 180° phase shift, and $v_{rb}$ and $v_{ob}$ are in phase (Fig. 1-19(b)). The flux density and core size are expected to be reduced.
Two or more interleaved transformers could form Omni-coupled inductors. An example is the phase-shifted Forward-Flyback converter with the schematic shown in Fig. 1-20(a). The intra-windings (in the same transformer) have in-phase voltages, as shown in Fig. 1-20(b). The inter-windings (between transformers) have interleaved voltages. The winding pattern is illustrated in Fig. 1-21. This Omni coupling allows a single E-E core used for two transformers. The dc fluxes generated by $L_{1a}$ and $L_{2a}$ are cancelled in the center leg.
Fig. 1-20. (a) Schematic and (b) typical inductor voltage waveforms of the Phase-shifted Forward-Flyback [66]. Two transformers form Omni-coupled inductors.

Fig. 1-21. Implementation of Omni-coupled inductors in the Phase-shifted Forward-Flyback [66].

The input inductor, output inductor, and transformer of an isolated Cuk converter in [59] can also form Omni-coupled inductors, as shown in Fig. 1-22(a). The $L_i$ is designed with zero current ripple since $L_i$ and $L_{d1}$ have in-phase voltages. The $L_o$ is also designed with zero current ripple since $L_o$ and $L_{d2}$ have in-phase voltages. The zero-ripple mechanism is introduced in Sub-section 1.4.3. The $L_{d1}$ and $L_{d2}$ have no dc current since $C_{dc1}$ and $C_{dc2}$ block dc current. The $L_i$ and $L_o$ are based on leakage inductors; thus, the turn’s ratio of $L_i$ and $L_o$ have no impact on the $V_{in}/V_o$. The $L_{d1}$ and $L_{d2}$ are mutual inductors; thus, the turn’s ratio of $L_{d1}$ and $L_{d2}$ has impact on
The Omni-coupled inductors are implemented by an E-I core as shown in Fig. 1-22(c). The $L_{t1}$ and $L_{t2}$ windings are placed at the center leg to maximize the coupling coefficient of $K_{t1t2}$. The $L_i$ and $L_o$ windings are placed at two side legs. The leakage inductances of $L_i$ and $L_o$ would not cause voltage spikes. However, the leakage inductances of $L_{t1}$ and $L_{t2}$ would cause voltage spikes on switched nodes, and thus high $K_{t1t2}$ is desired.

![Electrical schematic and voltage waveforms](image)

Fig. 1-22. (a) Schematic and (b) typical inductor voltage waveforms of the isolated Cuk converter [59]. (c) The $L_i$, $L_o$, and transformer form Omni-coupled inductors by using an E-I core.

The general principles to construct Omni-coupled inductors are summarized as follows:

- All windings are required to have the same frequencies.
- If two inductors have in-phase voltages, a positive coupling that increases the equivalent inductance in (1-5) is desired; otherwise, the volume of the coupled-inductor may be larger.
than that of discrete inductors. If two inductors have interleaved voltages, a negative coupling that increases the equivalent inductance in (1-3) is desired. If multiple windings are coupled, a small equivalent inductance, as exemplified in Section 4.2, is beneficial for the core size.

- If the coupled inductors are based on mutual inductors, the turn’s ratio has impact on voltage gain, e.g., Flyback converter, tapped-L buck converter, and three-switch buck converter. If the coupled inductors are based on leakage inductors, the turn’s ratio has no impact on voltage gain, e.g., Cuk converter, buck converter, and rccBuck converter.

In summary, this section classifies the coupled inductors by checking the energy-transfer component, energy-storage type, and winding-voltage relationships. This method may be helpful in understanding the intrinsic properties of the coupled inductors in various applications. The operating principles of the coupled inductors with in-phase or interleaved voltages are introduced by using the examples of the Cuk converter and buck converter. Besides those exemplary converters, the in-phase operation also exists in transformer-based converters, i.e., Flyback and LLC converters. The interleaved operation also exists in multi-stage converters, i.e., Boost-Flyback converter and Boost-Push-Pull converter. The coupling coefficient of the interleaved coupled inductors is usually designed around 0.4 – 0.7, lower than that of in-phase coupled inductors, ~0.9. The in-phase coupled inductor has the benefit of a small inductor size. The interleaved coupled inductor has the advantage of a fast transient response. The Omni-coupled inductors have both benefits, and are implemented in some existing converters such as the Boost-Flyback converter, phase-shifted Forward-Flyback converter, multi-phase LLC converter, etc. One-turn Omni-coupled inductors for the rccBuck converter are described in Chapter 4.
1.5 Small-Signal Modeling of Dc-Dc Converters

The small-signal modeling of dc-dc converters has been developed for about a half century and is important for the feedback loop design in POL regulators. According to the effective frequency range, the small-signal model can be classified as a low-frequency model or high-frequency model. The low-frequency model is available for voltage-mode-controlled pulse-width-modulated (PWM) converters, in which the output filter and compensator act as low-pass filters to block the high-frequency component in the control loop. The low-frequency model is accurate enough to predict the dynamic performance.

The high-frequency model applies for two kinds of converters: the fast-controlled PWM converter and the resonant converter. The fast controls in PWM converters include, but are not limited to, current-mode control, \( V^2 \) control, charge control, etc. The inductor current or capacitor voltage ripples are sensed in the feedback loop to improve the dynamic response. The low-frequency model without the ripple effect cannot work in this scenario. Another kind of converter that requires a high-frequency model is the resonant converter. The resonant frequency is close to the switching frequency, and the resonant components need to transfer energy. The high-frequency harmonics, up to the switching frequency, should be included in the model.

This dissertation is focused on the modeling and control of the resonant cross-commutated (RCC) converter. This converter belongs to the PWM converter family but with additional resonant filters. Three classical average models are introduced in this section. The average-behavior model is selected for deriving the transfer functions of the RCC converter. The impact of the resonant frequency of the filters on the model accuracy is studied by using the example of a buck converter at the end of this section.
1.5.1 Equivalent-Circuit based Average-Behavior Model

The basic concept in low-frequency modeling is to average the switching waveforms and represent the switched dc-dc converters by approximate continuous models. This average concept was first put forward by Gene W. Wester in 1972 [69]. Equivalent circuits were developed for designing and understanding the dynamic behavior of corresponding switched power stages. This sub-section introduces the equivalent-circuit based average-behavior model by using the example of a buck converter.

The schematic of a buck converter is shown in Fig. 1-23(a). The typical voltage waveform at the switch node $v_{sw}$ and the current $i_{M1a}$ are shown in Fig. 1-23(b). The $v_{sw}$ is averaged as $V_{sw} = dV_{in} = V_o$, and the $i_{M1}$ is averaged as $I_{M1} = dI_L$, where $d$ is the duty ratio. The $M_1$ is replaced by a dependent current source, $dI_L$, as illustrated in Fig. 1-23(c). Similarly, the $M_2$ is replaced by a dependent voltage source, $dV_{in}$. Those dependent sources are equivalent to a dc transformer with the turn’s ratio $1:d$, as shown in Fig. 1-23(d). The buck converter with switched waveforms is then modeled as a continuous circuit. A reversed replacement is also effective to obtain the continuous circuit: the MOSFET $M_1$ is replaced by a voltage source, $(1-d)V_{in}$, and $M_2$ is replaced by a current source, $(1-d)I_o$. The simplified circuit is equivalent to Fig. 1-23(d).

In order to derive the small-signal model, a small perturbation of the control parameter is applied on the average model. For example, $\hat{d}$ is taken into account to derive the control-to-output transfer function. Since the input source is ac shorted, and the small terms are ignored, the small-signal equivalent circuit is simplified to Fig. 1-24(b).
Fig. 1-23. (a) Buck converter with (b) the PWM waveforms of \(v_s\) and \(i_{M1}\). (c) MOSFETs are replaced by duty-ratio-controlled voltage source and current source. (d) Simplified large-signal model.

Fig. 1-24. (a) Perturbation is added on the average model of Fig. 1-23(d). (b) Simplified small-signal model.

The transfer function \(G_{vd} = \frac{v_o}{d}\) is calculated by using the Laplace transform

\[
G_{vd} = \frac{V_{in}}{L_o C_o s^2 + \frac{s}{C_o R_L} + \frac{1}{L_o C_o}}
\]  
(1-6)
The key steps to manipulate the average-behavior model are summarized below. The MOSFETs with switched voltages or current are replaced by duty-ratio-dependent voltage or current sources. A small perturbation of the control parameter is applied on the large-signal behavior model to derive the small-signal behavior model. Finally, the Laplace transform is performed to calculate the transfer function.

1.5.2 Three-Terminal Switch Model

The active and passive switches in a PWM converter are modeled as a three-terminal nonlinear device, called a three-terminal switch [74]. The dc and small-signal characteristics of a large class of PWM converters can then be obtained by a substitution of the PWM switch in Fig. 1-25(a), with its equivalent circuit models in Fig. 1-25(b).

![PWM switch models](image)

Fig. 1-25. PWM switch comprising (a) an active and a passive switch, (b) its PWM switch large-signal model, and (c) its PWM switch small-signal model.

The alternate forms of the PWM switch models introduced in [75] are more convenient for analysis and could be used to graphically manipulate the converter circuit to a form that can be analyzed by inspection. However, the three-terminal model is only effective for the converters with one or more basic ‘a-p-c’ switched cells (Fig. 1-25(a)) which can be identified easily. When the converter has a complicated switched network, this method may not work. For example, in the series-capacitor buck converter in Fig. 1-1(b), the MOSFETs $M_{1b}$ and $M_{2b}$ could be replaced by a
three-terminal switch cell easily, but the MOSFETs $M_{1a}$ and $M_{2a}$ are separated by a capacitor and cannot be modeled as a three-terminal switch. The rccBuck converter is another example that cannot be modeled by three-terminal switches because of the additional resonant tanks of $C_{ra/b}$ and $L_{ra/b}$.

1.5.3 State-Space Average Model

The state-space model is a general method to analyze the switched converter. The exact state-space representation could be used to derive the steady-state waveforms for any converters with or without resonant tanks in a numerical way and is performed in Chapter 2. The state-space model could also be averaged to derive the transfer functions. The state-space average model was proposed by R.D. Middlebrook in 1976 [71]. It was extended to a GSSA model in [72] and TIMF model in [73]. Those modified state-space models consider the effect of high-order harmonic ripples. This sub-section only introduces the original averaged state-space model by using the example of a buck converter.

![Switched states of buck converter when the active switch is (a) on and (b) off.](image)

The first step is to derive the state space matrices for each switch state. The buck converter has two switch stages as shown in Fig. 1-26. The state-space representations for the two switched linear networks are
\[
\frac{dx}{dt} = A_1 x + B_1 v_{in}, v_o = c_1^T x, x = [i_{L_o}, v_o] \quad 0 < t < \frac{D}{f_s}
\] (1-7)

\[
\frac{dx}{dt} = A_2 x + B_2 v_{in}, v_o = c_2^T x \quad \frac{D}{f_s} < t < \frac{1}{f_s}
\] (1-8)

\[
A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_tC_o} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_o} & 0 \\ 0 & 0 \end{bmatrix}, A_2 = \begin{bmatrix} 0 & -\frac{1}{L_o} \\ \frac{1}{C} & -\frac{1}{R_tC_o} \end{bmatrix}, B_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, c_{1,2} = [0] \]
(1-9)

The averaged system is given by

\[
\frac{dx}{dt} = [A_1 d + A_2 (1-d)] x + [B_1 d + B_2 (1-d)] v_{in}
\]

\[
v_o = [c_1^T d + c_2^T (1-d)] x
\] (1-10)

The steady-state average, or simply dc, values of the states are calculated by

\[
X = -A^{-1} B v_{in}, v_o = c^T X
\] (1-11)

where \( A = A_1 d + A_2 (1-d), B = B_1 d + B_2 (1-d), \) and \( c^T = c_1^T d + c_2^T (1-d) \).

Perturbations are applied on the large-signal average model: \( d = D + \hat{d} \) and \( x = X + \hat{x} \). The linearized small-signal model is

\[
\frac{d\hat{x}}{dt} = A\hat{x} + [(A_1 - A_2) X + (B_1 - B_2) v_{in}] \hat{d}
\]

\[
\hat{v}_o = c^T \hat{x} + (c_1^T - c_2^T) X \hat{d}
\] (1-12)

The control-to-state transfer function is then obtained by using Laplace transform

\[
\frac{\hat{x}(s)}{d(s)} = (sI - A)^{-1} [(A_1 - A_2) X + (B_1 - B_2) v_{in}]
\] (1-13)

The control-to-output transfer function is

\[
G_{vd} = \frac{\hat{v}_o(s)}{d(s)} = c^T \frac{\hat{x}(s)}{d(s)} + (c_1^T - c_2^T) X
\] (1-14)
The $G_{vd}$ calculated by (1-14) is the same as (1-6).

The most significant advantage of the state-space average model is the fast computing of transfer functions since the matrix calculation is easy for computers. The disadvantage is the lack of physical insights of the converters, especially when the order of the system is more than two. Opposite to the state-space average model, the equivalent circuit model has more physical meaning but is more time-consuming. In the modeling of the rccBuck converter, the equivalent-circuit model is employed for a better understanding of the poles and zeros caused by the output filters and input resonant filters.

1.5.4 PWM Converters with Resonant Filters

The $L_r$ and $C_r$ in the rccBuck converter are essentially filters, although they have resonant waveforms. They are similar to the $L_o$ and $C_o$ in a buck converter but with $f_{r0} = 1/(2\pi\sqrt{L_oC_o})$ closer to $f_s$. The objective of this sub-section is to check if the average model is effective when the $f_{r0}$ increases from dc to nearly $f_s$.

The simulated and modeled $G_{vd}$ parametric with $f_{oN} = f_{r0}/f_s$ for a synchronous buck converter is shown in Fig. 1-27. The dc gain of the average model at $f_{oN} = 0.9 f_s$ is 3 dB lower than that of Simplis. The phase has a $\sim 5^\circ$ discrepancy in 100 kHz to 1 MHz for $f_{oN} = 0.9 f_s$. If $f_{oN}$ is too high, e.g., 0.7 $f_s$, the output inductor and capacitor have significant resonant waveforms. However, the modeled $G_{vd}$ still matches with the simulated one with negligible discrepancies.
Fig. 1-27. Modeled control-to-output transfer functions agree with simulated ones when $f_{on}$ is swept from 0.1 to 0.9 in the synchronous buck converter in Fig. 1-23(a) with $V_{in} = 12$ V, $D = 0.275$, $f_s = 2$ MHz, $R_L = 0.33 \Omega$, and $Z_{on} = \sqrt{L_o/C_o/R_L} = 0.1$.

Compared with the resonant components in resonant converters, the filters in PWM converters may have resonant waveforms, but they do not transfer energy. They have no impact on the voltage gain. However, the resonant tanks in the resonant converters need to transfer energy. Their resonant frequencies and tank impedances have significant impacts on the voltage gain. The rccBuck converter belongs to the PWM converter family because the $L_r$ and $C_r$ have a negligible impact on the voltage gain when the converter operates under continuous voltage mode. Therefore, the average model is expected to be effective for the rccBuck converter, which will be demonstrated in Chapter 5.

1.6 Contributions of This Dissertation

1.6.1 Low-Noise Resonant Cross-Commutated Buck Converter

The resonant current from one phase of two interleaved dc-dc converters is injected into the other phase for zero turn-on of all switches within the entire load range and zero turn-off of synchronous switches at the nominal load. This concept, named resonant cross-commutation, was applied in a two-phase buck converter to reduce the voltage overshoot and switching noise. Clean
waveforms of drain-to-source voltage of the active switch, $v_{ds1a}$, switch node voltage, $v_{swa}$, and gate-driving voltage, $v_{g1a}$, are observed in the experiment (Fig. 1-28(a)). The conducted EMI is lower than that of the hard-switched buck by ~15 dB from 6 MHz to 500 MHz (Fig. 1-28(b)).

![Waveform Diagram](image)

---

**Fig. 1-28.** (a) The measured voltages are clean when ZVS is achieved. (b) High-frequency EMI noise is reduced by 15 dB for the rccBuck converter in Fig. 3-26(a) at $V_{in} = 12$ V, $V_o = 1.2$ V, $I_o = 20$ A, and $f_s = 2$ MHz.

The input inductors $L_{ra/b}$ conduct non-pulsating input current, thus the low-frequency harmonics, e.g., $2^{nd}$ and $3^{rd}$ orders, are reduced. The ZVS solves the turn-on ringing problem, consequently the high-frequency noise at 100–500 MHz is reduced. Some other technologies also contribute to the noise reduction. All switches are turned off with zero-current-switching (ZCS) or near-ZCS at nominal load under discontinuous voltage mode (DVM). The negligible turn-off current reduces the turn-off noise. The switching-loop layout of the GaN-based rccBuck converter employs an interleaved placement of $C_r$. The $C_{ra}$-$C_{rb}$ loop inductance is 0.33 nH, and the $C_r$-GND loop inductance is 0.25 nH. Those low parasitic inductances allow the rccBuck converter to run at a higher frequency, e.g., 10 MHz. The Omni-coupled inductors utilizing PCB windings and a twisted E-E core, lower the mismatch between the two phases, reducing the fundamental-frequency noise by 18 dB.
1.6.2 Steady-State Modeling of RccBuck Converter under CVM and DVM

The closed-form analytical formulas of four switched stages were derived in order to understand the operating principles of an rccBuck converter. The calculated steady-state waveforms of the inductor current agree with the measured ones with the error less than 1% (Fig. 1-29(a)). The state-space model was also developed to calculate the gain and stress curves. Based on those normalized curves, the step-by-step design procedure was presented. The normalized resonant frequency \( f_n \), voltage gain \( V_o/V_{in} \), and inductance ratio \( L_n \) under boundary voltage mode (BVM), follow the curves in Fig. 1-29(b). The operation mode is CVM when \( f_n \) is below the BVM line for lower \( L \tau \) loss, and DVM when \( f_n \) is above the BVM line for lower turn-off loss. The CVM design has less current ripple at heavy load, and the DVM design can achieve less current ripple at light load, by slightly increasing the switching frequency. The DVM rccBuck converter has a special low-impedance switched stage, in which the \( C_{ra} \) is shorted by the \( M_{2a}, M_{1b}, \) and \( M_{2b} \) (Fig. 2-1(b)). The capacitor \( C_{ra} \) and parasitic inductances cause a severe ringing but could be solved by adding a clamped diode without sacrificing the efficiency.

![Fig. 1-29](a) Modeled inductor current waveforms of rccBuck converters in Fig. 2-57 agree with measured and simulated ones at \( V_{in} = 12 \) V, \( V_o = 3.3 \) V, \( I_o = 20 \) A, and \( f_s = 2 \) MHz. (b) Normalized resonant frequency, \( f_n \), versus \( V_o/V_{in} \) with \( M_{1a,1b} \) turned on at zero voltage and \( M_{2a,2b} \) turned off at zero current (on BVM lines).
1.6.3 Design Methodology of a One-Turn Inductor with Significant Ac and Dc Fluxes

The inductors in an rccBuck converter need to conduct high current ripple for ZVS. Commercial one-turn inductors are not suitable for such applications due to the high core loss and high ac resistance. A systematic design of a one-turn inductor is presented to overcome the above limitations. Three gap placements were compared, and the vertical-two-gap design was selected due to the lowest ac resistance. The ac winding loss of the vertical-gap one-turn inductor was modeled considering the penetrating field, reducing the error from 41% ([140]) to 10%, compared with finite-element simulation (FES) in Fig. 3-12(a). Several MHz magnetic materials were compared, and the impact of dc bias on the core loss was modeled. The inductance and loss models greatly reduced the calculation time compared to the FES from 1.5 minutes to 0.12 seconds. The winding and core dimensions were designed to minimize the total loss within a smaller volume than that of a commercial product. The designed one-turn inductors were demonstrated experimentally to have 2.1% higher efficiency than the commercial inductors with similar inductances and double magnetic volumes, on the same rccBuck converter (Fig. 1-30).

![Graph showing efficiency comparison](image)

Fig. 1-30. (a) Fabricated one-turn inductors were applied in the rccBuck converter to achieve (b) the maximum efficiency. The converter prototypes are shown in Fig. 3-26.
1.6.4 Omni-Coupled Inductors Implemented by a Twisted E-E Core

The steady-state currents of the Omni-coupled inductors (OCI) were modeled by the decomposition of the common mode voltage and differential mode voltage. The OCI with specified inductances was realized by a twisted E-E core. The $L_{ra}$ and $L_{ob}$ are negative coupled so the input and output dc currents have a cancelling effect. The inductances of the twisted E-E core were modeled by a reluctance network with an error less than 10%. The time-domain core loss was modeled by the equivalent elliptical loop (EEL) method. The inductance and core loss models greatly reduced the calculation time compared to the FES from 13 minutes to 4 seconds. The winding loss was modeled numerically through a finite element simulation. The PCB winding in the OCI simplifies the fabrication work and reduces the labor. The prototype of the OCI-rccBuck converter is shown in Fig. 1-31(a). The total volume is reduced by 43%, and the efficiency is improved by 3.3% at 20 A, compared with the Murata module in Fig. 1-31(b).

![Diagram of OCI and Murata module comparison](image)

Fig. 1-31. (a) The OCI realized by a twisted E-E core was applied in a 2 MHz rccBuck converter in Fig. 4-43 to achieve (b) the maximum efficiency (96.2% peak) compared with commercial POL modules in [13]–[16].
1.6.5 Small-Signal Modeling and Feedback Design of RccBuck Converter

The modeled control-to-output transfer function is accurate up to $f_s/2$, as demonstrated in Fig. 1-32. The type-III compensator with an additional phase-lead compensation could offer a $56^\circ$ phase margin for the rccBuck converter under voltage mode control. The corresponding load-transient performance is comparable to that of a buck converter with the same bandwidth and without input filters, as shown in Fig. 1-33(a) and (b). An input filter is added in the buck converter to mitigate the high-frequency EMI, and causes 60% lower bandwidth, three times larger $C_o$, and doubled settling time during a load transient, compared to the rccBuck converter with the same EMI spectrum.

![Graph showing gain and phase responses](image)

**Fig. 1-32.** Modeled $G_{vd}$ of rccBuck converter in Fig. 5-23 agrees with simulated one. Buck converter without input filters (Fig. 5-17) has the same bandwidth (100 kHz) with rccBuck converter. Buck converter using an input filter (Fig. 5-23) achieves similar EMI with rccBuck converter, but has a lower bandwidth (40 kHz).

The motivations and contributions of this dissertation are summarized in Table 1-4. Steady-state analysis, one-turn inductor design, Omni-coupled inductors design, and feedback design, are discussed in Chapter 2–Chapter 5, respectively. All of the innovations used for the rccBuck converter could be extended to other topologies. For example, the design methodology of the one-turn inductor is also available for a CRM buck converter. The design methodology of the Omni-coupled inductors is also available for the Phase-shifted Forward-Flyback converter [66].

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Fig. 1-33. Simulated load-transient response of (a) rccBuck converter in Fig. 5-23(a) is similar to that of (b) buck converter without input filter in Fig. 5-17. (c) Buck converter with an input filter in Fig. 5-23(b) has a longer settling time. The compensator parameters are given in Table 5-1.

Table 1-4. Motivations and contributions of this dissertation

<table>
<thead>
<tr>
<th>Motivations</th>
<th>Contributions</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimize switching noise of POL converters</td>
<td>• RccBuck converter with ZVS and minimum current stress</td>
<td>• ( V_{\text{SW}} ) overshoot &lt; 1 V</td>
</tr>
<tr>
<td></td>
<td>• ZCS for all switches under DVM</td>
<td>• High-frequency EMI reduced by 15 dB</td>
</tr>
<tr>
<td>Minimize size and loss of a one-turn inductor with significant ac and dc fluxes</td>
<td>• Modified winding loss model considering penetrating field</td>
<td>• Error of winding loss model &lt; 10%</td>
</tr>
<tr>
<td></td>
<td>• Systematic design of one-turn inductor</td>
<td>• Magnetic volume reduced by 50%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Efficiency improved by 2%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Compared to commercial one-turn L)</td>
</tr>
<tr>
<td>Minimize the total magnetic volume of rccBuck converter</td>
<td>• Omni-coupled inductors implemented by twisted E-E core and PCB winding</td>
<td>• Error of inductance model &lt; 10%</td>
</tr>
<tr>
<td></td>
<td>• Inductances and loss models of twisted E-E core</td>
<td>• Error of core loss model &lt; 11%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Magnetic volume reduced by 57%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Efficiency improved by 0.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Compared to discrete one-turn L)</td>
</tr>
<tr>
<td>Realize feedback control of rccBuck converter</td>
<td>• Average-behavior small-signal model</td>
<td>• 56° phase margin, 0.12 V overshoot, and 25 μs settling time, comparable to buck converter</td>
</tr>
</tbody>
</table>
1.6.6 Dissertation Outline

This dissertation introduces the topologies, operation principles, steady-state modeling, magnetic design, small-signal modeling, and feedback control of the resonant cross-commutated (RCC) dc-dc regulators. The objective is to reduce the switching noise while maintaining the efficiency, size, and transient response.

Chapter 1 discusses the background of point-of-load converters and the noise from hard switching. A review of traditional methods to reduce the switching noise is also given which initiates the challenges and scope of this study. Chapter 2 introduces the operation principles of the rccBuck converter. The switched stages under CVM and DVM are described individually. A systematic design, based on the state-space model, is also given. Finally, the voltage gain and stress curves are verified experimentally by using Si-based rccBuck converters.

Chapter 3 introduces the design methodology of a one-turn inductor with significant dc and ac fluxes. Ac winding loss is modeled by calculating the magnetic field strength in the window area. The core loss is modeled by using the equivalent elliptical loop (EEL) method. The designed one-turn inductors are compared to the commercial ones in the same rccBuck converter.

Chapter 4 discusses the Omni-coupled inductors (OCI) design for the rccBuck converter. The required coupling coefficients and inductances are realized by a twisted E-E core and PCB windings. The fabricated OCI-rccBuck converter is compared to commercial POL power modules in terms of efficiency and volume.

Chapter 5 employs the average-behavior method to derive the small-signal model of the rccBuck converter. The compensator is designed accordingly. The closed-loop response is compared to that of buck converters with and without input filters.

Conclusions and future work are given in Chapter 6.
Chapter 2 Steady-State Modeling of Resonant Cross-Commutated Converter

Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_n$</td>
<td>Normalized resonant frequency $f_r/f_s$</td>
</tr>
<tr>
<td>$f_r$</td>
<td>Resonant frequency of $L_r$ and $C_r$</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>$L_n$</td>
<td>Inductance ratio $L_n/L_r$</td>
</tr>
<tr>
<td>$N$</td>
<td>Number of phases</td>
</tr>
<tr>
<td>$R_{ds(on)}$</td>
<td>On-state resistance</td>
</tr>
<tr>
<td>$t_{ZVS}$</td>
<td>Minimum dead time for ZVS</td>
</tr>
<tr>
<td>$Z_n$</td>
<td>Normalized impedance</td>
</tr>
</tbody>
</table>

The basic cell and operating principles of the resonant cross-commutated (RCC) converter are introduced in this chapter. Closed-form formulas of inductor current and capacitor voltages were derived during each switched state. In modeling continuous voltage mode, the complex fourth-order circuit mode was solved by decomposing it to two second-order modes. The current to discharge the parasitic capacitor of the MOSFET was calculated by using a state-plane trajectory. In the analysis of the discontinuous voltage mode, the severe ringing was addressed and solved by clamped diodes. The state-space representation method was employed to calculate the inductor RMS current, MOSFET turn-off current, and voltage stresses. The expectations of the CVM operation were validated by three RCC converters switched at 2 MHz with 12 V input, 3.3 V at 20 A output, and peak efficiencies of 93.6%, 93.6%, and 93.3%. The discrepancy between the measured and modeled instantaneous state variables was less than 2%. The DVM operation was validated by an rccBuck converter with the same specifications as the above CVM case, except for
the 1.2 V output. The severe ringing was eliminated in the experiment by using clamped diodes, while maintaining efficiency. Another 1.2 V CVM rccBuck converter was fabricated and compared to the DVM converter. The CVM converter achieved 1.2% higher efficiency at 20 A by switching at 2 MHz, but 1.9% lower efficiency at 5 A with a 2.6 MHz switching frequency. The related simulation files are given in Appendix F.

2.1 Introduction

2.1.1 Generalized Resonant Cross-Commutated Converters

Zero-voltage switching (ZVS) is realized by discharging the output capacitance (C_{oss}) of the MOSFET before the channel is turned on. The discharging current could be offered by the output inductor in a quasi-square-wave (QSW) converter, or the auxiliary inductor in a ZVT converter [76]–[77]. A two-phase buck converter with input filters, as shown in Fig. 2-1(a), is modified to a ZVS topology in Fig. 2-1(b). The resonant current generated from one phase, is injected into the switched node of the other phase, to turn on the active switch at zero voltage over a wide load range, and to turn off the synchronous switch at near-zero current at rated load. The modified two-phase buck converter in Fig. 2-1(b) is termed a resonant cross-commutated buck converter (rccBuck).

![Diagram](image_url)

Fig. 2-1. (a) Two-phase buck converter with input filters are modified to (b) an rccBuck converter. The general cell of the resonant cross-commutation (RCC) in Fig. 2-2(a) is also valid for other
multi-phase converters such as a boost converter, buck-boost converter, and full-bridge converter, in Fig. 2-2(b)–(d). ZVS is available for all switches, and voltage gain may be improved, due to the crossed capacitors storing energy. Crossed capacitors were also used in the converters in [78]–[83], but they have different functionalities, such as reducing the input current ripple, reducing the voltage stresses, offering Z-source features, etc.

![Image of multi-phase converters](image_url)

Fig. 2-2. (a) RCC cell applied on (b) boost converter, (c) buck-boost converter, and (d) full-bridge converter. The simulated waveforms of the rccBoost converter are shown in Fig. 2-3(a). The output voltage is higher than the input voltage with the voltage gain given by

\[
\left(\frac{V_o}{V_{in}}\right)_{rccBoost} = \frac{4 - D}{2 - D} \quad (1 \leq D \leq 2) \tag{2-1}
\]

The synchronous MOSFET \(M_{2a}\) achieves ZCS at the rated load, and all MOSFETs achieve ZVS within an entire load range. The ZVS is achieved when the valley of \(i_{Lia}\) is higher than the peak of \(i_{Lrb}\). The voltage stress is \(\sim 2(V_o - V_{in})\) for \(M_{2a/b}\) and \(\sim (V_o - V_{in})\) for \(M_{1a/b}\). The rccBoost converter is a dual circuit of rccBuck converter, and the rccBuck converter can be employed in bi-directional applications.
The simulated waveforms of the rccBuck-Boost converter are shown in Fig. 2-3(b). The voltage gain is

\[
\left( \frac{V_o}{V_{in}} \right)_{rccBuck-Boost} = \frac{D}{2-D} \quad (0 \leq D \leq 1)
\]  

(2-2)

The synchronous MOSFET M2a achieves ZCS at the rated load, and all MOSFETs achieve ZVS within an entire load range. The ZVS is achieved when the valley of i_{Lob} is higher than the peak of i_{Lra}. The voltage stress is \(~2V_{in}\) for M1a/b and \(~V_{in}\) for M1a/b. The output voltage is negative, following conventional Buck-Boost converter.

Fig. 2-3. (a) Simulated waveforms of rccBoost converter in Fig. 2-2(b) with \(V_{in} = 12\) V, \(V_o = 48\) V, \(f_s = 2\) MHz, \(I_o = 2\) A, \(L_r = L_o = 1.4\) μH, \(C_r = 18\) nF, and \(C_o = 800\) nF. (b) Simulated waveforms of rccBuck-Boost converter in Fig. 2-2(c) with \(V_{in} = 12\) V, \(V_o = 3.3\) V, \(f_s = 2\) MHz, \(I_o = 20\) A, \(L_r = L_o = 230\) nH, \(C_r = 110\) nF, and \(C_o = 4.2\) μF. Both converters achieve ZVS for all switches.

An isolated full-bridge converter, even without RCC, can achieve ZVS within a wide load range. The MOSFET M2a conducts the circulating current of the magnetizing inductor when M2a and M1b are turned on, inducing high RMS current of M2a, as illustrated in Fig. 2-4(c).
Fig. 2-4. Schematics of (a) conventional full-bridge converter and (b) rcc-full-bridge converter in Fig. 2-2(d), with $V_{in} = 100 \, V$, $V_o = 12 \, V$, $f_s = 2 \, MHz$, and $I_o = 50 \, A$. (c) and (d) are corresponding simulated waveforms. The rcc-full-bridge converter has lower RMS current of $M_{2a}$.

In the rcc-full-bridge converter in Fig. 2-4(b), the MOSFET $M_{2a}$ conducts ($i_{Lra} + i_{Lrb}$) when $M_{2a}$ and $M_{1b}$ are turned on, reducing the RMS current of $M_{2a}$, as shown in Fig. 2-4(d). The RMS currents of $M_{1a}$ in both converters are similar. The voltage stresses of all MOSFETs in conventional full-bridge converter are $V_{in}$. The voltage stress is $2(V_{in} - N_t V_o)$ for the active MOSFETs and $(V_{in} - N_t V_o)$ for the synchronous MOSFETs in the rcc-full-bridge converter, where $N_t$ is the turn’s ratio of the transformer. The voltage gain of the rcc-full-bridge converter is 48
\[ \frac{V_o}{V_{in}}_{\text{rcc-full-bridge}} = \frac{D}{N_t(2 + D)} \quad (0 \leq D \leq 1) \] (2-3)

The voltage stresses and voltage gain of rcc-full-bridge are similar to those of the rccBuck converter. The functionality of \( L_r \) and \( C_r \) is to reduce the RMS current of \( M_{2a/b} \) (in rcc-full-bridge converter) instead of to realize ZVS of \( M_{1a/b} \) (in rccBuck converter).

### 2.1.2 Multi-Phase Resonant Cross-Commutated Buck Converter

The two-phase rccBuck converter in Fig. 2-1(b) is extended to a three-phase converter in Fig. 2-5(a). The input currents \( i_{Lra}, i_{Lrb}, \) and \( i_{Lrc} \), are injected into the switched nodes \( swc, swa, \) and \( swb \), respectively. ZVS is realized for all switches. The three-phase and two-phase converters have the same voltage stresses, \( 2(V_{\text{in}} - V_o) \) for the active MOSFET, and \( (V_{\text{in}} - V_o) \) for the synchronous MOSFET, as shown in Fig. 2-6. The driving signals of the active MOSFETs are not recommended to be overlapped because the MOSFET would sustain a high voltage stress. For example, if \( M_{1a} \) and \( M_{1b} \) were turned on at the same time, the voltage across \( M_{1c} \) would be \( V_{\text{Cab}} + V_{\text{Cbc}} + V_{\text{Cca}} = 3(V_{\text{in}} - V_o) \). If three active MOSFETs were turned on at the same time, all capacitors would be shorted, and this situation should be avoided.

![Fig. 2-5. (a) Three phase rccBuck converter and (b) N-phase rccBuck converter.](image)
The active MOSFETs and resonant capacitors in Fig. 2-1(b) form a loop: M_{1a}-C_{rb}-M_{1b}-C_{ra}-M_{1a}. Similarly, Fig. 2-5(a) has a loop: M_{1a-c_{ab}}-M_{1b-c_{bc}}-M_{1c-c_{ac}}-M_{1a}. Following this idea, a multi-phase rccBuck converter is then constructed. The schematic of an N-phase rccBuck converter is shown in Fig. 2-5(b). All of the resonant capacitors and active switches form a loop. The input inductors converge to the V_{in} node. The output inductors converge to the V_{o} node.

![Image](image_url)

Fig. 2-6. Typical waveforms for three-phase rccBuck converter in Fig. 2-5(a) at V_{in} = 12 V, V_{o} = 2.5 V, L_{r} = 150 nH, C_{r} = 350 nF, L_{o} = 200 nH, f_{s} = 2 MHz, and I_{o} = 20 A.

Let D = t_{D}Nf_{s}, where t_{D} is the on-time of the active MOSFET (Fig. 2-6). Each capacitor in Fig. 2-5(b) has the dc voltage (V_{in} - V_{o}). The switched node voltages are (V_{in} - V_{o}). The averaged v_{sw} is V_{o}, namely, D(V_{in} - V_{o})/N = V_{o}. The voltage gain of the N-phase rccBuck converter is

\[
\frac{V_{o}}{V_{in}}_{\text{N-phase,rccBuck}} = \frac{D}{N + D} \quad (0 \leq D \leq 1, N \geq 2) \tag{2-4}
\]

According to (2-4), the maximum V_{o} decreases with N. The multi-phase configuration is suitable for low-voltage and high-current applications. The voltage stress of the active switches is 2(V_{in} - V_{o}), same as two-phase rccBuck converter. This dissertation only focuses on a two-phase rccBuck converter. The one-turn inductor design in Chapter 3 could be extended to multi-phase rccBuck converters. However, the steady-state modeling in this chapter, the small-signal modeling in Chapter 5, and the Omni-coupled inductors design in Chapter 4, are only available for a two-phase rccBuck converter at this point.
2.2 Steady-State Modeling under Continuous Voltage Mode (CVM)

The rccBuck converter in Fig. 2-1(b) is a fourth-order circuit when $M_{1a, 2b}$ turns on and $M_{2a, 1b}$ turns off, and it changes to a second-order circuit when $M_{1a, 1b}$ turns off and $M_{2a, 2b}$ turns on. The state-plane trajectory is an effective method to analyze resonant converters, but it requires resonant tanks no higher than second order [84]–[85]. The transfer-characteristics curve is a useful tool to analyze the resonant converter with high-order tanks, but these tanks are required to be invariant and connect to a half bridge or full bridge [86]–[87]. Modeling the steady state of the rccBuck converter with a hybrid fourth-order and second-order tank is then challenging.

A state-space representation that can give an exact steady-state solution numerically [88], is a fundamental tool for circuit simulation, but it is difficult to give physical meaning to high-order systems. Decomposition of high-order circuit modes into basic second-order resonant modes makes it possible to obtain a geometrical representation for the steady-state response [89]. Both methods are used in this section to understand the operating principles of an rccBuck converter, and to derive its characteristic curves.

The inductance $L_{ra} = L_{rb} = L_r$ (Fig. 2-1(b)), capacitance $C_{ra} = C_{rb} = C_r$ (Fig. 2-1(b)), inductance ratio $L_m = L_o/L_r$, and duty ratio $D = 2(t_2 - t_1)/f_s$ (Fig. 2-7) are defined in the steady-state analysis. The normalized frequency $f_n$ is defined from the switching frequency $f_s$ and the resonant frequency $f_r$ of $L_r$ and $C_r$ according to

$$f_n = f_r/f_s = \frac{\omega_r}{(2\pi f_s)} = \frac{1}{(2\pi f_s \sqrt{L_r C_r})}$$

(2-5)

The base frequency selects $f_s$ here since $f_s$ is fixed in an rccBuck converter, and the $f_r$ is the studied object in steady-state design. In resonant converters such as parallel-resonant converter (PRC) and LLC converter in [90]–[91], the studied object is the switching-frequency range as the load or gain.
varies; thus, the $f_n$ is defined as $f_n = f_s/f_r$ for convenience.

\[
Z_n = \frac{Z_r}{V_{in}/(I_{omax} + I_{CossZVS})} = \frac{\sqrt{L_r/C_r}}{V_{in}/(I_{omax} + I_{CossZVS})}
\]  

(2-6)

where $I_{omax}$ is the rated current below which ZVS is feasible, and $I_{CossZVS}$ is the current to discharge the $C_{oss}$ for ZVS.

Fig. 2-7. Simulated (a) waveforms and (b) corresponding switched stages of rccBuck converter operating under CVM with $f_n = 0.6$, $L_n = 1$, and $Z_n = 1.8$. 

The normalized impedance of $L_r$ and $C_r$ is defined as
2.2.1 Analysis of Switched Stages

Let [0, 1, 1, 0] represent the switch states with M\(_{1a}\) (an active switch) off, M\(_{2a}\) (a synchronous switch) on, M\(_{1b}\) on, and M\(_{2b}\) off, respectively. The rcc-Buck converter cycles from [0, 1, 1, 0] to [0, 1, 0, 0] to [0, 0, 1, 0] to [1, 0, 0, 1] to [0, 1, 0, 1] to [0, 1, 0, 0] to [0, 1, 1, 0] in each switching period. The first four switch states generate the switched circuits in Fig. 2-8–Fig. 2-13 in one half of a switching period. The other switch states create the same waveforms, but in opposite phases. The purpose of this sub-section is to analyze the resonant circuit in each interval, derive the closed-form formulas of the key state variables, study the requirement for ZVS realization, and calculate the minimum turn-off current of the synchronous MOSFET.

The switched circuit during \(t_1 - t_2\) is illustrated in Fig. 2-8(a). The Active MOSFET M\(_{1b}\) is turned on with zero voltage at \(t_1\); M\(_{2a}\) is on and M\(_{1a, 2b}\) are off in this interval. The current \(i_{d2a} (= i_{Loa} + i_{Lob} - i_{Lra} - i_{Lrb})\) and \(i_{d1b} (= i_{Lob} - i_{Lra})\) are dependent on inductor current; the voltage \(v_{ds1a} (= v_{Cra} + v_{Crb})\) and \(v_{ds2b} (= v_{Crb})\) are dependent on capacitor voltages. The state variables, \(i_{Lr}, i_{Lo},\) and \(v_{Cr},\) are analyzed by using the simplified resonant converter in Fig. 2-8(b) with the assumption of negligibly large \(C_o\) and constant \(V_o.\) The output inductor \(L_{oa}\) is linearly discharged by \(V_o;\) other capacitors and inductors comprise a fourth-order resonant circuit.

![Diagram](image.png)

Fig. 2-8. (a) Circuit during interval \((t_1 - t_2)\) defined in Fig. 2-7 and (b) corresponding simplified schematic.
The complete time response of each state variable is the sum of zero-input response and zero-state response. The zero-input response relies on the initial condition of each component and ignores input sources. The zero-state response relies only on the circuit structure, including sources and components, and ignores initial conditions.

The differential equations that describe Fig. 2-8(b) are

\[
\frac{d i_{Lra}}{dt} = -\frac{1}{L_r} v_{Cra} - \frac{1}{L_r} v_{Crb} + \frac{1}{L_r} V_{in} \quad (2-7)
\]

\[
\frac{d i_{Lrb}}{dt} = -\frac{1}{L_r} v_{Crb} + \frac{1}{L_r} V_{in} \quad (2-8)
\]

\[
\frac{d i_{lob}}{dt} = \frac{1}{L_r L_n} v_{Crb} - \frac{1}{L_r L_n} V_{o} \quad (2-9)
\]

\[
\frac{dv_{Cra}}{dt} = \frac{1}{C_r} i_{Lra} \quad (2-10)
\]

\[
\frac{dv_{Crb}}{dt} = \frac{1}{C_r} i_{Lra} + \frac{1}{C_r} i_{Lrb} - \frac{1}{C_r} i_{lob} \quad (2-11)
\]

The corresponding matrices are

\[
\dot{x} = A_{12} x + B_{12} U \quad (2-12)
\]

\[
x = \begin{bmatrix} i_{Lra} \\ i_{Lrb} \\ i_{lob} \\ v_{Cra} \\ v_{Crb} \end{bmatrix}, \quad A_{12} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_r} & -\frac{1}{L_r} \\ 0 & 0 & 0 & 0 & -\frac{1}{L_r} \\ 0 & 0 & 0 & \frac{1}{L_r L_n} & 0 \\ \frac{1}{C_r} & 0 & 0 & 0 & 0 \\ \frac{1}{C_r} & \frac{1}{C_r} & -\frac{1}{C_r} & 0 & 0 \end{bmatrix}, \quad B_{12} = \begin{bmatrix} 1 \\ \frac{1}{L_r} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad U = \begin{bmatrix} V_{in} \\ V_{o} \end{bmatrix} \quad (2-13)
\]

The S-domain zero-state response of \( x \) during (\( t_1 \)–\( t_2 \)) is solved by Laplace transform of (2-12)

\[
x_{zs} = (SI_{5 \times 5} - A_{12})^{-1} \frac{B_{12} U}{S} \quad (2-14)
\]

\( I_{5 \times 5} \) is a 5 × 5 unit matrix
The zero-state responses of $i_{Lra}$ and $v_{Cra}$ are simplified as

$$
i_{Lra, zs} (s) = x_{zs} (1) = \frac{V_{in s^2} + (V_{in} - V_o)}{L_r} \frac{C_r L_r L_n}{s^4 + (3L_n + 1)} + \frac{L_n + 1}{L_n L_r C_r} = \frac{1}{L_r} \frac{V_{in s^2} + \omega_r^2 (V_{in} - V_o)}{s^4 + (\omega_r^2 + \omega_1^2)(s^2 + \omega_2^2)}$$

$$
v_{Cra, zs} (s) = x_{zs} (4) = \frac{V_{in s^2} + \frac{V_{in} - V_o}{L C}}{s^4 + \omega_1^2 s (s^2 + \omega_2^2)}$$

$$
= \frac{(V_{in} - V_o) \omega_1^4}{L_n \omega_1^2 \omega_2^2} \frac{1}{s} + \frac{(V_{in} - V_o) \omega_1^4 - L_n V_{in} \omega_1^2 \omega_2^2}{L_n \omega_1^2 (\omega_1^2 - \omega_2^2)} \frac{s}{s^2 + \omega_1^2} + \frac{L_n V_{in} \omega_1^2 \omega_2^2 - (V_{in} - V_o) \omega_1^4}{L_n \omega_1^2 (\omega_1^2 - \omega_2^2)} \frac{s}{s^2 + \omega_2^2}
$$

$$
\frac{\omega_1}{\omega_r} = \sqrt{\frac{3L_n + 1 + \sqrt{5L_n^2 + 2L_n + 1}}{2L_n}} \quad \text{and} \quad \frac{\omega_2}{\omega_r} = \sqrt{\frac{3L_n + 1 - \sqrt{5L_n^2 + 2L_n + 1}}{2L_n}}
$$

Corresponding time-domain zero-state responses of $i_{Lra}$ and $v_{Cra}$ are

$$
i_{Lra, zs} = \frac{L_n \omega_1^2 V_{in} - \omega_1^2 (V_{in} - V_o)}{L_n L (\omega_1^2 - \omega_2^2) \omega_1} \sin(\omega_1 t) + \frac{\omega_r^2 (V_{in} - V_o) - L_n V_{in} \omega_1^2 \omega_2}{L_n L (\omega_1^2 - \omega_2^2) \omega_2} \sin(\omega_2 t)
$$

$$
v_{Cra, zs} = \frac{(V_{in} - V_o) \omega_1^4}{L_n \omega_1^2 \omega_2^2} \frac{1}{s} + \frac{(V_{in} - V_o) \omega_1^4 - L_n V_{in} \omega_1^2 \omega_2^2}{L_n \omega_1^2 (\omega_1^2 - \omega_2^2)} \cos(\omega_1 t) + \frac{L_n V_{in} \omega_1^2 \omega_2^2 - (V_{in} - V_o) \omega_1^4}{L_n \omega_1^2 (\omega_1^2 - \omega_2^2)} \cos(\omega_2 t)
$$

In the analysis of zero-input responses, $V_{in}$ and $V_o$ are set to 0, and initial conditions of $x$ are considered. The S-domain zero-input response of $x$ during (t1–t2) is

$$
x_{zt} = (SI_{5x5} - A_{12})^{-1} x_0
$$

$$
X_0 = [I_{Lra \oplus t_1} \ I_{Lrb \oplus t_1} \ I_{Lab \oplus t_1} \ V_{Cra \oplus t_1} \ V_{Crb \oplus t_1}]^{-1}
$$

The S-domain zero-input responses of $i_{Lra}$ and $v_{Cra}$ are simplified as

$$
i_{Lra, zt} (s) = x_{zt} (1) = \frac{k_{a1} + k_{a2} s}{s^2 + \omega_1^2} + \frac{k_{a3} + k_{a4} s}{s^2 + \omega_2^2}
$$

$$
v_{Cra, zt} (s) = x_{zt} (4) = \frac{k_{b1} + k_{b2} s}{s^2 + \omega_1^2} + \frac{k_{b3} + k_{b4} s}{s^2 + \omega_2^2}
$$

55
Through observations and proper simplifications, the time-domain zero-input responses for $i_{Lra}$ and $v_{Cra}$ are

$$i_{Lra,zi} = \frac{k_{a1}}{\omega_1} \sin(\omega_1 t) + \frac{k_{a2}}{\omega_2} \cos(\omega_2 t) + \frac{k_{a3}}{\omega_3} \sin(\omega_3 t) + \frac{k_{a4}}{\omega_4} \cos(\omega_4 t)$$

$$v_{Cra,zi} = \frac{k_{b1}}{\omega_1} \sin(\omega_1 t) + \frac{k_{b2}}{\omega_2} \cos(\omega_2 t) + \frac{k_{b3}}{\omega_3} \sin(\omega_3 t) + \frac{k_{b4}}{\omega_4} \cos(\omega_4 t)$$

Notice that the coefficients for the $\sin(\omega_1 t)$ of $i_{Lra,zi}$ in (2-19) and the $\cos(\omega_1 t)$ of $v_{Cra,zi}$ in (2-19) have the common term $\frac{L_n \omega_1^2 V_{in}}{L_n(\omega_1^2 - \omega_2^2)}$. Through observations and proper simplifications, $i_{Lra}$ and $v_{Cra}$ could be decomposed to two second-order resonant modes by

$$i_{Lra} = \frac{\omega_r V_{in}}{\omega_1 Z_r} i_{Lra,s1} + \frac{\omega_r V_{in}}{\omega_2 Z_r} i_{Lra,s2}$$

$$v_{Cra} = \frac{(V_{in} - V_o) \omega_r^4}{L_n \omega_1^2 \omega_2^2} - \frac{V_{in} \omega_r^2}{\omega_1^2} v_{Cra,s1} - \frac{V_{in} \omega_r^2}{\omega_2^2} v_{Cra,s2}$$

$$i_{Lra,s1} = A_1 \sin(\omega_1 t + \theta_1), \quad i_{Lra,s2} = A_2 \sin(\omega_2 t + \theta_2)$$

$$v_{Cra,s1} = A_1 \cos(\omega_1 t + \theta_1), \quad v_{Cra,s2} = A_2 \cos(\omega_2 t + \theta_2)$$

$$A_1 = \sqrt{i_{Lra,s1}^2 + V_{Cra,s1}^2} \quad A_2 = \sqrt{i_{Lra,s2}^2 + V_{Cra,s2}^2}$$
\[
\theta_1 = \arctan \frac{I_{Lra,s1}@t1}{V_{Cra,s1}@t1}, \quad \theta_2 = \arctan \frac{I_{Lra,s2}@t1}{V_{Cra,s2}@t1}
\]

\[
\begin{bmatrix}
I_{Lra,s1}@t1 \\
I_{Lra,s2}@t1
\end{bmatrix} = \begin{bmatrix}
\omega_r V_{in} \\
\omega_r V_{in}
\end{bmatrix} \left[ \frac{k_{a2}\omega_2 Z_r}{\omega_2 - \omega_2^2} - \frac{\omega_r^2}{\omega_r^2 - \omega_2^2} \left( \frac{\omega_2^2}{\omega_r^2} - 1 \right) \frac{\omega_1}{\omega_r} - \frac{\omega_1}{\omega_r} \right] \frac{I_{Lra}@t1 Z_r}{V_{in}} + \frac{I_{Lra}@t1 Z_r}{V_{in}}
\end{bmatrix}
\]

\[
\begin{bmatrix}
V_{Cra,s1}@t1 \\
V_{Cra,s2}@t1
\end{bmatrix} = \begin{bmatrix}
\omega_r^2 \left( \frac{\omega_2}{\omega_r} - \frac{1}{L_n} \right) \frac{V_{Cra}@t1}{V_{in}} - \left( \frac{\omega_1^2}{\omega_r^2} - \frac{1}{L_n} \right) \frac{V_{Cra}@t1}{V_{in}} \\
\omega_r^2 \left( \frac{1}{L_n} \right) \frac{V_{Cra}@t1}{V_{in}} - \left( \frac{\omega_1^2}{\omega_r^2} + \frac{1}{L_n} \right) \frac{V_{Cra}@t1}{V_{in}}
\end{bmatrix}
\]

where \(I_{Lra}@t1, I_{Lrb}@t1, I_{Lob}@t1, V_{Cra}@t1, \) and \(V_{Crb}@t1\) are \(i_{Lra}, i_{Lrb}, i_{Lob}, v_{Cra}, \) and \(v_{Crb}\) at \(t_1\), respectively.

The base variables \((i_{Lra,s1}, v_{Cra,s1})\) and \((i_{Lra,s2}, v_{Cra,s2})\) are circulating with angular frequencies of \(\omega_1\) and \(\omega_2\), respectively. The initial current of \(i_{Lra,s1}\) and \(i_{Lra,s2}\) depends on \(I_{Lra}@t1\) and \((I_{Lob}@t1 - I_{Lrb}@t1)\), and the initial voltages of \(v_{Cra,s1}\) and \(v_{Cra,s2}\) depend on \(V_{Cra}@t1, V_{Crb}@t1, V_{in}, \) and \(V_o\). The amplitude \(A_{1,2}\) and angle \(\theta_{1,2}\) depend on initial conditions of state variables in Fig. 2-8(b). Other state variables, \(i_{Lrb} = I_{Lrb}@t1 + \frac{1}{L_r} \int (L_r \frac{dv_{Cra}}{dt} + v_{Cra}) \, dt, v_{Crb} = V_{in} - L_r \frac{dv_{Cra}}{dt} - v_{Cra}, \) and \(i_{Lob} = I_{Lob}@t1 + \frac{1}{L_r} \int (v_{Crb} - V_o) \, dt)\) could be derived, with \(i_{Lra}\) and \(v_{Cra}\) replaced by (2-27) and (2-28). The \(v_{Crb}@t2 > 0\) should be satisfied; otherwise, the converter operates at discontinuous voltage mode (Section 2.3).

The initial condition \(X_0\) is calculated in Sub-section 2.2.2. The steady-state solution is then obtained by cascading switched-stage solutions. For example, \(X_0\) is the initial condition of stage 1; the solution of stage 1 is the initial condition of stage 2, and so on.

As \(L_n\) decreases to zero, the \(\omega_1/\omega_r\) converges to infinite and \(\omega_2/\omega_r\) converges to 1, as shown in Fig. 2-9. Both \(i_{Lra}\) and \(v_{Cra}\) are dominated by the mode of \(\omega_2\) since the coefficients in (2-27) and
(2-28) are inversely proportional to $\omega_{1,2}$ and $\omega_{1,2}^2$, respectively. As $L_n$ increases to infinite, $\omega_1/\omega_r = \sqrt{(3 + \sqrt{5})/2} \approx 1.62$ and $\omega_2/\omega_r = \sqrt{(3 - \sqrt{5})/2} \approx 0.62$. All state variables have harmonics when $L_n \geq 0.5$ since $\omega_1/\omega_2 \approx 2.6$ (Fig. 2-9). The harmonics may lower the slope of $i_{Lra}$ near the valley, and that of $i_{Lob}$ near the peak, as shown in Fig. 2-7, reducing the turn-off current of $M_{1b} (= i_{Lob} - i_{Lra})$ at $t_2$.

![Graph](image.png)

**Fig. 2-9.** Normalized angular frequency, $\omega_{1,2}/\omega_r$, versus inductance ratio $L_n$ in (2-17).

The interval $t_2 - t_3$ (“dead time” in Fig. 2-7) is reserved for the ZVS turn-on of the synchronous MOSET, $M_{2b}$. The active MOSFET $M_{1b}$ is hard turned off at $t_2$. The turn-off voltage, $V_{ds1b} = V_{Crb}$, is lower than that of the conventional buck converter, $V_{in}$. The low turn-off current and voltage of $M_{1b}$ contribute to the low turn-off loss. The inductor current $i_{Lrb}$ flows into $swa$ after $M_{1b}$ is turned off, as shown in Fig. 2-10(a). The high current $(i_{Lob} - i_{Lra})$ discharges $C_{oss} (= C_{oss,M1a} + C_{oss,M1b} + C_{oss,M2b})$ in Fig. 2-10(b) with a short time, thanks to high $i_{Lob}$ and low $i_{Lra}$ at $t_2$ as illustrated in Fig. 2-7. Moreover, the voltage across $C_{oss}$ at $t_2$ is the valley of $v_{Crb}$, easing the ZVS of $M_{2b}$. 
Fig. 2-10. (a) Circuit during interval \((t_2 - t_3)\) defined in Fig. 2-7 and (b) corresponding simplified schematic.

The synchronous MOSFET, \(M_{2b}\), is ZVS turned on at \(t_3\). The load current is disconnected with the input source as illustrated in Fig. 2-11(a). A higher ratio of \((t_2 - t_1)/(t_4 - t_3)\) leads to a higher \(V_o\). The inductors \(L_{ra}, rb\) and capacitors \(C_{ra}, rb\) comprise two independent second-order resonant tanks as shown in Fig. 2-11(b).

Fig. 2-11. (a) Circuit during interval \((t_3 - t_4)\) defined in Fig. 2-7 and (b) corresponding simplified schematic.

The state variables of \(v_{Cra}, i_{Lra}, v_{Crb},\) and \(i_{Lrb}\) during \(t_3\) to \(t_4\) are sinusoidal and given by

\[
v_{Cra} = V_{in} + (V_{Cra@t_3} - V_{in}) \cos[\omega_r(t - t_3)] + I_{Lra@t_3}Z_r \sin[\omega_r(t - t_3)] \tag{2-35}
\]

\[
i_{Lra} = I_{Lra@t_3} \cos[\omega_r(t - t_3)] + \frac{V_{in} - V_{Cra@t_3}}{Z_r} \sin[\omega_r(t - t_3)] \tag{2-36}
\]

\[
v_{Crb} = V_{in} + (V_{Crb@t_3} - V_{in}) \cos[\omega_r(t - t_3)] + I_{Lrb@t_3}Z_r \sin[\omega_r(t - t_3)] \tag{2-37}
\]
\[ i_{Lrb} = I_{Lrb@t3} \cos[\omega_r(t - t_3)] + \frac{V_{in} - V_{Crb@t3}}{Z_r} \sin[\omega_r(t - t_3)] \]  

(2-38)

where \( I_{Lra@t3}, I_{Lrb@t3}, I_{Lob@t3}, V_{Cra@t3}, \) and \( V_{Crb@t3} \) are \( i_{Lra}, i_{Lrb}, i_{Lob}, v_{Cra}, \) and \( v_{Crb} \) at \( t_3 \), respectively.

Notice that \( V_{Crb@t3} \ll V_{in} \); thus \( i_{Lrb} \) increases quickly during \( t_3 - t_4 \), which is beneficial for the ZVS of \( M_{1a} \).

The output inductors \( L_{oa} \) and \( L_{ob} \) are discharged by \( V_0 \) with the linearly decreasing current of

\[ i_{Loa} = I_{Loa@t3} - \frac{V_0}{L_n L_r} (t - t_3) \]  

(2-39)

\[ i_{Lob} = I_{Lob@t3} - \frac{V_0}{L_n L_r} (t - t_3) \]  

(2-40)

The short \( t_2 - t_3 \) for ZVS transition is ignored in the steady-state verification in Fig. 2-12. The closed-form equations in (2-15)–(2-40) are validated by the numerical state-space model in Subsection 2.2.2.

The synchronous MOSFET, \( M_{2a} \), is turned off at \( t_4 \) with \( (I_{Loa@t4} - I_{Lrb@t4}) \). The current \( (i_{Lrb} - i_{Loa}) \) then discharges \( C_{oss} \) \( (= C_{oss,M1a} + C_{oss,M2a} + C_{oss,M1b}) \) during \( t_4 - t_5 \) as shown in Fig. 2-13(a). The equivalent circuit is shown in Fig. 2-13(b) and further simplified to the second-
order circuit in Fig. 2-14(a), as a result of $C_{oss} \ll C_r$. Next steps are to derive the $I_{CossZVS}$, $I_{off,M2a}$, and $t_{ZVS}$.

The voltage source $V_{eq}$ in Fig. 2-14(a) equals the $v_{Coss}$ after reaching the equilibrium state and solved by

$$V_{eq} = V_{Cra}@t_4 + \frac{L_n}{L_n + 1} V_{Crb}@t_4 - \frac{L_n}{L_n + 1} V_{in} - \frac{1}{L_n + 1} V_o$$

(2-41)

The state variables $i_{Leq} (i_{Loa} - i_{Lrb})$ and $v_{Coss}$ follow the state trajectories in Fig. 2-14(b) when $2V_{eq} > V_{Cra}@t_4$, and in Fig. 2-14(c) when $2V_{eq} \leq V_{Cra}@t_4$. The extra current for discharging $C_{oss}$ considered in (2-6) is approximated by

$$I_{CossZVS} = \frac{2V_{eq} V_{in}}{Z_{eq}(V_{in} - V_o)} = \frac{2V_{eq} V_{in}}{(V_{in} - V_o)} \sqrt{\frac{C_{oss}}{L_{rb} / / L_{oa}}} \approx \frac{2.6V_{in}^2}{(V_{in} - V_o)} \sqrt{\frac{C_{oss}}{L_{rb} / / L_{oa}}}$$

(2-42)

The approximation of $I_{CossZVS}$ at the last step of (2-42) is valid since $V_{eq}$ can be simplified conservatively as $1.3V_{in}$ for $0.5 < L_n < 2$ from the numerical calculation.

The active MOSFET $M_{1a}$ is ZVS turned on at $t_5$. If ZVS can be realized at rated load, it is also feasible at lighter load since $i_{Lrb} \geq i_{Loa} + I_{CossZVS}$ at $t_4$ is always true. The body diode of $M_{2a}$ is always off within the load range ($0 \text{ A} - I_{oMax}$), eliminating the losses associated with reverse recovery.
The required turn-off current $I_{\text{off,M2a}}$ is $\sqrt{V_{\text{Cra@t4}}(2V_{\text{eq}} - V_{\text{Cra@t4}})/Z_{\text{eq}}}$ for $2V_{\text{eq}} > V_{\text{Cra@t4}}$ (Fig. 2-14(b)) and 0 for $2V_{\text{eq}} \leq V_{\text{Cra@t4}}$ (Fig. 2-14(c)). The triangular regions, on behalf of $2V_{\text{eq}} \leq V_{\text{Cra@t4}}$, are surrounded by three lines in Fig. 2-15. The upper line represents BVM, the same as Fig. 2-20. The right line represents maximum voltage gain at the maximum D. The left line satisfies $2V_{\text{eq}} = V_{\text{Cra@t4}}$. The converter with higher $L_n$, higher $f_n$, and higher $V_o/V_{\text{in}}$ is easier to realize zero-current switching (ZCS) of $M_{2a}$.

![Diagram](image)

Fig. 2-14. (a) Equivalent circuit of Fig. 2-13 by assuming $C_r \gg C_{\text{oss}}$ and corresponding state planes with (b) $2V_{\text{eq}} > V_{\text{Cra@t4}}$ and (c) $2V_{\text{eq}} \leq V_{\text{Cra@t4}}$.

The time to realize ZVS is

$$t_{ZVS} = t_5 - t_4 = 2\pi \sqrt{(L_{rb}/L_{oa})C_{\text{oss}}} \left(1 + \arctan \frac{V_{\text{Cra@t4}} - V_{\text{eq}}}{V_{\text{eq}}} \right) \approx \pi \sqrt{(L_{rb}/L_{oa})C_{\text{oss}}} \quad (2-43)$$

The approximation of (2-43) at the last step is available since the angles of the arcs in Fig. 2-14(b) and (c) are always smaller than $180^\circ$. The $t_{ZVS} < D/(2f_s)$ should be satisfied to have regulation.
Fig. 2-15. Normalized resonant frequency \( f_n \) versus \( V_o/V_{in} \) with \( 2V_{eq} \leq V_{Cra@t4} \) at CVM.

The impact of \( C_{oss} \) on the inductor current and turn-off current is shown in Fig. 2-16. When \( C_{oss} = 0 \), the \( i_{Lra} \) and \( i_{Lob} \) have no overlap, and \( M_{2a} \) is turned off at zero current. When \( C_{oss} = 1 \) nF, an overlapped, \( I_{CossZVS}/2 \), is required for \( i_{Lra} \) and \( i_{Lob} \). The turn-off current of \( M_{2a} \) is \( I_{off,M2a} > 0 \) in Fig. 2-16(b) and \( I_{off,M2a} = 0 \) in Fig. 2-16(c). The Fig. 2-16(b) corresponds to the regions with \( 2V_{eq} > V_{Cra@t4} \), and Fig. 2-16(c) corresponds to the regions with \( 2V_{eq} \leq V_{Cra@t4} \); however, the turn-off current of \( M_{2a} \) is negligible compared with the load current. Moreover, the ZCS or near-ZCS condition of \( M_{2a} \) is only available at rated load. The turn-off current of \( M_{2a} \) at 25% load is much higher than that at the rated load, and is independent of \( C_{oss} \), as shown in Fig. 2-16(d)–(f). Thus, the ZCS or near-ZCS of \( M_{2a} \) is not emphasized in later analysis.

The impacts of \( C_{oss} \) on \( I_{CossZVS} \) and \( tZVS \) are shown in Fig. 2-17. The \( I_{CossZVS} \) is dependent on \( V_{in} \) and \( V_o \) since \( (L_d/L_o) I^2_{CossZVS} \) offers the energy to discharge the drain-to-source voltage of \( M_{1a} \), while the simplified \( tZVS \) in (2-43) is almost independent of \( V_{in} \) and \( V_o \) since the time constant of \( C_{oss} \) and \( L_d/L_o \) is independent of \( V_{in} \) and \( V_o \). Higher \( L_d/L_o \) corresponds to smaller \( I_{CossZVS} \) because \( (L_d/L_o) I^2_{CossZVS} \approx C_{oss} V_{eq}^2 \) is almost constant. Higher \( L_d/L_o \) corresponds to higher \( tZVS \) because of a larger time constant.
Fig. 2-16. Simulated waveforms of inductor and MOSFET currents in rccBuck converters with (a) $V_o = 3.3$ V, $I_o = 20$ A, $f_n = 0.6$, $Z_n = 2.5$, and $C_{oss} = 0$, (b) $V_o = 3.4$ V, $I_o = 20$ A, $f_n = 0.6$, $Z_n = 1.9$, and $C_{oss} = 1$ nF, and (c) $V_o = 3.8$ V, $I_o = 20$ A, $f_n = 0.65$, $Z_n = 2.3$, and $C_{oss} = 1$ nF. All converters have the same $V_{in} = 12$ V, $f_s = 2$ MHz, and $L_o = 1$. (d), (e), and (f) are corresponding waveforms of (a), (b), and (c) at 25% load.

Fig. 2-17. Calculated (a) $I_{CossZVS}$ by (2-42) and (b) $t_{ZVS}$ by (2-43) for rccBuck converter with $V_{in} = 12$ V.

2.2.2 State-Space Model of CVM rccBuck Converter

The objective of a state-space model is to calculate time-domain waveforms of the state-
variable vector

\[ \mathbf{x} = [i_{Lra}, i_{Lrb}, i_{Loa}, i_{Lob}, v_{Cra}, v_{Crb}, v_{Co}]^T \]  

(2-44)

The output capacitance \( C_{\text{oss}} \) in Fig. 2-13 is set to 0 so that \( t_3 - t_2 = t_5 - t_4 = 0 \) in Fig. 2-7.

![Circuit Diagram](image)

Fig. 2-18. Circuits during intervals (a) \( t_1 - t_2 \) and (b) \( t_3 - t_4 \) defined in Fig. 2-7.

The differential equations that represent the switched stages in Fig. 2-8(a) and Fig. 2-11(a) are

\[ \dot{x} = A_1 \mathbf{x} + B \mathbf{u} \]  
\[ \dot{\mathbf{x}} = A_2 \mathbf{x} + B \mathbf{u} \]

respectively, where

\[ A_1 = \begin{bmatrix} 0_{4 \times 4} & L_{\text{mat}}^{-1} v_{L1} \\ \frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_r} & \frac{1}{C_r} & 0 & -1 & \frac{1}{C_r} & 0 & 0 \\ 0 & \frac{1}{C_o} & \frac{1}{C_o} & 0 & 0 & 0 & 0 \end{bmatrix}, \quad A_2 = \begin{bmatrix} 0_{4 \times 4} & L_{\text{mat}}^{-1} v_{L2} \\ \frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & \frac{1}{C_o} & 0 & 0 & 0 \end{bmatrix} \]

\[ B = \begin{bmatrix} L_{\text{mat}} v_{LVin} \\ 0_{4 \times 1} \end{bmatrix} \]

(2-45)

\[ L_{\text{mat}} = \begin{bmatrix} L_r & 0 & 0 & 0 \\ 0 & L_r & 0 & 0 \\ 0 & 0 & L_o & 0 \\ 0 & 0 & 0 & L_o \end{bmatrix}, \quad v_{L1} = \begin{bmatrix} -1 & -1 & 0 \\ -1 & 0 & -1 \\ 0 & 0 & -1 \end{bmatrix}, \quad v_{L2} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix}, \quad v_{LVin} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \]

(2-46)

The corresponding transition matrixes are \( \Phi_1(t) = e^{A_1(t-t_1)} \) and \( \Phi_2(t) = e^{A_2(t-t_2)} \). Since the two phases are symmetric, the initial condition of \( \mathbf{x} \) (at \( t_1 \)) is given by

\[ X_0 = [P - \Phi_2(t_4)\Phi_1(t_2)]^{-1}[\Phi_2(t_4)\Omega_1(t_2) + \Omega_2(t_4)] \]  

(2-47)

\[ \Omega_1(t) = \int_0^{t-t_1} e^{A_1(t-t_1-\tau)} B \mathbf{u} d\tau, \quad \Omega_2(t) = \int_0^{t-t_2} e^{A_2(t-t_2-\tau)} B \mathbf{u} d\tau \]  

(2-48)
The time-domain state-variable vector is

\[
P = \begin{bmatrix}
0 & 1 & 0 & 0 & 0 & 0 & 0
1 & 0 & 0 & 0 & 0 & 0 & 0
0 & 0 & 0 & 1 & 0 & 0 & 0
0 & 0 & 1 & 0 & 0 & 0 & 0
0 & 0 & 0 & 0 & 0 & 1 & 0
0 & 0 & 0 & 0 & 1 & 0 & 0
0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\]  

(2-49)

\[x = \Phi_1(t)X_0 + \Omega_1(t) \quad (t_1 \leq D \leq t_2)\]  

(2-50)

\[x = \Phi_2(t)x(t_2) + \Omega_2(t) \quad (t_3 \leq D \leq t_4)\]

Notice that \(v_{C_{rb}@t_2} > 0\) should be satisfied, otherwise the converter operates in discontinuous voltage mode (DVM). The state-space model of DVM is introduced in Section 2.3.

### 2.2.3 Required Conditions for CVM Operation

The rccBuck converter operates at continuous voltage mode (CVM) when \(C_r\) has a continuous steady-state voltage with the corresponding waveforms shown in Fig. 2-7, and at DVM when \(C_r\) has a discontinuous steady-state voltage with the corresponding waveforms shown in Fig. 2-31. The discontinuous capacitor voltage is caused by the clamping effect of the body diodes of half-bridge MOSFETs, when significant resonance exists, and the capacitor voltage drops to zero. The boundary voltage mode (BVM) is defined as the boundary of them, where the capacitor-voltage valley can just touch zero. This sub-section derives the BVM curves first, and then discusses the requirement for CVM.

Two constraints are met in the calculation of BVM in Fig. 2-20(a). The valley of \(i_{L_{rb}}\) equals the peak of \(i_{L_{rb}}\), so \(M_{1a}\) is turned on with zero voltage, and \(M_{2a}\) is turned off with zero current. The capacitor voltage \(v_{C_{rb}}\) drops to zero at \(t_2\), and is higher than zero at other times of the cycle. There is a unique pair of \(f_n\) and \(Z_n\) to meet these constraints for the given \(D\) and \(L_n\).

The BVM curve in Fig. 2-20(a) was calculated following the procedure in Fig. 2-19. The
innermost loop is sweeping $Z_n$. For a given $V_{in}$, $I_o$, $L_n$, and $f_n$, $Z_n$ is adjusted to satisfy ZVS, i.e., the valley of $i_{Lob}$ equals the peak of $i_{Lra}$. The medium loop is sweeping $f_n$ to ensure the valley of $v_{Cra}$ can just touch zero. The outermost loop is sweeping $D$, corresponding to the voltage gain, the x-axis of Fig. 2-20(a).

The BVM curve is extended for more $L_n$ in Fig. 2-20(b). The normalized resonant frequency $f_n$ decreases with $V_o/V_{in}$ since high $V_o/V_{in}$ requires a large $D$, long interval of $(t_2 - t_1)$, and long resonant period of $L_r$ and $C_r$. Higher $L_n$ corresponds to a higher $L_o$, and needs lower $L_r$ to maintain...
ZVS of the active MOSFETs. When $L_n$ is negligibly large, e.g., $L_n = 10$, most current ripple for ZVS is contributed from $L_r$, and $f_n$ is then independent of $L_n$. All curves in Fig. 2-20(b) converge to $f_n = 1$ as $V_o/V_{in}$ decreases to 0. The reason is as $D$ shrinks, the second-order mode during $(t_3 - t_4)$ is dominant, and $f_n$ needs to be close to $f_r$ to meet the BVM constraints.

![Diagram](image)

Fig. 2-20. (a) Definition of CVM, BVM, and DVM; (b) normalized resonant frequency, $f_n$, versus $V_o/V_{in}$ with $M_{1a,1b}$ turned on at zero voltage and $M_{2a,2b}$ turned off at zero current, parametric with respect to inductance ratio, $L_n$.

The maximum $f_n$ is limited by the specified $V_o/V_{in}$ in the CVM region that is below the BVM curve, as shown in Fig. 2-20(a). Higher $L_n$ allows more choices of $f_n$ under CVM. Generally, for the active MOSFETs, the design close to the BVM has high voltage stress but low turn-off current, which is demonstrated in Section 2.5.1. Conversely, if $f_n$ is away from the BVM curve, e.g., $f_n = 0.1$, the converter would operate with linear waveforms and low voltage stresses, as well as a wide-range $V_o/V_{in}$ (from 0 to 0.33). The properties of rccBuck converter under CVM are depicted in Section 2.2.1.

2.2.4 Impedance and Stress Curves under CVM

The state-space model in Sub-section 2.2.2 was used in this sub-section to calculate the normalized impedance $Z_n$, voltage stress, RMS current of the MOSFET and inductors, turn-off
current of M_{1a,1b}, and duty ratio D versus voltage gain V_o/V_{in}, parametric with the inductance ratio L_n (= 0.5, 1, and 2). The L_n is usually designed in the range of 0.5 \leq L_n \leq 2 so that the current ripples of L_r and L_o are comparable. The L_n = 0.5, 1, and 2 are exemplary points. All cases are under CVM.

The curves of normalized impedance Z_n in Fig. 2-21 are used for calculating L_r and C_r by (2-5), (2-6), (2-33), and (2-34). A higher V_o/V_{in} and higher f_n (=f_i/f_s) need a higher Z_n, since L_{r,o} needs to increase for ZCS (or near ZCS) as the volt-second increases. Thus, one limitation of the high f_n is high inductance, usually related to higher losses or footprint. The maximum voltage gain also limits the selection of f_n, e.g., f_n = 0.7 is not valid for V_o/V_{in} = 0.25 at L_n = 2.

![Fig. 2-21. Normalized impedance Z_n versus V_o/V_{in} with (a) L_n = 2, (b) L_n = 1, and (c) L_n = 0.5 under CVM. Zero-voltage turn-on is guaranteed for M_{1a/b}, and zero-current turn-off is guaranteed for M_{2a/b}. Design points in Table 2-2 are marked by the symbol ⊗.](image)

Another limitation of high f_n is the voltage stress of the MOSFET as shown in Fig. 2-22. With a high f_n, voltage stresses would increase. Without the resonance, i.e., f_n is low, the voltage stresses of M_{1a,1b} and M_{2a,2b} are 2(V_{in} - V_o) and (V_{in} - V_o), respectively. If V_{in} = 12 V and V_o = 1.2 V, the voltage stress is \sim 22 V for M_{1a,1b} and \sim 11 V for M_{2a,2b}. If V_{in} = 12 V and V_o = 3.3 V, the voltage stress is \sim 18 V for M_{1a,1b} and \sim 9 V for M_{2a,2b}. The MOSFET with a 15-V voltage rating and low on resistance is available for the synchronous switch, while a 30-V or 25-V MOSFET is required for the active switch in those applications.
Fig. 2-22. Normalized MOSFET voltage stresses versus $V_o/V_{in}$ with (a) $L_n = 2$, (b) $L_n = 1$, and (c) $L_n = 0.5$ under CVM. Zero-voltage turn-on is guaranteed for $M_{1a/b}$, and zero-current turn-off is guaranteed for $M_{2a/b}$. Design points in Table 2-2 are marked by the symbol $\circ$. The operating conditions are the same as Fig. 2-21.

The RMS current for both active and synchronous MOSFETs is independent of $L_n$ and $f_n$, as illustrated in Fig. 2-23. This is because their current ripples are related to the sum of $i_{Lr}$ ripple and $i_{Lo}$ ripple, which relies only on $(I_o - I_{in})$, except in the case of extremely high $f_n$, e.g., 0.9. Similar to a buck converter, as the $V_o/V_{in}$ increases, the RMS current increases for the active MOSFET and decreases for the synchronous MOSFET.

The RMS current for $M_{1a,1b}$ at CVM and nominal load is

$$I_{M1,RMS} = \sqrt{\frac{V_o(V_{in} - V_o)}{3V_{in}^2}} I_o$$  (2-51)
The corresponding RMS current of \( M_{2a, 2b} \) at nominal load is

\[
I_{M2,RMS} = \sqrt{\frac{2V_{in}^3 - 5V_{in}^2 V_o + 3V_o^3}{6V_{in}^2 (V_{in} - 2V_o)}} I_o \tag{2-52}
\]

The total switch stress \( S \) and switch utilization \( U \), defined in [165], of the rccbuck converters and state-of-the-art buck converter in Fig. 1-9, are shown in Fig. 2-24. The voltage stress is 1.45 \( V_{in} \) for the synchronous switch and 1.25 \( V_{in} \) for the active switch in the hard-switched buck converter, considering the power-loop inductance and voltage overshoot. The rccBuck converters achieve ZVS and almost zero voltage overshoot (Fig. 1-28(a)); thus, the voltage stresses in Fig. 2-22 without voltage spike effect are utilized to calculate \( S \) and \( U \). The switch utilizations of the rccBuck converters and buck converter are similar, yielding their total conduction losses are similar if MOSFETs are optimized. Notice that the rccBuck converters have lower switching loss and lower noise, thanks to ZVS operation.

![Fig. 2-24. Total switch stresses S (defined in [165] and normalized by \( V_{in}I_o \)) and switch utilization U versus \( V_o/V_{in} \) for the rccBuck converters at (a) \( L_n = 2 \), (b) \( L_n = 1 \), and (c) \( L_n = 0.5 \) under CVM, compared with the state-of-the-art two-phase buck converter in Fig. 1-9. Zero-voltage turn-on is guaranteed for \( M_{1a/b} \) and zero-current turn-off is guaranteed for \( M_{2a/b} \). The operating conditions are the same as Fig. 2-21.](image)

The duty ratio \( D \) increases with \( V_o/V_{in} \) as shown in Fig. 2-25. Higher \( f_n \) gives higher \( D \), but not significantly. The voltage gain under CVM is \( V_o/V_{in} \approx D/(2 + D) \) with an error less than 10%.
at \(0.5 \leq L_n \leq 2\).

![Diagram](image)

**Fig. 2.25.** Normalized duty ratio \(D\) versus \(V_o/V_{in}\) with (a) \(L_n = 2\), (b) \(L_n = 1\), and (c) \(L_n = 0.5\) under CVM. Zero-voltage turn-on is guaranteed for \(M_{1a/b}\), and zero-current turn-off is guaranteed for \(M_{2a/b}\). Design points in Table 2-2 are marked by the symbol \(\odot\). The operating conditions are the same as Fig. 2-21.

The ac RMS currents of \(L_r\) and \(L_o\) depend on both \(L_n\) and \(f_n\), as illustrated in Fig. 2-26(a)–(c). Since the sum of \(i_{Lr}\) ripple and \(i_{Lo}\) ripple is almost fixed, the inductance ratio \(L_n\) controls the ac current sharing for \(L_r\) and \(L_o\). A higher \(L_n\) gives a lower \(L_r\) and a higher RMS current of \(L_r\). The peak-to-peak current of \(L_o\) is \(I_{ppLo} = (1 - D/2)V_o/(f_n L_r L_r)\). As \(f_n\) increases, \(L_r\) would increase, and \(I_{ppLo}\) decreases. Finally, the ac RMS current of \(L_r\) would increase.

The total RMS currents of \(L_r\) and \(L_o\) are shown in Fig. 2-26(d)–(f). The \(L_o\) has a constant RMS current since its dc current is dominant. The \(L_r\) has low dc current; thus, the total RMS current is similar to the ac RMS current. In high-frequency POL applications, the ac RMS current should be paid more attention since the ac resistance is much higher than the dc resistance, e.g., \(R_{ac} > 5R_{dc}\) at 2 MHz for one-turn gapped inductor in Chapter 3.
Fig. 2-26. Normalized inductor ac RMS current versus $V_o/V_{in}$ with (a) $L_n = 2$, (b) $L_n = 1$, and (c) $L_n = 0.5$ under CVM. (d), (e), and (f) are corresponding total RMS currents. Zero-voltage turn-on is guaranteed for $M_{1a/b}$, and zero-current turn-off is guaranteed for $M_{2a/b}$. Design points in Table 2-2 are marked by the symbol ◦. The operating conditions are the same as Fig. 2-21.

The synchronous MOSFET is turned-off with near ZCS, whereas the active MOSFET is hard turned off with the current $I_{M1off}$, as shown in Fig. 2-27. A higher $f_n$ leads to a lower $I_{M1off}$ since the drain-to-source current of $M_{1a, 1b}$ has harmonics, instead of a linear triangular waveform, as shown in Fig. 2-7. The reduction of $I_{M1off}$ is important for high-current applications. In particular, when ZVS is achieved for all MOSFETs, the turn-off loss is the only switching loss, which is demonstrated in Fig. 2-65.

To summarize, a high $f_n$ is beneficial for the ac RMS current of $L_o$ and the turn-off current of $M_{1a, 1b}$, with the sacrifice of increased voltage stresses and increased ac RMS current of $L_o$. A higher $L_n$ could reduce the ac RMS current of $L_o$ but increase that of $L_r$. The RMS current of the MOSFETs is independent of both $f_n$ and $L_n$. For a high-current application, e.g., $I_{oMax} = 20$ A, a
high \( f_n \) is preferred, since the turn-off loss is the main switching loss.

![Normalized turn-off current of M1a, 1b versus V_o/V_in with (a) \( L_n = 2 \), (b) \( L_n = 1 \), and (c) \( L_n = 0.5 \) under CVM. Zero-voltage turn-on is guaranteed for M1a, and zero-current turn-off is guaranteed for M2a/b. Design points in Table 2-2 are marked by the symbol ø. The operating conditions are the same as Fig. 2-21.](image)

2.2.5 MOSFET Current Comparison for Two-Phase ZVS Buck Converters and RccBuck Converter

The MOSFET RMS current of the rccBuck converter is compared to that of the two-phase QSW buck converter in Fig. 2-28(a) and the self-assisted ZVS buck converter in Fig. 2-28(b). They operate at a constant \( f_s \) and achieve ZVS for all switches within the entire load range. The operating principles and current waveforms of those two-phase ZVS converters have been introduced in Section 1.3.

![Fig. 2-28. (a) Two-phase quasi-square-wave (QSW) ZVS buck converter needs two inductors with high current ripples; (b) self-assisted ZVS buck converter needs only one inductor with high current ripple [46].](image)
The simulated RMS current of the active and synchronous switches for three cases is shown in Fig. 2-29. Two output conditions are considered: $V_o/V_{in} = 0.1$ and 0.275. The $L_n = 0.5$ and 1 are selected for $V_o/V_{in} = 0.1$ and 0.275, respectively, so that the ac RMS currents of $L_r$ and $L_o$ are comparable (Fig. 2-26(a)–(c)). The designs of $f_n = 0.7$ at $V_o/V_{in} = 0.1$ and $L_n = 0.5$, and $f_n = 0.6$ at $V_o/V_{in} = 0.275$ and $L_n = 1$, are close to the BVM lines in Fig. 2-20(b), having resonant inductor currents and capacitor voltages. The $f_n = 0.2$ that offers linear waveforms is also considered as a reference design to demonstrate the impact of $f_n$ on RMS currents. The self-assisted ZVS buck converter has the highest RMS current under all conditions, owing to the plateau current. The normal two-phase QSW buck converter has a similar RMS current as the rccBuck converter with a small $f_n$ at $V_o/V_{in} = 0.1$. The rccBuck converter with $f_n = 0.7$ has resonant waveforms and the lowest RMS current, especially at $V_o/V_{in} = 0.275$. As the $V_o$ increases, the assistance of input current is more significant, and the current ripple in the MOSFETs is lower.

The simulated current stresses, voltage stresses, and inductor counts of the hard-switched buck converter, the two-phase ZVS buck converters, and the rccBuck converter are compared in Table 2-1. The rccBuck converter has a lower voltage spike than the hard-switched buck converter, and a lower current stress than the two-phase ZVS buck converters. The advantages are more significant at a higher $V_o$, e.g., 3.3 V. The rccBuck converter employs more inductors than the hard-switched and ZVS converters, but the total magnetic volume can be minimized by the Omni-coupled inductors, as discussed in Chapter 4.
Fig. 2-29. Simulated RMS currents of (a) active switch and (b) synchronous switch at $V_o/V_{in} = 0.1$ for rccBuck converter and two-phase ZVS buck converters in Fig. 2-28; (c) and (d) are the RMS currents at $V_o/V_{in} = 0.275$.

Table 2-1. Normalized current and voltage stresses of the hard-switched and ZVS converters with the state-of-the-art layout ($L_{loop} = 0.15$ nH)

<table>
<thead>
<tr>
<th>$V_{in}$ = 12 V, $f_s$ = 2 MHz, and $I_o$ = 20 A</th>
<th>Hard-SW buck</th>
<th>Normal ZVS buck</th>
<th>Self-assisted ZVS buck</th>
<th>rccBuck $f_n = 0.7, L_n = 0.5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of L’s</td>
<td>$I_{dM1\text{-RMS}}$</td>
<td>$I_{dM2\text{-RMS}}$</td>
<td>Max. $V_{sw}$</td>
<td>$I_{dM1\text{-RMS}}$</td>
</tr>
<tr>
<td>----------------</td>
<td>-------------------</td>
<td>-------------------</td>
<td>-----------------</td>
<td>-------------------</td>
</tr>
<tr>
<td>$V_o = 1.2$ V</td>
<td>$I_{dM1\text{-RMS}}$</td>
<td>1 (3.2 A)</td>
<td>1.19</td>
<td>1.19</td>
</tr>
<tr>
<td></td>
<td>$I_{dM2\text{-RMS}}$</td>
<td>1 (9.5 A)</td>
<td>1.20</td>
<td>1.51</td>
</tr>
<tr>
<td></td>
<td>Max. $V_{sw}$</td>
<td>1 (17 V)</td>
<td>0.76</td>
<td>0.76</td>
</tr>
<tr>
<td>$V_o = 3.3$ V</td>
<td>$I_{dM1\text{-RMS}}$</td>
<td>1 (5.3 A)</td>
<td>1.13</td>
<td>1.21</td>
</tr>
<tr>
<td></td>
<td>$I_{dM2\text{-RMS}}$</td>
<td>1 (8.5 A)</td>
<td>1.15</td>
<td>1.35</td>
</tr>
<tr>
<td></td>
<td>Max. $V_{sw}$</td>
<td>1 (17 V)</td>
<td>0.76</td>
<td>0.76</td>
</tr>
</tbody>
</table>
The total switch stress $S$ and switch utilization $U$ of two-phase ZVS buck converters and rccBuck converter are shown in Fig. 2-32. All of them have negligible voltage spikes since ZVS is achieved. At $V_o/V_{in} = 0.1$, the $S$ and $U$ of the QSW-ZVS buck converter and rccBuck converter with $f_n = 0.2$ have similar $S$ and $U$. The rccBuck converter has lower current stresses but higher voltage stresses. As $V_o/V_{in}$ increases to 0.275, the voltage stresses and current stresses decrease in the rccBuck converter, leading to the highest $U$. As $f_n$ increases, the increase of voltage stress is more significant than that of current stress; thus, the $S$ increases and $U$ decreases with $f_n$.  

![Graphs showing total switch stresses and switch utilizations](image.png)

Fig. 2-30. Simulated (a) total switch stresses $S$ and (b) switch utilizations $U$ of rccBuck converter and two-phase ZVS buck converters in Fig. 2-28 at $V_o/V_{in} = 0.1$; (c) and (d) are the $S$ and $U$ at $V_o/V_{in} = 0.275$.  

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2.3 Steady-State Modeling under Discontinuous Voltage Mode (DVM)

When the \( f_n \) is designed above the boundary-voltage-mode (BVM) curve in Fig. 2-20(b), the rccBuck converter is operating at discontinuous voltage mode (DVM). This mode also exists for other topologies such as Cuk [92]–[93], buck [94], and buck-boost [95] converters. The advantages of DVM in those topologies include the inherent power factor correction (PFC) capability, zero turn-off voltage of the active switch, and zero turn-on current for the synchronous switch. In the rccBuck converter, the major benefits of the DVM are smaller turn-off current of active switches and improvement of light-load efficiency.

Fig. 2-31 shows the simulated switched voltages and current of a DVM rccBuck converter. The \((t_1–t_3)\) is a half switching cycle. The converter operates with the same waveforms during \((t_3–t_0)\), but in the opposite phase.

The challenges in designing a DVM rccBuck converter are as follows. (1) The synchronous-switch turn-on time \((t_1–t_2)\) is dependent on \(C_t\) and \(L_t\) in DVM and independent of them in CVM. The state-space model for the DVM is more difficult because of the variable \((t_1–t_2)\). The updated model is introduced in Sub-section 2.3.1. (2) The driving voltages of the active and synchronous switches need an overlap during \((t_2–t_3)\) in the DVM, which makes the control more complicated. That special interval is discussed in Sub-section 2.3.2. (3) The DVM has higher current and voltage stresses, as demonstrated in Sub-section 2.3.3. (4) The steep current drop of \(i_{d1b} \) at \(t_2\) may cause severe ringing if parasitic inductance exists at DVM. This phenomenon is not seen in the CVM condition. The modeling of this ringing, and solutions are introduced, in Sub-section 2.3.4.
Fig. 2-31. Simulated waveforms and corresponding switched states of rccBuck converter under DVM with $V_{in} = 12 \text{ V}$, $I_o = 20 \text{ A}$, $f_s = 2 \text{ MHz}$, $D = 0.8$, $C_o = 2\mu F$, $L_r = 140 \text{ nH}$, $C_r = 71 \text{ nF}$, $f_o = 0.8$, $L_n = 1$, and $Z_n = 2.3$.

2.3.1 State-Space Model of DVM rccBuck Converter

The state-space matrix for the interval $(t_2-t_3)$ is
\[ A_d = \begin{bmatrix} 0_{4\times4} & L_{mat}^{-1}v_{Ld} \\ \frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & \frac{1}{C_o} & 0 & 0 \\ \end{bmatrix} \quad v_{Ld} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & 0 & -1 \end{bmatrix} \] (2-53)

The corresponding transition matrix is \( \Phi_d(t_2, t_3) = e^{A_d(t_3-t_2)} \). Other state matrices, \( A_1, A_2, \) and \( B \), are the same as (2-45) – (2-46). The initial condition at DVM is

\[ X_0 = (P - \Phi_2 \Phi_d \Phi_1)^{-1} (\Phi_2 \Phi_d \Omega_1 + \Phi_2 \Omega_d + \Omega_2) \]

\[ \Omega_d(t_2, t_3) = \int_{t_0}^{t_3-t_2} e^{A_d(t_3-t_2-\tau)} BU \, d\tau \] (2-54)

The time-domain state-variable vector is

\[ x = \Phi_1(t)X_0 + \Omega_1(t) \quad (t_1 \leq t \leq t_2) \]

\[ x = \Phi_d(t)x(t_2) + \Omega_d(t) \quad (t_2 < t \leq t_3) \]

\[ x = \Phi_2(t)x(t_3) + \Omega_2(t) \quad (t_3 < t \leq t_4) \] (2-55)

The procedure to calculate the time-domain waveforms of a CVM or DVM rccBuck converter is shown in Fig. 2-32. The operating mode is determined by the capacitor voltage \( v_{Cr@t_2} \) at \( t_2 \). The converter operates in CVM at \( v_{Cr@t_2} \geq 0 \) and DVM at \( v_{Cr@t_2} < 0 \). An iteration of (2-55) is needed to calculate the \( (t_2-t_1) \). Thus, the DVM calculation takes more time than the CVM calculation. All state variables are calculated by

\[ x = [i_{Lra}, i_{Lrb}, i_{Loa}, i_{Lob}, v_{Cra}, v_{Cr@t_2}, v_{Co}]^T \] (2-56)

The MOSFET voltages and current could be calculated accordingly. This model is also valid for the rccBuck converter with Omni-coupled inductors by replacing the discrete \( L_{max} \) in (2-46) by a coupled \( L_{max} \) in (4-1).
The calculated waveforms of inductor current and capacitor voltages under DVM agree with the simulated ones, as shown in Fig. 2-33. The state-space model is able to detect the zero-cross point of $v_{Cra/b}$ and calculate the resonant waveforms. $i_{Lrb}$

**2.3.2 Analysis of Switched Stages**

As mentioned earlier, the interval $(t_2–t_3)$ is special for DVM. The equivalent circuits during the other intervals are the same for DVM and CVM. The equivalent circuit during $(t_2–t_3)$ is shown in Fig. 2-34. The synchronous switches $M_{1b}$ and $M_{2b}$ are turned on. The $C_{rb}$ is virtual shorted, and $v_{swa/b}$ is connected to ground. The current through $M_{1b}$ during $(t_2–t_3)$ at DVM is $i_{M_{1b}} = i_{Lrb}$, lower
than that at CVM, \( i_{L_{\text{ob}}} - i_{L_{\text{ra}}} \). Thus, the turn-off current of \( M_{1b} \) at \( t_3 \) is reduced. As duty ratio \( D \) increases, the \( (t_2 - t_3) \) is longer, and the turn-off current of \( M_{1b} \) is higher. The BVM has the minimum turn-off current \( I_{M_{1\text{off}}} \), which is discussed in Sub-section 2.3.3.

**Fig. 2-34.** (a) Circuit during interval \((t_2 - t_3)\) defined in Fig. 2-31 and (b) corresponding simplified schematic.

### 2.3.3 Impedance and Stress Curves under CVM or DVM

When the \( f_n \) and \( V_o/V_{\text{in}} \) exceed the boundary conditions in Fig. 2-20(b), the rccBuck converter operates in DVM, and the state-space model in (2-53)–(2-55) is used to calculate the impedance and stress curves.

Fig. 2-35 shows the normalized turn-off current of the active MOSFET. The dramatic dip corresponds to the BVM, which is mentioned in Sub-section 2.2.3. The negative turn-off current means the diode is still on when the channel is turned off. The turn-off current of DVM is much lower than that of CVM, especially when it is close to the BVM point. The turn-off loss of the DVM rccBuck converter then is lower than that of the CVM case. When \( f_n \) is small enough, e.g., \( f_n = 0.5 \) at \( L_n = 2 \), the DVM is not available, and there is no dip.
Fig. 2-35. Normalized turn-off current of M1a,1b versus Vd/Vin with (a) Ln = 2, (b) Ln = 1, and (c) Ln = 0.5 for both CVM and DVM. Zero-voltage turn-on is guaranteed for M1a/b, and zero-current turn-off is guaranteed for M2a/b.

Another benefit of the DVM is the extended duty ratio as shown in Fig. 2-36. As discussed earlier, the voltage gain is almost independent of fn at CVM (2-4). However, the DVM voltage gain would increase with fn. This is the result of the reduced effective turn-on time of the active MOSFETs. It is noted that the DVM here is only for the nominal load. At light load, all cases in Fig. 2-36 would operate at CVM. Therefore, if an rccBuck converter is designed with DVM at nominal load, the duty ratio would decrease at light load.

Fig. 2-36. Normalized D versus Vd/Vin at (a) Ln = 2, (b) Ln = 1, and (c) Ln = 0.5 for both CVM and DVM. Zero-voltage turn-on is guaranteed for M1a/b, and zero-current turn-off is guaranteed for M2a/b. The operating conditions are the same as Fig. 2-35.

The modeled RMS current of the MOSFETs under CVM and DVM at the nominal load is shown in Fig. 2-37. The DVM case has lower RMS current for the active FET and synchronous...
FET. The active FET at DVM has two triangular ripples in a switching cycle (Fig. 2-31), reducing the peak current and RMS current. The synchronous FET also has a multi-level ripple in a switching cycle, reducing the RMS current.

The operating conditions are the same as Fig. 2-35.

The DVM rccBuck converter usually has a lower $C_r$ and higher voltage stress, as illustrated in Fig. 2-38. The maximum voltage stress is 2.2 $V_{in}$ for the active FET and 1.7 $V_{in}$ for the synchronous FET. For 12 V input applications, the 30-V rating MOSFET is recommended for the active switch, and the 25-V rating MOSFET is recommended for the synchronous switch.

The total switch stress S and switch utilization U of the rccBuck converter and hard-switched buck converter are shown in Fig. 2-39. The DVM-rccBuck converter has higher S and lower U.
owing to higher voltage stress.

Fig. 2-39. Total switch stresses S (defined in [165] and normalized by \(V_i I_o\)) and switch utilization U versus \(V_o/V_{in}\) at (a) \(L_n = 2\), (b) \(L_n = 1\), and (c) \(L_n = 0.5\) for both CVM and DVM, compared with the state-of-the-art two-phase buck converter in Fig. 1-9. Zero-voltage turn-on is guaranteed for \(M_{1a/b}\) and zero-current turn-off is guaranteed for \(M_{2a/b}\). The operating conditions are the same as Fig. 2-35.

The ac RMS current increases for \(L_r\) and decreases for \(L_o\) when the operation mode changes from CVM to DVM, as shown in Fig. 2-40. At large \(V_o/V_{in}\), the impact of \(f_n\) on the inductor ac current is not significant since the total current ripple is low. At small \(V_o/V_{in}\), the ac current increases with \(f_n\) dramatically, and a high \(f_n\) should be avoided. The \(L_n\) is usually designed in the range \(0.5 \leq L_n \leq 1\). To simplify the design, \(L_n = 1\) is recommended when \(V_o/V_{in} \geq 0.2\), and \(L_n = 0.5\) is recommended when \(V_o/V_{in} < 0.2\), so that the ac RMS currents of \(L_r\) and \(L_o\) are comparable.

Fig. 2-40. Normalized inductor ac RMS currents versus \(V_o/V_{in}\) at (a) \(L_n = 2\), (b) \(L_n = 1\), and (c) \(L_n = 0.5\) for both CVM and DVM. Zero-voltage turn-on is guaranteed for \(M_{1a/b}\) and zero-current turn-off is guaranteed for \(M_{2a/b}\). The operating conditions are the same as Fig. 2-35.
The RMS current of \( L_o \) is almost independent of \( f_n \) since dc current is dominant, as shown in Fig. 2-41. The RMS current of \( L_r \) is significant at DVM, i.e., high \( f_n \), since the ac current is dominant, especially at small \( V_o/V_{in} \).

![Fig. 2-41. Normalized inductor RMS currents versus \( V_o/V_{in} \) with (a) \( L_n = 2 \), (b) \( L_n = 1 \), and (c) \( L_n = 0.5 \) for both CVM and DVM. Zero-voltage turn-on is guaranteed for \( M_{1a/b} \), and zero-current turn-off is guaranteed for \( M_{2a/b} \). The operating conditions are the same as Fig. 2-35.](image1)

The resonant tank design for the DVM is similar to that for the CVM. The \( f_n \) and \( Z_n \) are obtained from Fig. 2-42. The \( L_r \) and \( C_r \) are calculated by (2-5)–(2-6). The higher impedance means higher \( L_r \), larger size, and higher core loss. The design of \( L_r \) is challenging under DVM, due to the high RMS current and high \( Z_n \).

![Fig. 2-42. Normalized impedance \( Z_n \) versus \( V_o/V_{in} \) with (a) \( L_n = 2 \), (b) \( L_n = 1 \), and (c) \( L_n = 0.5 \) for both CVM and DVM. The designs in Table 2-5 are marked by symbols ⊗. Zero-voltage turn-on is guaranteed for \( M_{1a/b} \), and zero-current turn-off is guaranteed for \( M_{2a/b} \). The operating conditions are the same as Fig. 2-35.](image2)
mode, namely, a variable-frequency control. The \( Z_n \) is proportional to the \( I_{o\text{Max}} \) in (2-5), and the \( f_n \) is proportional to the \( 1/f_s \) in (2-6). If the rccBuck converter has no resonance, i.e., \( C_r \) is infinity, the frequency at 25% load is \( f_{s,25\%\text{load}} = 4 f_{s,100\%\text{load}} \). If the \( f_n = 0.9 \) and \( L_n = 0.5 \) are designed at the nominal load, \( Z_n \) is 3.8 at the nominal load and 0.95 at 25% load, corresponding to \( f_n = 0.9 \) and \( L_n = 0.5 \) in Fig. 2-42(c). The frequency change is \( f_{s,25\%\text{load}} = 1.8 f_{s,100\%\text{load}} \). The light-load efficiency then could be improved, thanks to the narrower frequency range. Summarized from the above analysis, the DVM rccBuck converter has the advantages of low turn-off current, extended \( D \), lower MOSFET RMS current, and higher light-load efficiency. The disadvantages are high voltage stresses and high ac current for \( L_r \).

The current and voltage stress curves in Fig. 2-35–Fig. 2-38 are modified to the contour plots in Fig. 2-43(a)–(e). The RMS currents of the MOSFETs are not considered since they are almost independent of \( f_n \) (Fig. 2-37). Higher \( V_o/V_{\text{in}} \) corresponds to lower \( V_{\text{ds}h}, V_{\text{ds}l}, I_{\text{M1off}}, I_{\text{LracRMS}}, \) and \( I_{\text{LoacRMS}} \); thus, the worst condition of an rccBuck converter is at the minimum \( V_o/V_{\text{in}} \). Lower \( f_n \) is beneficial to voltage stresses and \( I_{\text{LracRMS}}, \) and higher \( f_n \) is beneficial to \( I_{\text{M1off}} \) and \( I_{\text{LoacRMS}} \). The available \( f_n \) range and \( V_o \) range are then obtained when all voltage and current constraints are specified, as shown in Fig. 2-43(f). In this example, the constraints are: \( V_{\text{ds}h} < 1.9 \ V_{\text{in}}, V_{\text{ds}l} < 0.9 \ V_{\text{in}}, I_{\text{M1off}} < 0.8 \ I_o, I_{\text{LracRMS}} < 0.12 \ I_o, \) and \( I_{\text{LoacRMS}} < 0.1 \ I_o \). Higher \( V_o/V_{\text{in}} \) offers more choices of \( f_n \), e.g., \( 0.2 < f_n < 0.5 \) at \( V_o/V_{\text{in}} = 0.3 \). The available \( f_n \) range decreases as \( V_o/V_{\text{in}} \) decreases. The minimum \( V_o/V_{\text{in}} \) is 0.19 in this case, limited by the \( I_{\text{LracRMS}} \) constraint. In the available range of \( f_n \) and \( V_o/V_{\text{in}} \) in Fig. 2-43(f), higher \( f_n \) offers lower \( I_{\text{LoacRMS}} \) and higher \( V_{\text{ds}l} \). Finally, one can design an rccBuck converter with a proper \( V_o/V_{\text{in}} \) range, considering the trade-off among the voltage and current stresses. When \( f_n \) is determined, \( Z_n \) is read from Fig. 2-42, and \( L_r \) and \( C_r \) are calculated by (2-5) and (2-6).
Fig. 2-43. Contours of (a) $V_{dsh}/V_{in}$, (b) $V_{dsl}/V_{in}$, (c) $I_{M1off}/I_o$, (d) $I_{LracRMS}/I_o$, and (e) $I_{LoacRMS}/I_o$ versus $V_o/V_{in}$ and $f_n$ at $L_n = 1$. (f) Exemplary $f_n$ and $V_o/V_{in}$ ranges with specified $V_{dsh}$, $V_{dsl}$, $I_{M1off}$, $I_{LracRMS}$, and $I_{LoacRMS}$. All data is same as Fig. 2-35–Fig. 2-38.
2.3.4 Elimination of DVM Ringing by Clamped Diodes

The low impedance path (M₂ᵃ-Cₐᵇ-M₁ᵇ-M₂ᵇ) in the equivalent circuit Fig. 2-34(a) may cause severe current ringing, EMI noise, or efficiency degradation. This sub-section solves the DVM ringing by a clamped-diode method.

The schematic of the rccBuck converter with parasitic inductors is shown in Fig. 2-44(a). The MOSFET package inductance (Lₘᵃᵇ) and capacitor ESL (Lₖᵃᵇ) are considered. The low-impedance path during t₂–t₃ in Fig. 2-31 is highlighted in Fig. 2-44(b). The Cₖᵇ is resonant with Lₖᵇ + Lₘₖᵇ.

![Diagram](image)

Fig. 2-44. (a) RccBuck converters with parasitic inductors and (b) low-impedance path during t₂–t₃ (Fig. 2-31) under DVM.

The current waveforms for the DVM rccBuck converters with and without the parasitic inductances are compared in Fig. 2-45. The iₖ₁ᵇ, iₖ₂ᵃ, and iₖ₂ᵇ in Fig. 2-45(b) have severe ringing and higher RMS current. The current change of iₖ₁ᵇ at t₂ offers the initial energy of the resonant tank in Fig. 2-44(b).
Fig. 2-45. Simulated current waveforms of the DVM rccbuck converter (a) without and (b) with the parasitic inductances. The converter is operating at $V_{in} = 12$ V, $V_o = 1.2$ V, $I_{oMax} = 20$ A, $f_s = 2$ MHz, $L_r = 125$ nH, $L_o = 62$ nH, and $C_r = 56$ nF. The parasitic inductances are given in Fig. 2-44(a).

The equivalent circuit of Fig. 2-44(b) is simplified to Fig. 2-46(a) considering only ac component. The $L_{Mb}$ and $L_{Cb}$ are considered as an equivalent inductor $L_p$. The $R_{dc}$ is the total dc parasitic resistance, and the $R_{acp}$ is the total equivalent ac parallel resistance.

![Equivalent Circuit Diagram]

Fig. 2-46. (a) Simplified low impedance path in Fig. 2-45(b) during $t_2 - t_3$; corresponding modeled and simulated waveforms of (b) $v_{Crb}$ and (c) $i_{Lp}$ at $C_{rb} = 56$ nF, $R_{dc} = 4$ mΩ, $L_p = 0.9$ nH, $R_{acp} = 0.9$ Ω, $I_{Lp_initial} = 10$ A, and $V_{Crb_initial} = 0$.

The initial conditions of this resonant tank are $V_{Crb_initial} = 0$ and $I_{Lp_initial} = I_{Lob@t2} - I_{Lrb@t2}$.

The S-domain responses of $v_{Crb}$ and $i_{Lp}$ are

$$v_{Crb}(s) = \frac{-I_{Lp0}}{C_{rb}} \frac{1}{s^2 + 2\zeta \omega_0 s + \omega_0^2}, \quad i_{Lp}(s) = \frac{I_{Lp0}}{s^2 + 2\zeta \omega_0 s + \omega_0^2}$$

(2-57)

The corresponding time-domain responses are
\( v_{Crb}(t) = -\frac{L_{p0}Z_0}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_0 t} \sin(\omega_d t) \)  \hspace{1cm} (2-58)

\[ i_{Lp}(t) = L_{p0} e^{-\zeta\omega_0 t} \cos(\omega_d t) + \frac{L_{p0}}{2\omega_d} \left( \frac{1}{R_{acr}C_{rb}} - \frac{R_{dc}}{L_{p}} \right) e^{-\zeta\omega_0 t} \sin(\omega_d t) \]  \hspace{1cm} (2-59)

\[ Z_0 = \sqrt{\frac{L_{p}}{C_{rb}}} , \omega_0 = \frac{1}{\sqrt{L_{p}C_{rb}}} , \zeta = \frac{1}{2\omega_0} \left( \frac{1}{R_{acr}C_{rb}} + \frac{R_{dc}}{L_{p}} \right) , \omega_d = \sqrt{1-\zeta^2}\omega_0 \]  \hspace{1cm} (2-60)

Higher parasitic resistances could reduce the ringing during \( t_2-t_3 \), but the efficiency is sacrificed. In order to improve the impedance or damping during \( t_2-t_3 \), while maintaining low damping for the other intervals, two diodes are used to clamp the capacitor voltages, as illustrated in Fig. 2-47(a). The DVM noise is eliminated, and the RMS current of the MOSFETs is reduced.

Fig. 2-47. RccBuck converter with clamped diodes \( D_{ra} \) and \( D_{rb} \); corresponding simulated current waveforms. The operating conditions are given in Fig. 2-46.

The mechanism of diode clamping is illustrated in Fig. 2-48(b). When the diode voltage \( v_3 (\approx v_{Cb}) \) decreases to zero, the diode \( D_{rb} \) is turned on, and the forward voltage \( V_d \) forces the inductor \( i_{LMB} \) to decrease. The energy in the resonant tank is then partially consumed by the \( D_{rb} \).
The diode loss is calculated as follows: The $\Delta t_1 = t_{21} - t_{20}$ is calculated from

$$-v_3 = V_d = \frac{L_{Mb}}{L_{Cb} + L_{Mb}} \frac{I_{Lp0} Z_0}{\sqrt{1 - \zeta^2}} e^{-\zeta \omega_d \Delta t_1} \sin(\omega_d \Delta t_1)$$  \hspace{1cm} (2-61)

The inductor current $i_{LCB}$ at $t_{21}$ is

$$I_{LCB@t21} = I_{Lp0} e^{-\zeta \omega_d \Delta t_1} \cos(\omega_d \Delta t_1) + \frac{I_{Lp0}}{2 \omega_d} \left( \frac{1}{R_{acp} C_{rb}} - \frac{R_{dc}}{L_p} \right) e^{-\zeta \omega_d \Delta t_1} \sin(\omega_d \Delta t_1)$$  \hspace{1cm} (2-62)

The interval $\Delta t_2 = t_{22} - t_{21}$ is determined by $I_{LMB@t22} = I_{LCB@t22}$. The $I_{LMB@t22}$ and $I_{LCB@t22}$ are calculated by

$$I_{LMB@t22} \approx I_{LCB@t21} - \frac{V_d}{L_{Mb}} \Delta t_2$$  \hspace{1cm} (2-63)

$$I_{LCB@t22} \approx I_{LCB@t21} e^{-\zeta \omega_{cd} \Delta t_2} \cos(\omega_{cd} \Delta t_2) + \frac{I_{LCB@t21}}{2 \omega_d} \left( \frac{1}{R_{acp} C_{rb}} - \frac{R_{dc}}{L_{Cb}} \right) + v_d + v_{Crb@t21} \frac{v_{Crb@t21}}{L_{Cb} \omega_{cd}} e^{-\zeta \omega_{cd} \Delta t_2} \sin(\omega_{cd} \Delta t_2)$$  \hspace{1cm} (2-64)
\[
V_{crb@t21} = -\frac{L_{cb} + L_{Mb}}{L_{Mb}} V_d \omega_c \omega_{c0} = \frac{1}{\sqrt{L_{cb} C_{crb}}} \zeta_c = \frac{1}{2 \omega_c \left( \frac{1}{R_{cab} C_{crb}} + \frac{R_{cdd}}{L_{cb}} \right)} \omega_{cd} = \sqrt{1 - \zeta_c^2 \omega_c} \quad (2-65)
\]

The diode loss is then calculated by
\[
P_{Drb} = f_s V_d \Delta t_2 (i_{LMb} - i_{Lcb})_{AVG(t21-t22)} \quad (2-66)
\]

For the exemplary DVM rccBuck converter in Fig. 2-45, the loss caused by the parasitic ringing is 193 mW when the \(R_{ds(on)}\) is 8 mΩ for the active MOSFET and 3 mΩ for the synchronous MOSFET. The diode loss is 270 mW in Fig. 2-47. The efficiency degradation by the clamped diode is \((270-193)/24000=0.3\%\). In practice, the parasitic ringing may cause higher trace loss. Finally, the efficiencies for the rccBuck converters with and without the clamped diodes are similar.

### 2.4 Current-Sharing Analysis for Unbalanced Phases

The component and layout mismatches between the two phases may lead to the unbalanced current, which is detrimental for the system efficiency and EMI [96]–[101]. Both CVM- and DVM- rccBuck converters may have the mismatches. The unbalanced current of the CVM-rccBuck converter is exemplified in this section. The parasitic resistances and component tolerances are considered. The worst-case analysis and Monte Carlo analysis are performed in Subsection 2.4.1. The current-self-balancing mechanism is introduced in Subsection 2.4.2.

#### 2.4.1 Component Tolerance Analysis

When the rccBuck converter has mismatched components, the system has seven orders, and the analysis is complicated. The analytical formulas are difficult to derive; thus the state-space method is used herein to analyze the impact of component tolerance. Four inductors and two resonant capacitors are independent in the modeling. Duty ratios of the two phases are also considered as independent variables. The capacitor ESR is not considered since it is much smaller
than the inductors’ ac resistances. The phase shift is always 0.5, and the $C_{\text{oss}} = 0$ is assumed.

Since the two phases are asymmetric, the state-space matrixes of $A_1$ and $A_2$ in (2-45) are modified to

$$
A_1 = \begin{bmatrix}
-L^{-1}_{\text{mat}} R_{\text{mat}} & L^{-1}_{\text{mat}} v_{L1} \\
\frac{1}{c_{ra}} & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{c_{rb}} & \frac{1}{c_{rb}} & 0 & -\frac{1}{c_{ra}} & 0 & 0 \\
0 & 0 & \frac{1}{c_o} & 0 & 0 & 0
\end{bmatrix},
A_2 = \begin{bmatrix}
-L^{-1}_{\text{mat}} R_{\text{mat}} & L^{-1}_{\text{mat}} v_{L2} \\
\frac{1}{c_{ra}} & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{c_{rb}} & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{c_o} & \frac{1}{c_o} & 0 & 0
\end{bmatrix}
$$

(2-67)

The resistance matrix $R_{\text{mat}}$ is constructed by the dc resistances of $L_{ra/rb}$ and $L_{oa/ob}$

$$
R_{\text{mat}} = \begin{bmatrix}
R_{ra} & 0 & 0 & 0 \\
0 & R_{rb} & 0 & 0 \\
0 & 0 & R_{oa} & 0 \\
0 & 0 & 0 & R_{ob}
\end{bmatrix}
$$

(2-68)

The state-space matrix for the interval $(t_5-t_6)$ in Fig. 2-7 is

$$
A_3 = \begin{bmatrix}
-L^{-1}_{\text{mat}} R_{\text{mat}} & L^{-1}_{\text{mat}} v_{L3} \\
\frac{1}{c_{ra}} & \frac{1}{c_{ra}} & -\frac{1}{c_{ra}} & 0 & 0 & 0 \\
0 & \frac{1}{c_{rb}} & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{c_o} & \frac{1}{c_o} & 0 & 0
\end{bmatrix},
\begin{bmatrix}
\gamma_{L3} \\
\end{bmatrix}
$$

(2-69)

The corresponding state-space differential equations are

$$
\frac{dx}{dt} = A_1 x + B V_{in} \quad 0 \leq t < \frac{D_a}{f_s}
$$

(2-70)

$$
\frac{dx}{dt} = A_2 x + B V_{in} \quad \frac{D_a}{f_s} \leq t \leq \frac{0.5}{f_s}
$$

(2-71)

$$
\frac{dx}{dt} = A_3 x + B V_{in} \quad \frac{0.5}{f_s} < t \leq \frac{1 - D_b}{f_s}
$$

(2-72)

$$
\frac{dx}{dt} = A_2 x + B V_{in} \quad \frac{D_b}{f_s} \leq t \leq \frac{0.5}{f_s}
$$

(2-73)

The calculation of the initial condition is similar to (2-47), except the transition matrix $A_3$ is
included. The steady-state variables and their average values are calculated by (2-70)–(2-73), and
the current and voltage mismatches are calculated accordingly. Only one parameter is unbalanced
each time. For example, a 5% variation is applied for \( L_o \), namely, \( L_{oa} = 0.95 \) \( L_o \) and \( L_{ob} = 1.05 \) \( L_o \),
and other parameters (\( R_{Lo}, L_r, R_{Lr}, \) and \( C_r \)) are balanced.

The mismatches of the inductor dc current, peak-to-peak current, and voltage stresses of the
MOSFETs are shown in Fig. 2-49. The x-axis means the mismatch of the component, and the
y-axis means the unbalanced current or voltages. The normalized variation is defined by the
difference between the two phases over the balanced value. The parasitic resistances and
capacitances have negligible impacts on the current sharing and voltage stresses. The mismatch of
\( L_r \) leads to a significant current imbalance. The unbalanced current at high \( f_n \), e.g., \( f_n = 0.4 \), is more
severe since the resonant waveforms are significant. At small \( f_n \), e.g., \( f_n = 0.2 \), the waveforms are
straight, and the switched node voltages have symmetric rectangular waveforms.

![Fig. 2-49. Calculated variations of inductor current and MOSFET voltage stress for a single component with 5% mismatch at (a) \( f_n = 0.4 \) and (b) \( f_n = 0.2 \). Converter operates at \( V_{in} = 12 \) V, \( V_{o} = 3.3 \) V, \( I_o = 20 \) A, \( C_o = 2 \) \( \mu F \),
\( L_o = 100 \) nH, \( L_r = 144 \) nH, \( R_{Lr} = R_{Lo} = 5 \) m\( \Omega \), \( C_r = 264 \) nF, \( D = 0.78 \), and \( f_s = 2 \) MHz.](image)

In the Monte Carlo analysis, the interaction among multiple variations is considered. The
variations of \( L_{ra}, L_{oa}, R_{ra}, R_{oa}, \) and \( C_{ra} \) are generated simultaneously and randomly in the range
of \(-5\%–5\%\). The calculated results with 500 sweeping times are shown in Fig. 2-50. The variations
of \( I_{Lopp} \) and \( I_{Lrpp} \) follow the uniform distributions, indicating the current ripple is only dependent
on the inductance. The variations of $I_{L\text{duc}}$ and $I_{L\text{rdc}}$ follow normal distributions, indicating the current sharing is dependent on multiple variables. The imbalance of $f_n = 0.4$ is more severe than that of $f_n = 0.2$, which agrees with the conclusion from the worst-case analysis.

Fig. 2-50. Histograms of phase-a variations in rccBuck converter with the parameters in Fig. 2-49 by Monte Carlo analysis. The mismatch at (a) $f_n = 0.4$ is more severe than that at (b) $f_n = 0.2$.

The unbalanced current could be solved by the current-sharing control. Let $G_{di}$ be the transfer function from $\Delta d = d_a - d_b$ to the $\Delta i = i_{Lob} - i_{Loa}$. The averaged matrix of $A_1$, $A_2$, and $A_3$ is

$$A = D_a A_1 + D_b A_3 + (1 - D_a - D_b) A_2 \quad (2-74)$$

The averaged state-space model is

$$\dot{x} = Ax + (A_1 - A_2) X_0 \Delta d \quad (2-75)$$

$$\Delta i = C x, \ C = [0 \ 0 \ -1 \ 1 \ 0 \ 0 \ 0]$$

The $G_{di}$ is calculated by

$$G_{di} = C \frac{(A_1 - A_2) X_0}{SI - A} \quad (2-76)$$

A closed-form $G_{di}$ is complicated and not available at this point, since it is a seventh-order system. The numerically calculated $G_{id}$ for an unbalanced rccBuck converter is shown in Fig. 2-51(a). A type-II compensator with the bandwidth of 20 kHz was designed by using the method in [165]. The compensated zero was placed at 6 kHz to improve the phase margin, and the
compensated pole was placed at 1 MHz to reduce the high-frequency noise.

Fig. 2-51. Simulated (a) $G_{id}$ and (b) loop-gain of the rccBuck converter in Fig. 2-49 with 10% mismatch for $L_r$ ($L_{ra} = 158 \text{ nH}$ and $L_{rb} = 144 \text{ nH}$), 5% mismatch for $L_o$ ($L_{oa} = 95 \text{ nH}$ and $L_{ob} = 100 \text{ nH}$), and 5% mismatch for $C_r$ ($C_{ra} = 251 \text{ nF}$ and $C_{rb} = 264 \text{ nF}$).

Another low-path filter with 250 kHz corner frequency was placed between the power stage and the compensator to reduce the switching ripples. The overall schematic is shown in Fig. 2-52(a). The feedback parameter is a weighting function of input and output imbalances. The normalized mismatch is $\Delta I_{LrN} = 2|I_{Lra,dc} - I_{Lrb,dc}|/(I_{Lra,dc} + I_{Lrb,dc})$ for the input current and $\Delta I_{LoN} = 2|I_{Loa,dc} - I_{Lob,dc}|/(I_{Loa,dc} + I_{Lob,dc})$ for the output current. If the percentage of $\Delta I_{LoN}$ is 100%, the control objective is to minimize the output current mismatch. If that percentage is 0, the control objective is to minimize the input current mismatch. The current balance control reduces the mismatches below 2% as demonstrated in Fig. 2-52(b).
2.4.2 Current Self-Balance Mechanism in RccBuck Converter

The current self-balance mechanisms exist for several multi-phase converters such as the series-capacitor buck converter [102], the ZVS buck converter [103], and the series resonant converter [104]. The rccBuck converter also has a current self-balance mechanism, based on the partial ZVS operation.

Fig. 2-53 shows the simulated current and voltages for the unbalanced rccBuck converter with ideal switches (zero $C_{oss}$). The $R_{ds(on)}$ is 8 mΩ in the simulation. The two phases have significant unbalanced current and voltages. The mismatch of the input current is $\Delta I_{LN} = 103\%$, and the mismatch of the output current is $\Delta I_{LoN} = 31\%$. 

Fig. 2-52. (a) Current balance control of the rccBuck converter with $G_{id}$ and loop gain in Fig. 2-51; (b) simulated normalized output and input dc-current imbalances versus output/input weight. The input current mismatch is more significant since resonant current is dominant in $L_r$. 

<table>
<thead>
<tr>
<th>Weight of Output Current Mismatch</th>
<th>Normalized Current Imbalance</th>
</tr>
</thead>
<tbody>
<tr>
<td>0%</td>
<td>0.0%</td>
</tr>
<tr>
<td>20%</td>
<td>0.4%</td>
</tr>
<tr>
<td>40%</td>
<td>0.8%</td>
</tr>
<tr>
<td>60%</td>
<td>1.2%</td>
</tr>
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<td>80%</td>
<td>1.6%</td>
</tr>
<tr>
<td>100%</td>
<td>2.0%</td>
</tr>
</tbody>
</table>
Fig. 2-53. Simulated (a) current waveforms and (b) voltage waveforms for the unbalanced rccBuck converter in Fig. 2-49 with ideal switches at I_o = 20 A.

When the ideal switches were replaced by the real GaN model, EPC2100, the current and voltages are more balanced as shown in Fig. 2-54. The input mismatch $\Delta L_{IN}$ and output mismatch $\Delta L_{rN}$ decreases to 36% and 11.5%, respectively.

Fig. 2-54. Simulated (a) inductor current, (b) MOSFET voltages and MOSFET current for the unbalanced rccBuck converter in Fig. 2-49 using the half-bridge module, EPC2100, at I_o = 20 A.

The self-balance mechanism is explained as follows: If $L_{ra} > L_{rb}$, $i_{ra}$ has a lower current ripple, and $L_{ra}$ has a lower loss than $L_{rb}$. Therefore, the equivalent impedance of the $L_{ra}$ is lower than that
of \( L_{rb} \), leading to a higher dc current \( I_{Lra,dc} \), as shown in Fig. 2-54(a). The \( i_{Lob} - i_{Lra} \) has more negative current than \( i_{Loa} - i_{Lrb} \), and \( i_{M1b} \) has more negative current than \( i_{M1a} \), as shown in Fig. 2-54(b). The \( M_{1b} \) realizes ZVS, and \( M_{1a} \) realizes partial ZVS. Finally, the partial ZVS of \( M_{1a} \) increases the loss and the equivalent impedance of phase a. The higher imbalance of \( i_{Lra} \) and \( i_{Lrb} \), the higher switching loss of \( M_{1a} \). The mismatch of the two phases is then self-balanced.

The GaN model was modified in Fig. 2-55(a) so that the parasitic capacitors \( C_{gd}, C_{gs}, \) and \( C_{ds} \) could be configured in the top-level schematic. The current imbalances decrease with \( C_{gd} \) significantly since higher \( C_{gd} \) leads to higher switching loss, as shown in Fig. 2-55(b). The \( V_{ds}-I_{d} \) crossover loss during the gate plateau interval is the dominant loss at turn-on, for the MOSFET or GaN [153]–[155]. The \( C_{gs} \) and \( C_{ds} \) have no significant impacts on the switching loss; thus, the mismatch variation is only 20% as \( C_{gs} \) or \( C_{ds} \) increases from 0 to 2 nF.

![Diagram of RccBuck converter with configurable parasitic capacitors](image)

![Normalized Current Mismatch vs Capacitance](image)

**Fig. 2-55.** (a) RccBuck converter with configurable parasitic capacitors (\( C_{gd}, C_{gs}, \) and \( C_{ds} \)); (b) simulated input and output current mismatch versus those capacitances. The nominal condition is: \( C_{gs} = 1.3 \text{ nF} \), \( C_{ds} = 0.7 \text{ nF} \), and \( C_{gd} = 0.3 \text{ nF} \). Other parameters are the same as Fig. 2-49.

### 2.5 Experimental Verification

The state-space model, gain curves, stress curves, and DVM ringing are verified experimentally in this section. Three rccBuck converters switched under CVM with \( L_{n} = 2, 1, \) and
0.5 are designed in Sub-section 2.5.1. The measured waveforms and voltage gains are compared to the modeled ones. A DVM rccBuck is designed in Sub-section 2.5.2 and compared to a CVM reference design. Their waveforms and efficiencies were measured under the same input and output conditions.

All of the converters mentioned above use the PCB layout in Fig. 2-56. The resonant capacitors were placed close to the MOSFETs to reduce the parasitic inductances. The parasitic inductance $L_{Ca} = L_{Cb} = 0.2 \text{nH}$ and $L_{sa} = L_{sb} = 0.87 \text{nH}$ were extracted from the finite element simulation tool, Q3D. Those inductances may induce voltage spikes at the switched nodes when the active MOSFETs $M_{1a/1b}$ are turned off, especially at heavy load. Two half bridges $M_a$ and $M_b$ have negligible parasitic inductances of $L_{ga}$ and $L_{gb}$ since they are connected by a large copper plane (GND), on the top layer of the PCB.

![Fig. 2-56. (a) Resonant capacitors are close to MOSFETs to minimize (b) the parasitic inductances $L_{Ca}$ and $L_{Cb}$ in rccBuck converter.](image)

**2.5.1 CVM Verification**

The time-domain model and stress curves of CVM rccBuck converters in Section 2.2 were verified by three examples ($L_n = 2, 1,$ and 0.5) with $V_{in} = 12 \text{ V}$, $V_o = 3.3 \text{ V}$, $I_{oMax} = 20 \text{ A}$, and
$f_s = 2$ MHz. The specified and calculated parameters are given in Table 2-2.

**Table 2-2. Step-by-step design for CVM rccBuck converters with examples**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Design Method</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$L_n = 2$</td>
</tr>
<tr>
<td>$V_o$</td>
<td>Specified</td>
<td>3.3 V</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Specified</td>
<td>12 V</td>
</tr>
<tr>
<td>$I_{o\text{Max}}$</td>
<td>Specified</td>
<td>20 A</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Specified</td>
<td>2 MHz</td>
</tr>
<tr>
<td>$D$</td>
<td>Approximated by $V_o/V_{in} = D/(2+D)$</td>
<td>0.76</td>
</tr>
<tr>
<td>$f_n$</td>
<td>Max. $f_n$ at specified $V_o/V_{in}$ in Fig. 2-21</td>
<td>0.6</td>
</tr>
<tr>
<td>$Z_n$</td>
<td>Read from Fig. 2-21</td>
<td>1.8</td>
</tr>
<tr>
<td>$V_{dsM1a}$</td>
<td>Read from Fig. 2-22</td>
<td>18.6 V</td>
</tr>
<tr>
<td>$V_{dsM2a}$</td>
<td></td>
<td>11.4 V</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>$2C_{oss,M1a} + C_{oss,M2a}$ from [105]</td>
<td>4.2 nF</td>
</tr>
<tr>
<td>$L_r$</td>
<td>Calculated by (2-36), (2-37), and (2-42)</td>
<td>93 nH</td>
</tr>
<tr>
<td>$C_r$</td>
<td></td>
<td>189 nF</td>
</tr>
<tr>
<td>$L_o$</td>
<td>$L_o = L_n L_r$</td>
<td>186 nH</td>
</tr>
<tr>
<td>$t_{ZVSf_s}$</td>
<td>Calculated by (2-43)</td>
<td>0.10</td>
</tr>
</tbody>
</table>

For achieving high resonance at the required gain, $f_n = 0.6$, 0.6, and 0.5 were selected and marked by circular symbols (*) on Fig. 2-21 (a), (b), and (c), respectively; $Z_n = 1.8$, 2.5, and 2.9 were selected accordingly. Corresponding voltage stresses are ~20 V for $M_{1a/b}$ and ~13 V for $M_{2a/b}$ (Fig. 2-22). The switches were realized by Texas Instruments’ CSD87353Q5D Power Blocks offering $R_{\text{ds(on)}}$ of 2.8 mΩ for $M_{1a/b}$ and 0.9 mΩ for $M_{2a/b}$, and 30 V voltage rating. Gate drivers were LM5113. With the capacitor $C_o = 4.7 \mu$F for $L_n = 2$, the peak-to-peak voltage across the output is 5% of $V_o$. The normalized RMS current is 0.5 for $M_{2a/b}$ and 0.24 for $M_{1a/b}$ (Fig. 2-23). The normalized ac RMS current is 0.14 for $L_r$ and 0.05 for $L_o$ (Fig. 2-26). The normalized turn-off
current of M1a/b is 0.59 (Fig. 2-27). The duty ratio is \( D = 0.8 \) at rated load (Fig. 2-25). Corresponding numbers for \( L_n = 1 \) are 6.8 \( \mu \)F, 0.5, 0.24, 0.1, 0.08, 0.55, and 0.78. Corresponding numbers for \( L_n = 0.5 \) are 12 \( \mu \)F, 0.5, 0.24, 0.12, 0.07, 0.59, and 0.76. Equivalent output capacitance was calculated by \( C_{oss} = 2C_{oss,M1a} + C_{oss,M2a} \). Since \( V_{in}, V_o, I_{oMax}, f_s, f_n, Z_n, L_n, \) and \( C_{oss} \) were already specified or derived, three unknown parameters, \( L_r, L_o, \) and \( C_r \) could be solved from \( (2-36) \), \( (2-37) \), and \( (2-42) \). The last step is to check \( t_{ZVS} < \frac{D}{(2f_s)} \), as mentioned in Sub-section 2.2.1. All three exemplified designs met that constraint.

The \( C_r \) of \( L_n = 2 \) consists of one 100-nF, one 20-nF, and two 33-nF ceramic capacitors in parallel with ESR = 1.6 m\( \Omega \) in total. The \( C_r \) of \( L_n = 1 \) consists of one 100-nF and one 33-nF ceramic capacitors in parallel with ESR = 1.5 m\( \Omega \) in total. The \( C_r \) of \( L_n = 0.5 \) consists of one 100-nF, one 33-nF, and one 10-nF ceramic capacitors in parallel with ESR = 2 m\( \Omega \) in total. The prototypes are shown in Fig. 2-57, and the active footprint is 22 mm \( \times \) 27 mm.

![Fig. 2-57. Prototypes of rccBuck converter with (a) \( L_n = 2 \), (b) \( L_n = 1 \), and (c) \( L_n = 0.5 \), operating at \( V_{in} = 12 \) V, \( I_o = 20 \) A, and \( f_s = 2 \) MHz. Other parameters are given in Table 2-2.](image)

The measured inductances, dimensions, number of turns, dc resistances (\( R_{dc} \)), and ac resistances at 2 MHz (\( R_{ac@2MHz} \)) of \( L_r \) and \( L_o \) are shown in Table 2-3. The ac resistance is \( \sim 10 \) times the dc resistance, owing to skin effect and proximity effect. A thick wire was selected for \( L_o \) to reduce dc winding loss.
Table 2-3. Measured inductances, dimensions, and resistances of \( L_r \) and \( L_o \) for CVM recBuck converters

<table>
<thead>
<tr>
<th>( L_n )</th>
<th>( L_r ) (nH)</th>
<th>Wire diameter (mm)</th>
<th>Coil diameter (mm)</th>
<th>Number of turns</th>
<th>( R_{dc} ) (mΩ)</th>
<th>( R_{ac@2MHz} ) (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>96</td>
<td>1.06</td>
<td>11.27</td>
<td>3</td>
<td>2.3</td>
<td>17.7</td>
</tr>
<tr>
<td></td>
<td>193</td>
<td>1.22</td>
<td>11.60</td>
<td>5</td>
<td>2.9</td>
<td>37.0</td>
</tr>
<tr>
<td>1</td>
<td>130</td>
<td>1.06</td>
<td>10.65</td>
<td>4</td>
<td>2.6</td>
<td>27.7</td>
</tr>
<tr>
<td></td>
<td>132</td>
<td>1.22</td>
<td>11.71</td>
<td>4</td>
<td>2.3</td>
<td>25.0</td>
</tr>
<tr>
<td>0.5</td>
<td>180</td>
<td>1.06</td>
<td>13.11</td>
<td>5</td>
<td>3.4</td>
<td>33.2</td>
</tr>
<tr>
<td></td>
<td>91</td>
<td>1.22</td>
<td>11.96</td>
<td>3</td>
<td>1.8</td>
<td>16.8</td>
</tr>
</tbody>
</table>

The measured drain-source voltages of \( M_{1a} \), gate-driving signals of \( M_{1a} \), and \( v_{Cra} \) at \( I_o = 20 \) A and \( V_o = 3.3 \) V are shown in Fig. 2-58. ZVS is achieved for \( M_{1a} \). Voltage stress is \( \sim 19 \) V for \( M_{1a} \) and \( \sim 12 \) V for \( M_{2a} \). The converters operated under CVM since \( v_{Cra} > 0 \). The slight voltage ringing is caused by the hard turn-off of \( M_{1b} \). The voltage waveform of \( v_{swa} \) is clean as a result of ZVS of all MOSFETs and low turn-off current of \( M_{2a/b} \), as discussed in Section 2.2.

![Waveform](image)

**Fig. 2-58.** Measured \( v_{ds1a} \), \( v_{g1a} \), \( v_{Cra} \), and \( v_{swa} \) for the converters in Fig. 2-57 with (a) \( L_n = 2 \), (b) \( L_n = 1 \), and (c) \( L_n = 0.5 \) at \( I_o = 20 \) A.
The measured waveforms of $v_{ds1a}$, $v_{gs1a}$, $v_{Crb}$, and $v_{swa}$ at 25% load ($I_o = 5$ A) are shown in Fig. 2-59(a)–(c). ZVS is also achieved for $M_{1a}$. The voltage ringing of $v_{swa}$ is higher than that at rated load owing to the hard turn-off of $M_{2a/b}$. The ZVS of all MOSFETs is maintained within the whole load range, but ZCS of $M_{2a/b}$ is realized only at rated load using fixed switching frequency. If both ZVS and ZCS are required, switching frequency should increase at light load.

![Graphs](image)

**Fig. 2-60.** Measured, simulated, and modeled inductor current of rccBuck converters in Fig. 2-57 with (a) $L_n = 2$, (b) $L_n = 1$, and (c) $L_n = 0.5$ at $I_o = 20$ A.
The measured, simulated, and modeled inductor current waveforms are compared in Fig. 2-60. The error is less than 2%, calculated by one minus Pearson correlation coefficient introduced in [106] for measured and modeled waveforms. The current ripple increases for $L_o$, and decreases for $L_r$, as $L_n$ decreases (Table 2-4).

**Table 2-4. Recorded voltage stresses of $M_{1a/2a}$ (Fig. 2-58), peak-to-peak current, $I_{ppLr/Lo}$ (Fig. 2-60), and peak-to-peak voltages, $V_{ppCr}$ (Fig. 2-61).**

<table>
<thead>
<tr>
<th>$L_n$</th>
<th>$V_{ds1a}$ Max (V)</th>
<th>$V_{swa}$ Max (V)</th>
<th>$I_{ppLr}$ (A)</th>
<th>$I_{ppLo}$ (A)</th>
<th>$V_{ppCr}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>17.2 V</td>
<td>9.9 V</td>
<td>12.5 A</td>
<td>5.3 A</td>
<td>5.9 V</td>
</tr>
<tr>
<td>1</td>
<td>17.6 V</td>
<td>10.8 V</td>
<td>9.3 A</td>
<td>7.4 A</td>
<td>9.3 V</td>
</tr>
<tr>
<td>0.5</td>
<td>17.9 V</td>
<td>10.7 V</td>
<td>5.6 A</td>
<td>10.3 A</td>
<td>8.1 V</td>
</tr>
</tbody>
</table>

The measured, simulated, and modeled capacitor voltages are compared in Fig. 2-61(d)–(f). The impact of $C_{oss}$ on the waveforms is negligible here as a result of $C_{oss} \ll C_r$. The peak-to-peak voltage, $V_{ppCr}$, of $L_n = 1$ is higher than that of $L_n = 2$ as shown in Table 2-4, since the design point, $(V_o/V_{in} = 0.275, f_n = 0.6, L_n = 1)$, is closer to the BVM line shown in Fig. 2-20(b), than the design point, $(V_o/V_{in} = 0.275, f_n = 0.6, L_n = 2)$.

The measured and simulated efficiency curves in Fig. 2-62(a) ascend up to rated load. Peak efficiencies of $L_n = 2, 1,$ and 0.5 are 93.3%, 93.6%, and 93.6%, respectively. ZVS is realized from 0 to 20 A using constant switching frequency (2 MHz). A variable switching frequency will be
tried in the future to improve the light-load efficiency, similar to the critical-mode ZVS buck converter in [107]‒[108].

![Graph](image)

**Fig. 2-62.** (a) Simulated and measured efficiencies; (b) simulated loss breakdown versus load current of rccBuck converters in Fig. 2-57.

The loss breakdown of three rccBuck converters at $I_o = 20$ A is evaluated in Fig. 2-62(b). The winding loss of $L_r$ is calculated by $P_{Lr} = I_{Lrdc}^2 R_{Lrdc} + I_{LracRMS}^2 R_{Lrac}$. The dc winding loss, $I_{Lrdc}^2 R_{Lrdc}$, is negligible because $I_{Lrdc} < I_{LracRMS}$ and $R_{Lrdc} << R_{Lrac}$. The normalized $I_{LracRMS}$ for $L_n = 2, 1, \text{and } 0.5$ (Fig. 2-26) is 0.14, 0.1, and 0.07, respectively. The corresponding $R_{Lrac}$ (Table 2-3) is 17.7 mΩ, 27.7 mΩ, and 33.2 mΩ. Finally, the case of $L_n = 2$ has the highest $P_{Lr}$. The winding loss of $L_o$ is calculated by $P_{Lo} = I_{Lodc}^2 R_{Lodc} + I_{LoacRMS}^2 R_{Loac}$. The case of $L_n = 2$ has the highest $R_{Lodc}$ and $R_{Loac}$ (Table 2-3), and the lowest $I_{LoacRMS}$ (Fig. 2-26). The total winding loss of $L_o$ is similar for the three cases. The conduction loss of the active MOSFET is $P_{\text{cond},h} = I_{M1,RMS}^2 R_{dsh}$, where $I_{M1,RMS}$ can be calculated by (2-51), and $R_{dsh}$ includes the $R_{ds(on)}$ of the MOSFET and connecting trace resistance (~1 mΩ for the layout in this experiment). The conduction loss of the synchronous MOSFET, $P_{\text{cond},l}$, is higher than $P_{\text{cond},h}$ since $I_{M2,RMS}$ (in (2-52)) > $I_{M1,RMS}$ (in(2-51)). Three cases were designed with the same MOSFET, layout, and RMS current so that their conduction losses are almost the same. All MOSFETs have low turn-on loss ($P_{\text{h,on}}$ and $P_{\text{l,on}}$),
as a result of the realization of ZVS, and low turn-off loss of M_{2a/b} (P_{L_{off}}) because of ZCS of M_{2a/b} at rated load. The normalized turn-off current of M_{1a/b} for \( L_n = 2, 1, \) and 0.5 (Fig. 2-27) is 0.59, 0.55, and 0.59, respectively. The case of \( L_n = 1 \) has the lowest turn-off loss of M_{1a/b} (P_{h_{off}}) because its turn-off current is the lowest. The total gate-driving loss is 0.85 W, independent of \( L_n \). Notice that \( P_{g_{,b}} < P_{g_{,t}} \) since the synchronous MOSFET has larger die and larger \( C_{iss} \). Capacitor loss \( P_{Cr} \) is relatively low since multiple ceramic capacitors were placed in parallel to lower the ESR of \( C_r \) (below 2 mΩ). Overall, from the semiconductor point of view, the case of \( L_n = 1 \) is the best since its turn-off current and switching loss are minimal. From the inductor point of view, the case of \( L_n = 0.5 \) is the best according to the lowest loss of \( L_r \).

### 2.5.2 DVM Verification

The air-core inductors in Fig. 2-57 were redesigned for the verification of the DVM operation. The specifications are the same with Table 2-2 except \( V_o = 1.2 \) V. Two design points are marked in Fig. 2-42(c): \( f_n = 0.9, L_r = 128 \) nH, \( L_o = 64 \) nH, and \( C_r = 60 \) nF for the DVM design; \( f_n = 0.8, L_r = 90 \) nH, \( L_o = 45 \) nH, and \( C_r = 111 \) nF for the CVM reference design. The parameters of the air-core inductors are given in Table 2-5.

Table 2-5. Measured inductances, dimensions, and resistances of \( L_{r/o} \) for DVM/CVM rccBuck converters with \( V_{in} = 12 \) V, \( V_o = 1.2 \) V, \( I_o = 20 \) A, and \( f_s = 2 \) MHz.

<table>
<thead>
<tr>
<th>( f_n )</th>
<th>( L ) (nH)</th>
<th>Wire diameter (mm)</th>
<th>Coil diameter (mm)</th>
<th>Number of turns</th>
<th>( R_{dc} ) (mΩ)</th>
<th>( R_{ac@2MHz} ) (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9 (DVM)</td>
<td>( L_r )</td>
<td>127</td>
<td>1.06</td>
<td>10.8</td>
<td>4</td>
<td>2.6</td>
</tr>
<tr>
<td></td>
<td>( L_o )</td>
<td>67</td>
<td>1.72</td>
<td>12.0</td>
<td>3</td>
<td>0.83</td>
</tr>
<tr>
<td>0.8 (CVM)</td>
<td>( L_r )</td>
<td>130</td>
<td>1.06</td>
<td>11.8</td>
<td>3</td>
<td>2.1</td>
</tr>
<tr>
<td></td>
<td>( L_o )</td>
<td>132</td>
<td>1.72</td>
<td>9.8</td>
<td>3</td>
<td>0.67</td>
</tr>
</tbody>
</table>

The measured waveforms of the DVM rccBuck converter with and without the damped diodes
are shown in Fig. 2-63. The damped diodes were MBRS130LT3G with a 30 V rating. The switches were realized by Texas Instruments’ CSD87355Q5D Power Blocks offering $R_{ds(on)}$ of 3.9 mΩ for $M_{1a/b}$ and 0.9 mΩ for $M_{2a/b}$, and 30 V voltage rating. The output current for the case without damped diodes was limited by $I_o \leq 15$ A, owing to the significant ringing, which was caused by the low-impedance path in Fig. 2-44(b). The waveforms for the rccBuck converter with the damped diodes are clean (Fig. 2-63(b)). The damped-diode method could eliminate the ringing effectively.

The DVM rccBuck converters with and without clamped diodes have the same efficiencies as shown in Fig. 2-64(a). The maximum current increases from 15 A to 20 A by using the clamped diodes.

**Fig. 2-63.** Measured voltage waveforms for the DVM rccBuck converter in Table 2-5 (a) without clamped diodes at $I_o = 15$ A and (b) with clamped diodes at $I_o = 20$ A. Both cases have the same $V_{in} = 12$ V, $V_o = 1.2$ V, and $f_s = 2$ MHz.

The efficiency of the CVM converter is higher than that of the DVM converter within an entire load range for a fixed switching frequency (Fig. 2-64(a)). The light-load efficiency of the DVM converter can be improved significantly by increasing the efficiency, as illustrated in Fig. 2-64(b). This is the result of reduced current ripple. The improvement of light-load efficiency for the CVM
converter is not significant (Fig. 2-64(c)). Finally, the CVM converter has a 1.2% higher efficiency than the DVM converter at 20 A by switching at 2 MHz. The DVM converter has a 1.9% higher efficiency at 5 A by switching at 2.4 MHz.

![Graphs showing efficiency comparison](image)

**Fig. 2-64.** Measured efficiencies for (a) the converters in Table 2-5 switched at 2 MHz; (b) DVM and (c) CVM converters switched at a fixed \( f_s \); (d) CVM and DVM converters switched at a variable \( f_s \). All converters operate with \( V_{\text{in}} = 12 \) V and \( V_o = 1.2 \) V.

The estimated loss breakdown of the CVM and DVM converters at the nominal load is shown in Fig. 2-65. The inductor loss \( P_{\text{Lr}} \) of the DVM case doubles that of the CVM case because of the higher RMS current (Fig. 2-40) and high \( R_{\text{ac}} \) (Table 2-5). The turn-off loss of the active MOSFET, \( P_{\text{offh}} \), is negligible under DVM because of the small turn-off current. The clamped-diode loss is much lower than the inductor loss and conduction loss.
Fig. 2-65. Simulated loss breakdown for the CVM and DVM rccBuck converters in Fig. 2-64 at $I_o = 20$ A.

2.6 Conclusion

The steady state of the rccBuck converter under CVM was calculated by the state-space model. Closed-form formulas were presented and verified by three 12 V-to-3 V converters switched at 2 MHz with $L_n = 2$, 1, and 0.5, reaching peak efficiencies of 93.3%, 93.6%, and 93.6% at 20 A, respectively. The errors between measured and modeled time-domain state variables were less than 2%. The recommended design of $L_n$ is $0.5 \leq L_n \leq 1$. The active switch is turned on with zero voltage over a wide load. The voltage stress is $1.6V_{in}$ for the active switch and $V_{in}$ for the synchronous switch. The turn-off current of the active switch is below $0.6I_o$, as a result of the resonance between $L_r$ and $C_r$. Air-core inductors were employed in the experiment since the commercial ferrite inductors with the required inductances (usually < 200 nH) have high ac winding loss and high core loss at 2 MHz. Those air-core inductors are replaced by designed ferrite one-turn inductors in Chapter 3 to reduce the loss and volume.

The clamped diodes were demonstrated experimentally and effectively eliminated the parasitic ringing under DVM while maintaining efficiency. The resonant inductor in the DVM
rccBuck converter needs to handle high ac flux and has high ac winding loss. The light-load efficiency can be improved significantly by increasing the switching frequency for the DVM converter.

The major losses at rated load for both CVM and DVM converters are the MOSFET conduction loss and inductor losses. The synchronous switch could use a low rating MOSFET to reduce the conduction loss. Salient findings also include the significant impact of $L_e$ on current sharing and a partial-ZVS based self-balance mechanism.
Chapter 3  Design Methodology of a One-Turn Inductor with Significant Ac and Dc Fluxes – Demonstration in a GaN-Based RccBuck Converter

Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_e$ and $l_e$</td>
<td>Effective cross-sectional area and effective length</td>
</tr>
<tr>
<td>$C_m$, $\alpha$, and $\beta$</td>
<td>Core loss coefficients</td>
</tr>
<tr>
<td>$H_{dc}$ and $H_{max}$</td>
<td>Dc and maximum magnetic field strength</td>
</tr>
<tr>
<td>$h_w$ and $w_w$</td>
<td>Winding thickness and width</td>
</tr>
<tr>
<td>$H_x$ and $H_y$</td>
<td>Magnetic field strength in x- and y- directions in the window area</td>
</tr>
<tr>
<td>$H_{x,RMS}$ and $H_{y,RMS}$</td>
<td>The RMS value of $H_x$ and $H_y$ on top winding surface</td>
</tr>
<tr>
<td>$I_{dc}$ and $I_{pk}$</td>
<td>Dc current and peak current</td>
</tr>
<tr>
<td>$J_{ac}$</td>
<td>Ac current density</td>
</tr>
<tr>
<td>$K_{dc}$</td>
<td>Dc effect on core loss density</td>
</tr>
<tr>
<td>$K_{Hy}$</td>
<td>Curve-fitted factor representing $H_y$ effect on ac winding loss</td>
</tr>
<tr>
<td>$l_c$, $w_c$, and $l_g$</td>
<td>Core length, core width, and gap length</td>
</tr>
<tr>
<td>$L_n$</td>
<td>Inductance ratio of $L_o/L_r$</td>
</tr>
<tr>
<td>$l_{wg}$</td>
<td>Vertical distance from the winding to the gap for vertical-gap core</td>
</tr>
<tr>
<td>$l_{wc}$</td>
<td>Vertical distance from the winding to the core for horizontal-gap core</td>
</tr>
<tr>
<td>$P_{CL}$ and $P_{v0}$</td>
<td>Total core loss with dc effect and core loss density without dc effect</td>
</tr>
<tr>
<td>$P_{condh}$ and $P_{condl}$</td>
<td>Conduction loss of high-side and low-side MOSFETs</td>
</tr>
<tr>
<td>$P_{gateh}$ and $P_{gatell}$</td>
<td>Gate-driving loss of high-side and low-side MOSFETs</td>
</tr>
<tr>
<td>$P_{swh}$ and $P_{swl}$</td>
<td>Switching loss of high-side and low-side MOSFETs</td>
</tr>
<tr>
<td>$P_{wt}$ and $P_{wac}$</td>
<td>Total winding loss and ac winding loss</td>
</tr>
<tr>
<td>$R_{dc}$ and $R_{ac}$</td>
<td>Dc an ac resistances</td>
</tr>
<tr>
<td>$V_{ol}$</td>
<td>Magnetic volume</td>
</tr>
<tr>
<td>$\Delta T$</td>
<td>Temperature difference between the inductor surface and ambient</td>
</tr>
<tr>
<td>$\delta$</td>
<td>Skin depth</td>
</tr>
<tr>
<td>$\mu_0$ and $\mu_r$</td>
<td>Vacuum permeability and relative permeability</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Copper conductivity</td>
</tr>
</tbody>
</table>
One-turn inductors must cope with high dc flux in conventional hard-switched point-of-load converters. These inductors need to handle both high dc and ac fluxes in soft-switched converters with high current ripple, for example, resonant cross-commutated buck (rccBuck) converters. In order to understand the losses associated with those fluxes, the winding loss in MHz range was modeled through calculating the fringing field in the window area. The dc-biased core loss for resonant waveforms was modeled by the Equivalent Elliptical Loop (EEL) method. According to the loss models, winding and core dimensions were designed systemically to minimize the total loss within a smaller volume than that of a commercial product. An rccBuck converter switched at 12 V input and 1.2 V at 20 A output was constructed and compared with a two-phase synchronous buck converter with the same specifications. They employ the same GaN switches and filter capacitors, and are designed to have the same magnetic volume, so that the overall volumes are comparable. The rccBuck converter using the designed one-turn inductors achieved 1.1% higher efficiency at rated load, by switching at 2 MHz, and 0.8% higher efficiency at medium load, by switching at 2.5 MHz. All switches have clean waveforms and low noise within a wide load range even with zero gate resistances. The rccBuck converter with ZVS operation, achieves ~15 dB lower conducted-EMI noise in 100–500 MHz than that of the hard-switched buck converter. The experiment also demonstrated, the designed one-turn inductors gave 2.1% higher efficiency than the commercial inductors with similar inductances and double magnetic volumes, on the same rccBuck converter. The related simulation files are given in Appendix F.

3.1 Introduction

Multi-phase buck converters for point-of-load (POL) applications operate at low output voltage and high dc current, usually requiring filter inductors to have low inductance for low
volume and low dc resistance for high efficiency [109]. One-turn inductors with both features and a simple structure are generally adopted in such converters. They are classified as lateral-flux inductors [110]–[115] or vertical-flux inductors [116]–[117]. A lateral-flux pattern means the magnetic flux path plane parallels the core substrate. The winding is realized by a short round wire or the printed circuit board (PCB) via, so the winding loss is reduced significantly; however, the ac-current capability is limited. This is a result of the short flux path length, high ac flux density, and high core loss density [110]. A vertical-flux pattern means the flux path plane is perpendicular with the core substrate. It employs rectangular flat wire with a longer flux path length and thus can handle higher ac current. The gapped ferrite inductor with a vertical-flux pattern is selected and studied in this section because of the low core loss density of ferrite at MHz range, high dc-flux capability of the gapped core, and high ac-flux capability of the vertical-flux inductor.

Fig. 3-1. (a) Resonant cross-commutated buck converter and (b) current waveforms for $L_{ra/b}$ and $L_{oa/b}$.

The Si-based rccBuck converters with air-core inductors were introduced in Chapter 2. This chapter extends the concept to a 1.2 V GaN-based point-of-load converter with four inductors, realized by one-turn gapped cores, as shown in Fig. 3-1(a). The simulated MOSFET losses for the commercial half-bridge power blocks at 2 MHz are compared in Fig. 3-2. The rccBuck converter offers lower switching loss than the hard-switched buck converter. Compared with the Si switch
with a slow turn-off speed, the GaN switch with low turn-off loss is more suitable for the ZVS converter with high turn-off current [108]. The half-bridge e-GaN, EPC2100, with the minimum loss, was selected in this chapter.

The passive components $L_r$, $L_o$, and $C_r$ in Fig. 3-1(a) are designed by using the steady-state model in Sub-section 2.2.2. With this configuration, all switches can achieve ZVS at $I_o = 0 – 20$ A. The $C_r$ was implemented by paralleling several ceramic capacitors, shown in Table 3-1. The C0G-0805-33μF capacitor was selected due to the minimum ESR. The total ESR was 0.3 mΩ when eight were paralleled to achieve the specified value, 264 nF, in Fig. 3-1(a).

All inductors need to handle high ac current ripple as shown in Fig. 3-1(b). The design for the $L_{oa/b}$ is more difficult than that for $L_{ra/b}$ since $L_{oa/b}$ conducts higher dc current. Reducing core loss for the inductors with high dc and ac fluxes is challenging. As shown in [124], the core loss of a commercial inductor grows exponentially as the current increases, for realizing an entire-load-

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**Fig. 3-2.** Simulated MOSFET loss (including driving, switching, and conduction losses) per phase for commercial half-bridge modules [111]–[113] used in the buck and rccBuck converters with $V_{in} = 12$ V, $V_o = 1.2$ V, $f_s = 2$ MHz, and $I_o = 10$ A per phase. Half-bridge GaN module has the lowest loss.
range ZVS in a series-capacitor buck converter. The limitation of high core loss is also mentioned in the design of high ac-flux inductors for the QSW-ZVS flyback converter [125]. Along with ac flux, dc flux has an adverse impact on core loss of the ferrites such as MMG F49, N87, LTCC, and 3F3 [126]–[129]. Moreover, high dc current may induce irreversible high core loss for Ni-Zn ferrite [130]. Selecting proper magnetic material and modeling dc-biased core loss are challenges.

### Table 3-1. ESR and ESL for Commercial Ceramic Capacitors [131]

<table>
<thead>
<tr>
<th>EIA package</th>
<th>Quality type</th>
<th>Rating</th>
<th>C (nF)</th>
<th>ESL (nH)</th>
<th>ESR@2MHz (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0402</td>
<td>X7R</td>
<td>50 V</td>
<td>10</td>
<td>0.64</td>
<td>206</td>
</tr>
<tr>
<td>0402</td>
<td>X7R</td>
<td>50 V</td>
<td>100</td>
<td>0.53</td>
<td>30.2</td>
</tr>
<tr>
<td>0603</td>
<td>C0G</td>
<td>50 V</td>
<td>10</td>
<td>0.93</td>
<td>4.4</td>
</tr>
<tr>
<td>0603</td>
<td>X7R</td>
<td>50 V</td>
<td>33</td>
<td>0.77</td>
<td>48</td>
</tr>
<tr>
<td>0603</td>
<td>X7R</td>
<td>50 V</td>
<td>100</td>
<td>0.64</td>
<td>23.5</td>
</tr>
<tr>
<td>0603</td>
<td>X7R</td>
<td>25 V</td>
<td>1000</td>
<td>0.84</td>
<td>6.6</td>
</tr>
<tr>
<td>0805</td>
<td>C0G</td>
<td>100 V</td>
<td>10</td>
<td>0.64</td>
<td>3.7</td>
</tr>
<tr>
<td>0805</td>
<td>C0G</td>
<td>50 V</td>
<td>22</td>
<td>0.61</td>
<td>3.3</td>
</tr>
<tr>
<td>0805</td>
<td>C0G</td>
<td>50 V</td>
<td>33</td>
<td>0.93</td>
<td>2.4</td>
</tr>
<tr>
<td>0805</td>
<td>X7R</td>
<td>50 V</td>
<td>100</td>
<td>1.01</td>
<td>23.4</td>
</tr>
<tr>
<td>0805</td>
<td>X7S</td>
<td>100 V</td>
<td>1000</td>
<td>0.70</td>
<td>7.9</td>
</tr>
<tr>
<td>0805</td>
<td>X7R</td>
<td>25 V</td>
<td>4700</td>
<td>0.80</td>
<td>2.9</td>
</tr>
</tbody>
</table>

High ac winding loss, caused by the fringing flux in the window area, is another challenge of a gapped one-turn inductor. A conventional one-turn inductor with full utilization of a winding window is not available for high ac-flux applications. A little space between the gap and winding would be helpful in reducing the ac winding loss. This method is discussed in this chapter, and its impact on winding loss and volume is modeled.

In summary, one-turn gapped inductors with significant dc and ac fluxes are designed and
applied for the rccBuck converter in this work. The core structure and ac resistance of commercial one-turn inductors are surveyed in Section 3.2. The ac resistance and time-domain core loss are modeled in Sections 3.4 and 3.5, respectively; both are verified by finite element simulations. Section 3.6 describes the effects of the winding thickness, core thickness, winding width, and utilization factor of the winding window on the total loss. The overall design procedure is then presented. Modeled inductances, efficiency improvement, and ZVS operations are verified experimentally in Section 2.3. The conclusion and future work are given in Section 3.8.

### 3.2 Limitations of Commercial One-Turn Gapped Inductors

Commercial one-turn gapped inductors are usually designed with full utilization of the window area for low dc resistance as shown in Fig. 3-3(a) and (b). The winding is close to the air gap and exposed to significant fringing flux as shown in Fig. 3-3(c). The ac current density is crowded around the gap because the fringing flux goes through the winding.

![Fig. 3-3. (a) Commercial one-turn inductor [136] and its side view. (b) Simulated flux lines and ac current density (J_{ac}) at 2 MHz when winding is near the gap.](image)

The surveyed dc resistance (R_{dc}), ac resistance at 2 MHz (R_{ac@2MHz}), and the dimensions of commercial one-turn inductors from [136] are listed in Table 3-2. The inductance range is 36–100 nH. For the inductors in Table 3-2, the ac power loss is given by the calculator in [137] multiplied by a factor of 2.5 recommended by the manufacturer. The excitation in this calculator
is 2 MHz PWM voltage with a 0.2 V-µs volt-second and 50% duty ratio. The $R_{ac}$ in Table 3-2 is the equivalent ac resistance, representing the sum of the ac winding loss and core loss. For a fixed core dimension, higher inductance tends to have more significant core loss and higher $R_{ac}$. High $R_{ac@2MHz}/R_{dc}$ of the commercial one-turn gapped inductors in Table 3-2, yields they are not suitable for MHz converters with high ac current. The magnetic material could be replaced by the low-loss ferrite selected in Section 3.3 to reduce the core loss. Core and winding dimensions could be redesigned by using the models in Sections 3.4 and 3.5 to reduce the ac winding loss.

### Table 3-2. $R_{dc}$, $R_{ac}$ at 2 MHz, and dimensions of Commercial One-Turn Inductors from [136]

<table>
<thead>
<tr>
<th>Package No.</th>
<th>Footprint (mm$^2$)</th>
<th>Height (mm)</th>
<th>L (nH)</th>
<th>$R_{dc}$ (mΩ)</th>
<th>$R_{ac@2MHz}$ (mΩ)</th>
<th>$R_{ac@2MHz}/R_{dc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC7649</td>
<td>7 × 7.6</td>
<td>5</td>
<td>36</td>
<td>0.18</td>
<td>7.78</td>
<td>43.20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>51</td>
<td>0.18</td>
<td>15.61</td>
<td>86.70</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>70</td>
<td>0.18</td>
<td>29.40</td>
<td>163.33</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>0.18</td>
<td>52.50</td>
<td>291.67</td>
</tr>
<tr>
<td>SLC7530S</td>
<td>6.7 × 7.5</td>
<td>3</td>
<td>50</td>
<td>0.123</td>
<td>30.00</td>
<td>243.90</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>64</td>
<td>0.123</td>
<td>49.15</td>
<td>399.61</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>82</td>
<td>0.123</td>
<td>80.69</td>
<td>656.00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>0.123</td>
<td>120.00</td>
<td>975.61</td>
</tr>
<tr>
<td>SLC1175</td>
<td>7.5 × 10.8</td>
<td>7.2</td>
<td>70</td>
<td>0.252</td>
<td>14.70</td>
<td>58.33</td>
</tr>
<tr>
<td>SLC1049</td>
<td>6.9 × 10.2</td>
<td>5.2</td>
<td>75</td>
<td>0.23</td>
<td>21.09</td>
<td>91.71</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>0.23</td>
<td>37.50</td>
<td>163.04</td>
</tr>
</tbody>
</table>

### 3.3 Dc-Biased Core Loss Densities of MHz Magnetic Materials

A one-turn inductor with significant dc and ac fluxes requires magnetic material with a low
dc-biased core loss density. This section compares the core loss densities of the state-of-the-art ferrites without dc bias first, and then discusses the dc bias effect.

The measured core loss densities without the bias at 2 MHz of 4F1 (Ferroxcube), 67 (Fair-rite), 3F46 (Ferroxcube), and ML91S (Hitachi Metals) are compared in Fig. 3-4. The measurement procedure followed [132]. The dimensions of the toroids under test were as follows: OD (outer diameter) = 25.7 mm, ID (inner diameter) = 14.9 mm, and Ht (height) = 10.5 mm for 4F1; OD = 9.5 mm, ID = 4.75 mm, and Ht = 3.3 mm for 67; OD = 14 mm, ID = 7 mm, and Ht = 5 mm for ML91S; OD = 10 mm, ID = 5 mm, and Ht = 3.5 mm for 3F46. The core loss densities from datasheets [133]–[134] are also included. The discrepancy between the measurement and datasheet might come from capacitor ESR, phase discrepancy, parasitic capacitances, environmental temperature, etc.

![Graph showing core loss densities](image)

**Fig. 3-4. Zero-biased core loss densities of 4F1, 67, 3F46, and ML91S at 2 MHz.**

The Mn-Zn ferrites (3F46 and ML91S) could handle higher ac flux density ($B_m$) than the Ni-Zn ferrites (4F1 and 67) at 2 MHz. For example, the $B_m$ is ~ 30 mT for Mn-Zn ferrites and ~ 20 mT for Ni-Zn ferrites at $P_v = 200$ mW/cm$^3$. In terms of the dc characteristic, the saturation flux density of Mn-Zn ferrites is ~ 0.5 T, higher than that of Ni-Zn ferrites, ~ 0.3 T. The Mn-Zn
ferrites also have a higher permeability and lower dc magnetic field strength ($H_{dc}$) for gapped cores. Therefore, the Mn-Zn ferrites are more suitable for the one-turn inductor operating at 2 MHz with high ac and dc fluxes.

As mentioned earlier, the dc effect on the core loss is also important and needs to be characterized. Another winding was added on the toroidal core as the dc current excitation. The measurement procedure followed [130]. According to the shape of the $P_v - H_{dc}$ curve, the dc effect is classified as either a reversible dc effect or irreversible dc effect. The reversible dc effect means the $P_v$ increases with $H_{dc}$, and recovers to initial $P_v$, after $H_{dc}$ decreases to 0. The irreversible dc effect means the $P_v$ increases with $H_{dc}$, but cannot recover to initial $P_v$ after $H_{dc}$ decreases to 0. The material is not stable if the irreversible dc effect is significant. An unstable example is shown in Fig. 3-5(a). The maximum $H_{dc}$ is 70 A/m for the small loop and 100 A/m for the large loop. The $P_v$ at $H_{dc} = 0$ increases to 2.3 times the initial $P_v$ after the large loop is applied. This phenomenon was also observed in [130], but the inner mechanisms are still unknown.

![Fig. 3-5. Measured core loss densities at $B_{ac} = 20$ mT and $f_s = 2$ MHz under room temperature for (a) unstable case and (b) the stable material, 3F46.](image)

The most stable material is 3F46 with a tiny irreversible effect as shown in Fig. 3-5(b). The $P_v$ at $H_{dc} = 0$ has only a 16% variation after the large loop is applied. The hysteresis loss
phenomenon was verified experimentally by applying a 3F46 toroid in a buck converter switched with $V_{in} = 2.4 \text{ V}$, $V_o = 1.2 \text{ V}$, $f_s = 2 \text{ MHz}$, and $I_{oMax} = 2.4 \text{ A}$. The magnetic core operates with $B_m = 17 \text{ mT}$ and $H_{dc\_Max} = 100 \text{ A/m}$. The setup is shown in Fig. 3-6(a) and (b).

The difference between the core temperature and ambient temperature was recorded as the output current increased from 0 to $I_{oMax}$, and back to 0. The steady state was reached for each point by waiting at least 30 minutes. The winding loss was much lower than the core loss, as a result of the short wire.

![Fig. 3-6. A Buck converter for testing the core loss of the one-turn toroidal core; (c) measured thermal map at $I_o = 1.6 \text{ A}$.

The hysteresis loss density in Fig. 3-5(b) was then verified by the hysteresis temperature in
Fig. 3-7(a) and hysteresis loss in Fig. 3-7(b). The 3F46 has a negligible irreversible dc-biased loss since the temperature increased by only 1°C after the 100-A $H_{dc}$ loop was applied.

The 3F46 with a low core loss density and stable biased property was selected in this design. The dc-biased core loss, $P_{CL}$, is modeled by

$$P_{CL} = A_e l_e P_{v0} K_{dc}(H_{dc})$$  \hspace{1cm} (3-1)

where $A_e$ and $l_e$ are the equivalent cross-sectional area and length of a one-turn gapped core; $P_{v0}$ is the zero-biased core loss density; $K_{dc}$ represents the dc effect on core loss and is derived from Fig. 3-5(b). The maximum $H_{dc}$ in the analysis of Section 3.6 is less than 70 A/m, which is in the small loop of Fig. 3-5(b). Since the hysteresis feature of the small loop is not significant, the $P_v - H_{dc}$ curve of the small loop at $B_m = 20$ mT was averaged for simplification and fitted by

$$K_{dc}(H_{dc}) = 0.00053 H_{dc}^2 + 0.0098 |H_{dc}| + 1$$  \hspace{1cm} (3-2)

The $K_{dc}$ is usually treated as a factor independent of $B_m$ as demonstrated in [128] and [135]. The reason to choose $B_m = 20$ mT at this point, is $B_m = 15 - 26$ mT is used for the designs in Section 3.6.

### 3.4 Modeling of Winding Loss

The placement of the air gap, core structure, and winding dimensions are key factors that determine the ac winding loss. There are three types of gap placement: vertical one gap, vertical two gaps, and horizontal two gaps. One-turn inductors with these gap placements are shown in Fig. 3-8. The core with one vertical gap (Fig. 3-8(a)) is utilized for the commercial one-turn inductors in Fig. 3-3. The gap length is fixed and cannot be adjusted by spacers. As opposed to commercial inductors, a space exists between the winding and gap in Fig. 3-8(d) for a lower
fringing effect. The core with two vertical gaps (Fig. 3-8(b)), has two symmetric C-cores. The gap length could be easily controlled by inserting Kapton tapes between the two C-cores. The winding in Fig. 3-8(e) is located at the center of the window area for the minimum fringing effect. The core with two horizontal gaps (Fig. 3-8(c)) is compatible with the PCB winding and usually applied for embedded power supplies. The gaps are close to the edges of the winding in Fig. 3-8(f), inducing a higher ac winding loss than the other two cases [138]. This section focuses on modeling the ac resistance of vertical gaps. The ac resistance of one vertical gap is modeled first and then extended to two symmetrical gaps. Both are verified by 2-D finite element simulations.

Fig. 3-8. One-turn inductor with (a) one vertical gap, (b) two vertical gaps, and (c) two horizontal gaps; (d) – (f) corresponding cross sections.

The inductor current with an arbitrary waveform can be decomposed into several harmonic currents with a sinusoidal waveform by the Fourier transform. The total winding loss is obtained from the sum of winding loss under each harmonic frequency i·f, by
\[ P_{wt} = I_{dc}^2 R_{dc} + \sum_{i=1}^{\infty} I_{RMS@ifs}^2 R_{ac@ifs} \] (3-3)

where \( I_{dc} \) is the dc current and \( I_{RMS@ifs} \) is the \( i \)th-order harmonic RMS current. In practice, only the first several harmonics are considered since the \( I_{RMS@ifs} \) quickly decreases with frequency.

Ac resistance is modeled for the inductor with one vertical gap. The method described in [139] modeled the air gap as the line-current-density by the Fourier-decomposition in space, but it ignores the penetration depth and is not accurate for MHz applications. Reference [140] gives the formulas to describe the magnetic field strength in the window area but with the assumption of an infinite winding width and no penetration depth. This paper modifies the formulas in [140] to satisfy the boundary conditions for a finite winding width. The penetration effect is also included by using a curve fitted factor from finite element simulation.

The fringing field along the x-axis in the window area of Fig. 3-8(d) is given in [140] by

\[ H_{fringing,x}(x,y) = -\frac{H_g}{\pi} \left\{ \tan^{-1} \left( \frac{y l_g}{x^2 + y^2 - \frac{l_g^2}{4}} \right) + m \pi \right\} \] (3-4)

The fringing field along the y-axis is

\[ H_{fringing,y}(x,y) = \frac{H_g}{2\pi} \left\{ \ln \left( \frac{y^2 + \left( x + \frac{l_g}{2} \right)^2}{y^2 + \left( x - \frac{l_g}{2} \right)^2} \right) \right\} \] (3-5)

where \( H_g = 0.9 I_{ac}/l_g \), \( m = 0 @ x^2 + y^2 > \frac{l_g^2}{4} \) and \( m = 1 @ x^2 + y^2 < \frac{l_g^2}{4} \), \( I_{ac} \) is the amplitude of sinusoidal current. The fringing field is assumed independent of the frequency. On the top surface of the winding, \( x \) and \( y \) in (3-4) and (3-5) should satisfy \( y = l_{wg} \) and \( -w_w/2 \leq x \leq w_w/2 \).

The modeled \( H_{fringing,x} \) along the winding top surface is far below the simulated \( H_x \), as shown in Fig. 3-9(a), since the winding width \( w_w \) is not included in (3-4). The boundary conditions
between the winding and core in Fig. 3-8(d) should be considered. The $H_y$ at two sides, and the $H_x$ at the bottom surface of the winding, are zero because the winding is adjacent to the core, and the permeability is assumed infinity. According to Ampere’s law, the $H_x$ on the top surface of the winding is modified as

$$H_x(x) = \frac{I_{ac} H_{fringing,x}(x, l_{wg})}{\int_{-\frac{w_w}{2}}^{\frac{w_w}{2}} H_{fringing,x}(x, l_{wg}) dx}$$

(3-6)

The modified $H_x$ then matches with the simulated one, as shown in Fig. 3-9(a).

![Figure 3-9](image)

**Fig. 3-9.** Calculated and simulated normalized (a) $H_x$ and (b) $H_y$ along the top winding surface in Fig. 3-8(d) at $f_s = 2$ MHz with $l_g = 0.2$ mm, $w_c = 1.2$ mm, $w_w = 2$ mm, $h_w = 0.25$ mm, and $l_{wg} = 0.5$ mm.

The calculated fringing field along the $y$-axis, on the top surface of the winding, is compared with the simulated $H_y$ in Fig. 3-9(b). Notice that $H_y = 0$ at two sides and the center. A linear subtraction is applied on $H_{fringing,y}$ to ensure the boundary condition and symmetry.

$$H_y(x) = H_{fringing,y}(x) - 2xH_{fringing,y}\left(\frac{w_w}{2}\right)/w_w$$

(3-7)

A large discrepancy still exists for the modeled and simulated $H_y$, although the two sides can agree. An accurate formula of $H_y$ is difficult to develop, but numerical $H_y$ could be obtained easily by a finite element simulation. Furthermore, the impact of $H_y$ on the ac winding loss could also be corrected by using the simulation method. Those two steps are then combined into one correction
factor for simplification.

If only \( H_x \) exists, the ac winding loss is obtained by

\[
P_{\text{wac}} = \frac{w_w}{2 \sigma \delta} H_{x,\text{RMS}}^2 [141],
\]

where \( \sigma \) is the copper conductivity, \( \delta = 1/\sqrt{\pi f_0 \mu_0 \sigma} \) is the skin depth, and \( H_{x,\text{RMS}} \) is RMS value of \( H_x \) in \(-w_w/2 < x < w_w/2\). If the \( H_y \) effect is considered, \( H_{y,\text{RMS}}^2 \) multiplied by a correction factor \( K_{Hy} \) is added on \( H_{x,\text{RMS}}^2 \).

\[
P_{\text{wac}} = \frac{w_w}{2 \sigma \delta} \left( H_{x,\text{RMS}}^2 + K_{Hy} H_{y,\text{RMS}}^2 \right) \tag{3-8}
\]

The factor \( K_{Hy} \) depends on \( w_w/\delta \), as shown in Fig. 3-10(a), and could be fitted by

\[
K_{Hy} = \begin{cases} 
2.12 \times 10^{-6} \left( \frac{w_w}{\delta} \right)^3 - 4.197 \times 10^{-4} \left( \frac{w_w}{\delta} \right)^2 + 2.989 \times 10^{-2} \frac{w_w}{\delta} - 0.2726 & (10 < \frac{w_w}{\delta} < 65) \\
0 & (\frac{w_w}{\delta} \leq 10) \text{ and } K_{Hy} = 0.48 & (\frac{w_w}{\delta} \geq 65) 
\end{cases}
\tag{3-9}
\]

Ac and dc resistances are given by

\[
R_{ac} = \frac{2 P_{\text{wac}} l_c}{I_{ac}^2} \text{ and } R_{dc} = \frac{l_c}{\sigma w_w h_w} \tag{3-10}
\]

The modeled \( R_{ac}/R_{dc} \) with and without the \( H_y \) effect is shown in Fig. 3-10(b). They both agree with the simulated \( R_{ac}/R_{dc} \) at small \( w_w \) \((w_w/\delta = 10)\). As \( w_w \) increases, \( H_y \) is more significant, and \( K_{Hy} \) is effective to predict the additional loss caused by \( H_y \).

![Fig. 3-10. (a) Curve-fitted \( K_{Hy} \) and (b) modified \( R_{ac}/R_{dc} \) versus normalized winding width with \( l_{wg} = 0.1 \) mm and other specifications in Fig. 3-9.](image)

The \( K_{Hy} \) in (3-9) is obtained at \( l_g/\delta = 4 \) and \( l_{wg}/\delta = 2 \). After \( l_g \) and \( l_{wg} \) are extended to
2 < \frac{l_g}{\delta} < 13 \text{ and } \frac{l_{wg}}{\delta} > 2, \text{ the modeled } R_{ac}/R_{dc} \text{ can also agree with the simulated one with an error less than 10\%, as shown in Fig. 3-11. It is reasonable to assume that } K_{Hy} \text{ is independent of } l_g \text{ because the } R_{ac} \text{ is almost independent of } l_g, \text{ according to the simulation. In terms of } l_{wg}, \text{ the } H_y \text{ decreases with } l_{wg} \text{ according to (3-5). The } K_{Hy} \text{ is not important and could be considered independent of } l_{wg} \text{ at } l_{wg}/\delta >> 2.}

![Modeled and simulated R_{ac}/R_{dc} for the vertical one-gap inductor in Fig. 3-8(a) with (a) l_g = 0.1 mm, (b) l_g = 0.2 mm, (c) l_g = 0.3 mm, and (d) l_g = 0.6 mm; other dimensions are given in Fig. 3-9.](image)

Finally, the effective range with 10\% error for the model in (3-4)–(3-10) is as follows: \( w_c/l_g > 4, h_w/\delta > 4, 10 < w_w/\delta < 65, 2 < l_g/\delta < 12, \text{ and } l_{wg}/\delta > 2. \) The first constraint is required to ensure (3-4) and (3-5) are valid. The second constraint ensures that } R_{ac} \text{ could be considered
independent of \( h_w \) since the current density is crowded at the top surface of the winding. The other constraints are limited by the effective range of \( K_{Hy} \).

The analysis above is based on the vertical one-gap design in Fig. 3-8(a). The model could be easily extended to a vertical two-gap design in Fig. 3-8(b), due to the symmetric field and current distributions. The current excitation and gap length are halved in (3-4)–(3-10) for calculating the \( R_{ac} \) of each gap. The modeled \( R_{ac}/R_{dc} \) can also agree with the simulated one with an error less than 10\%, as shown in Fig. 3-12(a). The total \( R_{ac} \) is slightly lower than that of a one-gap design as demonstrated in Fig. 3-12(b). The horizontal two-gap core is also simulated and compared with the vertical gap designs, and it is almost constant with \( l_{wg} \). The reason for this is the \( H_y \) is dominant in the horizontal gap. Higher \( l_{wg} \) does not decrease \( H_y \) significantly; however, higher \( l_{wc} \) might be useful to reduce \( R_{ac} \) since \( H_y \) decreases with \( l_{wc} \).

![Modeled and simulated \( R_{ac}/R_{dc} \) for vertical two-gap inductor in Fig. 3-8(b) with \( h_w = 0.25 \) mm and \( l_g = 0.2 \) mm; (b) Simulated \( R_{ac}/R_{dc} \) for vertical one-gap inductor (Fig. 3-8(a)), vertical two-gap inductor (Fig. 3-8(b)), and horizontal two-gap inductor (Fig. 3-8(c)) with the same dimensions of \( l_g = 0.2 \) mm, \( w_c = 1.2 \) mm, \( w_w = 2 \) mm, \( h_w = 0.25 \) mm, \( l_g = 0.5 \) mm, \( h_w = 0.25 \) mm, \( l_{wc} = 0.2 \) mm, and \( l_g = 0.2 \) mm at \( f_s = 2 \) MHz.]

This model is also effective for high order harmonic current since the frequency effect is reflected by the skin depth \( \delta \). As the frequency increases, the \( \delta \) decreases, the \( l_g/\delta \) increases, and the \( w_w/\delta \) increases. The model was verified by simulation to be effective up to 8 MHz (4th order order
harmonic) with the error less than 11%, as demonstrated in Fig. 3-13.

![Graph showing modeled and simulated R\textsubscript{ac}/R\textsubscript{dc} versus frequency, parametric with w\textsubscript{w}, for vertical two-gap inductor in Fig. 3-8(b) with l\textsubscript{wg} = 0.5 mm and other dimensions in Fig. 3-12(a).]

3.5  Modeling of Core Loss and Inductance

Resonance exists in the rccBuck converter. The classical Steinmetz equations ($P_{v0}[W/m^3] = C_m f [Hz]^\alpha B_m [T]^\beta$) and RGSE method in [146] will not work since the voltage across L\textsubscript{ca/b} is neither sinusoidal nor rectangular. The MSE method in [143] and GSE method in [144] model are frequency-domain based, and the field needs to be integrated over an entire period for calculation. The iGSE method in [145] could solve an arbitrary waveform by using the transient dB/dt and steady-state $B_m$. The transient $B$ is not included in the iGSE model. Another method, the EEL model in [147], could solve the arbitrary waveform by using transient $B$, transient dB/dt, and steady-state $B_m$. The EEL method was adopted by the finite element simulation software (Ansys Maxwell) and also selected in this work. The zero-biased core loss density is then modeled by

\[
P_{v0} = \overline{P_{vt}}
\]

\[
P_{vt}(t) = \frac{C_m (B_m \cos \theta)^{\beta - \alpha} (dB(t)/dt)^{\alpha}}{(2\pi)^{\alpha} \frac{\pi}{2} \left( \int_0^\frac{\pi}{2} \cos^\beta \theta \ d\theta \right)}
\]
\[ \cos \theta = \sqrt{1 - \left( \frac{B(t) - B_{dc}}{B_m} \right)^2} \] (3-13)

where \( B_{dc} = \frac{B_{max} + B_{min}}{2}, B_m = \frac{B_{max} - B_{min}}{2} \); \( B_{\text{max/min}} \) is the maximum/minimum flux density in a switching cycle.

The transient flux density \( B(t) \) is integrated from inductor voltage \( v_L \) by

\[ B(t) = \frac{\int v_L(t) \, dt}{A_e} \] (3-14)

By observing the simulated \( B \) of the one-turn inductor in Fig. 3-14, the equivalent magnetic length \( l_e \) and cross-sectional area \( A_e \) are approximated by

\[ l_e = 2w_w + 2l_{wg} + 2h_w + \frac{\pi w_c}{2} - l_g \] (3-15)

\[ A_e = \left( w_c + \frac{l_g}{2} \right) l_c \] (3-16)

The cross-sectional area \( A_e \) is extended by \( l_g/2 \) with the consideration of the leakage flux in the air. The \( l_e \) in (3-15) and \( A_e \) in (3-16) are utilized for calculating the flux density in (3-14) and core loss in (3-1).

Fig. 3-14. Simulated B for two-vertical gap inductor with unit current excitation, \( w_w = 2 \) mm, and other specifications in Fig. 3-12(a).

The zero-biased time-domain core losses calculated by (3-1), (3-2), and (3-11)–(3-16) match
with the simulated time-domain core losses in Fig. 3-15(b). The resonant inductor $L_{ra}$ has a higher core loss than that of $L_{ob}$, as a result of the higher volt-second (Fig. 3-15(a)).

![Graphs showing simulated voltage waveforms and modeled vs. simulated core losses.](image)

**Fig. 3-15.** (a) Simulated voltage waveforms for the designed vertical two-gap inductors in Table 3-3. (b) Modeled and 2D-transient-simulated core losses without dc effect.

The dc and maximum magnetic field strength are approximated by

$$H_{dc} = \frac{I_{dc}}{l_g \mu_r} \quad (3-17)$$

$$H_{max} = \frac{I_{pk}}{l_g \mu_r} \quad (3-18)$$

where $I_{dc}$ is the dc current and $I_{pk}$ is the peak current; both are derived from circuit simulation or a state-space model. The $H_{dc}$ determines the dc effect of core loss in (3-2). The $H_{max}$ is the worst operating condition for the core. In magnetic design, $H_{max}$ is selected first, and $H_{dc}$ is calculated accordingly.

The inductance of a vertical two-gap core in Fig. 3-8(b) is calculated by

$$L_{2gaps} = \frac{\mu_0 (w_c + l_g)(l_c + l_g)}{l_g} \quad (3-19)$$

Both core width and core length are extended by $l_g$ to include the fringing effect [161]. The modeled inductance agrees with the simulated one, as shown in Fig. 3-16.
Fig. 3-16. Modeled and simulated inductances for vertical two-gap inductor in Fig. 3-8(b) with $w_w = 2$ mm, $l_{wg} = 0.5$ mm, and other specifications in Fig. 3-12(a).

3.6 Parametric Analysis and Systematic Design of One-Turn Inductors

The one-turn inductors with inductances of $L_r = 69$ nH and $L_o = 38$ nH were designed in this section. Table 3-3 shows a systematic design. Steinmetz parameters are derived from the core loss densities at 1, 2, and 3 MHz in [133]. The peak current, dc current, and RMS current up to the $4^{th}$-order harmonic for $L_r$ and $L_o$ are calculated by a state-space model and Fourier decomposition. The core and winding parameters, i.e., $H_{max}$, $w_w$, $h_w$, $w_c$, and $l_{wg}$ are selected first, based on the design curves. The inductance model in Section 3.5 then can be applied to calculate other parameters. The winding loss and core loss are calculated by the models in Sections 3.4 and 3.5.

In the parametric analysis of $H_{max}$ (Fig. 3-17), $w_w$ (Fig. 3-18), $h_w$ (Fig. 3-19), and $l_{wg}$ (Fig. 3-20), $w_c$ is swept from 0.5 mm to 2.5 mm; $l_c$ is adjusted to meet the required inductance. Magnetic volume is related to those parameters by

$$V_{ol} = l_c(2w_c + w_w)(2w_c + l_{wg} + h_w)$$  \hspace{1cm} (3-20)
Table 3-3. Step-by-step design of one-turn gapped inductor with examples

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Design Method</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Specified</td>
<td>69 nH</td>
</tr>
<tr>
<td>Material</td>
<td>Selected from Fig. 3-4</td>
<td>3F46</td>
</tr>
<tr>
<td>$C_m$, $\alpha$, and $\beta$</td>
<td>Curve fitted from [133]</td>
<td>$C_m = 5.567 \times 10^6$, $\alpha = 2.21$, and $\beta = 2.29$</td>
</tr>
<tr>
<td>$\mu_r$</td>
<td>From measurement</td>
<td>710</td>
</tr>
<tr>
<td>$I_{pk}$</td>
<td>State-space model</td>
<td>6.4 A</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>State-space model</td>
<td>1.0 A</td>
</tr>
<tr>
<td>$I_{RMS@fs}$</td>
<td>State-space model</td>
<td>2.93 A</td>
</tr>
<tr>
<td>$I_{RMS@2fs}$</td>
<td>State-space model</td>
<td>1.05 A</td>
</tr>
<tr>
<td>$I_{RMS@3fs}$</td>
<td>State-space model</td>
<td>0.53 A</td>
</tr>
<tr>
<td>$I_{RMS@4fs}$</td>
<td>State-space model</td>
<td>0.36 A</td>
</tr>
<tr>
<td>$H_{max}$</td>
<td>Selected from Fig. 3-17(a)</td>
<td>50 A/m</td>
</tr>
<tr>
<td>$w_c$</td>
<td>Selected from Fig. 3-17(c)</td>
<td>1.2 mm</td>
</tr>
<tr>
<td>$w_w$</td>
<td>Selected from Fig. 3-18</td>
<td>2 mm</td>
</tr>
<tr>
<td>$h_w$</td>
<td>Selected from Fig. 3-19</td>
<td>0.25 mm</td>
</tr>
<tr>
<td>$l_{wg}$</td>
<td>Selected from Fig. 3-20</td>
<td>0.5 mm</td>
</tr>
<tr>
<td>$l_g$</td>
<td>Calculated by (3-18)</td>
<td>0.2 mm</td>
</tr>
<tr>
<td>$H_{dc}$</td>
<td>Calculated by (3-17)</td>
<td>7.1 A/m</td>
</tr>
<tr>
<td>$K_{dc}$</td>
<td>Calculated by (3-2)</td>
<td>1.1</td>
</tr>
<tr>
<td>$l_c$</td>
<td>Calculated by (3-19)</td>
<td>7.6 mm</td>
</tr>
<tr>
<td>$R_{dc}$</td>
<td>Calculated by (3-10)</td>
<td>0.26 mΩ</td>
</tr>
<tr>
<td>$R_{ac@fs}$</td>
<td>Calculated by (3-4)–(3-10)</td>
<td>1.4 mΩ</td>
</tr>
<tr>
<td>$R_{ac@2fs}$</td>
<td>Calculated by (3-4)–(3-10)</td>
<td>1.9 mΩ</td>
</tr>
<tr>
<td>$R_{ac@3fs}$</td>
<td>Calculated by (3-4)–(3-10)</td>
<td>2.4 mΩ</td>
</tr>
<tr>
<td>$R_{ac@4fs}$</td>
<td>Calculated by (3-4)–(3-10)</td>
<td>2.8 mΩ</td>
</tr>
<tr>
<td>$P_{wt}$</td>
<td>Calculated by (3-3)</td>
<td>15.1 mW</td>
</tr>
<tr>
<td>$P_{CL}$</td>
<td>Calculated by (3-1), (3-2), and (3-11)–(3-17)</td>
<td>34.9 mW</td>
</tr>
<tr>
<td>$V_{ol}$</td>
<td>Calculated by (3-20)</td>
<td>106 mm³</td>
</tr>
</tbody>
</table>

The valley point exists for loss versus volume when $H_{max}$ is fixed, as shown in Fig. 3-17(a). Lower volume means smaller $w_c$ and higher ac flux density, which causes higher core loss. Higher volume means lower $l_c$ and causes higher winding loss. Higher $H_{max}$ usually corresponds to lower $l_g$, lower $l_c$, smaller size, and higher loss. The Pareto fronts in Fig. 3-17(a) represent the lowest
volumes when $H_{\text{max}}$ and $w_c$ are swept. As the magnetic volume increases on the front Pareto, $H_{\text{max}}$ would decrease, and $w_c$ would increase, as shown in Fig. 3-17(b) and (c). This design chose the knee point in Fig. 3-17(a), $H_{\text{max}} = 50$ A/m, for both $L_r$ and $L_o$. The corresponding $w_c$ is 1.2 mm. With this configuration, the total magnetic volume is 464 mm$^3$ for the two phases.

![Diagram](image)

Fig. 3-17. (a) Modeled inductor losses versus magnetic volume for $L_r$ and $L_o$ in Table 3-3, parametric with $H_{\text{max}}$; corresponding (b) $H_{\text{max}}$ and (c) $w_c$ versus magnetic volume on the Pareto fronts.

The loss versus magnetic volume parametric with $w_w$ is shown in Fig. 3-18(a). The sweeping parameter is still $w_c$. As the winding width $w_w$ increases, the loss would increase since $w_c$ needs to decrease to maintain the volume and induce higher ac flux density. The loss versus $w_w$ parametric with magnetic volume is shown in Fig. 3-18(b). The loss would increase dramatically at $w_w > 2.2$ mm and slightly for $w_w < 2.2$ mm. From a fabrication point of view, a small $w_w$, e.g., 1 mm, makes it difficult to assemble the core and winding. Here, $w_w = 2$ mm was selected for
both \( L_r \) and \( L_o \) for easy fabrication and low loss.

![Graph](image1)

**Fig. 3-18.** (a) Modeled inductor losses versus magnetic volume for \( L_r \) and \( L_o \) in Table 3-3, parametric with \( w_w \); (b) modeled loss versus \( w_w \), parametric with magnetic volume.

The winding thickness, \( h_w \), is selected according to the modeled loss-volume curves in Fig. 3-19(a). For \( L_r \), the dc current is negligible, and the ac winding loss is dominant. A higher \( h_w \) cannot reduce the ac winding loss at \( h_w \gg \delta \), as discussed in Section 3.4. A small winding thickness, \( h_w = 0.25 \) mm, was selected for \( L_r \).

![Graph](image2)

**Fig. 3-19.** (a) Modeled inductor losses versus magnetic volume for \( L_r \) and \( L_o \) in Table 3-3, parametric with \( h_w \); (b) modeled loss versus \( h_w \), parametric with magnetic volume.

The output inductor \( L_o \) conducts both high dc and ac current. Lower \( h_w \) leads to higher \( R_{dc} \) and higher dc winding loss. However, the loss is almost constant when \( h_w \) is higher than 0.5 mm,
as shown in Fig. 3-19(b), because the ac winding loss is dominant. Finally, \( h_w = 0.5 \) mm was selected for \( L_o \).

The most important parameter that affects the ac winding loss is \( l_{wg} \). The total loss reduces \( \sim 10 \) mW when \( l_{wg} \) increases from 0.25 mm to 0.5 mm, as illustrated in Fig. 3-20(a), but the loss reduction is negligible when \( l_{wg} \) increases from 0.5 mm to 0.75 mm. A continuous impact of \( l_{wg} \) on the total inductor loss is shown in Fig. 3-20(b). The minimum point, \( l_{wg} = 0.5 \), was chosen for \( L_r \) and \( L_o \) in this design.

![Fig. 3-20. (a) Modeled inductor losses versus magnetic volume for \( L_r \) and \( L_o \) in Table 3-3, parametric with \( l_{wg} \); (b) modeled loss versus \( l_{wg} \), parametric with magnetic volume.](image)

The modeled, 2D-transient-simulated, and 3D-transient-simulated inductances, winding losses, and core losses are compared in Table 3-4. The discrepancy of inductance is less than 5%. The modeled core loss can agree with the 2-D transient simulated loss but is smaller than the 3-D simulated one because the ac flux density along the winding direction is not uniform (Fig. 3-21(c)).

The 2-D simulated and modeled \( B_m \) is higher than that of the 3-D FEA at the center of the winding. This phenomenon could be understood by analyzing the magnetic field generated by a finite wire (scenario of 3-D FEA) and an infinite wire (scenario of 2-D FEA). The Biot-Savart law yields the magnetic flux density on the bisecting plane generated by a finite wire, is lower than the magnetic
flux density generated by an infinite wire [148].

Table 3-4. Modeled, 2-D and 3-D simulated inductances, winding losses, and core losses for one-turn inductors in Table 3-3

<table>
<thead>
<tr>
<th></th>
<th>Model</th>
<th>2-D Transient FEA</th>
<th>3-D Transient FEA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_r$</td>
<td>Inductance</td>
<td>69.0 nH</td>
<td>67.1 nH</td>
</tr>
<tr>
<td></td>
<td>Winding</td>
<td>15.1 mW</td>
<td>16.3 mW</td>
</tr>
<tr>
<td></td>
<td>loss</td>
<td>34.9 mW</td>
<td>35.0 mW</td>
</tr>
<tr>
<td>$L_o$</td>
<td>Inductance</td>
<td>38.0 nH</td>
<td>37.1 nH</td>
</tr>
<tr>
<td></td>
<td>Winding</td>
<td>41.5 mW</td>
<td>45.4 mW</td>
</tr>
<tr>
<td></td>
<td>loss</td>
<td>29.0 mW</td>
<td>28.9 mW</td>
</tr>
</tbody>
</table>

![Diagram](image1)

Fig. 3-21. 3-D models of (a) $L_{ra/rb}$ and (b) $L_{oa/ob}$ with the specifications in Table 3-3; (c) 2-D and 3-D simulated $B_m$ along line A.

The winding loss from a 3-D FEA is higher than that of a 2-D FEA since the terminal effect is included. This is shown in Fig. 3-22(a) and (b). The one-turn inductor with one vertical gap in Fig. 3-8(a) has a lower fringing field at the terminals and may have a lower terminal loss.
Fig. 3-22. 3-D simulated averaged Ohmic losses for (a) $L_{ra/rb}$ and (b) $L_{oa/ob}$ in Fig. 3-21 with meshes.

The methods used in this section can be extended to other converters. The inductances need to be specified in Table 3-3. The RMS currents are obtained from the circuit analysis. The loss-volume Pareto front, parametric with $H_{\text{max}}$ (Fig. 3-17), is plotted by using the core loss and winding loss models. The $H_{\text{max}}$ is selected on the front according to the required loss and volume. The $w_w$, $h_w$, and $l_wg$ are selected on the loss-volume curves, e.g., Fig. 3-18 – Fig. 3-20. The design of other parameters follow the procedure in Table 3-3.

### 3.7 Experimental Verification

The inductors designed in Section 3.6 and commercial inductors with the same inductances are applied in the rccBuck converter to verify the efficiency improvement by magnetic design. A two-phase interleaved buck converter with commercial inductors was also fabricated as a reference design, to demonstrate the efficiency improvement by the RCC topology.

All converters have the same input/output capacitors and the same specifications in Fig. 3-1. With the capacitor $C_o = C_{in} = 8 \times 4.7 \mu \text{F}$ for the two phases, the peak-to-peak voltage is 15 mV across the output and 10 mV across the input for the rccBuck converter. The switches were realized by EPC2100 enhanced GaN half bridges offering $R_{\text{ds(on)}}$ of 8 m$\Omega$ for $M_{1a/b}$ and 2 m$\Omega$ for $M_{2a/b}$, and
a 30 V rating. Gate drivers were LM5113. The $C_r$ for one phase consists of $8 \times 33$ nF ceramic capacitors (Table 3-1) with ESR = 0.3 mΩ in total. The $C_{ra}$ and $C_{rb}$ were mounted and interleaved on two sides of the PCB, as shown in Fig. 3-23(a) and (b). The interleaving placement could reduce the parasitic inductance effectively [149]. The ground on the second and third layers provides a short path in the switching loop. Moreover, the ground can cancel the flux generated by the capacitor path (ina-sw b and inb-swa), further reducing the parasitic inductance.

![Fig. 3-23. (a) Top view and (b) side view of the components placement in the switching loop for the rccBuck converter; (c) 3-D layout model for Q3D simulation.](image)

The high-frequency switching loop inductors in the rccBuck converter are shown in Fig. 3-24(a). Those loop inductors and the $C_{oss}$ will cause ringing at the switch nodes when $M_{1a/b}$ or $M_{2a/b}$ are hard turned off. Since the GND, swa/b, and ina/b traces in Fig. 3-23(c) have a flux cancelling effect, the simulated inductance matrixes were used to calculate the equivalent loop inductances in Fig. 3-24(b)–(d). The simulated $L_{Cra-Crb}$ is 0.33 nH. The simulated $L_{Cra/b-GND}$ is 0.25 nH. The switching loop inductance of the rccBuck converter is higher than that of the buck converter in [150], 0.15 nH, owing to the multiple switching loops and more components.
Fig. 3.24. (a) RecBuck converter with switching loop inductances (b) \( L_{Cra-Crb} \), (c) \( L_{Cra-GND} \), and (d) \( L_{Crb-GND} \).

The real dimensions and measured inductances of the designed \( L_r \) and \( L_o \) are given in Fig. 3.25(a) and (b). The \( L_r \) and \( L_o \) have a similar footprint. The major difference is the gap length, 0.1 mm for \( L_r \) and 0.24 mm for \( L_o \). The gap was filled by Kapton tapes with 2 layers stacked for \( L_r \) and 5 layers stacked for \( L_o \); each layer has a thickness of 48 \( \mu \)m.

![Fig. 3.25. Prototypes of designed (a) \( L_{ra/rb} \) and (b) \( L_{oa/ob} \) with dimensions given in Table 3.3. (c) Commercial one-turn inductor from [136] for comparison.](image)

The output inductors \( L_{oa/ob} \) are on the top layer of the PCB as illustrated in Fig. 3.26(a); the input inductors \( L_{ra/rb} \) are on the bottom layer, opposite to \( L_{oa/ob} \). All inductors are placed close to the GaN switches to minimize the trace losses. The recBuck converter in Fig. 3.26(b) employs the same board as Fig. 3.26(a) but with commercial inductors. The commercial inductance is 36 nH for \( L_r \) and 70 nH for \( L_o \); all inductors have the same package, SLC7649, as shown in Fig. 3.25(c). The volume is almost two times the designed one.
Fig. 3-26. Prototypes of (a) GaN-based rccBuck converter with designed inductors and (b) commercial inductors; (c) GaN-based buck converter. All of them operate at $V_{in} = 12$ V, $V_o = 1.2$ V, and $I_o = 20$ A.

The output inductors of the two-phase buck converter in Fig. 3-26(c) are also commercial inductors with 230 nH inductance and the package shown in Fig. 3-25(c). The total magnetic volume for the buck converter is 532 mm$^3$, similar to that of rccBuck converter (Fig. 3-26(a)), 504 mm$^3$. Both converters employ the same GaN switches, drivers, and filter capacitors. The rccBuck converter has more $C_r$, but with negligible volume. The overall volumes of the two converters are almost the same if the layout is optimized. The active volume of the rccBuck converter (Fig. 3-26(a)) is $17 \times 23 \times 7.6$ (height) = 2972 mm$^3$, smaller than that of the buck converter (Fig. 3-26(c)), $20.4 \times 29.1 \times 5.8 = 3443$ mm$^3$.

ZVS is achieved for all switches within an entire load range. The waveforms of the drain-to-source voltages and gate voltage at nominal load ($I_o = 20$ A) and light load ($I_o = 5$ A) are shown in Fig. 3-27. The switch node voltage $v_{swa}$ has a clean waveform and low noise. The tiny ringing of $v_{ds1a}$ is caused by the hard turn-off of $M_{1a}$. The maximum voltage stress is 24.8 V for $M_{1a}$ and 12 V for $M_{2a}$. 

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3.7.1 Efficiency Measurement

The measured peak efficiency is 88.2% for the rccBuck converter with the designed inductors and 86.1% for the same converter with commercial inductors, both at 20 A and 2 MHz (Fig. 3-28). The higher switching frequency, 2.5 MHz, improves the light-load efficiencies as the circulating current is reduced. The peak efficiency of the buck converter with commercial inductors is 87.2%, 1% lower than that of the rccBuck converter with designed inductors.

Fig. 3-27. Measured voltage waveforms for the rccBuck converter in Fig. 3-26(a) at (a) $I_o = 20$ A and (b) $I_o = 5$ A.
A circuit simulation was performed to estimate the conduction, switching, and driving losses. Core and winding losses for customized inductors were obtained from finite-element simulation. The commercial inductors losses were calculated by the online tool [137]. Finally, the loss breakdown at 20 A is summarized in Fig. 3-29. The most significant loss of the buck converter is the switching loss of the active GaN, $P_{\text{swh}}$, since it is hard switched. The rccBuck converter has much lower switching losses thanks to ZVS for all switches. The conduction loss of synchronous GaN, $P_{\text{condl}}$, is the main loss for rccBuck converter. New diodes with lower rating and lower $R_{\text{ds(on)}}$ could be helpful in reducing $P_{\text{condl}}$. The two converters have the same driving loss since the switches and frequencies are the same. The winding and core losses are much lower than the conduction and driving losses in this design, revealing a potential improvement of power density by core size reduction. The other loss, $P_{\text{other}}$, includes the trace loss and dead-time loss. The rccBuck converters have higher $P_{\text{other}}$ than the buck converter, owing to higher current ripple and higher trace loss. The commercial inductors used in the rccBuck converter have higher ac winding loss and core loss compared with the designed inductors, decreasing efficiency by ~2%.
Fig. 3-29. Simulated loss breakdown for the converters in Fig. 3-26 at $V_{in} = 12$ V, $V_o = 1.2$ V, and $I_o = 20$ A.

As $V_{in}$ increases from 8 V to 12 V, the peak efficiency of the rccBuck converter drops from 90.0% to 88.2% (Fig. 3-30). As $V_o$ increases from 1 V to 1.5 V, the peak efficiency increases from 87.3% to 89.6% (Fig. 3-31). The rccBuck converter has ~1.1% higher efficiency than the buck converter under all variations, except at $V_{in} = 8$ V and $I_o < 10$ A. The hard-switched turn-on loss of the buck converter is relatively small at the low $V_{in}$ and low current. All these curves demonstrated the rccBuck converter is robust and maintains high efficiency with the variation of $V_{in}$ (8–12 V) and $V_o$ (1–1.5 V). The efficiency of the rccBuck converter is also higher than that of the state-of-the-art buck converter in [150] using the same half-bridge GaN module. The power level is expected to be improved since the efficiencies in Fig. 3-30 ascend up to the nominal load. The maximum efficiency of the POL converters is usually designed at the medium load.
Fig. 3.30. Measured efficiencies of the GaN-based buck converter in Fig. 3.26(c) and the rccBuck converters in Fig. 3.26(a), operating at $V_{in} = 8$–12 V and $V_o = 1.2$ V; the efficiency of the state-of-the-art single-phase buck converter in [150] was converted to two-phase efficiency for fair comparison.

Fig. 3.31. Measured efficiencies of the GaN-based buck converter in Fig. 3.26(c) and the rccBuck converters in Fig. 3.26(a), operating at $V_{in} = 12$ V and $V_o = 2.5$–3.5 V.

The rccBuck converter with the designed one-turn inductors is compared to the state-of-the-
art POL converters in Table 3-5. They have the same switching frequency, input voltage, and output voltage. The rccBuck converter has the advantages of low noise (benefit from ZVS) and slightly higher efficiency. However, its total volume is the highest due to the four inductors on two sides of the PCB. The layout of the rccBuck converter will be optimized in the future, and the total volume is expected to be comparable to the state-of-the-art products.

Table 3-5. Switch, volume, inductor, and efficiency comparison of the state-of-the-art hard-switched POL converters and rccBuck converter at $V_{in} = 12$ V, $V_o = 1.2$ V, and $f_s = 2$ MHz

<table>
<thead>
<tr>
<th>Reference</th>
<th>Topology</th>
<th>Switches</th>
<th>Phase #</th>
<th>Rated $I_o$ (A)</th>
<th>Inductor Package</th>
<th>Volume (mm$^3$)</th>
<th>Maximum Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>[24]</td>
<td>Buck</td>
<td>Si (CSD97370)</td>
<td>1</td>
<td>20</td>
<td>PCB inductor</td>
<td>12×20×4</td>
<td>85.1%</td>
</tr>
<tr>
<td>[25]</td>
<td>Buck</td>
<td>GaN (IR)</td>
<td>1</td>
<td>20</td>
<td>LTCC substrate</td>
<td>15×21×3</td>
<td>86.0%</td>
</tr>
<tr>
<td>[26]</td>
<td>Buck</td>
<td>GaN (EPC2100)</td>
<td>1</td>
<td>20</td>
<td>Discrete L</td>
<td>18×23×6</td>
<td>87.6%</td>
</tr>
<tr>
<td>[22]</td>
<td>SCBuck</td>
<td>Si (CSD16411Q3)</td>
<td>2</td>
<td>10</td>
<td>Discrete L</td>
<td>13×30×4</td>
<td>86.1%</td>
</tr>
<tr>
<td>[23]</td>
<td>SCBuck</td>
<td>Si (TPS54A20)</td>
<td>2</td>
<td>10</td>
<td>Discrete L</td>
<td>10×16×2</td>
<td>87.1%</td>
</tr>
<tr>
<td>Fig. 3-26(a)</td>
<td>RccBuck</td>
<td>GaN (EPC2100)</td>
<td>2</td>
<td>20</td>
<td>Discrete L</td>
<td>17×23×8</td>
<td>88.2%</td>
</tr>
</tbody>
</table>

3.7.2 Conducted-EMI Measurement

The conducted-EMI spectra of the rccBuck converter was compared to that of the two-phase benchmark buck converter in [164]. The measurement schematic and setup are shown in Fig. 3-32. The test procedure followed [151]. Lines 1 and 2 were measured separately, and the scan with the highest graphical results at the fundamental frequency was selected. The 5-μH line impedance stabilization network (LISN) was TBOH01 [152]. The spectrum analyzer was Agilent E7402A. The experimental hardware is shown in Fig. 3-33. A large copper ground was under the tested converter and LISN.
Fig. 3-32. Schematic of conducted-EMI measurement for (a) rccBuck converter in Fig. 3-26(a) and (b) two-phase buck converter in [164] with $V_{in} = 12$ V, $V_o = 1.2$ V, $f_s = 2$ MHz, and $I_o = 20$ A.

Fig. 3-33. Experimental hardware with the schematics in Fig. 3-32.

The hard-switched buck converter has a ~340 MHz ringing in Fig. 3-34 when the active switch is turned on. That ringing causes a high amplitude of EMI beyond 100 MHz in Fig. 3-35. The spectra at the fundamental frequency are caused by the mismatched components. They are similar for the buck and rccBuck converters switching at 2 MHz. The rccBuck converter running at 2.5 MHz and $I_o = 5$ A has 6 dB lower amplitude at the fundamental frequency, thanks to the reduced current ripple. The high-frequency (100–500 MHz) noise of the rccBuck converter at $I_o = 20$ A is 15 dB lower than that of the buck converter, due to the ZVS of active switch and ZCS of the synchronous switch.
Fig. 3-34. Measured switch node voltage for the buck converter in Fig. 3-32(b) at (a) $I_o = 5$ A and (b) $I_o = 20$ A.

Fig. 3-35. Measured conducted EMI for the buck converter in Fig. 3-32 at (a) $I_o = 5$ A and (b) $I_o = 20$ A.

### 3.8 Conclusion

A conventional one-turn inductor cannot handle high ac flux, due to high core loss and high ac winding loss. This chapter describes how to reduce those losses through the selection of low-loss material and optimization of the core structure. The ferrite of 3F46 was recommended since it has the lowest and most stable core loss density at 2 MHz. The inductance, ac winding loss, and transient core loss of a one-turn gapped inductor were modeled. The inductance and loss models greatly reduced the calculation time compared to the finite-element simulation (FES) from 1.5
minutes to 0.12 seconds. A 0.25 mm distance between the gaps and winding was recommended to reduce $R_{ac}$ by >50% without sacrificing too much volume. Other parameters were selected according to the loss-volume front Pareto. A 12 V to 1.2 V rccBuck converter, switched at 2 MHz, was fabricated and demonstrated experimentally to achieve 88.2% efficiency at 20 A output by using the designed inductors. All switches have clean waveforms and low noise within load range, even with zero gate resistances. After the designed inductors were replaced by commercial one-turn gapped inductors, the efficiency degraded to 86.1%. The rccBuck converter with ZVS operation achieves ~15 dB lower conducted-EMI noise in 100 – 500 MHz than that of the hard-switched buck converter at the nominal load.
Chapter 4 Omni-Coupled Inductors for the RccBuck Converter

– Geometry, Analysis, Implementation, and Design

Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_e$ and $l_e$</td>
<td>Effective cross-sectional area and effective length</td>
</tr>
<tr>
<td>$F_{Lo}$ and $F_{Lr}$</td>
<td>Effective winding width considering eddy effect</td>
</tr>
<tr>
<td>$h_c$ and $w_c$</td>
<td>Total height and total width of twisted E-E core</td>
</tr>
<tr>
<td>$H_{dc}$</td>
<td>Dc magnetic field strength</td>
</tr>
<tr>
<td>$h_w$ and $h_1$</td>
<td>Winding thickness and window height</td>
</tr>
<tr>
<td>$J_{ac}$</td>
<td>Ac current density</td>
</tr>
<tr>
<td>$l_{g1}$, $l_{g2}$, and $l_{g3}$</td>
<td>Side gap length, center gap length, and horizontal gap length</td>
</tr>
<tr>
<td>$l_{wc}$ and $l_{ww}$</td>
<td>Horizontal distance from winding to core and horizontal winding space</td>
</tr>
<tr>
<td>$N_{pcb}$</td>
<td>Number of PCB layers</td>
</tr>
<tr>
<td>$P_{CL}$ and $P_{v0}$</td>
<td>Total core loss with dc effect and core loss density without dc effect</td>
</tr>
<tr>
<td>$P_{wt}$ and $P_{wac}$</td>
<td>Total winding loss and ac winding loss</td>
</tr>
<tr>
<td>$R_{dc}$ and $R_{ac}$</td>
<td>Dc an ac resistances</td>
</tr>
<tr>
<td>$R_{g1}$, $R_{g2}$, and $R_{g3}$</td>
<td>Reluctances of gaps ($l_{g1}$, $l_{g2}$, and $l_{g3}$)</td>
</tr>
<tr>
<td>$R_{gLo}$ and $R_{gLr}$</td>
<td>Reluctances of window areas ($L_o$ and $L_r$)</td>
</tr>
<tr>
<td>$V_{ol}$</td>
<td>Magnetic volume</td>
</tr>
<tr>
<td>$w_{c1}$, $w_{c2}$, and $w_{c3}$</td>
<td>Side core width, center core width, and top/bottom core thickness</td>
</tr>
<tr>
<td>$w_{Lo}$ and $w_{Lr}$</td>
<td>Winding width for $L_o$ and $L_r$</td>
</tr>
<tr>
<td>$\delta$</td>
<td>Skin depth</td>
</tr>
<tr>
<td>$\mu_0$ and $\mu_r$</td>
<td>Vacuum permeability and relative permeability</td>
</tr>
<tr>
<td>$\rho$</td>
<td>Copper resistivity</td>
</tr>
</tbody>
</table>

The input and output inductors of an rccBuck converter are coupled to shrink the core size while maintaining the converter efficiency. The steady-state currents of the Omni-coupled
inductors (OCI) are modeled by the decomposition of the common mode (CM) voltage and differential mode (DM) voltage. With this model, mutual and self-inductances are designed to achieve zero voltage switching (ZVS) for all switches within the entire load range. The OCI with specified inductances are realized by a twisted E-E core. The inductances of the twisted E-E core are modeled by a reluctance network, bearing in mind the eddy effect and fringing effect. The time-domain core loss is modeled by the equivalent elliptical loop (EEL) method. The winding loss is modeled numerically by a finite element simulation. Finally, winding and core dimensions were designed by Pareto fronts to minimize the total loss, within a volume smaller than that of discrete inductors. The related simulation files are given in Appendix F.

4.1 Introduction

The schematic of the rccBuck converter with Omni-coupled inductors is shown in Fig. 4-1(a). When $M_{1b,2a}$ is on and $M_{1a,2b}$ is off, the voltage is $-(V_{in} - 2V_o)$ for $v_{Lra}$ and $(V_{in} - 2V_o)$ for $v_{Lob}$. When $M_{1b}$ is off and $M_{2b}$ is on, the voltage is $V_o$ for $v_{Lra}$ and $-V_o$ for $v_{Lob}$. Therefore, the $L_{ra}$ and $L_{ob}$ have reversed voltages and current ripples as shown in Fig. 4-1(b) and (c). The intra-windings, i.e., $L_{ra}$ and $L_{rb}$, operate with a 180° phase shift because of the interleaved phases.

Fig. 4-1. (a) RccBuck converter with Omni-coupled inductors. Typical waveforms of inductor (b) voltages and (c) currents.

The OCI for an rccBuck converter is a leakage based coupled inductor, which is determined
by using the method in Section 1.4.1. If all mutual inductances decrease to zero, the OCI becomes a discrete inductor, and the rccBuck converter can still work. If the leakage inductance between \( L_{ra} \) and \( L_{ob} \) decreases to zero, the rccBuck converter cannot work, as a result of the infinity current ripple that is discussed in Section 4.2.

The leakage inductors of the OCI in Fig. 4-1 must conduct dc current since the input or output current has dc components (Fig. 4-1(c)). The mutual inductors \( L_{rarb} \) and \( L_{oaob} \) have no dc current. The mutual inductors \( L_{raob}, L_{rboa}, L_{raoa}, \) and \( L_{rbob} \) have dc current. Finally, the OCI of the rccBuck converter is a leakage based, \( L_{\text{mutual}} \) with dc and ac currents, \( L_{\text{leakage}} \) with dc current, in-phase, and interleaved coupled inductor, as shown in Table 4-1.

**Table 4-1. Classification of coupled inductors, including the OCI in rccBuck converter**

<table>
<thead>
<tr>
<th>Winding voltages</th>
<th>Current in</th>
<th>( L_{\text{mutual}} )</th>
<th>( L_{\text{leakage}} )</th>
<th>( L_{\text{mutual}} ) and ( L_{\text{leakage}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>In-phase</td>
<td>In-phase and interleaved</td>
<td>In-phase</td>
</tr>
<tr>
<td>Ac</td>
<td>Dc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dc</td>
<td>Dc &amp; ac</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ac</td>
<td>Ac</td>
<td>Line transformer, HB/FB based resonant converters [64], [65]</td>
<td>Phase-shifted Forward-Flyback with OCI [66], Multi-phase LLC with OCI [67]</td>
<td></td>
</tr>
<tr>
<td>Dc &amp; ac</td>
<td>Dc &amp; ac</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dc &amp; ac</td>
<td>Dc</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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The benefits of Omni-coupling include smaller inductor size, lower flux densities, and lower core loss. If PCB winding is feasible, the total module height could be reduced. The organization of this chapter is as follows: The Omni-coupled inductance matrix and the method of DM/CM decomposition are introduced in Section 4.2 from the circuit point of view. A preliminary design of coupling coefficients is given from the mathematical point of view. Section 4.3 compares several core and winding structures for the implementation of the OCI. The twisted E-E core is recommended. The inductance model, core loss model, and winding loss model, from the geometric point of view, are derived in Sections 4.4, 4.5, 4.6, respectively. With those models, the Pareto analysis is performed in Section 4.7 to minimize the total loss and the volume. The core dimensions, coupling coefficients, and inductances are studied along the Pareto fronts. The efficiency and EMI measurements are discussed in Section 4.8. The conclusion is given in Section 4.9.

4.2 Current-Ripple Model of Omni-Coupled Inductors (OCI)

The possible couplings among four inductors can be represented by the inductance matrix

\[
L_{\text{mat}} = \begin{bmatrix}
L_r & K_{rarb}L_r & K_{raoa}\sqrt{L_rL_o} & K_{raob}\sqrt{L_rL_o} \\
K_{rarb}L_r & L_r & K_{rbaoa}\sqrt{L_rL_o} & K_{rbob}\sqrt{L_rL_o} \\
K_{raoa}\sqrt{L_rL_o} & K_{rbaoa}\sqrt{L_rL_o} & L_o & K_{oaob}L_o \\
K_{raob}\sqrt{L_rL_o} & K_{rbob}\sqrt{L_rL_o} & K_{oaob}L_o & L_o \\
\end{bmatrix}
\] (4-1)

The instantaneous inductor voltages are related to the inductor currents by

\[
v_L = L_{\text{mat}} \frac{di_L}{dt}
\] (4-2)

where \(v_L = [v_{Lra}, v_{Lrb}, v_{Loa}, v_{Lob}]^T\) and \(i_L = [i_{Lra}, i_{Lrb}, i_{Loa}, i_{Lob}]^T\). The coupling coefficients in the \(L_{\text{mat}}\) represent three coupling mechanisms: inter-couplings (\(K_{rarb}\) and \(K_{oaob}\)), cross-couplings (\(K_{raob}\) and \(K_{rbob}\)), and self inductances (\(L_r\) and \(L_o\)).
and $K_{rboa}$), and intra-couplings ($K_{raoa}$ and $K_{rbob}$). The $K_{raoa} = K_{rbob}$ and $K_{raob} = K_{rboa}$ are satisfied since the two phases are symmetric. The inter-couplings are usually negative, and cross couplings are usually negative according to the knowledge from the in-phase and interleaved coupled inductors that are discussed in Section 1.4. The $L_r$ and $L_o$ are assumed to have the same self-inductances in the circuit analysis since they have strong couplings and symmetric one-turn structures in Section 4.3. The assumption of $K_{rarb} = K_{oaob}$ is also valid because of the symmetric design. Finally, there are only three independent coupling coefficients: $K_{rarb} (= K_{oaob})$, $K_{raob} (= K_{rboa})$, and $K_{raoa} (= K_{rbob})$.

The total inductor voltage is decomposed to differential-mode (DM) and common-mode (CM) voltages, as shown in Fig. 4-2(b) and (c). This decomposition transforms the interleaved voltages, e.g., $v_{Loa}$ and $v_{Lob}$, into in-phase voltages, so that current ripples can be calculated by using one voltage level.

![Fig. 4-2. (a) Inductor voltages in the rccBuck converter are decomposed to (b) CM voltages and (c) DM voltages.](image-url)
The DM voltage of \( v_{Loa} \) and \( v_{Lob} \) is \((v_{Loa} - v_{Lob})/2\), and the CM voltage is \((v_{Loa} + v_{Lob})/2\). Superposition is available for the DM and CM current ripples. This method was also demonstrated for a four-phase coupled inductor in [157]. According to (4-2), the current ripples under DM and CM are calculated by

\[
\begin{bmatrix}
\Delta I_{r,DM}, -\Delta I_{r,DM}, \Delta I_{o,DM}, -\Delta I_{o,DM}
\end{bmatrix}^T = L_{mat}^{-1} \begin{bmatrix} v_{Lr_{DM}}, v_{Lr_{DM}}, v_{LoaDM}, v_{LobDM} \end{bmatrix}^T \frac{D}{2f_s} \tag{4-3}
\]

\[
\begin{bmatrix}
\Delta I_{r,CM}, \Delta I_{r,CM}, -\Delta I_{o,CM}, -\Delta I_{o,CM}
\end{bmatrix}^T = L_{mat}^{-1} \begin{bmatrix} v_{Lr_{CM}}, v_{Lr_{CM}}, v_{LoaCM}, v_{LobCM} \end{bmatrix}^T \frac{1 - D}{2f_s} \tag{4-4}
\]

The DM voltage vector in (4-2) is \( \mathbf{v}_{L,DM} = [v_{Lr_{DM}}, v_{Lr_{DM}}, v_{LoaDM}, v_{LobDM}] = \frac{V_o}{D} [1, -1, 1, -1]^T \) by Fig. 4-2(c). Similarly, the CM voltage vector is \( \mathbf{v}_{L,CM} = [v_{Lr_{CM}}, v_{Lr_{CM}}, v_{LoaCM}, v_{LobCM}] = \frac{1-D}{D} V_o [-1, -1, 1, 1]^T \) by Fig. 4-2(b). The elements in each vector having the same magnitudes, simplify the derivation process.

Replacing the \( L_{mat} \) in (4-3) and (4-4) by (4-1), the DM and CM current ripples are calculated by

\[
\begin{bmatrix}
\Delta I_{r,DM} \\
\Delta I_{o,DM}
\end{bmatrix} = \begin{bmatrix}
\Delta I_{r_{DM}} \\
\Delta I_{o_{DM}}
\end{bmatrix} = \begin{bmatrix}
\Delta I_{r_{oDM}} \\
\Delta I_{o_{oDM}}
\end{bmatrix} = \begin{bmatrix}
\Delta I_{r_{bDM}} \\
\Delta I_{o_{bDM}}
\end{bmatrix} = \frac{V_o}{2f_s} \left[ \frac{(1 - K_{oaob})L_o + (K_{raob} - K_{raoa})\sqrt{L_rL_o}}{(1 - K_{raar})L_r + (K_{raoa} - K_{raob})\sqrt{L_rL_o}} \right] \tag{4-5}
\]

\[
\begin{bmatrix}
\Delta I_{r,CM} \\
\Delta I_{o,CM}
\end{bmatrix} = \begin{bmatrix}
\Delta I_{r_{CM}} \\
\Delta I_{o_{CM}}
\end{bmatrix} = \begin{bmatrix}
\Delta I_{r_{oCM}} \\
\Delta I_{o_{oCM}}
\end{bmatrix} = \begin{bmatrix}
\Delta I_{r_{bCM}} \\
\Delta I_{o_{bCM}}
\end{bmatrix} = \frac{(1 - D)V_o}{2f_s} \left[ \frac{(-1 - K_{oaob})L_o - (K_{raoa} + K_{raob})\sqrt{L_rL_o}}{(1 + K_{raar})L_r + (K_{raoa} + K_{raob})\sqrt{L_rL_o}} \right] \tag{4-6}
\]

The modeled DM and CM currents in (4-5) and (4-6) agree with the simulated ones from LTSpice, as shown in Fig. 4-3. The input self-inductance \( L_{r} \) and output self-inductance \( L_{o} \) are unbalanced on purpose. A negative \( K_{raob} \) is preferred since the current stresses are lower.
Fig. 4-3. Modeled current ripples under DM and CM in (4-5) and (4-6) are validated by LTspice, using the OCI with \( L_r = 120 \text{ nH} \), \( L_o = 150 \text{ nH} \), \( V_o = 3.3 \text{ V} \), \( D = 0.75 \), \( f_s = 2 \text{ MHz} \), \( K_{rARB} = -0.2 \), \( K_{oaob} = -0.3 \), and \( K_{raoa} = K_{rbob} = 0.1 \).

If \( L_r \) and \( L_o \) are designed with symmetrical windings, \( K_{rARB} = K_{oaob} \) and \( L_r = L_o \) are satisfied.

The DM and CM current ripples are simplified to

\[
\frac{\Delta I_{r,DM}}{\Delta I_{o,DM}} = \frac{V_o \left[ 1 - K_{rARB} + K_{oaob} - K_{raoa} \right]}{\left[ (1 - K_{rARB})^2 - (K_{raoa} - K_{oaob})^2 \right] 2f_s L_r}
\]

(4-7)

\[
\frac{\Delta I_{r,CM}}{\Delta I_{o,CM}} = \frac{(1 - D)V_o \left[ -1 - K_{rARB} - (K_{raoa} + K_{oaob}) \right]}{\left[ -(1 + K_{rARB})^2 + (K_{raoa} + K_{oaob})^2 \right] 2f_s L_r}
\]

(4-8)

The total current ripples under the DM and CM are

\[
|\Delta I_{r,DM}| + |\Delta I_{o,DM}| = \frac{V_o}{(1 - K_{raoa} - K_{rARB} + K_{oaob}) L_r f_s}
\]

(4-9)

\[
|\Delta I_{r,CM}| + |\Delta I_{o,CM}| = \frac{(1 - D)V_o}{(1 - K_{raoa} + K_{rARB} - K_{oaob}) L_r f_s}
\]

(4-10)

The current ripple \( \Delta I_{o,CM} \) in (4-8) is negative. The ZVS condition is only related to the sum of peak-to-peak current ripples of \( L_r \) and \( L_o \). Thus, only the absolute current ripples are considered in (4-9) and (4-10). The denominators of (4-9) and (4-10) are very close because \( 1 - K_{raob} \gg K_{rARB} - K_{raoa} \). The numerator of (4-9) higher than that of (4-10), yields the DM current ripple is dominant. The CM current ripple is zero at \( D = 1 \), which means there are no even harmonics.
However, the CM current cannot be ignored at small \( D \) since the numerator of (4-10) is comparable to that of (4-9) at \( D \approx 0 \).

The denominators of (4-9) and (4-10) are always non-negative according to the criterion for determining the realizability of the inductance matrix. This criterion states: a set of coupled inductors is physically available if and only if all of the eigenvalues of the inductance matrix are non-negative [158]. The requirement to ensure non-negative eigenvalues of \( L_{\text{mat}} \) in (4-1) is

\[
1 - K_{raob} \geq |K_{rarb} - K_{raoa}|
\]
\[
1 + K_{raob} \geq |K_{rarb} + K_{raoa}|
\]

(4-11)

The effective ranges of \( (K_{rarb} - K_{raoa}) \) and \( (K_{rarb} + K_{raoa}) \) versus \( K_{raob} \) are shown in Fig. 4-4. The limitations of \( K_{raob} \) and \( (K_{rarb} - K_{raoa}) \) in (4-11) can prove the denominators of (4-9) and (4-10) are non-negative. If only \( K_{raob} \) exists, namely, \( K_{rarb} = K_{raoa} = 0 \), \( K_{raob} \) is valid from -1 to 1. If four inductors are coupled with each other, namely, all couplings are not zero, the range of \( K_{raob} \) is narrower and limited by the difference between \( K_{rarb} \) and \( K_{raoa} \). For example, \( K_{raob} \) is limited by \(-1 < K_{raob} < -0.4\) at \( K_{rarb} = -0.7 \) and \( K_{raoa} = 0.7 \).

![Fig. 4-4. Effective ranges of \( K_{raob} - K_{raoa} \) and \( K_{raob} + K_{raoa} \) given by (4-11).](image)

The total peak-to-peak current of \( L_r \) and \( L_o \) is calculated by

\[
I_{pp,Lr} + I_{pp,Lo} = \frac{[2 - D](1 - K_{raob}) + D(K_{rarb} - K_{raoa})]V_o}{[(1 - K_{raob})^2 - (K_{rarb} - K_{raoa})^2]L_r f_s}
\]

(4-12)
The normalized total current ripple is $I_{ppN} = (I_{pp,lr} + I_{pp,lo})L_r f_s/V_o$. The impact of $K_{raob}$ and $(K_{rarb} - K_{raoa})$ on the $I_{ppN}$ parametric with $D$ is shown in Fig. 4-5. The modeled $I_{ppN}$ curves agree with the simulated ones. All curves achieved ZVS. A lower $I_{ppN}$ corresponds to a lower inductance $L_r$ and a smaller core size. Higher $K_{raob}$ reduces $I_{ppN}$ dramatically. For example, $I_{ppN}$ is reduced by 50% from $K_{raob} = 0$ to $K_{raob} = -0.96$ at $D = 0.8$ and $K_{raoa} - K_{rarb} = 0$.

![Fig. 4-5](image)

Fig. 4-5. Calculated and simulated normalized total current ripple versus $K_{raob}$ and $(K_{raoa} - K_{rarb})$ at (a) $D = 0.2$, (b) $D = 0.4$, (c) $D = 0.6$, and (d) $D = 0.8$. The design point is marked by $\bullet$ in (d). The simulated rccBuck converter is switched at $V_{in} = 12$ V, $I_o = 20$ A, $L_r = L_o = 120$ nH, $C_r = 40$ μF, and $f_s = 2$ MHz. The modeled $I_{ppN}$ agrees with the simulated $I_{ppN}$. Lower $I_{ppN}$ corresponds to lower $L_r$ and smaller core size.

From the self-inductance point of view, the design of $K_{raob} = -1$ with the minimum $I_{ppN}$ is preferred. However, a leakage inductance between $L_{ra}$ and $L_{ob}$ is required for stabilizing the circuit.
The capacitor \( C_{ra/b} \) and voltages source \( V_{in/o} \) may be shorted if the leakage inductance is zero, as illustrated in Fig. 4-6. If the resonant frequency of \( L_r \) and \( C_r \) is close to \( f_s \), the resonant frequency of the leakage inductors and \( C_r \) may exceed \( f_s \). The converter would have a high current ripple on the leakage inductor, even higher than that through the magnetizing inductors. This severe condition could be avoided by increasing \( L_{lk} (=L_{lra} + L_{lob}) \) or \( C_r \). The recommended resonant frequency of \( L_{lk} \) and \( C_r \) is \( \frac{1}{2\pi \sqrt{L_{lk} C_r}} = 0.5f_s \). The ESL of \( C_r \) is also beneficial for the stability since it is in series with \( L_{lk} \); however, the ESL causes high voltage spike when \( M_{1a} \) is turned off. The \( L_{lk} \) has no impact on such voltage spike and is more helpful than the ESL.

![Low-impedance paths](image)

**Fig. 4-6. Low-impedance paths (a) when one active switch (\( M_{1a/b} \)) is on and (b) when active switches are off.**

The design point in Section 4.7 (\( K_{raob} = -0.96, K_{raoa} - K_{raob} = 0.2 \)) is marked in Fig. 4-5(d). The high \( K_{raob} \) can be achieved when \( L_{ra} \) and \( L_{ob} \) are very close in the same winding window. During the implementation of the OCI, the \( K_{raob} \) and \( K_{raoa} \) have different signs and a similar magnitude, yielding \( K_{raoa} = 0.1 \) and \( K_{raob} = -0.1 \).
In Section 2.2, the ZVS transition has been analyzed for the rccBuck converter with discrete inductors. The formulas of the minimum inductor current ripple for ZVS should be modified if Omni-coupling is involved, but the analysis procedure of the OCI is similar to that of discrete inductors. The simplified $L_{eq}C_{oss}$ resonant circuit is shown in Fig. 4-7(c). For discrete inductors, the $L_{eq} = L_{r}/L_{o}$ is given in Sub-section 2.2.1. When couplings are involved, the $L_{eq}$ is related to the inductance matrix in (4-1) and the sub-circuit in Fig. 4-7(b).

![Fig. 4-7. (a) Sub-circuit of rccBuck converter with OCI during ZVS transition of $M_{1a}$; (b) simplified circuit; (c) equivalent $L_{eq}C_{oss}$ circuit.](image)

The capacitors $C_{ra}$ and $C_{rb}$ are assumed shorted because of $C_{ra/b} \gg C_{oss}$. The $V_{in}$ and $V_{o}$ are also shorted from the ac point of view. Comparing Fig. 4-7(b) and Fig. 4-7(c), $v_{Leq} = v_{Loa} = -v_{Lrb}$ is obtained. The voltage relationship between Fig. 4-7(b) and Fig. 4-7(c) is

$$v_{L} = [v_{Lra}, v_{Lrb}, v_{Loa}, v_{Lob}]^T = v_{1}^Tv_{Leq}$$  (4-13)

where $v_{1} = [0 \ -1 \ 1 \ 0]$. Similarly, the current relationship between Fig. 4-7(b) and (c) is

$$v_{1}i_{L} = i_{eq}$$  (4-14)

The current-voltage relationship of $L_{eq}$ is

$$v_{Leq} = L_{eq} \frac{di_{eq}}{dt}$$  (4-15)

The inductance $L_{eq}$ is derived from (4-1) and (4-13)–(4-15) by
\[ L_{eq} = (v_1 L_{mat}^{-1} v_1^T)^{-1} = \left[ 1 - K_{raob} - \frac{(K_{raoa} - K_{rarb})^2}{(1 - K_{raob})} \right] \frac{L_r}{2} \approx \frac{1 - K_{raob}}{2} L_r \] (4-16)

The \( V_{Lrb} \) is solved by

\[ v_L = [V_{in} - V_{ CRA}, V_{ Lrb}, V_{in} - V_o - V_{ CRb} - V_{ Lrb}, -V_o]^T = M v_{inc} - v_1^T V_{Lrb} \] (4-17)

\[ M = \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & -1 \\ 0 & -1 & 0 & 0 \end{bmatrix}, \quad v_{inc} = \begin{bmatrix} V_{in} \\ V_o \\ V_{ CRA} \\ V_{ CRb} \end{bmatrix} \] (4-18)

\[ v_1 i_L = 0 \text{ and } v_1 \frac{di_L}{dt} = v_1 L_{mat}^{-1} v_L = 0 \] (4-19)

\[ V_{ Lrb} = (v_1 L_{mat}^{-1} v_1^T)^{-1} v_1 L_{mat}^{-1} M v_{inc} = L_{eq} v_1 L_{mat}^{-1} M v_{inc} = -\frac{K_{raoa} - K_{rarb}}{1 - K_{raob}} V_o \] (4-20)

The \( V_{eq} \) is calculated by

\[ V_{eq} = -V_{in} + V_{ CRA} + V_{ CRb} + V_{ Lrb} = V_{in} - 2V_o - \frac{K_{raoa} - K_{rarb}}{1 - K_{raob}} V_o \] (4-21)

The minimum current for ZVS is

\[ I_{cosszvs} = \frac{2V_{eq} V_{in}}{Z_{eq}(V_{in} - V_o)} = \frac{2V_{eq} V_{in}}{\sqrt{L_{eq}/C_{oss}(V_{in} - V_o)}} \] (4-22)

The time for ZVS transition is

\[ t_{ZVS} = 2\pi \sqrt{L_{eq}/C_{oss}} \left( \frac{1}{4} + \arctan \frac{V_{in} - V_o - V_{eq}}{V_{eq}} \right) \] (4-23)

The calculated ZVS transition time \( (t_{cal}) \) agrees with the simulated one \( (t_{sim}) \) as demonstrated in Fig. 4-8. If \( V_{eq} \geq \frac{(V_{in} - V_o)}{2}, i_{Lrb} > i_{Loa} \) is required at \( t_1 \) for ZVS (Fig. 4-8(a)). If \( V_{eq} < \frac{(V_{in} - V_o)}{2}, i_{Lrb} = i_{Loa} \) at \( t_1 \) (Fig. 4-8(b)).
Fig. 4-8. Simulated inductor current and active MOSFET voltages ($v_{ds1a}$ and $v_{g1a}$) during ZVS transition at (a) $V_o = 3.40$ V and $K_{rarb} = K_{oaob} = -0.16$ and (b) at $V_o = 3.56$ V and $K_{rarb} = K_{oaob} = -0.3$. In both cases, the rccBuck converter operates with $V_{in} = 12$ V, $I_o = 20$ A, $L_r = L_o = 60$ nH, $C_{oss} = 3$ nF, $C_r = 4.8$ μF, $C_o = 10$ μF, $K_{raoa} = 0.12$, $K_{raob} = -0.74$, and $f_s = 2$ MHz.

The required inductance $L_r$ for ZVS increases with $V_o/V_{in}$, as shown in Fig. 4-9(a). The $t_{ZVS}$ also increases with $V_o/V_{in}$ since the time constant of $L_{eq}$ and $C_{oss}$ in (4-23) increases with $L_r$. The modeled $t_{ZVS}$ agrees with simulated $t_{ZVS}$ with an error less than 5%, as demonstrated in Fig. 4-9(b).

Fig. 4-9. (a) Self-inductance $L_r$ increases with $V_o/V_{in}$ in the rccBuck converter in Fig. 4-8(a) for ZVS and minimum current stress of OCI. (b) Calculated and simulated $t_{ZVS}$.

4.3 OCI Implemented by a Twisted E-E Core

The normal E-E core in Fig. 4-10(a) with negative couplings has the disadvantage of high winding losses. The normal twisted core in Fig. 4-10(b) has a smaller winding loss but at the
sacrifice of core volume. A combination of those structures, the twisted E-E core, is put forward in this section to implement the OCI in an rccBuck converter, having the benefits of small core size, low total loss, and easy fabrication. The PCB winding simplifies the fabrication work and reduces the module height.

![Diagram](diagram)

Fig. 4-10. Negatively-coupled inductors implemented by (a) E-E core with long winding path and (b) twisted core [159].

The one-turn gapped inductor is discussed in Chapter 3. The vertical gap was selected for the discrete inductors in the rccBuck converter due to the low ac resistance. However, the integration of the vertical-gapped inductor is not compatible with the PCB winding, as shown in Fig. 4-11. Although horizontal gaps may induce higher ac winding losses, they are compatible with the PCB winding. If a high $K_{maob}$ is required, five legs could be reduced to three legs, further reducing the fabrication difficulty. The normal E-E core with the PCB windings is then available for the OCI. The concept of the twisted core could be applied on the one-turn E-E core to reduce winding losses while realizing the required coupling coefficients.
Three basic winding/core patterns of the OCI are shown in Fig. 4-12. All cases have the desired negative $K_{raob}$. The normal E-E core with a short winding path can just realize a positive $K_{rarb}$ and $K_{oaob}$. A longer winding path could realize the negative $K_{rarb}$ and $K_{oaob}$ with the sacrifice of the winding loss (Fig. 4-12(b)). The input/output terminals for the two phases are located on the two sides of the OCI, inducing higher terminal losses. In order to realize negative $K_{rarb}$ and $K_{oaob}$ while maintaining the low winding path, two cores could be twisted to couple the flux in an opposite way as shown in Fig. 4-12(c). With a longer magnetic path instead of a longer winding path, the core loss may increase, but it has the minimum total loss because the winding loss and the negative $K_{rarb/oaob}$ are more important than the core loss.
Fig. 4-12. Omni-coupled inductors implemented by (a) a normal E-E core and positive $K_{rarb/oaob}$, (b) a normal E-E core and negative $K_{rarb/oaob}$, (c) a twisted E-E core and negative $K_{rarb/oaob}$.

The concept of the twisted core was proposed by [159]. The first-generation core structure is shown in Fig. 4-13(a). The bar cores surrounding the straight windings guide the magnetic fluxes generated by the two windings flow from opposite ways. The wasted space shown in Fig. 4-13(a) limits the height of this twisted core. In order to reduce the height, the core was compressed in the second-generation twisted core (Fig. 4-13(b)) [160]. The windings were bent accordingly to adapt to the core compression. A scalable three-phase twisted core is shown in Fig. 4-13(c). The inductor comprises three bent windings, an E-core and a TT-shaped core.

Fig. 4-13. (a) First-generation twisted core [158]; (b) second-generation twisted core with reduce height [159]; (c) three-phase twisted core [159].

The major drawback of the bent winding is it is incompatible with the PCB process. A twisted
E-E core with straight windings (compatible with the PCB process) is shown in Fig. 4-14. One can achieve a positive coupling or a negative coupling, depending upon the horizontal gap length, \( l_{g3} \). It is similar to the first-generation twisted core in Fig. 4-13(a) but with a reduced height. Since the twisted E-E core has a larger cross-sectional area, the core loss density of Fig. 4-14 is lower than that of Fig. 4-13(a). The normal twisted core is usually designed with \( K_{oaob} = -(0.5 - 0.8) \), while the twisted E-E core is designed with \( K_{raob} = -(0.1 - 0.3) \) when \( l_{g3} \) is comparable with \( l_{g1} \). If \( l_{g3} \) is zero, the twisted E-E core becomes a normal E-E core. If \( l_{g3} \) equals the winding width, the twisted E-E core becomes a normal twisted core in Fig. 4-13(a).

![Diagram](image)

*Fig. 4-14. (a) Twisted E-E core for two-phase buck converter comprises (b) four identical core pieces.*

The possible symmetric magnetic paths in the two-phase twisted E-E core are shown in Fig. 4-15. The leakage flux in Fig. 4-15(a) goes through the gaps \( l_{g1} \), \( l_{g2} \), and \( l_{g3} \). The positively coupled flux in Fig. 4-15(b) goes through the gaps \( l_{g1} \) and \( l_{g3} \). The negatively coupled flux in Fig. 4-15(c) goes through the gaps \( l_{g1} \) and \( l_{g2} \). The total coupling coefficient is determined by the sum of these effects. If \( l_{g3} \) is zero, the negatively coupled flux is zero, and the twisted E-E core becomes the normal E-E core. If \( l_{g3} \gg l_{g1} \), the magnetic flux prefers the negatively coupled path in Fig. 4-15(c), and the total coupling is negative.

At this point, the two-phase twisted E-E core cannot be scaled to more phases since the negatively coupled flux is developed based on two adjacent windings. If there are three windings,
e.g., \( w_1, w_2, \) and \( w_3, \) and the twisted E-E cores are applied for \((w_1, w_2)\) and \((w_2, w_3)\), the \( w_1 \) and \( w_3 \) would have a positive coupling instead of a negative coupling.

![Fig. 4-15. Symmetric magnetic flux paths in twisted E-E core: (a) leakage flux path, (b) positively coupled flux path, and (c) negatively coupled flux path.](image)

The OCI for the rccBuck converter is implemented by a two-phase twisted E-E core as shown in Fig. 4-16. Since high \( K_{raob} \) is desired, the crossed windings \( L_{ob} \) and \( L_{ra} \) are placed in the same winding window. The input coupling \( K_{rab} \) and output coupling \( K_{oaob} \) are similar because of the high \( K_{raob} \). The winding is implemented by one-turn multi-layer PCB traces. The PCB has four layers in this design. The thickness of each layer is 0.07 mm (2-oz copper). The top gapped E core and bottom gapped E core are the same but with a 180° rotation. The parasitic winding capacitance is negligible since the one-turn PCB windings are not overlapped vertically.

![Fig. 4-16. Assembly of the OCI for an rccBuck converter and corresponding dimensions.](image)

The structures of normal E-E cores with and without a center gap, and a twisted E-E core, are
compared in Fig. 4-17. In order to ease the fabrication of the E-E core, the gap lengths $l_{g1}$ and $l_{g2}$ are the same in Fig. 4-17(a). In order to avoid positive couplings of $K_{rafb}$ and $K_{oaob}$, the center gap length is zero in Fig. 4-17(b). Case 3 is a twisted E-E core with $l_{g1} = l_{g2}$. All cases achieve ZVS at nominal load ($I_o = 20$ A) and have a similar footprint and height.

The dimensions of the three cases in Fig. 4-17 are listed in Table 4-2. The winding dimensions are the same, and the major differences are the gap length and core width. A normal E-E core is just a special twisted E-E core with $l_{g3} = 0$. The side gap $l_{g1}$ is adjusted to realize required inductance and ZVS at the nominal load. The converter operates at $V_{in} = 12$ V, $V_o = 3.3$ V, $I_o = 20$ A, and $f_s = 2$ MHz.

<table>
<thead>
<tr>
<th>(mm)</th>
<th>$l_{g1}$</th>
<th>$l_{g2}$</th>
<th>$l_{g3}$</th>
<th>$w_{c1}$</th>
<th>$w_{c2}$</th>
<th>$w_{Lr}$</th>
<th>$w_{Lo}$</th>
<th>$h_1$</th>
<th>$l_c$</th>
<th>$l_{wc}$</th>
<th>$l_{ww}$</th>
<th>$h_w$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>0.24</td>
<td>0.24</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>1.2</td>
<td>3.2</td>
<td>1.5</td>
<td>8</td>
<td>0.2</td>
<td>0.2</td>
<td>0.07</td>
</tr>
<tr>
<td>Case 2</td>
<td>0.55</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>1.2</td>
<td>3.2</td>
<td>1.5</td>
<td>8</td>
<td>0.2</td>
<td>0.2</td>
<td>0.07</td>
</tr>
<tr>
<td>Case 3</td>
<td>0.144</td>
<td>0.144</td>
<td>0.67</td>
<td>2</td>
<td>2.5</td>
<td>1.2</td>
<td>3.2</td>
<td>1.5</td>
<td>8.1</td>
<td>0.2</td>
<td>0.2</td>
<td>0.07</td>
</tr>
</tbody>
</table>

The simulated coupling coefficients and self-inductances are shown in Table 4-3. All cases
have $K_{raob} \approx 1$ since $L_{ra}$ and $L_{ob}$ are in the same window. Case 1 has positive $K_{oaob}$ and $K_{rarb}$. Case 2 has zero couplings of $K_{oaob}$, $K_{rarb}$, and $K_{raoa}$ due to $I_{g2} = 0$. Case 3 has negative $K_{oaob}$ and $K_{rarb}$. The $K_{raoa}$ and $K_{oaob}$ always have different signs since the $L_{ra}$ and $L_{ob}$ are tightly coupled. In terms of self-inductances, case 3 has the minimum $L_{r}$ and $L_{o}$, corresponding to the lowest $I_{ppN}$ in Fig. 4-5.

**Table 4-3. Simulated coupling coefficients and self-inductances of the exemplary OCI in Table 4-2**

<table>
<thead>
<tr>
<th></th>
<th>$K_{raob}$</th>
<th>$K_{oaob}$</th>
<th>$K_{rarb}$</th>
<th>$K_{raoa}$</th>
<th>$L_{r}$</th>
<th>$L_{o}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>-0.977</td>
<td>0.33</td>
<td>0.35</td>
<td>-0.34</td>
<td>76.8 nH</td>
<td>75.2 nH</td>
</tr>
<tr>
<td>Case 2</td>
<td>-0.971</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>61.6 nH</td>
<td>58.3 nH</td>
</tr>
<tr>
<td>Case 3</td>
<td>-0.966</td>
<td>-0.1</td>
<td>-0.1</td>
<td>0.1</td>
<td>51.5 nH</td>
<td>52.6 nH</td>
</tr>
</tbody>
</table>

The calculated current waveforms and RMS values of the three cases are compared in Fig. 4-18. The couplings have a significant impact on the shape of the inductor current. In case 1, the positive couplings of $K_{rarb}$ and $K_{oaob}$ lead to the plateau and high RMS value of $i_{Lra}$. In case 2, the couplings of $K_{rarb}$ and $K_{oaob}$ are zero, and $L_{r}$ is slightly lower than $L_{o}$. The mutual inductance $M_{raob} \approx L_{r}$ leads to near-zero ripples of $i_{Lra}$ and $i_{Lrb}$, as shown in Fig. 4-18(b). This scenario is similar to the in-phase coupled inductor in the zero-ripple Cuk converter. The input inductor $L_{r}$ has a near-zero current ripple, but the $L_{o}$ has a high current ripple for realizing ZVS. The RMS current of $i_{Lob}$ for case 2 is higher than that of the other cases. The OCI of case 3 has the desired couplings (negative $K_{rarb}$ and $K_{oaob}$) and desired current waveforms (balanced current ripples and no plateau). The $I_{Lra,RMS}$ for case 3 and case 1 is the same, but the $i_{Lra}$ in case 3 has a higher peak-to-peak current. Since $(I_{ppLr} + I_{ppLo})$ is almost the same for all cases, the RMS current of $i_{Lob}$ in case 3 is the minimum. At light load, the ac winding loss is dominant, and the advantage of case 3 is more significant due to the minimum ac component.
Fig. 4-18. Calculated inductor current waveforms for the OCI of (a) case 1, (b) case 2, and (c) case 3 in Fig. 4-17, applied in the rccBuck converter with $V_{\text{in}} = 12$ V, $V_o = 3.3$ V, $I_o = 20$ A, and $f_s = 2$ MHz.

Conventional E-E cores have uniform ac flux densities, as shown in Fig. 4-19(a) and (b). The center leg has a smaller $B_m$ because of the flux-cancelling effect of the interleaved current ripples. The $B_m$ of case 3 is not uniform, since the side gap has a double cross-sectional area of the center leg, in the negatively coupled flux path (Fig. 4-15(c)). The ac flux density is crowded in the center.

Fig. 4-19. Simulated ac flux densities ($B_m$) for the OCI of (a) case 1, (b) case 2, and (c) case 3 in Fig. 4-17 with the specifications in Fig. 4-18.

One benefit of the OCI is the cancelling effect of the dc magnetic field strength, $H_{\text{dc}}$. Since the $L_{ra}$ and $L_{ob}$ have a strong negative coupling, the effective dc current of the OCI is $(I_o - I_{\text{in}})$, lower than that of the discrete output inductor, $I_o$. Fig. 4-20 shows the simulated $H_{\text{dc}}$ of the three cases. Case 3 has the minimum $H_{\text{dc}}$, thanks to the large $l_{g3}$ for blocking the dc flux. The distribution
of the $H_{dc}$ in case 3 is more uniform than that of $B_m$ in Fig. 4-19(c) since the flux paths for $H_{dc}$ are Fig. 4-15(a) and (b), while the flux paths for $B_m$ are Fig. 4-15(a) and (c). The negatively coupled flux path is only effective for the interleaved fluxes, and the positively coupled flux path is only effective for the in-phase fluxes.

![Simulated dc magnetic field strength ($H_{dc}$) for the OCI of (a) case 1, (b) case 2, and (c) case 3 in Fig. 4-17 with specifications in Fig. 4-18.](image)

The simulated winding losses and core losses of the three cases are compared in Fig. 4-21(a). The dc-bias effect is included in the core loss simulation. The twisted core has the highest core loss, owing to the highest $B_m$. The twisted inductor has the minimum winding loss, thanks to the lowest RMS current (Fig. 4-18) and the lowest ac resistance (Fig. 4-21(b)). The winding loss and core loss for cases 1 and 2 imply that the winding loss is dominant for the normal E-E cores. The E-E core with a negative $K_{carb}$ and a long winding path in Fig. 4-12(c), has a significant winding loss and should be avoided. The twisted E-E core with the smallest size (Fig. 4-17), and the minimum loss (Fig. 4-21(a)), was finally selected for the OCI in the rccBuck converter.
Fig. 4-21. (a) Simulated winding loss and core loss for three cases in Fig. 4-17 and the specifications in Fig. 4-18. (b) Comparison of flux and current density distributions under ac excitation with and without horizontal gap \(l_{g3}\). The \(l_{g3}\) reduces \(R_{ac}\) by \(\approx 50\%\).

4.4 Inductances and Coupling Coefficients Model

The objective of this sub-section is to derive the analytical formulas of mutual inductances, self-inductances, and coupling coefficients for the twisted E-E core in Fig. 4-17(c). The strategy is to calculate the reluctance of each region (the air gap or winding window) and then calculate the total equivalent reluctance of the entire network.

Core reluctances are not considered in the inductance calculation since the ferrite has a negligibly high permeability with \(\mu_r = 710 > 140\). If \(\mu_r < 140\), the gap reluctance is less than four times core reluctance, e.g., case 3 in Table 4-2, and the ferrite permeability cannot be neglected. The reluctances of the winding window areas are included since they provide the leakage flux paths.
The calculation of the side-gap reluctance is based on the gap dimensions in Fig. 4-22(a). The gap width and length are both extended by \( l_{g1} \) to consider the fringing effect [161]. The reluctance of \( l_{g1} \) is

\[
R_{g1} = \frac{l_{g1}}{(l_c + l_{g1})(w_{c1} + l_{g1})\mu_0}
\]  

(4-24)

Similarly, the reluctances of \( l_{g2} \) and \( l_{g3} \) are calculated by

\[
R_{g2} = \frac{l_{g2}}{(l_{c2} + l_{g2})(w_{c2} + l_{g2})\mu_0}
\]

(4-25)

\[
R_{g3} = \frac{l_{g3}}{(l_c + 1.5l_{g3} + w_{c2})(w_{c1} + h_2/2 + 0.5l_{g3})\mu_0}
\]

(4-26)

where \( l_{c2} = (l_c - l_{g3})/2 \) and \( h_2 = (h_c - l_{g2})/2 \).

Fig. 4-22. Dimensions used in the reluctance calculations for (a) side gap \( l_{g1} \), (b) center gap \( l_{g2} \), (c) horizontal gap \( l_{g3} \), (d) winding window of \( L_o \), and (e) winding window of \( L_r \).

The reluctance of the winding window consists of a copper region (\( w_{Lr} \) or \( w_{Lo} \) in Fig. 4-16) and an air region (\( l_{ww} \) and \( l_{wc} \) in Fig. 4-16). The air region can be ignored because of \( l_{ww/wc} < w_{Lr/Lo} \).
The window reluctances are approximated by

\[
R_{gL_o} = \frac{h_1 - N_{pcb} h_w + N_{pcb} h_w / F_{L_o}}{(l_c + h_1) w_{L_o} \mu_0} \approx \frac{h_1 - N_{pcb} h_w + N_{pcb} h_w / F_{L_o}}{(l_c + h_1) w_{L_o} \mu_0}
\] (4-27)

\[
R_{gL_r} = \frac{h_1 - N_{pcb} h_w + N_{pcb} h_w / F_{L_r}}{(l_c + h_1) (w_{L_r} - l_{g3}/2) \mu_0} \approx \frac{h_1 - N_{pcb} h_w + N_{pcb} h_w / F_{L_r}}{(l_c + h_1) (w_{L_r} - l_{g3}/2) \mu_0}
\] (4-28)

where \(N_{pcb}\) is the number of PCB layers; \(F_{L_r}\) and \(F_{L_o}\) are the factors that represent eddy effects.

The impact of the frequency on the flux distribution is shown in Fig. 4-23. The winding window is filled with the magnetic flux at dc excitation. As the frequency increases to 2 MHz, the ac flux is prevented from penetrating the winding by the eddy effect. The equivalent cross-sectional area of the winding window is then reduced. The corresponding reluctance increases, and the ac inductance is smaller than the dc inductance. In terms of the coupling coefficient, the \(K_{raob}\) under ac is much higher than that under dc since the ac flux is forced to go to the magnetic core and air gaps instead of the winding windows.

Fig. 4-23. Simulated current density and flux density distributions under dc and ac excitations, for the OCI with the dimensions in Table 4-2. The excitation is the sinusoidal current with an amplitude of 10 A for \(L_o\) and 2.75 A for \(L_r\).

The reduction of the effective cross-sectional area of winding windows is determined by the factor of \(F_{Lr/o}\). This factor is introduced in [162] and given by

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\[
F_{L_0} = \left| \frac{3I_{\text{mag}}(aw_{L_0} \coth(aw_{L_0}))}{\alpha^2 w_{L_0}^2} \right| \\
F_{L_r} = \left| \frac{3I_{\text{mag}}(aw_{L_r} \coth(aw_{L_r}))}{\alpha^2 w_{L_r}^2} \right|
\]

(4-29) (4-30)

where \( \alpha = \sqrt{2\pi f_s \mu_0 / \rho} \). The factor \( F_{L_r/o} \) decreases from 1 to 0 as the frequency increases from 0 to infinity. At 2 MHz, \( F_{L_0} = 0.02 \) for \( w_{L_0} = 3.2 \) mm and \( F_{L_r} = 0.06 \) for \( w_{L_r} = 1.2 \) mm.

The inductance calculation is based on the reluctance models in (4-24)–(4-30). All reluctances except the window reluctance of the winding under study are included in the calculation. For example, all reluctances except \( R_{g_{L_0}} \) are considered in the calculation of the self-inductance of \( L_0 \) (Fig. 4-24(a)).

The magnetic path and surrounding reluctances for \( L_{ab} \) are shown in Fig. 4-24(a). The total reluctance is \( R_{g_1} + R_{g_{Lr}} / / R_4 \), where \( R_4 = \frac{R_{g_1} / / R_{g_{Lr}} / / R_{g_{L0}} (R_{g_2} + R_{g_3}) + 2R_{g_2} R_{g_3}}{2 (R_{g_1} / / R_{g_{Lr}} / / R_{g_{L0}}) + R_{g_2} + R_{g_3}} \). The self-inductance of \( L_0 \) is obtained by

\[
L_0 = \frac{1}{R_{g_1} + R_{g_{Lr}} / / R_4} \\
\]

(4-31)

Similarly, the self-inductance of \( L_r \) is modeled by using the reluctance network in Fig. 4-24(b)

\[
L_r = \frac{1}{R_{g_1} / / R_{g_{L0}} + R_4} \\
\]

(4-32)

The reluctance network associated with the \( L_{ra}/L_{rb} \) is symmetric and independent of \( R_{g_2} \) as shown in Fig. 4-24(c). The mutual inductance \( L_{rarb} \) is related to \( L_{ra}/L_{rb} \) and \( L_r \) by

\[
L_{rarb} = 2(L_{ra}/L_{rb}) - L_r = \frac{1}{R_{g_3} + R_{g_1} / / R_{g_{L0}}} - L_r \\
\]

(4-33)

Similarly, the mutual inductance \( L_{oarb} \) is related to \( L_{oa}/L_{ob} \) and \( L_0 \) by
\[ L_{oaob} = 2L_{Loa} - L_o = \frac{1}{\frac{R_{g1}}{} + \frac{R_{g3}}{}/\frac{R_{gLr}}{}} - L_o \quad (4.34) \]

The inductance of \( L_{ra}/L_{ob} \) in Fig. 4-24(e) is \( L_{ob}/L_{ra} = \frac{1}{R_{g1}+R_4} \). The mutual inductance \( L_{raob} \) is obtained by

\[ L_{raob} = -L_{ob}/L_{ra} + \sqrt{(L_{ob}/L_{ra})^2 - L_{ob}/L_{ra}(L_{r} + L_{o}) + L_{r}L_{o}} \quad (4.35) \]

The mutual inductance \( L_{rbob} \) cannot be calculated by the approach of \( L_{rb}/L_{ob} \) because of the asymmetrical reluctance network, as shown in Fig. 4-24(f). Neither can the method for calculating \( L_{oaob} \) be used for calculating \( L_{rbob} \), since the \( L_{rb} \) and \( L_{ob} \) windings are separated by \( R_{g2}, R_{g3}, \) and \( R_{gLr} \). Fortunately, the reluctance path could represent the coupling coefficient. The flux generated by the \( L_{ob} \) has two paths to flow, the leakage path \( R_{gLr}-R_{g2}-R_{g3} \), and the coupled path \( R_{gLo}-R_{g1} \). The coupling coefficient could be represented by the ratio of the coupled flux over the total flux. The mutual inductance \( L_{rbob} \) is then obtained by

\[ L_{rbob} = \frac{-L_oR_{gLr}}{R_{g3} + R_{gLr} + \frac{2R_{gLr} + R_{g3} + R_{g2}}{R_{g3} - R_{g2}}(R_{g3} + R_{g1}/R_{gLr})} \quad (4.36) \]

The coupling coefficients among four inductors are calculated accordingly

\[ K_{rarb} = \frac{L_{rarb}}{L_r} \quad (4.37) \]

\[ K_{oaob} = \frac{L_{oaob}}{L_o} \quad (4.38) \]

\[ K_{raob} = K_{rboa} = \frac{L_{raob}}{\sqrt{L_rL_o}} \quad (4.39) \]

\[ K_{raoa} = K_{rbob} = \frac{L_{rbob}}{\sqrt{L_rL_o}} \quad (4.40) \]
The inductance equations (4-31)–(4-36) are verified by finite element simulation. The horizontal gap length $l_{g3}$ of case 4 in Table 4-4, is swept from 0 to 1 mm. The modeled inductances agree with the simulated ones, as demonstrated in Fig. 4-25. The discrepancy between them is less than 8%.
Table 4-4. Core dimensions of the twisted E-E cores under study

<table>
<thead>
<tr>
<th>(mm)</th>
<th>(l_{g1})</th>
<th>(l_{g2})</th>
<th>(l_{g3})</th>
<th>(w_{c1})</th>
<th>(w_{c2})</th>
<th>(w_{Lr})</th>
<th>(w_{Lo})</th>
<th>(h_{1})</th>
<th>(l_{c})</th>
<th>(l_{wc})</th>
<th>(l_{ww})</th>
<th>(h_{w})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 4</td>
<td>0.1</td>
<td>0.1</td>
<td>0.5</td>
<td>1.3</td>
<td>1.5</td>
<td>2</td>
<td>4</td>
<td>1.4</td>
<td>10</td>
<td>0.1</td>
<td>0.1</td>
<td>0.07</td>
</tr>
<tr>
<td>Case 5</td>
<td>0.15</td>
<td>0.15</td>
<td>0.75</td>
<td>2</td>
<td>2</td>
<td>1.5</td>
<td>3.5</td>
<td>1</td>
<td>10</td>
<td>0.3</td>
<td>0.3</td>
<td>0.07</td>
</tr>
<tr>
<td>Case 6</td>
<td>0.15</td>
<td>0.15</td>
<td>0.5</td>
<td>1.5</td>
<td>2.2</td>
<td>1.2</td>
<td>3.2</td>
<td>1.5</td>
<td>10</td>
<td>0.2</td>
<td>0.2</td>
<td>0.07</td>
</tr>
</tbody>
</table>

The self-inductances \(L_r\) and \(L_o\) are very close because most of the flux goes through the magnetic core and gaps, instead of the winding windows. This tendency is more significant in Fig. 4-25(b) due to the eddy effect as mentioned earlier. The mutual inductances \(L_{raoa}\), \(L_{oaob}\), and \(L_{raoa}\) intersect in the same point, \(l_{g3} = 0.27\) mm and \(L = 0\) nH. At the intersection, \(R_{g2} = R_{g3}\) is satisfied (Fig. 4-25), and the negatively coupled flux in Fig. 4-15(b) equals the positively coupled flux in Fig. 4-15(c). As a result, the windings in one window area are decoupled from the windings in the other window.

![Fig. 4-25. Simulated and modeled self and mutual inductances at (a) dc and (b) 2 MHz for the twisted E-E core of case 4 in Table 4-4.](image)

The modeled and simulated coupling coefficients are compared in Fig. 4-26. Their discrepancy is less than 10%. The input inductor \(L_{ra}\) and output inductor \(L_{ob}\) are loosely coupled \((-K_{raob} \approx 0.8)\) at dc and tightly coupled \((-K_{raob} > 0.9)\) at 2 MHz. Since the windings in the same
window have a strong coupling, the $K_{rarb}$, $K_{oaob}$, and $-K_{raoa}$ have negligible differences. Fig. 4-26 also implies that the polarities of $K_{rarb}$ and $K_{oaob}$ are controlled by $l_{g3}$, which could be understood by looking at the flux paths in Fig. 4-15. At small $l_{g3}$ ($R_{g2} < R_{g3}$), the flux prefers the path in Fig. 4-15(b), and the positive coupling is dominant. At large $l_{g3}$ ($R_{g2} > R_{g3}$), the flux prefers the path in Fig. 4-15(c), and the negative coupling is dominant. In terms of the cross coupling, a high $K_{raob}$ may induce low impedance paths in Fig. 4-6 and should be avoided. However, if the $K_{raob}$ is designed too low, the core size would be large. In the final design, $K_{raob}$ is around -0.95 so that both the self-inductances and the capacitance of $C_r$ are acceptable.

![Graph](image)

**Fig. 4-26.** Simulated and modeled coupling coefficients at (a) dc and (b) 2 MHz for the twisted E-E core of case 4 in Table 4-4.

In order to ensure a good accuracy of the modeled inductances and coupling coefficients, there are some limitations of the OCI dimensions. The core width, core length, core height, winding width, and window height, should be much larger than the gap length ($w_{c1} > 10 l_{g1}$, $w_{c2} > 10 l_{g2}$, $l_c > 10 l_{g3}$, $l_c > 10 l_{g1}$, $l_c > 10 l_{g2}$, $h_c > 10 l_{g1}$, $h_c > 10 l_{g2}$, $w_{Lz/o} > 5 l_{wc}$, $w_{Lz/o} > 5 l_{ww}$, $h_1 > 5 l_{g1}$, and $h_1 > 5 l_{g2}$). If the core or winding dimensions are beyond those ranges, the effective cross-sectional areas for calculating the reluctances in (4-24)–(4-30) should be revised.
This inductance model can also be applied for buck converters. The \( L_{ra} \) and \( L_{ob} \) could be combined as a single winding in the buck converter. Self-inductances and mutual inductances are calculated by using \( w_{Lr} = 0 \) and \( l_{ww} = 0 \).

### 4.5 Time-Domain Core Loss Model

The method to model the time-domain core loss of the discrete one-turn gapped inductors in Chapter 3 is also available for the twisted E-E core. The transient flux density is derived first, and the EEL method is applied to calculate the core loss density. The \( H_{dc} \) is also needed for calculating the dc-biased core loss. The challenge for modeling the core loss of the OCI is the non-uniform \( B_m \) as shown in Fig. 4-27(a). In order to simplify the calculation, the entire core is separated by homogeneous sections, as illustrated in Fig. 4-27(b). Each section is assumed to have a uniform flux density. Those sections are named by the following principles. The first number in the lower subscript of “C” means the order of the quarter piece, i.e., \( C_1, C_2, C_3, \) and \( C_4 \). Each quarter piece has four flux paths, e.g., \( \Phi_{ra,C1_1}, \Phi_{ra,C1_2}, \Phi_{ra,C1_3}, \) and \( \Phi_{ra,C1_4} \). The second number in the lower subscript of “C” then corresponds to the flux path, e.g., \( \Phi_{ra,C1_1} \) goes through \( C_{1_1} \), and \( \Phi_{ra,C1_2} \) goes through \( C_{1_2} \). The section \( C_{1_3.1} \) and \( C_{1_3.2} \) conduct the same flux, \( \Phi_{ra,C1_3} \), but have different cross-sectional areas. The procedure to calculate the core loss of each section is as follows: The flux generated by all windings in each region is calculated first by using the superposition theory. The flux density and core loss in each section are calculated by using the equivalent cross-sectional area and length. The total core loss of the OCI is the sum of the core loss in each region.
Since the $L_{ra}$ and $L_{ob}$ have in-phase voltage waveforms, as shown in Fig. 4-2, and a strong negative coupling (Fig. 4-26), they can be treated as a single winding from the ac point of view. Symmetrically, the $L_{rb}$ and $L_{oa}$ are treated as another single winding. The fluxes in $C_1$ and $C_3$ generated by $v_{Lra}$ and $v_{Lrb}$ are listed in Table 4-5. The base flux $\Phi_{ra/b}$ is the integration of $v_{Lra/b}$. The total flux is the sum of fluxes from $v_{Lra}$ and $v_{Lrb}$. For example, the total flux of $C_{1_1}$ is $\Phi_{ra} + \Phi_{rb} - 2K_1\Phi_{rb}$.

**Table 4-5. Magnetic fluxes in $C_1$ and $C_3$ of Fig. 4-27(b)**

<table>
<thead>
<tr>
<th>Caused by $v_{Lra}$</th>
<th>$C_{1_1}$</th>
<th>$C_{1_2}$</th>
<th>$C_{1_3}$</th>
<th>$C_{1_4}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Phi_{ra}$</td>
<td>$K_2\Phi_{ra}$</td>
<td>$(1 - K_2)\Phi_{ra}$</td>
<td>$K_1\Phi_{ra}$</td>
<td></td>
</tr>
<tr>
<td>$\Phi_{ra} - 2K_1\Phi_{ra}$</td>
<td>$(1 - K_2 - K_1)\Phi_{ra}$</td>
<td>$(K_2 - K_1)\Phi_{ra}$</td>
<td>$K_1\Phi_{ra}$</td>
<td></td>
</tr>
<tr>
<td>$C_{3_1}$</td>
<td>$C_{3_2}$</td>
<td>$C_{3_3}$</td>
<td>$C_{3_4}$</td>
<td></td>
</tr>
<tr>
<td>$\Phi_{ra} - 2K_1\Phi_{ra}$</td>
<td>$C_{3_1}$</td>
<td>$C_{3_2}$</td>
<td>$C_{3_3}$</td>
<td>$C_{3_4}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Caused by $v_{Lrb}$</th>
<th>$C_{1_1}$</th>
<th>$C_{1_2}$</th>
<th>$C_{1_3}$</th>
<th>$C_{1_4}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Phi_{rb} - 2K_1\Phi_{rb}$</td>
<td>$C_{1_1}$</td>
<td>$C_{1_2}$</td>
<td>$C_{1_3}$</td>
<td>$C_{1_4}$</td>
</tr>
<tr>
<td>$\Phi_{rb}$</td>
<td>$K_2\Phi_{rb}$</td>
<td>$(1 - K_2)\Phi_{rb}$</td>
<td>$-K_1\Phi_{rb}$</td>
<td></td>
</tr>
</tbody>
</table>

The flux distribution in Table 4-5 is determined by the reluctance network in Fig. 4-24. For simplification, the winding window reluctances are not considered here. The ratio between

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Here the core loss of $C_{1,4}$ and $\Phi_{ra}$ is calculated by

$$K_1 = \frac{\Phi_{ra,C_{1,4}}}{\Phi_{ra}} = \frac{R_{g1}/R_{gLr}/R_{gL0} + R_{g2}}{2(R_{g1}/R_{gLr}/R_{gL0}) + R_{g2} + R_{g3}}$$

(4-41)

The ratio between $\Phi_{ra,C_{1,2}}$ and $\Phi_{ra}$ is calculated by

$$K_2 = \frac{\Phi_{ra,C_{1,2}}}{\Phi_{ra}} = \frac{l_c/2 + l_{g3}/2}{l_c + w_{c2} + l_{g3}} K_1$$

(4-42)

The fluxes through $C_1$ and $C_3$ could be expressed by using $K_1$, $K_2$, $\Phi_{ra}$, and $\Phi_{rb}$. It is noted the $v_{Lra}$ and $v_{Lrb}$ may generate fluxes with opposite directions in the same region. For example, the flux in the $C_{1,4}$ is $K_1 \Phi_{ra}$ from $L_{ra}$ and $-K_1 \Phi_{rb}$ from $L_{rb}$.

The time-domain flux density of each region is calculated by

$$B(t) = \frac{\Phi_{ra}(t) + \Phi_{rb}(t)}{A_e}$$

(4-43)

The equivalent cross-sectional areas $A_e$, and lengths $l_e$ for the regions in $C_1$, are shown in Table 4-6. The fringing effect is considered by extending the cross-sectional areas. The width ratio of $C_{1,2}$ and $C_{1,3,1}$ is determined by the flux ratio $K_2$ as shown in Table 4-6. Another factor 1.2 is applied for $C_{1,3,1}$, considering the non-uniform flux density distribution of $C_{1,3,1}$ in Fig. 4-27(a). Finally, the fluxes in Table 4-5 and the equivalent dimensions in Table 4-6, are applied in the EEL model in (3-11)–(3-13) to calculate the time-domain core loss.

| Table 4-6. Equivalent cross-sectional area and length for $C_1$ in Fig. 4-27(b) |
|-----------------|-----------------|-----------------|-----------------|-----------------|
| $A_e$           | $C_{1,1}$       | $C_{1,2}$       | $C_{1,3,1}$     | $C_{1,3,2}$     | $C_{1,4}$       |
| $l_e$           | $(w_{c1} + l_g)/(l_c + l_g)$ | $w_{c1}l_cK_2$  | $1.2w_{c1}l_c(1 - K_2)$ | $(w_{c1} + \frac{l_g2}{2})(\frac{l_c}{2} + w_{c2} + l_{g3})$ | $(w_{c1} + 2l_{g3})(l_c/2 + 2l_{g2} - \frac{l_g3}{2})$ |
|                 | $w_{c1}/2 + (h_1 - l_g)/2$ | $w_{Lr} + w_{L0} - l_{g3}$ | $w_{c2}/2 + l_{g3}$ | $w_{c1}/2 + (h_1 - l_g)/2$ |

The time-domain core loss of each section in $C_1$ is calculated by using Table 4-5 and Table 4-6. Here the core loss of $C_{1,1}$ is calculated as an example. The total flux through $C_{1,1}$ is first obtained.
by

\[ \phi_{C1,1}(t) = \phi_{C1,1,Lra}(t) + \phi_{C1,1,Lra}(t) = \phi_{ra}(t) + \phi_{rb}(t) - 2K_1\phi_{rb} \] (4-44)

\[ \phi_{ra}(t) = \int v_{lra}(t) dt \quad \phi_{rb}(t) = \int v_{lrb}(t) dt \] (4-45)

The flux density of \( C_{1,1} \) is calculated by (4-44) and Table 4-6

\[ B_{C1,1}(t) = \frac{\phi_{C1,1}(t)}{A_{e,C1,1}} = \frac{\phi_{ra}(t) + \phi_{rb}(t) - 2K_1\phi_{rb}}{(w_{C1} + l_{g1})(l_c + l_{g1})} \] (4-46)

The core loss density of \( C_{1,1} \) is calculated by the EEL method in [147]:

\[ P_{vt,C1,1}(t) = \left| \frac{C_m(B_m \cos \theta)^{\beta-\alpha}}{(2\pi)^{\alpha} \int_0^{\pi} \cos^\alpha \theta d\theta} \left( \frac{dB_{C1,1}(t)}{dt} \right)^{\alpha} \right| \] (4-47)

\[ \cos \theta = \sqrt{1 - \left( \frac{B_{C1,1}(t) - B_{dc}}{B_m} \right)^2} \] (4-48)

where \( B_{dc} = \frac{B_{max} + B_{min}}{2} \), \( B_m = \frac{B_{max} - B_{min}}{2} \); \( B_{max/min} \) is the maximum/minimum flux density of \( B_{C1,1}(t) \).

The time-domain core loss without dc bias effect of \( C_{1,1} \) is

\[ P_{v0,C1,1}(t) = P_{vt,C1,1}(t)A_{e,C1,1}l_{e,C1,1} \] (4-49)

where \( A_{e,C1,1} \) and \( l_{e,C1,1} \) are from Table 4-6. The core losses of \( C_{1,2}, C_{1,3.1}, C_{1,3.2}, \) and \( C_{1,4} \) follow the procedure of (4-44)–(4-49). The total time-domain core loss without dc bias effect of \( C_1 \) is

\[ P_{v0,C1}(t) = P_{v0,C1,1}(t) + P_{v0,C1,2}(t) + P_{v0,C1,3.1}(t) + P_{v0,C1,3.2}(t) + P_{v0,C1,4}(t) \] (4-50)

Since \( C_1, C_2, C_3, C_4 \) are symmetrical, the total time-domain core loss without dc bias effect of
the OCI is

\[ P_{v0t}(t) = 4P_{v0,c1}(t) \]  \hspace{1cm} (4-51)

The total core loss without dc bias effect of the OCI is

\[ P_{v0} = \overline{P_{v0t}(t)} \]  \hspace{1cm} (4-52)

The modeled and simulated \( P_{v0t}(t) \) for the OCI in case 3 and case 4 are compared in Fig. 4-28(a). Case 3 has a higher \( w_{c1/2} \), a lower ac flux density, and a lower core loss. The modeled \( P_{v0} \) versus \( w_{c1} \) for case 4 is compared with the simulated one in Fig. 4-28(b). The error is less than 10% at 1 < \( w_{c1} < 2.5 \). The error may be caused by the reluctances in (4-24)–(4-30), the flux distribution in Table 4-5, or the equivalent dimensions in Table 4-6.

The dc magnetic flux density \( H_{dc} \) is calculated by using the reluctance model in Fig. 4-29(a). The winding window reluctance is considered in this model because the flux is allowed to go
through the window area without the eddy effect. The $H_{dc}$ distribution is more uniform than the $B_m$ distribution. The assumption of the constant $H_{dc}$ inside the core is then reasonable.

The total dc current excitation of the OCI is

$$I_{dc, OCI} = I_o - I_{in} = (1 - V_o/V_{in})I_o$$  \hspace{1cm} (4-53)

The center leg has cancelled dc flux densities and is neglected in the reluctance model in Fig. 4-29(a). The $H_{dc}$ of the side gap $l_{g1}$ is

$$H_{g1} = \frac{B_{g1}}{\mu_0} = \frac{\phi_{g1}}{w_{c1}l_{c}\mu_0} = \frac{I_{dc, OCI}}{w_{c1}l_{c}\mu_0} = \frac{I_{dc, OCI}}{w_{c1}l_{c}\mu_0} = \frac{I_{dc, OCI}}{2w_{c1}l_{c}\mu_0(R_{g1}/R_{gL0} + R_{gLr} + R_{g3})}$$ \hspace{1cm} (4-54)

The $H_{dc}$ of the core in the rccBuck converter is solved by (4-53) and (4-54):

$$H_{dc, rccBuck} = \frac{H_{g1}}{\mu_r} = \frac{(1 - V_o/V_{in})I_o}{2w_{c1}l_{c}\mu_0(R_{g1}/R_{gL0} + R_{gLr} + R_{g3})}$$ \hspace{1cm} (4-55)

The simulated $H_{dc, rccBuck}$ is compared with the modeled $H_{dc, rccBuck}$ in Fig. 4-29(b). Case 4 has a higher $H_{dc}$, owing to the smaller thickness and smaller gap length. The calculated $H_{dc, rccBuck}$ of case 3 with $l_{g3}$ swept from 0.4 mm to 0.75 mm agrees with simulated $H_{dc}$ in Fig. 4-29. The discrepancy is less than 11%.

![Fig. 4-29. (a) Reluctance model for calculating $H_{dc, rccBuck}$; simulated $H_{dc, rccBuck}$ of case 3 in Table 4-2 and case 4 in Table 4-4.](image)
The total dc-biased core loss is calculated by
\[ P_{CL} = P_{vo} K_{dc} (H_{dc, rccBuck}) \] (4-56)

The dc effect \( K_{dc} \) is the material property given in (3-2). The dc magnetic field strength \( H_{dc, rccBuck} \) is modeled by (4-55).

Similar to the inductance model, the core loss model for the OCI in the rccBuck converter can also be extended to a buck converter. The zero-biased core loss model is the same. The \( H_{dc} \) is modified to
\[ H_{dc, buck} = \frac{I_o}{2w_c l_c \mu_r \mu_0 (R_{g1} // R_{gL0} // R_{gLr} + R_{g3})} \] (4-57)

Comparing (4-55) and (4-57), the coupled inductor for the buck converter has a higher \( H_{dc} \) because there is no dc cancelling effect between the input inductor and output inductor.

### 4.6 Parametric Analysis of Winding Loss

The significant winding loss is a common issue for PCB winding designs, especially in high-current and high-frequency applications. The loss breakdown in Fig. 4-21 yields the comparable core loss and winding loss for the designed OCI. However, if the OCI dimensions are not designed
carefully, the winding loss might increase dramatically. The winding loss modeling for the twisted E-E core is more difficult than that for the normal E-E core, since the twisted core cannot be simplified as a 2-D structure. Half of the L_r winding is exposed to l_g3, and the remaining half is hidden in the core. Finite element simulation is used in this sub-section to study the ac winding loss.

The objective of this sub-section is to figure out the effects of the l ww, l wc, h1, mutual resistance, PCB via, gap lengths, and core widths on the ac winding loss. The winding widths are fixed in the design. According to the current ratio, I_{L_r,dc}/I_{L_o,dc} = 1:2.7, and the PCB layout constraint, w_{L_r} = 1.2 mm and w_{L_o} = 3.2 mm are chosen for the later analysis.

From the dc point of view, the space between the winding and core stores no energy and sacrifices the volume. The example of case 5 in Table 4-4 has a very small h1 to minimize the volume. The distance between the two adjacent windings, l ww, and the distance between the winding and the core in the horizontal direction, l wc, have negligible impacts on R_{ac}, as shown in Fig. 4-31. The minimum l ww and l wc are limited by the PCB fabrication tolerance. A recommended design of the l ww and l wc is 0.2 ≤ l ww = l wc ≤ 0.4 mm.

The impact of the PCB vias on the ac resistance is studied by using the finite element simulation. The model of the twisted E-E core with PCB vias is shown in Fig. 4-32(a). The case with vias has a tiny advantage on R_{L_o} as shown in Fig. 4-32(b), since the vias help to balance the current in the PCB layers. The R_{L_r} has no such phenomenon because the horizontal gap l_g3 helps to balance the current of L_r, with or without vias.
The vertical distance between the winding and the core, \( h_1 \), is important for the ac winding loss, since the ac flux in the winding window is related to \( h_1 \). Fig. 4-33(a) shows that self-resistances, \( R_{Lo} \) and \( R_{Lr} \), decrease with \( h_1 \). This tendency of \( R_{Lo} \) is more significant because \( L_o \) has a larger aspect ratio and more non-uniform \( J_{ac} \). Conversely, higher \( h_1 \) induces higher \( K_{raob} \) in Fig. 4-33(b) and may cause the instability problem in Fig. 4-6. The recommended \( h_1 \) is 1.5 mm and is highlighted in Fig. 4-33(a).
Fig. 4-33. Simulated (a) ac resistances and (b) $K_{Raob}$ versus window height $h_1$ for case 5 (Table 4-4) with vias.

The mutual resistances are much lower than the self-resistances and could be assumed as zero in the later design. The vias, $l_{ww}$, and $l_{wc}$, have negligible effects on the ac resistance. Case 6 in Table 4-4 with proper designs of $l_{ww}$, $l_{wc}$, and $h_1$, is used for the analysis of the core width effect and gap length effect. The effects of the core widths $w_{c1}$ and $w_{c2}$ on the $R_{Lo}$ and $R_{Lr}$ are shown in Fig. 4-34. The $R_{Lo}$ increases with $w_{c1}$ but decreases with $w_{c2}$. The $R_{Lr}$ is almost constant. The $1 \text{ mm} \leq w_{c1} \leq 2 \text{ mm}$ and $1.5 \text{ mm} \leq w_{c1} \leq 2.5 \text{ mm}$ are the ranges of interest because of the small $R_{Lo}$. In those ranges, the variations of $R_{Lo}$ are less than 10% and are assumed independent of $w_{c1}$ and $w_{c2}$.

Fig. 4-34. Simulated self-resistances versus (a) $w_{c1}$ and (b) $w_{c2}$ for case 6 in Table 4-4.
The twisted E-E core has a lower ac winding loss than the normal E-E core (Fig. 4-21). The main reason is the presence of a horizontal gap \( l_{g3} \). The simulated ac current density \( (J_{ac}) \) of the twisted E-E core is shown in Fig. 4-35(a). The \( J_{ac} \) is high for one and half edges of \( L_r \), and two edges of \( L_o \). The lower \( J_{ac} \) on a half side of \( L_r \) is beneficial for the \( R_{Lr} \). The simulated flux lines and \( J_{ac} \) with and without \( l_{g3} \) in Fig. 4-35(b), also demonstrate the benefit of \( l_{g3} \). Without \( l_{g3} \), the flux lines are crowded near the vertical gap \( l_{g2} \) and induce high \( J_{ac} \) for four edges of the PCB windings. With \( l_{g3} \), the fringing flux moves to the right upper corner of the winding window, inducing high \( J_{ac} \) on only the first layer of the PCB winding. This phenomenon could also be explained by the theory of distributed air gaps mentioned in [163].

![Simulated current densities of \( L_r \) and \( L_o \) for case 6 in Table 4-4 with \( I_{ac} = 1 \) A for both \( L_r \) and \( L_o \). (b) Comparison of ac flux and current density distributions with and without horizontal gap \( l_{g3} \).](image)

Since the \( l_{g3} \) changes the shape of the flux lines, the ac resistance of \( L_r \) decreases with \( l_{g3} \) as shown in Fig. 4-36. The \( L_o \) is away from \( l_{g3} \) and almost independent of \( l_{g3} \). The vertical gaps \( l_{g1} \) and \( l_{g2} \) have a tiny effect on the \( R_{Lr} \) and \( R_{L0} \) with the variation of \( 0.15 \text{ mm} \leq l_{g1} = l_{g2} \leq 0.35 \text{ mm} \). On the other hand, the \( l_{g3} \) is related to the inductances in Fig. 4-25. The \( l_{g3} \) cannot be designed too high; otherwise, the self-inductances are difficult to satisfy, and the core size is large.
In the Pareto analysis, the winding widths are fixed, and the winding length $l_c$ determines the dc resistances. The effects of $w_{c1}$, $w_{c2}$, and $l_{g1}$ are not included in the winding loss model; only $l_{g3}$ and $l_c$ are included. Dc resistances of $L_r$ and $L_o$ of the baseline design (case 6) are $R_{dcLr} = 0.62 \, \text{m} \Omega$ and $R_{dcLo} = 0.23 \, \text{m} \Omega$. The dc resistances are scaled by a factor of $l_{c,\text{new}}/l_{c,\text{case6}}$ for a new design, where $l_{c,\text{new}}$ is the new $l_c$. The ac resistance $R_{acLo}$ is 7.05 mΩ for the case 6. The factor of $R_{acLo}/R_{dcLo}$ is fixed for the new designs since $R_{acLo}$ is almost independent of $l_{g3}$ (Fig. 4-36). For the resonant inductor $L_r$, the relationship between $R_{acLr}/R_{dcLr}$ and $l_{g3}/l_{g3,\text{case6}}$ is fit by

$$\frac{R_{acLr}}{R_{dcLr}} = -7.84 \left( \frac{l_{g3}}{l_{g3,\text{case6}}} \right)^3 + 25 \left( \frac{l_{g3}}{l_{g3,\text{case6}}} \right)^2 - 26.95 \frac{l_{g3}}{l_{g3,\text{case6}}} + 17.79 \quad (4-58)$$

Only fundamental frequency is considered here for simplification. The $R_{ac}$ for high-order harmonics could be derived using the same curve-fitting method. The total winding loss is calculated by

$$P_{wt} = 2[I_{dcLr}^2 R_{dcLr} + I_{dcLo}^2 R_{dcLo} + (I_{RMSLr}^2 - I_{dcLr}^2) R_{dcLr} + (I_{RMSLo}^2 - I_{dcLo}^2) R_{acLo}] \quad (4-59)$$

where $I_{dcLr/0}$ and $I_{RMSLr/0}$ are dc and RMS current of $i_{Lr/0}$, which is calculated by (4-2).

### 4.7 Loss-Volume Pareto Fronts

The complete diagram of the Pareto analysis for the twisted E-E core design is shown in
Fig. 4-37. The variations of $w_{c1}$, $w_{c2}$, $l_{g1}$, and $l_{g3}$ are applied on the baseline design, e.g., case 6. The sweeping ranges for those parameters are $\pm$ 40%. They are randomly generated in the allowed ranges for a new design. The coupling coefficients and self-inductances are calculated by (4-24)–(4-40). With those coupling coefficients, the required inductance for ZVS, $L_{r,ZVS}$, is calculated by (4-12). The $l_c$ and $L_{o,ZVS}$ are adjusted accordingly. If the new $l_c$ satisfies $l_{c\text{ new}} < l_{c\text{ max}}$, the design proceeds to the current and voltage waveforms calculation. The waveforms are imported into the models in (4-56) for the core loss calculation and (4-59) for the winding loss calculation. If $l_{c\text{ new}}$ exceeds $l_{c\text{ max}}$, or the index exceeds the maximum allowed cycles $N_{\text{max}}$, the current sweeping loop would stop, and a new design would start. The total magnetic volume is calculated by

\[ V_{ol} = l_c(2w_{c1} + h_1)(2w_{c1} + w_{c2} + 2w_{Lr} + 2w_{Lo} + 4l_{wc} + 2l_{ww}) \] (4-60)

The loss-volume Pareto fronts are obtained by following Fig. 4-37. The results with 400 design points are shown in Fig. 4-38. The loss tends to decrease with the volume; however, the loss cannot decrease further for the volume higher than 800 mm$^3$. The volume increase is caused by the $l_c$ increase or $w_{c1/2}$ increase. Higher $l_c$ induces higher winding loss. Higher $w_{c1/2}$ is beneficial for the core loss density but may induce lower $l_{g3}$ and higher winding loss. Finally, the recommended volume range is 700–900 mm$^3$. The final design is case 3, and it is compared to the normal E-E core designs, case 1 and case 2. Case 3 achieves lower volume and lower loss. Notice that all points in the 700-900 mm$^3$ range in Fig. 4-38 are lower than case 1 and case 2, yielding a robust design of the twisted E-E core. In terms of the model accuracy, the calculated total loss for case 3 is 400 mW, slightly lower than the simulated total loss, 415 mW.
**Initial design:** \( l_g1, l_g3, w_c1, w_c2, w_Lr, w_Lo, h_1, l_c, l_{wc}, l_{ww}, \) and \( h_w \) (e.g., case 6)

**Allowed variations:** \( l_g1, l_g3, \ldots \)

Generate \( l_g1, l_g3, w_c1, w_c2 \) randomly in allowed variation ranges \([- Δ, Δ]\)

Plot loss-volume Pareto front

Yes

\( i \leq N_{max} \)

\( i = i + 1 \)

Calculate magnetic volume by (4-60), core loss by (4-52), and winding loss by (4-59)

Calculate \( i_{Lza}, i_{Lob}, v_{Lza}, \) and \( v_{Lhb} \) for OCI with \( L_{r-zvs}, L_{o-zvs}, K_{raob}, K_{rarb}, K_{oaob}, \) and \( K_{raoa} \) by (4-2)

No

\( l_{new} = l_{c-max} \)

Calculate \( l_{r-zvs} = L_{r-zvs}/L_r, l_c, \) and \( L_{o-zvs} = l_{o-zvs}/L_o \)

Calculate \( L_{r-zvs} \) by (4-12)

**Fig. 4-37. Flow chart of Pareto analysis for a twisted E-E core applied in the rccBuck converter.**

**Fig. 4-38. Loss-volume Pareto front of the twisted E-E cores by running Fig. 4-37.**

The parameters on the Pareto front in Fig. 4-38 are studied in Fig. 4-39, including the \( K_{raob}, K_{rarb}, L_r, \) winding loss (WL), core loss (CL), total loss, core length (\( l_c \)), side-leg width (\( w_{c1} \)), and center-leg width (\( w_{c2} \)). As the \(|K_{raob}| \) and \(|K_{rarb}| \) decrease, the self-inductance \( L_r \) increases, and the
volume increases, validating the mathematical analysis in Fig. 4-5. As volume increases, winding loss increases, and core loss decreases. The core loss is higher than winding loss at volume < 700 mm$^3$. The core length and side-leg width increase with the volume, leading to core loss decrease and winding loss increase, respectively. The center-leg width is almost independent of the volume.

![Graphs showing various parameters vs. volume](image)

Fig. 4.39. Pareto front study: $K_{raob}$, $K_{arb}$, $L_r$, winding loss (WL), core loss (CL), total loss, $l_c$, $w_{c1}$, and $w_{c2}$, versus volume on the Pareto front of Fig. 4-38. Zero-phase digital filtering is applied to smoothen the curves.

### 4.8 Experimental Verification

The self-inductances and coupling coefficients of the designed OCI are listed in Table 4-2. The leakage inductance between $L_{ra}$ and $L_{ob}$ is $L_{lk} = 1.8$ nH. The resonant capacitance $C_r$ should satisfy $C_r \geq 14 \mu F$ to ensure $1/(2\pi \sqrt{L_{lk}C_r}) \leq 0.5f_s$. In this work, $C_r = 36 \mu F$ was selected with enough margin to avoid the instability. Other components of the OCI-rccBuck converter, e.g., the switches, input capacitor, and output capacitor, follow the design of the discrete-L-rccBuck converter. The organization of this section is as follows: The PCB layout of the OCI is introduced...
in Sub-section 4.8.1. The terminal resistances were simulated by the Q3D. The measured efficiencies of the rccBuck converter with the OCI and discrete inductors are compared in Sub-section 4.8.3. The ac and dc flux densities of the OCI and discrete inductors are also compared. The EMI performance of the OCI-rccBuck converter is discussed in Sub-section 4.8.4.

4.8.1 PCB Layout of OCI

Four one-turn windings of the designed OCI are implemented by a 4-layer 2-oz PCB with a 0.07 mm thickness for each layer. The layout is shown in Fig. 4-40. The high-frequency switching-loop layout follows Sub-section 3.7.1. The PCB windings of the OCI are close to GaN FETs to minimize the trace losses. The input windings \( L_{ra} \) and \( L_{rb} \) connect the switches by the 1\(^{st} \) and 4\(^{th} \) layers of the PCB. The output windings \( L_{oa} \) and \( L_{ob} \) conduct higher dc current and connect the switches through the 1\(^{st} \), 2\(^{nd} \), and 4\(^{th} \) layers of the PCB. Large ground (GND) planes are placed on the 2\(^{nd} \) and 3\(^{rd} \) layers to provide short return paths of the load current.

During the design of the OCI, the connections between the OCI and other components, e.g., GaN FETs and input/output capacitors, are assumed ideal. However, parasitic resistances exist in those connections and induce undesired trace losses. Each winding has three types of parasitic resistances as shown in Fig. 4-41, the winding resistances (\( R_{Lr} \) and \( R_{Lo} \)), the diode-to-inductor terminal resistances (\( R_{DL} \) and \( R_{SL} \)), and the inductor-to-capacitor terminal resistances (\( R_{Cin} \) and \( R_{Co} \)). The equivalent series resistances (ESR) of the \( C_{in} \) and \( C_{o} \) can be ignored since the ESRs are much lower than those trace resistances.
Fig. 4-40. PCB Layout of rccBuck converter with the twisted E-E core of the case 3 in Table 4-2 on (a) the 1st layer, (b) the 2nd layer, (c) the 3rd layer, and (d) the 4th layer.

The PCB layout in Fig. 4-40 was imported into the finite element simulation tool, Q3D, to extract the $R_{\text{Cin/C0}}$ and $R_{\text{SL/DL}}$. The winding resistances $R_{\text{Lr/o}}$ are simulated by another tool, Maxwell, since they are related to a more complicated structure, the twisted E-E core. The paths of the $L_o$ parasitic loop and $L_r$ parasitic loop are shown in Fig. 4-42. The traces of $R_{\text{Lo/Lr}}$ are exposed to the fringing fields and have the highest ac resistances. The return paths $R_{\text{Cin/C0}}$, have the longest traces.
and thus have the highest dc resistances. As mentioned earlier, the output windings $L_o$ conduct higher dc current and have larger winding widths. Tens of vias are employed in $R_{Lo}/R_{Lr}$ to help balance the current in the PCB layers.

![Fig. 4-41. Schematic of rccBuck converter with OCI and parasitic resistances.](image)

![Fig. 4-42. PCB traces corresponding to the parasitic resistances in Fig. 4-41 for (a) $L_o$ loop and (b) $L_r$ loop.](image)

The simulated parasitic resistances are shown in Table 4-7. The two phases are designed symmetrically, thus the parasitic resistances are almost balanced. The major terminal losses are $R_{Cin}$ and $R_{Co}$, owing to the long PCB traces. A possible improvement method is to add distributed capacitors along the return paths, to reduce the ac resistances. The dc resistances of $R_{Cin}$ and $R_{Co}$
will not contribute to the losses, since \( C_{in} \) and \( C_o \) conduct only ac current. Finally, the total copper loss of the designed OCI is 201 mW without terminal losses and 432 mW with terminal losses.

Table 4-7. Simulated winding resistances and trace resistances for the layout in Fig. 4-42

<table>
<thead>
<tr>
<th></th>
<th>Phase a</th>
<th>Phase b</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{dc} )</td>
<td>( R_{ac} )</td>
<td>( R_{dc} )</td>
</tr>
<tr>
<td>( R_{Cin} )</td>
<td>1.45 mΩ</td>
<td>2.96 mΩ</td>
</tr>
<tr>
<td>( R_{Lr} )</td>
<td>0.72 mΩ</td>
<td>3.56 mΩ</td>
</tr>
<tr>
<td>( R_{DL} )</td>
<td>0.86 mΩ</td>
<td>1.81 mΩ</td>
</tr>
<tr>
<td>( R_{Co} )</td>
<td>1.03 mΩ</td>
<td>2.65 mΩ</td>
</tr>
<tr>
<td>( R_{Lo} )</td>
<td>0.30 mΩ</td>
<td>6.30 mΩ</td>
</tr>
<tr>
<td>( R_{SL} )</td>
<td>0.26 mΩ</td>
<td>0.54 mΩ</td>
</tr>
</tbody>
</table>

4.8.2 Loss and Temperature-Rise Comparisons of OCI and Discrete One-Turn Inductors

The prototype of the rccBuck converter with the designed OCI is shown in Fig. 4-43(a). The PCB thickness is 0.8 mm. The active volume of the whole power stage is 17 mm × 23 mm × 5.5 mm = 2150 mm³. The resonant capacitors \( C_r \) and output capacitors \( C_o \) are close to the GaN switches to minimize the switching-loop inductances. Both \( C_o \) and \( C_{in} \) consist of four 4.7 \( \mu \)F X7R-0805 ceramic capacitors for each phase. The \( C_r \) consists of eight of the same type of capacitors for each phase. The switches were implemented by the monolithic half-bridge GaN module, EPC2100, the same module used in Chapter 3. The gate drivers were LM5113, and the driving signals were provided by two two-channel signal generators, AFG3102.

Fig. 4-43(b) shows one half of the designed twisted E-E core, which was constructed by two L-cores with a S-shape gap in the middle. The horizontal gap \( l_{g3} = 0.67 \) mm was implemented by 14 layers of Kapton tapes; each layer has the thickness of 48 \( \mu \)m. The vertical gap was filled by three layers of Kapton tapes. The magnetic material is ML91S from Hitachi Metals, which has a
similar core loss density as the material used in previous designs, 3F46. The volume of the entire twisted E-E core in Fig. 4-43(a) is \(16.5 \text{ mm} \times 8.1 \text{ mm} \times 5.5 \text{ mm} = 735 \text{ mm}^3\), which is about \(1/3\) of the power stage volume.

Fig. 4-43. (a) Prototype of the rccBuck with Omni-coupled inductors (case 3 in Table 4-2), switched at \(V_{in} = 12 \text{ V}, V_o = 3.3 \text{ V}, I_o = 20 \text{ A},\) and \(f_s = 2 \text{ MHz}\). (b) Prototype of the twisted E-E core (half) with the designed parameters in Table 4-2.

Four discrete one-turn gapped inductors with the inductances of \(L_{ra/b} = 160 \text{ nH}\) and \(L_{oa/b} = 95 \text{ nH}\) were fabricated as a reference design. They were applied in an rccBuck converter with the same specifications, \(V_{in} = 12 \text{ V}, V_o = 3.3 \text{ V}, I_o = 20 \text{ A},\) and \(f_s = 2 \text{ MHz}\). The dimensions of one discrete inductor are shown in Fig. 4-44(a). The magnetic material is 3F46. Each inductor has two symmetric gaps. The gap length is 0.15 mm for \(L_o\) and 0.09 mm for \(L_r\). The air gap of \(L_o\) was implemented by three layers of Kapton tapes, and the air gap of \(L_r\) was implemented by two layers of Kapton tapes. The round windings are placed in the center of the window areas for reducing the ac resistances. Other spaces in the window areas are filled by erasers as shown in Fig. 4-44(b). The total magnetic volume of the discrete inductors is \(4 \times 6.62 \text{ mm} \times 6.47 \text{ mm} \times 10 \text{ mm} = 1713 \text{ mm}^3\). Compared with those discrete inductors, the OCI achieves a 57% reduction of the magnetic volume.
Fig. 4-44. (a) Dimensions of the discrete one-turn gapped inductor used in a 12 V to 3.3 V rccBuck converter; (b) Prototypes of L_{ra}, L_{rb}, L_{oa}, and L_{ob} with one-turn round wires.

Fig. 4-45. Simulated ac flux densities of the (a) discrete L_{ra}, (b) discrete L_{rb}, and (c) OCI. Simulated dc magnetic field strengths of the (d) discrete L_{ra}, (e) discrete L_{rb}, and (f) OCI. Converter specifications are given in Fig. 4-43.

The ac flux densities B_m and dc magnetic field strengths H_{dc} of the discrete inductors and the OCI are compared in Fig. 4-45. The discrete inductors have a uniform B_m since the magnetic flux path is a single loop. The OCI has a negatively coupled flux path, inducing the non-uniform B_m. In terms of H_{dc}, the OCI has the minimum H_{dc} because of the input/output cancelling effect and a
large horizontal gap for blocking the dc flux. Lower $H_{dc}$ is beneficial for the core loss and makes the core more stable, as discussed in Section 3.3. The lower volume also contributes to the loss reduction. Finally, the total core loss of the OCI is 63% lower than that of the discrete inductors, as shown in Fig. 4-46.

One disadvantage of the OCI is the high winding loss, since the PCB winding has a high proximity loss, especially when the window height ($h_1$) is very small to satisfy the required leakage inductances. Other losses, e.g., conduction losses, switching losses, and driving losses, are the same, as shown in Fig. 4-46, due to the same switches and gate drivers.

![Simulated loss breakdown for the discrete-L-rccBuck converter in Fig. 4-48(d) and the OCI-rccBuck converter in Fig. 4-43(a) at $V_{in} = 12$ V, $V_o = 3.3$ V, $I_o = 20$ A, and $f_s = 2$ MHz.](image)

The measured thermal images in Fig. 4-47 imply the discrete inductors and the OCI operate at a similar temperature, ~50°C. The GaN temperature is only 60°C under natural cooling, which means this power stage has the ability to handle even higher current.
Fig. 4-47. Measured temperatures for the discrete-L-rccBuck converter in Fig. 4-48(d) and the OCI-rccBuck converter in Fig. 4-43(a) at $V_{in} = 12$ V, $V_o = 3.3$ V, $I_o = 20$ A, $f_s = 2$ MHz, and natural cooling.

Fig. 4-48. Prototypes of the (a) Si-based buck converter, (b) GaN-based buck converter, (c) Si-based rccBuck converter, and (d) GaN-based rccBuck converter, operating with the same conditions in Fig. 4-43(a).
4.8.3 Efficiency Comparison of OCI-rccBuck, Discrete-L-rccBuck, and Buck Converters

The efficiency of the OCI-rccBuck converter is compared to that of Si-based and GaN-based, buck and rccBuck converters in Fig. 4-48. The one-turn inductors in Fig. 4-44 were used for the rccBuck converters in Fig. 4-48(c) and (d). The commercial inductors with the inductance of 230 nH from Coilcraft were used for the buck converters. The switches were realized by a half-bridge Si module, CSD87351Q5D, for Si-based converters, and a half-bridge GaN module, EPC2100, for the GaN-based converters. They utilized the same input and output capacitances, $C_{in} = C_o = 47 \, \mu F$.

The measured efficiencies at the nominal condition for the OCI-rccBuck converter and the converters with discrete inductors, are shown in Fig. 4-49. The GaN-based buck converter has higher efficiency than the Si-based buck converter at light load, since GaN FETs have lower switching losses. As the load current increases to 20 A, the conduction loss is more significant, and the Si-based buck converter with lower $R_{ds(on)}$ tends to have higher efficiency. The OCI-rccBuck converter has the highest efficiency over the entire load range, which benefits from RCC, GaN FETs, low-loss magnetic material, and Omni-coupled inductors.
Fig. 4-49. Measured efficiencies of Si-based and GaN-based, buck and rccBuck converters in Fig. 4-48 and Fig. 4-43 with $V_{\text{in}} = 12$ V and $V_o = 3.3$ V.

As $V_{\text{in}}$ varies from 11 V to 14 V, the peak efficiency of the OCI-rccBuck converter drops from 96.2% to 95.5% (Fig. 4-50). As $V_o$ varies from 2.5 V to 3.5 V, the peak efficiency is 94.9%–96.2% (Fig. 4-51). The OCI-rccBuck converter has ~4.5% higher efficiency than the buck converter, and ~0.6% higher efficiency than the Discrete-L-rccBuck converter, under all variations.

Fig. 4-50.Measured efficiencies of the GaN-based buck in Fig. 4-48(b), and the rccBuck converters in Fig. 4-48(d) and Fig. 4-43(a) with $V_{\text{in}} = 11$–14 V, $V_o = 3.3$ V, and $f_s = 2$ MHz.
Fig. 4-51. Measured efficiencies of the GaN-based buck in Fig. 4-48(b), and the rccBuck converters in Fig. 4-48(d) and Fig. 4-43(a) with \( V_{in} = 12 \) V and \( V_o = 2.5–3.5 \) V.

Compared to the commercial power modules operating at the same power level, the OCI-rccBuck converter had the maximum efficiency at \( I_o = 7–20 \) A (Fig. 4-52). The efficiency advantage increases with \( I_o \). In the commercial modules, the Murata product has the maximum efficiency at the nominal load (\( I_o = 20 \) A). The OCI-rccBuck converter has 3.3% higher efficiency at 20 A and 43% lower volume than the Murata module. At light load (\( I_o = 0–5 \) A), the MPS module has the maximum efficiency, due to the phase-shading and DCM operations.
4.8.4 Conducted and Radiated EMI Measurements

Since the OCI-rccBuck converter achieves ZVS for all switches, the high-frequency ringing is lower than that of hard-switched converters. The reduced noise is verified by the conducted and radiated EMI measurements in this sub-section. Both light load ($I_o = 5\, A$) and nominal load ($I_o = 20\, A$) conditions are considered.

The measured switching waveforms in Fig. 4-53 shows ZVS is achieved for $M_{1a}$ at 5 A and 20 A. The $v_{ds1a}$ is a straight waveform because $C_r$ is very large. The dead time was adjusted in a wide range for realizing ZVS, i.e., 5 ns at $I_o = 5\, A$ and 20 ns at $I_o = 20\, A$. A programmable-dead-time controller is desired for a varied load. The maximum drain-to-source voltage is 18.2 V for $M_{1a}$ and 10.8 V for $M_{2a}$. The ringing of $v_{ds1a}$ is caused by the hard turn-off of $M_{1a}$. 

Fig. 4-52. Efficiency comparison for the rccBuck converter with OCI in Fig. 4-43(a) and commercial power modules in [13]–[16].
Fig. 4-53. Measured voltage waveforms for the OCI-rccBuck converter in Fig. 4-43(a) at (a) $I_o = 5$ A with zoom-in view in (b), and (c) $I_o = 20$ A with zoom-in view in (d).

Fig. 4-54 shows the measured conducted EMI spectra for the benchmark buck converter, Discrete-L-rccBuck converter, and OCI-rccBuck converter at 5 A and 20 A. They have the same $C_{in} = C_o = 47 \ \mu F$ and same GaN FETs. The measurement procedure follows Sub-section 3.7.2. The manually-fabricated discrete inductors for the rccBuck converter are not balanced well, inducing high amplitude at the fundamental frequency, 2 MHz. The OCI-rccBuck converter has symmetric PCB windings and symmetric gaps, reducing ~20 dB EMI at 2 MHz.
Fig. 4-54. Measured conducted EMI for benchmark buck converter [164], discrete-L-rccBuck converter in Fig. 4-48(d), and OCI-rccBuck converter in Fig. 4-43(a), with $V_{in} = 12$ V, $V_o = 3.3$ V, and $f_s = 2$ MHz at (a) $I_o = 5$ A and (b) $I_o = 20$ A.

The third harmonic (6 MHz) is reduced by ~15 dB for the rccBuck converter since the resonant current has a lower third harmonic than the squared current in the buck converter. The most significant advantage of the rccBuck converter, in the aspect of EMI, is the >15 dB lower spectrum.
at 100–500 MHz, thanks to the ZVS of all switches.

The radiated EMI was measured by the field probe of the Langer EMV-MS-02, as shown in Fig. 4-55. The distance between the field probe and the tested board is about 3 cm. A 50 μH LISN was applied at the input side to block the noise from the input source, consistent with the conducted EMI measurement setup. The field probe was adjusted manually and horizontally to find the point with the maximum field strength. The spectrum at that point was then recorded.

![Field probe](OCI-rccBuck)

![Field probe](Buck converter)

Fig. 4-55. Radiated EMI measurement setups for (a) OCI-rccBuck converter in Fig. 4-43(a), and (b) two-phase buck converter in Fig. 4-48(b).

Fig. 4-56 shows the measured radiated spectra of the OCI-rccBuck converter and two-phase buck converter at 5 A and 20 A. They have high EMI spectra at the fundamental frequency (2 MHz) since the ripple cancelling effect may not be significant in the radiation path. The buck converter has a significant noise at 150 MHz and 400 MHz as a result of the hard switching. At those frequencies, the rccBuck converter with ZVS operation has 18–25 dB lower amplitude.
Fig. 4-56. Measured radiated EMI for buck converter and OCI-rccBuck converter with $V_{in} = 12$ V, $V_o = 3.3$ V, $f_s = 2$ MHz, (a) $I_o = 5$ A, and (b) $I_o = 20$ A. The setup is shown in Fig. 4-55.
4.9 Conclusion

The Omni-coupled inductors in the rccBuck converter are leakage-based inductor with in-phase and interleaved windings. The Omni coupling includes three basic coupling mechanisms: intro-coupling, inter-coupling, and cross-coupling. The intro- and inter- couplings are usually designed in the range of \(-0.1\sim0.3\). The cross coupling is usually designed in the range of \(-0.9\sim0.96\). A tiny leakage inductance between the cross-coupled inductors is required to avoid the instability. The twisted E-E core with the benefits of negative couplings, short winding paths, small size, low dc bias, and small ac resistance, is adopted to implement the OCI. The inductance is modeled by using a gap/window-based reluctance network. The ac coupling coefficient is higher than the dc coupling coefficient because of the eddy effect. The core loss is modeled by using the EEL method. The inductance and core loss models greatly reduced the calculation time compared to the FES from 13 minutes to 4 seconds. The winding loss is modeled numerically by using simulation and curve fitting.

The designed Omni-coupled inductors were applied in a 12 V to 3.3 V rccBuck converter and demonstrated experimentally to have a 3.3% higher efficiency at 20 A output and 43% smaller size than the state-of-the-art product. Compared to the rccBuck converter with discrete inductors, the OCI-rccBuck converter achieves 0.5% higher efficiency and 57% smaller magnetic volume. The conducted EMI is also improved at the fundamental frequency with 12 dB reduction, at the third harmonic with 15 dB reduction, and at the high-frequency range with 15 dB reduction.
Chapter 5  Small-Signal Modeling and Feedback Control

Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>$D$, $d$, and $\dot{d}$</td>
<td>DC, instantaneous, and small-signal duty ratio</td>
</tr>
<tr>
<td>$f_o$</td>
<td>Resonant frequency of $L_o$ and $C_o$</td>
</tr>
<tr>
<td>$f_{p1}, f_{p2}, f_{p3},$ and $f_{p4}$</td>
<td>Compensated poles</td>
</tr>
<tr>
<td>$f_r$</td>
<td>Resonant frequency of $L_r$ and $C_r$</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>$f_{z1}, f_{z2},$ and $f_{z3}$</td>
<td>Compensated zeros</td>
</tr>
<tr>
<td>$G_{VoVin}$</td>
<td>Line to output transfer function</td>
</tr>
<tr>
<td>$G_{vo}$</td>
<td>Control to output transfer function</td>
</tr>
<tr>
<td>$Z_o$</td>
<td>Output impedance</td>
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In this chapter, an average-behavioral model was developed for the rccBuck converter. The corresponding small-signal model can predict two double poles and one right-half-plane zero in the open-loop control-to-output transfer function. According to this small-signal model, a modified type-III compensator was designed for a voltage model control. The closed loop has a $56^\circ$ phase margin and $20$ dB gain margin. The PWM generator is designed to have a programmable dead time and a protected duty ratio. The load-transient performance of the rccBuck converter is compared to that of a buck converter with the same switching frequency, output capacitance, and closed-loop bandwidth. The related simulation files are given in Appendix F.

5.1 Introduction

Previous chapters have demonstrated the efficiency, size, and EMI advantages of the rccBuck converter. The transient response is another important merit for a POL regulator. In order to design
a fast and stable feedback loop, an accurate small-signal model of the power stage is needed. As discussed in Section 1.5, the $L_r-C_r$ tank in the rccBuck converter is a filter-type component instead of an energy-transfer component. Therefore, the average model then is available for this converter. The Section 1.5 introduces three classical average models: the average-behavioral model, the three-terminal switch model, and the state-space model. The three-terminal switch model is invalid for the rccBuck converter since the assumptions of an a-p terminal parallel with a “voltage source” and c terminal connecting a “current source” are not satisfied. The waveforms in Fig. 5-1(b) yields the $v_{ap}$ is a three-level voltage, and the current through $C_{rb}$ is discontinuous. As a result, the $M_{1a}$ and $M_{2a}$ cannot be represented by a three-terminal switch. The average-behavioral model is more general than the three-terminal switch model. The average concept is applied for each single switch instead of a half bridge. The state-space model is available for any PWM converter, including the rccBuck converter. This model is based on the matrix calculation and suitable for numerical processing, but has a lack of physical insights of the converters. Finally, the average-behavioral model is selected for the rccBuck converter.

Fig. 5-1. (a) Schematic of rccBuck converter and (b) typical waveforms of $v_{ap}$, $i_{Loa}$, and $i_{Loa}+i_{Crb}$.

The PWM generator of the rccBuck converter has more limitations than the buck converter. For example, the maximum duty ratio is 1 for the buck converter but 0.5 for the rccBuck converter.
The active switches in the rccBuck converter are not allowed to turn on at the same time. The conventional buck control chip cannot be used for the rccBuck converter.

![Image](image_url)

**Fig. 5-2.** The ZVS-transition time (a) at $I_o = 5 \text{ A}$ is longer than that at (b) $I_o = 20 \text{ A}$ for the rccBuck converter in Fig. 4-48(d) at $V_{in} = 12 \text{ V}$, $V_o = 3.3 \text{ V}$, and $f_s = 2 \text{ MHz}$.

The rccBuck converter achieves an entire load ZVS but requires a variable dead time for the ZVS transition. At the light load, the $V_{ds1a}$ drops quickly before the $M_{1a}$ is turned on, as shown in Fig. 5-2(a). At the heavy load, tiny current discharges $C_{oss}$, and the $V_{ds1a}$ drops slowly, as shown in Fig. 5-2(b). A PWM generator with a programmable dead time is built to control the dead time by the external dc voltages. The dead times of the active switch and the synchronous switch are controlled separately. The dead time variation range is $0 - 20 \text{ ns}$.

The organization of this chapter is as follows: The large-signal average-behavioral model is derived in Section 5.2. The corresponding small-signal model is introduced in Section 5.3. The analytical transfer functions of the control-to-output, line-to-output, and output impedance are derived and verified by Simplis simulations. Section 5.4 compares the compensator designs for an rccBuck converter and a buck converter. The other functional blocks in the feedback loop are implemented in Section 5.6. The transient response of the closed rccBuck converter is discussed in Section 5.7.
5.2 Large-Signal Average-Behavioral Model

The average-behavioral model is helpful in understanding the dc voltage gain and the operation principles of the converter. The objective of this model is to represent the switched circuit by a continuous circuit. The first step is to average the active-switch voltage and the synchronous-switch current in Fig. 5-3(b). When $M_{1a}$ is turned on, the $v_{swa}$ equals $v_{Cra}$, and the $i_{dM_{1a}}$ equals $i_{Loa} - i_{Lrb}$. The average values for $v_{swa}$ and $i_{dM_{1a}}$ are $Dv_{Cra}$ and $D(i_{Loa} - i_{Lrb})$, respectively.

![Diagram](image)

**Fig. 5-3.** (a) Schematic of rccBuck converter and (b) typical waveforms of $v_{swa}$ and $i_{dM_{1a}}$.

All switches are replaced by the dependent voltage or current sources as shown in Fig. 5-4(a). The interaction between the two phases exists in the $i_{1a}$, which makes it difficult to analyze this complex circuit. Notice that the averaged voltages at $ina$ and $inb$ are the same since the two phases are symmetric. The averaged voltages at the switching nodes $swa$ and $swb$ are also the same. The two-phase circuit in Fig. 5-4(a) then could be simplified to a single-phase circuit in Fig. 5-4(b). Some important features of the rccBuck converter could be explained by this equivalent circuit. For example, the $C_r$ stores the energy from the input source and then transfers the energy to the switching node. The voltage gain, $V_o/V_{in} = D/(2+D)$, is then obtained by using the volt-second balance. The topology of the simplified circuit is very similar to a Cuk converter, but they have significant different characteristics. The extended duty ratio and positive $V_o$ are available for the
rccBuck converter but not seen in the Cuk converter.

Fig. 5-4. (a) Large-signal average-behavioral model of rccBuck converter simplified to (b) one-phase equivalent circuit.

The average-behavioral model is verified by a transient simulation with the setup shown in Fig. 5-5(a). The load current changes between 5 A and 15 A. The average value of the $V_o$ could be predicted by the average-behavioral model. The $v_{o\text{, real}}$ waveform is thicker than the $v_{o\text{, avg}}$ waveform because the switching ripples are ignored in the average model. The transient-response comparison implies the average model is effective for a low-bandwidth design.

Fig. 5-5. (a) Large-signal model compared with real rccBuck converter with $V_{in} = 12$ V, $V_o = 3.3$ V, $f_s = 2$ MHz, $L_r = 160$ nH, $L_o = 95$ nH, $C_r = 264$ nF, and $C_o = 100$ μF; (b) simulated load step-up and step-down responses.

The effect of the MOSFET on-resistances are represented by the $R_e$ in Fig. 5-4(a), similar to
the \( R_e \) in the three-terminal switch model. The \( R_e \) is obtained by considering the conduction loss during the calculation of the averaged switching node voltage.

![Diagram](image)

*Fig. 5-6. Switched states of rccBuck converter for calculating (a) \( V_{swb\_off} \), (b) \( V_{swb\_on1} \), and (c) \( V_{swb\_on2} \).*

When \( M_{2b} \) is turned off (Fig. 5-6(a)), the \( V_{swb\_off} \) is calculated as

\[
V_{swb\_off} = V_{Crb} - R_{ds}h (i_{Lb} - i_{Lra}) + R_{ds}l (i_o - i_{in})
\]  

(5-1)

When \( M_{2b} \) and \( M_{1a} \) are on (Fig. 5-6(b)), the \( V_{swb\_on1} \) is calculated as

\[
V_{swb\_on1} = -R_{ds}l (i_o - i_{in})
\]  

(5-2)

When \( M_{2b} \) is on and \( M_{1a/b} \) is off (Fig. 5-6(c)), the \( V_{swb\_on2} \) is calculated as

\[
V_{swb\_on2} = -R_{ds}l (i_{Lob} - i_{Lra})
\]  

(5-3)

The \( V_{swb} \) for the real rccBuck converter is averaged as

\[
V_{swb} = \frac{(V_{swb\_on1} + V_{swb\_off})D}{2} + V_{swb\_on2} D' = \frac{DV_{Crb}}{2} - (i_{Lob} - i_{Lra}) \left( \frac{D}{2} R_{ds}h + D' R_{ds}l \right)
\]  

(5-4)

On the other hand, \( V_{swb} \) in the average-behavioral model in Fig. 5-4(a) is

\[
V_{swb} = \frac{DV_{Crb}}{2} - (i_{Lob} - i_{Lra}) R_{eb}
\]  

(5-5)

Comparing (5-4) and (5-5), the \( R_e \) for a single-phase rccBuck converter is obtained by

\[
R_e = \frac{R_{eb}}{2} = \frac{R_{ea}}{2} = \frac{D}{4} R_{ds}h + \frac{D'}{2} R_{ds}l
\]  

(5-6)

### 5.3 Small-Signal Average-Behavior Model

The large-signal model without any parasitic resistances is shown in Fig. 5-7(a). The perturbation of \( \hat{d} \) is added in the behavioral model to obtain the small-signal model in Fig. 5-7(b).
Fig. 5-7. (a) Single-phase large-signal model of rccBuck converter without parasitic resistances. (b) Perturbation \( \hat{d} \) is applied on D to derive \( G_{vd} \).

The relationship between the \( \hat{v}_o \) and \( \hat{d} \) in Fig. 5-7(b) is calculated by

\[
\hat{v}_o = \frac{2V_{in}}{(2 + D)L_0C_o} s^4 + \frac{1}{R_L C_o} s^3 + \left[ \frac{(D + 2)^2}{4L_r L_r} \right] s^2 + \left[ \frac{D^2}{4R_L L_o L_r C_r} \right] s + \left( \frac{D}{2C_r L_r L_o C_o} \right) \tag{5-7}
\]

The denominator of (5-7) is a fourth-order polynomial. If the small terms are ignored, the \( G_{vd} \) with a quartic denominator could be simplified to

\[
G_{vd} = \frac{\hat{v}_o}{\hat{d}} = \frac{2V_{in}}{(2 + D)L_0 C_o} \left( s^2 + \frac{1}{R_L C_o} s + \frac{2}{L_o C_o} \right) \tag{5-8}
\]

Notice the \( L_r / C_r \) and \( L_o / C_o \) are decoupled in (5-8). The \( L_o \) and \( C_o \) result in a double pole. The \( L_r \) and \( C_r \) result in another double pole and a double right-half-plane (RHP) zero. The ignored terms represent the coupling effect between the resonant (\( L_r \) and \( C_r \)) and filter (\( L_o \) and \( C_o \)) tanks.

The modeled \( G_{vd} \) without parasitic resistances agrees with the Simplis-simulated \( G_{vd} \), as shown in Fig. 5-8. The double pole of the \( L_o / C_o \) is at 75 kHz, lower than that of \( L_r / C_r \), 1 MHz. The RHP zero of the \( L_o / C_o \) is at 850 kHz, close to the double pole. The zeros and poles higher than the half switching frequency cannot be predicted by the average model. They may be caused by the resonance between \( L_r \) and \( C_o \), or \( L_o \) and \( C_r \).
Fig. 5-8. Simulated and modeled $G_{vd}$ for the rccBuck converter with power-stage parameters and operating conditions in Fig. 5-5. Parasitic resistances are not considered.

If the resonant frequency of $L_r$ and $C_r$ is higher than the half switching frequency, the average model cannot predict the double pole of $L_d/C_r$ correctly, as shown in Fig. 5-9. The effect of the switching ripple should be included in the model to calculate those high-frequency ($> f_s/2$) poles.

Fig. 5-9. Simulated and modeled $G_{vd}$ for rccBuck converter with $C_r = 200 \text{ nF}$. Other power-stage parameters and operating conditions are given in Fig. 5-5. Parasitic resistances are not considered.

If the resonant frequency of $L_r$ and $C_r$ is too close to that of $L_o$ and $C_o$, the simplified average model (5-8) is inaccurate since the coupling effect between $L_d/C_r$ and $L_o/C_o$ has been ignored. The double pole predicted by the average model has lower frequency and lower damping than the simulated one, as shown in Fig. 5-10. The complete equation (5-7) is able to predict the interaction between $L_d/C_r$ and $L_o/C_o$. As a result, the $G_{vd}$ calculated by (5-7) agrees with the simulated one.
In summary, the effective range of the complete model in (5-7) is \( f_r = \frac{1}{(2\pi\sqrt{L_rC_r})} \leq f_s / 2 \).

The simplified model in (5-8) is effective for \( f_o = \frac{1}{(2\pi\sqrt{L_oC_o})} \leq f_r \leq f_s / 2 \).

Fig. 5-10. Simulated and modeled G\(_{vd}\) for rccBuck converter with \( C_r = 50 \text{ nF} \). Other power-stage parameters and operating conditions are given in Fig. 5-5. Parasitic resistances are not considered.

The average-behavioral circuit including the parasitic resistances is shown in Fig. 5-11. The ESR of \( C_{io} \) and dc resistance of \( L_{io} \) are considered. The \( f_r \) is usually designed higher than the \( f_o \). The assumption of the decoupled \( L_r-C_r \) loop and \( L_o-C_o \) loop is still true.

![Diagram](image)

The damping effect is taken into account for each loop. The \( G_{vd} \) is then modified to

\[
G_{vd} = \frac{\bar{v}_d}{d} = \frac{2V_{in}}{(2+D)L_oC_o} \left( \frac{s^2 - \frac{D I_o}{4V_{in}L_r} s + \frac{2 + D}{2C_r L_r}}{s^2 + \frac{\omega_0}{Q_o} s + \omega_0^2} \right) \left( \frac{s^2 + \frac{\omega_r}{Q_r} s + \frac{(D+2) \omega_r^2}{4}}{s^2 + \frac{\omega_r}{Q_r} s + \frac{(D+2)^2 \omega_r^2}{4}} \right)
\]

(5-9)

\[
\omega_o = \sqrt{\frac{2}{L_o C_o}} \omega_r = \frac{1}{\sqrt{L_r C_r}} Q_o = \frac{1}{\omega_o \frac{L_o}{L_L + (R_{L+2R_e+2R_{Co})C_o}}} Q_r = \frac{1}{\omega_r \left( \frac{R_{L+2R_e+4R_{Co}}}{(D+2)^2} \right) C_r}
\]

Comparing (5-8) and (5-9), the ESRs of \( C_r \) and \( C_o \) give rise to two zeros. The winding

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resistances and $R_e$ affect the dampings of the double poles. The modeled $G_{vd}$ with parasitic resistances agrees with the simulated one, as shown in Fig. 5-12.

![Simulated and modeled $G_{voVin}$ for the rccBuck converter with power-stage parameters and operating conditions in Fig. 5-5. Parasitic resistances of $R_{Lr} = R_{Lo} = 1 \, \text{m} \Omega$, $R_{Cr} = 0.28 \, \text{m} \Omega$, $R_{Co} = 0.14 \, \text{m} \Omega$, $R_{dsh} = 8 \, \text{m} \Omega$, and $R_{dsl} = 1.5 \, \text{m} \Omega$ in Fig. 5-11 are considered.

According to the average-behavioral model in Fig. 5-11, the line to output transfer function is obtained by

$$G_{VoVin} = \frac{\hat{V}_o}{V_{in}} = \frac{D(2 + D)}{2L_C C_o L_r C_r} \left( \frac{1 + R_C C_o s}{s^2 + \frac{\omega_C}{Q_o} s + \omega_C^2} \right) \left( \frac{1 + R_C C_r s}{s^2 + \frac{\omega_C}{Q_r} s + \frac{(D + 2)^2}{4} \omega_r^2} \right) \tag{5-10}$$

The $G_{VoVin}$ has no RHP zero because the input source is always connected to the $V_o$. In the analysis of $G_{vd}$, the $\hat{V}_o$ is independent of $\hat{d}$ when $L_r$ and $C_r$ are resonant, leading to the RHP zero.

The modeled $G_{VoVin}$ is verified by the Simplis simulation (Fig. 5-13). The effective frequency of this model is up to 1 MHz.

![Simulated and modeled $G_{voVin}$ for the rccBuck converter with power-stage parameters and operating conditions in Fig. 5-5. Parasitic resistances are given in Fig. 5-12.](image-url)
The output impedance is derived by Fig. 5-11

\[
Z_o = R_{Co} \frac{s^2 + \left( \frac{1}{R_{Co}C_o} \right) s + \frac{R_{Lo} + R_{elr}}{L_o C_o}}{s^2 + \frac{\omega_o^2}{Q_o} s + \omega_o^2} + R_{Lo} + R_{elr}
\]

(5-11)

\[
R_{elr} = \frac{(2 + D)^2}{D^2} \left( \frac{2R_e}{D^2R_{lr}} \right)
\]

The \( L_r \) and \( C_r \) are not important for the \( Z_o \). At a low frequency, the impedance of \( L_r \) is approximated by \( R_{Lr} \), and the \( C_r \) is considered open because of \( C_r \ll C_o \). At a high frequency, the \( Z_o \) is determined by the ESR of \( C_o \). Finally, the \( Z_o \) in (5-11) is independent of \( L_r \) and \( C_r \). The modeled \( Z_o \) agrees with the simulated one as shown in Fig. 5-14.

![Graphs showing simulated and modeled Z_o for the rccBuck converter with power-stage parameters and operating conditions in Fig. 5-5. Parasitic resistances are given in Fig. 5-12.](image)

The mismatched components of the two phases may cause an unbalanced current as discussed in Section 2.4, but it has a negligible impact on the small-signal model. The simulated control-to-output transfer functions, with balanced and unbalanced phases, are compared in Fig. 5-15. The unbalanced case has an additional pair of double pole and double zero at \( \sim 570 \) kHz. They induce a negligible gain increase and phase change. In order to simplify the calculation in the later analysis, the two phases are assumed symmetric and balanced.
Simulated $G_{vd}$ for balanced and unbalanced rccBuck converters; the nominal conditions are given in Fig. 5-5 and Fig. 5-12. The unbalanced case is retrofitted from the balanced case. Phase $b$ is the same, and phase $a$ has $L_{ra} = 0.9 \ L_{rb}$, $L_{oa} = 0.9 \ L_{ob}$, and $C_{ra} = 0.9 \ C_{rb}$.

5.4 Compensator Design under Voltage Mode Control

A challenge of the rccBuck converter design is the presence of the RHP zero, which does not exist in a normal buck converter. The basic control diagram is shown in Fig. 5-16. The complete closed loop consists of the power stage, the compensator, and the PWM generator. The intent of this section is to design a compensator for the rccBuck converter under voltage mode control. The conventional type-III compensator is modified to offer a higher phase margin. A buck converter switched at the same frequency, with the same bandwidth, is also designed. The buck converter could achieve the required phase margin, $> 45^\circ$, by using a conventional type-III compensator.

Fig. 5-16. Schematic of the closed-loop rccBuck converter with voltage mode control.
The open-loop $G_{vd}$ of the rccBuck converter and the two-phase interleaved buck converter are compared in Fig. 5-17. The $L_o-C_o$ double pole of the rccBuck converter is higher than that of the buck converter. The buck $G_{vd}$ is clean at high frequency because it has no $L_r$ and $C_r$. The dc gain of the rccBuck $G_{vd}$ is lower than that of the buck $G_{vd}$. From an efficiency point of view, a lower dc gain represents an extended duty ratio, which is beneficial for the switching loss of the active switch and the conduction loss of the synchronous switch. However, from a control point of view, it is more difficult to design a compensator for a $G_{vd}$ with a small dc gain.

![Plot](image-url)

**Fig. 5-17.** Simulated open-loop $G_{vd}$ of rccBuck converter with power-stage parameters in Fig. 5-5 and a two-phase buck converter with $L_o = 230$ nH, $C_o = 100$ μF and $f_s = 2$ MHz. They have the same parasitic resistances in Fig. 5-12 and same operating conditions in Fig. 5-5.

Conventional type-III compensators are used in the feedback loops of the rccBuck converter and buck converter in Fig. 5-17. The compensated poles and zeros are listed in Table 5-1. The design procedure follows [165].

The simulated loop gains are shown in Fig. 5-18. The 1 MHz double pole of the rccBuck $T_{loop}$ is damped significantly compared with Fig. 5-17 because the $C_{oss}$ is simulated in the feedback loop. Two converters are designed with the same bandwidth, 100 kHz. The closed buck converter has a higher gain at 20–100 kHz. The compensated zeros of the buck converter are 15 kHz and 30 kHz, away from the output-filter double pole. Those zeros improve the phase at 100 kHz and increase
the phase margin. The compensated zeros of the rccBuck converter cannot be placed away from the 75 kHz double pole; otherwise, the gain at 30–40 kHz would decrease below 0 dB and would induce a very low bandwidth. The dc gain could increase to improve the bandwidth and ensure the gain at 30–40 kHz higher than 0 dB, but the phase margin is very small.

Table 5-1. Compensator designs for the buck converter and rccBuck converter in Fig. 5-17, as well as the buck converter with an input filter in Fig. 5-23(b). The compensator schematic is shown in Fig. 5-19.

<table>
<thead>
<tr>
<th></th>
<th>Buck</th>
<th>RccBuck design 1</th>
<th>RccBuck design 2</th>
<th>Buck with input filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>100 kHz</td>
<td>100 kHz</td>
<td>100 kHz</td>
<td>40 kHz</td>
</tr>
<tr>
<td>PM</td>
<td>50°</td>
<td>33°</td>
<td>56°</td>
<td>42°</td>
</tr>
<tr>
<td>(f_z1)</td>
<td>15 kHz</td>
<td>80 kHz</td>
<td>80 kHz</td>
<td>5 kHz</td>
</tr>
<tr>
<td>(f_z2)</td>
<td>30 kHz</td>
<td>90 kHz</td>
<td>90 kHz</td>
<td>10 kHz</td>
</tr>
<tr>
<td>(f_p1)</td>
<td>300 kHz</td>
<td>700 kHz</td>
<td>700 kHz</td>
<td>100 kHz</td>
</tr>
<tr>
<td>(f_p2)</td>
<td>800 kHz</td>
<td>1.3 MHz</td>
<td>1.3 MHz</td>
<td>200 kHz</td>
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<tr>
<td>(f_z3)</td>
<td></td>
<td></td>
<td>55 kHz</td>
<td></td>
</tr>
<tr>
<td>(f_p3)</td>
<td></td>
<td></td>
<td>130 kHz</td>
<td></td>
</tr>
<tr>
<td>(f_z4)</td>
<td></td>
<td></td>
<td>100 kHz</td>
<td></td>
</tr>
<tr>
<td>(f_p4)</td>
<td></td>
<td></td>
<td>200 kHz</td>
<td></td>
</tr>
<tr>
<td>(R_1)</td>
<td>1.2 kΩ</td>
<td>1.2 kΩ</td>
<td>1.2 kΩ</td>
<td>1.2 kΩ</td>
</tr>
<tr>
<td>(C_1)</td>
<td>7 nF</td>
<td>2.2 nF</td>
<td>1.7 nF</td>
<td>22 nF</td>
</tr>
<tr>
<td>(R_2)</td>
<td>1.5 kΩ</td>
<td>1.2 kΩ</td>
<td>1.1 kΩ</td>
<td>729 Ω</td>
</tr>
<tr>
<td>(C_2)</td>
<td>4.3 nF</td>
<td>1.7 nF</td>
<td>1.3 nF</td>
<td>25 nF</td>
</tr>
<tr>
<td>(R_3)</td>
<td>47 Ω</td>
<td>133 Ω</td>
<td>177 Ω</td>
<td>63 Ω</td>
</tr>
<tr>
<td>(C_3)</td>
<td>370 pF</td>
<td>75 pF</td>
<td>120 pF</td>
<td>1.14 nF</td>
</tr>
<tr>
<td>(R_{o1})</td>
<td>10 kΩ</td>
<td>10 kΩ</td>
<td>10 kΩ</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>(R_{o2})</td>
<td>10 kΩ</td>
<td>10 kΩ</td>
<td>6.8 kΩ</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>(C_{o1})</td>
<td></td>
<td>300 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_4)</td>
<td></td>
<td>10 Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_4)</td>
<td></td>
<td>400 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_5)</td>
<td></td>
<td>2 kΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

One compensated pole is placed slightly lower than the RHP zero to damp the \(L_r-C_r\) peak. The other compensated pole is placed near the half \(f_s\) to reduce the high-frequency noise. The phase
margin of the designed rccBuck converter is 33°, lower than the required phase margin, 45°. The phase margin for the buck converter is 50°, meeting the requirement. If the C₀-ESR zero is close to the bandwidth, the loop gain achieves a higher phase margin [166]–[168]. In this case, low ESR ceramic capacitors are employed for reducing the capacitor loss, which makes the design difficult.

![Fig. 5-18. Simulated loop gains for the rccBuck converter and buck converter with the open-loop designs in Fig. 5-17 and compensator designs in Table 5-1.](image)

In order to improve the phase margin, the type-III compensator in Fig. 5-19(a) is modified to Fig. 5-19(b) with a front phase-lead compensation.

![Fig. 5-19. Type-III compensator (a) without and (b) with the front phase-lead compensation.](image)

The transfer function for the conventional type-III compensator is

\[
G_{voc,1} = \frac{R_{o2}}{R_{o1} + R_{o2}} \frac{\omega_1 (1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s (1 + s/\omega_{p1})(1 + s/\omega_{p2})}
\]  

(5-12)
\[ \omega_I = \frac{1}{R_1(C_1 + C_3)}, \omega_{z1} = \frac{1}{R_2C_1}, \omega_{z2} = \frac{1}{C_2(R_1 + R_3)}, \omega_{p1} = \frac{1}{R_3C_2}, \omega_{p2} = \frac{1}{\frac{R_2C_1C_3}{C_1 + C_3}} \]

The \( G_{voc} \) for the modified type-III compensator is

\[
G_{voc_{-2}} = G_{voc_{-1}} \frac{(1 + s/\omega_{z3})(1 + s/\omega_{z4})}{(1 + s/\omega_{p3})(1 + s/\omega_{p4})}
\]

\[
\omega_{z3} = \frac{1}{C_1R_1}, \omega_{p3} = \frac{1}{C_1R_1/R_2}, \omega_{z4} \approx \frac{1}{2C_4R_5}, \omega_{p4} \approx \frac{1}{C_4R_5}, R_5 > 100R_4
\]

(5-13)

The \( \sqrt{f_{z3}f_{p3}} \) is designed slightly lower than the cross-over frequency \( f_{co} \), and the \( \sqrt{f_{z4}f_{p4}} \) is slightly higher than the \( f_{co} \). The phase improvement of the phase-lead compensation is verified by Simplis simulation. The \( v_o \)-to-\( v_1 \) and \( v_o \)-to-\( v_2 \) transfer functions are shown in Fig. 5-20. The first stage \( G_{vo-vol} \) could offer a 25° phase improvement, and the second stage \( G_{vol-vol} \) could offer an 18° phase improvement. The total phase improvement is 43° at 100 kHz.

![Fig. 5-20. Simulated \( G_{vo-vol} \) and \( G_{vol-vol} \) for the front lead-phase compensation in Fig. 5-19(b). Bandwidth of the operational amplifiers is 100 MHz.](image)

The modeled \( G_{voc_{-2}} \) agrees with the simulated \( G_{voc_{-2}} \) in Fig. 5-21. The discrepancy at 10 MHz is caused by the nonlinearity of the operational amplifiers. This compensator offers 42° phase increase at the closed-loop cross-over frequency, 100 kHz. The bandwidth cannot be designed at 200 kHz with the peak phase of \( G_{voc_{-2}} \) because the small gain of \( G_{voc_{-2}} \) at 50 kHz would cause a severe dip at 50 kHz and a low cross-over frequency for the closed loop gain.

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Fig. 5-21. Simulated and modeled $G_{\text{voc}_2}$ for the modified type-III compensator in Fig. 5-19(b). Bandwidth of
the operational amplifiers is 100 MHz.

The configurations of zeros and poles of the modified compensator in Fig. 5-19(b) have been discussed earlier. The compensator components are then designed by the procedure as follows:

- Specifications: $V_{\text{in}}$, $V_o$, $D$, $f_s$, $I_o$, $L_r$, $L_o$, $C_r$, $C_o$, and bandwidth $f_{co}$
- Power-stage double pole and RHP zero: $f_0 = \frac{1}{2\pi \sqrt{L_o C_o/2}}$ and $f_{RHP} = \frac{1}{2\pi \sqrt{\frac{2}{L_r C_r} + \frac{1}{L_r C_r}}}$
- Compensated zeros and poles: $f_{z1,2} \approx 0.8 f_{co}$, $f_{z3,4} \approx 0.2 f_{co}$, $f_{p1} \approx f_{RHP}$, $f_{p1} \approx f_s/2$, and $f_{p3,4} \approx 5 f_{co}$
- Gain of $G_{vd}$ at $f_{co}$, $|G_{vd,fco}|$, calculated by (5-9)
- Modulator gain, $|FM|$, assumed independent of frequency
- Gain of $G_{\text{voc}_2}$ at $\omega_l = 1$ and $f = f_{co}$, $|G_{\text{voc}_2, w=1}|$, calculated by (5-12) and (5-13)
- $\omega_l$ in (5-12) calculated by $\omega_l = \frac{1}{|G_{vd,fco}||FM||G_{\text{voc}_2, w=1}|}$
- Resistances and capacitances calculated by (5-12) and (5-13)

The compensated zeros, poles, and corresponding components are listed in Table 5-1. The loop gain of the modified closed-loop-rccBuck design is compared with that of the old designs in Fig. 5-22. The phase margin of the rccBuck converter increases to 56°. The $T_{\text{loop1}}$ and $T_{\text{loop2}}$ have the same dc gain and similar high-frequency gain.

The disadvantage of the modified type-III compensator is it has more components, which
increases the cost and complicity. The method to improve the phase margin without adding components will be explored in the future.

Fig. 5-22. Simulated loop gains for rccBuck and buck converters in Fig. 5-17 with compnsators in Table 5-1.

5.5 Comparison of Buck and RccBuck Feedback Designs

The input filter was designed for the buck converter to achieve the same conducted EMI as the rccBuck converter with a 100 nF input/decoupling capacitor (Fig. 5-23). The design procedure of the input filter followed [165]. The resonant frequency of the $L_{in}$ and $C_{in}$ is 160 kHz, and the characteristic impedance is $0.3V_o/(I_oD^2) = 1\,\Omega$. The $L_{in}$ is 1 $\mu$H, and $C_{in}$ is 1 $\mu$F. The switching-loop parasitic inductances in Fig. 1-7(c) and Fig. 3-24, and capacitor ESL from Table 3-1 were considered. A LISN was applied to simulate the conducted DM noise. The CM noise was not considered for simplicity.

Fig. 5-23. Schematics of (a) rccBuck converter without input filter and (b) buck converter with input filter, having the same $f_s = 2$ MHz and same conducted noise.
The simulated EMI for two converters are similar as shown in Fig. 5-24. The noise at 200 – 500 MHz is difficult to reduce for hard-switched buck converter due to the ESL of $C_{in}$. In practice, the contact inductance may be dominant if the ESL of $C_{in}$ is lower than 0.1 nH. The rccBuck converter operates with ZVS and has low switching noise, thus does not need the input filter.

![Simulated conducted EMI spectra](image)

**Fig. 5-24. Simulated conducted EMI spectra of (a) the rccBuck converter without input filter and (b) buck converter with input filter in Fig. 5-23.**

The simulated control-to-output transfer functions for the converters in Fig. 5-23 and a buck converter without input filter are compared in Fig. 5-29. The input filter of the buck converter induces a peak at 200 kHz that limits the resonant frequency of $L_o$ and $C_o$. The $C_o$ is 100 μF for the buck converter without input filter and 400 μF for the buck converter with an input filter. Higher $C_o$ is required to separate the input filter’s and output filter’s resonant frequencies, otherwise the bandwidth is very low in the feedback design. The effect of $L_{in}$ and $C_{in}$ in a buck converter is similar to the effect of $L_r$ and $C_r$ in an rccBuck converter. The $L_r$ and $C_r$ have the functionalities of input filter and ZVS, while $L_{in}$ and $C_{in}$ have only one functionality, the input filter. High resonant frequency of $L_r$ and $C_r$ also allows high-bandwidth design of the rccBuck converter.
Fig. 5-25. Simulated open-loop \( G_{vd} \) of rccBuck converter in Fig. 5-23, two-phase buck converter without input filter and with power-stage parameters in Fig. 5-17, and buck converter with an input filter in Fig. 5-23.

Fig. 5-26 shows the simulated loop gains, corresponding to the open-loop \( G_{vd} \) in Fig. 2-32 and compensators in Table 5-1. In the compensator design of the buck converter with an input filter, two compensated zeros are much lower than the resonant frequency of \( L_o \) and \( C_o \), 20 kHz. The compensated poles are near the RHP zero of \( L_r \) and \( C_r \) to reduce the 200 kHz peak. The bandwidth of the buck converter with input filter is 40 kHz, lower than that of buck converter without input filters, and the rccBuck converter. The input filter also reduces the phase margin from 50° to 42°.

Fig. 5-26. Simulated loop gains for the converters with open-loop \( G_{vd} \) in Fig. 5-25 and compensators in Table 5-1.

### 5.6 PWM Generator with Protected D and Programmable Dead Times

The input of the PWM generator is the \( v_c \) signal from the compensator, and the outputs are
the driving signals for the power stage, as shown in Fig. 5-16. The PWM generator contains a comparator, a duty-ratio limiter, and a dead-time programmer.

The compensator output $v_c$ is compared with triangular references to generate the PWM waveforms. Fig. 5-27(a) shows the schematic. The corresponding simulated waveforms are shown in Fig. 5-27(b). The two-phase interleaved triangular waveforms could be generated by a J-K flip-flop phase splitter followed by an integrator [169]. In this work, the triangular waveforms are offered by the function generators, AFG3102. The amplitudes of two triangular signals are tuned to balance the two phases. For example, in the experiment, the maximum voltage is 3.1 V for $v_{\text{tria}}$ and 3.3 V for $v_{\text{trib}}$. The minimum and maximum voltages of $v_{\text{tria}}$ and $v_{\text{trib}}$ determine the minimum duty ratio $D_{\text{Min}}$, e.g., $D_{\text{Min}} = 0.2 / (0.2+3.1) = 0.06$ when the $v_{\text{tria}}$ swings from -0.2 V to 3.1 V.

![Diagram of two-phase PWM generator](image)

Fig. 5-27. (a) Schematic of a two-phase PWM generator and (b) corresponding waveforms.

The high-side driving signals $v_{g1a}$ and $v_{g1b}$ (Fig. 5-16) are not allowed to have overlaps. The duty ratio $D$ should be limited by $D/2 < 0.5$. This functionality is realized by a latch as shown in Fig. 5-28(a). The input signals $p_{a1}$ and $p_{b1}$ are from the outputs of the comparators in Fig. 5-27(a). When $p_{a1}$ and $p_{b1}$ have $D/2 < 0.5$, the duty ratios of $p_{a/b1}$ and $p_{a/b2}$ are the same. When $p_{a1}$ and $p_{b1}$ have $D/2 > 0.5$, the duty ratios of $p_{a2}$ and $p_{b2}$ are limited by the $D_{\text{Max}}$. The RC filter controls the
rising time of \( p_{a1n} \) and the \( D_{\text{Max}} \). The recommended design is \( 2\pi R_{\text{latch}} C_{\text{latch}} f_s \approx 0.2 \) and \( D_{\text{Max}} \approx 0.47 \). A 150 \( \Omega \) \( R_{\text{latch}} \) and a 100 pF \( C_{\text{latch}} \) were used in the experiment.

The functionality of the programmable dead time is realized by the circuit in Fig. 5-29(a). The rising edge of \( p_{a3/4} \) is controlled by the RC constant of \( R_{\text{dead}} \) and \( C_{\text{dead}} \). The dead time is obtained by comparing this rising edge with a threshold voltage as shown in Fig. 5-29(b). The falling edge is very fast since the \( R_{\text{dead}} \) is shorted by the diode. The dead times for the high-side and low-side switches then could be controlled independently. The design of \( R_{\text{dead}} \) and \( C_{\text{dead}} \) in this work is \( 2\pi R_{\text{dead}} C_{\text{dead}} f_s \approx 0.2 \) for \( T_{\text{dead,Max}} \approx 20 \text{ ns} \) at \( f_s = 2 \text{ MHz} \). A 150 \( \Omega \) \( R_{\text{dead}} \) and a 100 pF \( C_{\text{dead}} \) were used in the experiment.
The rccBuck converter with a complete feedback loop is shown in Fig. 5-30. The power stage is designed by the state-space model or normalized curves in Chapter 2. The compensator and PWM generator are introduced in Sections 5.4 and 5.6.

![Fig. 5-30. Implementation of the feedback control for an rccBuck converter.](image)

### 5.7 Load-Transient Response

The closed rccBuck and buck converters with the compensators in Table 5-1 were tested with a load transient. The load current is switched between 5 A and 15 A as shown in Fig. 5-31(a). The buck converter without an input filter has the minimum settling time since it has the highest gain at 20–100 kHz (Fig. 5-22). The rccBuck converter with the second design has the highest phase margin (56°) and the minimum overshoot voltage. The buck converter with an input filter has a similar voltage overshoot but doubled settling time compared to the rccBuck converter and buck converter without input filters.
Fig. 5-31. (a) Switched load current and simulated output responses for (b) the buck converter without input filters, (c) rccBuck converter (design 1), (d) rccBuck converter (design 2), and (e) buck converter with an input filter, corresponding to the converters with closed-loop gains in Fig. 5-26 and Fig. 5-22. The compensator parameters are given in Table 5-1.

The load-transient responses were verified experimentally by using the control board in Fig. 5-32 and the power stages in Fig. 4-48(a) and (d). The buck converter with an input filter was not tested. In the control board, the error amplifier was the AD823 with a 16 MHz bandwidth [170]. The comparators were LTC6752 with a 2.9 ns propagation delay and a 280 MHz toggle rate [171]. The AND gates were SN74LVC1G97DBVR with a ~4 ns propagation [172]. A 0.33 Ω resistor and a 0.7 Ω resistor were built to offer 10 A and 4.7 A load current, respectively.
Fig. 5-32. Prototypes of the control board (implementation of Fig. 5-30) and the load resistors for the load-transient test.

The measured load-transient responses for the buck converter and rccBuck converters with the compensators in Table 5-1 are shown in Fig. 5-33. The load resistor is $R_{\text{load}2}$ at light load ($I_o = 4.7$ A) and $R_{\text{load}1}/R_{\text{load}2}$ at heavy load ($I_o = 14.7$ A). The experimental load-current change is $13 - 4 = 9$ A, lower than the designed one, 10 A, because of the terminal loss. The buck converter has large output inductors ($L_o = 230$ nH) and a small steady-state $V_o$ ripple, $< 40$ mV. During the load transition, the first peak of $V_o$ is caused by the bandwidth of the feedback loop. Three cases are designed with the same bandwidth, 100 kHz. Therefore, the frequency of the first peak of $V_o$ in Fig. 5-33 is $\sim 100$ kHz. The rccBuck converter with a 33° phase margin (design 1) has more cycles of the 100-kHz ringing, especially at the fast load step down. That ringing is reduced significantly for design 2 with a higher phase margin, 56°.

An unexpected low-frequency ($\sim 20$ kHz) noise exists in the $V_o$ transient waveforms. This might be caused by the CM current in the long ground loop between the control board and the
power stage, as well as the noisy ground of the signal generators and auxiliary power supplies. Integrating the control circuit and the power stage into one board and avoiding auxiliary power supplies, should be helpful in reducing that noise.

![Fig. 5-33. Measured transient responses of (a) the buck converter, (b) rccBuck converter (design 1), and (c) rccBuck converter (design 2) with the power-stage parameters in Fig. 5-17, compensator parameters in Table 5-1, and the control board in Fig. 5-32, at \( V_m = 12 \) V, \( V_o = 3.3 \) V, and \( f_s = 2 \) MHz.]

Table 5-2 compares the settling times and overshoot/undershoot voltages for the designed
converters and the commercial products with the same $V_{in}$ and $V_o$. The designed converters operate at a higher frequency (2 MHz) with a smaller $C_o$ (100 μF). The undershoot/overshoot voltages and settling times of the rccBuck converters are comparable with those of the buck converters.

Table 5-2. Load-transient comparison for the buck and rccBuck converters with measured waveforms in Fig. 5-33; transient responses of commercial products in [173]–[175] are also included.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>$C_o$ (μF)</th>
<th>$f_s$ (MHz)</th>
<th>Load Change</th>
<th>Undershoot Voltage</th>
<th>Step-up Settling time</th>
<th>Overshoot Voltage</th>
<th>Step-down Settling time</th>
</tr>
</thead>
<tbody>
<tr>
<td>OKL2-T/12-W12</td>
<td>188</td>
<td>0.4</td>
<td>6 – 12 A</td>
<td>0.12 V</td>
<td>30 μs @ 1.2%</td>
<td>0.15 V</td>
<td>30 μs @ 1.2%</td>
</tr>
<tr>
<td>LTM4633</td>
<td>200</td>
<td>0.7</td>
<td>0 – 5 A</td>
<td>0.14 V</td>
<td>55 μs @ 2.0%</td>
<td>0.14 V</td>
<td>46 μs @ 2.0%</td>
</tr>
<tr>
<td>LTM4649</td>
<td>440</td>
<td>0.75</td>
<td>5 – 10 A</td>
<td>0.10 V</td>
<td>15 μs @ 2.0%</td>
<td>0.10 V</td>
<td>15 μs @ 2.0%</td>
</tr>
<tr>
<td>RCC (PM = 33°)</td>
<td>100</td>
<td>2</td>
<td>4 – 13 A</td>
<td>0.12 V</td>
<td>22 μs @ 2.5%</td>
<td>0.16 V</td>
<td>18 μs @ 2.5%</td>
</tr>
<tr>
<td>RCC (PM = 56°)</td>
<td>100</td>
<td>2</td>
<td>4 – 13 A</td>
<td>0.12 V</td>
<td>25 μs @ 2.5%</td>
<td>0.17 V</td>
<td>20 μs @ 2.5%</td>
</tr>
<tr>
<td>Buck (PM = 50°)</td>
<td>100</td>
<td>2</td>
<td>4 – 13 A</td>
<td>0.17 V</td>
<td>24 μs @ 2.5%</td>
<td>0.17 V</td>
<td>24 μs @ 2.5%</td>
</tr>
</tbody>
</table>

5.8 Conclusion

The average-behavior small signal model is accurate for frequency up to $f_s/2$. It predicts the double pole and RHP zero of $L_r$ and $C_r$. If the resonant frequency of $L_r$ and $C_r$ is much higher than that of $L_o$ and $C_o$, the $G_{vd}$ could be simplified to (5-8). If their resonant frequencies are very close, the complete $G_{vd}$ in (5-7) should be used.

The rccBuck converter has the drawbacks of low dc gain and RHP zero compared with the buck converter without input filters. The conventional type-III compensator cannot meet the phase margin requirement. A front-stage phase-lead compensation network is added to increase the phase margin from 33° to 56° with 100 kHz bandwidth. The input filter in the buck converter would
cause 60% lower bandwidth, three times larger $C_0$, and doubled settling time during a load transient, compared to the rccBuck converter with the same EMI spectrum. For the PWM generator, the $D_{\text{Min}}$, $D_{\text{Max}}$, and dead time are controlled by external threshold voltages and triangular waveforms. In practice, the dead time should be controlled by the zero-cross point of drain-to-source voltage of the MOSFETs [177]–[178]. The goal of the adaptive dead time is to realize ZVS with the minimum dead time when the input voltage or load current varies.

Compared with the commercial 12 V to 3.3 V buck regulators, the rccBuck converter has a smaller output capacitor while maintaining the load-transient response. A low-frequency noise was observed in the load-transient experiment. It is expected to be solved in the future by optimizing the layout of the power stage and control board.
Chapter 6  Conclusions and Future Work

6.1 Summary of Work

Conventional point-of-load converters have low output voltage, high current, and usually hard-switched. They have high di/dt during the active switch turn-on due to the fast switching speed or reverse-recovery effect. A tiny parasitic inductance would induce voltage overshoot, as well as EMI noise, on the switched node. The voltage overshoot is about 40% \( V_{\text{in}} \) for a GaN-based buck converter with a state-of-the-art layout. The traditional QSW ZVS buck converters have no such problem, but the switches and inductors must conduct a high current ripple, which is detrimental to converter efficiency.

The resonant cross-commutated buck (rccBuck) converter is put forward in this dissertation to realize ZVS and reduce the noise, while maintaining efficiency, size, and transient response. The operation principles of this converter are introduced in Chapter 2. The switched stages and steady-state waveforms under continuous voltage mode (CVM) or discontinuous voltage mode (DVM) are analyzed. The gain and stress curves are obtained by using the state-space model. The RMS current of the active switch in the rccBuck converter is 20% smaller at nominal load, and 50% smaller at 20% load, than that in the QSW buck converter. The turn-off current of the active switch is reduced by 40% at \( V_o = 3.3 \) V under CVM. The turn-off current is almost zero under DVM when ZCS, or near-ZCS, is achieved. The CVM is recommended if the design target is to maximize the heavy-load efficiency, and DVM is recommended if the design target is to maximize the light-load efficiency. Both operation modes were verified experimentally by using Si-based rccBuck converters with air-core inductors.

The air-core inductors with relatively high volume are replaced by one-turn inductors in
Chapter 3. The core loss densities of MHz magnetic materials are compared. The 3F46 is suggested due to the lowest core loss density and the most stable property. The time-domain core loss of the inductor with an irregular voltage waveform is modeled by the EEL method. The modeled core loss matches well with the 2-D simulated one. The ac winding loss is also modeled by calculating the magnetic field strength on the top surface of the winding. Both horizontal and orthogonal fields are included. The inductor with two vertical gaps is suggested because of the lowest $R_{ac}$. A 0.25 mm distance between the winding and the gap is recommended to overcome the high ac resistance problem in the commercial one-turn inductors. Four one-turn inductors were designed, and fabricated. They gave 2% higher system efficiency, compared to the commercial inductors with the same inductances and double total volume, in the same rccBuck converter. The rccBuck converter with ZVS operation achieves ~15 dB lower conducted-EMI noise in 100 – 500 MHz than that of a hard-switched buck converter at nominal load.

In order to further reduce the magnetic volume, four inductors are coupled in Chapter 4. The concept of Omni-coupled inductors is implemented by a twisted E-E core with PCB windings. The $K_{nrb}$ and $K_{aoob}$ are positive when the horizontal-gap reluctance ($R_{g3}$) is smaller than the center-leg-gap reluctance ($R_{g2}$) and are negative when $R_{g3} > R_{g2}$. The mutual inductances, leakage inductances, and core loss are calculated from the reluctance network. The ac winding loss is analyzed by using a finite-element simulation. The simulated total loss of a twisted E-E core is 25% smaller than that of a traditional E-E core. A 3.3 V GaN-based rccBuck converter with Omni-coupled inductors was fabricated and achieved a 57% reduction of magnetic volume and 0.5% efficiency improvement, compared to the rccBuck converter with discrete one-turn inductors.

Chapter 5 introduces the small-signal modeling of the rccBuck converter with discrete inductors. Compared with the buck converter, the rccBuck converter has a lower dc gain, one more
double pole, and an additional right-half-plane zero. A conventional type-III compensator cannot meet the phase margin requirement; thus, a phase-lead compensation is added to achieve a 56° phase margin with 100 kHz bandwidth. The transient performance of a 0.12 V overshoot and 25 μs settling time under a 4 – 13 A load change, is comparable to that of a buck converter with the same bandwidth and similar phase margin (50°). The input filter in a buck converter was verified by simulation to have 60% lower bandwidth, three times larger C0, and doubled settling time during a load transient, compared to the rccBuck converter with the same EMI spectrum.

All rccBuck converters built in this dissertation are summarized in Table 6-1. The GaN-based CVM rccBuck converter with the designed one-turn inductors, described in Chapter 3, is recommended for 1.2 V POL applications. The GaN-based CVM rccBuck converter with OCI, described in Chapter 4, is recommended for 3.3 V POL applications.

Table 6-1. Fabricated rccBuck converters for POL applications with \( V_o = 1.2 \) V and 3.3 V

<table>
<thead>
<tr>
<th>Chapter 2</th>
<th>Chapter 3</th>
<th>Chapter 4</th>
<th>Chapter 5</th>
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<tr>
<td>( V_o = 1.2 ) V&lt;br&gt;Si-based, CVM, air core&lt;br&gt;• 83.7% at 20 A, 2 MHz&lt;br&gt;• 74.0% at 5 A, 2.4 MHz&lt;br&gt;• 27 × 22 × 15 mm³</td>
<td>( V_o = 1.2 ) V&lt;br&gt;GaN-based, CVM&lt;br&gt;commercial one-turn L&lt;br&gt;• 86.1% at 20 A, 2 MHz&lt;br&gt;• 73.2% at 5 A, 2.5 MHz&lt;br&gt;• 17 × 23 × 11 mm³</td>
<td>( V_o = 3.3 ) V&lt;br&gt;GaN-based, CVM&lt;br&gt;Round-wire one-turn L&lt;br&gt;• 95.4% at 20 A, 2 MHz&lt;br&gt;• 91.4% at 5 A, 2 MHz&lt;br&gt;• 17 × 23 × 15 mm³</td>
<td>( V_o = 3.3 ) V&lt;br&gt;GaN-based, CVM&lt;br&gt;Round-wire one-turn L&lt;br&gt;( I_o = 4 – 13 ) A transient&lt;br&gt;• 100 kHz bandwidth&lt;br&gt;• 56° phase margin&lt;br&gt;• 0.12 V overshoot of ( V_o )&lt;br&gt;• 25 μs settling time&lt;br&gt;• Transient response comparable to buck without input filter&lt;br&gt;• 75% ( C_o ) and 50% settling time reduction compared to the buck converter with input filter to achieve the same EMI (verified by simulation)</td>
</tr>
<tr>
<td>( V_o = 1.2 ) V&lt;br&gt;Si-based, DVM, air core&lt;br&gt;• 82.3% at 20 A, 2 MHz&lt;br&gt;• 76.1% at 5 A, 2.4 MHz&lt;br&gt;• 27 × 22 × 15 mm³</td>
<td>( V_o = 1.2 ) V&lt;br&gt;GaN-based, CVM&lt;br&gt;Flat-wire one-turn L&lt;br&gt;• 88.2% at 20 A, 2 MHz&lt;br&gt;• 78.4% at 5 A, 2.5 MHz&lt;br&gt;• 0.6% higher eff. than buck&lt;br&gt;• 17 × 23 × 7.6 mm³&lt;br&gt;• Size comparable to buck&lt;br&gt;• ( v_{oc} ) overshoot &lt; 1 V at 20A&lt;br&gt;• 15 dB lower conducted EMI at 100–500 MHz</td>
<td>( V_o = 3.3 ) V&lt;br&gt;GaN-based, CVM&lt;br&gt;Omni-coupled inductors&lt;br&gt;• 95.9% at 20 A, 2 MHz&lt;br&gt;• 96.2% at 17 A, 2 MHz&lt;br&gt;• 92.3% at 5 A, 2 MHz&lt;br&gt;• 3.3% higher eff. than buck&lt;br&gt;• 17 × 23 × 5.5 mm³&lt;br&gt;• 43% smaller size than buck&lt;br&gt;• ( v_{oc} ) overshoot &lt; 1 V at 20A&lt;br&gt;• 15 dB lower conducted EMI at 100–500 MHz</td>
<td>( V_o = 3.3 ) V&lt;br&gt;GaN-based, CVM&lt;br&gt;Round-wire one-turn L&lt;br&gt;( L_o = 0.5 ) and 1&lt;br&gt;• 93.8% at 20 A, 2 MHz&lt;br&gt;• 86.7% at 5 A, 2 MHz&lt;br&gt;• 27 × 22 × 15 mm³</td>
</tr>
</tbody>
</table>
In summary, an rccBuck regulator solves the turn-on noise of hard-switched converters by additional resonant tanks. Converter efficiency increases since ZVS is guaranteed for all switches within an entire load range. Steady-state modeling is given to guide the power stage design. Power density is maintained as the resonant inductors are coupled with the output inductors. The additional resonant tanks lead to additional double poles and right-half-plane zeros. However, the dynamic response of the fourth-order rccBuck regulator, using a modified type III compensator, is comparable to that of a second-order buck regulator. The RCC concept can be extended for other topologies and multi-phase converters to achieve higher voltage gain or higher power level.

6.2 Future Work

Due to the high current ripple, the light-load efficiency of the rccBuck converter is still lower than that of the state-of-the-art POL power module. A straight-forward method to reduce the current ripple is to increase the switching frequency, but this is limited by the driving loss. The discontinuous current mode may be helpful for the current ripple, but the ZVS is difficult to achieve, and the control is complicated. A clamped switch, paralleling the output inductor, is a potential method to reduce the current ripple at light load while maintaining the switching frequency [176]. That method will be applied in the rccBuck converter to improve the light-load efficiency.

The active switches of the rccBuck converter are subjected to the voltage stress of $2(V_{in} - V_o)$, which limits this converter in 48 V – 1 V applications. The input inductors $L_{ra/b}$ could be replaced by two switches to reduce the voltage stress to $V_{in}$. The capacitor $C_r$ could be replaced by a $L_r$-$C_r$ resonant tank to realize ZVS for all switches and ZCS for synchronous switches.

Chapter 5 provides only the transfer function of the rccBuck converter with discrete inductors.
The small-signal modeling of the OCI-rccBuck converter will be studied in the future. The mutual and leakage inductances must be considered in that model. The compensator will also be optimized to maximize the phase margin and bandwidth.

A low-frequency (~ 20 kHz) noise existed in the load-transient experiment in Chapter 5. This noise might be caused by the CM paths of the auxiliary power supplies and function generators. The power stage and the control board, as well as the reference signals, will be integrated into one board, or one step further, one chip, to improve the noise immunity.

Future work also includes exploring the RCC topologies in other applications, studying the mechanism of irreversible core loss increase, modeling the ac winding loss of the OCI, and optimizing the layout of the OCI-rccBuck converter for a higher power density.

6.3 List of Publications

Journal Papers


Conference Papers


Appendix A Matlab Code for Steady-State Model of RccBuck Converter

Matlab code for the flowchart of Fig. 2-32. CVM, DVM, and coupled inductor are considered.

function result = rccBuckCVMDVM(Lr, Lo, Cr, Co, Io, Vin, D, fs, Krarb, Koaob, Kraob, Kraoa)
%Calculate waveforms of inductor current, capacitor voltage, FET current, and FET voltage
N = 400;   %Number of points in an interval
t1 = linspace(0,D/2/fs,N);
t2 = linspace(D/2/fs,1/2/fs,N);
t21= t2-t2(1);
T1 = t1(end);
T21 = t2(end)-t2(1);
%Inductance matrix; Krboa=Kraob and Krbob=Kraoa due to symmetric phases
L = [Lr,Krarb*Lr,Kraoa*sqrt(Lr*Lo),Kraob*sqrt(Lr*Lo);
     Krarb*Lr,Lr,Kraob*sqrt(Lr*Lo),Kraoa*sqrt(Lr*Lo);
     Kraoa*sqrt(Lr*Lo), Kraob*sqrt(Lr*Lo), Lo, Koaob*Lo;
     Kraob*sqrt(Lr*Lo), Kraoa*sqrt(Lr*Lo), Koaob*Lo, Lo];
vL1 = [-1 -1 0;  
     0 -1 0;  
     0 0 -1;  
     0 1 -1];
vL2 = [-1 0 0;  
     0 -1 0;  
     0 0 -1;  
     0 0 -1];
vLvin = [1;1;0;0];
%State matrix
A1=[zeros(4,4),L\vL1;  
     1/Cr 0 0 0 0 0 0;  
     1/Cr 1/Cr 0 -1/Co 0 0 0;  
     0 0 1/Co 1/Co 0 0 0];
B = [L\vLvin zeros(4,1);  
     0 0;  
     0 0;  
     0 -1/Co];
A2=[zeros(4,4),L\vL2;  
     1/Cr 0 0 0 0 0;  
     0 1/Cr 0 0 0 0;
\[ P = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}; \]

\[ U = [V_{in}; I_0]; \]

\[ \phi_1 = \expm(A_{21} \cdot T_{21}) \cdot \expm(A_{1} \cdot T_{1}); \]

\[ \text{intresult1} = \text{zeros}(7, 1); \]

\[ \text{intresult2} = \text{zeros}(7, 1); \]

\[ \text{for } i = 1 : N; \]

\[ \text{intresult1} = \text{intresult1} + \expm(A_{11} \cdot (T_{1} - t_{1}(i))) \cdot B \cdot U \cdot (T_{1}/N); \]

\[ \text{intresult2} = \text{intresult2} + \expm(A_{21} \cdot (T_{21} - t_{21}(i))) \cdot B \cdot U \cdot (T_{21}/N); \]

\[ \text{end} \]

\[ \phi_2 = \expm(A_{21} \cdot T_{21}) \cdot \text{intresult1} + \text{intresult2}; \]

\[ x_0 = (P - \phi_1) \backslash \phi_2; \] %Initial condition

\[ x_1d = \expm(A_{1} \cdot T_{1}) \cdot x_0 + \text{intresult1}; \] %Condition at t2

\[ %\text{Determine CVM or DVM} \]

\[ %x_1d(6) \text{is the } v_{Crb} \text{ at } t_2 \]

\[ \text{if } (x_1d(6) > 0) \text{ } %\text{CVM} \]

\[ \text{sys1} = \text{ss}(A_{1}, B, \text{eye}(7), \text{zeros}(7, 2)); \]

\[ \text{sys2} = \text{ss}(A_{2}, B, \text{eye}(7), \text{zeros}(7, 2)); \]

\[ U_t = [V_{in} \cdot \text{ones} \left( \text{length}(t_1), 1 \right), I_0 \cdot \text{ones} \left( \text{length}(t_1), 1 \right)]; \]

\[ [~, t_1, x_1] = \text{lsim} (\text{sys1}, U_t, t_1, x_0); \]

\[ x_20 = x_1 \left( \text{end}, . ; \right); \]

\[ [~, t_2, x_2] = \text{lsim} (\text{sys2}, U_t, t_{21}, x_20); \]

\[ t_s = t_2 \left( \text{end} \right) + t_2; \]

\[ t_3 = t_2 \left( \text{end} \right) + t_1; \]

\[ t_4 = t_2 \left( \text{end} \right) + t_2; \]

\[ i_{Lr1} = x_1 \left( . ; 1 \right); \]

\[ i_{Lr2} = x_2 \left( . ; 1 \right); \]

\[ i_{Lr} = x_1 \left( . ; 2 \right); \]

\[ i_{Lr2} = x_2 \left( . ; 2 \right); \]

\[ i_{Lo1} = x_1 \left( . ; 3 \right); \]

\[ i_{Lo2} = x_2 \left( . ; 3 \right); \]

\[ i_{Lb} = x_1 \left( . ; 4 \right); \]

\[ i_{Lb} = x_2 \left( . ; 4 \right); \]

\[ v_{Cr1} = x_1 \left( . ; 5 \right); \]

\[ v_{Cr2} = x_2 \left( . ; 5 \right); \]

\[ v_{Cr} = x_1 \left( . ; 6 \right); \]

\[ v_{Cr} = x_2 \left( . ; 6 \right); \]
%Inductor current under CVM
iLra = [x1(:,1);x2(:,1);x1(:,2);x2(:,2)];
iLrb = [x1(:,2);x2(:,2);x1(:,1);x2(:,1)];
iLoa = [x1(:,3);x2(:,3);x1(:,4);x2(:,4)];
iLob = [x1(:,4);x2(:,4);x1(:,3);x2(:,3)];
%Capacitor voltages under CVM
vCra = [x1(:,5);x2(:,5);x1(:,6);x2(:,6)];
vCrb = [x1(:,6);x2(:,6);x1(:,5);x2(:,5)];
%Output voltage
vCo = [x1(:,7);x2(:,7);x1(:,7);x2(:,7)];
vds1a1 = vCra1+vCrb1;
vds1a2 = vCra2;
vds1a3 = zeros(length(ts3),1);
vds1a4 = vCrb2;
%High-side MOSFET drain-to-source voltages
vds1a = [vds1a1;vds1a2;vds1a3;vds1a4];
vds1b = [vds1a3;vds1a4;vds1a1;vds1a2];
vswa1 = zeros(length(ts1),1);
vswa2 = zeros(length(ts2),1);
vswa3 = vCrb1;
vswa4 = zeros(length(ts4),1);
%Switched node voltages
vswa = [vswa1;vswa2;vswa3;vswa4];
vswb = [vswa3;vswa4;vswa1;vswa2];
id1a1 = zeros(length(ts1),1);
id1a2 = zeros(length(ts2),1);
id1a3 = iLob1-iLra1;
id1a4 = zeros(length(ts4),1);
id1a = [id1a1;id1a2;id1a3;id1a4]; %Channel current for M1a
id2a1 = iLoa1+iLob1-iLrb1-iLra1;
id2a2 = iLoa2-iLrb2;
id2a3 = zeros(length(ts3),1);
id2a4 = iLob2-iLra2;
id2a = [id2a1;id2a2;id2a3;id2a4]; %Channel current for M2a
frn = 1/2/pi/sqrt(Lr*Cr)/fs; %Normalized resonant frequency of Lr and Cr
Zrn = sqrt(Lr/Cr)/(Vin/Io); %Normalized impedance of Lr and Cr
result.Vcmode='CVM';
result.fs = fs;
result.Zrn = Zrn;
result.frn = frn;
result.time = time;
result.iLra = iLra;
result.iLrb = iLrb;
result.iLoa = iLoa;
result.iLob = iLob;
result.vCra = vCra;
result.vCrb = vCrb;
result.id1a = id1a;
result.id2a = id2a;
result.vswa = vswa;
result.vswb = vswb;
result.vds1a = vds1a;
result.vds1b = vds1b;
result.vo = vCo;
result.Vo = trapz(time,vCo)*fs;
result.Io = Io;
result.ILrRMS = sqrt(trapz(time,iLra.^2)*fs);
result.ILoRMS = sqrt(trapz(time,iLoa.^2)*fs);
result.ILrpp = max(iLra) - min(iLra);
result.ILopp = max(iLoa) - min(iLoa);
result.IhRMS = sqrt(trapz(time,id1a.^2)*fs);
result.IIRMS = sqrt(trapz(time,id2a.^2)*fs);
result.Ihoff = id1a3(end);
else %DVM
Ddvmguess=D/2; %Initial condition of (t2-t1)fs
options = optimset('MaxIter',20,'Display','off','TolX',1e-6,...
'MaxFunEvals',15,'TolFun',0.1);
%Calculate the t2-t1 by iteration such that vCrb=0 at t2
Ddvm = fminsearch(@(Ddvm) rccDVMcheckVcrb(Lr, Lo, Cr, Co, Io, Vin, D,...
Ddvm, fs, Krarb, Koaob, Kraob, Kraoa),Ddvmguess,options);
%Call DVM function
result = rccBuckDVM(Lr, Lo, Cr, Co, Io, Vin, D, Ddvm, fs, Krarb, Koaob, Kraob, Kraoa);
Zrn = sqrt(Lr/Cr)/(Vin/Io);
frn = 1/2/pi/sqrt(Lr*Cr)/fs;
result.Zrn = Zrn;
result.frn = frn;
result.Vcmode='DVM';
end
end
Sub-function of steady-state model of DVM rccBuck converter.

```matlab
function result = rccBuckDVM(Lr, Lo, Cr, Co, Io, Vin, D, Ddcm, fs, Krarb, Koaob, Kraob, Kraoa)
    N = 200;  %Number of points in an interval
    if (Ddcm>D); Ddcm = D-0.001; end;
    t1 = linspace(0,Ddcm/2/fs,N);
    t1d = linspace(Ddcm/2/fs,D/2/fs,N);
    t2 = linspace(D/2/fs,1/2/fs,N);
    t1d1 = t1d-t1d(1);
    t21d = t2-t2(1);
    T1 = t1(end);
    T1d = t1d(end)-t1d(1);
    T21d = t2(end)-t2(1);
    %Inductance matrix; Krboa=Kraob and Krbob=Kraoa due to symmetric phases
    L = [Lr,Krab*Lr,Kraoa*sqrt(Lr*Lo),Kraob*sqrt(Lr*Lo);
         Krarb*Lr,Lr,Kraob*sqrt(Lr*Lo),Kraoa*sqrt(Lr*Lo);
         Kraoa*sqrt(Lr*Lo), Kraob*sqrt(Lr*Lo), Lo, Koaob*Lo;
         Kraob*sqrt(Lr*Lo), Kraoa*sqrt(Lr*Lo), Koaob*Lo, Lo];
    vL1 = [-1 -1 0;
           0 -1 0;
           0 0 -1;
           0 1 -1];
    vL2 = [-1 0 0;
           0 -1 0;
           0 0 -1;
           0 0 -1];
    vL1d = [-1 0 0;
            0 0 0;
            0 0 -1;
            0 0 -1];
    vLvin = [1;1;0;0];
    A1=[zeros(4,4),L\vL1;
        1/Car 0 0 0 0 0 0 0;
        1/Car 1/Car 0 -1/Car 0 0 0;
        0 0 1/Co 1/Co 0 0 0 0];
    B = [L\vLvin zeros(4,1);
         0 0;
         0 0;
         0 -1/Co];
```

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\[ A_2 = \begin{bmatrix} \text{zeros}(4,4) & L_vL2 \\ 1/Cr & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/Cr & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/Co & 1/Co & 0 & 0 \\ 0 & 0 & 0 & 1/Co & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ \end{bmatrix}; \]

%DVM state for rccBuck
\[ A_{1d} = \begin{bmatrix} \text{zeros}(4,4) & L_vL1d \\ 1/Cr & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/Co & 1/Co \\ 0 & 0 & 0 & 1/Co & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ \end{bmatrix}; \]

\[ P = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ \end{bmatrix}; \]

\[ U = [\text{Vin};Io]; \]

\[ \phi_1 = \expm(A_2*T_{21d})*\expm(A_{1d}*T_{1d})*\expm(A_1*T_1); \]

\[ \text{intresult1} = \text{zeros}(7,1); \]

\[ \text{intresult2} = \text{zeros}(7,1); \]

\[ \text{intresult1d} = \text{zeros}(7,1); \]

for \( i = 1:N; \)
\[ \text{intresult1} = \text{intresult1} + \expm(A_1*(T_1-t_1(i)))*B*U*(T_1/N); \]
\[ \text{intresult1d} = \text{intresult1d} + \expm(A_{1d}*(T_{1d}-t_{1d1}(i)))*B*U*(T_{1d}/N); \]
\[ \text{intresult2} = \text{intresult2} + \expm(A_2*(T_{21d}-t_{21d}(i)))*B*U*(T_{21d}/N); \]
end

\[ \phi_2 = \expm(A_2*T_{21d})*\expm(A_{1d}*T_{1d})*\text{intresult1} + \expm(A_2*T_{21d})*\text{intresult1d} + \text{intresult2}; \]

\[ x_0 = (P-\phi_1) \backslash \phi_2; \quad \text{Initial condition at } t_1 \]

\[ \text{sys1} = \text{ss}(A_1,B,\text{eye}(7),\text{zeros}(7,2)); \]

\[ \text{sys1d} = \text{ss}(A_{1d},B,\text{eye}(7),\text{zeros}(7,2)); \]

\[ \text{sys2} = \text{ss}(A_2,B,\text{eye}(7),\text{zeros}(7,2)); \]

\[ \text{Ut} = [\text{Vin}\ast \text{ones(length(t1)),Io}\ast \text{ones(length(t1),1)}]; \]

\[ [~,ts1,x1]=\text{lsim(sys1,Ut,t1,x0)}; \]
\[ x1d0 = x1(\text{end},:); \]
\[ x1d0(6) = 0; \quad \text{Force the } vCrb \text{ at } t_2 \text{ to be zero; avoid the tolerance effect} \]

\[ [~,ts1d,x1d]=\text{lsim(sys1d,Ut,t1d1,x1d0)}; \]
\[ x20 = x1d(\text{end},:); \]
\[ [~,ts2,x2]=\text{lsim(sys2,Ut,t21d,x20)}; \]
\[ ts1d = ts1(\text{end}) + ts1d; \]
\[ ts2 = ts1d(\text{end}) + ts2; \]
\[ ts3 = ts1 + 0.5/fs; \]
\[ ts3d = ts1d + 0.5/fs; \]
\[ ts4 = ts2 + 0.5/fs; \]
iLra1=x1(:,1);
iLra1d=x1d(:,1);
iLra2=x2(:,1);
iLrb1=x1(:,2);
iLrb1d=x1d(:,2);
iLrb2=x2(:,2);
iLoa1=x1(:,3);
iLoa1d=x1d(:,3);
iLoa2=x2(:,3);
ilob1=x1(:,4);
ilob1d=x1d(:,4);
ilob2=x2(:,4);

%Calculation of inductor current
iLra = [x1(:,1);x1d(:,1);x2(:,1);x1(:,2);x1d(:,2);x2(:,2)];
iLrb = [x1(:,2);x1d(:,2);x2(:,2);x1(:,1);x1d(:,1);x2(:,1)];
iLoa = [x1(:,3);x1d(:,3);x2(:,3);x1(:,4);x1d(:,4);x2(:,4)];
ilob = [x1(:,4);x1d(:,4);x2(:,4);x1(:,3);x1d(:,3);x2(:,3)];

%Calculation of capacitor voltages
vCra = [x1(:,5);x1d(:,5);x2(:,5);x1(:,6);x1d(:,6);x2(:,6)];
vCrb = [x1(:,6);x1d(:,6);x2(:,6);x1(:,5);x1d(:,5);x2(:,5)];

%Calculation of MOSFET voltages
vds1a1 = vCra1+vCrb1;
vds1a1d = vCra1d;
vds1a2 = vCra2;
vds1a3 = zeros(length(ts3),1);
vds1a3d = zeros(length(ts3d),1);
vds1a4 = vCrb2;
vds1a = [vds1a1;vds1a1d;vds1a2;vds1a3;vds1a3d;vds1a4];
vds1b = [vds1a3;vds1a3d;vds1a4;vds1a1;vds1a1d;vds1a2];
vswa1 = zeros(length(ts1),1);

vswa1d = zeros(length(ts1d),1);
vswa2 = zeros(length(ts2),1);
vswa3 = vCrb1;

vswa3d = zeros(length(ts3d),1);
vswa4 = zeros(length(ts4),1);
vswa = [vswa1;vswa1d;vswa2;vswa3;vswa3d;vswa4];
vswb = [vswa3;vswa3d;vswa4;vswa1;vswa1d;vswa2];
%Calculation of channel current
id1a1 = zeros(length(ts1),1);
id1a1d = zeros(length(ts1d),1);
id1a2 = zeros(length(ts2),1);
id1a3 = iLob1-iLra1;
id1a3d = iLrb1d;
id1a4 = zeros(length(ts4),1);
id1a = [id1a1;id1a1d;id1a2;id1a3;id1a3d;id1a4];
id2a1 = iLoa1+iLob1-iLrb1-iLra1;
id2a1d = iLoa1d;
id2a2 = iLoa2-iLrb2;
id2a3 = zeros(length(ts3),1);
id2a3d = iLob1d-(iLra1d+iLrb1d);
id2a4 = iLob2-iLra2;
id2a = [id2a1;id2a1d;id2a2;id2a3;id2a3d;id2a4];
time = [ts1;ts1d;ts2;ts3;ts3d;ts4];

%Normalized impedance and resonant frequency
Zrn = sqrt(Lr/Cr)/(Vin/Io);
frn = 1/2/pi/sqrt(Lr*Cr)/fs;

%Output struct
result.Vcmode='DVM';
result.fs = fs;
result.Zrn = Zrn;
result.frn = frn;
result.time = time;
result.iLra = iLra;
result.iLrb = iLrb;
result.iLoa = iLoa;
result.iLob = iLob;
result.vCra = vCra;
result.vCrb = vCrb;
result.id1a = id1a;
result.id2a = id2a;
result.vswa = vswa;
result.vswb = vswb;
result.vds1a = vds1a;
result.vds1b = vds1b;
result.vo = vCo;
result.Vo = trapz(time,vCo)*fs;
result.Io = Io;
result.Vo = trapz(time,vCo)*fs;
result.IlrRMS = sqrt(trapz(time,iLra.^2)*fs);  
result.iloRMS = sqrt(trapz(time,iLoa.^2)*fs);  
result.IhrRMS = sqrt(trapz(time,id1a.^2)*fs);  
result.IlrRMS = sqrt(trapz(time,id2a.^2)*fs);  
result.Ihoff = id1a3d(end);  
end

Sub-function to check the capacitor voltage at t2.

function deltaV = rccDVMcheckVcrb(Lr, Lo, Cr, Co, Io, Vin, D, Ddvm, fs, Krarb, Koaob, Kraob, Kraoa)  
% Output is the vCrb at t2  
N = 200;  
% Number of points in an interval  
if (Ddvm>D); Ddvm = D-0.001; end;  
% Ddvm should be smaller than D  
t1 = linspace(0,Ddvm/2/fs,N);  
t1d = linspace(Ddvm/2/fs,D/2/fs,N);  
t2 = linspace(D/2/fs,1/2/fs,N);  
t1d1 = t1d-t1d(1);  
t21d =t2-t2(1);  
T1 = t1(end);  
T1d = t1d(end)-t1d(1);  
T21d = t2(end)-t2(1);  
% Inductance matrix; Krboa=Kraob and Krbob=Kraoa due to symmetric phases  
L = [Lr,Krab^*Lr,Kraoa*sqrt(Lr*Lo),Kraob*sqrt(Lr*Lo);  
     Krarb^*Lr,Lr,Kraob*sqrt(Lr*Lo),Kraoa*sqrt(Lr*Lo);  
     Kraoa*sqrt(Lr*Lo), Kraob*sqrt(Lr*Lo), Lo, Koaob*Lo;  
     Kraob*sqrt(Lr*Lo), Kraoa*sqrt(Lr*Lo), Koaob*Lo, Lo];  
vL1 = [-1 -1 0;  
     0 -1 0;  
     0 0 -1;  
     0 1 -1];  
vL2 = [-1 0 0;  
     0 -1 0;  
     0 0 -1;  
     0 0 -1];  
vL1d = [-1 0 0;  
     0 0 0;  
     0 0 -1;  
     0 0 -1];
vLvin = [1;1;0;0];
A1=[zeros(4,4),L\vL1;
    1/Cr 0 0 0 0 0 0;
    1/Cr 1/Cr 0 -1/Cr 0 0 0;
    0 0 1/Co 1/Co 0 0 0];
B = [L\vLvin zeros(4,1);
    0 0;
    0 0;
    0 -1/Co];
A2=[zeros(4,4),L\vL2;
    1/Cr 0 0 0 0 0 0;
    0 1/Cr 0 0 0 0 0;
    0 0 1/Co 1/Co 0 0 0];

% DVM state of rccBuck
A1d=[zeros(4,4),L\vL1d;
    1/Cr 0 0 0 0 0 0;
    0 0 0 0 0 0 0;
    0 0 1/Co 1/Co 0 0 0];
P = [0 1 0 0 0 0 0;
    1 0 0 0 0 0 0;
    0 0 1 0 0 0 0;
    0 0 0 0 1 0 0;
    0 0 0 0 0 1 0;
    0 0 0 0 0 0 1];
U = [Vin;Io];
phi1 = expm(A2*T21d)*expm(A1d*T1d)*expm(A1*T1);
intresult1=zeros(7,1);
intresult2=zeros(7,1);
intresult1d=zeros(7,1);
for i=1:N;
    intresult1=intresult1+expm(A1*(T1-t1(i)))*B*U*(T1/N);
    intresult1d=intresult1d+expm(A1d*(T1d-t1d1(i)))*B*U*(T1d/N);
    intresult2=intresult2+expm(A2*(T21d-t21d(i)))*B*U*(T21d/N);
end
phi2 = expm(A2*T21d)*expm(A1d*T1d)*intresult1+expm(A2*T21d)*intresult1d+intresult2;
x0=(P-phi1)\phi2; % Initial condition at t1
x1d=expm(A1*T1)*x0+intresult1; % Condition at t2
deltaV = abs(x1d(6)); % vCrb at t2
Appendix B Matlab Code for Core Loss and Winding

Loss of One-Turn Gapped Inductor

Steady-state core loss without dc effect of one-turn inductor for Section 3.5.

```matlab
function result = OneTurnCoreLoss_0dc(t,VL,Ae,le,Cm,alpha,beta)
    % Zero-bias Core loss for one-turn inductor by EEL method
    % (t,VL) is the voltage waveform across the inductor
    % Ae is effective cross-sectional area; le is effective length
    % Cm,alpha, and beta are core loss coefficients
    % Pvo[W/m^3]=Cm*f[Hz]^alpha*Bm[T]^beta
    if length(t)~=length(VL)
        error('t and VL should have same numbers!');
    else
        N = length(t);
    end
    B = cumtrapz(t,VL)/Ae; % Instantaneous B(t)
    Bmax = max(B);
    Bmin = min(B);
    Bdc = (Bmax+Bmin)/2;
    Bm = (Bmax-Bmin)/2; % Ac flux density
    theta = linspace(0,pi/2,N);
    Cab = (2*pi)^alpha*2/pi*trapz(theta,(cos(theta)).^beta);
    costheta = sqrt(1-(B-Bdc)/Bm).^2);
    K = 1/Cab*Cm*(Bm*costheta).^(beta-alpha);
    dBdt = diff(B)./diff(t);
    dBdt(N) = dBdt(N-1);
    Pv = abs(K.*dBdt.^alpha); % Instantaneous core loss density
    Volume = Ae*le;
    result.Pv = Pv;
    result.B = B;
    result.Bm = (max(B)-min(B))/2;
    result.Vol = Volume;
    result.CLt = Pv*Volume; % Instantaneous core loss without bias
    result.CL = trapz(t,Pv*Volume)/(max(t)-min(t)); % Total core loss
end
```

Ac resistance of one-turn inductor for Section 3.5.
function [ Rdc, Rac ] = OneTurnRac_2gaps(f,ww,hw,lg,lwg,lc)
%Aac resistance of one-turn inductor with two vertical gaps
%f: frequency
%ww: winding width
%hw: winding thickness
%lg: single gap length
%lwg: distance from winding to gap
%lc: core length
sigma = 5.8e7; %copper conductivity
mu0 = 4*pi*1e-7; %vacuum permeability
skindept = sqrt(1/pi/f/mu0/sigma); %skin depth
N = 300; %number of points along the winding for analysis
wwnom = ww/skindept; %normalized winding width
%ky: correction factor for Hy
if (wwnom<10.7), ky=0;
elseif (wwnom>85.6), ky=0.55;
else
    ky=2.12e-6*wwnom^3-0.0004197*wwnom^2+0.02989*wwnom-0.2726;
end
xsweep = linspace(-ww/2,ww/2,N);
Hg = 0.9/lg; %Approximated H in the gap
%Calculation of Hx and Hy along top winding surface
for i=1:length(xsweep)
    x = xsweep(i);
    y = lwg;
    if((x^2+y^2)>(lg^2/4))
        m=0;
    else
        m=1;
    end
    Hy(i)=-Hg/2/pi*log((y^2+(x+lg/2).^2)./(y^2+(x-lg/2).^2));
    Hx(i)=-Hg/pi*(atan(y*lg/(x^2+y^2-lg^2/4))+m*pi);
end
xsweep = xsweep';
Hy=Hy';
deltaHy = xsweep*(Hy(end)-Hy(1))/ww;
Hy = Hy-deltaHy; %Linear substraction
Hx=Hx';
kself = 1/(mean(Hx)*ww); %Integration of Hx should satisfy Ampere's law
Hxkself = Hx*kself/2; %Half field for two gaps
Hy = Hy/2; %Half field for two gaps
Hxavg = sqrt(mean(Hxkself.^2));
Hyavg = sqrt(mean(Hy.^2));
P_x = 1/2*ww/sigma/skindept*Hxavg^2; %Winding loss caused by Hx
P_y = 1/2*ww/sigma/skindept*Hyavg^2*ky; %Winding loss caused by Hy
Rac = (Px+Py)*2*lc*2;   %Ac resistance
Rdc = 1/(sigma*ww*hw)*lc;   %Dc resistance
end

Total loss of Lr and Lo in the rccBuck converter for Table 3-3.

clc;
%Circuit information
Vin = 12;   %Input voltage
Io = 20;    %Output current
fs = 2e6;   %Switching frequency
D = 0.24;   %Duty ratio
Co = 10e-6; %Output Cap
Lr = 69e-9; %Resonant L
Lo = 38e-9; %Output L
Cr = 264e-9; %Resonant Cap
%Inductor current and voltage
result = rccBuckCVMDVM(Lr, Lo, Cr, Co, Io, Vin, D, fs, 0, 0, 0, 0);
[time,index]=unique(result.time); %Remove duplicated points
ILrmax = max(result.iLra);
ILomax = max(result.iLob);
vLra = Vin-result.vds1a-result.vswa;
vLob = result.vswb-result.vo;
vLra = vLra(index); %Instantaneous voltage of Lra
vLob = vLob(index); %Instantaneous voltage of Lob
iLra = result.iLra(index); %Instantaneous current of Lra
iLob = result.iLob(index); %Instantaneous current of Lob
ILodc = Io/2;
ILrdc = ILodc*result.Vo/Vin;
ILrRMS = result.ILrRMS;
ILoRMS = result.ILoRMS;
%Material properties of 3F46
Cm = 5.567e-6;
alpha = 2.215;
beta = 2.29;
mur = 710; %Relative permeability
mu0 = 4*pi*1e-7; %Vacuum permeability
%Core dimensions
lgLr = 0.2e-3; %Total gap length
lgLo = 0.5e-3;
wwLr = 2e-3;    %Winding width
wwLo = 2e-3;
lwgLr = 0.5e-3; %Total vertical distance from winding to gap
lgwLo = 0.5e-3;
hwLr = 0.25e-3; %Winding thickness
hwLo = 0.5e-3;
wclr = 1.2e-3; %Core width
wcllo = 1.2e-3;
lclr = 7.6e-3; %Core length
lcllo = 8.4e-3;
AeLr = (wclr+lgLr/2)*(lclr);
AeLo = (wcllo+lgLo/2)*(lcllo);
leLr = 2*(wwLr+lwgLr+hwLr+wcLr*pi/4)-lgLr;
leLo = 2*(wwLo+lwgLo+hwLo+wcLo*pi/4)-lgLo;

%Zero-bias core loss
LrPv = OneTurnCoreLoss_0dc(time,vLra,AeLr,leLr,Cm,alpha,beta);
LoPv = OneTurnCoreLoss_0dc(time,vLob,AeLo,leLo,Cm,alpha,beta);

%Hdc = ILrdc/lgLr/mur;
KdcLr = 0.00053*HdcLr^2+0.0098*HdcLr+1; %3F46, Bm=20mT
KdcLo = 0.00053*HdcLo^2+0.0098*HdcLo+1;

%Ac resistances up to 4th-order harmonic
[Rdc_Lr,Rac_Lr] = OneTurnRac_2gaps(fs,wwLr,hwLr,lgLr/2,lwgLr/2,lclr);
[Rdc_Lo,Rac_Lo] = OneTurnRac_2gaps(fs,wwLo,hwLo,lgLo/2,lwgLo/2,lcllo);
[~,Rac_Lr_2] = OneTurnRac_2gaps(2*fs,wwLr,hwLr,lgLr/2,lwgLr/2,lclr);
[~,Rac_Lo_2] = OneTurnRac_2gaps(2*fs,wwLo,hwLo,lgLo/2,lwgLo/2,lcllo);
[~,Rac_Lr_3] = OneTurnRac_2gaps(3*fs,wwLr,hwLr,lgLr/2,lwgLr/2,lclr);
[~,Rac_Lo_3] = OneTurnRac_2gaps(3*fs,wwLo,hwLo,lgLo/2,lwgLo/2,lcllo);
[~,Rac_Lr_4] = OneTurnRac_2gaps(4*fs,wwLr,hwLr,lgLr/2,lwgLr/2,lclr);
[~,Rac_Lo_4] = OneTurnRac_2gaps(4*fs,wwLo,hwLo,lgLo/2,lwgLo/2,lcllo);

%Ac winding loss (1st-4th harmonics)
time2 = linspace(0,1/fs,length(time));
iLra2 = interp1(time,iLra,time2,’spline’);
P2Lr = abs(fft(iLra2)/length(iLra));
P1Lr = P2Lr(1:round(length(iLra)/2)+1);
P1Lr(2:end-1) = sqrt(2)*P1Lr(2:end-1); %FFT of inductor current
iLob2 = interp1(time,iLob,time2,'spline');
P2Lo = abs(fft(iLob2)/length(iLob));
P1Lo = P2Lo(1:round(length(iLob)/2)+1);
P1Lo(2:end-1) = sqrt(2)*P1Lo(2:end-1);
PacwLr = sum(P1Lr(2:5).^2.*[Rac_Lr,Rac_Lr_2,Rac_Lr_3,Rac_Lr_4]);
PacwLo = sum(P1Lo(2:5).^2.*[Rac_Lo,Rac_Lo_2,Rac_Lo_3,Rac_Lo_4]);
%Dc winding loss
PdcwLr = ILrdc^2*Rdc_Lr;
PdcwLo = ILOdc^2*Rdc_Lo;
%Total loss and volume
PLr = (PvLr+PacwLr+PdcwLr)*1e3; %mW
PLo = (PvLo+PacwLo+PdcwLo)*1e3;
VolLr = ((2*wcLr+wwLr)*(2*wcLr+lwgLr+hwLr)*lcLr*1e9); %mm^3
VolLo = ((2*wcLo+wwLo)*(2*wcLo+lwgLo+hwLo)*lcLo*1e9);
Appendix C Matlab Code for Inductance, Core Loss and Pareto Fronts of Omni-Coupled Inductors (OCI)

Modeled inductances and coupling coefficients of the OCI in Section 4.4.

```matlab
function result = OCI_Lmat(wc1,wc2,wLr,wLo,lc,lg1,lg2,lg3,h1,fs,hw,Npcb,lww,lwc)
%Inductances and coupling coefficients of OCI with twisted E-E core
%wc1 & wc2: core widths  lc: core length
%wLr & wLo: winding widths
%lg1, lg2, and lg3: gap lengths
%h1: window height
%fs: switching frequency
%hw: winding thickness of each layer
%Npcb: number of PCB layers
%lww: horizontal winding space
%lwc: horizontal space between winding and gap
mu0 = 4*pi*1e-7;  %vacuum permeability
hc = wc1*2+h1;    %total core height
lc2 = (lc-lg3)/2;
h2 = (hc-lg2)/2;
p = 1.68e-8;      %copper resistivity
%Impact of eddy effect on winding width
alpha = sqrt(1j*2*pi*fs*mu0/p);
M = alpha*wLo*coth(alpha*wLo);
M2pri = imag(M);
FLo = abs(3*M2pri/abs(alpha^2*wLo^2));
M = alpha*wLr*coth(alpha*wLr);
M2pri = imag(M);
FLr = abs(3*M2pri/abs(alpha^2*wLr^2));
%Gap reluctances
Rg1 = lg1/(lc+lg1)/(wc1+lg1)/mu0;
Rg2 = lg2/(lc2+lg2)/(wc2+lg2)/mu0;
Rg3 = lg3/(lc+lg3+wc2+lg3/2)/(wc1/2+h2/2+lg3/2)/mu0;
RgLr = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lww+lwc)/mu0);
RgLr_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
RgLro_2 = paralleln((h1-Npcb*hw+Npcb*hw/Flr)/(lc+h1)/(wLr-lg3/2)/mu0,h1/(lc+h1)/(lwc)/mu0);
RgLro = paralleln(RgLr_2,RgLr_2,h1/(lc+h1)/(lww)/mu0); %Reluctance of RgLr//RgLr
```
R4 = (Rg1ro*Rg2+Rg1ro*Rg3+2*Rg2*Rg3)/(2*Rg1ro+Rg2+Rg3);

%Self inductances
Lo = 1/(Rg1+RgLr*R4/(RgLr+R4));
Lr = 1/(Rg1*RgLo/(Rg1+RgLo)+R4);

%Mutual inductances
Mraob = -1/(Rg1+R4)+sqrt((1/(Rg1+R4))^2-1/(Rg1+R4)*(Lr+Lo)+Lr*Lo);
Mraoa = -Lo*RgLr/(Rg3+RgLr-(2*RgLr+Rg3+Rg2)/(Rg3-Rg2)*(Rg3+Rg1ro));
Mrarb = 1/(Rg3+Rg1*RgLo/(Rg1+RgLo))-Lr;
Moaob = 1/(Rg1+Rg3*RgLr/(Rg3+RgLr))-Lo;

%Output
result.Lr = Lr;
result.Lo = Lo;
result.Lraob = Mraob;
result.Lrarb = Mrarb;
result.Loaoa = Moaob;
result.Lraoa = Mraoa;
result.Kraob = Mraob/sqrt(Lr*Lo);
result.Krarb = Mrarb/Lr;
result.Koaob = Moaob/Lo;
result.Kraoa = Mraoa/sqrt(Lr*Lo);
end

function paraout = paralleln( varargin )
%Parallel resistance or reluctance
N = nargin;
temp = cell2mat(varargin(1));
for i=2:N
    temp = temp*cell2mat(varargin(i))/(temp+cell2mat(varargin(i)));
end
paraout = temp;
end

Modeled core loss without dc bias effect for the OCI with a twisted E-E core in Section 4.5.

function result = OCI_CoreLoss(time,vLra,vLrb,Cm,alpha,beta,wc1,wc2,wLr,wLo,...
    ...lc/lg1/lg2/lg3/h1/fs/hw/Npcb/lww/lwc)
%Core loss without bias for OCI
mu0 = 4*pi*1e-7;  %vacuum permeability
hc = wc1*2+h1;    %total height
lc2 = (lc-lg3)/2;
h2 = (hc-lg2)/2;
p = 1.68e-8;   %copper resistivity
%Impact of eddy effect on winding width

\[
\alpha_2 = \sqrt{1j \cdot 2\pi \cdot f_s \cdot \mu_0 / p};
\]

\[
M = \alpha_2 \cdot w_{Lo} \cdot \coth(\alpha_2 \cdot w_{Lo});
\]

\[
M_{2pri} = \text{imag}(M);
\]

\[
F_{Lo} = \text{abs}(3 \cdot M_{2pri} / \text{abs}(\alpha_2^2 \cdot w_{Lo}^2));
\]

\[
M = \alpha_2 \cdot w_{Lr} \cdot \coth(\alpha_2 \cdot w_{Lr});
\]

\[
M_{2pri} = \text{imag}(M);
\]

\[
F_{Lr} = \text{abs}(3 \cdot M_{2pri} / \text{abs}(\alpha_2^2 \cdot w_{Lr}^2));
\]

%Gap reluctances

\[
R_{g1} = l_{g1} / (l_{c+g1}) / (w_{c1+g1}) / \mu_0;
\]

\[
R_{g2} = l_{g2} / (l_{c2+g2}) / (w_{c2+g2}) / \mu_0;
\]

\[
R_{g3} = l_{g3} / (l_{c+g3}+w_{c2+g3}) / (w_{c1+2h2/2+g3}) / \mu_0;
\]

\[
R_{gLr_2} = \text{parallel}(h_1 - N_{pcb} \cdot h_w + N_{pcb} \cdot h_w / F_{Lr}) / (l_{c+h1}) / (w_{Lr} - lg3/2) / \mu_0, h1 / (l_{c+h1}) / (l_{wLr}/\mu_0);
\]

\[
R_{gLr_2} = \text{parallel}(h_1 - N_{pcb} \cdot h_w + N_{pcb} \cdot h_w / F_{Lo}) / (l_{c+h1}) / w_{Lo} / (h1 / (l_{c+h1}) / (l_{wLr}/\mu_0);
\]

\[
R_{gro} = \text{parallel}(R_{gLr_2}, R_{gLr_2}, h1 / (l_{c+h1}) / (l_{ww}/\mu_0);
\]

\[
R_{g1ro} = R_{g1} \cdot R_{gro} / (R_{g1} + R_{gro});
\]

\[
R_{g1ro} = (R_{g1ro} + R_{g2}) * (l_{c/2+g3/2}) / (l_{c+wc2+g3}) / (2 * R_{g1ro} + R_{g2} + R_{g3});
\]

%voltage from Lrabo

\[
v_{ra1_1} = v_{Lra};
\]

\[
v_{ra1_2} = k_2 \cdot v_{Lra};
\]

\[
v_{ra1_3} = v_{Lra} - v_{ra1_2};
\]

\[
v_{ra1_4} = (R_{g1ro} + R_{g3}) / (2 * R_{g1ro} + R_{g2} + R_{g3}) \cdot v_{Lra};
\]

\[
v_{ra2_1} = (v_{Lra} - 2 \cdot v_{ra1_4});
\]

\[
v_{ra2_2} = v_{ra1_3} - v_{ra1_4};
\]

\[
v_{ra2_3} = v_{ra1_2} - v_{ra1_4};
\]

\[
v_{ra2_4} = v_{ra1_4};
\]

%voltage from Lrboa

\[
v_{rb2_1} = v_{Lrb};
\]

\[
v_{rb2_2} = k_2 \cdot v_{Lrb};
\]

\[
v_{rb2_3} = v_{Lrb} - v_{rb2_2};
\]

\[
v_{rb2_4} = -(R_{g1ro} + R_{g3}) / (2 * R_{g1ro} + R_{g2} + R_{g3}) \cdot v_{Lrb};
\]

\[
v_{rb1_1} = (v_{Lrb} + 2 \cdot v_{rb2_4});
\]

\[
v_{rb1_2} = v_{rb2_3} + v_{rb2_4};
\]

\[
v_{rb1_3} = v_{rb2_2} + v_{rb2_4};
\]

\[
v_{rb1_4} = v_{rb2_4};
\]

%totalvoltage

\[
v_{1_1} = v_{ra1_1} + v_{rb1_1};
\]

\[
v_{1_2} = v_{ra1_2} + v_{rb1_2};
\]

\[
v_{1_3} = v_{ra1_3} + v_{rb1_3};
\]

\[
v_{1_4} = v_{ra1_4} + v_{rb1_4};
\]
v2_1 = vra_2_1 + vrb_2_1;
v2_2 = vra_2_2 + vrb_2_2;
v2_3 = vra_2_3 + vrb_2_3;
v2_4 = vra_2_4 + vrb_2_4;

% Equivalent cross-sectional area and length
Ae1 = (wc1 + lg1*1) * (lc + lg1*1);
Ae2 = wc1 * (lc*k2);
Ae31 = wc1*1.2 * (lc*(1-k2));
Ae32 = (wc1+lg3/2) * (lc/2 + wc2+lg3);
Ae4 = (wc2+lg2*2) * (lc2-lg3/2+2*lg2);
le1 = 1/2 * wc1 + (h1-lg1)/2;
le2 = (wLr+wLo-lg3);
le31 = (wLr+wLo-lg3);
le32 = (wc2/2+lg3);
le4 = 1/2 * wc1 + (h1-lg1)/2;

% Calculate loss
P1_1 = OneTurnCoreLoss_0dc(time, v1_1, Ae1, le1, Cm, alpha, beta);
P1_2 = OneTurnCoreLoss_0dc(time, v1_2, Ae2, le2, Cm, alpha, beta);
P1_31 = OneTurnCoreLoss_0dc(time, v1_3, Ae31, le31, Cm, alpha, beta);
P1_32 = OneTurnCoreLoss_0dc(time, v1_3, Ae32, le32, Cm, alpha, beta);
P1_4 = OneTurnCoreLoss_0dc(time, v1_4, Ae4, le4, Cm, alpha, beta);
P2_1 = OneTurnCoreLoss_0dc(time, v2_1, Ae1, le1, Cm, alpha, beta);
P2_2 = OneTurnCoreLoss_0dc(time, v2_2, Ae2, le2, Cm, alpha, beta);
P2_31 = OneTurnCoreLoss_0dc(time, v2_3, Ae31, le31, Cm, alpha, beta);
P2_32 = OneTurnCoreLoss_0dc(time, v2_3, Ae32, le32, Cm, alpha, beta);
P2_4 = OneTurnCoreLoss_0dc(time, v2_4, Ae4, le4, Cm, alpha, beta);

% Core loss
result.CLt = 2*(P1_1.CLt+P1_2.CLt+P1_31.CLt+P1_32.CLt+P1_4.CLt+...
P2_1.CLt+P2_2.CLt+P2_31.CLt+P2_32.CLt+P2_4.CLt);
result.CL = 2*(P1_1.CL+P1_2.CL+P1_31.CL+P1_32.CL+P1_4.CL+...
P2_1.CL+P2_2.CL+P2_31.CL+P2_32.CL+P2_4.CL);
result.Bm = [P1_1.Bm,P1_2.Bm,P1_31.Bm,P1_32.Bm,P1_4.Bm];
end

function paraout = paralleln( varargin )
% Parallel resistance or reluctance
N = nargin;
temp = cell2mat(varargin(1));
for i = 2:N
    temp = temp * cell2mat(varargin(i)) / (temp + cell2mat(varargin(i)));
end
paraout = temp;
end
H_{dc} of OCI for Section 4.5.

function Hdc = OCI_Hdc(lo,in,mur,wc1,wc2,wLr,wLo,lc/lg1/lg2/lg3,h1)
    \%Hdc of OCI
    mu0 = 4*pi*1e-7; \%vacuum permeability
    hc = wc1*2+h1; \%total core height
    h2 = (hc-lg2)/2;
    \%gap reluctances
    Rg1 = lg1/(lc+lg1)/(wc1+lg1)/mu0;
    Rg3 = lg3/(lc+lg3+wc2+lg3)/(wc1/2+h2/2+lg3)/mu0;
    Rgro = h1/(lc+h1)/(wLr+wLo+lg3)/mu0;
    Hdc = (lo-in)/(Rg1*Rgro/(Rg1+Rgro)+Rg3)/2/wc1/lc/mur/mu0;
end

Pareto-fronts plot of OCI for Fig. 4-37 and Fig. 4-38.

clc;
tic;
\%nominal dimensions of OCI; max variation
lg1_nom = 0.15e-3; lg1_tol = 0.4;
lg3_nom = 0.5e-3; lg3_tol = 0.4;
wc1_nom = 1.5e-3; wc1_tol = 0.4;
wc2_nom = 2.2e-3; wc2_tol = 0.4;
\%fixed dimensions and circuit parameters
h1 = 1.5e-3; wLr = 1.2e-3; wLo = 3.2e-3; lc = 10e-3;
hw = 0.07e-3; Npcb = 4; lww = 0.2e-3; lwc = 0.2e-3;
Vin = 12; Io = 20; fs = 2e6; D = 0.76; Dps = 0.5;
Co = 2e-6; Cr = 8*4.7e-6; lcos = 2.5;
lin = Io*D/(2+D);
\%material properties of 3F46
Cm = 5.567e-6;
alpha = 2.2153;
beta = 2.2929;
mur = 710;
N = 400; \%sweep count
RdcLr = 0.616e-3; \%resistance at lc = 10 mm
RdcLo = 0.231e-3;
RacLo = 7.05e-3;
lc_max = 15e-3; \%max lc
i=0;
h = waitbar(0,'Please wait...');
for j=1:N
    %generate lg1,lg3,wc1,and wc2 randomly in specified ranges
    lg1 = lg1_nom*(1+lg1_tol*(2*rand-1));
    lg2 = lg1;
    lg3 = lg3_nom*(1+lg3_tol*(2*rand-1));
    wc1 = wc1_nom*(1+wc1_tol*(2*rand-1));
    wc2 = wc2_nom*(1+wc2_tol*(2*rand-1));
    %curve-fitted ac resistance at 2 MHz
    RacLr = (-38.88*(lg3*1e3)^3+62.012*(lg3*1e3)^2-33.425*lg3*1e3+11.03)*1e-3;
    %inductance and coupling coefficients
    result = OCI_Lmat(wc1,wc2,wLr,wLo,lc,lg1,lg2,lg3,h1,fs,hw,Npcb,lww,lwc);
    Lr = result.Lr; Lo = result.Lo;
    Kraob = result.Kraob; Krarb = result.Krarb;
    Kraoa = result.Kraoa; Koaob = result.Koaob;
    %calculate inductor current and voltages
    result_cir = rccBuckCVMDVM(Lr,Lo,Cr,Co,Io,Vin,D,fs,Krarb,Koaob,Kraob,Kraoa);
    index = 1:2:length(result_cir.time);
    time = result_cir.time(index);
    iLra = result_cir.iLra(index);
    iLoa = result_cir.iLoa(index);
    vds1a = result_cir.vds1a(index);
    vswa = result_cir.vswa(index);
    vds1b = result_cir.vds1b(index);
    vswb = result_cir.vswb(index);
    Vo = result_cir.Vo;
    vLra = Vin - vds1a - vswa;
    vLrb = Vin - vds1b - vswb;
    vLoa = vswa - Vo;
    vLob = vswb - Vo;
    Ln = Lo/Lr;
    %peak to peak current
    lppLr = max(iLra)-min(iLra);
    lppLo = max(iLoa)-min(iLoa);
    IdmLr = Vo/2/fs*[(1-Koaob)*Ln+(Kraob-Kraoa)*sqrt(Ln);...
        (1-Krarb)+(Kraob-Kraoa)*sqrt(Ln)]/...
        ((1-Krarb)*(1-Koaob)-(Kraoa-Kraob)^2)/Ln;
    lcmLr = (1-D)*Vo/2/fs*[(1+Koaob)*Ln+(Kraoa+Kraob)*sqrt(Ln);...
        (1+Krarb)+(Kraoa+Kraob)*sqrt(Ln)]/...
        (-1+Krarb)*(1+Koaob)+(Kraoa+Kraob)^2)/Ln;
    %required Lr for ZVS
    Lr_zvs = sum([abs(IdmLr);abs(lcmLr)])/(Io-Io*Vo/Vin+Icoss*2);
    lc_new = Lr_zvs/Lr*lc; %new lc for ZVS

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if(lc_new<lc_max) %if lc_new<lc_max, this is a valid point, and i=i+1
    i=i+1;
    Lomni = OCI_Lmat(wc1,wc2,wLr,wLo,lc_new,lg1,lg2,lg3,h1,fs,hw,Npcb,lww,lwc);
    Loss = OCI_CoreLoss(time,vLra,vLrb,Cm,alpha,beta,wc1,...
    wc2,wLr,wLo,lc_new,lg1,lg2,lg3,h1,fs,hw,Npcb,lww,lwc);
result = rccBuckCVMDVM(Lomni.Lr,Lomni.Lo,Cr,Co,Jo,Vin,D,fs,...
%dc current
    ILrdc = result.Vo/Vin*Io/2;
    ILodc = Io/2;
%dc winding loss
    PLrdc = ILrdc^2*RdcLr*lc_new/10e-3;
    PLodc = ILodc^2*RdcLo*lc_new/10e-3;
%ac winding loss
    PLaac = (result.ILrRMS^2-ILrdc^2)*RacLr*lc_new/10e-3;
    PLoc = (result.ILoRMS^2-ILodc^2)*RacLo*lc_new/10e-3;
%total winding loss of two phases
    Pwt = 2*(PLrac+PLoac+PLrdc+PLodc);
    Hdc = OCI_Hdc(Io,Iin,mur,wc1,wc2,wLr,wLo,lc_new,lg1,lg2,lg3,h1);
%dc effect on core loss
    Kdc = 0.00053*Hdc^2+0.0098*Hdc+1;
%total volume
    Vol = (wc1+wc2/2+wLr+wLo+2*lwc+lww)*2*(2*wc1+h1)*lc_new;
%output
    Volume(i,1) = Vol*1e9;
    Totalloss(i,1) = Loss.CL*Kdc+Pwt;
    dataout(i,1) = lg1*1e3;
    dataout(i,2) = lg2*1e3;
    dataout(i,3) = lg3*1e3;
    dataout(i,4) = wc1*1e3;
    dataout(i,5) = wc2*1e3;
    dataout(i,6) = lc_new*1e3;
    dataout(i,7) = Lomni.Kraob;
    dataout(i,8) = Lomni.Krarb;
    dataout(i,9) = Hdc;
    dataout(i,10) = Vol*1e9;
    dataout(i,11) = Loss.CL*Kdc;
    dataout(i,12) = Pwt;
    dataout(i,13) = Loss.CL*Kdc+Pwt;
end
waitbar(j/N);
plot(Volume, Totalloss, '*'); hold on; % Plot all points
grid on;
xlabel('Volume (mm^3)');
ylabel('Loss (W)');
ylim([0.3, 0.7]);
xlim([400, 1000]);
[membership, member_value] = find_pareto_front([Volume, Totalloss]);
plot(member_value(:,1), member_value(:,2), 'r'); % Plot pareto front
close(h)
toc;

%------------------------------------------------------------------------------------------------------------------------
% This function identifies the pareto frontier of a set of points (this function consider smaller values are more desirable)
%------------------------------------------------------------------------------------------------------------------------
% Input: input, a matrix, each row corresponds to a point, each column correspond to a dimension
%------------------------------------------------------------------------------------------------------------------------
% Outputs:
% (1) membership: a logical array, have same number of rows as input matrix, 1 indicate the corresponding point in input matrix is a member of pareto frontier, 0 otherwise
% (2) member_value: matrix, contain point(s) on the pareto frontier.
%------------------------------------------------------------------------------------------------------------------------
% https://www.mathworks.com/matlabcentral/fileexchange/45885-find-pareto-frontier
function [membership, member_value] = find_pareto_front(input)
out = [];
data = unique(input, 'rows');
for i = 1:size(data,1)
    c_data = repmat(data(i,:), size(data,1), 1);
t_data = data;
t_data(i,:) = Inf(1, size(data,2));
smaller_idx = c_data >= t_data;
idx = sum(smaller_idx, 2) == size(data, 2);
if ~nnz(idx)
    out(end+1,:) = data(i,:);
end
end
membership = ismember(input, out, 'rows');
member_value = out;
end
Appendix D Matlab Code for Small-Signal Models of RccBuck Converter

Transfer functions $G_{vd}$, $G_{v_{invo}}$, $Z_o$, and Compensator of rccBuck converter for Chapter 5.

```matlab
Vin = 12; %Input voltage
Io = 15; %Output current
D = 0.37*2; %Duty ratio
Vo = D/(2+D)*Vin; %Output Voltage
fs = 2e6; %Switching frequency
Lr = 160e-9; %Resonant inductance
Lo = 95e-9; %Output inductance
Cr = 264e-9; %Resonant capacitance
RL = Vo/Io; %Load resistor
Co = 100e-6; %Output capacitance
Rdsh = 8e-3; %Rds(on) of high-side FET
Rdsl = 1.5e-3; %Rds(on) of low-side FET
RLr = 1e-3; %DCR of Lr
RLo = 1e-3; %DCR of Lo
RCr = 0.28e-3; %ESR of Cr, 8 in parallel: 2.28/8
RCo = 0.29e-3; %ESR of Co, 10 in parallel: 2.85/10
Dpri = 1-D;
Re = D/2*Rdsh+Dpri*Rdsl;
syms s;
%Control to output transfer function
Gvd = 2*Vin/(2+D)/Lo/Co* ...
(s^2-D*Io/Vin/(Cr^4)*s^2+(2+D)/(Cr^4)/Lr)* ...
(1+RCo*Co*s)*(1+RCr*(Cr^4)/4*s)/ ...
(1+RLo+Re+2*RCo)/Lo)*s+2/Lo/Co)/ ... 
Gvovin = D/Lo/Co* ...
2*(2+D)/(Cr^4)/Lr* ...
(1+RCo*Co*s)*(1+RCr*(Cr^4)/4*s)/ ...
(1+RLo+Re+2*RCo)/Lo)*s+2/Lo/Co)/ ...
%Output impedance
Zout = RCo*(s^2+(1/RCo/Co+(RLo+Re+2*RCo)/Lo)*s+2/Lo/Co)/ ...
(s^2+(RLo+(D/2*Rdsh+Dpri*Rdsl)/2+2*RCo)/Lo)*s+2/Lo/Co);
```
for i=1:length(f)
    s = 2*pi*1j*f(i);
    Gvds = eval(Gvd);
    Gvdamp(i) = 20*log10(abs(Gvds));
    Gvdphase(i) = angle(Gvds)*180/pi;
    Goins = eval(Gvovin);
    Goinamp(i) = 20*log10(abs(Goins));
    Goinphase(i) = angle(Goins)*180/pi;
    Zs = eval(Zout);
    Zsamp(i) = 20*log10(abs(Zs));
    Zsphase(i) = angle(Zs)*180/pi;
end

% Plot transfer functions
figure(1);
subplot(3,2,1); semilogx(f,Gvdamp); grid on; axis tight;
title('Gvd');
subplot(3,2,2); semilogx(f,Gvdphase); grid on; axis tight;
subplot(3,2,3); semilogx(f,Goinamp); grid on; axis tight;
title('Gvinvo');
subplot(3,2,4); semilogx(f,Goinphase); grid on; axis tight;
subplot(3,2,5); semilogx(f,Zsamp); grid on; axis tight;
title('Zout');
subplot(3,2,6); semilogx(f,Zsphase); grid on; axis tight;

% Compensator design
fc = 100e3; % Crossover frequency
s=2*pi*fc*1i;
Gvdmagfc=abs(eval(Gvd));
omegac=fc*2*pi;
%Type-III compensator + phase-lead compensation
fp1 = 0.7e6; % Slightly lower than RHP zero
fp2 = 1.3e6; % Slightly higher than RHP zero
fz1 = 80e3; % Close to Lo/Co double pole
fz2 = 90e3; % Close to Lo/Co double pole
fz3 = 80e3; % Lower than Lo/Co double pole
fz4 = 120e3; % Higher than Lo/Co double pole
fp4 = 2*fp4;
omegap1=fp1*2*pi;
omegap2=fp2*2*pi;
omegaz1=fz1*2*pi;
omegaz2=fz2*2*pi;
omegaz3=fz3*2*pi;
omegaz4=fz4*2*pi;
omegap4=fp4*2*pi;
sfc=1i*omegac;
Ro1=10e3; Ro2=6.8e3;  \text{%Voltage divider}  
Gpwm = 10/16.8/2/3.3*2; \text{%Voltage divider + PWM gain}  
Co1 = 1/omega(3)/Ro1;
fp3 = (Ro1+Ro2)/Ro2*fz3;
omega(3)=fp3*2*pi;
R5 = 2e3;
R4 = 10; \%R4<<R5
C4 = 1/omega4/(R5*2+R4);

\text{%required dc gain of compensator}
omega(1)=1/Gvdmagfc/Gpwm*abs((1+sfc/omega(1))*(1+sfc/omega(2))*(1+sfc/omega(3))
/((1+sfc/omega(1))*(1+sfc/omega(2))*(1+sfc/omega(3))*(1+sfc/omega(4))*sfc);
syms s;
Gcom=omega(1)/s*(1+s/omega(1))*(1+s/omega(2))*(1+s/omega(3))*(1+s/omega(4));
Tloop=(Gvd*Gcom*Gpwm);

\text{%Calculation of cap and R of type-III compensator}
syms R2 R3 C1 C2 C3;
R1=1.2e3;
F1=omega(1)-1/R2/C1;
F2=omega(2)-1/R1+R3;
F3=omega(3)-1/R1/(C1+C3);
F4=omega(4)-1/R3/C2;
F5=omega(2)-1/R1/(C1*C3/(C1+C3));
parsol=solve(F1,F2,F3,F4,F5,R2,R3,C1,C2,C3);
C1=eval(parsol.C1);
R2=eval(parsol.R2);
C2=eval(parsol.C2);
R3=eval(parsol.R3);
C3=eval(parsol.C3);

\text{%Calculation of magnitude and phase}
fsweep=logspace(2,log10(10e6),502);
Tloopmag=zeros(1,length(fsweep));
Tloopphase=zeros(1,length(fsweep));
for i=1:length(fsweep);
    fs=fsweep(i);
s=fs*2*pi*1i;
    Tloops=eval(Tloop);
    Tloopmag(i)=20*log10(abs(Tloops));
    Tloopphase(i)=180*phase(Tloops)/pi;
    Tloopphase(i)=mod(Tloop-phase(i)+180,360)-180;
end
% Plot of loop gain

figure(2);
semilogx(fsweep,Tloopmag,'LineWidth',2); hold on; grid on;
xlabel('Frequency (Hz)');
ylabel('Amplitude (dB)');
figure(3);
semilogx(fsweep,Tloopphase,'LineWidth',2); hold on; grid on;
ylim([-180,180]);
xlabel('Frequency (Hz)');
ylabel('Phase (deg)');
Appendix E Automatic Data Acquisition System

Functionalities of automatic data acquisition system:

- Record input/output current/voltage automatically with the sampling rate of 1 Hz
- Obtain waveform data from the oscilloscope
- Adjust load current, duty ratio, and dead time of PWM signals in Matlab GUI
- Calculate real-time losses and efficiency

Commutation approaches: GPIB, serial port, and USB.

Test setup
Schematic of efficiency measurement system for a dc-dc converter

Graphical user interface (GUI) in Matlab

Measured input and output voltage, current, and losses.

Configuration of the Oscilloscope: D, phase shift, and dead time

Recorded efficiency versus load current

Efficiency data is saved in a text file.
Appendix F Directory of Raw Files

The original simulation files and experimental results in this dissertation are located at the //ADFS directories shown in Table B-1.

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