Energy Harvesting IC Design for an Electromagnetic Generator Based on the Split-Capacitor Approach

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ABSTRACT

The proposed energy harvesting system intends to harvest vibrational energy via an electromagnetic generator (EMG). The proposed circuit intends to extract maximum power from the EMG by utilizing the maximum power transfer theorem which states that maximum power is transferred to the load when the source resistance equals the load resistance. The proposed circuit is a synchronous split-capacitor boost converter operating in boundary conduction mode (BCM) to achieve impedance matching and therefore maximum power transferred to the load. The circuit topology combines the rectifier and power stage to reduce power loss of the power management integrated circuit (PMIC).

The proposed circuit is designed and fabricated in 130 nm BiCMOS technology. The circuit is validated through schematic level simulations and post-layout simulations. The results conclude the proposed circuit and control operates in a manner to achieve BCM.

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GENERAL AUDIENCE ABSTRACT

Tracking and monitoring systems and products has become more prevalent in our society. Consumers want to know when a package they ordered will arrive. Grocery stores would like to track a produce from harvest to the shelves, ensuring their produce is safe to eat. Produce should be kept around 0 °C and if it exceeds that anywhere during the supply chain, the store should be alerted.

Wireless sensor nodes (WSNs) are such devices that would be able to monitor the temperature of produce or the location of a package. These devices must be small, reliable, long-life and cost efficient. Using a battery to power WSNs is an inconvenience as the battery must be replaced often.

The proposed circuit enables a self-sufficient WSN that is compact, dependable, long-lasting and economical when deployed at large scale. The proposed circuit has been designed, fabricated and proven through simulations.

Acknowledgements

Thank you to my advisor, Dr. Dong S. Ha, for his unwavering support, leadership and laughter. Dr. Ha makes the Multifunctional Integrated Circuits and Systems (MICS) group a fun place to conduct leading research. I would like to also thank Dr. Qiang Li and Dr. Daniel Sable for being excellent committee members and assisting in my thesis work.

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I am extremely appreciative of every friend I have gained throughout my 5 years at Virginia Tech through undergraduate and graduate school. Thank you to my Maple + PB + 3 + Jordan friend group for getting me away from my work every once in a while. Also thank you to my hometown friends in Chesapeake, Virginia.

Finally, I praise God for always being there for me and never allowing me to break. I am forever grateful to my mother, Angela Haskins, father, Jarrod Dancy, brothers Jalen Dancy and Chris Jennings, my grandparents, and my girlfriend Taylor Beauprez. Also I am grateful for other members of my immediate and extended family. Thank you for your love, support and sacrifice.

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Chapter 1

Introduction

1.1 Motivation

Internet of Things (IoT) is a system of interconnected devices transferring data over a network. Such devices include, but are not limited to smartwatches, thermostats, home alarm systems, sensors and smart speakers. As some IoT devices must be portable or secluded, providing electrical power can be challenging. Batteries have a finite life and charge, so they must be replaced or recharged continuously. Energy harvesting (EH) is a viable solution to continuously provide power to a device or recharge batteries.

Energy harvesting is the technique of scavenging energy from ambient sources such as light, heat, vibration or RF radiation. These particular energies can come from environmental conditions (the Sun, wind, waves) or may be biological (body heat, walking). The transducers used to capture the energy include electromagnetic generators (EMGs), piezoelectric, electrostatic, photovoltaic cell, thermoelectric generator and antenna.

To transfer energy from the transducer to the battery or device, a power management circuit is required for rectification, voltage conversion or impedance matching. This project's goal is to develop an EH system that effectively and efficiently transfers energy from an EMG to a battery.

1.2 Scope of the Proposed Research

Typical EH EMG applications output a low AC voltage and high current. The AC voltage must be rectified before being traveling to a DC converter. A full-bridge rectifier is not viable because of the high voltage drop across the diodes and large conduction loss. [1, 2] propose a negative voltage converter that uses MOSFETs to reduce the voltage drop to the threshold voltage of the MOSFET. Merging the rectifier and converter has been proposed previously to reduce power loss and number of components in the power management circuit [3-5].

Maximum power transfer theorem states that maximum power is transferred to the load when the load impedance matches the source impedance. For EH it is imperative that maximum power is transferred to load as the input power is small. A buck-boost converter operating in discontinuous conduction mode (DCM) is commonly used because the input impedance is easily controlled [6]. One drawback for a buck-boost converter operating in DCM is that the input current flows through the switching MOSFET causing high conduction loss.

This project intends to extract maximum power from an EMG using synchronous split-capacitor boost converter operating in boundary conduction mode (BCM) to achieve rectification, voltage step-up and impedance matching.

1.3 Proposed Approach and Technical Contributions

A synchronous split-capacitor boost converter operating in BCM is designed, tested and fabricated. The major objective of this EH circuit is to extract maximum power from the EMG while dissipating minimal power by utilizing a single-stage topology and BCM operation.

Typically for BCM operation a zero current detector (ZCD) is used. A ZCD sensing when the inductor current is zero. This can be achieved via four methods: shunt resistor sensing, current sensor, transformer sensing and inductor DCR sensing. As the input power is low for energy harvesting applications, inductor DCR sensing is selected in the proposed design. Passive components interfering with the circuit are not required, therefore less power is loss during sensing.

The major contribution of this work is the control strategy to achieve a synchronous split-capacitor boost converter operating in BCM. The proposed circuit avoids using large resistor banks to control the pulse width for the switching MOSFET, but instead utilizes clocked components to reduce power consumption with components are not in use.

The proposed EH circuit was designed in Cadence and fabricated in GlobablFoundries BiCMOS 0.13 μm technology. Schematic level simulations and post-layout simulations provide evidence for the functionality of the integrated circuit.

1.4 Organization of this Thesis

The organization of this thesis is as follows. Chapter 2 provides background necessary to understand the proposed design and the state of the energy harvesting single-stage boost converters. This chapter discusses the basics of EMGs and previous design's successes and challenges. A table summarizes the input impedance of the boost, buck and buck-boost converter operating in BCM, DCM, and continuous conduction mode (CCM). Chapter 3 discusses the proposed design by first detailing the design specifications. The circuit operation is stepped through to thoroughly explain current paths and switching cycles. Waveforms are presented to visualize the functionality of the synchronous split-capacitor boost converter. Each sub-circuit is explained to detail how it contributes to this mission of achieving BCM. Chapter 4 presents schematic and post-layout simulations of the converter from the Cadence design environment. Finally, Chapter 5 draws conclusions, provides lessons learned and ideas on what can be done to improve circuit performance.

Chapter 2

Preliminaries

This chapter provides background information on EMGs and previous research necessary to understand the proposed single-stage boost converter and the contributions of this thesis paper. Section 2.1 details the basics of EMGs and why conventional AC-DC boost converters are not used. Section 2.2 explains the achievements and shortcomings of a previous EMG EH circuit. Section 2.3 explains why BCM operation is used for impedance matching. Lastly, Section 2.5 summarizes the chapter.

2.1 Design Requirements

2.1.1 Electromagnetic Generator Characteristics

Electromagnetic generators have been studied extensively in [2-5, 7, 8]. An EMG can be excited via vibration, flow or rotation. The model for a rotational EMG is given in Figure 2-1. A AC voltage source is in series with and inductor, L_s, and resistor, R_s. The inductance and resistance come from the internal coil windings on an EMG. The inductance of an EMG is typically ignored if its reactance $|\omega L_s|$ is much smaller than R_s [5]. Therefore, the inductance will be ignored as the EMG source frequency is low. This assumption eases the impedance matching process as the imaginary component is ignored. Now, for maximum power transfer, the source impedance, R_s,

must be equal to the load resistance, R_{in}, where the input impedance to the converter is the load of the EMG source.

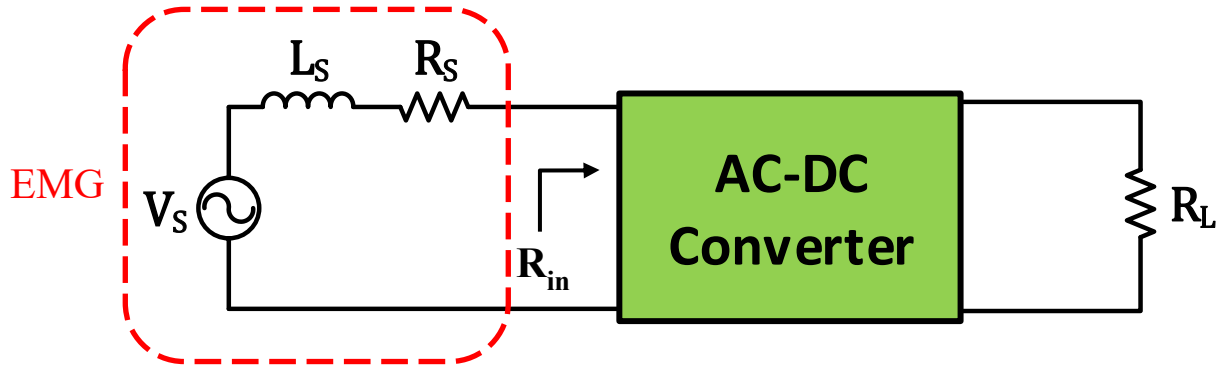


Figure 2-1: Rotational EMG model

2.1.2 Conventional AC-DC Boost Converter

A conventional AC-DC boost converter is shown in Figure 2-2. The full bridge rectifier, diodes D1—D4, serve to rectify the input voltage, Vin, from AC to DC. D5 is used to prevent the load current from flowing backwards into the input. For positive half cycle and the negative half cycle, the input current must flow through two diodes necessary for rectification. D1 and D4 for the positive half and D2 and D3 for the negative half cycle. EMGs produce a low amplitude voltage while a diode normally has a voltage drop around 0.7 V; with each having 0.7 V voltage drop, 1.4 V is lost during the positive half cycle and negative half cycle. This is okay for large power applications such as [9], because 1.4V is okay to loss when the input voltage is large. A large voltage drop leads to a large power loss and insufficient power to operate the circuit. Other methods must be used to alleviate the voltage drop during rectification.

Another disadvantage for the conventional AC-DC boost converter is large power dissipation as the input current is higher than the output current. Large power dissipation loss to the bridge rectifier is not advantageous towards energy harvesting.

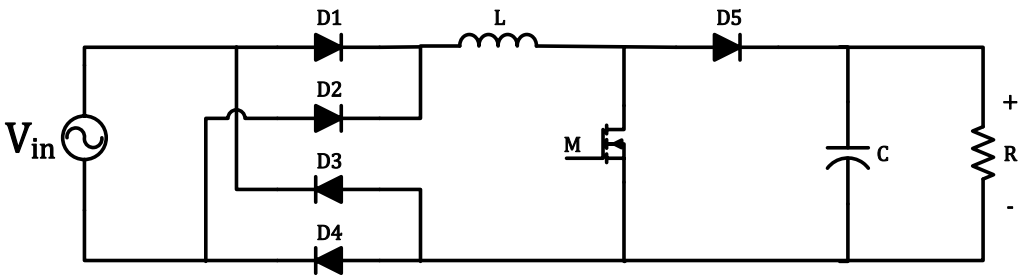


Figure 2-2: Conventional AC-DC boost converter

2.2 Previous Converter Design Approaches for EMG

2.2.1 Xu's EH BCM Boost Converter

Xu proposed split-capacitor boost converter operating in boundary conduction mode [5] as seen in Figure 2-3; a similar topology is adopted for the proposed design. The circuit is composed of an AC voltage source V_s, an inductor L1, a bidirectional switch NMOS and PMOS, two diodes D1 and D2 and capacitors C_P, C_N and C_1.

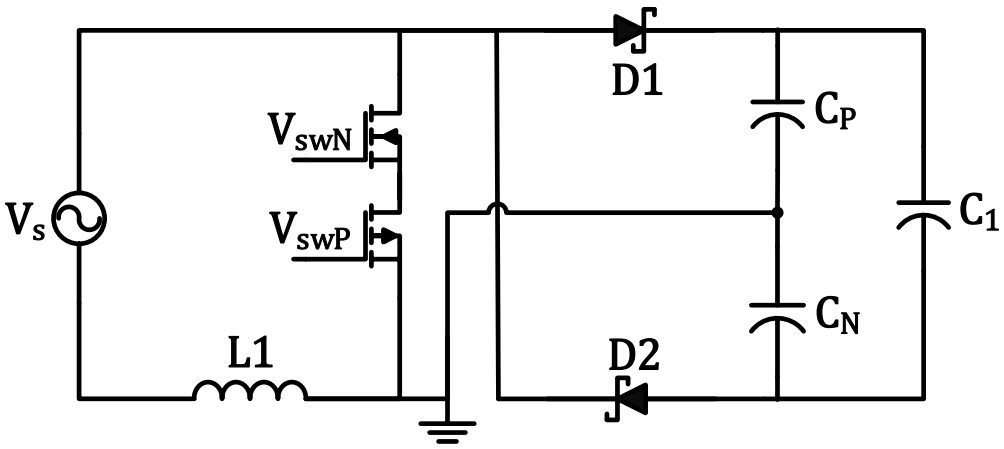


Figure 2-3: Xu's split-capacitor boost converter

During the positive half cycle of V_s, the bidirectional switch is turned on by applying a positive voltage to V_{swN} and a negative voltage to V_{swP} to charge the inductor L1. During discharge for the positive half cycle of V_s, the bidirectional switch is turned off and current is blocked via body diodes of the MOSFET pair. The discharge current flows through D1 and charges C_p returning to

the source to complete the loop. During the negative half cycle of V_s, the bidirectional switch is turned on by applying a positive voltage to V_{swN} and a negative voltage to V_{swP} to charge the inductor L1. During discharge for the negative half cycle of V_s, the bidirectional switch is turned off and current is blocked via body diodes of the MOSFET pair. The discharge current charges C_N and flows through D2 returning to the source. The capacitors C_P, C_N and C_1 use charge recycling to share energy. C_1 voltage is the sum of C_P and C_N voltages. The positive cycle charge and discharge current paths are shown in Figure 2-4 (a) and (b) respectively, while the negative charge and discharge current paths are shown in Figure 2-4 (c) and (d) respectively.

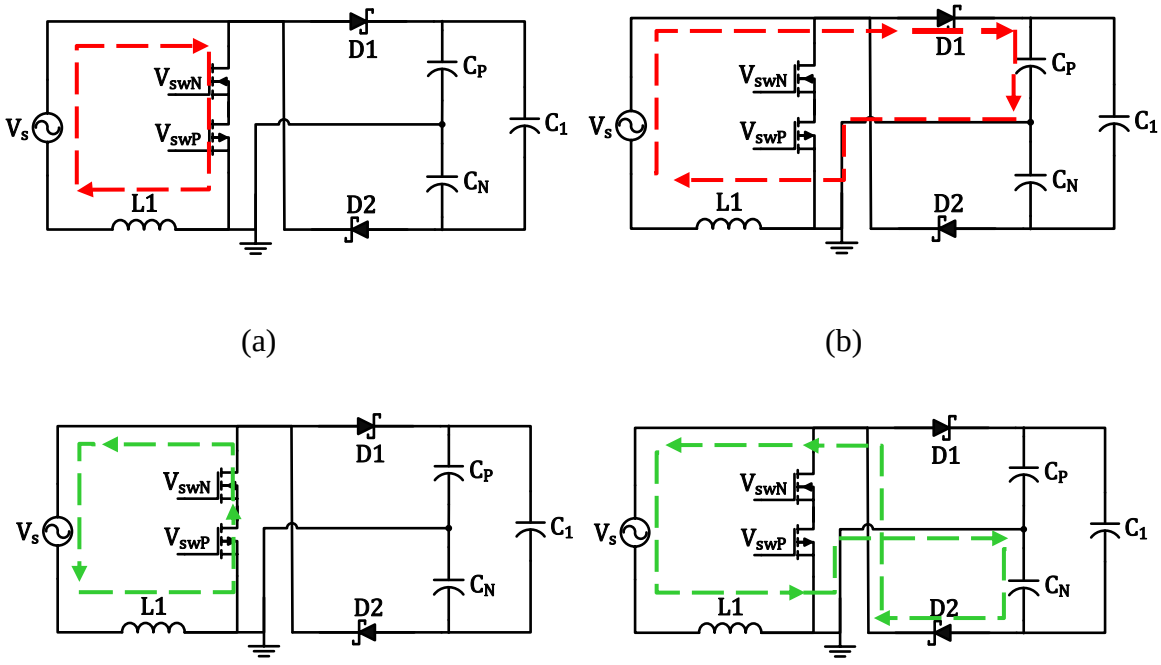


Figure 2-4: Current waveforms for positive cycle (a) charging (b) discharging and negative cycle (c) charging (d) discharging

It is claimed that the input impedance for a boost converter operating in BCM is

$$R_{in} = \frac{2L}{T_{on}} \tag{2.1}$$

BCM operation will further be discussed in Section 2.3. However, for BCM operation it is necessary for the inductor current to discharge to 0 A and them immediately began charging again. Xu detects the inductor current by sensing the inductor voltage. As the inductor voltage switches

between positive and negative, the current changes direction. This change in direction is detected by Xu's zero current detector (ZCD). The main disadvantage of sensing the inductor voltage is its small magnitude as the direct current resistance (DCR) is small. The comparator for sensing the inductor voltage is constantly operating meaning it is a power sink when voltage sensing is not needed. Other shortcomings come from the bidirectional switch and diodes D1 and D2. Using a NMOS and PMOS for the switching requires separate level shifters and drivers for each MOSFET. A PMOS also requires larger area. This increases the count of auxiliary circuits and area of the circuit. Having two MOSFETs in the conduction paths during charging increases the conduction loss. One diode is used during the positive or negative cycle which is an improvement over the conventional boost converter with bridge rectifier. However, the use of a diode still incurs a large voltage drop and should be analyzed for improvement.

2.3 Converter Operation Modes

In power electronics, two main modes of operation are typically used: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM is the operation where the inductor current has a DC offset greater than its ripple value. The inductor current charges and discharges without returning zero amps. DCM operation occurs when the inductor current does not have a DC offset. The current charges from zero and then discharges to zero, remaining at zero for a period of time before charging again. BCM, also referred to as critical conduction mode (CrM), operation is the middle ground of CCM and DCM. The inductor current discharges to zero and then immediately charges again with ideally minimal time at zero amps. BCM operation is typically used for power factor correction [10-12], but here BCM will be used for impedance matching.

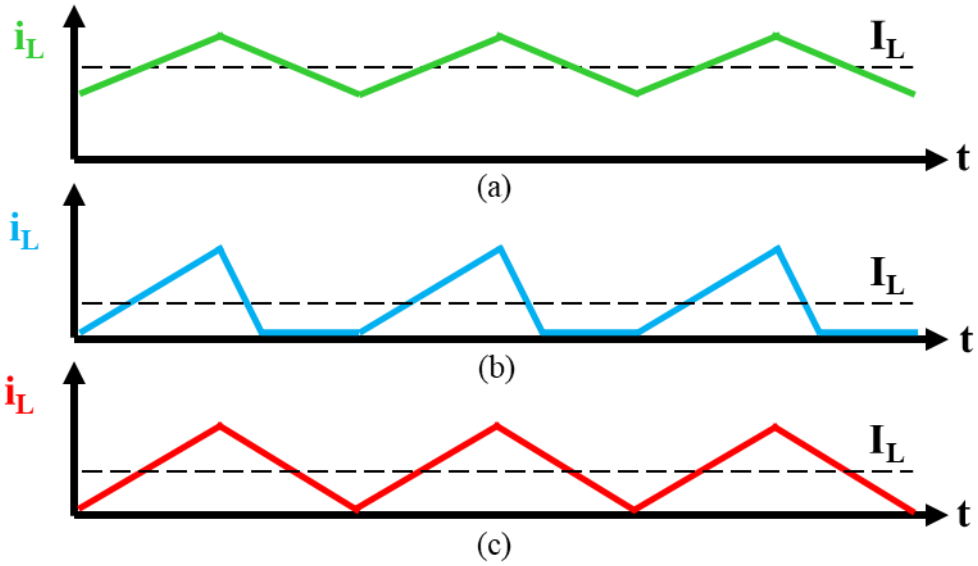
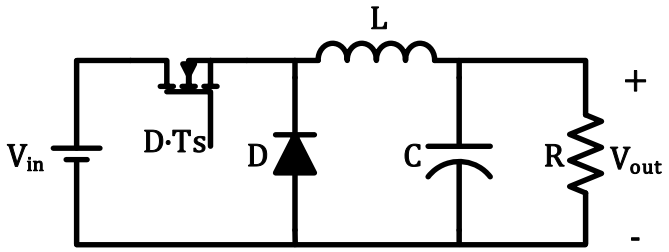


Figure 2-5: Inductor current waveforms during (a) CCM (b) DCM (c) BCM

2.4 Impedance Matching

The three primary power converters are shown in Figure 2-6 with each comprising of an input source V_{in}, switching NMOS with duty cycle D and switching period T_s, a diode D, inductor L, capacitor C, resistor R and output voltage V_{out}. The on-time of the switch is defined as T_{on}.



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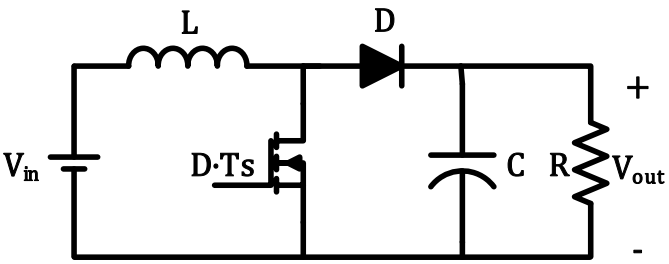

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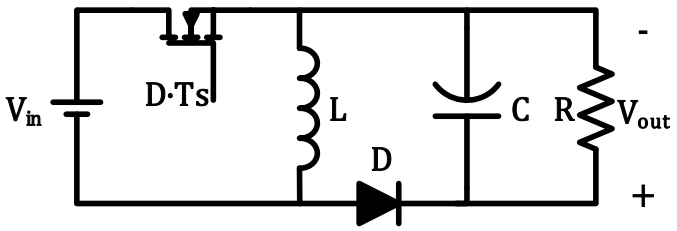


(c)

Figure 2-6: Power converters: (a) buck (b) boost (c) inverting buck-boost

Here, the derivation of a BCM boost converter will be focused on as [13] has derived the input impedance for others summarized in Table 1. For a boost converter operating in BCM with constant on-time (COT) the peak inductor current is

$$i_{\mathrm{pk}} = \frac{V_{in}}{\mathrm{L}} T_{on} \tag{2.2}$$

Since the boost converter is operating in BCM the average current is

$$I_{\mathrm{in}} = \frac{i_{pk}}{2} = \frac{V_{in}}{2\mathrm{L}} T_{on} \tag{2.3}$$

Therefore, the input impedance of the boost converter operating in BCM is

$$R_{\mathrm{in}} = \frac{V_{in}}{I_{\mathrm{in}}} = \frac{2L}{T_{on}} \tag{2.4}$$

Table 1: Input impedance equations for buck, boost and buck-boost converter during CCM, BCM and DCM

Operation	Buck	Boost	Buck-Boost
CCM	$R_{in} = \frac{R_L}{D^2}$	$R_{in} = R_L(1-D)^2$	$R_{in} = \frac{R_L(1-D)^2}{D^2}$
BCM	$R_{in} = \frac{R_L}{D} + \frac{2L}{D^2 T_s}$	$R_{in} = \frac{2L}{T_{on}}$	$R_{in} = \frac{2L}{D^2 T_s}$
DCM	$R_{in} = \frac{2L}{(1-M)D_1^2 T_s}$	$R_{in} = \frac{2L}{(D_1 + D_2)D_1 T_s}$ $R_{in} = \frac{2L}{{D_1}^2 T_s}(1 - \frac{V_{in}}{V_{out}})$	$R_{in} = \frac{2L}{D_1^2 T_s}$

$$where,\ M = \frac{2}{1 + \sqrt{1 + \frac{8L}{D_1^2 R_L T_s}}}$$

For the purposes of impedance matching an EMG with its load of a converter, little to none variability should occur in the load impedance of the converter, input voltage and output voltage. Typically, a converter only has control over its output voltage and the load impedance and input voltage will not always be constant. From Table 1, a buck converter is not typically used for impedance matching because the input impedance to the buck converter relies on R_L in CCM, BCM and DCM. A boost converter operating in DCM is feasible if the output voltage is much greater than the input voltage to reduce the effect of those two variables interacting to shift the input impedance. A buck-boost converter operating in DCM is commonly used in energy harvesting applications because of its input impedance independence from other variables. The duty cycle, switching frequency and inductor size can also be easily controlled by the designer. In the proposed design, a boost converter operating in BCM is selected for its simplicity and reduced input conduction loss in comparison to a buck-boost converter operating in DCM. A boost

converter operating in BCM only has to control one variable, T_{on}, circuit-wise in comparison to two for a buck-boost DCM converter—D_1 and T_s.

2.5 Chapter Summary

The EMG characteristics were introduced in this chapter outlining its design challenge of low input voltage. A conventional full-bridge boost converter was analyzed to demonstrate with a more sophisticated circuit is necessary. Xu provided a solution by utilizing a split-capacitor boost converter operating in BCM. Conduction loss through MOSFETs and diodes are the major drawbacks of the design. The differences between CCM, DCM, and BCM circuit operations was examined. Lastly, Table 1 summarized the major three converter input impedances in the three operation modes.

Chapter 3

Proposed Energy Harvesting Circuit

The proposed energy harvesting circuit for EMG should satisfy several requirements based on the input characteristics. First, the circuit should rectify low amplitude AC voltage to a higher amplitude DC voltage. This is accomplished by using a single-stage boost converter. Second, the circuit should be able to emulate the given EMG source resistance for maximum power transfer. This achieved through BCM operation. Lastly, the circuit should operate as a synchronous rectifier to reduce power loss. This is achieved by adoption of high-side MOSFETs rather than diodes.

This chapter describes in detail the proposed energy harvesting circuit to accomplish the above requirements. Section 3.1 outlines the specifications for energy harvesting circuit. Section 3.2 further details the proposed impedance matching methodology. Section 3.3 details the building blocks and circuit operation, while Section 3.4 summarizes the chapter.

3.1 Specification of the Proposed Converter

The target specifications of the proposed circuit is shown in Table 2. The intended EMG has an output voltage of 1.5 V_p operating at 700 Hz and an internal resistance of 1 Ω. The inductance is ignored as the internal resistance is much greater than the reactance. The output voltage is unregulated as the goal of this circuit to prove BCM operation can induce impedance matching for a boost converter.

Table 2: Target Specifications for Proposed Energy Harvesting Circuit

Specification	**Requirement**
Input Voltage Amplitude	1.5 V_p
Input Frequency	700 Hz
Input Resistance	1 Ω
Output Voltage	Unregulated

3.2 Proposed Impedance Matching Method

For the boost converter, BCM operation is chosen rather than CCM or DCM because in CCM the converter impedance is dependent upon the load resistor and for DCM the converter impedance is dependent upon the input and output voltages. For an energy harvesting circuit to operate effectively, the converter impedance should not be dependent upon the load resistor or input and output voltages. The proposed energy harvesting circuit operates in BCM to achieve impedance matching as discussed in Section 2.3. As the input resistance of the EMG source is equal to 1 Ω,

$$R_{\text{in}} = \frac{2L}{T_{on}} = 1\Omega \tag{3.1}$$

The inductance value is initially set and then T_{on} is decided.

3.3 Implementation of the Proposed Method

The proposed energy harvesting circuit is shown in Figure 3-1. The circuit consists of the input voltage $V_{in,}$ source resistance R_s, inductor L, bidirectional switch M1—M3, PMOS M4, NMOS M5 and capacitors C1—C3. The voltage V_i is the input voltage to the converter, V_{sw} is the bidirectional switch voltage while V_{out1} and V_{out2} are the positive and negative output voltages respectively.

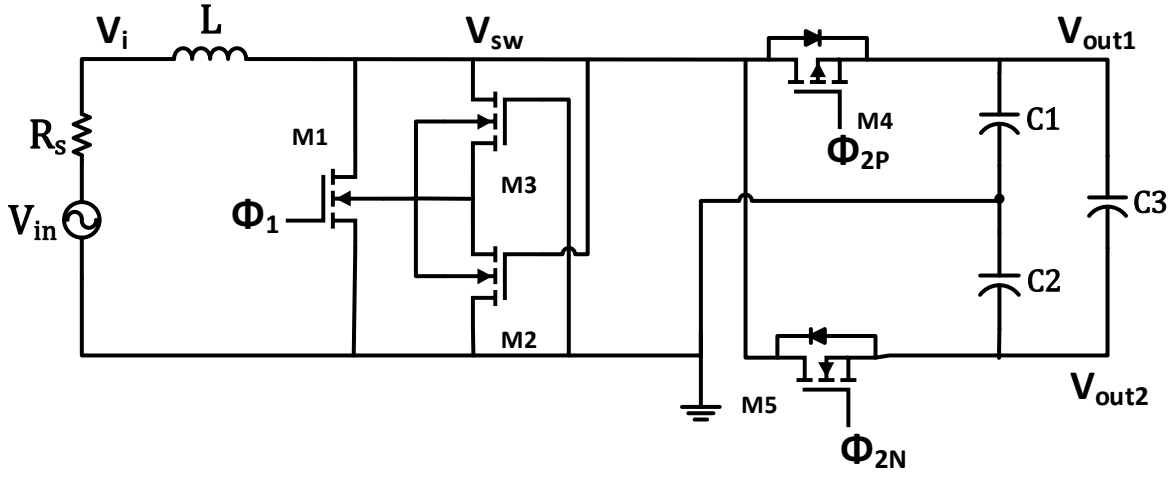
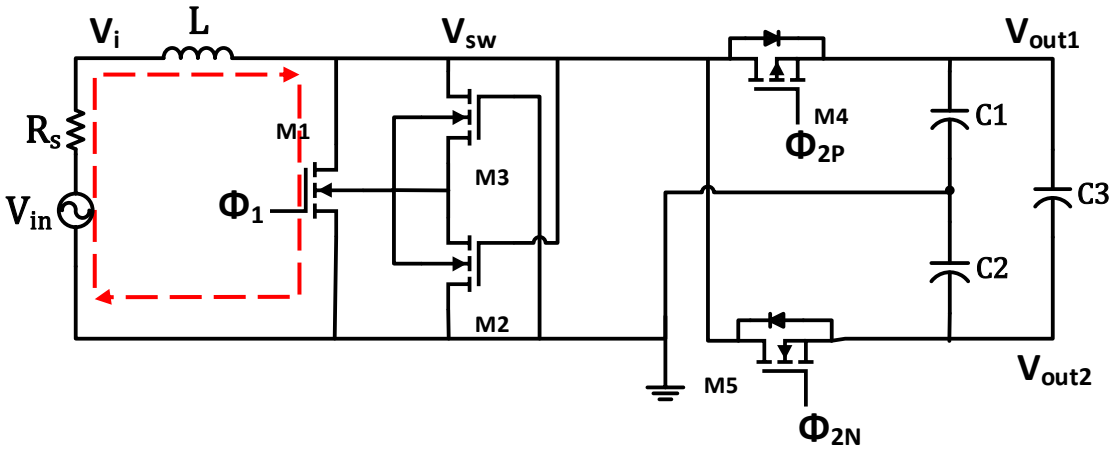


Figure 3-1: Proposed energy harvesting boost converter

The charging pattern is similar to the pattern shown in Figure 2-4, but once again repeated in Figure 3-2. When the inductor current or input current i_{in} is positive, M1 and M4 switch. When the inductor current is negative, M1 and M5 switch. In this way, M1 acts as bidirectional switch with a fixed on-time. The off-time varies making the circuit pulse frequency modulation.

During the positive half cycle of V_{in}, the bidirectional switch is turned on by applying a positive voltage to Φ_1 to charge the inductor L. During discharge for the positive half cycle of V_{in}, the bidirectional switch is turned off. The discharge current flows through PMOS M4 by applying a negative voltage to Φ_{2P} and charges C1 returning to the source to complete the loop. During the negative half cycle of V_{in}, the bidirectional switch is turned on by applying a positive voltage to Φ_1 to charge the inductor L. During discharge for the negative half cycle of V_{in}, the bidirectional switch is turned off. The discharge current charges C2 and flows through NMOS M5 by applying a positive voltage to Φ_{2P} and returning to the inductor and source. The capacitors C1, C2 and C3 use charge recycling to share energy. C3 voltage is the sum of C1 and C2 voltages. The positive cycle charge and discharge current paths are shown in Figure 3-2 (a) and (b) respectively, while the negative charge and discharge current paths are shown in Figure 3-2 (c) and (d) respectively.



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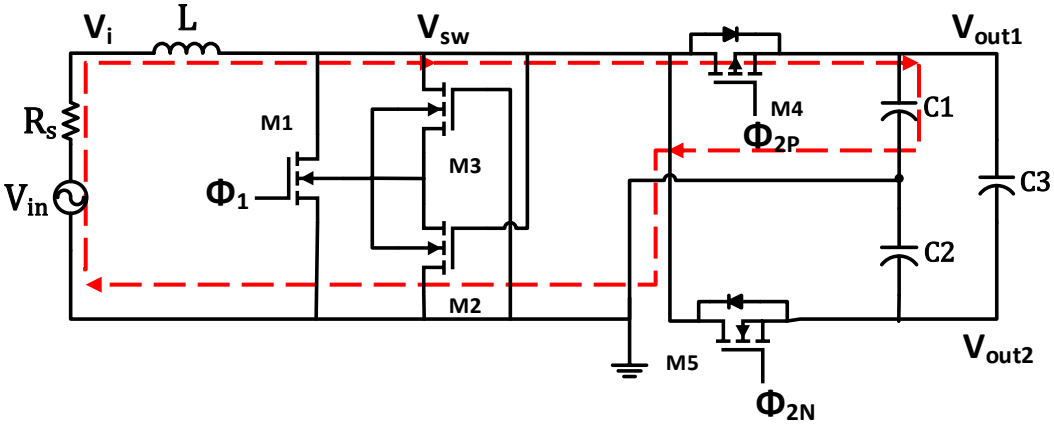

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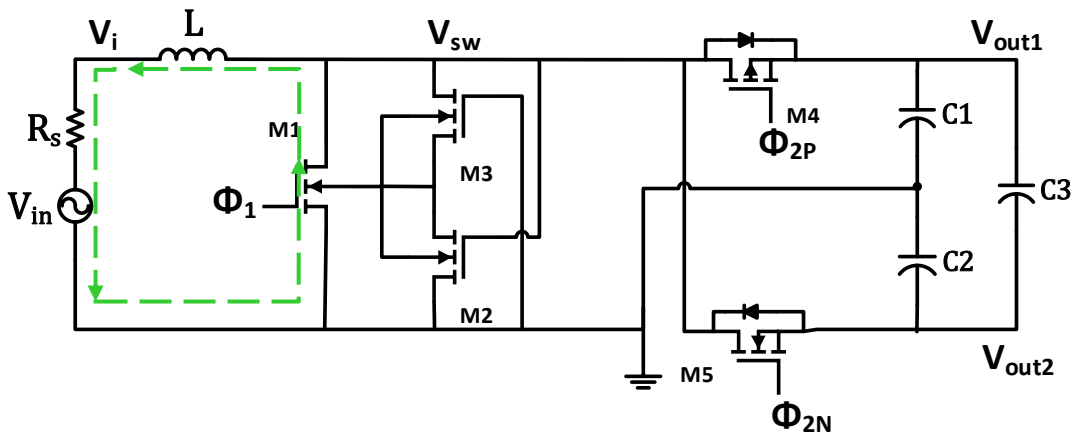

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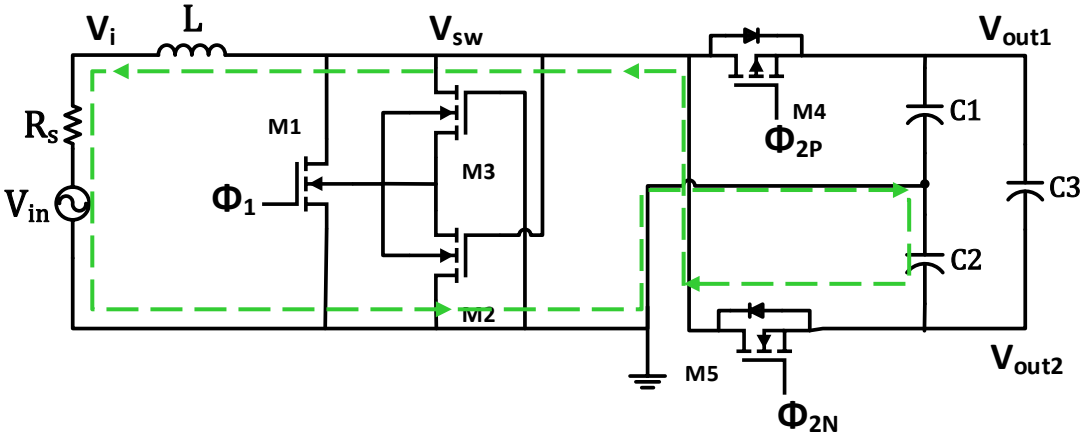

(d)

Figure 3-2: Proposed circuit current waveforms for positive cycle (a) charging (b) discharging and negative cycle (c) charging (d) discharging

The ZCD is used to determine when the converter must switch between charging and discharging. The following sections will describe building blocks of the converter and control system.

3.3.1 Bidirectional Switch

A bidirectional switch is used for the low-side. Similar combinations and uses for the bidirectional switch shown in Figure 3-3 are used in [14-19]. The bidirectional switch consists of three NMOS transistors and during the proposed circuit's operation, the bulk of M1 always connects to the lower potential so that a body diode can be formed in either direction. When V1 is high, M2 will turn on connecting the bulk of M1 to the lower potential V2. When M1 turns on

(charge), current will flow from V1 to V2 through M1. A body diode is formed with the anode at V2 and cathode at V1 across M1. This body diode will block current from flowing through M1 when M1 is turned off (discharge). The opposite is true when V2 is more positive than V1. M2 and M3 are small in size as no current flows through them; their only purpose is bulk regulation.

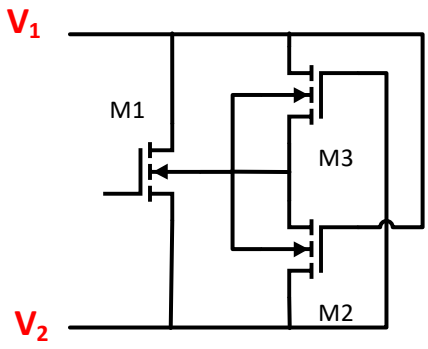

Figure 3-3: Bidirectional switch

3.3.2 Dynamic Comparator

The dynamic comparator is used as the main sensor enabling BCM operation. A dynamic or clocked comparator is adopted in the proposed circuit. A comparison of different dynamic comparators has been done by [20, 21] and designs discussed there are adopted. The dynamic comparator shown in Figure 3-4 consists of a differential amplifier and latch circuit. Dynamic comparators are typically used for high-speed analog-to-digital converters [22-24], but in this application a dynamic comparator is used for its low-power consumption. There is zero static power dissipation as the comparator is only active during a clock pulse. During a clock pulse, if the negative input VinN is greater than the positive input VinP then Vout2 will be high and Vout1 will be low. Similar effect occurs when VinP is greater than VinN.

When the CLK is low, or during the reset phase, M19 is turned off while M11 and M14 are on. Nodes f_p and f_n are pulled to VDD through transistors M11 and M14, thus M12 and M13 are turned off. With nodes f_p and f_n pulled high, M7 and M10 are turned on pulling Vout1 and Vout2 to VSS. During this phase, tail current sources M1 and M2 are also turned off restricting current flow to either output.

When the CLK is high, or during the decision-making phase, M19 is on while M11 and M14 are off. Transitioning from CLK low to high, f_p and f_n are still high during the beginning of the decision making phase. Analyzing when VinP is greater than VinN, f_n begins to fall at faster

than f_p because more current flows through M16. With f_n falling, M12 turns on and maintains f_p at VDD. With f_p high, the output Vout1 must be VSS as explained during the reset phase. With f_n now low, M2 turns on allowing current to flow through M5 and M9. Thinking of M5 and M9 as an inverter where the output is Vout1 and the input is Vout2, Vout2 must be VDD as Vout1 is VSS. A similar analysis can be performed for when VinN is greater than VinP.

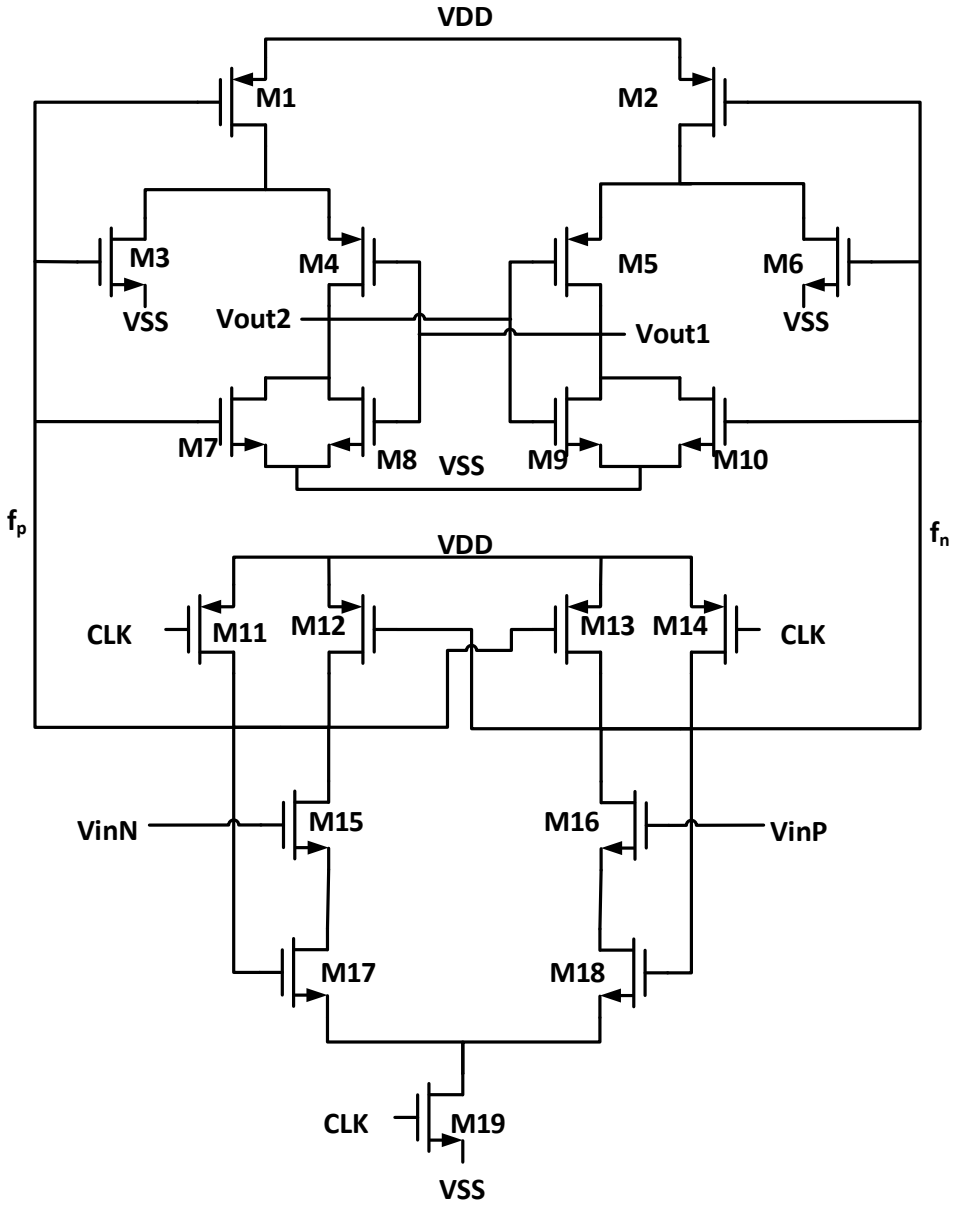

Figure 3-4: Dynamic comparator

3.3.3 Mono-stable Multi-vibrator

To generate controlled pulse-widths for the switching MOSFETs, a mono-stable multi-vibrator (MS-MV) is used as shown in Figure 3-5. The circuit consists of a NOR gate, capacitor C, resistor R, NMOS M1 and inverter. The circuit takes in a short input pulse and outputs a fixed pulse-width dependent on the RC time constant and threshold voltage of the inverter. The inverter can be replaced with a comparator to make the MS-MV resilient against environmental changes.

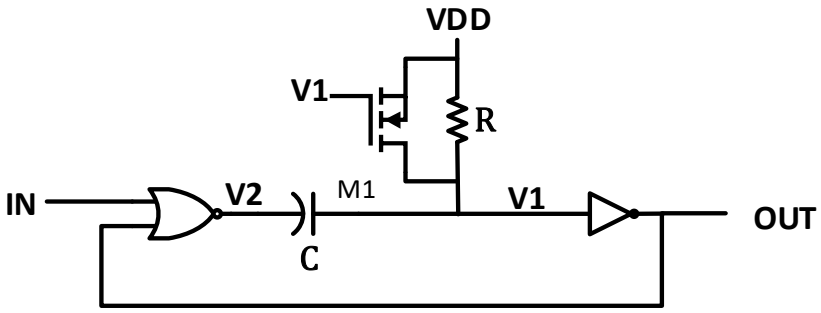

Figure 3-5: Proposed mono-stable multi-vibrator

The waveforms for the MS-MV are shown in Figure 3-6. The output goes high as soon as there is a high input. When the input is high, NOR output becomes low and the capacitor C begins charging through resistor R. As the capacitor continues to charge, the voltage V1 increases and approaches the inverter's threshold voltage. Once the inverter's threshold voltage is reached, the output becomes low making the NOR output high. As reported by [25], the output pulse width can vary because the capacitor may not discharge back to zero every time. Therefore, the proposed design adds NMOS M1 to provide a faster discharge path when the output is low. M1 is a diode connected NMOS where the anode is connected to V1 and the cathode is connected to VDD. In this configuration, during charging of capacitor, C, the current flows through resistor, R. During discharge, the current from the capacitor will flow through the diode connected NMOS. This lowers the time constant and provides a faster discharge path. Equation (3.2) shows the dependencies for the pulse width: resister, R, capacitor, C, supply voltage VDD and inverter threshold, V_{th}. This ensures the capacitor charges from the same voltage for consecutive pulses. Other MS-MV circuits [26, 27] have been used for ZCS, but they have not included the M1 MOSFET for the discharging period.

$$t = RC \cdot \ln \frac{VDD}{VDD - V_{th}} \tag{3.2}$$

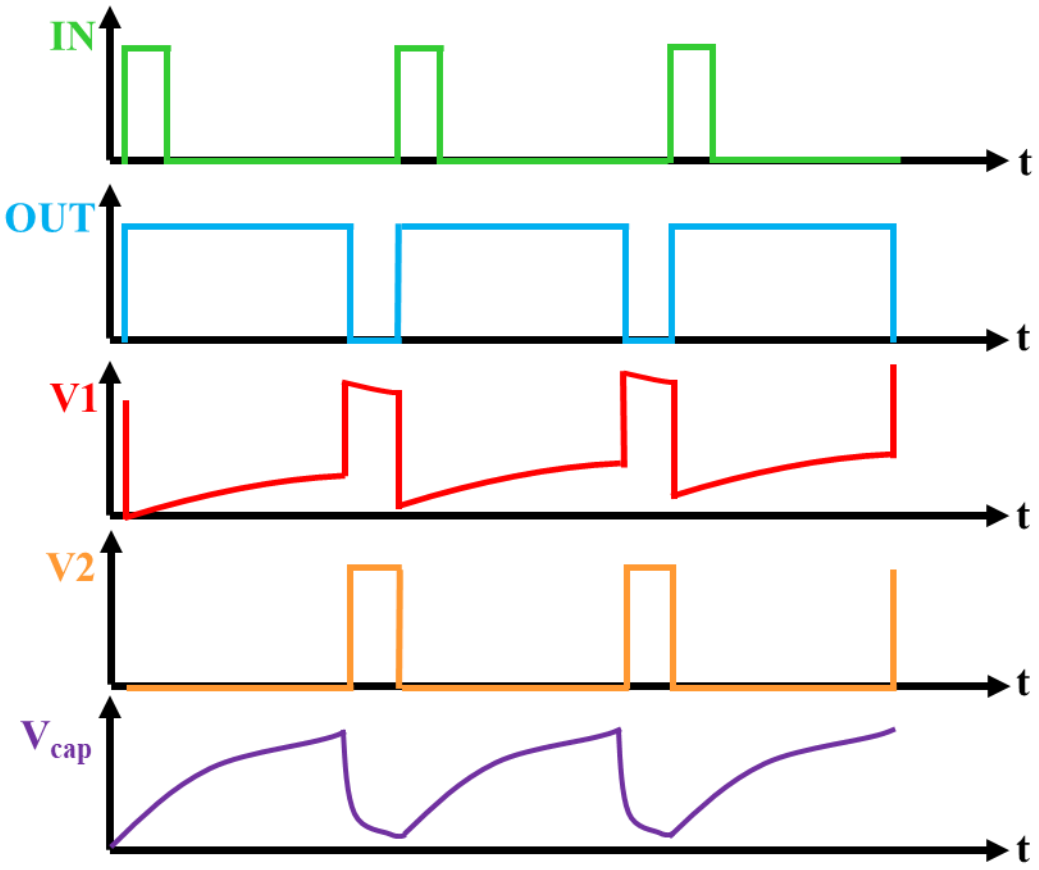

Figure 3-6: Waveforms of proposed mono-stable multi-vibrator

3.3.4 Level Shifters

Level shifters are used to transition a signal from one voltage range to another voltage range with minimum signal distortion and delay. In the proposed design, they will be used as the transition point between the digital blocks and analog block. The two level shifters used in the proposed design are shown in Figure 3-7 and Figure 3-8. The positive level shifter is used to change the VDD rail while the negative level shifter is used to change the VSS rail. The inverter inside each level shifter is powered by the first set of rails in their respective circuits. This conventional level shifter design is explained thoroughly in [28].

Analyzing the positive level shifter, M1, M2 and M7,M8 form inverters. When the input, A, is low, M1 turns on while M2 turns off. The input to M5 becomes VDD1 and the input to M6 becomes VSS, turning on M5 and off M6. With M5 on, M4 turns on and input to M7,M8 becomes VDD2. The last set of inverters M7,M8 make the output, Y, VSS. A similar analysis can be performed on the negative level shifter.

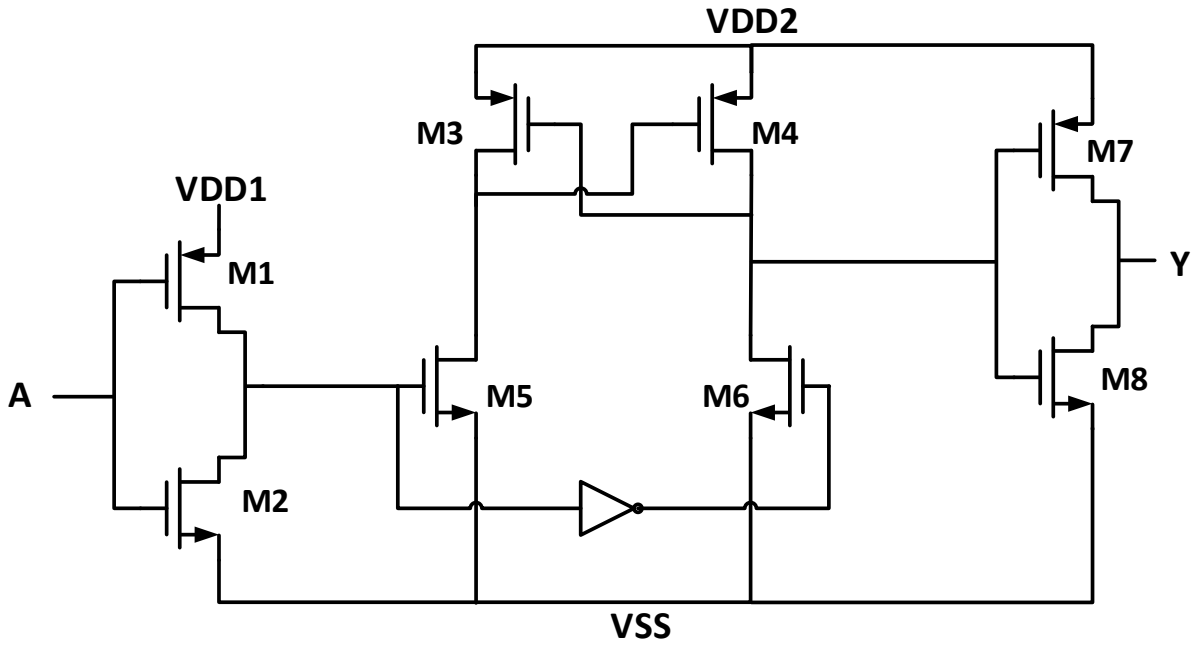

Figure 3-7: Positive level shifter

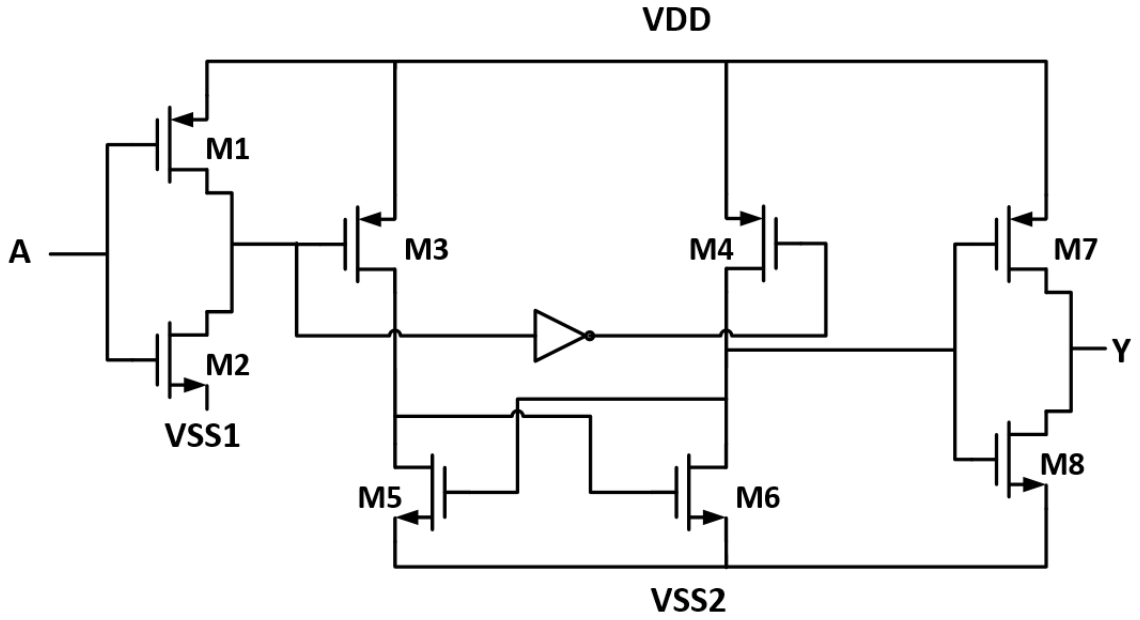

Figure 3-8: Negative level shifter

3.3.5 Falling Edge Detector

A common falling edge detector shown in Figure 3-9 is used determine when Φ_1 or Φ_2 falls. The waveforms are shown in Figure 3-10. The circuit is composed of a delay, inverter and NOR gate. NOR is high when both inputs are zero, otherwise NOR output is low so when the input to the circuit is high, the output is low. Once the input signal changes from high to low, the output signal changes from low to high as both inputs to the NOR gate are zero. The top input to the NOR gate will stay low as long as the input signal is low, but the bottom input to the NOR gate will go high because of the inverter. The high pulse width of the output signal is determined by delay gate. This falling edge detector circuit must have an odd number of inverter to function properly.

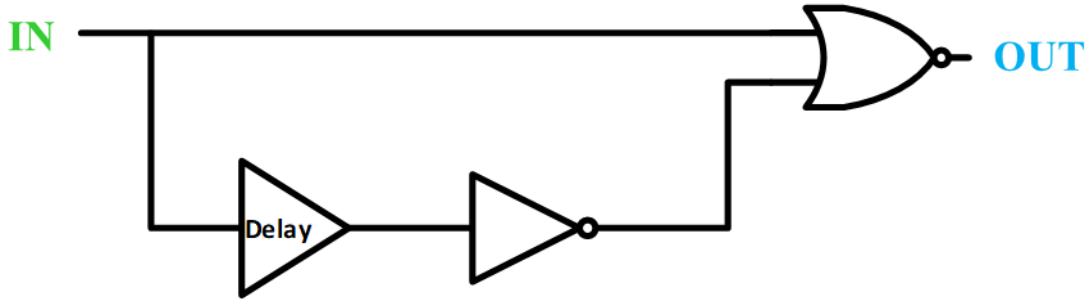

Figure 3-9: Falling edge detector circuit

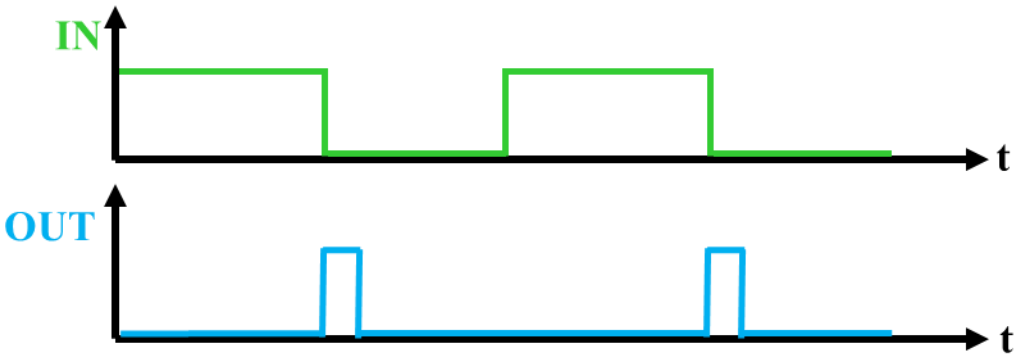

Figure 3-10: Falling edge detector waveforms

3.3.6 Ring Oscillator

A common ring oscillator design is shown in Figure 3-11 consisting of an odd number of inverters and an AND gate for enable. Noise kick-starts the ring oscillator once the circuit is enabled and powered. Once one output is high then the succeeding inverter becomes low and the cycle continues throughout the ring. The switching frequency of the ring oscillator is dependent of

the delay of one inverter and the number of inverters. As the number of inverters, n, and/or the delay of a single inverter, t_d, increases, the switching frequency, f_{sw}, decreases as shown by Equation (3.3).

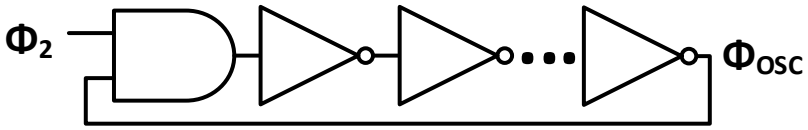

Figure 3-11: Ring oscillator circuit

$$f_{\text{sw}} = \frac{1}{2t_d n} \tag{3.3}$$

3.3.7 Start-up and Supply Currents and Voltages

External voltage sources and current source was chosen to supply the circuit as on-chip bang gap reference for on-chip voltage reference is not the main focus of the proposed circuit. For the digital control, +/- 1.2 V is used and +/- 2.5 V is used to drive the MOSFETs of the boost converter.

To start up the converter, a one-time short pulse width signal is needed to kick-start the circuit into operation.

3.3.8 Proposed Circuit Overview

To detect the point when the inductor current reaches zero, a closed-loop zero-current detection scheme is adopted [26, 27, 29-33]. The voltage across the inductor is compared with a high input impedance dynamic comparator as shown in Figure 3-12. Major waveforms for the positive cycle are shown in Figure 3-13. During Stage 1, the inductor is charging and M1 is on while M4 and M5 are turned off. Φ_1 is the gate signal for M1 while Φ_2 is the gate signal for M4 and M5. Note that the input voltage, V_i, is greater than V_{sw} during Stage 1 and that the dynamic comparator is not operating. Stage 2 begins once Φ_1 falls and Φ_2 goes high triggering the ring oscillator to operate the dynamic comparator. The inductor current is discharging to the load during this time so V_{sw} steady decreases, while V_i is seen as a fixed voltage because of the high switching frequency of the inductor current in comparison to the input voltage. Once the inductor current

reaches zero, V_{sw} is less than V_i causing there to be a change in the dynamic comparators output triggering Φ_1 to charge the inductor and the cycle repeats.

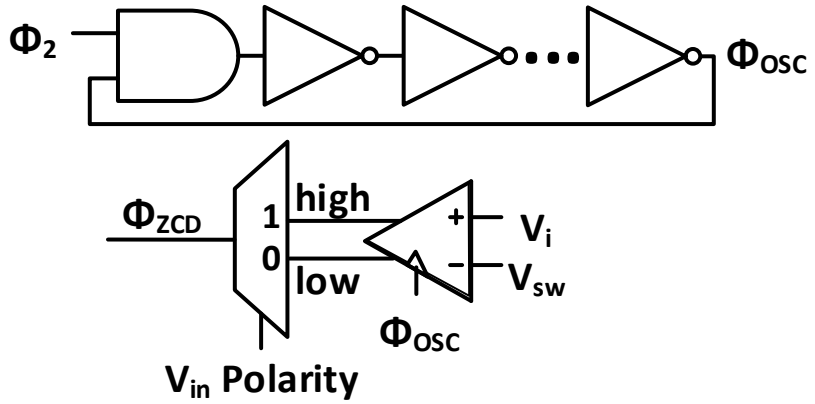

Figure 3-12: ZCD circuit

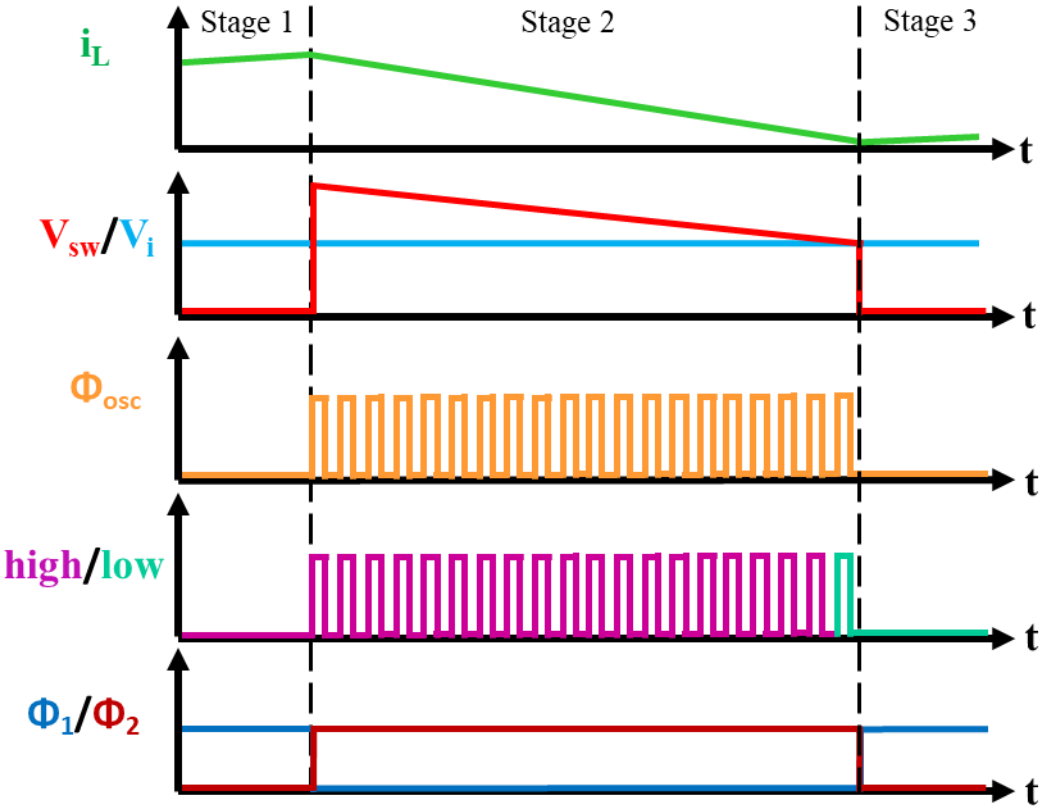

Figure 3-13: ZCS Waveforms

The proposed circuit overview can be seen in Figure 3-14. The sub-blocks discussed in this section are included in the diagram displaying how they contribute to the overall circuit operation. As a brief overview, during the positive cycle Φ_1 is a fixed on-time pulse generated by the MS-

MV circuit. This fixed pulse is precisely controlled as it controls the input impedance of the converter. Once Φ_1 drops low, a falling edge pulse is generated to set the SR Latch beginning Φ_2. Pulse Φ_2 does not fall until the inductor current reaches zero. The zero crossing point is determined by sensing the voltage across the inductor using a dynamic comparator and ring oscillator. The ZCD block is only operated when Φ_2 is high allowing for large power savings. Once V_{sw} becomes less than V_i, the SR Latch is reset causing Φ_2 to go low. The falling edge of Φ_2 is detected triggering the Φ_1 pulse generation block and the cycle repeats. A comparator is used to determine if the input polarity is positive or negative allowing for M4 or M5 to be switched.

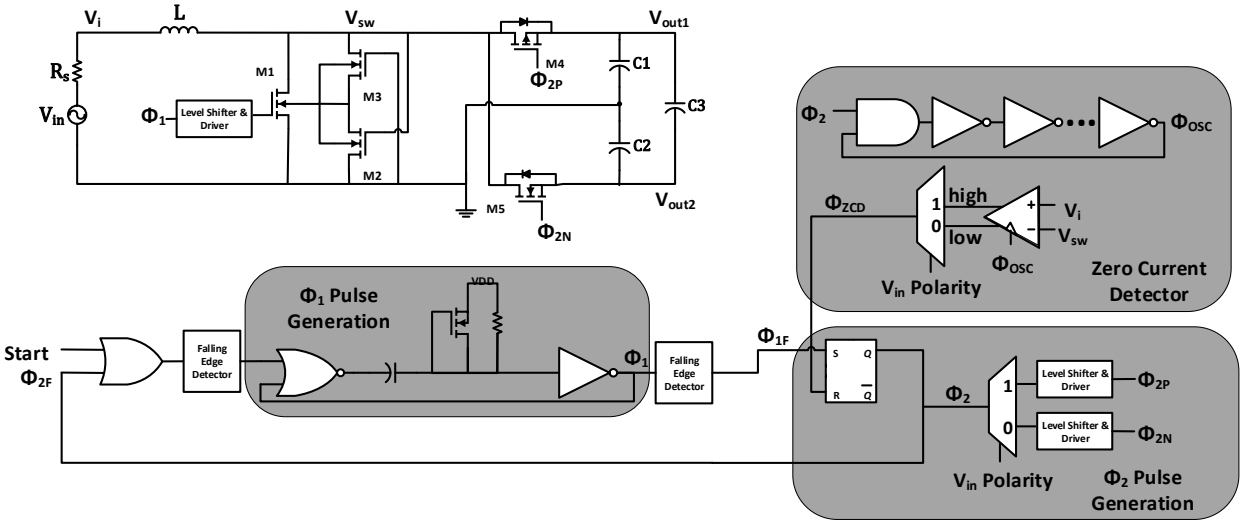

Figure 3-14: Proposed circuit overview

3.4 Chapter Summary

This chapter described the proposed energy harvesting circuit. Major design achievements are:

- BCM operation
- Synchronous rectification
- Control simplicity
- Impedance matching
- Low power design

The design is able to achieve BCM operation and low power design by use of a dynamic comparator. The dynamic comparator has low sensitivity allowing it to detect small voltage difference. The dynamic nature of the circuit reduces power consumption by not actively

consuming power. The use of high-side MOSFETs achieves synchronous rectification and reducing conduction losses. BCM operation is achieved by using an improved MS-MV circuit to fix the on-time, T_{on}.

Chapter 4

Simulation and Measurement Results

The circuit was designed and tested using Cadence Virtuoso 6.1.6 and GloabalFoundries BiCMOS 8HP 130 nm V1.7 process design kit (PDK).

The path to designing an integrated circuit (IC) is lengthy and visualized in Figure 4-1. To begin the design, specifications for the circuit operation were given and explained in Section 3.1. After the design specifications were given and understood, a design or schematic capture was created in Cadence to address the design specifications. Schematic capture includes designing the transistor level sub-blocks, creating symbols for the sub-blocks and connecting the sub-blocks together. Designing and simulation is an iterative intensive process and most of the time on the project was spent here to ensure proper circuit functionality. After simulation achieved the correct behavior, layout of the sub-blocks began. Each sub-block underwent the iterative process of design rule check (DRC), layout versus schematic (LVS), parasitic extraction (PEX) and post-layout simulation for design performance. DRC is the process of ensuring the layout created meets manufacturing requirements defined by the foundry: metal spacing, antenna rules, latchup, etc. LVS confirms that the connections in layout match the connections defined during the schematic capture phase. After DRC and LVS was performed, parasitic extraction was executed to determine added parasitic effects (resistance, capacitance, inductance) from metal layer interconnects. Once each sub-block underwent the iterative layout process, the chip level underwent the same process in a more stringent manner to safeguard proper operation after fabrication.

The following sections display the schematic and post-layout simulations to confirm proper operation of the synchronous split-capacitor boost converter operating in boundary conduction mode.

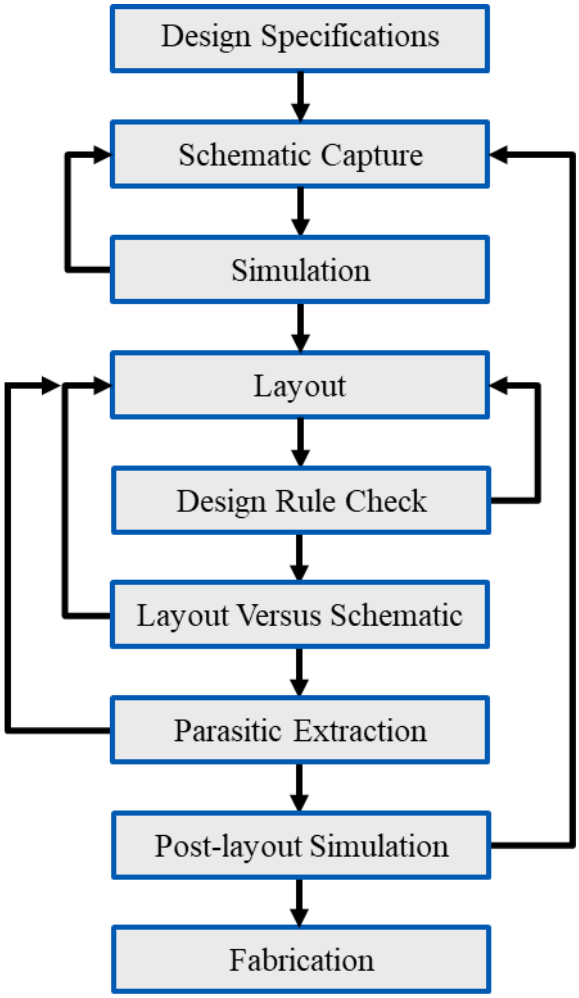

Figure 4-1: IC design flow

4.1 Schematic Capture Results

4.1.1 Dynamic Comparator

The simulation is run with a clock frequency of 50 MHz; a frequency well beyond the needs for the proposed design. When the positive input is higher than the negative input, then Vout1 is high and vice versa. The comparator is able to differ the difference between at least 7 mV. Notice the comparator is only operating when the clock pulse is high. This behavior is known as dynamic and plays an important role in the proposed design. For the proposed design, the dynamic comparator will only have a clock pulse during discharge. Figure 4-3 zooms in on the clock pulses to show operation only when a clock signal is present.

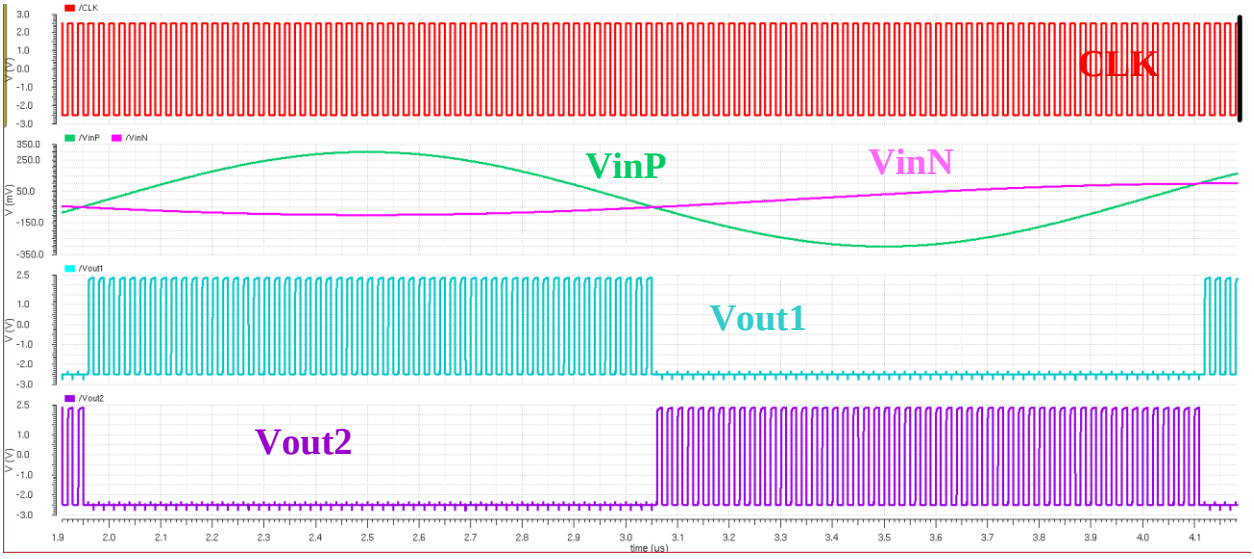

Figure 4-2: Dynamic comparator schematic simulation

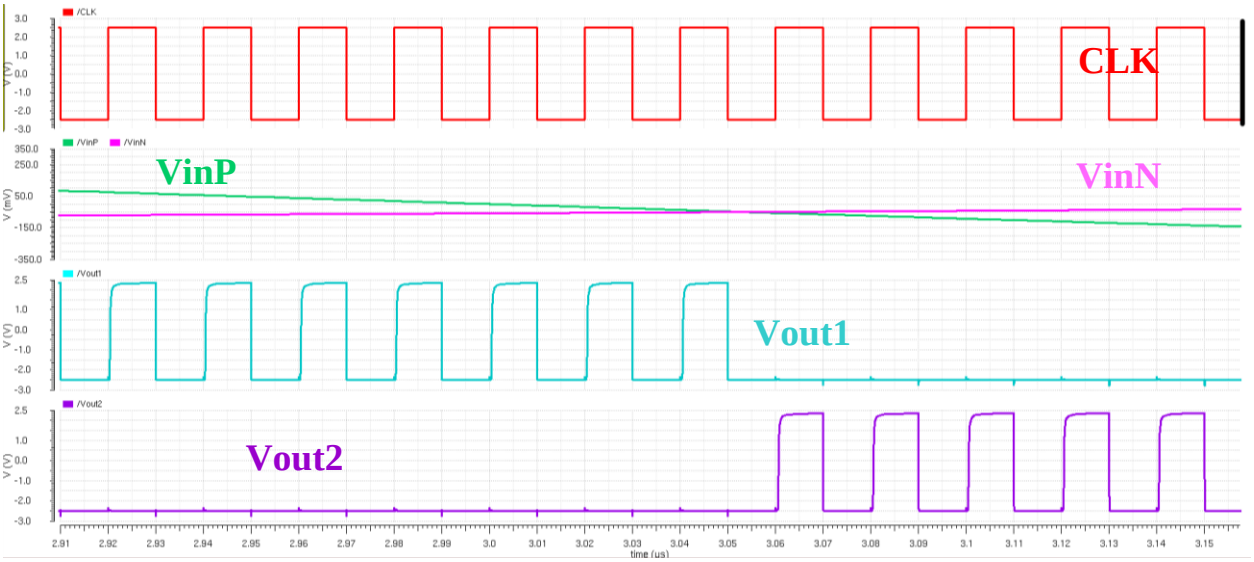

Figure 4-3: Zoomed-in view of Figure 4-2

4.1.2 Mono-stable Multi-vibrator

The MS-MV produces a fixed-width output signal when a short pulse is inputted. The input pulse can be as small as 375 ps. The output signal shown in Figure 4-4 is about 5 µs. The output pulse can be adjusted by tuning the R and C values. With the added NMOS to the MS-MV, the capacitor discharges much faster than it charges. This is because the resistance of the MS-MV circuit is much greater than the on-resistance of the NMOS. This allows the circuit to be retriggered more frequently as the capacitor voltage nears zero quickly. Figure 4-5 shows what occurs when

the NMOS is not added. Notice the time constant has drastically changed during the discharge period. The output pulse width is no longer consistent since the capacitor begins charging from a different value each cycle.

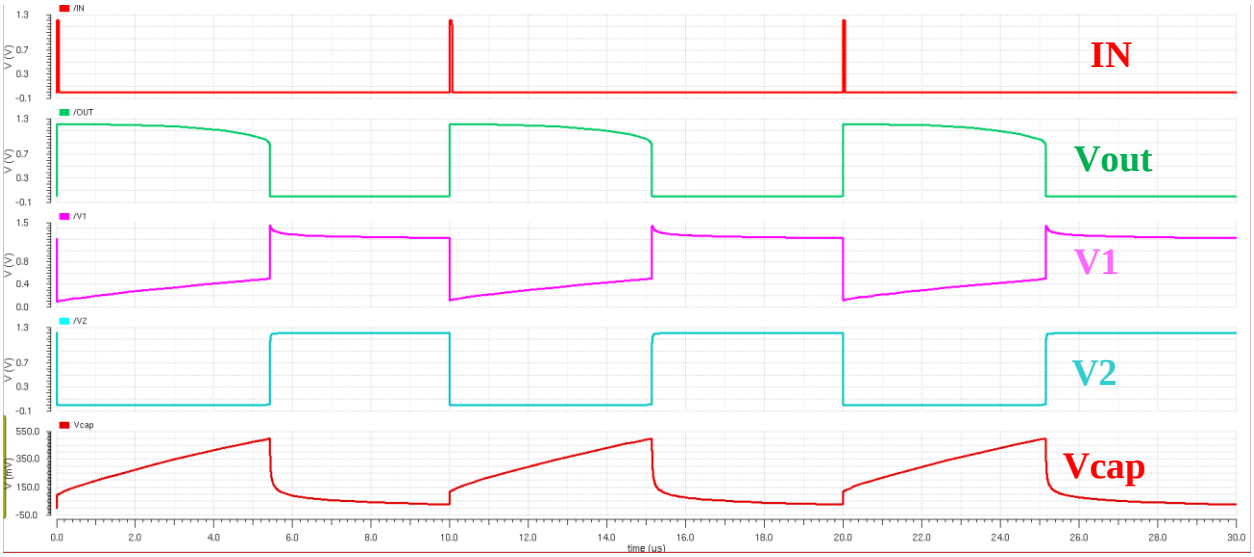

Figure 4-4: MS-MV schematic simulation with NMOS

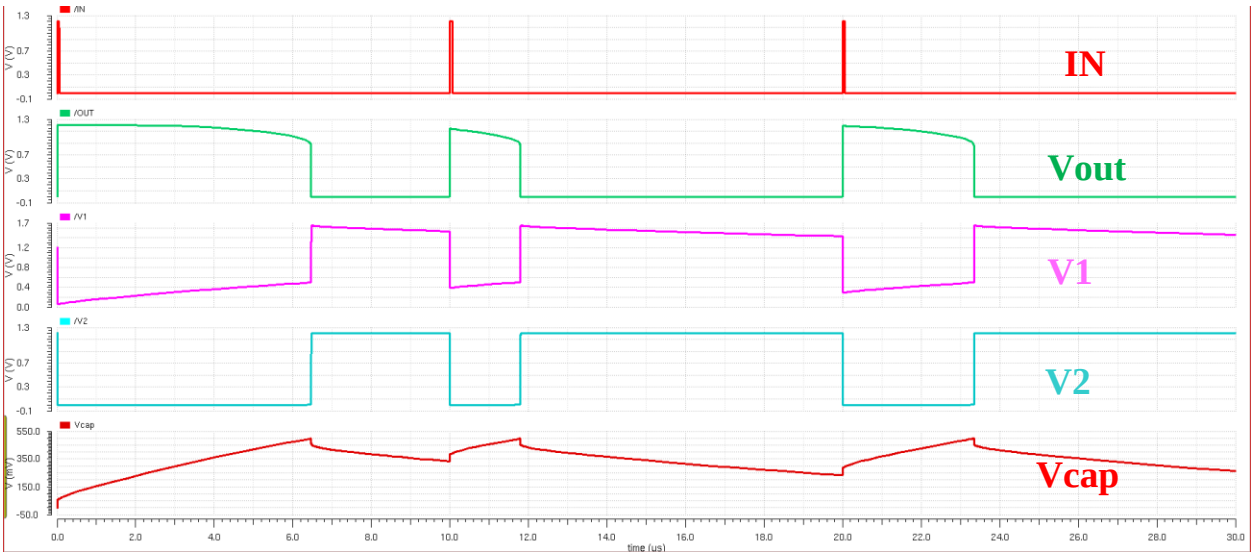

Figure 4-5: MS-MV schematic simulation without NMOS

4.1.3 Level Shifters

In Figure 4-6, the positive level shifter adjusts the positive supply from 1.2 V to 2.5 V. The delay for the positive level shifter is 1.5 ns. The negative level shifter in Figure 4-7 transitions its negative rail from -1.2 V to -2.5 V with a delay of 400 ps. The level shifters exhibit exceptional

signal integrity through the transition process. This is key because the level shifters are used to drive the switching MOSFETs. Following the level shifters is a gate driving connecting to the MOSFETs. The gate drivers were not included in this simulation in order to demonstrate the performance of the level shifters solely.

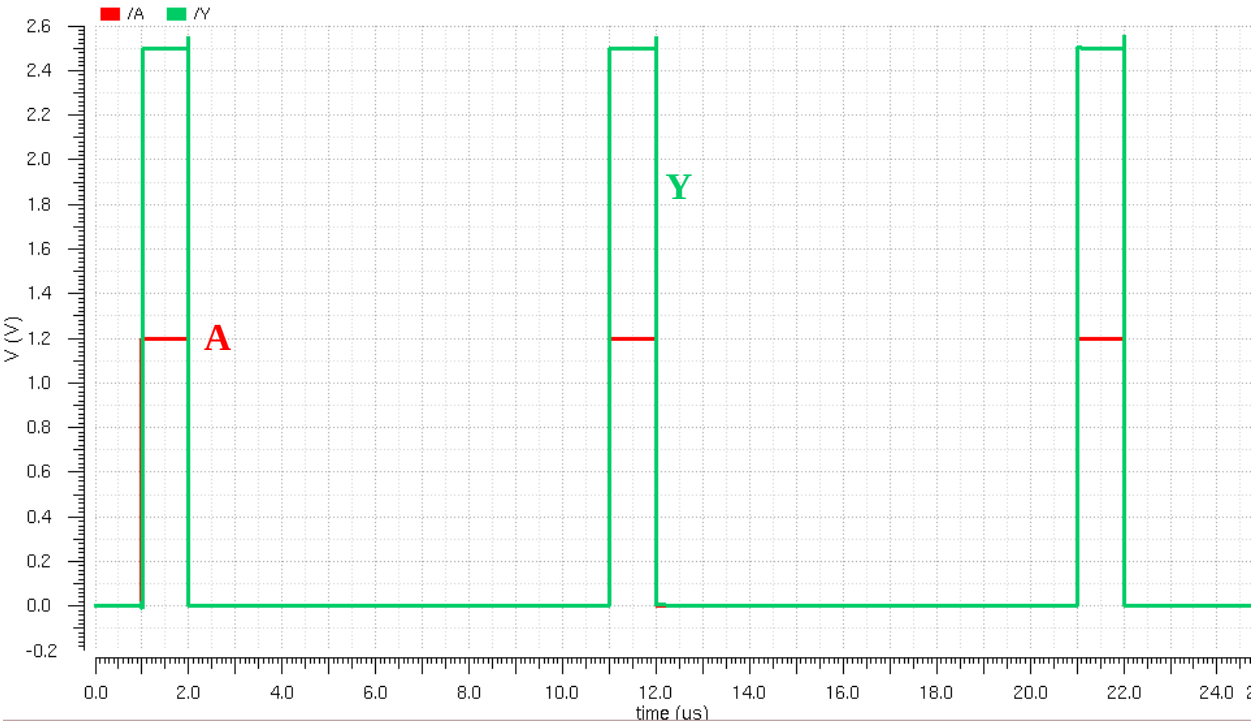

Figure 4-6: Positive supply level shifter schematic simulation

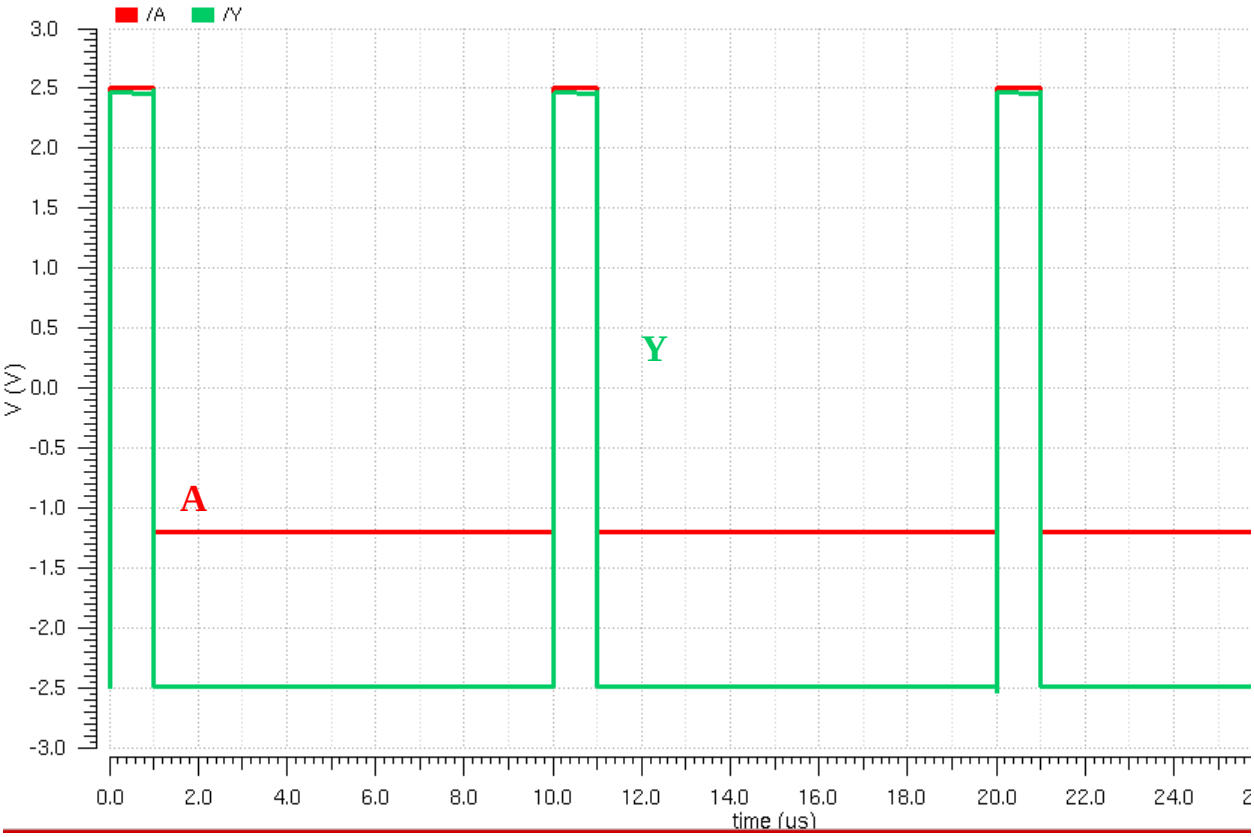

Figure 4-7: Negative supply level shifter schematic simulation

4.1.4 Falling Edge Detector

Figure 4-8 demonstrates the ability of the falling detector block. In this case, Φ_1 fell from 1.2 V to 0 V. The falling edge detector is able to response within 200 ps of Φ_1 falling. Referencing Figure 3-14, the falling edge detector is placed prior to the level shifter and gate driver so that the dead-time between switching can be minimized and the delay of the level shifter and gate driver do not interfere with the falling edge detector. The falling edge detector is responsible for initiating the next cycle for Φ_1 and Φ_2.

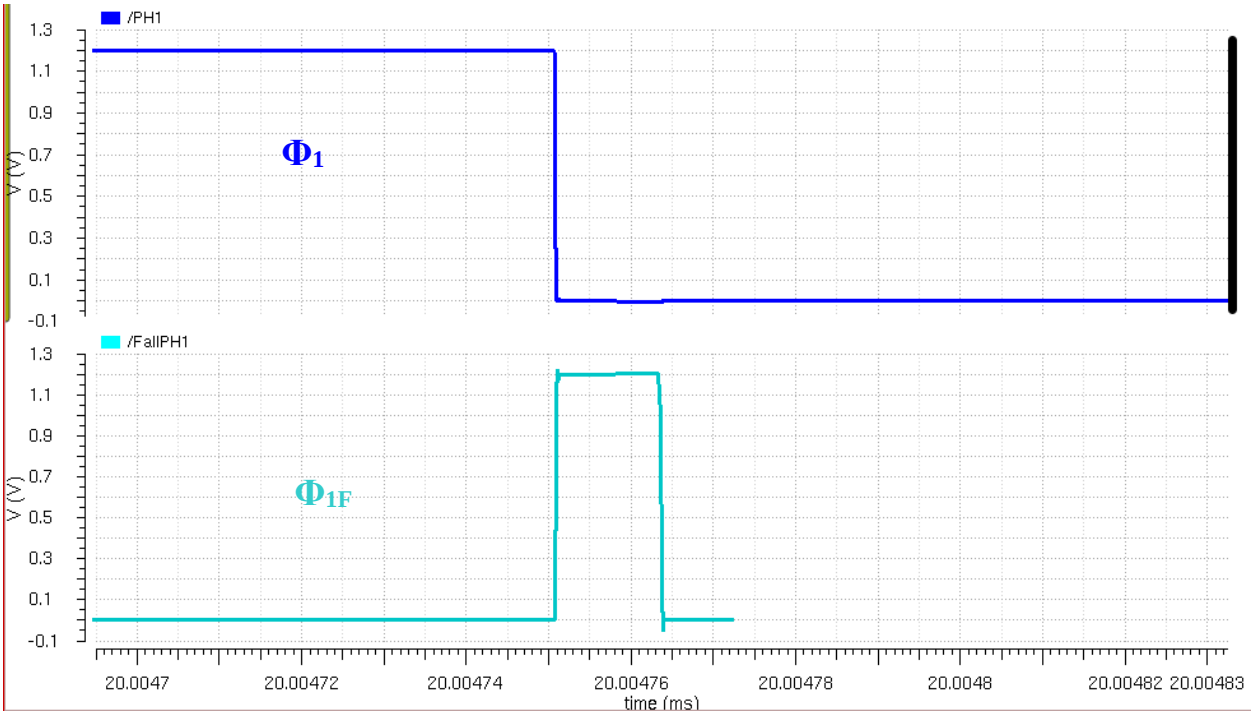

Figure 4-8: Falling detector simulation

4.1.5 Ring Oscillator

The schematic capture simulation of the ring oscillator is shown in Figure 4-9. The circuit able to effectively generate a square wave signal with a frequency of 160 MHz to serve as the dynamic comparator's clock signal. A phase locked loop is not required for this ring oscillator as the frequency or phase drift is not an importance.

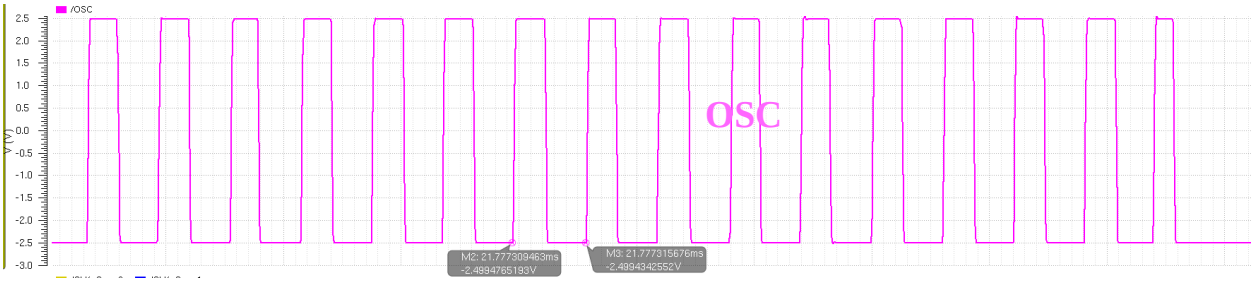

Figure 4-9: Ring oscillator circuit simulation

4.1.6 Cold-start

Cold-start is defined as the circuit's ability to start the circuit, when the load is completely discharged. For the proposed EH circuit, a Start signal is used to begin switching of the converter as seen in Figure 3-14. The start signal is initially high and then switches low to produce a falling

edge. This falling edge is sent to the falling edge detector, initiating the switching to perform BCM operation.

Without inputting a Start signal, the circuit is still able to operate as a boost converter. Albeit in an inefficient manner as impedance matching is lost without switching the converter.

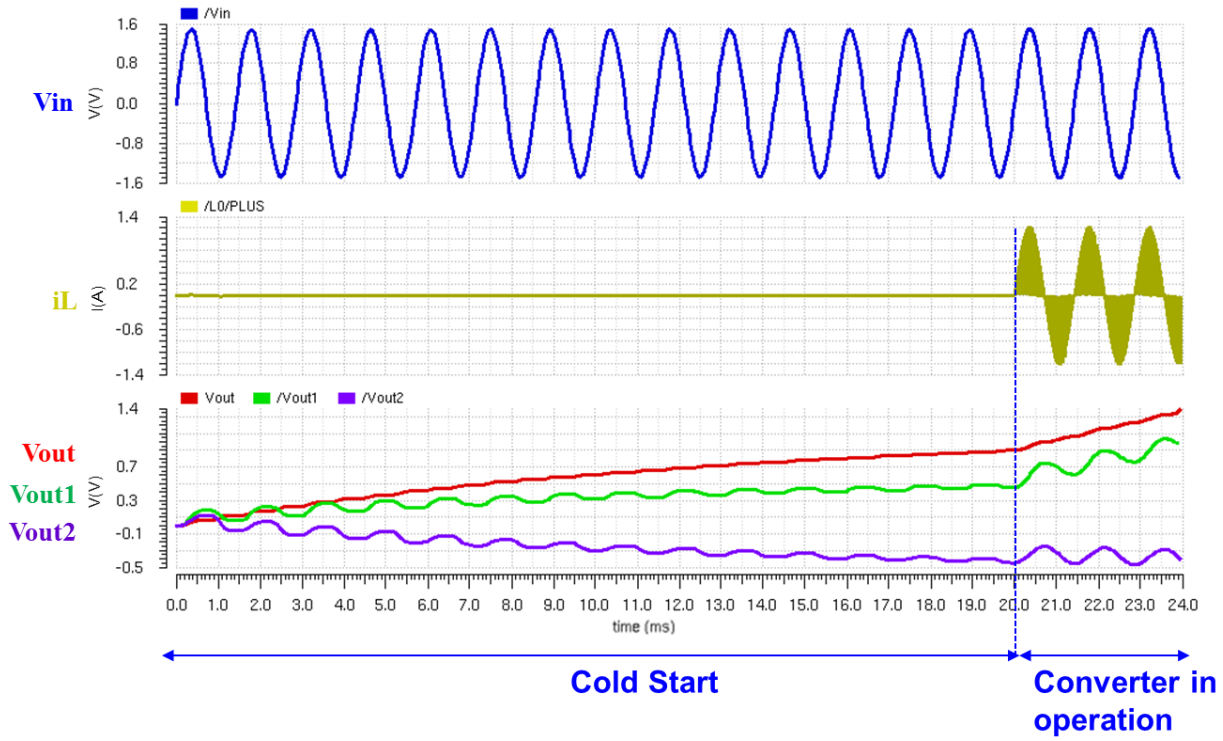

Figure 4-10: Cold-start operation

4.1.7 Proposed Circuit Operation

Following are simulations for the complete proposed circuit design. The EMG has an input amplitude of 1.5 V, 700 Hz frequency and a 1 Ω series resistance, R_s. The components in Figure 3-14 are L = 2.1 µH, C1 = 10 µF, C2 = 10 µF and C3 = 10 µF. These four components including the EMG and R and C from the MS-MV are separate from the IC chip. Temporary values of R and C for the MS-MV are 10 MΩ and 1 pF. They are temporary and left off-chip so they may be tuned during measurement testing to achieve the proper on-time. Per Equation (3.1), the T_{on} is equal to 4.2 µs as L = 2.1 µH and R_s = 1 Ω.

The ZCD timing diagram is shown in Figure 4-11 and analyzes the positive half cycle. The inductor current, iL, discharges to 0 A and immediately begins charging again. During the charging period, voltage Vsw is 0 V as transistor M1 is turned on from Figure 3-14. The voltage Vi is

relativity constant the as the inductor current switches around 1.5 MHz and the input voltage frequency is 700 Hz. The oscillator, OSC, does not operate during the charging period, therefore reducing power dissipation of the power management unit. The output signals, high and low, of the dynamic comparator are also not operating at this time as the dynamic comparator is turned off. The signal Φ_1 is high during the charging period and turns NMOS M1 on. The 2.5 V signal Φ_{2P} maintains an off state for PMOS M4. Once Φ_1 reaches the allotted on-time, T_{on}, M1 turns off and M4 turns on. The inductor current begins discharging. The voltage Vsw quickly rises as there is now a voltage at the node and steadily decreases with iL as less current flows through node Vsw. The ring oscillator is turned on during the discharge period to operate the dynamic comparator. The dynamic comparator compares Vi and Vsw until Vi becomes greater than Vsw and at this point, the inductor current has reached zero. The dynamic comparator output changes to trigger a new cycle and the inductor current begins charging again.

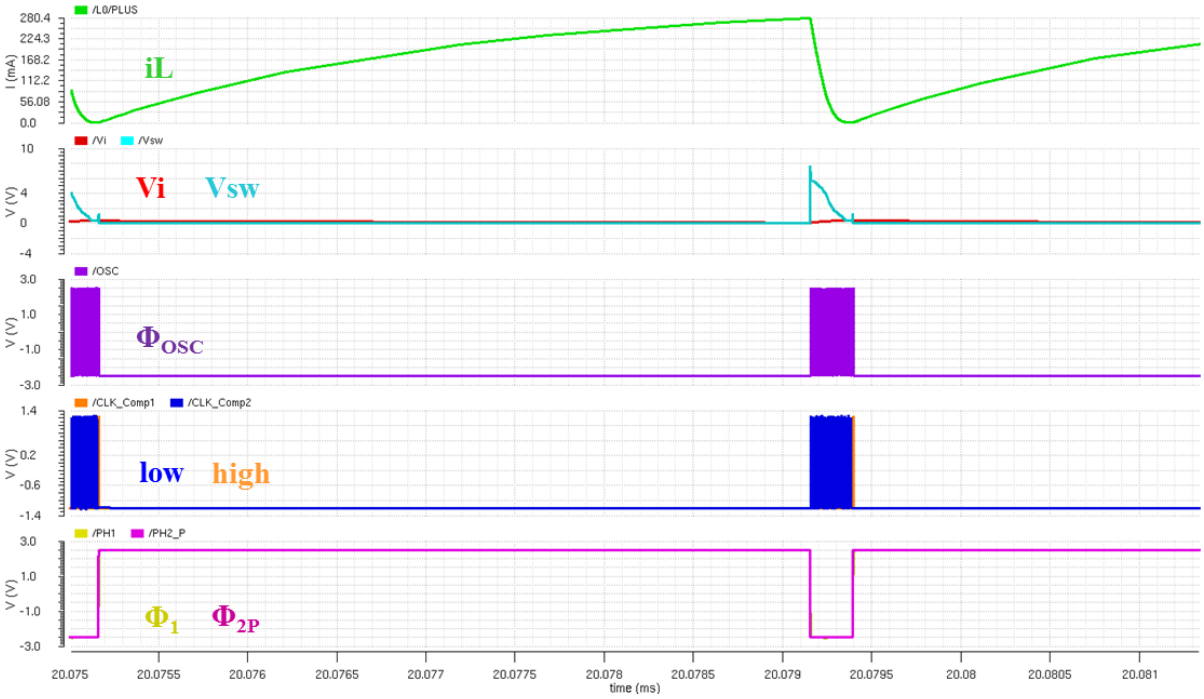

Figure 4-11: ZCD timing diagram simulation of positive half cycle

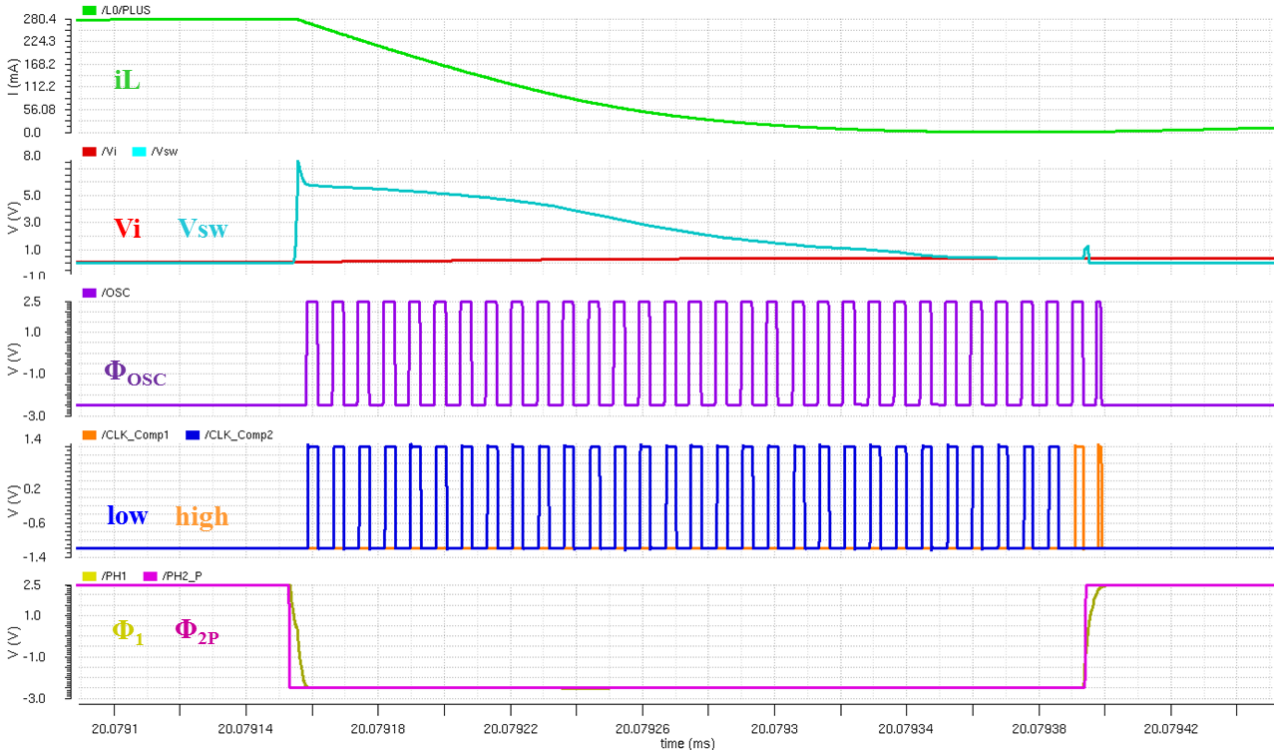

Figure 4-12: ZCD timing diagram simulation of positive half cycle (close up)

Figure 4-13 visualizes the current sharing between M1, M4 and M5 during the positive half cycle. M1 receives all of the current during the charging period and no current is leaked through M4 or M5. During the discharge phase of the positive half cycle, current discharges through M4 to the load and minimal current is leaked through M1 for a short amount of time. No current is leaked through M5 during the positive half cycle as M1 and M4 are the main switches during this period.

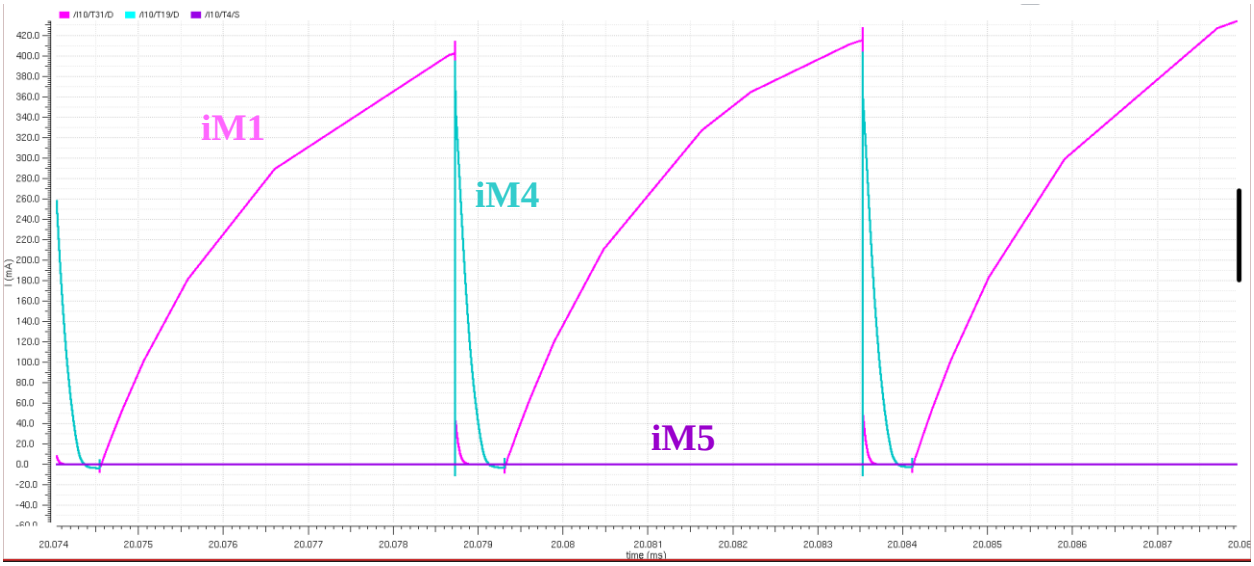

Figure 4-13: MOSFET current sharing during positive half cycle

The curvature in the inductor current is due to the time constant of an inductor, $\frac{L}{R}$. As the direct current resistance or DCR or series resistance with the inductor decreases, the inductor takes a longer time saturate as seen in Figure 4-14. If the charging time was reduced, the inductor current would appear more like a constant slope line as typically seen in power electronics. Varying the three parameters of inductance, series resistance and time, the inductor current would behave differently.

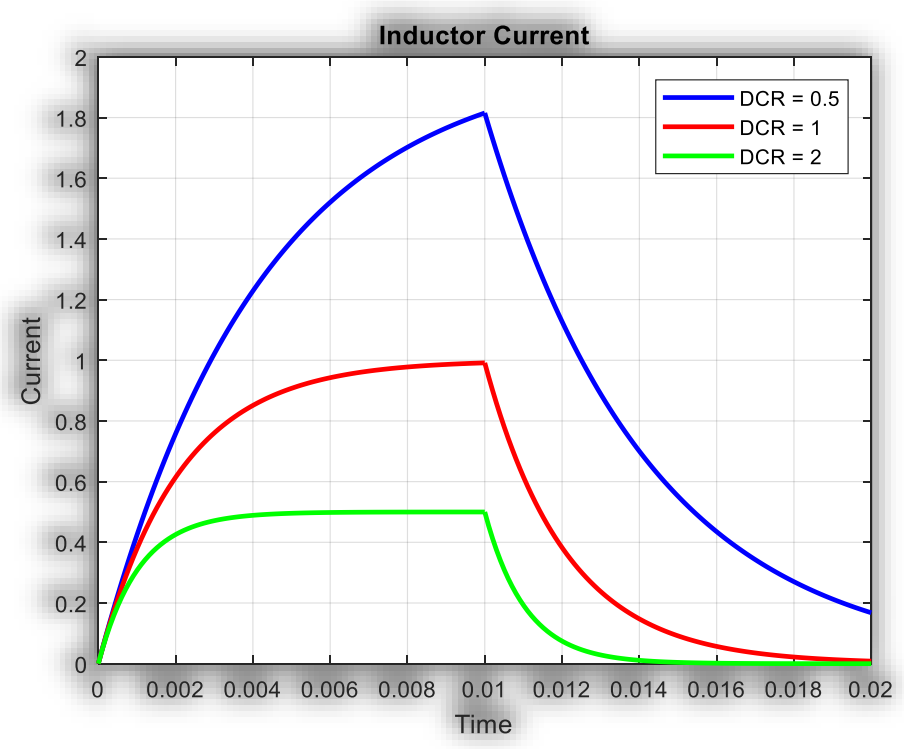

Figure 4-14: Resistance impact on inductor charging

4.2 Post Layout Results

Post layout simulations include the parasitic effects and metal interconnects adding unintended resistors, capacitors and inductors to the circuit. Post layout simulation will have a reduced performance because of this. Layout design techniques were taken into account to mitigate unnecessary parasitic elements. The post-layout simulations are performed at the cell level, while chip level performance will be evaluated after the IC has been fabricated.

4.2.1 Dynamic Comparator

Figure 4-15 shows the post layout simulation of the dynamic comparator. The comparator is placed through the same test case as the schematic level simulation. The dynamic comparator is still able to operate at high frequencies and low input amplitude while still differentiating. The performance difference between schematic level and post layout simulation can be seen in Figure 4-16. The post layout comparator is able to determine the difference greater than 14 mV while the schematic level comparator discerned 7 mV. The decreased performance is tolerable for the proposed design.

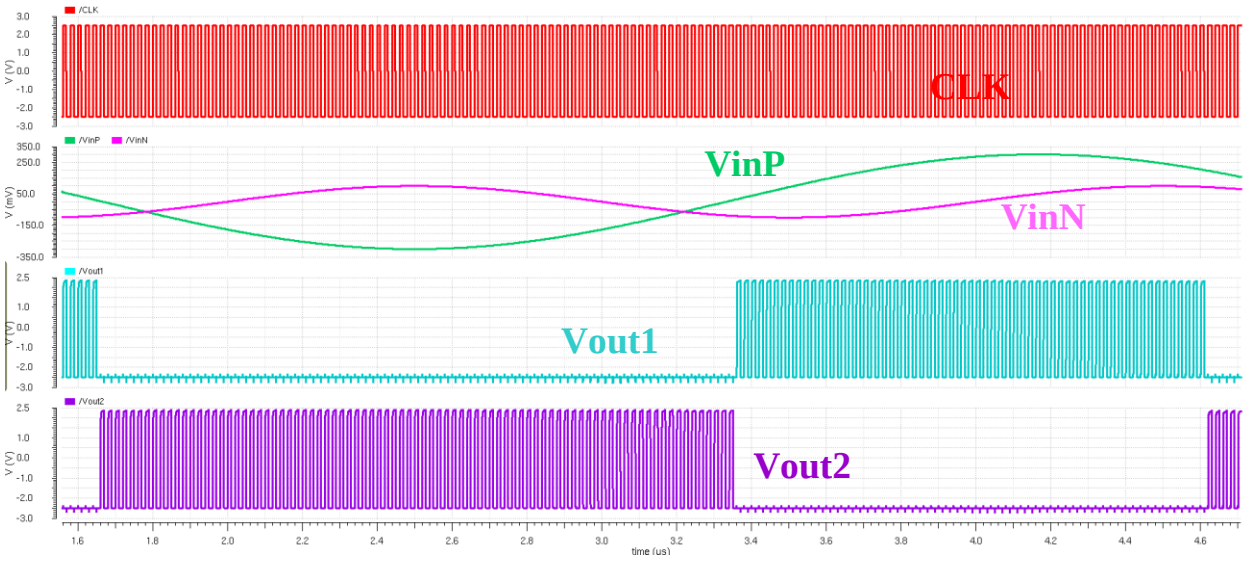

Figure 4-15: Dynamic comparator post layout simulation

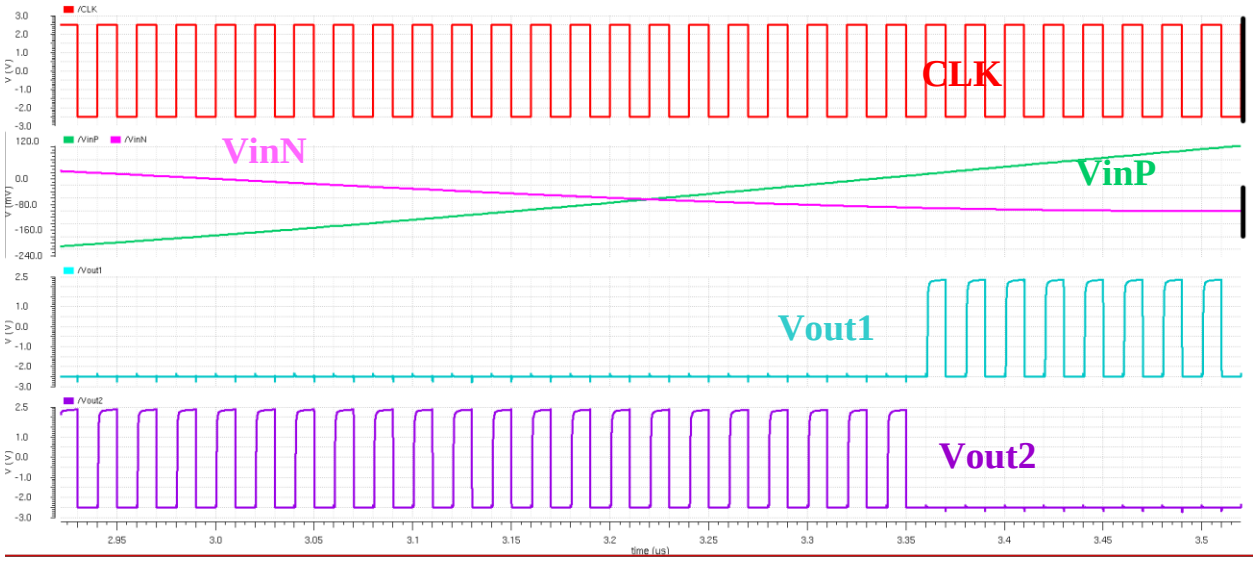

Figure 4-16: Zoomed-in view of Figure 4-15

4.2.2 Mono-stable Multi-vibrator

The post layout MS-MV exhibits the similar performance compared to the schematic capture. A large difference is not noticeable because the MS-MV is comprised of few components. The post layout MS-MV is able to operate with an input pulse of 375 ps as well.

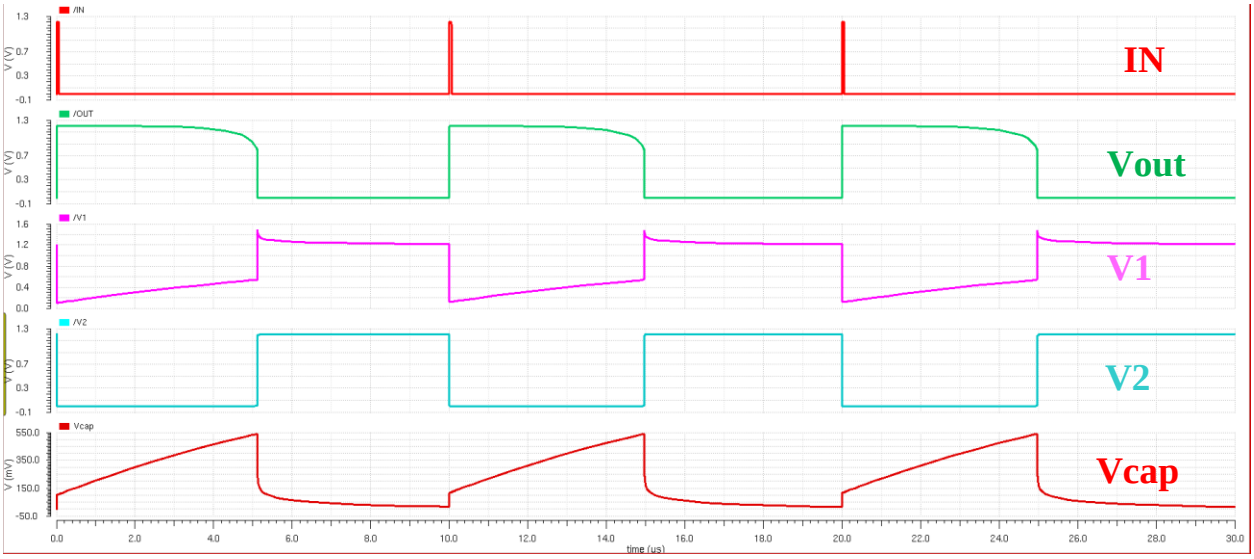

Figure 4-17: MS-MV post layout simulation with NMOS

4.2.3 Level Shifters

The post layout simulation exhibited similar behavior to the schematic capture simulations with the positive supply level shifter having a delay of 1.2 ns and the negative supply level shifter delay was 470 ps. This small delay will help to minimize the delay between switching for the synchronous rectifier.

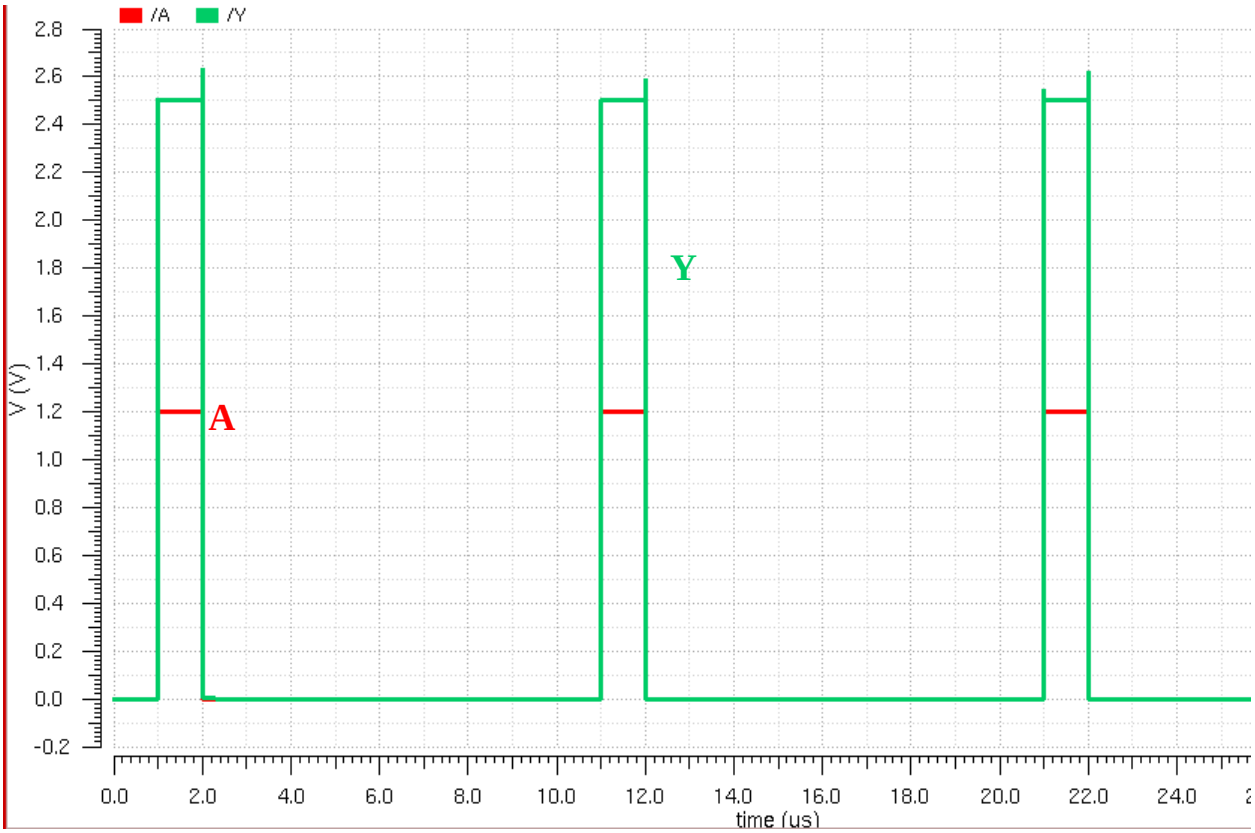

Figure 4-18: Positive supply level shifter post layout simulation

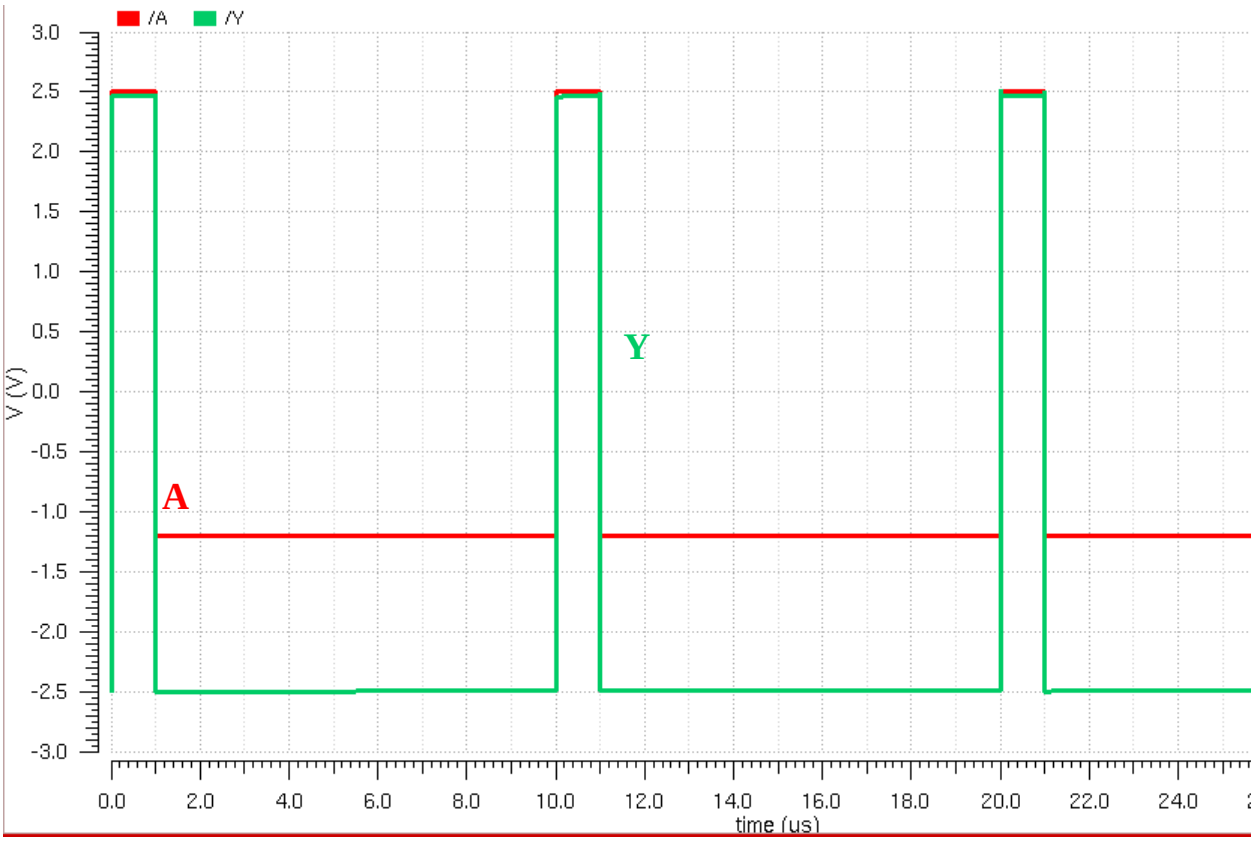

Figure 4-19: Negative supply level shifter post layout simulation

4.2.4 Falling Edge Detector

Compared to the performance of the schematic falling edge detector, the post-layout falling edge detector is able to response within 250 ps compared to 200 ps. The fast response time is critical to reducing dead-time and the simplicity of the circuit achieves a fast response time.

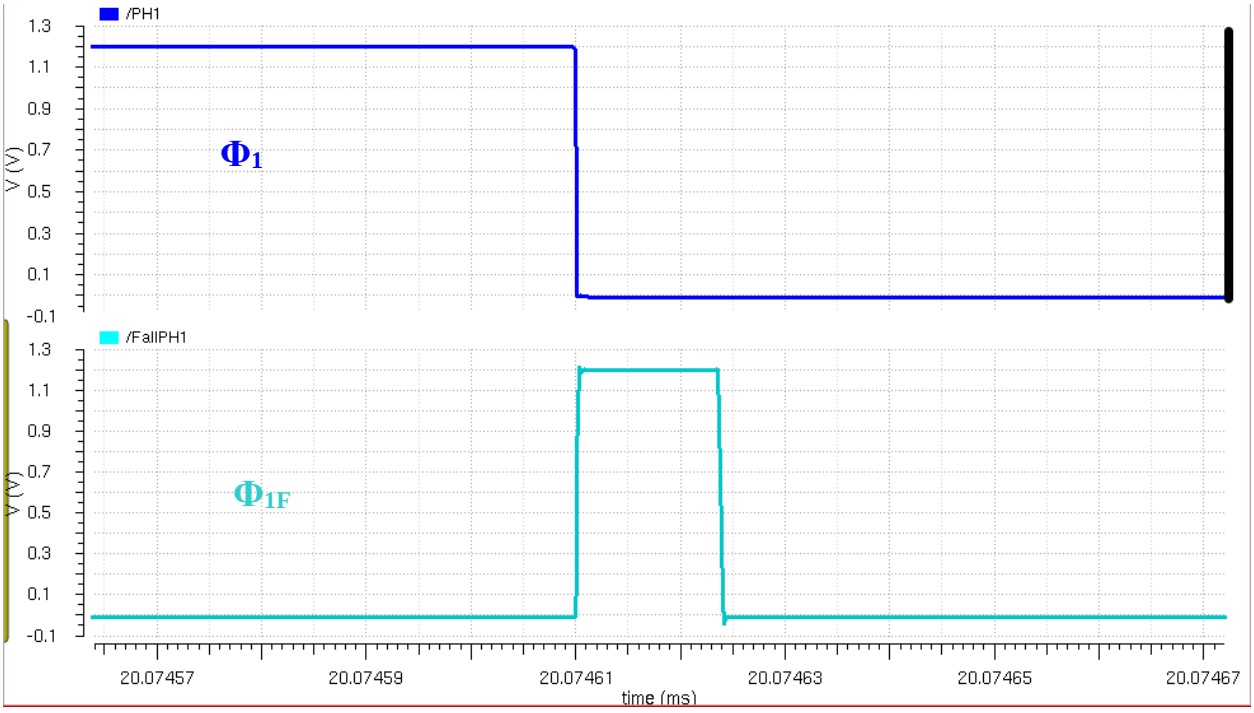

Figure 4-20: Falling edge detector post layout simulation

4.2.5 Ring Oscillator

The post layout ring oscillator achieves 153 MHz switching frequency which is reduced from the 160 MHz of the schematic simulation. The reduced switching frequency is trivial and the frequency does not play an important rule. The clock pulse is used to switch the dynamic comparator. The rise time is 300 ps while the fall time is 250 ps.

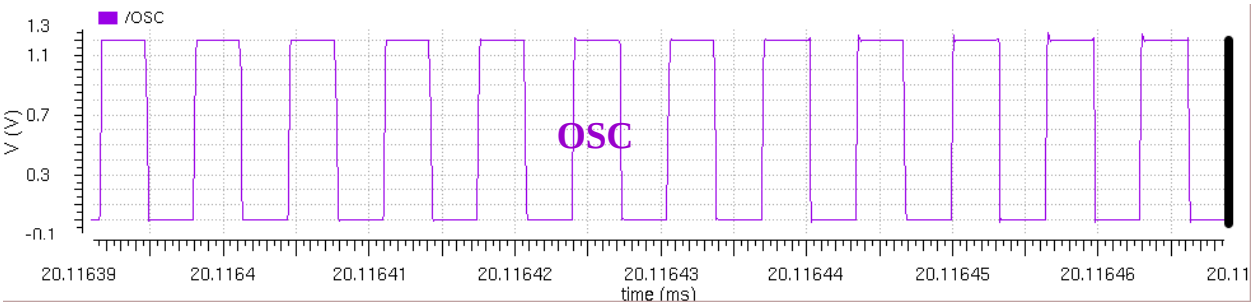

Figure 4-21: Ring oscillator post layout simulation

4.3 Circuit Implementation

To ensure effective testing and ease of block replacement, 40 pins have been utilized. Most of the pin locations are shown in Figure 4-22, while other pins are used for accessory ground, voltage and current supplies. The completed IC chip layout is shown in Figure 4-23. The chip is 2

mm by 2 mm with 40 pin connections. After fabrication, the chip will be packaged in a DIP package for testing. Figure 4-24 demonstrates minimal external connections with the EMG source and boost converter inductor, L, on the input side. The output capacitors C1-C3 perform charge recycling and control the output voltage ripple and charge rate. The external component values may be changed for tuning during testing. A test plan has been created to properly ensure safe and effective measurements.

The test plan and chip design provides flexibility to achieve superb performance. The SR FETs may be bypassed and replaced with external components to vary the on-resistance of the MOSFETs. The terminals to the dynamic comparator can be adjusted to be across the SR FETs instead of the inductor as well. These two options were analyzed during the design and they may be adjusted post-fabrication.

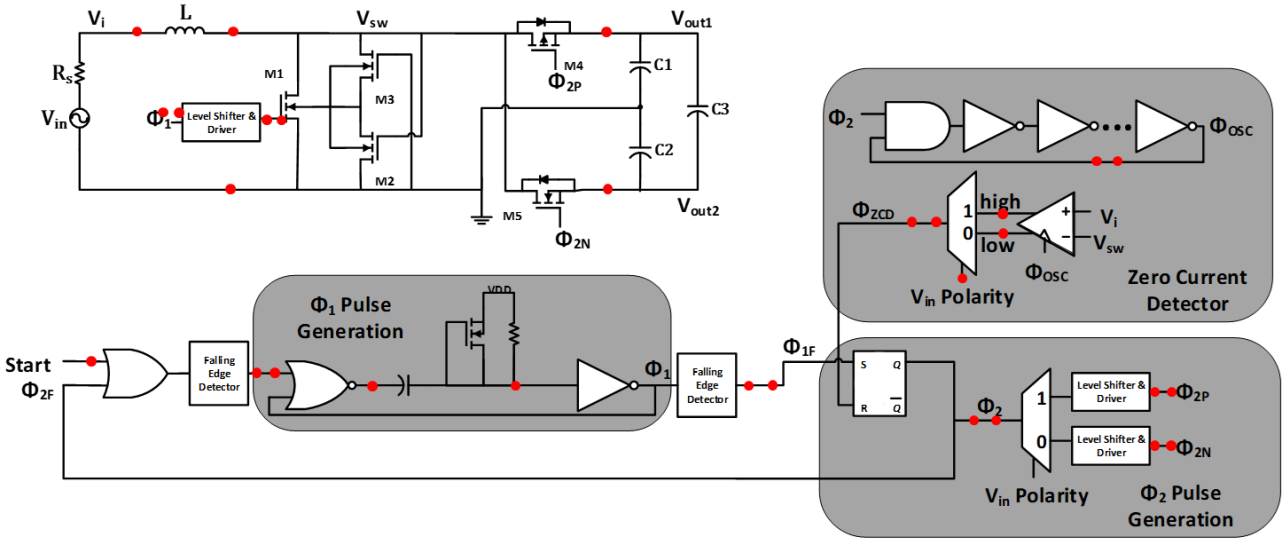

Figure 4-22: Circuit diagram with pin locations

The total area of the chip is 4 mm^2. The dimensions of each block are given in Appendix A. Three negative level shifters are used in the design. The cells used for the chip total to approximately 40 nm^2 of the 4 mm^2 necessary to fabricated the chip. The remaining area used for bondpads, routing and dummy metal.

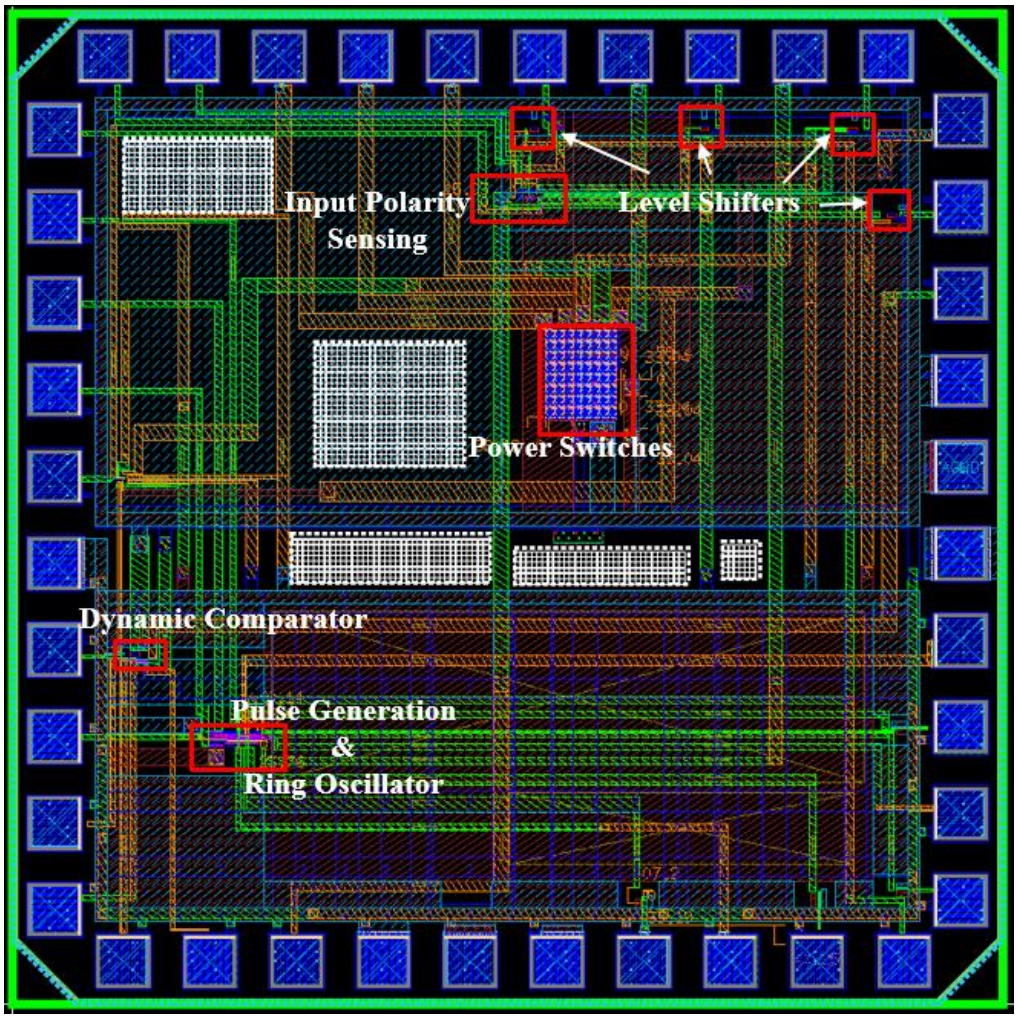

Figure 4-23: IC chip layout

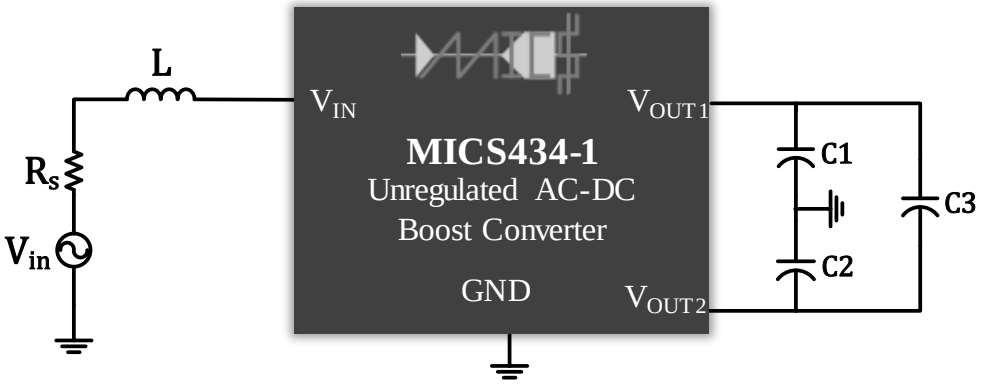

Figure 4-24: Chip and external components

4.4 Chapter Summary

In this chapter, the proposed EH circuit was designed and built in Cadence. Simulation results prove the circuit functionality to perform BCM operation and boost the input voltage. Simulation results also proved the functionality of the improved MS-MV circuit. Post-layout simulations demonstrated reduced performance for cell blocks, however they were still able to perform their main function. A measurement plan was step-up to perform testing once chip arrives from fabrication.

Chapter 5

Conclusion

The proposed EH harvesting circuit introduced a synchronous split-capacitor boost converter operating in boundary conduction mode. The circuit achieved maximum power transfer from the EMG to the load utilizing impedance matching and BCM operation. Simplicity of the power stage and control circuity helped to reduce power consumption of the power management unit.

To control the synchronous converter in BCM operation, a ZCD method was implemented. The inductor DCR was sensed via a dynamic comparator. The major advantage of the dynamic comparator is reduced power consumption. Few components were needed to control the circuit and some were not functional during the charging phase. An improved MS-MV circuit was introduced to expedite retriggering of the circuit. All of these features helped to design a responsive, efficient energy harvesting circuit.

The proposed EH circuit was designed in Cadence and fabricated in GlobablFoundries BiCMOS 0.13 μm technology. Pre and post-layout simulations provide evidence for the functionality of the integrated circuit post-fabrication.

5.1 Key Contributions

The proposed circuit design outlines a framework for a synchronous split-capacitor boost converter operating in boundary conduction mode. The EH circuit develops an improved MS-MV circuit to quickly discharge the capacitor and prevent unequal output pulses. The proposed circuit implements a simpler and more efficient BCM control strategy. A significant reduction in components was used and therefore a smaller IC was developed. A complete listing of input impedances for a buck, boost and buck-boost converter operating in CCM, DCM, and BCM was outlined; this eases converter and operating mode selection for future power management circuit designs.

5.2 Future Work

Once the IC chip returns from fabrication, the chip should be tested following the established measurement plan and designed PCB. As far as the circuit design, there are few areas where the design can be improved:

- **MS-MV:** The MS-MV can be improved further by discharging the capacitor at a faster rate so that the MS-MV is able to retrigger more frequently. The capacitor voltage should be able to start from 0 V for each cycle. Another circuit other than MS-MV may be implemented to output an accurate, consistent T_{on} pulse.
- **Dynamic comparator:** The dynamic comparator and sensing configuration in general can be improved so that BCM operation is more effectively achieved. Tuning of the comparator hysteresis and offset should be performed to ensure the inductor current switches precisely at 0 A.
- **Control strategy:** The control strategy can be provided to reduce the number of components used and to increase the response time from sensing to switching. Increasing the response time and reducing delay will reduce power dissipation and dead-time during synchronous rectification.
- **Output voltage regulation:** A regulation stage should be added to control the output voltage. If feasible, the output voltage regulation stage should be combined with the circuit and not as a separate block. Combining the output voltage regulation will produce a circuit that is capable of rectification, conversion and regulation all in one block.

Appendix

A. Layout of Component Blocks

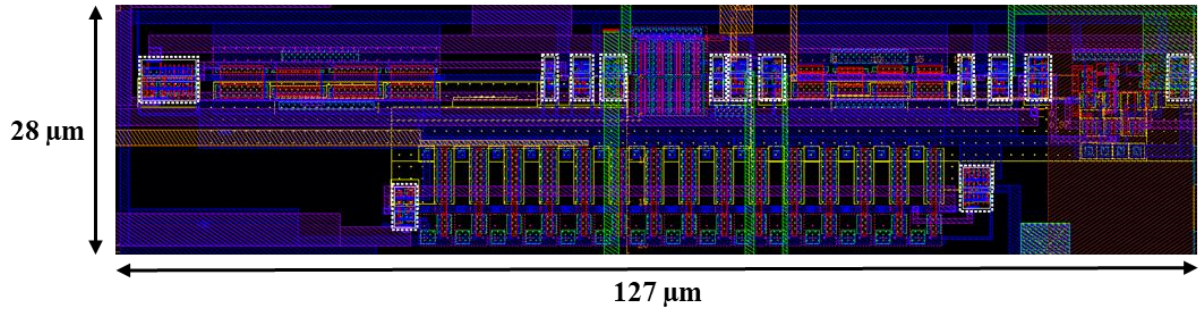

Figure A-1: Pulse generation and ring oscillator layout

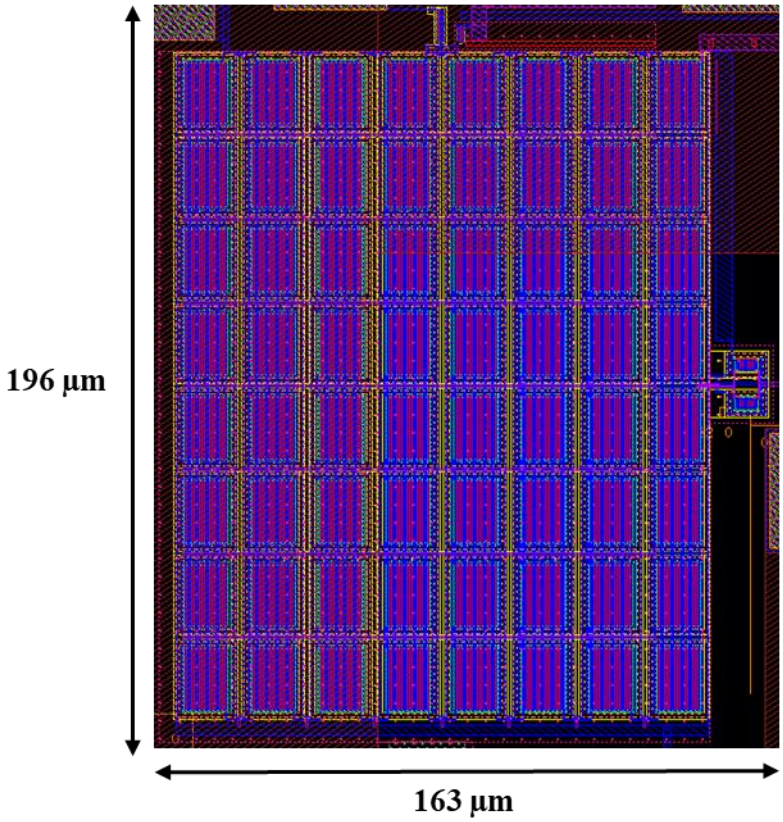

Figure A-2: Power switches layout

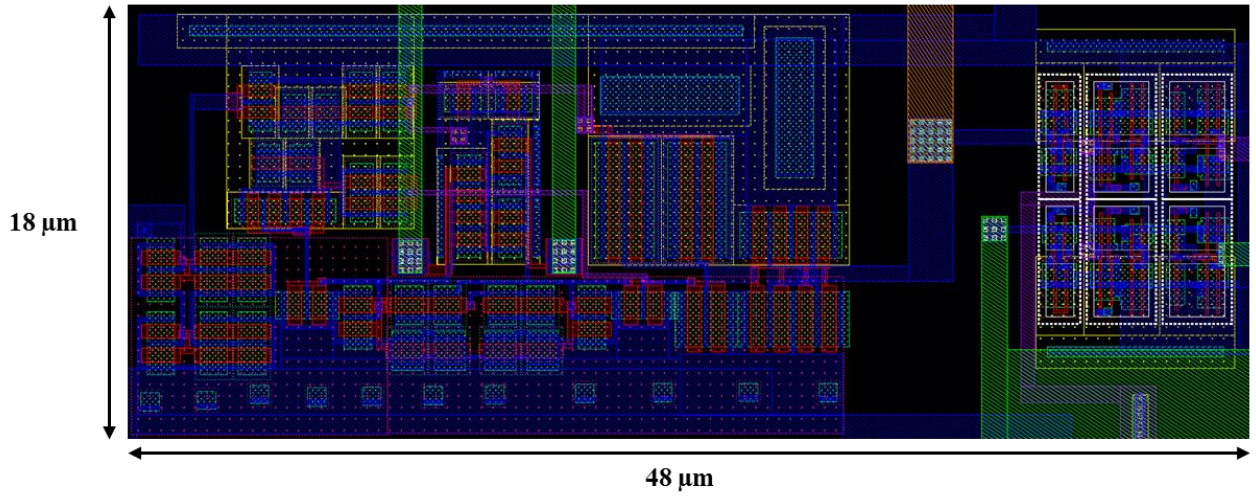

Figure A-3: Dynamic comparator and corresponding logic gates

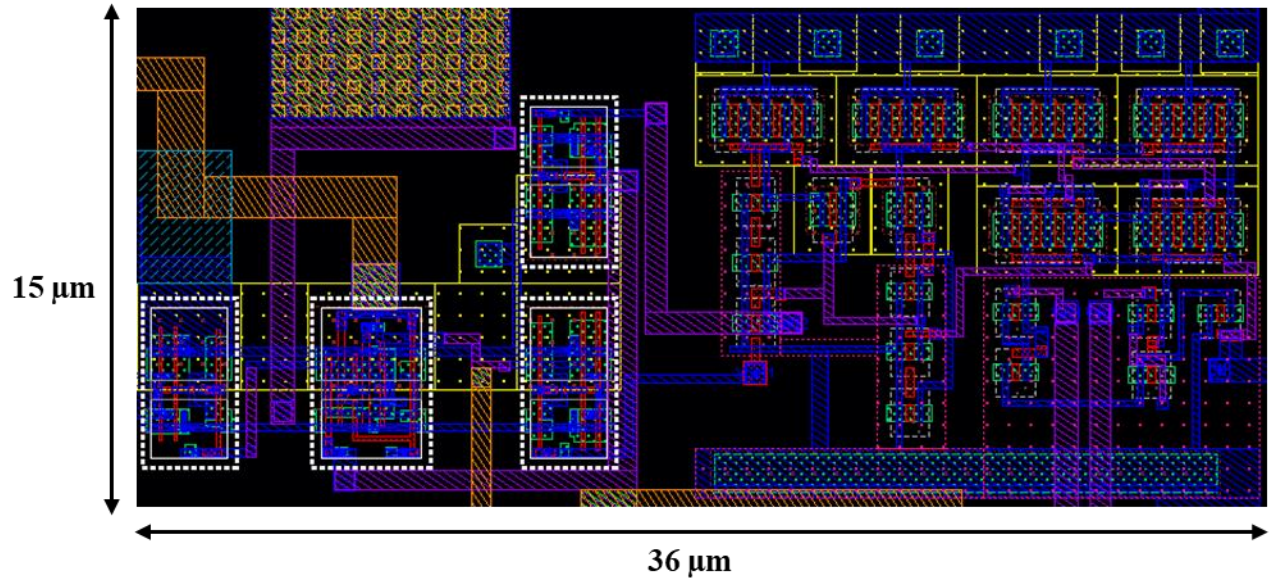

Figure A-4: Input polarity sensing layout

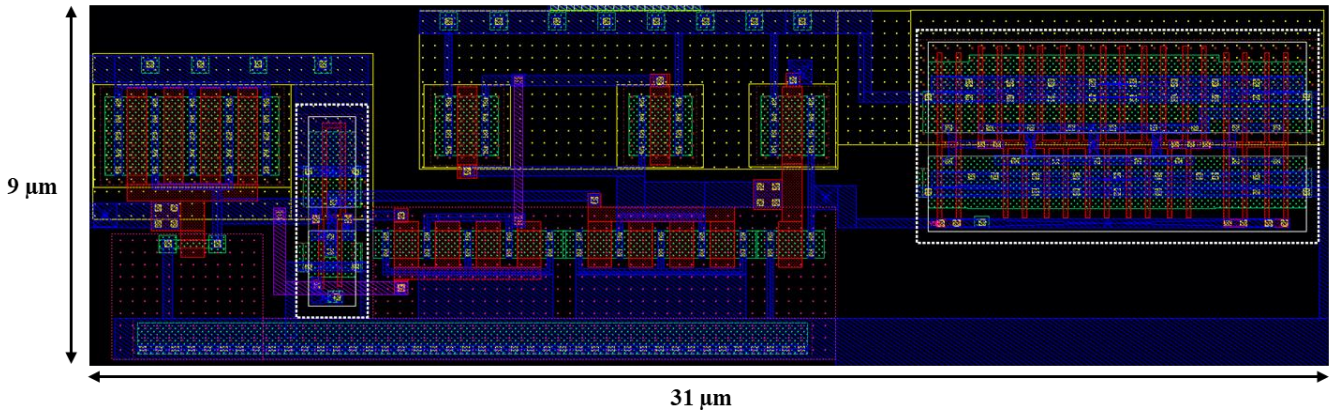

Figure A-5: Positive level shifter and driver

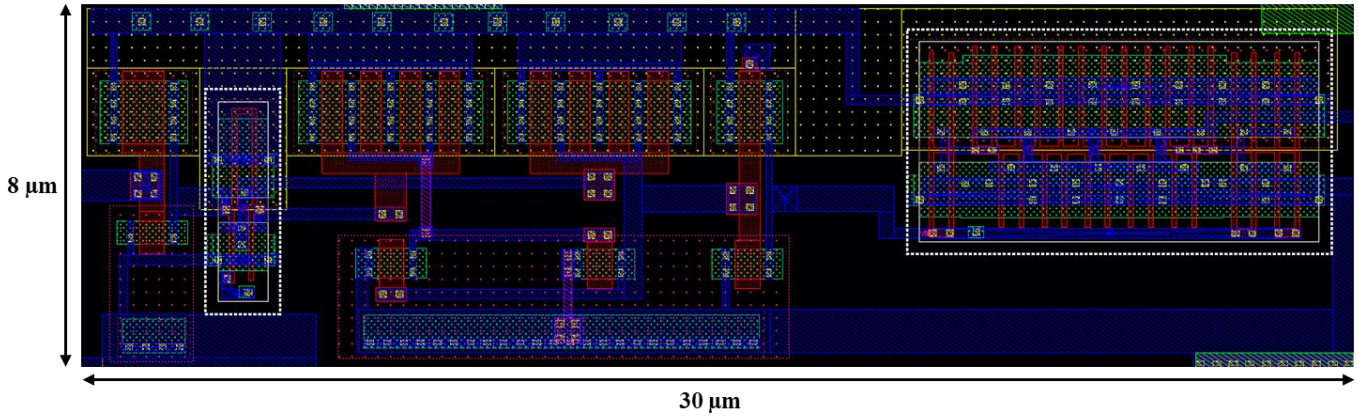

Figure A-6: Negative level shifter layout and driver

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