High-Frequency Oriented Design of Gallium-Nitride (GaN) Based High Power Density Converters

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Abstract

The wide-bandgap (WBG) devices, like gallium nitride (GaN) and silicon carbide (SiC) devices have proven to be a driving force of the development of the power conversion technology. Thanks to their distinct advantages over silicon (Si) devices including the faster switching speed and lower switching losses, WBG-based power converter can adopt a higher switching frequency and pursue higher power density and higher efficiency.

As a trade-off of the advantages, there also exist the high-frequency-oriented challenges in the adoption of the GaN HEMT under research, including narrow safe gate operating area, increased switching overshoot, increased electromagnetic interference (EMI) in the gate loop and the power stages, the lack of the modules of packages for high current application, high gate oscillation under parallel operation. The dissertation is developed to addressed the all the challenges above to fully explore the potential of the GaN HEMTs.

Due to the increased EMI emission in the gate loop, a small isolated capacitor in the gate driver power supply is needed to build a high-impedance barrier in the loop to protect the gate driver from interference. A 2 W dual-output gate driver power supply with ultra-low isolation capacitor for 650 V GaN-based half bridge is presented, featuring a PCB-embedded transformer substrate, achieving 85% efficiency, 1.6 pF isolation capacitor with 72 W/in^3

power density. The effectiveness of the EMI reduction using the proposed power supply is demonstrated.

The design consideration to build a compact 650 V GaN switching cell is presented then to address the challenges in the PCB layout and the thermal management. With the switching cell, a compact 1 kW 400 Vdc three-phase inverter is built and can operate with 500 kHz switching frequency. With the inverter, the high switching frequency effects on the inverter efficiency, volume, EMI emission and filter design are assessed to demonstrate the tradeoff of the adoption of high switching frequency in the motor drive application. In order to reduce the inverter CM EMI emission above 10 MHz, an active gate driver for 650 V GaN HEMT is proposed to control the dv/dt during turn-on and turn-off independently. With the control strategy, the penalty from the switching loss can be reduced.

To build a high current power converter, paralleling devices is a normal approach. The dissertation comes up with the switching cell design using paralleled two and four 650 V GaN HEMTs with minimized and symmetric gate and power loop. The commutation between the paralleled HEMTs is analyzed, based on which the effects from the passive components on the gate oscillation are quantified. With the switching cell using paralleled GaN HEMTs, a 10 kW LLC resonant converter with the integrated litz-wire transformer is designed, achieving 97.9 % efficiency and 131 W/in^3 power density. The design consideration to build the novel litz-wire transformer operated at 400 kHz switching frequency is also presented.

In all, this work focuses on providing effective solutions or guidelines to adopt the 650 V GaN HEMT in the high frequency, high power density, high efficiency power conversion and demonstrates the advance of the GaN HEMTs in the hard-switched and soft-switched power converters.

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General Audience Abstract

Silicon (Si) -based power semiconductor has developed several decades and achieved numerous outstanding performances, contributing a fast development of the power electronics. While the theatrical limit of the silicon semiconductor is almost reached limiting the progress speed to purse the high-efficiency, high-density high-reliability power conversion, the new material, including gallium-nitride (GaN) and silicon-carbide (SiC), based semiconductor, becomes the driven force to retain the development.

Compared with Si-based device, GaN and SiC device own a faster switching speed and a lower on-resistance, enabling the adoption of high switching frequency and the possibility to increase the efficiency, power density and dynamic response. The GaN-based semiconductor is explored to be an even promising game changer than SiC device thanks to a higher theoretical ceiling. However, to adopt GaN-based semiconductors and fully utilize its benefits with high switching frequency, there are numerous high-frequency-oriented challenges, including high frequency oscillation at device termination, increased electromagnetic interference (EMI), the lack of the modules of packages for high current application, high frequency oscillation under parallel operation.

The dissertation is developed to address the key high-frequency-oriented challenges to adopt GaN-based semiconductors in the power conversion and come up with the novel design strategy and analysis for high-switching-frequency power conversion using GaN devices.

To the reduce the increased EMI emission in the gate loop, a novel PCB-embedded transformer structure is proposed to maintain a low isolation capacitor in the gate driver power supply for the GaN phase leg. With the proposed technique, the dual-output gate driver power supply can achieve high efficiency (85%), ultra-low isolation capacitor (1.6 pF) with high power density (72 W/in^3).

To reduce the high frequency oscillation at the GaN device termination, the strategy to layout GaN devices and its gate driver is proposed with corresponding thermal management A compact structure for three-phase inverter is then presented, operating with a very high switching frequency (500 kHz). Within the inverter, the high switching frequency effects on the inverter performances are assessed to demonstrate the tradeoff and bottle neck to adopt high switching frequency in the motor drive application. In order to reduce the inverter EMI emission at high frequency (>10 MHz), an active gate driver for GaN device is proposed for the active dv/dt control strategy.

To build a high current power converter, the strategy to parallel GaN devices is proposed in the dissertation with the analysis on the commutation between the paralleled GaN devices. A high-frequency high-current litz-wire transformer structure for LLC resonant converter is presented with modeling and optimization. With the technique, a 10 kW LLC resonant converter achieves high efficiency (97.9 %) and high power density (131 W/in^3)

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Chapter 1. Introduction

1.1 Advantages of Gallium-Nitride high-electron-mobility transistors

Nowadays wide-band-gap (WBG) devices, like silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) and gallium nitride (GaN) high-electron-mobility transistors (HEMTs), have been widely applied in the power converter design. Thanks to the advantages of the material, whose properties are listed in Table 1-1 [1], the WBG devices feature the wider band gap, higher critical field, faster electron mobility and velocity, allowing the faster transition and lower switching loss.

Table 1-1 Material properties of GaN, SiC, and Si [1]

Parameter	***GaN***	***SiC***	***Si***
Band Gap E_g (eV)	3.4	3.2	1.12
Critical field E_{crit} (MV/cm)	3.3	3.5	0.3
Electron mobility μ_n ($cm^2/(V•s)$)	990-2000	650	1500
Saturated drift velocity V_s ($x10^7$ cm/s)	2.5	2.0	1.0
Relative permittivity ε_r	9	9.7	11.8

The wider band gap of the WBG devices reflects stronger bonds between atoms in the lattice within the semiconductors, which means the electron needs more energy to jump between the sites. To this end, the WBG devices tend to have smaller leakage current and higher operating temperature. With a higher critical field energy, the width of the drift region w_{drift} is smaller with a given breakdown voltage V_{BR} according to (1.1), leading to a higher concentration of

carriers in the drift region. This also verifies by (1.2), where q is the electron charge, N_D is the electron number, ε_0 is the vacuum permittivity and ε_r is the relative permittivity of the material. As a result of the higher electron concentration, the on-resistance R_{on} with a higher E_{crit} and a larger electron mobility μ_n is smaller with a given V_{BR} according to (1.3). With (1.3) and the material properties listed in Table 1-1, the theoretical limitation of GaN, SiC and Si can be calculated and shown in Fig. 1-1. As shown in Fig. 1-1, both SiC and GaN devices can achieve low on-resistance with a given breakdown voltage due to their higher critical electrical field strength. GaN has further illustrated its potential advantage compared with SiC as a result of the enhanced mobility of electrons, allowing a smaller size for a given R_{on} and V_{BR} [1]. With a smaller die size, the die capacitance can be reduced so that the switching transition can be faster, contributing to a lower switching loss and enabling high switching frequency operation [2].

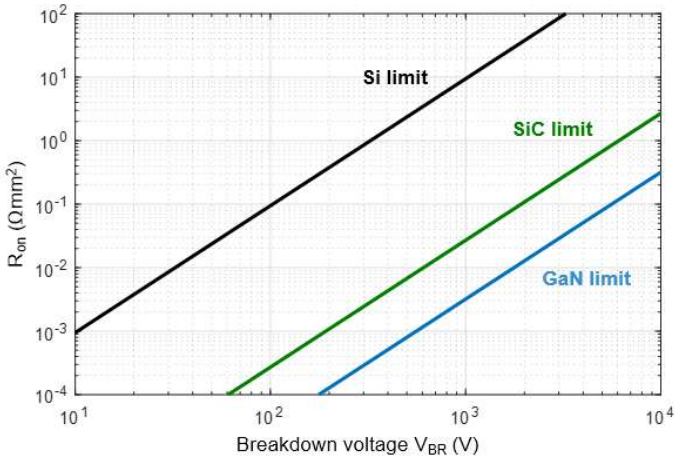


Fig. 1-1 Theoretical on-resistance vs blocking voltage capability for Si, SiC and GaN [1]

$$V_{BR} = \frac{1}{2} w_{drift} E_{crit} \tag{1.1}$$

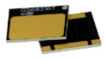
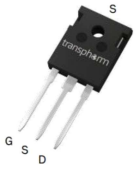
$$N_D q = \frac{\varepsilon_0 \varepsilon_r E_{crit}}{w_{drift}} \tag{1.2}$$

$$R_{on} = \frac{w_{drift}}{N_D q \mu_n} = \frac{4V_{BR}^{\ 2}}{\varepsilon_0 \varepsilon_r \mu_n E_{crit}^{\ 3}} \tag{1.3}$$

Thanks to the higher theoretical limitation of GaN devices than Si and SiC devices, many semiconductor companies join the GaN market, where 600 - 650 V rating is one of the most attractive area that many manufacturers target on. One of the greatest opportunities for energy conservation by using 600 - 650 V GaN devices involves the use of efficient motors driven by the inverters in appliances and transportation drive systems [2]. With the adoption of the GaN devices, the switching loss can be significantly reduced to achieve a high efficiency compared with traditional Si-based inverter design. In addition, the GaN devices have also shown its advantages in the plug-in electrical vehicle (PEV) or plug-in hybrid electrical vehicle (PHEV) charger design, where a high switching frequency can be applied to shrink the passive component size, such as the transformer, input and output capacitors, enabling a high power density and high efficiency design.

Table 1-2 compares the characteristics of the typical GaN, SiC and Si devices within 600 – 650 V voltage rating or similar current rating (60 A) [3]-[7]. Fig. 1-2 compares the parasitic capacitors of these devices under different drain-source voltage V_{ds}. Based on the comparison, enhanced-mode (E-mode) GaN HMETs from GaN System have the lowest on-resistance, the smallest capacitors and the smallest package. The footprint of this E-mode GaN can be one quarter of that of To-247. Furthermore, unlike the SiC and Si devices, the GaN devices do not have the reverse recovery loss. To this end, around 650V and 60A rating, the E-mode GaN from GaN System is a very competitive candidate.

Table 1-2 Comparison among GaN, SiC and Si devices under similar rating

				
	GaN Systems	transphorm	CREE	infineon
	E-mode GaN	***Cascade GaN***	***SiC MOSFET***		***Si CoolMOS***
Part No.	GS66516T [3]	TPH3207WS [4]	C3M0065090D [5]	C2M0025120D [6]	IPW60R045CP [7]
V_{ds} /V	650	650	900	1200	650
I_{ds} /A	60	50	60	90	60
R_{ds_on} /mΩ	25	35	40	25	40
C_{oss} /pF	130	202	150	220	320
Size /mm	9.0 x 7.6 x 0.54	TO-247 (15.88x20.85x5)			

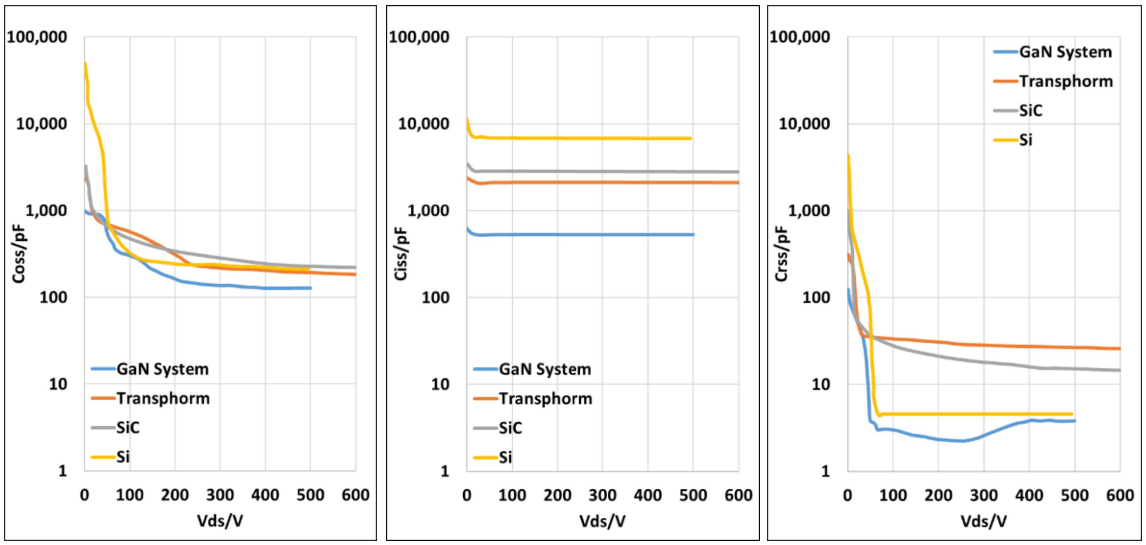


Fig. 1-2 Capacitance vs V_{ds} of GaN, SiC and Si [3]-[7]

To this end, this dissertation targets on the application and research on the 650V 60A E-mode GaN HMETs [3], including its gate driver design, power circuit design, dynamic characteristics, thermal design, EMI consideration in order to build high-efficiency high-power-density power converters.

1.2 Challenges Using GaN HEMTs

1.2.1 Challenges using the e-mode GaN HEMTs in question

A. Narrow gate safe operation area

As a tradeoff of these benefits using GaN devices, there are several challenges using them. First, the safe operation area of the GaN HEMT gate is very narrow. To driver the 650 V enhanced-mode GaN HEMT in question, 6.5 V is adopted to turn on the device whereas the maximum gate voltage is only 10 V [3]. To reduce the gate oscillation and maintain a fast turn-on speed, a small gate loop is expected. Table 1-3 compares the recommended driving voltage and maximum gate voltage of E-mode GaN and cascade D-mode GaN. The E-mode GaN driving voltages are very close to the maximum voltage, whose gate voltage margin is less than 3.5V. A large gate parasitic inductance from an inappropriate gate layout may introduce large gate oscillation and break the gate. As a comparison, driving margin of the cascade D-mode GaN is as high as half of the maximum driving voltage, in favor of device gate driver layout.

Table 1-3 Gate safe operation voltage of different GaN devices

	E- mode GaN			***Cascade D-mode GaN***	
Manufacture	*GaN System*	*EPC*	*Panasonic*	*IR*	*Transphorm*
V_{th}(V)	1.2	1.4	1.2	2	1.8
Driving turn-on voltage (V)	6.5	5	3.2	6	10
Driving turn-off voltage (V)	-4~0	0			
Max V_{gs} (V)	±10	-5 ~ 6	-10 ~ 4.5	±20	±18

B. Increased electromagnetic interference in the gate loop

With the increased electromagnetic interference (EMI) emission generation, the EMI emission circulating through the gate driver circuit also increases. As illustrated in Fig. 1-3, the EMI generated by the high dv/dt at the switching node of a converter phase-leg can propagate from the high-side device source terminal, through the isolated power supply to ground. Z_l in Fig. 1 refers to the impedance between the power loop ground and the ground of the gate driver power supply primary side. i_{CM_GD} in Fig. 1-3 represents the total CM current in the gate driver loops, including the main propagation path at the high side gate driver and the path in the low side gate driver power supply. The isolation capacitance of the high-side isolated power supply builds an inherent barrier to attenuate i_{CM_GD}. The EMI propagation path puts at risk the integrity of the gate-drive circuitry and the converter itself by disrupting the logic circuitry and making possible the generation of spurious gate-signals and shoot-through faults as it was analyzed in [3][9]. In effect, the conducted CM emission in the gate-driver loop i_{CM_GD} was measured in [9] with different isolation (input-output) capacitance in the gate driver power supply, showing how this conducted CM emission could distort the output of the gate driver power supply and gate drive [10]. Accordingly, to protect the gate driver from the increased EMI emission, a small isolation capacitance is necessary to attenuate the EMI emission within the gate driver loop [3]–[10].

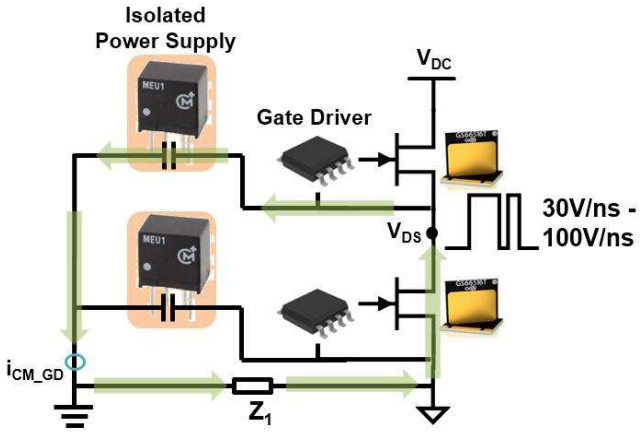


Fig. 1-3 EMI emission propagation path in the gate driver loops

C. Increased EMI noise in power loop

Another challenge brought by the high dv/dt is the EMI generated in the power loop, which is effectively increased as the switching frequency and commutation speed increase. Specifically, it was found in [11] that with SiC devices the voltage spectrum in double-pulse tests increased by 10 dB at frequencies above 1 MHz when compared to Si devices due to the higher dv/dt slew rates. Similarly, in a SiC-based flyback converter the EMI noise was shown to increase by 20 dB in the 5–20 MHz range [12]. In SiC-based motor drives switching with voltage slew rates higher than 40 V/ns, the common mode (CM) and differential mode (DM) EMI noise were found to be 30 dB larger than those in Si-based converters switching at the same switching frequency but with lower voltage slew rate [13]. The overarching effect is that the higher the switching frequency and voltage slew rate are, the higher will be the CM and DM EMI emissions generated above the first switching frequency harmonic component [14][15]. As a result of the increasing EMI noise, the EMI filter may suffer from a large volume and it can decrease the converter power density. It deserves to explore the switching frequency effect on the CM and DM EMI emission in a GaN-based converter and assess the impact from the high switching frequency operation on the EMI filter design.

Besides the effect from the high switching frequency, it is also necessary to reduce the turn-off V_{ds} overshoot to attenuate the EMI emission at very high frequency range (10 MHz – 100 MHz). To achieve this, a smaller power loop inductance is needed. To address this, the common way is to use the overlapped PCB top and bottom layer (or internal layer) to attain magnetic flux cancellation within the power loop [16]-[20]. In [16]-[18], both the high and low side transistors locate on the top layer. In [19][20] the high and low side devices are back to back on the top and bottom layer separately, saving 50% footprint compared with the previous solution.

D. Critical thermal design

The thermal management of 650V e-mode GaN HEMTs in question is also a challenge due to its small topside thermal pad, addressed in[16]-[20] . In [17][18], the heat sink was mounted on the top of the devices with an insulation layer as an interface. To further force the heat sink to the device thermal pad to reduce the contact thermal resistance, several screws were used for connection from the heat sink to the PCB [17][18]. The thermal solution of the double-side power loop in [19][20] is limited due to their utilization of the old generation of GaN HEMTs. Nonetheless, a large heat sink was used in [16]-[20] to dissipate the heat, thus reducing the converter power density. To this end, a general approach to design the heat sink size or its thermal resistance is needed to fully utilize its volume and control device temperature.

E. Paralleling GaN devices

Paralleling devices is a common approach in the high current application to reduce the conduction loss. In a 12-to-1 V GaN-based point of load (POL) converter with 2.5 – 30 A load current, the efficiency improved by 8% at 30 A load current by paralleling devices [20]. To effectively parallel devices, the current balance is expected in the steady state and the switching transient. Thanks to the positive-temperature-coefficient on-resistance of the device in question, the current is equally shared among the devices at the steady state. The dynamic current balance during turn-on and turn-off transient is highly dependent on the parasitic inductances within the gate and power loops [22][23]. It was found out in [23] that the GaN FET with the smaller gate loop would turn on first giving rise to a higher current overshoot compared with the other device in parallel. To this end, the loop inductances of the paralleled GaN HEMTs are not only required minimization but also symmetry so that the effects from the parasitic inductances on the transient waveforms are the same for the two GaN devices. To

address this problem, [23] proposed a symmetric power loop and gate loop design to parallel four low voltage e-mode GaN FETs, where the gate drive is located in the center of four power switches to maintain the symmetry. To parallel 650 V GaN devices in question, a minimized power loop layout (30 mm x 40 mm) for four HEMTs was proposed in [24][25]. In this design, a 4.55 Ω turn-on gate resistor was adopted to attenuate the oscillation within the gate loop, whose loop inductance is large to the distributed layout of the HEMTs, nonetheless, limiting the turn-on speed. A more compact layout to parallel the devices in question is needed.

The gate oscillation under paralleling operation was observed and analyzed with Si MOSFETs [26], cascode GaN transistors [27]-[30] and e-mode GaN HEMTs [31]-[33]. This issue was initially addressed in [26], which stated that the origin of the oscillation was a potential right-half-plant (RHP) pole within the commutation loop, related to gate, power loop parasitic inductors, the gate resistors, the device parasitic capacitors and the device transient transconductance g_m in the saturation region. A larger g_m, corresponding to a high di/dt, leads to a larger gate oscillation during paralleling operation [26]. Therefore, the GaN devices suffer from a larger gate oscillation under paralleling operation compared with Si devices [28]. In [29], a ferrite bead, whose dc resistance is zero and 120 Ω at 100 MHz, was used in series with the gate resistor to attenuate the high frequency gate oscillation for paralleled cascade GaN devices. To attenuate the observed gate oscillation for the paralleled e-mode 650V GaN devices, the common way is to add a split gate resistor between the common on-resistor and each device gate [24][25][31]-[33]. The resistance combination of the split gate resistor and the common on-resistor was found in [33] to have a significant impact on the gate oscillation when two GaN HEMTs in question are paralleled. Given that the limited spice model from the manufacture cannot capture the oscillation observed, a circuit model is needed here to analyze

the origin of the oscillation, its propagation path and assess effects from the passive components within the commutation loop.

1.2.2 Gate drive power supply design for GaN

Generally, in order to have a small isolation capacitance in the isolated power supply, the distance between the primary and secondary sides of the transformer in question should be as large as possible. As a result, the power supply would suffer from low power density. Table 1-4 lists the isolation capacitance, the typical efficiency, and the volume of 2 W state-of-the-art isolated power supplies recently developed at universities and industry. The input voltages of the listed converters range from 5–15 V, and the output voltages are within 5–7 V. In Table 1-4, [34] has an ultra-low isolation capacitance, but also a large volume or a low power density with a high switching frequency. From the comparison among [35]–[38], it is found that the power supplies with isolation capacitances smaller than 10 pF have a power density less than 13.7 W/in3. This represents one of the key challenges tackled in this work; namely how to minimize the effect of this tradeoff to attain both an ultra-low isolation capacitance and high power density in gate-drive power supplies for GaN power semiconductors.

Table 1-4 State-of-the-art 2 W isolated power supply characteristics

Reference	[34]	[35]	[36]	[37]	[38]
Part No.	Ampere Lab	SC02S1205A	MEJ2S0509SC	R05P205S	LTM8068
Output No.	2	1	1	1	1
Switching frequency /Hz	1.2M	80k	45k	50k	250k
Isolation capacitance /pF	0.9	15	4	1.5 ~ 10	13.5
Efficiency	75%	82%	76%	73%	70%
Size/mm	23 x18 x2.8	19.6x10.5x7.2	19.6 x12.6x10	19.5 x12.5x9.8	11.3 x9 x4.9
Power density/ W/in^3	26.7	22.11	13.2	13.7	59
Isolation voltage	--	1kVdc	5.2kVdc	6.4kVdc	2kVac

Reference	[34]	[35]	[36]	[37]	[38]
Temperature/℃	200	100	85	95	125

Besides the above tradeoff, efficiency is also a key design variable affected by the power supply volume. For instance, though [35] achieved a higher efficiency than [38], while both featured comparable isolation capacitances, the former had a larger volume than the latter. In general, to achieve high efficiency and simultaneously high power density, high switching frequency operation is essential in order to reduce the size, and consequently the losses, of all passive components. Then, to counteract the resultant increase in losses due to the higher switching frequency operation, a soft-switching technique can be adopted, at the expense of a limited selection of power converter topologies. Consequently, all these tradeoffs must be judiciously handled throughout the entire design process.

Further, the printed-circuit-board (PCB) -embedded technique has been demonstrated to be an effective way to increase the integration level of power converters. PCB is a widely-used and low-cost substrate in the converter design, which can be manufactured based on a standard lamination process. Thanks to it, the converter can be fabricated following an automated and high-volume production process. Though the PCB is thin, there is still space to embed some components seeking to reduce the total converter size. As example, a transformer with an air core was implemented into a PCB in [39] for a 27.14 MHz resonant LLC-type converter. In [40][41], a low temperature cofired ceramic (LTCC) inductor was embedded into a PCB, which also doubled as a substrate for a point-of-load (POL) converter, increasing the power density to 800 W/in^3. A comparative 2 W gate driver power supply design in [34][42] succeeded embedding the UI-shape magnetic ferrite core and copper-trace windings into the PCB, which verified the feasibility of building a complex transformer structure within a PCB using a

standard lamination process. Furthermore, the dies of the Si insulated-gate bipolar transistor (IGBT) and diode were also embedded into a PCB in [43][44]. It was found in [43] that the thermal resistance of the PCB-embedded devices was reduced by 30–44 % compared with the traditional method and the insulation strength of the PCB-embedded module could be as high as 41–50 kVrms/mm. Ref. [44] explained the detailed die-embedding process. In [45], an investigation concerning the failure of PCB-embedded electrical components and electronics was presented, analyzing and predicting the main phenomenon observed, namely the crack initiation propagation within the PCB-embedded structure. Lastly, seeking to extend the application range of the isolated power supply, [42][46] evaluated the feasibility of operating at ambient temperatures of up to 200 °C, focusing on possible reliability effects of the PCB-embedded transformer. Along these lines, a novel PCB-embedded transformer structure is investigated in this dissertation seeking to achieve the maximum possible power density for the gate-driver power supply at hand.

1.2.3 Motor drive design using GaN (hard-switched topology)

As above discussed, GaN HEMTs have been widely used in the power converter design thanks to their distinct advantages over Si devices, such as higher switching speed, lower switching loss, lower reverse recovery loss and high switching frequency. Thanks to these advantages, the power converter using GaN devices can achieve high power density and simultaneously high efficiency. For example, in the application of the energy storage system, a 1 kW bidirectional DC-DC converter achieved at least 1% higher efficiency increase by replacing Si to GaN devices [47]. In the motor drive application, it was found that a higher switching frequency with GaN HEMTs could reduce the motor loss in the high-speed

permanent-magnet electric machine [48] and increase the light load efficiency of the motor drive [49].

To design a compact three-phase inverter using the GaN HEMTs in question, the potential challenges has been explored in Section 1.2.1, including the sensitive gate and power loop, and critical thermal management. Within on this existed solutions, the highest switching frequency of a GaN-based three phase inverter in question can be as high as 100 kHz [17][18][20].

In what regards to the two level three-phase inverter, it deserves to come up with a comprehensive study on the assessment of the switching frequency effect on its efficiency, power density and conducted electromagnetic interference noise (EMI). Several literatures have already studied the switching frequency effect on the inverter loss and the inverter EMI noise, with WBG devices. If the switching frequency increases by 10 times, the common mode (CM) and differential mode (DM) EMI noise were 20dB higher above MHz [15]. Resultantly, the output CM chokes for motor drives can be 20 times heavier [50]. However, the increasing switching frequency reduces volt-second across the magnetic components, which brings potential reduction on magnetic components [14]. Reference [51] found out that a high dv/dt reduced the switching loss but increased CM EMI noise on a GaN-based boost converter.

The interest of the research here is to build a compact GaN-based three-phase inverter, including the half bridge design with ultra-low power loop inductance and standard double-side thermal solution. It also deserves to come up with a comprehensive study on the assessment of the switching frequency effects on the two-level three-phase inverter performance, including losses, efficiency, heat sink volume, CM/DM EMI emissions, and corresponding EMI filter design.

1.2.4 Active gate driver design for GaN-based inverter

Active gate control technique is developed to provide a solution to change dv/dt or di/dt slew rate [47]-[59], to reduce voltage overshoot during turn off transient [53][60], to render the gate voltage within safe operating area (SOA), to reduce delay time [54]-[56], and to reduce EMI noise resulting from the high dv/dt slew rate [61], in the hard-switching power converters with the Si switching devices like MOSFET and insulated-gate bipolar transistor (IGBT). A larger gate resistance can also contribute the former three advantages but increase the delay time, which suppresses the highest switching frequency and produces higher total harmonic distortion (THD). To this end, the large gate resistor is not considered in terms of EMI reduction due to the dramatically increase of switching loss with few benefit of EMI reduction. As a comparison, in [61], it was proved that active dv/dt control is an effective tool to reduce CM EMI with less penalty of the switching loss. In [61] the active gate driver attenuated the CM EMI noise by 5 dB ~ 10 dB in the several megahertz range with only 4% power loss increase in Si-based setup.

In order to pursue different targets of active gate driver, there exist different gate drive structures or circuits to control the gate charge during turn-on and turn-off transient of Si device, such as changing equivalent gate resistor in two values [54][60][62], close loop feedback to find voltage change transient [55][56][59][63], 2-step or 3-step gate voltage [57], and injecting extra current into gate [58]. In [64]-[67], the gate control techniques for SiC JFET and MOSFET have been developed. However, there is no papers proposing an effective dv/dt control method for the GaN devices. The challenge to control gate charge of GaN devices is how to make the control fast enough to capture the transient within in 10 ns. Besides, the GaN HEMT in question has a very limited gate voltage SOA, requiring a careful gate loop

design within the active gate driver. To this end, another challenge of the work is to suppress the spike at the device gate under 10 V or lower. Therefore, the active gate driver for the GaN in question is expected to be built in a simple circuit with a few transistors, whose delay, response time and effect from PCB layout can be minimized.

1.2.5 LLC resonant converter design using GaN HEMTs (Soft-switching topology)

Due to the concerns regarding the increasing fuel cost and air pollution, plug-in electrical vehicle (PEV) or plug-in hybrid electrical vehicle (PHEV) become a promising trend. The on-board charger is the interface between the PEV or PHEV battery bank and an external electrical source. The most commonly used structure for the on board charger consists of two stages, AC/DC converter with power factor correction (PFC) followed by an isolated DC/DC converter featuring isolation and regulation. For PFC stage, bridgeless PFC has significant advantages thanks to its elimination of the diode bridge and reduced conduction loss accordingly [68][69]. Among bridgeless PFC, the totem-pole PFC is the most simplified topology, featuring the minimum number of the switches [70]-[72]. To eliminate the tremendous turn-on loss in the bridgeless totem-pole PFC in the continuous-current mode (CCM) [73], the critical-current mode (CRM) was proposed and reported in [74]-[77]. With the CRM, zero-voltage switching (ZVS) (turn-on) can be achieved for the main switches with the elimination of the turn-on loss, rendering it a very efficient operation mode for PFC using WBG devices with a high switching frequency. As a trade-off of the benefits, the CRM generates a large current ripple, increasing the conduction losses and requiring a large filter volume. To tackle this issue, the interleaved multi-channel PFC can be adopted [75]-[78]. For isolated DC/DC converter, LLC or CLLC resonant converter has been widely used with high switching frequency thanks to its ability to achieve soft switching for all the switches to full

load conditions elimination the turn-on loss [79]- [83]. While the primary side device can switching with ZVS, the secondary side synchronous rectifiers (SRs) achieve zero-current switching (ZCS). Furthermore the soft-switched operation also helps the EMI reduction [82]. Compared with other soft-switching PWM converter, for example, dual active bridge (DAB), the LLC or CLLC resonant converter has slightly higher rms current but a much smaller turm-off current, rendering a much lower switching loss [83]. In the commercial products of 5- 10 kW on-board charger design [84][85], the switching frequency with Si devices is around 10 - 100 kHz, which is highlighted in Fig. 1-4, resulting in low power density. In [85], with adoption of the Si MOSFET, the charger utilized the CRM totem-pole PFC and LLC resonant converter and achieved 96.3 % total efficiency. However due to the limitation of the Si MOSFET switching speed, the switching frequency in [85] is 50 kHz and the converter power density is thus low.

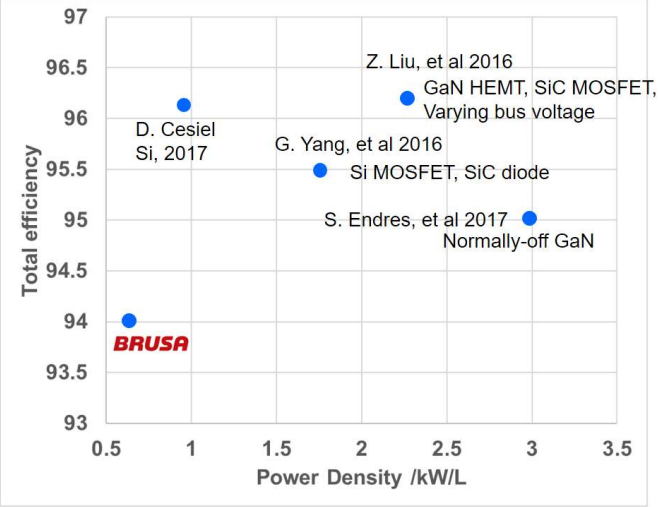


Fig. 1-4 State-of-the-art 5-10 kW on-board charger design

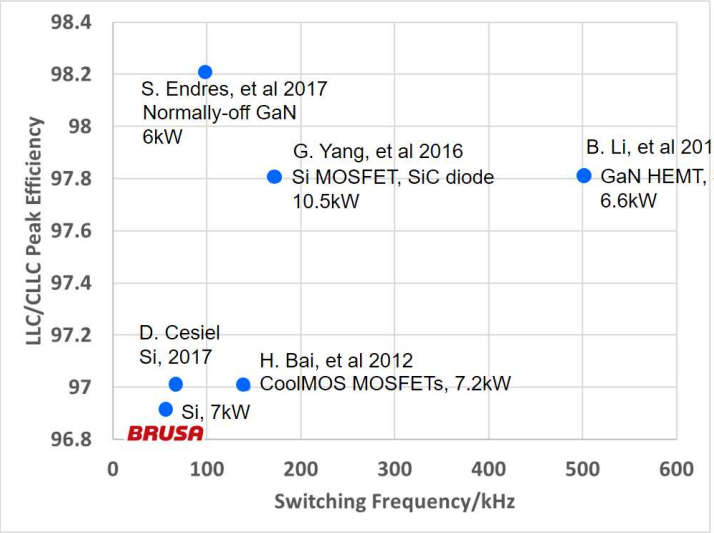


Fig. 1-5 State-of-the-art DC/DC stage performance for on-board charger

Fig. 1-4 shows the comparison on the power density and efficiency of Si-based design [84][85] and the approaches using normally-off GaN transistors [86], or SiC diode [87], or GaN HEMTs combined with SiC MOSFET [77][88]. The switching frequency and the peak efficiency of the DC/DC stage are compared in Fig. 1-5 [84]-[89]. It is observed that with adoption of the WBG devices, the converter design for on-board charger application can operate under high switching frequency (> 100 kHz), achieving a high power density and high efficiency as well [83][86] - [91].

Within the design of the isolated DC/DC stage, the transformer plays an important role in terms of the efficiency and power density. Litz-wire is an essential tool enabling low-resistance high-current transformer winding up to hundreds of kHz [92]. Ref. [92]- [94] have discussed and developed an appropriate way to apply litz-wire effectively, such as, selection on strand diameter, bundle construction, air-gap effect and simplified loss estimation. The core loss estimation with sinusoidal and non-sinusoidal excitation were explored in [95]- [97]. The common construction of a litz-wire transformer is to use an EQ or ER core such as the examples in [92][98][99]. Ref. [88] utilized the center leg of the E core to control the transformer leakage

inductor so that the leakage inductor can be used as the resonant inductor in the LLC resonant converter.

The interest of the research here is to design a 10 kW LLC resonant converter to evaluate the performance of GaN HEMTs under soft-switching operation. The first challenge here is to build a half-bridge switching cell using paralleled GaN HEMTs with a high current conduction capability and its adaptive thermal solution. The second challenge is to build a litz-wire transformer suitable for high switching frequency operation, requiring the optimization among the transformer loss, device loss, and converter volume as well.

1.3 Contributions and accomplishments

As described in this chapter, to adopt the e-mode GaN HEMT in question to achieve the high efficiency and high power density in the power converters, there are various high-frequency oriented challenges, including narrow gate operating range, increased EMI emissions in the gate loop and power loop and critical thermal management. These issues exacerbate the difficulty to parallel GaN HEMTs to increase current conduction capability and further reduce on-resistance.

To attenuate the increased EMI emissions in the gate loops as described in Section 1.2.2, an integrated, dual-output gate drive power supply is proposed for the 650 V, 60 A, GaN half-bridge phase-legs, rated at 2 W (2 × 1 W), 15 V to 2 × 7 V, featuring an ultra-low isolation capacitance of 1.6 pF, an output-to-output parasitic capacitance of 1.6 pF, a power density of 72 W/in3, and an efficiency of 85 %. All this is attained using an active-clamp flyback converter switching at 1 MHz using 65 V GaN HEMT devices and Schottky output rectifiers, and a Pareto-optimized transformer design minimizing its interwinding capacitances, volume, and losses. Lastly, the transformer is fully embedded in PCB material, doubling as substrate

for the topside active layer of the power supply, contributing the impressive high power density compared the state of the art. The EMI emission in the gate loop using the proposed power supply to drive the 650 V/60 A GaN phase leg is measured to be 3dB smaller than the state-of-the-art power supply, which features an ultra-low 3.9 pF isolation capacitance. Furthermore, the reliability impact of the magnetic-PCB material interface in high ambient temperature (200 ˚C) is also evaluated. It is found that the difference of the coefficient of thermal extension between the PCB and the magnetic material has to be minimized to secure the complete magnetic structure in the high temperature operation.

To adopt the GaN HEMT in question in the hard-switching topology such as the three-phase two level inverter, the guidelines to minimize the parasitic inductance in the gate and power loop in the PCB layout are provided. The corresponding thermal management of the vertical power loop is also illustrated with the design consideration and the standard thermal resistance evaluation method. A modular GaN half bridge is built then, based on which a 116 W/in^3 1 kW 400 Vdc inverter is assembled with the ability to work with 500 kHz switching frequency. With the design approach, the switching frequency effects on the two-level three-phase inverter performance are assessed, including losses, efficiency, heat sink volume, CM/DM EMI and the EMI filter volume. It is found that the inverter loss increases significantly with a higher switching frequency, leading to a lower efficiency and a large heat sink volume (air-cooling). It is further observed that with a higher switching frequency, both the CM and DM EMI emissions increase in the range from 1 MHz to 30 MHz. From the switching frequency harmonic to 1 MHz, the CM EMI increases while the DM EMI decrease. The trend in the frequency range is due to the nature of the propagation impedance, which is inductive for DM and capacitive for CM. As a result of the trend, the DM output filter volume can be reduced while the CM filter volume increases.

To attenuate the increased CM EMI emission in the GaN-based inverter above 10 MHz, a novel active dv/dt control circuit is proposed, featuring a fast response to change the 650 V GaN HEMT turn-off and turn-on dv/dt slew rate freely and independently while the converter is running. With the proposed control circuit, the dv/dt can be varied from 8.7 V/ns to 27.1 V/ns during turn-on and from 7.6 V/ns to 34.7 V/ns during turn-off. Compared with the state-of-the-art active gate driver for Si and SiC devices, the proposed circuit cannot only slow down the dv/dt but also owns the ability to speed up the dv/dt, with even less components. Due to the sensitive gate operation of the 650 V GaN HEMT, there is observed a large oscillation at the gate induced by the extra added miller capacitors in the circuit. To attenuate the oscillation, a damping resistor is necessary to put in series with the extra miller capacitor to ensure the gate voltage within 7 V.

With the solutions developed to address the high-frequency oriented issues to adopt the single 650 V GaN HEMT, the approach to parallel two and four HEMTs is proposed then. The PCB layout featuring the symmetric and minimized the gate loop and power loop is proposed, with which the driving resistor for turn-on and turn-off can be as small as 1 Ω. The thermal solution is also come up with for the switching cell using two and four paralleled GaN HEMTs. With the paralleled GaN HEMTs, an interesting phenomenon is observed that with the larger turn-on gate resistor the gate oscillation during turn-on is higher when the turn-off resistor is smaller. To explain it, the commutation loop during turn-on with the paralleled HEMTs is analyzed. It is found that oscillation is generated by the difference between the parasitic inductance in the gate loop and the device capacitance tolerance, which can be either damped by a larger split gate resistor (the resistor between the turn-off pin and the device gate) or bypassed through a small common on-resistor (the resistor applied between the gate driver turn-on pin and turn-off pin) to the gate driver ground (HEMT source).

With the 650 V 12.5 mΩ/6.25 mΩ switching cells designed above for high current conduction capability, a 10 kW LLC resonant converter featuring a wide output range (Gain = 1:3.3) is designed. To achieve the high power density and high efficiency, a novel litz-wire transformer integrated with a large resonant inductor for high switching frequency operation is designed. A complete model is built to estimate the inductances, the core loss and the winding loss, based on which the transformer parameters are optimized. In the design, it is found that the proximity effect dominates the AC winding loss for high switching frequency operation, which can be reduced effectively by using a litz-wire with the smaller strand diameter than half of the skin depth. As a tradeoff, the cost and complexity needs to careful consideration. To further increase the power density, a 3D assembly method is used to build the LLC resonant converter, whose power density reaches 116 W/in^3 (8 kW/l). Thanks to the optimized transformer, the switching cell with low on-resistance, low switching loss using the GaN HEMTs, the converter achieved 97.9% peak efficiency with >97% efficiency over wide output range.

1.4 Proposed Dissertation Outline

To tackle the challenges described in Section 1.2, and present the analysis and design procedures to achieve the contribution in Section 1.3, this dissertation is organized as follows.

In Chapter 2, the complete design procedures to build the integrated, dual-output gate drive power supply for the GaN half-bridge phase-leg are first presented, including the topology selection, the operation analysis of the active clamp flyback, the device selection, the transformer design and its Pareto-front-based optimization. The PCB-embedded process and the converter assembly are illustrated then. The experimental results including efficiency, isolation capacitance, power density, thermal distribution, PCB material thermal reliability in

high ambient temperature (200 ˚C) are shown afterwards. The EMI emissions propagated in the gate loop using the state-of-art power supply and the design power supply are measured and compared to demonstrate the effectiveness of the proposed design to reduce EMI emission in the gate loop.

In Chapter 3, the guidelines to build a compact 650V/60A GaN half bridge module with ultra-low power loop inductance and standard thermal solution are presented first. The inverter built with the modular phase leg is tested with 500 kHz switching frequency, whose evaluation is shown next. With this inverter, the switching frequency effects on the two-level three-phase inverter performance are assessed, including losses, efficiency, heat sink volume, CM and DM EMI. The procedure to design EMI filter using the unterminated EMI behavioral mode with optimization is illustrated based on which the effect from the switching frequency on EMI filter volume is evaluated.

Chapter 4 presents the proposed active gate driver design for the 650V GaN HEMT. First, the idea of the control dv/dt slew rate using the proposed active gate driver is illustrated. The BJT-based circuits for turn-on and turn-off dv/dt control is then presented, whose function is verified by Spice simulation. Afterwards, the detailed circuit design, including key component selection and the control source, is illustrated. With the hardware test, the gate oscillation is first observed introduced by the active control circuit. The solution to damp the oscillation is then presented. The experimental verification of the active gate driver is then presented. Finally, comparison with different gate resistors is provided, showing the proposed method has a smaller switching loss under the same dv/dt condition than using a large gate resistor.

Chapter 5 presents the solution to parallel two and four GaN HEMTs in question. First, the guidelines to design PCB layout to achieve symmetric gate and power loop using two or four

paralleled GaN are presented. Based on the layout, the adaptive thermal solution for the switching cells using paralleled GaN HEMTs is shown. The experimental results of the dynamic characteristics with different gate resistor under 400 Vdc and up to 200 A are illustrated next. The thermal resistance of the thermal solution is then evaluated based on a standard procedure. Finally, the gate oscillations observed when two HEMTs are paralleled is analyzed with a simplified equivalent circuit, based on which the effects from the passive components in the gate loop on the gate oscillation magnitude are assessed.

Chapter 6 presents the 10 kW LLC resonant converter design using the switching cell using paralleled GaN HEMTs developed in Chapter 5. First, the litz-wire transformer integrated with large resonant inductor is presented with the consideration of the core material, litz wire selection for high frequency (400 kHz) operation. To optimize the transformer volume and loss, the models of the inductance, the core loss and the winding loss are demonstrated then. The transformer optimization process is then presented with the optimization results. The experimental results of the converter are depicted in the end.

Chapter 7 summarizes the whole dissertation and lists the conclusions based on the research.

Chapter 2. Ultra-low Input-Output Capacitance PCB-Embedded Dual-Output Gate-Drive Power Supply for 650 V GaN-Based Half-Bridges

In this chapter, a gate-drive power supply is designed for 650 V, GaN HEMT devices in half-bridge configuration. Accordingly, the power supply features two isolated 7 V, 1 W outputs, feeding from a 15 V input bus. The main challenge, as described in Section 1.2.2, is to find simultaneously an appropriate design approach to achieve maximum power density, minimum isolation capacitance, and high efficiency. Accordingly, a PCB-embedded transformer structure is proposed to fully utilize the PCB substrate, whose dimensions are optimized to achieve a small transformer loss, isolation capacitance, and volume. GaN devices from EPC are selected, switching at 1 MHz. To eliminate turn-on loss to ensure high efficiency, the topology with the zero voltage switching (ZVS) is adopted. Further, the transformer operation at high temperature is evaluated conducting thermal cycling test at 200℃, showing the benefits of using high-temperature rated PCB materials.

To design the targeted gate driver power supply, this chapter presents the circuit design, including the topology selection, operation mode analysis, and active and passive component selections. The design optimization of the PCB-embedded transformer is then presented, including the core and PCB material selection. Based on the optimized dimensions, the transformer is built, and the fabrication process, including the standard lamination procedure and converter assembly, is presented. The transformer and the converter hardware are then characterized, showing the results of experimental tests conducted to verify the efficiency,

isolation voltage, isolation capacitance, total volume, EMI performance, and the impact of high temperature operation.

2.1 Circuit Design and Operation Mode Selection

2.1.1 Topology selection

As the work presented targeted isolated dc-dc conversion at very low power with high power density, the topology candidates had to be simple and fairly efficient under high switching frequency, such as the classic flyback, active-clamp flyback, and LLC resonant converters. Before the selection, one fact had to be taken into consideration that the leakage inductance in the proposed PCB-embedded transformer structure was found to be around 50 % of the magnetizing inductance. This was found in the finite element analysis (FEA) numerical calculations and verified later on by hardware measurements.

Accordingly, if the classic flyback topology were selected, critical current mode (CRM) should be used to achieve soft turn-on of the main switch [106]; however when the main switch turns off, the large leakage inductor induces a large turn-off voltage overshoot, resulting in a high turn-off loss when operating at high switching frequency. Also, the output diodes cannot turn off with zero current in the classic flyback. To solve these issues, the active-clamp flyback converter adds a clamp capacitor and a series switch as shown in Fig. 2-1, effectively clamping the voltage of the main switch S_1, and avoiding the large turn-off voltage overshoot. The clamp capacitor C_C role is to collect the leakage inductor L_r energy and release it to the secondary side while inducing a resonance with L_r and the magnetizing inductor L_m. Thanks to this resonant operation [107]–[110], S_1 and S_2 have ZVS, and the secondary diodes achieve zero-current switching (ZCS). In the simulation with the same switching devices, the active-clamp flyback has an 88 % estimated efficiency, which is 19 % higher than the classic flyback. The

LLC resonant converter is another option for the high-efficiency DC-DC converter design, which attains a 90 % estimated efficiency in simulation at full power. However, with the center-type secondary side, the two isolated outputs require four diodes and five transformer windings (one primary and four secondary windings), increasing the transformer volume significantly. If the full bridge is selected for the secondary sides, there are three transformer windings required with the eight diodes, leading to a large footprint of the circuit layer. All above is summarized in Table 2-1. In conclusion, the active-clamp flyback is finally selected thanks to its simple topology, relatively high efficiency, and small transformer size as it will be demonstrated.

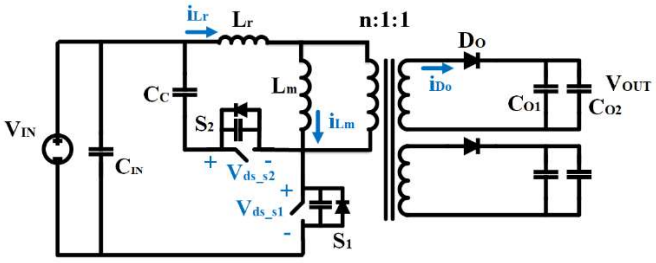


Fig. 2-1 Active-clamp flyback topology.

Table 2-1 Topology comparison summary

	Flyback	Active-clamp flyback	LLC (center-type)
Primary switch No.	1	2	2
Secondary diode No.	2	2	4
Winding No.	3	3	5
Simulated Efficiency	69%	88%	90%

2.1.2 Operating modes of the active-clamp flyback

According to the inductor operation condition, there are three operation modes, where both switches in the active-clamp flyback can achieve zero-voltage turn-on. When the magnetizing inductor L_m current is higher than zero, the active clamp flyback runs in the continuous current mode (CCM). Fig. 2-2 shows the simplified operation waveforms of the drain-source voltage of S_1 and S_2 ($V_{ds\text{-}s1}$, $V_{ds\text{-}s2}$), the leakage and magnetizing inductor current (I_{Lr}, I_{Lm}) and the output diode junction voltage and current (V_{Do}, I_{Do}) under CCM. At t_1, S_1 turns off, $V_{ds\text{-}s1}$ increase to V_{in} from t_1 to t_2. At the same time, the output capacitance C_{oss} of S_2 can be discharged by the L_m, before S_2 turns on. To this end, S_2 achieves ZVS. After S_1 turns off at t_2, L_m discharges and L_r is resonant with C_c. When $i_{Lr} > 0$, C_c is charging. C_c starts to discharge when i_{Lr} becomes smaller than zero. When S_2 turns off at t_4, the i_{Lr} starts to discharge C_{s2}. At t_4, i_{Do} is not zero but at its maximum value. Therefore during $t_4 \sim t_0$, the secondary current needs to charge the diode junction capacitor C_{Do}. S_1 can achieve soft-turn-on if the energy in the leakage inductor is larger than the energy stored in the output capacitance of S_1 and D_o. If the leakage inductance is small, the soft-switching of S_1 is lost at light load condition, or high input voltage condition. In this way, the leakage inductor is expected to be relatively large when the active clamp flyback runs in CCM.

Once the leakage inductor is small due to the transformer (coupled inductor) design, the active clamp flyback cannot operate in CCM with ZVS in the all conditions, L_m can run with the critical current mode (CRM), whose current drops below zero before S_1 turns on. The simplified operation waveforms of the switches and the diode are shown in Fig. 2-3. The key difference between CRM and CCM is the magnetizing current at t4, when the former is negative to help L_r to discharge the output capacitance of S_1 and D_o. Therefore the condition

for S_1 to achieve ZVS in CRM is that energy in L_m and L_r is larger than the energy stored in the output capacitance of S_1 and D_o. In CCM and CRM, the resonant capacitor C_c is chosen to be a large value that the resonant time between C_c and L_m, and between C_c and L_r is larger than S_1 off time. Therefore, the waveforms of i_{Lm} and i_{Lr} is close to the triangle waveforms instead of the sinusoidal waveforms.

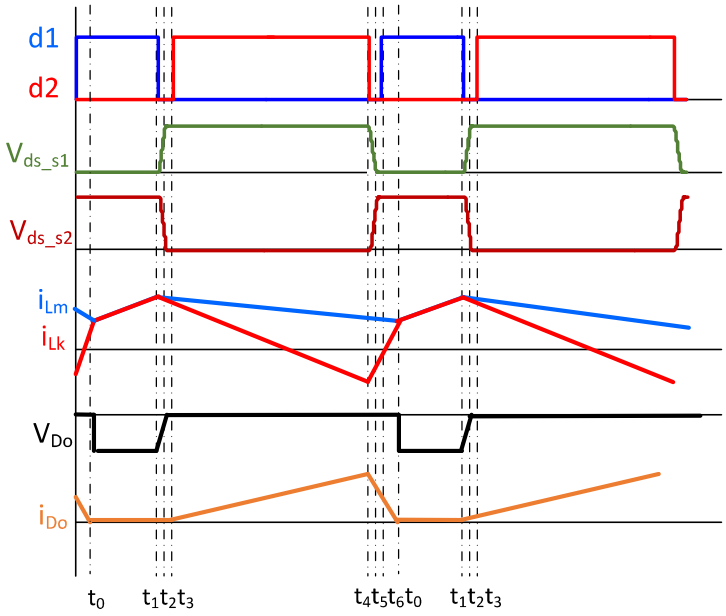


Fig. 2-2 Operation of continuous current mode of the active clamp flyback

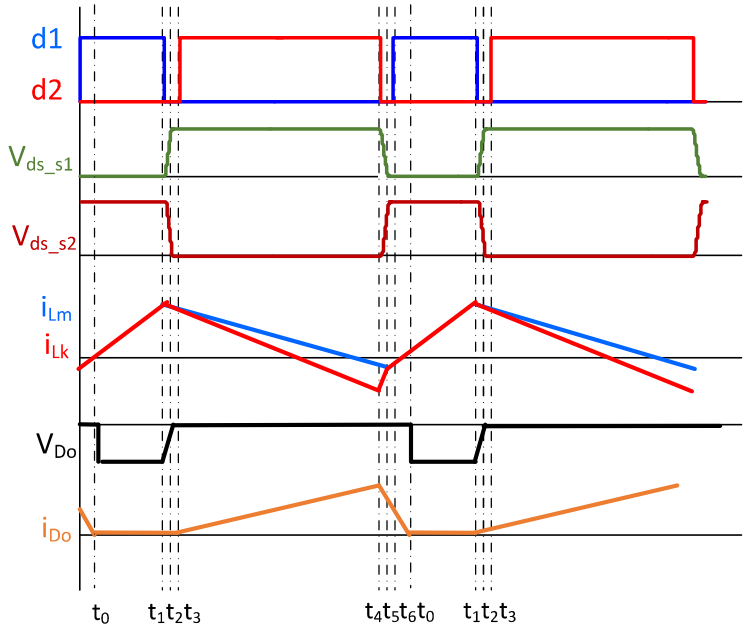


Fig. 2-3 Operation of critical current mode of the active clamp flyback

The third way to perform soft switching in the active-clamp flyback is the resonant operating mode, explained in detail in [107][108] and illustrated in Fig. 2-4. According to [107], the transformer first works in CRM. Before S_1 turns on at t_0, the negative current in the magnetizing inductor can discharge the S_1 junction capacitor during t_5–t_6, with which the soft turn-on of S_1 is achieved. When S_1 is turned off at t_1, L_r and L_m discharge the junction capacitor of S_2 during t_1–t_2, before it turns on at t_3, with which S_2 achieves zero-voltage turn-on. During t_2–t_5, C_C resonates with L_m and L_r before t_4, and solely with L_r after t_4. At the instant that S_2 turns off at t_5, L_r has almost the same current as L_m and the secondary side current is almost zero. As a result, the secondary side diodes achieve zero-current turn-off. To this end, the resonant operating mode is selected to build the power supply to reduce the high frequency oscillation at the output and the output diode.

The main characteristics and the comparison among the three different modes are listed in Table 2-2. The main advantages of CCM is a smaller current ripple, compared with CRM and

the resonant mode, leading to a smaller conduction loss in the switches and the inductors. However, it requires a large leakage inductor to maintain ZVS for the switches for the different load condition. An alternative way is to add a discrete inductor in series with the primary inductor, which increases component number and footprint, but also induces extra losses in the power supply. To this end, CRM has an advantage that it have no requirement on the leakage inductor. With a proper selection of the resonant capacitor, the CRM can operate into the resonant mode to further achieve ZCS for the output diode. The rms loss during the period S1 is off is slightly higher in the resonant operating mode than in CRM.

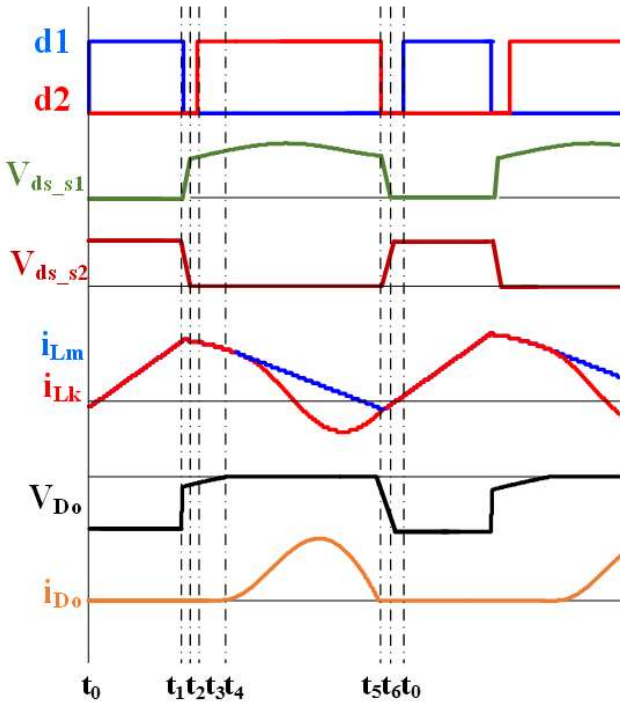


Fig. 2-4 Resonant operation mode in active-clamp flyback.

Table 2-2 Comparison among three operation modes of the active-clamp flyback

	CCM	CRM	Resonant mode
L_m current	>0 all the time	<0 before S1 turns on	<0 before S1 turns on
L_r value	large	No requirement	No requirement

Inductor ripple	Small	Large	Large
Rms current	Small	Mid	Large
Diode ZCS	No	No	Yes

2.1.3 Circuit design

According to the circuit analysis in the resonant operating mode, the negative magnetizing inductor current $|i_{Lr}(t_5)|$, at the moment S_2 turns off, is calculated with (2.1) to be smaller than –0.2 A in order for S_1 to achieve ZVS; where $C_{S1/2}$, t_{DT}, n, V_{IN}, and V_{OUT} are, respectively, the junction capacitor of S_1 and S_2, the dead time between S_1 and S_2, the turns ratio of the transformer, the input voltage and the output voltage. In (2.1), $C_{S1/2}$ is estimated as 20 pF, t_{DT} takes 25 ns, and n is 1. If the turns ratio n is larger than 1, the corresponding $|i_{Lr}(t_5)|$ is smaller than 0.2 A so that '$|i_{Lr}(t_5)| = 0.2A$' is also an appropriate estimation for n larger than 1.

The corresponding maximum magnetizing inductance L_m needed is calculated to be 6 μH according to (2.2) [107], where L_r, L_m, P, D, and f are respectively the leakage inductance, the magnetizing inductance, the total output power, the duty ratio, and the switching frequency. The switching frequency of the design is fixed to 1 MHz due to the high temperature limits of the switch module from [34].

$$|i_{Lr}(t_5)| \geq 2C_{S1/2}\frac{V_{IN}+\frac{V_{OUT}}{n}}{t_{DT}} \tag{2.1}$$

$$L_m = \frac{V_{IN}\frac{D^2}{f^2} - 2L_r\left(\frac{P}{V_{IN}f} + |i_{Lr}(t_5)|\frac{D}{f}\right)}{\left(\frac{P}{V_{IN}f} + |i_{Lr}(t_5)|\frac{D}{f}\right)} \tag{2.2}$$

According to (2.1)(2.2), the magnetizing inductance should be smaller than 6 μH. The clamp capacitor can be selected after the leakage inductance is finalized after the transformer fabrication. If L_r is around 2 μH, the clamp capacitor can be selected to be 10 nF in order to achieve ZCS for the diodes.

With the selected L_m and C_C, the two switches S_1 and S_2, and the output diodes can be selected based on the estimated rms current, the turn-off transient current and voltage, and the maximum voltage during the resonant operation.

In consideration of a small total switch loss, including the turn-off loss and conduction loss, S_1 and S_2 utilize EPC GaN devices. The maximum voltage of the two devices is simulated to be less than 30 V, considering there could be 1 nH power loop parasitic inductance. The devices with 60–80 V maximum junction voltage are selected. The estimated loss using the selected devices for S_1 is listed in Table 2-3. From Table 2-3, the device EPC8009 has the smallest total loss thanks to its small on-resistance and small output capacitor, compared with other candidates. To this end, EPC8009 is selected for S_1. A similar loss estimation is performed for S_2 and its results are summarized in Table 2-4, based on which the device EPC8009 is selected for S_2.

Table 2-3 S_1 candidate loss estimation

Part Number	Vds /V	Rds(on) /mΩ	Id /A	Qoss/ nC	Loss/mW		
					Conduction	Turn-off	Total
EPC2020	60	2	60	50	0.84	372.41	373.26
EPC8009	65	130	2.7	0.94	54.76	8.34	63.09
EPC8002	65	530	2	0.344	223.24	2.16	225.40
EPC2021	80	2.5	60	63	1.05	496.55	497.61

Table 2-4 S_2 candidate loss estimation

Part Number	Vds /V	Rds(on) /mΩ	Id /A	Qoss/ nC	Loss/mW		
					Conduction	Turn-off	Total
EPC2020	60	2	60	50	0.58	330.19	330.77
EPC8009	65	130	2.7	0.94	37.77	7.39	45.16
EPC8002	65	530	2	0.344	153.98	1.92	155.89

Furthermore, the Si Schottky diode STPS0560Z is selected as output diode. The gate drives for S_1 and S_2 use the highly integrated chip LM5113, where the bootstrap circuit is embedded to drive the high-side switch S_2. The input and output capacitors are also selected based on the ripple requirements. The summary of the component selections is presented in Table 2-5.

Table 2-5 Component list

S_1	EPC8009	**C_c**	10 nF (0603)
S_2	EPC8009	**C_{o1}**	10 μF (0603)
D_o	STPS0560Z	**C_{o2}**	0.33 μF (0402)
Gate drive	LM5113	**C_{in}**	10 μF (0603)

2.2 PCB-Embedded Transformer Design and Optimization

2.2.1 PCB-embedded transformer structure

The proposed transformer structure is shown in Fig. 2-5 and Fig. 2-6, where the toroidal core is shown in black color and the three windings—one primary and two secondary sides—are wound around the core symmetrically. The top and bottom sides of the windings as laid out as PCB traces, whereas the vertical connection between the top and bottom turns are constructed using vias. There are six vias with longer length above the transformer, which are

used to connect the transformer to the circuit layer. The material surrounding the transformer is the PCB. In order to increase the isolation voltage among the windings, PCB material covers the top and bottom PCB traces as well, which is illustrated clearly in the front view ofFig. 2-6. The air gap locates in the middle of the two secondary windings, as shown in the top view of Fig. 2-6. This ensures the symmetric inductance and the balanced output voltage for the two output channels. Besides, the air gap is placed far from the windings to avoid any fringing effect and reduce the ac winding loss. In the structure, only one air gap is allowed because two or more air gaps would separate the core into several pieces. This multi-piece core structure would require the precise horizontal alignment of the pieces during the lamination process, complicating the manufacturing process significantly.

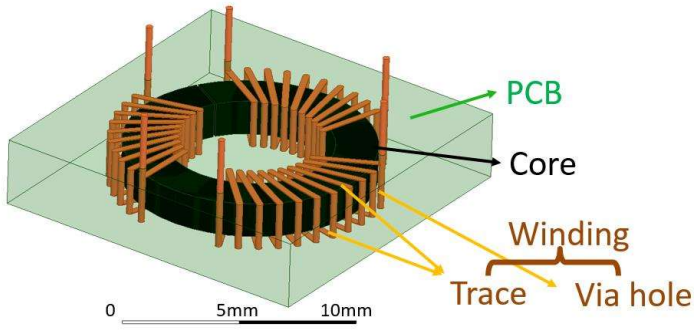


Fig. 2-5 PCB-embedded transformer structure illustration.

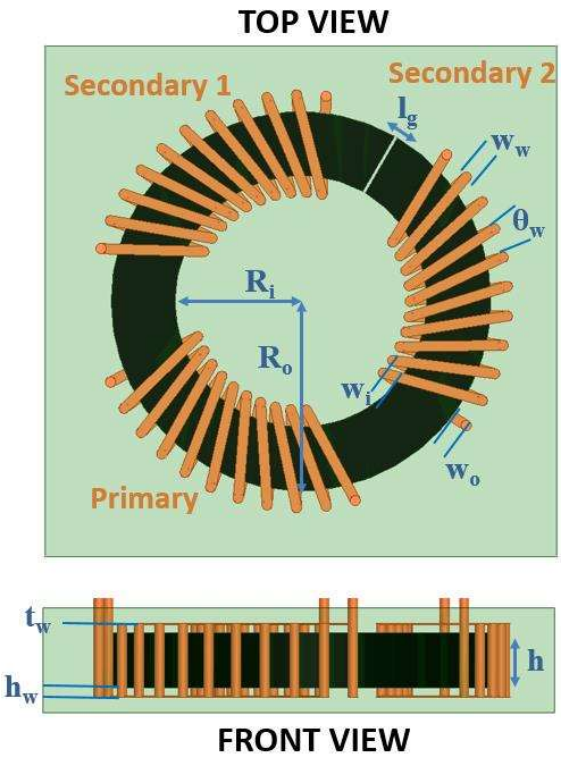


Fig. 2-6 Top and front view of the PCB-embedded transformer

In addition, the leakage inductance of the transformer would increase even more exceeding the already high 50 % of the total inductance. The large leakage is the result of the loose structure of the windings. For example, the part of the magnetic flux generated by the outer via-holes goes into the surrounding PCB material, instead of circulating in the core. If there is a need to reduce the leakage inductance, the winding structure would have to be changed, for instance, flat and wide traces instead of the wire-type traces. The leakage value here, however, is not a problem. On the contrary, it is needed to ensure soft switching for S_1 for all operating condition.

In terms of the core material selection, the core material chosen is P61 from ACME, whose Curie temperature is 280 °C and the core loss coefficient is 150 kW/m^3 at 50 mT, 100 °C, 1 MHz. The core loss coefficient of P61 is lower compared with other commercial MnZn ferrite

materials [110]. The highest temperature during the standard PCB lamination process is 190℃, and the highest operating temperature is 200 °C, both of which are safely within the capabilities of the material in question, eliminating the risk of possibly affecting its magnetic properties.

Two different PCB materials were selected, one for standard temperature range applications (< 100 °C), and one for 200 °C applications. FR4 is a low-cost commonly-used PCB material suitable for the first case, and as such was selected to test with the structure in room temperature. However at 200°C, FR4 has delamination problems. The coefficient of thermal expansion (CTE) of FR4 is 70 ppm/°C, large enough that it could break the ferrite core at 200°C. To this end, MEGTRON2 (R-1577) from Panasonic is a better option to build the high temperature version, which has a smaller CTE of 34 ppm/°C.

The winding trace material is copper, whose thickness can be selected either 1 oz or 2 oz. 2 oz copper can reduce the winding conduction loss thanks to a smaller DC resistance, however it increases the clearance distance between two turns. 1 oz copper clearance is 10 mil (0.254 mm) according to the PCB manufacture requirements, and 2 oz clearance is twice of that of 1 oz. Assuming 10 turns are used in one winding, 2 oz copper has at least 100 mil (2.54 mm) wider windings than 1 oz copper. If the core size is fixed, a wider winding leads to a larger isolation capacitance due to the closer distance between the windings. If the same isolation capacitance is expected, the core with 2 oz copper winding should accordingly have a larger radius than that with 1 oz copper winding. As a result, in the consideration of the minimum transformer volume and isolation capacitance, 1 oz copper is preferred. Accordingly the thickness of the copper trace t_w is fixed to be 0.0356 mm.

Table 2-6 Dimensions of the PCB-embedded Transformer

	Description	Optimized Value
R_i/mm	Core inner radius	3.7
R_o/mm	Core outer radius	5.65
h/mm	Core thickness	1.8
l_g/mm	Air gap width	0.1
w_w/mm	Turn width	0.2
w_i/mm	Space between winding and core at inner circle	0.5
w_o/mm	Space between winding and core at outer circle	0.5
h_w/mm	Space between winding and core in the vertical direction	0.1
$\vartheta_w/degree$	Angle between turns	2.86
t_w/mm	Winding copper thickness	0.0343
N	Turn number	10

The parameters defining the winding and core dimensions are illustrated in Fig. 2-6 and are described in Table 2-6. Specifically, the core has four dimensions: the inner radius R_i, the outer radius R_o, the thickness h, and the air gap length l_g. As for the windings, the trace width w_w, thickness t_w, the turn number N and the angles between two turns θ_w are used to describe them. The angles between two turns θ_w is directly related to the clearance distance between the neighbor inner vias w_m, the inner radius of the core R_i, and the via diameter w_w as shown in (2.3). In order to quantify the space between the winding and the core, h_w, w_o, and w_i describe respectively the space from the core to the top or bottom layer copper trace, to the inner via-holes and to the outer via-hole. These three parameters are limited by the PCB manufacturing ability. If w_i, and w_o are too small, the via-holes may hit and break the core during the

fabrication. On the contrary, large w_i and w_o result in a large leakage inductance for the transformer. h_w is fixed due to the smallest PCB laminate layer thickness of the selected PCB material. In this design, w_i and w_o are fixed to be 0.5 mm, and h_w is fixed to be 0.1 mm.

$$\theta_w = \arctan\left(\frac{w_m / 2}{R_i - w_i - w_w / 2}\right) \tag{2.3}$$

2.2.2 Transformer model and optimization

There are three targets the transformer optimization focuses on: the transformer volume V, the transformer loss P_t, and the isolation capacitance C_i. To perform the optimization, there are three steps. The first step is to define the optimized parameters and their varying range. Then the models are constructed describing the relationship between the targets and the optimized parameters. Based on the models, a Pareto surface is plotted to illustrate the relationships among the three targets. One design point on the Pareto optimal-solution surface satisfying all three characteristics is finally picked as the optimized transformer design.

The optimized parameters include R_i, R_o, h, l_g, w_w, and N. To ensure enough space for the circuit on the transformer substrate, R_o was set to be larger than 4 mm; h was set to be smaller than 2.5 mm because a thick PCB may suffer from delamination issues; and l_g was limited by the core saturation flux density and L_m.

The models describing the relationship between the target V, P_t, C_i and the optimized parameters were built. V was calculated using (2.4). P_t was separated into the core loss P_{core} and winding loss $P_{winding}$; the core loss estimated with (2.5), where $(FWC)_{sq}$ is the flux waveform coefficient and is approximately $\pi/4$ in this case [111]. The core loss coefficient P_v in (2.5) is provided by the magnetic manufacturer. The winding loss was calculated using (2.6),

where R_{dc} is calculated based on the winding length and width using (2.7). $I_{p\text{-}rms}$ and $I_{s\text{-}rms}$ in (2.6) are the rms current of the transformer primary and secondary sides respectively. The ac winding loss is hard to estimate here given that the magnetic field around the turns is very complex and hard to calculate. FEA calculations are used instead to estimate a close value for R_{ac}, which in this case is $0.4R_{dc}$.

$$V = (2(R_o + w_o + w_w))^2 (2h_w + h) \tag{2.4}$$

$$P_{core} = (FWC)_{sq} P_v V \tag{2.5}$$

$$P_{winding} = (I_{p-rms}{}^2 + 2I_{s-rms}{}^2)(R_{dc} + R_{ac}) \tag{2.6}$$

$$\begin{aligned} l_{winding1} &= 2N(R_o - R_i + w_i + w_o) \\ S_{Cu1} &= t_w w_w \\ l_{winding2} &= 2N(h + 2h_w) \\ S_{Cu2} &= \pi(\frac{w_w}{2})^2 \\ R_{DC} &= \rho_{Cu}(\frac{l_{winding1}}{S_{Cu1}} + \frac{l_{winding2}}{S_{Cu2}}) \end{aligned} \tag{2.7}$$

The isolation capacitance model is very complex to build due to its dependence on the large number of variables. To simplify the models, the isolation capacitance is separated into two parts: $C_{w\text{-}w}$ the winding-to-winding capacitance, assuming there is no core, and $C_{w\text{-}c\text{-}w}$, the equivalent capacitance from the winding to the core, and then from the core to the winding as illustrated in Fig. 2-7. Each kind of capacitance is analyzed using Q3D simulations. If there are only two windings in the PCB material and no core, $C_{w\text{-}w}$ is mostly dependent on the shortest distance between the windings and the facing surface area. The curve-fitting method is used to get $C_{w\text{-}w}$. $C_{w\text{-}c}$ is estimated by calculating the winding surface area, and the distance from the winding to core as (2.8) shows. R_c in Fig. 2-7 is the resistance of the core between the two windings. Then the equivalent isolation capacitance C_i can be calculated according to the equivalent circuit in Fig. 2-7.

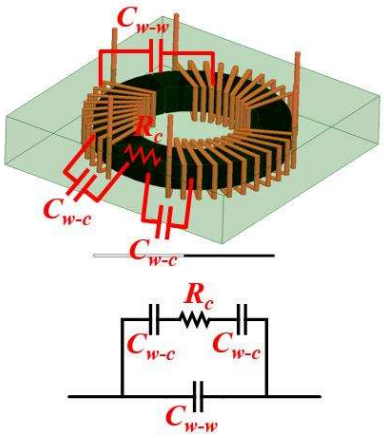


Fig. 2-7 Isolation capacitance illustration in the structure

$$C_{w-c} = C_{c-w} = \varepsilon_{PCB}\left(\frac{l_{winding1} w_w}{h_w} + \frac{l_{winding2} w_w}{w_i}\right) \tag{2.8}$$

The error of the transformer isolation capacitance model between the simulation and the practical measurement is 0.5 pF. This extra 0.5pF may relate to the extra measurement cable connected on the power supply, and the circuit layer on the transformer substrate.

2.2.3 Optimization results

With the models, the optimization is implemented in the optimization software, named CADES. To get a Pareto surface among P_t, V and C_i, there are three steps in the software. The software first finds the solutions of the transformer dimensions to the given V and C_i. The second step is to find the solution which comes up with the smallest P_t among the first-step results. This solution is marked as the best design with the given V and C_i. The final step in the software is to sweep values of V and C_i and to find the best design points for each V and C_i combination. The output of the software is plotted in Fig. 2-8.

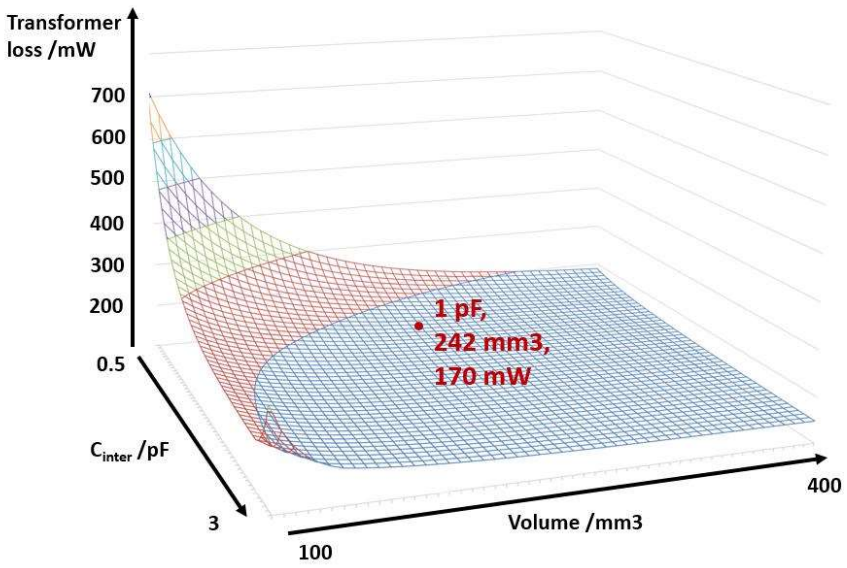


Fig. 2-8 Pareto surface within loss, isolation capacitance, and volume for the transformer design.

It is observed in Fig. 2-8 that when V comes smaller with a fixed C_i, the transformer loss increases significantly because the maximum flux density increases when the core size shrinks. It is also concluded from the surface that when the volume is fixed, the larger the isolation capacitance is, the smaller the loss is. This is caused by the winding width variation. When the winding width is larger, the winding resistance reduces and the loss reduces correspondingly. However, with wider-trace windings on a fixed core, the distance between the windings gets closer and the facing area is larger, and therefore the isolation capacitance is larger. On the Pareto surface, one design with estimated 1 pF isolation capacitance, 170 mW transformer loss with the size of 242 mm^3 is selected to fabricate and test. The optimized dimensions at this point are listed in Table 2-6.

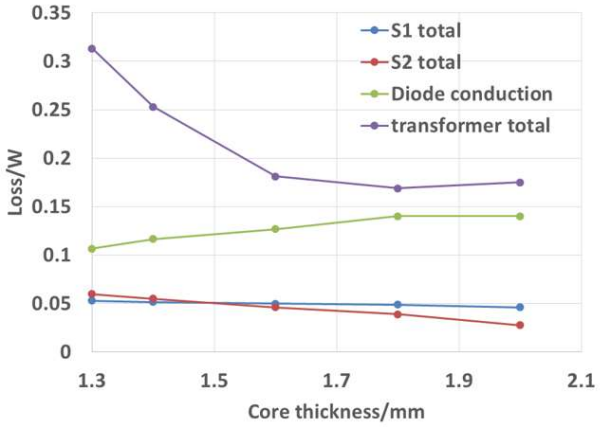


Fig. 2-9 Loss analysis for different *h*, with 1 MHz switching frequency.

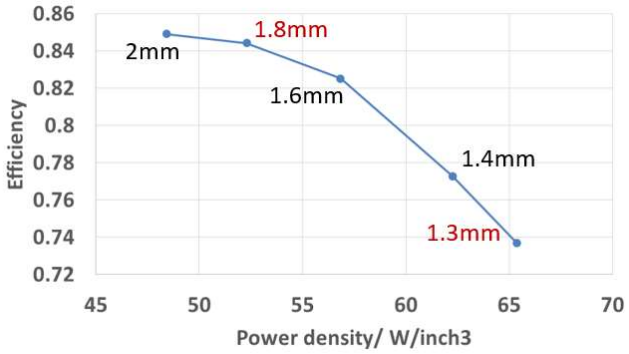


Fig. 2-10 Efficiency estimation vs power density for different h, with 1 MHz switching frequency.

With the selected design point, the magnetizing inductance L_m is 3.7 μH. With 1.8-mm-thickness core the 84% efficiency is expected. Almost half of the total loss dissipates on the transformer and the diode takes 30% of the loss. Detailed design is explored near 1.8 mm thickness. Fig. 2-9 and Fig. 2-10 show the loss break-down and the estimated efficiency with 1.3 mm ~ 2 mm thickness core, whose inner and outer radius is the same as the value in Table 2-6. When the core thickness increases, the cross-area of the toroidal core becomes larger and therefore core loss reduces. With the fixed turn number N=10, the magnetizing inductance increases as well, the rms current and the turn-off current of switches reduces and therefore the

switching conduction loss and turn-off loss reduces. As the penalty of the reduced loss, the volume of the PCB containing the transformer increases and the power density of the overall converter decreases.

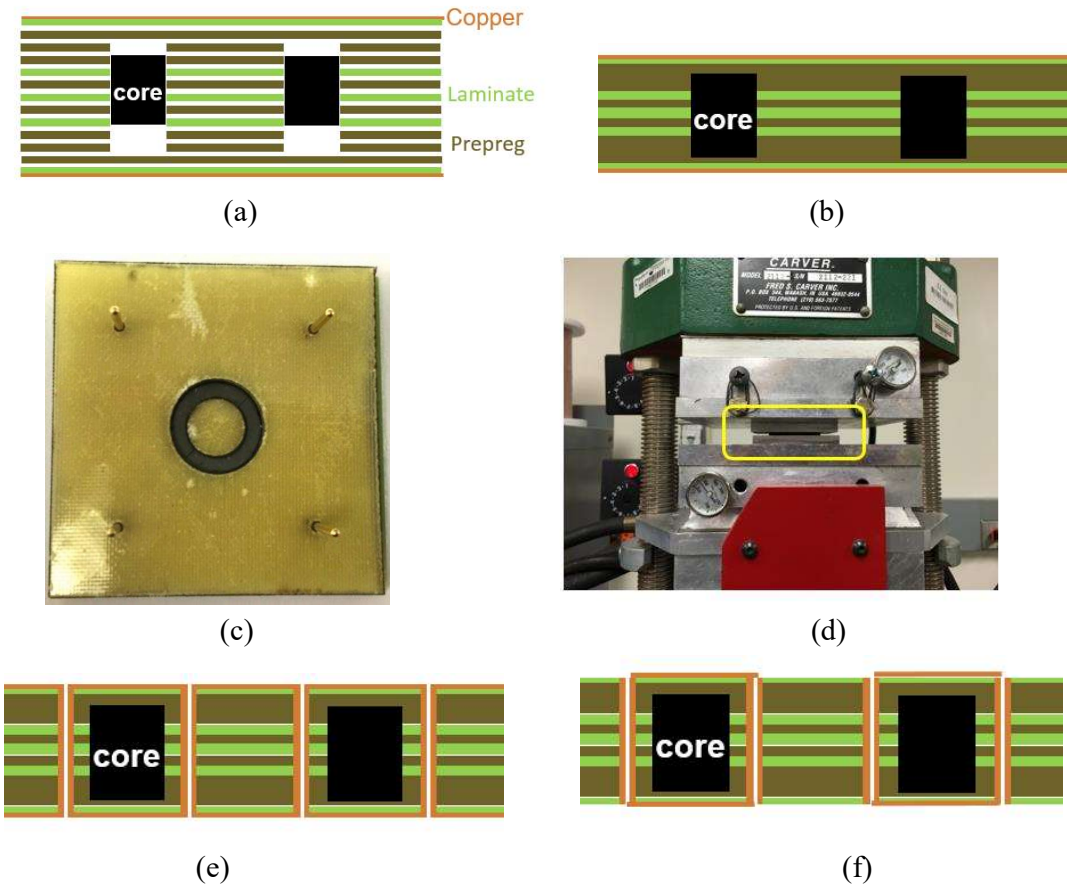
2.3 Transformer Fabrication and Converter Assembly

With the design parameters listed in Table 2-6, the PCB-embedded transformer is constructed based on standard PCB lamination. As a comparison of selected design with 1.8 mm thickness, another sample with 1.3 mm thickness core is built as well. Afterwards, the converter is built by connecting the transformer and the circuit layer with one more lamination process.

2.3.1 Embedding of transformer core

To connect several laminate layers with copper into one board, a PCB lamination process is carried out. In the dual stage pressure cycle, the prepreg material is melted to connect the laminate layers, and the air within the layers is extracted. In order to embed the magnetic core within the PCB material, before the dual stage pressure cycle, the laminate and prepregmaterial are first cut with the shape of the core, and the core is put into the 'sandwiched' layer stack composed of the laminate and prepreg material. These steps are illustrated in Fig. 2-11 (a). The middle layers of the laminate material should have similar thickness as the core in order to relieve the vertical pressure on the core during the dual-stage pressure cycle. As the ferrite is easy to break under imbalanced pressure on the surface, it is better to put several prepreglayers between the middle laminate layers and the top and bottom laminate layers as a pressure buffer for compliance purposes. After the lamination, the core is fixed within the PCB material, as Fig. 2-11 (b) shows. The air gap of the core is also filled with prepreg material. The relative permeability of the prepreg material is almost the same as that of air, so the magnetic

parameters of the transformer remain constant after lamination. Fig. 2-11 (c) and (d) show one sample under the layer stack before lamination and the during lamination process.



(a) (b)

(c) (d)

(e) (f)

Fig. 2-11 (a) Layer stack before PCB lamination; (b) PCB after lamination; (c) one sample during layer stack before lamination; (d) one sample is under dual stage pressure cycle; (e) Via-hole construction after PCB lamination; (f) winding construction.

2.3.2 Winding fabrication

With the core embedded in the PCB, the transformer windings are fabricated around the core. First the vias are constructed as Fig. 2-11 (e) shows. Then the copper, except for the winding traces on the top and bottom layer, is removed. The resultant PCB is shown in Fig. 2-11 (f). The constructed transformer is shown in Fig. 2-12, where the vias, the PCB traces,

and the air gap are clearly seen. The finished thickness of the transformer in Fig. 2-12 is 2.1 mm. The primary magnetizing inductance is 3.7 μH and the leakage inductance is 1.7 μH.

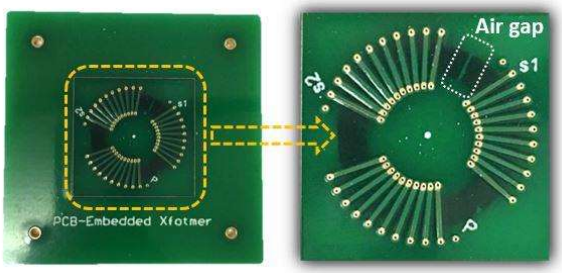
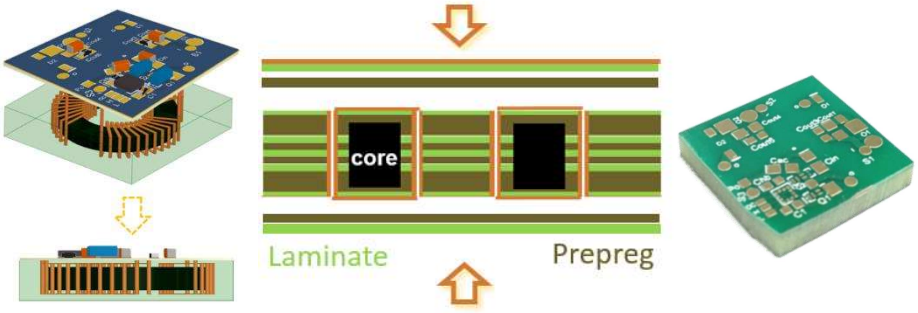


Fig. 2-12 PCB-embedded transformer.

2.3.3 Converter assembly

With the fabricated transformer, the circuit layer is connected to the transformer with a second lamination process, shown in Fig. 2-13 (a) and (b). The six winding terminals can connect to the circuit layer by vias. In this way, the PCB-embedded transformer works as a substrate of the converter, rather than taking space on the circuit layer. The converter after assembly is shown in Fig. 2-13 (c). It is seen in Fig. 2-13 (b) that both the winding top and bottom traces are covered by the PCB material, which helps increase the isolation voltage among the three windings. Otherwise, the electrical break-down through air may happen under high voltage difference conditions between the input and the output side of the power supply. It is also suggested to coat the circuit with insulation material to avoid the electrical break-down along the converter surface.



(a) (b) (c)

Fig. 2-13 (a) Converter assembly with the transformer substrate; (b) PCB lamination to connect the transformer and the circuit; (c) Converter after the assembly

The proposed PCB-embedded transformer structure and fabrication process can be applicable in other low power isolated power converter design, with the similar leakage inductor requirement. The adoption of the high power converter can be limited by the large size of the core, larger inductor or transformer loss, high temperature and manufacture, which is more challenging. Furthermore, the curie temperature of the magnetic material should be higher than the temperature used during PCB lamination process. The discussion above is also applicable for other PCB-embedded transformer structures, like the planar core with PCB windings [42].

The steps to design a PCB-embedded transformer in the proposed structure for a given topology and working condition are summarized below. 1) Select devices based on loss estimation and determine the bounds for the magnetic inductance and leakage inductance; 2) Considering manufacturing limitations, design the winding structure, select PCB and core material; 3) Define dimensions to be optimized, set design targets, such as loss, efficiency, volume, power density, isolation capacitance, current ripple, etc.; 4) Build model or equation between the optimized parameter and the targets, extract a Pareto-front or Pareto-surface; 5) With the selected design dimensions, fabricate transformer, including embedding core,

constructing via-holes and winding traces; 6) Design the circuit layer and connect the circuit layer to the transformer.

2.4 Evaluation and characteristics of the Gate Drive Power Supply

2.4.1 Electrical characteristics

Based on the fabrication procedures above, the final converter hardware is built and shown in Fig. 2-14, whose characteristics are listed in Table 2-7. The total size of the converter with a 1.3-mm-thick core (Sample 1) is 321 mm^3 (13 mm x 13 mm x 1.9 mm), and it is 405 mm^3 (13 mm x 13 mm x 2.4 mm) for Sample 2, with a 1.8-mm-thick core. With 2 W output, the overall power density of the converter is 91.6 W/in^3 for Sample 1 and 72 W/in^3 for Sample 2. The isolation voltage between the windings was measured to be 2 kV at 60 Hz. After 5 min of high voltage excitation, there was no partial discharge or breaking-down phenomena observed. The isolation capacitance was measured to be 1.5 pF for Sample 1, and 1.6 pF for Sample 2. It is also found in the measurement that the capacitance between the two secondary windings was 1.5 pF in Sample 1, and 1.6 pF in Sample 2. These small capacitance values guarantee a negligible interference from the high side gate-driver to the low side gate-driver through the power supply. The overall efficiency of Sample 2 with 2 W load was measured to be 85 %. The thermal distribution of the circuit layer, shown in Fig. 2-15, under full load with 25℃ room temperature is illustrated in Fig. 2-16, where the GaN devices reach 41.1℃ and the diode temperature is 59.6℃. The efficiency under different load condition is measured and is depicted in Fig. 2-17. When the load drops to 15% (0.3 W), the efficiency decreases to 68% and the duty cycle of S_1 needs to drop from 33% to 31% to maintain 7 V output voltage.

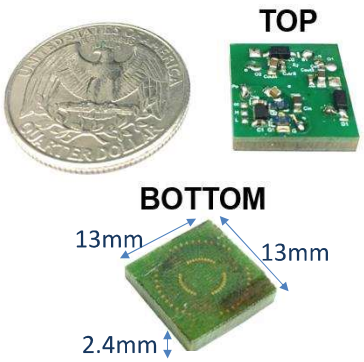


Fig. 2-14 Active-clamp flyback with the PCB-embedded transformer substrate.

Fig. 2-15 Circuit layer and the power loop (black dash line) when S_1 turns off.

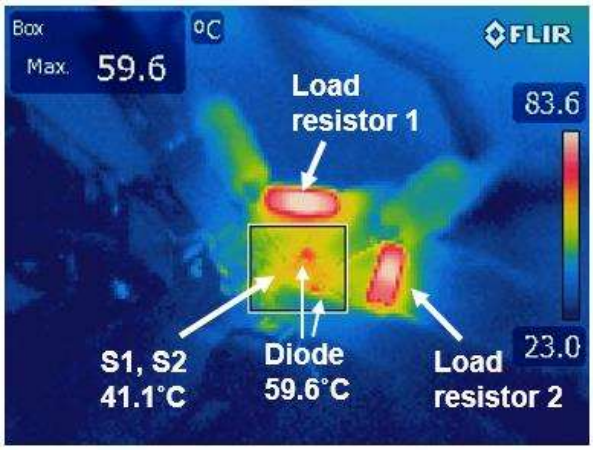


Fig. 2-16 Thermal distribution under full load

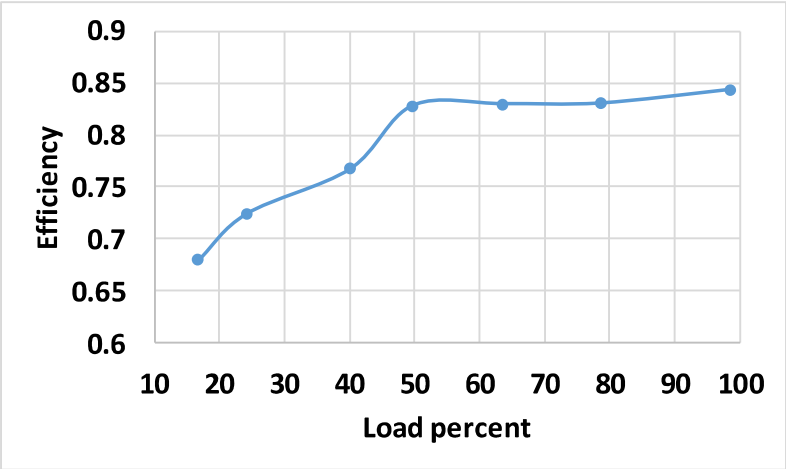


Fig. 2-17 Efficiency under different load

Table 2-7 characteristics of 2 W isolated power supply with PCB-embedded transformer

Sample No.	*Core thickness /mm*	*Switching frequency /MHz*	*Efficiency*	*Volume /mm³*	*Isolation capacitance /pF*	*Power density / W/in³*	*Isolation voltage*
1	1.3	1	73%	321	1.5	91.6	2kV AC >1min
2	1.8	1	85%	405	1.6	72	

Lastly, the PWM gate-signals of the converter were created by a function generator, as the PWM controller implementation was out of the immediate scope of this work. Nonetheless, the control circuitry was planned to be implemented on the bottom layer of the power supply shown in Fig. 2-14, minimizing the impact on the converter power density. Sufficient space was left for its implementation. One suitable controller for the design is UCC28780, an adaptive zero voltage switching active-clamp flyback controller [113], whose maximum switching frequency is 1 MHz with peak-current mode control, soft-startup and short-circuit protection. When the load current is zero, referring to the condition that the supported 650V GaN HEMT does not switch, the controller enters in 'standby power mode' to maintain the output voltage with minimum switching cycles [113].

Before the converter assembly, the circuit was tested with the PCB-embedded transformer connected by wires. In this way, the transformer current can be measured simultaneously with the drain-source voltage V_{ds} of S_1 and S_2, whose transient waveforms are captured in Fig. 2-18. The waveforms in Fig. 2-18 follow the same pattern as Fig. 2-4. Due to the discrete value of the ceramic capacitor, the resonant time is slightly longer than the S_1 off time, resulting the oscillated energy between L_r and the diode output capacitor. To this end, there are some oscillations observed in the transformer primary side current and the output voltage. When S_1 turns off, there is an obvious voltage overshoot, which is induced by the parasitic power loop inductance of the PCB layout. As the circuit is built on a single-layer PCB, the power-loop between the primary transformer terminals is long, which is highlighted in Fig. 2-15 as the black dash line, and it introduces a large parasitic inductance. If a two-layer PCB is utilized for the circuit layer, the power loop inductance could be minimized at the expense of a total PCB thickness increase by 0.1 - 0.2 mm.

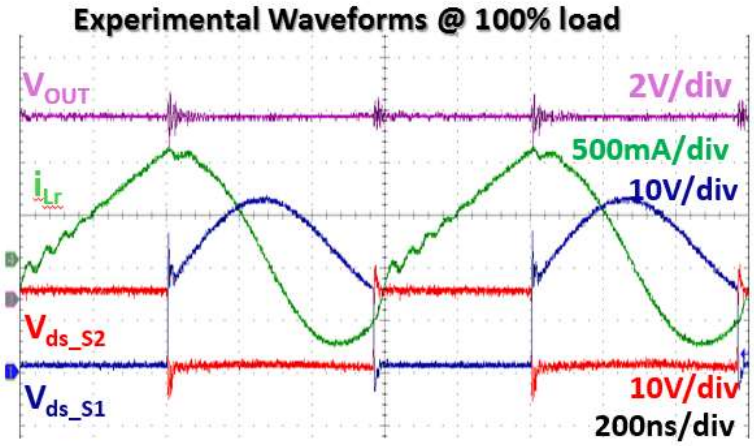


Fig. 2-18 Experimental waveforms of the gate drive power supply with 1 MHz switching frequency.

2.4.2 EMI measurement

To verify the effect from the isolation capacitance on the EMI emission in the gate driver loop, i_{CM_GD} highlighted in Fig. 1-3, is measured with the designed power supply and the state-of-the-art power supply MEJ2S0509SC [36]. Typical gate driver power supplies with reinforced solution have an isolation capacitance in the 10pF. MEJ2S0509SC with 4pF is unique in the market. To drive two HEMTs in a phase leg, two MEJ2S0509SC are adopted. The experimental setup is shown in Fig. 2-19. One phase leg with 650 V 60 A GaN HEMTs is switching with 100 kHz 50% duty cycle, with no load and 400 V input voltage. The drain-source voltage of the low-side HEMT V_{DS} is captured by a high voltage differential probe. The CM current within the gate driver loop i_{CM_GD} is measured by a 100 MHz high-bandwidth current probe.

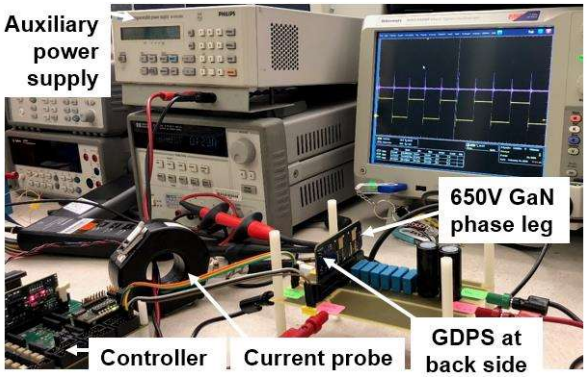


Fig. 2-19 Setup to measure i_{CM_GD} with 650V GaN HMETs

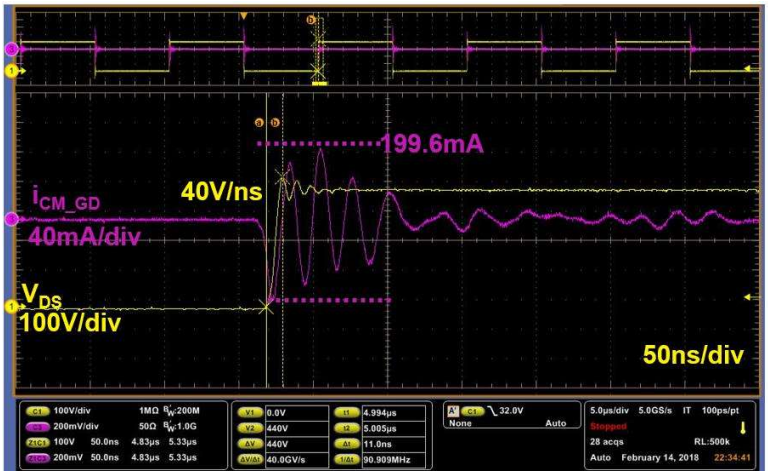


Fig. 2-20 Transient waveforms using MEJ2S0509SC

Fig. 2-20 shows the transient waveforms of V_{DS} and i_{CM_GD} using MEJ2S0509SC. The dv/dt of the 650V GaN HEMTs is 40 V/ns during turn-off, generating the CM emission i_{CM_GD} with 199.6 mA magnitude in the gate driver loops. With the replacement by the proposed power supply, i_{CM_GD} magnitude is reduced to 157.4 mA, corresponding to a 27% reduction in CM current, depicted in Fig. 2-21. The spectra of i_{CM_GD} in the two experiments are plotted and compared in Fig. 2-22. It is found that the conducted EMI emission in the gate driver loop is reduced by 3 dB from 100 kHz to 10 MHz from replacing MEJ2S0509SC by the designed gate driver power supply.

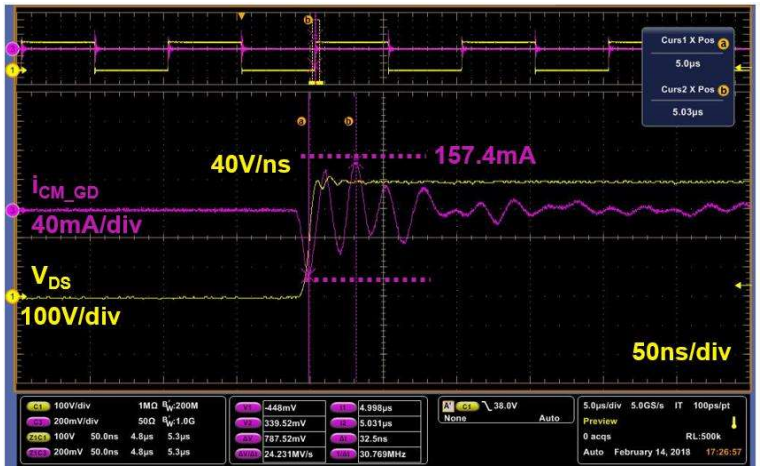


Fig. 2-21 Transient waveforms using proposed gate driver power supply

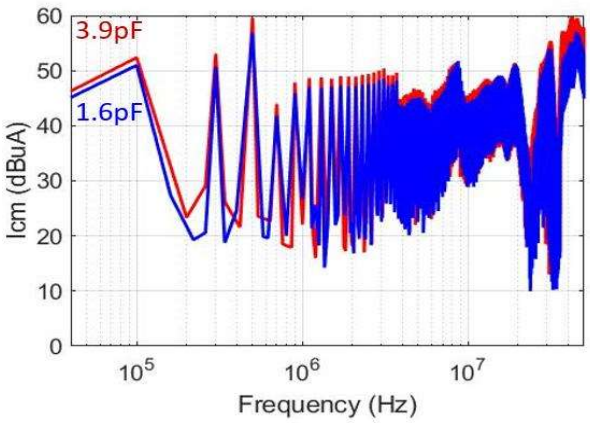


Fig. 2-22 i_{CM_GD} comparison using the proposed design and MEJ2S0509SC

2.4.3 Thermal reliability

A thermal cycling test was performed to explore the thermal reliability of the embedded transformer structure. The main concern here was that the core may break under the differing thermal expansion between the PCB material and the core when the operating temperature varies from –50 °C to 200 °C. To this end, a total of 150 one-hour temperature cycles we conducted on six samples, whose profile is shown in Fig. 2-23; three of them were made of FR4, and the rest of MEGTRON2 (R-1577). Before the test, the FR4 samples were visually inspected to ensure that there was no damage around that the core and the air gap were clearly seen. One sample before the test is shown in Fig. 2-24 (a). The MEGTRON samples could not be visually inspected due to non-transparent nature of the laminate material.

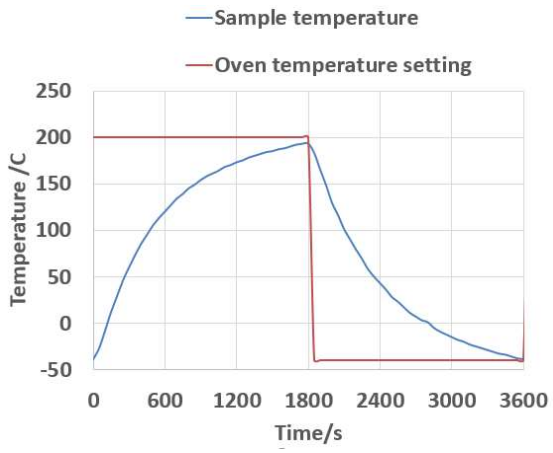
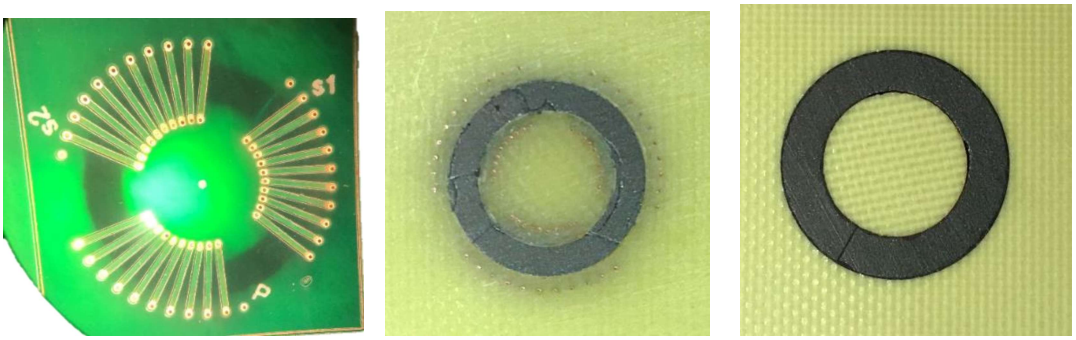


Fig. 2-23 Sample temperature in one cycle



(a) (b) (c)

Fig. 2-24 (a) FR sample image before the thermal cycling test; (b) FR4 sample image after the thermal cycling test; (c) MEGTRON 2 sample image after the thermal cycling test

The resultant core images after the thermal cycling tests were conducted are shown in Fig. 2-24 (b) and (c). To get the images, the top PCB layer covering the core was polished. In Fig. 2-24 (b), it is seen that the core within FR4 is completely cracked. The large thermal expansion from the PCB material puts so much pressure on the ferrite core that the core cannot withhold it. On the other hand, the core embedded in the MEGTRON2 sample, shown in Fig. 2-24 (c), looked the same after the tests, showing no evidence of cracking. This simple test pointed out the importance of selecting the right PCB material for power supplies intended to operate at high ambient temperature conditions, demonstrating as well the desirable properties of the MEGTRON2 material. To fully assess the lifetime of the power supply operating in such conditions an extended number of cycles would be required.

2.5 Summary and Conclusions

This chapter presented the design of an integrated dual-output gate-driver power supply with a PCB-embedded transformer based on GaN HEMT devices operating at a switching frequency of 1 MHz. With careful design, the constructed converter with two 1-W isolated outputs was demonstrated to achieve 85 % overall efficiency, featuring a minimal 1.6 pF isolation capacitance, both primary-to-secondary and secondary-to-secondary, achieving a power density of 72 W/in^3. An optimization of the transformer dimension was performed and presented to identify the key tradeoffs among the transformer loss, inter-winding capacitance, and volume, with which a solution on the Pareto-optimal surface was found. The designed PCB-embedded transformer was then fabricated and effectively embedded into the PCB material, being finally integrated with a top active circuit layer hosting the GaN devices and passive components. Experimental tests were conducted to demonstrate its operation and attained performance. Further, thermal cycling tests with alternative PCB materials were conducted to assess the feasibility of operating at high ambient temperature (200 °C), where the MEGTRON 2 material from Panasonic showed superior qualities matching the ferrite material used for the transformer core. Lastly, the proposed optimization design approach and the proposed power supply structure demonstrated the feasibility of simultaneously achieving high power density and high efficiency when utilizing the PCB-embedded transformer as substrate for GaN-based power converters.

Chapter 3. High Switching Frequency 3-Phase GaN-Based Inverter Design

Based on the existing study in section 1.2.3, this chapter first presents a modular half bridge design of 650V GaN HEMTs, enabling 100 kHz - 500 kHz switching frequency, for the application of a 1 kW 400 Vdc two-level three-phase inverter. It uses double-side power loop to achieve a small power loop and a compact size, with the adaptive double side thermal solution. To control the device temperature and fully utilize the space, the minimum heat sink volume is calculated based on the thermal resistance requirement. A compact inverter structure is then proposed, rendering a power density of 7.1 kW/L for 500 kHz switching frequency operation. Experimental results on the design inverter are illustrated to verify the thermal design and EMI noise prediction. Based on the inverter design with modular half bridge, a comprehensive study on the switching frequency effect on the two-level three-phase inverter performance is presented. First the switching frequency effect on the inverter loss is estimated, based on which the corresponding inverter efficiency and the required heat sink volume are estimated. The second study on the EMI noise is performed with the measured conducted EMI spectral under different switching frequency. The effects from the switching frequency on the common-mode (CM) and differential-mode (DM) EMI are demonstrated respectively. The corresponding input and output, CM and DM EMI filters are designed using the unterminated behavioral model developed in [114][115] with optimization. The switching frequency effect on the CM and DM EMI filter volume is then assessed to demonstrate the tradeoff between the switching frequency and CM/DM EMI filter volume.

3.1 Compact GaN-based inverter design

3.2.1 Modular design of a GaN HEMT phase leg

In order to achieve a minimized power loop for 650V 60A GaN HEMTs, the back-to-back power loop, also called the double-side power loop is utilized, depicted in Fig. 3-1. The high side and low side GaN transistors are located back to back at the separate side of the PCB. The whole power loop inductance in this design is 1.775nH, based on the Q3D simulation. Compared with the existent solution by arranging the high side and low side devices on the same layer of PCB, the designed phase leg has a smaller power loop footprint and a smaller parasitic inductance.

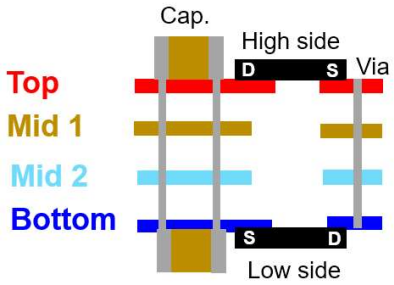


Fig. 3-1 Back-to back power loop design

The gate drivers of the high side and low side devices locate next to the transistors closely, shown in Fig. 3-2. The gate driver is selected as Si8271AB, an isolated gate driver with 200 V/ns CM immunity, which makes a suitable gate driver for the GaN HEMT in question. The maximum turn-on current is 1 A, and 4 A for turn-off, large enough to drive one or two HEMTs. The turn-on gate voltage V_{GCC} is 6.4 V and the turn-off voltage is -1.9 V. The latter value is selected to avoid the false turn-on of the transistor when the other transistor in the phase leg turns-on due to the miller effect. As for the PCB layout of the gate loop, it is highlighted in Fig. 3-2 with the high-side turn-off loop as an example. Thanks to the small loop, the gate resistance for turn-on is 1 Ω and 0 Ω for turn-off. Furthermore, it is observed that the gate loops

are in the same horizontal plane as the PCB, whereas the power loop is vertical to the PCB plane (in Fig. 3-1). This configuration can reduce the radiative interference from the high dv/dt in the power stage to the sensitive gate loop. The isolation capacitance of the selected gate driver power supply is only 2.1 pF, reducing the CM EMI emission generated in the power loop propagated through the gate driver power supply and protecting the gate driver from the high dv/dt.

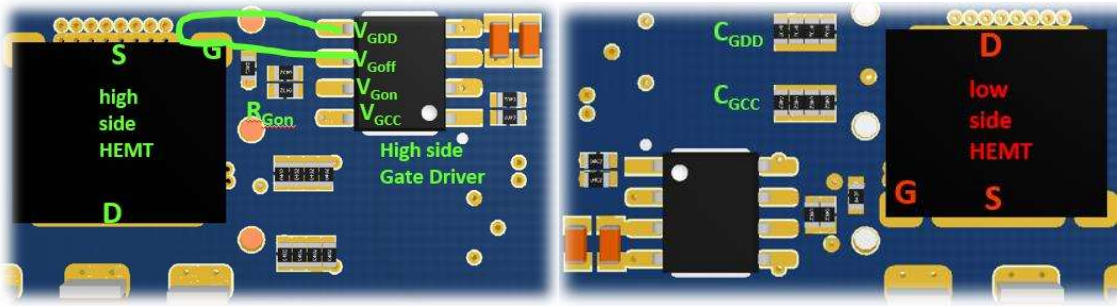


Fig. 3-2 Gate loop design of the GaN phase leg; left: top layer with high-side HEMT, right: bottom layer with low-side HEMT

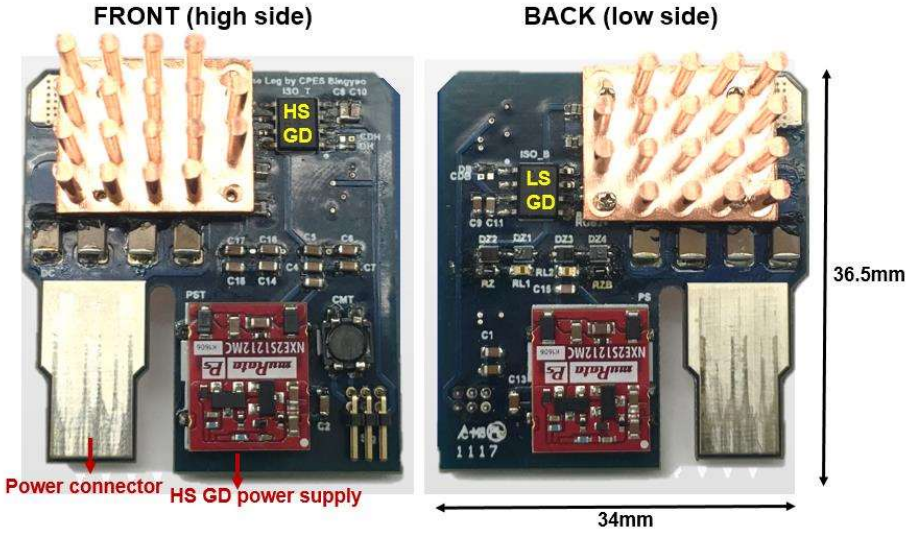
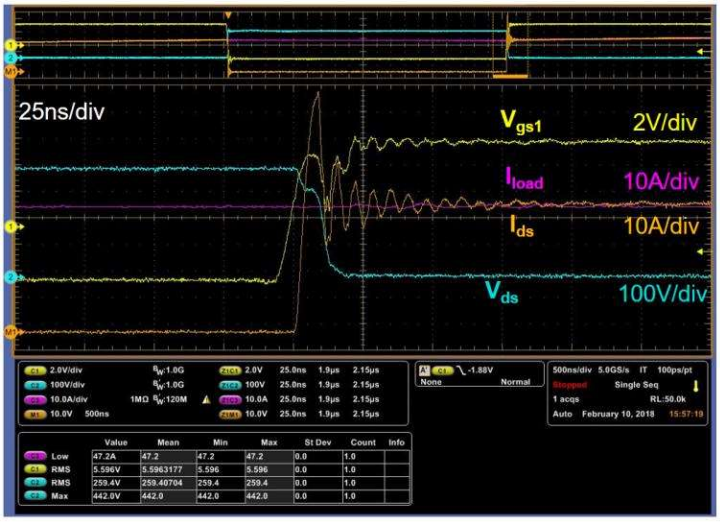


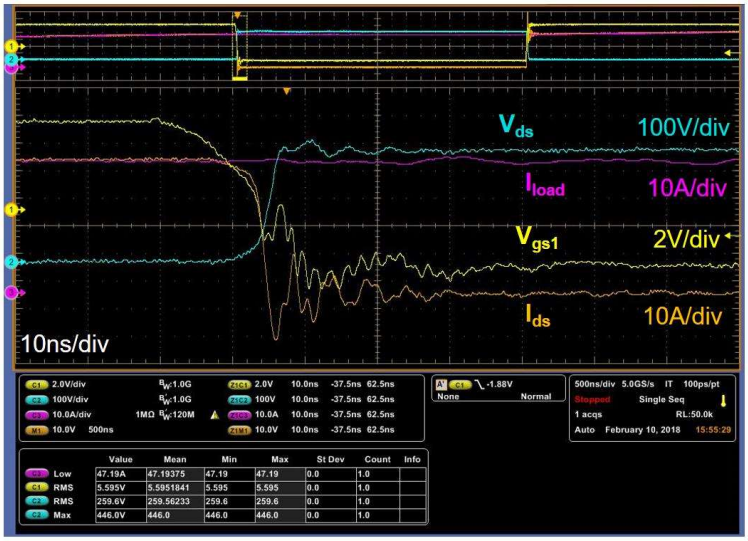
Fig. 3-3 Designed GaN half bridge module

The switching cell evinced in Fig. 3-3 is also implemented with the power contacts and a signal connector. Thanks to this configuration, the switching cell can be plugged in and out

from the socket on the inverter mother board once a failure occurs, saving cost and deluging time.



(a)



(b)

Fig. 3-4 Transient waveforms of the turn-on (a) and turn-off (b) under 400 Vdc, 50 A load current with 1 Ω turn-on resistor and 0 Ω turn-off resistor

3.2.2 Switching loss characterization

To character the switching loss of the device in question, a double pulse tester was built based on the half bridge with a current shunt implemented to measure I_{ds}. The transient

waveforms of the test under 400 Vdc, 50 A load current with 1 Ω turn-on resistor and 0 Ω turn-off resistor are shown in Fig. 3-4 respectively. The voltage drop during turn-on is due to the parasitic inductance introduced by the current shunt. The switching cell turn-on and turn-off energy was measured with different load current, whose results are summarized in Fig. 3-5 with different I_{ds}. It is observed that the turn-on loss increases almost linearly with the I_{ds}, as well as the turn-on resistor.

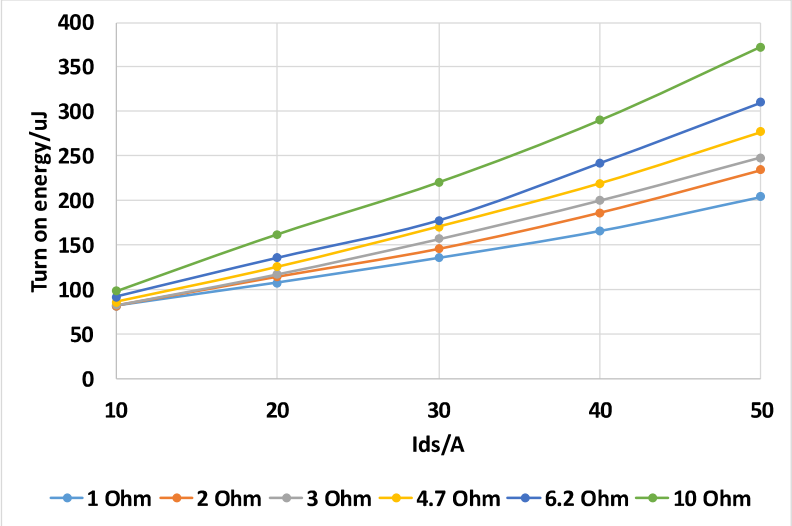


Fig. 3-5 Turn-on energy with different load current

3.2.3 Thermal management

Fig. 3-3 and Fig. 3-6 exhibit the front and side view of the adaptive heat sink design for the phase leg. Two separate heat sinks are mounted on the top size of the two HEMTs. Screws are used to force the heat sink to the device thermal pad tightly. In this way, two heat sinks are short-circuit through the mental screws and are required insulation from the device thermal pad, which is connected to the device drain terminal. To this end, one thin alumina layer is inserted between the heat sink and the device. Thanks to the small thickness and the good thermal conductivity, the alumina layer has ignorable thermal resistance. Furthermore, this alumina layer increases the vertical distance from the heat sink to the PCB. The gate resistor

and the gate decoupling capacitors thus can be placed under the heat sink, utilizing the PCB space under the heat sink and enabling a smaller gate loop inductance. This part is highlighted in Fig. 3-6 circled by the blue dashed line.

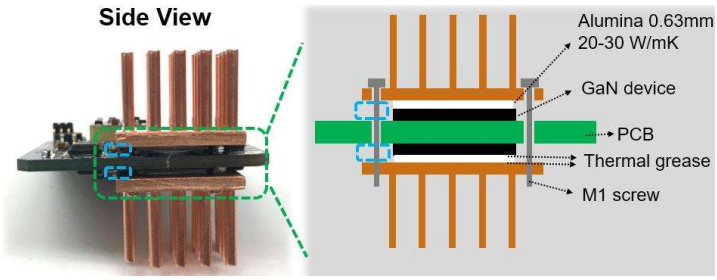


Fig. 3-6 Thermal solution for the designed GaN half bridge

Within the converter, the thermal management or the heat sink volume takes a large partial of volume and weight. Proper heat sink design helps to increase the converter power density and control the device temperature. With the given device loss in the worst case, the heat sink volume can be optimized. In the heat sink design of the proposed switching cell, given the heat sink cross-area 17.2 x 13.7 mm, the thermal resistance of the heat sink is controlled by the heat sink pin height. Based on the heat sink datasheet, the relationship between the pin height H_{th} (mm) and the thermal resistance R_{th} (˚C/W) is formulated as (3.1) under 400 linear foot per meter (LFM). The heat sink R_{th} required with the device loss P , the room temperature T_0 and the device operating temperature T is calculated in (3.2) given that the junction-to-case thermal resistance is 0.3 ˚C/W [3]. For example, under 500 kHz switching frequency 1 kW 400 Vdc input voltage, the device loss is estimated as 13.64 W at 100 ˚C operation temperature. The thermal resistance needed under 25 ˚C room temperature is 5 ˚C/W and the corresponding heat sink pin height is 14.2 mm. The estimated heat sink temperature is 93.2 ˚C. The designed heat sink thermal resistance is further verified by experimental evaluation. With the standard design approach above, the effect on the heat sink volume from the switching frequency can be assessed.

$$H_{th} = 58.503 R_{th}^{-0.878} \tag{3.1}$$

$$R_{th} = (T - T_0)/P - 0.3 \tag{3.2}$$

$$l_{total} = 6h_{hs} + 33.8 \tag{3.3}$$

3.2.4 Compact inverter structure

To build a compact three phase inverter, the proposed three-phase inverter structure is depicted in Fig. 6, where the three switching cells stand on the inverter mother board. The input film capacitors with different capacitance combination locate on the mother board as well, fully utilizing the space under the heat sink. These capacitors also serve as the input DM EMI filter. The inverter length l_{total} shown in Fig. 6 is dependent on the heat sink pin height. For example, with 15 mm heat sink height, the inverter length is 123.8 mm as (3) formulates. The inverter shown in Fig. 6 is designed for 500 kHz switching frequency operation, whose power density is as high as 7.1 kW/L. Another advantage of the prototype is that its power cell volume can be estimated using (1)~(3) with a given working condition. To this end, the switching frequency effect on the power cell volume can be assessed.

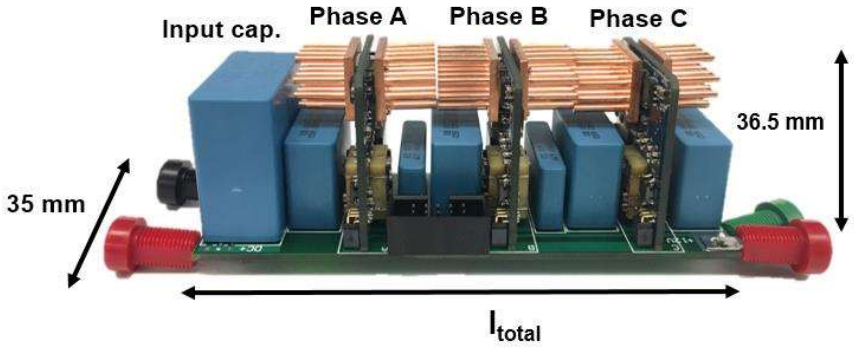


Fig. 3-7 Proposed compact three-phase inverter structure

3.2.5 Experimental verification of the design consideration

The experimental waveforms of the inverter within the test setup in Fig. 7 operating under 500 kHz switching frequency, 400 Vdc input voltage, 1 kW output power and the discontinues

SVPWM, are depicted in Fig. 8. The maximum overshoot during turn-off transient is 20V. The thermal distribution is shown in Fig. 9, where the temperature drops from the center of switching cell (the device location) to the end of heat sink pin is within 5˚C, indicating an effective heat dissipation of the design thermal management. The heat sink temperature matches the previous predicted value, also indicating that the previous device loss estimation is accurate.

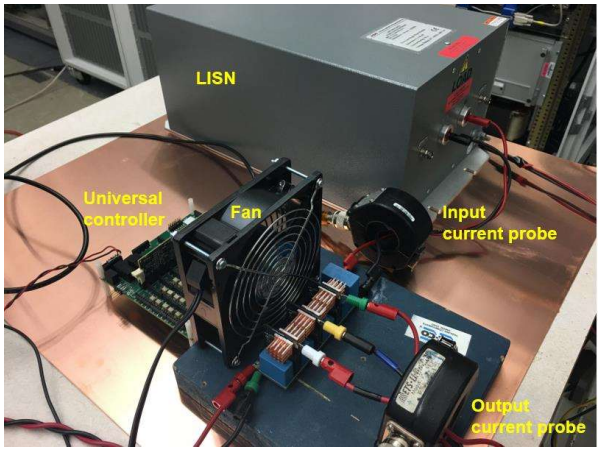
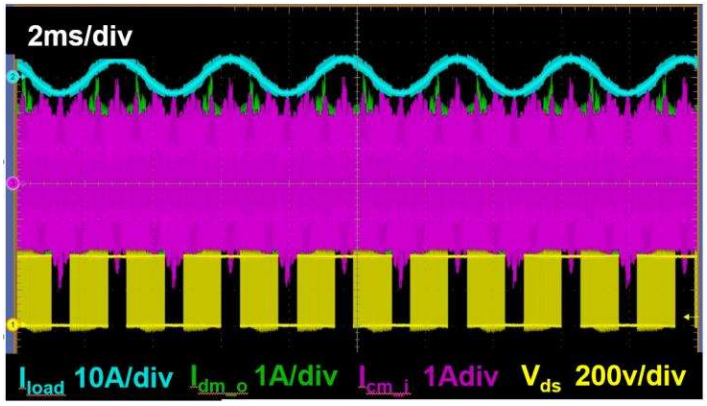
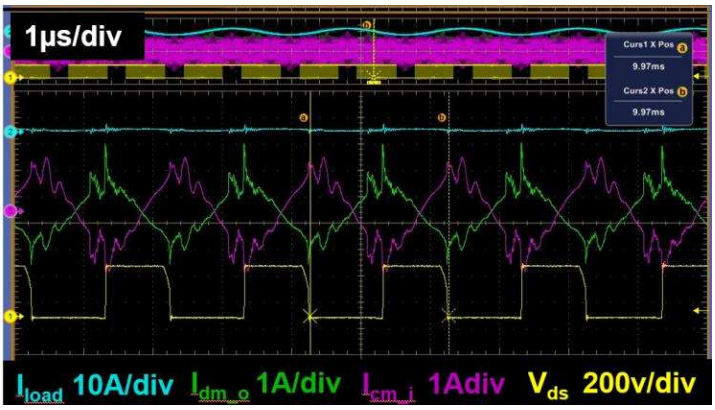


Fig. 3-8 Test setup of the three-phase inverter



(a)



(b)

Fig. 3-9 Transient waveforms under 500 kHz switching frequency

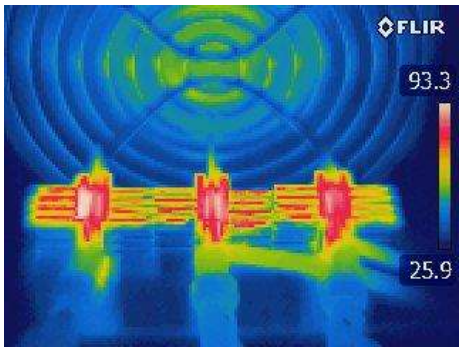


Fig. 3-10 Thermal distribution under 500 kHz switching frequency

3.2 Assessment of switching frequency effect on the efficiency and power cell volume of GaN-based inverter

In the two-level three-phase inverter, the dominated loss comes from the switching devices, including the conduction loss, the switching loss, and the dead-time loss. The first portion is dependent on the rms current and the on-resistance R_{ds}. The R_{ds} is also determined by the junction temperature and the transient current. To this end, the conduction loss of the inverter is calculated as (3.4), where α_T is the temperature factor and β_{Ids} is the I_{ds} effect on R_{ds}. To have a fair comparison among different switching frequency operation, the device temperature is expected to 95 ˚C under different cases, resulting in α_T =1.75. β_{Ids} is found to be increase with I_{ds} in [3] and measured with the static characterization. When I_{ds} increases from 0 to 50

A, $R_{ds}\beta_{Ids}$ increases from 22.5 mΩ to 25 mΩ [3]. Due to the varying I_{ds} during the inverter operation, $R_{ds}\beta_{Ids}$ is estimated based on the transient I_{ds} during each PWM cycle. The switching loss is estimated using (3.5), where E_{on} and E_{off} are determined by the I_{ds} in each PWM cycle. Furthermore, the switching loss is only considered for the half line-cycle for each device. To perform the switching loss estimation, a two-level three-phase inverter with the ideal switch model is implemented in Simulink, featuring 1 kW output power, 400 Vdc and the discontinuous SVPWM. With the simulation, the transient I_{ds} in each switching cycle can be recorded to calculate the switching loss. The efficiency can be then estimated based on the total loss of the devices.

$$P_{cond} = 3I_{rms}R_{ds}\alpha_T\beta_{Ids} \tag{3.4}$$

$$P_{sw} = 6\sum_{i=1}^{i=fsw/2}(E_{on}(i)+E_{off}(i)) \tag{3.5}$$

$$V_{pc} = l_{total}\times 36.5\times 35(mm^3) \tag{3.6}$$

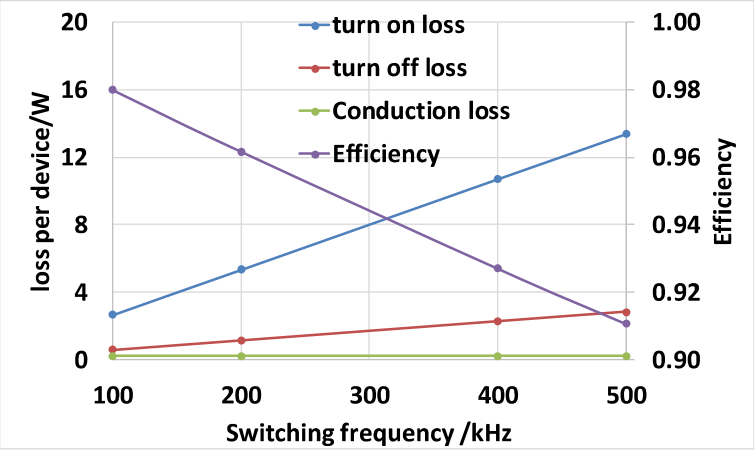


Fig. 3-11 Estimated loss and efficiency with different switching frequency

Fig. 3-11 exhibits the switching frequency effect on the loss and the efficiency. It is observed that the conduction loss is constant with the varying frequency. When the switching

frequency increases, the switching loss, especially the turn-on loss, dominates the total loss. To this end, the efficiency drops significantly with the increased switching frequency. The efficiency is 98% with 100 kHz switching frequency and drops to 91% with 500 kHz switching frequency.

With the estimated device loss above and the assumption that the devices maintain the same junction temperature under different switching frequency (to have a fair comparison), the minimum heat sink volume can be estimated for the different cases using (3.1)-(3.2). The inverter power cell volume following the structure in Fig. 3-7 can be calculated using (3.3) and (3.6). The resultant volume with different switching frequency is demonstrated in Fig. 3-12. Due to the increased switching loss, the heat sink volume or the heat sink pin has to increases to attain a smaller thermal resistance so that the device temperature is the same under the different switching frequency. Fig. 3-12 also illustrates that the inverter power cell volume increases with the increased switching frequency. This resultant trend is related to the forced air thermal solution. If fluid cooling is applied, the power cell volume maintains almost constant due to the fixed cold plate volume.

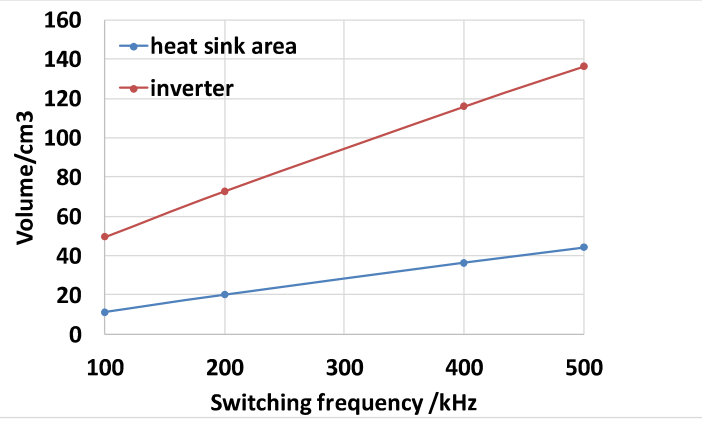


Fig. 3-12 Estimated heat sink volume and the inverter power cell volume with different switching frequency

3.3 Assessment of switching frequency effect on the EMI emission and filter design of GaN-based inverter

3.3.1 Switching frequency effect on EMI emissions

With the inverter hardware tested with the line impedance stability network (LISN), the input and output, CM and DM EMI spectral can be measured separately under different switching frequency 100 kHz – 500 kHz using 100-MHz-bandwidth current probes, whose test setup is shown Fig. 3-8. Fig. 3-13 shows the comparison of the output DM spectral under different switching frequency in the range of 150 kHz to 30 MHz. It is found that the first peak of the spectral, also the maximum peak, decreases when the switching frequency increases. The natural reason behind the trend is the inductive impedance of the load inductor below 1 MHz. The inductive impedance magnitude increases with the frequency, rendering a lower current at a high frequency. In Fig. 3-13, it is also observed that above 1 MHz a higher switching frequency leads to a larger emission. Different from the phenomenon below 1 MHz, this increased emission is due to the increased noise sources within the inverter due to the increased switching frequency.

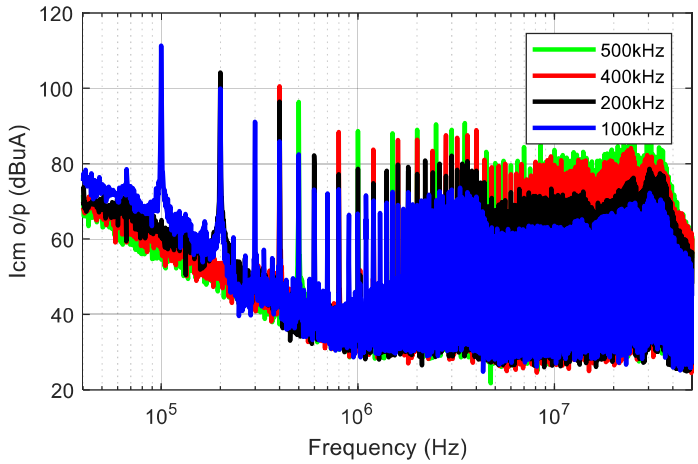


Fig. 3-13 Output DM noise spectrum comparison

In terms of CM EMI emission, the main CM propagation path within the inverter includes the parasitic distributed capacitors from the device drain and source terminals to the heat sink or the CM ground. To this end, the CM propagation path features a capacitive impedance. As a result, the first CM spectrum peak, also the maximum peak, increases with the increased switching frequency, shown in Fig. 3-14. Above 1 MHz, similarly as the DM spectral, the emission is larger with a higher switching frequency due to the increased noise sources.

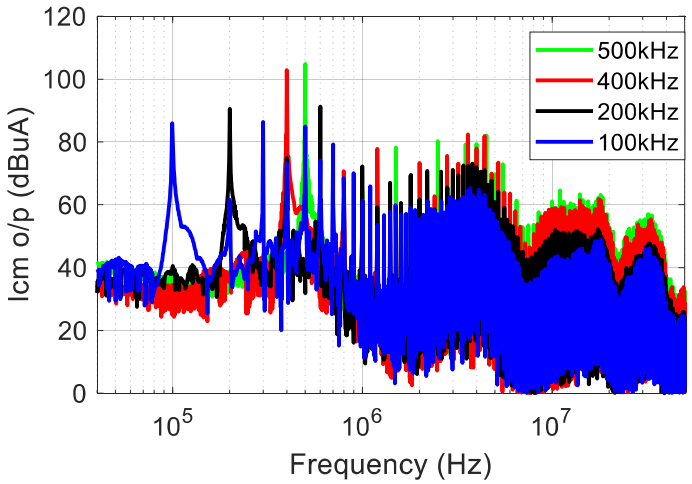


Fig. 3-14 Output CM noise spectrum comparison

Based on Fig. 3-13 and Fig. 3-14, it can be derived that the corner frequency of the DM filters increases with the switching frequency, whereas the CM filter corner frequency decreases. As a result, DM filter volume can be reduced and CM filter volume may be increased with a higher switching frequency.

3.3.2 EMI filter design using the EMI unterminated behavioral model

To design the CM and DM EMI filter for the inverter under different switching frequency, the EMI behavioral model is used. Compared with the traditional approach based on the estimated corner frequency, the unterminated EMI behavioral model, proposed in [114], can design the input, output EMI filter simultaneously. For the CM emission, it is found that the

input and output are coupled, which means the input filter affects the output spectrum. To this end, the input and output filter have to design simultaneously so that the impedance change due to the filters at both input and output side can be considered.

The unterminated behavioral model (UBM) is shown in Fig. 3-15, where V_{N1} and V_{N2}, are two noise sources and Z_{11}, Z_{12}, Z_{21} and Z_{22} are a two-port impedance network. Fig. 3-15 also shows the total CM input impedance seen by the inverter at its dc terminals, Z_{CMi}, which includes the dc source, LISN, and any EMI filter, and the corresponding CM output impedance, Z_{CMo}, which includes the feeder, load, as well as any output EMI filter. This model can be formulated in closed form as (3.7). The parameters within the model can be derived using experimental method following the procedures in [114][15]. With the model, the emission can be predicted with different filter design (different input/output impedance). Fig. 3-16 shows the predicted (calculated) CM spectral under 500 kHz switching frequency at the input and output side, which match the measured spectral up to 30 MHz.

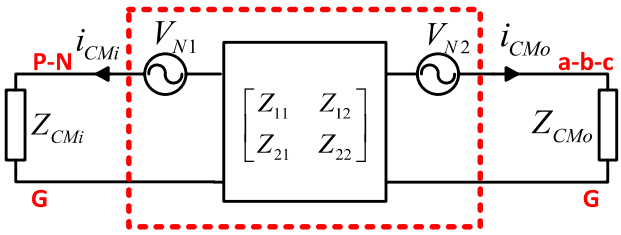


Fig. 3-15 Unterminated EMI behavioral model

$$\begin{bmatrix} -i_{CMi}Z_{CMi} \\ -i_{CMo}Z_{CMo} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_{CMi} \\ i_{CMo} \end{bmatrix} + \begin{bmatrix} V_{N1} \\ V_{N2} \end{bmatrix} \tag{3.7}$$

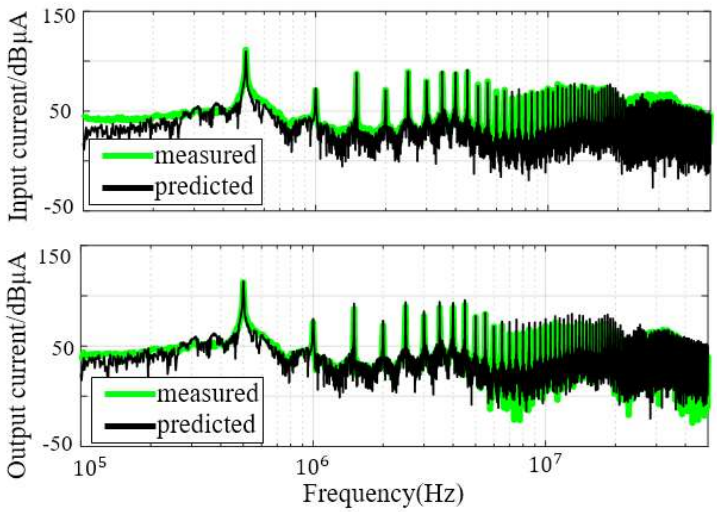


Fig. 3-16 Comparison between the measurements and the predictions of the GaN-based inverter without EMI filters.

With the developed UBM, input and output EMI filter can be designed to meet the DO-160 EMI standard with optimization following the procedures in [115], where different size of the core, combined with the different capacitors are considered and the filter topology follows the circuit in Fig. 3-17. The filter inductor design is also included in the optimization process, considering the limitation from the temperature, the magnetic saturation and the maximum turn number, shown in Fig. 3-18. The inductor in the DM input filter utilizes the leakage inductor from the input CM inductor and the capacitor in the DM input capacitor is included in the inverter power cell.

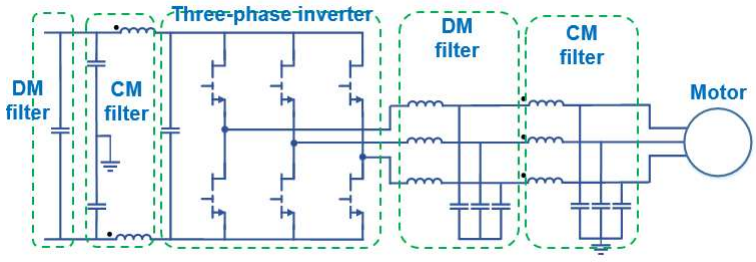


Fig. 3-17 Filter design topology

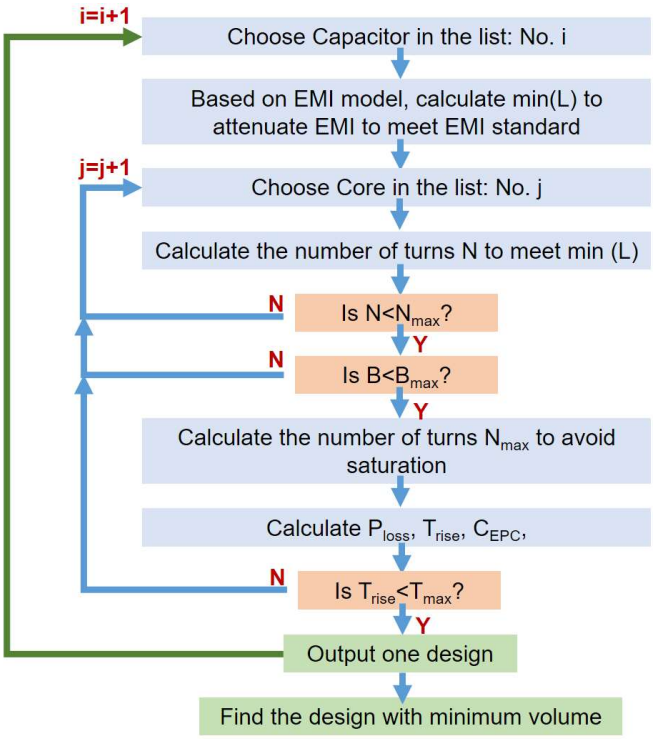


Fig. 3-18 Filter optimization process

3.3.3 Switching frequency effect on EMI filter volume

The EMI filter design featuring the minimum filter volume among the different combination of the cores and the capacitors is listed in Table 3-1, whose volume comparison under different switching frequency is plotted in Fig. 3-19. In Table 3-1, it is found that the DM output filter has a much larger size than the CM filters because of the three separate cores used in the DM output filter. In Fig. 3-19, it is observed that above 200 kHz switching frequency, the DM filter volume is reduced when the switching frequency increases. This is thanks to the small switching ripple under a higher switching frequency operation. As for the CM filter, it is found that with a higher switching frequency, the total CM filter size, including the input and output filter, increases, which matches the conclusion derived in the sub-section above. Though with a higher switching frequency a smaller voltage-second applied on the CM filter inductor providing a chance to reduce the core size, the system needs a filter with a higher attenuation

rate, leading to the size increase of the core and the capacitor. In addition to the cases above 200 kHz switching frequency, the filter design with 100 kHz switching frequency does not follow the trends observed above. The second switching frequency harmonic in the case determines the filter attenuation rate, instead of the switching frequency harmonic as the cases of '200 kHz' – '500 kHz'. It is also deserved to mention that a second-stage high-frequency EMI filter may be needed for a high switching frequency operation to attenuate the noise above 10 MHz, which is hard to be attenuated by the first-stage EMI filter in Fig. 3-17. The filter design in Table 3-1is mainly determined by the first harmonic higher than 150 kHz. Due to the parasitics of the inductor and the capacitor, the first-stage loses its desired attenuation rate at high frequency.

Table 3-1 Switching frequency effect on the EMI filter design of the GaN-based three-phase inverter

	f_{sw}/kHz	**100**	**200**	**400**	**500**
CM input filter	Inductor/mH	5.88	7.114	7.114	12.44
	Capacitor/μF	0.022	0.01	0.0047	0.0047
	Volume/cm^3	4.519	3.82	3.36	5.04
CM output filter	Inductor/mH	1.944	1.944	1.944	1.19
	Capacitor/μF	0.0047	0.01	0.022	0.022
	Volume/cm^3	3.495	4.185	5.235	5.04
DM output filter	Inductor/mH	0.5	0.5	0.5	0.5
	Capacitor/μF	0.1	0.22	0.047	0.033
	Volume/cm^3	15.69	17.58	15	14.25

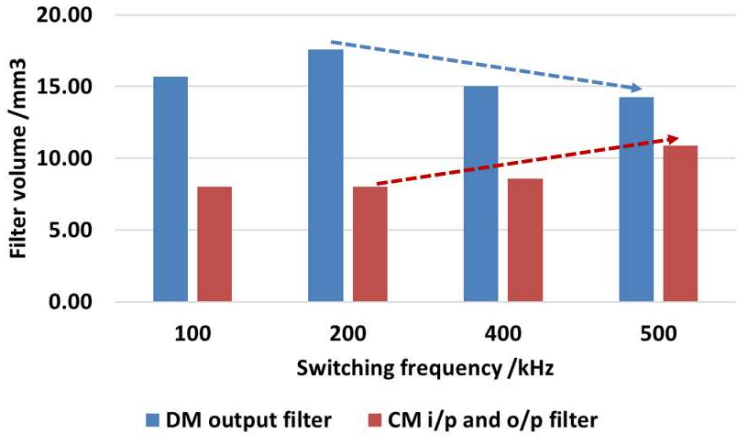


Fig. 3-19 Filter design under different switching frequency

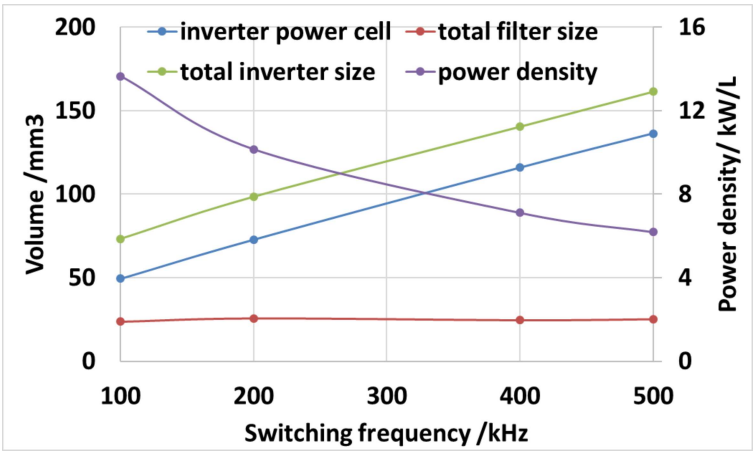


Fig. 3-20 Switching frequency effect on the inverter volume and power density

The EMI volume together with the inverter power cell volume under different switching frequency is compared in Fig. 3-20. Based on the estimated EMI filter size, the total EMI filter under different switching remains almost the same. This conclusion may change when the inverter propagation impedance changes or the operation condition changes. When the power cell volume dominates the total inverter volume, the total power density of the inverter drops with the increased switching frequency.

3.4 Summary and conclusions

This chapter presented a compact three-phase inverter design based on a modular switching cell design using 650 V 60 A e-mode GaN HEMTs. The design consideration on the power loop layout and the gate loop were demonstrated in detail. The standard design procedure for the heat sink was presented then so that the switching frequency effect on the heat sink could be quantified. The prototype built for the 500 kHz switching frequency operation verified the design approached for the targeted efficiency, power density and temperature.

The effect from the switching frequency on the inverter loss, efficiency, heat sink volume, CM/DM EMI emission, and filter design were assessed. It was found that the efficiency dropped significantly with the increased switching frequency when the switching loss dominated the total loss. As a result, the air-cooling heat sink volume increased. When switching frequency increased, the DM EMI spectral below 1 MHz decreased whereas the CM EMI increased. Above 1 MHz, the EMI emission increased. As a result of the trend below 1 MHz, the DM filter volume tended to decrease and the CM filter volume increases with a higher switching frequency. Considering the effect from heat sink and EMI filter volume, the inverter power density decreased with the increased switching frequency. The conclusions above is limited by the design approach, topology, operation conditions and thermal management.

Chapter 4. Active Gate Driver Design of 650V GaN HEMT

The CM EMI emission in the motor drive or three-phase voltage source inverter (VSI) was observed to increase with a higher switching frequency and adoption of wide-bandgap devices. For the emission within 150 kHz to 10 MHz, the EMI filter can be designed with optimization to attenuate it to satisfy the EMI standard or the CMV cancellation approach can be adopted in the multilevel inverter [86]-[102]. However, the EMI emission above 10 MHz, generated by the high dv/dt, cannot be attenuated by the first stage of the EMI filter designed for the low frequency attenuation, due to the effect from the parasitic inductance and capacitance within the filter inductors and capacitors. To this end, a second stage filter targeting high frequency (>10 MHz) attenuation is needed or the active gate driver can be adopted.

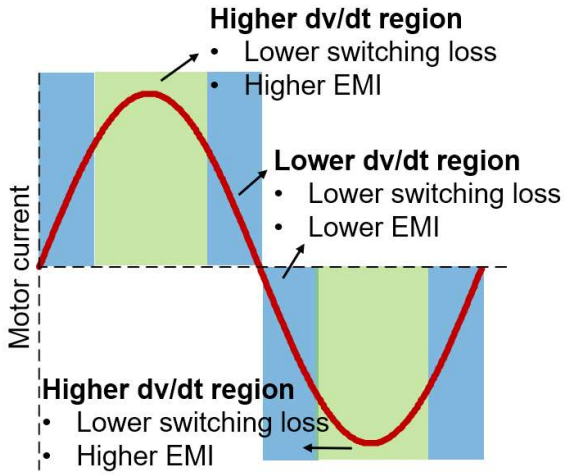


Fig. 4-1 Active dv/dt control strategy for CM EMI reduction

To attenuate high frequency CM emission within the three-phase inverter with minimum penalty of the switching losses, the general idea is described in Fig. 4-1. As evinced in Fig. 4-1, when the sinusoidal motor current reaches its high current region, the switches with the active gate driver would switch with a high dv/dt, rendering low switching loss and high CM EMI emission. When the output motor current reaches the low current region, a low dv/dt

contributes low CM EMI emission with small switching loss. In this operation strategy, the inverter benefits from the low CM emission in the low current region, with little switching loss increased. This method has been verified effective with Si-IGBT-based three-phase inverter in [61].

This chapter proposes a novel gate control schematic to control the dv/dt of the 650V GaN devices by extending the equivalent miller plateau period into different duration. The method has significantly short response time and free flexibility to change dv/dt during turn on and turn off while the device is running. The idea of how to extend miller plateau duration is explained first, and followed by the proposed turn-on and turn-off control circuit with detailed design. The LTspice simulation circuit was built according to the experimental hardware, considering all the possible parasitics, to verify the control circuit function and check how the transient changes with the commands. Further, the circuit design is explained in detail, including the device selection and design of the magnitude-varying voltage source. Finally, the double pulse test (DPT) on the 650 V 30 A GaN HEMT with the active dv/dt control is performed at 300 V dc and 15 A load current. The transient waveforms with different dv/dt are compared, and compared with the transient waveforms with different gate resistance to exhibits the benefits of the proposed method.

4.1 Proposed dv/dt Control Technique

4.1.1 Idea to control dv/dt

The simplified switching transient behavior for Si device, such as MOSFET is explained in detail in [103][104]. For a MOSFET or HEMT, the miller plateau duration, the charging and discharging period of C_{DG}, dominates the dv/dt slope during turn-off and turn-on. The idea to change dv/dt by changing the miller plateau duration can be described in Fig. 4-2.

First one extra capacitor C_M is connected between the drain and the gate of the device under test (DUT), rendering an equivalent miller capacitance C_M+C_{DG}. With the same driving current of the gate driver and the load current, the discharging/charging current for C_M+C_{DG} is the same as the case for C_{DG}, which is only dependent on the turn-on/off driving voltage V_{CC}/V_{EE}, the miller plateau voltage V_{miller} and the gate resistor R_g as it is estimated in (4.1) and (4.2). The miller plateau voltage V_{miller} is related to the threshold gate voltage V_T, the device transconductance g_m (A/V), and the drain current (load current) I_D, as (4.3) shows. The equivalent miller plateau duration can be estimated in (4.4) and (4.5), where V_{DC} is the bus voltage. Based on (4.1)-(4.5), the miller plateau duration is extended to t_{o_on}, t_{o_off} with an extra C_M and the dv/dt is reduced to the values in (4.6) and (4.7). The simplified switching waveforms with C_M is plotted in green curve in Fig. 4-3, compared with the waveforms without C_M. With one fixed C_M, there is only one fixed reduced dv/dt.

$$I_{CDG\_on} \approx \frac{V_{CC} - V_{miller}}{R_g} \tag{4.1}$$

$$I_{CDG\_off} \approx \frac{V_{miller} - V_{EE}}{R_g} \tag{4.2}$$

$$V_{miller} \approx V_T + \frac{I_D}{g_m} \tag{4.3}$$

$$t_{o\_on} \approx \frac{V_{DC}(C_{DG} + C_M)}{I_{CDG\_on}} \tag{4.4}$$

$$t_{o\_off} \approx \frac{V_{DC}(C_{DG} + C_M)}{I_{CDG\_off}} \tag{4.5}$$

$$\frac{dV_{on}}{dt} = \frac{V_{DC}}{t_{o\_on}} \approx \frac{I_{CDG\_on}}{(C_{DG} + C_M)} = \frac{V_{CC} - V_{miller}}{R_g(C_{DG} + C_M)} \tag{4.6}$$

$$\frac{dV_{off}}{dt} = \frac{V_{DC}}{t_{o\_off}} \approx \frac{I_{CDG\_off}}{(C_{DG} + C_M)} = \frac{V_{miller} - V_{EE}}{R_g(C_{DG} + C_M)} \tag{4.7}$$

In order to have a varying and controllable dv/dt slope, a varying and controllable driving current is expected, which is depicted in Fig. 4-2. The current-controlled current source is connected between the gate and the ground (or Kevin pin), whose multiplying coefficient A varies from zero to one or larger. Equipped with the current-controlled current source, the equivalent C_M added into the system is (1-A)C_M. The corresponding dv/dt can be estimated in (4.8) and (4.9).

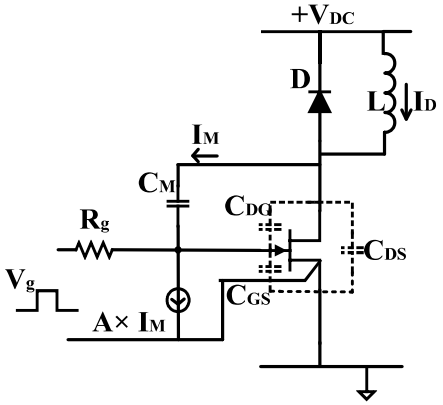


Fig. 4-2 Circuit to achieve a varying and controllable dv/dt

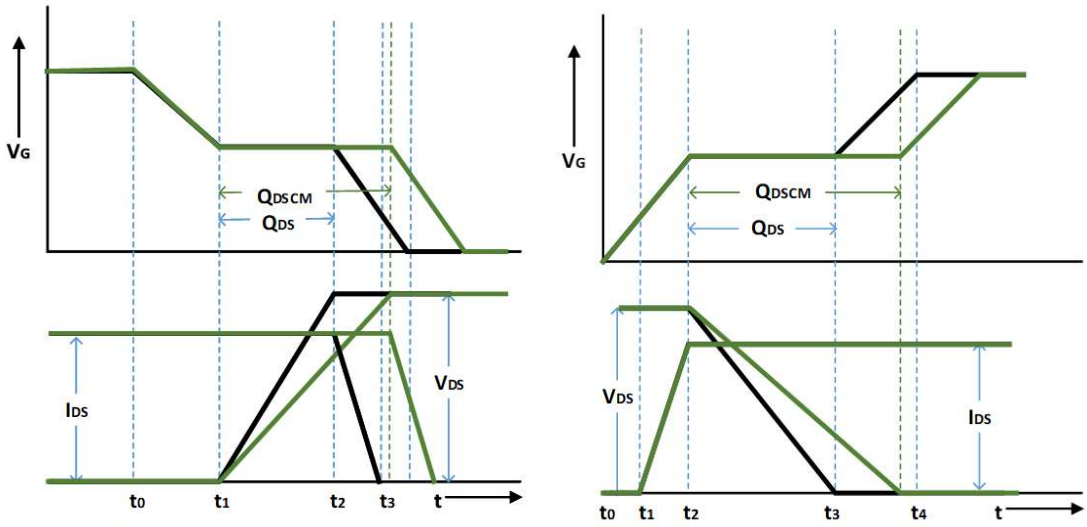


Fig. 4-3 Simplified turn-off (left) and turn-on (right) waveforms with the extra Miller capacitor C_M

$$\frac{dV_{off}}{dt} = \frac{V_T + \frac{I_D}{g_m} - V_{EE}}{R_g(C_{DG} + (1-A)C_M)} \tag{4.8}$$

$$\frac{dV_{on}}{dt} = \frac{V_T + \frac{I_D}{g_m} - V_{CC}}{R_g(C_{DG} + (1-A)C_M)} \tag{4.9}$$

When A is equal to 0, it is the same as the case where there is no current-controlled current source equipped. The turn-off waveforms in this case, shown in red dash line in Fig. 4-4 is the same as the cases with C_M only, represented as green solid line in Fig. 4-4. When A is equal to 0.5, the 50% of the current of CM is flowed into the current-controlled current source and the rest of the current propagates through the gate driver. To this end, the equivalent miller capacitor is C_{DG}+0.5C_M. The dv/dt in this case, depicted in yellow dash line in Fig. 4-4, slows down compared with the dv/dt in Case 'A=0', but still larger than the original dv/dt, represented in the black solid line in Fig. 4-4. When A is larger than 1, for example 'A=1.2', the equivalent miller capacitor is C_{DG}-0.2C_M, rendering a faster turn-off dv/dt compared with the device original value. The simplified switching waveforms in this case is shown in Fig. 4-4 as the blue dash line. From the circuit point view, the case with 'A>1' is equivalent to the condition that there is an extra driving current source connected from the gate to the source to charge C_{DG}. To ensure the device switching operation, the maximum value for A should be smaller than $1+\frac{0.5C_{DG}}{C_M}$.

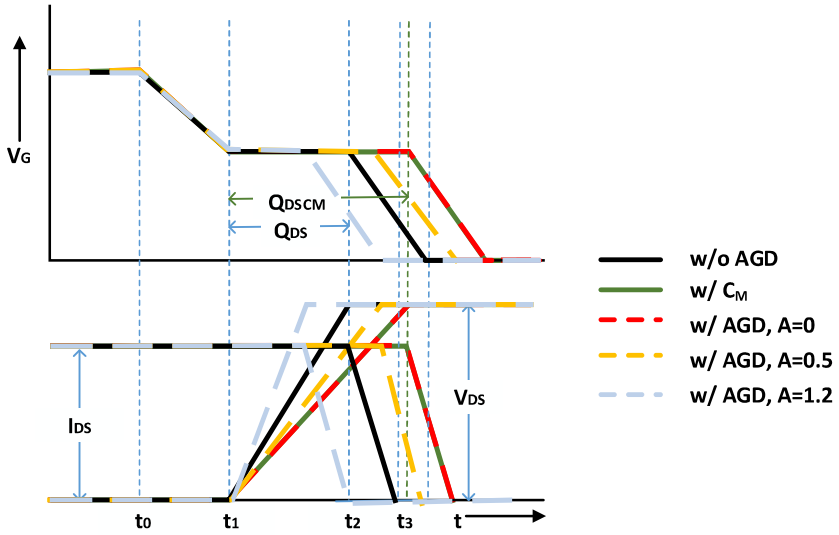


Fig. 4-4 Simplified turn-off waveforms with the active gate driver

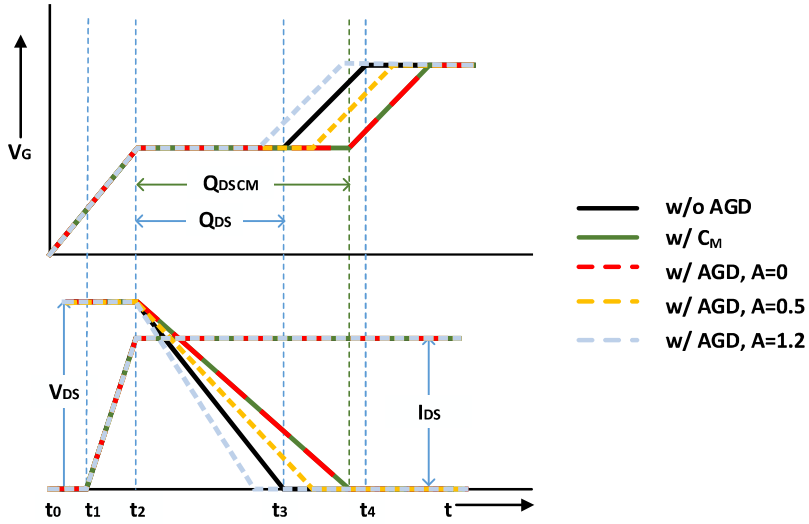


Fig. 4-5 Simplified turn-on waveforms with the active gate driver

The simplified turn-on waveforms for Case 'A=0', 'A=0.5', 'A=1.2' are depicted and compared in Fig. 4-5, in red dash line, yellow dash line and blue dash line respectively. For Case 'A=0', the waveforms matches with the case where only C_M is equipped and the dv/dt slows down to the minimum value. While A is larger than 1, the turn-on dv/dt with the active gate driver can be faster than the original value.

Compared with the real cases, the equations above can provide a close estimation to the dv/dt but they are not accurate enough as the dynamic dv/dt is dependent on several non-linear factors, such as the parasitic C_{DG}, the transient miller plateau voltage, parasitic inductance within the gate loop.

4.1.2 Proposed turn-off control circuit

The proposed circuit to implement the current-controlled current source for turn-off is illustrated in Fig. 4-6. There are one PNP, three NPN BJTs and one voltage source V_1. With the controlled source V_1, the Q_1 current I_{Q1} is αI_M. Q_2 works a freewheeling diode, which conducts $(1-\alpha)I_M$ current. Q_3 and Q_4 work as a mirror circuit, where Q_4 current I_{Q4} copies Q_3 current I_{Q3}. As a result, I_{Q4} is equal to I_{Q1} (αI_M). Q_4 works as the current-controlled current source in Fig. 4-2, where A is equal to $\frac{1-\alpha}{\alpha}$. α is controlled by V_1.

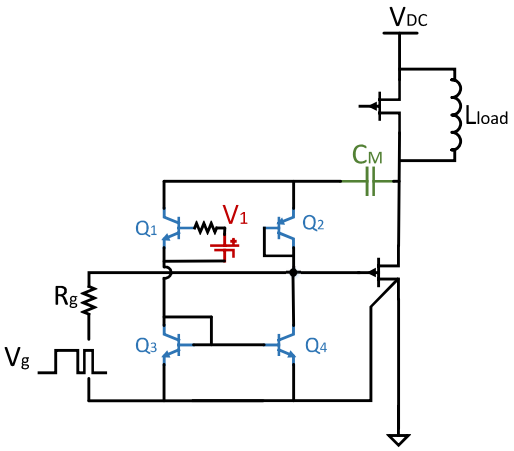


Fig. 4-6 Proposed turn-off dv/dt control circuit.

If V_1 is zero, and fully turns off Q_1, there is '$I_{Q4}=I_{Q3}=I_{Q1}=0$' and '$\alpha=1$'. All the charging current in C_M flows through the gate resistor R_g, leading to the slowest dv/dt. If V_1 is 0.7 V or higher, enabling Q_1 channel conducted, A is within the range of 0 to 1, rendering a

higher dv/dt. When V_1 is large enough that I_{Q1} is larger than $0.5I_M$, operating as Case 'A>1', I_{Q4} is larger than I_{Q2} as a result and Q_4 also works as the miller clamp capacitor which increases the driving capability, enabling a faster turn-off dv/dt than the original value.

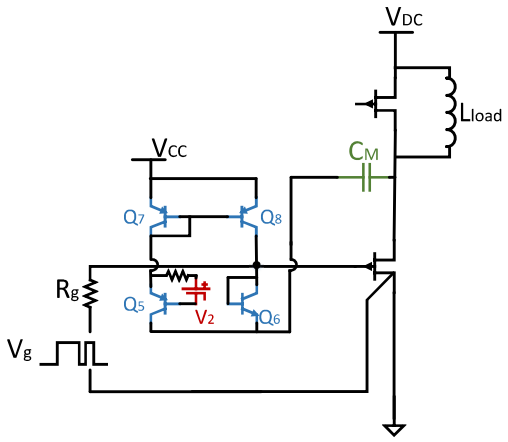


Fig. 4-7 Proposed turn-on dv/dt control circuit.

4.1.3 Proposed turn-on control circuit

As for turn-on dv/dt control, it is expected to vary the dv/dt, independent from turn-off circuit. Therefore, the turn-on active control requires an independent current-controlled current source from the turn-off one. Similarly to the turn-off circuit, the turn-on current-controlled current source circuit, illustrated in Fig. 4-5, utilizes one NPN BJT (Q_6), three PNP BJT (Q_7, Q_8, Q_5) and one control voltage source V_2. Q_5 operates in the same role as Q_1 in the turn-off circuit in Fig. 4-4. Q_7 and Q_8 compose the mirror circuit and therefore the Q_8 current I_{Q8} equals to Q_5 current I_{Q5}. I_{Q5} is controlled to be $(1-\beta)I_M$ by V_2 and A in the turn-on circuit is equal to $\frac{1-\beta}{\beta}$.

The complete active gate driver for the turn-on and turn-off control is illustrated in Fig. 4-8. C_M charges during turn-off and discharges during turn-on. The turn-on and turn-off circuits can be adopted separately. For example, the turn-off circuit is applied to dynamic voltage balancing

for fast-switching SiC MOSFETs in series [105] without adoption of the turn-on circuit. To ensure the operation for the turn-off circuit, it is essential to have Q_6 to discharge C_M during turn-on.

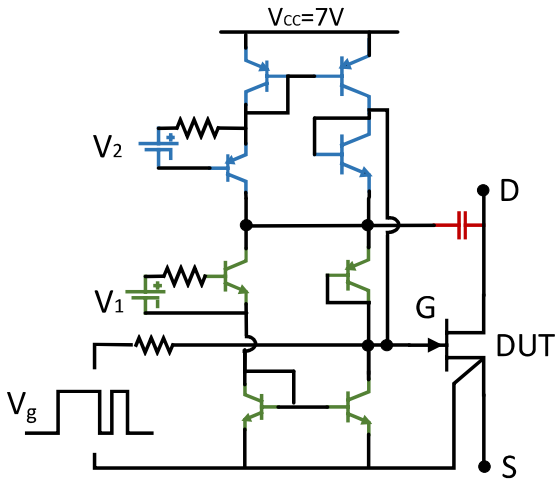


Fig. 4-8 Complete circuit of the proposed active gate driver for GaN HEMT

V_1 and V_2 are two isolated voltage sources, whose magnitude varies from 0 V to 2 V, such as 0.1 V, 0.5 V and 1 V. V_1 should be on with the desired magnitude during DUT is off and fully off (0V) during DUT turn-on because V_1 pulls down the gate voltage to 0V gradually once it is on. As for V_2, it has the same timing as V_g, which mean V_2 turns on and off with V_g. The gate can be pulled to 7V unless V_2 is off during DUT turn-off. The logic between V_1, V_2 to V_g is illustrated in Fig. 4-9.

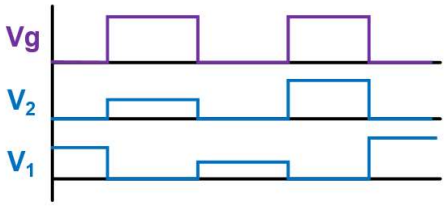


Fig. 4-9 Logic between V_1, V_2 and V_g

4.1.4 Simulation verification

The DPT setup, in Fig. 4-10, is first built to evaluate the 600 V 30 A GaN device in the phase leg, with 5 Ω gate resistor without the active dv/dt control. The bottom device is DUT, and the top device works as a free-wheel diode. The gate to source voltage V_{gs}, drain to source voltage V_{ds} and the drain to source current I_{ds} were measured. The phase leg in DPT PCB board layouts in a vertical way to achieve an ultra-low power loop inductance, illustrated in Fig. 4-11. The parasitic inductance from the PCB trace in the power loop is 3 nH, simulated by the Q3D Extractor. With 2 nH inductance from the current shunt, the total power loop inductance is 5 nH, as the simulation circuit in Fig. 4-12 shows. The device model comes from the manufacture. The DC bus decoupling capacitor parasitics - equivalent series inductance (ESL) and resistance (ESR) - are also taken into considered in the model. The model of the load inductor is curve-fitted to the inductor impedance measurements up to 30 MHz.

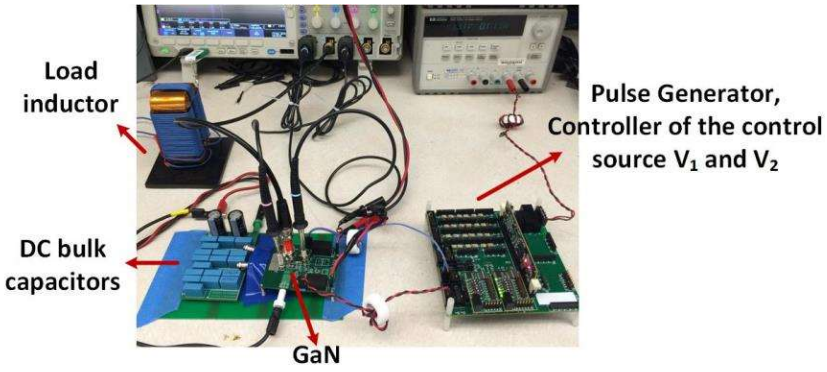


Fig. 4-10 DPT setup with the active gate driver

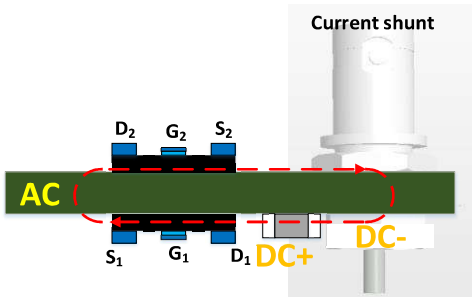


Fig. 4-11 Vertical layout of a phase leg GaN to achieve ultra-low power loop inductance.

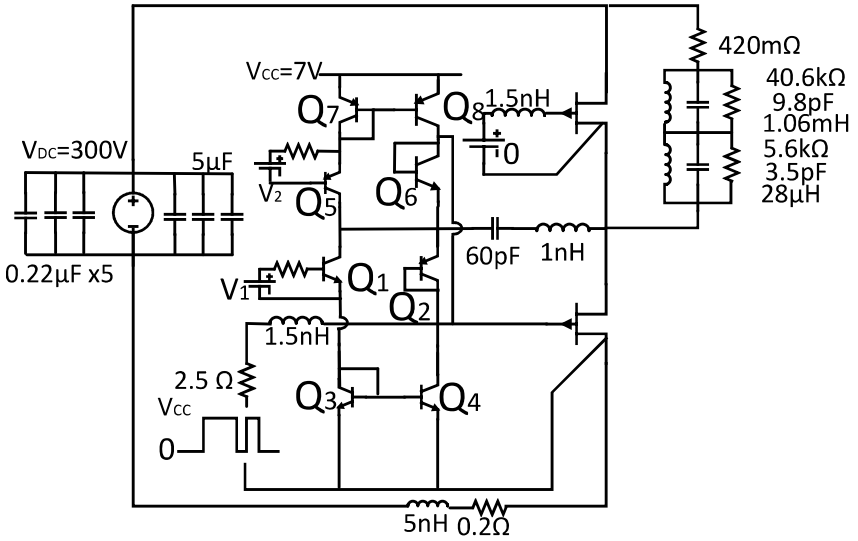
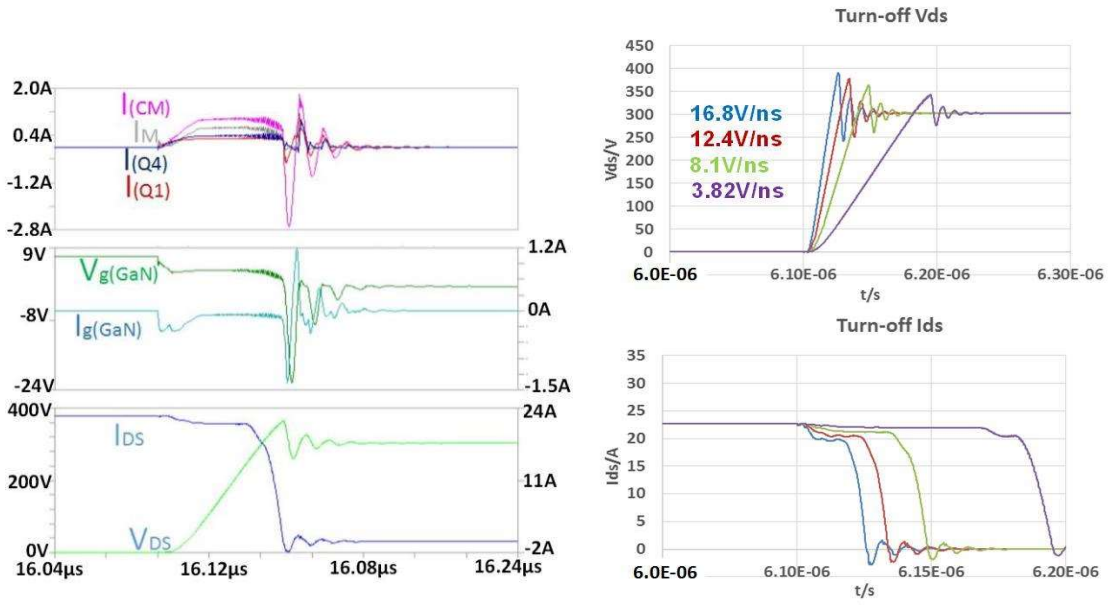


Fig. 4-12 Simulation circuit with the active control circuit.

Another important parasitics in the setup are situated at the DUT gate. The gate drive chip locates as close as to the gate, 1.5 nH inductance in the gate loop. This value comes from the Q3D Extractor simulation with the inserted 3D PCB trace file.

The active control BJTs are also added in the simulation to verify its function. All the BJTs utilize the spice models of the selected devices. C_M is selected as 60 pF, whose ESL is 1 nH from its package and the PCB connection trace. 1 nH inductor is added around each BJT to emulate the possible ESL comes from the PCB layout. V_1, V_2, and V_g are ideal voltage sources, whose parasitics have less influence on V_{gs}.

The transient current of Case 'A = 0.5' is shown in Fig. 4-13 (a). In the graph, during the miller effect time, the gate voltage is flat and C_M charges. I_{Q1} is half of I_{Q2}. I_{Q4} is very close to I_{Q1} (I_{Q1} = I_{Q3}), but not completely equal to I_{Q1} because the mirror circuit is not ideally symmetric. It is because the emitter-collector voltage V_{CE} of Q_3 cannot be exactly equal to that of Q_4. However, this error does not affect the circuit function. Additionally, the parasitics from the turn-off BJT circuit cause small high frequency oscillation at the gate, as well as among the BJTs. However, the gate voltage keeps within SOA during the turn-off transient. Fig. 4-13 (b) compares the waveforms of different dv/dt at turn-off ranging from 3.83 V/ns to 16.8 V/ns, with almost the same di/dt. V_1 ranges from 0V to 2V in the four cases.

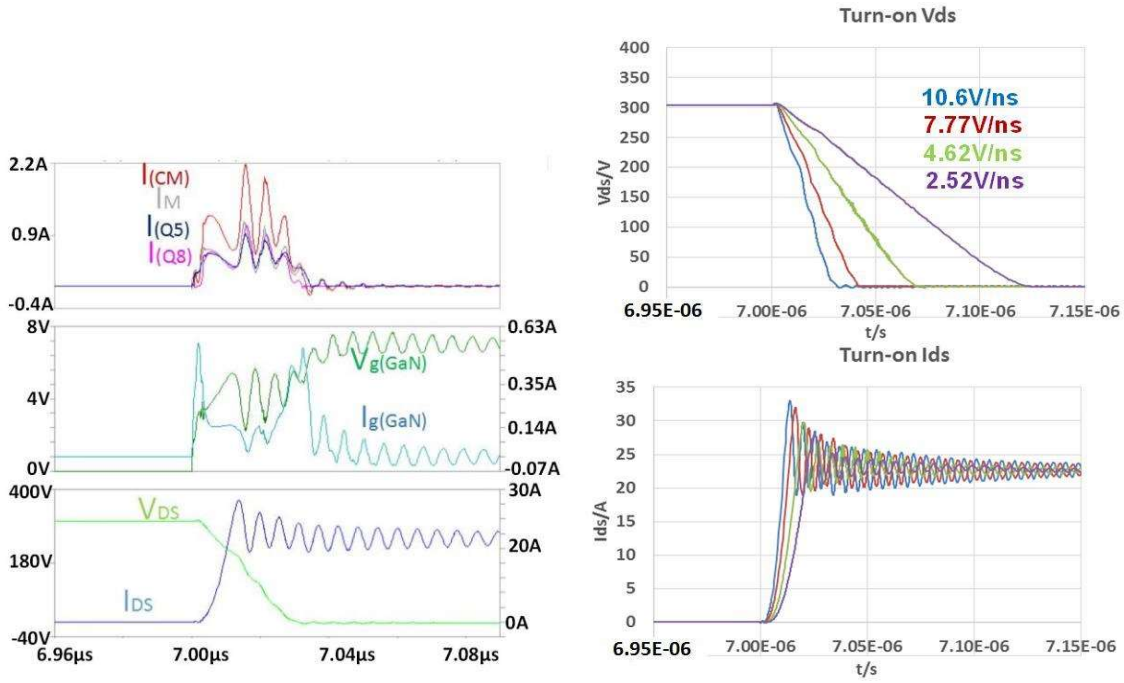


(a) (b)

Fig. 4-13 (a) transient waveform in active circuit during turn-off; (b) the turn off waveforms with different dv/dt.

Fig. 4-14 (a) displays the transient waveforms in the active turn-on control circuit with 'A = 1', which matches the theoretical explanation in the previous section. The different turn-on dv/dt waveforms are compared in Fig. 4-14 (b). It is found that the turn-on circuit can control

the turn-on slope freely and does not influence the di/dt too much. The parasitics from the turn-on loop cause oscillation with 7.8V peak but the gate keeps within SOA.



(a) (b)

Fig. 4-14 (a) transient waveform in active circuit during turn-on; (b) the turn off waveforms with different dv/dt.

With the simulation results above, the active gate driver is verified to be able to control dv/dt effectively by changing V_1 and V_2 magnitude. The circuit design is explained in detail in the next section.

4.2 Circuit design

4.2.1 BJT selection and layout consideration

First though an integrated chip is a better solution, the discrete BJTs are utilized to realize the proposed method considering the cost and feasibility. To control the capacitor charge of a GaN device during the fast switching transient, the all BJTs should have a total turn-on time

shorter than 10ns. The bandwidth should be high enough for the mirror circuit to follow the I_M current change, which is at least 200 MHz. From the simulation, the largest BJT current is around 1.5 A and the largest V_{CE} among all the BJTs is 20 V. Above all, CPH3215 and CPH3115 are finally selected as NPN and PNP transistors separately, whose parameters are shown in Table 4-1.

Table 4-1 Selected BJT Characteristics

	Bandwidth /MHz	***Max I_c /A***	***Max V_{CE} /V***	***C_o /pF***
Requirements	200	1.5	>20	smallest
CPH3115	500	1.5	30	8
CPH3215				

To reduce PCB parasitic inductance around BJTs, all the BJTs locate as close to the DUT gate as possible. Q_5 ~Q_8 layout on the bottom layer and the same area at the top layer locate Q_1~ Q_4. Q_2, Q_4, Q_6 and Q_8 are placed nearest to the gate because of their direct connection to the gate. The gate drive source V_{CC} (7 V) and ground are distributed in the PCB middle layers to cancel partial trace inductance.

4.2.2 Control source circuit design

The requirements of the control sources V_1 and V_2 includes synchronization with V_g, depicted in Fig. 4-9, a controlled and variable magnitude, and a floating ground. The circuit is depicted in Fig. 4-15. V_{DD} (3.3 V) comes from an isolated converter, creating an isolated ground. The digital signal carrying magnitude information goes to the digital-to-analog convertor (DAC) after a digital isolator. The amplifier next to the DAC operates as a voltage follower to provide maximum 50 mA to control the BJT base. The gate signal after a digital

isolator controls the analog switch to generate the pulse between zero and the desired magnitude. In order to update the DAC output, 2 µs at least is required. Therefore, the V_1 or V_2 magnitude can update as fast as 500 kHz. However, there is no necessity to change dv/dt within 2 µs. For example, the five different dv/dt values are distributed in a line cycle (50 Hz) in a three-phase inverter topology Fig. 4-1. The update rate in this case is 2 ms, much longer than 2 µs.

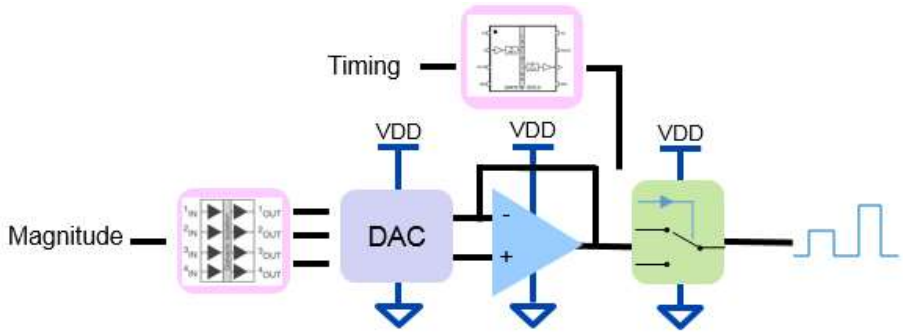
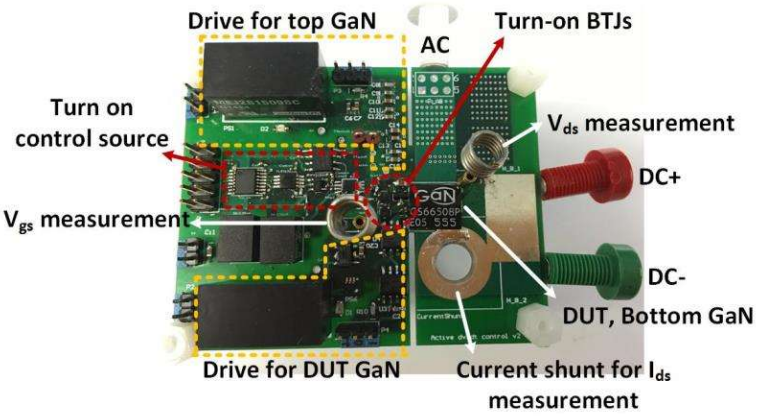


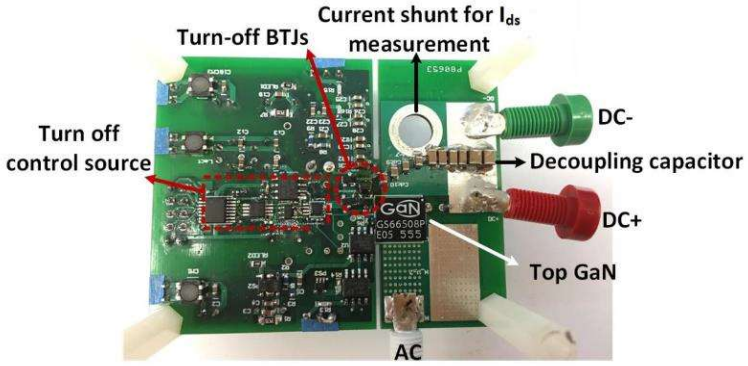
Fig. 4-15 Proposed control source circuit for V_1 and V_2, where 'Magnitude' and 'Timing' are digital signals.

A resistor-capacitor delay circuit can be added before the timing isolator, adjusting the output to compensate the time delay between V_g and V_1 and V_2, considering that the analog switch output is 70 ~ 90 ns faster than the gate driver.

Fig. 4-16 illustrates the test board with the one phase leg of GaN devices, the measurement placements, the gate drivers, the selected BJT, V_1, and V_2. In this PCB board, only the bottom device (DUT) owns the active dv/dt control.



(a)



(b)

Fig. 4-16 Hardware for Double pulse test with active dv/dt control circuit (a) top view; (b) bottom view.

4.3 Experimental Verification of Active Gate Driver

4.3.1 DPT with C_M without BJT

Before experiments with the active dv/dt control, the DPT with different C_M without BJTs is performed to evaluate how C_M affects dv/dt.

Fig. 4-17 shows turn-on transient waveforms at 150V dc 8 A load current with 22 pF C_M. A very large ringing is captured at gate, caused by oscillation between C_M and its ESL. This spike could break down gate if a higher dc voltage is pushed. In order to attenuate the oscillation, one damping resistor R_M is added in series with C_M, highlighted in Fig. 4-18. Fig.

4-19 (a) and (b) show separately the turn-on and turn-off waveforms at 300 V DC and 10 A load current and 22 Ω R_M, 47 pF C_M. With the fully attenuated gate oscillation, the average turn-on dv/dt is 9.77 V/ns while the average turn-off dv/dt is 6.3 V/ns. The extended miller plateau period is clearly seen in the graphs. The larger current overshoot 42 A in Fig. 4-19 (a) is not caused by C_M. A larger value in the same DPT condition without C_M was captured. The PCB board introduces extra capacitance between the positive DC bus and AC, as larger as 400 pF, because of the closely overlapped copper layers.

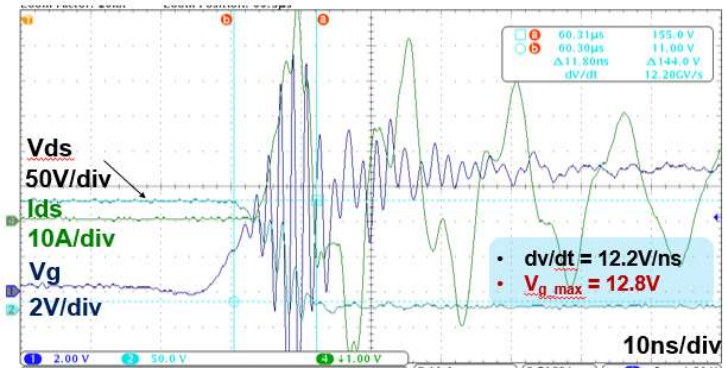


Fig. 4-17 Turn-on waveforms with C_M without BJTs at 150 V dc, 8 A, C_M = 22pF, R_M = 0;

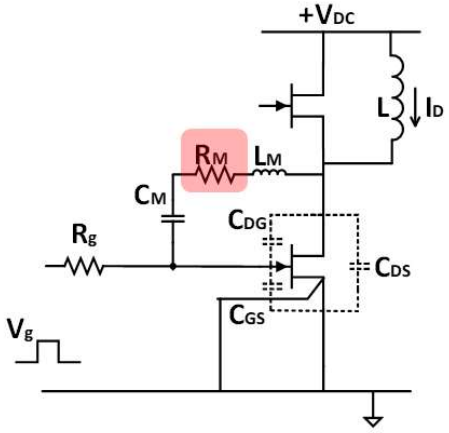
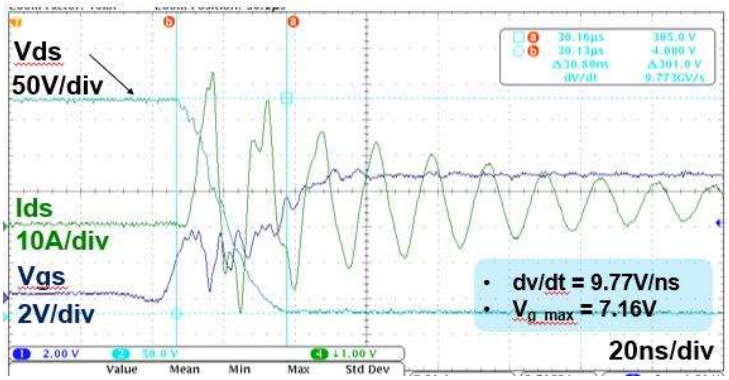
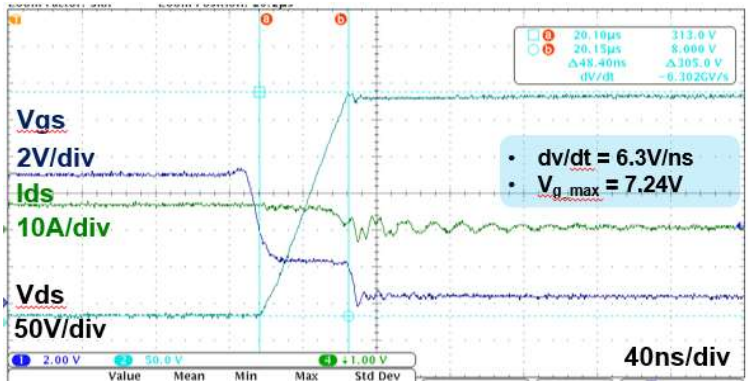


Fig. 4-18 R_M added to attenuate the gate oscillation induced by C_M



(a)



(b)

Fig. 4-19 DPT results with C_M without BJTs: (a) turn-off (b) turn-on waveforms at 300 V dc, 8 A, C_M = 47pF, R_M = 22 Ω.

With the experiment, it is also observed that a smaller R_M cannot fully damp the oscillation and a significant increase driving loss comes with a large R_M, which is also simulated and summarized in Table 4-2. Moreover, it is found that, with a larger R_M, the turn-on current overshoot is lower and the turn-on switching loss decreases. This is because R_M increases the turn-on current ringing loop (through the gate) impedance at high frequency. It is also found that R_M does not influence dv/dt in simulation and in experiments (300 V dc) significantly, because the C_M impedance is dominated in the related frequency range. R_M is finally selected as 22 Ω to avoid the gate oscillation and have a relatively smaller driving loss.

Table 4-2 Simulated Loss Analysis with Different R_M

	R_M /Ω	Vds x Ids /μJ	R_g loss /nJ	R_M loss /nJ
Turn on	4.7	41.726	122.7	169.92 (ringing)
	10	41.607	71.847	78.203
	22	40.892	71.476	170.36
	50	39.34	70.902	355.52
Turn off	4.7	36.327	70.079	44.537
	10	36.295	68.535	84.126
	22	36.203	67.348	166.34
	50	36.178	66.207	333.25

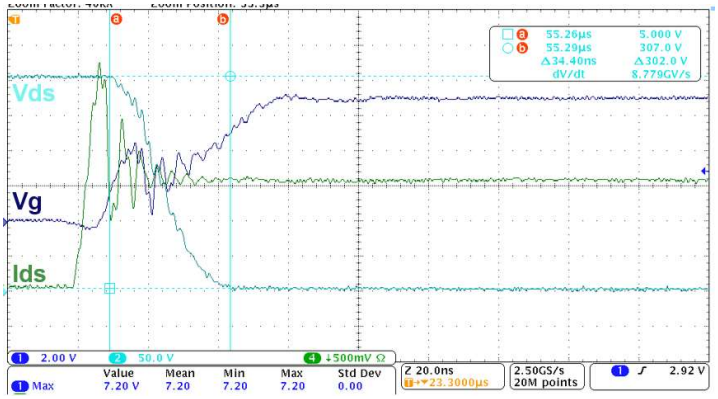
4.3.2 DPT with different dv/dt at turn-on with active dv/dt control

The DPT at 300 V dc, 15 A load current, 5 Ω gate resistor is performed with active dv/dt control, 47 pF C_M, and 22 Ω R_M. Fig. 4-20 shows the turn-on transient waveforms with different V_2 magnitude. V_2 (and V_1) magnitude is controlled by the DSP controller, shown in Fig. 4-10. With V_2 ranging from 0 V to 1.6 V, dv/dt varies from 8.8 V/ns to 27.1 V/ns. The gate voltage is suppressed under 8V in all cases. The switching energy is calculated in Table 4-3. From Table 4-3, with a 3 times higher dv/dt, the turn-on switching energy only decreases 24% given thay the switching energy is dominated by the current-increasing duration before the voltage drops. The maximum current peak values are also listed in Table 4-3. It is observed that with a higher dv/dt, the overshoot is larger.

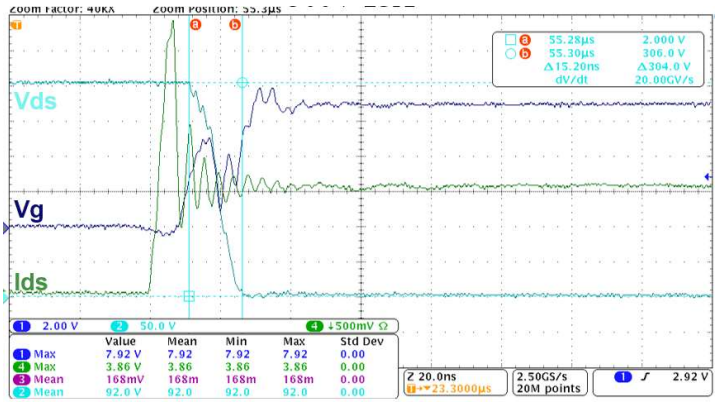
Table 4-3 V_1 and V_2 vs dv/dt

	V /V	dv/dt V/ns	Vds x Ids /μJ	Ids-max /A
Turn on: V_2	0	8.78	133.2	32.2
	0.78	15.61	115	38.3

	V /V	*dv/dt V/ns*	*Vds x Ids /µJ*	*Ids-max /A*
	1.1	20	110.8	39.2
	1.6	27.11	101.2	45
Turn off: V_1	0	7.628	39	---
	0.85	11.84	9.16	---
	1.1	16.19	3.7	---
	1.8	34.67	2.86	---



(a)



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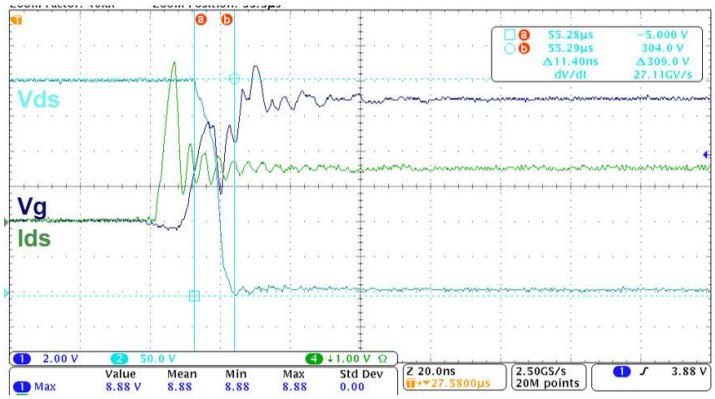
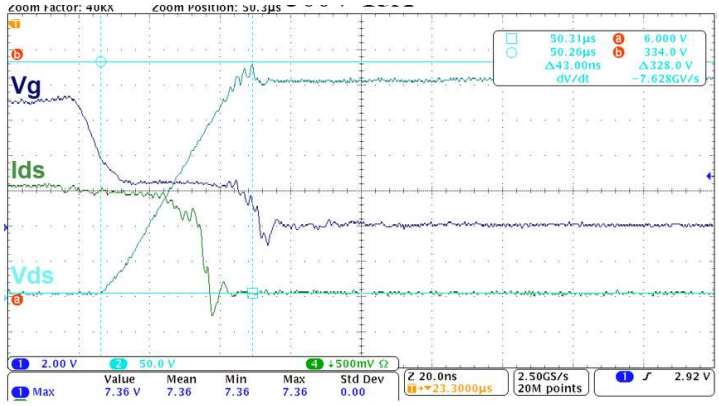


(c)

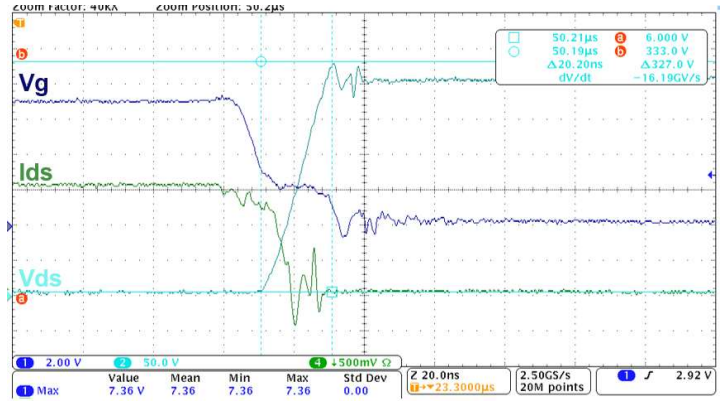
Fig. 4-20 DPT turn-on waveforms at 300 V dc 15 A load current with active dv/dt control (a) V_2 = 0 V; (b) V_2 = 1.1 V; (b) V_2 = 1.6 V.

4.3.3 DPT with different dv/dt at turn-off with active gate control

Fig. 4-21 shows the turn-off waveforms with the active gate control in the same working condition as Fig. 4-20. The turn-off dv/dt goes down to 7.6 V/ns and up to 34.7 V/ns when V_1 changes from 0V to 1.8 V. The turn-off energy values in different cases are listed in Table 4-3. With 5 times difference of dv/dt, the turn-off energy has more than 14 times difference given that the Ids decreases almost after V_{ds} increases to half dc voltage. It is also found that the average di/dt of the three cases keeps almost constant, which verifies the independence between the proposed dv/dt control and the device di/dt.



(a)



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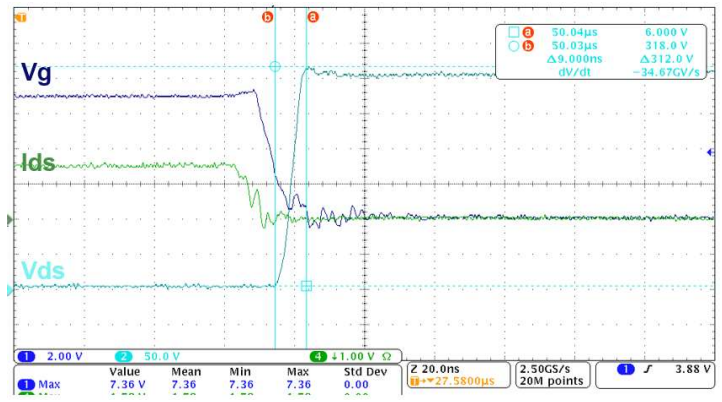


(c)

Fig. 4-21 DPT turn-off waveforms at 300 V dc 15 A load current with active dv/dt control (a) V_1 = 0 V; (b) V_1 = 1.1 V; (c) V_1 = 1.8 V.

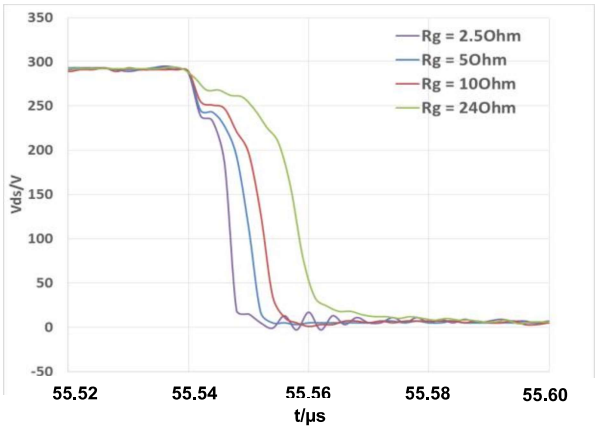
4.3.4 Comparison on DPT between with the proposed method and with different gate resistance

In order to locate the dv/dt capability of the active dv/dt control, the DPTs at 300 V dc, 15 A load current, and with different gate resistances, without the C_M and the active control are performed. The average dv/dt and the switching energy are listed in Table 4-4, as a comparison of those in Table 4-3. In terms of the turn-on dv/dt, the active dv/dt control (C_M = 47 pF, R_M = 22 Ω, R_g = 5 Ω) can achieve 27.1 V/ns, which is higher than that using the 5 Ω gate resistor, which verifies the feasibility of the proposed active gate driver to speed up the dv/dt. Furthermore, it is observed that the turn-on loss using the active control with 20 V/ns dv/dt is

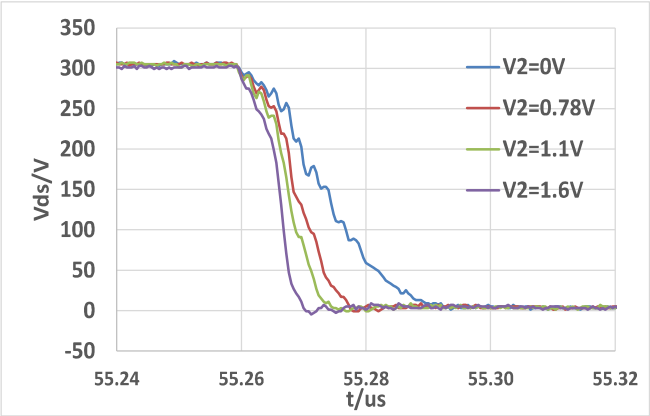
110.8 μJ, which is 2.1 μJ smaller than that using the 5 Ω gate resistor with a faster dv/dt slew rate (22.58 V/ns). This is because the active control can reduce the current overshoot, which reduces more turn-on loss than the loss increased by the lower dv/dt. As for the turn-off dv/dt, the fastest dv/dt of the active control is 34.7 V/ns, which is 4.9 V/ns slower than that using a single 5 Ω gate resistor, due to the limited Q_1 emitter current. The slowest turn-on dv/dt is 8.78 V/ns, and the slowest turn-off dv/dt 7.63 V/ns, far smaller than those using a 24 Ω gate resistor.

Table 4-4 R_G vs dv/dt

	Rg /Ω	***dv/dt V/ns***	***Vds x Ids /μJ***
Turn on:	24	12.57	154.6
	10	16.8	124.2
	5	22.58	112.9
	2.5	42.14	71.4
Turn off:	24	14.95	16.8
	10	25	3.29
	5	39.6	1.86
	2.5	42.14	0.7



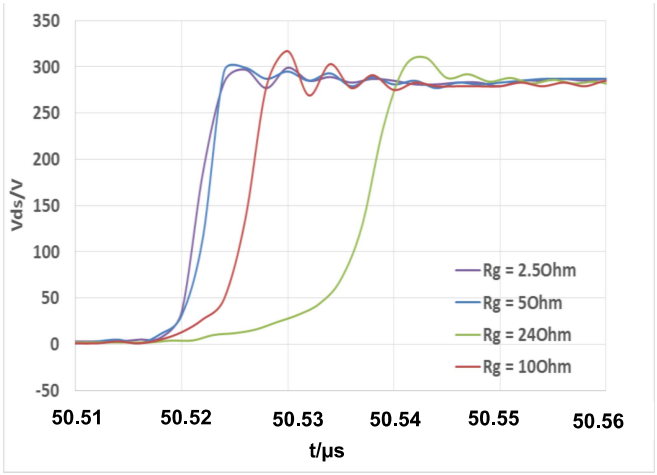
(a)



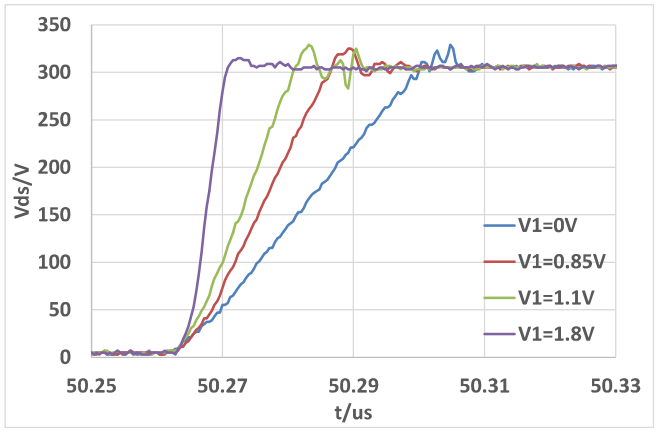
(b)

Fig. 4-22 DPT turn-on V_{ds} waveforms at 300 V dc 15 A load current (a) with different gate resistors, (b) with active gate driver.

Fig. 4-22 and Fig. 4-23 compare how dv/dt changes with different gate resistors, and with active gate control. Firstly, the active gate control does not affect turn-on di/dt as significantly as the gate resistor, according to the initial voltage drop induced by the di/dt and the loop inductance, depicted in Fig. 4-22. Then at turn-off waveforms in Fig. 4-23, a larger gate resistor attenuates the V_{ds} slope under 50 V. This results from the non-linear C_{DG}, which is larger than 10 times larger under 50V than under 400V. Above 50V, dv/dt keeps constant, which means high dv/dt is not truly attenuated. As for the V_{ds} slope with active gate control, it is constant in the miller plateau duration in each case. Additionally, the active gate control does not extend the delay time when dv/dt decreases thanks to the nature of the dv/dt control approach.



(a)



(b)

Fig. 4-23 DPT turn-off V_{ds} waveforms at 300 V dc 15 A load current (a) with different gate resistors, (b) with active gate driver.

4.4 Summary and Conclusions

This section introduced the proposed a novel active gate control circuit dedicated to the e-mode GaN HEMT, which could change turn-on and turn-off dv/dt in wide range and independently. The circuit was carefully designed and tested. Both simulation and experiments are performed to verify the dv/dt varying capability of the proposed methods, which ranges 8.7 V/ns to 27.1 V/ns during turn-on and ranges from 7.6 V/ns to 34.7 V/ns during turn off.

Compared with the active gate driver design for Si device in [58], the proposed approach for GaN HEMTs has a wider dv/dt varying range. In addition to the ability to slow down the dv/dt, the latter can speed up both the turn-on and turn-off dv/dt, which increases the functionality of the active gate driver. Furthermore, the proposed circuit was designed with a simpler circuit with less components. In total of the turn-on and turn-off circuit, the proposed approach has eight BJTs and two control sources, which is almost half of the device number of the Si approach. With the careful selection of the BJTs, the active gate driver can capture the fast transient current from the miller capacitors and respond within 5 ns. It was found as well that the proposed active gate control helps attenuate the current overshoot during turn-on and the delay time is almost constant with varying dv/dt. The advantages above are summarized and compared with the Si approach in Table 4-5.

Table 4-5 Comparison between the active gate driver for Si with the proposed approach for GaN HEMT

	Solution for Si	*Proposed solution for GaN*
Original dv/dt speed (V/ns)	On: 1.8	On: 22.58
	Off: 2.3	Off: 24.75
Total BJT No.	12	8
BJT Bandwidth	10 MHz	500 MHz
Control source No.	4	2
dv/dt varying range (nominal at original speed)	On: 0.28 - 1	On: 0.38 – 1.2
	Off: 0.3 - 1	Off: 0.3 – 1.4
Effect from parasitics	Little	Device is very sensitive

As a penalty of adding an external miller capacitor C_M in parallel with the GaN HEMT in the proposed approach, it was found in the experiments that C_M introduced a large oscillation at the gate. The proper solution was to add a series resistor R_M with C_M to damp the resonance

between C_M and its ESL. R_M is not necessary for C_M with Si and even SiC devices in [58] and [105] respectively thanks their relatively larger C_{DG} and larger gate SOA.

Chapter 5. Design and Analysis of 650 V 12.5 mΩ / 6.25 mΩ Half Bridge Using Paralleled GaN HEMTs

To switch the paralleled 650 V 60 A e-mode GaN HEMTs faster, this chapter proposes a more compact power loop layout for two and four paralleled devices, whose gate loop also shrinks more than a half compared with the state of the art. The symmetry in the gate loop is achieved with only 0.1 nH difference for the turn-on loops, and 0.02 nH difference for the turn-off loops between the paralleled devices. Thanks to the symmetry, 1 Ω gate resistor can be adopted to turn on the devices, reducing switching loss by half compared with that of 5 Ω gate resistor. Furthermore, a complete thermal solution is provided with the thermal resistance evaluation. With the quantified thermal resistance, the device temperature is controlled under 80 ˚C. Furthermore, the gate oscillation observed during double pulse tests are emulated based on a proposed simplified equivalent circuit. With this circuit, the main commutation between the paralleled devices is discussed and the gate oscillation is assessed considering the different gate resistor, the difference of gate loop inductance and the device parasitic capacitor tolerance. A full design consideration is provide in the end to parallel the devices in question.

To provide a comprehensive analysis and application consideration of paralleling 650V GaN HEMTs, the chapter first presents the proposed minimized and symmetric layout of paralleling two and four GaN HEMTs. With this designed switching cell, the corresponding thermal solution is illustrated. To evaluate the performance of the switching cell, the double pulse tests (DPT) with different gate resistance are performed to capture the transient waveforms and to calculate switching loss. The thermal resistance of the designed heat sink on the switching cell is then evaluated based on a standard procedure. Finally, the observed gate

oscillation is analyzed on the proposed equivalent circuit, based on which the effect from the passive components on the oscillation is assessed.

5.1 Proposed design for paralleling two and four GaN HEMTs

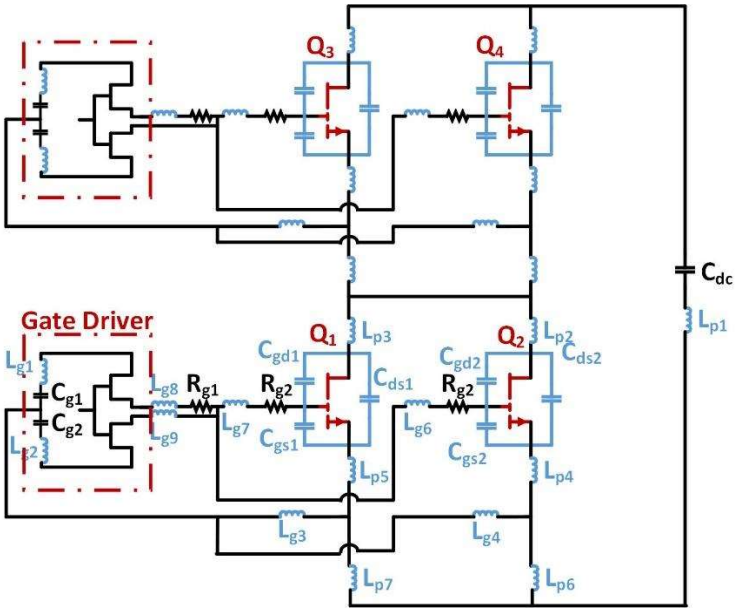


Fig. 5-1 Schematic of the phase leg of two paralleled GaN HEMTs

As the state of the art claimed in Section 1.2.1, the key factor to parallel GaN HEMTs is the symmetry, including the gate loop, power loop and the devices themselves. Fig. 5-1 depicts the all the possible parasitic components in the phase leg with two HEMTs paralleled, namely Q_1 and Q_2. According to [31], the parasitic inductor L_{g3}, L_{g4}, L_{g6}, L_{g7}, L_{p2}~L_{p7}, and the gate resistor R_{g1}, R_{g2} have strong effects on the current sharing between Q_1 and Q_2. R_{g2} is the split gate resistor mentioned above in [24][25] [31]-[33]. Under the configuration, the turn-off resistor R_{off} is R_{g2} while the turn-on resistor R_{on} is the sum of R_{g1} and R_{g2}. To achieve symmetry, it is expected that L_{g6}, L_{g3} equals to L_{g7}, L_{g4} respectively. In the power loop, L_{p2}, L_{p4}, L_{p6} should be identical to L_{p3}, L_{p5}, L_{p7}, respectively. To switch the devices faster, these inductors are expected to be minimized as well.

5.1.1 Power loop design

In the switching cell design with two devices paralleled, all the devices are located on the top layer of PCB, as shown in Fig. 2. The bus decoupling capacitors are put on the bottom layer, yielding enough space on the top layer for the mounted heat sink. With the layout in Fig. 5-2, the mutual magnetic inductance cancellation [24] is obtained and the total power loop inductance is 0.814 nH based on Q3D simulation.

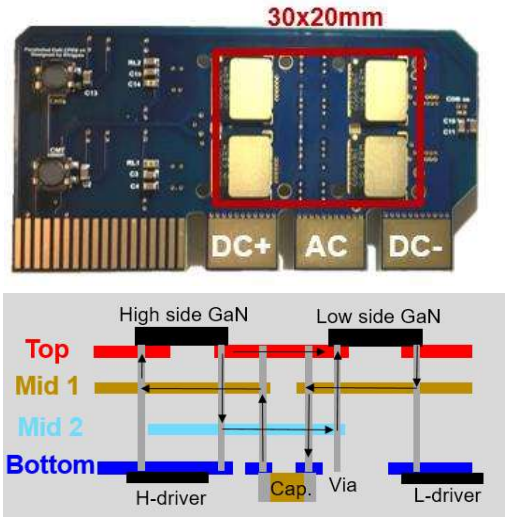


Fig. 5-2 Power loop design of the phase leg with two paralleled GaN HEMTs

In the proposed phase leg design with four devices paralleled, instead of all four devices on the top layer [25][28][29], only two devices Q_1 and Q_2 layout on the top layer and the other two paralleled devices Q_3 and Q_4 are put under the location of Q_1 and Q_2, as evinced in Fig. 5-3. In this way, the four devices only take the footprint of two devices, saving the space by half. From Fig. 5-3, it is observed that the eight HEMTs in the phase leg has the same footprint dimension 30 mm x 20 mm as the two HEMTs paralleled in Fig. 5-2. It should be pointed out that the total size of the proposed phase leg with the double-side heat sink is the same as that of design with all devices on the top layer with single side heat sink. The total power loop

inductance in Fig. 5-3 is only 0.672 nH. One more benefit of this compact design is the potential aid in minimizing the gate loop.

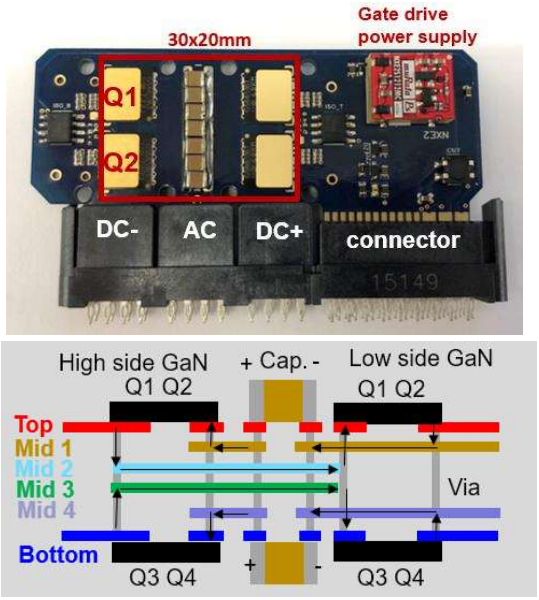


Fig. 5-3 Power loop design of the phase leg with four paralleled GaN HEMTs

5.1.2 Gate loop design

To achieve the symmetry in the gate loop, the split resistor R_{g2}, and the decoupling capacitor C_{g1} and C_{g2} in Fig. 1 should be layout symmetrically first. The alternative way to layout gate loop for two devices paralleled is shown in Fig. 5-4. In this way, the turn-on capacitor C_{g1} is closer to Q_1 and the turn-off capacitor C_{g2} locate closer to Q_2. Under this configuration the turn-on loop for Q_2, highlighted in the green solid line in Fig. 5-4, is longer than that for Q_1 in the red solid line. Similarly, the Q_1 has longer turn-off loop than Q_2. This imbalance leads to the dynamic current mismatch.

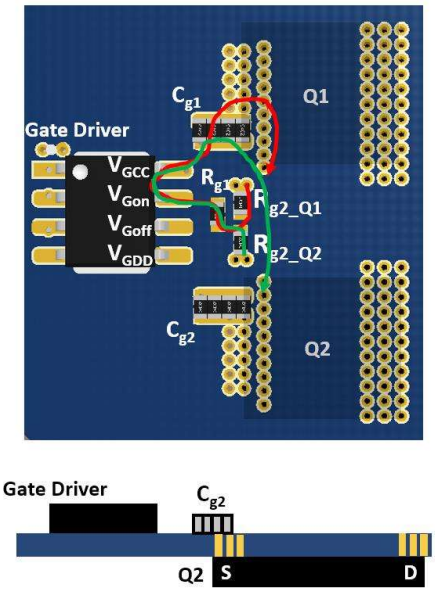


Fig. 5-4 Turn-on gate loop with only one set of decoupling capacitor

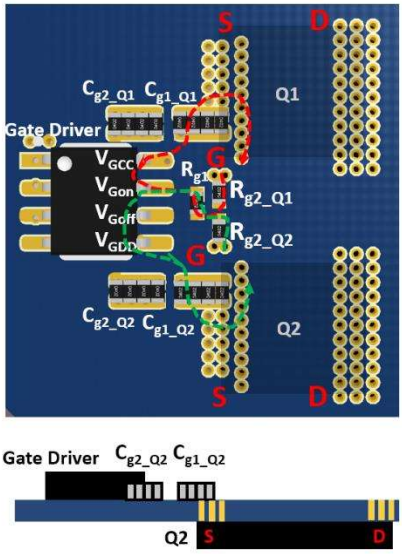
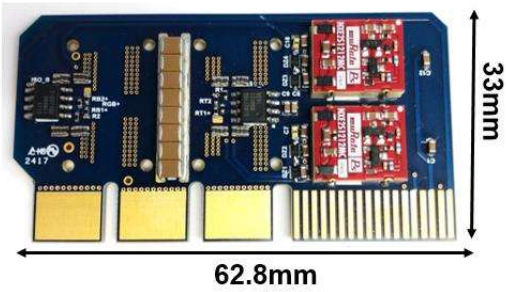


Fig. 5-5 Proposed symmetric gate driver loop with minimized loop inductance

To enhance the symmetry, in the proposed gate loop layout as evinced in Fig. 5-5, each switching device has its own decoupling capacitor C_{g1}, C_{g2} as $C_{g1\text{-}Q1}$, $C_{g1\text{-}Q2}$, $C_{g2\text{-}Q1}$ and $C_{g2\text{-}Q2}$. Fig. 5-5 depicts the turn-on loop for Q_1 and Q_2 in the green and red dash lines respectively. These two lines have almost the same length with the exception of the distance from the gate driver pin V_{GCC} to the decoupling capacitors C_{g1_Q1} and C_{g2_Q2}. The simulated turn-on loop

inductance for Q_1 and Q_2 are 2.4 nH and 2.5 nH. The turn-off loop inductance for Q_1 and Q_2 are simulated as 3.62 nH and 3.6 nH separately. This small difference 0.02 nH in the turn-off loop is contributed by the balanced PCB trace distance from V_{GDD} to C_{g2_Q1} and C_{g2_Q2} in Fig. 5-5.



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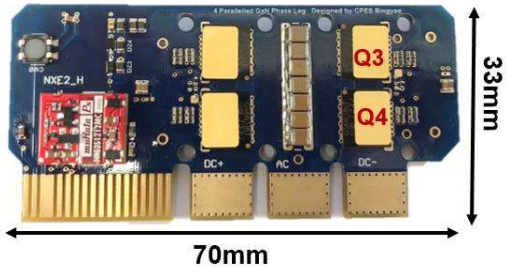


(b)

Fig. 5-6 Back view of the designed switching cell with two (a) and four (b) GaN HEMTs paralleled

To drive four devices, the gate loop layout adopts the design in Fig. 5-5. Based on the power loop design for four paralleled devices in Fig. 5-3, all the four devices $Q_1 - Q_4$ locate within the area of Q_1 and Q_2 in Fig. 5-3. Q_3 is at the backside of Q_1. Hence the split gate resistor for Q_3, R_{g2_Q3} puts at the backside of the Q_1 split gate resistor R_{g2_Q1}. The decoupling capacitor for Q_3, C_{g1_Q3} and C_{g2_Q3} are under the location of C_{g1_Q1} and C_{g2_Q1}. The same configuration is done for Q_4. In this way, the gate loop inductance for four paralleled devices maintain the same value as those for two paralleled devices. Compared with the state of art, where all four HEMTs

spread on the top layer, this approach shrinks the gate loop dimensions significantly. Thanks to this minimized and symmetric gate loop, 0 Ω R_{g1} and 1 Ω R_{g2} are applied.

The backside of the designed switching cell with two and four paralleled GaN devices are exhibited in Fig. 5-6 while the top views are depicted in Fig. 5-2 and Fig. 5-3 separately. In Fig. 5-6, the gate drivers and the gate resistors can be identified. The total footprint size of the switching cell with two devices paralleled is 62.8 mm x 33 mm and 70 mm x 33 mm for four devices paralleled. The later has only 11.5% percent more footprint than the former.

On each phase leg, the isolated gate drive power supplies are implemented for the high and low side devices, shown in Fig. 5-3 and Fig. 5-6. The isolation capacitance for the gate drive power supply should be as small as possible in order to attenuate the common-mode (CM) electromagnetic inference (EMI) noise propagated from the gate drive to the auxiliary power supply [3][9][42]. The isolation capacitance of the selected isolated power supplies in two switching cells is 2.1 pF.

It is worth pointing out that a universal connector is employed for the both switching cells in Fig. 5-6. This connector, as also highlighted in Fig. 5-3, has six power contacts for three power terminations and 24 signal contacts. The model of the connector is selected to fit in the length of the switching cell. The corresponding socket is fixed on the converter board. This configuration allows for the switching cell plugging in and out from the converter board, enabling easy replacement and debugging, which saves cost and debug time if a failure occurs. Furthermore, the connector, which is vertical to the converter mother board, enables a 3D assembly of the converter, fully utilizing the vertical space of the converter, considering the height of the transformer and the film capacitor.

5.1.3 Thermal management

In what follows, the heat sink is designed. Due to the selected connector, the phase leg stands on the converter board. It requires the heat sink to attach to the device tightly, also in favor of the reduction of the contact thermal resistance. The screw, recommended by[16][19], is thus used for connection instead of the double-side thermal tape. To further reduce the contact thermal resistance between the device thermal pad and the heat sink, the insulation interface mentioned above is replaced with the thermal grease. Given the fact that the device thermal pad is electrically connected to the drain terminal, the heat sink is shortcircuit to the drain in consequent. To this end, two separate heat sinks are required for a phase leg.

The designed heat sink is exhibited in Fig. 5-7, where the conventional pin-style heat sink is adopted. The cross-section area of the heat sink is fixed by the given phase leg footprint. The pin height is capable to control the heat sink thermal resistance with a given air speed. From the heat sink datasheet [116], the relation between the thermal resistance R_{th} (˚C/W) and the pin height H_{th} (mm) is plotted in Fig. 8 and formulated in (5.1) under 600 linear foot per meter (LFM). The heat sink thermal resistance R_{th} required with the device loss P, the room temperature T_0 and the device operating temperature T is calculated in (5.2) considering the thermal resistance from the junction to the thermal pad is 0.3 ˚C/W.

$$R_{th} = 58.394 H_{th}^{-1.113} \tag{5.1}$$

$$R_{th} = (T - T_0)/P - 0.3 \tag{5.2}$$

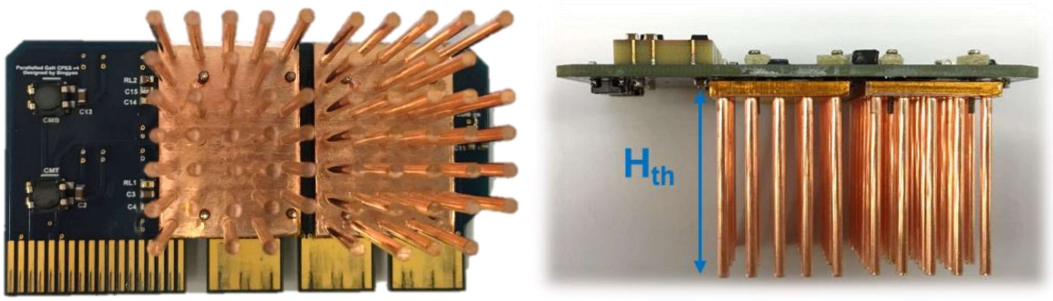


Fig. 5-7 Heat sink mounted on the switching cells

For example, the maximum loss *P* on one pair of the GaN HEMTs is 24.9 W in the worst case. To maintain the device working temperature within 80℃ under 25℃ room temperature. The required thermal resistance is calculated using (5.2) as 1.71 ˚C/W and the corresponding heat sink pin height is 25 mm according to (5.1).

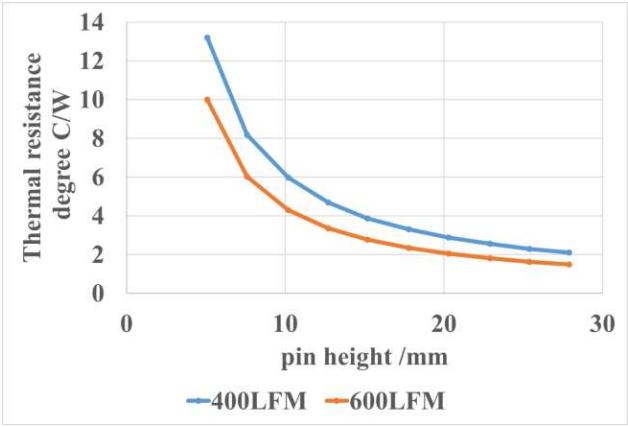


Fig. 5-8 The heat sink thermal resistance is dependent on the pin height.

The heat sink design for the switching cell using four paralleled GaN HEMTs is illustrated in Fig. 5-9 and Fig. 5-10. Two standard copper heat sinks are employed for the paralleled four HEMTs in one position, which are forced to attach on the device thermal pads by screws. The insulated thermal tape is added between the heat sink and the thermal pad in this design to demonstrate an insulated thermal solution, which is safer compared with the design in Fig. 5-7. As a penalty, the contact thermal resistance between the device to the heat sink is larger. With the four paralleled GaN HEMTs, the on-resistance of the switching cell is as small as 6.25 mΩ

at 25℃, leading to 50% reduction of the conduction loss compared with the switching cell using two paralleled HEMTs. To this end, the total heat sink volume needed to control the junction temperature in Fig. 5-9 is smaller compared with that in Fig. 5-7.

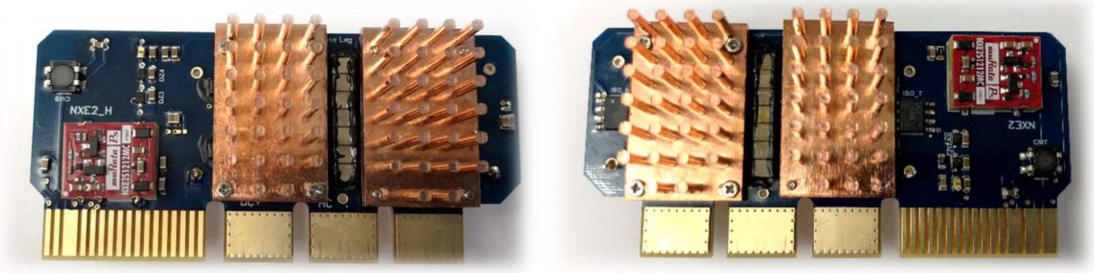


Fig. 5-9 Front and back view of the heat sink design for the switching cell using four paralleled GaN HEMTs

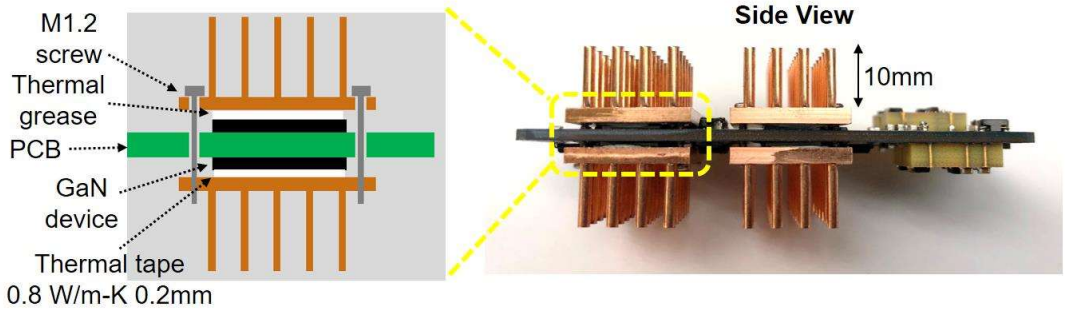
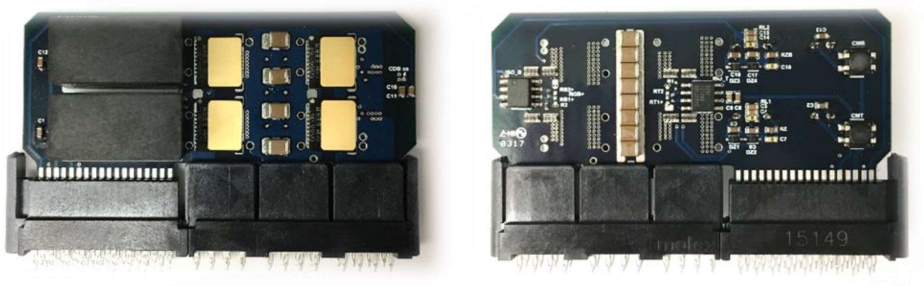


Fig. 5-10 Side view of the heat sink design for the switching cell using four paralleled GaN HEMTs

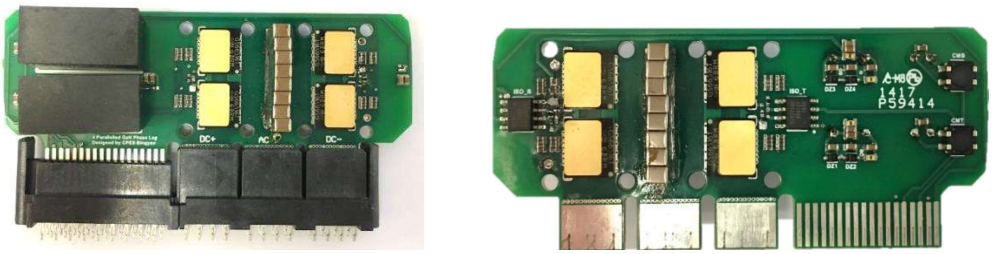
Besides the standard heat sink design, it deserves to show the first generation of the heat sink design for the first version switching cell design using two and four paralleled HEMTs. The first version switching cell for 100 A and 200 A are shown in Fig. 5-11 and Fig. 5-12 respectively. The main improvement from the first version to the version shown above in Fig. 5-2 and Fig. 5-3 is the gate driver power supply from MEJ2S0509SC [36] to NXE2S1212MC [117], whose isolation capacitance is only 2.1 pF, one time smaller than that of the former. Furthermore, the height of the MEJ2S0509SC is 9 mm, which blocks the air flow from the left

edge to the right edge on the power supply. To tackle the problem, the heat sink with curved-fin was designed, shown in Fig. 5-13. With the heat sink, the air flows from the top edge of the switching cell to the right edge, relieving the thermal stress on the design in the left corner. Accordingly, the fan for this heat sink would locate on the top of the switching cell to push the cool air into the heat sink. Though the solution worked with the converter test, the thermal resistance is large due to the limited exposed surface to the air.



(a) Front view (b) Back view

Fig. 5-11 First version of the switching cell with two paralleled GaN HEMTs



(a) Front view (b) Back view

Fig. 5-12 First version of the switching cell with four paralleled GaN HEMTs

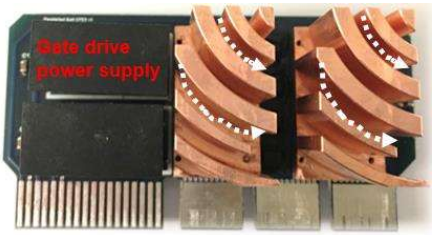


Fig. 5-13 Curved-fin heat sink design for the first-version switching cell

5.2 Evaluation of the designed switching cells

5.2.1 Dynamic characteristics

With the designed switching cell, the DPT with different gate resistor R_{g1} and R_{g2} are performed to obtain the dynamic characteristics of the paralleled devices. To capture the drain current I_{ds}, the PCB with a current shunt inserted is fabricated based on the design above. The current shunt is only capable to measure the total I_{ds} of the paralleled devices. This avoids the large oscillation introduced by using one current shunt to measure one device I_{ds} [31][32]. The test setup of the phase leg with two paralleled GaN HEMTs is exhibited in Fig. 5-14. The transient waveforms with 400 Vdc, 100A load current, 1 Ω R_{on}, 1 Ω R_{off} with two devices paralleled are depicted in Fig. 5-15, where the turn-on dv/dt is 43.24 V/ns and the turn-off dv/dt reaches 80.22 V/ns. The transient gate voltage V_{gs}, whose maximum magnitude is under 6.6 V, contains some small oscillation. The clean I_{ds}, the drain-source voltage V_{ds} waveforms and the fast dv/dt verify the feasibility of driving the paralleled HEMTs with 1 Ω gate resistance, thanks to the careful design consideration explained in the section above. Furthermore, the total switching losses of two paralleled devices under different I_{ds} are calculated and shown in Fig. 5-16. In Fig. 5-16, it is observed that the turn-on loss at 100 A I_{ds} with 1 Ω R_{on} is 390 μJ, saving 30% loss by driving with 3 Ω R_{on} and 50% loss by driving with 5.7 Ω R_{on}.

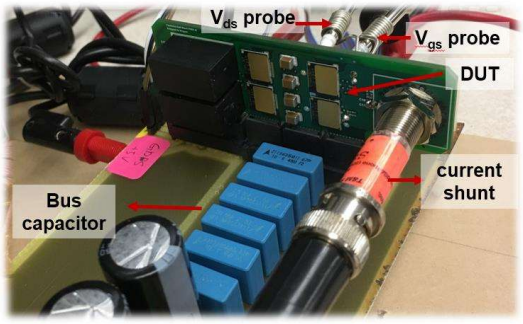
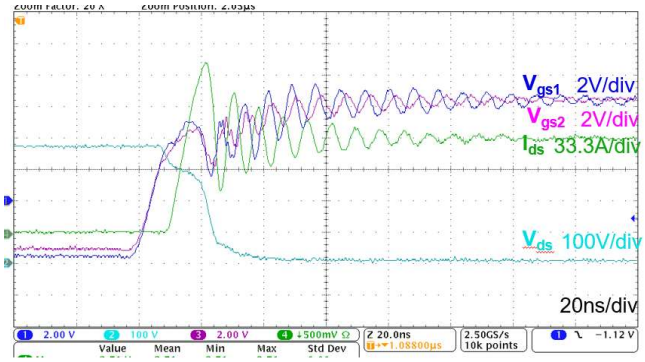
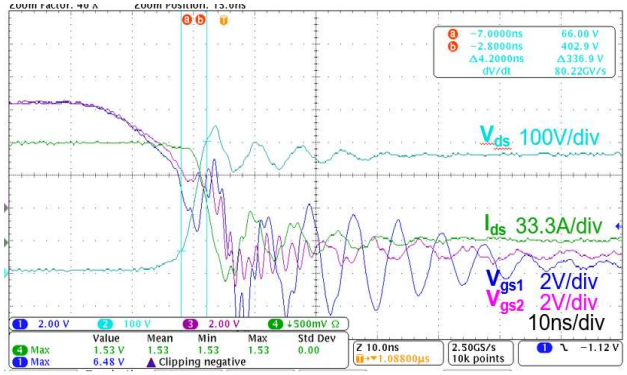


Fig. 5-14 Double pulse test setup of two GaN paralleled with the current shunt



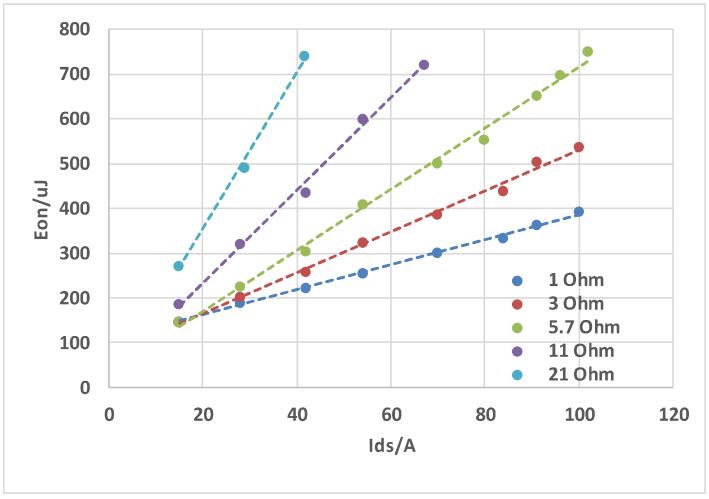
(a)



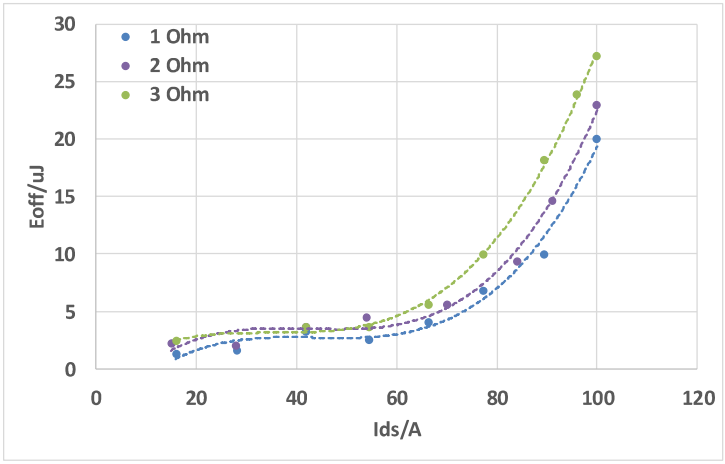
(b)

Fig. 5-15 DPT waveforms with two devices paralleled V_{dc}= 400V, I_{ds}=100A, R_{g2}=1Ω, R_{g1}=0:

(a): turn-on, (b): turn-off



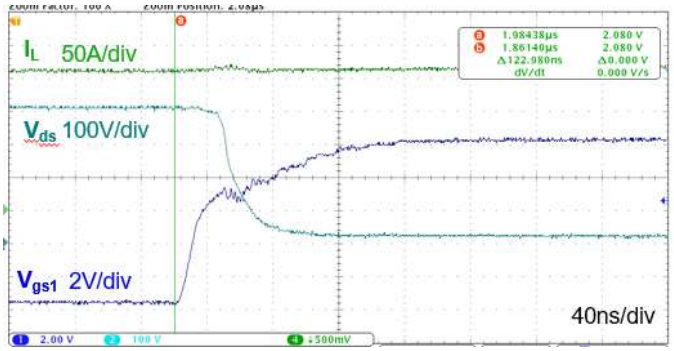
(a)



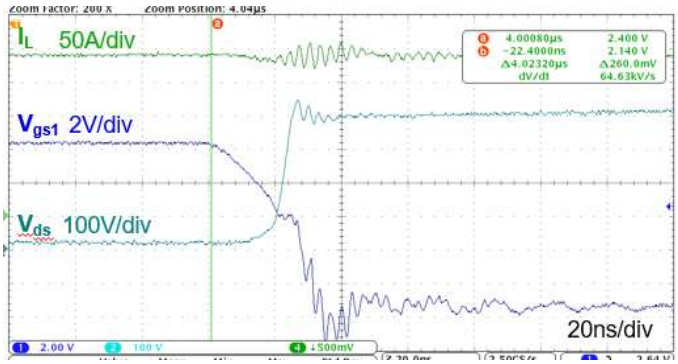
(b)

Fig. 5-16 (a): Turn-on and (b) turn-off loss estimation with different R_{on} and R_{off}

The DPT is also performed for the four GaN HEMTs paralleled without the current shunt inserted using the switching cell in Fig. 5-3. Fig. 5-17 exhibits the transient waveforms under 400 Vdc, 200 A load current, 1 Ω R_{on}, 1 Ω R_{off} where turn-on and turn-off dv/dt are 11.9 V/ns and 77.42 V/ns respectively. In comparison with the two devices paralleled, the turn-on dv/dt slow down, due to the limited driving turn-on capability of the gate driver. The gate driver turn-on channel suffers from the saturation and limits the driving current to 1 A. To reduce the turn-on loss for the four GaN HEMTs paralleled for hard turn-on operation, a gate driver with larger saturated current is recommended.



(a)



(b)

Fig. 5-17 DPT waveforms with four devices paralleled V_{dc}= 400V, I_{ds}=200A, R_{g2}=1Ω, R_{g1}=0.5: (a): turn-on, (b): turn-off

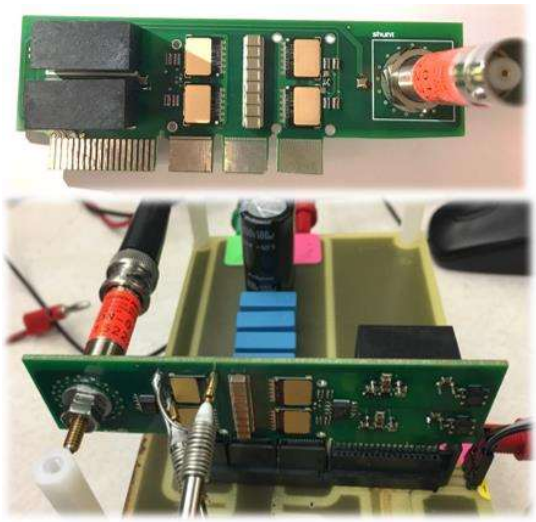


Fig. 5-18 Double pulse test setup of four GaN paralleled with the current shunt

In order to estimate the switching loss of the switching cell with four paralleled GaN HEMTs, the switching cell with the current shunt was fabricated, shown in Fig. 5-18. The

current shunt can only measure the total current of the four paralleled devices. Under 400 Vds 60 A total load current with 1.5 Ω turn-on resistor, there observed a large I_{ds} oscillation, whose transient peak value reaches 1000 A in Fig. 5-19. The gate is also oscillated with the I_{ds}, due to the effect on the parasitic common source inductance with the device package. The large I_{ds} oscillation is introduced by the large power loop inductance, which is dominated by the current shunt inductance (around 2 nH). With the shunt short-circuit, under the same test condition, there is no oscillation observed in Fig. 5-20 as expected. To perform the DPT with the current shunt, the turn-on gate resistance has to increase to slow the turn-on di/dt, so that the I_{ds} oscillation can be smaller.

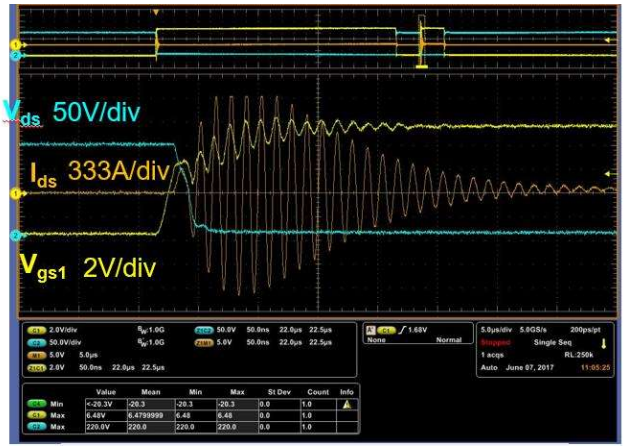


Fig. 5-19 DPT waveforms with four devices paralleled with current shunt V_{dc}= 200V, I_{ds}=60A, R_{g2}=1Ω, R_{g1}=0.5

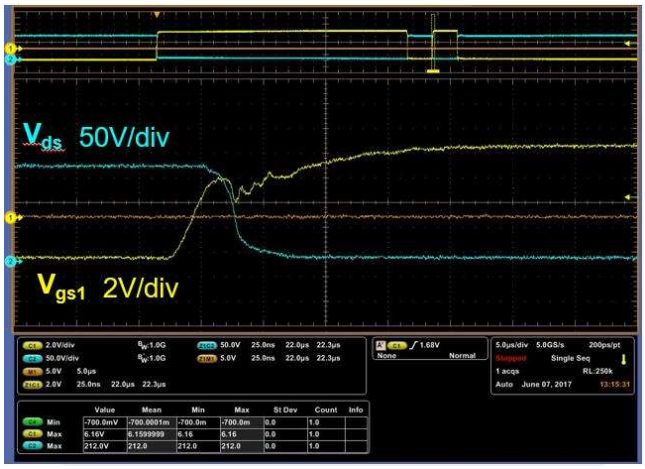
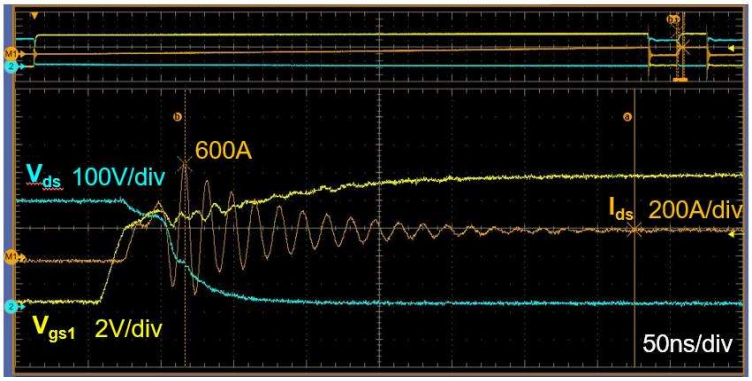
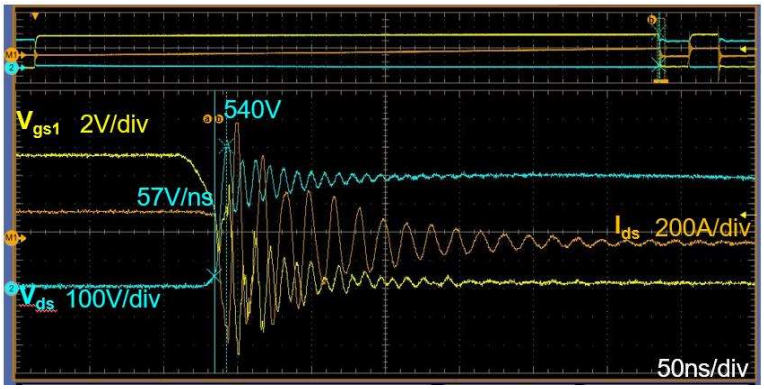


Fig. 5-20 DPT waveforms with four devices paralleled with current shunt removed, V_{dc}= 200V, I_{ds}=60A, R_{g2}=1Ω, R_{g1}=0.5

The DPT with current shunt for the switching cell of four devices paralleled was performed under 400 Vdc, 200 A load current, 5 Ω R_{on}, 1 Ω R_{off}, whose transient waveforms are illustrated in Fig. 5-21. During turn-on, the maximum overshoot is 600 A and the dv/dt slows down to 6 V/ns. As a result, the turn-on loss in this case is large, which is 2620.84 μJ. Compared with 751.33 μJ turn-on loss of the switching cell under 400 Vdc 100 A I_{ds}, 5.7 Ω R_{on}, the former value is more than two times larger. It means under the same load current and turn-on resistor, the turn-on loss of one switching cell with four paralleled GaN is larger than that of the switching cell with two GaN paralleled, depicted in Fig. 5-22. This is caused by the limited driving capability of the gate driver. To this end, it can be concluded that in the hard-switching topologies it is better to parallel two switching cells of two paralleled GaN HEMTs, rather than using one switching cell of four paralleled GaN HEMTs.



(a)



(b)

Fig. 5-21 DPT waveforms with four devices paralleled with current shunt V_{dc}= 400V, I_{ds}=200A, R_{g2}=1Ω, R_{g1}=3.9: (a): turn-on, (b): turn-off

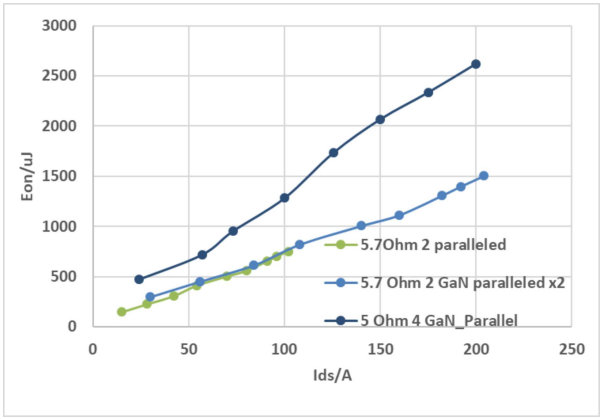


Fig. 5-22 Turn-on loss estimation with four paralleled GaN, compared with one and two switching cells two paralleled GaN

5.2.2 Thermal resistance evaluation

The thermal resistance of the heat sink on the two paralleled HEMTs is evaluated to verify the target value. To this end, a complete procedure is developed. First the paralleled devices Q_1 and Q_2 continuously generate a DC constant loss by conducting a DC current. If the current is injected in the forward direction while the devices are on, a large current source is needed for a large-loss case, for example, 41 A DC current for 21.4 W loss. Furthermore, the slight change on V_{ds}, caused by the increased device on-resistance due to the increased die temperature, requires a high-precision voltage probe and oscilloscope. Instead of injecting current in the forward direction, the DC current can be conducted in the reverse direction from the source terminal to the drain while the devices are off, depicted in Fig. 5-23. For example, a constant 21.4 W is generated when the device V_{ds} is around -5.35 V under -4 A I_{dc} excitation. In the second step, the heat sink temperature is measured by the thermocouple attached on the end of the heat sink pin until Q_1 and Q_2 reach thermal stability.

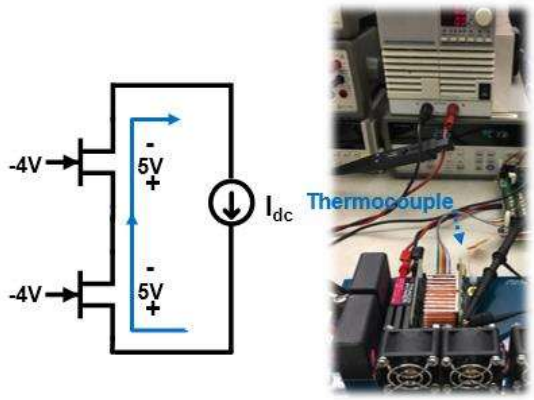


Fig. 5-23 Setup to measure the heat sink thermal resistance

Following the evaluation process, the device loss and the heat sink temperature are measured and plotted in Fig. 5-24. The trend line is extracted then. The thermal resistance of the heat sink is the slope of the trend line, which is 1.7516℃/W. This value matches the

previous target value. With (5.1), the heat sink pin height can be approximately estimated, saving the converter size and protecting the device from over temperature. Based on (5.2), with this heat sink design, the maximum allowed loss with 80℃ junction temperature under 25℃ room temperature of the one position is 24.9 W. If all of the loss comes from the conduction loss, the maximum allowed rms current is 36.4 A.

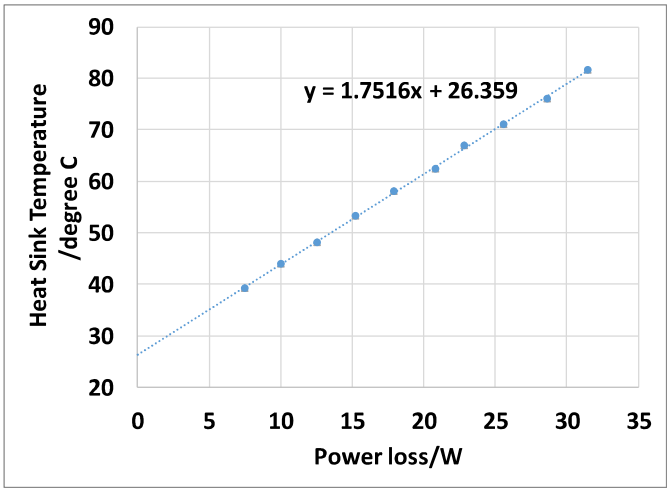


Fig. 5-24 Heat sink temperature vs device loss for the switching cell using two paralleled GaN HEMTs

As for the switching cell using four paralleled GaN HEMTs, the thermal resistance of the heat sink in Fig. 5-9 is also evaluated based on the approach explained above, whose value is 1.08℃/W based on the measurements shown in Fig. 5-25. Based on (5.2), with this heat sink, the maximum allowed loss with 80℃ junction temperature under 25℃ room temperature of the one position is 40 W. If all of the loss comes from the conduction loss, the maximum allowed rms current is 65 A.

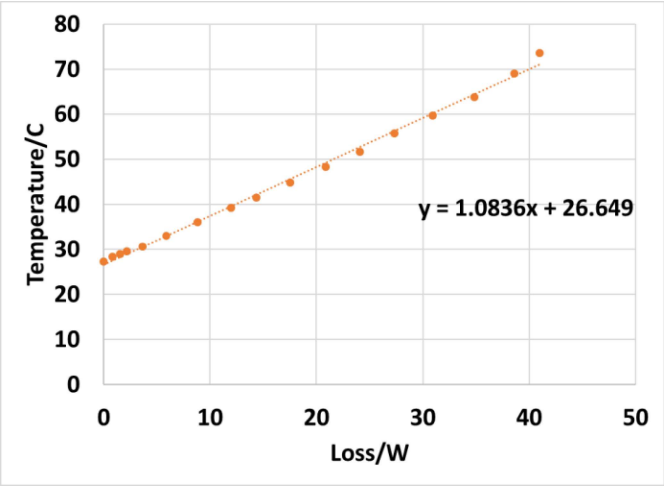


Fig. 5-25 Heat sink temperature vs device loss for the switching cell using four paralleled GaN HEMTs

The approach above to evaluate heat sink resistance can also be generalized to other converter thermal management. With the evaluated heat sink thermal resistance and the measured heat sink temperature during the converter operation, the loss on the devices can be estimated accurately then using (5.2). This helps to verify the loss estimation performed in the initial design stage.

5.3 Analysis on the commutation during turn-on transient with paralleled GaN HEMTs

In what follows, the gate oscillation due to the commutation between the two paralleled devices is assessed in this section. Though the asymmetry between the two paralleled GaN HEMTs is almost eliminated in the proposed design, a large gate oscillation is still observed with a large R_{g1} during DPT. Fig. 5-26 shows the turn-on transient with two GaN paralleled under 400 Vdc, 42 A, 20 Ω R_{g1} and 1 Ω R_{g2}. The maximum gate oscillation magnitude can be 10.9 V, higher than the claimed maximum gate voltage in the datasheet. Compared with the

waveforms in Fig. 5-15, it is deemed that a larger gate resistor R_{g1} does not help to attenuate the gate oscillation, but worsen the problem.

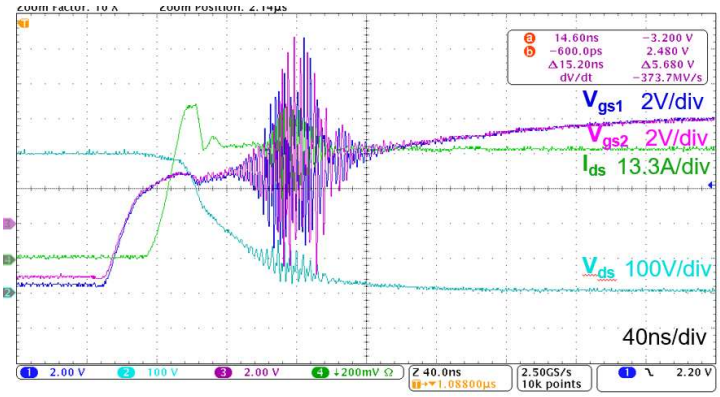


Fig. 5-26 Double pulse test waveforms with Vdc= 400V, I_{ds} = 42A, R_{g2}=1Ω, R_{g1} = 20Ω

5.3.1 Proposed simplified equivalent circuit

To address the phenomena above, the device spice model was first used. However, it could not emulate the device behavior shown in Fig. 5-26. Therefore, a simplified equivalent circuit is derived to analyze V_{ds} and V_{gs} within the miller plateau duration. It is worth to point out that the target of the circuit is to assess the passive component effect on the gate oscillation, not to characterize the switching loss or the complete switching behavior.

The proposed circuit is illustrated in Fig. 5-27, where two paralleled GaN HEMTs Q_1, Q_2, the gate driver, the gate resistors and the parasitic inductance within the gate loop are included. Within the device model, the junction capacitors C_{DG}, C_{DS}, C_{GS} and the package inductors L_S, L_D, L_G are considered. Among them, C_{DG} and C_{DS} are non-linear capacitors, referring to the datasheet [3]. The initial voltage of C_{GS} is set to 3 V, the claimed miller plateau voltage [3]. The channel is simplified into a voltage-controlled current source I_{cha}. I_{cha} is controlled by both V_{ds} and V_{gs} as (5.3) formulates, where V_{th} is the threshold voltage. The constant g_{m1} and g_{m2} in (5.3) are determined by a given DPT dv/dt. To focus on V_{gs} and exclude the effect from the

load current, the channel here only conducts the capacitor-discharging current. The gate driver with the turn-on decoupling capacitor is simplified into a voltage source V_{PS} (6.5V) with a parasitic inductor L_{GD4}, assuming the driver is not saturated. L_{GD4} can be deemed as the decoupling capacitor equivalent inductance (ESL). L_{GD1}, L_{GD2}, L_{GD3} represent the parasitic inductor from the PCB traces. Among them, L_{GD3} is taken as the shared traces in the gate loops of Q_1 and Q_2, highlighted in Fig. 5-5. L_{GD1} and L_{GD2} represent the difference in the gate loops between Q_1 and Q_2.

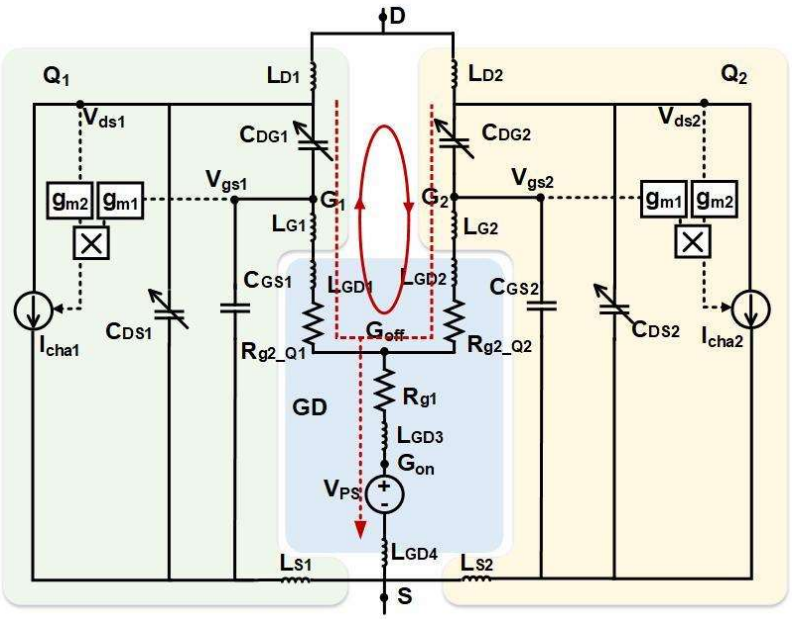


Fig. 5-27 Proposed circuit to explain the commutation between two paralleled GaN HEMTs

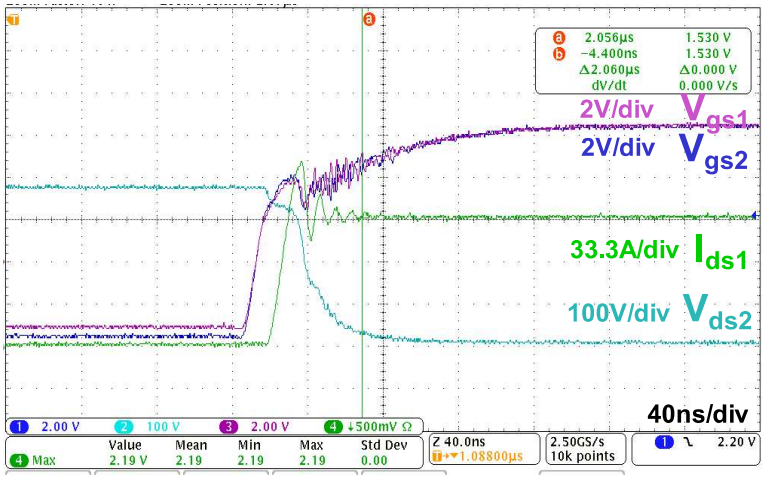
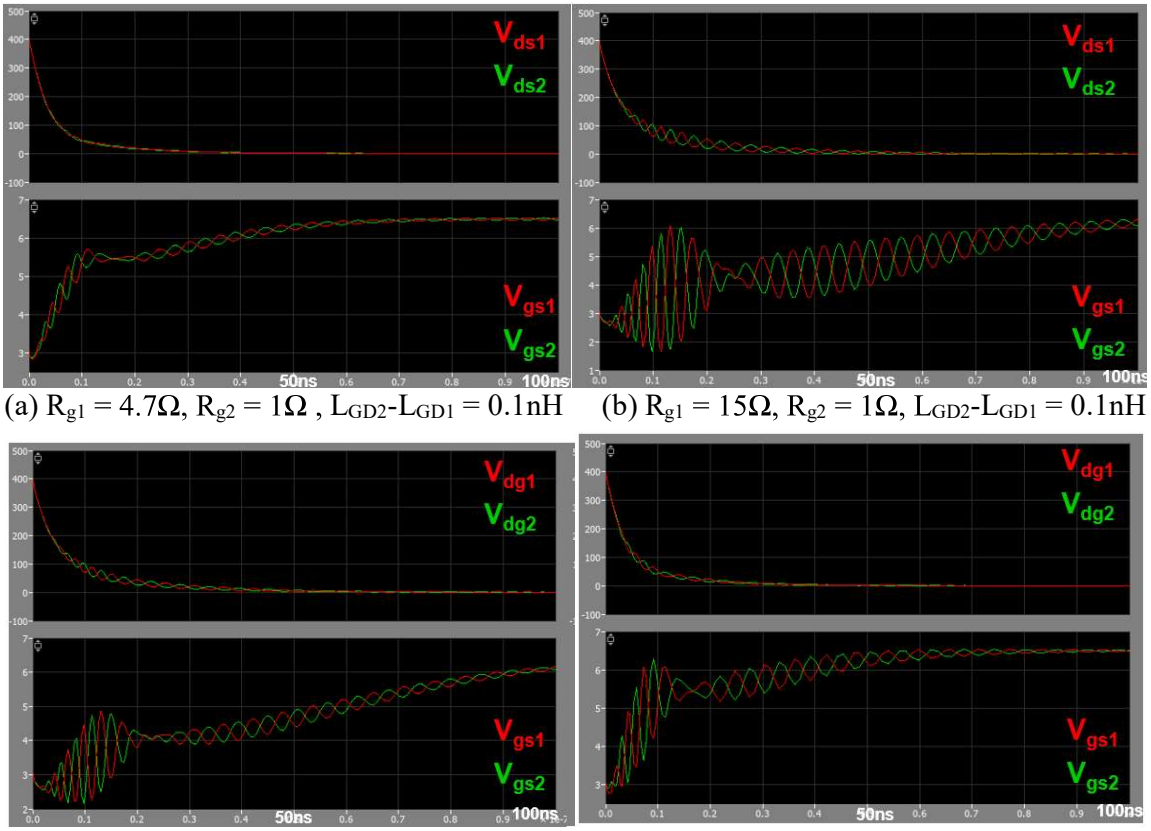


Fig. 5-28 Double pulse test waveforms with Vdc= 400V, I_{ds} = 100A, R_{g2}=1Ω, R_{g1} = 4.7Ω.

$$I_{cha} = g_{m1}(V_{gs} - V_{th}) \cdot g_{m2} V_{ds} \tag{5.3}$$



(a) R_{g1} = 4.7Ω, R_{g2} = 1Ω , L_{GD2}-L_{GD1} = 0.1nH (b) R_{g1} = 15Ω, R_{g2} = 1Ω, L_{GD2}-L_{GD1} = 0.1nH

(c) R_{g1} = 15Ω, R_{g2} = 5Ω, L_{GD2}-L_{GD1} = 0.1nH (d) R_{g1} = 4.7Ω, R_{g2} = 1Ω , L_{GD2}-L_{GD1} = 0.6nH

Fig. 5-29 Simulated V_{ds} and V_{gs} in miller plateau duration with different passive component values

The circuit is implemented in the simulation software PLECS. To match experimental dv/dt under 400 V, 100 A, 4.7 Ω R_{g1}, 1 Ω R_{g2} in Fig. 5-28, g_{m1} and g_{m2} are estimated first. The simulated transient waveforms V_{ds} and V_{gs} in this case are plotted in Fig. 5-29(a), in comparison with Fig. 5-28. It is observed in both Fig. 5-28and Fig. 5-29 (a) that the gate oscillation starts when V_{ds} drops to around 150 V. This relates to the non-linearity of the miller capacitor C_{DG}, whose capacitance is around 4 pF at 400 V V_{ds}, and starts to increase to tens of picofarads around 150 V V_{ds}. Additionally, in both the simulation and experiment, the oscillation duration

holds until V_{gs} reaches around 6 V and the resonant frequency is close to 500 MHz. Fig. 5-28and Fig. 5-29 (a) also have V_{ds} dv/dt slope in common. When R_{g1} increases to 15 Ω, the significant oscillation on V_{gs} is predicted by the simulation, as indicated in Fig. 5-29 (b), matching the condition observed in Fig. 5-28. While the proposed circuit can predict the gate oscillation, more analysis is performed below.

5.3.2 Assessment of the effects from the passive components on the gate oscillation

A. Effect from the gate resistor

From the experimental waveforms in Fig. 5-15, Fig. 5-26and Fig. 5-28, it is evident that the gate oscillation is larger with a larger R_{g1}, also verified by the simulation in Fig. 5-29 (a) (b). To turn on the device, C_{DG} is discharging through R_{g2}, R_{g1}, the gate driver and to the decoupling capacitors, along the dashed line in Fig. 5-27. Once R_{g1} is large enough, it blocks the discharging current from Terminal G_{off} to Terminal S in Fig. 5-27. The oscillation due to the imbalance between C_{DG1} and C_{DG2}, or between L_{GD1} and L_{GD2} would circulate within the solid loop highlighted in Fig. 5-27. A smaller R_{g1} creates a path to bypass the circulated energy and hence attenuate the gate oscillation. Furthermore, a larger R_{g2} aids in the oscillation reduction. As evinced in Fig. 5-29 (c), the oscillation magnitude is smaller with 5 Ω R_{g2} compared with the waveforms in Fig. 5-29 (b) using 1 Ω R_{g2}.

To assess the effect, the predicted gate oscillation magnitude by the proposed circuit is recorded with different gate resistors. In Fig. 5-30, the gate oscillation increases with the increased R_{g1}. When R_{g1} is quite large, a large R_{g2} helps to attenuate the oscillation. Conversely when R_{g1} is small, the oscillation is bypassed and thus there is no need of a large R_{g2}.

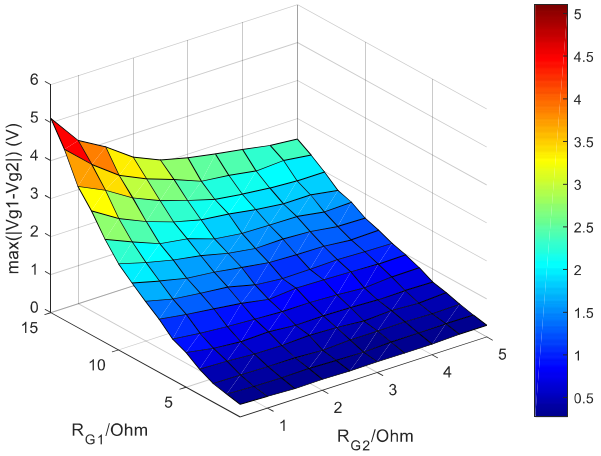
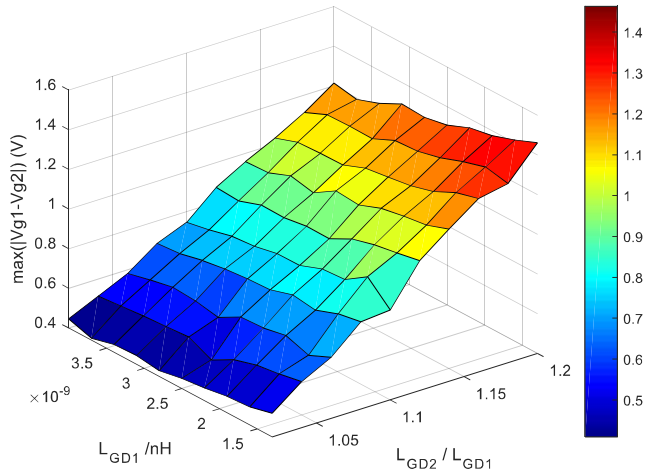


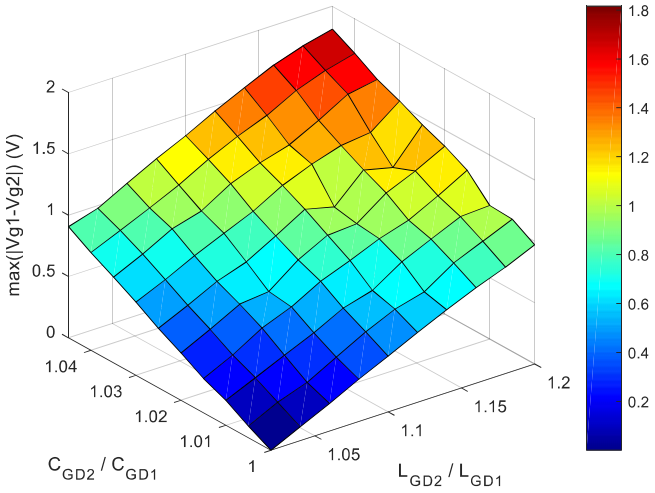
Fig. 5-30 Predicted gate oscillation with different gate resistors (C_{DG2} = 1.02C_{DG1}, L_{GD1} = 1.4nH, L_{GD2}-L_{GD1} = 0.1nH, varying R_{g1} R_{g2}

B. Effect from the gate loop inductance and C_{DG} tolerance

R_{g1} and R_{g2} discussed above affect the gate oscillation magnitude only. The origin of the oscillation is the imbalanced inductor or capacitor along the solid circle in Fig. 5-27. Ideally, if all the parasitics of the two devices are symmetric, there would not be any difference between the two V_{gs}. Fig. 5-31 (a) assesses the effect on the gate oscillation from the difference between L_{GD1} and L_{GD2}. Compared with the inductance absolute value, the difference of the inductances has a more significant effect on the gate oscillation. When the difference between L_{GD1} and L_{GD2} increases from 5% to 20%, the oscillation is three times larger. When the gate loop inductance of Q_1 and Q_2 reduce simultaneously, the oscillation frequency tends to increase and the Q factor in the solid circle in Fig. 5-27 increases, leading to a larger oscillation magnitude. Besides, the device parasitic capacitance tolerance plays a significant role as well. In Fig. 5-31 (b), only 5% of C_{DG} difference has the same effect on the gate oscillation as 20% difference between L_{GD1} and L_{GD2}. The C_{DG} tolerance can be controlled by the device manufacture process.



(a) $C_{DG2} = 1.02C_{DG1}$, varying L_{GD1} and L_{GD2}/L_{GD1}



(b) $L_{GD1} = 1.4$nH, varying L_{GD2}/L_{DG1}, C_{DG2}/C_{DG1}

Fig. 5-31 Predicted gate oscillation with different gate resistors and gate loop inductances

($R_{g1} = 4.7\Omega$, $R_{g2} = 1\Omega$,)

Based on the observation and the analysis above, to parallel the GaN HEMTs in question, the gate oscillation during turn-on transient is sensitive to the gate resistor combinations, the gate loop inductors and the device parasitic capacitors. When the gate loop inductances of the two devices are closely identical and minimized, for example, less than 4 nH, small R_{g1} and R_{g2} can be applied. In this case, R_{g1} can be 0 Ω and R_{g2} is recommended to 1 Ω considering the

oscillation due to the C_{DG} tolerance. When the gate oscillation needs attenuation, it is recommended to increase R_{g2} first.

5.4 Summary and conclusion

This chapter has presented a complete design consideration and analysis for paralleling two and four 650 V 60 A e-mode GaN HEMTs, including power loop and gate loop design, thermal management, dynamic characterization, high power converter application and analysis on observed gate oscillation. For the layout of paralleling GaN HEMTs, the key is to achieve symmetry in the gate loop. This paper came up with an integrated power loop with symmetric and minimized gate loop, as well as two adaptive thermal solutions. Thanks to the careful arrangement at layout, the paralleled GaN HEMTs can be driven with 1 Ω turn-on resistance, verified by the double pulse test. The heat sink volume was pre-calculated based on the required thermal resistance, which was also later characterized experimentally. This helps to control device temperature and increase converter power density.

Furthermore, the reason of the gate oscillation observed in DPT was explained based on a proposed simplified circuit. Based on the circuit, the effect from the passive components in the gate loop was assessed. In experiment, it was found that GaN HEMT gate was very sensitive and the oscillation between the parasitic capacitors and the gate loop inductance could break the gate, which could be more severe under paralleling operation. A 10% difference in the gate loop between the paralleled GaN can introduce observable oscillation at the gates. Furthermore, a proper gate resistor should be chosen. The combination with a large common on-resistor R_{g1} and a small split resistor R_{g2} leads to large oscillation in the gate voltage.

Chapter 6. 10 kW DC-DC Converter Using Paralleled GaN

With the 650V 100 A/ 200 A switching cell with paralleled GaN HEMTs designed in Chapter 5, a 10 kW LLC resonant converter is built in this chapter for on-board charger application. The input voltage is 400 V and the output voltage ranges from 150 V to 500 V with 35 A maximum output current. As mentioned in Section 1.2.5, the challenge tackled in this chapter is the high frequency litz-wire transformer design to achieve high efficiency and high power density for the LLC resonant converter, whose schematic is depicted in Fig. 6-1.

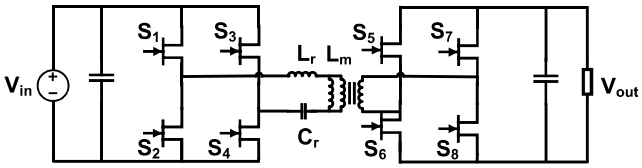


Fig. 6-1 Schematic of the LLC resonant converter

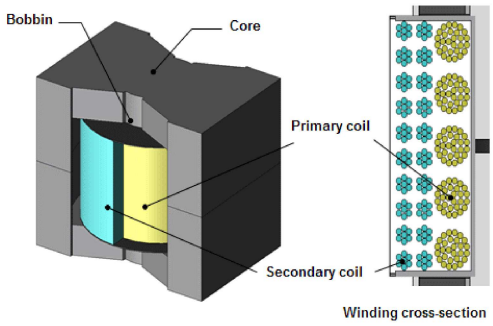


Fig. 6-2 Common litz-wire transformer structure based on EQ or ER core

To integrate the magnetic components, the leakage inductor L_k of the transformer usually works the resonant inductor L_r. The resonant capacitor is then adjusted to meet the desired resonant frequency. In the conventional litz-wire transformer design, the primary and secondary winding twist on the center leg of the core, illustrated in Fig. 6-2. The leakage inductance L_k in this structure takes only 1%-5% of the magnetizing inductance L_m thanks to the strong coupling between the primary and the secondary windings. To achieve the regulation

of the desired output voltage from 150 V to 500 V, equivalent to the gain M ranging from 1 to 3.3, the switching frequency needs to decrease. The range of the switching frequency variation is determined by the ratio between the magnetizing inductance L_m and the resonant inductance L_r. Based on the specifications of the converter, the gain of the converter M is simulated with different ratio L_m/L_r, whose results are shown in Fig. 6-3. It is observed in Fig. 6-3 that L_m/L_r needs to be larger than 2 so that the gain can be pushed to 3.3. However as a tradeoff of the larger gain thanks to the larger L_m/L_r, the switching frequency to meet 'M=3.3' decreases, rendering an increase of the secondary peak current. To limit the secondary current peak under 100 A, the switching frequency in the design is simulated to be smaller than 7. To this end, L_m/L_r in this design is limited from 2 to 7, which is impossible to achieve with the conventional transformer design, where L_k is used as L_r.

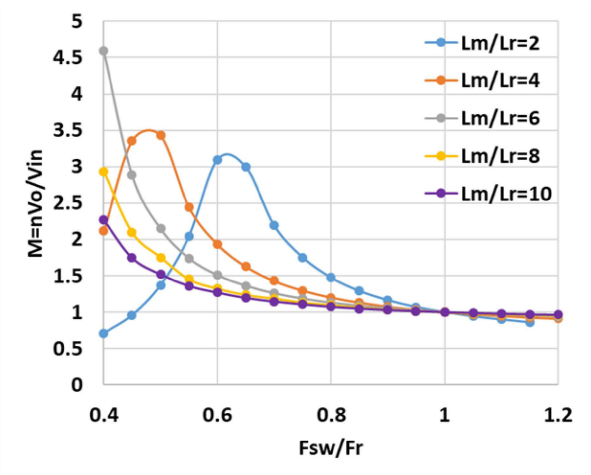


Fig. 6-3 L_m/L_r effect on the converter gain and the switching frequency range

In this chapter, an integrated litz-wire transformer is designed with a desired leakage inductance based on the 'E' 'I' core. A detailed modeling for the inductance, core loss and winding loss for the transformer and a transformer optimization process are illustrated. Experimental results with the converter are provided to validate the transformer loss estimation.

6.1 Transformer design

The proposed transformer with litz-wire windings are illustrated in Fig. 6-4, where the primary and secondary windings are twisting on the two side legs of the 'E' core. With this configuration, the magnetizing flux circulate within the two side legs while the center leg generates the leakage flux. The equivalent magnetic circuit of the transfomer is illustrated in the Fig. 6-5, where Φ_1 Φ_3 represent the magnetizing flux and Φ_2 is the leakage flux. With the defined core dimensions in Fig. 2, the flux above can be calculated in (6.1)-(6.3), where l_g, l_{g_r}, w, c are, respectively, the air gap of the side leg and the center leg, width of legs, and depth of the core. Based on (6.3), the leakage flux Φ_2 is not only determined by the reluctance of the core but also by the winding distribution of the primary and secondary windings. N_{1P}, N_{2P}, N_{1S}, N_{2S} are respectively the number of the turns of the primary winding on the left leg and right leg, the number of the turns of the secondary winding on the two side legs. A larger leakage flux can be generated with a larger difference between N_{1P} and N_{2P}, N_{1S} and N_{2S}.

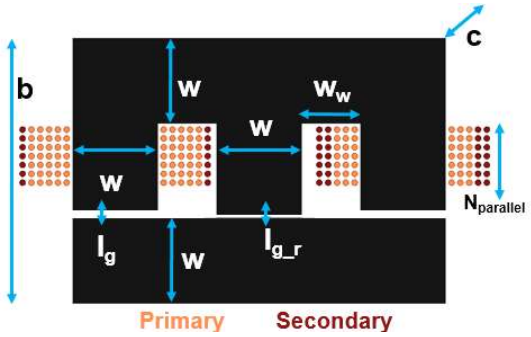


Fig. 6-4 Core with controlled center leg gap and the horizontal winding arrangement (turns ratio 8:3)

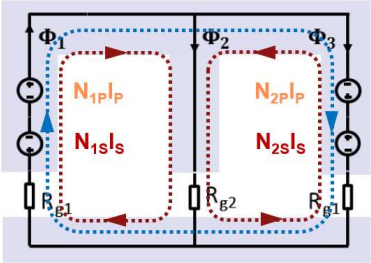


Fig. 6-5 Magnetic circuit of the transformer in Fig. 6-4

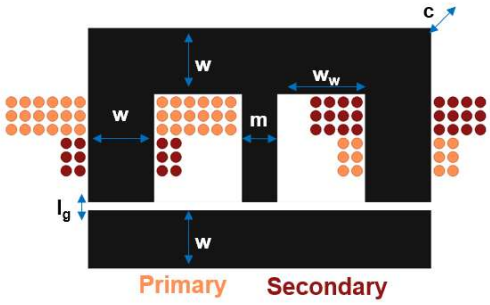


Fig. 6-6 Core with controlled center leg width and the vertical winding arrangement (turns ratio 8:3)

$$R_{g1} = \frac{l_g}{\mu_0 wcp_{fringing}}, R_{g2} = \frac{l_{g\_r}}{\mu_0 wcp_{fringing}} \tag{6.1}$$

$$R_a = R_{g1} + \frac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}, R_b = R_a \frac{R_{g1}+R_{g2}}{R_{g2}} \tag{6.2}$$

$$\begin{aligned} \Phi_1 &= \frac{N_{1P}I_P - N_{1S}I_s}{R_a} + \frac{N_{2P}I_P - N_{2S}I_s}{R_b} \\ \Phi_3 &= \frac{N_{2P}I_P - N_{2S}I_s}{R_a} + \frac{N_{1P}I_P - N_{1S}I_s}{R_b} \\ \Phi_2 &= \Phi_1 - \Phi_3 \end{aligned} \tag{6.3}$$

The core material is 3C97, which is suitable for the switching frequency within 100 kHz – 400 kHz under 60 ˚C to 140 ˚C. The core loss density of this material at 400 kHz, 50 mT, 100 ˚C is 100 kW/m^3, smaller than that of other ferrite material under the same condition, rendering a small core loss.

To adopt the litz wire in the transformer under high switching frequency, more than skin effect should be taken into consideration [92]. With 400 kHz switching frequency, the skin depth is 100 μm for copper. To this end, the litz wire with the strand size AWG 44, 46 48 are selected as the candidates, whose strand diameter is 50.8 μm, 40 μm and 32 μm respectively. For the small strand size, the bundle AWG is limited by the cost and complexity. In the design, the bundle size is fixed to AWG 18, which is equivalent to 400 strands of AWG 44 (44/400), 640 strands of AWG 46 (46/640) and 1000 strands of AWG 48 (48/1000). To conduct the high current, several litz-wire bundles have to be paralleled, illustrated in Fig. 6-4. The number of the paralleled bundles $N_{parallel}$ is dependent on the core window size and the bundle diameter. Due to this configuration, each bundle of one turn suffers from the different magnetic field distribution, which is hard to predict using the theoretical calculation. In this work, 2D FEA simulation using Maxwell is applied to explore the magnetic field change in the different working operation in each bundles.

6.2 Transformer model and optimization

6.2.1 Inductance and core loss model

Based on the magnetic circuit for the structure in Fig. 6-5, the inductance matrix of the transformer can be derived in (6.4)(6.5), where R_a, R_b are calculated in (6.2). Equation (6.4) and (6.5) refer to the transformer model in The magnetizing inductance L_m and the leakage inductance L_k can be calculated in (6.6)(6.7).

$$\begin{bmatrix} v_p \\ v_s \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} di_p/dt \\ di_s/dt \end{bmatrix} \tag{6.4}$$

$$L_{11} = \frac{{N_{1P}}^2 + {N_{2P}}^2}{R_a} + \frac{2N_{1P}N_{2P}}{R_b}$$

$$L_{12} = \frac{N_{1P}N_{1S} + N_{2P}N_{2S}}{R_a} + \frac{N_{1P}N_{2S} + N_{2P}N_{1S}}{R_b} \tag{6.5}$$

$$L_{22} = \frac{{N_{1S}}^2 + {N_{2S}}^2}{R_a} + \frac{2N_{1S}N_{2S}}{R_b}$$

$$L_m = nL_{12} \tag{6.6}$$

$$n = \frac{N_{1P} + N_{2P}}{N_{1S} + N_{2S}}$$

$$L_{kp} = L_{11} - nL_{12}, L_{kS} - \frac{L_{12}}{n} \tag{6.7}$$

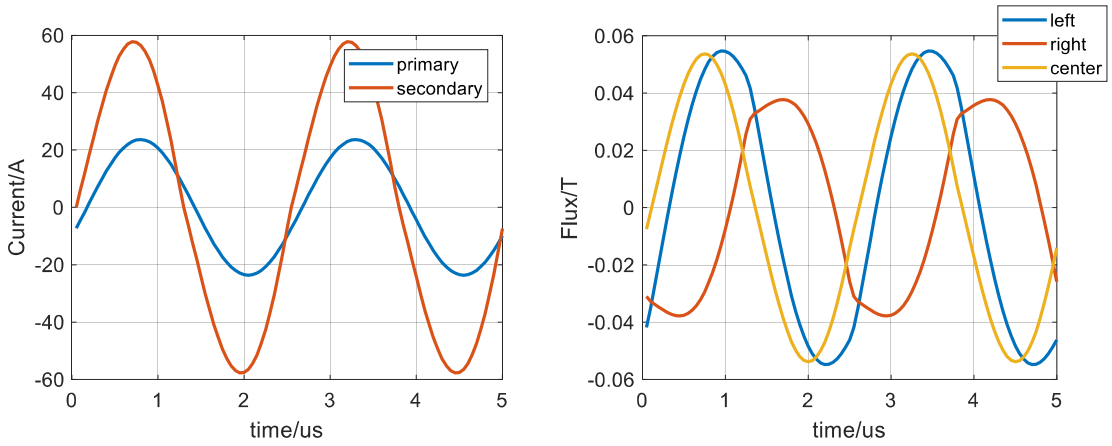
$$L_k = L_{kp} + \frac{n^2 L_m L_{kS}}{L_m + n^2 L_{kS}}$$

To estimate the core loss under different operation condition with different switching frequency considering the transient flux change, the improved generalized Steinmetz equation [97] is adopted here, which is illustrated in (6.8), where k_1, α, β are referring to the constants used in the Steinmetz equation, provided by the core manufacture. To use the improved generalized Steinmetz equation, it is necessary to calculate the transient flux density in the core under different current excitation. For example, when the LLC resonant converter operates with the resonant frequency, the primary and secondary winding current I_P I_S are in sinusoidal waveforms shown in Fig. 6-7 (a), the flux and the flux density in each leg can be calculated with (6.3), shown in Fig. 6-7 (b). With (6.8), the core loss is estimated for each leg and the total core loss in this case is 16.7 W, close to the estimation using Steinmetz equation in (6.9) [95]. When the switching frequency of the LLC resonant converter is lower than the resonant frequency, the transient current I_P and I_S are not in sinusoidal waveforms, such as the waveforms in Fig. 6-8 (a). The flux density in each leg with this current excitation are illustrated in Fig. 6-8 (b), which includes sub-harmonic and high frequency distortion. The core

loss calculated with (6.8) in this case is 65.8 W, which is 50% higher than the value 43.29 W using (6.9).

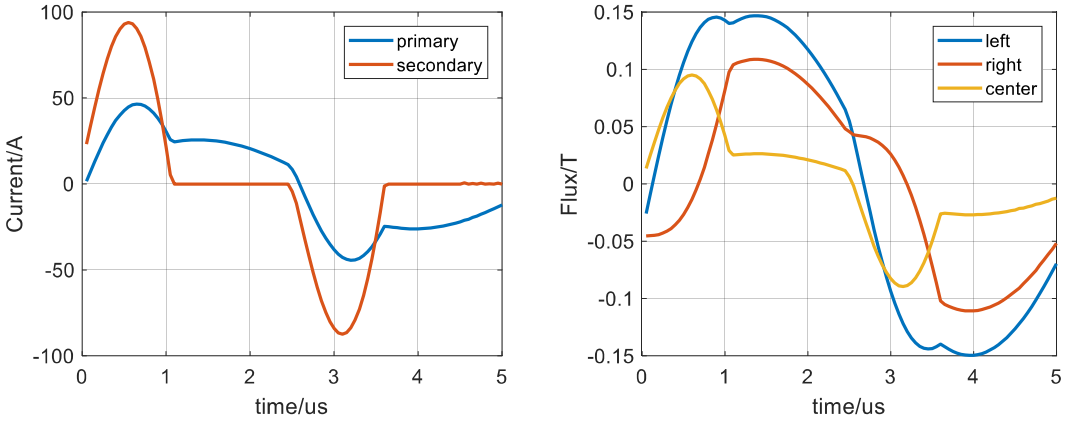
$$\left\langle P_v(t)\right\rangle = \frac{1}{T}\int_0^T k_1 \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\, dt \tag{6.8}$$

$$P_v = C_m f^{\alpha} B^{\beta} \tag{6.9}$$



(a) (b)

Fig. 6-7 (a) Primary and secondary current when $f_{sw}=f_r=400$kHz (b) corresponding flux density in each leg of the core (N_{1P} = 5, N_{2P} = 3, N_{1S} = 1, N_{2S} = 2, w = 14.5mm, c = 60mm, L_m = 33μH, L_m/L_r =5)



(a) (b)

Fig. 6-8 (a) Primary and secondary current when f_{sw}=200kHz <f_r=400kHz, (b) corresponding flux density in each leg of the core (N_{1P} = 5, N_{2P} = 3, N_{1S} = 1, N_{2S} = 2, w = 14.5mm, c = 60mm, L_m = 33μH, L_m/L_r =5)

6.2.2 Litz wire AC winding loss model

With the assumption that the field remains constant inside the conductor, equivalent to that diameter is not large compared with the skin depth, the eddy current instantaneous power dissipation within the litz-wire windings can be estimated using (6.10) in a wire of length l_t using spatial average of the time-averaged square field derivative [94]. In (6.10), $P_{e,j}$ is time-average ac loss in winding j, N_j is the number of turn in winding j, d_c is the strand diameter, l_t is average length of one turn, $\langle \square \rangle$ is the region average, $\bar{x}$ is the time average.

$$P_{e,j} = \frac{\pi l_{t,j} N_j d_{c,j}^{\ 4}}{64\rho_c} \left\langle \overline{(\frac{dB}{dt})^2} \right\rangle_j \tag{6.10}$$

To estimate $\frac{dB}{dt}$, 2D transient FEA simulation in Maxwell is performed with the transient current excitation of the primary and secondary sides. One transient distribution of the flux density around windings is shown in Fig. 6-9. The complete winding area are separated into four parts. The transient flux density within one cycle in the Area 1is plotted in Fig. 6-10 for the condition at the resonant frequency with the current excitation in Fig. 6-7 (a). The transient flux density using the current excitation in Fig. 6-8 (a) when the switching frequency is lower than the resonant frequency is plotted in Fig. 6-11 and Fig. 6-12. It is observed that the transient flux density is highly dependent on the current excitation and the bundle position. The simulation data needs to be updated when the current excitation change, such as the change of the magnitude, the phase between I_P and I_S. In addition, $N_{parallel}$ also has an effect on the transient B, given that the shared current in each bundles is also determined by $N_{parallel}$. With

the transient flux density, the AC winding loss calculation based on (6.10) can be processed following the procedures depicted in Fig. 6-13.

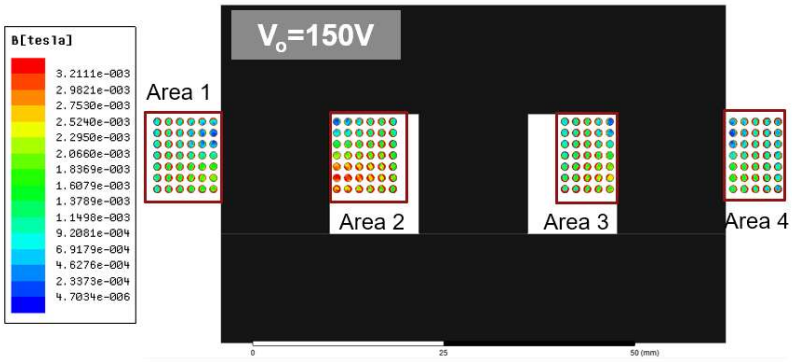


Fig. 6-9 Transient flux density distribution on the winding area when $f_{sw}=f_r=400kHz$

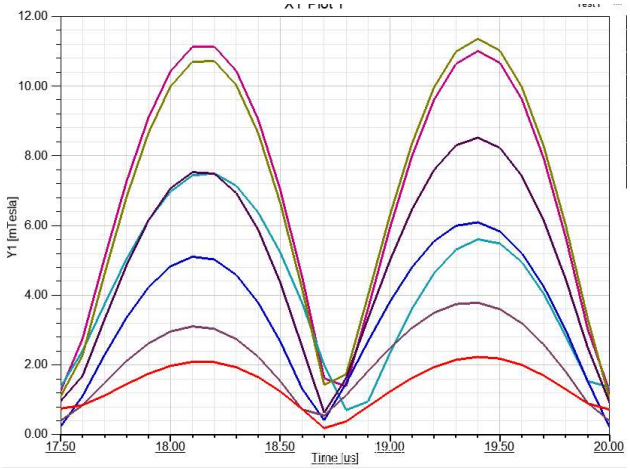


Fig. 6-10 Flux density distribution in one switching cycle of seven typical points at the winding Area 1 when $f_{sw}=f_r=400kHz$

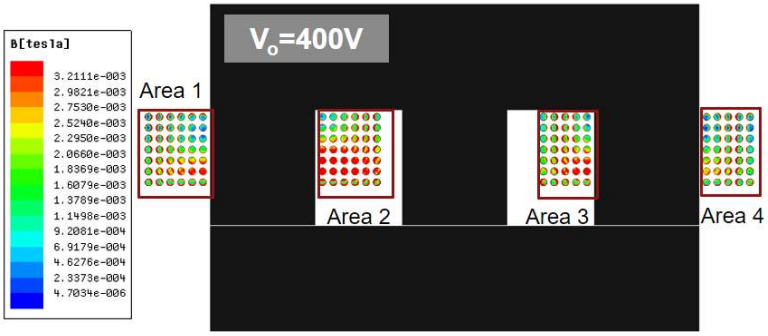


Fig. 6-11 Transient flux density distribution on the winding area when $f_{sw}<f_r=400kHz$

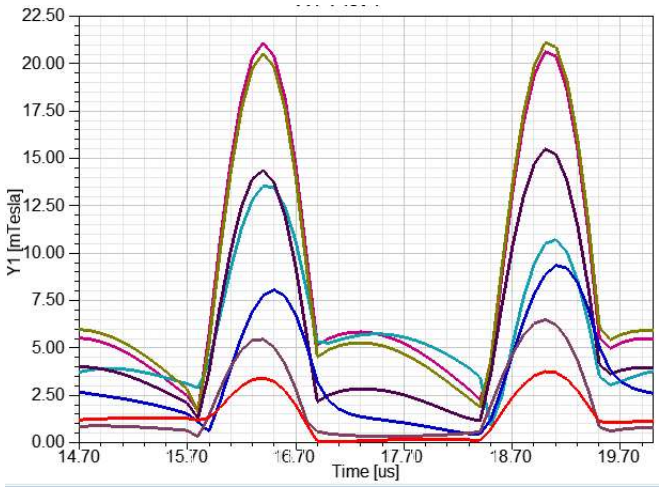


Fig. 6-12 Flux density distribution in one switching cycle of seven typical points at the winding Area 1 when $f_{sw}<f_r$=400kHz

As indicated in Fig. 6-13, the first step is to simulate the winding field with Maxwell and record the transient flux density along the time for every bundle. Due to limited process capability of Maxwell, not all of the data can be saved and plotted. Therefore the area in Fig. 6-9 is separated into several regions, seven in Area 1, seven in Area 2, six in Area 3 and six in Area 4. In each region, the region average B is plotted and recorded. The rest of the data processing is performed in Matlab. With the transient B, the $\frac{dB}{dt}$ at each time step is calculated. Then the spatial time-average for each region is then calculated, based on which the spatial area-average is calculated. Finally, the total ac winding loss is calculated based on (6.10).

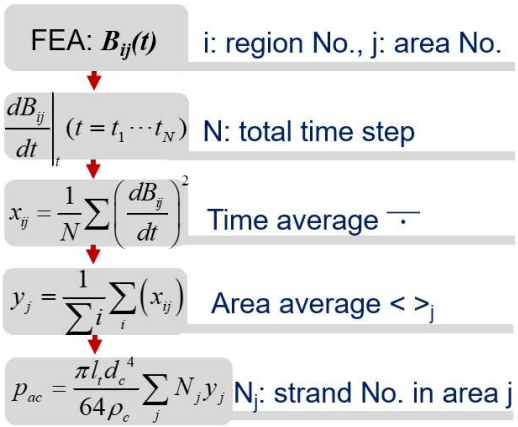


Fig. 6-13 AC winding loss calculation process based on (6.10)

Furthermore, the litz-wire selection is finalized based on the winding loss estimation. The DC winding loss can be easily calculated based on the DC resistance of the windings, which is the same for the three candidates (44/400, 46/640, 48/1000) thanks to their same bundle AWG. With seven bundles paralleled, the DC loss is 2.63 W at the resonant frequency. With (6.10) and the flux density distribution in Fig. 6-10, the AC winding loss is estimated for the three candidates under different switching frequency with sinusoidal current excitation, whose results are plotted in Fig. 6-14. In Fig. 6-14, it is observed that AC winding loss dominates the total winding loss, which is highly dependently on the stand diameter and the operation frequency. With (6.10), it can be furthermore concluded that when the strand diameter decreases by half, the AC winding loss can be reduced to 1/16. With the switching frequency increasing by x times, the AC winding loss increases by x^2 times. In order to minimize the winding loss, 48/1000 is finally selected thanks to its minimum loss among the three candidates.

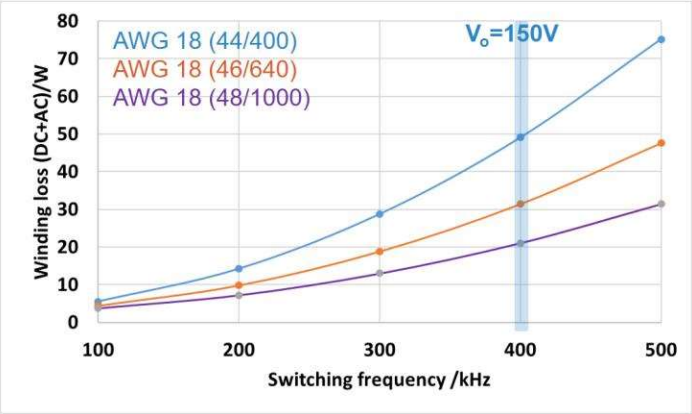


Fig. 6-14 Effect on winding loss from the litz-wire strand diameter

6.2.4 Optimization

With the models above to quantify the relationship between the transformer dimensions and the inductance, core loss, winding loss, the optimization is performed on the transformer parameters targeting the high power density and high efficiency for the converter.

To describe the transformer, the related parameters are illustrated in Fig. 6-4. The turns ratio n of the transformer is fixed to 8:3 in order to put the resonant frequency at the condition 'V_o=150V'. To have an asymmetric distribution of the primary and secondary windings, N_{1P}, N_{2P}, N_{1S} and N_{2S} are selected to be 5, 3, 1 and 2 respectively. The resonant frequency is selected to be 400 kHz and L_m is optimized to be 33 μH based on the design guide in [80]. To regulate the output voltage from 150 V to 500 V within 200 kHz – 400 kHz switching frequency range, the ratio L_m/L_r is simulated to be smaller than 7 and larger than 2. The air gap l_g, l_{g_r} are limited with the given L_m, L_r and core dimension. Among the core dimensions, the core height b is fixed to 45 mm, which is the height as the switching cell so that the vertical space of the converter is fully utilized. To avoid the core saturation, the cross area of each leg (w*c) should be larger than 500 mm^2. To this end, w ranges from 10 mm to 18 mm and c is within 50 mm to 65 mm.

The optimized parameters of the transformer are the ratio L_m/L_r, w and c. The optimization target is the Pareto front between the converter efficiency and power density. The optimization process is performed following the procedures in Fig. 6-15 using Matlab. With a given ratio L_m/L_r, the transient I_P, I_S, the rms current of I_P, I_S, the primary turn-off current are simulated. The simulation is performed instead of the calculation given that the accuracy of the calculation is poor when the switching frequency is lower than the resonant frequency. With the core dimension w and c, the air gap for each leg can be calculated using (6.1) - (6.7), with which

the flux in each leg can be calculated using (6.3) and the corresponding core loss is calculated using (6.8). As for the winding loss, $N_{parallel}$ is determined first. The dc resistance of the winding is easily estimated then. The winding flux density distribution is simulated and the corresponding AC winding loss can be calculated as the explanation above. The device conduction loss and switching loss are estimated based on the simulated current value. The efficiency under the five selected studied operating points can be estimated. As for the converter volume, which is also affected by the transformer dimension, it can be estimated using (6.11) based on the assembly method depicted in Fig. 6-16, where the dimensions are in mm. As a result, the efficiency and the converter power density for each design point is output and plotted in one figure, featuring a Pareto-front between the two design targets.

$$V = b(c + 40mm)(a + 4I_{HS} + 100mm) \ (\text{mm}^3) \tag{6.11}$$

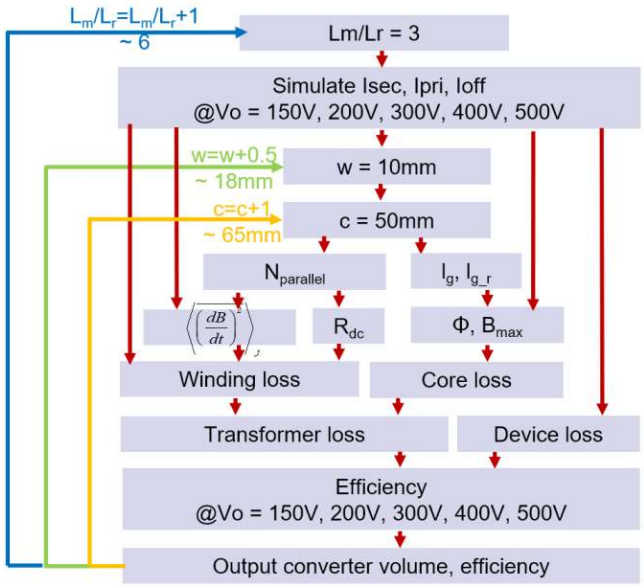


Fig. 6-15 Optimization process of the litz-wire transformer

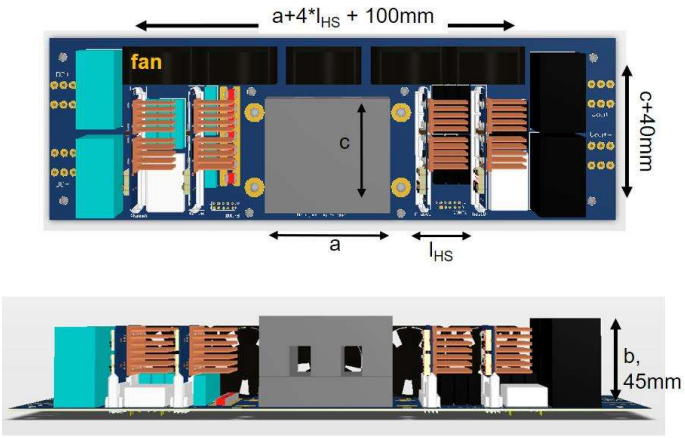


Fig. 6-16 Illustration of the 10 kW GaN-based LLC resonant converter hardware structure

Fig. 6-17 illustrates the Pareto front between the power density and the maximum estimated efficiency among the five operating conditions. One design on the front featuring 'Lm/Lr=4, w=14.5 mm, c=59 mm' is selected as the final design. The maximum estimated efficiency is 98.05% and the estimated power density is 131 W/in3 (8 kW/l). The Pareto front between the power density and the minimum efficiency among the five operating points is shown in Fig. 6-18, where the selected design above is also found to be on this front as well. The minimum estimated efficiency among the five operating points is 97.6%.

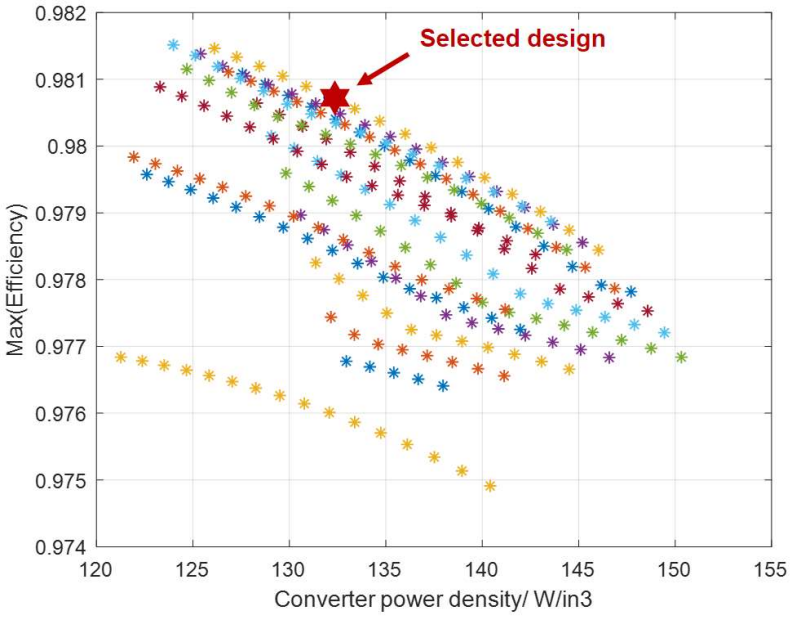


Fig. 6-17 Maximum efficiency within 5 operating points vs converter total power density

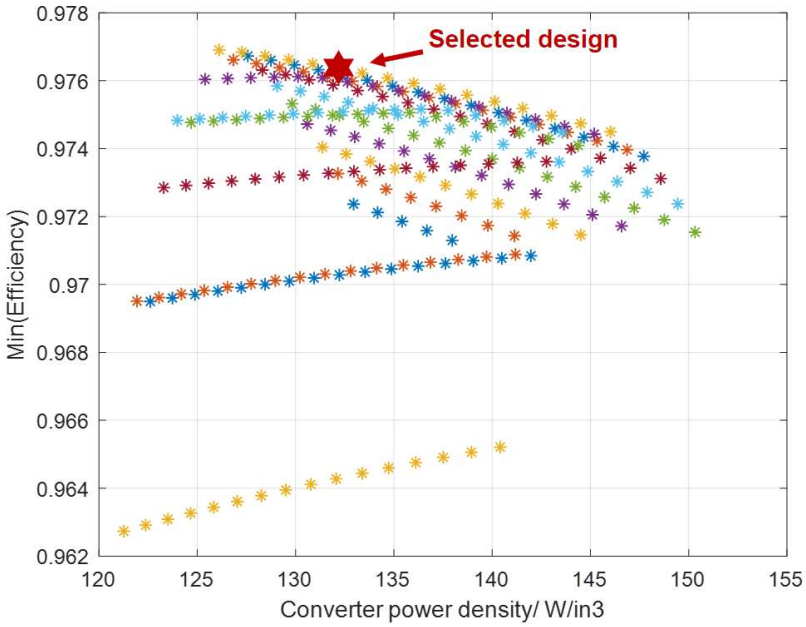


Fig. 6-18 Minimum efficiency within 5 operating points vs converter total power density

With the optimization, the effect of the transformer parameters on the converter loss can also be assessed. For example, with the different transformer dimension w an c, the estimated core loss and winding loss are shown in Fig. 6-19 for the condition 'V_o=150V' and in Fig. 6-20 for the condition 'V_o=400V'. When w and c increase, the core cross area increase and the core loss density decreases rendering a smaller core loss. On the contrary, the litz wire length increases as the result of the increased w and c, the winding loss increases. It is observed that when the output voltage is low with a high switching frequency, the winding loss dominates the transformer loss. With a high output voltage under a low switching frequency operation, the core loss dominates the transformer loss due to the increased voltage second applied on the core.

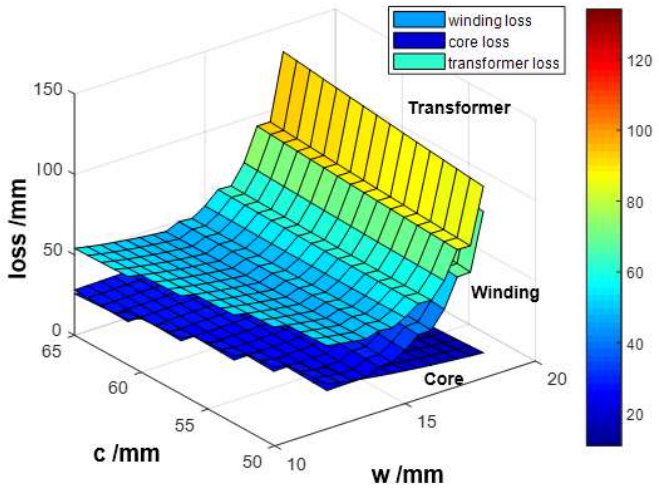


Fig. 6-19 Effect from the transformer dimensions on the transformer loss when V_o=150V, f_{sw} = 400 kHz

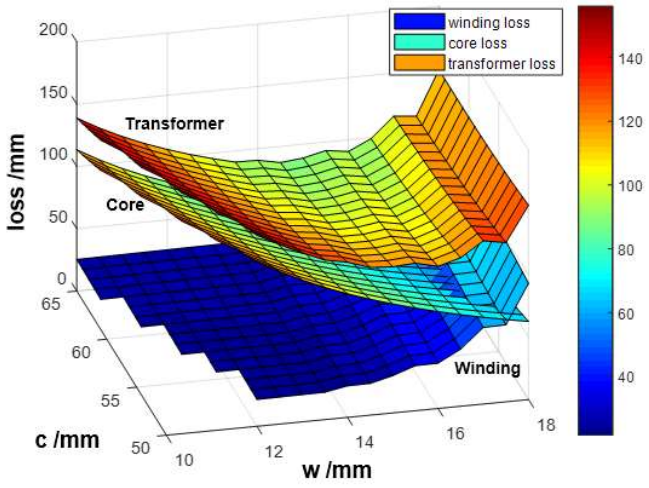


Fig. 6-20 Effect from the transformer dimensions on the transformer loss when V_o=400V, f_{sw} = 200 kHz

The rms of the secondary current with the different ratio L_m/L_r is estimated as well, shown in Fig. 6-21, which has a big effect on the device loss, shown in Fig. 6-22. The effect on the transformer loss from the ratio L_m/L_r can be also observed in Fig. 6-22, where the worst case is the condition with the highest output voltage. In this condition, the core loss is dominant in the transformer loss.

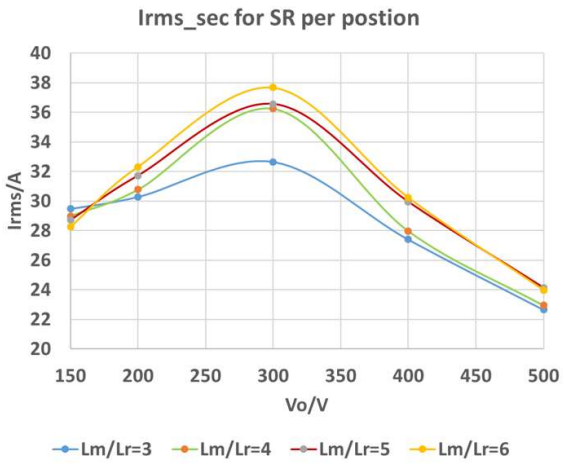


Fig. 6-21 L_m/L_r effect on the secondary rms current

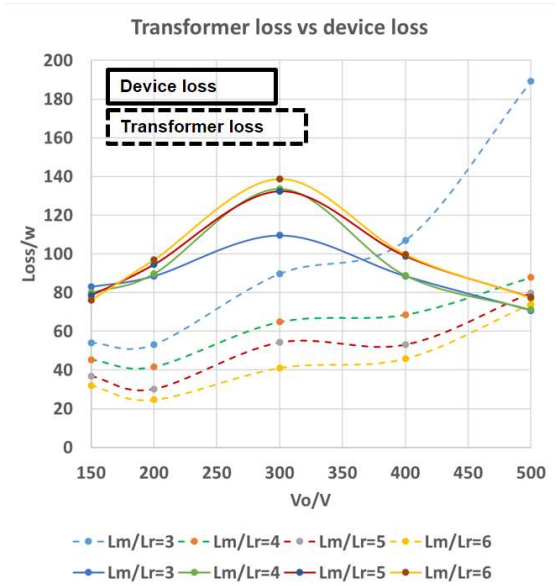


Fig. 6-22 L_m/L_r effect on the transformer and device loss

6.3 Experiment Results

6.3.1 Converter design using the switching cell of the paralleled GaN

The fabricated transformer of the selected design in Fig. 6-17 is shown in Fig. 6-23. The litz wire is crossed in the front view because there are the primary and secondary windings at the both side legs. The GaN-based LLC resonant converter is shown in Fig. 6-24, which includes two primary half-bridges, two secondary half-bridges, the litz-wire transformer, the

resonant capacitor, the input, output film capacitors and the fans. To fully utilize the space within the converter, the switching cells, the transformer, the fans, the large input and output capacitors share the same height. In addition, the resonant capacitor, the small film input and output capacitors locate in the space under the switching cell heat sink. On the mother-board of the converter, one of the fan locates next to the transformer to cool the litz-wire in the core window and the core center leg. The converter size is 278 x 100 x 45 mm, rendering a 131 W/in^3 (8 kW/l) power density.

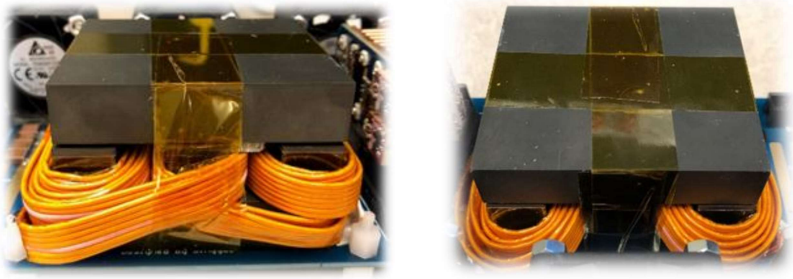


Fig. 6-23 Front and back view of the designed transformer

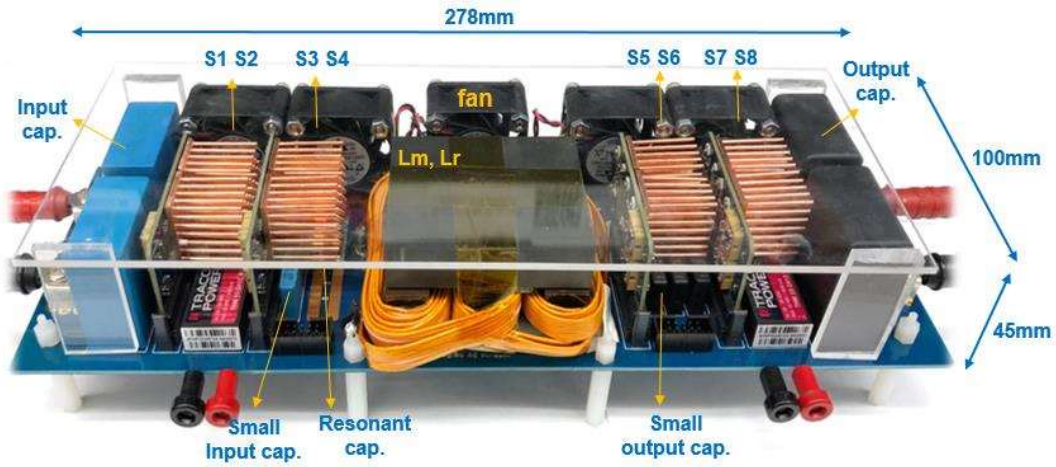


Fig. 6-24 GaN-based LLC resonant converter with the designed litz-wire transformer

6.3.2 Efficiency measurements

The experimental waveforms are shown in Fig. 6-25. Fig. 6-25 shows the primary V_{ds_pri}, the secondary SR V_{ds_SR}, the transformer primary-side current I_{pri}, and the output voltage V_{out}

under 150 V output voltage, 35 A output current and 400 kHz switching frequency. The efficiency in this case is measured to be 97.5%. With the loss break-down in Fig. 6-26, around 50% of loss is dissipated as the switch conduction loss. The transformer takes 1/3 of the total loss, which is dominated by the winding conduction loss. The estimated winding loss 33.72 W shown in Fig. 6-26 is calculated based on the rms current and the measured transformer resistance at 400 kHz using the impedance analyzer (in sinusoidal excitation). This value is close to the estimated winding loss 29.2 W using the method described above, verifying the feasibility to calculate AC winding loss using the simulated flux density distribution.

Fig. 6-27 shows the waveforms for the condition 'f_{sw} =205kHz, V_o=440V'. The efficiency in this case is measured to be 97.6%. The efficiency over the wide output range is plotted in Fig. 6-28, where the peak efficiency is 97.9%, contributed by the low switching loss, the low on-resistance using the paralleled GaN HEMTs and the fully-optimized transformer design. Furthermore, the 3D package of the LLC resonant converter helps to increase the converter power density by fully utilizing the vertical space with the converter.

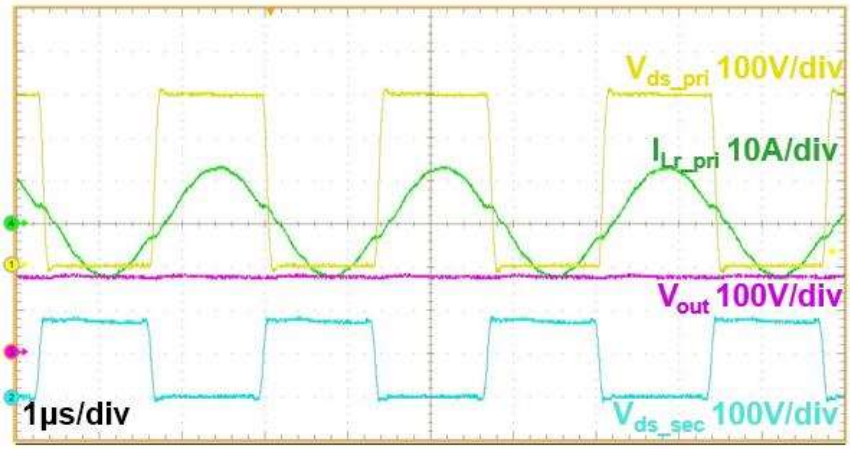


Fig. 6-25 Experimental results of the GaN-based LLC resonant converter: f_{sw} =f_r= 400kHz, V_o=150V

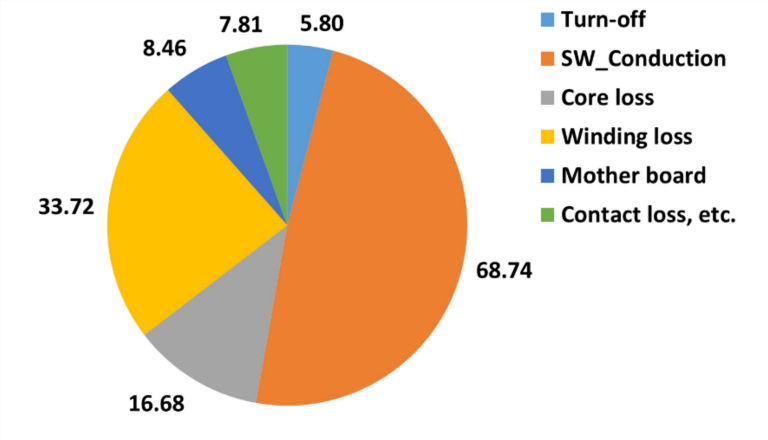


Fig. 6-26 Loss break-down for the condition 'f_{sw} =f_r= 400kHz, V_o=150V'

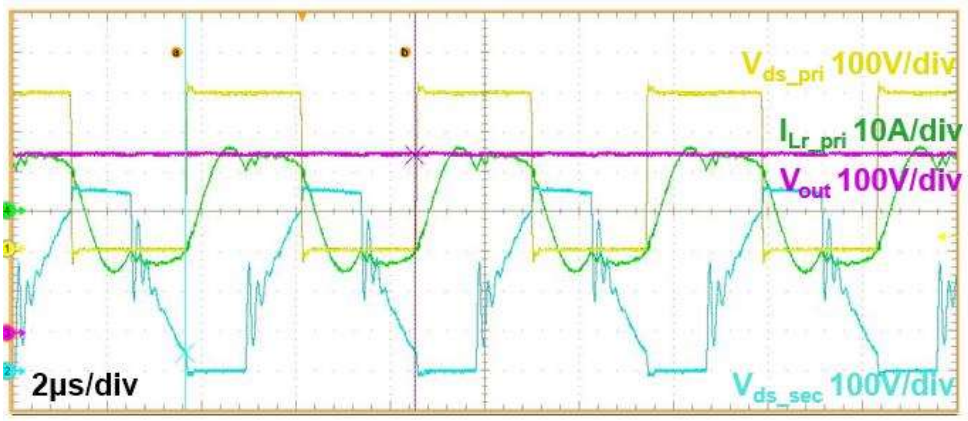


Fig. 6-27 Experimental results of the GaN-based LLC resonant converter: f_{sw} = 205kHz, V_o=440V

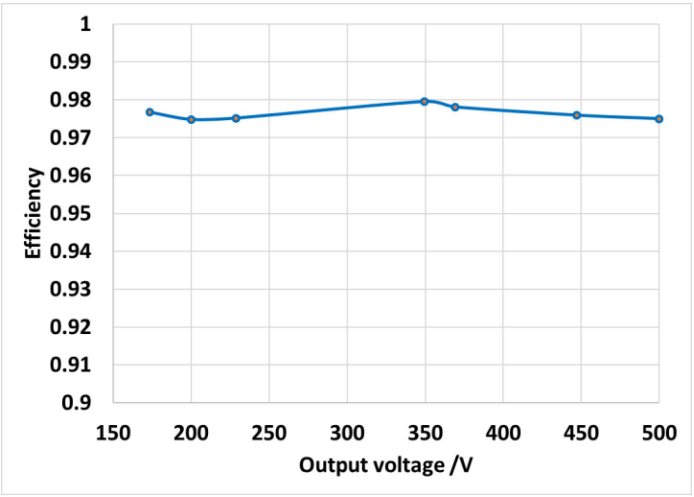


Fig. 6-28 Measured efficiency over wide output range

6.4 Summary and conclusions

In this chapter, a litz-wire transformer was came up with for a high switching frequency GaN-based LLC resonant converter, which integrated the large resonant inductor with the transformer. The model of the inductance, core loss and winding loss were described in detail, with which, an optimization was performed to find the design featuring the highest efficiency design with a given power density. One design point on the Pareto-front was selected and tested with the GaN HEMT switching cells. With the optimized transformer, the LLC resonant converter achieved 97.9% peak efficiency and 131 W/in3 (8 kW/l) power density.

With the work, it was found that the core loss of the designed transformer should consider the transient flux density change over one switching cycle rather than applying the conventional Steinmetz equation. To adopt the litz-wire in the high frequency transformer design, it requires more than the skin depth into consideration. The AC winding loss can be effectively reduced by a small stand gauge. Proper strand number needs to be considered during the optimization.

Chapter 7. Conclusions

Thanks to the advantages of the material property of GaN compared with Si, given a voltage rating, the GaN HEMT owns a smaller on-resistance with a faster speed. To this end, GaN HEMTs are taken as an emerging replacement of Si devices in various applications, such as power supply design, motor drive, and EV chargers. The e-mode 650 V GaN HEMT from GaN System featuring a small on-resistance and small junction capacitors is one of most competitive candidates in this voltage rating. To adopt the HEMT in question in the power converter design, there are several high-frequency oriented challenges, including narrow gate operating range, increased EMI emissions in the gate loop and power loop, possible high-frequency oscillation while the devices are paralleled for high conduction current. The thermal management for this small-footprint device is also critical. This dissertation was developed to address all of above challenges and provided guidelines to adopt the GaN HEMT in question in the hard-switched and soft-switched power converter to pursue high power density and high efficiency simultaneously.

In the PCB layout using the GaN HEMT in question, the primary concern is to minimize the gate and power loop inductance to reduce the V_{gs} and V_{ds} oscillation. One of the effective methods is to use the overlapped PCB layers helps to achieve flux cancellation. The orthogonal power loop to the PCB plane can reduce its inference to the gate loop which is horizontal to the PCB plane. When the HEMTs are paralleled, the symmetry is also necessary to ensure the current balancing. Q3D Extractor cooperated with AnsoftLink can estimate the parasitic inductance from the PCB traces, in favor of quantifying the effect from the parasitics from the PCB layout.

The large EMI emissions circulated in the gate and power loop within the GaN-based converter with a high switching frequency was observed, and it is expected to be contained in the converter itself to avoid influence to other neighbor electronics. In the gate drive, the control, the sensing circuitry, or other circuity using auxiliary power supplies, a high-impedance barrier needs to build between the power stage and the auxiliary circuitry ground. The easiest way to realize 'high-impedance barrier' here is to adopt an isolated auxiliary power supply with ultra-low isolation capacitance. To design an auxiliary power supply with low isolation capacitance, there are also multiple ways to pursue high power density, such as, by employing a higher switching frequency or embedding magnetic into PCB material as the substrate of the circuit layer. In the power stage, the EMI filter is the most common way to attenuate EMI emissions, whose volume is determined by the noise sources and the EMI propagation path. The former is increased with a higher switching frequency and its high frequency portion gets even higher when a high dv/dt is generated by WGB devices. It was concluded that with a higher switching frequency, the DM EMI filter volume can be reduced but the CM EMI filter volume would increase. As for the increased EMI emission above 10 MHz due to the high dv/dt from the GaN HEMTs, the active gate driver proposed in the dissertation can change the dv/dt in order to attenuate the high frequency EMI emission with less penalty of switching loss from the 'slowed-down' dv/dt.

To adopt the GaN HEMTs in question in the converter, the small thermal pads allows only small loss dissipated within the device. To reduce the thermal resistance from the device to the ambient, several different heat sink designs were come up with in the dissertation, such as the single-PCB-side, double-PCB-side heat sink, insulated and non-insulated heat sink. To properly design the heat sink, its thermal resistance should be estimated first based on the estimated device loss, with which the smallest heat sink volume to control the device

temperature can be calculated. In the dissertation, an experimental approach to evaluate the heat sink thermal resistance was shown, with which the experimental device loss can be accurately quantified.

With the potential issue solve above to adopt the GaN HEMTs, the devices are ready to operate with a high switching frequency. In the three-phase two-level inverter, it was found that with a higher switching frequency, the switching loss increased significantly rendering a decreased efficiency. With an air-cool heat sink, the heat sink volume also increases, leading to a deceased power density. However, in the power supply design, the high switching frequency can reduce the voltage-second applied on the magnetics and capacitors, which transfer and store energy, enabling a volume reduction of these passive components and a higher power density of the power supplies design. To design a high-frequency transformer with litz wire, proper litz wire loss estimation method should be used. The transient FEA simulation can be used to predict the transient magnetic flux change in the winding areas, which helps to estimate the AC winding loss when the current excitation is not sinusoidal and the flux distribution is complex. The litz wire selection and construction for high switching frequency operation consider more than the skin effect. To reduce the loss from the proximity effect, one of the effective way is to use the strand with a much smaller diameter than the skin depth. Furthermore, the integration and optimization of the magnetic structure is also necessary in order to build a high-efficiency and high-power-density power converter.

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